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Packaging of Two Dimensional Optoelectronic Device Arrays for Optical Backplanes

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Abstract

The use of existing packaging techniques for microelectronics are studied in terms of their applicability to the packaging of optoelectronic device arrays for photonic interconnect applications. In particular, the packaging of smart pixel arrays for free-space optical backplanes is quantitatively explored. This assessment is made from three basic perspectives: thermal management capabilities, connectivity and bandwidth, and alignment to a free-space optical system. In the assessment, a smart pixel array design space analysis is derived which shows that, by constraining the smart pixel array characteristics, the use of existing packaging technologies is possible. This leads to the derivation of expressions which relate both system and smart pixel array parameters to representative packaging parameters. It is seen in the analysis that while the thermal management imposes constraints on the window size, smart pixel density and size, the alignment imposes constraints mostly on the window size. The architectural characteristics of the smart pixel array are mostly affected by the connectivity and bandwidth of the packaging technology.

The integration of packaged smart pixel arrays into optical backplane demonstrators is also discussed, and the design and implementation of an optical backplane demonstrator is presented. This is complemented by the design, implementation and characterization of an optomechanical assembly which uses the interface between a single chip carrier and a socket to provide means of alignment in three degrees of freedom. Prealigned and modular plug-in device array integration is demonstrated.

Résumé

L'utilisation des techniques courantes pour l'assemblage des circuits intégrés est étudiée en fonction de leur applicabilité pour l'assemblage des matrices de dispositifs opto-électroniques dans le cadre d'interconnections photoniques. Ces études touchent particulièrement l'assemblage des matrices de pixels intelligents dans la réalisation de plaques de raccordement arrières optiques. Trois critères sont considerés dans cette évaluation: les possibilités de gestion thermique, le nombre d'interconnections et la largeur de bande, et l'alignement à un système optique. Cette évaluation mène à une analyse des paramètres de conception des pixels intelligents. Cette analyse des paramètres de conception permet l'utilisation de techniques courantes pour l'assemblage opto-électronique en imposant des contraintes sur les caractéristiques de la matrice de pixels intelligents. La formulation d'expressions mathématiques rattachant les paramètres du système et les matrices de pixels intelligents aux paramètres critiques de l'assemblage opto-électronique est aussi obtenue. L'analyse démontre que la gestion thermique influence la grandeur des fenêtres opto-électroniques, la densité de pixels intelligents dans la matrice, et la grandeur de cette matrice, tandis que l'alignement a un impact plus important sur la grandeur des fenêtres opto-électroniques. Les caractéristiques architecturelles de la matrice de pixels intelligents sont surtout influencées par le nombre d'interconnections et la largeur de bande de la technique d'assemblage utilisée.

L'intégration de matrices de pixels intelligents assemblés dans un demonstrateur de plaque de raccordement arrière optique, ainsi que la conception et la réalisation de ce demonstrateur sont aussi présentées. Ce demonstrateur est complemente par la conception, la réalisation et la caractérisation d'un assemblage opto-mécanique qui utilise l'interface entre le boîtier et le receptacle de façon à pouvoir obtenir trois axes d'alignement. Le pre-alignement et la modularité sont aussi demontrés.

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Table of Contents

Chapter 1

Introduction and motivation

1.1 Introduction

As the requirements on multiprocessor computing systems, large ATM switching systems and even synchronous telecommunications systems become more stringent and more demanding, driven by the ever growing needs of our society, the performance of such systems needs to improve at unprecedented rates. Performance parameters, other than the ones inherent to the individual components of the system, are the system speed and system interconnectivity. The interconnectivity between discrete components within the system is provided by their packaging, and is defined at different levels or hierarchies. These levels of packaging provide die to die, module to module, board to board and sub-system to sub-system connectivity, and partly define the physical layer of the system, where the component's electrical and mechanical support is implemented (such as connectivity, power supplies, physical integration structure and thermal management facilities). It is evident that as systems grow larger architecturally, their physical size must remain the same in order to preserve performance parameters (such as delays, speed of operation, etc.) the same, or to better them, resulting in highly compact systems with interconnection bottlenecks and large heat dissipations. These bottlenecks will occur at the highest level in packaging hierarchy, where the largest amount of information travels: the backplane[1]. The current technological approaches for this interconnection, namely those related to electrical backplanes are starting to fail to keep up with the growth and developments of microprocessor systems. In a similar fashion, future application for telecommunications, such as B-ISDN and large ATM switches, are seen to be limited by the electrical interconnection approach[2].

It is believed that transport of data signals can be advantageous if performed at the photonic layer because of the high speed and large connectivities that can be achieved[3][4]. Long distance communications over waveguide structures, namely optical fibers, has developed dramatically over the past 30 years and has directed the attention of the telecommunications and computing industry towards the use of photons instead of electrons where it proves advantageous to do so. This has resulted in a great deal of

research effort being dedicated towards the integration of electronics and optoelectronic devices. In addition, systems research has complemented these efforts and built upon them to demonstrate the potential of optical interconnects, particularly for optical backplanes [5],[6],[7],[8],[9].

The following section will define the concept of a backplane, and will outline the predicted capabilities of optical backplanes. Section 1.3 will describe the smart pixel array and will formulate the packaging problem by outlining the characteristics and properties of existing packaging technologies and their applicability to optical backplanes. Finally, the scope and outline of this thesis will be presented in section 1.5.

1.2 Definition of a backplane

A backplane is an interconnect module located and contained in the back panel of a board shelf within a bay or chassis. It constitutes the highest level of packaging in a system, and provides the support and connectivity between cards or boards. In most cases, these cards or boards contain switching nodes, processors, and need to be have removal and reinsertion capabilities. This is illustrated in Figure 1.1. Electrical backplanes provide point to point connections, implemented in hardware through traces on a board, or discrete wiring embedded in a module, and are non-reconfigurable. Thus, the slot assignment for the specific boards is fixed, and the backplane is designed as a function of the board functionality.

Current backplane standards can support aggregate capacities in the Gbits/s range[10], however they are becoming limited by the technologies they employ. This result depends as much on the performance of the board to backplane interface connectors, as it does on the properties within the backplane, such as maximum line density and line speed. The cost of implementing such panels becomes increasingly high as the number of I/O gets higher, since the number of module layers required to support high performance data channels increases. Furthermore, increasing the aggregate capacity of the backplane must be done by reaching a compromise between speed and number of interconnections. High speed lines not only require tight control in their impedance and length, but also require the line density to be limited to certain values, dependent on the properties of the lines in

the module. At the connector level, this is manifested as the signal lines needing to be interleaved with ground lines to preserve signal integrity, resulting in limited I/O.

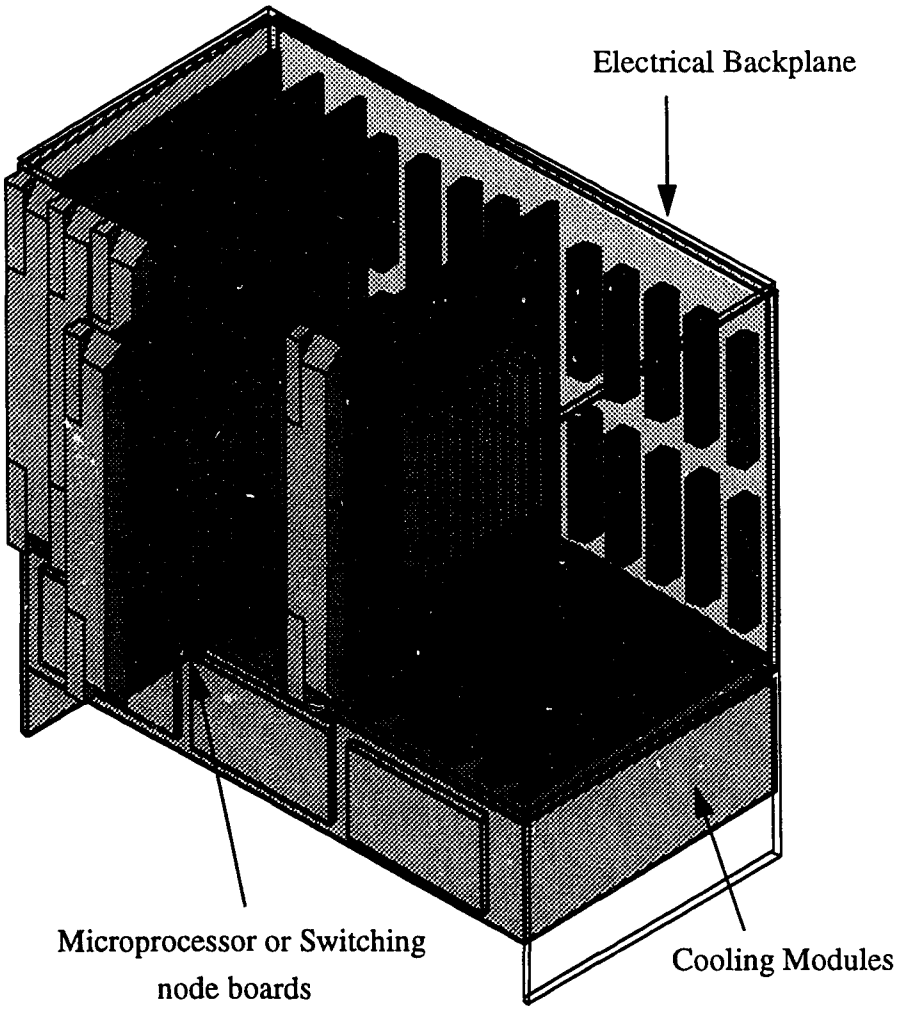

Figure 1.1 - Board rack or chassis showing the way electrical backplanes interconnect boards to one another.

The advantages of using optical channels to transport data signals lies in the high bandwidths that can be achieved for large density interconnections of optical channels. These channels can be, in addition, arranged in a two dimensional array configuration, allowing higher interconnect densities than those electrical backplanes are capable of.

Each channel in the optical backplane is an optical interconnect between two transceivers composed of optoelectronics with associated electronics, denominated smart pixels. By implementing these on a single die in a repetitive fashion, a smart pixel array

can be obtained. This smart pixel array constitutes one of the building blocks of optical backplanes and are described in more detail in section 1.2.1.

The advantages of an optical backplane, in addition to high interconnect densities and high speed (as the electronics and optoelectronics are integrated in the same substrate), is the ability to carry large amounts of information between all nodes, providing a fully connected network (Figure 1.2). This information can be then extracted at each node according to its destination, allowing reconfigurability of the interconnect[1]. This also results in a reduction between the ratio of information travelling along the backplane to that travelling out of the backplane and into each node and is illustrated in Figure 1.3.

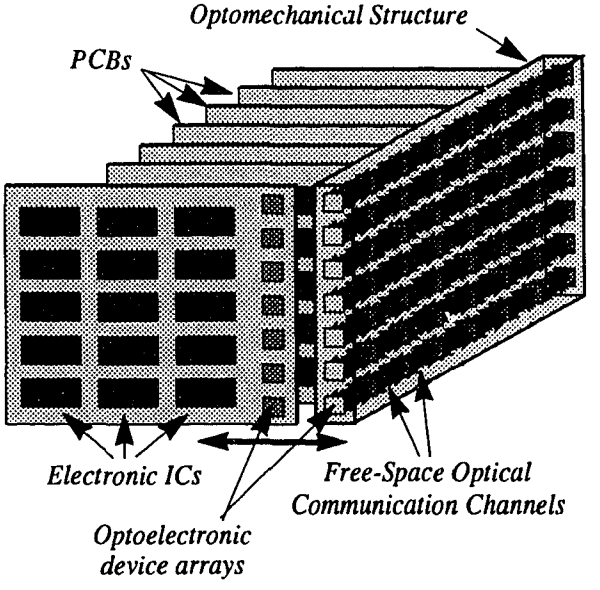

Figure 1.2 - Free space optical backplane concept (after [1]).

A question that remains is whether a guided wave approach or a free-space optics approach should be used in this backplane. Examples of the former are the schemes proposed by various research groups[11],[12]. Although guided wave structures (fibers are a good example of this) can provide nearly lossless transmission for large distances, their applicability to backplanes is limited. This because of the fact that the connection density that can be achieved becomes limited by the waveguide size (including cladding, and other mechanical support features), and the distances over which data needs to be transferred (about an inch) is too short to justify their use. In such applications, free-space optics offers greater advantages, as the density of interconnects is not limited by the

guiding wave structure, and the optical components over the inter-board separation distance can be made relatively simple. The use of a free-space approach in combination with smart pixel arrays has been the subject of extensive study within the photonics community. These smart pixel arrays will be the subject of study in this thesis from a packaging perspective and are introduced in the following section.

1.2.1 Optoelectronic devices and smart pixel arrays

As the research throughout the evolution and the applications of photonic systems has demonstrated, an optical approach to interconnection is elegant and promises to alleviate some of the problems in the transmission of data between separate system components. Its elegance relies on the fact that the optics are only part of the transport of the data signals, while the high speed electronics do the processing on die and without leaving it. It is in the process of leaving the die through I/O interfaces (of chip carriers for example) where the signals degrade the most.

In order to apply this approach to optical backplanes, two dimensional arrays of optoelectronic devices combined with microelectronic devices are needed. Each optoelectronic device can be a transmitter or a receiver and is combined with electronics for signal amplification, signal address recognition and reconfigurability, and for optoelectronic device biasing and driving. Although there is no preferred technology at present, because of the fact that most proposed technologies are at the early stages in their development, several technologies have been proposed[4],[13],[14],[15]. These approaches can be categorized in two groups: modulator based approaches and surface emitting device based systems in view of the transmitter technology used. These are discussed in more detail in chapters 2 and 4.

The technologies that will be considered throughout this thesis are Self Electro-optic Effect Devices (FET-SEED and CMOS-SEED) for modulator based systems, and Vertical Cavity Surface Emitting Lasers (VCSELs) for surface emitter device based systems. The former are more mature technologies for arrayed structures including electronics, and have been used in demonstrator systems, while the latter, although they have been used in systems in arrayed structures and have been hybridized with electronics and detectors in an array form, have not reached yet such a level of maturity.

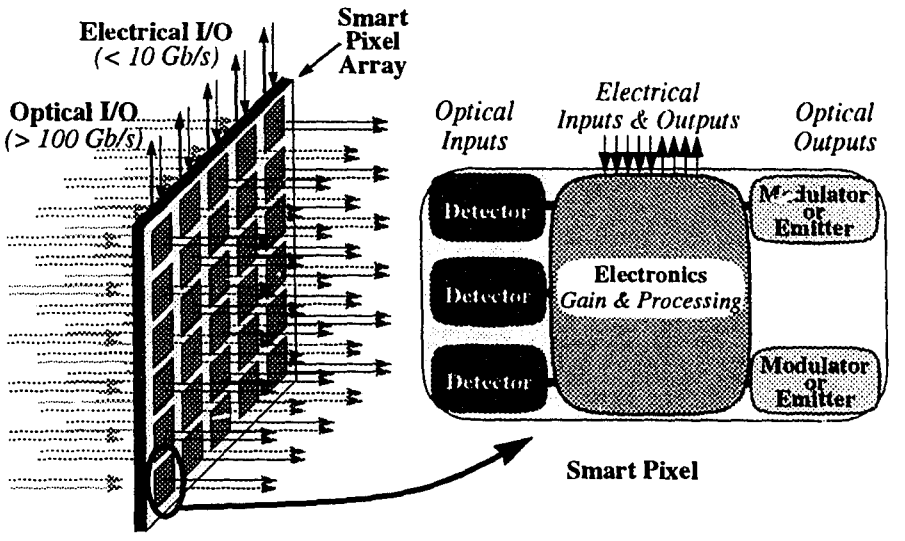

Figure 1.3 - Configuration of a smart pixel. The electrical I/O into and out of the smart pixel array is orders of magnitude smaller than the backplane aggregate throughput (after [1]).

The device arrays would be of very little use without their integration into systems, and this is done, as mentioned earlier, through the packaging. This is discussed in the following section.

1.3 Packaging of electronics and optoelectronics

The problem of packaging is a rather complex one as it makes the integration of discrete components in a system possible. As it provides a mapping between microscopic structures, such as transistors and traces on a die, onto macroscopic features, such as traces on a board or module, and interconnection interfaces, it can be very challenging. Signal properties and signal integrity need to be preserved throughout this mapping. For this the packaging of microelectronics field has devoted a great deal of effort in conceiving packaging techniques, and designing and manufacturing hardware. Such techniques have, so far, kept up with the developments in the microelectronics industry, however they are running short of breath with the new application driven developments. Package I/Os are driven to higher and higher counts and speeds. It is seen that new techniques will be needed to provide the I/O capabilities in and out of dies that are needed. One such approach is the use of die level optical I/O, and is being pursued extensively[13],[16],[17]. With these I/O capabilities, dies have more relaxed requirements on their electrical I/O, however this is dependent on the application. The packaging of smart pixel arrays for

photonic applications poses a whole new set of conditions and constraints that were not seen in the microelectronics packaging area. Such constraints are dictated by the now different on-die power dissipations, optical I/O alignment, and I/O or connectivity requirements. It is therefore desired to assess whether the existing packaging technologies (designed initially for microelectronics) will be able to support the packaging of smart pixel arrays, or whether a totally new approach to packaging must be taken.

Although work in the latter has shown that custom approaches results in compact and efficient systems for discrete devices[18], and in some cases for arrayed devices[17],[19], their design is in most cases application specific. The application of existing packaging technologies offers the benefit of using an existing and standardized infrastructure, and adapting it to support the requirements of photonic applications. It also provides a smoother transition for industry in a change from electronic to photonic technologies.

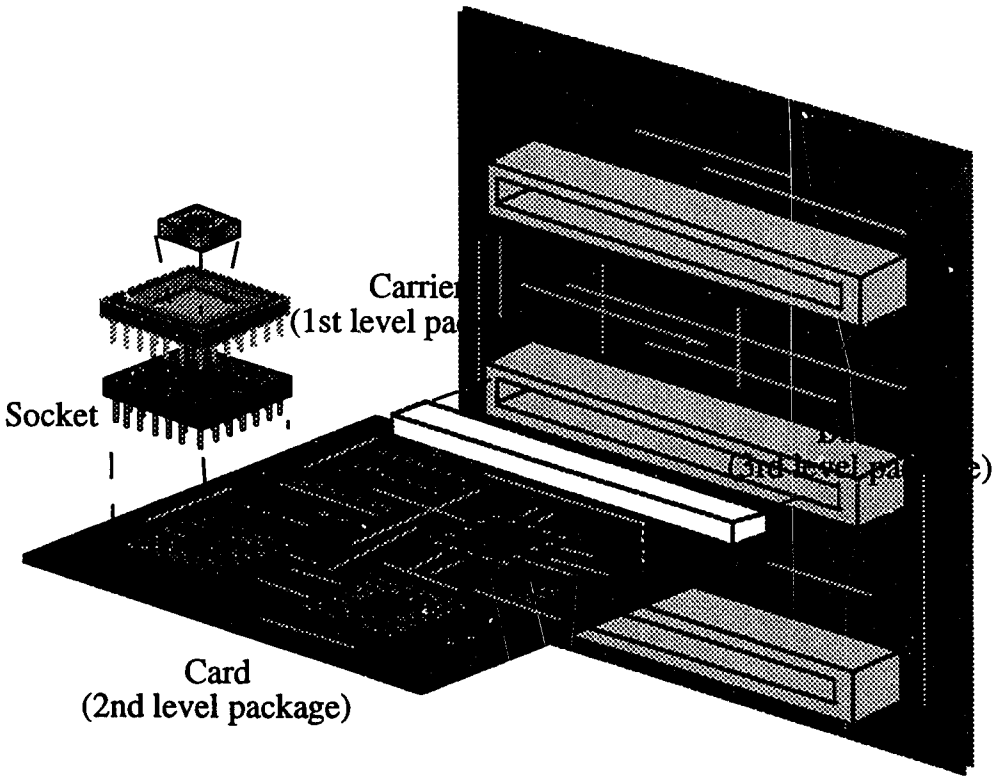

Figure 1.4 - Levels of packaging, starting with the bare die and ending in a board. The 3rd level package board can be related to the backplane of Figure 1.1.

Applying existing packaging technologies implies adding features that allow them to be useful. As is expected, this changes will not suffice, and will require a certain degree of tolerance of the device arrays in the areas constraining the packaging and that were

mentioned earlier. Such tolerance can be obtained by changing the design parameters in smart pixels and will be studied in this thesis.

For this analysis to be possible the existing microelectronic industry approaches to packaging must be assessed. The following section is an overview of such approaches and techniques, and will point to some of the properties of interest, which are developed in more detail throughout this thesis.

1.3.1 Existing packaging approaches

The microelectronics packaging industry has developed a wide range of package types that are suited to different system requirements. The I/O capabilities of such packages have increased in accordance to the levels of integration of transistors on single dies. Initial techniques, such as Dual-In-Line packages (DIP) were devised to support LSI circuitry, while VLSI circuitry imposed requirements on these packages that eventually they could not provide. The requirement on I/O lead to an increase in the size of these carriers. Since then, the trend has been to minimize the size to I/O ratio for packages. More advanced packages, such as leadless chip carriers (LCC), Quad Flat Packs (QFP) and Pin Grid arrays (PGA) increased considerably the I/O capabilities and while keeping or even reducing the on-board footprint area of the package[20],[21],[22]. This was greatly influenced by the transition from plastic packages to ceramic packages for the enhancement of both thermal and electrical properties and resulted in great developments in the packaging of VLSI circuitry[23],[24]. All these techniques considered a second level of packaging of the form of a Printed Wiring Board (PWB) or Printed Circuit Board (PCB), and in most cases involved a through hole soldered connection to this board, either by direct interface, or by interfacing through another level of packaging (such as a socket). The use of LCCs and QFPs allowed the incorporation of surface mounting, which resulted in better signal transmission performance in view of the reduced inductances. They also provided very high I/O counts, as the separation between the leads became smaller.

The leading edge single carrier packaging technology is that of Ball Grid Arrays (BGA), which incorporate surface mount to the module or board through solder reflow of solder balls in the bottom of the package[22],[25]. The connectivities that can be achieved surpass those of any other package. These packages, however, are starting to experience problems in their interface to standard FR-4 PCBs due to contact pad density.

The module technologies are developing high connectivity and high bandwidth boards, and permit direct soldering of dies on them. A particular case of this, and perhaps a hybridization between traditional single chip carrier packages, and PCBs are Multi-Chip Modules (MCM). The are three main types or categories of Multi-chip Modules available[26], MCM-L, MCM-C, and MCM-D. Of these the first two, although they differ in their wiring technology (deposited vs. embedded through cofiring), their properties are very similar in terms of bandwidth (in the GHz range) and depends mostly in the ceramic dielectric constant and wiring properties. MCM-C technology promises lower cost and higher bandwidths with the development of better ceramics. MCM-D technology uses silicon and ceramic with deposited wiring and is the most suitable for high speed applications (easily in the tens of GHz). This technology allows the implementation of thin film MCM layers[27], and allow wiring densities of up to 80% of the footprint area.

The properties of these packages and that of MCMs are discussed in more detail in chapter 3 of this thesis.

1.4 Packaging of optoelectronics in optical backplanes

As was mentioned earlier, the use of optical I/O alleviates the I/O requirements on single chip carriers and in general, on the packaging itself, as the packaging is mainly used to provide control bits, bias and support for the optical channels circuitry. This however may or may not be true for the case of optical backplanes. In such an application, the packaging is not only required to provide I/O for device circuitry support, but it must also provide I/O for the data channels that are being extracted from the optical information mainstream. This is again dependent on the application and is further studied in this thesis.

The objective of this thesis is to analyze the applicability of microelectronic packaging technologies to optical backplane applications, namely to the packaging of two dimensional device arrays. The limitations of microelectronic packaging technologies will be related to heat removal, connectivity and bandwidth and system-alignability constraints. Based upon these constraints, an analysis on how the smart pixel parameters can be modified to allow more flexibility in these constraints and the possibility of these technologies being used in optical backplane systems will be done, resulting in a

packaging constrained smart pixel array design space. In addition, the incorporation of optomechanical techniques to alleviate the alignability component of such constraints is analyzed.

1.5 Thesis organization

The thesis will start by showing the considerations and issues associated with the thermal management in the packaging of two dimensional arrays of electronics. A design space analysis will be formulated constrained by the packaging thermal management capabilities. Chapter three will investigate the connectivity and bandwidth issues in smart pixel array packaging, mainly focussing on the application of standard single chip carrier packaging techniques. In chapter 4, the alignment issues associated with the packaging of smart pixel arrays in optical interconnect systems are analyzed. This again is done from a standard packaging technology perspective, resulting in the formulation of a design space analogous to that of chapter two. This will lead, in chapter five, to a discussion of optomechanical approaches designed to complement what can be achieved through the smart pixel design space analysis of chapter four in terms of alignment. The optomechanical and packaging approaches used in the Phase II Optical Backplane demonstrator built at McGill, as well as a demonstrator assembly that complements the optomechanics of such systems will be presented in this chapter. To conclude, chapter five will summarize the design space of two dimensional arrays of optoelectronic devices as constrained by the packaging. The trade-offs between each of the areas analyzed throughout this thesis will be assessed, determining the applicability of standard microelectronic packaging technologies to the packaging of smart pixel arrays for optical backplane applications.

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Chapter 2

Thermal issues and constraints in the packaging of two dimensional optoelectronic device arrays

2.1 Introduction

It is well known that any process has heat as its end result, which flows along a temperature gradient from hot to cold. This constitutes one of the laws of thermodynamics, as well as the basis for an area in electronics that has been the subject of extensive study.

Throughout the evolution of the electronics technology over the last 20 years, the increase in integration has been dramatic. The scaling however has not been a true scaling, as voltage levels have not decreased proportionally to the size of the devices they drive, causing the on-die power to increase, as has been the case for both MOS and bipolar technologies[1]. Similarly, chips have also seen an increase in size, as well as the integration of optoelectronics with impinging optical power[2], leading to larger powers being dissipated. Chip power dissipations easily reach $100W/cm^2$[3]. Because reliable operation of both the electronics and optoelectronics on the die require junction temperatures to be kept below certain values and optoelectronic devices within a certain temperature stability range, the temperature has to be tightly controlled.

Extensive studies on the analysis that models the heat dissipation in devices has been done, as well as analysis on models to incorporate the packaging and allow the engineer to design the heat removal system appropriate to the device requirements, however the nature of the role of the packaging has always been subsequential. This role has changed in the past few years, as packaging issues are being more and more a part of the front end of the design cycle of systems[4], however, the packaging is incorporated into the design at a stage in which it has to deal with the problems that the associated optoelectronics and electronics bring along with them. It is intended in this chapter to describe some of the issues, trade-offs and considerations in the design of thermal management systems for optoelectronic devices, namely for two dimensional devices arrays. Based

upon the constraints imposed by the limitations of the thermal management systems, limitations in device array design are to be defined.

The following section will review the theory of heat diffusion. The formulation of Fourier's Law will lead to the concept of thermal resistances, and thermal contact resistances. Following, an overview of the heat dissipation in devices, and the techniques used to remove this heat will be presented. The ideas outlined in these sections will lead to models that will define the design space of two-dimensional arrays of optoelectronics, and to an analysis of the trade-offs between the parameters in this design space, as well as those related to system operation and packaging.

2.2 Heat Transfer in Solids

2.2.1 Theory

Kinetic theory states that the transfer of energy occurs at the molecular level from more energetic molecules to less energetic molecules. In thermodynamics this is represented as a flow of heat from a higher to a lower temperature[5], in a direction perpendicular to constant temperature planes. In equilibrium the rate at which heat flows, $\dot{Q}$, is given by Fourier's law

$$\dot{Q} = -KA\frac{dT}{dn} \tag{2.1}$$

where A is the cross sectional area through which heat flows, n is the normal to the area and K is the thermal conductivity of the material. The heat equation, which governs the propagation of heat in materials is expressed as

$$\nabla^2 T - \frac{1}{\kappa}\frac{\partial T}{\partial t} = -\frac{\dot{Q}}{K} \tag{2.2}$$

where $\kappa = K/\rho C$, the thermal conductivity divided by the density-heat capacity product. The right hand side term is the heat generated within the volume. Note that for steady flow the time dependent derivative goes to zero and the equation reduces to Poisson's equation.

There are three mechanisms for the transfer of heat: conduction, convection, and radiation. In the analysis of a system dominated by conduction, and with interfaces that transfer heat through different mechanisms or with different properties, the boundary

conditions can be used are the functions describing the different temperatures and fluxes at the boundaries.

The analysis of the resulting boundary value problems that arise for complex systems is computationally intensive, however a first order model can be used that simplifies the analysis in complex systems. This model, the thermal resistance model, is described in the next section.

2.2.2 Thermal Resistance

By looking at the heat equation, it can be seen that the diffusion of heat and the transport of charge are analogous. As a result, heat diffusion through systems has been modeled by methods analogous to those used in transmission line theory[6], and through network analysis analogous to that of electrical networks[10]. Most important of all, is the analogy between the thermal resistance and the electrical resistance. This thermal resistance is given by the drop in temperature over the heat flow rate[11], [12], and corresponds to Fourier's Law, which describes the heat flux in one direction. By using expression (2.2), the thermal resistance can be expressed as

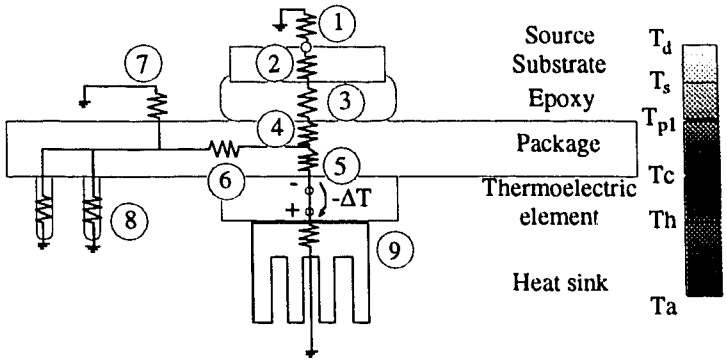
$$R = \frac{\Delta T}{\dot{Q}} = \frac{l}{KA} \tag{2.3}$$

where $l=\Delta x$, the distance through which there is a temperature drop ΔT, and K is the thermal conductivity of the material.

To a first order approximation, and for rough estimates, the model is good and can give ballpark figures on the various system temperatures. It is important to note that in most applications, heat diffusion does not occur along a linear path, resulting in thermal resistances that are lower than predicted. Such is the case for small heat sources on large substrates, or small dies on large packages. For these cases the thermal resistance is better represented by the spreading resistance, which is a function of source to heat spreader ratio and is tabulated[11].

In the analysis, the resistance circuit is obtained and parallel and series addition is performed to find the total thermal resistance of the packaged device. These individual resistances will be of one of the following types: spreading resistances, bulk resistances, or interface resistances. The thermal resistance seen by the device is the equivalent

thermal resistance through all the possible paths through which heat can be removed. This is illustrated in Figure 2.1.



① Device surface to air thermal resistance
② Substrate thermal resistance
③ Epoxy thermal resistance
④ Spreading resistance
⑤ Thermal resistance to back of package
⑥ Thermal resistance to pins and package top
⑦ Package surface to air thermal resistance
⑧ Pins thermal resistance
⑨ Heat sink thermal resistance

Figure 2.1 - Thermal resistances in a die-package-TE cooler-heat sink system.

Interface thermal resistances occur due to the fact that flat surfaces in contact only make contact in 2 to 5% of the apparent area of contact due to the microscopic roughness of the surface [13]. Part of the heat transfer occurs through convection or radiation for a bare joint, or through conduction in the presence of a substance or interstitial material. These interstitial materials have been analyzed in terms of the thermal resistance they introduce[1], [13], [14], and show that soft metal alloy treatment of the surfaces is key in reducing the resistance at the contact.

The concept of thermal resistance, in addition to on-chip power dissipation will determine the operating temperature of the devices. For this, a discussion of the power dissipation levels that should be expected is presented in the following section, and a review of the heat management techniques is done in the section 2.4.

2.3 Heat dissipation of various interconnect technologies

In order to be able to assess what the requirements in thermal management of two dimensional arrays of optoelectronics devices are, the heat dissipation and required

thermal stability of devices and systems must be reviewed. This section is such a review, starting with the heat generation mechanisms in semiconductors, and followed by discrete and arrayed optoelectronic device requirements in both modulator based and surface emitting based systems.

In the analysis of device heat dissipation, the main mechanisms that contribute heat are field-carrier interactions, carrier-lattice interactions[15], and photon-carrier interactions (of optoelectronic devices)[16]. These combined will result in ohmic heating and heating due to recombination and relaxation processes. For both electronics and optoelectronics, the non-radiative recombination of photo-generated carriers is not as significant as their ohmic contribution[2]. In the review to follow, the heat dissipation values are presented assuming ohmic heating.

The performance of electronics, although degraded by increases in temperature, do not see such dramatic effects as those seen by optoelectronics, especially since properties such as wavelength, efficiency, and contrast ratios tolerate not more than a few degrees, depending on the application.

One of the applications that has been shown to have the most stringent dependence on temperature, has been that of laser diodes. Usual wavelength dependence upon temperature are in the nm/°C range[17], [18], [19].

2.3.1 Optoelectronic device heat dissipation

In optical backplane systems, devices of interest are those that can be integrated in arrays. These devices can be of three types: light emitting devices, modulating devices and detectors. Table 2.1 outlines some of these devices and their characteristics.

It can be seen that the problems that have to be managed when making the transition from discrete to arrayed devices are those related to large heat dissipations over small die areas, as well as nearest neighbour effect under decreasing device pitch. For this, the existing thermal management techniques for electronics and optoelectronics have to be looked upon, and their applicability to optoelectronic device arrays assessed. This is done in the following section.

Table 2.1 - Optoelectronic device heat dissipation.

Device	Comments	Function	Discrete	Array (125 μm pitch)
VCSEL (vertical cavity surface emitting laser)	Power dissipation depends on bias conditions (after [20],[24]).	Light emitting device	20-40 mW	2.6 W/mm^2
VC-VSTEP (vertical to surface electrophotonic devices)	Measured thermal crosstalk resulting in 7°C (after [21]).	Light emitting device	10mW	500mW/mm^2
LED (light emitting diode)	(after [23]).	Light emitting device	50-150 mW	-
SEED (Self electro-optic effect device)	Temperature stability req. 2°C for 50% contrast ratio variation (after [2], [17], [25]).	Light modulating device	1-2 mW	200mW/mm^2
FET-SEED (Field effect transistor/SEED receiver)	Temperature stability req. 2°C for 50% contrast ratio variation (after [2], [17], [25]).	Detector	40 mW	200mW/mm^2 (500 per cm^2)

2.4 Existing heat removal techniques

The different approaches found for the management of heat in systems, and hence for proper operation of the devices they house is briefly discussed in this section. The figure of merit for the comparison is the thermal resistance of the packaging scheme with or without external heat management systems.

Since standard commercially available packages are probably the most used and attractive alternative for the packaging of bare dies, it is important to see the capabilities they offer as far as the thermal management problem is concerned. These properties have been studied through simulations and the results outlined by Mahalingam[1] and emphasize the importance of proper heat sinking of the packages. Table 2.2 shows the thermal properties of interest of these packages for various configurations.

More advanced heat sinking systems have to be devised when the technology power dissipation is larger. Packaging systems with thermal resistances of less than 2°C/W have been shown[28], [29], however their applicability to optoelectronic device arrays is

questionable as they are bulky, or do not allow optical access to the dies being cooled. These involve some sort of fluid, usually water in the cooling of the package.

Table 2.2 - Package thermal properties.

Package	Thermal Resistance (°C/W)	Convection	Heat sink attached	Comments
Plastic DIP with heat spreader	70	Yes	No	With heat spreader, [1].
Ceramic Dual-in-line	50	No	No	With heat spreader, [1].
Ceramic Dual-in-line	25	Yes	No	With heat spreader, [1].
Leadless chip carrier (LCC)	5-10	Yes	Yes	for Berylia-alumina respectively, [1].
Leadless chip carrier (LCC)	20	Yes	No	Alumina, [1]
Ceramic Pin grid array	55	No	No	Alumina, [1].
Ceramic Pin grid array	3-10	Yes	Yes	Alumina, [1], [20].

Thus the requirement of optical access limits the paths through which heat can be removed to the wirebonds and the bottom of the die in contact with the package through conduction, and to air through radiation and convection. More aggressive packaging techniques which use direct coupling of the unpopulated side of the die to high thermal conductivity substrates, such as silicon substrates[24], have achieved the lowest package thermal resistances. Techniques using water flow though etched microchannels in these substrates have been shown to have thermal resistances of less than 0.1°C/W [17], [30]. It is worth mentioning that although these methods can prove to be efficient and promising, more conventional approaches must be sought, which will allow a smoother transition between industry approaches to packaging and packaging of free space optical links.

Such a method would be to combine standard package with thermo-electric (TE) coolers, which are a compact reasonable way of decreasing the temperature on the device, as well as keeping it within a certain stability range. These can be used in applications where up to 2 Watts of heat must be removed, however, their contribution to the overall decrease in temperature of the device is poor [24], and require adequate heat sinking.

Having reviewed some of the methods used in the thermal management in electronic and optoelectronic systems, it is seen that their capabilities are limited, specially when high connectivity through optical access and compactness are required. The design

of proper heat sinks can be rather difficult because of this, as well as because of the fact that optomechanics and optics use part of the space resources that should or could be dedicated to heat sinks. It is clear that ways of sharing resources between optoelectronics and optomechanics will have to be thought of and implemented.

By having outlined the limitations of heat removal systems, it becomes apparent that as device arrays become larger, these systems become less and less able to support them. If a *divide and conquer* idea is used to provide this connectivity over various arrays of devices with independent thermal management systems or reduced complexity, then this problem can be made solvable. The remainder of this chapter will analyze and explore the design space for optoelectronic devices and determine the trade-offs that will govern the proper partitioning of the system.

2.5 Formulation of the models for heat dissipation

In this section, smart pixel array thermal models will be formulated using the heat dissipation levels, device characteristics of section 2.3 and based on the theory of section 2.2.

In order to formulate the models that will describe the various factors that affect the heat dissipation and temperature of the devices in a two dimensional array of optoelectronic devices, it is assumed that the packaging is capable of removing the power dissipated by the devices in the smart pixel array. In other words, the dominant path for heat ends in a proper heat sink, and is reflected by the value of the associated thermal resistance.

2.5.1 Smart pixel array design space geometrical considerations

Let us first define a smart pixel cell. Consider the geometry of Figure 2.2, where a smart pixel cell of side d_2 is defined. The cell is composed of an optical I/O window of side d_1 and logic occupying the area on the cell not occupied by the window[1]. By repeating these cells in two dimensions, one can obtain an array of smart pixels. The two quantities of interest in the analysis that will follow are smart pixel density and optical window size. The former is equal to $(1/d_2)^2$ and has units of smart pixels per unit area.

1. This definition is based on a monolithic smart pixel approach, or a hybrid smart pixel approach where no logic is allowed under the optoelectronic windows.

These two quantities will define the connectivity and the processing capabilities of the smart pixel array, and are related by

$$A_1 = \frac{1}{D} - A_2. \tag{2.4}$$

where D is the density and A_1 and A_2 are as defined in Figure 2.2.

Note that the allowed design space in the density-window size plane is limited by the line where the area of the logic is zero. This design space can be seen in Figure 2.3, where the optical window size (expressed as d_1 and A_1) is plotted against smart pixel densities for various values of A_2, the area occupied by the logic.

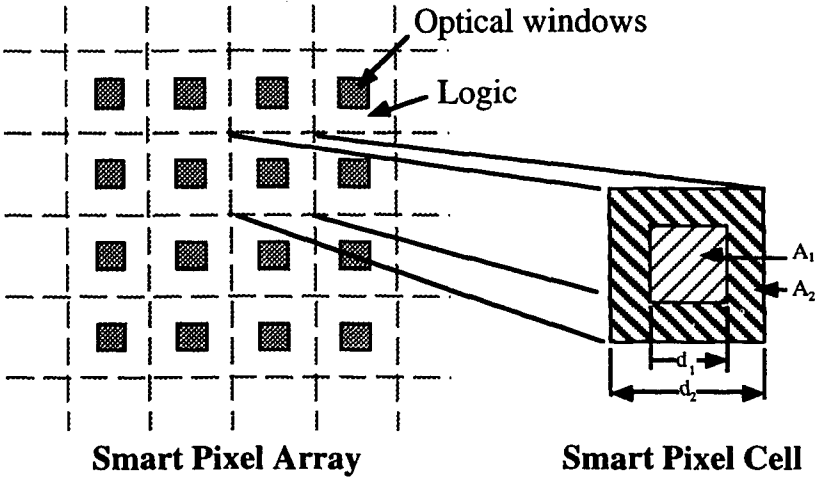


Figure 2.2 - Geometry of a smart pixel cell.

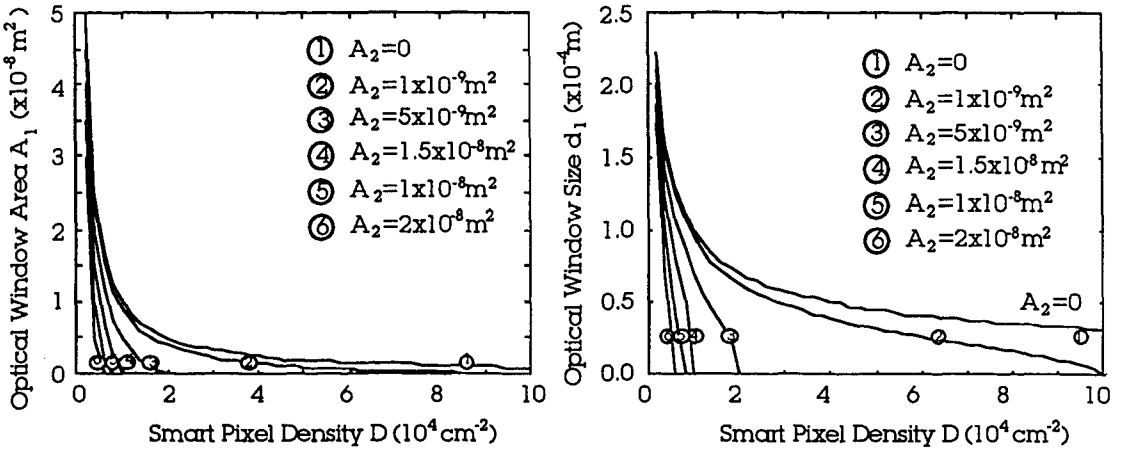


Figure 2.3 - Design space in the optical window-smart pixel density for fixed values of logic area.

Another parameter of importance is the smart pixel array size. Throughout the analysis of this chapter, the physical size of the smart pixel array, L, will be used. The number of smart pixels in the array is then given by $NxN=DL^2$.

In this analysis we will start with an infinite design space in density, optical window size and smart pixel cell number and define a subset of that space representative of the allowed design space for smart pixel array dies. The following section will define the thermal model for the smart pixel array based upon the definitions of window sizes and smart pixel density.

2.5.2 Die level model

The die with the two dimensional array of smart pixels on its top surface, is treated as a volume of semiconductor, in which steady state heat flow occurs[7],[8]. It is assumed in the model that the power dissipation occurs in a thin film containing all the electronics and optoelectronics. This treatment of the layer where heat is dissipated, will define the heat flux boundary condition at this surface. The mathematical analysis of this model is developed in Appendix A. A more rigorous analysis would include an iterative procedure to look at multiple layers[7], with the thin top layer having heat being generated within a volume. Since the analysis in this model is rigorous, it can be extended to include the addition of another layer.

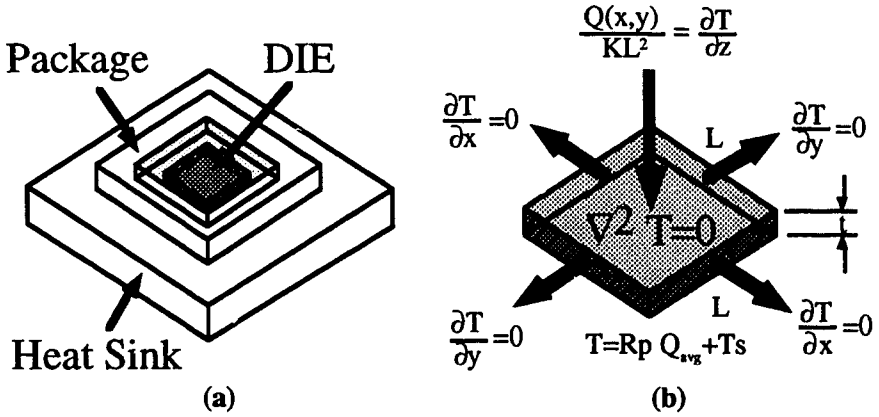


Figure 2.4 - Boundary value problem boundary conditions.

The die level boundary value problem (BVP) is shown in Figure 2.4. The heat entering the volume through the top surface is expressed as the Fourier series expansion of the configuration of the smart pixel in two dimensions. Note that based on the numbers from sections 2.3 and 2.4, the optoelectronic heat dissipation is larger than the electronic

heat dissipation, however occurs over a smaller area. The normalized (1 or 0) function that defines the presence or absence of an optical window used is the following

$$f(x,y) = \left(d^2 + \sum_{m=1}^{\infty} 2d^2 \cos m\pi \frac{\sin \pi m d}{\pi m} \cos m\sqrt{D}x \right) \left(d^2 + \sum_{n=1}^{\infty} 2d^2 \cos n\pi \frac{\sin \pi n d}{\pi n} \cos n\sqrt{D}y \right) \quad (2.5)$$

which is the Fourier series expansion of a varying duty cycle periodic two-dimensional square pulse train. The heat dissipation can be looked in terms of this function. The optoelectronic window power dissipation has to be represented by the high value of the above function and the electronics power dissipation has to be represented by the low value of the above function. The heat is then given by

$$F(x,y) = (C_1 - C_2) f(x,y) + C_2 \quad (2.6)$$

where C_1 and C_2 fix the power dissipation levels of the optoelectronics and electronics respectively, to the desired values. This is illustrated in Figure 2.5.

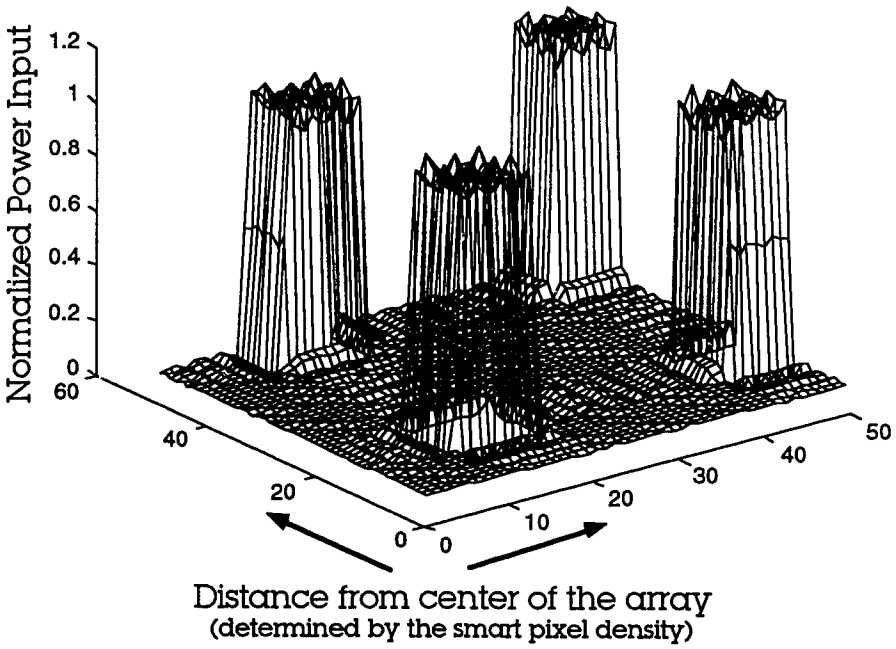


Figure 2.5 - Die heat input function for 4 windows with duty cycle of 0.3 (first 5 harmonics in the series).

It is to be noted that the density or pitch of the smart pixel cells is determined by the periods in the periodic functions in the two axis spanning the plane in which the

function is defined. Also, the device size is determined by the duty cycle of the square wave periodic function in both coordinates.

By analyzing the problem in steady state, the solution of the heat equation reduces to the solution of Laplace's equation in three dimensions. The heat flow at the sides of the die is assumed to negligible when compared to the heat flow at the surface and bottom of the die.

The boundary condition at the bottom of the die is given by the package thermal models discussed in the following section.

2.5.3 Package level models

The package model to be incorporated into the evaluation of the expressions resulting from the BVP is the thermal resistance model described earlier. This thermal resistance under a given power input will have an associated drop in temperature, which in conjunction with the heat sink temperature or the ambient temperature will determine the temperature at the die to package interface. This is the final boundary condition needed in the formulation of the problem and allows the problem to be solved without loss of generality (packaging-wise) and as outlined in the following section.

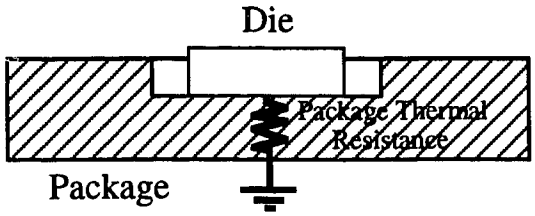


Figure 2.6 - Package level model used in the formulation of the boundary conditions for the die.

2.5.4 Boundary value problem solution

The formulated BVP is non-standard and inhomogeneous. Using the principle of superposition, the problem is divided into two subproblems which can be solved using Fourier's Rule. This results in a correspondence between the coefficients of the varying duty cycle square pulse train series defining the power dissipation boundary condition and the infinite fourier series solution to the BVP. The analytical solution for the temperature that arises from the coefficient matching in the boundary condition is shown in Appendix A at the end of this thesis.

This analytical model is applied to an array of fixed size, and with increasing cell densities (varying the period of the function) and for given window sizes or logic areas (varying the duty cycle of the function).

2.6 Heat dissipation effects on device array characteristics

Having formulated the model, a MATLAB™ program was developed to compute the solution for the temperature at the hottest point in the array for varying array parameters. The results are shown and discussed in the following section.

2.6.1 Overview of results

The plots of Figure 2.7 show qualitatively the temperature dependence for varying density and window size for a 5mm x 5mm die. Note that if a maximum operating temperature is set, there are maximum densities and device windows values that are allowed. Similarly, the number of devices per die is seen to affect the temperature of the devices as well. These observations are quantified in the next sections.

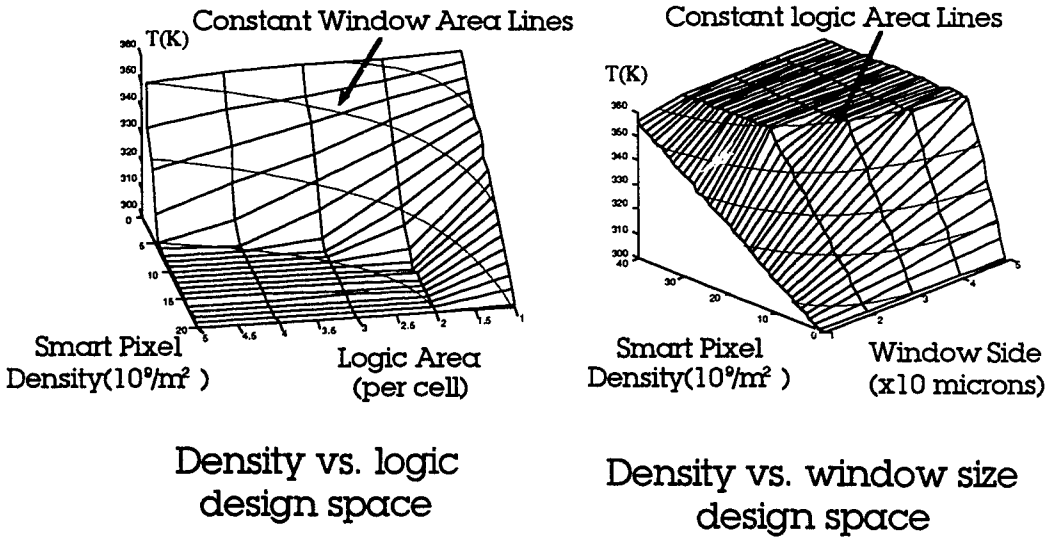


Figure 2.7 - Design space for fixed die size. Maximum and minimum density values correspond to no logic with minimum window size, and no logic with maximum window size.

It is important to note that the solution of the BVP allows the design space to be looked upon both in terms of the window size and the density or the logic area and the density, as it is shown in Figure 2.7. This follows from the expression discussed in section 2.5.1, relating all these three parameters.

2.6.2 Technology dependence

One of the primary results that this model allows us to see, is that which relates different smart pixel arrays as a function of the technology they employ. The analysis will be limited to a modulator based technology, in which the optical windows are SEED devices dissipating 320W/cm^2 over their area[1]. It is assumed that these windows are embedded in a substrate containing electronics (CMOS-SEED[34]) and (FET-SEED[35]). The analysis of this section will show the results for two main technologies for the smart pixel electronics: GaAs-FET and Si-CMOS. The power dissipation used for each is based upon the numbers from sections 2.3 and 2.4. It is important to note the difference between these technologies, as they will strongly affect the design parameters of the smart pixel array.

The power dissipation in CMOS and GaAs is made up of two components: a static component and a dynamic component[36]. The former, is due to leakage, as well as other currents drawn constantly from the power supplies. The latter is due switching transient currents in addition to charging and discharging of load capacitances and is a function of the switching speed. For GaAs FETs, the static power dissipation is the dominant component due to the constant current that flows in the presence or in the absence of switching, whereas in CMOS, the dominant component is the dynamic power dissipation. The above information leads to a power dissipation density function F_e, which is a function of frequency f, and can be expressed as

$$F_e = Af + B \tag{2.7}$$

where the values of the constants A and B are dependent on the technology. For digital CMOS, there is no constant power being dissipated when there is no switching ($B \approx 0$), whereas for GaAs-FET technology, there is an inherent dissipation, independent of frequency ($A \approx 0$).

In the technology dependence comparison, GaAs-FET with B=50W/cm^2 was used. The power density level for CMOS that was used was 50 W/cm^2. This number was chosen from the numbers seen in section 2.3, and assumes 1000 transistors per mm^2 for

1. Assuming a 10μm x 10 μm window with 0.5 A/W responsivity and 8V bias with 80 μW of optical power impinging on it.

1μm technology, with 6μW/MHz per gate[38], and an operating frequency of 84 MHz for the CMOS case. The power dissipation for various CMOS technologies and various operating frequencies will be discussed in section 2.7.

Note that other than the difference in dissipated powers, the only difference between the two smart pixels is the semiconductor thermal conductivities, as the optical windows will have identical properties.

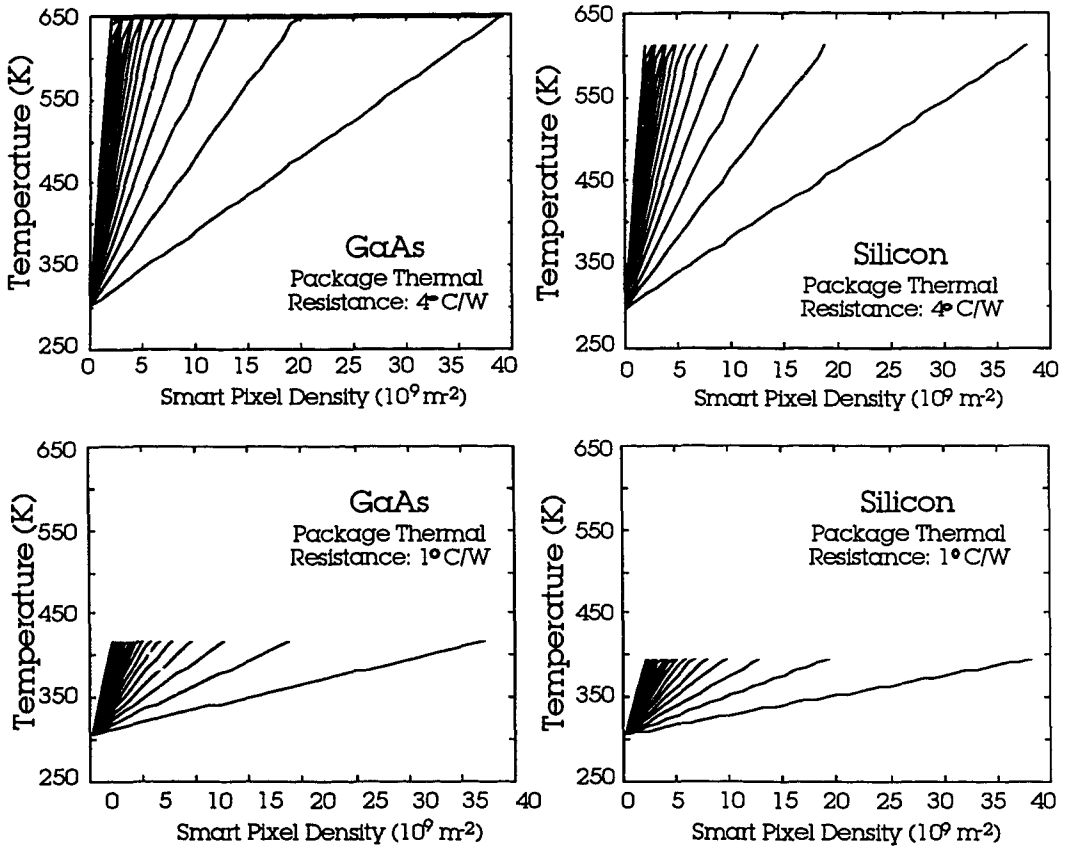


Figure 2.8 - Temperature at the windows for 5mm die for two cases of thermal resistance of the package for Gallium Arsenide and for Silicon. The different lines represent various window sizes, with larger windows as the slope increases.

In addition to the different power dissipation in the electronics in the above technologies, the effect of different boundary conditions at the bottom of the die can be seen, namely different package thermal resistances.

Package thermal resistances can vary according to their characteristics, use, and environment as it was seen in section 2.4. The plots of Figure 2.8 show the temperature as a function of smart pixel density for various optical windows, ranging from 3.5μmx3.5μm to 20μm x 20μm. This is done for two technologies and for two package thermal resis-

tances: 1°C/W and 4°C/W. The former corresponds to a more advanced packaging scheme. Throughout the remainder of this chapter and the analysis of the formulated model, a thermal resistance of 4°C/W will be used, which is representative of standard technology applicable to two dimensional arrays of optoelectronics.

For a maximum allowed temperature of 325 K (51.85°C) and a fixed package thermal resistance of 4°C/W, the maximum density that can be achieved for window sizes of 5μm on the side is $2.5x10^5$ cm^{-2} for GaAs-FET and $4x10^5$ cm^{-2} for Si-CMOS operating at 84 MHz. Similarly, for a window of 20μm on the side, the maximum densities are less than $3x10^4$ cm^{-2} and $5x10^4$ cm^{-2} respectively, with logic areas of $3x10^{-5}$ cm^2 for GaAs and $1.6x10^{-5}$ cm^2 for silicon. This can be contrasted to the case where the temperature is set to 340 K (66.85°C), where 5μm windows allow $4.5x10^5$ cm^{-2} for GaAs-FET and $6x10^5$ cm^{-2} for Si-CMOS and 20μm windows allow $4x10^4$ cm^{-2} and $6x10^4$ cm^{-2} respectively. This means logic areas of $2x10^{-5}$ cm^2 and $1.3x10^{-5}$ cm^2 for GaAs and silicon respectively for the latter case.

It is important to point out that the dynamic power dissipation of CMOS makes the comparison for these technologies unfair. A fairer comparison will have to look at specific circuits, and under predetermined operating conditions, such as high speeds for instance.

2.6.3 Increasing array size

Increases in the number of smart pixel cells per die can be achieved in two ways: increasing the density for fixed die size, or increasing the die size. The former does not have an impact on the total dissipated power, provided the ratio of the window to cell size is kept constant. The latter could or could not result in an increase in dissipated power, depending on the relative change in the window to cell size ratio.

The other alternative is to increase the die size, which results in an increase in the on-chip power dissipation proportional to the area of the die. The plots of Figure 2.9 show the results for Si-CMOS running in the 160 MHz range for 1cm x 1cm and 5mm x 5mm die sizes. It can be seen that if the temperature of the optoelectronic devices is to be kept below 325 K (51.85°C), window sizes of 25μm x 25μm and above imply densities of 3000 smart pixels per cm^2 or less for 1cm x 1cm dies. For the same operating temperature and for 5mm x 5mm dies, smart pixel densities of 10000 smart pixels per cm^2 would be allowed. This, of course, with the corresponding sacrifice in smart pixel logic.

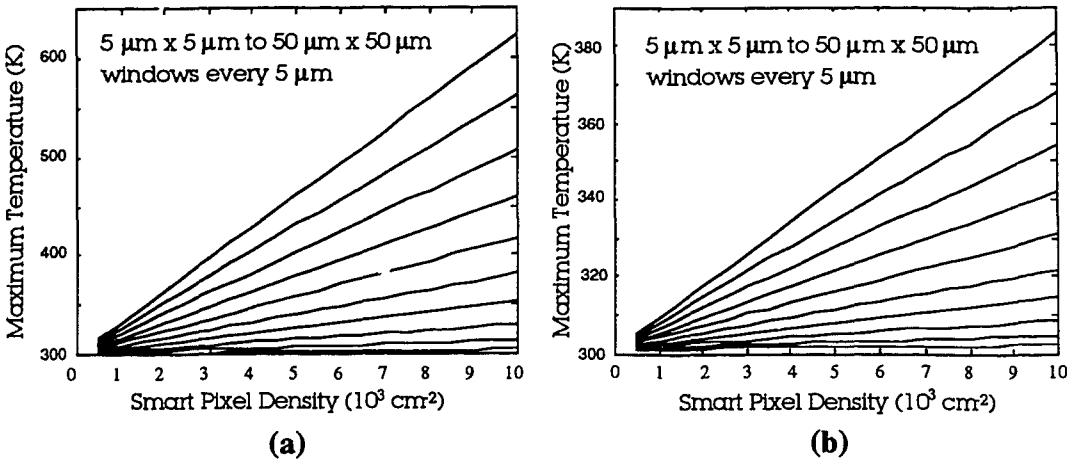


Figure 2.9 - Plots for CMOS technology with a power dissipation of 100W/cm^2, and for (a) 10 mm die, and (b) 5 mm die.

For operating speeds of 100MHz and 300MHz, or power dissipation densities of 60W/cm^2 and 180W/cm^2,the design space for 5mmx5mm dies looks like that of Figure 2.10, showing that for a maximum temperature of 325K and 25μm windows, the densities are 12000 cm^{-2} and 9000 cm^{-2} respectively.

It is interesting to note that for densities of 1x10^8 m^{-2} (or 100μmx100μm smart pixel cells), the temperature for different operating frequencies is not affected greatly by increases in the operating frequency of the logic, specially for large optical windows. This is due to the fact that most of the power dissipation occurs at the windows.

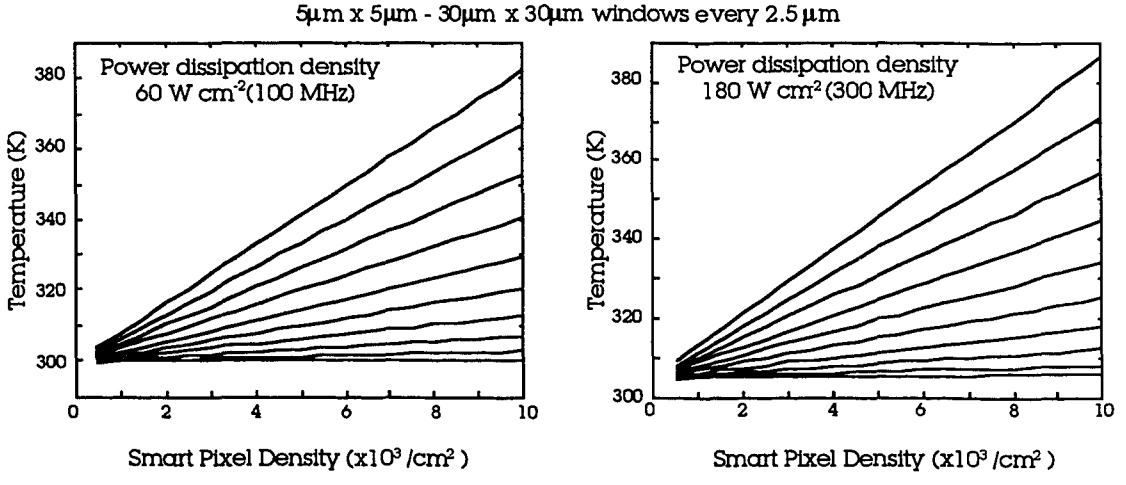


Figure 2.10 - Plots for CMOS technology for window ranges between 5μm x 5μm and 30μm x 30μm for 5mm x 5mm dies.

The results point to the fact that for smart pixel densities of 10000 cm^{-2}, windows not greater than 25μmx25μm should be used. It should be also noted that windows of such size, with large densities will limit the area occupied by the logic in the smart pixel.

2.6.4 Device window size and power dissipation effects on smart pixel density

The heat dissipation levels at the windows can be assumed to be due mainly to the Joule heating from the generated carriers, and under given bias conditions[2] will have the following form

$$P_{heat} = VI_{photocurrent} = VP_{opt}\Re \tag{2.8}$$

where $\Re$ is the responsivity of the detector, and P_{opt} is the input optical power. For the plots of Figure 2.8, Figure 2.9 and Figure 2.10, a heat flux of 320 W/cm^2 was used, which, under a bias of 8V and a responsivity of 0.5A/W, would mean 80μW and 500μW of optical power were impinging on 10μmx10μm and a 25μmx25μm SEED windows respectively. It was assumed throughout the model that as the window size grew in size, the optical power required to drive it increased linearly with its area. This can be justified by the fact that window capacitance will be larger for larger windows (if the windows are assumed to have capacitance as that of a parallel plate capacitor), requiring more carrier generation in the switching. It is for this reason that the optical power input was treated as a uniform power density over the window area.

By looking at the heat dissipation power densities, one can clearly see that the heat dissipation per unit area can be an order of magnitude higher for the windows than for the logic (tens of W/cm^2 for the electronics vs. hundreds of W/cm^2 for the windows) if the required switching energy is high. It is found, however, that the optical window power dissipation is not the dominant factor for small windows with any reasonable amount of logic, that is with duty cycles d smaller than the square root of the ratio of optical to electronic power. As the density increases for a fixed window size, the logic will have to decrease, increasing the ratio of optoelectronic window to logic area, and making the effect of the windows more and more dominant, as was seen in the plots of Figure 2.10.

It is interesting to point out that the above analysis was made assuming power dissipation levels for CMOS smaller than the power dissipation levels for the optoelec-

tronics. As the required switching energies become smaller, and the operating speeds become larger, the above assumption is no longer valid. It is therefore desirable to see how the analysis might be affected by a change in the conditions set initially for the problem, under the mentioned assumptions.

The design space geometrical considerations show us that the range of windows and densities for fixed values of logic area of the smart pixel, are limited to the 5000 smart pixel per cm^2 for windows if 25 μm windows are used and at least 20 transistors are designed into the smart pixel. If transistor counts on the order of 100 are needed, the density of smart pixels in the array should be limited to 1000 cm^{-2}.

For such densities, the window size for 1cm x 1cm arrays will be limited to the 30μm range, whereas for smaller dies can go as high as 70μm on the side. The operating speed of the logic will have an effect on these numbers, thus it is desirable to quantify this as well, and will be seen in the following chapter.

By having developed a model which allows us to set the boundaries in the design space of smart pixel arrays under given packaging constraints, it was seen that the factors that affect the design space are various. The following section will look in more detail at the trade offs between these factors, and how the design bounds for smart pixels can be changed by changing the properties of the packaging.

2.7 Trade-offs in the design of smart pixel arrays and systems

2.7.1 Formulation of a trade-off expression

The difference in temperature between the optoelectronic device windows and the area occupied by electronics, found using the analytical solution based upon thermal resistance modelling, is seen to be negligible. This is due to the fact that the model considers the heat on the windows and logic to be over an infinitesimally thin volume, and is treated as a heat flux at the boundary. In addition, the boundary condition at the sides of the die constrains the flow of dissipated power from the top of the die to the bottom.

For the purpose of analyzing the trade-offs between the chip area, package thermal resistance and thermal conductivity of the substrate, the temperature at the windows can be derived from a thermal resistance model which assumes uniform power dissipation at the top surface of the die. This power dissipated will be just the average

power dissipation of the combined system of optical windows and logic. It can be clearly seen that this power will be proportional to the average power density at the surface of the die which is just a weighted sum of the power densities at the windows (F_o) and at the electronics (F_e) with respect to their areas (and expressed in terms of the previously defined duty cycle). The temperature at the top of the die T_w reduces to the sum of the heat sink temperature (T_s) and the temperature drop across the die and the package for a given power input and can be seen to be

$$T_w \approx T_s + (R_{die} + R_{packg}) P_{avg} = T_s + \left(\frac{t}{K} + R_{packg} L^2\right) F_o \left(d^2\left(1 - \frac{F_e}{F_o}\right) + \frac{F_e}{F_o}\right) \qquad (2.9)$$

where the thermal resistance of the die (R_{die}), as well as the average power were substituted in. Also, for fixed substrate thermal conductivities, and a set of power densities, window size and cell density, the temperature is proportional to the substrate area of the die or the thermal conductivity of the package. This can be seen in Figure 2.11, where the packaging parameters are varied to change the temperature of the die. The plots of Figure 2.11 show the results for a die with 25μmx25μm windows and a smart pixel density of 1024 per cm^2.

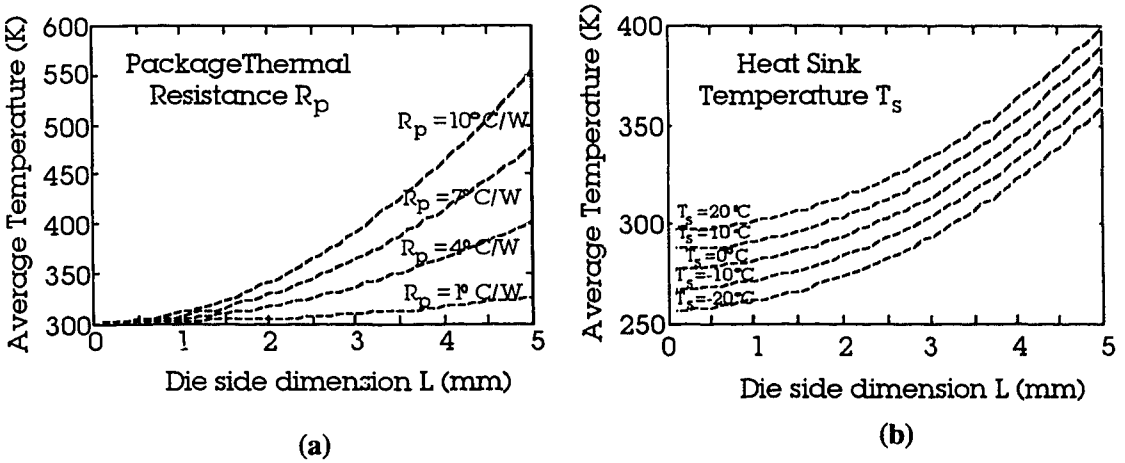


Figure 2.11 - Average die temperature (ordinate) against die dimension L (ordinate) for varying thermal environment parameters of the die (50μm windows, 1024 cm^2 density).

It can be seen that the two ways of reducing the temperature of the device array by changing packaging parameters will affect this temperature differently, with the reduction of the thermal resistance of the package being better, particularly for large arrays (5mm and above). A drop in thermal resistance from 4°C/W to 1°C/W results in a die of over 4

times the area, and can be achieved by providing better heat sinking capabilities to the package, such as fins under convection, larger heat sinks, etc. Changes in the heat sink temperature will benefit the system with smaller dies (1mm-3mm). These heat sink temperature changes can be achieved through thermoelectric coolers [33].

Once the packaging parameters are fixed, the operating conditions of the die will be directly responsible for the die temperature. The expression found earlier allows us to investigate these die parameters. This is the subject of the following section

2.7.2 Frequency dependence and die size

Using the expressions found for the frequency dependence of the heat dissipation of the electronics in the smart pixel, equation 2.9 can be used to see some of the trade-offs between CMOS technologies and the limits on operating speeds and die sizes. The value of constant A from equation 2.7 is calculated by finding the capacitance per gate for the scalable *1.2* and *2.0μm* technologies, with voltage levels of 3.5V and a transistor area density normalized to the density of 1000 transistors per mm^2 for 1.0μm technology, and is shown in Table 2.3. It is assumed that the transistor number per unit area is proportional to the area occupied by each transistor. Figure 2.12 shows the temperature as function of die size for a density of 1024 per cm^2 and a window size of 50μm for scalable *2.0μm and 1.2μm technology*[37], *1μm technology*[38] and for *0.8μm technology*[39]. The area occupied by the logic for the density and window size used, is equal to $9.5x10^{-8}m^2$ per pixel. For these technologies, and assuming 1000 transistors per mm^2 the transistor count per smart pixel would be around 100.

Table 2.3 - Constant A for CMOS technologies estimated from [37], [38], [39].

Technology	Constant A (W/m^2MHz)
0.8 μm	3000
1.0 μm	6000
1.2 μm (scalable)	14000
2.0 μm (scalable)	18000

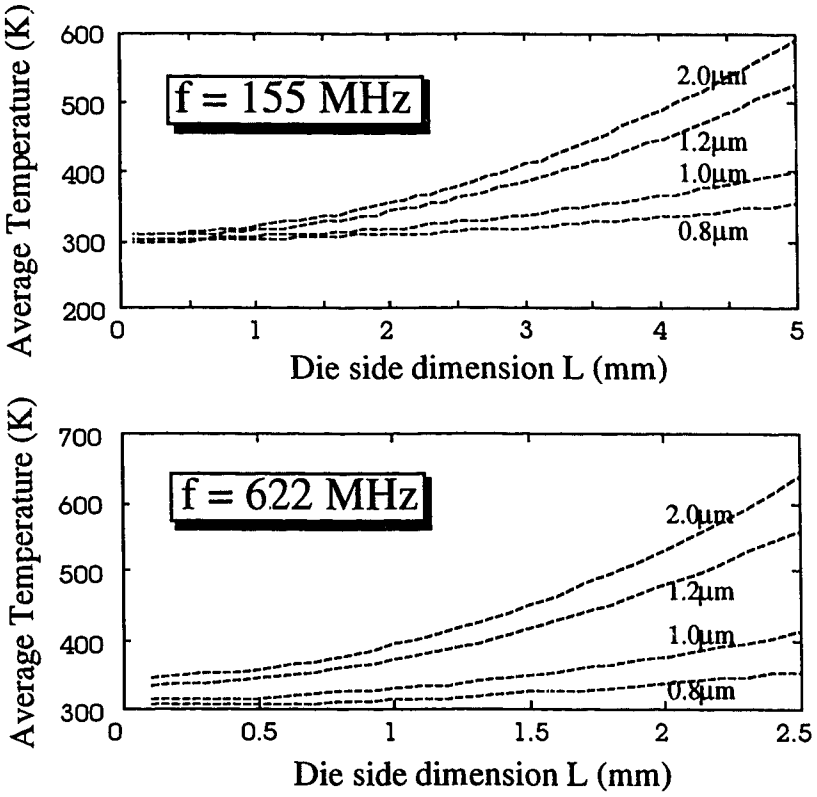


Figure 2.12 - Average die temperature vs. die size for switching frequencies of 155MHz and 622MHz and 50μmx50μm optical windows with 320 Wcm^{-2}.

It is interesting to see that for *0.8 μm technology* at 155MHz, dies in the 3.5mmx3.5mm range will operate at temperatures around 325 K, thus allowing 12 x 12 arrays of smart pixels to be designed. Operation at 622 MHz would yield 2mmx2mm dies with arrays of 7x7 arrays of smart pixels. *1μm technology* will allow 3mmx3mm at 155MHz and 1mmx1mm dies at 622MHz.

Further simulations show that 25μm windows will exhibit very similar behaviour (to within less than 5 K) to that for 50μm windows since the area occupied by the windows for a density of 1024 smart pixels per cm^2 is about 2.5% of the smart pixel cell area for 50μm windows and 0.6% for 25μm windows. Thus the heat dissipation for cases of large logic area and small windows is dominated by the CMOS circuitry.

Further manipulation of equation 2.9 allows a way of determining all three design space parameters, namely the optical window size, smart pixel density and array size, for a given operation frequency for silicon CMOS logic. The expression that arises from such manipulation is

$$d = \sqrt{\left[\left(\frac{T_w - T_s}{t/K + R_{pack}L^2}\right) - F_e\right]\frac{1}{F_o - F_e}} \qquad (2.10)$$

and shows how the duty cycle can be used to define the smart pixel properties.

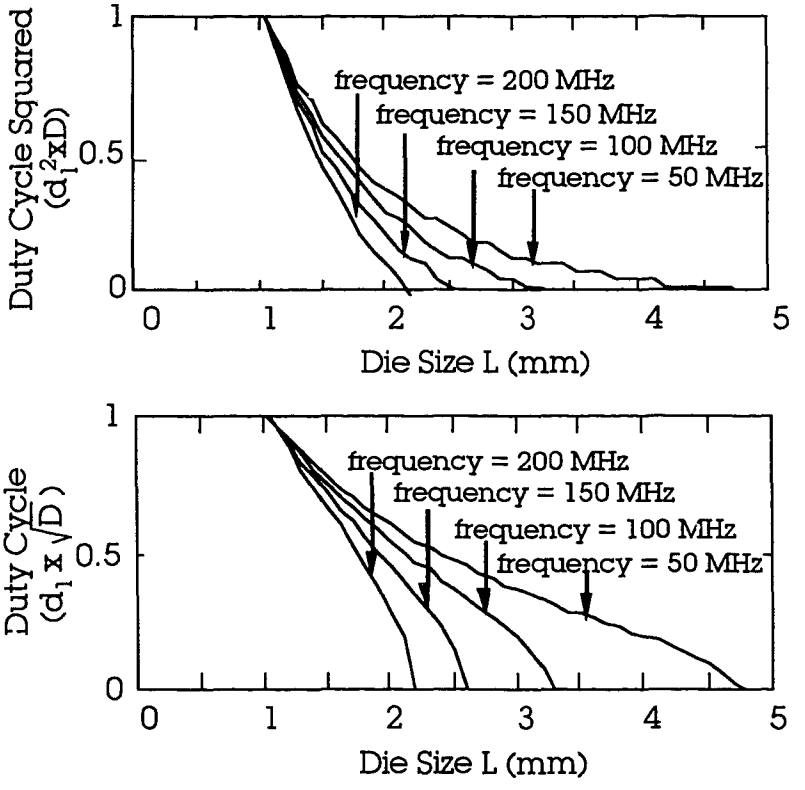
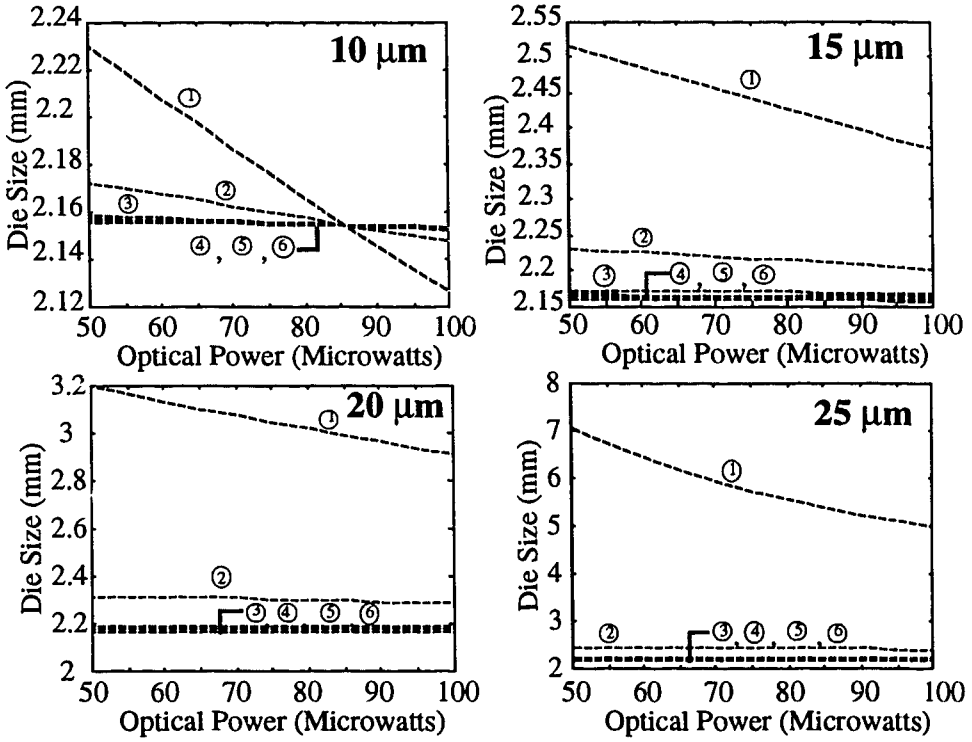


Figure 2.13 - Design space variables for various frequencies for operation at 325 K and with package thermal resistance of 4 K/W and heat sink temperature of 297.15 K.

The usefulness of the plots of Figure 2.13 lies in the fact that for a given frequency, and for a fixed maximum allowed temperature of 325 K, the choice of window size and density determines the die size. In a similar way, a target die size will define the ratio of window area to smart pixel cell area at a given frequency of operation. For instance a 25μm window smart pixel array with densities of 10000 cm^{-2} will have a duty cycle value of 0.25, allowing dies of 1.9mm, 2.2mm, 2.6mm and 3.3mm for 200, 150, 100 and 50 MHz respectively. Similarly, for 25μm windows and densities of 1000 cm^{-2} the die sizes are 2.1mm, 2.5mm, 3.1mm, and 4.4mm for 200, 150, 100 and 50 MHz operation respectively.

2.3 Maximum die size vs. Optical power input

In the analysis so far, we have considered cases in which the optical power input is varied as the optical window size is varied. By analyzing specific cases with fixed window sizes, one can see the trade offs that exist between the other parameters, given a prescribed operating temperature, in our case 325 K. The following plots show the maximum die size that can be attained for 4 cases of window size, and density ranges between 3200 and 160000 smart pixels per cm^2 against varying optical power input. The responsivity used is 0.5 with bias voltage of 3.5 Volts. These parameters determine the heat dissipation at the windows.



	Density (cm^{-2})	Cell Side (μm)	Window to cell area ratio for window size side of:			
			10 μm	15 μm	20 μm	25 μm
①	160000	25	0.160	0.36	0.640	1.000
②	40000	50	0.040	0.09	0.160	0.250
③	10000	100	0.010	0.02	0.040	0.062
④	6400	125	0.006	0.014	0.026	0.040
⑤	4444	150	0.004	0.010	0.018	0.027
⑥	3265	175	0.003	0.007	0.013	0.020

Figure 2.14 - Maximum die size vs. optical power input (per window) for (a) 10 μm, (b) 15 μm, (c) 20 μm, and (d) 25 μm windows and for smart pixel densities as shown.

It can be seen that as the cell becomes mainly composed of logic (or the ratio between the area of the window and the cell area decreases), the die size approaches the maximum possible die size (2.16mm) determined by the logic power dissipation levels, fixed at those determined by *0.8μm technology* parameters and a switching speed of 500MHz.

In the plot for 10μm x 10μm windows, there is a crossover whose location increases as the window size increases. This just relates to the fact that a smaller window area will experience a much higher heat density, as it is assumed that the optical power is distributed over the area of the window. Also, the resulting size of the smart pixel array is larger as the windows are larger since for given densities, larger windows mean less logic. It becomes evident then that for the operating speed near 500 MHz, the dominant heat dissipation mechanism is that from the logic, specially for the cases where the smart pixel cell area is much larger than the window area. This is illustrated in the following section, in which an example is presented.

2.9 Application Example

It is of interest to see what the maximum die size is for a given set of smart pixel configuration parameters. A current example of this technology is the AT&T/ARPA SEED on Silicon Design Workshop parameters which allows dies with fixed cell size of 125μm (containing *0.8mm technology* silicon CMOS) and with two SEED windows 20μm x 20μm each. In this example the ratio of areas between optoelectronic windows and cell

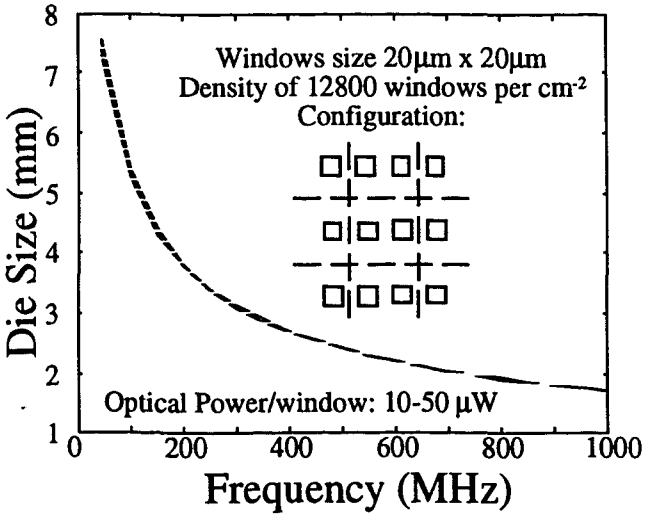


Figure 2.15 - Maximum die size vs. frequency for the AT&T/ARPA SEED on Silicon geometry.

size is 0.05, thus it is expected that the optoelectronic heat dissipation contribution be of small significance. The resulting die size is shown Figure 2.15 where the maximum array size plotted against the Silicon CMOS logic switching speed.

It is worth noting that optical power inputs of 10, 20, 30, 40 and 50 μW are shown, but are not readily distinguishable from one another, thus confirming that in this regime the maximum allowed size is driven by the heat dissipation of the logic. It can be seen that as the operating speed gets higher than 700 MHz, the smart pixel array die size drops below 2 mm. For the density of 6400 smart pixels per cm^2, this represents a maximum number of smart pixels of 256.

2.10 Results and Conclusions

This chapter outlined the limitations on the characteristics of two dimensional arrays of optoelectronic devices imposed by the packaging in terms of the heat dissipation. It was seen how the package affects the performance of the device array, as well as how the actual design of the array of devices can be manipulated to cope with a given packaging environment. For this, a model was derived which, although being a first order approximation, provided a good insight into the allowed design space for smart pixel arrays. In addition, an expression based upon thermal resistance considerations that relates the various parameters that affect the temperature at the die surface was derived.

The design space for smart pixels, from the packaging point of view, depends on three fundamental variables: smart pixel array die size, smart pixel density, and window or logic area size. In addition parameters inherent to the smart pixel technology and its operation parameters play a key role in this design space. The analysis for GaAs FET-SEED showed that the array densities that can be achieved for a given window size are about three times smaller than those that can be achieved in Si-CMOS under similar heat dissipations (or low frequencies). Advantages of FET-SEEDs in addition to the non-hybrid nature of the smart pixel, are those related to the frequency-independent power dissipation, allowing larger arrays at large frequencies. However, the thermal conductivity difference between GaAs and Silicon will guarantee that Si-CMOS technology will still be more advantageous at roughly 3 times the crossover frequency.

It was shown that the geometrical considerations constrain the design space density to about 1000 smart pixels per cm^2 for windows between 10 to 50 μm on the side, if 75 to 100 transistors are to be included in the smart pixel cell. The analysis shows that die sizes between 2 and 3.5 mm (7 x7 to 12 x 12 arrays of smart pixels) will be achievable for CMOS logic operating 100 and 700 MHz. It was also seen that for such window sizes and smart pixel densities, the effect of window size is not the dominant factor, specially for optical powers below 150 μW per window.

By manipulating the packaging environment to minimize the thermal resistance, and guaranteeing efficient removal of the dissipated power will only allow the systems designer to cope with some of the heat dissipation problems. By analyzing the design space of smart pixels, the problems that have to be dealt with by the packaging are of lesser complexity. In addition, relating the required operating parameters of these device arrays to the physical limitations imposed by the on-die heat dissipation allows the assessment of the feasibility of a proposed system.

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Chapter 3

Connectivity issues and constraints in the packaging of two dimensional optoelectronic device arrays

3.1 Introduction

In chapter 2 it was shown that the design of smart pixels is constrained by the thermal management properties of the package. The maximum achievable density, window size and array size were affected by the package thermal resistance and the heat sink temperature, as well as the smart pixel technology and operating conditions. In this chapter the constraints imposed by connectivity, bandwidth and package geometry on the design space will be analyzed. Section 3.2 will introduce the connectivity requirements and relate them to requirements in package I/O. Following in section 3.3, the applicability of single chip carriers to photonic backplane interconnects will be analyzed, starting from connectivity considerations, followed by bandwidth, and geometry considerations. An overview of the applicability of Multi Chip Module technology will be made in contrast to single chip carriers. As a result the chapter will conclude with a discussion on smart pixel design space constraints.

3.2 Trends in connectivity increase

As outlined in chapter 1, connection intensive switching architectures will require backplanes to provide a high capacity for the flow of information between switching nodes in the 1-10 Terabit per second range[1]. Current electrical backplanes will not be able to provide the degree of connectivity required by such systems, thus optical backplanes are attractive alternatives to supply the connectivity and the bandwidth requirements of switches. In order to supply the bandwidth requirements 1000 to 10000 channels capable of carrying information at rates between 100 and 1000 Mbits/sec between switching nodes are envisioned in architectures for photonic backplanes[2],[3]. Clearly, the architecture will determine what the traffic will be in and out of the backplane into a single switching node (board or panel). The amount of information that needs to come out of the two dimensional optoelectronic device array electrically is related to the complexity in the on die circuitry by virtue of the decisions in the routing of information

that are made at the die level. We can then envision a large I/O die with smart pixels with no logic, or very little logic, or a small I/O die with complex smart pixels. In the following section, the architectural design parameters are related to the hardware limitations imposed by the packaging.

3.2.1 Connectivity requirements of smart pixel arrays

Since smart pixel arrays provide a certain connectivity through optical channels, each with associated control logic, it can be readily seen that the number of connections out of the package will be required to be large. In order to assess the connectivity requirements on the packaging a measure of connectivity is used. This connectivity parameter depends on the number of control lines and the number of I/O supported by those control lines. The total number of connections required between the PCB and the package to be used or to be designed can be expressed as

$$N_p = gm\left(1 + \frac{1}{r}\right)N^2 \qquad (3.1)$$

where N_p is the required package I/O, N^2 is the number of optical channels (in and out), r is the ratio of signal to control and bias lines and g is a factor that allows the introduction of ground lines or unused lines. The constant *m* is a measure of the fraction of lines that are used at any given time, as the information travelling to the switches or nodes is less than that travelling through the backplane optically[3]. This constant will be fixed by hardware and depends on the probability of information being sent to a given node in the switching system. In architectures where the information to a given node is moved out of the smart pixel by virtue of its priority status, and which allows only one channel (b bits long), the value of m is b/N^2.

Note that r is a measure of complexity for the smart pixel array, as it reflects the ratio of the number I/O to the number of lines it requires to support it and constitutes a good way of assessing how much on-die processing is done.

In figure 3.1, the plot shows the required number of connections the package needs to provide as a function of r. The plots are done for 32, 128, 512 and 2048 I/O.

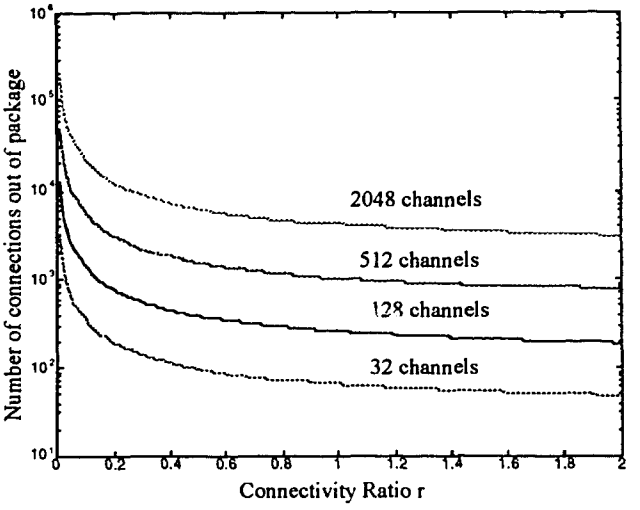

Figure 3.1- Number of Connections per package Required vs. Connectivity Measure

The above graph shows the effect control and support lines, as well as ground lines, have on the required package I/O. When designing a smart pixel, the ratio r must be minimized. Also, it reveals that a one-to-one mapping between the optical I/O to the electrical I/O going in and coming out of the smart pixel will not be realizable for smart pixels with 200 or more optical channels. This however can be solved by a single electrical I/O being shared by multiple channels, or by design of the architecture which is translated as a change in the parameter m in equation 3.1. The Hyperplane Architecture[2] with N bits wide channels uses a value of m of $1/N$, having each channel occupying a whole row in the array.

For a given m, and a given package I/O, a set of values of r can be found. Such analysis yields the plot of figure 3.2 where the existing trade-offs between the parameters in equation 3.1 can be seen graphically.

The plot is done for Np=400, and for varying r. The m parameter is varied as follows: No multiplexing or line sharing, multiplexing 10 and 100 lines, and for the case where only a row and half a row in the array is connected at a time. The last two cases correspond to the maximum number of allowed smart pixels for a given package size, although it can be seen that the effect of r makes them less efficient than straight multiplexing for large number of control lines per optical I/O.

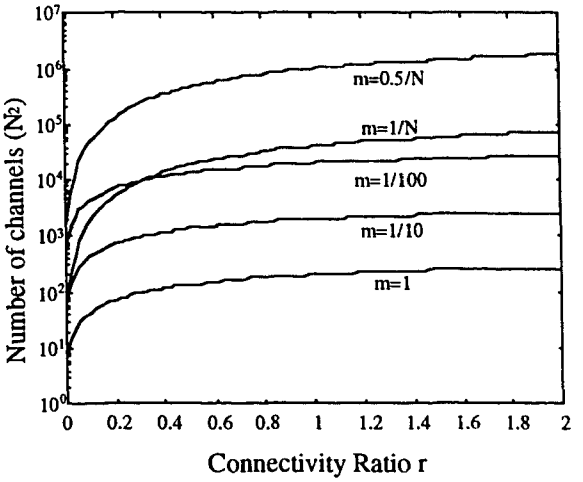

Figure 3.2 - Trade offs between the different parameters in smart pixel design for fixed Np of 400.

The number of I/O to support the logic is something that needs to be assessed. Without knowledge of the smart pixel architecture or without a specific design, it is difficult to get a number for this. However, a simple approximation to Rent's Rule[4],[5], which relates the number of pinouts to the number of gates in an IC, can be insightful. Rent's Rule can be written for the smart pixel logic as

$$\text{Pinouts} = k(xN^2)^{1/c} \tag{3.2}$$

where x is the number of transistors per smart pixel. For values of c and k of 2 and 0.5 respectively, the required I/O versus the number of channels for various values of x is shown in figure 3.3.

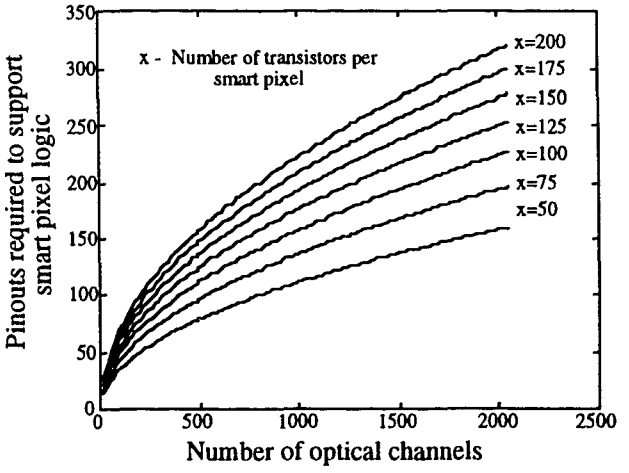

Figure 3.3 - Required I/O to support the logic for varying smart pixel array size and for 50 to 200 transistors per smart pixel.

The numbers from the plot give a better insight than the parameter r in equation 3.1, since now the package I/O can be looked upon in terms of the number of channels only, and of course the value of m. This follows from the fact that the ratio r can be rewritten as

$$r = \frac{N^2 m}{k(xN^2)^{1/c}} \tag{3.3}$$

and when substituted in equation 3.1 yields an expression in terms of the number of optical channels, the number of transistors per smart pixel and the parameters m and g, as well as the Rent's Rule relevant parameters.

While it is expected that the electrical I/O in and out of the die will be small in comparison to the optical I/O of the die, the transistors in the array will have an associated number of control and bias lines. Ultimately, the smart pixel array will be limited by the number of pinouts of the package, thus the parameters m, r, and g in equation 3.1 will determine the number of optical channels that will be allowed. To assess this, considerations on the various architectures that can be used in an optical backplane as well as information on the I/O capabilities of carriers are required. It is interesting to note that Rent's Rule will show that if only one tenth of the optical channels are connected at a time, smart pixels with 100 to 150 transistors will allow 32x32 arrays. This result already assumes a package with I/O of about 300 and a value of g of 1. 10x10 arrays will require 100 electrical I/O, while 20x20 arrays will require approximately 250 electrical I/O.

The sections to follow will relate the connectivity requirements to the physical and electrical properties of die carriers. The physical characteristics will impose limitations on the bandwidth, electrical properties such as inductance and capacitance, while the geometrical characteristics will impose limitations on the maximum electrical I/O.

3.3 Single chip carriers on boards or modules

The following section describes standard packaging technologies that can be applied to photonic systems in the context of optical backplanes. The investigations cover primarily single chip carriers, however most of the concepts are applicable and are extended to multiple chip modules. These will be discussed in section 3.4.

3.3.1 Connectivity

The various types of carriers have a certain degree of connectivity which they can provide. This connectivity is limited mostly by their geometry and physical attributes. While there exists a trade-off between the connectivity of the packages and their bandwidth, many ways of improving the performance of packages have been devised[11]. The connectivity provided by standard single chip carriers can be as high as 450[6], however the physical space they utilize on the board, which determines their applicability to real systems, specially to optical backplane systems, is large. Packages that take advantage of their footprint or area on the board efficiently to provide the electrical connectivity to this board will be the packages of interest for optical backplanes. These are the packages that will give the largest I/O. In addition, their thermal properties and their alignability properties will determine the size of additional hardware that is required around them, making the connectivity-footprint parameter of greater importance.

This figure of merit for single die carriers is shown in figure 3.4, which shows that most commercially available packages (standard technology) have pinouts limited to a prescribed pitch, which limits their pin-out count vs. area.

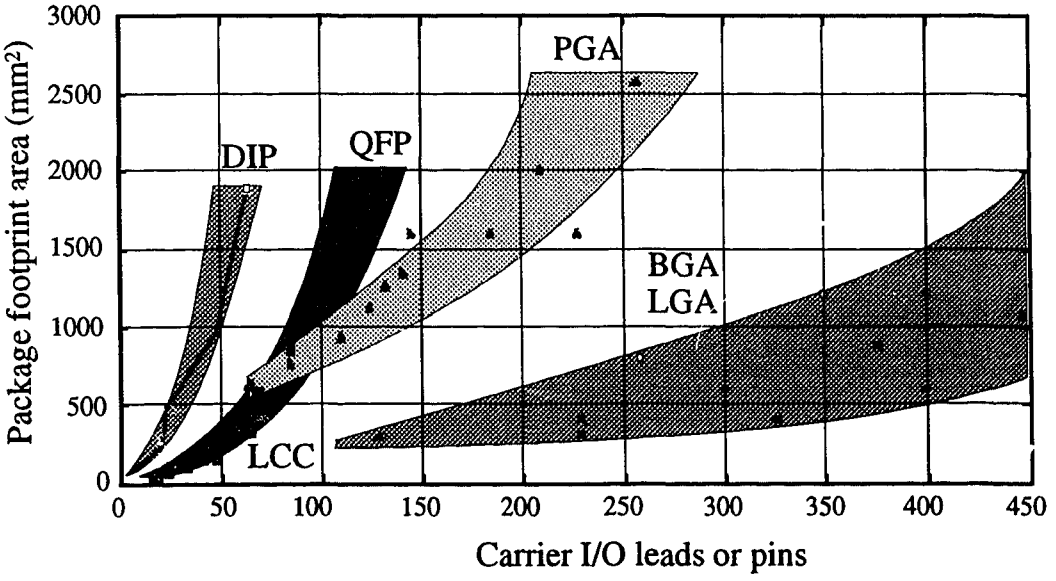

Figure 3.4 - Area occupied on board vs. package I/O for various standard commercially available packaging technologies ([6], [7], [8]).

It is important to note that the connectivity provided by packages with 0.1 inch (2.54 mm) pitch is limited to counts in the 300 I/O range. More advanced packages, such

as LGAs and BGAs, or interstitial pin PGAs, allow very compact carriers to be incorporated into boards with very high I/O, with up to 400 I/O on a footprint of 645 mm^2 [9]. BGA packages will however be able to achieve a reduction in area factor of 2.5 relative to interstitial PGAs[9]. It is worth noting that standard FR-4 PCBs experience problems as the BGA pad pitches go below 1.27mm [10], in addition to the requirement on multiple layers that are needed to support the footprint of such packages.

Nevertheless, the figure of merit mentioned above is still key to optical interconnect systems since, as it was pointed out in chapter 2, the real estate occupied by the carriers has to share resources with optomechanics and cooling systems. This makes the carriers required to be as compact and as connectivity-efficient as possible. In addition, for system optical I/O partitioning into multiple dies, the size of each carrier needs to be as small as possible if the die optical connection density is to be taken advantage of.

3.3.2 Cavity size constraints

Something to bear in mind is the bondability of the die to the package. For this it is necessary to quantify the relationships between cavity size and number of bond pads. The plot of figure 3.5 in which the abscissa represents the I/O of the package and the ordinate is the side of a square cavity, shows the status of single carrier standard technology as well as the size of cavities for custom single chip carriers design specifications[6] for multilayer ceramic technology.

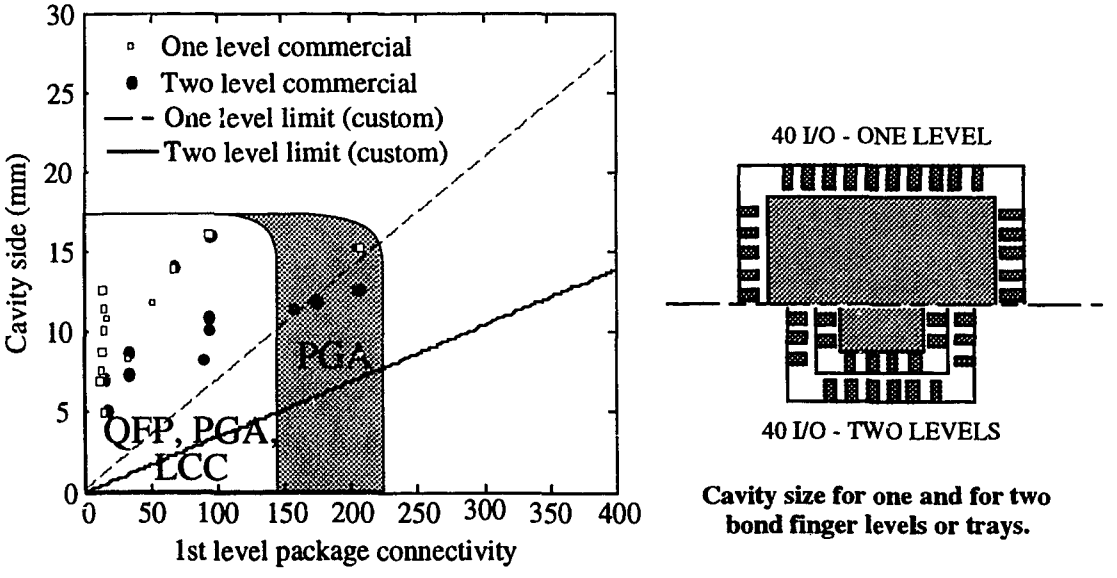

Figure 3.5 - Cavity size vs. package I/O for standard PGA technology and for custom designed multilayer packages (standard/one tray or level and high density/two trays or levels connection module [6]).

The two solid lines in the plots represent the cavity side limit for one tray and two trays of bond fingers. It can also be seen that commercially available PGA packages have bond fingers larger than those specified by design rules for custom packages, resulting in larger cavities for a given I/O. It is important to realize that for applications where optical access to the die is required, and hence wirebonding is required, this will be the limiting factor as far as pinouts is concerned. In addition, the cavity will have to have a tight relationship with the die size, thus considerations on bondability need to be made.

To assess the bondability of the die within a cavity, the bond pad to package bond finger length is required. For this the die must be looked upon in terms of its true length L', rather that the total length of the arrayed smart pixels L used previously. If we let the true size of the die be composed of bond pads in a one dimensional array, this length can be seen to be given by

$$L' = \left(\frac{1}{4}N_p + 1\right)(d_{bp}) \tag{3.4}$$

where d_{bp} is the size of the bondpad along the array direction, as shown in Figure 3.6, and for $L' \geq L$. As seen earlier, $L = N/\sqrt{D}$, so L' and L are related to each other through the mapping between N and N_p, or the parameters m, g, and r, and the smart pixel density D as shown in equation 3.5.

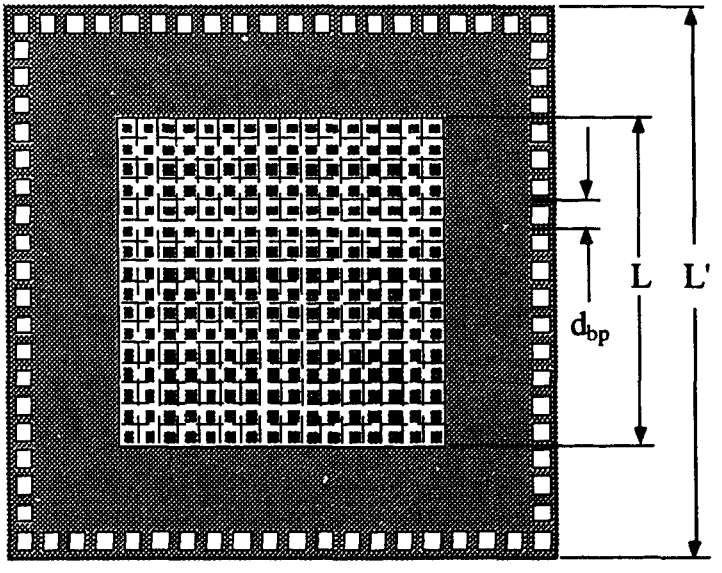

Figure 3.6 - Die size L' relation to smart pixel array size L.

$$L' = \left(\frac{gm(1 + 1/r) L^2 D}{4} + 1 \right) d_{bp}. \quad (3.5)$$

The relationship between the true size L and the size L' of the smart pixel array is better illustrated through an example. Assuming a smart pixel array with a density of 3000 cm^{-2}, a 32x32 array (1024 channels) will have a length of 3.4 mm. For 100 μm bondpads (d_{bp}), the size of the die will be determined by the array size L if the total number of bondpads is less than 132. Also, fully connecting the 1024 channels (with m =1 and r very small) would imply having a die which is 2.5 cm on the side, and an unrealizable size package. Implementing an architecture which has each row carrying eight 4-bit channels, for a total of 256 channels and capable of connecting any eight channels at the same time ($m=1/\sqrt{N}$), the electrical signal I/O reduces to 32. With two control lines per 4 bit channel (r=2), the number of bondpads is 48, thus die size L' can be found to be determined by L. In contrast, if four times the number of channels can be connected electrically ($m=4/\sqrt{N}$), the number of bondpads required will be 192, resulting in a die size determined by the bondpad frame and with L' of 4.8 mm.

Also, equation 3.4 shows that if d_{bp} is approximately 100μm, 1cm dies will have a maximum of 400 bond pads, while 5mm dies will have 200 bondpads. For a one-to-one mapping of the bondpads to the carrier cavity bond fingers (g=1), the carriers will have to have two trays (or two bond finger levels). Single tray packages will provide about half the pinouts required by the die under the above conditions, unless the cavity and the wirebond lengths are allowed to be large. For this it is necessary to quantify the effect of wirebond length on signal integrity.

The effect of long wirebonds was observed in a 3 GHz board and package, used to assess the attenuation and loss introduced by different wirebond lengths. S_{21} parameter measurement on a through connection show that the 3dB point is reduced by 150MHz with every mm increase in the wirebond length. It has been estimated that wirebonds will have a 1nH/mm inductance per length[15]. Inductive dips consistent with those in [15] were also observed as the wirebond length was increased.

Under a 1mm long wirebond constraint, the cavities will then have to be 2mm (or less) larger than the die size L'. As shown in figure 3.5, the cavity sizes span a range of values between 5 and 15 mm, and with differences in size of about 2 mm. This tells us

that commercially available packages, from the wirebond length criterion alone, are able to support dies with cavity sides of 3mm to 15 mm for 1mm wirebonds. If the bondpad density and die size, number or channels, and wirebond length criteria are combined, it is seen that a sacrifice in electrical I/O out of the chip will have to be made.

3.3.3 Bandwidth

The Terabit/sec aggregate b width requirement can be achieved by varying two system parameters. These system parameters that can be changed are the connectivity or number of optical links or channels, and the bandwidth or maximum operating speed capability of each of these individual channels. The latter is affected both by the device electronics and the packaging. Under ideal conditions, it is desirable that the effect of the packaging be minimized, so that the electronics are the limiting factor as far as speed.

Under the standard technology constraint, it is desirable to assess the properties of existing packages. The transmission properties of packages depend strongly on the properties of the materials, their configuration and geometry which determines in turn their associated electrical properties. High speed packages have 50 Ohm characteristic impedance lines which allows proper matching between board and device. In addition, an important parameter is the length of the wires embedded in the package, as well as the path they go through. High speed packages will have the path between the bond pad and the pin or pad that interfaces with the board or module as short as possible. The introduction of power and ground planes improves greatly the performance of packages, as the transmission line properties of the wires within the package are improved. It is important to point out that the path within the package is greatly affected not only by its length but by its geometry. Pin grid array packages, have smaller bandwidths than leadless chip carries or flat packs because of the fact that the wires have to go through vias through the ceramic to different layers in their routing between the bond fingers to the leads or pins in this case. These vias introduce undesired inductances. Side brazed packages and flat packs have the routing between bond fingers and leads on the same layer or mesa[11]. For instance PGA packages will have their -3dB point at about 1.5 GHz. Side brazed packages could potentially go higher than 1 GHz, however the traces within the package usually have varying width and do not have microstrip properties. QFPs can go as high as 8-10 GHz [11],[12], depending on the design of the bond fingers and bond pads and routing.

Leadless chip carriers perform best, as they do not have leads brazed onto them, reducing both inductance, resistance and capacitance of the circuit.

Different lines within the same package will also exhibit different properties. It has been shown through time and frequency domain techniques[13], that for a PGA package, the propagation delay ranges between 211 and 286 ps and the rise time contributed to the system by the packages ranges from 199 to 299 ps, with a strong dependence on the line length, plating line length and the line's distance to the nearest ground pin. It is interesting to note the effect of ground delays within the package, where the signal ground experiences a delay due to the extra path it must travel as there is a short between this ground and the board grounds. Transmission measurements also show that the 3dB bandwidth of these packages varies for the different lines between 1.1 and 2.2 GHz. This is consistent with the 600-800 Mbits/sec range figure in [14]. The plots of figure 3.7 show network analyzer measurements of a line of a PGA package on a 50 Ohm line board. The measurement is achieved through SMA to board connectors, going into and out of the package and through a wirebond within the package. The results are adjusted to reflect the fact that the characterization is done for two lines in the carrier and show a -3dB point of 1.6 GHz. Other studies[16] have shown the effect the pins have on the package, by comparing Land Grid Arrays (LGAs) to PGAs (Figure 3.8).

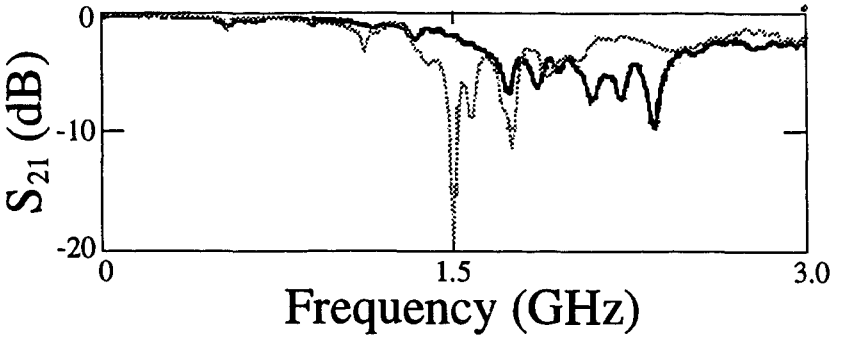

Figure 3.7 - S_{21} parameter of a PGA with and without a socket on a high speed board.

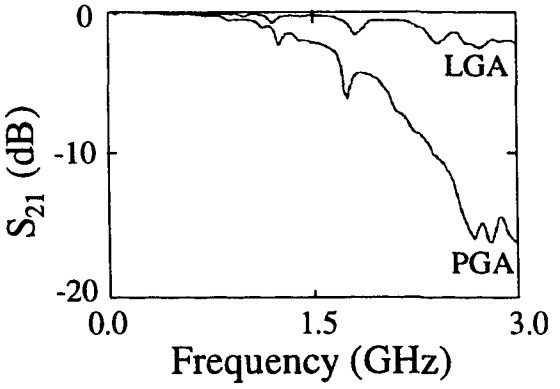

Figure 3.8 - Plots of the S_{21} parameters of PGA and LGA showing the better performance of LGAs (after[16])

Quad flat packs have better bandwidth properties than PGAs for the reasons mentioned earlier. The following shows a custom designed package from TriQuint semiconductor mounted on a PCB designed as a test fixture for characterization up to 5 GHz. The plot shows an S_{21} parameter network analyzer measurement of this package on a board. It is to be noted that the measurement was done for two lines coupled together with conductive epoxy at the bond finger level, thus the attenuation observed corresponds to two lines butted together back to back. The interface to the network analyzer is through 3.5 mm SMA connectors perpendicular to the board. The -3dB point of this package/ board assembly is at approximately 5 GHz, however the bandwidth is limited by the board. The bandwidth of Quad Flat Packs can go as high as 10 GHz. The network analyzer range did not allow characterization beyond 3 GHz.

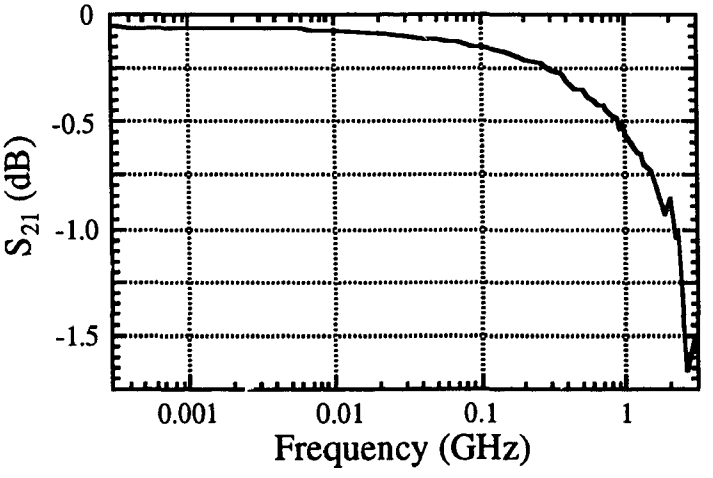

Figure 3.9 - S_{21} (transmission) parameter for a QFP mounted on a high speed board through a solderless contact.

The following table shows the performance parameters of common standard carriers. The maximum speed is expressed in Mbits/sec, and assumes that the first harmonic of 50/50 duty cycle square pulse train is set at the -3dB point in the analog measurements shown in figure 3.7, figure 3.8 and figure 3.9.

Table 2.1 - Single chip carrier characteristics

Chip Carrier	Bandwidth (f_{3dB})	Data Rate	Maximum I/O	Aggregate data rate
DIP	300 MHz	0.1 Gbits/sec	50	5 Gbit/sec
QFP	> 3 GHz	1.0 Gbits/sec	150	150 Gbit/sec
LCC	> 5 GHz	2.0 Gbits/sec	75	150 Gbit/sec
PGA (0.1" pin spacing)	1 - 2 GHz	0.4 Gbits/sec	400	160 Gbit/sec
BGA/LGA	3 - 5 GHz	1.0-2.0 Gbits/sec	600	600 Gbit/sec

It can be seen that if high speed and connectivity are to be required by the system, BGAs and LGAs will be the right choice. It is also noted that PGAs would provide the required connectivity if the smart pixel is designed with a value of m<<1. In this case, the information to the nodes from the backplane or from the nodes to the backplane is small compared with the information travelling through the backplane. For this package however, the data rates would be limited to not more than 500 MHz per electrical I/O.

3.4 Multi-chip carriers

Multi-chip Modules are an attractive way to provide interconnection between bare dies (or packaged dies), through stacked dielectric films with conductive media between them. They provide the connectivity through various layers of wiring, which distribute the signals, power through vias and traces on each layer Figure 3.10. The stacked materials can be uniform or can consist of combinations of ceramics. The technologies offered by Kyocera fine ceramics are based upon Alumina, however, thin films (Aluminum or other if high temperature thin film is required) can be incorporated, as well as other materials such as Aluminum Nitride and Molybdenum. The choice of these ceramics or materials depends on the application and the desired attributes and properties on the MCM.

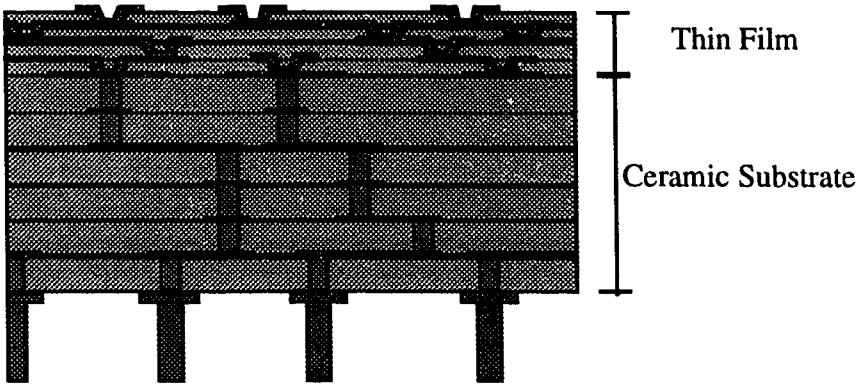

Figure 3.10 - MCM cross section showing a combination of thin film and ceramic layer stack

3.4.1 MCM technology capabilities

Multi-chip Modules can house 200 chips with around 2000 connections per module, through modules with 60 to 80 layers. The limiting factor to what can be done is essentially the functionality/cost ratio, as the technology offers higher and higher connectivities and speeds. Under standard packaging 1 GHz is typically low end, with different configurations and particularly materials being used for higher frequencies. The chips can be either wirebonded or interfaced through other technologies.

The choice of materials and MCM technology will determine the connection density, speed and thermal properties of the MCM[17]. The high connectivity vs. footprint they can offer, as well as the very high speeds they can support makes multichip modules a very promising technology candidate. Their availability for prototype systems however is limited. In addition, issues associated with the alignment of multiple chips on the same module, as will be seen in the following chapter, complicates the use of this technology in optical backplane systems. It is important to note also, that because for optical backplane systems, optical access to the optoelectronic devices is a requirement, technologies such as C4- Flip chip bonding[9], Chip-Scale Packages CSP[10] technology, or direct low temperature solder bonding of the die to the MCM are not an option, resulting in dies with I/O limited by the size of the wirebond and the perimeter of the die or bond frame.

3.5 Conclusions

This chapter outlined the I/O requirements of smart pixel arrays and presented the current status of packaging technology with a perspective on its integration into optical backplane system demonstrators. Although the connectivity capabilities of carriers were assessed, the way in which they would affect system partitioning, smart pixel design parameters, and system operation, could only be discussed qualitatively. This, because of the fact that the variables in the architecture of a smart pixel array are strongly dependent on the ultimate smart pixel functionality. These architecture defined variables were identified and defined in terms of packaging design space parameters which allowed the formulation of expressions relating them to the smart pixel array I/O. In addition the analysis attempted to obtain an insight of the I/O requirements to support the logic embedded in the smart pixel through the use Rent's rule. In such attempt, a set of equations and plots was developed that allow the smart pixel and system architecture designers to relate the system parameters to the physical layer and hence investigate the system realizability.

With an ever growing emphasis on the development of new packaging schemes with higher aggregate capacities, the mapping of the requirements of systems to the existing technology will become easier. Technologies such as MCMs and advanced single chip carriers being developed now, will substitute the ones reviewed in this chapter, however will still be assessed in terms of the figures of merit described.

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Chapter 4

Alignment issues and constraints in the packaging of two dimensional optoelectronic device arrays

4.1 Introduction

Since the connectivity that optical links can provide requires a high density in the optical channels, as well as relatively small optical windows for low switching energies, the constraints the packaging will impose on the alignability of the optoelectronic device arrays through an optical system has to be studied.

This chapter will start with a brief review of the existing packaging technology from an alignability perspective through a tolerance analysis of standard packaging technology. In section 4.3 the mathematical formulation of the power coupling on square detector windows will be introduced. This will allow the introduction of the alignment problem in optical backplane demonstrators, as well as the alignment requirements of such system demonstrators, both for surface emitter laser (SEL) based systems and modulator based systems. Section 4.5 will follow, describing quantitatively the alignability of a system as a function of window size and array density and size. This last section will aim to provide results that are analogous to those found earlier in chapter 2.

4.1.1 Types of carriers

The use of single chip carriers as the first level package was found in chapter 2 to be a need, as the connectivity provided by the smart pixel arrays must be divided among various dies. The integration of these into a second level package to connect it to the corresponding switching node must be then considered. It is here where the alignability of the system must be taken into account. A review of the tolerances of existing packages must be made in order to see what misalignments are introduced when a system is put together without any means for alignment. The chip to package alignment accuracy and the package to board tolerances have to be combined together to get an overall positional accuracy of the device array. Additional optomechanical hardware will also have associated accuracy in the alignment due to the resolution of the positioning mechanisms. These two bits of information will determine which design space parameters are constrained by the alignment.

4.1.2 Other packaging schemes

Custom packaging techniques to provide better alignment capabilities is being studied extensively[1],[2],[3]. It is necessary, as was mentioned in chapter 2, to assess the applicability of existing microelectronics packaging technologies to the packaging of optical interconnects.

A promising technology for the implementation of photonic backplanes and in general for that of optical interconnects is the Multi-Chip Module (MCM) technology. Although this technology has its advantages in terms of speed and area vs. connectivity, its availability in small quantities is a disadvantage due to its custom design nature. In addition, the status of the reliability of the optoelectronic technologies for smart pixel implementation does not allow the dies to be integrated into a module without some demountability features. As the smart pixel technologies mature, the costs and availability of such devices will allow non-demountable dies to be integrated into systems through this packaging technique.

The alignability of the dies within these modules gets somewhat simplified, as the carrier to board alignment accuracy is no longer present. The disadvantage is that related to positioning the dies relative to a reference. For the case of single chip carriers, the reference is the cavity. For both cases, the problem can be solved using *advanced pick and place techniques*[5],[4] currently used in the optoelectronics/fiber optics industry, which position dies within microns. At an experimental level and for prototype or demonstrator systems, other means have to be devised to achieve the die to carrier alignment. These will be studied further in this chapter and in chapter 5.

4.2 Tolerance analysis

Based upon technical drawings of single chip carriers[6] and board manufacturing specifications[7], the tolerances on the first level package are analyzed. Although the calculations presented are estimates based upon the individual component specifications, they will help in the understanding of what can be achieved with the existing technology. The tolerance analysis is divided into two parts, in accordance to the levels of packaging required to integrate the bare die into the system: die to package and package to board or second level package.

4.2.1 Die to package tolerance analysis

The positioning of the die within the package cavity will contribute to the decrease in positional accuracy of the device array. It is assumed that the alignment of the die is performed with respect to one of the corners of the package cavity. With no other reference, usually the die is positioned by eyeballing its location within the cavity. This works for electronics, as the position of the die within the carrier cavity, for reasonable die to cavity size ratios, has no effect on the performance of the system. It is assumed that the die is positioned ideally with respect to the package cavity. By ideally it is meant that the die positioning will introduce no other source or error in its positioning. Thus the die will be at a distance C from the reference corner of the package. The tolerances on the sides of the cavity range between 0.005" (130μm) and 0.008" (200μm) in the two coordinates on the plane of the cavity. Thus the die will be expected to lie within 0.007" (180μm) and 0.011" (280 μm) for the best and worst cases respectively, of its desired position at the center of the cavity. The following diagram shows this in more detail.

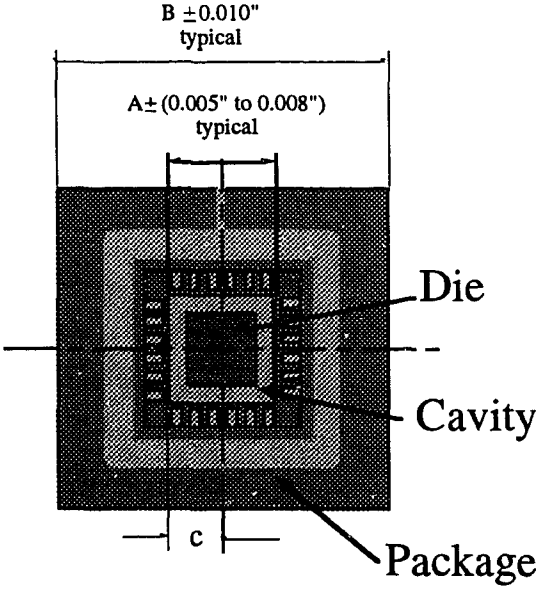

Figure 4.1 - Tolerance analysis for the packaging of smart pixel arrays using single chip carriers.

4.2.2 Package to board tolerance analysis

For QFPs, PGAs and other packages that required brazing of the leads of pins to the package, the leads or pins are manufactured with a tolerance of 0.008" in their position, giving an alignment accuracy of the package of 0.012" (305μm). This is based

upon the assumption that the package positional accuracy relative to a board is determined by the pin tolerance. It is later shown that the accuracy in the positioning of the package relative to the board will be less than or equal to this tolerance. The tolerances on the pads (for surface mounting) or through holes after plating (for pins) on the PCB vary among manufacturers, and are a function of cost. With typical numbers[8],[7], the tolerances can be seen to vary between ±0.001 " (25μm) and ±0.005 " (130μm). Using ±0.003 " (76μm), the maximum displacement is ±0.013 " (330μm).

4.2.3 Die to PCB positional accuracy

By adding the tolerances of the two levels of packaging in quadrature, the position of the die relative to the board is found to be within 0.017" (432μm).

The analysis then shows us that based upon the tolerances of the boards and carriers alone, the misalignment error will be in the hundreds of microns range. It is therefore important to investigate this alignment requirement and how this alignment requirement varies with smart pixel design parameters. This is studied in the following sections. Also, the alignment accuracy provided by the packaging alone must be assessed in terms of whether it will serve system alignment requirements. It will become evident that the packaging of dies will have to include means of alignment other than the packaging alone.

4.3 Theory for the misalignment of Gaussian beams on square detectors

The analysis of this section will provide the theoretical basis for the alignment of Gaussian beams on square detectors, and will be used to quantify the effect of window size, smart pixel density and array size on the power coupled and maximum allowed misalignments. The irradiance of a Gaussian beam focussed on a plane is given by

$$I = I_0 \cdot \exp\left(-2\frac{(-2(x \pm \Delta x)^2 + (y \pm \Delta y)^2)}{w_0^2} \right) \qquad (4.1)$$

where w_o is the spot size and Δx and Δy are the misalignments in x and y respectively.

The power coupled as a function of position in x-y ($x+\Delta x$ and $y+\Delta y$), is the integral of the irradiance over the window area. This can be seen to be given by

$$P = I_o \frac{w_o}{8}\pi \left[\operatorname{erf}\left(\frac{d_1/2 - \Delta x}{w_o/\sqrt{2}} \right) - \operatorname{erf}\left(\frac{-d_1/2 + \Delta x}{w_o/\sqrt{2}} \right) \right] \left[\operatorname{erf}\left(\frac{d_1/2 - \Delta y}{w_o/\sqrt{2}} \right) - \operatorname{erf}\left(\frac{-d_1/2 + \Delta y}{w_o/\sqrt{2}} \right) \right]. \qquad (4.2)$$

The normalized power coupling ratio, given by the ratio of misaligned power coupling to maximum (perfectly aligned) power coupling is given by

$$\frac{P}{P_{max}} = \frac{\left(\mathrm{erf}\left(\sqrt{2}\frac{(d_1/2)-\Delta x}{w_o}\right)-\mathrm{erf}\left(\sqrt{2}\frac{(-d_1/2)-\Delta x}{w_o}\right)\right)\left(\mathrm{erf}\left(\sqrt{2}\frac{(d_1/2)-\Delta y}{w_o}\right)-\mathrm{erf}\left(\sqrt{2}\frac{(-d_1/2)-\Delta y}{w_o}\right)\right)}{\left(\mathrm{erf}\left(\frac{d_1}{\sqrt{2}w_o}\right)-\mathrm{erf}\left(-\frac{d_1/2}{\sqrt{2}w_o}\right)\right)^2} \quad (4.3)$$

The effect of misalignment is shown in figure 4.2 where both the misalignment in one direction with the other direction perfectly aligned, and that of simultaneous misalignments in x and y of equal magnitude are shown. The plots are done for various spot sizes and fixed window sizes, and show that for small spot size to window size ratios, the decrease in power is not as high as that of larger spots for the same misalignment, however drops in a more abrupt fashion, being less tolerant to larger misalignments. For the case of the spot size w_o being one fifth of and equal to the window side dimension, it is more advantageous as far as the misalignment tolerance to use the latter if the required power coupling is less than 75% and 60% in one and two dimensions respectively. However, most systems will require over 80% power coupling, showing that larger windows, relative to the spot size will be better as far as power coupling.

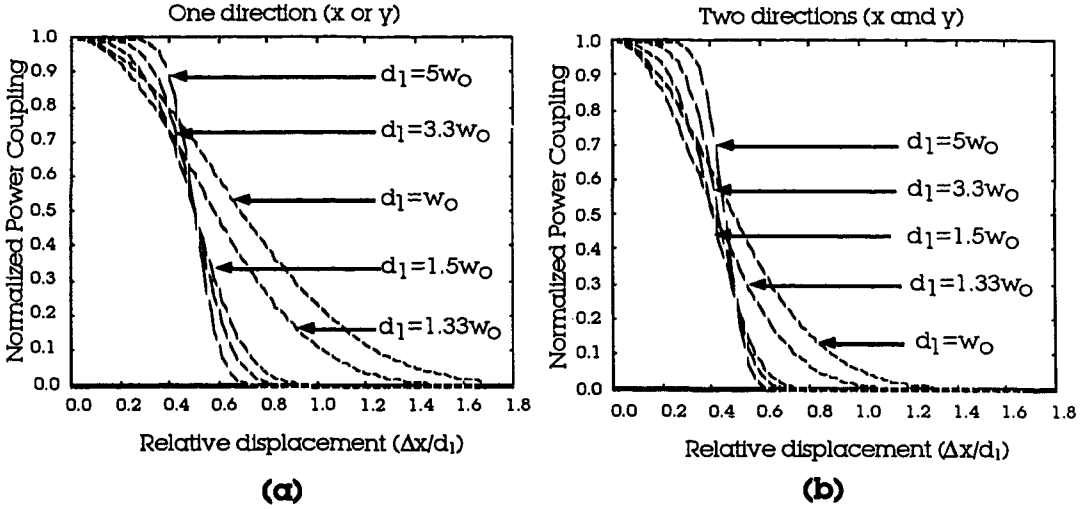

Figure 4.2 - Power coupling efficiency vs. lateral misalignment for (a) one direction only, and (b) two directions simultaneously for different spot size to window ratios.

For the purpose of finding the maximum misalignment tolerance for a given power coupling efficiency, the value of Δx for a given normalized power coupling efficiency is desired. This maximum displacement or misalignment Δx or Δy in a specific direction is

not directly solvable due to the nature of the error function. This will be analyzed further in section 4.5.

The power coupling as a function of misalignment in z is dependent on the size of the waist on the device plane. The size of the waist as a function of misalignment along the axis of propagation of the light Δz_e for a Gaussian beam is given in [9] to be

$$w = w_o \sqrt{1 + \left(\frac{\lambda \Delta z_e}{\pi w_o^2}\right)^2} \tag{4.4}$$

where w is the waist, w_o is the spot size and λ is the wavelength of the light. Thus the power coupling can be obtained as function of z misalignment by combining equations (4.3) and (4.4). Figure 4.3 shows how the power coupling decreases as the spot size increases for different spot sizes and window sizes.

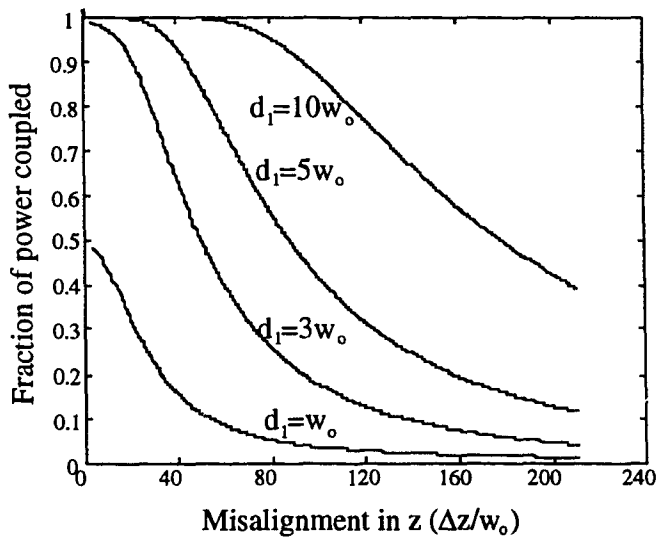

Figure 4.3 - Plot of the defocus effect on power coupling for w_o=5μm.

For large window to spot size ratios, the defocus can be very large in magnitude before the optical power coupling is decreased considerably. Large windows thus, are favoured from an alignment point of view, however, as it was previously seen, the smart pixel density and the amount of logic per smart pixel will limit the size of the window sizes.

4.4 Optical backplane alignment requirements

In order to be able to relate the packaging positional accuracy to system requirements and hence develop a set of constraints on the design space for smart pixel arrays,

the basic optical interconnect has to be analyzed from two technology perspectives. The two technologies that can be used in an optical backplane to transmit data between the nodes are surface emitting device or laser (SEL) based systems and modulator based systems. The former uses devices which can emit light under given electrical bias conditions which are used to generate light with a given bit pattern. The latter uses an external light source, or optical power supply, and has the devices either reflect or absorb that light under given bias conditions. In both instances the light is detected by detectors and receiver circuitry. The alignment requirements are different for both systems, and are of interest for the analysis to follow later in this chapter. These different requirements are outlined qualitatively in sections 4.4.1 and 4.4.2, while a quantitative analysis comparing the two approaches is done in section 4.4.3.

4.4.1 Surface emitting based systems

The main advantage in using SEL based systems, is related to the compactness that can be achieved in the optical system as the modulated emitted light is generated at the device arrays, thus requiring no optical beam splitting optics along the path. In addition, the optics can be made very simple. Among the disadvantages, we can mention the fact that most surface emitting devices have very strong beam divergence due to a combination of a small spot size and diffraction effects at the aperture, therefore they require very fast optics to capture most of the light they generate. This affects the tolerance in the direction along the optical axis of the system. The use of prealigned lenslets to the die has been an alternative to overcome this problem. In such systems, the alignment tolerance in the z direction between the device and the lenslet becomes critical but can be achieved through prealignment or in the manufacturing process under controlled conditions. The separation between the packages, through this technique, sees a more relaxed alignment tolerance.

The densities achieved in arrays of surface emitting devices are on the order of 1000 cm^{-2} [2],[11],[12], however only small arrays (up to 8x8) have been reported[10]. In such arrays simultaneous operation of all devices in the array was not possible. This, as it was discussed in chapter 2, is affected mainly by thermal crosstalk between the devices, which results in some devices being turned on by the adjacent ones[11],[10]. Under such densities, the optical crosstalk between devices will have a very small effect on system performance.

The analysis of optical crosstalk is beyond the scope of this comparison and will not be treated further.

4.4.2 Modulator based interconnects

The need of an external optical power supply in modulator based systems adds complexity to both the alignment and the optical system between the two device arrays. Board-to-board or inter-array plane separation will experience an increase in magnitude as the addition of beam-splitting and polarizing optics is required. Also, in modulator based systems, the alignment problem is complicated by the addition of optical power supply alignment, that is, the alignment of the sub-system in charge of the generation of light impinging on the modulators. Assuming this is dealt with and the array of spots on the modulator set the reference to which the devices need to be aligned, it can be seen that the coupling of power for this type of system will be of a different nature than that of SEL based system in the transverse direction to the optical axis (or along the device plane). Tilts of the modulator array result in the beams being reflected at an angle resulting in a translation in the transverse direction at the lens and the possibility of clipping of the light. The net result of tilts is a translation in the longitudinal direction or in z, as well as spot profile deformation. It is worth noting that tilt will result in reflection at twice the tilt angle relative to z. This is not the case for SEL based systems, where tilt results in the beam being emitted at the tilt angle.

Although modulator based systems might have less diverging beams, the tolerance in the longitudinal direction is also critical, and will be seen to be lees tolerant to misalignment than for SEL based systems. This will be assessed quantitatively in the following sections.

4.4.3 Comparison between different approaches

For the purpose of comparison between the alignment requirements of surface emitter based systems and modulator based systems, and in order to normalize this brief analysis, a 4f telecentric system as that shown in figure 4.4 is assumed for the optics. The implementation of such system can be through micro-optics (lenslet arrays), or bulk optics. The latter will have a limited field of view and will limit the size of the array for a given density if aberration free spots are desired.

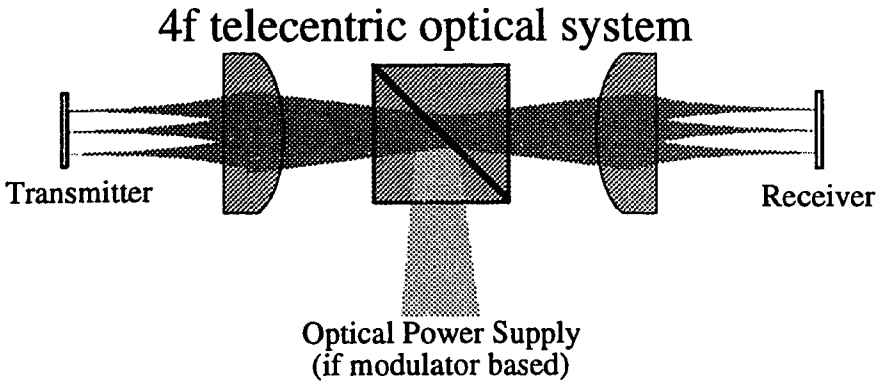

Figure 4.4 - System used for the purpose of normalizing the comparison between SEL based and modulator based systems.

As can be seen in figure 4.5, the transverse misalignment (Δx_e, Δy_e) resulting from misalignment of the light source array in SEL based systems (Δx_{eSEL}, Δy_{eSEL}) and that of the detector array (Δx_{eDET}, Δy_{eDET}) is given by their addition in quadrature

$$\Delta x_e, \Delta y_e = \sqrt{(\Delta x_{eSEL}, \Delta y_{eSEL})^2 + (\Delta x_{eDET}, \Delta xy_{eDET})^2}. \qquad \textbf{(4.5)}$$

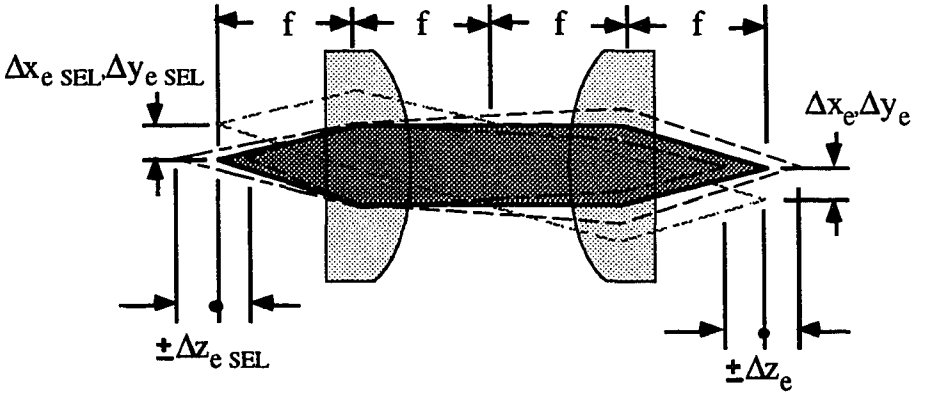

Figure 4.5 - SEL based system misalignment in all three directions.

The misalignment in z is somewhat more complex, however using the thin lens formula[13] for the above optics and as shown in figure 4.5, the total misalignment in z is given by

$$\pm\Delta z_e = \sqrt{\left(\frac{\pm f \Delta z_{eSEL}}{f \mp 2\Delta z_{eSEL}}\right)^2 + (\Delta z_{eDET})^2} \qquad \textbf{(4.6)}$$

with, again both contributions from the SEL and the detector being added in quadrature.

For the case of modulator based systems, the effect of misalignment along the optical axis of the modulator array plane (defocus) results in twice the misalignment along this axis as far as the beam is concerned because of the fact that it is being reflected when modulated. This misalignment is shown graphically in figure 4.6 and given by

$$\pm\Delta z_e = \sqrt{\left(\frac{\pm 2f\Delta z_{eTX}}{f \mp 4\Delta z_{eTX}}\right)^2 + (\Delta z_{eDET})^2}. \qquad (4.7)$$

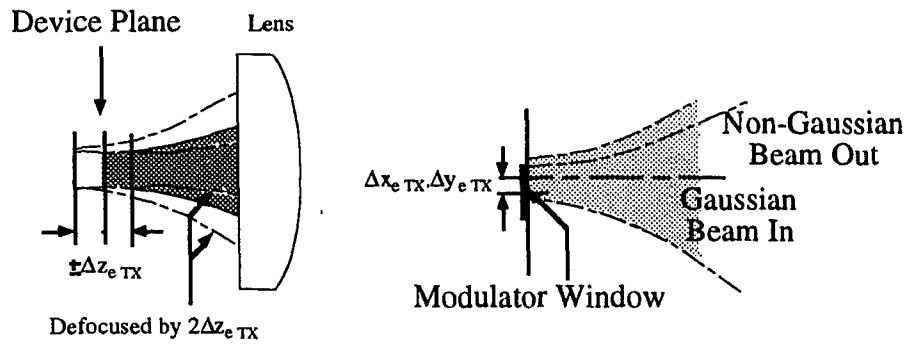

Figure 4.6 - Misalignment in all three directions for modulator based systems.

The misalignment in the x-y plane of modulator based systems is somewhat different than that of the SEL based system approach. Misalignment in x-y of the modulator array results in reflected beam clipping which results in non-Gaussian beam behaviour and more divergence. In addition, part of the light is not absorbed at the absorbing state, and less light is reflected at the reflecting state, resulting in a smaller contrast ratio between the two states.

In the plot to follow (figure 4.7), 15μm windows are assumed for 5μm spot sizes, resulting in 3*w* or 99% power coupling under perfect alignment. The power coupling efficiency for z misalignment is done for three different focal lengths with increases of 10mm and starting at 5mm.

It can be seen that the tolerance to pure misalignment in z is better for SEL based systems. This translates also to misalignment due to tilt about the axis on the device plane (x and y), as the net effect under the 4f system conditions is a non uniform translation along the z direction of the devices on the array.

A comparison between the expression for the misalignment in the x and y directions for the two approaches shows that in the SEL case, pure misalignment in x-y results in the addition of two independent displacements. For the case of modulator based

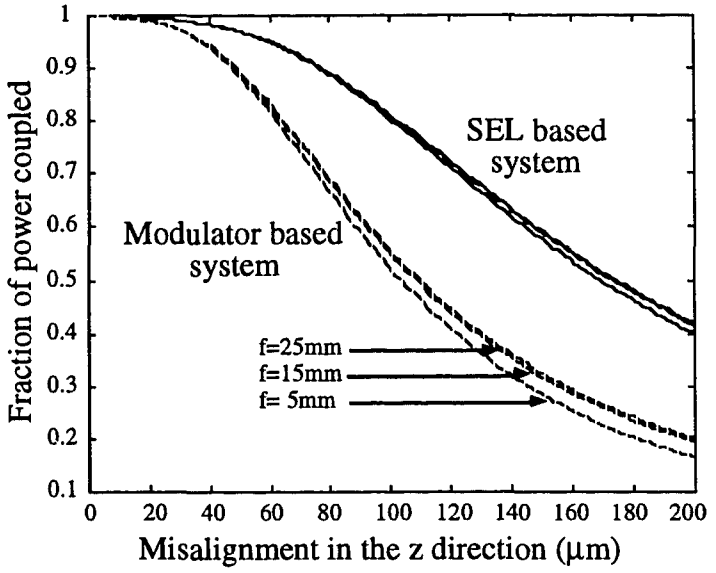

Figure 4.7 - Comparison of misalignment in z for SEL vs. modulator based systems.

systems, the effect of misalignment of the modulator array reduces the power reflected to the receiver array, but does not introduce a net displacement of the beam, assuming the non-Gaussian beam will not have larger divergence. Thus the net misalignment in x and y

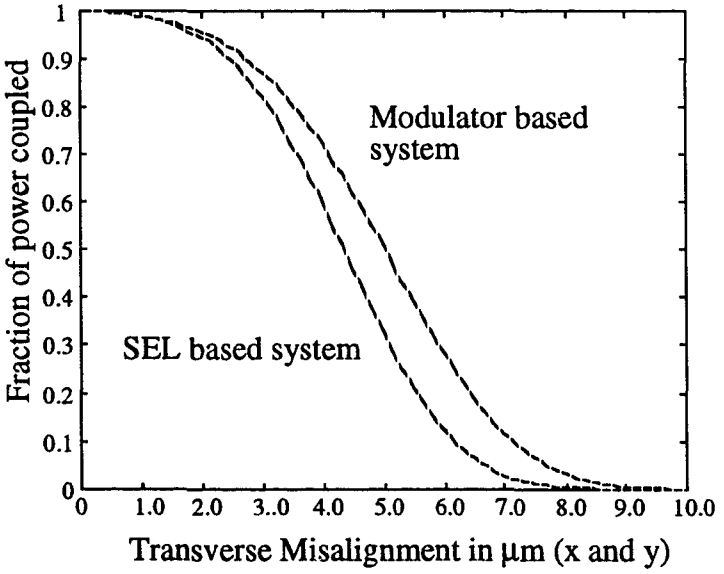

Figure 4.8 - Comparison of misalignment in x and y for SEL vs. modulator based systems.

is only due to that of the detector array. Therefore, modulator based systems are more tolerant to pure x-y misalignment than SEL based systems, neglecting the diffraction effects introduced by the clipping of the modulated Gaussian beam. The plot of figure 4.8 shows this result.

The other degrees of freedom, such as tilt about x and y, and rotation about z will result, to first order, in a combination of defocus (misalignment in z) and translation in x-y. Clipping of the beams at the lenses due to tilt of the device array, as well as translations for the modulator case, will result in beam aberrations and increased divergence, and will affect modulator based system in a stronger way. A tilted image plane in a bulk optics implementation will result in uneven defocus of the devices in the array. This defocus, if the assumptions used so far are applied, will favour the SEL based system. It is important to note however, that for a lenslet based system, a tilt of $\Delta\theta$ in the device plane, results in the light from the SEL going off at an angle of $\Delta\theta$ with respect to the optical axis of the system. For a modulator based system, this angle becomes $2\Delta\theta$, which, for small angles, will double the misalignment of the beam on the lenslet, increasing the clipping of the signal.

Something important and worth noting is the fact that both systems are more sensitive to misalignment in the transverse plane to the optical axis (or device plane), than to defocus or misalignment in z.

For both cases however, the difference is large. It is seen that for 80% power coupling with $3w_o$ windows and w_o=5μm, SEL based systems and modulator based systems will allow 3μm and 4μm x-y misalignment respectively. The z misalignment will be around 100μm and 60μm respectively for the same system. This shows how much more susceptible the misalignment in x-y is to that in the z direction.

In the following section, the geometry of the smart pixel array will be seen in terms of how it affects power coupling under misalignment. This will lead to a design space definition for smart pixels arrays constrained by alignment issues.

4.5 Design space analysis and constraints from the alignment point of view

Based upon the smart pixel cell and array defined previously in chapter 2, a set of expressions governing the translation due to misalignment as a function of smart pixel cell

parameters will be derived. It is important to note that since parameters such a[illegible]dow size, smart pixel density and array size will be related to a misalignment in x-y, only rotation about z and translation in x-y will be studied.

4.5.1 Rotation about z misalignment

The effect that rotation about the optical axis of the system (z) has on misalignment is a net translation in x and y. The net translation of a point at (x_o, y_o) from the axis about which the plane is rotated by $\Delta\theta$ is Δx_r, Δy_r given by

$$\Delta x_r = x_o(\cos\Delta\theta - \sin\Delta\theta - 1) \tag{4.8}$$

$$\Delta y_r = y_o(\cos\Delta\theta + \sin\Delta\theta - 1)\,. \tag{4.9}$$

Rotation will then affect the most distant point from the axis of rotation the greatest. The location of x_o and y_o is then at the corner of the arrays as seen in figure 4.9.

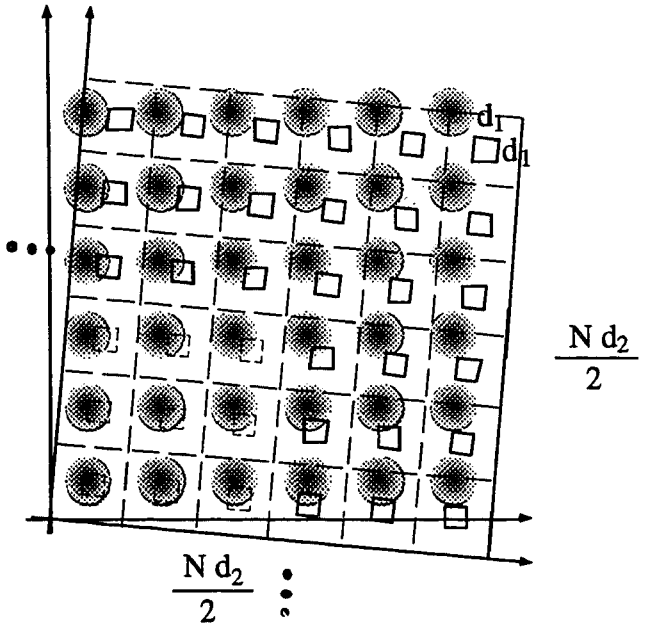

Figure 4.9 - Illustration of the net translation resulting from rotation.

The maximum allowed rotation misalignment can be that of the worst position in the array, and will depend on the size of the array, dependent on the number of smart pixels and the smart pixel density.

4.5.2 Translation misalignment

The translation misalignment can be incorporated in the x_o, y_o terms in a translate then rotate scheme and results in the following equations:

$$\Delta x = \left(\Delta x_T + \frac{(N-1)}{2} d_2\right)(\cos\Delta\theta - \sin\Delta\theta - 1) \qquad \textbf{(4.10)}$$

$$\Delta y = \left(\Delta y_T + \frac{(N-1)}{2} d_2\right)(\cos\Delta\theta + \sin\Delta\theta - 1)\,. \qquad \textbf{(4.11)}$$

However, equation 4.10 and equation 4.11 couple the translation due to rotation to that due to pure translation. and results in a larger misalignment.

Let $\varphi = \cos\Delta\theta - \sin\Delta\theta - 1$, so that the translation in x due to rotation of the corner detector is $\Delta x_R = \frac{1}{2}(N-1)\, d_2\varphi$, with N and d_2 as defined in chapter 2. It can then be seen that combining rotation and misalignment results in two translations such that $\Delta x = \Delta x_T + \Delta x_R$. It is worth noting that by doing this, we are decoupling the rotation misalignment from the translation by effectively first rotating and then translating. Now, if we express the translation misalignment in terms of the total misalignment as $\Delta x_T = q\Delta x$, and $\Delta x_R = (1-q)\,\Delta x$, the total misalignment can be expressed as

$$\Delta x = \frac{(N-1)\, d_2\varphi}{2(1-q)} \qquad \textbf{(4.12)}$$

In this case, q is the fraction of the total misalignment in x that is due to pure translation misalignment, which affects identically every device in the array.

The design space analysis, in contrast to that from the packaging thermal constraints point of view, is divided into two parts. This is a result of the decoupling the window size, array size and smart pixel density, have as far as alignment. The first part will deal with window size, which is affected by the displacement due to translation of the array, while the second part will deal with array size and density, depending on the transverse displacement due to rotation. It is noted that the two can be combined and are related by the total displacement and the previously defined displacement ratio.

From equation 4.3 the maximum allowable displacement for a given power coupling (with respect to perfect alignment) can be obtained. This displacement will have translation and rotation components with ratio defined by q in equation 4.12. The question

that remains to be asked is what spot size is to be used as the optoelectronic device windows are increased in size? The plot below show the power coupling for a range of spot size to window ratios.

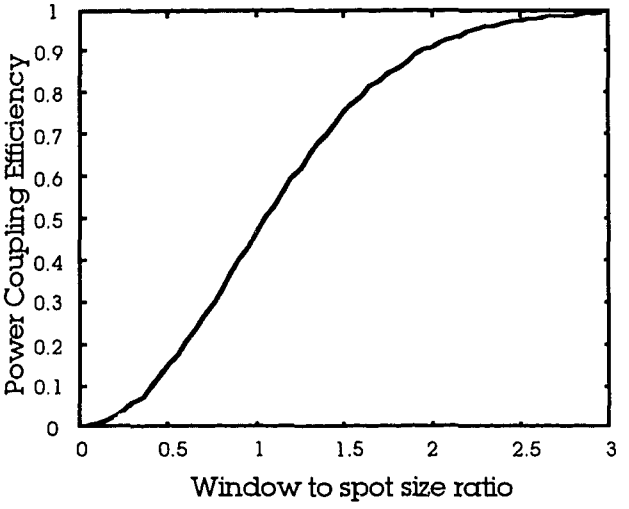

Figure 4.10 - Power coupling plotted against the window to spot size ratio (from equation 4.1).

The maximum misalignment that results in 80% power coupling is plotted as a function of window size for various spot sizes. In the plot of figure 4.11, the power coupling ratio of 80% is relative to the maximum achievable power coupling. Thus, true 80% power coupling is achieved only for windows larger than $3w_o$.

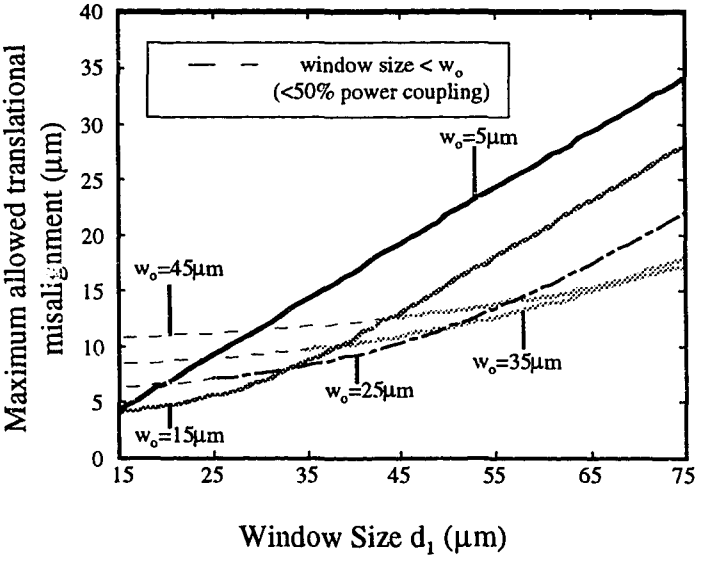

Figure 4.11 - Maximum allowed translational misalignment for 80% power coupling against window size.

For spot sizes up to 15 μm, and total power coupling greater than 80%, windows between 25 and 45 μm will allow between 10μm and 20μm misalignment. If greater tolerance is required, the window sizes have to be increased as shown in figure 4.11. It can be seen from the tolerance analysis that packages will not be able to provide such positional accuracies, thus other means of alignment will have to be sought. For 5μm spot sizes or less, the tolerance to misalignment is larger for large windows than it is for larger spot sizes. With such spot sizes, alignment tolerances of 25μm or greater will require 55μm or greater window sizes. This puts constraints on the density, as the windows occupy a larger area.

The allowed densities are plotted below for q ratios of 0.5 and 0.25, as defined previously, and for 32x32 smart pixel arrays. For translational misalignment around 15μm, densities between 1000 cm^{-2} and 10000 cm^{-2} will result in rotational misalignments of 0.002 to 0.004 radians (or 0.1 to 0.2 degrees). For q=0.25, which implies allowing the total misalignment to be mostly due to rotation, the same range of densities will allow rotational misalignments between 0.002 and 0.005 radians (0.1 to 0.25 degrees). Smaller arrays, such as 10x10 arrays for the same densities will allow approximately 0.006 and 0.012 radians (0.3 and 0.6 degrees) for q=0.5 and 0.006 and 0.015 radians (0.3 and 0.75 degrees) for q=0.25. This, again, leads in the direction of system partitioning.

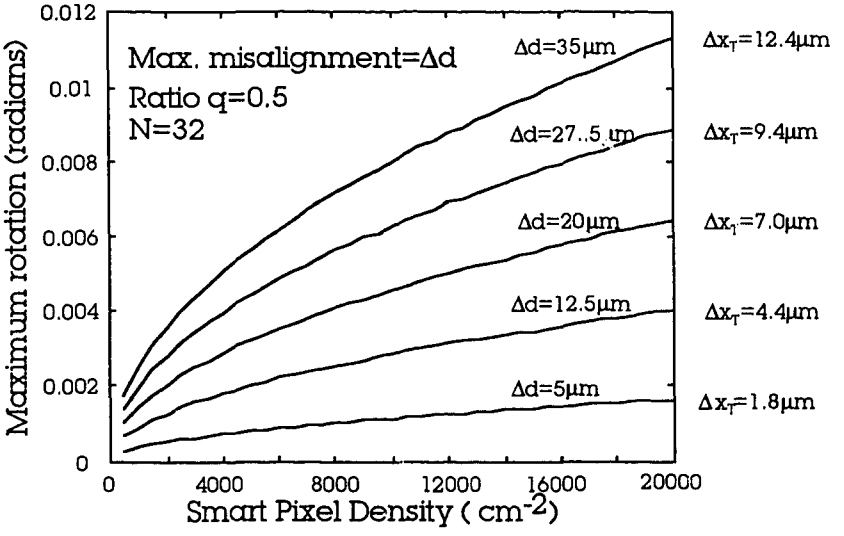

Figure 4.12 - Maximum rotation as a function of density for fixed total translational misalignment. Plot for q=0.5

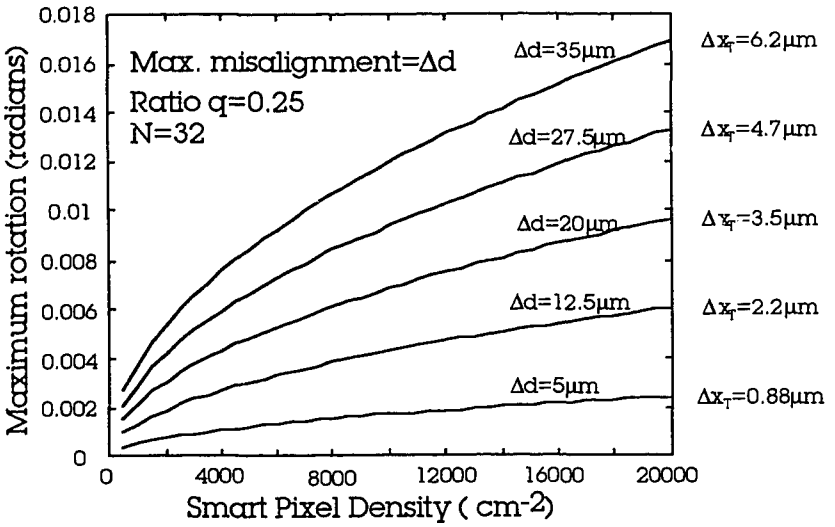

Figure 4.13 - Maximum rotation as a function of density for fixed total translational misalignment.Plot for q=0.25

The above analysis shows how sensitive to x-y misalignment the smart pixel array is. Clearly, the misalignment introduced by the packaging will be much larger than that tolerated by varying system parameters, so the effect of changing smart pixel window size, density and array size to improve the alignability of the system is small. Nevertheless, the results obtained allow us to have alignment requirements to aim for when designing optomechanical systems, and when introducing alignment sub-systems in the optics, as will be seen in chapter 5.

4.6 Multiple chip alignment considerations

One issue that needs to be discussed is the alignment of multiple dies in one board. It has been seen in chapter 2, that a partitioning of the channels is required when designing a system with about 10000 optical channels[14],[15]. It is therefore crucial that the analysis on how this partitioning affects the alignment be done. The following section will be a discussion on how individual die tolerancing affects multiple die tolerancing and alignment. Following, a discussion of the effect of soldered pin, pad or contact tolerances on the overall package alignment accuracy is done, exploring the possibility of multiple die alignment.

4.6.1 Individual package tolerancing effects on multiple die alignment

When dealing with a single die on a single die carrier, alignment of the die through optomechanics can be possible, as the whole set of optics moves as a group to be aligned

with respect to the device arrays, or vice versa. Thus, the two units can be moved independently from one another to achieve alignment. If the optical system is composed of two separate optical trains which are mechanically coupled, the alignment must be made at the device array level, as now we have more than one device array, yet still only one optical system. One approach is to have the dies independent or mechanically decoupled from one another, however the advantage in the connectivity gained through the use of smart pixel arrays is decreased as the optomechanics and electrical connectors needed to support the device arrays are independent units requiring a given physical space. The other approach is that of introducing optomechanics that interface to many dies on a single module. This results in a reduction in the optomechanics size and takes advantage or the routing capabilities of boards or multi-chip modules. In this case we are back to two units that need to be aligned to one another: the optical system and corresponding optomechanics, and the devices, packaged in a single board or multi-chip module. However, motion of any of the two units to align one device array, will result in misalignment on the other device arrays unless the device arrays are perfectly aligned relative to one another. Using optomechanics, an optimum position can be reached where all device arrays are receiving the same amount of light. Depending on the alignment accuracy of the individual packages, this coupling will be lower or higher. The misalignment will then be required to be compensated through means of alignment within the optical system. Such approaches will be discussed in chapter 5. For this, the alignment accuracy that can be achieved in multiple dies on a single module is required. Earlier in this chapter a tolerance analysis on chip to board tolerancing showed alignment accuracies of hundreds of microns. The analysis was based solely on the tolerances on pin and lead positions, and general package manufacturing tolerances. The following section will discuss the application of alignment through soldered pins, pads, in the context of self-alignment.

4.6.2 Multiple dies on a single module

If an arrayed package is used which has pins or balls with a given tolerance, self alignment principles can be applied to align them on a board relative to one another. Self alignment techniques through solder reflow have been used to align devices to lenslets, and in systems[4],[3],[16], and micron resolution alignment has been achieved. The use of

such techniques can be used to provide alignment of multiple packages on boards, or on modules. The principle for self-alignment is that of energy minimization, where the surface tension of the solder balls during reflow shapes the solder to its most favourable energetic state[4],[18]. For BGAs with pads with a given tolerance, and assuming a Gaussian distribution in their position around the ideal position relative to the package, the solder in each pad would pull against the others. Clearly, for an infinite number of pads, the pads compensate for each other, bringing the package closer to its ideal position. Intuitively, the position of the package will have a standard deviation smaller than the tolerance on the position of the pins. For a worst case scenario, in which the position of all pads in the BGA are offset by the given tolerance in the same direction, the misalignment of the package will be the tolerance on the pins. This is also true for PGAs in sockets, in which each pin will experience a restoring force due to the socket spring contacts and due to their own spring-like properties as they are bent under non-ideal position. One thing to point out is the fact that the restoring force is proportional to the misalignment, thus perfect alignment of the packages with the solder in each pad pulling against each other is not possible. It is however possible to intentionally offset the pads on the package from the wettable pads on the board and have the solder pull against a stop. This technique has been used to achieve micron resolution accuracies[17],[4].

Reported experiments show that alignment accuracy of 5μm or less can be achieved through solder self alignment[19], and that this alignment accuracy decreases with solder diameter. The results also show that an increase in the number of pads and solder contacts favours the alignment accuracy. If the results are extrapolated to solder volumes as those of BGAs, alignment in the tens of microns can be possible.

The key result from this is the fact that multiple die alignment on a single board can be done, as the package can provide coarse alignment of around 50 microns or less. The fine alignment can then be done through optomechanics, or through other means of alignment, within the optical system, which will be discussed in chapter 5.

4.7 Conclusions

The system alignment requirements were analyzed for two different approaches, showing that for both, the transverse alignment is the most critical as far as power

coupling. It was also seen that modulator systems are much more susceptible to misalignment as the degrees of freedom of the system are more numerous. With the numbers seen from the alignment tolerances and alignment accuracies that can be obtained from the packaging alone, the requirements proved to be tighter than what standard packaging techniques for the microelectronic industry can achieve. Based upon other alignment techniques, such as self-alignment, optical, or optomechanical means of alignment, alignment accuracies on the order of 10 μm can be obtained. The design space parameters can then be adjusted to provide a prescribed minimum power coupling under such misalignment magnitudes. It was seen that 25 to 45 μm windows combined with densities between 1000 and 10000 cm^{-2} for up to 32x32 arrays were a good combination to match the alignment that can be achieved through simple, low-cost optomechanics or alignment techniques.

The alignment of multiple packaged dies on a common second level package was also discussed. Mechanical techniques will allow positioning of these dies to within tens of microns, and the use of self alignment through solder balls or pins on sockets can potentially solve the alignment problem.

To conclude this chapter, it is worth mentioning that although the analysis of the capabilities of packages yields large misalignments, the figures mentioned are worst case figures, which correspond to what is standard in the area of microelectronics. Better toleranced boards and packages could be manufactured, however the advantages they would provide must be weighed against their cost.

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Chapter 5

Alignment and packaging techniques for optical backplane demonstrators

5.1 Introduction

The alignment of two dimensional arrays of optoelectronic devices to provide an optical link between them is the most crucial factor in the performance of the system. Chapter 4 showed the required alignment accuracy that would allow a fraction of the optical power to be coupled and discussed the smart pixel design parameters that affect the system tolerance to misalignment. It was seen that means of alignment were needed to meet the alignment requirements. These means are discussed in this chapter, starting with a review of optomechanical and optical systems, followed by a discussion of these systems outlining their strengths and weaknesses and pointing out their applicability to optical backplane systems. Section 5.2.2 will introduce the concepts of decoupling the optical channels from the electrical boards, through a proposed scheme that utilizes the less stringent alignment requirements of electrical contacts. The concepts will then be extended to the optomechanics of the Phase II VCSEL-MSM demonstrator, where the work done at McGill in the system optomechanics will be described. As a result, the addition of means of aligning the degrees of freedom that were not dealt with in the Phase II demonstrator will be presented through the design, implementation and characterization of PCB optomechanics which allow tilt and translational alignment (tilt/z). The chapter will conclude with a discussion of the designed alignment tool and future directions.

5.2 Alignment techniques for two dimensional optoelectronic device arrays

Alignment of two dimensional optoelectronic device arrays relative to an optical system can be obtained through two approaches: through the use of optomechanics, and through the use of optical elements along the optical path of the interconnect. These techniques can be used to provide various degrees of alignment, and in most systems are combined to achieve a prescribed alignment accuracy. Simple optomechanical means of alignment can be used to provide coarse alignment, while optical means are used to provide fine alignment. More complex optomechanical systems, including high precision

micrometers/screws and/or positioners can be used to provide sub-micron resolution positioning of components[9],[4]. However, there seems to be a correlation or mapping between the size these optomechanical elements occupy and the resolution they can achieve. Section 5.2.1 will be an overview of the alignment techniques which utilize optical components within the system, while section 5.2.2 will review the optomechanical techniques used to achieve alignment.

5.2.1 Alignment techniques though optical system design

Alignment in the two coordinates on the device plane (x and y) can be achieved through beam steering with the use of Risley prisms[1],[2],[3],[5],[10]. The principle of Risley prism steering is based on the fact that light through a prism will be redirected at an angle relative to the angle of incidence. The angular deviation δ of the beam will be given by

$$\delta = (n-1)\beta \tag{5.1}$$

where β is the wedge angle, and n its index of refraction. A displacement of $r=f*\tan\delta$ will be then achieved at the focal plane of the system[2],[1] for a lens of focal length f. The whole transverse plane can be spanned by combining the action of two wedges. It can be seen that proper choice of the parameters can yield micron resolution alignment with maximum displacements in the 100 μm range. For instance 5 degree wedge systems with a lens of focal length of 10mm will have a range of 400μm. A 15 degree wedge with a 5mm focal length lens will have r=700μm. Other approaches based on the same principle for beam steering used variations in the index of refraction n in equation 5.19[8] through the use of liquid crystal microprisms and by varying the voltage to change n. In these demonstrations, resolutions of 10μm for over 3mm were shown.

Other degrees of freedom can also be compensated through optical elements within the optical system. Rotation can be compensated through a dove prism[8] and has been used to in systems to provide image rotation by any angle. The use of these prisms however is limited by their size, and will not be applicable to array to array (SEL type system) interconnects with small inter array separation. Its applicability will be mainly on longer optical path systems.

The alignment capabilities of the above methods require initial or coarse alignment to align the device arrays to within their range. As was mentioned earlier, coarse alignment through techniques such as self-alignment, or simple optomechanical assemblies will allow the use of such methods for fine alignment, while manipulation of the smart pixel parameters will reduce the requirement on alignment accuracy through the above techniques. In addition, their use must be assessed in terms of the cost in optical power and system compactness they will have.

5.2.2 Optomechanical techniques

In the design of complex free-space optical systems, in which multiple components have to be aligned relative to each other, the optomechanics need to provide alignment capabilities for 6 degrees of freedom for each component. These degrees of freedom as seen earlier are 3 rotations and 3 translations. It becomes evident that as the number of components gets large, the alignment of the system gets overly complicated, if not impossible. Adding drift of the components due to unstable optomechanics, the presence of springs, or components with backlash, the early systems had very short aligned state lifetimes. Multiple techniques to improve and simplify the alignment have been realized and implemented as the area of optomechanics evolved from the very early system demonstrators. The reduction of tensioned components and the introduction of modular prealigned setups is one of them[5],[7]. One of the most significant steps was the introduction of the slotted (v-grooved) baseplate in AT&T's $System_3$ and $System_4$[5]. This technique has been used extensively as it fixes the optical axis of the system, allowing a reduction in the degrees of freedom in most components in the system to two, as the optical axis of the system is defined by the slot in the baseplate. Careful alignment of the components within the holders was achieved through extensive and iterative prealignment steps[7], adding to the modularity of the optomechanics on the slotted baseplate.

In addition to the above, careful considerations on the optical system design to minimize the components, and to make them more tolerant to misalignment have been an integral part of optical interconnect demonstration.

The Phase I McGill Photonic systems group demonstrator used modified AT&T optomechanics and showed the use of a compact optical system in both a bulk and lenslet based system [3],[4]. In both cases the interconnect was a unidirectional board-to-board

interconnect using FET-SEED technology. The use of boards required them to be aligned in all six degrees of freedom. A positioning setup was used which was coupled to the baseplate, and consisted of a commercially available positioner modified to fit into the system and to interface mechanically to the boards (Figure 5.1). Electrical interface to the boards was achieved through SMA cables and complicated the alignment as they added tensions and stresses to the assembly with their stiffness and weight. It is noted that the system was designed to be tolerant to misalignments in x and y of 10μm in the lenslets, 5 μm in the input array, 50 μm in the receiver arrays, and rotations of 0.25 degrees in the device arrays[3]. The boards containing the device arrays lacked alignment capabilities in tilt about the horizontal transverse axis ($tilt_x$) and rotation about the optical axis of the system, however the overall system tolerances allowed the system to be aligned and to remain aligned. More stringent alignment requirements were met in the bidirectional interconnect using Phase I optomechanics, where the positioning setup was modified to allow alignment in one of the tilts not dealt with before. Rotation alignment was achieved through a dove prism in the optics, which also provided the required mapping of the transceiver array planes. While these demonstrators showed board-to-board interconnects, the emphasis was on the optical and the optoelectronic packaging of the system. It is worth mentioning that the package (QFP) to board interface was achieved through a high speed solderless contact, which was very tolerant to misalignment. Registration of the leads of the package was achieved coarsely, and were seen not to affect the transmission properties of the package as long as they stayed within the registration range (of about 400μm). This package was characterized for various package to board registrations and showed the characteristics of Figure 3.9 not to vary as far as bandwidth. This is important to note as it can be used to alleviate the alignment problem and will be discussed at the end of this section.

As the Phase I demonstrator system showed, the board to board interconnect alignment is something that needs extensive study. The use of positioners must be either driven toward more compact custom optomechanics or discarded altogether, as they occupy a large physical space. Chapter 4 showed that the alignment accuracy of the packaging alone will not match the system requirements, unless some advanced techniques such as self-alignment, pick-and-place, and custom optomechanics are used.

The remainder of this section will introduce a scheme which can potentially be used in optical backplane systems, and will lead the way toward the principles and concepts used in the Phase II Optical backplane demonstrator.

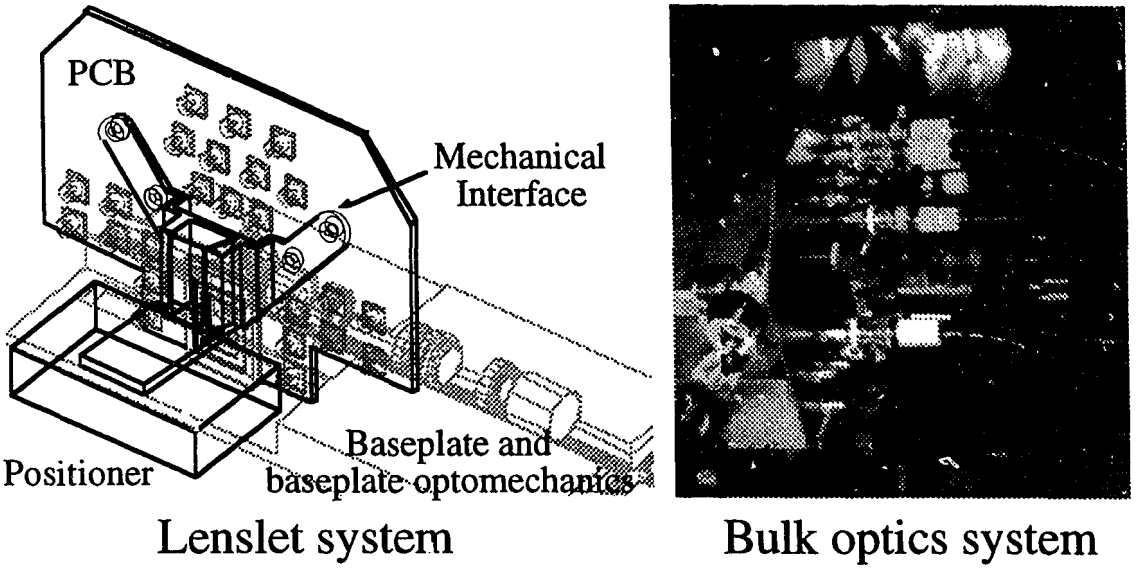


Figure 5.1 - Phase I packaging optomechanics for the lenslet system and for the bulk optics system.

In an optical backplane, a desired feature is that which allows insertion and extraction of boards. If these boards, which are the switching nodes that need to be interconnected, contain the optoelectronics on them, each extraction/insertion cycle will result in misalignment of the optical system. Even if the smart pixel arrays are perfectly aligned within the board, the board position relative to the rails it rests upon and that fix its position will be a source of misalignment.

The alignment required by the optical system on the packaging can be overcome through a prealignment of the optoelectronic device array and the optics. This would imply a separation between the boards and the optoelectronics. This is possible because of the fact that the tolerance in the position of the electrical contacts between package and boards is much larger than that required by the optical interconnect, and can be achieved through a mechanical guiding/registration setup. This is illustrated in figure 5.2 where the optoelectronic/optomechanics and optics form one unit and are coupled between one another.

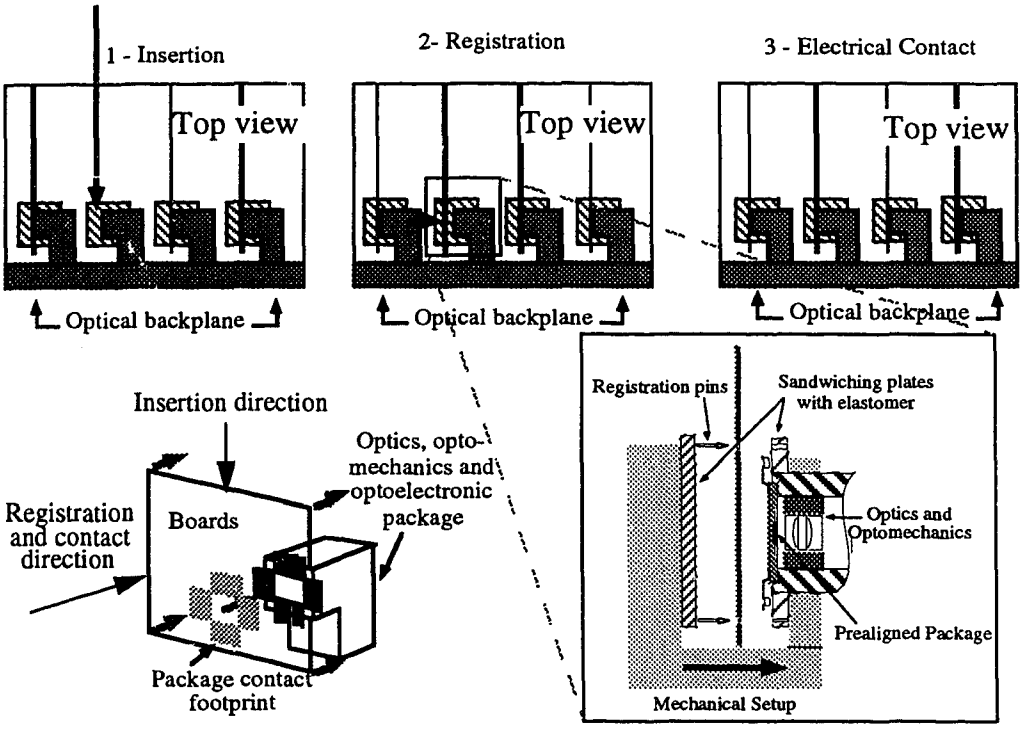


Figure 5.2 - Board insertion cycle: 1- Board is inserted, 2- pins achieve a registration of the board within approximately 200 mm, 3- Electrical contact is achieved by pulling the board toward the package. Note that the package is not pressed against the optomechanics as only the leads are manipulated and are flexible enough to not disturb a fixed and prealigned package.

The boards when inserted are guided to a mechanical setup, which sandwiches the leads from the prealigned package containing the smart pixel array, between the board pads or contacts and the optomechanical set up. This last step is done through an elastomer between the optomechanical setup and the leads which electrically insulates the leads and provides a spring force to ensure a good pressure contact between the leads and the board contacts. The prealigned package is coupled to the optomechanical setup containing the optics, thus its electrical contacts, or leads are the target for the board traces or pads to match during registration. The boards can have, in addition, guides which would direct the leads slightly to compensate for their misalignment relative to the board contacts.

The strength of this approach lies in the fact that multiple smart pixel arrays on one board can be supported, as the smart pixel arrays are prealigned to the optics. In addition, proper design of the pads can allow for better misalignment tolerances on the interface

between the first level package and the board. The weakness of this setup is related to the fact that a power-up of the smart pixel arrays must be done every time the boards are inserted. In addition a pad grounding procedure must be performed as the boards are inserted in order to protect the device arrays. Although the mechanical system which is to provide the sandwiching of the leads must be compact, its design can be rather simple.

The evolution of free-space optomechanics has shown that modular and simple approaches as well as the removal of tensioned components and degrees of freedom in the individual components, are better. Board-to-board interconnection alignment was seen to be simplified if the optical system and optoelectronics are decoupled from the boards to be inserted and extracted taking advantage of the tolerance of the electrical contact between package and board. The following section discusses this a step further and in the context of a decoupling between the switching nodes and the backplane.

5.3 Phase II Optomechanics

5.3.1 Different optomechanical approaches and concepts

Having seen the benefits that arise from the decoupling of the alignment sensitive optoelectronic device arrays from the boards which undergo insertion and extraction cycles, the design and construction of the Phase II optical backplane demonstrator is discussed. The approach taken for this system is that of mechanically decoupling the switching nodes or boards, and the backplane. As was mentioned in chapter 3, the requirement on connectivity into or out of the backplane is a fraction of the information through the backplane, thus a scalable high speed flexible connector[11] can be used to connect the boards to the backplane. This results in the concept of a motherboard and daughterboard, with the latter being part of the optical backplane. Thus, there is a one-to-one correspondence between the boards sending and receiving information into and out of the backplane and the daughterboards in the backplane. In addition, each daughterboard provide the first and second level packaging for the smart pixel as well as support

electronics. The arrays of devices used to provide the optical link between the daughter-

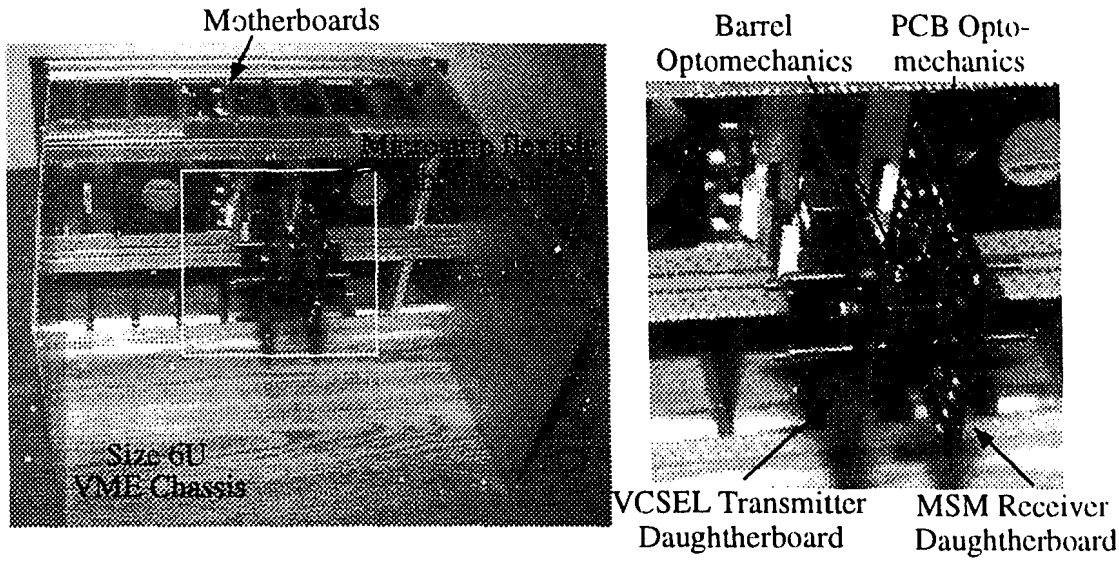


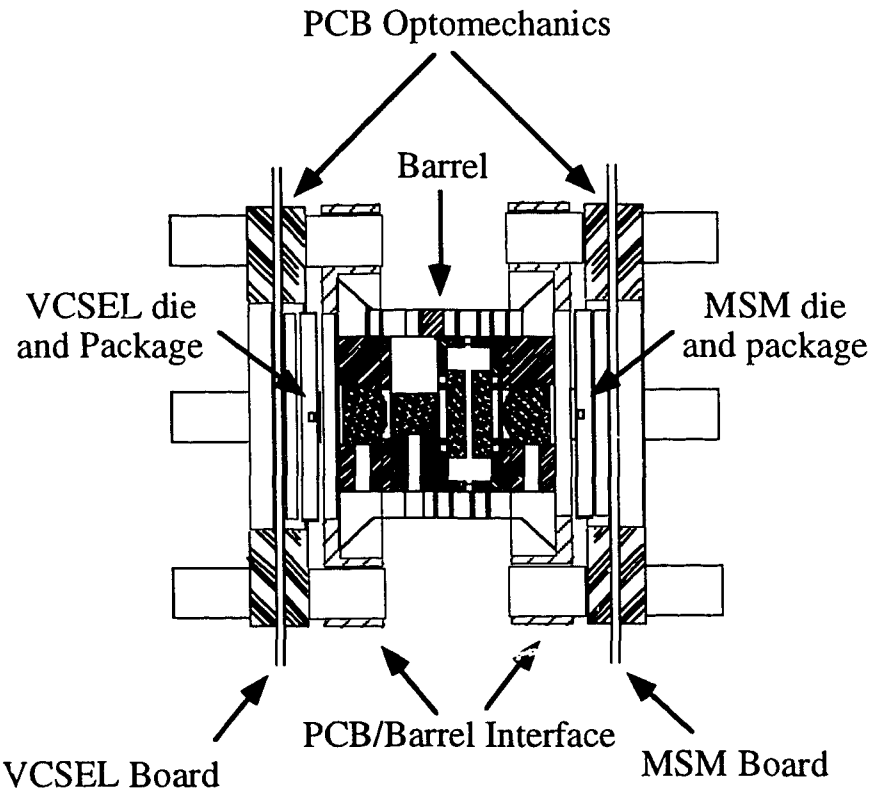
Figure 5.3 - Phase II VCSEL-MSM Optical backplane demonstrator hardware showing the concept of daughterboard optomechanics

boards were Vertical Cavity Surface Emitting Laser (VCSEL) device array for the transmitter, and Metal Semiconductor Metal (MSM) device arrays for the receiver. The light was relayed from the VCSEL plane to the MSM plane through a 4f telecentric system, with external imaging capabilities. The optomechanics of the system are described in the following section.

5.3.2 Phase II system optomechanics

The optomechanics of the Phase II VCSEL-MSM optical backplane demonstrator departed from the slotted baseplate optomechanical setup, and they introduced optomechanics that employ and adapt to a VME chassis. These are integrated into the back of a free standing VME 6U chassis as shown in figure 5.3. The concept of a daughterboard, was taken further in this system, and again following more of the ideas discussed earlier in this chapter, by coupling the optics and the optoelectronics. This was achieved by means of a mechanical interface between the optics optomechanics and the boards (Figure 5.4).

(a)



(b)

Figure 5.4 - Phase II VCSEL-MSM (a) board optomechanical interface and (b) system opto-mechanical assembly, showing the barrel, the PCB/Barrel interface and the PCB Optomechanics.

This interface allowed longitudinal (z) and transverse (x-y) alignment of the daughterboards relative to the optical system and to one another, and were coupled to the optomechanics containing the optical system. The interface also allowed external

adjustment of the rotation of the arrays relative to each other, with means of fixing the position once the desired rotation was achieved.

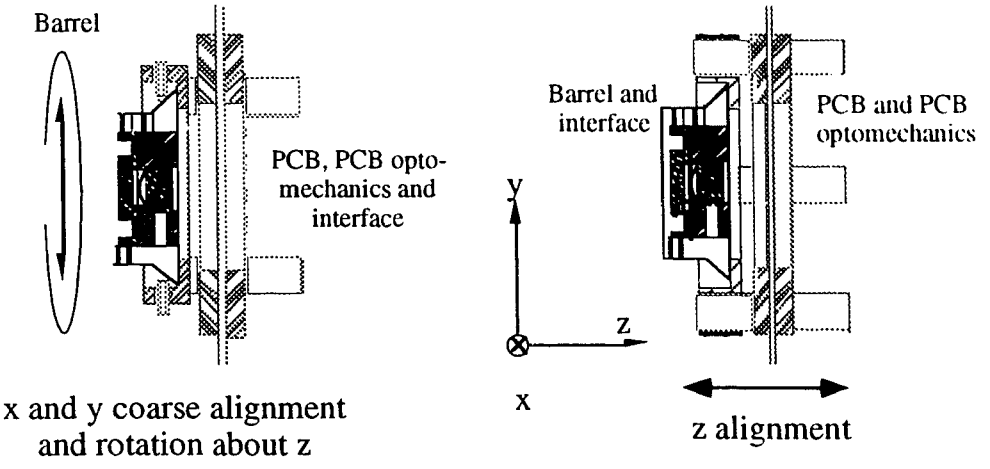


Figure 5.5 - Degrees of freedom adjusted through PCB optomechanics and barrel to PCB interface.

The adoption of a barreled structure to hold optical components, prealigned through the use of spacers was used. The barrel contains machined optical component holders with prealigned optics, and provides a bore-sited optical axis for these holders. The barrel optomechanics have tolerances between ±10μm and ±20μm while the daughter board interface tolerances are ±50μm. The barrel itself is fixed in position relative to the VME chassis, and the optomechanical interface allows the relative motion of the daughterboards relative to the barrel. The importance of a flexible connector between mother and daughter boards is evident here, as the boards are required to move independently relative to the chassis, and also as any motion of the boards results in a force being exerted on the optomechanics by the connector assembly.

Something to be pointed out is that neither the die to package alignment tolerance nor the package to board alignment tolerance, are critical for the alignment of the system as the daughterboard optomechanics are designed to compensate for these misalignments. During assembly, the optomechanics easily allow the spots generated by the SEL array to be placed within less than 50μm of their required position. Additional alignment is provided by the Risley Steerers within the optical system which have a range of 80μm and resolution in the micron range. The positioning capabilities of the optomechanics in this system have a theoretical resolution of 10μm, the compactness of the system, as well as

the fact that two actuators must be adjusted simultaneously, allowed a resolution of ± 4 to ± 6 μm in the transverse direction to the optical axis of the system.

Alignment in the directions not handled by the optomechanics is achieved through prealignment steps. The first prealignment step is the adjustment of the tilt of the packaged die relative to the board, and hence relative to the optomechanics, necessary because of the die to package tilt and package to board/optomechanics tilt that arises when the die is glued in the package cavity and when the package pins are inserted in to the socket receptacles. The combined tilt (about the two transverse axes) was as high as ± 2.5 degrees. The assembly included a prealignment stage that positioned the die to within 0.25 ± 0.12 degrees. The prealignment could not be done to better values of this tilt as the tilt was adjusted by varying the position of the package relative to the socket. After upgrading the system to custom high speed PCB assemblies, the MSM die package was soldered directly to the boards, showing the tolerance of the system to tilt about x and y to be rather high.

The alignment in the longitudinal direction or along the optical axis of the system, was achieved by externally pushing the boards attached mechanically to the barrel, and through the optomechanical piece of figure 5.5. As it can be seen, the rods allow for adjustment in the z-position, but do not provide the means to do so. Thus, an external positioner, used only during assembly is used to push the board and hence adjust the distance between the lens and the devices.

The alignment of the system was preserved, showing 0.0 ± 1.0 μm transverse (x-y) misalignment due to drift over 3 weeks, and with thermocycling of 5 degrees over 24 hours. In addition, the system also was tested under board insertion and board extraction, showing no misalignment after over 30 insertion/extraction cycles. Finally, both the introduction of mechanically coupled fans to the chassis and shock on the daughterboards showed again no measured effect on the alignment of the system. The vibration coupling into the system was observed through an external imaging system to be in the micron range, however the system (both the optics/barrel and optoelectronics/daughterboards) moved as a whole, not suffering misalignment from this coupling.

The defocus, or translation in z due to drift was not quantifiable, as the spots did not increase in size by more than the experimental error in the measurements. However, alignment in this direction was critical, specially at the VCSEL array.

5.3.3 Phase II optomechanics upgrade

In view of the required prealignment stages and external alignment tools required during the assembly of the Phase II VCSEL_MSM system, a board-to-optomechanics interface was designed and tested that incorporates alignment capabilities along the optical axis (z) of the system and tilt about the transverse axis ($tilt_x$ and $tilt_y$). In the remainder of this section, this setup will be discussed, starting by describing the desired results and the technique used to achieve them, followed by a description of the experimental setup used to demonstrate this technique and ending with the results obtained.

The aim of this optomechanical assembly is to allow the adjustment of $tilt_x$ and $tilt_y$ as well as prealignment of the die in z relative to a datum or reference plane. This reference can be subsequently used as a reference to which optics are prealigned. The assembly works under the same ideas discussed earlier in this chapter as far as taking advantage of the tolerance to misalignment the electrical contacts of the package have, and the methods that were employed in the prealignment stage for the tilt of the VCSEL-MSM system, which involved tilting the package relative to a socket while the pins maintain electrical contact. Fine adjustment of the package in the z direction can be obtained relative to the top surface of the assembly, allowing the prealigned optics to be mechanically coupled, eliminating and external adjustment step in then z axis and adding to the modularity of the system and simplifying the assembly. Figure 5.6 shows how the assembly works and how alignment is achieved.

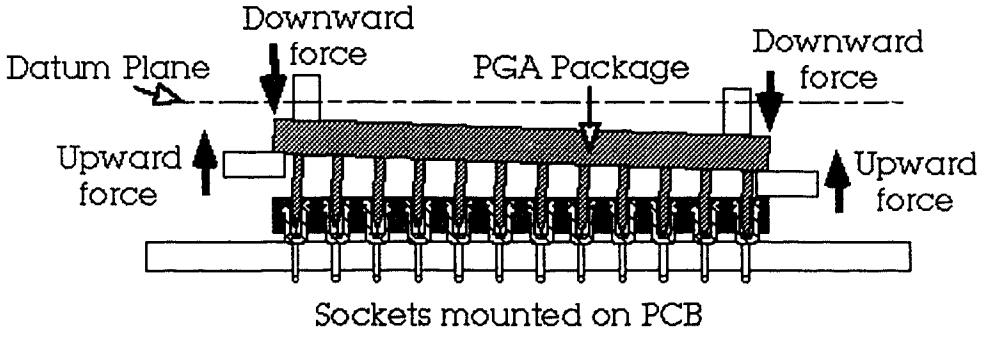


Figure 5.6 - Tilt and z assembly adjustment technique.

The positioning of the package is such that it contains no springs. Also, backlash is prevented by having the actuator screws pressing against one another at all times. Adjustment of one of the 4 corners of the package requires both actuators in each position to be adjusted simultaneously. To define the tilt of a plane, three of such positions are required, while in this assembly four were used. This was done in order to provide a symmetrical adjustment of the package, and to allow an easier quantification of the travel by virtue of this symmetry.

5.3.4 Tilt-z assembly design

Based on the drawing in figure 5.6, the optomechanical assembly to allow the adjustment of the two tilts and the translation in z was designed to be incorporated mechanically attached to the board. The package is moved within the assembly, and relative to it and the board, using eight screws from the top of the assembly (or datum plane). Four of these screws exerted a downward force on the package, while four screws 'pulled' a washer-like piece to provide the upward force on the bottom corners of the package. All screws acting together also locked the package in place, however, it was

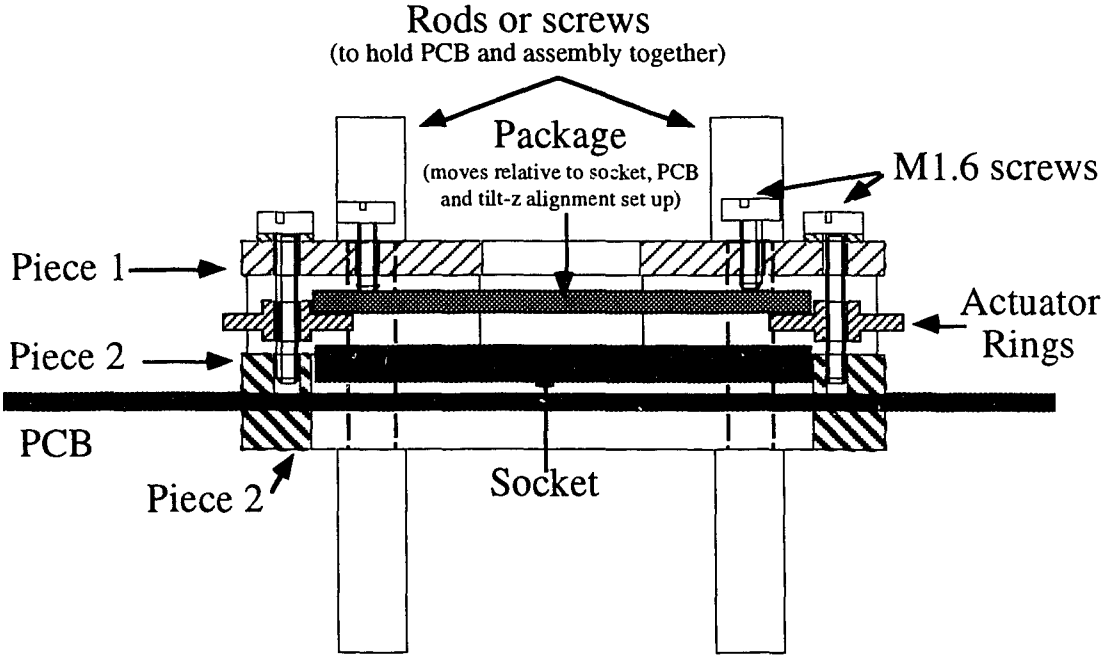


Figure 5.7 - Tilt-z setup assembly drawing.

seen that the action of the contacts in socket also fixed the position of the package, as it stayed in position after been adjusted without the need of this locking. Further and more in-depth assessment of this was not done. The assembly is shown in figure 5.7, while the technical drawings of the individual parts are shown in Appendix B at the end of this thesis. The tolerance on the components in the assembly was not tighter than 0.005" (127μm), however a high degree of flatness was required for the datum plane. The theoretical resolution of the assembly is given by the pitch of the screws used and the size of the package. Thus for 1/4 turn of M1.6 screws (350μm pitch), approximately 0.2 degrees can be obtained. The maximum tilt is limited by the distance the package can travel in z within the assembly and maintaining electrical contact with the socket at all pins. This is estimated to be 4.6 degrees in the diagonal of the package. These parameters are verified through the experimental procedures described in the following section.

5.4 Experimental setup

Two setups were used to test and characterize the assembly. The first was a retroreflection setup to assess the maximum tilt that could be achieved and to what resolution. The second was a setup to assess the integrability of the assembly to a system like that of the Phase II optical backplane demonstrator. These are described in this section, followed by the experimental results obtained for the characterization of the tilt-z assembly.

5.4.1 Range and resolution characterization

For the assessment of the tilt range and resolution of the assembly, a setup as that shown in figure 5.8 was used. A Helium Neon laser beam was aligned relative to two irises which acted as alignment apertures. The irises were aligned relative to each other and relative to a coupling piece to the assembly through Spindler & Hoyer optomechanics. The beam reflection was then seen at the first aperture, and the deflection angle could be calculated. Maximum tilts of ±3.5 degrees (with an experimental error of 4%) for tilt in the direction of the package diagonal were measured, and showed to be slightly larger than

the expected values from the design. Resolutions of 0.12 degrees (±0.06 degrees) were

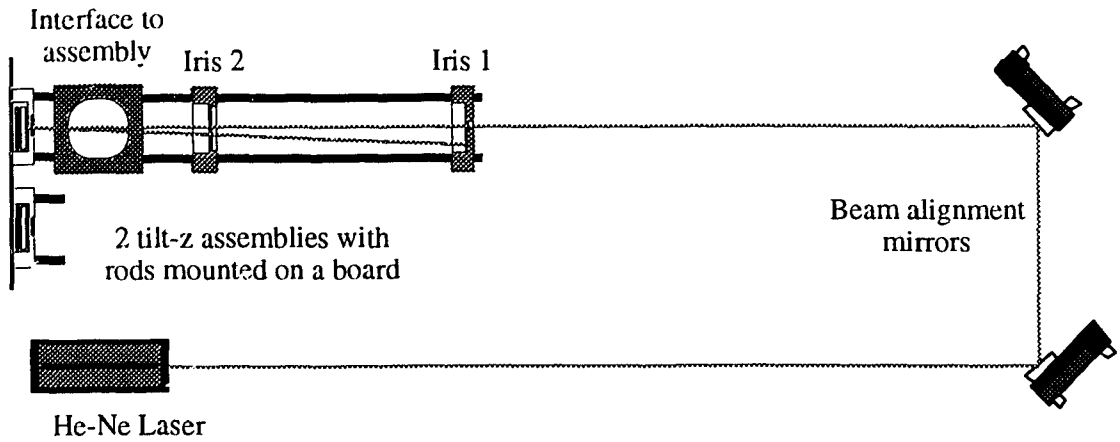


Figure 5.8 - Tilt range and resolution characterization setup.

seen for 1/4 turns of the screws in the assembly. These measurements were taken with a dummy packaged die and did not require prealignment of the die within the cavity. However, for the second setup, which will be described later, two device arrays are aligned relative to the package through the die to cavity technique described in the following section.

5.4.2 Die to package alignment

The alignment of the dies relative to the package to be used in the experiments was achieved through the use of spacers between the cavity sides and the die. This allowed a minimization of the rotation of the array of devices relative to the carrier or packages as one of the sides of the die was placed against the cavity walls. The spacers used are 50 Ohm chip resistors (Mini Systems Inc.) with mean side dimension of 1.31 mm and a standard deviation of 0.01 mm over 89 samples. These resistors were epoxied against one side of the cavity. The array of detectors was epoxied against it and against the top cavity side. This was done for two devices which are shown in figure 5.9. The positioning of the devices deviates form one another by approximately 10 μm or half a division in the 25 μm graticule. It is also interesting to note that the rotation of the dies relative to the cavity is too small to be quantified, however can be estimated, using the graticule, to be less than 0.2 degrees.

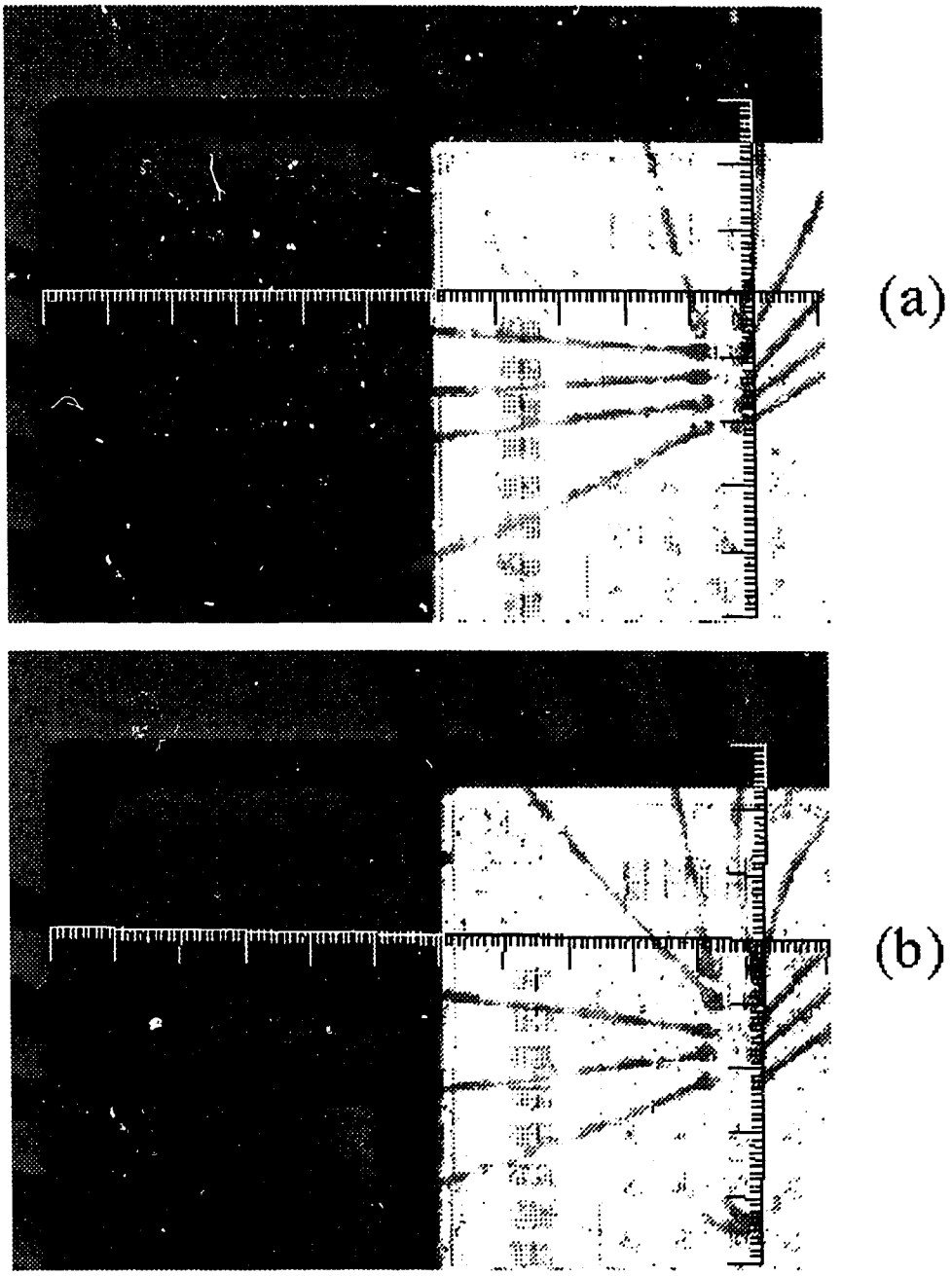


Figure 5.9 - Die to cavity positioning using spacers for two device arrays.

With the arrays packaged and the assembly ready to be tested for integrability, the optical system was designed and built and is discussed in the following section.

5.4.3 Optical System Considerations

The experimental setup used 850 nm light which was input into the system through an optical fiber and refocused onto the device plane by a 4f system with focal lengths of

40mm and 50mm[1] and 25mm and 50 mm[2] for the second set of measurements. The choice of such lenses was driven mainly by the optomechanics used to simulate an optical interconnect like that of the VCSEL/MSM system. The optomechanics used were based on Spindler & Hoyer components and allowed certain degree of flexibility in the test rig manipulation, limited however, by the compactness of the system. The *25-50 system* also introduced the use of Risley steerers to move the beam around to align the beam with each window in the experiments, which proved too difficult when this alignment was done by moving the assembly relative to the optical system. In addition an LED based illumination and imaging system was incorporated into the setup. The array of devices and the focused spot were imaged through a CCD and a 4f relay.

The 4f system used to relay the light input provided a magnification of the spot size of 1.25 for the *40-50 system* and 2 for the *25-50 system*, resulting in an increase in the spot size from 2.55 to 3.19μm and to 5.1μm respectively. In addition the system had an f number of approximately 3. The Raleigh range of the system was 24μm for the *40-50 system* and 61μm for the *25-50 system.*

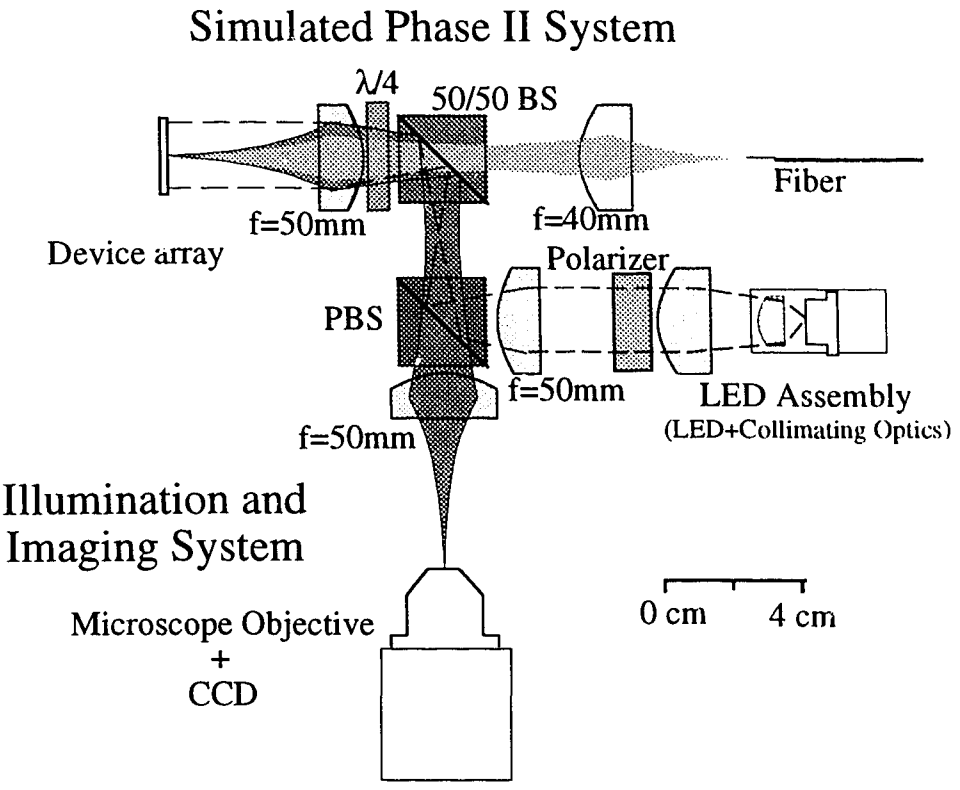
The screws used to manipulate the height and the tilt of the package were M1.6 with a thread pitch of 350μm, allowing 22 μm displacement in z for a $\pi/8$ turn. Given the spot sizes, 22μm misalignment in z represents an increase in the waist of the beam from 3.19 μm to 3.7 μm for the *40-50 system* and from 5.1 to 5.4μm for the *25-50 system.*

5.4.4 Experimental

The experiments performed, aimed at demonstrating the integrability of the assembly into a Phase II-like optical backplane demonstrator, were done for two dies, both prealigned to the same optical system. With the assembly decoupled from the optical system and without any prealignment in tilt or z, the maximum photocurrent at the detectors under a reverse bias of 2V was measured maximizing the light coupling by adjusting the die position within the assembly through an x-y-z stage. A barrel "termination" was then added to the optical system's optomechanical assembly which fixed the closest distance the tilt-z assembly could be positioned at. The assembly was then pressed

1. Setup 1, referred to as *40-50 system* and which is used for 2 dies/assemblies.
2. Setup 2, referred to as *25-50 system* and which is used with 1 die/assembly and Risley Steerers.

against this barrel and the datum plane of the tilt-z was butted against the barrel flat face.



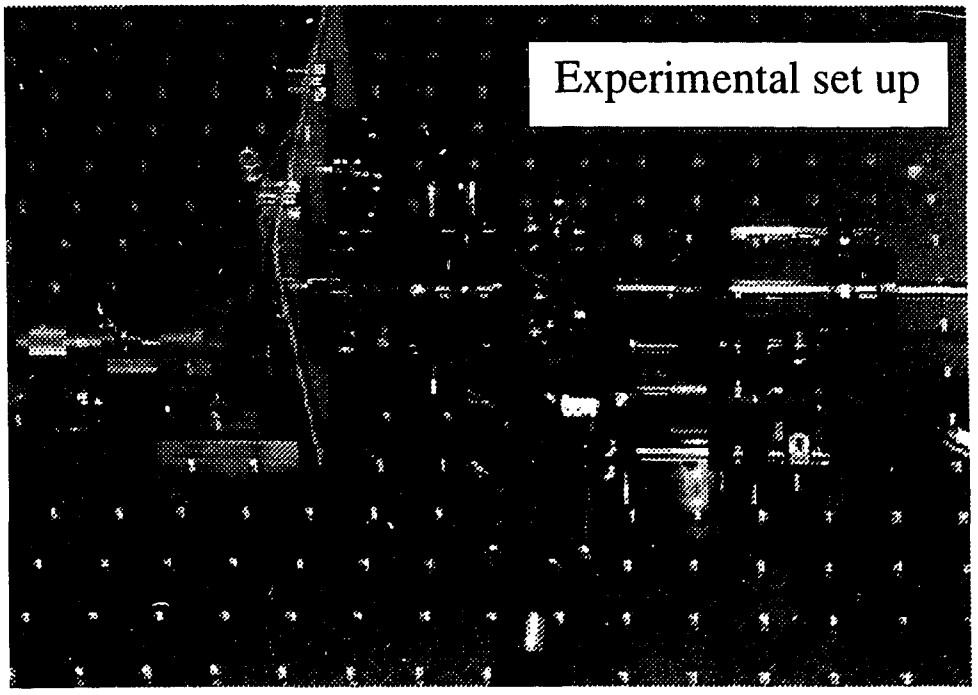


Figure 5.10 - Optical system used to simulate a VCSEL-MSM-like system to which the tilt-z assembly can be coupled to show integrability into the system.

Alignment of the die within the package was done through the assembly and with the assembly integrated into the system as described, the photocurrents for the detectors in the array were measured for the adjusted package position. The beam was aligned in each window through the positioner by only changing the x-y position of the setup, keeping the z direction defined by the assembly/barrel interface. This simulated the x-y positioning in the Phase II demonstrator by moving the board relative to the optical system in the same fashion as that shown in figure 5.5 earlier in this chapter. The experiments were repeated for the *25-50 system* in which Risley steerers were added. This was done because the friction between the assembly and the barrel resulted in hysteresis when the x-y direction was adjusted to align the beam to the windows in the array. Also, the fact that the position of the die was biased to one corner of the package cavity added difficulty in the x-y alignment, as the x-y travel range was limited by the actuator screws in the assembly. In some cases the fiber input had to be slightly moved to allow alignment of the beams on the windows. This might have resulted in beam clipping, and hence less power coupling, introducing a source of experimental error in the measurements of the *40-50 system.*

In the *25-50 system*, the steering was achieved through both a set of Risley's and the x-y adjustment capabilities of the x-y-z positioner. The results for the first set of experiments (*40-50 system*) are shown in table 5.1, where the percentage of the power coupled is also calculated. The defocus or misalignment in z is then obtained from these numbers for the various detectors and is shown in figure 5.11 where the theoretical or expected values are plotted along with the values obtained in the experiments. As can be

Table 5.1 - Percent coupling before and after correction

Array 1	I_{max} (μA)	I (μA)	%*	Array 2	I_{max} (μA)	I (μA)	%*
Det.5(100μm)	-	-	-	Det.5(100μm)	60.3	60.5	100(100)
Det.4 (50μm)	108.5	106.0	98 (100)	Det.4 (50μm)	59.5	56	94 (99)
Det.3 (25μm)	104.5	91.0	87 (90)	Det.3 (25μm)	48.0	43.5	90 (94.5)
Det.2 (15μm)	65.0	45.0	69 (71)	Det.2 (15μm)	38.0	30.0	79 (83)
Det.1 (5μm)	-	-	-	Det.1 (5μm)	23.0	15.0	65 (68)

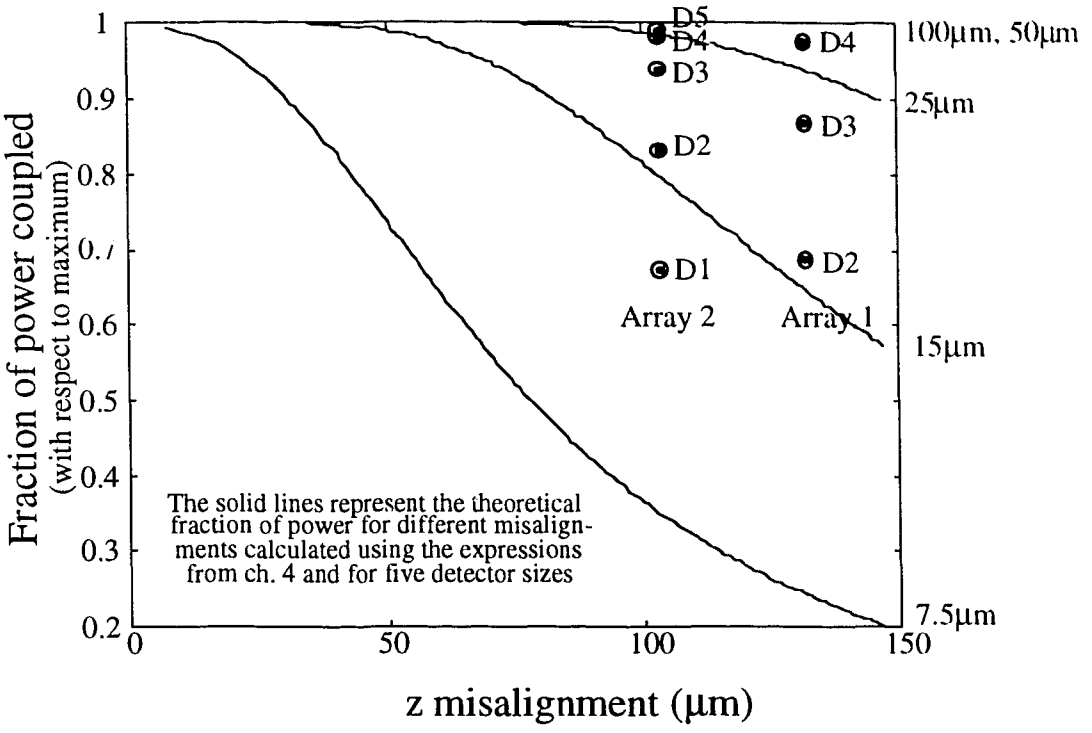


Figure 5.11 - Power coupling for Array 1 and Array 2 as a function of misalignment in z or defocus. Percentage values calculated with compensation for input power variation.

seen the alignment achieved through the assembly is on the order of 100 μm, however the results were strongly affected by the rough optical system (barrel) to assembly interface, which was not ideal. For this system, an identical setup to that of the Phase II optomechanics incorporating the tilt-z assembly would have been preferred which added a force between the barrel and the PCB interface optomechanics, however the system optomechanics were not available for experiments at the time of the characterization. Although the assembly was designed to fit the Phase II system, a different testing setup had to be designed and implemented.

The input power (at the fiber) showed the total power to decrease from 230 to 200 μW throughout the length of the measurements and was monitored only at the beginning and at the end. This constitutes a source of experimental error. Another source of error was that related to the reverse bias voltage of the detectors, which was seen to affect the photocurrent by 2μA for 100 mV over 2 V variation (5%) in voltage and affected the measured photocurrent as the bias was powered down and up every time the beam was moved to another device in the array.

Once the detector arrays in the 2 different assemblies were prealigned with respect to the same optical setup (in z and $tilt_x/tilt_y$), the focused spot in both array planes was observed through the imaging system, as these were interchanged in plug-in/plug-out manner. This showed the a detector array to optical system modular setup, which can be integrated into a Phase II VCSEL-MSM like system. The assembly is shown both by

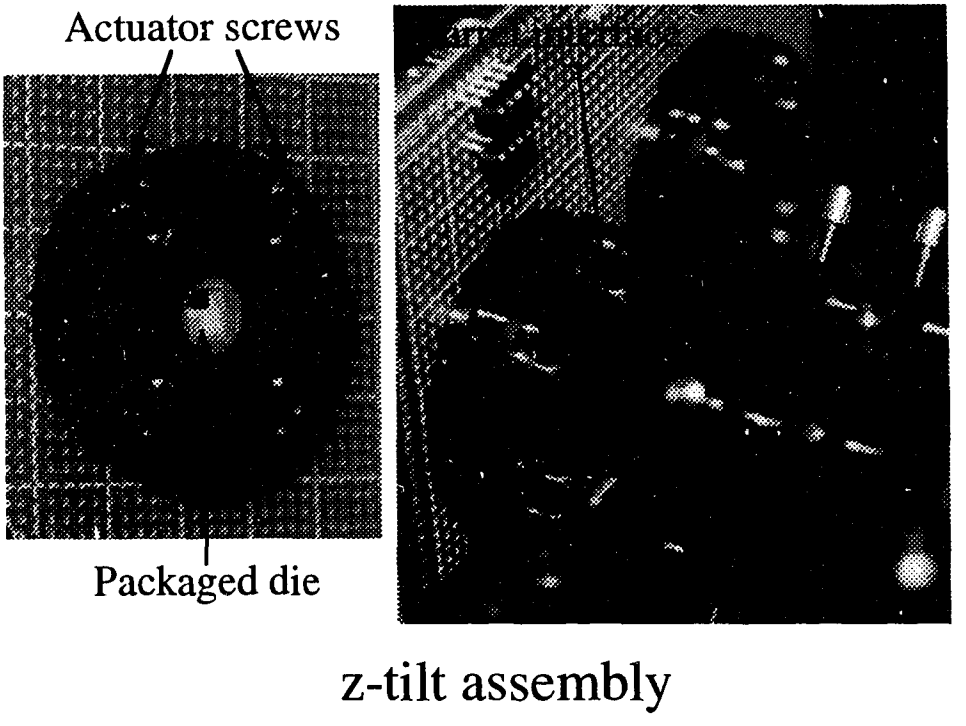


Figure 5.12 - Tilt-z assembly picture (left) and assembly coupled through a "barrel interface" to optical system.

itself and coupled to the optical system through a "barrel interface" in figure 5.12. The two arrays after alignment are shown in figure 5.13, where frame grabbed images of the arrays and spot are aligned simultaneously relative to the same optical system in z as seen through the imaging system.

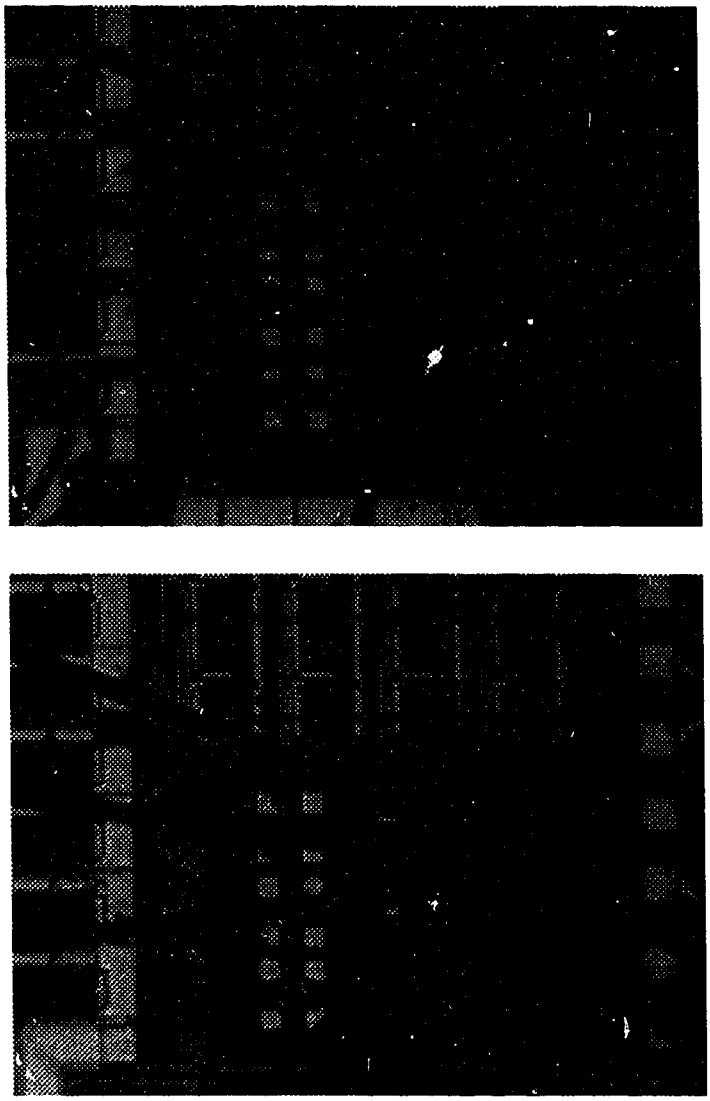


Figure 5.13 - Focused spots on two device arrays prealigned to the same optical setup.

The *25-50 system* experimental procedure was in principle the same as that of the *40-50 system*, however it differed through the fact that once the optical system was aligned, the only thing that changed was the position of the Risley steerers. A single device array was also used, which was epoxied and wirebonded at the center of the package cavity avoiding the travel in x-y problems experienced in the previous system. The voltage effect on the measured photocurrent was minimized by live biasing of the detectors as the beam was moved within the array.

The devices within the assembly where aligned with constant monitoring of the input optical power, which remained constant throughout the experiments, and through

iterative stages until the best possible result was obtained for the power coupling. These iterations are shown in Table 5.2 and Figure 5.14.

Table 5.2 - *25-50 system* experimental data.

	Max. Current	1st Pass [μA(%)]	2nd Pass [μA(%)]	3rd Pass [μA(%)]
Detector 5 (100μm)	44.5μA	44.3 (99.55)	43.5 (97.75)	43.9 (97.0)
Detector 4 (50μm)	42.5μA	32.0 (75.30)	40.2 (94.60)	41.0 (96.50)
Detector 3 (25μm)	33.7μA	-	33.0 (97.90)	35.1 (100)
Detector 2 (15μm)	22.0μA	-	8.5 (38.60)	18.0 (81.80)

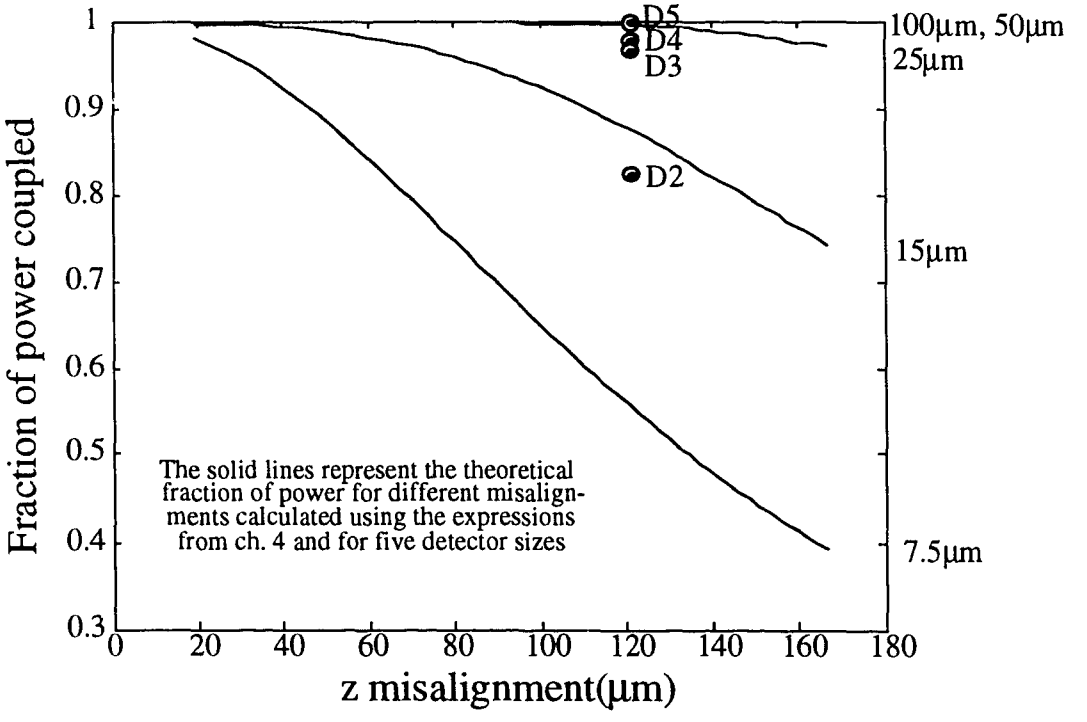


Figure 5.14 - 25-50 system theoretical plots of relative power coupling showing the power coupling for the four detectors in the prealigned array.

The adjustment was done by removing the assembly from its position against the optical system, thus the plug in criteria was verified, as the powers were reproducible. It can be seen that the power on the larger detectors for the third pass, are smaller than those of the second pass. This could be due to a tilt introduced when maximizing the power coupling for D2, or simply due to errors in the x-y alignment of the spot relative to the

window. The latter seems to be a better explanation as the sensitivity to tilt is not as high as the sensitivity to x-y misalignment.

5.5 Conclusions and discussion

This chapter described the multiple optomechanical/packaging approaches devised to cope with the alignment problem. The transition from multiple degree of freedom systems to more rigid systems, with certain degrees of freedom defined and constrained by the mechanical structure surrounding the optical elements in the system was shown. It was also seen that in order to achieve a board to board interconnect, where the optoelectronic device arrays are packaged up to a switching node level of packaging, the degrees of freedom in the device array were needed to be manipulated and hence unconstrained. Manipulation of these degrees of freedom was seen to be achieved both through optical and optomechanical/packaging techniques.

The concept of a mechanical decoupling of the photonic layer from the electronic layer in the system, or the backplane and the actual boards was introduced and illustrated through a system which, with the optics and optoelectronics prealigned, takes advantage of the tolerance to misalignment existing between package and board. These ideas are extended in a total decoupling of the boards containing the switching nodes, and that require to be inserted and extracted and the boards which are the packaging for the optoelectronic device arrays. This motherboard/daughterboard decoupling is achieved by connecting them through a flexible high speed connector. This approach showed a fundamental departure from more traditional approaches, namely the AT&T baseplate approach, and showed the integrability of the optomechanics into a standard electrical backplane chassis. The custom optomechanics developed for this system were also described. Complete six degree of freedom alignability was seen to be possible if prealignment steps were used for two tilts. A positioning system, covering the degrees of freedom not covered by the optomechanics of the Phase II demonstrator, which allowed the prealignment of device arrays relative to a datum plane which can define the alignment of the optical system was developed and described. The merit of the setup is not as much on its alignment capabilities, but on the pre-alignment which allows a Phase II-like system to come together in a plug-in manner, without requiring alignment in the z direction and tilts

about the transverse directions to the optical axis. The resolution of the alignment that can be achieved through the system was seen to be limited by the screws used as actuators, however, and as was seen in the Phase II optomechanics, adjustments smaller than 10μm can be achieved if opposing actuators are moved simultaneously. The alignability of two device arrays to the same optical system by coupling the optical system to the assembly at the datum plane was shown. This allows the system to have multiple dies on the same board for a fixed optical system, aligned in z to a given datum plane common to all optical trains that link the multiple device arrays. In addition, all tilts can be taken care of as well by aligning relative to the datum plane with the z-tilt assembly. If alignment in x-y is achieved through techniques such as those described earlier in this chapter (Risleys, die to carrier prealignment and Phase II optomechanics-like alignment techniques) and in chapter 4 (carrier to board and smart pixel design parameter manipulation), the use of multiple dies in the same board can be possible.

Optomechanical techniques have shown a steady drift toward alignment without springlike components. Prealignment, and alignment through actuators that act against one another are techniques that were discussed in this chapter and that deal with the problems often encountered in the alignment and stability of optical interconnects. In addition to reducing drift, these techniques can provide locking mechanics for preserving the alignment of components, in this case the optoelectronic device arrays.

The alignment of the arrays was seen to be, in general, simplified if prealignment steps are introduced. This will lead to systems that require alignment mechanisms with less required travel, and hence more compact, and with inherent gains in their resolution. Such prealignment techniques, can also eliminate altogether the need of optomechanical assemblies for further alignment. This is most likely to be the case for the tilts, z axis, and rotation of the arrays, while x-y might still require alignment through optical elements such as Risley Steerers.

Systems which apply techniques such as those described in section 5.2.2, and require operation under harsh environmental conditions will benefit from the introduction of less rigid packaging elements, such as flexible boards, packages with (Tape Automated Bonding) TAB techniques, or flexible leads on the electrical interface, and rigid optomechanics with prealigned components on the optical interface. Furthermore, the alignment

of multiple dies relative to an optical system could be possible through these techniques, and will require further investigation.

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Chapter 6

Conclusions and future work

6.1 Thesis overview

This thesis has shown the complexity of the packaging of two dimensional arrays of optoelectronic devices. The focus of the investigations throughout this thesis was on the application of existing microelectronic packaging technologies to the packaging of smart pixel arrays for optical backplane applications. The main question that was addressed is that related to whether it makes sense to apply existing packaging technologies, or not. If so, the application of existing packaging technologies would have to be achieved by modifying them, either through external structures, such as optomechanical techniques, or by building in some tolerance in the smart pixel arrays by varying their design parameters. In contrast to this, the other option is to take a custom design approach, which would be application driven. This alternative could potentially develop into an area of optoelectronics that would develop the technological platform for the packaging of optoelectronic device arrays. However, it would require some standardization of the optoelectronic device array configuration, in addition to a compilation and understanding of the issues that need to be addressed in the development of such packaging technologies, particularly of those issues which are common ground to multiple photonic applications. This thesis addressed the required areas of development of this platform indirectly by aiming at the application of standard packaging techniques, and provided empirical formulations for thermal management, I/O and bandwidth, and alignability requirements. These will be briefly outlined in the following three sections, in conjunction with the results obtained throughout this thesis.

6.1.1 Packaging thermal management constraints

Thermal dissipation issues were seen to affect the packaging of optoelectronic device arrays by a different set of constraints as those from microelectronic (namely VLSI) packaging. The tight temperature control required for adequate optoelectronic device performance was seen to be one of them. In addition to the required temperature stability, the removal of heat was a problem in itself as smart pixels, being an integrated combination of technologies, showed to have high heat dissipations when implemented in

arrays. This arrayed structure results in nearest neighbour thermal crosstalk, and is very difficult to quantify. Adding to these is the absence of one of the possible paths for the removal of heat, and the most direct one, as the dies are required to be accessed optically.

An analysis of the heat removal capabilities of existing packaging techniques was presented. These were applied to a smart pixel array model in order to assess the on-die temperature as a function of smart pixel array parameters. This resulted in a design space for optoelectronic device window size, smart pixel density and array size, constrained by the heat removal capabilities of chip carriers. Other parameters which are more specific to the technology employed, such as operating speed, were included in the analysis to determine the properties of a given smart pixel array technology. The combination of all these constraints was seen to ultimately affect the optical channel partitioning into multiple dies, as the smart pixel array sizes that can be supported diminish in size.

The consequences of such partitioning is evident in two areas which require careful attention. The first is the net optical channel density that can be achieved after the packaging is included. The second is the problem of system alignment, which gets complicated as soon as more than one array needs to be aligned. The addition of optomechanical resources to achieve alignment as a result of this contributes to the first problem, as the net optical channel density gets reduced even further.

The variation of the packaging heat removal properties, such as the reduction of package thermal resistance and the heat sink temperature, could potentially allow larger arrays, and as a result better net optical channel density, however the methods of varying such parameters results in an increase in the area occupied by the packaging, affecting again the net optical channel density. Such methods are, for instance, the addition of heat sinks, or the addition of cooling techniques such as Peltier coolers, or water cooling techniques. Another way of manipulating the packaging heat removal capabilities is through the use of custom packaging techniques which has more potential to increase the net optical channel density and result in a leaner system. This can be done through the use of high thermal conductivity substrate and the design of a more compact packaging set-up by virtue of the fact that it is driven only by the system requirements.

For either approach, the system designer must work under the assumption that optomechanical techniques are going to be used, and will occupy the least amount or

space possible. Under this assumption, the net optical channel density will be ultimately influenced by the packaging technique employed. For a standard microelectronic packaging approach it is crucial to use a packaging technique that will minimize the area of its footprint on a board and maximize the electrical I/O capabilities for the smart pixel array. This was part of the investigations of chapter three which is discussed in the following section.

6.1.2 Packaging characteristics, connectivity and bandwidth

The constraints imposed by different VLSI packaging techniques from a heat management point of view resulted, as a consequence, in die partitioning. In addition, the ranges of array sizes that could be achieved suggested that packages with relatively large electrical I/O would be required if a one to one mapping of the electrical I/O to the optical I/O were used. Although this application is not realistic, the I/O requirement could ultimately be the limiting factor in smart pixel array design parameters and was seen to require assessment for optical backplane applications. For this, a general approach was taken in the analysis of the required package I/O to support a generic smart pixel array. Such a smart pixel array would be represented by parameters inherent to the architecture it implemented, which would allow the application of more specific architectural considerations at a later stage. In doing so, a set of relations between the smart pixel array I/O and the physical parameters that are constrained by the packaging was developed.

A review of the figures of merit of packages, as well as their properties was also done. Among these were the data rates and number of channels that can be supported, the size of the carriers as a function of their I/O, cavity size and bondability issues.

By combining the two results, the design of smart pixel arrays can be constrained by the packaging issues related to connectivity, as the smart pixel architectural characteristics relevant to or affected by the packaging were related to requirements in the electrical I/O by means of simple connectivity parameters. It was seen in this chapter, that the application specific nature of the smart pixel array's architecture does not permit the acquirement of design space constraints that are not application driven. A specific example, based upon the requirements of optical backplane applications, showed that standard packaging techniques could be used to package smart pixels, as the electrical I/O

aggregate capacity is at least one order of magnitude smaller than the optical channel aggregate capacity.

The analysis of chapter 4 provided a set of expressions that address the issues related to the connection the optical I/O in the backplane to the electrical interface with the boards in the system. These expressions can be used as a tool to assess the applicability of standard microelectronics packaging techniques, or custom packaging techniques, to photonic applications where smart pixel arrays are used. Furthermore, the physical realizability of the system can be assessed as a consequence of this analysis and from a design space/packaging point of view.

6.1.3 Alignment constraints

The alignment issues in the integration of optoelectronic device arrays in an optical backplane were also studied. The misalignment sensitivity of SEL based systems was compared to that of modulator based systems for a 4f telecentric optical system, and lead to a design space formulation for the smart pixel array. This formulation was obtained in terms of the tolerance to misalignment of the optical windows in the array, and it was constrained by the alignment accuracy that can be achieved through standard packaging techniques. This alignment accuracy was seen to vary for different packaging techniques, and showed to be promising for techniques which employ self-alignment. The analysis also showed that the variation of the smart pixel array parameters to enhance the tolerance to misalignment will not be able to solve the alignment problem on its own.

It becomes evident that the packaging alone in conjunction with smart pixel design parameter manipulation will require the addition of hardware, particularly for the case of alignment. Techniques for complementing the packaging and allowing its use in optical backplane demonstrators, were proposed, designed and implemented in Chapter 5, both through the discussion of alignment and optomechanical/packaging techniques, the implementation of the Phase II optical backplane demonstrator optomechanics and the Phase II optomechanics upgrade assembly. These are discussed briefly in the following section.

6.1.4 Alignment techniques

As part of the evolution of optomechanical approaches, the introduction of rigid systems (or systems with constrained degrees of freedom), and the removal of flexure or spring-like components in optomechanical systems, resulted in the techniques that are

currently being used and that are leading to the implementation of very compact and solid systems. The departure from traditional approaches was discussed through a packaging (electrical and mechanical) proposal, and through the mapping of the concepts of such proposal to an optical backplane demonstrator. This demonstrator, the Phase II VSCEL-MSM Optical backplane demonstrator was implemented in a VME chassis, and introduced optomechanical approaches which resulted in a very robust system from an alignment point of view. The packaging of the device arrays in such system used standard microelectronic packaging techniques and utilized some of their features to achieve system alignment.

The deficiencies in the system were strengthened through the design of an optomechanical assembly that takes advantage of the packaging techniques employed to increase alignment capabilities as well as reducing the alignment procedure execution time. This allows the use of prealignment techniques for device arrays and show how the system can be designed in a such a modular way as to essentially plug them in to the optics in the system. This point is discussed in more detail in the following section, as it leads into the introduction of modular approaches to optomechanics/packaging of smart pixel arrays.

6.2 Discussion

The analysis of the packaging issues in the implementation of optical backplane demonstrators led to a thorough understanding of the microelectronics packaging technology. The way in which the use of this technology in optical backplane systems affects them was assessed from various perspectives and resulted not only in the identification of the areas in which the packaging needs to be studied further, but also in an assessment of the requirements of optical backplanes, and in a more general context, photonic interconnects.

Although the focus was on the application of standard microelectronics packaging techniques, particularly on the use of single chip carriers, the work in this thesis can be extended to the use of a more general packaging scheme. This is possible because the analysis was based on the issues that need consideration in the various optical interconnect applications. What was clearly seen is that microelectronic packaging technologies could be used from most points of view, provided the smart pixel arrays are designed following

certain guidelines, as dictated by the design space analyzed in this thesis. In a similar way, the implementation of systems which employ any packaging scheme, whether adapted or custom made, will require to address the issues discussed and analyzed throughout this thesis. The need for a standard set of constraints which, although not satisfying every system design, covers the common ground most systems have, is something that needs to be ultimately satisfied. This is, at present, the focus of study of many research groups in the photonics community.

An important point to make is that related to the fact that the constraints imposed by the various areas of study in the packaging problem, are not necessarily coupled in a way in which one benefits from the other. In most cases, adding or reducing hardware, or modifying the smart pixel array to alleviate some of the constraints in certain areas, will result in the complication of others. Thus, a compromise between the areas that need to be dealt with, in the packaging, must be achieved to maintain the delicate balance between them which results in no system performance degradation. Among these is the addition of optomechanics which has as a result a net connection density decrease, and possibly a bulkier system, which limits accessibility to the optics and complicates system integration. In a similar way, heat sinking the device arrays results in addition of hardware that affects mainly the targeted system design parameters, such as board separation, optical channel density, and the alignment capabilities of the system. The latter is a result of the reduction of physical space where the needed optomechanics can be implemented in. The heat dissipation problem can be solved partially by partitioning the system I/O, which was seen to complicate the alignment of the device arrays, and also was seen to reduce the net optical I/O density, as each individual package will occupy a portion of the physical space of the system, which would otherwise be used for optical channels.

This last point leads to two important considerations which are briefly discussed in the following two sections: scalability and trade-offs.

6.2.1 Scalability considerations

Optomechanical systems for alignment as well as packages will limit the scalability of systems, specially if the arrays are already limited by design space constraints. Ideally, the package should occupy areas on the board slightly larger than the smart pixel array, while providing the desired thermal management, connectivity and

alignability capabilities, in order to point to system scalability. Unfortunately, this is not the case for single chip carriers. The removal of a level of packaging then can be considered as an alternative in the die-on-module configuration. This, however, needs to be investigated in more depth as alignment issues, although alleviated, can be somewhat complicated by the difficulties in the techniques used in the hardware implementation. In a similar way, the heat dissipation capabilities of the module would have to be assessed, as die densities could potentially become very high, specially in view the interconnection densities that can be obtained with state-of-the-art multi-chip modules.

The breakthroughs in the technology dependence of thermal management imposed constraints will allow the scalability arguments of optical backplane systems to be more convincing, as the smart pixel array technologies will mature to provide cooler chips that can run faster, or have heat dissipations independent of switching speed.

6.2.2 Packaging trade-offs

Another issue which is seen throughout this thesis, is that related to the allocation of resources to deal with the issues in the packaging. The final design parameters, and hence packaging constraints, ultimately depend on the target system specifications, and system design will have to involve a thorough analysis of the trade-offs between different approaches to solving the packaging problem. The tools in this thesis can be used for this purpose. In addition to trade-offs, and possibly more important than these, are the use of the tools in this thesis to identify the resources that can be shared by one or more areas of the packaging to alleviate the constraints they impose on the system implementation. For instance, optomechanical hardware can be part of the heat sinking for the optoelectronic device arrays. This can be combined with prealigned optoelectronics to the optics though a heat sink/optomechanical system, which would partially solve the I/O and alignment problem.

6.2.3 Future work

The use of prealignment in optomechanical/packaging was seen to offer multiple advantages. Among such, are the system compactness that can be achieved, and the ease in which system integration can be attained. These can be thought of as analogous to the optomechanical solutions to fiber based transmission systems, where the prealignment permits the launching or collecting of light to be done through a plug-in connector. This

area needs to be studied further and shows to have a great potential in providing some of solutions to the alignment issues and system integration issues which the development of optical backplane systems is faced with.

6.3 Conclusions

Optical backplanes will offer very high channel densities and bandwidths, and also the ability to reconfigure the interconnects in the backplane. Even with current optomechanical systems and packaging, the net optical densities that can be achieved provide connectivities that are head to head to those provided by electrical backplanes. What can be done in terms of aggregate bandwidth was shown to be limited by the packaging of smart pixel arrays. The two possible paths in the solution of the packaging issues were discussed: custom technologies and standard technologies.

The strengths of using a technology that exists and is available, not only represents the unique ability to provide a smooth transition between existing industrial approaches in the packaging field to a new field altogether: the packaging of optoelectronics, but also, provide the ability to balance, and favourably bias the cost/performance ratio of photonic systems for optical backplane applications against those of electrical backplanes. Multilayer technology boards and modules are currently available, as well as many other technologies that can potentially develop the electrical backplane area to accommodate the emerging systems, however their cost/performance ratio is reaching a point where their use will cease to be advantageous. On the other hand, photonic systems offer great potential, however they are a field in its infancy, and cannot justify their use from an economic point of view yet. The development of short-term technologies, as those used in electrical backplanes, can represent ill-fate for the development of photonic system applications if a whole new infrastructure to manufacture them is seen to be required. The availability of inexpensive optics, and the applicability of existing packaging technologies and infrastructure are the points that can favour, and expedite the development of optical backplane systems.

It is evident that optoelectronic device array packaging is a new packaging area being born. The ease of its growth will be determined by whether it is the offspring from the microelectronic packaging area and the photonic systems field, or simply from the

requirements of this field. Regardless of which path this growth takes place in, the packaging issues related to heat management, connectivity and bandwidth, and alignment will have to be assigned a key role in the system design process.

Appendix A

Solution of the heat dissipation boundary value problem

The heat equation in steady state is

$$\nabla^2 T = 0 \tag{A.1}$$

The boundary conditions are given by

$$\left.\frac{\partial T}{\partial x}\right|_{x=\pm\frac{L}{2}} = 0 \tag{A.2}$$

$$\left.\frac{\partial T}{\partial y}\right|_{y=\pm\frac{L}{2}} = 0 \tag{A.3}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0} = -\frac{\dot{Q}(x,y)}{L^2 K} \tag{A.4}$$

$$T(x,y,z)|_{z=t} = Ts + T_p \tag{A.5}$$

where T_p is the temperature drop across the package and given by the average power at the top of the die multiplied by the package thermal resistance. The function $\dot{Q}(x,y)/L^2$ is given by

$$\frac{\dot{Q}(x,y)}{L^2} = (C_1 - C_2) f(x,y) + C_2 \tag{A.6}$$

where C_1 and C_2 are given by the power dissipation densities at the optical windows and at the electronics respectively and f(x,y) is given by

$$f(x,y) = \left(d^2 + \sum_{m=1}^{\infty} 2d^2 \cos m\pi \frac{\sin \pi md}{\pi m} \cos m\sqrt{D}x\right)\left(d^2 + \sum_{n=1}^{\infty} 2d^2 \cos n\pi \frac{\sin \pi nd}{\pi n} \cos n\sqrt{D}y\right) \tag{A.7}$$

Expressing equation (A.6) in terms of the optoelectronic heat dissipation density Q_O and the electronic heat dissipation density Q_E we get

$$\frac{\dot{Q}(x,y)}{L^2} = Q_O\left[\frac{Q_E}{Q_O} + \left(1 - \frac{Q_E}{Q_O}\right) f(x,y)\right] \tag{A.8}$$

The solution of the BVP is obtained subdividing the problem into two subproblems, each solvable using Fourier's rule. The solution to the problem is found from the boundary conditions and is of the form

$$T(x, y, z) = A(z-t) + \sum_{n=1}^{\infty} B_n \cos\frac{2\pi n y}{d_2} h_n(z) + \sum_{m=1}^{\infty} B'_m \cos\frac{2\pi m x}{d_2} h_m(z) + \sum_{n=1}^{\infty}\sum_{m=1}^{\infty} C_{n,m} \cos\frac{2\pi m x}{d_2} \cos\frac{2\pi n y}{d_2} h_{m,n}(z) \tag{A.9}$$

where d_2 is the period of the array and

$$h_{m,n}(z) = e^{-\left(\frac{2\pi}{L}\right)^2 (m^2+n^2) z} - e^{\left(\frac{2\pi}{L}\right)^2 (m^2+n^2)(z-t)} \tag{A.10}$$

for the corresponding values of m and n.

The values of A, B'_m, B_n, and $C_{m,n}$ are obtained by matching substituting equation (A.9) and equations (A.7) and (A.8) in the boundary condition from equation (A.4). These are given as:

$$A = -\frac{Q_O}{K}\left[\frac{Q_E}{Q_O} + \left(1 - \frac{Q_E}{Q_O}\right) d^2\right] \tag{A.11}$$

$$B_n = \frac{Q_O}{K}\left(1 - \frac{Q_E}{Q_O}\right) \frac{2d^2 \operatorname{sinc}(\pi n d)\cos(n\pi)}{\left(\frac{2\pi n}{L}\right)^2 \left(1 + e^{-\left(\frac{2\pi n}{L}\right)^2 2t}\right)} \tag{A.12}$$

$$B'_m = \frac{\frac{Q_O}{K}\left(1 - \frac{Q_E}{Q_O}\right) 2d^2 \operatorname{sinc}(\pi m d)\cos(m\pi)}{\left(\frac{2\pi m}{L}\right)^2 \left(1 + e^{-\left(\frac{2\pi m}{L}\right)^2 2t}\right)} \tag{A.13}$$

$$C_{n,m} = \frac{\frac{Q_O}{K}\left(1 - \frac{Q_E}{Q_O}\right) 4d^2 \operatorname{sinc}(\pi n d)\operatorname{sinc}(\pi m d)\cos(n\pi)\cos(m\pi)}{\left(1 + e^{-\left(\frac{2\pi}{L}\right)^2 (m^2+n^2) 2t}\right)\left(\frac{2\pi}{L}\right)^2 (m^2+n^2)} \tag{A.14}$$

With expressions (A.9) to (A.14), the temperature in any point on the die can be calculated for various values of L, d_2, K, R_p, T_s, and $\dot{Q}$, which depends on the value of d, the duty cycle for the array, and the values of Q_O and Q_E.

Appendix B

Tilt-z optomechanical assembly drawings

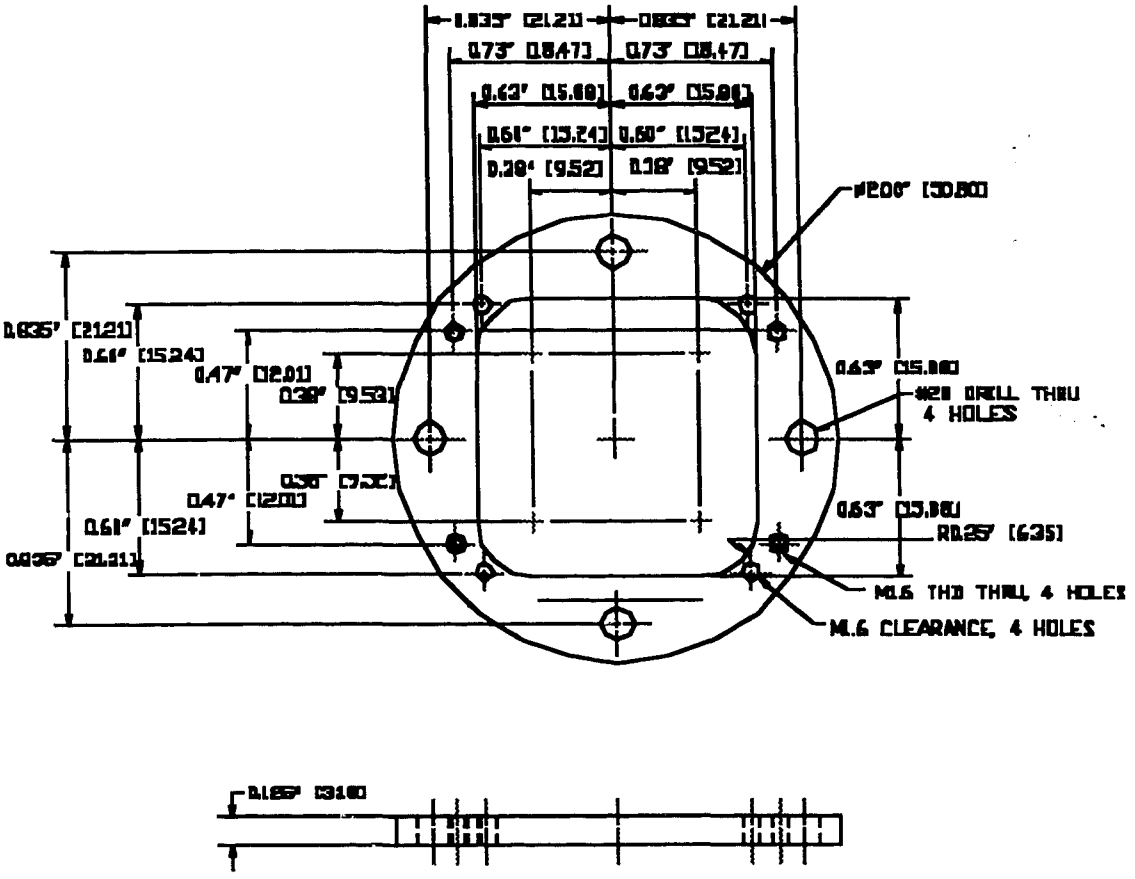

Figure B.1 - Ring piece used in the VCSEL-MSM system used for sandwiching the board for rigidity, and for guiding and locating the multiple actuator screws in the assembly.

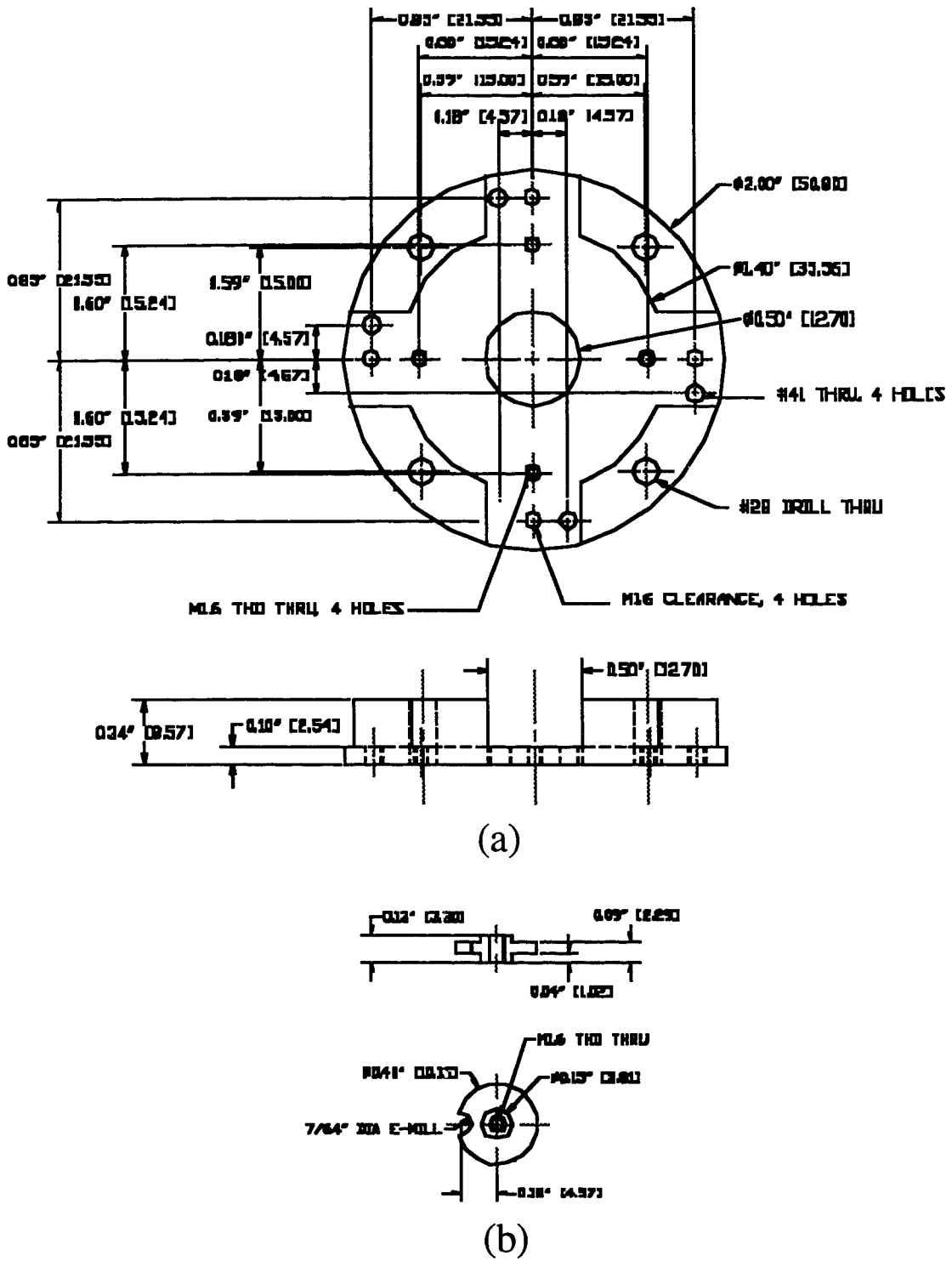

Figure B.2 - (a) Top plate encasing the package with threaded holes for the actuator screws from the top surface, and (b) washer-like rings to provide the upward motion of the package in conjunction with actuator crews located by the through holes on the piece shown in (a).

Terminology

A_1	Optical window area.
A_2	Logic area per smart pixel cell.
c	Package cavity size.
χ	Wirebond length.
d	Duty cycle or ratio of window side to smart pixel cell side.
d_{bp}	Bondpad dimension along nearest die side edge.
D	Smart pixel array density.
d_1	Optical Window side dimension.
d_2	Smart pixel cell side dimension.
$\Delta x, \Delta y$	Misalignment in the x and y coordinates.
$\Delta x_e, \Delta y_e$	Misalignment in the x and y coordinates for system comparison.
$\Delta x_r, \Delta y_r$	Misalignment in the x and y coordinates due to rotation.
$\Delta x_T, \Delta y_T$	Misalignment in the x and y coordinates due to translation alone.
Δz	Misalignment in the z coordinate.
Δz_e	Misalignment in the z coordinate for system comparison.
f	Frequency of operation.
F_o	Optoelectronic power dissipation density.
F_e	Electronic power dissipation density.
g	Package I/O per control or signal line to include ground line interleaving.
k'	Total number of bond fingers in package per unit distance in cavity side.
K	Thermal conductivity.
L	Smart pixel array physical size.
L'	Smart pixel array die size (which is equal to $L+\Delta L$).
λ	Light wavelength.
M	Smart pixel array number.
m	Fraction of I/O used by the switching node relative to backplane I/O.
N	Square root of the array size: Defines an NxN array of smart pixels.
N_p	Package I/O.
P	Optical power coupled under misalignment conditions.
P_{max}	Optical power coupled on perfectly aligned window.
r	Signal lines per control line per channel.
R_p	Package thermal resistance.
$\Re$	Responsivity of optoelectronic devices.
t	Die thickness.

T_s	Heat sink temperature.
w	Beam waist of a Gaussian beam.
w_o	Gaussian beam spot size.
x	Number of transistors per smart pixel
x_o, y_o	Initial or reference position in x and y (before misalignment).