Voltage Balancing of DC Capacitors in Chain-Link STATCOMs

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ABSTRACT

Modular Multilevel Converters (MMC) have become an interesting alternative to other converter topologies for Static synchronous Compensator (STATCOM) applications due to the modularity of their design and to their increased effective switching frequency which reduces the harmonics on the AC side. The drawback is that these converters have a large number of DC capacitors whose voltages have to be controlled independently. This becomes particularly important when the converter is required to operate during unbalanced conditions. The purpose of this thesis is therefore to define the problem of DC capacitor voltage balancing in MMC based STATCOMs, and to solve this problem for four different STATCOM topologies. A comparison of the advantages and disadvantages of each converter topology is then performed, and the proposed control schemes are implemented and tested using *Matlab/Simulink*.

ABRÉGÉ

Les convertisseurs modulaires multiniveaux (MMC - de l'anglais : Modular Multilevel Converter) deviennent une alternative intéressante aux topologies de convertisseurs conventionnelles pour des applications de compensateurs synchrones statiques (STATCOM - de l'anglais : Static Synchronous Compensator) grâce, entre autres, à leur conception modulaire ainsi qu'à leur fréquence effective de commutation élevée qui réduit les harmoniques générées. L'inconvénient des convertisseurs à topologie MMC est qu'ils comportent un grand nombre de condensateurs CC dont les tensions doivent être contrôlées de façon indépendante. Ceci devient particulièrement important lorsque ces convertisseurs doivent opérer dans des conditions débalancées. L'objectif de cette thèse est donc de comprendre le problème qu'est le débalancement des tensions CC dans les STATCOM de type MMC et de résoudre ce problème pour quatre topologies différentes. Une comparaison des avantages et des inconvénients de chaque topologie de convertisseur sera faite, et les algorithmes de contrôle dévelopés seront réalisés et testés à l'aide de *Matlab/Simulink*.

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LIST OF ABBREVIATIONS

AC: Alternating Current

DC: Direct Current

FACTS: Flexible Alternating Current Transmission Systems

HVDC: High Voltage Direct Current

IGBT: Integrated Gate Bipolar Transistor

KCL: Kirchhoff's Current Law

KVL: Kirchhoff's Voltage Law

MMC: Modular Multilevel Converter

PI: Proportional-Integral

PLL: Phase Locked Loop

PWM: Pulse Width Modulation

SPWM: Sinusoidal Pulse Width Modulation

STATCOM: Static Synchronous Compensator

SVC: Static var Compensator

TCSC: Thyristor Controlled Series Capacitor

VSC: Voltage Source Converter

CHAPTER 1
Introduction

With the ever increasing need for energy, many power transmission networks are reaching their limits. Building new transmission lines could possibly alleviate this problem, but the associated cost is extremely high, and the level of urbanization in many regions often makes this impossible. One possible solution is to optimize existing networks.

Given that networks need a stability margin in order to cope with transient events, the power transmission capabilities cannot be increased up to the thermal limits of lines and transformers. However, if the size and severity of these transient events can be reduced, the necessary margin can also be reduced, and more transmission capability can be obtained from the same network.

Several devices can be used in order to improve network transient stabiliy. One such device is the Static Synchronous Compensator or STATCOM as it will be referred to from here on. In addition to improving network transient stability, STATCOMs can also be used for voltage support and to improve power quality in many industrial processes. Utilities impose strict power quality requirements on industries, and the costs associated with the penalties for not fulfilling these requirements are quite high. Therefore, STATCOMs are often a worthwhile investment for large industrial customers.

For these reasons, much research in the field of STATCOM technologies has occured in the last decades, and the arrival of new converter topologies has generated new challenges and created the need for more sophisticated control strategies. One of these innovations has been the advent of modular multilevel converters (MMC). MMC based topologies have many advantages over other converter topologies, namely the modularity of the design, but also the increased effective switching frequency which reduces the harmonics on the AC side. However, this modularity comes at a cost: The increased complexity of the system requires more sophisticated controls.

One of the main differences with MMC based converters is that they are composed of many modules or cells which each have a DC capacitor. This means that several DC voltages need to be controlled. For a STATCOM application under normal conditions with balanced phase voltages and currents, the converter provides only reactive power. However, in unbalanced conditions, the converter will supply/absorb unbalanced active power. In other words, each phase will supply/absorb a different amount of active power. This flow of active power changes the DC capacitor voltages, and this is of course not sustainable. The purpose of this thesis is therefore to define the problem of DC capacitor voltage balancing in MMC based STATCOMs, and to solve this problem for four different STATCOM topologies. A comparison of the advantages and disadvantages of each converter topology is then performed.

Chapters 2 and 3 of this thesis are dedicated to giving a brief overview of the basic purpose of STATCOMs as well as the operating principles of Voltage Source Converters (VSCs).

Chapter 4 presents a detailed explanation of the problem of capacitor DC voltage balancing. The flow of active power into the STATCOM legs is separated

into common mode active power flow and differential mode active power flow. It is then explained that the common mode active power flow can be easily controlled by setting the correct angle between the positive and negative sequence current references and the positive and negative sequence voltages present on the network. The control of differential mode active power flow requires additional controls which are specific to the converter topology. The subsequent chapters describe the four STATCOM topologies which are studied in this thesis, and the applicable methods for differential mode active power flow control are developed.

One solution applicable to all topologies that are evaluated in this thesis is to control the voltage of each cell locally. This is done by comparing the cell voltage to a reference, and modifying the switching pattern of each cell in order to change the time during which each cell is conducting. By doing so, it is possible to control the average energy absorption of each cell over a switching cycle and therefore control the voltage of each cell. Such methods are for example described in [18], [21] and [22]. A similar method is used in this thesis and is described in chapter 9 and in section 12.3.3. The difference is that in this thesis, localized control for each cell is not the only method used. It is used as part of a scheme of nested control loops. The reason is that these localized methods rely on the detection of an error in DC voltage. The additional control loops used here rely on measured network voltages and STATCOM currents in order to anticipate DC voltage drift caused by unbalanced operation. These methods anticipate the error and take corrective measures in order to prevent it. They are therefore different from methods which rely on the detection of an error.

These additional methods are however dependant on the converter topology. For a single wye-coupled or delta-coupled converter supplying positive sequence

currents to a network with unbalanced voltages, it is possible to impose a negative-sequence current that will cancel the flow of active power. Such methods are used, for example, in [5], [14] and [20]. This is not a preferred solution as the negative sequence currents increase the unbalance condition in the network. Furthermore, this method imposes a restriction on the operating range of the STATCOM. Indeed, it is not possible to provide any wanted positive sequence currents and negative sequence currents simultaneously as they are related by the need to cancel active power flow.

Chapter 6 presents another solution for the wye-coupled converter which is to impose a zero-sequence voltage on the neutral point of the converter. Such a method is presented in [19]. A similar method is developed in this thesis, with the difference that the calculation of the zero sequence voltage is simplified. This method does not create additional unbalance in the network, and is flexible in the sense that positive-sequence currents and negative sequence currents can be chosen somewhat independently. It can be shown that it is not always possible to find a finite zero-sequence voltage that will cancel the flow of active power if both a negative sequence current and a positive sequence current need to be supplied. Furthermore, this method requires that the converter be rated for a much higher voltage than the nominal system voltage.

Chapters 5 and 7 present the methods applicable to a delta-coupled converter or a wye-coupled converter with a neutral current path respectively. Both of these methods are based on the use of a zero-sequence current. A similar method to the ones which are developed in these chapters are also described in [4], [5] and [20] but again, the method presented for calculating the zero-sequence current reference produced by the converter assumes balanced leg currents, and is therefore not a general method. Moreover, the methods presented in this thesis are developed

based on the calculation of a differential power vector which is simpler and less cumbersome than the method described in [4], [5] and [20]. The zero-sequence current method does not require the converter to be overrated from a voltage perspective, however, it does require a higher current rating. It can also be shown for this method that it is not always possible to find a finite zero-sequence current that will cancel the flow of active power if both a positive sequence voltage and a negative sequence voltage are present in the network. This method also relies on the existence of a zero-sequence current path which requires the use of additional components such as a grounding transformer in the case of a wye-coupled converter.

Chapter 8 then explains how the exchange of common mode active power flow between the positive sequence and the negative sequence can be used in order to minimize the STATCOM leg currents and effectively increase the available reactive power output of the converter.

Chapter 9 gives a brief explanation of one more cause of DC capacitor unbalance which is the drift of cell DC voltages due to the non-ideal nature of components and switching patterns. A solution to this problem based on individual control of each cell is presented. This method is applicable regardless of the converter topology, and is used in conjunction with the common mode active power control and the differential mode active power control. Other methods such as selective swapping are described in [12]. The advantage of the method presented in this thesis is that it can be implemented locally for each cell and does not require centralized control.

Chapter 10 presents a fourth converter topology. This converter is composed of two wye-coupled converters with their neutral points connected together (or not). This type of converter configuration is used in the latest non-traditional HVDC applications [9]. A control scheme for DC capacitor voltage balancing is

presented in [13], but this control scheme requires the existence of a path for neutral current. In this thesis, it is shown that for this converter configuration, all methods described previously are applicable, but there also exists another method. Indeed, it is possible to use DC currents to cancel the active power flow. Due to the fact that this method relies on DC quantities, it can be shown that there always exists a finite solution that will cancel the active power flow. However, it also requires a converter with a higher current rating. It will also be shown how combining these methods may result in a reduction of the converter stresses. However, due to its topology the double-wye coupled converter requires more leg reactors and DC capacitors than the single wye-coupled converter, and is therefore more expensive and has a larger footprint.

Chapter 11 presents a brief comparison of the advantages and disadvantages of each of the converter topologies. The comparison is mainly done on the basis of limitations of the operating ranges due to the necessity of balancing DC voltages. The cost and complexity of each topology are also briefly mentioned.

Chapter 12 presents one proposed implementation of the methods described above for a simple STATCOM containing three cells per phase. This implementation is directly scalable for a converter with more cells.

Chapter 13 presents the results of simulations which were performed in order to validate that the DC voltage control methods function correctly.

CHAPTER 2
STATCOM Principles and Applications

The STATCOM, is one member of the large family of Flexible AC Transmission Systems Controllers (FACTS Controllers). In simple terms, the STATCOM is a shunt device which acts as a voltage source by controlling the amount of reactive power it absorbs or generates. This chapter briefly explains what STATCOMs are used for, and how they operate from a system point of view.

2.1 STATCOM Principles

Starting from a two bus network such as the one shown in figure 2–1, one can derive the following equations for active and reactive power flow. The derivation

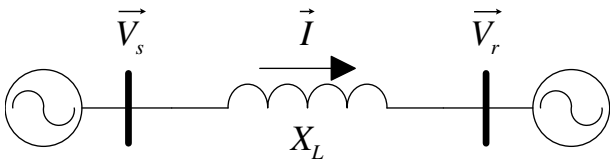

Figure 2–1: Two bus network with active/reactive power flow

is presented in appendix D and assumes that the angle between the sending end voltage and the receiving end voltage δ is small.

$$P_r \approx -\frac{V_r V_s \delta}{X_L} \tag{2.1}$$

$$Q_r \approx \frac{V_r V_s}{X_L} - \frac{V_r^2}{X_L} = \frac{V_r(V_s - V_r)}{X_L} \tag{2.2}$$

As demonstrated by equation (2.2), if one assumes that V_s is constant, then changing Q_r will mainly have an impact on V_r. In the network of figure 2–1, the

impedance X_L can be split into two parts. The first part can represent a Thevenin equivalent network together with the source V_s, and the second part can represent the combined transformer reactance and phase reactance of a STATCOM where the source V_r represents the converter. A schematic of a STATCOM is shown in figure 2–2. If the system is taken in per-unit, the transformer leakage inductance is

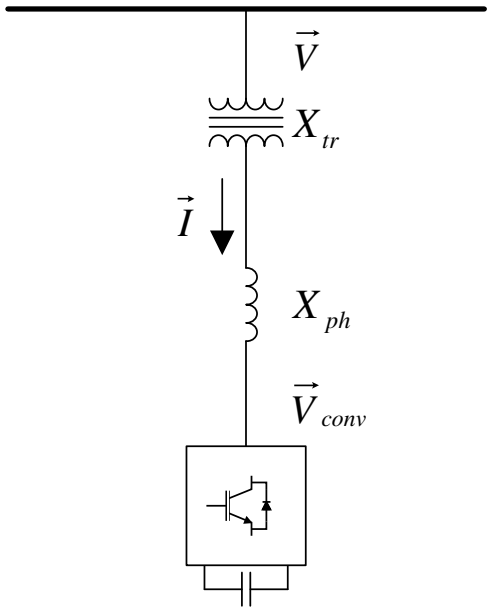

Figure 2–2: Typical STATCOM single-line diagram

lumped with the phase inductance of the STATCOM to form X_{stat}. If pure reactive power flow is assumed, the following relations can then be stated:

$$I = \frac{V - V_{conv}}{X_{stat}} \tag{2.3}$$

$$Q = \frac{1 - \frac{V_{conv}}{V}}{X_{stat}} V^2 \tag{2.4}$$

If V_{conv} is larger than V, the reactive power becomes negative and the STATCOM is therefore behaving as a capacitor. On the other hand, if V_{conv} is smaller than V, the reactive power becomes positive and the STATCOM is then behaving as a

reactor. In reality, a small amount of active power can flow into the STATCOM under certain conditions, and this will be dealt with in the subsequent chapters.

A simple control scheme is presented in figure 2–3 to control the positive sequence voltage at the STATCOM busbar. The busbar voltages are measured and

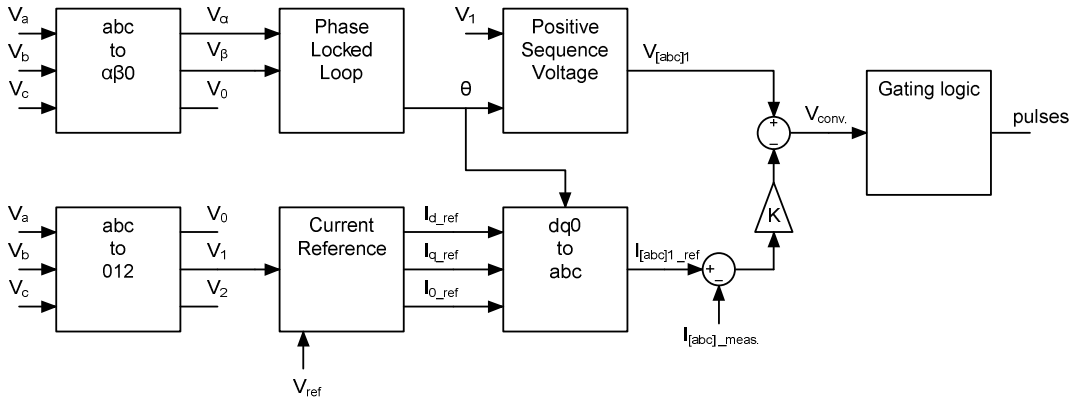

Figure 2–3: Simple STATCOM control scheme for positive sequence voltage control

transformed to the $\alpha\beta 0$ reference frame by applying the following transformation:

$$\begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \\ \vec{V}_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{2.5}$$

This transformation is also called the Clarke transformation [6], and for reference purposes, the inverse Clarke transformation is:

$$\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \\ \vec{V}_0 \end{bmatrix} \tag{2.6}$$

The Clarke transformation is basically a projection of the three-phase quantities onto two orthogonal axes where the α axis is in phase with phase a of the rotating three-phase system.

In order to obtain the positive sequence voltage and the d-q frame so as to implement the controls, it is necessary to acquire the argument $\theta = \omega t + \phi$ of the a-phase voltage. Along the upper path of figure 2–3, the a-b-c frame voltages are transformed to the $\alpha\beta 0$ frame using equation 2.5 and then passed to the Phase Locked Loop (PLL) of figure 2–4 which acquires the argument $\theta = \omega t + \phi$. The design of a phase-locked loop is fairly complex in the sense that its behaviour must be optimized according to several design criteria such as the desired response time, the range of frequencies to which it must be able to latch on to, the behavior in the presence of a negative sequence component as well as the behavior in the presence of harmonics to name a few. A simple phase-locked loop is shown in figure 2–4. Once the angular position θ is extracted by the PLL, it is used to reconstruct the

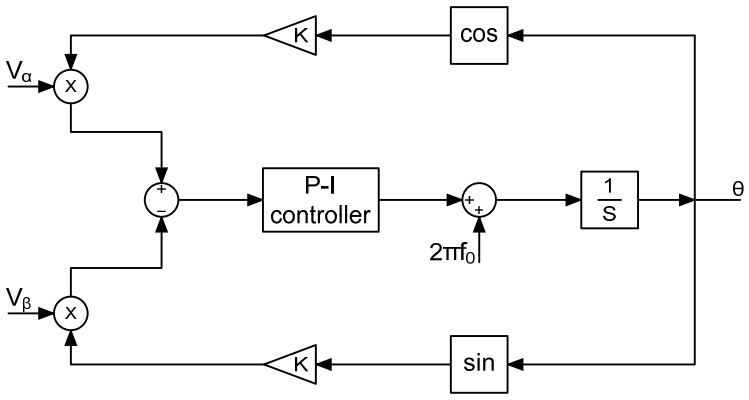

Figure 2–4: Simple Phase-Locked Loop

positive sequence voltage component of the phase voltages. This is simply done by implementing the following equation:

$$v_{a1}(t) = V_1 sin(\theta) \tag{2.7}$$

$$v_{b1}(t) = V_1 sin(\theta - \tfrac{2\pi}{3}) \tag{2.8}$$

$$v_{c1}(t) = V_1 sin(\theta - \tfrac{4\pi}{3}) \tag{2.9}$$

In parallel to this, the phase voltages are also transformed into their sequence components using the following equation.

$$\begin{bmatrix} \vec{V}_0 \\ \vec{V}_1 \\ \vec{V}_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{2.10}$$

where a is equal to $e^{j\frac{2\pi}{3}}$.

Equation (2.10) is derived in Appendix A. For a STATCOM application of positive sequence voltage support such as the one described here, the magnitude of the positive sequence current is computed based on the difference between the measured positive sequence voltage magnitude and the desired reference. The currents are computed in the $dq0$ reference frame and then transformed into the abc reference frame using equation 2.12 which is the inverse of the $dq0$ transformation. The $dq0$ transformation is:

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta - \frac{4\pi}{3}) \\ -sin(\theta) & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} I_a(t) \\ I_b(t) \\ I_c(t) \end{bmatrix} \tag{2.11}$$

and the inverse of the $dq0$ transformation is:

$$\begin{bmatrix} I_a(t) \\ I_b(t) \\ I_c(t) \end{bmatrix} = \begin{bmatrix} cos(\theta) & -sin(\theta) & 1 \\ cos(\theta - \frac{2\pi}{3}) & -sin(\theta - \frac{2\pi}{3}) & 1 \\ cos(\theta - \frac{4\pi}{3}) & -sin(\theta - \frac{4\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} \tag{2.12}$$

The $dq0$ is also a projection of the three-phase quantities onto two orthogonal axes where the d and q axes are orthogonal to each other, but this time they rotate at the same angular velocity $\theta = \omega t$ as the three-phase quantities. The d axis is in phase with phase a of the three-phase system at $t = 0$ and at every cycle. One

reason for using a current reference in the $dq0$ reference frame is that by using the angle $\theta = \omega t$ of the three-phase voltages produced by the PLL, the d component of the current then corresponds to a three-phase quantity which is in phase with the three-phase voltages. Similarly, the q component of the current corresponds to a three-phase quantity in quadrature with the three-phase voltages. In the dq frame, the active and reactive power are therefore:

$$P = V_d I_d + V_q I_q \tag{2.13}$$

$$Q = V_d I_q - V_q I_d \tag{2.14}$$

When the PLL is locked on to phase a, $V_q = 0$. Therefore:

$$P = V_d I_d \tag{2.15}$$

$$Q = V_d I_q \tag{2.16}$$

In other words, the d component of the current carries only active power whereas the q component of the current carries only reactive power. Since the desired operation of the STATCOM is to exchange only reactive power with the network, the reference current needed to support the positive sequence voltage should only have a q component. Once the current reference is transformed from the $dq0$ reference frame to a three-phase quantity, the measured phase currents are subtracted from it, the result is scaled by a proportional gain, and then subtracted from the positive sequence voltage which was reconstructed earlier. The result becomes the voltage reference that the converter will follow.

2.2 STATCOM Applications

The uses for STATCOMs and shunt compensation in general are multiple. In the context of transmission networks, they are often used for:

- End of line voltage support in order to prevent voltage instability. An example of this would be for voltage support at a load center in the event of load fluctuations or loss of one of several feeders.
- Improvement of transient stability, an example of which would be to provide fast dynamic voltage support during faults in order to avoid loss of synchronism of generators.
- Power oscillation damping in poorly damped power systems. Disturbances in poorly damped networks will have the tendancy to create mechanical oscillations in the rotors of generators, thus changing the voltage angle and creating oscillations in the active power transmitted.

In addition to the applications stated above, other applications exist which are more specific to industrial processes. These include:

- Flicker compensation for loads with a very stochastic behavior. An example of this would be flicker compensation for arc furnaces.
- Low order harmonic cancellation. STATCOMs being devices with a very fast response time, they are capable of cancelling the first few harmonic orders created by non-linear loads.
- Compensation of load unbalances. As will be seen in later chapters, STATCOMs are capable of generating unbalanced currents. This property can be used to compensate for unbalanced three-phase loads.

Additional information and more detailed explanations about some of these applications can be found in [10], [15] and [16]. The following chapter explains how the actual converter is implemented, and how it operates.

CHAPTER 3
Voltage Source Converters

This chapter explains what a Voltage Source Converter is, and describes how several of them can be connected to create a Modular Multilevel Converter (MMC).

3.1 Principles of a Basic Voltage Source Converter

The conventional thyristor, used in several FACTS devices such as the Static Var Compensators(SVC) or the Thyristor-Controlled Series Capacitors (TCSC) can be triggered to turn-on at any point on the half-cycle of voltage waveform during which the device is positively biased. However, the turn-off cannot be controlled. The device can only stop conducting once the current flowing through it goes to zero. Other devices such as the Integrated Gate Bipolar Transistor (IGBT) have both turn-on and turn-off capability. These devices therefore enable new converter concepts which can have significant cost and performance advantages [17]. One such converter type is the voltage source converter (VSC). The VSC concept can be applied to single-phase or multi-phase converters using either half-bridges or full-bridges. A single-phase, full bridge VSC is presented in figure 3–1. This converter is presented here in more detail because it is the building block of the STATCOMs which will be discussed in subsequent chapters. The VSC is composed of one DC capacitor, one series AC reactor, as well as four switches and four anti-parallel diodes. Since the DC voltage never changes polarities, anti-parallel diodes are sufficient to ensure operation in all four power quadrants. The four switches offer sixteen different on/off combinations. However, it is clear that closing both switches of the same leg at the same time, that is 1 and 2 or 3 and 4, would result in a short circuit across the capacitor which is of course undesireable. Eliminating

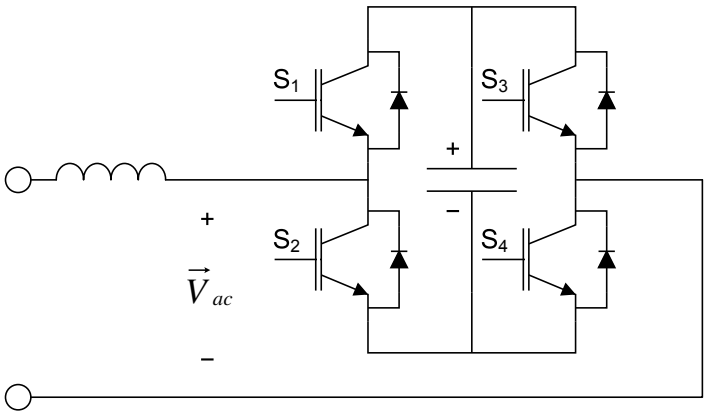

Figure 3–1: Single-phase, full-bridge voltage source converter

all switch combinations which include two switches of the same leg being closed at the same time, as well as all four combinations where only one switch is closed (which are of no use), five combinations of interest remain. These combinations are given in table 3–1. The last combination is valid, but is of no great interest

Table 3–1: Valid switch combinations in a full-bridge VSC

S_1	S_2	S_3	S_4	Voltage at terminals
1	0	0	1	$+V_{dc}$
0	1	1	0	$-V_{dc}$
1	0	1	0	0
0	1	0	1	0
0	0	0	0	Open Circuit

since it simply results in the converter being idle. The other four combinations are of more interest because by alternately changing between them, the voltage across the VSC terminals can be made to follow an AC voltage reference. This is done through the process of Sinusoidal Pulse Width Modulation (SPWM).

The full-bridge VSC can operate with two switching schemes; either bipolar switching or uni-polar switching. Bipolar switching requires that diagonal switch pairs always have the same state, meaning that the converter can only operate

using the two first switch combinations. Uni-polar switching on the other hand, allows for the use of all four switch combinations.

The principle of SPWM is that the sinusoidal reference $m(t)$ is compared to a triangular waveform $c(t)$ called the carrier. In the bipolar switching scheme, when $m(t) > c(t)$, switches 1 and 4 are on and switches 2 and 3 are off. When $m(t) < c(t)$, switches 1 and 4 are off and switches 2 and 3 are on. Assuming that

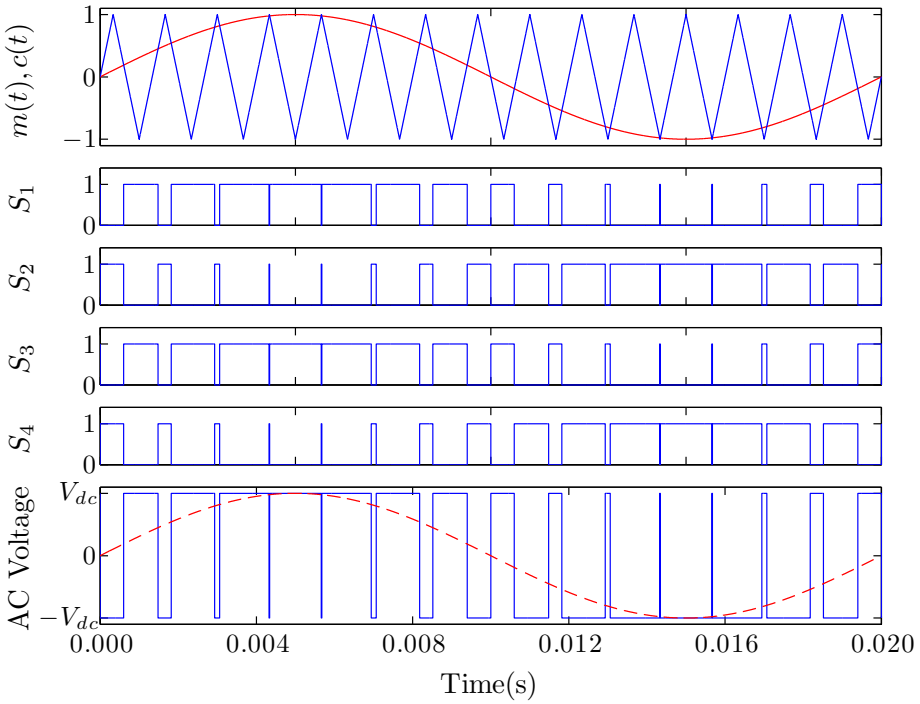

Figure 3–2: SPWM for a full-bridge bipolar switching VSC

the DC capacitor is large enough so that the DC voltage remains constant, and that the frequency of $c(t)$ is much higher than that of $m(t)$, the average of the AC voltage over one switching period is equal to the duty cycle times the DC voltage. This situation is illustrated in figure 3–2. In the unipolar switching scheme, the on/off states of switches 1 and 2 are generated in exactly the same way as for the bipolar switching scheme. The on/off states of switches 3 and 4 are generated by

comparing $-m(t)$ with $c(t)$. when $-m(t) < c(t)$, switch 4 is on and switch 3 is off. When $-m(t) > c(t)$, switch 4 is off and switch 3 is on. This situation is illustrated in figure 3–3. The major advantage of the uni-polar switching scheme over the

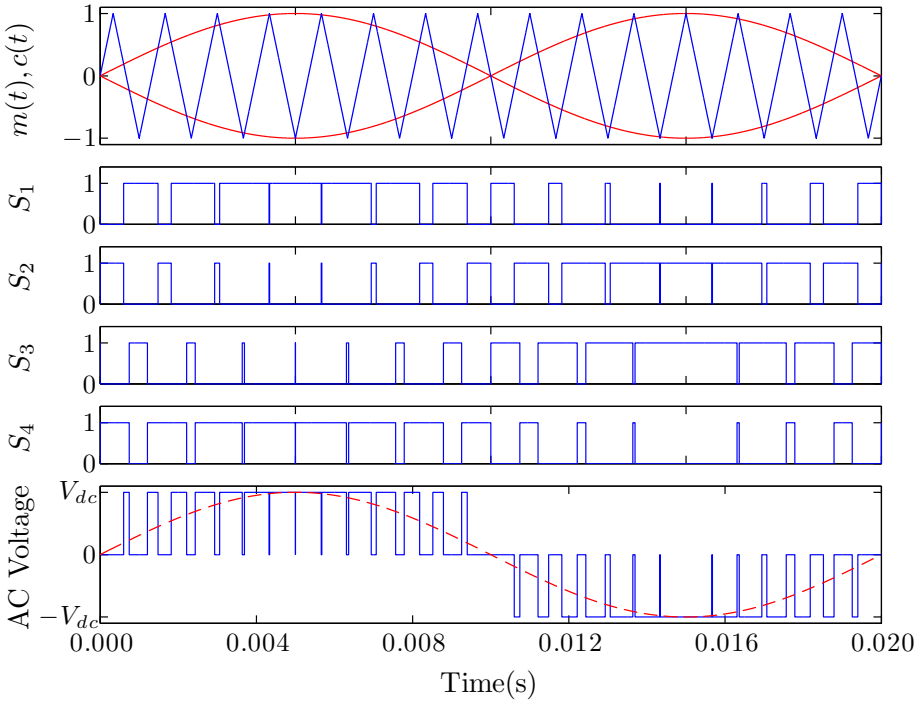

Figure 3–3: SPWM for a full-bridge uni-polar switching VSC

bipolar scheme is that the generated waveform is a much better approximation to the reference waveform. The result is much lower harmonic distortion.

It should be noted that although this converter allows four quadrant operation, the flow of active power is restricted to exactly the amount necessary to replace the converter losses and maintain the DC capacitor voltage. Indeed, since the DC buses are not connected to a generator or load, a larger flow of active power would result in a change in DC capacitor voltage. In this configuration, the VSC is therefore more suitable for a STATCOM application since in this case, the converter supplies/absorbs reactive power.

3.2 Modular Multilevel Converter

The full-bridge VSC with uni-polar switching as described in the previous section cannot be used for applications with high voltages since the withstand capability of the switching devices is in the order of a few kilovolts. Furthermore, the AC-side voltage waveform at the output of the VSC of figure 3–1 has a fairly high harmonic content. A solution to the latter problem could be to increase the carrier frequency and therefore the switching frequency. This would indeed generate less lower order harmonics from the switching itself, however, this would also increase switching losses to an undesirable level. A better solution to the two problems stated above is to connect several VSCs in series. The result is that the total required AC voltage is then shared between several cells, and by staggering the switching pattern of the cells, it becomes possible to obtain an effective switching frequency which is much higher, thus obtaining a cleaner waveform. This type of converter is referred to as a chain-link Modular Multilevel Converter (MMC) due to the fact that it is composed of several identical cells (or modules) connected in a chain. An example of such an MMC based chain-link VSC with three cells is presented in figure 3–4. It should be noted that a single AC reactor is necessary

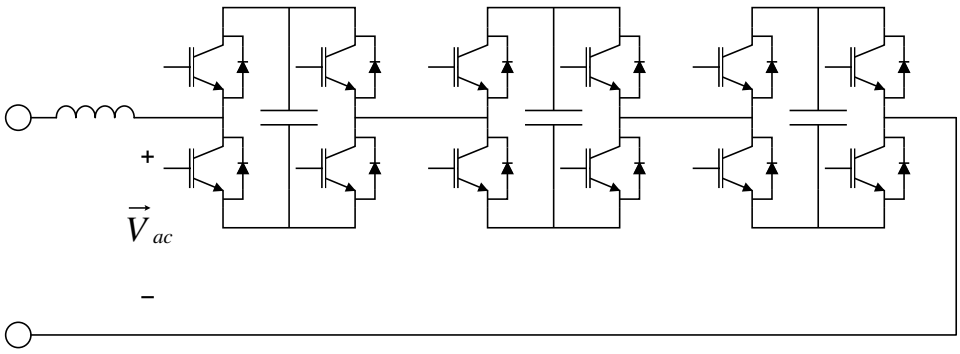

Figure 3–4: Modular Multilevel Converter based chain-link VSC

for the entire converter due to the series connection. It is also worth noting that

in theory, any number of cells can be connected in series. In order to achieve the staggering of the switching patterns, each cell uses the same AC reference, but the triangular carriers are shifted by an angle

$$\phi_{c,n} = \frac{\pi}{N}(n-1) \tag{3.1}$$

where $\phi_{c,n}$ is the phase shift applied to the carrier of cell n, and N is the total number of series connected cells in the chain. Figure 3–5 shows the shifted triangular carriers as well as the resulting AC waveform for $N = 3$.

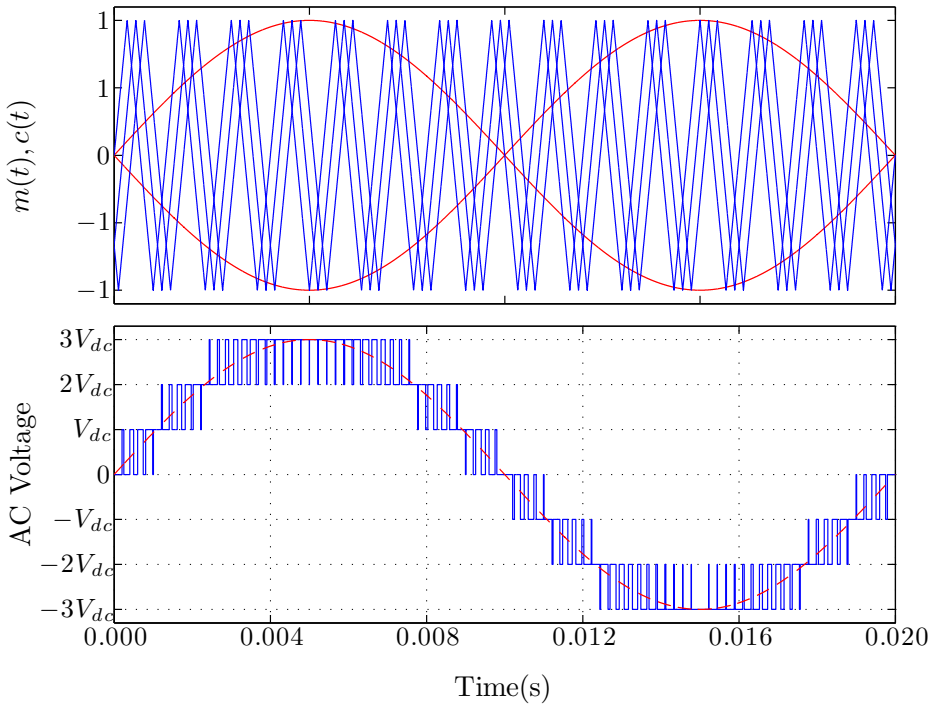

Figure 3–5: SPWM for a full-bridge uni-polar switching MMC chain-link VSC using three cells

For the case of the single VSC in the previous section, the DC voltage on the capacitor had to be at least as high as the maximum AC voltage waveform to be reproduced in order to avoid overmodulation. In the case of the chain-link converter, it is the sum of all DC voltages that has to be at least as high as the maximum

AC voltage waveform to be reproduced. This clearly shows the suitability of the MMC chain-link converter for high voltage applications. Not surprisingly, the total number of voltage levels that can be reproduced is proportional to the number of cells.

$$n_{levels} = 2N + 1 \tag{3.2}$$

The AC waveform presented in figure 3–5 is a much better approximation to the AC reference than the AC waveforms in figures 3–2 and 3–3. By increasing the number of cells in a given converter, the harmonic content of the AC waveform is reduced to a point where AC harmonic filters may no longer be required. The following chapter will describe one of the problem which MMC based STATCOMs are faced with when operating in unbalanced network conditions.

CHAPTER 4
The Problem of DC Capacitor Voltage Balancing

The STATCOM described as a three phase voltage source in chapter 2 can be constructed by using individual MMC-based VSCs such as the one shown in figure 3–4 for each phase. Several different topologies can be acheived by connecting the VSCs in different ways. For example, two of the simplest and more intuitive topologies are the wye-coupled converters, where each phase of the STATCOM is connected phase-to-ground, and the delta-coupled converters, where each phase of the STATCOM is connected phase-to-phase. Variants of these topologies as well as other topologies also exist. However, all of them suffer from the same problem which is DC capacitor voltage unbalance. The present chapter will describe the problem, and the subsequent chapters will present the main converter topologies of interest as well as the applicable solutions for balancing these DC capacitor voltages.

As explained earlier, except for the active power needed to replace the losses in the converter, a STATCOM should only exchange reactive power with the network. A larger (or smaller) exchange of active power would result in a change of the DC voltages of the capacitors since these DC buses are floating. For now, and until section 12.1, converter losses will be neglected in order to simplify the explanation. Therefore, under normal operation in a network having only a positive sequence voltage, it can be assumed that the STATCOM will generate a positive sequence current which is either purely capacitive or purely inductive (or zero). However, in unbalanced conditions such as those explained in appendix C, if, for example, the STATCOM is to supply positive sequence reactive power, it will also

supply/absorb active and reactive power due to the product of positive sequence current with negative sequence and zero sequence voltage. Furthermore, not only will the STATCOM exchange active power with the network, but it will do so in an unbalanced way. That is, the active power flowing in/out of each phase will be different.

In order to quantify and understand how this occurs, let us first consider the general case where STATCOM voltages and currents have positive sequence, negative sequence and zero sequence components ("1", "2" and "0" sub-indices).

$$\vec{V}_a = \vec{V}_{a0} + \vec{V}_{a1} + \vec{V}_{a2} \tag{4.1}$$

$$\vec{V}_b = \vec{V}_{b0} + \vec{V}_{b1} + \vec{V}_{b2} \tag{4.2}$$

$$\vec{V}_c = \vec{V}_{c0} + \vec{V}_{c1} + \vec{V}_{c2} \tag{4.3}$$

$$\vec{I}_a = \vec{I}_{a0} + \vec{I}_{a1} + \vec{I}_{a2} \tag{4.4}$$

$$\vec{I}_b = \vec{I}_{b0} + \vec{I}_{b1} + \vec{I}_{b2} \tag{4.5}$$

$$\vec{I}_c = \vec{I}_{c0} + \vec{I}_{c1} + \vec{I}_{c2} \tag{4.6}$$

The equations above use a simplified notation for the sequence components in each phase quantity. For the full expression of each component, the reader may refer to Appendix A. The active power flowing in each phase is the dot product of voltage and current which gives

$$P = \vec{V} \cdot \vec{I} \tag{4.7}$$

$$= (\vec{V}_0 + \vec{V}_1 + \vec{V}_2) \cdot (\vec{I}_0 + \vec{I}_1 + \vec{I}_2) \tag{4.8}$$

$$= \vec{V}_0 \cdot \vec{I}_0 + \vec{V}_0 \cdot \vec{I}_1 + \vec{V}_0 \cdot \vec{I}_2 + \vec{V}_1 \cdot \vec{I}_0 + \vec{V}_1 \cdot \vec{I}_1 + \vec{V}_1 \cdot \vec{I}_2 + \vec{V}_2 \cdot \vec{I}_0 + \vec{V}_2 \cdot \vec{I}_1 + \vec{V}_2 \cdot \vec{I}_2 \tag{4.9}$$

By applying the transformation developed in appendix B to equation 4.9 for all three phases of the STATCOM, it is possible to identify the terms of equation 4.9 which result in a balanced flow of active power, and those which result in an unbalanced flow of active power.

$$\begin{bmatrix} x_{1,diff} \\ x_{2,diff} \\ x_{comm} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} P_a \\ P_b \\ P_c \end{bmatrix} \tag{4.10}$$

The P_a, P_b and P_c are the expressions for active power flow into each phase as given by equation 4.9. In equation 4.10, the x_{comm} term represents the common mode power, that is, the power which is common to all three phases, whereas the $x_{1,diff}$ and $x_{2,diff}$ terms represent together the differential mode power, that is, the power which is unbalanced in all three phases. Similar methods for finding the common mode and differential mode quantities of three phase variables are described in [8] and [23]. Applying this to the product of positive sequence voltage and positive sequence current,

$$\begin{bmatrix} P_{a11} \\ P_{b11} \\ P_{c11} \end{bmatrix} = \begin{bmatrix} Re\{V_1\angle(\phi_{V1}) \cdot I_1\angle(\phi_{I1})\} \\ Re\{V_1\angle(\phi_{V1} - \frac{2\pi}{3}) \cdot I_1\angle(\phi_{I1} - \frac{2\pi}{3})\} \\ Re\{V_1\angle(\phi_{V1} - \frac{4\pi}{3}) \cdot I_1\angle(\phi_{I1} - \frac{4\pi}{3})\} \end{bmatrix} = \begin{bmatrix} V_1 I_1 cos(\Delta\phi_{V1I1}) \\ V_1 I_1 cos(\Delta\phi_{V1I1}) \\ V_1 I_1 cos(\Delta\phi_{V1I1}) \end{bmatrix} \tag{4.11}$$

we get the following expression for differential mode and common mode power.

$$\begin{bmatrix} x_{1,diff} \\ x_{2,diff} \\ x_{comm} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ V_1 I_1 cos(\Delta\phi_{V1I1}) \end{bmatrix} \tag{4.12}$$

As expected, the product of positive sequence voltage and positive sequence current gives only common mode power. Now, applying the same procedure to the product of positive sequence voltage and negative sequence current,

$$\begin{bmatrix} P_{a12} \\ P_{b12} \\ P_{c12} \end{bmatrix} = \begin{bmatrix} Re\{V_1\angle(\phi_{V1}) \cdot I_2\angle(\phi_{I2})\} \\ Re\{V_1\angle(\phi_{V1} - \frac{2\pi}{3}) \cdot I_2\angle(\phi_{I2} - \frac{4\pi}{3})\} \\ Re\{V_1\angle(\phi_{V1} - \frac{4\pi}{3}) \cdot I_2\angle(\phi_{I2} - \frac{2\pi}{3})\} \end{bmatrix} = \begin{bmatrix} V_1 I_2 cos(\Delta\phi_{V1I2}) \\ V_1 I_2 cos(\Delta\phi_{V1I2} + \frac{2\pi}{3}) \\ V_1 I_2 cos(\Delta\phi_{V1I2} - \frac{2\pi}{3}) \end{bmatrix} \tag{4.13}$$

we get the following expression for differential mode and common mode power.

$$\begin{bmatrix} x_{1,diff} \\ x_{2,diff} \\ x_{comm} \end{bmatrix} = \begin{bmatrix} V_1 I_2 cos(\Delta\phi_{V1I2}) \\ -V_1 I_2 \left(\frac{1}{2} cos(\Delta\phi_{V1I2}) + \frac{\sqrt{3}}{2} sin(\Delta\phi_{V1I2})\right) \\ 0 \end{bmatrix} \tag{4.14}$$

The product of positive sequence voltage and negative sequence current gives only differential mode power. In fact, the previous analysis can be done for all the terms in equation 4.9, and the result is that the product of same sequence voltages and currents gives only common mode power whereas the product of different sequence voltages and currents gives only differential mode power.

$$\left.\begin{matrix} \vec{V_0} \cdot \vec{I_0} \\ \vec{V_1} \cdot \vec{I_1} \\ \vec{V_2} \cdot \vec{I_2} \end{matrix}\right\} \Rightarrow x_{comm} \qquad \left.\begin{matrix} \vec{V_0} \cdot \vec{I_1} \\ \vec{V_0} \cdot \vec{I_2} \\ \vec{V_1} \cdot \vec{I_0} \\ \vec{V_1} \cdot \vec{I_2} \\ \vec{V_2} \cdot \vec{I_0} \\ \vec{V_2} \cdot \vec{I_1} \end{matrix}\right\} \Rightarrow x_{diff} \tag{4.15}$$

The common mode power terms cause a uniform change of capacitor voltage in all phases. This situation can usually be prevented by properly defining the current

reference of the STATCOM so that all sequence currents are out of phase by $\pm\frac{\pi}{2}$ with respect to the voltages of the same sequence. The differential mode power terms on the other hand, cause an unbalanced change of capacitor voltage in each of the phases. Methods for preventing this situation depend on the configuration of the converter, and will be the focus of the subsequent chapters.

CHAPTER 5
Delta-Coupled Chain-Link STATCOM

The first topology that is of interest is the delta-coupled chain-link STATCOM. The intent of this chapter is to describe this topology, and to solve the problem of capacitor DC voltage balancing which is described in chapter 4 for this specific topology. A schematic of the delta-coupled chain-link STATCOM is shown in figure 5–1. By delta-coupled, it is implied that the VSCs are connected between

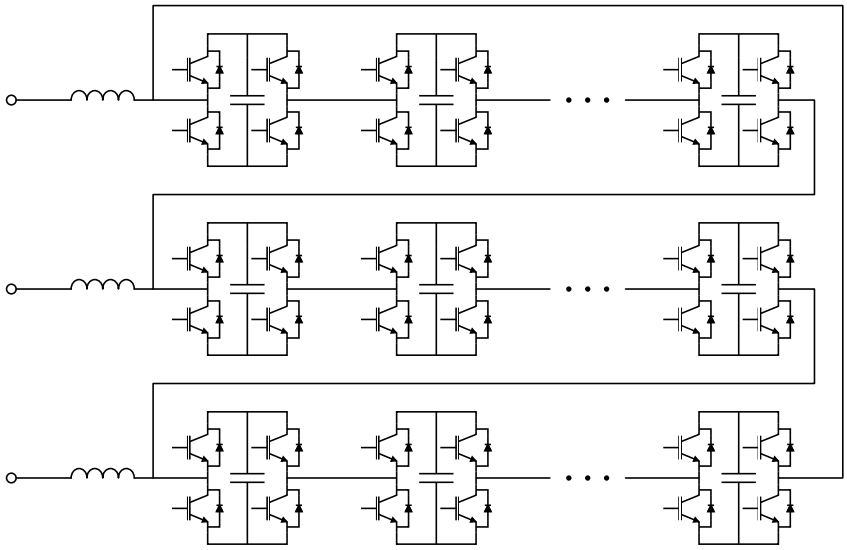

Figure 5–1: Delta-Coupled Chain-Link STATCOM

phases of a three-phase system. The voltage reference developed in figure 2–3 is computed using phase to phase quantities, and is applied to the SPWM algorithm of section 3.2 for all cells of the three phases of the STATCOM in figure 5–1.

The currents and voltages to consider in the calculation of the previous chapter are of course the currents through the converter legs, and the voltages across them. In the case of the delta-coupled STATCOM, the currents are therefore the currents

inside the delta, while the voltages are the phase to phase voltages. This means that positive sequence, negative sequence and zero sequence currents can flow around the delta, however, only positive sequence voltages and negative sequence voltages are present across the legs since zero sequence voltages are eliminated due to the delta-connection. Equation 4.9 therefore reduces to

$$P = \vec{V_1} \cdot \vec{I_0} + \vec{V_1} \cdot \vec{I_1} + \vec{V_1} \cdot \vec{I_2} + \\ \vec{V_2} \cdot \vec{I_0} + \vec{V_2} \cdot \vec{I_1} + \vec{V_2} \cdot \vec{I_2} \tag{5.1}$$

Considering a case where the following positive and negative sequence voltages are present while the STATCOM is providing positive sequence currents and negative sequence currents,

$$\vec{V_1} = V_1 \angle \phi_1 \tag{5.2}$$

$$\vec{V_2} = V_2 \angle \phi_2 \tag{5.3}$$

it is possible to choose

$$\vec{I_1} = I_1 \angle \left(\phi_1 \pm \frac{\pi}{2} \right) \tag{5.4}$$

$$\vec{I_2} = I_2 \angle \left(\phi_2 \pm \frac{\pi}{2} \right) \tag{5.5}$$

in order to ensure that

$$\vec{V_1} \cdot \vec{I_1} = 0 \tag{5.6}$$

$$\vec{V_2} \cdot \vec{I_2} = 0 \tag{5.7}$$

However, it cannot be guaranteed in all conditions that

$$\vec{V_1} \cdot \vec{I_2} + \vec{V_2} \cdot \vec{I_1} = 0 \tag{5.8}$$

From equation 5.1 and from the fact that the STATCOM is delta-coupled, it is interesting to notice that another degree of freedom is available. That is, a zero sequence current reference can be imposed on the STATCOM which will not influence the phase currents outside the delta. However, inside the delta, this current can be used to cancel the effect of the remaining unbalance terms. In other words, the idea is to chose $\vec{I_0}$ so that

$$\vec{V_1} \cdot \vec{I_0} + \vec{V_1} \cdot \vec{I_2} + \vec{V_2} \cdot \vec{I_0} + \vec{V_2} \cdot \vec{I_1} = 0 \tag{5.9}$$

A different approach to the one developed here is used in [4] where an expression for $\vec{I_0}$ is defined using space vectors for an application where a delta-coupled STATCOM is compensating for an asymmetrical load. This is a specific case where only the differential power term $\vec{V_1} \cdot \vec{I_2}$ needs to be cancelled. However, the space vector approach becomes somewhat cumbersome when trying to solve the general case of equation 5.9. The power vector approach is more suitable for deriving a full expression for $\vec{I_0}$ in the general case.

In order to solve for $\vec{I_0}$, equation 5.9 can be rewritten in the following form:

$$Re\left(\vec{V_1}\vec{I_0}^*\begin{bmatrix}1\\a^2\\a\end{bmatrix} + \vec{V_2}\vec{I_0}^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}\right) = -Re\left(\vec{V_1}\vec{I_2}^*\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \vec{V_2}\vec{I_1}^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{5.10}$$

To obtain equation 5.10, equation 5.9 was expressed for each of the three phases, and the terms were reorganised so that the three rows of equation 5.10 represent the active power in each of the three phases. It is then possible to solve for $\vec{I_0}$. Indeed, there are two unknowns which are the magnitude and the phase of the zero sequence current. It is therefore required to solve two of the three rows of equation 5.10. In other words, since equation 5.10 contains only differential mode active power terms, if the active power flow is cancelled in two phases, it will

necessarily be zero in the third phase as well. Solving for example the first and second rows, one gets:

$$I_0 = \frac{(-V_1 I_2 sin(\phi_{2,i} - \phi_2) + V_2 I_1 sin(\phi_{1,i} - \phi_1))\, sin(\phi_1 - \phi_2)}{V_1 cos(\phi_1 - \phi_0) + V_2 cos(\phi_2 - \phi_0)} \tag{5.11}$$

$$\phi_0 = -arctan\left(\frac{V_1 + V_2 cos(-3\phi_1 + 3\phi_2)}{V_2 sin(-3\phi_1 + 3\phi_2)}\right) + 2\phi_1 - \phi_2 \tag{5.12}$$

The subscripts i in 5.11 denote that the angle in question is the angle of the current phasor. The other angles are related to the voltage phasors. The latter equations are valid only if sequence currents are orthogonal to the corresponding sequence voltages as described in equations 5.2 to 5.5. Therefore, the first two sine terms in the numerator of equation 5.11 simplify to ± 1 depending if the sequence currents are inductive or capacitive with respect the sequence voltages. In order to simplify the notation here and in further chapters, the following quantities will be defined:

$$\sigma_1 = I_1 sin(\phi_{1,i} - \phi_1) \tag{5.13}$$

$$\sigma_2 = I_2 sin(\phi_{2,i} - \phi_2) \tag{5.14}$$

Equation 5.11 then become:

$$I_0 = \frac{(-V_1 \sigma_2 + V_2 \sigma_1)\, sin(\phi_1 - \phi_2)}{V_1 cos(\phi_1 - \phi_0) + V_2 cos(\phi_2 - \phi_0)} \tag{5.15}$$

Also, looking at equations 5.11 and 5.12, it is clear that the magnitude of the zero sequence current becomes zero for $\phi_1 - \phi_2 = 0$ or π. However, this solution does not solve equation 5.9 and can therefore be considered degenerate. In fact, the first row of equation 5.10 becomes degenerate for $\phi_1 - \phi_2 = 0$ or π, the second row becomes degenerate for $\phi_1 - \phi_2 = -\frac{2\pi}{3}$ or $\frac{\pi}{3}$ and the third row becomes degenerate for $\phi_1 - \phi_2 = \frac{2\pi}{3}$ or $\frac{5\pi}{3}$.

In other words, each of the three equations becomes degenerate for a different angle difference between positive and negative sequence voltages. Referring to table C–1 in appendix C, the reader will realise that several fault cases result in an angle difference $\phi_1 - \phi_2$ which causes one of the equations to become degenerate. Hence, in order to have a robust system which gives a correct solution in all conditions, all three combinations of two equations must be solved simultaneously. In that way, at least two of the three solutions will be correct at all times.

CHAPTER 6
Ungrounded Wye-Coupled Chain-Link STATCOM

It is also possible to connect the single-phase chain-link VSCs to create an ungrounded wye-coupled STATCOM such as the one shown in figure 6–1. The current chapter describes this topology, and solves the problem of capacitor DC voltage balancing specific to this topology. The individual converter legs are con-

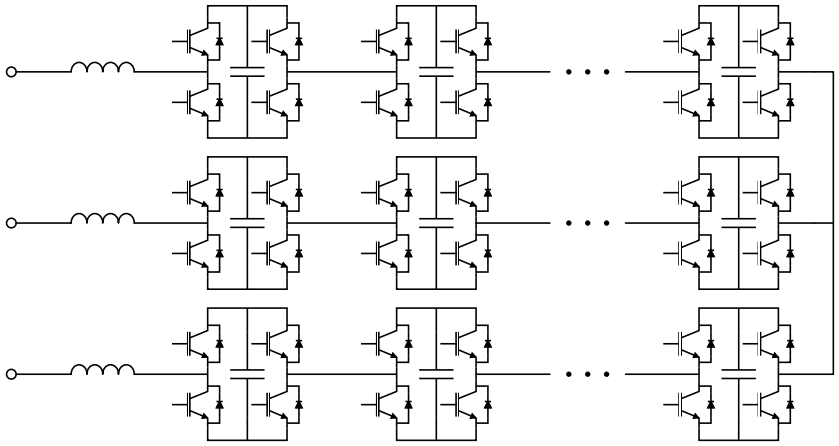

Figure 6–1: Ungrounded Wye-Coupled Chain-Link STATCOM

nected between the phase voltage and a floating neutral point. This means that a method analogous to the zero sequence current method of the previous chapter can be used in this case by applying a zero sequence voltage on the converter neutral point. Equation 4.9 therefore reduces to

$$P = \vec{V}_1 \cdot \vec{I}_1 + \vec{V}_1 \cdot \vec{I}_2 + \vec{V}_2 \cdot \vec{I}_1 + \vec{V}_2 \cdot \vec{I}_2 + \vec{V}_0 \cdot \vec{I}_1 + \vec{V}_0 \cdot \vec{I}_2 \tag{6.1}$$

The zero sequence voltage can then be chosen such that the sum of all unbalanced active power terms is zero. In other words, the idea is to chose $\vec{V_0}$ so that

$$\vec{V_1} \cdot \vec{I_2} + \vec{V_2} \cdot \vec{I_1} + \vec{V_0} \cdot \vec{I_1} + \vec{V_0} \cdot \vec{I_2} = 0 \tag{6.2}$$

In order to solve for $\vec{V_0}$, equation 6.2 can be rewritten in the following form:

$$Re\left(\vec{V_0}\vec{I_1^*}\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \vec{V_0}\vec{I_2^*}\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) = -Re\left(\vec{V_1}\vec{I_2^*}\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \vec{V_2}\vec{I_1^*}\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{6.3}$$

where each of the three rows represents the application of equation 6.2 in each of the three phases. It is then possible to solve for $\vec{V_0}$. Indeed, there are two unknowns which are the magnitude and the phase of the zero sequence voltage. It is therefore required to solve two of the three rows of equation 6.3. Solving for example the first and second rows, one gets:

$$V_0 = \frac{(-V_1\sigma_2 + V_2\sigma_1)sin(\phi_1 - \phi_2)}{\sigma_1 sin(\phi_0 - \phi_1) + \sigma_2 sin(\phi_0 - \phi_2)} \tag{6.4}$$

$$\phi_0 = arctan\left(\frac{\sigma_2 sin(-3\phi_1 + 3\phi_2)}{\sigma_1 + \sigma_2 cos(-3\phi_1 + 3\phi_2)}\right) + 2\phi_1 - \phi_2 \tag{6.5}$$

As in the previous chapter, the latter equations are valid only if sequence currents are orthogonal to the corresponding sequence voltages as described in equations 5.2 to 5.5. The definitions of σ_1 and σ_2 are given in 5.13 and 5.14 respectively.

Also, looking at equations 6.4 and 6.5, it is clear that the magnitude of the zero sequence voltage becomes zero for $\phi_1 - \phi_2 = 0$ or π. However, this solution does not solve the power balance equation 6.2. This solution can therefore be considered degenerate. In fact, the first row of equation 6.3 becomes degenerate

for $\phi_1 - \phi_2 = 0$ or π, the second row becomes degenerate for $\phi_1 - \phi_2 = -\frac{2\pi}{3}$ or $\frac{\pi}{3}$ and the third row becomes degenerate for $\phi_1 - \phi_2 = \frac{2\pi}{3}$ or $\frac{5\pi}{3}$.

In other words, each of the three equations becomes degenerate for a different angle difference between positive and negative sequence voltages. Referring to table C–1 in appendix C, the reader will realise that several fault cases result in an angle difference $\phi_1 - \phi_2$ which causes one of the equations to become degenerate. Hence, in order to have a robust system which gives a correct solution in all conditions, all three combinations of two equations must be solved simultaneously. In that way, at least two of the three solutions will be correct at all times.

CHAPTER 7
Grounded Wye-Coupled Chain-Link STATCOM

It is also possible to connect the single-phase chain-link VSCs to get a grounded wye-coupled STATCOM such as the one shown in figure 7–1. The current chapter describes this topology, and solves the problem of capacitor DC voltage balancing specific to this topology. The neutral point is grounded through a grounding

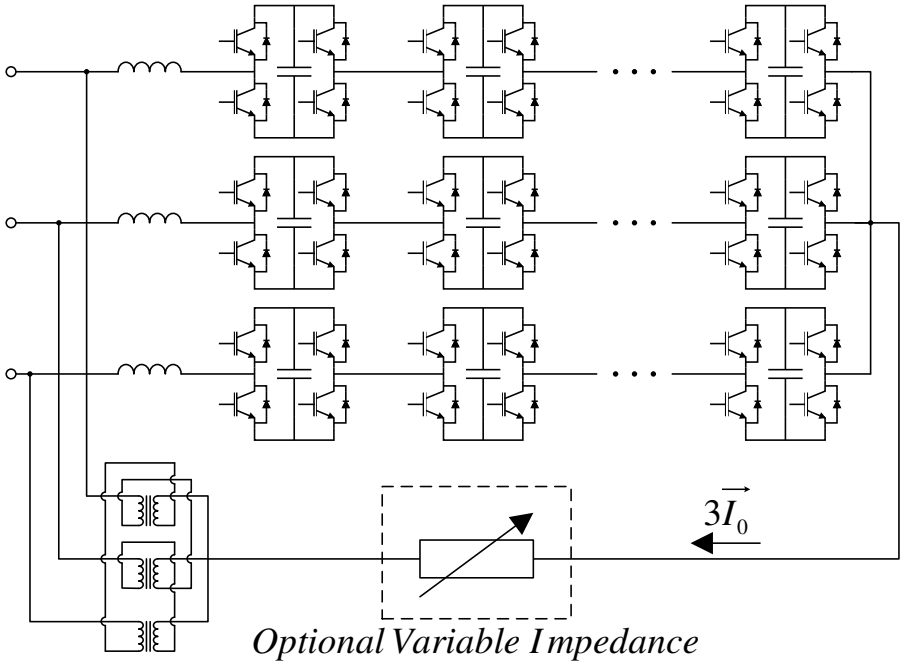

Figure 7–1: Grounded Wye-Coupled Chain-Link STATCOM

transformer, and the grounding path allows for a zero sequence current to flow. If the grounding path impedance is assumed to be negligible, the only contribution to the zero sequence voltage at the neutral point comes from the zero sequence voltage already present in the network (if any). In other words, the neutral is still floating with respect to ground and thus, no zero sequence voltage appears

across the valves. This means that this converter is similar to the delta coupled converter of chapter 5, and equations 5.11 and 5.12 could still apply with the slight modification that the voltages to be controlled are the phase to ground voltages.

In practice however, the grounding path impedance is not negligible. This is due to the non-zero impedance of the grounding transformer, but it can also be due to the fact that a series impedance may be purposely added. In this case, the flow of zero sequence current will create a zero sequence voltage at the neutral point where the relation is:

$$\vec{V_0} = 3Z_n\vec{I_0} \tag{7.1}$$

The factor three arises from the fact that each phase contributes a current $\vec{I_0}$ to the neutral current. The neutral impedance Z_n is a complex number representing the grounding path impedance. This grounding path impedance may be defined in three ways:

- Only grounding transformer impedance
- The sum of grounding transformer impedance and fixed series impedance
- The sum of grounding transformer impedance and variable series impedance

The first two cases are similar in the sense that the neutral path impedance has a fixed value. For the following derivation, a fixed neutral path impedance is assumed and Z_n will be expressed in polar coordinates as $Z_0\angle\zeta$. Due to the existence of both a zero sequence voltage and a zero sequence current, all terms of equation 4.15 are present. In order to have no unbalanced active power flow, the following condition

must be met:

$$Re\left(\vec{V}_1\vec{I}_0^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}+\vec{V}_2\vec{I}_0^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}+\vec{V}_0\vec{I}_1^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}+\vec{V}_0\vec{I}_2^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right)$$
$$=-Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}+\vec{V}_2\vec{I}_1^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{7.2}$$

Equation 7.2 can be simplified by using 7.1 to either solve for $\vec{I}_0$ or $\vec{V}_0$. Solving for $\vec{I}_0$ will result in the following expression:

$$Re\left(\vec{V}_1\vec{I}_0^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}+\vec{V}_2\vec{I}_0^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}+3Z_n\vec{I}_0\vec{I}_1^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}+3Z_n\vec{I}_0\vec{I}_2^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right)$$
$$=-Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix}1\\a\\a^2\end{bmatrix}+\vec{V}_2\vec{I}_1^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{7.3}$$

Note that the three rows of 7.2 and 7.3 are simply stating that the sum of the terms resulting in unbalanced active power flow must be zero for each of the three phases. It is then possible to solve for $\vec{I}_0$ in a similar way as in chapter 5. The result is:

$$I_0=\frac{(-V_1\sigma_2+V_2\sigma_1)sin(\phi_1-\phi_2)}{3Z_0\sigma_1 sin(\zeta+\phi_0-\phi_1)+3Z_0\sigma_2 sin(\zeta+\phi_0-\phi_2)+V_1 cos(\phi_1-\phi_0)+V_2 cos(\phi_2-\phi_0)} \tag{7.4}$$

$$\phi_0=-arctan\left(\frac{(3Z_0\sigma_1 sin(\zeta)+V_1)-3Z_0\sigma_2 cos(\zeta)sin(-3\phi_1+3\phi_2)+(3Z_0\sigma_2 sin(\zeta)+V_2)cos(-3\phi_1+3\phi_2)}{3Z_0\sigma_1 cos(\zeta)+3Z_0\sigma_2 cos(\zeta)cos(-3\phi_1+3\phi_2)+(3Z_0\sigma_2 sin(\zeta)+V_2)sin(-3\phi_1+3\phi_2)}\right)$$
$$+2\phi_1-\phi_2 \tag{7.5}$$

As in the previous chapter, the latter equations are valid only if sequence currents are orthogonal to the corresponding sequence voltages as described in equations 5.2 to 5.5. The definitions of σ_1 and σ_2 are given in 5.13 and 5.14 respectively. Also, as in the two previous chapters, all three combinations of two rows in equation 7.3 should be solved in parallel in order to ensure that a non-degenerate solution is found.

Unless there is a source or sink of active power in the neutral path, the neutral path impedance can be assumed to be purely reactive. This means that:

$$Z_n = Z_0 \angle \zeta = Z_0 \angle \pm \frac{\pi}{2} \tag{7.6}$$

and the equations above simplify to:

$$I_0 = \frac{(-V_1\sigma_2 + V_2\sigma_1)sin(\phi_1 - \phi_2)}{\pm 3Z_0\sigma_1 cos(\phi_0 - \phi_1) \pm 3Z_0\sigma_2 cos(\phi_0 - \phi_2) + V_1 cos(\phi_1 - \phi_0) + V_2 cos(\phi_2 - \phi_0)} \tag{7.7}$$

$$\phi_0 = -arctan\left(\frac{(\pm 3Z_0\sigma_1 + V_1) + (\pm 3Z_0\sigma_2 + V_2)cos(-3\phi_1 + 3\phi_2)}{(\pm 3Z_0\sigma_2 + V_2)sin(-3\phi_1 + 3\phi_2)}\right) + 2\phi_1 - \phi_2 \tag{7.8}$$

Note that the $(\pm)$ signs in equations 7.7 and 7.8 correspond to the two solutions generated by the $(\pm)$ sign in the expression for the angle of Z_n.

If a variable impedance such as an additional single phase MMC-based voltage source converter like the one presented in figure 3–4 is connected in series in the neutral path, the zero sequence voltage and the zero sequence current become independent. Indeed, equation 7.2 can be solved by choosing $\vec{V_0}$ and $\vec{I_0}$ separately, and choosing the neutral path impedance to be equal to:

$$Z_0 \angle \zeta = \frac{1}{3}\frac{\vec{V_0}}{\vec{I_0}} \tag{7.9}$$

The result is that an optimal combination of $\vec{V_0}$ and $\vec{I_0}$ can be chosen to minimize leg voltages and currents. To solve the power balance equation using both the zero sequence voltage and the zero sequence current, it is necessary to define how much of the unbalance compensation should be done by each of the zero sequence quantities. One way of defining this is to use the valve voltage rating. Indeed, it is possible to use the zero sequence voltage method to the extent where the valve voltage reaches its rated value. The remaining balancing is then done using the zero sequence current method, and the necessary neutral path impedance is calculated as per equation 7.9. The first step is therefore to calculate the required zero sequence voltage as if only that method was used. This amounts to solving equation 6.3. Once this is done, the angle of the zero sequence voltage is kept fixed and the amplitude is recomputed so that the resulting leg voltage magnitudes remain smaller than the maximum allowed leg voltage V_{max}. That is, writing the expression for the line to neutral voltage across the converter legs, where the neutral point is taken as the converter neutral before the variable neutral path impedance:

$$\vec{V}_{conv} = \vec{V}_0 \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} + \vec{V}_1 \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{V}_2 \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} \tag{7.10}$$

the individual phase voltages can be written as:

$$\vec{V}_a = 1V_0 e^{(j\phi_0)} + 1V_1 e^{(j\phi_1)} + 1V_2 e^{(j\phi_2)} \tag{7.11}$$

$$\vec{V}_b = 1V_0 e^{(j\phi_0)} + a^2 V_1 e^{(j\phi_1)} + aV_2 e^{(j\phi_2)} \tag{7.12}$$

$$\vec{V}_c = 1V_0 e^{(j\phi_0)} + aV_1 e^{(j\phi_1)} + a^2 V_2 e^{(j\phi_2)} \tag{7.13}$$

The inequality condition can then be solved for each phase. For example, the inequality condition for phase a is:

$$\|\vec{V_a}\| = \|V_0 e^{(j\phi_0)} + V_1 e^{(j\phi_1)} + V_2 e^{(j\phi_2)}\| \leq V_{max} \tag{7.14}$$

Solving for the amplitude of $\vec{V_0}$:

$$\begin{aligned} V_0 \leq & -\left(V_1 cos(\phi_0 - \phi_1) + V_2 cos(\phi_0 - \phi_2)\right) \\ & \pm \sqrt{\left(V_1 cos(\phi_0 - \phi_1) + V_2 cos(\phi_0 - \phi_2)\right)^2 - \left(V_1^2 + V_2^2 + 2V_1 V_2 cos(\phi_1 - \phi_2) - V_{max}^2\right)} \end{aligned} \tag{7.15}$$

Negative solutions for V_0 are then discarded since the angle of $\vec{V_0}$ has already been defined. The smallest solution from all three phases is taken as the largest allowed V_0. Finally, the remaining unbalance is cancelled by solving equation 7.2 for $\vec{I_0}$. The neutral path impedance required to achieve this is calculated using equation 7.9.

CHAPTER 8
Further Optimization to Increase STATCOM Output

It is possible to do some additional optimization in order to increase the STATCOM output while remaining within the constraints of leg current and voltage ratings. The following derivation is done for the delta-coupled STATCOM topology. However, this method also applies directly to the wye-coupled STATCOM with grounded neutral, and could apply to the wye-coupled STATCOM with floating neutral by modifying the equations to consider $\vec{V}_0$ instead of $\vec{I}_0$.

8.1 Defining a Degree of Freedom

In the general case for the delta-coupled STATCOM, the voltages across the legs and the currents in the legs are:

$$\vec{V}_a = \vec{V}_{a1} + \vec{V}_{a2} \tag{8.1}$$

$$\vec{V}_b = \vec{V}_{b1} + \vec{V}_{b2} \tag{8.2}$$

$$\vec{V}_c = \vec{V}_{c1} + \vec{V}_{c2} \tag{8.3}$$

$$\vec{I}_a = \vec{I}_{a0} + \vec{I}_{a1} + \vec{I}_{a2} \tag{8.4}$$

$$\vec{I}_b = \vec{I}_{b0} + \vec{I}_{b1} + \vec{I}_{b2} \tag{8.5}$$

$$\vec{I}_c = \vec{I}_{c0} + \vec{I}_{c1} + \vec{I}_{c2} \tag{8.6}$$

The active power flowing in each phase is the dot product of voltage and current which gives

$$P = \vec{V} \cdot \vec{I} \tag{8.7}$$

$$= (\vec{V_1} + \vec{V_2}) \cdot (\vec{I_0} + \vec{I_1} + \vec{I_2}) \tag{8.8}$$

$$= \vec{V_1} \cdot \vec{I_0} + \vec{V_1} \cdot \vec{I_1} + \vec{V_1} \cdot \vec{I_2} + \vec{V_2} \cdot \vec{I_0} + \vec{V_2} \cdot \vec{I_1} + \vec{V_2} \cdot \vec{I_2} \tag{8.9}$$

and as explained in the previous chapters, these terms can be divided as follows

$$\left.\begin{array}{l} \vec{V_1} \cdot \vec{I_1} \\ \vec{V_2} \cdot \vec{I_2} \end{array}\right\} \Rightarrow P_{comm} \qquad \left.\begin{array}{l} \vec{V_1} \cdot \vec{I_0} \\ \vec{V_1} \cdot \vec{I_2} \\ \vec{V_2} \cdot \vec{I_0} \\ \vec{V_2} \cdot \vec{I_1} \end{array}\right\} \Rightarrow P_{diff} \tag{8.10}$$

In order to prevent DC capacitor voltage unbalance, it is necessary that the sum of these terms be zero. In the existing method, the positive sequence current and positive sequence voltage are forced to be orthogonal in order to ensure that

$$\vec{V_1} \cdot \vec{I_1} = 0 \tag{8.11}$$

The same reasoning applies to the negative sequence current. It should be orthogonal to the negative sequence voltage so that

$$\vec{V_2} \cdot \vec{I_2} = 0 \tag{8.12}$$

A zero sequence current is then imposed inside the converter delta such that the sum of the differential power terms is zero.

$$\vec{V_1} \cdot \vec{I_0} + \vec{V_1} \cdot \vec{I_2} + \vec{V_2} \cdot \vec{I_0} + \vec{V_2} \cdot \vec{I_1} = 0 \tag{8.13}$$

This necessarily results in unbalanced leg currents. The STATCOM output power limitation is set by the maximum leg current, and in this unbalanced operation case, the STATCOM output is limited by the current in the phase which has the highest current, while the other two phases are operating at a lower current. The idea presented here is to minimize the maximum leg current in order to have a higher STATCOM output power limitation. However, it is clear from the equations above that there are no degrees of freedom available. In order to add a degree of freedom, it is proposed to allow positive sequence current and negative sequence currents to exchange common mode active power. This is done by relaxing the individual orthogonality conditions in 8.11 and 8.12, and replacing them by

$$\vec{V_1} \cdot \vec{I_1} + \vec{V_2} \cdot \vec{I_2} = 0 \tag{8.14}$$

This amounts to fixing the common mode reactive power for both the positive and the negative sequence, but leaving common mode active power as a degree of freedom as long as the sum for both the positive sequence and negative sequence is zero.

$$Q_{11} = V_1 I_1 sin(\phi_{1,v} - \phi_{1,i}) = fixed \tag{8.15}$$

$$Q_{22} = V_2 I_2 sin(\phi_{2,v} - \phi_{2,i}) = fixed \tag{8.16}$$

$$P_{11} = V_1 I_1 cos(\phi_{1,v} - \phi_{1,i}) = -V_2 I_2 cos(\phi_{2,v} - \phi_{2,i}) = -P_{22} \tag{8.17}$$

Now that an additional degree of freedom is available, it can be used to try to minimize leg currents while keeping the requirement that the sum of differential power terms remains zero. The problem then becomes one of constrained optimization.

8.2 The Optimization Problem

In order to solve this minimization problem, some equality and inequality constraints are defined, and the symmetrical components of the STATCOM currents are used as optimization variables. The goal is therefore to find the current symmetrical components which will minimize leg currents while satisfying all the constraints.

8.3 Inequality Constraints

In this problem, three inequality constraints are defined:

$$g_1(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = \|\vec{I_a}\| = \|I_0\angle\phi_{I0} + I_1\angle\phi_{I1} + I_2\angle\phi_{I2}\| \leq \gamma \quad (8.18)$$

$$g_2(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = \|\vec{I_b}\| = \|I_0\angle\phi_{I0} + a^2 I_1\angle\phi_{I1} + aI_2\angle\phi_{I2}\| \leq \gamma \quad (8.19)$$

$$g_3(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = \|\vec{I_c}\| = \|I_0\angle\phi_{I0} + aI_1\angle\phi_{I1} + a^2 I_2\angle\phi_{I2}\| \leq \gamma \quad (8.20)$$

Where the six optimization variables are: I_0, ϕ_{I0}, I_1, ϕ_{I1}, I_2 and ϕ_{I2}. The variable γ is simply the cost function of the minimization. It is understood that all voltage and current magnitudes are greater or equal to 0, while all voltage and current phase angles are between 0 and 2π. On the other hand, γ can take any value between zero and the rated STATCOM current.

8.4 Equality Constraints

The solution to the minimization problem must also satisfy certain equality constraints:

$$h_1(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = \vec{V_1} \cdot \vec{I_1} + \vec{V_2} \cdot \vec{I_2} = 0 \quad (8.21)$$

$$h_2(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = \vec{V_1} \cdot \vec{I_0} + \vec{V_1} \cdot \vec{I_2} + \vec{V_2} \cdot \vec{I_0} + \vec{V_2} \cdot \vec{I_1} = 0 \quad (8.22)$$

$$h_3(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = V_1 I_1 sin(\phi_{1,v} - \phi_{1,i}) = C_1 \quad (8.23)$$

$$h_4(I_0, \phi_{0,i}, I_1, \phi_{1,i}, I_2, \phi_{2,i}) = V_2 I_2 sin(\phi_{2,v} - \phi_{2,i}) = C_2 \quad (8.24)$$

Constraint h_1 ensures that the sum of the common mode power terms is zero, constraint h_2 ensures that the sum of the differential mode power terms is zero, constraint h_3 ensures that the required common mode positive sequence reactive power is met, and finally, constraint h_4 ensures that the required (if any) common mode negative sequence reactive power is met.

8.5 Solution of the Problem

Ideally, convex optimization methods would be used to solve the problem above because they ensure that if a minimum is found, it is necessarily a global minimum [7]. However, in order to be able to use convex optimization methods, two important conditions need to be fulfilled. Firstly, the function must be convex. The condition for convexity of a function is that the matrix of its second order partial derivatives (Hessian matrix) must be positive semi-definite. Secondly, the constraints must be linear. It is obvious that the constraints are nonlinear and therefore, without further analysis, it is clear that convex minimization methods cannot be applied. Nonlinear optimization methods must therefore be used in this case.

8.6 Example of Results With and Without the Optimization

In order to illustrate the benefits of this optimization on leg current magnitudes, the problem described above was solved using the *fmincon* function in the *Matlab* optimization toolbox. In this specific example, the positive and negative sequence voltage magnitudes are chosen as:

$$V_1 = \frac{2}{3} \tag{8.25}$$

$$V_2 = \frac{1}{3} \tag{8.26}$$

and the common mode reactive powers in positive and negative sequence are chosen as:

$$Q_{11} = -0.1924 \tag{8.27}$$

$$Q_{22} = 0.0962 \tag{8.28}$$

The angle between the positive sequence and negative sequence voltages is then varied from 0°to 360°by steps of 1°. At every step, the optimization algorithm is run to compute the optimal leg currents. The figure below shows in blue the magnitude of the current in the leg having the highest current when the optimization method is not used. In other words, for the blue curve, equations 8.11 and 8.12 are enforced, leaving no degree of freedom for the optimization of leg currents. The

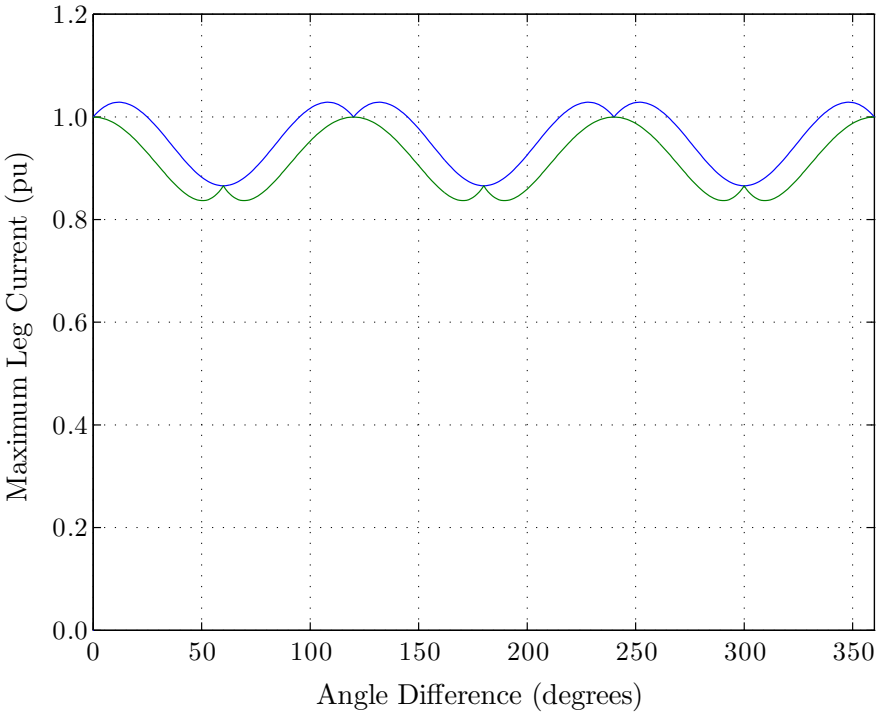

Figure 8–1: Optimization of leg currents using common mode active power flow

green curve is the magnitude of the current in the leg having the highest current

when the optimization method is used. In other words, for the green curve, equation 8.14 was used instead of equations 8.11 and 8.12, leaving a degree of freedom for the optimization of leg currents. The largest difference between the two curves is approximately 7%. Although this is a relatively small difference, this optimization method is a low cost improvement since it does not require any additional components. Indeed, only software changes are required in order to apply this method.

CHAPTER 9
Unbalance Between Cells in a Given Phase

One additional type of unbalance is that which occurs between cells of the same phase. Indeed, even though commom mode and differential mode active power flow can be controlled using the methods explained in the previous chapters, there may still be a drift in cell voltages within a given phase of the converter. This phenomenon may have many causes, some of which are

- Slightly different component values in different cells
- Slightly different losses in different cells
- Small errors in switching time of the IGBTs

In order to correct this drift, it is necessary to exchange energy between cells of the same phase. Selective swapping algorithms such as the one described in [12] and [11] exist in order to re-order the switching patterns of the cell and therefore adjust the time during which each individual cell is charged/discharged. An alternative method is presented in chapter 12 of this thesis, and its effectiveness is demonstrated in chapter 13. The advantage of this method is that it can be implemented in simple logic implemented outside the main controller and therefore does not require centralized control of all cells. This is done by measuring the DC voltage of each cell, and adding to the AC voltage reference for the SPWM of each cell a small voltage component which is in phase with the leg current based on whether the capacitor should be charged or discharged. In fact, this method amounts to creating a small active power flow in/out of the cells that need charging/discharging. Since this is done for all cells at the same time, the situation for the whole leg amounts to an exchange of energy between the cells. The problem

with this method is that it requires a current to flow in the leg. Indeed, it is impossible to exchange energy without having current flow. This means that when the STATCOM is at zero reactive power output, there cannot be an exchange of energy between the cells. However, for the delta-coupled STATCOM or for the wye-coupled STATCOM with neutral current path, even when the net reactive power output of the STATCOM is zero, it is possible to circulate a third harmonic zero sequence current. This third harmonic will not create an active power flow in/out of the phases because the product of a fundamental frequency voltage with a third harmonic current is zero on average. However, if the AC voltage reference of the cells that need charging/discharging is modified to include a small third harmonic voltage in phase with the leg current, active power will flow in/out of the cells with the third harmonic current.

CHAPTER 10
Double Wye-Coupled Chain-Link STATCOM with Half-Bridge Cells

The double-wye coupled STATCOM topology presented in this chapter relies on the use of half-bridge cells rather than full-bridge cells as for the topologies presented in the previous chapters. Since a half-bridge can only have 2 switching states, its output voltage can only be 0 or V_{DC}. For this reason, two converters are necessary in order to operate over the full range of the ac voltage waveform. A double wye coupled chain-link STATCOM with half-bridge cells is shown in figure 10–1. The upper and lower converters have leg voltages with identical AC components, and DC components of equal magnitude but opposite polarity. The upper and lower converters also supply identical AC currents. The major advantage of the double-wye STATCOM resides in the fact that the flow of active power created by unbalanced operation can be cancelled with DC currents. Indeed, expressing the voltages of the upper and lower converter legs:

$$\vec{V}_U = \vec{V}_1 \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{V}_2 \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} + \frac{V_{DC}}{2} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{10.1}$$

$$\vec{V}_L = \vec{V}_1 \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{V}_2 \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} - \frac{V_{DC}}{2} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{10.2}$$

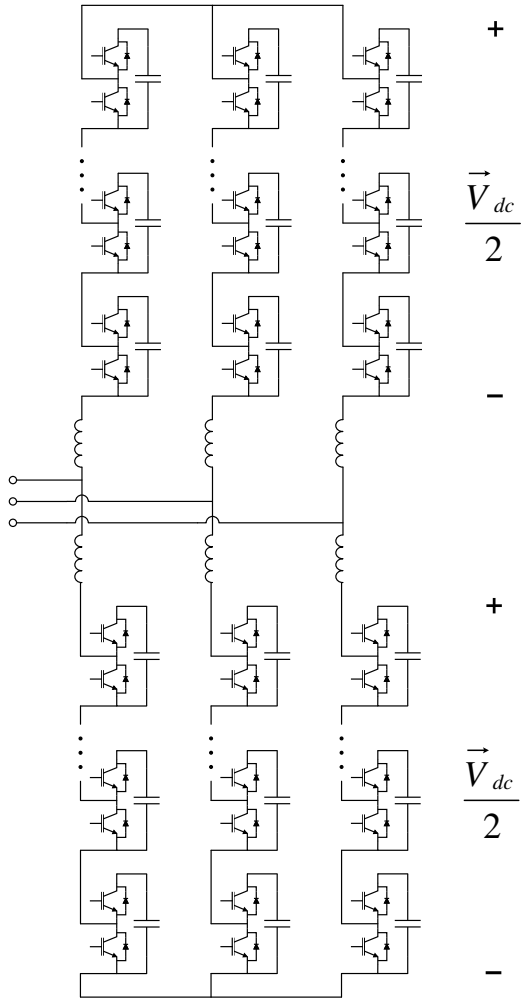

Figure 10–1: Un-grounded Double Wye-Coupled Chain-Link STATCOM

In normal operation, the upper and lower converters share the total ac converter current equally. The leg currents can therefore be expressed as:

$$\vec{I}_U = \vec{I}_L = \vec{I}_1 \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{I}_2 \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} \tag{10.3}$$

As before, the common mode active power flow can be chosen to be zero by ensuring that the voltages and currents of the same sequence are orthogonal to each

other. The unbalanced active power in the upper and lower converters can then be calculated as follows:

$$\vec{P}_U = Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \vec{V}_2\vec{I}_1^*\begin{bmatrix}1\\a^2\\a\end{bmatrix} + \frac{V_{DC}}{2}\vec{I}_1^*\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \frac{V_{DC}}{2}\vec{I}_2^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{10.4}$$

$$\vec{P}_L = Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \vec{V}_2\vec{I}_1^*\begin{bmatrix}1\\a^2\\a\end{bmatrix} - \frac{V_{DC}}{2}\vec{I}_1^*\begin{bmatrix}1\\a\\a^2\end{bmatrix} - \frac{V_{DC}}{2}\vec{I}_2^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{10.5}$$

Note that the three rows of 10.4 and 10.5 represent the sums of the terms resulting in unbalanced active power flow in each of the three phases. The product of DC voltages with AC currents give an average value of zero. In other words, they represent pulsating power and do not contribute to the net active power flow in or out of the legs. Therefore, the only terms contributing to a net flow of active power are the same for the upper and lower converters and are:

$$\vec{P}_U = \vec{P}_L = Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix}1\\a\\a^2\end{bmatrix} + \vec{V}_2\vec{I}_1^*\begin{bmatrix}1\\a^2\\a\end{bmatrix}\right) \tag{10.6}$$

The idea is then to choose a DC current that will give a product with the DC voltage that couteracts the active power flow caused by the unbalanced operating conditions. Since the DC voltages of the upper and lower converters are of the same magnitude but of opposite polarity, and since the unbalanced active power flows are equal, a DC current of same amplitude but of opposite polarity is needed

in the upper and lower converter legs of the same phase in order to correct the situation. Also, because these DC currents are used only to correct the differential active power flow terms, the sum of the DC currents in all three phases needs to be zero. These two conditions ensure that no DC current flows out of the converter and into the grid. The DC currents in the upper converter are therefore defined by setting the following equality:

$$\frac{V_{DC}}{2}\begin{bmatrix} I_{DC,a} \\ I_{DC,b} \\ I_{DC,c} \end{bmatrix} = -Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} + \vec{V}_2\vec{I}_1^*\begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix}\right) \tag{10.7}$$

and the DC currents are simply

$$\begin{bmatrix} I_{DC,a} \\ I_{DC,b} \\ I_{DC,c} \end{bmatrix} = -\frac{2}{V_{DC}}Re\left(\vec{V}_1\vec{I}_2^*\begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} + \vec{V}_2\vec{I}_1^*\begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix}\right) \tag{10.8}$$

As described previously, the DC currents in the lower converter are then the negative of the currents defined in equation 10.8 for the corresponding phases.

This method has the major advantage that the balancing is done solely by DC quantities without interfering with the AC quantities. It is however possible to combine the DC current method described above with one or more of the zero sequence methods defined in the previous chapters in order to reduce leg voltages and currents. Indeed, in a manner similar to the one presented in chapter 7, the zero sequence voltage method can be applied to both the upper and lower converters up to the point where the leg voltage rating is met. The remaining differential active power flow can then be cancelled by using the DC current method. The first step for this method is to calculate the zero sequence voltage that would be necessary to cancel the differential active power flow if only this method was used.

The individual AC phase to neutral voltages (where the neutral is the neutral point of each wye-coupled STATCOM) can then be written as:

$$\vec{V_a} = 1V_0e^{(j\phi_0)} + 1V_1e^{(j\phi_1)} + 1V_2e^{(j\phi_2)} \tag{10.9}$$

$$\vec{V_b} = 1V_0e^{(j\phi_0)} + a^2V_1e^{(j\phi_1)} + aV_2e^{(j\phi_2)} \tag{10.10}$$

$$\vec{V_c} = 1V_0e^{(j\phi_0)} + aV_1e^{(j\phi_1)} + a^2V_2e^{(j\phi_2)} \tag{10.11}$$

The inequality condition is then solved for each phase. For example, the inequality condition for phase a is:

$$\|\vec{V_a}\| = \|V_0e^{(j\phi_0)} + V_1e^{(j\phi_1)} + V_2e^{(j\phi_2)}\| \leq V_{max} \tag{10.12}$$

Solving for the amplitude of $\vec{V_0}$:

$$\begin{aligned} V_0 \leq & -\left(V_1cos(\phi_0 - \phi_1) + V_2cos(\phi_0 - \phi_2)\right) \\ & \pm \sqrt{\left(V_1cos(\phi_0 - \phi_1) + V_2cos(\phi_0 - \phi_2)\right)^2 - \left(V_1^2 + V_2^2 + 2V_1V_2cos(\phi_1 - \phi_2) - V_{max}^2\right)} \end{aligned} \tag{10.13}$$

Negative solutions for V_0 are then discarded since the angle of $\vec{V_0}$ has already been defined. The smallest solution from all three phases is taken as the largest allowed V_0. Finally, the remaining unbalance is cancelled by the DC current method which gives the following currents in the upper converter:

$$\begin{bmatrix} I_{DC,a} \\ I_{DC,b} \\ I_{DC,c} \end{bmatrix} = \frac{-2}{V_{DC}} Re \left(\vec{V_1}\vec{I_2^*} \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} + \vec{V_2}\vec{I_1^*} \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{V_0}\vec{I_1^*} \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} + \vec{V_0}\vec{I_2^*} \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} \right) \tag{10.14}$$

The DC currents found with equation 10.14 are necessarily lower or equal to the DC currents that would be needed if that method was used without the zero sequence voltage method.

If the converter has a neutral path, the zero sequence current method can also be used in a similar way. Indeed, the zero sequence current method can be used to the extent where the leg currents reach a defined limit. The remaining differential active power flow is then cancelled using the DC current method. First, the zero sequence current is computed as if only that method was used. The individual AC phase currents are then:

$$\vec{I_a} = 1I_0e^{(j\phi_0)} + 1I_1e^{(j\phi_1)} + 1I_2e^{(j\phi_2)} \tag{10.15}$$

$$\vec{I_b} = 1I_0e^{(j\phi_0)} + a^2I_1e^{(j\phi_1)} + aI_2e^{(j\phi_2)} \tag{10.16}$$

$$\vec{I_c} = 1I_0e^{(j\phi_0)} + aI_1e^{(j\phi_1)} + a^2I_2e^{(j\phi_2)} \tag{10.17}$$

The inequality condition is then solved for each phase. For example, the inequality condition for phase a is:

$$\|\vec{I_a}\| = \|I_0e^{(j\phi_0)} + I_1e^{(j\phi_1)} + I_2e^{(j\phi_2)}\| \leq I_{max} \tag{10.18}$$

Solving for the amplitude of $\vec{I_0}$:

$$\begin{aligned} I_0 \leq & -\left(I_1cos(\phi_0 - \phi_1) + I_2cos(\phi_0 - \phi_2)\right) \\ & \pm \sqrt{\left(I_1cos(\phi_0 - \phi_1) + I_2cos(\phi_0 - \phi_2)\right)^2 - (I_1^2 + I_2^2 + 2I_1I_2cos(\phi_1 - \phi_2) - I_{max}^2)} \end{aligned} \tag{10.19}$$

Negative solutions for I_0 are discarded since the angle of $\vec{I_0}$ has already been defined. The smallest solution from all three phases is taken as the largest allowed I_0. Finally, the remaining unbalance is cancelled by the DC current method which

gives the following currents in the upper converter:

$$\begin{bmatrix} I_{DC,a} \\ I_{DC,b} \\ I_{DC,c} \end{bmatrix} = \frac{-2}{V_{DC}} Re \left(\vec{V}_1 \vec{I}_2^* \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} + \vec{V}_2 \vec{I}_1^* \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{V}_1 \vec{I}_0^* \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} + \vec{V}_2 \vec{I}_0^* \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} \right) \tag{10.20}$$

The DC currents found with equation 10.20 are necessarily lower or equal to the DC currents that would be needed if that method was used without the zero sequence current method. As discussed in chapter 7, the neutral path impedance has in fact a non-zero impedance. This results in the fact that a zero sequence current would create a zero sequence voltage drop along the neutral path. The methods defined in chapter 7 for a STATCOM with a fixed or variable neutral path impedance should therefore be used. In that case, the leg voltage limits and the leg current limits should then be checked simultaneously in order to find the necessary DC currents.

It must be noted that if the purpose of using the zero sequence current method is to reduce the necessary DC current, little gain is made since this hardly reduces the total necessary leg current. One use of this method can however be to reduce the leg voltage. Indeed, assuming one of the legs has a high voltage due to the unbalanced network voltages, the zero-sequence current can be used to generate a zero sequence voltage which reduces the total voltage in that particular phase. This will most likely result in a larger differential active power flow, which can however still be cancelled by the DC current method. The zero sequence voltage method can also be directly used in this way.

CHAPTER 11
Comparison of Chain-Link STATCOM Topologies

The delta coupled STATCOM presented in chapter 5, the ungrounded wye-coupled STATCOM presented in chapter 6, the grounded wye-coupled STATCOM presented in chapter 7 and the double-wye STATCOM with or without neutral path presented in chapter 10 can be compared based on operating range, complexity and cost in order to define the strengths and weaknesses of each one. The comparison of operating ranges is done using phasor diagrams. These diagrams show phase voltages and STATCOM currents during certain faults and STATCOM operating conditions. The intent is to show the limitations of different STATCOM topologies by illustrating that for certain faults and operating conditions, a given STATCOM topology may not be able to produce the required zero sequence voltage or zero sequence current necessary to keep the DC capacitor voltages balanced. It will be shown that these limitations are different for each STATCOM topology, and occur during different operating conditions. The faults discussed here are explained in appendix C, and are summarized in table C–1. In order to facilitate the reader's understanding of the phasor diagrams presented in this chapter, the following convention will be used. This convention is also illustrated in figure 11–1.

The phase voltages and leg currents are thick vectors, and the current phasors are a darker shade of the same color as the phase voltages. The thinner dashed vectors of a given color are the positive and negative sequence components of the phase quantity of the same color. The thick black vector is the zero sequence component of either phase voltages or leg currents depending on which converter topology (and therefore which control method) is used in the case which is shown in

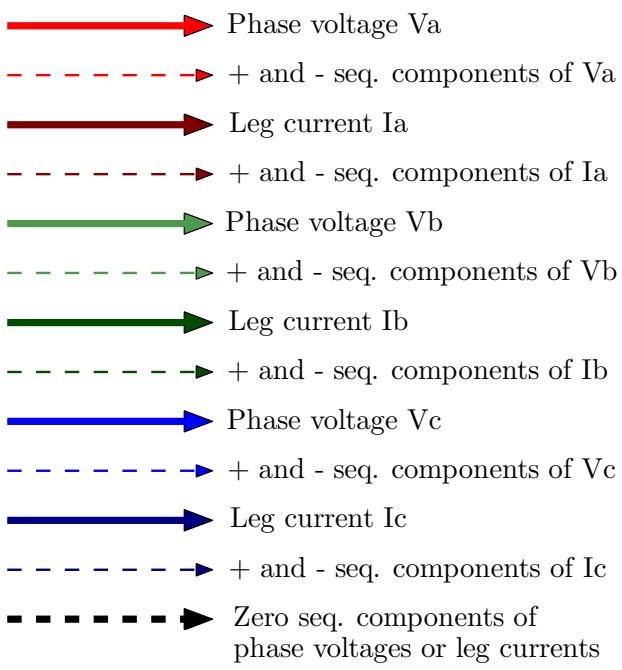

Figure 11–1: Legend for interpreting phasor diagrams

the phasor diagram. Note that the positive, negative and zero sequence components are added vectorially to construct the phase quantities.

11.1 Delta-Coupled STATCOM

It must be noted that for the delta-coupled converter, it may not be possible for the STATCOM to supply both the desired common mode positive sequence reactive power and the desired common mode negative sequence reactive power during certain unbalanced conditions while simultaneously controlling the DC capacitor voltages. For example, referring to table C–1, if the positive sequence voltage and the negative sequence voltage have the same amplitude as is the case for a phase to phase fault, a zero sequence current with an infinite magnitude is necessary to ensure that no unbalanced active power flows. As derived in appendix C and summarized in table C–1, the symmetrical components of the network voltage

during a bolted phase to phase fault at the STATCOM busbar between phases b and c are:

$$\vec{V_0} = 0.5V\angle 0 \tag{11.1}$$

$$\vec{V_1} = 0.5V\angle 0 \tag{11.2}$$

$$\vec{V_2} = 0 \tag{11.3}$$

where V is the positive sequence voltage of the healthy network. Figure 11–2 shows

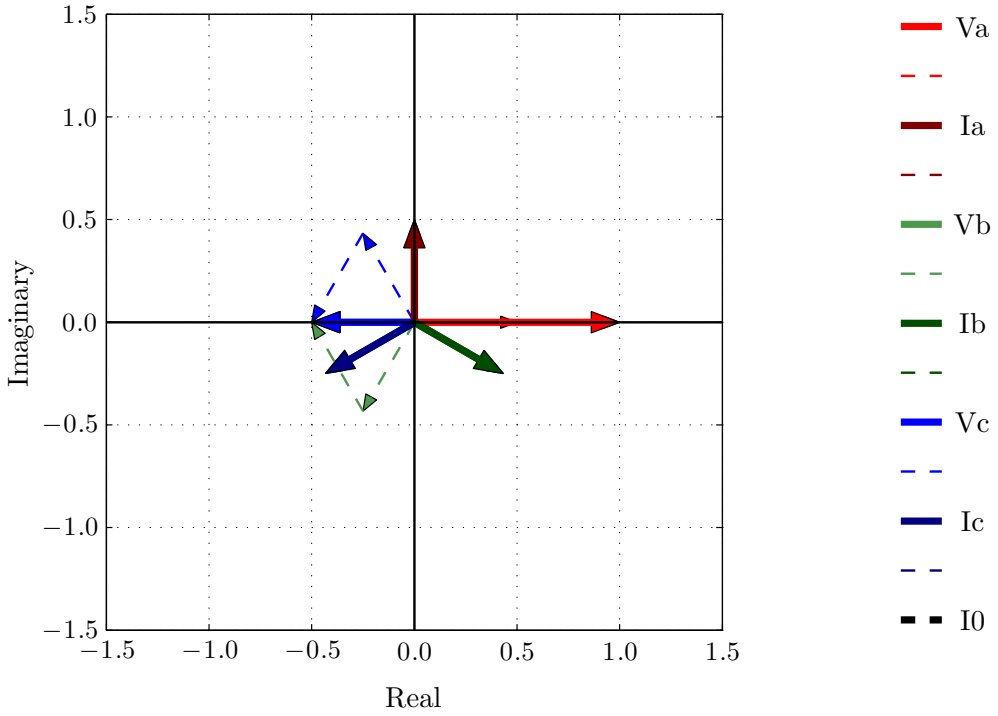

Figure 11–2: Phase Voltages and Positive Sequence Leg Currents in a Delta-Coupled STATCOM During a Phase to Phase Fault

the voltages appearing across the STATCOM legs as well as, for example, a positive sequence capacitive leg current of $0.5\angle 0$ which the STATCOM could be required to supply during the fault. It is clear from this figure that unbalanced active power will flow since not all three currents are in quadrature with their respective

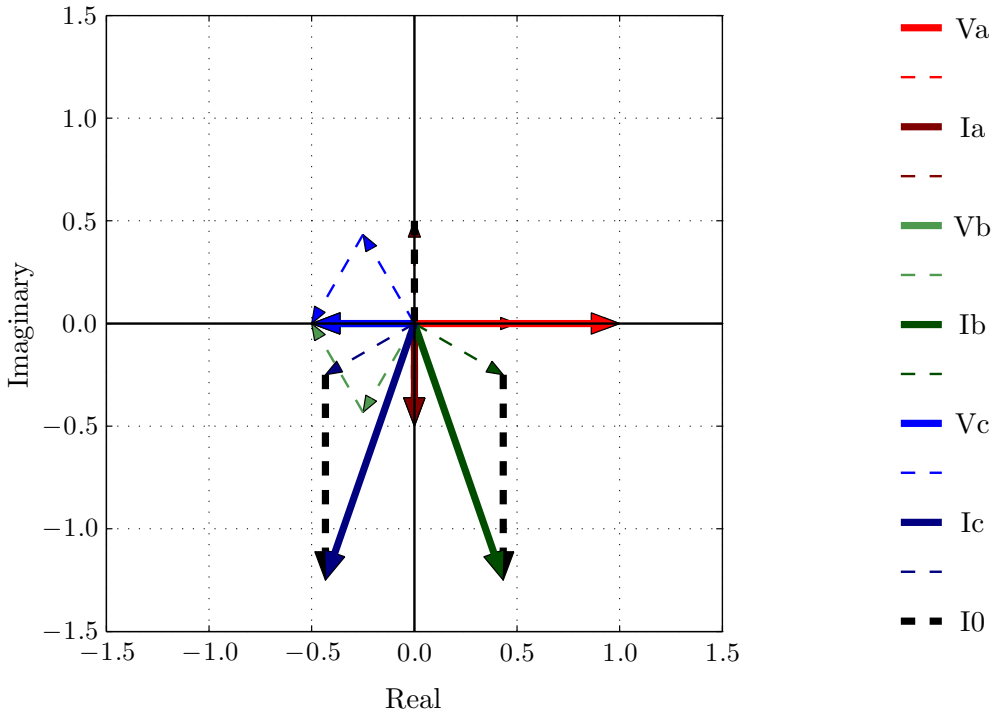

Figure 11–3: Phase Voltages and Positive Sequence Leg Currents in a Delta-Coupled STATCOM During a Phase to Phase Fault with Zero Sequence Current Injection

voltages. Trying to balance the active power flow only by using a zero sequence current results in the need for an infinite zero sequence current. This is illustrated in figure 11–3 where a 1pu component of zero sequence current is shown in black. Although it helps in balancing the active power flow, it is clearly insufficient. Since preventing an unbalance in DC capacitor voltages is essential, another constraint needs to be relaxed because it is obvious that such a large zero sequence current cannot be allowed to flow.

It is interesting to note that the ungrounded wye-coupled STATCOM could cope with this situation. Indeed, as shown in figure 11–4, a finite zero sequence voltage can be found which ensures that the leg currents and voltages are in quadrature with each other thus cancelling all active power flow. Also, from a cost perspec-

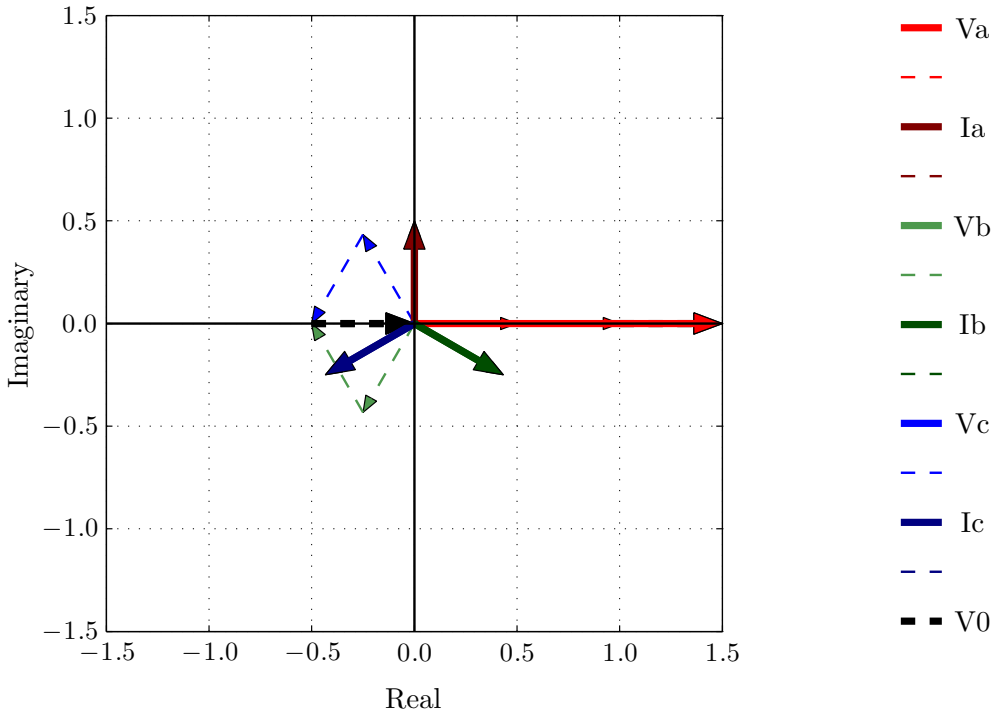

Figure 11–4: Phase Voltages and Positive Sequence Leg Currents in a Wye-Coupled STATCOM During a Phase to Phase Fault with Zero Sequence Voltage Injection

tive, the leg voltages are a factor $\sqrt{3}$ higher than for the wye coupled converter, therefore more series connected cells are needed.

11.2 Ungrounded Wye-Coupled STATCOM

In the same manner, the wye-coupled converter also has certain limitations. Stating the problem differently, it may not be possible for the STATCOM to supply both the desired common mode positive sequence currents and the desired common mode negative sequence currents during certain unbalanced conditions while simultaneously controlling the DC capacitor voltages. For example, if the positive sequence current and the negative sequence current have the same amplitude and phase, a zero sequence voltage with an infinite magnitude is necessary to ensure that no unbalanced active power flows. To illustrate this example, the STATCOM

could be required to supply the following currents

$$\vec{I_1} = 0.5\angle\frac{\pi}{2} \tag{11.4}$$

$$\vec{I_2} = 0.5\angle\frac{\pi}{2} \tag{11.5}$$

while the positive sequence network voltage is $1V\angle 0$. This case does not correspond to a specific fault case but could occur if, for example, the STATCOM was used to compensate for an unbalanced load. Figure 11–5 shows the voltages appearing across the STATCOM legs as well as a leg currents which the STATCOM should supply in this case.The current phasors are a darker shade of the same color as the

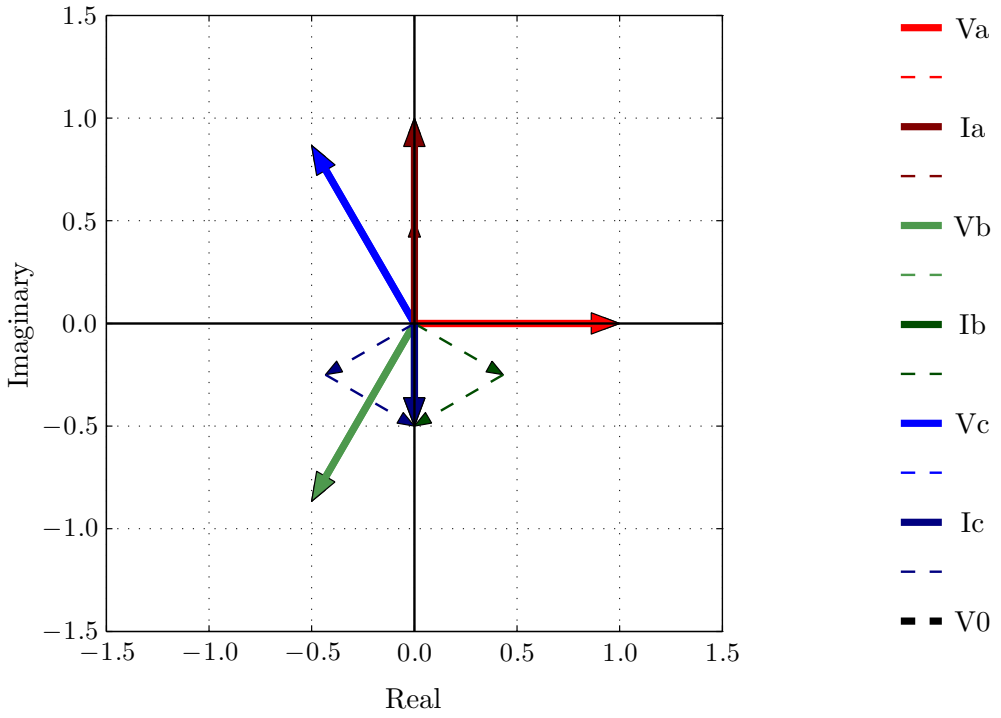

Figure 11–5: Positive Sequence Phase Voltages and Unbalanced Leg Currents in a Wye-Coupled STATCOM

phase voltages. It is clear from this figure that unbalanced active power will flow since not all three currents are in quadrature with their respective voltages. Trying to balance the active power flow only by using a zero sequence voltage results in

the need for an infinite zero sequence voltage. This is illustrated in figure 11–6 where a 1pu component of zero sequence voltage is shown in black. Although it helps in balancing the active power flow, it is clearly insufficient. Since preventing

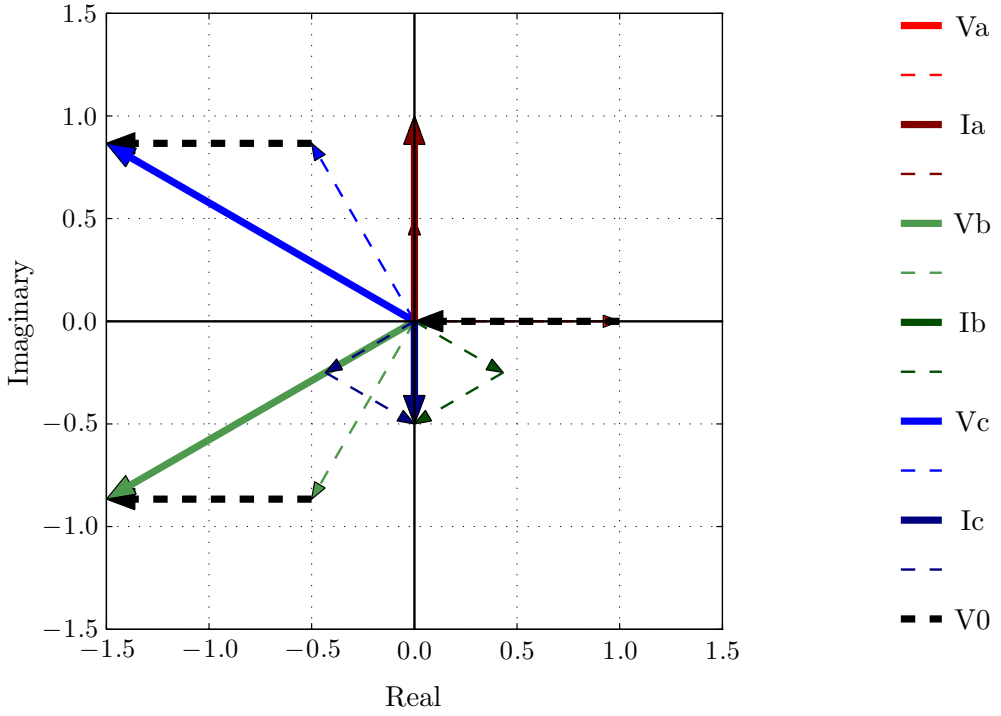

Figure 11–6: Positive Sequence Phase Voltages and Unbalanced Leg Currents in a Wye-Coupled STATCOM with Zero Sequence Voltage Injection

an unbalance in DC capacitor voltages is essential, another constraint needs to be relaxed because it is obvious that such a large zero sequence current cannot be allowed to flow. It is interesting to note that the delta-coupled STATCOM could cope with this situation. Indeed, as shown in figure 11–7, a finite zero sequence current can be found which ensures that the leg currents and voltages are in quadrature with each other thus cancelling all active power flow. Also, from a cost perspective, the leg currents are a factor $\sqrt{3}$ higher than for the delta coupled converter, therefore more parallel connected cells are needed.

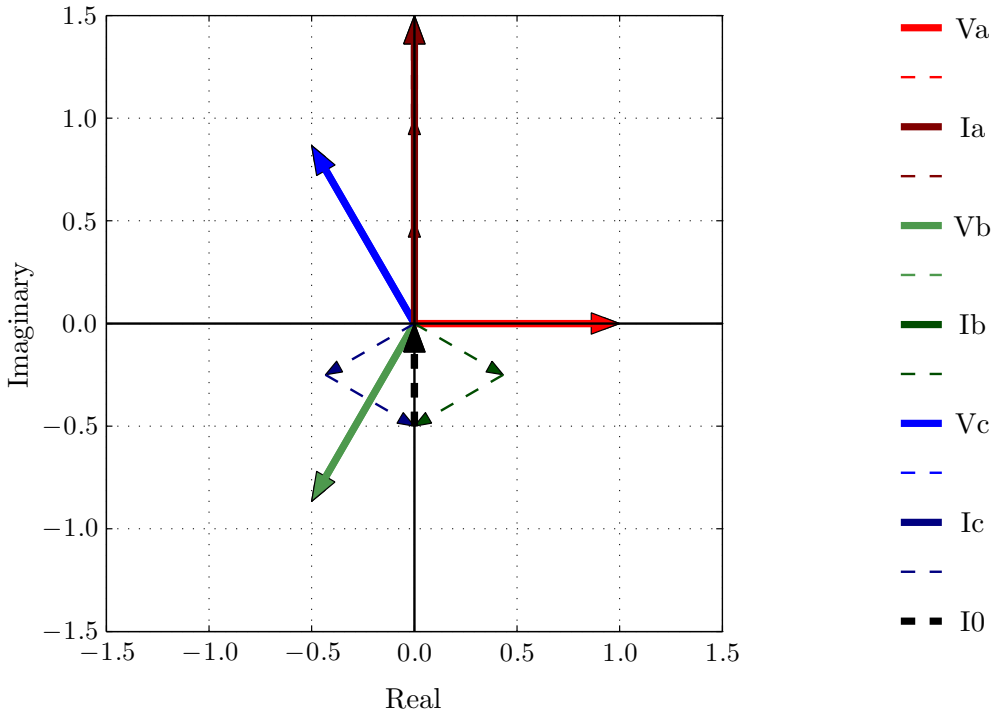

Figure 11–7: Positive Sequence Phase Voltages and Unbalanced Leg Currents in a Delta-Coupled STATCOM with Zero Sequence Current Injection

11.3 Grounded Wye-Coupled STATCOM

As described in chapter 7 the grounded wye-coupled STATCOM has a non-zero neutral path impedance, and therefore, both the zero sequence current and the zero sequence voltage methods can be used to balance the differential mode active power flow. If a fixed impedance is used, its value must be chosen carefully in order to coordinate with the desired contributions of each zero sequence quantities. If a variable impedance is used, the neutral path impedance can vary from an open-circuit where the zero sequence voltage method can be utilized alone, to a low impedance grounding path where mainly the zero sequence current method can be utilized. In this case, the STATCOM becomes more flexible in the sense that it can cope with both of the situations presented sections 11.1 and 11.2. This additional flexibility however comes at the cost of a variable impedance in the neutral path.

11.4 Double Wye-Coupled STATCOM

The double wye-coupled STATCOM has as much flexibility as the grounded wye coupled STATCOM with a variable neutral path impedance since there always exist finite DC currents which will cancel the differential mode active power flow. Furthermore, the zero sequence methods can also be used to optimize the leg currents and voltages. The cost of this converter is slightly higher than the cost for a same size single wye-coupled converter. Indeed, the number of semiconductor devices in this topology is the same as for a single wye-coupled due to the fact that half-bridge cells are used instead of full H-bridge cells. The number of DC capacitors is doubled, but the size of each capacitor is half of the capacitors in the single wye-coupled converter for a given STATCOM size.

11.5 Summary of STATCOM Topology Comparison

The following table summarizes the comparison of STATCOM topologies described in this chapter.

Table 11–1: Summary of STATCOM topology comparison

Topology	Operating Range	Complexity	Cost
Delta	Limited when $\vec{V}_1$ and $\vec{V}_2$ are in phase and of equal amplitude	Low	High due to rating for ph-ph voltage
Ungrounded Wye	Limited when $\vec{I}_1$ and $\vec{I}_2$ are in phase and of equal amplitude	Low	Low due to rating for ph-g voltage
Grounded Wye	Not limited by specific operating conditions	High due to variable impedance	High due to variable impedance
Double Wye	Not limited by specific operating conditions	High due to double wye	Low (assuming a large STATCOM)

CHAPTER 12
Implementation of Control Strategies in Matlab/Simulink

A simple STATCOM model was implemented in *Matlab/Simulink* for each of the topologies presented in order to test the control strategies that were developed. Due to the fact that the modeling is very similar for all topologies, only the wye-coupled STATCOM is shown in details.

12.1 Converter Modeling

The test circuit used is shown in figure 12–1. The network model is a simple

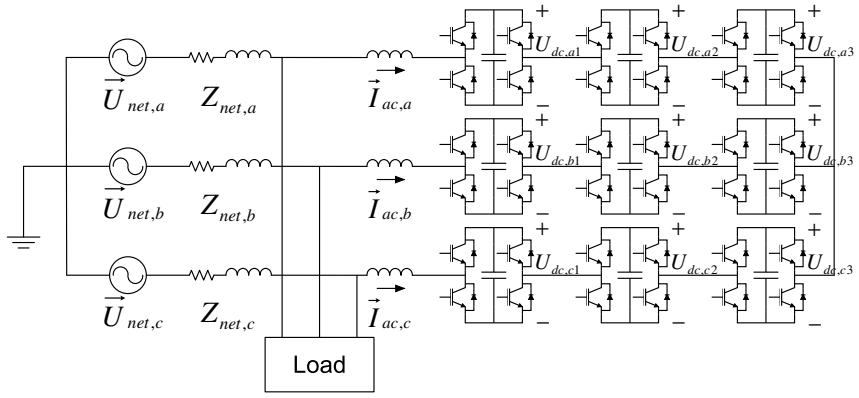

Figure 12–1: Test circuit used in *Matlab/Simulink* simulations

grounded network with an R-L Thevenin impedance. The load is resistive, and enables dynamic changes in active power absorption as well as unbalance. Finally, the STATCOM is wye-coupled with a floating neutral. It has three cells per phase which is sufficient to demonstrate the efficiency of the DC capacitor unbalance correction. In order to accelerate simulation time, and to avoid complicating the model unnecessarily, each converter cell is replaced by a controllable voltage source as shown in figure 12–2. This simplification is acceptable because the purpose is

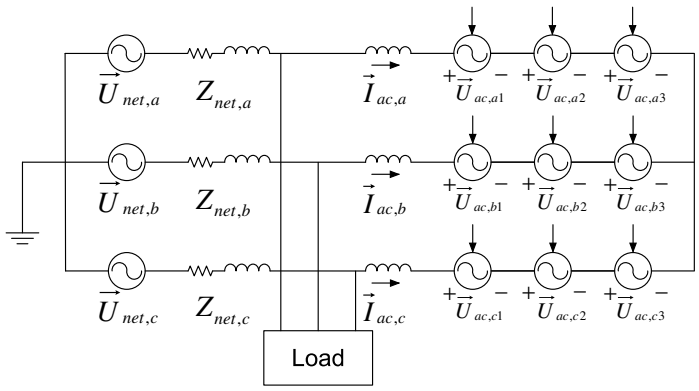

Figure 12–2: Simplified test circuit used in *Matlab/Simulink* simulations

not to model the actual switching of the cells, but rather to test the DC capacitor voltage balancing algorithms. Of course, in order to do this, the dynamics of the DC capacitors must be modeled. Figure 12–3 shows how this is achieved. Figures 12–3a

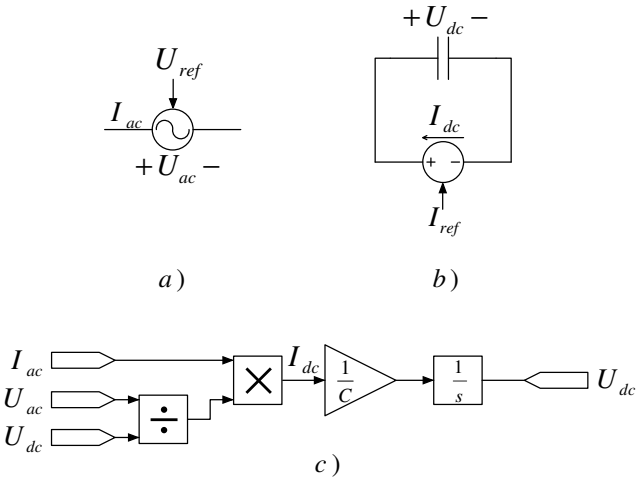

Figure 12–3: Modeling of converter cells as controllable voltage sources

and 12–3b show the AC and DC dynamics respectively. The voltages and currents from each of these circuits are related according to equation 12.1.

$$I_{dc} = \frac{I_{ac} \cdot U_{ac}}{U_{dc}} \tag{12.1}$$

This is essentially saying that there is conservation of power between the AC side and the DC side of the cell. Furthermore, a capacitor has a transfer function of the form:

$$\frac{v(s)}{i(s)} = z(s) = \frac{1}{sC} \tag{12.2}$$

Equations 12.1 and 12.2 are then implemented as shown in figure 12–3c. A more elaborate model of the cell also includes losses. These can be modeled by using a resistor R_p in parallel with the ideal capacitor, and a series resistor R_s. In this case, the transfer function becomes:

$$\frac{v(s)}{i(s)} = z(s) = \frac{R_p}{sCR_p + 1} + R_s \tag{12.3}$$

The behaviour of such a cell model is close to the behaviour of a cell model with switching elements. The main difference is that the high order harmonics caused by the PWM are not modeled. This has little impact on the behaviour of the DC voltage balancing algorithms, and the simplification is therefore acceptable. For a real converter cell, the reference voltage computed by the controller would normally be used in the PWM process as described in chapter 3. In the case of the simplified cell models described above, the reference is directly applied as the input to the controllable voltage source.

12.2 STATCOM Controls

The positive sequence voltage control loop described in figure 2–3 is implemented, and a negative sequence voltage control loop is added. This results in the controls presented in figure 12–4. The inputs from the various DC voltage controllers are also shown in figure 12–4. Each of these controllers will be presented in the following sections.

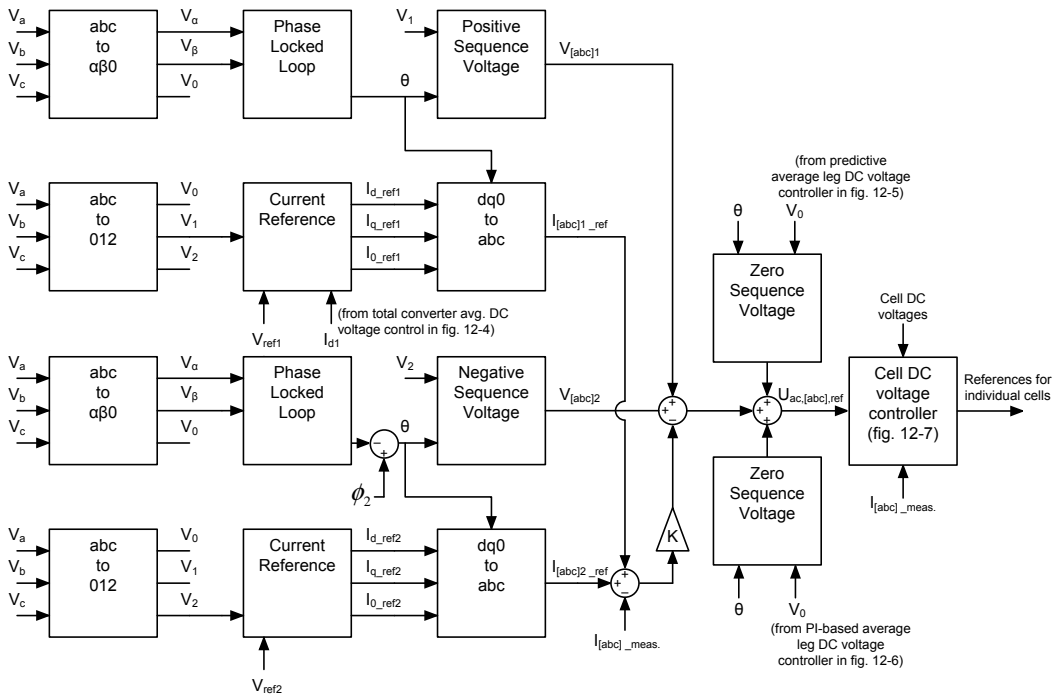

Figure 12–4: Full controls of the STATCOM

12.3 DC Voltage Controls

The DC capacitor voltage balancing is then implemented in three separate control loops. The first control loop regulates the average voltage of all cells in the converter, the second loop regulates the average voltage of all cells in each leg, and the third control regulates the voltage in each cell. These nested control loops are more efficient than having only localized DC voltage correction in each cell. The reason is that these localized methods rely on the detection of an error in DC voltage. The first and third control loops operate on a similar principle; acting on an error measurement. The second control loop however, relies on measured network voltages and STATCOM currents in order to anticipate DC voltage drift caused by unbalanced operation. This method anticipates the error and take corrective measures in order to prevent it. This is therefore much faster and efficient than methods which rely on the detection of an error.

12.3.1 Total Converter Average DC Voltage

The first control loop takes the sum of all DC voltages and controls it to a reference with the use of a proportional-integral (PI) controller. The implementation of this control loop is shown in figure 12–5. Note that the sum of all DC voltages ($U_{dc,conv}$) is computed in figure 12–7. The output of this controller is a

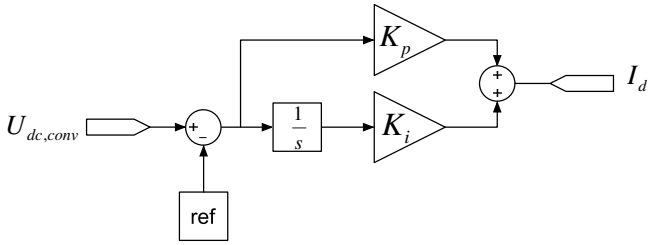

Figure 12–5: Control loop for total converter average DC voltage

direct component of positive sequence leg current which is added to the current reference of the STATCOM. As described in chapter 4, the common mode flow of active power created by the direct current component charges evenly the entire STATCOM.

12.3.2 Converter Leg Average DC Voltage

The second control loop acts on the sum of all DC voltages in each converter leg. It is actually implemented as two different controllers. The first one is a predictive control which implements the zero sequence method developed in chapter 6. Figure 12–6 shows the implementation of this controller. The output of this controller is a zero sequence voltage which is then added to the converter AC voltage reference for each STATCOM leg. This reference is the one that each MMC based converter leg will follow. The summation of the converter AC voltage reference and the zero sequence voltage is shown as the last summation on the right of the control diagram shown in figure 12–4. This ensures that the converter legs do not absorb differential mode active power during unbalanced conditions. This controller acts

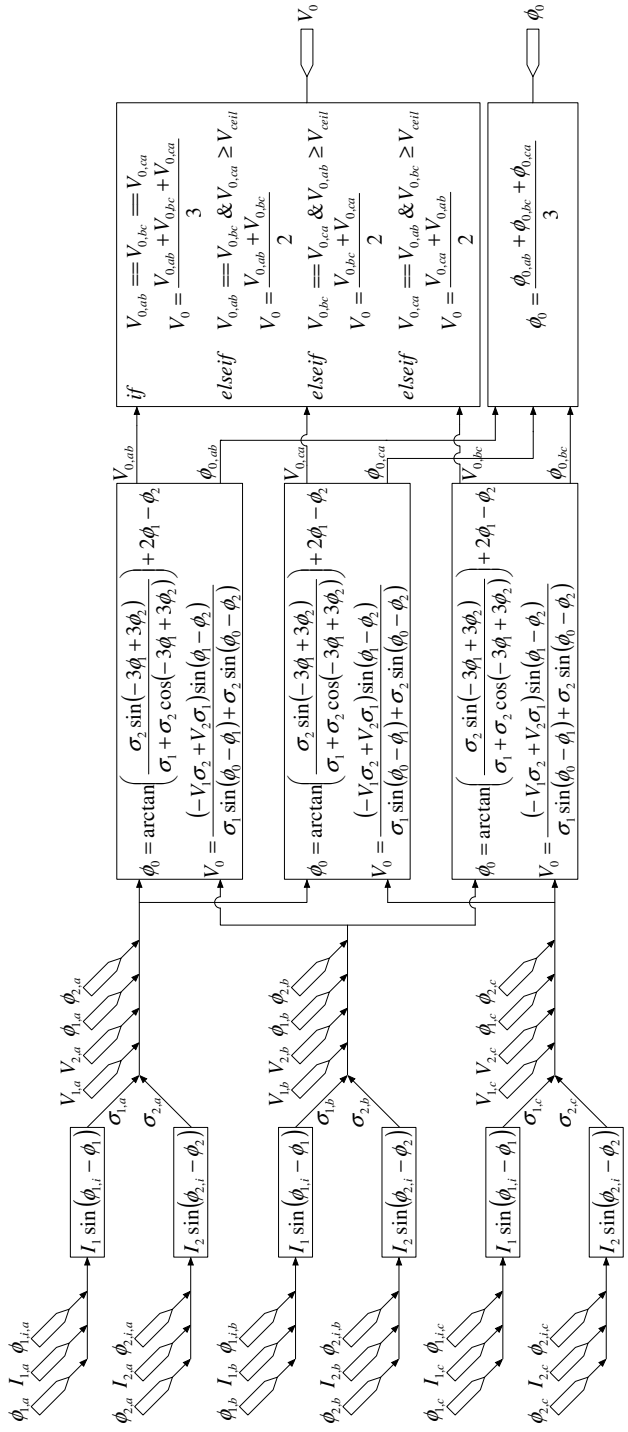

Figure 12–6: Predictive control loop for converter leg average DC voltage

instantaneously, but it leaves a steady-state error due to the time delay inherent to the voltage measurement as well as the measurement error. A second controller is

therefore necessary in order to get rid of this error. The second controller is similar to the one regulating the total converter average DC voltage. Indeed, it takes the sum of all DC voltages in each leg and controls it to a reference with the use of a PI controller. The reference is defined as the average of total leg DC voltages. In other words, this controller can only correct unbalance between converter leg voltages. Therefore, it is independent from the total converter average DC voltage controller. Figure 12–7 shows the implementation. The output of this controller

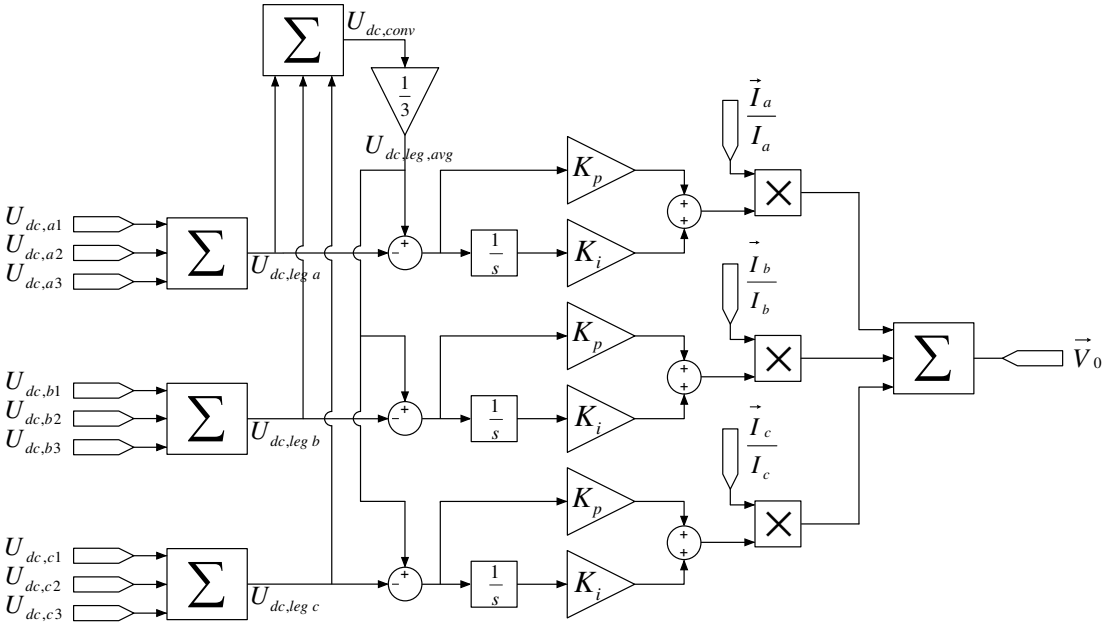

Figure 12–7: PI control loop for converter leg average DC voltage

is a zero sequence voltage which is also added to the converter voltage reference. One may expect that having two different controllers acting on the same quantity might have some adverse effects. It must however be noted that these two controllers have different purposes and act differently. The predictive controller acts instantaneously only when unbalanced operation of the STATCOM is causing a flow of differential mode active power, thus preventing converter leg voltage unbalance. The PI controller acts on the converter leg voltage unbalance and is oblivious

to the unbalanced operation of the STATCOM. Furthermore, the gains of the PI controller are tuned such that its dynamics are slow.

12.3.3 Converter Cell Voltage

The third control loop acts on the individual cell voltages. It compares the voltage in each cell to the average of all cell voltages in that leg. It measures the instantaneous polarity of the leg current, and adds an offset to the ac voltage reference of each cell which is proportional to the DC voltage error in that cell. The polarity of the offset changes with the instantaneous polarity of the current. In essence, this method amounts to adding a direct current reference for each individual cell. Figure 12–8 shows the implementation of this controller for the cells in the leg of phase a. Note that the sum of all DC voltages in leg a ($U_{dc,leg\,a}$) is computed

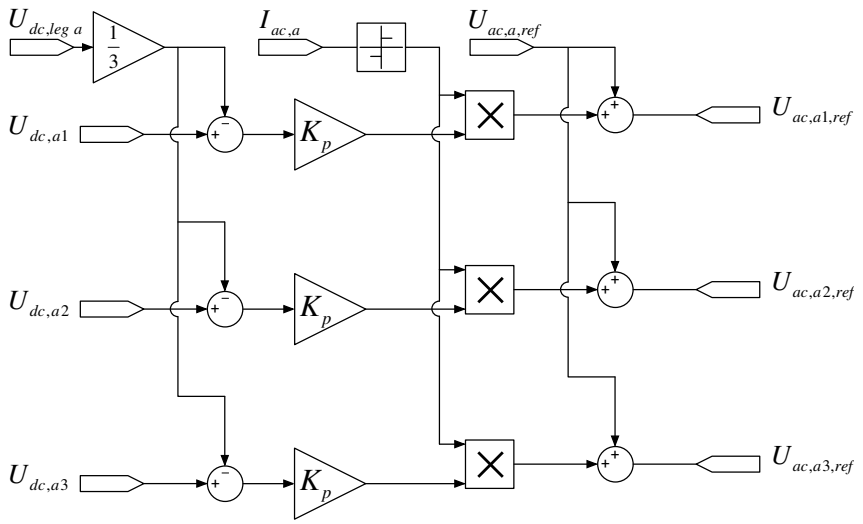

Figure 12–8: Control loop for converter cell voltage (phase a)

in figure 12–7. The advantage of this method is that it can be implemented by simple logic located outside the main controller. Due to the fact that this method basically reduces the spread in cell voltages with respect to the average in a given

leg, it does not change this average value. This controller is therefore independent from the two other controllers.

The efficiency of the controllers presented in this chapter was tested by simulation. The controls were first tested as a whole system, and then each DC voltage controller was tested individually. The results are presented in the next chapter.

CHAPTER 13
Simulation Results

In order to demonstrate the efficiency of the DC voltage control method, different scenarios are simulated. The simulations presented in this chapter are done with the wye-coupled MMC based STATCOM with floating neutral, and the controls used are those developed in chapter 6 and implemented in chapter 12.

Firstly, in order to have a reference case, a fault is simulated while the STATCOM is not active. The AC voltage is therefore not regulated. Then, the same fault is simulated while the STATCOM is active and regulates the AC voltage. The DC voltage controls are however not active. This shows how the cell voltages drift during the fault. Finally, the same fault case is simulated again. This time, the DC voltage controls are active, and the result is that the cell voltages do not drift during the fault.

In the last sections of this chapter, the individual control loops shown in chapter 12 are disabled one after the other to show their effect on the cell voltages.

13.1 Phase to Phase Fault with no STATCOM

In order to have a base case to compare other simulations with, a phase to phase fault is applied between phases B and C while the STATCOM is not in operation. Phase to phase faults are generally less common than phase to ground faults. Nevertheless, this type of fault was chosen because in the model described in chapter 12, the coupling transformer was not modeled. If a WYE-delta coupling transformer is used, a phase to ground fault on the primary of the transfomer is seen as a phase to phase fault on the secondary. Figure 13–1 shows the sequence voltages across the STATCOM legs resulting from this simulation.

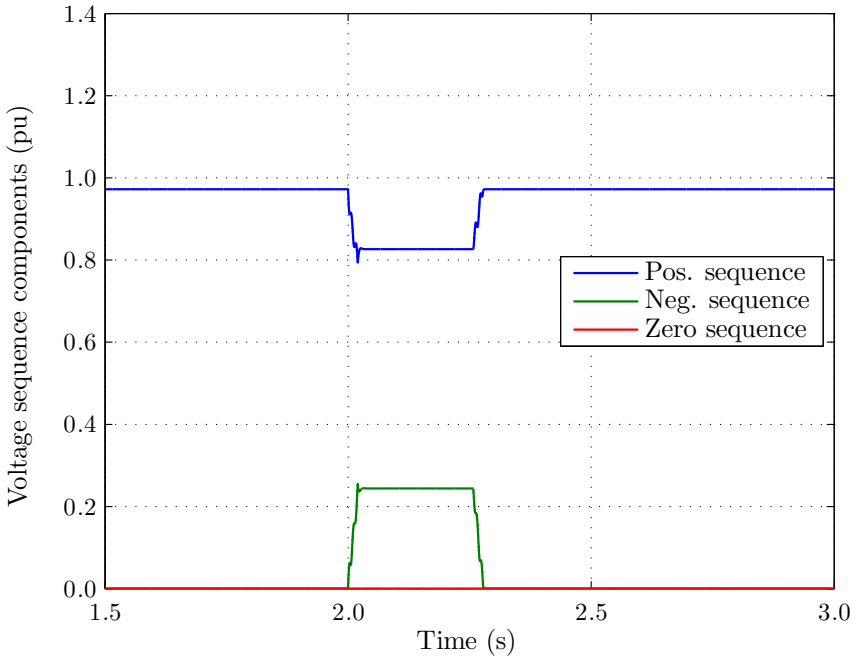

Figure 13–1: Sequence voltages (STATCOM inactive)

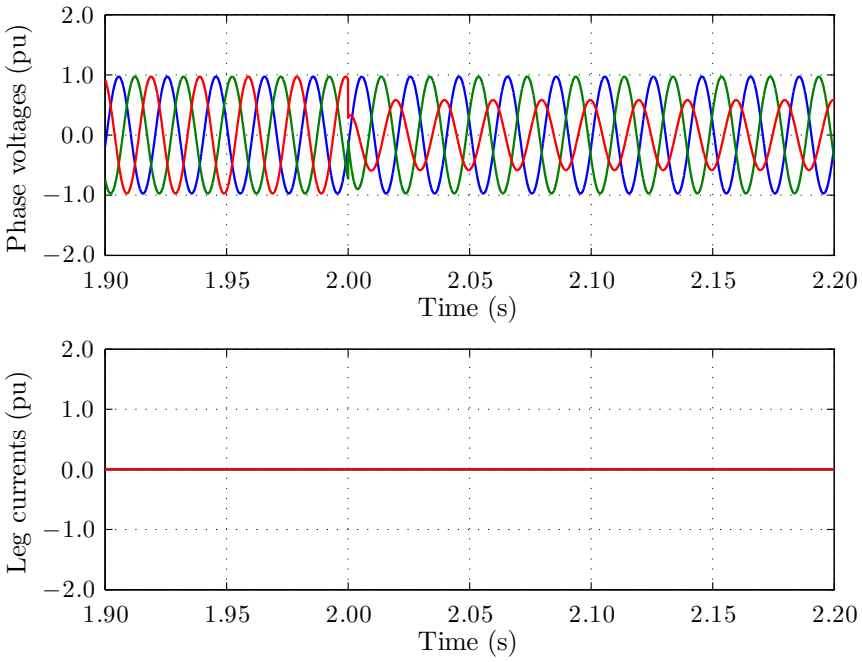

Figure 13–2: Phase voltages and currents (STATCOM inactive)

Before the fault is applied, the load is balanced, and results in a positive sequence voltage at the point of common coupling of 0.97 pu. At $t = 2s$, a high impedance phase to phase fault is applied for a duration of 250 ms. During the fault, the positive sequence voltage drops to 0.83 pu, and a negative sequence voltage of 0.24 pu appears. The phase to ground voltages and STATCOM currents are shown in figure 13–2. The effect of the fault is seen on the voltages, while the STATCOM leg currents are of course zero since the STATCOM is not active during this simulation.

13.2 Phase to Phase Fault with STATCOM (no DC voltage control)

The same fault case is then repeated with the STATCOM connected, but with the DC voltage controls disabled. Figure 13–3 shows the sequence voltages across the STATCOM legs resulting from this simulation. This time, the STATCOM

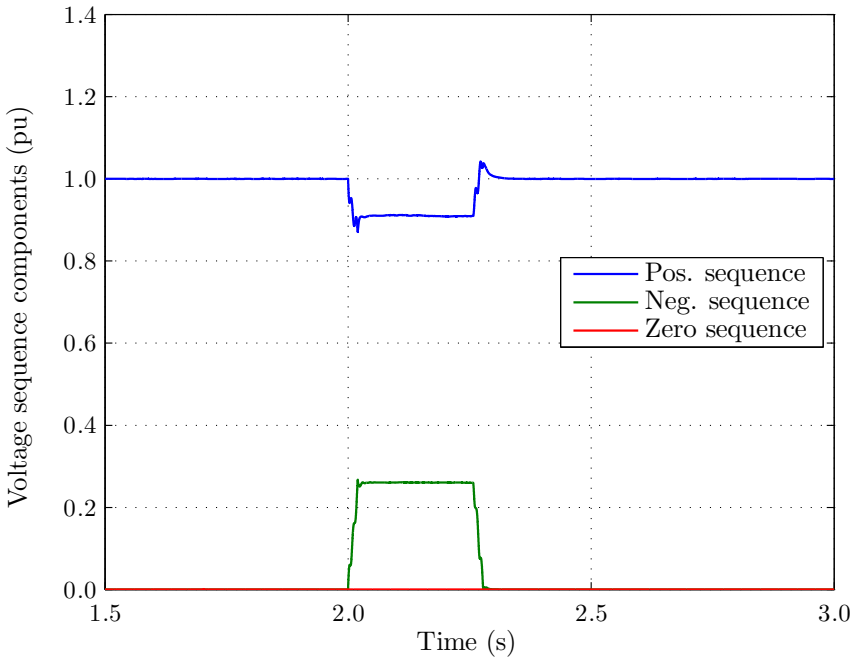

Figure 13–3: Sequence voltages (STATCOM active but no DC voltage control)

controls the positive sequence voltage to a reference of 1.0 pu before the fault.

At $t = 2s$, a high impedance phase to phase fault is applied for a duration of 250 ms. During the fault, the STATCOM reacts to support the positive sequence voltage, while the negative sequence voltage control is inactive in order to simplify the simulations. As can be seen in figure 13–3, the positive sequence voltage only drops to 0.91 pu this time, while the negative sequence voltage remains relatively unchanged. The phase to ground voltages and STATCOM currents are shown in figure 13–4.

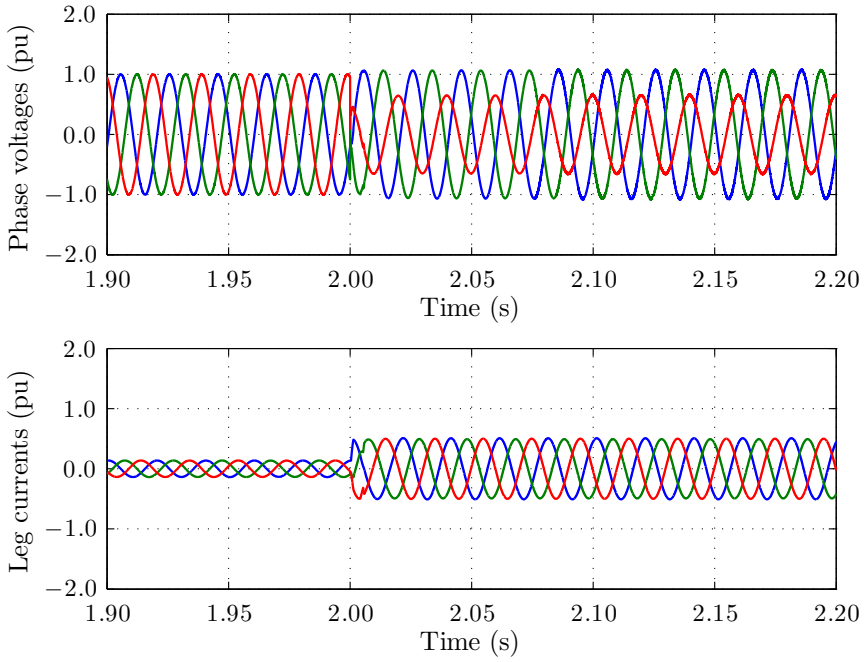

Figure 13–4: Phase voltages and currents (STATCOM active but no DC voltage control)

The DC capacitor voltages are shown in figure 13–5. Each of the three subplots shows the cell DC voltages of all three cells in blue while the reference is shown in red. It is clear from this figure that the cell DC voltages drift during the fault. The drift stops when the fault is cleared, and the voltage unbalance disappears. The drift is of course unacceptable and illustrates the necessity for the DC

voltage control scheme developed in chapter 6 and implemented in chapter 12. The following section will show the results of the same fault, but with the DC voltage controls of the STATCOM enabled.

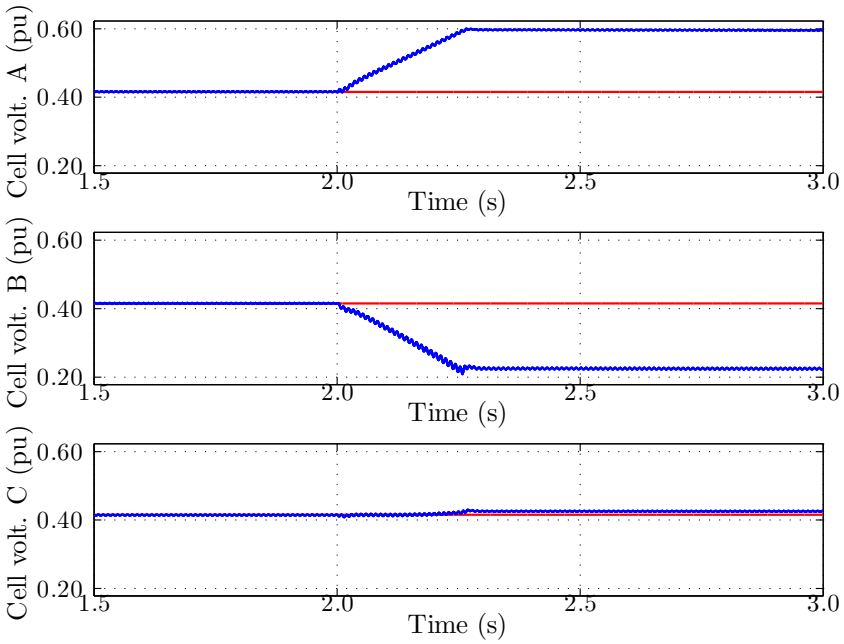

Figure 13–5: Cell voltages (STATCOM active but no DC voltage control)

13.3 Phase to Phase Fault with STATCOM (with DC voltage control)

In order to prevent the drift in DC voltage seen in the previous section, the DC voltage controls implemented in chapter 12 are enabled. The same fault case is simulated, and the resulting sequence voltages across the STATCOM legs are shown in figure 13–6. It can be seen from this figure that the positive and negative sequence voltages are the same as in the previous simulation, but this time, a zero sequence voltage with a magnitude of 0.25 pu also appears. This voltage is ordered by the DC voltage control loops in order to prevent the sum of the cell voltages in each phase to drift apart.

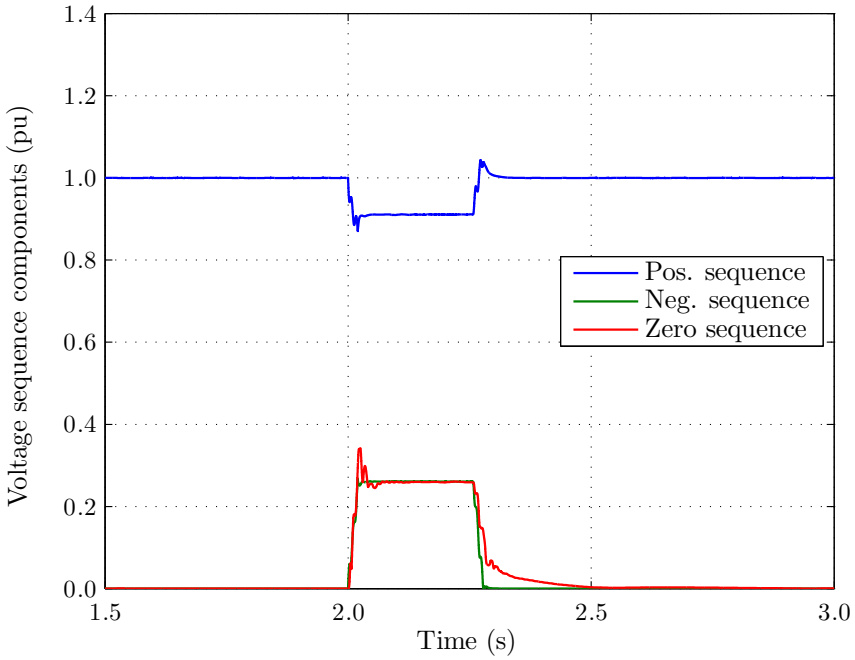

Figure 13–6: Sequence voltages (STATCOM active and DC voltage control enabled)

The phase to ground voltages and STATCOM currents are shown in figure 13–7. Comparing this figure with figure 13–4, one sees that the AC behavior of the STATCOM is unchanged by the DC voltage control. Note that the zero sequence voltage does not appear in the phase to ground quantities. It appears only across the converter legs.

The individual cell DC voltages are shown in figure 13–8. It can be seen in this figure that the DC voltage control loops are functioning correctly since all cell voltages now closely follow the references. It is interesting to note that a second harmonic component is present in the DC voltage. This is due to the fact that the STATCOM is now supplying reactive power, and this results in a charging/discharging of the DC capacitors at every half-cycle.

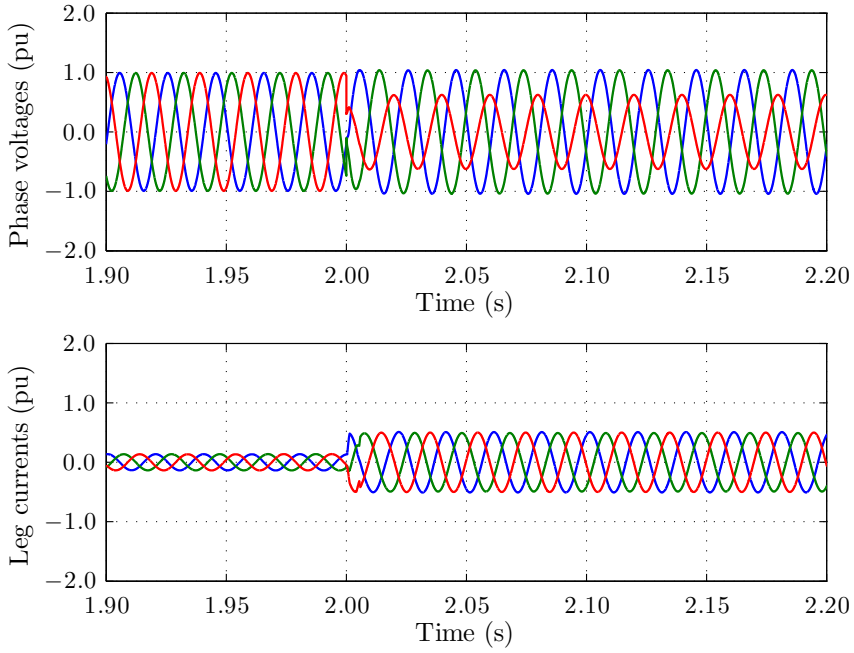

Figure 13–7: Phase voltages and currents (STATCOM active and DC voltage control enabled)

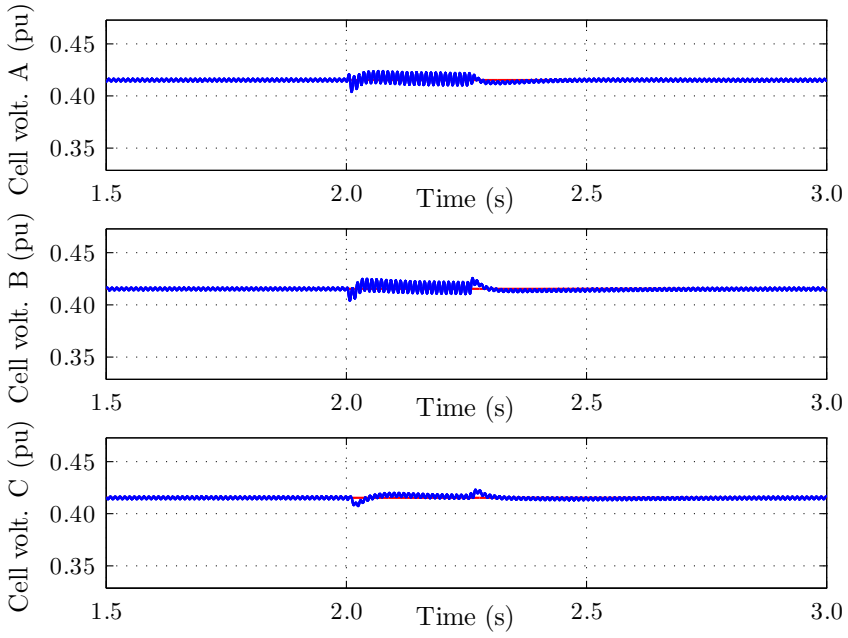

Figure 13–8: Cell voltages (STATCOM active and DC voltage control enabled)

The magnitude of the second harmonic component depends on the magnitude of the STATCOM output, and therefore, a higher amplitude is visible during the fault. This ripple is therefore part of the normal operation of the STATCOM, and must be tolerated by the controls. Since the purpose of the controls developed here is to control only the DC voltage, it suffices to filter the ripple from the capacitor voltage measurements in order to retrieve the DC quantity which is of interest.

13.4 Test of Individual control loops

In the following subsections, all the DC control loops implemented in chapter 12 are tested individually in order to show their effect on the cell DC voltages.

13.4.1 Total Converter Average DC Voltage Control Loop

In order to test that the control loop for total converter average DC voltage of figure 12–5 is working correctly, a step is applied to its reference.

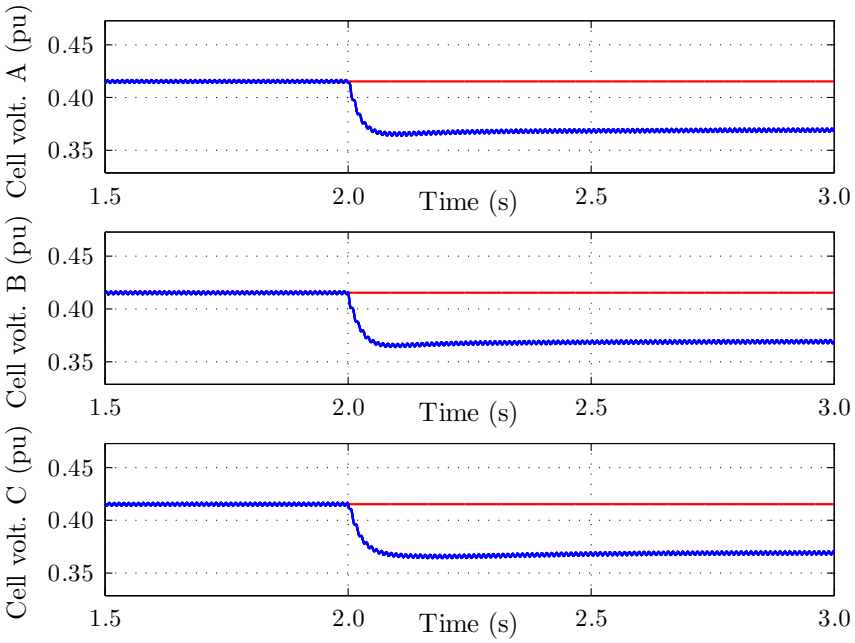

Figure 13–9: Cell voltages after a step in total converter avg. DC voltage reference

Figure 13–9 shows the individual cell DC voltages. It is clear that all cell DC voltages change. The fact that they all change together indicates that neither the converter leg average DC voltage controller nor the converter cell voltage controller are affected by the step change in reference for the total converter average DC voltage controller.

13.4.2 Test of PI based Converter Leg Average DC Voltage Control Loop

In order to show the purpose of the PI based control loop for converter leg average DC voltage shown in figure 12–7, the same phase to phase fault as in sections 13.1 to 13.3 is applied again, but this time, the PI controller is disabled. The resulting cell DC voltages are shown in figure 13–10. It is clear from this

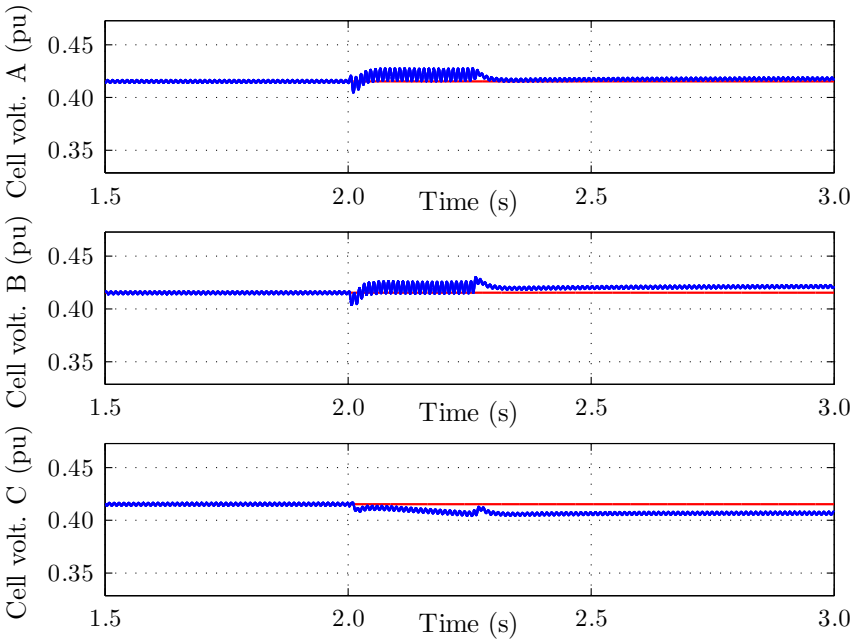

Figure 13–10: Cell voltages (PI controller for leg avg. DC voltage disabled)

figure that the predictive control loop works correctly since the DC voltages do not drift during the fault. However, as explained earlier, the non-ideal voltage and

current measurements, as well as the reaction time of the STATCOM result in a steady-state error. By comparing figure 13–10 with figure 13–8 one immediately sees that when the PI controller for leg average DC voltage balancing is disabled, a steady-state error appears.

13.4.3 Test of Predictive Converter Leg Average DC Voltage Control Loop

In order to show the purpose of the predictive control loop for converter leg average DC voltage shown in figure 12–6, the same phase to phase fault as in sections 13.1 to 13.3 is applied again, but this time, the predictive controller is disabled. The resulting cell DC voltages are shown in figure 13–11. It is clear from

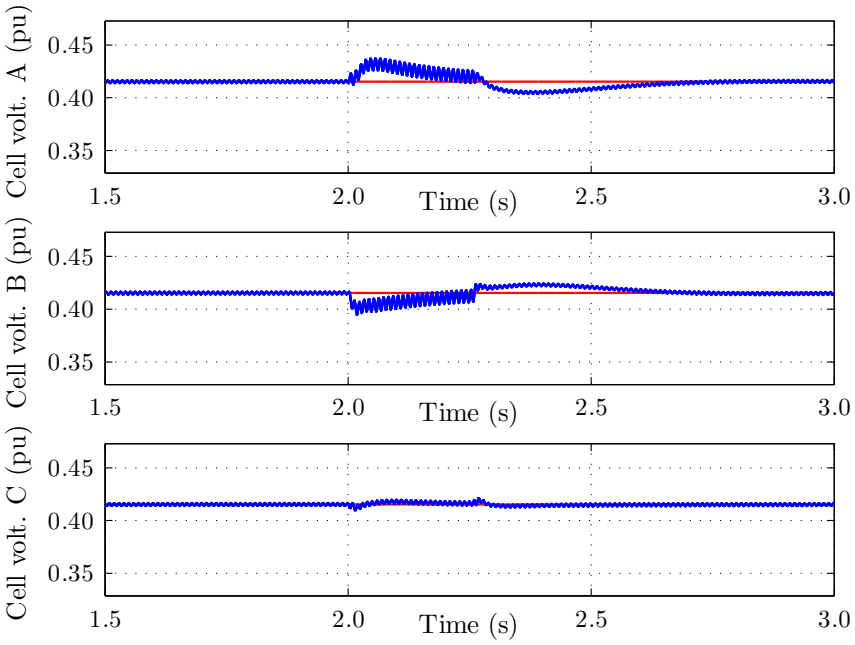

Figure 13–11: Cell voltages (Predictive leg avg. DC voltage controller disabled)

this figure that the PI based control loop works correctly since the error in the DC voltages tends to zero after some time. However, by comparing figure 13–11 with figure 13–8 one immediately sees that response of the controls is slower and a

larger drift in DC voltage occurs. This is because the predictive controller is faster that the PI based controller by nature.

The case where both leg average DC voltage controllers are disabled has already been shown in figure 13–5. It is obvious from that figure that the leg average DC voltage controllers are necessary because without them, the leg DC voltages drift considerably.

13.4.4 Test of Converter Cell Voltage Control Loop

In order to show that the control loop for converter cell voltage of figure 12–8 is working correctly, a small workaround is necessary. Indeed, the attentive reader will have noticed that in all figures showing the cell DC voltages so far, only one waveform appears in the plot of each phase. However, each of these plots should actually show three waveforms: one for each of the cells of each phase. The reason why only one waveform appears is that actually all three waveforms follow each other exactly. This is due to the fact that the cells are modeled using the simplification described in section 12–3. To show that the control loop for converter cell voltage is working correctly, the integrators of each of the cells in phase A are initialized to different values. The resulting cell DC voltages are shown in figure 13–12. The three different cell voltages can now be seen in the plot of phase A. The figure also shows how the control loop for cell voltage of each cell corrects the error between the cell voltage and the reference, which is the average of all three cell voltages in phase A.

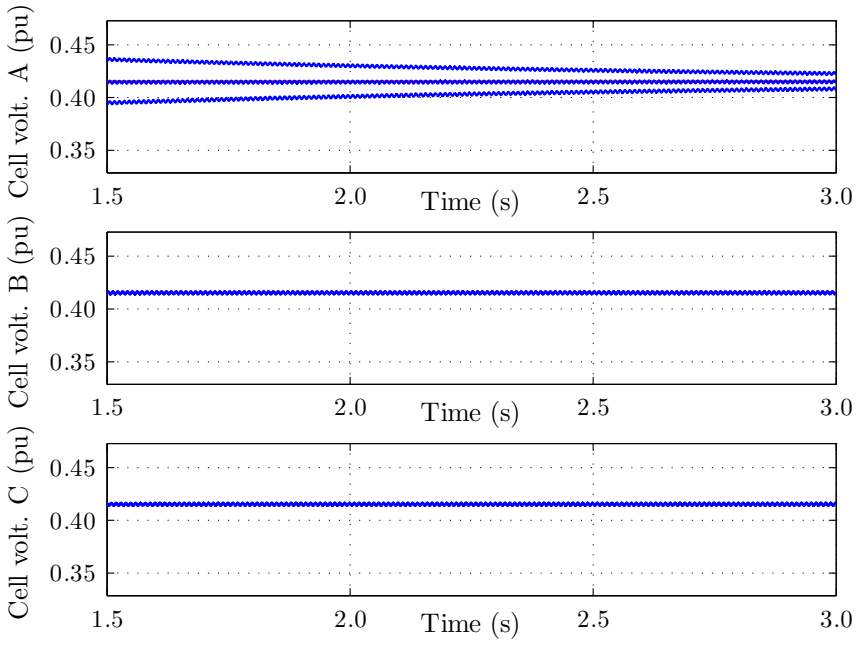

Figure 13–12: Unbalanced cell voltages within the same phase (phase A)

13.5 Summary

In this chapter, it was demonstrated in sections 13.1 to 13.3 that the DC voltage controls developed in this thesis for the the wye-coupled STATCOM function correctly globally. Furthermore, section 13.4 demonstrated that each of the control loops has its purpose and is necessary in order to correctly control the cell DC voltages.

The controls developed in chapters 5 and 7 respectively for the delta-coupled converter and wye-coupled converter with neutral path are similar in implementation to what has been shown in chapter 12 for the wye-coupled converter with floating neutral. The validations results are also similar to those presented in this chapter.

CHAPTER 14
Conclusion

The problem of DC capacitor voltage balancing in MMC based STATCOMs during unbalanced operating conditions was defined in chapter 4. It was explained that a change in DC voltage of the capacitors occurs if they are subject to a net flow of active power.

The active power flowing into the STATCOM was expressed in terms of products of sequence voltages and sequence currents, and it was shown that these terms can be grouped in two categories: those creating common mode active power flow, and those creating differential mode active power flow. The flow of common mode active power is caused by the products of voltages and currents of the same sequence, and is easily controlled to zero by ensuring that the STATCOM leg voltages and currents of same sequence are in quadrature. The flow of differential mode active power is caused by the product of voltages and currents of different sequences, and the method for controlling differential mode active power flow depends on the STATCOM topology.

Subsequent chapters then presented various STATCOM topologies, and a solution for controlling the flow of differential mode active power was developed for each topology. Chapter 5 presented a delta-coupled STATCOM, and it was shown that by imposing a zero-sequence current to flow inside the delta connection, the differential mode active power flow can be cancelled. Chapter 6 presented a wye-coupled STATCOM with ungrounded neutral, and it was shown that by imposing a zero-sequence voltage on the neutral point, the differential mode active power

flow can be cancelled. Chapter 7 presented a wye-coupled STATCOM with a neutral path, and it was shown that a combination of zero-sequence voltage and zero sequence current can be used to cancel the differential mode active power flow. Finally, chapter 10 presented a double wye-coupled STATCOM, and it was shown that in addition to the zero sequence current and zero sequence voltage methods developed in the previous chapters, a DC current can also be used to exchange active power between the corresponding legs of both wye-coupled STATCOMs. It was explained how these methods can be used individually or combined together in order to cancel the differential mode active power flow.

The implementation in *Matlab/Simulink* of a wye-coupled MMC based STATCOM with ungrounded neutral as well as the required DC voltage controls were presented in chapter 12. The validation of these controls was then done by simulation, and the results were presented in chapter 13. The proposed controls were shown to function adequately, and the main objective of this thesis was therefore achieved.

The converter topologies presented in this report were also compared, and were shown to each have their advantages and drawbacks from a performance and cost point of view. The optimal topology for a given application greatly depends on the required voltage level and desired reactive power output, as well as the unbalance conditions in which the STATCOM will be operating.

The single-wye with floating neutral and the delta-coupled STATCOMs are cost effective solutions due to the fact that they require a minimum of components. However, their operating ranges are greatly reduced during unbalanced operation, and required overrating of the voltage capability in the case of the wye-coupled STATCOM and overrating of the current capability in the case of the delta coupled STATCOM. An alternative to this is the wye-coupled STATCOM with

grounded neutral, where the neutral path is equipped with a variable impedance. This topology has the major advantage that in unbalanced operating conditions, any combination of the zero sequence voltage and the zero sequence method can be used. This results in a larger operating range, and a converter which has a lower current and voltage rating.

The double wye-coupled STATCOM topology with floating neutrals does however stand out as being the most flexible from the point of view of its operating range. It is also similar in terms of cost to a single wye-coupled STATCOM of similar size. Its main drawbacks are its increased size, and the fact that this solution is only economical if the required STATCOM size is large enough to be able to be split into two smaller wye converters.

It would therefore be interesting to perform a cost/benefit analysis of the wye-coupled STATCOM with a variable impedance in the neutral path to verify if the additional flexibiliy provided by this solution is worth the investment for the additional components which are required.

It would also be interesting to investigate the feasibility of implementing the optimization method described in chapter 8 in real-time. The available computation power is limited by the hardware platform used to implement the control and protection software functions of the STATCOM, and it may therefore be a challenge to implement in real-time such computation-intensive nonlinear optimization methods.

CHAPTER 15
Future Work

As possible future work, it would be interesting to perform a cost/benefit analysis of the wye-coupled STATCOM with a variable impedance in the neutral path to verify if the additional flexibiliy provided by this solution is worth the investment for the additional components which are required.

It would also be interesting to investigate the feasibility of implementing the optimization method described in chapter 8 in real-time. The available computation power is limited by the hardware platform used to implement the control and protection software functions of the STATCOM, and it may therefore be a challenge to implement in real-time such computation-intensive nonlinear optimization methods.

The implementation of the voltage and current limitations of the various topologies, as well as the dynamic behaviour of the STATCOM when these limits are reached during transient conditions is also a topic where further investigations are needed.

Finally, the effect of sampling and measurement delays should be investigated in order assess the performance and stability of the proposed control methods for DC voltage balancing.

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APPENDIX A
Symmetrical Components

The concept of symmetrical components being central to this thesis, a brief review of the matter is presented here. It was shown by Charles L. Fortescue that a group of n coplanar unbalanced phasors of the same nature can be represented as the sum of n balanced systems of n phasors. An example is given in figure A–1 for three phasors representing the voltages of a three-phase electrical system.

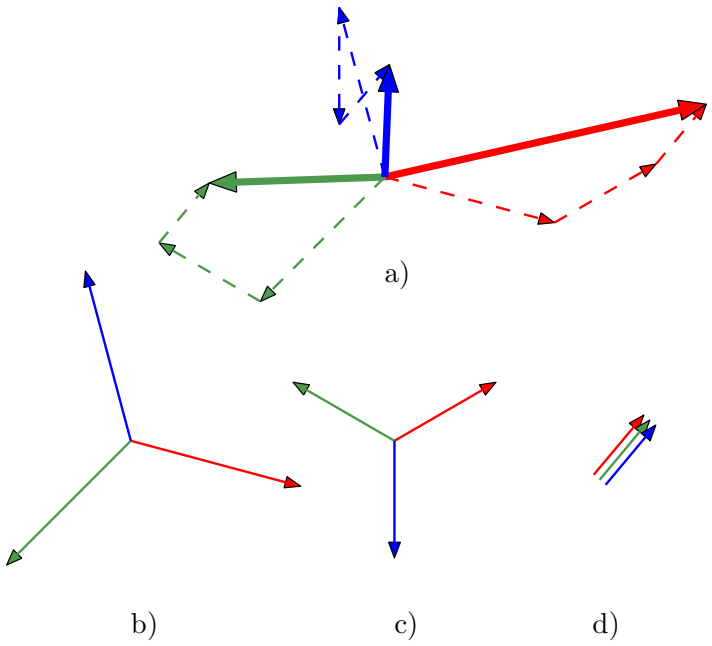

Figure A–1: a: Unbalanced voltages, b: Positive seq. , c: Negative seq. , d: Zero seq.

The three unbalanced voltages of figure A–1 a) can indeed be decomposed into the three balanced systems of three phasors shown in figure A–1 b), c) and d).

The system in b) consists of three phasors of equal amplitude and phase shifted by 120°. These phasors rotate anti-clockwise in the complex plane at an angular frequency of ω and cross any given axis in an a-b-c sequence. This system is called the positive sequence. Mathematically, we can formulate the three voltages of this positive sequence system as:

$$\vec{V}_{a1} = V_1 \angle(\phi_1) \tag{A.1}$$

$$\vec{V}_{b1} = V_1 \angle(\phi_1 - \tfrac{2\pi}{3}) \tag{A.2}$$

$$\vec{V}_{c1} = V_1 \angle(\phi_1 - \tfrac{4\pi}{3}) \tag{A.3}$$

The system in c) also consists of three phasors of equal amplitude and phase shifted by 120°. These phasors rotate anticlockwise in the complex plane at an angular frequency of ω and cross any given axis in a c-b-a sequence. This system is therefore called the negative sequence. Mathematically, we can formulate the three voltages of this negative sequence system as:

$$\vec{V}_{a2} = V_2 \angle(\phi_2) \tag{A.4}$$

$$\vec{V}_{b2} = V_2 \angle(\phi_2 - \tfrac{4\pi}{3}) \tag{A.5}$$

$$\vec{V}_{c2} = V_2 \angle(\phi_2 - \tfrac{2\pi}{3}) \tag{A.6}$$

The system in d) consists of three phasors of equal amplitude and identical phase. These phasors rotate anti-clockwise in the complex plane at an angular frequency of ω and cross any given axis at the same time. This system is therefore called the zero sequence. Mathematically, we can formulate the three voltages of this

negative sequence system as:

$$\vec{V}_{a0} = V_0 \angle \phi_0 \tag{A.7}$$

$$\vec{V}_{b0} = V_0 \angle \phi_0 \tag{A.8}$$

$$\vec{V}_{c0} = V_0 \angle \phi_0 \tag{A.9}$$

To simplify the notation, it is possible to introduce an operator which represents a rotation of 120° in the complex plane.

$$a = 1 \angle \tfrac{2\pi}{3} \tag{A.10}$$

By squaring this operator, we get:

$$a^2 = 1 \angle \tfrac{2\pi}{3} \cdot 1 \angle \tfrac{2\pi}{3} = 1 \angle \tfrac{4\pi}{3} \tag{A.11}$$

which represents a rotation of 240° in the complex plane. It is then possible to re-write equations (A.1) to (A.6) using (A.10) and (A.11) as follows:

$$\vec{V}_{a1} = \quad V_1 \angle \phi_1 \tag{A.12}$$

$$\vec{V}_{b1} = a^2 \cdot V_1 \angle \phi_1 \tag{A.13}$$

$$\vec{V}_{c1} = \ a \cdot V_1 \angle \phi_1 \tag{A.14}$$

$$\vec{V}_{a2} = \quad V_2 \angle \phi_2 \tag{A.15}$$

$$\vec{V}_{b2} = \ a \cdot V_2 \angle \phi_2 \tag{A.16}$$

$$\vec{V}_{c2} = a^2 \cdot V_2 \angle \phi_2 \tag{A.17}$$

To reconstruct the unbalanced phase voltages, the individual sequence components must be added as follows:

$$\vec{V}_a = \vec{V}_{a1} + \vec{V}_{a2} + \vec{V}_{a0} = \quad V_1\angle\phi_1 + \quad V_2\angle\phi_2 + V_0\angle\phi_0 \tag{A.18}$$

$$\vec{V}_b = \vec{V}_{b1} + \vec{V}_{b2} + \vec{V}_{b0} = a^2 \cdot V_1\angle\phi_1 + a \cdot V_2\angle\phi_2 + V_0\angle\phi_0 \tag{A.19}$$

$$\vec{V}_c = \vec{V}_{c1} + \vec{V}_{c2} + \vec{V}_{c0} = a \cdot V_1\angle\phi_1 + a^2 \cdot V_2\angle\phi_2 + V_0\angle\phi_0 \tag{A.20}$$

Equations (A.18), (A.19) and (A.20) can then be re-written in matrix form:

$$\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} \vec{V}_0 \\ \vec{V}_1 \\ \vec{V}_2 \end{bmatrix} \tag{A.21}$$

Finally, the inverse transformation can be found to be:

$$\begin{bmatrix} \vec{V}_0 \\ \vec{V}_1 \\ \vec{V}_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{A.22}$$

APPENDIX B
Differential Mode and Common Mode Extraction for Scalar Quantities

The purpose of this appendix is to explain how to extract the differential mode and common mode of three-phase scalar quantities. First, the concept of differential mode and common mode quantities is defined using two variables in order to simplify the explanation.

Taking two scalar variables x_1 and x_2, the common mode and the differential mode of these variables are then:

$$x_{comm} = \frac{x_1 + x_2}{2} \tag{B.1}$$

$$x_{diff} = \frac{x_1 - x_2}{2} \tag{B.2}$$

Note that these equations are commonly used in signal processing, and are applicable for AC quantities as well as DC quantities. This therefore justifies their validity for use with scalar quantities. The latter equations can then be put into matrix form as follows:

$$\begin{bmatrix} x_{comm} \\ x_{diff} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{B.3}$$

The inverse of this relationship is:

$$x_1 = x_{comm} + x_{diff} \tag{B.4}$$

$$x_2 = x_{comm} - x_{diff} \tag{B.5}$$

and in matrix form:

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} x_{comm} \\ x_{diff} \end{bmatrix} \tag{B.6}$$

Another way of formulating this relationship is:

$$x_{1,diff} = x_1 - x_{comm} \tag{B.7}$$

$$x_{2,diff} = x_2 - x_{comm} \tag{B.8}$$

However, by definition,

$$x_{1,diff} = -x_{2,diff} = x_{diff} \tag{B.9}$$

This means that only one of the two equations B.7 and B.8 is sufficient in order to define x_{diff} if an expression for x_{comm} is known. Taking equation B.7, and substituting the definition for x_{comm}, one gets:

$$x_{1,diff} = x_{diff} = x_1 - x_{comm} = x_1 - \frac{x_1 + x_2}{2} = \frac{x_1 - x_2}{2} \tag{B.10}$$

The latter is, as expected, the same as B.2. All the manipulations above may seem trivial, however, the methodology developed for the case with two variables was meant to be a simple example. The same methodology will now be used for the case with three variables. Taking three scalar variables x_1, x_2 and x_3, the common mode and the differential mode of these variables are then:

$$x_{comm} = \frac{x_1 + x_2 + x_3}{3} \tag{B.11}$$

$$x_{1,diff} = x_1 - x_{comm} \tag{B.12}$$

$$x_{2,diff} = x_2 - x_{comm} \tag{B.13}$$

$$x_{3,diff} = x_3 - x_{comm} \tag{B.14}$$

This time, by definition,

$$x_{3,diff} = -x_{1,diff} - x_{2,diff} \tag{B.15}$$

Therefore, two of the three equations B.12, B.13 and B.14 are sufficient in order to define the differential components if an expression for x_{comm} is known. Taking equations B.12 and B.13, and substituting the definition for x_{comm}, one gets:

$$x_{1,diff} = x_1 - x_{comm} = x_1 - \frac{x_1 + x_2 + x_3}{3} = \frac{2x_1 - x_2 - x_3}{3} \tag{B.16}$$

$$x_{2,diff} = x_2 - x_{comm} = x_2 - \frac{x_1 + x_2 + x_3}{3} = \frac{-x_1 + 2x_2 - x_3}{3} \tag{B.17}$$

Finally, putting equations B.11, B.16 and B.17 in matrix form:

$$\begin{bmatrix} x_{1,diff} \\ x_{2,diff} \\ x_{comm} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} \tag{B.18}$$

Equation B.18 is the same as equation 2 in [23]. For reference purposes, the inverse is:

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \\ -1 & -1 & 1 \end{bmatrix} \begin{bmatrix} x_{1,diff} \\ x_{2,diff} \\ x_{comm} \end{bmatrix} \tag{B.19}$$

APPENDIX C
Network Unbalances

C.1 Network Unbalances During Faults

This appendix gives a brief description of the behavior of network voltages during faults. For the analysis here, it is assumed that all faults occur on the STATCOM busbar. This assumption is justified in the sense that a bolted fault at the terminals of the STATCOM constitues the worst possible fault condition in terms of voltage unbalance. A fault elsewhere in the network will result in lesser constraints on the STATCOM operating modes. For this analysis, a simple Thevenin network equivalent is considered. That is, the network is modeled as an ideal voltage source behind an impedance. Therefore, this model does not represent changes in frequency or voltage angle during the fault. It is also assumed for this analysis that the ideal three-phase source supplies only positive sequence voltages. This appendix contains several phasor plots. The legend to interpret these plots is given in figure 11–1.

C.1.1 Grounded Network

The first type of three-phase network model to be considered is the grounded network as shown in figure C–1. During normal conditions, the phase voltages with respect to ground at the point of common coupling are:

$$\vec{V_a} = V\angle 0 \tag{C.1}$$

$$\vec{V_b} = V\angle -\tfrac{2\pi}{3} \tag{C.2}$$

$$\vec{V_c} = V\angle -\tfrac{4\pi}{3} \tag{C.3}$$

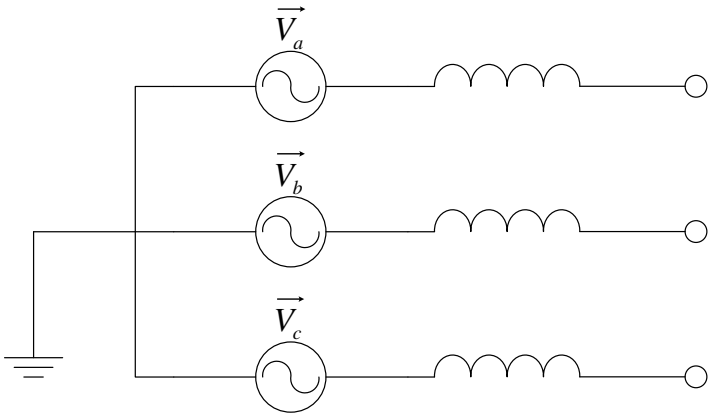

Figure C–1: Grounded Net

Single-Phase to Ground Fault

If any of the three phases is grounded, the voltage with respect to ground for that phase becomes zero. For example, grounding the phase a, we get:

$$\vec{V_a} = 0 \tag{C.4}$$

$$\vec{V_b} = V\angle -\tfrac{2\pi}{3} \tag{C.5}$$

$$\vec{V_c} = V\angle -\tfrac{4\pi}{3} \tag{C.6}$$

and by applying (A.22) we get:

$$\vec{V_0} = \tfrac{1}{3}V\angle \pi \tag{C.7}$$

$$\vec{V_1} = \tfrac{2}{3}V\angle 0 \tag{C.8}$$

$$\vec{V_2} = \tfrac{1}{3}V\angle \pi \tag{C.9}$$

Figure C–2 is a phasor diagram representing the phase to ground voltages during the fault. The symmetrical components composing each phase voltage are represented by the smaller dashed phasors.

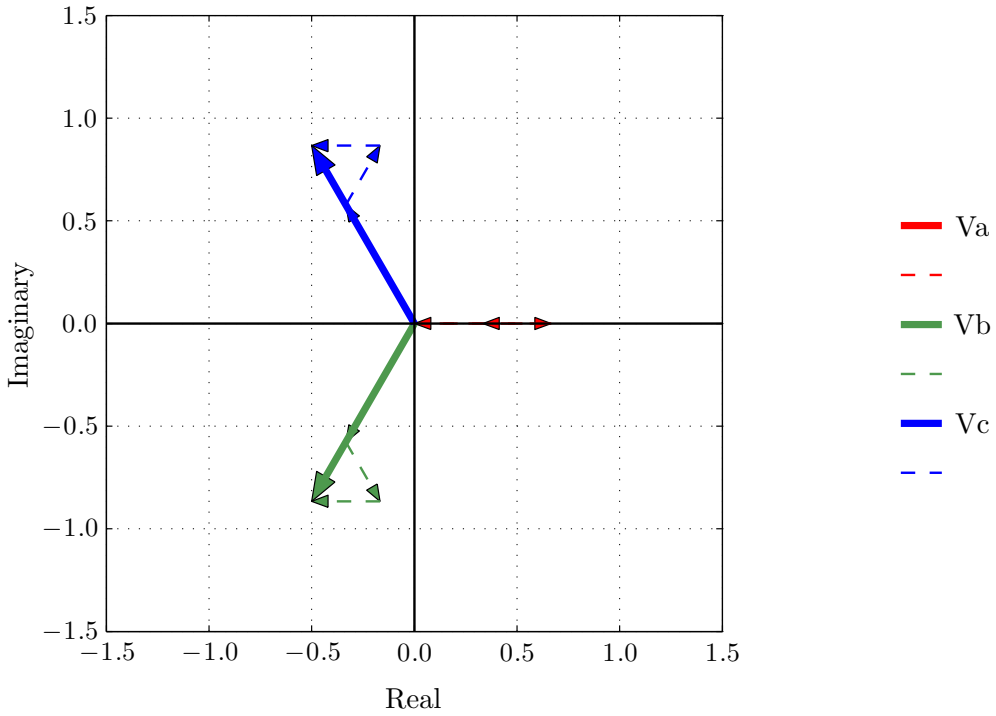

Figure C–2: Phase voltages during a single phase to ground fault in phase a

Two-Phases to Ground Fault

If any two of the three phases are grounded, the voltages with respect to ground for those phases become zero. For example, grounding the phases a and b, we get:

$$\vec{V_a} = 0 \tag{C.10}$$

$$\vec{V_b} = 0 \tag{C.11}$$

$$\vec{V_c} = V \angle -\tfrac{4\pi}{3} \tag{C.12}$$

and by applying (A.22) we get:

$$\vec{V_0} = \tfrac{1}{3} V \angle -\tfrac{4\pi}{3} \tag{C.13}$$

$$\vec{V_1} = \tfrac{1}{3} V \angle 0 \tag{C.14}$$

$$\vec{V_2} = \tfrac{1}{3} V \angle -\tfrac{2\pi}{3} \tag{C.15}$$

Figure C–3 is a phasor diagram representing the phase to ground voltages during the fault. The symmetrical components composing each phase voltage are represented by the smaller dashed phasors.

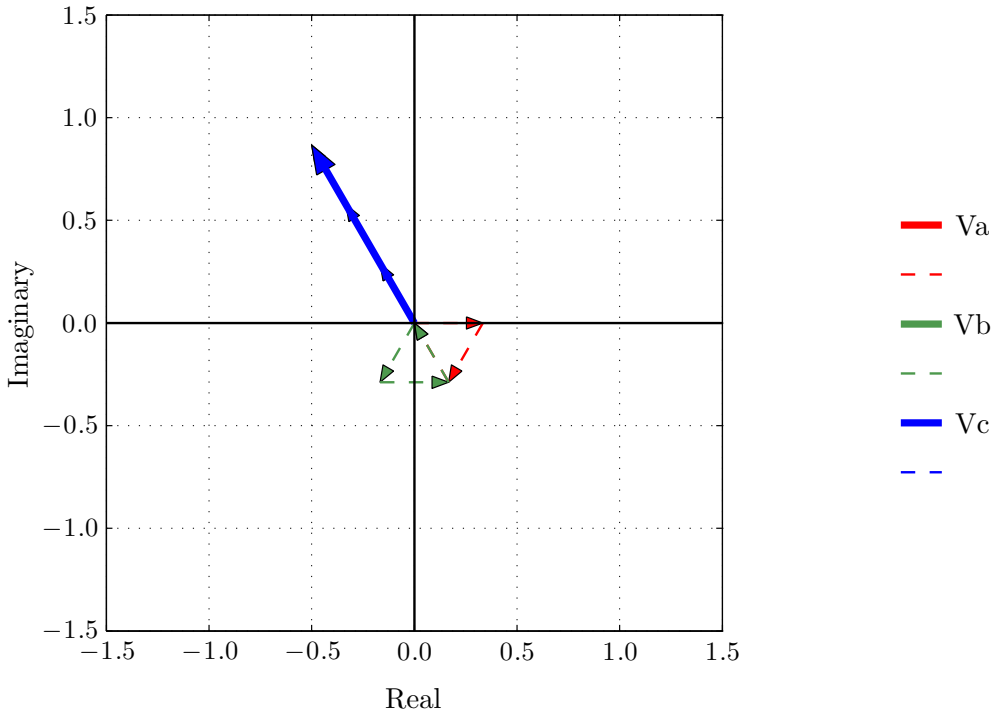

Figure C–3: Phase voltages during a two phase to ground fault in phases a and b

Phase to Phase Fault

If two phases are connected together but not to ground, the voltage with respect to ground for these two phases will of course be the same. For example, figure C–4 shows the case where phases b and c are connected together. To calculate

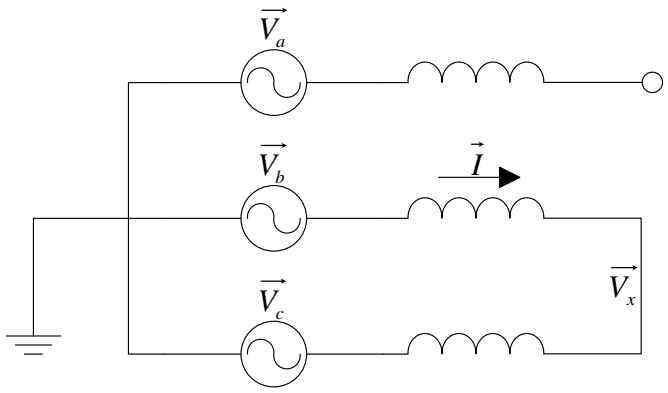

Figure C–4: Phase to Phase fault in a grounded network

the voltage which appears at the connection point of the faulted phases, KVL is first applied around the loop.

$$\vec{V}_b - \vec{I}\vec{Z}_l = \vec{V}_c + \vec{I}\vec{Z}_l \tag{C.16}$$

$$\vec{I}\vec{Z}_l = \frac{\vec{V}_b - \vec{V}_c}{2} \tag{C.17}$$

Then, solving for $\vec{V}_x$ we get:

$$\vec{V}_x = \vec{V}_b - \vec{I}\vec{Z}_l \tag{C.18}$$

$$= \frac{\vec{V}_b + \vec{V}_c}{2} \tag{C.19}$$

Since the ideal three-phase source supplies positive sequence voltages only, the latter expression can be simplified as:

$$\vec{V}_x = \tfrac{1}{2} V \angle \pi \tag{C.20}$$

The voltages during the fault are therefore:

$$\vec{V}_a = V\angle 0 \tag{C.21}$$

$$\vec{V}_b = \tfrac{1}{2}V\angle \pi \tag{C.22}$$

$$\vec{V}_c = \tfrac{1}{2}V\angle \pi \tag{C.23}$$

and by applying (A.22) we get:

$$\vec{V}_0 = 0 \tag{C.24}$$

$$\vec{V}_1 = \tfrac{1}{2}V\angle 0 \tag{C.25}$$

$$\vec{V}_2 = \tfrac{1}{2}V\angle 0 \tag{C.26}$$

Figure C–5 is a phasor diagram representing the phase to ground voltages during the fault. The symmetrical components composing each phase voltage are repre-

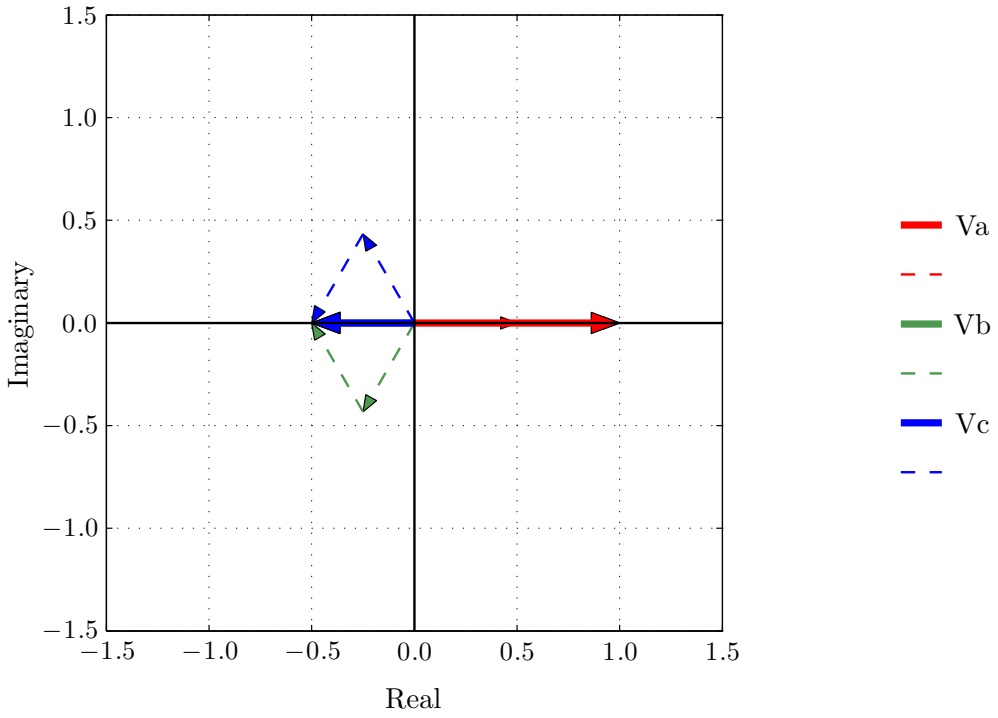

Figure C–5: Phase voltages during a phase to phase fault between phases b and c

sented by the smaller dashed phasors.

Three-Phase Fault

The three-phase fault is a balanced fault and therefore creates no unbalances in the voltages. The fact that the fault is three-phase to ground or simply three-phase makes no difference here because it is assumed that the sources provide only positive sequence voltage, and the series impedances are equal. Therefore, in the event of a three-phase fault, the voltages become:

$$\vec{V}_a = 0 \tag{C.27}$$

$$\vec{V}_b = 0 \tag{C.28}$$

$$\vec{V}_c = 0 \tag{C.29}$$

and of course, by applying (A.22) we simply get:

$$\vec{V}_0 = 0 \tag{C.30}$$

$$\vec{V}_1 = 0 \tag{C.31}$$

$$\vec{V}_2 = 0 \tag{C.32}$$

C.1.2 Ungrounded Network

The second type of three-phase network model to be considered is the ungrounded network as shown in figure C–6. During normal conditions, the phase voltages with respect to ground at the point of common coupling are indentical to the previous model, that is:

$$\vec{V}_a = V\angle 0 \tag{C.33}$$

$$\vec{V}_b = V\angle -\tfrac{2\pi}{3} \tag{C.34}$$

$$\vec{V}_c = V\angle -\tfrac{4\pi}{3} \tag{C.35}$$

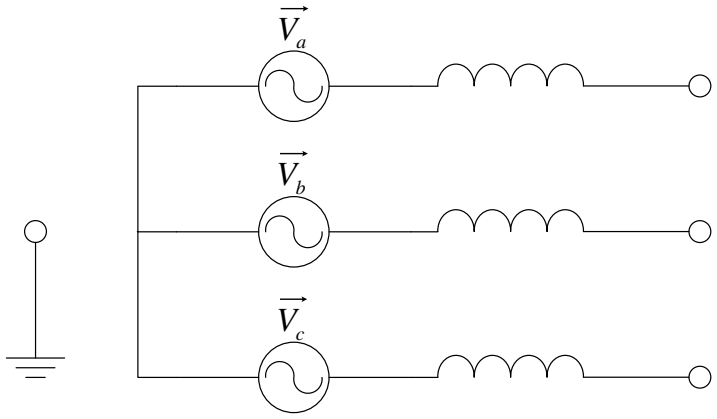

Figure C–6: Ungrounded Network

The difference is that the neutral point of the network is floating with respect to ground.

Single-Phase to Ground Fault

Revisiting the case of the single phase to ground fault, it is clear that if any of the three phases is grounded, the voltage with respect to ground for that phase becomes zero. However, the neutral point being floating, it is free to take any potential. In the current case of interest, the neutral will therefore take a potential equal to the negative of the source in the grounded phase. This will result in an increase of the phase to ground voltage in the healthy phases. For example, grounding the phase a, we get:

$$\vec{V}_a = 0 \tag{C.36}$$

$$\vec{V}_b = V\angle -\tfrac{2\pi}{3} - V\angle 0 = \sqrt{3}V\angle -\tfrac{5\pi}{6} \tag{C.37}$$

$$\vec{V}_c = V\angle -\tfrac{4\pi}{3} - V\angle 0 = \sqrt{3}V\angle -\tfrac{7\pi}{6} \tag{C.38}$$

and by applying (A.22) we get:

$$\vec{V_0} = V\angle\pi \tag{C.39}$$

$$\vec{V_1} = V\angle 0 \tag{C.40}$$

$$\vec{V_2} = 0 \tag{C.41}$$

Figure C–7 is a phasor diagram representing the phase to ground voltages during the fault. The symmetrical components composing each phase voltage are represented by the smaller dashed phasors.

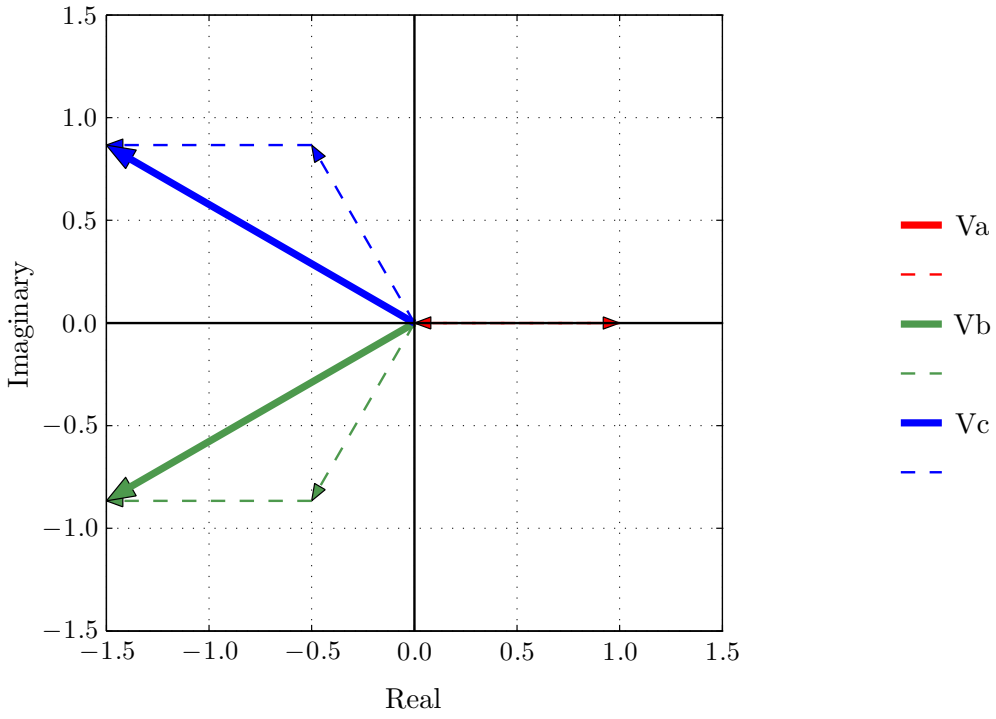

Figure C–7: Phase voltages during a single phase to ground fault in phase a

Two-Phases to Ground Fault

If any two of the three phases are grounded, the voltages with respect to ground for those phases become zero. However, the neutral point being floating, it is free to take any potential. In the current case of interest, the neutral will

therefore take a non-zero potential. For example, grounding the phases a and b, we get the situation described by figure C–8 In a similar fashion to the phase to

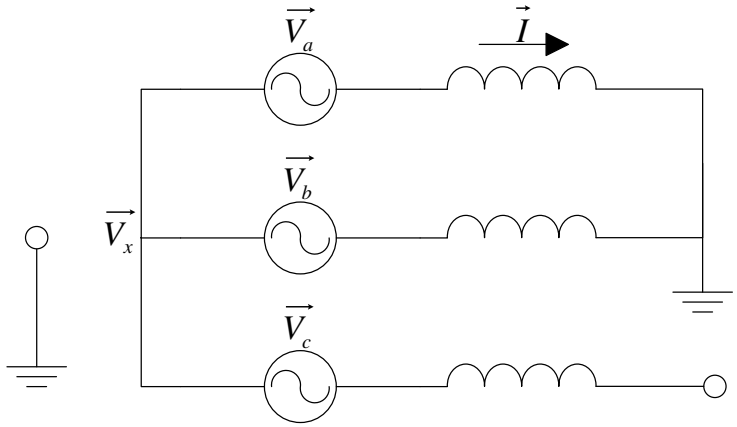

Figure C–8: Two-Phase to Ground Fault in an Ungrounded Network

phase fault in the grounded network, KVL can be applied around the loop.

$$-\vec{V}_a + \vec{I}\vec{Z}_l = -\vec{V}_b - \vec{I}\vec{Z}_l \tag{C.42}$$

$$\vec{I}\vec{Z}_l = \frac{\vec{V}_a - \vec{V}_b}{2} \tag{C.43}$$

Then, solving for $\vec{V}_x$ we get:

$$\vec{V}_x = -\vec{V}_a + \vec{I}\vec{Z}_l \tag{C.44}$$

$$= \frac{-\vec{V}_a - \vec{V}_b}{2} \tag{C.45}$$

Again, since the ideal three-phase source supplies positive sequence voltages only, the latter expression can be simplified as:

$$\vec{V}_x = \tfrac{1}{2}V\angle -\tfrac{4\pi}{3} \tag{C.46}$$

In other words, a two-phase to ground fault in phases a and b results in an increase of the neutral voltage by $\vec{V}_x$ calculated above. Therefore, the phase to ground

voltages at the point of common coupling become:

$$\vec{V_a} = 0 \tag{C.47}$$

$$\vec{V_b} = 0 \tag{C.48}$$

$$\vec{V_c} = V\angle -\tfrac{4\pi}{3} + \tfrac{1}{2}V\angle -\tfrac{4\pi}{3} = \tfrac{3}{2}V\angle -\tfrac{4\pi}{3} \tag{C.49}$$

and by applying (A.22) we get:

$$\vec{V_0} = \tfrac{1}{2}V\angle -\tfrac{4\pi}{3} \tag{C.50}$$

$$\vec{V_1} = \tfrac{1}{2}V\angle 0 \tag{C.51}$$

$$\vec{V_2} = \tfrac{1}{2}V\angle -\tfrac{2\pi}{3} \tag{C.52}$$

Figure C–9 is a phasor diagram representing the phase to ground voltages during the fault. The symmetrical components composing each phase voltage are repre-

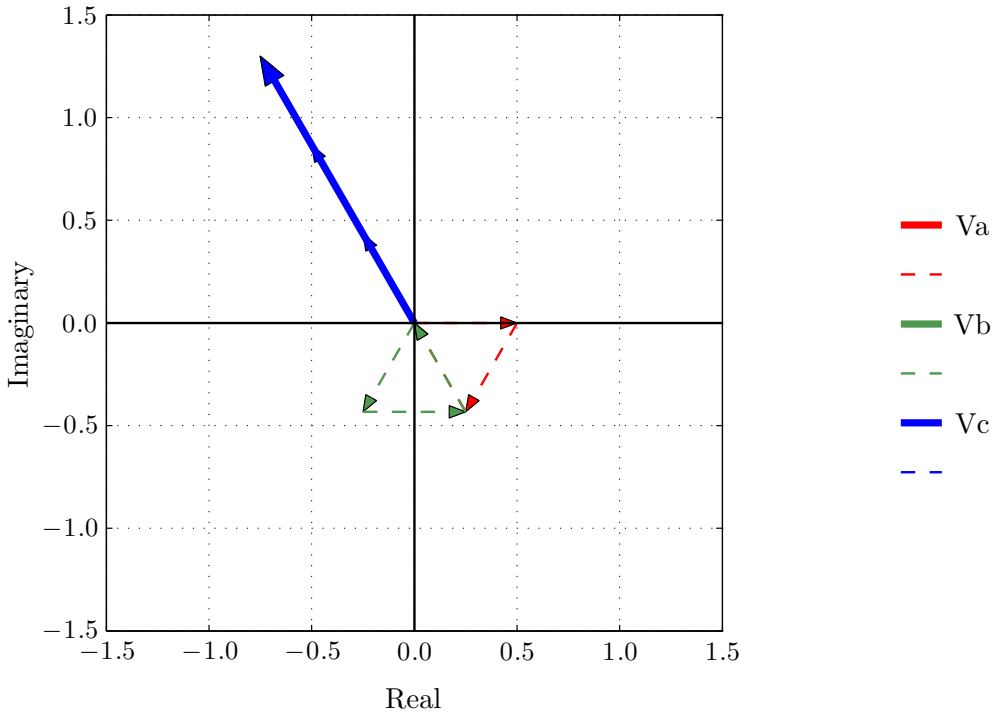

Figure C–9: Phase voltages during a two phase to ground fault in phases a and b

sented by the smaller dashed phasors.

Phase to Phase Fault

If two phases are connected together but not to ground, the voltage with respect to ground for these two phases will of course be the same. Revisiting the phase to phase fault case for the grounded network but with an ungrounded network this time, we can rewrite (C.16) and (C.17) as follows:

$$\vec{V}_b - \vec{I}\vec{Z}_l + \vec{V}_y = \vec{V}_c + \vec{I}\vec{Z}_l + \vec{V}_y \tag{C.53}$$

$$\vec{I}\vec{Z}_l = \frac{\vec{V}_b - \vec{V}_c}{2} \tag{C.54}$$

Where $\vec{V}_y$ is the voltage of the neutral point. It is clear that $\vec{V}_y$ has no impact on the voltage drop across the impedance. Solving for $\vec{V}_x$ we get:

$$\vec{V}_x = \vec{V}_y + \vec{V}_b - \vec{I}\vec{Z}_l \tag{C.55}$$

$$= \vec{V}_y + \frac{\vec{V}_b + \vec{V}_c}{2} \tag{C.56}$$

As shown by (C.53) and (C.54), the neutral voltage is completely independent from the phase to phase fault condition and could take any value including zero. Since the ideal three-phase source supplies positive sequence voltages only, and since the impedances are balanced, it is obvious that the neutral voltage is zero prior to the fault and therefore remains zero during the fault. The latter expression can then be simplified as:

$$\vec{V}_x = \tfrac{1}{2} V \angle \pi \tag{C.57}$$

The voltages during the fault are therefore:

$$\vec{V_a} = V\angle 0 \tag{C.58}$$

$$\vec{V_b} = \tfrac{1}{2}V\angle \pi \tag{C.59}$$

$$\vec{V_c} = \tfrac{1}{2}V\angle \pi \tag{C.60}$$

and by applying (A.22) we get:

$$\vec{V_0} = 0 \tag{C.61}$$

$$\vec{V_1} = \tfrac{1}{2}V\angle 0 \tag{C.62}$$

$$\vec{V_2} = \tfrac{1}{2}V\angle 0 \tag{C.63}$$

Figure C–10 is a phasor diagram representing the phase to ground voltages during

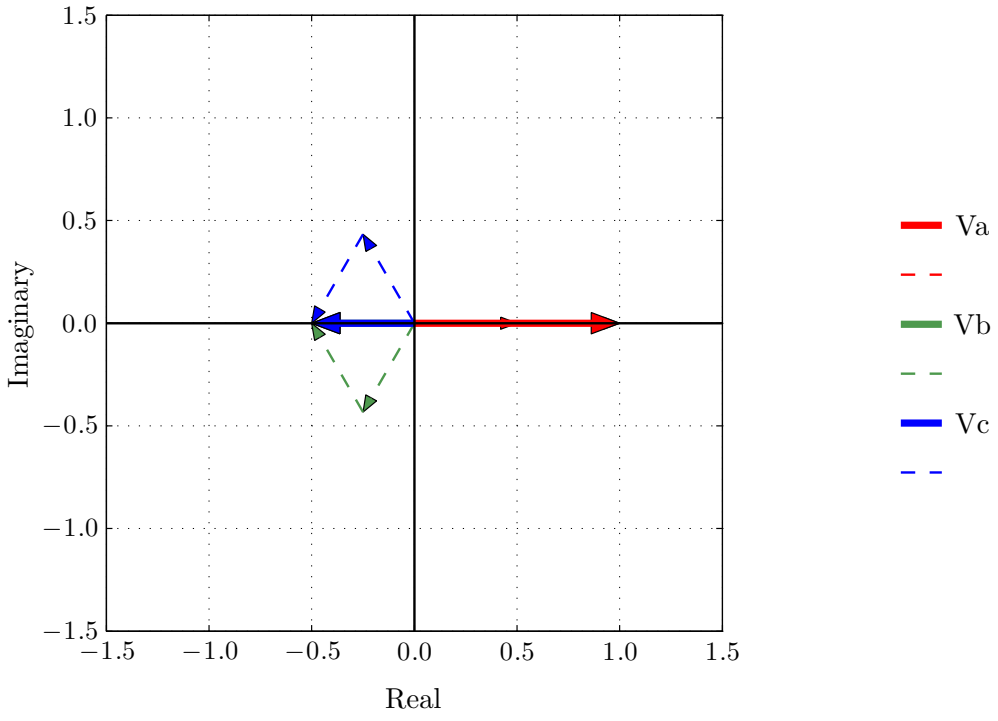

Figure C–10: Phase voltages during a phase to phase fault between phases b and c

the fault. The symmetrical components composing each phase voltage are represented by the smaller dashed phasors.

Three-Phase Fault

The three-phase fault is a balanced fault and therefore creates no unbalances in the voltages. Equations (C.27) to (C.32) thus remain valid.

C.2 Network Unbalances During Normal Operation

The network voltages may also be unblanced during normal operation. These unbalances can be attributed to several phenomena occuring both at the transmission level and at the distribution level in many networks. The two main causes of network voltage unbalances during normal operation are: unbalanced mutual inductance between phases in a transmission line, and unbalanced loads. The following sections will not present an in depth analysis of these problems, but will rather present them in a general way so that the reader may become familiar with the concepts.

C.2.1 Transmission Line Unbalanced Impedances

A typical high voltage alternating current transmission line is shown in figure C–11. The three phase conductors are physically arranged in a coplaner manner, and a neutral wire is placed above the phase conductors. The ground should also be considered as a conductor. The voltages at the sending end and at the receiving end of this line are:

$$\vec{V}^s = \begin{bmatrix} \vec{V}_a^s \\ \vec{V}_b^s \\ \vec{V}_c^s \\ \vec{V}_e^s \\ \vec{V}_g^s \end{bmatrix} \qquad \vec{V}^r = \begin{bmatrix} \vec{V}_a^r \\ \vec{V}_b^r \\ \vec{V}_c^r \\ \vec{V}_e^r \\ \vec{V}_g^r \end{bmatrix} \tag{C.64}$$

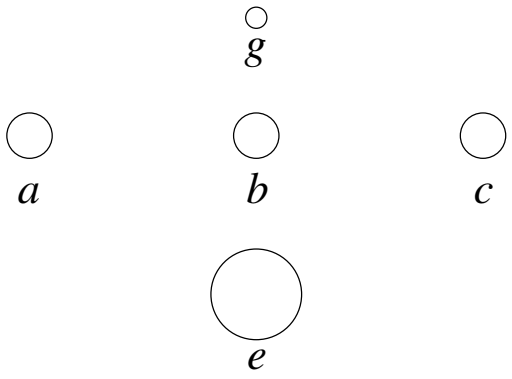

Figure C–11: Typical three-phase transmission line

A primitive admittance matrix can be found which relates the currents and voltages according to

$$\begin{bmatrix} \vec{I}_a \\ \vec{I}_b \\ \vec{I}_c \\ \vec{I}_e \\ \vec{I}_g \end{bmatrix} = \begin{bmatrix} \vec{Y}_{aa} & \vec{Y}_{ab} & \vec{Y}_{ac} & \vec{Y}_{ae} & \vec{Y}_{ag} \\ \vec{Y}_{ba} & \vec{Y}_{bb} & \vec{Y}_{bc} & \vec{Y}_{be} & \vec{Y}_{bg} \\ \vec{Y}_{ca} & \vec{Y}_{cb} & \vec{Y}_{cc} & \vec{Y}_{ce} & \vec{Y}_{cg} \\ \vec{Y}_{ea} & \vec{Y}_{eb} & \vec{Y}_{ec} & \vec{Y}_{ee} & \vec{Y}_{eg} \\ \vec{Y}_{ga} & \vec{Y}_{gb} & \vec{Y}_{gc} & \vec{Y}_{ge} & \vec{Y}_{gg} \end{bmatrix} \left(\begin{bmatrix} \vec{V}_a^s \\ \vec{V}_b^s \\ \vec{V}_c^s \\ \vec{V}_e^s \\ \vec{V}_g^s \end{bmatrix} - \begin{bmatrix} \vec{V}_a^r \\ \vec{V}_b^r \\ \vec{V}_c^r \\ \vec{V}_e^r \\ \vec{V}_g^r \end{bmatrix} \right) \tag{C.65}$$

Since the ground conductor and the earth are at the same potential, this five conductor system can be reduced to a three conductor equivalent by expressing the phase voltages at both ends of the line with respect to their local ground potentials. A full demonstration of this is presented in [10]. The result is a simplified system

$$\begin{bmatrix} \vec{I}_a \\ \vec{I}_b \\ \vec{I}_c \end{bmatrix} = \begin{bmatrix} \vec{Y}_{aaeq} & \vec{Y}_{abeq} & \vec{Y}_{aceq} \\ \vec{Y}_{baeq} & \vec{Y}_{bbeq} & \vec{Y}_{bceq} \\ \vec{Y}_{caeq} & \vec{Y}_{cbeq} & \vec{Y}_{cceq} \end{bmatrix} \begin{bmatrix} \left(\vec{V}_a^s - \vec{V}_g^s\right) - \left(\vec{V}_a^r - \vec{V}_g^r\right) \\ \left(\vec{V}_b^s - \vec{V}_g^s\right) - \left(\vec{V}_b^r - \vec{V}_g^r\right) \\ \left(\vec{V}_c^s - \vec{V}_g^s\right) - \left(\vec{V}_c^r - \vec{V}_g^r\right) \end{bmatrix} \tag{C.66}$$

By transforming the simplified admittance matrix to its equivalent symmetric admittance matrix, we get

$$\frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} \vec{Y}_{aaeq} & \vec{Y}_{abeq} & \vec{Y}_{aceq} \\ \vec{Y}_{baeq} & \vec{Y}_{bbeq} & \vec{Y}_{bceq} \\ \vec{Y}_{caeq} & \vec{Y}_{cbeq} & \vec{Y}_{cceq} \end{bmatrix}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} = \begin{bmatrix} \vec{Y}_{00} & \vec{Y}_{01} & \vec{Y}_{02} \\ \vec{Y}_{10} & \vec{Y}_{11} & \vec{Y}_{12} \\ \vec{Y}_{20} & \vec{Y}_{21} & \vec{Y}_{22} \end{bmatrix} \quad \text{(C.67)}$$

For the latter to represent a balanced transmission line, the off-diagonal terms must be zero. This can be understood as the requirement that a zero sequence voltage give rise solely to a zero sequence current, a positive sequence voltage give rise solely to a positive sequence current and a negative sequence voltage give rise solely to a negative sequence current. In other words, a balanced line will not create coupling between sequence networks. For the off-diagonal terms of the symmetric admittance matrix to be zero, two constraints are imposed on the simplified admittance matrix:

$$\vec{Y}_{aaeq} = \vec{Y}_{bbeq} = \vec{Y}_{cceq} \quad \text{(C.68)}$$

$$\vec{Y}_{abeq} = \vec{Y}_{aceq} = \vec{Y}_{baeq} = \vec{Y}_{bceq} = \vec{Y}_{caeq} = \vec{Y}_{cbeq} \quad \text{(C.69)}$$

These constraints can in turn be understood as the requirement for the self admittances of the phase conductors to be equal, and for the mutual admittances between phases to be equal. The only way for this second requirement to be possible is for the physical arrangement of the conductors to be symmetrical with respect to all three phase conductors. That is, the distances between phases must be equal, the distances from each phase to the ground conductor must be equal and the distances from each phase to the earth must be equal. The way to achieve this in practice is to transpose the phase conductors so that over the entire length of the transmission line, each phase conductor will be in each position equally.

C.2.2 Unbalanced loads

For various reasons, loads may be unbalanced as well. Often, this is caused by the presence of single phase loads. Single phase loads are sometimes preferred at the distribution level because they are fed by less conductors than three-phase loads. The way to minimize this problem is to try to distribute single-phase loads evenly on all three phases so that the total loading is approximately balanced.

C.3 Summary

The goal of this chapter was to show the worst unbalance conditions to be expected in a network during fault conditions as well as during normal operating conditions. The table below summarizes the results of the analysis regarding fault conditions. With regards to transmission line and load unbalances, utilities generally try to minimize these problems by transposing long transmission lines and by ditributing evenly unbalanced loads. The result is that network unbalances during normal operation are usually kept at very low levels. Generally speaking, the ratio of negative sequence voltage to positive seuquence voltage is around 1%, and the zero sequence voltage is at negligible levels.

Table C–1 summarizes the results obtained in sections C.1.1 and C.1.2. The reader should keep in mind that the voltage unbalances summarized in this table were calculated using several assumptions. The major assumptions are that:

- The network model uses an ideal three-phase source which supplies only positive sequence voltages
- The impedances are equal in all phases
- The network model is not dynamic (i.e. does not represent phase shifts or changes in frequency during the fault)
- Transient phenomena are ignored (conditions during a fault are considered steady-state conditions for the entire duration of the fault)

Table C–1: Summary of Voltage Unbalances Due to Faults

Fault Type	Grounded Network	Ungrounded Network
One phase to ground	$\vec{V_0} = \frac{1}{3}V\angle\pi$ $\vec{V_1} = \frac{2}{3}V\angle 0$ $\vec{V_2} = \frac{1}{3}V\angle\pi$	$\vec{V_0} = V\angle\pi$ $\vec{V_1} = V\angle 0$ $\vec{V_2} = 0$
Two phases to ground	$\vec{V_0} = \frac{1}{3}V\angle-\frac{4\pi}{3}$ $\vec{V_1} = \frac{1}{3}V\angle 0$ $\vec{V_2} = \frac{1}{3}V\angle-\frac{2\pi}{3}$	$\vec{V_0} = \frac{1}{2}V\angle-\frac{4\pi}{3}$ $\vec{V_1} = \frac{1}{2}V\angle 0$ $\vec{V_2} = \frac{1}{2}V\angle-\frac{2\pi}{3}$
Phase to phase	$\vec{V_0} = 0$ $\vec{V_1} = \frac{1}{2}V\angle 0$ $\vec{V_2} = \frac{1}{2}V\angle 0$	$\vec{V_0} = 0$ $\vec{V_1} = \frac{1}{2}V\angle 0$ $\vec{V_2} = \frac{1}{2}V\angle 0$
Three phase	$\vec{V_0} = 0$ $\vec{V_1} = 0$ $\vec{V_2} = 0$	$\vec{V_0} = 0$ $\vec{V_1} = 0$ $\vec{V_2} = 0$

Voltage unbalances may be different from those shown in table C–1 if the aforementioned assumptions do not hold. However, these assumptions are justified and sufficient for the development of the control stategies in this thesis.

APPENDIX D
Active and Reactive Power Flow

The main goal of a network is of course to transmit electrical power from the generation and to distribute it to the load centers. This appendix biefly describes how active and reactive power flow along a transmission line. A simple two bus network is shown in figure D–1. The direction of current flow establishes a con-

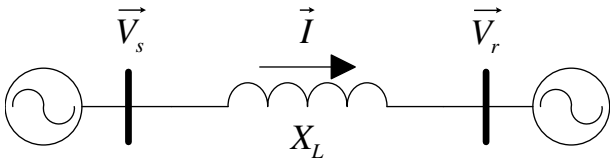

Figure D–1: Transmission line and active/reactive power flow

vention where the bus from which the current is originating is considered as the sending end, while the bus to which the current is flowing is considered as the receiving end. This convention also means that generated power has a positive sign, and absorbed power has a negative sign. For the purpose of the analysis presented here, the line is considered as a short lossless line and is therefore modeled by a simple reactance X_L. The voltages at the sending end and receiving end are

$$\vec{V_s} = V_s \angle \phi_s \tag{D.1}$$

$$\vec{V_r} = V_r \angle \phi_r \tag{D.2}$$

The apparent power at the receiving end is therefore

$$S_r = \vec{V_r}\vec{I}^* \tag{D.3}$$

Expressing the current in terms of voltages and line reactance, we get

$$\vec{I} = \frac{V_s \angle \phi_s - V_r \angle \phi_r}{\jmath X_L} \tag{D.4}$$

and the expression for apparent power becomes

$$S_r = V_r \angle \phi_r \left(\frac{V_s \angle -\phi_s - V_r \angle -\phi_r}{-\jmath X_L} \right) \tag{D.5}$$

$$= \frac{V_r V_s \angle (\phi_r - \phi_s) - V_r^2 \angle 0}{-\jmath X_L} \tag{D.6}$$

$$= \jmath \frac{V_r V_s \angle \delta}{X_L} - \jmath \frac{V_r^2 \angle 0}{X_L} \tag{D.7}$$

The active power at the receiving end of the line is therefore the real part of (D.7) and the reactive power is the imaginary part. For simplicity, the difference in the sending end voltage angle and receiving end voltage angle $(\phi_r - \phi_s)$ is replaced by δ.

$$P_r = Re \left(\jmath \frac{V_r V_s \angle \delta}{X_L} \right) \tag{D.8}$$

$$= - \frac{V_r V_s sin(\delta)}{X_L} \tag{D.9}$$

$$Q_r = Im \left(\jmath \frac{V_r V_s \angle \delta}{X_L} \right) - \jmath \frac{V_r^2 \angle 0}{X_L} \tag{D.10}$$

$$= \frac{V_r V_s cos(\delta)}{X_L} - \frac{V_r^2}{X_L} \tag{D.11}$$

Assuming that δ is small, (D.9) and (D.11) become

$$P_r \approx -\frac{V_r V_s \delta}{X_L} \tag{D.12}$$

$$Q_r \approx \frac{V_r V_s}{X_L} - \frac{V_r^2}{X_L} = \frac{V_r(V_s - V_r)}{X_L} \tag{D.13}$$

These results show that the difference in phase angle between the sending end voltage and the receiving end voltage has a large impact on the active power flow on the line whereas it is the diffence in voltage magnitudes that has an impact on the reactive power flow. The implication of this is that by controlling the reactive power flow, the voltage magnitude at the receiving end can be controlled without having a significant impact on the active power flow.