A SINGLE - PHASE CYCLOCONVERTER

by

T M Hamblin, B. Eng (McGill)

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Department of Electrical Engineering
McGill University,
Montreal, Canada

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ABSTRACT

The three-phase to single-phase cycloconverter has a maximum continuous rating of 250 Vdc at 30 Adc and operates without circulating current (figure 8 current) between its six-pulse thyristor bridges. The voltage biased cosine wave technique is used for phase-control. Phase forward and phase back limit pulses are superimposed on each cosine wave. An "alpha blanking" circuit prevents the formation of spurious gating pulses in the range of $180^\circ < \alpha < 360^\circ$. A new, high-speed, current zero detector is presented which depends upon continuous monitoring of the voltage across each thyristor in the cycloconverter. There are two types of circulating current elimination logic suitable for 1) resistive or lagging loads, and 2) leading, resistive, or lagging loads. When the cycloconverter has other than a dc armature load, auxiliary gating pulses are supplied to the oncoming converter to prevent gaps in the load current. The transfer characteristics of the bridges have a dead band between them to prevent current surges after crossover when the cycloconverter is used as a dc armature supply. A single converter with a four thyristor reversing switch has been used as a cycloconverter at 40 Hz.

ABREGE

Le cyclo-convertisseur à commutation naturelle triphasé / monophasé peut fournir 30 A cc à 250 V et fonctionne sans circulation de courant entre ses ponts de thyristors à six impulsions. Le circuit de commande utilise la technique de "l'onde cosinusoïdale avec polarisation de tension" pour obtenir le terme "arc cosinus" et ainsi rendre le gain constant. Les impulsions de restriction de l'angle de retard sont superposées sur chaque onde cosinusoïdale. Toutes les fausses impulsions de commande créées dans l'intervalle de $180^{\circ} < \alpha < 360^{\circ}$ sont supprimées. L'auteur présente un nouveau détecteur de "courant zéro" à haute vitesse dont le principe est la surveillance continuelle de la tension aux bornes de chaque thyristor du convertisseur. Il y a deux sortes de logique électronique d'élimination de circulation de courant: 1) pour les charges résistives ou inductives 2) pour les charges capacitives, résistives ou inductives. Quand la charge du cyclo-convertisseur n'est pas celle imposée par l'induit du moteur à cc, des impulsions auxiliaires sont envoyées au convertisseur à l'amorçage pour prévenir des "trous" dans le courant de charge. Quand le cyclo-convertisseur alimente l'induit d'un moteur à cc, les courbes de transfert caractéristiques des ponts sont espacées (système à bande morte) afin de prévenir des surintensités transitoires après inversion. Un seul convertisseur avec quatre thyristors fonctionnant en inverseur du courant a été utilisé comme cyclo-convertisseur pour fournir une fréquence secondaire de 40 Hz.

ACKNOWLEDGEMENTS

This thesis and its experimental work has taken a long time to complete. During this period I have become gratefully indebted to many people both in and out of the McGill Electrical Engineering Department.

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This project would not have been possible without the help of the technicians of the Department. Before his retirement Jack Turley assisted me with my first construction work. John Foldvari helped me with the machine shop work throughout the project. The major component blocks of the second converter, and all the portions of the reversing switch were built to my specifications by technicians George Hexner, Peter Conroy, Jack Krabbendam, and Walter Taal. I appreciate their help and I admire their constructional abilities. My thanks go to Igor Borissov, senior technician, for taking all the Equipment Photographs and for preparing slides and enlargements for most of the Figures in this thesis.

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CHAPTER I

AN INTRODUCTION TO THE CYCLOCONVERTER

1.1 Definition and Basic Configuration

Modern usage of the term cycloconverter denotes an ac to ac static frequency changer without an intermediate dc link utilizing line commutation of controlled rectifiers. The most common cycloconverter building block is the anti-parallel combination of two controlled rectifier connections. Figure 1.1 illustrates the anti-parallel combination of both one-way and two-way (three-phase) rectifier connections. If suitably controlled thyristor gating circuitry is provided, a single basic building block may be used directly as a single-phase output cycloconverter. Or, as will be described in Chapter III, multiple, anti-parallel combinations may be combined to form a multiple phase output cycloconverter.

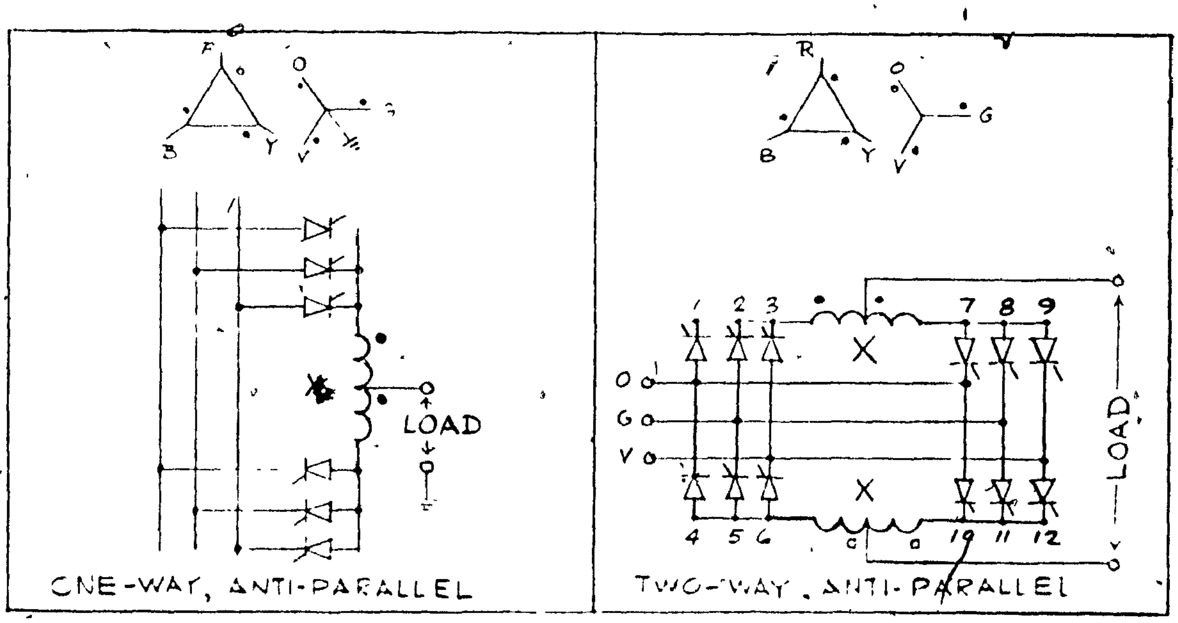

FIGURE 1.1. BASIC THREE-PHASE TO SINGLE PHASE CYCLOCONVERTER BUILDING BLOCKS

1.2 The Origin of the Cycloconverter

The first practical form of cycloconverter, using grid-controlled mercury arc rectifiers, was described in a British patent application lodged by Hazeltine in 1923. Hazeltine's scheme converted three-phase, 50 Hz voltages to four-phase voltages at 10 Hz.[1] The first commercial applications were in the conversion of three-phase, 50 Hz supplies to 16 2/3 Hz single-phase at 10 to 15 kV for railway electrification. Both envelope cycloconverters and grid-controlled (phase-controlled) cycloconverters were used.

The envelope cycloconverter, now extinct, was suitable for use only with resistive, single-phase loads. Any reactive power requirements on the single-phase side had to be supplied by other means (such as a single-phase synchronous condenser). The input to output frequency changing ratio was fixed by the rectifier and transformer configuration (usually at 3:1). Regeneration (inversion) of power from the single-phase side to the three-phase side was not possible. Transformer tap changing was the only method of voltage control.[2,3]

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[1] H. Rissik, The Fundamental Theory of Arc Convertors (London: Chapman and Hall Ltd., 1939), p. 270.

[2] Ibid., pp. 240-258.

[3] S. Miyairi and M. Shioya, "Gate Control Circuit for Thyristor Cyclo-convertor," Electrical Engineering in Japan (IEEE Translation), Vol. 88, No. 12, 1968, pp. 31-32.

However, the grid-controlled (phase-controlled)[4] cycloconverter utilizing grid-controlled mercury arc rectifiers did permit the use of reactive loads without need for any added reactive power source on the single-phase side. The frequency ratio was adjustable simply by changing the reference frequency supplied to the grid-control circuitry. This meant that for a given cycloconverter controlled-rectifier and transformer configuration, the ratio could be changed from 50 Hz:16 2/3 Hz (that is, 3:1) to 50 Hz:20 Hz (that is, 5:2) simply by changing the grid-control reference frequency from 16 2/3 Hz to 20 Hz. Continuous regeneration of power from the single-phase side to the three-phase side occurred when the power factor angle of the single-phase side exceeded 90°. In addition, smooth voltage control was possible by changing the amplitude of the reference frequency supplied to the grid-control circuitry. The term cycloconverter, as defined in Section 1.1, applies to the grid-controlled (or phase-controlled) cycloconverter rather than to the envelope cycloconverter. The latter will not be further mentioned in this thesis.

The cycloconverter, with its mercury arc type of controlled rectifiers, gradually fell from popularity. Its decline was principally due to the limited power inversion capability of the mercury arc rectifiers themselves, and to the bulk and relative complexity of the systems at that time. However, a body of theory was developed that analyzed cycloconverter operation. The classic reference in English

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[4] Phase-controlled operation of mercury arc rectifiers has traditionally been called grid-control.

for cycloconverter theory (and polyphase rectifier connections) was H. Rissik's book published in 1939.[5] The standard reference in German for that period is in an article by J. von Issendorf published by Siemens Works.[6] A number of other cycloconverter references of the 1930's are listed in the bibliographies of articles by R.J. Bland[7] and L.J. Lawson[8].

1.3 The Return of the Cycloconverter

In 1957 General Electric announced the development of a solid state controlled rectifier (SCR) now known as the thyristor. Interest in the long-dormant cycloconverter concept revived as thyristor voltage, current, and reliability ratings quickly rose. The small size and physical soundness of the thyristor made it naturally suited for its first new cycloconverter applications in three-phase to three-

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[5] H. Rissik, op. cit., Chaps. X, XI, XII.

[6] J. von Issendorf, "Der Gestewerte Umrichter [The Controlled Static Frequency Changer]", Wissenschaftliche Veroffentlichungen, Siemens-Werken, Vol. 14, Pt. III, 1935, pp. 1-31.

[7] R.J. Bland, "Factors Affecting the Operation of a Phase-Controlled Cycloconvertor," Proc. IEE, Vol. 11A, No. 12, December 1967, pp. 1908-1916.

[8] L.J. Lawson, "The Practical Cycloconverter," IEEE Transactions on Industry and General Applications, Vol. IGA-4, No. 2, March/April 1968, pp. 141-144.

phase aircraft variable-speed, constant-frequency (VSCF) supply schemes.[9,10] Closed-loop with controlled-slip speed control of three-phase induction motors in traction service was the next important application.[11] At the same time a number of manufacturers were developing circulating-current-free reversing drives which were essentially three-phase to single-phase cycloconverters.[12,13] Chapter III will trace the development of the modern cycloconverter by reviewing a selected group of articles published in English in Europe and North America since 1959.

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[9] K.M. Chirgwin and L.J. Stratton, "Variable-Speed, Constant-Frequency Generator System for Aircraft," AIEE Transactions, Pt.II, (Applications and Industry), Vol. 78, November 1959, pp. 304-310.

[10] K.M. Chirgwin, L.J. Stratton, and J.R. Toth, "Precise Frequency Power Generation from an Unregulated Shaft," AIEE Transactions, Pt. II, (Applications and Industry), Vol. 79, January 1961, pp. 442-451.

[11] Walter Slabiak and Louis J. Lawson, "Precise Control of a Three-Phase Squirrel-Cage Induction Motor Using a Practical Cycloconverter," IEEE Transactions on Industry and General Applications, Vol. 1GA-2, No. 4, July/August 1966, pp. 274-280.

[12] Franz Wesselak, "Thyristor Converters with Natural Commutation," Siemens Review, No. 12, December 1965, pp. 405-410.

[13] L.F. Stringer, "Thyristor D-C Drive Systems for a Non-ferrous Hot Line," IEEE Industrial Static Power Control Conference Record, November 1965, pp. 40-56.

1.4 Thesis Justification and Outline

The historical development in Chapter III will reveal that the circulating-current-free cycloconverter is now a well known device to many firms working in the aerospace, military, and industrial drive systems fields. However, the core of this thesis was first prepared as a conference paper [14, 15] in the spring of 1970 for presentation at the October, 1970 IEEE Industry and General Applications Group Annual Meeting. Many papers had alreayd been published which demonstrated cycloconverter operation in various drive systems. But of course, these papers tended to be guarded about the details of the proprietary control circuitry which were vital to the smooth operation of their cycloconverters. The purposes of the conference paper by T. Hamblin and T. H. Barton was to discuss cycloconverter control circuitry problems, and to describe some particular solutions using a practical three-phase to single-phase circulating-current-free cycloconverter as an example.

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[14] T. M. Hamblin and T. H. Barton, "Cycloconverter Control Circuits," _IEEE Industry and General Applications Group Annual Meeting Conference Record,_ October, 1965, pp. 559-570.

[15] T. M. Hamblin and T. H. Barton, "Cycloconverter Control Circuits," _IEEE Transactions on Industry Applications,_ Vol. IA-8, No. 4, July/August 1972, pp. 443-453.

The intent of the paper, and of the work leading to this thesis, has been definitely non-mathematical for two reasons. First, the cycloconverter transformer and thyristor sizing requirements could be reasonably well estimated from well known exact analyses of polyphase converters under steady-state conditions which were available in books by J. Schaeffer[16] and H. Rissik.[17] Both H. Rissik[18] and J. von Issendorf[19] had published approximate performance analyses of cycloconverters with circulating current. Hence a new mathematical analysis was not really necessary before investigating the control circuitry problems of a cycloconverter. Second, the problem of doing more than an approximate analysis of cycloconverter waveform appeared formidable if the three parameters of frequency, output voltage, and output current displacement factor were to be varied over their full ranges. Hindsight shows that the complexity of successful analytic or numeric Fourier analyses of the waveforms followed by a logical unification of the results would be an accomplishment worthy of presentation as a book or as a doctoral thesis. Indeed B. R. Pelly and his colleague L. Gyugyi demonstrated just that with the publishing in 1971 of Pelly's book[20] and

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[16] J. Schaefer, Rectifier Circuits - Theory and Design (New York: John Wiley and sons, 1965) pp. 347.

[17] H. Rissik, op. cit. [18] Ibid., pp. 265-270.

[19] J. von Issendorf, op. cit.

[20] B.R. Pelly, Thyristor Phase - Controlled Converters and Cycloconverters - Operation, Control, and Performance (New York: Wiley - Interscience, 1971) pp. 434.

Gyugyi's thesis.[21] The book covered the topics stated in its title in such a thorough, organized manner that it became a standard reference text in the thyristor drive systems field almost immediately after its release by Wiley Interscience at the start of 1971.

The conference paper by T. M. Hamblin and T. H. Barton was presented in October, 1970 and hence was not influenced by Pelly's book nor by Gyugyi's thesis. Similarly the vast majority of the experimental work to be described in this thesis, as well as some of the writing itself, was finished in 1970. However the completeness of Pelly's description of the operation, control, and performance of converters and cycloconverters has had a definite influence on the contents of this thesis as it is now submitted. These areas of influence will be specifically acknowledged as they appear in the text.

Another book on cycloconverters written by W. McMurray[22] was discovered by T. M. Hamblin as this thesis was being put into its final draft form. McMurray's book is somewhat complementary to Pelly's and references will be made to it from time to time in the text.

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[21] L. Gyugyi, "Generalized Theory of Static Power Frequency Changers" (Ph. D. thesis, University of Salford, October, 1970).

[22] W. McMurray, The Theory and Design of Cycloconverters (Cambridge, Massachusetts: The MIT Press, 1972) pp. 165.

Chapter II of this thesis introduces the basic operation of cycloconverters by describing the phase-control of antiparallel converter bridges and the problem of limiting the magnitude of the circulating current between them. Chapter III is a historical review of how various companies approached the design of cycloconverter and reversing converter drive systems between 1959 and 1970. This step-by-step tracing of the development of the field following the introduction of the thyristor by General Electric in 1958 is admittedly lengthy. But hopefully it gives the credits due to the many contributors to the field and also places this thesis in the proper perspective to the papers discussed. Chapter IV covers the thyristor gating, control, and protection circuitry used in a three-phase to single-phase cycloconverter with circulating current. The necessary logic and detection circuits added to the cycloconverter to successfully eliminate the circulating current are discussed in Chapter V. Two innovations made during the experimental work are described in this chapter:

1. High speed current zero-detection (so as to permit circulating current elimination) by continuous monitoring of the existence of voltage across each of the thyristors of the cycloconverter.
2. Auxiliary gate pulsing supplied to thyristors in the on-coming half of the cycloconverter to eliminate gaps in the output

current waveform immediately after crossover by the interlocking logic. Chapter V demonstrates cycloconverter operation with three types of loads: a single-phase induction motor under open loop control, a single-phase synchronous motor under open loop control, and a dc motor under closed loop control. In addition this chapter contains the details of a three-phase to single-phase cycloconverter that uses only one bridge combined with a dpdt, thyristorized reversing switch. The final chapter (VI) contains a résumé of the previous chapters with some suggestions for future work.

CHAPTER II

BASIC CYCLOCONVERTER OPERATION

2.1 Introduction

This chapter will describe the bias-shift method of phase-control generally used in most cycloconverter schemes. In addition, the problem of controlling the amplitude of the circulating current passing between the anti-parallel converters will be discussed.

2.2 Average Output Voltage Versus Firing Angle

The presumption is made that the reader is familiar with the phase-controlled rectifier operation of one-way and two-way rectifier connections. Two recent articles,[1,2] and books by Schaefer[3] and Pelly[4] explain phase-control.

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[1] A. Ludbrook and R.M. Murray, "A Simplified Technique for Analyzing the Three-Phase Bridge Rectifier," IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June 1965, pp. 182-187.

[2] E.E. Rabek, "Characteristics of AC Powered DC Motor Controls Using Three and Six Controlled Elements," IEEE Transactions on Industry and General Applications, Vol. IGA-5, No. 2, March/April 1965, pp. 187-191.

[3] J. Schaefer, Rectifier Circuits (New York: Wiley, 1964), pp. 75-86.

[4] B.R. Pelly, Thyristor Phase-Controlled Converters and Cycloconverters Operation, Control and Performance (NewYork: Wiley Interscience, 1970) pp. 27-54.

Figure 1.1 showed the anti-parallel connection of one-way and two-way rectifier circuits. Phase-controlled gating of the thyristors, combined with the anti-parallel interconnection of the circuits, permits smooth control of the amplitude and polarity of the voltage applied to the load. The anti-parallel interconnection allows bi-directional current flow in the load with uni-directional flow through each converter. The relationship between the firing angle α and the average output voltage V_d of a converter operating with continuously flowing load current is well known,[5,6] and can be shown to be

$$V_d = (\sqrt{2}\,E\,\frac{p}{\pi}\sin\frac{\pi}{p})\cos\alpha = V_{do}\cos\alpha \qquad (2.1)$$

where $\sqrt{2}\,E$ = peak instantaneous output voltage and p = pulse number.

For a three-phase, one-way rectifier,

$\sqrt{2}\,E$ = peak line-neutral voltage, and $p = 3$.

And for a three-phase, two-way rectifier (bridge circuit)

$\sqrt{2}\,E$ = peak line-to-line voltage, and $p = 6$.

To ensure that the two converters operated in anti-parallel (one rectifying, one inverting) have balanced output voltages, their firing angles should be supplementary

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[5] J. Schaefer, op. cit., pp. 75-86.

[6] H. Rissik, The Fundamental Theory of Arc Converters (London: Chapman and Hall Ltd., 1939), p. 183.

as is shown below.

$$V_{d1} = V_{do}\cos\alpha = -V_{d2} = V_{do}\cos\beta \text{ provided } \beta = 180^{\circ} - \alpha \qquad (2.2)$$

2.3 The Circulating Current Problem

If the firing angles are not truly supplementary then a dc current will circulate between the converters if there is a positive average voltage difference between them. This current can be very large, even through the firing angle error causing it is small, because the circulating current avoids the load and is limited only by the low series resistance of the converters and circulating current limiting reactor (labelled X in Figure 2.3).

Even if the average converter voltages are held equal, there will still be an inherent, alternating voltage difference between the converters due to the shape of their phase-controlled output voltages. The purpose of the circulating current limiting reactor connected between the converters is to support this sawtooth shaped voltage difference waveform. The reactance value is chosen so as to limit the 360 Hz circulating current pulses due to the alternating voltage difference to some fraction of the normal full load current.

Figure 2.1 and 2.2 are photographs of these waveforms for firing angles of approximately $\alpha = 60$ and $\beta = 120^{\circ}$ under no-load conditions. Figure 2.3 shows the interconnection of the converters and where each trace was taken. Note that the voltage appearing at the center-tap of the reactor (Trace 3, Figure 2.2) is the instantaneous average of the two converter voltages because the reactor

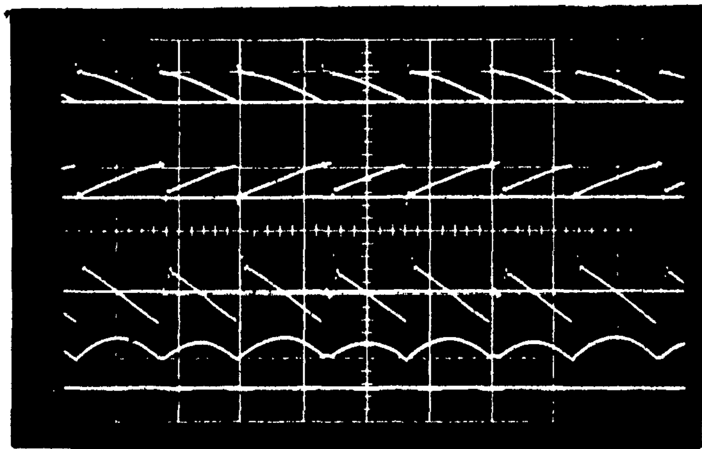

FIGURE 2.1. CIRCULATING CURRENT AND VOLTAGE AT NO LOAD

Sweep = 5 ms / cm ; $V_c \simeq 5.0$ V ; $\alpha \simeq 60^\circ$, $\beta \simeq 120^\circ$

Trace 1 : V_o , P converter ; scale = 420 V / cm

Trace 2 : V_o , N converter ; scale = 420 V / cm

Trace 3 : V_d , across reactor ; scale = 420 V / cm

Trace 4 : I_c , circulating current ; scale = 5 A / cm

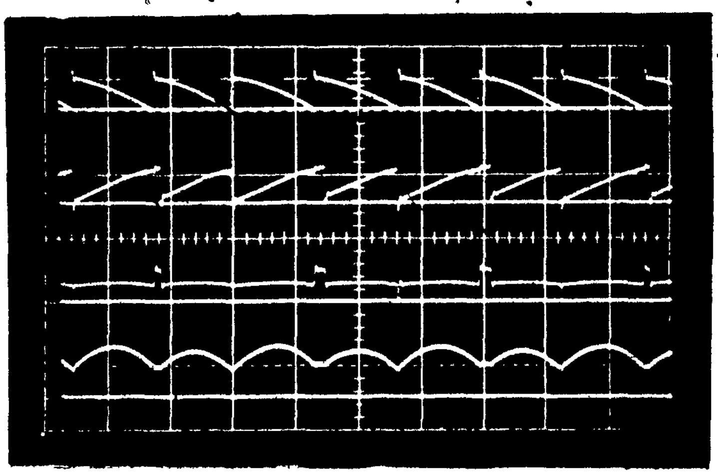

FIGURE 2.2. NO LOAD VOLTAGE WITH CIRCULATING CURRENT

Sweep = 5 ms / cm ; $V_c \simeq 5.0$ V ; $\alpha \simeq 60^\circ$, $\beta \simeq 120^\circ$

Trace 1 : V_o , P converter ; scale = 420 V / cm

Trace 2 : V_o , N converter ; scale = 420 V / cm

Trace 3 : V_l , at reactor center-tap ; scale = 420 V / cm

Trace 4 : I_c , circulating current ; scale = 5 A / cm

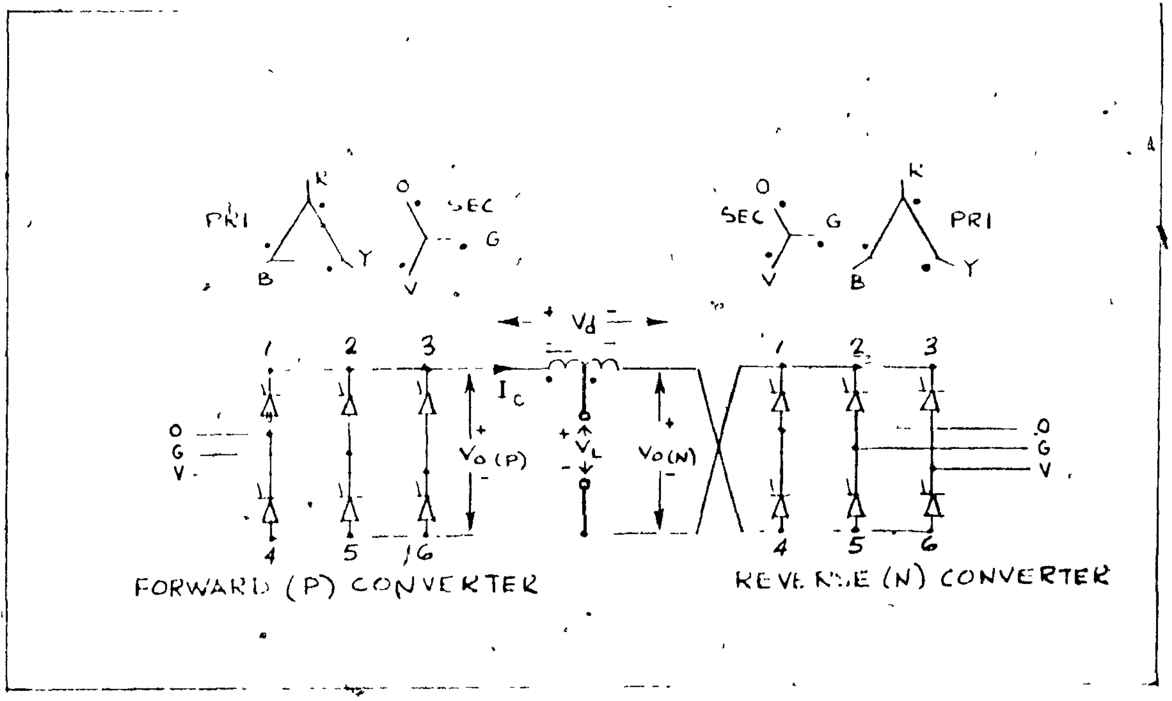

FIGURE 2.3. CONNECTION DIAGRAM FOR FIGURES 2.1 AND 2.2

acts as a voltage divider. Observing that the circulating current is definitely continuous (Trace 4 Figures 2.1 and 2.2) implies that the firing angles were not perfect. Theoretically at $\alpha = 60^{\circ}$ and $\beta = 120^{\circ}$ the no load circulating current should be on the edge of discontinuity, and the reactor center-tap voltage should be uniformly cusp-shaped.[7]

Pelly has described a third component which he has named the self-induced circulating current.[8] The requirement of conservation of flux linkages in the circulating current limiting reactor itself may induce a free-wheeling circulating current through the reactor and the anti-parallel converters. This self-induced circulating current will be further discussed in Section 4.12 of Chapter IV.

2.4 Bias-Shift Control of Gating

Equation (2.1) for the average output voltage of a phase controlled converter operating with continuous current was $V_d = V_{do} \cos \alpha$. Preferably the input control voltage to average output voltage ratio should be a constant relation such as:

$$V_d = K_1 V_c \tag{2.3}$$

[7] B. R. Pelly, op. cit., p. 130.

[8] B. R. Pelly, op. cit., pp. 134-144 and 156-161

where V_c = input control voltage.

A technique for obtaining such a linear relation was originally developed for grid-controlled arc converters by Mittag in 1925.[9] Rissik refers to this technique as "bias-shift control". The method consists of adding a "cosine wave" to the control voltage. Gate pulsing circuitry generates a pulse starting at the instant that the sum of the two waveforms changes polarity (crosses zero). One cosine wave must be supplied for each thyristor in a converter. The phasing of each cosine wave must be such that for zero control voltage, the firing angle for its particular thyristor is delayed by 90° ($\alpha = 90^\circ$). That is, zero control voltage ($\alpha = 90^\circ$) should yield zero average output voltage ($\cos 90^\circ = 0$). Due to the linear dc transfer function of the cycloconverter with bias-shift control, a sinusoidal control voltage at a particular frequency will yield an output voltage with a sinusoidally varying average value at that same frequency. To obtain a three-phase output, three cycloconverter building blocks are used. Each block is supplied with a control voltage that is one phase of a three-phase set at the desired output frequency.

Studying the phase relationships of Figure 2.4 will explain how the bias-shift control technique might be applied to a cycloconverter building block using two, anti-parallel, one-way connected converters. The output of converter P is the voltage from point A to neutral point n . The voltage from point B to

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[9] H. Rissik, op. cit., p. 181 and p. 263.

point n is the output of converter N. The converter output voltages are shown for the 90° phase back condition. This corresponds with the condition of zero control voltage added to each cosine voltage on the second trace. It is assumed that the firing pulse generators for converter P detect the positive going crossings of cosines P1, P2, and P3. The same cosine voltages (but relabelled N1, N2, and N3) are monitored by negative crossing detectors to generate firing pulses for converter N. In total, three cosine voltages, three summer amplifiers, three positive crossing detectors, and three negative crossing detectors are needed to synchronize the cycloconverter firing pulses.

The third trace illustrates the effect of control voltage on the timing for the thyristors tied to phase 1 of converters P and N. Raising the control voltage phases forward the firing pulse(s) of converter P while phasing back the firing pulse(s) of converter N. The phase forward and phase back movement keeps the values of the firing angles supplementary as will now be shown. Using the variables defined in Figure 2.4:

$$V_c = V_{cm} \sin\theta_P = V_{cm} \cos(90^{\circ} - \theta_P) = V_{cm} \cos(\alpha_P). \tag{2.4}$$

Also,

$$V_c = V_{cm} \sin\theta_N = V_{cm} \cos(90^{\circ} - \theta_N) = V_{cm} \cos(180^{\circ} - \alpha_N) \tag{2.5}$$

or

$$V_{cm} \cos\alpha_P = V_{cm} \cos(180^{\circ} - \alpha_N) . \tag{2.6}$$

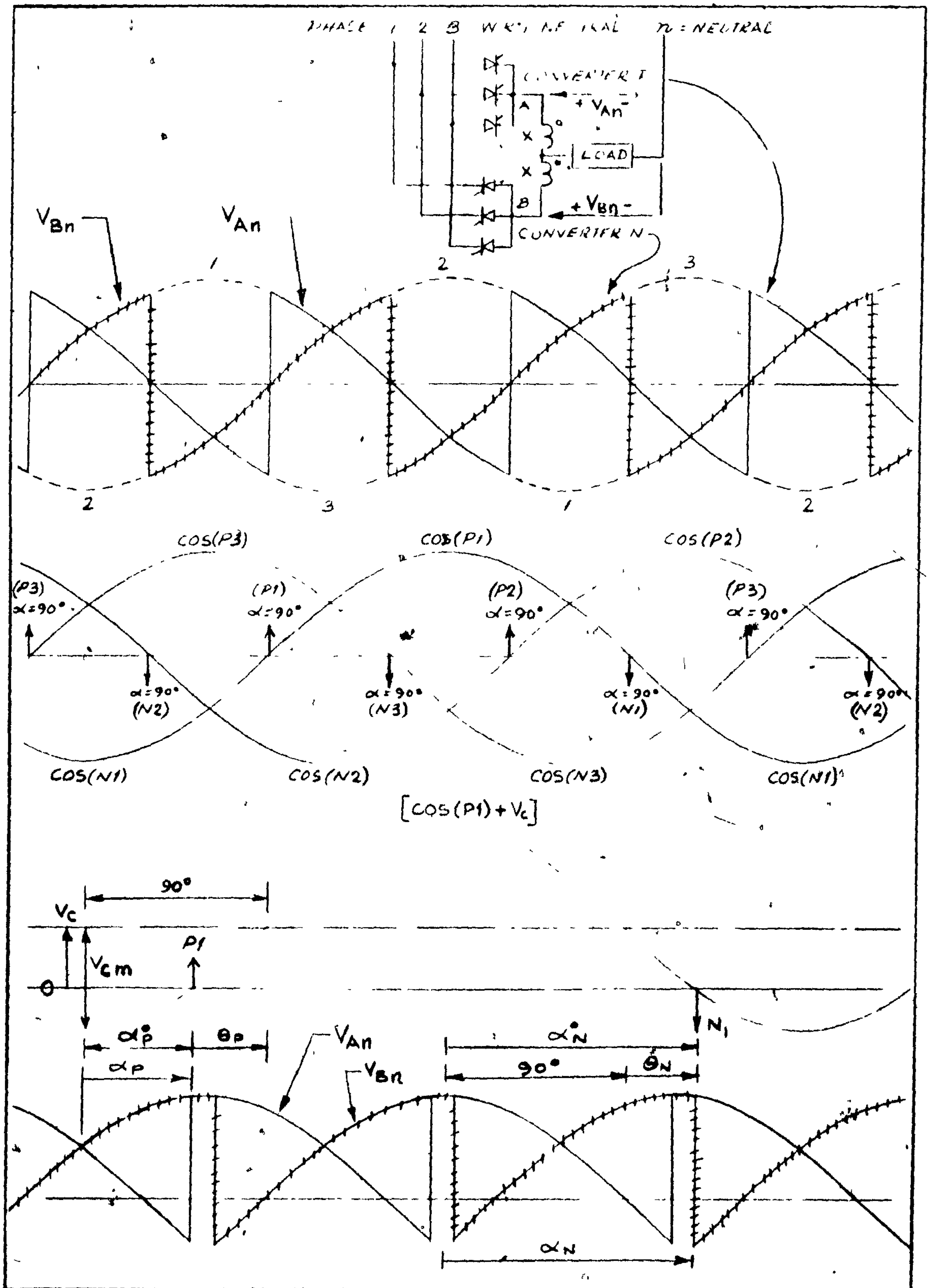

FIGURE 2.4. BIAS-SHIFT CONTROL OF GATING

The significant solution is $\alpha_P = 180 - \alpha_N$ or $\alpha_P + \alpha_N = 180^\circ$. Hence, the firing angles of the two converters are supplementary. For a steady value of control voltage V_c and continuous current flow, the average output voltage of converter P (from A to neutral) will be

$$V_{d(An)} = V_{do} \cos \alpha_P = V_{do} \cos \cos^{-1} \frac{V_c}{V_{cm}} = V_{do} \cdot \frac{V_c}{V_{cm}} \tag{2.7}$$

Similarly, the average output voltage of converter N (from neutral to B) will be

$$V_{d(nB)} = V_{do} \cos(180 - \alpha_P) = - V_{do} \cos \alpha_P = -V_{do} \cdot \frac{V_c}{V_{cm}} \tag{2.8}$$

But, the converters are connected in anti-parallel, so that the average output voltage of converter N from (B to neutral) will be

$$V_{d(Bn)} = V_{do} \cdot \frac{V_c}{V_{cm}} = V_{d(An)} . \tag{2.9}$$

Consequently, the average output voltages are equal and have a linear relation to the control voltage V_c, assuming that both converters are in continuous conduction.

Trace 4, of Figure 2.4 represents the output voltages of the converters (V_{An}, V_{Bn}) corresponding to the value of control voltage in trace 3.

An alternate scheme to obtain supplementary firing angles and a linear input to output relationship uses six cosine voltages, six summing amplifiers, and six positive-crossing detectors. Three of each item mentioned are used in each converter. An additional unity gain, inverting amplifier supplies $(-V_c)$ to the input of one of the converters. Since the converters are in anti-parallel, their average output voltages will be equal.

2.5 Oscilloscope Photographs of Cycloconverter Operation

Figure 2.5 and 2.6 respectively are oscillograph photographs of a three-phase to single-phase cycloconverter operated both with and without circulating current. The basic building block is shown in Figure 2.7 for the circulating current case. For operation without circulating current, necessary logic and detection circuitry for circulating current elimination was provided. Circulating-current-limiting reactors were not needed, but current limiting fuses were inserted in the interconnection between the converters as shown in Figure 2.8 .

The four oscilloscope traces for the circulating-current case of Figure 2.5 are (1) the output voltage of the P converter, (2) the output voltage of the N converter, (3) the load voltage at the center-tap of the reactor, and (4) the load current.

The traces for the circulating-current-free case of Figure 2.6 are (1) the control voltage at 0.9 p.u., (2) the load voltage, (3) the load current, and (4) the logical NOR of the firing pulses supplied to the P converter. For both photographs the control voltages were 0.9 p.u. peak at 30 Hz. and the load was approximately (8.7 + j13.3) ohms at that frequency. The unsaturated impedance of

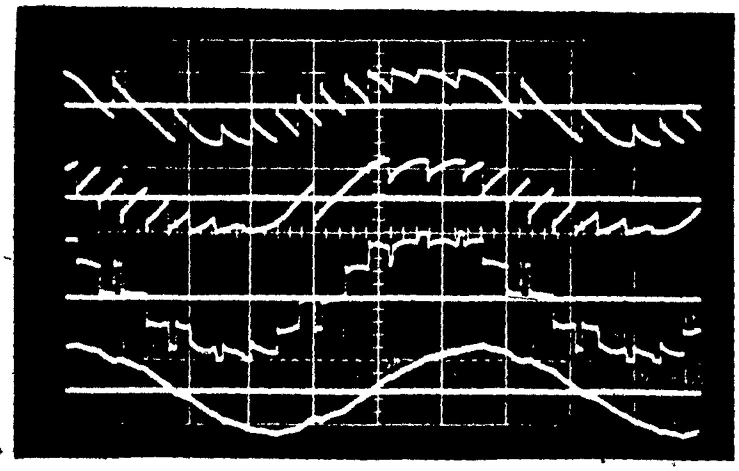

FIGURE 2.5. WAVEFORMS WITH CIRCULATING CURRENT

Sweep = 5 ms/cm; $V_c = 18V_{pp}$ at 30 Hz.

Trace 1: V_O, P converter; scale = 420V/cm

Trace 2: V_O, N converter; scale = 420 V/cm

Trace 3: Reactor center-tap voltage; scale = 200 V/cm

Trace 4: Load current; scale = 20 A/cm

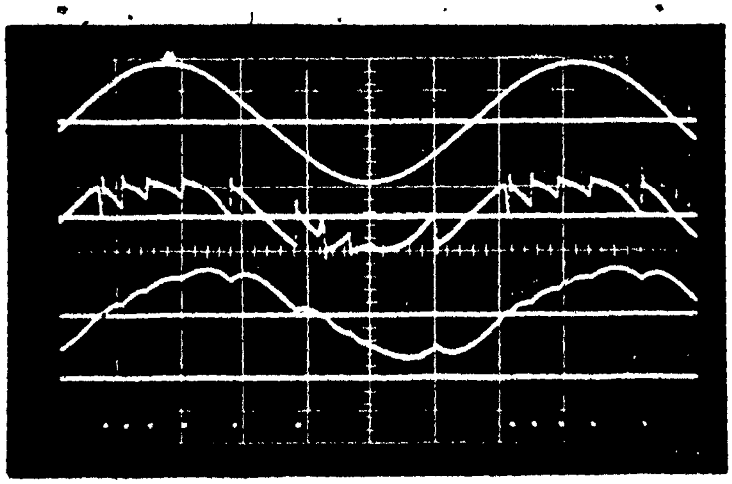

FIGURE 2.6. WAVEFORMS WITHOUT CIRCULATING CURRENT

Sweep = 5 ms/cm; $V_c = 18\ V_{pp}$ at 30 Hz.

Trace 1: control signal, V_c; scale = 10 V/cm

Trace 2: Load Voltage; scale = 420 V/cm

Trace 3: Load Current; scale = 20 A/cm

Trace 4: Firing pulse detector, P converter; scale = 10 V/cm

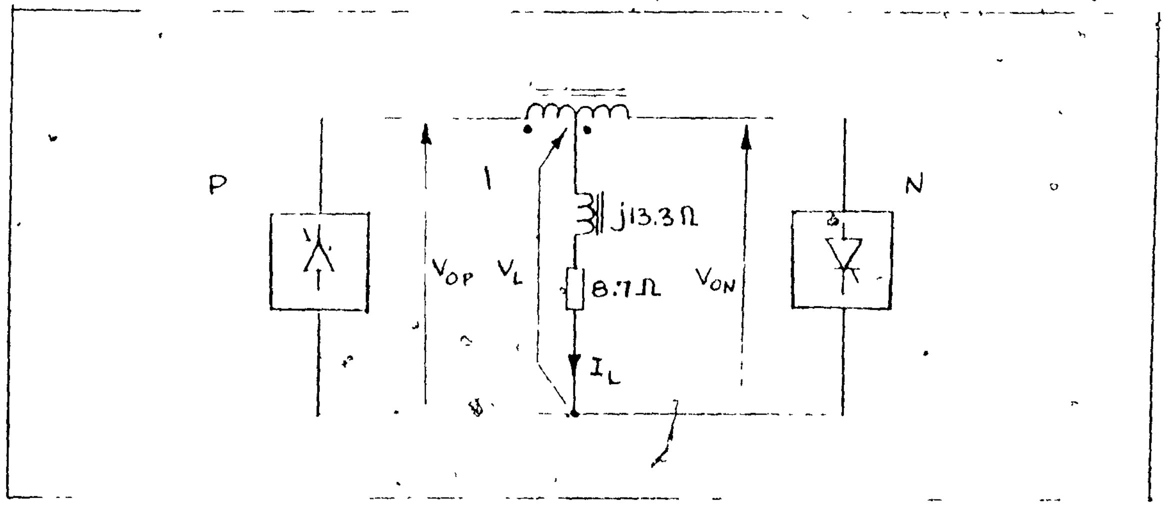

FIGURE 2.7. CONNECTION DIAGRAM FOR FIGURE 2.5

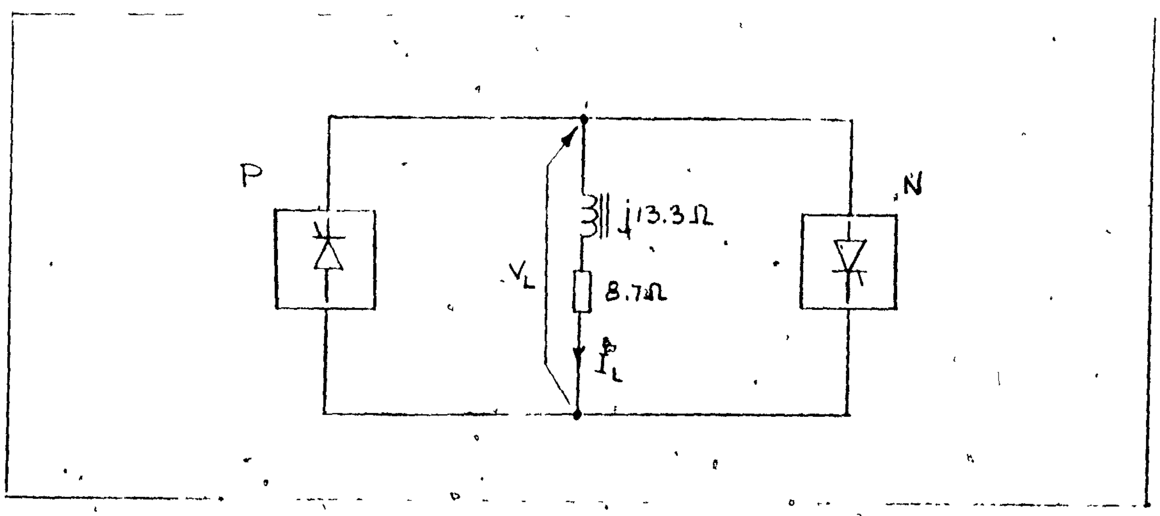

FIGURE 2.8. CONNECTION DIAGRAM FOR FIGURE 2.6

the reactor to the circulating current was approximately (.86 + j248) ohms at 360 Hz. Note that because of the self-induced circulating current caused by the reactor (see Section 4 9), the impedance of the reactor appeared to be only (.43 + j0) ohms when viewed from the load. Then, maintaining identical control voltage waveforms and load impedances for Figures 2.5 and 2.6 lead to almost identical load current amplitudes The load current in Figure 2.5 is smoother than in Figure 2.6 because the reactor instantaneously averaged the converter input voltages yielding an output voltage which has been shown[10] to have a harmonic content lower than that of either converter voltage by itself. Trace 4 of Figure 2 6 is the output of the positive converters firing pulse detector NOR logic showing that the firing pulses in the positive converter were suppressed whenever the negative converter was in operation.

2.6 Summary

The anti-parallel parallel connection of the converters in the basic cycloconverter building block permits reversal of the load current. The bias-shift method of phase-control provides a linear dc transfer function as long as the load current is continuous. In addition this method produces supplementary firing angles in the two converters so that their average output voltages are in balance. However, slight deviations from true supplementary operation may cause large dc circulating currents to flow. The phase-controlled operation of the cycloconverter generates a sawtooth voltage waveform that (despite its

[10] B. R. Pelly, op. cit, pp. 311-313.

zero average value) forces a pulsating dc current to circulate between the converters. The magnitude of this circulating current is normally limited by a reactor (or reactors) between the converters However the presence of the reactor itself produces a self-induced circulating current which freewheels through the the reactor and the anti-parallel converters. As the next chapter will show, the modern approach has been to completely eliminate the circulating current by means of detection and logic circuitry which permits only the alternate operation of the two converters comprising one cycloconverter building block.

CHAPTER III

THE DEVELOPMENT OF THE MODERN CYCLOCONVERTER

3.1 Introduction

As mentioned in Chapter I, Hazeltine applied in 1926 for a patent to what might be considered the ancestor of the modern cycloconverter. Three-phase to single-phase cycloconverters for single-phase railway traction motor supplies were built during the Twenties and Thirties. But, the use of cycloconverters gradually declined, and was quite dormant by the time that General Electric announced the development of the thyristor in 1957. The possibility of using this new compact and rugged controlled rectifier revived the cycloconverter concept. Soon a number of firms were involved in cycloconverter development work.

This chapter will trace the development of the cycloconverter since 1959 by reviewing selected articles published in English since that date. German contributions to cycloconverter development have been significant. But a number of German authors have published cycloconverter articles in English, so that German innovations can be followed without needing a reading knowledge of German.

3.2 The First Aircraft VSCF Systems Using the Cycloconverter

A number of papers on variable-speed, constant-frequency (VSCF) three-phase airborne power systems were originally presented at the AIEE Summer and Pacific General Meeting and Air Transportation Conference, Seattle, Washington in late June of 1959. Three of the papers dealing with electrical means (rather than mechanical means) of maintaining constant output frequency were later published in Volume 78 of the "AIEE Transactions".

The first paper,[1] submitted by B.V. Hoard of the Boeing Airplane Company, described the use of a transistorized, three-phase inverter to supply the correct value of make-up (slip frequency) power to the wound rotor of an induction generator. The engine driven, variable speed shaft of the induction machine always rotated at less than the synchronous speed corresponding to its stator output frequency. This meant that the inverter always supplied make-up power to the rotor. The inverter was not required to regenerate power because synchronous speed was not exceeded at any time. The author's VSCF system was successful, but the use of transistors in the inverter section limited its power level to about 1 kVA.

The second paper[2] was submitted by K.M. Chirgwin and L.J. Stratton of Jack and Heintz, Inc. in Cleveland, Ohio. They described their VSCF system development which used a wound rotor induction generator (operated both above and below synchronous speed), a slip channel comprised of a three-phase to three-phase cycloconverter (capable of handling power flow in both directions), and a

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[1] B.V. Hoard, "Constant Frequency Variable-Speed Frequency-Make-Up Generators," AIEE Transactions, Pt. II (Applications and Industry), Vol. 78, November 1959, pp. 297-304.

[2] K.M. Chirgwin and L.J. Stratton, "Variable-speed, Constant Frequency Generator System for Aircraft," AIEE Transactions, Pt. II (Applications and Industry) Vol. 78, November 1959, pp. 304-310.

synchronous machine. The synchronous machine and the induction generator were driven by the same variable speed shaft. The output frequency of the synchronous machine was a number of times higher than that of the induction machine so that the cycloconverter always had a sufficient frequency change ratio from the synchronous machine side to the rotor slip frequency side. The rating of the VSCF system was not specified, but it was probably about 60 kVA. This meant that the cycloconverter handled up to 20 kVA plus system losses assuming the shaft speed varied over a 2:1 range.

After submitting their first paper to the AIEE on March 23, 1959, Chirgwin and Stratton, in conjunction with J.R. Toth, submitted a second paper[3] on March 27, 1959, describing an alternative VSCF system. A high speed alternator driven by a variable speed shaft supplied three-phase power at variable frequency to a cycloconverter. The cycloconverter frequency reference was a high stability, three-phase, 400 Hertz oscillator. The frequency stability of the three-phase cycloconverter output was equal to that of the reference oscillator.

Chirgwin and Stratton started experimentation with their first VSCF system even before thyristor ratings were sufficiently well developed for use in their cycloconverter. They were able to generate several kVA of 400 Hz power from a

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[3] K.M. Chirgwin, L.J. Stratton, and J.R. Toth, "Precise Frequency Power Generation from an Unregulated Shaft," AIEE Transactions, Pt. II (Applications and Industry), Vol. 79, 1960 (January, 1961 section), pp. 442-449.

variable speed shaft using simulated thyristors in the cycloconverter section of their VSCF system. Each thyristor was simulated by using three transistors and approximately fifteen other circuit components! When thyristor ratings had advanced sufficiently, they built a second set of hardware, now using thyristors and incorporating other improvements suggested by their first experiments.[4]

Chirgwin and Stratton did not mention in their first paper whether or not their cycloconverter operated without circulating current. It was stated in Section 2.5 of this thesis, and illustrated in Figures 2.5 and 2.6 that the output voltage waveforms of a cycloconverter operating with and without circulating current are different. Unfortunately, the oscilloscope photographs[5] of the output voltage and current in the authors' first paper are indistinct so that no conclusions can be drawn on the basis of oscilloscope photographs. However, careful examination of other photographs in the two papers indicates that the same experimental "bread-board" was used for the cycloconverters in both VSCF systems. The second cycloconverter definitely was circulating-current-free as the following paragraphs will show.

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[4]Chirgwin and Stratton, op. cit., p. 308.

[5]Chirgwin and Stratton, op. cit., p. 308.

Chirgwin, Stratton, and Toth explained that their cycloconverter had three positive groups of thyristors (three P converters) and three negative groups of thyristors (three N converters). Quoting from their article:

> The function of the positive groups is to carry current during the positive half-cycle of the output frequency [current] wave, and the negative groups carry the current during the negative half-cycle of the output frequency [current] wave.
>
> . . . .
>
> Thus, all that is necessary in order to fabricate a precise frequency output wave is to control the delay in the firing of the rectifiers in an appropriate manner, to arrange to switch from the positive group to the negative group at the appropriate instances and to filter the output wave. Figure 4 [in their paper, but similar to Figure 2.6 in this thesis] illustrates that the instant appropriate for switching from the positive to the negative group is not necessarily the instant of zero voltage output but rather the instant of current zero in the output circuit. If the switching from positive to negative groups always occurs at the current zero, it is possible to transmit real or reactive power in either direction through the frequency changer.[6]

The statement quoted above, verified by Figures 4 and 5 in the body and Figure 12 in the appendix of their second paper confirms that they had been the first to build a successful three-phase to three-phase, circulating-current-free,

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[6] Chirgwin, Stratton, and Toth, op. cit., pp. 443-444.

thyristorized cycloconverter. Other companies, such as General Electric[7,8] were also working on cycloconverter systems. But Chirgwin, Stratton, and Toth of Jack and Heintz in Cleveland were the first to achieve success.

Judging from the submission dates of the two papers by Chirgwin, Stratton, and Toth, it is probable that the cycloconverter used in their first VSCF system paper also operated in the circulating-current-free mode.

Figure 12, parts A, B, and C in the discussion of the authors second paper[9] consisted of six oscilloscope photographs of voltage and current waveforms for both input to and output from a single cycloconverter building block. Operation with unity, lagging, and leading PF loads was illustrated. Observing these waveforms leads to two conclusions:

1. The circulating current elimination logic and detection circuitry was suitable for leading, unity, and lagging PF loads. Hence, the operation of the logic depended only upon the detection of current zero in the output circuit.

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[7] S.C. Caldwell, L.R. Peaslee, and D.L. Plette, "The Frequency Converter Approach to a Variable Speed, Constant Frequency System," AIEE Conference Paper No. 60-1076 presented at the AIEE Pacific General Meeting, San Diego, California August 1960.

[8] D.L. Plette and H.G. Carlson, "Performance of a Variable Speed Constant Frequency Electrical System," IEEE Transactions on Aerospace, Vol. 2, No. 2, April, 1964, pp. 957-970.

[9] Chirgwin, Stratton, and Toth, op. cit., p. 450.

2. No matter whether the load PF is leading or lagging, the input PF is lagging and decreases as the load PF decreases. Even unity PF loads have an average lagging input PF because of the phase-controlled operation of the cycloconverter as it produces a sinewave output voltage.

The second point was well known in the Thirties,[10,11] and the authors referred to the article by Von Issendorf in which he calculated the input PF versus the load PF assuming an infinite number of supply phases and zero commutation reactance. Chirgwin, Stratton, and Toth presented calculations in the appendix to their article showing that the best possible input PF was λ = .843 . This occurred for a purely resistive load fed by a cycloconverter putting out a sinewave voltage of 1.0 p.u. amplitude.

The six oscilloscope photographs were placed in the discussion section of the paper as an answer to a request by R.D. Jesse of Westinghous Electric. Mr. Jesse felt that some test results "to substantibte the statement that leading loads have the same effect on the generator as do lagging loads would be of interest."[12]

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[10] J. von Issendorf, "Der Gesteuerte Umrichter [The Controlled Frequency Changer]," Wissenshaftliche Veroffentlichungen, Siemens-Werken, Vol. 14, Pt. III 1935, pp. 1 - 31.

[11] H. Rissik, The Fundamental Theory of Arc Converters (London: Chapman and Hall, Ltd., 1939) p. 267 .

[12] Chirgwin, Stratton, and Toth, op. cit., p. 449.

R.D. Jesse and W.J. Spaven of Westinghouse Electric submitted a paper in March, 1959 for presentation at the AIEE Summer and Pacific General Meeting and Air Transportation Conference in June, 1959.[13] The authors proposed a hetrodyne or mixer technique in which the fundamental frequency of the converter output voltage was to be the difference between the generator frequency and the switching frequency of the converter. Other non-desirable frequencies generated by the hetrodyning process were to be removed by filtering. The paper was actually a mathematical analysis of the voltage wavefoms that could be produced by using forced-commutation in a cycloconverter rather than the normal line-commutation. Forced - commutation permits successful operation with positive values of phase back angle α (as with line-commutation), and with negative values of α (this is not possible with line-commutation alone).

The authors did not propose any forced-commutation technique to actually make their scheme feasible for use with thyristors. This omission was pointed out in the discussion section of the authors' paper by their reviewers, Chirgwin and Stratton, who commented that their line-commutated cycloconverter was a practical success. Indeed there have been many more line-commutated cycloconverter (i.e.

[13] R.D. Jesse and W.J. Spaven, "Constant-Frequency A-C Power Using Variable Speed Generation," AIEE Transactions, Pt. II (Applications and Industry) Vol. 78, 1959 (January, 1960 section), pp. 411-418.

"normal" cycloconverter) articles than articles on forced-commutated cycloconverters.[14]

G.J. Hoolboom of McMaster University, actually built a frequency changer[15] based on the mixer technique proposed by Jesse and Spaven. The cycloconverter was only partially successful because forced-commutation was not used. Hoolboom concluded that a successful cycloconverter operating in the mixer mode would need forced-commutation.

One interesting aspect of Hoolboom's approach was his method of current zero detection. The output lines had power diodes connected in anti-parallel so that the diodes carried the load current. Absence of voltage across the diodes indicated zero current flow. The nonlinear volt-ampere characteristics of the diodes made the detection of very small currents simple without causing high power dissipation when large currents were flowing.

3.3 A Synchronous Motor Drive

In May, 1961 D.C. Griffith and R.M. Ulmer of Thompson Ramo Wooldridge in Cleveland, Ohio published a short paper on an 18 thyristor, three-phase

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[14] S. Miyairi and I. Takahashi, "Application of Power Modulation Technique Employing Thyristors." Electrical Engineering in Japan (IEEE Translation), Vol. 88, No. 11, 1968, pp. 36-45.

[15] G.J. Hoolboom, "An All Solid State Cycloconverter." IEEE Conference Paper 63-1040, October 1963, pp. 1-8 and Figs. 1 - 10.

to three-phase cycloconverter.[16] The unit had a 30 kVA rating and a frequency range of 0 - 15 Hz for a 60 Hz input.

The cycloconverter operated with circulating current, unlike those made by Chirgwin, Stratton, and Toth at Jack and Heintz in Cleveland. Instead of generating constant output frequency from a variable input frequency as in a VSCF system, Griffith and Ulmer's cycloconverter generated a variable output frequency from a fixed 60 Hz input. The authors used an electromechanical scheme involving a driven synchro resolver and three demodulators to generate a low frequency set of three-phase reference voltages. The frequency and phase rotation of these voltages governed the frequency and phase rotation of the three-phase cycloconverter power output. The controlled motor was of the synchronous -induction type, and operated open loop. No design information was presented, but the paper contained several excellent waveform photographs taken at 0.5 Hz output.

3.4 The First Lear Siegler Article

By 1961, a third company in Cleveland, Ohio was working on the cycloconverter problem. R.A. Van Eck of Lear Siegler, Inc. presented a theoretical paper on cycloconverters to the June, 1961 AIEE Aero-Space Transportation Conference.[17]

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[16] D.G. Griffith and R.M. Ulmer, "A Semiconductor Variable Speed A-C Motor Drive," Electrical Engineering, May 1961, pp. 350-353.

[17] R.A. Van Eck, "Frequency-Changer Systems Using the Cycloconverter Principle," AIEE Transactions, Pt. II (Applications and Industry), Vol. 82, May 1963, pp. 163-168.

The paper reviewed the relationship of cycloconverter input power factor to the harmonic distortion factor and the average phase displacement of the current input to the cycloconverter. These relationships had been developed in the Thirties[18,19] and were mentioned by Chirgwin, Stratton, and Toth.[20] Van Eck also reviewed voltage drop due to commutation overlap.

Several paragraphs and one figure in the article pointed out the circulating current problem.[21] Then, making the assumption that circuit resistance could be neglected, Van Eck developed two equations predicting the maximum amplitude of circulating current to be expected between the anti-parallel converters in a building block. One equation applied to three-pulse, one-way converters, which have maximum circulating current when $\alpha_P = 60^\circ$ and $\alpha_N = (180^\circ - 60^\circ)$. The other equation applied to six-pulse converters (also to 12, 18, 24, ... pulse) which have maximum circulating current when $\alpha_P = 90^\circ$ and $\alpha_N = (180^\circ - 90^\circ)$.

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[18] Von Issendorf, op. cit., pp. 1 - 31.

[19] Rissik, op. cit., Chap. XII.

[20] Chirgwin, Stratton, and Toth, op. cit., pp 446-448.

[21] Van Eck, op. cit., p. 166 and Fig. 5.

3.5 A German Cycloconverter

In the November, 1963 issue of the "Siemens Review", R. Heck and M. Meyer described the closed-loop speed control of a 30 kW induction motor using a circulating-current-free cycloconverter.[22]

Three separate cycloconverter building blocks were used. Each building block had two, three-phase, two-way converters connected in anti-parallel. The induction motor had three separate pairs of stator leads, so that each phase was isolated. This meant that the cycloconverter building blocks did not need three-phase transformers to prevent block to block short circuits of their two-way converters.

As will be shown later herein, the torque versus slip frequency characteristic of a singly-fed induction motor will be independent of its stator frequency provided that its airgap flux level is maintained at a constant value despite any changes in stator frequency and current. Similarly, for constant airgap flux, there is a fixed functional relationship between the slip frequency and the amplitude of the stator current. Heck and Meyer used these relationships to build a cycloconverter control system with several inner loops.

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[22] R. Heck and H. Meyer, "A Static-frequency-changer-fed Squirrel-cage Motor Drive for Variable Speed and Reversing," Siemens Review, November, 1963, No. 11, pp. 401-405.

Each building block had a high speed current loop built around it. The three-phase set of current references were supplied by a frequency and amplitude controller. Hall generators were used in the air gap of the machine to measure the air gap flux. The actual flux magnitude was compared with the desired constant flux reference in the field controller. The output of the field controller adjusted the amplitude of the three-phase set of current references, leaving the frequency and amplitude controller. That is, the air gap flux was maintained at a constant value by a feedback loop manipulating stator current amplitude. The frequency and phase sequence of the three-phase current reference set was controlled by the amplitude and sign of the output of the speed controller. The authots did not comment on the control modes of the speed controller. However, it was possibly of the proportional plus integral type so that zero steady-state speed error could be achieved despite various values of steady state load torques.

At the conclusion of their paper, Heck and Meyer commented that, "The limit frequency of a six-pulse convertor operating on a 50 - c/s system is approximately 20 c/s ."[23] This corresponds to a frequency stepdown ratio of 2.5 to 1. Several years later, W. Slabiak and L.J. Lawson writing about the Lear Siegler cycloconverter commented, "Typically a stepdown frequency ratio of 2

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[23] Heck and Meyer, op. cit., p. 405.

to 1 is used from input-to-output of the frequency changer. With a small sacrifice in system efficiency of about 5 per cent, a ratio of 1.5 to 1 may be used."[24] Unlike the Siemens cycloconverter, the Lear Siegler cycloconverter did not need to use direct closed loop control of the induction motor stator current. Hence, the cycloconverter output could be higher for a given particular input frequency.

3.6 General Electric's Cycloconverter VSCF System

It was mentioned earlier in this thesis that companies other than Jack and Heintz were also working on VSCF systems.[25] In 1964, D.L. Plette and H. G. Carlson published an excellent summary of the VSCF system development that had been carried out over the previous five years in the specialty Control Department of the General Electric Company.[26] They started work in 1959, but had found it difficult to develop large, three-phase output VSCF systems. Quoting

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[24] W. Slabiak and L.J. Lawson, "Precise Control of a Three-Phase Squirrel-Cage Induction Motor Using a Practical Cycloconverter," IEEE Transactions on Industry and General Applications, Vol. IGA-2, No. 4, July/August 1966, p. 276.

[25] See page 31 herein.

[26] D.L. Plette and H.G. Carlson, "Performance of a Variable Speed Constant Frequency Electrical System," IEEE Transactions on Aerospace, Vol. 2, No. 2, April 1964, pp. 957-966.

from their 1964 paper[27]

> For example, the 20 kVA VSCF generating system shown in Figure 1 was delivered to the Bureau of Weapons by General Electric in early 1962 after nearly three years of intensive development and design effort. Although this system was flight tested, the electrical performance of the equipment was somewhat below normal power quality in the areas of voltage modulation, voltage transients, and voltage imbalance.

However by 1964, the authors had developed a satisfactory system and presented a considerable amount of test data on it in their paper. The cycloconverter output was rated at 30 kVA, 115/220 volts, three-phase, 400 Hz for a three-phase input varying from 1333 Hz to 2666 Hz. The cycloconverter operated without circulating current, and small LC output filters were used to reduce high frequency ripple. Negative feedback was used around each cycloconverter building block to improve the wave shape and to lower the converter impedance.

The necessary three-phase, 400 Hz reference voltages were obtained from a ring counter triggered by a high stability 2400 Hz oscillator. Individual phase voltage regulators (that is, one for each building block) adjusted the level of clipping applied to the square wave voltages taken from the ring counter. The three-phase, controlled amplitude square waves were then filtered to give high quality sine wave references. Three separate voltage regulators were provided so that balanced three-phase voltages could be generated despite the single phase loads in

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[27] Ibid., p. 957

the aircraft. The oscillator, ring-counter, clipper, lowpass filter approach of generating the three-phase references is very suitable for VSCF systems because they operate at a fixed output frequency. Later in this chapter a method will be described to generate variable frequency, three-phase references for use in closed loop, controlled slip operation of induction motors driven by three-phase cycloconverters.

Plette and Carlson were concerned with meeting existing military standards for VSCF systems. Their conclusion from their testing was that the cycloconverter system compared favorably with the conventional system. Voltage control with individual phase voltage regulators was satisfactory. The frequency stability depended completey upon the precision of the 2400 Hz oscillator. Amplitude and frequency modulation of the output voltage exceeded military standards. But the authors felt (quite justifiably) that the particular test procedures and equipment specified by MIL-STD-704 were not really applicable to a cycloconverter VSCF system. The dc content in the cycloconverter output was less than 0.1 volts.

The authors found that the outputs of two cycloconverter systems could be successfully paralleled, and presented an oscilloscope photograph of the synchronizing operation.[28]

Appendix B of the paper discussed the effect of varying load PF on the cycloconverter input PF. The input PF affects the alternator rating. The

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[28] Ibid., Figure 11, p. 970.

results derived by the authors agreed with those originally presented by Von Issendorf[29] and by Rissik.[30]

3.7 A Small Reversing Drive

In the May/June, 1965 issue of IGA Transactions, R.A. Johnson and F.T. Thompson described an eight thyristor, single-phase to single-phase cycloconverter, with circulating current.[31] The cycloconverter was actually used as a reversing supply for a $\frac{1}{6}$ th horsepower motor positioning a steam valve shaft. The authors provided a very complete description of their system, including block diagrams, circuit diagrams, frequency response diagrams, and oscilloscope photographs.

The article is very interesting, and the position control system was quite successful. However, the firing circuit details are not directly applicable to polyphase, circulating-current-free cycloconverters.

3.8 A Large, Circulating-Current-Free, Reversing Drive

In the same May/June, 1965 issue of the IGA Transactions, D.L. Duff and A. Ludbrook presented an important paper on the design of a high performance,

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[29] Von Issendorf, op. cit., pp. 1-31.

[30] Rissik, op. cit., pp. 268-270.

[31] R.A. Johnson and F.T. Thompson, "Throttle Valve Position Control System," IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3 May/June, 1965, pp. 199-205.

circulating-current-free, reversing armature supply.[32] The reversing supply was, in fact a three-phase to single-phase cycloconverter using anti-parallel two-way converters.

The authors first compared, in tabular form, circulating current operation with circulating-current-free operation based on the considerations of cost, efficiency, regulator response, and fault susceptibility.

The circulating-current mode of operation does have the advantage of avoiding discontinuous armature current flow. And as K.G. Black pointed out,[33] if the motor armature current becomes discontinuous (for instance, due to a low torque load or the motor shaft), then the incremental gain of the converter drops. This loss of gain impairs the transient response of the control system to sudden load changes. However, the system response is still excellent. Duff and Ludbrook chose the circulating-current-free mode on the basis of lower cost, higher efficiency, and lower fault susceptibility.

They then proposed two methods of eliminating circulating current, describing them as: the biased transfer function, and the coincident transfer function with crossover logic. The biased transfer function would supposedly eliminate the

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[32] D.L. Duff and A. Ludbrook, "Reversing Thyristor Armature Dual Converter with Logic Crossover Control," IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June, 1965, pp. 216-222.

[33] K.G. Black, "Effect of Rectifier Discontinuous Current on Motor Performance," IEEE Transactions on Applications and Industry, Vol. 83, November, 1964, pp. 377-382.

circulating current by placing a deadband between the input-output relationships of the two converters. The authors chose the second alternative, making the input-output transfer functions of the anti-parallel converters coincident by using the bias-shift technique combined with both positive and negative crossing detectors.[34] Current zero detection and input reference polarity were used to control the crossover logic (circulating-current-elimination logic).

The cycloconverter was put inside a high speed armature current loop. The armature current was measured by using separate sets of ac current transformers and rectifiers for each converter. Figure 4 in the paper showed that the regulator response was fast even when the armature current was discontinuous.

Duff and Ludbrook then outlined how they used the bias-shift technique for phase control. By using both positive and negative crossing detectors, the phase back angles of the firing pulses supplied to the anti-parallel converters were kept supplementary. This meant that the average output voltages of the anti-parallel converters would have been in balance (coincident) if the cycloconverter was operating in the circulating current mode. Of course, because the cycloconverter was designed to be circulating-current-free, firing pulses were supplied to only one converter at a time. The thyristors of the other converter were left in their blocking state by not supplying them with firing pulses.

[34]See pages 17 to 20 herein.

Each cosine wave had two "marker" pulses electronically superimposed on it every cycle. One marker pulse guaranteed that a crossing would be detected (and a firing pulse formed) at $\alpha = 0^{\circ}$ even when the control voltage (bias voltage) exceeded the peak value of the cosine wave. The other marker pulse was used as a phase back limit to prevent the phase back angle α from exceeding the retardation limit when the converter was inverting. These marker pulses will be called phase forward limit (PFL) pulses and phase back limit (PBL) pulses in Chapter IV of this thesis.

Then, under the heading "Crossover Philosophy," subheading "Regulator Action" the authors pointed out an important fact about back EMF loads and discontinuous current operation. Quoting from the paper:

> The coincident transfer function would be ideal if, during discontinuous current conditions, the rectifier output voltage was ... governed by the expression set down in (1). [$V_d = V_{do} \cos \alpha$] The transfer function breaks away from the continuous current characteristic at a point determined by the time constant of the load circuit and approaches zero volts at the 120 degree phase delay instead of the 90 degree phase delay for the continuous current condition (provided the back EMF is zero). As the EMF of the machine varies, the characteristic converges on the value of the EMF instead of zero. Figure 2 shows the transfer curve for zero EMF, and Figure 8 reproduced as Figure 3.1 of this thesis shows the curve for a particular value of back EMF.[35]

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[35] Duff and Ludbrook, <u>op</u>. <u>cit</u>., pp. 219-220

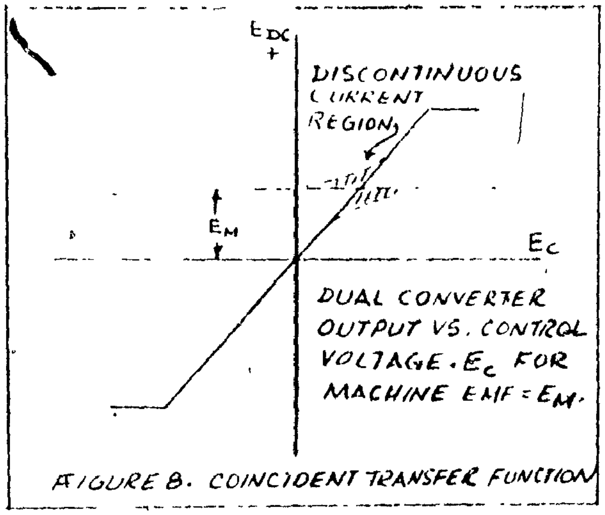

FIGURE 3.1. COINCIDENT TRANSFER FUNCTION (BY DUFF AND LUDBROOK)

Again quoting from the paper:

It can be seen from Figure 8 that if the value of the input signal to the gating circuit were to remain the same when pulses were transferred to the incoming bridge, the bridge would operate in the continuous current portion of the characteristic at a voltage differing considerably from the EMF of the machine. To prevent the catastrophic overshoot of current which would result, the incoming bridge must be phased back before gating pulses are released to it. Ideally, the incoming bridge should be released to operate just short of the zero current point. This point is a function of the EMF of the machine which must be sensed in order to position the pulses correctly. A less sophisticated but more economical approach is to inject a signal into the operational amplifier to drive its output in such a direction as to phase back the incoming bridge <u>beyond</u> the zero current point. Subsequently, the incoming bridge is released to the action of the regulator. A very smooth crossover can thus be obtained without the need to sense machine EMF.[36]

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[36] Duff and Ludbrook, op. cit., p. 220.

Figure 9 in the paper consisted of four oscilloscope photographs showing a change in armature current reference to the armature current controller, the output of that controller, and the crossover of the armature current. The change in armature current reference was varied so that all four possibilities of continuous and discontinuous current operation before and after crossover were demonstrated. The dead time during which neither converter was in conduction appeared to vary from 10 ms to 30 ms. This dead time was caused by the need to temporarily phase back the incoming converter away from the coincident transfer function at crossover time to prevent an armature current surge.

Duff and Ludbrook's current zero scheme depended upon two signals, one of which was derived from ac current transformers on the cycloconverter input lines. However it was difficult to detect exactly when the current started and stopped using this method by itself. So a second M-shaped waveform with sharp edges formed by rectifying and clipping the ac component of the cycloconverter output voltage was combined with the current signal to give a more reliable indication of current zero.

The circulating-current elimination logic (crossover logic) controlled the firing pulses so that only one of the anti-parallel converters operated at a time. The logic permitted a change of converters when the following three conditions were met: 1) the polarity of the analog reference to the armature current controller had changed, 2) zero current in the outgoing converter, and 3) no gate pulses were being applied to the outgoing converter. Note that the analog voltage polarity monitored by the logic was taken from current controller input reference rather than from the output of the controller. As will be shown in Section 5.8 of Chapter V the polarity of the gating control signal (which was the output of the current controller in this case) could have also been used by the logic if Duff and Ludbrook had chosen to bias the two transfer functions apart rather than using their coincident transfer function approach.

The final sections of their paper covered overcurrent protection, control cicuit packaging, and applications of the drive. Fault protection was handled by ac breakers, dc breakers and individual thyristor fuses. Packaging of the control logic and firing circuitry was compact using card racks to hold the cards. The cycloconverter system had been used in high performance dc motor field supplies from 10 to 100 kW and in armature supplies to 100 hp (900 ampere, 460 volt maximum).

In summary, the paper by Duff and Ludbrook is very worthwhile because of their discussion of four topics: 1) the advantages and disadvantages of circulating current free operation, 2) the bias-shift method of phase control with supplementary firing angles plus phase forward and phase back limit pulses, 3) crossover logic requirements, and 4) the need to phase back the incoming converter when using a back EMF load.

3.9 Two dc Reversing Drives for Rolling Mills

The IEEE Industrial Static Power Conversion Conference was held in Philadelphia, Pennsylvania from November 1st to 3rd, 1965. At that conference L. F. Stringer presented an eighteen page paper describing the thyristorized drives built by Westinghouse Electric Corporation for a complete aluminum hot mill.[37]

The reversing mill section used two 5000 hp dc motors. Each of the 5000 hp motors was fed by an effective 12 pulse supply consisting of two sets of circulating-current-free, anti-parallel, three-phase, two-way converters operating with 30 degrees of phase displacement. The circulating current was suppressed by using the biased transfer function technique. That is, when the common control voltage to the anti-parallel converters was zero, the phase back angle of each converter was about 142°. This retardation beyond the normal 90° phase back was provided by independent bias voltages in each converter.

The added retardation suppressed the circulating current, but put a

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[37] L. F. Stringer, "Thyristor D-C Drive Systems for a Non-Ferrous Hot Line," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, pp. 40-58.

deadband between the transfer functions of the converters. To narrow the deadband and minimize gain changes due to discontinuous load current flow, high speed voltage feedback loops were put around the converters. Outer armature current loops provided the reference signals for the high speed, inner voltage loops. Finally, a voltage command controller driven by a ramp function generator provided the reference to the current controllers. Even the block diagram describing the control system is quite formidable and it is easy to see why Duff and Ludbrook rejected the biased transfer function approach for their circulating-current-free drive.

Actually, the article is worthwhile reading because of the vast amount of detail in the text and illustrations pointing out the problems that must be considered when building a successful, dc reversing drive system.

At the same conference, C.E. Rettig and P. J. Roumanis of General Electric presented a paper on their company's experience with thyristorized drives for rolling mill applications.[38] Their largest reversing drive had used two 6000 hp motors in parallel. The armature supply used four sets of 6 pulse, anti-parallel bridges fed from delta and wye transformer secondaries (30° displacement) which

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[38] C. E. Rettig and P. J. Roumanis, "Thyristor Drives for Metal Rolling Applications," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., pp. 59-68.

were then paralled through interphase reactors to provide an effective 12 pulse supply. The circulating current was suppressed by using a biased transfer function such that each bridge was phased back 150° when the gating control signal was zero. Again, a high speed inner voltage loop around the converters was used for linearization before the current and speed regulating loops were applied to the drive.

3.10 German Developments in dc Reversing Drives

Both the method of coincident transfer function with crossover logic and the method of biased transfer function have been used successfully in circulating-current-free reversing drives. In the latter method each of the two anti-parallel converters has its own gating control circuit which is biased back far enough so that no more than one converter conducts at a time provided the control voltage to the gating circuits is steady or varying slowly. On the other hand, if the control voltage swings too rapidly from positive to negative (or negative to positive) during crossover, then the oncoming converter may start conduction before the offgoing converter ceases, thereby creating a circulating current fault through the two converters. The requirement that the maximum rate of change of gating control voltage be limited then restricts the speed to which the usual proportional plus integral action linearizing loop around the converters may be tuned. The usual first step to solve this problem is to provide logic circuits which block all firing pulses in the reverse converter if the forward converter is in conduction and vice versa. If neither converter is in conduction, then neither converter is blocked. The first converter to start conduction should immediately block the other but occasionally this race ends in a tie resulting in a circulating current fault. A common approach is to detect any such fault with a logical AND of the converter current logic signals thereby triggering a flip-flop that blocks gate pulses to both converters until the flip-flop is manually reset. Even an occasional fault such as this is a nuisance and it would be better to prevent the race in the first place by permitting only one converter at a time to attempt to establish conduction. The two logic signals which may be so used for the case of converters with biased transfer functions are either the polarity of the gate control voltage, or the polarity of the reference signal fed to the linearizing proportional plus integral controller built around the converters. The latter approach is the most commonly used industrially, but a comparison between the two will be made in Chapter V.

The earliest paper found during the preparation of this thesis[38.1] which

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[38.1] This paper was actually discovered by Geza Joos of McGill University and given to the writer after the typing of this chapter was complete. Hence the footnote numbering scheme has been modified at this point to permit insertion of references to the paper.

described the use of controller reference polarity along with the converter current signals to interlock operation of a reversing dc drive was written in 1961 by S. Zurcher of Brown Boveri.[38.2] The three logical variables involved (one polarity signal and two current signals) may be permuted into eight distinct states. For each state there exists a corresponding correct state for the converter blocking signals to be in. By tabulating these states in a truth table, Zurcher synthesized a Boolean logic equation for blocking a converter which satisfied all the states. He then simplified the equation with Boolean identities and implemented the result with NOR logic. There are some minor inconsistencies in the paper but these are attributable to semantic difficulties often experienced when attempting to explain positive and negative logic and their implementation with NOR or NAND blocks. Figure 3 2 herein is an adaption of Table III, Figure 4, and Figure 8 of the paper with more consistent labelling of the Boolean variables. Because the current zero detection circuits were non-perfect, it was necessary to use the delay circuits to retard the unblocking (1 - 0 change) of the oncoming converter by a delay usually adjusted to between 6 and 10 ms. Schemes were presented in the paper using the logic for the circulating-current-free operation of anti-parallel converters in

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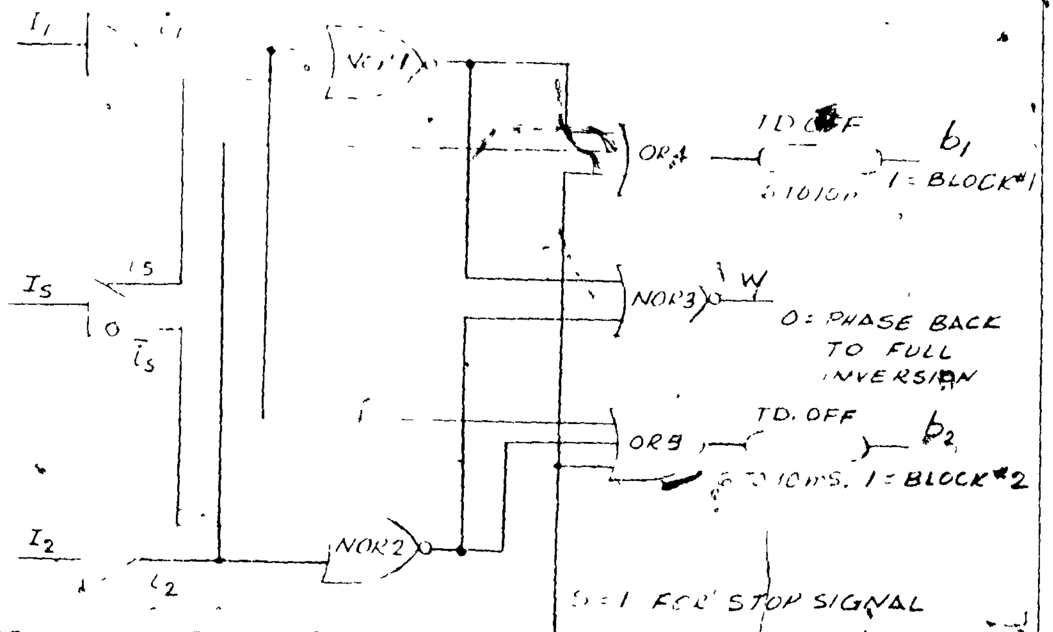
[38.2] S. Zurcher, "Two-converter Connections with Suppressed Figure-eight Current," The Brown Boveri Review, Nov./Dec. 1961, Vol. 48, No 11/12, pp. 650-662.

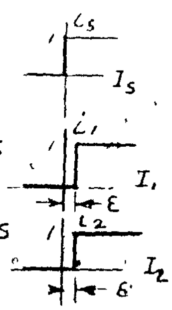


INPUT A/D BUFFERS

$i_s = 1$ FOR $I_s > 0$ THUS

$i_1 = 1$ FOR $I_1 > \varepsilon$ THUS

$i_2 = 1$ FOR $I_2 > \varepsilon$ THUS



BOOLEAN EQUATIONS:

$$\text{BLOCK\#1} = b_1 = (\bar{i}_s \cdot \bar{i}_1) + i_2 = 1$$

$$\text{BLOCK\#2} = b_2 = (i_s \cdot \bar{i}_2) + i_1 = 1$$

This Figure has been adapted from Table III, Figure 4 and Figure 8 of a paper by :

S. Zurcher, "Two-converter Connections with Suppressed Figure-eight Current," The Brown Boveri Review, Nov. / Dec. 1961, Vol. 48, No. 11 / 12, pp. 654, 655, and 662.

FIGURE 3.2. BROWN BOVERI CROSSOVER LOGIC (BY ZURCHER)

1) an armature controlled, reversing drive with an inner current loop and an outer speed loop, 2) a Brown Boveri Contiflux drive with reversing field supply, 3) a Ward-Leonard drive with reversing field supply, and 4) a two-quadrant armature supply combined with a discontinuous reversing field supply to yield an effective four quadrant operation. The fourth scheme required an additional NOR gate in the logic (NOR 3, Figure 3.2) to provide a full inversion signal to the offgoing converter. Full inversion combined with a field forcing ratio of four to six drove the field current to zero within 35 ms. After a delay period of about 10 ms the other converter was unblocked and the current rose to its rated reverse value in about 40 ms.

Zurcher stated that the gating circuits were controlled an equal and opposite amount so that if both were in operation at the same time they would produce the same mean voltage.[38.3] Stated in another way, the transfer functions of the converters were coincident. Duff and Ludbrook demonstrated that because of the possibility of discontinuous armature current (see Figure 3.1 herein) drives using coincident converter transfer functions had to temporarily phase back the oncoming converter before its gating pulses were unblocked. Failure to do so would result in a tremendous current overshoot in the oncoming converter unless the offgoing converter had been in continuous conduction. This phasing back

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[38.3] Ibid., p. 652.

action really implied that the transfer functions of the converters were temporarily noncoincident, or in other words, biased apart. The output voltage of the proportional plus integral action controller had to sweep across the temporary deadband between the converters until the oncoming converter current started and rose into regulation. The point is that when considering the regulator action, there is very little difference between crossing the temporary deadband between normally coincident transfer functions and crossing the permanent deadband between biased transfer functions. Zurcher very carefully stated that a distinction had to be made between armature supplies and field supplies, and that in all his examples the current was assumed to change continuously.[38.4] But because he had separate gating circuits which could easily have been biased apart to prevent armature current surges, the suspicion exists that Brown Boveri was declining to reveal at that time all its knowledge about armature supplies.

In 1965 L. Abraham, J. Forster, and G. Schiephake of Allgemein Elektricitats - Gesellschaft (AEG) in Berlin, Germany presented an IEEE conference paper[39] describing some AEG, Brown Boveri, and Siemens developments since 1963.

[38.4] Ibid., p. 65.

[39] L. Abraham, J. Forster, and G. Shiephake, "German Developments in Thyristor Application," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, pp. 197-203.

The authors chose as one of their examples a circulating-current-free reversing drive by Siemens which had also been described by F. Wesselak in the "Siemens Review" in 1965.[40]

The drive was an armature supply with anti-parallel converters and an outer speed loop which provided push-pull references for two parallel, high-speed, current regulators. Each current regulator controlled its own converter via its own firing circuit set. Push-pull references were required because the current feedback was developed by rectifying the signals from ac current transformers which were on the ac line side of the drive at a point where they carried the current of both converters.

To prevent an overshoot of armature current when the oncoming converter was unblanked, the firing circuit set for the blanked converter was given an input voltage that corresponded to the instantaneous armature voltage (as indicated by the tachogenerator). Possibly this was done by switching the current regulator of the blanked converter so that it was forced to follow the tachometer voltage in a manner similar to that described by Pelly.[41] When the

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[40] F. Wesselak, "Thyristor Converters with Natural Commutation," Siemens Review, December 1965, No. 12, pp. 405-410.

[41] B. R. Pelly, Thyristor Phase-Controlled Converters and Cycloconverters - Operation, Control, and Performance (New York: Wiley - Interscience, 1970) pp. 121-126

sign of the speed regulator output changed, the crossover logic switched the firing circuits of the conducting converter to the inverter limit so that the armature current was quickly reduced to zero. After the current had ceased, there was a 1 ms delay during which firing pulses to both converters were blocked, before the firing pulses of the oncoming converter were released. Because the firing angle of the oncoming converter had been matched to the armature voltage by the voltage check arrangement while it was still blocked, the armature current came into regulation without a surge or long dead period.

The crossover logic depended upon two signals: the polarity of the speed regulator output, and the detection of current zero in both converters. Unlike the Brown Boveri scheme described by S. Zurcher, the logic was not supplied with current zero detection signals from each converter. Hence the crossover logic probably used the current zero detection signal as the commands to either set or reset a flip-flop, while the polarity signal specified which command was permissible. The 1 ms double blocking period could have been produced by adding a delay circuit to each flip-flop output. Each inversion signal which drove the offgoing converter to the inversion limit could have been formed by a logical AND of the polarity signal (or else its inverse) and one (or else the other) of the flip-flop outputs.

Siemens produced a simplified version of their drive using a single current regulator and one set of firing circuits to control two anti-parallel bridges.[42]

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[42] H. Geissing and G. Moltgen, "Thyristor Convertors for D. C. Reversing Drives," Siemens Review, October 1965, No. 10, pp. 330-333.

The gating pulses from the firing circuits were routed to either the forward bridge or the reverse bridge by logic gates under control of the crossover logic. Again the criteria for the crossover logic were the change of polarity of the input of the speed regulator and detection of current zero in both bridges. When the polarity changed, the logic clamped the output of the speed loop to zero and injected a negative reference into the current regulator. The negative reference forced the regulator output in such a direction that the firing circuits phased back to the inversion limit and quickly reduced the armature current to zero. Once the current zero was detected the crossover logic blocked the gate pulses to both converters for 5 to 10 ms. At the end of this delay period the pulses to the oncoming converter were unblocked, the speed loop was unclamped, and the negative current reference was removed. The armature current then rose into regulation without a surge. However there was a short deadtime because the converter had been phased back well beyond the zero current point. Siemens also had similar logic for armature supplies that had a single converter combined with electromechanical reversing contactors. In addition they had experimented with both approaches for reversing field supplies. One point that Siemens neglected to mention in their articles is that the gain inversion (that is, a factor of minus one) caused by operating the reversing switch had to be compensated by synchronously inserting another gain inversion at some point in the speed loop.

This fact is more clearly explained in Section 3.11 below.

3.11 ASEA dc Reversing Drives

A more recent example of European practice was the new series of drives announced in 1968 and described in 1969 in the "ASEA Journal" by J. Lidberg.[43] The family of thyristor converters was structured on a functional module basis to maximize flexibility while minimizing assembly time and cost.

One type in the series, the YMHC, was the classic anti-parallel combination of three-phase, two-way converters operating without circulating current. Change of reference voltage polarity to the inner current loop and detection of current zero were the criteria for the blocking module (circulating current elimination logic) to interchange the blanking of the anti-parallel converters. The current zero signal was derived from ac current transformers on the input side of the drive. Voltage matching of the incoming converter voltage to the armature voltage was carried out over a 10 ms interval during which the load current was zero and both converters were blanked. This is in contrast with the scheme used in the Siemens dc reversing drive where the voltage matching was supplied to the firing circuits in the blanked converter for its full blanking period. Consequently, Siemens was able to make the current zero period (that is, the double blanking period) much shorter (1 ms in length). ASEA could have used the same scheme as Siemens, but they wished to maintain the interchangeability between the blocking

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[43] K. Lidberg, "New Series of Thyristor Converters for Industrial Motor Drives, 20 - 500 kW," ASEA Journal, Vol. 42, No. 5, 1969, pp. 63-68.

modules for types YHMC and YHMB.

Type YHMB used a single, three-phase, two-way converter combined with a four thyristor armature reversing switch. The control logic was very similar to the dual converter case, and the changeover criteria were identical. The difference was that the problem of eliminating the circulating current had changed to the problem of operating the reversing switch at the right moment so as to avoid short circuiting the single converter.

Because the single converter and its firing circuits were always in use during armature current flow, the only possible time to carry out the voltage matching in the YHMB type of drive was during the 10 ms period equivalent to the 10 ms double blanking period of the YHMC dual converter system. And, as mentioned above, the voltage matching for the YHMC dual converter was carried out during the 10 ms double blanking period so that the blocking modules would be interchangeable between the two types. Actually, the YHMB blocking module also contained control logic and an oscillator for providing gating pulses to one pair (at a time) of the four thyristors in the reversing switch.

Reversing the armature connection at crossover time did not affect the stability of the inner current loop because its current feedback was the rectified version (after isolation by ac current transformers) of the three-phase currents to the three-phase, two-way converter. But, reversing the armature connection did invert the sign of the gain of the outer speed loop at that point in the transfer function block diagram. However this inversion was cancelled by connecting at the output of the speed regulator a unity gain, inverting amplifier that could be inserted or bypassed synchronously with the armature connection reversal. Chapter VI in this thesis will illustrate the alternate approach of inserting the unity gain, inverting amplifier inside the current loop (the armature feedback current is not rectified), using a thyristor reversing switch to switch the armature connection, and leaving the outer speed loop alone.

Lidberg concluded in his "ASEA Journal" article that because both the YHMB single converter with thyristor armature reversal and the YHMC dual converter had exactly the same control characteristics, the choice between them should be based upon cost. ASEA's experience was that thyristor armature reversal had the lower cost at current levels for which the armature reversing thyristors did not have to be paralleled.[44] This meant the YHMB armature reversal type was generally used at power levels from 20 to 140 kW and the YHMC dual converter type from 125 to 500 kW.

3.12 Cycloconverter Speed Control of Run-out Table ac Motors

The usual arrangement in a hot strip mill is that run-out tables, with each table roll driven by a single motor, are placed on either side of the reversing

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[44] *Ibid.*, pp. 67-68

roughing mill. The run-out tables support and transport the slab as it is elongated by the reversing roughing mill. They are then used to support and transport the rough strip as it enters the continuous finishing mill. The run-out tables are also used to spot the slab for the initial head and tail end trimming by the cropping shear. It is important that the speed of the run-out tables be synchronized, first with the reversing roughing mill, and then afterwards with the continuous finishing mill. At the conference in Philadelphia in November, 1965, R.A. Hamilton and G. R. Lezan described a General Electric installation with four circulating-current-free cycloconverter variable frequency supplies controlling a total of three-hundred 2.6 hp induction motors rotating individual run-out table rolls located around a reversing mill.[45, 46]

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[45] R.A. Hamilton and G. R. Lezan, "Thyristor Adjustable Frequency Power Supplies for Hot Strip Mill Run-out Tables," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, pp. 69-77.

[46] R.A. Hamilton and G. R. Lezan, "Thyristor Adjustable Frequency Power Supplies for Hot Strip Mill Run-out Tables," IEEE Transactions on Industry and General Applications, Vol. IGA-3, No. 2, March/April 1967, pp. 168-175.

The use of a cycloconverter to control multiple ac induction motors rather than a thyristor dc reversing drive to control multiple dc shunt motors had three advantages: (1) elimination of brush and commutator maintenance ; (2) better tracking of the mill tachometer since the induction motor slip under accelerating conditions was less than the comparable IR drop and speed droop in a dc motor ; and (3) lower shoot-through fault currents under inverting conditions because of the higher inductance of the induction motor combined with the commutating ability of the induction motors.[47]

Despite the increased complexity of the cycloconverter hardware over that of the thyristorized dc reversing drive, the overall system costs were estimated to be the same for several reasons : (1) the cost of the ac motor was about one-half that of a comparable dc motor, thereby leaving more money available for the cycloconverter development ; and (2) the ac motors specifications including frequency, phase voltage, number of poles, number of phases, and allowable current ripple level were made with a view to lowering the cost of the cycloconverter itself.[48]

Four cycloconverters were built, each supplying a number of two-phase six pole induction motors. Two, 60 Hz input, three-phase, one way converters were connected in anti-parallel in each cycloconverter building block. Depending

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[47] Ibid , p. 73 .

[48] Ibid , p. 69 .

on the rating of the cycloconverter, one or more trays of power thyristors were used per building block. But the cycloconverters always had two building blocks because a two-phase output was required.

A bi-polar dc reference voltage from the mill speed control reference was supplied to the sinewave reference generating tray in each cycloconverter. The circuitry in the tray sensed the reference amplitude, polarity, and rate of change providing a two-phase output sinewave reference to the cycloconverter. The frequency of the sinewave reference varied from 13 to 0 to 13 Hz depending on the amplitude of the dc signal, with its phase rotation dependent upon the polarity of the dc signal. The two-phase reference amplitude depended upon both the amplitude and the rate of change of the dc reference signal.

High speed current loops were placed around each cycloconverter building block. The output of dc current transformers was used to compare with the reference tray sinewave output. The output currents were controlled proportionally to the sinewave references. Adequate motor torque was available for acceleration of the motors because the sinewave reference tray sensed the rate of change (acceleration) as well as the amplitude of the reference signal.

Hamilton and Lezan did not mention the criteria they had used for circulating current suppression. An induction motor is a lagging load even when regenerating power to the line. Consequently, current zero detection alone, or current zero detection combined with the changeover of the sinewave reference polarity to a cycloconverter building block could have been used. The authors displayed several oscillograms at the end of the paper showing the two-phase voltage and current waveforms which occurred with motor reversal, first from 4 Hz and then from 11 Hz. The period of current zero during changeover from one converter to another appears from the oscillographs to be about 10 ms

In summary, the paper by Hamilton and Lezan did not reveal any details of cycloconverter control circuitry. However it did present an example of a cycloconverter system in an industrial application that was both a technical and economic success.

In October, 1964 J.C. Guyeska and H E. Jordan of Reliance Engineering in Cleveland, Ohio published a paper describing their use of a cycloconverter in a similar run-out table application.[49] The cycloconverter operated with circulating current, had a three-phase output, and used the anti-parallel combination of six-phase, one way converters in each building block. No power ratings were given for the cycloconverter. The ac motors on the table rolls were supplied with two forward and two reverse speed frequencies plus a stop position under manual control.

3.13 The Lear Siegler Cycloconverter System Papers

Earlier in this chapter, a paper written by R. A. Van Eck of Lear Siegler Inc., Cleveland, Ohio was introduced under subtitle 3.4, as "The First Lear Siegler Article". The paper, presented at the June, 1961 AIEE Aero-Space Transportation Conference, did not mention any practical work carried out at Lear

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[49] J.C. Guyeska and H.E. Jordan, "Static AC Variable Frequency Drive," Proc. National Electronics Conference., Vol. 20, 1964, pp. 358-365.

Siegler, nor did it discuss how circulating current might be eliminated.

In 1961 the U.S. Army Tank-Automotive Center in Warren, Michigan started development work on a cross country, wheeled vehicle. In 1962, the contract for the electric drive system was awarded to Lear Siegler. C.J. Amato joined the Power Equipment Division of Lear Siegler in February, 1962 as a Senior Engineer. As well, L.J. Lawson joined the Lear Siegler Power Equipment Division as Chief Project Engineer, Electronics in 1962. Amato, Lawson and W. Slabiak of the U.S. Army Tank-Automotive Center were involved in the development of the electric propulsion system.

At the November, 1965 Industrial Static Power Conversion Conference in Philaselphia, C.J. Amato presented a paper describing the variable frequency closed loop, controlled slip operation of a three-phase induction motor.[50] In a companion paper,[51] W. Slabiak and L.J. Lawson described the control systems for the heavy-duty, gasoline engine powered, highway and off-highway vehicle that had been in full scale operation for nearly two and one-half years by November 1965.

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[50] C.J. Amato, "Variable Speed with Controlled Slip Induction Motor". IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, pp. 181-185.

[51] W. Slabiak and L.J. Lawson, "Optimizing Control Systems for Land Vehicles," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, pp. 188-189.

At that time the Lear Siegler cycloconverter systems had reached full maturity. Their basic building block was the anti-parallel connection of two, three-phase, two-way converters. The twelve thyristors were mounted in an eight pound, 3.0 x 9.5 x 11.5 inch package using five aluminum heat sinks that were insulated from each other. With 140 CFM of forced air cooling at 50°C, the single building block was rated at 100 kVA with a 440 volt, three-phase input.

Mounted along the 11.5 inch edge were six logic modules using integrated circuits to generate the firing pulses for the 12 thyristors. Six firing modules containing 12 pulse transformers and other components to shape the pulses were mounted beside their logic modules. At one end of the 11.5 inch side was the single-blanking module which generated the blanking logic for the anti-parallel converters. The blanking module used current zero detection alone as its criterion for circulating-current-elimination.[52] An article by G. Pinter of Lear Siegler shows a side-by-side photographic comparison of the control circuitry sizes before and after the use of integrated circuit techniques.[53]

The experimental vehicle had six wheels. Each wheel was provided with a three-phase to three-phase cycloconverter driving an oil cooled, low slip induction motor weighing 167 pounds and having a continuous rating of 200 hp at 12,000 rpm.

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[52] W. Slabiak and L. J. Lawson, "Precise Control of a Three-Phase Squirrel Cage Induction Motor Using a Practical Cycloconverter," IEEE Transactions on Applications and Industry, Vol. IGA-2, No. 4, July/August, 1966, p. 277.

[53] G.E. Pinter, "The Cycloconverter Adjustable Frequency Drive," Machine Design, June 23rd, 1966, pp. 4-11.

Each cycloconverter was manipulated by the control system built around it so as to maintain essentially constant airgap flux level in its induction motor despite the changing of stator frequency with speed control. At the same time, the slip frequency of each induction motor was under individual closed loop control.

Equation 13 in C. J. Amato's paper showed the torque of an induction motor to be[54]

$$T \propto \left(\frac{E_S}{\omega_S} \right)^2 \cdot \frac{\omega_{SL} R_2}{R_2^2 + (\omega_{SL} L_2)^2} \qquad (3.1)$$

where T = the electrical torque

E_S = the airgap voltage; that is, the motor terminal voltage less the stator impedance drop.

ω_S = the stator electrical frequency

ω_{SL} = the electrical slip frequency in the rotor

R_2 = the rotor resistance

L_2 = the rotor leakage inductance.

If the airgap voltage was made directly proportional to the stator frequency as

$$E_S = k \ E_B \qquad (3.2)$$

[54] C. J. Amato, op. cit., p. 182.

with

$$k = \frac{\omega_S}{\omega_B} \tag{3.3}$$

where ω_B = the stator base frequency

and E_b = the airgap base voltage at ω_b and for some specified value of stator current

then torque equation (3.1) could be rewritten as

$$T \propto \left(\frac{E_B}{\omega_B}\right)^2 \cdot \frac{\omega_{SL} R_2}{R_2^{\,2} + (\omega_{SL} L_2)^2} \tag{3.4}$$

Equation (3.4) shows that the torque of an induction motor is proportional only to the slip frequency, ω_{SL}, provided that the volts per cycle ratio $\frac{E_S}{\omega_B}$ remain constantly equal to $\frac{E_B}{\omega_B}$. Of course, maintaining a constant volts per cycle ratio maintains the airgap flux at a constant level.

Hence, closed loop control of slip frequency ω_{SL}, while holding the airgap flux level constant, is equivalent to closed loop control of the induction motor torque. Amato presented Figures 3 and 4 in his paper, reproduced here as Figures 3.3 and 3.4 respectively, to illustrate these facts.

Figure 3.3 is a normalized torque versus normalized slip frequency curve applicable to any induction motor provided that its airgap flux level is held constant. The curve is valid and anti-symmetrical for positive and negative values of slip.

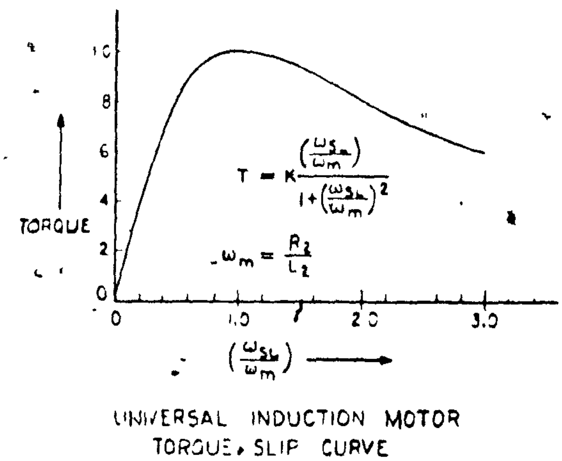

FIGURE 3 *

*C. J. Amato, "Variable Speed with Controlled Slip Induction Motor," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, Figure 3 on p. 183.

FIGURE 3.3. UNIVERSAL INDUCTION MOTOR TORQUE SLIP CURVE (BY AMATO)

The basic block diagram of the Lear Siegler controlled slip system is shown in Figure 3.4. The three-phase frequency converter was made up of three, 100 kVA, three-phase to single-phase cycloconverters described earlier. The three-phase induction motor (also described earlier) had an internally mounted brushless tachometer whose output signal was useable over the entire speed range, including zero speed.[55]

The slip frequency generator was used to change the torque command to a slip frequency reference. Torque limiting (to avoid exceeding the maximum point

[55] C. J. Amato, op. cit., p. 185.

on the torque-slip curve) and other torque optimizing operations[56] were also performed in this block.

The control signal generator (labelled as a mixer-demodulator in another paper[57]) produced a three-phase set of reference signals for the cycloconverter. The frequency of the three-phase set was equal to the algebraic sum of the mechanical frequency plus the reference slip frequency. The phase rotation of the set depended upon the polarity of the algebraic sum of those frequencies. Finally amplitude of the reference voltages was programmed to be proportional to their frequency. This kept the airgap flux level approximately constant.

The induction machine torque and slip frequency followed the torque command signal in closed loop fashion. Motoring operation could be changed to generating operation simply by changing the polarity of the torque command, thereby reversing the slip frequency reference, ω_{SL}. The scheme could be used as an inner torque loop in a speed control system (for example) by obtaining the torque command from the output of a speed regulator. The inputs to the speed regulator would be the reference speed and the tachometer feedback signal, ω_r. The use of an outer speed loop and inner torque (slip) loop for induction motor control

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[56] W. Slabiak and L.J. Lawson, "Optimizing Control Systems for Land Vehicles," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, p. 188.

[57] W. Slabiak and L.J. Lawson, "Precise Control of a Three-Phase Squirrel-Cage Induction Motor Using a Practical Cycloconverter," IEEE Transactions on Applications and Industry, Vol. IGA-2, No. 4, July/August, 1966, p. 274.

is exactly analogous to the use of an outer speed loop and inner torque (armature current) loop for dc shunt motor control.

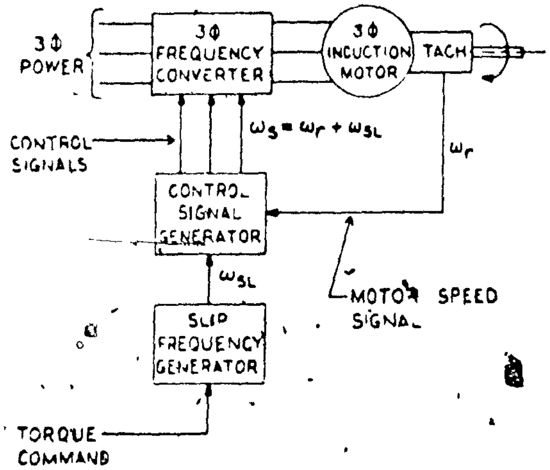

Fig. 4. Motor Control Loop*

*C. J. Amato, "Variable Speed with Controlled Slip Induction Motor," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, Figure 4 on p. 183.

FIGURE 3.4. INNER TORQUE (SLIP) LOOP (BY AMATO)

There is no question that the Power Equipment Division of Lear Siegler had produced an excellent cycloconverter package. Their effort after producing the package was in developing new applications. L. J. Lawson listed ten applications with sixteen reference articles. Quoting from his paper "The Practical Cycloconverter":

> The new frequency converter has been applied with success to the following systems described in the references:
>
> 1) ac electric vehicle drives for land vehicles
> 2) aircraft VSCF generating systems
> 3) servo-controlled antenna drives (both torque-differential antibakclash, and direct driven)

[continuing the quotation]

4) fuel cell cycloinverter
5) shipboard power systems
6) high gain power amplifiers
7) portable gas turbine generating sets
8) rapid transit drives
9) adjustable speed industrial drives
10) locomotive and multiple-unit railway car drives.[58]

The articles are all very similar in contents, differing only in the particular use to which the cycloconverter was put. Lear Siegler revealed all the information it intended to release about the cycloconverter itself in the first two Static Power Conversion Conference papers presented in 1965. Actually, some papers had already been published earlier in 1965 revealing much the same information.

3.14 The AEI Cycloconverter Induction Motor Drive

P. Bowler of Associated Electrical Industries, Manchester, England presented a paper describing controlled slip operation of an induction motor at the IEE Conference on Power Applications of Controllable Semiconductor Devices held on November 10th and 11th, 1965 in London, England.[59] The same cyclo-

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[58] L.J. Lawson, "The Practical Cycloconverter," IEEE Transactions on Industry and General Applications, Vol. IGA-4, No. 2, March/April, 1968, p. 144.

[59] P. Bowler, "The Application of a Cycloconverter to the Control of Induction Motors," Power Applications of Controllable Semiconductor Devices, IEE Conference Publication 17, Part I, November 1965, pp. 137-145.

converter system was also described in the November/December 1965 issue of "AEI Engineering".[60]

The basic building block was the anti-parallel combination of two, six-phase star converters with interphase transformer. Circulating current limit reactors were provided, but circulating current suppression was provided.

Quoting from Bowler's conference paper:

> Two methods of control [of circulating current] are used: firstly a non-overlap method where one or the other group is fired. Secondly an overlap method where the load current is detected and used to remove firing pulses from the unwanted group of thyristors. The firing pulse gating circuits must not operate on the output current ripple and to achieve this a threshold level is to be built into the system. When the output current is below this threshold level, both groups of thyristors conduct and and inter-group reactor is used to limit the circulating current.[61]

The cycloconverter system operates with an inner torque (slip) loop exactly as did the Lear Siegler scheme. An outer speed loop was arranged around the inner torque loop. Positive and negative limits were provided on the output of the speed regulator, limiting its output to less than the pull out torque (slip) of the induction motor. The voltage amplitude of the three-phase reference signals was of the form $V = a + K f_s$ where f_s was the frequency of the reference signals. This kept the airgap flux level approximately constant as the stator frequency was varied.

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[60] P. Bowler, "The Speed Control of Induction Motors Using Static Frequency-Converters," AEI Engineering, November/December, 1965, pp. 286-291.

[61] P. Bowler, "The Application of a Cycloconverter to the Control of Induction Motors," Power Applications of Controllable Semiconductor Devices, IEE Conference Publication 17, Part 1, November, 1965, p. 138.

Bowler briefly described the AEI technique for generating the three-phase reference voltages. First, the motor speed voltage from the tachometer was added to the torque (slip) demand voltage to form a control voltage. Then, quoting from Bowler's paper:[62]

> The control voltage is converted to a variable frequency three-phase voltage of constant amplitude by the block labelled "voltage to frequency converter". This is an electronic circuit using a fixed and a variable frequency oscillator, the output being the difference frequency. The converter being static, has a fast response and can operate through d.c. with a range of 100 c/s. The output reverses its phase sequence as the input "control voltage" reverses polarity.

It is likely that all the developers of cycloconverter controlled slip systems used the same basic scheme. Block diagrams of the scheme for two-phase and three-phase output will be provided in Chapter IV.

Bowler did not specifically mention the upper frequency limit of the cycloconverter, but an oscillogram was in the paper showing induction motor reversal from 20 Hz. This corresponded to a 2.5 to 1 step down ratio from the power line input frequency to the cycloconverter output frequency.

3.15 A Second Siemens Cycloconverter Induction Motor Drive

The first Siemens cycloconverter, described by Heck and Meyer in 1963 used Hall effect devices to measure the airgap flux.[63] The airgap flux was then

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[62] Ibid, p. 138.

[63] R. Heck and M. Meyer, "A Static-frequency-changer-fed Squirrel-cage Motor Drive for Variable Speed and Reversing," Siemens Review, No. 11, November, 1963, p. 403.

controlled directly by varying the amplitude of the current reference signals in such a way that the magnitude of the airgap flux was kept constant. Closed loop current control was used on each motor phase.

F. Wesselak described a second, circulating-current-free cycloconverter operating an induction motor in the controlled slip mode in his article "Thyristor Converters with Natural Commutation".[64] The airgap flux level was kept constant by using subordinated stator control. Induction motor theory shows that for a given machine with constant airgap flux, there exists a functional relationship between the slip frequency and the amplitude of the stator current, independent of the stator frequency.[65]

Using this fact, the Siemens cycloconverter was controlled with its induction motor using an inner torque (slip) loop and an outer speed loop. The Lear Siegler and AEI schemes adjusted the stator voltage amplitude on an open loop basis to maintain approximately constant airgap flux with changing stator frequency. However, the Siemens scheme adjusted the stator currents on a closed loop basis in response to the torque (slip frequency) command at the output of the speed regulator.

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[64] F. Wesselak, "Thyristor Converters with Natural Commutation," Siemens Review, No. 12, December, 1965, pp. 405-410.

[65] A. Schonung and H. Stemmler, "Static Frequency Changers with Subharmonic Control in Conjunction with Reversible Variable-Speed A. C. Drives," The Brown Boveri Review, Aug./Sept. 1964, Vol. 51, No. 8/9, pp. 567-577.

All three schemes have similar results. Because each stator current was under closed loop control, the highest output frequency was limited by loop stability considerations. Wesselak presented current and voltage waveforms for one stator phase (10 Hz, Pf = .91 lagging, motoring operation).

3.16 A Single-Phase to Single-Phase Cycloconverter

In a Fairchild Semiconductor application bulletin, S.A. Schwartz and D. Fleming proposed some novel control circuitry for a single-phase to single-phase cycloconverter.[66] On the basis of their use of 17 transistors, 11 linear IC's, and 31 digital IC's to control the eight thyristors making up the two, anti-parallel, single-phase bridges of the cycloconverter, it might be concluded that they were attempting to develop a new market for Fairchild semiconductors. The multiplicity of components would probably make their scheme uneconomical. The circulating current elimination logic was to operate with current zero information alone making it suitable for leading, resistive, and lagging loads. However no actual oscilloscope waveforms were presented in the paper to indicate that the unit had been successfully tested.

3.17 The First McGill Cycloconverter

T. H. Barton and R.S. Birtch of McGill University published an article

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[66] S.A. Schwartz and D. Fleming, "Single-Phase Control for Cycloconverter," Fairchild Semiconductor Application Bulletin, APP-132, August, 1967, pp. 1-8.

in April, 1967 describing a three-phase to single-phase cycloconverter operating with circulating current.[67] This cycloconverter was fully described by R.S. Birtch in his Master of Engineering thesis "A High Powered Servo-analyzer" submitted in December, 1965 to the Faculty of Graduate Studies and Research at McGill University from the Electrical Engineering Department.

Two, three-phase, two-way converters were connected in anti-parallel through a center-tapped current limiting reactor. The bias-shifted cosine technique was used to ensure a linear d.c. transfer function under open loop conditions when continuous converter current was flowing. Operation in the circulating current mode ensured that current was flowing continuously in each converter, even when a motor armature (back EMF) load was used. The maximum ratings of each converter were 250V at 30 A average.

The paper contained oscilloscope photographs of voltage and current waveforms of the cycloconverter output to a passive, lagging load at 0.5, 5.0 and 50 Hz. The paper also presented some d.c. machine frequency response plots showing illustrating the utility of the cycloconverter as a servo-analyzer.

T.H. Barton and R.S. Birtch concluded that their scheme was robust

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[67] T.H. Barton and R.S. Birtch, "A 5 - kW Low Frequency Power Amplifier of Improved Frequency Response," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-14, No. 1, April 1967, pp. 33-39.

and working remarkably well. However they felt that the thyristor gating pulses were too wide, that the circulating current was sometimes excessive, and that improvements were needed in the current limit circuitry.

3.18 The Brown Boveri Gearless Tube Mill

Ac motor drives have generally been applied in situations where the characteristics of the ac motor itself were definitely required, despite the possible lower cost of a variable voltage dc supply compared to a variable frequency and voltage ac supply. Examples presented up to now have included those with adverse motor environments and high drive performance criteria such as steel mill run-out tables and individual wheel drives in cross country vehicules.[68] However in very large drives, the combination of the rising cost of the dc motor and the possibility of commutation problems with the huge armature currents may again tip the scales in favour of ac motors.

In 1969 Brown Boveri published a series of articles describing an 8700 hp (6400 kW) cycloconverter - synchronous motor drive for a tube mill grinding

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[68] See Sections 3.12 and 3.13 herein.

cement clinker at a Ciments Lambert-Lafarge plant at Le Havre in France.[69, 70, 71] The ~~very~~ large horsepower required precluded using a geared drive, and so the synchronous motor was concentrically wrapped around one end of the mill. The mill itself was 5 m in diameter by 16.5 m in length and the motor airgap diameter was 8 m. The rotor and stator were contained in one air/water cooled, dust proof assembly under positive pressure, while the sliprings and carbon brushes for the rotor field were in another.

The normal maximum operating frequency was 5.5 Hz, which corresponded to 15 r/min for the 44 pole machine. The full speed range was continuously adjustable from a maximum of 20 r/min (7.3 Hz) down to standstill for inching the mill.

Each cycloconverter output phase had its own transformer with paralleled 100 A avg, 3.5 kV peak, mercury-arc, controlled rectifiers arranged in a 12 pulse,

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[69] E. Blauenstein, "The First Gearless Drive for a Tube Mill," The Brown Boveri Review, March 1970, Vol. 57, No. 3, pp. 96-105.

[70] J. Langer, "Static Frequency Changer Supply System for Synchronous Motors Driving Tube Mills," The Brown Boveri Review, March 1970, Vol. 57, No. 3, pp. 112-119.

[71] H. Stemmler, "Drive System and Electronic Control Equipment of the Gearless Tube Mill," The Brown Boveri Review, March 1970, Vo. 57, No. 3, pp. 120-128.

circulating-current-free, H connection The motor windings were connected in three wire star to suppress any third harmonic currents when running at normal speeds However it was necessary to tie the cycloconverter and motor star points together through an impedance for about one-half second when initializing conduction in the three cycloconverter phases.

The control system, described by H Stemmler[72] was very ingenious. The speed, f, of the synchronous motor and mill was measured by an ac tachometer consisting of a small three-phase machine excited with 50 Hz, so that its output was at (50 f) Hz These voltages were then three-phase demodulated in a computing unit which yielded a three-phase sinusoidal signal of constant amplitude at frequency, f, which was in phase with the d - axis of the rotor The computing unit also provided a second three-phase set at 90° from the first set. These two sets of signals were sent to the "stator current desired value unit" which modified their phase position and amplitude to form a single three-phase reference set. This reference set was fed to the three cycloconverters, each of which had closed loop control over one stator current phase. The stator current desired value unit was controlled by two dc analog voltages representing the desired stator current

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[72] H. Stemmler, op., cit., pp. 125-127.

amplitude and the desired stator current phase with respect to the d - axis of the rotor. The desired current amplitude signal fed two function generators. One of the generators provided the desired stator current phase with respect to the d - axis of the rotor (as just mentioned above). The other generator provided the current reference to the thyristor converter supplying the rotor field. The function generators were designed so that for any given desired stator current amplitude, the stator current phase and rotor field current amplitude would be adjusted to keep 1) the magnetic stator flux linkage at full rated value (except for operating with above base speed, field-weakening conditions); and 2) the stator current and voltage in phase. Under these circumstances Stemmler demonstrated that the motor torque was directly proportional to stator current amplitude and not limited by a pull-out torque.[73]

The object of the control scheme was to control the mill speed, hence a speed regulating outer loop with dc tachometer feedback was used to provide the desired stator current amplitude signal. The speed loop output was scaled to limit the maximum torque request to 1.6 times the rated torque. Because the control system for the desired stator current amplitude and phase effectively took

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[73] H. Stemmler, op. cit., p. 124.

one of its references as the d-axis of the rotor itself, the motor could not be pulled out of synchronism The control system suppressed all hunting tendencies and rotor damper windings were not needed The PF of the machine remained at unity for all speeds and loads For lower speeds the system PF was low because the cycloconverter peak voltage was correspondingly low. However at normal speeds of 13 to 15 r/min the cycloconverter output voltage was trapezoidal in shape so that the system PF climbed to 0.86 The three wire star connection of the motor suppressed the third harmonic current which otherwise would have been high due to the trapezoidal waveform. The lack of damper windings further reduced current harmonics In conclusion, the cycloconverter-synchronous machine drive described had control properties equal to those of a dc drive but without the limitations imposed by the commutator

3.19 <u>The Second McGill Cycloconverter</u>

At the October, 1970 IEEE Industry and General Applications Group Meeting, T. M Hamblin presented a paper written with his coauthor T. H. Barton, which was republished in the "IA Transactions".[74, 75] The paper titled "Cycloconverter Control Circuits" forms the core of the material to be presented in Chapters IV and V herein.

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[74] T. M Hamblin and T. H. Barton, "Cycloconverter Control Circuits," <u>IEEE Industry and General Applications Group Annual Meeting Conference Record,</u> October, 1965, pp. 559-570.

[75] T. M. Hamblin and T. H. Barton, "Cycloconverter Control Circuits," <u>IEEE Transactions on Industry Applications</u> Vol. IA-8, No. 4, July/August 1972, pp. 443-453.

3.20 A Note on Polyphase Sinusoidal References

Polyphase cycloconverters require polyphase reference signals with controllable amplitude and frequency. And as explained in Section 3.18, synchronous motor drives require that the phase of the reference set be adjustable as well. An excellent method of obtaining all these controls for synchronous motors has been described in detail by H. Stemmler[76] and reviewed herein.

For controlled slip operation of induction motors at variable frequency the problem is to generate a controlled amplitude, polyphase set which is separated from the motor speed frequency by the desired value of slip frequency. One modern approach is to have the polyphase reference set values stored in large read only memories. The memory contents may then be repetitively interrogated and converted with digital to analog converters to yield a stepped approximation to a polyphase sinewave set. Analog multipliers after the converters may be used to provide amplitude control. An FET dpdt reversing switch located between the outputs of the digital to analog converters and the inputs to the multipliers may be used to reverse the phase sequence. The control logic for sequence reversal should be designed so that it cannot operate the switch unless the analog amplitude control has reduced the sinewave output from the multipliers to an acceptably small fraction

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[76] H. Stemmler, *op. cit.*, pp. 125-127.

of full output.

The method used by most cycloconverter drive manufacturers has employed the principle of polyphase mixing or demodulation.[77, 78] The familiar trigonometric identity for the product of two sinewaves is

$$(A_1 \sin \omega_1 t)(A_2 \sin \omega_2 t) = \frac{1}{2} A_1 A_2 \left[\cos (\omega_1 - \omega_2) t - \cos (\omega_1 + \omega_2) t\right]$$

Hence by multiplying two sinewaves together in an analog multiplier and passing their product through a lowpass filter to attenuate the sum frequency term, a sinewave is obtained which has a frequency equal to the difference in frequency of the two sinewaves.

If a single sinewave is multiplied in three separate analog multipliers with a set of sinewaves at a common frequency, but having a three-phase displacement, (that is, simply a three-phase set), then the three difference frequency sinewaves recovered after the three lowpass filters will also be three-phase.[79] When the frequency of the single sinewave is exactly equal to the frequency of the

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[77] W. Slabiak and L. J. Lawson, "Precise Control of a Three-Phase Squirrel-Cage Induction Motor Using a Practical Cycloconverter," IEEE Transactions on Applications and Industry, Vol. IGA-2, No. 4, July/August, 1966, p. 274.

[78] P. Bowler, "The Applications of a Cycloconverter to the Control of Induction Motors," Power Applications of Controllable Semiconductor Devices, IEE Conference Publication 17, Part 1, November, 1965, p. 138.

[79] H. Stemmler, op. cit., p. 126.

three-phase set, then the three filtered outputs will have dc values which depend upon the phase displacements of the four waves. And best of all, the phase sequence of the three filtered outputs reverses when the sign of the difference frequency changes from positive to negative or vice versa.

If square waves with three-phase displacement are supplied to the analog multipliers, certain additional components will be created at frequencies higher than the sum frequency. But all the high frequency components will be attenuated by the lowpass filters so that again only the three-phase difference frequency will be recovered. Indeed, if three-phase square wave signals are to be used with the sinewave, then the analog multipliers may be replaced with on-off, solid state choppers with no change in results. Or, one author has demonstrated that the filtered outputs will again be three-phase if a three-phase set of sinewaves are fed to three choppers which are driven by a single squarewave.[80]

The outputs of a ring counter arranged to divide its triggering pulse frequency by six may be used as the source of the three-phase squarewave set for the three choppers. These triggering pulses may be created by a stable linear

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[80] S. K. Datta, "A Novel Three-Phase Oscillator for the Speed Control of AC Motors," <u>IEEE Transactions on Industry and General Applications</u>, Vol. IGA-7, No. 1, January/February 1971, pp. 61-68.

voltage controlled oscillator. The sinewave is usually derived from a high purity, high stability, fixed frequency oscillator. Alternately the ring counter may be arranged to divide by four, and only two choppers used so that a two-phase sinewave is obtained after lowpass filtering. The two-phase signals may then be used to create a three-phase set by using operational amplifiers to add and subtract the two phase components in a manner analogous to the Scott transformer connection. The latter method has been described very well by A. Schonung and H. Stemmler.[81] In addition the author presented three alternative schemes for variable frequency, controlled slip operation of an induction motor. His description of the function of the component blocks related very well to an analysis in another part of his paper of the steady state characteristics of an induction motor operated at variable frequency.

3.21 Conclusions

It would be possible to continue reviewing articles right up to the present date. However, the appearance of B.R. Pelly's book[82] on converters and cycloconverters in early 1972 left very little unsaid in the thyristor drive field. His

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[81] A. Schonung and H. Stemmler, "Static Frequency Changers with Subharmonic Control in Conjunction with Reversible Variable-Speed A.C. Drives," The Brown Boveri Review, Aug./Sept. 1964, Vol. 51, No. 8/9, pp. 573-576

[82] B. R. Pelly, Thyristor Phase - Controlled Converters and Cycloconverters - Operation, Control and Performance (New York: Wiley - Interscience, 1970) pp. 434

description and depth of coverage of circuit configurations, expected waveforms, discontinuous current operation, firing pulse circuitry, harmonic analysis of waveforms, and drive component sizing were all excellent.

W. McMurray's book on cycloconverters[83] was just in the final stage of preparation when Pelly's book was published. McMurray acknowledged this in the preface of his book and stated that,

> . . . . the emphasis of Pelly's work differs considerably from the treatment presented here, and there is surprisingly little duplication considering the similar subject matter.[84]

McMurray's book provides more information than did Pelly's on modelling of the cycloconverter for simulation of the drive. In addition he presented practical information on thyristor snubber design, on choosing thyristor ratings, and on a number of other items to be considered when designing cycloconverter drives.

Several of the papers reviewed in this chapter have been reprinted in an IEEE Selected Reprint Series two volume collection titled "Power Semiconductors Applications".[85] The collection provides an excellent survey of the thyristor drive industry and also included an extensive bibliography of papers not reprinted in the collection.

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[83] W McMurray, The Theory and Design of Cycloconverters, (Cambridge Massachusetts: The MIT Press, 1972) pp. 165.

[84] Ibid., [Preface page].

[85] J.D. Harden, Jr. and F.B. Golden (editors), Power Semiconductor Applications (New York : IEEE Press, 1972), Vol. 1, pp. 555 and Vol. II, pp. 344.

Because of the attempt to point out in some detail the progress made by various companies and individuals, this chapter has become quite lengthy. In fact perhaps these contributions have been obscured by the detail, so the list below is presented as a summary of the more important points:

1. In March, 1959 Chirgwin, Stratton, and Toth of Jack and Heintz in Cleveland, Ohio submitted the first description of circulating-current-free cycloconverters for use in VSCF systems.

2. S. Zurcher from Brown Boveri described their circulating-current-free, reversing supplies for armature or field control in November 1961.

3. Heck and Meyer of Siemens Works in Germany described the closed loop speed control of a three-phase induction motor using a circulating-current-free cycloconverter in November 1963.

4. In 1963, Amato and Lawson of Lear Siegler in Cleveland, Ohio and Slabiak of the U.S. Army Tank-Automotive Center perfected the controlled-slip method of torque control of an induction motor connected to a circulating-current-free cycloconverter. Starting in 1965, Lear Siegler employees published a flurry of papers describing various applications for their cycloconverter systems.

5. Duff and Ludbrook of Canadian Westinghouse published an excellent article in June 1965 describing their circulating-current-free dc reversing drive which was used as a power amplifier in an armature current control loop.

6. In November, 1965 Bowler of AIE, England published a description of an AEI cycloconverter with suppressed circulating-current operating an induction motor in the controlled slip mode.

7. Wesselak of Siemens Works published a paper on December, 1965 describing a similar drive with inner armature current loops and an outer speed loop. The same paper also described a Siemens circulating-current-free cycloconverter system for controlled slip operation of an induction motor.

8. Hamilton and Lezan's paper in November, 1965 related General Electric's experience with the open loop speed control of runout table motors in a hot strip mill using a two-phase output cycloconverter.

9. In 1969 Lidberg reported on ASEA's new circulating-current-free d.c. reversing drives. The YHMB style of drive was unusual in that it had one converter followed by a thyristorized, armature reversing switch to permit armature current reversal.

10. Books by B. R. Pelly and W. McMurray published in 1971 and 1972 respectively gave converter and cycloconverter design on a firm practical and theoretical basis. Two volumes of selected reprints by the IEEE Press titled "Power Semiconductor Applications" published in 1972 brought many valuable papers together in book format.

CHAPTER IV

CYCLOCONVERTOR CONTROL CIRCUITRY FOR OPERATION WITH CIRCULATING CURRENT

4.1 Introduction

The basic technique of bias-shift phase-control was illustrated in Chapter II with several diagrams, oscilloscope photographs, and accompanying written description. The photographs showed the operation of a successful three-phase to single-phase cycloconvertor both with and without circulating current. This chapter will describe the thyristor gating circuitry of that cycloconvertor for operation in the former mode. This circuitry has been previously presented in block diagram form in an IGA conference paper written by T. M. Hamblin and Dr. T.H. Barton,[1] and the text and illustrations of this chapter follow closely those of the paper.

4.2 The Cycloconvertor Connection

Figure 1.1 in Chapter I gave the two configurations possible for a three-phase to single phase cycloconvertor connected to a single, three-phase transformer secondary. However, the cycloconvertor described in this Chapter uses two, three-phase secondaries connected as in Figure 4.1. This connection has no definite ad-

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[1] T.M. Hamblin and T.H. Barton, "Cycloconvertor Control Circuits," IEEE Conference Record of the 1970 Fifth Annual Meeting of the IEEE Industry and General Applications Group, 70-C51GA, Chicago, October 1970, pp. 559-571.

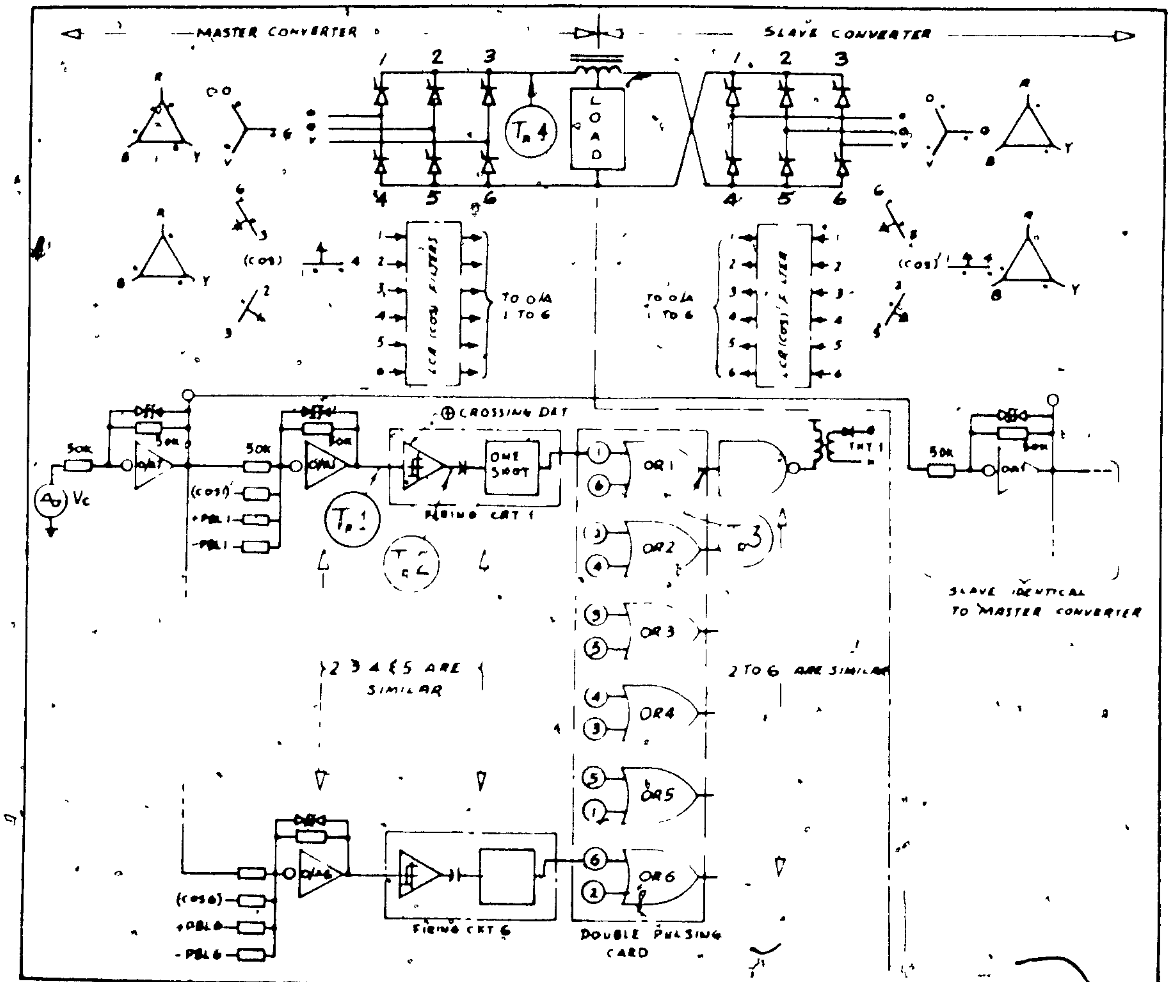

FIGURE 4.1 THREE PHASE TO SINGLE PHASE CYCLOCONVERTOR

vantage over that of Figure 1.1B, except that it permits separation of the convertors for other uses. In fact the convertors were built as a matched pair, and each was mounted in its own cabinet (Figure 4.2). Note that only one current limiting reactor is needed in this connection because the separate three-phase

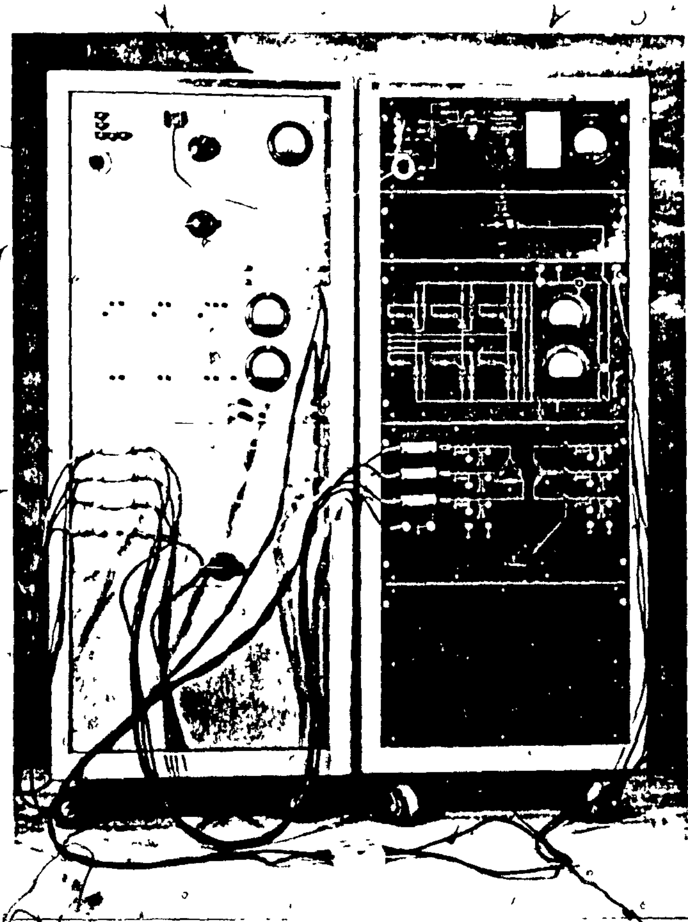

FIGURE 4.2. THE CONVERTERS (FRONT VIEW)

secondaries force the 360 Hz (fundamental component) circulating current completely through both bridges. On the other hand, the connection of Figure 1.1B requires two reactors, each of which handle circulating current with both 180 Hz and 360 Hz fundamental frequencies.

4.3 Thyristor Firing Pulse Generation Circuitry

The bias-shift method of phase control, as outlined in Chapter II, has the advantage of providing a linear control voltage to average convertor output voltage relationship when the convertor current is continuous. Hence if both convertors in Figure 4.1 have continuous current flow, then their output voltages at the load terminals will be in dc balance. This balance is due to the anti-parallel connection combined with the use of the negative of the master convertor control voltage as the control voltage for the slave convertor. Because of this dc balance condition, circulating current between the two convertors will be at a minimum. Of course, balance can be maintained steadily only if the control voltage (V_c) is itself a constant. If the control voltage is varied sinusoidally (or otherwise) with increasing frequency, then there will be a general trend to increasing circulating current (compared with the load current amplitude) due to the discrete nature of the convertor firing pulse occurences and the increase of the self-induced circulating current.[2]

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[2] See Sections 2.3 and 4.9.

The bottom half of Figure 4.1 shows in block diagram form how the bias-shift method of phase control was actually implemented. The negative of the control voltage, V_c was supplied through unity-gain inverting amplifier 0/A7 to six summing invertors 0/A1 to 0/A6 in the master convertor. A six phase set of cosine wave voltages was filtered by LCR low pass filters which contributed negligible phase lag at 60 Hz Each inverting summer added the negative of the control voltage to its particular filtered cosine waveform (ignoring the +PBL and -PBL signals for the moment). Each of the six positive-going crossing detectors (or level detectors) triggered its own one-shot multivibrator at the instant of positive going voltage zero crossing at the output of its particular inverting summer. Each one shot pulse was then amplified, passed through the double pulsing card (to be described later), further amplified, and finally sent through an isolating pulse transformed to gate its thyristor. The circuitry of the slave convertor is identical to that of the master convertor except that the output of its unity-gain inverting amplifier 0/A7 does not run back to the other convertor.

Plates 1 and 2 in Appendix I are wiring diagrams showing full circuitry details for the operational amplifiers and the firing circuit cards. Each firing circuit card contains a Schmitt trigger type of zero crossing detector (Q1, Q2) followed by a one-shot multivibrator (Q3, Q4, Q5). The operation of these circuits is completely explained by Millman and Taub in their book and therefore will not be described herein [3] The purposes of the several diode gates, two amplifying stages, and

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[3] J. Millman and H. Taub, Pulse Digital and Switching Waveforms (New York : McGraw-Hill, Inc., 1965), Chapters 10 and 11).

an additional one-shot multivibrator which appear on the board will be explained in Sections 4.6 and 5.5.

Note that the above scheme is analogous to the "alternate approach" for the three-phase, one-way connection mentioned on page 20 of Chapter II since only the positive going voltage crossings are detected. Using both positive and negative crossing detectors as described in Chapter II (and as by Duff and Ludbrook[4]) would have cut in half the number of inverting summers and crossing detectors. Figure 4.3 demonstrates how this may be done. The cosine wave relations would be identical to those in Figure 4.1 and the thyristor numbering system was shown in Figure 1.1B.

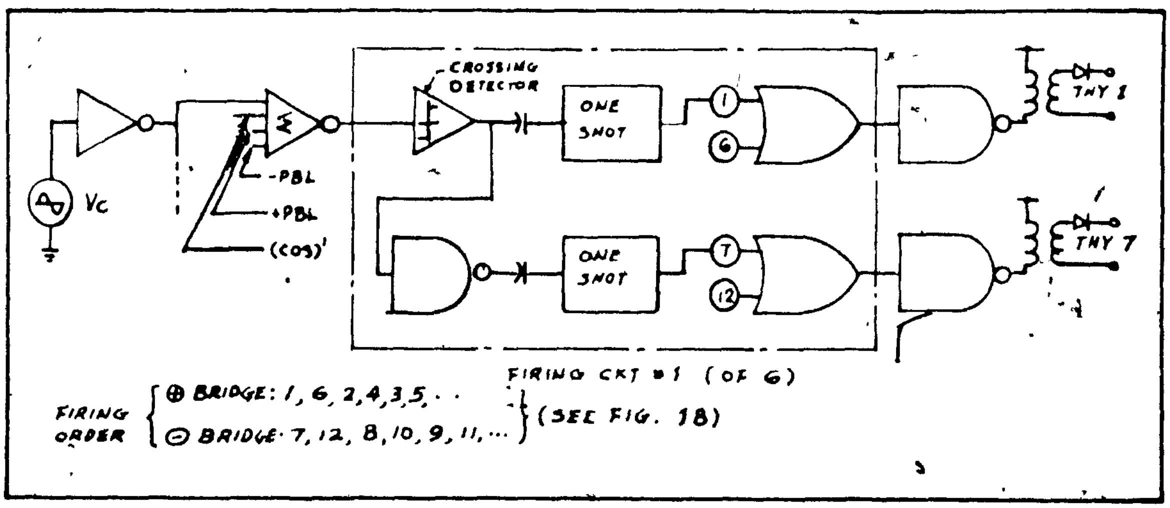

FIGURE 4.3. POSITIVE AND NEGATIVE CROSSING DETECTION

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[4]D. L. Duff and A. Ludbrook, "Reversing Thyristor Armature Dual Convertor with Logic Crossover Control", IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June 1965, pp. 216-222.

4.4 Phase Forward and Phase Back Limit

Figure 4.4 is an oscilloscope photograph of the thyristor firing circuitry waveforms with the control voltage held constant at +5.0 volts (0.5 p.u.) to yield a phase-back angle of $\alpha = 60^{\circ}$ in the master convertor ($\alpha = 120^{\circ}$ in the slave convertor). The four points in the circuity corresponding to the oscilloscope

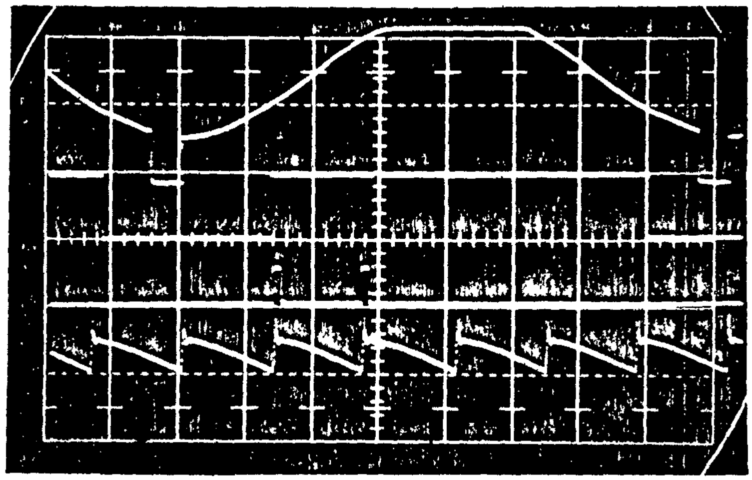

FIGURE 4.4 FIRING CIRCUIT WAVEFORMS

Sweep = 2ms/cm; V = +5V, hence $\alpha = 60^{\circ}$

Trace 1: $-(V_{\cos 1} + V_c)$, scale 10V/cm.

Trace 2: Schmitt trigger output; scale = 10 V/cm.

Trace 3: Double pulsed firing pulses; scale = 5 V/cm

Trace 4: Convertor output voltage; scale = 420 V/cm

traces have been marked on Figure 4.1. Trace 1, the displaced cosine wave equal to the sum of $+V_c$ and $-(\cos 1)'$, has been modified by the zener diode clipping circuit around inverting summer 0/A1 and by the addition of phase-forward and phase-back limit pulses (+PBL and -PBL) at the summer input. The latter pulse is not visible in Trace 1 because of the zener clipping at +11 volts. If however V_c had been -5.0 volts ($\alpha = 120^{\circ}$ in the master convertor), then the -PBL pulse would have been visible while the +PBL pulse was clipped.

The trailing edge of the +PBL pulse acts as a phase-forward limit by ensuring that a positive going zero crossing will occur at the detector input no earlier than the instant $\alpha = 0^{\circ}$ even though the control voltage V_c may be equal to or greater than the peak value of the cosine wave (normalized to 10.0 volts peak). The -PBL pulse acts as a phase-back limit by ensuring that a positive going crossing shall occur no later than its leading edge even when V_c is more negative than the peak of the cosine wave. The front edge of the -PBL pulse is readily adjustable and is normally set for $\alpha = 165^{\circ}$ to limit the maximum phase back angle so that the necessary volt second margin for successful commutation will always exist.

The twelve separate pulses needed per convertor (six + PBL and six -PBL) were generated on three phase-back limit (PBL) cards, one of which appears in block diagram form with explanatory waveforms in Figure 4.5. Note that the four outputs taken from one card supply two thyristors which are connected to the same three-phase supply line. Hence PBL card 2 supplies thyristors 2 and 5 and PBL card 3 supplies 3 and 6. Plate 3 in Appendix I is a schematic diagram of the PBL card. Comparison of this Plate with Figure 4.5 shows that diodes D1 and D2 form OR1,

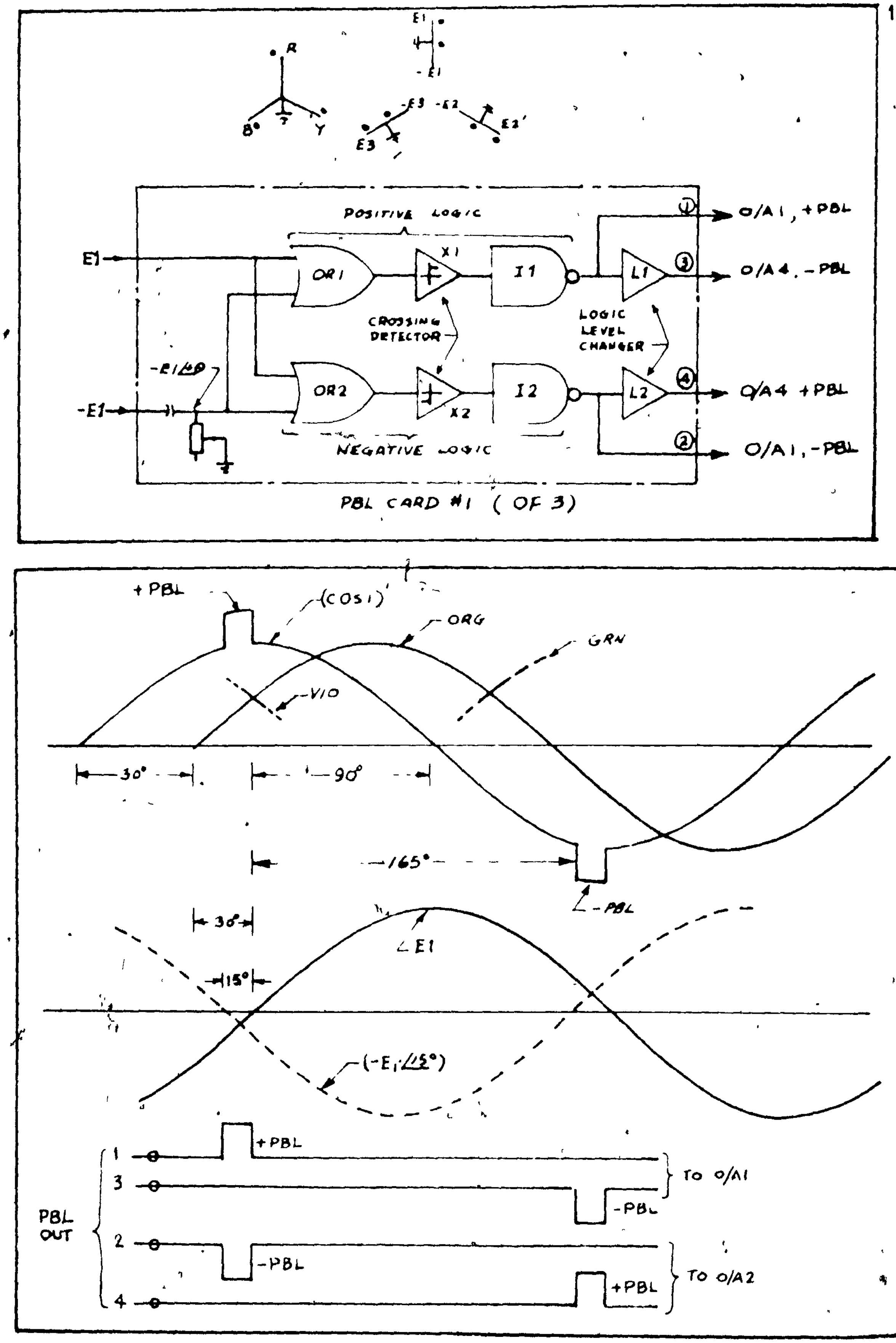

FIGURE 4.5 PHASE BACK LIMIT CARD AND ITS PHASE RELATIONSHIPS

and differential pair Q5, and Q7 make up crossing detector X1. Also, Q1 is inverter I1, and Q4 is the positive logic to negative logic level changer L1. The second half of the card is an NPN to PNP mirror image of the first. Study of the ideal waveforms will quickly reveal how the +PBL and -PBL pulses were generated to supply to O/A1.

LCR filters (not shown in Figure 4.5) identical to the cosine wave filters were used for the E1 voltages while the -E1 voltages were left unfiltered. Although no noise problems were encountered in the PBL cards it would have been prudent to take advantage of the 30° and 60° leads available from the 12 phase supply to permit the use of RC lag filters to supply voltages +E1 and -E1. A more modern approach to the PBL card design would be to use IC zero crossing detectors to square the previously filtered and phase shifted sine waves. Then gates, inverters, and logic level changes to generate the four pulses per card would be arranged to follow after the crossing detectors.

4.5 The Double Pulsing OR Matrix

The detection of the positive going zero crossing of a summer amplifier output (Traces 1 and 2, Figure 4.4) triggers a 200 μ sec. firing pulse (Trace 3). This pulse, after amplification and isolation, gates its thyristor (Trace 4). Examination of Traces 3 and 4 indicates that a second pulse is then applied to the same thyristor when the next thyristor is gated in the normal (1, 6, 2, 4, 3, 5) bridge convertor thyristor gating sequence. Indeed, in order to ensure that a load current path exists through both the top and bottom halves of the bridge convertor for at least the duration of the thyristor gating pulse, a second pulse is always applied simultaneously to the thyristor last gated on the other half of the bridge. Since the firing sequence is fixed, this double pulsing operation is carried out quite simply by the diode OR matrix outlined in Figure 4.1. Hence, when thyristor 6 is gated a second pulse is automatically sent to thyristor 1. Then, gating thyristor 2 will regate thyristor 6 and so on.

It is possible to avoid the double pulsing scheme by using long firing pulses (greater than 60° wide at line frequency) so that the pulses overlap when the phase back angle α is steady. However there are three advantages to be found in the use of the double pulsing OR scheme with short firing pulses :

1. The pulses always overlap no matter how rapidly the convertor is being phased back.

2. A smaller pulse transformer may be used with shorter pulses.

3. It is prudent when operating a circulating-current free cycloconvertor (to be discussed in Chapter V) to consider a convertor to be "on" whenever its thyristors are being gated, even though the load current of that convertor may be zero at that moment. The use of short pulses minimizes the length of such intervals.

However, if wide pulses and double pulsing are combined there is much less tendency for a cycloconverter normally operated with circulating current to drop out of conduction on light loads than if narrow pulses and double pulsing were used.

Plate 4 in Appendix 1 is a schematic diagram of the double pulsing OR matrix card. Note that the purpose of the six firing pulse delay circuits on the card will be discussed in Chapter V since they are required only for circulating-current free operation.

4.6 Alpha Blanking

The normal range of phase-back angle α is from the phase-forward limit of 0° to the adjustable phase-back limit usually set at 165°. Outside of this range there are no positive going zero crossings to be detected when the control voltage has a steady dc value. However with a sufficiently rapid positive increase in control voltage, it is possible for the output of one or more of the summing invertors to cross zero volts in the positive direction during the interval which would correspond to $180^{\circ} < \alpha < 360^{\circ}$ for that particular firing circuit. This positive crossing would cause the simultaneous generation of a least two spurious pulses because the first pulse would be duplicated by the diode OR matrix. Of course, at the same time legitimate firing pulses ($0 < \alpha < 165^{\circ}$) may occur due to the sudden increase in control voltage.

If the overlap in time of legitimate and spurious pulses affects two thyristors connected to the same input phase of a convertor, and if the convertor has been inverting power back to the ac line immediately before the positive change in control voltage, then an inversion shoot-through fault will occur through those two thyristors. That is, the load current will bypass the convertor transformer and flow directly through the two thyristors establishing a free-wheel path. This type of fault may be very severe if it occurs in a three-phase to single-phase cycloconvertor connected to an active, low impedance load such as a motor armature. For three-phase to three-phase cycloconvertors driving induction motor loads, the magnitude of the fault current will be smaller because of the reactance of the motor. However, in either case it is still very desirable to prevent any spurious gating.

The overlap of legitimate and spurious firing pulses occurs more readily with long than with short pulses because the control voltage need not change as rapidly in order to cause the overlap. However even with very short pulses, if α is near 120°, then just a small jump in control voltage occuring at exactly the wrong moment will cause a shoot-through. Figure 4.6 illustrates how the positive step of control voltage created legitimate firing pulses 1 and 5 plus spurious pulses 3 and 4. Since thyristors 1 and 4 are connected to the same (orange) input phase on the bridge, the active inverting load will immediately establish a free-wheeling load current through them. The amplitude of this current may in turn be large enough to cause a commutation failure when thyristor 6 is gated. A large braking torque will probably be applied to the motor before the fault is cleared by one or more of the following occurences: thyristor failure, individual thyristor fuse clearances, dc breaker trip (if one is provided), or natural commutation. Except for the natural commutation case, the motor will be at least temporarily disconnected from the convertor because of the fault.

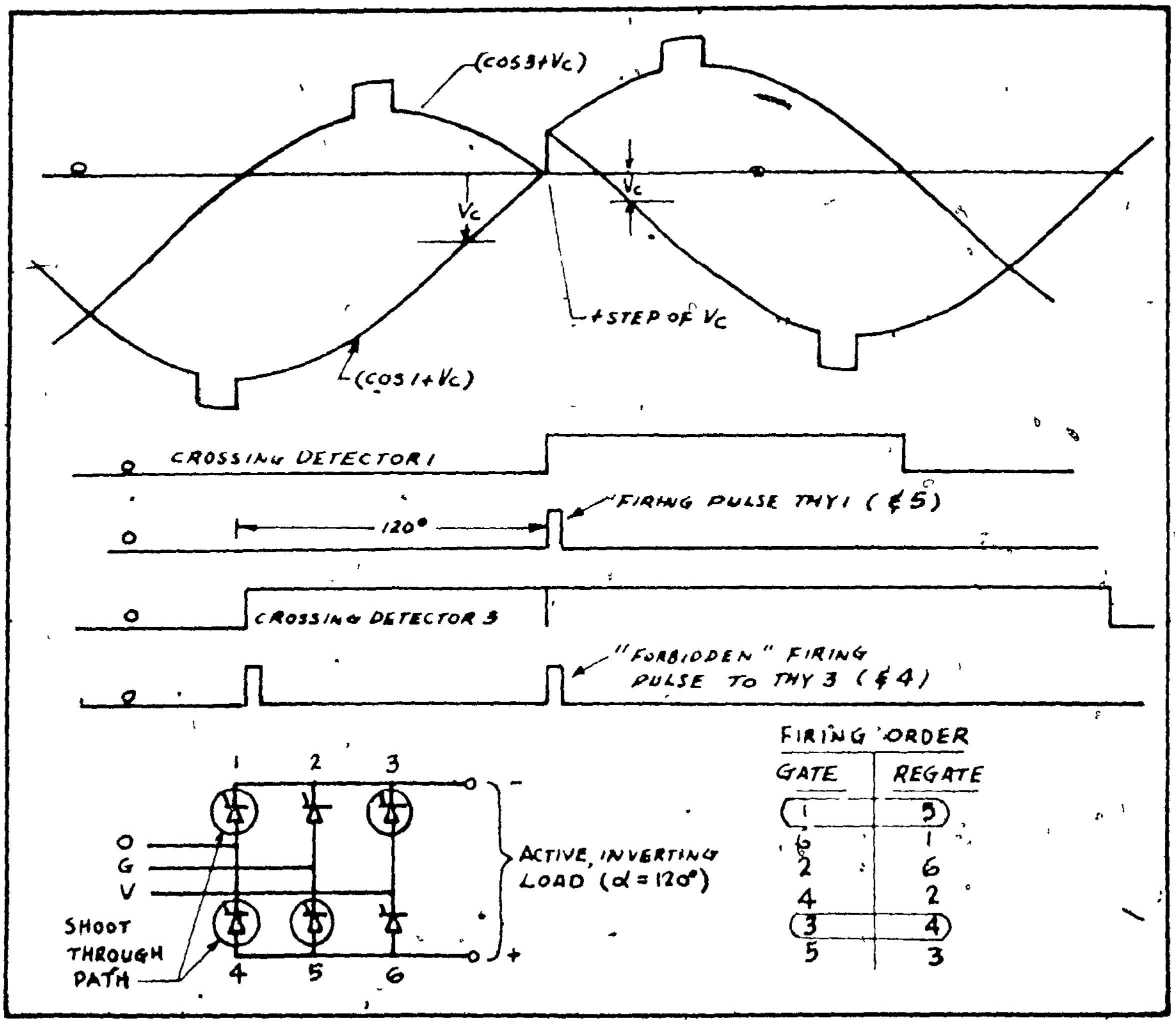

FIGURE 4.6. SHOOT THROUGH, α = 120°.

The production of such spurious firing pulses is suppressed by the alpha blanking card in each convertor. This card generates six separate blanking signals that are supplied to NAND gates in each of the six firing circuits. The alpha blanking signals are arranged to be at the logic zero level for $180^\circ < \alpha < 360^\circ$ so as to blank any firing pulse generated in a given card during that interval (See Figure 4.7 and Plate 5, Appendix I). Diode clamp AND1 connected to the output of one-shot multivibrator OS1 in Figure 4.8 (also see diode D9 in Plate 2, Appendix I) blocks all pulses during the forbidden interval. Similarly AND3 suppresses the output of the memory one-shot. This one-shot is needed only for circulating current free operation, which will be described in the next chapter.

4.7 Thyristor Gating

When the cycloconvertor was first constructed, long firing pulses (approximately 75° wide at 60 Hz) were used for triggering purposes. In order to simultaneously provide a gating pulse with short rise-time (less than several μs) and long duration (75° = 3480 μ sec.) each pulse transformer was wound on an Arnold Engineering 4 mil Deltamax toroidal core type 3T5233-D4-AA with 1.5 inch outside diameter and .094 in^2 cross section. A tertiary winding connected to an effective constant current source provided a reset MMF to prevent saturation of the core by the unidirectional firing pulses. The 250 turn primary, 275 turn secondary and 150 turn tertiary windings were each distributed completely over the core to minimize leakage inductance between them. The three windings were insulated from each other by two layers of Scotch brand electrical tape between each winding. When the gating scheme was changed to short double pulses (200 μs each)

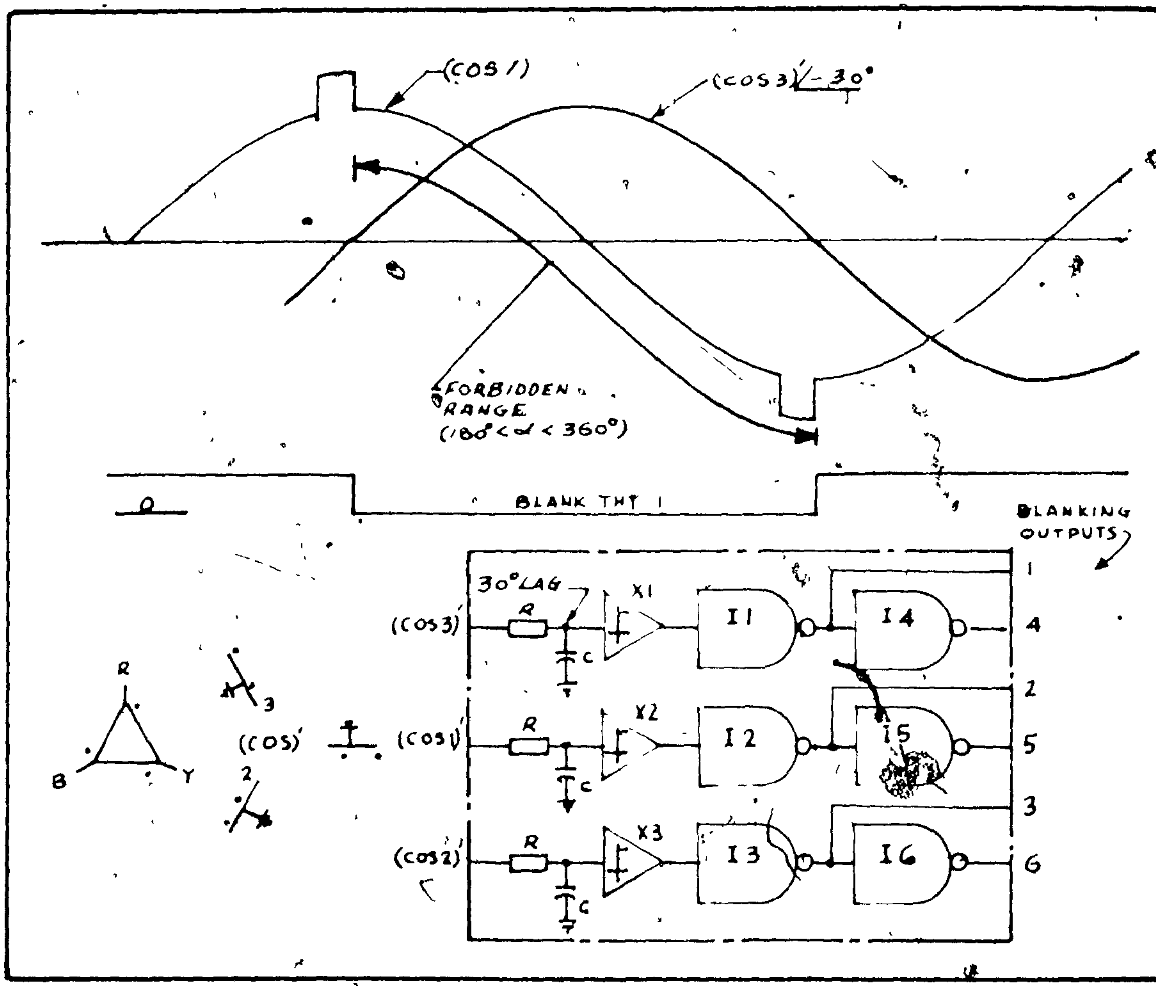

FIGURE 4.7 ALPHA BLANKING CARD

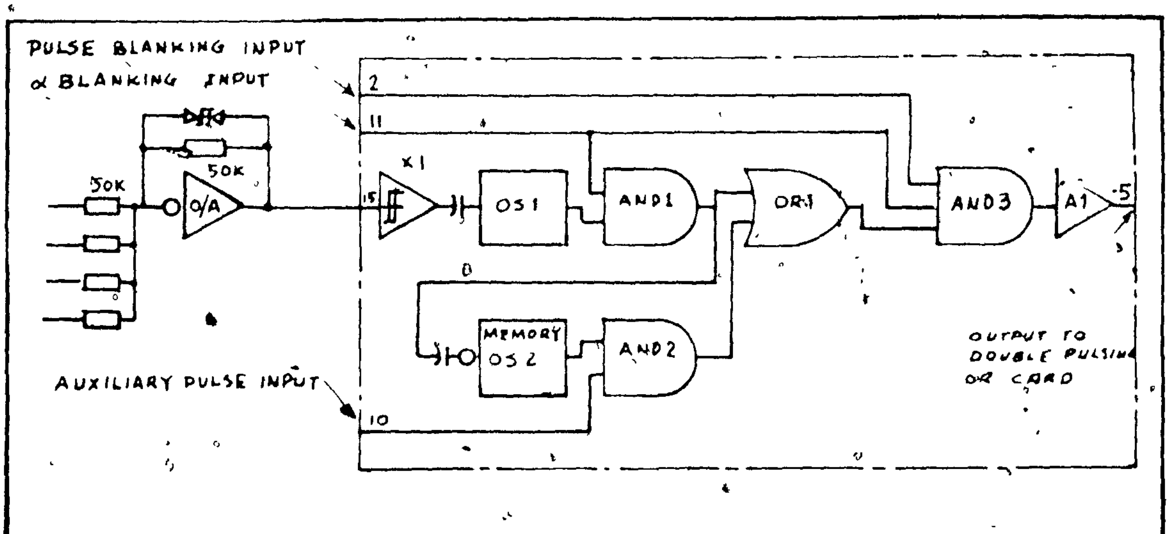

FIGURE 4.8. FIRING PULSE CARD

the transformers were not reduced in size because the pulse rise-time was already sufficiently short to ensure efficient thyristor gating. Plate 6 in Appendix I is a schematic diagram of the pulse amplifier power supply, constant current supply, pulse amplifiers, and pulse transformers. Design details on thyristor gating itself may be found in several thyristor application manuals.[5,6]

4.8 Current Limit

In many cases cycloconvertor drive systems (both ac and dc) are set up with the cycloconvertor inside a current control loop so that there is no need for a spill-over type of current-limit in the individual convertors. However since this particular cycloconvertor is often opertated open-loop in the laboratory, a spill-over current limit (Plate 1, Appendix I) has been permanently installed in each convertor. Current transformers CT1, CT2, CT3 have wye connected secondaries (matching the delta to wye power transformer) so that the convertor output current waveform is correctly reassembled by the diode bridge D1 to D6 with minimum possible ripple. C1 combined with R30 provide a wide range of current feedback signal filtering. Ganging R30, R31, and R32 keeps the current limit knee point

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[5] F.W. Gutzwiller (ed.), The GE SGR Manual (fourth edition; Chicago: The General Electric Company, 1967), Chapter 4.

[6] R. Murray, Jr. (ed.), Westinghouse Silicon Controlled Rectifier Designers' Handbook (first edition. Youngwood, Penn: Semiconductor Division, Westinghouse Electric Corporation, 1963), p. 5-9.

(set by R33) approximately constant as the filter time constant is adjusted. Rheostat R38 sets the dc gain in combination with R30 and R31. The 0.5 volt cutin voltage of diode D8 keeps the current limit signal line completely "clean" when the convertor current limit is below the current limit knee. In practice, the current limit is very easily adjusted for a new type of load without any need for preliminary analysis of the control system stability. When the cycloconverter forms part of the inner current loop for a dc armature supply, the knee points of the spillover current limits built into the converter must be set above the maximum current demand that can be made by the outer speed loop. If this is not done, ill defined limit cycles may be caused by the interaction of the current loops.

4.9 Protection Against Fault Currents

The cycloconverter described herein relies upon the internal spillover current limits to keep the normal load current within the continuous ratings of the thyristors. Fault currents caused by such things as load short circuits are interrupted by Chase - Shawmutt A25X30 Amp Trap thyristor fuses. The coordination of the thyristors and the fuses was performed by R.S. Birtch when he built the first McGill cycloconverter. As he explained, the thyristors, fuses, and current limit must be coordinated together on a current versus time basis.[7]

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[7] R.S. Birtch, "A High-powered Servo-analyser"(M. Eng. Thesis, McGill University, 1965) pp. 22-24.

The fuses were placed on the secondary of the delta-wye transformer as shown in Plate 8. Because these fuses are not in the path of inversion faults (shoot throughs) which may occur with counter EMF loads such as motor armatures, additional A25X30 fuses were connected on the dc side of the converters as shown in Figure 4.8. The dc side fuses remained in the same positions for protection against inversion faults when the drive was used in the circulating current free mode which did not require the circulating current limiting reactor to be used.

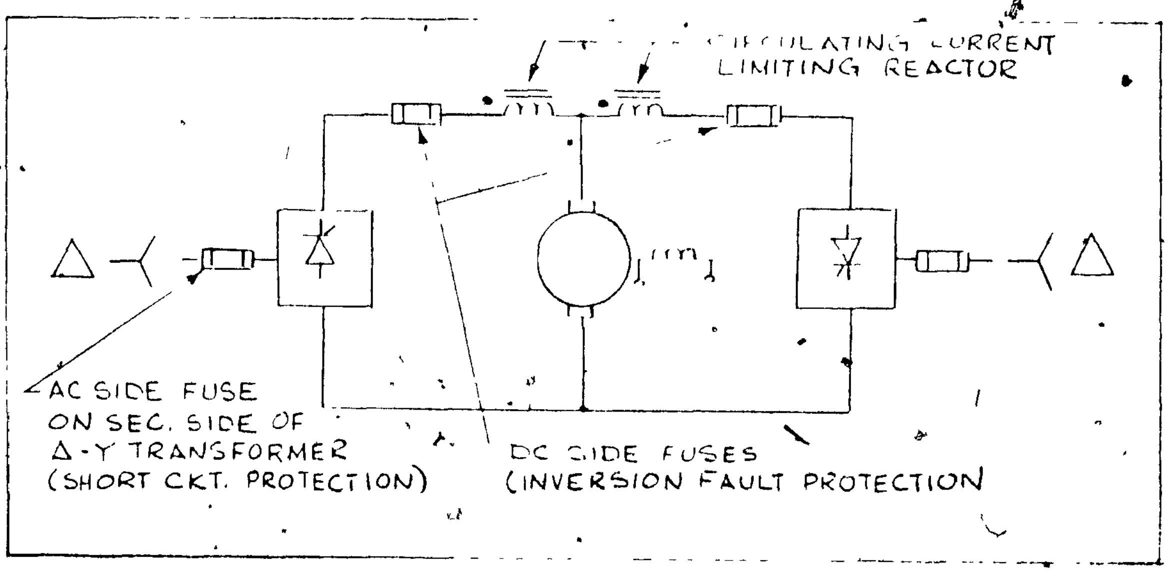

FIGURE 4.9. ONE LINE DIAGRAM SHOWING FUSING

The fusing and current limit scheme described above has worked well and there has never been a thyristor failure despite many faults caused by human errors during testing, development, and laboratory usage. However it is not uncommon for very large drives to contain several hundred thyristors, each with its own fuse. It is not acceptable under such circiumstances to make the fuses the first line of defence against faults. Most manufacturers follow a carefully coordinated scheme involving ac circuit breakers on the ac side, individual thyristor fuses, and dc breakers on the dc side of the converters.[8-11]

4.10 Protection Against Voltage Transients

At the power level chosen (250 Vdc, 30 A dc maximum) there was no need to to operate thyristors in series to increase the voltage blocking capacity, nor in parallel to increase the current carrying capacity. Hence the parallel resistive dividers to force voltage sharing and series inductors to force current sharing by combination of thyristors were not required either.

However it was necessary to use LRC networks to prevent dv/dt triggering of thyristors which were supposed to remain in the blocking condition while thyristors were commutating in other parts of the bridge. The leakage inductances of the three

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[8] F.W. Gutzwiller (ed.), The GE SCR Manual (fourth edition; Chicago: The General Electric Company, 1967), Chapter 14.

[9] D. L. Duff and A. Ludbrook, "Reversing Thyristor Armature Dual Converter with Logic Crossover Control," IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June, 1965, pp. 216-222.

[10] H. Pisecker, "Semiconductor Converters for Electric Drives," The Brown Boveri Review, October 1966, Vol. 53, No. 10, pp. 685-686.

[11] L. F. Stringer, "Thyristor D-C Drive Systems for a Non-Ferrous Hot Line," IEEE Conference Record of the Industrial Static Power Conversion Conference, 34C20, Philadelphia, Pa., November 1965, pp. 43-44.

phase transformer act as an inductive voltage divider during the commutation of current from one thyristor to the next. This means that the output voltage of the bridge has the familiar commutation notches. The height of the step to the notch is one-half of the phase-to-phase commutating voltage which exists for that particular firing angle (neglecting transformer series resistances). Examining the circuit voltages around a loop through the bridge shows that this notch voltage also appears as a positive going voltage step to the thyristor in the other half of the bridge which is connected to the same phase as the thyristor entering conduction. If the firing angle α is 120° or more, the thyristor in the other half will be already blocking a forward (positive) voltage when the positive going step is applied to it. The rate of rise of the voltage (dV/dt) applied to the blocking thyristor exceeded several hundred volts per microsecond before a choke was put in series with each thyristor as shown in Plate 8 of Appendix I. Neglecting the capacitor of the RC snubber across the thyristor permits calculating the initial dV/dt which will be found to depend upon the line-to-line secondary voltage, the transformer leakage inductance, the inductance in each thyristor leg, and the resistance value in the RC snubber. Two excellent articles, one by J.B. Rice and L.E. Nickels of Allis Chalmers and the other by G. Irminger of Brown Boveri explain how the circuitry of the bridge may be simplified for analysis of the initial dV/dt.[12, 13] The latter article also

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[12] J.B. Rice and L.E. Nickels, "Commutation dv/dt Effects in Thyristor Three-Phase Bridge Converters," IEEE Transactions on Industry and General Applications, Vol. IGA-4, Nov./Dec. 1968, pp. 665-668.

[13] G. Irminger, "Thyristor Circuitry," The Brown Boveri Review, October 1966, Vol. 53, No. 10, pp. 663-664.

had an equivalent circuit which proved that the thyristor leg inductors need not be air core types. Saturating inductors are almost as effective as linear ones. For this reason the thyristor leg inductors for the cycloconverter described herein were wound on small toroidal Deltamax cores without airgaps. The final circuit values for the RC snubber were chosen by experiment to be 15 ohms and 0.25 μF. The inductor consisted of 19 turns of number 12 AWG copper in Flameseal insulation on an Arnold 3T5387L4 Deltamax core. The dv/dt to the thyristor did not exceed 5V/μs with these component values Not attempt was made to optimize the design, but articles have been written on this topic.[14, 15, 16]

Because of the charge stored in the junction regions of a thyristor during its conduction period, it does not immediately go to the blocking state when the current through it reaches zero. Instead, driven by the commutating, the current reverses and continues changing at the same rate until the stored charge has been swept out by the current or absorbed by carrier recombination.[17]

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[14] J. B. Rice, "Design of Snubber Circuits for Thyristor Converters," Power Semiconductor Applications, Vol. 1 (New York: IEEE Press, 1972), pp. 21-24.

[15] W. McMurray, "Optimum Snubbers for Power Semiconductors," Power Semiconductor Applications, Vol. 1 (New York: IEEE Press, 1972), pp. 33-41.

[16] W. McMurray, The Theory and Design of Cycloconverters, (Cambridge, Massachusetts: The MIT Press, 1972), pp. 100-105.

[17] J.B. Rice and L.E. Nickels, op. cit., p. 668.

Once this has occurred the blocking capability is quickly regained and the current snaps off. The snap off is so rapid that if the RC snubbers were not placed across the thyristor, the thyristors could possibly be destroyed by overvoltages caused by the leakage inductances of the transformer. In addition the sudden rise of voltage may cause dV/dt triggering of the thyristor in the other half of the bridge which is connected to the same phase. Rice and Nickels have established that the dV/dt induced by the thyristor reverse recovery transients is generally less severe than that induced by turn-on.[18] Consequently the LCR snubbers for the turn-on transient dV/dt will also handle the turn-off transient.

The six diode bridge with RC load in Plate 8 is used to protect the thyristors against overvoltage when the primary supply to the transformer is disconnected. The bridge also helps to suppress overvoltages due to the reverse-recovery snapoff of the thyristor current. Sometimes RC networks without the diode bridge are attached to the transformer secondary to decouple the leakage inductances of the transformer from the snubber circuits of the bridge.[19] These did not prove to be necessary for the cycloconverter described herein.

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[18] Ibid., p. 669.

[19] G. Irminger, op. cit., pp. 670-671.

4.11 Metering and Packaging

Extensive metering capabilities were provided in the cycloconverter power circuitry to facilitate its use in a university laboratory for both experimental and demonstrative purposes. Plate 8 in Appendix I shows the use of current transformers and potential transformers on both sides of the delta to wye power transformer. A dc average reading ammeter and zero-center voltmeter monitored each convertor output, and small resistors (made from parallel strands of No. 12 AWG resistance wire) provided a millivolt output for oscilloscope monitoring of the output current waveform. Similar small resistors were placed in series with each thyristor for oscilloscope observation of the thyristor current waveforms. Voltage attenuators (21:1 ratio) simplified oscilloscope monitoring of the thyristor voltages and the output voltage. All of the above items appear in full graphic form on the front panel power circuitry mimic engraving (Figure 4.2). Also visible in Figure 4.2 is the mimic of the circuitry for input operational amplifier 0/A7, whose schematic diagram appears in Plate 1 of Appendix I. The zero centre meter to the top right of the convertors is wired to a 12 point rotary switch (8 points in use) with various voltage multiplying resistors that permit a rapid check of six of the convertor dc power buses. The first two positions of the switch connect the meter to the bias offset voltage (0 to + 10 volts) supplied to the input of operational amplifier 0/A7, and to the output voltage of 0/A7. The other points monitor for the ± 10 volt regulated, + 11 volt unregulated, and ± 15 volt regulated power supplies.

An attempt was made to make the packaging of the drive as "industrial" as possible. That is, the unit was built in subassemblies which were interconnected by cables terminating on barrier strips or other non-soldering type connections. The firing circuit cards, phase back limit cards, crossover logic cards and auxiliary logic card were mounted in a card rack. The card rack was mounted on a rack plate which also had the ± 15 V power supplies and the operational amplifiers mounted on it in another assembly. Some of these features may be seen in the equipment photographs in Appendix II. An honest appraisal of the packaging is that it is good but, not as good as it could be. One person can strip a single converter to subassemblies in about two hours, but to put it back together takes several times that period. If the cycloconverter were to be built again, probably a pull-out drawer configuration would be favored rather than the present rack and panel configuration. Possibly greater use would be made of plug and socket connection between subassemblies rather than barrier strip and cable lug connections.

4.12 The Self-induced Component of Circulating Current

The basic circulating current problem was discussed in Section 2.3 with Figures 2.1 and 2.2 illustrating cycloconverter operation with circulating current when the control voltage was constant and the load circuit was open. A sawtooth-shaped, zero average, 360 Hz voltage difference forced a cusp-shaped circulating current to flow between the convertors. The amplitude of this circulating current was limited by a center-tapped circulating current reactor interposed between the convertors. The introduction of the reactor did limit the 360 Hz circulating current, but unfortunately the presence of the reactor itself produced a new component of circulating current at the cycloconverter output frequency.

This second component was termed the "self-induced" circulating current when it was described by B. R. Pelly.[20] The circulating current reactor induced the circulating current by attempting to maintain its flux linkages steady at their peak value, even though the load current drawn through the center-tap of the reactor was not steady. Maintenance of flux linkages required that any decrease in load current in one-half of the reactor be made up by an increase in current in the other half of the reactor. This increase was, in fact, the self-induced circulating current because ideally (ignoring the 360 Hz ripple frequency circulating current) there should be current flow in only on convertor, and hence in only one-half of the reactor at a time.

Starting with the assumption that the total MMF of the circulating current reactor does remain constant at whatever its largest value was in the past, expressions for the circulating current and the individual convertor currents are easily made in terms of the load current. The following development is similar to that by Pelly[21]

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[20] B. R. Pelly, Thyristor Phase - Controlled Convertors and Cycloconverters (New York: Wiley Interscience, 1971), pp. 134-142 and 156-161.

[21] Ibid.

and the current polarities are as shown in Figure 4.10.

$$\text{Total MMF} = i_p * \frac{n}{2} + i_n * \frac{n}{2} = \hat{i}_o * \frac{n}{2} \tag{4.1}$$

where i_p = the instantaneous current in the positive convertor

i_n = instantaneous current in the negative convertor

$\hat{i}_o$ = the peak load current

n = the total number of turns on the center-tapped reactor

Hence $\hat{i}_o = i_n + i_p$ (4.2)

Noting that the instantaneous load current i_o is the difference between the currents in the positive and negative convertors yields:

$$i_o = i_p - i_n \tag{4.3}$$

Then $i_p = i_o + i_n$ (4.4)

But $i_p = \hat{i}_o - i_n$ (4.5)

Then the positive convertor's current $i_p = \dfrac{\hat{i}_o + i_o}{2}$ (4.6)

And the negative convertor's current $i_n = \dfrac{\hat{i}_o - i_o}{2}$ (4.7)

The circulating current is the current in the negative convertor when the load current is positive, and vice versa.

Thus: $i_c = i_n$ when $i_o > 0$ (4.8)

$i_c = i_p$ when $i_o < 0$ (4.9)

where i_c = the instantaneous circulating current

The above results may now be used to explain the waveforms of Figure 4.10 which were obtained with the cycloconverter connected as shown in Figure 4.11. Trace 1 is the load voltage as seen at the center-tap of the circulating current reactor. As long as the MMF level of the circulating current reactor is constant or non-increasing, the center-tap voltage is essentially the instantaneous average of the terminal voltages of the two convertors. Moreover, changes in load current may occur instantly by using part of the reserve MMF of the reactor. That is, as long as the load current does not cause an increase in total MMF in the reactor, the cycloconverter output impedance is essentially zero (except for resistive drops). But if the load current is forcing an increase in the reactor MMF, the cycloconverter output impedance is then approximately L/4, where L is the total inductance of the two reactor halves in series connection. Note that in most cases the three-phase line inductance and the cycloconverter transformer leakage inductance are much smaller than that of one-half of the reactor (L/4).

The second and fourth traces in Figure 4.10 are the positive convertor's current i_p and the negative convertor's current i_n. The third trace is the load current i_o, and all three current traces are displayed at approximately 8 A/cm. Note that the positive and negative peaks of the load current i_o match reasonably with the peaks of the positive convertor's current i_p and the negative convertor's

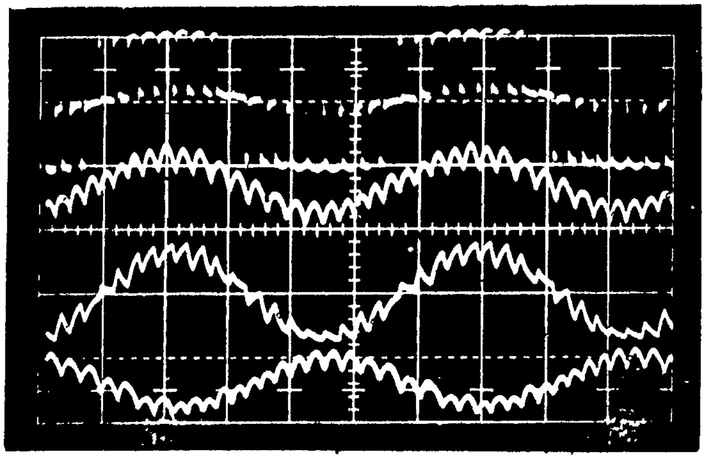

FIGURE 4.10 SELF-INDUCED CIRCULATING CURRENT CASE

Sweep = 5 ms/cm; V_c = sinewave at 30 Hz

Trace 1: V_o, at reactor center-tap; scale 200 V/cm

Trace 2: i_p, P converter; scale 8 A/cm

Trace 3: i_o, load current; scale 8 A/cm

Trace 4: i_n, N converter; scale 8 A/cm

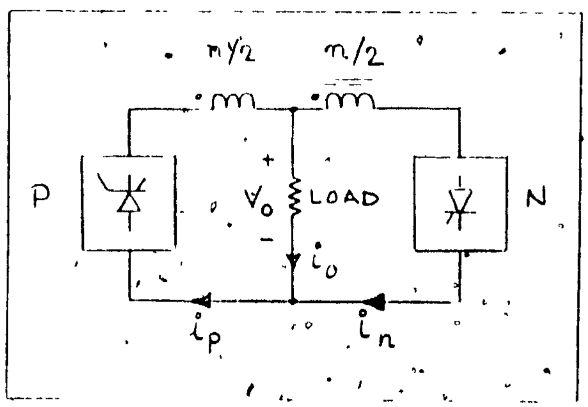

FIGURE 4.11. CONNECTION DIAGRAM FOR SELF-INDUCED CIRCULATING CURRENT CASE

current i_n. And as the amplitude of i_p falls below its peak value, the amplitude of i_n increases from zero[22] to maintain the MMF level in the circulating current reactor. The load current is sinusoidal except for a small ripple component, and hence it may be expressed as:

$$i_o = \hat{I}_o \sin \omega t \qquad (4.10)$$

Then the current in the positive convertor must be, by substitution in equation 4.6:

$$i_p = \frac{\hat{I}_o}{2} + \frac{\hat{I}_o}{2} \sin \omega t \qquad (4.11)$$

Similarly from equation 4.7:

$$i_n = \frac{\hat{I}_o}{2} - \frac{\hat{I}_o}{2} \sin \omega t \qquad (4.12)$$

Comparison of Equations 4.11 and 4.12 with the convertor waveforms in Traces 2 and 4 of Figure 4.10 yields a good agreement (neglecting the ripple components). This confirms that the constant MMF concept correctly describes the self-induced circulating current mechanism.

By using Equations 4.8, 4.9 and 4.10, the circulating current expressions are

$$i_c = \frac{\hat{I}_o}{2} - \frac{\hat{I}_o}{2} \sin \omega t \qquad \text{for } i_o > 0 \qquad (4.13)$$

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[22] Actually, the average firing angles of the two convertors were not quite complementary when the photograph for Figure 4.10 was taken. Hence i_p and i_n did not drop completely to zero.

and $$i_c = \frac{\hat{I}_o}{2} + \frac{\hat{I}_o}{2}\sin\omega t \qquad \text{for } i_o < 0 \qquad (4.14)$$

The average value of the circulating current is

$$\bar{i}_c = \left(\frac{\pi-2}{2\pi}\right)\hat{I}_o \qquad (4.15)$$

which is 0.571 times the average output load current: $\bar{I}_o = \frac{2}{\pi}\hat{I}_o$ (4.16)

From a different viewpoint, if the self induced circulating current were not present, the average convertor current would be reduced from $\frac{I_o}{2}$ to $\frac{I_o}{\pi}$, neglecting the circulating ripple and averaging over a full cycle of output load current.

In summary, interposing the circulating current reactor between the convertors did suppress the 360 Hz circulating current ripple. But the presence of the reactor caused a self-induced circulating current to flow, the amplitude of which depended directly upon the peak amplitude of the load current. This puts a substantial wattless load upon the convertors. Hence the pure circulating current mode of operation is a luxury usually permitted only when it is absolutely necessary to have a very linear relationship between control voltage and cycloconverter output voltage on an open loop basis. B.R. Pelly proposed a compromise between pure circulating current operation and completely circulating-current-free operation that involved using a smaller circulating current reactor combined with a controlled firing pulse overlap period between the two convertors.[23]

[23] *Ibid.*, pp. 190-198.

The controlled overlap approach appeared to yield superior waveforms without increasing the average convertor current by a significant amount. The crossover distortion with LCR loads was substantially lower for the controlled overlap arrangement than with the circulating current free arrangement. Section 3 14 of this thesis described the AEI cycloconverter which could be operated either without circulating current or else with circulating current and a controlled firing pulse overlap.

4.13 Summary and Conclusions

The circuitry of a successful three-phase to single-phase cycloconverter has been described. Each convertor was supplied from its own delta-wye transformer so that the steady-state circulating current ripple fundamental was at 360 Hz rather than 180 Hz. An independent gating circuit set was provided with each convertor. The biased cosine technique was chosen for phase control so that the input to output transfer function was linear as long as the output current was continuous. Phase forward and phase back limit pulses were added to the cosine waves to ensure that a firing pulse always occured somewhere between the limits no matter what extreme value the control voltage amplitude might have. Double pulsing with short firing pulses was used. However it was possible to use double pulsing with longer pulses to permit smoother operation. The Alpha blanking card suppressed any firing pulses which might have occurred in the forbidden range $180^\circ < \alpha < 360^\circ$ if the rate of change of control voltage had been rapid. An easily adjusted spillover current limit was provided in each convertor. Fault current protection was provided by fuses, but references were made to more complete protection schemes used in industrial drives. The method of suppression of voltage transients due to commutation was discussed and references were made to detailed articles on the topic. The metering facilities and the packaging of the convertors were discussed. The conclusion was that the metering was good while packaging was only adequate. A detailed explanation of the self-induced circulating current was made which followed that made by B.R. Pelly. This component of circulating current was shown to add a substantial current load to the convertors. However references were made to a compromise solution which permitted circulating current to flow only when the load current was below a small, preset value. Chapter V, now to follow, will describe a scheme to completely eliminate the circulating current.

CHAPTER V

ELIMINATION OF THE CYCLOCONVERTOR CIRCULATING CURRENT

5.1 Introduction

The previous chapter described a successful cycloconvertor that operated with circulating current between its anti-parallel convertors. However the modern approach to cycloconvertor design starting with the VSCF system cycloconvertors described by Chirgwin, Stratten, and Toth[1,2] (see Section 3.2 of this thesis) has been to completely eliminate the circulating current. This has been done with current detection and logic circuitry that permits only the alternate operation of the pairs of anti-parallel convertors making up a polyphase output cycloconvertor. The alternate conduction rather than simultaneous conduction of the convertors eliminates the circulating current by preventing the establishment of a completed series path for circulating current through both convertors at once. Thus, the bulky circulating-current limiting reactors may be discarded, thereby eliminating the large additional wattless load imposed by the induced circulating current in them. In addition, the requirement for matching of the anti-parallel convertors' average (dc)

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[1] K.M. Chirgwin and C.J. Stratton, "Variable-Speed, Constant-Frequency Generator System for Aircraft", AIEE Transactions, Pt. II (Applications and Industry) Vol. 78, November 1959, pp. 304-310.

[2] K.M. Chirgwin, L.J. Stratton, and J.R. Toth, "Precise Frequency Power Generation from an Unregulated Shaft", AIEE Transactions, Pt. II (Applications and Industry), Vol. 79, 1960 (January 1961 section), pp. 442-449.

output voltage need not be as strict because the cycloconvertor load circuit path would probably be more tolerant of a small dc offset voltage than would the circulating current circuit path.

As in Chapter IV, the development of the text and illustrations in this chapter will follow closely an IGA conference paper written by T.M. Hamblin and Dr. T.H. Barton [3]

5.2 Current Zero Detection

Successful circulating-current free operation requires that the elimination logic receive reliable and rapid indication of the zero load current condition in each anti-parallel convertor pair. Several articles (see Chapter III of this thesis) have described the use of ac current transformers on the input side[4,5] of the cycloconvertor, or dc current transformers on the output side[6] to isolate the detection circuitry from the power circuitry. The isolated current zero detection circuitry must then correctly respond to a wide range of current amplitudes varying from full output down

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[3] T.M. Hamblin and T.H. Barton, "Cycloconvertor Control Circuits", IEEE Conference Record of the 1970 Fifth Annual Meeting of the IEEE Industry and General Applications Group, 70-C5(GA, Chicago, October 1970, pp. 559-571.

[4] D.L. Duff and A. Ludbrook, "Reversing Thyristor Armature Dual Convertor with Logic Crossover Control", IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June 1965, pp. 216-222.

[5] Frank Wesselak, "Thyrsitor Convertors with Natural Commutation", Siemens Review, No. 12, December 1965, pp. 405-410.

to the holding current of the thyristors. Duff and Ludbrook (see Section 3.8 of this thesis) approached the problem of correctly detecting the minimum current by rectifying the ac component of the dc output wave of their single-phase output cycloconvertor type of dc armature supply. This extra signal was combined with a signal derived from ac current transformers on the input to provide a reliable current zero detection system.

The thyristor voltage monitoring technique, now to be described, relies upon voltage signals alone and hence avoids the difficulties with wide ranging current amplitudes common to other schemes that use current transformers. The absolute value of the voltage across each of the six thyristors in a convertor is continuously monitored. If the voltage across each and every thyristor has been 10 volts or greater for not less than a certain timing interval (adjustable from 50 to 400 μs) the shaped output of the current zero detection logic will change from low to high signalling that the bridge current is zero. If the voltage across one or more of the thyristors becomes less than 10 volts, the shaped logic output will quickly revert to low as the timing capacitor is discharged to the zero bus by the clamping action of NOR1 in the current zero timing circuit of Figure 5.1. This low voltage condition will occur whenever one or more thyristors is conducting, or for a short period of time

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[6] R.A. Hamilton and G.R. Lezan, "Thyristor Adjustable Frequency Power Supplies for Hot Strip Mill Run-Out Tables", IEEE Transactions on Industry and General Applications, Vol. IGA-2, No. 2, March/April 1967, pp. 168-175.

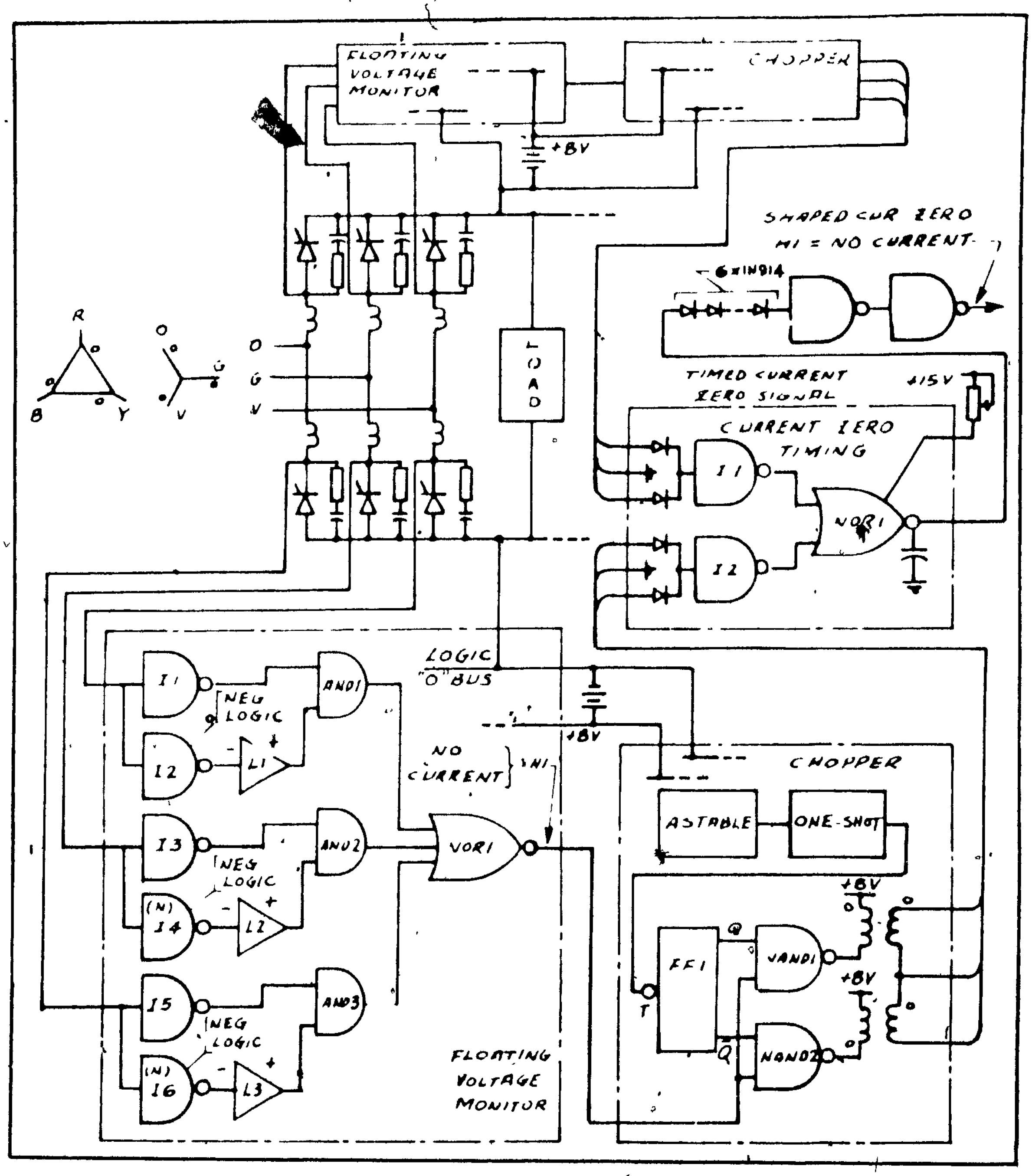

FIGURE 5.1. CURRENT ZERO DETECTOR FOR ONE CONVERTOR

whenever the voltage across a blocked (non-conducting) thyristor crosses zero. That is, the voltage monitoring scheme will give some false indications of current flow during actual current zero conditions (but not vice versa). These false indications are not a problem because the circulating current elimination logic depends upon the true indication of the current zero condition for a period only long enough to operate a logic flip-flop.

Two floating voltage monitor cards in each convertor (Figure 5.1, and Plate 9 in Appendix I) check the thyristor voltages with respect to the positive and negative buses of the convertor. Since both positive and negative thyristor voltages must be monitored, PNP invertors I2, I4 and I6 (Q2, Q5, Q8 in Plate 9) are combined with negative to positive logic level changers L1, L2, and L3 (Q3, Q6 and Q9 in Plate 9). The remainder of the circuit uses conventional positive logic circuits with NPN transistors.

A chopper card with chopper and isolating pulse transformer couples each current zero logic signal from its floating voltage monitoring card to the current zero timing circuits. This scheme, using a toggled flip-flop to feed NAND gates that have a common push-pull pulse transformer load, was developed in 1968 and has worked reliably since that time. Since then however, a number of manufacturers have introduced inexpensive photo-electric digital isolators packages (using GaAs light emitting diodes illuminating photo-transistors or photo-diodes) that would replace the chopper very nicely. In fact, they are inexpensive enough so that one isolator (plus attenuator and four diode bridge) could be used to monitor each thyristor voltage. Isolated (floating) power supplies would not be necessary and the combining logic to obtain one current zero signal could be done with the photo-transistors or photo-diodes.

The chopped logic signals are then rectified at the secondaries of the pulse transformers (Plate 11, Appendix I) before being combined in such a way that an integrating (timed) logical AND is performed on them. Both top and bottom of the bridge must be monitored because the RC snubbers circuits provide alternate paths for thyristor current flow so that the top and bottom of the bridge may not always cease conduction simultaneously. The chopping-isolating operation is fail-safe for the case of floating power supply failure because thyristor current flow is indicated by the absence of a chopped logic signal at the pulse transformer secondary.

The output of the current zero shaping circuit (Figure 5.1 and Plate 12, Appendix I) remains low until the output of the current zero timing ramp reaches the approximately three volt switching point set by the six diodes in series with the input to transistor Q4. The slope of the timing ramp is set by rheostat R18 (Plate 12), fixed resistor R9 (Plate 11) and capacitor C1 (Plate 11).

Figure 5.2 clearly demonstrates the speed of the thyristor voltage monitoring technique of current zero detection. Even with the timing set for a 100 μs integration time, the shaped current zero output (Trace 2) signalled the end of thyristor conduction before the load current (Trace 3) had stopped ringing through the RC snubbers connected across the thyristors. The actual moment at which the thyristors stopped conducting is pinpointed by the start of timing in Trace 1 which coincides with the inflection in the output voltage waveform (Trace 4). Figure 5.2 also shows that the start of thyristor current flow was detected rapidly as well.

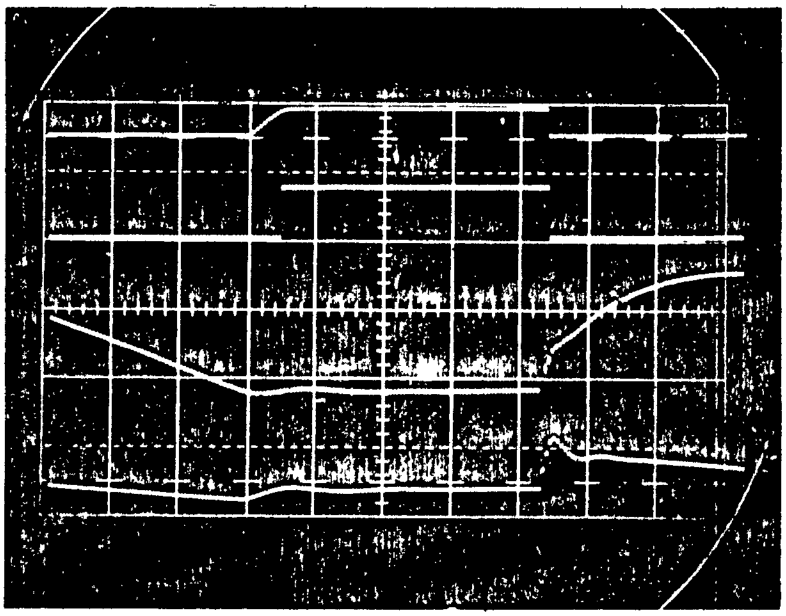

FIGURE 5.2. CURRENT ZERO DETECTION. $V_c = 1.6$ V, HENCE $\alpha = 99^o$, RL LOAD;

Sweep = 200 μ sec/cm.

Trace 1: Timed current zero signal; scale = 10 V/cm.

Trace 2: Shaped current zero signal; scale = 20 V/cm.

Trace 3: Convertor load current; scale = 2A/cm.

Trace 4: Convertor output voltage; scale = 210 V/cm.

Because the anti-parallel convertors are mounted in separate cabinets, each convertor has its own complete current zero detection system. The circulating current elimination logic requires that the current in both convertors be simultaneously zero, before switching over the convertors, hence an AND circuit in the master convertor is used to combine the two signals yielding one total current zero signal. If the anti-parallel convertors had been permanently connected together, then the AND operation between convertors could have been performed by using a single current zero detector for the two convertors. Two voltage monitoring cards, each one covering six thyristors connected to a bus, would have made up the detector. Note that in either case, the voltage monitoring cards must be connected to check the thyristor voltages alone That is, they should not be connected across the series combination of a thyristor and its $\frac{dv}{dt}$ suppression reactor if the response time of the detector is to be at a minimum.

5.3 Circulating Current Elimination Logic for Unity and Lagging PF Loads

As stated in Section 5.1 of this thesis, the circulating current elimination logic prevents circulating current between anti-parallel convertors by never permitting them to be in simultaneous conduction. To prevent simultaneous conduction, circulating current elimination logic suitable for resistive and lagging pf loads depends upon the logic AND of the following three conditions to set the correct moment to release thyristor firing pulses to the previously blocked (non-conducting) convertor :

1. The control voltage polarity has changed to that which would now operate the previously nonconducting convertor as a rectifier (that is, $0^\circ < \alpha < 90^\circ$)

2. The load current is zero, or less restrictively, all the thyristors in the anti-parallel pair are nonconducting.

3. No gate pulses are occuring at that moment in the previously conducting convertor.

The logic AND of these conditions is used to trigger an RS type flip-flop, the outputs of which drive gating circuits that (1) immediately stop further firing pulses to the previously conducting but presently nonconducting convertor, and (2) after a short delay permit the normal transmission of firing pulses to the on-coming convertor.

This particular scheme is fundamentally suited to resistive and lagging loads controlled on either an open loop or closed loop basis because the zero crossing of the control voltage, which is essentially in phase with the fundamental component of the cycloconvertor load voltage, will be detected either in advance of or at the same time as the load current zero. However with leading pf loads, the load current will go to zero first causing an undesirable gap in the load current until the control voltage polarity changes to satisfy the logic AND gate in the circulating current elimination circuitry.

Figure 5.3 is a block diagram of the main section of the crossover logic card (or circulating current elimination logic card) used for unity and lagging pf loads. Invertor I1 supplies the complement of the control voltage polarity signal to AND1. AND1 plus AND2 check the three conditions for convertor current "crossover before gating the flip-flop NOR1, NOR2 The outputs of the AND gates cannot be simultaneously true (high) because of the complementing action of I1 Pulses from single-shot multivibrators OS1 and OS2 define the "double blanking" period (set to 50 μs) at crossover during which time thyristor firing pulses in both bridges are blanked (that is, suppressed) The (low) outputs of gates NOR3 and NOR4 blank the master and the slave bridges respectively. Small capacitor delays were added to NOR3 and NOR4 to suppress timing race spikes that briefly unblanked the on-coming convertor as the flip-flop changed states. Plate 13 in Appendix I shows the interconnection detail of the master convertor to slave convertor logic signal cable plus certain jumpers required in the master convertor. The "extra" logic gates shown on the crossover card in Plate 13 (but not in Figure 5.3) will be described in Section 5.10. The use of the artificial current limit circuit, (on the auxiliary logic card, Plates 12 and 13) will be described in a later section of this chapter. The voltage crossover detector (Plates 12, 13 and Figure 5.3) is a simple regenerative level detector with a (zeroing) input bias signal and adjustable hysteresis which is normally set to a width of 0.1 V.

Figure 5.4 shows the output waveforms of the cycloconvertor when feeding a single-phase induction motor at 45 Hz. As is normal for an induction motor, the current (Trace 3) lags the motor terminal voltage (Trace 2), which is essentially in phase with the cycloconvertor reference voltage (Trace 1). Trace 4 is the output of the firing pulse detector NOR in the master convertor (Plates 4 and 13, Appendix I). Examining the waveforms confirms that the logic crossover did indeed occur when the three necessary logic conditions previously mentioned were simultaneously satisfied.

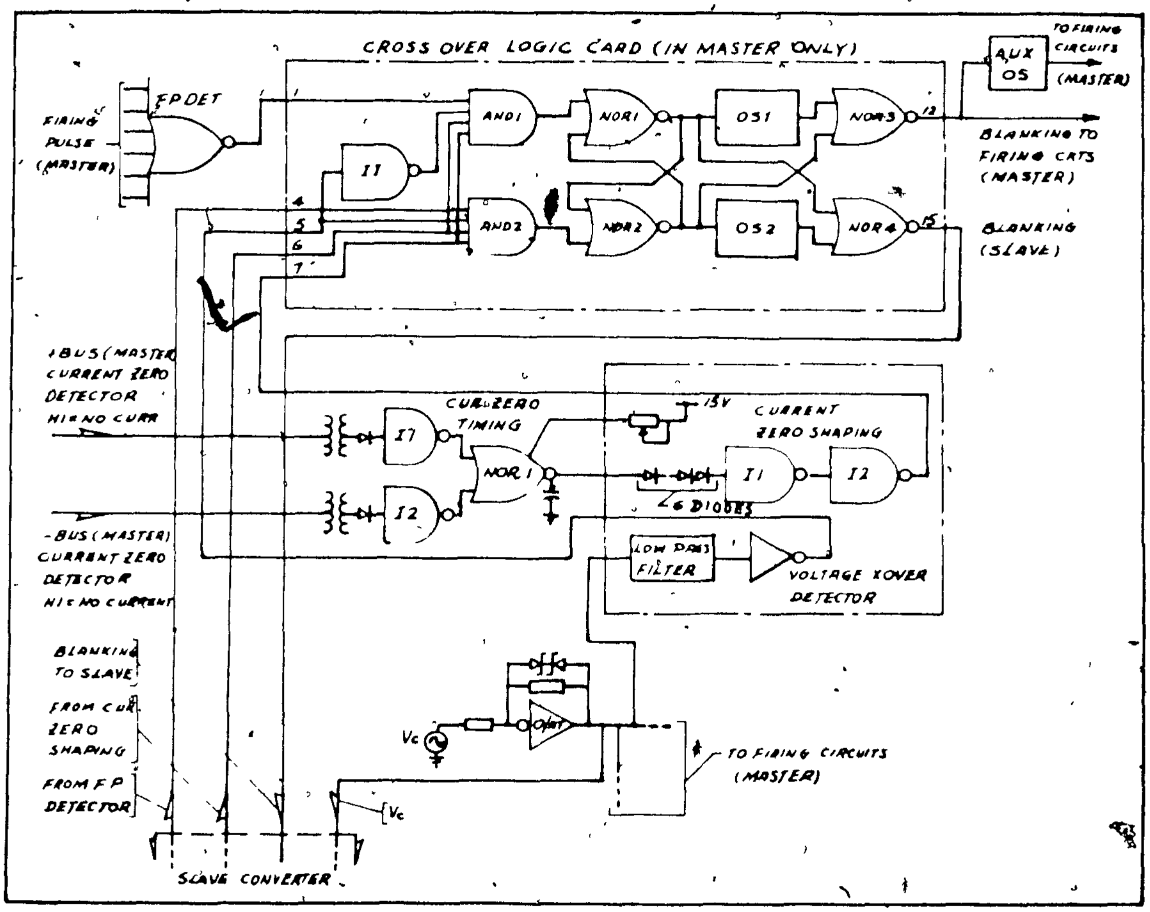

FIGURE 5 3 CROSSOVER LOGIC CARD FOR RESISTIVE AND LAGGING LOADS

This type of crossover logic is well suited to induction motor control because the current always lags the motor voltage, even when the motor is rotated faster than its synchronous speed by the regenerative action of its mechanical load. Figure 5.5 is a double exposure showing the current lagging the motor voltage when the four-pole induction machine was motoring at 820 rpm, and when it was being driven at 930 rpm with a 30 Hz cycloconvertor output frequency in both instances.

5.4 Firing Pulse Delay and Double Pulsing OR Card

The absence of firing pulses in the off-going convertor is one of the conditions that must be satisifed before triggering the interlocking flip-flop on the crossover logic card. However due to various circuit delays, there is a period of approximately 1.5 µs between the start of the flip-flop triggering action and the time at which the firing pulse blanking becomes effective in the off-going convertor. If by coincidence a firing pulse has started in the supposedly off-going convertor during this period, then a segment of it up to a maximum of 1.5 µs in length will be transmitted through the double pulsing OR gates to two thyristors. It is possible that this stray pulse will successfully gate one or both of these thyristors in the supposedly blocked and off-going bridge. For the cycloconvertor connections of Figure 1.1a and 1.1b (but without the circulating current limit reactors X) a line-to-line circulating current fault then occurs when the first (auxiliary) firing pulses are applied in the on-coming convertor at the end of the 50 µs double blanking period if one (or both) of the thyristors in the supposedly off-going convertor is still conducting. With separate three phase transformers as in Figure 4.1 (but less the reactor) the fault cannot occur unless both of the thyristors are still conducting. When simulating the cycloconvertor connection

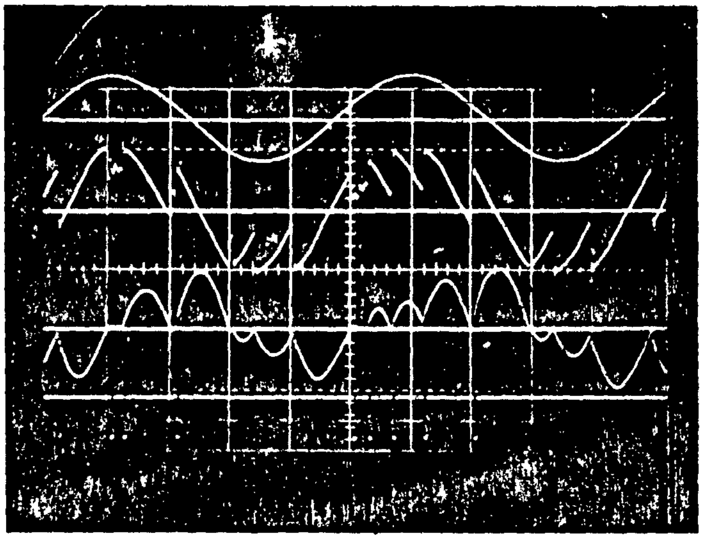

FIGURE 5 4 SINGLE-PHASE INDUCTION MOTOR LOAD

Sweep 5 ms/cm

Trace 1. V_c 5 0 V peak, 40 Hz sinewave, scale = 10 V/cm.

Trace 2. Load voltage, scale 220 V/cm

Trace 3: Load current, scale 20 A/cm

Trace 4: Firing pulse detector NOR (Master), scale 20 V/cm

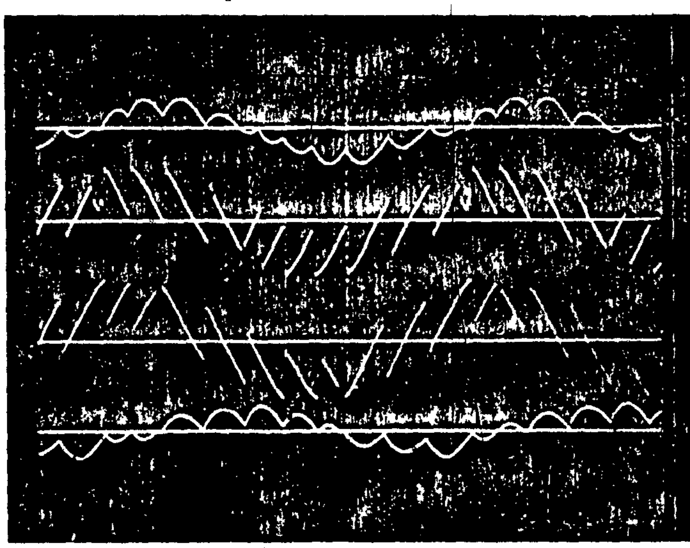

FIGURE 5 5 SINGLE PHASE INDUCTION MACHINE (LAGGING pf) AT 30 Hz; N syn = 900 RPM; V_c = 5 0 V PEAK.

Sweep: 180° = 3 cm.

Trace 1: Load current (30° lagging), 820 rpm, scale 50 A/cm.

Trace 2: Load voltage, 820 rpm; scale 210 V/cm

Trace 3: Load voltage, 930 rpm; scale 210 V/cm.

Trace 4: Load current (135° lagging), 930 rpm; scale 50 A/cm.

of Figure 1.1b (less reactors X) by tying the three-phase transformer star points together in the connection of Figure 4.1 (less the reactors), circulating current faults were audible every few seconds as soon as the double blanking period was cut to less than 100 µs.

The stray pulses causing the faults were eliminated by applying a 10 µs delay to each firing pulse after it had passed the firing pulse detector NOR. That is, if at any instant the firing pulse detector NOR indicated that no firing pulses were occurring, then a firing pulse could reach a thyristor no sooner than 10 µs after that instant. This 10 µs interval provides sufficient time for the crossover logic flip-flop to operate and the firing pulse blanking to become effective in suppressing any firing pulses. Figure 5.6 and Plate 4, Appendix I show how the double pulsing OR matrix card was successfully modified. RC filters combined with regenerative switches operating at an 8.0 volt threshold provided the required delays. A silicon controlled switch (SCS) could be used to replace each 2N3702, 2N3704 combination if desired. The switches had a very consistent threshold level combined with a rapid regenerative break-over to give a fast rising leading edge on the delayed firing pulses.[7]

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[7] The writer gratefully acknowledges the assistance of Mr. P.A. Morrison of McGill University who first observed the fault phenomenon, devised the cure with the writer, and then built the delay circuits.

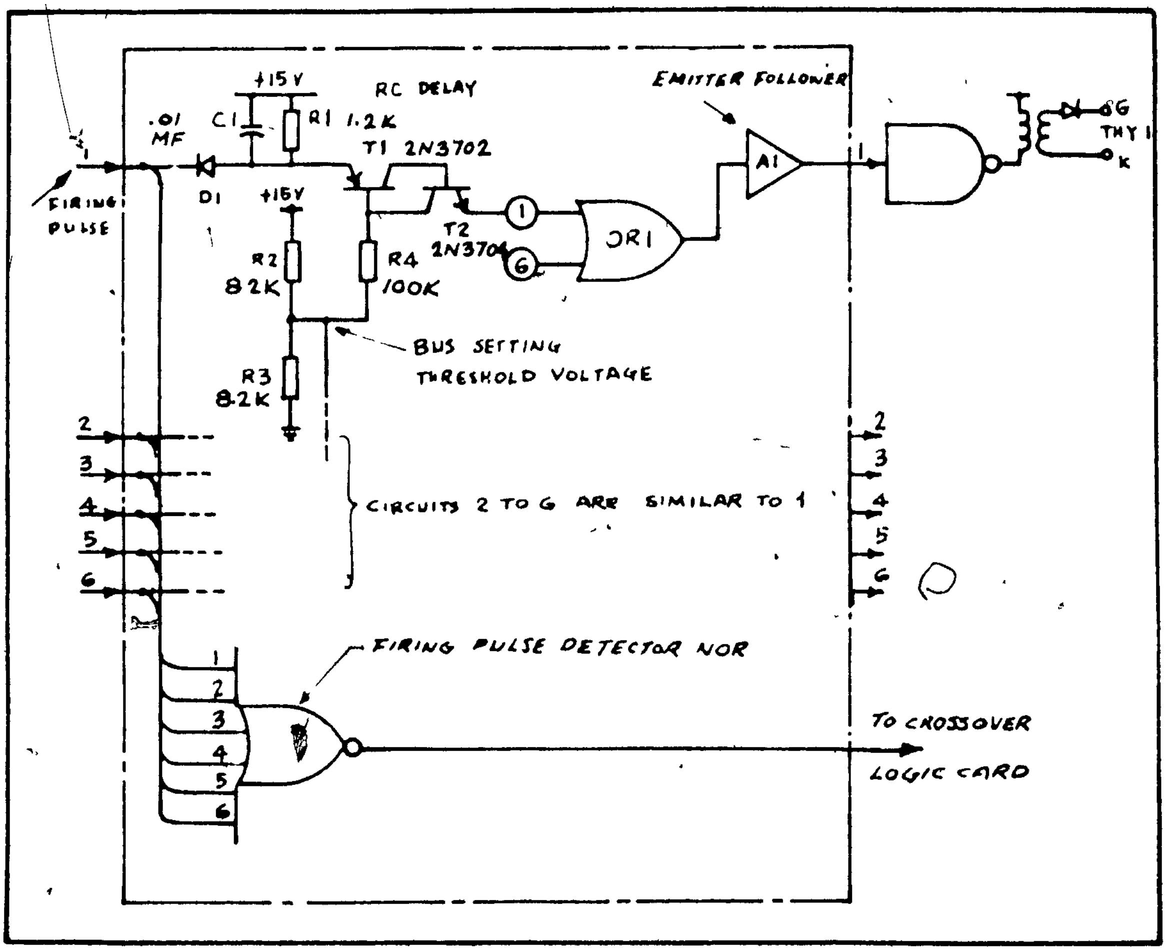

FIGURE 5.6. FIRING PULSE DELAY-DIODE OR CARD.

5.5 Auxiliary Pulsing

The crossover of load current from one anti-parallel convertor to the other may occur only after the detection of current zero. Then after a short double blanking period during which no thyristor firing pulses are permitted in either bridge, the firing circuits in the on-coming bridge are unblanked. However the first normal firing pulse will not necessarily occur immediately after the unblanking of the on-coming convertor, so that relatively large gaps may appear in the cycloconvertor output voltage and current waveforms thereby limiting the maximum usable output frequency.

To minimize such gaps in the waveforms, each firing circuit card (Figure 4.8 and Plate 2, Appendix I) is provided with a "memory" one-shot multivibrator OS2 that produces a pulse 55° wide (relative to 60 Hz) when triggered by the fall of the original firing pulse from OS1 on the card. The end of the double blanking period triggers an auxiliary one-shot in the on-coming convertor (AUX OS, Figure 5.3) that generates a 200 μs pulse which is sent to the auxiliary pulse input on each firing pulse card in the convertor. The card that has produced a firing pulse (and hence a memory pulse) within the last 55° will then produce a 200 μs firing pulse at the output of AND2 (Figure 4.8). This pulse is handled in the usual manner by the double pulsing OR matrix to produce a second pulse for the other half of the bridge convertor. The oscilloscope photographs for Figure 5.4 (with auxiliary pulsing) and Figure 5.7 (without) were both taken with 5.0 volts peak, 40 Hz sinusoidal cycloconvertor control voltage and the same induction motor load to show how the auxiliary pulsing improved the output waveform. In some cases more than one firing card will have produced a firing pulse within the last 55° (at 60 Hz), but no shoot-through faults have been traced to this cause. Note that AND3 in Figure 4.8 acts as an alpha blanking gate to suppress any auxiliary firing pulses that might appear in the forbidden interval $180^{\circ} < \alpha < 360^{\circ}$.

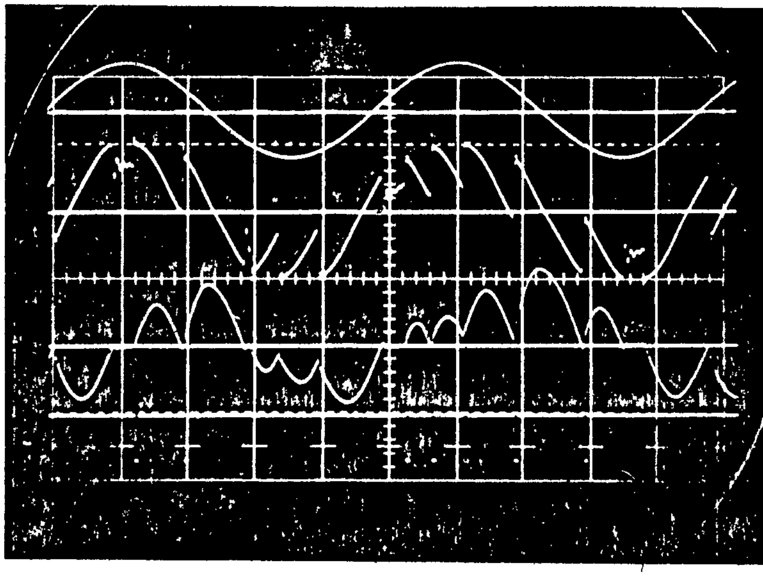

FIGURE 5.7. SINGLE PHASE INDUCTION MOTOR (WITHOUT AUXILIARY PULSING) .

Sweep: 5 msec/cm.

Trace 1: V = 5.0 V peak, 40 Hz sinewave; scale 5 V/cm.

Trace 2: Load voltage; scale 220 V/cm.

Trace 3: Load current; scale 20 A/cm.

Trace 4: Firing pulse detector (NOR), master bridge; scale 20 V/cm.

5.6 A Reversing DC Armature Drive

Although three-phase to single-phase cycloconvertors may be used for single-phase induction motor drives, their most common application, as outlined in Chapter III, has been for dc motor armature supplies. Induction motor and synchronous motor cycloconvertor drives have consistently had polyphase outputs so that the motors could be controlled at any speed and in either direction (unlike single-phase motors). Ward-Leonard systems have been almost completely displaced by thyristor drives in new variable speed drive installations because of the higher efficiency, reliability, and lower weight of the latter. However there are certain problems that must be faced when using a thyristor supply for a dc motor armature. These (three) problems will now be outlined and references will be made to articles which discuss them in detail.

The first problem is the reduction of dc motor armature commutation ability caused by the large harmonic ripple superimposed on the dc average value of armature current because of the high harmonic content of the convertor output voltage. The motor torque is related to the average value of the current, but the higher rms value of the current determines the copper and eddy current losses, while the still higher peak value of current limits the motor armature commutation ability. The phase shift and distortion of the interpole flux by the eddy currents driven by the convertor voltage harmonics may drastically reduce the black-band[8,9] range of sparkless commutation. However C.E. Robinson pointed out that lamination of both the interpole and the motor frame would decrease the phase shift significantly.[10] In addition

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[8] R.M. Dunaiski, "The Effect of Rectifier Power Supply on Large D-C Motors", AIEE Transactions, Pt. III (Power Apparatus and Systems), Vol. 79, June 1960, pp. 253-258.

[9] N. Kaufman, "An Application Guide for the Use of D-C Motors on Rectified Power", IEEE Transactions on Power Apparatus and Systems, Vol. 84, October 1964, pp. 1006-1009.

[10] C.E. Robinson, "Redesign of DC Motors for Applications with Thyristor Power Supplies", IEEE Transactions on Industry and General Applications, Vol. IGA-4, No. 5, September/October 1968, pp. 508-514.

he proposed that the best 4-pole motors for rectified power should tend to larger diameter armatures, shorter core lengths, and armature windings requiring more commutator bass and fewer turns per coil.[11] In other words, dc motor design may be readjusted to provide adequate operation under convertor power.

The second problem is brought about by the characteristic soaring of the convertor output voltage in a positive direction with decreasing current amplitude once it has fallen low enough to become discontinuous. As long as the convertor output current is continuous, the bias-shift method of phase-control provides a linear relationship (see Equation 2.1) between input control voltage V_c and the average output voltage V_d of the convertor (neglecting commutation and resistive drops). However, decreasing the current so that it becomes discontinuous causes an upward swing in the convertor regulation curve (taken for any constant α), and this change in the regulation characteristic presents two difficulties:

(1) The (non-linear) voltage gain of the convertor operating with continuous current is drastically less than the (linear) gain of the convertor operating with continuous current. This decrease in gain adversely affects the drive system response to impact loads striking when the convertor is in the discontinuous current region. A saturable reactor may be used in the armature circuit

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[11] Ibid., p. 514.

to decrease the size of the discontinuous region,[12] or various closed loop techniques[13] may be applied to minimize the effect of this gain change.

(2) If the motor current is switched from one anti-parallel convertor operating as a rectifier with discontinuous current to the other (previously blocked) convertor ready to act as an invertor while keeping the control voltage constant, there will be a disasterously large initial overshoot of current through the invertor before its current limit circuit has a chance to function. This over current appears because the motor armature voltage will be initially nearly equal to the rectifying convertor voltage running with discontinuous current, while the inverting convertor will come on with continuous current and hence, a lower output voltage. The surge current is limited only by the (low) impedance of the armature until the motor speed increases to compensate or the current limit circuit takes hold. A similar situation would exist when switching from inversion to rectification with the rectifying convertor starting with continuous current flow and an output voltage higher than the initial motor armature voltage. As

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[12] K.G. Black, "The Effect of Rectifier Discontinuous Current on Motor Performance", IEEE Transactions on Applications and Industry, Vol. 83, November 1964, pp. 377-382.

[13] E.A. Wilkes and P.J. Wirtz, "Frequency Response Compensation of D-C Drives", IEEE Conference Record of the 1969 Fourth Annual Meeting of the IEEE Industry and General Applications Group, 69 C5-IGA, Detroit, Michigan, October 1969, pp. 117-123.

described on pages 45 and 46 of Section 3.8 and page 57 of Section 3.10, the oncoming convertor should not be unblanked unless it has been phased back beyond the point of zero current. This point depends upon the level of armature voltage at that time, so that some manufacturers use a voltage matching scheme which senses either the armature voltage or the tachometer voltage.[14, 15] Duff and Ludbrook of Canadian Westinghouse preferred not to use voltage matching but to temporarily phase back the oncoming convertor well beyond the zero current point by injecting a signal into the current regulator.[16] When used as an armature supply, the cycloconverter described herein has a permanent deadband between the convertors provided by phasing back the individual gating circuits with fixed bias signals. This permanent deadband prevents armature current surges just as did the temporary deadband used by Duff and Ludbrook.

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[14] F. Wesselak, "Thyristor Convertors with Natural Commutation," Siemens Review, December 1965, No. 12, pp. 407-408.

[15] K. Lidberg, "New Series of Thyristor Convertors for Industrial Motor Drives, 20 - 500 KW," ASEA Journal, Vol. 42, No. 5, 1969, pp. 63-68.

[16] D.L. Duff and A. Ludbrook, "Reversing Thyristor Armature Dual Convertor with Logic Crossover Control," IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June 1965, pp. 219-220.

The final problem for the thyristor drive designer is deciding on how to model the thyristor drive itself for calculation or simulation of drive performance. Wilkes and Wirtz suggested that the use of a ficticious output impedance in the convertor model would aid in the frequency response calculations when the convertor entered the discontinuous current mode.[17] But a second complication in the modelling process is the sampling action of the phase-controlled thyristor gating circuits which introduce a varying transport lag into the system. Parrish and McVey viewed the system as a sampler followed by a partial zero-order hold device.[18] Then, assuming that the overall control system was low pass with an open loop cross-over frequency well below the sampling frequency, the convertor model could be reduced to a transport delay equal to half the average conduction period of each thyristor. Thus for six-pulse, 60 Hz operation with continuous conduction, the convertor model would be a transport delay of 1/720th second. Generally this simple model should be sufficient, but R.D. Jackson has suggested a describing function approach to explain sustained current oscillations that may occur when only one convertor is used in a non-reversing armature drive application.[19] Also,

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[17] E.A. Wilkes and P.J. Wirtz, op. cit.

[18] E.A Parrish, Jr. and E.S. McVey, "A Theoretical Model for Single-Phase Silicon-Controlled Rectifier Systems", IEEE Transactions on Automatics Control, Vol. AC-12, No. 5, October 1967, pp. 577-579.

[19] R.D. Jackson, "Oscillations in Single Convertor Drives", Proceedings of the IEE, Vol. 116, No. 4, April 1969, pp. 633-637.

F. Fallside and A.R. Farmer[20] have developed describing function techniques to predict subharmonic instabilities (1/2, 1/3, etc. of 360 Hz) when the overall open loop bandwidth is not low in comparison to the sampling frequency (360 Hz). Recently G. De and A.K. Mandal published a paper on incremental describing functions for the analysis of such subharmonic oscillation.[21] The introductory sections of their paper provides a good review of the work done by others in this field (including Fallside and Farmer). De and Mandal proposed that at the subharmonic frequencies the converter could be modelled as an asymmetrical saturation type nonlinearity in series with a linear block whose factors depend upon the number of pulses of the converter and the order of the subharmonic.

The dc drive to be described herein uses the circulating-current-free cycloconverter detailed in Chapter IV and this chapter as its power amplifier. V. Stefanovic of McGill University has applied the drive as part of a high power servo-analyzer in his research on the stability of an induction motor with a variable frequency supply. The speed and current regulators of the drive were part of the experimental apparatus used by G. Joos of McGill University in his research on thyristor drive modelling, simulation, and compensation. Because the work of designing and tuning the regulators in the drive was performed by G. Joos, the

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[20] F. Fallside and A.R. Farmer, "Ripple Instability in Closed Loop Systems with Thyristor Amplifiers," Proceedings of the IEE, Vol. 114, No. 1, January 1967, pp. 139-152.

[21] G. De and A.K. Mandal, "Incremental Describing Function Analysis of Subharmonic Oscillations in Control Systems with Thyristor Converters," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-20, No. 4, November 1973, pp. 229-235.

following discussion will avoid that topic. Instead it will concentrate further on the effect of discontinuous current upon the converters' dc transfer function and on a comparison of methods to prevent armature current surge following crossover.

5.7 Three Methods of Preventing Armature Current Surge after Crossover

Figure 3.1 on Page 46 of this thesis showed that the output voltage of a converter moves away from the straight line transfer function when the converter current becomes discontinuous. The converter current will cease completely when the armature voltage exactly matches the peak converter voltage. This peak voltage is a function of the control voltage to the converter. Using this information, the boundaries of the dc transfer function of a single converter are shown in Figure 5.8. The abscissa and ordinate scales were chosen to match the transfer function for which the converter was designed. That is, a control signal of +10.0 V should phase the converter full-forward ($\alpha = 0^{\circ}$) yielding 1.0 per unit output neglecting commutation and resistive losses. Equation (2.1) on Page 12 herein stated that the average output voltage V_d of a six pulse bridge converter with continuous current is

$$V_d = (\sqrt{2}\,E)\,\frac{6}{\pi}\sin\left(\frac{\pi}{6}\right)\cos\alpha \tag{5.1}$$

or

$$V_d = \frac{\sqrt{2}\,E\cos\alpha}{1.045} \tag{5.2}$$

where $\sqrt{2}E$ = the peak value of instantaneous output voltage of the converter. (This is equal to the peak line-to-line voltage for a six pulse bridge converter).

Consideration of the output waveforms for peak rectification (not shown herein) will yield a peak output voltage V_p relation

$$V_p = \sqrt{2}E \qquad \text{for } 0^{\circ} \leq \alpha \leq 30^{\circ} \qquad (5.3)$$

and

$$V_p = \sqrt{2}E \cos(\alpha - 30^{\circ}) \text{ for} \qquad \text{for } 30^{\circ} \leq \alpha \leq 180^{\circ} \qquad (5.4)$$

The phase control circuitry uses the biased cosine wave technique so that the firing angle is

$$\alpha = \cos^{-1}\left[\frac{V_c}{10.0}\right] \qquad (5.5)$$

Hence the average converter output voltage V_d defined by Equation (5.2) is linear with respect to the control voltage V_c between the phase forward limit (7) and the phase back limit (6). The phase back limit at $\alpha = 165^{\circ}$ is necessary to ensure sufficient margin to complete commutation when the converter is inverting. The same phase back limit also puts an inflection, (4), in the peak voltage locus. Phasing the converter forward increases the peak voltage until ($\alpha = 30^{\circ}$) is reached. Provided firing pulses longer than 30° are used, the peak output voltage then remains constant until $\alpha = 0^{\circ}$. Further increases in the control voltage V_c do not change the firing angle after the phase forward pulse limit at 0° has been reached. Hence the peak voltage inflects the point (1) and then remains constant for increasing values of V_c.

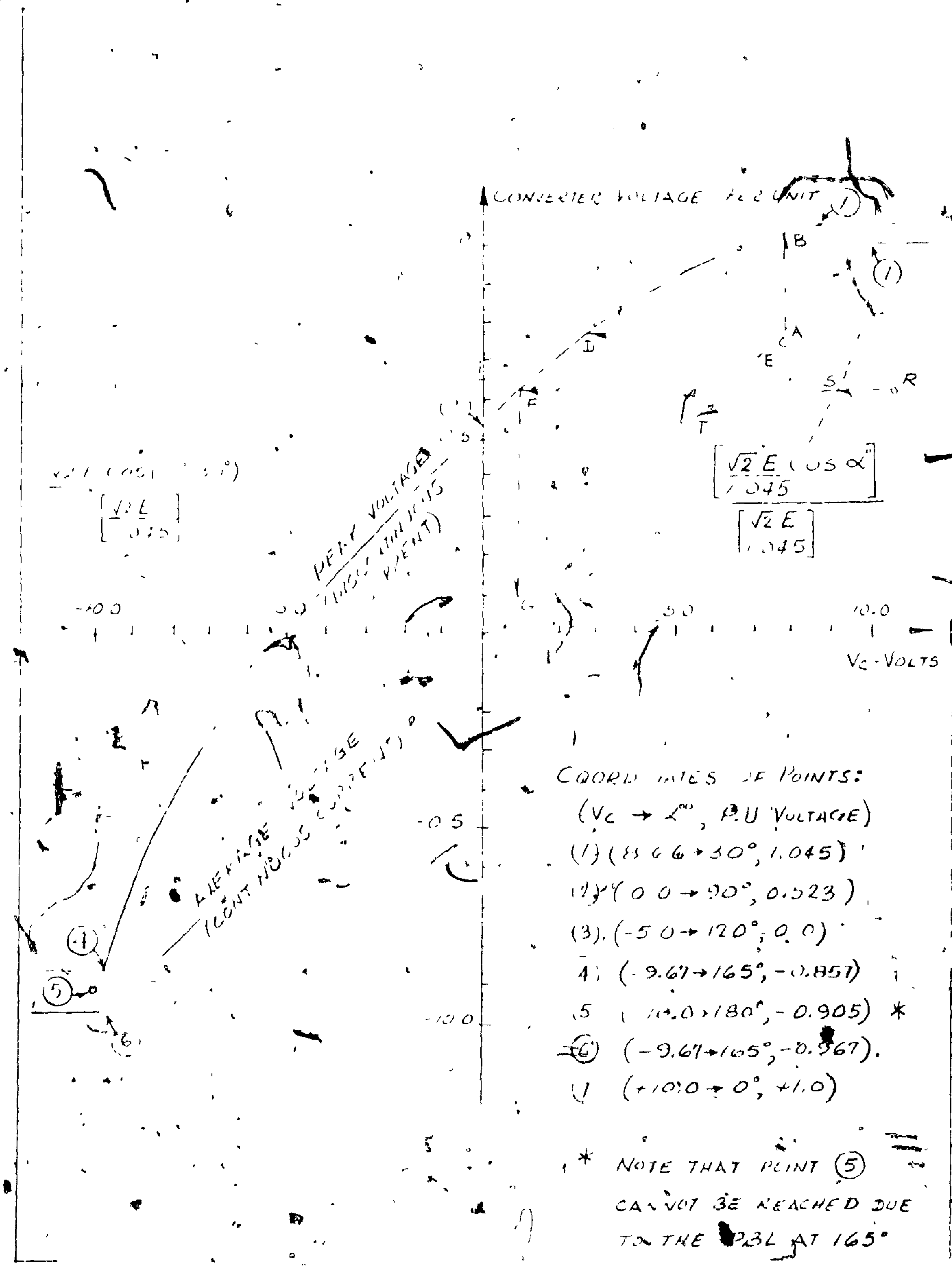

FIGURE 5.8. BOUNDARIES OF THE DC TRANSFER FUNCTION FOR A SINGLE CONVERTER

If the converter is supplying a motor armature on an open loop basis, then the converter voltage will move from point (A) in Figure 5.8 to point (B) when the motor load is removed while keeping the control voltage constant. The motor speed and armature voltage rise correspondingly while the motor armature current falls. The current would reach zero if there were no losses present. On the other hand, if the motor speed is held constant by an auxiliary motor which gradually acquires the load as the control voltage V_c is decreased, then the converter voltage remains constant and the armature current gradually decreases to zero as path (C) to (D) is traced. More realistic is the path (E) to (F) which represents the decrease of converter output voltage and control voltage under closed loop speed control as the load is removed from the motor. The closed loop control system will decrease the control voltage in an attempt to match the motor speed to the setpoint speed. The load might be removed from the motor in one of several ways:

1. The motor may be following an upward speed setpoint ramp which suddenly levels off.

2. The motor speed and setpoint are constant until a step reduction in setpoint is made.

3. The setpoint speed is constant but the motor load has an over-hauling characteristic.

If the motor speed is not under regulation by the time the zero armature current point

(F) is reached, then the control voltage will decrease still further towards (F) while the motor coasts downward in speed. If the performance requirements of the drive are not stringent, then this coasting condition may be tolerated provided that the removal of load from the motor was due to reason (1) or (2) as just described. But if the performance requirements are stringent, or if the motor load does have an overhauling characteristic, then once point (F) has been reached the motor torque must be reversed by reversing the armature current (field reversal will not be discussed). If the transfer functions of the two converters are coincident, then the crossover to the reverse converter will cause an overcurrent surge as the voltage impressed upon the armature circuit by oncoming converter will be at point (G) on the continuous conduction locus. This is exactly the case described by Duff and Ludbrook and quoted on Page 46 of this thesis. They solved the problem by injecting a signal into the current regulator during the period that both converters were blanked so that the oncoming converter was phased back beyond the zero current point.[22] That is, the current regulator output was driven beyond the peak voltage curve for the reverse converter (only partially shown) and then released at point (R). The regulator then continued decreasing the control voltage so that reverse armature

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[22] D.L. Duff and A. Ludbrook, "Reversing Thyristor Armature Dual Converter with Logic Crossover Control," IEEE Transactions on Industry and General Applications, Vol. IGA-1, No. 3, May/June 1965, p. 220.

current first started to flow at point (S) and the system settled into continuous current (assuming this was required) at point (T).

Duff and Ludbrook chose to make their converter transfer characteristics coincident by using the bias shifted cosine wave technique combined with both positive and negative crossing detectors.[23, 24] The cycloconverter described in this thesis used two identical firing pulse generators, each using positive crossing detectors only. However because the control voltage to the reverse converter was supplied by a unity gain inverter so that it was always the negative of that for the forward converter, the transfer functions for continuous current flow were again coincident.[25] Because separate firing pulse generators were already in each converter, it was possible to either follow the same scheme as Duff and Ludbrook (or a similar scheme), or else to put a permanent deadband between the converters by phasing back each converter with its own biasing signal.

On Pages 55 and 56 of Section 3.10 herein it was argued that Duff and Ludbrook's scheme of injecting a signal into the current regulator was really equivalent to putting a temporary deadband between normally coincident transfer functions.

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[23] Ibid., pp. 218-219.

[24] See pages 17 to 20 herein.

[25] See pages 20-21 and 93-99 herein.

In fact provision has been made in the cycloconverter described herein to put an actual temporary deadband between the converters at crossover time. This can be done by injecting a single sawtooth shaped artificial current limit (ACL) pulse into the current limit line of the oncoming converter starting at the beginning of the double blanking period. During the pulse decay after the end of the double blanking period, the regulator of the inner current loop should capture the oncoming converter as it enters conduction after being initially phased off. Comparison of this scheme with that by Duff and Ludbrook will show that in each case the temporary displacement of the regulator output voltage with respect to the transfer characteristic of the oncoming converter is the same.

It was also proposed on Page 56 herein that there is very little difference at crossover time between having the current regulator integrate across an equivalent temporary deadband between two normally coincident transfer characteristics and having the current regulator integrate across a permanent deadband between two constantly biased apart transfer characteristics. This is true provided the system is behaving at that moment in such a way that the regulator output will be driven fully across the deadband and that the deadband has been adjusted to the same width in each case. A reasonable assumption is that Duff and Ludbrook implemented their scheme by injecting a phase back pulse (whose polarity at the regulator output depended upon which bridge was oncoming) into the input of a proportional plus integral current regulator. The width of the pulse, and hence the rise time of the regulator output step, probably was the same as the double blanking period of the converters. The height of the regulator output step, and hence the width of the deadband, would then depend upon the width and amplitude of the phase back pulse and upon the open loop step response of the regulator. Therefore any adjustment to the current regulator open loop response would necessitate a compensating adjustment to amplitude of the phase back pulse, assuming that the double-blanking period was kept constant. If instead, a sawtooth artificial current limit pulse were used, as is possible with the cycloconverter described in this thesis, then an adjustment of the current regulator response would require a compensating adjustment to the decay rate of the sawtooth and perhaps to its amplitude in order to keep the deadband width effectively the same. The permanent deadband scheme, unlike the two temporary deadband schemes just described, does not have any interaction between the current regulator adjustments and the deadband width adjustment. The width desired may be obtained by 1) clamping the firing circuits' control voltage input to zero after disconnecting it from the current regulator output, and 2) changing the firing angle of each converter from ($\alpha = 90^{\circ}$) for zero control voltage to a value[26] ($120^{\circ} \leq \alpha \leq 165^{\circ}$) by adjustment of the bias input in the thyristor gating circuit set of each converter. The current regulator may now be tuned without any further adjustment to the deadband.

[26]The phase back limit (PBL) pulses have been adjusted to 165° for the cycloconverter described herein.

That is, although all three schemes should be equally effective in preventing armature current surge in the oncoming converter, the permanent deadband scheme is the easiest to adjust.

Except for dc armature supply applications, the design, construction, and testing of the cycloconverter described in this thesis was completed in 1970. By that time the ACL pulse circuitry had been put on the auxiliary logic card (Plate 12, Appendix I) and provision had been made in the crossover logic cabling and jumpers to handle the ACL pulses (Plate 13, Appendix I). However, the ACL pulse scheme had not been tested in a closed loop armature drive and consequently no mention of it was made in the conference paper[27] written by Hamblin and Barton at that time. No further experimental work was done with the cycloconverter by T.M. Hamblin until early fall in 1973. At that time G. Joos and V. Stefanovic of McGill University wished to use the cycloconverter as a circulating-current-free, reversing, armature supply in their experiments.[28] Except for an easily repaired fault in one power supply, the cycloconverter was functional. Joos and Stefanovic at first used only one converter as a non-reversing supply or else operated the two converters with circulating current as a reversing supply. T.M. Hamblin promised them he would connect the converters as a circulating-current-free reversing armature supply after his return from the October annual general meeting of the Industry

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[27] T.M. Hamblin and T.H. Barton, "Cycloconverter Control Circuits," IEEE Industry and General Applications Group Annual Meeting Conference Record, October 1965, pp. 559-570.

[28] See page 148 herein.

Applications Society of the IEEE. During part of his return trip he met A. Kronk and A.C. Stevenson of the Drive Systems Group at Canadian General Electric in Peterborough, Ontario. After discussing some of the papers they had heard at the convention, T.M. Hamblin asked them their opinion of the temporary deadband scheme as presented by Duff and Ludbrook versus the permanent deadband scheme. A.C. Stevenson felt that the simpler, more reliable approach was to use two sets of gating circuits with a permanent deadband between them. The regulator loop around the converters would automatically swing in the correct direction through the deadband to maintain control, and there was no need for switching circuits (which could be misadjusted) to inject a signal into the current regulator during the double blanking period. Stevenson thought that the two schemes would have identical results for a complete crossover from one converter to another. However he suspected that the permanent deadband scheme would behave more naturally than would the temporary deadband scheme when feeding light, variable loads which cause the drive to run in discontinuous current and to move in and out of the deadband without necessarily fully crossing it.[29]

When reconsidering the above discussion after his return to Montreal, T.M. Hamblin again concluded that the effective action of the Duff and Ludbrook scheme would be the same as that of a permanent deadband scheme. This would be true even on light loads provided that 1) the phase back signal injection period

[29] Summary of a conversation between T.M. Hamblin, A. Kronk and A.C. Stevenson when travelling by car from Toronto to Peterbororough, Ontario on October 11, 1973.

could be kept short compared to the step response time of the current regulator, 2) both schemes had identical loads and regulator tuning, and 3) the deadband widths were identical. On the other hand, T.M. Hamblin realized that the ACL pulse scheme which he had provided in the cycloconverter described herein would not have the same effective behaviour on light loads. Figure 5.9 A shows a trajectory of falling output voltage as the control voltage decreases and is about to enter the deadband. Provided the current regulator reference voltage has changed sign,[30] the double blanking period will begin as soon as there is a sufficiently long current zero period.[31] During the double blanking period the ACL pulse to the reverse converter will move transfer characteristic R away from that of the forward converter as in Figure 5.9 B. The gradual sawtooth decay of the ACL pulse slides transfer characteristic R back towards coincidence as shown by the arrows. Normally the current regulator output voltage would soon intercept transfer characteristic R and armature current would start in the reverse converter. If however because of a pecularity of the load at that moment, the speed regulator output (which is also the current regulator reference input) changes sign, then the current regulator output swing will reverse as in Figure 5.9 C. Because the armature current is zero in the deadband, the reversal of the current regulator reference voltage will immediately trigger another double blanking period. During this period the ACL pulse to the

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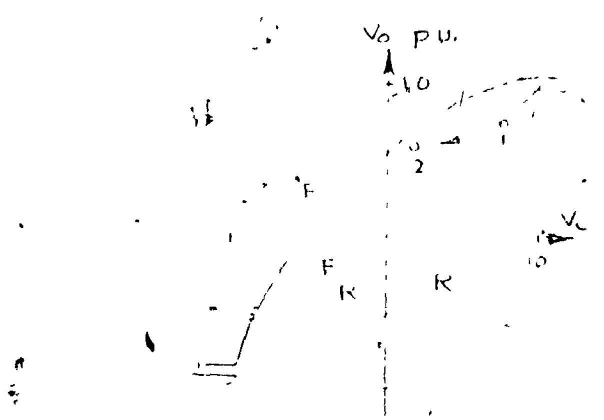
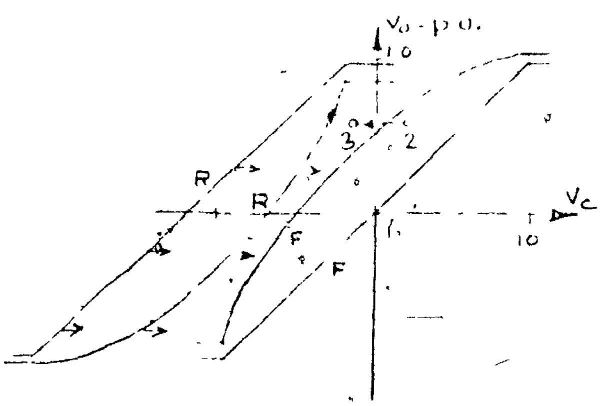
[30] See pages 48, 58 and 60. [31] See pages 131 and 132.



A. COINCIDENT TRANSFER FUNCTIONS

1) Continuous current.

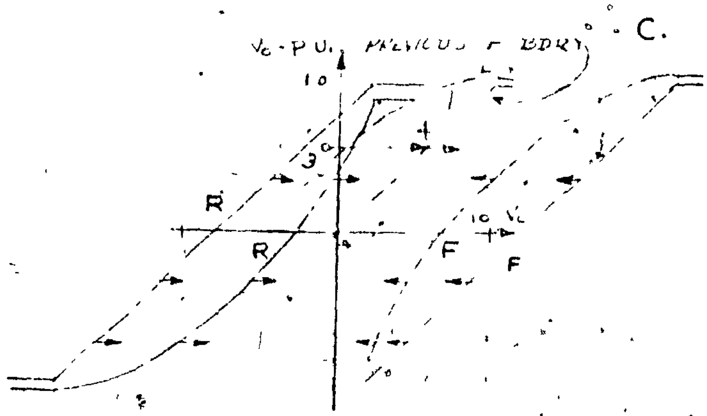
2) Current regulator reference has changed sign. F converter current stops. Crossover logic blanks F and R converters. ACL pulse to converter R phases it back to give case B.



B. REVERSE CONVERTER PHASED BACK

2) Current regulator output is crossing the deadband towards the R characteristic which is sliding back to coincidence.

3) Current regulator reference changes sign. Crossover logic blanks F and R converters. ACL pulse to converter F phases it back to give case C.



C. FORWARD CONVERTER ALSO PHASED BACK

3) The direction of the current regulator output swing reverses after the regulator reference changed sign.

4) If the F characteristic had not been phased back, the F converter would have been in continuous conduction by point 4. Current will restart in the F converter when the F characteristic sliding back towards coincidence is intercepted by the swinging regulator output somewhere beyond point 4.

FIGURE 5.9. ACL PULSE ACTION DURING PARTIAL CROSSOVER

forward converter will move its transfer characteristic F to a new phased back position. At the end of the double blanked period the output of the current regulator will be moving to intercept characteristic F as it slides down the sawtooth of the decaying ACL pulse. But because the reverse converter never entered conduction, there was no need to phase back the forward converter. That is, in this case the performance of the ACL pulse scheme is not as good as that of the permanent deadband scheme. There is no danger of a current surge under these circumstances. Quite the opposite problem exists; the deadband is wider than need be because of the unneccessary ACL pulse applied to the forward converter.

On the basis that the ACL pulse scheme was probably not as good as the permanent deadband scheme on light loads, and that it would probably not be as easy to adjust, the decision was made to put a permanent deadband between the converters. The scheme did prove simple to adjust and satisfactory in operation as the oscilloscope photographs in the next section will show. Admittedly the voltage matching schemes referenced on page 146 herein can provide a shorter dead period at crossover, but the permanent deadband scheme was quite adequate for the servo-analyzer application mentioned earlier herein.[32]

5.8 An Armature Supply with Deadband between the Converters

For reasons explained in Section 5.7, the decision was made to control

[32] See page 148.

the armature current after crossover by putting a deadband between the converters. Originally the drive was set up with each converter phased fully back ($\alpha_f = \alpha_r = 165^\circ$) when the cycloconverter control voltage was zero. The signal line to the voltage crossover detection was disconnected from the output of the master converter input operational amplifier (O/A7 in Plate 13, Appendix I). Instead the detector was connected as shown in Figure 5.10 except that the SPDT switch was in position B. Also the bias voltages were each -10V and the input resistors were 25 kΩ instead of 33 kΩ.

The drive operated satisfactorily from the current surge suppression point of view. But the dead time, which was in the order of 100 ms, seemed excessive. G. Joos felt that the deadband could be reduced safely by readjusting the bias voltages until for ($V_c = 0$) the firing angles were ($\alpha_f = \alpha_r = 120^\circ$). This is less than the ($\alpha_f = \alpha_r = 142^\circ$) point chosen by Stringer[33] or the ($\alpha_f = \alpha_r = 150^\circ$) point chosen by Rettig and Roumanis.[34] However, both of these reversing drives relied entirely upon the width of the deadband to eliminate circulating current between the converters, while the drive described herein depends entirely upon the crossover logic. G. Joos convinced T.M. Hamblin of the validity of using the narrower deadband by developing for him a dimensioned sketch of Figure 5.8 which they, together with W. Scott of McGill University, modified to form the basis of Figure 5.11. The higher slope of

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[33] See page 49 herein. [34] See page 51 herein.

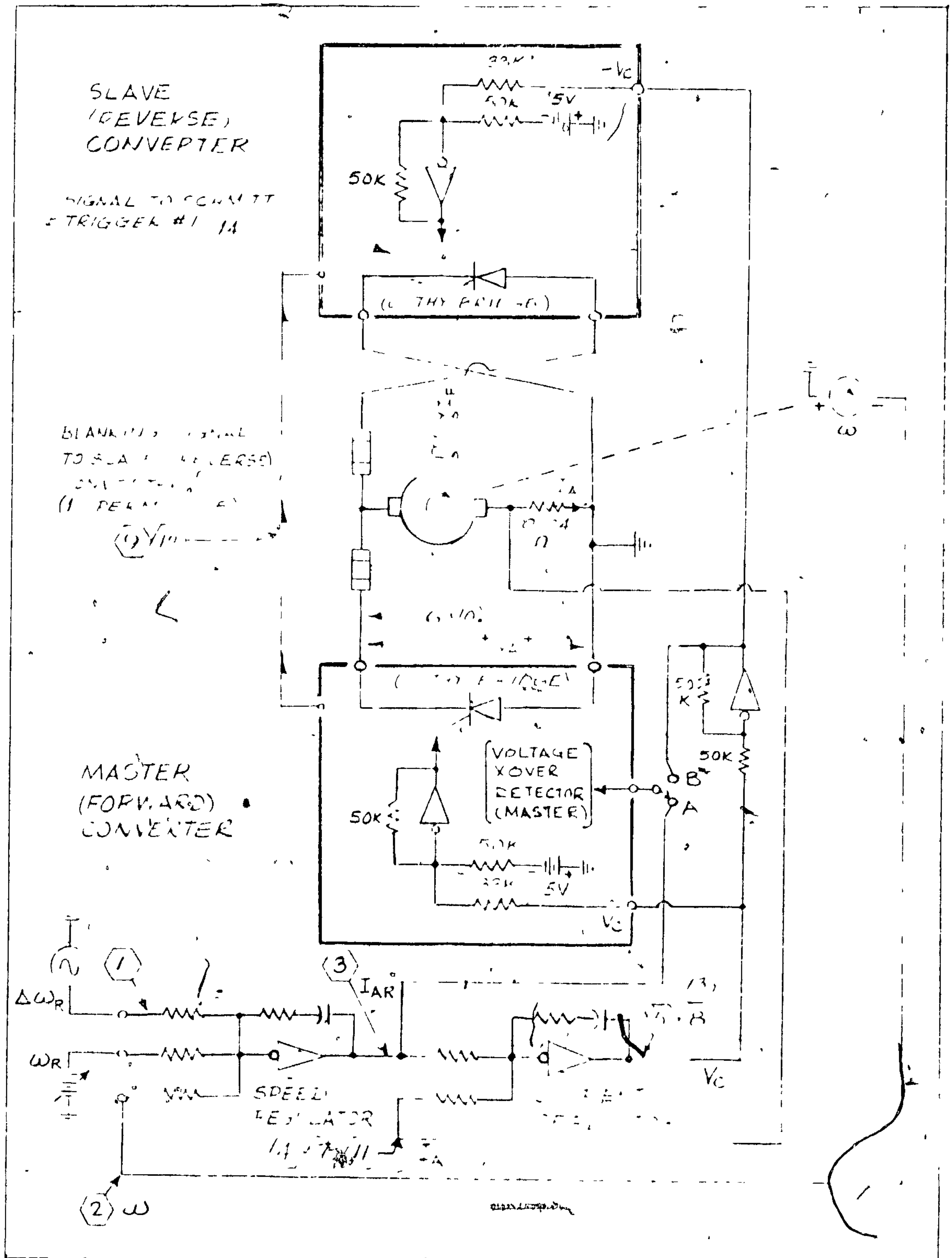

FIGURE 5.10. A SIMPLIFIED CONNECTION DIAGRAM OF AN ARMATURE SUPPLY WITH DEADBAND BETWEEN THE FORWARD AND REVERSE CONVERTERS

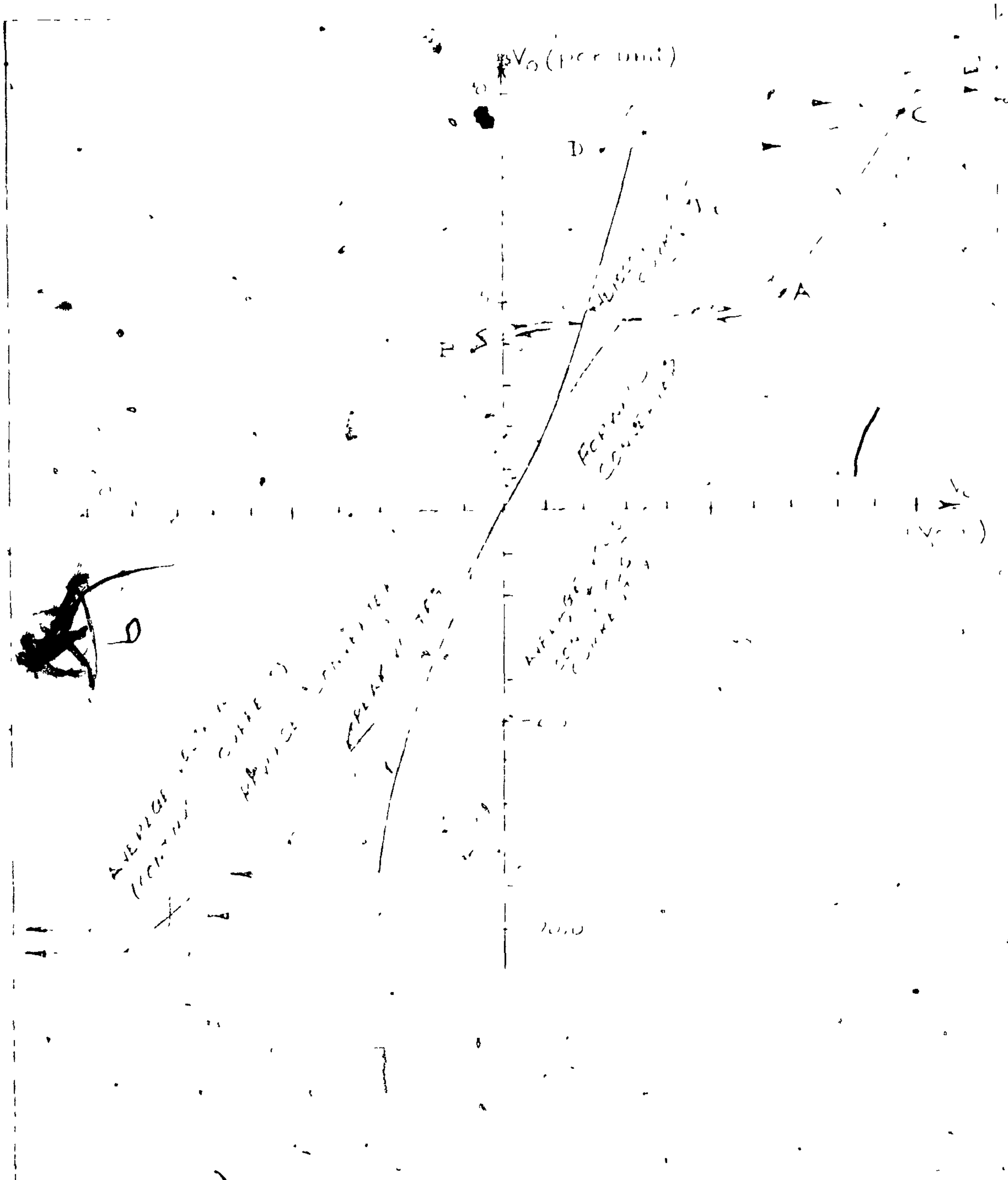

FIGURE 5.11. FORWARD AND REVERSE CONVERTER VOLTAGE TRANSFER CHARACTERISTICS WITH A 120° DEADBAND

the converter voltage versus control voltage characteristic in the latter Figure is due to the use of a 33K rather than a 50K input resistor. Figure 17 in an excellent paper by Haggerty, Maynard, and Koenig[35] is similar to Figure 5.11 herein, but the former is not dimensioned. The input resistor and bias valves in Figure 5.10 were chosen so that peak voltage curves of the anti-parallel, six thyristors bridges were tangent at the (V_c 0) point.

Figures 5.12 to 5.16 are multiple exposure oscilloscope photographs showing the crossover action of the drive when the speed reference was varied sinusoidally at 6 Hz. The markings to the left of each Figure show the sequence in which exposures were made (A, B, C, etc.) and the zero reference mark for each trace. The trace numbers to the right of the Figures also appear on the simplified connection diagram of the drive (Figure 5.10). The regulator portion of the diagram is a simplified equivalent of the regulator designed by G. Joos. Traces 1 and 3 have inverted polarity with respect to Figure 5.10 because an incorrect equivalent circuit was first used when planning the oscilloscope photograph sequence.

The average speed for Figures 5.12 and 5.13 was 840 r/min with an incremental speed reference of 200 r/min peak to peak (Trace 1) supplied by a sinewave signal of 2V peak to peak at 6 Hz. This frequency was well above the

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[35] J. K. Haggerty, J.T. Maynard, and L.A. Koenig, "Application Factors for Thyristor Converter DC Motor Drives," IEEE Transactions on Industry and General Applications, Vol. IGA-7, No. 6, November/December 1971, p. 727.

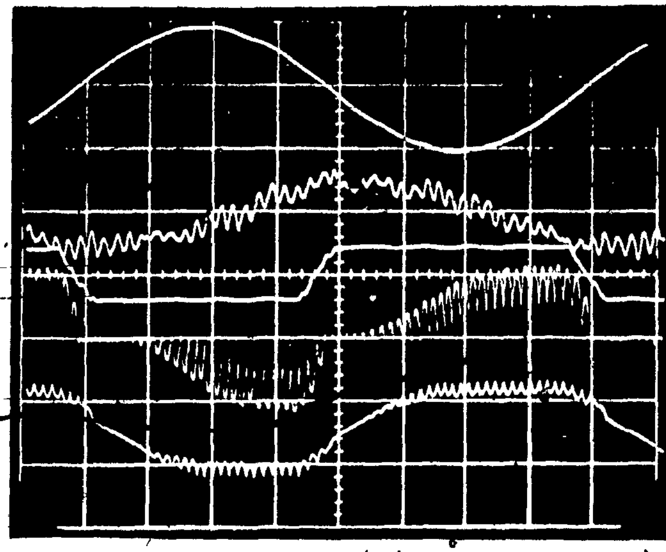

FIGURE 5.12. REGULATOR WAVEFORMS WITH 100 V CEMF AT CROSSOVER

Sweep - 20 ms / cm ; , $\Delta\omega_R = 2\ V_{pp}$ at 6 Hz, ω_R = 840 r/min

Current zero timing period - 150 µs

Double blanking period - 200 µs

For V_c 0 V, α_F α_R - 120°.

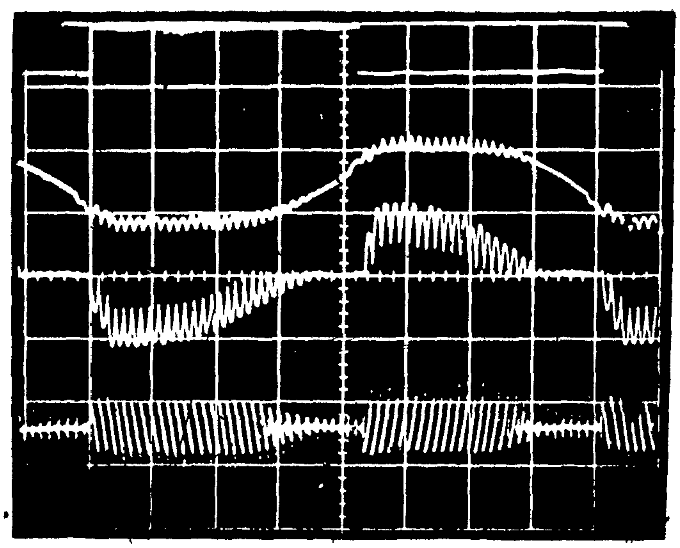

FIGURE 5.13. CONVERTER WAVEFORMS WITH 100 V CEMF AT CROSSOVER

Conditions same as for Figure 5.12 above.

closed loop band width of the system so that the resultant speed change (Trace 2) was only 20 r/min peak to peak. The swing of the speed reference was large enough to drive the current regulator output (Trace 3) into saturation at $\pm$ 10 V which corresponded to $\pm$ 25 A of armature current (Trace 4). The internal spillover current limit of each converter were set to 30 A to avoid interaction with the current regulator. The output of the current regulator (Trace 5) varied between -1V and +6V when swinging from inversion to rectification. The armature voltage (Trace 6) remained close to 100 V during inversion, deadtime, and rectification because the actual speed change (Trace 2) was only $\pm$ 1.2% of the average speed of 840 r/min. Traces 6 and 7 show that the alternating slant of the sawtooth of the output voltage waveform corresponds to the alternating polarity of the armature current. Trace 9 is the firing pulse blanking signal to the slave bridge. The crossover logic used depended upon the logical AND of the output voltage crossover detector and the detection of current zero. The current zero detection timing was 150 μs and the double blanking period was 200 μs for Figures 5.12 to 5.16 The voltage crossover detector input was connected to the output of the speed regulator (Trace 3) via position A of the SPDT switch (Figure 5.10). Comparison of Trace 3 with the armature current (Traces 4 and 7) shows that the crossover logic was performing correctly. Examining the output voltage (Trace 6), the armature current (Traces 4 and 7) and cycloconverter control voltage V_c (Traces 5 and 8) shows that system was following a locus marked with the end points A and B in Figure 5.11. The slight hysteresis in the locus occured because the crossover logic blanked the offgoing converter firing pulses as soon as the crossover conditions were satisfied.

The arrows on the ends of the transfer characteristic boundary lines in Figure 5.11 indicate that once phase back and forward limits have been reached, control voltage V_c may be varied without affecting the converter firing angle. In fact the characteristics of the forward and reverse converters cross each other. Hence if the system has been operating at point C (Figure 5.11) then the reverse converter should immediately enter discontinuous conduction once it is unblanked following blanking of the offgoing forward converter. However when starting back from point D in Figure 5.11, the oncoming forward converter cannot enter discontinuous conduction after unblanking until the control voltage V_c has increased enough to pass through the peak voltage characteristic boundary. The validity of the path between C and D in Figure 5.11 is demonstrated by the immediate start of discontinuous conduction in the reverse converter (Trace 11 of Figure 5.14) when the reverse converter firing pulses are unblanked (Trace 12). Once control voltage V_c (Trace 13) dropped to approximately 2 V, the reverse converter entered continuous conduction. During both the discontinuous and continuous period, the reverse converter was inverting power back to the three phase ac line. Trace 14 shows that the positive going zero crossing point detected by Schmitt trigger 1 in the reverse converter was initially held at ($\alpha = 165^{\circ}$) by the PBL pulse superimposed on the sum of the control voltage and the cosine wave for that thyristor. Then as the control voltage moved towards zero, the zero crossing points and consequent firing pulses phased forward, thereby increasing the current amplitude in the reverse converter.

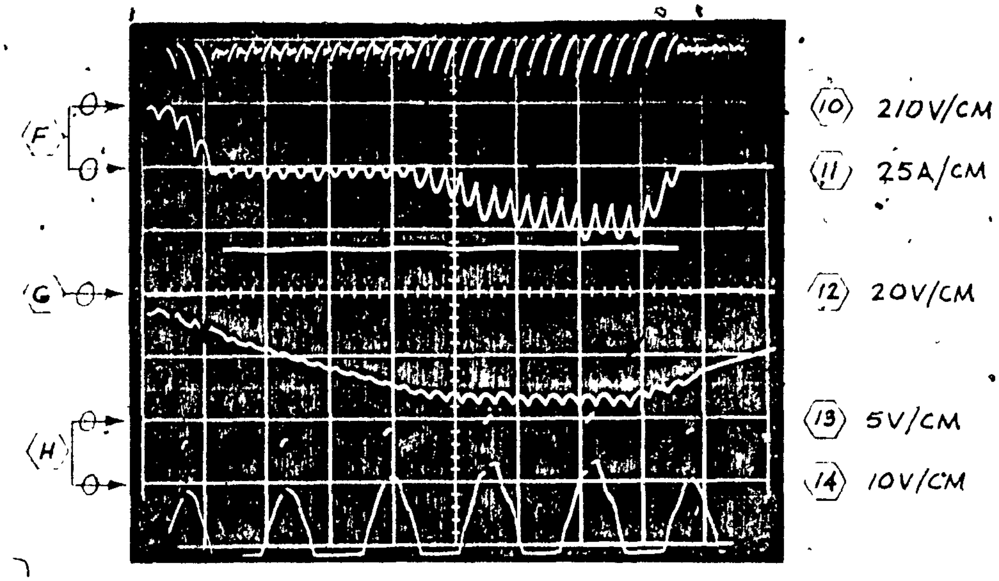

FIGURE 5.14 . CONVERTER WAVEFORMS WITH 200 V CEMF AT CROSSOVER

ω_r = 1680 r/min. Other conditions same as for Figures 5.12 and 5.13

The parameters of the speed control system were kept the same in Figure 5.13 as they were for Figures 5.11 and 5.12 except that the average motor speed was raised to 1680 r/min for Figure 5.13. This corresponded to an average armature voltage of 200 V which placed path CD in Figure 5.11 above the peak voltage transfer characteristic and below the continuous current transfer characteristic of the reverse converter. Increasing the average speed reference raised the average motor speed and armature voltage so that path CD was raised towards the continuous current transfer characteristic of the reverse converter. That is, the amplitude of the discontinuous current which appeared immediately in the reverse converter following unblanking increased as path CD was elevated. When CD matched or lay above the continuous current transfer characteristic, the current appearing immediately in the reverse converter was continuous. No inversion shoot throughs were experienced due to the amplitude of the immediate current in the reverse converter. However, it might prove necessary with other converters having higher commutating reactances to retard the phase forward limit in each converter in order to more closely match the maximum values of the voltage transfer characteristics of the converters.

It was mentioned on page 162 herein that the drive was originally set up so that each converter was fully phased back ($\alpha_f = \alpha_r = 165^{\circ}$) when cycloconverter control voltage V_c was zero. The voltage crossover detector on the auxiliary logic card checked the polarity of the control voltage via the SPDT switch (Figure 5.10) which was in position B. The rise of current in the oncoming converter was smooth, but the deadband seemed excessive. In order to decrease the deadband, the biasing was modified so that each converter was phased back to ($\alpha_f = \alpha_r = 120^{\circ}$) for zero control voltage. The system still operated satisfactorily, but the motor armature current (Traces 4 and 7 in Figures 5.15 and 5.16) seemed to start with a jump when the reverse converter entered conduction. In contrast, the forward converter entered conduction smoothly. Examining the blanking signal (Trace 9 of Figure 5.16) showed that current in the reverse converter (Traces 4 and 7) commenced exactly when the control voltage (Traces 5 and 8) became negative thereby releasing the crossover logic. At this time the operating point (Point B in Figure 5.17) in the reverse converter had

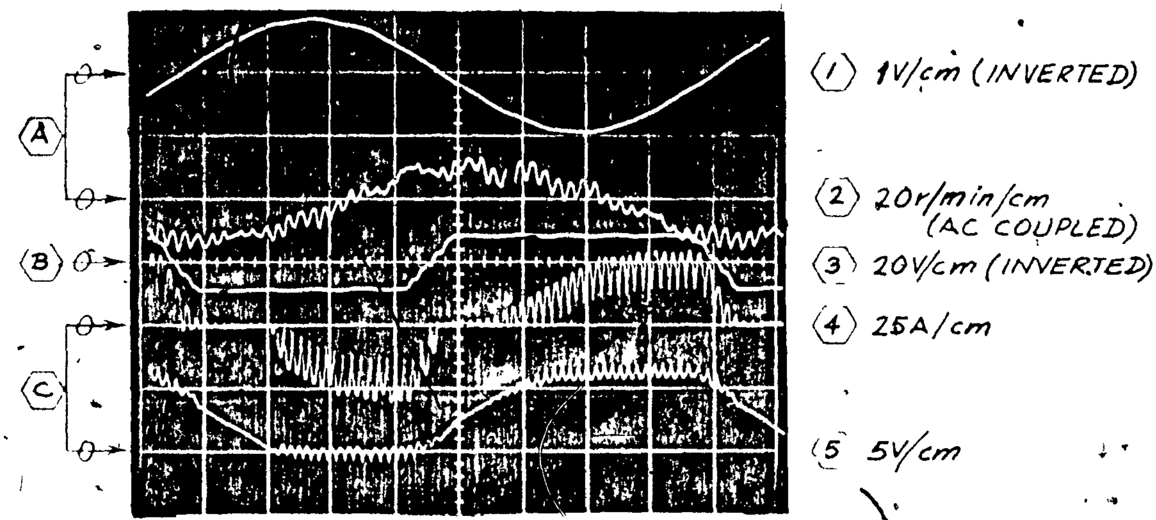

FIGURE 5.15. REGULATOR WAVEFORMS WITH 100V CEMF AT CROSSOVER AND THE SPDT SWITCH OF FIGURE 5.10 IN POSITION B

Other conditions same as for Figure 5.12

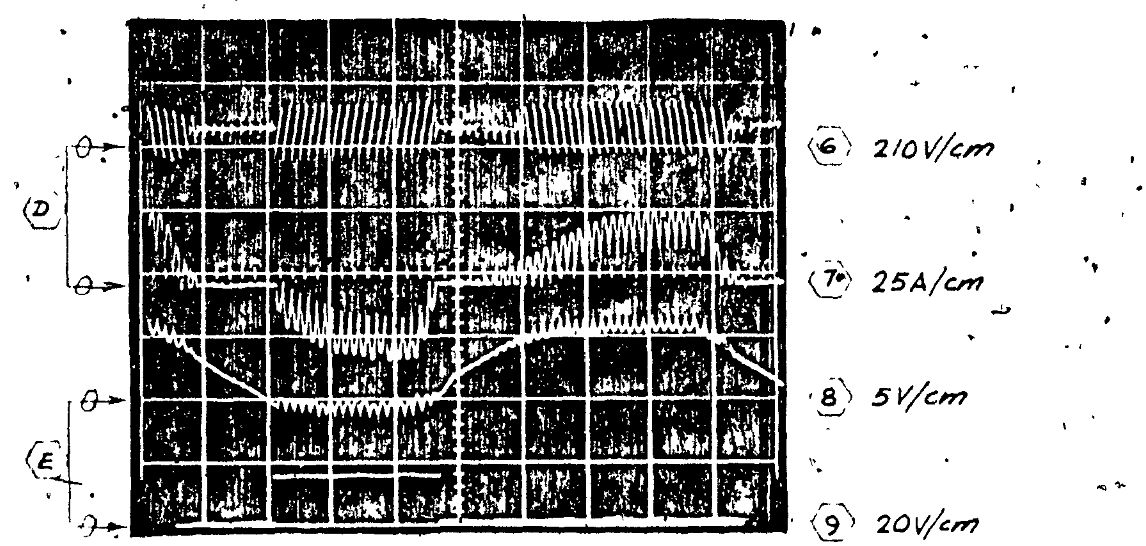

FIGURE 5.16. CONVERTER WAVEFORMS WITH 100V CEMF AT CROSSOVER AND THE SPDT SWITCH OF FIGURE 5.10 IN POSITION B

Other conditions same as for Figure 5.12

already passed the peak voltage characteristic boundary, so that the current amplitude immediately jumped up from zero when the converter firing pulses were released. However the forward converter current started smoothly because the forward converter was released by the crossover logic well before the peak voltage characteristic of the forward converter was reached.

There is no danger in this type of operation provided that the motor armature voltage is less than 0.5 PU output voltage. Path ABC in Figure 5.17 matches the operating conditions of Figures 5.16 and lies below 0.5 PU output voltage. Comparing the armature current Traces 4 and 7 of Figures 5.12 and 5.13 with those of Figures 5.16 and 5.17 shows the latter are almost like the former except that a wedge of reverse armature current is missing in the latter. If however path CDEF was followed in Figure 5.17 because the armature voltage was above 0.5 PU, then there would have been a definite initial overshoot of current when conduction in the reverse converter started at point D. This overshoot may be almost as bad as if the two converter transfer characteristics were not separated at all (Figure 5.8). Hence, it is definitely better to connect the voltage crossover detector to the armature current reference signal as shown in Figure 5.10 with the SPDT switch in position A.

5.9 Circulating Current Elimination Logic Independent of the Load PF

In Section 5.3 herein circulating current elimination logic was described which was suitable for resistive loads and lagging loads controlled on either an open

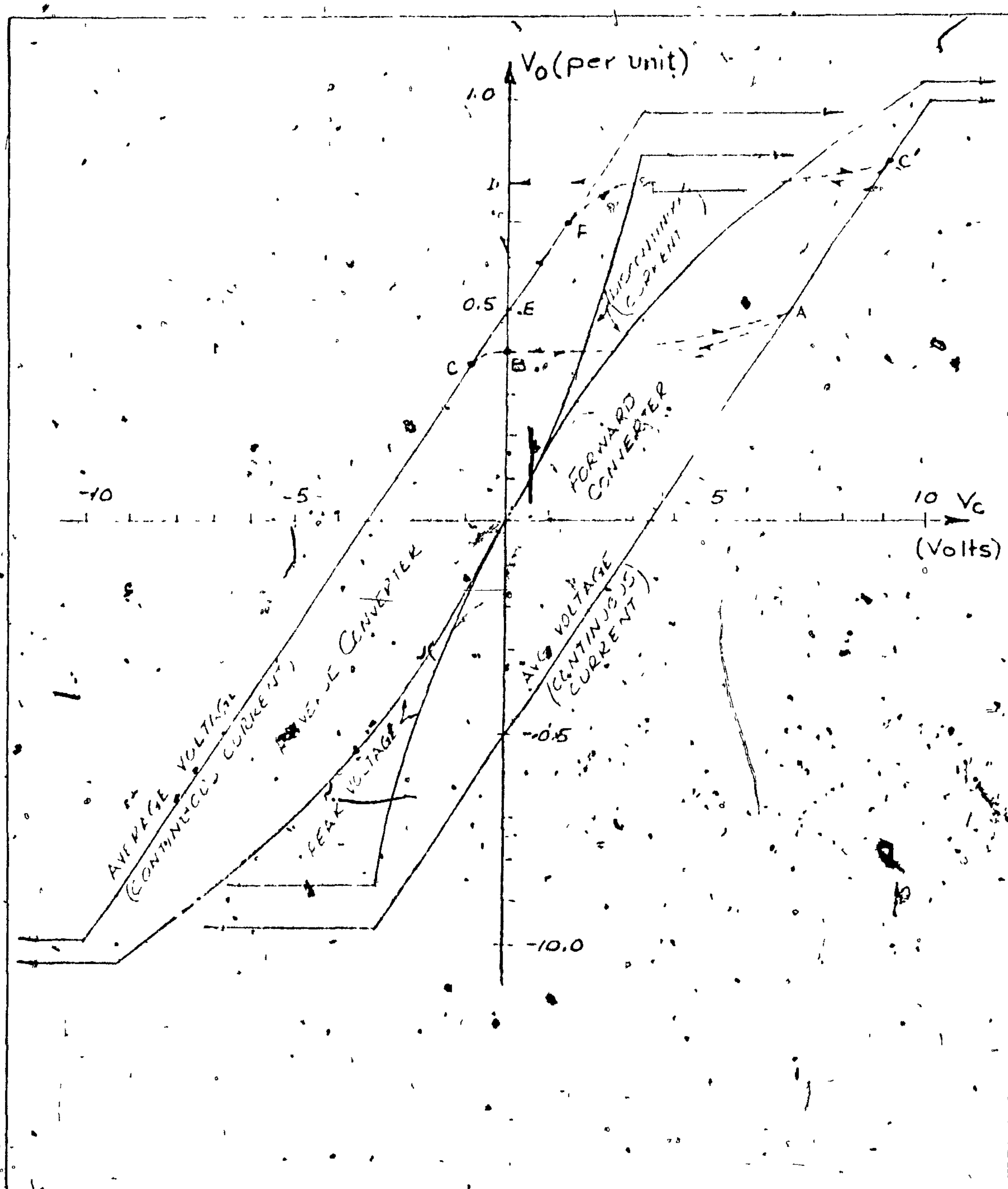

FIGURE 5.17. CROSSOVER OPERATION WITH 120° DEADBAND AND VOLTAGE CROSSOVER DETECTOR MONITORING CYCLOCONVERTER CONTROL VOLTAGE V_c

loop or closed loop basis. The crossover logic depended upon 1) the change of cycloconverter control voltage polarity, 2) the detection of the current zero condition, and 3) an absence of firing pulses in the offgoing converter. This type of logic is excellent for induction motor control because the motor current always lags the motor voltage even when it operates as an induction generator. Figure 5.5 showed both single phase induction motor and induction generator operation under control of this type of crossover logic. Section 5.8 herein demonstrated that this crossover logic was also suitable for closed loop control of dc motor armature current provided that 1) a sufficient deadband was placed between the converters, and 2) the voltage crossover detector monitored the change of polarity of the armature current reference rather than the armature current controller output. The dc motor armature may be regarded as a leading load which was controlled successfully because of the closed loop put around it.

If however it is desired to control other leading loads on an open loop basis, then the crossover logic should depend upon the logical AND of only 1) the detection of the current zero condition, and 2) an absence of firing pulses in the off-going converter. Because the logic does not depend upon detection of the control voltage polarity, the output current may cross through zero ahead of the output voltage and the control voltage without causing large gaps in the current waveforms.

The PF independent crossover logic implemented on the cycloconverter described herein controls the alternate operation of the converters in the following manner:

1. The detection of the current zero signal for 100 μs AND the absence of firing pulses in the offgoing converter will toggle the interlocking flip-flops.
2. Toggling the flip-flop will start a double blanking period fixed at 50 μs.
3. The end of the double blanking period is normally used to trigger auxiliary pulsing in the oncoming converter (Section 5.5 herein).
4. The detection of current zero is not permitted to cause toggling of the interlocking flip-flop again until the end of a timing pulse which begins with the end of the first firing pulse applied to the oncoming converter. This timing pulse limits the maximum rate at which the interlocking flip-flop may toggle while attempting to set up a steady current flow in one or other of the anti-parallel converters.

Figure 5.18 is a logic diagram of a crossover logic card which satisfies the above four requirements.[36] Plate 17 in Appendix 1 and Photograph 4 in Appendix 2 show the card as it was finally constructed. The additional logic elements shown in Plate 17 will be described later herein since they do not apply to the present discussion.

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[36]The writer gratefully acknowledges the assistance of Mr. R.A. Morrison of McGill University in designing the PF independent crossover logic card.

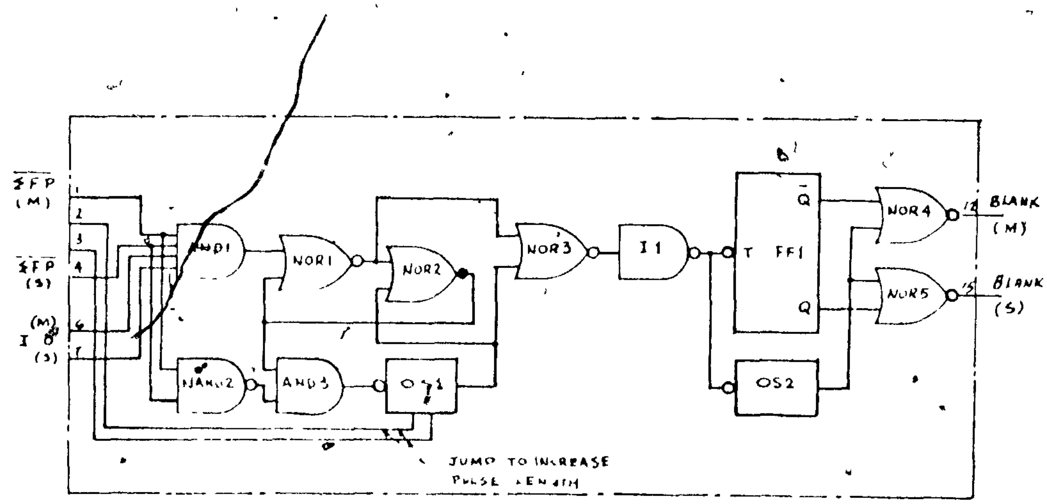

FIGURE 5.18. CROSSOVER LOGIC CARD, PF INDEPENDENT

In addition, the logic is so designed that it ignores any indications of current flow that might appear between the start of the double blanking period and the end of the first firing pulse in the oncoming converter. This was done because the current zero detector scheme, (Section 5.2 herein) was based on monitoring the voltages across all the thyristors of each converter. Hence it may give false indications of current flow during actual current zero conditions (but not vice versa). Figure 5.19 is a flow diagram which explains the states through which the crossover logic passes. Note that NOR 1 and NOR 2 form a latch (NOR 2 output high) during the double blanked state and the latched state to prevent toggling of FF 1 by the rise and fall of any false current zero signals. The end of the first firing pulse in the oncoming converter triggers OS 1 through NAND 2 plus AND 3 to start the holding states during which FF 1 still cannot be toggled. Only after the OS 1 pulse has ended may a high output from AND 1 toggle FF 1 to initiate the current crossover. And of course the AND 1 output will not be high unless there is a current zero detected and no firing pulses are occurring.

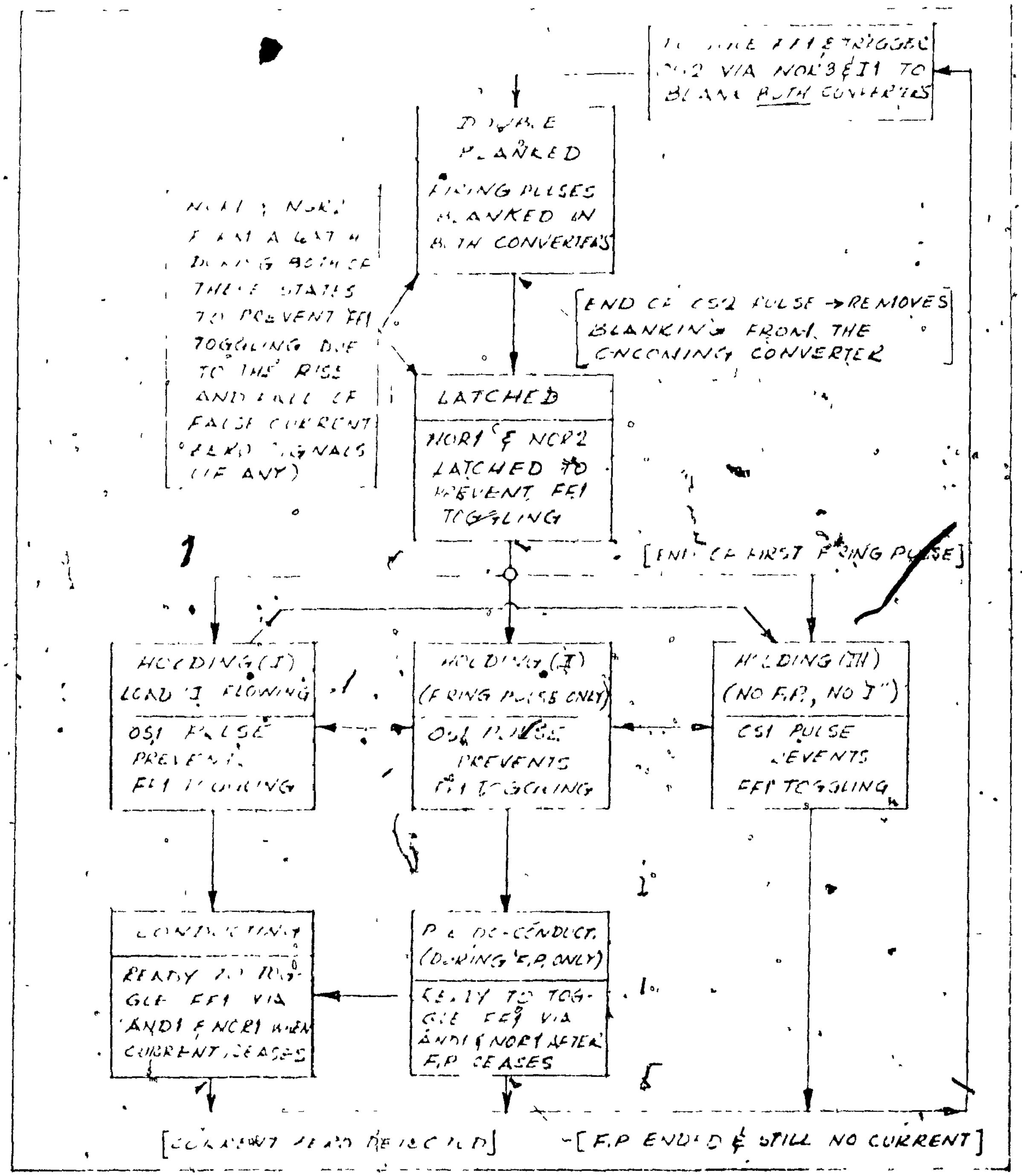

FIGURE 5.19. LOGIC STATES FOR THE PF INDEPENDENT CROSSOVER LOGIC CARD

If by chance a firing pulse starts in the offgoing converter just as FF 1 is toggled, the removal of the firing pulse by the double blanking action may trigger OS 1 prematurely. However this will not adversely affect the changeover of converters provided that the first firing pulse in the oncoming converter appears before the end of the OS 1 pulse. If desired, this problem may be avoided by taking the inputs to NAND 2 from additional firing pulse detector NORs to be connected at the emitter follower outputs of the firing pulse delay circuits (Figure 5.16 on Page 140).

Figure 5.20 is a double exposed oscilloscope photograph of the waveforms of a single phase synchronous motor supplied with 26 Hz single phase power from the cycloconverter when using the PF independent crossover logic. The top three traces show the motor operating as a leading load. Trace 3, cycloconverter control voltage V_c, was superimposed during the second exposure. Hence the bottom three traces which show the motor operating with lagging PF may be directly compared with the top traces showing leading PF operation.

If the combination of the control voltage and load is such that the load current is not continuous following crossover, the PF independent crossover logic will alternately call on the two converters until one of them manages to establish continuous current. This type of behaviour is seen in Figure 5.21 wherein the cycloconverter control voltage was a $6V_{pp}$, 9 Hz sinewave and the load was a

4.3Ω resistance in series with a 9 mH inductance. In Figure 5.22 all circuit conditions are the same except that the PF independent crossover logic card has been removed and the crossover logic card suitable for resistive and lagging PF loads substituted. Comparison of the two Figures shows the advantage of using the latter card if the load PF is known to never be leading. Alternately the pulse from OS 1 in the PF independent crossover logic may be lengthened sufficiently to permit more than one firing pulse by the oncoming converter when it is attempting to establish continuous current flow.

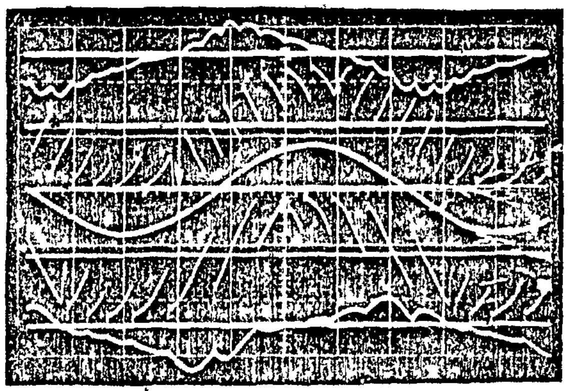

FIGURE 5.20. SYNCHRONOUS MOTOR OPERATION AT 26 HZ WITH PF INDEPENDENT CROSSOVER LOGIC CARD

Sweep = 5 ms/cm; V_c = 7.5 V peak, 26 Hz sinewave

Trace 1 = Load current (30° leading) at 10 A/cm

Trace 2 = Load voltage at 210 V/cm

Trace 3 = Control voltage V_c at 10 V/cm

Trace 4 = Load voltage at 210 V/cm

Trace 5 = Load current (30° lagging) at 10 A/cm

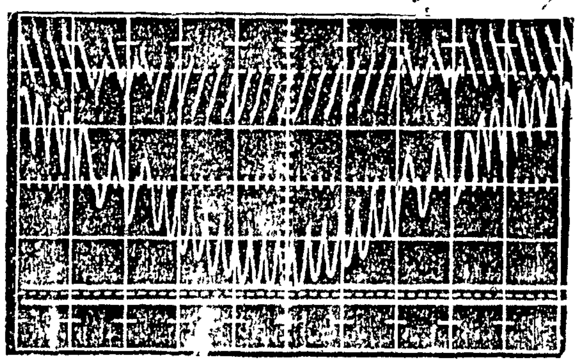

FIGURE 5.21. PF INDEPENDENT CROSSOVER LOGIC ATTEMPTING TO ESTABLISH CONTINUOUS CURRENT

Sweep = 10 ms/cm
V_c = 3.0 V peak, 9 Hz sinewave; Load = $(4.3 + j\,0.51)\,\Omega$
Current zero timing = 100 μs; Double blanking = 50 μs
Trace 1 = Load voltage at 210 V/cm
Trace 2 = Load current at 10 A/cm
Trace 3 = One shot OS1 (short period) at 20 V/cm
Trace 4 = Firing pulse detector NOR, master bridge, at 20 V/cm

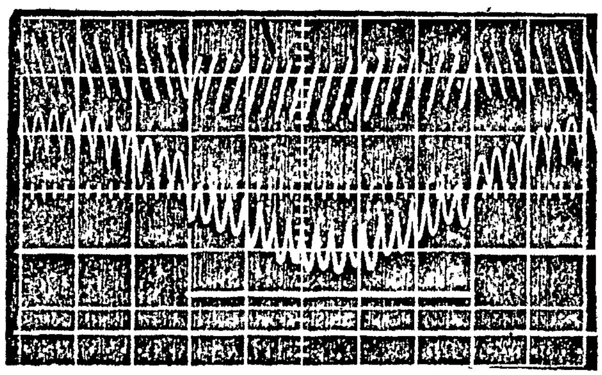

FIGURE 5.22. WAVEFORMS WITH CROSSOVER LOGIC SUITABLE FOR RESISTIVE AND LAGGING LOADS

Conditions same as for Figure 5.21

Trace 1 = Load voltage at 210 V/cm
Trace 2 = Load current at 10 A/cm
Trace 3 = Master bridge blanking signal at 20V/cm
Trace 4 = Firing pulse detector NOR, master bridge, at 20 V/cm

Examining Plate 17 in Appendix 1 shows that provision was made for generating ACL pulses when using the PF independent crossover logic. For reasons explained on Pages 159 to 161 of Section 5.7 herein, the ACL pulse scheme has not been used with either type of crossover logic. However, the PF independent crossover logic was tested in the closed loop armature supply described herein first with a 165° biasing deadband and then with a 120° biasing deadband. Neither experiment was worthwhile. The deadband between the converters did prevent armature current surge, but because the crossover logic was continually making unsuccessful attempts to start current in the other converter whenever the armature current became discontinuous, the armature current pulses appeared in unpredictable bunches. Hence the crossover logic suitable for resistive and lagging loads is the preferred type for closed loop, dc armature supplies.

5.10 A Four Thyristor Reversing Switch

The forward and reverse converters of a single-phase, circulating-current-free cycloconverter are only used alternately. Hence it would appear to be possible to form a single-phase cycloconverter by combining a single converter with a sufficiently rapid, four thyristor reversing switch. The switch permits reversal of the load current without reversal of the current in the single converter. The control logic problem changes from preventing the flow of circulating current between two converters to preventing the reversing switch from short-circuiting the single converter. And because the slave converter of the cycloconverter is normally controlled by the negative of the control voltage to the master converter (see Figure 4.1 on Page 94), then there should be a corresponding means of inverting the control signal to the single converter whenever the reversing switch is in the reverse position.

The analog gates to control the inversion of the control signal were being constructed in 1969 when K. Lidberg published his article in the "ASEA Journal" describing the ASEA type YHMB dc drive which had one converter and a four thyristor reversing switch.[37] The ASEA drive used an outer speed loop and inner armature current loop. During the 10 ms double blanking interval at crossover, the current regulator output was matched to the scaled tachometer voltage so that there was no tendency for armature current surge. The current feedback signal was obtained by rectifying the current transformer signals on the ac side of the single converter. Hence, as explained earlier herein,[38] reversing the armature connection at crossover time did not affect the stability of the current inner loop. But reversing the armature connection did invert the sign of the gain of the outer speed loop at that point. This inversion was then cancelled by connecting at the output of the speed regulator a unity gain, inverting amplifier that could be inserted or bypassed synchronously with the armature connection reversal.

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[37] K. Lidberg, "New Series of Thyristor Converters for Industrial Motor Drives, 20 - 500 kW," <u>ASEA Journal</u>, Vol. 42, No. 5, 1969, pp. 63-68.

[38] See Pages 61 and 62 in Section 3.11 herein.

Locating the analog control signal reversing switch inside the single converter described herein permits the converter and four thyristor reversing switch to be used for either open loop or closed loop operation. However this also implies that the load current feedback, if any, must change polarity just as the load current does: Hence a chopper-isolator or photo-isolator must be used if it is desired to isolate the control circuitry from the power circuitry. Perhaps then if the system will be used only for closed-loop applications, the ASEA scheme is preferable.

Plate 18 in Appendix 1 shows how the crossover logic signals should be interconnected when using the single converter with the four thyristor reversing switch. Below operational amplifiers OA7 and OA8 the analog signal reversing switch is represented by two SPST switch symbols. When the (Hi = Normal) line is true the "Normal" switch connects the analog signal from the output OA7 to summers OA1 to OA6 via the "Normal Bus". Conversely, when the (Hi = Reverse) line is true, the output of OA8 is connected to summers OA1 to OA6 via the "Reverse Bus". The "Normal" logic signal is set true whenever the four thyristor reversing switch is commanded to be in the forward position. Plate 19 shows that each SPST switch was actually implemented by using a six diode analog gate.[39] The gain of the gate was made very close to unity and quite linear by proper choice of the circuit values and careful matching of the diodes. The four 60V

[39] J. Millman and H. Taub, Pulse Digital and Switching Waveforms (New York: McGraw Hill, 1965), pp. 646 - 647.

power supplies for the diode switches are visible at the top of Photograph 1 in Appendix 2. The analog signal switches and drivers are mounted beneath the horizontal plate which supports operational amplifiers OA1 to OA9. Diode gates were used rather than FET gates to switch the analog signals because the FET gate packages were not common in 1969. However their simplicity and ready availability today makes them preferable to the more complex diode switches.

Plate 20 is a schematic of the four thyristor reversing switch and its gating circuitry. As presently connected, the forward pair of thyristors (T1 and T2) each receive a continuous gate signal as long as the crossover logic is calling for forward (normal) current. During the double blanking period neither pair of thyristors is gated. Then the reverse pair (T3 and T4) receives continuous gating signals when the logic calls for reverse current. The square wave carrier frequency gating scheme described by Turnbull[40] was used to provide long duration, isolated gating pulses without saturating the pulse transformers. Plate 21 shows how the square wave carrier was generated by an astable multivibrator, divide-by-two flip-flop, and push-pull power amplifier. They may be seen in Photograph 7 of Appendix 2 mounted along with the pulse transformers and power supply on the bottom of the chassis on which the four thyristors and heat sinks are mounted.

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[40] F. G. Turnbull, "A Carrier Frequency Gating Circuit for Static Inverters," IEEE Transactions on Magnetics, Vol. MAG-2, March 1966, pp. 14-17.

Once the converter and reversing switch were operating successfully, it was realized that continuous gating of the thyristor pairs in the reversing switch was not necessary. All that is required is to use short firing pulses concurrent with the firing pulses in the single converter and directed to either the forward or the reverse pair as required. One direct method of making the pulses concurrent is to derive them from an OR gate connected to the six outputs of the firing pulse delay and double pulsing OR card (Figure 5.6 on Page 140). However this modification has not been made. The only precaution taken has been to lengthen the current zero timing period to 300 μs and the double blanking period to 150 μs to ensure that the thyristors in the switch are definitely nonconducting before crossover even though they do not have their own current zero detectors. Figure 5.23 shows the waveforms of the single converter and reversing switch driving a passive lagging load at 40 Hz. Trace 1 demonstrates the gating action of the diode gate connected to the "Normal Bus" (Plate 18). During the time that one diode gate was off, the other was on as may be seen by the converter output voltage in Trace 2. The load voltage (Trace 3) and load current (Trace 4) reversed smoothly with a short dead time. The auxiliary pulsing was not used when Figure 5.23 was made. Hence the dead time varied from 450 μs to several times that value depending upon circuit conditions at crossover time.

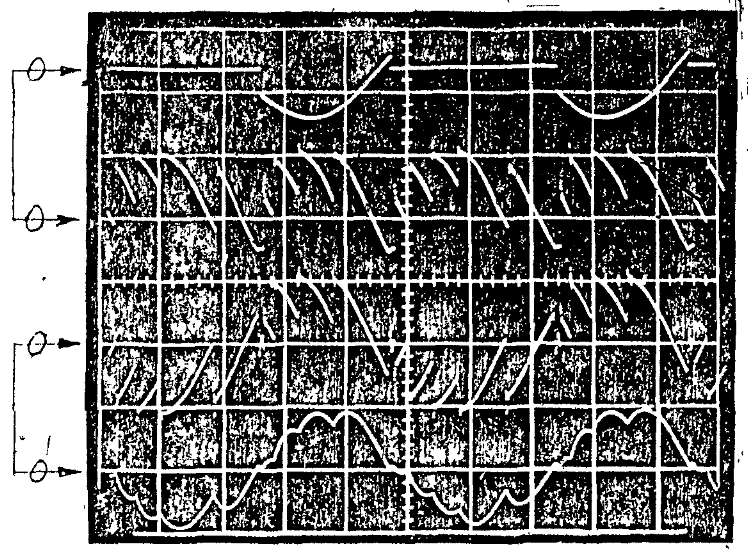

FIGURE 5.23. FOUR THYRISTOR REVERSING SWITCH WAVEFORMS

Sweep = 10 ms/cm
V_c = 8V peak sinewave at 40 Hz; Load = (12 +j22) ohms
Current zero timing period = 300 μs
Double blanking period = 150 μs
Trace 1 = Diode SW "normal" output line at 10 V/cm
Trace 2 = Converter voltage before REV switch at 210 V/cm
Trace 3 = Load voltage after REV switch, at 200 V/cm
Trace 4 = Load current after REV switch, at 9 A/cm

Although no oscilloscope photographs are presented herein, the converter and reversing switch have also been tested successfully with other active and passive, lagging and leading loads. There has been no attempt to use the converter and switch in a closed loop dc armature supply. However the problem of preventing armature current surge after crossover could be solved by using the ACL pulse scheme, or by introducing an adjustable, phase-back, biasing signal into operational amplifiers OA1 to OA6.

It would be logical in the latter case to disconnect the front panel 10 turn biasing potentiometer (Figure 4.2 on Page 95) from the input OA7 (Plate 18 in Appendix 1) and instead connect it to the six operational amplifiers via six 100 kΩ resistors. If the feedback resistors of OA1 to OA6 are doubled to 100 kΩ, then a +10V signal to the input of the converter (input of OA7) will make ($\alpha = 0^{\circ}$) even when the bias potentiometer is set for full phase retard (+10V). A more involved alternative solution would be to adopt one of the armature voltage or tachometer voltage matching schemes referred to earlier.

5.11 Summary

Chapter IV described the features of a three-phase to single-phase cycloconverter which operated with circulating current between its converters. Chapter V has dealt with the additional circuitry required for circulating current free operation with various types of active and passive loads.

The key to successful operation of a circulating current free cyclo-converter is the rapid, absolutely reliable operation of its current zero detector. The thyristor voltage monitoring approach described in Section 5.2 is very fast and works perfectly over the complete range of converter current amplitudes from greater than full output down to less than the holding current of the thyristors. This extremely wide amplitude range gives a very definite advantage over techniques making use of ac or dc current transformers.

The crossover logic suitable for resistive and lagging loads (Section 5.3) depended upon three conditions to choose the crossover time : 1) the change of polarity of the cycloconverter control voltage (or else the current regulator reference voltage in dc armature supplies) ; 2) the detection of the current zero condition in the converters, and 3) the absence of gating pulses at that time. Chapter III herein established that these three conditions are commonly used by thyristor drive manufacturers. Oscilloscope photographs were presented of the cycloconverter described herein using this type of logic to control a single-phase induction motor at 40 Hz.

The development of the firing pulse delay circuits removed the last "bug" from the operation of the cycloconverter. Until that time the transformers of the converters made very ominous grumbles and growls when the cycloconverter output frequency approached 60 Hz. However once the need for the pulse delay circuits had been realized and met as described in Section 5.4, the cycloconverter operated smoothly and quietly through 60 Hz.

Because the first normal firing pulse in the oncoming converter is unlikely to occur immediately after the crossover double blanking period ends, unnecessary gaps may occur in the voltage and current waveforms of the cycloconverter thereby limiting its maximum usable output frequency. The auxiliary pulsing scheme of Section 5.5 provided a method of producing an immediate firing pulse in the oncoming converter following the end of the double blanking period. The auxiliary pulse was generated only if the oncoming converter would have had a firing pulse within the previous 55^{o} (at 60 Hz) had it not been blanked off by the crossover logic. A comparison of two oscilloscope photographs (Figures 5.4 and 5.7) showed the improvement in the waveforms because of the auxiliary pulsing. Auxiliary pulsing is not used with dc armature supplies because of the possibility of armature current surge following crossover.

Section 5.6 discussed three basic problems concerning reversing thyristor armature supplies. The problem of motor heating and decrease of commutation ability due to the high harmonic content of the converter output voltage waveform has been solved by revision of the dc motor design by the manufacturers. The second problem, that of the rise of converter output voltage from the average value of the voltage waveform towards the peak value of the waveform as the load current becomes more and more discontinuous, had two implications. The loss of voltage gain in discontinuous current could be allowed for to some extent by careful regulator compensation techniques (see Page 145). Or, a recent article by M. Johansson and J. Gustafsson has mentioned that in ASEA type YOMC reversing drives an adaptive controller is used to compensate for the loss in converter gain.[41] The second implica-

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41 M. Johansson and J. Gustafsson, "New high-power convertors for d.c. motor drives," ASEA Journal, Vol. 45, No. 3, 1972, p. 85.

tion was that the rise of voltage could cause a disastrous overcurrent surge following crossover because the motor armature voltage would not match the voltage of the oncoming converter. At least one manufacturer had a system to shift the current regulator output in such a manner during the double blanking period that the oncoming converter voltage would match the armature voltage. However this approach was not taken and instead three alternative methods to prevent current surge were discussed in Section 5.7. The final problem mentioned in Section 5.6 was that of modelling the drive for the study of system stability and response. Several references to the literature were made but the topic was not pursued further because the designing and tuning of the regulators in the drive described herein had been performed by G. Joos.

Section 5.7 reviewed the cause of the armature surge problem in detail and three approaches to solve it. All three methods involved introducing either a temporary deadband between the converter characteristics at crossover time, or else introducing a permanent deadband between them. The latter method was chosen because the cycloconverter as it was designed with completely separate gating circuitry for each converter lent itself naturally to putting a permanent phase-back bias into each converter. Also the adjustment of the permanent deadband size, unlike the temporary deadband size, had no interaction with the tuning of the current regulator around the cycloconverter.

Oscilloscope photographs in Section 5.8 illustrated the crossover action of the drive without armature current surge and with a dead time of approximately 20 ms.

Figures 5.11 and 5.14 accounted for the crossover behaviour when the motor armature voltage was higher than the peak voltage characteristic of the oncoming inverting converter. It was demonstrated that for a dc armature supply the best place to connect the voltage crossover detector input was to the armature current regulator reference input (i.e. the speed regulator output) rather than to the armature current regulator output (i.e. the cycloconverter input).

Certain ac loads such as synchronous motors may present a leading PF to the cycloconverter. In order to prevent large gaps in the load current at crossover, the crossover logic for such leading loads should depend upon only 1) the detection of current zero and 2) the absence of firing pulses in the offgoing converter. Section 5.9 describes such a crossover card which also allows for the periodic false indications of current flow produced by the thyristor voltage monitoring type of current zero detector. A double exposed oscilloscope photograph of a single phase synchronous motor operated with both leading and lagging PF at 26 Hz proved out action of the PF independent crossover logic card. The logic may be described as PF independent because it also works for resistive and lagging loads. However if the load is known to never be leading, the crossover logic suitable for resistive and lagging loads should be used beacuse it yields a smoother crossover action than does the PF independent crossover logic when the load current is discontinuous around the crossover point. Experiments showed that the former logic is also preferable for the control of dc armature supplies.

Because the forward and reverse converters of a single-phase, circulating-current-free cycloconverter are only used alternately, it is possible to form a single-phase cycloconverter by combining a single converter with a fast, four thyristor reversing switch. This has been done by ASEA in their YHMB dc armature supply, and by this writer as described in Section 5.10 herein. In the latter case the converter and reversing switch have been used as a cycloconverter at 40 Hz for active and passive, leading and lagging ac loads. The combination has not been used as a dc armature supply, but suggestions were made on how this could be done. Because the performance of the two converter cycloconverter and the single converter with reversing switch cycloconverter is almost identical, the choice between the two may be made strictly on a cost basis. As mentioned earlier on Page 62 of Section 3.11 herein, ASEA's experience was that the single converter and reversing switch had a lower cost at current levels for which the reversing switch thyristors did not have to be paralleled.

CHAPTER VI

CONCLUSIONS

6.1 Review of the Chapters

The cycloconverter was defined in Chapter I of this thesis to be an ac to ac static frequency changer, without an intermediate link, utilizing line commutation of controlled rectifiers. The first commercial applications of cycloconverters were in the conversion of three-phase 50 Hz supplies to single phase 16 - 2/3 Hz at 10 to 15 kV for railway electrification. The use of cycloconverters fell from popularity at the end of the Thirties, mainly because of the limited inversion capability of the mercury arc rectifiers at that time, and because of the relative bulk and complexity of the cycloconverter systems. However before the decline of the cycloconverter, the theoretical operation of converters and cycloconverters with continuous current had been reasonably well analyzed. Interest in the dormant cycloconverter concept was quickly revived following the announcement in 1957 by the General Electric Company of the development of the thyristor. The first applications of cycloconverters were in three-phase to three-phase, variable-speed, constant-frequency supply (VSCF) systems for aircraft. Closed-loop, controlled-slip, variable-frequency induction motor drives quickly followed. At the same time a number of manufacturers were developing circulating current free, reversing, dc armature supplies which were basically three-phase to single-phase cycloconverters. The activity of the manufacturers in the field has been indicated by the publication since 1959 of several hundred papers in English, and in other languages, on converters and cycloconverters. Finally, books by B.R. Pelly in 1971 and by W. McMurray in 1972 added new performance analyses while tying together already published information to finally put cycloconverter design on a completely firm theoretical and practical basis.

Chapter II reviewed some fundamental characteristics of converters and cycloconverters. As long as the converter current was continuous, the average output voltage was proportional to the cosine of the firing angle. This implied that the two anti-parallel converters of a single-phase output cycloconverter should have supplementary firing angles for their average voltages to be in balance. However oscilloscope photographs of the waveforms for constant control voltage showed that a 360 Hz, pulsating, circulating current flowed between the converters because of the sawtooth instantaneous voltage difference between them even when their average voltages were in balance. This circulating current was usually limited by a circulating current limiting reactor. The well known bias shifted cosine wave method was used to make the firing angle of a converter proportional to the inverse cosine of the per unit control voltage. This linearized the average voltage transfer characteristic for continuous current operation and also provided an easy method of keeping the firing angles of the converters supplementary. Oscilloscope photographs compared the waveforms of a single-phase output cycloconverter operating both with and without circulating current. The load current for the circulating current case appeared to have a lower harmonic content. However it was stated that because of various problems experienced in keeping the circulating current amplitude under control, the most popular approach now is to completely eliminate the circulating current by means of detection and logic circuitry which permits only the alternate operation of the two anti-parallel converters.

Chapter III traced in some detail the development of the modern cycloconverter following the introduction of the thyristor by General Electric in 1957. Pages 91 to 93 of that Chapter contain a summary of some of the important contributions to the field. Probably the most remarkable achievement was that of Chirgwin, Stratton, and Toth of Jack and Heintz in Cleveland who were able to generate several kVA of 400 Hz in a VSCF system using simulated thyristors in the cycloconverter ! Once thyristor ratings had increased sufficiently they built a second cycloconverter, this time using real thyristors, and described it in their 1959 and 1961 papers. Their cycloconverter operated without circulating current and became the prototype for the Lear Siegler cycloconverters following their takeover of Jack and Heintz in the early Sixties. The Lear Siegler cycloconverters were developed largely with military and aerospace applications in mind so that by 1963 they had a complete 100 kVA three-phase to single-phase cycloconverter in an eight pound, 3.0 x 9.5 x 11.5 inch package. However other manufactures continued to follow more conventional industrial construction techniques. In 1963 Heck and Myer of Siemens Works described their 30 kW circulating-current-free cycloconverter drive which powered an induction motor with controlled slip and motor airgap flux. An overview of the papers discussed in Chapter III suggests that the European manufacturers had an advantage for several years in the theory and practice of designing variable frequency control systems for induction motors and synchronous motors. In 1965 articles by Duff and Ludbrook of Canadian Westinghouse and by Wesselak of Siemens Works showed that three-phase to single phase, circulating-current-free, dc armature supplies were well established. The series of Brown Boveri articles in 1969 on their 8700 hp, gearless, cycloconverter - synchronous motor cement grinding mill drive demonstrated that methods of constructing and controlling very large three-phase to three-phase cycloconverters had also reached maturity. Finally, books by B.R. Pelly and W. McMurray in 1971 and 1972 put converter and cycloconverter design on equally firm theoretical and practical bases.

The circuitry of a successful three-phase to single-phase cycloconverter was described in Chapter IV. Each converter had a continuous output rating of 30 A average at up to 250 V average. Because one wye-delta transformer was used in each converter rather than one for the two anti-parallel converters, the fundamental frequency of the steady-state circulating current was 360 Hz rather than 180 Hz. Each converter had its own firing pulse generator set using the biased cosine wave principle which linearized the average voltage transfer function as long as the output current was continuous. The converter characteristics were usually very slightly over-lapped so that the circulating current kept both converters in continuous conduction. Phase forward and phase back limit pulses were superimposed on the cosine waves to ensure that the regular firing pulses always occurred in the range ($0^\circ < \alpha < 165^\circ$) no matter what the amplitude of control voltage might be. The 165° phase back limit was chosen to ensure successful commutation during inversion with a 30 A load. Short firing pulses with double pulsing OR gates were used. But it was possible to use longer pulses with double pulsing OR gates to ensure smoother continuous current operation on light loads. An Alpha Blanking Card suppressed any irregular firing pulses which might have occurred in the forbidden range ($180^\circ < \alpha < 360^\circ$) if the rate of change of control voltage had been too rapid in the positive direction. An easily adjusted spillover current limit was provided in each converter so that they could be used individually on an open loop basis if desired. Fault current protection was provided by fuses, but references were made to the much more complete protection schemes required in industrial drives. Standard techniques for suppression of voltage transients due to commutation were followed and references were made to detailed articles on the topic. A detailed review of the phenomenon of self-induced circulating current was made which followed the explanation of B.R. Pelly and was illustrated with an oscilloscope photograph of the load current and the converter currents. The substantial additional load imposed by the self-induced circulating current is one of the main reasons that most modern cycloconverters are designed to be circulating current-free.

Chapter V described the additional control circuitry required so that the cycloconverter described in Chapter IV could operate without circulating current while driving various types of active and passive loads. The circulating current was eliminated by permitting the anti-parallel converters to conduct only alternately. This meant that the detection of current zero when neither converter was conducting had to be very fast and absolutely reliable. The thyristor voltage monitoring type of current zero detector described in Chapter V satisfied these requirements over the complete range of converter current amplitudes from greater than full output down to less than the holding current of the thyristors. Two types of crossover logic were presented. The first type depended basically upon the detection of current zero and the change of polarity of the cycloconverter control voltage (or else the current regulator reference voltage in dc armature supplies). This type of logic was suitable for active or passive loads with unity or lagging PF. It was also suitable for dc armature supplies having an inner armature current loop and an outer speed loop. The second type of crossover logic depended basically only upon the detection of the current zero and hence was independent of the load PF. This was demonstrated by an oscilloscope photograph of ~~a single-~~phase synchronous motor operated at both leading and lagging PF driven by the cycloconverter using the PF independent crossover logic. However other oscilloscope photographs demonstrated that if the load is known to always be nonleading, then it is better to use the crossover logic suitable for unity and lagging PF loads. This type of logic provides a smoother crossover when the load current is discontinuous around the crossover point. When the ~~cyclo~~converter had other than a dc motor armature load, auxiliary firing pulses were applied to the oncoming converter immediately following the end of the double blanking period. This generally reduced the gaps in the load current at the crossover. Three basic problems concerning reversing thyristor armature supplies were discussed. The problem of motor heating and the decrease of commutation ability due to the high harmonic content of the converter output waveform has been solved by revision of the dc motor design by the motor manufacturers. The second problem was the loss of voltage gain and the soaring of the converter output voltage from the average value towards the peak value of the waveform as the current became discontinuous. The loss of voltage could be allowed for to some extent by careful regulator compensation techniques. Also, one manufacturer used an adaptive controller to compensate for the loss in converter gain. The voltage rise when the current became discontinuous could also lead to a disastrous overcurrent surge following crossover because the voltage of the motor armature would not match the voltage of the oncoming converter. Several methods of preventing this surge were discussed. On the basis of simplicity of adjustment combined with reasonable drive response time, the choice was made to put a permanent deadband between the characteristics of the converters. Oscilloscope photographs were presented showing a typical dead time at crossover of 20 ms on an armature load. Because the two converters of a single-phase cycloconverter are used only alternately, it is possible to form a single-phase cycloconverter by combining a single converter with a four thyristor reversing switch. The circuitry needed to do this was described and an oscilloscope photograph of 40 Hz cycloconverter operation was presented. A comparison was made with the ASEA type YHMB reversing dc armature supply which also used a single converter and a four thyristor reversing switch.

6.2 Some Comments on the State of the Art

The converter and cycloconverter portion of the thyristor drive industry is now close to full maturity. All the major manufacturers have the ability to build cycloconverters from the very small sizes (e.g., Lear Siegler at 8 pounds, 100 kVA) to the very large (e.g., Brown Boveri at 6400 kW). And if a cycloconverter (or especially a converter) is desired in a medium power range between these design extremes, then probably they can supply an almost standard package. The package will be no more than almost standard because it will probably have to fit in as part of a much larger control system with other drives, analog controls, and sequence interlocking. The ability of a manufacturer to sell his drive may depend more on the excellence of his reputation for meeting delivery schedules and successfully starting up the total control system than on the technical advances in the control circuitry of his particular converter or cycloconverter. This need for an established reputation may explain why certain manufacturers maintained their share of the market with slightly inferior but definitely working drives while others with highly developed drives but unestablished reputations were unable to take a share of it.

At present most of the manufacturers use the biased cosine method of phase control with some type of phase forward and phase-back limits on the firing angle range. The phase back limit circuit may be the type that adjusts its angle partially or fully to match a change in the load current amplitude. Or it may be fixed as is the phase back limit pulse circuit described herein. Firing pulses outside that range are blocked by a circuit of equivalent effect to the Alpha blanking circuit described herein. The current zero detector is generally based on dc or ac side current transformers rather than the thyristor voltage monitoring principle described herein. But the appropriate safety factors in timing, and so forth, are taken so that the current zero detection functions reliably. The crossover logic generally depends upon the detection of current zero and a change of an analogue control signal polarity unless the load PF is known to be sometimes leading. Armature current surge after crossover may be eliminated by armature or tachometer voltage matching techniques or by deadband techniques. If there is a cost advantage, a single converter and four thyristor reversing switch may be used instead of two converters. Controlled-slip, controlled airgap flux, variable frequency drive systems for induction motors have been described by several manufacturers. Similarly the Brown Boveri articles on their 8700 hp cycloconverter-synchronous motor drive had a very complete description of their system to control the synchronous motor magnetic stator flux linkage to a constant value while keeping the stator current and voltage in phase with each other and at the same speed as the rotor. The net effect was that the motor could not be pulled out of synchronism and the drive ran at the best possible PF.

The manufacturers naturally differ in their methods of packaging of their drives. They all are attempting to make their drives as modular as possible to maximize the ease of maintenance and expandability. And at the same time they are attempting to minimize the cost of materials and assembly. The number of power modules operated in parallel by a manufacturer depends upon his estimate of the load current time profile, the capacity of his individual thyristors considering the estimated load current time profile and their cooling means, and his past success in forcing the thyristors to share the load current. Chapter III briefly described some of the remarkable paralleling done on large drives, but each manufacturer learns his limits by experience. Component current ratings versus load current for converters have been well established since H. Rissik's book,[1] and the book by B.R. Pelly[2] has clarified the special current rating problems that cycloconverters have due to the beat frequency subharmonics and the higher quadrature currents inherently caused by the way they fabricate their output waveform. Of course some sort of safety margin must still be left in case the estimated load current time profile is too low.

The degree of protection provided against long term overloads and against fault currents varies depending upon the drive size. It may consist simply of fuses in very small drives such as the cycloconverter described herein. Or the scheme may include individual thyristor fuses, high speed dc breakers, and high speed ac breakers all carefully coordinated so that it hopefully is not necessary to replace

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[1] H. Rissik, The Fundamental Theory of Arc Converters (London : Chapman and Hall Ltd, 1939) pp. 129 - 132.

[2] B.R. Pelly, Thyristor Phase-Controlled Converters and Cycloconverters - Operation, Control, and Performance (New York : Wiley-Interscience, 1971) pp. 328 - 388 .

several hundred fuses following a fault. In addition current limit circuits and thermal overloads of various types provide protection against long term overloads. Transient voltage protection using LCR networks is a necessity recognized by all drive manufacturers because thyristor drives simply do not operate reliably without them. Also the choke portion of the LCR network is an aid in forcing current sharing among the parallelled thyristors of a large drive.

6.3 Suggestions for Future Work

As explained on Pages 7 and 8 of Chapter I herein, the intent of the work leading to this thesis has always been non-mathematical. And once B.R. Pelly had published his book[3] in early 1971 after his colleague L. Gyugyi had published his thesis[4] in late 1970, there was very little about cycloconverters left for mathematical analysis. However as noted on Pages 147 and 148 of Section 5.6 herein, the problem still exists of how to best model the thyristor drive and to then predict its stability limits. A recent paper by G. De and A.K. Mandal on incremental describing

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[3] B.R. Pelly, op. cit.

[4] L. Gyugyi, "Generalized Theory of Static Power Frequency Changers" (Ph.D. Thesis, University of Salford, October, 1970).

functions for the analysis of subharmonic oscillations in thyristor drives has a good discussion of bibliography on related papers.[5]

M. Johansson and J. Gustafsson briefly mentioned in their paper[6] that ASEA uses an adaptive controller to counteract the loss of converter gain when the load current becomes discontinuous. There would appear to be room for some theoretical and experimental work on this approach.

Chapters 9 and 10 of B.R. Pelly's book[7] dealt with the theoretical principles of and three functional schemes for thyristor firing pulse circuitry. He first proved that the commonly used biased cosine wave type of phase control produces the theoretically minimum possible overall rms harmonic distortion of the output voltage

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[5] G. De and A.K. Mandal, "Incremental Describing Function Analysis of Subharmonic Oscillations in Control Systems with Thyristor Converters," *IEEE Transactions on Industrial Electronics and Control Instrumentation*, Vol. IECI-20, No. 4, November 1973, pp. 229-235.

[6] M. Johansson and J. Gustafsson, "New high-power converters for d.c. motor drives," *ASEA Journal*, Vol. 45, No. 3, 1972, p. 85.

[7] B.R. Pelly, *op. cit.*, pp. 229-277.

wave. But he also presented two other types of firing circuits. One was called "integral control" because its basic principle was to generate a firing pulse each time the integral of the difference between the control voltage and the (suitably scaled) converter output voltage was equal to zero. The other type of firing circuit used a phase-locked oscillator with feedback from the converter output voltage being compared with the reference voltage to yield a difference signal which locked the oscillator. Both of these methods were much less sensitive to ac line noise than was the biased cosine waveform firing circuitry. In particular the "integral control" scheme lent itself to VSCF systems because it was not sensitive to ac input frequency changes either. The functional scheme for the biased cosine wave was more complex than it needed to be, but this was done so that it would have the same type of pulse output as did the other two schemes. Pelly's approach is quite interesting and should be studied by anyone interested in building a cycloconverter.

If, despite the advice in the above paragraph, the cycloconverter described in this thesis were rebuilt following the same general principles, then full use would be made of modern hardware. This would mainly mean using analog and digital integrated circuits as well as FET analog gates instead of discrete components. Pull-out drawer construction would be used to improve accessibility. Analog components and relaying used for the dc armature supply regulators would be built into one of the drawers. Greater use would be made of plug and socket connections rather than barrier strip and cable lug connections between subassemblies. Certain other suggestions for improvements have been made in the body of this thesis.

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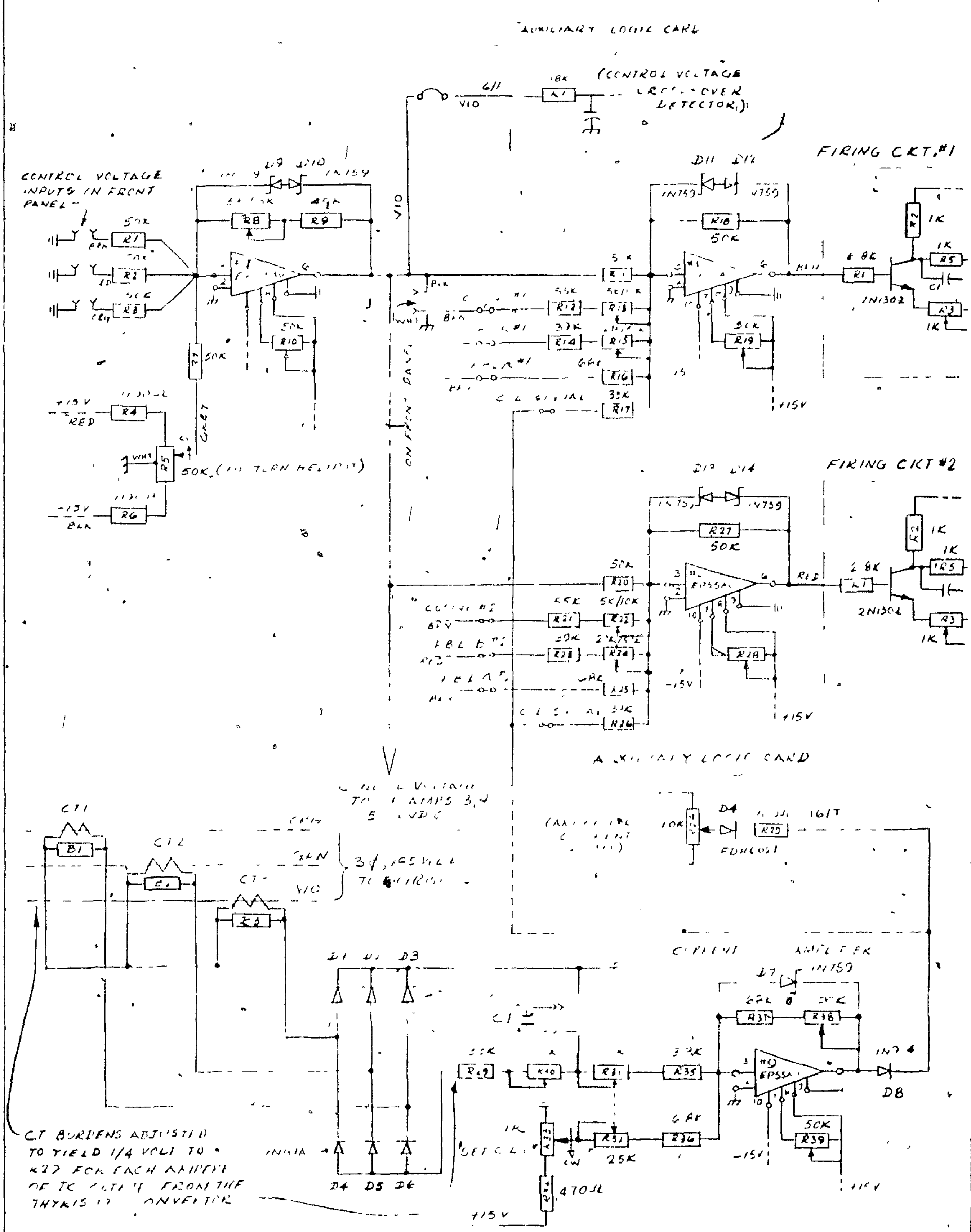
APPENDIX 1

PLATES

PLATE 1.

INPUT, FIRING CIRCUIT, AND CURRENT LIMIT OPERATIONAL AMPLIFIERS



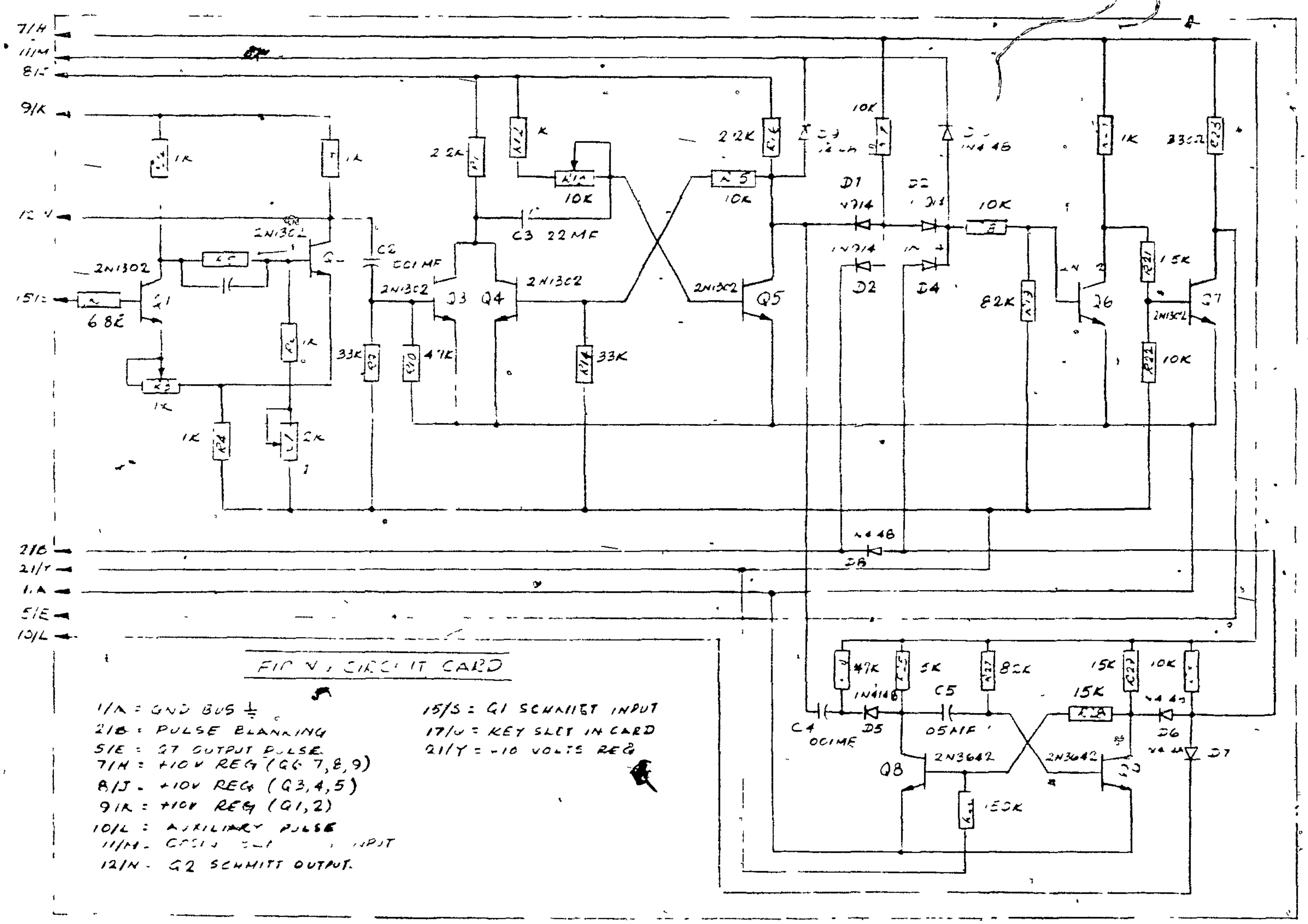


PLATE 2.
FIRING CIRCUIT CARD

PLATE 3.

PHASE-BACK LIMIT (PBL) CARD

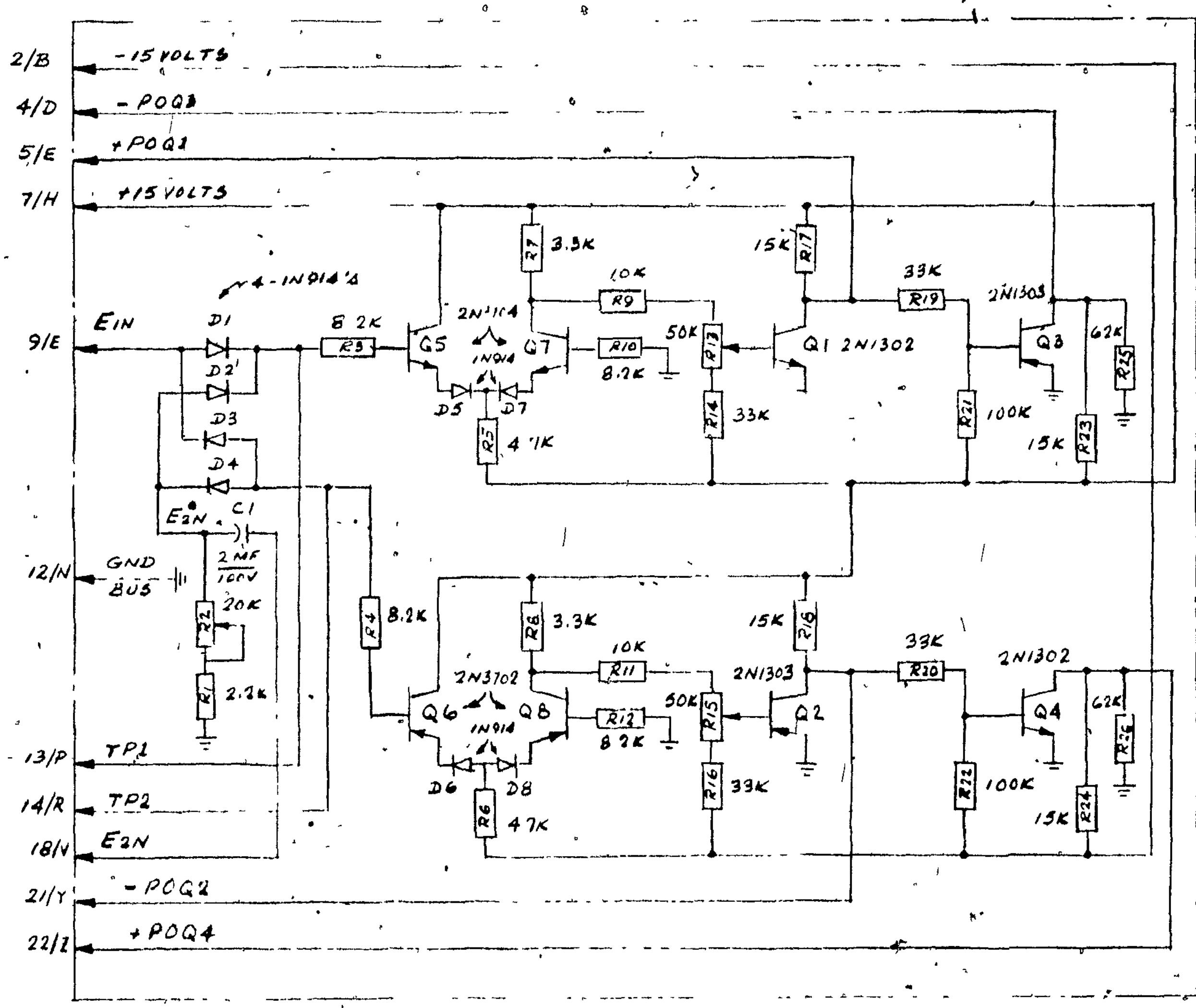
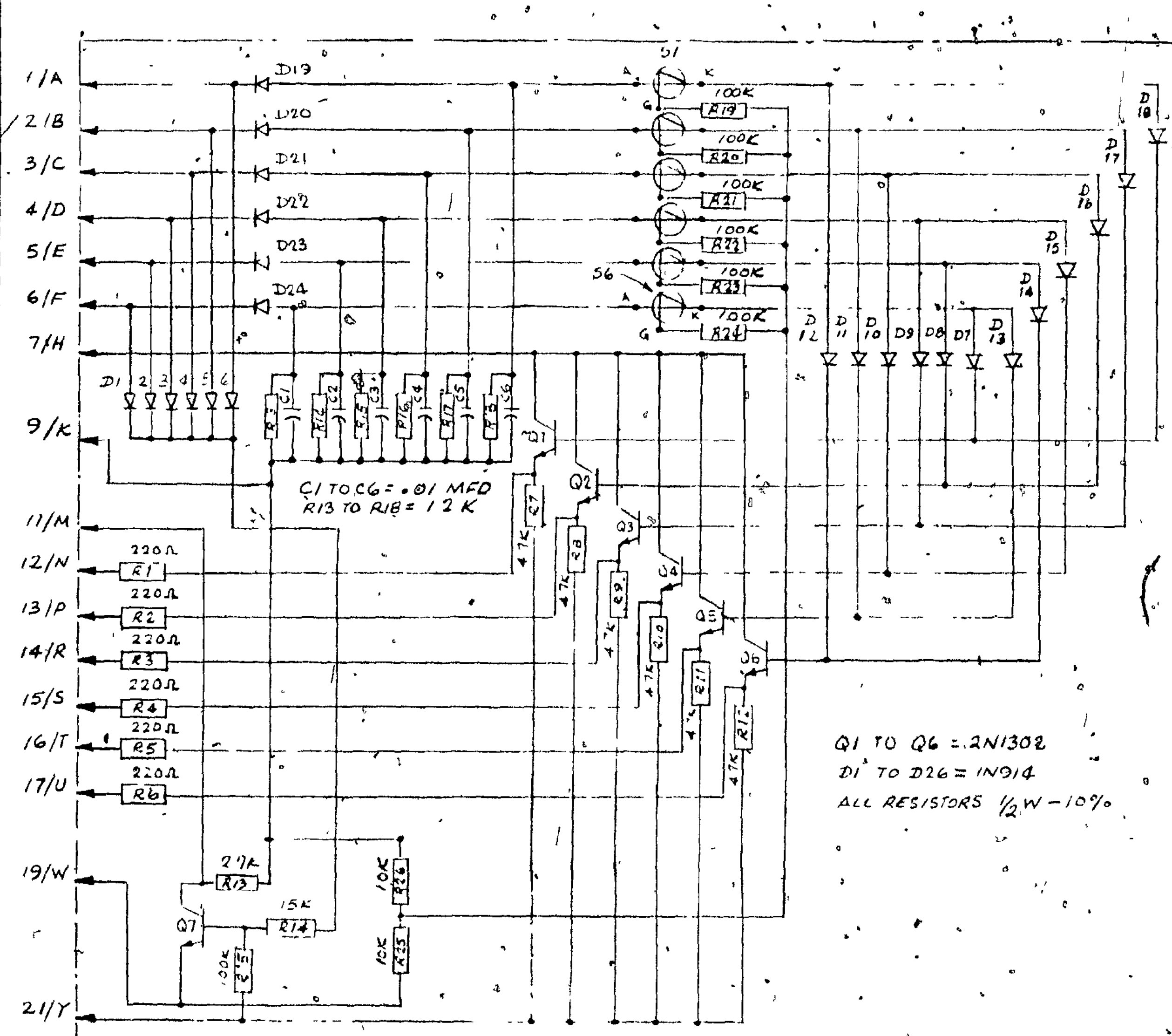


PLATE 4.

FIRING PULSE DELAY AND DOUBLE PULSING OR CARD



Q1 TO Q6 = 2N1302
D1 TO D26 = IN914
ALL RESISTORS 1/2 W − 10%

CONNECTION LIST

1/A = SINGLE PULSE INPUT #6
2/B = " " " #5
3/C = " " " #4
4/D = " " " #3
5/E = " " " #2
6/F = " " " #1
7/H = +10 VOLTS REGULATED
8
9/K = +15 VOLTS, REGULATED
10
11/M - FIRING PULSE DETECTOR OUTPUT.
12/N = DOUBLE PULSE OUTPUT #1
13/P = " " " #2
14/R = " " " #3
15/S = " " " #4
16/T = " " " #5
17/U = " " " #6
18
19/W = GROUND BUS ⏚
20/X =
21/Y = −10 VOLTS, REGULATED
22

THYRISTOR FIRING PULSE SEQUENCE

FIRE #1 RE-FIRE #5
" #6, " " #1
" #2 " " #6
" #4, " " #2
" #3, " " #4
" #5, " " #3

NOTE: THE SILICON UNILATERAL SWITCHES WERE ACTUALLY PNP-NPN ANALOGUES (SEE BELOW)

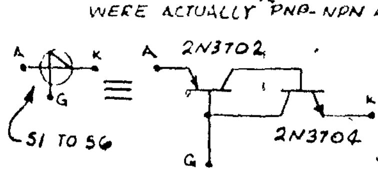


PLATE 5.

ALPHA BLANKING CARD

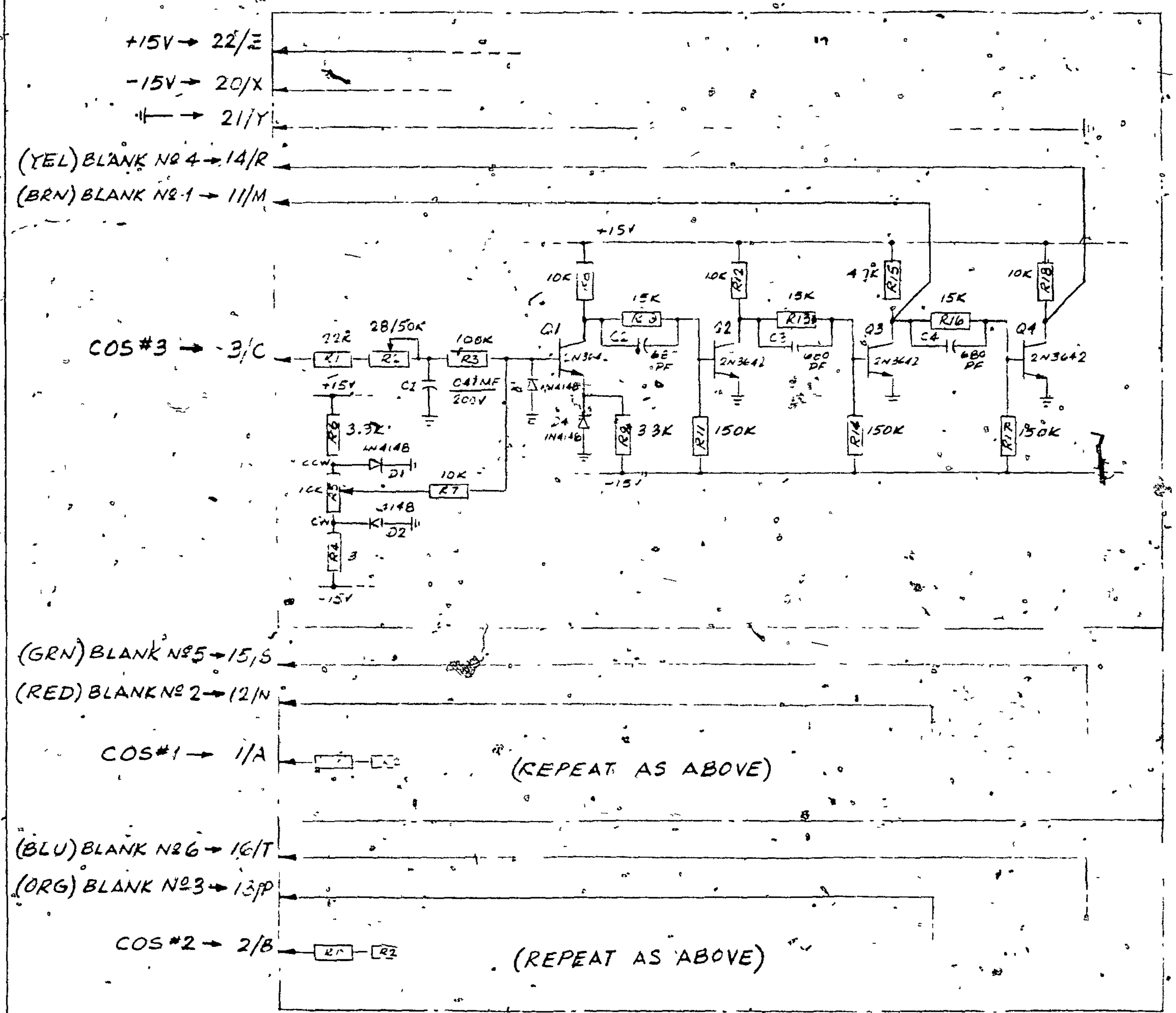


PLATE 6.

GATE PULSE AMPLIFIERS WITH THEIR POWER SUPPLY

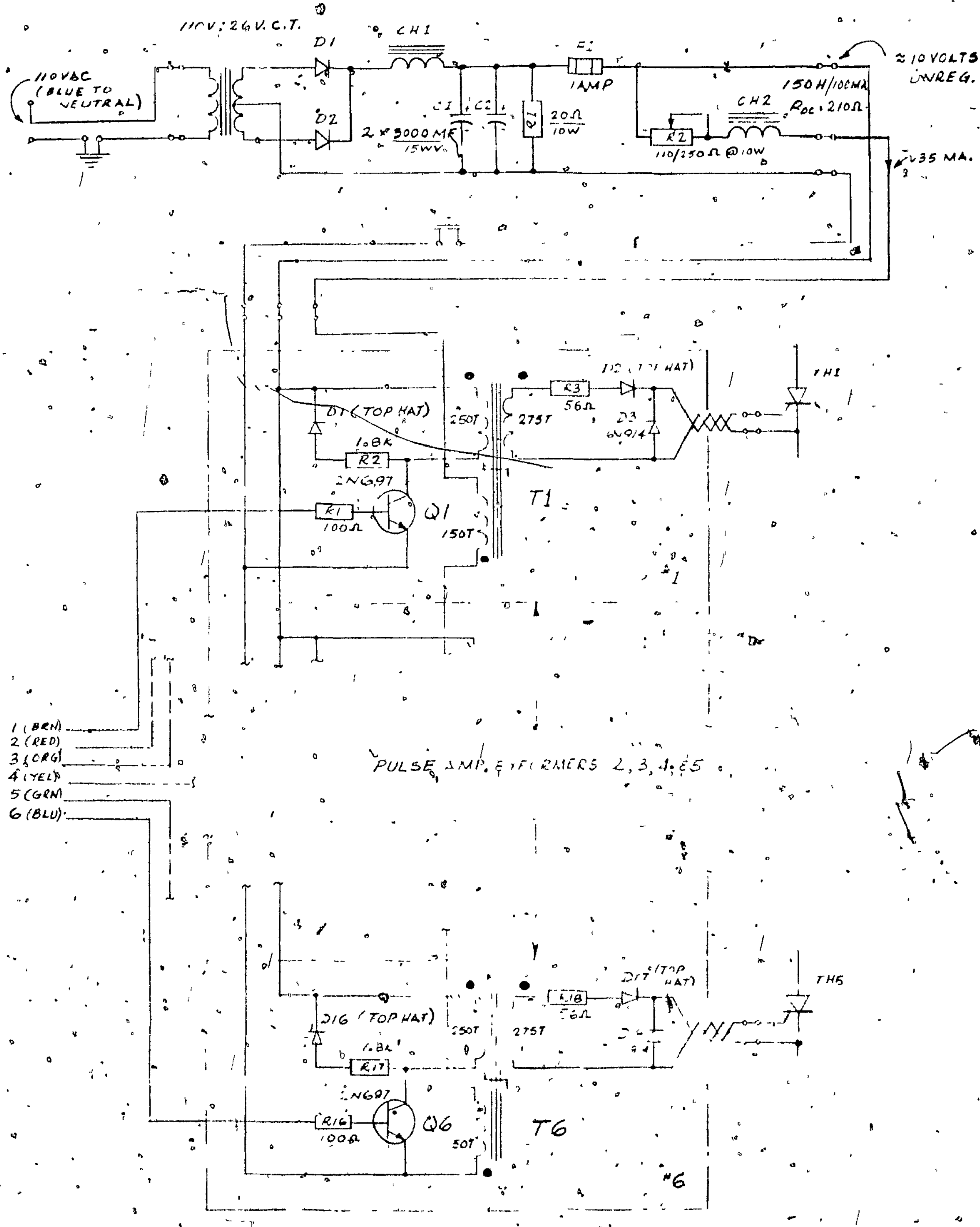
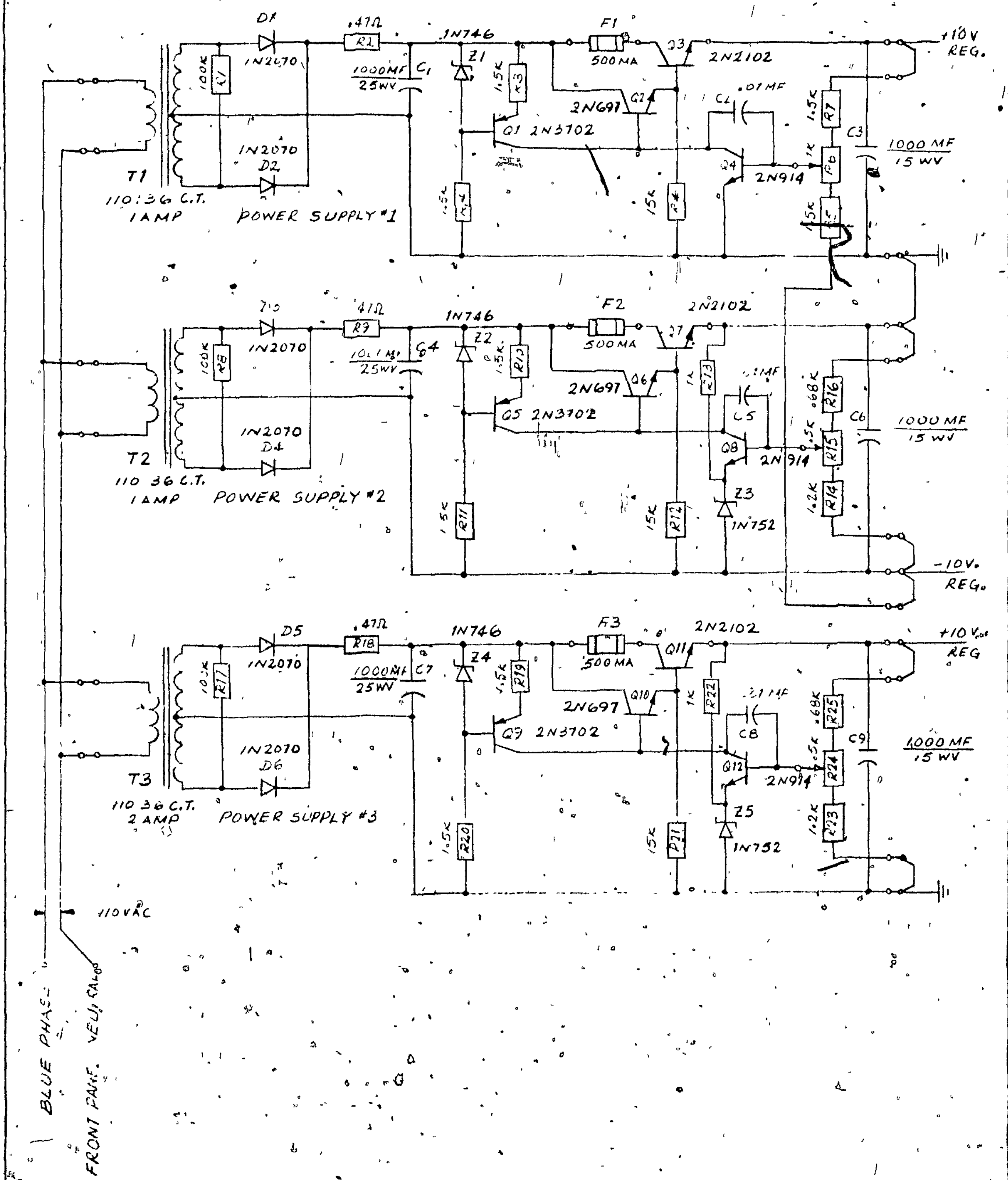


PLATE 7.

±10V REGULATED POWER SUPPLIES



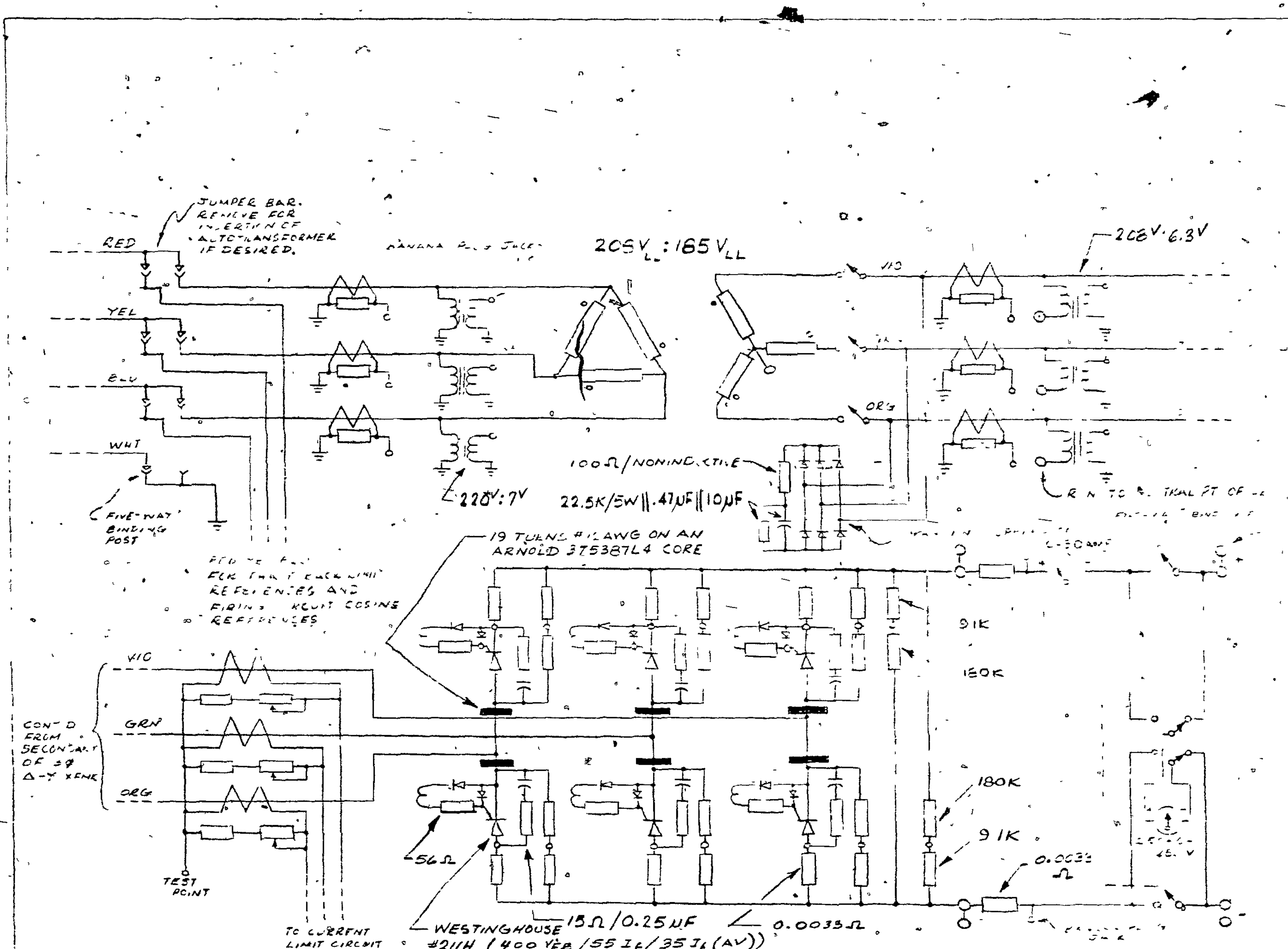
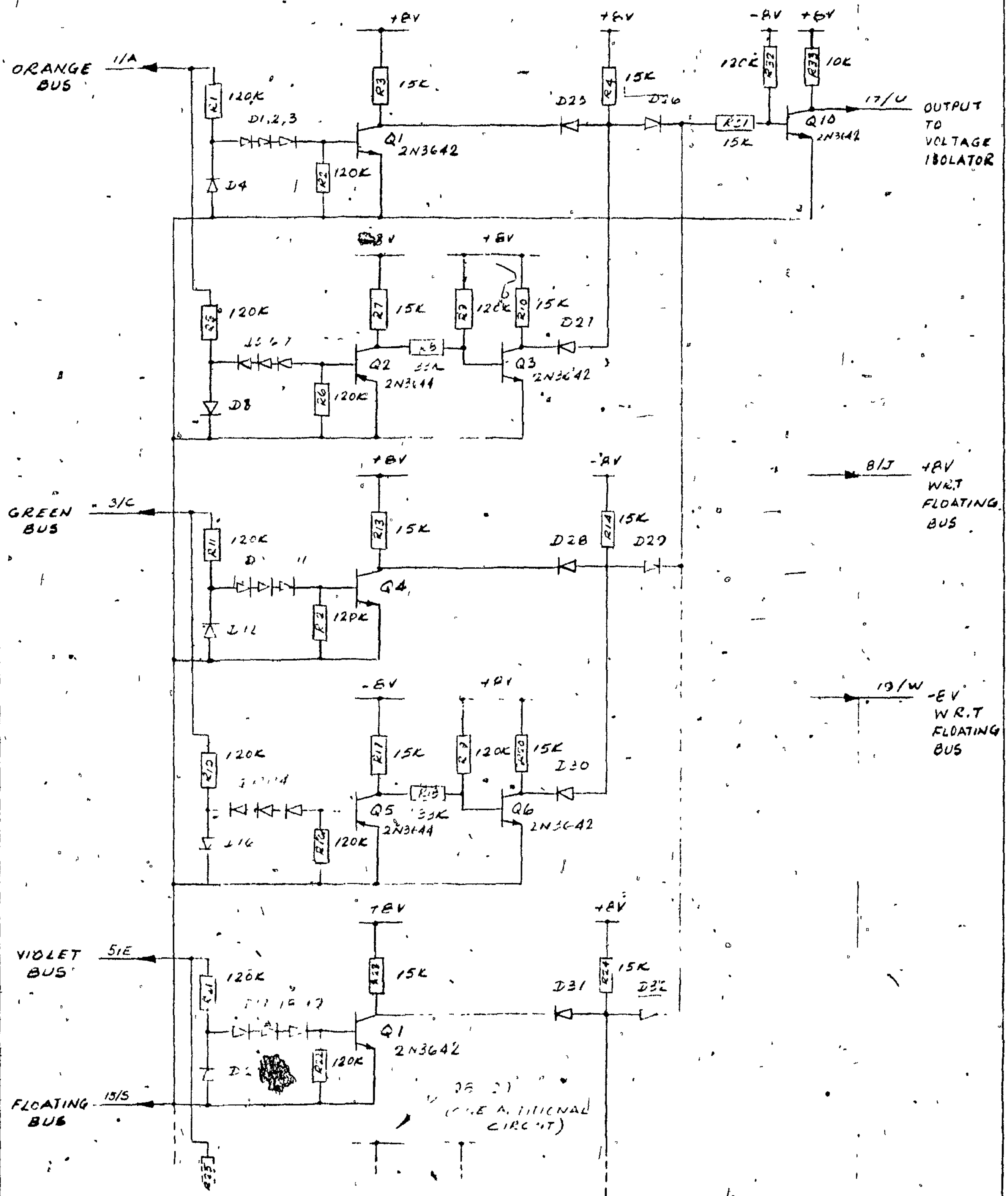


PLATE 8.

CONVERTER POWER SCHEMATIC

PLATE 9.

FLOATING VOLTAGE MONITOR CARD



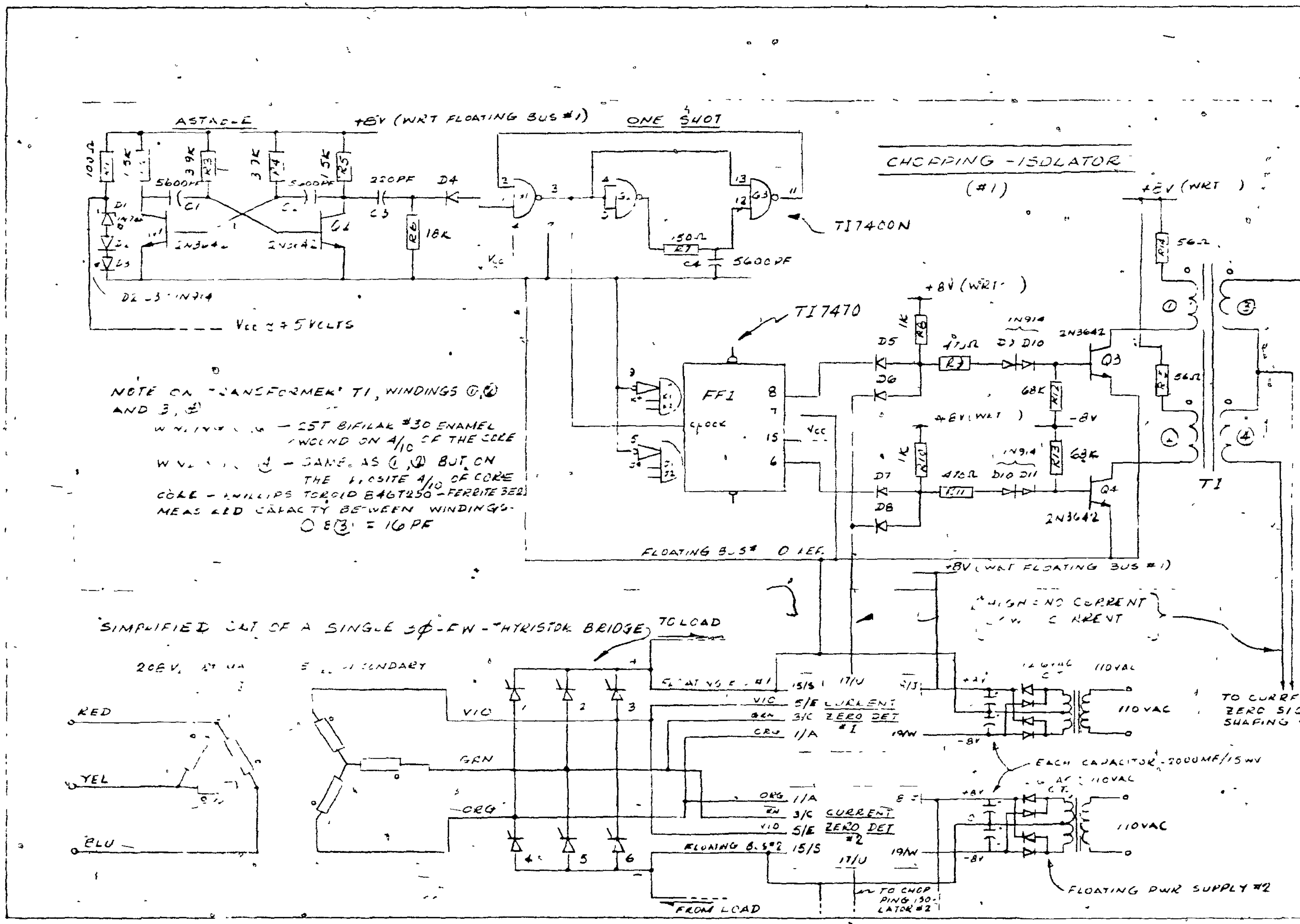


PLATE 10. CHOPPING ISOLATORS

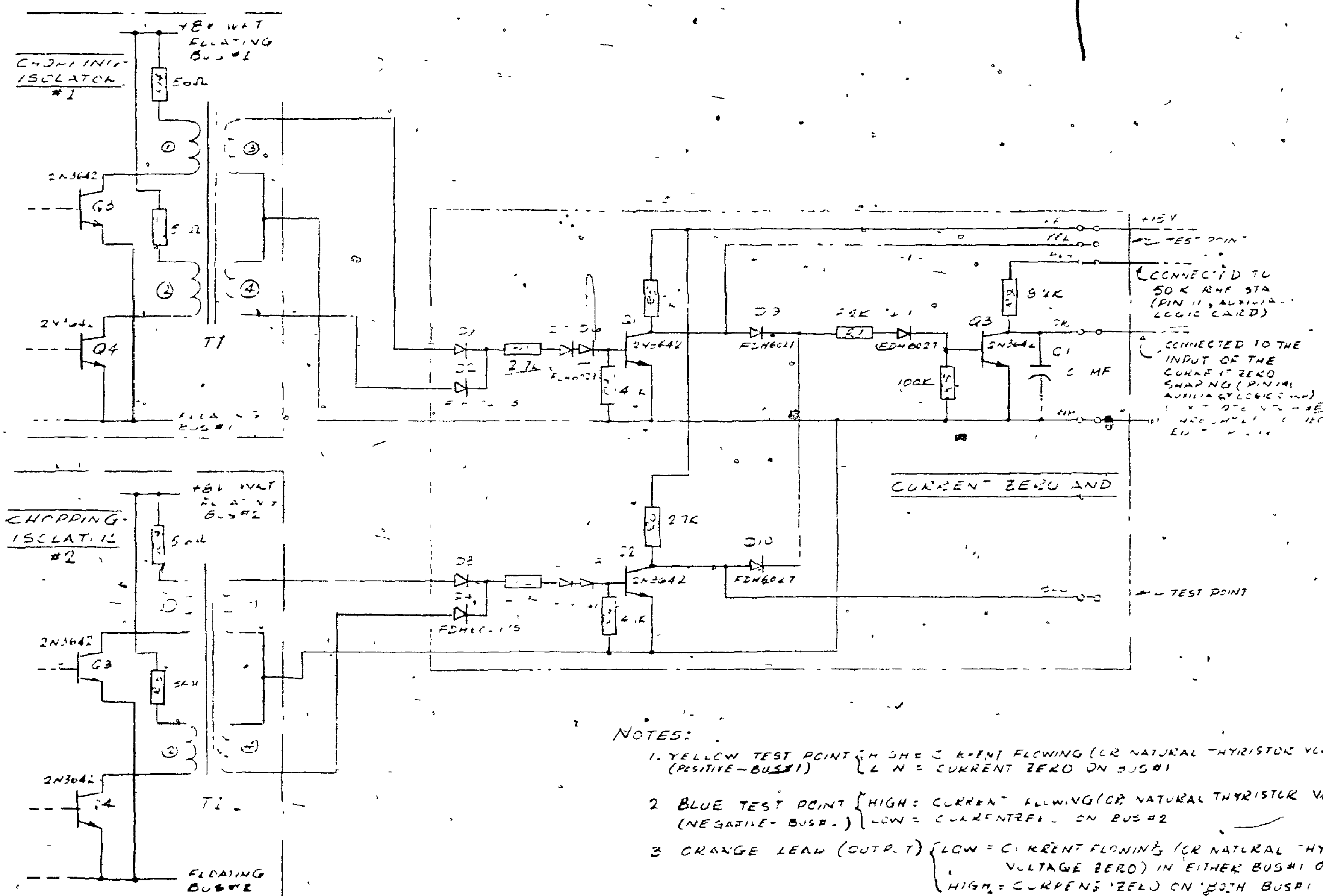


PLATE 11.

CURRENT ZERO "AND"

NOTES:

1. YELLOW TEST POINT (POSITIVE – BUS#1) { HIGH = CURRENT FLOWING (OR NATURAL THYRISTOR VOLTAGE ZERO) ; LOW = CURRENT ZERO ON BUS#1

2. BLUE TEST POINT (NEGATIVE – BUS#2) { HIGH = CURRENT FLOWING (OR NATURAL THYRISTOR VOLTAGE ZERO) ; LOW = CURRENT ZERO ON BUS#2

3. ORANGE LEAD (OUTPUT) { LOW = CURRENT FLOWING (OR NATURAL THYRISTOR VOLTAGE ZERO) IN EITHER BUS#1 OR BUS#2 ; HIGH = CURRENT ZERO ON BOTH BUS#1 AND BUS#2

4. THE 50K RHEOSTAT IS USED TO ADJUST THE CHARGING RATE OF CAPACITOR C1, THEREBY CONTROLLING THE DELAY BETWEEN A CURRENT ZERO OCCURRING ON BOTH BUSES #1&2 AND THE VOLTAGE ON PIN 12 (AUX LOGIC CARD [illegible]

PLATE 12.

AUXILIARY LOGIC CARD

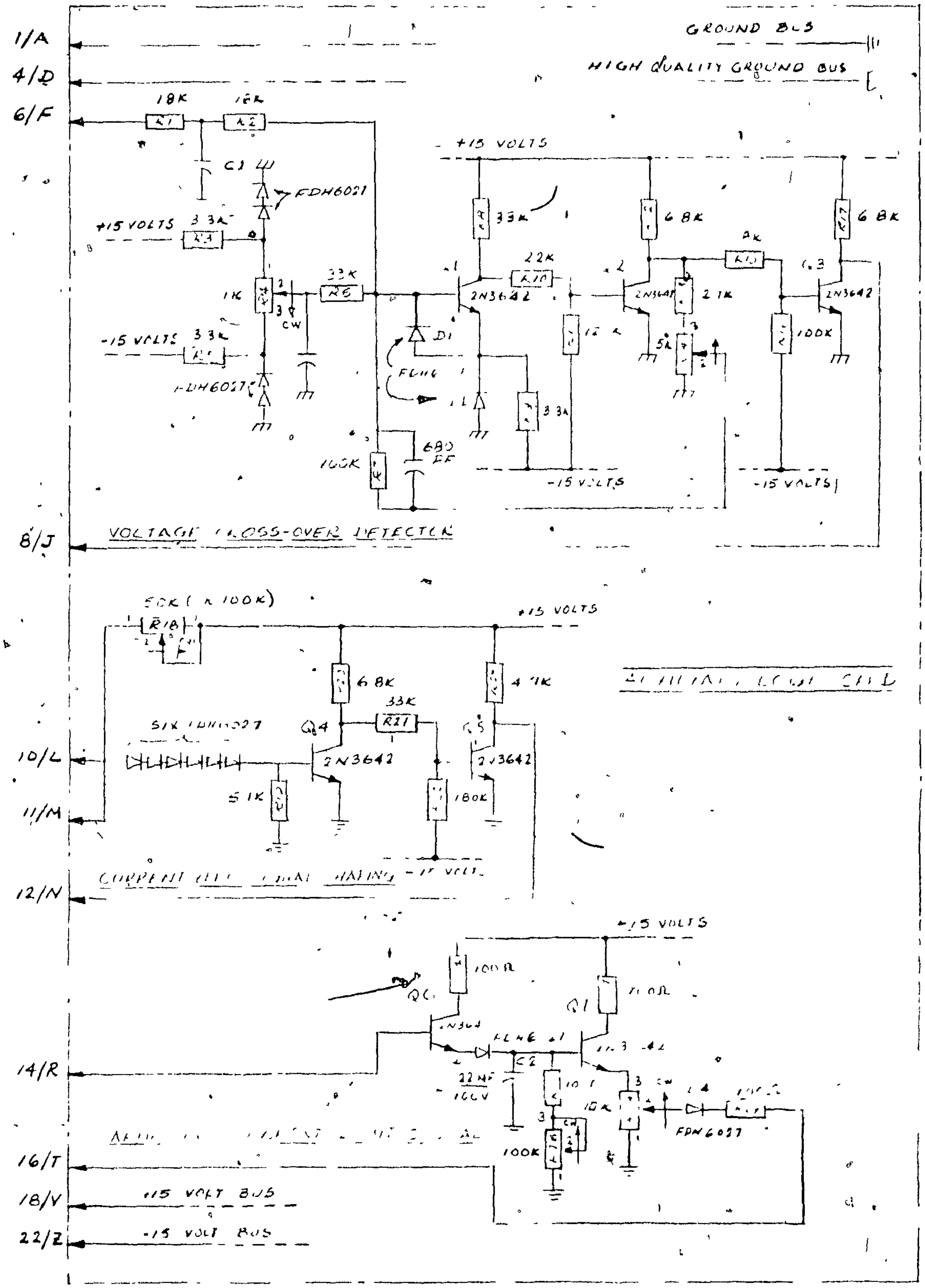


PLATE 13.

CROSSOVER LOGIC INTERCONNECTIONS FOR
TWO CONVERTERS WITH A RESISTIVE OR LAGGING LOAD

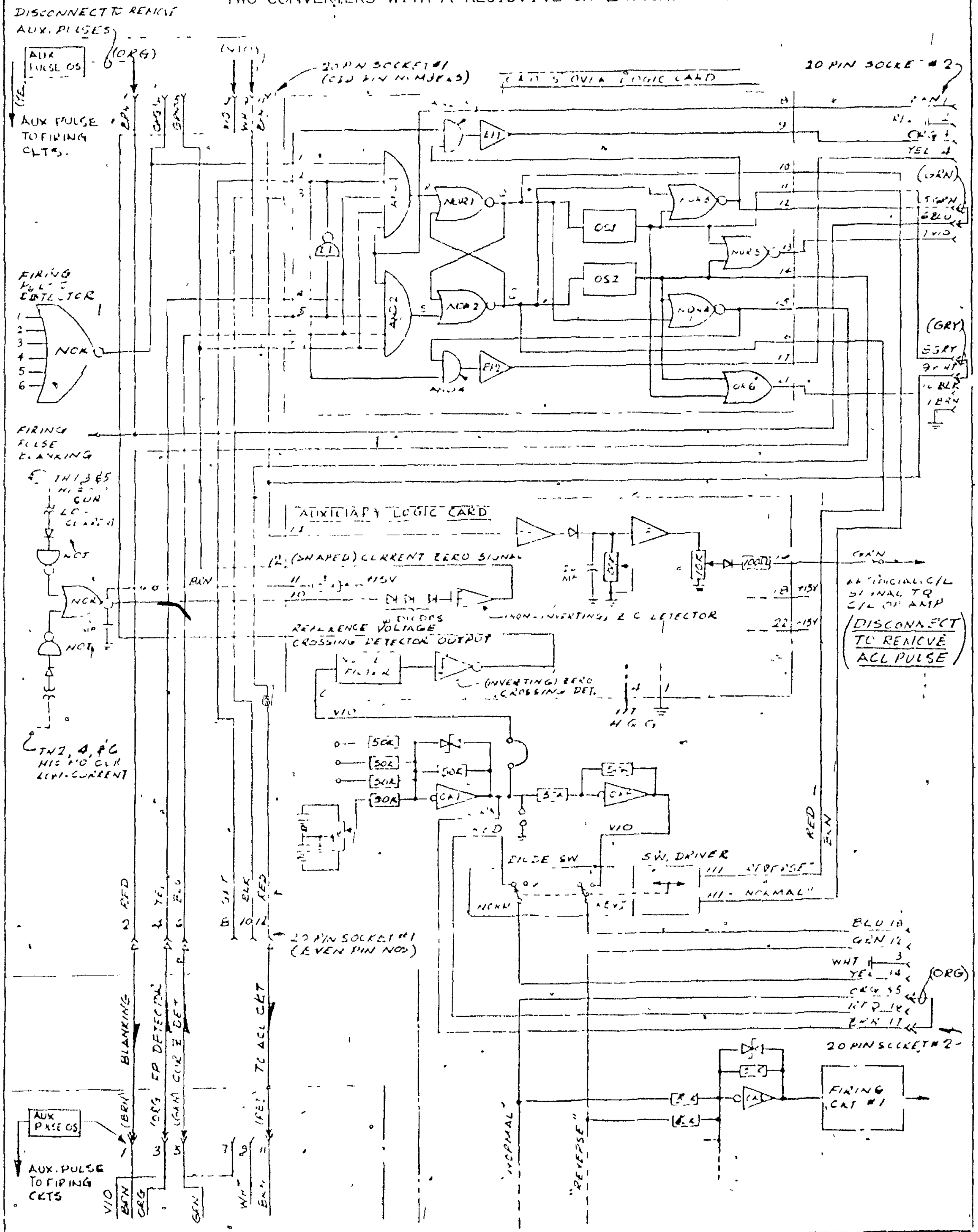


PLATE 14.

SCHEMATIC DIAGRAM OF THE CROSSOVER LOGIC CARD
FOR RESISTIVE OR LAGGING LOAD

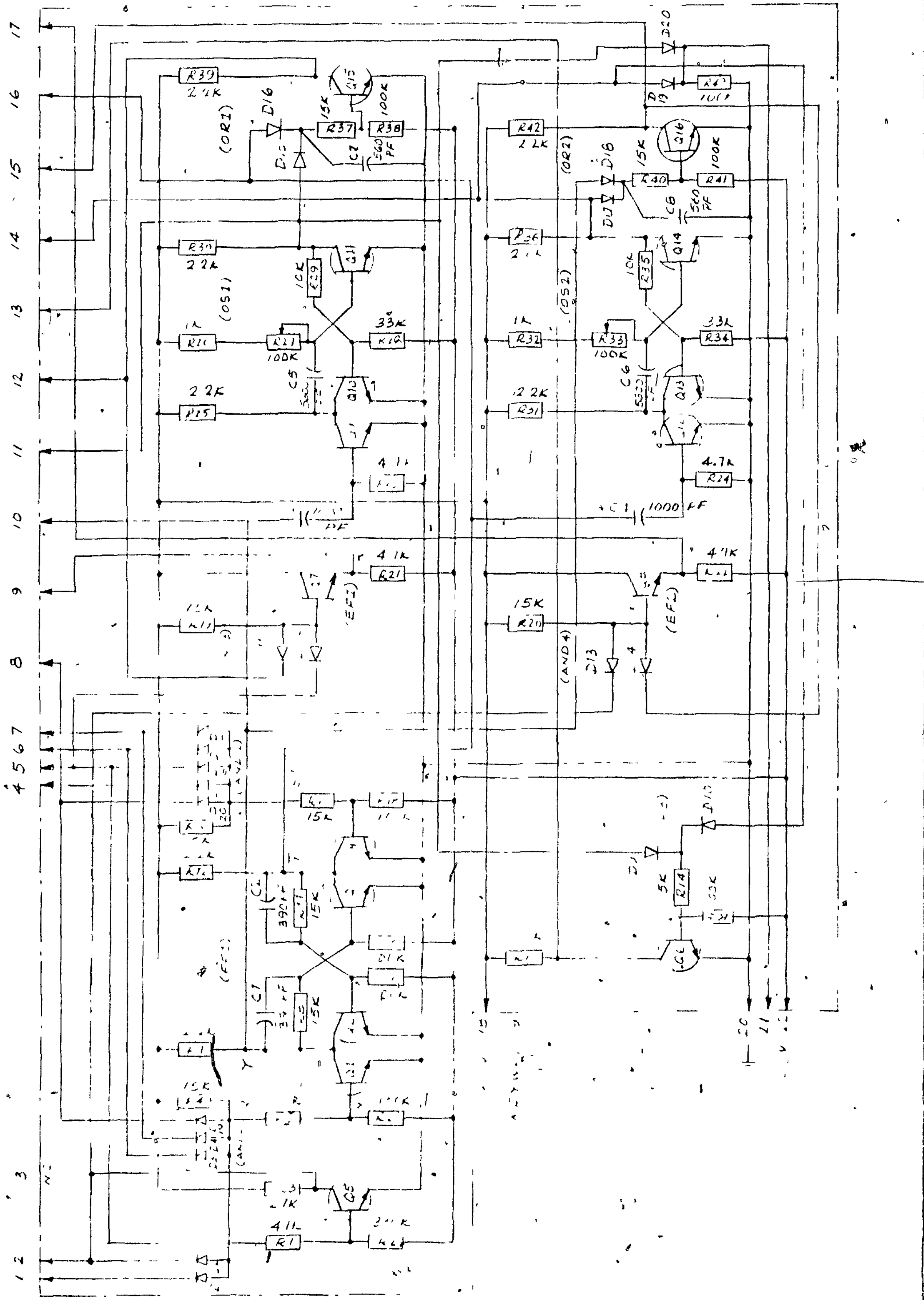


PLATE 15.

CROSSOVER LOGIC INTERCONNECTIONS FOR AN ARMATURE SUPPLY WITH ACL PULSES TO PREVENT ARMATURE CURRENT SURGES.

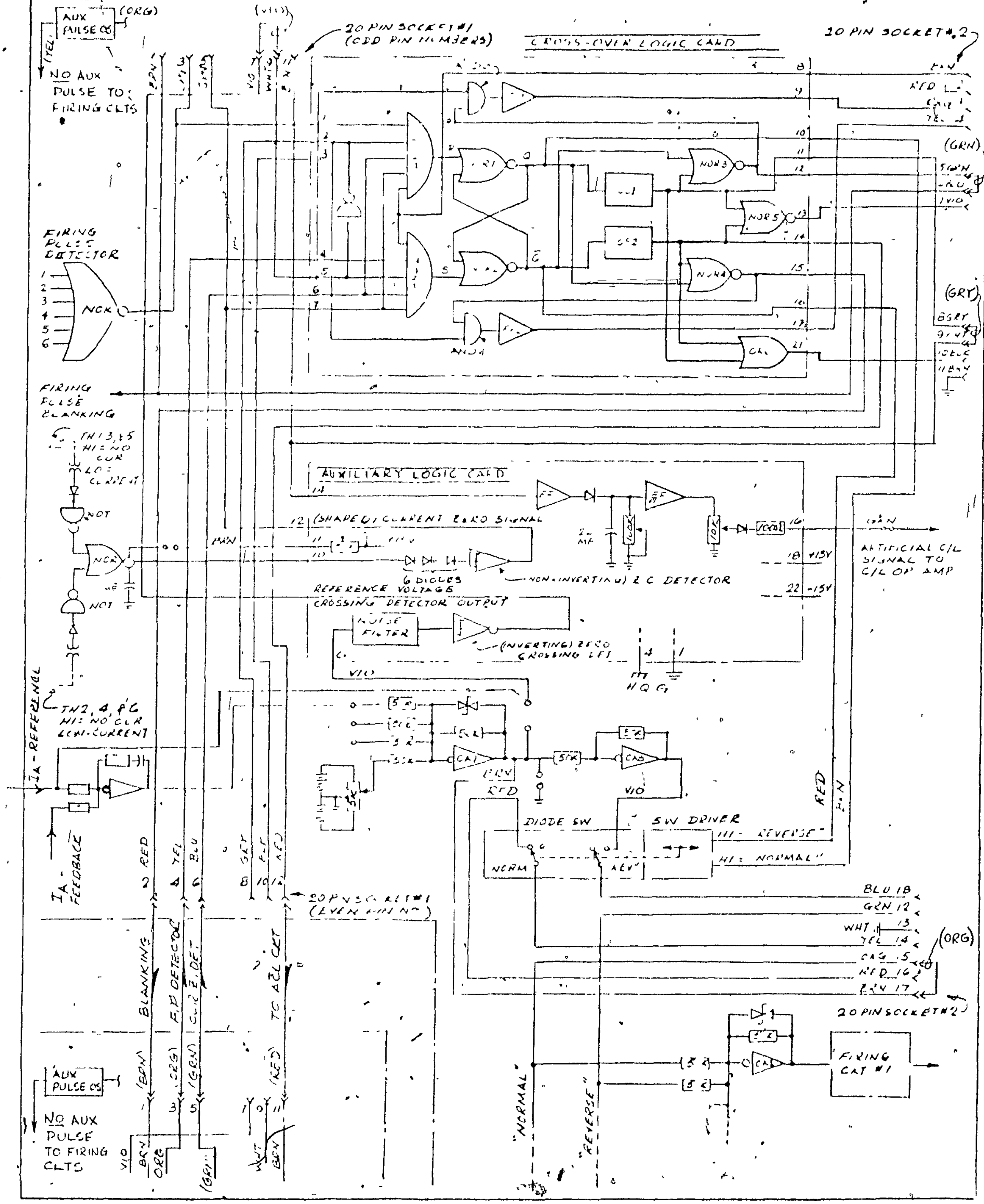


PLATE 16.

CROSSOVER LOGIC INTERCONNECTIONS FOR AN ARMATURE SUPPLY WITH DEADBAND BETWEEN THE CONVERTERS TO PREVENT ARMATURE CURRENT SURGES.

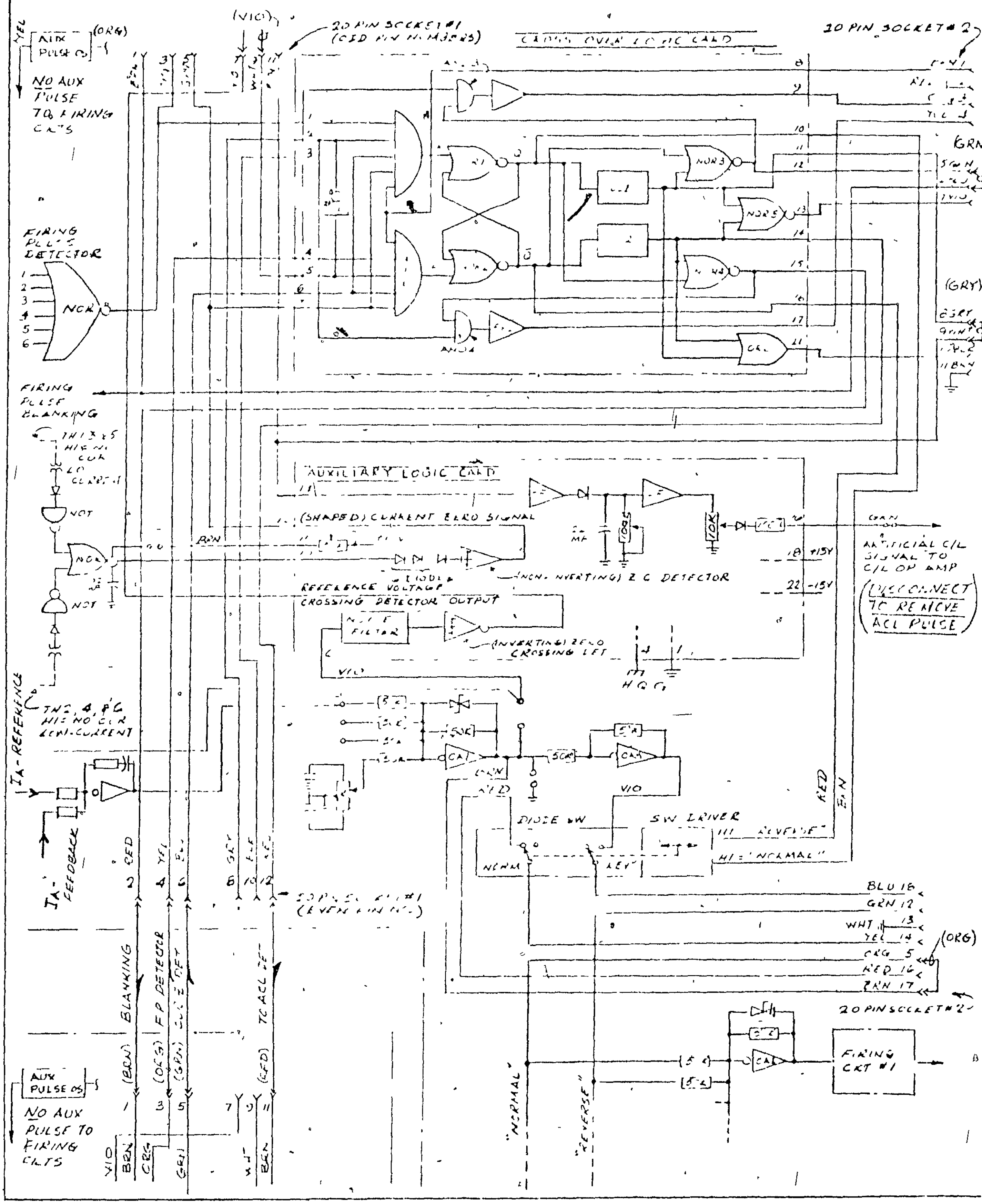


PLATE 17.

POWER FACTOR INDEPENDENT CROSSOVER LOGIC CARD

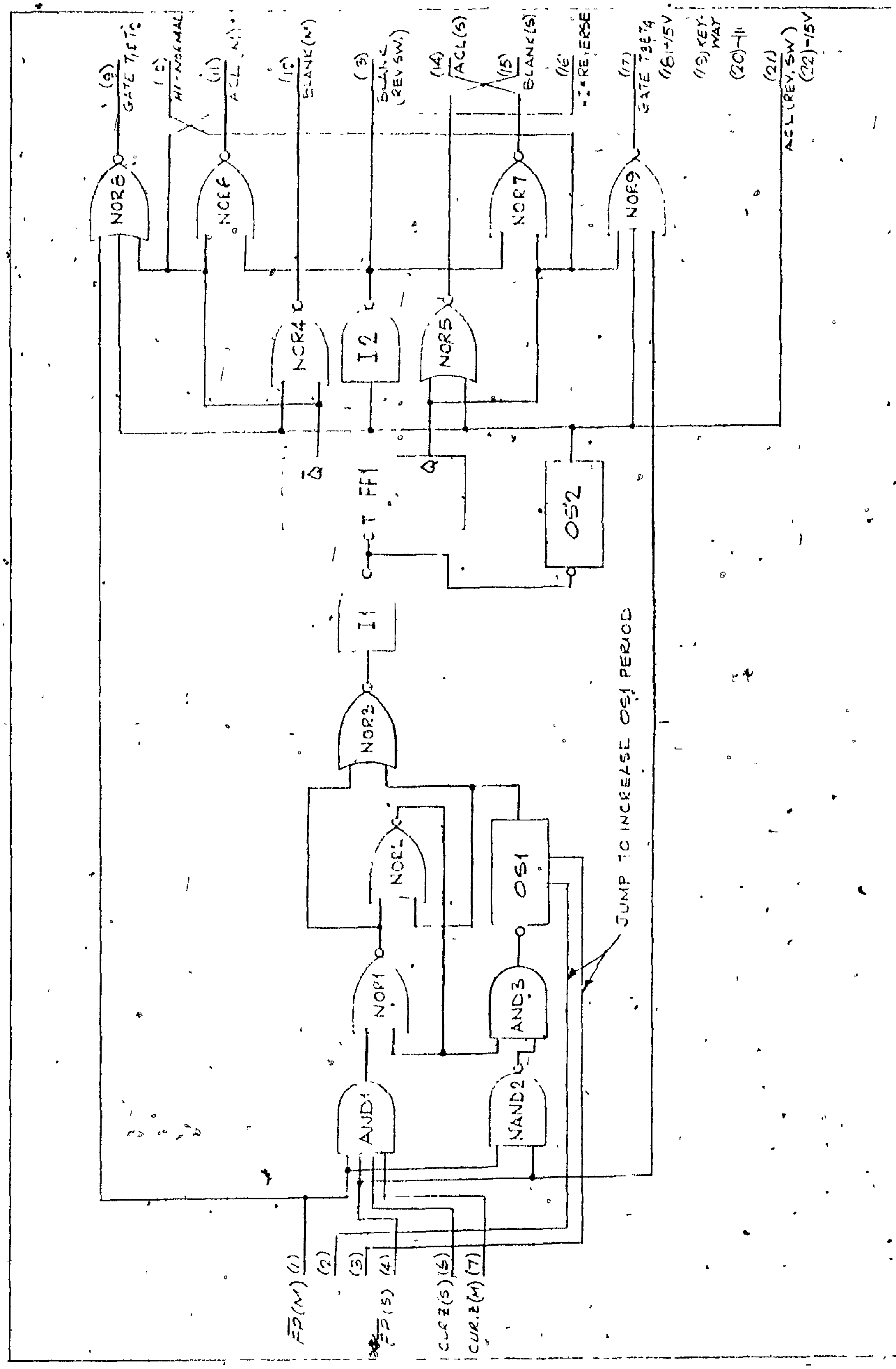


PLATE 18.

CROSSOVER LOGIC INTERCONNECTIONS FOR USING ONE CONVERTER AND A FOUR THYRISTOR REVERSING SWITCH AS A CYCLOCONVERTER

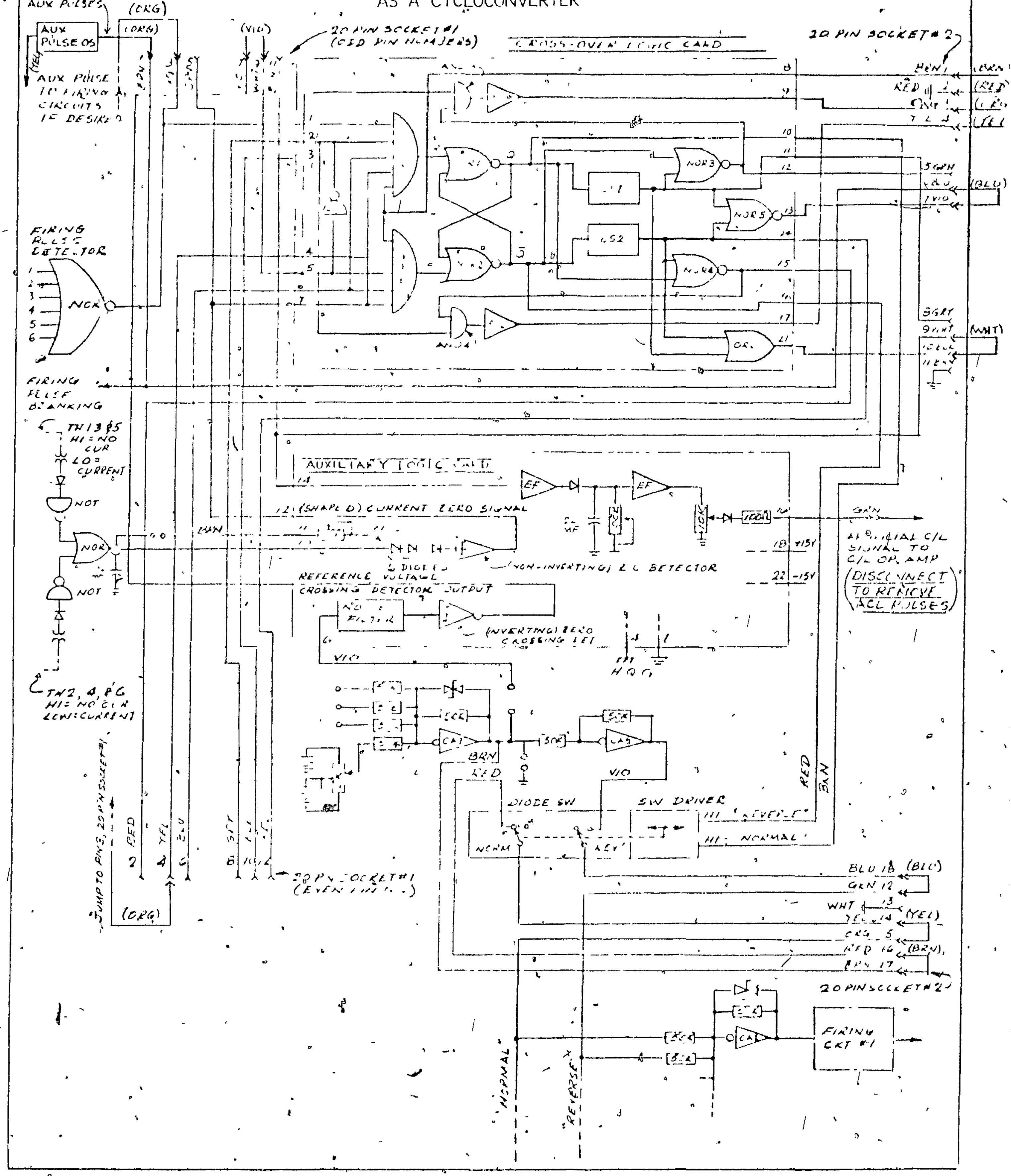


PLATE 19.

ANALOG SIGNAL DIODE SWITCHES AND DRIVERS.

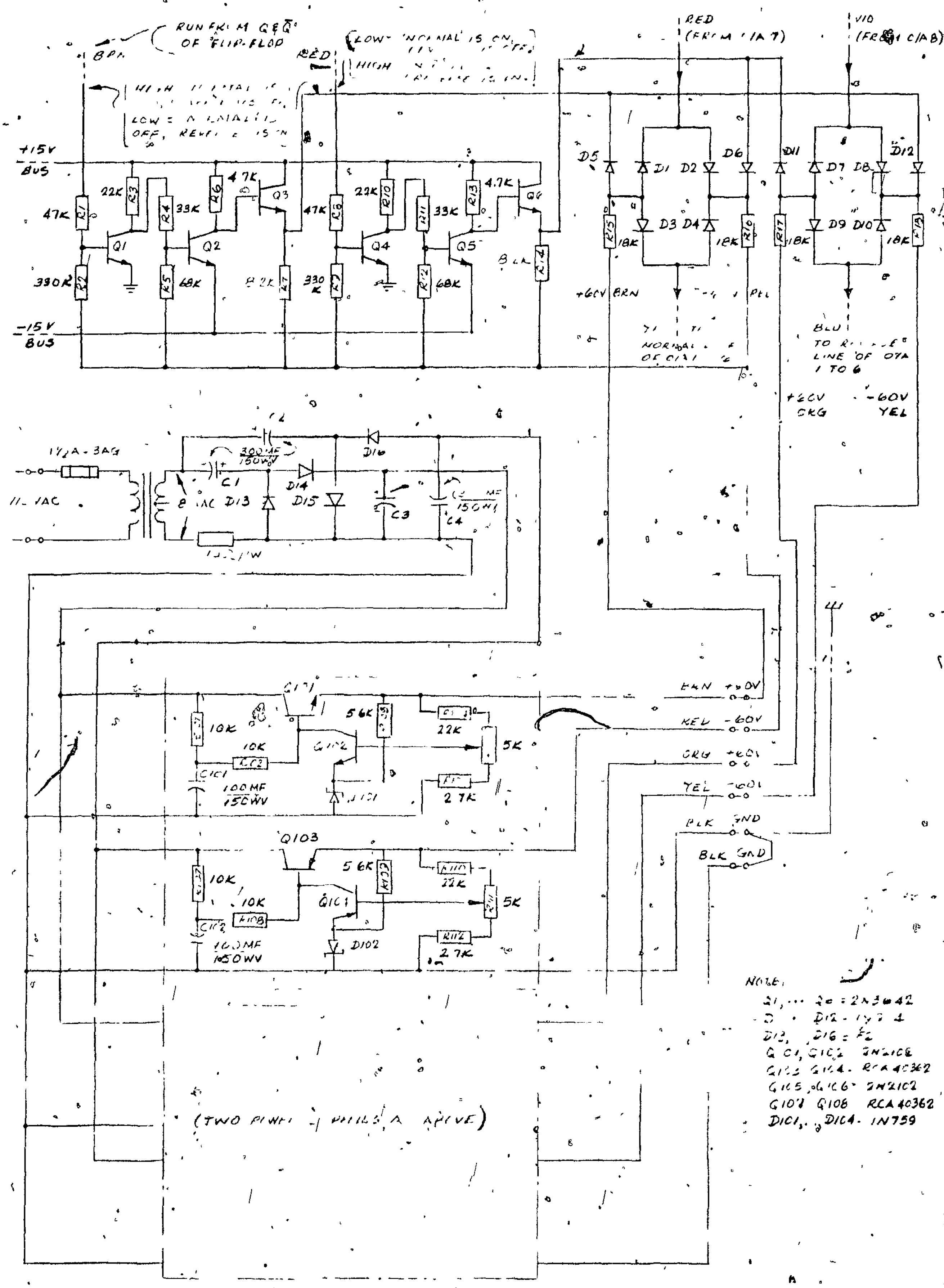
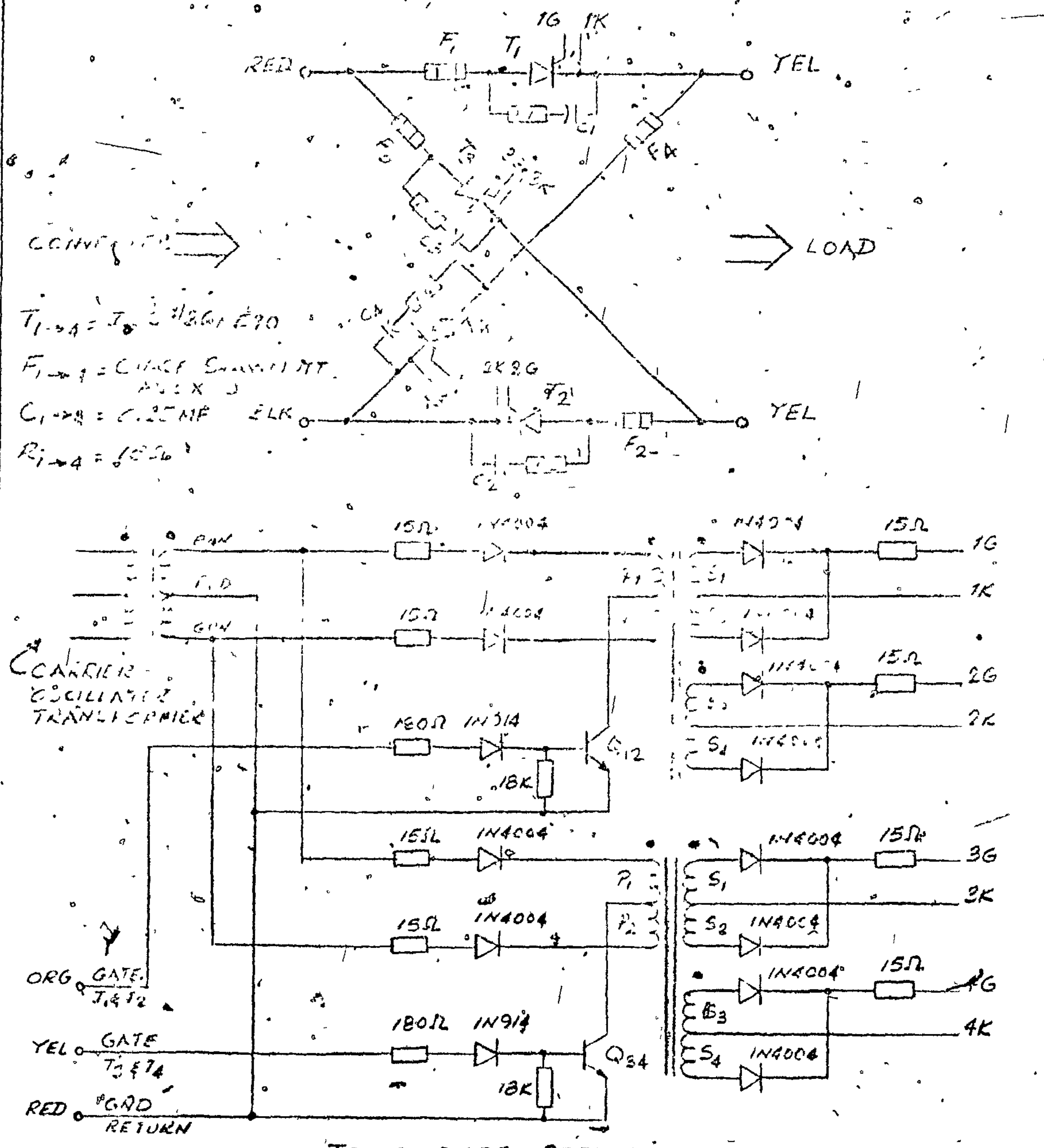


PLATE 29. FOUR THYRISTOR REVERSING SWITCH



TRANSFORMER DETAILS:

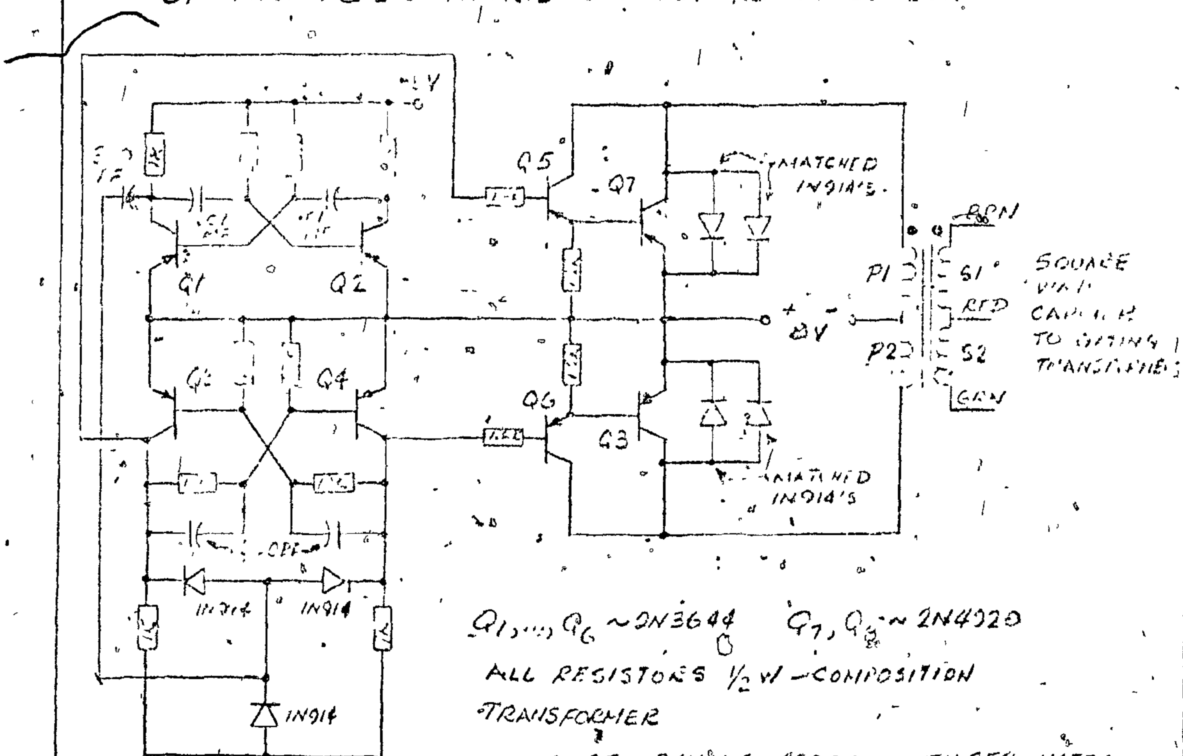
CORE ~ PHILLIPS K300500 WITH 3E2 MATERIAL.

WINDINGS ~ P1, P2, ETC 30T BIFILAR #26 CU WITH NYTHERM INSUL.

INSULATION ~ 2 LAYERS SCOTCH ELECTRICAL TAPE OVER CORE & BETWEEN WINDINGS

PLATE 21.

CARRIER OSCILLATOR FOR CONTINUOUS GATING OF THE FOUR THYRISTOR REVERSING SWITCH

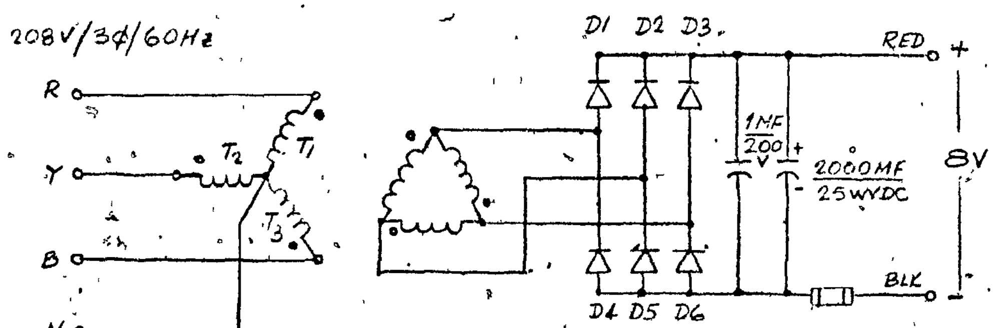


$Q_1, \ldots, Q_6 \sim$ 2N3644 $Q_7, Q_8 \sim$ 2N4920

ALL RESISTORS ½ W ~ COMPOSITION

TRANSFORMER

CORE ~ PHILLIPS K300500 WITH 3F2 MATERIAL.
WINDINGS ~ P_1, P_2 AND S3, S4 ARE 30 TURNS. QUADRIFILAR #26 CU WITH NYTHERM INSULATION.
INSULATION OVER CORE ~ 2 LAYERS OF SCOTCH ELECTRICAL TAPE

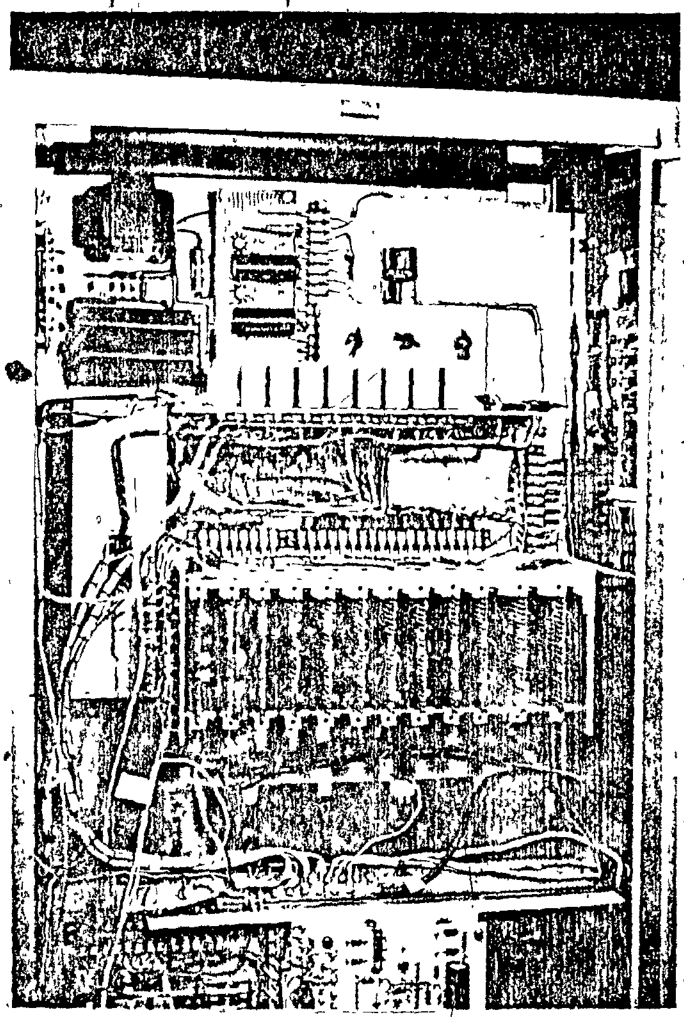


$T_1, T_2, T_3 \sim$ 110V:6.3V FILAMENT TRANSFORMERS
$D_1, \ldots, D_6 \sim$ ESK 1/10 DIODES — 1A/600PIV

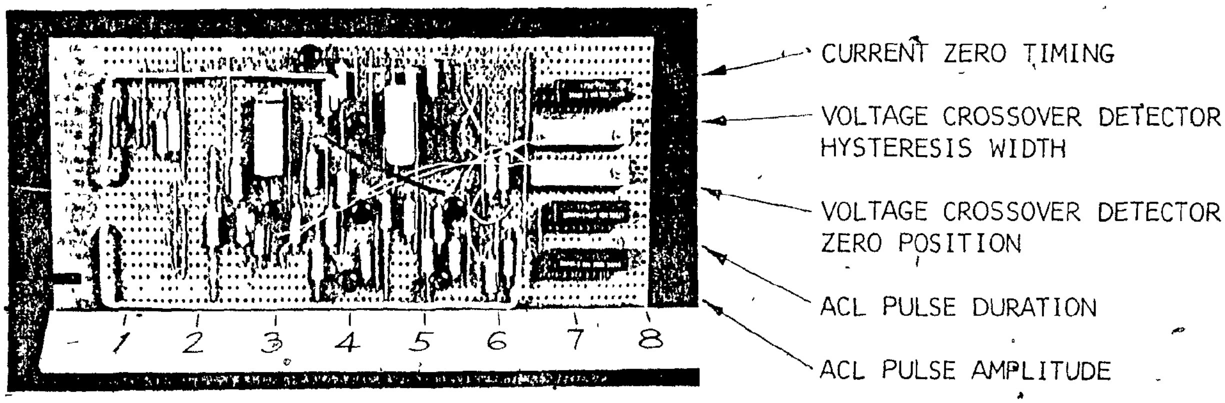
APPENDIX 2

EQUIPMENT PHOTOGRAPHS

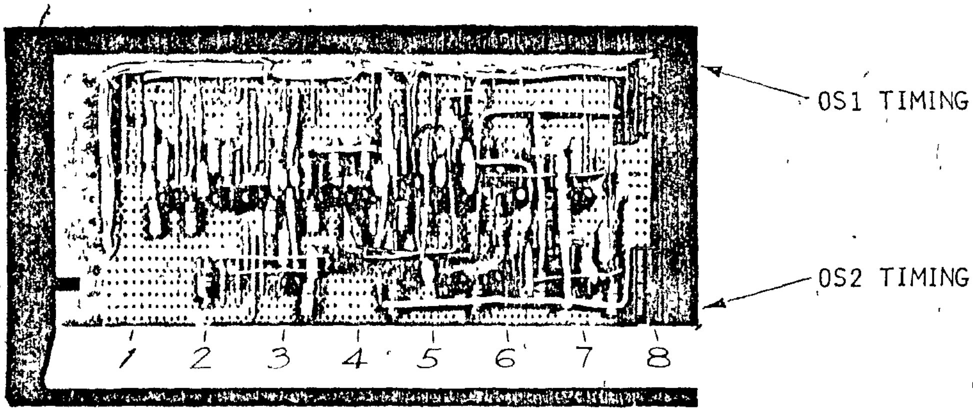
PHOTOGRAPH 1. GREEN CONVERTER-REAR VIEW



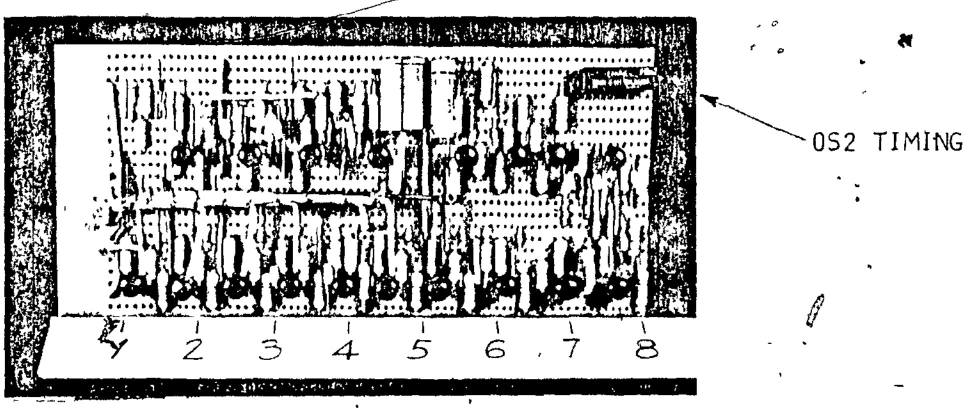
PHOTOGRAPH 2. AUXILIARY LOGIC CARD



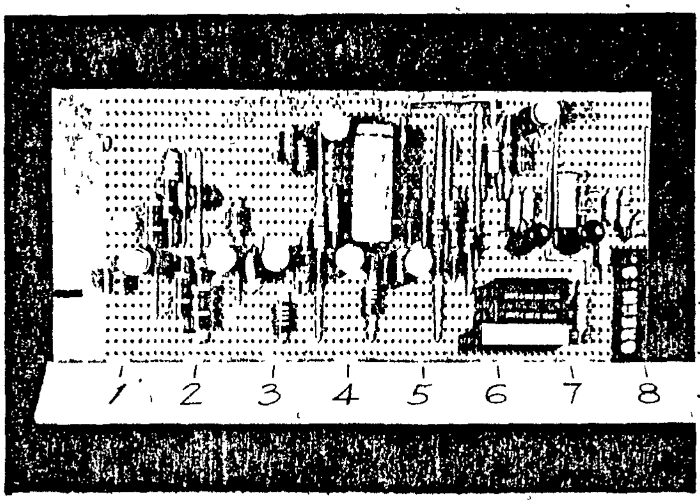
PHOTOGRAPH 3. CROSSOVER LOGIC CARD SUITABLE FOR UNITY AND LAGGING PF LOADS



PHOTOGRAPH 4. PF INDEPENDENT CROSSOVER LOGIC CARD



PHOTOGRAPH 5. FIRING CIRCUIT CARD

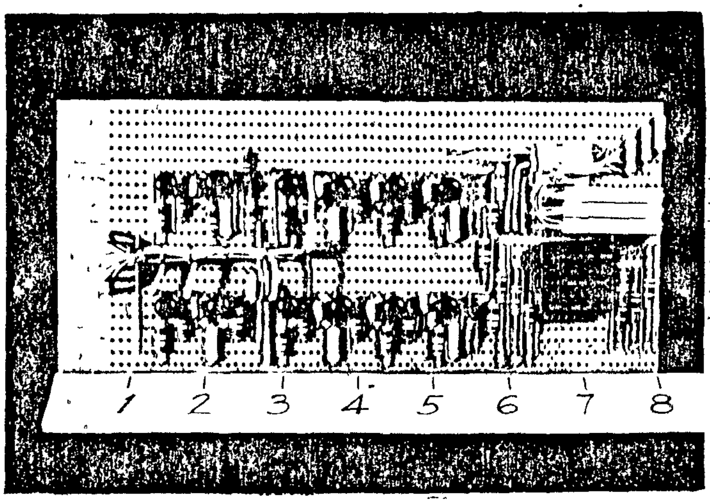


FIRING PULSE WIDTH

SCHMITT TRIGGER HYSTERESIS

SCHMITT TRIGGER ZERO

PHOTOGRAPH 6. ALPHA BLANKING CARD



COS(#1-30°)

COS(#2-30°)

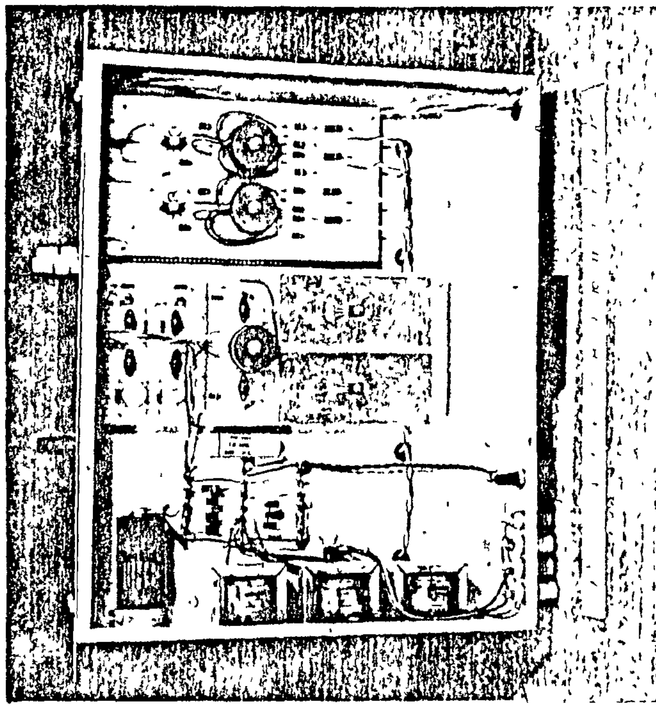
COS(#3-30°)

ZERO #1

ZERO #2

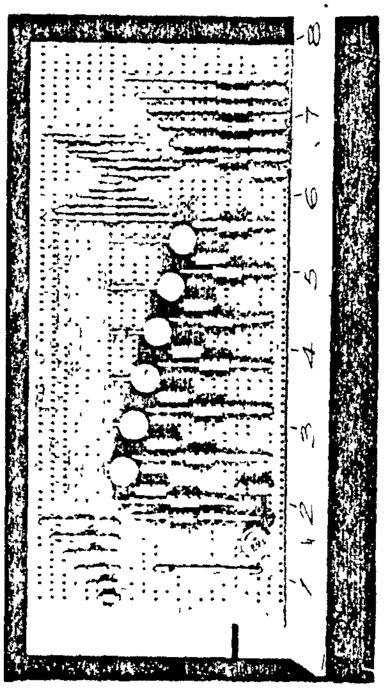
ZERO #3

PHOTOGRAPH 7. FOUR THYRISTOR REVERSING SWITCH
(BOTTOM VIEW)



PHOTOGRAPH 8.

DOUBLE PULSING OR CARD
BEFORE ADDING DELAY CIRCUITS



PHOTOGRAPH 9.

FLOATING VOLTAGE
MONITORING CARD