FABRICATION AND MEASUREMENTS ON METAL-SEMICONDUCTOR DIODES

by

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Master of Engineering.

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October, 1987.

ABSTRACT

Rectifying selenium diode structures have been made by evaporating metals on to a layer of crystallized selenium. These diodes were Al-Bi-Se-metal or Al-Te-Se-metal structures, where the metal was either Cd, Tl, Au or Bi. The highest forward current and lowest rectification ratio were observed with a Au counterelectrode, arising from its high work function. The highest rectification ratio was observed with Tl due to its low work function but Se-Tl diodes showed a degradation of rectification with time and post-fabrication heating. Barrier heights, obtained from capacitance Mott-Schottky plots, were found to decrease consistently with increase of metal work function and from this variation the density of interface states between the selenium and metal was estimated to be of the order of 10^{14} cm^{-2}. While the counterelectrode metal mainly controlled the current-voltage characteristics of the diodes, the back contact also had a detectable influence, in that a lower series resistance was found using polycrystalline tellurium as the back contact material in the place of bismuth. An anomalous capacitance minimum was observed in plots of capacitance against bias voltage in several diodes. In Se-Tl diodes, this anomalous capacitance dip occurred at a small forward bias, whereas in Se-Au and Se-Bi diodes, dips were also observed but near zero bias. Dispersion of capacitance and resistance in the diodes with frequency up to about 1MHz could be largely explained by

the depletion layer and capacitance and resistance contributions from the selenium itself.

Des diodes à redressement au sélénium ont été fabriquées par évaporation de métaux sur une couche de sélénium cristallisé. Ces diodes avaient une structure Al-Bi-Se-métal ou Al-Te-Se-métal, où le métal était soit du Cd, du Tl, de l'Au ou du Bi. Les plus hautes valeurs de courant direct et les plus faibles rapports de redressement ont été observés avec une contre-électrode en or; cela est dû à la haute fonction de travail de l'or. C'est le Tl qui a fourni le rapport de redressement le plus élevé, grâce à sa fonction de travail moins élevée; mais les diodes au Se-Tl montrent une dégradation de redressement avec le temps ou lorsqu'elles sont exposées à la chaleur, après fabrication. On a constaté que les hauteurs de barrière, déterminées par des tracés de capacité de Mott-Schottky, décroissaient en fonction de l'augmentation de la fonction de travail du métal; à partir de cette variation, on a estimé que la densité des états d'interface entre le sélénium et le métal était de l'ordre de 10^{14} cm^{-2}. Si le métal de la contre-électrode contrôlait surtout les caractéristiques de courant-tension des diodes, le contact arrière avait également un effet détectable: nous avons constaté que la résistance série était plus faible lorsque l'on utilisait du tellure polycristallin à la place du bismuth, comme matériau de contact arrière. Un minimum de capacité anormal a été observé dans les tracés de la capacité par rapport à la tension de polarisation, dans plusieurs diodes. Dans les diodes au Se-Tl, ce creux de capacité se produisait à de faibles valeurs de tension directe, alors que dans les diodes au Se-Au et au Se-Bi, des creux ont également été observés, mais à une tension presque nulle. La dispersion de la capacité et de la résistance dans les diodes en fonction de la fréquence, jusqu'à environ 1MHz, pourrait en grande partie être due à la couche de transition, et à l'effet que le sélénium lui-même exerce sur la capacité et la résistance.

ACKNOWLEDGEMENTS

The author wishes to express his sincere gratitude to his supervisor, Dr. C. H. Champness, for his patient guidance and assistance throughtout this study.

The help of Mr. J. Foldrari and the staff of the mechanical workshop at the Department of Electrical Engineering in preparing mechanical parts in this work is greatly appreciated.

Special thanks are also due to Mr. Y. F. Go for his help in computation of experimental results.

The author is specially thankful to his parents for their support and encouragement.

The financial support of this work by the Natural Science and Engineering Research Council of Canada is gratefully acknowledged.

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CHAPTER 1

INTRODUCTION

Selenium is a very important photoreceptor material used extensively in the dry photocopying industry. For these applications, the material is used in the amorphous form. The application of selenium in the trigonal crystalline form is much less extensive, but this form is very interesting scientifically because it is always p-type and it has the highest reported work function among all the elements (see Fig. 1.1) [1]. This means, in principle, that Schottky junctions with varying barrier heights can easily be fabricated by deposition of metals on crystalline selenium because all metals have a smaller work function than selenium.

Arising from previous work done in the Solid State Laboratory at McGill University [2] [3], the present research program was undertaken. This has consisted of fabricating Se-metal diodes and investigating their electrical characteristics, involving measurements of current as function of voltage and capacitance and resistance as a function of voltage and frequency on the diodes. Cadmium was one of the counterelectrode materials used in the structures studied, since this metal was employed as the major constituent in the counterelectrodes of commercial selenium rectifiers. Diodes with bismuth, gold and thallium were also

investigated. Gold has a relatively high work function, while thallium has a relatively low value, so that these metals would be expected ideally to yield Schottky junctions with a low and a high barrier height respectively, which turns out to be the case. As will be seen, Se-Tl diodes are excellent rectifiers and even better than Se-Cd diodes. However, their performance falls off rapidly with time. Some results were obtained on a few diodes using monocrystalline selenium.

The structure of the thesis is as follows. In chapter 2, a brief review is given of the theory of the Schottky junction and of the effect on barrier height of interface states. Chapters 3 and 4 describe respectively the preparation of the samples and the methods of measurement. The experimental results obtained on the diodes are given in chapters 5, 6 and 7. These results are comprehensively discussed in chapter 8 and the over-all conclusions are given in chapter 9.

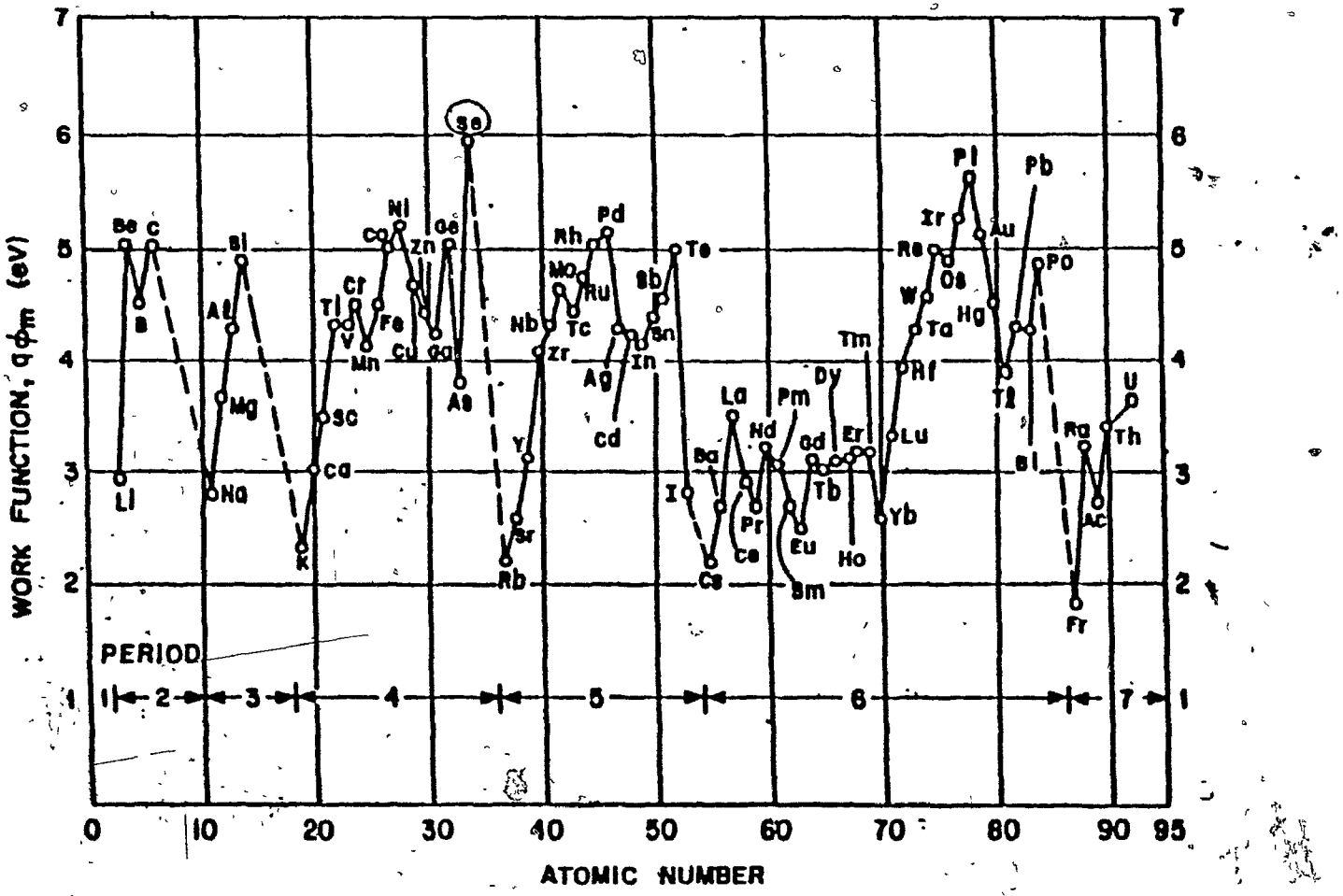

Fig. 1.1 Metal work function for a clean metal surface in a vacuum versus atomic number [1].

CHAPTER 2

THEORETICAL CONSIDERATIONS

2.1 Introduction

This chapter briefly reviews the basic theory of metal-semiconductor contacts relevant to this project. A simple band diagram is presented to illustrate a Schottky barrier. The current transport mechanisms, capacitance-voltage characteristics and the effect of surface states are also treated briefly. More detailed treatments of the Schottky junction are, however, given in various texts [4] [5] [6].

2.2 Schottky Barrier for a P-type Semiconductor

When a metal and a p-type semiconductor are brought into contact (Fig. 2.1), a redistribution of charge occurs. If the work function of the metal (ϕ_m) is smaller than that of the semiconductor (ϕ_s), then electrons flow from the metal into the semiconductor. A final equilibrium condition is reached when the Fermi levels of the two substances are lined up (Fig. 2.2). Under the assumption of the absence of an interfacial layer and surface states, a potential barrier for holes is formed with a height (ϕ_{bp}), as seen from the metal side of the contact, given by :

$$\phi_{bp} = \frac{E_G}{q} + \chi_s - \phi_m \qquad (2.1)$$

where, E_G is the energy band gap of the semiconductor, q is the magnitude of a unit electron charge and χ_s is the electron affinity of the semiconductor.

2.3 Current Transport Mechanisms

Current transport in metal-semiconductor contacts is mainly due to majority carriers, i.e., electrons for an n-type and holes for a p-type semiconductor. Theoretically, there are four basic transport mechanisms under forward bias [4]. They are

(1) transport of majority carriers from the semiconductor over the potential barrier into the metal (the dominant process for Schottky diodes with moderately doped semiconductors),

(2) quantum-mechanical tunnelling of holes through the barrier (especially for a heavily doped semiconductor),

(3) recombination in the space-charge region and

(4) minority carrier injection from the metal to the semiconductor.

In this project, selenium was used, which is always p-type and moderately doped, so that the Schottky diode was a majority-carrier device under low-injection condition (small bias). Therefore, only the first process is concerned here.

There are essentially two theories concerning the transport of holes over the barrier, namely, the thermionic

emission theory and the diffusion theory. The diffusion and thermionic emission processes act in series and the one, which creates the greater resistance, controls the current.

(a) Thermionic Emission Theory

For high mobility semiconductors, the transport is dominated by the thermionic emission theory. Under the assumptions [5] that

(1) the barrier height ϕ_{bp} is much larger than kT, where k is Boltzmann's constant and T is temperature,

(2) thermal equilibrium is established at the plane that determines emission and

(3) the existence of a net current flow does not affect this equilibrium,

the current density j_{th} as a function of forward potential V is :

$$j_{th} = A^* T^2 \exp\left(\frac{-q\phi_{bp}}{kT}\right)\left\{\exp\left(\frac{qV}{kT}\right) - 1\right\}$$
$$= j_{ST}\left\{\exp\left(\frac{qV}{kT}\right) - 1\right\},$$

where $j_{ST} = A^* T^2 \exp\left(\frac{-q\phi_{bp}}{kT}\right)$ is the saturation current density, $A^* = \frac{4\pi q m^* k^2}{h^3}$ is the effective Richardson constant for thermionic emission, h is Planck's constant and m^* is the effective mass of holes.

(b) Diffusion Theory

The diffusion theory can adequately describe the current transport for low mobility semiconductors under the assumptions [5] that

(1) the barrier is much larger than kT,

(2) the effect of hole collisions within the depletion region is included,

(3) the current concentrations at the contact interface in the depletion region are unaffected by current flow.

The current density equation is then given by :

$$j_d = \left(\frac{q^2 D_p N_V}{kT}\left[\frac{q(V_o - V)\ 2\ N_A}{\epsilon_s}\right]^{\frac{1}{2}} \exp\left(\frac{-q\phi_{bp}}{kT}\right)\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$= j_{SD}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] ,$$

where D_p is the diffusion ceofficient of holes, N_V is the effective density of states at the valence band, given by $N_V = \left(\frac{2\pi m_p kT}{h^3}\right)^{\frac{3}{2}}$, V_o is the diffusion potential, N_A is the acceptor impurity density (assumed to be uniform) and ϵ_s is the semiconductor permittivity.

The current density expressions of the diffusion and thermionic emission theories are basically of the same form, except that j_{SD} varies specifically with voltage, while j_{ST} is more sensitive to temperature.

2.4 Evaluation of Barrier Height from Capacitance-Voltage Measurements

According to Sze [5], there are basically four methods used to measure barrier height, namely, current-voltage characteristics, activation energy measurements, photoelectric measurements and capacitance-voltage (C-V)

measurements. The C-V method was used in this project and is briefly described as follows.

The depletion region of a Schottky barrier acts like a capacitor especially in reverse bias. The differential capacitance can be then expressed as [4] :

$$C = A \left(\frac{q\epsilon_s N_A}{2} \right)^{\frac{1}{2}} \left(V_o + V_R - \frac{kT}{q} \right)^{\frac{1}{2}} ,$$

where V_R is the reverse voltage and A is the area of the junction. This formula assumes a uniform concentration N_A of shallow acceptors in the semiconductor, which are fully ionized at room temperature, i.e. $p=N_A$, where p is the hole concentration.

Rearranging the above equation and neglecting the $\frac{kT}{q}$ term gives :

$$\left(\frac{A}{C} \right)^2 = \frac{2}{q\epsilon_s N_A} \left(V_o + V_R \right)$$

Thus, a plot of $(A/C)^2$ versus V_R will give a straight line with an intercept on the voltage axis of $V_R = -V_o$. From the slope, the acceptor concentration is given by :

$$N_A = \frac{2}{q\epsilon_s} \frac{\Delta V_R}{\Delta[(\frac{A}{C})^2]} \qquad (2.2)$$

Hence, both the diffusion potential V_o and N_A can be obtained from the plot. The Fermi level $E_{Fp} = E_F - E_V$ above the valence band is given by :

$$E_{Fp} = kT \ln \left(\frac{N_V}{N_A} \right) , \quad \text{since } p = N_A \qquad (2.3)$$

The barrier height can then be obtained according to Fig. 2.2 from :

$$\phi_{bp} = |V_o| + \left|\frac{E_{Fp}}{q}\right| \qquad (2.4)$$

2.5 The Effect of Interfacial States

All of the above theories are based on the assumption that there are no surface states. However, in reality, surface states arise because the surface of a crystal interrupts the perfect periodicity of the crystal lattice and because impurities and imperfections may be present. In general, the barrier height is determined not only by the metal work function alone, but also by the surface states, any thin interfacial oxide layer between the metal and the semiconductor, and the electric field applied across this layer. Arising from a treatment of assumed surface states, Cowley and Sze [7] have shown that the barrier height can be expressed as :

$$\phi_{bp} = \gamma \left(\frac{E_G}{q} + \frac{\chi_s}{q} - \phi_m \right) + (1 - \gamma)\phi_o - \alpha \epsilon_{max} , \quad (2.5)$$

where $\gamma = \left(1 + \frac{q\delta D_s}{\epsilon_i} \right)^{-1}$, $\alpha = \frac{\delta \epsilon_s}{\epsilon_i + q\delta D_s}$, ϕ_o is the neutral level of the interface states (see Fig. 2.3) above the valence band edge, D_s is the density of interface states per unit area per eV of band gap, ϵ_i is the dielectric constant of the oxide layer of thickness δ and ϵ_{max} is the maximum electric field across this layer. For small bias voltages, thin interfacial layer and moderate doping, the contribution of the last term of the above equation is so small that it

can be neglected [4]. Therefore, equation (2.5) is reduced to

$$\phi_{bp} = \gamma\left(\frac{E_G}{q} + \chi_s - \phi_m \right) + (1 - \gamma)\phi_o \quad , \quad (2.6).$$

If the density of states is negligible, i.e. $D_s \rightarrow 0$, ϕ_{bp} tends to the result of eqn. (2.1) $(E_G/q) + \chi_s - \phi_m$, which is called the Mott limit. However, if $D_s \rightarrow \infty$, ϕ_{bp} approaches ϕ_o, which is called the Bardeen limit. In this case the barrier height is totally dependent on interface states.

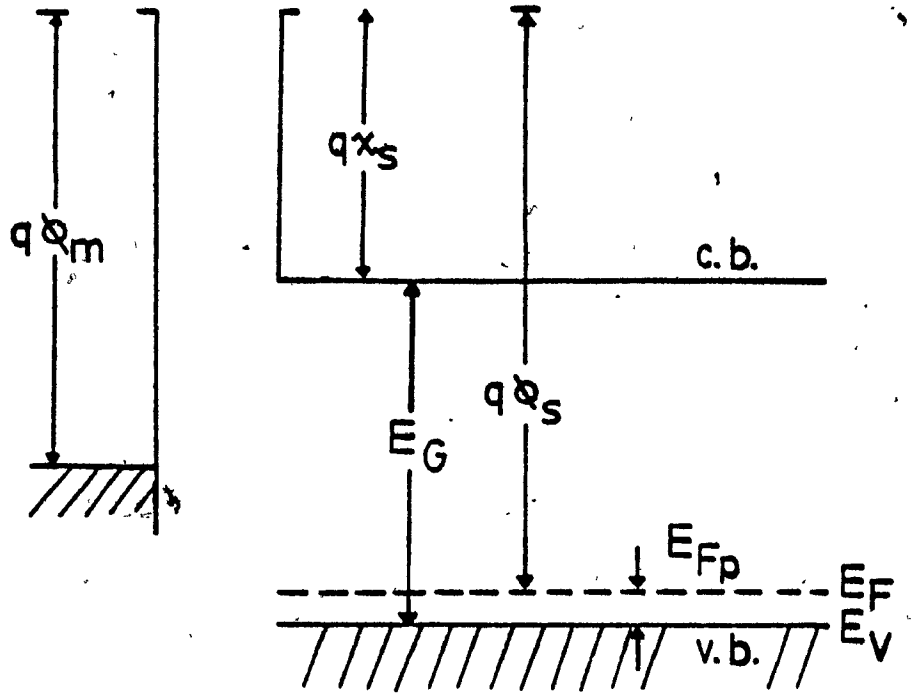

Fig. 2.1 Band diagram of a metal and a p-type semiconductor when neutral and isolated from each other.

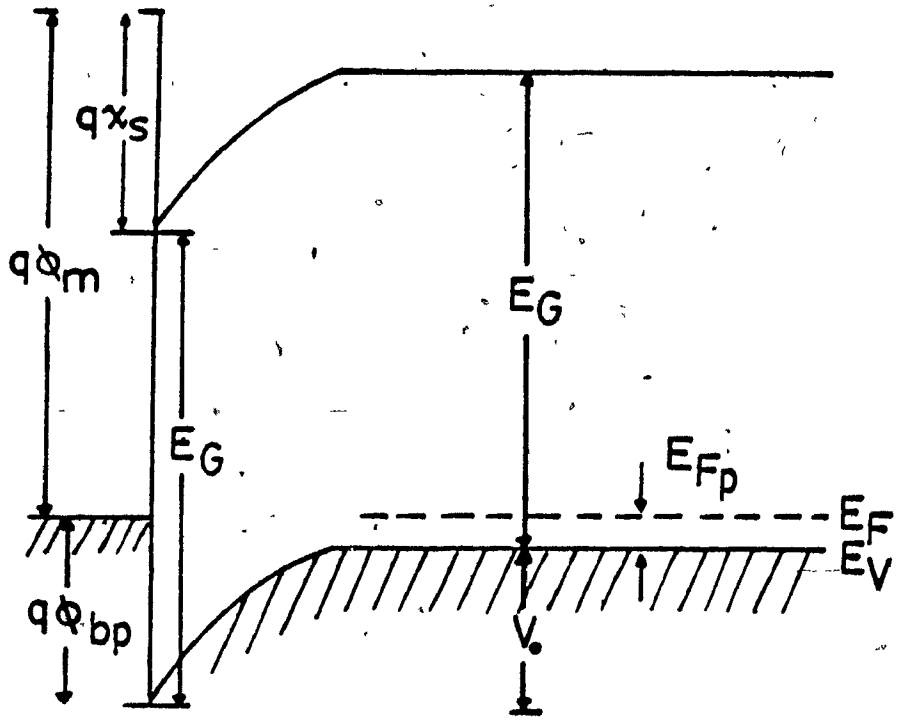

Fig. 2.2 Formation of a barrier between a metal and a p-type semiconductor in perfect contact.

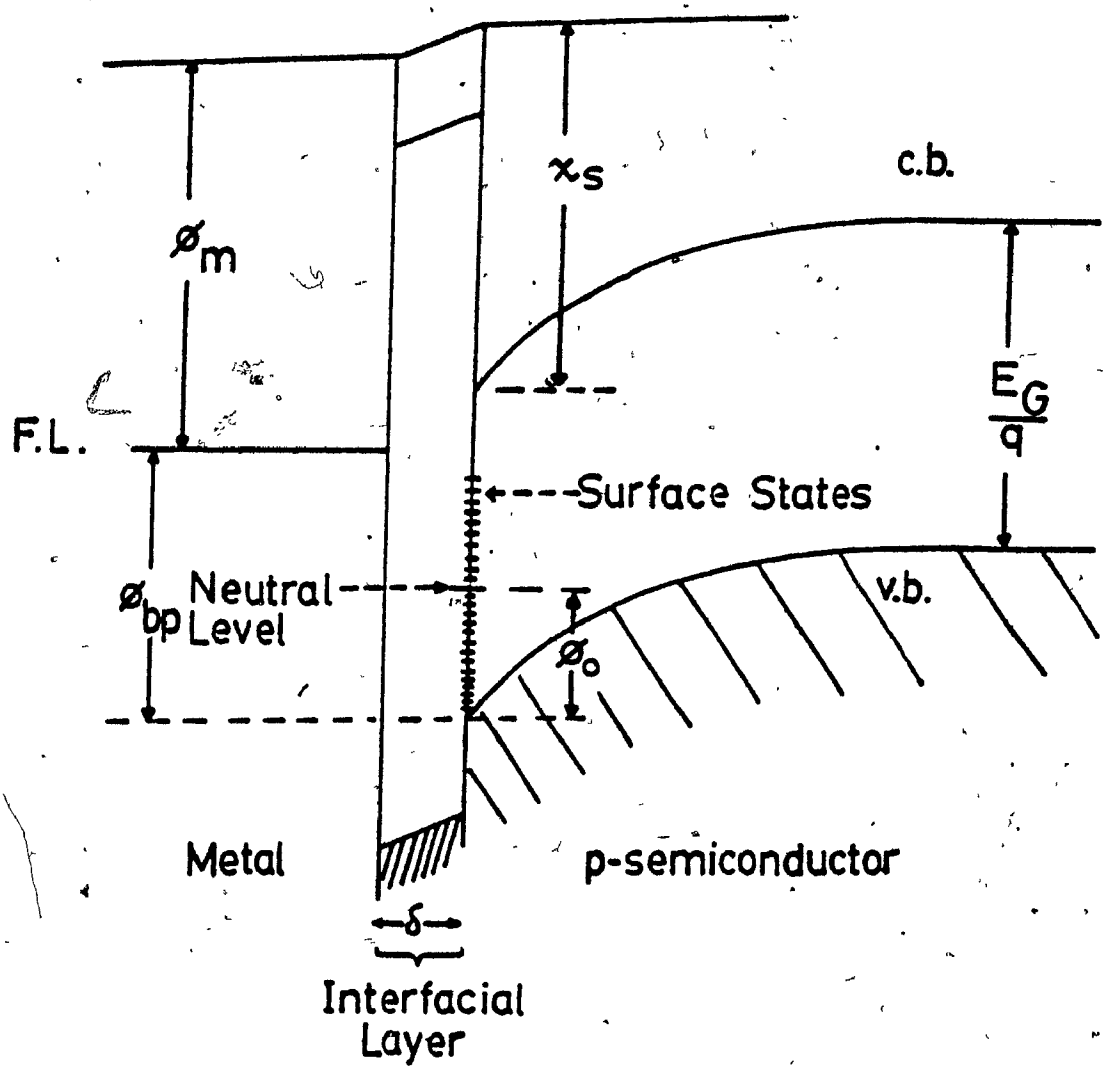

Fig. 2.3 Band diagram of a metal-p-type semiconductor contact with interface states associated with an interfacial layer.

CHAPTER 3

TECHNIQUES OF SAMPLE FABRICATION

3.1 Introduction

The procedures for fabricating selenium-metal Schottky diodes in the present studies are described in this chapter. The preparation of polycrystalline samples is first described, followed by the preparation of single crystal samples. Table 3.1 summarizes the fabrication details of all the structures prepared for study in this thesis.

3.2 Polycrystalline Structures

Fig. 3.1 shows a cross sectional view of a multi-layered polycrystalline structure, consisting of a contact material of either bismuth or polycrystalline tellurium, a selenium layer and a metallic counterelectrode material of either Cd, Tl, Bi or Au. These layers were all deposited in order on a polished cylindrical aluminum stud by evaporation in vacuum. Fine copper wires were finally soldered to the counterelectrodes to form the electrical contacts for measurement. Details of these processes are now given.

3.2.1 Substrate Polishing

The flat surface of a cylindrical aluminum stud was polished using 0.3 micron Emery paper (number 600) and then cleaned in alcohol. The stud was afterwards air-dried and loaded into a vacuum coater for the deposition of the back contact material.

3.2.2 Back Contact Material Deposition

Following the polishing of the aluminum stud, either bismuth or polycrystalline tellurium was deposited by evaporation.

(a) Bismuth

In this case, the stud was loaded into an Edwards Model 6E4 6-inch vacuum coater, which was pumped down to a pressure of about 10^{-4} torr. Bismuth was then evaporated on to the surface of the stud by passing a current of 30-35 amperes through a molybdenum boat containing three pellets of bismuth for about 5-7 minutes. After this, the stud was allowed to cool down in vacuum for about 30 minutes and then removed from the system.

(b) Polycrystalline Tellurium Film

In the case where Te was required for the back contact, the polished aluminum stud was mounted in a 12-inch Edwards Model E12E3 vacuum system, which was subsequently pumped down to a pressure of 10^{-5}-10^{-6} torr. The tellurium source, which was located about 10 cm below the aluminum substrate and covered by a shutter, was heated to about 425°C and stablized at this temperature for 5 minutes. Then the

temperature was raised to about 450°C and the shutter opened, so that deposition could take place. After evaporating for 5 minutes, the shutter was closed. The substrate was allowed to cool down for about 1 hour and removed from the vacuum system for further preparation.

3.2.3 Selenium Deposition

The substrate, coated with either bismuth or tellurium, was next mounted in a 12-inch Edwards evaporation system Model E12E3. The selenium source was located 10 cm below the sample, covered by a shutter and the system was pumped down to a pressure of 10^{-5}-10^{-6} torr. The sample was then heated to 100-130°C using a temperature controlled substrate heater and stablized at this temperature for two hours. After this, the selenium source was heated to 200°C and stablized at this temperature for 15 to 20 minutes to prevent the initial vapour arising from the bubbling of the melted selenium from affecting the deposited film. The source temperature was then raised to 225-250°C and the shutter opened so that deposition could take place. After the required evaporation time, the shutter was closed and the power of the controller to the source was switched off. The substrate temperature was decreased gradually at a controlled rate of 0.5°C/min. to avoid the selenium film from peeling off the substrate, due to the difference in expansion coefficients. Finally, the substrate was cooled down to room temperature and removed from the vacuum system for the next steps.

3.2.4 Deposition of Counterelectrode Materials

(a) Cadmium, Thallium and Bismuth

For the deposition of cadmium, thallium or bismuth as counterelectrode, a metal mask with four circular apertures of diameter 0.42 cm was used (Fig. 3.2). The substrate, with its already deposited selenium film, was loaded, with the mask on the top of the film, into an Edwards Model 6E4 6-inch vacuum system. It was then pumped down for two hours and the metal was evaporated on to the selenium film by applying a current of 30 to 35 amperes for 5 minutes through a molybdenum boat containing 3 pellets of the required metal. The deposition time was controlled by an externally operated shutter between the source and the substrate. After the evaporation, the system was allowed to cool down for at least two hours before the sample was removed.

(b) Gold Deposition

For the deposition of gold, the setup was the same as described above, except that a tungsten filament was used instead of the molybdenum boat. Gold wire was cut into small pieces, each of which was bent into a V-shape and suspended on the tungsten filament. After the system had been pumped down for two hours, the gold was evaporated on to the selenium film by applying a current of 70 amperes for 5 minutes through the tungsten filament. Following the evaporation, the system was allowed to cool down for two hours, after which the sample was removed.

3.2.5 Electrical Contacts

The sample, with its successively deposited back contact material, Se and counterelectrode material, was mounted in a Teflon block with terminals in it. In most cases, fine copper wires were directly connected to the counterelectrode areas using Wood's metal as the solder, while the other ends of the wires were attached to the terminals in the Teflon block using normal electric solder. In some cases, Wood's metal was also evaporated with a mask containing apertures in desired shapes (stripes or circles) on each counterelectrode area. The procedure of evaporation was the same as described in the bismuth evaporation, except that the evaporation time was only 3 minutes. Following this, copper wires were soldered to the Wood's metal areas using Wood's metal itself, with the other ends attached to the terminals in the Teflon block. After soldering the wires, the sample was ready for measurement.

3.3 Single Crystal Structures

As indicated in Table 3.1, four samples were prepared with a monocrystalline selenium film grown epitaxially on a monocrystalline substrate of tellurium. Details of this process are given in reference [8]. Briefly, however, the procedure used here was as follows. A slice of single crystal tellurium from a Czochralski-grown monocrystal was

cut perpendicular to the c-axis and attached to the flat surface of an aluminum stud using silver epoxy resin. The resultant (0001) surface of the tellurium substrate was then polished chemically using a mixture of CrO_3, HNO_3 and H_2O [8]. This was continued until a shiny surface was obtained. The sample was then loaded into a 12-inch evaporation system for selenium deposition, following the same procedure described for the polycrystalline selenium samples. This was followed by the deposition of counterelectrode material and the soldering of electrical contacts, as described above. The monocrystallinity of the selenium film was checked by observation of characteristic microcrack patterns [8].

Table 3.1

Fabrication Details of the Se-Metal Structures

Structure	Sample No.	Selenium Deposition[1,2]			Remarks
		Source Temp. (°C)	Substrate Temp. (°C)	Evaporation Time (min.)	
Bi-Se-Cd	C20	220	110	20	3 Cd areas. Poor vacuum during Se deposition.
	C24	240	110	20	4 Cd areas. Poor vacuum during Cd deposition.
	C25	245	110	20	4 Cd areas. Se film heat-treated at 195°C for 24 hrs. in wet O_2 before Cd deposition
	C27	240	110	30	3 evap. Cd areas. 1 sput. Cd area for 20 min. 1 sput.area for 10 min.
	C29	245	140	30	4 Cd areas.
	C30	245	90	25	4 Cd areas.
	C33	240	80	25	4 Cd areas.
Poly Te-Se-Cd	C42	250	120	30	4 Cd areas.
Monocrystalline Te-Se-Cd	C50	250	150	30	Dots of Cd areas with diameter of 2 mm.
	C51	250	150	35	Dots of Cd areas with diameter of 2 mm.
Bi-Se-Au	C26	240	110	20	4 Au areas.
Polycrystalline Te-Se-Au	C48	250	120	30	4 Au areas.
	C58	255	115	40	4 Au areas.
	C59	255	115	45	4 Au areas.
	C62	255	125	45	4 Au areas.
	C64	250	120	40	4 different size Au areas.
	C65	250	120	45	4 Au areas. 4 different size Wood's metal eletrode contact.
Au-Se-Au	C35	240	115	30	4 Au areas. Heat-treated at 120°C in air for 2 hrs and 4 hrs. Again heat-treated at 160°C and 190°C respectively for 2 Hrs.

Table 3.1 cont.

Structure	Sample No.	Selenium Deposition[1,2]			Remarks
		Source Temp. (°C)	Substrate Temp. (°C)	Evaporation Time (min.)	
Bi-Se-Tl	C21	225	140	20	3 Tl areas.
	C22	225	90	20	4 Tl areas.
	C31	240	70	25	3 Tl areas. Heat-treated at 160°C in dry N_2 for 20hrs.
	C34	240	110	30	4 Tl areas. Heated deliberately by soldering iron for indefinite time.
	C36	240	110	30	4 Tl areas. Teat-treated at 195°C in dry N_2 for 2 hrs.
	C37	240	110	30	4 Tl areas. Heat-treated at 170°C in dry N_2 for 2 hrs.
	C40	240	110	35	4 Tl areas. Heat-treated at 140°C in dry N_2 for 2 hrs.
	C43	240	110	35	4 Tl areas. Heat-treated at 155°C in dry N_2 for 2 hrs.
	C44	240	110	30	4 Tl areas. Heat-treated at 180°C in dry N_2 for 2 hrs.
	C46	240	110	35	4 Tl areas. Heat-treated at 130°C in dry N_2 for 2 hrs.
	C52	240	110	30	4 Tl areas. Heat-treated in 140°C in dry N_2 for 2 hrs.
	C54	245	115	35	4 Tl areas. Se film heat-treated in wet O_2 for 24 hrs. before deposition of Tl.
	C55	250	125	30	4 Tl areas. Se film heat-treated in dry N_2 for 24 hrs. before deposition of Tl.
Polycrystalline Te-Se-Tl	C45	240	120	35	4 Tl areas.
	C49	245	120	35	4 Tl areas.
	C53	250	125	40	4 Tl areas.
Monocrystalline Te-Se-Tl	C47	250	150	30	Dots of Tl area with diameter of 2mm.
	C57	250	150	40	Dots of Tl area with diameter of 2mm.

Table 3.1 cont.

Structure	Sample No.	Selenium Deposition[1,2]			Remarks
		Source Temp.(°C)	Substrate Temp.(°C)	Evaporation Time (min.)	
Bi-Se-Bi	C28	240	110	30	3 Bi areas. Heat-treated at 110°C for 2 hrs. in dry N_2
Polycrystalline Te-Se-Bi	C56	250	110	40	4 Bi areas.
	C61	255	130	45	4 Bi areas.
	C63	250	125	45	4 Bi areas. 2 Wood's metal stripes deposited on each Bi area.

Notes : (1) Se source contained nominally 60 ppm Cl.

(2) Source to substrate distance is 10 cm.

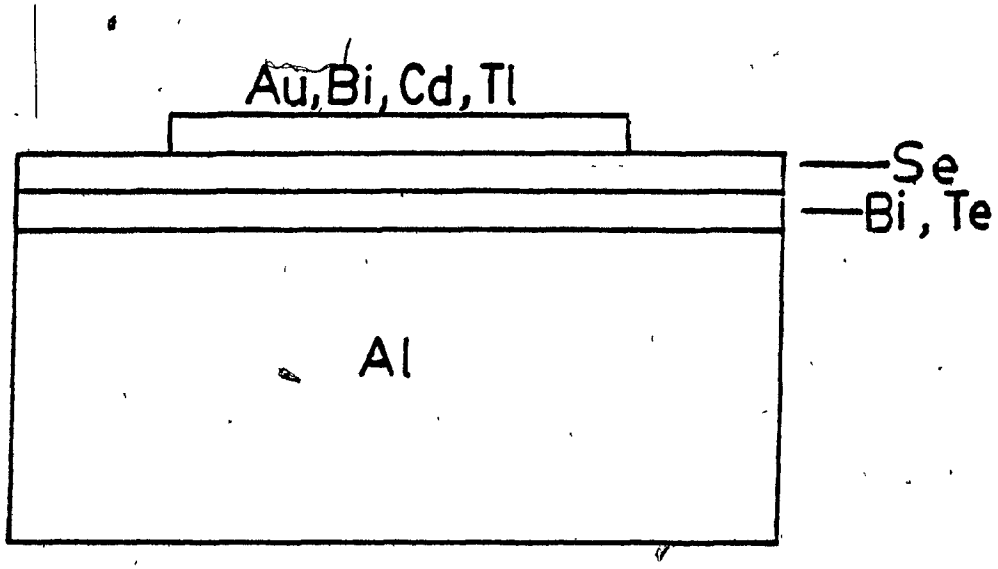

Fig. 3.1 A cross-sectional view of the Se-metal diode structure studied.

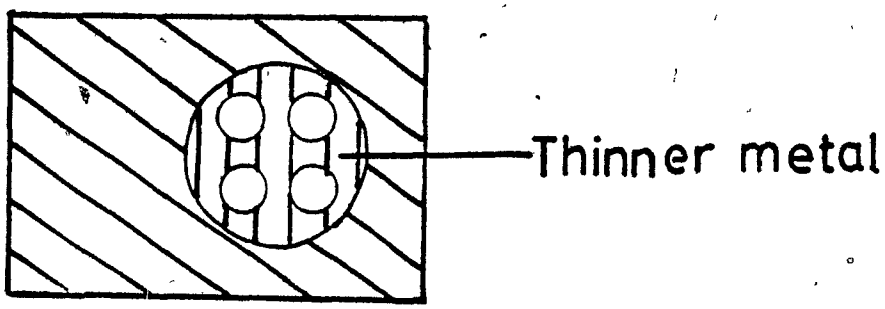

Fig. 3.2 Mask used for counterelectrode material deposition.

CHAPTER 4

MEASUREMENT TECHNIQUES

4.1 Introduction

The methods of measurement made to characterize the electrical behavior of each selenium-metal structure after fabrication are described in this chapter. The actual results of these measurements, however, will be presented in detail in later chapters.

The measurements were :

(1) Dark current density (j) as a function of voltage (V).

(2) Parallel incremental capacitance (C_p) and resistance (R_p) versus frequency (f) at zero bias.

(3) Parallel incremental capacitance versus bias voltage in the reverse (V_R) and forward (V) directions at a fixed frequency.

4.2 Dark Current Density (j) - Voltage (V) Characteristics

The setup for measurement of current-voltage characteristics over a range of V=-1.2 to 1.2 volt is shown in Fig. 4.1. Measurements were taken in a point-to-point manner in both forward and reverse directions. The current was measured over several decades with a Keithley 610B

electrometer and the voltage with a Keithley 169 multimeter. The device was covered with a piece of black cloth during the measurements to avoid the influence of light.

4.3 Parallel Incremental Capacitance and Resistance versus Frequency

Measurements of parallel incremental capacitance (C_p) and resistance (R_p) were made at zero bias over the frequency range from 100Hz to 4MHz. For frequencies below 100kHz, a Hewlett-Packard Model 4274A multi-frequency LCR meter was used. For the higher frequency range above 100kHz, a Wayne Kerr type B601 bridge was used together with a General Radio type 1001A oscillator. A Tektronics Model 7403N oscilloscope was used as the bridge detector, which enabled the null of the fundamental frequency, to be separated from that of harmonics generated by the sample. The arrangement of the measuring system is shown schematically in Fig. 4.2.

4.4 Parallel Capacitance versus Bias Voltage at a Fixed Frequency

Parallel capacitance versus bias voltage was measured using a Hewlett-Packard Model 4274A Multi-Frequency LCR meter. The reverse bias voltage was varied from V_R=-1.0 to 1.2 volt applied internally from the LCR meter and the a.c. signal level was kept at 20 mV. A Keithley 169 multimeter

was attached to the LCR meter to monitor the applied bias voltage.

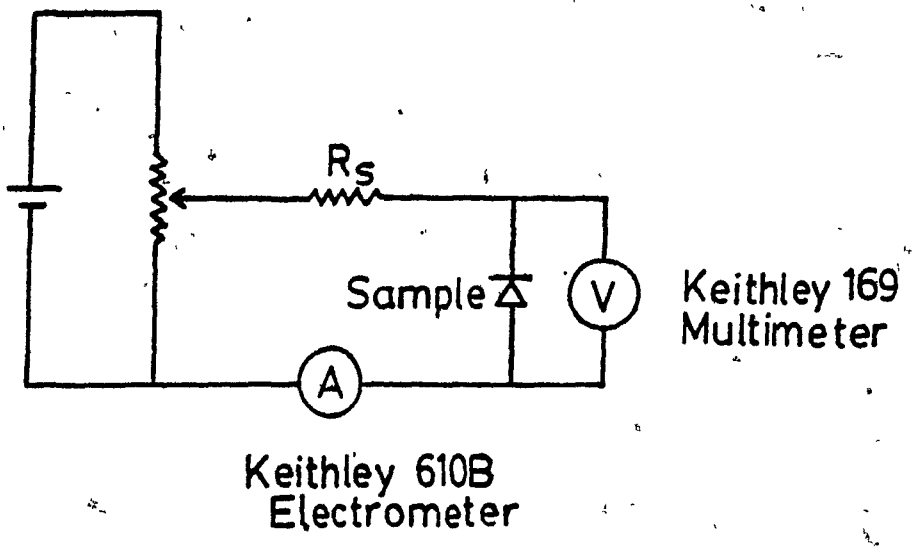

Fig. 4.1 Experimental circuit arrangement used for measurement of current voltage characteristics.

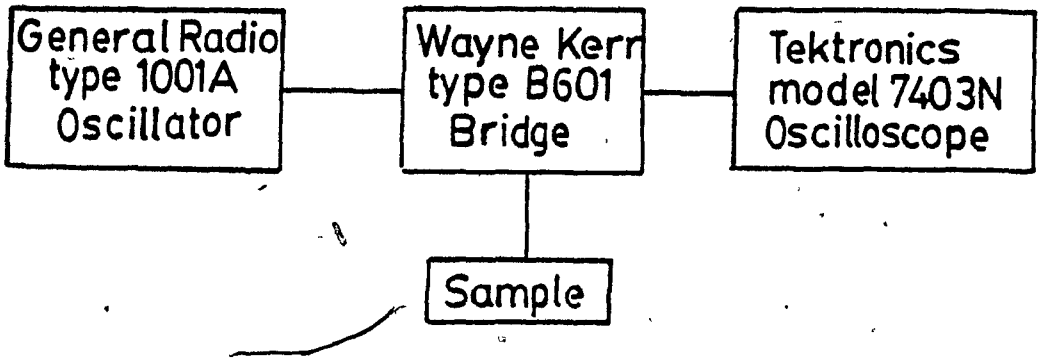

Fig. 4.2 Experimental arrangement used for measurement of incremental capacitance and resistance as a function of frequency in the range above 100kHz.

CHAPTER 5

BASIC DIODE CHARACTERISTICS AND BARRIER HEIGHT DETERMINATION

5.1 Introduction

In this chapter, the results of electrical measurements of many of the various structures listed in Table 3.1 are presented. The first section of the chapter gives the results of static dark current-voltage characteristics of the different samples, categorized according to the different counterelectrode metals employed. This is principally to illustrate the differences in the rectifying characteristics of the various diodes. Then, the results of capacitance-voltage measurements are presented as plots of $(A/C)^2$ against reverse voltage. Only results obtained at a frequency of 1 kHz are shown, since variation at other frequencies is reported in chapter 7. Furthermore, comment on certain capacitance singularities will also be postponed to a later chapter. In the final section, values of barrier height are deduced from the experimental results and compared with corresponding metal work functions.

5.2 Dark j-V Static Characteristics

5.2.1 Se-Cd Structures

Fig. 5.1 shows a semilogarithmic plot of current density against voltage of four Se-Cd samples with different back contact materials between the selenium layer and the aluminum stud surface. These diodes consist of one sample (C29) with bismuth, one (C42) with polycrystalline tellurium and two (C50 & C51) with single crystal tellurium as back contact materials. As indicated, all four samples show prominent forward-to-reverse rectification. Sample C42, with a polycrystalline Te back contact, exhibits the highest current density at 1 volt in the forward direction, whereas C51 shows the lowest value. Since series resistance is dominant at this forward voltage, the results suggest that polycrystalline tellurium may give the lowest resistance at the back contact. It is noted that the two samples (C50 & C51), where epitaxial selenium on single crystal tellurium was used, showed the largest rectification ratio of about 5 decades between forward and reverse current at 1 volt, while the other two samples, C29 and C42, showed ratio of about 4 and 3 1/2 decades respectively.

Between a forward voltage of 0.1 to 0.4 volt, all the samples gave approximately the same slope, with an ideality factor of n=2, assuming a variation in this range of the form $j = j_o \exp(\frac{qV}{nkT})$. The two samples with monocrystalline selenium also show a somewhat smaller extrapolated intercept on the vertical axis of current density (j_o).

Fig. 5.2 shows the results of three Bi-Se-Cd samples C29, C30 and C33, for which the substrate temperatures during

the selenium film deposition were 140, 90 and 80°C respectively. This result clearly illustrates that higher selenium deposition temperature gives higher forward current, which is presumably due to an increase of electrical conductivity of the selenium with increase of substrate temperature.

5.2.2 Se-Bi Structures

Fig. 5.3 presents current-voltage characteristics of two Te(poly)-Se-Bi samples (C56 & C63) and one Bi-Se-Bi sample (C28). Sample C63 was fabricated with Wood's metal contact stripes evaporated on the top of the Bi counterelectrode, while the other two were without evaporated Wood's metal. However, all wires were soldered to the counterelectrode with Wood's metal.

It is apparent that all three samples showed rectifying characteristics. The rectification ratio amounted to some 3 or more decades for samples C56 and C63 at 1 volt but for the Bi-Se-Bi sample C28, this ratio was more than 4 decades. This clearly confirms the low resistance and ohmic character of the back contact, despite the fact that it was made with the same metal as used for the counterelectrode.

At smaller forward voltage, samples C63 and C28 showed approximately the same slope with an ideality factor n between 1 and 2.

5.2.3 Se-Au Structures

Fig. 5.4 depicts the results of five Se-Au samples. Three samples (C48, C62 & C65) were fabricated with polycrystalline tellurium back contacts, while sample C26 and C35 were made with bismuth and gold respectively. Sample C65 was fabricated with four different areas of evaporated Wood's metal on the top of the gold counterelectrodes. In the case of the other four samples, the contact wires were soldered directly to the gold with Wood's metal.

It is seen that the overall rectification ratio lies between 1 and 2 decades. Sample C48 showed a ratio of almost 2 decades, while sample C65 showed a ratio of less than 1 decade.

At small forward bias voltage for all the samples, a constant slope is not apparent, suggesting an almost ohmic character. However, the average slope in this region appears to correspond to approximately n=2.

5.2.4 Se-Tl Structures

Figs. 5.5 (a) and (b) show current-voltage results of sixteen Se-Tl samples. Twelve of these (C21, C22, C31, C34, C36, C37, C40, C43, C44, C46, C52 & C55) were Bi-Se-Tl structures. Three samples (C45, C49 & C53) were Te(poly)-Se-Tl structures and one (C57) was a Te(single crystal)-Se-Tl structure. As will be reported specifically in chapter 6, the characteristics on these samples change considerably with storage in air and with

subsequent heating. For this reason, the measurements were always made immediately after fabrication.

As seen from Figs. 5.5 (a) and (b), the Se-Tl structures showed a strong forward-to-reverse rectification ratio amounting to about four decades at 1 volt. This ratio varies from more than 5 decades (sample C49) to less than 3 decades (C40).

Apart from two samples (C45 & C55), all the curves in Fig. 5.5 (a) and (b) merge essentially into one straight line at low forward voltage; the slope in this region corresponds to an ideality factor of n=1.2.

5.2.5 Comparison of j-V Characteristics of the Four Counterelectrode Materials

A comparison of the diodes with the four different counterelectode materials Cd, Bi, Au and Tl is now made. The specific samples for this comparison were chosen on the basis that all of them were fabricated with a polycrystalline tellurium back contact, since this appeared to give the lowest series resistance. Fig. 5.6 shows the current-voltage variation of four such samples. It can be seen that at 1 volt the Se-Au structure (C48) gave the highest forward current density, followed by the Se-Bi (C56), Se-Tl (C49) and Se-Cd (C42) structures. However, at a forward potential of 0.1 volt, the order, in decreasing current, is seen to be Au, Bi, Cd and Tl. Values of current density extrapolated from the straight line regions to zero voltage (in the same

sequence) are as follows: 7×10^{-5}, 1.3×10^{-5}, 5×10^{-7} and 1.4×10^{-7} amp/cm^2. In respect of the forward-to-reverse current rectification ratio measured at 1 volt, the Se-Tl structure has a value of about 10^5, the Se-Cd structure has nearly 10^4, Se-Bi more than 10^3 and Se-Au 10^2 to 10^3.

At small forward voltage, the Se-Tl structure gave the steepest slope with n=1.2, while the other three structures gave n-values varying between 1 and 2.

5.3 Results of Capacitance-Voltage Measurements

In this section, the results of capacitance measurements as a function of bias are presented as plots of $(A/C)^2$ against reverse bias V_R at a test frequency of 1kHz. This frequency was chosen to avoid capacitance singularities observed at lower frequencies and bias-independent contributions at higher frequency. The samples were the same as those in section 5.2.

5.3.1 Se-Cd Structures

Fig. 5.7 shows a plot of $(A/C)^2$ against reverse voltage of four Se-Cd structures. For reverse voltages, all four experimental lines have a slight curvature but with very different average slopes.

Extrapolated intercepts to the voltage axis from the V_R range of 0 to about 0.2 volt vary from -0.3 to -0.5 volt for samples C29, C50 and C42. For sample C51, the extrapolated

intercept is anomalously large. In the forward direction (V_R negative) minima are observed for all samples.

A plot of $(A/C)^2$ versus V_R for the three Se-Cd samples (C29, C30 and C33) fabricated with different substrate temperatures during the selenium deposition, is shown in Fig. 5.8. It is noted that the extrapolated intercept on the voltage axis is much larger numerically for the sample prepared at 80°C.

5.3.2 Se-Bi Structures

The results of $(A/C)^2$ versus V_R of three Se-Bi samples are shown in Fig. 5.9. The average slope ranged over almost an order of magnitude, despite the fact that nominally 60 ppm chlorine doping in the selenium was used for all three samples. The extrapolated voltage intercepts of C28 and C56 from the low V_R regions are -0.42 and -0.6 volt respectively, while that of C63 is less than -0.1 volt. Samples C28 and C63 show minima in $(A/C)^2$ in the forward direction.

5.3.3 Se-Au Structures

Fig. 5.10 shows the experimental capacitance results of five Se-Au samples. A minimum in $(A/C)^2$ is seen to occur for sample C62 at a reverse voltage near V_R=0.3 volt and for sample C35 near V_R=0.1 volt. A minimum and maximum were observed in the reverse direction in orginal measurements made just after fabrication on sample C26 but which are not shown here. More recent measurements on this sample are

plotted in Fig. 5.10 showing a monotonic increase of $(A/C)^2$ with reverse voltage, as observed also on samples C48 and C65. Extrapolated intercepts on the voltage axis from the low voltage reverse regions of C26, C48 and C62 are -0.1, -0.12 and -0.17 volt respectively.

5.3.4 Se-Tl Structures

Figs. 5.11 (a) and (b) exhibit the capacitance results of sixteen Se-Tl structures. Almost all of the experimental lines on the $(A/C)^2$ versus V_R plots are straight lines for the reverse direction and with slopes varying over a smaller range than for the other structures. Furthermore, the extrapolated voltage intercepts converge to a relatively small range between -0.55 and -0.6 volt. Thus, the consistency observed for the j-V characteristics of the Se-Tl structures also occurs for the capacitance characteristics. In the forward direction (negative V_R), $(A/C)^2$ shows a minimum and then a maximum for all the measured samples.

5.3.5 Comparison of Capacitance Results for the Four Counterelectrode Materials

In Fig. 5.12, $(A/C)^2$ versus V_R is replotted for the same four samples shown in Fig. 5.6, where, it is recalled, all diodes had the same back contact material of polycrystalline tellurium. Extrapolation from the low reverse voltage regions yields the values given as V_o in Table 5.1. This

table also lists the initial slopes, namely $\frac{\Delta[(A/C)^2]}{\Delta V_R}$ for the four structures.

5.4 Evaluation of Barrier Heights from Experimental Results

From the $(A/C)^2$ versus V_R slopes in Table 5.1, carrier concentrations are calculated using eqn.(2.2) of chapter 2 and the values are given in column 4. Here, it is assumed that the concentrations, so-obtained, represent mobile holes. From these concentrations $(p=N_A)$, the location of the Fermi level above the valence band E_F-E_V is given by (eqn.(2.3)):

$$E_F-E_V = \frac{kT}{q} \ln\left(\frac{N_V}{p}\right) \quad . \qquad (2.3)$$

Assuming the effective mass ratio for the holes to be unity, values of E_F-E_V were calculated and are listed in column 5 of Table 5.1. Finally, using the extrapolated intercept voltages V_o (column 6) and the Fermi energies E_F-E_V, values of Schottky barrier height ϕ_{bp} were obtained in column 7 using eqn.(2.4), namely:

$$\phi_{bp} = \frac{E_F-E_V}{q} + V_o \quad . \qquad (2.4)$$

Fig. 5.13 shows a plot of these calculated barrier heights plotted against work function values (ϕ_m) obtained from the literatures [9] [10] [11]. It is noted that although there are only four points, plus another point from selenium itself (assuming a Se-Se contact to have zero

barrier height), there is a systematic correlation seen between ϕ_{bp} and ϕ_m.

5.4.1 Estimate of Density of Surface States

According to simple Schottky junction theory, the slope of a plot of ϕ_{bp} against ϕ_m should be -1 with an intercept on the ordinate axis of $\left(\frac{E_G}{q} + \chi_s \right)$ (chapter 2). However, because of surface states, the slope is actually given by $-\gamma$, as discussed in sec. 2.5. The slope of the line drawn through the points in Fig.5.13 is -0.34 with an intercept on the ϕ_{bp} axis of 2.0 volt. From eqn.(2.5), the density of interface states is thus given by

$$D_s = \frac{\epsilon_o \cdot \epsilon_{ri}}{q\delta} \frac{1-\gamma}{\gamma}$$

If the interfacial layer is taken to have a thickness of 10A and a relative dielectric constant ϵ_{ri} of 10 is assumed, then substitution of these numbers and the measured γ-value of 0.34, yields a D_s value of about 10^{14} per cm^2 per eV of energy gap. The intercept as given by (eqn. 2.6) is :

$$\gamma \left(\frac{E_G}{q} + \chi_s \right) + (1-\gamma)\,\phi_o$$

Substituting the values E_G=1.85 eV and χ_s=4.2 V for Se gives a calculated intercept of $2.06+0.66\phi_o$, which when, equated to the observed value of 2.0 volt, yields ϕ_o=-0.1 volt. Thus, with this interpretation, there are some $10^{14}/cm^2$ interfacial states located close to the valence band edge.

Table 5.1
Barrier Height from C-V Results

Counterelectrode Material	Reported Work Function ϕ_m (volt)	$\frac{\Delta[(A/C)^2]}{\Delta V_R}$ ($cm^4F^{-2}V^{-1}$)	N_A (cm^{-3})	$\frac{E_F-E_V}{q} = -\frac{kT}{q}\ln(\frac{2.5\times10^{19}}{N_A})$ (eV)	Extroplated Intercept Voltage V_o (volt)	Barrier Height $\phi_{bp} = -\frac{E_F-E_V}{q}+V_o$ (volt)
Tl	3.8	1.78×10^{14}	7.9×10^{16}	0.14	0.6	0.74
Cd	4.2	6.34×10^{13}	2.2×10^{17}	0.12	0.44	0.56
Bi	4.3	1.62×10^{14}	8.7×10^{16}	0.14	0.34	0.48
Au	5.1	4.33×10^{14}	3.2×10^{16}	0.17	0.12	0.29

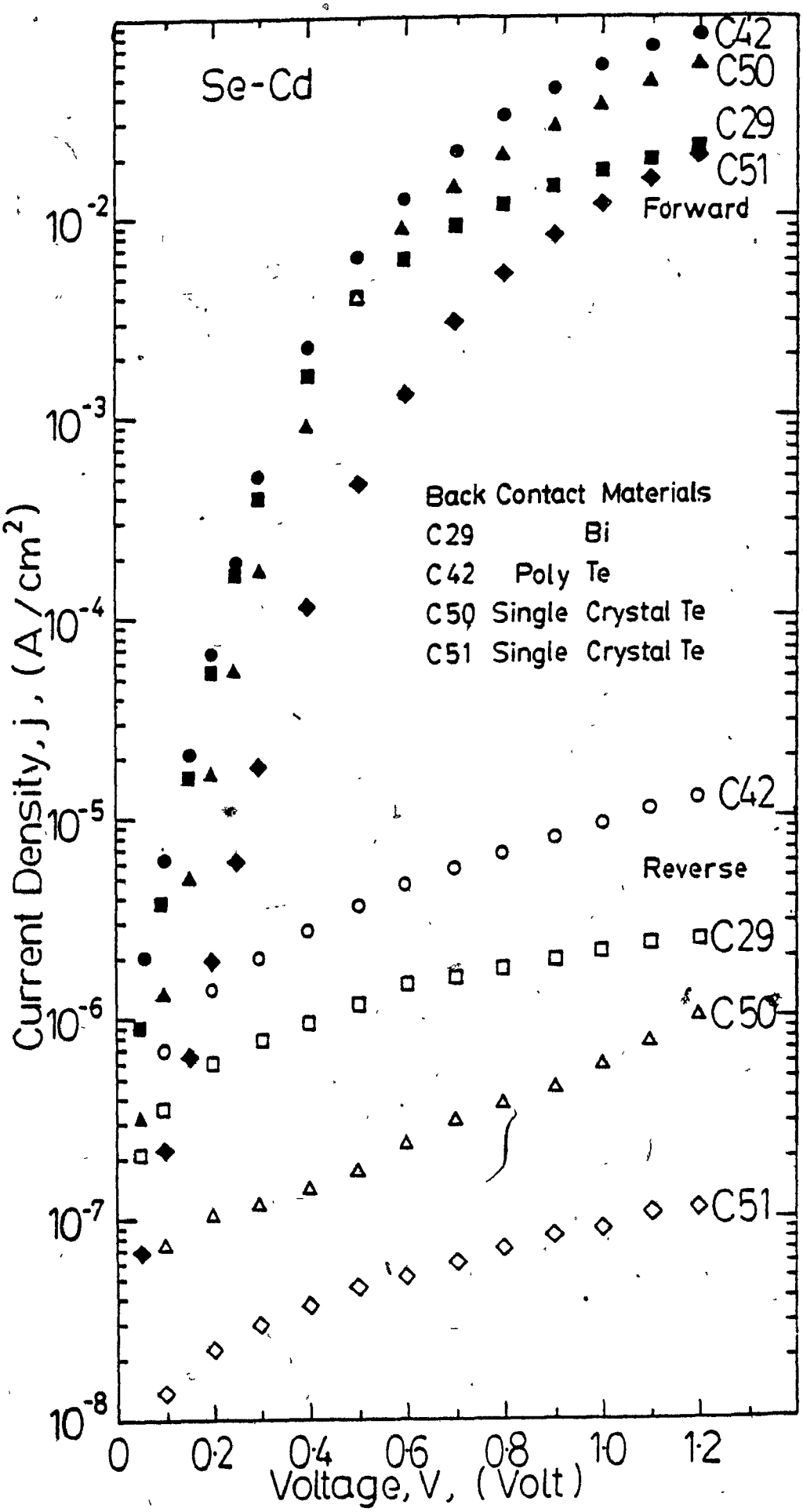

Fig. 5.1 Plot of the logarithm of current density against voltage for 4 Se-Cd structures with different back contact materials.

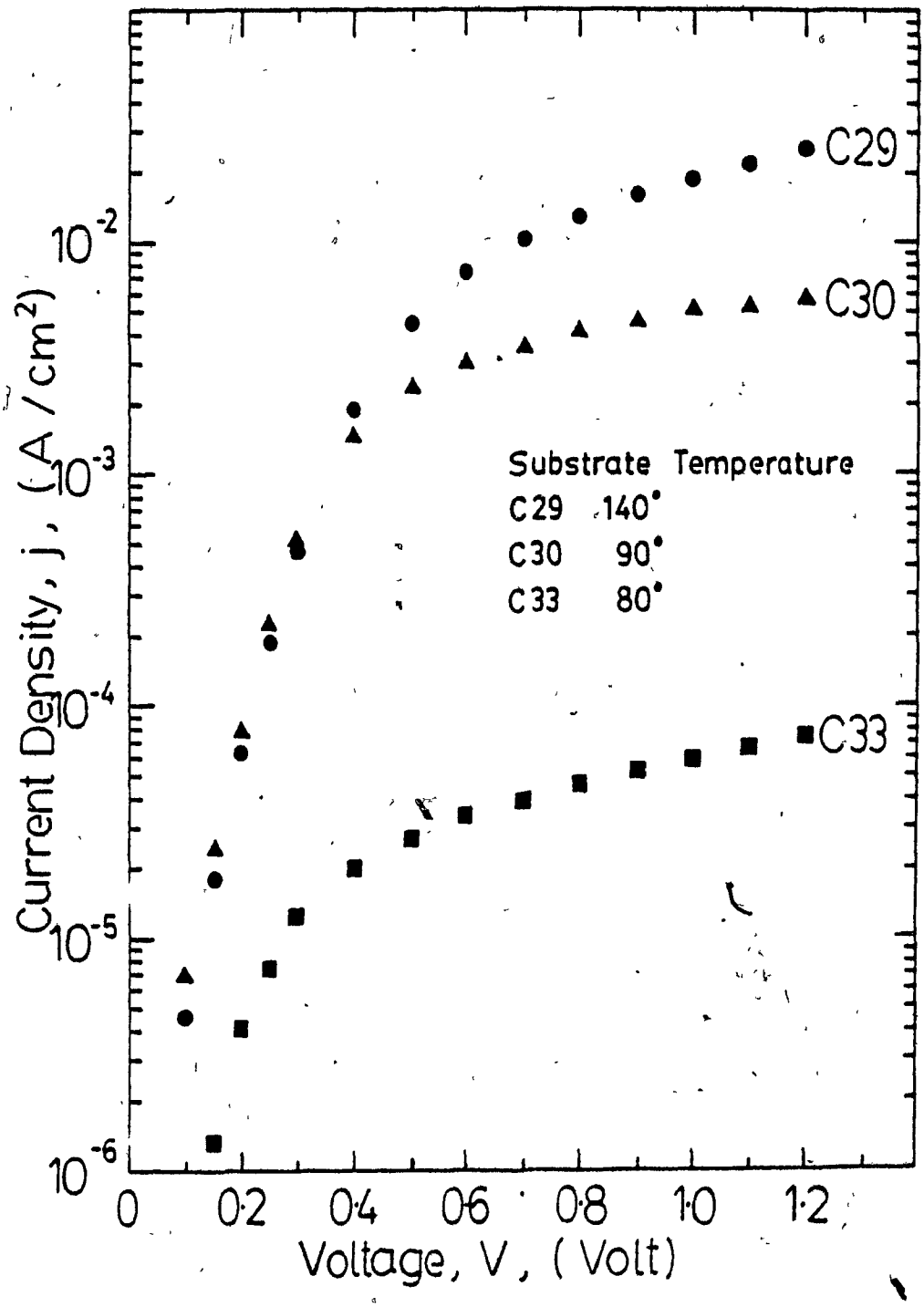

Fig. 5.2 Plot of the logarithm of current density against voltage for 3 Bi-Se-Cd structures with different substrate temperatures during Se deposition.

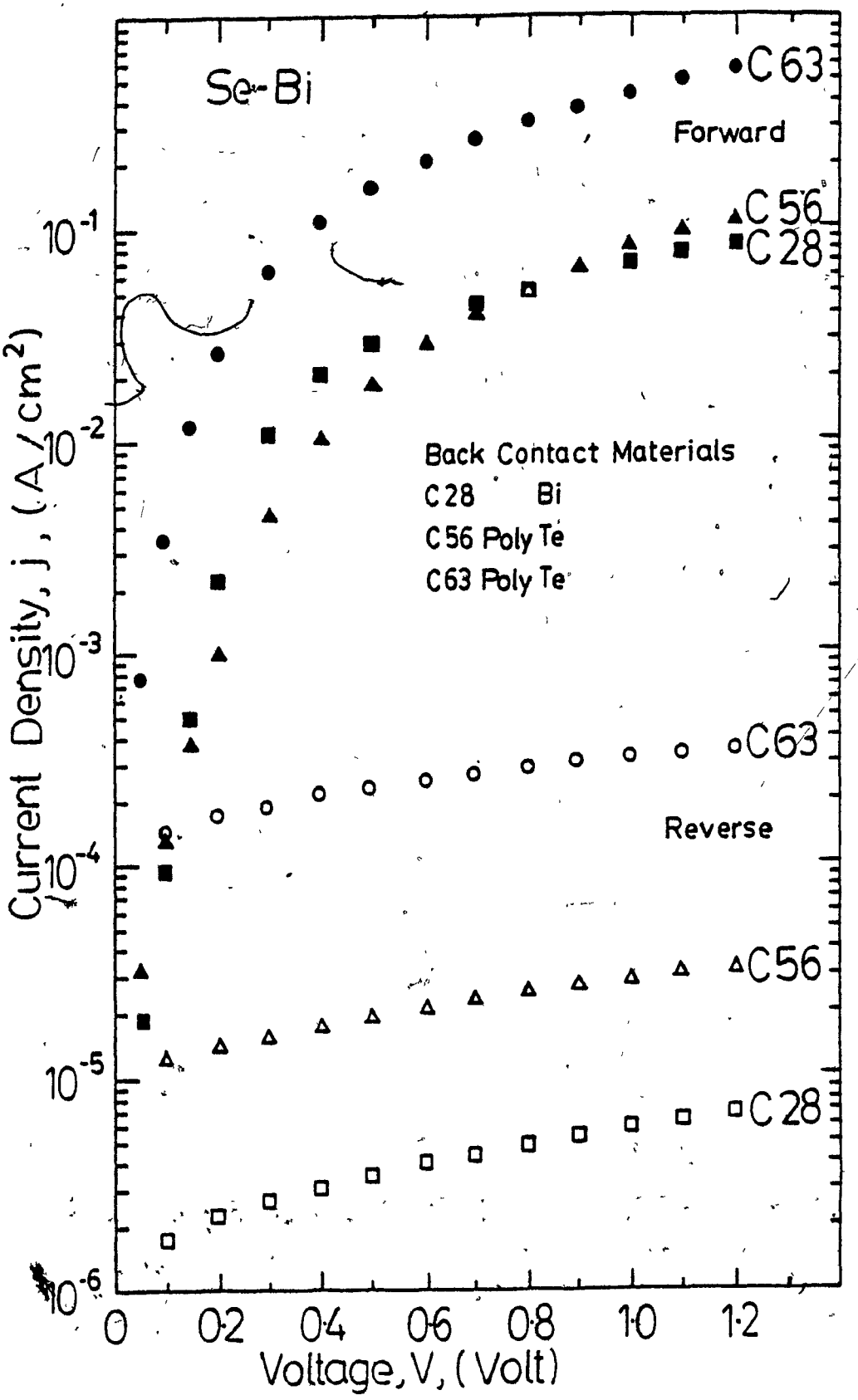

Fig. 5.3 Plot of the logarithm of current density against voltage for 3 Se-Bi structures with different back contact materials.

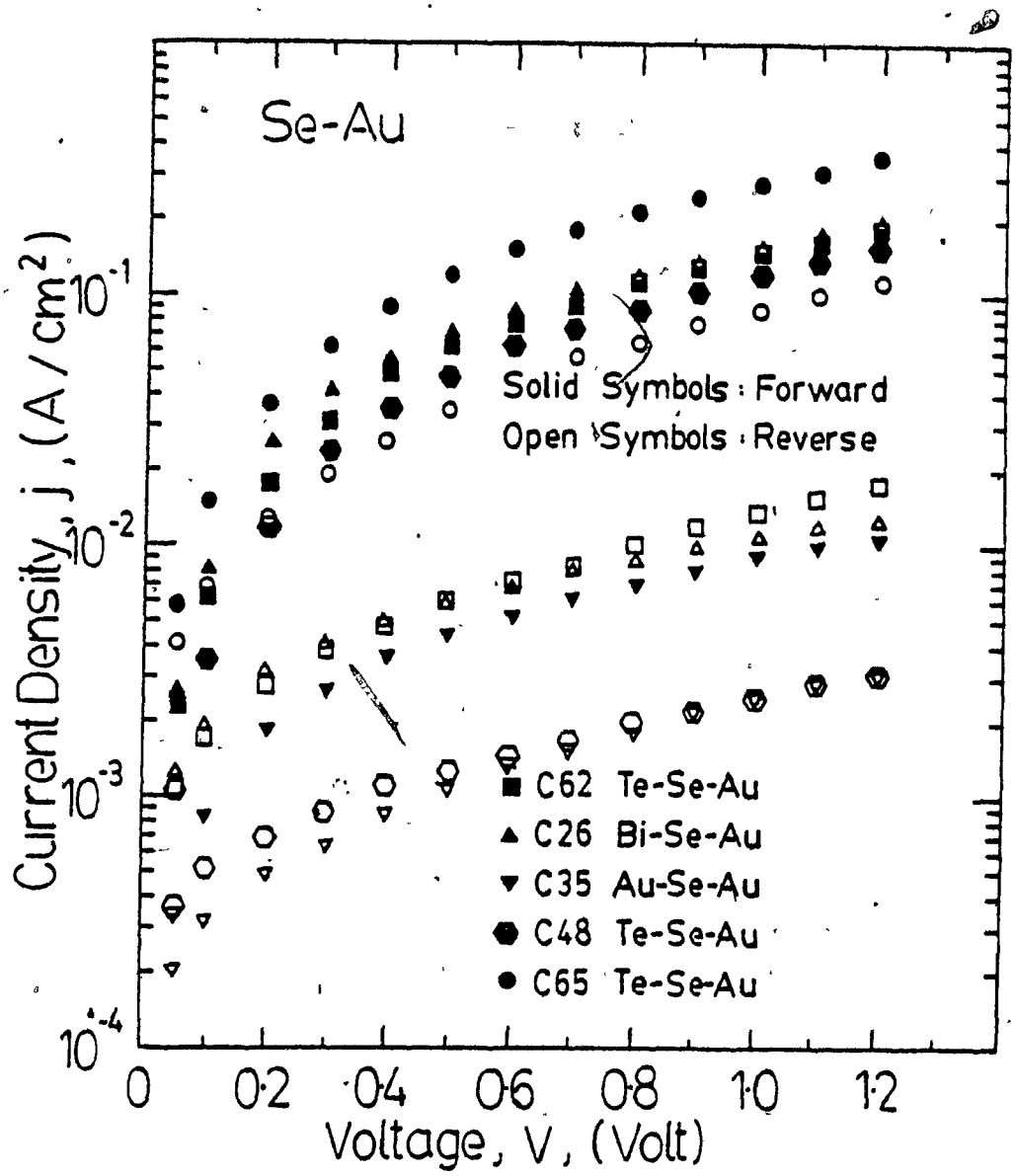

Fig. 5.4 Plot of the logarithm of current density against voltage for 5 Se-Au structures with different back contact materials.

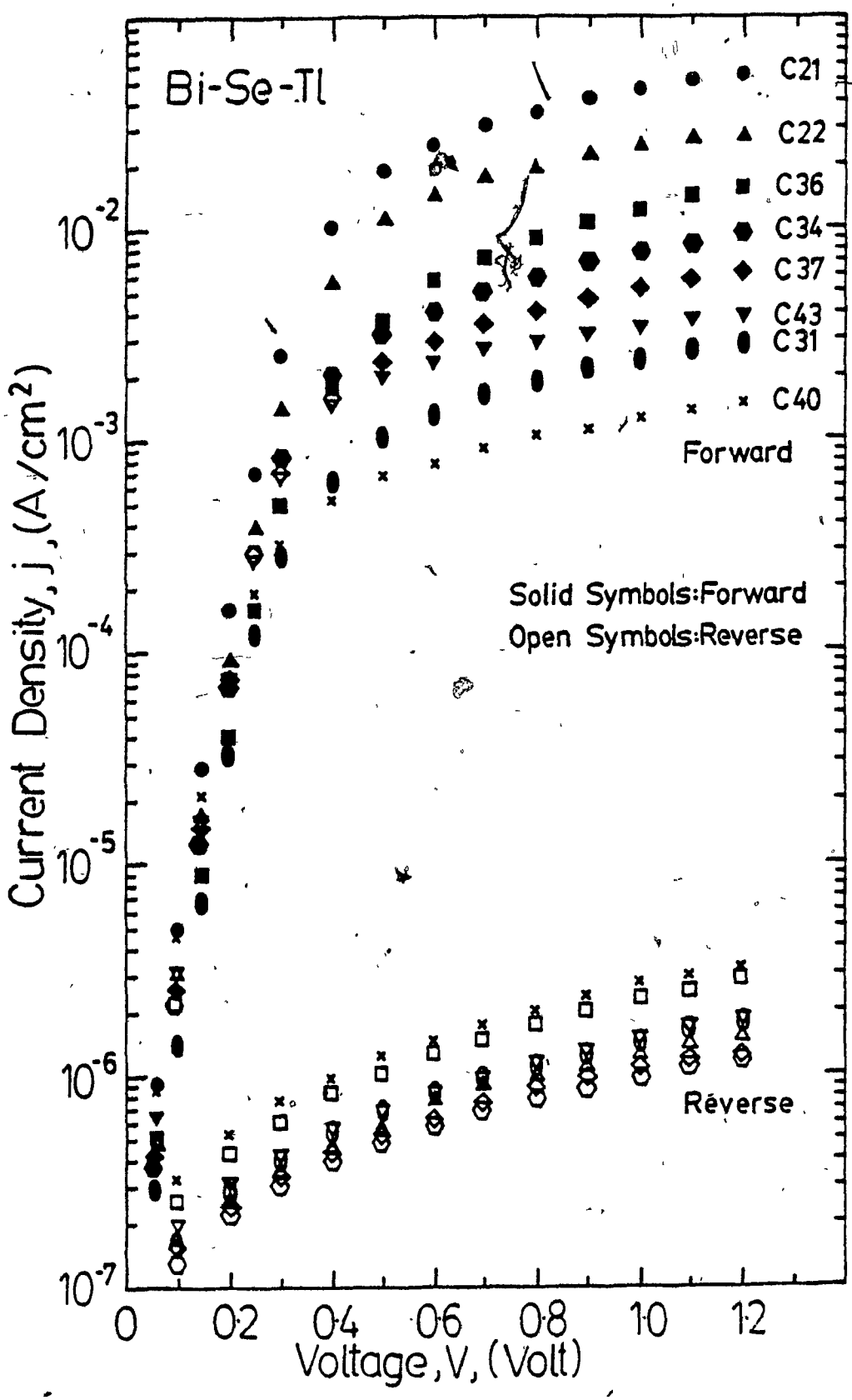

Fig. 5.5(a) Plot of the logarithm of current density against voltage for 8 Bi-Se-Tl structures.

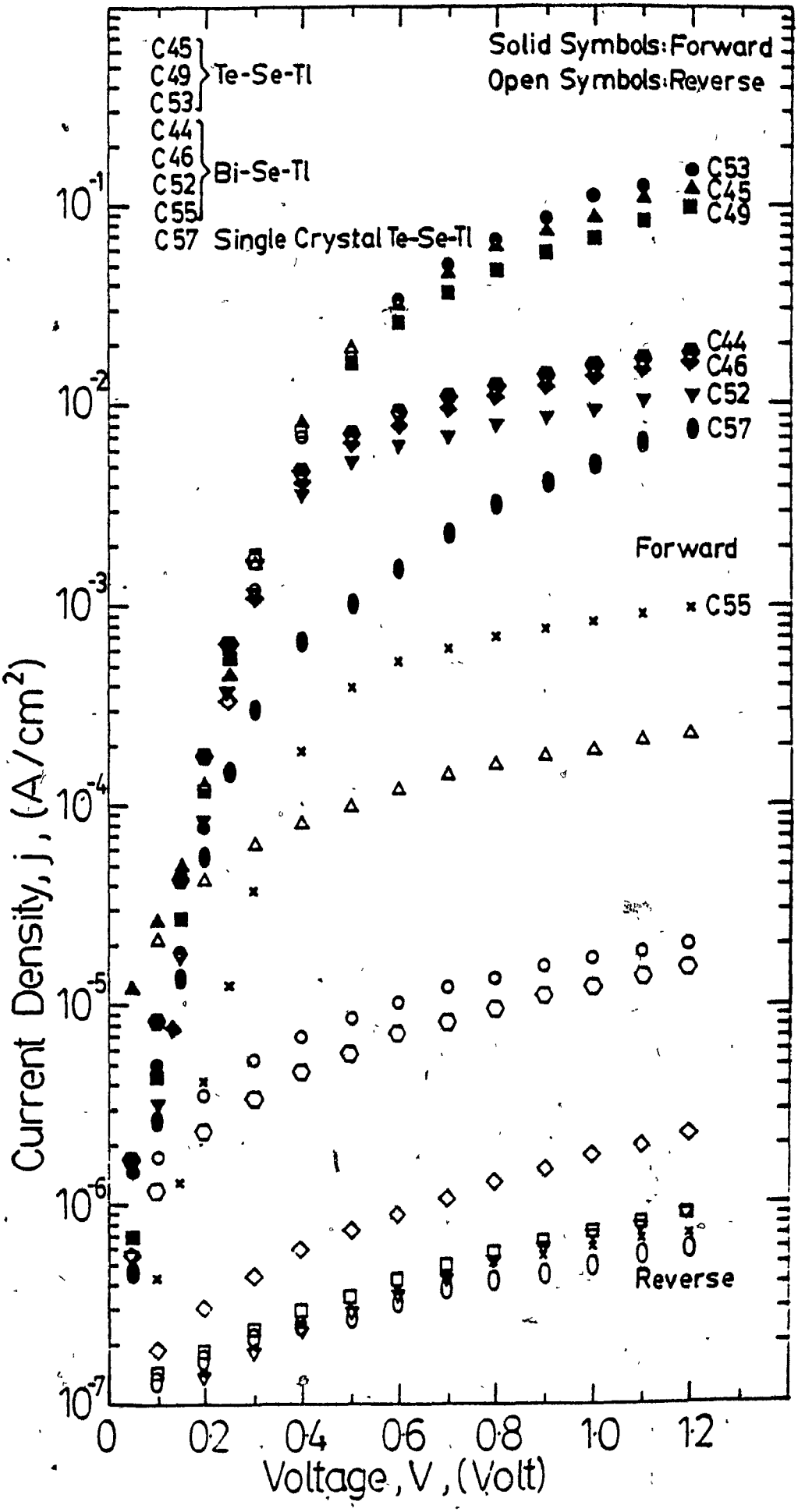

Fig. 5.5(b) Plot of the logarithm of current density against voltage for 8 Se-Tl structures with different back contact materials.

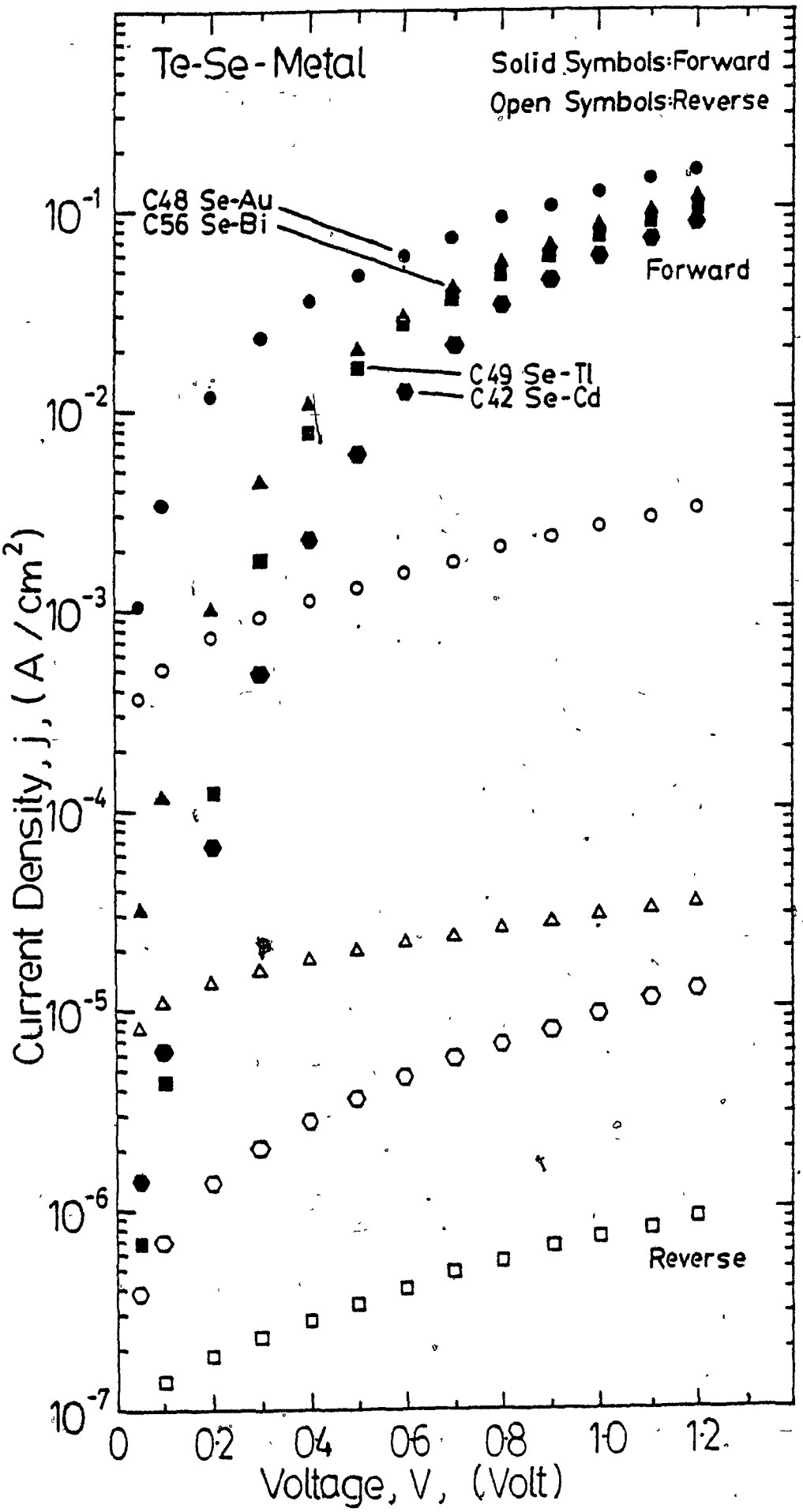

Fig. 5.6 Comparison of the dark ln(j)-V characteristics of 4 polycrystalline Te-Se-metal structures with different counterelectrode materials.

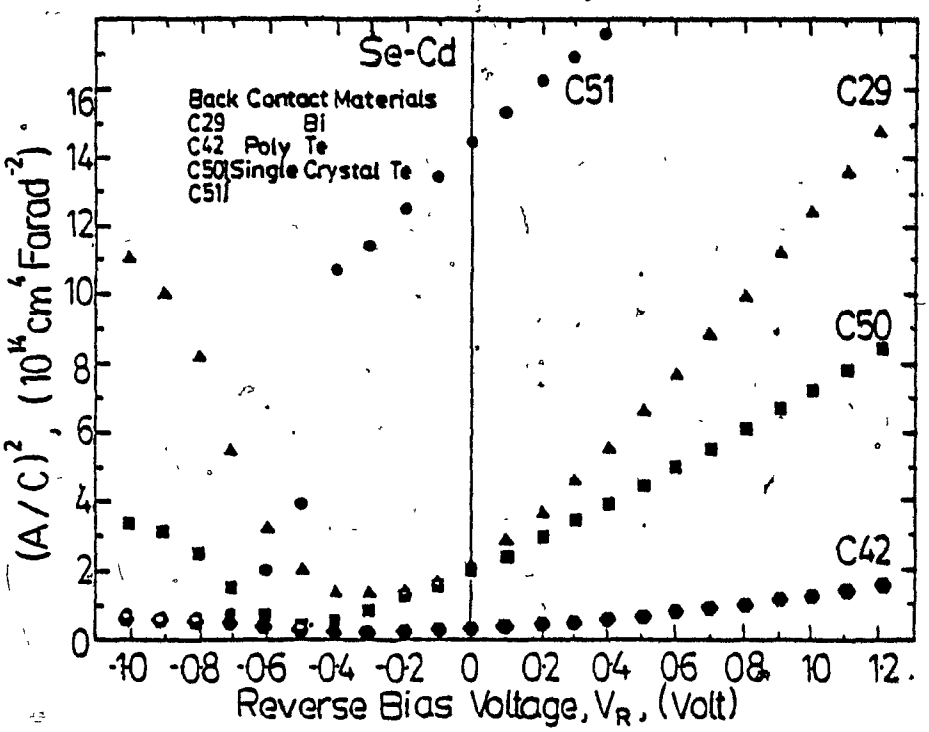

Fig. 5.7 Plot of $(A/C)^2$ versus V_R for 4 Se-Cd structures with different back contact materials, where C is parallel capacitance and A is the Cd area.

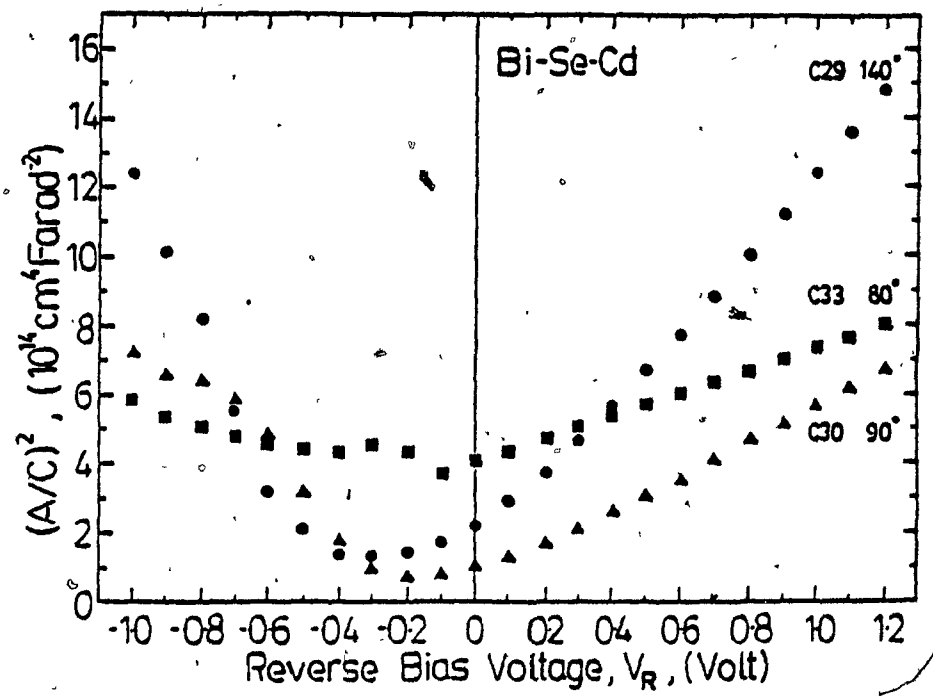

Fig. 5.8 Plot of $(A/C)^2$ versus V_R for 3 Bi-Se-Cd structures with different substrate temperature during Se deposition.

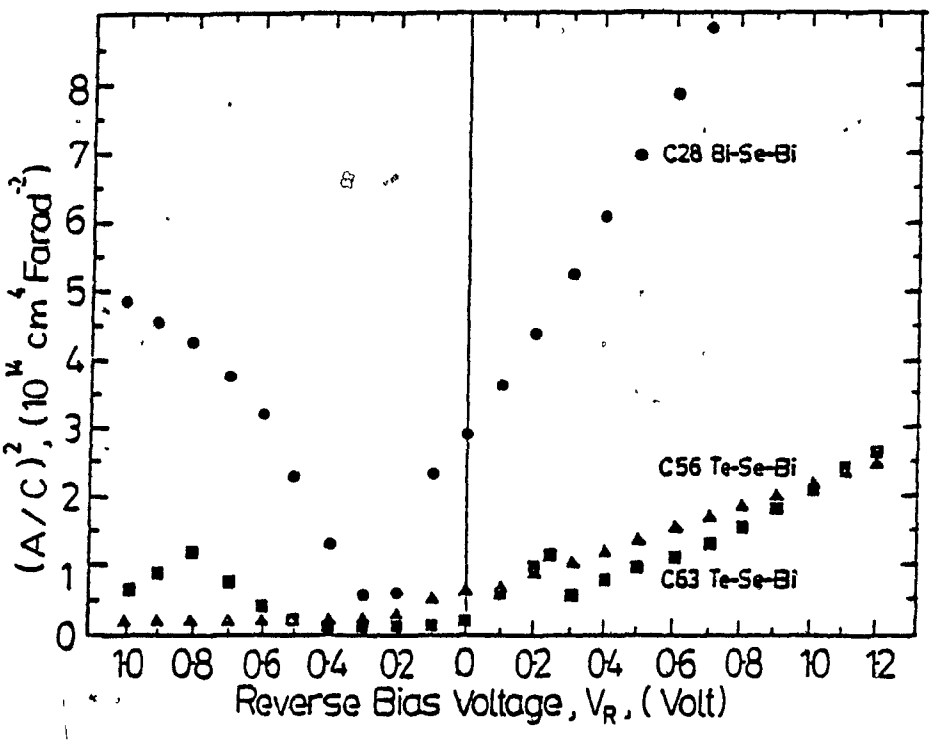

Fig. 5.9 Plot of $(A/C)^2$ versus V_R for 3 Se-Bi structures with different back contact materials.

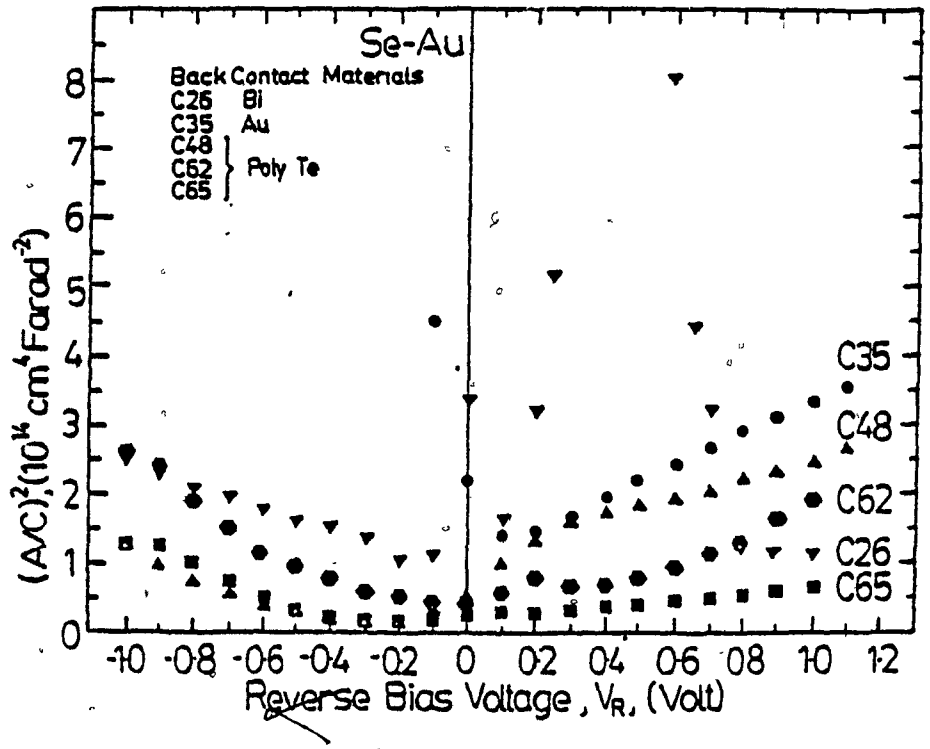

Fig. 5.10 Plot of $(A/C)^2$ versus V_R for 5 Se-Au structures with different back contact materials.

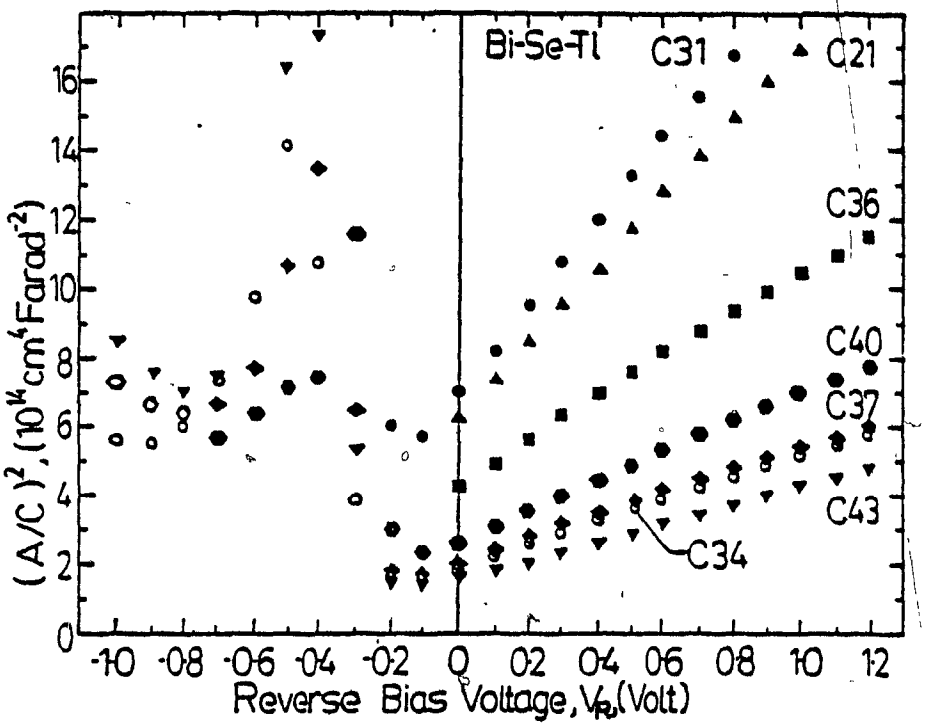

Fig. 5.11(a) Plot of $(A/C)^2$ versus V_R for 7 Bi-Se-Tl structures.

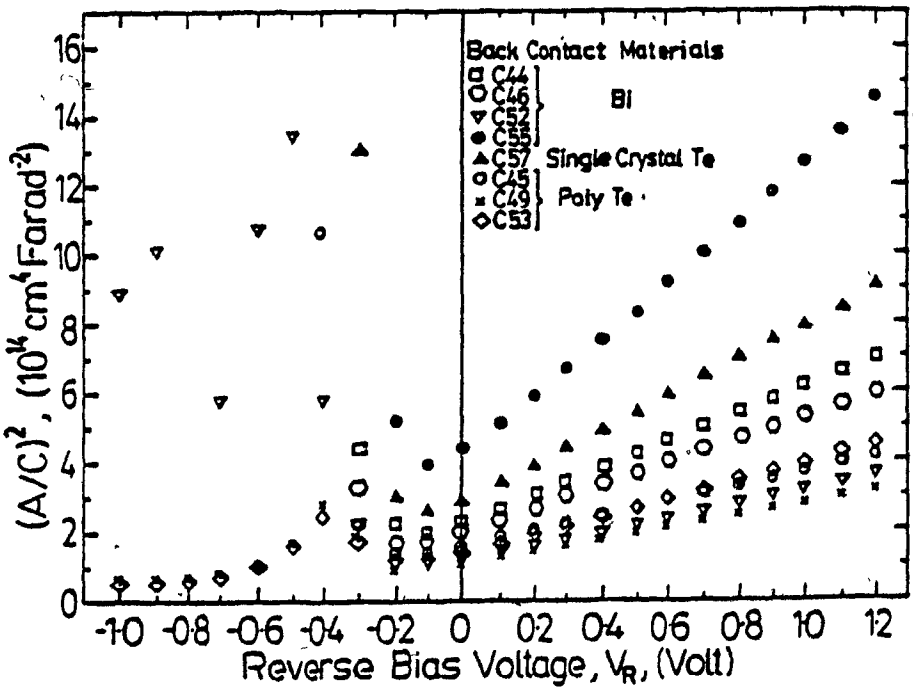

Fig. 5.11(b) Plot of $(A/C)^2$ versus V_R for 8 Se-Tl structures with different back contact materials.

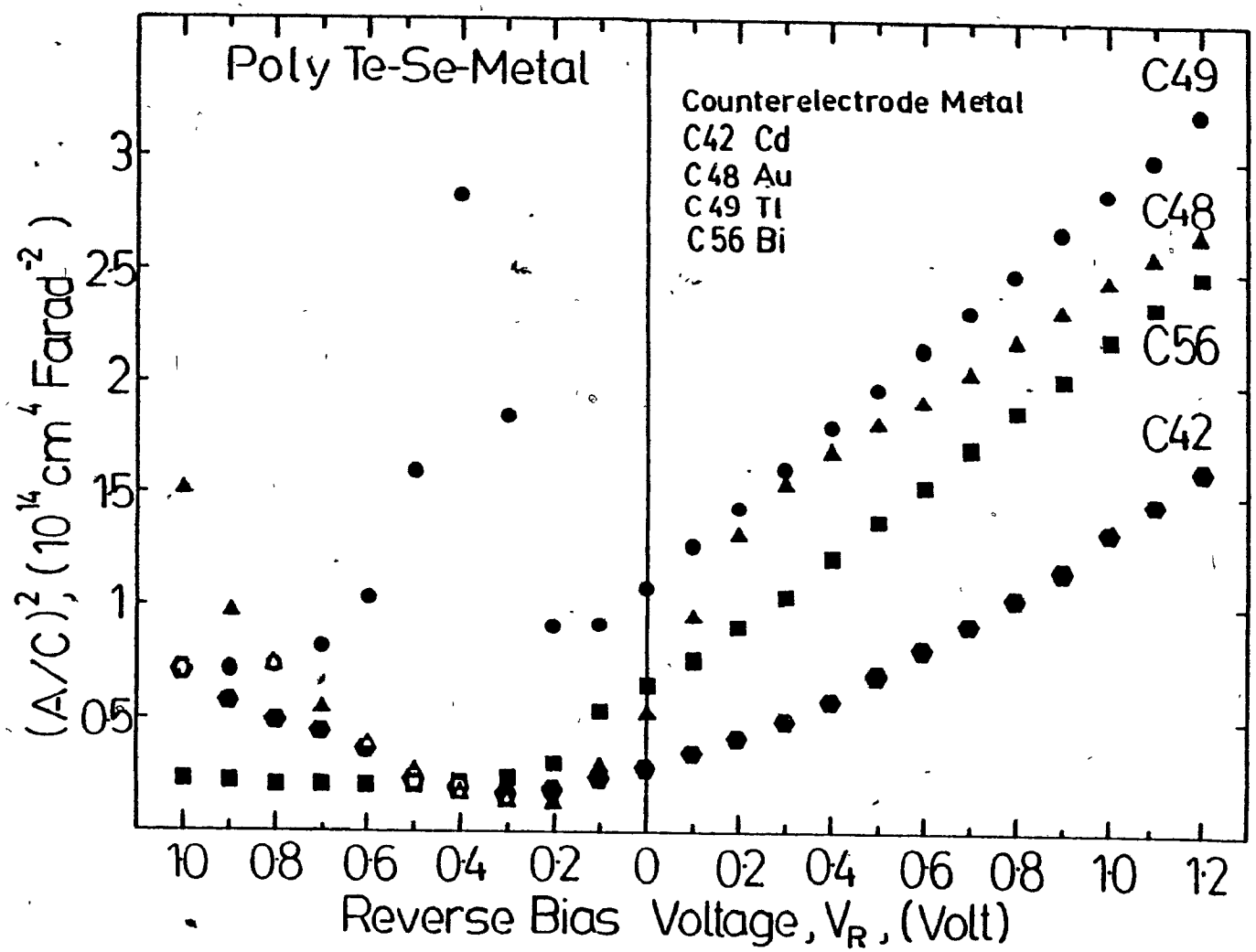

Fig. 5.12 Comparison of $(A/C)^2$ versus V_R plots of 4 polycrystalline Te-Se-metal structures with different counterelectrode materials.

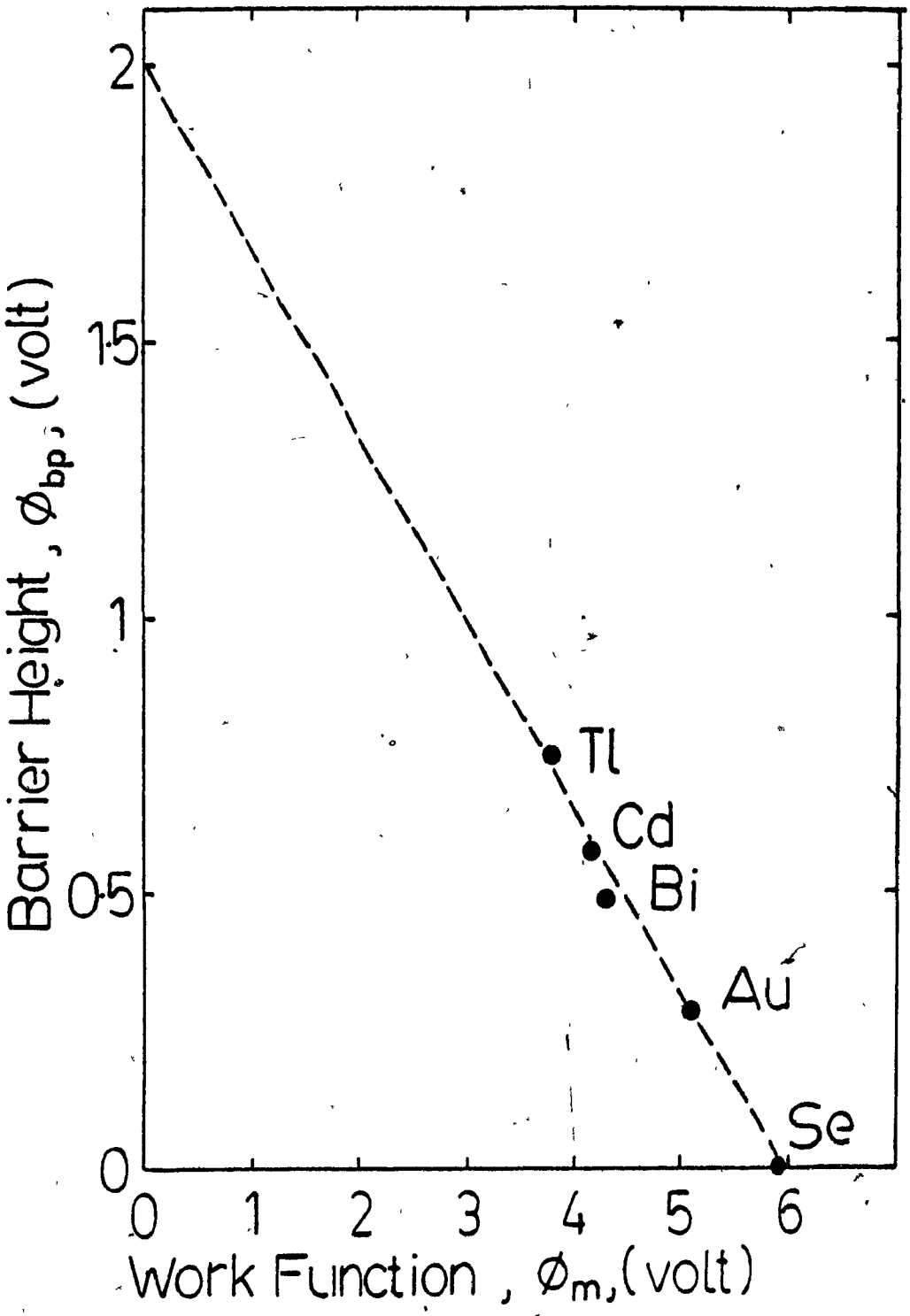

Fig. 5.13 Plot of barrier height, calculated from capacitance results, versus reported work function of the counterelectrode material.

CHAPTER 6

POST-FABRICATION HEATING OF Se-Tl DIODES

6.1 Introduction

The results on Se-Tl structures described in Chapter 5 were for samples immediately after fabrication . However, the electrical characteristics of these samples changed with time when stored in air. Furthermore, it was found that during the soldering stage of attaching fine copper wires to the thallium areas with Wood's metal, if the heating action was too long, or the soldering iron temperature too high, the results of measurement showed that the forward current density was reduced and the general slope of the current density-voltage curve was also decreased. It was thus apparent that post-fabrication heat treatment adversely affected at least the forward characteristics of these diodes. Accordingly, a study was made to feature the changes in electrical characteristics with heat treatment of samples in nitrogen. The present chapter describes these studies.

6.2 Experimental Procedure

Electrical measurements of current density versus voltage and capacitance versus voltage were first taken

immediately after the fabrication of the Al-Bi-Se-Tl structure. Then, the electrical wires and Wood's metal were removed from the sample, which was placed in a Pyrex tube located within an oven (Fig. 6.1). Nitrogen gas (industrial grade purity) was passed through the tube and a thermometer, placed near the sample, was used to monitor the annealing temperature. After maintaining the temperature at a fixed value for 2 hours, the sample was taken out and the same set of measurements was repeated. A total of six samples were heat-treated at temperatures of 130, 140, 155, 170, 180 and 195°C.

6.3 Dark Current Density-Voltage Characteristics

Fig. 6.2 shows a comparison of current density versus voltage plots for the Se-Tl structures before and after the heat treatments. It is apparent that after annealing, the current density decreases considerably and that the amount of the decrease increases with increase of annealing temperature. The slopes at low forward bias voltage are appreciably reduced, corresponding to a change in ideality factor from $n=1.2$, before annealing, to a value of 2 or more afterwards. The ratio of current density at 1 V forward, measured after heat treatment to that measured before, is plotted against temperature in Fig. 6.3, where it is seen that the decrease amounts to some three orders of magnitude for the heat treatment at 195°C.

6.4 Capacitance-Voltage Measurements

Fig. 6.4 shows the results of measurements of capacitance versus reverse bias voltage. It is seen that the capacitance was significantly reduced after the heat treatment at all values of reverse voltage. This is brought out more easily in the plot of the ratio of the capacitance, measured after annealing at zero bias to that before, against annealing temperature in Fig. 6.5, which shows a decrease of more than an order of magnitude for the 195°C case.

The capacitance results are re-plotted in Fig. 6.6 as $(A/C)^2$ versus reverse bias voltage V_R. The measurements before heat treatment are approximately straight lines, which converge to an extrapolated intercept on the voltage axis near V_R=-0.6 volt. The slopes correspond to a hole concentration of about 5×10^{16} cm^{-3} in the selenium. The results of only four samples after annealing are shown because of the very large $(A/C)^2$ values of the other two samples. All of these lines for the annealed samples are non-linear curves and show much steeper slopes than those for the samples before annealing. The latter fact suggests that the carrier concentration is reduced by the heat treatment.

6.5 Post-Fabrication Heating of Se-Bi and Se-Au Structures

Although the present study of heat treatment was focused on Se-Tl structures, some preliminary results were also obtained from heat treatment of Se-Bi and Se-Au samples.

Fig. 6.7 shows results of j-V characteristics of a Bi-Se-Bi structure before and after heat treatment at 110°C for 2 hours in nitrogen. It is noted that even though the back contact and the counterelectrode were of the same material, the sample gave a large rectification ratio of 4 decades at 1 volt before heat treatment. The results after heat treatment show a much smaller rectification ratio, a lower forward current density at 1 volt and, from a linear current-voltage plot (not shown), an almost ohmic current-voltage dependence.

Fig. 6.8 presents the measurements of j-V characteristics of a Au-Se-Au structure (C35) before and after heat treatment in nitrogen at 3 different temperatures of 120, 160 and 190°C. All the measurements show a small rectification ratio of around one decade at 1 volt, together with an increase of forward current density with increase of annealing temperature. The results at 120°C (2 hrs.) are an exception to this. The trend thus shows that heat treatment enhanced the conductivity of the Au-Se contact. A plot of $(A/C)^2$ versus V_R for this sample in Fig. 6.9 shows that, while the heat treatment increased the slope, the extrapolated intercept on the voltage axis was not altered.

Since the slope increase suggests a decrease of carrier concentration, the increase of conductivity with annealing must arise from increased carrier mobility.

6.6 Discussion of Heat-treatment Results

The changes observed after heat treatment in the Se-Tl structures could be attributed to the formation of an interfacial layer, presumed to be thallium selenide, at the Se-Tl interface (Fig. 6.10). Thallium selenide (TlSe) is a semiconductor with an energy gap of about 0.7eV [12] [13]. Thus, the heat treatment process would change the structure from a Schottky junction to a heterojunction.

The current density-voltage characteristics show a drastic change of ideality factor before and after annealing. This trend could be explained by the formation of a heterojunction after heat treatment. Because of differences in lattice parameters between Se and TlSe, energy traps would be produced at the interface [14]. These interface states make carrier recombination a dominant current transport process, which in turn alters the value of n.

The transition from a Se-Tl Schottky junction to Se-TlSe heterojunction would cause the depletion region to extend from the Se film into the TlSe layer and, therefore, decrease the capacitance at a given voltage. The results from the capacitance-voltage characteristics clearly show this decrease. The $(A/C)^2$ versus V_R plots after heat treatment

show much steeper slopes which suggest that the carrier concentration was decreased. If this concentration corresponds to the TlSe, it is much less than that in the Se. The carrier concentration for the samples heat treated at 170 and 195°C has a value of 6×10^{14} cm^{-3} compared with 5×10^{16} cm^{-3} for selenium before heat treatment. The smallest measured value of capacitance, corresponding to the largest depletion width, occurs at 1.2 volt on the sample annealed at 195°C. The estimated depletion width according to this value is 3 microns. Since the capacitance seems to decrease with further increase of forward voltage, the thickness of the TlSe layer must be larger than 3 microns, which, therefore, could be observed under the microscope. An alternative interpretation for the increase of the slopes of the $(A/C)^2$ plots, is a decrease of acceptor concentration in the selenium, due to out-diffusion.

In the case of the Se-Bi structure, it is possible that the heating caused formation of Bi_2Se_3, which is a low gap semiconductor, whose presence would reduce the rectification. In the case of the Se-Au structure, it is possible that a selenide was also formed.

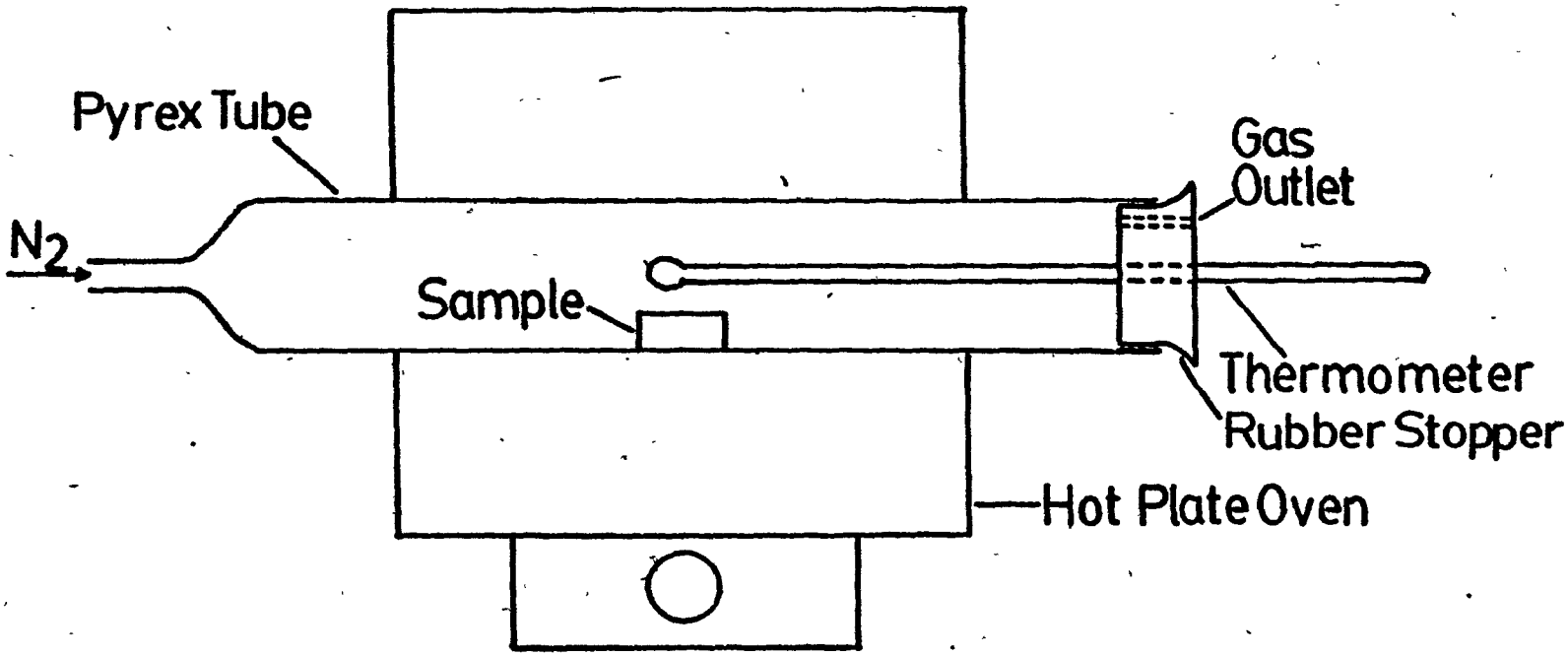

Fig. 6.1 Experimental arrangement used for heat treatment studied.

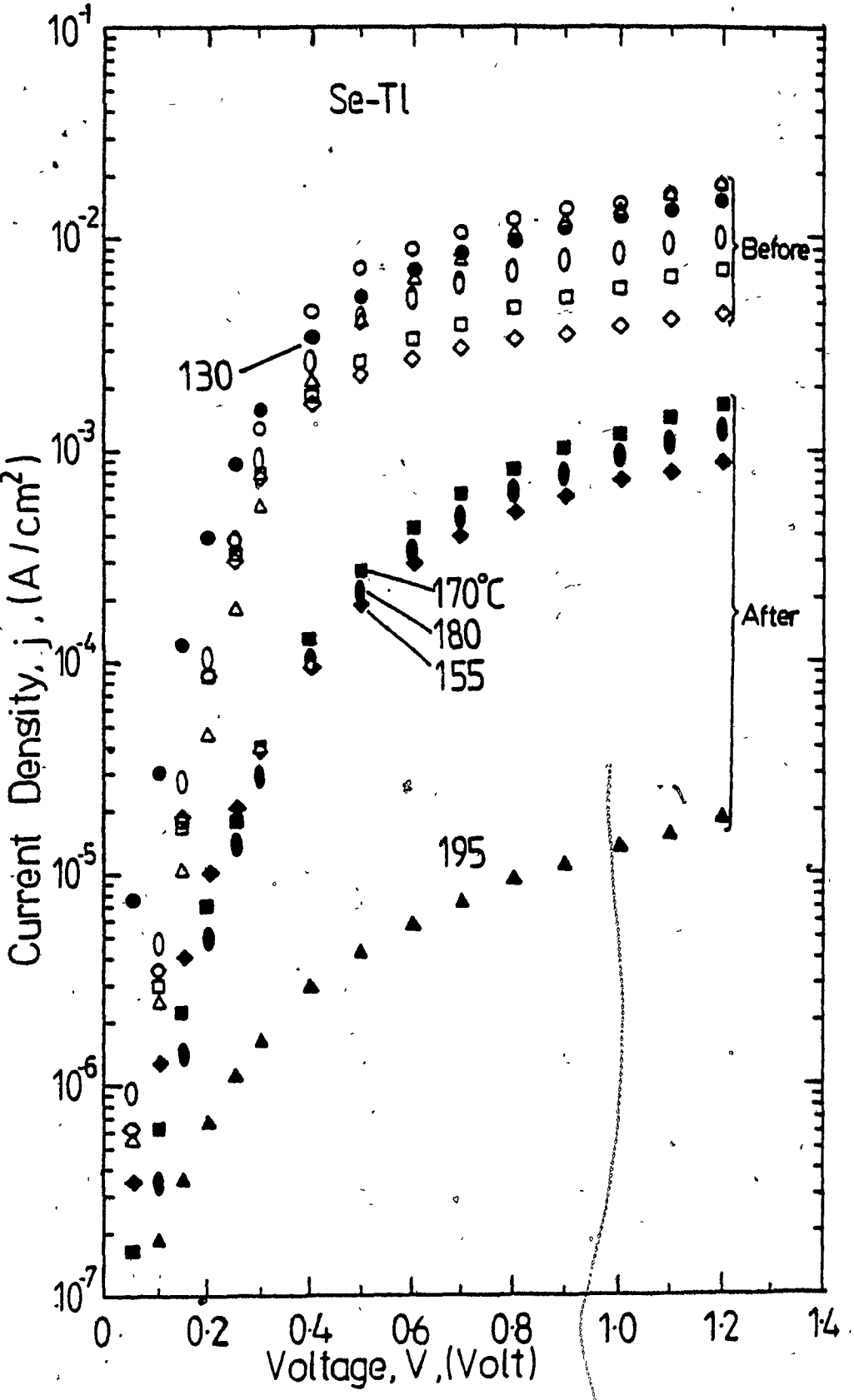

Fig. 6.2 Plot of the logarithm of current density versus voltage for Se-Tl diodes before and after 2 hours of heat treatment in N_2.

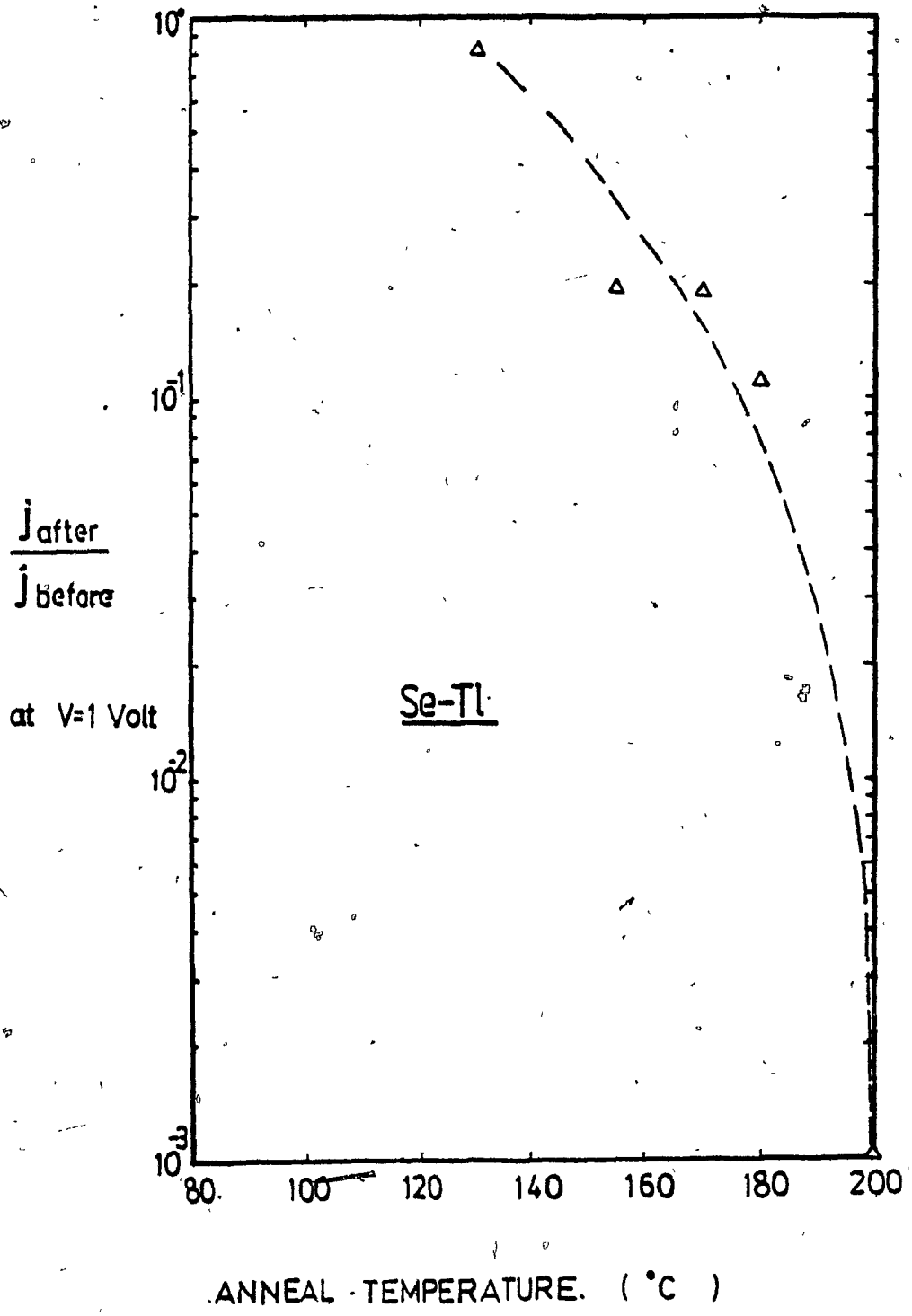

Fig.6.3 Plot of the ratio of current after to that before heat treatment against annealing temperature, for Se-Tl samples.

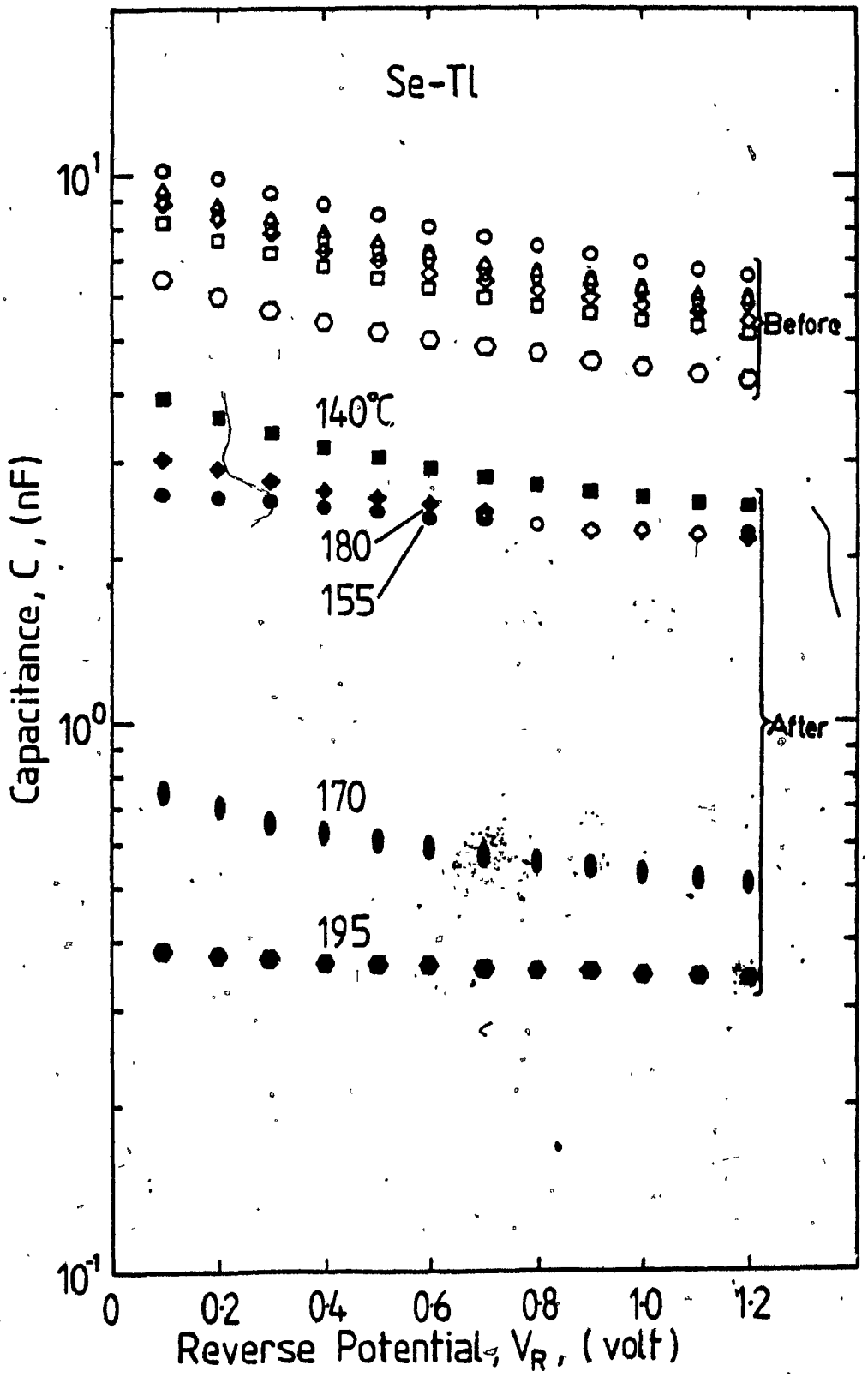

Fig. 6.4 Plot of incremental capacitance versus reverse bias voltage for the Se-Tl samples before and after 2 hours of heat treatment in N_2.

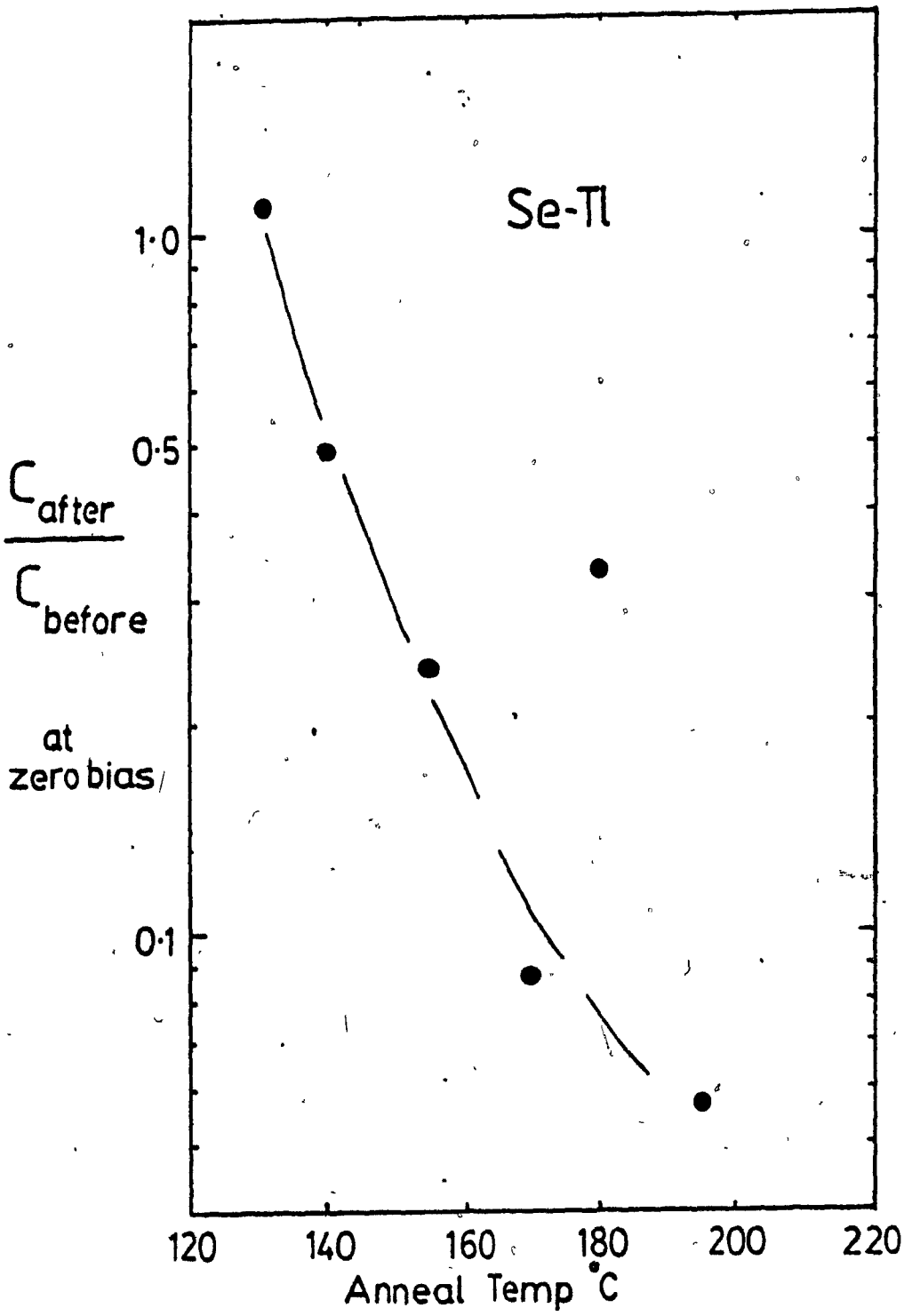

Fig. 6.5 Plot of ratio of capacitance after to that before heat treatment versus annealing temperature, for Se-Tl samples.

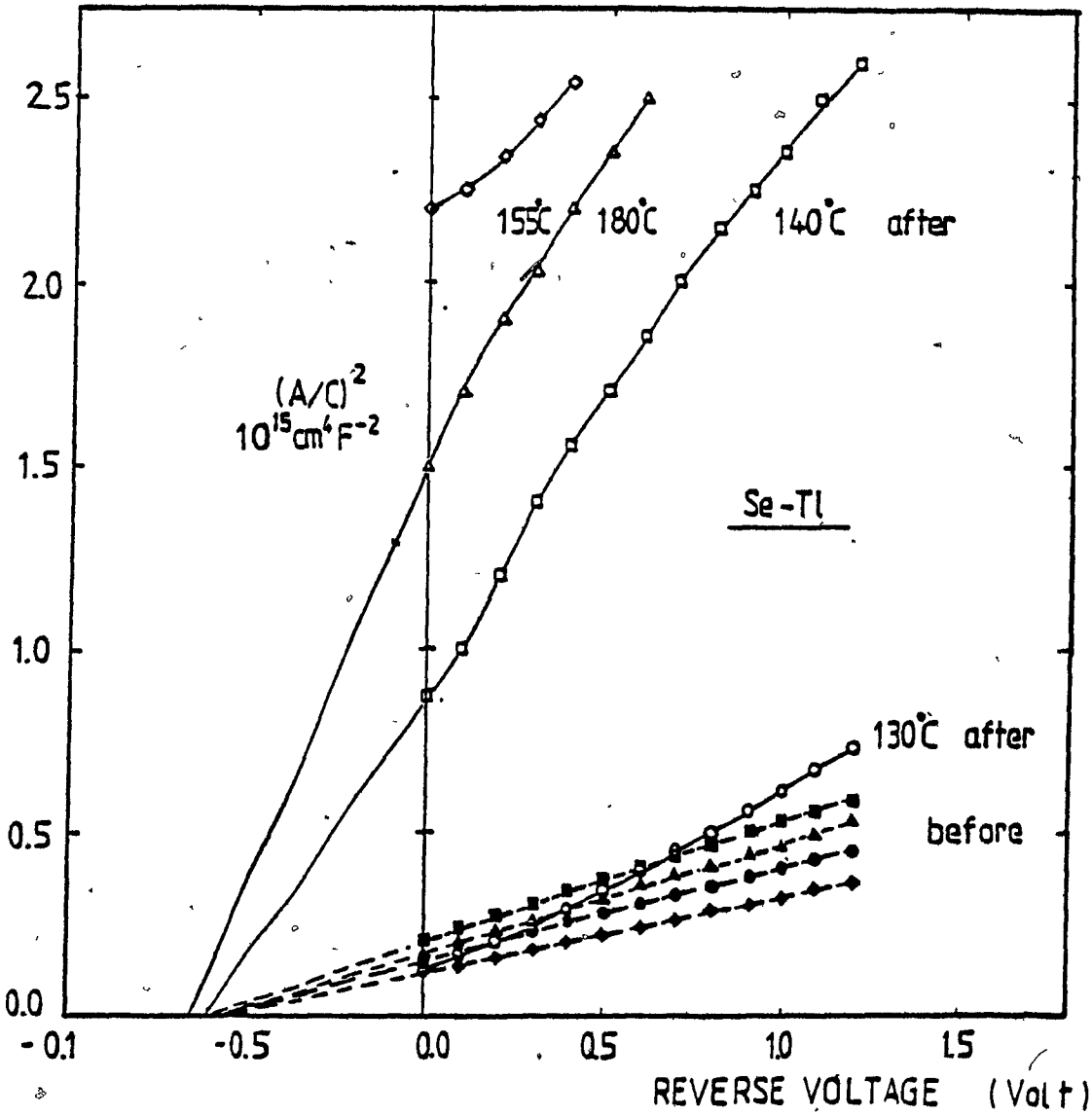

Fig. 6.6 Plot of $(A/C)^2$ versus reverse bias voltage for four Se-Tl samples before and after heat treatment.

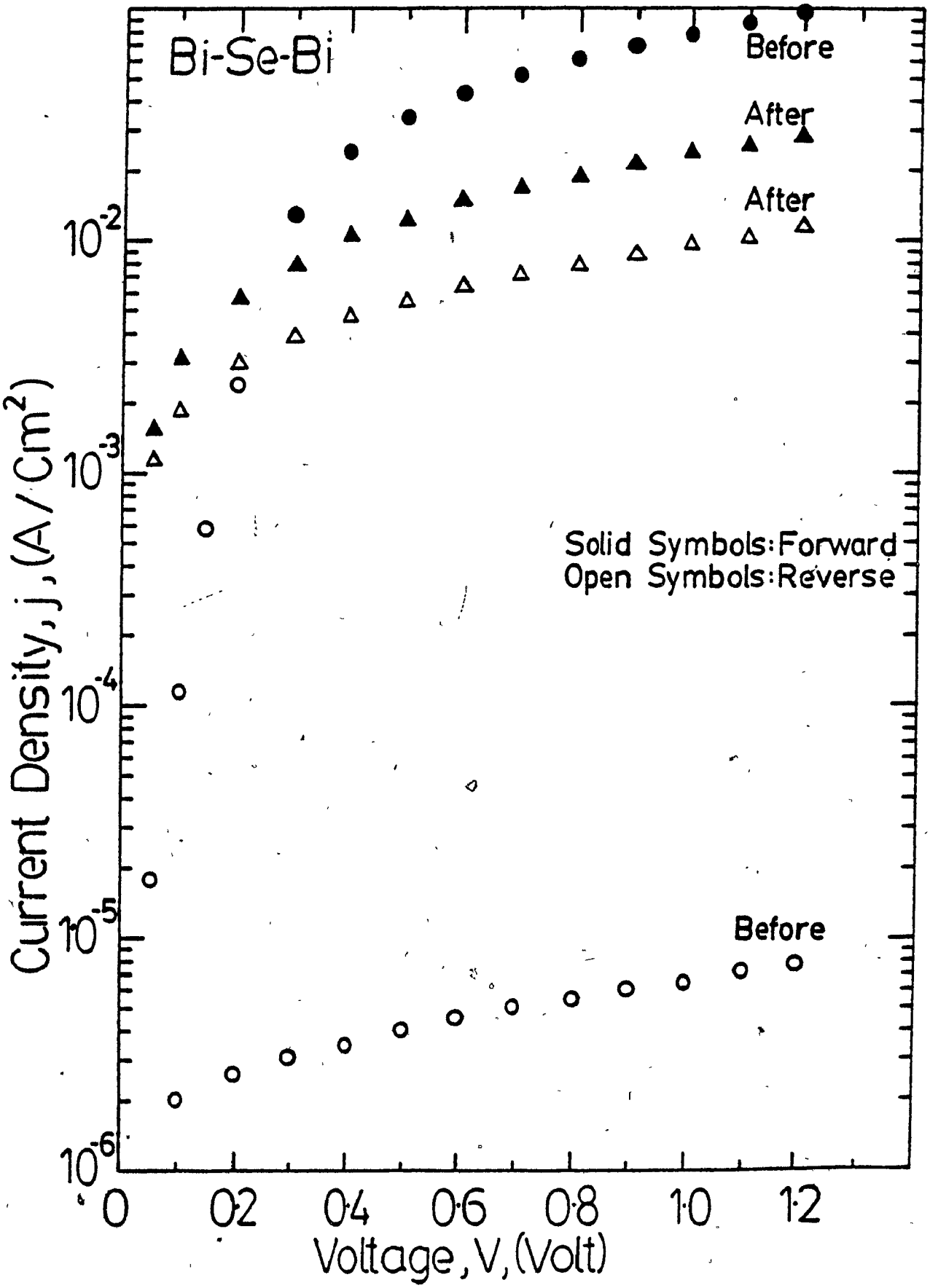

Fig. 6.7 Plot of ln(j)-V characteristics on Bi-Se-Bi sample (C28) before and after heat treatment at 110°C for 2 hours in N_2.

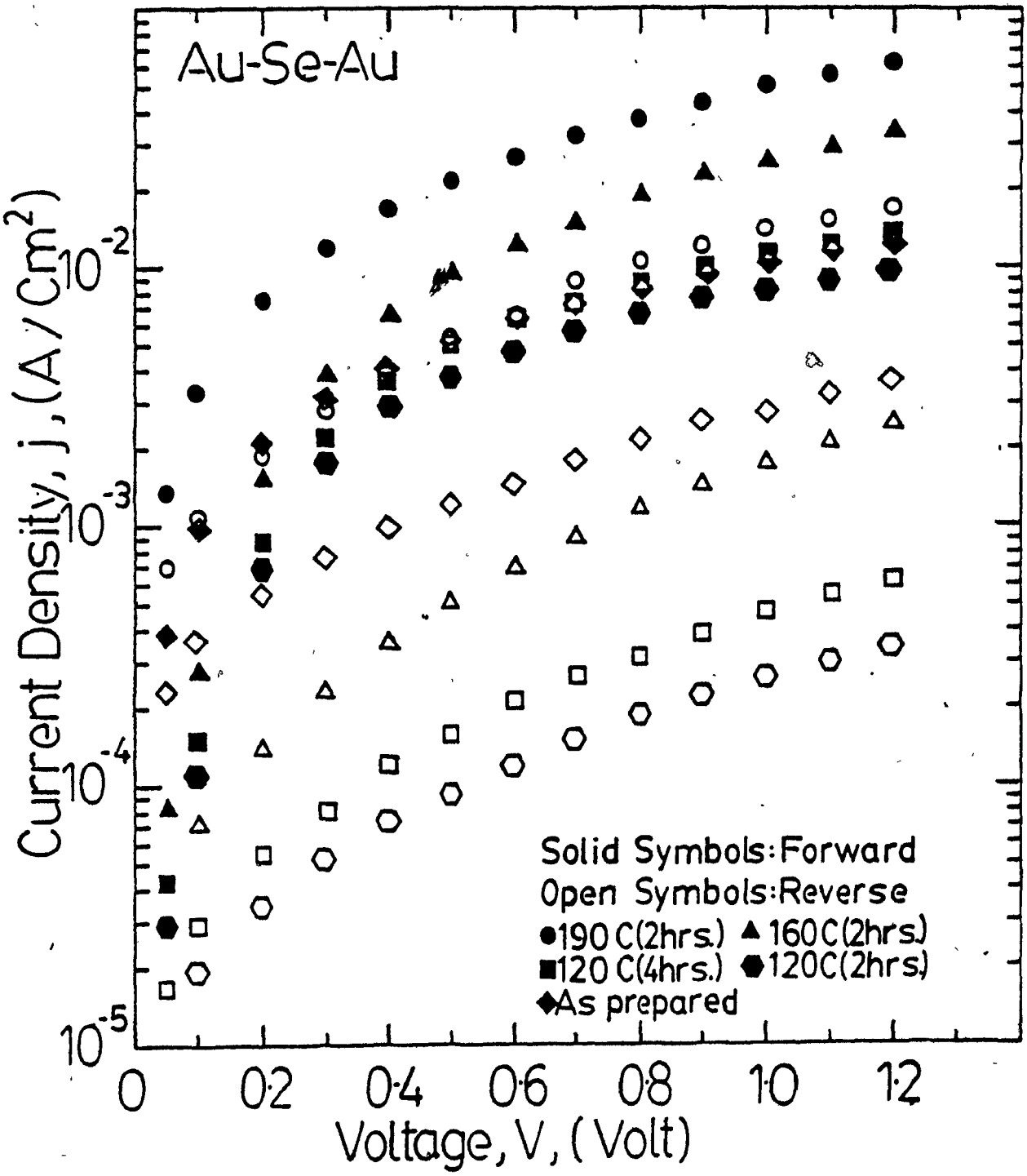

Fig. 6.8 Plot of ln(j)-V characteristics on Au-Se-Au sample (C35) before and after heat treatments.

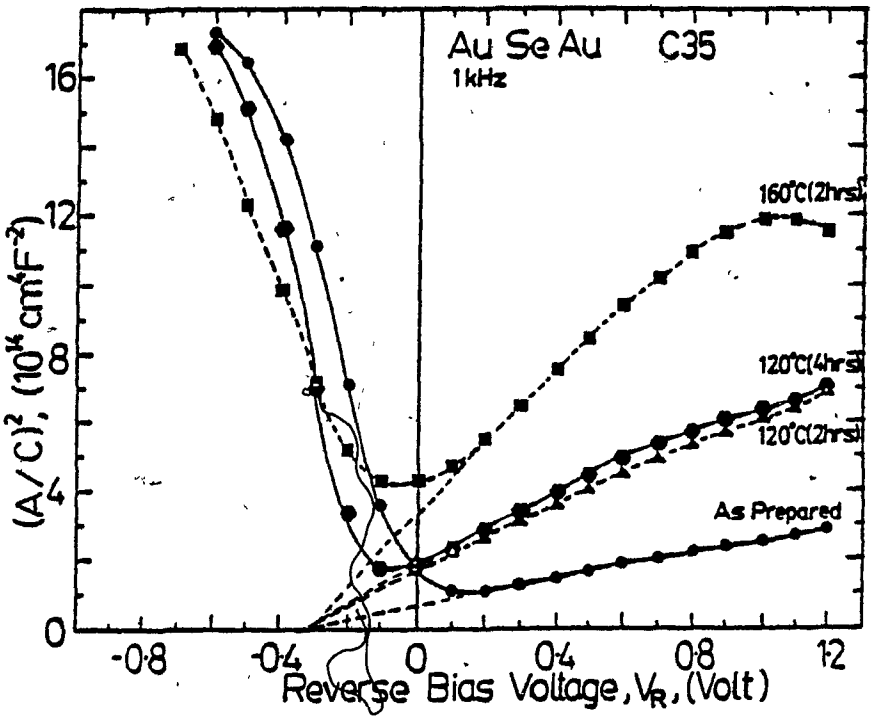

Fig. 6.9 Plot of $(A/C)^2$ versus reverse bias voltage on Au-Se-Au sample (C35) before and after heat treatments.

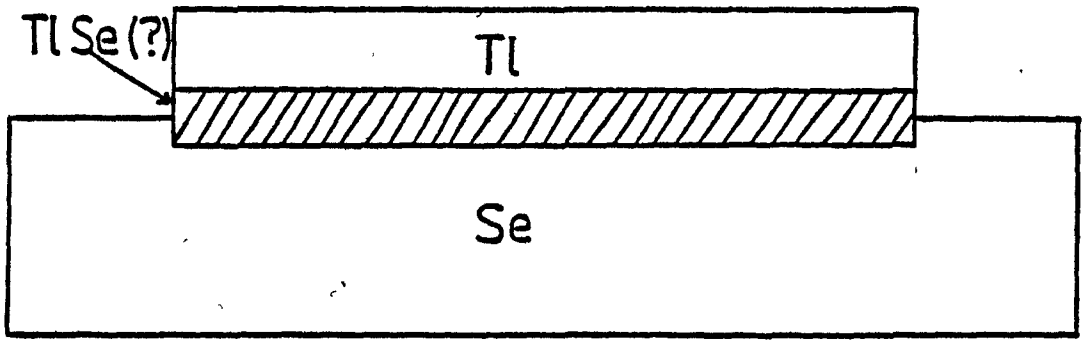

Fig. 6.10 Cross-sectional view of the interface between Tl and Se after heat treatment, showing a possible TlSe layer.

CHAPTER 7

BIAS AND FREQUENCY DEPENDENCE OF CAPACITANCE

7.1 Introduction

This chapter presents the dependence of capacitance of the diode structures on bias and frequency and that of resistance on frequency as well. While Mott-Schottky plots were shown in chapter 5 to obtain data for barrier height determination, the data in the present chapter is displayed simply as capacitance versus bias voltage at fixed frequencies or capaciatnce (or resistance) against frequency at zero bias. The capacitance results given for forward bias in this chapter should be regarded as somewhat preliminary, since such measurements in this high conductance region are relatively inaccurate.

7.2 Capacitance-Voltage Variation

7.2.1 Se-Cd Structures

Fig. 7.1 shows plots of capacitance against reverse voltage of a polycrystalline Te-Se-Cd structure (C42), measured at four different frequencies (100Hz, 1kHz, 10kHz and 100kHz). At all frequencies, the capacitance decreases with increasing reverse voltage, starting from a maximum in the forward direction. The capacitance decreases with

increasing frequency at all voltages. Fig. 7.2 shows capacitance-voltage plots for a single crystal Te-Se-Cd sample (C50). The results are somewhat similar to those of the polycrystalline sample shown in Fig. 7.1, except, firstly that the capacitance values in the reverse direction are less than half those for sample C42 and secondly that the variation at 100Hz is much larger for forward bias.

7.2.2 Se-Au Structures

Fig. 7.3 shows plots of capacitance-voltage characteristics measured at four different frequencies (100Hz, 1kHz, 10kHz and 100kHz) for a polycrystalline Te-Se-Au structure (C48). While at the higher frequencies, capacitance decreases with increasing reverse bias V_R, at 100Hz it first decreases to a minimum near V_R=0.2 volt and then increases. In the forward direction (negative V_R), there is a maximum for the 100Hz and 1kHz results near V_R=-0.2 volt.

Plots are shown in Fig. 7.4 of capacitance versus reverse voltage, measured at four different frequencies (100Hz, 1kHz, 10kHz and 100kHz) on another polycrystalline Te-Se-Au structure (C62). The results here were taken about a year after fabrication. At higher frequencies, the capacitance for the most part decreases with increasing reverse voltage. However, it is noted that a minimum occurs near V_R=0.1 volt at frequencies of 10kHz or less. This

minimum is particularly pronounced at 100Hz, at which frequency there is a second minimum around V_R=0.6 volt.

In Fig. 7.5, capacitance-voltage results are shown for yet another polycrystalline Te-Se-Au sample (C65), which was fabricated with different areas of Wood's metal (see inset to Fig. 7.5), deposited on the top of the gold counterelectrode areas. The results of both areas A1 (0.14 cm^2) and A2 (0.06 cm^2) were measured at 100Hz and 1kHz. It can be seen that at 100Hz, the capacitance of A1 is lower than that of A2 in the reverse direction, but the broad minima for both the 100Hz curves occur over the same range of voltage, near 0.6 volt. It is noted that this sample, in contrast to samples C48 and C62, shows no minimum at small V_R for 100Hz. At all frequencies, however, there is a maximum of capacitance for forward bias.

A comparison of the results on the three samples C48, C62 and C65 is given in Fig. 7.6 for a frequency of 100Hz. As mentioned previously, two of the diodes show minima near V_R=0.2 volt and all three show a maximum in the forward direction.

Earlier in chapter 6, a plot of $(A/C)^2$ versus V_R was shown (Fig. 6.9) for a Au-Se-Au sample after heat treatment. Fig. 7.7 shows capacitance against reverse voltage for the same sample (C35) at 1kHz before and after the heat treatment. It is noted that the capacitance generally decreased with annealing and the voltage of the maximum shifted from reverse to forward bias. Furthermore, no

minimum of capacitance was observed at any voltage for this sample.

7.2.3 Se-Tl Structures

Fig. 7.8 exhibits plots of capacitance versus reverse voltage for a fairly typical freshly-made Bi-Se-Tl sample (C43), measured at four different frequencies (100Hz, 1kHz, 10kHz and 100kHz). At all frequencies, the capacitance decreases from a maximum in the forward direction with increasing reverse voltage. With increasing forward voltage, following the maximum, there is a minimum, which occurs at all frequencies. This minimum is more pronounced at lower frequencies but hardly exists at 100kHz.

In Fig. 7.9, capacitance results measured at 100Hz on eight Se-Tl samples are compared. In the reverse direction, all show a gradual decrease of capacitance as reverse voltage increases. In the forward direction, maxima occur near V_R=-0.1 volt for all samples, followed by a sharp decrease around V_R=-0.2 volt to -0.3 volt. At least three samples (C43, C54 and C55) also show minima around V_R=-0.3 volt. It may be noted from Fig. 7.9 that the highest values of capacitance were observed using polycrystalline tellurium as the back contact material.

Fig. 7.10 shows a similar plot of capacitance against reverse voltage for eleven Se-Tl structures measured at 1kHz. As indicated, all samples show in the forward direction

maxima near V_R=-0.15 volt and minima between -0.3 and -0.45 volt.

Fig. 7.11 is a comparison of capacitance measurements at 1kHz for three Se-Tl samples with different back contact materials between the selenium layer and the aluminum stud surface. These consist of samples C49 with polycrystalline tellurium as the back contact material, C37 with bismuth and C57 with single crystal tellurium. Although the magnitude of capacitance is different from one sample to another, the maximum for all three samples occurs at about the same voltage of V_R=-0.15 volt. Samples C49 and C37 also show a prominent minimum at about -0.4 volt. As in Fig. 7.10, the sample with polycrystalline tellurium as the back contact shows the highest capacitance.

Fig. 7.12 shows plots of capacitance-voltage measurements for two polycrystalline Te-Se-Tl samples (C45 and C49). The inset depicts the corresponding plots of current density against voltage. Sample C49 shows a rectification ratio of 5 decades at 1 volt, compared with about 2.5 decades for sample C45. Their maximum capacitance values both occur at about V_R=-0.15 volt. However, sample C49, a relatively better rectifier, shows a somewhat more pronounced minimum than that of sample C45, although the effect is not strong.

Fig. 7.13 displays capacitance-voltage plots at 1kHz on two Bi-Se-Tl samples (C43 and C37), which were heat-treated at 155 and 170°C respectively. Both samples show prominent capacitance variation before heat treatment, whereas this and

the magnitude of capacitance both decrease substantially afterwards. Furthermore, after annealing the minimum in the forward direction has disappeared.

7.3 Capacitance-Frequency Variation

7.3.1 Se-Cd Structures

Fig. 7.14 is a plot of incremental capacitance and incremental resistance versus frequency for a Bi-Se-Cd sample (C27). At low frequency, the capacitance decreases only slightly with increasing frequency but beyond about 100kHz, the decrease becomes greater. The total capacitance decrease is more than one decade up to a frequency of a megahertz. The decrease of resistance is very much larger, amounting to more than four decades over the same frequency range.

Fig. 7.15 shows capacitance and resistance versus frequency results for three Bi-Se-Cd samples (C29, C30 and C33), which were fabricated with the selenium deposited with different substrate temperatures of 140, 90 and 80°C. The samples prepared at 90 and 140°C show a similar initial variation with frequency. However, sample C33, fabricated at 80°C shows an initial decrease of capacitance to a plateau between about 1kHz and 10kHz, beyond which it decreases like sample C30, prepared at 90°C. The resistance of sample C33 also decreases with a tendency to a plateau around 1kHz and thereafter decreases rapidly with increasing frequency. Apart from these differences, the capacitance and resistance

values have much the same order of magnitude, despite the fact that selenium deposited at 80°C is amorphous and that at 140°C is polycrystalline.

7.3.2 Se-Bi Structures

Plots of capacitance and resistance versus frequency for two Se-Bi samples (C28 and C56) are shown in Fig. 7.16. Sample C56 was prepared with polycrystalline tellurium as the back contact material, while sample C28 used bismuth. Both capacitance curves show initially a slow decrease to about 100kHz. At low frequency, sample C56 shows a capacitance about twice that of sample C28 and a resistance almost an order of magnitude smaller. As in the case of the Se-Cd diodes, the decrease of resistance over the frequency range is much larger than that for the capacitance.

7.3.3 Se-Au Structures

Plots of capacitance and resistance versus frequency are shown in Fig. 7.17 for a Bi-Se-Au structure (C26) and a Au-Se-Au structure (C35). Sample C26 shows a decrease of capacitance with frequency around 1kHz to a plateau between about 4kHz and 100kHz, with a slow decrease beyond. The capacitance of sample C35 on the other hand decreases only slowly at low frequency but shows a larger decrease beyond 10kHz. The resistance curves of both samples show little variation with frequency at low frequency, with a larger

decrease beyond 10kHz for sample C35 and 100kHz for sample C26.

Fig. 7.18 show capacitance-frequency plots of a polycrystalline Te-Se-Au sample (C64) with 3 different gold areas, A1 (0.14 cm^2), A3 (0.03 cm^2) and A4 (0.015 cm^2) (see diagram in inset). All three curves show an initial decrease of capacitance at low frequency, with the two smaller areas A3 and A4 showing the more pronounced decrease. With further increase of frequency, the capacitance decreases more slowly in a plateau region and then shows a larger decrease beyond 100kHz. It is noted that area A1 gives the smallest value of capacitance at low frequency but the largest value at higher frequency. At the highest frequency of 1MHz, the capacitance of all three areas seem to converge together.

Fig. 7.19 shows capacitance and resistance versus frequency for a polycrystalline Te-Se-Au sample (C65) with four different Wood's metal contact areas, A1 (0.14 cm^2), A2 (0.06 cm^2), A3 (0.03 cm^2) and A4 (0.015 cm^2), but the same area of gold (0.14 cm^2), as indicated in the inset. All four areas show a decrease of capacitance at low frequency, with a plateau between about 2kHz and 100kHz, beyond which the capacitance decreases more rapidly, with convergence towards the highest frequency of 1MHz. It is noted that at higher frequency, A1 gives the largest capacitance as expected, followed by A2, A3 and A4 in that order. The values of resistance for all four areas are seen to show little change at low frequency and only begin to decrease near 100kHz with

convergence near 1MHz. The resistance is highest for area A4 as might be expected.

Fig. 7.20 shows plots of capacitance measured at 10kHz and 100kHz versus area for the samples C64 and C65. It should be noted that the areas corresponded to the gold counterelectrodes for sample C64 but to the Wood's metal contact areas for sample C65. It is observed that there is a linear relationship between capacitance and the size of the gold area for sample C64 at both frequencies. For sample C65, the capacitance increases with area of the Wood's metal contact but, in this case, the curves are non-linear.

7.3.4 Se-Tl Structures

Capacitance and resistance versus frequency plots for a typical polycrystalline Te-Se-Tl sample (C48) are shown in Fig. 7.21. It is observed that the capacitance decreases slowly at low frequency but shows a larger decrease of more than one decade beyond 100kHz. As for the Se-Cd and Se-Bi diodes, the decrease of resistance with frequency is much greater, amounting to more than four decades.

7.4 Summary of Results of Variation with Bias and Frequency

In respect of the plots of variation with bias, it is clear that generally speaking the capacitance at higher frequencies decreased in a regular way with increasing V_R. This fact was already used in chapter 5, in the plots of

$(A/C)^2$ versus V_R. However, at low frequencies, anomalous capacitance dips were observed for the Se-Tl, Se-Bi (not shown) and Se-Au diodes. These anomalous minima occurred at a forward bias for the Se-Tl samples and at a reverse bias for two of the Se-Au samples. For the Se-Cd diodes, however, no anomalous minima were observed.

The data for the Se-Tl diodes, which were measured on freshly made samples, showed higher capacitance for samples made using polycrystalline tellurium as the back contact material. This result would seem to be generally consistent with the fact (indicated in Fig. 5.5(b)) that the lowest series resistance occurred in these same samples.

In respect of variation with frequency, the decrease of incremental capacitance over the range 100Hz to 1MHz was generally much less than that for incremental resistance, at least for the Se-Cd, Se-Bi and Se-Tl samples. The resistance decrease can generally be understood in terms of a junction shunt resistance, which is by-passed at higher frequency by the junction capacitance, so that at higher frequency a series resistance of lower value becomes important. A circuit model for this is considered in Chapter 8.

The C-f and R-f results on the Se-Cd samples, where the selenium was deposited at different substrate temperatures, indicate not only a relatively small difference between the devices with amorphous and crystalline selenium but also that the crystalline sample gave the highest shunt resistance value at 100Hz and not the amorphous sample, as one might

have expected. Furthermore, the resistance of the samples at high frequency, which may be taken as series resistance values, were of similar magnitude for all three.

The C-f and R-f data for the Se-Au samples were rather different from those for the Se-Cd, Se-Bi and Se-Tl samples. Firstly, the variation of resistance with frequency was much less, amounting to only about a decade over the frequency range, rather than the approximate four decades observed for the other samples. Secondly, the capacitance at 100Hz was much larger and showed an initial decrease with increasing frequency. Thirdly, this larger value of capacitance at low frequency was more pronounced for the smaller gold areas. At higher frequencies, however, the capacitance scaled correctly with the gold areas.

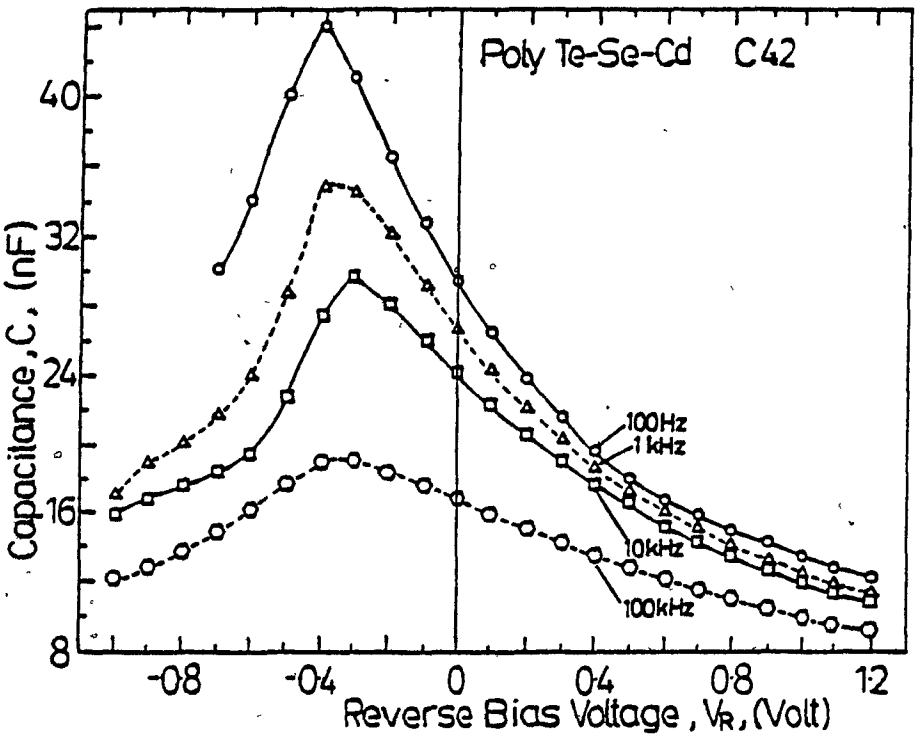

Fig. 7.1 Plot of capacitance against reverse voltage for polycrystalline Te-Se-Cd sample (C42) at four different frequencies.

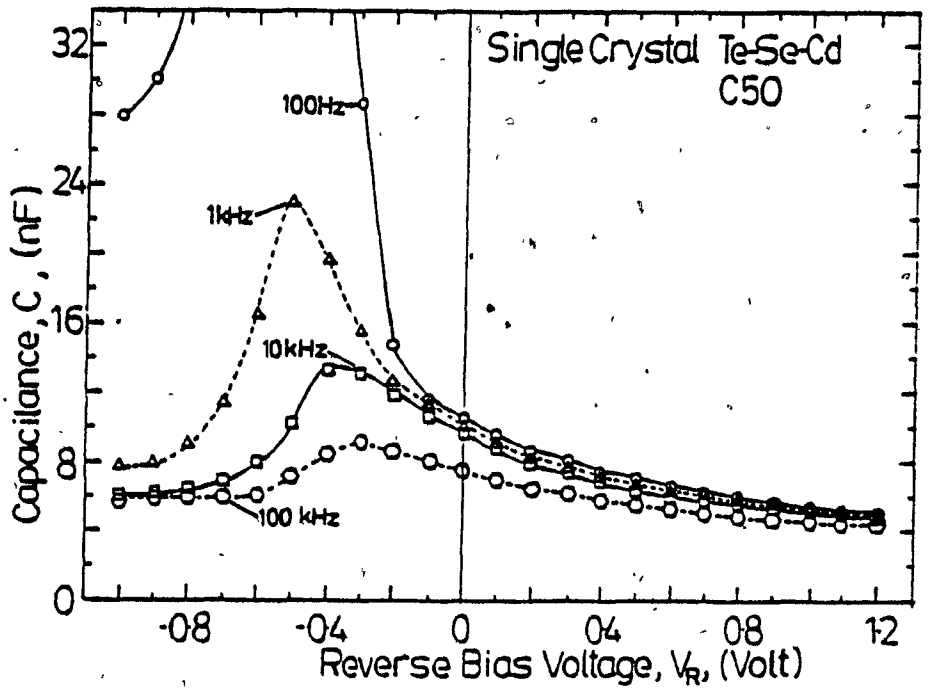

Fig. 7.2 Plot of capacitance against reverse voltage for single crystal Te-Se-Cd sample (C50) at four different frequencies.

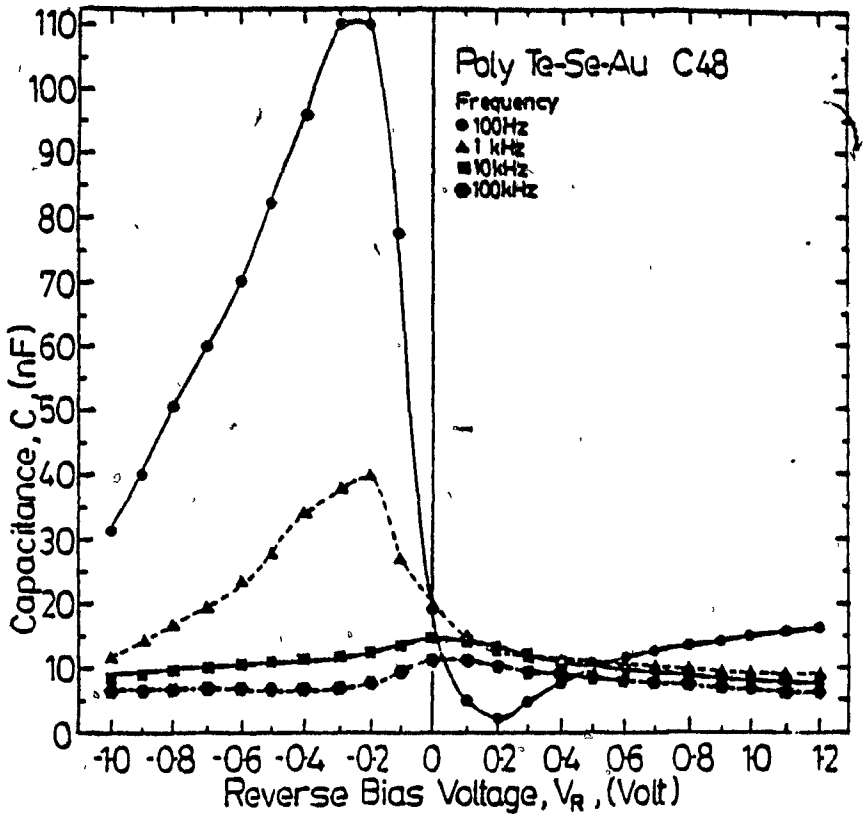

Fig. 7.3 Plot of capacitance against reverse voltage for polycrystalline Te-Se-Au sample (C48) at four different frequencies.

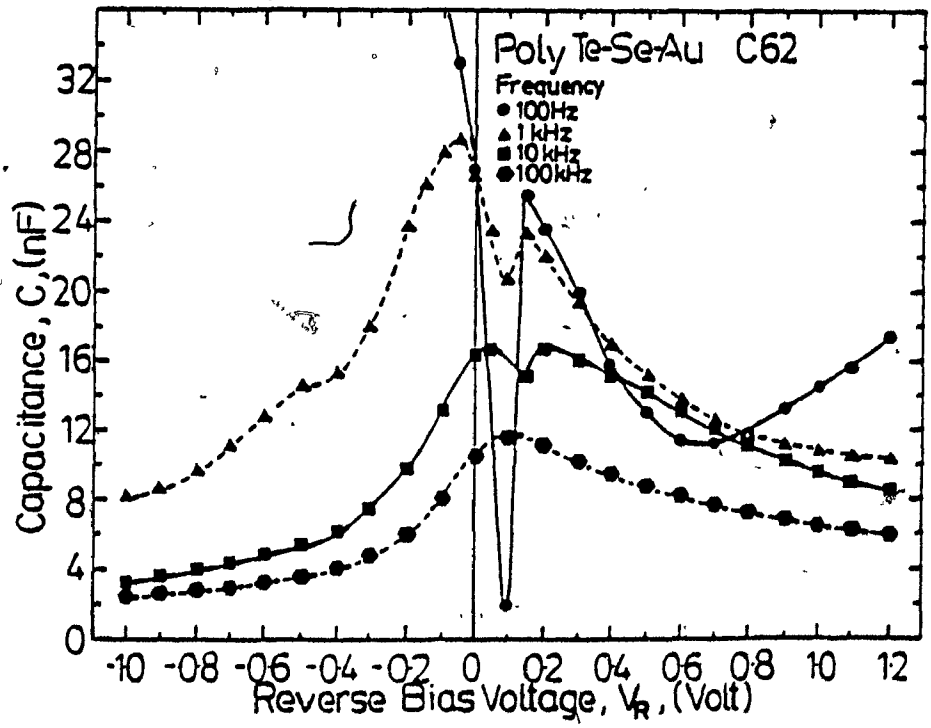

Fig. 7.4 Plot of capacitance against reverse voltage for polycrystalline Te-Se-Au sample (C62) at four different frequencies.

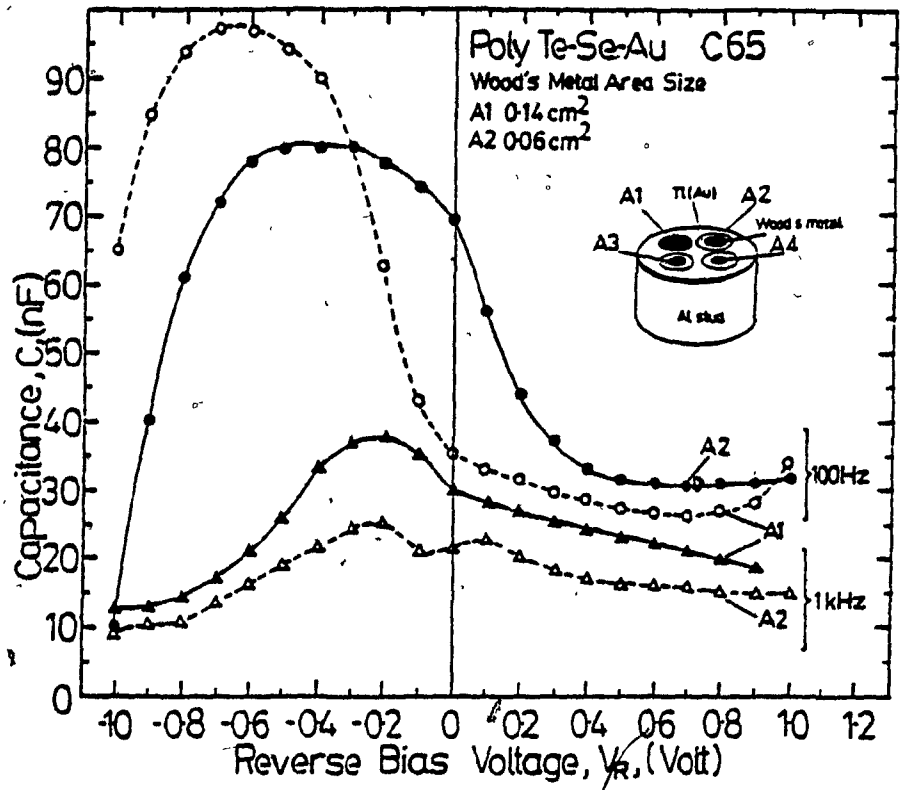

Fig. 7.5 Plot of capacitance against reverse voltage for polycrystalline Te-Se-Au sample (C65) at 100Hz and 1kHz on two of the Wood's metal contact areas A1 and A2.

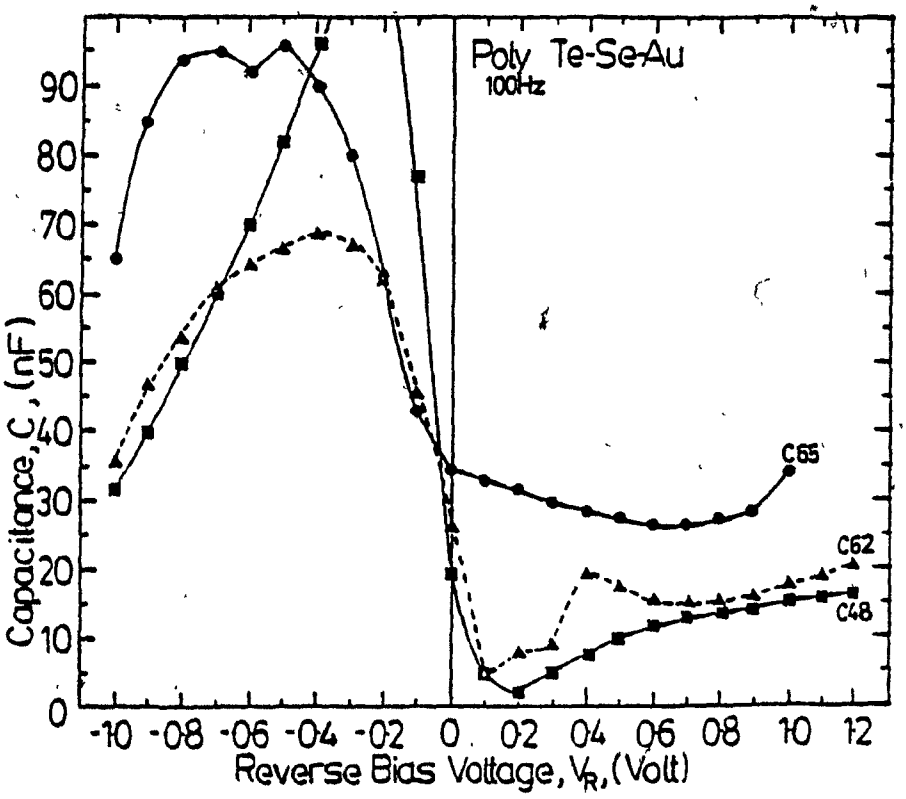

Fig. 7.6 Plot of capacitance as a function of bias at 100Hz for three polycrystalline Te-Se-Au samples.

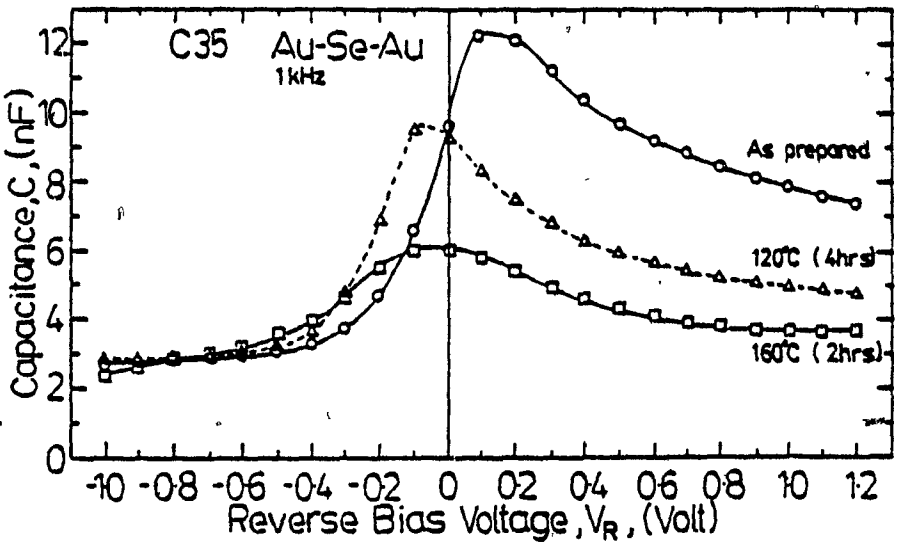

Fig. 7.7 Plot of capacitance versus reverse voltage V_R at 1kHz for Au-Se-Au sample (C35), before and after heat treatment at 120°C and 160°C in air.

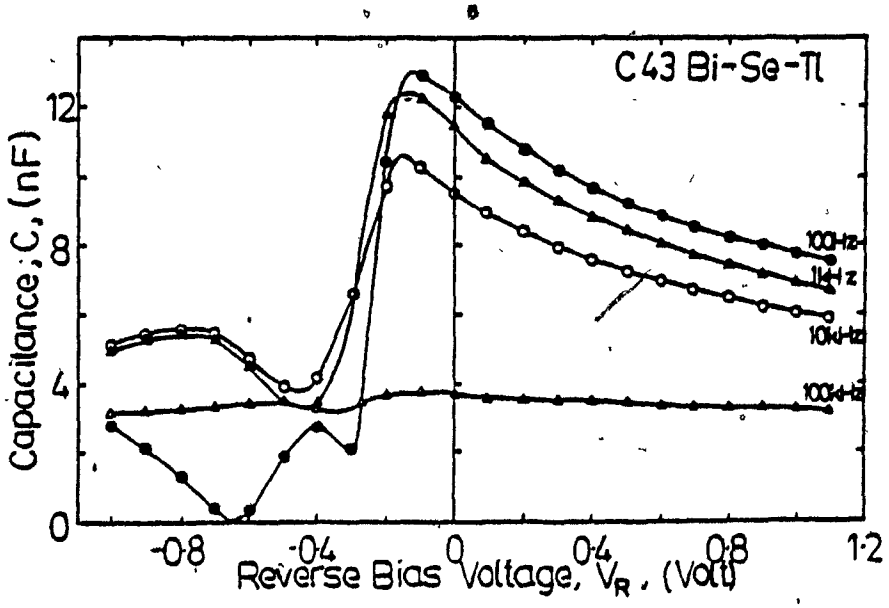

Fig. 7.8 Plot of capacitance against reverse voltage for Bi-Se-Tl sample (C43) at four different frequencies.

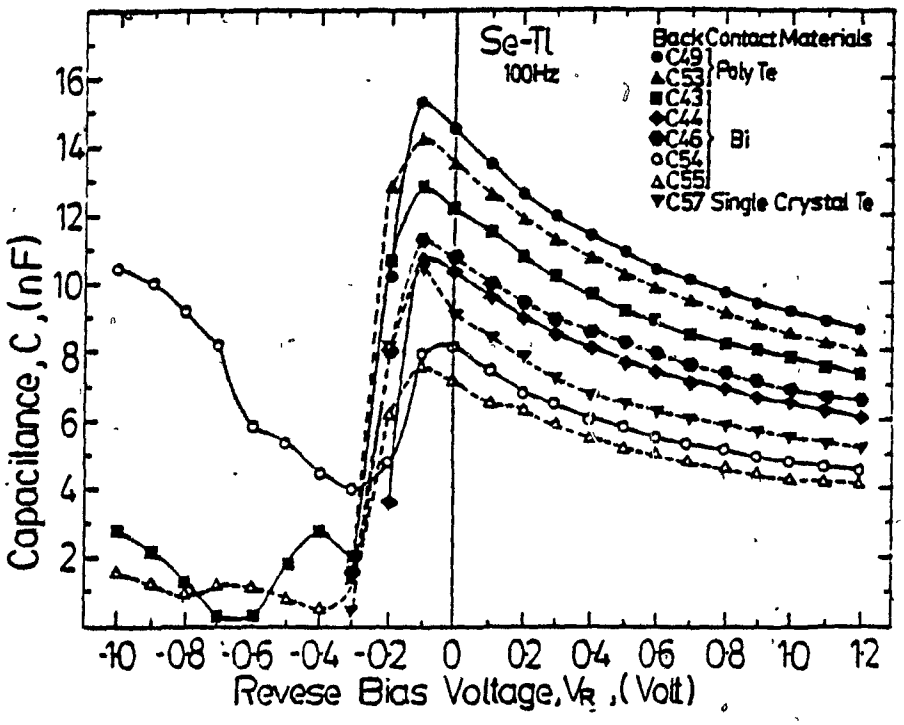

Fig. 7.9 Plot of capacitance as a function of bias at 100Hz for 8 Se-Tl samples with different back contact materials.

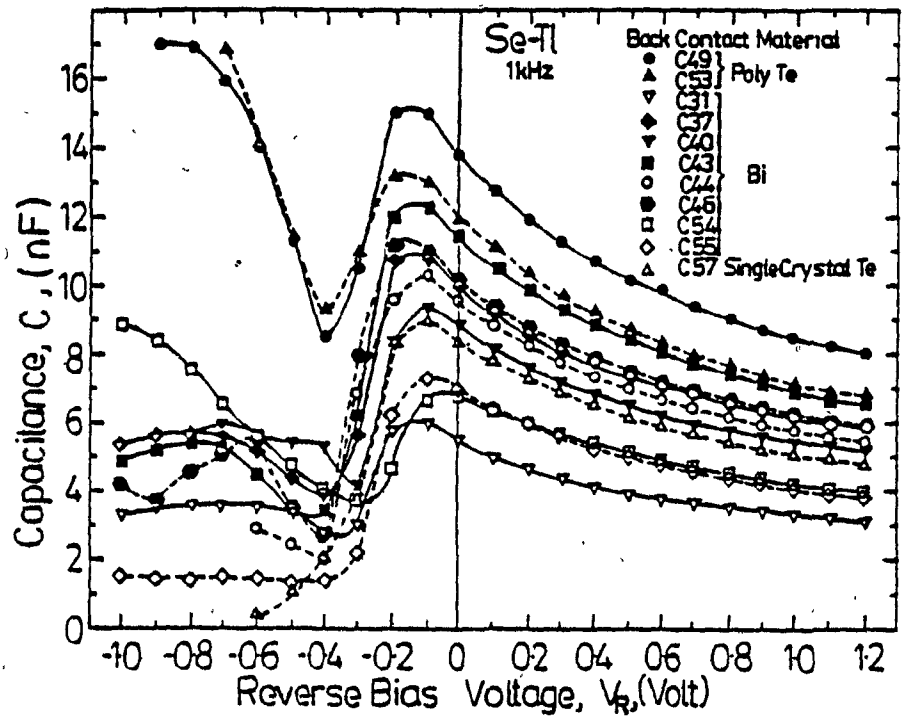

Fig. 7.10 Plot of capacitance as a function of bias at 1kHz for 11 Se-Tl samples with different back contact materials.

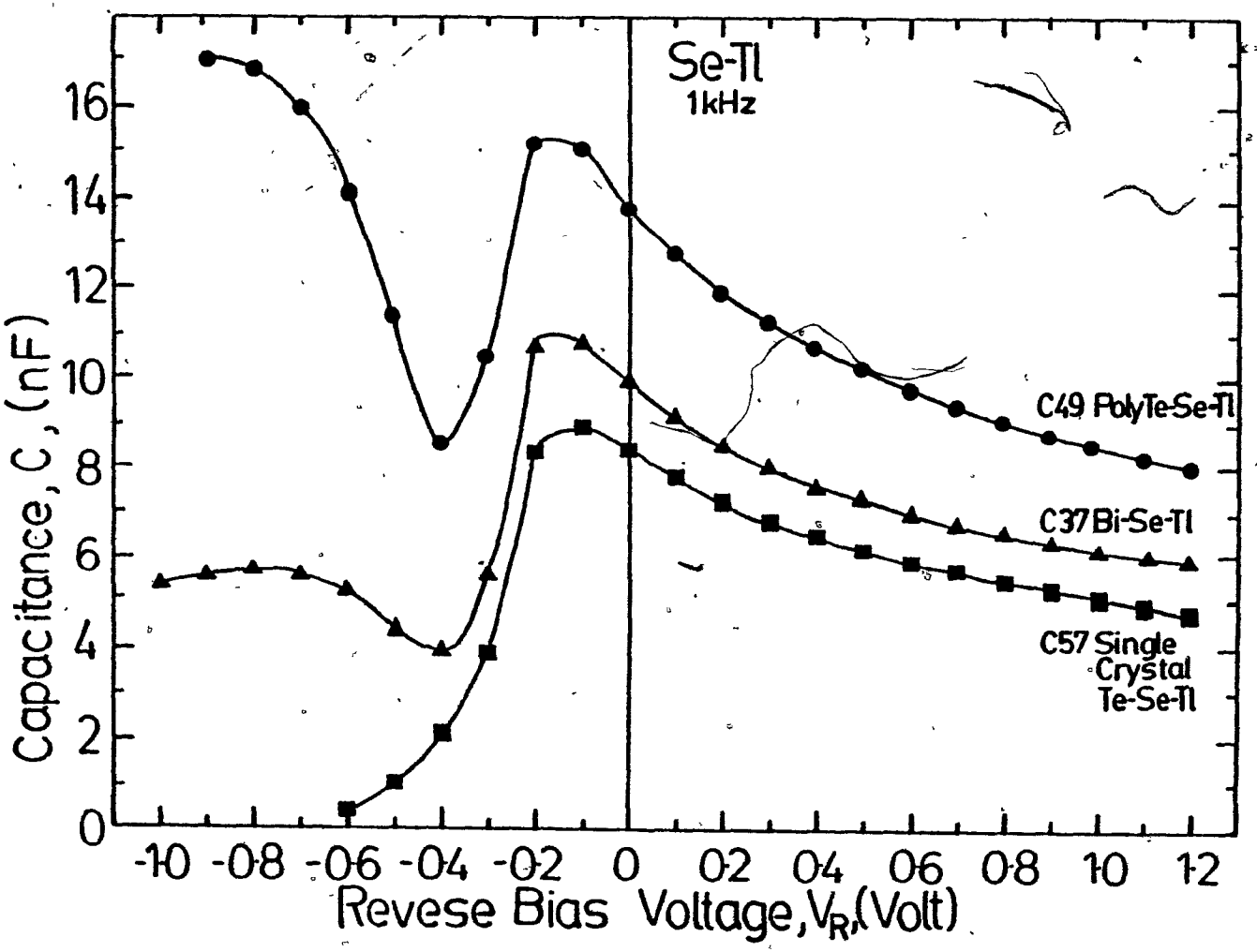

Fig. 7.11 Plot of capacitance as a function of bias at 1kHz for 3 Se-Tl samples with different back contact materials.

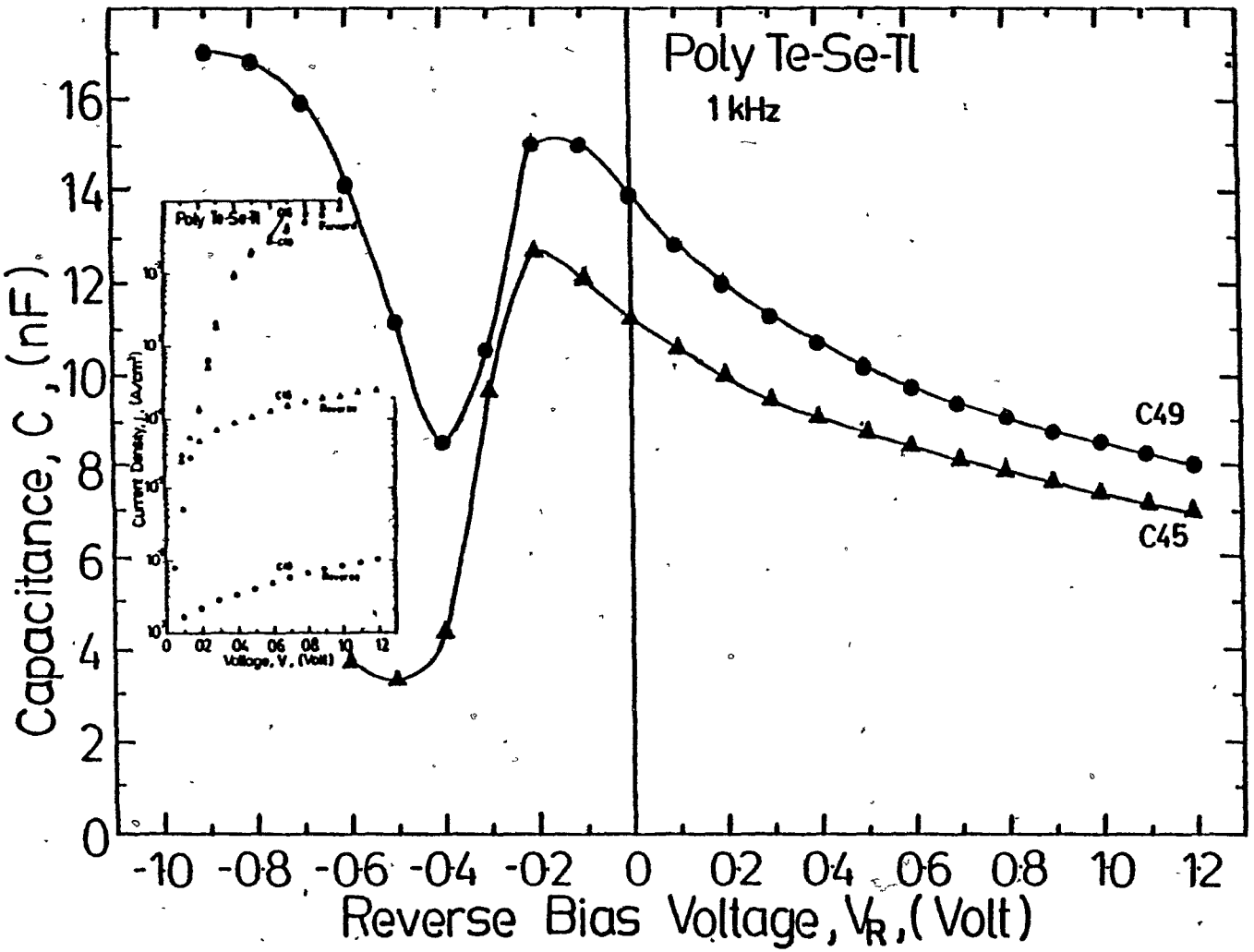

Fig. 7.12 Plot of capacitance as a function of bias at 1kHz for 2 polycrystalline Te-Se-Tl samples with different ln(j)-V characteristics, as shown in inset.

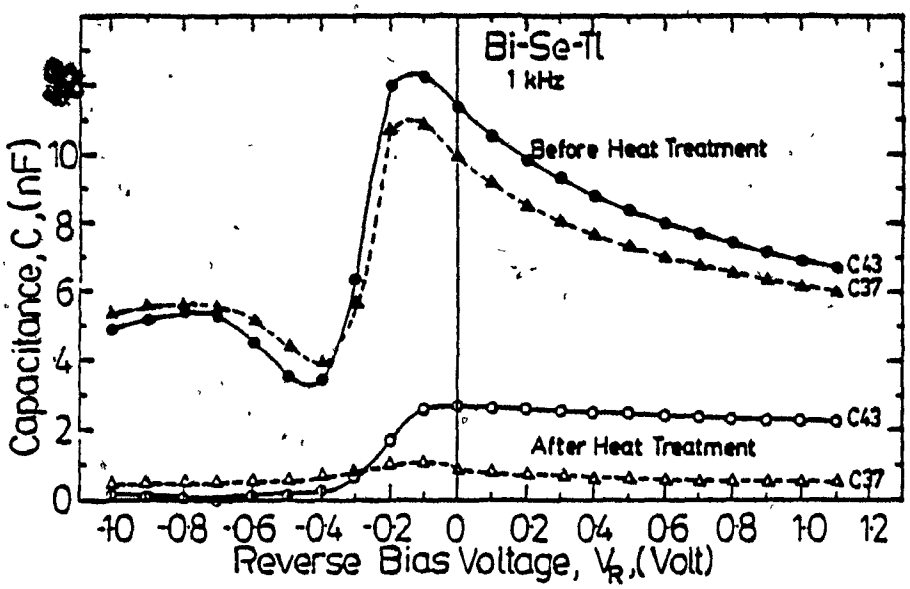

Fig. 7.13 Plot of capacitance as a function of bias at 1kHz for 2 Bi-Se-Tl samples, before and after heat treatment.

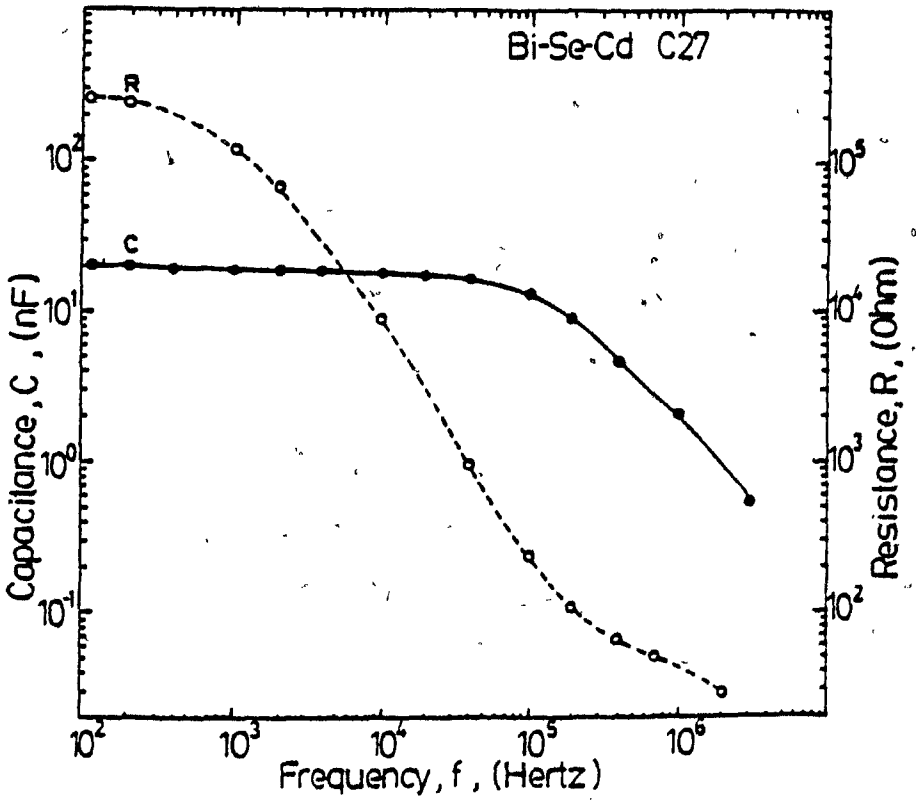

Fig. 7.14 Plot of incremental parallel capacitance (C) and resistance (R) against frequency (f) for Bi-Se-Cd sample (C27).

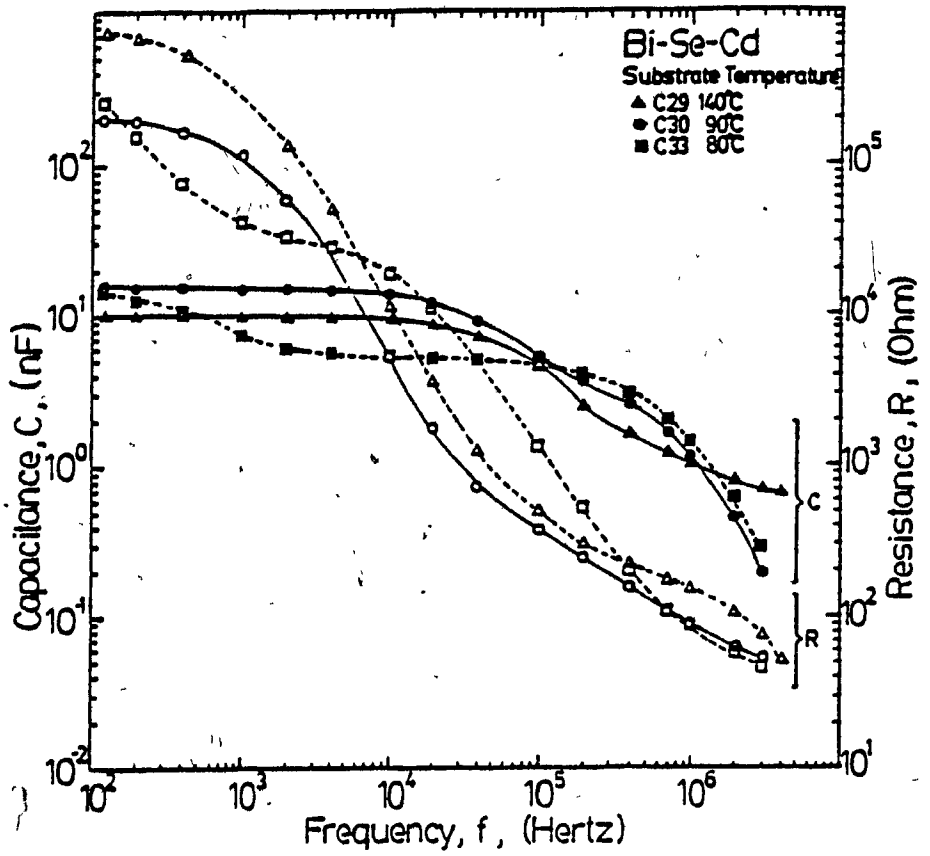

Fig. 7.15 Plot of C-f and R-f for 3 Bi-Se-Cd samples prepared at different substrate temperatures during Se deposition.

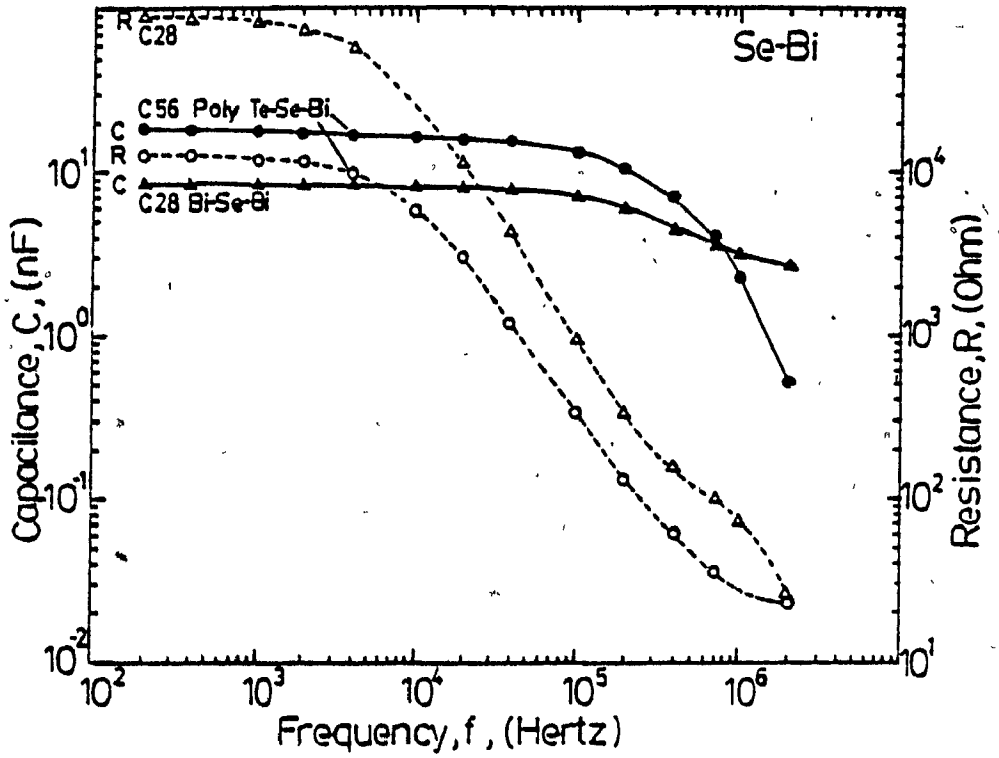

Fig. 7.16 Plot of C-f and R-f for 2 Se-Bi samples with different back contact materials.

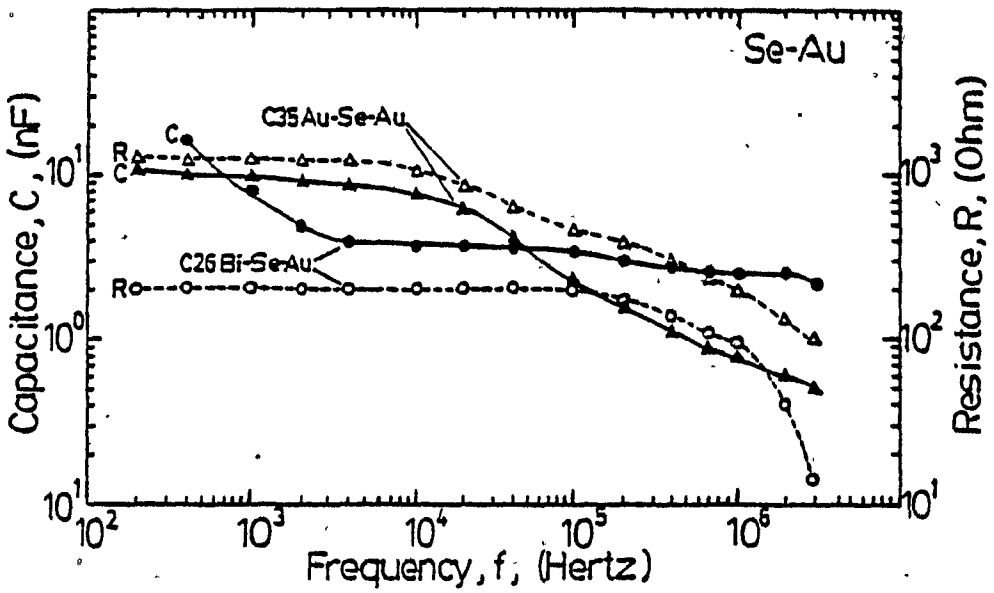

Fig. 7.17 . Plot of C-f and R-f for 2 Se-Au samples with different back contact materials.

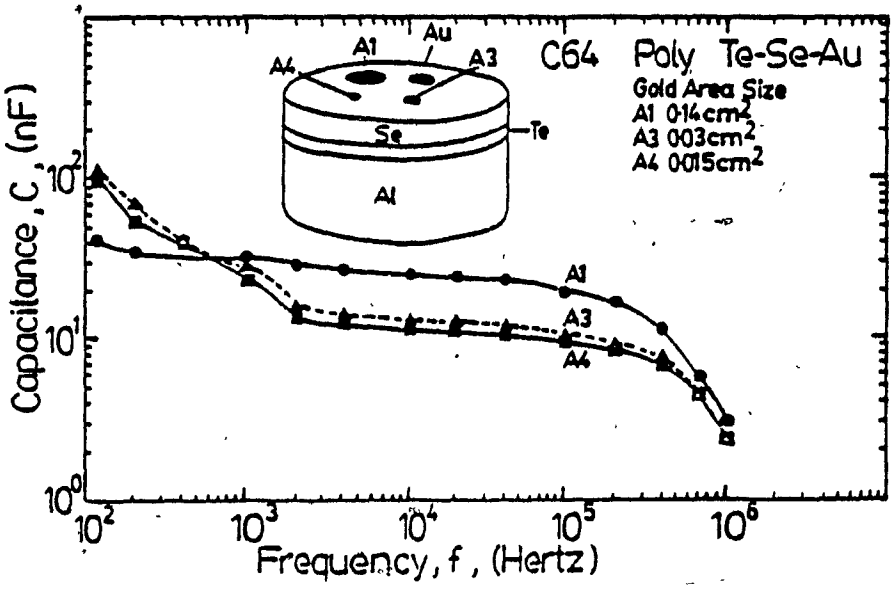

Fig. 7.18 Plot of C-f for polycrystalline Te-Se-Au sample (C64) on three gold areas A1, A3 and A4.

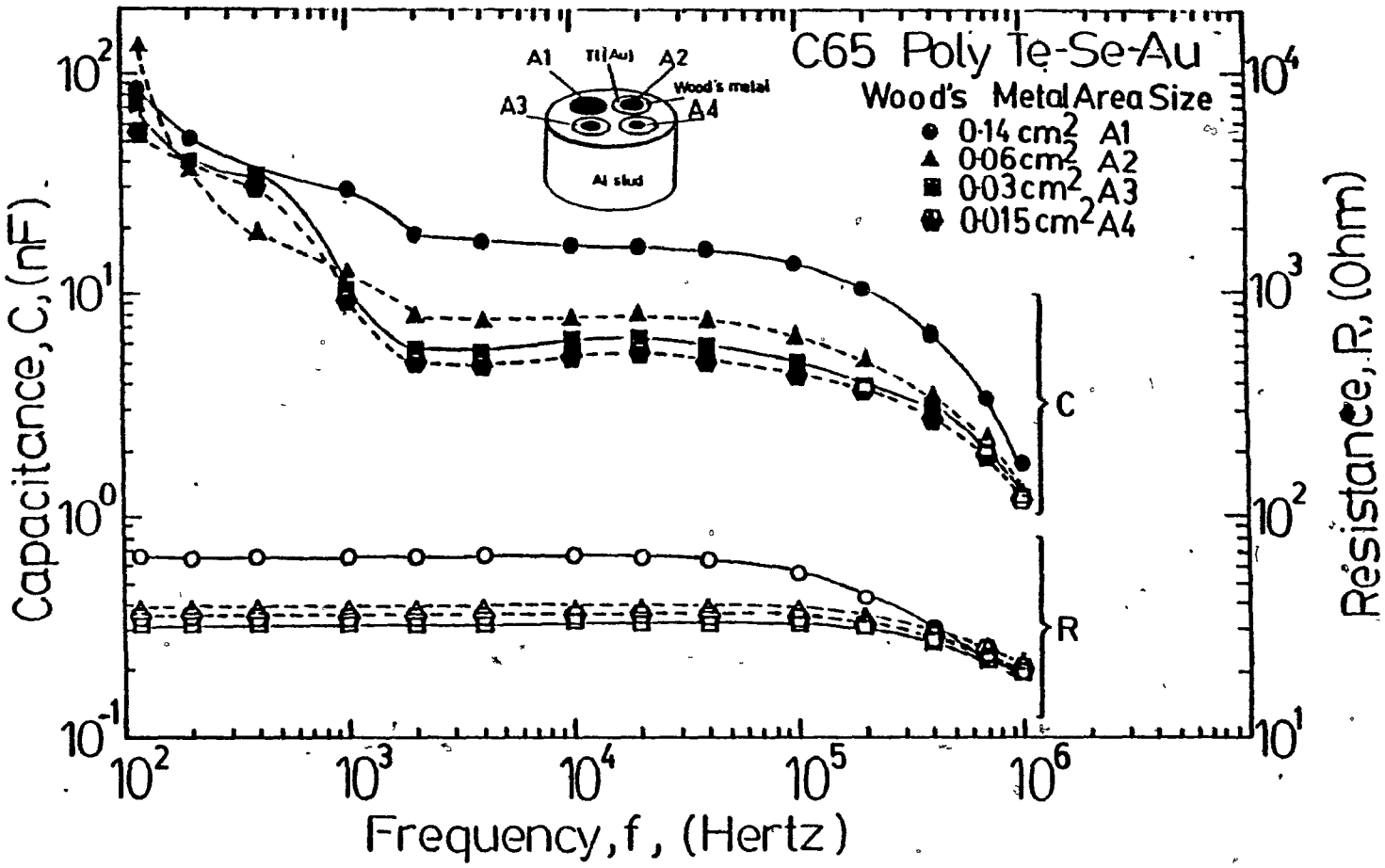

Fig. 7.19 Plot of C-f and R-f for polycrystalline Te-Se-Au sample (C65) on four Wood's metal contact areas A1, A2, A3 and A4.

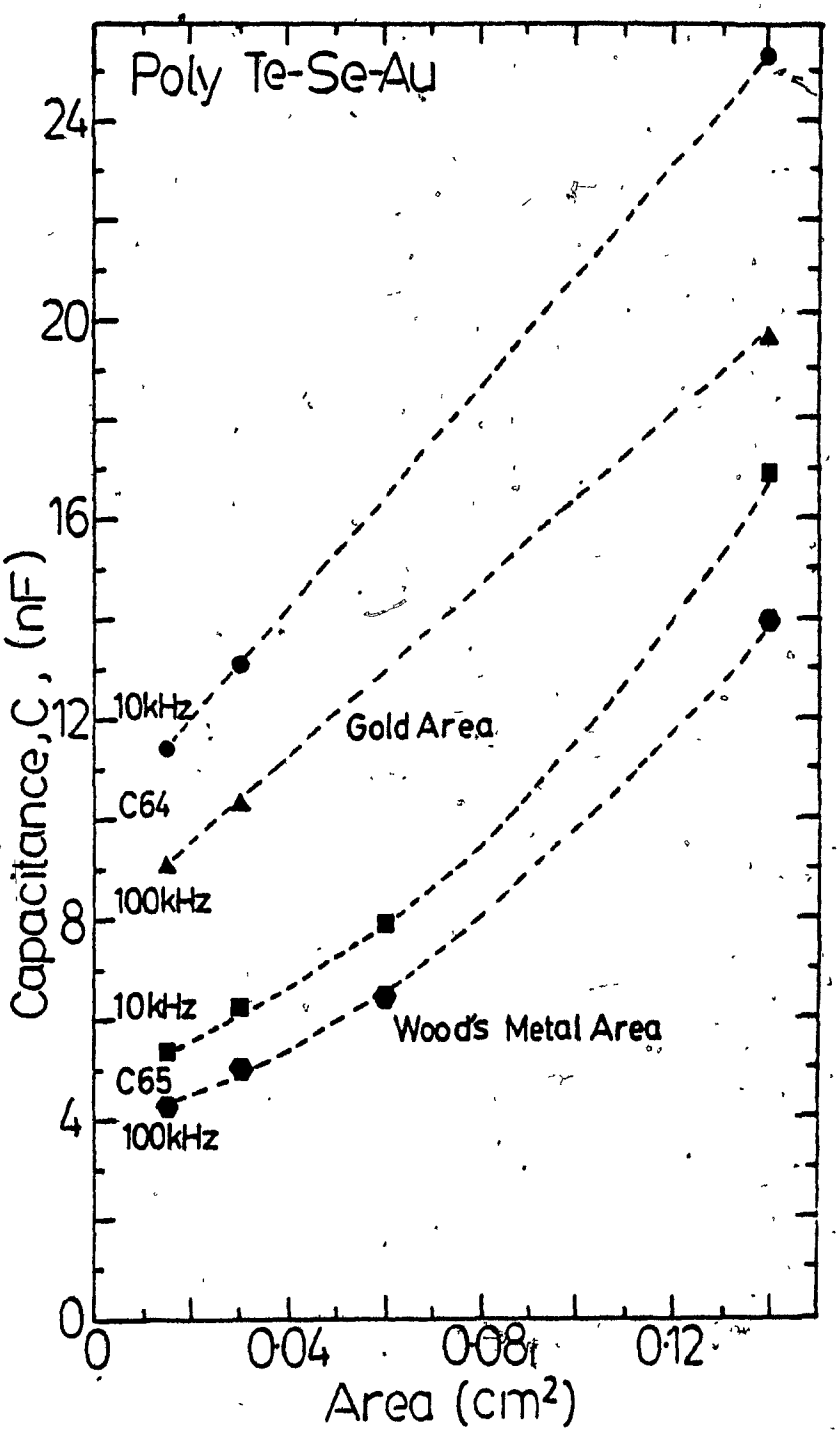

Fig. 7.20 Plot for 2 polycrystalline Te-Se-Au samples of capacitance versus gold area (C64) and Wood's metal contact area (C65) at 10kHz and 100kHz.

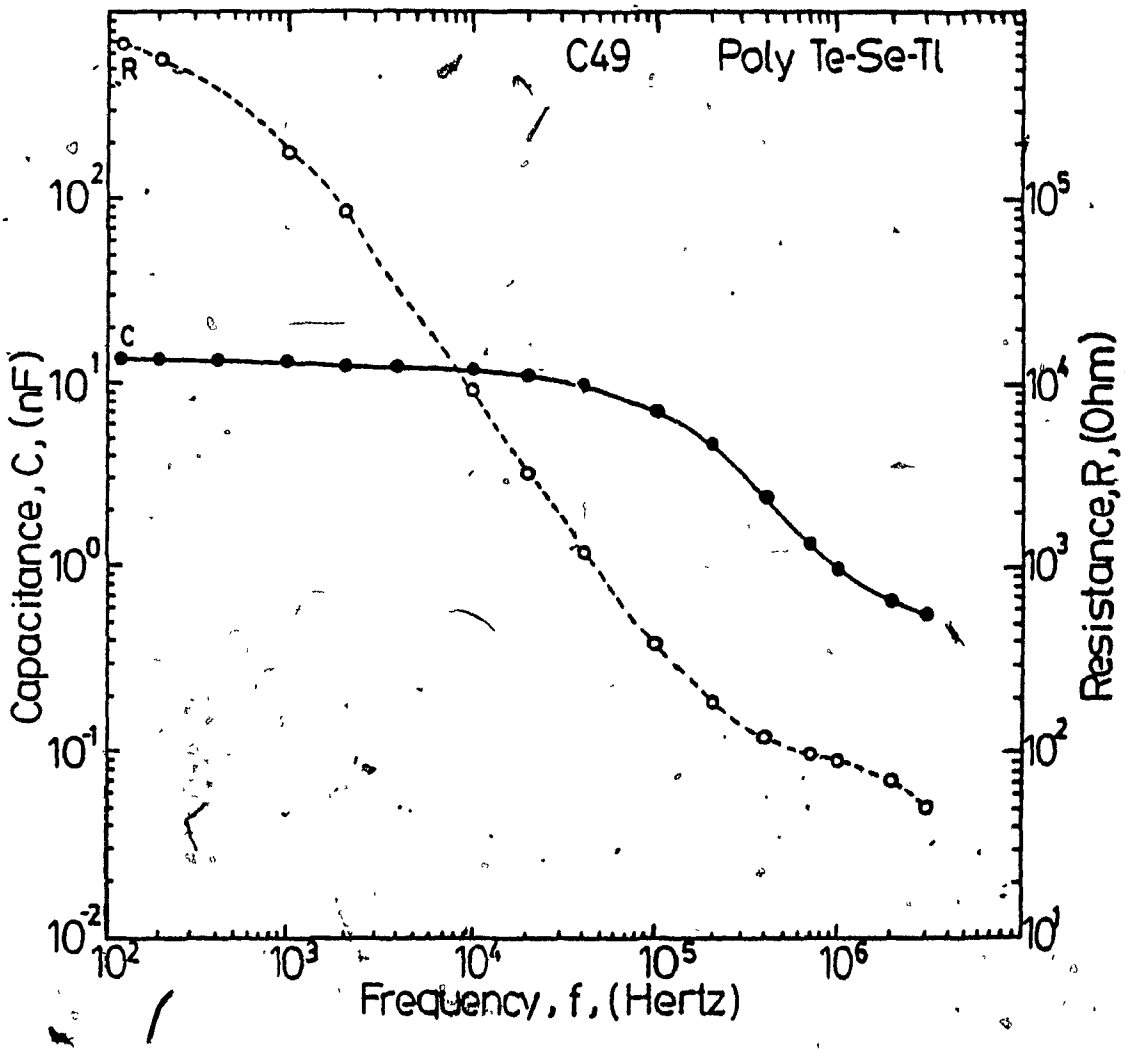

Fig. 7.21 Plot of C-f and R-f for a typical polycrystalline Te-Se-Tl sample (C49).

CHAPTER 8

DISCUSSION OF RESULTS

The experimental results presented in chapters 5,6 and 7 are now discussed together in a comprehensive manner.

It is clear that in the case of selenium-metal contacts, the work function (ϕ_m) of the metal plays an important role in determining the current-voltage characteristics. The proof of this is the plot of Fig. 5.13, showing that the barrier height ϕ_{bp} is indeed related to ϕ_m, despite the presence of interface states. This plot suggests a concentration of around 10^{14} of such states per cm^2, assuming an interfacial layer thickness of 10 Å [15]. It should be pointed out that the ϕ_{bp}-values obtained in this thesis may be underestimates of the work function values because the hole concentrations deduced from the slopes of the $(A/C)^2$ versus V_R plots represent, not just the free carriers, but also any charged trap centers. However, while the absolute magnitudes of the ϕ_{bp} values may be larger, the slope in Fig. 5.13 should not be greatly affected, leaving the estimate of the interface state density at about the same magnitude. It should also be pointed out that the results apply to an interface with polycrystalline selenium. Experiments should therefore be carried out with single crystal selenium to see if orientation effects exist.

The plots of current density against voltage reflect qualitatively the different barrier heights of the metals Au, Bi, Cd and Tl in Se-metal Schottky junctions. Thus, the Se-Au diodes gave the highest value of current density at low forward voltage and the Se-Tl diodes the smallest value. However, an attempt at obtaining barrier heights from the extrapolated intercepts of the j-V curves was quantitatively not successful.

Detailed studies on the aging of the selenium Schottky diodes were not done in work for this thesis but rapid aging was very much apparent for the Se-Tl diodes. A study was made, however, of post-fabrication heating of these diodes. It was found (chapter 6) that the forward current density (at 1 volt for example) was greatly reduced after heating in nitrogen, with resultant decrease of the rectification ratio. This was attributed to an increase of series resistance, resulting from the formation of thallium selenide at the Se/Tl interface [16]. The capacitance decreases observed were consistent with this explanation but experiments to detect the TlSe chemically have not been carried out. All other studies on the Se-Tl diodes in this thesis were therefore performed with freshly-made samples.

Some smaller changes were observed in post-fabrication heating of Se-Au diodes but these effects could be due to changes at the back contact. In comparing back contact materials, it would seem that the highest j-values at 1 volt forward and the highest zero-bias capacitance values were

observed on Se-Tl structures with polycrystalline tellurium as the back contact material, instead of bismuth. If this is confirmed for other Se-metal structures, it suggests that polycrystalline tellurium would be preferable to bismuth as the ohmic contact to the diode base.

In chapter 7, some anomalous capacitance results were reported. These should be regarded as tentative, particularly in the case of the Se-Bi and Se-Au diodes, since not many of these samples were prepared. In the case of the Se-Tl diodes, a minimum of capacitance was observed for a small forward voltage at lower frequencies. It was particularly marked at 100Hz. Anomalous minima were observed in Se-Au structures for a small reverse bias and also in Se-Bi diodes near zero bias (no results shown) at low frequencies. A possible explanation of these capacitance anomalies is an effect predicted by Roberts and Crowell [17] arising from a deep level in the semiconductor. Another explanation is that it arises from a partially blocking back contact. It is interesting to note that no dips were observed for the Se-Cd diodes. The present results, however, are too preliminary to determine the cause of the effects, which will be examined further in future investigations.

The main part of the variation of incremental capacitance and resistance with frequency can be explained assuming the simple equivalent circuit model shown in the inset to Fig. 8.1, arising from an analysis given in reference [18]. As seen, this consists of two capacitors in

series, C_j and C_o, shunted by resistors R_j and R_o; there is also an additional series resistor R. Using the formulae from reference [18] for the equivalent parallel capacitance C and resistance R, approximate values of the parameters C_j, C_o, R_j, R_o and R can be obtained by curve fitting. This was done for the C-f and R-f results for the Se-Tl sample C49, shown in Fig. 8.1, where the broken lines represent the calculated curves. It is seen that, while the fit is far from perfect, the calculated curves do explain the main over-all variation of the measured parallel capacitance and resistance for this sample with frequency for the values C_j=13.5 nF, C_o=1 nF, R_j=5x10^5 ohms, R_o=75 ohms and R=20 ohms. According to reference [18], C_j and R_j are the parallel capacitance and resistance values for the Schottky junction depletion layer, while C_o and R_o are respectively the corresponding quantities for a postulated layer depopulated of acceptors in the selenium adjacent to the counterelectrode; R is interpreted as the series resistance of the contacts and leads.

It would seem likely that a similar fit could be made to the results for the Se-Cd and Se-Bi diodes. In the case of the Se-Au samples, however, the resistance variation with frequency was much less and also anomalously high capacitance values were observed at low frequency, particularly for the small Wood's metal contact areas. Thus, the simple equivalent circuit may not be sufficient to explain these results.

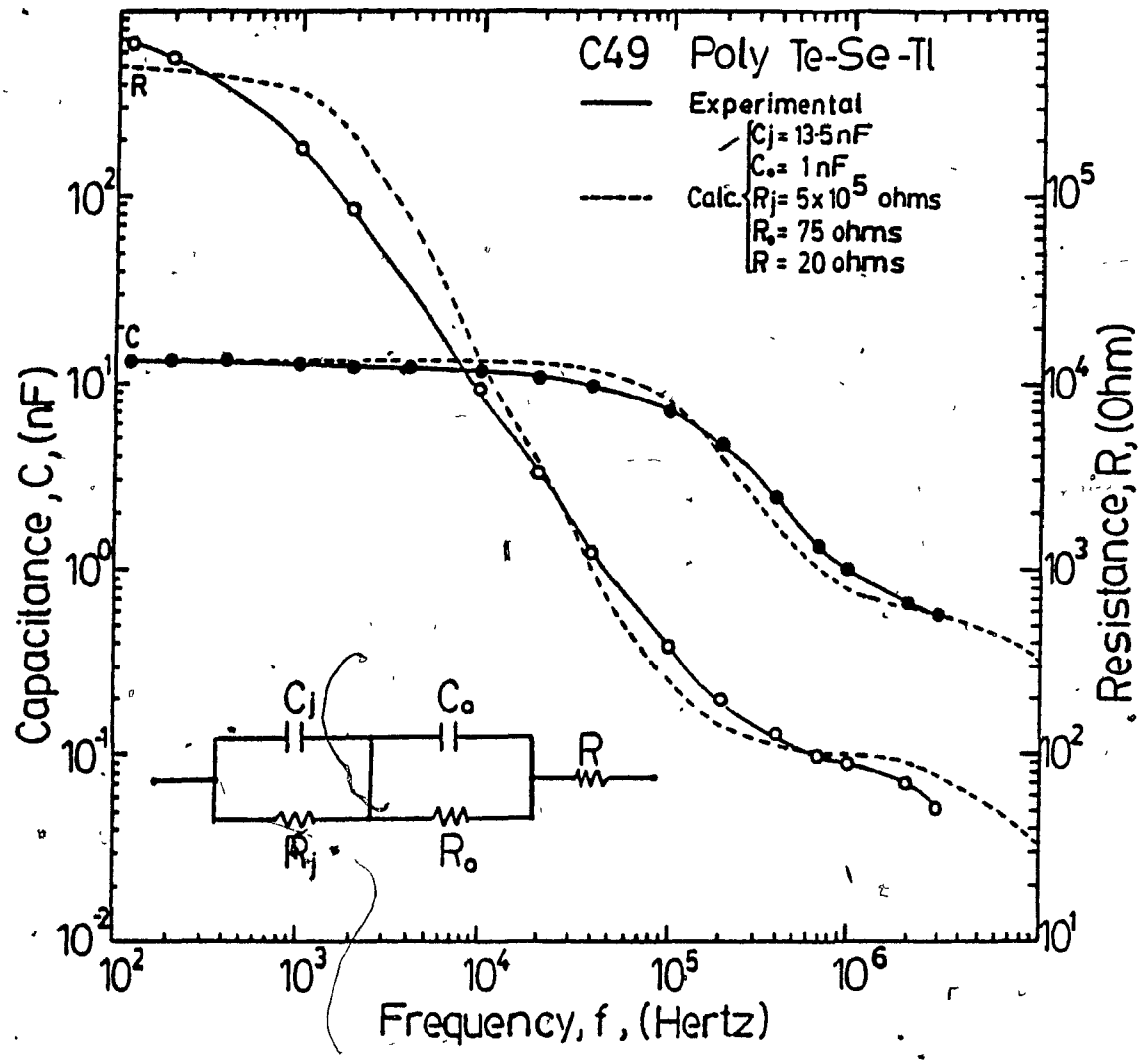

Fig. 8.1 Comparison of experimental and calculated curves of C-f and R-f for a polycrystalline Te-Se-Tl sample (C49), with inset showing the equivalent circuit used for the calculated values.

CHAPTER 9

OVER-ALL CONCLUSIONS

From the present results, it is clear that selenium-metal contacts are very convenient structures for studying Schottky junctions for a low mobility semiconductor, since the work functions of the metals do indeed play a decisive role in determining the barrier heights, despite a high concentration of interface states. This would seem to be due to the very high work function of selenium itself. The density of interface states for an assumed interfacial layer thickness of 10Å was estimated at about 10^{14} cm^{-2}. The Schottky junctions are easily made by evaporation of the metal on to a crystallized selenium film, without the need for ultra high vacuum techniques. It is important, however, to do the counterelectrode deposition at a low temperature and also to avoid heating the structure after fabrication, otherwise a selenide may be formed at the metal/selenium interface, resulting in a heterojunction, rather than a Schottky junction. This was very evident in the work on Se-Tl structures. The anomalous capacitance effects should be further studied, since if the Roberts-Crowell [17] explanation applies, these could yield the energy position of a deep level (or levels) in the selenium. The results with different back contact materials suggest that polycrystalline tellurium may give a lower series resistance than bismuth.

Most of the variation of incremental capacitance and resistance with frequency appears to be due to resistance arising from the selenium itself external to the depletion layer. A contribution by a smaller equivalent capacitor in series with that arising from the depletion layer was also apparent.

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