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Investigation of Photovoltaic Cells on Bridgman Grown CuGa_xIn_{1-x}Se₂ Crystals

by

Wai Wing Malcolm Lam

(M.Eng., McGill University)

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

> Department of Electrical Engineering McGill University Montreal, Canada

> > June, 1998

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ABSTRACT

Several important aspects of ZnO/CdS/CuGa_xIn_{1-x}Se₂ photovoltaic cells have been examined in this thesis. First of all, CuGa_xIn_{1-x}Se₂ crystals free from ampoule adhesion and suitable for photovoltaic cell studies were grown using a horizontal Bridgman method. The composition variation for ingots with different starting Ga content was analyzed and the results were interpreted using established pseudobinary phase diagrams. Various optimizations in the cell fabrication, such as crystal polishing, window layer deposition and cell area patterning, were carried out to establish a highly reproducible cell fabrication process for routine studies.

The effects of substrate annealing in Ar were investigated for cells with different Ga content. It is believed that Ar substrate annealing is beneficial to $CuGa_XIn_{1-X}Se_2$ cells regardless of the Ga content. However, to optimize performance, the same cell fabrication conditions should not be applied to fabricate cells with different Ga content. From illuminated I-V measurements, conversion efficiencies exceeding 10 % were achieved in two of the best cells. In particular, a $CuGa_{0.45}In_{0.55}Se_2$ cell attained a 10.1 % efficiency which is the highest among single crystal $Cu(Ga,In)Se_2$ cells with similar Ga content.

To establish the energy band diagrams of ZnO/CdS/CuGa_XIn_{1-x}Se₂ cells, the band lineup model was examined by considering the variations of electron affinity and energy gap of the absorber. In addition, the built-in potential V_{bi} as a function of Ga content was calculated based on the relative shift in Fermi level. Then, the lattice mismatch in CuGa_XIn_{1-x}Se₂ cells was also estimated. Following that, the dark current transport and photo-generated current collection mechanisms were analyzed. It was shown that the effect of shunting was greatly reduced for cells with Ar substrate annealing. Furthermore, the photo-generated current was found to follow a voltage dependent current collection mechanism which was independent of light intensity.

Capacitance-voltage measurements were carried out on cells with and without Ar substrate annealing. There is evidence showing the co-existence of both interfacial and bulk states. A substrate annealing in Ar was found to improve the interface properties. Moreover, deep level characteristics of $CuGa_{0.3}In_{0.7}Se_2$ were analyzed using DLTS technique. Two hole trap levels (0.32 eV and 0.43 eV) and one electron trap level (0.51 eV) were deduced. It is believed that the observed hole trap levels were formed independent of preparation conditions.

RESUMÉ

Plusieurs des aspects importants des cellules ZnO/CdS/CuGa_xIn_{1-x}Se₂ solaire seront abordés dans cette thèse. Premièrement, les cristaux CuGa_xIn_{1-x}Se₂ qui sont exempt d'adhésion d'ampoule et appropriés pour les recherches des cellules solaire sont fabriqués en utilisant la méthode Bridgman horizontale. La variation de la composition des lingots avec la contenue initiale de Ga différents étaient analysés et les résultats étaient interprétés en utilisant les diagrammes phases pseudobinaire. Plusieurs d'optimisations dans la fabrication de la cellule, telle comme astiquer des cristaux. déposition de la couche de fenêtre et la gravure des aires cellules, ont donner suite a établi un processus de fabrication de reproductibilité dans les cellules qui sont plus élevées pour les études routine.

Les effets du recuisissent du substrat Ar sont examinés pour les cellules avec différents de contenu Ga. On croit que le recuisissent du Ar est avantageux pour les cellules CuGa_XIn_{1-X}Se₂ sans considérer le contenu de Ga. Par ailleurs, pour améliorer les performances, la même condition de fabrication ne devrait pas être appliquée pour fabriquer des cellules avec du contenu Ga différentes. D'après les mesures I-V illuminer, les conversions d'efficacité excédant 10 % ont été démontrer dans les deux meilleurs cellules. L'efficacité du 10.1 % obtenu dans la cellule CuGa_{0.45}In_{0.55}Se₂ est la plus haute parmi toutes les cellules Cu(Ga,In)Se2 des cristaux simples avec du contenu Ga semblable.

Pour établir les diagrammes de bande d'énergie des cellules $ZnO/CdS/CuGa_XIn_1$. $_XSe_2$, le modèle de bande file était calculer en considérant la variation de l'affinité d'électron et du trou d'énergie de CuGa_XIn_{I-X}Se₂. D'ailleur, le potentiel d'intégration V_{bi} comme une fonction du contenu Ga était calculé en se basant sur le changement relative dans le niveau du Fermi. Donc, le courant de transport foncé et le courant de photo générer des mécanismes de collection ont étaient analysés. En particulier, l'effet de triage était grandement réduit pour les cellules avec le recuisissent du substrat Ar. De plus, le courant photo générer a suivi un mécanisme du courant de collection de voltage dépendant qui était indépendant de l'intensité de l'éclairage.

Les mesures de C-V sont exécutés sur les cellules avec et sans le recuisissent du substrat Ar. Il y a de l'évidence qui nous montre la coexistence des interfaces et des états en masse. Un recuisissent du substrat dans l'Ar a été constitué d'améliorer les propriétés interfaces. De plus, les niveaux profonds dans le CuGa_{0.3}In_{0.7}Se₂ ont été identifié en utilisant la technique DLTS. Deux niveaux de la trappe de trou (0.32 eV et 0.43 eV) at un niveau de trappe d'électron (0.51 eV) ont été déduit. Il, peut être suggéré que le niveau de la trappe de trou observer étaient formés indépendamment des conditions de préparation.

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Chapter 1

INTRODUCTION

As world energy consumption increases at an accelerating pace, concerns on the exhaustion of conventional fossil fuels are rising. In recent years, the environmental impacts of fossil fuels such as air pollution, acid rain and global warming also catch the attentions from people around the world. Although nuclear energy has been able to provide low cost alternative to fossil fuels, issues such as nuclear waste disposal and safety concerns are still under active debate. In view of the above factors, renewable energies have been under intense development especially after the energy crisis of the 1970's.

There are various kinds of renewable energies, such as hydroelectric, wind, solar, geothermal, ocean current and ocean wave. Among all the renewable energy sources, solar energy is the only kind which is accessible everywhere on the surface of the earth. Solar energy could be utilized in various ways including photothermal, photochemical, photoelectrochemical, and photovoltaic. In all these forms, photovoltaic could be considered to be the most robust form of implementation. It converts sunlight directly into electrical power. The conversion process usually employs semiconductor devices such as p-n junctions, Schottky junctions and metal-insulator-semiconductor junctions.

Among the three kinds of junctions, p-n junctions appear to give the best performance in photovoltaic (PV) energy conversion [5.4].

PV energy possesses several distinct advantages over other energy sources. To name a few: no moving parts, low demand in maintenance, unattended operation, could be placed physically near the load and large tolerance in operating temperature. Because of the above advantages, it has already excelled in several areas, such as powering spacecrafts, consumer electronics and remote area power generation. Although it is still too expensive at this moment for PV cells to become a major contender in bulk power generation, recent advances in PV cell technologies allow the cost of PV modules to reduce continuously. The use of PV systems for bulk electricity generation may be within reach in the near future.

Among semiconductors such as silicon (Si), cadmium telluride (CdTe), and III-V compounds, copper gallium indium diselenide (CuGa_xIn_{1-x}Se₂) based compounds appear to be one of the best compound systems for PV applications. There are three major advantages in CuGa_xIn_{1-x}Se₂ based PV cells. First, due to the extremely high absorption coefficient ($\geq 10^5$ cm⁻¹), efficient PV cells could be constructed in thin film form. An absorber layer of this compound of about 1-2 µm in thickness is enough to produce high efficiency cells. This property is important in reducing the material and processing cost as well as the weight of PV modules. Second, according to a nine year outdoor stability study carried out by National Renewable Energy Laboratory (NREL) (1997) [1.1], CuInSe₂ PV modules have been able to demonstrate extremely good stability. Good long term stability implies less frequent module replacements in future. Third, CuGa_xIn_{1-x}Se₂ based PV cells have extremely good resistance to radiation damage. This advantage is particularly important for space applications where the PV modules are constantly exposed to various kinds of radiation. According to a recent study carried out by Boeing Commercial Space Company (1997) [1.2], when the CuGa_XIn_{1-X}Se₂ cells were exposed to a flux of protons which would normally degrade the performance of Si space cells by 20 % or more, the degradation in CuGa_XIn_{1-X}Se₂ cells was only 1 %. Overall, it could be concluded that CuGa_XIn_{1-X}Se₂ based thin film PV cells are able to achieve high efficiency, low cost, light weight and long term stability for the purposes of large scale terrestrial and space applications.

CuGa_xIn_{1-x}Se₂ compounds are I-III-VI₂ multinary semiconductors with direct bandgaps varying from about 1 eV (x = 0) to 1.65 eV (x = 1). The CuGa_xIn_{1-x}Se₂ compounds possess a chalcopyrite structure. The corresponding lattice structure is shown in Fig. 1.1 [1.5]. There are three major advantages of using Ga containing absorbers (i.e. x > 0) instead of using just CuInSe₂ (x = 0). First, conversion efficiencies could be improved through better bandgap matching to the solar spectrum. Second, the increased open circuit voltage of Ga containing cells can relax the tight constraints on series resistance loss of large area cells and modules. Finally, due to the limited annual production capacity of indium, the pressure on the demand of indium is reduced by replacing some of the indium with gallium.

Since the pioneer work carried out by researchers at Bell Laboratories (1975) [4.71] demonstrating the potential of CuInSe₂ heterojunction PV cells, the development of thin film CuGa_xIn_{1-x}Se₂ based PV cells is notable. After more than 20 years of development. the best thin film $CuGa_XIn_{1-X}Se_2$ PV cell has achieved a conversion efficiency of 17.7 % (1996) [1.3]. This value is the highest among all thin film cells. In contrast, the best single crystal $CuGa_XIn_{1-X}Se_2$ cell stays at 12 % efficiency [4.71]. The large difference in conversion efficiency could be attributed to the lack of research in single crystal cells. However, the progress in thin film $CuGa_XIn_{1-X}Se_2$ cell efficiency appears to have slowed down recently. This is probably due to the lack of understanding of the properties of $CuGa_XIn_{1-X}Se_2$ and the corresponding devices. Since the grain size of the polycrystalline thin films is usually limited to ~ 1-2 µm, in many cases, they could not provide the long range order necessary for the study of various properties. In recent years, more attention is being put in the single crystal related researches to help understanding the material formation, absorber properties, junction formation and photovoltaic action [1.4, 2.9, 3.30,45-46, 4.1-7, 5.3,12, 6.4-6,16,30, 7.1-4] in CuGa_XIn_1-_XSe_2 based materials and devices. This is also the major motivation behind this project.

Previously, our laboratory had fabricated single crystal cells using the $ZnO/CdS/CuInSe_2$ structure [2.9, 4.3]. In this work, a similar $ZnO/CdS/CuGa_xIn_{1-x}Se_2$ cell structure is adopted. This particular structure is adopted because it is the most commonly employed structure in high efficiency thin film $CuGa_xIn_{1-x}Se_2$ cells. Thus, it provides a common ground to compare the single crystal cell results to the thin film cell results. Although other variations of the window structure have also been reported recently [1.6-9], the best cells are still obtained using the ZnO/CdS window structure.

Our laboratory has been investigating materials and devices of single crystal and thin film CuInSe₂ for more than fifteen years [2.4,9, 3.13-17,46,48,55,60-61,65,74-

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75.77.82 4.1-5,13,26-27,73, 5.1-2, 7.14-16,30-31,45-46]. This thesis research program represents the first study in our laboratory on Ga containing CuGa_XIn_{1-x}Se₂ alloys. Since single crystal CuGa_XIn_{1-x}Se₂ cells have not been studied extensively, many questions are still unanswered. Indeed, to the author's best knowledge, this is the first investigation of PV cells fabricated on Ga containing (x > 0) Bridgman grown CuGa_XIn_{1-x}Se₂ crystals. This project is set out to examine some of the immediate issues such as crystal growth, cell fabrication, cell performance, current transport mechanisms and deep levels. This thesis consists of eight chapters including this chapter. The chapter headings and the corresponding major objectives are given below.

Chapter 2 Theory of Photovoltaic Cells

- To give a brief review on the operation of photovoltaic cells.

Chapter 3 Growth and Characterization of CuGa_XIn_{1-x}Se₂ Crystals

- To grow $CuGa_XIn_{1-X}Se_2$ crystals using horizontal Bridgman method and understand various crystal properties.

Chapter 4 Optimization of the Cell Fabrication Process

- To establish a highly reproducible cell fabrication process for routine studies.

Chapter 5 Photovoltaic Characteristics of ZnO/CdS/CuGa_xIn_{1-x}Se₂ Cells

- To study the photovoltaic properties of CuGa_XIn_{1-X}Se₂ cells with various Ga contents.

Chapter 6 Energy Band Diagram and Current Transport of ZnO/CdS/CuGa_XIn_{1-X}Se₂ PV Cells

- To construct energy band diagrams of CuGa_XIn_{1-x}Se₂ cells and analyze current

transport mechanisms both in dark and under illumination.

Chapter 7 Capacitance Measurements of ZnO/CdS/CuGa_xIn_{1-x}Se₂ PV Cells

To study the interface and bulk properties of CuGa_XIn_{1-X}Se₂ cells using steady state (C-V) and transient (DLTS) capacitance techniques.

Chapter 8 Conclusions

- To summarize the results obtain in this work and make suggestions on future work.



Fig. 1.1. A schematic diagram showing the lattice structure of $CuGa_XIn_{1-X}Se_2$.

THEORY OF PHOTOVOLTAIC CELLS

2.1 Introduction

A photovoltaic (PV) cell is a semiconductor device that is used as an energy converter. When the PV cell is illuminated under solar irradiation, it converts the solar energy directly into electrical energy. A PV cell usually consists of a semiconductor p-n junction in the form of either homojunction or heterojunction. To understand the conversion process, the energy band diagram of a typical homojunction PV cell is first described. The concepts developed from it can be used to understand the operation of heterojunction PV cells, which is the main research interest in this work. The theory of p-n junction PV cell is very well developed. Detailed treatments on the theory can be found in various references such as Refs. [2.1-2, 6.22]. Here, only some of the most important issues are presented.

In this chapter, several important aspects of PV cells are described. Section 2.2 presents the basic principles of homojunction PV cells. The absorption coefficient and spectral response are described in sections 2.3 and 2.4, respectively. Descriptions of equivalent circuit, current-voltage relations and important parameters of PV cells are given in section 2.5. Important aspects of heterojunction PV cells are given in section 2.6. In this particular research, absorbers with different bandgaps are studied. The effects of

bandgap on the electrical characteristics of PV cells are presented in section 2.7. Finally. conclusions of this chapter are drawn in section 2.8.

2.2 Photovoltaic Effect

Fig. 2.1 illustrates the energy band diagram of a homojunction PV cell [2.4]. For instance, let us assume that solar irradiation is incident from the n-type semiconductor. In such case, we will call the n-type semiconductor as window and p-type semiconductor as absorber. In this figure, E_C represents the energy of conduction band edge, E_V represents the energy of valence band edge, and E_G denotes the bandgap of the semiconductor. The open circuit voltage (V_{OC}) indicated in this figure will be described in section 2.5.

Under solar illumination, a semiconductor material absorbs most of the photons with energies greater than the bandgap of the material, E_G . The absorbed photons excite electrons from the valence band to the conduction band. This excitation leaves free holes in the valence band. Thus, this process creates electron-hole pairs. The electron-hole pairs could be created either inside or outside the depletion region of the p-n junction as shown in Fig. 2.2. When electron-hole pairs are generated outside the depletion region, some of this photo-generated carriers will diffuse into the depletion region. The carriers generated inside the depletion region generated and swept by the strong electric field of the depletion region. When this happens, the electrons are swept towards the left side and the holes are swept towards the right side. Finally, to complete the process of utilizing the electrical energy resulting from

the photovoltaic effect, the charge carriers are collected by the external load as electrical current.

2.3 Absorption Coefficient

As described in the previous section, a semiconductor absorbs photons with energies greater than its bandgap. The ability of a material to absorb photons at a given wavelength is described by its optical absorption coefficient, α . The reciprocal of α gives the absorption length. Considering a monochromatic photon flux entering a semiconductor with a surface flux density F(0), the photon flux as a function of depth (x)below the semiconductor surface can be defined as the following,

$$F(x) = F(0)e^{-\alpha x} \tag{2.1}$$

where F(x) is the photon flux at depth x, with a unit of number of photons per square centimeter per second.

Photons with smaller energies normally penetrate deep inside the material before the absorption occurs. Therefore, larger absorption lengths and smaller absorption coefficients are observed for small energy photons. On the other hand, photons with energies sufficiently greater than the bandgap are most likely to be absorbed close to the surface. This results in small absorption depths and, of course, large absorption coefficients. Fig. 2.3 shows the absorption coefficient as a function of photon energy for CuInSe₂ and some other semiconductors which are commonly used to fabricate PV cells [2.3]. As shown in Fig. 2.3, the absorption coefficient of CuInSe₂ is the highest among the commonly used PV materials. For photons with energies higher than the bandgap of $CuInSe_2$ (~ 1 eV), the absorption coefficient is always higher than 10^4 cm⁻¹. This means an absorption length of 1 µm or less. This result shows that the absorption of photons is extremely efficient in CuInSe₂. Another important observation from Fig. 2.3 is that the transition of absorption coefficient is abrupt for direct bandgap materials such as CuInSe₂, GaAs, and CdTe. This indicates a high efficiency in absorption coefficient is gradual for indirect bandgap materials such as x-Si and a-SiH. This implies a relatively inefficient absorption even when photon energies are greater than the bandgap. Furthermore, the magnitude of the absorption coefficient is usually larger for direct bandgap materials.

To understand the significance of high absorption coefficient, let us consider two contrary examples, Si and CuInSe₂. In the case of Si PV cells, due to the relatively low absorption coefficient, most of the photons will penetrate deep inside the semiconductor before electron-hole pairs could be created. Thus, a thick layer of Si (tens of micrometers) is needed to absorb most of the photons in the solar spectrum. In contrast, for a direct bandgap material such as CuInSe₂, the absorption of photons is extremely efficient. With small absorption lengths, only a thickness of about 1 μ m is needed to absorb most of the photons in the solar spectrum. Therefore, semiconductors with high absorption coefficients, such as CuInSe₂, are generally suitable for the fabrication of low cost thin film PV cells. In addition, Fig. 2.4 illustrates the shift in absorption edge due to different bandgaps for CuInSe₂ [2.12] (~ 1 eV), CuGa_{0.25}In_{0.75}Se₂ [2.10] (~ 1.15 eV) and CuGaSe₂ [2.11] (~ 1.65 eV).

2.4 Spectral Response

The spectral response of a PV cell at a specific wavelength is defined as the number of electron-hole pairs collected per incident photon at that wavelength. It can be expressed by the following equation,

$$SR(\lambda) = \frac{I_L(\lambda)}{qAF(\lambda)}$$
(2.2)

where $I_L(\lambda)$ is the photocurrent (light generated current) measured at a specific wavelength (λ) which is the total photocurrent contribution due to the front, depletion and back regions of a PV cell, q is the magnitude of electron charge, A is the effective area of the PV cell, and $F(\lambda)$ is the incident photon flux density at a specific wavelength.

In reality, the spectral response depends on many parameters such as surface recombination velocity, absorption coefficient, minority carrier diffusion length, carrier concentrations as well as thickness of window and absorber regions. Ideally, the spectral response is a step function of energy when the surface recombination velocity is zero. The calculated spectral response of a Si p-n junction PV cell with a non-zero surface recombination velocity is shown in Fig. 2.5 (a) [2.1]. The three calculated components due to the front, depletion and base regions are seen to have peaks located at different

energy values. It can be seen from the figure that the low energy photons are mainly absorbed by the base region while the high energy photons are mainly absorbed by the front region due to different absorption lengths. In this figure, the total spectral response is seen to first rise with the increase of photon energy and reaches a maximum. It then decreases as the energy is further increased when most of the electron-hole pairs are generated near the surface region and then recombine because of the non-zero surface recombination velocity.

In Fig. 2.5 (b) [2.1], the total spectral response calculated for different surface recombination velocities are shown. We can see that the response in the high energy region decreases with the increase of the surface recombination velocity. Therefore, to achieve a good spectral response, one should minimize the effect of surface recombination. This problem could be tackled by adopting a heterojunction structure as described in section 2.6.

2.5 Equivalent Circuit, Current-Voltage Characteristics and Parameters

The equivalent circuit of an ideal p-n junction PV cell under illumination is shown in Fig. 2.6 (a). It consists of an ideal p-n junction diode in parallel with a light generated current source. The photocurrent is flowing in the direction opposite to the forward bias current of the p-n junction diode. As a result, the output current (*I*) which is available to the load can be expressed as

$$I = I_{L} - I_{O} \left(e^{\frac{qV}{kT}} - 1 \right) , \qquad (2.3)$$

where I_L is the photocurrent, I_O is the reverse saturation current of the p-n junction. q is the magnitude of electron charge, V is the voltage across the load. k is Boltzmann constant, and T is temperature. However, this only represents an ideal case, where an ideal PV cell is assumed.

In a more practical model, several changes have to be made to accommodate the non-ideal characteristics. The modified equivalent circuit is shown in Fig. 2.6 (b). In such a circuit, several elements are different from the ideal circuit. First, the ideal diode is replaced by a non-ideal diode. This leads to the introduction of an ideality factor (*n*) in the exponential term of the diode dark current. Normally speaking, the ideality factor is governed by the current transport mechanism. Second, a shunt resistance (R_{SH}) is introduced across the PV cell to represent current loss across the junction due to junction defects such as diffusion spikes and pin holes. If the junction defect density is small, R_{SH} is usually large. Finally, a series resistance (R_S) is introduced to represent the resistive loss. This resistive loss is usually due to the sheet resistance of the window, internal resistance of absorber and contact resistances (front and back). Since it represents the resistive loss 'outside' the p-n junction, it should be minimized to deliver maximum power to the load. As a result of various modifications, the current-voltage (I-V) relation becomes the following:

$$I = I_{L} - I_{O} \left[e^{\frac{q(V+R_{S}I)}{nkT}} - 1 \right] - \frac{V+R_{S}I}{R_{SH}}$$
(2.4)

From Eq. 2.4, we can then derive two important parameters. The first one is the short circuit current (I_{SC}), which represents the current flowing through the PV cell in a short circuit condition (V = 0). The expression can be written as

$$I_{SC} = I_{L} - I_{O} \left(e^{\frac{qR_{S}I_{SC}}{nKT}} - 1 \right) - \frac{R_{S}I_{SC}}{R_{SH}} \quad .$$
 (2.5)

Under normal conditions where R_S is small, R_{SH} is large and $I_L >> I_O$, I_{SC} will be very close to I_L (i.e., $I_{SC} \approx I_L$). The second parameter is called open circuit voltage (V_{OC}). It represents the voltage across the PV cell when I = 0. The expression can be written as

$$I_O\left(e^{\frac{qV_{CC}}{nkT}}-1\right) + \frac{V_{CC}}{R_{SH}} = I_L \quad .$$
(2.6)

If R_{SH} is large, the expression for V_{OC} can be simplified as,

$$V_{OC} \approx \frac{nkT}{q} \ln \left(\frac{I_L}{I_O} + 1 \right).$$
(2.7)

Following the definitions of I_{SC} and V_{OC} , we can then define some of the more important parameters in evaluating PV cells. Let us first consider the I-V characteristic of a typical PV cell under illumination as shown in Fig. 2.7 (a) [2.13]. For easy assessment, we can invert the I-V characteristic of Fig. 2.7 (a) about the voltage axis and the result is shown in Fig. 2.7 (b) [2.2].

When a finite load resistance is connected to the PV cell, the power delivered to the load is equal to the product of I and V, i.e., $P_{OUT} = I \times V$. In practice, a particular load resistance can be matched such that the power output is maximum. If such a condition is met, the maximum power output (P_M) is defined as

$$P_{\mathcal{M}} = I_{\mathcal{M}} V_{\mathcal{M}} \tag{2.8}$$

where I_M and V_M are the corresponding current and voltage that give maximum output power. This case is illustrated in Fig. 2.7 (b) as the maximum power rectangle.

Furthermore, the fill factor (FF) can be defined as the following,

$$FF = \frac{P_M}{I_{SC}V_{OC}} = \frac{I_M V_M}{I_{SC}V_{OC}}.$$
(2.9)

The fill factor is affected by series resistance, shunt resistance, and current transport mechanism, which determine the shape of the illuminated I-V characteristics of a PV cell.

Regardless of the current transport mechanism, the effects of series and shunt resistances on FF as well as I_{SC} and V_{OC} are illustrated in Figs. 2.8 (a) and (b), respectively [2.1]. Ideally, the series resistance should be close to zero. A large series resistance will lead to a decrease in I_{SC} as well as drastic decrease in FF. While an ideal shunt resistance should be as large as possible, a small shunt resistance will result in small V_{OC} and FF.

Finally, the most important parameter in evaluating PV cells is the conversion efficiency (η). It is defined as the ratio of the maximum output power to the input power. The expression is given as

$$\eta = \frac{P_{M}}{P_{IN}} = \frac{I_{M}V_{M}}{P_{IN}} = \frac{FF \cdot I_{SC}V_{OC}}{P_{IN}},$$
(2.10)

where P_{IN} is the incident power of the solar radiation that reaches the surface of PV cell. Therefore, the conversion efficiency of a PV cell is proportional to FF and the product of I_{SC} and V_{OC} .

2.6 Heterojunction PV Cells

A heterojunction PV cell usually consists of two semiconductors with different bandgaps. The energy band diagram of a typical n-on-p heterojunction PV cell under illumination is shown in Fig. 2.9 [2.9]. The n-type window layer is usually a wide bandgap ($E_{Gl} > 2$ eV) and low resistivity semiconductor such as cadmium sulphide (CdS), indium doped tin oxide (ITO) or zinc oxide (ZnO). While the p-type absorber is usually a smaller bandgap (E_{G2}) semiconductor with high absorption coefficients such as CulnSe₂.

The basic principles of heterojunction PV cells are very similar to those of homojunction PV cells. However, heterojunction cells have two major advantages over homojunction cells. First, in a homojunction PV cell, photons with energies greater than the bandgap of the material will be absorbed either close to the surface or inside the semiconductor depending on the penetration depth. Thus, a relatively large portion of photons could be absorbed very close to the surface of the PV cell. Some of the electron-hole pairs created close to the surface of the PV cell could recombine before reaching the depletion region. This phenomenon leads to a significant loss in spectral response due to the surface recombination. In contrast, due to the large bandgap for the window layer of a heterojunction cell, photons with energies smaller than the bandgap of window layer (E_{G1}) could effectively penetrate the window layer and reach the p-type absorber. Electron-holes pairs are then created predominantly inside the p-type absorber and only an extremely small portion of electron-hole pairs is created close to the surface of the PV.

cell. Therefore, the heterojunction structure could effectively reduce the effect of surface recombination.

Second, to reduce the series resistance to a minimum, the sheet resistance of the window region should be minimized. In a homojunction PV cell, this is usually done by utilizing a highly doped diffusion layer. While this is readily achieved in silicon, it is difficult to fabricate and control the quality of the diffused layer in compound semiconductors. However, by adopting the heterojunction structure, a low resistivity window layer could be deposited onto the p-type absorber to form PV cells. This eliminates the need for a highly doped diffusion layer. On the whole, the heterojunction structure is usually preferred for the development of high efficiency thin film PV cells.

2.7 Effect of Bandgap on PV Cell Performance

Eq. 2.10 indicates that the conversion efficiency is directly proportional to FF as well as the product of I_{SC} and V_{OC} . In this section, the effect of absorber bandgap on the theoretical conversion efficiency will be discussed. In particular, the parameters of CulnSe₂ will be used to estimate the theoretical conversion efficiency for CuGa_XIn_{1-X}Se₂ based PV cells.

First of all, to understand the effect of absorber bandgap on the I_{SC} , let us consider Fig. 2.10 which shows the solar spectrum (in number of photons per square centimeter per second per eV) as a function of photon energy for AM 0 and AM 1.5 [2.5] conditions. The AM 1.5 (84.4 mW-cm⁻²) condition represents a reasonable average for terrestrial applications. By assuming one electron-hole pair will be created for every absorbed photon with an energy greater than the bandgap of the absorber (E_{G2}) , the theoretical short circuit current density (J_{SC}) can be obtained graphically from the AM1.5 spectrum in Fig. 2.10 as the following [2.2],

$$J_{SC} = \frac{I_{SC}}{A} = q \int_{nv=E_{G2}}^{\infty} \left(\frac{dn_{ph}}{dhv}\right) dhv \qquad , \qquad (2.11)$$

where A is the area of the PV cell. The result, J_{SC} as a function of E_{G2} , is shown in curve (1) of Fig. 2.11 [2.2,5]. In the figure, the theoretical J_{SC} varies from 61 mA-cm⁻² to approximately 1 mA-cm⁻² as the bandgap (E_{G2}) varies from 0 eV to 3.5 eV. However, in our particular case, the bandgap of CuGa_XIn_{1-X}Se₂ only varies from approximately 1 eV (x = 0) to 1.7 eV (x = 1). As shown from Fig. 2.11, J_{SC} varies almost linearly from about 41 mA-cm⁻² to 18.5 mA-cm⁻² in the range of interest. Therefore, an empirical formula for I_{SC} can be derived as the following,

$$I_{sc} \approx A(73.1 - 32.1E_{G2}) \cdot 10^{-3}, \qquad 1 \text{ eV} < E_{G2} < 1.7 \text{ eV}.$$
 (2.12)

To determine the relationship between the absorber bandgap and V_{OC} , let us consider Eq. 2.7. Under normal solar irradiation where $I_L / I_O >> 1$, and since $I_{SC} \approx I_L$, Eq. 2.7 can be approximated as the following,

$$V_{oc} \approx \frac{nkT}{q} \left(\ln I_{sc} - \ln I_o \right).$$
(2.13)

While I_0 can be expressed in the following form [2.6],

$$I_o = C e^{\frac{-E_{c_1}}{BkT}}, \qquad (2.14)$$

where B is a constant greater than 1 and usually $B \approx n$. For an n⁺-p junction, C can be approximated by [2.14]

$$C \approx qA \left(\frac{D_N N_C N_V}{L_N N_A} \right), \tag{2.15}$$

where A is the area of the PV cell (total area \approx effective area is assumed), D_N is the diffusion coefficient of electrons in the absorber, L_N is the electron diffusion length in the absorber, N_A is the hole concentration in the absorber, E_{G2} is the bandgap of the absorber, N_C and N_V are effective density of states for conduction and valence bands in the absorber. For instance, $D_N = \mu_n kT/q$ with μ_n = electron mobility, $N_{C.V} = 2(2\pi m_{n,p} kT/h^2)^{3.2}$ with h = Planck's constant, $m_{n,p} = effective mass of electrons and holes, respectively.$

By substituting Eqs. 2.14 and 2.15 into Eq. 2.13, one can obtain V_{OC} as a functions of I_{SC} and E_{G2} as shown in the following,

$$V_{OC} \approx \frac{nkT}{q} \left[\frac{E_{G2}}{BkT} + \ln I_{SC} - \ln \left(\frac{qAD_N N_C N_V}{L_N N_A} \right) \right].$$
(2.16)

Now, we need to derive V_M and I_M to obtain a complete picture. If we neglect the effects of series and shunt resistances, Eq. 2.4 could be simplified as the following,

$$I = I_{L} - I_{O} \left(e^{\frac{qV}{nkT}} - 1 \right).$$
 (2.17)

The output power is therefore given by,

$$P = IV = I_{L}V - I_{O}\left(e^{\frac{qV}{nkT}} - 1\right)V \qquad (2.18)$$

The condition for maximum power is met when dP/dV = 0, one can show that

$$V_{M} + \frac{nkT}{q} \ln\left(1 + \frac{qV_{M}}{nkT}\right) \approx V_{OC} \quad \text{and} \quad (2.19)$$

$$I_{M} \approx \frac{I_{SC}}{1 + \frac{nkT}{qV_{M}}} \quad . \quad (2.20)$$

Once V_M and I_M are known, FF and hence conversion efficiency can be readily computed. Please note that while the I_{SC} decreases with absorber bandgap, both V_{OC} and FF are predicted to increase with absorber bandgap [2.1].

By using this model, the theoretical conversion efficiencies for n = 1 and 1.5 are plotted against absorber bandgap as shown in Fig. 2.12. The parameters used are: $\mu_n = 500 \text{ cm}^2/\text{V-s}$ [2.8], T = 298 K, $m_p^* = 6.643 \times 10^{-31} \text{ kg}$ [2.8], $m_n^* = 8.19 \times 10^{-32} \text{ kg}$ [2.7], $L_N = 4 \mu \text{m}$ and $N_A = 10^{17} \text{ cm}^{-3}$ [2.9]. As shown in Fig. 2.12, the conversion efficiency for n = 1 is always higher than that for n = 1.5, this is expected since n = 1represents an ideal p-n junction. For n = 1, the efficiency attains its maximum at approximately 1.4 eV and decreases as the bandgap continues to increase. Similar behavior is observed for n = 1.5 with the maximum efficiency located at about 1.5 eV. Although the absolute values might not represent the actual situations due to various assumptions and approximations, the effect of absorber bandgap on theoretical conversion efficiency is illustrated.

On the whole, Eqs. 2.12, 16, 19 and 20 give us an insight on the theoretical influence of the absorber bandgap on the performance of a PV cell. Please keep in mind that this model does not consider the effects of shunt and series resistances. The effect of

window bandgap is also not considered and the current transport mechanism is assumed to be represented by a single ideality factor (n).

2.8 Conclusions

In this chapter, various important aspects in the operation of homojunction and heterojunction PV cells are discussed. Important ideas such as absorption coefficient, spectral response and equivalent circuits are introduced. Special attention has been directed to the effect of absorber bandgap on the theoretical performance of heterojunction PV cells.



Fig. 2.1. Energy band diagram of a homojunction PV cell under illumination [2.4].



Fig. 2.2. A band diagram showing the carrier generation, separation and collection in a homojunction PV cell under illumination.


Fig. 2.3. Absorption spectrum of some semiconductors commonly used for PV cell fabrication [2.3].



Fig. 2.4. Absorption spectrum of CuInSe₂ [2.12], CuGa_{0.25}In_{0.75}Se₂ [2.10] and CuGaSe₂ [2.11].



Fig. 2.5. Calculated spectral response of a Si n-on-p PV cell, (a) showing contributions from different regions, and (b) with different surface recombination velocities. [2.1]





Fig. 2.6. Equivalent circuit of (a) an ideal PV cell under illumination, and (b) a practical PV cell under illumination.



Fig. 2.7. (a) Current-voltage characteristics of a Si PV cell under illumination. [2.13] (b) Inversion of (a) about the voltage axis. [2.2]



Fig. 2.8. Effect of (a) series resistance and (b) shunt resistance on the current-voltage characteristics of a Si PV cell. [2.1]



Fig. 2.9. Energy band diagram of a typical heterojunction PV cell under illumination [2.9].



Fig. 2.10. Solar spectrum as a function of photon energy for AM 0 and AM 1.5 conditions. [2.5]



Fig. 2.11. Ideal short circuit current density (curve (1)) as a function of absorber bandgap. [2.5]



Fig. 2.12. Theoretical conversion efficiency as a function of absorber bandgap for n = 1and n = 1.5.

GROWTH AND CHARACTERIZATION OF CuGa_xIn_{1-x}Se₂ CRYTALS

3.1 Introduction

Both the CuInSe₂ (x = 0) and CuGaSe₂ (x = 1) bulk crystals have been grown using various methods such as directional freezing (including Bridgman and Stockbarger methods) [2.8-9, 3.1-17,46-47,55,72,77], zone growth (also called zone melting or zone leveling) [3.1,18-21], solution growth (including traveling heater method) [3.12,22-27], selenization of Cu-In or Cu-Ga alloy [3.28-30] and chemical vapour transport [3.4,31-35]. In addition, CuInSe₂ crystals were also grown by liquid encapsulated Czochralski method [3.6] and hydrothermal solution method [3.36].

In our laboratory, we had concentrated our efforts on the crystal growth of CuInSe₂. Both the vertical [3.15,17,46,55,77,82] and horizontal [2.9, 3.13-14,16,77] Bridgman methods were used. One of the difficulties in CuInSe₂ crystal growth is the adhesion between the compound and the quartz ampoule wall. The adhesion induces large amount of cracks and other defects which significantly limit the size of the crystals. To solve this problem, in the early experiments, quartz ampoules coated completely with carbon were used. Although the adhesion problem was solved, carbon coating was often found to detach from the quartz wall and incorporated into the ingots which limited the

size of single crystal grains. However, recent results from our laboratory showed that a partially carbon coated ampoule could eliminate the adhesion problem even if the melt was not in contact with the carbon coating for the whole crystal growth process [2.9, 3.16]. In addition, by introducing a small piece of solid graphite into the ampoule, the adhesion problem could also be eliminated. These two methods allowed the growth of adhesion-free ingots without any carbon contamination. Furthermore, it was found that boron nitride coating could also effectively eliminate the adhesion problem [3.17,46]. More recently, oxygen in the starting Cu shots was identified as the source of the adhesion problem despite a purity of at least 99.999 % [3.46,48]. Moreover, various experiments have been carried out in our laboratory to study the effect of non-stoichiometric starting melt on conduction type, composition and crystal phases of as-grown CuInSe₂ crystals [3.46,60,65,75,82].

Unlike the two end point compounds (x = 0, 1), research work on Cu(Ga,In)Se₂ (0 < x < 1) mixed crystals remains scarce. Few papers have described the crystal growth experiments of Cu(Ga,In)Se₂. Details were reported by Paorici et al. [3.37-38] and Tinoco et al. [3.39] using chemical vapour transport. Ciszek et al. [3.40-42] reported crystal growth experiments using liquid encapsulated vertical Bridgman/Stockbarger method. Not long ago, Miyake et al. [3.45] reported the details of crystal growth using a kind of solution growth technique (traveling heater method). Although there were other papers [3.43-44] reporting the growth of Cu(Ga,In)Se₂ bulk crystals, no experimental detail was disclosed.

From the above literature survey, it is clear that no experimental details on horizontal Bridgman growth of Cu(Ga,In)Se2 bulk crystals was reported before. In addition, although the use of partially carbon coated ampoules could effectively eliminate adhesion between CuInSe₂ and guartz, it is still not known if a similar method could result in adhesion-free ingots when Ga is introduced. Therefore, one of the objectives in the present work is to investigate the horizontal Bridgman growth of adhesion-free Cu(Ga,In)Se₂ and CuGaSe₂ bulk crystals. The details of the crystal growth experiments are reported in section 3.2. Even though composition variation along Bridgman grown CuInSe₂ ingots has been studied [3.14,46,47], the effect of Ga on the composition variation along Bridgman CuGa_XIn_{1-X}Se₂ ingots is still not known. Accordingly, composition variations along the as-grown ingots with different starting Ga contents were studied and the results are presented in section 3.3. Moreover, powder x-ray diffraction experiments were carried out to study the crystal structure and lattice constants as a function of Ga content. The details are given in section 3.4. Electrical characteristics were studied and the results are discussed in section 3.5. Finally, the conclusions of this chapter are drawn in section 3.6.

3.2 Bridgman Growth of CuGa_xIn_{1-x}Se₂

In a typical Bridgman crystal growth process, the starting materials are usually sealed inside an evacuated quartz ampoule. The starting materials could be polycrystals of the compound to be grown or pure elements. The sealed ampoule is then heated up in a furnace to a temperature above the melting point of the compound to be grown. If pure elements are used as starting materials, the melt is allowed to stay at that temperature for a prolonged period of time in order to ensure the complete reaction between elements. Mixing of the materials (either manually or mechanically) is sometimes performed in addition to the high temperature soaking. After the reaction phase, the ampoule is then slowly moved along a stable temperature gradient from high temperature zone towards the low temperature zone. Directional freezing occurs when the melt experiences a temperature lower than the melting point of the compound to be grown.

In the present work, the crystal growth experiments were performed using a horizontal Bridgman system. The optimized crystal growth conditions employed in the present study were modified from procedures originally developed to grow CuInSe₂ crystals in our laboratory [2.9, 3.16]. The details of the present crystal growth experiments are described below.

3.2.1 Ampoule Preparation

To avoid the adhesion problem, ampoules partially coated with carbon were used. A schematic diagram of the specially formed ampoule used in the present study is shown in Fig. 3.1 (a). The ampoule consisted of two sections. The upper section was partially coated with carbon, while the melt was located in the lower section. During the whole crystal growth process, the melt was isolated from the carbon coating all the time. The use of this non-contact method is believed to eliminate carbon contamination. The outer diameter (OD) and inner diameter (ID) of the quartz tubes used were 1.6 cm and 1.2 cm, respectively. The lower section of the ampoule had a typical length between 10 and 12 cm.

Before the ampoule was allowed to form, one end of the quartz tube was sealed by H_2/O_2 torch. This end of the quartz tube was normally made into a conical shape in order to facilitate nucleation of the melt at the early stage of crystallization. The quartz tube (with one end sealed) was first cleaned with trichloroethylene (TCE), acetone (ACE) and then rinsed with de-ionized (D.I.) water. It was then etched using aqua regia (3 parts of HCl + 1 part of HNO₃) for 24 hours. After the etching, the quartz tube was then first rinsed with cold D.I. water for many times and finally rinsed with boiling D.I. water. Following the cleaning process, the quartz tube was dried using torch flaming. The carbon coating located in the upper section of the ampoule was prepared by pyrolysis of ACE using low temperature torch flaming until an opaque layer of carbon was formed. After the formation of carbon coating, the quartz tube was connected to a vacuum system and allowed to bake at 1050 °C for 5 hours for outgassing while it was vacuum pumped.

The starting materials consisted of elements with purity of at least 99.999 %. Before loading the materials into the quartz tube, some cleaning steps were performed on the elements. Cu and In shots were etched in diluted HCl for 5 minutes to remove the surface oxides and then rinsed with D.I. water followed by methanol. Se shots and Ga pieces were rinsed with TCE, ACE, D.I. water and finally with methanol. After the cleaning, the materials were weighted according to the stoichiometric composition and then quickly loaded into the quartz tube. The ampoule was allowed to pump down to $5 \ge 10^{-6}$ Torr before sealing by H₂/O₂ torch. The total weight of the materials used in each round was about 30 g.

3.2.2 Crystal Growth by Horizontal Bridgman Method

The crystal growth experiments were carried out in a commercially available THERMCO MB-80 horizontal resistive heating furnace and a custom made horizontal ampoule transporting system. No structural modification was made to the furnace. The schematic diagram of the complete crystal growth system is shown in Fig. 3.2 (a) [2.9]. The ampoule transporting system is capable of pulling/pushing the ampoule between the edge and the center of the furnace at rates ranging from 1 mm/hr to 30 mm/hr. The distance between the edge and the center of the furnace is about 70 cm. The central zone of the furnace can be adjusted to temperatures between 400 °C and 1400 °C. It is equipped with a custom made temperature controller which can adjust the heating or cooling rates of the center zone from 20 °C/hr to 200 °C/hr.

Before the crystal growth process started, the upper section of the ampoule (newly sealed end) was joined to the quartz rod. With the center of furnace preset to 400 °C, the ampoule was pushed in slowly from the edge of the furnace towards the central zone. This resulted in an equivalent heating rate of about 20 °C/hour. A low heating rate was used in this initial heating stage to avoid ampoule cracking. Once the ampoule reached the central zone, the furnace was heated up at a rate of 100 °C/hour until the temperature climbed to 1120 °C. The materials were then allowed to react for 24 hours at this temperature. During the 24 hour period, the materials were mixed by agitating the

ampoule manually. To avoid any possible contact between the melt and the carbon coating, manual agitation was chosen instead of mechanical mixing.

After the reaction phase, the ampoule was then pulled across a stable temperature gradient at a rate of 8 mm/hour until it reached the edge of the furnace. This resulted in equivalent cooling rates between 8 °C/hour and 16 °C/hour until the temperature reached about 500 °C. The temperature of furnace plotted against the distance from center of furnace is shown in Fig. 3.2 (b). The temperature gradients at 1000 °C and 650 °C were about 10 °C/cm and 20 °C/cm, respectively. Once the ampoule reached the edge of furnace, the temperature of the center zone was decreased such that cooling rate was about 30 °C/hour at the edge of the furnace. When the temperature at the edge of furnace reached about 250 °C, the furnace was then shut down. The whole crystal growth process starting from the initial heating usually took about six days. It is well known that CuInSe₂ goes through a solid state phase transition at about 810 °C [3.51-53]. In addition, there is also a suspected solid state phase transition at 665 °C [3.52]. To assure that the ampoule went through the transition temperatures smoothly, the temperature at the edge of furnace was intentionally chosen to be lower than 665 °C.

A total of over 20 ingots with different Ga contents were grown using the described procedure. In the early stage of the present work, various crystal growth conditions were investigated. For instance, temperatures higher than the one used were attempted. It was found that temperature setting higher than 1120 °C led to a rather large temporal fluctuation in temperature profile. By using the present setting, the temperature of the central zone was found to fluctuate within ± 2 °C. Also, attempts have been made to

change the temperature gradients and it was found that the range at which the gradients could be changed was confined by the original design of the furnace to a narrow domain. Furthermore, pulling rates lower than 8 mm/hour were tried, however, no significant effect in crystal size was observed. This is consistent with earlier result obtained in our laboratory in vertical Bridgman growth of CuInSe₂ [3.46]. In that case, no significant change in single crystal grain size was observed when the pulling rate was reduced from 10 to 2 mm/hour. Although in the case of vertical growth, the temperature gradient was about 70 °C/cm which was about five times larger than the present case.

3.2.3 Experimental Results - General Observations

Using the present procedure, adhesion-free ingots were obtained. Single crystal grains with dimensions ranging from 5 to 10 mm could be extracted from the polycrystalline ingots. The size of single crystals appeared to be affected by the Ga content. Generally, the size decreased as the Ga content was increased. The reduction in single crystal size was mainly due to the increase in density of cracks. Indeed, this finding agrees with the early results reported by Tomlinson [3.47] that crystal yield of CuGaSe₂ was lower than that of CuInSe₂. In addition, Tomlinson [3.47] also reported that it was difficult to avoid the adhesion between quartz and CuGaSe₂ (especially in the last-to-freeze zone) unless carbon coated ampoule was used. However, in the present case, all the as-grown ingots were free from adhesion regardless of Ga content. This indicated partially carbon coated ampoules could effectively eliminate the adhesion problem for the whole range of Ga content ($0 \le x \le 1$). Even occasionally when the ampoules cracked

after the melt solidified and the ingots were oxidized, no adhesion was observed. This suggested that the oxides formed after the crystallization of the melt were not responsible for the adhesion. According to recent results from our laboratory, oxygen is identified to be the main agent which caused adhesion [3.17,46], it is therefore believed that the involvement of oxygen in the adhesion is mainly in the early stage of solidification. Fig. 3.3 shows a polished crack-free and void-free CuGa_{0.15}In_{0.85}Se₂ single crystal.

3.3 Composition Analysis

Composition variations along as-grown ingots which were grown from stoichiometric melt with different starting Ga contents were studied by electron probe microanalysis (EPMA). The measurements were carried out using a JEOL 8900 L Electron Probe Microanalyzer. Before the EPMA measurements, the samples were polished using the process described in chapter 4. After polishing, the samples were loaded into a vacuum chamber and pumped down to a pressure of about 10^{-6} Torr. An electron beam (beam current = 20 nA, accelerating voltage = 20 kV and beam diameter = 5 μ m) was then allowed to bombard the surface of the samples. The characteristic x-rays emitted from the samples were analyzed. By comparing the emitted x-rays to those obtained from the elemental or compound standards (Cu, In, Se and GaAs in this particular case), the composition of the samples could be computed.

Five as-grown ingots with different starting Ga contents (x = 0, 0.25, 0.4, 0.8, 1) were studied. The crystals were extracted from three regions (first-to-freeze zone, middle zone, and last-to-freeze zone) of the ingots. Fig. 3.1 (b) illustrates the approximate positions where the EPMA measurements were carried out. Six to eight measurements were carried out in each region with an area of about 0.5 cm^2 to obtain the average values. The results are summarized in Table 3.1 which shows the Cu/(Ga+In) and Ga/(Ga+In) ratios of the five ingots at different regions.

Starting	First-to-freeze zone		Middle zone		Last-to-freeze zone	
Composition (x)	Cu/(Ga+In)	Ga/(Ga+In)	Cu/(Ga+In)	Ga/(Ga+In)	Cu/(Ga+In)	Ga/(Ga+In)
0.00	0.98	0.00	1.01	0.00	1.05	0.00
0.25	0.84	0.28	0.91	0.25	0.95	0.21
0.40	0.84	0.45	0.90	0.41	0.92	0.32
0.80	0.80	0.87	0.83	0.83	0.91	0.68
1.00	0.76	1.00	0.81	1.00	0.84	1.00

Table 3.1. Results from composition analysis.

The Cu/(Ga+In) ratio was found to vary between 0.76 and 1.05. The majority of the crystals were found to be Cu poor. While the Se/(Cu+Ga+In) ratio was found to vary between 0.94 and 1.02 (data not shown) and the majority of the crystals appeared to be slightly Se poor, the Se/(Cu+Ga+In) ratio was not found to be dependent on position and starting Ga content. However, three trends can be observed from the results of Cu/(Ga+In) and Ga/(Ga+In) ratios. These trends could be explained qualitatively with the help of the established pseudobinary phase diagrams. The Cu₂Se-In₂Se₃ [3.44,49,51,53] and Cu₂Se-Ga₂Se₃ [3.50,56] pseudobinary phase diagrams have been reported by various authors. Earlier studies suggested that CuInSe₂ melts congruently at the stoichiometric composition [3.49,51]. However, recent detailed studies showed that CuInSe₂ indeed melts incongruently at the stoichiometric composition with the maximum of the liquidus

located at the In₂Se₃ rich side [3.44,53]. On the other hand, there has been no ambiguity that CuGaSe₂ melts incongruently with the maximum of liquidus located at the Ga₂Se₃ rich side and the compound goes through a peritectic melting at about 1030 °C [3.50.56]. In Fig. 3.4, the latest version of the pseudobinary phase diagrams for Cu₂Se-In₂Se₃ [3.53] and Cu₂Se-Ga₂Se₃ [3.50] systems are partially reproduced and plotted in the same temperature scale. The melting point of CuInSe₂ (~ 987 °C) [3.51.52.54] and peritectic melting point of CuGaSe₂ (~ 1030 °C) [3.50,56] are also indicated. The three observable trends are explained with reference to Fig. 3.4. In evaluating the composition data, one should keep in mind that the main attentions should be put on the tendency of the composition variation rather than the absolute values. This is because a nominal error of \pm 0.5 atom. % is usually present in EPMA measurements and measurements are carried out only at approximate positions.

As shown in Table 3.1, the Cu/(Ga+In) ratio has a tendency to increase from the first-to-freeze zone towards the last-to-freeze zone. The fact that both CuInSe₂ and CuGaSe₂ were found not to melt congruently at the stoichiometric composition, and the maximums of the liquidus lines are both located on the Cu₂Se poor side of the pseudobinary phase diagrams account for the variation of Cu/(Ga+In) ratio along the ingot. Upon cooling, one could expect Cu poor phase to freeze first. Further cooling on the melt will result in Cu richer compound. Indeed, this trend could also be observed from early results obtained by Mandel et al. [3.20] on zone grown CuGaSe₂ ingots. Tomlinson [3.47] also discussed this trend on his review of CuGaSe₂ crystal growth.

Detailed inspection on the recent composition results obtained in our laboratory on vertical Bridgman grown CuInSe₂ ingots [3.46] also indicated a similar tendency.

The second observable trend is the reduction in Cu/(Ga+In) ratio as the starting Ga content increases. As can be seen from Fig. 3.4, the maximum of the liquidus for the Cu₂Se-Ga₂Se₃ and Cu₂Se-In₂Se₃ systems are located at about 65% of Ga₂Se₃ and 55% of In₂Se₃, respectively. Thus, the phenomenon of Cu poor is expected to be more severe in the Cu₂Se-Ga₂Se₃ system. Therefore, as the starting Ga content increases, the situation of Cu poor is expected to progress as well.

Finally, the Ga content tends to decrease from the first-to-freeze zone towards the last-to-freeze zone. Since the liquidus of the Cu₂Se-Ga₂Se₃ system is above that of the Cu₂Se-In₂Se₃ system, upon freezing, Ga rich phase would preferentially be solidified rather than In rich phase. This hypothesis is supported by a study on CuInSe₂-CuGaSe₂ phase diagram [3.39]. When the CuInSe₂-CuGaSe₂ liquid solution was freezed, the first phase came across was a Ga rich phase rather than an In rich phase. In addition, Ciszek [3.40] actually found that the segregation coefficient of Ga is greater than that of In in vertical Bridgman/Stockbarger grown Cu(Ga,In)Se₂ ingots. This difference in segregation coefficient agrees with the present result. The present result of composition analysis was first presented in PVSEC-9 (1996) in Japan. In the same conference, a similar tendency on the Ga/(Ga+In) ratio was also reported in Cu(Ga,In)Se₂ ingots prepared by traveling heater method [3.45].

3.4 X-Ray Diffraction Studies

X-rays are radiations with wavelengths in the order of 1 Å, which is the same order of magnitude as the lattice spacings of crystals. Therefore, x-rays can be used to gather information on crystal structure and lattice constants. When a monochromatic x-ray beam is incident on a surface at an angle, part of the beam is deflected. At certain incident angle, θ , the scattered x-rays from adjacent crystal planes (as shown in Fig. 3.5 (a) [2.9]) are in phase if their path differences are multiples of the x-ray wavelength. If such a condition is met, the intensity of scattered x-rays reaches a maximum due to constructive interference. The equation governing the condition for constructive interference is Bragg's Law,

$$2d\sin\theta = n\lambda \quad (3.1)$$

where d is the lattice spacing, θ is the x-ray incident angle, n is an integer number and λ is the wavelength of incident x-ray beam.

Fig. 3.5 (b) [2.9] shows the schematic diagram of a modern x-ray diffractometer. It should be noted that the x-ray beam is deflected through an angle of 2θ by the diffraction. In the powder x-ray diffraction (XRD) method, the sample is in the form of tiny crystal grains with random crystal orientations. When there are a large number of crystal grains with different crystal orientations, there are bound to be some crystal planes which satisfy the Bragg's law at certain incident angle, θ . By changing the incident angle, diffraction maxima for different crystal planes could be obtained at different values of θ . The corresponding d spacings are characteristics for a material with a particular crystal structure. By comparing the obtained powder x-ray diffraction pattern with established crystal data, the crystal structure and the existence of different phases can be identified. Lattice constants can also be determined from the diffraction pattern.

In the present work, powder x-ray diffraction measurements were carried out on $CuGa_XIn_{1-X}Se_2$ samples grown from stoichiometric melt and a $CuGaSe_2$ sample grown from Cu_2Se rich melt. A RIGAKU D/MAX 2400 x-ray diffractometer with a characteristic wavelength of 1.54059 Å was used. The resulting x-ray diffraction patterns were compared with the established crystal data [3.57-59,76]. Crystals extracted from the main portion of the as-grown ingots were used.

3.4.1 CuGa_XIn_{1-X}Se₂ Grown from Stoichiometric Melt

Cu poor samples with Cu/(Ga+In) ratios ranging between 0.8 and 1 were studied. Despite the low Cu/(Ga+In) ratios for some of the samples, samples grown from stoichiometric melt were found to have single phase chalcopyrite structure. Indeed, previous results from our laboratory in non-stoichiometric CuInSe₂ crystal growth showed that single phase chalcopyrite structure could be maintained for a Cu/In ratio as low as 0.79 [3.60]. Furthermore, according to the pseudobinary phase diagrams, both chalcopyrite CuInSe₂ [3.53] and CuGaSe₂ [3.50] were believed to tolerate a Cu/In or Cu/Ga ratio of about 0.8. The powder x-ray diffraction pattern of a CuGa_{0.44}In_{0.56}Se₂ crystal showing a single phase chalcopyrite structure is shown in Fig. 3.6.

The lattice constants for samples with different Ga contents were determined by successive approximation method. Similar methods have been used by various authors in determining the lattice constants of CuInSe₂ [3.57], CuGaSe₂ [3.58] and CuGa_XIn_{1-X}Se₂ [3.42] crystals. The method used in the present case is briefly described below.

In a tetragonal system, the values of lattice constants, a and c, are given by

$$a = \frac{\lambda}{2\sin\theta} \left[(h^2 + k^2) + \frac{l^2}{(c/a)^2} \right]^{\nu_2} \quad \text{and} \tag{3.2}$$

$$c = \frac{\lambda}{2\sin\theta} \left[\left(\frac{c}{a}\right)^2 (h^2 + k^2) + l^2 \right]^{1/2} , \qquad (3.3)$$

where *h*, *k*, and *l* are the Miller index representation correspond to a specific diffraction peak at an x-ray incident angle θ . To calculate the lattice constant *a*, the first step is to obtain an approximate value for the axial ratio c/a, namely c_0/a_0 . For instance, it has been established that the c/a ratios of CuInSe₂ and CuGaSe₂ were around 2.01 and 1.97, respectively [3.57-59]. Therefore, in this case, the values of c_0/a_0 was taken as 2.01. The c_0/a_0 ratio is then substituted into Eq. 3.2 to calculate the values of *a* for various diffraction peaks on the diffraction pattern. These values of *a* are then extrapolated against Nelson and Riley extrapolation function $(\cos^2\theta/2\sin\theta + \cos^2\theta/2\theta)$ [3.63] to find a more accurate value of *a*, namely a_1 . The value of c_1 is found in a similar manner by using Eq. 3.3. This process is repeated with the new ratio, c_1/a_1 , to find more accurate values of lattice constants, namely a_2 and c_2 . Usually, four to seven extrapolations are sufficient to yield parameters with high accuracy.

To confirm the accuracy of the present procedure, the obtained lattice constants of the two end point compounds, CuInSe₂ (a = 5.782 Å, c = 11.619 Å) and CuGaSe₂ (a = 5.613 Å, c = 11.042 Å), were compared to other crystal data [3.57-59] as well as early CuInSe₂ results from our laboratory (a = 5.789 Å, c = 11.612 Å) [3.61]. It was found that the latest results are in good agreement with the above published data and the worst case difference was less than 0.2 %.

The present results (**m**) are plotted in Figs. 3.7 (a) and (b) together with other published data [3.37,39,42-43,59,62] on CuGa_XIn_{1-X}Se₂ ($0 \le x \le 1$) crystals. It was found that the lattice constants generally varied linearly with Ga content (x) and the present results have good agreement with the published data. Although the studied crystals were generally Cu poor, the lattice constants do not appear to be affected by the Cu/(Ga+In) ratio. In addition, while several reports have suggested that the lattice constants were linear functions of Ga content (x) [3.37,39,43,59], the lattice constants obtained by different researchers were found to scatter within a narrow margin due to various systematic and random errors. Therefore, to establish more meaningful relationships between Ga content and lattice constants, linear fits were obtained from all the data shown in Figs. 3.7 (a) and (b). Accordingly, the lattice constants, *a* and *c*, were found to be fitted by the following two linear functions,

$$a = 5.781 - 0.173 x$$
 Å ± 0.019 Å and (3.4)
 $c = 11.614 - 0.594 x$ Å ± 0.066 Å. (3.5)

The two linear functions were obtained using least square fitting method. Although the above two equations might not give the absolute values of the lattice constants, they could give the readers quick and reasonable estimations on the lattice constants of $CuGa_XIn_{1-}$ $_XSe_2$ compounds. These two equations are also found to have excellent agreement with the latest thin film results (1998) [3.84].

While the lattice constants (a and c) could be readily fitted by linear functions, the axial ratio (c/a) appears to vary non-linearly. Fig. 3.8 shows the plot of axial ratio as a function of Ga content, a trend line is also shown. The c/a ratio varies approximately from 2.005 to 1.965 as x goes from 0 to 1. From Fig. 3.8, the c/a ratio is found not to be a strong function of Ga content for 0 < x < 0.3. For 0.3 < x < 0.7, the c/a ratio is found to decline in an almost linear fashion as x increases. The rate of reduction slightly decreases as x continue to increase.

3.4.2 CuGaSe₂ Grown from Cu₂Se Rich Melt

According to early report on zone leveling of CuGaSe₂, size of CuGaSe₂ crystals could be increased by growing the crystals from 7 wt. % Cu₂Se enriched melt [3.20]. It is therefore interesting to study the effect of Cu₂Se enriched melt on Bridgman grown crystals. Experiments were carried out to grow CuGaSe₂ crystals from Cu₂Se enriched melt, however, no increase in crystal size was observed in the present case. X-ray diffraction results showed that multi-phase crystals were obtained in the main region of an ingot. The x-ray diffraction pattern of a CuGaSe₂ sample grown from 5 wt.% Cu₂Se enriched melt is shown in Fig. 3.9. Most of the diffraction peaks could be identified as belonging to the chalcopyrite phase of CuGaSe₂ [3.58-59], except the two peaks as indicated by arrows in Fig. 3.9. These two peaks indicated the presence of extra phase(s). The measured *d* spacings for these two peaks were 2.030 Å and 3.324 Å. By comparing the *d* spacings with the JCPDS x-ray diffraction records for all possible binary and ternary compounds, it was found that the Cu_{1.85}Se [3.64] compound has the closest match. The two extra peaks matched the first (d = 2.03 Å) and second (d = 3.33 Å) highest intensity lines of the Cu_{1.85}Se diffraction file. The existence of such a Cu_xSe phase was also observed in vacuum evaporated CuGaSe₂ thin films [3.83].

It is interesting to note that early results from our laboratory on vertical Bridgman growth of non-stoichiometric CuInSe₂ showed evidence of $In_3Se_2+Cu_{0.65}In_{0.35}$ and Se phases in the main region of the ingots grown from In and Se enriched melts [3.65], respectively, although the extra phases were mainly found in the last-to-freeze zone of the ingots. The existence of extra phases in CuInSe₂ and CuGaSe₂ indicated the difficulties in growing single phase CuGa_xIn_{1-x}Se₂ crystals from non-stoichiometric melts using the Bridgman method.

3.5 Electrical Characteristics

The conduction type of as-grown CuGa_XIn_{1-X}Se₂ ingots were examined using the hot-point probe method. All the as-grown crystals appeared to be p-type regardless of atomic composition. Our laboratory recently discovered that n-type CuInSe₂ crystals resulted only when the In (a group III element) concentration in the starting melt was greater than 25 % [3.46,82]. It is possible that a similar analogy could be extended to Cu(Ga,In)Se₂ and CuGaSe₂ crystals. Since the starting composition of group III elements (Ga+In) was always 25 % in this case, a p-type conduction was expected. Moreover, a p-type conduction was also reported in CuGa_XIn_{1-X}Se₂ crystals prepared by liquid encapsulated vertical Bridgman/Stockbarger method (with 3 mole % Se enriched melt) [3.42] and chemical vapour transport [3.37]. On the other hand, n-type conduction was

found in $CuInSe_2$ and $Cu(Ga.In)Se_2$ crystals prepared by solution growth (traveling heater method) [3.45] using In as solvent - it was possible that the excessive In presented in the melt led to n-type conduction.

The electrical characteristics of as-grown CuInSe₂ [2.8-9, 3.5,7,11,13,26,29-30.49.54-55,60-61,66-70,73-74,77], CuGaSe₂ [3.18,20,24,71-73] and Cu(Ga,In)Se₂ [3.37,42,45] crystals have been reported by various authors. The room temperature resistivities of p-type CuGa_XIn_{1-X}Se₂ were reported to span a wide range from 0.01 to 1.9 x 10⁵ Ω -cm. In the present case, the resistivity of the as-grown CuGa_XIn_{1-x}Se₂ crystals was measured using the van der Pauw method [4.78-81]. The resistivity was found to vary between 1 and 15 Ω -cm regardless of the atomic composition. This result is in general agreement with previous CuInSe₂ results from our laboratory [2.9, 3.13,55,60-61,74,77]. According to our previous results, resistivity in p-type CuInSe₂ crystals ranged from 0.4 to 156 Ω -cm. The present result is also comparable to results obtained in CuGaSe₂ crystals grown by directional freezing [3.72] and zone leveling [3.20,71], although resistivities as high as $1.9 \times 10^5 \Omega$ -cm have also been reported on CuGaSe₂ crystals grown by zone leveling [3.18] and the traveling heater method [3.24]. Furthermore, certain tendencies in resistivity of CuGa_xIn_{1-x}Se₂ crystals have also been reported previously. Paorici et al. [3.37] observed a reduction in resistivity from 100 to 0.01 Ω -cm as x increased from 0 (CuInSe₂) to 1 (CuGaSe₂) for crystals prepared by chemical vapor transport. While the results obtained by Ciszek et al. [3.42] suggested an opposite trend on crystals prepared by vertical liquid-encapsulated Bridgman/Stockbarger method. Their results showed an increase in resistivity from 1 to 250 Ω -cm when x was

increased from 0 to 0.83. Although both of the above two tendencies are not observed in the present case, the results are indeed confined within the above two ranges.

3.6 Conclusions

In this chapter, the crystal growth conditions of horizontal Bridgman grown CuGa_XIn_{1-X}Se₂ were reported. It was discovered that adhesion free ingots could be obtained using partially carbon coated ampoules over the whole composition range. Using the optimum growth conditions, single crystals with linear dimensions ranging from 5 to 10 mm were grown using a commercial horizontal furnace. The variation in compositions for ingots with different starting Ga contents were studied and the results were explained qualitatively by the established pseudobinary phase diagrams. Furthermore, x-ray diffraction measurements were carried out to confirm crystal structure and determine lattice constants. All the samples grown from stoichiometric melts showed a single phase chalcopyrite structure. The lattice constants found in the present case generally agreed with other published data. Two linear functions were obtained to summarize the relations between Ga content and lattice constants based on results obtained in the present study as well as results reported by other research groups. Finally, from electrical measurements, all the samples were found to have p-type conduction regardless of atomic concentrations. The measured resistivity was found to agree with other published results.





Fig. 3.1. (a) Schematic diagram of a partially carbon coated ampoule. (b) Diagram showing the approximate positions where composition analysis was carried out.



Fig. 3.2. (a) Schematic diagram of the complete horizontal Bridgman crystal growth system [2.9]. (b) Temperature plotted against distance from center of furnace.





Fig. 3.3. A picture showing a polished crack-free and void-free CuGa_{0.15}In_{0.85}Se₂ single crystal.



Fig. 3.4. Cu₂Se - In₂Se₃ and Cu₂Se - Ga₂Se₃ pseudobinary phase diagrams [3.50,53].



Fig. 3.5. (a) Scattering of x-rays from adjacent lattice planes. The path difference is $2d\sin\theta$. (b) Schematic diagram of an x-ray diffractometer.



Fig. 3.6. Powder x-ray diffraction pattern for a CuGa_{0.44}In_{0.56}Se₂ crystal showing a single phase chalcopyrite structure.


Fig. 3.7. Lattice constants, (a) a and (b) c, plotted as a function of Ga content (x).



Fig. 3.8. Axial ratio, c/a, plotted as a function of Ga content (x).



Fig. 3.9. Powder x-ray diffraction pattern of a multi-phase CuGaSe₂ sample grown from Cu₂Se enriched melt.

OPTIMIZATION OF THE CELL FABRICATION PROCESS

4.1 Introduction

In the present work, Bridgman grown p-type $CuGa_XIn_{1-X}Se_2$ single crystals were used as the substrates to fabricate PV cells. The PV cells utilized a $ZnO/CdS/CuGa_XIn_{1-X}Se_2$ structure. The n-type window was formed using CdS and ZnO films prepared by chemical bath deposition (CBD) and rf-sputtering, respectively. A similar structure had been used to fabricate PV cells on both single crystal CuInSe₂ [2.9, 4.1-5] substrates in our laboratory and CuGaSe₂ substrates by Saad et al. [4.6-7].

The fabrication procedures consisted of five steps: (1) preparation of single crystal substrates, (2) deposition of CdS films by chemical bath (CBD) method, (3) deposition of ZnO films by rf-sputtering, (4) deposition of front and back contacts by vacuum evaporation, and (5) defining cell areas by photolithography. A schematic diagram showing the structure of a single crystal ZnO/CdS/CuGa_XIn_{1-x}Se₂ PV cell is shown in Fig. 4.1. In this chapter, each of the five fabrication steps and the corresponding process optimization will be discussed in detail. Special attention was paid to establishing cell fabrication conditions which are time efficient and have high consistency for routine studies.

4.2 Preparation of Substrates

Single crystal substrates were selectively cut from the as-grown $CuGa_xIn_{1-x}Se_2$ ingots. Most of the substrates had typical sizes between 10 and 25 mm² with a thickness of about 1 mm. Due to the lengthy crystal growth process, limited amounts of single crystal substrates were available. Selecting substrates with designated orientations appeared to be difficult. Therefore, substrates with random orientations were used. Indeed, previous results from our laboratory on single crystal ZnO/CdS/CuInSe₂ PV cells suggested that the cell performance was not affected by the substrate orientation [2.9, 4.3]. According to the thin film results, high quality PV cells were usually fabricated on Cu deficient films with Cu/(Ga+In) ratios ranging between 0.8 and 1 [4.8-11,14,86]. Since most of the crystals obtained were Cu deficient as stated in chapter 3, accordingly, $CuGaxIn_{1,x}Se_2$ single crystals with similar Cu/(Ga+In) ratios were used for cell fabrication. The substrate preparation techniques used in the present work were modified from a process previously employed to fabricate single crystal CuInSe₂ cells [2.9, 4.3]. The substrate preparation started with lapping both sides of the substrates with a grit 600 silicon carbide paper mounted on a rotating polishing wheel. One side of the substrate was polished with 6 µm and then 1 µm diamond abrasive. The final polishing step was done by using 0.05 µm alumina paste.

Previously [2.9], about 30 to 45 minutes of polishing time was needed for each step and only one substrate was mounted in a sample holder for each polishing run. Hence, the minimum total polishing time for each substrate was approximately 1 1/2 hour. Since our laboratory is not equipped with an automatic polishing system, the sample holder with mounted substrate had to be held using bare hands during the whole polishing process. This led to significant physical stress for the operator, especially when more than one sample was prepared in the same day. Therefore, in the early stage of the present study, two time efficient practices were introduced to reduce the chance of repetitive stress injury. It was found that up to six substrates could be mounted onto the same sample holder and polished at the same time. No noticeable differences at the polished surfaces were observed after implementing this multi-substrate polishing scheme. Furthermore, the polishing time was reduced from 30 minutes to 15 minutes for each polishing step. It was discovered that any polishing time less than 10 minutes for each step led to poor quality or irreproducible results. A polishing time of at least 15 minutes was found to give reproducible mirror like surfaces. These two practices reduce the effective polishing time for each sample to about 1/10 of the original duration needed. No evidence of compromise in PV cell performance was found after the implementation of this time efficient polishing process.

After the polishing steps, the polished surface appeared to be mirror like with no visible scratches. However, scratches were observable under the scanning electron microscope (SEM). Variations of the present polishing steps have also been applied to study metal contacts [4.61,63-64] and fabricate PV cells on single crystal CuInSe₂ [4.67] substrates by other laboratories. Following the polishing, the substrates were rinsed using trichloroethylene (TCE), acetone (ACE) and then de-ionized (D.I.) water to remove contaminations resulting from the polishing. The substrates were then etched in a Brmethanol solution (0.5 % Br by volume). The etching time was kept below one minute.

Etching times longer than one minute, and higher concentration solutions were avoided to prevent excessive etching, which could result in non-stoichiometric surface atomic concentrations and etch pits [2.9, 4.12-13]. Early results from our laboratory suggested that abrasive polishing created a damaged layer at the polished surface of CuInSe₂ crystals and this damaged layer could be removed by chemical etching [3.15]. Thus, the purpose of the etching was to remove the thin damaged layer and the surface oxide formed after polishing. Following the etching, the substrates were rinsed by D.I. water and then dried using pure nitrogen or argon stream. Br-methanol is a common etchant for CuInSe₂ and other semiconductors. It has been used to study metal contacts [4.61-64] and to fabricate PV cells on single crystal CuInSe₂ [4.67,69] and InP [4.15] substrates. Although other etchants such as HCl + HNO₃ and diluted HF have also been used to fabricate PV cells on single crystal CuInSe₂ [4.66,70-71], CuGa_{0.5}In_{0.5}Se₂ [4.68] and CuGaSe₂ [4.72] substrates, previous results from our laboratory and others suggested Br was the most favorable etchant [2.9, 4.12-13]. Figs. 4.2 (a) and (b) show the SEM photographs of as-polished and Br-methanol etched CulnSe₂ surface. From Fig. 4.2, the density of surface scratches was found to reduce substantially after etching.

After the etching step, the substrates were annealed in a flowing argon (Ar) environment at 350 °C for two hours. The purpose of this annealing step was to further reduce the surface defects induced by abrasive polishing as well as to minimize the bulk defects. The substrate annealing was found to be crucial in improving cell performance. This optimum annealing condition was previously established [2.9] by analyzing the effects of different combinations of annealing gas, temperature and time on the performance of single crystal ZnO/CdS/CuInSe₂ PV cells. A custom made furnace was used in this work. The schematic diagram is shown in Fig. 4.3 [2.9]. To reduce contamination, the substrates were loaded into the quartz tube right after the etching step. It was previously found that the presence of oxygen during annealing was detrimental to the cell performance. To reduce the effect of oxygen, the quartz tube with samples loaded was first flushed with Ar for 30 minutes before heating up the furnace. During the annealing, the temperature of the furnace was controlled to 350±5 °C by an electronic temperature controller. After annealing, the substrates were allowed to cool down to room temperature with a continuous flow of Ar before proceeding with the deposition of CdS thin films. In our laboratory, Ar substrate annealing was also found to be beneficial in improving cell performances of CdO/CuInSe₂ PV cells fabricated on cleaved single crystal substrates [3.46] as well as ZnO/CdS/CuInSe₂ PV cells fabricated on

4.3 Process Refinement on CdS Film Deposition

According to the latest results from polycrystalline thin film $CuGa_XIn_{1-X}Se_2$ [4.9,11,16-25,38-39] as well as single crystal $CuInSe_2$ [2.9, 4.3] and $CuGaSe_2$ [4.7], high performance PV cells were usually fabricated with a CdS buffer layer deposited using chemical bath deposition (CBD). The thickness of CdS ranged between 10 and 100 nm. The best cells appeared to have CdS thickness between 50 and 100 nm [4.18-19,22,25]. Usually, the spectral response of the PV cells at short wavelengths would be reduced by the use of thicker CdS films [4.30,35]. This is due to the reduced optical transmission for photons with energies close to the bandgap of CdS (~ 2.4 eV) when a thicker CdS film is used. However, a CdS thickness which is too thin could result in poor junction quality. Thus, the CdS thickness is usually a trade off between junction quality and spectral response. In our laboratory, it was found that a CdS thickness greater than 30 nm was capable of producing reasonably good junctions in both single crystal and thin film CuInSe₂ PV cells. The best cells in our laboratory were obtained with a CdS thickness of about 50 nm.

A large variety of chemical baths have been used to deposit CdS thin films. However, the most commonly used chemical baths consist of four chemicals. The four chemicals are: (1) a cadmium salt such as $CdCl_2$, CdI_2 or $Cd(CH_3COO)_2$, (2) thiourea: $CS(NH_2)_2$, (3) ammonium hydroxide: NH_4OH and (4) an ammonium salt such as NH_4Cl , NH_4I or NH_4CH_3COO . While the first three chemicals are essential, the ammonium salt is optional. In such a CBD process, the cadmium salt and thiourea act as the cadmium and sulfur sources, respectively. It is generally believed that the deposition follows the global reaction [4.36-37,48,50,56-57] as shown in Eq. 4.1.

$$Cd(NH_3)_4^{2+} + CS(NH_2)_2 + 2OH^- \rightarrow CdS + CH_2N_2 + 4NH_3 + 2H_2O$$
 (4.1)

In a typical CBD process, the formation of CdS could take place either heterogeneously or homogeneously. The heterogeneous growth mode was usually preferred since the CdS compound was formed right at the surface of the substrates by means of nucleation. In a homogeneous process, CdS particles were formed in the solutions and subsequently deposited onto the substrates. This could lead to an overall reduction in film quality. Moreover, chemical baths used for CdS deposition were found to remove the surface oxides of $CuGa_XIn_{1-X}Se_2$, which allowed the forming of CdS on an in-situ cleaned surface [4.41-44].

Our laboratory have previously deposited CdS thin films using water based solutions consisting of four chemicals: CdCl₂, CS(NH₂)₂, NH₄OH and NH₄Cl. Using the established conditions, PV cells were fabricated on both single crystal [2.9, 4.1-5] and polycrystalline thin film CuInSe₂ [4.26-27]. In addition to the application in CuGa_XIn₁. $_X$ Se₂ cells [4.7,16-18,19-22,28-30,39,91], CdS films deposited using CBD method with various deposition conditions and chemicals were also used to fabricate single crystal InP [4.15] PV cells as well as polycrystalline thin film CdTe [4.31-34] PV cells by other researchers. They were also applied to the fabrication of photoelectrochemical cells [4.45-46]. The studies of CdS thin film growth using various chemical baths were reported by different authors in Refs. [4.18,26-29,31-32,35-37,40-44,47-60,87].

The substrates used in this work were $CuGa_xIn_{1-x}Se_2$ crystals prepared using the substrate preparation techniques described in section 4.2 and microscope glass slides obtained from Fisher Scientific. Glass slides were mainly used for quality control purposes and to study various characteristics of the CdS thin films such as thickness, resistivity and optical transmission. Before the deposition, the glass slides (area = $2.5 \times 7.5 \text{ cm}^2$) were cleaned in an ultrasonic bath using TCE, ACE and then rinsed with D.I. water. For single crystal samples, the CdS thin films were deposited right after the substrate Ar annealing. This was done to ensure minimum contamination.

The deposition experiments were carried out in a warm water bath. In the early developing stage of the CBD process used in our laboratory [4.26-27], the temperature of

the water bath was controlled by flowing hot water. In this method, it was difficult to obtain reproducible deposition temperature, which led to inconsistent junction properties. Therefore, a hot plate was used to heat up the water bath in the present experiments to improve the temperature control. The schematic diagram of the present experimental setup is shown in Fig. 4.4. The deposition solution inside the inner beaker was formed by mixing 40 ml of solutions containing $CdCl_2 + CS(NH_2)_2 + NH_4Cl$ and 40 ml of diluted NH₄OH solutions. As a result, a total volume of 80 ml of deposition solution was used in each run. The beaker, containing deposition solutions, was first immersed into a preheated water bath. The temperature of the deposition solutions inside the small beaker reached 60 °C in about 8 to 10 minutes. Then the single crystal substrates and/or glass slides were immersed into the deposition solutions. In such a deposition set-up, the glass substrates were placed vertically while the $CuGa_xIn_{1-x}Se_2$ single crystals were suspended horizontally in the middle of the deposition solutions using a molybdenum (Mo) holder. The deposition was started when the substrates were first immersed into the chemical bath and ended when the substrates were removed from the chemical solutions. After the deposition, the substrates were then rinsed with D.I. water immediately and blown dry using nitrogen or argon. During the deposition, the temperature of the chemical bath was controlled to 60 ± 2 °C using the hot plate. The control of the bath temperature is much improved in the present case as opposed to the ±5 °C margin allowed in the original flowing water method. The thicknesses of the CdS films were measured using a DEKTAK surface profile measuring system. A film thickness of about 50 nm was

obtained for a 15 minute deposition. The variation in CdS film thickness from run to run was found to be within ± 10 %.

In the previous work [4.26-27], the concentration of NH_4OH in the chemical bath was controlled by applying concentrated ammonia solutions using pipette in a drop by drop basis (~ 30 drops). Depending on the type of pipette used and the size of the droplets, different concentrations could be resulted from run to run. Thus, this led to inconsistent film thickness and film quality. To obtain a highly controllable and reproducible process, pre-diluted NH4OH solutions were used in the present case to improve the consistency. Furthermore, when CdS depositions were carried out in the previous single crystal work, the single crystal substrates were placed at the bottom of the beaker as reported by Yip [2.9]. However, large CdS particles were often found to attach onto the surface of the crystals using such a configuration. The CdS particles were difficult to remove using water rinsing. Even if the particles were removed, CdS films with non-uniform thickness were resulted. Thus, by suspending the single crystal substrates in the middle of the solutions as in this work, the amount of CdS particles deposited on top of the substrates were substantially reduced. This led to higher film uniformity.

The CdS films prepared in our laboratory had a dark resistivity of about $5 \times 10^4 \Omega$ -cm. Under simulated AM 1.5 condition, the resistivity dropped by about two orders of magnitude [4.26-27]. Optical transmissions of the CdS films deposited on glass slides were measured using the setup shown in Fig. 4.5. The monochromatic light was supplied by a Beckman model DU Spectrophotometer equipped with an Oriel tungsten

light source. The measurements were done using a Si p-n junction detector connected to a Princeton Applied Research model 124A lock-in amplifier. The chopping frequency of the chopper (model 125A) was 136 Hz. The transmissions were calculated by comparing data between CdS/Glass and plain glass slides. The optical transmission plotted as a function of wavelength for a typical CdS film with a thickness of about 50 nm is shown in Fig. 4.6. A transmission about 80 % was observed at a wavelength of 0.5 μ m which corresponded to the bandgap of CdS. The optical transmission was greater than 90 % for wavelengths between 0.6 μ m and 1.2 μ m. This result is comparable to transmission data reported by Solarex Corporation [4.29] for CdS films with similar thickness.

CdS films prepared by the CBD method generally have a polycrystalline structure. Several research groups reported that the CBD CdS films possessed mixed hexagonal and cubic phases [4.53,57,59,90]. However, the growth of epitaxial films is also possible under carefully selected conditions [4.50,52]. Other details in previous optimization and characterization of CdS films deposited in this laboratory have been reported elsewhere [4.26-27]. Since it is outside the scope of this thesis, the details will not be described. By using the present optimized CdS deposition method, a high V_{OC} of 0.502 V was achieved on a single crystal ZnO/CdS/CuInSe₂ PV cell.

4.4 Process Refinement on ZnO Film Deposition

Zinc oxide (ZnO) is the most commonly used low resistivity window material employed in the fabrication of modern $CuGa_XIn_{1-X}Se_2$ PV cells [4.1-7,9-11,14,16-23,25-28,35,38-39,42]. Although cadmium oxide (CdO) [3.46, 4.1-2,4-5] has also been used in

our laboratory and indium doped tin oxide (ITO) in other laboratories [4.22,24,77], the best results were usually obtained using ZnO. Furthermore, ZnO was also used to fabricate high efficiency single crystal InP PV cells [4.15]. The most commonly used dopant for low resistivity ZnO films appears to be Al. The sheet resistance of the ZnO layer for most of the high efficiency laboratory cells varies between 15 and 25 Ω/\Box [4.17,19,22,25,39, 42]. The thickness generally ranges from 0.3 to 3 µm depending on deposition methods and experimental conditions [4.3,9,11,16,19,22,23,25,35,39,42]. Such a low resistivity ZnO layer was often deposited using rf-sputtering [4.16,19,21-22,25,28,35,39,42,74-76], although other deposition methods such as dc-sputtering [4.14,76,83], ion beam sputtering [4.11], metal-organic chemical vapor deposition (MOCVD) [4.23,83] and spray pyrolysis [4.91-92] have also been used.

In our laboratory, a single layer low resistivity ZnO was deposited directly onto the CBD CdS film to form the ZnO/CdS window structure using rf-sputtering. Conversion efficiencies higher than 10 % have been reported by our laboratory on single crystal CuInSe₂ PV cells using such a window structure [2.9, 4.3]. However, high efficiency thin film CuGa_XIn_{1-X}Se₂ cells reported in recent years often employed a two layer ZnO structure [4.11,16,19,21-22,28,39,42,74]. The ZnO window was formed by combining a low resistivity and a high resistivity layer. As a result, the window structure became ZnO(low ρ)/ZnO(high ρ)/CdS. The presence of a high resistivity ZnO layer was reported to improve junction quality and led to higher open circuit voltage. The thickness of the high resistivity layer usually ranged between 40 and 90 nm. Due to the increased fabrication complexity and equipment limitations, the double layer ZnO structure has not been adopted in our laboratory. Nonetheless, high efficiency thin film cells have been reported even without the use of a high resistivity ZnO layer [4.23,30,75-76], although the existence of such a high resistivity ZnO layer could improve the thermal stability of the cells [4.76]. In the present work, the ZnO films were deposited by planar magnetron rf-sputtering. The original method was previously developed in our laboratory [4.73,78-82] and eventually used to fabricate single crystal and polycrystalline thin film CuInSe₂ PV cells [4.1-5,26-27].

The depositions were carried out in a Varian vacuum system (Model Turbo-V450) equipped with a 4-inch diameter water cooled rf-sputtering gun (US Inc.). The target used in the present case was a 2 wt.% Al₂O₃ doped ZnO ceramic disc with a diameter of about 7 cm. Argon (Ar) was used as the sputtering gas. The rf power supply and tuner were supplied by Advanced Energy (Model ATX 600 and RFX 600). Fig. 4.7 shows a schematic diagram [4.26] of the experimental setup. As shown in the figure, the substrates were mounted onto a water cooled substrate holder. The purpose of the water cooling was to reduce the undesirable heating effect of the substrates during the deposition. Using such a configuration, the temperature of the substrates was kept below 100 °C during deposition. Furthermore, the substrates were placed at an angle of about 45° from the target surface [4.26,73]. This was done to reduce the damage of bombardment by high energy particles at right angle. With reduced bombardment, the crystalline quality of the ZnO films was found to improve [4.26].

After the samples had been loaded into the vacuum system, the system was allowed to pump to a pressure of about 5 x 10^{-6} Torr. High purity Ar gas was then

introduced into the vacuum system at a maximum flow rate. The system was allowed to flush with Ar for at least 1/2 hour before sputtering. The flushing step was found to be crucial in obtaining ZnO films with high optical transmission. According to the present author's experience, the existence of even very small amount of oxygen could lead to a dramatic decrease in optical transmission of the ZnO films. After the Ar flushing, the pressure of the vacuum chamber was adjusted to a specific value by changing the flow rate of Ar. At this point, the rf power supply was switched on. The deposition was allowed to go on for as long as eight hours. After turning off the rf power upon finishing sputtering, the sputtering gun was allowed to cool for 10 minutes before switching off the vacuum unit.

Previously, the ZnO deposition was optimized for the use of an Al₂O₃ doped ZnO powder target [4.26]. However, there are some drawbacks in utilizing a powder target. First, the fine powder tends to contaminate the vacuum chamber and reduce the performance of the pumping unit. Second, the reproducibility and uniformity of the ZnO films depend strongly on the thorough mixing of the ZnO and Al₂O₃ powders. With these two disadvantages in mind, a sintered ceramic target was acquired to replace the powder target. After the utilization of the ceramic target, it was found that sheet resistance below $30 \ \Omega/\Box$ was not achievable even after eight hours of sputtering by using the conditions optimized for the powder target. Therefore, prior to the fabrication of PV cells, preliminary experiments were carried out to determine the optimum power and pressure to be used. It was found that rf powers greater than 100 W heated up the sputtering gun significantly. Generally speaking, deposition rate was found to increase with an

increasing power, therefore, to maximize the deposition rate without creating severe heating problem, a power of 100 W was used for the ZnO deposition.

In order to find the optimum chamber pressure, a set of experiments was carried out to determine the effect of pressure on sheet resistance. In each deposition run, five samples were obtained. The sheet resistance was measured using a four point probe method. The average values of five samples obtained in each run are plotted against deposition pressure in Fig. 4.8. All the ZnO films were deposited for three hours using a power of 100 W. As shown in Fig. 4.8, the average sheet resistance was reduced from about 155 Ω/\Box to 50 Ω/\Box when the pressure was increased from 4 to 14 mTorr. Thickness measurements revealed that the reduction in sheet resistance was mainly due to the increase in film thickness. The film thickness was increased from about 0.2 µm to 0.6 µm when the pressure was increased from 4 to 14 mTorr. Therefore, it can be concluded that 14 mTorr produced the highest deposition rate when sintered target is used. Accordingly, in all the subsequent experiments, the pressure and power were set to 14 mTorr and 100 W, respectively. Under this condition, ZnO films with a sheet resistance of about 20 Ω/\Box were routinely obtained after seven hours of deposition. The corresponding film thickness and resistivity were 1.5 μ m and 3 x 10⁻³ Ω -cm. The film resistivity was comparable to value obtained using powder target [4,26]. It is interesting to note that both the resistivity and optical transmission of the ZnO films are not found to be affected by the rf power and pressure used in the range of investigation.

The optical transmission of a typical 20 Ω/\Box ZnO film deposited on glass is shown in Fig. 4.9. At a wavelength of 0.4 μ m, the transmission was about 66 %. For wavelengths from 0.45 μ m to 0.95 μ m, the transmission varied between 80 % and 93 %. Beyond 0.95 μ m, the transmission was found to decrease steadily. The reduced optical transmission in the near infra-red region is commonly seen in low resistivity ZnO films [4.19,29-30,35,74,75,85]. Since the electron concentration of such a low resistivity ZnO film was previously found to range between 10²⁰ and 10²¹ cm⁻³ [4.84] in our laboratory, it is believed that free carrier absorption could dominate the transmission characteristics at the near infra-red region. The present transmission result was comparable to ZnO films prepared in our laboratory using powder target [4.26].

It has been previously established that ZnO films prepared in our laboratory using such a specific configuration have a highly oriented polycrystalline wurtzite structure [4.26,84] with *c*-axis perpendicular to the substrate. The highly oriented nature of the ZnO film is confirmed by the cross-sectional SEM image of a ZnO/CdS/CuInSe₂ PV cell as shown in Fig. 4.10. The grains are in the form of columns with a width of about 0.15 μ m. Such a columnar structure confirms the highly oriented nature of the ZnO film is too small (0.05 μ m) to be distinguished clearly in the SEM image. It can be seen from the figure that the polished surface has a surface flatness of about ±0.1 μ m.

4.5 Deposition of Metal Contacts

In this work, gold (Au) and aluminum (Al) with a purity of 99.999 % were used as the back and front contacts for single crystal $ZnO/CdS/CuGa_XIn_{1-X}Se_2$ cells, respectively. The metal contacts, with thickness about 2 μ m for each of Au and Al, were deposited using conventional vacuum evaporation at a base pressure of about 5 x 10⁻⁶ Torr. The high purity Au was in the form of strips with a thickness of about 0.5 mm. The Al was in the form of wire with a diameter of about 1 mm. To carry out the evaporation, Au was evaporated using a Mo boat and Al was evaporated using a tungsten filament. The Au back contact was deposited over the entire substrate, while the Al front contact had a circular shape. It was deposited through a metal mask to define the contact area.

Gold has been widely used as back contact for single crystal CuInSe₂ [3.46, 4.1-5,65-67], CuGaSe₂ [4.6-7] and CuGa_{0.5}In_{0.5}Se₂ [4.68] PV cells. Although Pt has also been used to fabricate single crystal CuInSe₂ PV cells [4.69], Au remains the most popular contact material for p-type single crystal CuGa_XIn_{1-x}Se₂ which could provide stable contacts with low contact resistance [4.61-64] - among materials such as Mo, Ni, Pt, In-Ga alloy and Au-Be alloy. Prior to the deposition of Au, the back sides of the substrates were lapped with a grit 600 silicon carbide paper to remove the surface layer. This lapping created a freshly damaged surface which was found to be beneficial in obtaining low resistance back contacts.

Several metals such as Ni [4.11,16,19,20-22,25,28-29,38], Al [2.9, 4.1-5,20,23,26-27] and In [4.6-7] have been used as the front ohmic contacts to ZnO/CdS/CuGa_XIn_{1-x}Se₂ PV cells. Since Ni has a high melting point (m.p. = 1726 °C), the control of the evaporation process is usually more difficult than for Al and In. According to the experiences of our laboratory, Al contacts generally give lower contact resistance and have better thermal stability than In contacts. Hence, Al was chosen as the front contact metal in this work. Our laboratory has been using Al front contacts in both single crystal [4.1-5] and polycrystalline thin film [4.26-27] ZnO/CdS/CuInSe₂ PV cells without any noticeable compromise in cell performance. In the case where soldering was necessary, an In layer with similar thickness was deposited on top of the Al contact without breaking the vacuum. In such a case, the soldering was done using a low melting point (\sim 70 °C) Wood's alloy. Also, to avoid excessive heating, a low temperature (\sim 100 °C) soldering iron was used.

4.6 Optimization on Cell Area Patterning

After depositing the back and front contacts, a UV photolithography step and wet chemical etching were carried out to define the circular cell area. The photolithography step was implemented using the microelectronics fabrication facility in our laboratory. The present cell area patterning process was an optimized version of the method originally employed by the present author to pattern InSb (a III-V semiconductor) [4.88] and BiSrCaCuO (a high temperature superconductor) [4.89] thin films for electrical studies. In the present case, an in-house produced chromium photomask made on an ultra-flat glass plate was used. The procedures are outlined as the following:

- (1) Spin positive photoresist (Shipley AZ 1350) at 6000 rpm for 15 seconds.
- (2) Pre-bake at 75 °C for 10 minutes.
- (3) Expose under UV light (Oriel) for 150 second through a chromium photomask.
- (4) Develop in photoresist developer for 30 seconds followed by D.I. water rinsing.

- (5) Post-bake at 75 °C for 10 minutes.
- (6) Etch the sample in diluted HCl solutions (HCl:H₂O = 1:5 by volume) for 10 to 15 seconds followed by D.I. water rinsing.
- Rinse the sample in acetone (ACE) to remove photoresist followed by D.I. water. (7) In establishing the above procedures, several important factors were studied. Firstly, due to the small size of the substrates used, the spinning speed of the photoresist played an important role in determining the quality of the resultant photoresist layer. A too low spinning rate would result in a thick photoresist with non-uniform thickness, which was found to be difficult to process in subsequent steps. However, a too high spinning speed could result in very thin layers of photoresist, which were often found to have pin holes. By using the stated spinning rate, the photoresist was found to be uniform in thickness with an absence of pin holes. Secondly, to reduce the effect of undesirable annealing during pre-bake and post-bake, baking temperatures and baking times should be minimal. However, a baking time which is too short, or a baking temperature which is too low, could result in various fabrication defects such as pin holes and/or severe undercut. The present baking conditions were found to be the lowest baking temperature and time possible for a highly reproducible process with good results. Finally, the concentration of the etching solutions was also found to be a crucial factor. While ZnO could be etched easily for a concentration as low as 1:40 (HCl:H₂O by volume), the CdS film underneath was found to be difficult to etch using such a low concentration etchant. However, a high concentration etchant was found to result in severe undercut which led to the partial striping off of photoresist. This had significant impact on reproducibility.

This large difference in etching property made the control of uniform etching difficult. The concentration used in the present case (1:5) was a compromise between etching rate and the undercutting condition. This concentration allowed thorough etching of the combined ZnO/CdS structure with controlled uniformity.

As a result of the contact metallization and cell patterning, PV cells with two different sizes were fabricated. The larger cells have the total cell area, front contact area and active area of 5.40 mm², 0.51 mm² and 4.89 mm², respectively. The corresponding dimensions of the smaller cells were 2.37 mm², 0.51 mm² and 1.86 mm², respectively. These dimensions of PV cells were chosen such that the cell area could be fitted into most of the $CuGa_xIn_{1-x}Se_2$ substrates. The stated cell dimensions were measured by a traveling microscope. The accuracy of the traveling microscope was confirmed by a standard microscope scale. The error margin in the determination of active cell area for each cell was estimated to be ± 1 %. The present optimized patterning procedures were found to be highly reproducible. The difference in active cell area was found to fall within ± 1.5 % from cell to cell. Therefore, the total error margin in active cell area determination was about ± 2.5 % when the error in cell area measurement and deviation in cell area from sample to sample were taken into account. In the present case, the shadings due to the Al front contact were about 9 % for large and 22 % for small area cells. These shading ratios were typically a few times larger than that of the high efficiency laboratory thin film cells [4.11,19,25,28,39]. Since probing or soldering would be extremely difficult in subsequent characterizations if smaller Al contacts were used, the shading could not be made smaller

in the present case. The present process could also be applied to pattern thin film cells without modification.

4.7 Conclusions

Each of the fabrication steps with various process optimizations was discussed in detail. First of all, a time saving polishing process is implemented in the present study. Such a process shortened the polishing time significantly with no compromise in device quality. Consequently, the physical stress on the operators was greatly reduced. Second, an improved CdS deposition process was applied to cell fabrication. This improved process leads to highly controllable and consistent depositions through enhanced control of bath temperature, ammonia concentration and film uniformity. Third, the deposition of low resistivity ZnO films was optimized for the newly acquired ceramic target. Highly transparent and uniform ZnO films with a sheet resistance of 20 Ω/\Box were routinely obtained using the optimum deposition conditions. Finally, the patterning procedure was optimized to give highly reproducible results by taking into account the photoresist spinning rate as well as baking and etching conditions. The cell and front contact areas were specifically designed and optimized for single crystal substrates.

Most of the optimization works presented in this chapter are not limited to the application of single crystal cells. Optimized processes such as CdS deposition, ZnO deposition and cell patterning process can be applied equally well to thin film cells. In addition, applications of ZnO and CdS films are not limited to the field of photovoltaics. Currently, field emission devices (FED) for flat-panel display applications are under

intense investigation in our laboratory as well as others. In a FED display panel, high quality ZnO films could be used as transparent conductor and/or phosphor. Our laboratory is also investigating the feasibility of adopting the CBD CdS films to build thin film transistor arrays for the switching circuit of liquid crystal display (LCD). The improved deposition conditions established in this work are being used by another graduate student to study electrical properties of CBD CdS films for such purposes. With further optimization, it is possible to extend the present deposition processes to prepare ZnO and CdS films with uniform properties for display applications.



Fig. 4.1. Schematic diagram showing the structure of the $ZnO/CdS/CuGa_XIn_{1-X}Se_2$ PV cells.





Fig. 4.2. SEM pictures of (a) as-polished surface and (b) Br-methanol etched surface of CuInSe₂ substrate.



Fig. 4.3. Schematic diagram of the furnace used for Ar annealing.



Fig. 4.4. Schematic diagram of the CdS deposition setup.



Fig. 4.5. Experimental setup for optical transmission measurements.



Fig. 4.6. Optical transmission plotted as a function of wavelength for a typical CdS thin film with a thickness of 50 nm.



Fig. 4.7. Schematic diagram of the rf-sputtering system used for ZnO deposition.



Fig. 4.8. Sheet resistance of ZnO films plotted as a function of chamber pressure.



Fig. 4.9. Optical transmission plotted as a function of wavelength for a typical 1.5 μ m thick ZnO thin film with a sheet resistance of 20 Ω/\Box .



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Fig. 4.10. A SEM picture showing the cross section of a ZnO/CdS/CuInSe₂ PV cell.

PHOTOVOLTAIC CHARACTERISTICS OF ZnO/CdS/CuGa_xIn_{1-x}Se₂ CELLS

5.1 Introduction

The first heterojunction single crystal CuInSe₂ PV cell was reported in 1974 by Bell Laboratories [4.70]. This cell had a CdS/CuInSe₂ structure with an evaporated CdS layer. The cell was fabricated on a polished CuInSe₂ single crystal substrate prepared by directional freezing and had a conversion efficiency of about 5 %. In 1975, the same research group reported a 12 % conversion efficiency on a small area cell (active area = 0.79 mm^2) fabricated on a cleaved (112) surface with the same structure [4.71]. With a silicon monoxide (SiO) anti-reflection (AR) coating, this cell yielded a J_{SC} of 38.0 mAcm⁻² under a solar illumination of 92 mW-cm⁻². This could be translated into a J_{SC} of 41.3 mA-cm⁻² under the normalized illumination of 100 mW-cm⁻². Such a high value of J_{SC} is equivalent to the value obtained in the highest efficiency thin film CuInSe₂ cell [4.22] and can be considered as the highest among all the CuInSe₂ cells. Before depositing the AR coating, the same cell yielded an efficiency of 10.6 %. To date, the 12 % conversion efficiency is still the best result obtained in single crystal CuInSe₂ cells.

Between 1975 and 1988, several attempts have been made to fabricate PV cells based on single crystal CuInSe₂ substrates. Various window materials such as CdS [4.67], CdIn₂S₄ [4.66], (Cd,Zn)S [4.69] and ITO [4.65] were used. In 1978, Kazmerski et al. [4.65] reported an 8.5 % ITO/CuInSe₂ cell with an active area of 0.13 cm². The cell was fabricated on a Bridgman grown substrate. Although this cell did not achieve a record high efficiency, it did give a record high V_{OC} of 0.50 V for a single crystal CuInSe₂ cell. The 10.6 % efficiency record set by Bell laboratories on single crystal CuInSe₂ cells without using AR coating remained unchallenged for eight years, until 1983, when Arya et al. [4.67] reported a single crystal CdS/CuInSe₂ cell which tied the Bell Laboratories record. This cell was fabricated on a polished Bridgman grown CuInSe₂ substrate and had a similar active area as the Bell Laboratories cell. A J_{SC} of 40 mA-cm⁻² was achieved which is the highest J_{SC} ever obtained for single crystal CuInSe₂ cells without AR coating.

After 1988, the majority of the research in single crystal CuInSe₂ PV cells was carried out at McGill University. In the late 1980's, our laboratory reported the first single crystal ZnO/CuInSe₂ cell [5.1,2]. Since then, cell structures such as CdO/CuInSe₂, CdO/CdS/CuInSe₂ and ZnO/CdS/CuInSe₂ were studied in our laboratory with various degree of success [2.9, 3.46, 4.1-5, 5.3]. To date, the best results were obtained using the ZnO/CdS/CuInSe₂ structure [2.9, 4.3-4] for cells fabricated on polished substrates. Conversion efficiencies as high as 11.5 % were achieved [2.9] without AR coating. The high efficiencies were obtained using Ar substrate annealing. The annealing improved the performance of the PV cells mainly through the enhancement of V_{OC} and FF. The best cell produced in our laboratory had an active area about five times that of the Bell Laboratories cell. Indeed, the 11.5 % cell has the highest FF among all the single crystal
CuInSe₂ PV cells and also the highest efficiency for single crystal CuInSe₂ cells without an AR coating.

The first single crystal CuGaSe₂ PV cell was reported in 1977 [4.72] which was two years after the report of the pioneer 12 % Bell Laboratories CuInSe₂ cell. This cell also utilized an evaporated CdS window layer. Although the conversion efficiency of this CdS/CuGaSe₂ cell was only 5 %, it produced a J_{SC} of 13 mA-cm⁻² under solar illumination of 71 mW-cm⁻² without AR coating. The equivalent J_{SC} under the normalized 100 mW-cm⁻² illumination was 18.3 mA-cm⁻². This high value of J_{SC} for CuGaSe₂ cells remains unchallenged today. Since the report of this cell, the research in single crystal CuGaSe₂ cells appeared to have stopped for more than 15 years, until recently, Saad et al. [4.6,7] reported improved performances by adopting the ZnO/CdS/CuGaSe₂ structure. To date, the highest efficiency reported is 9.7 % with the help of MgF₂ AR coating [4.7, 5.4]. The corresponding V_{OC} and FF reached values of 0.946 V and 66.5 %, respectively. The high efficiency in this cell was achieved by adopting post-fabrication annealing in vacuum. The 9.7 % is the highest efficiency ever obtained among all the thin film and single crystal CuGaSe₂ cells. More recently, Schon et al. [5.12] also reported the effects of post-fabrication vacuum annealing for single crystal CuGaSe₂ cells utilizing the same structure. The highest efficiency obtained by them was 7.4 % without using AR coating.

Since the reported results in single crystal CuInSe₂ and CuGaSe₂ PV cells are rather limited, one could expect the research in single crystal Cu(Ga,In)Se₂ (0 < x < 1) cells to be rare. According to the author's knowledge, there was only one paper which

reported the cell results for a single crystal Cu(Ga,In)Se₂ cell. In 1980, Romeo et al. [4.68] reported a (Cd,Zn)S/CuGa_{0.5}In_{0.5}Se₂ cell with a conversion efficiency of 7 % without AR coating and with an active area of 2 mm². It is interesting to note that all the CuGaSe₂ and Cu(Ga,In)Se₂ cells stated above were fabricated on the as-grown (112) surfaces of the crystals prepared using chemical vapor transport (CVT) technique.

Table 5.1. Summary of the most significant single crystal $CuGa_XIn_{1-X}Se_2$ PV cell results.

Reference	Substrate	Structure	Active Area (mm ²)	J _{SC} (mA-cm ⁻²)	Voc (V)	FF (%)	η (%)
[4.71]	Directional freezing, cleaved (112)	SiO/CdS/CuInSe ₂ CdS/CuInSe ₂	0.79 0.79	41.3	0.485	60.0	12.0 10.6
[4.65]	Bridgman	ITO/CuInSe ₂	13.00	30.8	0.500	55.0	8.5
[4.67]	Bridgman, polished	CdS/CuInSe ₂	0.80	40.0	0.450	59.0	10.6
[2.9] McGill	Bridgman, polished	ZnO/CdS/CuInSe ₂	4.00	33.8	0.480	71.0	11.5
[4.72]	CVT, as-grown (112)	CdS/CuGaSe ₂	2.50	18.3	0.500	55.0	5.0
[4.7, 5.4]	CVT, as-grown (112)	MgF2/ZnO/CdS/CuGaSe2	5.10	15.5	0.946	66.5	9.7
[4.68]	CVT, as-grown (112)	(Cd,Zn)S/CuGa _{0 5} In _{0 5} Se ₂	2.00	19.5	0.600	60.0	7.0

From the above survey, it is clear that only a limited amount of literature reported results on single crystal CuGa_xIn_{1-x}Se₂ PV cells. Some of the best single crystal cell results are summarized in Table 5.1. In Table 5.1, all the values of J_{SC} are normalized to an illumination level of 100 mW-cm⁻² to facilitate fair comparison. The values in bold faces represent the best parameters obtained in single crystal CuGa_xIn_{1-x}Se₂ cells so far. From Table 5.1, one can see that high performance cells could be fabricated on cleaved, polished or as-grown surfaces. In the present study, efforts are focused on the investigation of cells fabricated on polished substrates. There are some advantages for

using polished rather than cleaved or as-grown substrates from a practical point of view. Cleaved or as-grown surfaces usually have smaller area and/or are not smooth. This introduces extra difficulties in cell fabrication and reduces the reproducibility of experimental results. On the other hand, polished substrates should provide larger and smoother surfaces for cell fabrication. Furthermore, the crystal utilization rate could be much higher if polished substrates were used. This is especially important when considering the lengthy crystal growth process which results in relatively low crystal yield. Therefore, in the present case, polished substrates are used.

Although most of the single crystal CuInSe₂ cells reported were fabricated on Bridgman grown substrates, there has been no previous report on CuGaSe₂ and Cu(Ga,In)Se₂ PV cells fabricated using Bridgman grown substrates. Indeed, this is also the first investigation on single crystal Cu(Ga,In)Se₂ PV cells using the ZnO/CdS/Cu(Ga,In)Se₂ structure. Furthermore, the effect of Ar substrate annealing on Ga containing cells is still not known. In this chapter, the photovoltaic characteristics of the ZnO/CdS/CuGa_xIn_{1-x}Se₂ cells fabricated on Bridgman grown substrates are presented. Particular attention is drawn to the study of the effect of Ar annealing on photovoltaic performance. In section 5.2, the procedure to determine the illuminated current-voltage characteristics is first described. Then the effects of Ar substrate annealing on cell performance for cells with different Ga content are presented in section 5.3. The short circuit currents of several cells were also measured in the CANMET/EDRL under the AM 1.5G spectrum. The corresponding results will be discussed in section 5.4. In section 5.5, the spectral response of the cells with different Ga content is presented. To understand the difference between CdS/CuInSe₂ and CdS/CuGaSe₂ interfaces, the effects of post-fabrication annealing on photovoltaic performance are studied in section 5.6. Finally, conclusions of this chapter are drawn in section 5.7.

5.2 Measurement of Illuminated Current-Voltage Characteristics

Previously, both indoor and outdoor measurements were used in our laboratory to determine illuminated current-voltage (I-V) characteristics of CuInSe₂ PV cells [2.9, 3.46, 4.26]. In the case of outdoor measurements, the conditions of sunlight could change dramatically depending on time and weather conditions. Factors such as temperature and intensity as well as direction of sunlight and scattered light could all vary. Therefore, it is not adequate for routine measurements in comparing cell performances. However, outdoor testing is essential in evaluating the performance of large area PV modules. In contrast, standardized measurement conditions could be consistently reproduced under a laboratory environment. Therefore, indoor measurement using simulated solar light seems to be the logical choice for small area laboratory cells.

In our laboratory, two different light sources have been used to simulate solar lights, a tungsten lamp [2.9, 4.26] and a Kratos xenon arc solar simulator [3.46]. Both sources were found to give satisfactory results. In this work, a two step method was implemented to obtain the illuminated I-V characteristics. The first step was to obtain the short circuit current of each cell using either a Kratos LH 150/1 simulator in our laboratory or a Darentek UCT1000 xenon arc simulator in the Energy Diversification

Research Laboratory (CANMET/EDRL), Varennes, Quebec. The measured short circuit current was then used to obtain detailed I-V characteristics under a stable tungsten light source using automatic sampling. Such a two step measurement process is described below.

Simulator	Simulated Spectrum	Number of Filters	ASTM Compliance	Area with Uniform Illumination	Reference Cell Calibration	Reference Cell Uncertainty
Kratos	AM 1	1	No	$< 1 \text{ cm}^2$	Not known	Not known
Darentek	AM 1.5G	3	Class B	$\sim 80 \text{ cm}^2$	NREL	± 2 %

Table 5.2 Specifications of Kratos and Darentek sim	nulators.
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Before discussing the measurement method, it is important to understand the properties of the two solar simulators and the corresponding reference cells. Table 5.2 summarizes the different characteristics of the two simulators and reference cells. The Kratos simulator is equipped with a single filter to simulate the AM 1 spectrum while the Darentek simulator utilizes a triple filter system to simulate the AM 1.5G spectrum. The AM 1.5G spectrum is the standard spectrum adopted by most of the laboratories to evaluate PV cell performance. The Darentek simulator complies with the ASTM solar simulator class A specification for wavelengths less than 0.9 μ m and class B specification for wavelengths greater than 0.9 μ m. Generally speaking, such a simulator is classified as a class B simulator according to ASTM designation [5.7]. On the other hand, the Kratos simulator does not comply to any ASTM specification. Furthermore, a 2 x 2 cm² Si cell recently calibrated by NREL under the ASTM E 892 Global (AM 1.5G) spectrum [5.8] is used as the reference for the Darentek simulator. The error margin of such a reference cell

as stated by NREL is ± 2 %. The calibration for the reference cell used in our laboratory with the Kratos simulator is uncertain. By considering all of the above factors, it is believed that the Darentek simulator would produce more reliable results. Though, the Kratos simulator was used for routine measurements due to the easy accessibility, the Darentek simulator was used to obtain more reliable results for high performance cells.

The first step in illuminated I-V measurement was to obtain short circuit current. Fig. 5.1 shows a schematic diagram of solar simulator and the measurement circuit in determining short circuit currents. The solar simulator (either the Kratos or the Darentek) was first adjusted to the desired light intensity (usually 100 mW-cm⁻²) by referring to a reference cell. I_{SC} of the PV cell was then measured by shunting the cell with a high precision 1.00 Ω resistor and the voltage across the shunt resistor was obtained using either a HP 3478A or a Keithley 177 multimeter. The resistance value of the shunt resistor was used, the value of short circuit current could be read directly from the voltage reading of the multimeter.

In the present case, the active areas of all the PV cells are less than 5 mm². Hence, the maximum short circuit current for each PV cell would not exceed 2 mA regardless of Ga content when considering a maximum bound on J_{SC} to be around 40 mA-cm⁻². By shunting the cell with an 1 Ω resistor, the maximum possible operating voltage of the PV cell (which is equivalent to the voltage drop across the 1 Ω resistor) would not exceed 2 mV. Hence, the error in short circuit current measurements caused by biasing is negligible for such a small operating voltage.

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Once the value of I_{SC} was known, the PV cell was illuminated under a stable tungsten light source. The intensity of the illumination was adjusted such that the value of I_{SC} was reproduced to within a ±0.5 % margin. The illuminated I-V characteristics could then be obtained using a HP 4145A semiconductor parameter analyzer. The parameter analyzer is capable of sampling the complete I-V curve automatically in less than 3 seconds. Such a short sampling time is beneficial in obtaining reliable I-V characteristics by reducing the effects of temporal fluctuations in light intensity and temperature. No external biasing was needed. I-V characteristics were measured for biasing voltage from -1 to +1 V with steps of 0.025 V. During the measurements, special care was taken to prevent excessive heating of the PV cells. In all the cases, the measurements were carried out at a temperature of 25 ± 3 °C.

When using the Darentek simulator to evaluate the cell performance, an uncertainty of ± 10 % was estimated. This figure was obtained by taking into account the sources of errors such as uncertainty in active cell area (~ 2.5 %), temporal instability of irradiance (~ 2.5 %), uncertainties in reference cell reading (~ 2 %) and tungsten lamp intensity (~ 0.5 %), plus other errors such as temperature effect and difference in spectral content. Considerably higher error could be resulted when the in-house Kratos simulator was used. This was mainly because of the uncertain spectral distribution caused by the less sophisticated filtering system and the uncertain calibration for the reference cell used in our laboratory. However, the additional errors were most likely to appear in the determination of short circuit current. The measurement of open circuit voltage and fill factor should give insignificant additional errors.

5.3 Effects of Ar Substrate Annealing

In this section, the effects of Ar annealing on photovoltaic performance for cells with different Ga content are discussed. The cells were fabricated using the optimized fabrication procedures described in chapter 4, without using AR coating. Six groups of PV cells with different Ga contents ($x \approx 0, 0.15, 0.30, 0.45, 0.75, 1$) were fabricated. For each composition, six cells were prepared. Three of the cells were fabricated with Ar annealed substrates and the other three cells were fabricated on un-annealed samples. In each composition, the best results from cells fabricated on annealed and un-annealed substrates are shown in Table 5.3. All the short circuit currents were determined using the in-house Kratos AM 1 solar simulator under an illumination of 100 mW-cm⁻². The measurements were made within one month of cell fabrication. The current densities were calculated by dividing the measured currents with corresponding active cell areas. The efficiency of the PV cells were found to range from 2.6 % to 9.9 %. Two major observations could be seen from the data presented in Table 5.3.

Sample No.	Ga Content (x)	Ar Annealing	Active Area	J _{SC} (mA-cm ⁻²)	V _{oc} (V)	FF (%)	η (%)
A-1	0.00	No	S	21.6	0.325	55.6	3.9
A-2	0.00	Yes	L	27.6	0.502	71.1	9.9
A-3	0.15	No	L	16.6	0.388	60.1	3.9
A-4	0.15	Yes	S	20.3	0.416	65.5	5.5
B-1	0.30	No	S	21.8	0.490	57.2	6.1
B-3	0.30	Yes	L	17.0	0.491	65.3	5.4
C-2	0.45	No	S	20.6	0.598	61.1	7.5
C-3	0.45	Yes	S	19.1	0.647	66.1	8.1
D-1	0.75	No	S	11.7	0.507	52.8	3.1
D-4	0.75	Yes	L	14.4	0.641	55.8	5.2
E-3	1.00	No	S	10.7	0.518	46.2	2.6
E-4	1.00	Yes	L	10.2	0.529	60.8	3.3

 Table 5.3.
 Summary showing the effects of Ar substrate annealing.

 $S - 1.86 \text{ mm}^2$, L - 4.89 mm²

First, cells fabricated on Ar annealed substrates consistently produced higher FFand V_{OC} under the same measuring condition regardless of the Ga content. Increase in conversion efficiency was found in almost all the cases. This result suggests that the benefits of Ar annealing are not only limited to CuInSe₂ cells, but also extends to Ga containing cells. Since a similar Ar annealing was also found to improve the performance of thin film CuInSe₂ cells in our laboratory [4.26], it is quite possible that the improvement could be extended to thin film Cu(Ga,In)Se₂ and CuGaSe₂ cells.

Second, although V_{OC} as high as 0.647 V was obtained in a CuGa_{0.45}In_{0.55}Se₂ cell, the value of V_{OC} for higher Ga content cells did not show further improvement as predicted by the theory. In this study, since all the PV cells were fabricated using the same process regardless of Ga content, the fabrication process was not specifically tailored to use in high Ga content cells. Indeed, the present PV cells were prepared using the method optimized for CuInSe₂ cells. The same crystal growth process and/or substrate preparation might not be optimized for the whole range of Ga content. Furthermore, the CdS deposition process could also play an important role in determining the PV cell performance. According to the latest results on thin film ZnO/CdS/CuGaSe₂ cells [5.5-6.9], major modification to the CdS deposition process, such as bath composition and bath temperature, used in the low Ga content cells has to be made to obtain high V_{OC} on CuGaSe₂ cells. In particular, an increase in deposition temperature from 60 °C to 80 °C [5.5,9] was found to be crucial. Furthermore, in the case of the best single crystal CuGaSe₂ cell [4.7], the CdS deposition temperature was around 75 °C instead of 60 °C used in this work. Therefore, it is not surprising that optimum results are not obtained over the whole range of Ga content in the present case.

In addition to the above two major observations, it is also worthwhile to point out that V_{OC} and FF as high as 0.502 V and 71.1 % were produced in a single crystal CuInSe₂ cell using the current cell fabrication conditions. Since the highest V_{OC} previously reported by our laboratory was 0.480 V, the present result represents a 5 % improvement. The values of V_{OC} and FF were only 3 % and 2 % lower than the corresponding values for the most efficient (Eff. ~ 15 %) thin film CuInSe₂ cell [4.22]. Indeed, these values could also be considered as the highest among single crystal CuInSe₂ cells. The enhancement in V_{OC} could be attributed to the improved CdS deposition process. Furthermore, an efficiency of 8.1 % was obtained in a single crystal CuGa_{0.45}In_{0.55}Se₂ cell. This result reflects an improvement of 16 % over the 18 year old record of 7.0 % conversion efficiency obtained in a single crystal CuGa_{0.50}In_{0.50}Se₂ cell [4.68]. The present cell has a comparable J_{SC} to the previously reported one. However, the improvement in V_{OC} and FF were 8 % and 10 %, respectively. Indeed, the V_{OC} attained in this work was comparable with other high efficiency thin film cells with similar Ga content [4.23,38-39].

5.4 PV Characteristics Under AM 1.5G Conditions

To obtain the PV performance under the more commonly adopted AM 1.5G conditions, short circuit currents for three of the best cells were also determined using the Darentek simulator. The three cells were samples A-2 (CuInSe₂), C-3 (CuGa_{0.45}In_{0.55}Se₂) and E-4 (CuGaSe₂). The measurements were done 1 1/2 month after the initial in-house measurements using the Kratos simulator. In Table 5.4, the results obtained using the Kratos simulator were compared to that of the Darentek simulator. The I-V characteristics were obtained under an equivalent illumination of 100 mW-cm⁻².

Sample No.	Ga Content (x)	Ar Annealing	Active Area	J _{SC} (mA-cm ⁻²)	V _{oc} (V)	FF (%)	η (%)
A-2 ^K	0.00	Yes	L	27.6	0.502	71.1	9.9
A-2 ^D	0.00	Yes	L	29.3	0.502	70.2	10.3
C-3 ^K	0.45	Yes	S	19.1	0.647	66.1	8.1
C-3 ^D	0.45	Yes	S	24.1	0.640	65.6	10.1
E-4 ^K	1.00	Yes	L	10.2	0.529	60.8	3.3
E-4 ^D	1.00	Yes	L	16.0	0.511	57.7	4.7

Table 5.4. Comparison between results obtained from Kratos and Darentek simulators.

K - Kratos AM 1, D - Darentek AM 1.5G, S - 1.86 mm², L - 4.89 mm²

Slight degradation in V_{OC} and/or *FF* was found after 1 1/2 month from the initial measurements. However, the degradation was found to be less than 5 % in all cases. No change in V_{OC} was observed in the CuInSe₂ cell (sample A-2). From the measurement result, it was found that the in-house Kratos simulator consistently produce lower short circuit currents in all the three cells. The differences were 6 % in CuInSe₂ cell, 21 % in CuGa_{0.45}In_{0.55}Se₂ cell and 36 % in CuGaSe₂ cell. The 6 % difference in CuInSe₂ cell is relatively small and falls within the estimated margin of error. However, the 21 % and 36 % differences for CuGa_{0.45}In_{0.55}Se₂ and CuGaSe₂ cells could not be explained by experimental errors. Since the magnitude of discrepancy appeared to rise as the bandgap of absorber was increased, the differences were most likely to be the result of different spectral distribution between the Kratos and Darentek simulators. While the Darentek simulator complies with the ASTM specification with a more sophisticated filtering system, the specification for the in-house Kratos simulator is uncertain. It is therefore believed that the Darentek simulator produces more reliable results. Despite the

discrepancies, the current results also confirmed that the in-house Kratos simulator is capable of producing reasonable results when $CuInSe_2$ cells are tested. However, when cells with higher bandgaps are tested using the Kratos simulator, caution should be taken in interpreting the short circuit currents.

The illuminated J-V characteristics for all the three cells are shown in Fig. 5.2. The maximum power points are also indicated. Both the CuInSe₂ and CuGa_{0.45}In_{0.55}Se₂ cells exceed 10 % conversion efficiency. In particular, the CuInSe₂ cell achieved a record high V_{OC} of 0.502 V and had a FF exceeding 70 %. Furthermore, the CuGa_{0.45}In_{0.55}Se₂ cell attained an efficiency of 10.1 % which represents a significant improvement of 44 % over the previous single crystal record of 7.0 % efficiency for cells containing Ga. Despite the slight degradation in V_{OC} and FF, this cell still demonstrated higher values over the previously reported single crystal CuGa_{0.50}In_{0.50}Se₂ cell in each of the J_{SC} , V_{OC} and FF. Moreover, the J_{SC} of the present CuGaSe₂ cell reached a value of 16.0 mA-cm⁻² even without AR coating. This is an encouraging result since it is higher than that of the highest efficiency single crystal ZnO/CdS/CuGaSe₂ cell ($J_{SC} = 15.5 \text{ mA-cm}^{-2}$) reported in [4.7]. The J_{SC} of 15.5 mA-cm⁻² in that cell was achieved using MgF₂ AR coating. If the effect of AR coating is taken into consideration, the J_{SC} obtained in the present case would be about 10 % higher. The J_{SC} of 16.0 mA-cm⁻² obtained in this work is also equivalent to that of the best thin film CuGaSe₂ cell ($J_{SC} = 16.0 \text{ mA-cm}^{-2}$) [5.6].

In addition, the short circuit current densities for all of the three cells only reached about 65 % of the theoretical maximum values. Without the AR coating, the highly reflective surface obtained from fine alumina polishing should at least be partially responsible for this. Furthermore, the value of J_{SC} was found to decrease from 29.3 to 16.0 mA-cm⁻² as the absorber bandgap was increased from 1 eV (CuInSe₂) to 1.65 eV (CuGaSe₂). This reduction in J_{SC} is believed to be the result of reduced photon absorption due to the shift in absorption edge for cells with different absorber bandgap. The details in spectral response will be discussed in the next section.

5.5 Spectral Response

To further understand the characteristics of the PV cells, spectral response measurements for wavelengths from 0.4 μ m to 1.1 μ m were made in cells with different Ga content. More than ten cells fabricated on Ar annealed and un-annealed substrates were measured. The measurements were done using the same spectrophotometer, lock-in amplifier and light chopper (136 Hz) described in section 4.3. The photo-current of the PV cell under the illumination of chopped monochromatic light was converted into a voltage signal using a 50 Ω shunt resistor. The voltage signal was then measured using the lock-in amplifier. The intensity of the monochromatic light was determined using a calibrated Si detector (United Detector model PIN 6DP). The spectral response $SR(\lambda)$, as a function of wavelength, was calculated as the following:

$$SR(\lambda) = \frac{I_P}{Pq} \frac{hc}{\lambda}$$
(5.1)

where I_P is the photo-current, P is the incident optical power, q is electron charge and hc/λ is the photon energy.

The maximum values of absolute spectral response were found to vary between 45 % and 75 % from cell to cell. The substrate annealing was not found to affect the spectral response significantly. In Fig. 5.3, the normalized spectral response for five typical cells with different Ga content (x $\approx 0, 0.15, 0.45, 0.75, 1$) are plotted. For each spectral response curve, two cutoff edges could be observed. The first one occurs in the ultra-violet region below 0.5 µm. This short wavelength cutoff is the result of the absorption of high energy photons by the ZnO/CdS window structure. The other absorption edge occurs at longer wavelength region depending on the bandgap of absorber. In this particular case, the energy gap of the absorber ranged from about 1 eV (x = 0) to 1.65 eV (x = 1) depending on Ga content. Hence, the theoretical absorption edge should shift from about 1.24 µm to 0.75 µm as the Ga content was increased from x = 0 to x = 1. Thus, the result shown in Fig. 5.3 showed reasonably good agreement with bandgap variation. Moreover, as the long wavelength cutoff is shifted towards shorter wavelengths due to increasing absorber bandgap, the short circuit current for the PV cell should also decrease due to the reduced photon absorption. This phenomena was reflected in the results shown in the previous section.

Furthermore, the maximum values of the absolute spectral response for the three cells, samples A-2, C-3 and E-4, were all found to be around 70 %. In the previous section, it was found that the short circuit current densities for these three cells reached about 65 % of the theoretical maximum values using the Darentek simulator. Therefore, the present spectral response results appear to support the results obtained by the Darentek simulator. The smaller values of J_{SC} obtained using the Kratos simulator simply

could not have matched the 70 % maximum spectral response obtained in the present case.

5.6 Effect of Post-fabrication Annealing

To help clarify the interface properties of the PV cells, post-fabrication annealing was carried out. From the results presented in sections 5.3 and 5.4, it is clear that the quality of the heterojunctions are quite different for CdS/CuInSe₂ and CdS/CuGaSe₂ interfaces. Through the study of low temperature post-fabrication annealing, the difference in properties for these two kinds of interfaces could be better understood. Previously, the effects of post-fabrication annealing on PV performance have been studied by various authors. Most of the investigations were concentrated on thin film cells. Various annealing environments such as air [4.17,22,91, 5.5,9-11], argon [4.17] and vacuum [4.6-7, 5.12] have been reported with mixed results. Usually, the annealing temperature was below 250 °C and the annealing time was limited to 30 minutes, although annealing time in the order of hours was also reported [5.12]. In this work, annealing experiments were carried out in air using a Blue M oven, the temperature of the oven was monitored using a thermometer. The annealing temperature was set to about 175 °C and illuminated I-V characteristics were obtained after 3, 6, and 9 minutes of annealing. The two cells studied were fabricated on Ar annealed substrates.

In Fig. 5.4, two illuminated J-V characteristics (as-fabricated and after 3 minutes of annealing) of a ZnO/CdS/CuInSe₂ cell are shown. For this cell, deterioration was observed after 3 minutes of annealing. Reduction in all of the J_{SC} , V_{OC} and FF was found.

Further annealing led to the disappearance of PV effect. This result confirms the importance of limiting the cell processing temperature to below 100 $^{\circ}$ C in all fabrication steps. The low processing temperature could eliminate the uncontrollable annealing effects. Indeed, the latest experimental results suggested the interdiffusion between CdS and CuInSe₂ started at a temperature as low as 120 $^{\circ}$ C [6.4].

On the other hand, the results of a ZnO/CdS/CuGaSe₂ cell showed opposite behaviors. The corresponding I-V characteristics are shown in Fig. 5.5. As can be seen, after 3 minutes of annealing, the *FF* of the cell slightly increased. Further annealing led to significant improvements in V_{OC} . The V_{OC} of the cell was increased from 0.500 to 0.625 V after a total of 9 minutes annealing. This notable enhancement in V_{OC} was also reported in air annealed thin film [5.5,9] and vacuum annealed single crystal ZnO/CdS/CuGaSe₂ cells [4.6-7, 5.12] fabricated in other laboratories.

Since the window layers for these two cells were deposited under the identical conditions, the large discrepancy in post-fabrication annealing behaviors could not be explained by the change at the ZnO/CdS interface. The large difference in cell behavior was believed to be the result of different thermal properties at the CdS/CuInSe₂ and CdS/CuGaSe₂ interfaces. The results obtained in this section compliment the observations found in section 5.3 that the same cell fabrication process yielded interfaces with different qualities in cells with different Ga content. Furthermore, the present results also indicated the feasibility of applying the post-fabrication air annealing routinely to CuGaSe₂ and probably even high Ga content Cu(Ga,In)Se₂ cells for performance enhancement.

5.7 Conclusions

In this chapter, the illuminated I-V characteristics for cells with different Ga content were discussed. In the initial part, a literature survey was given on the development of single crystal CuGa_XIn_{1-X}Se₂ cells in the past two decades. Following that, the two step measuring procedures for the determination of cell performances were discussed in detail. The margin of error for the conversion efficiency determination was also estimated by taking into account various experimental parameters. The effects of Ar substrate annealing were then investigated on cells with various Ga content. By analyzing PV performances, it is believed that Ar annealing is beneficial not only to CuInSe₂ cells but also Ga containing cells. However, to optimize performance, the same fabrication condition should not be used in cells with different composition, especially those with high Ga content. Illuminated I-V measurements in some of the best cells (a CuInSe2 and a CuGa_{0.45}In_{0.55}Se₂ cell) revealed conversion efficiencies exceeding 10 %. In particular, a V_{OC} of 0.502 V and a FF exceeding 70 % were obtained in the CuInSe₂ cell. A record high efficiency of 10.1 % was achieved in the CuGa045In0.55Se2 cell. This represents a notable improvement over the previous record of 7 % on cells fabricated on Cu(Ga,In)Se₂ mixed crystals. The high performance obtained in this work could be attributed to the improved CdS film deposition. By adopting several enhancements in CdS deposition as stated in chapter 4, CuInSe₂ and Cu(Ga,In)Se₂ cells with V_{OC} values comparable to that of high efficiency thin film cells should be possible. In the case of CuGaSe₂ cells, a high short circuit current density of 16.0 mA-cm⁻² was achieved. This value is either higher than or equivalent to that of the best single crystal and thin film cells. Furthermore, results

of spectral response measurements showed the shift of long wavelength cutoffs corresponding to the bandgap variation for cells with different Ga content. Finally, the study of post-fabrication air annealing revealed two distinct types of interfaces between CdS/CuInSe₂ and CdS/CuGaSe₂. While the CuInSe₂ cell degraded significantly after a short air annealing, the behavior of the CuGaSe₂ was opposite. Improvements in *FF* and/or V_{OC} were observed for an annealing time three times that of the CuInSe₂ cell. With further optimization, post-fabrication air annealing could become a routine procedure in optimizing the performance of CuGaSe₂ and probably Cu(Ga,In)Se₂ cells of high Ga content.



Fig. 5.1. Schematic diagram of solar simulator and measurement circuit of short circuit currents.



Fig. 5.2. Illuminated J-V characteristics of cells A-2 (CuInSe₂), C-3 (CuGa_{0.45}In_{0.55}Se₂) and E-4 (CuGaSe₂) under AM 1.5G condition.



Fig. 5.3. Normalized spectral response for cells with various Ga contents.



Fig. 5.4. Effect of post-fabrication air annealing on illuminated J-V characteristics of a ZnO/CdS/CuInSe₂ cell.



Fig. 5.5. Effect of post-fabrication air annealing on illuminated J-V characteristics of a ZnO/CdS/CuGaSe₂ cell.

ENERGY BAND DIAGRAM AND CURRENT TRANSPORT OF ZnO/CdS/CuGa_xIn_{1-x}Se₂ PV CELLS

6.1 Introduction

In the previous chapter, the illuminated current-voltage characteristics were discussed. However, no discussion of the energy band diagram and the current transport mechanism has been given yet. In this chapter, efforts will be directed to address the above two issues. Before the construction of the energy band diagram in any heterojunction is possible, the understanding of band lineup is mandatory. Up to now, only a limited amount of experimental work has been directed to determine such band lineup in ZnO/CdS/CuGa_xIn_{1-x}Se₂ cells with various Ga content. In this work, based on the better understood model of ZnO/CdS/CuInSe₂, the band lineup for cells with different Ga content is calculated by considering variation in electron affinity and energy gap. The corresponding discussion is presented in section 6.2. Following that, the energy band diagram and hence the charge distributions could then be determined (see section 6.3). A crucial parameter in any energy band diagram of a heterojunction is the built-in potential. To establish the energy band diagrams, values of built-in potential are computed for cells with various Ga content and carrier concentration (section 6.4). In addition to the energy band diagram, lattice mismatch is also an important factor in understanding current

transport. A discussion on the lattice mismatch in ZnO/CdS/CuGa_XIn_{1-X}Se₂ cells is given in section 6.5.

Following the analysis of energy band diagrams and lattice mismatch, the current transport mechanisms will be discussed in section 6.6. First of all, reverse J-V characteristics are analyzed. Then an explanation is presented to discuss alternate tunneling paths for the forward diode currents based on energy band diagram and lattice mismatch data. Since very little analysis work has been done before on the current transport under illumination in single crystal CuGa_xIn_{1-x}Se₂ cells, an analysis is performed in this work to study the effect of illumination on current transport. The results obtained are presented in section 6.7. Finally, conclusions of this chapter are drawn in section 6.8.

6.2 Band Lineup in ZnO/CdS/CuGa_XIn_{1-X}Se₂ PV Cells

Before an energy band diagram can be constructed, it is essential to understand the band lineup. Since a three layer structure is used in the construction of PV cells, two interfaces (ZnO/CdS and CdS/CuGa_xIn_{1-x}Se₂) are formed. Little work has been done on the ZnO/CdS interface, so far. In fact, only one study was directed to resolve the band lineup in such an interface. Using photoelectron spectroscopy, Ruckh and co-workers (1994) [6.9-10] investigated the band lineup between rf-sputtered ZnO film and vacuum deposited CdS film. Their results indicated a valence band offset (ΔE_V) of 1.2 eV. If the bandgaps of ZnO and CdS are taken as 3.3 eV [6.12-13] and 2.4 eV [4.57,59],

respectively, the corresponding conduction band offset (ΔE_C) is equal to 0.3 eV. Fig. 6.1 shows the band lineup for ZnO/CdS interface. Also shown in the same diagram is the band lineup for CdS/CuInSe₂ interface, which will be discussed below.

In the case of CdS/CuGa_xIn_{1-x}Se₂ interface, more studies have been carried out to investigate the band lineup. However, the majority of the research work was concentrated on the CdS/CuInSe₂ interface. From the latest results of direct measurements (1990-98) on CdS/CuInSe₂ heterojunctions using photoelectron spectroscopy, the value of ΔE_{V} was found to be less than 1.4 eV [6.3-7]. If bandgaps of CdS and CuInSe₂ are taken as 2.4 eV and 1.0 eV [3.37,39,42-44, 6.11], respectively, the conduction band edge of p-CuInSe₂ is then below that of n-CdS. Thus, a conduction band spike is expected to form in the energy band diagram of the CdS/CuInSe₂ junction.

Table 6.1. Summary of reported ΔE_V and junction preparation conditions.

Reference	CdS Preparation	CuInSe ₂ Preparation	ΔEv (eV)
Nelson et al. [6.3]	Vacuum Deposition	Polished and Etched Crystal	0.3
Loher et al. [6.4-5]	Vacuum Deposition	UHV Cleaved (011) Crystal	0.8
Niles et al. [6.6]	CBD	Cleaved Crystal	1.0
Niles et al. [6.6]	CBD	Vacuum Deposited Thin Film	1.1
Okano et al. [6.7]	CBD	Selenized Thin Film	0.4

The value of ΔE_V between CdS and CuInSe₂ was reported to range from 0.3 to 1.1 eV. Table 6.1 summarizes the published values of ΔE_V and the corresponding junction preparation conditions. It can be seen from Table 6.1 that all these results were obtained from junctions with different preparation conditions. This could explain the large range of

values obtained. Among all the preparation conditions, the condition reported by Nile et al. (NREL) [6.6] is closest to the one used in this work. They deposited the CdS film onto a cleaved CuInSe₂ substrate using CBD method. Other single crystal work involved vacuum deposited CdS [6.3-5]. It has been established in our laboratory [2.9] as well as other [6.14] that vacuum deposition of CdS on a single crystal CuInSe₂ substrate led to the formation of a buried homojunction. This is probably the result of elemental interdiffusion. Thus, the accuracy of measurements in such junctions could be rather limited. On the other hand, our laboratory confirmed that no buried homojunction was formed between CBD CdS and single crystal CuInSe₂ [2.9]. In such a case, the junction could be considered as a true heterojunction. Hence, more reliable results should be obtained using CBD rather than vacuum deposited CdS. The results obtained between CBD CdS and thin film CuInSe₂ differ considerably from the single crystal values, and are not selected in the present case. This is because the surface and bulk properties of the thin film CuInSe₂ could be very different from that of single crystal due to various deposition and treatment conditions. Therefore, in this work, a ΔE_{V} value of 1.0 eV obtained between CBD CdS and single crystal CuInSe₂ is chosen to construct the band lineup. Indeed, this value is very close to the one predicted by the latest (1993) theoretical calculation in a separate NREL study [6.8].

By using $\Delta E_{\nu} = 1.0$ eV and taking into account the optical bandgaps of CdS and CuInSe₂, the value of ΔE_C is found to be 0.4 eV. If we combine the band lineups for both the ZnO/CdS and CdS/CuInSe₂ interfaces, a complete band lineup model for ZnO/CdS/CuInSe₂ could be constructed. The corresponding diagram is shown

schematically in Fig. 6.1. Since electron affinity is a measure of conduction band edge energy level with respect to vacuum level, the electron affinities of CBD CdS and rfsputtered ZnO films could be estimated if the value of CuInSe₂ is used as reference. According to the published data, the electron affinity (χ) of CuInSe₂ varies between 4.2 and 4.7 eV [6.4,16-17,22,51,53]. By taking the latest (1996) experimentally obtained electron affinity of 4.6 eV [6.16] for CuInSe₂, values of 4.2 eV and 4.5 eV are obtained for CBD CdS and rf-sputtered ZnO, respectively. The corresponding electron affinities are also shown in Fig. 6.1. The deduced values for CdS and ZnO are found to agree with published data within a ±0.3 eV margin [6.17-18,22,53]. Thus, the present band lineup model shows reasonable agreements with the electron affinity data.

In the early studies (1984-85) carried out by Turowski et al. [6.1-2], using Si and Ge as reference materials, ΔE_V between CdS and CuInSe₂ was determined indirectly by comparing the band lineup results of X/CdS and X/CuInSe₂ (X = Si, Ge) heterostructures using photoelectron spectroscopy. The results indicated $\Delta E_V \ge 1.4$ eV at the CdS/CuInSe₂ interface and suggested that the conduction band edge of p-CuInSe₂ was above that of n-CdS. In such a case, no conduction band spike was expected. Clearly, these results were not consistent with all the latest results obtained by direct measurements using CdS/CuInSe₂ heterojunctions. Since these results were not obtained using the actual CdS/CuInSe₂ junctions, the validity of the absolute value is questionable. Therefore, in this work, only the latest results from direct measurements are considered.

In the case of CdS/Cu(Ga,In)Se₂ interface, only one attempt has been made (in 1995) to investigate a CdS/CuGa_{0.09}In_{0.91}Se₂ junction formed between CBD CdS and thin

film CuGa_{0.09}In_{0.91}Se₂. Instead of finding the valence band offset (ΔE_{ν}), Kronik et al. [6.15] obtained the conduction band offset (ΔE_C) by monitoring the change in surface work function. Their result showed a ΔE_C of -0.1 eV. Hence, the conduction band edge of CuGa_{0.09}In_{0.91}Se₂ was found to be above that of CdS. However, in their work, several estimations had to be made before the final result could be computed. The uncertainties in those estimations could limit the accuracy. Therefore, by taking into account the fact that thin film Cu(Ga,In)Se₂ instead of single crystal was used and there is no other supporting publication, this result is not adopted in building the band lineup model in the present work.

For the CdS/CuGaSe₂ interface, no direct measurement result is available. However, in the early study carried out by Turowski et al. [6.2] in 1985, a Ge/CuGaSe₂ heterojunction was also studied using photoelectron spectroscopy. If a similar comparison is done with the results obtained in Ge/CdS heterojunctions as in the case of CuInSe₂, a value of 1.1 eV is deduced for ΔE_V at the CdS/CuGaSe₂ interface. If the bandgaps of CdS and CuGaSe₂ are taken as 2.4 and 1.65 eV [3.37,39,42-44, 6.11], respectively, a conduction band offset (ΔE_C) of -0.35 eV is found. In this case, the conduction band edge of CuGaSe₂ is above that of CdS, therefore no conduction band spike is anticipated. Nonetheless, since this result was not obtained using the actual CdS/CuGaSe₂ junction, caution should be taken in adopting this result to build the band lineup model. Despite the doubt in the validity of the absolute value, if this result is compared to the result obtained in CdS/CuInSe₂ interface from the same study, the outcome suggests that the valence band edge of $CuGaSe_2$ is below that of $CuInSe_2$ and the conduction band edge of $CuGaSe_2$ is above that of $CuInSe_2$.

Up to now, it seems that a reliable band lineup model can only be built for $CuInSe_2$ cells. Since no reliable experimental data are available for the construction of band lineups in Ga containing junctions, theoretical calculation has to be made. First. to understand the behavior of conduction band offset, the electron affinity of $CuGa_XIn_{1-X}Se_2$ has to be considered. An early report indicated that electron affinity of $CuGa_XIn_{1-X}Se_2$ was reduced by 0.4 eV as x increased from 0 (i.e. $CuInSe_2$) to 1 (i.e. $CuGaSe_2$) [6.17]. Such a reduction in electron affinity was supported by results of single crystal Ni/p-CuInSe₂ and Ni/p-CuGaSe₂ Schottky junctions [6.55]. By analyzing the barrier heights of the two devices, a smaller electron affinity for CuGaSe₂ was obtained.

A reduction in electron affinity is equivalent to an up-shift of the conduction band edge in the band lineup model. In previous paragraphs, the value of ΔE_C between CdS and CuInSe₂ (x = 0) was found to be about 0.4 eV. Hence, as x increases from 0 to 1, the conduction band offset between CdS and CuGaSe₂ (x = 1) would vanish due to the 0.4 eV up-shift of conduction band edge. In this work, to calculate the variation of ΔE_C , the electron affinity of CuGa_xIn_{1-x}Se₂ is assumed to vary linearly with Ga content (x). As a result, ΔE_C could be represented by the following linear equation:

$$\Delta E_C(x) = 0.4 - 0.4x \quad \text{eV} \quad . \tag{6.1}$$

To understand the behavior of valence band offset between CdS and CuGa_XIn₁. _xSe₂, the optical bandgap of CuGa_XIn_{1-x}Se₂ has to be examined. According to single crystal results, the optical bandgap of CuGa_XIn_{1-x}Se₂ was found to vary between 1 eV and 1.65 eV depending on Ga content. Most of the research groups suggested some sort of non-linear quadratic relationship [3.37,39,42,44, 6.11] although linear dependence on Ga content was also reported [3.43]. Fig. 6.2 summarizes the bandgap results as a function of Ga content (x). In the figure, the dashed lines indicate the boundaries where the bandgap data have been reported [3.37,39,42-44, 6.11], the solid line represents the average of the reported results. In the present work, the equation of the average bandgap is found to be the following:

$$E_G(x) = 0.133x^2 + 0.505x + 1.005 \quad \text{eV}.$$
(6.2)

Although this equation is deduced from single crystal data, it is found to be in good agreement with bandgap results reported on $CuGa_XIn_{1-X}Se_2$ thin films [3.84, 6.46-47] with a worst case difference of ±4 %.

Using Eqs. 6.1 and 6.2, the variation in valence band offset (ΔE_{ν}) between CdS and CuGa_XIn_{1-X}Se₂ could then be deduced by the following relationship:

$$\Delta E_{\nu}(x) = 2.4 - \Delta E_C(x) - E_G(x) \qquad \text{eV}. \tag{6.3}$$

As a result, $\Delta E_{V}(x)$ varies according to the following equation.

$$\Delta E_{\nu}(x) = 0.995 - 0.105x - 0.133x^2 \quad \text{eV}$$
(6.4)

In Fig. 6.3, both the conduction band and valence band offsets are plotted as a function of Ga content (x). It is clear that both band offsets decrease as the Ga content is increased. The conduction band offset (ΔE_C) decreases from 0.4 eV to 0 eV and the valence band offset (ΔE_V) reduces from 1 eV to about 0.75 eV as Ga content (x) is increased from 0 to 1. Fig. 6.4 shows the complete band lineups for ZnO/CdS/CuInSe₂ (x = 0) and ZnO/CdS/CuGaSe₂ (x = 1) cells in the same energy scale. From Fig. 6.4, it is

clear that the valence band edge of CuGaSe₂ is below that of CuInSe₂ and the conduction band edge of CuGaSe₂ is above that of CuInSe₂. Thus, the present model shows qualitative agreements with the early experimental results obtained by Turowski et al. [6.2]. In addition, such a band lineup model conforms to the results of theoretical calculations carried out by Wei and Zunger of NREL [6.54]. They have predicted that the conduction band edge of CuGaSe₂ is actually above that of CuInSe₂. Furthermore, Schock and co-workers [5.5,9] also discussed a similar tendency on ΔE_C variation recently, although no computational result was given.

6.3 Energy Band Diagram and Charge Distribution

After the band lineups are determined, energy band diagrams can be constructed. However, it is necessary to make several assumptions for this purpose. First of all, all the semiconductors (ZnO, CdS and CuGa_xIn_{1-x}Se₂) have uniform carrier concentrations. Second, the Fermi level of the low resistivity n⁺-ZnO layer is overlapped with the conduction band edge due to the extremely high carrier concentration ($n \sim 10^{20}$ cm⁻³). Third, since the carrier concentration of ZnO is much greater than CdS and CuGa_xIn_{1-x}Se₂, the depletion region is predominantly located in the n⁻-CdS and p-CuGa_xIn_{1-x}Se₂. Finally, the n⁻-CdS layer is assumed to be fully depleted in thermal equilibrium. Following these four assumptions, the energy band diagrams could be drawn. Fig. 6.5 shows a schematic energy band diagram for a typical ZnO/CdS/CuGa_xIn_{1-x}Se₂ cell. In the figure, the band bending inside the depletion region is approximated by straight lines for simplicity. In such a three layer structure, the entire thickness of ZnO (~ 1.5 μ m) is under a flat band condition due to the extremely high carrier concentration, while the high resistivity n⁻CdS layer (~ 50 nm) is assumed to be fully depleted. The structure is then terminated with a partially depleted CuGa_xIn_{1-x}Se₂ single crystal. To understand the charge distribution, let us first consider the carrier concentration in each of the semiconductors. It has been found in our laboratory that the carrier concentrations of ZnO and CuGa_xIn_{1-x}Se₂ are approximately 10²⁰ cm⁻³ and 10¹⁷ cm⁻³, respectively. Here, it is necessary to determine the carrier concentration of the CdS films prepared by CBD method was reported to vary between 1 and 10 cm²-V⁻¹s⁻¹ by various research groups [4.54-55,59,91, 6.24]. Since the resistivity of the CdS films prepared in our laboratory was determined to be 5 x 10⁴ Ω -cm [4.26-27], the carrier concentration of the CdS films could be calculated using the follow expression,

$$\rho = \frac{1}{q\mu n} \tag{6.5}$$

where ρ is the film resistivity, q is the electron charge, μ is electron mobility and n is electron concentration. The result thus indicated that the electron concentration in the CdS film varies between 10¹³ and 10¹⁴ cm⁻³. For the purpose of the charge distribution estimation, the carrier concentration of CdS is taken as 10¹⁴ cm⁻³.

For a p-n junction in thermal equilibrium, the total negative charge per unit area in the p side must be equal to the total positive charge per unit area in the n side [2.2]. In the present case where the PV cell is formed in a n^+-n^--p (ZnO-CdS-CuGa_XIn_{1-X}Se₂) structure, the charge distribution complies with the following relation,

$$N_{ZnO}X_{ZnO} + N_{CdS}X_{CdS} = N_{CGIS}X_{CGIS}$$

$$(6.6)$$

here N_{ZnO} , N_{CdS} and N_{CGIS} are the carrier concentrations of ZnO, CdS and CuGa_XIn_{1-X}Se₂, respectively, and X_{ZnO} , X_{CdS} and X_{CGIS} are the corresponding depletion widths in each layer. As previously stated, a fully depleted CdS layer was assumed in the energy band diagram. To verify the validity of this assumption, Eq. 6.6 could be used. Let us consider a hypothetical case where the whole thickness of CdS is just fully depleted (i.e. $X_{CdS} = 50$ nm and $X_{ZnO} = 0$). Taking N_{CdS} and N_{CGIS} as 10^{14} and 10^{17} cm⁻³, respectively. The corresponding depletion width in the p-CuGa_XIn_{1-x}Se₂ side (X_{CGIS}) is equal to 0.5 Å. This result indicates that in order to make 50 nm of CdS fully depleted, a corresponding depletion width of only 0.5 Å is needed in the $CuGa_XIn_{1-X}Se_2$. This is equivalent to a thickness thinner than one atomic layer. Even when the thickness of CdS is as thick as 100 nm, a depletion width of only 1 Å in the $CuGa_XIn_{1-X}Se_2$ is needed to make the CdS film fully depleted. Thus, this criteria could be easily fulfilled in almost all biasing conditions and a large variety of CdS thickness. Furthermore, to verify the assumption of negligible depletion width in the ZnO film, we could consider a hypothetical depletion width of 1 µm inside the p-CuGa_XIn_{1-X}Se₂ crystal. Taking N_{ZnO} , N_{CdS} and N_{CGIS} as 10²⁰, 10^{14} and 10^{17} cm⁻³, respectively, $X_{CdS} = 50$ nm and $X_{CGIS} = 1$ µm. The corresponding depletion width in ZnO is found to be about 1 nm using Eq. 6.6. This value is negligible when compare to the thickness of CdS film and the typical depletion width of $CuGa_{X}In_{1}$. $_{\rm X}$ Se₂. In Fig. 6.6, a schematic representation of charge distribution is shown. Also shown are the corresponding carrier concentration and electric field profile. The charge distribution diagram consists of three regions corresponding to ZnO, CdS and CuGa_XIn₁.

 $_X$ Se₂. In the ZnO layer, a large density of positive charges are accumulated right next to the ZnO/CdS interface. Next is a region of positive charges extend throughout the whole thickness of CdS. Finally, negative charges spread uniformly across the depletion region of CuGa_XIn_{1-x}Se₂.

6.4 Estimation of Built-in Potential

In an energy band diagram, the built-in potential (V_{bi}) is an important parameter. According to author's knowledge, no attempts were made before to deduce the theoretical V_{bi} of ZnO/CdS/CuGa_XIn_{1-X}Se₂ PV cells as a function of Ga content. In this work, the values of V_{bi} are deduced by calculating the shift in Fermi level. In the case where the n⁻CdS layer is fully depleted as discussed before, the Fermi level of p-CuGa_XIn_{1-X}Se₂ should lineup with that of n⁺-ZnO in thermal equilibrium. The magnitude of V_{bi} is then equivalent to the difference between the Fermi levels of ZnO and CuGa_XIn_{1-X}Se₂. Before V_{bi} can be determined, the positions of Fermi levels for both ZnO and CuGa_XIn_{1-X}Se₂ have to be known. While the Fermi level of ZnO is assumed to overlap with its conduction band edge, the position of Fermi level ($E_F - E_V$) with respect to valence band edge for CuGa_XIn_{1-X}Se₂ could be represented by the following expression [2.2]:

$$E_F - E_V = kT \ln\left(\frac{N_V}{p}\right) \qquad \text{eV.}$$
(6.7)

where kT = 0.026 eV at room temperature, N_V is the effective density-of-states in the valence band and p is the carrier concentration. After the determination of Fermi levels, the theoretical V_{bi} can be calculated using the following relationship:
$$V_{bi}(x) = \{ [\Delta E_C(x) + E_G(x) - (E_F - E_V)] - 0.3 \} / q \qquad V, \qquad (6.8)$$

where q is the electron charge. The schematic representation of the above relationship is shown in Fig. 6.7.

For the purpose of above calculation, the value of N_{ν} has to be determined. $N_{i'}$ of a semiconductor can be obtained by the following expression [2.2],

$$N_{\nu} = 2 \left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}} \qquad \text{cm}^{-3}.$$
 (6.9)

where m^{\bullet} is the effective mass of holes in CuGa_XIn_{1-X}Se₂, k is Boltzmann constant, T is temperature, and h is Planck constant.

The effective mass of holes for CuGa_XIn_{1-X}Se₂ was reported to range between $0.7m_o$ and $1.2m_o$ [2.8, 3.71, 6.20-21,23], where m_o is the mass of electron (9.1 x 10^{-31} kg). In this work, m^{\bullet} is taken as $1.0m_o$. Accordingly, N_V is found to be 2.5×10^{19} cm⁻³. Once N_V is obtained, $E_F - E_V$ can be calculated using Eq. 6.7. As a result, the values for $E_F - E_V$ are found to be 0.26, 0.20, 0.14 and 0.08 eV for carrier concentrations of 10^{15} , 10^{16} , 10^{17} and 10^{18} cm⁻³, respectively. In the present case, it is observed that the value of m^{\bullet} does not affect the $E_F - E_V$ calculation significantly. By using either $0.7m_o$ or $1.2m_o$ instead of $1.0m_o$, the difference in Fermi level calculation is within ± 0.01 eV.

Hence, using Eqs. 6.1, 6.2, 6.7 and 6.8, the variation of V_{bi} as a function of Ga content can be computed for absorbers with different carrier concentrations. The corresponding results are plotted in Fig. 6.8. The values of V_{bi} are seen to vary from about 0.85 to 1.25 V depending on Ga content and carrier concentration. Generally speaking, V_{bi} increases as Ga content and hole concentration are increased. Here, only the total

built-in potential of the whole PV cell is calculated. In principle, the total built-in potential of such a cell structure should be shared by both the CdS side and the CuGa_XIn₁. _xSe₂ side. Hence, $V_{bi} = V_{bi,CdS} + V_{bi,CGIS}$. The corresponding schematic representation indicating the contributions from both CdS and CuGa_XIn_{1-x}Se₂ is shown in Fig. 6.9. However, not enough information is available to separate the two contributions at this moment.

6.5 Estimation of Lattice Mismatch

It is well known that lattice mismatch plays an important role in affecting the properties of heterojunctions. To understand the properties of ZnO/CdS/CuGa_XIn_{1-X}Se₂ PV cells, the theoretical lattice mismatches of the ZnO/CdS and CdS/CuGa_XIn_{1-X}Se₂ interfaces must be known. As mentioned in chapter 4, the CBD CdS films were often found to have a mixed hexagonal (wurtzite) and cubic (zincblende) phase. This was (1997) recently confirmed HR-TEM high by a study on efficiency ZnO/CdS/Cu(Ga,In)Se₂ cells [4.90]. Therefore, in dealing with the lattice mismatch involving CBD CdS, both structures have to be considered. In this work, the matching examined interfaces are h-ZnO(001)/h-CdS(001), h-ZnO(001)/c-CdS(111), h- $CdS(001)/ch-CuGa_XIn_{1-X}Se_2(112)$ and $c-CdS(111)/ch-CuGa_XIn_{1-X}Se_2(112)$. Fig. 6.10 shows schematic diagrams of matching planes: (a) h-ZnO(001) and h-CdS(001), (b) c-CdS(111) and (c) ch-CuGa_XIn_{1-X}Se₂. Also shown are the corresponding inter-atomic distances (l) in terms of lattice constant a.

To start, the ZnO/CdS interface is first considered. The lattice constant *a* of h-ZnO films prepared by rf-sputtering was found to be 3.26 Å [6.25-26]. For h-CdS and c-CdS films prepared by the CBD method, *a* was found to be 4.16 and 5.83 Å [4.53,57], respectively. For the h-ZnO and h-CdS, the inter-atomic distance (*l*) on the (001) plane is equal to the lattice constant *a*. However, in the case of c-CdS(111), $l = a/\sqrt{2} = 4.12$ Å. Once all the inter-atomic distances are known, the lattice mismatch could be calculated using the following equation:

$$\Delta l_{h,c} = \frac{l_{h,c-CdS} - l_{h-ZnO}}{l_{h,c-CdS}}$$
 (6.10)

As a result, Δl is found to be 22 % and 21 % for h-ZnO/h-CdS and h-ZnO/c-CdS, respectively. Such a large lattice mismatch suggests that the ZnO/CdS interface could possess extremely high density of interfacial states.

To understand the lattice mismatch between CdS and CuGa_XIn_{1-X}Se₂, variation in lattice constant for CuGa_XIn_{1-X}Se₂ with different Ga content has to be considered. According to Eq. 3.4 deduced earlier, the lattice constant (*a*) varies linearly with Ga content. If an axial ratio (c/a) of 2 is assumed, the lattice mismatch could be calculated using the expression,

$$\Delta l_{h,c} = \frac{l_{h,c-CdS} - l_{ch-CGIS}}{l_{h,c-CdS}}$$
 (6.11)

where $l_{ch-CGIS} = a/\sqrt{2}$ on the (112) plane of CuGa_XIn_{1-X}Se₂ and *a* varies linearly according to Eq. 3.4. Following the calculation, the lattice mismatch is found to increase linearly with Ga content. In the case of h-CdS, the mismatch increases from 2 % to 5 % when x is increased from 0 to 1. For c-CdS, smaller mismatches are resulted, the corresponding range is found to be 1 % to 4 %. Fig. 6.11 shows the plots of mismatch as a function of Ga content for both h-CdS and c-CdS. In addition, the average of this two plots is also shown. The later plot is probably a good estimation for CdS films with a mixed hexagonal and cubic phase.

According to the model established by Oldham and Milnes [6.27], the lattice mismatch of a heterojunction has a profound impact on the dangling bond density and hence, interfacial state density. Kressel [6.28] further proposed that the density of recombination centers and interface recombination velocity are roughly proportional to lattice mismatch. Moreover, according to the calculations performed by Kazmerski [6.29] on the interfacial state density in heterojunction PV cells whose window is h-CdS, the interfacial state density was found to increase from about 0.6 x 10^{13} cm⁻² to 3.1 x 10^{13} cm⁻² ² for lattice mismatch ranging from 1 % to 5 %. A similar calculation performed by Arndt et al. [6.48] on the interfacial state density between h-CdS and CuGaSe₂ revealed an even higher density of 6×10^{13} cm⁻². Such results from theoretical calculations are supported by a recent (1997) experimental study on interfacial state density of thin film ZnO/CdS/Cu(Ga,In)Se₂ cells with a low Ga content. Igalson and Stolt [6.52] found that the density of interface electron traps at the CdS/Cu(Ga,In)Se₂ interface is at least 10¹³ eV⁻¹cm⁻². Since lattice mismatch at the CdS/CuGa_XIn_{1-x}Se₂ interface is proportional to Ga content as shown in Fig. 6.11, it could be concluded that the interfacial state density increases as the Ga content is raised. Furthermore, the lattice constant of CdS is larger than that of $CuGa_XIn_{1-X}Se_2$ for the whole range of Ga content, it is generally believed that

the dangling bonds at the interface mainly originate from the material with smaller lattice constant [6.27-28], i.e. $CuGa_XIn_{1-X}Se_2$. Therefore, the reduction of surface defects at the $CuGa_XIn_{1-X}Se_2$ surface prior to CdS deposition appears to be crucial in achieving high quality cells.

In this section, the lattice mismatch estimations are made on the best matching planes. In reality, if polycrystalline thin films or randomly oriented crystals are used as the absorber, the lattice mismatch could be much larger. Nonetheless, the main purpose of the present estimations is to understand the trend of lattice mismatch as a function of Ga content.

6.6 Dark Diode Currents

Previously, the forward current mechanism of single crystal ZnO/CdS/CuInSe₂ [2.9, 4.4] and ZnO/CdS/CuGaSe₂ [4.6, 6.30] cells had been studied in detail. However. very little discussion has been directed to the reverse current mechanism. Therefore, attention is first directed to the reverse current transport in this section. After that, the forward current transport is discussed based on the energy band diagram established in the previous section.

6.6.1 Reverse Dark Diode Current

The reverse current of a p-n junction can usually be formulated as the sum of diffusion currents from the neutral regions and generation current from the depletion region [2.2]. However, in the case of a heterojunction, current conduction due to shunting

and/or inter-band tunneling could also play an important role. Therefore, the total reverse current density (J_R) could be represented by,

$$J_{R} = J_{diff} + J_{gen} + J_{nun} + J_{sh} \quad , \tag{6.12}$$

where J_{diff} , J_{gen} , J_{tun} and J_{sh} are the diffusion, generation, tunneling and shunting components of the total current density. Generally speaking, the diffusion current does not have a strong dependence on bias voltage and tends to saturate. On the other hand, generation, tunneling and shunting currents tend to depend strongly on bias voltage.

In this work, the reverse currents of all the cells regardless of Ga content were found to be strong functions of reverse bias. Such a phenomenon has previously been observed in single crystal CuInSe₂ cells fabricated in our laboratory [2.9]. The reverse dark J-V characteristics of three typical cells are shown in Fig. 6.12. The cells shown were fabricated on Ar annealed substrates. Similar phenomenon is also observed on cells without substrate annealing. However, the magnitude is usually much larger. As can be seen in Fig. 6.12, the reverse currents show a soft breakdown with increasing bias. Since diffusion current usually shows saturation and is not a strong function of bias voltage, it is unlikely that the reverse current obtained in the present cells is dominated by diffusion process.

To clarify the nature of the reverse current, the reverse current density (at V = -1 V) for cells with and without substrate annealing is plotted against absorber bandgap in Fig. 6.13. The reverse current data are obtained from the same set of cells presented in Table 5.3, while the bandgaps are deduced using Eq. 6.2. For cells with no substrate annealing, the reverse currents tend to be much larger and vary randomly without

showing any dependence on absorber bandgap. On the other hand, for cells with substrate annealing, the reverse currents are generally found to be smaller and decrease exponentially with bandgap. A possible hypothesis to explain this behavior is given below.

For substrates without annealing, the highly damaged surface caused by abrasive polishing creates a notable amount of shunting paths at the CdS/CuGa_xIn_{1-x}Se₂ interface. These shunting paths dominate the reverse current transport. Thus, the reverse current appears to be independent of absorber bandgap. However, for cells with substrate annealing, the interface properties are greatly improved. This leads to a significant reduction in shunting paths and the effect of bandgap on magnitude of reverse current is then revealed. Hence, the results suggest that the reverse current for cells without substrate annealing is dominated by shunting. On the other hand, the reverse current for cells with substrate annealing is dominated by generation and/or tunneling. As discussed in chapter 2, the shunt resistance plays an important role in affecting V_{OC} . Therefore, the reduction in shunting current in the present case is consistent with the results presented in chapter 5 that higher V_{OC} is obtained for cells with substrate annealing.

To further clarify the reverse current conduction mechanism, the equation for generation current is examined. If we assume the charge carriers are mainly generated in the $CuGa_XIn_{1-X}Se_2$ side, the generation current density could be written as the following [2.2],

$$J_{gen} = \frac{qn_{i}W}{\tau_{e}} \qquad , \qquad (6.13)$$

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where q is electron charge, n_t is intrinsic carrier concentration of CuGa_XIn_{1-X}Se₂, W is depletion width in CuGa_XIn_{1-X}Se₂, and τ_e is effective lifetime of charge carriers inside the depletion region.

According to Eq. 6.13, J_{gen} is proportional to n_i which is in turn proportional to $exp(-E_G/2kT)$. Hence, as the bandgap of CuGa_xIn_{1-x}Se₂ is increased, the reverse diode current is expected to reduce exponentially. Thus, the data presented in Fig. 6.13 seem to show qualitative agreement with Eq. 6.13. However, more detailed analysis on the exponential relationship suggests this is not the case. In the generation current, the coefficient in the exponential function has the form of -1/2kT. At room temperature, the corresponding value equals to -19.2 eV^{-1} . With this value, the generation current should decrease by about 5 orders of magnitude as the bandgap increases from 1 to 1.65 eV. However, as shown in Fig. 6.13, the magnitude of reverse current only decreases by about 1 order of magnitude in the same bandgap range. Therefore, it is doubtful that the reverse current is dominated by the generation mechanism. Furthermore, according to Eq. 6.13, the generation current is also proportional to depletion width (W) which is in turn proportional to $(V_{bi} + V_R)^{1/2}$ where V_R is reverse bias voltage. Such a square root dependence on reverse bias does not fit the soft breakdown pattern observed in the present case. Given that such a soft breakdown is a typical behavior for inter-band tunneling mechanism [6.33], it is suspected that the reverse currents are dominated by inter-band tunneling which also shows a reduction in reverse current with increasing bandgap [2.2]. Although in the later case the reverse current has a more complex bandgap dependence.

According to the analysis performed by Bell Laboratories [6.33-34], a plot of $d(\ln J_R)/d(\ln V_R)$ versus V_R is a straight line if inter-band tunneling is the dominant mechanism in a reverse biased p-n junction. Therefore, to verify the reverse current transport mechanism, such a plot is made in Fig. 6.14 for the J-V characteristics presented in Fig. 6.12. It can be seen from the figure that the values of the derivative $d(\ln J_R)/d(\ln V_R)$ could be fitted with linear functions. Thus, based on the present analysis, it is suggested that the reverse currents are dominated by inter-band tunneling mechanism for cells with substrate annealing. Indeed, inter-band tunneling was also suggested to be the reverse current mechanism in thin film ZnO/CdS/CuInSe₂ cells [6.35].

6.6.2 Forward Dark Diode Current

The dark forward currents for single crystal ZnO/CdS/CuInSe₂ and ZnO/CdS/CuGaSe₂ cells have been studied in detail by our laboratory [2.9, 4.4] and Saad et al. [4.6, 6.30], respectively. By examining the temperature dependent J-V characteristics, both laboratories concluded the forward currents are dominated by tunneling. In particular, a multi-step tunneling process was suggested by our laboratory. Previous result from our laboratory also suggested that substrate annealing in Ar led to the reduction of forward (tunneling) current [2.9]. In this work, a similar behavior was also observed in most of the cases. As an example, the J-V characteristics (in semi-log scale) for two CuInSe₂ cells, one with (A-2) and one without (A-1) Ar substrate annealing, are shown in Fig 6.15. In addition to single crystal cells, tunneling was also suspected to play an important role in thin film ZnO/CdS/CuInSe₂ cells by other

laboratories [4.9, 6.31-32]. Indeed, the tunneling mechanism is commonly observed in other heterojunction PV cells such as Cu_2S/CdS [2.1] and ITO/Si [2.2] cells. In this work, the temperature dependent J-V analysis is not repeated. However, a discussion on alternate tunneling paths will be presented based on the analysis of energy band diagram and lattice mismatch results obtained in previous sections.

Previous study from our laboratory suggested that the tunneling currents may originate from the CdS/CuInSe₂ interface and assisted by interface and/or deep states in CuInSe₂. In addition, more than one tunneling path was observed. By examining the energy band diagram constructed in previous section, it is reasonable to expect that the tunneling process begins at the ZnO/CdS interface and/or the CdS/CuGa_XIn_{1-X}Se₂ interface. In Fig. 6.16, two situations corresponding to ZnO/CdS and CdS/CuGaxIn_{1-x}Se₂ originated tunneling are illustrated. Under forward bias, the injection of electrons begins in the ZnO. The first barrier encountered by the electrons is the 0.3 eV conduction offset between ZnO and CdS. Such a 0.3 eV barrier could act as a sink for some of the injected electrons. Given an extremely high lattice mismatch (> 20 %) at the ZnO/CdS interface as calculated before, the electrons could be trapped at the interfacial states. The tunneling electrons could then be assisted by the deep levels in the CdS and subsequently tunnel into the CuGa_XIn_{1-X}Se₂ for recombination. The electrons not being trapped at the ZnO/CdS interface would continue to travel to the CdS/CuGa_XIn_{1-X}Se₂ interface and start the deep level assisted tunneling process there.

The hypothesis that some of the tunneling process could start at the ZnO/CdS interface is supported by the results obtained by Saad et al. [4.6]. Their results on

photoluminescence of CBD CdS film and ZnO/CdS/CuGaSe₂ cell suggested the existence of deep levels in the CdS film and such deep levels may be capable of trapping and emitting charge carriers. Based on their results, they also suspected CdS played an important role in the tunneling process. Though it is difficult to prove the above hypothesis due to the indistinguishable temperature dependence of I-V characteristics for tunneling currents originating from ZnO/CdS and CdS/CuGa_XIn_{1-X}Se₂ interfaces, from the standpoint of energy band diagram and lattice mismatch, it is not appropriate to neglect the effect of the ZnO/CdS interface. Indeed, in a simulation study of CuInSe₂ cells, Lee and Gray [6.36] also pointed out the importance of interface properties between ZnO and CdS on PV cell performance. The fact that more than one tunneling path was found previously does not contradict the above hypothesis, although it is still not clear whether the multiple tunneling paths originate from different bandgap states or different interfaces.

6.7 Current Transport Mechanism Under Illumination

In this section, the current transport under illumination will be discussed. Efforts are concentrated on the analysis of results obtained from cells with substrate annealing. The current transport mechanisms under illumination have been investigated by various researchers on thin film $CuGa_XIn_{1-x}Se_2$ cells [4.38-39, 6.35,37-42]. In all of the above studies, there is one common observation. Under illumination, the J-V characteristics were found to shift towards smaller voltage regime.

In this work, a similar behavior is also observed. Fig. 6.17 shows the dark $(J_D(V))$ and light $(J_I(V))$ characteristics for a typical ZnO/CdS/CuGa_XIn_{1-X}Se₂ cell with x = 0.45. The illuminated characteristics were obtained under 100 mW-cm⁻² intensity. Also shown in the figure, in dashed line, is the vertical translation $J_I(V) + J_{SC}$ of the illuminated characteristics displaying the voltage shift. In Fig. 6.18, the $J_D(V)$ and $J_I(V) + J_{SC}$ are also plotted in a semi-log scale. It can be seen that relatively a large discrepancy is present in the low current region. This confirms that the failing of superposition is not due to the effect of light sensitive series resistance. Ideally, the two curves, $J_D(V)$ and $J_I(V) + J_{SC}$, should be superimposed if the diode current transport is not affected by the injection of photons and the photo-generated current is a constant which is independent of bias voltage. Hence, a failure in superposition implies one or both of the following: (1) the diode current transport is light sensitive and could be modified by photon injection, (2) the photo-generated current is a function of bias voltage.

To explain the similar behavior on thin film ZnO/CdS/CuInSe₂ cells, Potter and co-workers (1985-86) [6.35,37] employed a voltage dependent current collection model. In their model, the diode current transport is assumed not to be affected by illumination. The illuminated current follows the following relation:

$$J_{I}(V) = J_{D}(V) - J_{SC} H(V) , \qquad (6.14)$$

where H(V) is the collection function. Such a collection function is assumed to be independent of light intensity.

Using this collection function model, Potter [6.37] verified its validity experimentally. The author measured the spectral response of the cell at different forward

bias voltage using an extremely low level illumination (~ 1 mW-cm^{-2}). Using such spectral response data, a wavelength independent collection function was obtained. The obtained collection function was then found to be able to predict the illuminated J-V characteristics of the same cell under 100 mW-cm⁻² illumination. If the diode current transport mechanism is light sensitive, the collection function obtained in low level illumination should not be able to predict the J-V characteristics at high level illumination. Therefore, such results suggested the diode current transport mechanism is not affected by the injection of photons.

Potter and co-workers [6.35] interpreted the collection function H(V) as a function of carrier mobility, electric field at the interface and interface recombination velocity. In such an interpretation, electric field at the interface varies due to the change in bias. The interface recombination velocity varies due to the shifting of Fermi level at different bias. The hypothesis is that the number of electrically active traps at the CdS/CuInSe₂ interface is a strong function of Fermi level. As the forward bias is increased, the number of electrically active traps at the interface could increase drastically. This situation is translated into an increase in interface recombination velocity, thus increasing the likelihood of interface recombination for photo-generated carriers. This hypothesis is supported by a later (1990) study on thin film CuInSe₂ cells [6.50]. In such a study, Mauk et al. investigated in detail the capacitance-voltage characteristics of the thin film cells obtained from three different laboratories under dark and illuminated conditions. Their results revealed that the density of extraneous states increased notably as the bias voltage was increased. When the bias was changed from 0 to +0.2 V, the density increased by about two times. At the same time, the density of extraneous states was found to be insensitive to injection of photons. Therefore, these results confirmed that interface properties are not modified significantly under photon injection and the interfacial states are mainly electrically activated. Such a light insensitive behavior in the density of bandgap states could explain why the diode current is insensitive to light intensity.

In Potter's interpretation, the effect of deep levels is not considered. As will be discussed in the next chapter, according to the results from our laboratory as well as others, deep levels are present in both single crystal and thin film CuInSe₂. Therefore, neglecting deep levels in the interpretation seems to be unrealistic. However, this does not affect the validity of the voltage dependent current collection model. Whether the recombination is due to interface or deep level recombination, the collection function could still be voltage dependent and independent of light intensity.

Recently, Shafarman et al. (1996) [4.38-39] also observed a voltage dependent current collection phenomenon in their high efficiency (~ 15 %) thin film ZnO/CdS/Cu(Ga,In)Se₂ cells. However, little effort has been directed to verify whether the diode current is independent of light intensity in Cu(Ga,In)Se₂ cells. Until very recently (1997), Phillips et al. [6.38] proved the validity of such a mechanism in thin film ZnO/CdS/Cu(Ga,In)Se₂ cells using a technique originally developed for use in a-Si PV cells [6.43-44]. Their technique is based on the measurement of $J_1(V)$ characteristics at different intensities. For instance, let us assume that $J_{11}(V)$, $J_{12}(V)$ and $J_{13}(V)$ represent J-V characteristics obtained at three different intensities. According to Eq. 6.14, if the diode current is independent of light intensity and the photo-generated current is a function of bias voltage, the expressions for $J_{II}(V)$, $J_{I2}(V)$ and $J_{I3}(V)$ become

$$J_{II}(V) = J_D(V) - J_{SCI} H(V) , \qquad (6.15)$$

$$J_{l2}(V) = J_D(V) - J_{SC2} H(V)$$
 and (6.16)

$$J_{I3}(V) = J_D(V) - J_{SC3} H(V) \quad , \tag{6.17}$$

where J_{SC1} , J_{SC2} and J_{SC3} are the corresponding short circuit current densities at three different intensities. Consequently, we could also subtract any of the above two equations as the following:

$$J_{I3}(V) - J_{II}(V) = (J_{SCI} - J_{SC3}) H(V)$$
 and (6.18)

$$J_{I2}(V) - J_{II}(V) = (J_{SCI} - J_{SC2}) H(V) \qquad (6.19)$$

After re-arranging, the two equations could be written as:

$$H(V) = [J_{13}(V) - J_{11}(V)] / (J_{SC1} - J_{SC3}) \quad \text{and} \quad (6.20)$$

$$H(V) = [J_{12}(V) - J_{11}(V)] / (J_{SC1} - J_{SC2})$$
(6.21)

From Eqs. 6.20 and 6.21, we could then verify the validity of the assumptions made. If our assumptions are correct, the two collection functions H(V) obtained from Eqs. 6.20 and 6.21 should be identical. On the other hand, if the diode current $J_D(V)$ and/or H(V) are indeed intensity dependent, two different collection functions should be resulted. This technique will be used later to verify the validity of the voltage dependent current collection mechanism for the cells fabricated in this work.

Following the model employed by Potter, the collection functions H(V) for three of the cells (A-2, C-3, E-4) are deduced using Eq. 6.14. The results are shown in Fig. 6.19. The $J_1(V)$ characteristics used in Eq. 6.14 are obtained under an illumination level of 100 mW-cm⁻². As can be seen from Fig. 6.19, little reduction in collection functions is detected initially when the forward bias is small. As the forward bias is increased, the collection functions drop significantly. It is found that H(V) starts to drop substantially at about the voltages of maximum power points. Therefore, such a reduction in collection function could severely limit *FF* and V_{OC} .

To verify that such a voltage dependent current collection model is indeed valid, the numerical technique described before is applied. The three intensities used are 0 (Dark), 69 mW-cm⁻² (69 %) and 100 mW-cm⁻² (Full). Fig. 6.20 shows the resulted collection functions for cell C-3 obtained from three pairs of illumination conditions: Dark - Full, 69 % - Full and Dark - 69 %. It can be seen that the three curves are closely matched. Thus, the present results suggest that both the diode current $J_D(V)$ and the collection function H(V) are insensitive to light intensity. Similar results are obtained on other cells. These results show that the voltage dependent current collection mechanism is important not only in thin film but also in single crystal cells. Such a phenomenon also implies the primary loss mechanism for photo-generated current in the present cells is recombination rather than the change in diode current. The similarity in photovoltaic action between thin film and single crystal CuGa_xIn_{1-x}Se₂ cells is re-affirming the idea that the study of single crystal cells could help understanding the operation of corresponding thin film cells.

Some investigations in early and mid 80's suggested that the collection function in thin film CdS/CuInSe₂ cells was intensity dependent [6.39-40,42,49] and that the failure in superposition could be due to the photoexcitation of interfacial states [6.41,49]. Such

conclusions were drawn on thin films cells which were fabricated using technologies considered to be premature by today's standard. After more than 10 years of research and development, it is not fair to assume the same kind of interface property for the early and modern cells. Since the late 80's, the technologies for the preparation of both the absorber and the window have changed substantially. In the case of window deposition, early CdS/CuInSe₂ cells utilized a thick CdS layer (2 - 3 μ m) prepared by vacuum evaporation with substrate heating, while in today's modern cells the usually adopted ZnO/CdS window structure is often formed using CBD CdS (50 nm) and sputter deposited ZnO (0.35 -2 μ m) without intentional substrate heating. Though it is unlikely that the injection of photons does not modify the interface property of the modern cells at all, the results obtained in this work and from other laboratories [6.37-38] suggest such an effect is small when compared to the dominant voltage dependent current collection mechanism.

Apart from the analysis performed in previous paragraphs, strong evidence of the light insensitive diode current could also be obtained from intensity dependence of short circuit currents. It has been established that short circuit currents for ZnO/CdS/CuGa_xIn₁. $_x$ Se₂ PV cells vary linearly with light intensity [4.7, 6.31,56] and that the linearity spans a wide range of intensities from 0 to 130 mW-cm⁻². Such a linear dependence is supporting the idea that recombination probability of photo-generated carriers is independent of light intensity. If photoexcitation of bandgap states is so significant that it really plays an important role in modifying the interface property, the amount of electrically active states and hence recombination probability should increase as the light intensity is increased. Under such a situation, the rule of linearity could not have been followed.

As proposed by Potter, the origin of the voltage dependent current collection may be due to the recombination of photo-generated carriers at the CdS/CuGaxIn_{1-x}Se₂ interface. Such a severe interface recombination could be understood by examining the energy band diagram. In Fig. 6.21, the energy band diagram of a typical $CuGa_{XIn_{1-X}}Se_2$ cell under illumination is shown. Due to the large bandgaps of the ZnO/CdS window structure, most of the photo-generated carriers are generated in the $CuGa_xIn_{1-x}Se_2$ side. Upon generation, most of them will be swept across the depletion region and contribute to electric current. However, some of the carriers will be lost through recombination processes including interface, space charge and bulk recombinations. In the case of CuInSe₂ (x = 0), the conduction band discontinuity ΔE_C is 0.4 eV. Thus, the conduction band forms a spike-and-notch type barrier. It is well known that such a barrier could act as an efficient sink for photo-generated electrons [6.22,45] in PV cells. This barrier can promote interface recombination and space charge recombination close to the interface. As the forward bias is increased, the electric field close to the interface reduces, while the barrier height of the spike remains unchanged. A smaller electric field implies a lower carrier velocity which makes the carriers more vulnerable to recombination. Although the lattice mismatch is relatively small (~ 1 %) between CdS and CuInSe₂, the existence of such a spike in the conduction band could limit the photo-generated current especially in large forward bias where the electric field is small.

Therefore, from the standpoint of energy band diagram, one could expect a reduction in interface recombination with a diminishing ΔE_C . Thus, the interface recombination could be greatly reduced for CdS/CuGaSe₂ since ΔE_C equals to 0.

However, this might not be the case. As discussed before, the increase in Ga content is associated with an increase in lattice mismatch between CdS and CuGa_XIn_{1-X}Se₂. When Ga content (x) is increased from 0 to 1, the lattice mismatch increases by about three times. This drastic increase in lattice mismatch would be translated into an increase in interfacial state density with similar proportion. Such an increase in interfacial state density could suppress or even mask out completely the benefits obtained from the reduced ΔE_C .

In addition to the interface and space charge layer recombinations, bulk recombination could also be an issue although it is believed that this plays a less important role. As the forward bias is increased, the depletion width reduces. Such a reduction in depletion width increases the influence of bulk recombination. However, due to the large absorption coefficient of $CuGa_xIn_{1-x}Se_2$, most of the photons in the solar spectrum will be absorbed within the first 0.5 μ m of the absorber. With minority carrier diffusion lengths in the order of 1 μ m, the effect of bulk recombination should be small when compared to interface and space charge recombinations. On the whole, the phenomenon of voltage dependent current collection seems to be an intrinsic problem for ZnO/CdS/CuGa_xIn_1-xSe_2 PV cells. A small lattice mismatch is associated with a large conduction band spike, while a small conduction band spike is accompanied by a large lattice mismatch. Such a problem cannot be resolved by simply varying Ga content. To tackle this problem, different window materials or buffer layers with lattice and band edge matching have to be chosen for absorbers with different Ga content.

6.8 Conclusions

The energy band diagrams of ZnO/CdS/CuGa_xIn_{1-x}Se₂ cells have been constructed. Before constructing the band diagrams, the band lineup model for ZnO/CdS/CuInSe₂ cells was determined according to data reported in the latest literature. Based on that, the band lineup model was extended to Ga containing cells by considering variation in electron affinity and energy gap. As a result, a spike-and-notch type barrier was found at the CdS/CuGa_XIn_{1-X}Se₂ interface. The conduction band offset ΔE_C was found to vary from 0.4 eV to 0 eV as x is increased from 0 to 1. The valence band offset ΔE_V was found to reduce from about 1eV to 0.75 eV. Based on these results, the energy band diagrams were constructed. Then, the charge distribution was analyzed by considering the carrier concentration and depletion width in different layers. It has been shown that the thin CdS layer is usually fully depleted and the depletion width inside the ZnO is negligible. Following that, the theoretical built-in potential V_{bi} was predicted based on the relative shift in Fermi level. The built-in potential was found to vary from 0.85 to 1.25 eV for different carrier concentration and absorber bandgaps. Furthermore, the lattice mismatch at ZnO/CdS and CdS/CuGa_XIn_{1-X}Se₂ interfaces were estimated for the best matching planes. It was found that lattice mismatch between ZnO and CdS was in excess of 20 %, while the lattice mismatch between CdS and CuGa_XIn_{1-x}Se₂ increased linearly with Ga content from about 1 % to 4 %. Such an increase in lattice mismatch could lead to a drastic increase in interfacial state density.

The current transport and collection mechanisms have been discussed. In particular, it was concluded that shunting current dominates reverse diode current transport for cells without substrate annealing, while for the cells with substrate annealing, the reverse diode current is believed to be dominated by inter-band tunneling. For the forward diode current, alternate tunneling paths were discussed based on the energy band diagram and lattice mismatch data. In the case of cells under illumination, it has been shown that the photo-generated current in single crystal cells follows a voltage dependent current collection mechanism. Such a mechanism could be represented by a voltage dependent collection function which is independent of light intensity. In addition, the forward diode current was not found to be light sensitive. The above results suggested that the primary loss mechanism of photo-generated current is recombination of charge carriers rather than the change in forward diode current. Discussions of such a voltage dependent collection model were also given based on the variation of energy band diagram and lattice mismatch.



Fig. 6.1. A schematic diagram illustrating the band offsets at ZnO/CdS and CdS/CuInSe₂ interfaces.



Fig. 6.2. Variation of bandgap in $CuGa_XIn_{1-X}Se_2$ with Ga content.



Fig. 6.3. Variation of conduction band offset (ΔE_C) and valence band offset (ΔE_V) for ZnO/CdS/CuGa_XIn_{1-X}Se₂ PV cells.



Fig. 6.4. Band lineup models for ZnO/CdS/CuInSe₂ and ZnO/CdS/CuGaSe₂ PV cells.



Fig. 6.5. Energy band diagram of ZnO/CdS/CuGa_XIn_{1-X}Se₂ PV cells.



Fig. 6.6. Charge distribution of $ZnO/CdS/CuGa_XIn_{1-X}Se_2$ PV cells in thermal equilibrium.



Fig. 6.7. Schematic representation of the built-in potential calculation.



Fig. 6.8. Calculated $V_{bi}(x)$ plotted as a function of Ga content for different carrier concentrations.



Fig. 6.9. Energy band diagram of a ZnO/CdS/CuGa_XIn_{1-X}Se₂ cell showing the built-in potential contribution from CdS and CuGa_XIn_{1-X}Se₂.



Fig. 6.10. Schematic diagrams showing the atomic arrangements of (a) h-ZnO (001) and h-CdS (001), (b) c-CdS (111) and (c) ch-CuGa_XIn_{1-X}Se₂ (112) planes.



Fig. 6.11. Variation of lattice mismatch between CdS and CuGa_XIn_{1-X}Se₂.



Fig. 6.12. Reverse dark J-V characteristics of three cells: A-2, C-3 and E-4.



Fig. 6.13. Dark current density at -1 V for cells with and without substrate annealing.



Fig. 6.14. Values of $d(\ln J_R)/d(\ln V_R)$ plotted against V_R .



Fig. 6.15. J-V characteristics of two CuInSe₂ cells, one with (A-2) and one without (A-1) Ar substrate annealing.


Fig. 6.16. Energy band diagram illustrating the possible tunneling paths.



Fig. 6.17. Dark $(J_D(V))$, light $(J_l(V))$ and transposed $(J_l(V) + J_{SC})$ J-V characteristics of cell C-3 showing the shifting of J-V curve under illumination.



Fig. 6.18. $J_D(V)$ and $J_l(V) + J_{SC}$ of cell C-3 plotted in semi-log scale.



Fig. 6.19. Collection function H(V) plotted against bias voltage for cell A-2, C-3 and E-4.



Fig. 6.20. Collections functions for cell C-3 obtained from three pairs of illumination conditions.



Fig. 6.21. Energy band diagram of a ZnO/CdS/CuGa $_x$ In_{1-x}Se₂ cell under illumination.

Chapter 7

CAPACITANCE MEASUREMENTS OF ZnO/CdS/CuGa_xIn_{1-x}Se₂ PV CELLS

7.1 Introduction

From the discussion presented in chapter 6, it is clear that interfacial states and deep levels have significant impacts on the carrier transports, both in dark or under illumination. The existence of such defects could lead to degradation in PV performance. In this chapter, evidence of interfacial states and deep states will be discussed qualitatively based on capacitance-voltage measurements. Furthermore, deep level results will be reviewed and discussed based on the analysis of deep level transient spectroscopy (DLTS) measurements.

7.2 Capacitance-Voltage Measurements

Quantitative and qualitative information such as carrier concentration, built-in potential, effects of deep states and interfacial states can be obtained from capacitance-voltage (C-V) measurements. The capacitance (C) per unit area of an ideal abrupt p-n junction can be expressed by [2.2, 7.1]

$$C = \left[\frac{q\varepsilon_o\varepsilon_p\varepsilon_n N_A N_D}{2(\varepsilon_p N_A + \varepsilon_n N_D)(V_{bi} - V)}\right]^{\frac{1}{2}} , \qquad (7.1)$$

where ε_o is the free space permittivity, ε_p and ε_n are the corresponding dielectric constants for the p and n type semiconductors, N_A and N_D are the carrier concentrations for the p and n type semiconductors, and V is the applied bias voltage. In the case of n⁺-p junctions where $N_D >> N_A$ or a Schottky junction, Eq. 7.1 can be reduced to

$$C = \left[\frac{q\varepsilon_o\varepsilon_p N_A}{2(V_{b_l} - V)}\right]^{\frac{1}{2}} \qquad (7.2)$$

In analyzing C-V data, the above equation is often expressed in the following form,

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_o\varepsilon_p N_A} (V_{b_I} - V) \qquad . \tag{7.3}$$

In this work, the C-V characteristics will be discussed qualitatively based on $1/C^2$ vs. V graphs obtained at different small signal frequencies. Ideally, if deep and interfacial states are not present, the C-V characteristics should not depend on the frequency of the small signal superimposed onto the dc bias voltage (V). Thus, any frequency dependent C-V characteristics give strong evidence of deep and/or interfacial states. In carrying out C-V measurements, capacitance and voltage values were sampled using a HP 4247A LCR meter and a HP 3468A multimeter. The internal biasing circuit of the LCR meter was used to apply the bias voltage. The control of biasing and data acquisition were performed using an IBM PC computer. A schematic diagram of the C-V measurement system is shown in Fig. 7.1. Two small signal frequencies were used, 1 kHz and 100 kHz. The peak-to-peak magnitude of the small signal used was 20 mV. The data were measured from a bias of -1 V to +0.2 V with steps of 0.05 V. Before each data point was

sampled, a one minute delay time was imposed after switching to a new bias voltage.

Table 7.1 shows the properties of the studied cells.

Sample Number	Ga Content (x)	Substrate Annealing	
CV-1	0.00	No	
CV-2	0.00	Yes	
CV-3	0.45	No	
CV-4	0.45	Yes	
CV-5	1.00	No	
CV-6	1.00	Yes	

Table 7.1.Properties of the studied cells.

In Fig. 7.2, two $1/C^2$ vs. V plots (1 kHz and 100 kHz) are shown for a ZnO/CdS/CuInSe₂ (CV-1) cell fabricated on a substrate without annealing. Two distinct features can be observed. First, there is notable frequency dispersion between the two plots even at a reverse bias of -1 V. Second, the plots are curved close to the zero bias. Such frequency dependent capacitance and curved $1/C^2$ vs. V plots are commonly observed in thin film Cu(Ga,In)Se₂ cells [7.11-13].

According to a widely accepted p-n junction model [7.5], the frequency dependence of the junction capacitance is the result of finite time constants associated with the charging and discharging of the deep states close to the depletion edge. At low frequencies, the frequency of the small signal ac voltage is comparable to the time constants of the deep levels. Thus, the charging and discharging of the deep states could follow the small signal variation. Such a phenomenon will contribute to the measured junction capacitance. Therefore, a higher junction capacitance is expected. At high frequencies, the charge variation on the deep states cannot follow the small signal voltage applied to the junction and hence cannot contribute to the junction capacitance. In this case, lower capacitance is anticipated. These could explain the frequency dispersion between the 1 kHz and 100 kHz plots.

In addition to the effect of deep states, interfacial states could also play an important role in determining the junction C-V characteristics. It can be seen that both plots are curved close to the zero bias. Such curved $1/C^2$ vs. V plots are most likely to be the result of non-uniform carrier concentration or the effect of interfacial states. In this case, since the two plots start to curve at different bias voltages, it is unlikely that the curvature represents a concentration profile. Furthermore, the curvature only appears at small reverse bias indicating that it is not a bulk effect. If it is a bulk effect, the whole graph should be curved. It is believed that the curvatures are most likely caused by interfacial states. As the reverse bias voltage is reduced, the depletion edge will move closer to the interface. Hence, the charging and discharging of interfacial states [7.6] could dominate the C-V characteristics of the junction when the bias is close to zero.

According to the experimental results obtained in chapter 5 and chapter 6, a substrate annealing prior to window deposition greatly reduced the effect of shunting and improved cell performance. These results suggest such cells have better interface quality. If the curvature shown in Fig. 7.2 is indeed caused by interfacial states, similar plots on cells with substrate annealing should give reduced curvatures. To confirm this, C-V measurements were also carried out on cells with substrate annealing. Fig. 7.3 shows the

results of a ZnO/CdS/CuInSe₂ cell (CV-2) on an annealed substrate. It can be seen that the curvature close to zero bias is greatly reduced, indicating the improvement of interface quality. Similar behavior was also observed on other cells. Fig. 7.4 shows the C-V characteristics of two ZnO/CdS/CuGa_{0.45}In_{0.55}Se₂ cells fabricated on substrates with (CV-4) and without (CV-3) Ar annealing. The substrate annealing effect on the curvature of the $1/C^2$ vs. V plots is clearly seen.

From the straight portions of the I/C^2 vs. V plots, carrier concentrations of the CuGa_XIn_{1-X}Se₂ crystals were estimated to be between 10¹⁶ and 10¹⁷ cm⁻³. Accurate evaluation of carrier concentration appeared to be difficult due to the large discrepancy of reported dielectric constants for CuGa_XIn_{1-X}Se₂ crystals ($\varepsilon_p \sim 4 - 16$) [7.7-10]. Furthermore, because of the frequency dispersion and curved I/C^2 vs. V plots, evaluation of built-in potential is not possible.

7.3 Deep Level Transient Spectroscopy

It is well established that defects such as vacancies, substitutional and interstitial defects are dominating the electronic properties of $CuGa_XIn_{1-X}Se_2$ [7.18-19,47]. Such defects create shallow (activation energy < 0.1 eV) and deep (activation energy > 0.1 eV) levels. While the shallow acceptor and donor levels contribute to free carriers in the material, the deep levels could have significant impacts on both the dark and light-generated currents. Therefore, in this section, the properties of the deep levels in $CuGa_XIn_{1-X}Se_2$ crystals are analyzed.

Several methods such as deep level transient spectroscopy (DLTS) [6.39, 7.1,14-29,45], admittance spectroscopy [6.39, 7.2,11-12,30-37] and photoacoustic spectroscopy [7.3-4,38] have been used to study deep levels in CuGa_XIn_{1-x}Se₂. Among all the mentioned methods, DLTS appears to be the most popular technique. Since the discovery of this method in the 1970's [7.39-42], DLTS has emerged to become the standard ASTM testing method for characterizing deep levels in semiconductors [7.43].

The C-V measurements used in the last section could be considered as a steady state technique. In the present work, the characteristics of the deep levels are studied using DLTS, which is a capacitance transient technique. In this section, the basic concepts of DLTS will be briefly described and will be followed by the review and discussion of experimental results. Here, only the most essential concepts and equations are presented. Readers interested in the detailed derivation and theory of DLTS should refer to the original DLTS papers [7.39-42] and standard text books such as Ref. [7.44]. Furthermore, detailed derivation has also been described in a McGill thesis [7.45].

7.3.1 Description of DLTS Technique

There are several variations of DLTS techniques, however, the most commonly used is the conventional DLTS. Conventional DLTS is the least demanding type of DLTS in terms of equipment and data processing. Due to these advantages, it is used in the present work. To understand such a method, let us first consider Fig. 7.5 [7.46]. In Fig. 7.5, the bias sequence, energy band diagrams and the resultant capacitance variation are shown schematically for a typical n^+ -p junction. To simplify the treatment, we will only consider a single majority carrier (hole) deep level.

First, when a reverse bias V_R is applied to the junction (position 1), the emission process dominates the activity of the deep levels inside the depletion width. This is because the emitted holes are swept out of the reverse biased depletion region very quickly, causing a reduction in the recapturing probability. In this situation, the majority carrier trap level inside the depletion region is likely to be emptied. When a fill pulse is applied such that the bias is changed from V_R to zero as shown in position 2, the width of depletion region will reduce. With the high concentration of holes in the quasi neutral region, the formerly empty hole traps are quickly filled by majority carriers. In this case, the capturing process is dominant. Once the deep traps are filled, the junction is then driven to reverse bias V_R again (position 3). At this moment, the trapped holes will start to emit from the deep levels inside the depletion region. Right after switching to reverse bias, the depletion width is the widest and the junction capacitance is the lowest. As more holes are emitted from the deep traps, the net negative charge density inside the space charge region will increase with time. This time dependent variation in charge density will lead to a shrinking of the depletion width. The decrease in depletion width can be detected as an increase in junction capacitance. As a result, a capacitance transient will be observed.

It can be shown that the capacitance transient, C(t), for a junction with a single majority carrier trap level follows the exponential time dependence [7.44]

$$C(t) = C_o \left[1 - \frac{N_T}{2N_A} \exp(-et) \right]$$
(7.4)

with e depending on temperature as

$$e = \frac{1}{\tau} = A_o T^2 \exp\left(-\frac{E_{\tau} - E_{\nu}}{kT}\right) \qquad , \tag{7.5}$$

where C_o is the capacitance without any deep level at reverse bias V_R (according to Eq. 7.4, C_o is also equal to $C(\infty)$), N_T is the concentration of deep traps, t is time, e is the emission rate of the deep level, τ is the time constant of the capacitance transient, $E_T - E_V$ is the activation energy of the hole trap level and A_o is a constant.

From Eqs. 7.4 and 7.5, it is clear that the emission rate and hence the capacitance transient are highly temperature dependent. If the emission rates at various temperatures are known, the activation energy of the deep level can be obtained from the slope of the $ln(e/T^2)$ vs. 1000/T Arrhenius plot. To obtain the emission rate by sampling the capacitance transient, a boxcar technique is employed by the DLTS system used in this work. In this method, the capacitance transient at each temperature is sampled twice at time t_1 and t_2 . The corresponding sampling process is shown schematically in Fig. 7.6 [2.9]. The reciprocal of the time period between two sampling times is referred to as the rate window, $1/(t_2 - t_1)$. From the figure, it can be seen that there is little difference between the capacitance at the two sampling times for very slow and very fast capacitance transients, corresponding to low and high temperatures. Since the shape of the capacitance transient is a function of temperature, at a certain temperature T_{max} , when the

emission rate is in the same order of the rate window, a maximum value $C(t_2) - C(t_1) = \delta C_{max}$ will be obtained. Such a maximum is called a DLTS peak.

To obtain the emission rate (e_{max}) at which $C(t_2) - C(t_1) = \delta C_{max}$. We could simply differentiate $C(t_2) - C(t_1)$ with respect to emission rate (e) and set the derivative to zero. As a result, e_{max} is given by [7.44]

$$e_{\max} = \frac{\ln(t_2/t_1)}{t_2 - t_1}$$
 (7.6)

Hence, every DLTS peak gives a pair of e_{max} and T_{max} which will make one point at the $ln(e/T^2)$ vs. 1000/T Arrhenius plot. For every rate window used, a new data point is obtained. A collection of $C(t_2) - C(t_1)$ vs. T plots for various rate windows is called a DLTS spectrum. The activation energy of the deep level can be deduced quite accurately with four to six data points in the Arrhenius plot. Furthermore, to obtain the trap density, Eq. 7.7 can be used [7.44],

$$N_{\tau} = 2N_{A} \frac{\left| \delta C_{\max} \right|}{C_{o}} \frac{r^{r/(r-1)}}{r-1} , \qquad (7.7)$$

where $r = t_2/t_1$.

The above discussion outlines the procedure to extract the information for a single hole trap level. In the case where multiple hole trap levels are present, the total capacitance transient will be a summation of all the transients due to different trap levels, Hence, more than one DLTS peak could be observed in the same $C(t_2) - C(t_1)$ vs. T plot. To observe the capacitance transients due to minority carrier (electron) trap levels, a forward bias fill pulse was used. Such a fill pulse will result in the injection of electrons from the n⁺ semiconductor into the depletion region of the p semiconductor. Similar trap filling will occur as in the case of majority carrier trap levels. However, since the charge of an electron is opposite to that of a hole, the resulted capacitance transient due to electron emission will decrease with time which is opposite to the capacitance transient due to a majority carrier trap level. In such a case, one could expect to observe negative values for $C(t_2) - C(t_1)$ and hence a negative DLTS peak. In evaluating the activation energy and trap concentration, Eqs. 7.6 and 7.7 remain valid. However, Eq. 7.5 has to be rewritten as

$$e = \frac{1}{\tau} = A_o T^2 \exp\left(-\frac{E_c - E_T}{kT}\right) \qquad , \tag{7.8}$$

where $E_C - E_T$ is the activation energy of the minority carrier trap level. In the case where both majority and minority carrier trap levels are present, such a forward fill pulse will lead to the filling of both types of traps. Thus, positive and negative DLTS peaks could be observed at the same time.

In this work, the DLTS measurements were performed using a Bio-Rad model DL 4600 DLTS system. A HP model 9122 computer was used for data acquisition and processing. A schematic block diagram of the DLTS system used is shown in Fig. 7.7 [2.9]. In carrying out the measurements, reverse bias voltages ranging from 3 to 4.5 V were used. The width of the fill pulse was 50 ms. A zero bias fill pulse was used to investigate the hole trap levels, while a forward +0.4 V fill pulse was used to study the electron trap levels. The rate windows used were between 20 and 1000 s⁻¹. The

temperature range under investigation was between 100 and 350 K. The cooling and heating rate was about 0.2 K-s^{-1} .

According to previous DLTS results obtained in our laboratory [7.16,45] and others [7.17,19,25], the distributions of deep levels are quite distinct for n- and p-type CuInSe₂. Since p-type absorbers are used to fabricate PV cells, the discussion in this section will be focused only on deep levels found in p-type samples.

7.3.2. Review of the DLTS results on CuInSe₂

The deep levels in CuInSe₂ have been widely studied by various laboratories. Table 7.2 summarizes the DLTS results obtained in p-CuInSe₂. Also shown in the same table are the possible causes of the deep levels. Four deep levels are commonly reported in p-CuInSe₂, HL 2, 3, 4 and 6. In particular, HL 3 and 6 are the most commonly detected trap levels. They were found to co-exist [7.14-21,45] in most of the cases, although detection of only one of them was also reported [7.1,18,25-26,29]. Trap levels HL 2 and 4 were also detected more than once. However, these two hole trap levels tended to be detected alone. Since the four mentioned trap levels (HL 2, 3, 4, 6) were detected in both thin film and single crystal devices prepared in various ways, it is very possible that they are intrinsic defect levels which are independent of preparation conditions. Other trap levels including hole and electron traps were only reported once and there is no evidence to suggest that they are formed independent of preparation conditions. In particular, the formation of hole trap levels HL 1, 5, 7, 9 and electron trap level EL 2 could be related to certain device preparation conditions as shown in Table 7.2. The trap densities reported

for various trap levels ranged from 10^{12} to 10^{15} cm⁻³ without any sign of dependence on activation energy. Among all the four intrinsic deep levels, perhaps HL 6 is the one with the most significant impact. Its activation energy is about 0.51 eV which lies right at the mid-gap of CuInSe₂. Such a mid-gap deep level could act as efficient recombination centers.

Deep Level Notation	Activation Energy (eV)	Investigated Structures	Possible Cause	References
HL 1	0.12	Al/TF-CuInSe ₂	Post-fabrication annealing in Se vapor	[7.20]
HL 2	0.18±0.02	Al/SC-CuInSe ₂ , ZnO/CdS/TF-CuInSe ₂ , ZnO/CdS/SC-CuInSe ₂	Intrinsic	[2.9, 7.16- 17,29,45]
HL 3	0.23±0.03	Diffused SC-Homojunction, Al/SC-CuInSe ₂ , Al/TF-CuInSe ₂ , (Cd,Zn)S/SC-CuInSe ₂ , ZnO/CdS/TF-CuInSe ₂ , ZnO/CdS/SC-CuInSe ₂	Intrinsic	[2.9, 7.1,14- 21,25,29]
HL 4	0.28±0.01	Al/SC-CuInSe ₂ , Al/TF-CuInSe ₂	Intrinsic	[7.18-19,24]
HL 5	0.32	Al/SC-CuInSe ₂	Post-fabrication annealing in vacuum	[7.19]
HL 6	0.51±0.03	Diffused SC-Homojunction, Al/SC-CuInSe ₂ , Al/TF-CuInSe ₂ , (Cd,Zn)S/SC-CuInSe ₂ , ZnO/CdS/TF-CuInSe ₂	Intrinsic	[7.14-21,26]
HL 7	0.70	CdS/TF-CuInSe ₂	Post-fabrication annealing in air	[7.28]
HL 8	0.80	(Cd,Zn)S/TF-CuInSe ₂	Unknown	[6.39]
HL 9	0.85	Indium diffused SC-Homojunction	Diffusion carried out in air	[7.14,45]
EL 1	0.13	(Cd,Zn)S/TF-CuInSe ₂	Unknown	[7.26-27]
EL 2	0.18	Indium diffused SC-Homojunction	Indium diffusion	[7.16,45]
EL 3	0.57	ZnO/CdS/TF-CuInSe ₂	Unknown	[7.21]

Table 7.2. Summary of hole (HL) and electron (EL) trap levels in p-CuInSe₂.

SC - Single crystal, TF - Thin Film

The activation energies for the four intrinsic levels are found to scatter within narrow margins. The scattering in each level is only limited to about ± 0.03 eV. According

to a detailed study of capacitance transients carried out by Igalson and Bacewicz [7.1], the scattered activation energies observed in CuInSe₂ could be the result of distorted capacitance transients caused by a parallel carrier recombination process. Furthermore, from the practical viewpoint, the slightly scattered results could also be the consequence of small composition variation between samples prepared in different laboratories. Anyhow, regardless of the reason of discrepancy, due to the close proximity of the observed activation energies, it is reasonable to interpret the results as four single trap levels.

In our laboratory, the majority of the DLTS measurements in CuInSe₂ were carried out by Li [7.14-16,45] and Yip [2.9]. In particular, Li investigated the deep levels using In and Bi diffused homojunctions and Al/CuInSe₂ Schottky junctions. Yip investigated the deep levels using ZnO/CdS/CuInSe₂ PV cells. According to the results obtained by Li, hole trap levels HL 3 and 6 were found to co-exist in almost all of the homojunctions and Al/CuInSe₂ Schottky junctions, HL 2 was detected alone. As described before, HL 2, 3, 6 are believed to be intrinsic defects which are formed independent of device preparation conditions. These results are similar to the results obtained by other laboratories. In the case of homojunctions, an electron trap EL 2 was also found. Since it has not been reported in any heterojunctions or Schottky junctions, Li attributed this trap level as indium diffusion induced defect level.

In the case of ZnO/CdS/CuInSe₂ PV cells, Yip carried out DLTS measurements for cells fabricated on substrates with and without annealing. However, meaningful DLTS signals could only be extracted from cells with Ar substrate annealing. For cells without substrate annealing, the DLTS spectrum was found to be dominated by capacitance transients that did not change with temperature. Since the dominant forward current transport mechanism was found to be multi-step tunneling, Yip attributed this phenomenon to the de-ionization of interfacial states, through the tunneling process, which interacted with the Fermi level, thus, justifying the lack of temperature dependence. Such a large effect due to poor interface quality is consistent with the results obtained in the previous chapter that the bandgap dependence of reverse dark currents could only be revealed for cells with substrate annealing. In addition, the C-V results discussed in the previous section also indicated the evidence of large interfacial state density for cells without Ar substrate annealing.

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According to Yip's DLTS results for cells with substrate annealing, only relatively shallow levels such as HL 2 and 3 were found. In the five investigated samples obtained from two different ingots, no deep levels closed to the mid-gap such as HL 6 were observed. This result suggested that Ar substrate annealing could reduce the density of the mid-gap deep level (HL 6). Yip believed that the absence of the mid-gap deep level was one of the reasons for the high open circuit voltage and good performance for his cells. This hypothesis was supported by a SERI (now NREL) study [7.17]. For the single crystal (Cd,Zn)S/CuInSe₂ cells prepared by SERI, the shallow level HL 3 and mid-gap level HL 6 were detected to co-exist. The authors attributed the low open circuit voltage (0.25 V) for their single crystal cells to the existence of the mid-gap level. Furthermore, in a separate study carried out by the same group of authors [7.18], the density of the mid-gap HL 6 trap level was found to be 2 to 3 orders of magnitude smaller in thin film

CuInSe₂ than in single crystal CuInSe₂. Such an observation was consistent with the fact that their thin film CuInSe₂ cells showed much larger open circuit voltage than their single crystal cells. Thus, the authors were able to show the impact of the mid-gap deep level on cell performance.

7.3.3 Results on ZnO/CdS/CuGa_{0.3}In_{0.7}Se₂ PV Cells

Since no prior DLTS data were available for Cu(Ga,In)Se₂, this work was concentrated on the analysis of deep level characteristics in Cu(Ga,In)Se₂, six PV cells fabricated on CuGa_{0.3}In_{0.7}Se₂ crystals extracted from two different ingots were studied. The particular composition ($x \sim 0.3$) was chosen because this is the composition ($x \sim 0.25$ to 0.3) adopted in most of the high efficiency thin film Cu(Ga,In)Se₂ cells. To make sure that meaningful DLTS signals were extracted, cells with Ar substrate annealing were studied. The conversion efficiencies of the cells under investigation ranged from 5 % to 6 %.

The results of the DLTS investigation on ZnO/CdS/CuGa_{0.3}In_{0.7}Se₂ PV cells are summarized in the Arrhenius plots as shown in Fig. 7.8. Two hole trap levels and one electron trap level are identified. The trap densities vary from 10^{15} to 10^{16} cm⁻³. The two hole trap levels have activation energies of about 0.32 ± 0.02 eV and 0.43 ± 0.03 eV from the valence band edge. The electron trap level has an activation energy of about 0.51 ± 0.04 eV from the conduction band edge. The 0.32 eV hole trap level is observed in four of the samples (CGIS 1, 4, 5, 6). It is found to co-exist with the 0.51 eV electron trap level (CGIS 4 and 6) or stand alone (CGIS 1 and 5). Meanwhile, the 0.43 eV hole trap level is detected in two of the samples (CGIS 2 and 3). According to Eq. 6.2, the energy gap of $CuGa_{0.3}In_{0.7}Se_2$ is about 1.17 eV. Thus, the 0.51 eV electron trap level is very closed to the mid-gap energy. The presence of such minority carrier trap level close to the mid-gap is potentially detrimental to cell performance.

Two types of DLTS spectrum are usually observed. The first kind consists of relatively broad DLTS signals due to only hole trap levels. An example (CGIS 2) is shown in Fig. 7.9. Although only a single trap level could be deduced from the DLTS spectrum, such broad DLTS spectrum indicates the existence of more than one trap level. This is also evident from the observed capacitance transients. Fig. 7.10 shows a normalized *log [capacitance transient] vs. time* plot of a capacitance transient at 230 K for sample CGIS 2. If the capacitance transient is the result of only one trap level, a straight line should be observed in such a plot. Thus, any non-linear behavior gives strong evidence of more than one trap level. Such a non-linear behavior in capacitance transients had also been observed in our laboratory in single crystal CuInSe₂ samples with multiple trap levels [7.45].

The second type of DLTS spectrum is considered to be more complicated. The DLTS spectrum due to both hole and electron trap levels is observed. Fig. 7.11 shows the DLTS spectrum of sample CGIS 6. Although the DLTS spectrum clearly indicates three groups of DLTS peaks (group A, B, C) due to at least three hole trap levels, reliable activation energy could only be deduced from group B (HL, 0.30 eV) peaks because of the fused DLTS signals. Furthermore, one group of DLTS peaks due to electron trap level (group D) could also be seen. In Fig. 7.11, the DLTS spectrum due to minority carrier

trap level is plotted in the positive capacitance scale. The activation energy of such an electron trap level is about 0.47 eV.

From the above results, it is clear that more than one trap level is present in CuGa_{0.3}In_{0.7}Se₂ crystals and the hole trap levels are found to co-exist with electron trap levels in some of the samples. Preliminary results of this DLTS investigation were first reported in the PVSEC-9 (Japan), 1996. At the time of first disclosure, this was the first study of its kind. Later in 1997, results of two DLTS studies on thin film Cu(Ga,In)Sey devices with similar Ga content were reported in subsequent international conferences [7.22-23]. Nakagawa et al. [7.22] reported a single hole trap level with an activation energy of 0.34 eV. This activation energy is similar to the 0.32 eV hole trap level obtained in this work. Furthermore, Keyes et al. [7.23] observed the co-existence of both hole and electron trap levels. Their results indicate an activation energy of 0.40 eV for the hole trap level. Such a value is also closed to the 0.43 eV hole trap level obtained in this work. However, the activation energy of their electron trap level was 0.31 eV which has not been observed in this study. By comparing the thin film results with the results obtained in this work, it is suggested that both the 0.32 eV and 0.43 eV hole trap levels are caused by intrinsic defects which are independent of preparation conditions. Table 7.3 summarizes the single crystal results obtained in this work and the thin film results reported by other laboratories [7.22-23].

Deep Level Notation	Activation Energy (eV)	Investigated Structures	Possible Cause	References
HL _{0.3} 1	0.32±0.02	ZnO/CdS/SC-Cu(Ga,In)Se ₂ Al/TF-Cu(Ga,In)Se ₂	Intrinsic	This work, [7.22]
HL _{0.3} 2	0.43±0.03	ZnO/CdS/SC-Cu(Ga,In)Se ₂ ZnO/CdS/TF-Cu(Ga,In)Se ₂	Intrinsic	This work, [7.23]
EL _{0.3} 1	0.31	ZnO/CdS/TF-Cu(Ga,In)Se ₂	Unknown	[7.23]
EL _{0.3} 2	0.51±0.04	ZnO/CdS/SC-Cu(Ga,In)Se ₂	Unknown	This work

Table 7.3. Summary of DLTS results in Cu(Ga,In)Se₂ with $x \sim 0.3$.

HL - Hole Trap Level, EL - Electron Trap Level, SC - Single Crystal, TF - Thin Film

7.4 Conclusions

In this chapter, two different capacitance techniques were used to study the properties of $ZnO/CdS/CuGa_XIn_{1-X}Se_2$ PV cells. First of all, steady state C-V measurements were carried out to study the shape and frequency dispersion of C-V characteristics for cells with and without substrate annealing. Evidence showing the existence of both interfacial and bulk states was discussed. From the observed C-V characteristics, substrate annealing prior to window deposition was found to improve the interface properties. This observation is consistent with the experimental results obtained in chapter 5 and chapter 6.

The principles of the DLTS technique were briefly described and a detailed review on the DLTS data obtained by various laboratories was presented. In the present work, deep levels in $CuGa_{0.3}In_{0.7}Se_2$ were studied using the DLTS technique. Two hole trap levels (0.32 eV and 0.43 eV) and one electron trap level (0.51 eV) were deduced from the DLTS spectrum. By comparing the present results with the latest thin film

results, it is suggested that the two hole trap levels observed in this work are intrinsic defects which are formed independent of preparation conditions.

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Fig. 7.1. Schematic diagram showing the C-V measurement setup.



Fig. 7.2. C-V characteristics of a ZnO/CdS/CuInSe₂ cell (CV-1) with no substrate annealing.



Fig. 7.3. C-V characteristics of a ZnO/CdS/CuInSe₂ cell (CV-2) with substrate annealing.



Fig. 7.4. C-V characteristics of two ZnO/CdS/CuGa_{0.45}In_{0.55}Se₂ cells, one with (CV-4) and one without (CV-3) substrate annealing.



Fig. 7.5. Schematic diagrams showing the energy bands, biasing sequence and capacitance transient in DLTS measurements.



Fig. 7.6. Schematic diagram showing the implementation of rate window sampling method in DLTS measurements.



Fig. 7.7. A block diagram of the DLTS system used in this work.



Fig. 7.8. Arrhenius plots showing the DLTS results of ZnO/CdS/CuGa_{0.3}In_{0.7}Se₂ PV cells.



Fig. 7.9. DLTS spectrum of CGIS 2 showing the DLTS signals due to multiple hole trap levels.



Fig. 7.10. Normalized capacitance transient of sample CGIS 2 at 230 K.



Fig. 7.11. DLTS spectrum of sample CGIS 6 showing complicated DLTS signals due to both hole and electron trap levels.
CONCLUSIONS

Photovoltaic cells in the form of ZnO/CdS/CuGaxIn_{1-x}Se₂ have been fabricated on bulk crystalline substrates. The $CuGa_XIn_{1-X}Se_2$ single crystals were prepared using horizontal Bridgman method; while the CdS buffer layer and ZnO window layer were deposited by chemical bath deposition and r.f. sputtering, respectively. Conversion efficiencies exceeding 10 % were achieved in CuInSe₂ and Cu(Ga,In)Se₂ cells. Meanwhile short circuit current densities as high as 16 mA-cm⁻² were attained in CuGaSe₂ cells. In particular, through the optimized CdS deposition scheme, an open circuit voltage of 0.502 V was obtained in a CuInSe₂ cell. This value is believed to be the highest open circuit voltage ever reported in single crystal CuInSe₂ cells. In the case of Cu(Ga,In)Se₂ cells, the highest conversion efficiency of 10.1 % was achieved in a CuGa_{0.45}In_{0.55}Se₂ cell. This result represents a notable improvement over the previous 7 % record set by a single crystal CuGa_{0.50}In_{0.50}Se₂ cell [4.68]. The open circuit voltages obtained in CuInSe₂ and CuGa $_{45}$ In $_{0.55}$ Se₂ cells are comparable to that of high efficiency thin film cells with similar Ga content. For CuGaSe₂ cells, the 16.0 mA-cm⁻² short circuit current density attained in this work is equivalent to the highest value achieved in thin film CuGaSe₂ cell and higher than that of the best single crystal cell with the similar ZnO/CdS/CuGaSe₂ structure reported by other laboratories.

Crystal growth experiments were carried out using a horizontal three zone resistive furnace. It is confirmed that the adhesion problem in the growth of $CuGa_xIn_1$. $_xSe_2$ crystals can be avoided using a method involving an ampoule partially coated by carbon. Using such a method, void-free and crack-free single crystals with a linear dimension up to 1 cm were obtained. Crystals obtained from this method were uniformly p-type with hole concentrations between 10^{16} and 10^{17} cm⁻³. The resulted crystals were found to be suitable for PV cell fabrication. EPMA measurements revealed various tendencies in composition variations along ingots. The majority of the crystals were found to be Cu poor. The variations in ingot composition could be explained qualitatively using established pseudobinary phase diagrams. XRD measurements confirmed that the lattice constants of CuGa_xIn_-xSe_2 crystals varied linearly with Ga content.

Various experiments were carried out to optimize the cell fabrication process. A time efficient crystal polishing procedure was used to replace the original lengthy step. An enhanced CdS deposition scheme was employed to improve both film uniformity and junction quality. The sputtering process of ZnO was optimized for the newly acquired ceramic target. Finally, the cell patterning process was optimized for use in small area $ZnO/CdS/CuGa_xIn_{1-x}Se_2$ cells to achieve highly reproducible results.

The performance of the PV cells was determined using simulated solar lights. The effects of Ar substrate annealing on the performance of cells with different Ga content were investigated. It was found that an Ar substrate annealing prior to the window deposition consistently improved the fill factor and open circuit voltage of the PV cells regardless of the Ga content. However, while reasonably good results were obtained in

low Ga content cells, the performance of high Ga content cells have not yet been optimized. From the results of spectral response measurements, the long wavelength cutoffs were found to shift towards shorter wavelengths as the bandgap of absorber was increased. Different behaviors were observed after post-fabrication annealing in air for CuInSe₂ and CuGaSe₂ cells. While the CuInSe₂ cell degraded significantly after a short annealing, the open circuit voltage of the CuGaSe₂ cell was found to improve through repetitive annealing.

The band lineup model and hence the energy band diagram for $ZnO/CdS/CuGa_xIn_{1-x}Se_2$ cells were discussed. The band lineup model for the CdS/CuGa_xIn_{1-x}Se_2 interface was deduced based on the latest results on CdS/CuInSe_2 heterojunctions and the variations of energy gap as well as electron affinity in CuGa_xIn_1. $_xSe_2$. It was discovered that both the conduction band and valence band offsets at the CdS/CuGa_xIn_{1-x}Se_2 interface decreased as the Ga content was increased. The conduction band at such an interface changed from a spike-and-notch type barrier to zero conduction band offset as Ga content (x) increased from 0 to 1. The charge distribution of the PV cells was also analyzed. It was found that the high resistivity CdS layer was likely to be depleted in most of the biasing conditions.

The theoretical built-in potential for cells with various Ga content and carrier concentration was calculated by considering the difference in Fermi levels. Generally speaking, an increase in built-in potential was observed for increasing Ga content and carrier concentration. Furthermore, the theoretical lattice mismatches at ZnO/CdS and CdS/CuGa_xIn_{1-x}Se₂ interfaces were deduced. For the CdS/CuGa_xIn_{1-x}Se₂ interface, both

wurtzite and zincblende CdS were considered. The transport mechanism for the dark reverse currents was analyzed. The results suggested that the band-to-band tunneling was the dominating mechanism for cells with substrate annealing. For cells without substrate annealing, the reverse currents were found to be dominated by shunting. Alternate tunneling paths were considered for the forward dark currents based on the lattice mismatch data and energy band diagram. Furthermore, the current transport mechanism under illumination was studied for single crystal Cu(Ga,In)Se₂ cells. It was shown that a voltage dependent current collection mechanism led to the apparent shift of the J-V characteristics towards the smaller voltage region upon illumination. Such a voltage dependent current collection mechanism was explained using energy band diagram and lattice mismatch data deduced in this work.

Capacitance measurements were carried out to investigate the interface and bulk properties. Results from the steady state C-V measurements showed strong evidence of interfacial states and deep states. It was found that the quality of the interface was greatly improved for cells with substrate annealing. The deep level characteristics for p-CuInSe₂ were reviewed in detail. Furthermore, the deep level characteristics of Cu(Ga,In)Se₂ mixed crystals were analyzed for the first time using the DLTS technique. PV cells fabricated on CuGa_{0.30}In_{0.70}Se₂ substrates were specifically studied. Two hole trap levels (0.32 eV and 0.44 eV from valence band edge) and one electron trap level (0.51 eV from conduction band edge) were observed. By comparing the results obtained in this work and the latest thin film results, it is suggested that the two hole trap levels are formed independent of preparation conditions. In summary, the main contributions of the present work are listed below. In this research project, the author:

- 1. showed that $CuGa_XIn_{1-X}Se_2$ crystals free from adhesion and suitable for PV cell studies can be grown using ampoules partially coated with carbon;
- studied the composition variation along Bridgman grown CuGa_xIn_{1-x}Se₂ ingots with different starting Ga content;
- optimized cell fabrication procedures such as substrate polishing, CdS deposition.
 ZnO deposition and cell patterning;
- 4. fabricated (a) a single crystal ZnO/CdS/CuInSe₂ (x = 0) cell with the highest reported open circuit voltage, (b) a single crystal Cu(Ga,In)Se₂ (x = 0.45) cell with the highest reported conversion efficiency and (c) a single crystal ZnO/CdS/CuGaSe₂ (x = 1) cell with the highest reported short circuit current density;
- 5. investigated the effects of Ar substrate annealing on the properties of $CuGa_XIn_1$. $_XSe_2$ cells and demonstrated the difficulties of applying an universal fabrication process to produce single crystal $CuGa_XIn_1$. $_XSe_2$ cells with different Ga content;
- 6. determined the spectral response of single crystal $CuGa_XIn_{1-X}Se_2$ cells;
- 7. analyzed the band lineup and built-in potential for $ZnO/CdS/CuGa_XIn_{1-X}Se_2$ cells;
- 8. analyzed and discussed the current transports of single crystal ZnO/CdS/CuGa_XIn_{1-X}Se₂ cells, both in dark and under illumination; and

9. studied the single crystal ZnO/CdS/CuGa_XIn_{1-X}Se₂ cells using capacitance techniques (C-V and DLTS) and analyzed deep level characteristics in CuGa_XIn_{1-X}Se₂ (with x = 0.3).

To the author's best knowledge, the present investigation is the first of its kind ever carried out on single crystal CuGa_xIn_{1-x}Se₂ cells. The investigation spans the whole range of Ga content from x = 0 to x = 1, starts with the synthesis of absorber materials from elements all the way to the characterization of PV cells. Although this thesis examined some of the immediate issues in single crystal CuGa_xIn_{1-x}Se₂ PV cells which had not been explored before, like other scientific researches, many more questions are still unanswered. However, being the first research project of its kind, it can be said that this investigation provides some of the key knowledge necessary for future research in single crystal CuGa_xIn_{1-x}Se₂ PV cells. With further efforts, thorough understanding of the material and cell properties should be possible.

At this moment, two other separate thesis research projects are being carried out in our laboratory to study the properties of single crystal Al/CuInSe₂ Schottky junctions and sodium doping effects on CuGa_XIn_{1-x}Se₂ and Cu(Ga_XIn_{1-x})₃Se₅ crystals and devices. Experimental conditions established in this work, such as crystal growth and device fabrication processes, are currently being used by other graduate students in the above two studies. To further understand the material and device properties, several suggestions for immediate future work are given here in addition to the two ongoing projects. First of all, the diffusion lengths for crystals with different Ga content have not been well established. It is worthwhile to carry out a detailed electron beam induced current (EBIC) study to investigate the effect of Ga content and treatment conditions on diffusion lengths. Second, since cell efficiencies exceeding 10 % have been achieved, it is essential to optimize the thickness of the ZnO window layer and develop an efficient AR coating technique to achieve optimum short circuit current densities. Such developments are important in order to explore the limit of the single crystal CuGa_XIn_{1-X}Se₂ cells. Finally, cell fabrication conditions, such as substrate preparation, CdS deposition and postfabrication annealing, have to be optimized to improve the performance of high Ga content cells.

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Chapter 1

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