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Optoelectronic Circuit design, Packaging and Characterization

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Abstract

The ever increasing demand of communication bandwidth places more stringent demands on the electronic systems. Optical interconnects can help satisfy these requirements. In order for an optical interconnect to be successful, a number of factors must be considered. These include the actual integration of the opto-electronic devices with silicon, the packaging of the opto-electronic chip, power and noise considerations. Of particular interest at present are the Hybrid/SEED devices implemented as Smart Pixel Arrays (SPA) to encode the electronic data (using intensity modulation) onto an array of constant power beams of light. The migration from modulator based systems to emitter based systems is also becoming critical.

This document deals with some aspects of a photonic backplane technology. It deals with the design of opto-electronic chips as well as considering power consumption reduction and noise in these chips. It also deals with the packaging of the chips with considerations of bandwidth and thermal issues. The packaging must deal with the space constraints defined by the optical interconnect as well the provide the electrical connectivity required by the opto-electronic chip. The issues involved in the testing and characterization of the opto-electronic chips as well as the package are also addressed. It contains some preliminary data for driving Vertical Cavity Surface Emitting Lasers (VCSEL) arrays with emphasis on modulation bandwidth. This is for characterizing VCSELs as high modulation bandwidth optical sources. A small signal model for the VCSLEs was also developed to calculate the modulation bandwidth of the VCSELs.

Sommaire

L'augmentation incessante de la demande en bande passante des systèmes électroniques modernes conduit à des problèmes de congestion sur le bus électronique reliant les cartes de processeurs entre elles. Des bus optiques sont envisagés pour permettre de résoudre ces problèmes. Plusieurs problèmes doivent être règlés pour que de telles interconnections puissent supplanter leur rival électronique: l'intégration des circuits opto-électroniques avec des circuits de silicium, l'encapsulage de la puce opto-électronique ainsi que les questions de puissance consommée et de bruit. Les systèmes utilisant des matrices de pixels savants ("smart pixel arrays") à base de circuits Hybrides/SEED sont d'un intérêt particulier pour encoder l'information digitale (en intensité) sur une matrice de faisceaux optiques à puissance constante. La migration de systèmes utilisant des modulateurs vers des systèmes employant des émetteurs est également d'une importance capitale.

Cette thèse adresse quelques uns de ces problèmes. La conception de puces opto-électroniques minimisant la consommation de puissance et le niveau de bruit sera abordée. L'encapsulage des composantes électroniques de façon à optimiser la bande passante et les effets de dissipation thermique seront également à l'ordre du jour. Divers tests de caractérisation ont été effectués sur des matrices de lasers à émission de surface (VCSEL) et des résultats seront présentés. Un modèle à signal faible a été développé pour calculer de façon théorique la bande passante des VCSELs. Ces calculs seront confrontés aux résultats expérimentaux.

Acknowledgements

I would like to thank my supervisor Prof. Frank Tooley most sincerely. Without his constant guidance and encouragement these last two years would not have been the learning experience they were.

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Sanjiv Khurana who was my strength, my support and my inspiration. I could never have done this without him. I would also like to thank my parents-in-law Madan and Adarsh Khurana for all their support and encouragement. In the end I would like to convey my special thanks to my parents Rattan and Radha Mittal for all the love and encouragement that I have received from them all through my life. They have made it possible for me to reach where I am today. Their love and belief in me was always behind me.

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Chapter 1: Introduction

1.1 Motivation

High speed data processing and handling systems, such as ATM switches and parallel computing systems, for years have been based upon an electrical foundation. The requirements of electronic systems are increasing, as the applications for these systems become more complex and require more bandwidth. Computing and switching systems these days are placing heavier demands on their supporting technology than ever before.

On-chip clock rates for current high-speed processor chips are typically 266MHz, resulting in huge aggregate bit rates of almost 100s of Gigabits per second (Gbps) per printed circuit board [1,2,3]. With the increase of off-chip clock rates and the number of pinouts per chip, within a few years, aggregate data rates will be in excess of a terabit per second [4]. Because the aggregate bandwidth of the integrated circuits inside these systems continues to increase, so must the capabilities of the interconnection network [5]. The observation made in 1965 by Gordon Moore, co-founder of Intel was that "the number of transistors per square inch on integrated circuits will double every year". This law has proved to be almost true for more than the past three decades.

Massively Parallel Optical Systems can offer a way to interconnect many data lines at very high data rates for use in future electronic and switching systems. In addition to the increased bandwidth, these interconnects could take advantage of silicon VLSI and opto-electronics to introduce "intelligence" into the interconnect media, e.g. by making the interconnect dynamically reconfigurable. These systems can be designed to support the ever increasing aggregate bit rates generated by

conventional and future silicon processors fig. 1 [2].

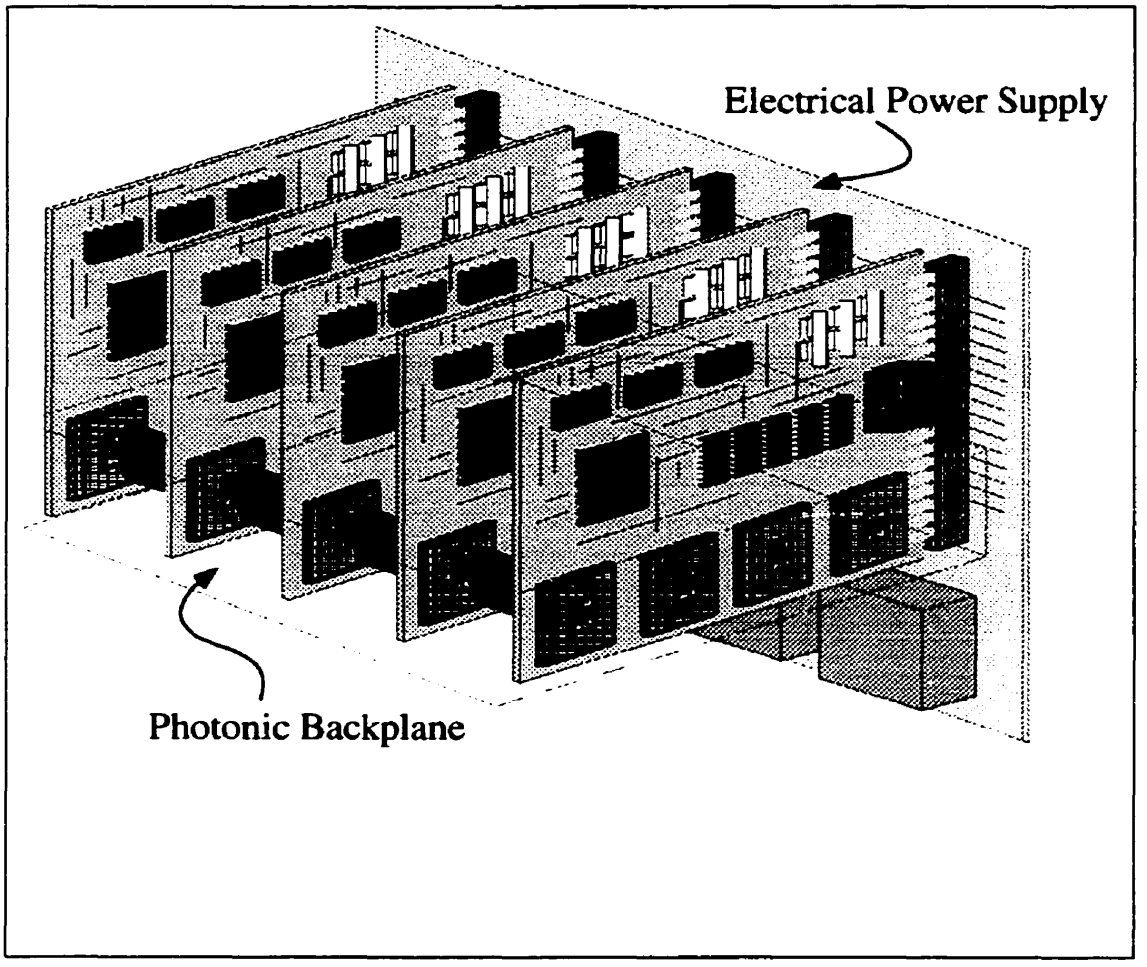

Figure 1: Free Space Optical Interconnect

The primary benefit of free-space optical backplanes is the additional dimension of connectivity that can be introduced. In a typical electrical bus there are typically 32 high speed data lines which are routed along a special PCB with many plug-in slots. In an optical bus, signals are not confined to run along a single plane. By using the third dimension of space, an entire plane can be connected via optical imaging and the linear array of the electrical backplane could be extended to an

array of 32 x 32 (1024) optical data lines within the same physical space. Because the opto-electronics can be made with dimensions in the tens of microns, their capacitance and resistance can be made very small and thus they can be driven at rates comparable with bandwidth of sub-micron silicon transistors [6]. As impedance matching and capacitive loading are no longer issues in Optical Interconnects (Ois), the only power concerns deal with the optical losses within the interconnect, and electrical-to-optical and optical-to-electrical conversions in the transmitter and in the receiver respectively [7]. For optics there is no EMI problem. Another advantage of OIs is that interconnection architectural maps (e.g. fan-in, fan-out, projection, perfect shuffle) can easily be realized with simple optical components (lenses, gratings etc).

Development of the opto-electronic devices that can support a photonic interconnect fabric continues to produce more advanced devices supporting more optical and electrical inputs and outputs, and their speed continues to increase. Hybrid integration of two dimensional arrays of Quantum Confined Stark Effect modulators and detectors onto CMOS circuitry is a reality, and reliable VCSEL detector arrays integrated on CMOS circuitry is in progress, with very promising applications forthcoming. The most critical part is the effective integration of such devices into systems. Such integration requires the successful satisfaction of three fundamental requirements: opto-mechanical interface to the photonic interconnect, electronic interface to the photonic interconnect and the optical interconnect design.

1.2 Thesis Organization

The Smart Pixel Array (SPA) is one method used to interface the electronic processing capability of Silicon with the interconnection capability of free-space-optics [8]. This can be done without significant

change in present-day electronics since these SPAs would themselves be silicon chips. The opto-electronics would simply provide a very large number of optical inputs and outputs by using the surface area of the chips. The optoelectronics would simply provide a very large number of optical inputs and outputs by using the surface area of the chip. The physical implementation of the optics could then remain completely transparent to the data processing elements (memory and CPU).

The current state of Smart Pixel technology is mostly modulator based with Quantum Confined Stark Effect (QCSE) modulators and PIN photodiodes (GaAs based), with underlying silicon processing electronics [9]. The Smart Pixel Technology is fast migrating towards emitter based chips having arrays of Vertical Cavity Surface Emitting Lasers (VCSELs). With the integration of emitters on the chips themselves, there are some critical issue of driving the VCSELs properly becomes significant for optimal communication bandwidths. The bandwidths are also dependant upon the temperature control of the die and packaging of the chips as well the electrical and optical interfaces with the opto-electronic chips. Borrowing from the advances in field of electronics, opto-electronic packaging has advanced steadily [10]. In this field, the major problem is of packaging two-dimensional arrays of surface-active components and to interface them the free-space optical interconnects.

This thesis deals with the design and layout constraints of a Smart Pixel Array and the various issues involved for packaging and characterizing the opto-electronic chips. The first chapter is a description of a 0.5um CMOS VLSI chip which has an array of 8 x 8 Smart Pixels. It describes the architecture of a Reconfigurable Array of Smart Pixels, the layout of the chip as well as the simulation results. Chapter 2 deals with power consumption and noise issues in opto-electronic chips. The first half of this chapter deals with Adiabatic CMOS, which is a power saving

technique in use with electronic chips. This technique is being experimented for use with optoelectronic chips. The second half of this chapter deals with noise reduction in the Smart Pixel Technology by incorporating optical powering rather than the conventional electrical powering.

After the fabrication of the opto-electronic chips, the logical next step is to test and characterize them. This involves the characterization of the photodiodes as well as the testing of the underlying electronic circuitry. Testing and characterizing the smart pixels is the subject of the third chapter. It describes two different optical test rigs designed and aligned for the purpose of testing and characterizing the photodiodes as well as the smart pixels.

Now, the chips have to be integrated into a system and for that there is a need for packaging them and to provide an electrical as well as on optical interface to the chip. Chapter 4 describes such a package and also deals with the testing and the characterization of the package.

As already mentioned, Smart Pixel Technology is migrating from modulator based systems towards Emitter based systems. Keeping this in mind, it is important to examine the behavior of VCSELs before incorporating them into the Smart Pixel Arrays. This includes biasing and driving the VCSELs, temperature characterization of the VCSELs, as well as bandwidth measurements. The next two chapters deal with the packaging and characterization of VCSELs. Chapter 5 deals with the packaging and the characterization of a single VCSEL available commercially in a TO46 can package. This involved designing a suitable PCB to house the VCSEL and to drive it at high modulation frequencies. Chapter 6 deals with designing a package for an array of VCSELs. It deals with characterizing the package as well as the VCSELs. A small

signal model of the VCSELs is also designed and the measured 3dB bandwidth of the VCSELs is compared with the simulated value. Active temperature control of the die substrate is also provided in the package. This package has the capability of driving 40 VCSELs simultaneously with each VCSEL being modulated at multi-gigahertz frequencies.

The Chapter 7 summarizes the material covered in this thesis and discusses the conclusions that can be drawn from it as well as proposing some future directions.

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Chapter 2: An 8x8 Array of Reconfigurable Smart Pixels

2.1 Introduction

Optical Interconnects using free space optics offer us great features in terms of communication bandwidth, data density and speed of communication. This technology tries to exploit the best features of both electronics as well as free space optics. The technology as it stands today, can be divided into three main parts: electronics, optics, and opto-mechanics.

The electronics defines the switching architecture. This usually consists of an opto-electronic chip and an interface to the optics. The chip contains the switching circuitry and the processing circuitry for handling the data. The circuitry is identical for each bit of data and forms a module known as a smart pixel. The smart pixel can be repeated to achieve the desired bit density. The packaging of the chip must facilitate an easy optical interface as well as an easy electrical interface.

The optics section deals with the channeling of the optical beams that carry the information to be communicated. Its main function is to direct a number of parallel optical beams from one optoelectronic chip to another.

The third sub-group is the opto-mechanical subgroup. Its function is to provide the mounting structures for the optics and the electronics so that the entire entity can take the form of a functioning system.

Together these three sections have to work in close coordination, as none of the three parts are independent of each other. The heart of any opto-electronic interconnect is the opto-electronic chip. This defines the interconnect functionality and the versatility of the setup. The Photonic Systems Group at McGill University is involved in the process of

designing demonstrators for the purpose of developing the opto-electronic interconnect technology and to demonstrate its functionality, use and advantages so that it may become a commercial product.

An implementation of the optical backplane concept can be envisaged as shown in Figure 2. In this figure there are a number optoelectronic chips (on daughter boards) able to communicate with one another through the optical ring interconnect.

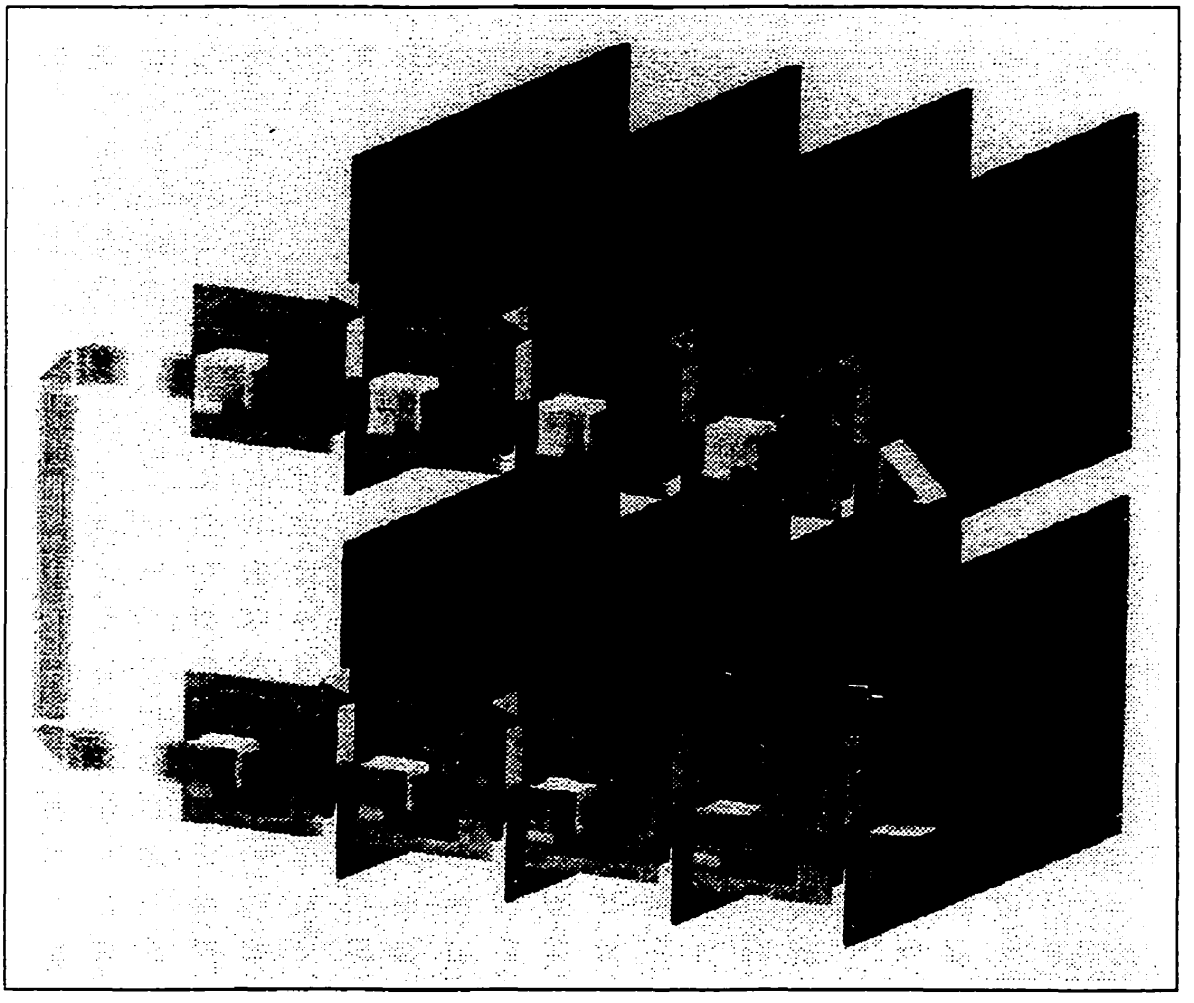

Figure 2: Ring Architecture with the Mother Board Daughter Board Concept

2.2 General Description of the chip

Any optical interconnection network that has a higher than point-to-point connectivity requires an optical or electronic fan-out and fan-in stage. The motivation for the design of the chip that is described here is to develop a low-latency ring-based optical backplane which can be used to interconnect an array of processing elements (PEs) in a multi-processor computer. Desirable properties for such a network when implemented within an optoelectronic technology are:

- Make use of the high potential bandwidth of optics;
- Require moderate off-chip electronic bandwidths;
- Use identical optoelectronic chips at each node;
- Allow modular construction to be scaleable;
- Have a minimum number of active components (modulators or modulators);
- Be robust and flexible (allowing different topologies to be constructed from the same components).

Figure 3 shows the topology of the broadcast bus as an example architecture for the implementation of an optical interconnect. It is considered here as an application of the chip designed. Each board has access to a linear array of optical modulators that inject M-bit words into a unique optical space channel. At each subsequent node $1/(N-1)$ of the signal power is tapped off to a receiver. On each board one receiver is dedicated to each signal and so an array of $(N-1) \times M$ receivers is required for N boards. Electrical fan-in is used to select which of the $N-1$ signals available is used at each node. If a single input channel is selected at each node this architecture is equivalent to a crossbar with optical fan-out and electrical fan-in.

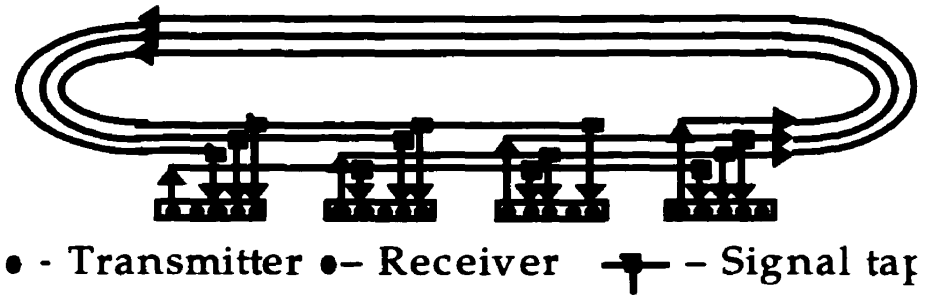

Figure 3: Single bit-slice of broadcast bus.

A schematic of one possible optical implementation of this architecture is shown in Figure 4. Each node contains a linear array of *M* vertical cavity surface emitting lasers (VCSELs) and *N* x *M* detectors. Light is emitted at 980 nm from the VCSEL with a p-polarization state [1], reflected from a micro-prism and injected onto the bus. Between each node an array of space-variant half-waveplates (SWP) is used to rotate the Polarization State of each row of beams by a different angle ($\theta_1 \ldots \theta_N$). A polarizing beam-splitter positioned above each optoelectronic chip is then used to tap a fraction of the signal power into the receiver array in the ratio $1/(N-1)$, $1/(N-2)$ ....1 as the distance from the modulating node increases. This splitting ratio ensures that each detector receives the same power. The untapped power remains as p-polarized light and continues in the bus. The design and layout of the chip for this technique is described in the next few pages.

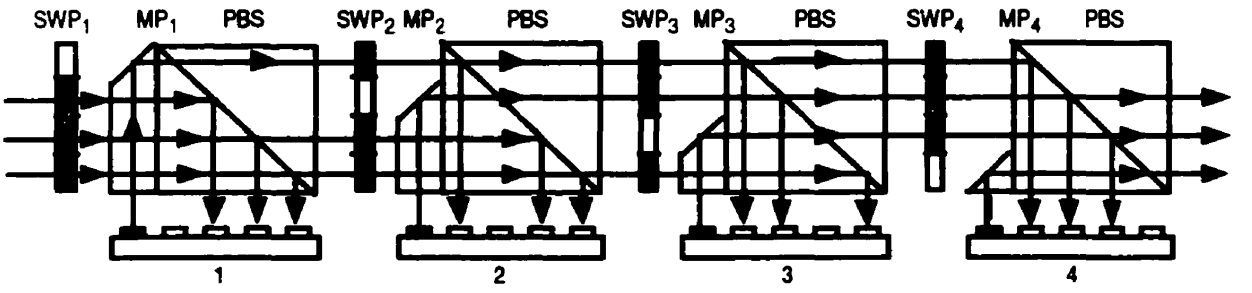

Figure 4. Optical implementation of the broadcast bus with polarization fan-out (SWP – space-variant waveplate, MP – micro-prism, PBS – polarizing beam-splitter).

The main design goal of the chip was versatility. This was achieved by allowing any channel of one chip to communicate with any channel of another chip. The chip consists of eight channels of eight bits each [Figure 5]. Any channel on the chip can be defined as a modulator or as a receiver. However, at a particular time, a channel can only be defined as a modulator or as a receiver, but not both. This is because the same photodiodes are used to transmit as well as receive depending upon the setting of control signals. This chip also has an electrical interface in the form of an 8 bit Electrical input signal port and an 8 bit electrical output signal port.

Figure 5 shows the 2x2 mm chip with a 20x10 array of photodiodes, out of which a 16x8 array were utilized for this chip. Each column forms a channel and they are labeled from A to H. The solid line indicates the area of the 8x8 array (eight channels of eight bits each).

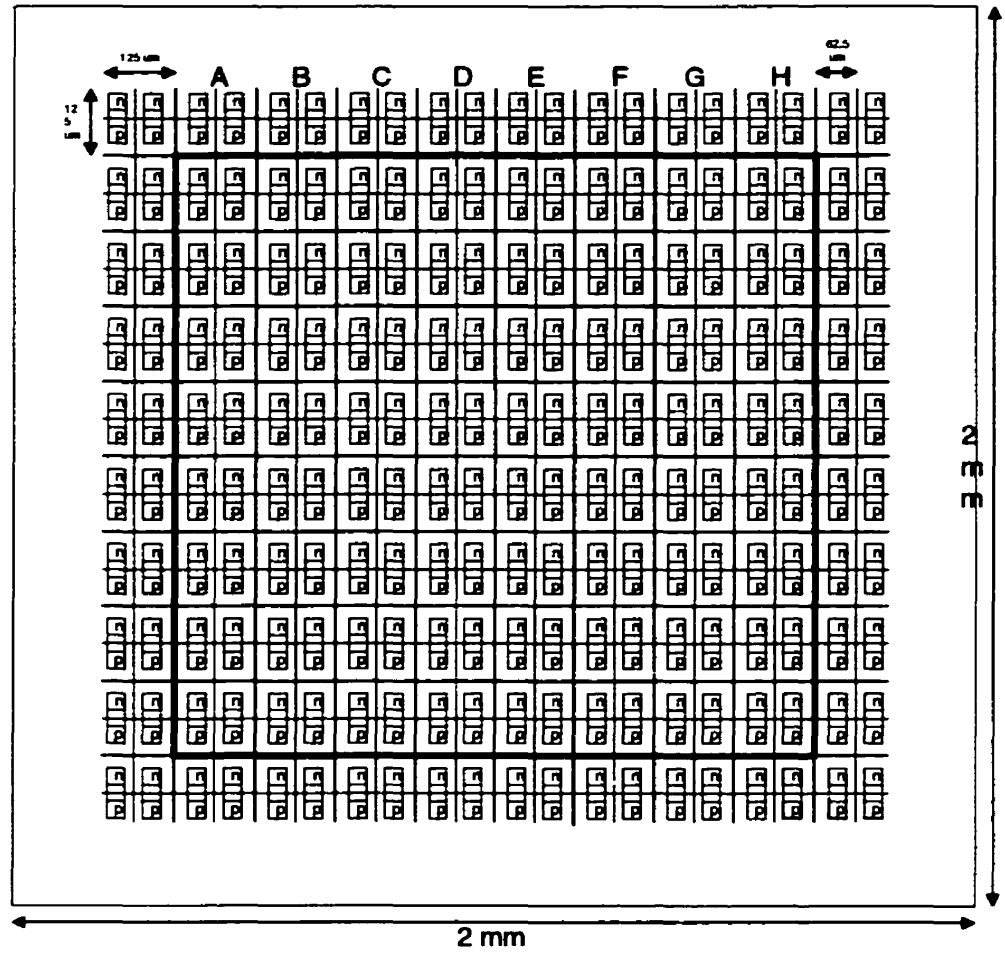

Figure 5: Array of Photodiodes on the 2 x 2 mm chip

Figure 6 shows the various electrical and optical interfaces for each bit of each channel (Smart Pixel). There is an optical input port, an optical output port, as well as an electrical input port and an electrical output port. Only one of the optical input or optical output ports can be active at any given instant. This is because both ports use the same photodiodes.

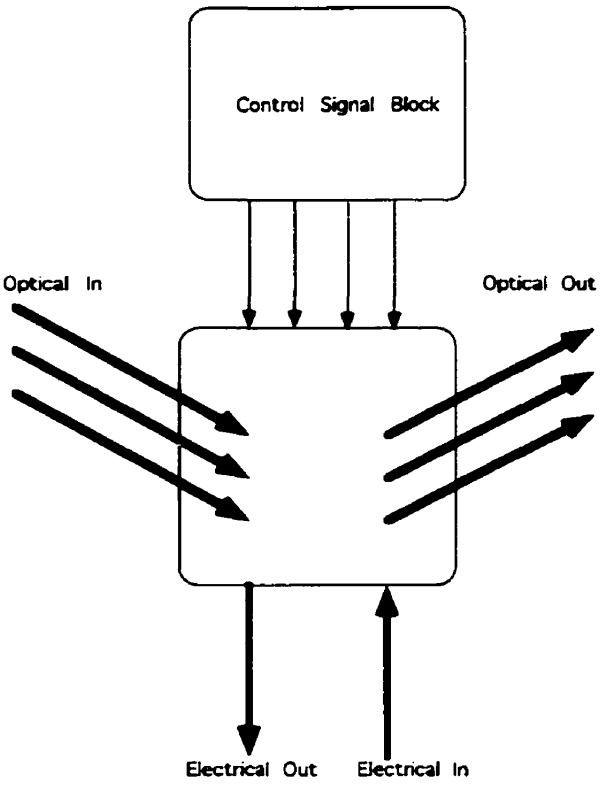

Figure 6: Electrical and Optical interfaces on each bit of each channel

The next few pages explain the operational characteristics, the logical design of the chip, and the simulation results. The simulations were carried out on the circuit as laid out in L-Edit, and then simulated using HSpice.

2.3 Operational Characteristics of the Chip

The chip was designed to have three modes of operation

1) Injection
2) Extraction
3) Pass–Through

2.3.1 Injection Mode

In the Injection mode, the 8 bit electrical signals are converted to optical and transmitted on the designated modulating channel. In this mode, only one channel can be designated as a modulator. For the chip to function in the Injection mode the *Electrical_Optical_Enable (E_O_En)* must be activated (active high). In this mode, the electrical port has the highest priority. If one of the other channels is receiving a signal, the electrical input will override it and only the 8 bit electrical input will be transmitted optically by the designated channel.

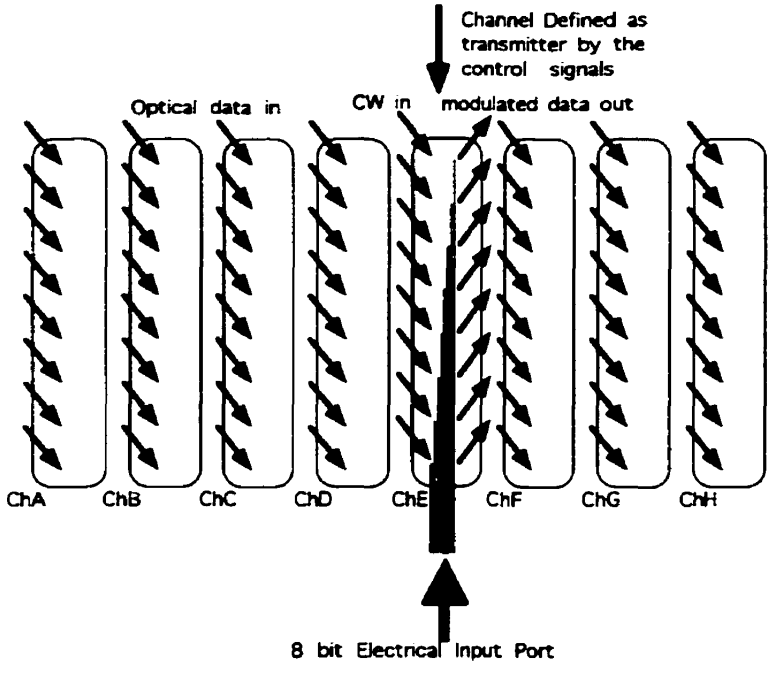

Fig 7: Injection mode of operation

2.3.2 Extraction Mode

In this mode of operation, the optical signals are extracted from the backplane and converted to electrical signals. This mode of operation requires the *Optical_Electrical_Enable (O_E_En)* signal to be activated (active high). The signal that is being received at the designated channel is transferred to the 8 bit electrical output signal lines. This is shown in Figure 8 below

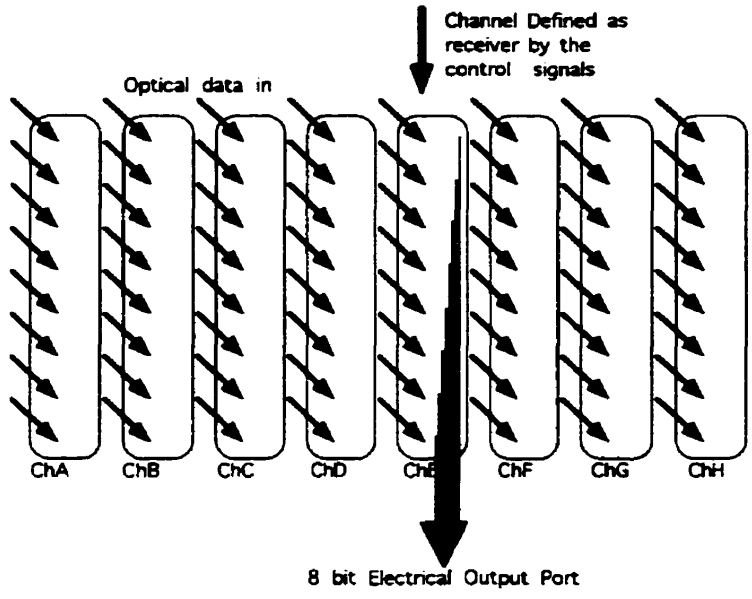

Figure 8: Extraction mode of operation

2.3.3 Pass-Through Mode

In the Pass-Through mode, the signal received at the designated channel is transmitted on the modulating channel. Any one of the eight channels can be designated as a modulating channel. When one channel is modulating, any one of the remaining channels can be the receiver.

Two other configurations are possible, in which four channels function as modulators simultaneously. When four channels are modulating the remaining four channels act as receivers. In one of these multi-channel configurations, channels A, C, E, and G are the modulators and the channels B, D, F, and H are the receivers. The signal from channel B is transmitted by channel A, from channel D by channel C, from channel F by channel E, and from channel H by channel G. This can be seen in the Figure 9 below

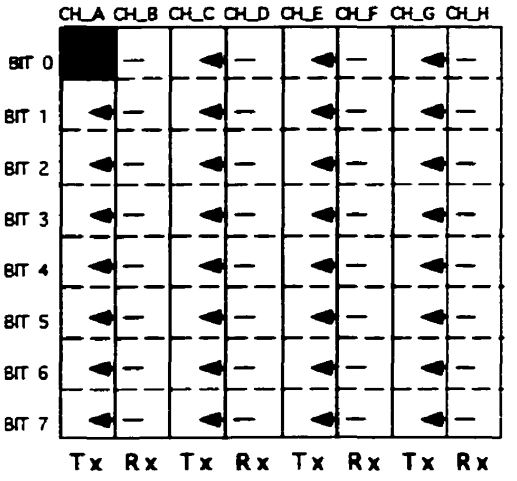

Figure 9: Four Channel Pass-Through Mode – (a)

The other multi-channel configuration is where channels A, C, E, and G are receiving channels and B, D, F, and H are the modulating channels. The signal from channel A is transmitted by channel B, from channel C by channel D, from channel E by channel F and from channel G by channel H. This can be seen in Figure 10 below.

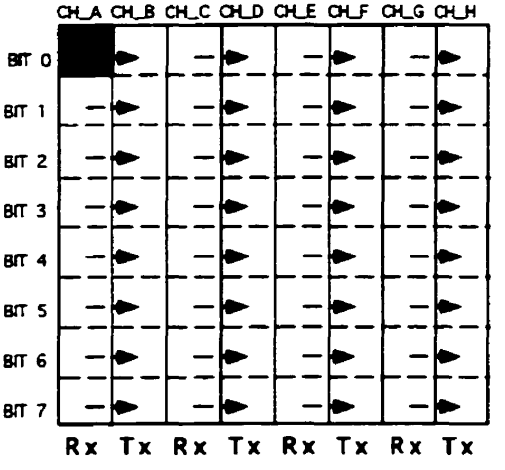

Figure 10: Four Channel Pass-Through Mode – (b)

Thus, in this mode of operation there are three sub-modes:

1) A, C, E, and G as modulators and B, D, F, and H as receivers.
2) B, D, F, and H as modulators and A, C, E, and G as receivers.
3) Any one of the channels defined as a modulator and any one of the remaining defined as a receiver.

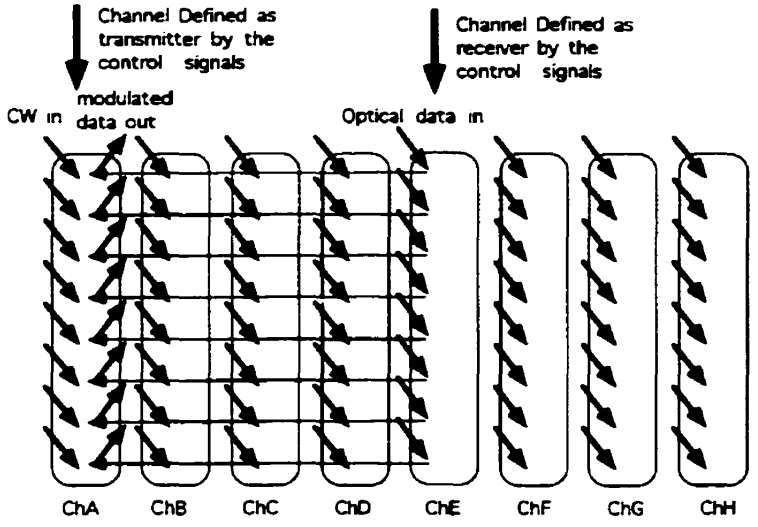

Figure 11: Pass-Through Mode of Operation

This mode of operation can also function in parallel with the extract mode. Thus we can extract the signal from the receiving channel and convert it to electrical at the same time as re-transmitting it on another channel. This is shown in Figure 12 below.

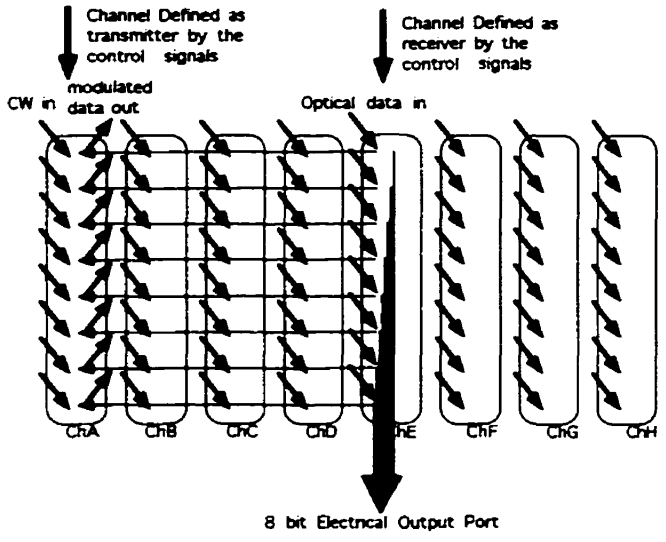

Figure 12: Pass-Though Mode of Operation in parallel with the Extract Mode

2.4 Description of the Schematic and Layout

Since this chip is an 8x8 array of identical smart pixels, the layout is made symmetrical along all possible axes of symmetry. The layout consists of one smart pixel instanced 64 times. The symmetry of the layout is shown in Figure 13.

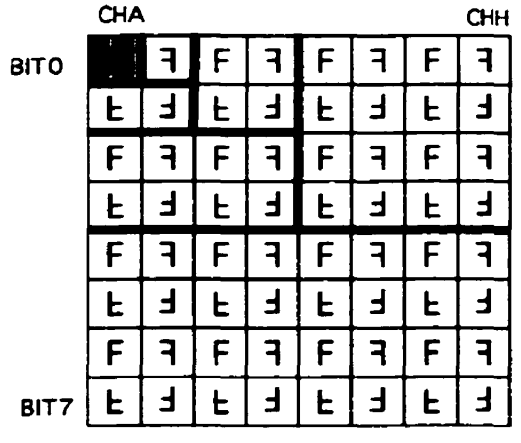

Figure 13: The axes of symmetry in the layout of the chip

The most important part of the chip is where the control signals are generated. These then have to be distributed all over the chip to ensure the correct operation of the chip. To provide easy access to the entire chip and for the routes to be symmetric, the control signals were generated in the center of the chip.

Various inputs are used for generating the control signals. Among these are the Modulator Select lines and the Receiver Select lines. These are routed horizontally across the chip from the bond pads for easy access for tapping in the central portion, wherever required by the control circuitry. Other inputs are the *Electrical_Optical_Enable (E_O_En)* and the *Optical_Electrical_Enable (O_E_En)* which are also routed across the chip.

There are seven input lines that define the configuration of the modulators and the receivers. These are the four modulator select lines (*s0, s1, s2, s3*) and the three receive select lines (*x1, x2, x3*). There are ten valid combinations for the values of modulator select lines. The first two combinations of the modulator select lines (Table 1) define the multi-channel modulation mode. The complete list of valid combinations for the modulator select lines is shown in the table below.

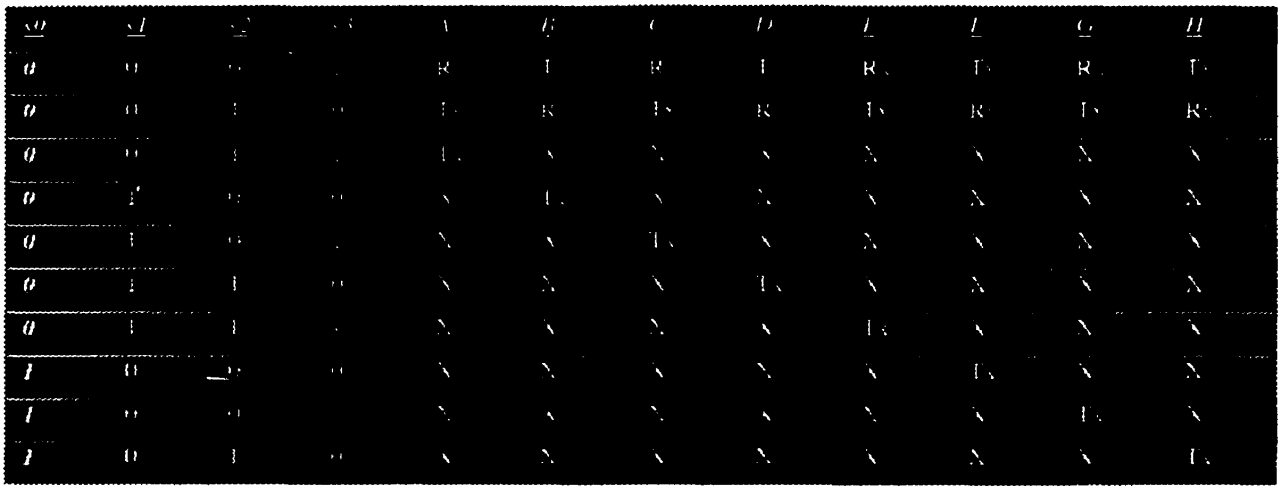

Table 1 : Definition of Channels as Modulators or Receivers

For the four-channel modes of operation, the value of the receive select lines is immaterial. The remaining eight define the modes of operation in which a single channel functions as the modulator at any particular time and one channel functions as the receiver. The table below shows the valid combinations of the receive select lines and also shows which channel is functioning as the receiver for a particular combination of the receive select lines *x1*, *x2* and *x3*.

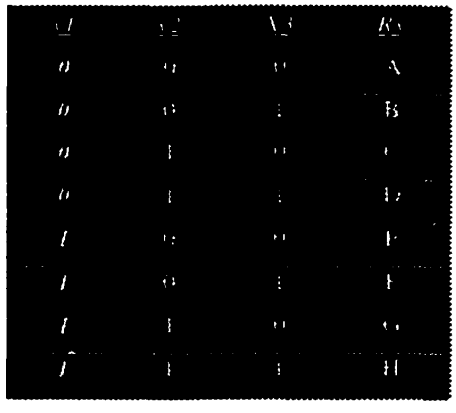

Table 2: Definition of Channels as Receivers

2.4.1 Optical Interface Module

The main difference in this design from most other chips designed in the field of Optoelectronics is that the same photodiodes function as both modulators and receivers. The advantages of this are that the number of photodiodes required for an optical backplane is reduced, and the density of smart pixels is increased for the same number of photodiodes. Hence, the density of the electrical input and output lines is also increased. The main disadvantage of this design is that it is not possible to simultaneously receive and transmit on the same channel. Thus, Pass-Through mode always needs at least two channels.

Fig 14(a) shows how the modulators and receivers are connected to the photodiodes by using a tri-state buffer for isolation. The two photodiodes are arranged in a totem pole arrangement and the central point of the two photodiodes is connected to both the receiver as well as the tri-state buffer. The output of the receiver is fed to a multiplexer that is selected when that particular channel is defined to act as a receiver, otherwise the output of the multiplexer is at ground level. Figure 14(b) and 14(c) shows how the photodiodes function in the totem pole configuration and how the detection and modulation occur for dual rail optical transmission and reception respectively.

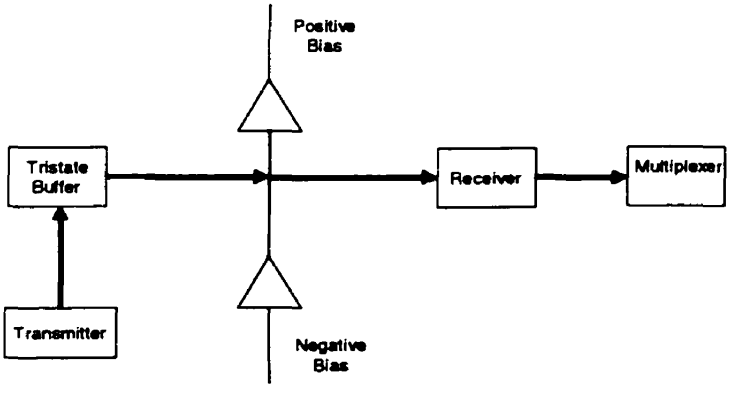

Figure 14(a): Photodiodes functioning as Modulators and Receivers

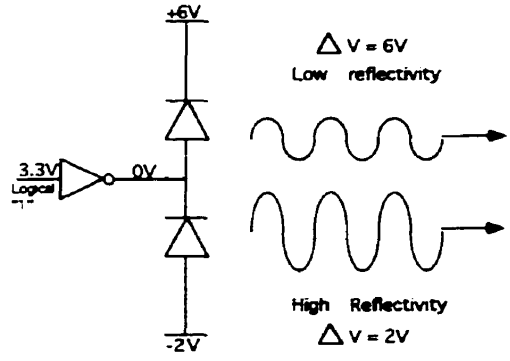

Figure 14 (b): Photodiodes as Modulators

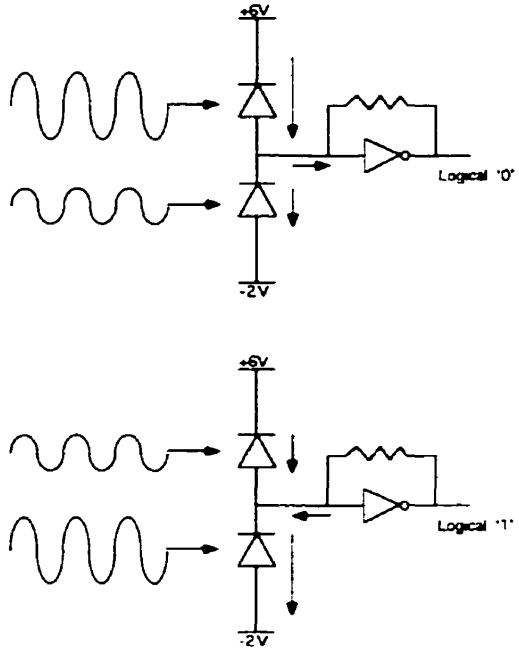

Figure 14(c): Photodiodes as Receivers

2.4.2 Receiver Design

In this chip, the receiver design used was a dual rail Trans-Impedance Amplifier (TIA). The main reason for using dual rail logic over single rail is that the bit error rate improves and the noise immunity of the circuit increases. The design and layout for this receiver were provided by Lucent Technologies for this 0.5um CMOS VLSI foundry run. The design and development of the photodetectors and the flip chip bonding to the silicon was also the responsibility of Lucent Technologies. Shown below is a schematic of the dual rail TIA receiver.

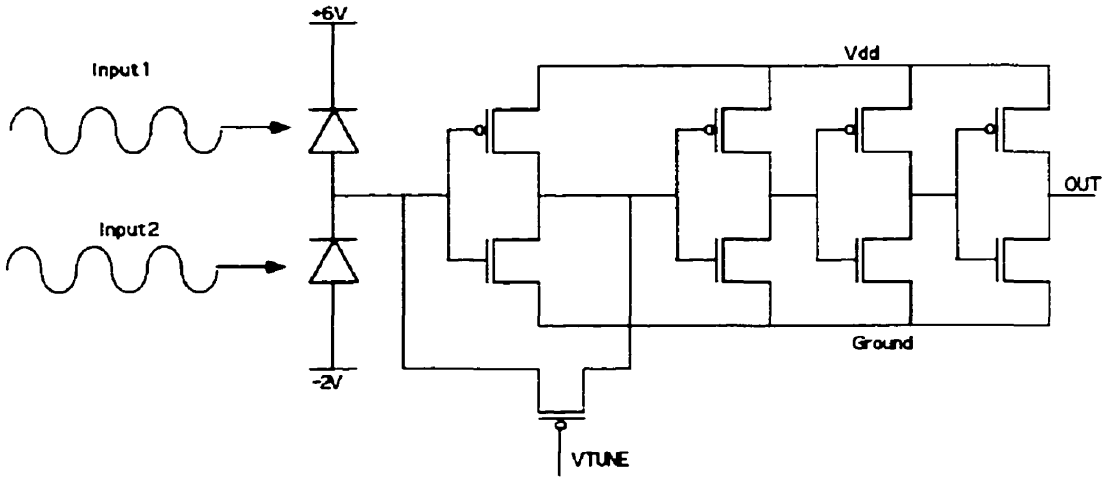

Figure 15: Block Diagram of Dual Rail Trans-impedance Amplifier Receiver

2.4.3 Selection of Receiver Channel

The control signals for designating the receiving channel are generated using the three receive select signals: *x1*, *x2* and *x3*. All of the channels which are not modulating act as receivers, and the output from the designated channel is chosen as the received signal. Figure 16 below shows the schematic for one smart pixel (one bit of each channel). This is repeated eight times in the chip for all eight bits of the received signal.

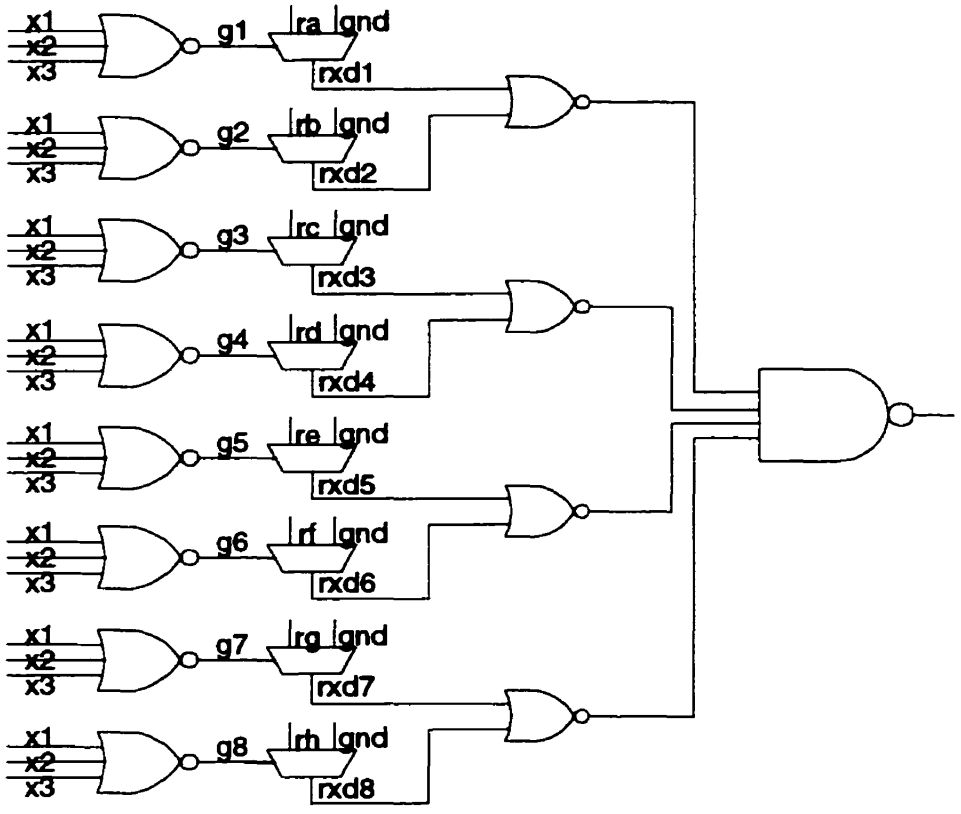

Figure 16: Selection of Receiver Channel

2.4.4 Selection of Modulator Channel

Define *MA1*, *MB1*, *MC1*, *MD1*, *ME1*, *MF1*, *MG1* and *MH1* to be the controls that select the modulating channel. These signals are active low and, the "1" at the end of each indicates that these controls are only valid for single channel. These eight control signals are generated using the four modulator select lines. For example, if channel A is to be the modulating channel i.e. *s0*, *s1*, *s2*, and *s3* are 0 0 1 1 respectively, then *MA1* should be activated (active low).

If it is a multi-channel configuration, then *MA1-MH1* signal lines are all high (inactive). Let *MA4*, *MB4*, *MC4*, *MD4*, *ME4*, *MF4*, *MG4* and

MH4 be the controls that are activated (active high) when any particular channel is defined to be a modulator (single channel or four-channel configurations). If *MA4*, *MC4*, *ME4*, and *MG4* are all active then the configuration is four modulators and four receivers. Similarly if *MB4*, *MD4*, *MF4*, and *MH4* are high, it also implies four modulators and four receivers. If only one of *MA4-MH4* is high, then its corresponding channel is the modulator. Thus if *MA1* is active (Low), *MA4* is high, but the inverse is not necessarily true. These control signals *MA4-MH4* are used to activate a tri-state buffer . This buffer sets the photodiode pair in the optical interface module to act as modulators rather than receivers.

The schematic of this portion of the control circuitry is shown below.

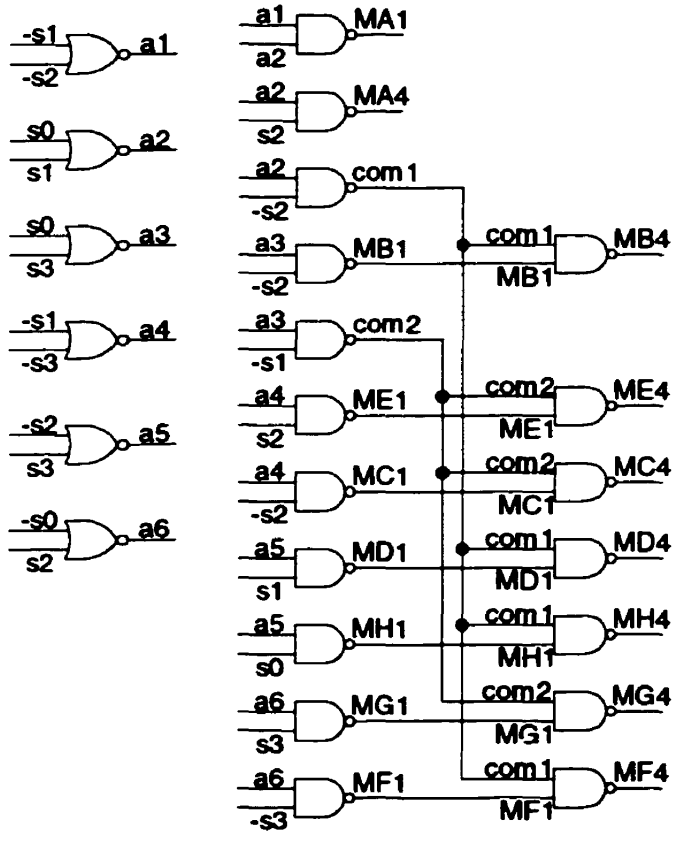

Figure 17: Selection of Modulator Channel

2.4.5 Determining the Mode of Operation

Next these MA4-MH4 are used to generate the mode select signals. These are the signals that decide among the three different configurations i.e. single channel configuration or the two four-channel configurations. *Mode_Select_1* is activated (high) if *MA4*, *MC4*, *ME4*, and *MG4* are activated and *Mode_Select_2* is activated (high) if *MB4*, *MD4*, *MF4*, and *MH4* are activated. If only one of the channels is to function as a modulator *Mode_Select_3* is activated.

If only one of *MA4*, *MC4*, *ME4*, and *MG4* is high then it is not the four-channel configuration, similarly if only one of *MB4*, *MD4*, *MF4* and *MH4* is high then it still is not the four-channel configuration. But if at least two of *MA4*, *MC4*, *ME4*, and *MG4* or *MB4*, *MD4*, *MF4* and *MH4* are high, then it must be one of the two four-channels configurations. Thus we can say that if both *MA4* and *MC4* are high we activate *Mode_Select_1* (active high). Similarly if both *MB4* and *MD4* are high we activate *Mode_Select_2* (active high). Now if both *Mode_Select_1* and *Mode_Select_2* are not activated then *Mode_Select_3* is activated. Shown below is the schematic block diagram of the implementation.

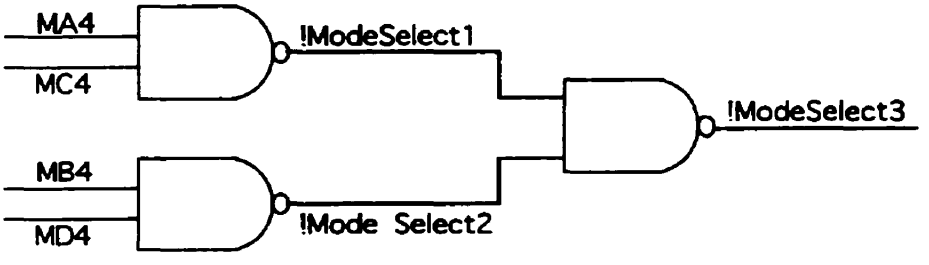

Figure 18: Controls for the Selection of the Mode of Operation

All this information is summarized in the table drawn below

Mode of operation	*MA4 MH4*	*MA1 MH1*	*Mode Select*	*E_O_En*	*O_E_En*
Injection Mode	Only one active	one active corresponding to MA1 MH1	Mode_Select_0 active	Active	Inactive
Extraction Mode	Only one active	one active corresponding to MA1 MH1 active	Mode_Select_3 active	Inactive	Active
Single-Channel Pass Through Mode	Only one active	one active corresponding to MA1 MH1 active	Mode_Select_0 active	Inactive	Don't Care
Four Channel Pass-Through Mode	Alternate four active	None Active	Mode_Select_1 or Mode_Select_2 active	Inactive	Inactive

Table 3: Summary of the Modes of Operation

2.4.6 Modes of Operation

In this section we consider the three modes of operation. Each mode has its own requirements in terms of control signals and the data. This section is divided into four parts. The first two are the Injection and the Extraction modes respectively. The third is the single channel Pass-Through and the fourth is the four-channel Pass-Through.

2.4.6.1 Injection Mode of Operation

The Injection mode is shown in Figure 19. In this mode each bit of the *Electrical_Input (ElecIn)* signal is selected by the *E_O_En* control signal and is fed to the corresponding bit of each Channel. This means that *ElecIn_1* is translated to *tae*, which is fed to the first bit of all the

eight channels, when *E_O_En* is activated.

2.4.6.2 Extraction Mode of Operation

In the Extraction mode, the data received at the designated channel is transferred to the *Electrical_Output (ElecOut)* lines by the *O_E_En* control signal. This is shown for one bit of data in the Figure 19.

2.4.6.3 Pass-Though Mode of Operation (Single Channel Configurations)

For the Pass-Through mode, the following signal conditions are required: *E_O_En* inactive, *Mode_Select_3* active and one of *MA1* to *MH1* active. This activates a control signal *t1-t8*, which is used to transfer the received signal to the appropriate modulating channel.

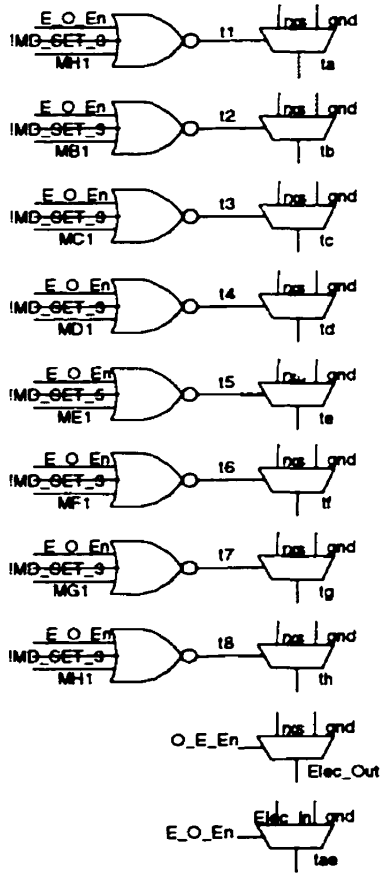

Figure 19: Block Diagram of the Pass-Through Mode of Operation (Single Channel)

2.4.6.4 Pass-Though Mode for Four-Channel Configuration

The first step is to route the received signals to the proper modulating channel in the two four-channel configurations. This is achieved by using *Mode_Select_1* and *Mode_Select_2* as shown in Figure 20.

The correct data is now routed to the input of the modulator(s). This can be any of the following three signals:

- The electrical input signal in the Injection mode of operation *(tae).*
- The received signal at the receiving channel if only one channel is receiving and only one channel is modulating *(ta – th).*
- The received signal in the case when four channels are receiving and four channels are modulating *(ta4 – th4).*

The output of this stage is what goes to the modulator.

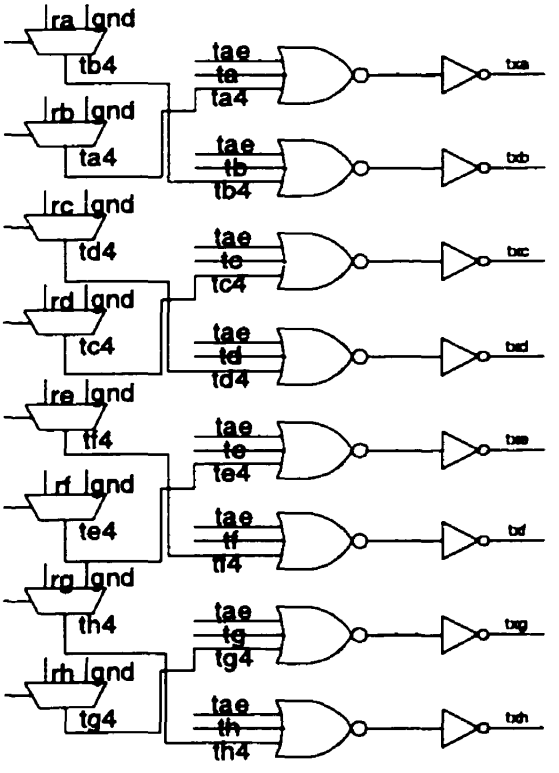

Figure 20: Block Diagram of the Pass-Through Mode of Operation (Four Channel)

2.4.7 Pin Diagram of the Chip

Shown below is the actual pin diagram of the chip. There are bond pads available for diagnostic purposes to easily test the functionality of the chip. Bond pads are also available to allow for the electrical testing of the chip.

For the electrical testing, almost the entire logical portion of the chip can be tested. However, the reconfigurable property of the chip can only be tested optically.

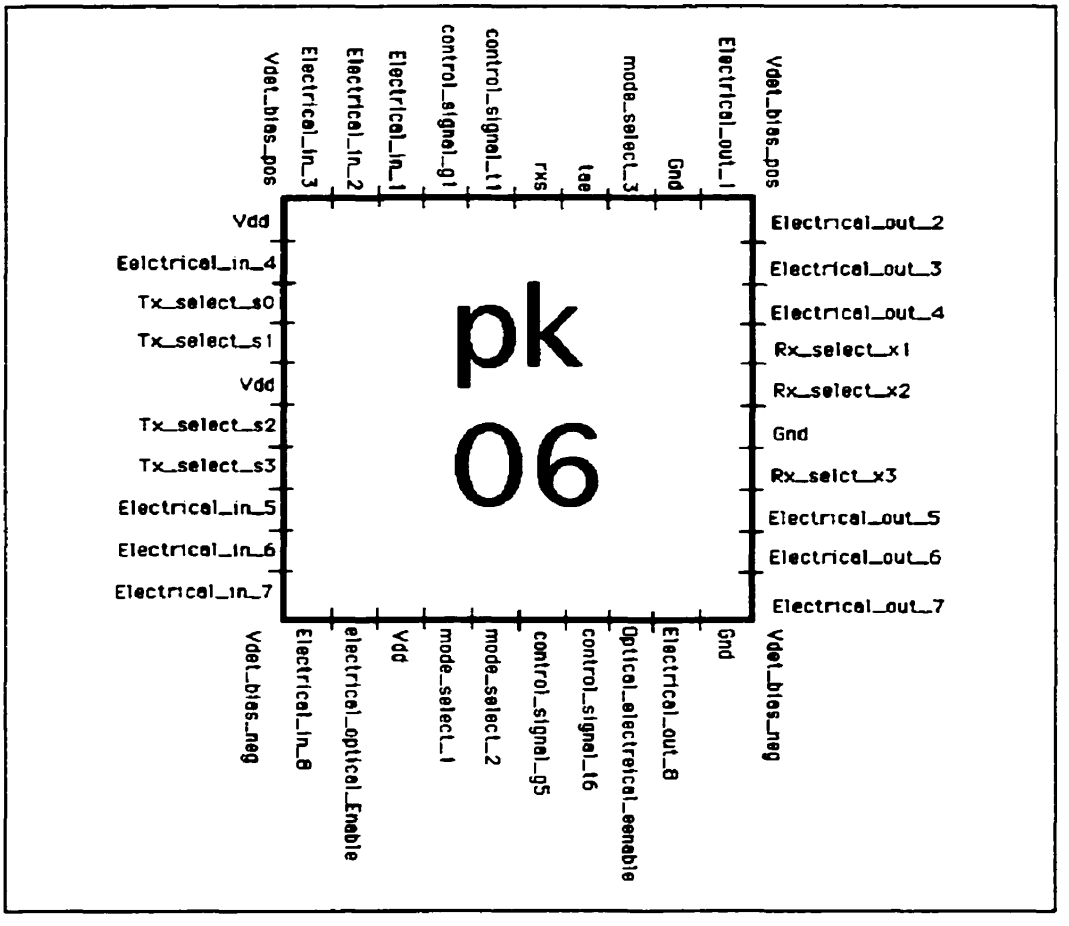

Figure 21: Pin – Diagram of the Chip

2.4.8 Bias Connections for the Photodiodes

Figure 22 below shows the bias connections for the photodetectors / modulators on the chip

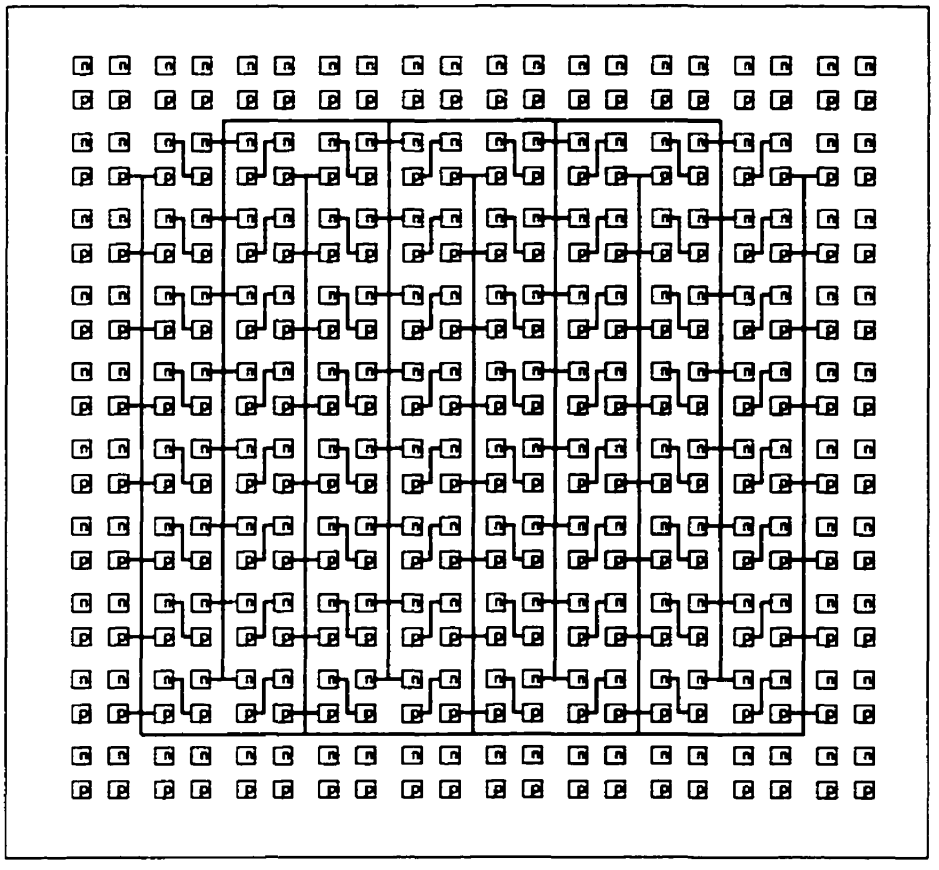

Figure 22: Bias Connections for the chip

2.5 Simulation Results

The next few pages show the simulation results of the chip after the entire chip had been designed and laid out using L-Edit. The chip was then extracted using L-Edit and the Netlist was obtained. These were input into HSpice along with the stimulus file that was created to simulate the operation of the chip.

2.5.1 Injection Mode of Operation

Figure 23 shows the simulation results of the Inject mode of operation. In this mode, the *E_O_En* is activated and the signals that are input on the eight electrical input port lines are transmitted optically from the designated modulator port. The four modulator select lines decide the modulating port. Only those combinations of the modulator select lines are valid in which only one of the channels is the modulator. Those modes in which four of the channels act as modulators cannot function in the inject configuration. In Figure 23 shown below six outputs are shown from the output of the modulator channel (Channel D in this particular example). The first two are static outputs and the next four are square waves. The simulation shows the correct functionality of this mode of operation of the chip.

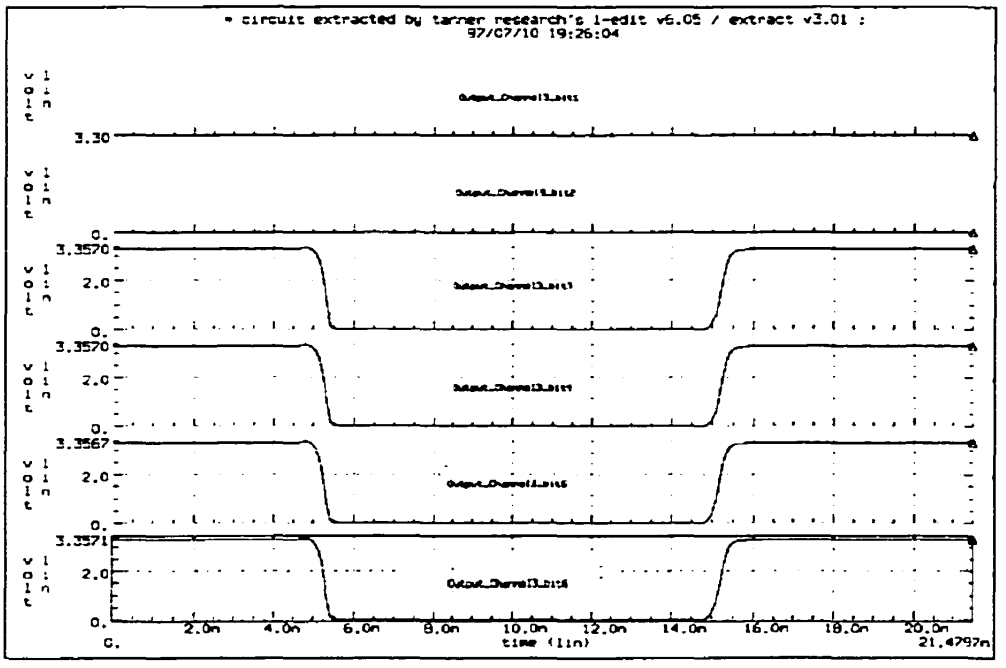

Figure 23: Simulation Results – Injection Mode of Operation

2.5.2 Extract Mode of Operation

Figure 24 shows the simulation results of the extract mode of operation. In this mode, as already explained, the *O_E_En* is activated and the receiving channel is selected by the three receive select lines. Shown below is the output of the first four bits of the electrical output port when a square wave is the stimulus applied to all the bits of the receiving channel. The square wave to the receiver consisted of current pulses of amplitude 10uA and 5uA for the high and the low signal out of the photodetectors respectively. The receiving channel was channel C. Shown also is the shape of the input pulse to the receiver.

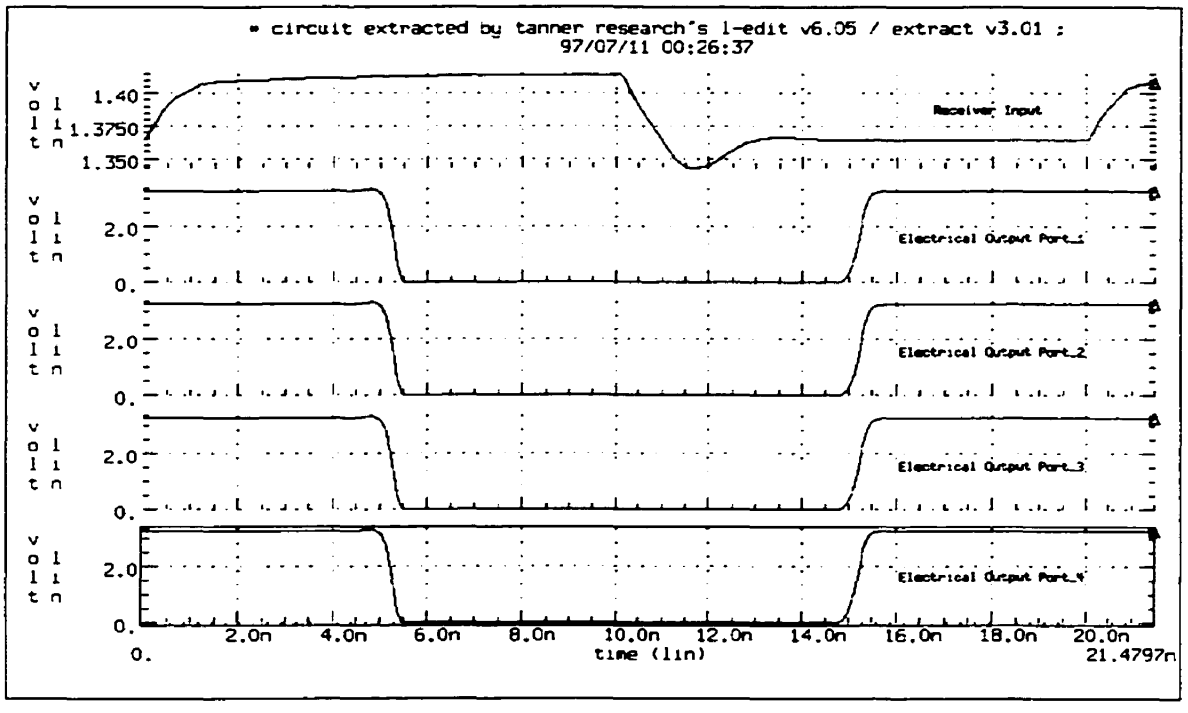

Figure 24: Simulation Results – Extraction mode of operation

2.5.3 Pass-Through Mode of Operation

2.5.3.1 Single Channel Mode

Figure 25 shows the Pass-Through mode of operation for a single channel. Thus for this particular example both *Mode_Select_1* and *Mode_Select_2* are inactive, and *Mode_Select_3* is activated. In this particular simulation the Channel D is modulating and Channel G is receiving. Figure 25 shows the input at three bits of channel G with the current levels as 10uA and 5uA as before. The output of the corresponding three bits at the modulating channel i.e. channel D are then shown.

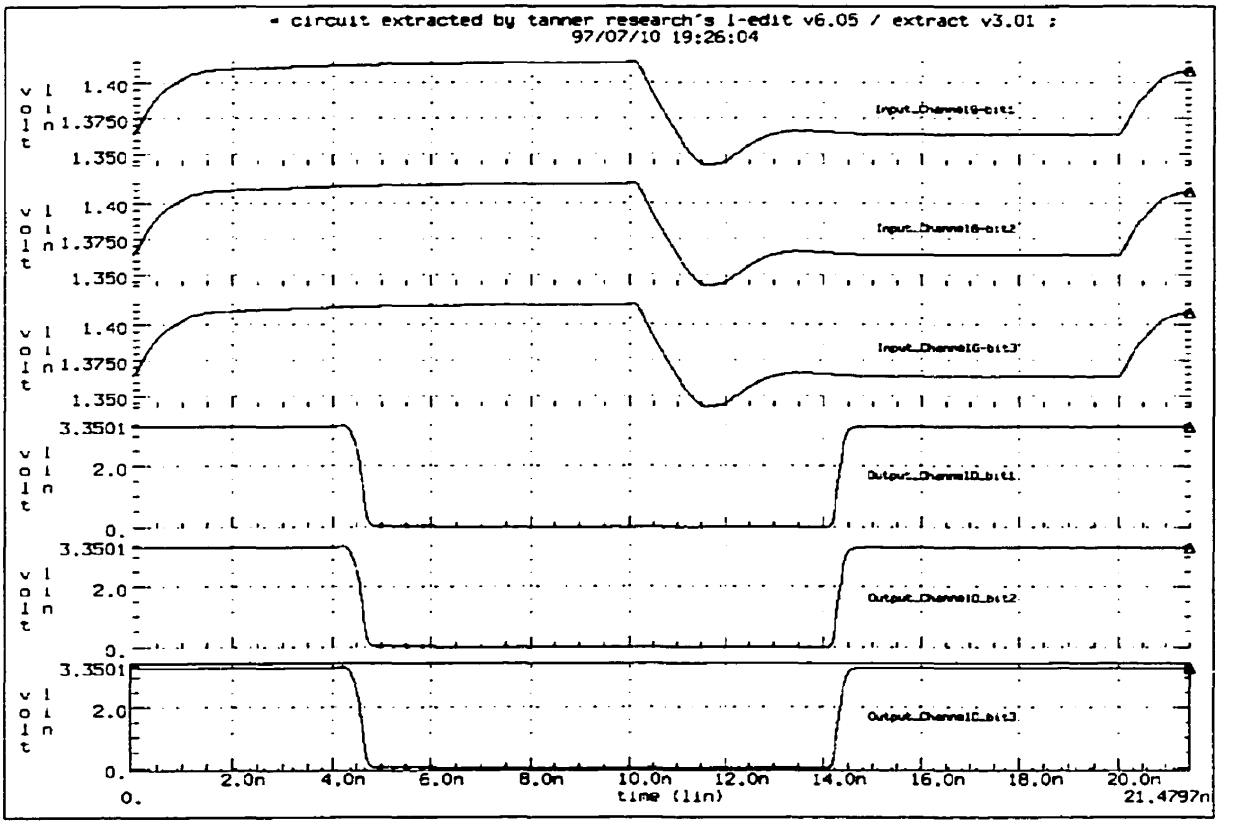

Figure 25: Simulation Results – Pass Through Mode of Operation (Single Channel)

2.5.3.2 Four-Channel Mode

Figure 26 shows the Pass-Through mode of operation. In this particular case four the channels are functioning as modulators and the remaining channels are functioning as the receivers. For this particular example, *Mode_Select_1* is activated and both *Mode_Select_2* and *Mode_Select_3* are inactive. Thus in this simulation channels A, C, E, and G are the modulators and channels B, D, F, and H are the receivers. Figure shows the input at three bits of channel B with the current levels as 10uA and 5uA as before and the output of the corresponding three bits at the modulating channel i.e. channel A. Similarly the results could be shown for the remaining pairs of modulators and receivers also.

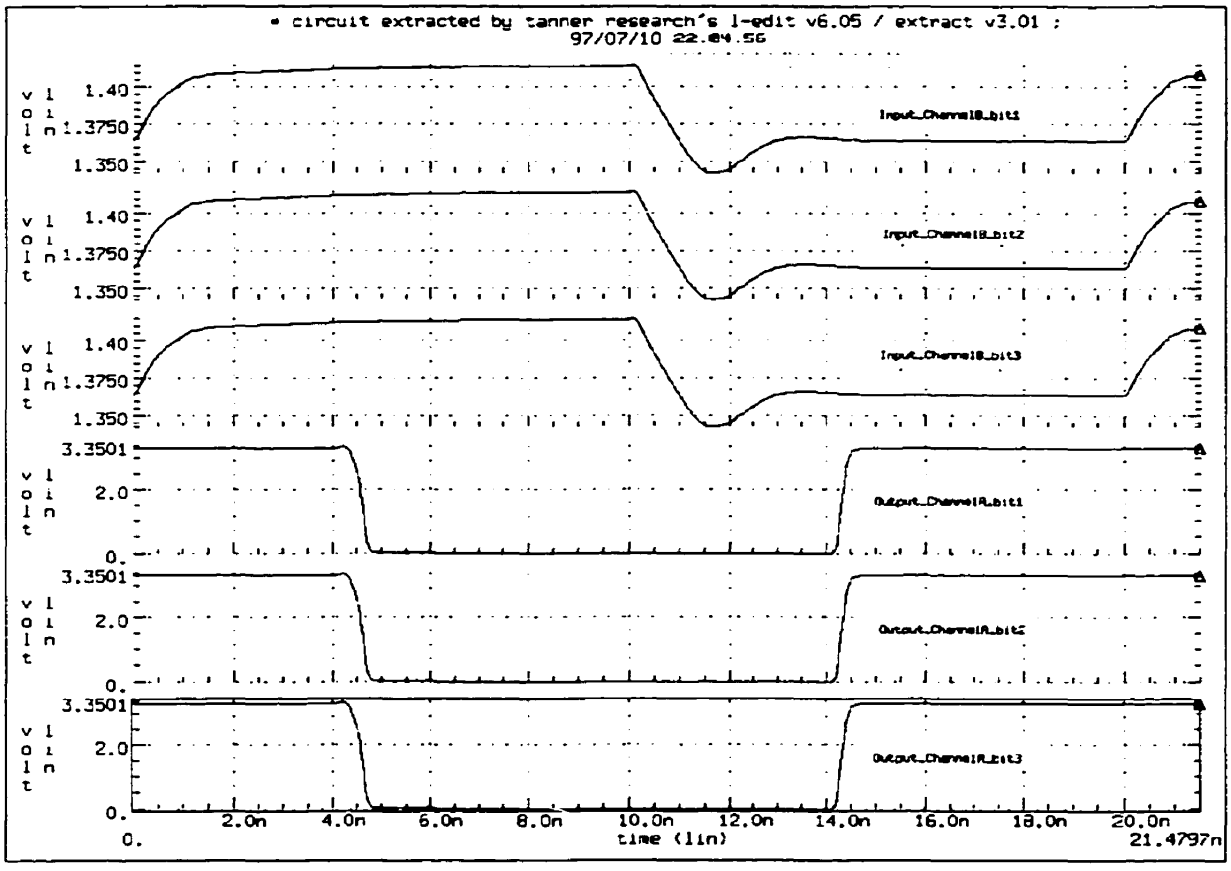

Figure 26: Simulation Results – Pass Through Mode of Operation (Four Channel (a))

2.5.3.3 Four-Channel Mode

Figure 27 shows the final configuration of the Pass-Through mode of operation. For this particular example, *Mode_Select_2* is activated and both *Mode_Select_1* and *Mode_Select_3* are inactive. Thus in this simulation channels A, C, E, and G are the receivers and channels B, D, F, and H are the modulators. Figure 27 shows the input at three bits of channel C with the current levels as 10uA and 5uA as before, and the output of the corresponding three bits at the modulating channel i.e. channel D. Similarly the results could be shown for the remaining pairs of modulators and receivers also.

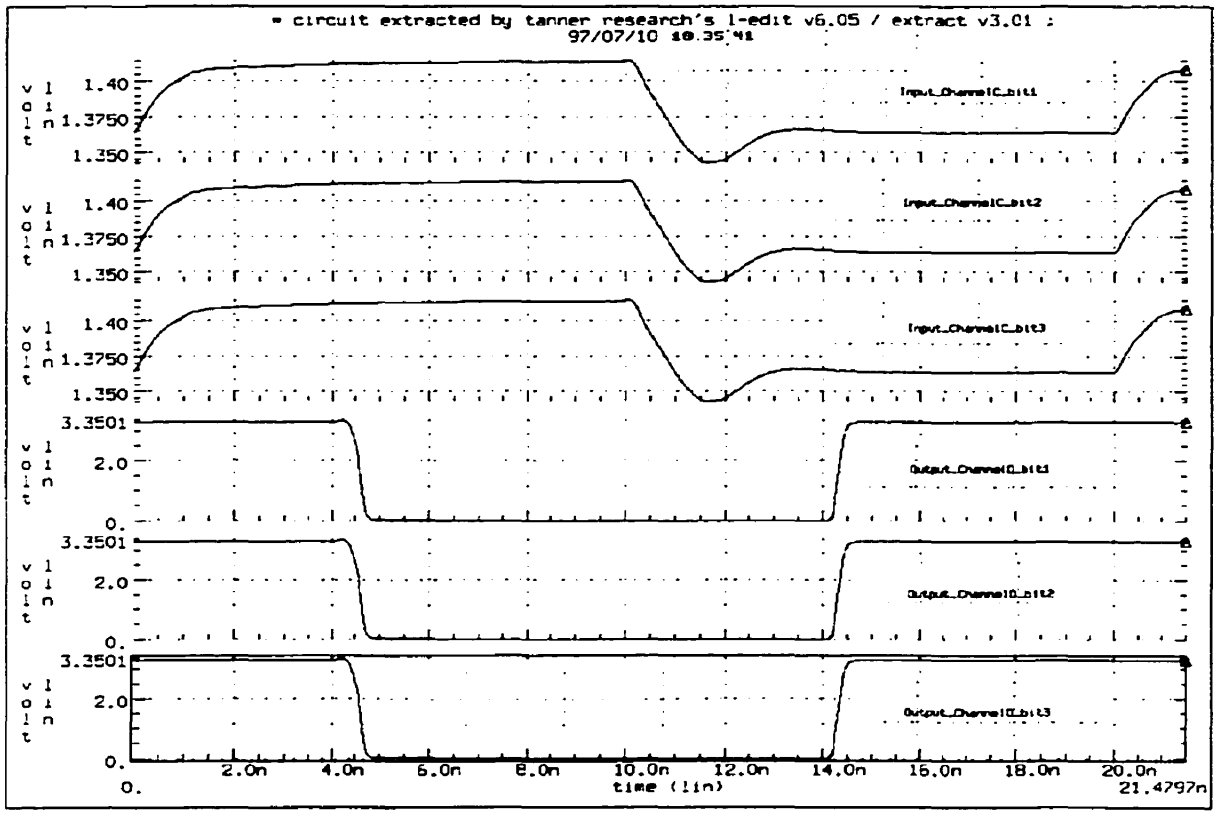

Figure 27: Simulation Results – Pass Through Mode of Operation (Four Channel (b))

2.6 Conclusions

This chapter deals with the design of a 8 x 8 array of reconfigurable smart pixels. The successful functioning if the three modes of operation i.e. the injection, the extraction and the pass through modes of operation is demonstrated by means of HSpice simulations. These SPAs can be of use in architectures like the polarization bus as already stated. The fact that the same photodiodes function as the transmitters as well as the receivers makes these SPAs unique.

Apart from the switching architectures there are a number of other issues that need to be addressed for the opto-electronic technology. Some of these issues like the power consumption reduction as well as noise reduction are addressed in the next two chapters. Chapter 2 deals with power consumption issues and discusses the use of Adiabatic CMOS for opto-electronics as a means of reducing power. Chapter 3 deals with noise reduction using optical powering instead of the conventional electrical powering.

2.7 References

1) Andrew Kirk, Frederick Matthew, Frederick Lacroix, Frank Tooley, "Demonstration of a Free-Space Optical Broadcast Network", Proceedings of the Optical Society of America Topical Meeting on Optical Computing, March 17-21, 1997.

Chapter 3: Adiabatic CMOS for Optoelectronic Technology

3.1 Introduction

With much of the research efforts in the past fifteen years directed towards increasing the speed of the digital systems, present day technologies make possible inexpensive personal workstations with sophisticated computer graphics, multimedia and video capabilities. Another significant change in the attitude of the users, is the desire to have access to this computation power at any location, without the need to be physically tethered to a wired network. This portability requirement poses severe restrictions on size. As the density and the operating speed of CMOS-VLSI chips increases, their power dissipation becomes of utmost importance since it restricts their design and performance. The dominant factor of the energy, E, dissipated in CMOS when a capacitance, C, is charged from 0 to a voltage V or discharged from V, is as follows.

$$E = \frac{1}{2} CV^2 \qquad \text{....(1)}$$

Efforts are being made to reduce this power dissipation without compromising the speed of operation of the circuit. The prevailing approach for reducing this dissipation is to scale down the power supply voltage V [1,2]. This is attractive due to its simplicity, but the threshold voltage V_t (of the MOS transistor) imposes a lower bound on the power dissipation. The power supply voltage cannot be reduced to lower than V_t. Moreover, as V approaches the threshold voltage the circuit performance becomes really poor and the bit error rate increases.

Energy recovery is another popular approach for reducing the energy dissipation [2,3,4]. In these implementations, signals and

clocks directly charge capacitive loads through charge steering logic blocks like pass gates, transmission gates etc. The energy dissipation of an energy recovery circuit when a capacitance C is charged from 0 to V Volts (or discharged from V Volts), through a series resistance R during time T and from a constant current source is given by the following equation.

$$E = \frac{RC}{T} CV^2 \qquad \ldots.(2)$$

Unlike the previous approach, energy recovery is arbitrarily scalable since the energy dissipation is proportional to the inverse of the charging time T. Theoretically, asymptotically zero energy dissipation is possible for infinitely large T. The problem with this approach is that as T increases, the speed of operation decreases.

Adiabatic CMOS (ACMOS) is a new systematic approach to reducing power dissipation in digital computer circuits by recycling a major part of the circuit energies rather than dissipating them as heat. A simple theory and practice for implementing switching circuits based on adiabatic charging is described here.

3.2 Theory of ACMOS

The major source of power dissipation in the case of optoelectronic chips is the charging of the metallic pads of the photodiodes. They have large capacitances (of a few 10s of pF), depending on their size (almost 100uF in the case of this chip). This design has tried to demonstrate a driver capable of significant reduction in power dissipation, for given values of voltage swing (3.3 V in this case), load capacitance and switching frequency, without performance loss. This is accomplished by using stepwise charging, an inductor free form of adiabatic charging [5,6,7].

3.1.1 Stepwise Charging

Since the charge to be transferred is given by the voltage swing and the load capacitance, the only way to reduce the dissipation while keeping the voltage swing and load constant, is to reduce the average voltage drop, $\bar{v}$. To achieve the entire voltage swing, the charging and discharging process is divided into a number of smaller voltage steps. Thus the charging time of the load capacitor is increased since charging is performed in a number of steps (of smaller potential differences), rather than a single step of the complete voltage swing (as in the conventional case). This is the principle of adiabatic switching, reduced power dissipation at the cost of decreased switching speed but without changing the voltage swing. Fig 28 shows a capacitance being charged from a bank of voltage supplies with uniform distributed voltages.

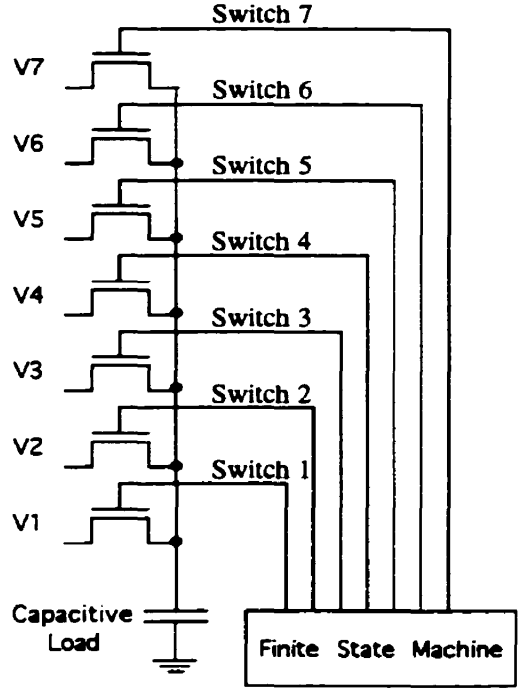

Figure 28: Block Diagram of Adiabatic CMOS

To charge a load, each of the N transistors ($Switch_1$ to $Switch_N$) is switched briefly in ascending order, until the load has reached the corresponding voltage. A bank of N voltage supplies with evenly distributed voltages, V_1 through V_N, are connected to the load in succession (by closing $Switch_1$, opening $Switch_1$ and closing $Switch_2$ etc). Each supply then injects a charge packet of size q_{int}:

$$q_{int} = C_L\left(V_i - V_{i-1}\right) \qquad \text{....(3)}$$

During charging, each supply except Ground injects one charge packet to the load. During discharging, each supply except V_N receives one charge packet, and one packet is dumped to ground. V_{N-1} through V_1 are switched in the same way, and then $Switch_0$ is closed, connecting the output to ground. The net effect over one complete cycle is to inject one packet at voltage V_N, and remove one packet at voltage 0. Since the initial and final states are identical, the total dissipated energy for a complete cycle of charging and discharging is equal to the net injected energy:

$$E_{diss} = E_{inj} = q_{int}V = \left(C_L V^2\right)/N \qquad \text{....(4)}$$

Charging through N steps instead of a single step reduces the energy dissipation by a factor of N. The decrease comes from a reduction of the voltage drop across the switch through which the charge flows, which is now on average a factor N smaller than in the conventional case.

For practical reasons, the use of multiple supply voltages for a chip is undesirable. Fortunately, capacitors can be substituted for all but one of the supplies. Also, there is no need to maintain the proper voltages on the capacitors because over time, they will automatically converge to the correct voltages. Thus, no additional circuitry is required to maintain the circuits' functionality. The circuit is self-stabilizing. Only one power supply is needed for this circuit's operation (just as in the conventional

case). The circuit for this is shown in figure 29.

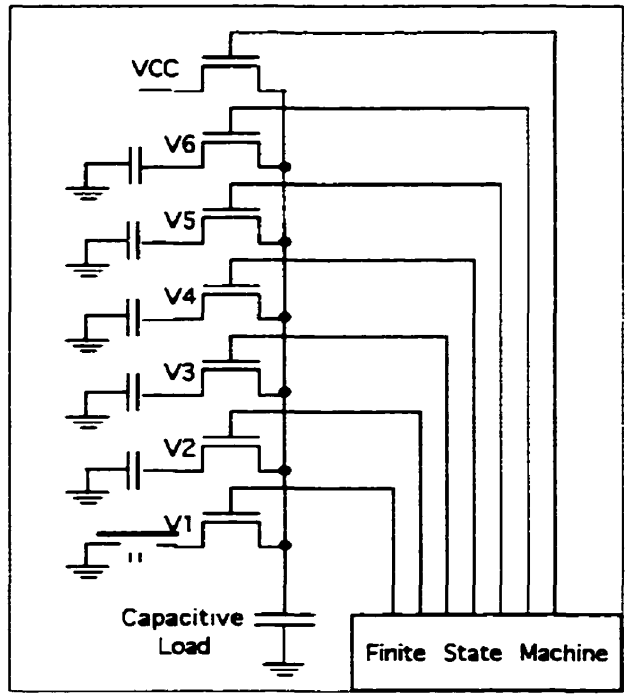

Figure 29: Block Diagram of Adiabatic CMOS with capacitors for storing charge

3.1.2 Power Saving Analysis for ACMOS

Equation 4 above appears to predict that the dissipation decreases monotonically with increasing N. However, N cannot be made very large, because all the switches need to be operated and this causes power dissipation. For a given total charging time (depending upon the maximum speed of operation), there is an optimal number of steps which leads to minimum power dissipation. The next step is to determine this optimal N. The energy needed to drive the gates of the N-transistor switches is:

$$E_{sw} = \left(\sum_{i=1}^{N} C_i + \sum_{i=0}^{N-1} C_i \right) V^2$$

....(5)

Allotting each step one Nth of the total charging time T. Then:

$$T/N = mR_i C_L \qquad \text{....(6)}$$

Where m is the number of RC time constants spent waiting for each charging step to complete. If m is chosen too small, there will be a significant voltage across a switch when the next switch is to take over. Hence there is an increase in the average voltage across each switch and therefore the dissipation increases. If on the other hand m is chosen unnecessarily large, time is wasted that could have been otherwise used. When m is 2.5 each step is allowed to charge to within 90% of its final value. Suitable values range from 2 to 4. All the switch devices should have equal on-resistance i.e. $R_i = R_{sw}$.

$$\rho_i = R_i C_i \qquad \text{....(7)}$$

Where ρ_i is the quality measure of the i_{th} switch and is the RC time constant of the switch. It is a function of i, since the bulk to channel and gate to channel voltages are different for different switches. This gives

$$E_{sw} = \frac{Nm}{T}\left(\sum_{i=1}^{N} \rho_i + \sum_{i=0}^{N-1} \rho_i\right) C_L V^2 \qquad \text{....(8)}$$

$$\bar{\rho} = \frac{1}{2N}\left(\sum_{i=1}^{N} \rho_i + \sum_{i=0}^{N-1} \rho_i\right) \qquad \text{....(9)}$$

Let, $\bar{\rho}$ be the weighted average for all the switches. If N is large, $\bar{\rho}$ is close to the unweighted average over the entire voltage range.

$$E_{tot} = \left(\frac{1}{N} + 2N^2 m \frac{\bar{\rho}}{T}\right) C_L V^2 \qquad \text{....(10)}$$

The N that minimizes this total energy is given by

$$N_{opt} = \sqrt[3]{\frac{T}{4m\bar{\rho}}} \qquad \text{....(11)}$$

Using equation 11, taking m to be 2 (i.e. time spent waiting for the charging to complete is equal to twice the R_iC_L time constant) and the maximum speed of operation as 500 MHz we can calculate the value of N. It came out to be 6 given the R_iC_i time constant of the switches to be 100ps. In this chip three circuits were laid out having 5, 6 and 7 stages respectively. This was done to be able to experiment with an optimal or near optimal number of stages and determine the difference in the power saving. It will also help to determine the effect on overhead costs (power and area) when the number of stages is no longer optimal.

The energy dissipation corresponding to optimal number of stages is given by the following equation

$$E_{opt} = \frac{3}{2}\sqrt[3]{\frac{4m\bar{\rho}}{T}}C_L V^2 \qquad \text{....(12)}$$

From this expression, the energy savings can be easily calculated.

The total energy present in an energy recycling system exceeds the energy dissipated per operation (otherwise there would be no energy to recover upon completion). All of this energy must initially be delivered to the system to make subsequent low power operation possible. Thus, ACMOS systems require an initial energy investment, *startup energy*, to reach the steady state where operations can be efficiently carried out. The startup energy receives considerably less attention than the energy dissipated during continuous operation. This is probably because the steady state energy dissipation is continuous, whereas the startup energy is only a single burst of energy consumed at system initialization. For a stepwise charger having N stages consisting of a load capacitance of C_L, and N-1 capacitors with identical capacitance C_T, the startup

energy can be shown to be approximately given by the following equation [6]

$$E_{startup} = \frac{N(N-1)}{\pi^2} C_T V^2 \qquad \text{....(13)}$$

This expression ignores the energy needed to control the MOS switches and it grows as the square of N. Therefore in ACMOS, any energy dissipation reduction requires a corresponding quadratic increase in the startup energy. This illustrates the problem of optimizing both the efficiency of initialization and the operation of the stepwise charger. Although this particular design does help to reduce the steady state power dissipation in any circuit, the startup power dissipation might be considerably higher. Other disadvantages of this technique are that it requires a voltage swing of at least twice the threshold voltage of a MOS transistor. Also, extra capacitors are charged and discharged in every cycle and the switching circuitry takes up expensive silicon space. Thus, ACMOS becomes economical when the same switching structure is used with a large number of highly capacitive loads to achieve power saving.

3.3 Design and description of the schematic

In the next few sections, using block diagrams of the design, the complete functionality of the 1x1 mm optoelectronic chip is described. This is actually the bottom right quarter of a 2x2 mm chip fabricated using 0.5um HPCMOS VLSI technology from Mosis. The purpose of this chip was to demonstrate the application of ACMOS to optoelectronics for charging and discharging the capacitance of the photodetectors.

As already described, for the charging of the capacitive load the requirement is to switch on and off N transistors sequentially. The voltages applied to their gates control these transistors. The drains of all the transistors are connected to one end of the capacitive load. The other

end of the capacitive load is at a potential of 0 V. The sources of these transistors are maintained at different voltages and control the voltage drop across the capacitve load when a particular transistor is turned on. The design of this chip involves switching N number of transistors in a particular order when the input was Logical 1 and in the reverse order when the input is a Logical 0. Also if the input is a Logical 1 and the previous input was also Logical 1, then none of the transistors should be switched. Similarly, if the input is a Logical 0 and previous output was a Logical 0, no switching is required. A Finite State Machine was used to generate these control signals.

3.3.1 Generating the signals for sequentially activating N-transistors

In the design of the finite state machine, the initial step was to generate a set of signals that would enable the sequential switching of the transistors. This was accomplished by using D Flip Flops with the *set* and *reset* options connected together in a ring configuration. A single pulse, double the width of a clock pulse, is generated by using one of the D Flip Flops and then circulated among the remaining N-1 D Flip Flops. These then form the signals that can be used to sequentially trigger N transistors. The ring arrangement is shown in Figure 30.

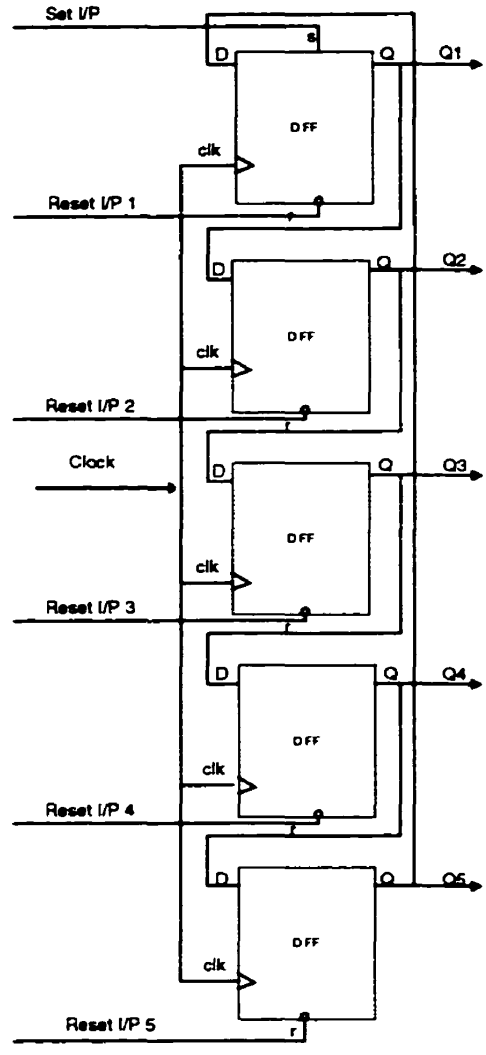

Figure 30: Ring Oscillator for Generating Trigger Pulses for ACMOS

3.3.2 Triggers for Sequential Operation

If Q1 to Q5 are used for sequentially switching the transistors such that an ascending voltage appears at the capacitive load with each successive transistor, the effect is of charging the capacitive load. If Q1 to Q5 are used for sequentially switching the transistors such that a descending voltage appears at the capacitive load with each successive transistor, the effect is of discharging the capacitve load. The values of the input signal and the capacitve load node are used to determine if

charging or discharging should take place. The block diagram for this is shown in the figure below.

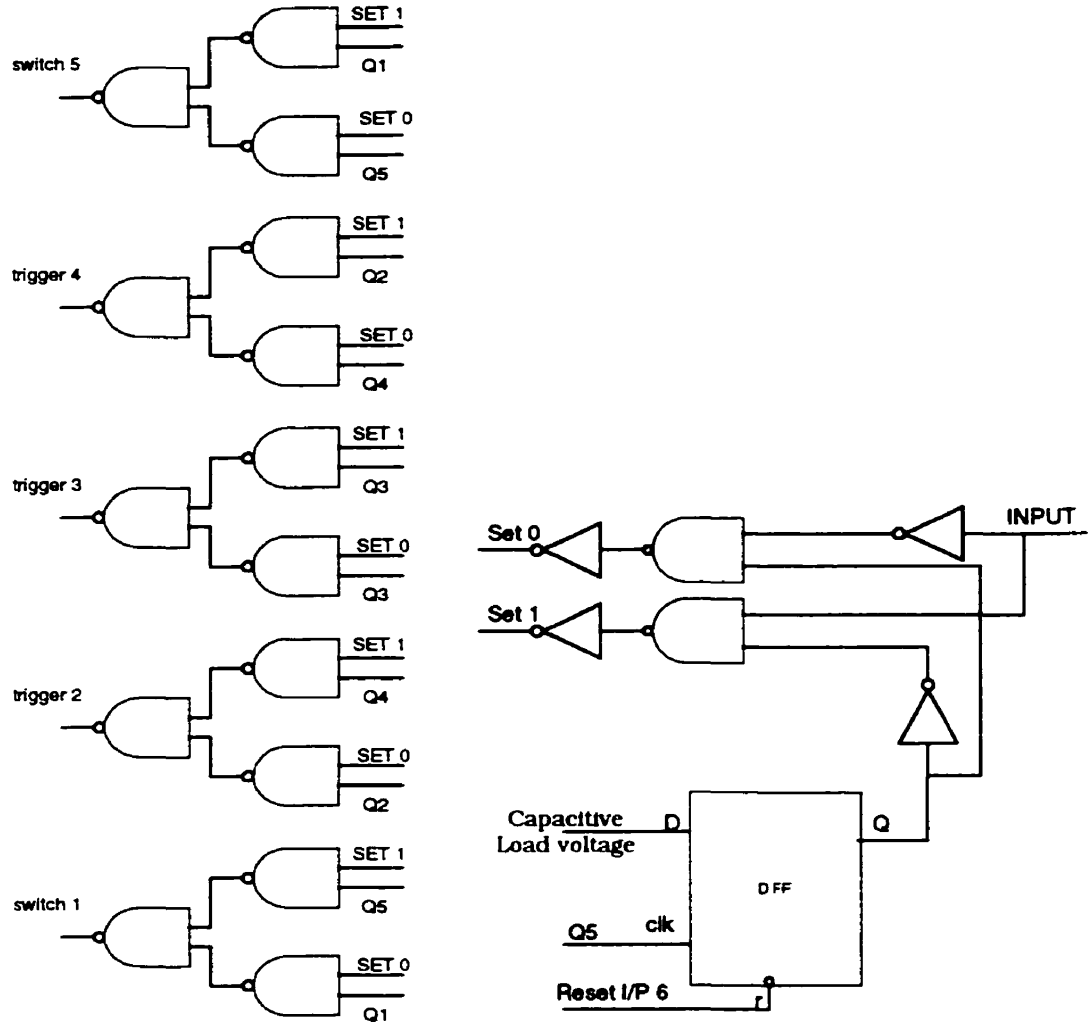

Figure 31: Trigger Pulses for charging and discharging of the Load Capacitance

There is also a provision made for checking the voltage at the capacitive load node. If it is the same as the input, then there is no switching during that particular "data bit". This is an additional power saving measure. It does not cause much increase in power to incorporate this saving measure since it only needs an AND gate. The rest of the

circuitry is common with the input and the trigger generation.

There are switches (Direct 0 and Direct 1) provided so that the load can be directly connected to the Vcc and ground rails without the intermediate switching architecture. Thus, the power consumption could be compared with and without the ACMOS power saving structure. This is shown in the figure shown below.

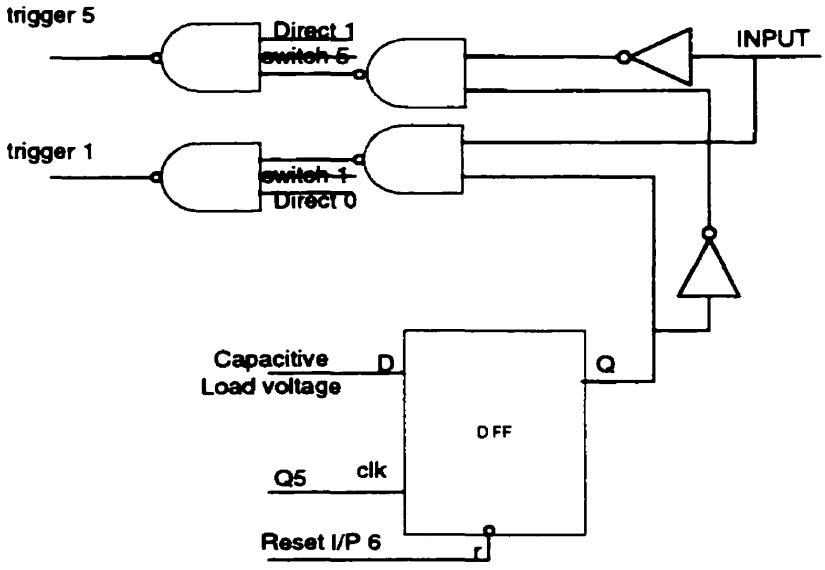

Figure 32: Additional Power saving Features on the ACMOS Chip

3.4 Layout of the Optoelectronic Chip

There were three ACMOS power saving experimental structures on the chip having 5, 6 and 7 stages respectively. The reason for putting three structures was to test the choice of the optimal number of stages (calculated to be 6 for charging a 100pf load). Also, this was a means of verifying the effect of the number of stages on the total power saving. Because of the limited number of bond pads, the three structures shared all the input lines. All three structures are simultaneously in operation. Also, the number of test points that could be incorporated was limited. To overcome this, five bond pads were used to monitor 16 outputs by

using a 16 x 1 multiplexer with four select lines. These select lines are the S0, S1, S2, and S3. The organization of the multiplexer is shown in the figure below:

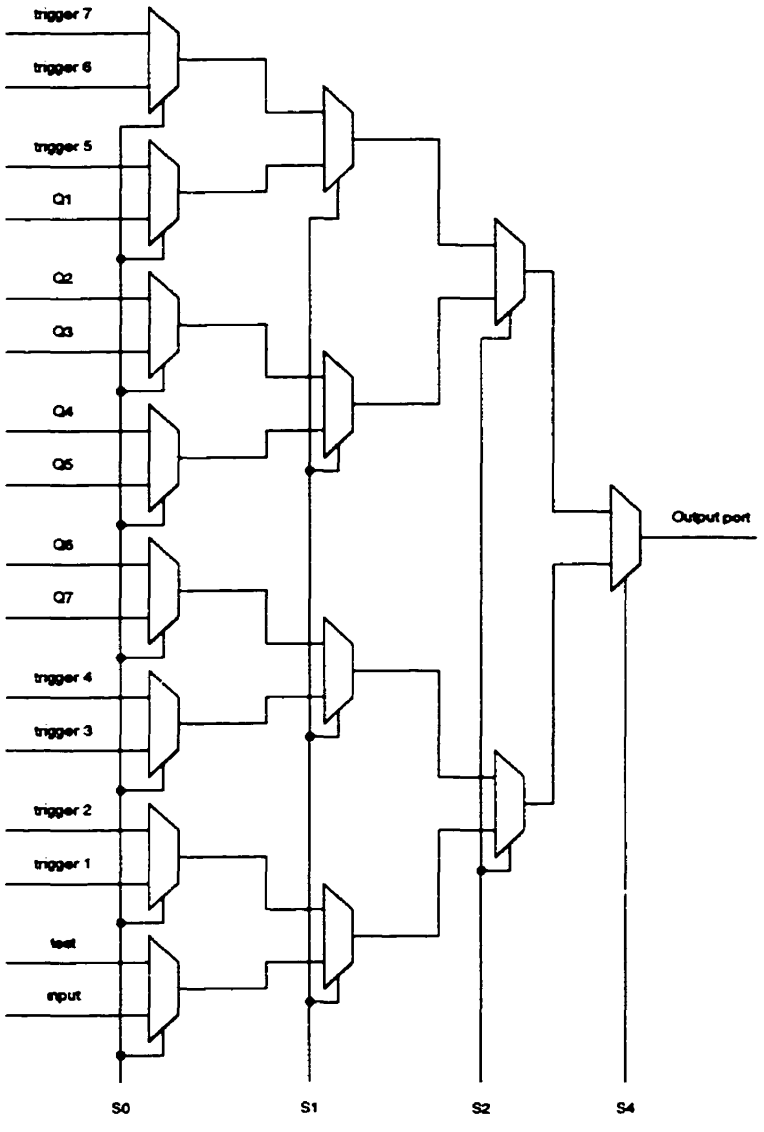

Figure 33: Multiplexer for Electrical and Optical Testing of the Chip

3.5 Pin Diagram of the Chip

Shown in the figure below is a pinout of the chip.

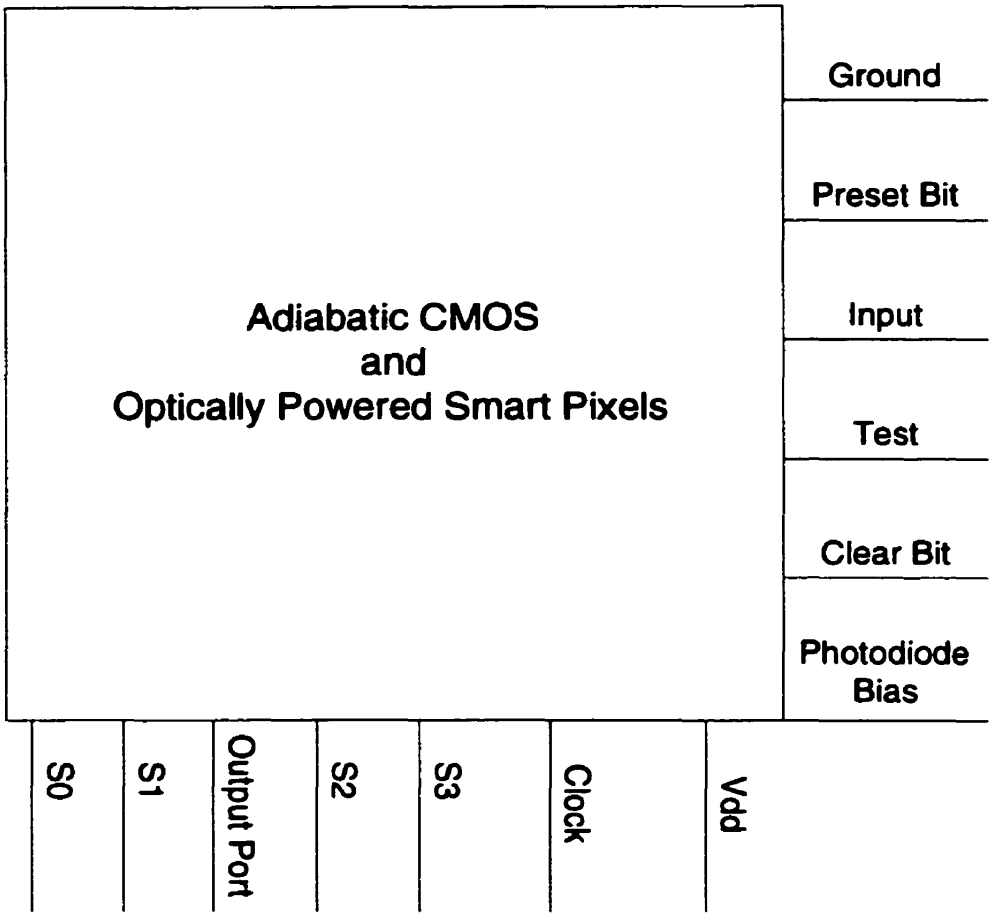

Figure 34: Pin – Diagram of the ACMOS Chip

3.6 Simulation Results:

The next few pages deal with the simulation results. These results demonstrate the correct operation of the schematic that was laid out using L-Edit and simulated using HSpice.

Shown in the figure below is the simulation result for the generation of the triggering pulses for a seven stage ACMOS. The fifth and the seventh stages are shown simultaneously.

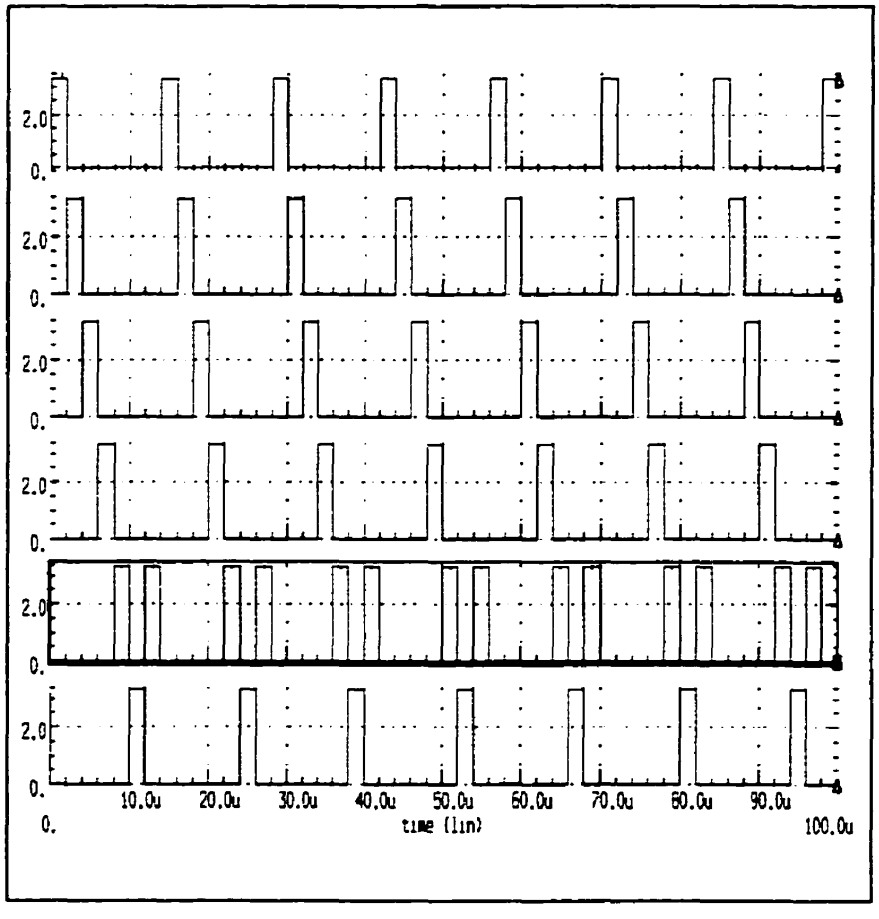

Figure 35: Trigger pulses at the output of the Ring Oscillator

The next figure shows the actual triggering pulses in sequence for

a charging step followed by a discharging step and then again by a charging step.

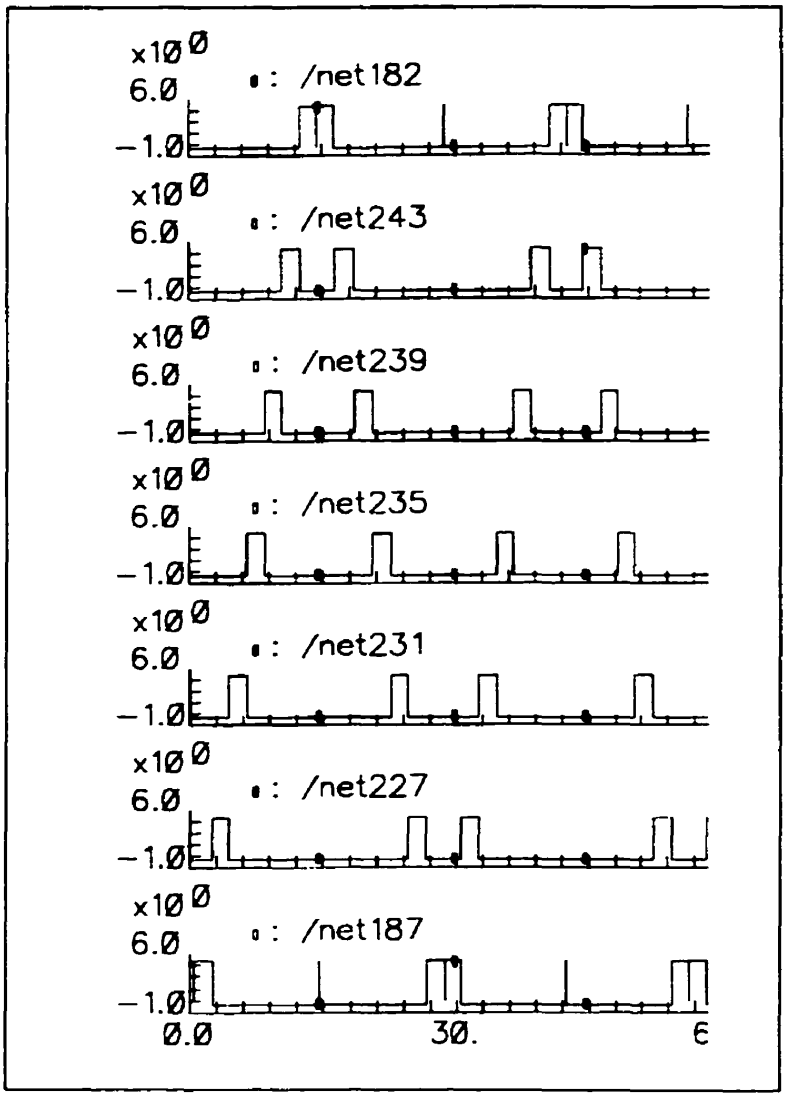

Figure 36: Charging and Discharging sequence of pulses

The next two results demonstrate the successful operation of the circuit. These are the simulation results at the capacitve load node. The first result is with a six step structure and the input is alternating ones and zeros.

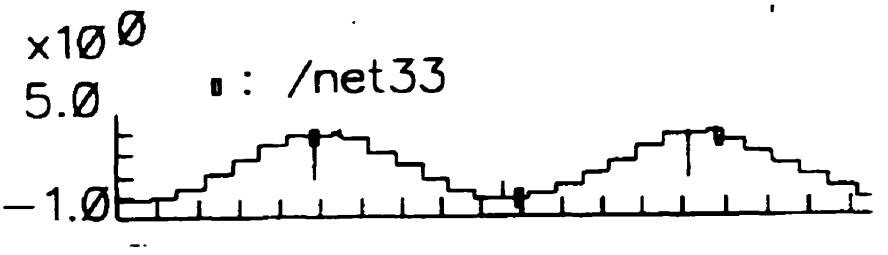

Figure 37: Charging and Discharging of the Load Capacitance

The second result shows the simulation result for the six step ACMOS but with the inputs as 1100 at the four rising edges of the clock respectively. Thus the simulation result shows how charging, no switching, discharging and then no switching occurs, as the input changes.

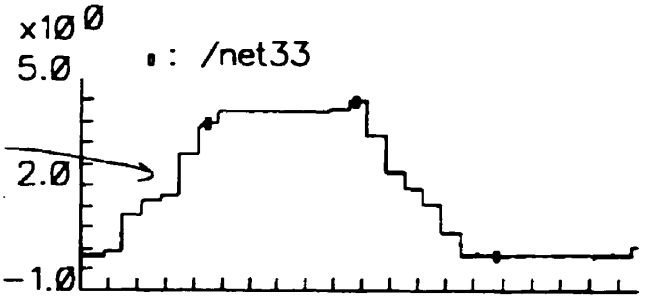

Figure 38: Charging and Discharging for consecutive ones and zeroes at the input

The next figure demonstrates how the capacitors in the structures acquire steady potentials immediately after startup. Initially there is no potential drop across them but they build up a potential that attains steady state.

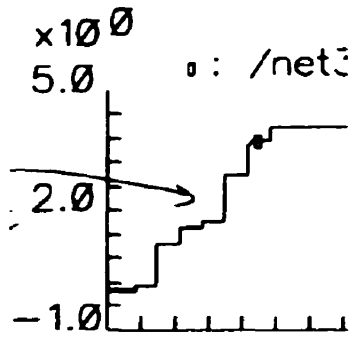

Figure 39: Startup procedure before the steady state is reached

3.7 Conclusion and Future Work

We have successfully shown using HSPICE simulation that this circuit works as far as charging and discharging of the capacitive load is considered. Experimentation with the actual chip (which is being fabricated at the present time) will tell if the ACMOS technology can help save power for optoelectronic chips. ACMOS has already proved to be a successful technique for power saving in the case of driving highly capacitive off chip load capacitances [8]. Its usefulness for the optoelectronic technology has yet to be determined. That was the reason for incorporating these test structures in this chip.

The next few paragraphs outline a testing procedure for the chip. Since the chip was designed for the ACMOS structures to drive optoelectronic modulators, one continuous wave beam is required to be incident on the modulator photodiode. This continuous wave is then modulated and can be detected to verify that the beam has been intensity modulated in accordance with the input signal. Thus, the first test would be to test the functionality of the circuit and see if the circuit functions as a modulator or not. To accomplish this, various input bond pads have to be set to proper values. These include the supply pads Vdd, Ground

and the Photodiode bias. There are a 16 possible outputs from the multiplexer (as already explained) which can be used to perform electrical testing on the chip and to verify if the logical part of the circuit was functioning as designed. The other inputs that have to be set include the clock, the preset and clear, the input and the test bit. The clock governs the maximum frequency of data transmission. The maximum speed of charging and discharging is clock/2N where N is the number of stages in an ACMOS structure. The preset and clear bits have to be set for the duration of the first clock cycle and then remain reset for the entire duration of operation. But, each time the circuit is restarted these bits have to be set. The input is the data that needs to be transmitted by the modulator. The test bit is connected to the Direct 0 and Direct 1 lines and when activated helps to bypass the ACMOS circuitry. Thus by supplying the proper signals to the pads the functionality can be verified. Using the test bit, comparison can be made for power savings. The usefulness of the ACMOS technology for optoelectronics can thus be determined experimentally.

3.8 References

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dissipating fCV²", Proceedings of the International Symposium on Low-Power Electronics and Design", San Diego, CA, Oct 10-12, 1994.

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8) W.C.Athas, L.J.Svensson, J.G.Koller, N.Tzartzanis, E.Chou, "A Framework for Practical Low-Power Digital CMOS Systems Using Adiabatic-Switching Principles", International Workshop on Low-Power Design, April 1994, pp. 189-194.

Chapter 4: Optically Powered Smart Pixels

4.1 Introduction

The advantages of using both optical and electronic technologies in hybrid systems become obvious as the strengths of optical interconnects are considered. In addition to the higher bandwidths that result from the non-interacting nature of the optical beams, there is inherent parallelism available from optics that results in interconnects with higher packing densities than electrical interconnects. However, it is more efficient to provide gain needed for both fan-in and fan-out in the electrical domain than in the optical domain. In addition, electronics provides flexibility in designing multifunctional, autonomous smart pixels that enhance the overall processing power of a system.

The performance of optoelectronic integrated circuits in high-density photonic systems is confronted with several critical limitations including crosstalk between channels, excessive power dissipation and difficulties inherent in device interconnection. One critical issue is the performance limitations imposed on the high-density arrays by the electrical voltage supply and logic control lines and their associated AC decoupling circuitry. It is therefore desirable to design a system with a minimum of inductive power supply lines that introduce parasitic signals at sensitive locations in the chip. Furthermore, in some complex switching networks, it is advantageous to remotely control the logic state of a switching element via optical, rather than electrical means. Recently, a novel architecture, based on optically powered smart pixels (OPSPs) which addresses all of these crosstalk and layout issues has been proposed [1]. In this architecture, optical powering replaces the DC bias lines with photovoltaic cells integrated into smart pixels. This chapter describes some applications of OPSPs and also the circuits designed and fabricated.

4.2 Applications of Optical Powering

4.2.1 Different wavelengths for Data and Power

One approach is that data and power are transmitted at different wavelengths, multiplexed and then demultiplexed at the remote end [2]. The optical power is coupled onto an array of photovoltaic cells, providing DC bias and control to a sensitive optical receiver circuit used for detecting a high bandwidth data signal. This is shown in the figure below:

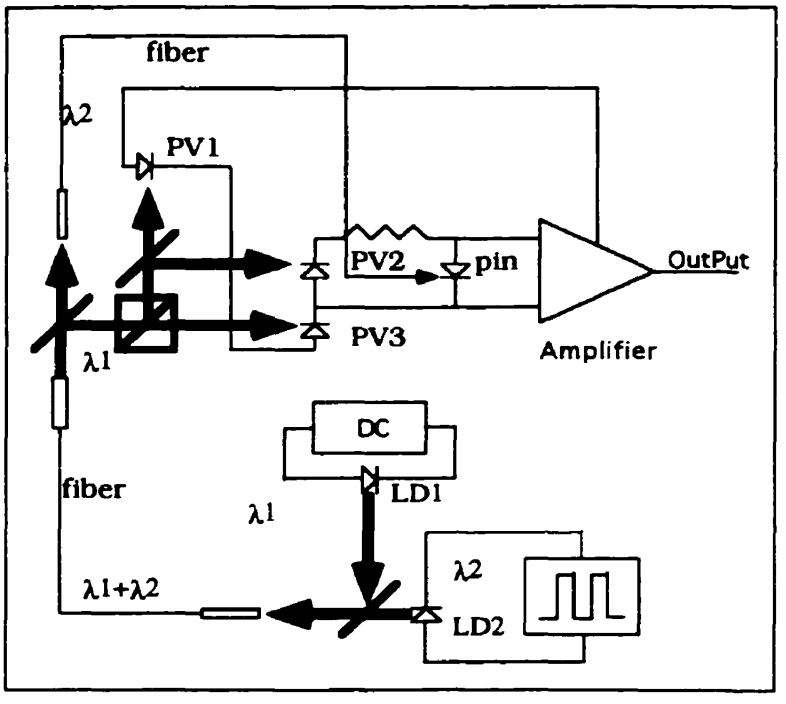

Figure 40: Different Frequencies for Data and Power

Two Laser diodes, LD1 and LD2 emit the DC and modulated signals at different wavelengths respectively. These two beams are then coupled into a fiber. At the receiver end, the beams from the fiber are separated into the two component wavelengths. The DC or continuous wave beam is then split into three parts: two parts are used for biasing

the photodetector, and the third part is used for biasing the amplifier. The modulated beam is made incident on the P-I-N photodiode, and is detected and amplified.

4.2.2 Optical Powering for Telephones

One proposed application of optical powering is to optically operate a telephone line. An optically powered sound alerter has been constructed which demonstrates the feasibility of converting optical power into sound power with good efficiency and at power levels comparable to those of the present telephone ringers [3]. This demonstration establishes the technical feasibility of optically delivering sufficient power to operate a telephone because in principle, all other telephone signaling functions can be accomplished with less power. The interconnect for this application is shown in the figure below:

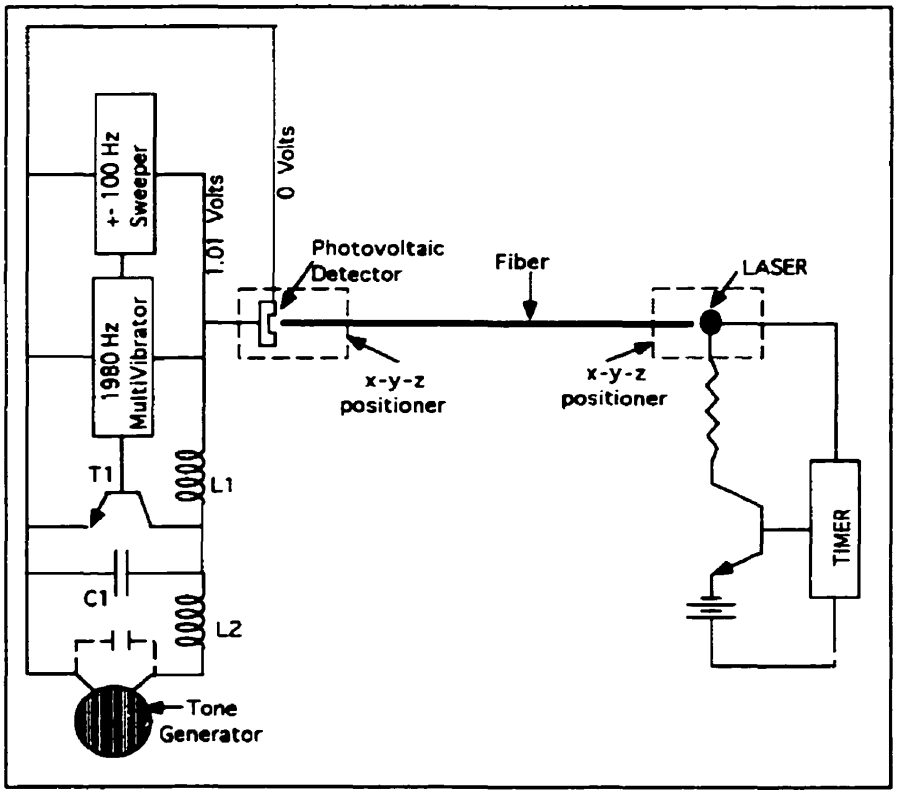

Figure 41: Optical Powering for Telephones

The Laser transmitter is operated in a 2 seconds on and 3 seconds off cycle, causing the alerter to respond similarly. These periodic bursts of optical power are converted to electrical power by the photodetectors. This power is converted into an audio signal by a free running, (2.0kHz nominal frequency), astable multivibrator and an acoustically damped, ringing choke circuit whose capacitive element is the tone generator. The ringing choke and the frequency control circuits are operated directly from the photovoltaic detector output terminals. The 100 Hz frequency modulation ameliorates some of the more irritating effects associated with the use of a single unmodulated tone:

- Strong standing waves (hence dead zones)
- Intensity piercing sound
- Masking of the alerter sound if the noise environment contains pure tones of similar frequency

Optical powering is also desirable in sensing applications for robotics, remote geographical probes and biomedical monitoring devices where it is not possible to locate a bulky power supply in an inaccessible or hostile environment. Remote powering can be used in the event of a power failure at a terminal connected to a LAN.

4.2.3 Optical Powering for Smart Pixels

The application of optical powering considered in this chapter is in the context of high density, high bandwidth smart pixels. Use of optical powering in smart pixels has already been demonstrated [4]. One of such demonstrations dealt with an optically powered, integrated, InP based smart pixel for use in optical interconnection networks. Integrating the optoelectronic pixel circuitry with an InP photovoltaic cell that is illuminated with a 0.82um wavelength laser beam provided optical powering. The circuit is tunable using an optical control beam functioning as a thresholding amplifier, a bistable switch, or as a set-

reset flip-flop. This is shown in the figure below

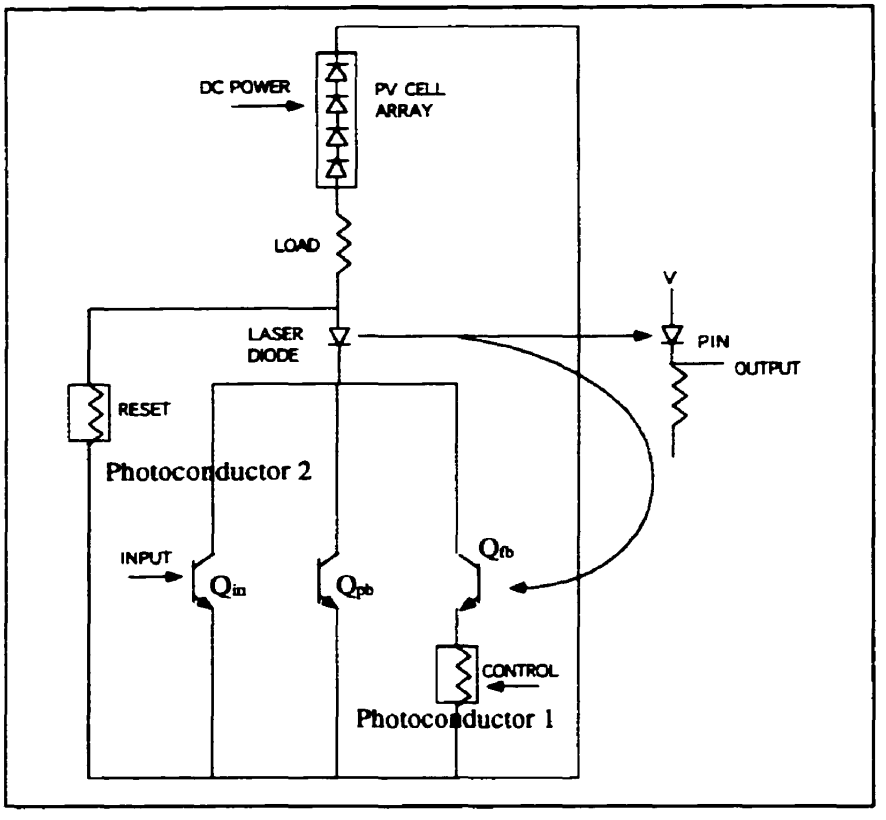

Figure 42: Optical Powering for Smart Pixels

The input data is detected and amplified by the photodetector Q_{in}. The output data signal is emitted by the Laser Diode and the power output is split between the Q_{fb}, which is the positive feedback and the monitor pin photodiode. The positive feedback is essential to drive the circuit into bistable operation. Photoconductor 1 controls the current I_{fb} through Q_{fb}. When $I_{fb} = 0$, the circuit operates in the thresholding amplifier mode. For I_{fb} greater then 0, the circuit operates in the bistable mode, and for $I_{fb} > (I_{th} - I_{fb})$ the circuit latches with I_{th}. Photoconductor 2 is the reset switch and when illuminated turns the circuit to off state thus providing the SR flip-flop operation.

4.3 Description of the OPSP chip

The reason for including an optically powered test structure in the chip was to observe its performance for an optical backplane application. In such an application, the CMOS circuitry as well as the GaAs photodiodes must be optically powered. The photodiodes must be biased to operate in the dual rail receive or transmit mode. Also, the CMOS circuitry has to be powered up by a 3.3V V_{DD}. It is also important to account for the current sourcing capability of this technology. It was for these measurements, that this test structure was put on the chip.

To test the strategy of optical powering, the number of cells put in series to develop adequate voltage drop varied from 4 to 6 (for different test structures). This was because the exact drop that would appear across the diodes was not certain. The CMOS circuitry included was minimal in the shape of a single inverter. The figure below shows the organization of the test structure. It has no electrical interface at all.

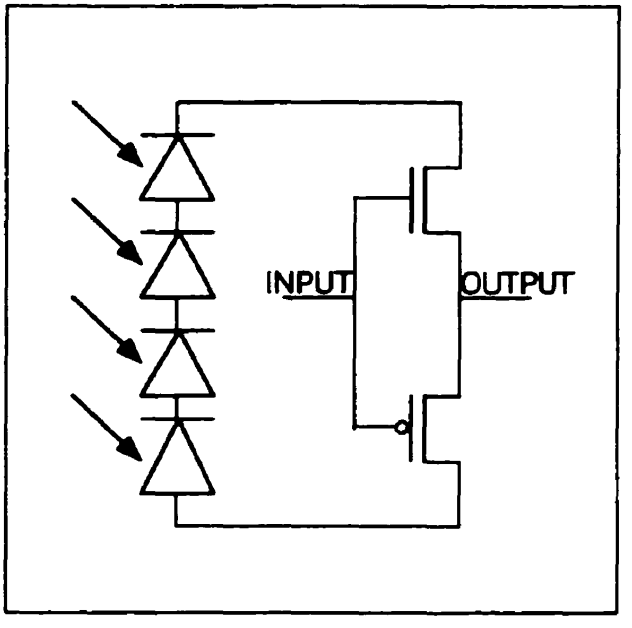

Figure 43: Block Diagram of the circuit on the OPSP chip

Since it does not have an electrical interface, the testing for this

needs to be entirely optical. A linear array of continuous wave beams is needed at 62.5 um pitch for optical powering. This can be provided by an array of VCSELs or by a fan out grating. A single continuous wave beam is needed for intensity modulation also. Probes can also be used for testing the functionality of the chip. They can be used to measure the voltage developed across the photodiodes. The pads of the modulator photodiode can also be probed to see if the voltage levels at the output are in accordance with the input optical beam or not. Thus the powering of the circuit as well as the operation of the Optically Powered Smart Pixel can be tested. To enable testing it is important to know the position of the photodiodes used for the OPSP structures. These can be seen in the figure below which shows the layout of the structures on the chip.

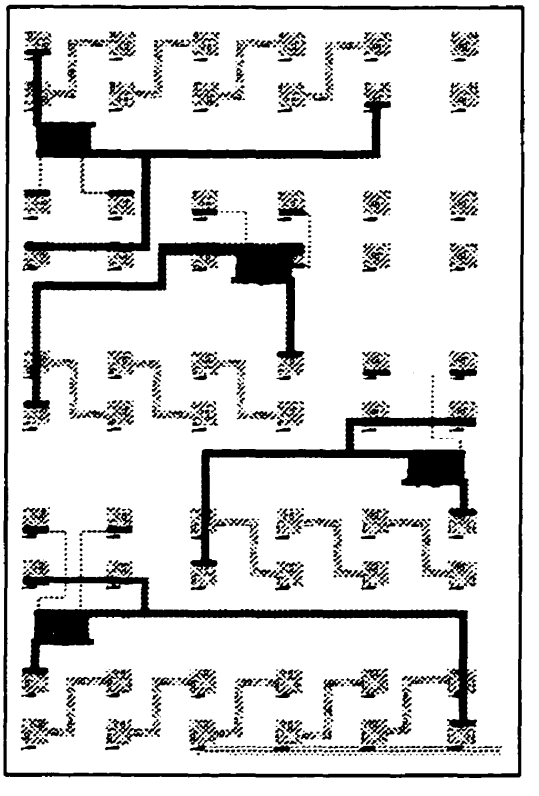

Figure 44: Layout of the OPSP Chip

From the layout it is easy to locate the test structures and to see where the optical beams are needed to be incident on the chip. The linear arrays for operating this chip range from 4 to 6 beams. The intensity of the beams in this linear array will need to be constant with time. This is to ensure that the voltage drop across the photodiodes remains constant and also that the current supplied by the photodiodes does not cause the voltage to drop across the photodiodes. Thus enough optical energy will be needed to source the required electrical power. If the intensity is low then the voltage drop across the photodiodes will fall if more current is drawn from them. The current drawn will depend on the circuit. Since in this case only an inverter is being driven the current requirements should not be too large.

4.4 Conclusions and future work

Optical powering is an interesting concept and promises to be advantageous in reducing noise for Smart Pixel technology. Using this information and some means of generating an array of beams, the test structures on the chip can be appropriately tested for functionality and performance. Based on these measurements the usefulness of optical powering of smart pixels can be evaluated and in future more complicated structures can be build so that the tests are more practical.

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Chapter 5: Optical Test Rigs

5.1 Introduction

For any system to be operational, stage by stage testing and characterization is extremely important. Photodiodes are a major component for characterization in an optical backplane. The biasing voltages and optimal temperature of operation of the photodiodes must be defined. This is because of the change in the responsivity of a photodiode with both temperature as well as the bias voltage[ ]. There is a range of temperatures and corresponding bias voltages for which the contrast ratio is maximized for a photodiode. Apart from the photodiodes, a functionality test of the silicon logic circuitry, the receivers and the modulators is required.

All of the optoelectronic chips made for the optical backplane application at PSG McGill University are dual rail circuit designs. They require a differential signal at the two receiver photodiodes. The modulator ports are also dual rail. If two continuous-wave optical beams are incident on the two modulator photodiodes they are differentially intensity modulated. The next few pages deal with test rigs designed for the purpose of testing and characterizing receivers and modulators along with empirical determination of the optimal prebias and temperature for the photodiodes.

5.2 Two-Beam Optical Test Rig

The first optical test rig was built to test only receivers. Thus, this test rig required two differentially modulated optical beams with intensity control as well as beam steering (in the plane of the chip) capability. Also, it was required to place the board horizontal (carrying the test chip) on the optical table to enable the user to probe the chips. Since the board could not be placed under the microscope, an imaging

system had to be developed which would image the surface of the chip and enable the user to probe the chip and steer the beams to the exact location on the chip. The board was mounted on a x-y-z stage. This also helped in steering the beams. Although a path was provided for illumination, it was not adequate for imaging. This is because the illumination beam would also get focussed and would not illuminate a wide enough area of the chip. Therefore, external illumination was required for this test rig.

There are two identical optical paths for the two modulated beams. These paths begin with the Finisar Transmitters that lead to collimating lenses. Then there is a risley prism pair for steering the beam on the board. A circular graded neutral density filter for intensity control follows the risleys. After the risley pair there is a 50/50 beam splitter which combines the two modulated beams in the same path to reach the board. Then, another 50/50 beam splitter is added for imaging. As already stated, external illumination is provided. Finally, all of the beams are directed through a 90 degree mirrored prism. The beam path is thus changed from horizontal to vertical beyond this point. The last component in the optical path is the microscope objective that serves the dual purpose of focusing the beams onto the board as well as providing the required magnification for imaging. The board is moved in y direction (up and down) till the plane of the board is the plane where the beams are focussed.

The modulation frequency of the Finisar Lasers ranges from DC to 1Gbps. The power output from these Lasers is about 1.5mW. The maximum power available at the board is about 75uW (which is more than sufficient for any receiver circuits that may need to be tested). Using the neutral density filters the power can be reduced to 5uW. Thus the power in the two beams can be varied over a large range. Also the risley prisms have a wedge angle of 1 degree, which allows a large travel to accommodate the wide variety of chips that may need to be tested using

this rig. The beam waist (2w) at the point where the beams focus (plane of the board) was measured to be 25um. This was acceptable, as most of the optical windows are about this size or a bit larger. But, there are no chips (at present) having smaller optical windows. There was a path provided for illumination, but because of the focusing of the illumination beam, the area on the chip that was illuminated and hence could be imaged was extremely small. Given below is a schematic of this test rig which is called the two-beam test rig since there were two significant beams in this rig i.e. the differentially modulated optical beams.

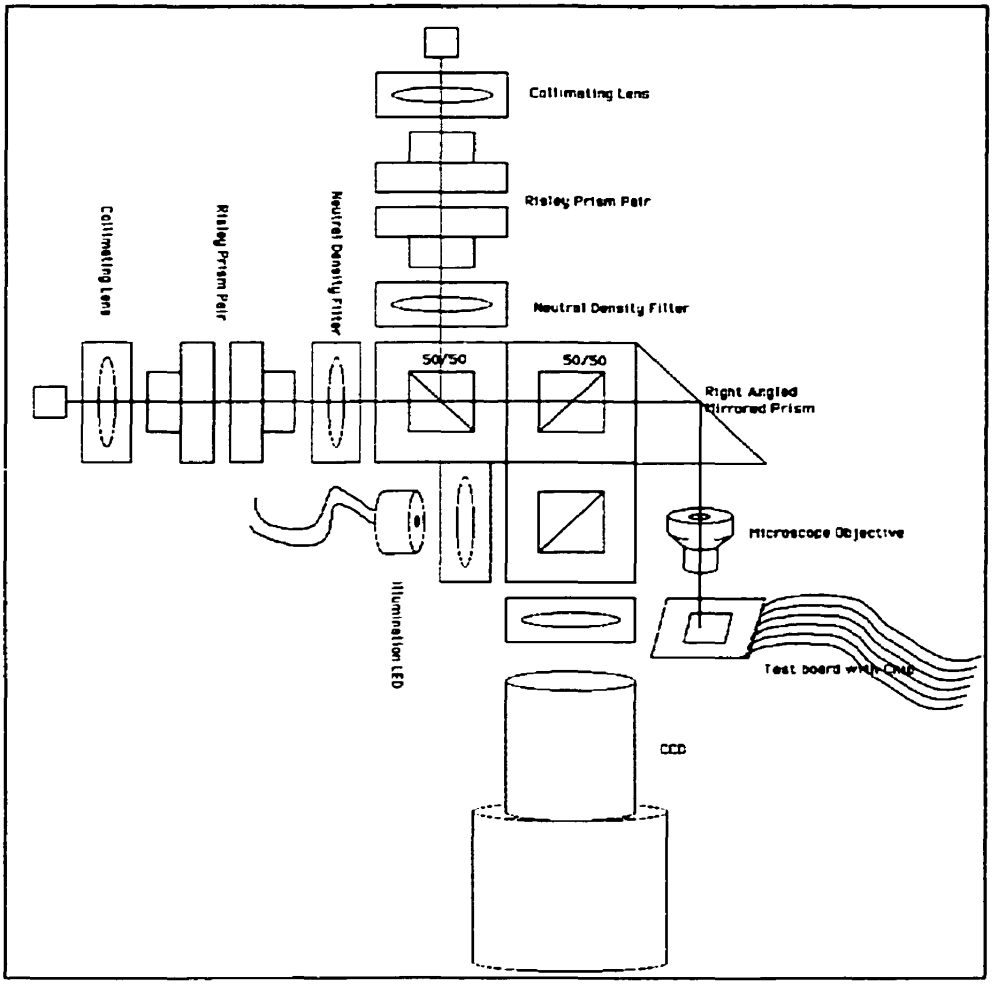

Figure 45: Schematic of the Two-Beam Optical Test Rig

The following figure is a photograph of the assembled two-beam

test rig

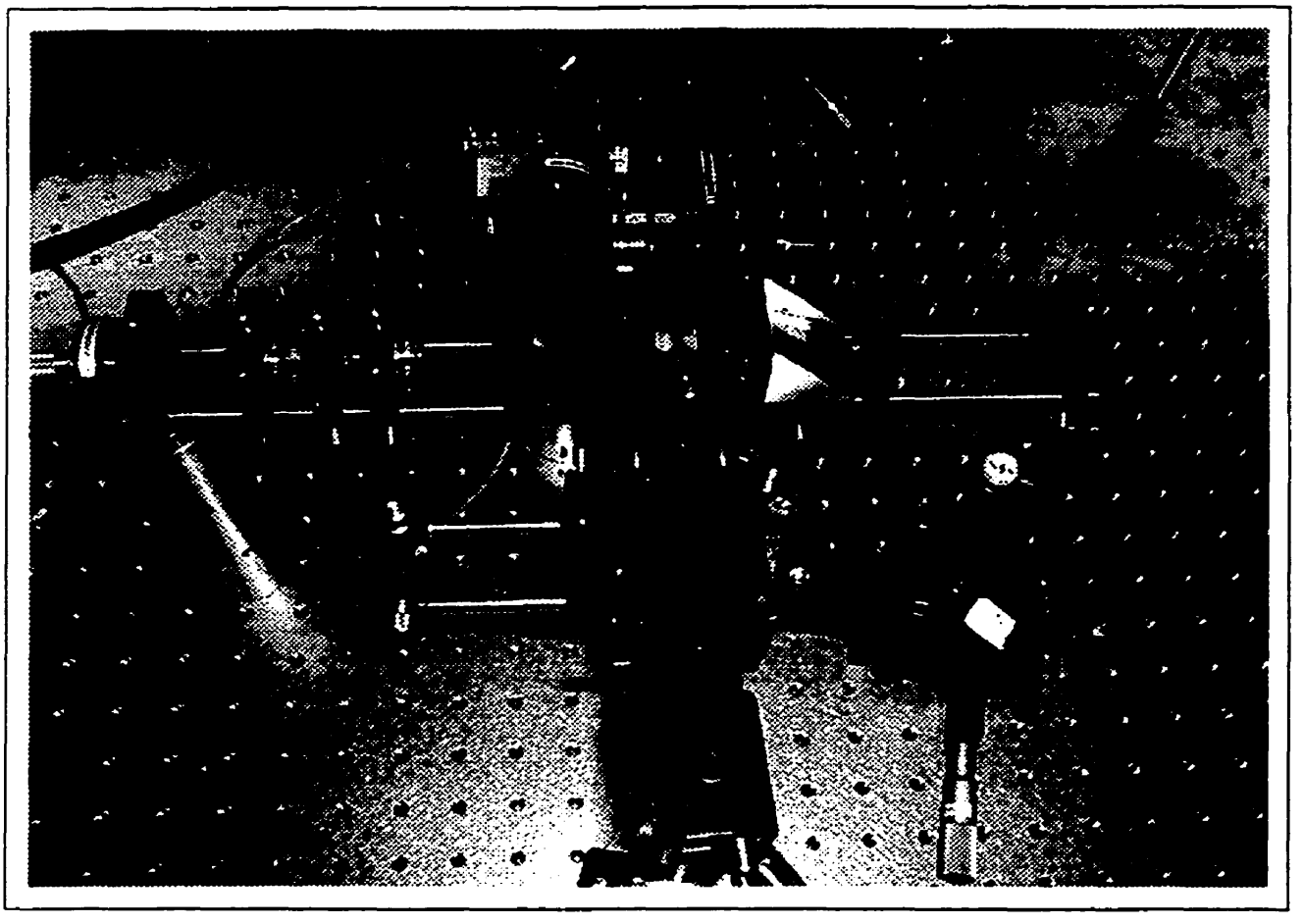

Figure 46: Photograph of the Two-Beam Optical Test Rig Setup

This test rig was extremely useful for testing receiver circuitry. Because of the intensity control on the beams the sensitivity of the receivers could be tested by decreasing the absolute power as well the difference between the two power levels corresponding to one and zero. If the board carrying the chip has active temperature control the response of the photo-detectors as a function of temperature can also be observed. Because of the facility of being able to steer the beams, it was much easier to position the beams so that they land in the center of the active

region of the photo-detectors. Since the beam sizes were small it was easy to get a single beam on a single detector instead of spreading in the surrounding area. The only problem was that the lenses used were very fast and this made the placement of all the components extremely critical and the alignment of the rig was very sensitive. Because of the mechanical drift with time the alignment of the rig had to be adjusted every few days. It would have been better to design the rig with slower lenses. If the rig had to be redesigned it would be better to try and incorporate illumination in the rig itself. Instead of using the microscope objective to control the size of the beams, the small beam waist can be obtained by using proper focal length lenses.

5.3 Three-Beam Optical Test Rig

This optical test rig was a much more advanced form of the first rig with three significant beams instead of two. It still has the same two differentially modulated optical beams and additionally a continuous wave (CW) optical beam for the modulators. The CW beam is called the read out beam.

The design of this rig was different from the two-beam test rig in many respects. The beams output from the Lasers are coupled into multimode fiber (these are pigtailed fibers) and then these beams are collimated at the other end. A major advantage of this rig over the previous one is that it is completely telecentric. A microscope objective is not used in the path of the beams. It is only used with the CCD camera for imaging. This was because the beam sizes needed were much larger (2w = 50um). Also this rig does not need the feature of probing. As a result the entire rig is horizontal and the board is mounted vertically. The intensity of the two modulated beams is controlled using polarization optics. The beams are polarized using a polarizing beam splitter. The beam emerging from the beam splitter is P polarized and the S-polarized beam gets reflected and is lost. Next, there is a half wave plate in front of

the beam that controls the angle of polarization of this beam. A half wave plate is a retardation plate that introduces a relative phase difference of π radians or 180 degrees between the o and the e waves. Suppose that the plane of vibration of an incoming beam of linear light makes some arbitrary angle θ with the fast axis. When the waves emerge from the plate there will be a relative phase shift of $\lambda_o/2$ (that is, $2\pi/2$ radians), with the effect that E will be rotated through 2θ. A half wave plate will flip elliptical light and invert the handedness of circular or elliptical light, changing right to left and vice versa. The effect of a half wave plate on linearly polarized light is shown in the figure.

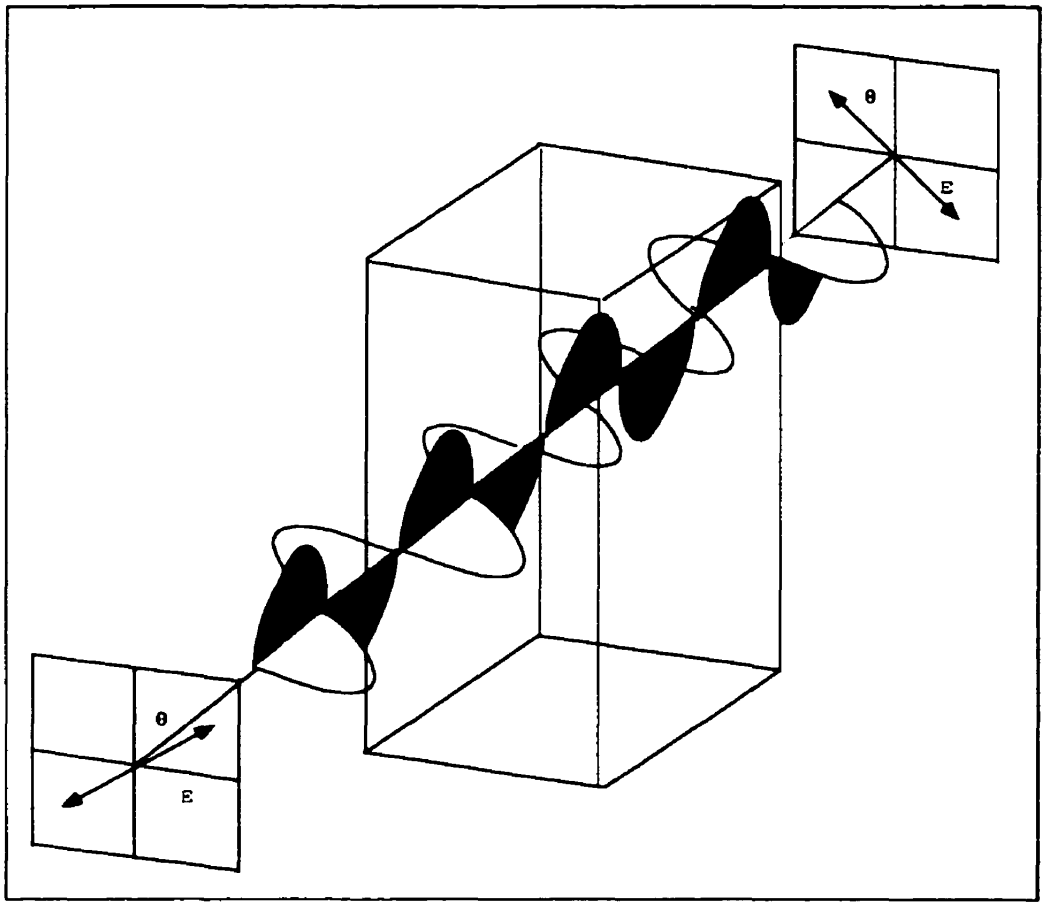

Figure 47: Effect of a Half Wave Plate on Linear Polarized Light

Thus the linearly polarized rotated by twice the angle that the fast

axis of the half plate makes with the E of the wave. After the half wave plate we have another polarizing beam splitter. The intensity at the output of this beam splitter depends upon the angle of rotation provided by the half wave plate. If it is zero the intensity is maximum, if it is 90 degrees the intensity is minimum. This beam splitter also helps to combine two beams in this setup. The other optical path that joins with this beam splitter is identical to the path just described and is the second modulated beam path. The only difference is that since it is the reflected beam that gets combined the angle of rotation has to be 90 degrees for maximum intensity at the output. This is shown in the following figure

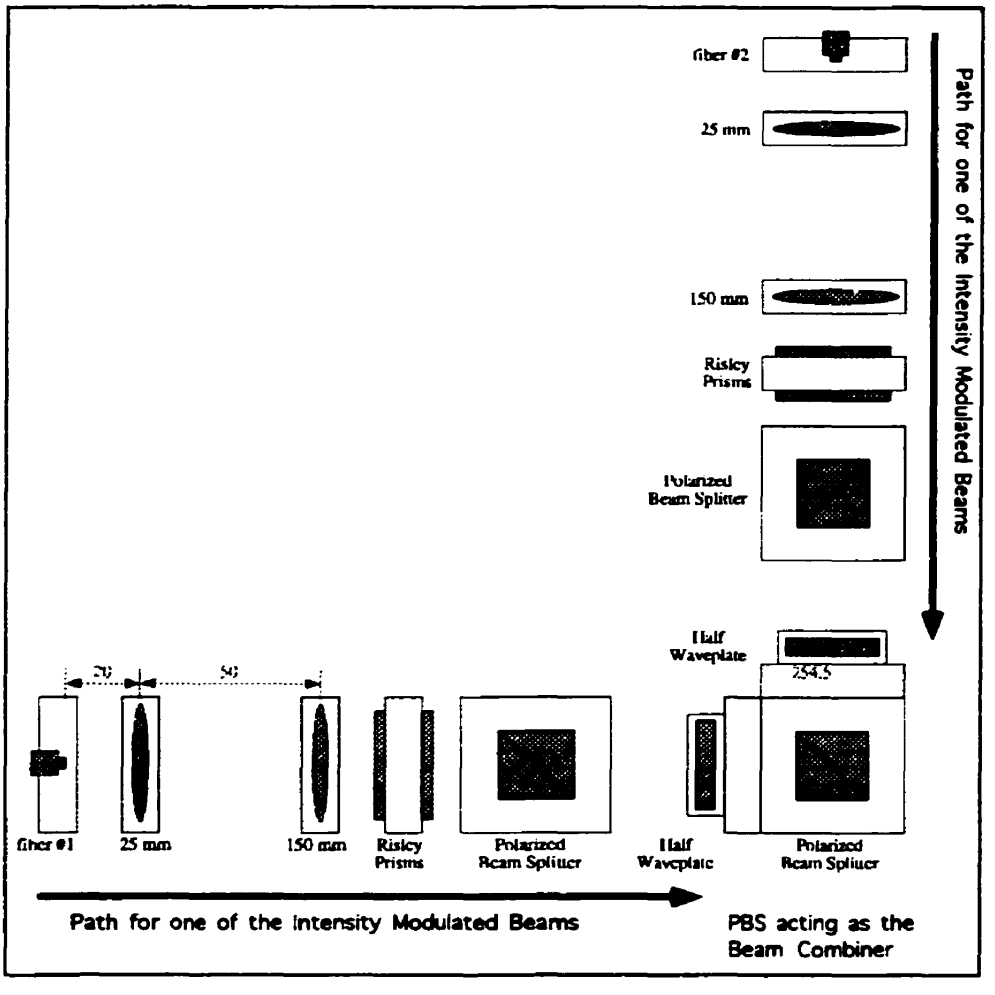

Figure 48: The Optical Path of the Two Differentially Modulated Optical Beams

The third beam is the read out beam. It is derived from a continuous wave source and combined with the other two beams by means of a 50/50 beam splitter. All three beams have risley beam steerers in their path to move the beams spatially so that they are at the required location on the board. The read out beam gets modulated at the chip and gets reflected (it is intensity modulated). The last 50/50-beam splitter in the significant path directs the modulated beam to a photodetector. Apart from this provision is also made to illuminate and image the surface of the chip as well as the face of the photodetector to guide the beams properly at their proper locations. This is shown in the next figure.

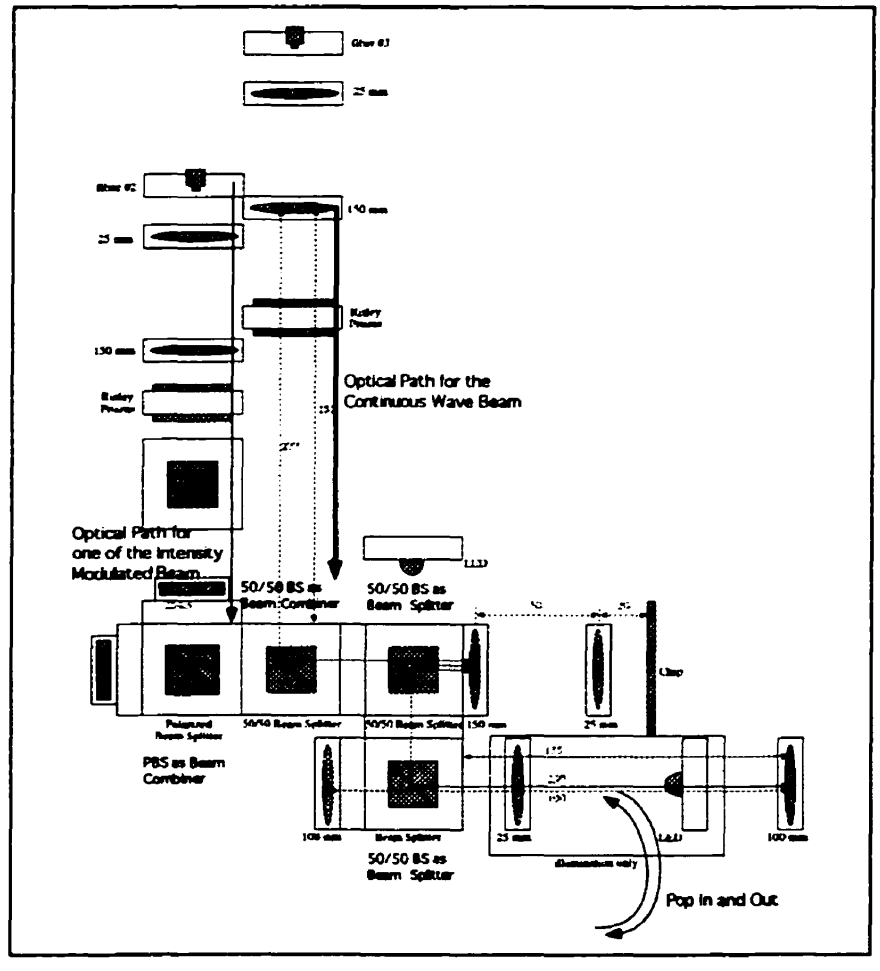

Figure 49: The Optical Path of the Continuous Wave Beam and imaging of the Chip

Thus there are two CCDs. One for viewing the chip and one for the photodetector. Also there is an illumination strategy for illuminating the chip by placing the LED and lens in front of the photodetector. When we need to see the read out beam the LED and the lens can be removed from the path. The other LED should only be turned on when the photodetector needs to be seen to direct the read out beam on its active region. The complete design of the optical test rig is shown in the following figure.

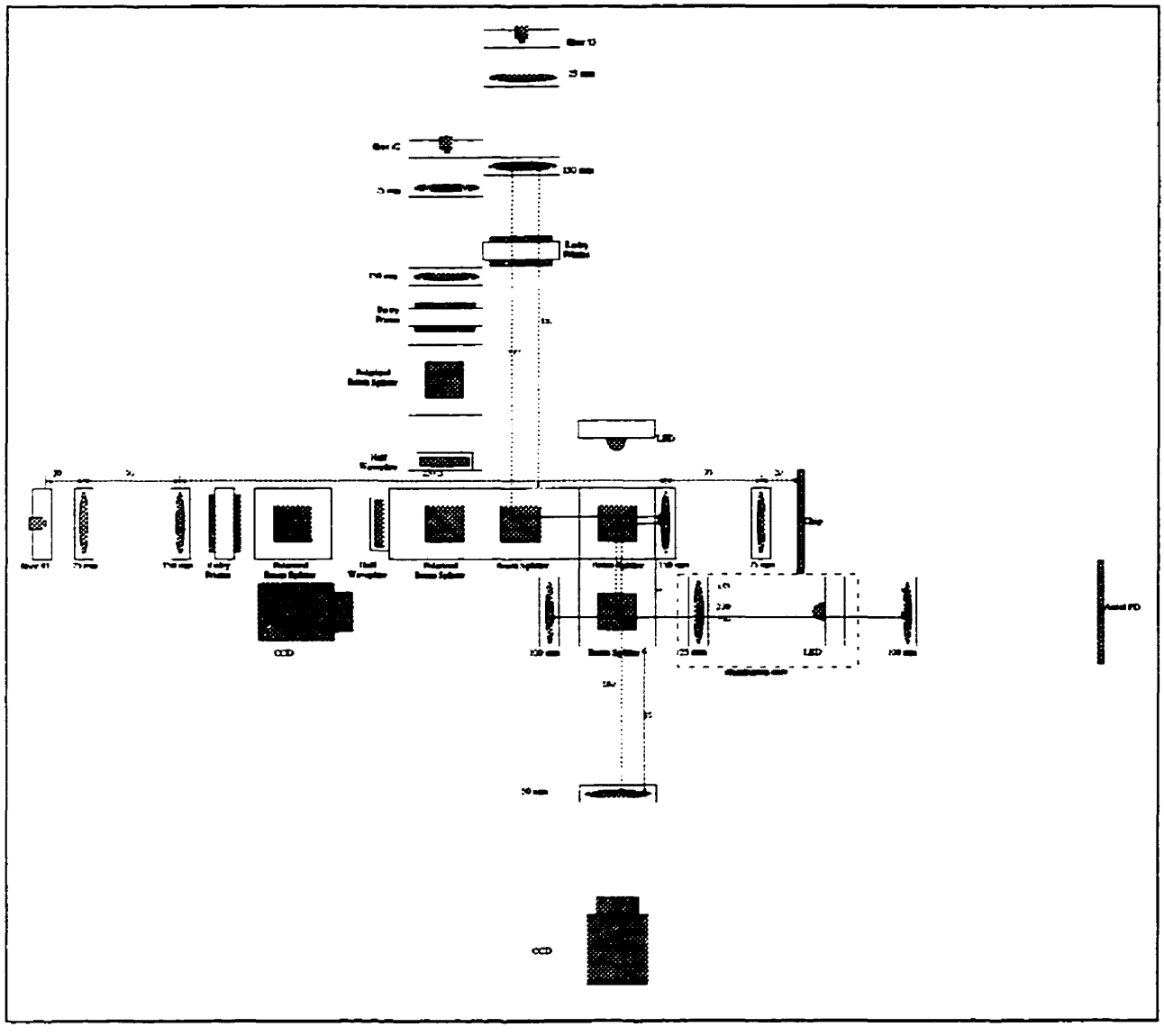

Figure 50: Block Diagram of the Three-Beam Optical Test Rig

The following is a picture of the actual test rig assembled and aligned completely

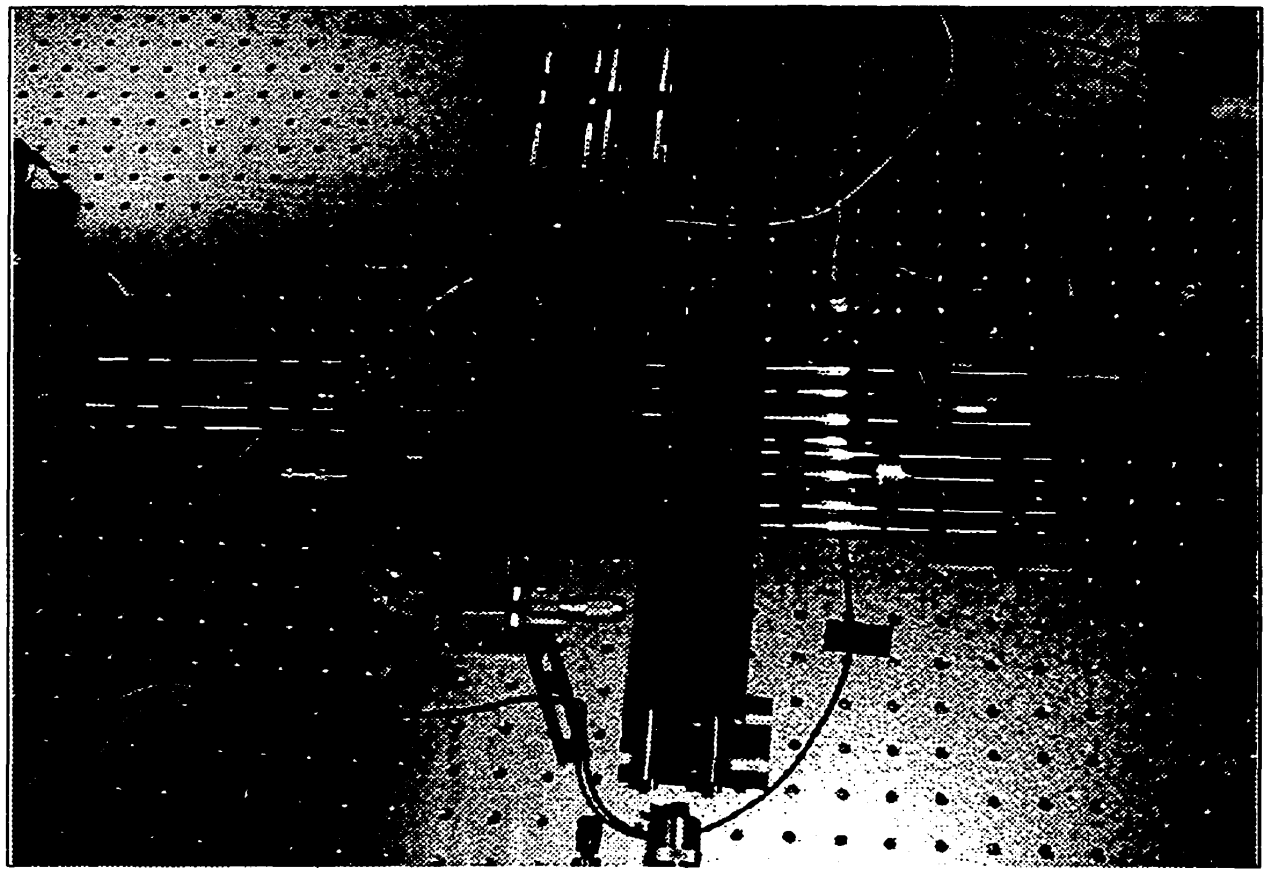

Figure 51: Photograph of the Three- Beam Optical Test Rig Setup

This optical test rig is extremely useful for characterizing receivers as well as modulators. Since it has three significant beams as well as illumination and imaging, it was a challenge to design and align. All three significant beams can be independently steered and adjusted in power level. The two modulated beams land at the receiver photodiodes and the continuous wave beam lands at the modulator photodiode, is intensity modulated, reflected from the modulator and received by a detector. Thus the photodiodes can be characterized for both modes of

operation i.e. as modulators as well as detectors. As mentioned before, if the electronics permit the bias on the photodiodes can be changed to characterize them and the temperature of the die can also be controlled and set at the desired value. It is a very useful setup and can be used to many different tests. Apart from the characterization of the photodiodes that was its primary purpose it can also be used for functionality tests of optoelectronic smart pixels. If the smart pixel being tested is made to operate in a transparent mode of operation, whatever is input at its receiver port is transmitted at the transmitter port. If a particular bit pattern is encoded in the modulated beams then the same bit pattern should be available from the detected beam also. This will prove the functionality of the transparent mode of operation. Similarly, for injection and extraction the electrical input and output ports can be used along with the test rig to test the complete functionality of a smart pixel. For extraction, the modulated data (from the differential beams) should appear at the electrical output port and in the case of injection the CW beam should get intensity modulated with the data at the electrical input port. Apart from this, the characterization of the receiver circuits on the chips can also be performed with the help of this rig. Using the intensity control on the input beams can test the receiver sensitivity. If the response of the photodiodes is already known then the receivers can be properly characterized and their performance evaluated. All this characterization ability makes this rig unique and extremely useful. The design and alignment of this rig was a joint effort of the author and David Rolston, another graduate student at PSG, McGill University.

5.4 Conclusions

These test rigs were designed and setup for the purpose of characterizing the photodiodes on the opto-electronic chips as well as testing of the modes of operation of the SPAs. The wavelengths of the two complementary modulated beams were about 845nm and the wavelength

of the continuous wave beam was about 852nm. These rigs can successfully make incident two differentially intensity modulated beams on the surface active photodetectors on the opto-electronic chips. The three beam rig also has a continuous wave beam incident on the modulators for intensity modulation. Thus these rigs can be used to fully characterize the photodiodes on any opto-electronic chip.

5.5 References

1) Eugene Hecht, "Optics", Addison-Wesley Longman, Inc.
2) B.E.A.Saleh, M.C.Teich, "Fundamentals of Photonics", A Wiley-Interscience Publication.

Chapter 6: Phase 3 Packaging and Characterization

6.1 Introduction

Photonics Systems Group (PSG) at McGill University is involved in the task of building yearly demonstrators for proving the feasibility of free-space optical interconnects. These demonstrators are based on the ring type architecture with four chips communicating with each other (concept of an optical backplane). The Phase III of this task is currently in progress. The optical interconnect for this demonstrator was designed by Brian Robertson [1]. The optical data links for this design are arranged in clusters [2]. The P3 BiCMOS-QCSE chip is the core device for this demonstrator. The chip is an 8x8-mm chip with a 16x16 array of Smart Pixels. On the surface-active chip there are 1024 QCSE (photodiodes) devices, arranged into an 8x8 array of optical clusters of 4x4 photodiodes. The phase 3 chip consists of 189 bond pads, consisting of 32 inputs, 32 outputs, 2 clocks, control, and power pads. The demonstrator is designed to form a 4 stage free space optical interconnect arranged in a ring type architecture. This chip had needed to be packaged and the electrical and optical interface to the chip had to be provided for the purpose of having an operational free-space optical interconnect demonstrator. There was active temperature control required for the die substrate. The next few sections deal with a description and the characterization of the package for this design. This chapter also deals with a brief description of a simple motherboard designed by various members of PSG for operating the phase 3 optical backplane. The board was laid out using Mentor Graphics by the author and another student, Madeleine Mony.

6.2 Description of the Package

David Kabal, a former student of PSG, McGill University, designed this package and the author characterized it. The optical interconnect for this system is extremely compact, and this compactness leads to a space constraint for the optoelectronic packaging. The total available footprint (area in chip's plane) was 4x4-cm. There was no volumetric constraint. Because of the tight space constraint the approach adopted was to move the connector away from the packaging. The electrical package needed 139 signal connections to the "Mother Board" (the board that supplies all the logical as well as power connectivity to each stage of the optical backplane). Terminations for the 32 electrical input, the 32 electrical output lines and the two clock lines were required. Impedance control for the data and the clock lines was required. Provision was made for the active temperature control of the chip. The chip was anticipated to dissipate about 5W. The optimal temperature was empirically determined to be around 50°C for these photodiodes. The designed package module is shown below in the figure 52

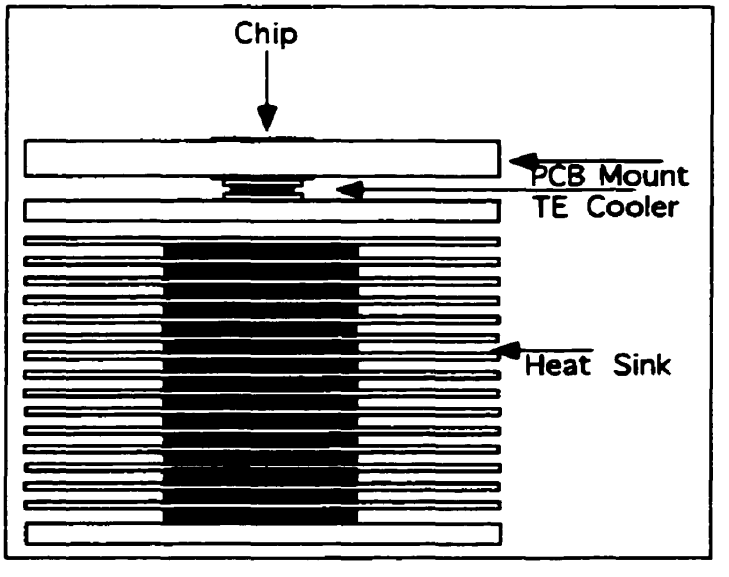

Figure 52: Schematic of the Package Module

For the package module, flexible printed circuit with 8 mil line pitch was designed [3]. This connected the package module to the Mother Board. A high density 190 pin connector was used at the mother board end. Bond pads were wire bonded directly onto the flexible PCB. The flexible PCB was 6 mil thick. The connector at the mother board end was 50Ω impedance controlled, as was the mictrostrip stackup. High speed inputs were terminated using active Schottky diode terminations. Clocks were terminated using ¼W 50Ω resistors. Outputs were to be terminated on the Mother Board. Surface mount decoupling capacitors were located next to the power supply rails on the flexible PCB where the bond pads of the chip are attached.

The P3 chip is mounted on a 0.0625 inches thick PCB mount that is attached to the flexible PCB. The PCB is also 40x40 mm in size. The chip is mounted using thermally and electrically conductive silver-filled epoxy (Epoxy Technology H20F) [4]. The mount is also used as a ground connection for the rear side of the chip, so the high electrical conductivity of the H20F adhesive was also desirable. The chip is wirebonded directly to the gold plated wire bond pads on the flexible printed circuit board using an aluminum wedge ultrasonic wirebonder. The flexible printed circuit is designed to allow for the required bends and space constraints imposed by the presence of four 100x160 mm (3U x 160mm) Mother Boards in a 3U VME chassis. The complete packaging system required for a 4 node optical interconnect is shown in the following figure.

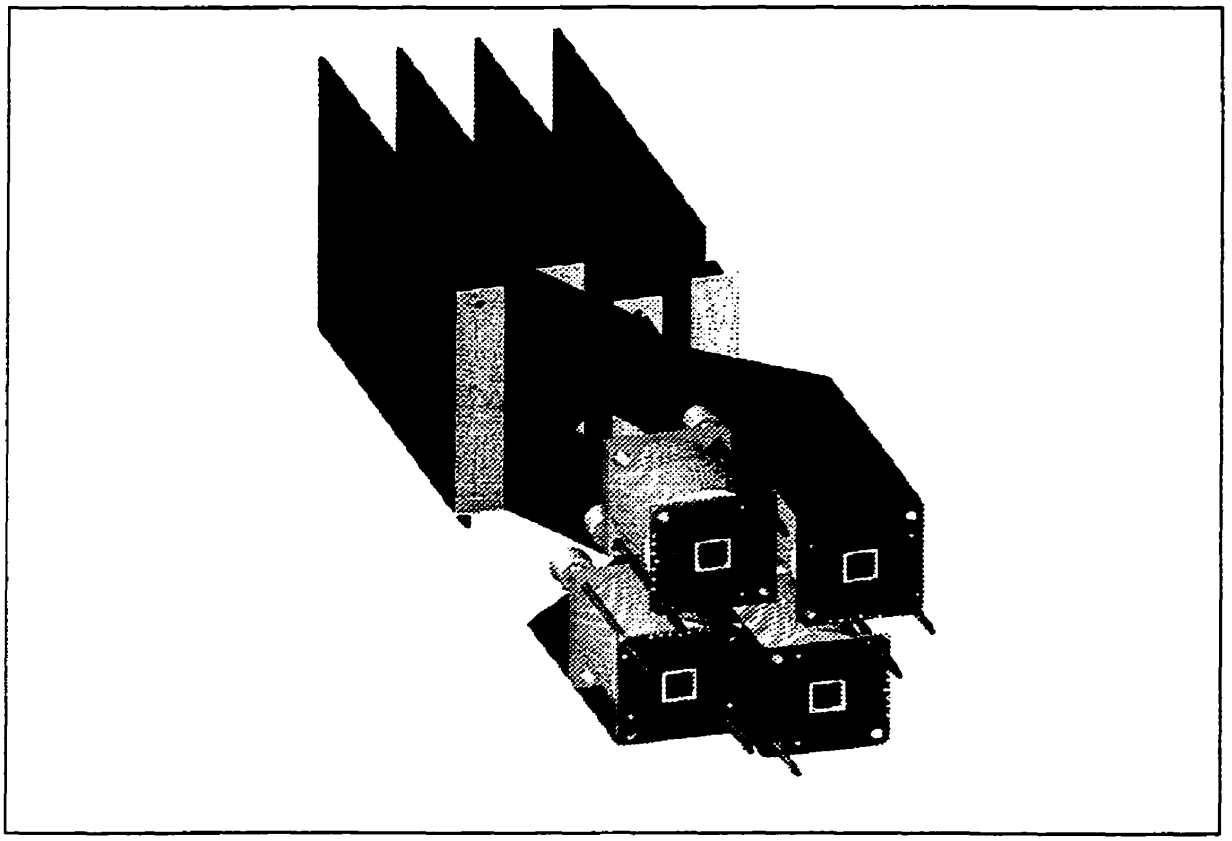

Figure 53: Packaging System with Four packages arranged in ring architecture

The flexible printed circuit board is shown in the following figure. The overall dimensions of the circuit were 260 x 120 mm when flattened. In the final packaging configurations the flexible circuit has two boards with 90° bends and two with 180° bends. The is shown in the following figure

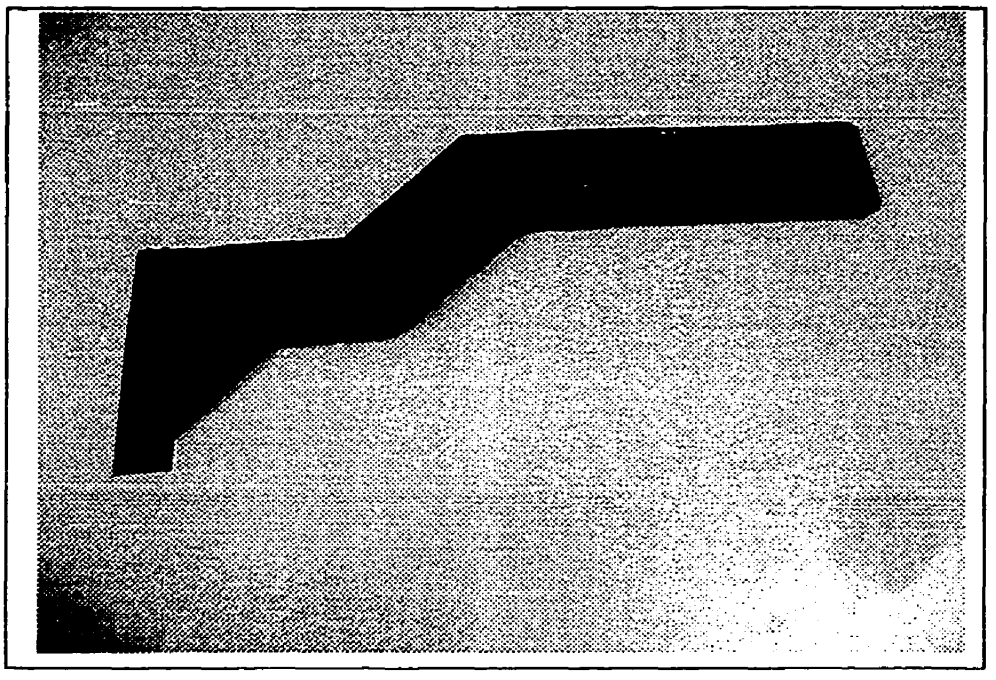

Figure 54: Photograph of the Flexible Printed Circuit Board

This alternating bending was mandated by the optical system, where each packaging module must be rotated by 90° clockwise. The flexible circuit is 150 um in thickness (6 mil) and has two copper layers. Where the "coverlayer" (solder mask) does not cover the traces, the copper has been plated with nickel and then a protective layer of gold, to allow exposed pads to be wirebonded using an aluminum wedge wirebonder.

The design constraints imposed by the system and the chip design dictated termination of the signal and clock lines. The clock lines are required to operate at a 5V swing at a frequency of 320 MHz. The input pads on the chip are standard high impedance CMOS pads, necessitating external resistor termination. The two clocks, designated by chip design as Clock and Receiver-Clock are terminated with a resistor of 50Ω (the characteristic impedance of the flexible printed circuit). Power

considerations in the terminating resistors determined the termination to 2.5V instead of Ground. For the high speed input lines, a termination method was needed to allow them to operate at the expected chip performance bit rate of 100 MHz. Resistive termination was not possible because of space constraint. Instead, active termination using Schottky diodes was used. This method allows for characteristic impedance independence, as the diode terminations are designed to prevent only excursions from supply rails (0V and 5V in this case). Two decoupling Capacitors are located immediately adjacent to the chip on the flex PCB. The thermistor is located on the back of the PCB mount close to the TE cooler. There are some other alignment features on the board, to interface with the rest of the system.

6.3 Characterization of the Package

To test the characteristics of the packaging system, one complete package module was assembled. This package module incorporated an electrical-only version of the P3 chip. This was attached and wirebonded into the mount. The measured lateral misalignment of the chip in this configuration was less than 50um. The connector, the termination components, and the decoupling capacitors were mounted using surface mount soldering techniques onto the flexible printed circuit. A front view of the assembled package is shown in fig 55 and the complete package module is shown in fig.56

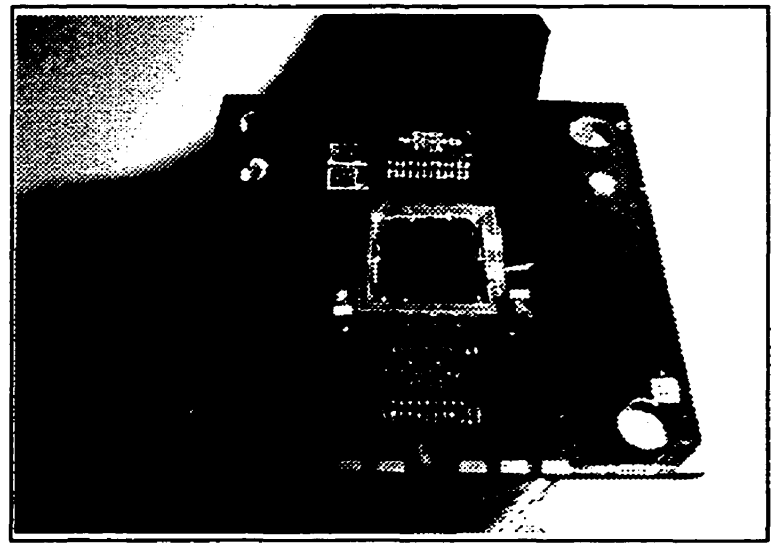

Figure 55: Front Face of the Populated Flexible Printed Circuit Board

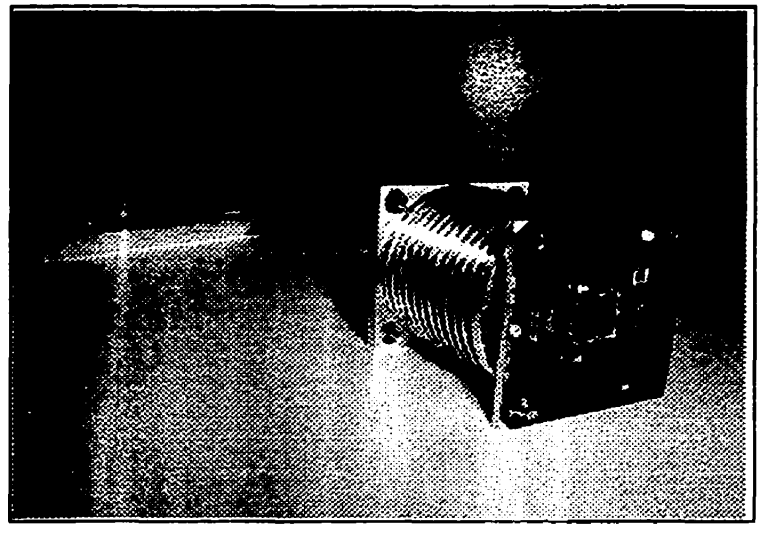

Figure 56: Photograph of the Complete Package Module

6.3.1 Thermal Characterization

The data collected for the photodetectors shows that for maximum responsivity, the prebias and the temperature have a certain optimal range. The optimal range for temperature is in between 40-50 degree centigrade. The power dissipation of the chip was anticipated at 5W. It

was thought that with 5W of power dissipation the temperature of the chip without any cooling mechanism would be much higher than desired. The designed package thus had a large heat sink for lowering the temperature of the chip with the help of a Thermo-Electric Cooler [5,6]. Experiments were carried out after the design of the package. These experiments involved placing a 5W dissipative resistance in place of the chip and trying to set the temperature at a fixed point between 40-60 degrees. It was found that the steady state temperature without the TE cooler was only about 40 degrees. Thus for a temperature within the determined optimal range the chip had to be heated rather than cooled. It was found that since the heat sink tried to keep the chip at room temperature, it was actually working in the reverse direction and caused the temperature to become very unstable. When the heat sink was removed and the TE cooler worked towards heating the chip the temperature could be controlled to within 0.01 degrees without any problems at all. Based on these empirical results it was decided that the heat sink will not be included in the package. The package was slightly redesigned to look as in the following figure

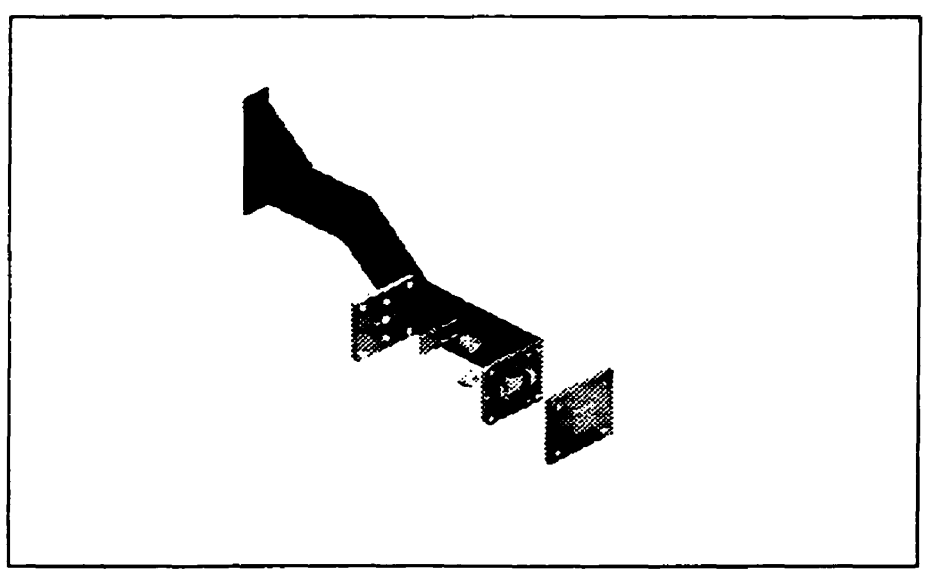

Figure 57: Exploded View of the Package Modified Package Module

6.3.2 Electrical Characterization of the Package

A test board was designed to allow for electrical characterization of the package before the Mother Board was designed as a means of testing the package and parts of the chip. This test board allowed high-speed connection via SMA-type connectors to a representative number of inputs on the package. Using a network analyzer, the performance of these specific traces can be measured. Individual trace performance can be measured using the Time Domain Reflectometer (TDR) features of the network analyzer, and an analysis of the characteristic impedance of the traces can be obtained using the Smith Chart feature.

The average characteristic impedance of these traces was 50Ω. The peak deviation was in the clock traces with a 20% error distribution over the entire length (from 41Ω to 60Ω). The resistance of the traces measured from the 190 pin connector to the end of the trace was less than 5Ω in all cases. The delay of the traces measured from the 190 pin connector was approximately 5ns. Using these values, measured by a properly calibrated network analyzer, the exact length of each trace and combining both coverlayer and dielectric permittivities, the relative permittivity of the stackup was calculated to be 4.7. This relationship was derived from :

$$v = \frac{c}{\sqrt{\varepsilon_R}}$$

where v is the velocity in the medium, c is the speed of light in a vacuum, and ε_R is the relative permittivity of the medium, such that

$$\varepsilon = \varepsilon_o \times \varepsilon_R$$

The permeability is assumed fixed at

$$\mu = \mu_o$$

Solving for a representative trace, given its exact length (available in the Mentor Graphics CAD environment)

$$\varepsilon_R = \left(\frac{c \times t}{l}\right)^2$$

where l is the length of the trace, t is the transit time obtained by measurement with the TDR.

To test the transmission of the clocks into the termination, a 3.1 V swing signal about 2.5 V (0.95 and 4.05 V) was used. Active FET probes were used to sample the resulting waveform at the termination on the flexible printed circuit board. The input waveform had a rise time and fall time of 200ps at an operating frequency of 320 MHz (square wave at 640 Mbps). The resultant is shown in the following figure

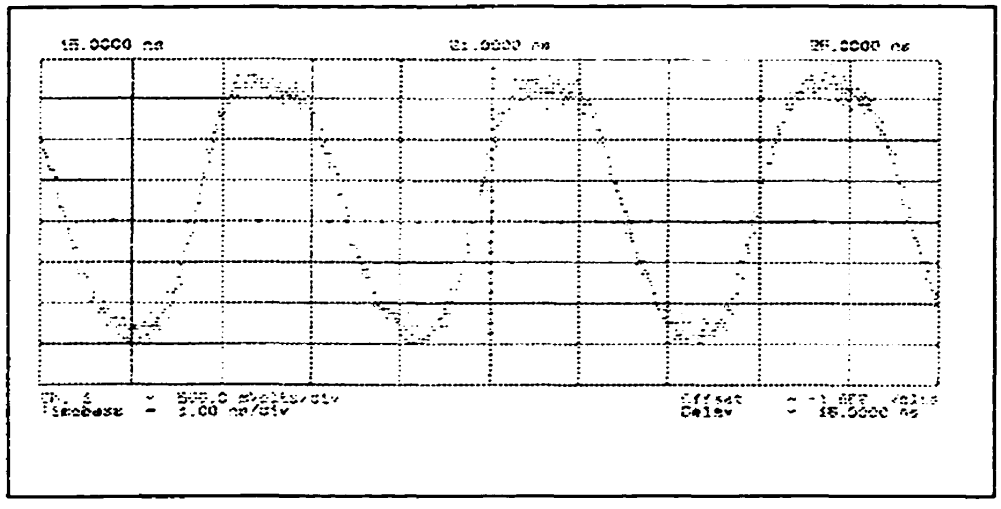

Figure 58: The Clock Waveform at 320MHz at the Chip and of the Flexible PCB

This waveform has a 50% duty cycle compared to the input 50% duty cycle, and has a rise time of 1.5ns, making it nearly sinusoidal [7].

Some other tests were conducted with the flexible printed circuit board with the input having a 5V peak to peak voltage swing. The rise time of the input signal was measured to be 2ns (at the input to the flexible connector). The rise time at the other end of the traces was also found to be 2ns. This experiment proved that the flexible PCB was capable of completely transferring a 2ns-rise time input signal from its input to the

output without any distortion.

Following are the TDR measurements taken for characterizing the printed circuit board. In each case the first peak represents the 190 pin connector along with the extremely close (approximately 1 cm away) SMA connector for the input signal, and the second peak represents the termination. The vertical scale is 100 mUnits/div, where 1Unit represents a reflection over incident factor of 1.0. These values indicate the absolute values of ρ, the reflection coefficient, where a value of 1 would indicate 100% reflection (for an un-terminated transmission line), and 0 indicates no reflection. In each of the TDR graphs, the peak value at the line termination is marked.

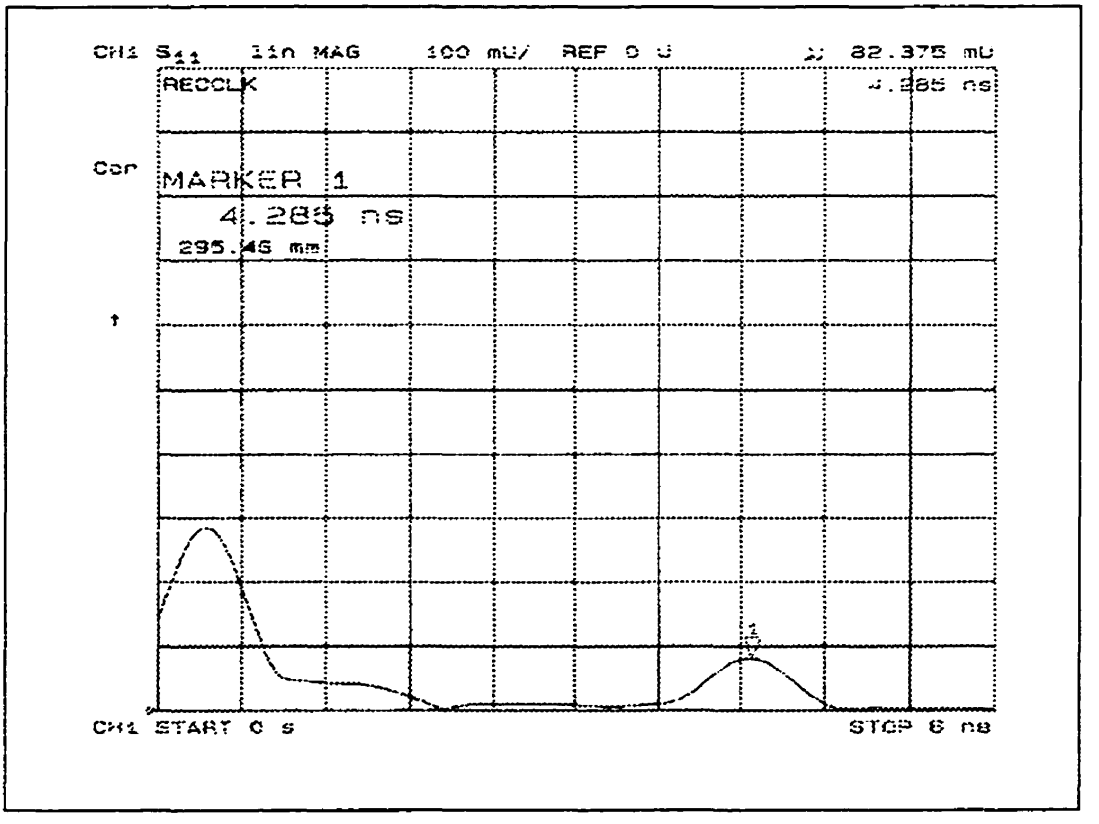

Figure 59: TDR Measurements of the Receiver Clock

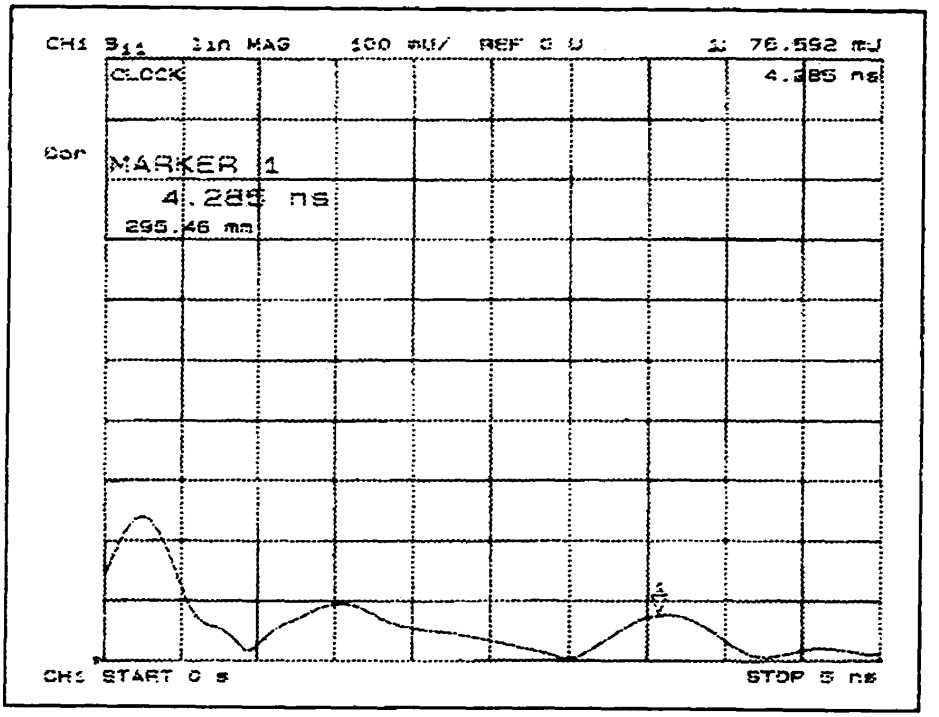

Figure 60: TDR Measurements of the Clock

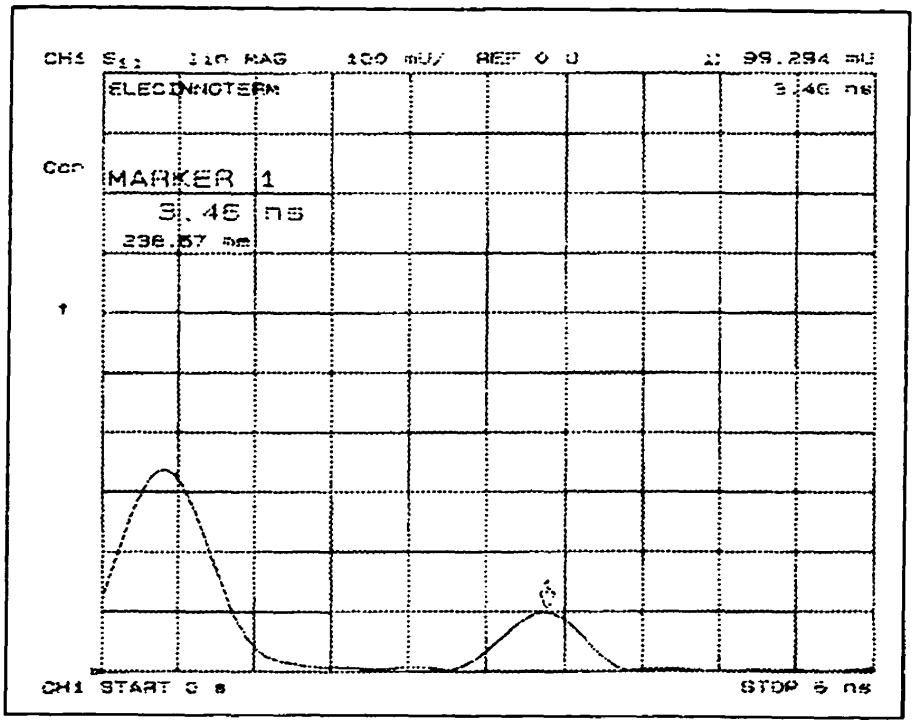

Figure 61: TDR Measurements of the non-terminated Electrical Input line

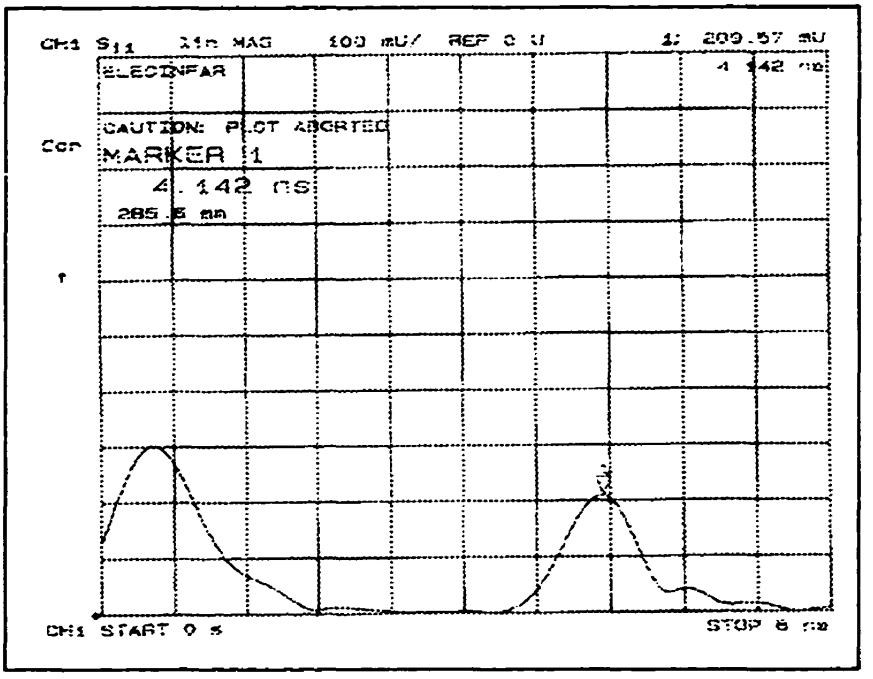

Figure 62: TDR Measurements of the Electrical Input line at the far side of the flex

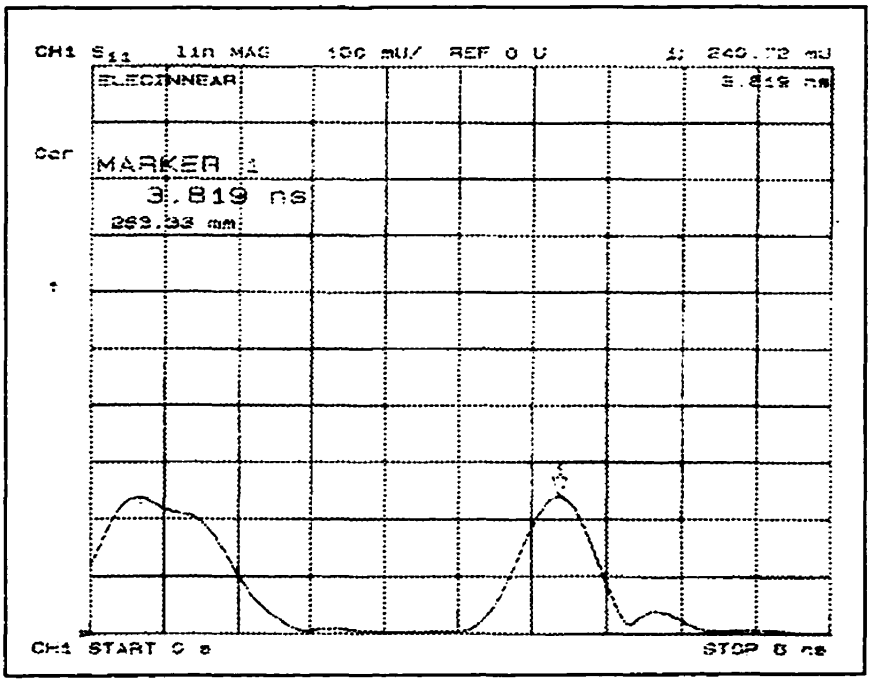

Figure 63: TDR Measurements of the Electrical Input line at the near side of the flex

6.4 Description of the Mother board

This board was designed and fabricated with the purpose of driving the P3 chip. Its main purpose was to be able to set all the inputs required on the chip as well as to be able to monitor all the outputs from the P3 chip. The board is fairly simple in design with a large number of monitoring ports on the board. There are 32 headers for monitoring 32 input lines as well as 32 headers for monitoring 32 output port lines. It has a 190-pin connector on one end (for connecting to the flexible PCB package for the phase 3 chip) and a 26-pin connector on the other end for interfacing to a PC. The PC sets all the control lines on the chip using a Digital input/output (DIO) board from National Instruments. The DIO board has digital outputs with voltage levels 0 and 5V.

The test board is a standard 3U chassis board having a fixed height of 10cm and a length of 16 cm. It has about 300 components on it. It is a double sided board having 5 signal layers and 5 power planes. There are both analog as well as digital circuits on the board. The analog part has been given separate power planes. VCC (analog) occupies one power plane. Vee and VTT (also required for the analog circuitry) share one power plane. The ground plane is common for all. There is a VCC (Digital) power plane and a plane for the bias lines for the photodetectors. These five planes are interlaced with the signal layers so that crosstalk among the various signal layers on the board is minimized. All the signal traces are made of close to 50Ω characteristic impedance. The range of impedance varied from 45-50Ω for all the traces. The power traces are not impedance matched. They are made much thicker to carry a lot more current rather than impedance matched for speed.

There is an 8 pin power connector for the 8 power lines and a four pin connector for the TE cooler and the thermistor. Apart from this there are 4 input coax cables which get split and feed the 32 input lines, 4 output coax cables for measuring the 32 output lines, an input coax for the

clock and one for the receiver clock. There is also another input clock coax for generating data from a Linear Feedback Shift Resistor (LFSR). There are a few multiplexers and buffers on the board. There are a few more chips such as a TTL to CMOS converter and a divide by 8.

There are a few buffers as well as line filters for the signals coming from the PC to protect against noise in the lines. The board is expected to operate at a frequency of 50 MHz with the clocks operating at almost 200 MHz frequencies.

The board was quite difficult to place and route since the placement of the components was critical and a number of lines (the high-speed lines) had to be routed manually. Also the 190-pin connector at the edge of the board is a high-density surface mount connector with pins on either side of the board. It was very difficult to get any "vias" close to the connector so an effort was made to keep the traces on the top and the bottom signal layers as much as possible. The 64 pin headers for the input and the output port had to be placed very close to the 190-pin connector. They were placed in two rows of 32 headers each. Since they were though hole components they made the routing all the more difficult.

An effort was made to keep the traces short and straight, at least the high speed traces. Because of the restrictions on a number of traces most of the routing had to be done manually.

Shown in the following figures is the layout of the board. The first two figures show the placement of the components on either side of the board. The third figure is the actual photograph of the board after fabrication and population.

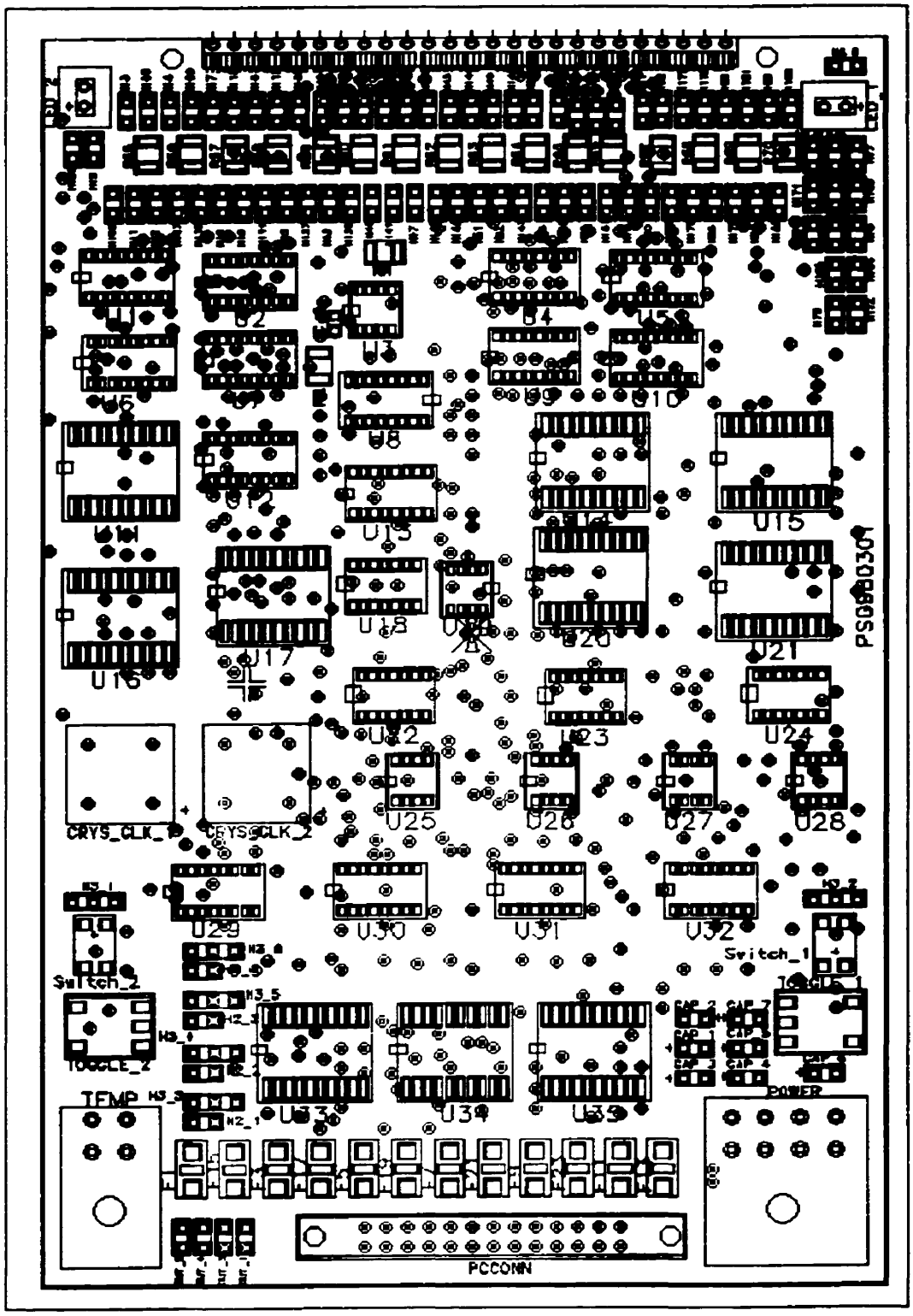

Figure 64: Front Side of the Mother Board

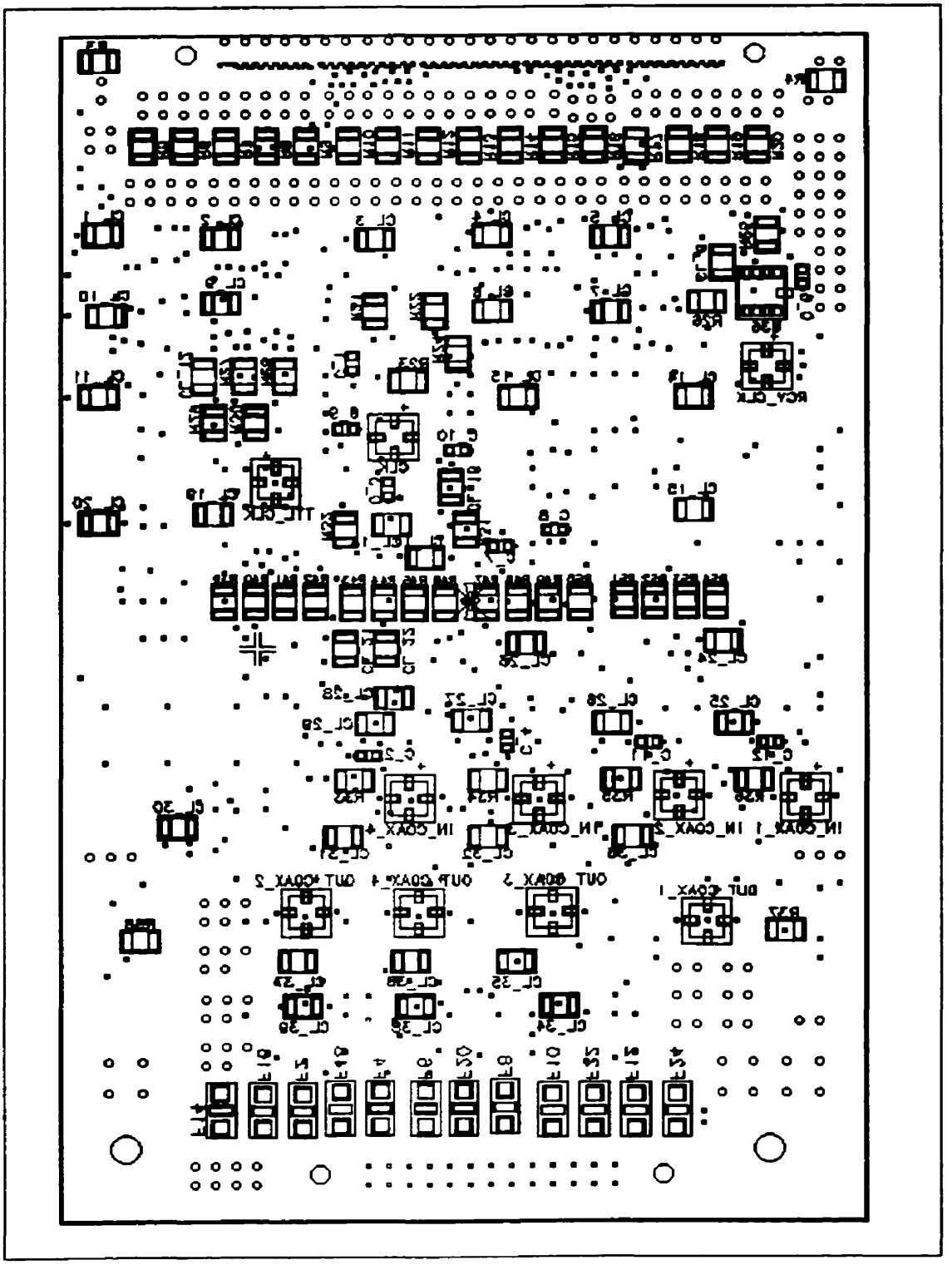

Figure 65: Back Side of the Mother Board

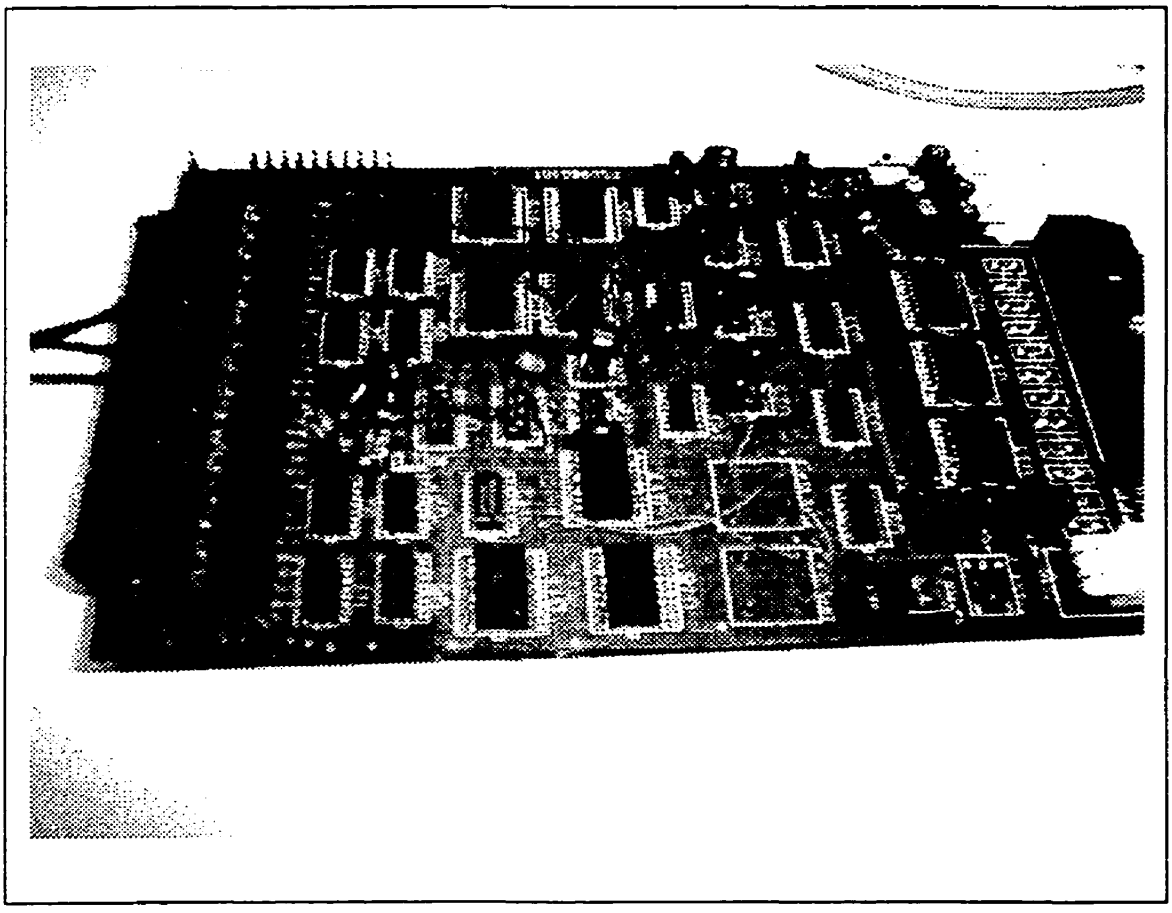

Figure 66: Photograph of the Populated Mother Board

6.5 Conclusions

The packaging module for this demonstrator has been characterized both thermally and electrically. It seems to satisfy the electrical, thermal and opto-mechanical packaging requirements. The system is not package bandwidth limited, and is able to effectively dissipate the expected chip power without sacrificing the QCSE performance. The mother board has the capability of driving all the inputs on the chip as well the power connections. It also has monitor ports for viewing the outputs from the chip. Using four package modules with the chips on them and four mother boards, the system can be

interfaced to the optical interconnect which is being designed in parallel by other members of the PSG. This project is due to finish in the month of June 1998.

6.6 References

1) Brian Robertson, "Design of a Compact Alignment-Tolerant Optical Interconnect for Photonic Backplane Applications, "Proceedings of the Fourth International Conference on Massively Parallel Processing Using Optical Interconnection, June 22-24, 1997, Montreal, Canada, IEEE Computer Society.
2) David R.Rolsron, B.Robertson, H.S.Hinton and D.V.Plant, "Analysis of a micro-channel interconnect based on the clustering of smart-pixel device windows", Applied Optics, 1996, vol. 35, pp. 1220-1233.
3) Howard W. Johnson, Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993.
4) Data Sheet, Epo-Tek, H20-F, Electrically Conductive, Silver Epoxy, Epoxy Technology Inc.
5) Frigichip Thermoelectrctric Cooling Devices, Thermoelectric Handbook, Melcor Thermoelectrics, 1995.
6) LDT 5910B Instruction Manual, Thermoelectric Temperature Controller, ILX Lightwave, June 20, 1997.
7) Lab-NB data acquisition board manual, National Instruments, 1995.

Chapter 7: Characterization of a single VCSEL in a TO46 can package

7.1 Introduction

The acronym VCSEL stands for a Vertical Cavity Surface Emitting Laser. This chapter deals with the high speed characterization of a VCSEL from Honeywell Micro-Switch. This VCSEL is encased in a TO46 Can package and can be modulated to multi gigahertz frequencies. The purpose of this exercise was to get familiar with the VCSEL technology and to acquire expertise with driving VCSELs properly. This included high speed testing and characterizing of a high data rate source that can have multiple uses, which involved observing the eyepatterns of the detected signals at multi gigahertz frequencies and also measuring the 3dB bandwidth of the laser.

7.2 Theory of a VCSEL

For a VCSEL, just like any other laser, it is the LI curve that is significant[1,2]. The LI-curve is the plot of the Light Intensity vs the Current injected into the VCSEL. The power is a function of the input current. The LI curve of the Honeywell VCSEL is as shown in the figure 67. The power is insignificantly small till the current reaches a specific value known as the threshold current and then the relationship between power and the current is almost linear. If the current is increased beyond a certain limit the LI curve is no longer linear. For small signal high frequency characterization the laser has to be biased above threshold, somewhere in the middle of the linear portion. This is because it is in this region that there is the most variation in the light intensity corresponding to a certain modulation current swing.

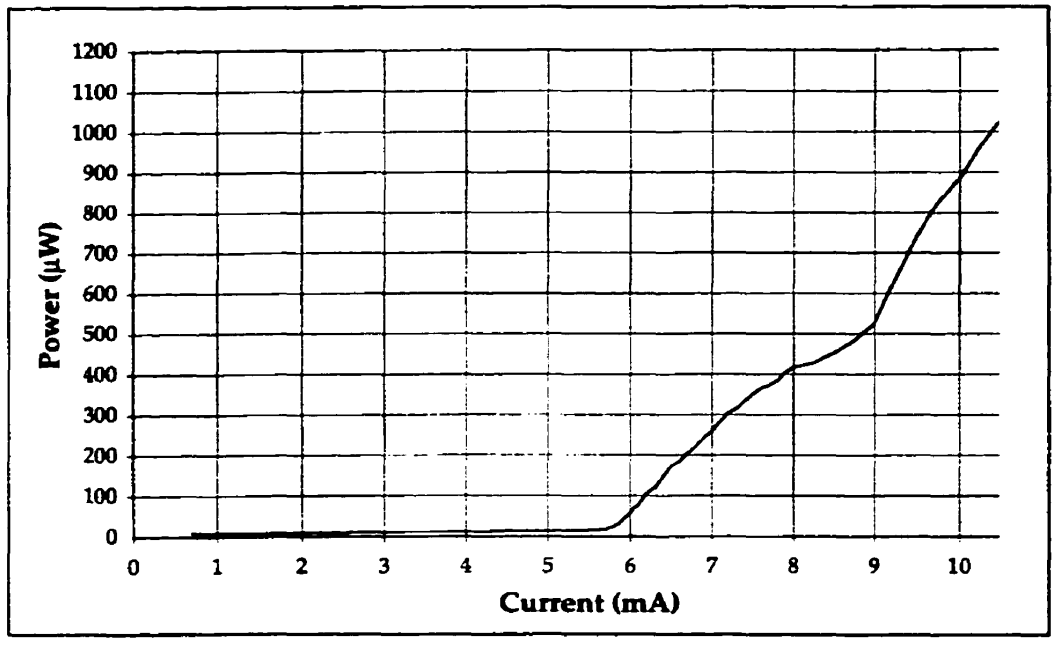

Figure 67: LI Curve of the Vertical Cavity Surface Emitting Laser Diode

The I-V Characteristics of the VCSEL are as shown in the following fig: This curve helps us in determining the DC characteristic impedance of the laser diode.

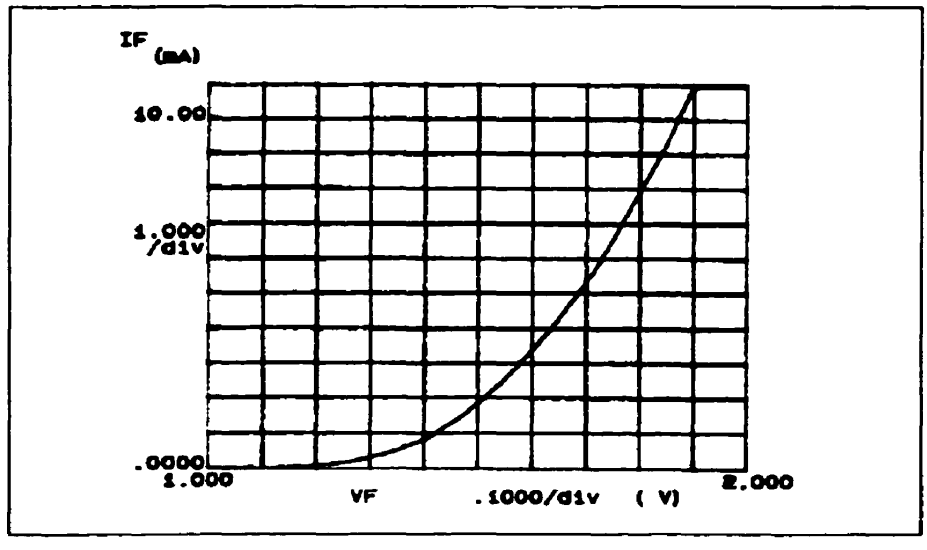

Figure 68: IV Characteristics of the Vertical Cavity Surface Emitting Laser Diode

The magnitude of the modulation and the biasing currents are such that the VCSEL is always biased above threshold and in the linear region of the L-I curve for that VCSEL. Whether the bit is low or high the VCSEL is biased above threshold. This is important otherwise there would be a distortion in the detected beam because of the turn on delay in the VCSEL. The turn on delay is the delay of a semiconductor laser to attain a steady state output optical power as the bias current is increased from zero to above threshold. Thus there is a delay between the current reaching the threshold value and the laser emitting a steady state optical power[1]. The delay time as a function of threshold current and the bias current for a semiconductor laser is given by the following equation.

$$t_{Delay} = \tau\left(\frac{I_{th}}{I}\right)^{1/2}\left[\tanh^{-1}\left(\frac{I_{th}}{I}\right)^{1/2} - \tanh^{-1}\left(\frac{I_O}{I}\right)^{1/2}\right]$$

Thus if the low or the high input corresponds to off or saturation current values there is a distortion introduced in the output beam. If the input beam is square wave, the output looks much more rectangular which decreases the bandwidth of the VCSEL source.

7.3 Description of the Custom Package

The requirements for driving a VCSEL are to provide current biasing and current modulation at the VCSEL input. It is not possible to do this with a regular power supply since they are voltages sources only. It is essential to have a VCSEL driver that translates this voltage to current. For this purpose a board was designed that had the capability of translating the dc bias voltage to bias current. The modulation was still a voltage modulation. The figure below shows a schematic diagram of the circuit on the board:

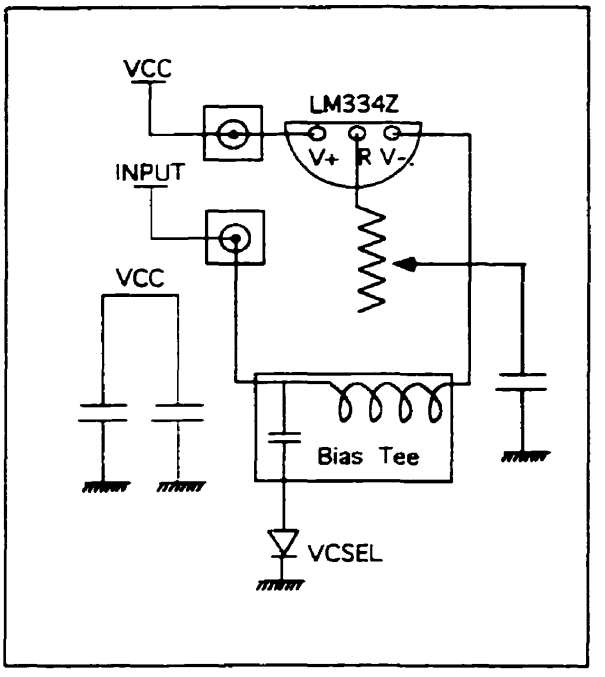

Figure 69: Schematic Block Diagram of the VCSEL Driving Board

Also shown is a snapshot of the board designed for this characterization. The board had a number of useful mounting features which enabled the board to be either used in telecentric systems using Spindler and Hoyer opto-mechanical hardware or with a slotted base plate. The shape of the board was such that the VCSEL formed the center of a 25mm diameter circle on the board. There were special 25 mm diameter barrels machined to go with the board. These could be mounted on the back of the board using four screws. These barrels fit into standard 25 mm Spindler and Hoyer (S&H) setups and helped to mount the VCSEL in the center of the S&H setups. This facilitated the use of lenses with this board for collimating and focussing the optical beam output from the VCSELs. Also this barrel was made from magnetic steel which enabled the use of the board with slotted base plates. The board was held vertical by this barrel which was held fast by the magnets in the slots of the base plate. This VCSEL could thus act as a modulated

source for the applications that are to be built on a slotted base plate. The board could thus be mounted as required by any particular application. The following a picture of the populated board along with the mounting barrel.

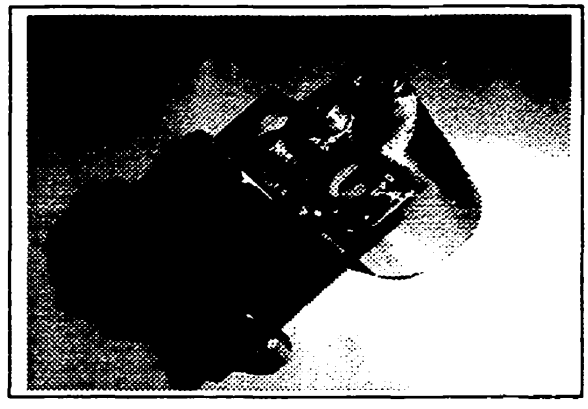

Figure 70: Photograph of the VCSEL Driving Board

7.4 Experimental Results

Using this board, the VCSEL could be biased very precisely and if the voltage swing of the modulation was kept small enough, the VCSEL could be made to operate in the linear portion of the L-I curve. The following pages show the waveforms and the eye patterns for different bias currents, different voltage swings and different frequencies of modulation.

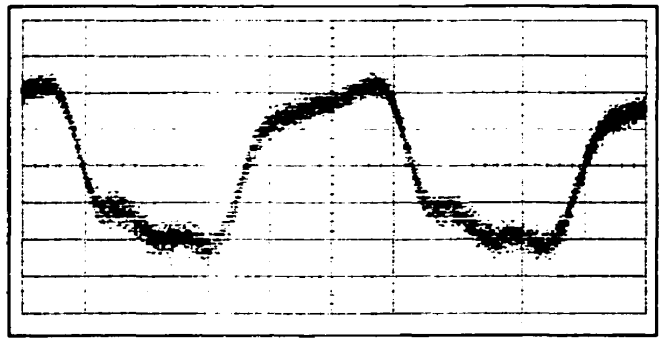

Figure 71: The Modulated output from the VCSEL at 500Mbps

The figure above is the waveform from the detector when the VCSEL was being modulated at 500 Mbps frequency with PRBS of 2^23-1. The bias current was 7mA and the modulation voltage swing was 100mV. Shown below is the eye pattern for the same biasing and modulation conditions.

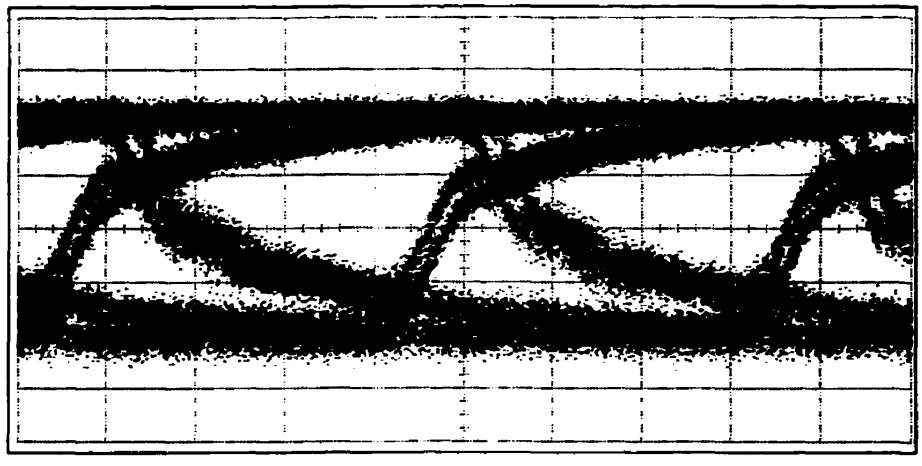

Figure 72: The Eye pattern of the Modulated output from the VCSEL at 500Mbps

The following two figures are similar to the figures shown above. The difference is, here the modulation frequency is 1Gbps instead of 500Mbps. The bias current and the modulation voltage are still 7mA and 100mV respectively. As can be seen from the figure the eye is open even at 1Gbps.

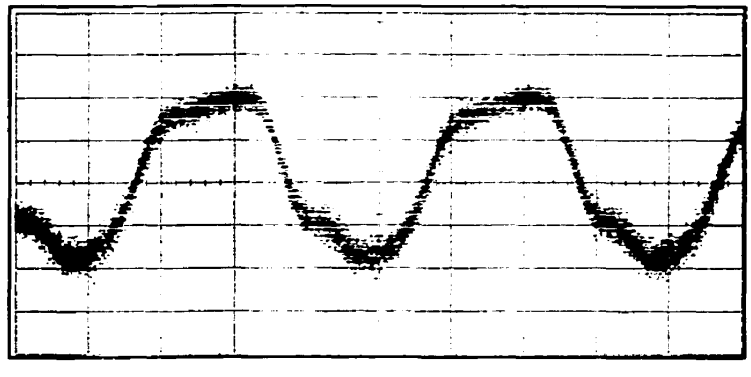

Figure 73: The Modulated output from the VCSEL at 1Gbps

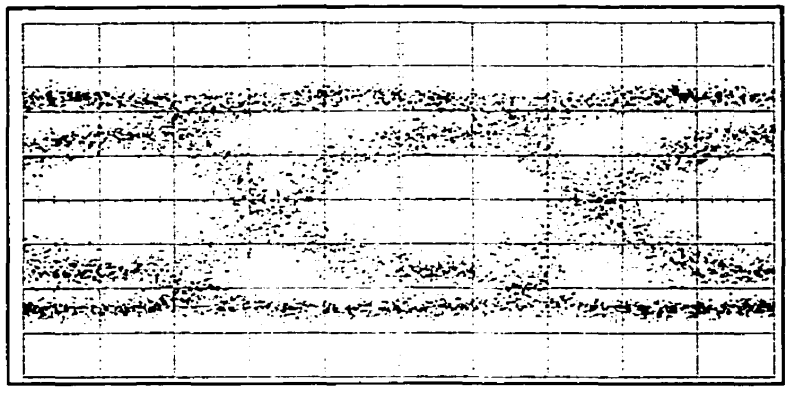

Figure 74: The Eye pattern of the Modulated output from the VCSEL at 1Gbps

These measurements were taken for frequencies ranging from 50Mbps to 1Gbps. They show the performance of the VCSEL as a high frequency modulated output source for various optical and optoelectronic applications [3]. The other measurements included small signal 3dB measurements using the network analyzer, the 2.5 GHz photodetector from ANTEL Optronics (ARX-SA) and a digitizing oscilloscope from Hewlett Packard (HP54120). This scope has a bandwidth of 20GHZ thus the limiting factor were the VCSELs and the photodetector. The network analyzer was calibrated with the VCSEL biased above threshold and the photodetector receiving continuous wave instead of modulated output from the VCSEL. When the VCSEL is modulated by the output from the network analyzer and the detected signal from the photodetector is fed back to the network analyzer, the 3 dB bandwidth of the VCSELs can be measured. The experimental setup for doing this is shown in the following figure

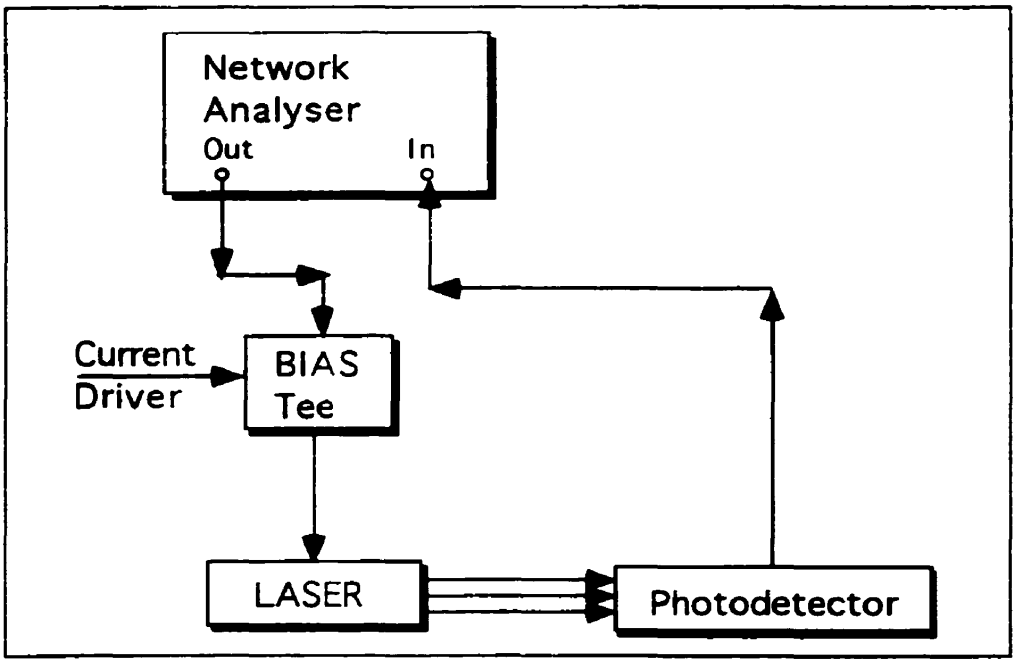

Figure 75: Experimental Setup for 3dB Measurements

The experiments conducted with the network analyzer yielded a 3dB bandwidth of 2Gbps. Since the 3dB for the photodetector is around 2.5Gbps the 2Gbps reflects the bandwidth of the VCSELs. The plot for the 3dB measurements is shown in the next figure

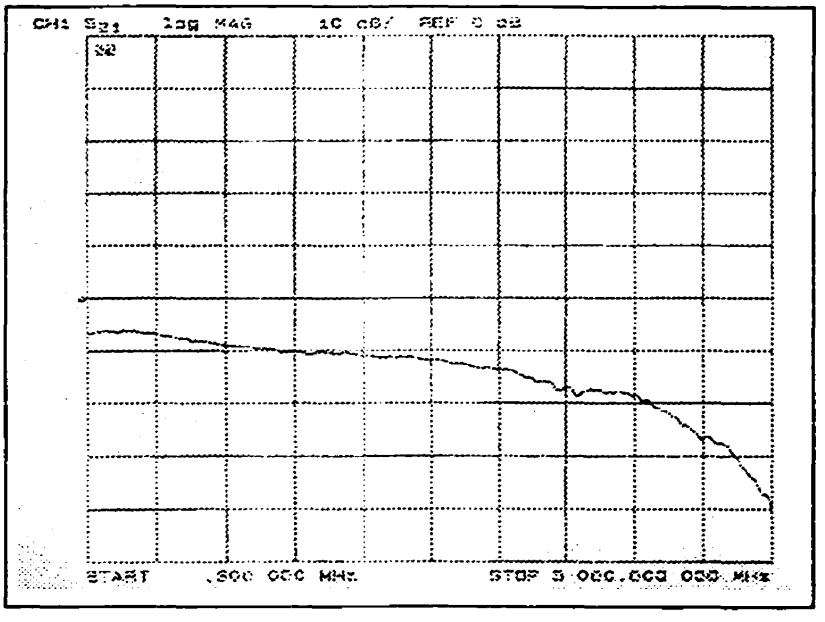

Figure 76: Measurement of the 3dB Modulation Bandwidth of the VCSEL

7.5 Conclusion and future work

This chapter has described the design and characterization of a package for driving a VCSEL in a TO46 can at muti-gigihertz frequencies. The experiments show the performance of a high frequency modulated optical data source that can be used for many different applications requiring a single optical beam. One such application might be for the characterization of photodiodes as discussed in chapter 4.

The experimental results have shown that the VCSEL can easily be modulated to a Gbps and the "eye" is still almost open. The 3dB measurements show that the optical power falls to half its intensity at about 1.5GHz. Thus, beyond the 3dB frequency the VCSEL could definitely not be used as a source especially in the package that was used for these measurements. The 3dB bandwidth width could be that of the VCSEL itself or of the package housing it. Since the package was calibrated out for these measurements, it is most likely the 3dB bandwidth of the VCSEL itself. This work shows the use of current biasing for driving VCSELs and in the future it can be expanded to current biasing as well as current modulation. Rather than using discrete components for driving the VCSELs on chip driver circuitries can be designed so that the modulation bandwidths are as high as possible for any given VCSEL.

7.6 References

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2) B.E.A.Saleh, M.C.Teich, "Fundamentals of Photonics", A Wiley-Interscience Publication
3) Rodney S.Tucker, "High Speed Modulation of Semiconductor Lasers", Journal of Lightwave Technology, Vol. LT-3, No. 6, December 1985, pp. 1180-1192.

Chapter 8: Characterization of an array of 2x10 VCSELs

8.1 Introduction

This chapter deals with the characterization of a 2 x 10 array of VCSELs from Nippon Telephone and Telegraph (NTT). This characterization involved similar measurements as the single VCSEL dealt with in the previous chapter [1,2]. This involved a more complicated scenario of having an array rather than a single VCSEL [3]. Thus there were the issues of crosstalk and temperature. The temperature of the die substrate of the VCSELs had to maintained at a fixed value. In the package for these VCSELs active temperature control had to be incorporated. In this package it was decided to have both current biasing as well as current modulation to activate the VCSELs.

The chapter will first show some measurement results using voltage biasing and voltage modulation for the VCSELs. These resulted in the decision to design a custom package for current biasing and current modulating arrays of VCSELs. This package is then described in the next few sections along with the characterization of the VCSELs using this package. The characterization involves modulating the VCSELs at high frequencies and observing the eye patterns for performance. A clear eye would indicate a very low bit error rate and hence acceptable transmission of data. It also involves 3dB bandwidth measurements which tell the maximum modulation frequencies these VCSELs can be operated at with reasonable performance. In this characterization a small signal model of the VCSELs was also developed to calculate the 3dB bandwidth of the VCSEL and to co-relate it to the measured value. This proves the validity of the small signal model.

8.2 Voltage Biasing and Voltage Modulation of the VCSELs

The 2 x 10 array of VCSELs were not packaged and in bare die form. Initially they were put on an existing board and a series of measurements (similar to the ones described in the previous chapter) were conducted using voltage biasing and voltage modulations. Since the VCSELs were being biased using voltage, the exact point of biasing was impossible to know and hence there was the associated uncertainty with the point of biasing the VCSELs. This is because although the I-V characteristics give you the current corresponding to the voltage the current is based on the DC impedance of the VCSEL. The impedance of a VCSEL modulated at high frequencies in much lower. It was then decided to build a custom package that could provide current biasing and current modulation at high multi-GHz frequency ranges. A few critical measurements taken with voltage biasing and voltage modulation are shown in the following two figures. These are taken at modulation rates of 100Mbps and 500Mbps respectively. The degradation in performance at 500Mbps is obvious.

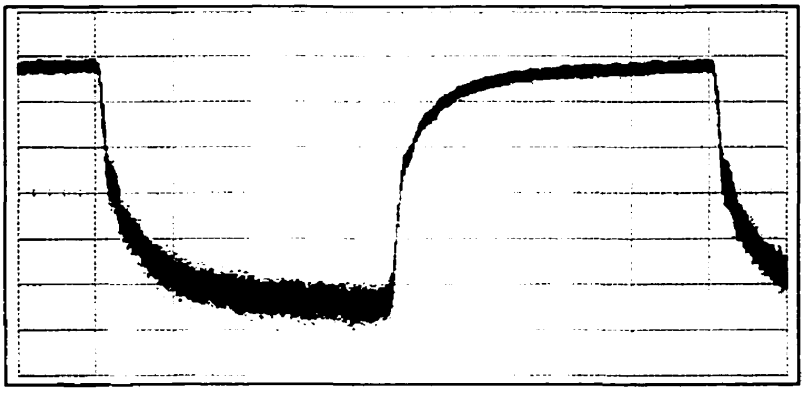

Figure 77: The Modulated output from the VCSEL at 500Mbps

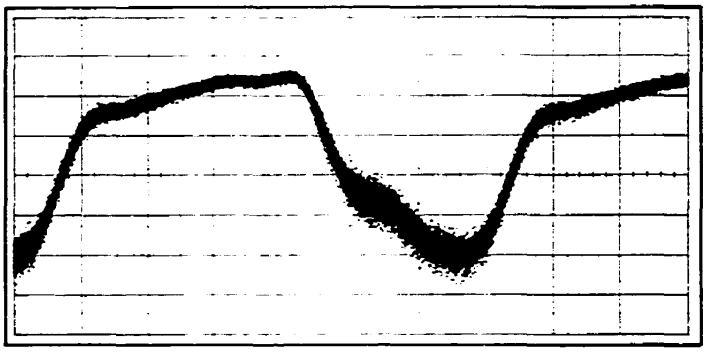

Figure 78: The Modulated output from the VCSEL at 1Gbps

8.3 Description of the Custom Package for Current Biasing and Current Modulation

There are many issues involved in designing a package capable of multi-gigahertz operation [4]. A custom package was designed to drive the VCSELs using current biasing and current modulation. For this purpose special driver chips were used having the capability of modulating the VCSELs up to 2.5Gbps. These chips are VSC7925 bought from Vitesse Semiconductors Ltd. and have the capability of supplying bias current in the range of 2-50mA and modulation current in the range of 2-50mA. The designed board can accommodate eight of these chips. Most of the VCSELs that were to be used with the board require small bias currents, the biasing currents are less than 10mA for each VCSEL. Thus each of the Vitesse chips has the capability of driving five VCSELs. In the design of the board, each Vitesse chip output was sent to five pads where five VCSELs could be wirebonded. The Vitesse Chips need to see an approximate impedance of 25-30 ohms at their output for correct operation. Thus, an impedance match has to be provided between the VCSEL and the output of the VSC7925. A series resistance provided was provided in the path from the VSC7925 to the VCSELs for this purpose.

The NTT VCSELs had a characteristic impedance of about 35 ohms at DC and hence no matching was needed for operation at high frequencies if only one VCSEL was operated by one VSC7925. If more than one VCSELs are operated in parallel, the characteristic impedance decreased and a corresponding series termination resistor was required. The value of the series resistor changes with the number of VCSELs being operated by the same VSC7925. The series impedance is approximately 10 ohms for the case one VSC7925 being used for two VCSELs and approximately 13 ohms for it driving three VCSELs. This is because as the number of VCSELs operating in parallel increases, the resultant impedance decreases. To make the impedance looking into the VSC7925 25 ohms the series resistance has to be increased.

The board has a mounting surface in its center where the VCSEL chip can be attached using conductive epoxy. There are 40 wirebond pads around the chip mount area for connecting the output of the VSC7925 to the VCSELs. Each VSC7925 goes to five of these wirebond pads and can thus drive five VCSELs. The pads are interlaced as shown in the following figure.

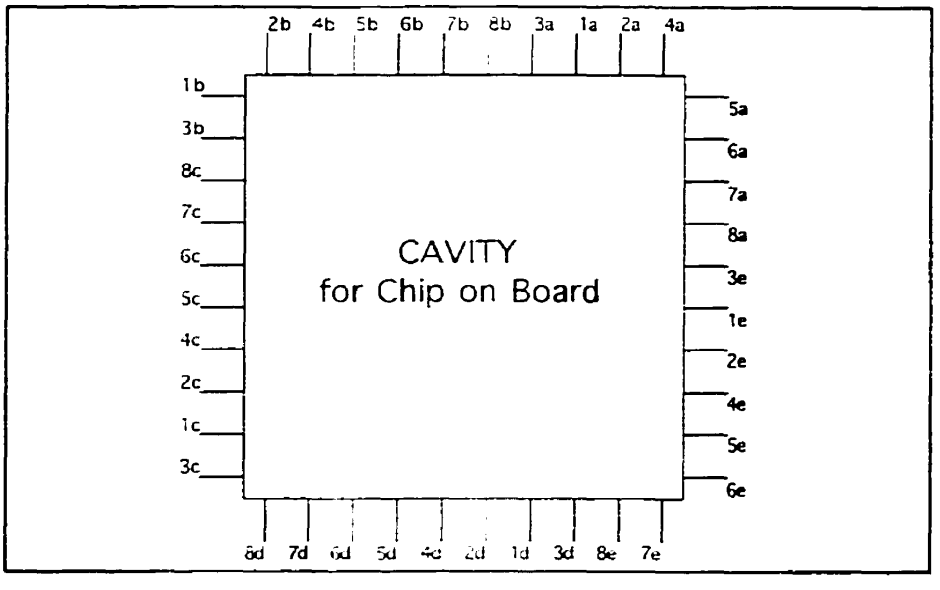

Figure 79: The Arrangement of the bonding pads on the VCSEL Driver board

There is provision for temperature control of the chip on this board. For active temperature control, a thermistor can be mounted on the back of the VCSELs behind the board along with a Thermo-Electric (TE) cooler and a heat sink. There is a thermal and electric connection between the top and the bottom of the board around the chip mount area because of a large number of thermal vias shorting the two sides together. The TE cooler then controls the temperature of the die substrate using the thermistor in a feedback loop. The heat sink helps in dissipating the heat removed from the die substrate into the surroundings.

Shown below is the pin diagram of the VSC7925 and the rest of the circuit diagram for driving any one of the VCSELs. This is repeated eight times on the board.

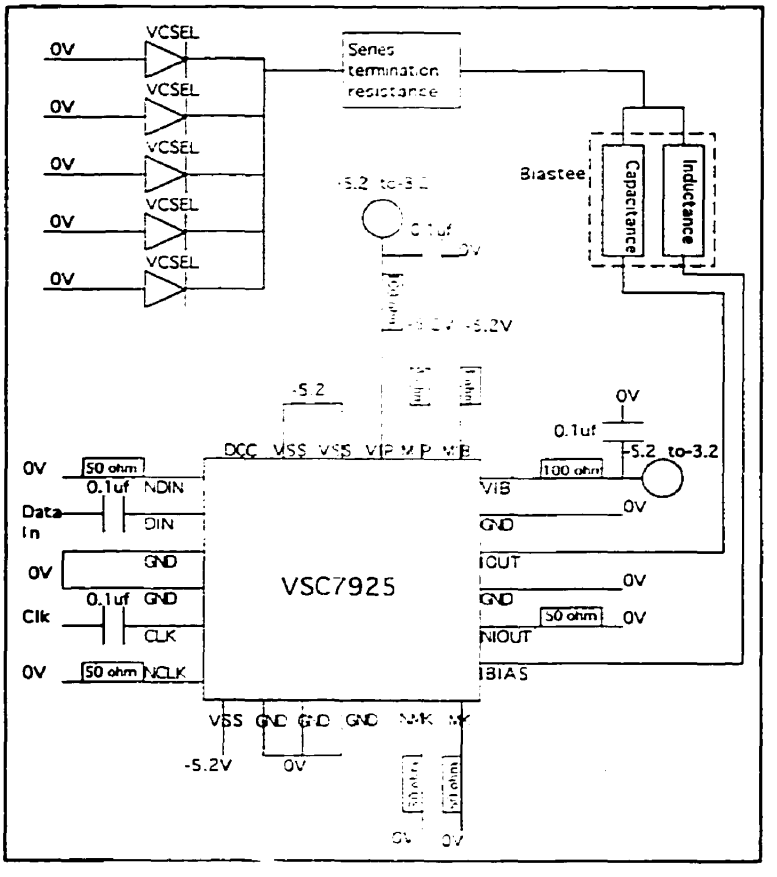

Figure 80: The Block Diagram Schematic of the VCSEL Driver Board

The figure below shows a block diagram schematic of the VSC7925. The chip controls the current by using a current mirror like configuration along with a differential pair of FETs. The two pins VIB and VIP control the bias current and the modulation current respectively. By changing the voltage at these ports the current can be changed.

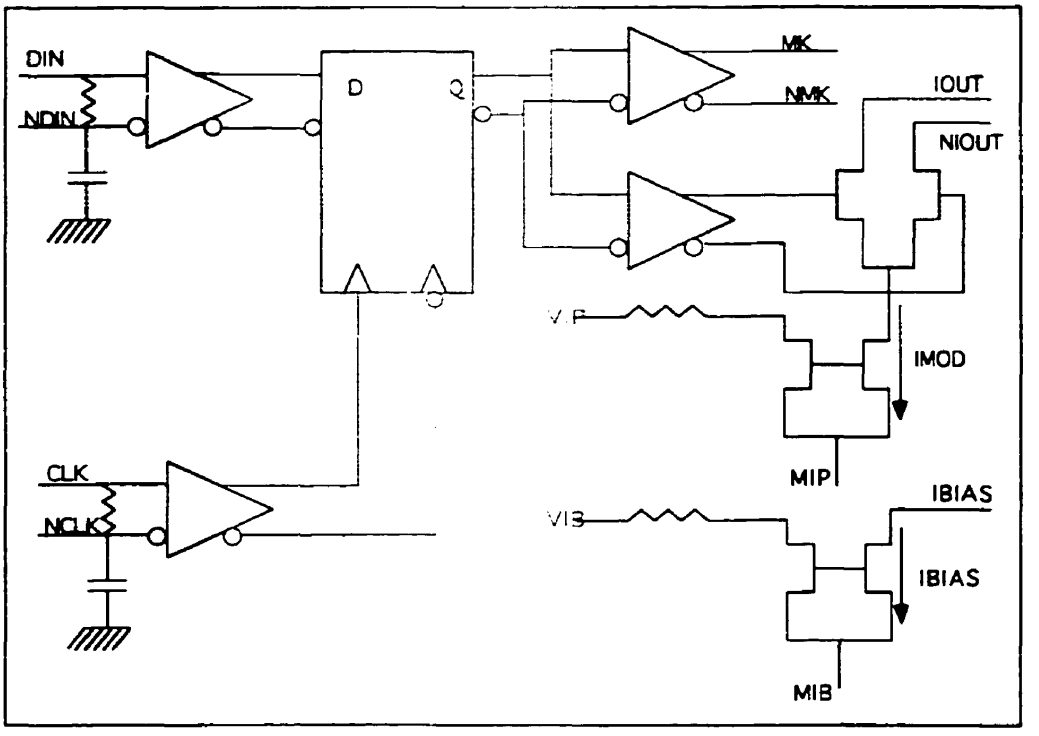

Figure 81: Block Diagram Schematic of the Laser Driver Chip - VSC7925

Shown in the figures below is a snapshot of the board from both the sides. For characterizing the board it was essential only to populate one "corner" of the board along with a VCSEL array and this is shown in the figure 82.

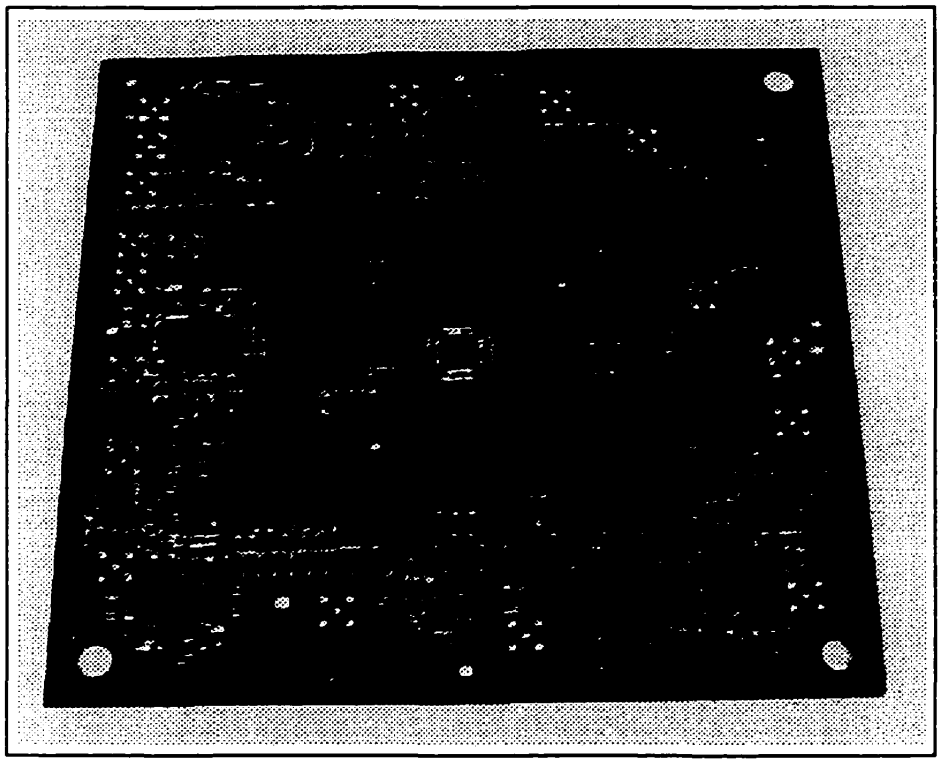

Figure 82: Photograph of the front of the VCSEL Driver Board

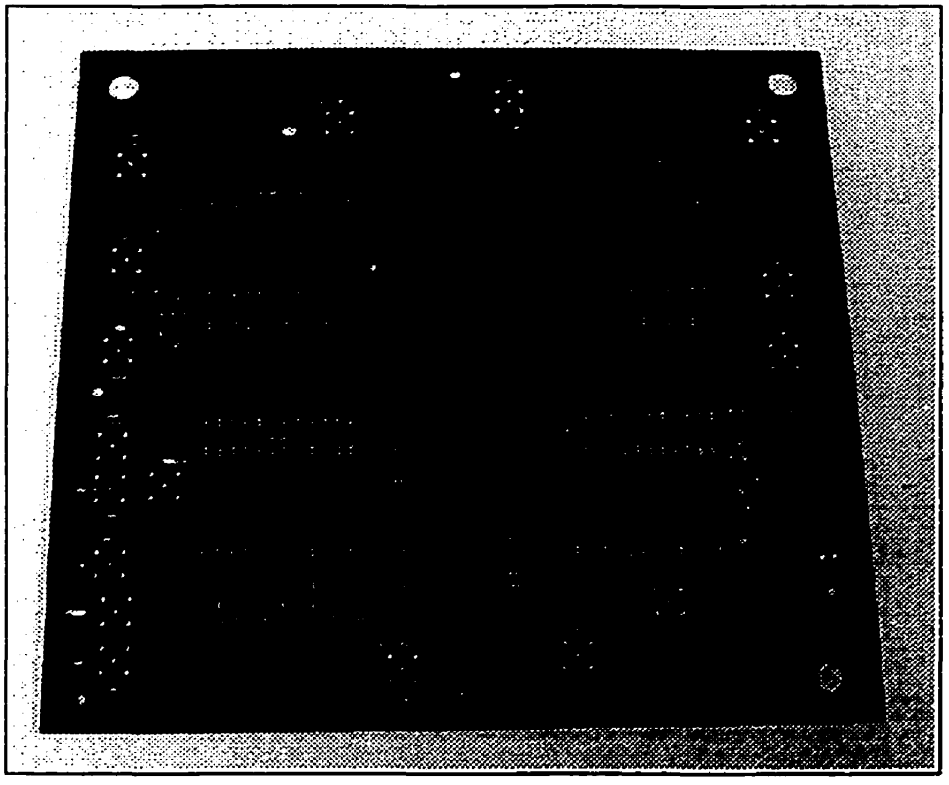

Figure 83: Photograph of the back of the VCSEL Driver Board

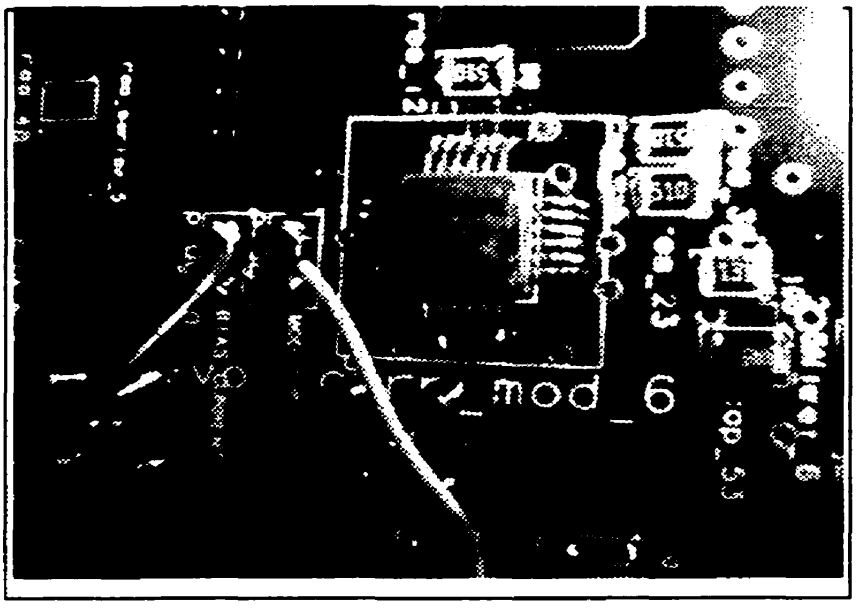

Figure 84: Photograph of the populated corner of the VCSEL Driver Board

8.4 Experimental Results

The following sections discuss the results of using this board to characterize the 2 x 10 array of VCSELs from NTT.

8.4.1 I-V Characteristics

The following are the I-V characteristics of the VCSELs obtained with the help of a parameter analyzer. These show that the DC characteristic impedance of the VCSELs is in between 35 and 38 ohms. Thus for driving only one VCSEL no series resistance was required in the path between the VSC7925 and the VCSEL.

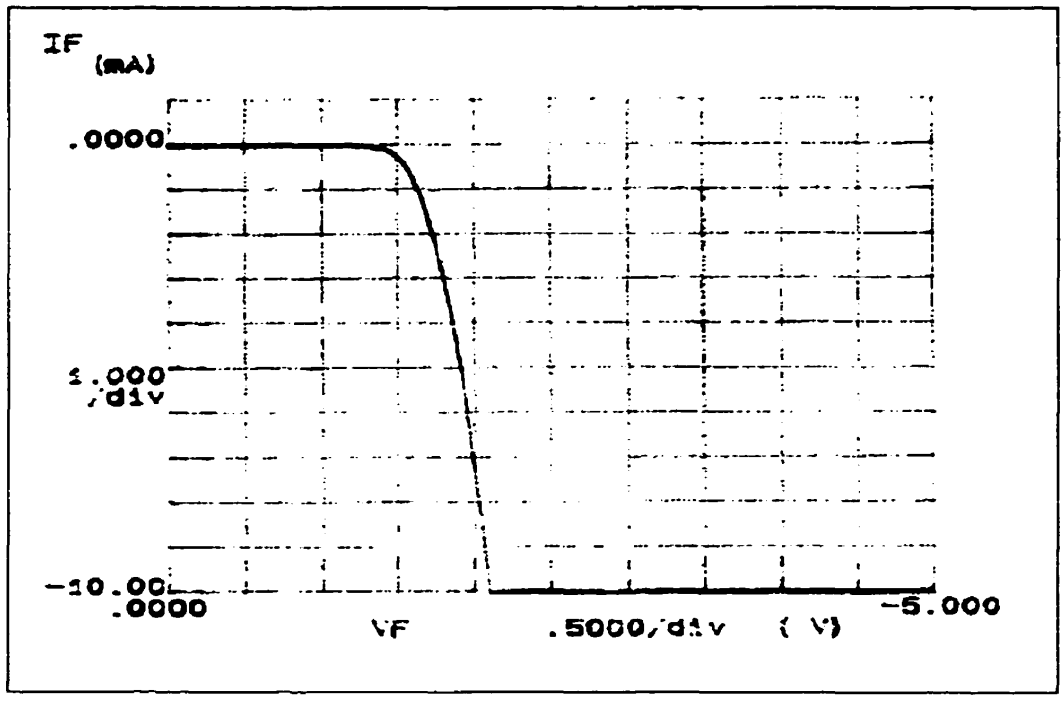

Figure 85: IV Characteristics of the VCSEL Diode

8.4.2 L-I Curves

The following is the L-I curve of the VCSEL. This was taken by varying the bias current from 2mA to 12mA.

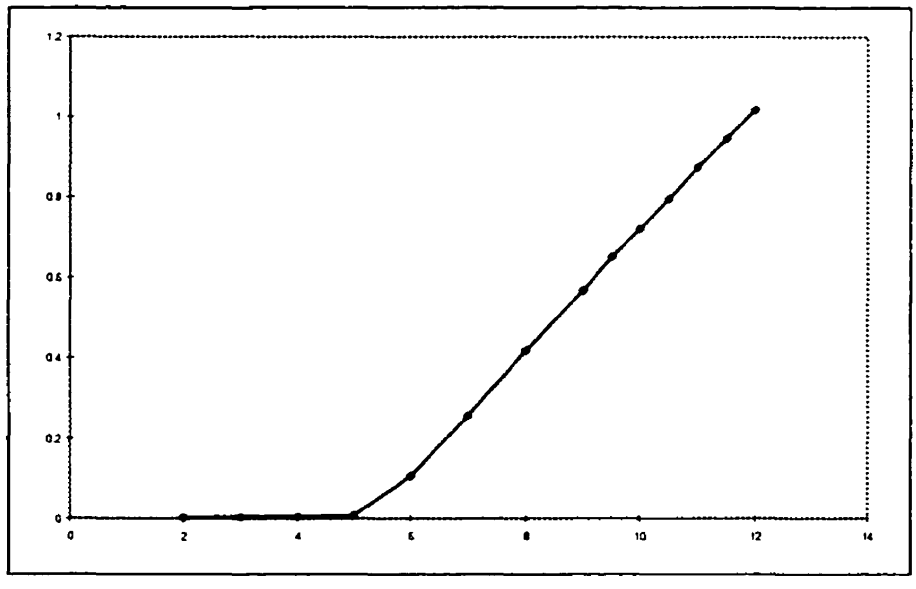

Figure 86: LI Curve of the VCSEL diode

8.4.3 High Frequency modulation measurements

The following figures show the waveforms and the eye patterns of the VCSELs biased above threshold and the modulation swing such that the VCSELs were always biased in the linear portion of the L-I curve. Thus the biasing current is in the range of 8.5 mA to 10 mA and the modulation swing is lower than 1 mA. This will ensure that the VCSEL is always biased above threshold and below saturation in the most linear portion of the L-I curve for that particular VCSEL. These curves are for modulation rates of 100Mbps, 500Mbps, and 1Gbps. As can be seen the eye is open even at 1Gbps.

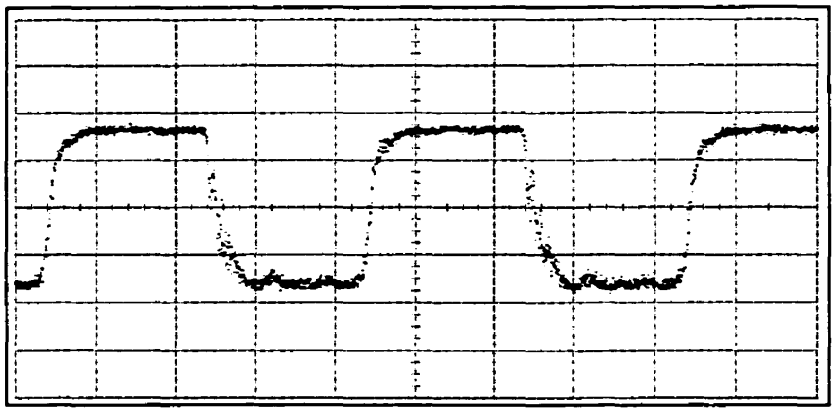

Figure 87: The Modulated Output from the VCSEL at 100Mbps

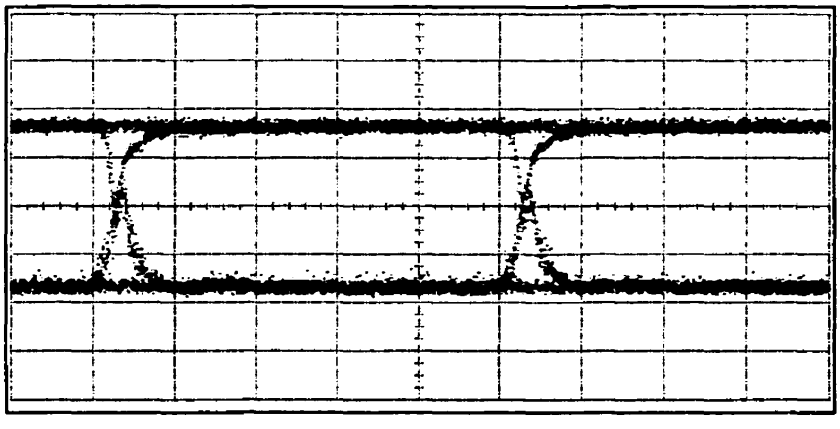

Figure 88: The Eye Pattern of the Modulated Output from the VCSEL at 100Mbps

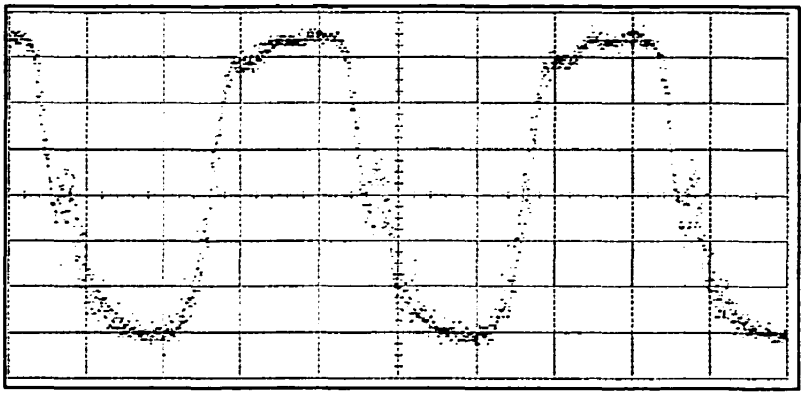

Figure 89: The Modulated Output from the VCSEL at 500Mbps

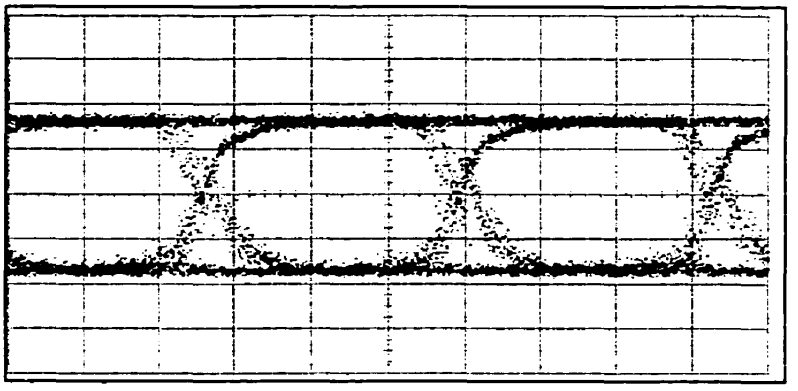

Figure 90: The Eye Pattern of the Modulated Output from the VCSEL at 500Mbps

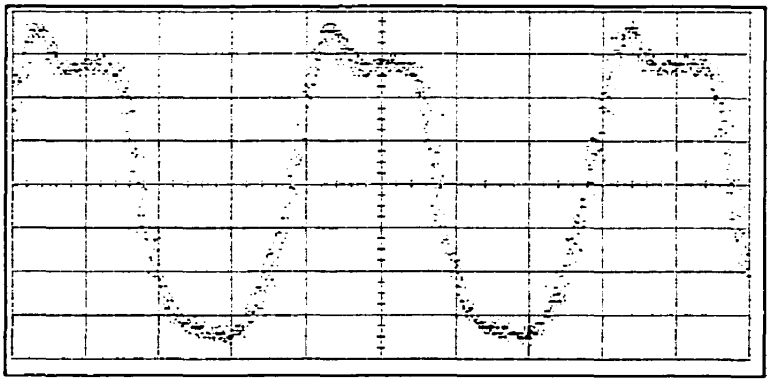

Figure 91: The Modulated Output from the VCSEL at 1Gbps

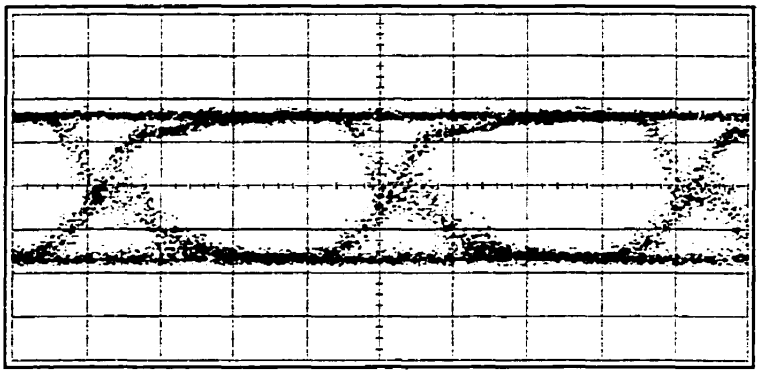

Figure 92: The Eye Pattern of the Modulated Output from the VCSEL at 1Gbps

From these figures it can be seen that the rise time of the waveform is 100ps and the fall time is 130ps. Also the duty cycle can be seen to be almost 50% which is good since the input waveform was a square wave of 1 mA amplitude. The eye patterns were obtained using a pseudo random bit stream of 2^23 –1. These waveforms prove that the bandwidth of the VCSEL source and the package together is at least 1Gbps.

8.4.4 3dB Bandwidth Measurements

The next step was to measure the 3dB bandwidth of the VCSELs [5,6]. The 3dB bandwidth of the VCSELs is a measure of the highest frequency that the VCSELs can be modulated. Since the main application of the lasers is as sources for optical communication systems, the problem of high-speed modulation of their output by the high-data-rate information is of great technological importance. A unique feature of semiconductor lasers is that, unlike other lasers that are modulated externally, the semiconductor lasers can be modulated directly by modulating the excitation current. For this purpose the experimental setup employed is shown in the figure below

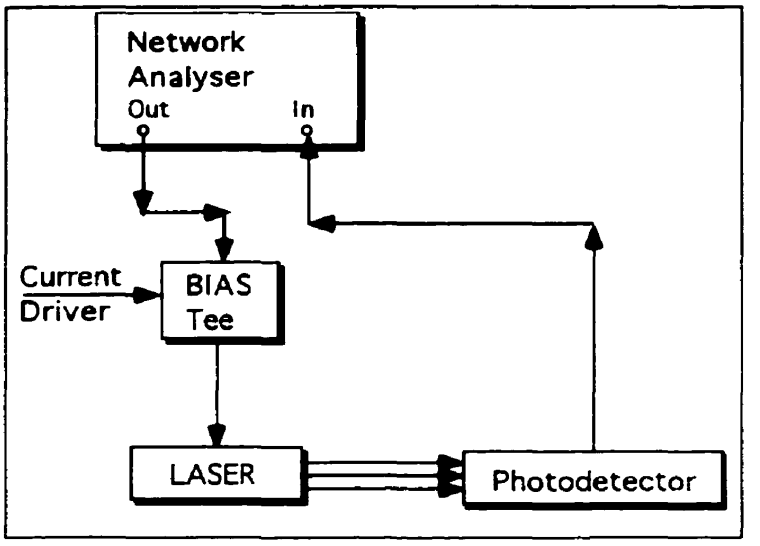

Figure 93: Experimental Setup for 3dB Modulation Bandwidth of the VCSELs

The figure below shows the frequency response measurements done using the experimental setup shown above. For these measurements the package was calibrated out by using a through calibration for measuring the S21 parameter with the network analyzer. If this is not done then the measurements will be limited by the bandwidth of the package.

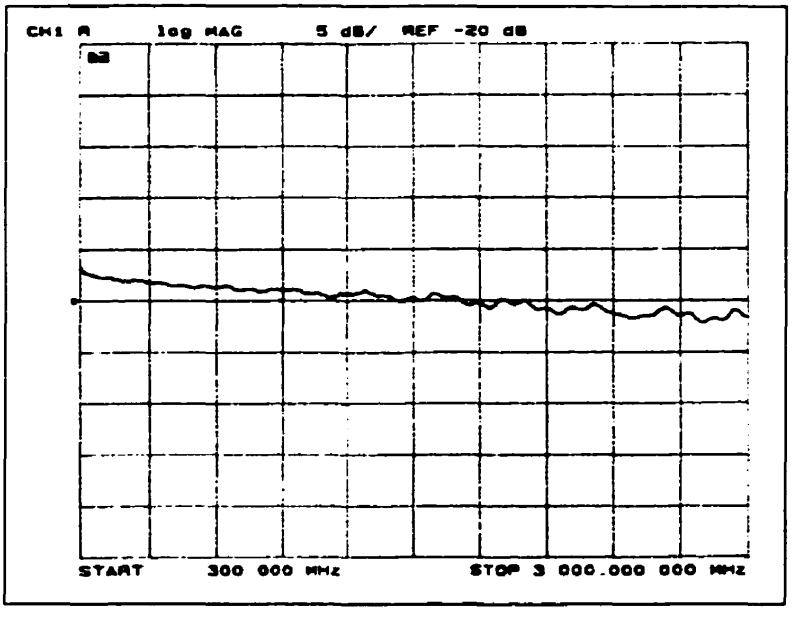

Figure 94: Measurement of the 3dB Modulation Bandwidth of a single VCSEL

8.4.5 Small Signal Modeling of the VCSELs

Small Signal Model of the VCSELs is based on the noise characteristics of the VCSEL and is thus independent of the package [7,8,9,10]. As a result the 3dB modulation bandwidth calculated using the small signal model should only be dependent upon the VCSEL and not reflect the package. Thus, it is a forms a means of comparing the measured 3dB bandwidth to the calculated value and ensure that the performance of the VCSEL is not package limited.

From the figure 94 of the measured 3dB characteristics we see the response of the VCSELs to be almost constant till nearly 3GHz and slightly tapering near the end of that range. Since the network analyzer as well as the photodetector had an upper limit of 3GHz, the test equipment limited the measurements. Typical frequency response curves (estimated curves based on the literature and the measurements for these VCSELs) for VCSELs are shown in the following figure 95 [5].

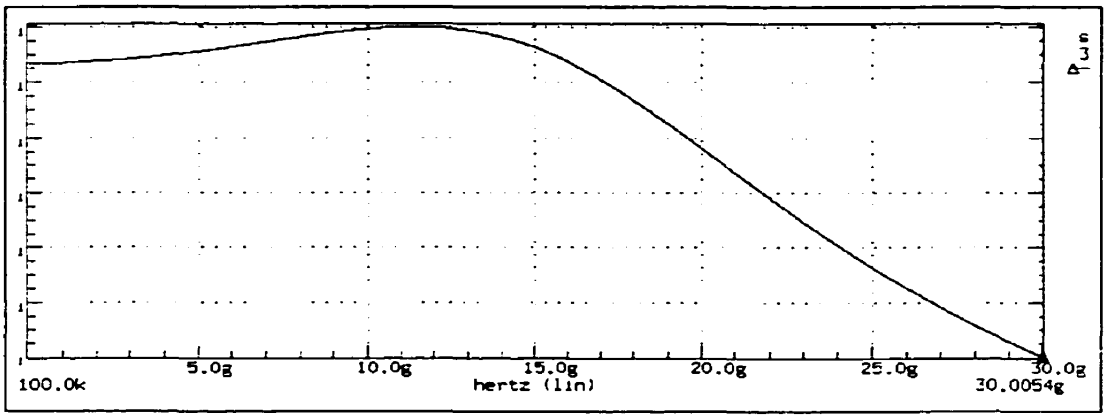

Figure 95: Typical Modulation Response curve for a VCSEL

The purpose of this exercise was to develop a small signal model for the VCSELs. This could be used for similar chips to find out the approximate 3dB bandwidth of the VCSELs. Also other analysis could be performed on the performance of the VCSELs once the small signal model had been obtained. A simple model for VCSELs is as shown in the

following purpose. The problem is to find the values of the various parameters that form this model.

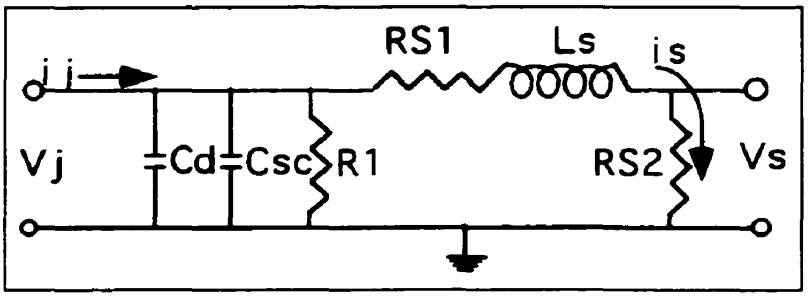

Figure 96: Small-Signal Model for the Vertical Cavity Surface Emitting Lasers

In this model the various parameters are:

C_d is the diffusion capacitance

L_s is the small signal photon storage

C_{sc} is the space charge capacitance of the junction

R1, R_{s1} and R_{s2} are the damping resistances

For the small signal model another useful measurement is the relative intensity noise (RIN) spectrum of the VCSEL biased above threshold [11]. The peak of this corresponds to the relaxation oscillation frequency of the VCSEL at that particular bias current. For this purpose a high frequency spectrum analyzer was needed but was unavailable. For the purpose of modeling, based on the literature available, the expected curves are shown in the following figure. The two curves are for two different values of the bias current.

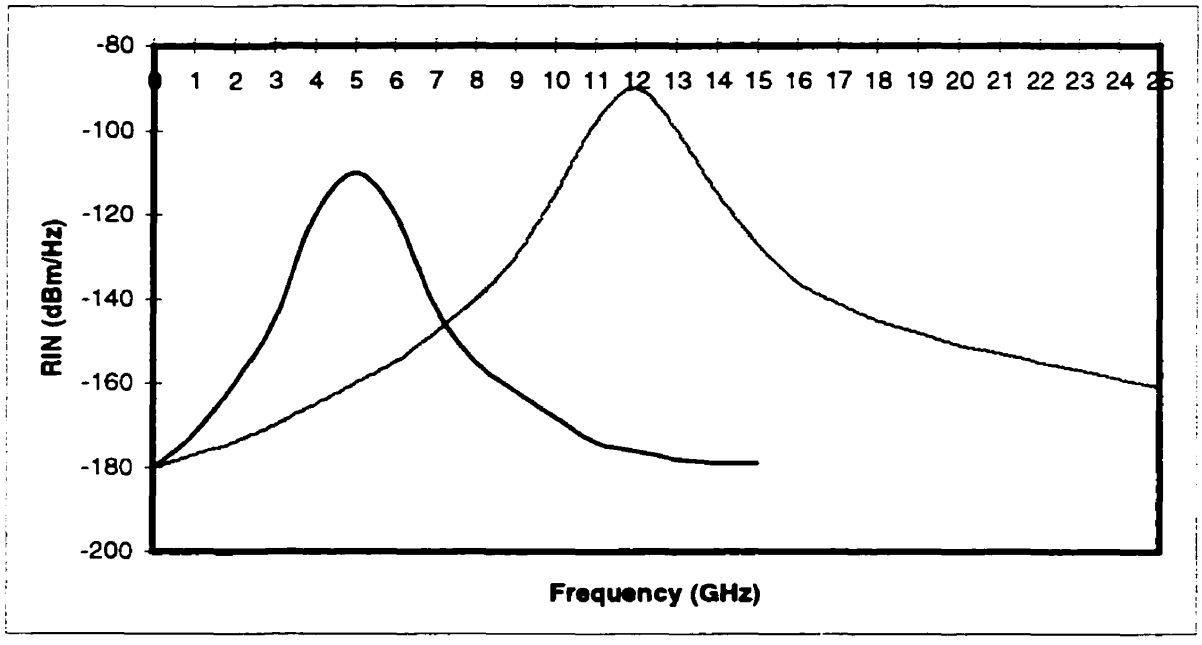

Figure 97: Relative Intensity Noise for a Typical VCSEL

Using these curves it is possible to build a small signal model for the VCSELs. The relative intensity noise as a function of frequency is given by the following expression[11]:

$$S_{RIN}(\omega) = K_1 \frac{\left[1+\omega^2\left(\tau_e^{'}\right)^2\right]}{\left|\left(\frac{\omega}{\omega_r}\right)^2 + \frac{\omega}{\omega_d} + 1\right|^2} \qquad \text{.....1}$$

where :-

$$\omega_r = 2\pi f_r, f_r = \text{Re}sonanceFrequency$$

$$\omega_d = dampingfactor$$

$$\frac{1}{\tau_e^{'}} = \frac{1}{\tau_n} + \omega_r^2 \tau_p$$

$$K_1 = cons\tan t$$

Also, the frequency of the VCSEL diode alone (not considering the package) is given by the following expression:

$$T(\omega) = K_2 \frac{\left|1+\omega\tau_e'\right|}{\left|\left(\frac{\omega}{\omega_r}\right)^2 + \frac{\omega}{\omega_d} + 1\right|} \qquad \text{.....2}$$

$$\omega_r = \left(\sqrt{C_L L_s}\right)^{-1}$$

where:- $$\omega_d = \left[C_T\left(R_{S1}+R_{S2}\right) + L_s/R_1\right]^{-1}$$

$$1/\tau_e' = 1/R_1 C_L$$

From these two equations it is clear that there is a square relation between them for high frequencies i.e.

$$\omega >> 1/\tau_e',$$

$$\left(1+\omega\tau_e'\right)^2 \equiv 1+\omega^2\left(\tau_e'\right)^2$$

By using HSPICE and curve fitting techniques the values of the parameters in the small signal model are as given in the following table.

S No	Parameter	Value
1	$C_T=C_d+C_{sc}$ = Total Capacitance	150pF
2	R_1 = Damping Resistance	912mohm
3	L_s = Small Signal Photon Storage	0.5pH
4	R_{S1} = Damping Resistance	63.9mohm
5	R_{S2} = Damping Resistance	0.1mohm

Two curves 94 and 95 are in accordance with each other and this proves the validity of the small signal model for the VCSEL. The extrinsic

parasitic effects of the package can also be included in this model. This will give a lower value for the 3dB bandwidth.

For calculating the 3dB bandwidth the expression is as given below:

$$f_{3dB}^2 = 0.5\left\{2f_r^2 - (\omega/2\pi)^2 + \sqrt{\left(2f_r^2 - (\omega/2\pi)^2\right)^2 + 4f_r^4}\right\}$$

.....3

The f_r is approximately 12GHz and w_d can be calculated from the parameters. The calculated 3dB comes out to be approximately 13GHz which is close to the typical curves chosen for these VCSELs. This proves the validity of the small signal model.

8.5 Conclusion and Future Work

This chapter has demonstrated the successful packaging of an array of VCSELs. The package has active temperature control for maintaining the die substrate at any given temperature [12]. It has the capability of modulating 40 VCSELs simultaneously. The modulating frequencies can be in the multi-gigahertz range. A small signal model was developed for the VCSELs. This model was used to co-relate the measured 3dB bandwidth with the value calculated using the small signal model. This is useful to ensure that the measured 3dB bandwidth does not reflect the package but is the modulation bandwidth of the VCSELs. This was found out to be approximately 13GHz. All these measurements reinforce the idea of using VCSELs for emitter based free-space optical interconnects. This is because they have a large modulation bandwidth and can be fabricated in arrays. As they can be integrated with silicon circuitry using flip chip techniques they are the most suited for emitter based opto-electronic chips. This work was an exercise to

drive an array of VCSELs using current biasing and current modulation at high modulation rates. The next step would be to design on chip VCSEL drivers and modulate the VCSELs using them instead of discrete components as in this case.

8.6 References

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Chapter 9: Conclusions and Future Work

9.1 Conclusions

This thesis has dealt with a broad range of topics concerning opto-electronics technology with special reference to optical backplanes. It has dealt with the design of opto-electronic chips, and has shown that these chips have special testing, characterization and packaging requirements. Special test rigs for the purpose of testing and characterization of the opto-electronic chips have been demonstrated along with a package for the opto-electronic chips which meets the temperature, bandwidth and connectivity requirements. This surface active chip had 1024 Quantum Confined Stark Effect photodiodes on it. Active temperature control of the die-substrate was incorporated into the chip. The measurements on the package showed that the package could be easily operated at the required clock frequency of 320MHz.

There are other considerations such as power consumption and noise that must be dealt with. This thesis considered Adiabatic CMOS as a possible power saving method for opto-electronic chips. In this technique the voltage swing is divided into N steps. This reduces the voltage drop for each step of charging or discharging while still keeping the net voltage swing constant. This leads to a power consumption of P/N where P is the normal power consumption. Thus power is saved at the cost of the frequency of operation. For noise reduction, optical powering of the chips is considered. Performance limitations are imposed on the high-density arrays by the electrical voltage supply and logic control lines and their associated AC decoupling circuitry. It is therefore desirable to design a system with a minimum of inductive power supply lines that introduce parasitic signals at sensitive locations in the chip. Optical powering removes/reduces the number of inductive power supply lines and hence removes a source of noise in these high density arrays.

The last two chapters of this thesis deal with driving Vertical Cavity Surface Emitting Lasers (VCSELs). The first package described provides current biasing and voltage modulation for the VCSELs. This package yielded a 3dB bandwidth of above 1 Gbps, thus producing a high frequency modulated VCSEL source for a number of applications. The second package discussed deals with a special package designed for an array of VCSELs. This package has the capability of simultaneously driving 40 VCSELs. It has the capability of current biasing and current modulating the VCSELs to high modulation rates of multi-gigahertz frequencies. It also has the provision for active temperature control of the die-substrate by using a Thermo-Electric cooler with a thermistor in a feedback loop. Using a small signal model of the VCSELs based on the noise characteristics and the relaxation oscillation frequency of the VCSELs, the 3dB modulation bandwidth of the VCSELs was calculated to be approximately 13 Gbps.

9.2 Ongoing and Future Work

The 8 x 8 array of Reconfigurable Smart Pixels, the Adiabatic CMOS and the Optically Powered Smart Pixel (OPSP) chips are currently being fabricated. Once fabricated, these will need to be tested in accordance with the testing strategies described earlier. Once the functionality and the performance of the Smart Pixel Array chip has been verified these chips can be used in the design of a polarization bus based optical interconnect for which they were designed.

The Adiabatic CMOS and the OPSP were test structures to prove a concept. They were not for designed for used with any system. Thus for these two structures, extensive testing and characterization needs to be performed. Functionality testing needs to be performed, and power reduction analysis needs to be carried out for ACMOS.

The Phase-3 demonstrator assembly is currently in progress and the demonstrator is expected to be fully functional by August 1998.

Currently the P3 chips are having the photodiodes being flip-chip bonded to them. Once they return they need to be packaged and characterized. The optical test rig will be used for the testing and the characterization of the chips. Finally, the packaged chips will be integrated into the photonic backplane.

The VCSEL sources can be used in the lab for many applications e.g. the optical test rigs, testing of detectors etc. The next step would be design on-chip driver circuits along with the VCSELs so that the chips for the photonic backplanes become emitter based instead of modulator based as is the present situation. This would remove the need of the optical power supply which at present provides the constant power beams for the modulators. This would significantly simplify the design and integration of the photonic backplane.