Low-Power Low-Voltage High-Speed Delta-Sigma Analog-to-Digital Converters

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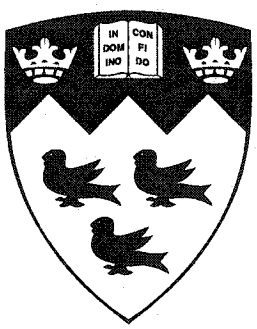

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Abstract

The increasingly stringent requirements of today's communication systems and portable devices are imposing two challenges on the design of Analog-to-Digital Converters (ADC) and delta-sigma modulators (ΔΣM) architecture in particular.

The first is the extension of the input frequency range to include applications where the input bandwidth exceeds the 1 MHz range.

This challenge in extending the operational speed of ΔΣM is further rendered more complicated by the ever shrinking transistor dimension. As predicted by the Semiconductor Industry Association (SIA) Roadmap for CMOS technology, the transistor dimension will reach 0.05 μm in 2011. With this dramatic shrink in the transistor length, and as a result in the supply voltage, device modelling becomes ambiguous and circuit non-idealities more pronounced. The design of the main analog building blocks that minimize the time-to-market is therefore becoming very complicated.

These two issues will be addressed in this thesis, namely a new design method that will minimize the design cycle of delta-sigma analog-to-digital converters (ΔΣ ADCs) intended for high-speed applications. This method will be demonstrated efficient in the implementation of two state-of-the-art modulators in terms of performance using a widely adopted figure of merit.

The validity of the top-down design methodology was verified through the fabrication of two prototype integrated circuits (ICs), both in TSMC 0.18 μm CMOS technology. In the first chip, a single-bit, fourth-order ΔΣ ADC was implemented achieving more than 12-bit resolution. The second chip further validated the methodology to include higher resolution, in the range of 13 bits, multi-bit ΔΣ ADCs. The experimental results from both prototype ICs closely mimic the system-level behavior of the designed modulator.

Résumé

Les exigences pour les systèmes de communication, portables ou autres, allant crescendo, deux défis majeurs se sont imposés pour la conception des Convertisseurs Analogiques-Numériques (CAN), desquels, en particulier, les modulateurs à architecture Delta-Sigma (MΔΣ).

Le premier défi consiste en l'extension de la gamme de fréquence pour inclure les applications requérant des bandes passantes dépassant le Mégahertz.

Par ailleurs, étendre la vitesse opérationnelle des MΔΣ est rendu encore plus compliqué par la diminution perpétuelle des dimensions fondamentales des transistors. En effet, il est prédit par l'Association de l'Industrie Semiconducteur (SIA) dans sa "feuille de route" pour la technologie de CMOS, que la dimension fondamentale des transistors atteindra 0.05 μm en 2011. Avec cette diminution dans la longueur fondamentale et, par ricochet, dans la tension d'alimentation, la modélisation des transistors devient beaucoup plus subtile. Aussi, la déviation des circuits de leur comportement idéal devient plus prononcée. En conséquence, la conception des principaux blocs analogiques qui minimise le temps de mise en marché devient très compliquée. D'où le second défi.

Ces deux problèmes seront adressés dans cette thèse par le biais d'une nouvelle méthode de conception qui minimisera le cycle de conception des CAN à architecture ΔΣ pour les applications hautes fréquences. L'efficacité de cette méthode sera démontrée par l'implémentation de deux modulateurs intégrés performants utilisant une figure de mérite largement adoptée.

La validité de la méthodologie de conception top-down a été vérifiée par la fabrication de deux circuits intégrés (IC) prototypes en technologie CMOS de 0.18 μm de TSMC. Le premier prototype correspond à un CAN à architecture ΔΣ du quatrième ordre et à un seul

bit atteignant une résolution de 12.6 bits. Le deuxième prototype a validé encore plus la méthodologie dans la conception des CANs ΔΣ multibit de qualité supérieure. Celle ci étant dans les environs de 13 bits. Les résultats expérimentaux des deux prototypes montrent une conformité étroite avec le comportement système des modulateurs conçus.

Acknowledgments

First and foremost, I would like to thank my supervisor, Professor Gordon W. Roberts for his continuous support and encouragement throughout this thesis. On the technical side, his guidance and insights were invaluable. On the financial side, his generosity was truly incomparable with his unconditional financial support until the thesis project was fully completed. For that, I am deeply grateful.

Second, I would like to thank Micronet for their financial support and the Canadian Microelectronics Corporation (CMC) for fabricating the prototype ICs.

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To my sister and best friend Samar: the continuous calls, e-mails, visits from your side and invitations to visit you, and the many more things you did to encourage me, the list of which is endless, the word thank you will never describe how I feel or express how indebted I am to you. You are truly wonderful!

Last but not least, a heart felt thank you for my parents: Riad and Fadia, brothers: Sobhi, Ahmad and Ziad, and sister Samar. Your constant support, patience and encouragement are what kept me going. I am so proud and thankful to have a family as loving and as sacrificing as you are. To you I dedicate this thesis.

Table of Contents

List of Tables

List of Figures

Chapter 1 - Introduction

1.1 - Motivation

Delta-sigma modulators (ΔΣM) are attractive architecture for the implementation of Analog-to-Digital Converters (ADCs). They allow for robust analog implementation due to their low sensitivity to analog component imperfections, as well as their relaxed anti-aliasing filter requirements. They were originally thought of as mostly suitable for high-resolution, medium-speed applications such as signal acquisition in voiceband telecommunications, digital audio, and Integrated Services Digital Network (ISDN) applications [1]. With the increase in high-speed digital communications, ΔΣM have recently emerged for applications where the input bandwidth extends well beyond the audio band to include broad input bandwidths in the MHz range, where self-calibrated pipelined converters have largely predominated [2].

1.1.1 - Lowpass ΔΣ Modulator Applications

The general block diagram of an ADC with the advantages of oversampling, feedback and noise shaping are shown in Figure 1.1.

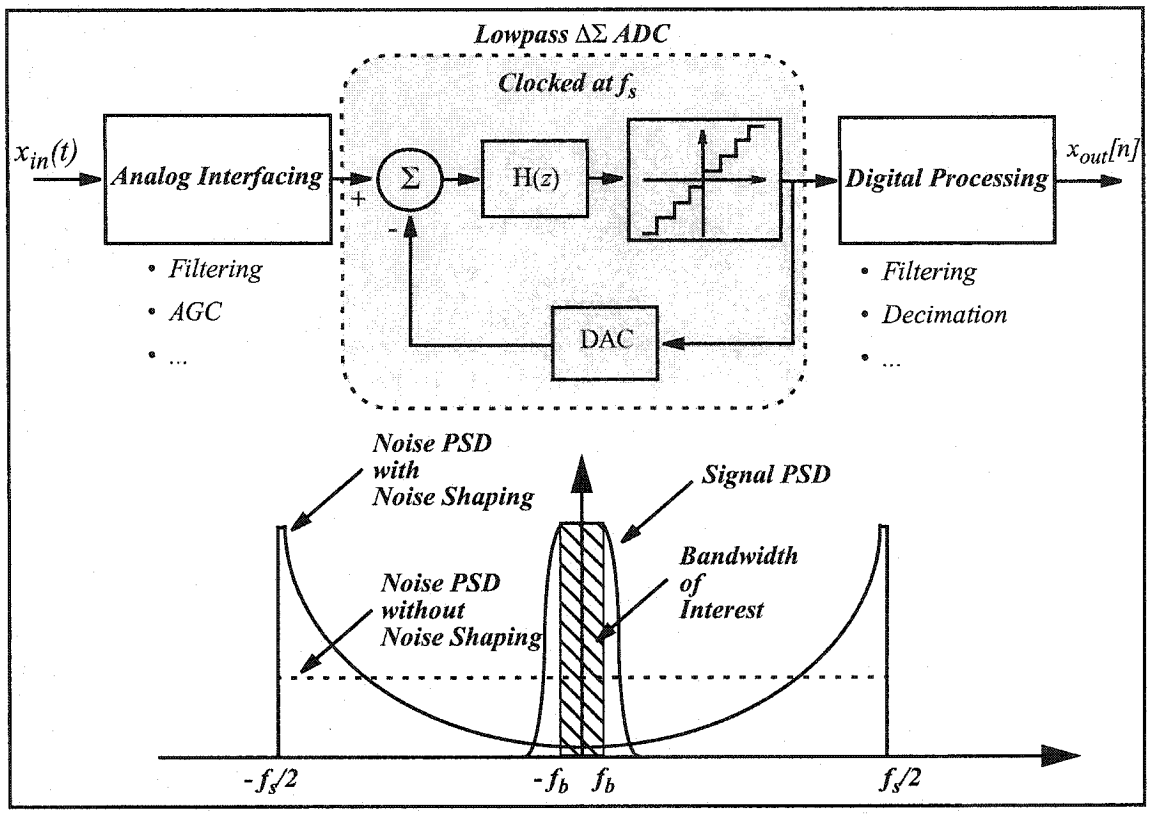


Figure 1.1 Block Diagram of an Oversampling Lowpass ΔΣ ADC Showing the Noise Shaping Advantages.

For low- to medium- speed applications such as audio band where the frequency of interest, f_b is relatively small, in the order of few kHz, oversampling by 64-256 (clocking therefore at ~ 11 MHz) is typical. High-resolution ΔΣ ADCs could therefore be achieved with modulators of low orders. As the input bandwidth increases beyond the 1 MHz range, the oversampling ratio (and therefore f_s) has to be kept low in order to allow for an achievable circuit implementation. In this situation, higher order modulators and in some cases depending on the resolution required, multi-bit quantization are needed.

The design of ΔΣ ADCs that are intended for digital communication systems, i.e., applications where the signal bandwidth is in the MHz range are therefore challenging.

The ever shrinking transistor length and supply voltage are adding another complexity dimension to the practical implementation of the analog circuit blocks and rendering the design task of high resolution modulators even more difficult.

Digital Subscriber Loops (DSL) is one such application where the input bandwidth can vary between 0.55 MHz - 2.2 MHz (or equivalently, the Nyquist output rate varies between 1.1 MSamples/s - 4.4 MSamples/s). The required resolution of the ADC for such applications is 12 - 14 bits. While the requirements on the ADC could be relaxed with the addition of a front-end Automatic Gain Control (AGC), it is desirable to eliminate the need for any additional block provided that the ADC could resolve such resolution.

Video applications is another place where high-speed ADCs are needed. In this case, the output rate is up to 14 MSamples/s with 10 - 12 bits of resolution required.

1.1.2 - Implementation Choices

Continuous-time modulators are possible ways for implementing such ADCs and they do in fact offer advantages over their discrete-time implementations such as avoiding problems of aliasing and wide band noise folding back to baseband frequencies, all of which are associated with sampling. On the other hand, continuous-time implementations suffer from their increased sensitivity to the feedback DAC and require accurate pulse shaping. They also are more sensitive to clock jitter. Switched-capacitor techniques are therefore used to circumvent the implementation complications of continuous-time modulators [1].

Based on the above discussion, the focus of this thesis will be on switched-capacitor implementations for DSL applications, and in particular, Asynchronous-DSL (ADSL) where the required input bandwidth is 1.1 MHz corresponding therefore to a Nyquist output rate of 2.2 MSamples/s.

The goal specifications of this thesis will next be placed in context with a literature survey summarizing the published-to-date high-speed ADCs.

1.1.3 - Lowpass ΔΣ Modulator Performance

Many lowpass ΔΣ modulators integrated circuits are published in the literature. Table 1.1 presents a brief literature survey [2]-[21] about the published-to-date modulators. They

vary in their performance, output rate, power dissipation, technology, choice of architecture and sampling frequency, f_s. With this wide range of design criteria, it becomes unclear as to which modulator provides the best "overall" performance. While some modulators might have a superior resolution, the power dissipation could be very large too. A fair mean for comparing these modulators is based on the normalization of the main design specifications such as resolution (or dynamic range), power dissipation and input bandwidth. Two figures of merit FM_1 [9] and FM_2 [4] are therefore introduced and defined in Eqn. (1.1) and Eqn. (1.2) respectively,

$$FM_1 = \frac{4KT \cdot BW \cdot DR}{P} \tag{1.1}$$

$$FM_2 = \frac{P}{2^b \cdot BW} \tag{1.2}$$

where DR is dynamic range, b is the bit-resolution, BW is the output rate, P is the power dissipation, K is the Boltzman's constant and T is the temperature. Note that $DR = 2^b$.

Either one of the two figures of merit could be used to classify the performance of the modulators since they are scaled (and inverted) versions of each other. But they are both shown here for completeness since both measures are used in publications. The entries in Table 1.1 are sorted in order of performance starting with the modulator achieving the best performance (lowest figure of merit FM_2).

With both criteria, the modulators implemented in this thesis (and which are highlighted in Table 1.1 and denoted by Chip 1 and Chip 2) are among the best modulators published to date. A plot of FM_2 is shown in Figure 1.2. In terms of supply voltage used, the modulators use the lowest supply voltage (Figure 1.3) and dissipate the lowest power among the broad output rates.

Table 1.1 - Performance Summary of Lowpass ΔΣ Modulator ICs

Reference/ Year	*DR (bits)*	*Output Rate (Ks/s)*	*Power (mW)*	*Process/Supply*	*Architecture*	*Fs (MHz)*	*FM_1*	*FM_2 (pJ)*	*Area (active), mm^2*
[3]/2000	16	2500	105	0.5um CMOS/5-3V	Cascade 2-1-1, 4b everywhere (DWA)	20	3.87E-05	0.64	24.84 (everything)
[4]/1997	16.15	50	2.5	0.8um CMOS/1.8V	Second order, 5b/ 12-b pipeline cascade	4	4.15E-05	0.69	1.30
Chip 2	14.45	2000	36	0.18um CMOS/1.8V	Cascade 2-1-1, 3b	50	4.86E-05	0.80	8.3
[5]/2001	15.49	4000	150	0.5um CMOS/2.5V	Cascade 2-2-1, 5b (P-DWA), 3b, 3b	64	4.92E-05	0.81	10.00
[6]/2002	14	4400	66	0.25um CMOS/2.5V	Cascade 2-1-1, 3b	70.4	5.53E-05	0.92	-
Chip 1	13	2000	18.8	0.18um CMOS/1.8V	Cascade 2-1-1	50	7.29E-05	1.21	10.20
[2]/2000	15.82	2500	295	0.65um CMOS/5V	Third order, 4b (DWA)	60	1.23E-04	2.04	5.30
[7]/2002	14.32	2200	92	0.18um CMOS/3.3-1.8V	Cascade 2-2-2, tri-level	64	1.23E-04	2.04	2.60
[8]/1999	15	2200	200	0.5um CMOS/3.3V	Cascade 2-1-1	52.8	1.68E-04	2.77	5 (with pads)
[9]/1999	12.9	2200	55	0.7um CMOS/5V	Cascade 2-1-1, 3b	35.2	1.98E-04	3.27	1.30
[10]/1993	15.7	320	65	1.2um CMOS/5V	Cascade 2-1	20.48	2.30E-04	3.82	1.60
[11][12]/1997-1998	14.82	2000	230	1um CMOS/5V	Cascade 2-1-1	48	2.40E-04	3.98	-
[13]/2000	12	50000	850	0.6um CMOS/3.3V	Pipeline	50	2.51E-04	4.15	16.00
[14]/2001	13	2000	77	0.35um CMOS/3.3V	Cascade 2-1-1 (programmable levels)	35.2 / 64 (12b)	2.84E-04	4.70	1.32
[15]/1991	12	2100	41	1um CMOS/5V	Cascade 2-1, 3b	50	2.88E-04	4.77	0.65
[16]/1997	14.5	2500	435	0.6um CMOS/5-3V	Second order, 5b/ 12-b pipeline cascade	20	4.53E-04	7.51	21.2 (with pads)
[17]/1994	14.7	200	40	1.2um CMOS/5V	Cascade 2-2-2, tri-level	3.25	4.54E-04	7.51	2.00
[18]/1996	13.7	500	58	1.2um CMOS/5V	Fourth order, 4b with self-calibration	8	5.26E-04	8.72	2.56
[19]/2000	12	12500	491.6	0.6um CMOS/5-3V	Third order, 4b (DWA)	100	5.80E-04	9.60	5.30
[20]/1995	15.65	40	67.5	1.2um CMOS/5V	Second order, 3b (ILA)	2.56	1.98E-03	32.82	3.10
[21]/1995	12	1540	250	0.7um CMOS/5V	Cascade 2-1-1	49.15	2.39E-03	39.63	65 (all)

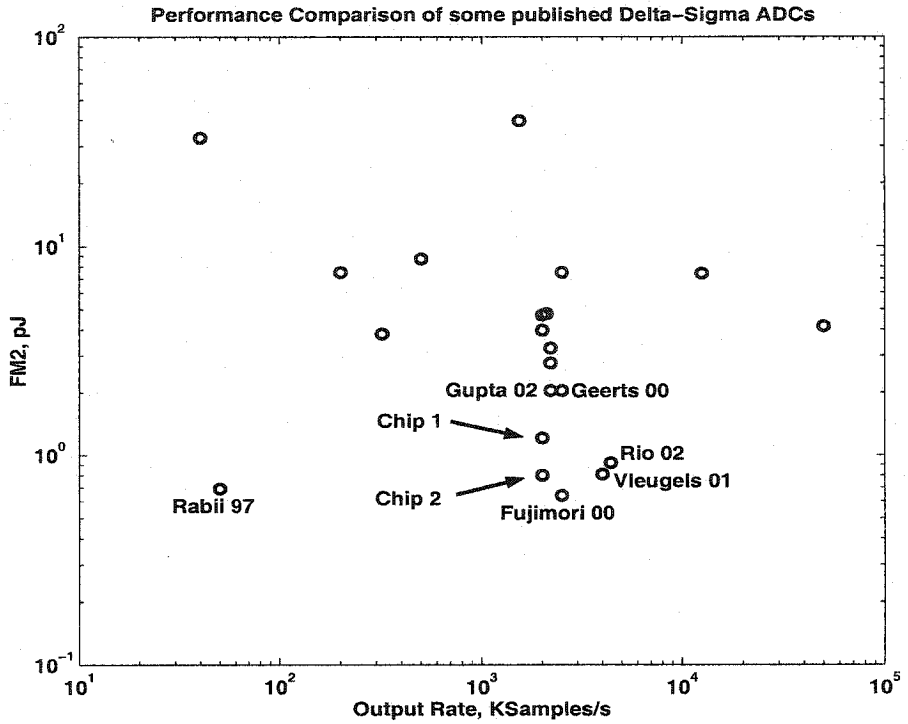


Figure 1.2 Performance Comparison of Different Modulators.

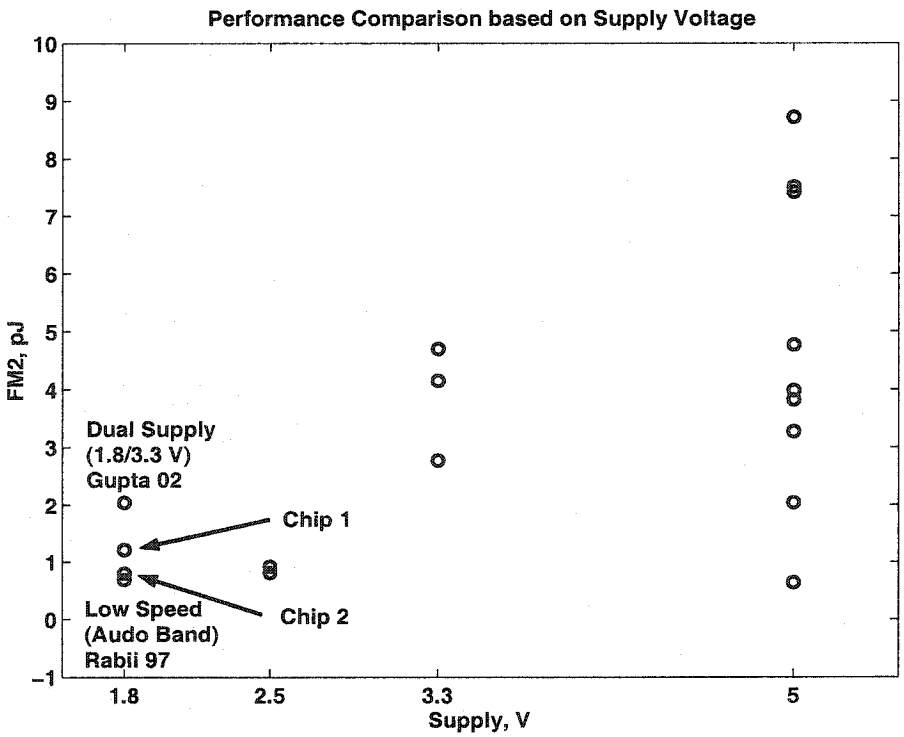


Figure 1.3 Performance Comparison Based on Supply Voltage.

1.2 - Thesis Outline

Chapter 1 provided a brief motivation to the work carried out in this thesis. In particular, the need for a fast top-down design methodology that minimizes the time-to-market was discussed. This method is then put in the context of the design of delta-sigma modulators ADCs for ADSL applications. A survey of the published-to-date modulators is presented and compared with the goal specification of this thesis.

Chapter 2 presents the system-level design of a fourth-order, single-bit ΔΣ ADC. The fast synthesis method for designing circuit specifications using what we will define later as 'separation of uncorrelated variables' is explained further and Matlab/Simulink®simulation results presented. Trade-offs in the choice of architecture, coefficients, and circuit building block specifications are discussed in details.

Chapter 3 presents the mapping of the system-level specifications into a switched-capacitor circuit design and implementation of the high-order, single-bit, ΔΣ ADC. The design of the main building blocks of the ΔΣ ADC such as the operational amplifier, comparator, clock generator, capacitor design and layout are all discussed in details with design choices and trade-offs. The layout floorplan of the chip and simulation results of the overall design are presented to verify the correct functionality and provide high level of confidence before fabrication.

Chapter 4 extends the design to include multi-bit delta-sigma modulation. Circuit implementation is discussed briefly since a more detailed study was presented in the earlier chapter. DAC non-idealities are however presented in details. In particular, the requirements imposed on the digital-to-analog converter (DAC) to meet the goal resolution are shown through modelling of the Integral- and Differential-non-Linearity (INL and DNL) simulations in Matlab/Simulink. From the DNL requirements, implementation choices of the multi-bit ADC and DAC are made. The full circuit and chip implementation are then presented with simulation results presented.

Chapter 5 presents the experimental results of both prototype ICs. In this chapter, comparison between simulation and experimental results are shown with attempts to

explain any discrepancy. Testing both chips and presenting the results in the same chapter and in parallel will help support the claims for explaining the discrepancies between simulation and experimental results.

A summary of the findings of this thesis together with concluding remarks are finally presented in Chapter 6.

Chapter 2 - System-Level Design

2.1 - Background

Like in any sampled system with feedback, delta-sigma modulators (ΔΣM) suffer from a long design cycle. This makes the time-to-market excessively long due to the long simulation time required to fully characterize the modulator performance. Commonly, an input power sweep is required to define the dynamic range of the modulator, and therefore its useful range. Many simulation runs are therefore needed which is computationally inefficient using widely available circuit simulators. Designers often require more than one iteration before meeting their goal specifications which further slows down the design process. The solution resides in synthesizing the modulator's main building block specifications, all on the system level.

In the design of ΔΣM, the main circuit non-idealities that need to be accounted for include, but are not limited to: finite DC gain, bandwidth, slew rate, thermal noise of the operational transconductance amplifier (OTA), offset and hysterisis of the comparator, and on-resistance of the switches. All these non-idealities could be modelled at the system-level. This modelling not only allows to underline the important parameters that the design is most sensitive to, but could also be used to optimize for them.

System-level simulations of ΔΣM have been suggested in the literature. In [22], Matlab/Simulink was used to study the effect of each circuit non-ideality on the Signal-to-

Noise-Ratio (*SNR*). In [23] and [24], the circuit non-idealities were modelled and used to optimize for the best set of specifications. C programming language to model the circuit non-idealities was also reported in [25] with faster simulation time when compared with Matlab, saving therefore much CPU time.

In this thesis, Matlab/Simulink is used to derive a new method that does not require any multi-dimensional optimization saving therefore much simulation time. Parameters dictating the final performance of the modulator were separated reducing the complexity of the algorithm from exponential to linear dependency on the variables. In other words, the complexity of the algorithm used to deduce the optimum parameters, assuming n parameters exist, is reduced from $O(n)$ to $n \cdot O(1)$. Long optimization time could therefore be avoided and simple sweeps on the key parameters are enough to determine blocks' specifications on the system level [26].

This method will be demonstrated efficient in the implementation of two state-of-the-art modulators in terms of performance using the widely adopted figure of merit introduced earlier. While circuit implementation and experimental results are presented later in the thesis, a detailed description of the system-level design of the modulator is presented next.

The system-level design of the modulator in particular (and any block of interest in the more general case) is shown in Figure 2.1. One or more steps requires going back to previous steps if the design constraints are not met. In the next section, the loop order and choice of architecture are described first. The optimization process is then detailed with a new method that makes this step less CPU and time consuming. The remaining steps will be described in later chapters of the thesis.

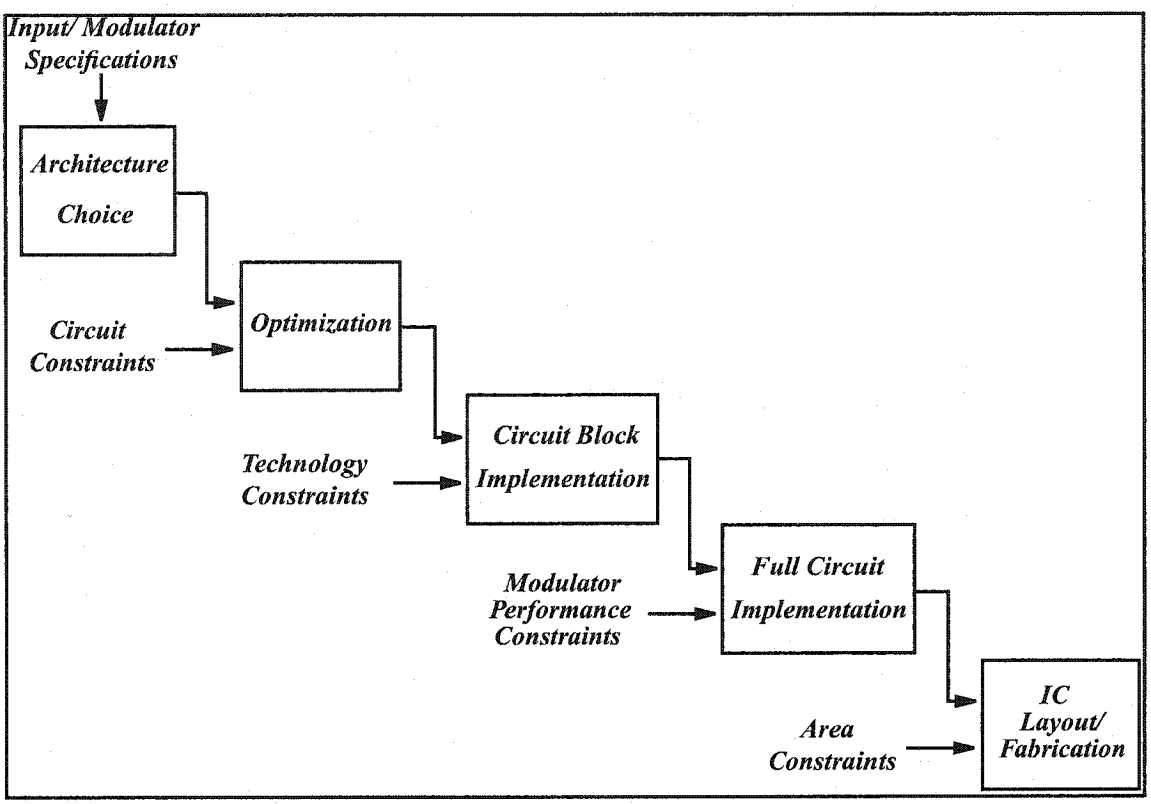


Figure 2.1 Block Diagram of the Top-Down System-Level Design of a ΔΣ Modulator.

2.2 - Architectural Considerations

2.2.1 - Loop Order

Degrees of freedom exist in the design of ΔΣM. *DR* is commonly used as an index for measuring modulators' performance, where larger *DR* implies better performance. The *DR* is determined primarily by the loop order, the *OSR* and the quantizer resolution, with higher loop order *n*, *OSR*, and/or quantizer resolution B_q yielding larger *DR*. All three parameters could be changed individually or simultaneously implying different design choices. A qualitative approach is first used to discuss how these parameters are chosen, followed by a quantitative analysis with graphs backing up the choice of *n* and *OSR*.

In the case of the design under consideration, an 80 dB *DR* corresponding to 13-bit resolution is the target specification. A single-bit quantizer is chosen (multi-bit

quantization will be addressed in Chapter 4 of this thesis). The two degrees of freedom left to be investigated are n and OSR. Limitations exist on increasing the OSR mainly dictated by the challenge in implementing the main building blocks at high sampling rates. The maximum n, on the other hand is dictated by the ability to maintain a small coefficient spread for implementation purposes.

Quantitatively, the peak SNR (which is assumed to be directly related or even equal to DR) relates to n, B_q and OSR according to [1]:

$$SNR_{max}(z) = \frac{3\pi}{2} \cdot (2^{B_q} - 1)^2 \cdot (2n+1) \cdot \left(\frac{OSR}{\pi}\right)^{(2n+1)}. \tag{2.1}$$

For the case of a single-bit quantizer where $B_q = 1$, the relationship becomes:

$$SNR_{max}(z) = \frac{3\pi}{2} \cdot (2n+1) \cdot \left(\frac{OSR}{\pi}\right)^{(2n+1)}, \tag{2.2}$$

which is graphically illustrated in Figure 2.2.

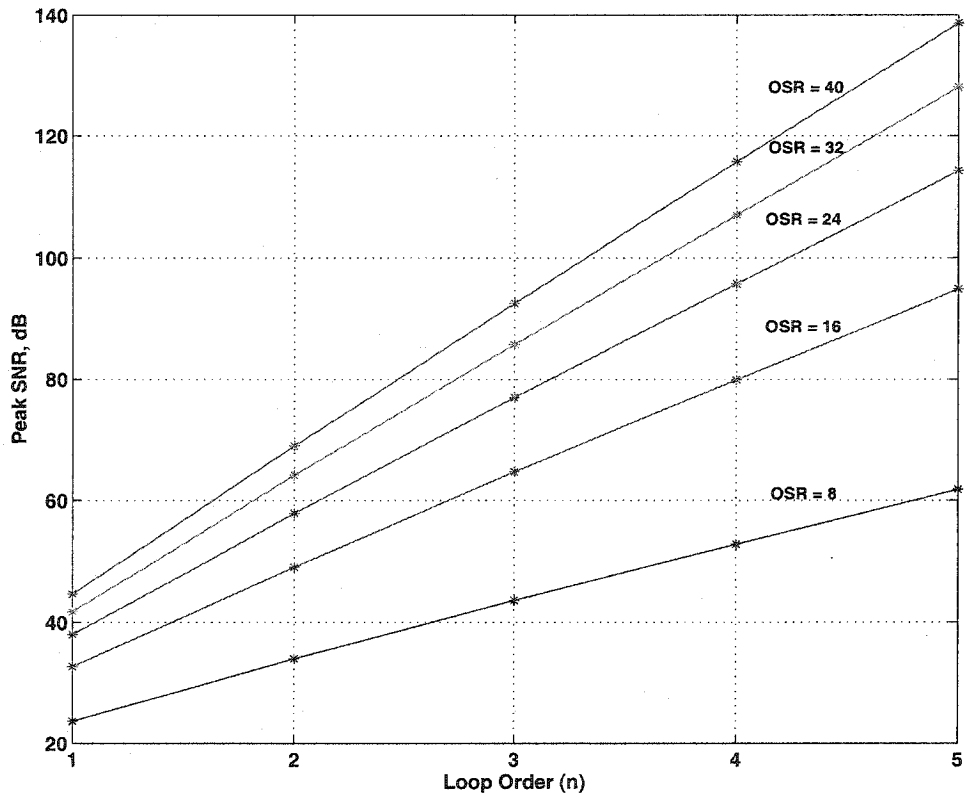


Figure 2.2 Theoretical *SNR* as a Function of Loop Order, *n*, for Different *OSR*.

In order to meet the 80 dB requirement, third- and fourth-order loops could be chosen, with f_s being ~ 1.7 times larger in the first case.

If power dissipation is to be brought into the equation, and assumed mainly dictated by the operational amplifiers, and therefore proportional to $n \cdot f_s$, then the fourth-order loop will result in a lower power dissipation. The ratio is given by: $\frac{P_{(n=3)}}{P_{(n=4)}} = \frac{3f_{s\,(n=3)}}{4f_{s\,(n=4)}} = \frac{3 \cdot [1.7f_{s\,(n=4)}]}{4f_{s\,(n=4)}} = 1.275$. In other words, choosing the fourth order loop results in a 27.5% decrease in the power dissipation.

This is simply first-order analysis that is not necessarily very accurate, but good enough to provide a starting point for the choice of n and OSR. Simulations will be used to verify these assumptions.

It is worth mentioning that with a fourth-order loop, an $OSR = 16$ is just enough to provide 80 dB peak SNR. A higher OSR will be used to allow for some safety margins.

In summary, a fourth-order ΔΣM with $OSR = 24$ will be chosen for the implementation of the modulator.

2.2.2 - Architecture Choice: Single-Loop versus MASH

The selection of the architecture is the first step in the top-down design process. In order to achieve a large dynamic range, a detailed study for the choice of the appropriate topology and proper topology parameters is outlined next.

The two architectures considered for the implementation were single-loop and Multi-stAge noise SHaping (MASH) architectures. Each architecture offers advantages and disadvantages and are outlined next.

For high bandwidth signals where low OSR is inevitable, high order loop and/or multi-bit are needed. As a result, stability becomes a concern. Even if coefficients were designed carefully and selected so as to place the system's poles inside the unit circle under different process variations, implementation becomes an issue. Namely, in a switched-

capacitor implementation where coefficients are implemented using capacitors, large coefficients spread implies large capacitance spread resulting in matching concerns.

As an example, DSMOD [27], a program for the design of ΔΣM developed at McGill University was used to design a single-stage fourth-order modulator. The block diagram for the Forward Euler structure which approximates a unity signal transfer function is shown in Figure 2.3.

The obtained coefficients for the modulator, before and after dynamic range scaling, are summarized in Table 2.2. The small coefficients were set to zero to minimize the coefficients spread. Simulations results shown in Figure 2.4 confirmed that no losses in the dynamic range occur when these coefficients are set to zero. The obtained coefficients still need to be rounded to a fraction of integers in order to allow for capacitor implementation. This step is not shown here since this will not be the architecture of choice used in the final implementation.

The coefficient spread was found to be 89 and 67 before and after dynamic range scaling respectively. The achieved dynamic range was 77 dB corresponding to 12.5 bits of resolution, with a peak *SNDR* of 68 dB.

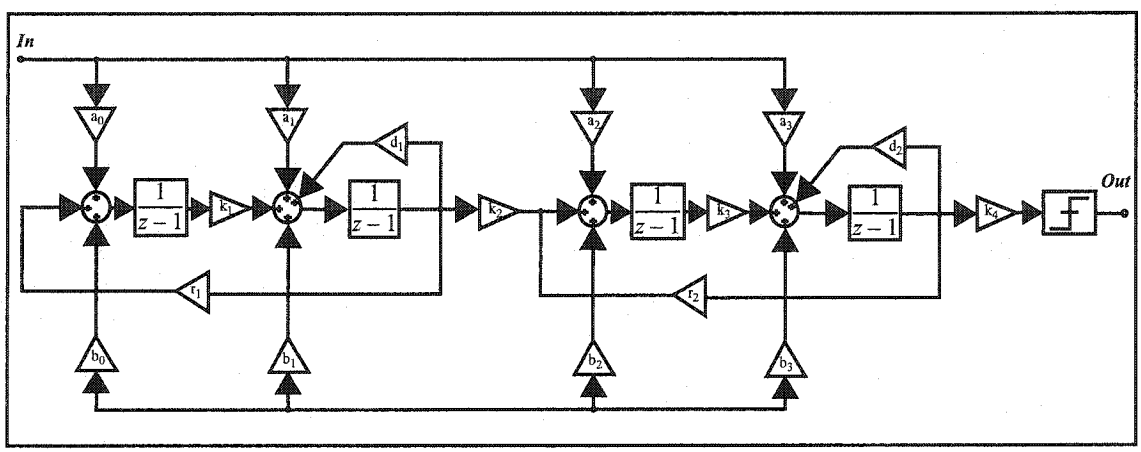


Figure 2.3 Simulink Model for the Single-Stage Forward Euler Fourth-Order Structure.

Table 2.1 - Summary of Coefficients Obtained from DSMOD for the Forward Euler Structure.

Coefficient	Before Scaling	After Scaling
a_0	-2.214E-2	-8.856E-2
a_1	-3.347E-2	-3.347E-2
a_2	-1.692E-2	4.230E-3
a_3	-2.841E-3: Set to zero	0
b_0	-1.494E-2	-5.976E-2
b_1	-1.536E-1	-1.536E-1
b_2	-5.825E-1	1.456E-1
b_3	-1.130E0	-2.825E-1
d_1	-1.269E-2	-1.269E-2
d_2	-1.948E-3: Set to zero	0
r_1	-1.269E-2	-5.076E-2
r_2	-1.981E-3: Set to zero	0
k_1	-	1/4
k_2	-	1/4
k_3	-	1
k_3	-	1
Maximum Spread	89	67

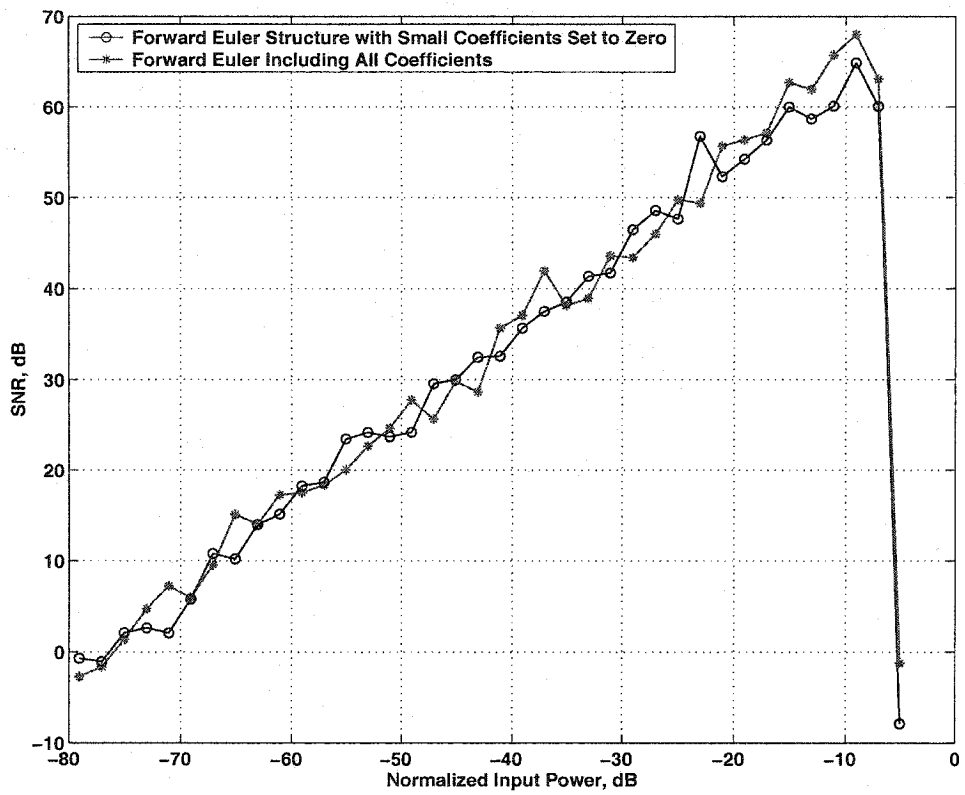


Figure 2.4 *SNDR* plot of the Fourth Order Forward Euler Structure Designed Using DSMOD Tool.

The MASH architecture on the other hand offers better stability because it is constructed from lower order sections. As it will be shown later, the maximum coefficients spread is 4 with a larger *DR* and peak *SNDR*, and will therefore be the architecture of choice. Its implementation is however more complicated for the following reasons:

- *A digital error cancellation block is needed since the reconstruction of the overall, high-order noise shaped output requires filtering in the digital domain to cancel out lower-order noise shaped outputs.*
- *Each additional stage requires one additional comparator.*
- *High gain operational amplifiers and high matching between analog and digital circuitry are needed in order to have "perfect" cancellation of noise from lower order stages. If not, noise leakage degrades the performance of the modulator.*

For the above reasons, MASH architectures have a higher overall power dissipation when compared with their single-loop counterparts.

For increased stability and ease of dynamic range scaling, MASH architecture will be selected. Attempts to reduce the power dissipation will be discussed later when circuit parameter optimization is presented.

The fourth-order MASH architecture was chosen to be implemented in 2 - 1 - 1 fashion. Second order section was used in the first stage to reduce tones incurred and uncancelled quantization error due to circuit non-idealities in the first stage which all feed to the subsequent stages when using first-order noise shaping in the first stage [15].

In summary, in order to meet the goal specifications, namely 80 dB *DR* for ~ 1 MHz input bandwidth, a fourth-order, single-bit, cascade 2-1-1 architecture with 50 MHz sampling frequency, *fs* was chosen. The complete Simulink system-level model for the chosen architecture is shown in Figure 2.5.

The derivation of the outputs of each section of the modulator together with the overall output after digital error cancellation is outlined next and will be used to derive all the coefficients shown in the modulator block diagram.

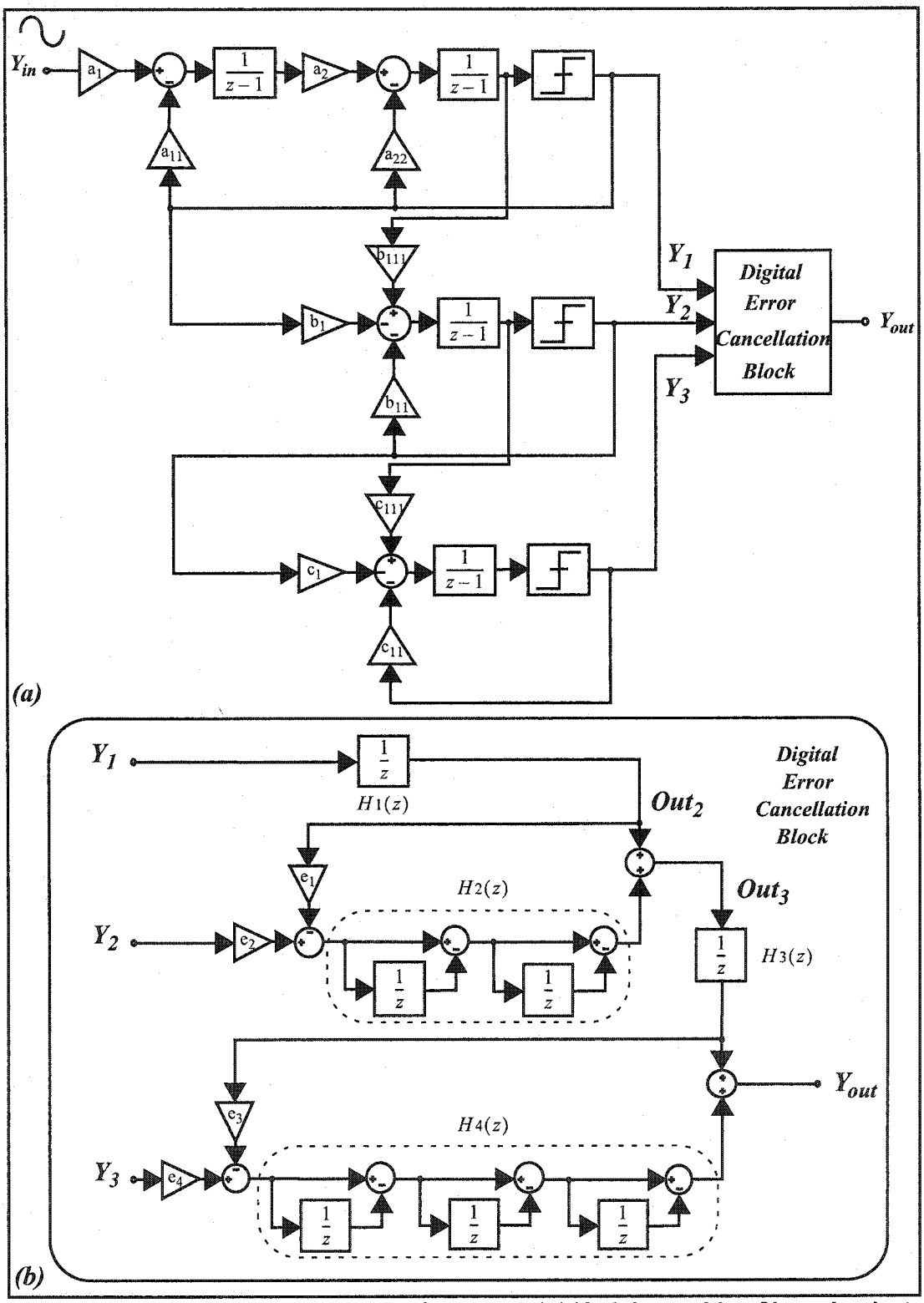


Figure 2.5 (a) Simulink Model for the Cascade 2-1-1 Modulator with a Closer Look at the (b) Digital Error Cancellation Logic.

2.2.3 - Coefficients Choice and Scaling for STF and NTF

Relative Scaling: Coefficients Relationships

Before the coefficients could be derived, the model for the quantizer used is shown in Figure 2.6. As can be seen, the quantizer is modelled as an additive noise source with power equal to E, and a preceding "phantom gain" stage. While there is little rigorous explanation for such gain insertion, the model works well. It is sometimes referred to as the "unity-gain approximation" [28] where the phantom gain is added to set the gain of the outermost loop to unity.

This linear model was used to replace all the quantizers in the block diagram shown in Figure 2.5, where p_i was used to refer to the phantom gain in the i^{th} stage. Similarly, E_i and Y_i represent the quantization noise power and output in the i^{th} stage respectively.

A straight forward derivation gives the outputs of each one of the three stages of the modulator:

$$Y_1(z) = In(z) \cdot \frac{a_1 \cdot a_2 \cdot p_1}{D_1(z)} + E_1(z) \cdot \frac{(z-1)^2}{D_1(z)}, \text{ where}$$

$$D_1(z) = z^2 - z \cdot (2 - a_{22} \cdot p_1) + (a_{11} \cdot a_2 \cdot p_1 - a_{22} \cdot p_1 + 1), \tag{2.3}$$

$$Y_2(z) = Y_1(z) \cdot p_2 \cdot \frac{b_{111}/p_1 - b_1}{D_2(z)} - E_1(z) \cdot \frac{b_{111} \cdot p_2/p_1}{D_2(z)} + E_2(z) \cdot \frac{z-1}{D_2(z)}, \text{ where}$$

$$D_2(z) = z - 1 + b_{11} \cdot p_2, \text{ and} \tag{2.4}$$

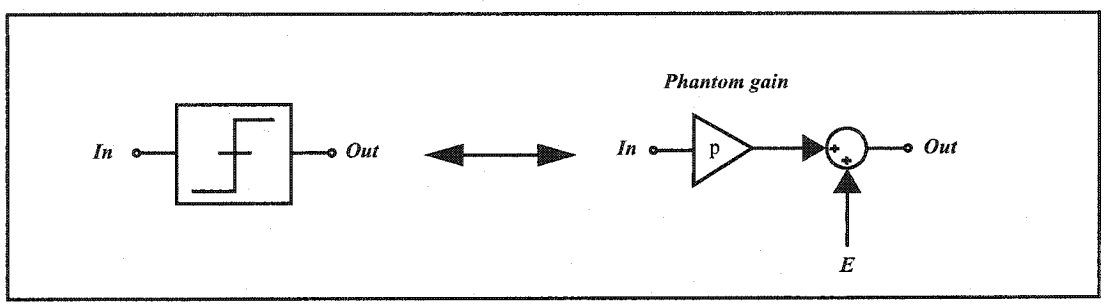


Figure 2.6 Linearized Quantizer Model.

$$Y_3(z) = Y_2(z) \cdot p_3 \cdot \frac{c_{111}/p_2 - c_1}{D_3(z)} - E_2(z) \cdot \frac{c_{111} \cdot p_3/p_2}{D_3(z)} + E_3(z) \cdot \frac{z-1}{D_3(z)}, \text{ where}$$

$$D_3(z) = z - 1 + c_{11} \cdot p_3 . \tag{2.5}$$

In order for these outputs to give meaningful results (i.e. a fourth-order noise-shaped output), the digital error cancellation block is supposed to give an overall output that, besides its dependency on the input, is solely a function of E_3.

In other words,

$$Y_{out}(z) = In(z) \cdot \frac{1}{z^4} + E_3(z) \cdot e_4 \cdot \left(\frac{z}{z-1}\right)^4 \tag{2.6}$$

needs to be satisfied under the constraints:

$$H_1(z) = \frac{1}{z},\ H_2(z) = \left(1 - \frac{1}{z}\right)^2,\ H_3(z) = \frac{1}{z}, \text{ and } H_4(z) = \left(1 - \frac{1}{z}\right)^3 . \tag{2.7}$$

With these criteria in mind, the relationships of the coefficients in the cancellation block as a function of the modulator coefficients are derived next.

It is worth mentioning that the "usual" MASH structure consists of feeding exactly the quantization error of the previous stage to the subsequent one (which corresponds to $b_1 = b_{111}$ and $c_1 = c_{111}$). This is not the optimum scaling for maximum dynamic range. Instead, non-equal coefficients are used when feeding quantization errors from previous stages to subsequent ones. This is directly linked to the concept of phantom gain introduced earlier which will be used when dynamic range scaling is performed to help prevent premature overloading of integrators of subsequent stages.

The drawback for such non-equal weighting is an increased complexity in the digital filter design (mainly due to the non-zero/non-unity e_i coefficients). However, with proper coefficient design, the latter problem could be eliminated in some cases, and alleviated in others, as will be shown next.

As mentioned above, with non-equal coefficients for (b_1, b_{111}) and (c_1, c_{111}), the design of the coefficients in the digital error cancellation is not straight forward. No where in the literature is the derivation shown, and is therefore presented here.

Using Eqn. (2.3), and equating it, for **all** z, to

$$Y_1(z) = In(z) \cdot \frac{1}{z^2} + E_1(z) \cdot \frac{(z-1)^2}{z^2}, \tag{2.8}$$

which represents the ideal transfer function of a second-order delta-sigma noise shaped output and where $D_1(z) = z^2$, the following conditions need to be simultaneously satisfied:

$$\left\{ \begin{array}{r} a_1 \cdot a_2 \cdot p_1 = 1 \\ 2 - a_{22} \cdot p_1 = 0 \\ a_{11} \cdot a_2 \cdot p_1 - a_{22} \cdot p_1 + 1 = 0 \end{array} \right\} \Rightarrow \left\{ \begin{array}{l} p_1 = 1/(a_1 \cdot a_2) \\ a_1 = a_{11} \\ a_{22} = 2/(a_{11} \cdot a_2) \end{array} \right\}. \tag{2.9}$$

From Eqn. (2.4) and Eqn. (2.5) the only two coefficients that could be derived are the phantom gains (by equating $D_2(z) = D_3(z) = z$):

$$\left\{ \begin{array}{l} b_{11} \cdot p_2 - 1 = 0 \\ c_{11} \cdot p_3 - 1 = 0 \end{array} \right\} \Rightarrow \left\{ \begin{array}{l} p_2 = 1/b_{11} \\ p_3 = 1/c_{11} \end{array} \right\}. \tag{2.10}$$

Using the digital error cancellation block, the remaining coefficients are derived as follows:

Re-arranging Eqn. (2.3), we get:

$$E_1(z) = Y_1(z) \cdot \frac{z^2}{(z-1)^2} - In(z) \cdot \frac{a_1 \cdot a_2 \cdot p_1}{(z-1)^2}. \tag{2.11}$$

Using Eqn. (2.4), and replacing $E_1(z)$ by its equivalent from Eqn. (2.11):

$$Y_2(z) = In(z)\cdot\frac{a_1\cdot a_2\cdot p_1}{(z-1)^2}\cdot\frac{b_{111}\cdot p_2/p_1}{z}+E_2(z)\cdot\frac{z-1}{z}+ Y_1(z)\cdot\left[p_2\cdot\frac{b_{111}/p_1-b_1}{z}-b_{111}\cdot p_2/p_1\right] \quad (2.12)$$

Using straight-forward derivation from the digital error cancellation block diagram where $Out_3(z) = Out_2(z) - Out_2(z)\cdot e_1\cdot H_2(z) + Y_2(z)\cdot e_2\cdot H_2(z)$, and replacing $Y_2(z)$ with its equal from Eqn. (2.12), we get:

$$\begin{aligned} Out_3(z) &= Y_1(z)\cdot\frac{1}{z} - Y_1(z)\cdot\frac{1}{z}\cdot e_1\cdot H_2(z) + [Y_2(z)\cdot e_2\cdot H_2(z)] \\ &= Y_1(z)\cdot\frac{1}{z} - Y_1(z)\cdot e_1\cdot\frac{(z-1)^2}{z^3} + e_2\cdot\frac{(z-1)^2}{z^2}\cdot \\ &\quad\left\{In(z)\cdot\frac{a_1\cdot a_2\cdot p_1}{\langle z-1\rangle^2}\cdot\frac{b_{111}\cdot p_2/p_1}{z}+E_2(z)\cdot\frac{z-1}{z}+\right. \\ &\quad\left. Y_1(z)\cdot\left[p_2\cdot\frac{b_{111}/p_1-b_1}{z}-b_{111}\cdot p_2/p_1\right]\right\} \\ &= In(z)\cdot e_2\cdot a_1\cdot a_2\cdot p_1\cdot\frac{b_{111}\cdot p_2/p_1}{z^3}+E_2(z)\cdot e_2\cdot\frac{(z-1)^3}{z^3}+ \\ &\quad Y_1(z)\cdot\left[\frac{1}{z}\cdot(1-e_2\cdot b_{111}\cdot p_2/p_1)-\frac{(z-1)^2}{z^3}\cdot\left(e_1-e_2\cdot p_2\cdot\frac{b_{111}/p_1-b_1}{z}\right)\right] \end{aligned} \quad (2.13)$$

Equating $Out_3(z)$ from Eqn. (2.13), for **all** z, to the ideal transfer function of a third-order noise shaping given by $In(z)\cdot\frac{1}{z^3}+E_2(z)\cdot e_2\cdot\frac{(z-1)^3}{z^3}$, we get:

$$\left.\begin{aligned} e_2\cdot a_1\cdot a_2\cdot p_1\cdot(b_{111}\cdot p_2/p_1) &= 1 \\ 1-e_2\cdot b_{111}\cdot p_2/p_1 &= 0 \\ e_1-e_2\cdot p_2\cdot(b_{111}/p_1-b_1) &= 0 \end{aligned}\right\}\Rightarrow\left\{\begin{aligned} e_1 &= 1-b_1/(a_1\cdot a_2\cdot b_{111}) \\ e_2 &= b_{11}/(a_1\cdot a_2\cdot b_{111}) \end{aligned}\right\} \quad (2.14)$$

Using the digital error cancellation block diagram, the following expression can be derived for the output:

$$Y_{out}(z) = Out_3(z) \cdot H_3(z) - Out_3(z) \cdot H_3(z) \cdot e_3 \cdot H_4(z) + Y_3(z) \cdot e_4 \cdot H_4(z). \quad (2.15)$$

Using the definition of $Y_3(z)$ and $Y_{out}(z)$ given in Eqn. (2.5) and Eqn. (2.15) respectively, we get:

$$Y_{out}(z) = In(z) \cdot \frac{1}{z^4} \cdot \left[1 - e_3 \cdot \frac{(z-1)^3}{z^3}\right] + E_3(z) \cdot e_4 \cdot \frac{(z-1)^4}{z^4} - E_2(z) \cdot \frac{\langle z-1\rangle^3}{z^4} \cdot \quad (2.16)$$
$$[-e_2 + e_2 \cdot e_3 + e_4 \cdot c_{111} \cdot p_3/p_2] + Y_2(z) \cdot e_4 \cdot \frac{\langle z-1\rangle^3}{z^3} \cdot p_3 \cdot \frac{c_{111}/p_2 - c_1}{z}$$

Equating $Y_{out}(z)$ given in Eqn. (2.16), for **all** z, to $In(z) \cdot \frac{1}{z^4} + E_3(z) \cdot e_4 \cdot \frac{(z-1)^4}{z^4}$, the following coefficients constraints are derived:

$$\left\{ \begin{array}{r} e_3 = 0 \\ -e_2 + e_2 \cdot e_3 + e_4 \cdot c_{111} \cdot p_3/p_2 = 0 \\ e_4 \cdot p_3 \cdot (c_{111}/p_2 - c_1) = 0 \end{array} \right\} \Rightarrow \left\{ \begin{array}{l} e_3 = 0 \\ c_1 = b_{11} \cdot c_{111} \\ e_4 = c_{11}/(a_1 \cdot a_2 \cdot b_{111} \cdot c_{111}) \end{array} \right\}. \quad (2.17)$$

Based on the derivation above, the relationships between the different coefficients are summarized with

$$a_1 = a_{11},\ a_{22} = 2 \cdot a_{11} \cdot a_2, \text{ and } c_1 = b_{11} \cdot c_{111} \quad (2.18)$$

for the analog coefficients, and

$$e_1 = 1 - b_1/(a_1 \cdot a_2 \cdot b_{111}),\ e_2 = b_{11}/(a_1 \cdot a_2 \cdot b_{111}),\ e_3 = 0, \text{ and}$$
$$e_4 = c_{11}/(a_1 \cdot a_2 \cdot b_{111} \cdot c_{111}) \quad (2.19)$$

for the digital coefficients.

The relationships derived in Eqn. (2.18) and Eqn. (2.19) were outlined in [9], with the only exception that e_3 was found to equal $[1 - b_1/(a_1 \cdot a_2 \cdot b_{111})] \cdot [1 - c_1/(b_{11} \cdot c_{111})]$. The second term in the product is always zero due to the constraint imposed earlier on the analog coefficient c_1, namely $c_1 = b_{11} \cdot c_{111}$. In other words, no matter what the choice of the coefficients are, e_3 will always equal zero.

Absolute Values: Dynamic Range Scaling

Now that the relationships between the different coefficients are derived, the choice of the absolute value for each coefficient is outlined next.

While ideally any choices for the coefficients satisfying Eqn. (2.18) and Eqn. (2.19) will give a mathematically correct signal and noise transfer functions, practical considerations limit the choices available. Namely, for ease of implementation and in order to minimize hardware used, it is desirable to choose the e_i digital coefficients equal to 0, ± 1, or multiples of 2 (which corresponds to a simple shift in the digital domain).

Another criteria in the coefficients' choice is the achievable swing for the integrators in the circuit implementation. Dynamic range scaling is therefore needed to bound the outputs of each integrator to a reasonable swing level.

With these two criteria in mind, the derivation of the coefficients was carried out.

For simplicity, the derivation is shown for the first two stages. The extension to a three-stage modulator is straight forward and won't be shown here.

The coefficients are set initially to unity except for a_{22} which has to satisfy $a_{22} = 2 \cdot a_{11} \cdot a_2$, and is therefore set to 2. These coefficients will then be scaled to bound their corresponding integrator outputs to ± 0.5 range which corresponds to a swing of 1 in a single-supply circuit implementation.

Figure 2.7 shows the histogram for the distribution of first integrator's output. The input is set to a 0.6 V sinusoidal input, equivalent to 60% of the full scale reference voltages, which corresponds to the input power at which peak *SNR* of the modulator occurs. This distribution shows that the output reaches approximately five times the desired swing imposed above. Setting $a_1 = a_{11} = 1/5$ is therefore the logical choice had the output swing been the only constraint. Ease of hardware implementation limits the choices of the digital coefficients to equal a power of two. The final choice is therefore by setting $a_1 = a_{11} = 1/4$.

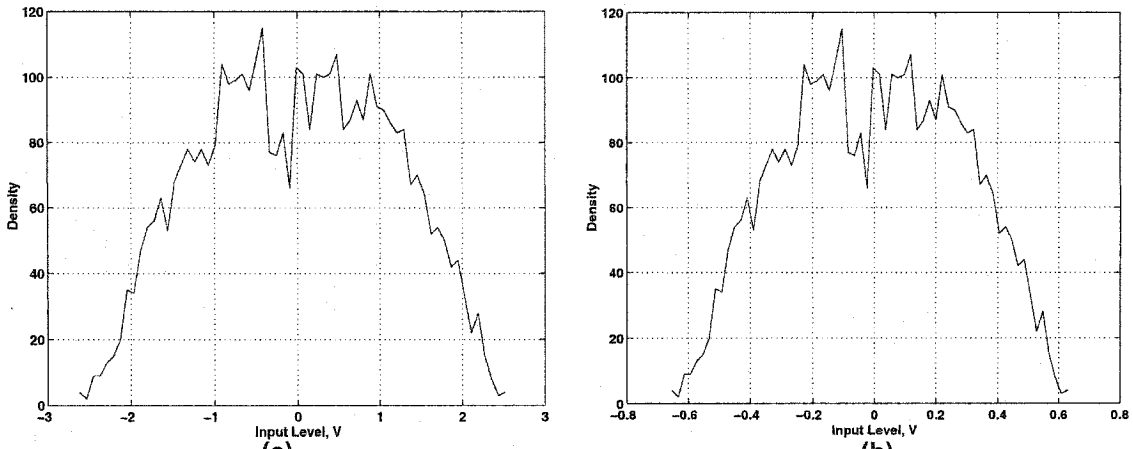


Figure 2.7 First Integrator Output Distribution: (a) Before and (b) After Scaling.

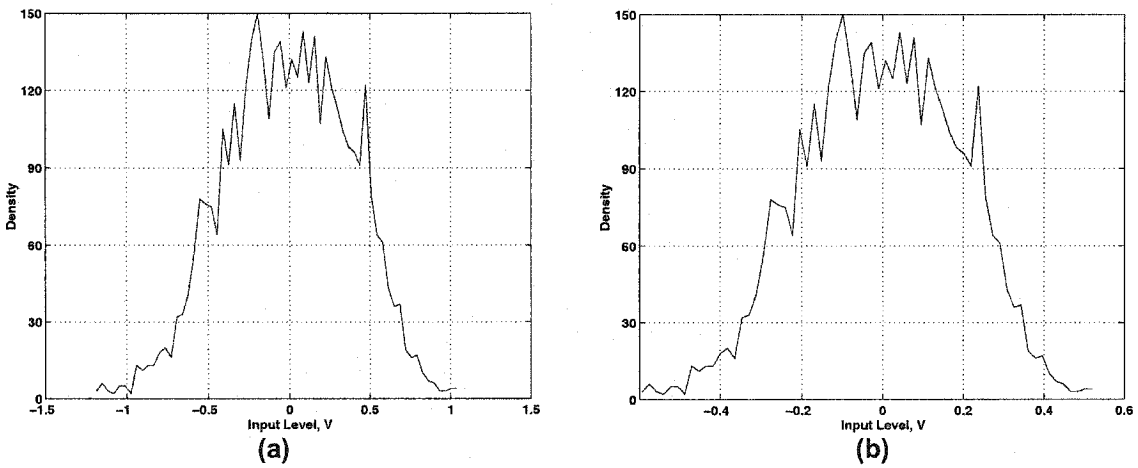


Figure 2.8 Second Integrator Output Distribution: (a) Before and (b) After Scaling.

The histogram for the second integrator's output is shown in Figure 2.8. To reduce the swing by a factor of two, the coefficients to the input of the second integrators need to be scaled with respect to their initial values by a factor of two implying $a_2 = 1/2$ & $a_{22} = 1/4$.

Having derived the coefficients of the first stage, the phantom gain p_1 could therefore be computed and set equal to 4. The derivation of the remaining coefficients follow logically and could be derived without any further simulation.

If all inputs to the third integrator are to be made equal for maximum dynamic range scaling together with the constraint on the output of the third integrator implies that $b_1 = b_{11} = 1/4$ and $b_{111} = b_{11} \cdot p_1 = 1$.

The coefficients of the last stage are chosen following the same reasoning presented above for the second stage. With the above scaling, the outputs from the third and fourth integrators are shown in Figure 2.9.

The optimized coefficients for the modulator are summarized in Table 2.2.

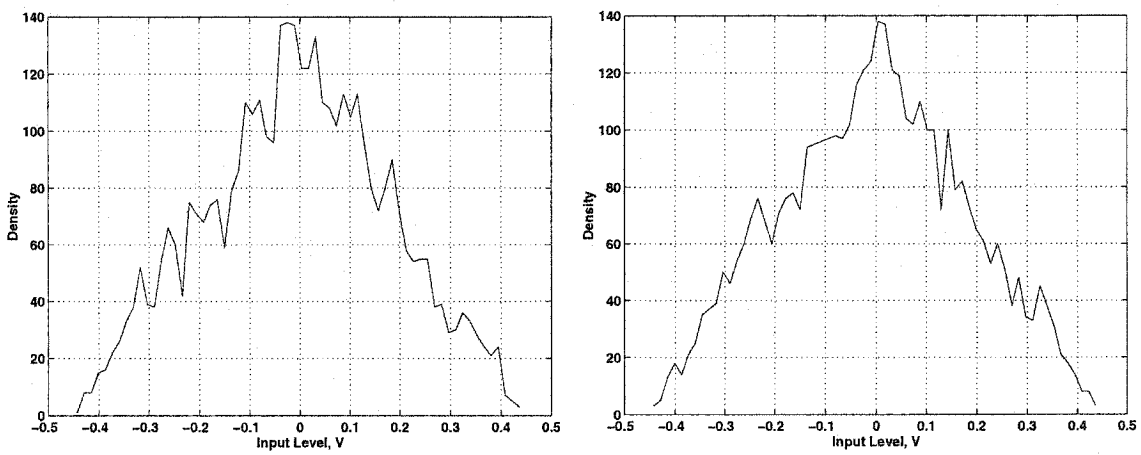


Figure 2.9 (a) Third and (b) Fourth Integrator Output Distribution After Scaling.

Table 2.2 - Summary of Coefficients Used in the Single-Bit ΔΣ Modulator Shown in Figure 2.5.

Coefficient	Coefficient Value
a_1	1/4
a_{11}	1/4
a_2	1/2
a_{22}	1/4
b_1	1/4
b_{11}	1/4
b_{111}	1
c_1	1/4
c_{11}	1/4
c_{111}	1
e_1	-1
e_2	2
e_3	0
e_4	2

It is worth mentioning that ideally, the overall output of the modulator should have the following form

$$V_{out_{ideal}}(z) = In(z) \cdot \frac{1}{z^4} + E_3(z) \cdot \left(\frac{z}{z-1}\right)^4. \tag{2.20}$$

Comparing Eqn. (2.16) to Eqn. (2.20), we see that the output noise has a fourth-order noise shaping characteristics. It is however scaled by e_4 (where $e_4 = 2$) which results in a 6 dB loss in the dynamic range when compared with the ideal fourth-order NTF (output of which is given in Eqn. (2.20)). Even with this loss, the achievable dynamic range is higher than that achieved in a single-loop configuration [29].

2.3 - Optimization Method

Now that the architecture is selected, the coefficients chosen and scaled for maximum dynamic range, the focus in this section will be on the impact of the circuit non-idealities on the system performance.

2.3.1 - Non-Idealities Considered

The complete system-level representation of the non-ideal model of the integrator was achieved in Matlab/Simulink [30]. The inputs to this block include the following non-idealities: OTA DC gain, bandwidth (*BW*), slew rate (*SR*), thermal noise density (S_n), switch on-resistance (*R*), and sampling capacitor (C_s). Other constants include the system *OSR*, Boltzman's constant (*K*) and the temperature (*T*). The comparator offset is another parameter that was included in the non-ideal characterisation of the modulator, even though noise-shaping alleviates its degradative effect on the overall system performance.

A complete description of the effect of each one of those non-idealities on the overall system performance was studied in great details and can be found in [22]-[24]. A less detailed description is provided here. The main difference with the method suggested in [24] is that optimization is carried out here for parameters such as DC gain, bandwidth, slew rate, etc., rather than parameters such as OTA differential pair transconductance g_m,

OTA output impedance r_{out} and biasing current I_{bias}. The latter assumes a certain op. amp. topology constraining therefore the mapping of the obtained results to any given circuit topology. The effect of each circuit non-ideality is explained next.

- The worst-case harmonic distortion due to R and C_s is computed according to [24]:

$$THD = \frac{e^{[-4R \cdot C_s \cdot f_s]^{-1}}}{1 - e^{[-4R \cdot C_s \cdot f_s]^{-1}}}.$$

- The OTA thermal noise is computed using a 2-pole system approximation. The RMS input-referred thermal noise is then given by:

$$\sqrt{\frac{S_n \cdot BW}{2A_1}}.$$

- The switched- capacitor (KT/C) noise is computed according to:

$$\sqrt{\frac{K \cdot T}{C_s \cdot OSR}}.$$

- All the previously mentioned inputs are then added together, with an input saturation block to represent the limited input swing of the OTA, to constitute the input to a modified delayed-integrator transfer function. The finite DC gain of the OTA denoted by A_1 as well as capacitor ratio mismatch denoted by a, will transform the transfer function to:

$$\frac{(1-a) \cdot \left[1 / \left(1 + \frac{(1-a)}{A_1}\right)\right]}{z - 1 / \left[1 + \frac{(1-a)}{A_1}\right]}.$$

- The limited OTA SR and BW are also modelled using a Matlab function that computes the current output given a current input, previous output and three cases which are determined by a purely slewing behavior, purely exponential behavior or a combination of both. A Matlab function is dedicated to compute the output value after checking for each one of the three cases.
- Finally the OTA output limited swing is modelled by a saturation block at the output of the modulator.

While the ideal transfer function of the delayed integrator is represented with a single-input, single-output transfer function given by $\frac{1}{z-1}$, combining all the previously mentioned non-idealities will transform the integrator to a more complex model. The complete non-ideal system-level block diagram of the delayed integrator, incorporating the non-idealities discussed above is shown in Figure 2.10.

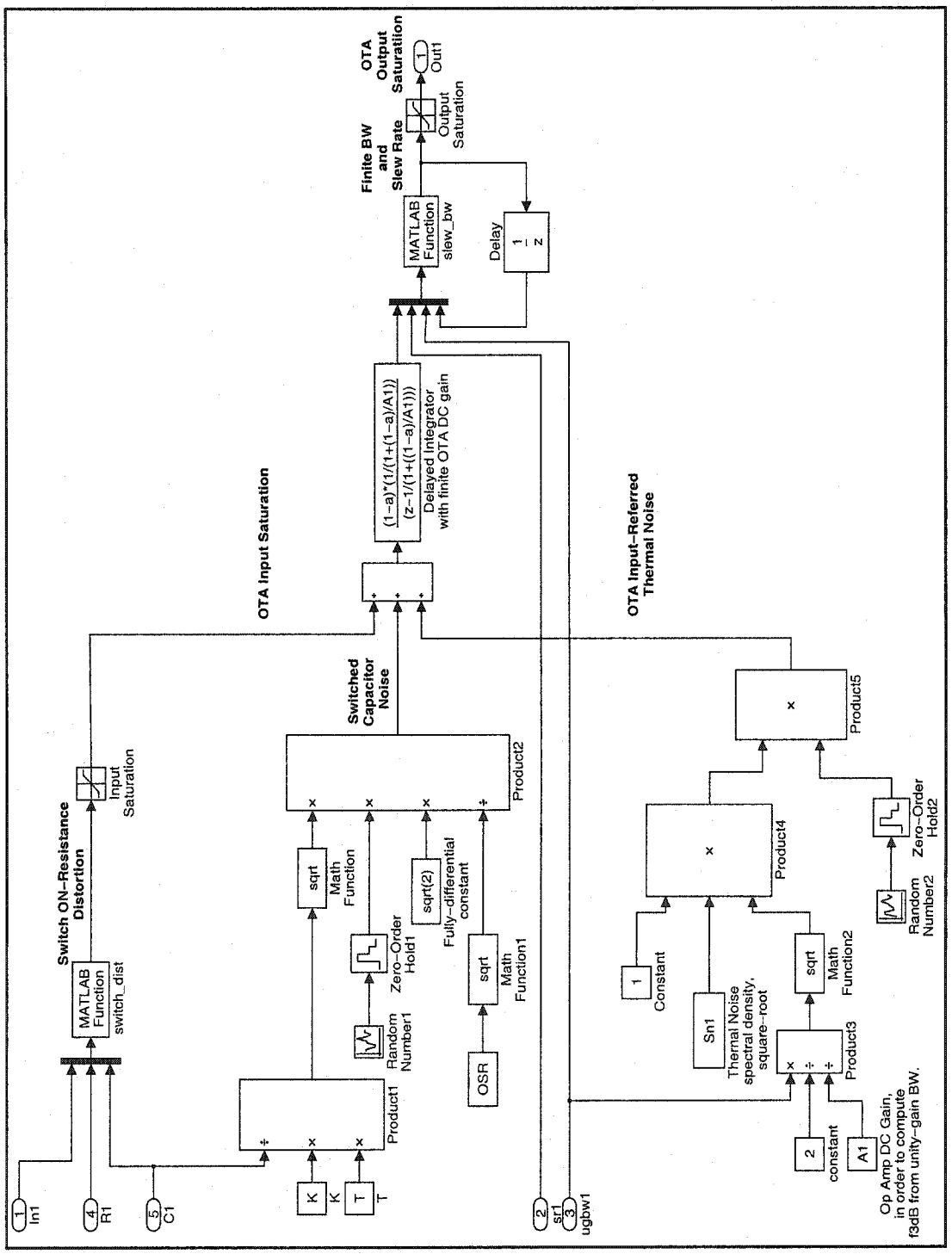


Figure 2.10 Simulink Model for the Non-Ideal Integrator.

2.3.2 - Separation of Variables

OTA Bandwidth (BW) and Slew Rate (SR)

Minimizing the power dissipation is one of the most important constraints when designing the building blocks of the modulator. Choosing the minimum specifications on each building block that meet the goal specification is guaranteed to minimize the power dissipation. Power therefore need not be included in the optimization process. A 3-D plot of *SNR* (where noise throughout includes harmonic bins) versus *SR* and *BW* is shown in Figure 2.11. By sweeping both slew rate and bandwidth simultaneously, power dissipation is indirectly minimized by deducing from Figure 2.11 the minimum *SR* and *BW* that meet the goal *SNR*.

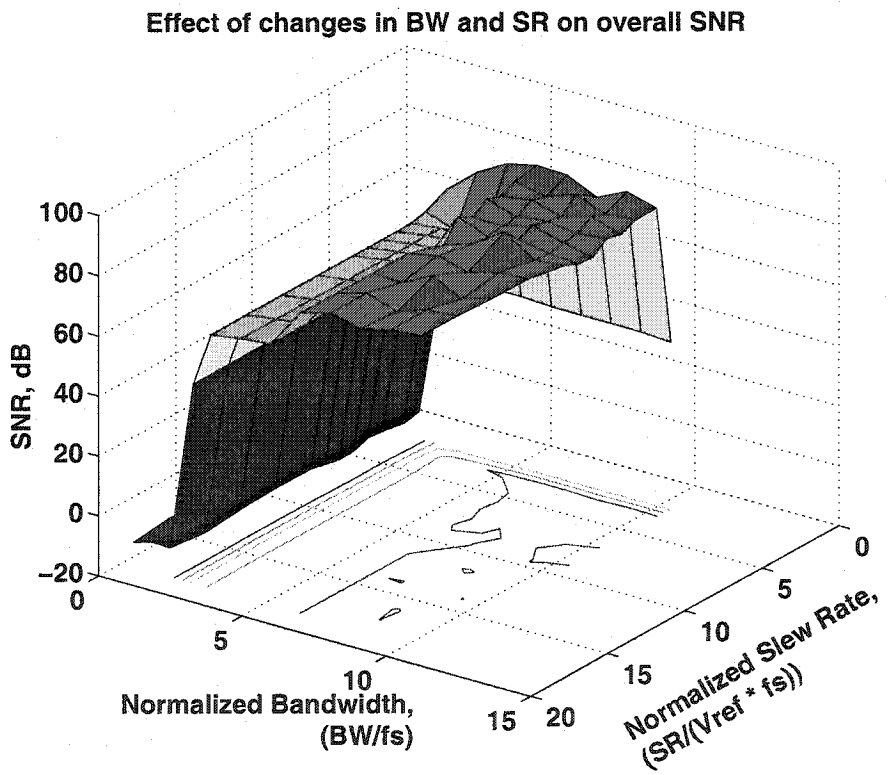


Figure 2.11 Peak *SNR* versus Bandwidth and Slew Rate.

Thermal Noise

It is also desired to include the OTA and *KT/C* thermal noise in the non-ideal model of the ΔΣM. *SNR* on the other hand monotonically decreases as the circuit thermal noise increases. The thermal noise (S_n) is a function of the OTA *BW* and DC gain, which might invoke the need for optimization. However, simulation results in Figure 2.12, Figure 2.13 and Figure 2.14 show that these parameters could be considered uncorrelated over a practically large range of *BW*, DC Gain and S_n. The contour plots are monotonic, implying the absence of any global minimum. In other words, these three factors (*BW*, DC Gain and S_n) could be assumed uncorrelated.

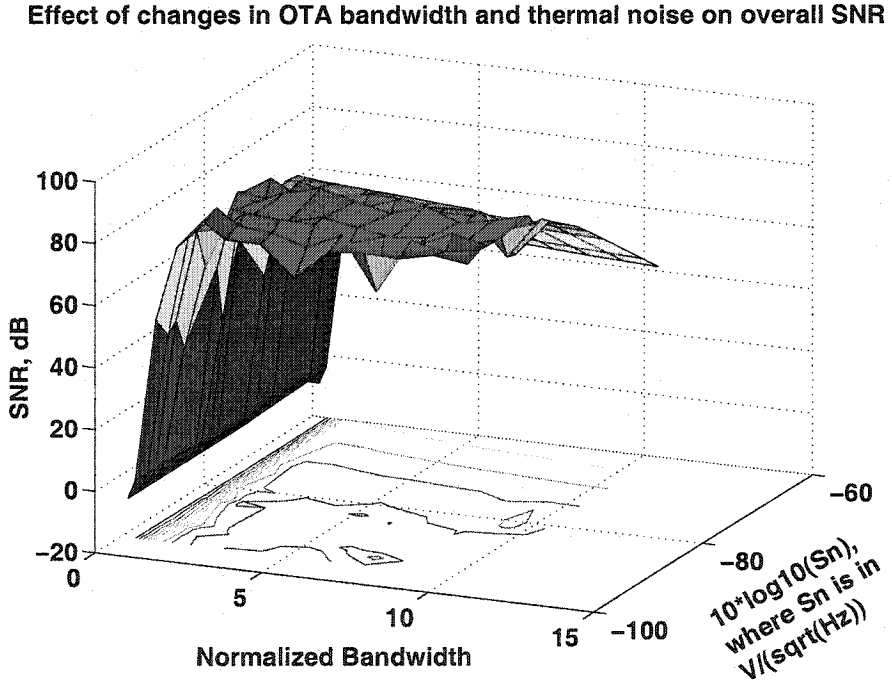


Figure 2.12 Peak *SNR* versus Bandwidth and Total Thermal Noise Spectral Density.

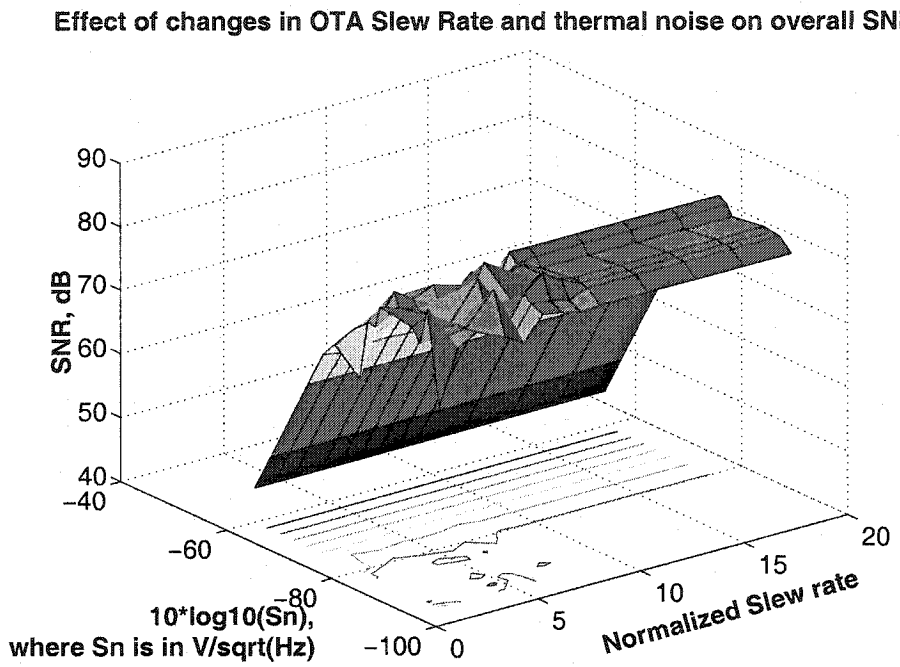


Figure 2.13 Peak *SNR* versus Slew Rate and Total Thermal Noise Spectral Density.

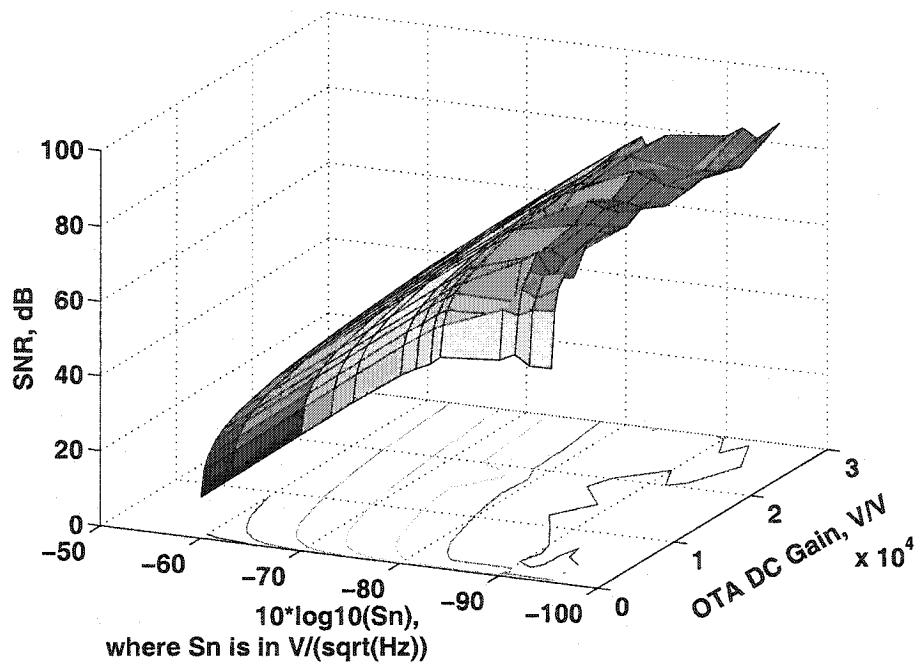


Figure 2.14 Peak *SNR* versus OTA DC Gain and Total Thermal Noise Spectral Density.

Switch Distortion

The switches of the front-end sampling network introduce distortion due to the dependency of their on-resistance on the input voltage. The worst-case distortion due to the variation in the resistance of the input switches was quantified in [24] and is given by:

$$THD \leq \frac{e^{[-2\cdot(2\cdot R_{max})\cdot C_s\cdot f_s]^{-1}}}{1-e^{[-2\cdot(2\cdot R_{max})\cdot C_s\cdot f_s]^{-1}}}. \tag{2.21}$$

A factor of 2 multiplies the maximum on-resistance, R_{max} to account for the two resistances on both sides of the sampling capacitor.

A plot of the magnitude of the Total Harmonic Distortion, $|THD|$, as a function of the switch on-resistance is shown in Figure 2.15. In the case where $C_s = 1$ pF, $f_s = 50$ MHz and a maximum allowable distortion of 80 dB, the maximum switch on-resistance, R_{max} should not exceed 540 Ω.

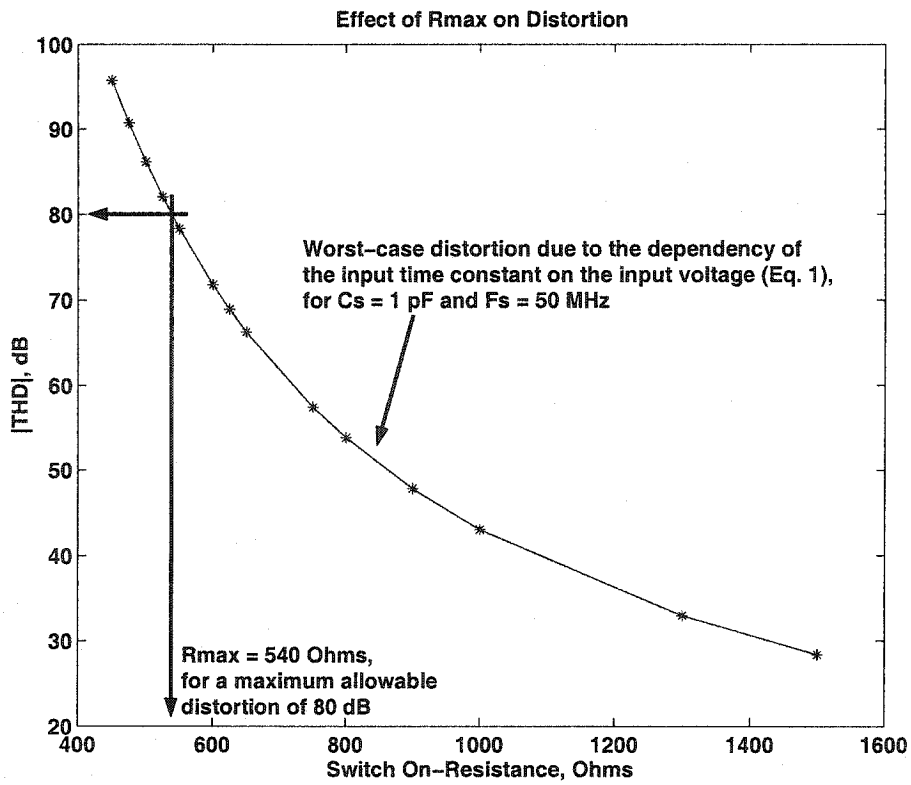


Figure 2.15 Distortion Due to Finite On-Resistance.

2.3.3 - Building Block Specifications Synthesis

Figure 2.16 summarizes the dependency of *SNR* on the circuit non-idealities, when independently swept. Only one variable was swept at a time, while the other variables were made ideal. In other words, for each one of those plots, a different non-ideal block diagram was generated, with the variable to be swept being the only non-ideal parameter. Only *BW* and *SR* were incorporated together in the same non-ideal block. For that, the *BW* (*SR*) plot was obtained while keeping the *SR* (*BW*) fixed.

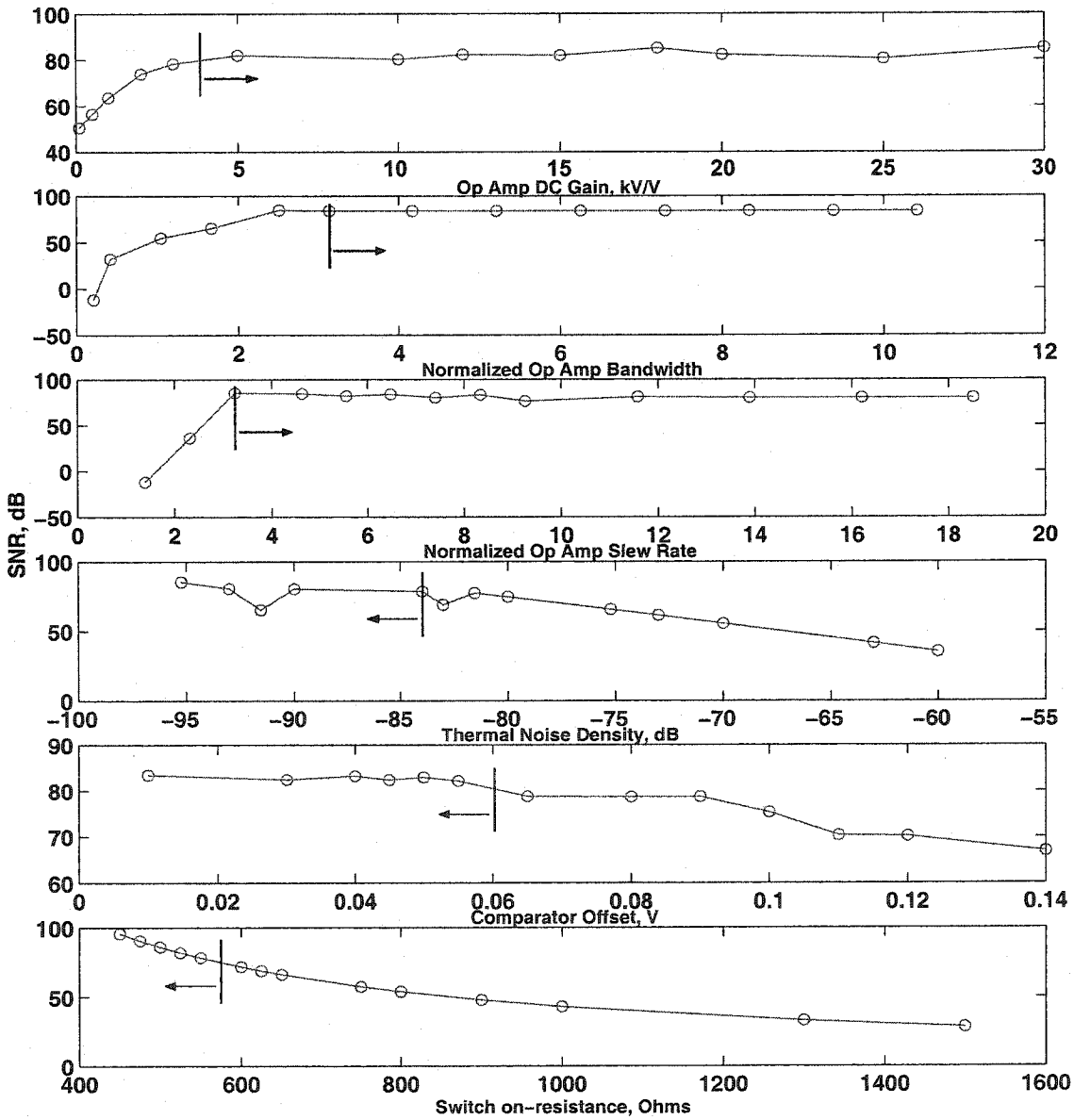


Figure 2.16 Peak *SNR* versus Normalized Time Constant for C_S = 1 pF, and All Other Parameters.

Since the plots are monotonic with the increase in *SNR*, the minimum OTA DC gain, *BW*, *SR*, thermal noise, comparator offset as well as the input switching network time constant could be deduced.

In summary, in order to design a 13–bit ΔΣM suitable for ADSL applications, the following specifications are needed:

- Input sampling capacitance (C_s) = 1 pF
- Input time constant ($\tau = R \cdot C_s$) = 0.54 ns
- OTA *DC gain* = 4000 V/V
- OTA *SR* = 150 V/μsec
- OTA *BW* = 200 MHz
- OTA input noise density (S_n) = 3.1 nV/$\sqrt{\text{Hz}}$
- Comparator offset = 60 mV

2.3.4 - Method Verification/Validation

From the plots, and based on the assumptions that the *SNR* is dependent on each parameter separately, it is therefore possible to deduce an expression for the *SNR* that has the following form:

$$SNR = a_0 + a_1 \cdot f_1(\text{BW}) + a_2 \cdot f_2(\text{SR}) + a_3 \cdot f_3(\text{DC Gain}) + \ldots . \qquad (2.22)$$

The support of this claim requires long derivations and curve fittings to derive the coefficients in Eqn. (2.22). This is beyond the scope of this thesis. Instead, a less rigorous approach was adopted.

In order to validate the separation of variables method and therefore the non-correlation between the different circuit non-idealities, block specifications meeting the goal *SNR* and deduced from one-dimensional sweeps were then incorporated all together in the full non-ideal model of the modulator shown earlier in Figure 2.10. Two dynamic range plots, the first corresponding to all the blocks being ideal and the second corresponding to the blocks being non-ideal with circuit parameters corresponding to the independently synthesized

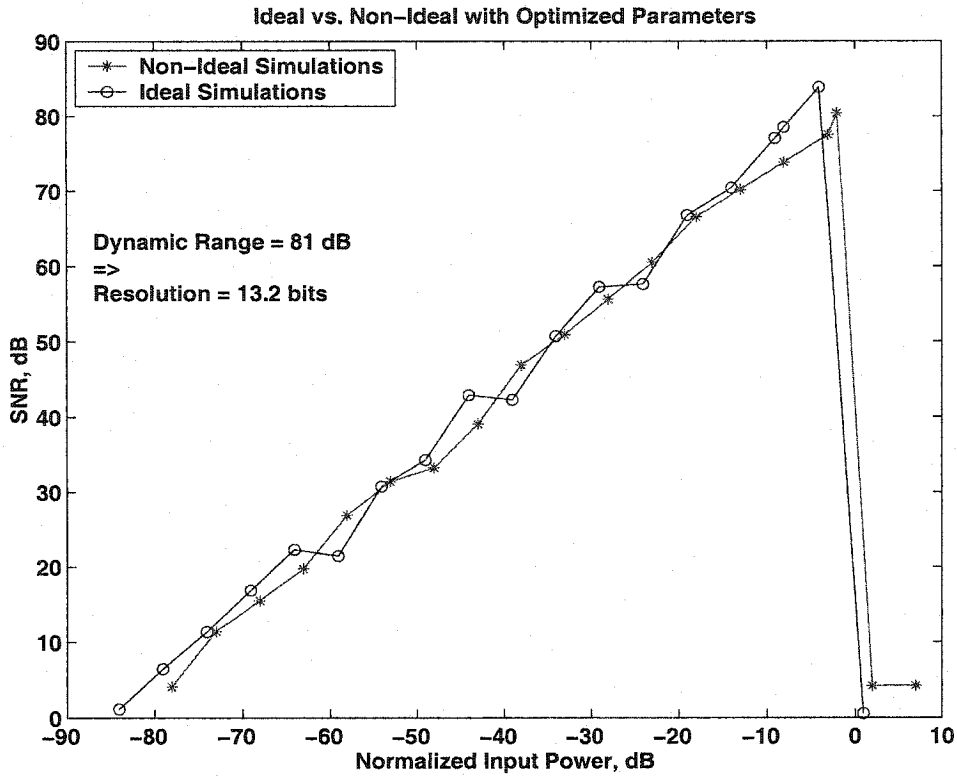


Figure 2.17 *SNDR* plot of Ideal versus Non-Ideal with Optimized Parameters.

variables are shown in Figure 2.17. The similarities between those two plots validate the little interaction existing between the different circuit non-idealities and as a result, the choice of the *independently* synthesized parameters. Had there been strong correlation between the variables, degradation in the *SNR* plot would have been observed. More conservatively stated, assuming independence can provide a practical means for achieving a target specifications in the presence of complex and unpredictable interactions between many circuit non-idealities.

2.4 - Conclusions

A fast synthesis methodology for deducing the minimum design specifications of the building blocks of a broad band ΔΣ ADC was presented. It was shown that a time-consuming multi-dimensional optimization is not necessarily needed and that tools that easily integrate analog and digital blocks with good DSP capabilities such as Matlab/Simulink could still be used to optimize with a reasonable amount of simulation time. By observing the weak relation existing between the different parameters to be

optimized, simple sweeps were proven enough for all practical purposes to reach the optimum set of circuit block parameters that meet the goal *SNR* while still minimizing power. This method was applied to the design, on the system-level of a fourth-order, single-bit ΔΣM. The architecture choice and the derivation of the coefficients for maximum dynamic range were presented in details.

Chapter 3 - Single-Bit ΔΣ ADC

In the previous chapter, a systematic method for designing modulators was presented. Circuit specifications on the main building blocks were derived while keeping optimization time to a minimum. In this chapter, the mapping of those specifications into circuit implementation is explained. In particular, the details of the OTA circuit are presented first, followed by the implementation of the comparator, switches, clock generator and capacitor arrays. The switched-capacitor implementation of the full ΔΣM is then presented with simulation results to validate the circuit design.

3.1 - OTA

The selection of the OTA topology includes a lot of trade-offs. A good summary of the different selection criteria and choice advantages and disadvantages can be found in [4]. Due to its high-frequency operation, folded cascode was the topology of choice. The OTA circuit can be seen in Figure 3.1 where two modifications (which will be explained next) were adopted with respect to the regular folded cascode OTA. This was done at the expense of higher power dissipation. This additional power dissipation is inevitable if the specifications on the OTA derived in Chapter 2 are to be met. However, optimization on these additional stages could and was performed in order to keep the additional power dissipation to a minimum. The two modifications are explained next.

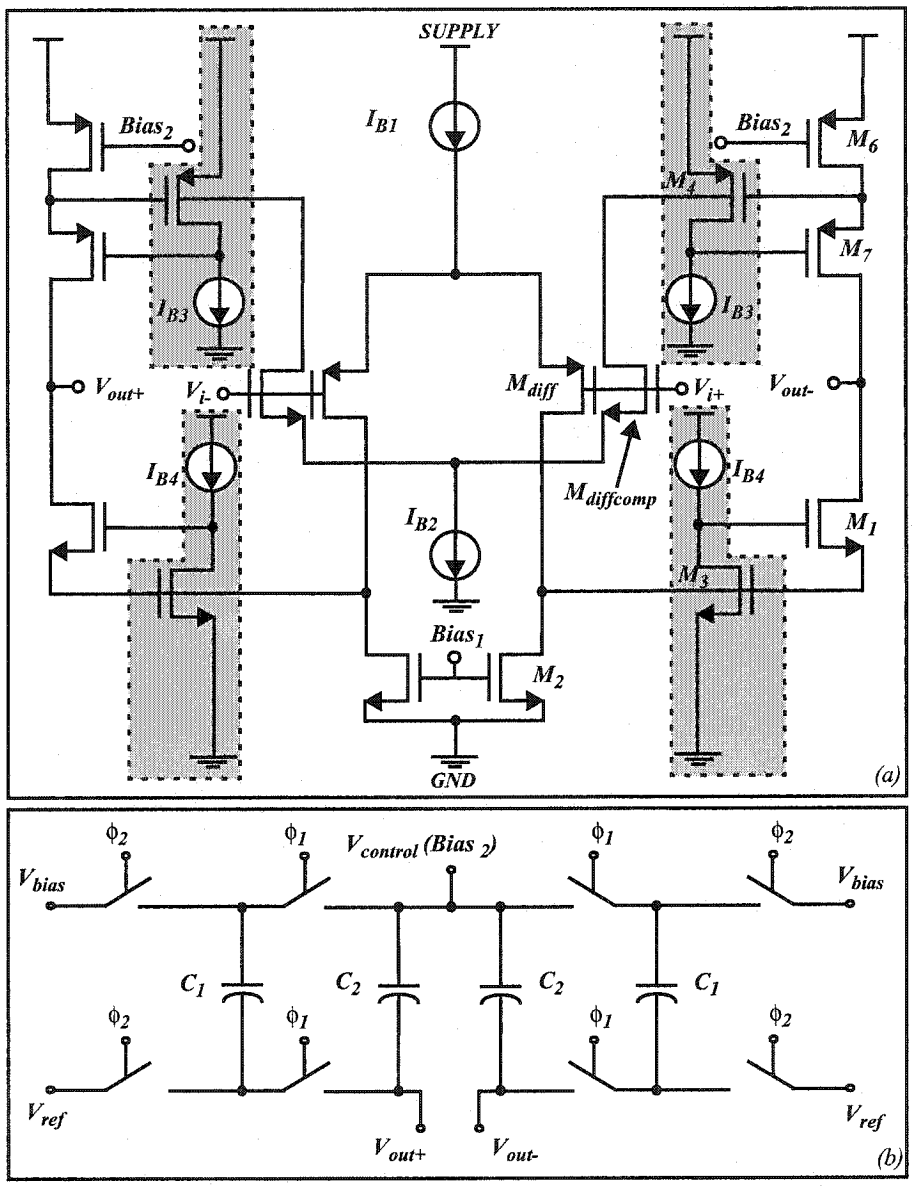


Figure 3.1 Schematics of a) the Folded Cascode OTA with Gain Boosting, b) SC-CMFB.

- *Complementary differential pairs were selected at the input stage. This increases the effective g_m of the input differential pair helping therefore increase the unity-gain frequency. Since the OTA is to be used around the input common-mode range where the transconductances of both PMOS and NMOS pairs add up, no extra constant-g_m circuit arrangement was needed [31].*

- *Output gain boosting stages were added. While these stages help increase the DC gain of the OTA, if not designed properly, they could degrade the frequency behavior, and*

increase the settling time of the OTA. The current in that stage needs therefore to be carefully designed.

A small-signal analysis on the gain boosting stage is performed next, with the different design trade-offs outlined.

3.1.1 - Low-Frequency Behavior

Gain Boosting

First, the low-frequency analysis is carried out to see how the DC gain is affected. For now, the analysis ignores parasitic capacitances and computes the output impedance from a purely resistive point of view. This is useful for analyzing the effect of including the stage on the DC gain.

The reader is referred to Appendix A for a detailed derivation of the equations. Only final results are shown here.

A simplified expression for the output impedance with gain-boosting is:

$$r_o = (r_{o,n} \| r_{o,p}) = [(g_{m3} \cdot r_{o3}) \cdot (g_{m1} \cdot r_{o1} \cdot r_{o2})] \| [(g_{m4} \cdot r_{o4}) \cdot (g_{m7} \cdot r_{o7} \cdot r_{o6})] \quad (3.1)$$

From Eqn. (3.1) we can readily see the advantage that gain boosting offers in terms of increasing the output impedance, and as a result, the DC gain. Assuming that the PMOS stage has a lower $(g_m \cdot r_o)$ product, an increase of the order of magnitude $(g_{m4} \cdot r_{o4})$ can be achieved. Trade-offs exist in sizing and biasing transistors M_3 and M_4 in order to increase the gain but not degrade the frequency performance of the amplifier. Namely, increasing the size of transistor M_3 increases g_{m3} and therefore the output impedance r_o, which in turn increases the gain. This however increases the parasitic capacitances which degrade the high frequency characteristics of the OTA. In order to better understand the trade-offs that exist in sizing the transistors in the gain-boosting stage, a frequency analysis, details of which are presented in Appendix A, was carried out.

Complementary Differential Pair

The addition of the complementary differential pair at the input has the advantages of increasing the bandwidth and providing a faster step response [31][32]. This is the result

of increasing the effective transconductance, $g_{meffective}$, which becomes the sum of both transconductances, g_{mdiff} and $g_{mdiffcomp}$.

As a result, the DC gain and bandwidth are increased by a factor of $\frac{g_{mdiffcomp} + g_{mdiff}}{g_{mdiff}}$.

The above analysis assumed operation at low frequencies and didn't include the effect of capacitances at the various nodes. An analysis including the high-frequency behavior is described next.

3.1.2 - High-Frequency Behavior

Matlab modelling for all the poles and zeros of the OTA, accounting for the addition of both gain boosting stages and the complementary differential pairs was carried out, the details of which are presented in Appendix A.

A plot of the AC response of the overall amplifier, for different currents in the gain-boosting stage (which directly determine the poles locations) as a function of the current in the main stage of the OTA is shown in Figure 3.2.

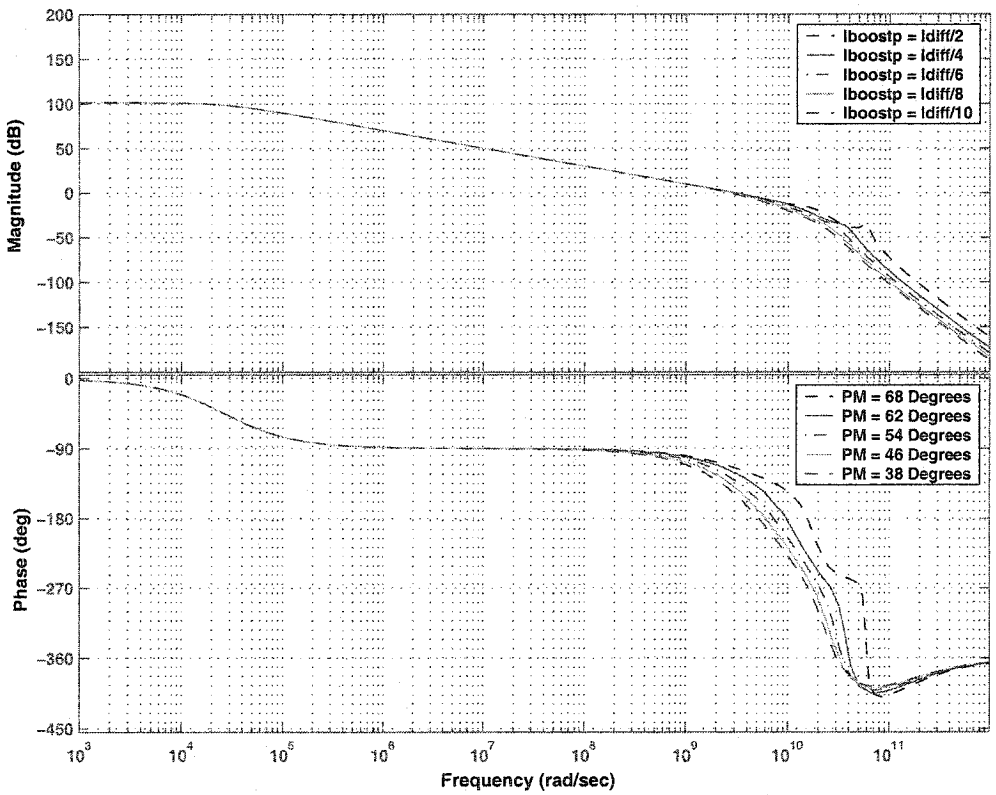


Figure 3.2 AC Response of the OTA as a Function of the Gain Boosting Current.

The corresponding step responses are shown in Figure 3.3.

From the plot, a current in the P gain-boosting stage equivalent to $1/6$ the current in the main OTA stage is expected to give optimum results without degradation in the high-frequency behavior. While larger currents in the gain boosting stage increase the phase margin, it also increases the power dissipation. The current in the N gain-boosting stage was chosen approximately 1.7 times the current in its P-gain boosting counterpart.

With lower boosting currents, overshoots and possible ringing exist due to a reduced phase margin, *PM*. The choice made here is that overshoots are allowed provided that the ringing, if any, dies out and the error at the end of the clock phase is no more than 0.01% of the final value, which corresponds to a 13-bit accuracy. In other words, provided that $9.2 \cdot \tau \leq \frac{T_s}{2} =$ 10 ns in the case of a 50 MHz sampling rate, then the design was assumed

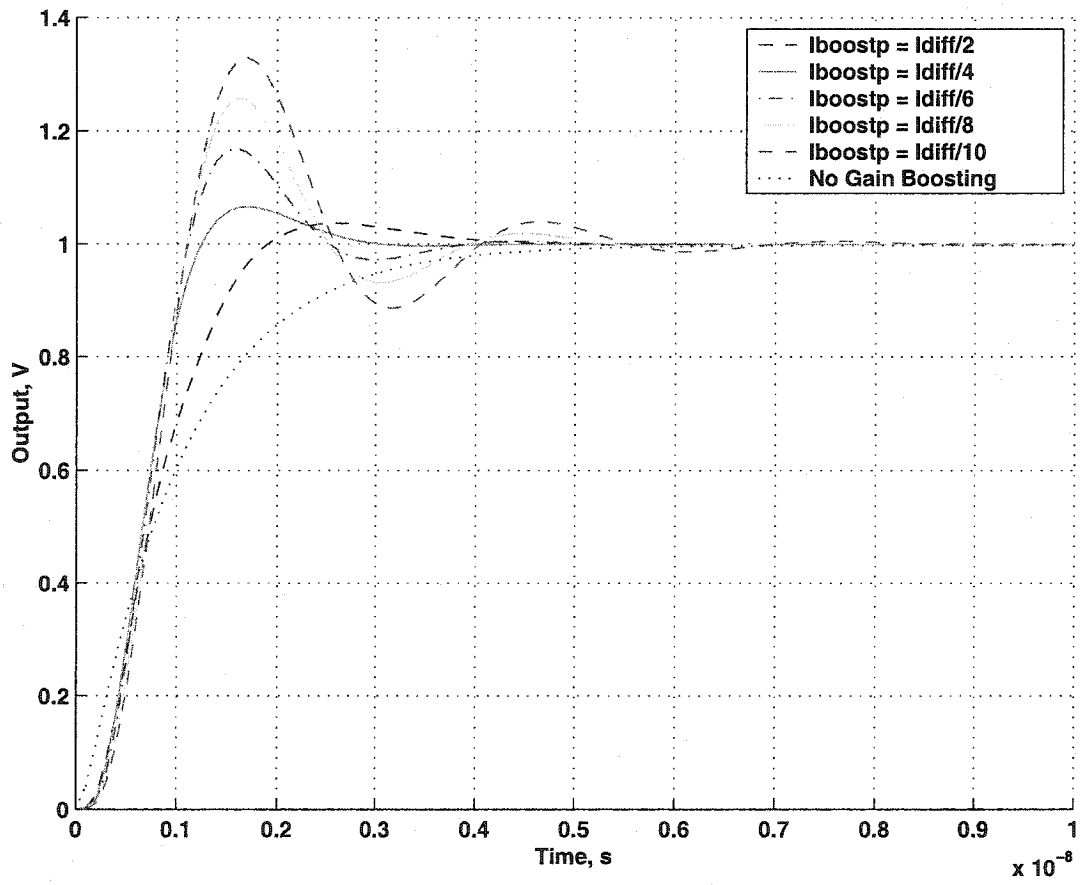


Figure 3.3 Step Response of the OTA as a Function of the Gain Boosting Current.

feasible. While keeping in mind that this design choice is more sensitive to process variations, it is the drawback for minimizing the power dissipation.

With the previous criteria in mind, the OTA was designed to meet the specifications derived earlier in Chapter 2. After some iterations on the step response, the current in the gain boosting stage was decreased to a ratio equal to $1/8.8$. While not optimum according to the Matlab analysis which predicted an optimum ratio of $1/6$, the analysis in Matlab adopted a simplified model and was used as a starting point only. Plots of the AC magnitude and phase, shown in Figure 3.4, reveal a differential DC gain of 100 dB, phase margin of 58°, and a unity-gain bandwidth of 410 MHz when driving a 1.5 pF capacitive load. A continuous-time CMFB was used for the AC simulations.

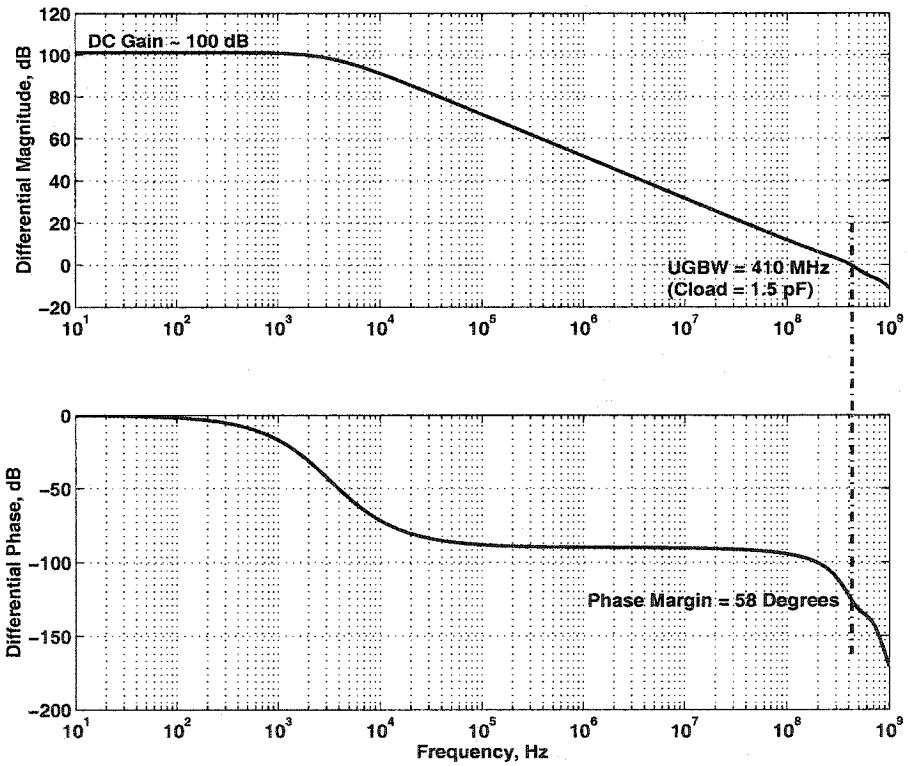


Figure 3.4 OTA AC HSpice Simulations: Magnitude and Phase.

The OTA was then connected in a unity-gain configuration with the other OTA input driven by a 500 kHz, 0.4 V_{p-p} pulse. Since the switched-capacitor (SC) CMFB has a direct effect on the settling behavior of the OTA, it was essential to perform this test with the actual SC-CMFB used in the final implementation. Transient response of the OTA is shown in Figure 3.5. When driving a 1.5 pF effective capacitive load, a rising slew rate of 246 V/μsec was achieved while the falling slew rate was measured to be 236 V/μsec.

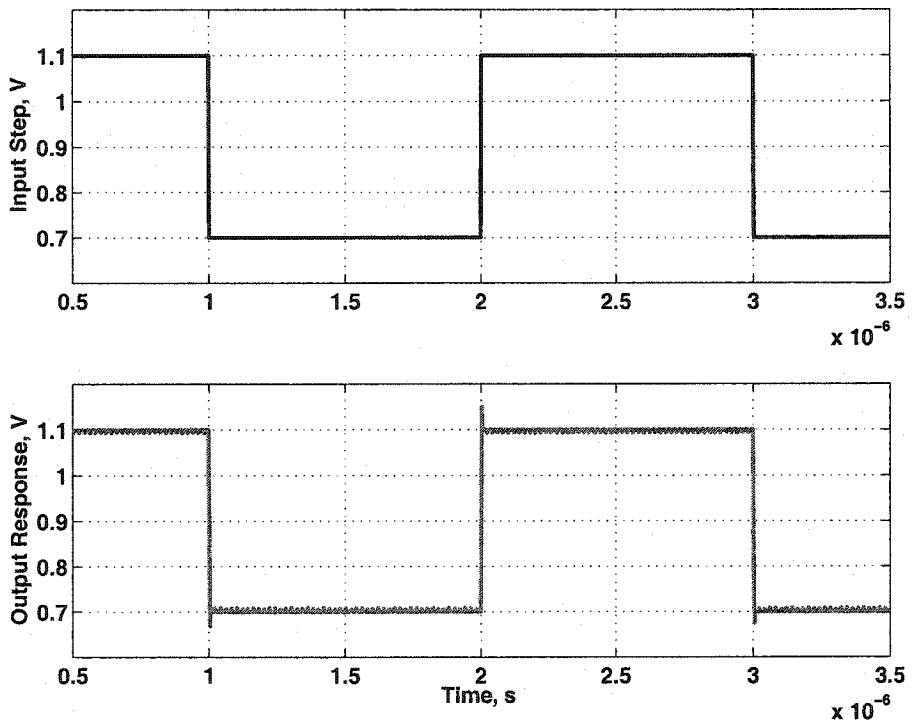


Figure 3.5 OTA HSpice Transient Simulations: Step Response.

3.2 - Comparator

A CMOS dynamic comparator with a clocked RS latch was used to implement the latched comparator (Figure 3.6). The implementation is straight forward. While a pre-amplification stage helps reduce the offset due to mismatches in the latches, it is also responsible for increasing the power dissipation. Given the relaxed offset requirements on the comparator circuit, it was deemed unnecessary to include a pre-amplification stage. The comparator core is shown in Figure 3.6 (a). It consists of an input differential pair and two cross-coupled inverters for positive feedback. When ϕ_1 is high (equivalently, when ϕ_2 is low), the NMOS transistors of the cross-coupled inverters are reset to a certain logic level while the PMOS transistors are reset to VDD. As soon as ϕ_1 goes low, the reset state is over and the two inputs are compared and amplified. The data is then latched on the rising edge of the Latch signal, using the clocked RS latch shown in Figure 3.6 (b).

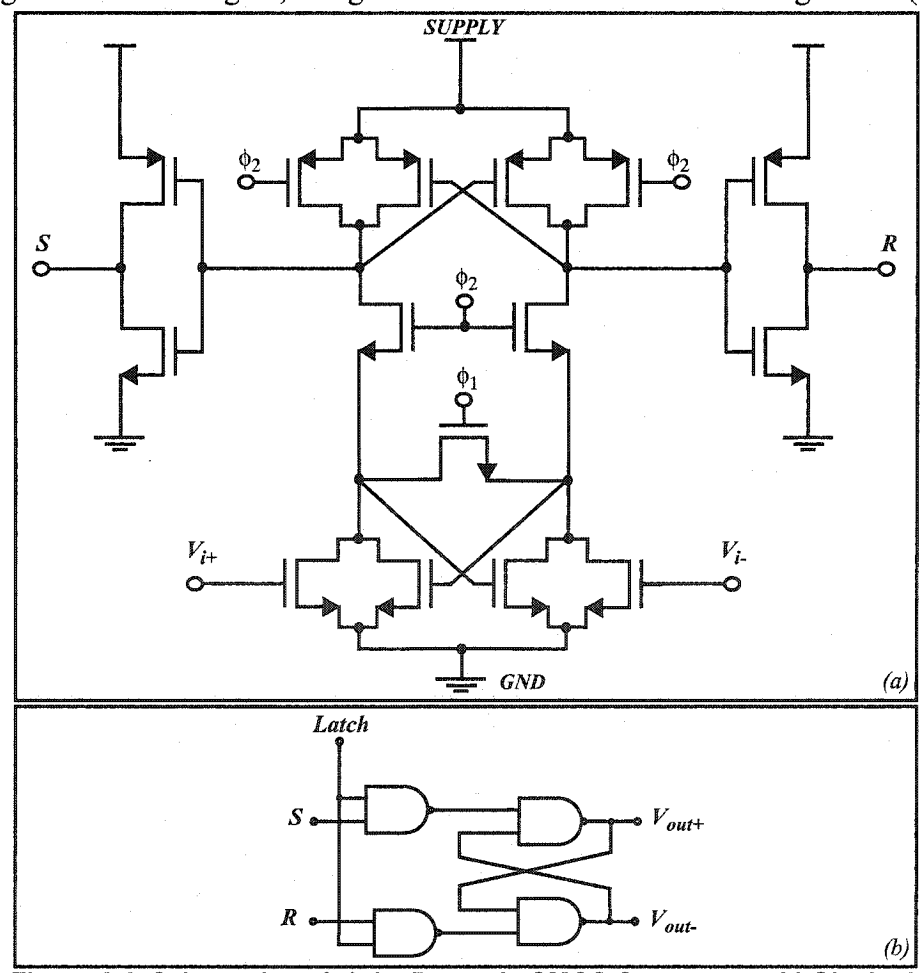


Figure 3.6 Schematics of a) the Dynamic CMOS Comparator, b) Clocked RS Latch (gate-level representation).

The comparator was tested with an input sequence that checks its ability to resolve the correct logic level for different input steps. This dynamic testing for the comparator, together with the input sequence, clocks, and output waveforms are shown in Figure 3.7. The extracted with parasitics performance reveals a resolution of ~ 11 bits (corresponding therefore to an LSB of 879 uV).

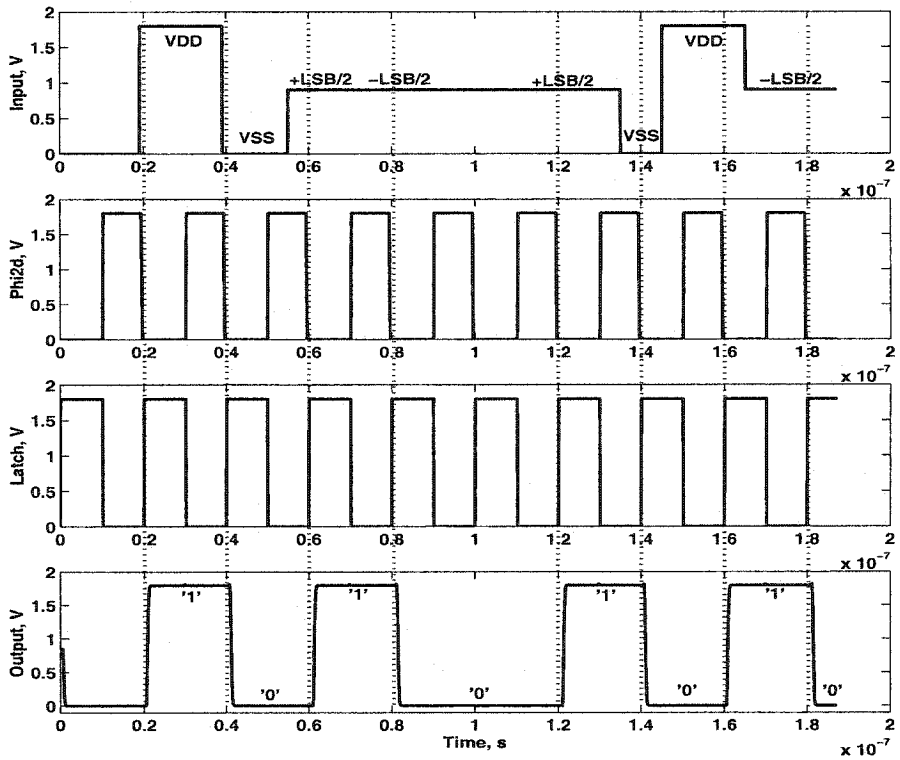


Figure 3.7 Comparator Dynamic Test Results.

3.3 - Switches

The switches were implemented using regular transmission gates. In order to keep the total resistance across the sampling capacitor below 540 Ω while minimizing parasitics and charge injection, the width and length of the NMOS and PMOS transistors were chosen equal to 30 μm and 0.18 μm respectively. Simulation of the transmission gate on-resistance was achieved using the circuit setup [33] shown in Figure 3.8. By sweeping the input voltage, V_{test}, and fixing the test current, I_{test}, to 200 μA in this case, the on-resistance is given by Eqn. (3.2)

$$R_{on} = \frac{v_1 - v_2}{I_{test}} = \frac{v_{test} - v_2}{I_{test}}. \tag{3.2}$$

Simulation results of the transmission gate on-resistance as a function of the $(v_1 - v_2)$ voltage across are shown in Figure 3.9. The peak value reads 119 Ω which guarantees a total on-resistance of the two switches across the sampling capacitor less than 540 Ω while allowing for some safety margins.

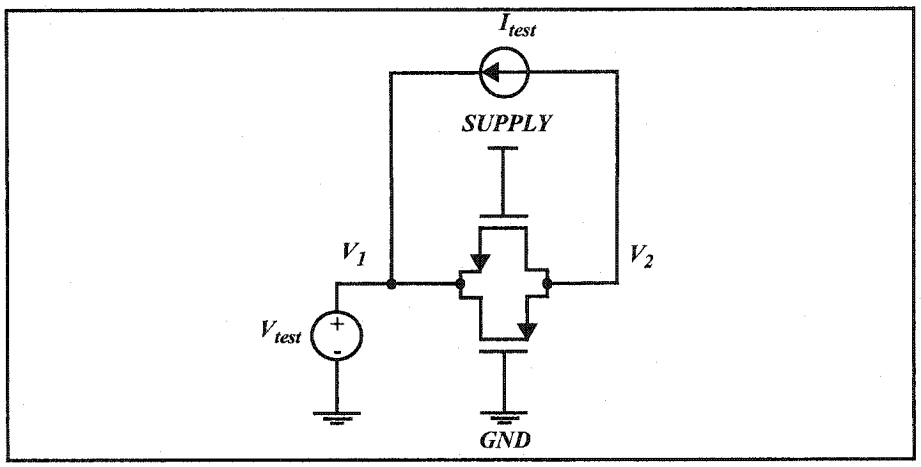


Figure 3.8 Circuit Setup to Calculate R_{on}.

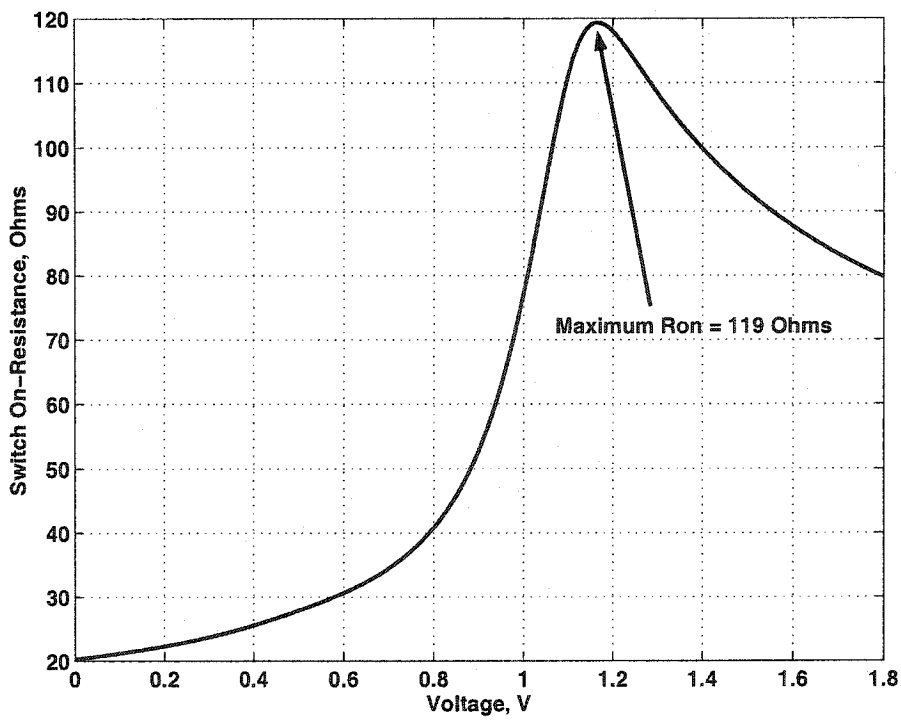


Figure 3.9 R_{on} of the Transmission Gate.

3.4 - Clock Generator

A four-phase clock generator circuit, shown in Figure 3.10, was used to generate the non-overlapping phases. Both clocks and their complementary phases were generated since all switches were implemented using transmission gates. Delayed versions of all clocks were also generated in order to minimize charge injection. A delay of 200 ps was used while 600 ps of non-overlap (equivalently, 1.2 ns per period) was adopted. While more delays and more non-overlap are desired, this is not feasible at high frequencies where a large non-overlap implies large percentage of the clock being unused, and therefore, less settling time for capacitors in the circuit.

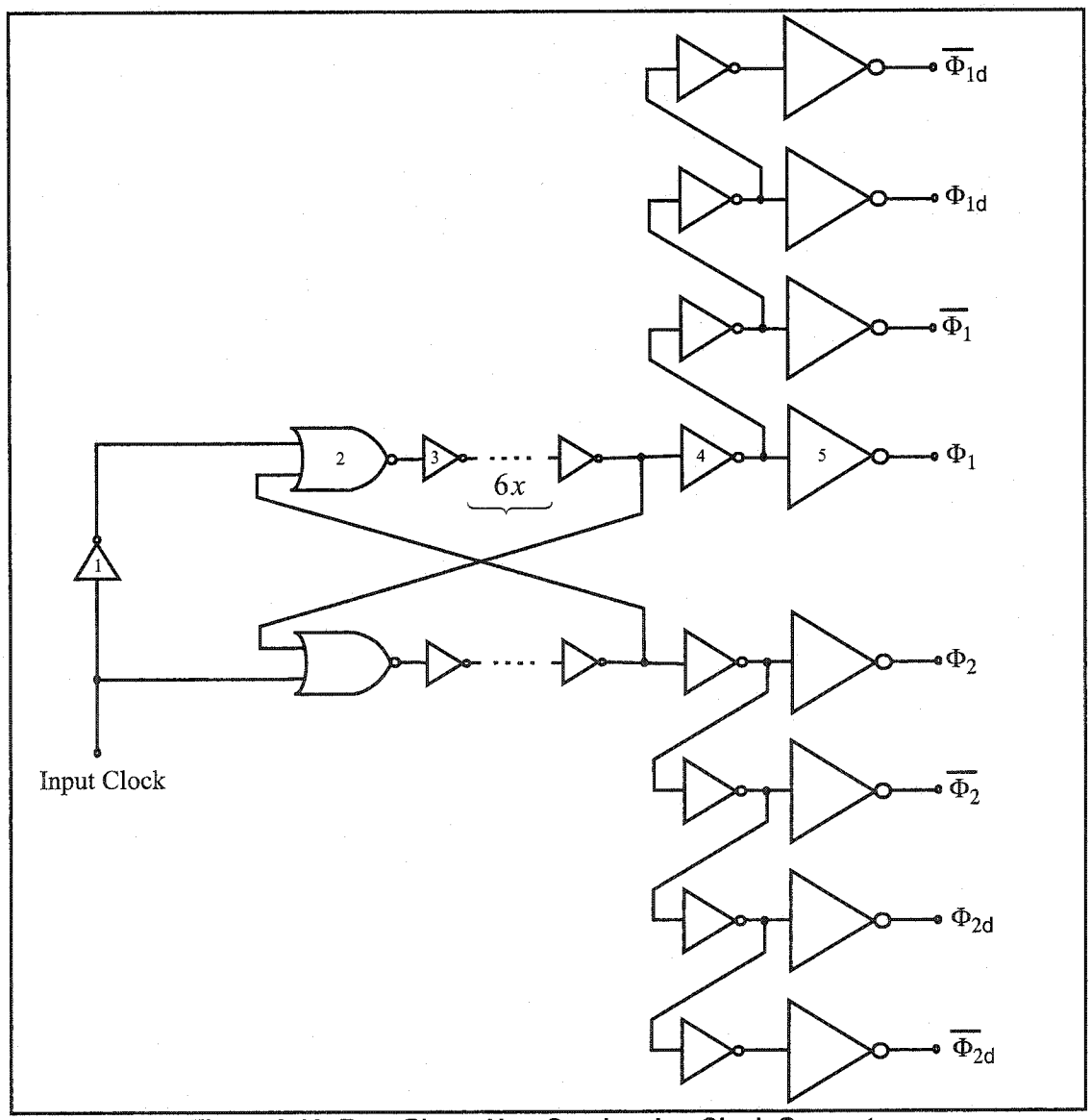


Figure 3.10 Four-Phase Non-Overlapping Clock Generator.

The transistor sizing for the clock generator circuit is summarized in Table 3.1, while the resulting clock waveforms are shown in Figure 3.11.

Table 3.1 - Clock Generator Transistor Sizing.

Gate	NMOS (μm/μm)	PMOS (μm/μm)
1	10/0.18	20/0.18
2	10/0.18	50/0.18
3	10/0.35	20/0.35
4	25/0.18	55/0.18
5	100/0.18	260/0.18

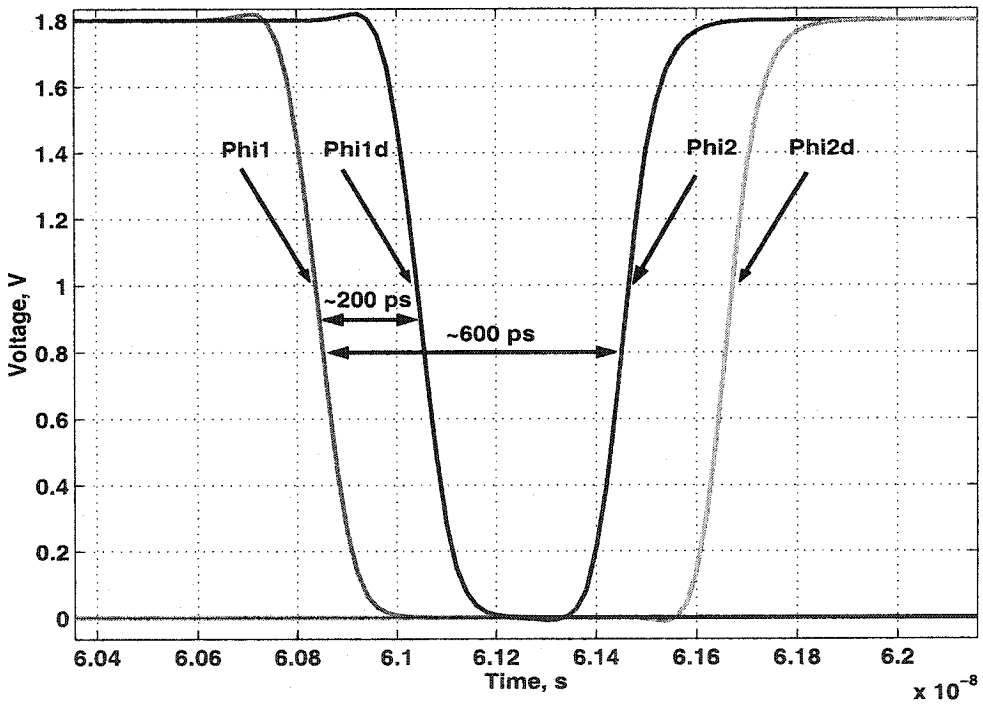


Figure 3.11 Clock Waveforms.

3.5 - Summary of Designed Specifications

Having presented the circuit implementation of the main building blocks in the design of the ΔΣM, a summary of the Matlab/Simulink synthesized versus Cadence/HSpice designed parameters is shown in Table 3.1.

Table 3.1 - Summary of Synthesized versus Designed Circuit Specifications.

Circuit Block	Non-Ideality	Synthesized	Designed
OTA (C_{load} = 1.5 pF)	DC Gain (dB)	72	100
	Bandwidth (MHz)	293	410
	Slew Rate (V/μs)	220	236/246
	Thermal Noise Density ($nV/\sqrt{Hz}$)	3.1	2.36
Comparator	Offset (mV)	60	-
Switch R_{max}	$R_{max} = f(V_{in})$ (Ω)	540	119

3.6 - Layout Considerations

3.6.1 - Capacitor Array

While absolute capacitor values are not critical in switched-capacitor designs, matching is of utmost importance since capacitor ratio is primarily responsible for pole/zero placement in the system. Shift of these poles/zeros result in different NTF's and STF's which could possibly result in an increased noise in the band of interest. In some cases, instability might even occur, but is unlikely to happen, since the system should be designed to be stable under the worst-case variation in capacitor values.

In order to achieve best matching, all capacitors were built from a unit-size capacitor equal to 125 fF. The capacitors were constructed from metal-metal capacitors. Metals 3 through 6 were used, while metals 1 and 2 were avoided due to their increased parasitic capacitances with respect to the substrate. Common centroid techniques were used to give good matching. An example of matching two 250 fF capacitors is shown in Figure 3.12.

Node A constitutes the top plate of the capacitor and is used to connect to sensitive nodes (such as op. amp. inputs), due to its lower parasitic capacitances, while node B constitutes the lower plate of the capacitor and connects to less sensitive nodes (such as op. amp. output nodes).

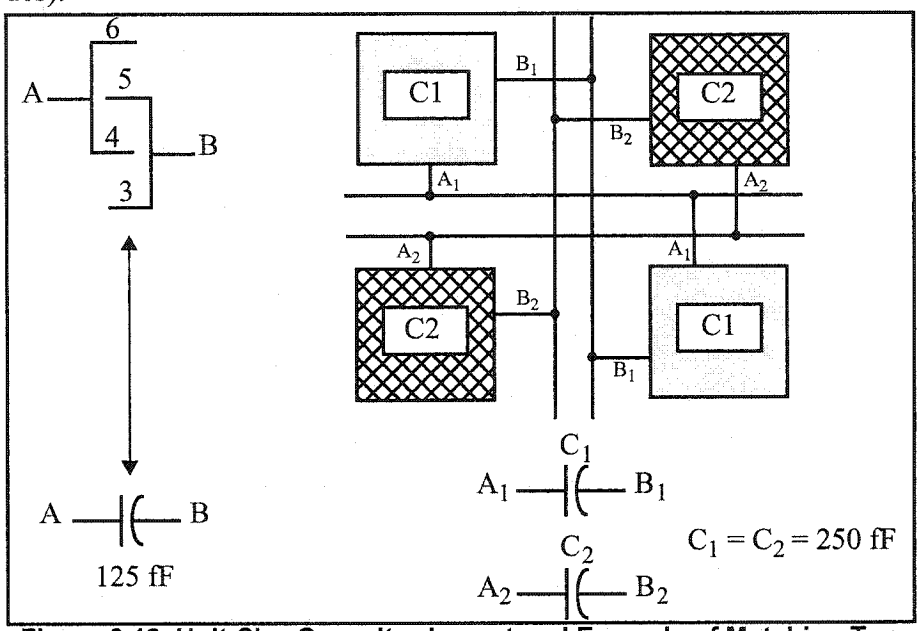


Figure 3.12 Unit-Size Capacitor Layout and Example of Matching Two 250 fF Capacitors.

Using the same strategy of matching capacitors, Figure 3.13 shows how the capacitors (all scaled down by a factor of 4 for simplicity) of the first-stage integrator in the fully differential structure are laid out.

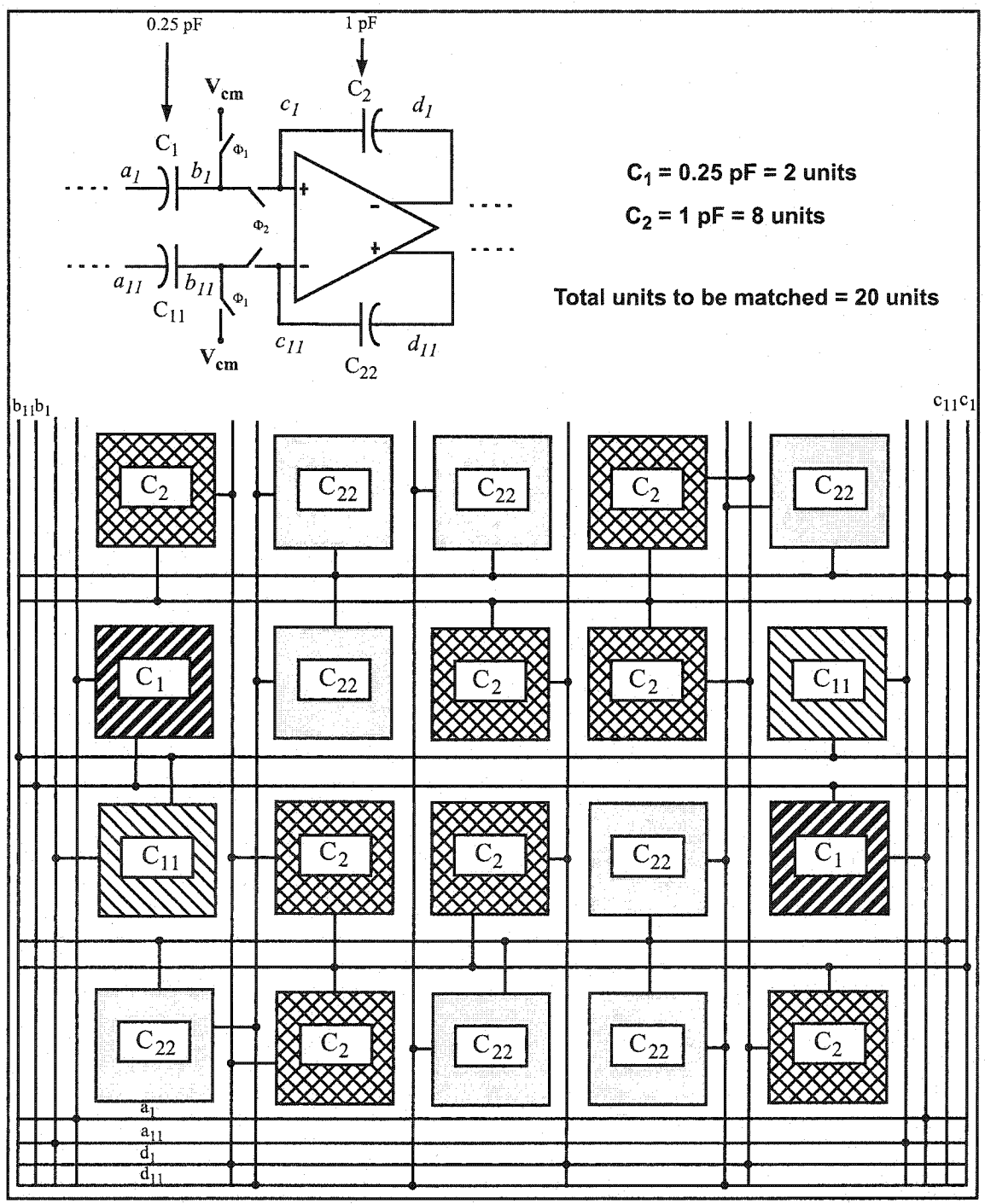


Figure 3.13 Capacitor Layout of the First-Stage Integrator. (scaled down by a factor of 4)

The ease of mapping and as a result, ease of repeatability of any number and values of capacitors using this technique into matched units makes it very attractive, especially in the design under consideration where different stages with different capacitors need to be matched. The main drawback of such layout technique is the increased parasitics due to the long interconnect metal lines. This could be, and was accounted for when designing the capacitor arrays by incorporating the capacitive parasitics of the interconnect into the capacitors to be matched.

3.6.2 - Circuit Floorplan

A good layout floorplan is an essential part in the integration of the full circuit. The building blocks, circuit details of which were outlined throughout this chapter, were then put together and laid out according to the floorplan shown in Figure 3.14.

The advantage of such layout floorplan is that the digital buses run horizontally, while the analog connections run vertically and are made as short as possible.

The disadvantage however is the increased length of digital buses which results in increased capacitive load and delay on the clock lines. This however was necessary in order to decrease and possibly eliminate analog and digital buses running in parallel. The buffers at the output of the clock generator were made large enough to drive the long digital lines without excessive increase in their rise/fall time.

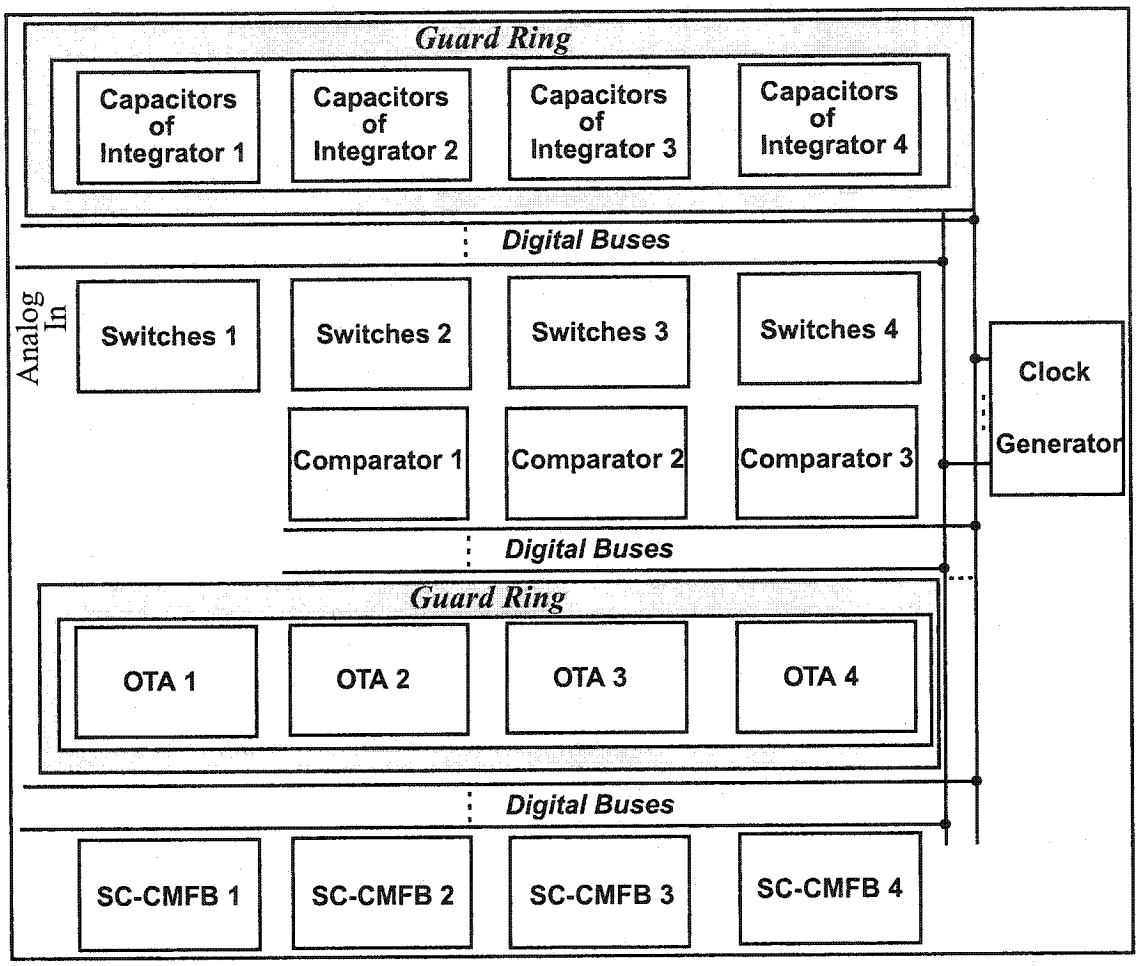


Figure 3.14 IC Core Layout Floorplan

Techniques such as separation of analog and digital blocks, as well as the addition of guard rings around sensitive blocks were adopted.

The overall circuit, shown in Figure 3.15, was implemented in TSMC 0.18 μm, single-poly 6-metal, 1.8 V supply CMOS technology. The extracted with full parasitics performance of the IC achieves 82 dB peak *SNR* and is shown Figure 3.16. The total power dissipation is 18.8 mW. The IC prototype, shown in Figure 3.17 and occupying an area of 3.4 mm x 3 mm, was fabricated with experimental results presented later.

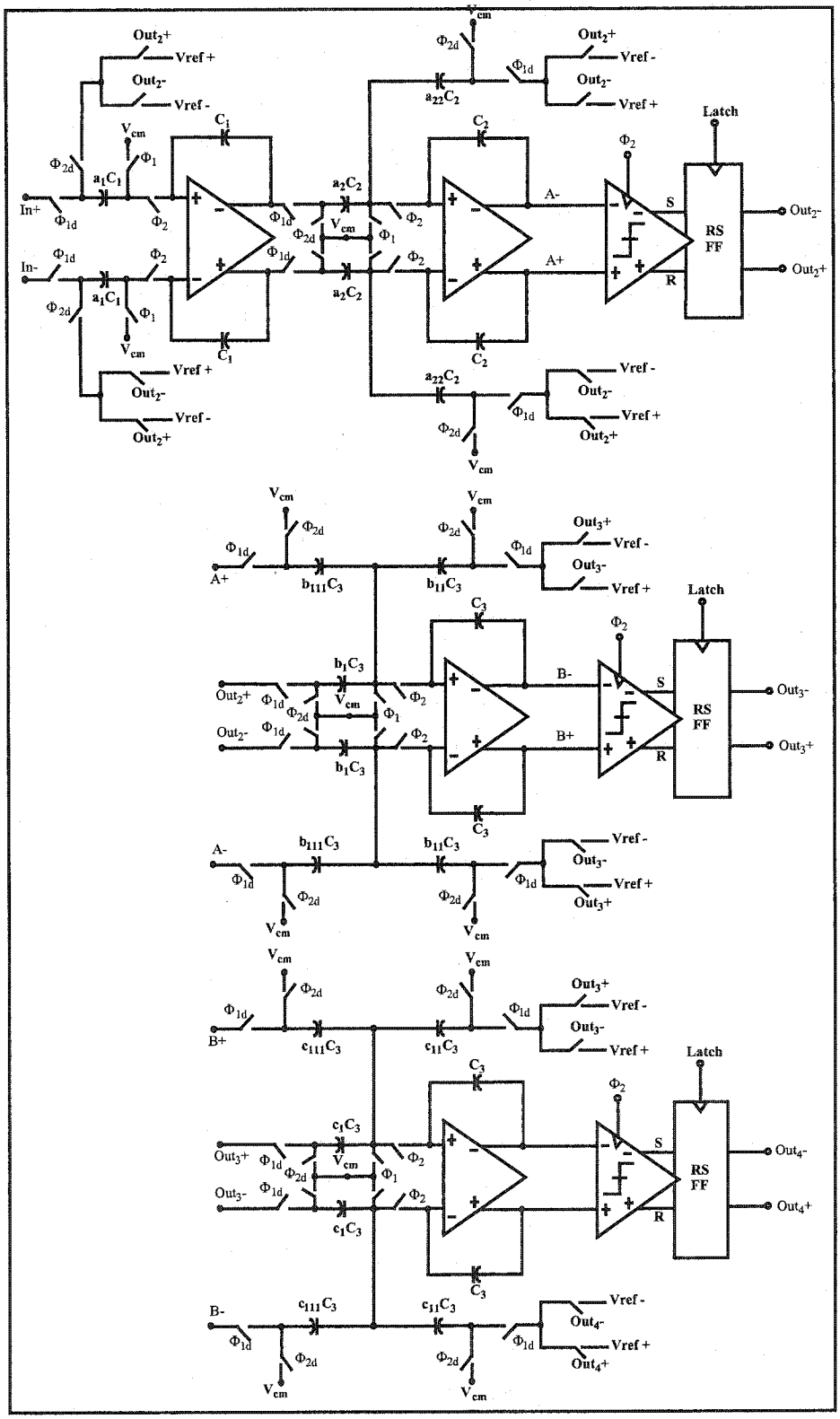


Figure 3.15 SC Implementation of the Single-Bit Modulator.

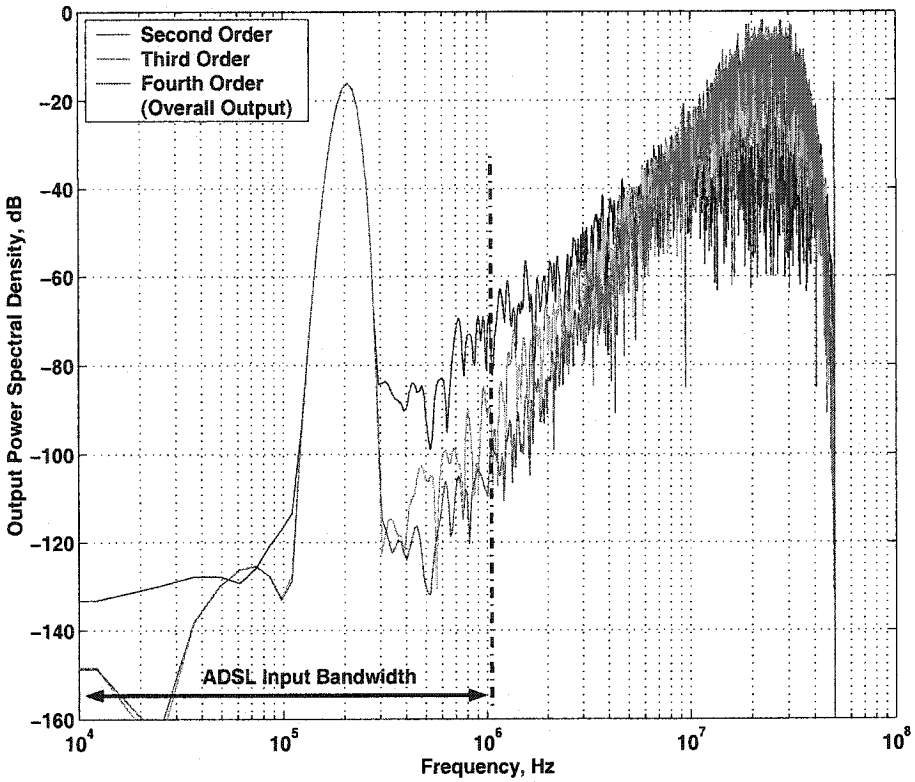


Figure 3.16 Output Power Spectral Density of the Extracted with Full Parasitics of the IC Implementation.

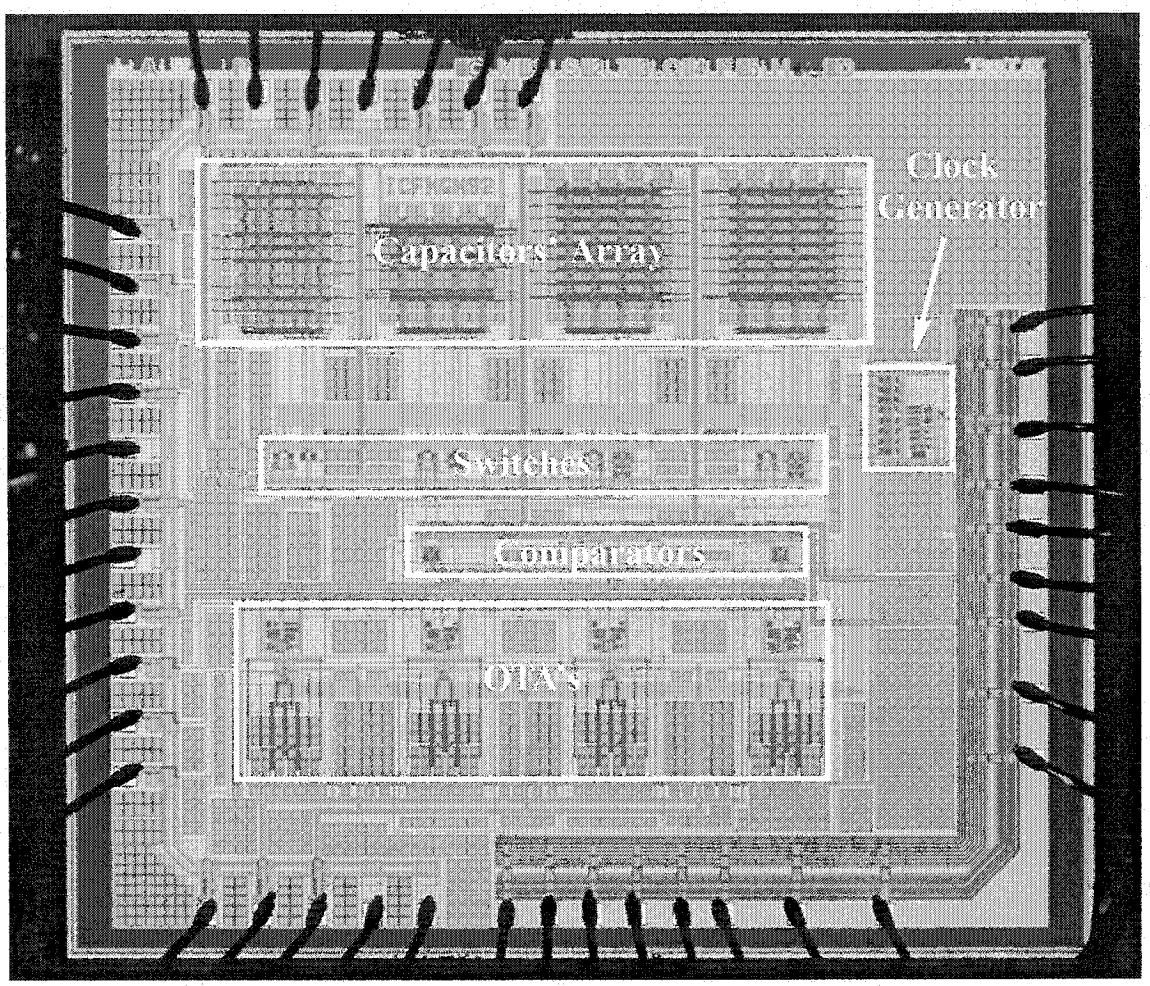


Figure 3.17 IC Implementation.

3.7 - Conclusions

A low-power low-voltage 2 MS/s output rate ΔΣM for ADSL applications was designed in TSMC 0.18 μm CMOS process. The modulator consumes 18.8 mW power when sampled at 50 MHz. A systematic method was used when designing the modulator was presented in the earlier chapter. In this chapter, the focus was on the circuit design and implementation of the main building blocks of the modulator including the OTA, comparator, switches, clock generator and capacitor arrays. All these blocks were then integrated in a prototype IC, the simulation results of which were presented. A subsequent chapter will be dedicated for the experimental results.

Chapter 4 - Multi-Bit ΔΣ ADC

In previous chapters, the design of a single-bit ΔΣ ADC was presented. This chapter deals with extending the performance of the ADC to the 14 bits or more of resolution. This will be achieved using multi-bit quantization. With multi-bit quantization, non-linearities associated with the digital-to-analog converter (DAC) become a concern. While the main building blocks used in this design are identical to those described in Chapter 3, focus here will be placed on the analysis of the DAC non-idealities and their effect on the system performance. DAC Integral- and Differential-non-linearities (INL and DNL) will be introduced and conclusions drawn about implementation choices. The full SC circuit implementation will also be presented and validated by simulations.

4.1 - Introduction

Given an *OSR* (and therefore a sampling rate, f_s) and a modulator order, n, improving the modulator's performance designed previously could be achieved by using a multi-level quantizer and a more complex feedback DAC. Increasing the number of bits in the quantizer by one results in an extra effective bit in the resolution of the modulator [1]. Therefore, in order to improve the resolution of the modulator designed previously by 2 bits, a 3-bit quantizer resulting therefore in an 8-level output is needed. The multi-bit quantizer will be used in the last stage only of the modulator as shown in Figure 4.1, with coefficients summarized in Table 4.1.

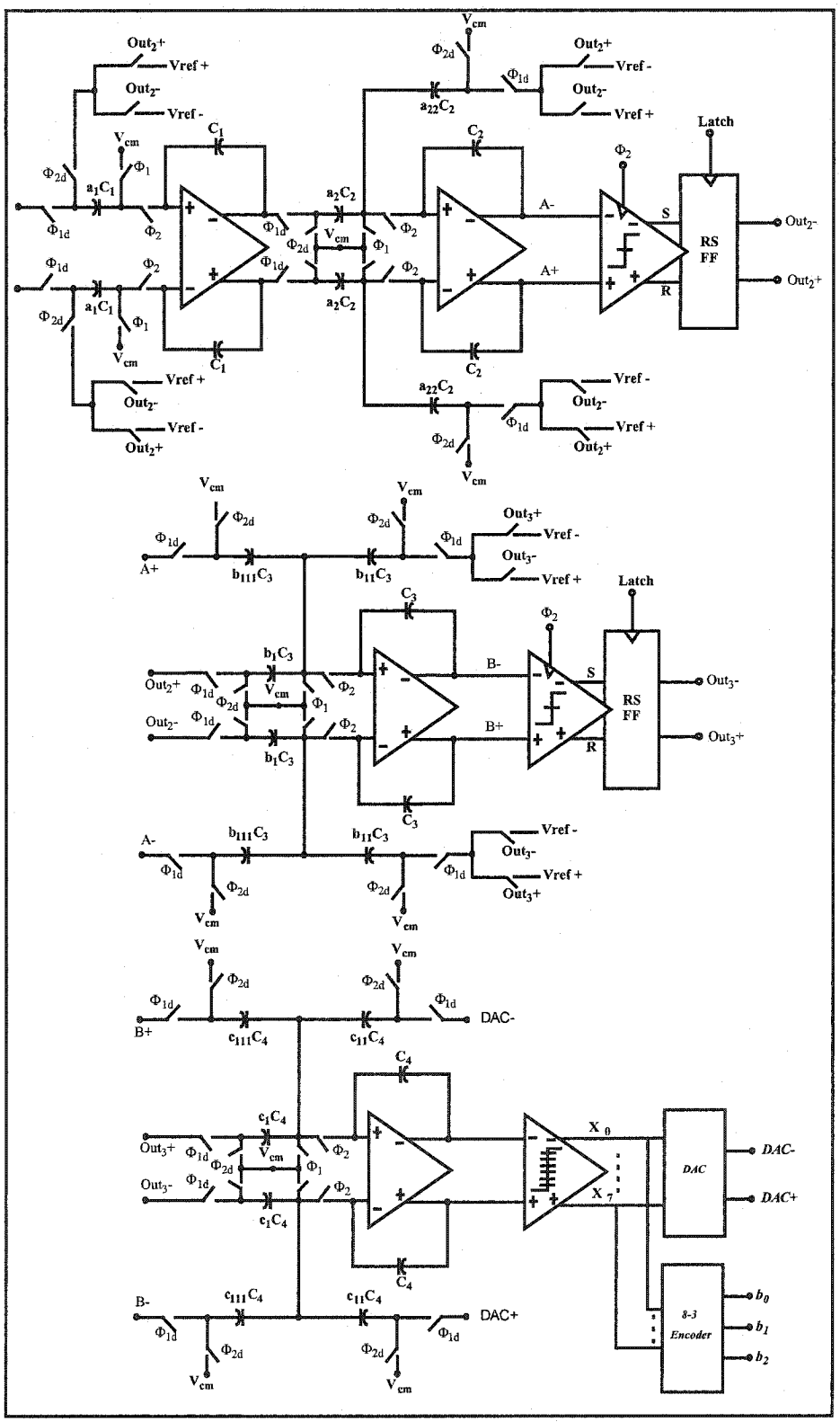


Figure 4.1 SC implementation of the Multi-bit Modulator.

Table 4.1 - Summary of Coefficients Used in the Multi-Bit ΔΣ Modulator Shown in Figure 4.1.

Coefficient	Coefficient Value
a_1	1/4
a_{11}	1/4
a_2	1/2
a_{22}	1/4
b_1	1/4
b_{11}	1/4
b_{111}	1
c_1	1/2
c_{11}	1/4
c_{111}	2
e_1	-1
e_2	2
e_3	0
e_4	1

Coefficients e_1 - e_4 refer to the digital error cancellation block which is identical to the one shown earlier in Chapter 2 and is therefore not presented here.

4.2 - DAC Non-Idealities in Multi-bit Quantization

First, a justification for the need of a multi-bit quantizer in the last stage only is given. The overall output of the modulator [6] shown in Eqn. (4.1) could be derived in a way similar to that outlined in Chapter 2

$$V_{out}(z) = In(z) \cdot \frac{1}{z^4} + E_3(z) \cdot e_4 \cdot \left(\frac{z}{z-1}\right)^4 - E_{DAC}(z) \cdot e_4 \cdot \left(\frac{z}{z-1}\right)^3. \qquad (4.1)$$

From Eqn. (4.1), two facts are observed:

- *The overall output is "ideally" a function of the last stage quantization noise only. So only the last-stage quantizer/DAC are theoretically needed to be multi-bit if performance improvement is desired. Having multi-bit quantization in the first two stages is therefore not beneficial.*
- *The DAC non-linearity errors are shaped by a third-order transfer function (due to the three integrators preceding it). Using multi-bit DAC's in previous stages causes the non-*

linearity to be shaped by a transfer function of lower order, placing therefore more stringent requirements on the DAC linearity.

For the above two reasons, multi-bit quantization in the last stage only will be used. This also helps in reducing the power dissipation.

The effect of the DAC non-linearity is discussed next. As mentioned earlier, with multi-bit quantization, the DAC linearity becomes a concern when high resolution ΔΣ ADCs are required. If the DAC exhibits non-linearities that exceed the overall system linearity requirement, then the converter will be limited to the DAC accuracy. Different calibration techniques were proposed in the literature to improve the performance of the internal DAC, either in the analog domain through the use of individual level averaging (ILA) [34], or data weighted averaging (DWA) [35], or in the digital domain [36], [37]. Each one of the proposed methods has advantages and disadvantages which won't be discussed here. One common feature to all these correction techniques is that they improve the DAC linearity at the expense of additional power dissipation. For the design under consideration, and in order to keep the power dissipation to a minimum, system-level simulations presented next will show that the required DAC INL is believed to be met with a simple resistor string and careful resistance choice and layout techniques.

The effect of the DAC Integral-Non-Linearity (INL) on the overall dynamic range of the modulator was simulated in Matlab/Simulink. The reference voltages in both the ADC and DAC of the last stage of the modulator were deviated from their ideal levels. To do so, an additive noise source having a Gaussian distribution, with variance (noise power) swept between 0 *LSB* (ideal DAC curve) and 1 *LSB*, where *LSB* = Least Significant Bit, and defined as follows:

$$1LSB = \frac{V_{FS+} - V_{FS-}}{2^N - 1}. \tag{4.2}$$

The DAC INL was then calculated using the best-fit line method [38] with the results of the selected INL curves shown in Figure 4.2. The corresponding *SNDR* as a function of input power of the modulator is shown in Figure 4.3. From the plots, it can be seen that

provided that the maximum DAC INL is limited to $0.15 \cdot LSB$, the achievable dynamic range is 92 dB corresponding to a resolution of 15 bits.

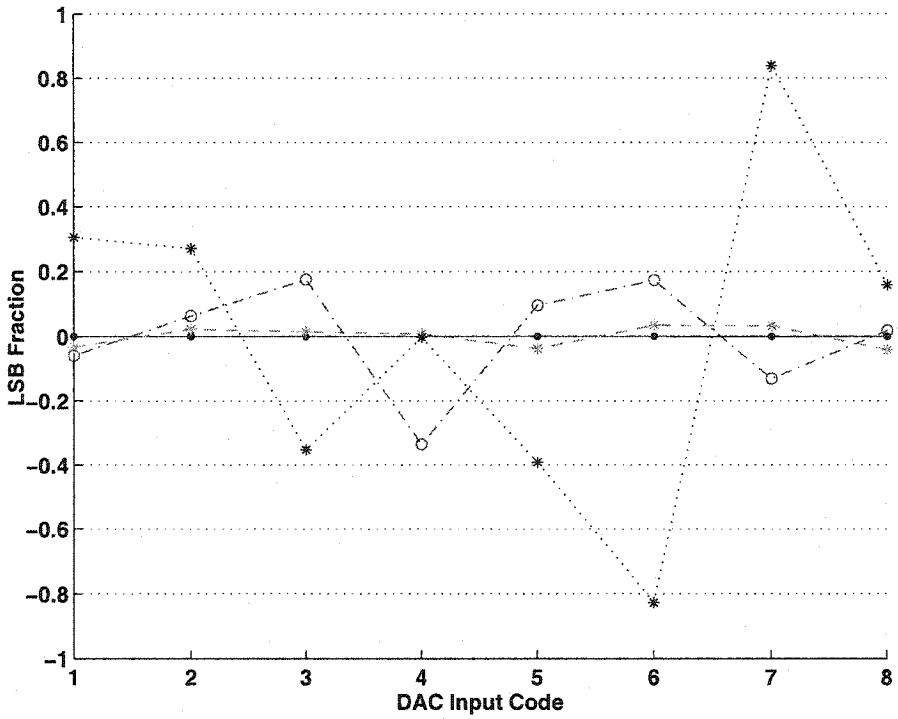


Figure 4.2 INL for Different Non-Ideal DAC Transfer Curves.

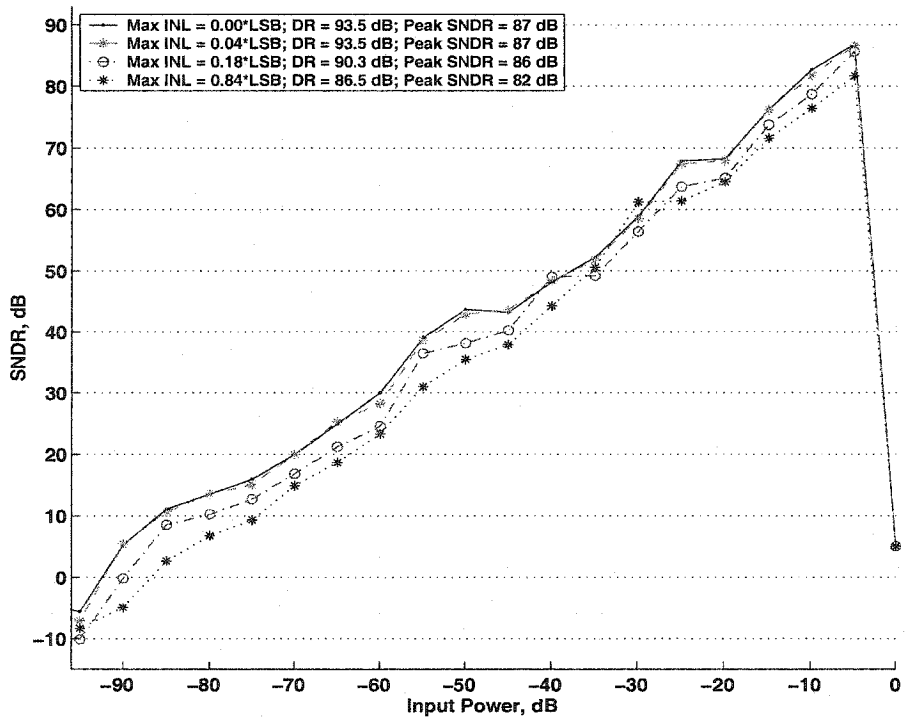


Figure 4.3 *SNDR* for the Non-Ideal DAC with INL Shown in Figure 4.2.

4.3 - Circuit Implementation

Only circuit blocks relevant to the multi-bit implementation, namely the multi-bit ADC, DAC and output encoder, are discussed here. The other building blocks such as the OTA, comparator, switches and clock generator were presented in details in Chapter 3 and were used in this design without modifications.

4.3.1 - Flash ADC

Detailed view of the flash ADC is shown in Figure 4.4. Regular resistor string was used to generate the DC voltage levels of the Flash ADC and the feedback DAC. The resistor values had to be chosen small enough in order not to require a long settling time, but large enough to minimize power dissipation. Values chosen for the resistors also have an impact on the matching which directly affects the resolution of the multi-bit ADC/DAC. As a result, a good compromise was to choose the unit resistance R, equal to 200 Ω.

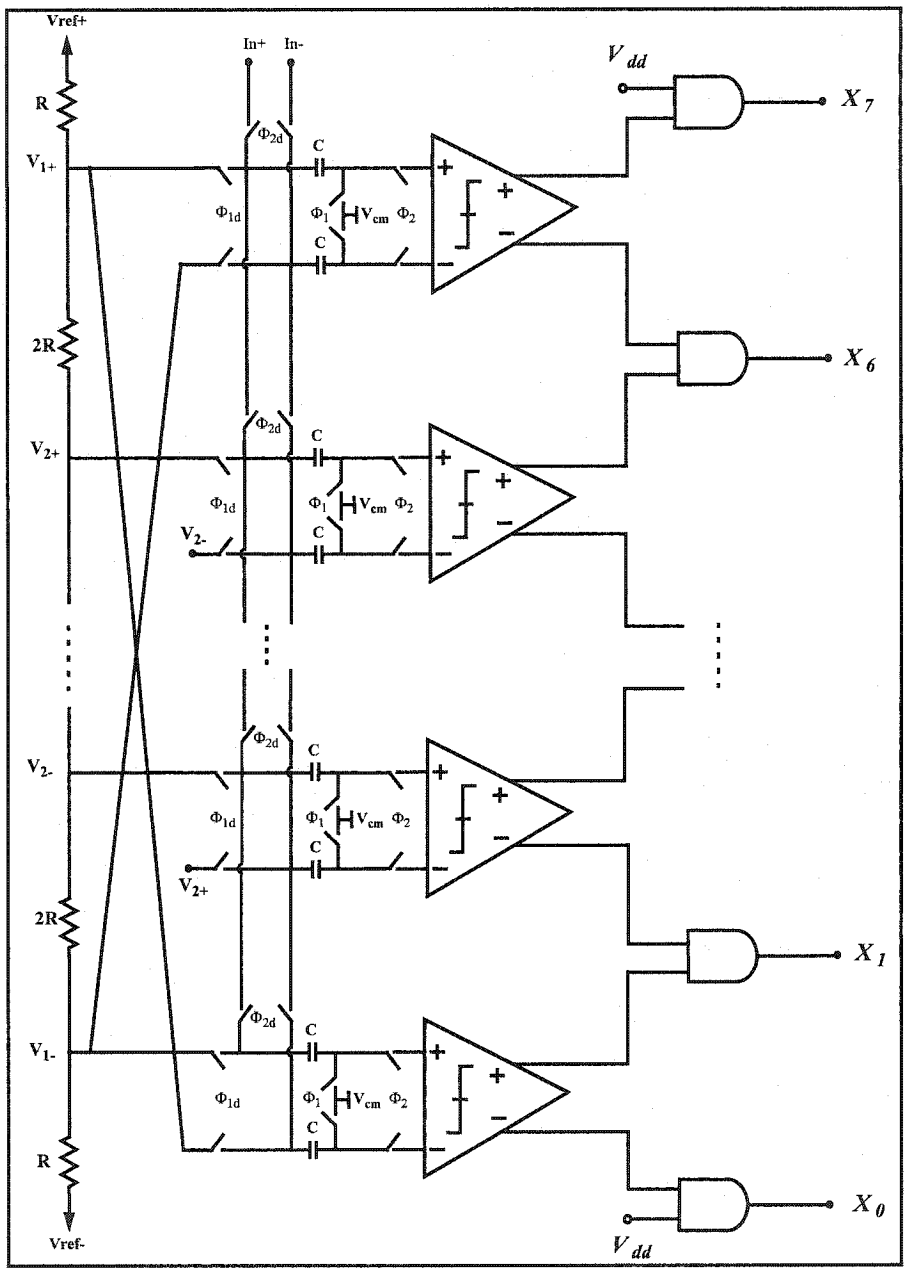


Figure 4.4 Schematics of the Flash ADC Showing the "Bubble" Code Digital Output.

4.3.2 - DAC

As explained earlier, the INL of the DAC had to be kept below $0.15 \cdot LSB$. Assuming a 3-bit DAC with full scale range of about 0.5 V, and using Eqn. (4.2), we get that the noise on the DAC reference voltages due to mismatch in the resistor values generating those levels (as well as some other noise sources such as substrate noise) have to be kept below 10.7 mV.

Since it is only matching between resistors and not absolute values that matters, with proper layout techniques, the matching between any two or more resistors could be made as small as 0.01% (1% being an achievable mismatch ratio with moderate layout techniques) [39].

Even with a moderate matching of 1% between the various resistors, the INL requirement of 10.7 mV is achievable with a simple resistor string.

It is worth mentioning that the choice of the resistor layout dimensions (width and length) also affects the matching percentage between two or more resistors due to process variations. All of the above considerations were taken into account when the resistors were laid out in order to minimize the process variation effects controllable by proper layout techniques.

The switches on the other hand were implemented using regular transmission gates with dimensions of 30 μm/0.18μm for both NMOS and PMOS transistors.

Detailed view of the DAC is shown in Figure 4.5.

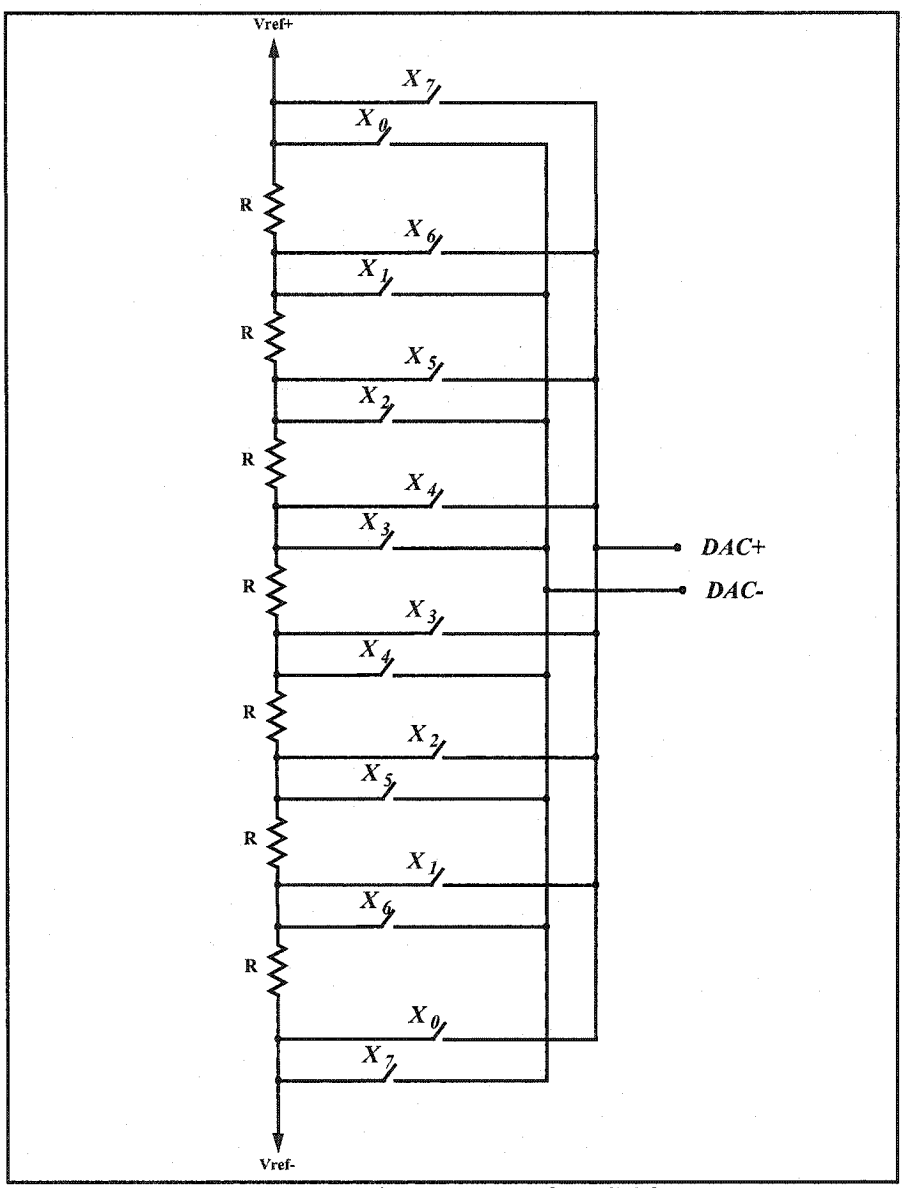


Figure 4.5 Schematics of the DAC.

4.3.3 - Output Encoder

The output of the flash ADC was converted to an 8-bit bubble code and driven off-chip via an 8-3 encoder shown in Figure 4.6. The design of this block is straight forward and is needed to simply minimize the number of digital output pins when taken off-chip. The Boolean expressions for all three outputs as functions of the 8-bubble outputs are also shown in Figure 4.6.

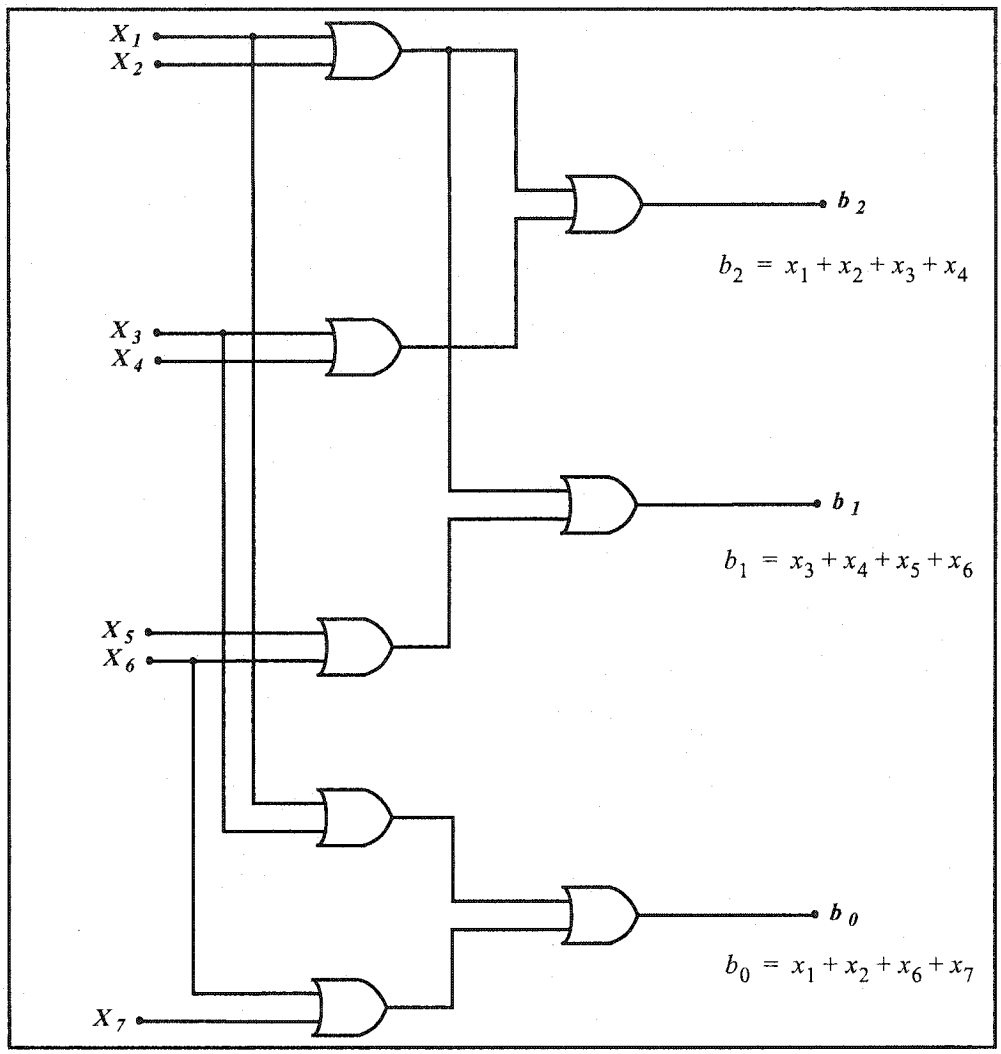


Figure 4.6 Gate-Level Schematics of the 8-3 Encoder.

4.3.4 - Full Circuit and IC Implementation

Building blocks such as OTA, comparators, switches and clock generator were presented in details in Chapter 3 and were used in this design without modifications.

The overall switched-capacitor implementation was shown earlier in Figure 4.1, with coefficients summarized in Table 4.1. The digital error cancellation block was now shown since it is identical to the one presented earlier in Chapter 2. The overall circuit was implemented in TSMC 0.18 μm, single-poly 6-metal, 1.8 V supply CMOS technology.

The IC prototype occupying an area of 3.2 mm x 2.6 mm is shown in Figure 4.7. Due to time and computing power constraints, the IC with full parasitics was simulated to provide an output with only 2048 points. The number of points chosen corresponds to a resolution bandwidth of 24.4 kHz/bin which is not accurate enough to characterize the performance of the modulator. This simulation run was nonetheless deemed essential in providing a high level of confidence about the correct functionality of the chip as well as a rough idea about the noise floor level. The results are shown in Figure 4.8. The peak *SNR* achieved was 89 dB which was deemed sufficient to fabricate the designed IC.

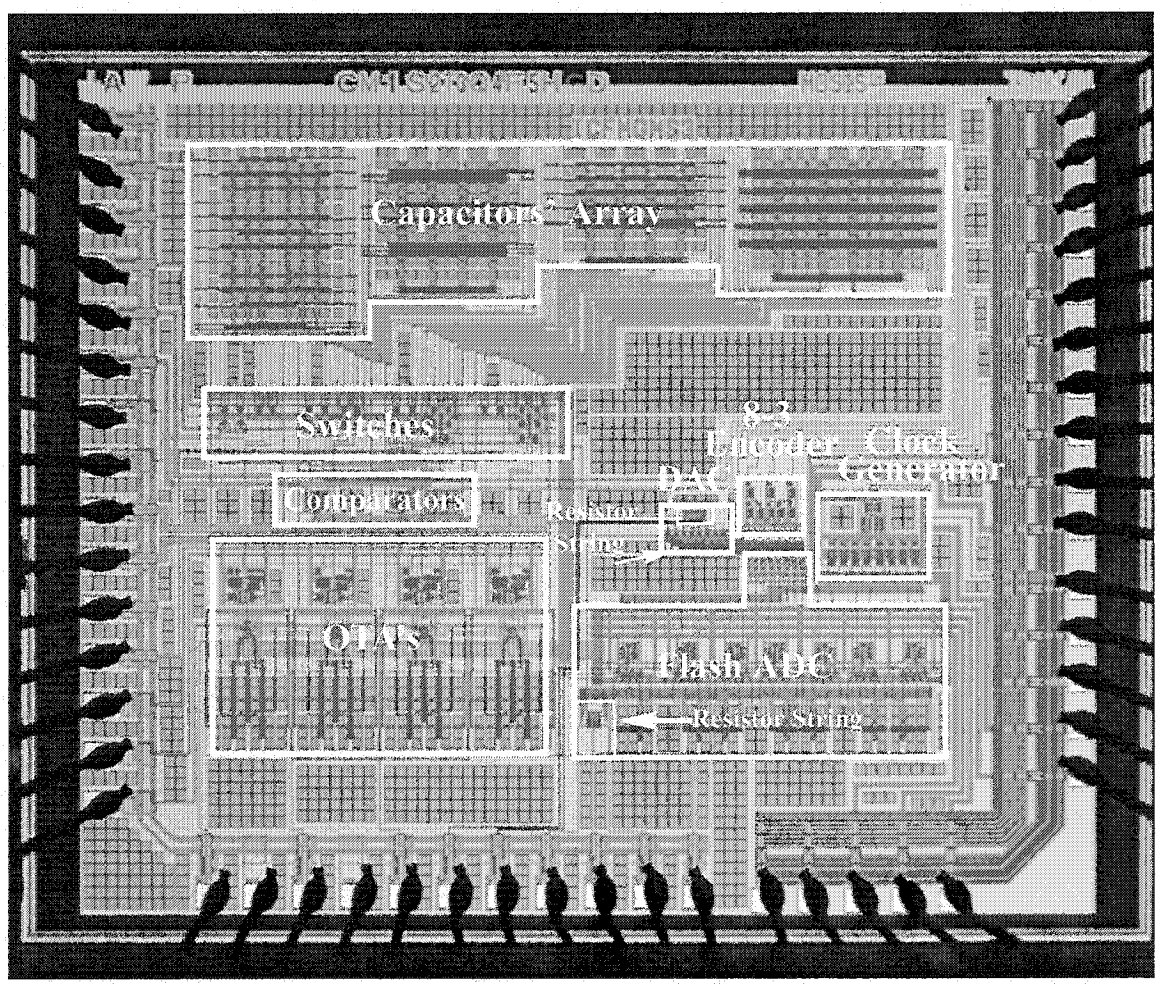


Figure 4.7 IC Implementation.

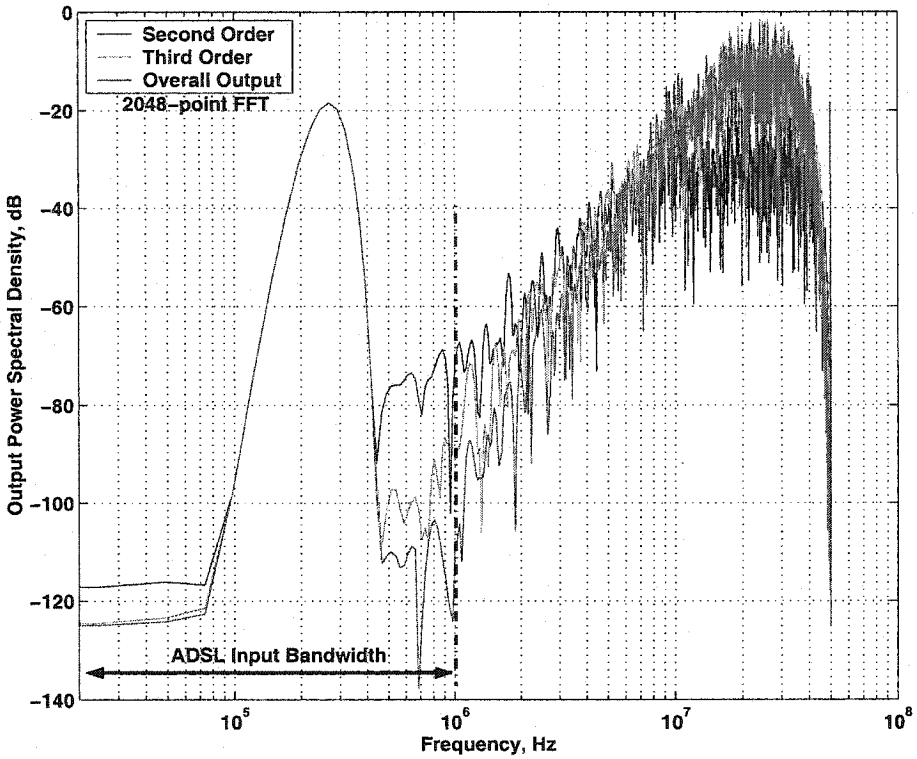


Figure 4.8 Output Power Spectral Density of the Extracted with Full Parasitics of the IC Implementation Shown in Figure 4.7.

4.4 - Conclusions

A low-voltage 2 MS/s Nyquist rate delta-sigma modulator for ADSL applications was designed in TSMC 0.18 μm CMOS process. The modulator is an extension of the previously presented single-bit modulator to multi-bit quantization. It consumes 36 mW power when sampled at 50 MHz and achieves, in simulations, 15 bits of resolution.

Chapter 5 - Experimental Results

This chapter presents the experimental results of both the single-bit and multi-bit modulators. Detailed description of the system, circuit, and layout levels of these modulators were presented in the previous chapters.

5.1 - Single-Bit ΔΣ Modulator

5.1.1 - Test Setup

A Teradyne A567 mixed-signal tester was used to test the fabricated ICs. A C-based language is used to program and control the tester's components.

A two-layer Printed-Circuit Board (PCB) was first designed to be interfaced and mounted onto the tester's Device-Interface-Board (DIB). Power supply decoupling, as well as careful ground plane placement and signal routing were adopted to minimize the effects of noise and crosstalk. Top layer was dedicated to the routing of the analog signals while digital signals were routed on the bottom layer. Analog and Digital ground planes were used to shield the traces on the top and bottom layers respectively and minimize therefore the crosstalk. Three power supplies were used to power up the system. Two supplies power up the digital system (core of 1.8 V and ring of 3.3 V), whereas the last one supplies power to the analog system. The analog system comprises both switched (integrators' switches and SC-CMFB) and non-switched (OTAs) components. Separation of these

supplies was achieved on-chip. This supply partitioning prevents switching noise from coupling onto the supply lines of the analog components. However, all analog components (switched and non-switched) were eventually powered up using a single analog power supply. This was done by connecting them all on-board. This ensures that no potential difference exists between the different analog supply nodes. A block-diagram description of the power supply separation on the IC core and PCB board levels is shown in Figure 5.1. While the description presented above refers to power, similar thinking was adopted for the ground pads.

Testing was initially achieved at half the intended sampling rate, corresponding therefore to half the input bandwidth (0.5 MHz, or 1 MS/s output rate). This was due to the maximum speed of 25 MHz at which sample collection could be performed using the mixed-signal tester. Testing at the full operating speed are shown later in a different test setup.

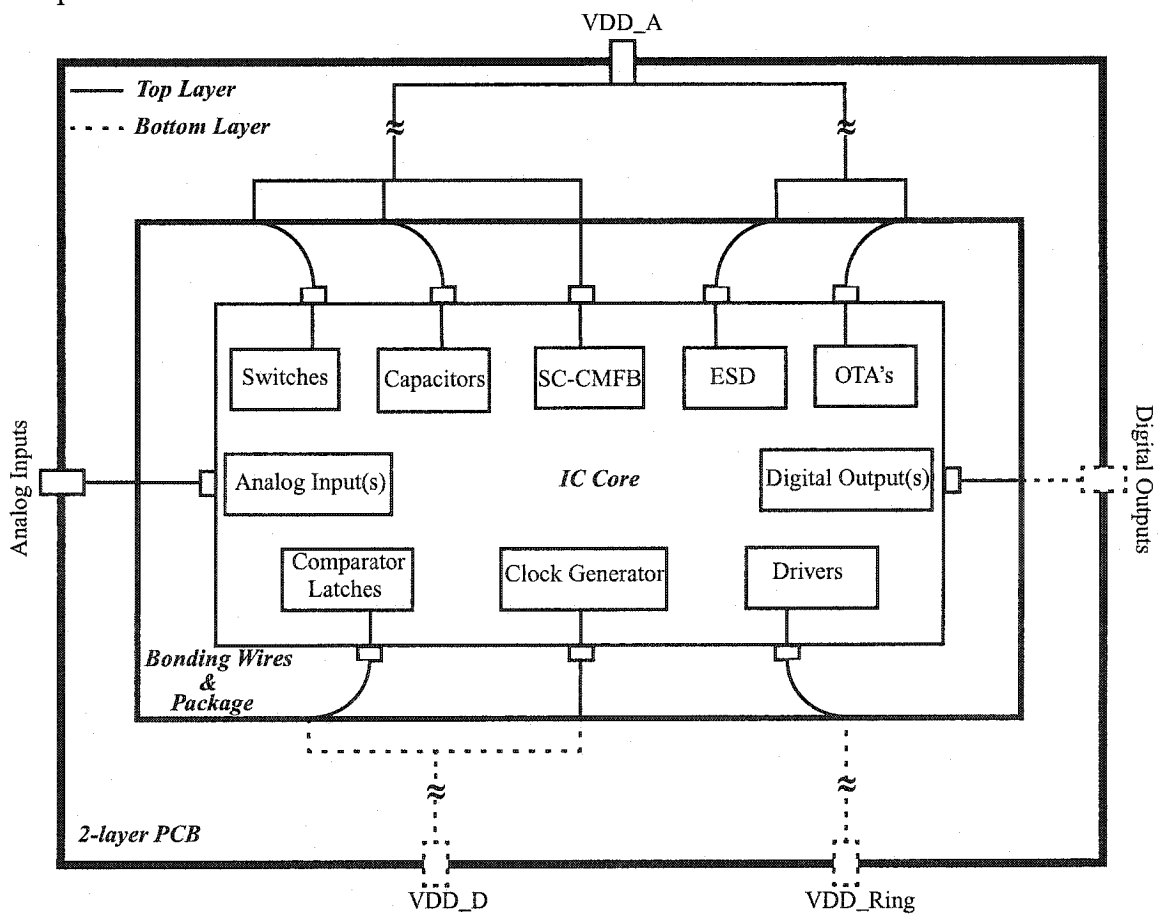


Figure 5.1 IC Core and Printed Circuit Board Power Distribution Floorplan

5.1.2 - Dynamic Range Measurements

In order to test the dynamic range of the modulator, an input sine wave, with varying input amplitude, was applied to the IC. The output *SNR* and *SNDR* were recorded for each input power.

To evaluate the performance of the modulator, 65536 points of the output bitstream were captured and stored straight off the PCB by the A567 mixed signal tester's digital capture memory. These points were then exported to Matlab, digital error cancellation performed, 2^{16}- point FFT taken, and results recorded. This was done for each test run.

A plot of the measured *SNR/SNDR* as a function of input power is shown in Figure 5.2. The reference level of the input used for computing the dB power is 1 V.

The effective dynamic range[1] of the modulator is 75 dB with a peak *SNR/SNDR* of 61/56 dB respectively.

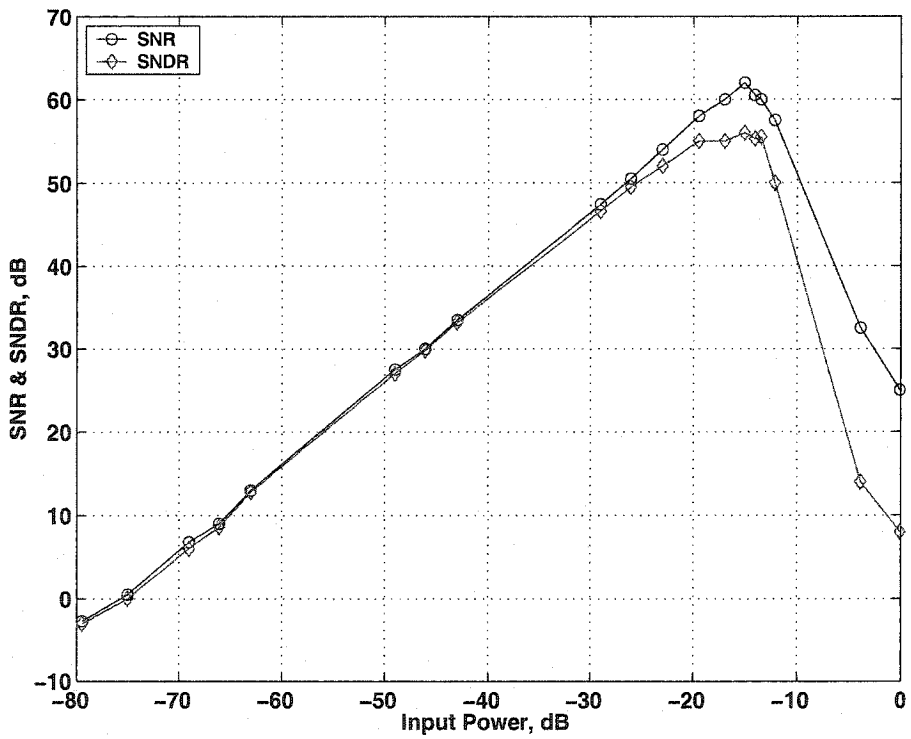


Figure 5.2 Dynamic Range of the IC at 25 MHz Sampling Rate.

1. Dynamic range is defined as the input range for which the output *SNR/SNDR* is greater than 0 dB and input power ≤ 0 dB.

5.1.3 - DAC Reference Voltage

The early saturation level at an input level of ~ -14 dB is due to the relatively low reference voltages. Even though this was designed for, reference voltages were increased gradually until the modulator stopped functioning. In fact, the reference voltages were increased to full scale, i.e. 0 V and 1.8 V, and the modulator was still functional. Better results in terms of preventing the early saturation were achieved, as expected. In fact, the noise power was also decreased to -77.5 dB. Two selected samples of the FFTs captured can be seen in Figure 5.3 and Figure 5.4. From both figures, the noise shaping action of the modulator can be seen, along with the thermal noise limitations at low frequencies.

These two sets in particular were chosen because the first (Figure 5.3) corresponds to a very small input amplitude where no distortion is observed whereas the second (Figure 5.4) corresponds to the amplitude where peak *SNR* occurs and where distortion is obvious. The new *DR* plot corresponding to testing the IC at full-scale DAC voltages and 25 MHz sampling frequency is shown in Figure 5.5. The new measured *DR* is now 77.5 dB with a peak *SNR*/*SNDR* of 70/57 dB respectively.

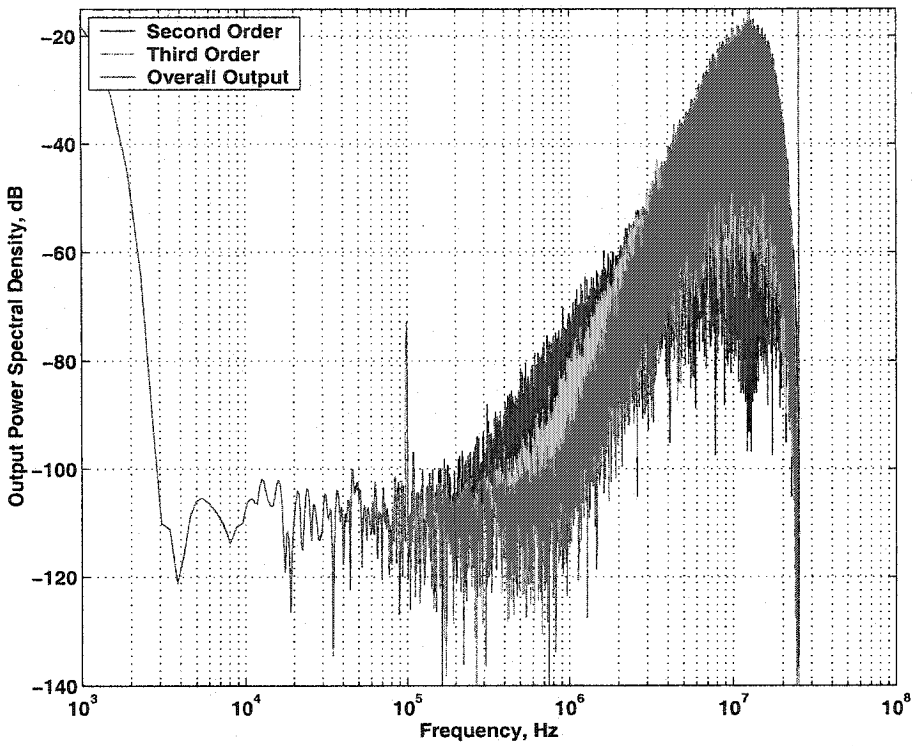


Figure 5.3 PSD of the Output for 1 mV_{peak} Input Sine Wave at 98.8 kHz Frequency, and Sampling Frequency of 25 MHz.

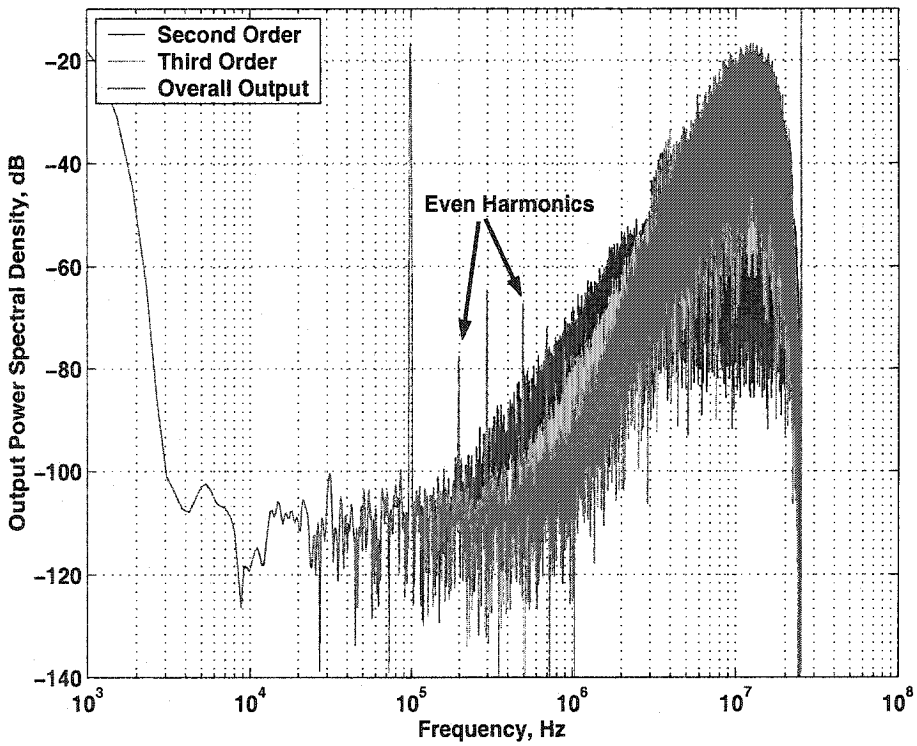


Figure 5.4 PSD of the Output for 0.675 V_{peak} Input Sine Wave at 98.8 kHz Frequency, and Sampling Frequency of 25 MHz.

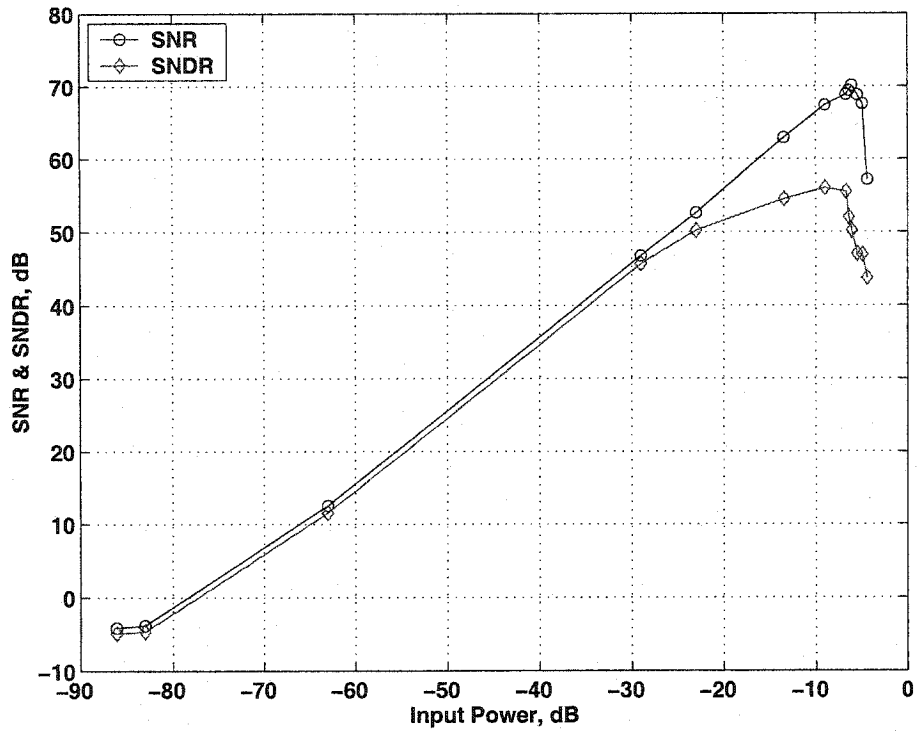


Figure 5.5 Dynamic Range of the IC at 25 MHz Sampling Rate and Larger Reference Voltages.

In order to decrease the harmonic distortion, a multi-layer board was designed and fabricated as explained next.

5.1.4 - Dynamic Range Improvement

Large even order harmonics present in the output spectrum, despite the fully differential structure suggested noise interference from the PCB. To improve the performance, it is essential to implement further shielding, grounding and decoupling of the device. As a result, a 4-layer fully-custom PCB, seen in Figure 5.6, was manufactured. Design rules used for the 2-layer PCB and outlined earlier were also used here. However, further device shielding and separation between analog and digital signal traces were made possible due to the two extra "quiet" layers that were available. While top and bottom layers were still used for routing digital and analog traces respectively, the two middle layers were dedicated split power/ground planes, carrying no signal traces.

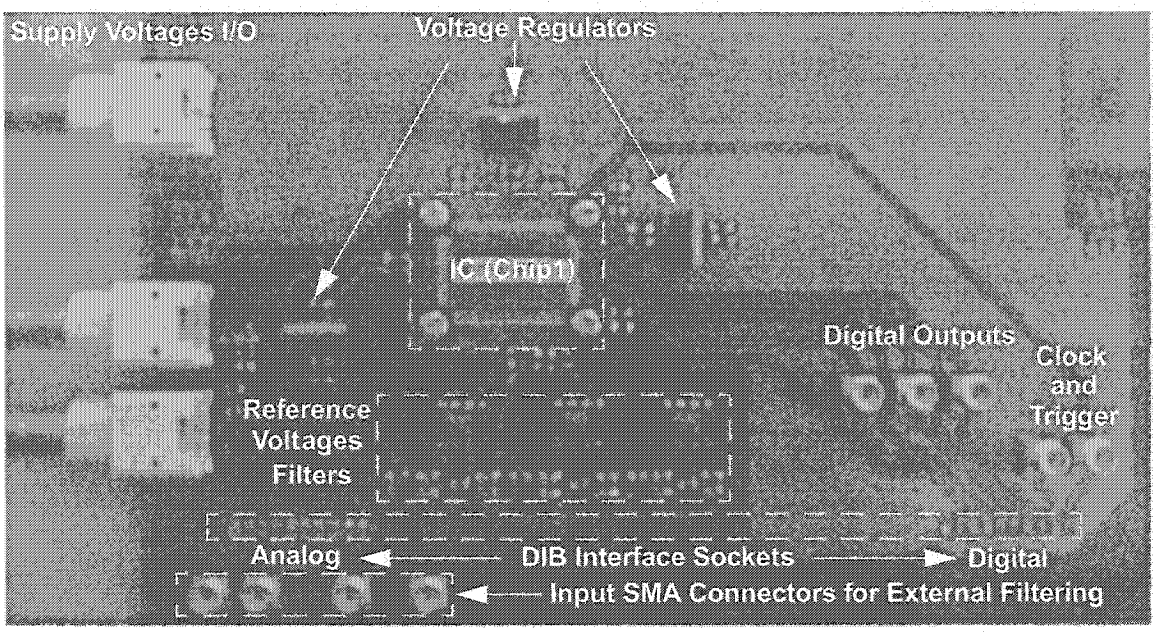


Figure 5.6 Four-Layer PCB for Chip 1.

Voltage regulation was also added. A 15 V supply was used to power up a series of regulators that provide the ICs supplies. Three regulators were used to regulate the three separate power supplies: two regulators power up the digital system (1.8 V core and 3.3 V ring), whereas the last one supplies 1.8 V to the analog system. Surface mount components were used whenever possible, decreasing therefore the capacitive, resistive and inductive parasitics of the leads.

In order to improve the resolution of the DC references and sinusoids output by the tester, some filtering was required [24]. The tester's DC sources, used as references for the modulator were cleaned up using the two-pole Butterworth filter seen in Figure 5.7.

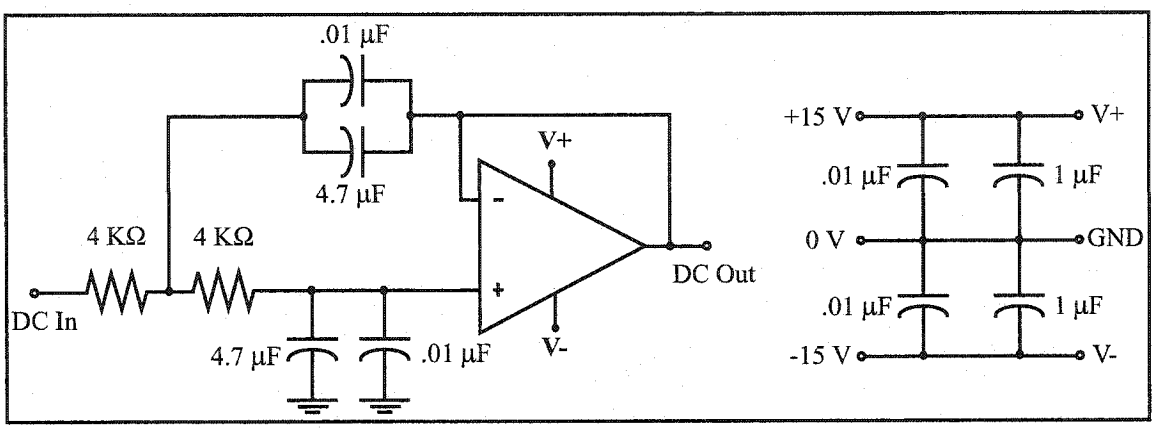


Figure 5.7 Filter for the DAC Voltage References.

The filter values were modified with respect to those outlined in [24] in order to fit the surface-mount capacitor values available.

The differential input signal was obtained from the tester's precision low frequency source. This input signal, once generated by the tester, was filtered using an external lowpass filter box with a programmable cutoff frequency.

As mentioned earlier, the tester clock and capture capability is limited to 25 MHz. The new PCB was configured to allow for testing at higher speed as explained next.

First, the low-speed input clock problem was overcome by using an external pulse generator. Synchronization of the external clock with the tester signal generator and digital capture was achieved using a dedicated tester digital pin to trigger the external clock. The test setup used can be seen in Figure 5.8.

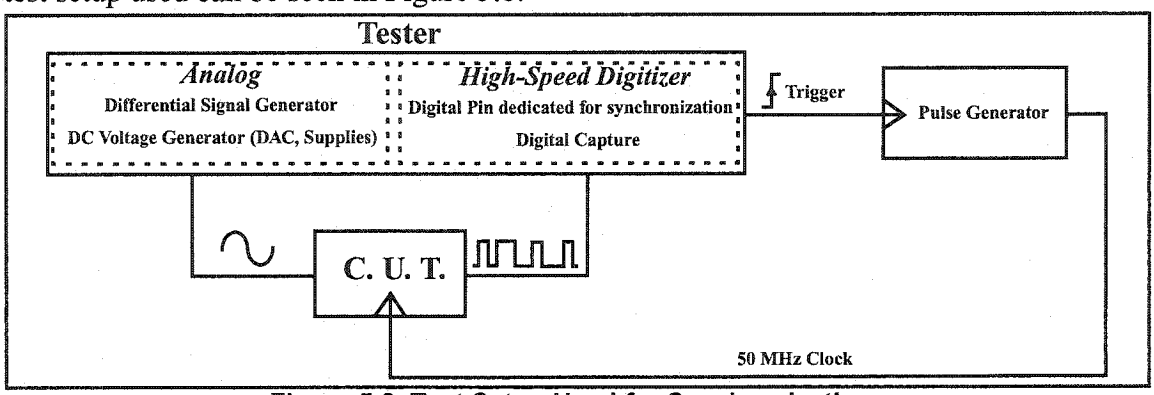


Figure 5.8 Test Setup Used for Synchronization.

Second, two attempts were made for capturing the digital output bits at 50 MHz rate. The capture even though limited to 25 MHz (i.e. a maximum of 1 bit can be captured every 40 ns), was thought achievable with either one of the two "multiplexing" methods described below:

- *Collecting the same digital output on two separate pins, at two different time instants (with time offset = 20 ns), or equivalently,*
- *Capturing the same digital output in two separate runs with a time offset of 20 ns.*

This is better described in Figure 5.9. As shown in the figure, both tester capture pin 1 and 2 are connected to the same IC digital output, but tester pin # 1 captures 1 bit every 40 ns starting at t = 5 ns, while tester pin # 2 captures 1 bit every 40 ns starting at t = 25 ns. The collected bits could then be multiplexed and the original IC output reconstructed at the high output rate of 1 bit every 20 ns, equivalent to an output data rate of 50 MHz.

Equivalently, only one digital pin (pin # 1) could be used with two separate runs. In the first run, every other bit is collected every 40 ns, starting at t = 5 ns. In the second run, the other bits are collected starting at t = 25 ns.

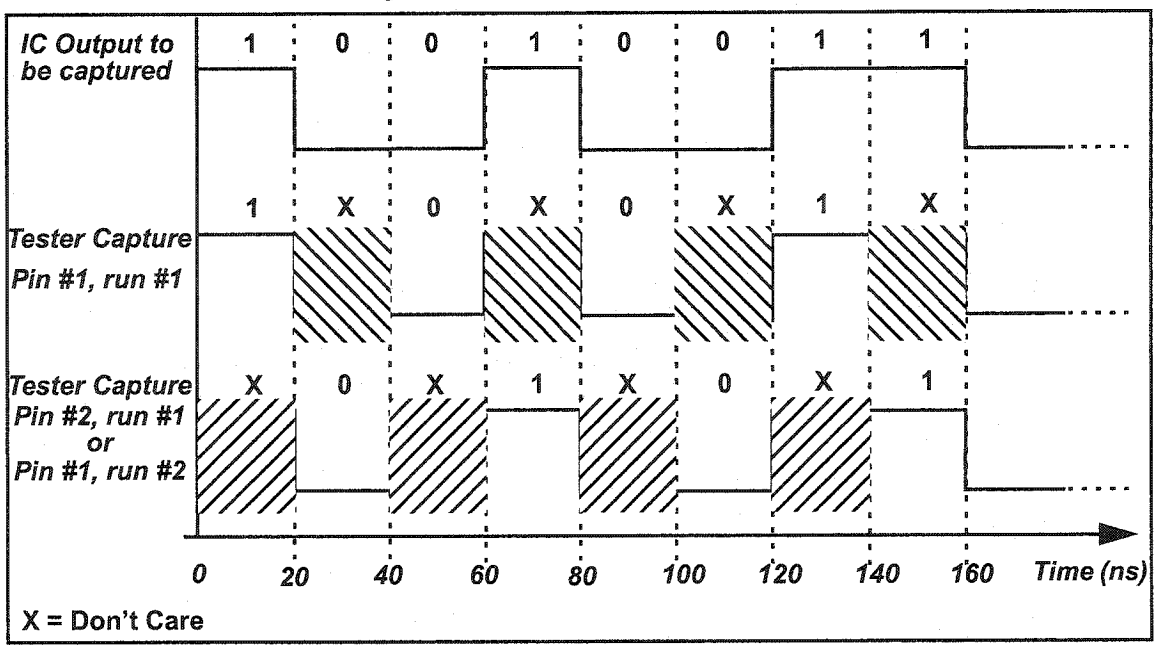


Figure 5.9 Test Setup Showing the Capture at 50 MHz Sampling Rate.

Neither attempt provided reliable results due to the hardware limitation of the tester being used. The rise/fall times of the digital waveforms at this rate when driving the tester's pins capacitive load made the results very susceptible to the collection time instant and interval. While occasionally some runs would give meaningful results (via tweaking and "guessing" the collection time down to the 500 ps interval), it was by no means reliable nor repeatable. Re-calibration of the tester's high-speed digitizer to re-align the capture edges to the new collection time offset was sometimes necessary. Phase errors that could be introduced by the tester after two different calibration runs made multiplexing the data collected from the two runs uncoordinated in terms of time.

A simultaneous observation of the output directly on a spectrum analyzer and a comparison with the data collected from the tester confirmed the non-reliability of the results.

Nonetheless, this test provided a high-level of confidence about the correct functionality (even though occasional) of the designed IC at the full speed of 50 MHz. More specifically, observations of the output on the spectrum analyzer further confirmed the constant noise floor for 1 MHz bandwidth for speeds up to 50 MHz.

Due to the relatively time consuming process of calibrating and multiplexing the data to reconstruct the overall output and results being non-reliable, another alternative was sought. The digital bistreams were captured via a logic analyzer synchronized with the external clock source, which in turn was synchronized with the tester's sine wave generator. Limitations in the logic analyzer memory constrained the depth of the data captured to 8192 points. As a result, a maximum of 8192 points were collected for further FFT analysis in Matlab. While not accurate, it was deemed enough to justify the correct functionality and estimate the noise floor, and as a result, the dynamic range of the modulator at 50 MHz.

Only one run corresponding to an amplitude of 0.6 V peak was tested. The results are shown in Figure 5.10. The new noise floor achieved at full speed is now -77.6 dB. The

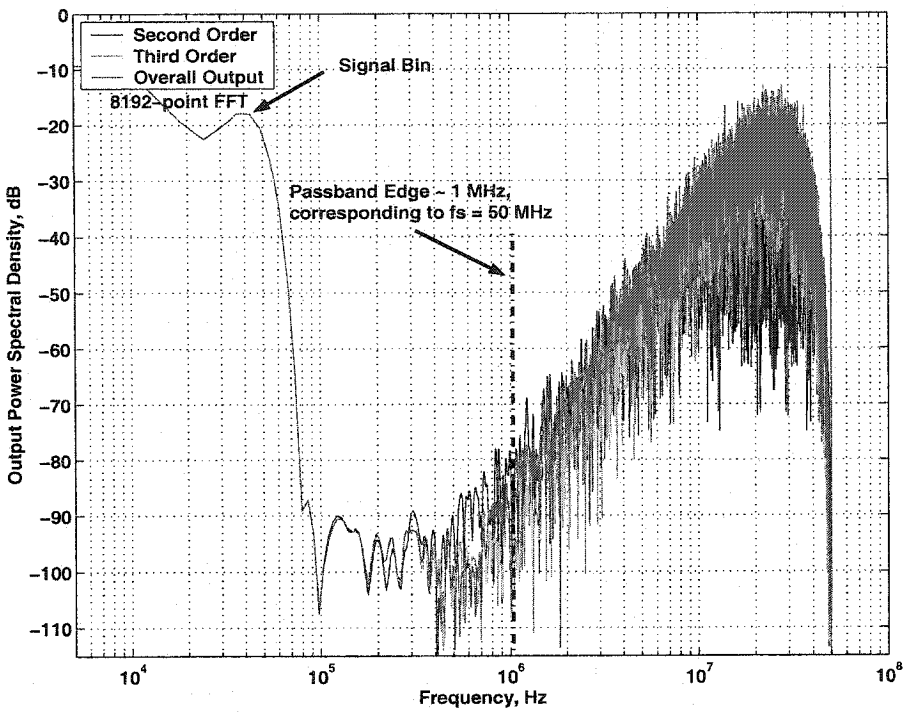


Figure 5.10 PSD of the Output at 0.6 V_{peak} Input Sine Wave at 48.828 kHz Frequency, and Sampling Frequency of 50 MHz.

measured noise floors are almost identical in the two cases where f_s = 25 MHz and f_s = 50MHz.

The additional voltage regulation, and input signal/reference voltage filtering that were added to the 4-layer PCB didn't seem to improve the performance. Only the extension in the DAC reference voltages to full scale helped decrease the noise floor from -75 dB to around -77.6 dB. With the new board however, the distortion was reduced, as anticipated. The effective dynamic range of the modulator is therefore 77.6 dB with a peak *SNR/SNDR* of 70/62 dB respectively.

A summary of the modulator's achieved performance is shown in Table 5.1.

Table 5.1 - Summary of Specifications for Chip 1.

Technology	0.18 μm CMOS
Total Area	3.4 mm x 3 mm
Supply	1.8 V
Power Dissipation	18.8 mW
Dynamic Range	77.6 dB
Peak *SNR*	70 dB
Peak *SNDR*	62 dB
Sampling Frequency	50 MHz
OSR	24
Output Nyquist Rate	~ 2 MS/s
Reference Voltages	1.8 V, 0 V
Input Range	1.5 V_{pp}

In summary, the 4-layer PCB helped improve the harmonic distortion by approximately 5 dB. Increasing the reference voltages to full scale, on the other hand, helped decrease the noise floor by ~ 3 dB providing therefore an extra half-bit of resolution. This improvement in noise floor was observed for both the two- and four-layer PCBs.

5.2 - Multi-Bit ΔΣ Modulator

5.2.1 - Test Setup

The test setup and care taken in the design of the PCB are identical to those discussed earlier for the single-bit modulator and won't be repeated. Only results will be shown with discussion when appropriate. Since this modulator is expected to achieve even better performance than the one previously discussed, a multi-layer PCB was directly designed. A photograph of the new four-layer PCB is shown in Figure 5.11.

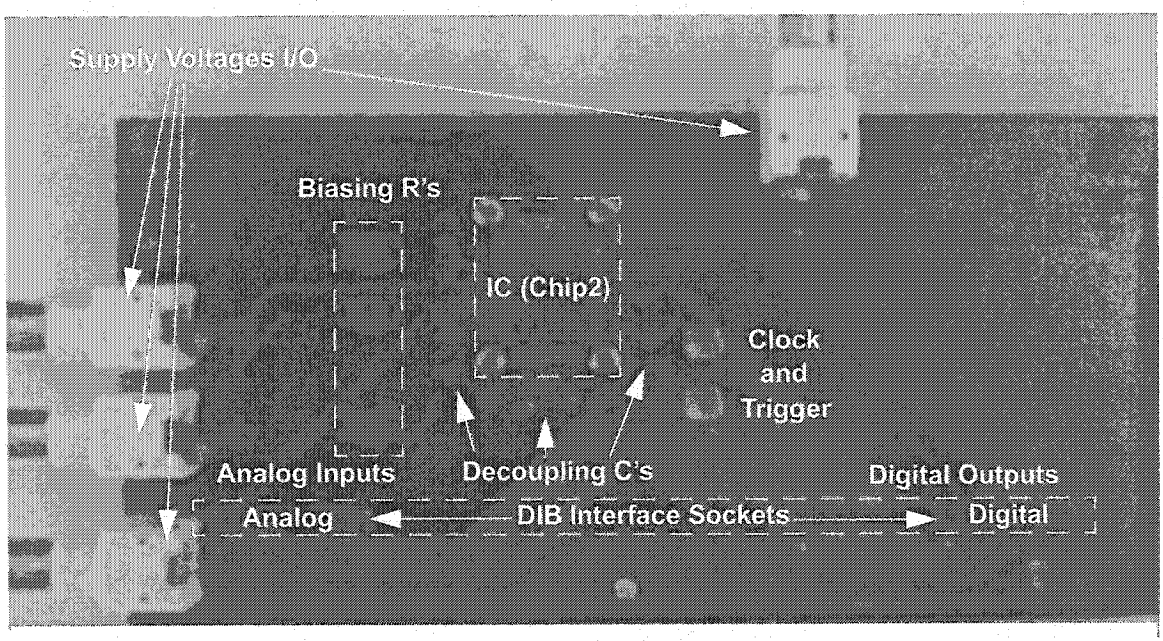


Figure 5.11 Four-Layer PCB for Chip 2.

5.2.2 - Dynamic Range Measurements

First, tests at half the speed were conducted with the mixed-signal tester to provide an accurate plot of the modulator's output spectrum with an output array of size 65536 (as opposed to the 8192 array-size provided by the spectrum analyzer). A plot of the output spectrum showing the noise shaping is shown in Figure 5.12, for an input sine wave of amplitude 0.6 V peak, frequency 98.8 kHz and differential reference voltage of 1.8 V. A plot of the *SNR/SNDR* of the multi-bit modulator as a function of input power is shown in Figure 5.12. The dynamic range is 81.3 dB.

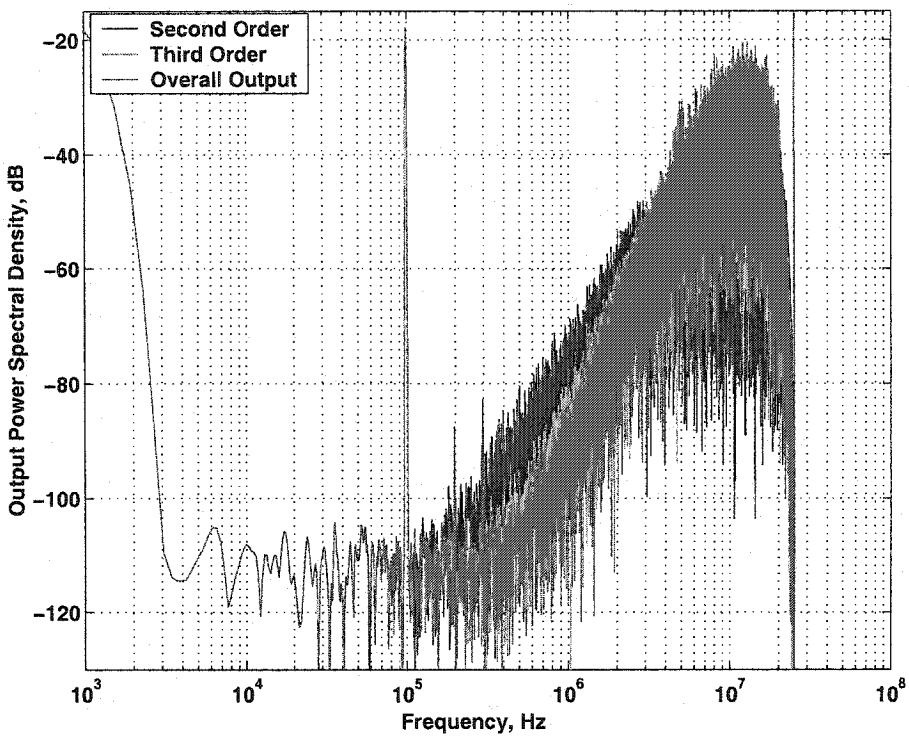


Figure 5.12 PSD of the Output at 0.6 V_{peak} Input Sine Wave at 98.8 kHz Frequency, and Sampling Frequency of 25 MHz.

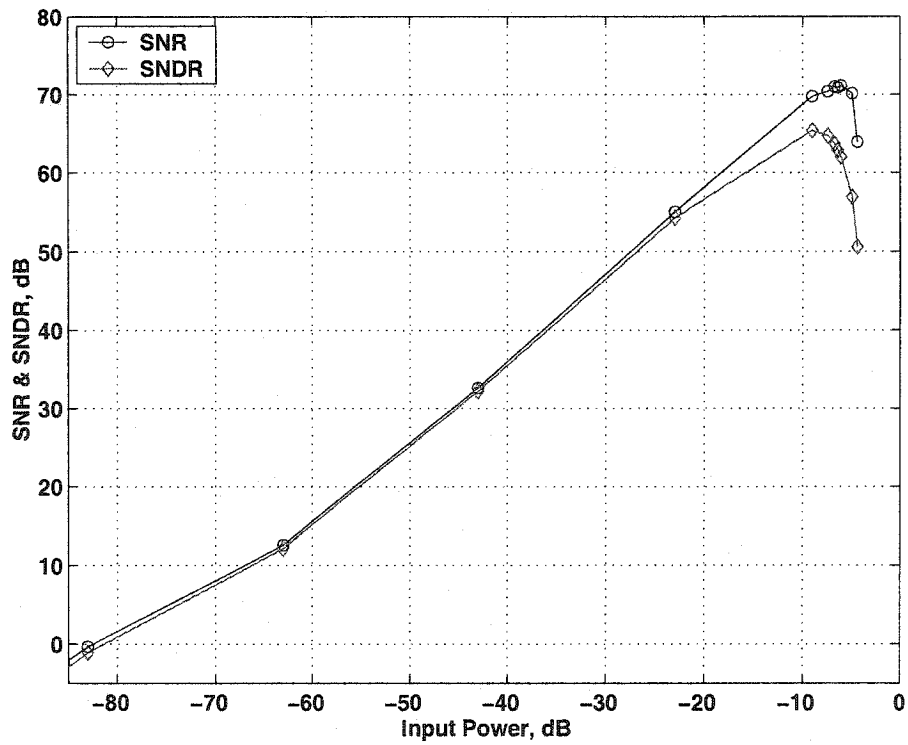


Figure 5.13 Dynamic Range of the IC at 25 MHz Sampling Rate.

Here too, only one sample run was conducted at the high sampling rate as discussed earlier. The run corresponds to an amplitude of 0.6 V peak at 48.828 KHz frequency. The results are almost identical to those collected when the modulator was tested at 25 MHz sampling frequency, with a noise floor of -81.38 dB, peak *SNR* of 72.7 dB and peak *SNDR* of 65.7 dB. The new FFT of the output spectrum is shown in Figure 5.14.

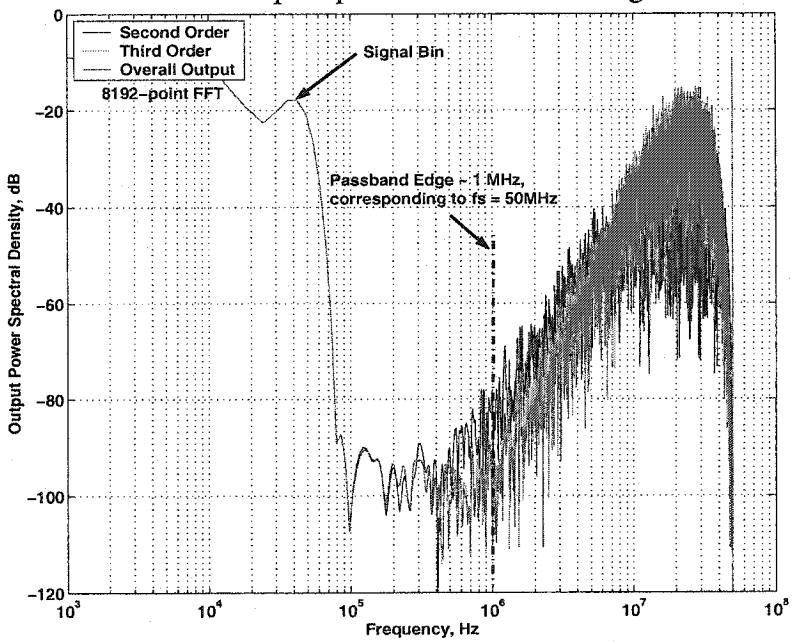


Figure 5.14 PSD of the Output at 0.6 V_{peak} Input Sine Wave at 48.828 kHz Frequency, and Sampling Frequency of 50 MHz.

A summary of the modulator achieved performance is shown in Table 5.2.

Table 5.2 - Summary of Specifications for Chip 2.

Technology	0.18 μm CMOS
Total Area	3.2 mm x 2.6 mm
Supply	1.8 V
Power Dissipation	36 mW
Dynamic Range	81.3 dB
Peak *SNR*	72.7 dB
Peak *SNDR*	65.7 dB
Sampling Frequency	50 MHz
OSR	24
Output Nyquist Rate	~ 2 MS/s
Reference Voltages	1.8V, 0.0 V
Input Range	1.5 V_{pp}

5.3 - Discussion of Results and Summary of Findings

In this chapter, the experimental results of both modulators were presented. The feasibility of building high resolution modulators for wideband applications at low supply voltages were demonstrated in a 0.18 μm CMOS process. Dynamic ranges in the order of 12-13.2 bits are possible and traditional architecture for ΔΣ M's are proven feasible solutions for implementing analog-to-digital converters for low-voltage, high-speed applications.

It is believed that this performance could have been further improved had supply decoupling capacitors been included on-chip. Adding very large decoupling capacitors (in the order of 1000 uF) on-board together with shrinking the ring supply voltage from 3.3 V to 2.1 V increased the dynamic range by approximately 6 dB. This suggests that digital noise propagating to the analog side and causing crosstalk is a possible source of increased noise floor.

The advantages of 2-layer versus 4-layer board design were also investigated. The 4-layer board helped improve the total harmonic distortion by about 5 dB but didn't help in reducing the noise floor. The biggest effect on reducing the noise floor came from extending the DAC reference voltages to full scale, which suggests limitations due to the test setup and mainly noise interference from the tester's voltage sources, rather than circuit design. The extra improvement in the noise floor was around 3 dB. At full scale reference voltages, and more specifically when V_{ref-} is shrunk from 0.5 V to 0 V, less noise gets generated from the test set-up since possibly the tester's voltage source generating V_{ref-} gets merged with the tester's ground when set to 0 V. On-board reference voltage filtering was incorporated specifically for the purpose of cleaning up the DAC reference voltages generated from the tester. Little improvement was achieved, possibly due to the additional noise generated by the filter itself such as the resistors and op. amp. used to implement the two-pole Butterworth filter. Extending the reference voltages to full scale also helped extend the linear region of the modulator and minimized the early overload/saturation input level. Higher peak *SNR*s resulted.

Also, the advantage of the multi-bit quantization wasn't explored to its fullest since noise interference from different sources limited the noise floor to around -81 dB, making the dynamic range of Chip 2 only 3 dB better than the performance of Chip 1. The extra 1.5-2 bits of resolution expected from the addition of the multi-bit quantization in the last stage was therefore masked by the relatively higher than anticipated noise floor. It could only be hypothesized at this point that the extra noise is due to external test setup, as well as the lack of on-chip decoupling capacitors.

All the previously reported results corresponding to the different test setups are summarized in Table 5.3.

Table 5.3 - Summary of Experimental Results for Different Test Setups.

	Peak *SNR*	Peak *SNDR*	*DR*/Noise Floor
Chip 1 • ***2-layer PCB*** • ***Small Vref***	61	56	75
Chip 1 • ***2-layer PCB*** • ***Large Vref***	70	57	77.5
Chip 1 • ***4-layer PCB*** • ***Large Vref***	70	62	77.6
Chip 2 • ***4-layer PCB*** • ***Large Vref***	72.7	65.7	81.3

Chapter 6 - Conclusions

In the preceding chapters, a fast synthesis method was used to design the circuit specifications of the modulator. This method proved both computationally and time efficient to design modulators, and more generally, any system that requires long simulation times.

The system-level deduced specifications were then mapped into the circuit implementation of two state-of-the-art modulators. In a single 1.8 V supply, 0.18 μm CMOS process, a single-bit as well as a multi-bit modulators were implemented. The issues behind the design of low-voltage, switched-capacitor CMOS ΔΣM were discussed. Design and layout steps followed to the IC implementations were then discussed.

The experimental results of both implemented circuits were then presented. The former achieves 77.5 dB dynamic range at a sampling rate of 50 MHz while the latter extends the dynamic range to 81.3 dB at the same sampling rate. The performance achieved was further used to justify the correct functionality of the proposed design method. Whenever discrepancies existed, attempts were made to justify them.

With the dynamic ranges achieved, a new plot including the experimental results of the two designed ICs and where they stand in the list of some published ΔΣ ADCs is shown. The comparison is done based on the same modulators introduced in the Chapter 1 of this thesis, and using the same figure of merit. Figure 6.1 presents the results as a function of

the output rate while Figure 6.2 presents the same information as a function of supply voltage.

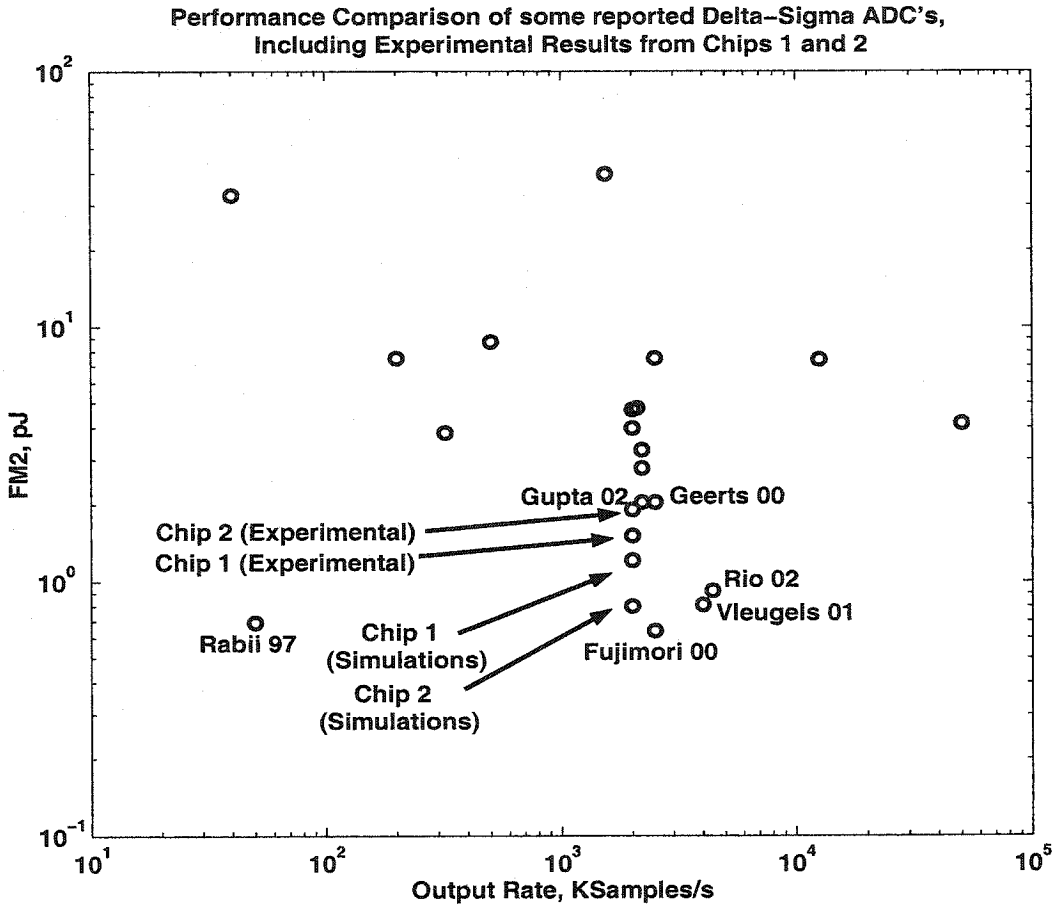


Figure 6.1 Performance Comparison of Different Modulators as a Function of Output Rate.

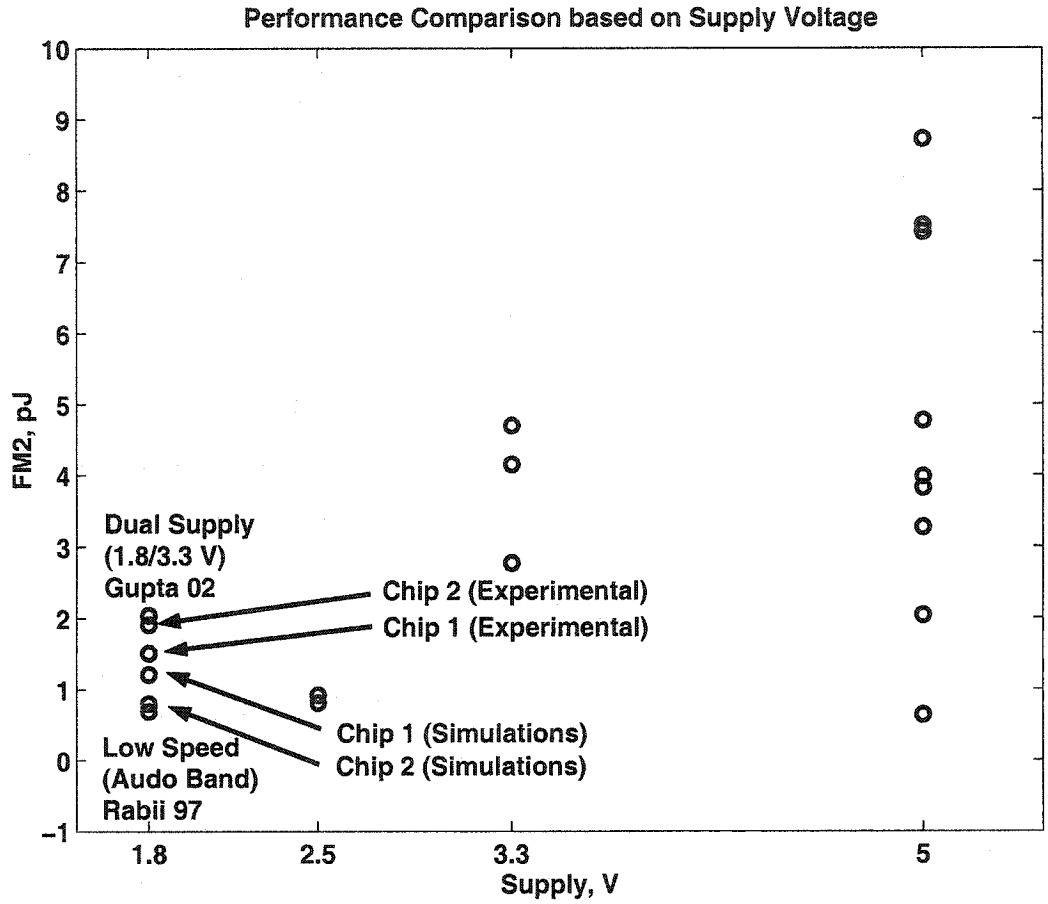


Figure 6.2 Performance Comparison of Different Modulators as a Function of Supply Voltage.

While the experimental results of both chips are below the target specifications, the performances achieved still place them within the best modulators reported to date.

In summary, it is safe to claim that the use of high resolution delta-sigma modulators is no longer restricted to low- to medium-speed applications. Its applications extend to include broad band applications, even in deep submicron technologies. The work presented in this thesis demonstrated extending the bandwidth range to include ADSL applications, using a single supply voltage of 1.8 V. Further improvement includes extending this bandwidth to video rate.

Appendix A - OTA Derivations

The effects of using gain boosting technique and complementary differential pairs on the OTA performance are outlined in this Appendix. The analysis will start with the low-frequency response (DC gain) and will conclude with the effect of parasitic capacitances on the high-frequency behavior (transient response).

A.1 - Low-Frequency Behavior

A.1.1 - Gain Boosting

First, the low-frequency analysis is carried out to see how the DC gain is affected. Figure A.1 shows a simplified model of the N- and P- gain boosting stages, added to the regular output stage of an op. amp. formed by transistor M_1 (M_6 and M_7 in the case of the P-gain boosting stage). Both gain-boosting stages are highlighted in the figure, and formed by transistor M_3 (M_4) and the ideal current source I_B. The equivalent small-signal models for the circuits in Figure A.1 are shown in Figure A.2 and Figure A.3. For now, the analysis ignores parasitic capacitances and computes the output impedance from a purely resistive point of view. This is useful for analyzing the effect of including the gain-boosting stage on the DC gain.

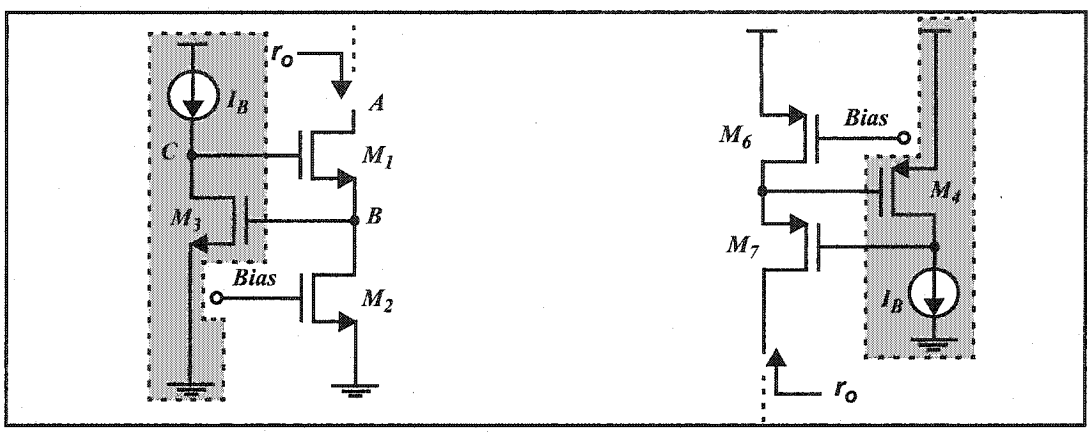


Figure A.1 NMOS and PMOS Gain Boosting Stage.

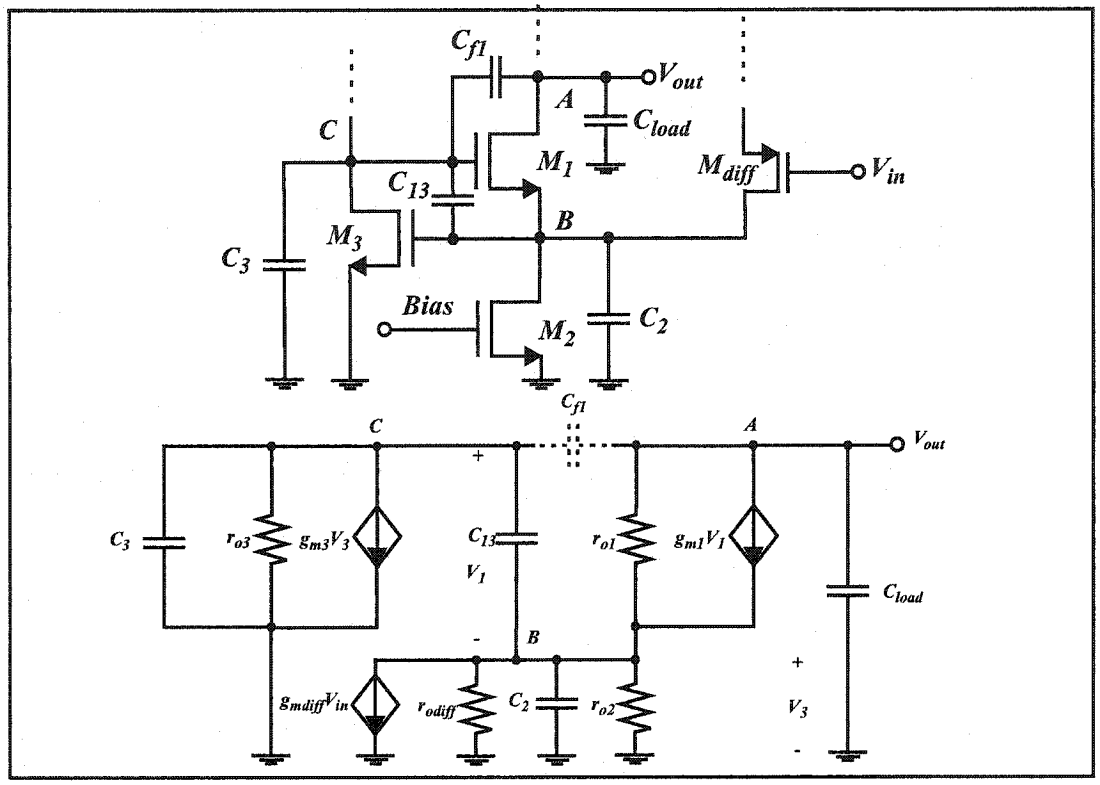


Figure A.2 Small-Signal Model of the N-Gain Boosting Stage.

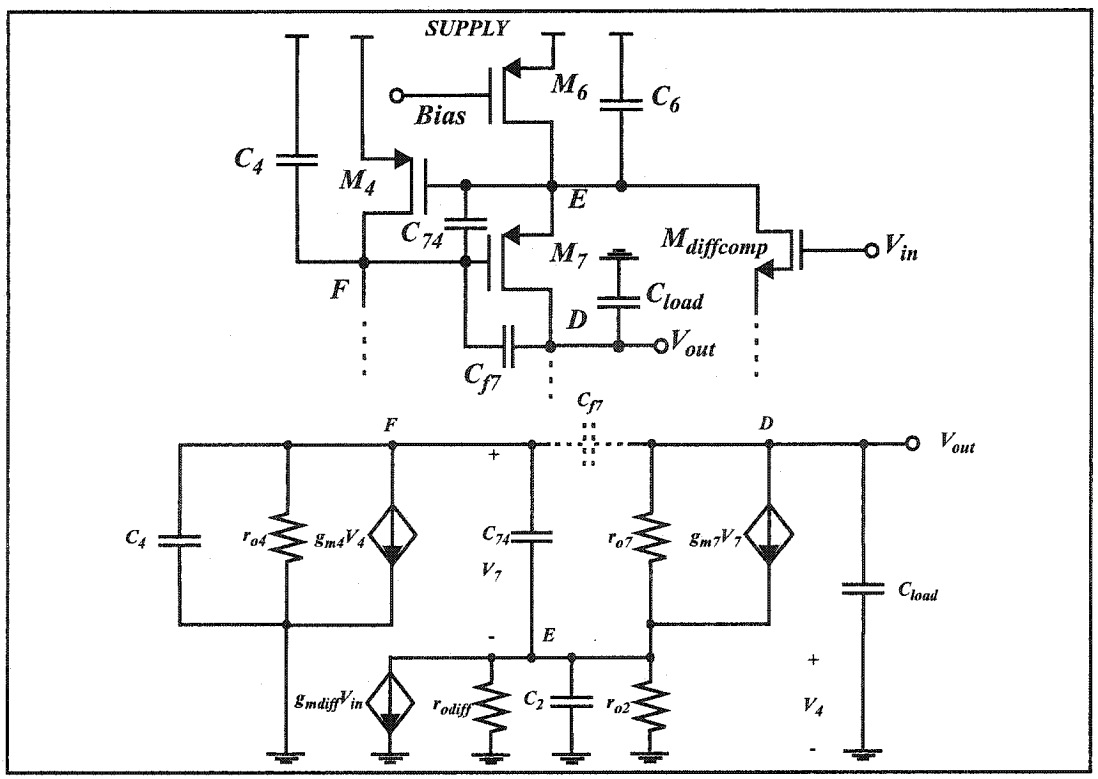


Figure A.3 Small-Signal Model of the P-Gain Boosting Stage.

By definition, the output impedance is given by:

$$r_o = \frac{v_x}{i_x}, \tag{A.1}$$

where i_x and v_x are test voltage and current sources applied at the node where the output impedance is to be computed, v_{out} in this case.

Referring to Figure A.2, Kirchoff's current law (KCL) at nodes A and B gives the following relationships between i_x, v_1, and v_3:

$$i_x = g_{m1} \cdot v_1 + \frac{v_x - v_3}{r_{o1}}, \tag{A.2}$$

and

$$i_x = \frac{v_3}{r_{o2} \parallel r_{odiff}} \Rightarrow v_3 = i_x \cdot (r_{o2} \parallel r_{odiff}), \tag{A.3}$$

where the voltage across r_{o1} is given, using Kirchoff's voltage law (KVL), by $v_x - v_3$.

Writing KCL at node C and re-arranging, we get:

$$v_3 = -\frac{v_1}{g_{m3} \cdot r_{o3} + 1}. \tag{A.4}$$

Combining Eqn. () and Eqn. (A.4), we find:

$$v_1 = -i_x \cdot (r_{o2} \parallel r_{odiff}) \cdot (g_{m3} \cdot r_{o3} + 1). \tag{A.5}$$

Using Eqn. (A.2) and replacing v_1 and v_3 by their equivalent in terms of i_x from Eqn. (A.4) and Eqn. (A.5), we get:

$$\frac{v_x}{i_x} = r_{o1} + (r_{o2} \parallel r_{odiff}) + g_{m1} \cdot r_{o1} \cdot (r_{o2} \parallel r_{odiff}) \cdot (g_{m3} \cdot r_{o3} + 1), \tag{A.6}$$

which represents an expression for the output impedance using the definition in Eqn. (A.1).

Eqn. (A.6) could be simplified by ignoring relatively small terms to get:

$$r_o \cong (g_{m1} \cdot g_{m3} \cdot r_{o1} \cdot r_{o2} \cdot r_{o3}) = (g_{m3} \cdot r_{o3}) \cdot (g_{m1} \cdot r_{o1} \cdot r_{o2}), \quad \text{(A.7)}$$

which we will define as $r_{o,n}$, representing the output impedance of the N-gain boosting stage.

Using similar derivation, we get:

$$r_{o,p} \cong (g_{m7} \cdot g_{m4} \cdot r_{o7} \cdot r_{o6} \cdot r_{o4}) = (g_{m4} \cdot r_{o4}) \cdot (g_{m7} \cdot r_{o7} \cdot r_{o6}) \quad \text{(A.8)}$$

for the output impedance of the P-gain boosting stage.

For the overall OTA, the overall output impedance, r_o, is the parallel combination of both resistances given in Eqn. (A.7) and Eqn. (A.8). In other words, $r_o = r_{o,n} \| r_{o,p} = \frac{r_{o,n} \cdot r_{o,p}}{r_{o,n} + r_{o,p}}$.

From Eqn. (A.7) or Eqn. (A.8), we can readily see the advantage that gain boosting offers in terms of increasing the output impedance. An increase of the order of magnitude $g_m \cdot r_o$ can be obtained.

Trade-offs exist in sizing and current biasing of transistor M_3 if increase in the OTA overall DC gain is desired without degradation in the frequency performance. Namely, increasing the size of transistor M_3 increases g_{m3} and therefore the output impedance r_o, which in turn increases the DC gain. This however alters the pole-zero locations of the amplifier which could degrade the high frequency characteristics of the OTA as will be explained in a subsequent section.

A.1.2 - Complementary Differential Pair

The addition of the complementary differential pair at the input of the OTA has the advantages of increasing the bandwidth and providing a faster step response [31], [32]. This is the result of increasing the effective transconductance, $g_{meffective}$, which becomes the sum of both transconductances, g_{mdiff} and $g_{mdiffcomp}$.

As a result, the DC gain and bandwidth are increased by a factor equal to $\frac{g_{mdiffcomp} + g_{mdiff}}{g_{mdiff}}$.

The above analysis assumed low frequencies and didn't include the effect of capacitances at the various nodes. An analysis including the high-frequency behavior is described next.

A.2 - High-Frequency Behavior

A.2.1 - Gain Boosting

In [40] and [41], the derivation is done for gain-boosted telescopic amplifiers, but the analysis holds in the case of folded cascode OTA with few changes.

Referring to Figure A.2, each capacitor is defined as follows:

$$C_{13} = C_{gs1} + C_{dg3}, \tag{A.9}$$

$$C_2 = C_{db,diff} + C_{sb1} + C_{gs3} + C_{db2} \cong C_{db,diff} + C_{sb1} + C_{gs3}, \text{ and} \tag{A.10}$$

$$C_3 = C_{gb1} + C_{db3} \cong C_{db3}. \tag{A.11}$$

To simplify the analysis, C_{fl} is ignored without having much effect on the final results [12].

First-order analysis on the N-gain boosting stage only reveals, after some simplifications, three poles and one zero at the following *non-optimized* locations (assuming no complex conjugate poles exist):

1. One pole (dominant pole) due to the 3-dB of the overall amplifier $w_{3-dB} = \frac{g_{dsout}}{C_{Load}}$, where g_{dsout} is the inverse of the output impedance of the overall OTA and was defined earlier in Eqn. (),
2. A non-dominant pole at node B due to the parasitics, given by $w_{p,n} = \frac{g_{m1}}{C_{13} + C_2}$,
3. A third pole due to the 3-dB of the gain boosting stage $w_{boost,n} = \frac{g_{ds3}}{C_{13} + C_3}$, and
4. A zero due to the feedforward path of the added gain boosting stage $w_{zero,n} = \frac{g_{m3}}{C_3}$.

By using the analysis above and extending it to the P-gain boosting stage by simply changing the subscripts, we find two more poles and one zero at $w_{p,\mathrm{p}} = \frac{g_{m7}}{C_{74}+C_6}$, $w_{pole,\mathrm{p}} = \frac{g_{ds4}}{C_{74}+C_4}$, and $w_{zero,\mathrm{p}} = \frac{g_{m4}}{C_4}$ respectively, where each capacitor is defined as follows in Figure A.3:

$$C_{74} = C_{gs7} + C_{dg4}, \tag{A.12}$$

$$C_6 = C_{db,diffcomp} + C_{sb7} + C_{gs4} + C_{db6} \cong C_{db,diffcomp} + C_{sb7} + C_{gs4}, \text{ and} \tag{A.13}$$

$$C_4 = C_{gb7} + C_{db4} \cong C_{db4}. \tag{A.14}$$

In the case where complex conjugate poles exist, using the derivation detailed in [41], and applying the same concepts to include the P-gain boosting stage, we get:

$$\frac{v_{out}}{v_{in}}(s) = \frac{g_{mdiff} + g_{mdiffcomp}}{r_{out}} \cdot \frac{N_n}{D_n} \cdot \frac{N_p}{D_p}, \tag{A.15}$$

where:

$$N_n = s(g_{ds1}C_{13} - g_{ds1}C_3 + g_{m1}C_3) - (g_{ds1}g_{ds3} + g_{m1}g_{m3} - g_{m3}g_{ds1}),$$

$$\begin{aligned} D_n = {} & s^2\left(C_2C_3 + C_{13}C_3 - C_2C_{13}\right) + \\ & s\left(g_{m1}C_3 - 2g_{m3}C_{13} + g_{ds3}C_2 + g_{m3}C_3 + g_{ds1}C_3 + g_{m1}C_{13}\right) + \\ & \left(g_{m1}g_{ds3} - 2g_{m1}g_{m3} + g_{m3}g_{ds3} + g_{ds1}g_{ds3}\right) \end{aligned},$$

$$N_p = s(g_{ds7}C_{74} - g_{ds7}C_4 + g_{m7}C_4) - (g_{ds7}g_{ds4} + g_{m7}g_{m4} - g_{m4}g_{ds7}), \text{ and}$$

$$\begin{aligned} D_p = {} & s^2\left(C_6C_4 + C_{74}C_4 - C_6C_{74}\right) + \\ & s\left(g_{m7}C_4 - 2g_{m4}C_{74} + g_{ds4}C_6 + g_{m4}C_4 + g_{ds7}C_4 + g_{m7}C_{74}\right) + \\ & \left(g_{m7}g_{ds4} - 2g_{m7}g_{m4} + g_{m4}g_{ds4} + g_{ds7}g_{ds4}\right) \end{aligned}.$$

Depending on the sign of the expression $b^2 - 4ac$, where a, b, and c correspond to the coefficients of s^2, s and constant of D_n and D_p, we either have real or complex conjugate poles. Optimum results corresponds to complex conjugate rather than real poles

as will become clear when Matlab pole-zero maps, AC and transient simulation results of the overall OTA are presented.

A.2.2 - Complementary Differential Pair

The addition of the complementary differential pair has the following three effects [32]:

1. Adding a zero at the location:

$$w_{zero\ \text{complementary}} = \frac{g_{m1} \cdot (g_{mdiffcomp} + g_{mdiff})}{(C_2 + C_{13}) \cdot \left[g_{mdiffcomp} + g_{mdiff} \cdot \frac{g_{m1}}{g_{m7}} \cdot \frac{(C_{74} + C_6 + C_{dbcomp})}{(C_2 + C_{13})} \right]},$$

and

2. Modifying the non-dominant pole at node E to include the drain-bulk parasitic capacitance of the complementary differential pair. In other words, $w_{p,\text{p}} = \frac{g_{m7}}{C_{74} + C_6}$ becomes $w_{p,\text{p}} = \frac{g_{m7}}{C_{74} + C_6 + C_{dbcomp}}$.

A.3 - Overall OTA Response

Given the above analysis, the sizing of the gain boosting stage is crucial in the design of the OTA. The effect of sizing both gain boosting stages (for given currents in the different branches of the OTA and given saturation voltages) was simulated in Matlab with both transient (Figure A.4) and AC (Figure A.5) analysis performed.

Corresponding pole-zero maps were also plotted to observe the locations of the poles and zeros and are shown in Figure A.6. As the current in the gain-boosting stage decreases, the complex conjugate pairs start to get closer to the real axis (Figure A.6 (a) - Figure A.6 (c)), until eventually the two complex conjugate poles become real (Figure A.6 (d)). Placement of the poles and zeros on the real-axis is responsible for a reduced phase margin and ringing in the step response and therefore frequency response degradation of the OTA as is shown in Figure A.4 and Figure A.5.

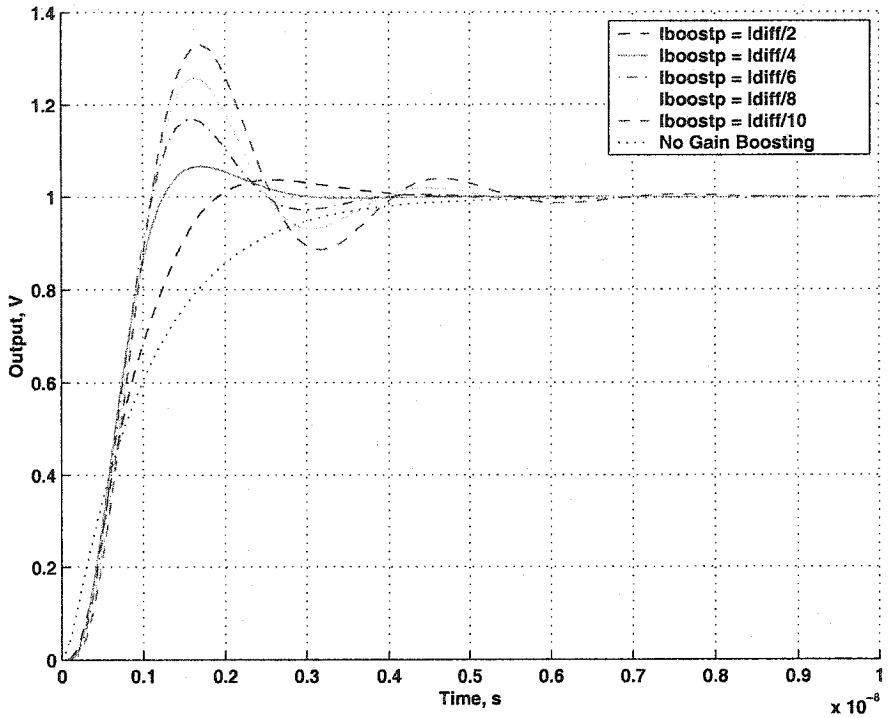


Figure A.4 Step Response of the OTA as a Function of the Gain Boosting Current.

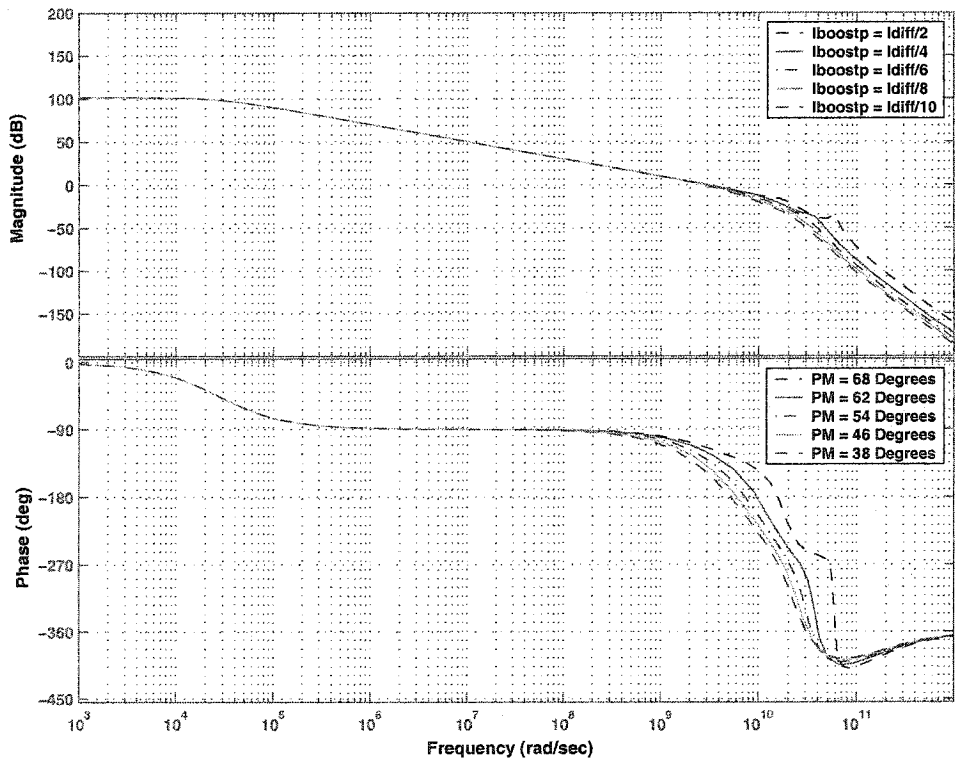
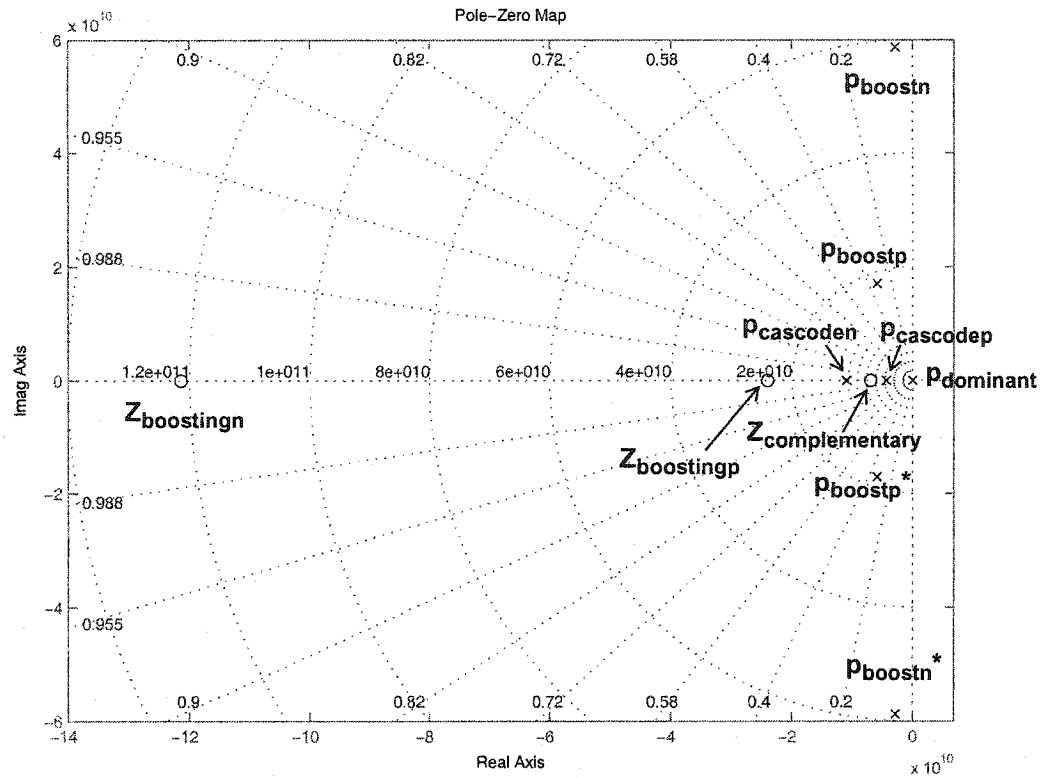
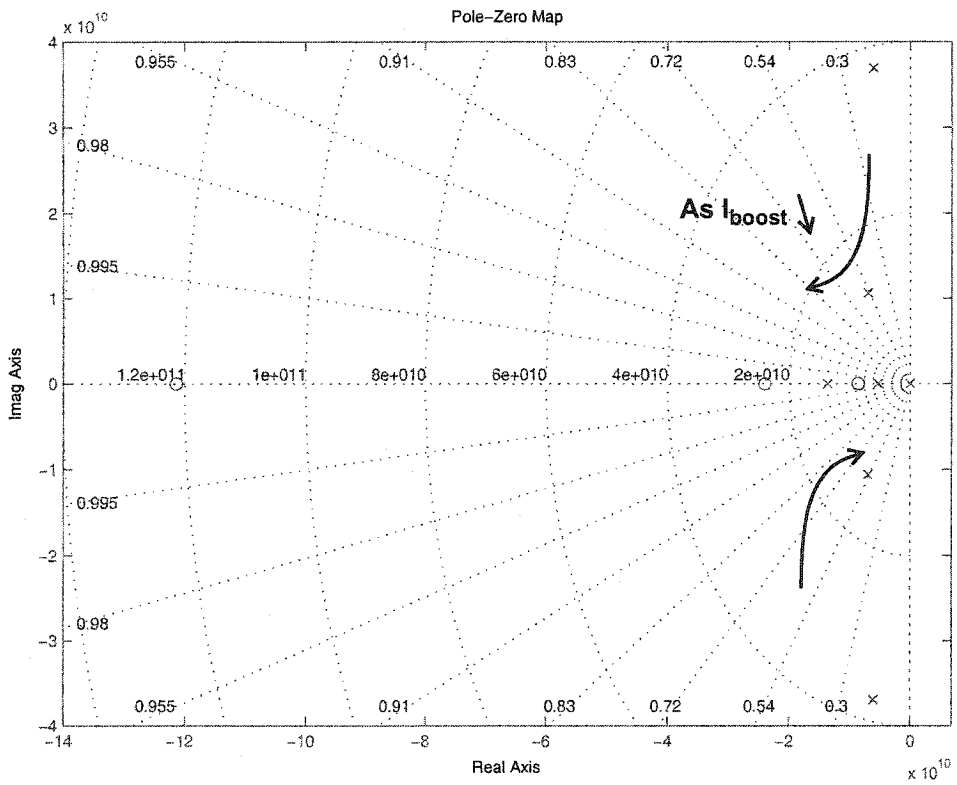


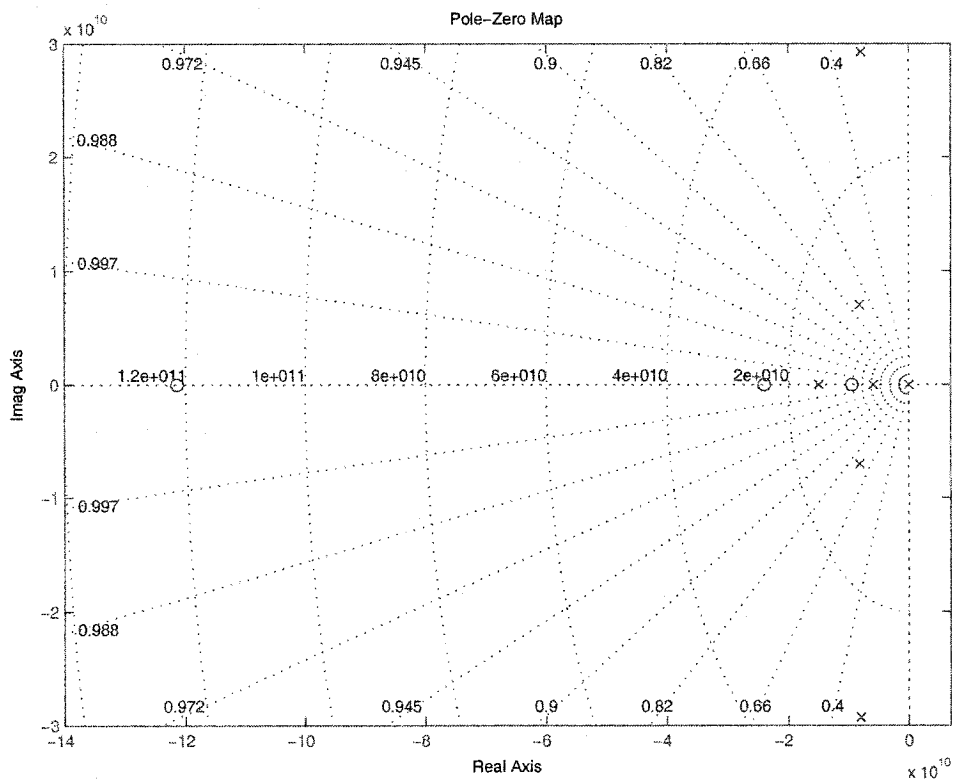
Figure A.5 AC Response of the OTA as a function of the Gain Boosting Current.



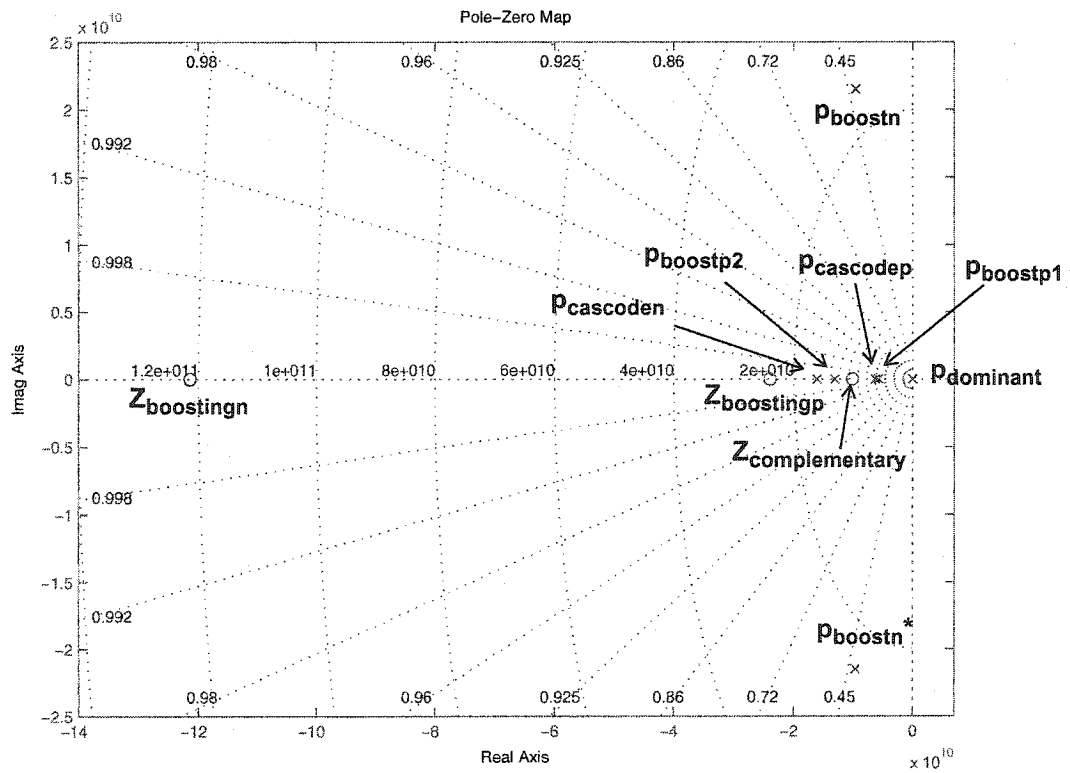
(a) Iboostp = Idiff/2



(b) Iboostp = Idiff/4



(c) Iboostp = Idiff/6



(d) Iboostp = Idiff/10

Figure A.6 Pole-Zero Map of the OTA for Different Gain Boosting Currents.

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