High-Speed Burst-Mode Clock and Data Recovery Circuits for Multiaccess Networks

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Subrahmanyan Chandrasekhar during his Nobel Prize lecture on December 8, 1983, was explaining the simplicity in the underlying physics and the beauty of mathematical description. He concluded his talk with the following words:

The simple is the seal of the true.

And beauty is the splendor of truth.

I begin my quest for knowledge and wisdom—truth in its purest—bearing the same words in mind, and the following poem in heart:

Where the mind is without fear and the head is held high;
Where knowledge is free;
Where words come out from the depth of truth;
Where tireless striving stretches its arms towards perfection;
Where the clear stream of reason has not lost its way into the dreary desert sand of dead habit;
into that haven of freedom, Let me awake.

—*Rabindranath Tagore*

To Ishana, my love

and

To Vibhuti, my Maa

About the Author

Bhavin J. Shastri received the Honours B.Eng. (with distinction) and M.Eng. degrees in electrical engineering in 2005 and 2007, respectively, from McGill University, Montreal, QC, Canada, where he is working toward the Ph.D. degree in electrical engineering at the Photonic Systems Group under the supervision of Prof. David V. Plant. He will start as Postdoctoral Research Fellow at the Lightwave Communication Research Laboratory, Princeton University under the guidance of Prof. Paul R. Prucnal.

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Mr. Shastri is a Student Member of the IEEE[1] Photonics Society, OSA[2], and SPIE[3]. He was the President and Co-Founder of the McGill OSA Student Chapter. He is the recipient of a prestigious IEEE Photonics Society 2011 Graduate Student Fellowship. He is the winner of a 2011 NSERC[4] Postdoctoral Fellowship. He was also awarded a 2011 SPIE Scholarship in Optics and Photonics. He is a Lorne Trottier Engineering Graduate Fellow and a winner of a prestigious Alexander Graham Bell Canada Graduate Scholarship from NSERC. He was the recipient of the Best Student Paper Award (2nd place) at the 2010 IEEE International Midwest Symposium on Circuits and Systems, the co-recipient of the Silver Leaf Certificate for the Best Student Paper at the 2008 IEEE Microsystems and Nanoelectronics Research Conference, and the recipient of the 2007 IEEE Photonics Society Travel Grant. In addition, he was the winner of the 2004 IEEE Computer Society Lance Stafford Larson Outstanding Student Award, and the 2003 IEEE Canada Life Member Award for the Best Student Paper.

[1]Institute of Electrical and Electronic Engineers
[2]Optical Society of America
[3]The International Society for Optics and Photonics
[4]National Sciences and Engineering Research Council of Canada

Abstract

Optical multiaccess networks, and more specifically passive optical networks (PONs) are considered to be one of the most promising technologies for the deployment of fiber-to-the-premises/cabinet/building/home/user (FTTx) to solve the problem of limited bandwidth in local area networks (LANs). PONs achieve this with a low-cost solution and with a guaranteed quality of service (QoS). In a PON, multiple users share the fiber infrastructure in a point-to-multipoint (P2MP) network topology. This is in contrast to current access technologies, including asymmetric or very high speed digital subscriber link (xDSL) and cable, which use a point-to-point (P2P) network topology. The nature of P2MP networks introduces optical path delays which inherently cause the data packets to undergo amplitude variations up to 20 dB and phase variations from -2π to $+2\pi$ rad—burst-mode traffic. Consequently, this creates new challenges for the design and testing of optical receivers front-ends and clock and data recovery (CDR) circuits, in particular, burst-mode CDR (BM-CDR) circuits. Moreover, the challenges depend on the multiple access method that is used to share the bandwidth among users. The research presented in this thesis provides both, theoretical and experimental demonstrations of BM-CDRs. While the theoretical work lays the foundations for analyzing novel BM-CDR architectures, the experimental expositions are designed to illustrate the application potential of these BM-CDRs in various optical testbeds—"a solution looking for problems".

We demonstrate two novel BM-CDR architectures based on oversampling in both the time and space domain. These BM-CDRs achieve error-free operation [bit error rate (BER) $< 10^{-10}$] while providing instantaneous (0 preamble bit) clock phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts. Instantaneous phase acquisition improves the physical efficiency of upstream PON traffic, and increases the effective throughput of the system by raising the information rate. Our eloquent, scalable BM-CDR architectures leverage the design of low complexity commercial electronics providing a cost-effective solution for PONs.

The first BM-CDR that we designed and implemented, is based on phase-tracking time domain oversampling (semiblind) CDR circuit operated at $2\times$ the bit rate and a clock phase aligner (CPA) that makes use of a phase picking algorithm. We demonstrate th BM-CDR operation at 5 Gb/s. The second BM-CDR is based on semiblind space domain oversampling and employs a phase-tracking CDR circuit with multiphase clocks

at the bit rate and a CPA with a novel phase picking algorithm. We demonstrate the BM-CDR operation at 10 Gb/s. Furthermore, we experimentally demonstrate these BM-CDRs in various optical test beds and study the effect of channel-impairments in: (1) 5 Gb/s time-division multiplexing (TDM) gigabit ethernet PON (GEPON) 20-km uplink; (2) 2.5 Gb/s overlapped subcarrier-multiplexing (O-SCM) wavelength-division multiplexed (WDM) PON 20-km uplink; (3) 1.25 Gb/s 1300-km deployed fiber link spanning from Montreal to Quebec City and back; and (4) 622 Mb/s in a 7-user incoherent spectral amplitude-coded optical code-division multiple access (SAC-OCDMA) 20-km PON uplink.

We also provide for the first time to our knowledge, a theoretical framework to model and analyze BM-CDRs. We develop a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$-oversampling CDRs. The theoretical model quantitatively explains the performance of these circuits in terms of the BER and packet loss ratio (PLR). The model accounts for the following parameters: (1) silence periods, including phase steps and the length of consecutive identical digits (CIDs) between successive upstream PON bursts from independent optical network units (ONUs); (2) finite frequency offset between the sampling clock and desired bit rate; (3) packet preamble length; (4) jitter on the sampling clock; and (5) pattern correlator error-resistance. On the basis of this theory, we analyze quantitatively the performance of the proposed BM-CDRs by performing a comprehensive theoretical analysis. That is, we evaluate the BER and PLR performance of the BM-CDRs to assess the tradeoffs between various parameters, and compare the results experimentally to validate the theoretical model. This analysis coupled with the experimental results will refine theoretical models of burst-mode front-end circuits and PONs, and provide input for establishing realistic power budgets.

Résumé

Les réseaux optiques à accès multiple, et plus spécifiquement les réseaux optiques passifs (PONs) sont considérés comme une des technologies les plus prometteuses pour le déploiement de fibre-aux-locaux/cabinet/bâtiment/domicile/usager (FTTx) qui résout le problème de bande passante limitée dans les réseaux locaux (LAN). Les PONs atteignent cet objectif à travers une solution à faible coût et avec une qualité de service (QoS) garantie. Dans un réseau PON, plusieurs usagers partagent la même infrastructure de fibre selon une topologie de réseau point-à-multipoint (P2MP). Ceci est opposé aux autres technologies d'accès actuelles qui sont basées sur une topologie de réseau point-à-point (P2P), notamment le 'digital subscriber line' asymétrique ou à vitesse très élevée (xDSL) et la technologie d'accès par câble coaxial. La nature des réseaux P2MP introduit des délais dans le chemin optique qui occasionnent des variations d'amplitude allant jusqu'à 20 dB et des variations de phase de -2π à 2π rad sur les paquets de données du trafic en mode rafale (burst-mode). En conséquence, cela crée de nouveaux défis pour la conception et le test des récepteurs optiques, des circuits de récupération d'horloge et de données (CDR); en particulier, les circuits CDR en mode rafale (BM-CDR). En plus, les défis dépendent de la méthode d'accès multiple qui est utilisée pour partager la bande passante entre les usagers. La recherche présentée dans cette thèse inclut des démonstrations théoriques et expérimentales de BM-CDRs. Alors que la théorie fournit les bases pour l'analyse de nouvelles architectures de BM-CDRs, les expositions expérimentales sont destinées à illustrer le potentiel d'application de ces BM-CDRs sur des bancs d'essais optiques divers, comme "une solution à la recherche de problèmes".

Nous démontrons deux architectures nouvelles de BM-CDRs basées sur un sur-échantillonnage dans le domaine temporel ainsi que dans le domaine spatial. Ces BM-CDRs atteignent un fonctionnement sans erreurs [taux d'erreur binaire (BER) $< 10^{-10}$] tout en fournissant une acquisition instantanée (0 bits préambule) de phase de l'horloge pour tous les pas de phases ($\pm 2\pi$ rad) entre les 'bursts' successives. L'acquisition de la phase instantanée améliore l'efficacité physique du trafic en amont du réseau PON, et accroît le débit effectif du système en augmentant le taux d'information. Nos architectures éloquentes et évolutives de BM-CDRs permettent la conception avec de l'électronique commerciale de faible complexité, offrant ainsi une solution rentable pour les PONs.

Le premier BM-CDR que nous avons conçu et réalisé est basé sur un circuit CDR à

sur-échantillonnage temporel (semi-aveugle, opéré à 2× le taux binaire) pour la suivie de phase et sur un aligneur de phase de l'horloge (CPA) qui utilise un algorithme de sélection de phase. Nous démontrons l'opération de ce BM-CDR à 5 Gb/s. Le deuxième BM-CDR est basé sur un sur-échantillonnage spatial semi-aveugle, et emploie un circuit CDR de suivi de phase avec des horloges à multi-phases au même débit binaire que l'information, et un CPA avec un algorithme nouveau pour la sélection de phase. Nous démontrons l'opération de celui-ci à 10 Gb/s. En plus, nous démontrons expérimentalement ces BM-CDRs sur différents bancs d'essais optiques et nous étudions l'effet de dépréciations de canal pour: (1) une liaison montante de 5 Gb/s d'un réseau optique passif gigabit Ethernet (GEPON) de 20 km, basé sur un multiplexage temporel (TDM); (2) une autre liaison en amont de 2.5 Gb/s d'un réseau optique passif à multiplexage par longueur d'onde (WDM PON), basé sur un multiplexage de sous-porteuses qui se chevauchent (O-SCM); (3) un lien optique de 1300 km (aller-retour) déployé entre Montréal et Québec à 1.25 Gb/s; et (4) une liaison montante de 7 usagers à 622 Mb/s sur un réseau optique passif de 20 km qui utilise un encodage spectral incohérent d'amplitude à accès multiple par répartition de codes (SAC-OCDMA).

Nous fournissons également, pour la première fois à notre connaissance, un cadre théorique pour modéliser et analyser les BM-CDRs. Nous développons une théorie unifiée probabiliste pour les BM-CDRs, basée sur des techniques de sur-échantillonnage semi-aveugle soit dans le domaine temporel, soit dans le domaine spatial. Cette théorie a été également généralisée pour les CDRs conventionnels et ceux à sur-échantillonnage de N fois. Le modèle théorique explique quantitativement les performances de ces circuits en termes de BER et du rapport de perte de paquets (PLR). Le modèle tient compte des paramètres suivants: (1) les périodes de silence y compris les pas de phase et la longueur des chiffres identiques consécutifs (CID) entre les 'bursts' successifs (en amont) qui viennent des unités de réseau optique (ONUs) indépendantes; (2) le décalage de fréquence fini entre l'échantillonnage de l'horloge et le débit binaire désiré; (3) la longueur de préambule des paquets; (4) la gigue de l'horloge de l'échantillonnage; et (5) la résistance aux erreurs du corrélateur de motif de bits. Sur la base de cette théorie, nous analysons quantitativement la performance des BM-CDRs proposés en effectuant une analyse théorique complète. Nous évaluons le BER et le PLR des circuits BM-CDRs pour évaluer les compromis entre les paramètres différents, et pour comparer les résultats avec les expériences afin de valider le modèle théorique. Cette analyse couplée avec ces résultats expérimentaux raffinera les

modèles théoriques des circuits ‘front-end’ de mode rafale et des PONs, et fournira des données pour établir des budgets de puissance réalistes.

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Many individuals have contributed to my research, and I would like thank them for everything they did. Dr. Ziad El-Sahn for the many fruitful collaborations including proposing, building, and characterizing the two SAC-OCDMA PON architectures and the O-SCM WDM PON architecture for testing my BM-CDRs, for reviewing my thesis at 2:30 AM, and for his camaraderie. Dr. Julien Faucher, PMC Sierra, for designing and implementing the original CPA at 622 Mb/s, for building the custom SMB-to-QSE interface PCB, and for all the enlightening discussions. Prof. Sophie LaRochelle, Laval University, for a fruitful collaboration on the 1300-km fiber link experiments. Ms. Ming Zeng and Mr. Nicholas Zicha, for porting the VHDL code of the CPA from the 622-Mb/s version on the Xilinx-II Pro FPGA board to the 5-Gb/s version on the Xilinx Virtex-IV FPGA board, and for providing technical assistance. Mr. Richard Karlquist, Agilent Technologies, and Mr. Bruce Massey, Hittite Microwave Corporation, for proposing the interface circuitry in the space sampling BM-CDR, and for the technical advice. Ms. Noha Kheder, for providing technical assistance during the SAC-OCDMA experiments. Ms. Yousra Ben M'Sallem, for characterizing the 1300-km deployed fiber link that spans from Montreal to Quebec City and back, to test the BM-CDR. Mr. Charles Allaire, for providing timely support on the 1300-km link on the RISQ network. Mr. Serge Doucet for building the lab prototype test bed to characterize the link. Mr. Christopher Rolston the *guru* and Ms. Kay Johnson for

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The long journey since my high school to graduate studies would not have been the same without my dear sister, Ami Talati, and dear friend and brother, Bharathram Sivasubramanian. I thank them for their constant encouragement and for always believing in me.

I would like to pay my humble respects to my Maa, Vibhuti J. Shastri and Paa, Jayprakash C. Shastri. They have dedicated their lives to my upliftment and no other cause is a noble as this one. No words can describe their importance in my life. I thank them for their prayers and blessings, and for always believing in me. I thank my Paa for lighting that "initial spark" that began everything—my interest in science and engineering. To my Maa who has redefined the term "Queen Sacrifice", I dedicate this thesis to her with all my love.

Finally, my beloved wife, Ishana M. Gopaul-Shastri. She is my source of inspiration and I feel complete with her. I thank her for always being by my side on this most magnificent journey. In her words "An infinite (∞) times yes by your side. Beyond time and space; one in the beauty of the cosmos." To quote Dr. John F. Nash, Jr. (Princeton University) "You are the reason I am. You are all my reasons." This thesis, for all its worth, is dedicated to her.

Bhavin J. Shastri
November 2011

Associated Publications

The evidence of the original contributions to the overall existing body of knowledge of burst-mode clock and data recovery circuits is manifested by the 22 peer-reviewed publications that have so far resulted from the research presented in this thesis. These papers are in the form of 7 journal articles [1–7] and 15 conference proceedings [8–22] along with two invited conference papers.

Journal Articles

[1] **B. J. Shastri** and D. V. Plant, "Truly modular burst-mode CDR with instantaneous phase acquisition for multiaccess networks," *IEEE Photonics Technology Letters,* in press, 2011.

[2] **B. J. Shastri**, C. Chen, K. D. Choquette, and D. V. Plant, "Circuit modeling of carrier–photon dynamics in composite-resonator vertical-cavity lasers," *IEEE Journal of Quantum Electronics,* in press, 2011.

[3] **B. J. Shastri** and D. V. Plant, "5/10-Gb/s burst-mode clock and data recovery based on semiblind oversampling for PONs: theoretical and experimental," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 16, no. 5, pp. 1298–1320, Sep.-Oct. 2010.

[4] **B. J. Shastri**, Y.-B. M'Sallem, N. Zicha, L. A. Rusch, S. LaRochelle, and D. V. Plant, "Experimental study of burst-mode reception in a 1300 km deployed fiber link," *IEEE/OSA Journal of Optical Communications and Networking,* vol. 2, no. 1, pp. 1–9, Jan. 2010.

[5] **B. J. Shastri**, J. Faucher, N. Kheder, M. Zeng, N. Zicha, and D. V. Plant, "Performance analysis of burst-mode receivers with clock phase alignment and forward error correction for GPON," *Analog Integrated Circuits and Signal Processing,* vol. 60, no. 1, pp. 57–70, Aug. 2009.

[6] **B. J. Shastri**, Z. A. El-Sahn, M. Zeng, N. Kheder, L. A. Rusch, and D. V. Plant, "A standalone burst-mode receiver with clock and data recovery, clock phase alignment, and RS(255,239) codes for SAC-OCDMA applications," *IEEE Photonics Technology Letters*, vol. 20, no. 5, pp. 363–365, Mar. 2008.

[7] Z. A. El-Sahn, **B. J. Shastri**, M. Zeng, N. Kheder, D. V. Plant, and L. A. Rusch, "Experimental demonstration of a SAC-OCDMA PON with burst-mode reception: local versus centralized sources," *IEEE/OSA Journal of Lightwave Technology,* vol. 26, no. 10, pp. 1192–1203, May 2008.

Conference Proceedings

[8] **B. J. Shastri** and D. V. Plant, "A 10-Gb/s space sampling burst-mode clock and data recovery circuit for passive optical networks," in *Proc. IEEE Photonics Conference (IPC),* Arlington, VA, USA, Oct. 2011, paper ThFF.3, pp. 937–938.

[9] Z. A. El-Sahn, **B. J. Shastri**, J. M. Busset, and D. V. Plant, "A robust overlapped-SCM WDM PON with a standalone burst-mode OLT receiver," in *Proc. IEEE Photonics Conference (IPC),* Arlington, VA, USA, Oct. 2011, paper TuE.6, pp. 226–227.

[10] D. V. Plant, Z. A. El-Sahn, J. M. Busset, and **B. J. Shastri**, "Overlapped subcarrier multiplexed WDM PONs enabled by burst-mode receivers,"in *Proc. Access Networks and In-house Communications (ANIC) Topical Meeting,* Toronto, ON, Canada, Jun. 2011; note this is an **Invited Paper**.

[11] **B. J. Shastri** and D. V. Plant, "Scaling technologies for terabit fiber optic transmission systems," in *Proc. SPIE,* vol. 7942, paper 794206, Feb. 2011; note this was an **Invited Paper** at the *SPIE Photonics West*, San Francisco, CA, USA, Jan. 2011.

[12] **B. J. Shastri** and D. V. Plant, "Probabilistic theory for semi-blind oversampling burst-mode clock and data recovery circuits," in *Proc. IEEE Midwest Symposium on Circuits and Systems (MWSCAS),* Seattle, WA, USA, Aug. 2010, pp. 161–164; note this work was the recipient of the **IEEE MWSCAS Best Student Paper Award** [international competition; second place from 321 papers; top 3 awarded annually].

[13] **B. J. Shastri** and D. V. Plant, "Burst-mode clock and data recovery for optically interconnected data centers," in *Proc. IEEE Photonics Society Summer Topical Meetings,* Playa del Carmen, Riviera Maya, Mexico, Jul. 2010, paper MD4.3, pp. 201–202; note this work received the **Graduate Research Enhancement Travel (GREAT) Award**, McGill University, 2010 [institutional competition].

[14] M. Zeng, **B. J. Shastri**, N. Zicha, and D. V. Plant, "Experimental demonstration of a novel 5/10-Gb/s burst-mode clock and data recovery circuit for Gigabit PONs," in *Proc. Optical Fiber Communication (OFC),* San Diego, CA, USA, Mar. 2009, paper OWA3; note this work was the winner of the **SYTA*Com* Student Research Competition** at the *Center for Advanced Systems and Technologies in Communications (SYTACom) Annual Workshop,* Montreal, QC, Canada, Apr. 2009 [provincial competition; first place; top 3 awarded annually].

[15] **B. J. Shastri**, N. Kheder, M. Zeng, N. Zicha, and D. V. Plant, "Experimental investigation of packet loss ratio performance of burst-mode receivers in GPON," in *Proc. IEEE Laser and Electro-Optics Society Annual Meeting (LEOS),* New Port Beach, CA,

USA, Nov. 2008, paper WW3, pp. 602–603; note this work was the winner of the **CIPI Best Student Poster Award** at the *Canadian Institute for Photonic Innovation (CIPI) Annual General Meeting,* Banff, AB, Canada, Jun. 2008 [national competition; first place; top 3 awarded annually].

[16] M. Zeng, **B. J. Shastri**, N. Zicha, M. Schueren, and D. V. Plant, "3.5 Gb/s burst-mode clock phase aligner for gigabit passive optical networks," in *Proc. IEEE Laser and Electro-Optics Society Annual Meeting (LEOS),* New Port Beach, CA, USA, Nov. 2008, paper WEE5, pp. 675–676.

[17] M. Zeng, **B. J. Shastri**, N. Zicha, M. Schueren, and D. V. Plant, "5 Gb/s burst-mode clock phase aligner with (64, 57) hamming codes for GPON applications," in *Proc. IEEE Microsystems and Nanoelectronics Research Conference (MNRC),* Ottawa, ON, Canada, Oct. 2008, pp. 17–20; note this work was the recipient of the **IEEE MNRC Silver Leaf Certificate** *for the best student paper* [international competition; top 3 awarded annually].

[18] **B. J. Shastri**, N. Kheder, and D. V. Plant, "Effect of channel impairments on the performance of burst-mode receivers in gigabit PON," in *Proc. IEEE Midwest Symposium on Circuits and Systems (MWSCAS),* Knoxville, TN, USA, Aug. 2008, pp. 390–393; note this work was the winner of the **CIPI Best Student Poster Award** at the *Canadian Institute for Photonic Innovation (CIPI) Annual General Meeting,* Ottawa, ON, Canada, May 2007 [national competition; first place; top 3 awarded annually].

[19] Z. A. El-Sahn, M. Zeng, **B. J. Shastri**, N. Kheder, D. V. Plant, and L. A. Rusch, "Dual architecture uplink demonstration of a 7×622 Mbps SAC-OCDMA PON using a burst-mode receiver," in *Proc. Optical Fiber Communication (OFC),* San Diego, CA, USA, Feb. 2008, paper OMR3.

[20] N. Kheder, Z. A. El-Sahn, **B. J. Shastri**, M. Zeng, L. A. Rusch, and D. V. Plant, "Performance of incoherent SAC-OCDMA using a burst-mode receiver with CDR and FEC," in *Proc. IEEE Laser and Electro-Optics Society Annual Meeting (LEOS),* Orlando, FL, USA, Oct. 2007, paper WX2, pp. 610–611.

[21] **B. J. Shastri**, J. Faucher, M. Zeng, and D. V. Plant, "Burst-mode clock and data recovery with FEC and fast phase acquisition for burst-error correction in GPONs," in *Proc. IEEE Midwest Symposium on Circuits and Systems (MWSCAS),* Montreal, QC, Canada, Aug. 2007, pp. 120–123; note this work was nominated for the **IEEE MWSCAS Best Student Paper Award** [international competition; top 10 finalist from 620 papers; top 3 awarded annually].

[22] **B. J. Shastri**, J. Faucher, M. Zeng, and D. V. Plant, "622/1244 Mb/s burst-mode clock and data recovery for gigabit passive optical network uplink," in *Proc. IEEE*

Laser and Electro-Optics Society Annual Workshop on Interconnections within High Speed Digital Systems (HSD), Santa Fe, NM, May 2007; note this work received the **IEEE Photonics Society Travel Grant**, 2007 [international competition].

Contents

List of Figures

List of Tables

List of Acronyms

ADSL	Asymmetric DSL
APD	Avalanche photodiode
ASIC	Application-specific integrated circuit
AWG	Arrayed waveguide grating
B2B	Back-to-back
BBS	Broadband source
BER	Bit error rate
BERT	BER tester
BBERT	Burst BERT
BIBD	Balanced incomplete block design
BM-CDR	Burst-mode CDR
BM-LA	Burst-mode limiting amplifier
BMRx	Burst-mode receiver
BM-TS	Burst-mode test setup
BPF	Band-pass filter
CATV	Cable television
CDMA	Code-division multiple-access
CDR	Clock and data recovery
CID	Consecutive identical digit
CLT	Central limit theorem
CML	Current mode logic
CLS	Centralized LS
CO	Central office
COTS	Commercial-off-the-shelf

CP	Charge pump
CPA	Clock phase aligner
CPE	Customer premise equipment
CRU	Clock recovery unit
dB	decibel
DBA	Dynamic bandwidth allocation
DCD	Duty cycle distortions
DCF	Dispersion compensation fiber
DCM	Digital clock manager
DDJ	Data-dependent jitter
DDR	Double-data rate
DEC	Decoder
DES	Deserializer
DFB	Distributed-feedback
D-FF	D flip-flop
DJ	Deterministic jitter
DSL	Digital subscriber link
DUT	Device under test
EAM	Electro-absorption modulator
EDFA	Erbium-doped fiber amplifier
EML	Electro-absorption modulated laser
ER	Extinction ratio
FBG	Fiber Bragg grating
FEC	Forward-error correction
FFH	Fast-frequency hop
FP	Fabry-Perot
FPGA	Field-programmable gate array
FTTx	Fiber-to-the-x; x denotes home (H), curb (C), building (B), or premises (P)
GE-PON	Gigabit ethernet PON
GPON	Gigabit-capable PON
GVCO	Gated VCO
HDTV	High-definition television
IC	Integrated circuit

IP	Internet protocol
ISI	Intersymbol interference
LA	Limiting amplifier
LAN	Local area network
LED	Light emitting diode
LO	Local oscillator
LPF	Low-pass filter
LS	Local sources
LT	Line terminator
LTI	Linear time-invariant
LVDS	Low-voltage differential signaling
MAI	Multiple access interference
MAN	Metropolitan area network
MZM	Mach-Zehnder modulators
NRZ	Non-return to zero
OCDMA	Optical CDMA
ODN	Optical distribution network
OE	Optical-to-electrical
OLT	Optical line terminal
ONT	Optical network terminal
ONU	Optical network unit
OOK	On-off keying
OPSN	Optical packet switched network
O-SCM	Overlapped SCM
P2MP	Point-to-multipoint
P2P	Point-to-point
PCB	Printed circuit board
PD	Phase detector
PLL	Phase-locked loop
PLR	Packet loss ratio
PMD	Physical medium dependent
PON	Passive optical network
PPM	Parts-per-million

PRBS	Pseudorandom binary sequence
PS	Power splitter
PVT	Process, temperature, and supply variation
PWDJ	Pulse-width-distortion jitter
QFN	Quad-flat no-leads
QoS	Quality of service
QSE	Q-strip interface socket
RF	Radio frequency
RJ	Random jitter
RN	Remote node
RS	Reed-Solomon
RSOA	Reflective SOA
SAC-OCDMA	Spectral amplitude-coded OCDMA
SCM	Subcarrier-multiplexing
SJ	Sinusoidal jitter
SMA	SubMiniature version A
SMB	SubMiniature version B
SMF	Single-mode fiber
SME	Small & Medium Enterprise
SMT	Surface-mount technology
SOA	Semiconductor optical amplifier
SOIC	Small-outline integrated circuit
SNR	Signal-to-noise ratio
SOHO	Small Office Home Office
SONET	Synchronous optical network
TDF	Threshold determination field
TDM	Time-division multiplexing
TDMA	Time-division multiple access
TIA	Transimpedance amplifier
T&M	Test and measurement
UBJ	Uncorrelated bounded jitter
UI	Unit interval
VCO	Voltage-controlled oscillator

VDSL	Very-high-bit-rate speed DSL
VOA	Variable optical attenuator
VoD	Video on demand
VPN	Virtual private network
WDM	Wavelength-division multiplexing
WDMA	Wavelength-division multiple access

Chapter 1

Introduction

THE past decade has seen profound changes not only in the way we communicate, but also in our expectations of what optical networks will deliver in terms of speed and bandwidth. As the explosive growth in Internet traffic continues, the need for highly-specialized low-cost application-specific integrated circuits (ASICs) in back plane routing and chip-to-chip interconnects, is undeniable. Furthermore, the coming decade promises to demand even more capacity and bandwidth in these networks, creating unique requirements and challenges for the design of optical receivers. It is in this context that in this thesis we present our research on novel high-speed receiver architectures, both theoretically and experimentally.

In this chapter, we set the stage for the entire thesis. Section 1.1 motivates the research by presenting the case for the introduction of fiber-optics in access networks. Section 1.2 details the problem statement putting our work on optical receivers in context. In Section 1.3 we outline the research objectives that demarcate the course of this research. A summary of our original contributions is presented in Section 1.4. Finally, Section 1.5 provides an overview of the thesis.

1.1 Motivation

In this section, we consider some of the motivating factors for introducing fiber-optics in access networks. We also look at some of the solutions for optical networks and briefly describe the typical architecture along with the various multiplexing schemes employed in these networks.

1.1.1 Access Networks

Fiber-optic communications has been a clear winner in the field of long-haul communications. In the last decade, fiber-optics has also found its way into metropolitan area networks (MANs). The fiber is now penetrating into the access domain.

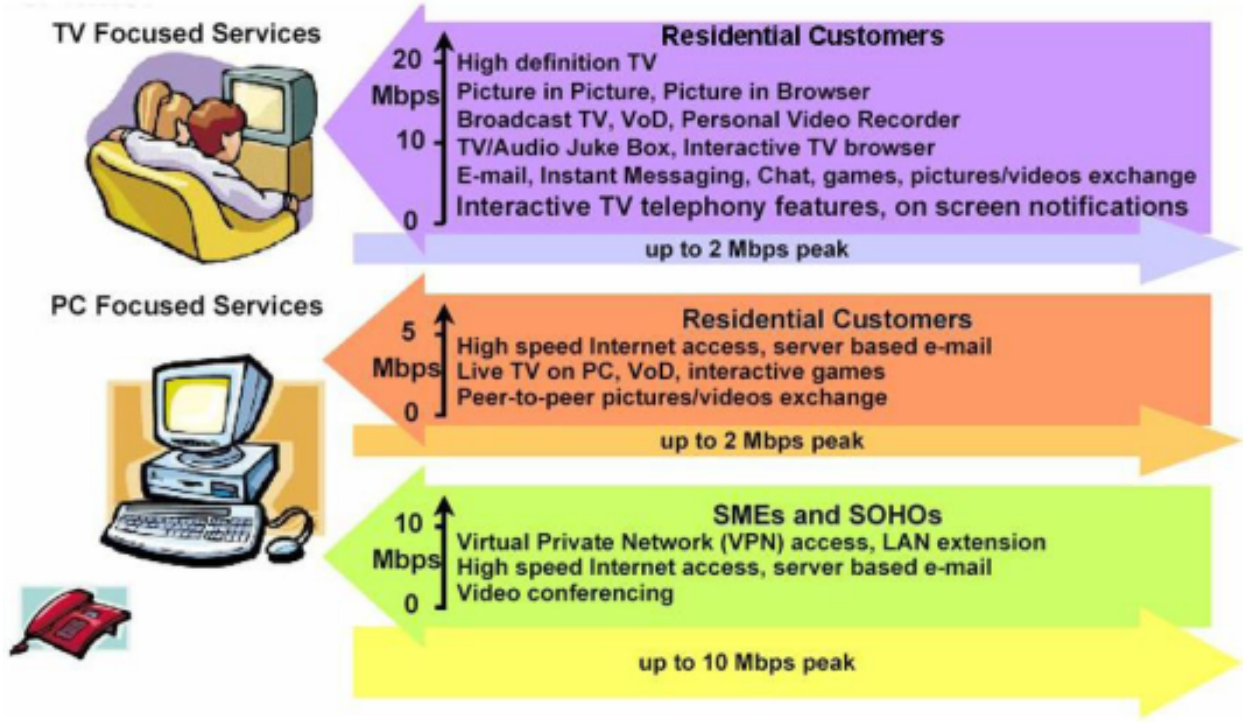

Fig. 1.1 Different applications for private homes, SOHOs and SMEs [3] (SOHOs: Small Office Home Offices; SMEs: Small & Medium Enterprises; VoD; video on demand).

After having experienced constant growth for numerous decades, fiber-optic system capacities are increasing exponentially with the plethora of data services—most notably by heavily data-centric users [1]—that drive the network traffic growths between 40 and 90 percent per year [2]. Fig. 1.1 looks at some of these applications for both residential customers, SOHOs (Small Office Home Offices) and SMEs (Small & Medium Enterprises) [3]. The applications can be classified by separating them into the triple services of voice, video and data. Voice services are not expected to be a significant driver of the bandwidth demand in the future. Video applications include high-definition television (HDTV) and broadcast digital TV. Data applications include virtual private network (VPN) access and

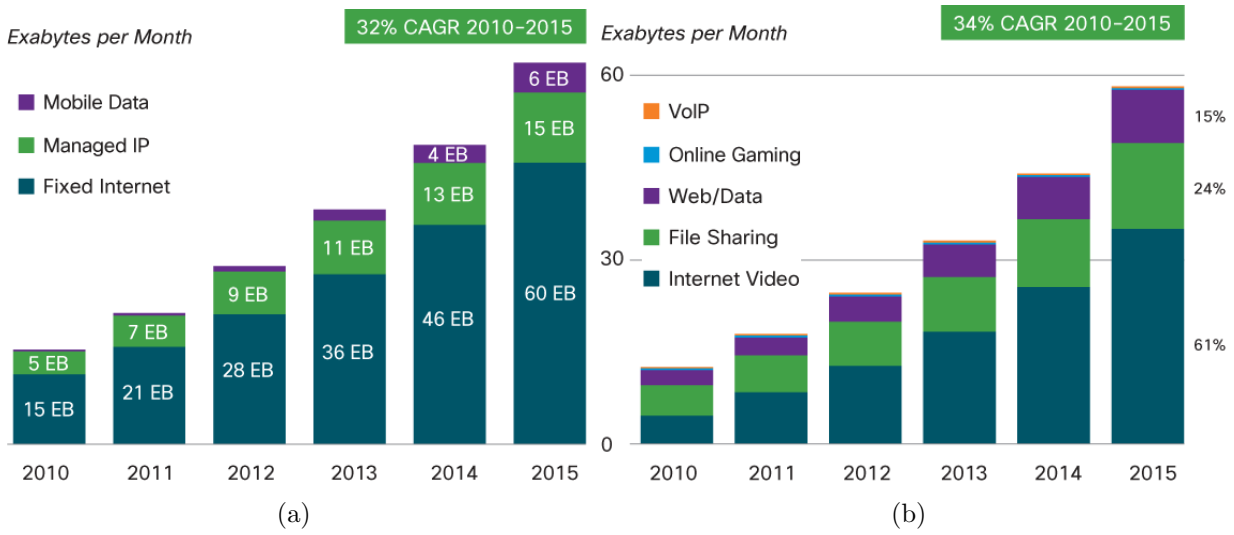

Fig. 1.2 (a) Cisco VNI Global IP Traffic Forecast [4]. (b) Global consumer Internet traffic [4].

teleconferencing applications. Video and data will be the main driver of bandwidth demand in the future. This trend is depicted in Fig. 1.2(a) [4] which shows that the overall IP traffic is expected to grow to 81 exabytes per month by 2015 (up from 20 exabytes per month in 2010), of which 60 exabytes per month are due to consumer traffic. Fig. 1.2(b) shows the components of consumer Internet traffic growth. It is interesting to note that by year end 2012, 50 percent of consumer Internet traffic that will be generated every month will nearly be due to Internet video. Clearly, over the last 15 years there has been an increase by more than three orders of magnitude in the capacity of fiber-optic networks, resulting in a proportional decrease in the cost to transport data across transport networks [5].

A considerably large number of economic and social benefits have been put forward to justify the cost of additional infrastructure necessary for broadband networks [6]. From the increase in number of broadband subscriptions (discussed next), more customers are also increasingly willing to pay for the excess bandwidth as shown by the increase. The importance of the access networks has also been encapsulated in the concept of "ambient intelligence", a concept identified by the European Union for developing a future information society [7, 8].

While the general success of fiber-optic technology in long-haul networks and MANs provides a strong motivation for its introduction in access networks, it is still instructive to

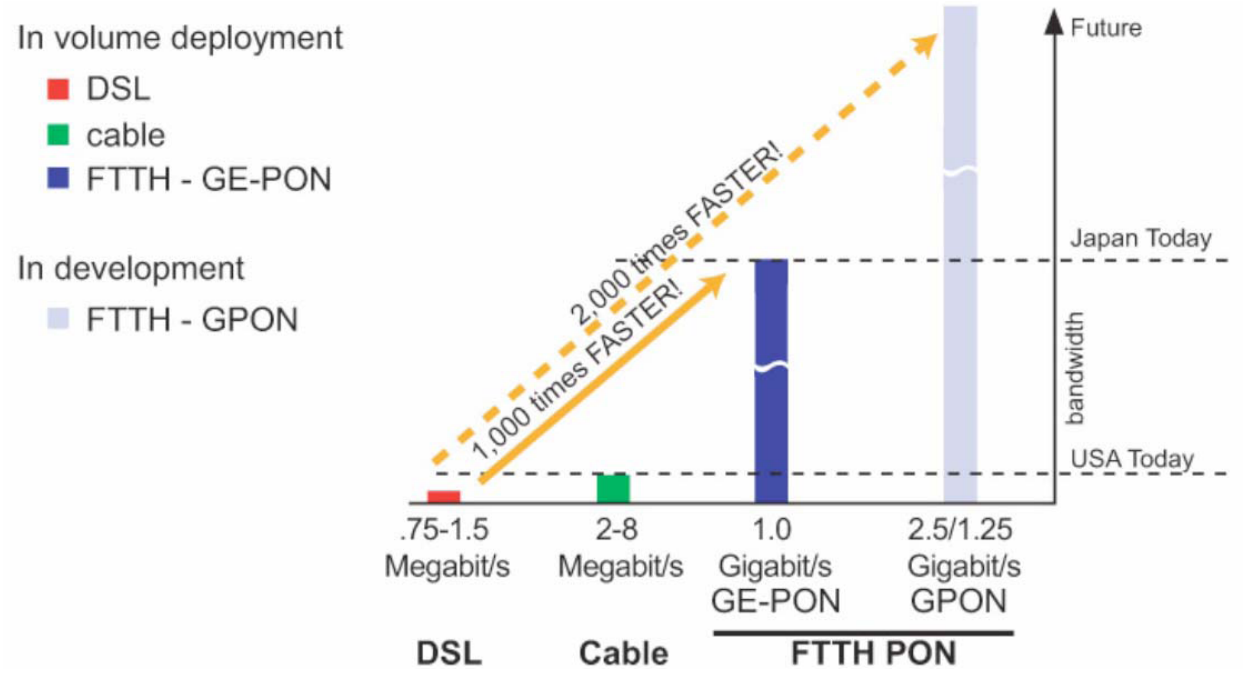

Fig. 1.3 Access network technologies: market and technology overview. Note that "today" corresponds to 2005, the publication year of the white paper [9] (DSL: digital subscriber link; FTTH: fiber-to-the-home; GE-PON; gigabit ethernet PON; GPON: gigabit-capable PON; PON: passive optical network).

take a careful look at the requirements and challenges that are unique to access networks.

1.1.2 Fiber-to-the-x

Various technologies have been considered as solutions for the access market. These broadband access technologies include the digital subscriber link (DSL), including asymmetric DSL (ADSL) and very-high-bit-rate DSL (VDSL), cable modem, wireless technologies such as WiFi and WiMax, satellite systems, power line solutions, and fiber-optic solutions—fiber-to-the-x (FTTx); where x, denoting home (H), curb (C), building (B), or premises (P), indicates how close the fiber endpoint comes to the actual user. From a historical perspective, the first bandwidth breakthrough in the access network was the arrival of DSL and cable-based solutions (see Fig. 1.3 [9]). They have provided nearly a 1000-fold increase in data rates over traditional 'dial-up' modems, and are the predominant technologies used currently for private homes. DSL is used to transport high-speed data traffic on copper

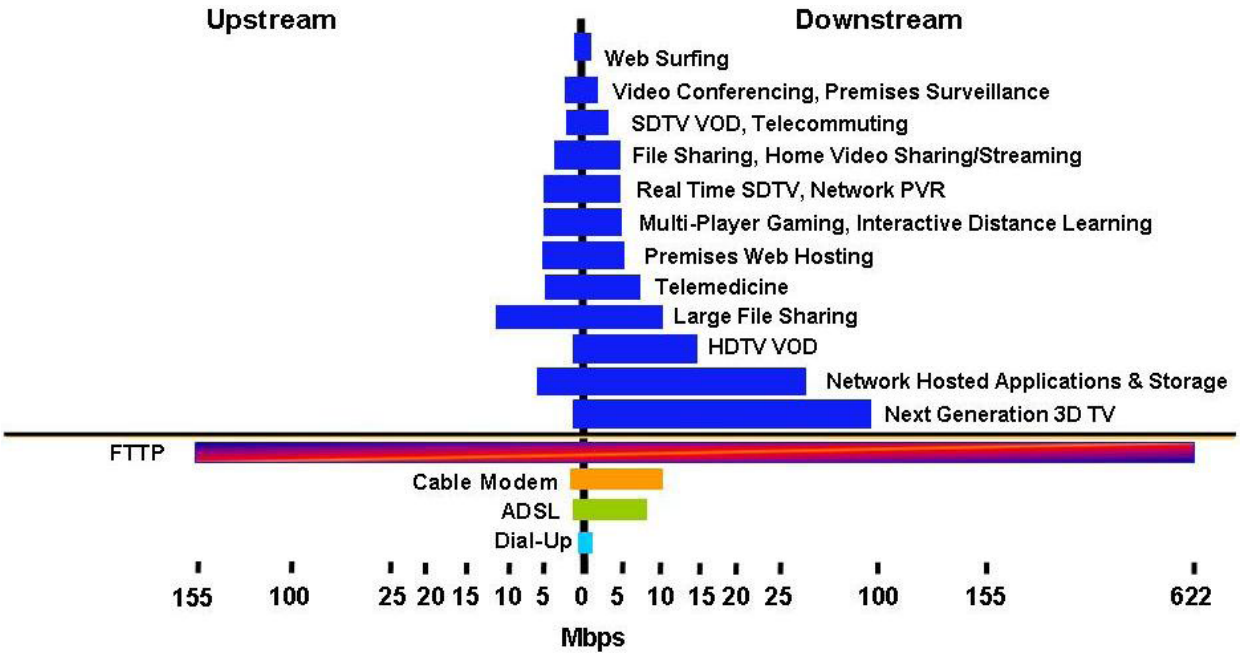

Fig. 1.4 Various applications and their demands for upstream and downstream bandwidth. Different access solutions and their capabilities in both directions are also illustrated [10] (ADSL: asymmetric digital subscriber link; HDTV: high-definition television; VoD; video on demand).

wires and provides dedicated bandwidth to each user. However, it suffers from a severe loss in bandwidth with distance. While cable modems do not have a degradation in bandwidth with distances, it does not offer dedicated bandwidth. Therefore, while DSL and cable solutions are more popular today than the other access solutions, they are only expected to be a transient solution.

Fig. 1.4 illustrates different applications with their requirements on upstream and downstream bandwidths [10]. Most of the applications that are prevalent today (HDTV and video on demand (VoD)) require very little upstream bandwidth and very high bandwidth downstream. In comparison, data services place a more symmetric requirement on the upstream and downstream bandwidths. In the future, the access infrastructure will be increasingly expected to handle both downstream and upstream bandwidths with equal amount of ease. From Fig. 1.4, we can see that this will be a tough requirement for both DSL and cable modems. As Fig. 1.3 illustrates, with the arrival of FTTx access solutions, another 1000-fold increase in data rates over DSL was achieved. It is expected that as a long-term scalable solution, FTTx may be the *only* solution for meeting these demands—

future-proof bandwidth, the end game for many service providers [11–15].

The reduction in the cost of electro-optic components and improvements in the handling of fiber optics now makes FTTx a cost effective solution in many situations. The transition to FTTx in the access network is also a benefit for both consumers and service providers because it opens up the near limitless capacity of the core long-haul network to the local user. FTTx is therefore currently being aggressively deployed by the service provider community worldwide [15, 16]. It is no longer a question of "if" FTTx is necessary to meet burgeoning residential and corporate user demands it is a question of "when".

In numbers, FTTH rollout has recently surpassed 30 million users on the globe and is continuing to grow at a rapid rate. In Japan, the number of FTTH users has overtaken the number of DSL users in March 2008, and has exceeded 15 million [17]. Furthermore, in North America a market trigger will push service providers to deploy fiber more widely than the current 6 million users. One of the life cycle analysis on the environmental benefits of FTTH concludes that the environmental impact of the deployment of a typical FTTH network in the United States will be positive within less than 6 years in average considering only the benefits associated to teleworking [17]. FTTH solutions can offer considerable additional social and economical benefits and are a key sustainable utility driver [18]. The most promising solution that has been recognized for deploying FTTx is the passive optical network (PON) [11, 19, 20, 23]. We discuss this next.

1.1.3 Passive Optical Networks

PONs are an emerging multiaccess network technology based on all-optical core. They are identified as an economic and future-safe solution to alleviate the so called "last mile" problem that remains a bottleneck between the backbone network and high-speed local area networks (LANs) [11, 12]. Consequently, the promise of a better bundle of distributive and interactive multimedia services such as video, voice, data, and fast Internet, to a large number of subscribers with guaranteed quality of service (QoS) by PONs, is compelling [21].

The notable feature of the PONs, as the name implies, is the complete absence of active elements at all points in the network other than at endpoints. Therefore, they have the advantage of being easy to operate. Also as community concerns about global enery consumption grow, the power consumption of broadband networks is becoming an important issue [17]. PONs can provide optical access services at low cost and low energy

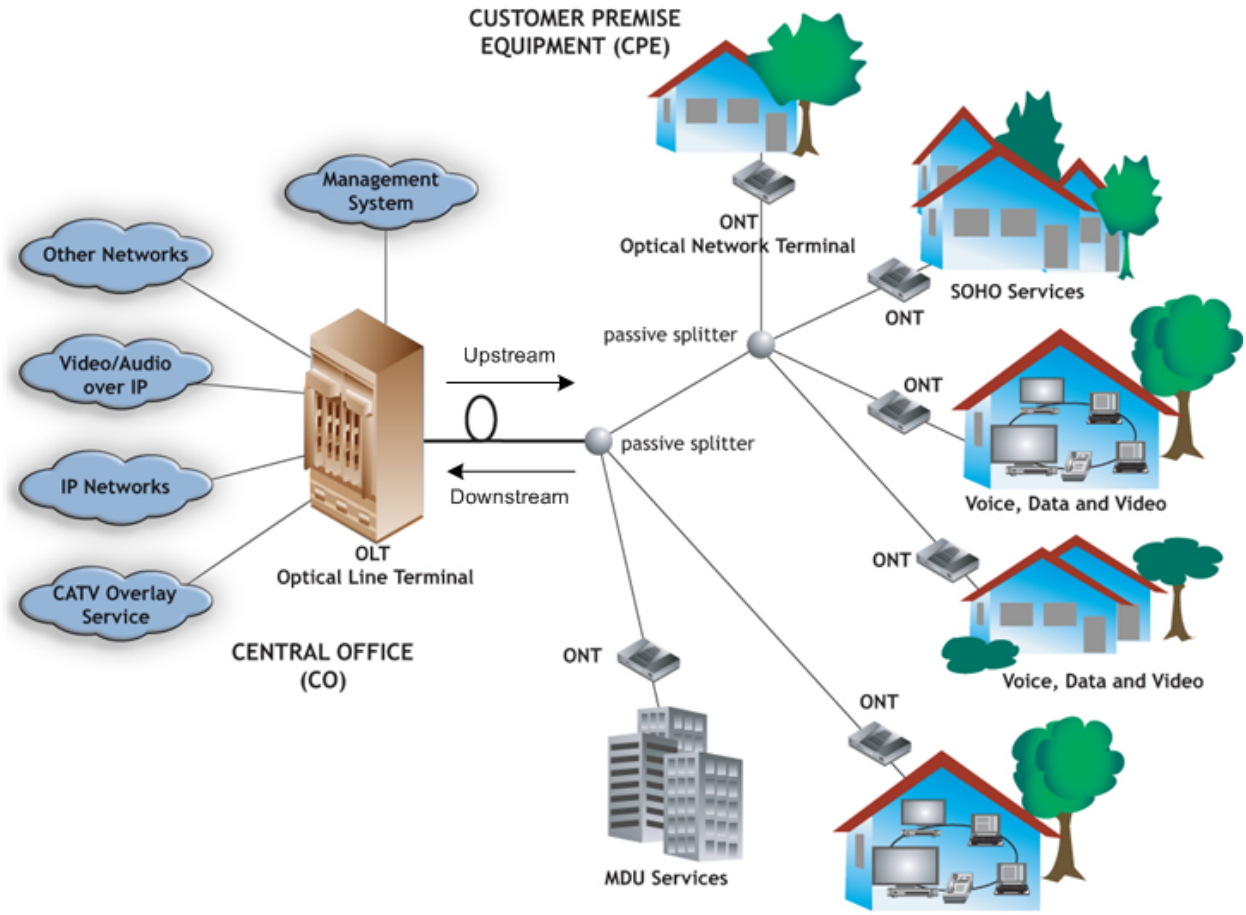

Fig. 1.5 Typical architecture of a PON for FTTx access networks [23] (CATV: cable television; CO: central office; CPE: customer premise equipment; OLT: optical line terminal; ONT: optical network terminal; SOHO: small office home offices).

(almost 50% reduction in lifetime emissions) by sharing optical fiber cables and transmission equipments in the network side by several users [22].

Fig. 1.5 shows a typical architecture of a PON [23]. A PON has a physical tree topology with the central office (CO) located at the root and the subscribers connected to the leaf nodes of the tree. At the root of the tree is an optical line terminal (OLT), which is the service provider equipment. Multiple optical network units (ONUs), also called optical network terminals (ONTs), are connected to the OLT through a passive optical coupler, and may be at different distances. The maximum transmission distance between the ONUs and the OLT is usually 10–20 km.

Each ONU can serve a single or multiple subscribers. The ONU buffers data received from its attached subscriber(s) and may use priority queues for different traffic classes. Due to the directional properties of the optical splitter/combiner, the OLT is able to broadcast data to all ONUs in the downstream direction. In the upstream direction, however, ONUs cannot communicate directly with one another. Instead, each ONU is able to send data only to the OLT. Thus, in the downstream direction the PON may be considered as a point-to-point (P2P) network, whereas for the upstream direction it may be viewed as a point-to-multipoint (P2MP) network.

In a PON, traffic multiplexing is done optically by merging the data streams at the optical combiner. Collision of the individual data streams needs to be avoided by well-designed multiple access techniques. We briefly introduce these multiplexing schemes which include time-division multiple access (TDMA), wavelength-division multiple access (WDMA), and optical code-division multiple access (OCDMA).

TDMA PONs

In time-division multiplexing (TDM) PONs, the upstream packets from the ONUs are time-interleaved at the power splitting point. This requires careful synchronization of the packet transmission instants at the ONUs. The synchronization is achieved by means of grants sent from the OLT, which instruct the ONU when to send a packet. The correct timing of these submissions is achieved by ranging protocols, which sense the distance from each ONU to the OLT. TDM PONs enjoy low installation and maintenance costs, however, they do not exploit the huge bandwidth of optical fibers. That is, as the ONUs jointly share the capacity of the OLT, the average capacity per ONU decreases when the number of ONUs grows.

WDMA PONs

Incorporating wavelength-division multiplexing (WDM) technology offers a good solution to increase the capacity of standard PONs. In a WDMA system (also known as WDM PON), each ONU is assigned dedicated wavelengths for upstream and downstream transmissions [24–26]. Wavelength multiplexing/demultiplexing components, usually realized with arrayed waveguide grating (AWG), must be deployed in the field to securely route each wavelength. WDM PONs create P2P links between the CO and each user, so no

sharing is needed. However, dedicated transceivers with accurate wavelength control result in significant installation and maintenance expenses. WDM PONs are high performance but expensive access solutions today. As the demand for bandwidth increase and the cost of optical components decrease, WDM PONs will become practical and consequential.

OCDMA PONs

An alternative to WDM is the use of OCDMA to upgrade existing PONs. OCDMA is receiving considerable attention because it combines the large bandwidth of the fiber medium with the flexibility of the code-division multiple-access (CDMA) technique to achieve high-speed connectivity [27]. It is a promising approach with its simple ONU and OLT configurations requiring no synchronization [28–30]. PON infrastructures (i.e., passive splitters) need not be upgraded to adopt OCDMA. Other attractive features of OCDMA include all-optical processing, truly asynchronous transmission, bandwidth efficiency, soft capacity on demand, protocol transparency, simplified network control, and flexibility on controlling the QoS [27, 28].

1.2 Problem Statement

Fig. 1.6 shows a general architecture of a standard commercial PON with our work in context. As already mentioned, in the downstream direction, the network is P2P. Continuous data is broadcast from the OLT to the ONUs in the 1480–1550-nm wavelength band. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous-mode integrated circuits (ICs). The challenge in the design of a chip set for PONs comes from the upstream data path. In the upstream direction, the network is P2MP; multiple ONUs transmit data in the 1310-nm window to the OLT in the CO. To use the shared medium effectively, the ONUs require a burst-mode transmitter with a short turn-ON/OFF delay [31]. Because of optical path differences in the upstream path, packets can vary in amplitude ΔA, and phase $\Delta\varphi$—bursty data.

Fig. 1.6 illustrates the concept of optical path differences, that is, large distance variations of customers from the CO. If the closest and the farthest customers attached to a common power splitter are 20 km apart and if the fiber attenuation is 0.5 dB/km, there is a 10-dB difference in the signal amplitudes that arrive at the OLT from these two users if both have the same upstream laser output level. If there is an additional power splitter in

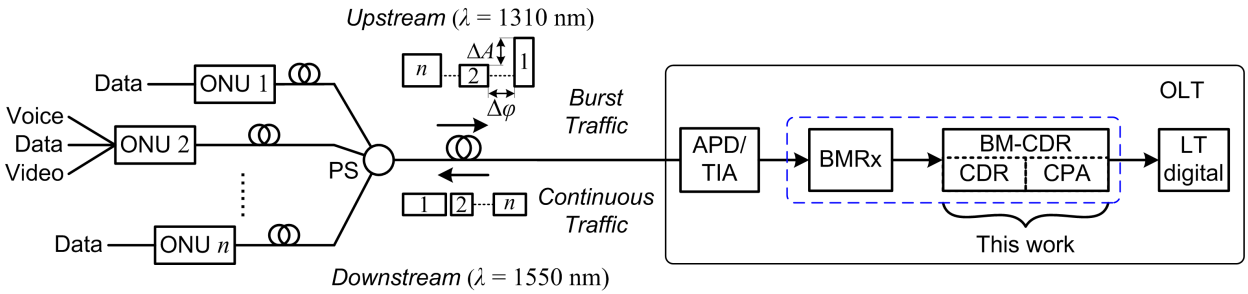

Fig. 1.6 Generic PON showing our work on optical receivers in context (APD: avalanche photodiode; BMRx: burst-mode receiver; BM-CDR: burst-mode CDR; CDR: clock and data recovery; CPA: clock phase aligner; LT: line terminator; OLT: optical line terminal; ONU: optical network unit; PS: power splitter; TIA: transimpedance amplifier).

the transmission path going to one of the ONUs, the difference in signals arriving at the OLT could vary up to 20 dB [32]. Moreover, the inevitable and random variations of phase steps between the successive packets may be anywhere between -2π rad to $+2\pi$ rad [33]. Fig. 1.7 depicts a typical burst-mode signal, which consists of a quick succession of packets [34].

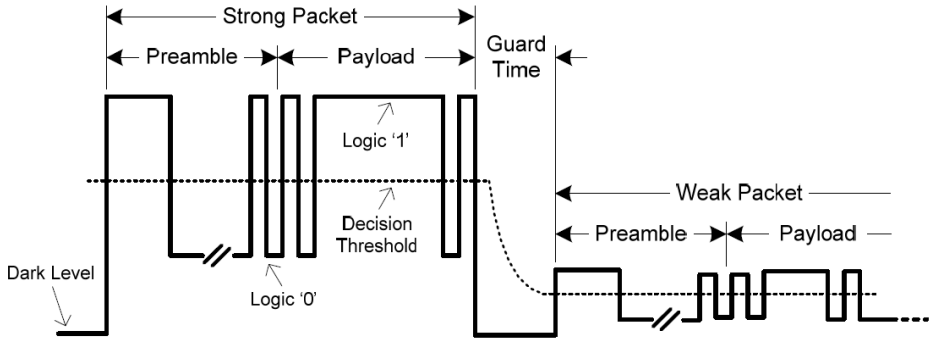

Fig. 1.7 Typical burst-mode signal consisting of a quick succession of packets [34].

Since a conventional optical receiver is not capable of instantaneous handling of rapidly changing differences in signal amplitude and clock phase alignment, a specially designed burst-mode receiver (BMRx) and burst-mode clock and data recovery (BM-CDR) circuits are needed, respectively. These circuits can quickly extract the decision threshold and determine the signal phase from a set of overhead bits—a preamble field—placed at the beginning of each packet burst. However, this methodology results in a receiver sensitivity

power penalty of up to 3 dB [32].

1.2.1 Burst-Mode Receivers

Amplitude variations between successive bursts impose limitations on conventional receivers that employ ac-coupling methods. This is because the residual charge in a coupling capacitor following any particular data burst cannot dissipate fast enough not to affect the initial conditions for the next burst. Consequently, to deal with these amplitude variations, the OLT requires a BMRx responsible for fast amplitude recovery, which must be achieved at the beginning of every packet.

Fast amplitude recovery is performed by the BMRx with dc-coupled operation accommodated by additional circuitry. The key requirements of a BMRx are high sensitivity, wide dynamic range, and fast response time. The sensitivity is important in relation to the optical power budget, since, for example, a 3-dB sensitivity improvement can double the size of the power splitter so that more subscribers can be attached to the PON. A wide dynamic range is essential for achieving a long network reach, that is, to be able to accommodate users located both close and far away from the power splitter.

1.2.2 Burst-Mode Clock and Data Recovery

The inevitable and random nature of phase steps between successive bursts can cause conventional clock and data recovery (CDR) circuits based on phase-locked loops (PLLs), to lose pattern synchronization leading to packet loss. Preamble bits can be inserted at the beginning of each packet to allow the CDRs enough time to settle down and acquire lock. However, this overhead reduces the effective throughput and increases delay. Consequently, to deal with these phase variations, the OLT requires a BM-CDR responsible for fast phase recovery, which must be achieved at the beginning of every packet. Fast clock and data recovery together with phase acquisition is performed by the BM-CDR with the help of a clock phase aligner (CPA). The most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible. Instantaneous phase acquisition improves the physical efficiency of upstream PON traffic, and increases the effective throughput of the system by raising the information rate.

The focus of this thesis is on the BM-CDR aspect of burst-mode reception, both theoretically and experimentally. It is in this context that we next outline the pertinent research

topics that we investigate together with the respective objectives.

1.3 Research Objectives

The research presented in this thesis aims to provide both, theoretical and experimental demonstrations of BM-CDRs. While the theoretical work lays the foundations for analyzing novel BM-CDR architectures, the experimental expositions are designed to illustrate the application potential of these BM-CDRs in various optical testbeds. Broadly speaking, we investigate the following two research topics: (1) BM-CDR circuits for PONs; and (2) probabilistic theory of BM-CDRs. More specifically, the following respective objectives demarcate the course of the research.

- **BM-CDR circuits for PONs:** Design, implementation, and application of novel BM-CDR circuit architectures for operation at high-speeds in multiaccess networks; and
- **Probabilistic theory of BM-CDRs:** Development of a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain.

1.4 Original Contributions

As will be elaborated upon in the forthcoming chapters, our contributions to these topics are all novel and have not been previously demonstrated. The evidence of our original scholarship to the overall existing body of knowledge of BM-CDRs is manifested by the 22 peer-reviewed publications that have so far resulted from the research presented in this thesis: journal articles [35–40] and conference proceedings [41–55] including two invited conference papers [43, 44].

1.4.1 BM-CDR Circuits for PONs

We demonstrate two novel BM-CDR architectures based on semiblind oversampling in both the time and space domain; that is, a hybrid combination of feedback (phase-tracking) and feed-forward. These BM-CDRs achieve error-free operation [bit error rate (BER) $< 10^{-10}$] while providing instantaneous (0 preamble bit) clock phase acquisition for any phase step

($\pm 2\pi$ rad) between successive bursts. Instantaneous phase acquisition can be used as follows: (1) improve the physical efficiency of the upstream PON traffic; (2) reduce the burst-mode sensitivity penalty; and (3) increase the effective throughput of the system by increasing the information rate. Our eloquent solution is to leverage the design of components for long-haul transport networks using low-complexity, commercial electronics providing a cost-effective solution for PON BM-CDRs. These components are typically a generation ahead of the components for multiaccess networks. Thus, our solution will scale with the scaling for long-haul networks.

BM-CDR Based on Semiblind Oversampling in Time Domain

- Design and implement a BM-CDR for PONs based on semiblind time domain oversampling. The BM-CDR is based on a phase-tracking CDR circuit operated at $2\times$ the bit rate and a CPA that makes use of a phase picking algorithm. We experimentally demonstrate the BM-CDR operation at 5 Gb/s.

- Experimentally demonstrate burst-mode reception at 5 Gb/s in a 20-km TDM gigabit ethernet PON (GE-PON) uplink. We carry out a detailed set of experiments to investigate the effect of silence period, including phase step and the length of consecutive identical digits (CIDs), between successive upstream PON bursts from independent ONUs, received signal power, and finite frequency offset between the sampling clock and desired bit rate, on the BER and packet loss ratio (PLR) performance of the BM-CDR. Consequently, we characterize the BM-CDR in terms of the phase acquisition time, CID immunity, burst-mode sensitivity penalty, dynamic range, and frequency acquisition range.

- Experimentally study burst-mode reception at 1.25 Gb/s in a 1300-km deployed fiber link that spans from Montreal to Quebec City and back. We investigate the effects of channel impairments on the performance of BM-CDR in terms of the PLR and BER, and quantify it as a function of the phase step between consecutive packets, received signal power, and CID immunity. We also assess the tradeoffs in preamble length, power penalty, and pattern correlator error-resistance. These results will help refine theoretical models of receivers employed in the optical packet switched networks (OPSNs), and provide input for establishing realistic power budgets.

- Experimentally investigate burst-mode reception at 622 Mb/s in a 7-user 20-km incoherent spectral amplitude-coded OCDMA (SAC-OCDMA) PON uplink. The receiver employed in this work is a variant of the BM-CDR based on semiblind time domain oversampling with a Reed-Solomon RS(255,239) forward-error correction (FEC) decoder. We consider two network architectures, namely, local sources (LS) and centralized LS (CLS), and study their relative merits in a two-feeder topology. The LS and CLS architectures are tested experimentally, and BER and PLR are measured. The immunity of the CDR in terms of CID is also measured. We simulate the BER with FEC in order to validate our measurements. We quantify the increase in soft capacity via FEC, while working with a nonideal recovered clock that provides realistic, achievable sampling.

- Develop a performance analysis approach and a practical measurement methodology to correctly and completely characterize any device under test (DUT) including synchronous optical network (SONET) CDRs, BMRx, BM-CDRs, and frequency synthesizers. This methodology is based on both BER and PLR measurements. In our burst-mode test setup, we can set the amplitude and relative phase of the packets, the preamble length, the length of CIDs, and control the received signal power. We characterize the proposed BM-CDR in terms of the phase acquisition time, burst-mode sensitivity penalty, frequency lock range, CID immunity, and dynamic range, while also assessing the tradeoffs in preamble length, burst-mode sensitivity penalty, and pattern correlator error resistance. We also propose two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition.

BM-CDR Based on Semiblind Oversampling in Space Domain

- Design and implement a BM-CDR for PONs based on semiblind space domain oversampling. The BM-CDR is based on a phase-tracking CDR circuit with multiphase clocks at the bit rate and a CPA that makes use of a novel phase picking algorithm. In contrast to the BM-CDR based on semiblind time domain oversampling, this BM-CDR uses electronics operated at the bit rate with *no a priori* knowledge of the packet delimiter, leading to a more efficient power consumption and being truly modular across application testbeds, respectively. We experimentally demonstrate the BM-CDR operation at 10 Gb/s.

- Experimentally show burst-mode reception at 2.5 Gb/s in a 20-km overlapped subcarrier-multiplexing (O-SCM) WDM PON uplink. The receiver employed in this work is a variant of the BM-CDR based on semiblind space domain oversampling.

1.4.2 Probabilistic Theory of BM-CDRs

We provide for the first time to our knowledge, a theoretical framework to model and analyze BM-CDRs. This coupled with the experimental results will refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets.

Theoretical Modeling of BM-CDRs

- Develop a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$-oversampling CDRs. The theoretical model quantitatively explains the performance of these circuits in terms of the BER and PLR. The model accounts for the following parameters: (1) silence periods, including phase steps and the length of CIDs between successive upstream PON bursts from independent ONUs; (2) finite frequency offset between the sampling clock and desired bit rate; (3) packet preamble length; (4) jitter on the sampling clock; and (5) pattern correlator error-resistance.

Theoretical Analysis of BM-CDRs

- Analyze quantitatively the performance of the proposed BM-CDRs by performing a comprehensive theoretical analysis. We evaluate the BER and PLR performance of the BM-CDRs to assess the tradeoffs between various parameters, and compare the results experimentally to validate the theoretical model. Specifically, we investigate the following: (1) effect of phase step between consecutive packets from independent ONUs; (2) effect of the packet preamble length; (3) effect of RMS jitter on the recovered sampling clock; (4) effect of pattern correlator error-resistance; and (5) effect of finite frequency offset between the local oscillator (LO) and desired bit rate.

1.5 Thesis Overview

Following this introductory chapter, the organization of the remainder of the thesis is as follows.

Chapter 2 provides the background necessary for the design and challenges of BMRx and BM-CDR circuits. We review existing BMRx solutions present in the literature, with the prime focus being on state-of-the-art BM-CDRs along with their respective shortcomings. Within this context, we propose our novel BM-CDR solutions.

In Chapter 3 we demonstrate two novel BM-CDR architectures based on semiblind oversampling in both the time and space domain. The architectures are based on a hybrid topology, composed of a feedback (phase-tracking) CDR and a feed-forward CPA. We detail the high-level architecture, the phase picking algorithm, and the hardware implementation of the proposed BM-CDRs. These BM-CDRs are designed to achieve error-free operation (BER $< 10^{-10}$) while featuring instantaneous (0 preamble bit) clock phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts.

In Chapter 4, we develop a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$ oversampling CDRs. The theoretical model quantitatively explains the performance of these circuits in terms of the BER and PLR. The model accounts for the silence periods, including phase steps and the length of CIDs between successive upstream PON bursts from independent ONUs, finite frequency offset between the sampling clock and desired bit rate, packet preamble length, jitter on the sampling clock, and the pattern correlator error-resistance.

Chapter 5 quantitatively analyzes the performance of our proposed BM-CDRs that are based on semiblind oversampling in either the time or space domain, with the probabilistic model developed in Chapter 4. More specifically, we perform a comprehensive theoretical analysis by investigating the BER and PLR performance of the BM-CDRs to assess the tradeoffs between the various parameters. In particular, we investigate the effect of phase step between consecutive packets from independent ONUs, the effect of the packet preamble length, the effect of RMS jitter on the recovered sampling clock, the effect of pattern correlator error-resistance, and the effect of finite frequency offset between the LO and desired bit rate.

In Chapter 6, we first verify the functionalities of the proposed BM-CDRs based on

semiblind time and space domain oversampling at the targeted bit rates of 5 Gb/s and 10 Gb/s, respectively. We also propose two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition. We then experimentally demonstrate and analyze the BM-CDR architectures in various optical test beds including: (1) 5 Gb/s TDM GEPON 20-km uplink; (1) 2.5 Gb/s O-SCM WDM PON 20-km uplink; 1.25 Gb/s 1300-km deployed fiber link spanning from Montreal to Quebec City and back; and 622 Mb/s in a 7-user incoherent SAC-OCDMA 20-km PON uplink. In particular, we validate the developed probabilistic theory of BM-CDRs with the experimental results, and study the effect of channel-impairments on burst-mode reception in these test beds. Furthermore, we note that these experimental expositions are designed to illustrate the application potential of these BM-CDRs—"a solution looking for problems".

Finally, the thesis is concluded in Chapter 7. We summarize and reiterate the central ideas in this work. We also give the direction for future work and other research opportunities.

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Chapter 2

Review of the State of the Art

2.1 Introduction

THIS chapter forms the background necessary for the design and challenges of burst-mode receiver (BMRx) circuits and burst-mode clock and data recovery (BM-CDR) circuits. We review existing BMRx solutions present in the literature, with the prime focus being on state-of-the-art BM-CDRs along with their respective shortcomings. Within this context, we will propose our novel BM-CDR solutions in the next chapter.

The chapter is organized as follows. In Section 2.2, we provide a primer on optical receivers. Section 2.3 clarifies what burst-mode data is, and illustrates the differences between conventional receivers and burst-mode receivers. The challenges and design of BMRx circuits together with the different architectures is presented in Section 2.4. In Section 2.5, we detail the problem of clock and phase recovery, and present the state-of-the-art solutions with their respective shortcomings. Section 2.6 gives a brief overview on the probabilistic theory of burst-mode reception.

2.2 A Primer on Optical Receivers

A general anatomy of an optical receiver is shown in Fig. 2.1. An optical receiver has two distinct blocks: a front-end and a clock and data recovery circuit.

The main function of the front-end is to perform optical-to-electrical (OE) conversion of the data signal. This is achieved by the photodiode that converts the received optical signal into an electric current. The detector is followed by a low-noise high bandwidth

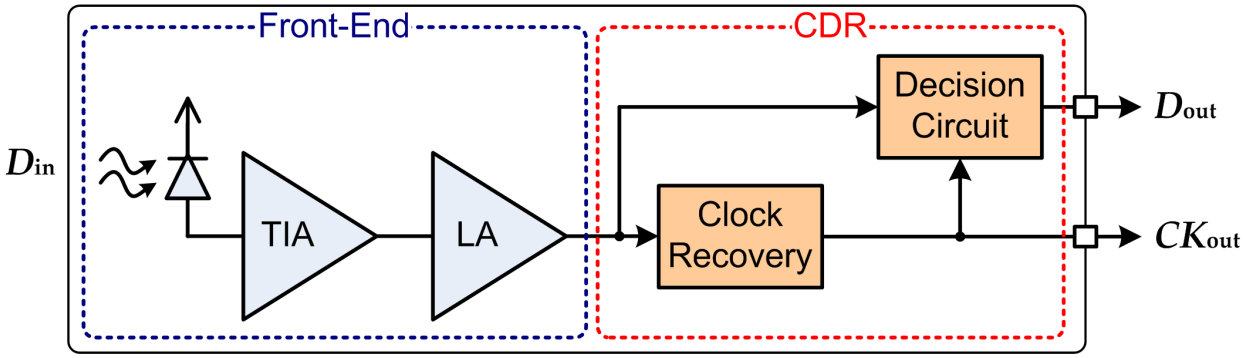

Fig. 2.1 General anatomy of an optical receiver (TIA: transimpedance amplifier; LA: limiting amplifier).

transimpedance amplifier (TIA) that converts the current into a voltage with a swing large enough for the proceeding blocks. The sensitivity of the photodiode can be increased by widening its light reception window [1]. However, this complicates the design of the high-bandwidth receiver, as the parasitic capacitance of the photodiode increases. This implies that the receiver sensitivity trades off with its bandwidth. The limiting amplifier (LA) increases the voltage swings to provide logic levels, while isolating its proceeding synchronous stages from the TIA. The clock feedthrough of the synchronous circuits to the sensitive TIA can heavily corrupt the data signal [2].

The data stream received and amplified by the front-end is both asynchronous and noisy. For subsequent processing, timing information—a clock—must be extracted from the data so as to allow synchronous operation. Furthermore, the data must be "retimed"such that the jitter accumulated during transmission is removed. The task of clock extraction and data retiming is called clock and data recovery (CDR). The core of the receiver is the CDR circuit. CDR circuits must satisfy stringent specifications defined by optical standards, presenting difficult challenges to system and circuit designers [2].

As illustrated in Fig. 2.2(a), a clock recovery circuit senses the data D_{in}, and produces a periodic clock CK_{out}. A decision circuit driven by the clock then retimes the data, that is, it samples the noisy data, yielding an output with less jitter. Note that the zero crossings of the received data are corrupted by noise and jitter whereas those at the decision circuit output area are as "clean" as the recovered clock itself. This removal of timing errors forms the essence of data retiming.

The signal-to-noise ratio (SNR) is dependent on the choice of the sampling instance if a

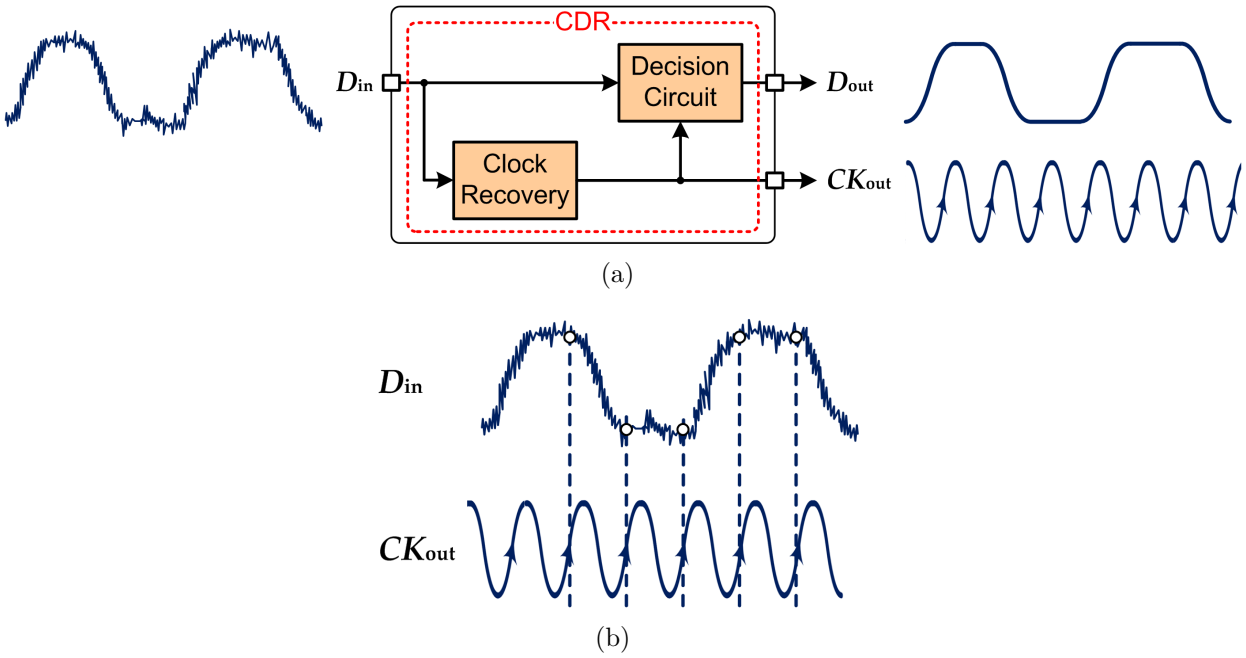

Fig. 2.2 Concept of clock and data recovery [2]. (a) Role of a CDR in retiming data. (b) Optimum sampling of noisy data.

single pulse is to be detected in the presence of additive noise and intersymbol interference (ISI). As exemplified Fig. 2.2(b), the output SNR is high if sampling is synchronized such that the peak value of the pulse is sensed. Synchronized sampling requires two important conditions to be simultaneously satisfied by the clock generated by the CDR. First, the clock must have a frequency equal to the data rate; that is, a data rate of 10 Gb/s with each bit 100 ps wide, translates to a clock frequency of 10 GHz with a period of 100 ps. Second, the clock must bear a certain phase relationship with respect to data, allowing optimum sampling of the bits by the clock. If the rising edge of the clock falls in the midpoint of each bit, then: (1) the signal level difference between logical ONE and logical ZERO is the largest, improving the SNR of the receiver; and (2) the sampling occurs the farthest from the preceding and following data transitions, providing maximum margin for jitter and other timing uncertainties.

To summarize, the front-end directly impacts both the sensitivity and the speed of the overall system. This is due to the noise, gain, and bandwidth of the TIA and the LA, and the non-idealities introduced by the photodiode. The CDR must provide high data rates, tolerate long runs of ONEs and ZEROs known as consecutive identical digits (CIDs), and

satisfy jitter and bandwidth.

Today's standard optical receivers are designed to recover data from point-to-point (P2P) optical links, which are digital in nature and use on-off keying (OOK)—binary modulation to represent digital data as the presence or absence of a carrier wave. In OOK, a binary ONE is represented as the presence of a carrier for a specific duration while a binary ZERO is represented by the absence of the carrier for the same duration. Although attractive for its simplicity, OOK is not spectrally efficient due to the abrupt changes in amplitude of the carrier wave [3]. This discussion will be detailed in Section 2.5.1.

Optimum bandwidth efficiency is achieved by massively multiplexing data from many sources by means of time-division multiplexing (TDM) or wavelength-division multiplexing (WDM). The synchronicity and network topology of P2P networks underline their three main characteristics namely: (1) continuous transmission of data; (2) same source used to generate data transmitted over the link; and (3) same link used for data communication. The first characteristic gives the continuous wave nature to the optical data seen by the receiver, while the latter two give the received data two distinct features making it continuous mode.

Since the data is generated by the same source, it is consistent in phase from bit-to-bit and the transmitted power at the source is the same for all data. Furthermore, as the data travels over the same optical link, the data undergoes the same amount of attenuation (or amplification). Also, the data undergoes equal delay over the link so that the phase of the received data never varies significantly. The overall outcome of these effects leads to: (1) the data having the same optical power levels at the receiver indicating a logical ONE or a logical ZERO—no amplitude variations; and (2) the data not having any phase variations. Given these two characteristics, conventional optical receivers are optimized by design for specific power levels and phase.

2.3 Conventional versus Burst-Mode

We now clarify what burst-mode data is, and illustrate the differences between conventional receivers and burst-mode receivers.

2.3.1 Continuous Mode

Continuing the discussion from Section 1.2, in passive optical networks (PONs), the downstream direction network from the optical line terminal (OLT) to the optical network units (ONUs) is P2P. Continuous data is broadcast from the OLT to the ONUs. As shown in Fig. 2.3, data in continuous mode signal format is a binary sequence with an approximately balanced ratio of ONEs and ZEROs. Here, the sequence has the same amplitude for the same logic symbols and the interval between any two logic transitions is strictly limited. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous mode integrated circuits (ICs).

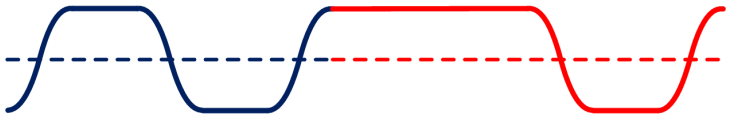

Fig. 2.3 Continuous mode PON traffic in downstream direction.

In a conventional receiver, ac coupling is used. The ac-coupled circuitry can provide high sensitivity for the receiver. However, because of the charging and discharging time of the capacitors associated with the ac-coupled signal path, the average amplitude of the received data is not allowed to vary rapidly with time [4]. Therefore, conventional receivers are only suitable for continuous mode data reception.

2.3.2 Burst-Mode

The challenge in the design of a chip set for PONs comes from the upstream data path. In the upstream direction, the network is point-to-multipoint (P2MP). Multiple ONUs transmit data to the OLT in the central office (CO). Because of optical path differences in the upstream path, the data is bursty in nature. As depicted in Fig. 2.4, the difference between the signal amplitude ΔA, may vary from packet to packet, and there is no restriction on the intervals between the logic transitions, that is, silence periods consisting of the phase steps $\Delta\varphi$. A guard time is usually inserted between the successive packets. The amplitude and phase of successive packets may vary anywhere between 0 to 20 dB [5] and -2π to $+2\pi$ rad [6], respectively.

Consequently, to deal with bursty data, the receiver at the OLT is responsible for amplitude and phase recovery, which must be achieved at the beginning of every packet.

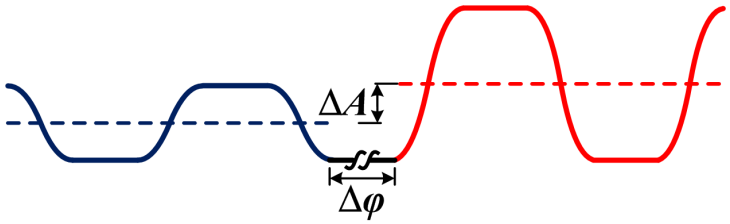

Fig. 2.4 Burst-mode PON traffic in upstream direction.

At the front-end of the receiver is a BMRx responsible for amplitude recovery [7–22] as shown in Fig. 2.5. Phase acquisition is then performed by a BM-CDR [5,6,23–38] with the help of a clock phase aligner (CPA) as illustrated in Fig. 2.6.

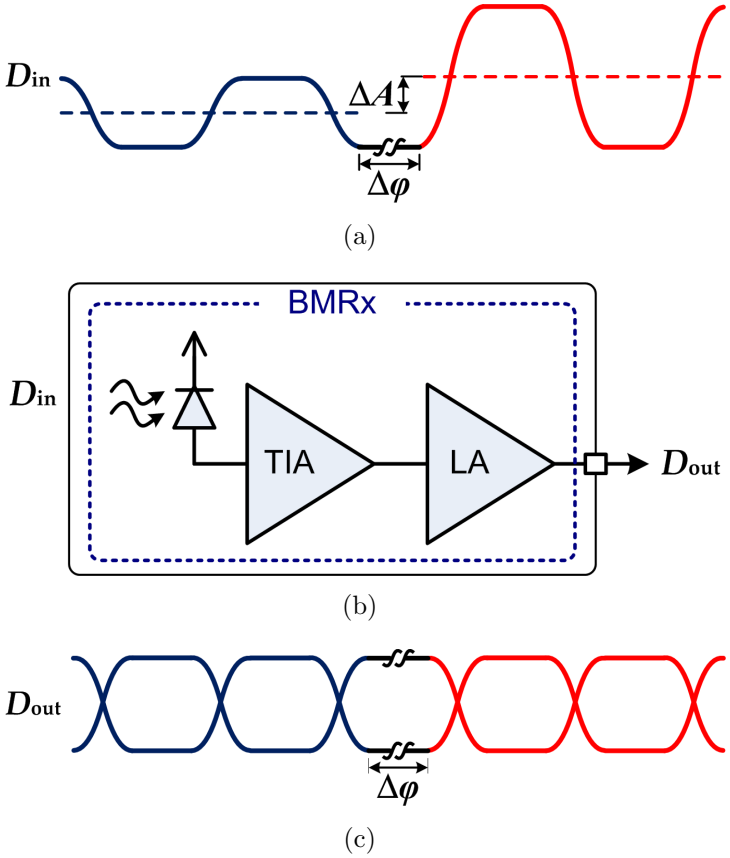

Fig. 2.5 BMRx handling the task of amplitude recovery. (a) Input signal with varying amplitude and phase (burst-mode traffic). (b) General anatomy of a BMRx. (c) Output signal with amplitude recovery (BMRx: burst-mode receiver; TIA: transimpedance amplifier; LA: limiting amplifier).

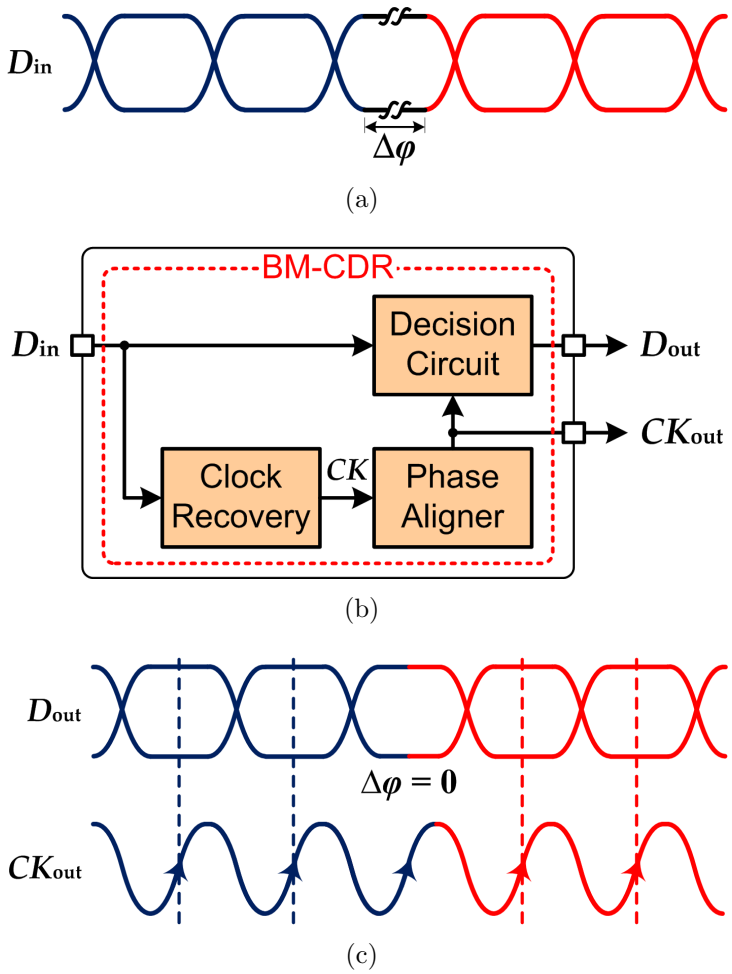

Fig. 2.6 BM-CDR handling the task of phase recovery. (a) Input signal with varying phase. (b) General anatomy of a BM-CDR. (c) Output signal with phase recovery (BM-CDR: burst-mode clock and data recovery).

The operation of a BMRx is very different from a conventional receiver. The main difference is that the BMRx is dc-coupled and the threshold setting of the circuitry must adapt to the amplitude of the received signal in a very short time. Second, the most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible. Table 2.1 summarizes the differences between conventional receivers and burst-mode receivers.

Table 2.1 Comparison of conventional receivers and burst-mode receivers [4]

	Conventional	Burst-mode
Signal Coupling	ac	dc
Threshold setting	Fixed	Adaptive
Amplitude and clock recovery	μs	ns
Access time for receiver	μs	ns

2.4 Burst-Mode Receivers

In order for PONs to be successful economically, they must provide a large splitting factor (i.e. the number of subscribers served by a single PON) and a long physical reach (i.e. the distance between the CO and the subscribers). The development of a BMRx is therefore aimed at providing a high sensitivity and a wide dynamic range. These two performance characteristics determine the physical reach and the splitting ratio of the PON, respectively. When the BMRx uses dc coupling, another aim is to minimize the burst-mode sensitivity penalty.

DC-coupled BMRx exhibit two sources of sensitivity penalty when compared to conventional receivers. First, the extracted decision threshold is noisy, giving rise to sensitivity penalty. This penalty, which can range from a few tenths of decibels up to a few decibels (dBs) [39], was studied extensively in [40–42]. A second sensitivity penalty stems from unavoidable dc offsets. The penalty due to a fixed dc off offset was studied in [42], while the penalty due to random dc offsets was studied in [39].

The main challenges in the design of a BMRx can be summarized as follows:

- Optimizing the avalanche photodiode (APD) factor for achieving both high sensitivity and wide dynamic range is not straightforward. The fast succession of upstream bursts does not allow for a change of the APD gain between bursts.

- The receiver must provide fast but accurate threshold settings on individual incoming packets to perform dynamic level detection and amplitude recovery.

- The receiver must quickly extract the decision threshold within a preamble length of a few bytes at the beginning of each packet.

- Due to the short guard time, the burst-mode receiver needs an active reset to erase the threshold of a preceding packet [19].
- As small amounts of optical power may be present during the guard time, it is difficult to distinguish between transmitted ZEROs and the dark level during the guard time. Therefore, the receiver cannot know precisely when a packet ends, and an external reset signal is necessary to signal the end of a packet.
- A power level measurement circuit must be integrated, which allows the OLT to tell a specific ONU to either increase or decrease its launched power.

2.4.1 BMRx Architectures

The bit error rate (BER) performance of all BMRx can be characterized by using only two parameters, namely, the rise time constant and the holding time constant of the adaptive threshold detection circuit. In literature, BMRx have been classified according to the way the threshold is set. The first type is that the receiver threshold is determined completely from the preamble field and held constant in the data field [40, 41]. These BMRx have a finite rise time constant and an infinite holding time constant. The second type is that the receiver threshold is adaptively determined according to the input signal [20–22]. Here, the BMRx have a small rise time constant but a finite holding time constant. BMRx can further be divided into two types according to their structures: (1) feedback architectures [20]; and (2) feed-forward architectures [40]. In general, feedback architectures are more stable than the feed-forward architectures, since the feedback loop enables the BMRx to work more reliably, but a differential input/output preamplifier is needed. In feed-forward architectures, a conventional dc-coupled preamplifier can be used in the BMRx. However, the circuitry needs to be carefully designed to prevent oscillations in the BMRx. We briefly describe these two architectures.

BMRx Based on Feedback Architecture

Fig. 2.7(a) shows a BMRx based on feedback architecture. This BMRx uses a differential input/output TIA with a peak detection circuit forming a feedback loop. The peak detector circuit determines the instantaneous detection threshold for the incoming signal. The output of the TIA or preamplifier is dc-coupled to a differential LA or postamplifier for

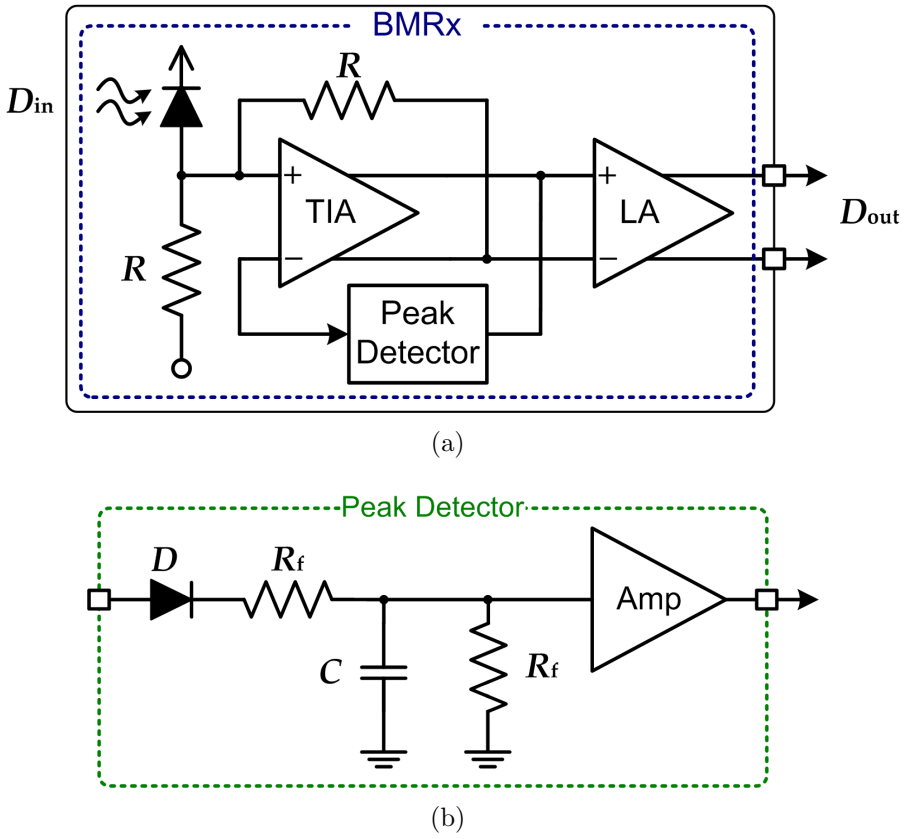

Fig. 2.7 (a) Feedback type BMRx. (b) Peak detection circuitry (TIA: transimpedance amplifier; LA: limiting amplifier).

further amplification. In this scheme, the amplitude recovery of the signal is done in the TIA.

BMRx Based on Feed-forward Architecture

Fig. 2.8 shows a BMRx based on feed-forward architecture. This BMRx employs a conventional dc-coupled TIA. The received signal is first amplified by this TIA or preamplifier, and then split into two branches. The first branch of the output from the TIA is dc-coupled to a differential LA or postamplifier. The second branch is fedforward into a peak detection circuitry to extract the amplitude information of received packets. From the output of the peak detector, the proper threshold level can be set in front of the differential amplifier. At the output of the LA, the amplitude-recovered data packet is ready for further processing.

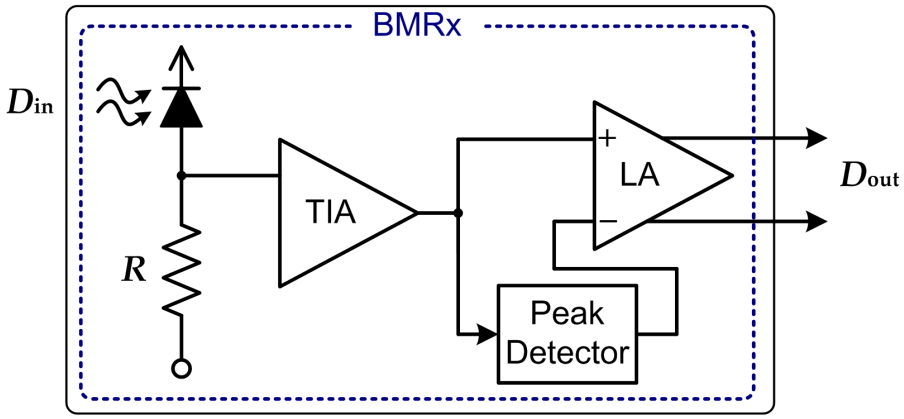

Fig. 2.8 Feed-forward type BMRx (TIA: transimpedance amplifier; LA: limiting amplifier).

2.5 Burst-Mode Clock and Data Recovery

The BM-CDR is the core of an optical receiver for PON (burst-mode) applications. The most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible. We note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [40,42]. However, by reducing the phase acquisition time—and therefore the length of the CPA field—more bits are left for amplitude recovery, thus reducing the burst-mode sensitivity penalty. Alternatively, with the reduced number of preamble bits, more bits can be left for the payload, thereby increasing the information rate. Instantaneous phase acquisition also has a significant improvement impact in the physical efficiency of the upstream PON traffic.

The main building blocks of a BM-CDR include a clock recovery circuit followed by a CPA. We first present the problem of clock recovery and address the problem with nonlinear architectures. We then discuss the problem of phase recovery and present the state-of-the-art solutions with their respective shortcomings. Against this backdrop, we present our solution moving to the next chapter.

2.5.1 Problem of Clock Recovery

PON systems employ a simple binary amplitude modulation data format—non-return to zero (NRZ)—for ease of detection. Random NRZ data has characteristic properties that

directly influence the design of clock recovery circuits. In general, a random binary sequence can be represented by

$$x(t) = \sum_{k=-\infty}^{+\infty} b_k \cdot p(t - kT_{\text{sym}}) \tag{2.1}$$

where $p(t)$ denotes the symbol pulse shape, T_{sym} is the duration of one symbol, and the set $\{b_k\}$ is the set of random data. For a random binary NRZ sequence, the pulse shape $p(t)$, is given by [46]

$$p(t) = \prod\left(\frac{t}{T_b}\right) \tag{2.2}$$

where $T_{\text{sym}} = T_b$ is the time that it takes to send 1 bit, that is, the bit period. The amplitude of $p(t)$ given by b_k depends on the k^{th} bit as

$$b_k = \begin{cases} 0, & \text{if } k^{\text{th}} \text{ bit is logical ZERO} \\ +A, & \text{if } k^{\text{th}} \text{ bit is logical ONE.} \end{cases} \tag{2.3}$$

If A is selected so that the normalized average power of the NRZ signal is unity, then $A = \sqrt{2}$. Assuming the data with equiprobable ONEs and ZEROs, the power spectral density (PSD) $S_x^{\text{NRZ}}(f)$, of the NRZ data sequence $x(t)$ is given by

$$S_x^{\text{NRZ}}(f) = \frac{1}{2T_b}|P(f)|^2 \tag{2.4}$$

where $P(f)$ represents the Fourier transform (FT) of the pulse shape $p(t)$, and can be expressed as

$$\begin{aligned} P(f) = \mathcal{F}\left[p(t)\right] &= \int_{-\infty}^{+\infty} \left[p(t)\right] \exp\left(-j\pi f t\right) dt \\ &= T_b \frac{\sin(\pi f T_b)}{\pi f T_b} \end{aligned} \tag{2.5}$$

where $\mathcal{F}[\cdot]$ denotes the FT of $[\cdot]$ and f is the frequency parameter with units of Hz (i.e. $1/s$). Thus, the PSD for the NRZ data sequence $S_x^{\mathrm{NRZ}}(f)$, can be expressed as

$$S_x^{\mathrm{NRZ}}(f) = \frac{T_b}{2}\left[\frac{\sin(\pi f T_b)}{\pi f T_b}\right]^2 \tag{2.6}$$

This analysis yields an important attribute of NRZ data. As depicted in Fig. 2.9, the spectrum of the NRZ data at a bit rate of $1/T_b$, exhibits no spectral component (nulls) at integer multiples of the bit rate frequency $f = n/T_b, n = 1, 2, \ldots$. This implies that a clock recovery circuit can lock to these spurious signals instead of the bit rate frequency or not at all. Furthermore, a linear time-invariant (LTI) operation cannot extract a periodic clock from this data [2]. However, the information about the frequency of the data can be extracted from the spacing between the data transitions. These transitions appear as the rising and falling edges of the data signal. Thus, a nonlinear function, for example, edge detection may be used to recover the clock. Edge detection may be performed with a feed-forward technique or with a feedback technique. Feed-forward techniques lead to open-loop architectures, whereas feedback techniques lead to phase-locking architectures. Although our proposed BM-CDRs are built on the latter approach, we briefly describe the open-loop architectures as the foundation of the phase-locking architectures.

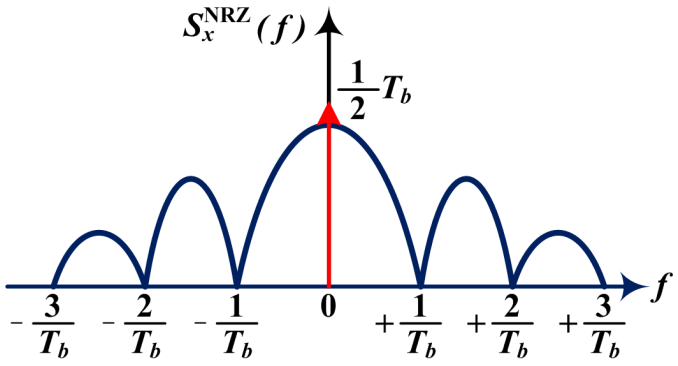

Fig. 2.9 Power spectral density of NRZ data in logarithmic scale (NRZ: non-return to zero).

Open-Loop Architecture

Feed-forward methods are generally comprised of a nonlinear element in front of the signal for generations of the spectral lines at the clock frequency followed by a very high-quality

filter to extract the clock. Edge detection is performed by a logical XOR operation. Fig. 2.10 depicts the structure of an edge detector that consists of an XOR gate operating on the input data D_{in}, and its delayed replica $\widehat{D}_{\text{in}}$. Theoretical derivations indicate that the highest degree of harmonic suppression can be achieved if these two waveforms are spaces within half a bit period from each other [2].

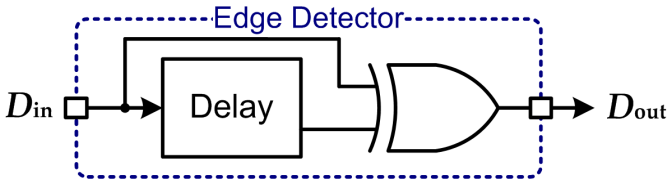

Fig. 2.10 Edge detection using an XOR gate.

As shown in Fig. 2.11, the clock signal can be recovered from the edge-detected waveform by passing through a band-pass filter (BPF) tuned to the clock frequency. In order to reduce jitter on the recovered clock signal, the filter should have a very high selectivity to suppress the unwanted data-dependent signal that results in amplitude and phase modulation. The recovered clock is then fed to the phase aligner to ensure that the output clock signal CK_{out}, samples the data at its optimum point in the D flip-flop (D-FF) yielding an output D_{out}. As such the D-FF is called a decision circuit.

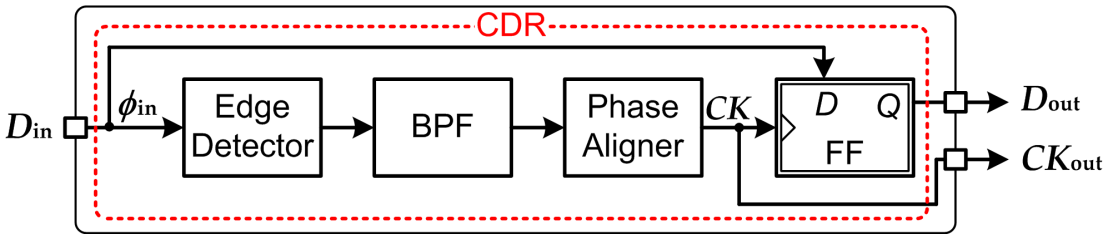

Fig. 2.11 Block diagram of an open-loop CDR architecture (BPF: band-pass filter; FF: flip-flop).

Although the low complexity associated with open-loop architectures makes them attractive, there are two main associated drawbacks with this architecture. Firstly, this technique provides limited phase tracking ability and therefore poor jitter tolerance. Secondly, the integration of highly selective BPFs operating at very high frequencies is not practical using available fabrication processes. This limitation calls for off-the-chip implementation.

However, these external filters suffer from high loss and the latency, which limiting their applicability to few a GHz operation.

Phase-Locking Architecture

Fig. 2.12 shows a block diagram of a conventional CDR circuit that senses data D_{in}, and produces a periodic clock CK_{out}. This phase-tracking CDR employs feedback, a phase-locked loop (PLL), to keep the recovered clock CK, in phase with the clock embedded in the received data. More specifically, the CDR is composed of a phase detector (PD), a charge pump (CP), a low-pass filter (LPF), a voltage-controlled oscillator (VCO), and a D-FF. The PD is responsible for detecting the phase difference $\Delta\phi = \phi_{\text{in}} - \phi_{\text{osc}}$, between the center of the incoming data eye and the data-sampling clock. Depending on the phase difference, $\Delta\phi > 0$ rad (data leads clock) or $\Delta\phi < 0$ rad (data lags clock), the PD generates up (U), or down (D), signals respectively, for the charge-pump. The charge-pump then supplies the LPF with charge according to these signals. The filtered charge via the loop filter becomes the VCO control voltage, and either speeds up or slows down the clock, hence, determining the frequency and phase of the sampling recovered clock. The generated clock signal CK, is then used to drive the D-FF that retimes the data D_{in}; that is, it samples the noisy data, yielding an output D_{out}, with less jitter. As the incoming data is regenerated, its additive noise and ISI is suppressed while the amplitude is significantly amplified.

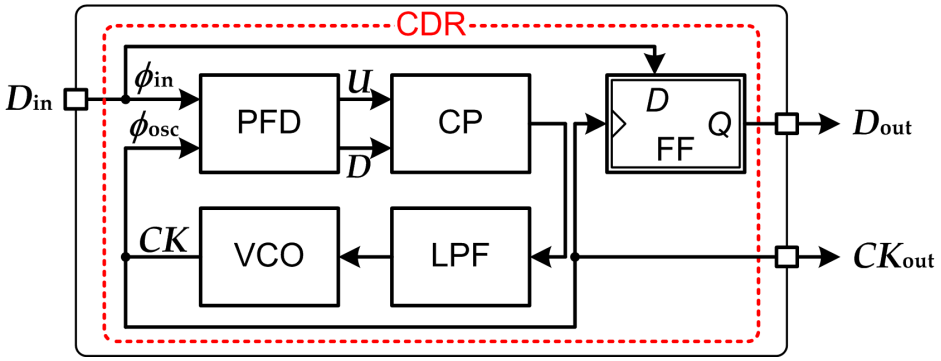

Fig. 2.12 Block diagram of a phase-locking CDR architecture (CP: charge pump; FF: flip-flop; LPF: low-pass filter; PD: phase detector; VCO: voltage-controlled oscillator).

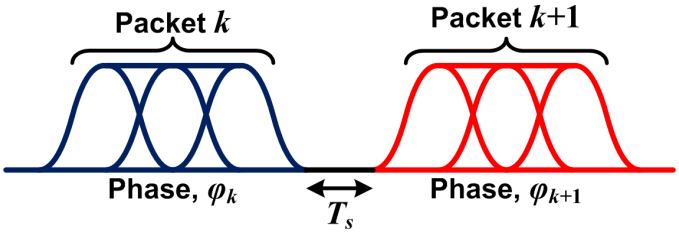

Fig. 2.13 Upstream PON traffic depicting the silence period between two successive bursts from independent ONUs.

2.5.2 Problem of Phase Acquisition

Moving forward, we next address the problem of phase acquisition. Under ideal conditions, with no ISI or clock jitter, error-free data recovery is achieved when the received data is sampled within half a bit period of the nominal sampling point. If the CDR is operated at the bit rate, the ideal sampling point is in the center of the data eye. In terms of the input clock phase ϕ_{in}, and the recovered clock phase ϕ_{osc}, the condition for error-free data recovery is expressed as

$$|\phi_{\text{in}} - \phi_{\text{osc}}| < \pi \ \text{ rad}\,. \tag{2.7}$$

Fig. 2.13 depicts the silence period T_s, between two successive bursts from independent ONUs, and can be expressed as

$$T_s = \left(m + \frac{\Delta\varphi}{2\pi}\right) T_b \tag{2.8}$$

where m an all-zero sequence, is the number of CIDs, and

$$|\Delta\varphi| = |\varphi_{k+1} - \varphi_k| \leq 2\pi \ \text{ rad} \tag{2.9}$$

represents the phase step that arises due to optical path differences between the consecutive k^{th} and $(k+1)^{\text{th}}$ packet. At the OLT, assuming that the CDR circuit is already in phase-lock ($\Delta\phi = 0$ rad) by the end of the k^{th} packet, the resulting input phase step to the CDR by the arrival of the $(k+1)^{\text{th}}$ packet is given as

$$\phi_{\text{in}} = \Delta\varphi \cdot u(t), \ \text{ for } \ t > 0 \tag{2.10}$$

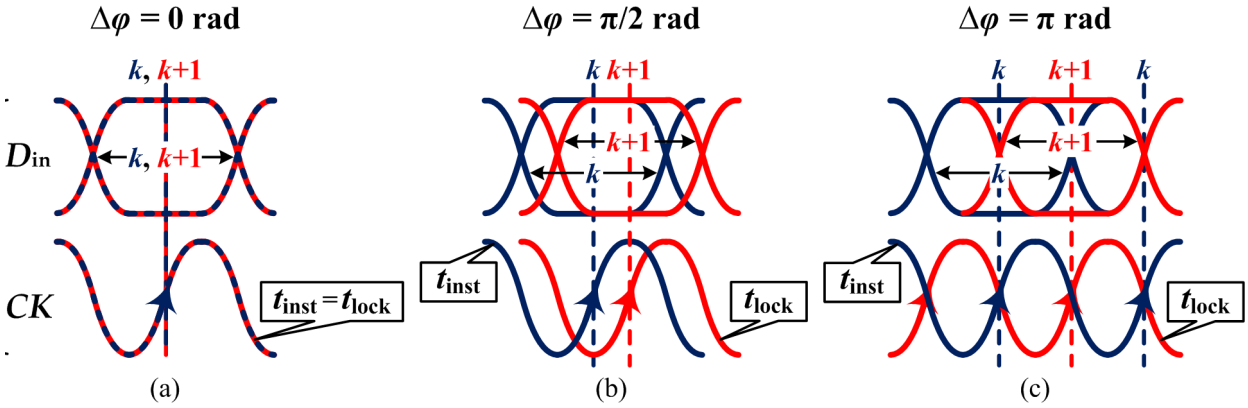

Fig. 2.14 Response of the conventional CDR to bursty traffic (consecutive packets with a phase step). Three different phase steps are considered: (a) $\Delta\varphi = 0$ rad; (b) $\Delta\varphi = \pi/2$ rad; and (c) $\Delta\varphi = \pi$ rad.

where

$$u_t = \begin{cases} 0, & \text{if } t > 0 \\ 1, & \text{if } t < 0. \end{cases} \tag{2.11}$$

is a unit step function. Fig. 2.14 shows the response of the CDR to bursty traffic. The input phase step will result in the instantaneous clock t_{inst}, in-phase with the last bit of the k^{th} packet, to be out-of-phase by $|\Delta\varphi| \leq 2\pi$ rad with the first bit of the $(k+1)^{\text{th}}$ packet. This asynchronous and inevitable presence of phase steps between the received consecutive packets can cause conventional CDRs to lose pattern synchronization. Preamble bits l, can be inserted at the beginning of each packet to allow the CDR feedback loop function[1]

$$\eta(l) = \frac{\phi_{\text{osc}}}{\phi_{\text{in}}} \tag{2.12}$$

enough time to settle down and thus acquire lock; that is, align the instantaneous clock t_{inst}, to the lock state t_{lock}, so as to sample in the middle of the data bit:

$$\lim_{\eta(l)\to 1} t_{\text{inst}} = t_{\text{lock}}. \tag{2.13}$$

However, the use of a preamble introduces overhead, reducing the effective throughput

[1]For a CDR based on a second-order PLL, $\eta(l)$ is analytically expressed in Chapter 4.

and increasing delay. The most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible to decrease the burst-mode sensitivity penalty and thus increase the power budget or alternatively increase the information rate with more bits available to the packet payload. We define the lock acquisition time as the number of preamble bits l, needed to achieve error-free operation. With the proposed BM-CDR architectures discussed next in Chapter 3, it will be demonstrated theoretically (in Chapter 4) and experimentally (in Chapter 6), that using the instantaneous clock t_{inst}, for sampling suffices for error-free data recovery for any phase step $|\Delta\varphi| \leq 2\pi$ rad between two consecutive packets. Hence, there is no need for a preamble field ($l = 0$), demonstrating instantaneous phase acquisition.

2.5.3 Prior Art

We now present the state-of-the-art solutions with their respective shortcomings. PONs have no repeaters in their data path unlike synchronous optical network (SONET) systems that impose a strict specification on jitter transfer. Jitter transfer refers to the suppression of the input jitter through the CDR circuit. Taking this into account, different approaches have been proposed to build BM-CDRs for PON applications by compromising the jitter transfer characteristics. These BM-CDRs are based on: (1) broad-band PLLs [6, 23]; (2) injection-locking techniques [24,25]; (3) gated VCOs (GVCOs) [5, 26–32]; (4) oversampling CDRs without phase-tracking—blind oversampling [33–35]; and (5) hybrid combination of phase-tracking and blind-oversampling CDRs—semiblind oversampling [36–38]. These solutions broadly fall into three categories: (1) feedback architectures; (2) feed-forward architectures; and (3) hybrid architectures—combination of feedback and feed-forward. Table 2.2 classifies the current state of the art BM-CDR solutions within these configurations.

BM-CDRs Based on Broad-band PLLs

In the first approach, BM-CDRs based on broad-band PLLs trade-off the loop-bandwidth of the PLL for fast phase acquisition time and large frequency capture range [6]. The disadvantages include stability issues, jitter peaking, and limited jitter filtering. If additional control logic or a reset signal is acceptable, then a work around consists in using a dynamic loop bandwidth. The bandwidth is increased while the CDR acquires lock and is restored

Table 2.2 BM-CDR Solutions Based on Feedback, Feed-forward, and Hybrid Architectures

Architecture	Solution	References
Feedback	Broad-band PLLs	[6, 23]
	Injection locking	[24, 25]
Feed-forward	Gated VCOs	[5, 26–32]
	Blind-oversampling	[33–35]
Hybrid	Semiblind oversampling	This work and [36–38]

to its original value for the rest of the packet to minimize output jitter [23].

BM-CDRs Based on Injection-Locking

The second approach is based on injection-locking technique that extracts the clock by injection locking the local oscillator (LO) to the tiny embedded clock signal, which primarily arises from leakage coupling [24, 25]. Fig. 2.15 illustrates the working principle. This design suffers from severe performance degradation, as the natural frequency of the VCOs deviates from the data rate due to process, temperature, and supply variations (PVT). This consequently limits their frequency tracking range.

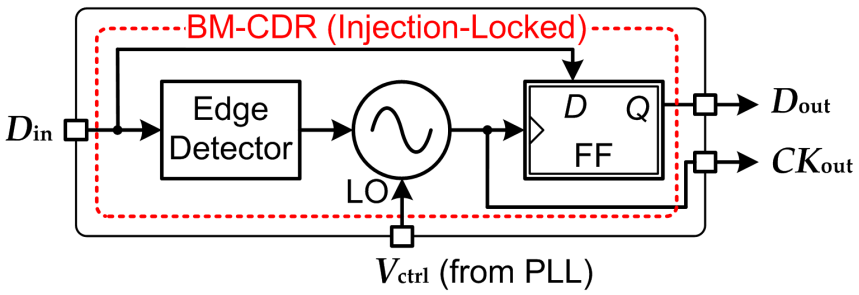

Fig. 2.15 Generic architecture of BM-CDRs based on injection-locking.

BM-CDRs Based on Gated VCOs

In the third approach, the BM-CDRs are built from GVCO or some kind of gating circuit as shown in Fig. 2.16. The approach was first proposed in [26] and then used in [5, 27–31]. These BM-CDRs perform clock phase alignment by triggering a local clock on each

transition of the input data. This solution provides rapid phase locking but results in higher phase noise as it does not filter out input jitter [4]. More seriously, the gating behavior would cause momentary fluctuation on the recovered clock, potentially incurring undesired jitter and ISI. In addition, the truncation or prolongation of the clock cycle during phase alignment induces other uncertainties such as locking (settling) time. A jitter rejection method was proposed in [32], but involved complex circuits.

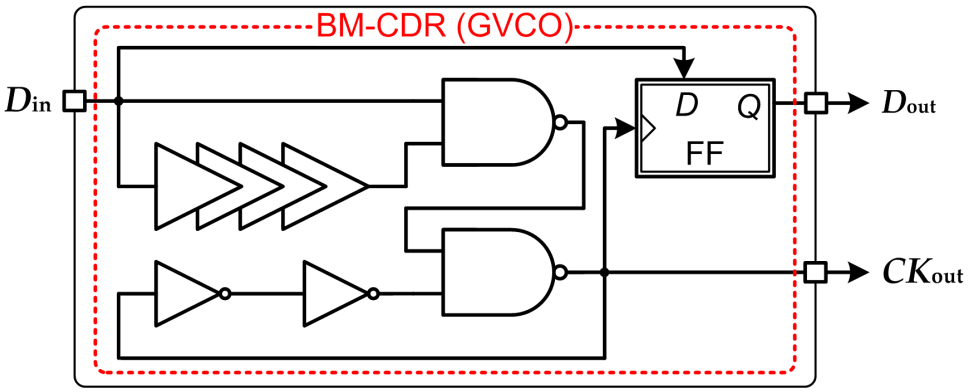

Fig. 2.16 Generic architecture of BM-CDRs based on gated VCO.

BM-CDRs Based on Oversampling

Fig. 2.15 depicts the last approach; that is BM-CDRs based on oversampling without or with phase-tracking, that is, blind oversampling [33–35] or semiblind oversampling [36–38], respectively. One can either oversample in time using a clock frequency higher that the bit rate, or oversample in space using a multi-phase clock with a frequency equal to the bit rate. Oversampling in time requires faster electronics, whereas oversampling in space requires low skew between multiple phases of the clock. The oversampling techniques, in general, suffer from high complexity and power consumption. The key advantage of the semiblind oversampling technique is that it produces a jitter tolerance, equal to the product of the phase-tracking jitter tolerance and the blind oversampling jitter tolerance, thereby increasing the low-frequency jitter tolerance. Note that jitter tolerance of the CDR refers to the peak-to-peak amplitude of sinusoidal jitter (as function of frequency) that can be applied at the input without causing data recovery errors. Our proposed BM-CDRs are

based on the semiblind oversampling[2] technique.

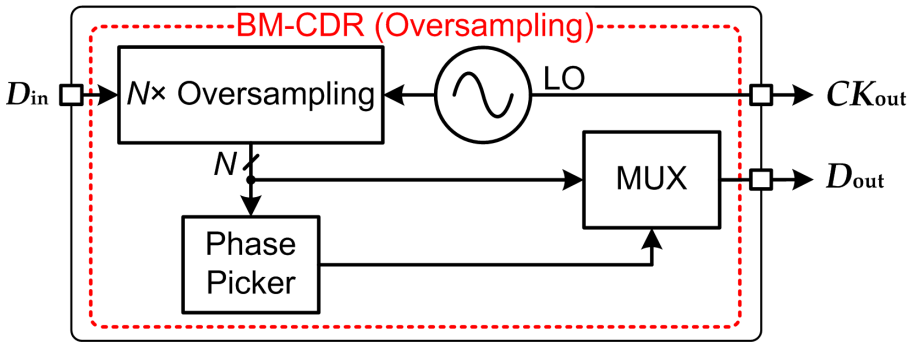

Fig. 2.17 Generic architecture of BM-CDRs based on oversampling.

Summary

Table 2.4 summarizes the performance of the current state of the art BM-CDRs reported in literature. In comparison, the PON standards are summarized in Table 2.3.

Table 2.3 Summary of PON standards

	GEPON [43]	**GPON [44]**	**10-GEPON [45]**
Data Rate	1.25 Gb/s	2.488 Gb/s	10 Gb/s
BER	$< 10^{-10}$	$< 10^{-10}$	$< 10^{-10}$
PLR	N/A	N/A	N/A
Phase Acquisition Time	540 bits	44 bits	964 bits
Frequency Lock Range	N/A	N/A	N/A

[2]For the sake of brevity, we will refer to semiblind oversampling as oversampling, unless otherwise explicitly stated. This is to differentiate it from blind oversampling.

2.6 Probabilistic Theory of Burst-Mode Reception

Random noise which is always present at the BMRx front-end affects the determination of the decision threshold and introduces sensitivity penalty. A sensitivity penalty using Gaussian noise statistics for BMRx using PIN photodiodes was first addressed in [40]. A more accurate model is provided in [41], while a unified theory which includes the interaction of Gaussian noise with the finite charging/discharging time of the adaptive threshold detection circuitry is derived in [4]. In [39], the influence of random dc offsets on the sensitivity of BMRx is analyzed. For BMRx employing APDs, where Gaussian approximation becomes unreliable, a sensitivity penalty analysis is detailed in [42]. While there has been an appreciable amount of research on the theory of BMRx front-end circuits in literature, virtually no attention has been paid to the probabilistic theory of BM-CDRs.

Table 2.4 Performance summary of the current state of the art BM-CDRs

BM-CDR Solution	**Broad-band PLL**	**Injection locking**	**Gated VCOs**			**Oversampling**
	[6]	**[25]**	**[27]**	**[28]**	**[29]**	**[47]**
Data Rate	2.488 Gb/s	10.3 Gb/s	10.3 Gb/s	10 Gb/s	10 Gb/s	10.3 Gb/s
BER	N/A	$< 10^{-12}$	$< 10^{-12}$	N/A	$< 10^{-12}$	$< 10^{-3}$
PLR	N/A	N/A	N/A	N/A	N/A	N/A
Phase Acq. Time	100 bits	N/A	1 bit	32 bits	5 bits	1 bit
Freq. Lock Range	N/A	160 MHz	N/A	N/A	N/A	N/A
CID Tolerance	32 bits	N/A	160 bits	7 bits	31 bits	N/A

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Chapter 3

Novel BM-CDR Architectures

3.1 Introduction

WE demonstrate two novel BM-CDR architectures based on semiblind oversampling in both the time and space domain. These architectures are based on a hybrid topology, composed of a feedback (phase-tracking) CDR and a feed-forward CPA. These BM-CDRs are designed to achieve error-free operation (BER $< 10^{-10}$) while featuring instantaneous (0 preamble bit) clock phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts; thus, improving the efficiency of upstream PON traffic, and increasing the effective throughput of the system by raising the information rate.

The rest of the chapter is organized as follows. Section 3.2 provides an overview of BM-CDRs based on semiblind oversampling and the associated challenges. In Sections 3.3 and 3.4, we detail the high-level architecture, the phase picking algorithm, and the hardware implementation of the proposed BM-CDRs based on semiblind time and space domain oversampling. Finally, the chapter is concluded in Section 3.5

3.2 BM-CDRs Based on Semiblind Oversampling

Carrying on with the discussion in Section 2.5.3, our proposed BM-CDR architectures are based on semiblind oversampling in either the time or space domain. Fig. 3.1 shows a top-level architecture of a BM-CDR based on semiblind oversampling with a phase-tracking CDR and a feed-forward CPA.

Figs. 3.2(a) and 3.2(b) illustrate oversampling in the time and space domain, respec-

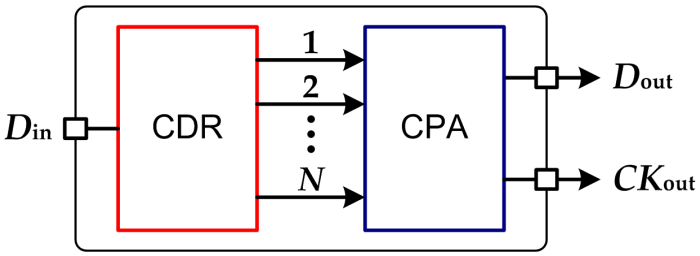


Fig. 3.1 Block diagram of the BM-CDR architecture based on semiblind oversampling (CDR: clock and data recovery; CPA: clock phase aligner).

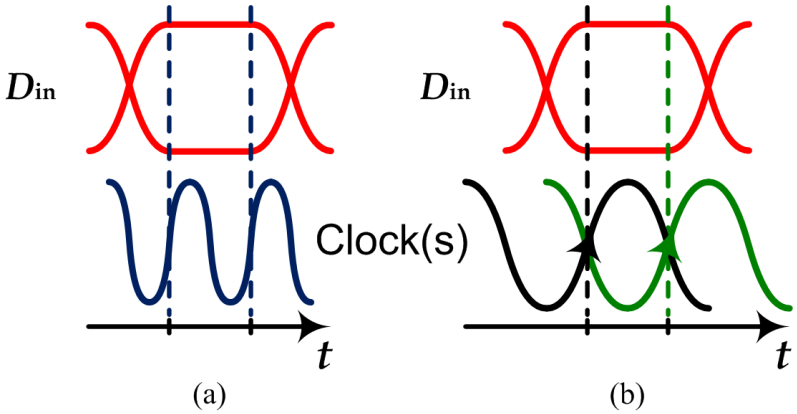


Fig. 3.2 Oversampling in the: (a) time domain; and (b) space domain.

tively. Time domain oversampling is achieved by utilizing a single clock with a frequency N *times* the bit rate, whereas space domain oversampling is achieved by utilizing multiphase N clocks that are all equally spaced with a frequency *equal* to the bit rate. In time oversampling, N *data* samples are forwarded to the CPA, whereas in space oversampling, N *clock* samples are forwarded to the CPA for picking the correct phase. The phase picking algorithm for time oversampling is based on selecting the best data sample by relying on a comparison with a known pattern. This technique is very simple but requires faster electronics, operated at $N\times$ the bit rate. On the other hand, the phase picking algorithm for space oversampling determines the clock sample closest to the center of the data eye. This technique is more complex, requiring low skew between the multiple phases of the clock. However, it has the advantage of all the electronics operated *at* the bit rate with *no a priori* knowledge of the packet delimiter, leading to a more efficient power consumption and being truly modular across applications test beds, respectively. We look at each one of the BM-CDR architectures in turn.

3.3 BM-CDR Based on Time Domain Semiblind Oversampling

In this section we propose a BM-CDR for PONs based on semiblind time domain oversampling. The BM-CDR is based on a phase-tracking CDR circuit operated at 2× the bit rate and a CPA that makes use of a phase picking algorithm. First, we detail the high-level architecture together with the phase picking algorithm. Next, we present the design of the proposed BM-CDR and its detailed hardware implementation.

3.3.1 Architecture

A block diagram of the proposed BM-CDR based on semiblind oversampling in the time domain is shown in Fig. 3.3. The BM-CDR is composed of a phase-tracking CDR and a CPA. The CDR can be operated in a 2×-oversampling mode. Thus, the BM-CDR architecture illustrated in Fig. 3.3, in essence can support three modes of operation: (1) conventional mode—a typical CDR; (2) oversampling mode—CDR operated at twice the bit rate; and (3) burst-mode—2×-oversampling CDR with the CPA. These modes of operation will be useful in measuring the relative performances theoretically and experimentally in the later sections.

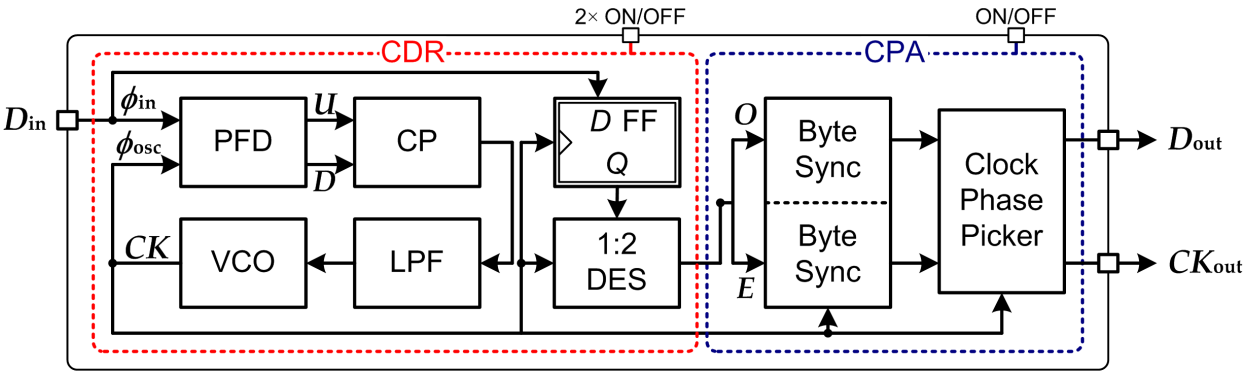


Fig. 3.3 Block diagram of the BM-CDR architecture based on semiblind oversampling in the time domain (CPA: clock phase aligner; CP: charge-pump; DES: deserializer; FF: flip-flop; LPF: low-pass filter; PFD: phase/frequency detector; Sync: synchronizer; VCO: voltage-controlled oscillator).

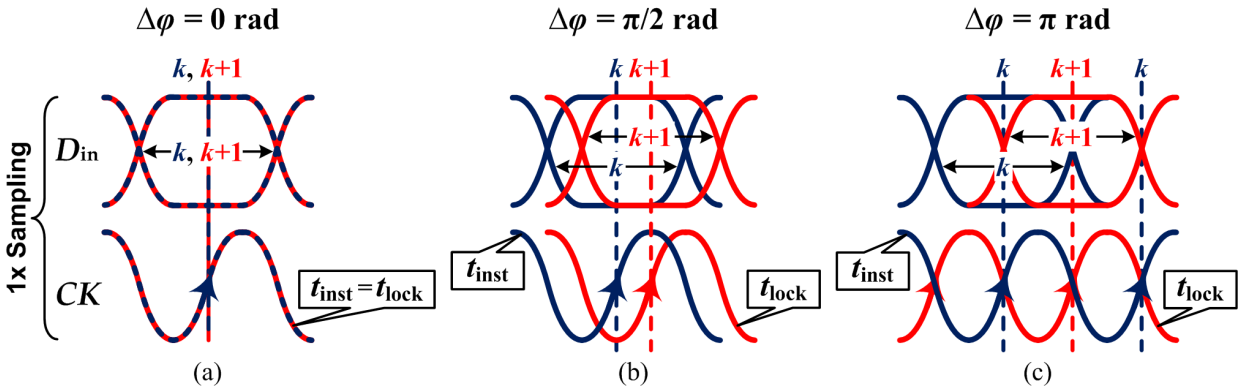


Fig. 3.4 Response of the conventional CDR to bursty traffic (consecutive packets with a phase step). Three different phase steps are considered: (a) $\Delta\varphi = 0$ rad; (b) $\Delta\varphi = \pi/2$ rad; and (c) $\Delta\varphi = \pi$ rad.

Clock and Data Recovery

The operation of the feedback CDR is explained in Section 2.5.1. The key difference however is that the generated clock signal can be used to recover the received data by sampling the data twice per bit with the decision circuit. Figs. 3.4 and 3.5 show the response of the CDR and 2×-oversampling CDR to bursty traffic. Recall that if the CDR is operated at the bit rate, the ideal sampling point is in the center of the data eye. In the case of a 2×-oversampling CDR, the two sampling points of the recovered clock t_{odd} and t_{even}, are located at $-\pi/2$ rad and $+\pi/2$ rad, respectively, from the center of the data bit. In terms of the input clock phase ϕ_{in}, and the recovered clock phase ϕ_{osc}, the condition for error-free data recovery is expressed as

$$|\phi_{\text{in}} - \phi_{\text{osc}}| < \frac{\pi}{2} \text{ rad}\,. \tag{3.1}$$

Clock Phase Aligner

The burst-mode functionality of the receiver is obtained by employing the CPA module. The CPA makes use of the 2×-oversampling CDR and a simple, fast, and effective phase picking algorithm [1, 2]. As depicted in Fig. 3.3, the CPA is based on a feed-forward topology, and comprises of two byte synchronizers and a clock phase picker. The odd and even samples (O and E, respectively, in Fig. 3.3) resulting from sampling the data

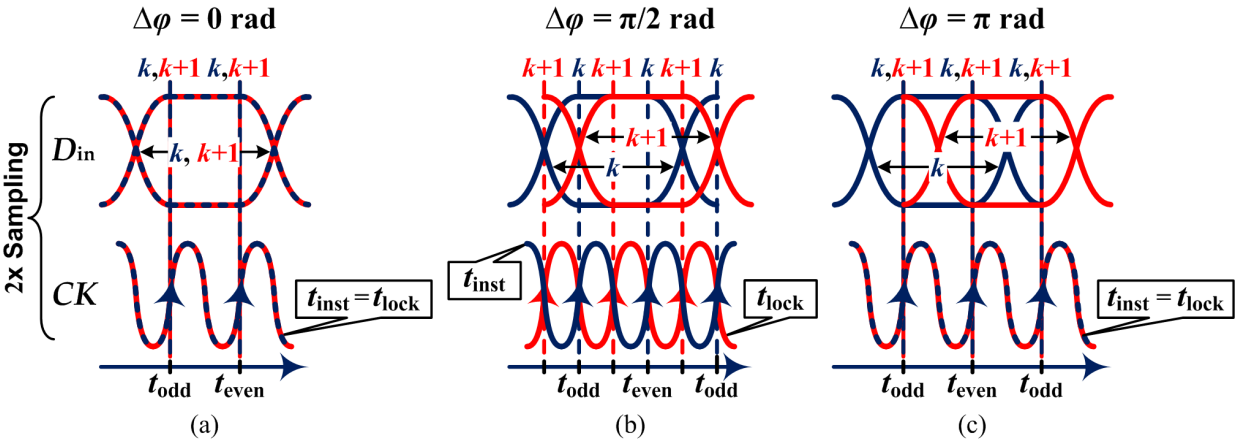


Fig. 3.5 Response of the 2×-oversampling CDR to bursty traffic (consecutive packets with a phase step) with the depiction of the odd and even samples resulting from t_{odd} and t_{even} sampling instants. Three different phase steps are considered: (a) $\Delta\varphi = 0$ rad; (b) $\Delta\varphi = \pi/2$ rad; and (c) $\Delta\varphi = \pi$ rad.

twice on the alternate (t_{odd} and t_{even}) clock rising edges (2× sampling in Fig. 3.5), are forwarded to path O and path E, respectively. The byte synchronizer is responsible for detecting the delimiter, a unique pattern indicating the start of the packet. It makes use of a payload detection algorithm to look for a preprogrammed delimiter pattern. Note that when there is no phase difference between the consecutive packets, $\Delta\varphi = 0$ rad, the odd and even samples are identical and uncorrupted. However, when there is a phase difference, $\Delta\varphi \neq 0$ rad, only one sample set is uncorrupted, while the other may or may not be corrupted. The concept then behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on either the odd and/or even samples of the data, respectively. That is, regardless of any phase step $|\Delta\varphi| \leq 2\pi$ rad, there will be at least one clock edge (either t_{odd} or t_{even}) that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the right path from the two possibilities. A more detailed explanation is presented in the next.

3.3.2 Phase Picking Algorithm—Intuitively

With the aid of some eye diagrams we review the idea behind the phase picking algorithm. Figs. 3.4 and 3.5 shows the response of the CDR operated at the bit rate, and the 2×-oversampling mode of the CDR with the CPA operation, respectively. Three specific phase

differences between the consecutive packets are considered: (1) $\Delta\varphi = 0$ rad; (2) $\Delta\varphi = \pi/2$ rad; and (3) $\Delta\varphi = \pi$ rad. Note that whereas $\Delta\varphi = \pi$ rad represents a worst-case phase step for the CDR operated at the bit rate [see Fig. 3.4(c)], $\Delta\varphi = \pi/2$ rad phase step is the worst-case scenario for the oversampling CDR at 2× the bit rate [see Fig. 3.5(b)]. The 2×-oversampling mode produces two samples per bit, which helps the CPA algorithm to lock at the correct phase of the incoming packet. To understand how the CPA works, consider the case when there is no phase step ($\Delta\varphi = 0$ rad); path O correctly samples the incoming pattern [see t_{odd} in Fig. 3.5(a)]. For phase step $\Delta\varphi = \pi/2$ rad, path O will sample the bits on or close to the transitions after the phase step [see t_{odd} in Fig. 3.5(b)]. In this situation, the byte synchronizer of path O will likely not detect the delimiter at the beginning of the packet. On the other hand, the byte synchronizer of path E will have no problems detecting the delimiter [see t_{even} in Fig. 3.5(b)]. The phase picker controller monitors the state of the two byte synchronizers and selects the correct path accordingly (path E in this particular case). Once the selection is made, it cannot be overwritten until the comma is detected, indicating the end of the packet. This process repeats itself at the beginning of every packet. Similarly, for a $\Delta\varphi = 3\pi/2$ rad phase step (not shown in Fig. 3.5 because the scenario is similar to the $\pi/2$ rad phase step), path E samples the bits on or close to the transitions and thus the phase picker controller selects path O. Consequently, the result is that the CPA achieves instantaneous phase acquisition (0-bit) for any phase step $|\Delta\varphi| \leq 2\pi$ rad; that is, no preamble bits ($l = 0$) at the beginning of the packet are necessary. In Chapter 4, we provide a mathematical proof by deriving a theoretical probabilistic model for the BM-CDR.

3.3.3 Design and Implementation

Next we present the design of the proposed BM-CDR and its detailed hardware implementation.

Building Blocks

The main building blocks of the BM-CDR we designed are illustrated in Fig. 3.6. The BM-CDR is essentially composed of a multirate CDR and a CPA module implemented on a Virtex IV field-programmable gate array (FPGA) from Xilinx. The multirate CDR is comprised of a clock recovery unit (CRU) from Centellax (Part #TR1C1-A) and a data

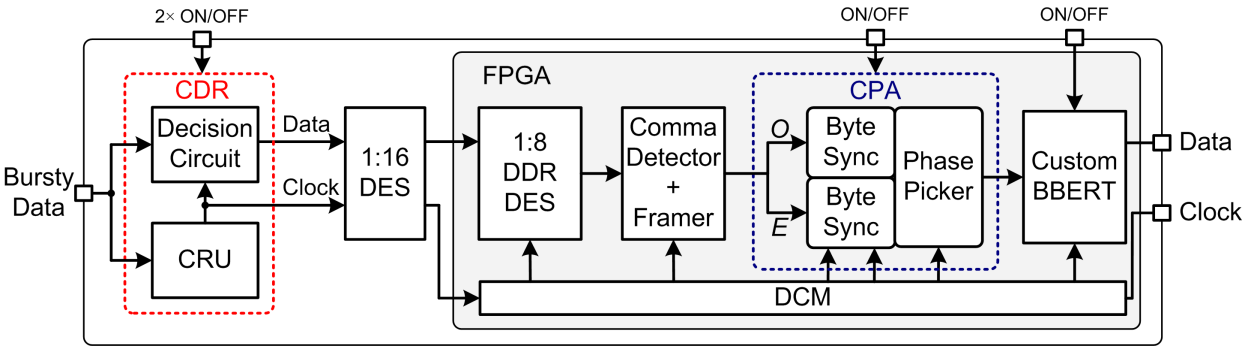


Fig. 3.6 Building block diagram of the BM-CDR based on time domain oversampling (BBERT: burst bit error rate tester; CDR: clock and data recovery; CPA: clock phase aligner; CRU: clock recovery unit; DCM: digital clock manager; DES:deserializer; FPGA: field-programmable gate array; Sync: synchronizer).

sampler or D flip-flop (D-FF) from Inphi (Part #13701DF), both rated at 13 Gb/s. The multirate CDR recovers the clock and data from the incoming signal. The CDR supports the following frequencies of interest: (1) 5 Gb/s for conventional mode; and (2) 10 Gb/s for 2× oversampling and burst-mode. The CDR is followed by a 1:16 deserializer (DES) from Maxim-IC (Part #MAX3950) rated at 10.3 Gb/s. The deserializer reduces the frequency of the recovered clock and data to a lower frequency that can be processed by the digital logic. The lower rate 16-bit parallel data and the divided clock are then brought onto the FPGA for further processing. The maximum data rate supported by the low-voltage differential signaling (LVDS) buffers of the FPGA is 840 Mb/s. Thereafter, a double-data rate (DDR) 1:8 DES, a framer, a comma detector, the CPA (including byte synchronizers and a phase picker), and a digital clock manager (DCM) are implemented on the FPGA alongside a custom burst BER tester (BBERT). A computer is then used to communicate with the BBERT.

On the board, it is first necessary to further parallelize the data and clock to a lower frequency that will ensure proper synchronization and better stability of these signals before they can be sent to the CPA for automatic phase acquisition. Thus, an integrated DDR 1:8 DES is implemented on the FPGA which will be elaborated upon in the next section. Automatic detection of the payload is implemented on the FPGA through a framer and a comma detector that are responsible for detecting the beginning (delimiter bits) and the end (comma bits) of the packets, respectively. As described in Section 3.3.1, the CPA

makes use of a phase picking algorithm and a CDR operated in 2×-oversampling mode. The CPA is turned ON for BER and PLR measurements with phase acquisition for burst-mode reception ($\Delta\varphi \neq 0$ rad); otherwise, it can be by-passed for continuous-mode reception ($\Delta\varphi = 0$ rad). The realigned data is then sent to the custom BBERT which will be detailed shortly.

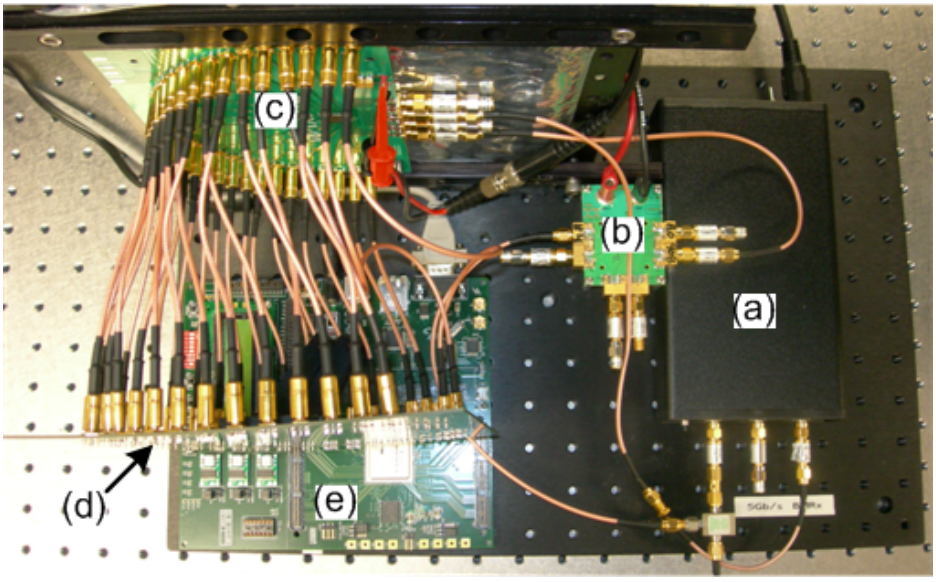
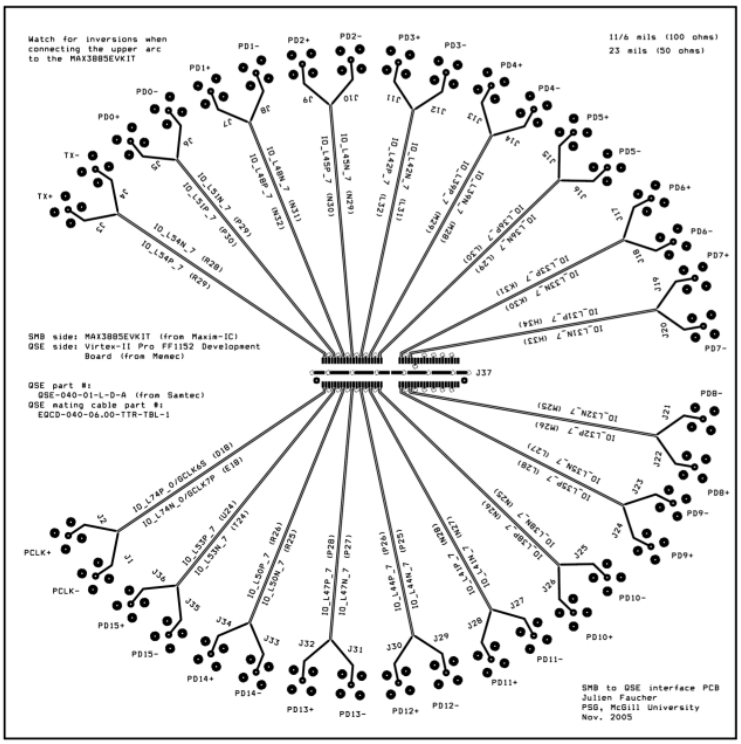


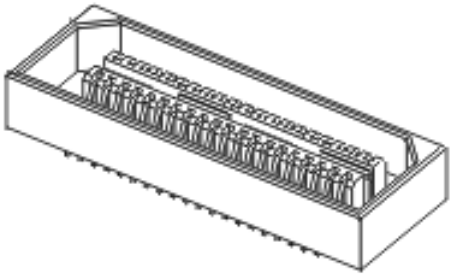
Fig. 3.7 Photograph of the current implementation of the BM-CDR based on time oversampling. (a) Clock recovery unit. (b) Data sampler. (c) 1:16 deserializer. (d) Custom SMB-to-QSE interface PCB. (e) FPGA.

Implementation Details

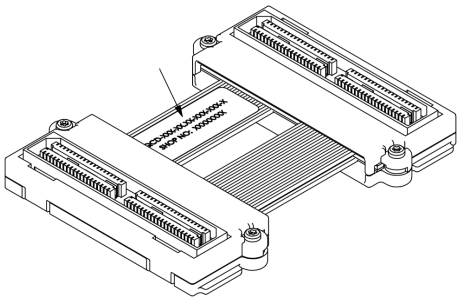
A photograph of the current implementation of the BM-CDR is shown in Fig. 3.7. The 1:16 DES evaluation board uses a SubMiniature version B (SMB) connector (rated at 4 GHz), whereas the FPGA evaluation board uses a high-speed micro Q-strip interface socket (QSE) connector. In Fig. 3.7, the printed circuit board (PCB) that sits between the deserializer and the FPGA serves as a SMB-to-QSE connector converter. Fig. 3.8(a) shows the PCB footprint of the custom SMB-to-QSE interface PCB [1]. We used 34 six-inch SMB cables (16-bit differential data + 1 differential clock) to connect the DES outputs to the SMB-to-QSE interface PCB. The QSE connector is from Samtec [Part #QSE-040-01-L-D-A; see Fig. 3.8(b)], rated at 8 GHz (differential signaling). Since the outputs of the DES and the



(a)



(b)



(c)

Fig. 3.8 Implementation details of the BM-CDR based on time oversampling. (a) QSE connector from Samtec (Part #QSE-040-01-L-D-A). (b) Mating cable, also from Samtec (Part #EQCD-040-06.00-TTR-TBL-1). (c) Custom SMB-to-QSE interface PCB [2].

inputs of the FPGA both use LVDS logic, no conversion other than a connector conversion is needed at the interface between the two. A high-speed parallel mating cable rated at 1.74 GHz, also from Samtec [Part #EQCD-040-06.00-TTR-TBL-1; see Fig. 3.8(c)], is used to complete the connections to the FPGA. Note that the SMB-to-QSE interface PCB would not be part of a commercial product and would not be needed if the main blocks were integrated on a single PCB or a single application-specific integrated circuit (ASIC).

Data Deserialization

The main challenge in designing gigabit-capable receivers based on FPGAs, is the limited processing speed of digital logic on commercially available FPGAs. For example, the DCM module on the FPGA, in essence a digital PLL, is limited to an operating range of 24 MHz to 500 MHz. The latter frequency is 20 times slower than the targeted 10 Gb/s (2×-oversampling of the 5 Gb/s data). Thus, two stages of deserialization are employed. Note that the DCM, an intellectual property (IP) block from Xilinx, is a key design component that provides multiple phases of a source clock, and a zero propagation delay with low clock skew between the output clock signals distributed throughout the board.

The first deserialization stage is performed by the off-board 1:16 deserializer. The oversampled 10 Gb/s data and clock are deserialized to 34 parallel signals (16 differential data signals + 1 differential clock signal), each at 625 Mb/s each. These signals are then brought on to the FPGA board through LVDS logic. The maximum data rate supported by the LVDS buffers of the FPGA is 840 Mb/s, well above (215 Mb/s) the deserialized signal data rate. However, the 625 MHz clock signal is 1.25× faster than the maximum operating frequency of DCM which is 500 MHz. Thus, a clock divider is used to reduce the frequency of the received clock to 312.5 MHz. This clock signal is then fed to a DCM block for further clock distribution throughout the system.

The second deserialization stage is based on the DDR signaling, and it is accomplished by a 1:8 deserializer designed and implemented on the FPGA. It uses the 312.5 MHz DCM output clock signal to sample the 625 Mb/s incoming data at both the rising and the falling clock edges—DDR signaling. In this way, each data signal is separated into two data lines by a half-rate clock signal. The same clock is then used to demultiplex these two lines of data into an 8-bit data path. In summary, the 16 input data signals are deserialized to 128 data lines at ∼78 Mb/s which is eight times lower than 625 Mb/s. The advantage of this

method is that the clock signal is well within the 24 MHz to 500 MHz operating range of the DCM guaranteeing system synchronization while keeping the same harmonic content of the clock and data lines.

Burst BER Tester

The FPGA-based BBERT designed is implemented to selectively perform BER and PLR measurements on only the payload of the packets. The BERT compares the incoming data, a pseudorandom binary sequence (PRBS), with an internally generated PRBS. Note that, while a conventional BERT can be used to make the BER measurements, PLR measurements on discontinuous, bursty data, is not supported. This is because conventional BERTs require a continuous alignment between the incoming pattern and the reference pattern, and milliseconds to acquire synchronization. The phase step response of the burst-mode CDR can make conventional BERTs lose pattern synchronization at the beginning of every packet while the sampling clock is being recovered by the CDR. The custom BERT does not require fixed synchronization between the incoming pattern and the reference pattern of the error detector. Synchronization happens instantaneously at the beginning of every packet, therefore enabling PLR measurements on discontinuous, bursty data.

There are a total of 19 counters on the FPGA to keep track of the PLR and the BER. 16 counters are used to count the number of errors in the deserialized data. The three remaining counters keep track of the number of packets received, the number of bits received, and the number of packets lost, respectively. We used MATLAB to compute and display the PLR and the BER in real time, and we used HyperTerminal to control and monitor the state of the BM-CPA. Both communicate with the FPGA core through the RS-232 protocol. In order to selectively perform BER measurements on the payload of the packets, we used the delimiter and the comma as gating signals for the 16 error counters. The 16-bit parallel data is compared with the PRBS loaded into a memory block of the FPGA. The memory address is incremented each time a new 16-bit vector is clocked in. It is reset to zero when the comma is detected in order to arm the BBERT for the next packet. The packet and packet lost counters are always enabled. Since the comma is far away from the beginning of the packet, it is always detected. Moreover, we used a long comma (48 bits) in order to reduce the probability of getting a false positive. The packet counter is incremented every time a comma is detected. The packet lost counter is incremented when

a comma does not pair up with a previously received delimiter. This situation arises when the CDR was not given a preamble long enough to recover the phase before the arrival of the delimiter. When a packet is lost, it does not contribute to the BER. Hence, a zero BER does not mean that there are no errors. Both the PLR and the BER must be monitored while measuring the phase acquisition time.

Author's Contribution

The author of this thesis designed the BM-CDR and carried out the hardware implementation.

Acknowledgment

The author would like to acknowledge the following individuals for their contributions during the early phases of this project. Dr. Julien Faucher (1) proposed the phase picking algorithm and implemented it in VHDL on a Virtex-II Pro FPGA board at 622 Mb/s; and (2) designed and implemented the custom SMB-to-QSE interface PCB. Ms. Ming Zeng and Mr. Nicholas Zicha, M.Eng. students, assisted in porting the VHDL code of the CPA from the 622-Mb/s version on the Xilinx-II Pro FPGA board to the 5-Gb/s version on the Xilinx Virtex-IV FPGA board, and provided technical assistance.

3.4 BM-CDR Based on Space Domain Semiblind Oversampling

In this section we propose a BM-CDR for PONs based on semiblind space domain oversampling. This BM-CDR is based on a phase-tracking CDR circuit with multiphase clocks at the bit rate and a CPA that makes use of a novel phase picking algorithm. In contrast to the BM-CDR based on semiblind time domain oversampling, this BM-CDR uses electronics operated at the bit rate with *no a priori* knowledge of the packet delimiter, leading to a more efficient power consumption and being truly modular across application testbeds, respectively. We first detail the high-level architecture together with the novel phase picking algorithm. Next, we present the design of the proposed BM-CDR and its detailed hardware implementation.

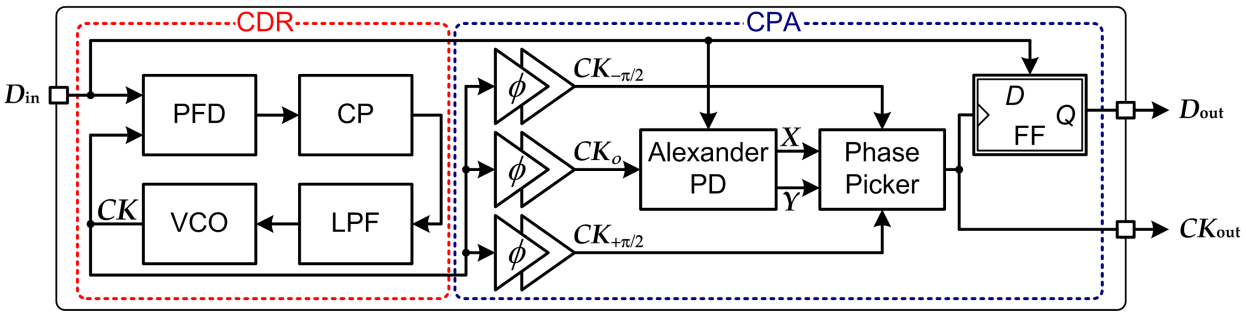


Fig. 3.9 Block diagram of the BM-CDR architecture based on a semi-blind oversampling in the space domain (CPA: clock phase aligner; CP: charge-pump; FF: flip-flop; LPF: low-pass filter; PD: phase detector; PFD: phase/frequency detector; VCO: voltage-controlled oscillator).

3.4.1 Architecture

A block diagram of the proposed BM-CDR based on semiblind oversampling in the space domain is shown in Fig. 3.9. As before, the BM-CDR is composed of a phase-tracking CDR and a CPA. However, the key difference being that the BM-CDR, instead of utilizing a phase-tracked oversampling clock in the time domain operated at $2\times$ the bit rate, employs phase-tracked simultaneous multiphase clocks at the bit rate; that is, oversampling in the space domain. Recall that if the CDR is operated at the bit rate, the ideal sampling point by the recovered clock is in the center of the data eye, and that the phase error process is modulo-2π rad. In the case of $2\times$-oversampling with multiphase clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, separated by π rad, the sampling points are located at $-\pi/2$ rad and $+\pi/2$ rad, respectively, from the center of the data bit; in this case, the phase error process is modulo-π rad.

Clock Phase Aligner

As already mentioned, the burst-mode functionality of the receiver is obtained by employing the CPA module. The CPA utilizes multiphase clocks at the bit rate and a novel phase picking algorithm based on an "early-late" detection principle that is simple, fast and effective. As illustrated in Fig. 3.9, the CPA is based on a feed-forward topology, and comprises of phase (ϕ-) shifters, an Alexander phase detector (PD), a phase picker, and a decision circuit (D-FF). The ϕ-shifters utilize the clock recovered by the CDR CK, to provide multiple clocks: CK_o, $CK_{-\pi/2}$, and $CK_{+\pi/2}$, with low skew and different phases:

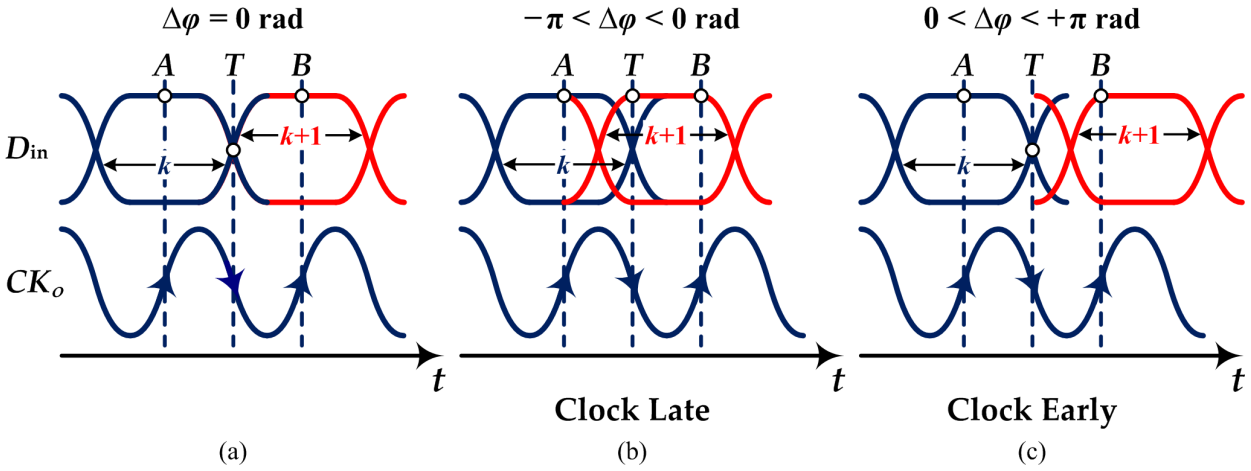


Fig. 3.10 Alexander PD three-point sampling scheme for different phases between consecutive packets: (a) $\Delta\varphi = 0$ rad, CK_o in-phase with D_{in}; (b) $-\pi < \Delta\varphi < 0$ rad, CK_o leads D_{in}—is late; and (c) $0 < \Delta\varphi < +\pi$ rad, CK_o lags D_{in}—is early.

0 rad, $-\pi/2$ rad, and $+\pi/2$ rad, respectively, with respect to CK. Next, an Alexander PD [3] which inherently exhibits *bang-bang* (binary) characteristics, compares edges of the data bit D_{in}, and the rising edges of clock CK_o. This results in one of the following outputs depending on the phase difference $\Delta\varphi$, between the consecutive packets: (a) CK_o lags D_{in}—is late—when $-\pi < \Delta\varphi < 0$ rad; (b) CK_o leads D_{in}—is early—when $0 < \Delta\varphi < +\pi$ rad; and (c) CK_o is either in-phase with D_{in} when $\Delta\varphi = 0$ rad, or antiphase with D_{in} when $|\Delta\varphi| = \pi$ rad. This is depicted in Fig. 3.10(a)–(c). This information together with the two multiphase clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, is provided to the phase picker which is responsible for selecting one of these clocks for sampling by the decision circuit. Note that when there is no phase difference between the consecutive packets $\Delta\varphi = 0$ rad, either of the clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, will correctly sample the data resulting in identical and uncorrupted sample sets. However, when there is a phase difference $\Delta\varphi \neq 0$ rad, only one clock, $CK_{-\pi/2}$ or $CK_{+\pi/2}$, will correctly sample the data, while the other clock may or may not corrupt the sample set. That is, regardless of any phase step $|\Delta\varphi| \leq 2\pi$ rad, there will be at least one sampling clock, either $CK_{-\pi/2}$ or $CK_{+\pi/2}$, that will yield an accurate sample. The phase picker then selects the most accurate sampling clock from the two possibilities. A more detailed explanation is presented next.

3.4.2 Novel Phase Picking Algorithm

The heart of the CPA constitutes the Alexander PD and phase picker. Three specific phase difference scenarios between the consecutive packets are considered: (1) $\Delta\varphi = 0$ rad; (2) $-\pi < \Delta\varphi < 0$ rad; and (3) $0 < \Delta\varphi < +\pi$ rad. The Alexander PD is a bang-bang system, exhibiting a very high gain in the vicinity of a zero phase; that is, a small phase difference between data and clock edges drive the output signals X and Y (see Fig. 3.9), to full logical levels. As shown in Fig. 3.10(a), the concept behind the Alexander PD is based on strobing the data waveform D_{in}, with consecutive clock CK_o edges, at multiple points in the vicinity of expected transitions, resulting in samples that can provide the necessary information. These data samples include: (1) the previous bit A; (2) the current bit B; and (3) a sample of the current bit at the zero crossing T. With these samples, the PD can determine whether a data transition is present and whether the clock CK_o, leads or lags the data edge D_{in}, based on the following rules: (a) if $A \neq T = B$, then the clock is late when $-\pi < \Delta\varphi < 0$ rad [see Fig. 3.10(b)]; (b) if $A = T \neq B$, then the clock is early when $0 < \Delta\varphi < +\pi$ rad [see Fig. 3.10(c)]; (c) if $A = B \neq T$, then no decision is possible as the clock is either in-phase with the dats when $\Delta\varphi = 0$ rad, or antiphase with D_{in} when $|\Delta\varphi| = \pi$ rad; and (d) if $A = T = B$, no data transition has occurred due to consecutive identical digits (CIDs). Consequently, the signals $X \equiv T \oplus B$ and $Y \equiv A \oplus T$ in Fig. 3.9 provide this early-late information to the phase picker as follows: (a) if X is low and Y is high, then CK_o lags D_{in}—is late; (b) if X is high and Y is low, then CK_o leads D_{in}—is early; (c) if $X = Y$, is low, no data transition is present; and (d) if $X = Y$ is high, no decision is possible.

With the aid of some eye diagrams we illustrate the idea behind the phase picking algorithm that is based on the early-late detection principle. Fig. 3.11 shows the response of sampling the data with the three clocks: the unshifted clock CK_o, and the multiphase clocks $CK_{-\pi/2}$, and $CK_{+\pi/2}$. As before, let t_{inst} be the instantaneous clock that is in-phase with the last bit of the k^{th} packet, and out-of-phase by $|\Delta\varphi| \leq 2\pi$ rad with the first bit of the $(k+1)^{\text{th}}$ packet. To achieve instantaneous phase acquisition, the CPA must be able to make use of the instantaneous clock t_{inst}, to correctly sample the bits of the $(k+1)^{\text{th}}$ packet until the CDR's feedback loop has had enough time to settle down and acquire lock; that is, align the instantaneous clock t_{inst}, to the lock state t_{lock}, so as to sample in the middle of the data bit.

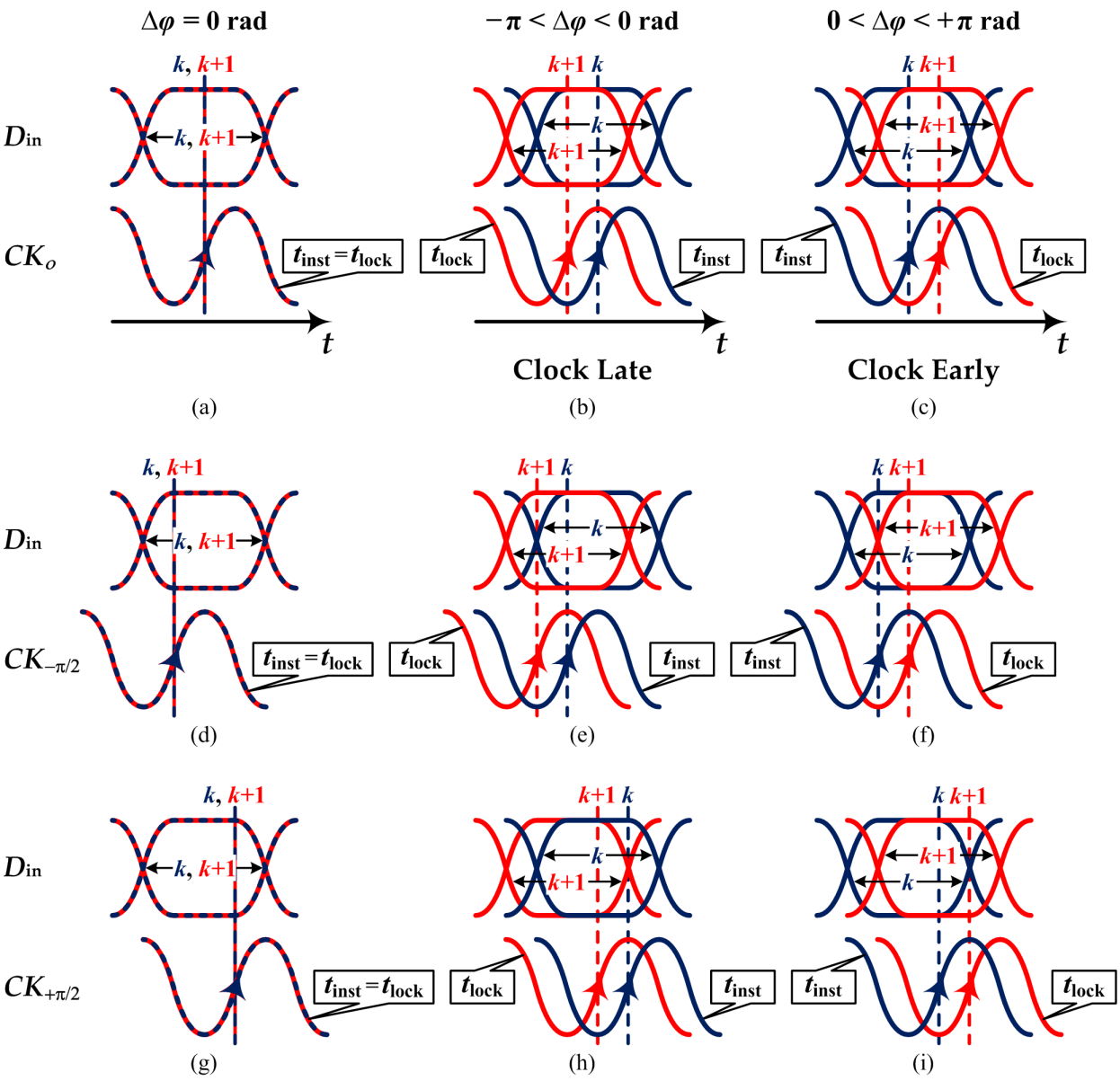


Fig. 3.11 CPA phase picking algorithm. Three different phase steps between consecutive packets are considered: $\Delta\varphi = 0$ rad; $-\pi < \Delta\varphi < 0$ rad; and $0 < \Delta\varphi < +\pi$ rad.

To understand how the CPA works, consider, the case when there is no phase step ($\Delta\varphi = 0$ rad); either of the clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, will correctly sample the incoming pattern [see Figs. 3.11(d) and 3.11(g)]. Similarly, this is the case for an antiphase step $\Delta\varphi = \pm\pi$ rad, (not shown in Fig. 3.11 because the scenario is similar to the 0 rad phase

step—a modulo-π process), either of the clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, will correctly sample the incoming pattern. For phase step $-\pi < \Delta\varphi < 0$ rad, the clock CK_o will lag the data [see Fig. 3.11(b)]; clock $CK_{+\pi/2}$ will sample the bits on or close to the transitions after the phase step [see Fig. 3.11(h)]. In this situation, the delimiter bits at the beginning of the packet will likely get corrupted and thus not be detected. On the other hand, clock $CK_{-\pi/2}$ will correctly sample the data resulting in the successful detection of the packet delimiter [see Fig. 3.11(e)]. Similarly, for a phase step $0 < \Delta\varphi < +\pi$ rad, the clock CK_o will lead the data [see Fig. 3.11(c)]; clock $CK_{-\pi/2}$ will sample the bits on or close to the transitions after the phase step [see Fig. 3.11(f)] and thus corrupt the bits. However, clock $CK_{-\pi/2}$ will correctly sample the data [see Fig. 3.11(i)]. The phase picker controller (combinational logic) monitors the state of the multiphase clocks with respect to the CK_o and select the correct one accordingly. Consequently, the result is that the CPA achieves instantaneous phase acquisition (0-bit) for any phase step $|\Delta\varphi| \leq 2\pi$ rad; that is, no preamble bits ($l = 0$) at the beginning of the packet are necessary. In Chapter 4, we provide a mathematical proof by deriving a theoretical probabilistic model for the BM-CDR. The CPA logic summarized as shown in Table 3.1. It is also depicted as a the two-state transition diagram in Fig. 3.12.

Table 3.1 CPA logic

Phase Condition	$\boldsymbol{CK_o}$	$\boldsymbol{CK_{\text{out}}}$
$-\pi < \Delta\varphi < 0$ rad	Late	$CK_{-\pi/2}$
$0 < \Delta\varphi < \pi$ rad	Early	$CK_{+\pi/2}$
$\Delta\varphi \in \{0, \pm\pi \text{ rad}\}$ or CIDs	$\times$	$CK_{\pm\pi/2}$

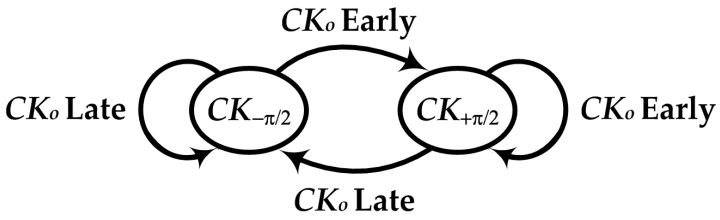


Fig. 3.12 CPA logic two-state transition diagram.

3.4.3 Design and Implementation

Next we present the design of the proposed BM-CDR and its detailed hardware implementation.

Building Blocks

The main building blocks of the BM-CDR we designed are illustrated in Fig. 3.13. The BM-CDR is built from low cost/complexity commercial-off-the-shelf (COTS) components. All these components are designed to support data transmission rates up to 13 Gb/s and clock frequencies as high as 13 GHz. The input data is first passed through a 1:3 fanout buffer from Hittite Microwave (Part #HMC940LC4B). The fanout buffer create three replicas of the input signal D_{in}. Two of the replicas are sent (via adjustable delay buffers) to the CPA, that is, the Alexander PD and a data sampler for further processing. One of the replicas is sent to a CRU from Centellax (Part #TR1C1-A). The CRU recovers a clock signal from the data stream. The CRU is followed by three analog ϕ-shifters from Hittite Microwave (Part #HMC538LP4). The ϕ-shifters utilize the clock recovered by the CRU CK, to provide multiple clocks: CK_o, $CK_{-\pi/2}$, and $CK_{+\pi/2}$, with low skew and different phases: 0 rad, $-\pi/2$ rad, and $+\pi/2$ rad, respectively, with respect to CK. The ϕ-shifters are followed by the Alexander PD and phase picker whose digital logic operation will be detailed shortly. The Alexander PD is also from Hittite Microwave (Part #HMC6032LC4B). It compares edges of the data bit D_{in}, with the clock signal CK_o, and provides the relative lead/lag information. The clock CK_o early-late information (X and Y) together with the two multiphase clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, is provided to the phase picker which is responsible for selecting one of these clocks for sampling by the decision circuit. The D-FF from Inphi (Part #13701DF) is nominally positive edge triggered.

Alexander PD

The foregoing observation on the Alexander PD in Sections 3.4.1 and 3.4.2 lead to the circuit topology illustrated in Fig. 3.14(a) [3].

The concept behind the Alexander PD as shown in Fig. 3.10(a), is based on strobing the data waveform D_{in}, with consecutive clock CK_o edges, at multiple points in the vicinity of expected transitions, resulting in three samples: (1) the previous bit A; (2) the current bit B; and (3) a sample of the current bit at the zero crossing T. From Fig. 3.14, D-FF$_1$

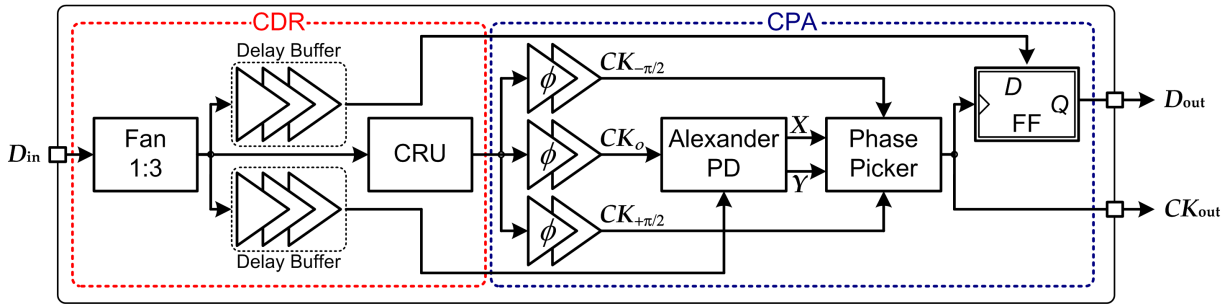


Fig. 3.13 Building block diagram of the BM-CDR based on space domain oversampling (CPA: clock phase aligner; CRU: clock recovery unit; PD: phase detector).

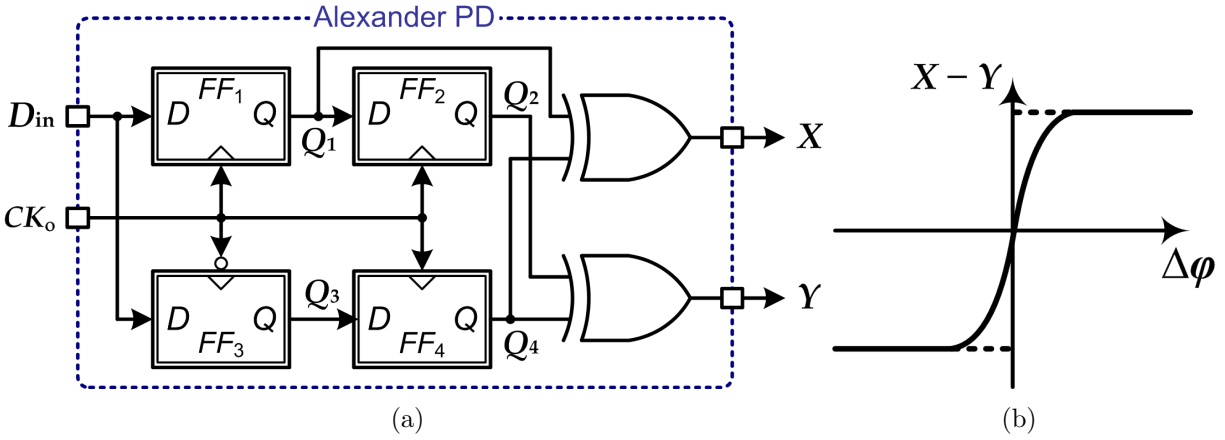


Fig. 3.14 Alexander PD (a) Circuit topology. (b) Transfer function exhibiting metastability.

samples A and B on the rising edge of CK_o and D-FF$_2$ delays the result by one clock cycle. D-FF$_3$ samples T on the falling edge of CK_o D-FF$_4$ delays this sample by half a clock cycle.

To gain more insight into its operation, consider Fig. 3.15 which examines the waveforms at various points in the Alexander PD when the phase difference $\Delta\varphi$, between the consecutive packets. For a phase step $-\pi < \Delta\varphi < 0$ rad, the clock CK_o will lag the data; X assumes a low level for each data transition and Y a high level. Thus, the average PD output $(X - Y)$avg, assumes a high negative value. Conversely, for a phase step $0 < \Delta\varphi < +\pi$ rad, the clock CK_o will lead the data; then $(X - Y)$avg assumes a high positive value. As $\Delta\varphi$ approaches zero, the second sample T, fall in the vicinity of the data crossing, thereby driving D-FF$_3$ and D-FF$_4$ into metastability [4]. This implies that the Alexander PD is a bang-bang (nonlinear) system, exhibiting a very high gain in the

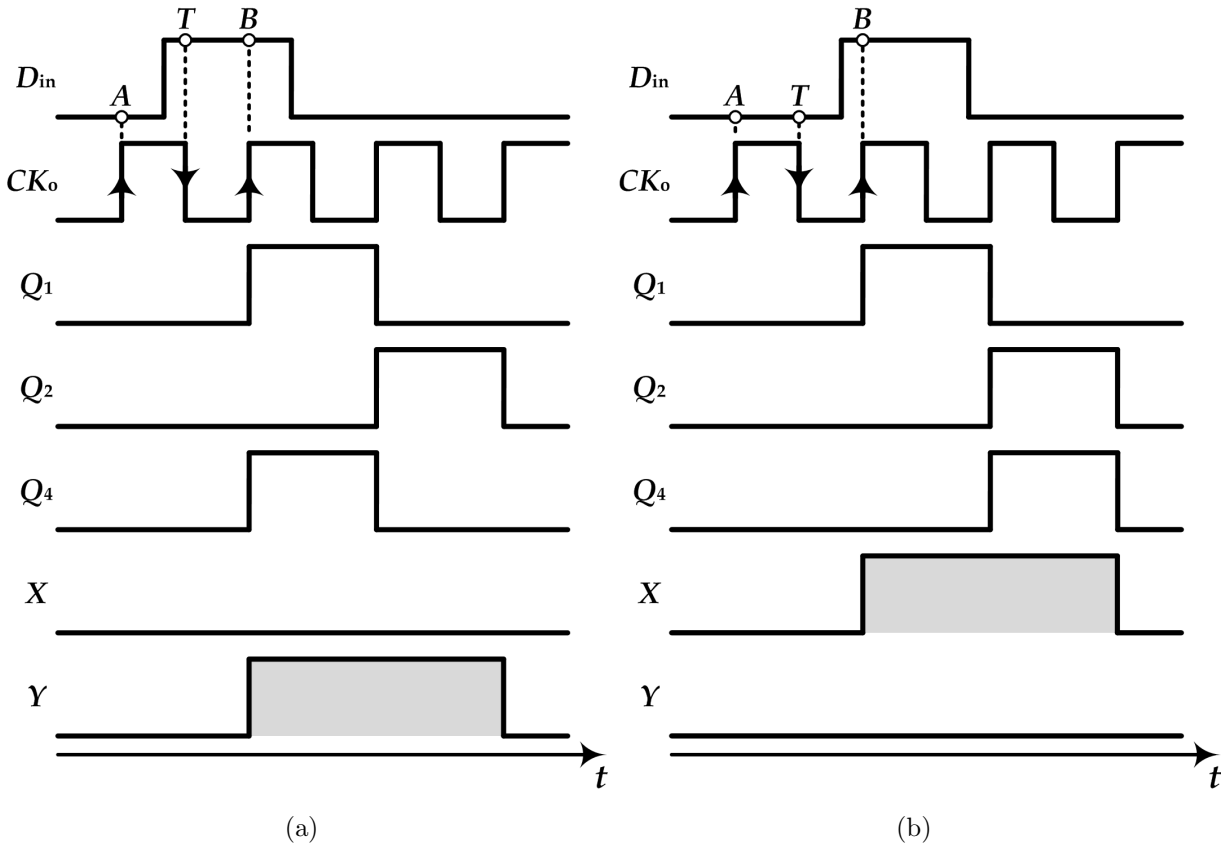


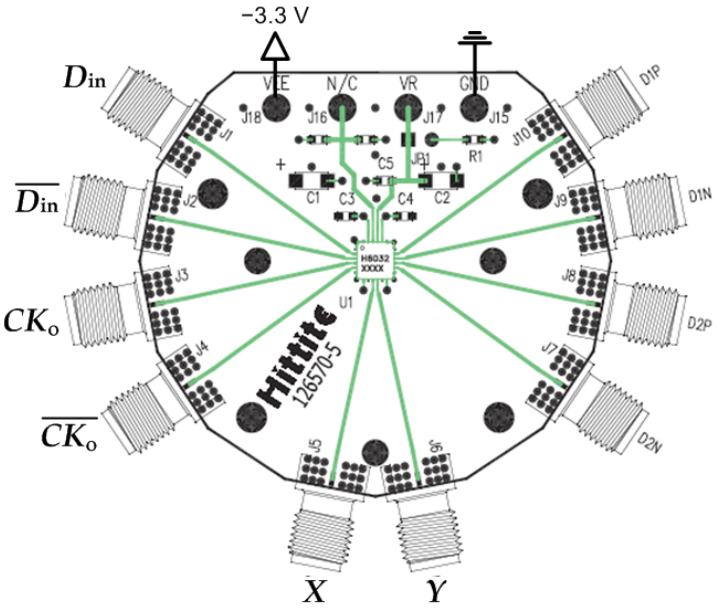
Fig. 3.15 Alexander PD waveforms for: (a) late clock; and (b) early clock. [4].

vicinity of $\Delta\varphi = 0$ rad as exemplified in Fig. 3.14(b).

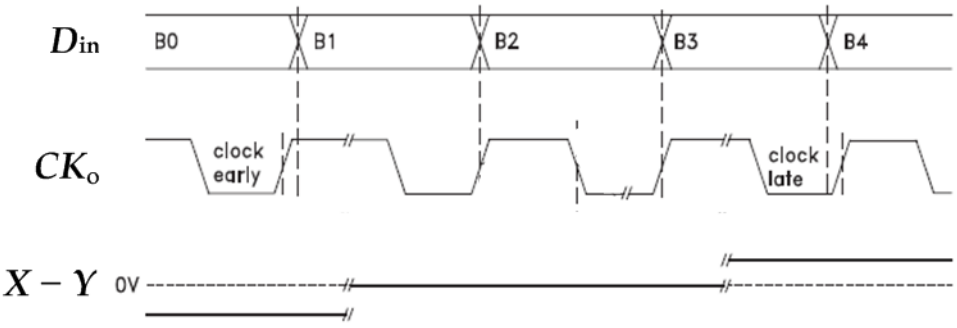
As mentioned, the Alexander PD evaluation board is from Hittite Microwave (Part #HMC6032LC4B). Fig. 3.16 shows the schematic of the PCB together with the corresponding timing diagram depicting the lead-lag of clock CK_o, with respect to the data D_{in}, resulting in the early-late information $(X - Y)$avg.

Phase Picker

The phase picker algorithm detailed in Section 3.4.2 leads to the truth table logic summarized in Table 3.2. This results into the phase picker being implemented as a digital combinational logic circuit as shown in Fig. 3.17. It is built from evaluation PCBs from Hittite Microwave. The phase picker is composed of an AND gate (Part #HMC722LC3C)



(a)



(b)

Fig. 3.16 Alexander PD. (a) Evaluation PCB. Note the two differential (four-signal) output ports to the right are not used in our configuration. (b) Timing diagram depicting the early-late conditions.

and a 2:1 selector (Part #HMC678LC3C). The schematics of the AND gate and 2:1 selector evaluation PCBs together with the corresponding timing diagrams are given in Figs. 3.18 and 3.19, respectively.

Table 3.2 Phase picker logic

Data Condition	CK_o	XY	CK_{out}
$-\pi < \Delta\varphi < 0$ rad	Late	$\downarrow\uparrow$	$CK_{-\pi/2}$
$0 < \Delta\varphi < \pi$ rad	Early	$\uparrow\downarrow$	$CK_{+\pi/2}$
$\Delta\varphi \in \{0, \pm\pi \text{ rad}\}$ or CIDs	$\times$	$\uparrow\uparrow, \downarrow\downarrow$	$CK_{\pm\pi/2}$

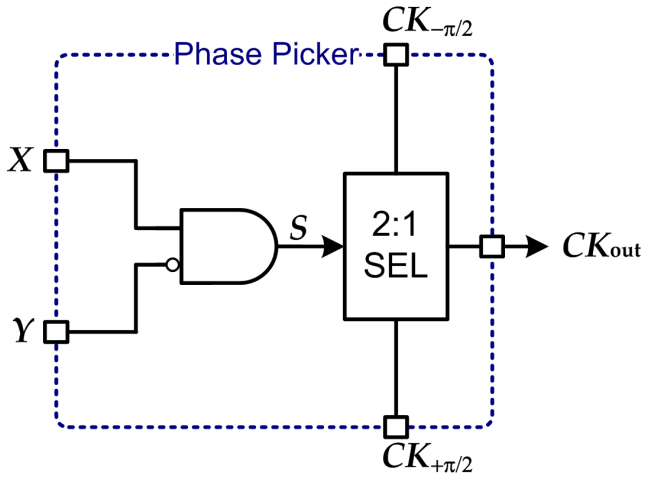


Fig. 3.17 Phase picker implemented with digital combinational logic.

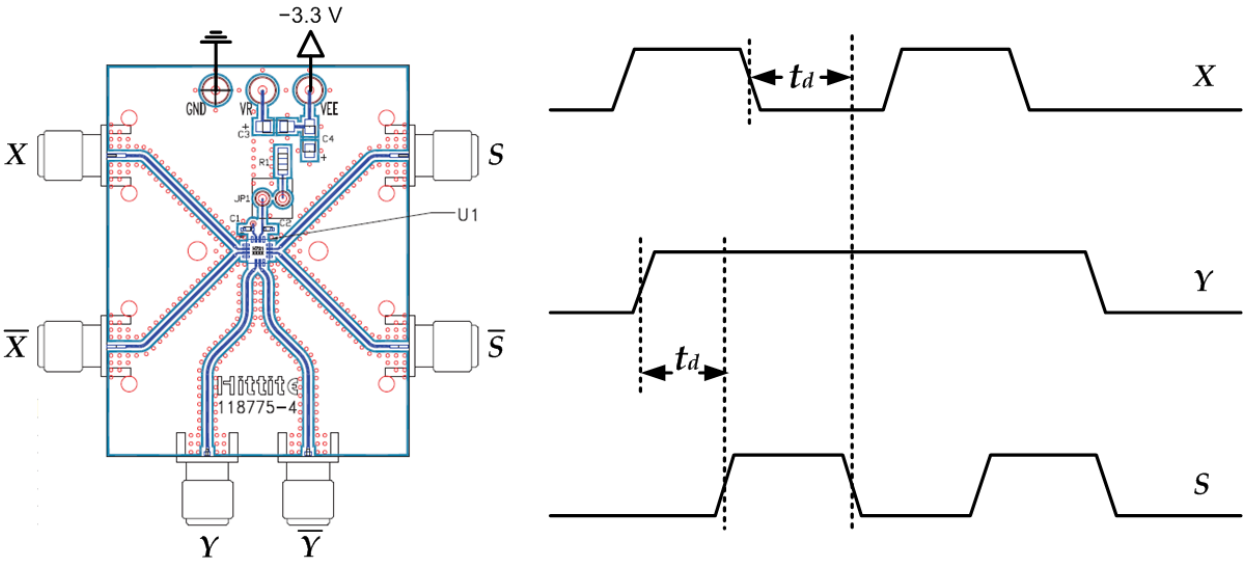


Fig. 3.18 AND gate evaluation PCB and timing diagram ($t_d = 96$ ps).

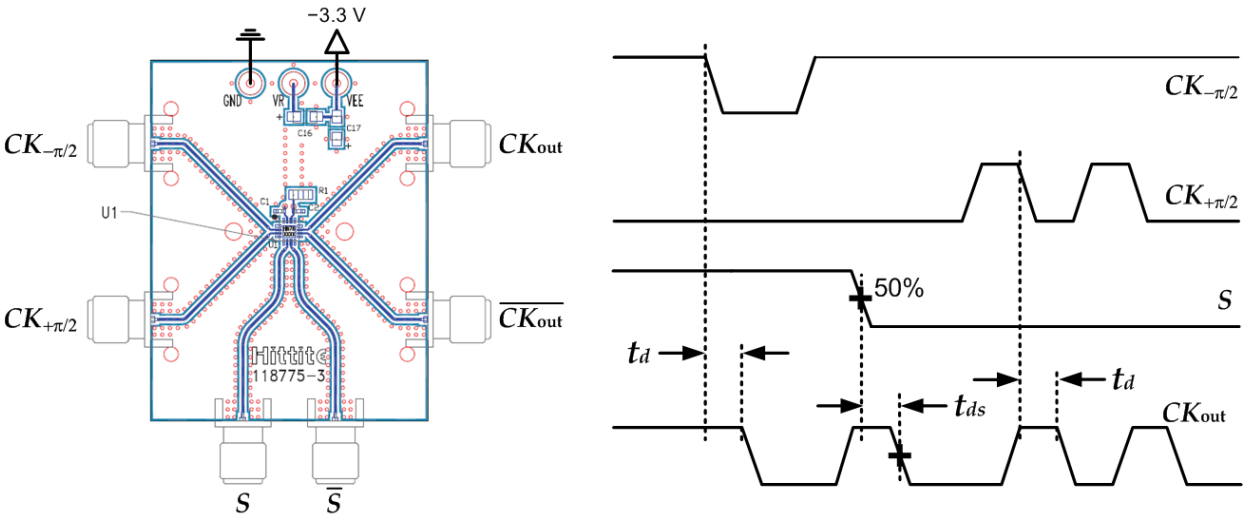


Fig. 3.19 AND gate evaluation PCB and timing diagram (t_d = 125 ps; t_{ds} = 135 ps).

Implementation Details

It should be noted that for the evaluation PCBs utilized to build the BM-CDR, unless otherwise specified, have the following general description. All differential input and outputs [mounted with SubMiniature version A (SMA) radio frequency (RF) connectors] are dc coupled and terminated on chip with 50 Ω resistors to ground. The outputs may be used in either single-ended or differential modes, and could be ac or dc coupled into 50 Ω resistors connected to ground. All these components are designed to support data transmission rates up to 13 Gb/s and clock frequencies as high as 13 GHz. The output amplitude voltage peak-to-peak is 550 mVp-p single-ended and 1100 mVp-p differential. The PCBs also feature an output level control pin V_{R}, which allows for loss compensation or for signal optimization. They all have an input and output return loss of 10 dB. Finally, all the chips operate from a single −3.3-V dc supply and are available in either 16 or 24 lead ceramic RoHS[1] compliant 3×3 mm (9 mm^2) or 4×4 mm (16 mm^2) surface-mount technology (SMT) packages, respectively.

Here we provide the implementation details necessary to interface the different building blocks correctly. We look at each one in turn:

1) 1:3 Fanout Buffer: The HMC940LC4B from Hittite Microwave draws 133 mA dissipat-

[1]Restriction of hazardous substances directive

ing 440 mW of power. It has a small signal gain of 20 dB. The propagation delay t_d, from the input to the output is 101 ps whereas the skew between the output replicas is ± 3 ps. The output rise and fall times (20%–80%) t_r and t_f, of this device are 26 and 25 ps, respectively. This PCB may be directly interfaced with the proceeding blocks.

2) ϕ-shifters: The HMC538LP4 from Hittite Microwave are analog phase shifters which are controlled via an analog control voltage from 0 to +5 V. They provide a continuously variable phase shift of 0 to 800 degrees at 6 GHz, and 0 to 450 degrees at 16 GHz, with consistent insertion loss versus phase shift. The phase shift is monotonic with respect to control voltage and the control port has a modulation bandwidth of 50 MHz. The typical insertion loss is 8 dB, whereas the return loss (input and output) is 7 dB. It has a phase voltage sensitivity of 120 deg/volt. This chip is housed in leadless quad-flat no-leads (QFN) surface mount packages and is available in both standard and RoHS compliant versions. This PCB may be directly interfaced with the proceeding boards.

3) Alexander PD: The HMC6032LC4B requires 220 mA of supply current and has an output rise/fall time (20%–80%) t_r/t_f, of 17 ps. It is designed to support data transmission rates up to 20 Gb/s, and clock frequencies as high as 20 GHz. All differential inputs are current mode logic (CML) and terminated on-chip with 50 Ω to the positive supply (ground), and may be ac or dc coupled. The differential CML outputs are source terminated to 50 Ω and may also be ac or dc coupled. Outputs can be connected directly to a 50 Ω ground-terminated system or drive devices with CML logic input.

On the other hand, the differential phase output signals that provide the early-late information X and Y, are terminated on-chip to ground with 400 Ω resistors. The open circuit output voltage swing on X and Y is 160 mVp-p differential. The problem is that X and Y cannot be connected to the following stage (AND gate of the phase picker) directly. This is because the inputs it connects to are, as stated before, terminated with 50 Ω resistors to ground. Thus the output voltage swing on X and Y is reduced by a factor of 9 compared to the open circuit voltage, that is, ∼17 mVp-p. Consequently, the output X and Y will not be able to provide the required 4-8 mA of sink/source current to drive the 50 Ω load. In order to solve this problem, we built an interface buffer circuit that would isolate X and Y by providing a high-input impedance while at the same time sourcing enough current to drive the phase picker AND gate inputs.

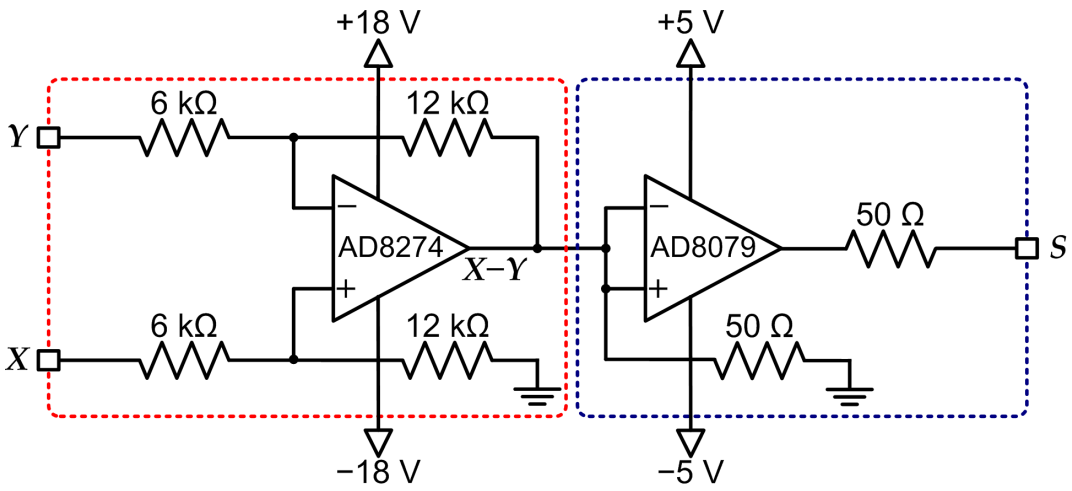


Fig. 3.20 Interface circuit for driving 50 Ω loads with 400 Ω sources and low input amplitude.

First, as shown in Fig. 3.20, we used a 10-MHz very low distortion amplifier from Analog Devices (Part #AD8274). It can be configured with no external components, as a gain $G = 1/2$ or $G = 2$ precision difference amplifier. We configured it with $G = 2$ to convert the differential signals X and Y to single-ended. Next, as illustrated in Fig 3.20, we employed a 260 MHz video buffer also from Analog Devices (Part #AD8079) with high input impedance. We configured it in unity-gain (noninverting) configuration, to drive the 50 Ω load of the AND gate. To input pins are tied together to minimize peaking. The AD8274 requires 2.6 mA supply current, consuming 94 mW from a ±18-V dc supply whereas the AD8079, offers low power of 50 mW by drawing 5 mA from a ±5-V dc supply while delivering 70 mA of load current. Both the chips are packaged in a small 8-pin small-outline integrated circuit (SOIC) package. We note that this would not be part of a commercial product and would not be needed if the main blocks were integrated on a single PCB or a single ASIC.

4) AND Gate: The HMC722LC3C from Hittite Microwave requires 70 mA supply current, consuming 230 mW of power. It has a small signal gain of 27 dB. The propagation delay t_d, from the input to the output is 95 ps. The devices has output rise and fall times (20%–80%) t_r and t_f, of 19 and 18 ps, respectively. This PCB may be directly interfaced with the 2:1 Selector.

5) 2:1 Selector: The HMC678LC3C from Hittite Microwave draws 76 mA dissipating 250 mW of power. The propagation delay t_d, from the input to the output is 125 ps whereas the propagation delay from the select to data output is 135 ps. The setup and hold time t_{SH}, of the device is 6 ps with the output rise and fall times (20%–80%) t_r and t_f, of 19 and 18 ps, respectively. This PCB may be directly interfaced with the decision circuit.

6) D-FF: The 13701DF from Inphi operates from a single +3.3-V supply and dissipates 300 mW. The part is nominally positive-edge triggered; however, by reversing the positive and negative clock connections, a negative-edge triggered application can be accommodated. The propagation delay t_d, from the input to the output is 110 ps. It has output rise and fall times (20%–80%) t_r and t_f, of 15 and 20 ps, respectively. The setup and hold time t_{SH}, for the device is 7 ps.

Author's Contribution

The author of this thesis designed the BM-CDR and carried out the hardware implementation.

Acknowledgment

The author would like to acknowledge the following individuals. Richard Karlquist, Agilent Technologies, for proposing the interface circuitry and technical advice. Bruce Massey, Hittite Microwave Corporation, for his suggestions on the interface circuitry and technical advice.

3.5 Conclusion

In this chapter, we demonstrated two novel BM-CDR architectures based on semiblind oversampling in both the time and space domain. The architectures are based on a hybrid topology, composed of a feedback (phase-tracking) CDR and a feed-forward CPA. We detailed the high-level architecture, the phase picking algorithm, and the hardware implementation of the proposed BM-CDRs. These BM-CDRs have been designed to achieve error-free operation (BER $< 10^{-10}$) while featuring instantaneous (0 preamble bit) clock

phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts; thus, improving the efficiency of upstream PON traffic, and increasing the effective throughput of the system by raising the information rate.

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[4] B. Razavi, *Design of Integrated Circuits for Optical Communication Systems*. New York: McGraw-Hill, 2003.

Chapter 4

Probabilistic Theory of BM-CDRs

4.1 Introduction

THE factors giving rise to errors are random processes and thus its mathematical treatment is based on probabilities and stochastic processes. In this chapter, we develop a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$ oversampling CDRs. The theoretical model quantitatively explain the performance of these circuits in terms of the BER and packet loss ratio (PLR). The model account for the following parameters: (1) silence periods, including phase steps and the length of consecutive identical digits (CIDs) between successive upstream passive optical network (PON) bursts from independent optical network units (ONUs); (2) finite frequency offset between the sampling clock and desired bit rate; (3) preamble length; (4) jitter on the sampling clock; and (5) pattern correlator error-resistance. It should be noted that the model developed here represents the theoretical minimum and maximum bounds, and should not be confused with the performance of an actual circuit as it may vary depending on the implementation from one process or technology to another.

The rest of the chapter is organized as follows. First, in Section 4.2 we state the assumptions and describe the general framework in which we develop the probailistic theory to model the BM-CDRs. Next, Sections 4.3 and Section 4.4 are devoted to the derivation of the probailistic theory by quantifying the performance of these circuits in terms of the BER and PLR, respectively. Finally, the chapter is concluded in Section 4.5.

The work presented in this chapter is a result of the research published in [1, 2].

4.2 Framework

Since all ONUs derive their timing information from the downstream optical line terminal (OLT) signal, we will assume that these circuits are already in frequency lock. In addition, we note that the model presented is for data transmitted in non-return to zero (NRZ) format, and it is independent of the bit rate and pulse shape, as long as the pulses are such that the intersymbol interference (ISI) at the sampling point is negligible. This will remain valid at high bit rates, as long as the channel remains limited by Gaussian noise, and not by severe distortion of the eye diagram resulting in closure at the sampling point [3].

Jitter can be interpreted as the perturbations of the threshold-crossing time of data transitions from their ideal position in time. Jitter affects the overall quality of the signal at the receiver in three ways [4]: (1) stability of the rise and fall times of the data bits; (2) stability of the rise and fall slopes of the data bits; and (3) stability of the width of the data bits. A part of the jitter of the data is inherited as phase uncertainty of the recovered sampling clock in the clock recovery circuit. As a result, the regenerated (retimed) data sequence by the CDR may be erroneous, degrading the BER and PLR performance. Jitter is in general classified into two main categories, namely, random jitter and deterministic jitter.

Random jitter (RJ) is unpredictable, unbounded, and results from physical noise sources based on random processes. The most prevalent RJ mechanism is thermal noise, however, other causes include shot noise, and flicker ($1/f$) noise. The generation of RJ is approximated to a Gaussian probability distribution. This follows from the central limit theorem (CLT) which states conditions under which the mean of a sufficiently large number of independent random variables, each with finite mean and variance, will be approximately normally distributed [5]. The Gaussian approximation is sufficiently accurate for design purposes and is far easier to evaluate than the more exact probability distribution within the receiver [6]. Furthermore, the receiver sensitivities calculated by using Gaussian approximation are generally within 1 dB of those calculated by other methods [7]. RJ is characterized by the standard deviation or the root mean square (RMS) value of the Gaussian probability distribution.

Deterministic jitter (DJ) is predictable, bounded, and is attributed to several causes such as duty cycle distortions (DCD), and initial frequency offset (when a clock from free-running tries to lock in a reference clock). This type of jitter, being deterministic and not

random, cannot be described by distributions. DJ is further classified as ISI and data-dependent jitter (DDJ), pulse-width-distortion jitter (PWDJ), sinusoidal jitter (SJ), and uncorrelated bounded jitter (UBJ). The effect of DJ is to shrink the data eye by a finite amount and will only further deteriorate the performance of the BM-CDR or CDR—device under test (DUT). Thus, in order to simplify the derivation of the theoretical models and the corresponding theoretical analysis, DJ is ignored.

In deriving the theoretical probabilistic model, we make use of continuous random variables $\widetilde{x}$, that follow a Gaussian distribution denoted as $\widetilde{x} \sim \mathcal{N}(\mu, \sigma^2)$, where μ is the mean, $\sigma > 0$ is the standard deviation, and the probability density function (PDF) $f(x)$ of $\widetilde{x}$, is given by

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right), \quad x \in \mathbb{R} \tag{4.1}$$

with the following characteristics: $f(x) > 0$, for all x and $\int_{-\infty}^{+\infty} f(x)dx = 1$.

4.3 Bit Error Rate Probability Model

In the context of clock and data recovery, we define the following continuous random variables with a Gaussian distribution:

- $\widetilde{\xi} \sim \mathcal{N}(0, \sigma_{t_s}^2)$, with PDF $f(\xi)$, is the jitter on the edges of the data bits with a zero mean, where σ_{t_s} corresponds to the RMS jitter on the sampling clock signal;
- $\widetilde{t_s} \sim \mathcal{N}(\widetilde{t_o}, \sigma_{t_s}^2)$, with PDF $f(t_s)$, is the *actual* clock sampling point in the presence of random jitter; and
- $\widetilde{t_o} \sim \mathcal{N}(t_o^{\text{ideal}}, \sigma_{t_o}^2)$, with PDF $f(t_o)$, is the clock sampling point *determined* by the CDR, where t_o^{ideal} is the *ideal* clock sampling point in the middle of the data bit, and $\sigma_{t_o}^2 = \kappa\sigma_{t_s}^2$, with κ being a constant of proportionality.

For convenience, the left and right edges of the data eye are located at $-T_b/2$ and $+T_b/2$, about the center of the data bit, respectively, as portrayed in Fig. 4.1(a). Thus, the

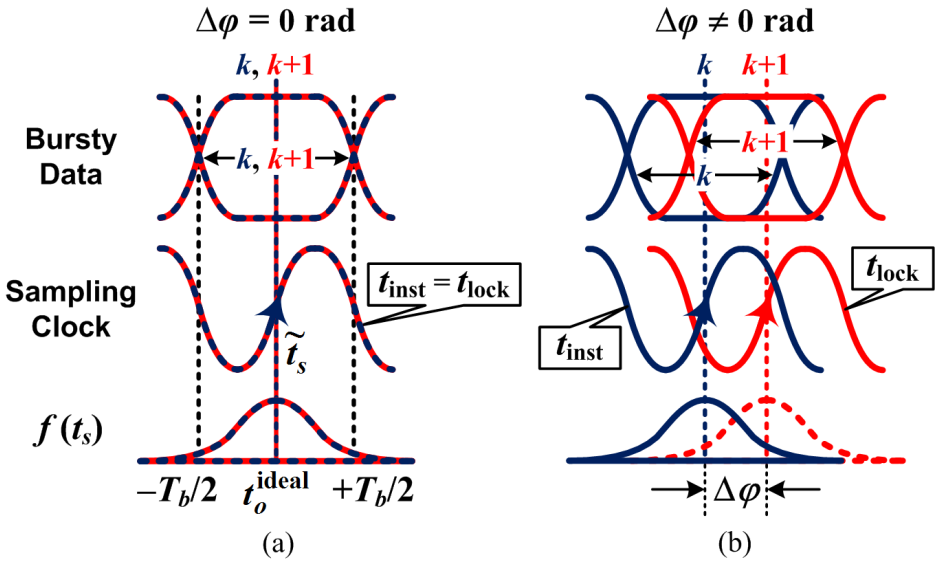


Fig. 4.1 Graphical depiction of the actual clock sampling point $\widetilde{t}_s$, in the presence of random jitter, and the associated probability density function $f(t_s)$, when the phase difference: (a) $\Delta\varphi = 0$ rad; and (b) $\Delta\varphi \neq 0$ rad.

expectation (mean) of the clock sampling point is given by

$$E\left[\widetilde{t}_o\right] \triangleq \int_{-\infty}^{+\infty} t_o f(t_o) dt_o = t_o^{\text{ideal}} = 0 \tag{4.2}$$

as the ideal clock sampling point is in the center of the data eye. Let $\widetilde{\xi}_j^{\text{left}}$ and $\widetilde{\xi}_j^{\text{right}}$ be the timing jitter on the left edge and right edge of the j^{th} bit of an l-bit preamble. We assume that $\widetilde{\xi}_j^{\text{left}}$ and $\widetilde{\xi}_j^{\text{right}}$ are independent (as the rise and fall times are uncorrelated) with common RMS jitter σ_{t_s}. Then the mid-point of the j^{th} bit $\widetilde{\tau}_j$, is expressed as

$$\widetilde{\tau}_j = \frac{\widetilde{\xi}_j^{\text{left}} + \widetilde{\xi}_j^{\text{right}}}{2}. \tag{4.3}$$

After the l-bit preamble, the clock sampling point determined by the CDR $\widetilde{t}_o$, at the first bit where the decision circuit will start sampling the data bits, is given by the average of

the individual mid-points in (4.3) as

$$\widetilde{t_o} = \frac{1}{(l+1)} \sum_{j=1}^{l+1} \widetilde{\tau}_j. \tag{4.4}$$

Subsequently, σ_{t_o} can be related to the sampling clock RMS jitter σ_{t_s}, as follows:

$$\begin{aligned}
\sigma_{t_o}^2 &\triangleq E\left[\left(\widetilde{t_o} - \underbrace{E[\widetilde{t_o}]}_{=0}\right)^2\right] \\
&= E\left[\left(\frac{1}{(l+1)} \sum_{j=1}^{l+1} \widetilde{\tau}_j\right)^2\right] \\
&= \frac{1}{4(l+1)^2} \left\{ \sum_{j=0}^{l} \left(\underbrace{E\left[\left(\widetilde{\xi}_j^{\text{left}}\right)^2\right]}_{=\sigma_{t_s}^2} + \underbrace{E\left[\left(\widetilde{\xi}_j^{\text{right}}\right)^2\right]}_{=\sigma_{t_s}^2} + 2\underbrace{E\left[\widetilde{\xi}_j^{\text{left}} \cdot \widetilde{\xi}_j^{\text{right}}\right]}_{=0 \text{ (uncorrelated)}} \right) \right\} \\
&= \underbrace{\frac{1}{2(l+1)}}_{=\kappa} \sigma_{t_s}^2.
\end{aligned} \tag{4.5}$$

Hence, the PDFs of the actual clock sampling point $f(t_s)$, and the clock sampling point determined by the CDR $f(t_o)$, can be expressed as:

$$f(t_s) = \frac{1}{\sqrt{2\pi}\sigma_{t_s}} \exp\left(-\frac{\left(t_s - \widetilde{t_o}\right)^2}{2\sigma_{t_s}^2}\right); \tag{4.6}$$

$$f(t_o) = \frac{1}{\sigma_{t_s}} \sqrt{\frac{(l+1)}{\pi}} \exp\left(-\frac{(l+1)t_o^2}{\sigma_{t_o}^2}\right). \tag{4.7}$$

The probability that the clock sampling point determined by the CDR $\widetilde{t_o}$, will be within the data eye after l preamble bits is given by

$$\begin{aligned}
\Pr\left(|\widetilde{t_o}| < \frac{T_b}{2}\right) &= \int_{-T_b/2}^{+T_b/2} f(t_o) dt_o \\
&= 1 - 2Q\left(\frac{1}{\sigma_{t_s}[\text{UI}]} \sqrt{\frac{(l+1)}{2}}\right)
\end{aligned} \tag{4.8}$$

where $Q(\cdot)$, called the "Q function", is the normalized Gaussian-tail probability defined as

$$Q(x) \triangleq \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp\left(-\frac{\lambda^2}{2}\right) d\lambda. \tag{4.9}$$

Note that (4.8) has been made independent of the data rate. Thus, the RMS jitter σ_{t_s}, is expressed in terms of the unit interval (UI); 1 UI corresponds to a 1-bit period T_b. In Fig. 4.2 we plot, (4.8) as a function of the RMS jitter σ_{t_s}, for different preamble lengths. It can be observed that the probability $\Pr\left(\left|\widetilde{t_o}\right| < T_b/2\right)$, decreases with increasing jitter but can be compensated by increasing the preamble length. Also, for $\sigma_{t_s} \leq 0.25$ UI, $\Pr\left(\left|\widetilde{t_o}\right| < T_b/2\right) \sim 1$ even with no preamble bits.

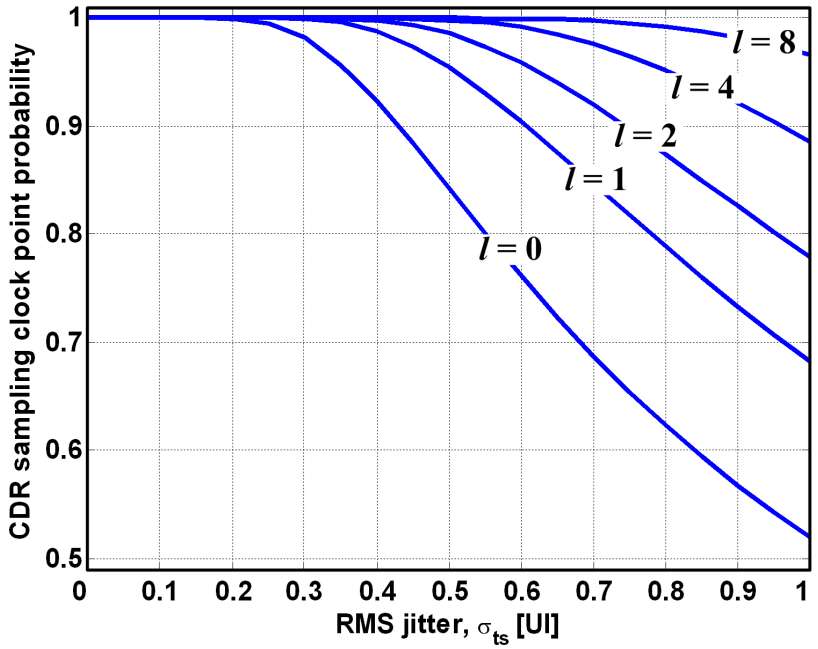


Fig. 4.2 Probability of the clock sampling point determined by the CDR $\widetilde{t_o}$, to be within the data bit after an l-bit preamble.

When there is no phase difference $\Delta\varphi = 0$ rad, between two consecutive packets in a PON uplink as depicted in Fig. 4.1(a), the CDR's sampling error probability is equivalent to the probability that the clock transition occurs either before the leading data transition or after the trailing data transition, $\Pr\left(\left|\widetilde{t_s}\right| > T_b/2\right)$, given that the sampling point determined by the CDR $\widetilde{t_o}$, is within the data eye. Assuming uncorrelated data with equiprobable ONEs

and ZEROs, the sampling error probability P_s, of the CDR can be expressed as

$$P_s = \frac{1}{2}\Pr\left(|\widetilde{t_o}| < \frac{T_b}{2}\right)\Pr\left(|\widetilde{t_s}| \geq \frac{T_b}{2}\right) \tag{4.10}$$

where

$$\Pr\left(|\widetilde{t_s}| \geq \frac{T_b}{2}\right) = \int_{-\infty}^{-T_b/2} f(t_s)dt_s + \int_{+T_b/2}^{+\infty} f(t_s)dt_s. \tag{4.11}$$

Ideally, the sampling clock must bear a well-defined phase relationship with respect to the received data so that the decision circuit samples each bit at the mid-point of the data eye. Thus, it is desirable that the CDR clock sampling point be as close as possible to the ideal clock sampling point, $\widetilde{t_o} \sim t_o^{\text{ideal}} = 0$. Also, since the PDF $f(t_s)$, is even-symmetric, then

$$\Pr\big(\widetilde{t_s} < -\frac{T_b}{2}\big) = \Pr\big(\widetilde{t_s} > +\frac{T_b}{2}\big) \tag{4.12}$$

and the sampling error probability is given as

$$P_s = Q\left(\frac{T_b}{2\sigma_{t_s}}\right). \tag{4.13}$$

4.3.1 Finite Phase Step Consideration

With a finite phase difference $\Delta\varphi \neq 0$ rad, between the consecutive packets as illustrated in Fig. 4.1(b), the phase step has the effect of displacing the instantaneous sampling clock determined by the CDR t_{inst}, by $|\Delta\varphi|(T_b/2\pi)$. By inserting preamble bits, the CDR feedback loop will have time to settle down. Specifically, after an l-bit preamble, the clock sampling point determined by the CDR $\widetilde{t_o}$, will be displaced by

$$t_{|\Delta\varphi|} = |\Delta\varphi|\big(1 - \eta(l)\big)\frac{T_b}{2\pi} \tag{4.14}$$

where the response of the phase-locked loop (PLL) $\eta(l)$, relates the phase of the recovered sampling clock ϕ_{osc}, to an input phase step ϕ_{in}, as

$$\eta(l) = \frac{\phi_{\text{osc}}}{\phi_{\text{in}}} \tag{4.15}$$

with

$$\phi_{\text{in}} = \Delta\varphi \cdot u(t), \quad \text{for } t > 0 \tag{4.16}$$

and the unit step function is

$$u(t) = \begin{cases} 0, & \text{if } t < 0 \\ 1, & \text{if } t > 0. \end{cases} \tag{4.17}$$

Note that the expression for $t_{|\Delta\varphi|}$ is only valid for phase steps $|\Delta\varphi| \leq \pi$ rad, and does not account for $\pi < |\Delta\varphi| \leq 2\pi$ rad. Thus, a correcting factor ψ, must be introduced to account for the symmetrical performance about the edges of the data bit at $-T_b/2$ and $+T_b/2$. Hence, the displacement $t_{|\Delta\varphi|}$, of the clock sampling point determined by the CDR $\widetilde{t_o}$, after an l-bit preamble can be expressed as

$$t_{|\Delta\varphi|} = \Big[\big(|\Delta\varphi| - \psi\big)\big(1 - \eta(l)\big)\Big]\frac{T_b}{2\pi} \tag{4.18}$$

where

$$\psi = \begin{cases} 0, & \text{if } |\Delta\varphi| \leq \pi \text{ rad} \\ 2\pi, & \text{if } \pi < |\Delta\varphi| \leq 2\pi \text{ rad}. \end{cases} \tag{4.19}$$

For a CDR based on a second-order PLL, $\eta(l)$ is analytically derived to be [8]

$$\eta(l) = 1 - \exp\left(-l\zeta\omega_n T_b\right) \times \Bigg\{\cosh\left(l\omega_n T_b\sqrt{\zeta^2 - 1}\right) - \frac{\zeta}{\sqrt{\zeta^2 - 1}}\sinh\left(l\omega_n T_b\sqrt{\zeta^2 - 1}\right)\Bigg\}, \quad \text{for } \zeta > 0 \tag{4.20}$$

where ζ is the "damping ratio" and ω_n in [rad/s] is the "natural frequency", both being functions of the CDR circuit parameters: charge-pump current; capacitance of the low-pass filter (LPF); gain of the voltage-controlled oscillator (VCO); and data transition density [9]. Appendix 4.6 describes a baseband model of a PLL-based CDR which can be used to customized to create specific synchronous optical network (SONET) CDR models running at a given frequency. Based on this equations, we can determine the parameters of these

CDRs.

It follows from (4.18), that the PDF $f(t_s)$ in (4.6), can therefore be modified to account for this phase step as

$$f(t_s) = \frac{1}{\sqrt{2\pi}\sigma_s} \exp\left(-\frac{\left(t_s - \widetilde{t_o} \mp t_{|\Delta\varphi|}\right)^2}{2\sigma_{t_s}^2}\right) \tag{4.21}$$

Thus, the probability that the clock transition occurs either before the leading data transition or after the trailing data transition can then be expressed as

$$\Pr\left(|\widetilde{t_s}| \geq \frac{T_b}{2}\right) = \frac{1}{2}\left\{Q\left(\frac{\frac{T_b}{2} - \widetilde{t_o} - t_{|\Delta\varphi|}}{\sigma_{t_s}}\right) + Q\left(\frac{\frac{T_b}{2} - \widetilde{t_o} + t_{|\Delta\varphi|}}{\sigma_{t_s}}\right)\right\}. \tag{4.22}$$

Before we proceed, we make two assumptions: (1) the clock sampling point determined by the CDR is ideally located at the center of the data eye ($\widetilde{t_o} = 0$) *before* a phase step $|\Delta\varphi|$; and (2) the RMS jitter on the clock signal $\sigma_{t_s} \leq 0.25$ UI, implying the probability that the CDR clock sampling point is within the data eye *after* the phase step is $\Pr\left(|\widetilde{t_o}| < T_b/2\right) \sim 1$, for any number of preamble bits l. Consequently, for a given phase step $|\Delta\varphi| \leq 2\pi$ rad, the sampling error probability P_s, in (4.10) can be expressed as

$$P_s\big(|\Delta\varphi|\big) = \frac{1}{2}\Bigg\{Q\left(\frac{\pi - \big(|\Delta\varphi| - \psi\big)\big(1 - \eta(l)\big)}{2\pi\sigma_{t_s}[\text{UI}]}\right) + Q\left(\frac{\pi + \big(|\Delta\varphi| - \psi\big)\big(1 - \eta(l)\big)}{2\pi\sigma_{t_s}[\text{UI}]}\right)\Bigg\}. \tag{4.23}$$

Recall from Chapter 3 that time domain oversampling is achieved by utilizing the clock recovered by the CDR with a frequency N *times* the bit rate, whereas space domain oversampling is achieved by utilizing N equally spaced mutliphase versions of the clock recovered by the CDR with a frequency *equal* to the bit rate. In either case, the absolute value of the maximum phase difference between the ideal sampling point t_o^{ideal}, and the N oversampling points derived from the CDR's recovered clock $\widetilde{t_o}$ is,

$$\max\big(|t_o^{\text{ideal}} - \widetilde{t_o}|\big) = \frac{T_b}{2N} \equiv \frac{\pi}{N}\ [\text{rad}]. \tag{4.24}$$

For $t_o^{\text{ideal}} = 0$, the N-clock sampling points $t_o^n|_N$, derived from the CDR's recovered clock are located at:

$$\widetilde{t_o} \in \Big\{t_o^n|_N\Big\} = \Big\{\frac{\pi}{N}(2n+1-N)\Big\}, \quad \text{for } n = 0, 1, \ldots, N-1. \tag{4.25}$$

For each of the N samples, the sampling error probabilities $P_s^n|_N$, can be calculated by convolving $P_s\big(|\Delta\varphi|\big)$ in (4.23), with the N-sampling points $t_o^n|_N$ in (4.25), as

$$P_s^n|_N = P_s\big(|\Delta\varphi|\big) \otimes \delta\big(|\Delta\varphi| - t_o^n|_N\big) \tag{4.26}$$

where

$$\delta\big(|\Delta\varphi| - t_o^n|_N\big) \triangleq \begin{cases} 1, & \text{if } |\Delta\varphi| = t_o^n|_N \\ 0, & \text{if } |\Delta\varphi| \neq t_o^n|_N. \end{cases} \tag{4.27}$$

is the Dirac-delta function. It follows from the sifting property

$$\begin{aligned} P_s^n|_N &= \int_{-\infty}^{+\infty} P_s\big(|\Delta\varphi| - \lambda\big)\delta\big(\lambda - t_o^n|_N\big)d\lambda \\ &= P_s\big(|\Delta\varphi| - t_o^n|_N\big). \end{aligned} \tag{4.28}$$

Our proposed BM-CDR architectures are based on semiblind oversampling in either the time domain or the space domain. In time oversampling, N *data* samples are forwarded the CPA, whereas in space oversampling, N *clock* samples are forwarded to the CPA for picking the correct phase. The phase picking algorithm for time oversampling is based on selecting the best data sample by relying on a simple comparison with a known pattern. On the other hand, the phase picking algorithm for space oversampling determines the clock sample closest to the center of the data eye. It follows that the sampling error probability of the BM-CDRs based on semiblind oversampling $P_s^{\text{BM-CDR}}$, can be mathematically expressed as the minimum of the sample set

$$P_s^{\text{BM-CDR}}\Big|_{N\times} = \min\Big\{P_s\big(|\Delta\varphi| - t_o^n|_N\big)\Big\}. \tag{4.29}$$

Note that $\min A$ or $\min_i a_i$ denotes the minimum value of a set of elements $A = \{a_i\}_{i=1}^N$. Figs. 4.3(a) and 4.3(b) illustrate a 2-$\times$ oversampling in the time and space domain, re-

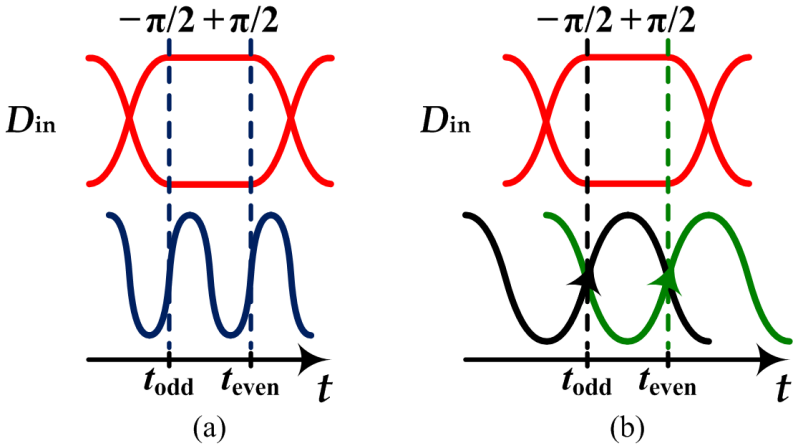


Fig. 4.3 2×-oversampling in the: (a) time domain; and (b) space domain.

spectively. In time domain scheme, the clock samples the data at frequency twice of the bit rate, whereas in space domain scheme, the two multiphase sampling clocks have a frequency equal to the bit rate. In either case, these two resulting sampling points, odd t_{odd} and even t_{even}, are located at $-\pi/2$ rad and $+\pi/2$ rad about the center of the data eye, respectively, as per (4.25) for $N = 2$. Consequently, for our proposed BM-CDRs based on the 2×-semiblind oversampling, where the CPA selects the correct set of samples (odd or even) with the aid of a phase picking algorithm, the sampling error probability $P_s^{\text{BM-CDR}}$, is given by

$$P_s^{\text{BM-CDR}}\Big|_{2\times} = \min\Big\{P_s^{odd}, P_s^{even}\Big\} \tag{4.30}$$

where

$$P_s^k = P_s\big(|\Delta\varphi| - t_k\big), \tag{4.31}$$

for

$$t_k = \begin{cases} -\pi/2 \text{ rad}, & \text{if } k \equiv odd \\ +\pi/2 \text{ rad}, & \text{if } k \equiv even \end{cases} \tag{4.32}$$

Finally, we define the BER, denoted as P_e, of the CDR and the BM-CDR, from the sampling

error probabilities in (4.23) and (4.30), respectively, as follows:

$$\text{BER} \equiv P_e \triangleq \begin{cases} P_s\big(|\Delta\varphi|\big), & \text{for CDR} \\ \min\Big\{P_s^{odd}, P_s^{even}\Big\}, & \text{for BM-CDR.} \end{cases} \tag{4.33}$$

4.3.2 Finite Frequency Offset Consideration

Recall from Section 2.5.2 that the silence period T_s, between two consecutive bursts from independent ONUs, consists, in addition to a phase step, an all-zero sequence of m CIDs, expressed as

$$T_s = \left(m + \frac{\Delta\varphi}{2\pi}\right) T_b \tag{4.34}$$

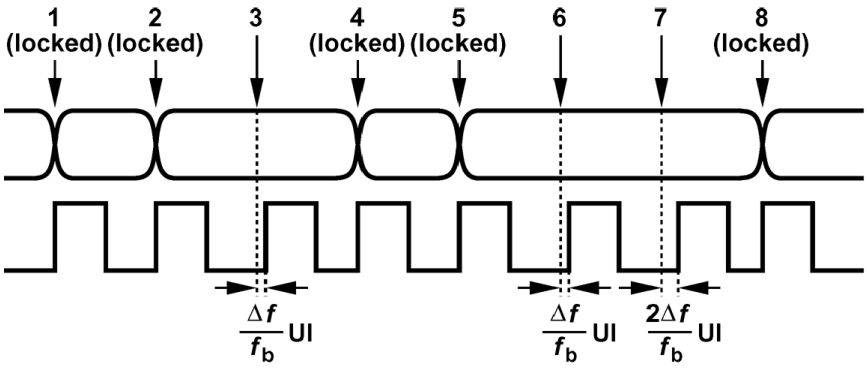
The presence of CIDs can cause the frequency of the local oscillator (LO), usually implemented as a crystal, to inevitably drift from the desired bit rate by a few tens of parts-per-million (PPM) such that the recovery of data would no longer be possible. The frequency error thus accumulates during consecutive runs of ONEs or ZEROs, resulting in jitter in the time domain. To quantify jitter, frequency deviation Δf, is defined as [10]

$$\Delta f = f_b - K f_{\text{ref}} \tag{4.35}$$

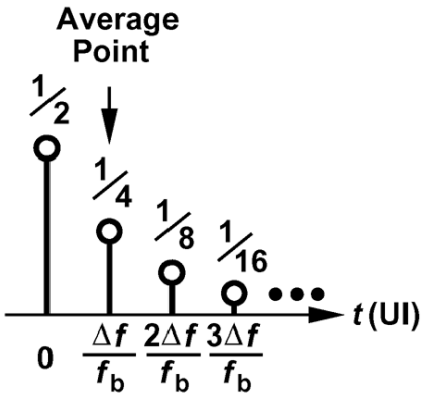
where $f_b = 1/T_b$ is the data rate, f_{ref} is the reference frequency, and K is the corresponding divide ratio. Since Δf is typically less than f_b, the sampling clock zero crossing shifts by $\Delta f/f_b$ per bit period during long runs [10] as depicted in Fig. 4.4(a) (see positions 3, 6, and 7). It is assumed that the clock zero crossings align to data transition immediately whenever it occurs (see positions 1, 2, 4, 5, and 8). For m CIDs, the phase error $\Delta\varphi_e$, between two consecutive bursts can accumulate up to'

$$\Delta\varphi_e = 2\pi k(m-1)\frac{\Delta f}{f_b} \tag{4.36}$$

in the last bit. For a CDR that uses both the rising and falling edge of the input data to adjust the clock phase, $k = 1$; in the case where the CDR uses only the rising or falling edge of the data input, $k = 2$ [11]. In the worst-case when the phase error $|\Delta\varphi_e|$ exceeds



(a)



(b)

Fig. 4.4 Finite frequency offset model [10]. (a) Phase error due to finite frequency offset for different data pattern. (b) Probability of zero-crossing positions.

π rad, the maximum tolerable length of CIDs $m_{\max}$, in the presence of frequency offset is given by

$$m_{\max} = \frac{1}{2k}\left|\frac{f_b}{\Delta f}\right| + 1. \tag{4.37}$$

This is of course an optimistic estimation since noise, in particular VCO phase noise, would deteriorate the result considerably.

Moreover, for a random sequence, the probability of occurring a phase deviation of $n\Delta f/f_b$ is equal to $2^{-(n+1)}$. Fig. 4.4(b) illustrates the probability distribution. That is, the clock zero-crossing points accumulate at equally-spaced positions with different probabili-

ties, and the average position is therefore given by

$$\frac{\Delta f}{f_b}\sum_{n=0}^{\infty}\frac{n}{2^{n+1}}=\frac{\Delta f}{f_b}. \tag{4.38}$$

The RMS jitter on the sampling clock due to this effect can be derived to be [10]

$$\begin{aligned}\sigma_{t_s}&=\left[(-1)^2\cdot\frac{1}{2}+0^2\cdot\frac{1}{4}+1^2\cdot\frac{1}{8}+2^2\cdot\frac{1}{16}+\cdots\right]^{1/2}\times\left|\frac{\Delta f}{f_b}\right|\\&=\left(\frac{1}{2}+0+\sum_{n=1}^{\infty}n^2\cdot\frac{1}{2^{n+2}}\right)^{1/2}\times\left|\frac{\Delta f}{f_b}\right|\\&=\sqrt{2}\left|\frac{\Delta f}{f_b}\right|.\end{aligned} \tag{4.39}$$

4.4 Relationship to Packet Loss Ratio

We now theoretically relate the PLR performance of the receiver to the BER performance. The BER will affect the bits in the packet delimiter. If the delimiter is not being correctly detected, the packet is declared lost, hence contributing to the packet loss count. The error resistance of the delimiter depends not only on its length, but also on the exact implementation of the pattern correlator. Let P_l^z represent the PLR obtained at a given BER of P_e with a pattern correlator having an error resistance of z bits in a d-bit delimiter. The PLR can then be estimated as

$$\mathrm{PLR}\equiv P_{l_z}\leq\sum_{j=z+1}^{d}\Pr(j)\sim\Pr(z+1)\ \text{ for }\ P_e\ll 1 \tag{4.40}$$

where $\Pr(x)$ gives the probability of finding x errors out of a d-bit delimiter given that the probability of finding a bit error is P_e, and can be expressed as a binomial distribution:

$$\Pr(x)=\binom{d}{x}P_e^x\left(1-P_e\right)^{d-x}. \tag{4.41}$$

4.5 Conclusion

In this chapter, we developed a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$ oversampling CDRs. The theoretical model quantitatively explains the performance of these circuits in terms of the BER and PLR. The model account for the following parameters: (1) silence periods, including phase steps and the length of CIDs between successive upstream PON bursts from independent ONUs; (2) finite frequency offset between the sampling clock and desired bit rate; (3) preamble length; (4) jitter on the sampling clock; and (5) pattern correlator error-resistance.

The model developed here is for data transmitted in NRZ format, and it is independent of the bit rate and pulse shape, as long as the pulses are such that the ISI at the sampling point is negligible. This will remain valid at high bit rates, as long as the channel remains limited by Gaussian noise. RJ, approximated to a Gaussian probability distribution, is account for in the model. The effect of DJ is to shrink the data eye by a finite amount and will only further deteriorate device under test's performance. Thus, in order to simplify the mathematical modeling, DJ is ignored. Furthermore, the model represents the theoretical minimum and maximum bounds, and should not be confused with the performance of an actual circuit as it may vary depending on the implementation from one process or technology to another.

4.6 Appendix

In this appendix, we review the baseband model of a conventional CDR that is well documented in literature [8, 12]. More specifically, we set up the equations that describe the baseband model of a PLL-based CDR. We then customize this generic model to create specific SONET CDR models, each running at a different frequency (2488.32, 4976.64, and 9953.28 Mb/s). Based on this equations, we determine the parameters of these CDRs such that they meet the jitter requirements of Telcordia GR-253-CORE [13].

Fig. 4.5(a) shows the schematic of a popular 3$^{\text{rd}}$-order charge-pump CDR architecture. The baseband CDR model illustrated in Fig. 4.5(c) assumes a linear model for the combination of the phase detector, charge-pump, and LPF. The baseband model further assumes that the VCO has a linear response. These assumptions only hold when the CDR is locked;

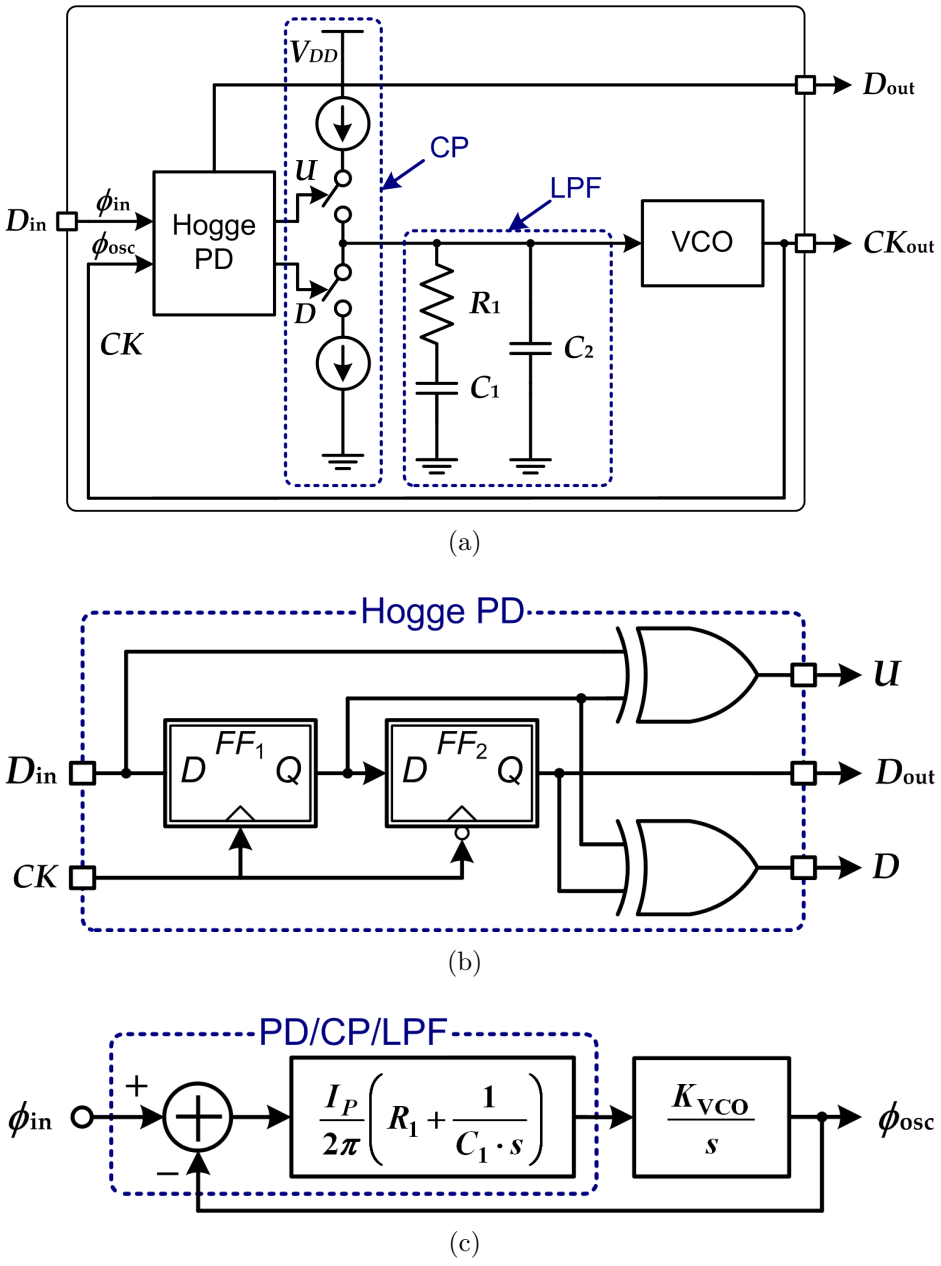


Fig. 4.5 Linear CDR model. (a) 3rd-order charge-pump CDR. (b) Hogge phase detector. (c) 2nd-order baseband model of the charge-pump CDR with C_2 neglected (s-domain model) [9]. (PD: phase detector; CP: charge pump; LPF: low-pass filter; VCO: voltage-controlled oscillator).

that is, the frequency of the input signal is close to the VCO frequency. Hence, we cannot use the baseband model to simulate the frequency acquisition time of a CDR starting from

an unlocked condition.

The jitter transfer requirements in Table 4.1 limit the amount of jitter on an input OC-N electrical signal that can be transferred to the output [13]. Jitter transfer is primarily of concern within two decades or less of the breakpoint in the jitter transfer mask. This is reflected in the values of f_L and f_H that appear in Fig. 4.6 and limit the jitter frequency range over which the following requirement applies. In particular, each value of f_L is a factor of 100 less than the breakpoint frequency (f_c)—jitter transfer bandwidth, and each value of f_H is either 10 or 80 times larger than f_c [13]. For SONET CDRs, the jitter transfer function shall be *under* the mask of Fig. 4.6. Note that J_P is the jitter peaking value.

Table 4.1 also lists the jitter tolerance requirements of SONET CDRs. For OC-N interfaces, jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes a 1-dB power penalty (BER $< 10^{-10}$). SONET compliant CDRs must have a jitter tolerance *above* the jitter tolerance mask of Fig. 4.7. Note that f_4 is the fourth corner frequency of the jitter tolerance mask ($f_4 = f_c/2$) and A_1 is the jitter amplitude at f_4.

Table 4.1 SONET specifications for the jitter transfer mask of Fig. 4.6 and the jitter tolerance mask of Fig. 4.7 [13]

SONET Rate	**Line Rate** [Mb/s]	**Jitter Transfer**		**Jitter Tolerance**	
		f_c [kHz]	J_P [dB]	f_5 [kHz]	A_1 [UIpp]
OC-48	2488.32	2000	0.1	1000	0.15
OC-192	9953.28	8000	0.1	4000	0.15
OC-768	39813.32	32000	0.1	16000	0.15

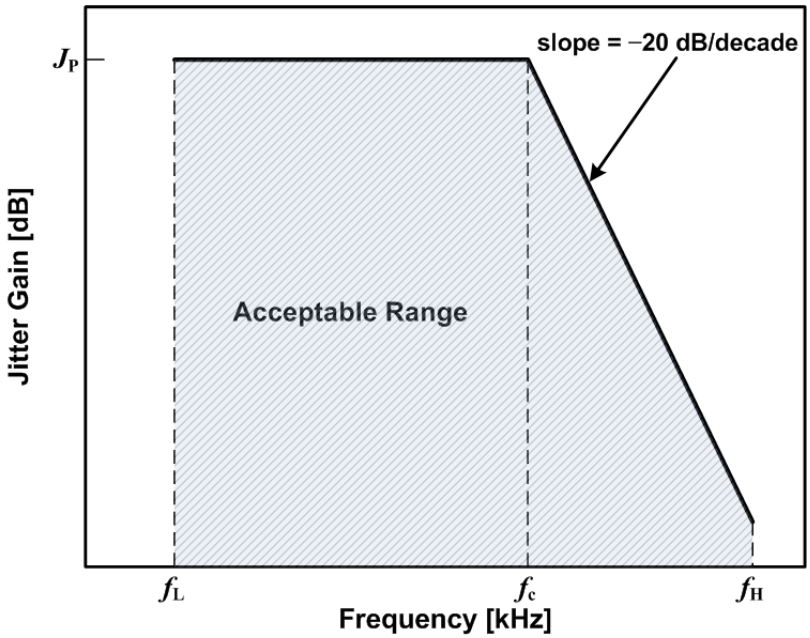


Fig. 4.6 SONET jitter transfer mask (category II) [13].

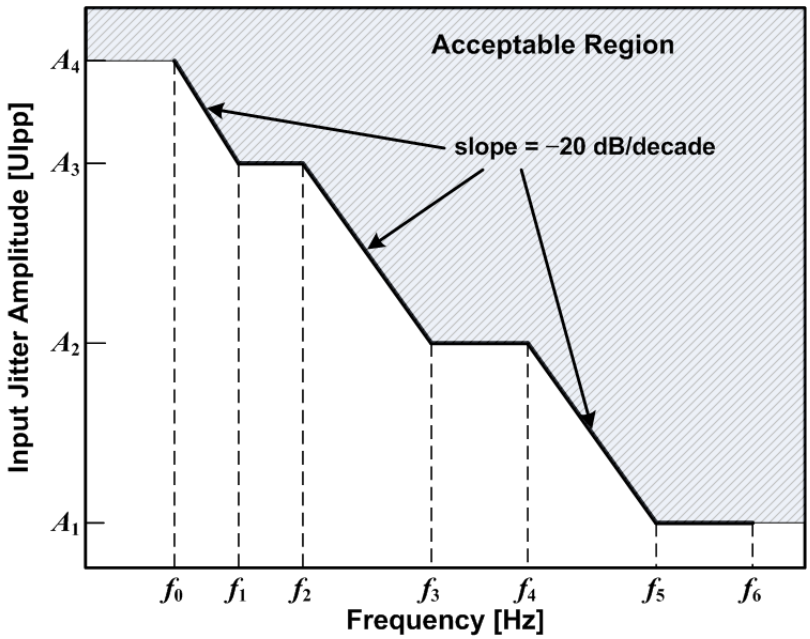


Fig. 4.7 SONET jitter tolerance mask (category II) [13].

In order to match the jitter requirements of Table 4.1, we treat the CDR as a linear feedback system. The open-loop transfer function of the CDR in Fig. 4.5(c) is

$$L(s) = \frac{\Phi_{\text{osc}}}{\Phi_{\text{in}}}\bigg|_{\text{open}} = \frac{I_P}{2\pi}\left(R_1 + \frac{1}{sC_1}\right)\frac{K_{\text{VCO}}}{s} \tag{4.42}$$

and its closed-loop transfer is

$$H(s) = \frac{\Phi_{\text{osc}}}{\Phi_{\text{in}}}\bigg|_{\text{closed}} = \frac{\frac{I_P K_{\text{VCO}}}{2\pi C_1}(sR_1C_1 + 1)}{s^2 + \frac{I_P}{2\pi}K_{\text{VCO}}R_1 s + \frac{I_P}{2\pi C_1}K_{\text{VCO}}} \tag{4.43}$$

where I_P is the current in charge-pump, and $K_m athrm VCO$ is the gain of the VCO. Note that we neglected C_2 in Fig. 4.5(c) in order to simplify the analysis. The main function of capacitor C_2 is to filter out the ripples at the input of the VCO. These ripples, in practice, cause jitter at the output of the VCO. If C_2 is smaller than one fifth to one tenth of C_1, the closed-loop time and frequency responses remain relatively unchanged [9].

We can rewrite the second-order transfer function of (4.43) in the form of $s^2+2\zeta\omega_n s+\omega_n^2$, as

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.44}$$

where ω_n, the "natural frequency" is given by

$$\omega_n = \sqrt{\frac{I_P D_T K_{\text{VCO}}}{2\pi C_1}} \tag{4.45}$$

and the "damping ratio" ζ, is

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P D_T C_1 K_{\text{VCO}}}{2\pi}}. \tag{4.46}$$

Note that in (4.45) and (4.46), the charge-pump is scaled by D_T to model the effect of data transition density on the gain of the phase detector. For example, the $1010\cdots$ has a transition density of 1; that is, the Hogge PD sees a transition on every rising edge of the clock. In the case of a pseudorandom binary sequence (PRBS) pattern, the transition density is 1/2. Using the closed-loop transfer function of (4.44), one can show that the

Table 4.2 Parameters for SONET compliant CDRs

SONET Rate	Line Rate [Mb/s]	CDR Parameter I_P [mA]	K_{VCO} [MHz/V]	R_1 Ω	C_1 [nF]	ζ [−]	ω_n [rad/s]
OC-48	2488.32	0.25	500	201.06	34.371	4.66	1.35×10^6
OC-192	9953.28	1	500	201.06	8.593	4.66	5.39×10^6
OC-768	39813.32	4	500	201.06	2.148	4.66	21.57×10^6

−3-dB bandwidth of the CDR is given by

$$\omega_{-3\text{dB}} = \sqrt{\left[(2\zeta^2+1) + \sqrt{(2\zeta^2+1)+4}\right]\omega_n^2}. \tag{4.47}$$

In order to guarantee loop stability, ζ must exceed $\sqrt{2}/2$. Moreover, as we will see in Table 4.2, ζ must be greater than 4.66 to ensure jitter peaking is less than 0.1 dB. If $2\zeta^2 \gg 1$, then (4.47) reduces to

$$\begin{aligned}\omega_{-3\text{dB}} &\approx 2\zeta\omega_n \\ &= \frac{R_1 I_P D_T K_{\text{VCO}}}{2\pi}.\end{aligned} \tag{4.48}$$

Jitter peaking J_P can be calculated using [9]

$$J_P = \frac{2.171}{\frac{R_1^2}{4} I_P D_T C_1 K_{\text{VCO}}} \tag{4.49}$$

Note that J_P is in dB. We will now use (4.48) and (4.49) to determine the physical parameters (I_P, K_{VCO}, R_1, and C_1) for the three SONET compliant CDRs. Since we have two equations for four unknowns, we must assume values for two of the parameters. In practice, the VCO may come from a library and have a predetermined sensitivity (K_{VCO}). We will assume a value of 500 MHz/V. Moreover, we assume that all three CDRs share the same VCO, as may be the case in a multirate CDR architecture. We finally assume a charge-pump current of $250\mu A$ for the OC-48 CDR; we scale this current for the OC-192 and OC-768 CDRs, respectively. This leaves us with two equations for two unknowns. To find R_1 for each CDR, we use (4.48)with $D_T = 1/2$ (PRBS data) and the −3-dB band-

widths of Table 4.1. We can then use (4.49) to find C_1, assuming a jitter peaking of 0.1 dB for all three CDRs. Table 4.2 shows the calculated values for I_P, K_{VCO}, R_1, C_1, ζ, and ω_n.

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Chapter 5

Theoretical Analysis of BM-CDRs

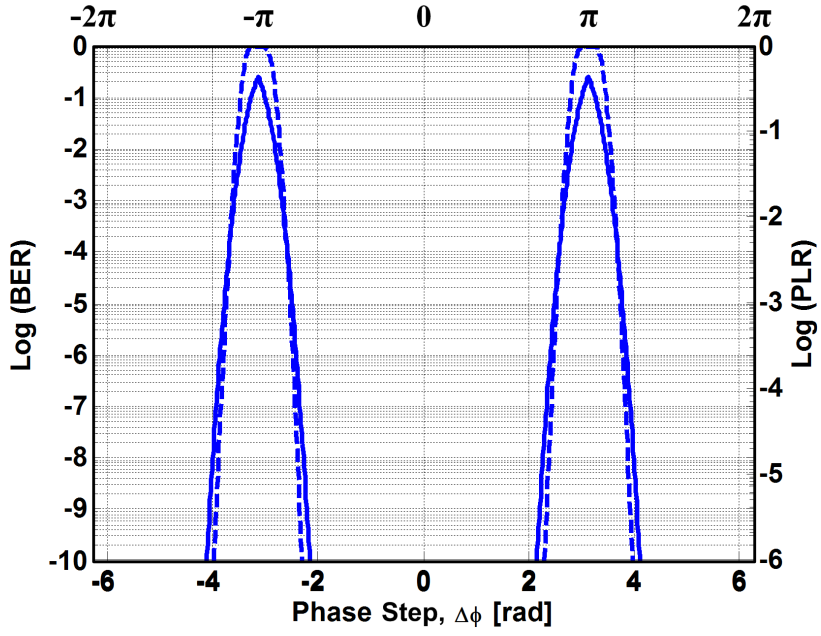
5.1 Introduction

BASED on the probabilistic theory developed in Chapter 4 of the proposed BM-CDRs based on semiblind oversampling in either the time or space domain, we quantitatively analyze the performance of these BM-CDRs by performing a comprehensive theoretical analysis. That is, we investigate the BER and PLR performance of the BM-CDRs to assess the trade-offs between various parameters. This analysis coupled with the experimental results in Chapter 6 will refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets. More specifically, Section 5.2 evaluates the effect of phase step between consecutive packets from independent ONUs. The effect of the packet preamble length is detailed in Section 5.3. Section 5.4 analyzes the effect of RMS jitter on the recovered sampling clock. The effect of pattern correlator error-resistance is presented in Section 5.5. Section 5.6 investigates the effect of finite frequency offset between the local oscillator (LO) and desired bit rate. Finally, this chapter is summarized and concluded in Section 5.7.

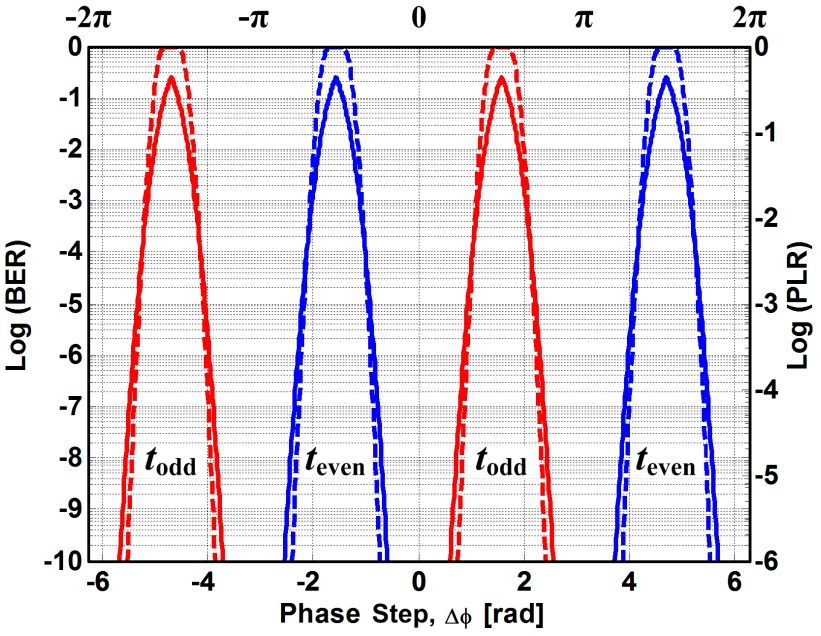
The work presented in this chapter is a result of the research published in [1, 2].

5.2 Effect of Phase Step

The plots shown in Figs. 5.1 and 5.2 depict the performance of a conventional CDR and BM-CDRs based on semiblind oversampling, respectively, in terms of the BER P_e in (4.33), and PLR P_{l_z} in (4.40), as a function of phase step $|\Delta\varphi| \leq 2\pi$ rad. Note that in both the figures,



(a)



(b)

Fig. 5.1 BER and PLR performance versus phase step for a zero preamble length (solid lines for BER curves; dashed lines for PLR curves). (a) Conventional CDR. (b) 2×-semiblind oversampling in either the time- or space domain.

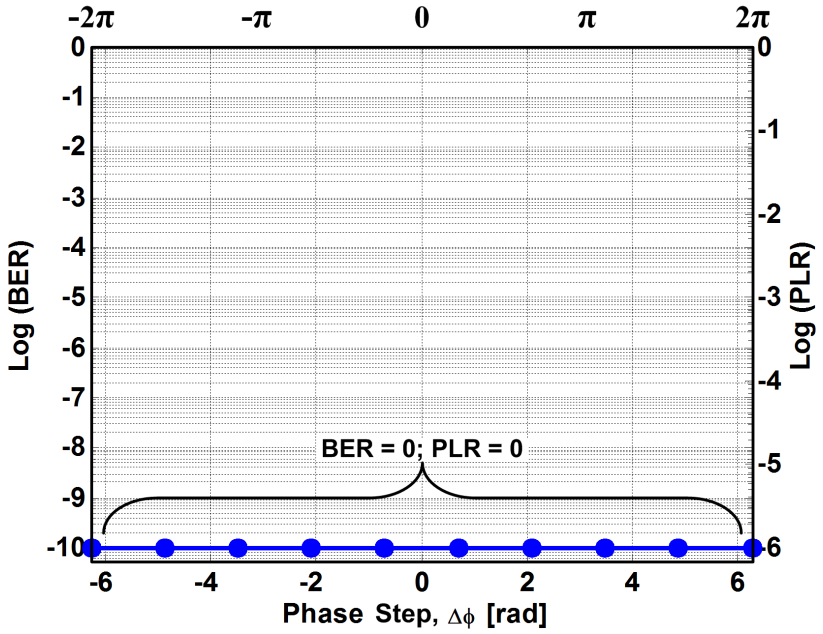


Fig. 5.2 BER and PLR performance of the BM-CDRs based on semiblind oversampling versus phase step for a zero preamble length (solid lines for BER curves; dashed lines for PLR curves).

the preamble length $l = 0$, RMS jitter on the recovered sampling clock $\sigma_{t_s} = 0.02$ UI, and pattern correlator error-resistance $z = 0$. As shown in Fig. 5.1(a) the worst-case phase steps for the CDR are $\Delta\varphi = \pm\pi$ rad because these represent the half-bit periods, and therefore the CDR is sampling exactly at the transition of the eye diagram, resulting in a BER ~ 0.5 and PLR ~ 1. This is as expected from the explanation provided in Chapter 2 [see Fig. 2.14(c)]. At phase shifts (near) $\Delta\varphi \in \{0 \text{ rad}, \pm 2\pi \text{ rad}\}$, we can easily achieve error-free operation, BER $< 10^{-10}$ and PLR $< 10^{-6}$, because the CDR is almost sampling at the middle of each data bit.

For 2×-semiblind oversampling (without phase picking) in either the time- or space domain, as illustrated in Fig. 5.1(b), the worst-case phase steps $\Delta\varphi \in \{\pm\pi/2 \text{ rad}, \pm 3\pi/2 \text{ rad}\}$, result from sampling the data on either the odd and even clock rising edges t_{odd} and t_{even}, located at $-\pi/2$ rad and $+\pi/2$ rad about the center of the data eye (Fig. 4.3). It is interesting to note that in the phase regions $-2\pi \leq \Delta\varphi \leq -\pi$ rad and $0 \leq \Delta\varphi \leq \pi$ rad, where errors arise due the odd sampling instant t_{odd}, error-free operation is achieved with the even sampling instant t_{even}. Similarly, in the phase regions $-\pi \leq \Delta\varphi \leq 0$ rad and $\pi \leq \Delta\varphi \leq 2\pi$ rad, where errors arise with the even sampling instant t_{even}, the odd sampling

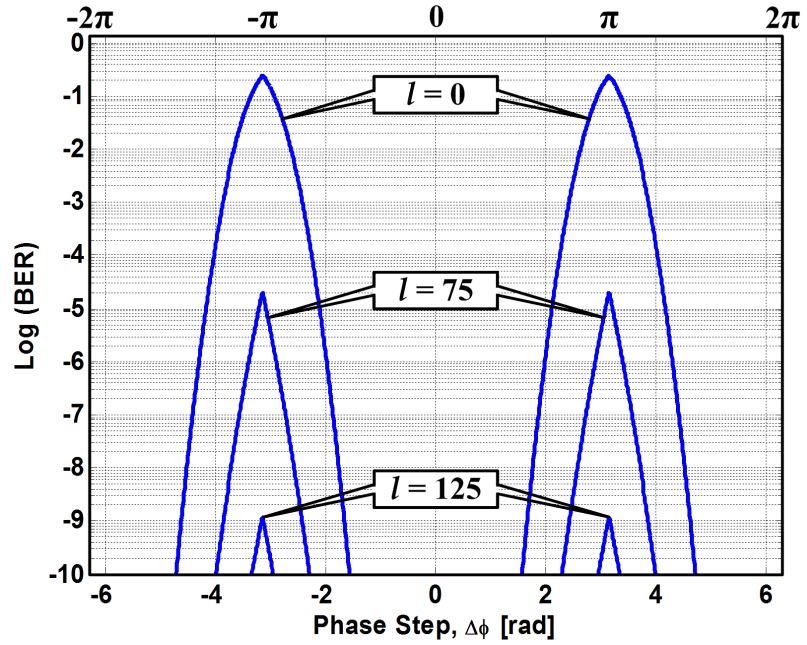
instant t_{odd}, achieves error-free operation. This is the key to the phase picking algorithm of our proposed BM-CDRs that are based on semiblind oversampling.

Finally, for our proposed BM-CDRs based on semiblind oversampling in either the time- or space domain, we achieve error-free operation, for any phase step $|\Delta\varphi| \leq 2\pi$ rad, as shown in Fig. 5.2. The progression from Figs. 5.1(a) and 5.1(b) to Fig. 5.2 shows that 2×-semiblind oversampling, combined with the appropriate CPA, can turn a conventional CDR into a BM-CDR with instantaneous phase acquisition (0-bit) verifying the claim made in Chapter 3.

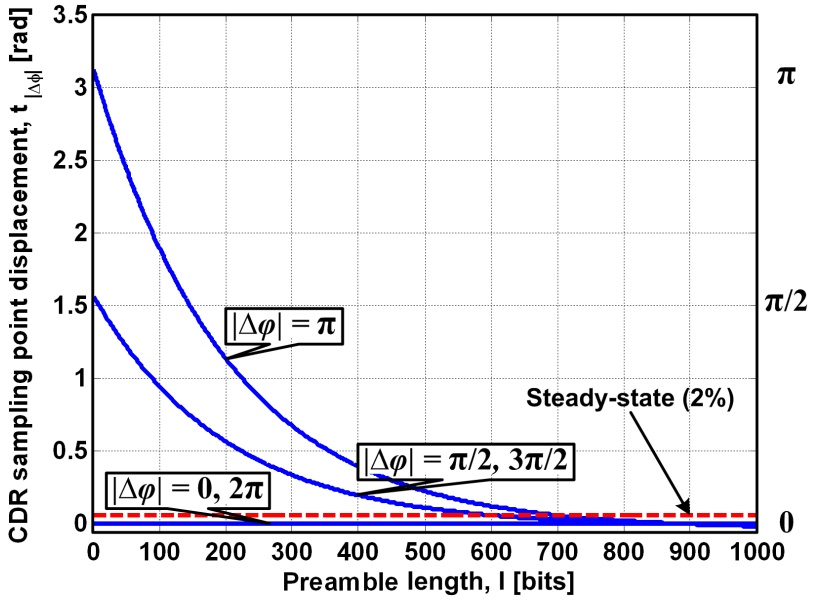
5.3 Effect of Preamble length

In order to compare the performance of the BM-CDRs to the phase acquisition time of the conventional CDR, consider the plot in Fig. 5.3(a) which illustrates the BER performance of the CDR as a function of phase step. Note that for convenience only the BER performance has been shown. We measure the phase acquisition time of the CDR by increasing the length of the preamble until error-free operation is achieved. Preamble bits ("1010$\cdots$"pattern) are inserted at the beginning of the packets to help the PLL of the CDR to settle down and acquire lock. As the preamble length is increased, the BER for the worst-case phase step $|\Delta\varphi| = \pi$ rad improves as the maximum (upper bound) of the curve decreases, and for a given BER, the phase step range for inducing errors becomes smaller as the curve narrows. After 125 preamble bits, we observe error-free operation for any phase step. However, the use of the preamble reduces the effective throughput and increases delay.

Before concluding this section, it should be noted that this method of measuring the phase acquisition time is more accurate than the qualitative method of monitoring the setting time of the CDR's sampling clock to within a certain percentage (usually 2–5%) of the steady-state value as shown in Fig. 5.3(b) where we plot (4.18). The drawback of the latter method is that it overestimates the lock acquisition time—a 14-fold discrepancy. This is because it is not necessary for the sampling clock to be perfectly in the middle of the data bit during the data recovery, but only close enough depending on the RMS jitter on the sampling clock. The effect of RMS jitter will be discussed next. We therefore conclude that the settling time provides, at best, a relative measure of the phase acquisition time.



(a)



(b)

Fig. 5.3 Comparison of two methodologies for measuring the phase acquisition time. (a) BER performance versus phase step and preamble length. (b) CDR sampling point displacement versus phase step and preamble length.

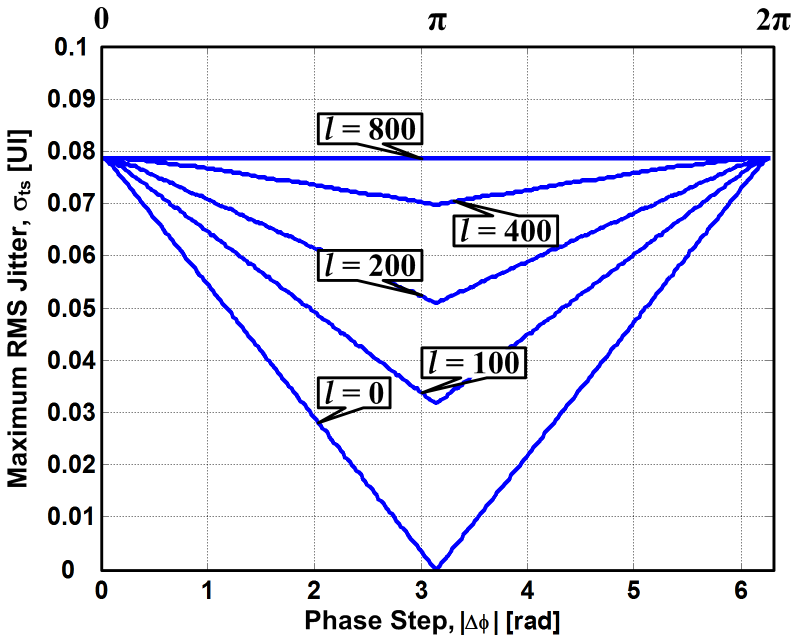


Fig. 5.4 Maximum allowable RMS jitter on the CDR sampling clock versus phase step and preamble length to maintain a BER $\leq 10^{-10}$.

5.4 Effect of RMS Jitter

Here we examine the effect that the RMS jitter on the recovered sampling clock has on the performance of the CDR and BM-CDRs in terms of the phase acquisition time and the BER. In Fig. 5.4, we plot the maximum allowable RMS jitter so as to maintain a BER $\leq 10^{-10}$ as a function of phase step for different preamble lengths. Note that we have restricted the horizontal axis to values from $0 \leq \Delta\varphi \leq 2\pi$ rad as the results are symmetrical about 0 rad from $-2\pi \leq \Delta\varphi \leq 0$ rad. From the plot, it can be observed that this dependence is linear and symmetrical about the worst-case phase step at $|\Delta\varphi| = \pi$ rad. For phase steps $\Delta\varphi \in \{0 \text{ rad}, \pm 2\pi \text{ rad}\}$, the maximum allowable jitter $\sigma_{t_s}^{\max} = 0.08$ UI, for any preamble length; however, at $|\Delta\varphi| = \pi$ rad, $\sigma_{t_s}^{\max} = 0$ UI for no preamble bits $l = 0$. This implies that it is not feasible for the CDR to obtain instantaneous phase acquisition since a jitter-free sampling clock is practically impossible. With increasing preamble length, the jitter tolerance on the sampling clock increases for a given phase step, and tends to become independent of the phase step in the presence of a large number of preamble bits:

$$\lim_{l \to \infty} \sigma_{t_s}^{\max} = 0.08 \text{ UI, for all } |\Delta\varphi| \leq 2\pi \text{ rad} \tag{5.1}$$

To compare the performance of the CDR with the proposed BM-CDRs, examine the plots in Fig. 5.5 which show the number of preamble bits required to obtain a BER $\leq 10^{-10}$ as a function of the maximum allowable RMS jitter for different phase steps. For now we have restricted the phase step range to $0 \leq |\Delta\varphi| \leq \pi$ rad. For phase steps $|\Delta\varphi| \leq \pi/4$ rad, the CDR has a better tolerance to jitter than compared to the BM-CDRs. This is expected as the CDR's recovered clock is sampling closer to the middle of the data bit than compared to the BM-CDR's multiphase clocks which are sampling further away from the center of the data eye for phase steps $|\Delta\varphi| \leq \pi/4$ rad [see Figs. 3.4(a) and 3.5(a)]. However, for phase steps $\pi/4 < |\Delta\varphi| \leq \pi$ rad, the proposed BM-CDRs have a better jitter tolerance. Moreover, it should be noted that the BM-CDRs are able to achieve instantaneous phase acquisition when the RMS jitter $\sigma_{t_s} \leq 0.04$ UI for any phase step. This is not the case for the CDR as the tolerance to jitter is 0 UI to obtain instantaneous phase acquisition for the worst-case phase step $|\Delta\varphi| = \pi$ rad. These theoretical limits can be summarized as:

$$\lim_{l\to 0} \sigma_{t_s}^{\max} = \begin{cases} 0 \text{ UI}, & \text{for CDR} \\ 0.04 \text{ UI}, & \text{for BM-CDR} \end{cases} \quad \text{for } |\Delta\varphi| = \pi \text{ rad}. \tag{5.2}$$

It is interesting to note that in the case of the CDR, a jitter tolerance of 0.04 UI corresponds to a preamble length of more than 125 bits for $|\Delta\varphi| = \pi$ rad. This confirms our findings in Fig. 5.3(a) and in particular the measurement methodology.

To investigate yet another perspective, in Fig. 5.6 we plot the BER performance of the CDR and the BM-CDRs as a function of phase steps for different RMS jitter and zero preamble bits. When the RMS jitter is $\sigma_{t_s} > 0.04$ UI, the shaded area in Fig. 5.6(a) depicts the tradeoff region with the phase steps $|\Delta\varphi| \leq \pi/4$ rad, where the CDR has a better jitter tolerance than compared to the BM-CDRs due to the more optimum location of the sampling point as explained before. However, the plots in Fig. 5.6(b) show that the BM-CDRs achieve instantaneous phase acquisition when the RMS jitter $\sigma_{t_s} \leq 0.04$ UI, for any phase step $|\Delta\varphi| \leq 2\pi$ rad.

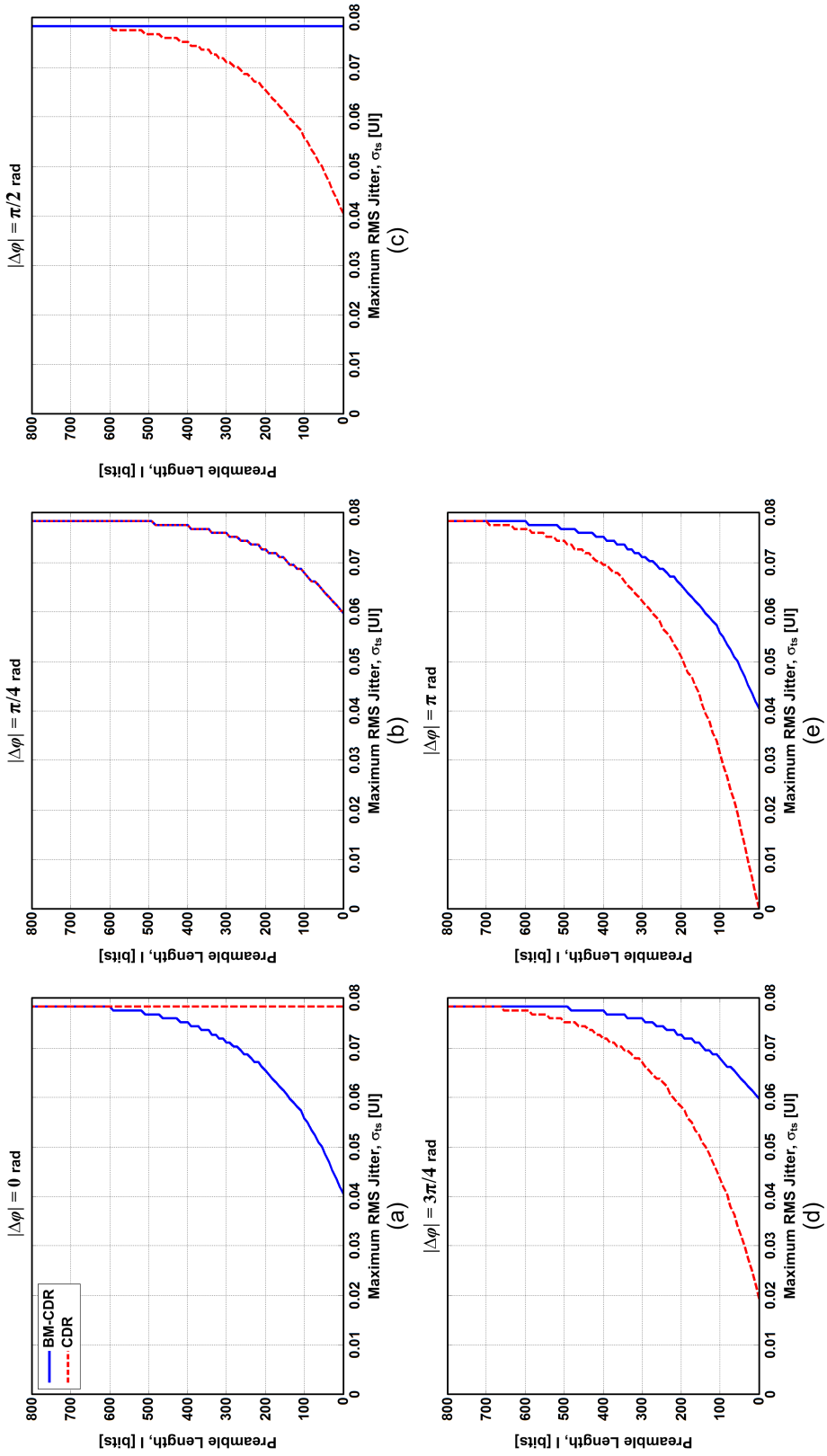
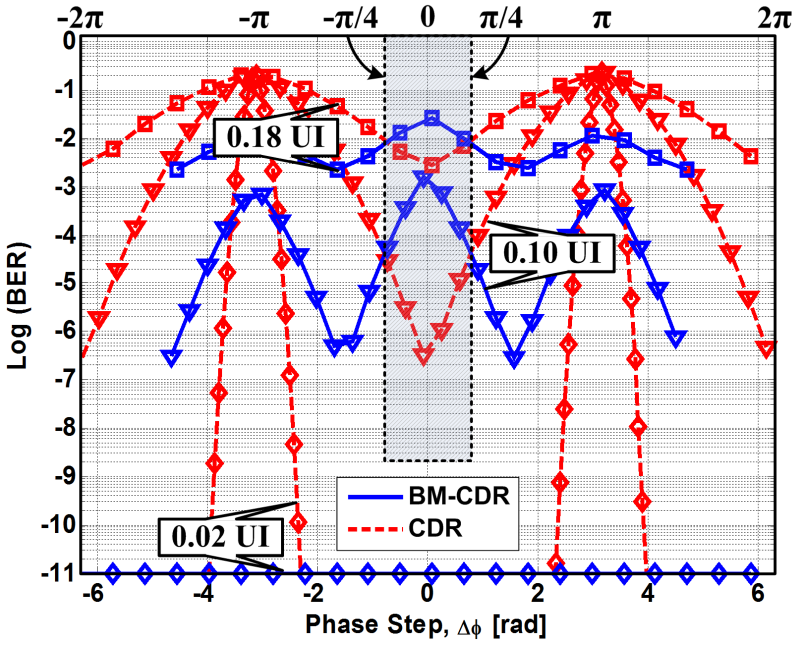
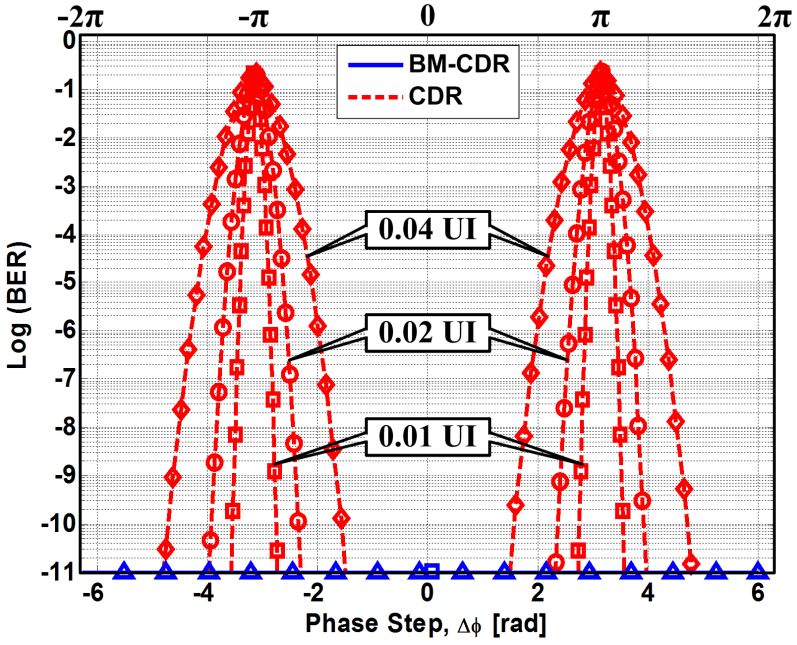


Fig. 5.5 Preamble length versus maximum allowable RMS jitter to achieve a BER $\leq 10^{-10}$ for different phase steps: (a) $|\Delta\varphi| = 0$ rad; (b) $|\Delta\varphi| = \pi/4$ rad; (c) $|\Delta\varphi| = \pi/2$ rad; (d) $|\Delta\varphi| = 3\pi/4$ rad; and (e) $|\Delta\varphi| = \pi$ rad.



(a)



(b)

Fig. 5.6 BER performance of the CDR and BM-CDRs versus phase step for different RMS jitter and zero preamble bits. (a) $\sigma_{t_s} > 0.04$ UI depicting the tradeoff region in the range $|\Delta\varphi| \leq \pi/4$ rad. (b) $\sigma_{t_s} \leq 0.04$ UI.

5.5 Effect of Pattern Correlator Error-Resistance

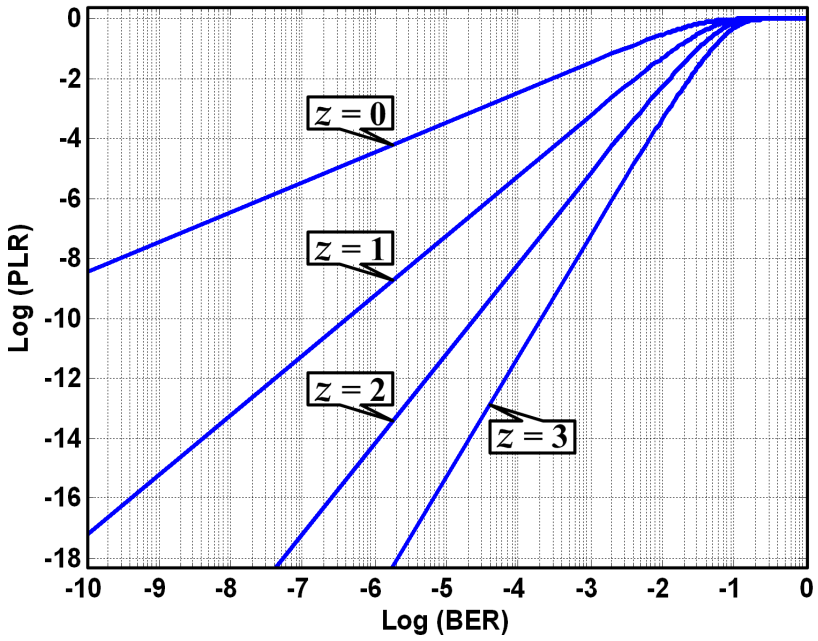
To improve the system performance, forward-error correcting (FEC) schemes can be employed by encoding the packet bits. Due to the associated overhead, most standards impose a strict requirement on the delimiter field—a unique pattern of fixed length. Therefore, while the payload bits can be encoded, it is usually not possible to encode the delimiter bits. Hence, while there is an improvement in the BER performance at a given signal-to-noise ratio (SNR), the same cannot be implied about the PLR performance which is dependent on the delimiter being correctly identified. Consequently, the BER may not be a true reflection of the system performance, but that of the properly received bursts only, as many other bursts may be lost without being included in the BER measurement.

The PLR performance can be improved by increasing the error-resistance of the pattern correlator with a more sophisticated design of the pattern correlator. Thus, the complexity of the pattern correlator depends on an acceptable error-resistance of the delimiter. Consider Fig. 5.7(a) where we plot (4.40), that is, the PLR performance P_{l_z}, as a function of the BER P_e, for different error-resistance values z, of the delimiter. Even with a simple pattern correlator having no error-resistance ($z = 0$ bits), we obtain error-free operation: PLR $< 10^{-9}$ at BER $= 10^{-10}$. Furthermore, by increasing the pattern correlator error-resistance to $z = 1$ bit, we obtain an improvement in the PLR performance by eight orders of magnitude.

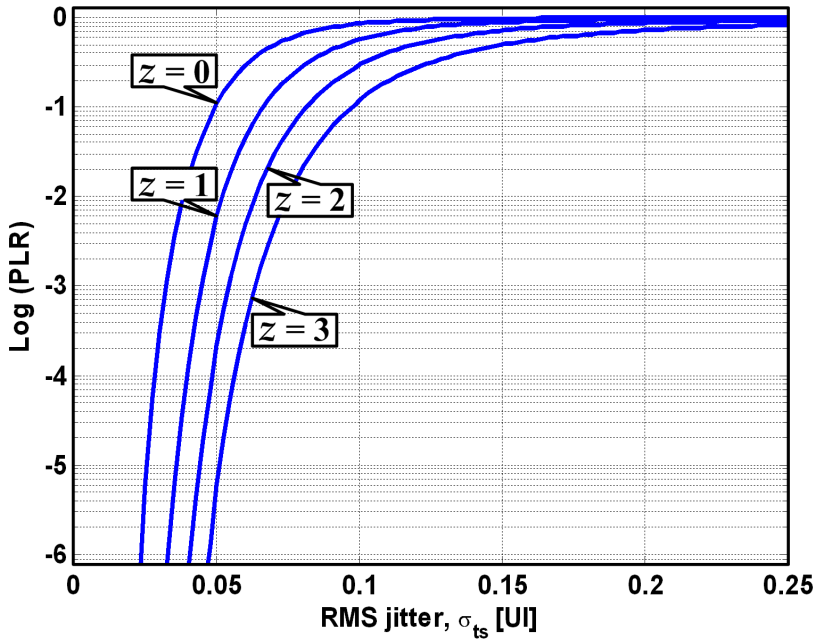
In Fig. 5.7(b), we plot the PLR performance of the BM-CDR as a function of the RMS jitter on the sampling clock for the worst-case phase step and zero preamble bits. As expected, the PLR performance degrades with increasing RMS jitter; however, by increasing the error-resistance of the pattern correlator, there is considerable amount of improvement in the PLR performance at a given RMS jitter, while the allowable RMS jitter increases for a given PLR.

5.6 Effect of Frequency Offset

To study the effect of frequency deviation of the sampling clock (LO) from the desired data rate on the BER and PLR performance of the BM-CDR, consider the plot in Fig. 5.8(a) resulting from (4.36) and (4.39). We set the length of CIDs $m = 0$, and assume that the CDR is using both the rising and falling edge of the input data to adjust the clock

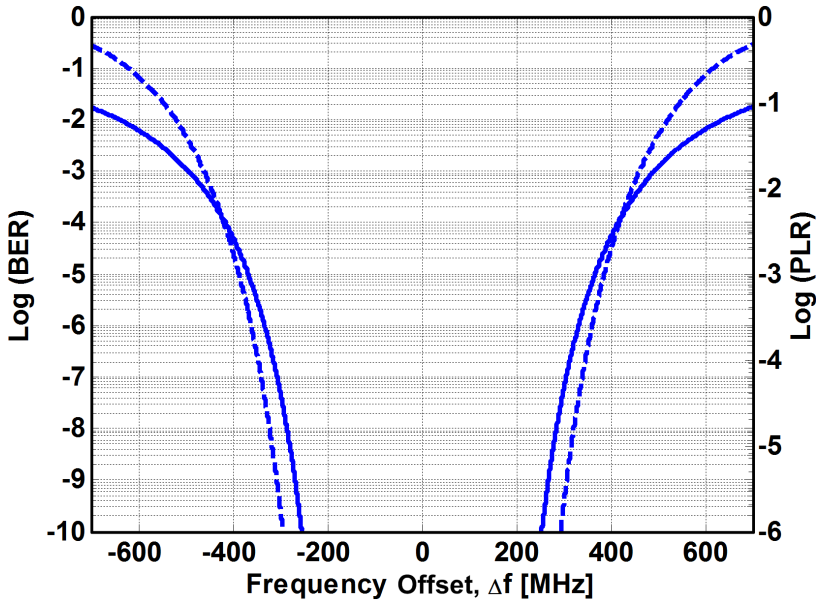


(a)

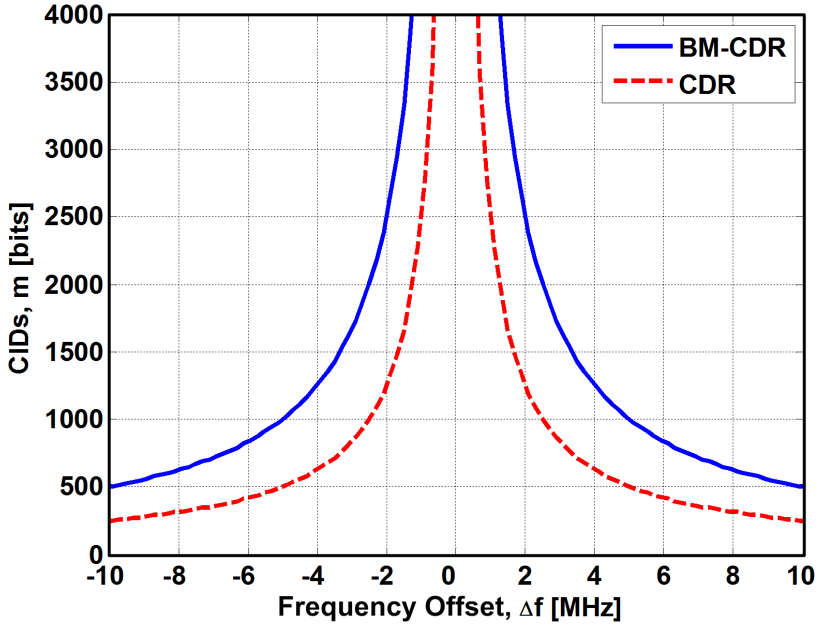


(b)

Fig. 5.7 Effect of pattern correlator error resistance on the PLR performance versus: (a) BER performance; and (b) RMS jitter on the sampling clock.



(a)



(b)

Fig. 5.8 (a) BER and PLR performance of BM-CDR versus frequency offset. (b) maximum length of CIDs tolerated by the CDR and BM-CDR versus frequency offset.

phase, thus $k = 2$. We vary the frequency offset parameter Δf, and determine its effect on the phase error between successive packets $\Delta\varphi_e$, and on the sampling clock RMS jitter σ_{t_s}. Plugging these parameters in (4.33) and (4.40), we can determine the BER and PLR performance of the BM-CDR, respectively. It can be seen the BM-CDR achieves error-free operation for a frequency lock range of 590 MHz, that is from −295 MHz to +295 MHz. This is obviously an optimistic result as the model does not account for the jitter generated by the circuit which would deteriorate the result appreciably. This will be further elaborated upon when presenting the experimental results in Section 6.3.3. After this lock-range, any further increase in the frequency offset will degrade the performance.

Next, we determine the maximum length of CIDs $m_{\max}$, that can be tolerated by the CDR and BM-CDR in the presence of a frequency offset. In Fig. 5.8(b) we plot (4.37). As can be expected in general, the tolerance to CIDs decreases with increasing frequency deviation:

$$\lim_{|\Delta f|\to\infty} m_{\max} = 1. \tag{5.3}$$

However, it can be inferred from Fig. 5.8(b) that the BM-CDR is able to tolerate significantly more CIDs than the CDR at lower frequency deviations.

5.7 Conclusion

In this chapter, we quantitatively analyzed the performance of our proposed BM-CDRs in Chapter 3 that are based on semiblind oversampling in either the time or space domain, with the probabilistic model developed in Chapter 4. More specifically, we performed a comprehensive theoretical analysis by investigating the BER and PLR performance of the BM-CDRs to assess the tradeoffs between the following parameters: (1) silence period, including phase step and length of CIDs, between consecutive packets from independent ONUs; (2) preamble length; (3) RMS jitter on the recovered sampling clock; (4) pattern correlator error-resistance; and (5) finite frequency offset between the LO and desired bit rate.

In summary, the jitter tolerance on the sampling clock of the CDR and BM-CDR with no preamble bits at the worst-case phase step is predicted to be 0 UI and 0.04 UI, respectively. This implies that it is not feasible for the CDR to obtain instantaneous

phase acquisition since a jitter-free sampling clock is practically impossible. By increasing the preamble length, the jitter tolerance for a given phase step increases. In the case of the CDR, at least 125 preamble bits are required to achieve error-free operation for any phase step; however, this comes at the cost of reduced effective throughput and increased delay. Due the superior jitter tolerance of the BM-CDR, instantaneous phase acquisition for any phase step is possible. The PLR performance can be improved by increasing the error-resistance of the pattern correlator with a more sophisticated design. With a simple pattern correlator having no error-resistance, the model predicts a PLR $< 10^{-9}$ at BER $= 10^{-10}$. By increasing the error-resistance to 1 bit, we observe an improvement of 1.5 dB at PLR $= 10^{-6}$ and eight orders of magnitude at a given BER, in the receiver sensitivity and PLR performance, respectively.

This analysis will refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets. In the next chapter, these results will be compared to the experimental results, thereby validating the theoretical model.

References

[1] B. J. Shastri and D. V. Plant, "5/10-Gb/s burst-mode clock and data recovery based on semiblind oversampling for PONs: theoretical and experimental," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 5, pp. 1298–1320, Sep.-Oct. 2010.

[2] B. J. Shastri and D. V. Plant, "Probabilistic theory for semi-blind oversampling burst-mode clock and data recovery circuits," in *Proc. IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, Seattle, WA, Aug. 2010, pp. 161–164.

Chapter 6

Experimental Expositions of BM-CDRs

6.1 Introduction

IN Chapter 3 we designed and implemented novel BM-CDR architectures based on semiblind oversampling in both the time and space domain. Moving forward, in Chapter 4 we developed a unified probabilistic theory of these BM-CDRs to quantify their performance in terms of the BER and PLR. In Chapter 5 we quantitatively analyzed the performance of the BM-CDRs by performing a comprehensive theoretical analysis to assess the tradeoffs between various parameters. Having laid the necessary foundation, in this chapter we experimentally demonstrate and analyze our proposed BM-CDR architectures in various optical test beds. The objective of this chapter is to: (1) validate the proposed theoretical model with the experimental results; and (2) study the effect of channel-impairments on burst-mode reception in these test beds. Furthermore, we note that the experimental expositions are designed to illustrate the application potential of these BM-CDRs—"a solution looking for problems".

The rest of the chapter is organized as follows. In Section 6.2, we verify the functionalities of the proposed BM-CDRs based on semiblind time and space domain oversampling at the targeted bit rates of 5 Gb/s and 10 Gb/s, respectively. We also propose two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition. In Section 6.3, we experimentally study burst-mode reception at 5 Gb/s in a 20-km time-

division multiplexing gigabit ethernet passive optical network (PON) uplink. The BM-CDR based on semiblind time domain oversampling is utilized in this work. In Section 6.4, we experimentally show burst-mode reception at 2.5 Gb/s in a 20-km overlapped subcarrier-multiplexing wavelength-division multiplexed PON uplink. The receiver employed in this study is a variant of the BM-CDR based on semiblind space domain oversampling. In Section 6.5, we experimentally demonstrate burst-mode reception at 1.25 Gb/s in a 1300-km deployed fiber link that spans from Montreal to Quebec City and back. The BM-CDR based on semiblind time domain oversampling is utilized in this study. In Section 6.6, we experimentally investigate burst-mode reception at 622 Mb/s in a 7-user 20-km incoherent spectral amplitude-coded optical code-division multiple access PON uplink. We consider two network architectures, namely, local sources and centralized local sources, and study their relative merits in a two-feeder topology. The receiver employed in this study is variant of the BM-CDR based on semiblind time domain oversampling with a Reed-Solomon RS(255,239) forward-error correction decoder. Finally, this chapter is summarized in Section 6.7.

6.2 10 Gb/s and 5 Gb/s Experimental Demonstrations

6.2.1 Introduction

Before exploring the application potential of our proposed BM-CDRs in various optical test beds, we first test these BM-CDRs in a conventional electric test bed. This is to verify their functionalities at their targeted bit rates. The BM-CDR based on semiblind time domain oversampling is implemented to operate at 5 Gb/s, whereas the BM-CDR based on semiblind space domain oversampling is implemented to operate at 10 Gb/s. We also proposed two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition. Moving forward, in the proceeding sections we will study the effect of channel-impairments on burst-mode reception in various optical test beds. The work presented in this section is a result of the research published in [1, 2].

6.2.2 Experimental Setup

Burst-mode experimental setups illustrated in Fig. 6.1 can be used to test the phase acquisition times of the proposed BM-CDRs. The key difference between these setups is the way the phase steps are generated, which in turn depends on the type of BM-CDR being tested. To further clarify, consider both the BM-CDRs in turn. The BM-CDR based on semiblind time domain oversampling employs a phase-tracking CDR circuit operated at 2× the bit rate and a clock phase aligner (CPA) that makes use of a phase picking algorithm. It makes use of a payload detection algorithm to look for a preprogrammed delimiter pattern, a unique pattern indicating the start of the packet, to lock at the correct phase of the incoming packet. Once the selection is made, it cannot be overwritten until the comma is detected, indicating the end of the packet. This process repeats itself at the beginning of every packet. This means that this BM-CDRs can acquire phase for any phase step *in between* two consecutive packet packets—inter-packet phase acquisition. However, it cannot account for any phase steps *within* a packet—intra-packet phase acquisition.

On the other hand, the BM-CDR based on semiblind space domain oversampling employs on a phase-tracking CDR circuit operated at the bit rate with two multiphase clocks and a CPA that makes use of a novel phase picking algorithm. In this case, the CPA does not require any *a priori* knowledge of the packet delimiter. Hence, this BM-CDR can also acquire phase in even more stringent conditions; that is, for any phase steps *within* a packet

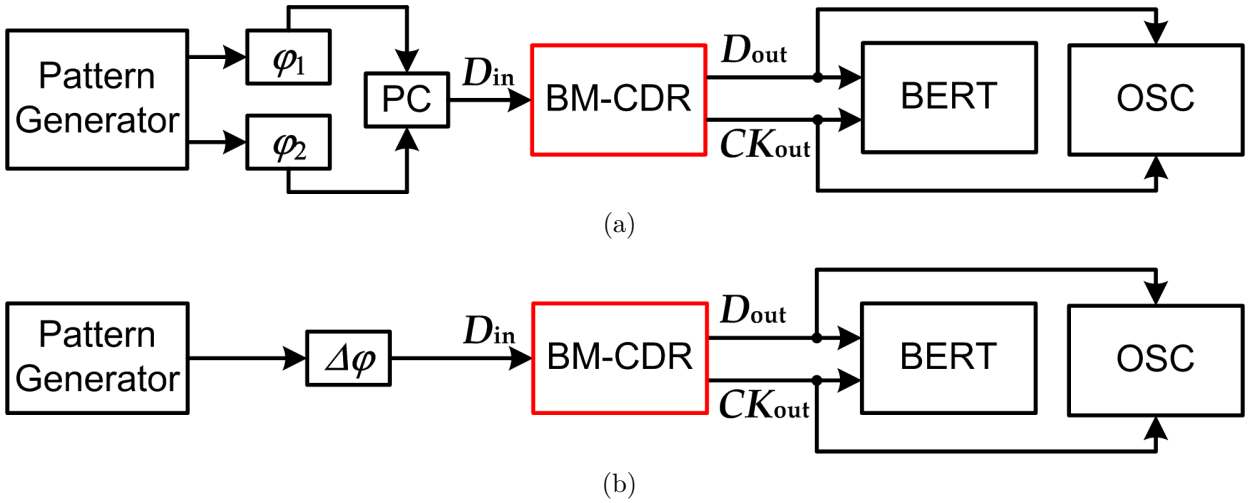


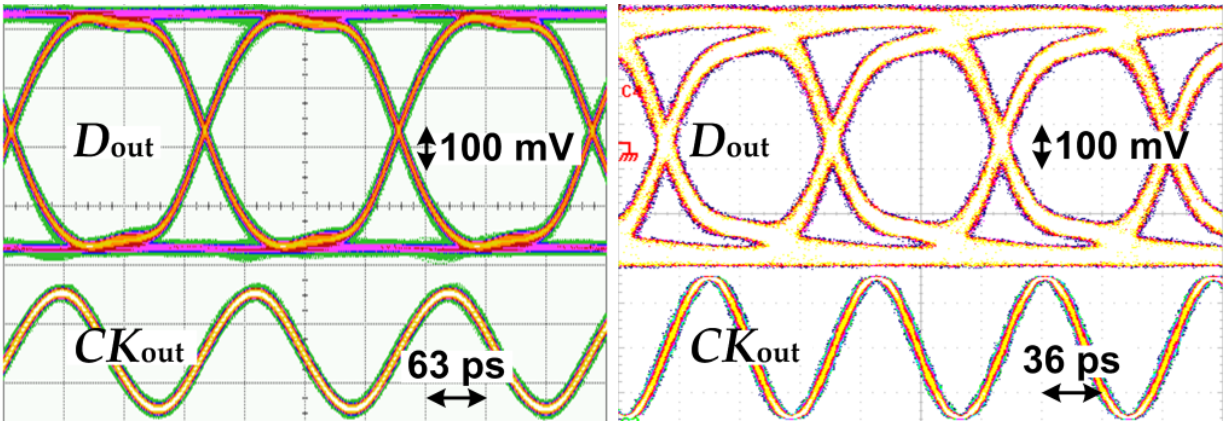
Fig. 6.1 Burst-mode experimental setup to test the proposed BM-CDRs. (a) Inter-packet phase generation to test BM-CDR based on semiblind time domain oversampling in Fig. 3.6. (b) Intra-packet phase generation to test BM-CDR based on semiblind space domain oversampling in Fig. 3.13 (BERT: bit error rate tester; OSC: oscilloscope).

(intra-packet phase acquisition), making it truly modular across application test beds.

Fig. 6.1(a) shows a burst-mode setup to test inter-packet phase acquisition, whereas Fig. 6.1(b) shows a burst-mode setup to test *intra-packet* phase acquisition. In Fig. 6.1(a), bursty traffic is generated by adjusting the phase φ_1 and φ_2, between alternating packets from two programmable ports of an Anritsu MP1800A pattern generator. These packets are then concatenated via a radio frequency (RF) power combiner. On the other hand, in Fig. 6.1(b), bursty traffic is generated by adjusting the phase $\Delta\varphi$ at any point within a packet with a phase shifter from Hittite Microwave (Part #HMC538LP4). The packets are formed from guard bits, preamble bits, delimiter bits, $2^{15}-1$ pseudorandom binary sequence (PRBS) payload bits, and comma bits. More details of the packets will be provided in Section 6.3.2. Note that the phase steps between the consecutive packets can be set anywhere between ± 250 ps and ± 150 ps with a 1-ps resolution, corresponding to a ± 1.25 unit interval (UI) at 5 Gb/s and 10 Gb/s, respectively.

6.2.3 Experimental Results

Figs. 6.2(a) and 6.2(b) show the eye diagrams of the recovered data and clock in response to a $2^{15} - 1$ PRBS for the BM-CDRs based on time and space domain oversampling at 5 Gb/s and 10 Gb/s, respectively.



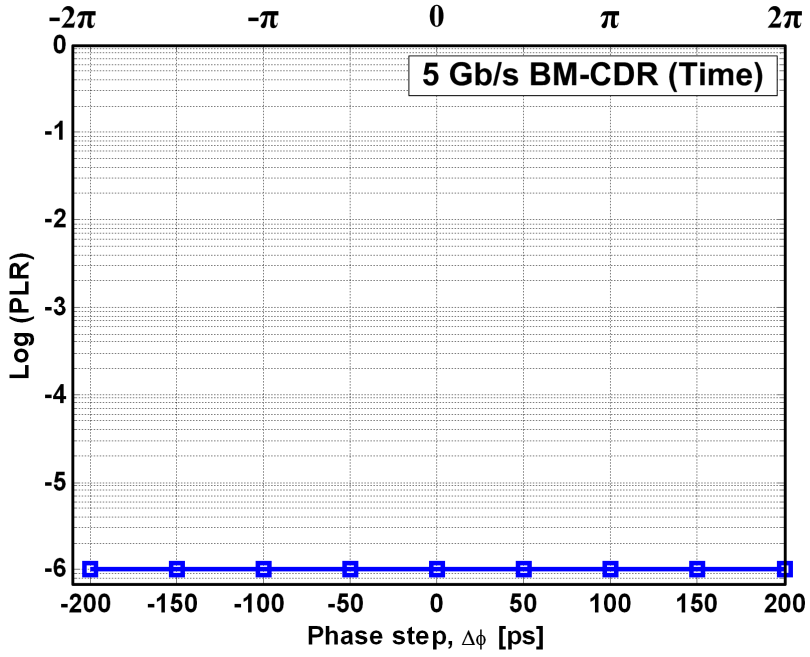
(a) (b)

Fig. 6.2 Eye diagram for recovered clock and data. (a) 5 Gb/s BM-CDR based on time domain oversampling. (b) 10 Gb/s BM-CDR based on space domain oversampling.

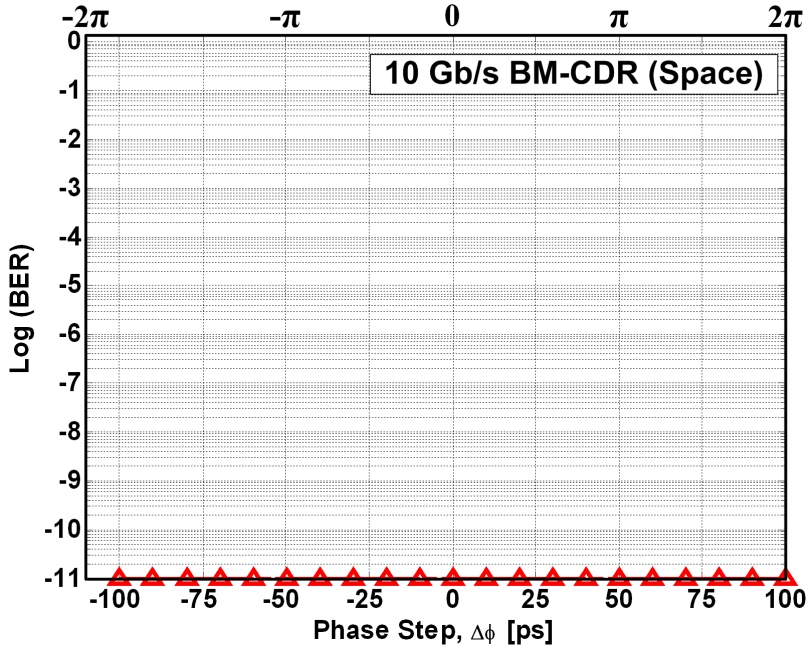
In Fig. 6.3, we plot the performance of the BM-CDRs as a function of the phase step $-2\pi \leq \Delta\varphi \leq 2\pi$ rad, with *no* preamble bits. Note that 1 UI or 2π rad corresponds to 200 ps and 100 ps at 5 Gb/s and 10 Gb/s, respectively. For the proposed BM-CDRs, we observe error-free operation for any phase step $|\Delta\varphi| \leq 2\pi$ rad, with 0-bit preamble, allowing for instantaneous phase acquisition. This is as predicted by the probabilistic theory in Chapter 4 and theoretical analysis in Section 5.2.

6.2.4 Conclusion

In this section, we verified the functionalities of the proposed BM-CDRs based on semiblind oversampling in both the time and space domain at the targeted bit rates of 5 Gb/s and 10 Gb/s, respectively. We tested them in conventional electric test beds. Both the BM-CDRs achieve error-free operation while providing instantaneous (0-preamble bit) phase acquisition for any phase step. We also proposed two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition. Moving forward, in



(a)



(b)

Fig. 6.3 Performance of the BM-CDRs versus phase step for a zero preamble length. (a) 5 Gb/s BM-CDR based on time domain oversampling. (b) 10 Gb/s BM-CDR based on space domain oversampling.

the proceeding sections we will study the effect of channel-impairments on burst-mode reception in various optical test beds.

6.3 5 Gb/s TDM GEPON 20-km Uplink Experiments

We experimentally study burst-mode reception at 5 Gb/s in a 20-km time-division multiplexing gigabit ethernet PON uplink. The BM-CDR based on semiblind oversampling in the time domain (see Section 3.3) is utilized in this work. The work presented in this section is a result of the research published in [3–12].

6.3.1 Introduction

Data rates on fiber optic networks are increasing dramatically after having experienced constant growth for numerous decades. Fiber-to-the-premises/cabinet/building/home/user (FTTx) networks using single-mode fiber is capable of meeting these access network requirements at high (10+ Gb/s) data rates with superior network capacities. FTTx is therefore currently being aggressively deployed by the service provider community worldwide [13,14]. PONs are an emerging multiaccess network technology based on all-optical core and are recognized as the most promising solution for deploying FTTx [14–16]. PONs provide a low-cost solution to alleviate the so called "last mile" problem that remains a bottleneck between the backbone network and high-speed local area networks (LANs). Consequently, the promise of a better bundle of distributive and interactive multimedia services such as video, voice, data, and fast Internet, to a large number of subscribers with guaranteed quality of service (QoS) by PONs, is compelling [17].

A PON typically has a physical tree topology with an optical line terminal (OLT) located at the root and optical networks units (ONUs) connected to the branches. Existing PON standards, including the IEEE 802.3ah gigabit ethernet PON (GEPON) [18], and ITU-T G.984 gigabit-capable PON (GPON) [19], are based on time-division multiplexing (TDM) and can serve up to 32 or 64 users. Fig. 6.4 shows a general architecture of a standard commercial TDM-PON structure with our work in context. The maximum transmission distance between the ONUs and the OLT is usually 10–20 km. In the downstream direction, the network is point-to-point (P2P). Continuous data is broadcast from the OLT to the ONUs using TDM in the 1480–1550-nm wavelength band. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous mode integrated circuits (ICs). The challenge in the design of a chip set for PONs comes from the upstream data path. In the upstream direction, the network is point-to-multipoint (P2MP); using time division multiple access (TDMA), multiple ONUs transmit data in the 1310-nm window

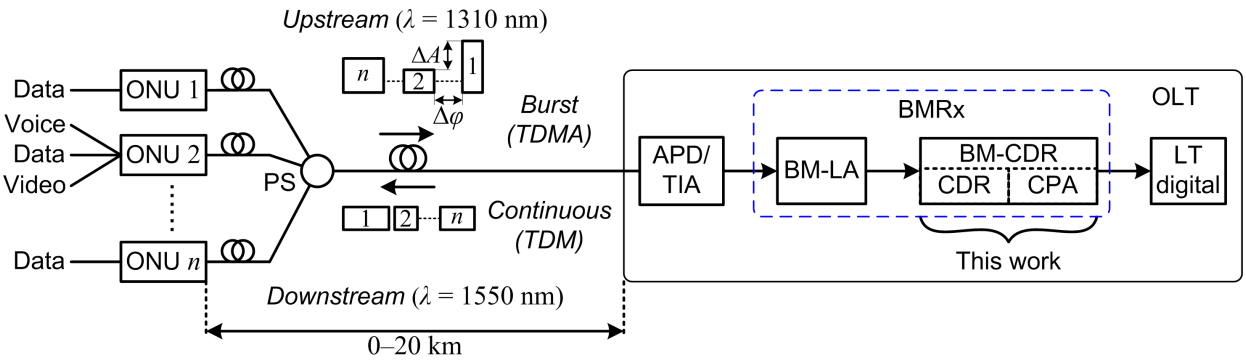


Fig. 6.4 Generic TDM PON for FTTx showing our work on BM-CDR in context (APD: avalanche photodiode; BM-LA: burst-mode limiting amplifier; BMRx: burst-mode receiver; CDR: clock and data recovery; CPA: clock phase aligner; LT: line terminator; OLT: optical line terminal; ONU: optical network unit; TDM: time division multiplexing; TDMA: time division multiple access; TIA: transimpedance amplifier).

to the OLT in the central office (CO). To use the shared medium effectively, the ONUs require a burst-mode transmitter with a short turn-ON/OFF delay [20]. Because of optical path differences in the upstream path, packets can vary in amplitude ΔA, and phase $\Delta\varphi$—bursty data. The amplitude and phase of successive packets may vary anywhere between 0 to 20 dB and -2π to $+2\pi$ rad, respectively [21]. The inevitable and random nature of phase steps causes conventional CDRs based on phase-locked loops (PLLs), to lose pattern synchronization. Preamble bits can be inserted at the beginning of each packet to allow the CDRs enough time to acquire lock. However, this overhead reduces the effective throughput and increases delay. Consequently, to deal with bursty data, the OLT requires a burst-mode receiver (BMRx). The BMRx is responsible for amplitude and phase recovery, which must be achieved at the beginning of every packet. At the front-end of the BMRx is a burst-mode limiting amplifier (BM-LA) responsible for amplitude recovery. Fast clock and data recovery together with phase acquisition is then performed by a BM-CDR with the help of a clock phase aligner (CPA). The most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible.

In this section we carry out a detailed set of experiments to investigate the effect of silence period, including phase step and the length of consecutive identical digits (CIDs), between successive upstream PON bursts from independent ONUs, received signal power, and finite frequency offset between the sampling clock and desired bit rate, on the BER and

PLR performance of the BM-CDR. Consequently, we characterize the BM-CDR in terms of the phase acquisition time, CID immunity, burst-mode sensitivity penalty, dynamic range, and frequency acquisition range.

Following this introduction, the rest of the section is organized as follows. Section 6.3.2 details the experimental setup together with the measurement methodology. In Section 6.3.3 we present and analyze the experimental results. Finally, Section 6.3.4 provides a summary and conclusion.

6.3.2 Experimental Setup

This section describes the burst-mode experimental setup, test signal specification, and measurement methodology used to test and characterize the BM-CDR in a 20-km PON uplink.

Burst-Mode Test Setup—PON Test Bed

The burst-mode experimental test setup (BM-TS) illustrated in Fig. 6.5 is used to test the BM-CDR in a 20-km PON uplink. Fig. 6.5 shows a photograph of the experimental setup built in the lab. Bursty upstream PON traffic is generated by adjusting the phase φ_1 and φ_2, between alternating packets from two programmable ports of an Anritsu MP1800A pattern generator which are then used to drive their respective polarization dependent Mach-Zehnder modulators (MZM). The amplitude of the packets A_1 and A_2, is adjusted by employing variable optical attenuators (VOA) at the output of each 1310-nm Fabry-Perot (FP) lasers. The launch power is set to 0.5 dBm with an extinction ratio of 10 dB as per the GPON standard [19]. These packets are formed from guard bits, preamble bits, delimiter bits, $2^{15}-1$ PRBS payload bits, and comma bits. As per (2.8), a silence period, T_s, consisting of a phase step $|\Delta\varphi| = |\varphi_1 - \varphi_2| \leq 2\pi$ rad, and an all-zero sequence of m CIDs can be inserted between the packets. Note that the phase steps between the consecutive packets can be set anywhere between $\pm$250 ps with a 1-ps resolution, corresponding to a $\pm$1.25 UI at 5 Gb/s. The packets from the two ONUs are then coupled and sent over a 20-km single-mode fiber (SMF-28) uplink. A VOA serves to control the received power level. At the OLT, the optical-to-electrical (OE) conversion is performed by a PIN photodiode from New Focus (Model #1434). The bursty signal is then low-pass filtered before being sent to the BM-CDR. The low-pass filter (LPF) is a fourth-order Bessel-Thomson filter

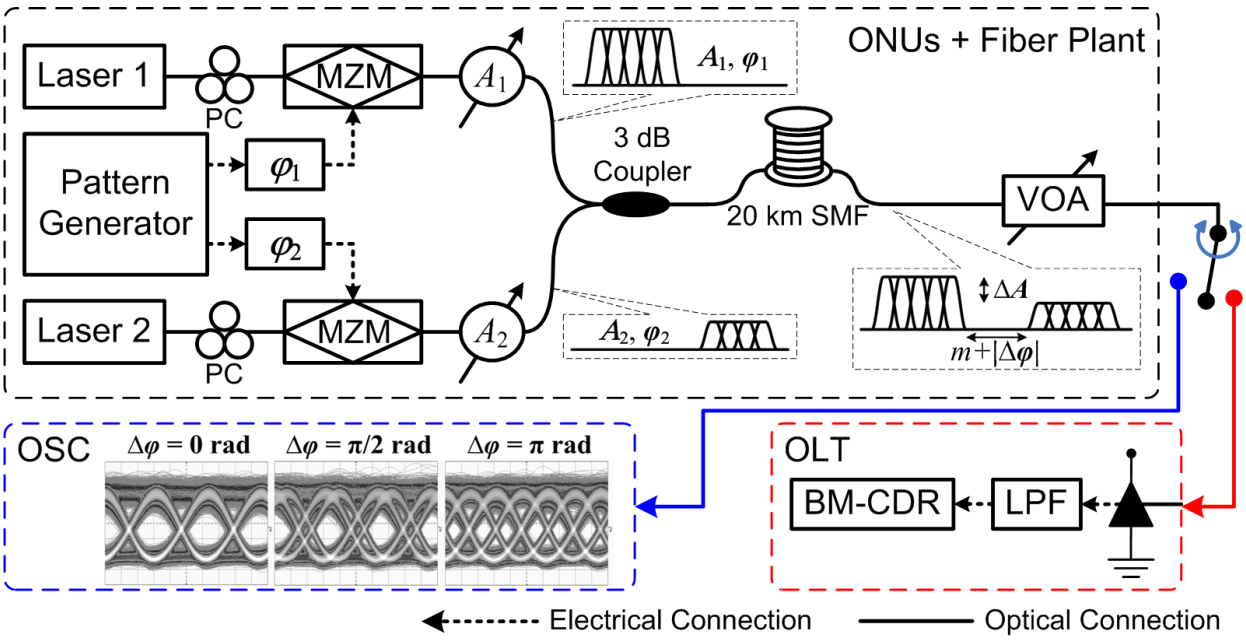


Fig. 6.5 Burst-mode experimental setup to test and characterize the BM-CDR in a 20-km PON uplink. Details of the BM-CDR and the test signal are depicted in Fig. 3.6 and Fig. 6.7, respectively (LPF: low-pass filter; MZM: Mach-Zehnder modulator; OLT: optical line terminal; ONUs: optical network units; OSC: oscilloscope; PC: polarizer controller; SMF: single-mode fiber; VOA: variable optical attenuator).

from Picosecond to remove out-of-band high-frequency electrical noise whose −3-dB cutoff frequency is 0.75 × bit rate, or 3.75 GHz. Such a filter has an optimum bandwidth to filter out noise while keeping intersymbol interference (ISI) to a minimum [22]. Eye diagrams of the bursty traffic at the input to the BM-CDR are shown in Fig. 6.5.

Test Signal Specification

At the time of this study, the IEEE 10G-EPON task force was engaged in detailed discussions aimed at standardizing the physical specifications to attain a total bandwidth of 10 Gb/s [23]. Since the 10G-EPON is backward compatible with GEPON [18], the timing parameters were assumed to be closely related. Table 6.1 compares the upstream burst-mode overhead parameters for GEPON and GPON [19]. While our BM-CDR is compatible with both standards, we have nonetheless decided to test the BM-CDR under the stringent timing requirements imposed by the latter. A typical bursty signal that complies with the

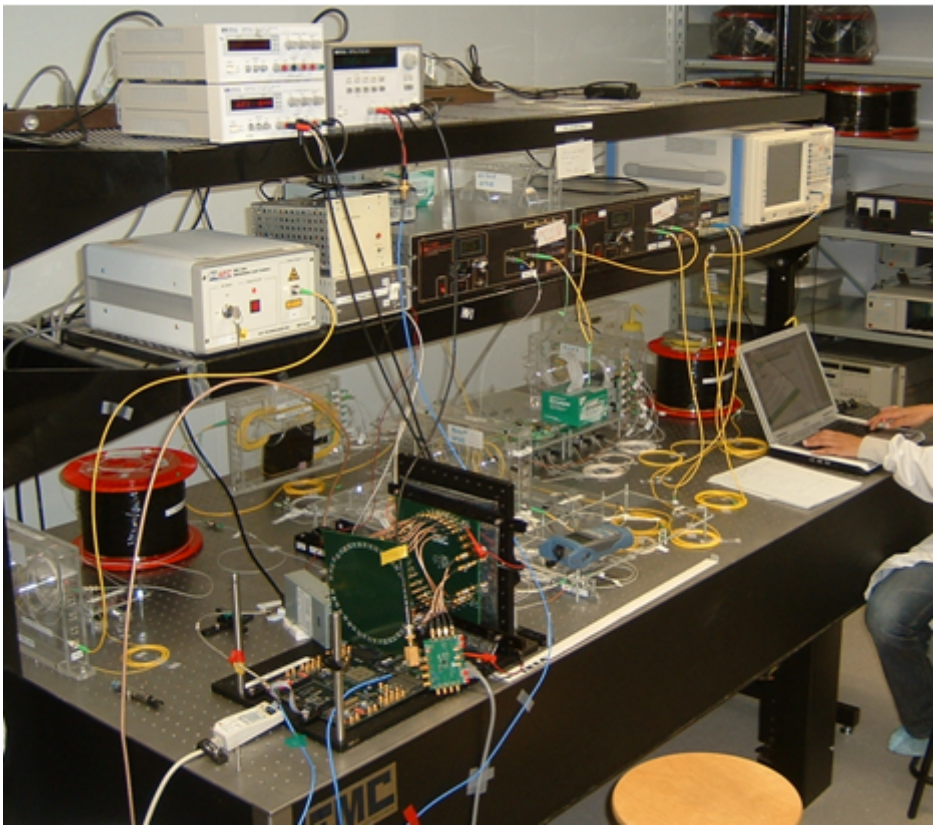


Fig. 6.6 Photograph of the 20-km GEPON uplink experimental setup to test the BM-CDR.

GPON standard is used as a test signal in our experiments and is depicted in Fig. 6.7. Packet k, with amplitude A_k, and phase φ_k, consists of 64 guard bits, 0-108 (l) preamble bits, 20 delimiter bits, 2^{15} payload bits, and 48 comma bits. The guard, preamble, and delimiter bits correspond to the physical-layer upstream burst-mode overhead of 24 bytes. The guard bits provide distance between two consecutive packets to avoid collisions. The preamble is split into two fields, a threshold determination field (TDF) for amplitude recovery and a CPA field for clock-phase recovery. The delimiter is a unique pattern indicating the start of the packet to perform byte synchronization. Likewise, the comma is a unique pattern to indicate the end of the payload. The payload is simply a non-return to zero (NRZ) $2^{15}-1$ PRBS with a zero appended at the end. The PLR and the BER are measured on the payload bits only.

Table 6.1 Upstream burst-mode overhead PON parameters

	Data Rate [Mb/s]	Guard Time [bits]	Preamble [bits]	Delimiter [bits]
GPON [19]	1244.16	32	44	20
	2488.32	64	108	20
GEPON [18]	1250	1280	1040	32

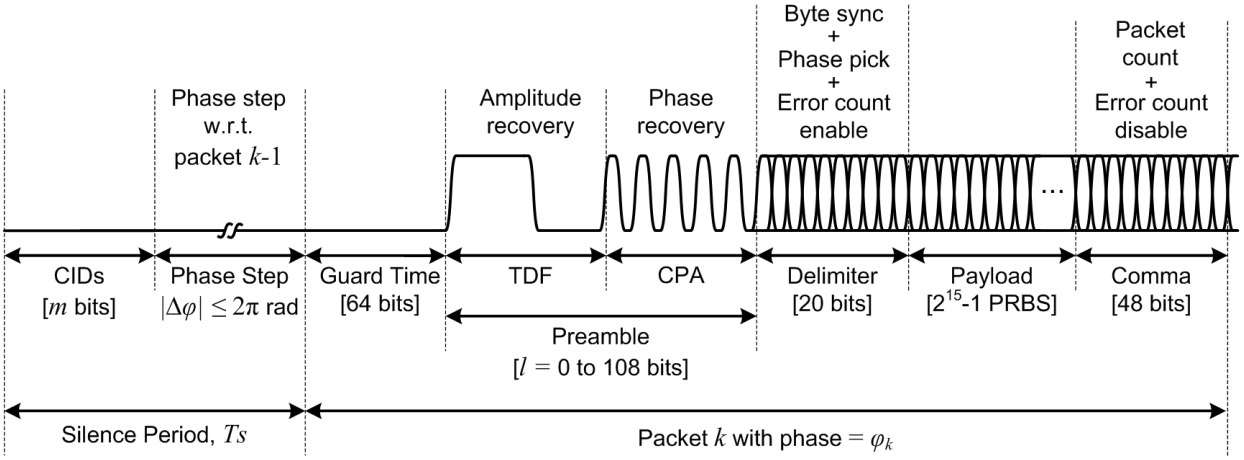


Fig. 6.7 Typical burst-mode uplink test signal and specification at 5 Gb/s (CIDs: consecutive identical digits; CPA: clock phase alignment; PRBS: pseudorandom binary sequence; TDF: threshold determination field).

Measurement Methodology

In our BM-TS, we can set the amplitude and relative phase of the packets, the preamble length, the length of CIDs, and control the received signal power. This consequently makes it possible to fully and correctly characterize CDRs and BM-CDRs—the device under test (DUT). In this context, we outline the following measurement methodologies.

1) Phase Acquisition Time: To measure the phase acquisition time accurately, packet 1 is made to serve as a dummy packet to force the DUT to lock to a certain phase φ_1, before the arrival of packet 2 with phase φ_2. The CID length is set to zero for this measurement. The BER and PLR measurements are made on packet 2 only. For a given phase step $|\Delta\varphi| \leq 2\pi$ rad, we measure the lock acquisition time of the DUT by increasing the length of the preamble l, until we obtain error-free operation, which we define as a BER $< 10^{-10}$ and a PLR of zero for over three minutes at 5 Gb/s ($> 30^6$

packets received). As already explained in Section 5.3, this method of measuring the phase acquisition time is more accurate than the qualitative method of monitoring the CDR's VCO control voltage [24]. In the latter case, the phase acquisition time is determined by measuring the settling time of the VCO control voltage envelope to within a certain percentage (usually 2–5%) of the steady-state value. The drawback of this method is that it overestimates the lock acquisition time as it is not necessary for the clock to be perfectly aligned with the data before the payload becomes valid.

2) CID Immunity: We measure the CID immunity of the DUT by inserting m ZEROs between the consecutive packets, until error-free operation can no longer be maintained. The preamble length is set to zero for this measurement. The phase step can be varied to observe the effects on the CID immunity. In this case, packet 1 is made to serve as a dummy packet, while BER and PLR measurements are made on packet 2 only.

3) Frequency Acquisition Range: The frequency lock range of the DUT is measured by tuning the frequency of the VCO away from the desired bit rate until error-free operation can no longer be maintained. The effect of phase steps can also be examined; however, the preamble length and CID length are both set to zero for this measurement.

4) Sensitivity Measurements: Sensitivity measurements of the DUT are made possible by adjusting the power level of the received packets until error-free operation can no longer be maintained. The CID length is set to zero for this measurement; however, the preamble length and phase step can both be varied to measure the burst-mode sensitivity penalty.

5) Dynamic Range: Finally, to measure the dynamic range of the DUT, we fix the amplitude A_1 of packet 1, and increase or decrease the amplitude A_2 of packet 2, until the DUT can no longer maintain error-free operation on packet 2. The phase step, preamble length, and CID length, are all set to zero for this measurement.

6.3.3 Experimental Results

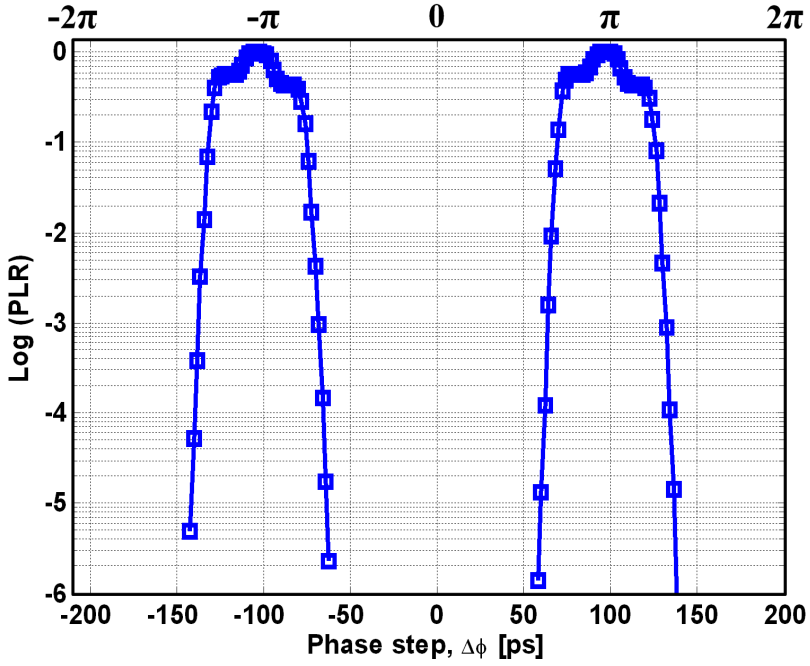
This section is devoted to the presentation and analysis of the experimental results obtained by testing our BM-CDR in the 20-km PON uplink testbed. We investigate the effect of phase step between consecutive packets, received signal power, frequency offset between the

sampling clock and desired bit rate, and length of CIDs, on the BER and PLR performance of the BM-CDR. We characterize the BM-CDR in terms of the phase acquisition time, burst-mode sensitivity penalty, frequency lock range, CID immunity, and dynamic range. Where appropriate, comparisons have been made with the predictions from the theoretical analysis in Chapter 5, thereby validating the probabilistic theoretical model in Chapter 4.

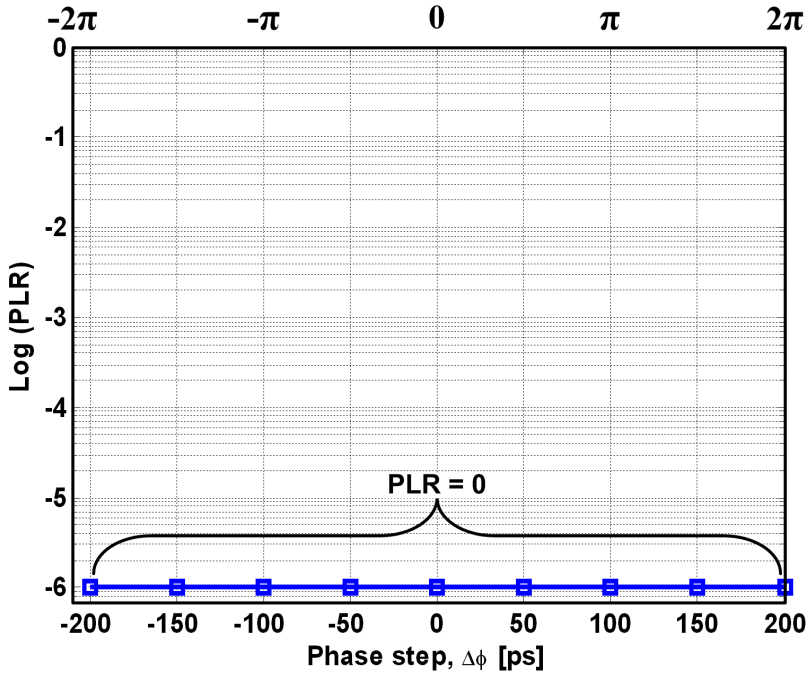
Phase Acquisition Time

Here we study the PLR performance of the CDR and the BM-CDR as a function of the phase step $|\Delta\varphi| \leq 2\pi$ rad, with *no* preamble bits. Note that 1 UI or 2π rad corresponds to 200 ps at 5 Gb/s. The methodology for measuring the phase acquisition time is delineated in Section 6.3.2. As shown in Fig. 6.8(a), with only the CDR (CPA turned OFF) we observe, as expected two bell-shaped curves centered at approximately ± 100 ps because these represent the half-bit periods corresponding to the worst-case phase steps at $\Delta\varphi = \pm\pi$ rad, respectively. It follows that the CDR is sampling at the edge of the data eye, resulting in a PLR ~ 1. We note that the slight shift of 4 ps from ± 100 ps is attributed to the sampling point of the recovered clock not being exactly at the center of the data eye. This may be as a result of: (1) VCO phase noise due to jitter generation by the CDR circuit; and (2) data bits being neither symmetric nor having the same slope for the rise and fall times leading to different distribution of jitter on the edges of the data bits. At relatively small phase steps (near 0 or $\pm 2\pi$ rad), we can easily achieve zero PLR because the CDR is sampling near the middle of each bit. Preamble bits ("$1010\cdots$"pattern) can be inserted at the beginning of the packets to help the feedback loop of the CDR settle down and acquire lock. As the preamble length is increased, there is an improvement in the PLR. After 125 preamble bits, as also explained in Section 5.3, we perceive error-free operation for any phase step. However, the use of the preamble reduces the effective throughput and increases delay. On the other hand, by switching ON the burst-mode functionality of the receiver with the CPA, as illustrated in Fig. 6.8(b), we observe error-free operation for any phase step with zero preamble bits, allowing for instantaneous phase acquisition. This is as predicted by the theoretical model.

It should be noted that whereas $|\Delta\varphi| = \pi$ rad represents the worst-case phase steps for the CDR sampling at the bit rate, $|\Delta\varphi| \in \{\pi/2 \text{ rad}, 3\pi/2 \text{ rad}\}$ phase steps are the worst-case scenario for the BM-CDR as it is based on an oversampling CDR at $2\times$ the bit rate. We



(a)



(b)

Fig. 6.8 PLR performance versus phase step for a zero preamble length. (a) Conventional CDR. (b) BM-CDR.

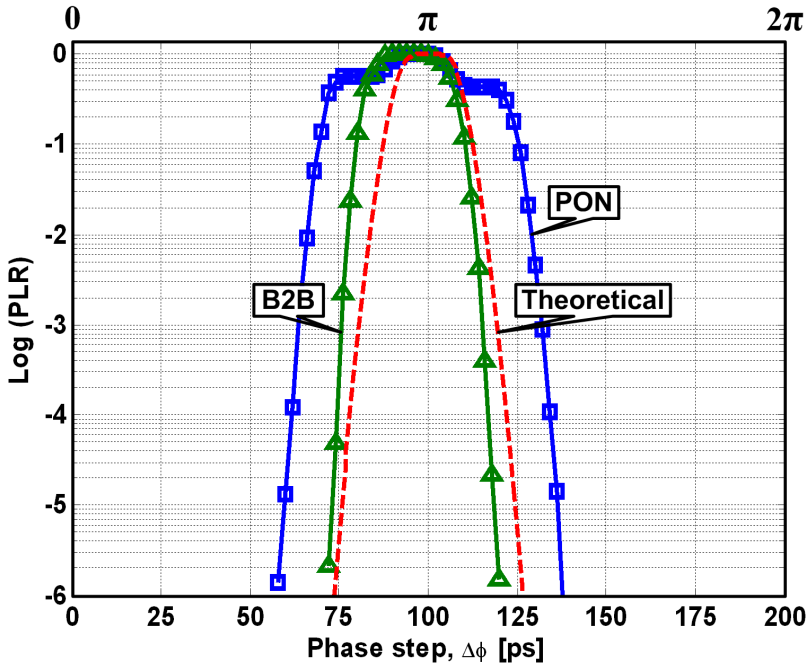


Fig. 6.9 PLR performance of the CDR versus phase step with no preamble bits in a B2B- and PON architecture, compared to the theoretical model.

note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [25, 26]. However, by reducing the phase acquisition time as demonstrated in this work—and therefore the length of the CPA field—more bits are left for amplitude recovery, thus reducing the burst-mode sensitivity penalty. Alternatively, with the reduced number of preamble bits, more bits can be left for the payload, thereby increasing the information rate. Instantaneous phase acquisition also has a significant improvement impact in the physical efficiency of the upstream PON traffic. This is further discussed in the next few Sections.

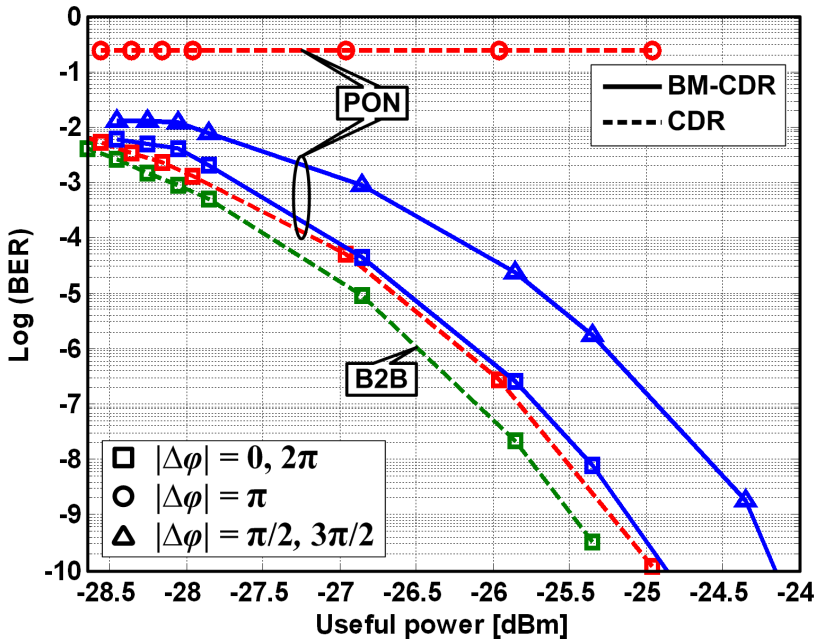
In Fig. 6.9, we compare the experimental and theoretical PLR performance of the CDR with no preamble bits. We have restricted the horizontal axis to values from $0 \leq \Delta\varphi \leq 2\pi$ rad (0 to 200 ps), as the results are symmetrical about 0 rad from $-2\pi \leq \Delta\varphi \leq 0$ rad. We first evaluate the PLR performance obtained in the PON architecture with the 20-km of fiber to the one in a back-to-back (B2B) configuration without the fiber. The "flatness" of the curve near the worst-case phase step $\Delta\varphi = \pi$ rad in the PON architecture is a manifestation of the presence of deterministic jitter as a result of channel impairments. This may include ISI, pulsewidth-distortion jitter (PWDJ), and data-dependent jitter (DDJ).

Next, we compare these results with the theoretical model by plotting (4.40) with the RMS jitter on the sampling clock $\sigma_{t_s} = 0.025$ UI. It can be seen that the curve spread of PLR performance in the B2B architecture is $9.8\sigma_{t_s}$ at PLR $= 10^{-6}$ whereas that obtained theoretically is $10.6\sigma_{t_s}$. This signifies that the results are in close agreement, albeit for the 4 ps shift in the experimental plots due to the non-ideal sampling point location determined by the CDR which as mentioned is most likely due to the VCO phase noise.

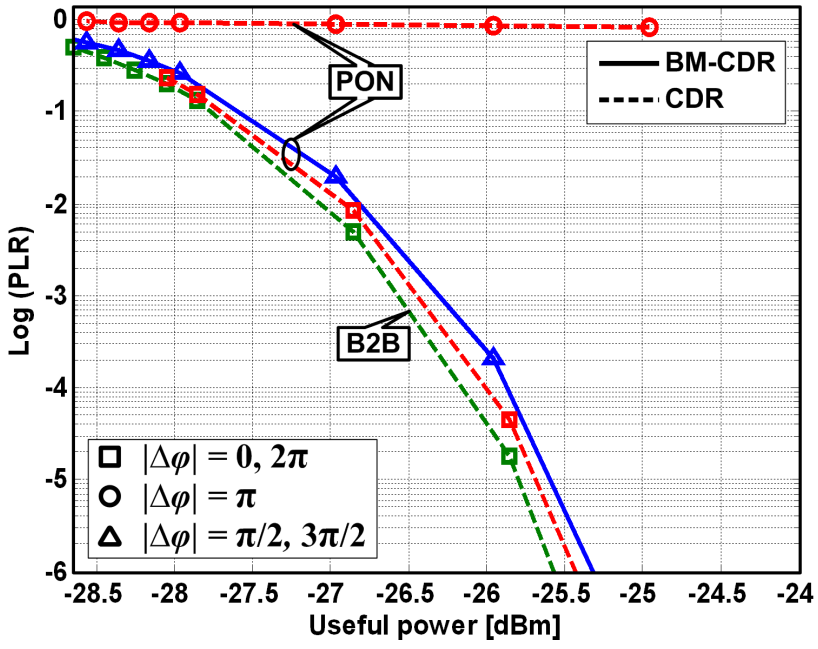
Burst-Mode Sensitivity Penalty

Consider the experimental results in Fig. 6.10 which shows the BER and PLR performance of the CDR and BM-CDR as a function of the received signal power for different phase steps. Note that the abscissa is the useful power, that is, the optical power contributed at the photodiode. To determine the burst-mode penalty of the receiver, the performance of the CDR sampling continuous data ($\Delta\varphi \in \{0 \text{ rad}, \pm 2\pi \text{ rad}\}$) at the bit rate is compared to the performance of the BM-CDR sampling bursty data with a worst-case phase step ($|\Delta\varphi| \in \{\pi/2 \text{ rad}, 3\pi/2 \text{ rad}\}$). Both measurements are made with a 0-bit preamble. Due to the 2×-oversampling (faster electronics) and the phase picking algorithm, we observe a 0.8-dB penalty in the BER performance as shown in Fig. 6.10(a); however, in the case of the PLR performance, the penalty is negligible due to the CPA as depicted in Fig. 6.10(b). It can also be observed that the BM-CDR achieves BER and PLR sensitivities of -24.2 dBm and -25.4 dBm, respectively, for the worst-case phase steps in the link. On the other hand, the CDR will not be able to recover any packets if there exists a worst-case phase step, regardless of the received signal power, resulting in a PLR ~ 1. However, by increasing the length of the preamble, the PLR performance of the CDR will tend to be comparable to that obtained with zero preamble bits and no phase steps. Hence, for the worst-case phase steps in the uplink, there is a trade-off between the sensitivity penalty obtained by employing the BM-CDR over the CDR, and the number of preamble bits required without the BM-CDR. Since random silence periods in the PON uplink are inevitable, the power penalty may be a small price to achieve error-free operation.

It should also be noted that the sensitivity penalty, 0.4-dB and 0.14-dB in the BER and PLR performance, respectively, between the B2B architecture and the PON architecture is minimal. This implies that the uplink does not need to be compensated by introducing dispersion compensation fiber (DCF), semiconductor optical amplifiers (SOA),



(a)



(b)

Fig. 6.10 BER and PLR performance of the CDR and BM-CDR versus useful power in a B2B architecture and PON architecture for different phase steps with no preamble bits.

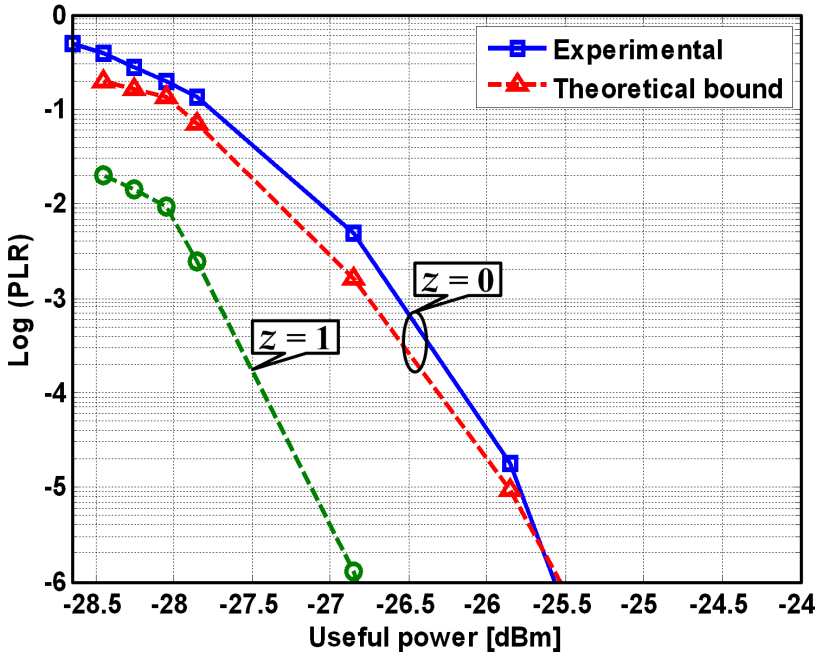


Fig. 6.11 Comparison of the theoretical and experimental PLR performance of the BM-CDR versus useful power.

or erbium-doped fiber amplifiers (EDFAs), as is generally necessary in a wavelength-division multiplexing (WDM) PON or optical code-division multiple access (OCDMA) PON [27].

We theoretically predict the PLR performance of the BM-CDR in the PON architecture as a function of the received signal power, with a pattern correlator having an error-resistance of $z = 0$ bit, and compare it to the experimental result in Fig. 6.11. The theoretical and experimental results are in close agreement. By increasing the pattern correlator error-resistance to $z = 1$ bit, an improvement of $\sim$1.5 dB in the sensitivity can be expected.

PON Efficiency

Dynamic bandwidth allocation (DBA) is generally employed in high-speed communication services, such as a PON system, to effectively assign the shared resource on demand to each ONU according to their respective requests [28]. Several DBA algorithms for PONs have been proposed in literature [29, 30], in which the upstream traffic is allocated according to the ONUs' request in every time cycle. In a PON link, the physical efficiency of the

upstream traffic E_{us}, is defined as [31]

$$E_{\text{us}} = 1 - \frac{n_{\text{ONU}} \cdot t_{\text{oh}}}{T_{\text{DBA}}} \tag{6.1}$$

where n_{ONU} is the number of ONUs in the PON, t_{oh} is the physical overhead time, and T_{DBA} is the cycle for bandwidth allocation. T_{DBA} can be expressed as

$$T_{\text{DBA}} = RTT + t_{\text{delay}} \tag{6.2}$$

where RTT is the round-trip time between the OLT and the ONU, and t_{delay} is the time required for bandwidth allocations other than the RTT. In a 20-km link, the round-trip time $RTT \sim 200\ \mu$s with light propagating at $\sim 5\ \mu$s/km in a SMF. Thus, the cycle for bandwidth allocation $T_{\text{DBA}} \geq 200\ \mu$s. The overhead time t_{oh} is represented as

$$t_{\text{oh}} = t_{\text{gt}} + t_{\text{pre}} \tag{6.3}$$

where t_{gt} is the guard time between back-to-back upstream bursts from different ONUs and mostly dependent on the laser ON and OFF times, and t_{pre} is the preamble time required for the BMRx to settle down and completely synchronize for each burst input in terms of the amplitude and the phase. In the GEPON standard [18], the overhead time $t_{\text{oh}} = 1856$ ns, the guard time $t_{\text{gt}} = 1024$ ns, when the overlap between the laser ON and OFF times is not considered, and the preamble time $t_{\text{pre}} = 832$ ns, of which 400 ns is for the amplitude recovery and 432 ns is for the phase acquisition. Hence, assuming 32 ONUs, an upstream efficiency $E_{\text{us}} \sim 70\%$, is obtained for the GEPON standard with a bandwidth allocation cycle $T_{\text{DBA}} = 200\ \mu$s.

In Fig. 6.12, we plot contours of the PON upstream efficiency that result as a function of the required preamble time and guard time. Since our BM-CDR provides instantaneous (0 preamble bit) phase acquisition, thus a high upstream efficiency $E_{\text{us}} \sim 99\%$, is expected for 32 ONUs and 200-μs T_{DBA}. Compared to the GEPON standard, this is a 24% improvement even though the bit-rate is four times higher. The burst-mode amplitude recovery circuit in [31], achieves an efficiency of 97%. In this context, our works can seamlessly integrate, albeit with a 2% trade-off in the upstream efficiency. In addition, note that the guard time is limited by the laser ON and OFF times. A shorter guard time and thus a higher upstream efficiency can be obtained when transmitters with faster response times become

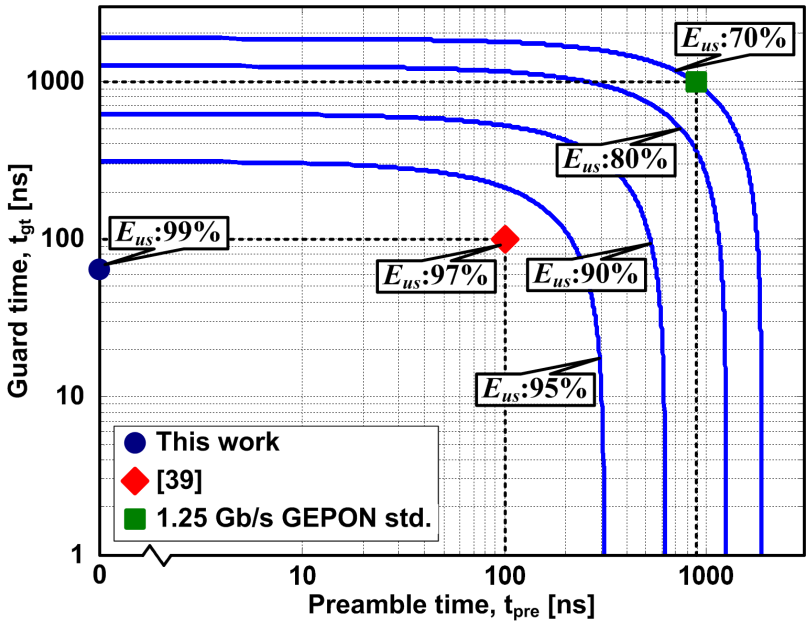


Fig. 6.12 Physical efficiency of the upstream PON traffic as a function of the preamble time and guard time.

available.

Frequency Acquisition Range

We measure the frequency acquisition range of the BM-CDR with the methodology outlined in Section 6.3.2 with the received signal power kept at −24 dBm. Fig. 6.13 shows the PLR performance of the BM-CDR in the presence of frequency offset. The frequency lock range of the BM-CDR is measured to be 242 MHz. Based on the theoretical analysis in Section 5.6, the lock range (maximum bound) is estimated to be 590 MHz. This discrepancy of ∼350 MHz can be expected as the finite frequency offset model is an optimistic estimation as it does not account for the jitter generated by the CDR circuitry. Jitter generation refers to the jitter produced by a circuit itself when the input random data contains no jitter. The sources of jitter are as follows [32]: (1) VCO phase noise due to electronic noise of its constituents devices; (2) ripple on the control voltage; (3) coupling of data transitions to the VCO through the phase detector and retiming circuits; and (4) supply and substrate noises. All these sources of jitter can considerably deteriorate the result.

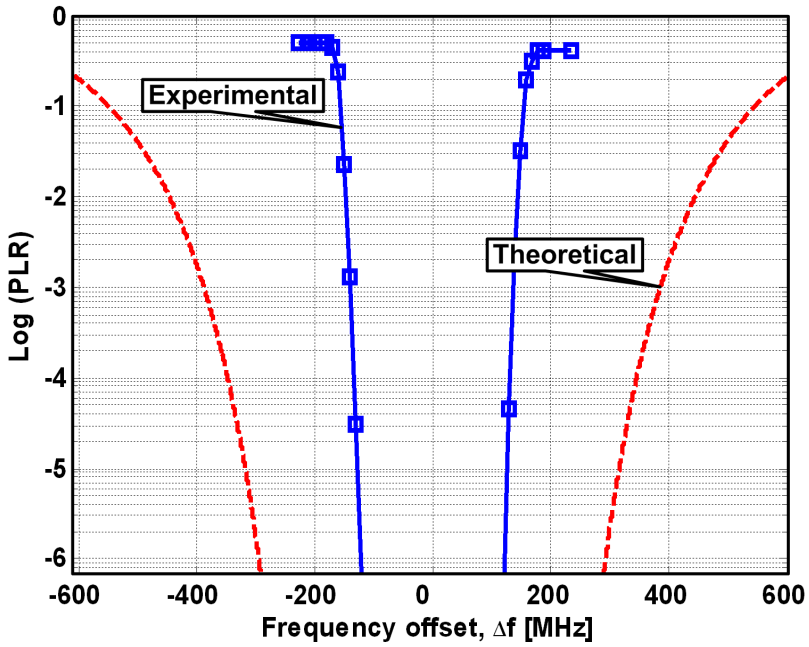


Fig. 6.13 Comparison of the theoretical and experimental PLR performance of the BM-CDR versus frequency offset.

CID Immunity

The PLR performance of the CDR and BM-CDR as a function of the length of CIDs is depicted in Fig. 6.14. The CID immunity is measured with the methodology in Section 6.3.2. The received signal power is kept at -24 dBm. The CDR can only support 500 CIDs with error-free operation, whereas the BM-CDR can support approximately six times this value, that is, 3100 CIDs. As the length of the CIDs is increased, the phase error between the two successive bursts can accumulate up to $|\Delta\varphi_e| = \pi$ rad resulting in a PLR ~ 1. In the case of the CDR, this happens when the CID length is roughly a 1000 bits, while for the BM-CDR it is 3500 bits. It can be inferred theoretically from Fig. 5.8(b), that a CID length of 3500 bits for the BM-CDR corresponds to a frequency offset of 1.73 MHz, implying a CID length of $\sim$1600 bits for the CDR. While the experimental results and the theoretical results are within the same order of magnitude, there is however, still a discrepancy. This is expected, as mentioned earlier, as the finite frequency offset model does not account for the jitter generated by the circuit. It should be noted that in addition to the length of CIDs, when a worst-case phase step is introduced between consecutive packets, the CDR regardless of its CID immunity will result in a PLR ~ 1. This is not the case with

the BM-CDR, which as demonstrated is immune to any phase step between consecutive packets.

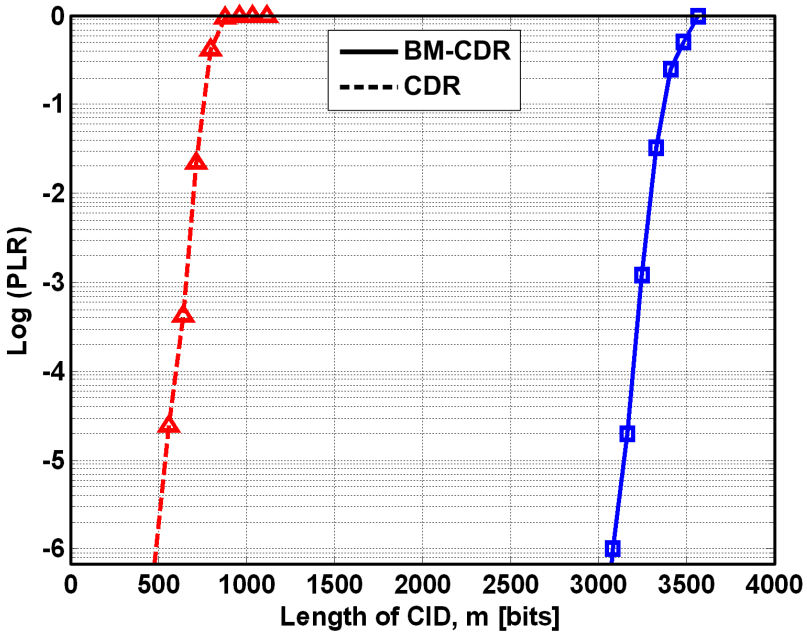


Fig. 6.14 PLR performance of the CDR and BM-CDR versus length of CID.

Dynamic Range

The methodology for measuring the dynamic range of a circuit is explained in Section 6.3.2. In a PON system, the BMRx front-end at the OLT is responsible for amplitude recovery. Thus, the dynamic range of the BM-CDR does not carry much value. However, with the application of the BM-CDR to optical burst/packet-switched networks which may require a cascade of BM-CDR, the dynamic range of the BM-CDR may seem useful. In either case, the measurement of the dynamic range verifies the functionality of the BM-TS.

The worst-case scenario is when a low amplitude packet follows a high amplitude packet [33]. The dynamic range of the BM-CDR is measured to be 3 dB. This also relaxes the requirements of the output voltage swings/fluctuations from a preceding circuit at high data rates. The dynamic range can easily be increased to more than 15 dB by integrating a front-end consisting of a burst-mode amplitude recovery circuit [31].

Recovered Clock Spectrum

The output spectrum of the recovered clock is shown in Fig. 6.15. The phase noise at 100-kHz, 500-kHz, and 1-MHz, is approximately −40 dBc/Hz, −77 dBc/Hz, and −80 dBc/Hz, respectively. Note that the spectrum analyzer attenuates the input signal by 30 dB internally.

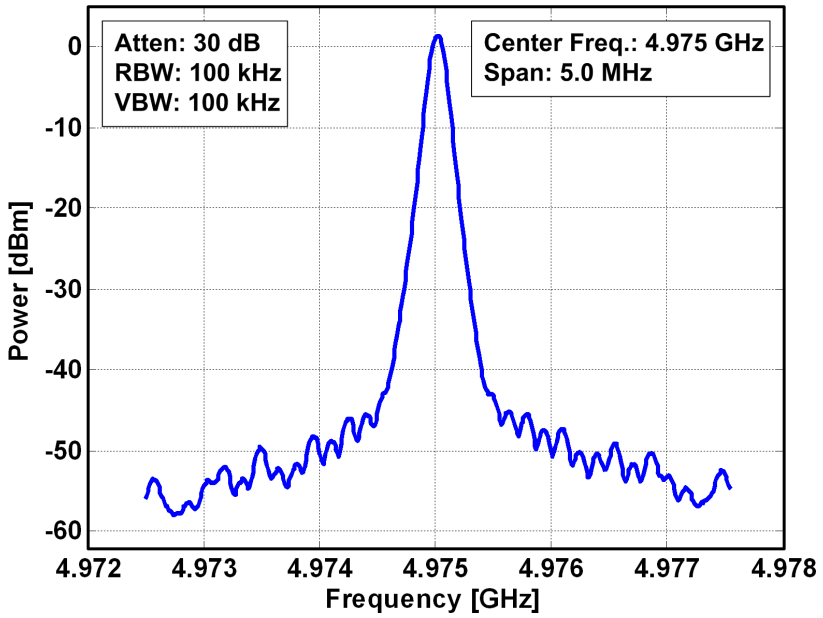


Fig. 6.15 Recovered clock spectrum (Atten: attenuation; Freq: frequency; RBW: resolution bandwidth; VBW: video bandwidth).

6.3.4 Conclusion

We experimentally investigated the effect of phase step, received signal power, frequency offset, and length of CIDs, on the BER and PLR performance of the BM-CDR in a 20-km PON uplink. Our burst-mode test solution, aided by the new measurement methodology based on both BER and PLR, can measure the amplitude, frequency, phase acquisition times of devices like synchronous optical network (SONET) CDRs, BMRx amplitude recovery circuits, BM-CDRs, and frequency synthesizers. We characterized the BM-CDR in terms of the phase acquisition time, burst-mode sensitivity penalty, frequency lock range, CID immunity, and dynamic range. In a nutshell, the BM-CDR achieves a BER $< 10^{-10}$ and PLR $< 10^{-6}$ while featuring: (1) instantaneous (0 preamble bit) phase acquisition

for any phase step $|\Delta\varphi| \leq 2\pi$ rad; (2) BER and PLR sensitivities of -24.2 dBm and -25.4 dBm, respectively; (3) negligible burst-mode (phase acquisition) sensitivity penalty of 0.8 dB; (4) frequency acquisition range of 242 MHz; (5) CID immunity of 3100 bits; and (6) dynamic range of 3 dB. This analysis coupled with the experimental results will help refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets. Instantaneous phase acquisition can increase the effective throughput of the system by increasing the information rate, and also dramatically improve the physical efficiency of the upstream PON traffic to 99% for 32 ONUs. The price to pay to obtain instantaneous phase acquisition is faster electronics. On the other hand, our solution is to leverage the design of components for long-haul transport networks using low-complexity, commercial electronics providing a cost-effective solution for PON BM-CDRs. These components are typically a generation ahead of the components for multiaccess networks. Thus, our solution will scale with the scaling for long-haul networks.

Author's Contribution

The author of this thesis: (1) designed and implemented the BM-CDR employed for this study; (2) built the burst-mode experimental setup (PON test bed) and developed the measurement methodology; and (3) carried out all the experiments, analyzed the results, and characterized the BM-CDR.

Acknowledgment

The author would like to acknowledge the following individuals for their contributions during the early phases of this project. Dr. Julien Faucher designed and implemented the original CPA in VHDL on a Virtex-II Pro FPGA board at 622 Mb/s. He also built the custom SMB-to-QSE interface PCB. Ms. Ming Zeng and Mr. Nicholas Zicha, M.Eng. students, assisted in porting the VHDL code of the CPA from the 622-Mb/s version on the Xilinx-II Pro FPGA board to the 5-Gb/s version on the Xilinx Virtex-IV FPGA board, and provided technical assistance.

6.4 2.5 Gb/s Overlapped-SCM WDM PON 20-km Uplink Experiments

We experimentally show burst-mode reception at 2.5 Gb/s in a 20-km overlapped subcarrier-multiplexing wavelength-division multiplexed PON uplink. The receiver employed in this study is a variant of the BM-CDR based on semiblind oversampling in the space domain (see Section 3.4). The work presented in this section is a result of the research published in [34, 35].

6.4.1 Introduction

Subcarrier-multiplexing (SCM) has been widely proposed for single-feeder wavelength-division multiplexed (WDM) PON architectures [36]. Among the other techniques used to mitigate Rayleigh backscattering effect [37], SCM is preferred due to its simplicity and low cost. However, when used with reflective semiconductor optical amplifier (RSOA) optical network units (ONUs), symmetrical gigabit per second bit rates are difficult to achieve because of the bandwidth limitations of the RSOA. In other words, the subcarrier frequency and the bit rates are carefully chosen to separate the uplink and downlink enough and to accommodate them within the modulation bandwidth of the RSOA [38].

Recently, we have proposed an overlapped-SCM (O-SCM) technique that allows a certain overlap between uplink and downlink, to maximize the spectrum usage of the RSOA [39]. A global clock was used to provide perfect synchronization between both optical line terminal (OLT) and ONU for proper SCM operation. However, in a real system a CDR unit is needed at the OLT. Furthermore, a phase aligner may be needed to support bursty uplink traffic and/or to correct for any phase shifts due to inherent signal jitter or other timing impairments.

In this work, we demonstrate a symmetric 2.5 Gb/s O-SCM WDM PON using a burst-mode (BM) receiver at the OLT that can capture instantaneous phase variations within the uplink for a robust SCM operation. For SCM applications the recovered clock is at a higher frequency, therefore a clock divider is needed before down-conversion. For a proof-of-concept SCM burst-mode operation, we had to modify the design of the BM-CDR (based on semiblind space domain oversampling) to perform perfect alignment between the recovered frequency divided clock and the uplink data for efficient O-SCM down-conversion. We also

propose a general SCM BM-CDR by replacing the Alexander *bang-bang* phase detector with a linear Hogge phase detector.

6.4.2 WDM PON with Overlapped-SCM

Fig. 6.16 shows the architecture of our overlapped-SCM WDM PON using an electro-absorption modulated laser (EML) at the OLT and a 2 GHz bandwidth-limited RSOA at the ONU side. The downlink is sent at 2.5 Gb/s over baseband with 2.43 dB extinction ratio (ER), whereas the uplink is sent at 2.5 Gb/s over a 2.5 GHz electrical RF subcarrier with a higher ER to trade-off downlink performance versus uplink efficient data remodulation. At the ONU, 70% of the downlink power is used to saturate the RSOA for proper downlink erasure, whereas the remaining 30% of power is passed to the downlink receiver. That coupling ratio was already optimized in [39] to guarantee error-free operation for both uplink and downlink with minimum OLT launch power. Different lengths of non-return to zero (NRZ) PRBS are used for downlink and uplink similar to [39]. An EDFA and a VOA are used at the OLT to vary the OLT launch power (measured at the circulator output port '2') for the purpose of measurements. The proposed BM receiver is used at the OLT for clock and data recovery, instantaneous phase acquisition and efficient SCM down-conversion. In that experiment we test the receiver by applying phase steps within the uplink data but without introducing silence periods. The situation emulates phase instabilities that may be caused by inexpensive ONU parts and the bursty nature of the uplink.

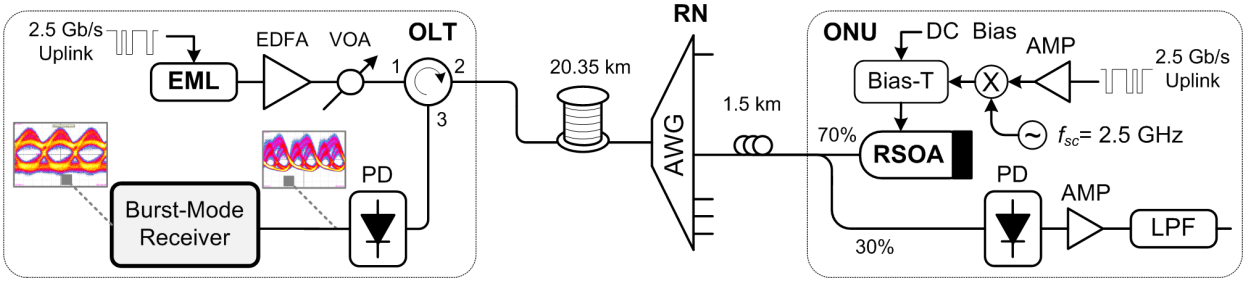


Fig. 6.16 Proposed WDM PON architecture with overlapped-SCM (AWG: arrayed waveguide grating, EDFA: erbium-doped fiber amplifier; f_{sc}: sub-carrier frequency; PD: photodiode, RN: remote node, VOA: variable optical attenuator).

6.4.3 SCM Burst-Mode Receiver Design

The architecture of the proposed proof-of-concept SCM burst-mode receiver is shown in Fig. 6.17. A clock recovery unit is used to extract a 5 GHz clock CK_o, from the 2.5 Gb/s O-SCM uplink received signal. The clock signal is then sent to some phase shifters to generate multiple clocks: $CK_{-\pi/2}$ and $CK_{+\pi/2}$, with low skew and different phases: $-\pi/2$ rad and $+\pi/2$ rad, respectively, with respect to CK_o. Next, the phase shifted clocks are passed to a phase picker circuit. At the same time, a bang-bang Alexander phase detector [40] compares CK_o with the incoming data D_{in}, to indicate whether it is leading or lagging. This information is used as a control signal by the phase picker to select the proper clock, either $CK_{-\pi/2}$ or $CK_{+\pi/2}$, which is in phase with the uplink data D_{in}. A clock frequency divider (in this case to go from 5 GHz to 2.5 GHz) then drives the RF mixer for SCM down-conversion. Because we are using here a 2-state phase detector, our proof-of-concept receiver will only be able to operate at two different states; that is, phase shifts of $-\pi/2$ rad and $+\pi/2$ rad. For experimental convenience, a phase shifted version of CK_o divided by 2 is used when no phase shifts are introduced. At the receiver output, a 1.875 GHz low-pass filter is used to remove out-of-band noise.

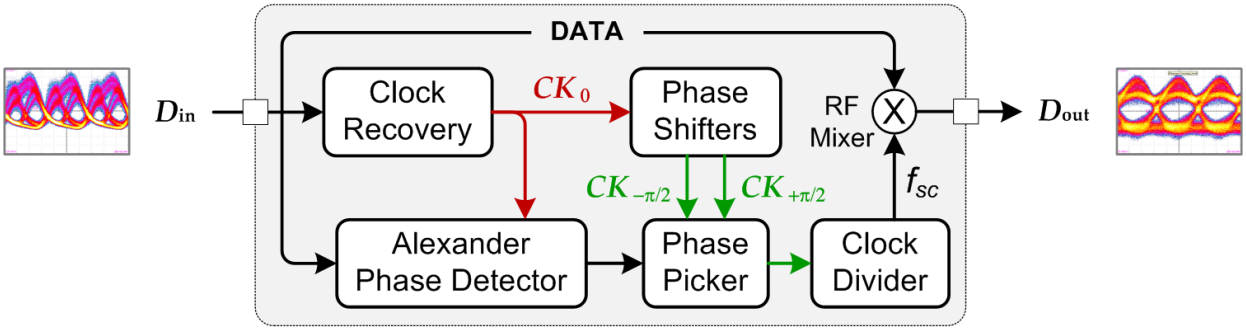


Fig. 6.17 Proof-of-concept burst-mode receiver for SCM applications using a bang-bang Alexander phase detector.

Fig. 6.18 shows the electrical eye diagrams of the received uplink signal (measured at the receiver input) for different phase shifts: 0 rad, $-\pi/2$ rad, and $+\pi/2$ rad. The optimum sampling instants are marked with the dotted black line in the middle of the eye. The 2.5 GHz versions of CK_o and $CK_{\pm\pi/2}$ to be used for down conversion are also shown. It can be seen that CK_o is only valid for the case of 0 rad phase shift, whereas for the cases of $-\pi/2$ rad and $+\pi/2$ rad phase shifts, the receiver has the ability to select between $CK_{-\pi/2}$

and $CK_{+\pi/2}$, respectively, for an efficient SCM down-conversion.

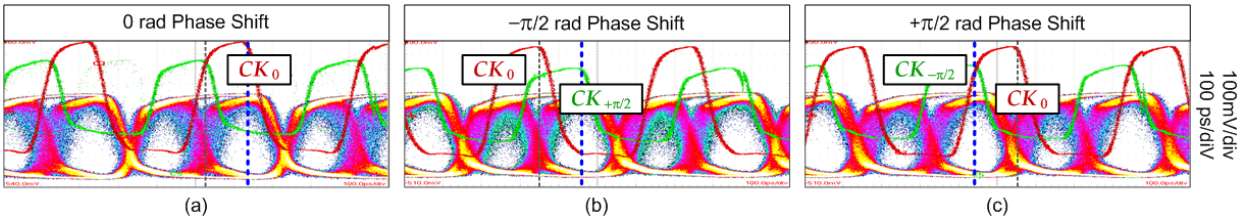


Fig. 6.18 Electrical eye diagrams before down-conversion for different phase shifts: (a) 0 rad; (b) $-\pi/2$ rad; and (c) $+\pi/2$ rad.

To make the receiver able to instantaneously track phase variations over a full 0 rad to $\pm\pi$ rad range, we propose replacing the Alexander phase detector with a linear Hogge phase detector [41]. In this case, the output of the phase detector would simply control a phase shifter that adjusts the phase of CK_o before being passed to the clock divider and the RF mixer.

6.4.4 Experimental Demonstration and Results

The performance of our overlapped-SCM WDM PON with the proposed SCM burst-mode proof-of-concept receiver is shown in Fig. 6.19. A 20.35 km feeder and 1.5 km distribution drop fiber all in standard single-mode fiber (SMF-28e+) are used at the optical distribution network (ODN) with a 100 GHz arrayed waveguide grating (AWG) at the remote node.

Fig. 6.19 shows the Q factor versus the OLT launch power for the different phase shifts presented in Fig. 6.18. When no phase steps introduced to the upstream, simply CK_o is used and the best Q factor can be achieved. As expected, the Q factor increases with the launch power. We have measured a Q factor of 14.25 dB at 6.65 dBm of launch power and corresponding to a BER of 10^{-10}. At around 9 dBm of power we achieved also error-free transmission for the downlink. Now when we have $-\pi/2$ rad and $+\pi/2$ rad phase shifts within the uplink, we can still achieve error-free operation when the correct clock $CK_{-\pi/2}$ and $CK_{+\pi/2}$, respectively, is picked by the proposed receiver. On the other hand the performance is significantly degraded when the wrong clock (CK_o) is used, that is, without phase picking. Our receiver provides more than 4 dB improvement in Q factor and guarantees error-free-operation due to its instantaneous phase picking. Eye diagrams shown in Fig. 6.20 confirm our Q factor measurements and the proof-of-concept operation.

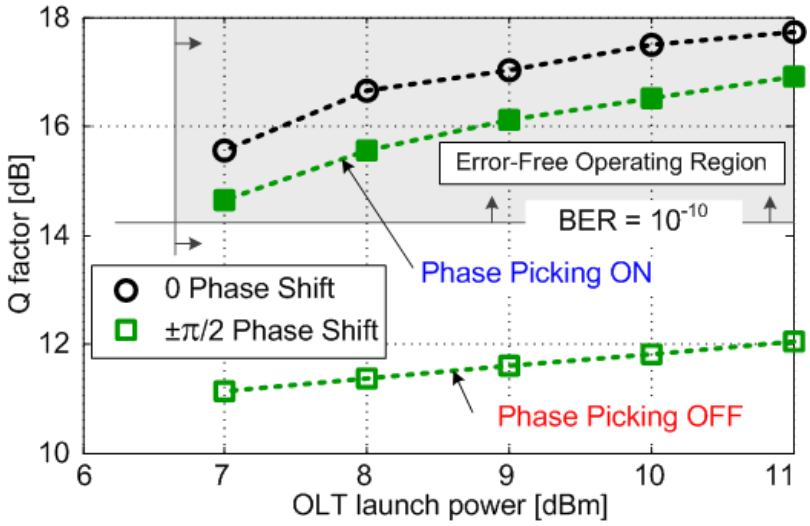


Fig. 6.19 Q factor versus OLT launch power for different phase shifts between the upstream data and the recovered clock.

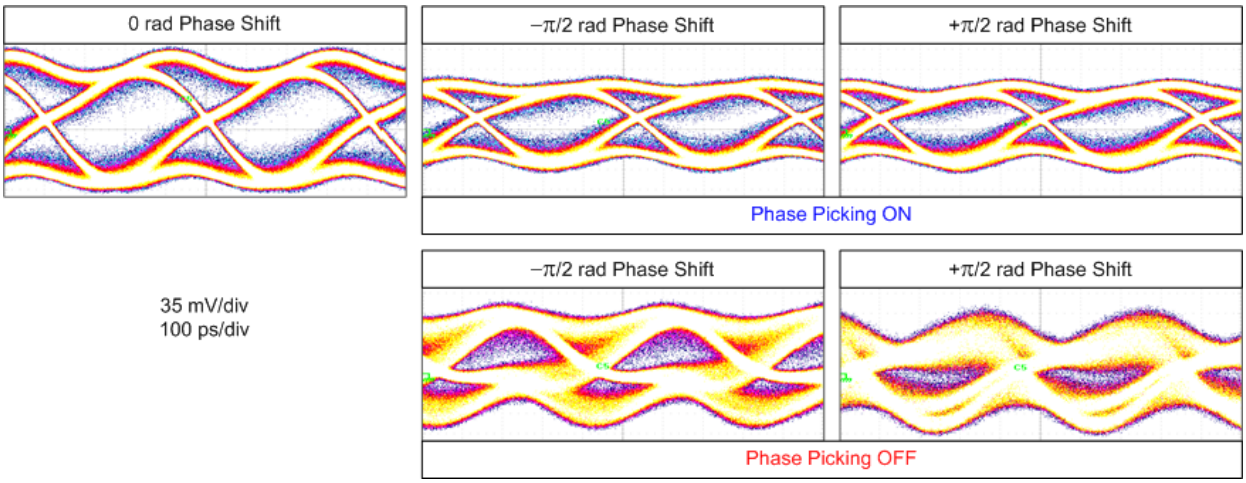


Fig. 6.20 Electrical eye diagrams after down-conversion with and without phase picking for different phase shifts: 0 rad; $-\pi/2$ rad; and $+\pi/2$ rad.

6.4.5 Conclusion

We demonstrated for the first time to our knowledge uplink burst-mode operation of a 2.5 Gb/s symmetrical WDM PON with overlapped-SCM. A proof-of-concept BM receiver based on a bang-bang Alexander phase detector was used to test the principle for $\pm\pi/2$ rad phase steps within the uplink. We showed that the receiver is able to track the instantaneous phase variations and to achieve efficient SCM down-conversion. We also suggested

guidelines for a practical receiver using a variant design with a linear Hogge phase detector.

Author's Contribution

The author of this thesis designed and implemented the BM-CDR employed for this study, participated in all the experiments, and characterized the BM-CDR.

Acknowledgment

The author would like to acknowledge the following individuals for their respective contributions. Dr. Ziad A. El-Sahn proposed, built, and characterized the O-SCM WDM PON architecture. Mr. Jonathan M. Buset, Ph.D. candidate, provided assistance in building the experimental setup.

6.5 1.25 Gb/s 1300-km Deployed Fiber Link Experiments

We experimentally demonstrate burst-mode reception at 1.25 Gb/s in a 1300-km deployed fiber link that spans from Montreal to Quebec City and back. The BM-CDR based on semiblind time domain oversampling is utilized in this study (see Section 3.3). The work presented in this section is a result of the research published in [42–44].

6.5.1 Introduction

Large scale computer networks are needed to support growing web applications that require fast and reliable interconnections to provide rapid access to information and services to millions of users. As the number of interconnected servers and storage media increases, optical technologies are expected to play a major role in the development of these local area networks (LANs) because of the high speed, low loss and small foot print of optical fiber communication links. Optical packet switched networks (OPSNs) are expected to overcome future bottlenecks in transport and access networks as they reduce the number of layers present in the current protocol stack to only two levels: Internet protocol (IP) over optical.

Much research into OPSN focuses on the optical design, while assuming the availability of high-speed electronics [45–48]. Also, the effect of channel impairments on the performance of electronic receivers has largely been overlooked. For example, silence periods between packets are inevitable and inherently arise in OPSN due to the statistical multiplexing. In fact, the sent packets only occupy capacity in the network when there is data to be routed over the network, whereas in silent periods the capacity becomes available to other traffic streams [49]. This asynchronous nature of silence periods can cause conventional receivers, CDR circuits based on phase-locked loops (PLLs), to lose pattern synchronization. Preamble bits can be inserted at the beginning of each packet to allow the CDRs enough time to acquire lock. However, this overhead reduces the effective throughput and increases delay. Consequently, to deal with busrty data, we employ our BM-CDR based on time domain semiblind oversampling in these networks. Recall, the most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible to decrease the burst-mode sensitivity penalty and thus increase the power budget or alternatively increase the information rate with more bits available to the packet payload.

In this section, we demonstrate experimentally for the first time, to our knowledge, burst-mode reception in a 1300-km deployed fiber link that spans from Montreal to Quebec City and back, over a RISQ[1] network. We note that while the round-trip distance between Montreal and Quebec City is ∼500 km, the deployed fiber link—leased from RISQ—is routed through available (unoccupied) paths through various cities which may not necessarily be the closest path. We investigate the effects of channel impairments on the performance of BM-CDR in terms of the PLR and BER, and quantify it as a function of the phase step between consecutive packets, received signal power, and consecutive identical digit (CID) immunity. We also assess the tradeoffs in preamble length, power penalty, and pattern correlator error-resistance. These results will help refine theoretical models of receivers employed in the OPSN, and provide input for establishing realistic power budgets.

6.5.2 Experimental Setup

The experimental setup illustrated in Fig. 6.21 is used to test the 1300-km deployed fiber link. A distributed-feedback (DFB) laser at 1538.98 nm is modulated by 1.25-Gb/s bursty data. Bursty traffic is generated by adjusting the phase φ_1 and φ_2, between alternating packets from two programmable ports of an Anritsu MP18000 pattern generator which are then concatenated via a radio frequency (RF) power combiner and used to drive a polarization-dependent Mach-Zehnder modulator (MZM) with an optical modulator driver also from JDSU (Model #H301-1110).

The time between two consecutive packets corresponding to the laser ON/OFF time is 16 bits. As depicted in Fig. 6.22, the packets are formed from 0 to 48 (l) preamble bits, 36 delimiter bits, $2^{15}-1$ payload bits, and 48 comma bits. The preamble bits are used to perform phase recovery. The delimiter is a unique pattern indicating the start of the packet and exploited for byte synchronization. Similarly, the comma is a unique pattern to indicate the end of the payload. The payload is simply a $2^{15}-1$ PRBS. The PLR and BER measurements are only performed on the delimiter and payload bits, respectively. Note that the lock acquisition time corresponds to the number of bits (l) needed in front of the delimiter in order to achieve error-free operation, that is, PLR $< 10^{-6}$ and BER $< 10^{-10}$, for any phase step, $|\Delta\varphi| = |\varphi_1 - \varphi_2| \leq 2\pi$ rad, between any two consecutive packets in the link. As per (2.8), a silence period, T_s, consisting of a phase step $|\Delta\varphi|$, and an all-zero

[1]Réseau d'informations scientifiques du Québec (Quebec's Scientific Information Network), `http://www.risq.qc.ca`.

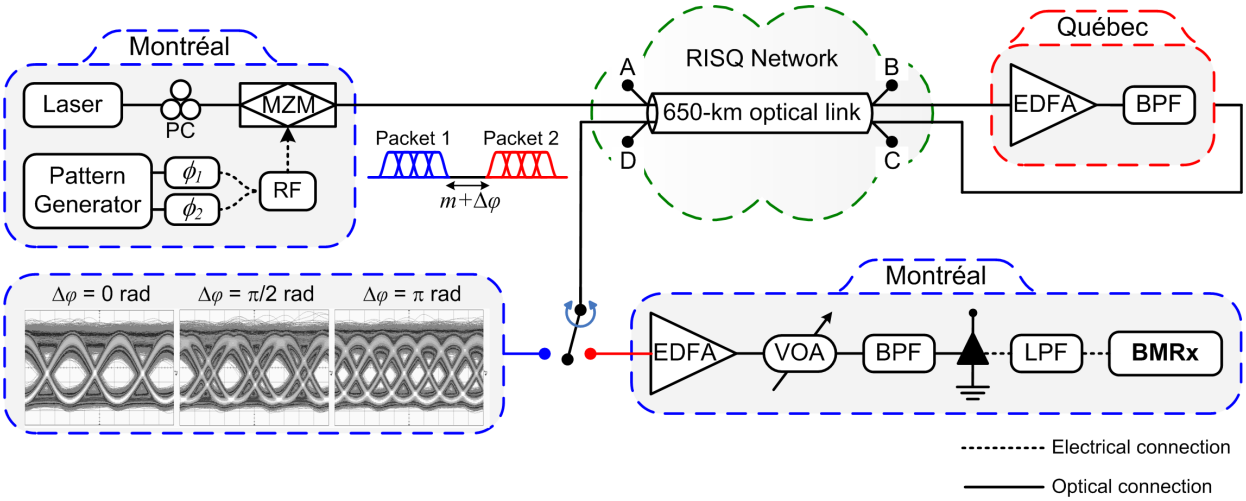


Fig. 6.21 Experimental setup for burst-mode reception in the 1300-km deployed fiber link. Details of the packet structure, optical link and BM-CDR are depicted in Figs. 6.22, 6.24, and 3.6, respectively (BPF: band-pass filter; EDFA: erbium-doped fiber amplifier; LPF: low-pass filter; MZM: Mach-Zender modulator; PC: polarizer controller; RF: radio frequency power combiner; VOA: variable optical attenuator).

sequence of m CIDs can be inserted between the packets. The phase steps between the consecutive packets can be set anywhere between ± 1 ns on a 1-ps resolution, corresponding to a ± 1.25 UI at 1.25 Gb/s.

The bursty data is then sent over the RISQ network on a deployed link consisting of 650 km of SSMF (G.652) from Montreal to Quebec City. Details of the RISQ network will be outlined next. At Quebec City, the signal is amplified by an erbium-doped fiber amplifier (EDFA) and band-pass filtered (BPF), before being looped back. In Montreal, the signal undergoes amplification by an EDFA before a variable optical attenuator (VOA) serves to control the received power level. The signal is then filtered before the optical-to electrical conversion is performed by a PIN photodiode from New Focus (Model #1434). The bursty signal is then low-pass filtered (LPF) before being sent to the BM-CDR. The LPF is a fourth-order Bessel-Thomson filter whose -3-dB cutoff frequency is 0.75 $\times$ bit rate, or 875 MHz, to remove the out-of-band high-frequency electrical noise. Such a filter has an optimum bandwidth to filter out noise while keeping intersymbol interference (ISI) to a minimum [22].

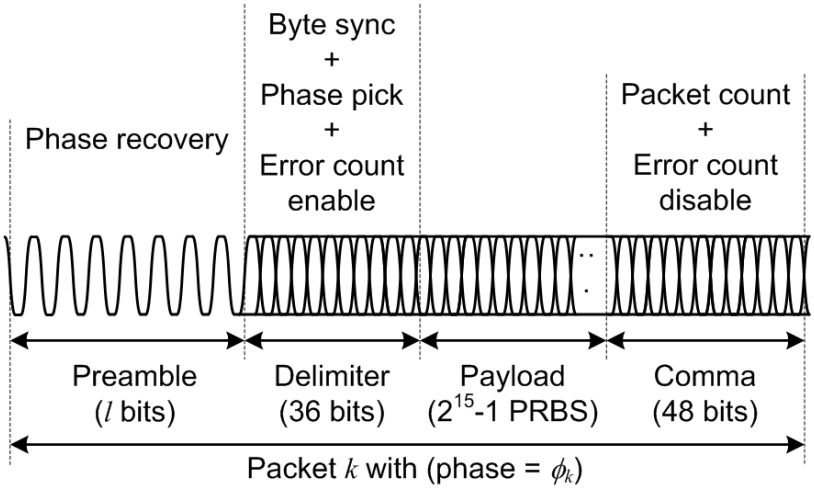


Fig. 6.22 Packet structure for the experiment.

6.5.3 RISQ Network

RISQ refers both to the network and the organization that manages the high speed optical access network that supports research and higher education institutions throughout Quebec with sophisticated telecommunications services. The RISQ network is the Quebec portal for the Canada-wide network (CA*Net) of CANARIE[2], a Canadian government-supported non-profit corporation, which maintains a set of leased wide area network links and also develops and deploys advanced network applications and technologies, for education and high-speed data transfer purposes.

Before conducting the experiments on the deployed link, we first performed prototype experiments in the lab to characterize the link, that is, study the effect of channel impairments with burst-mode reception. Fig. 6.23 shows a photograph of the fiber link built in the lab. Moving forward, Fig. 6.24 illustrates a block diagram of the 1300-km deployed link over the RISQ network from Montreal to Quebec City and back. We used an unoccupied wavelength on the wavelength division multiplexed RISQ network to measure the effect of real-world channel impairments on our BM-CDR at 1.25 Gb/s. There are ten amplification stages featuring both EDFAs and dispersion compensation modules on the 650-km fiber link from Montreal to Quebec City. Considering the extra amplifier at the loop back point, this implies a total of twenty one amplifications stages on the 1300-km deployed link.

[2]Canada's Advanced Research and Innovation Network, `http://www.canarie.ca/`

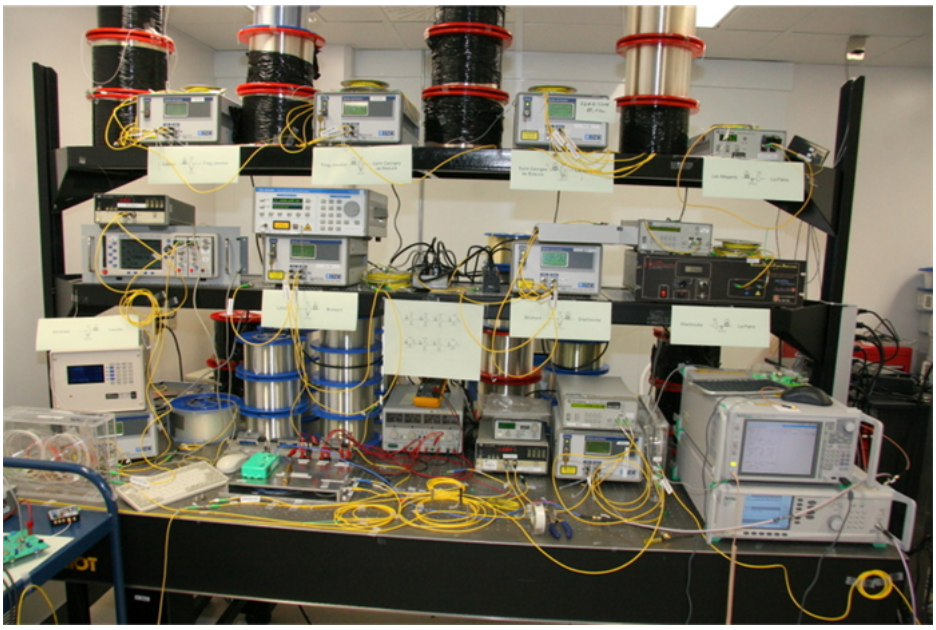


Fig. 6.23 Photograph of the 1300-km fiber link constructed in the lab for prototype experiments to characterize the link.

We measured the residual chromatic dispersion of the link using the phase-shift method (f_{mod} = 100 MHz, Anritsu model 8509BR). The group delay measurement, shown in Fig. 6.25, is performed with 16 averages and fitted to the standard linear polynomial. We consider only the first order dispersion because we realize our experiments at a bit rate which is less than 10 Gb/s and over a narrow waveband (0.2 nm). The residual chromatic dispersion thus obtained is 2533.25 ps/nm over the channel bandwidth. This residual dispersion is not expected to have any significant impact on 1.25 Gb/s transmission. Fig. 6.26 shows the eye diagrams of the launched data (0 km), received data (1300 km) before the photodiode, and the recovered clock and data by the receiver.

6.5.4 Experimental Results

Fig. 6.27 shows the PLR performance of the 1300-km fiber link as a function of phase difference $\Delta\varphi$, between consecutive packets for different preamble lengths with only the CDR (CPA turned OFF). The received signal power is kept at -18 dBm. We consider that all packets are correctly received when PLR $< 10^{-6}$, corresponding to a BER $< 10^{-10}$. We have restricted the horizontal axis to values from $0 \leq \Delta\varphi \leq 800$ ps, corresponding

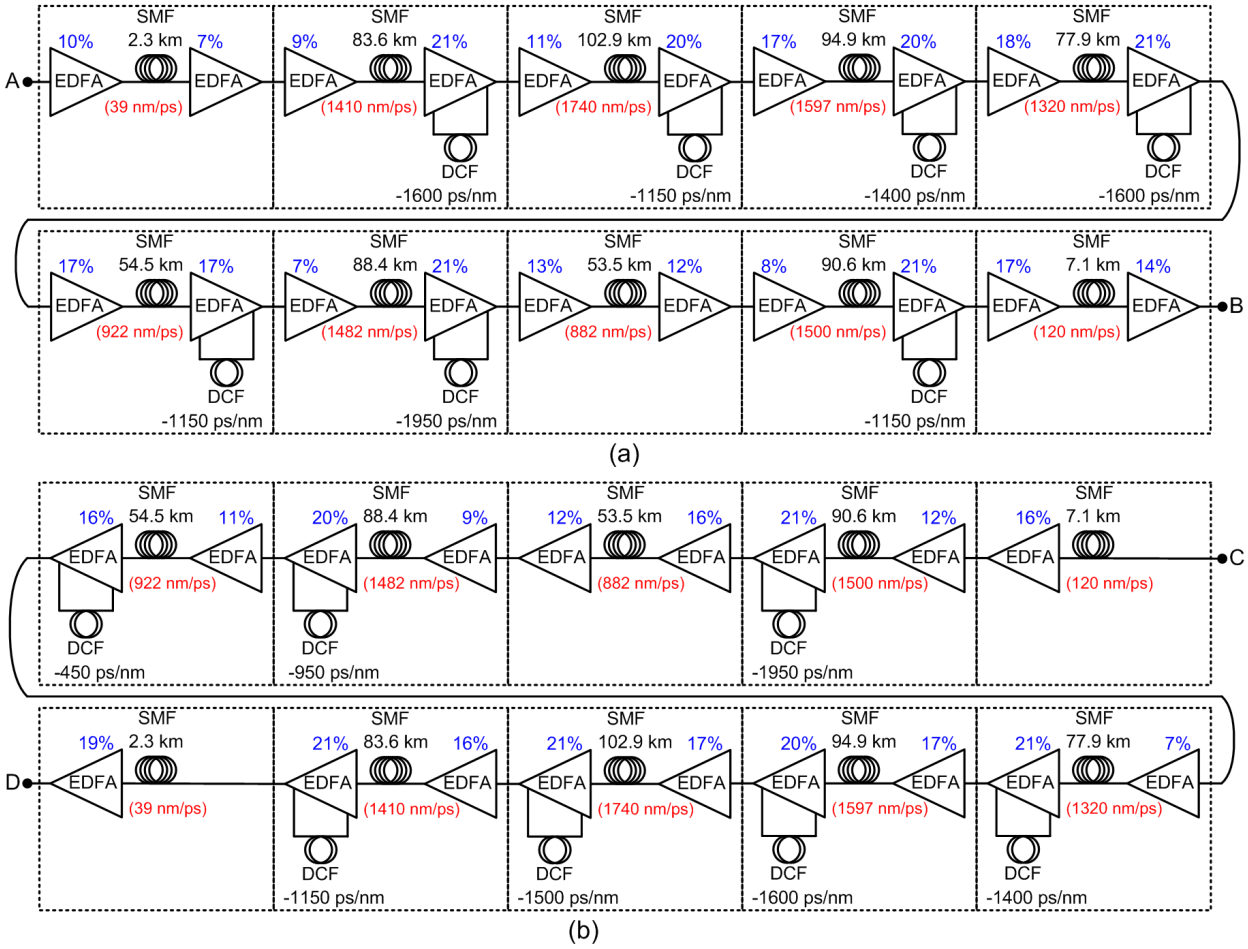


Fig. 6.24 Block diagram of the 1300-km link on the RISQ network. (a) Montreal to Quebec City. (b) Quebec City to Montreal (SMF: single-mode fiber; EDFA: erbium-doped fiber amplifier; DCF: dispersion compensation fiber).

to $0 \leq \Delta\varphi \leq 2\pi$ rad at 1.25 Gb/s. Also, note that the results are symmetrical about 0 rad from $-2\pi \leq \Delta\varphi \leq 0$ rad. We observe a bell-shaped curve centered at 400 ps because this represents the half bit period corresponding to the worst-case phase step at $\Delta\varphi = \pi$ rad, and therefore, the CDR is sampling exactly at the edge of the data eye, resulting in a PLR ~ 1. At relatively small phase shifts (near 0 or 2π rad), we can easily achieve zero PLR because the CDR is almost sampling at the middle of each bit. Preamble bits ("1010$\cdots$" pattern) can be inserted at the beginning of the packets to help the CDR settle down and acquire lock. As the preamble length is increased, there is an improvement

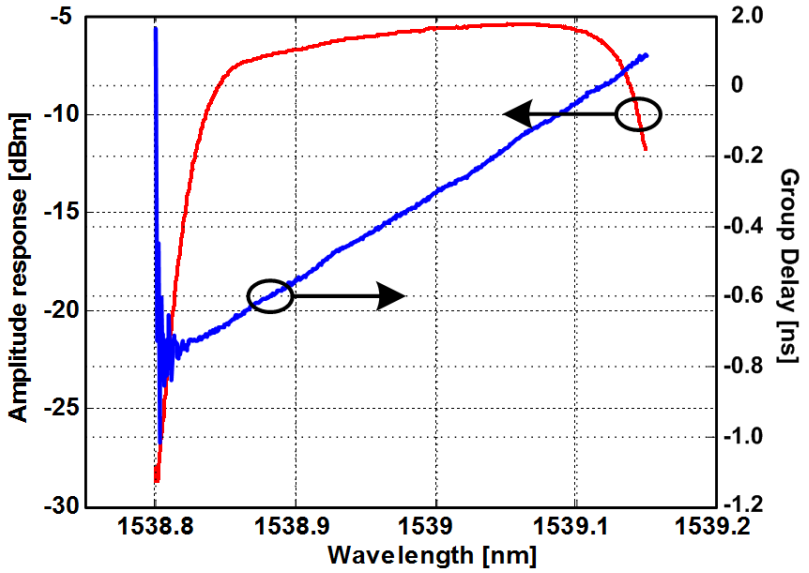


Fig. 6.25 Measured residual dispersion in a loop-back (Montreal-Quebec city) of RISQ link.

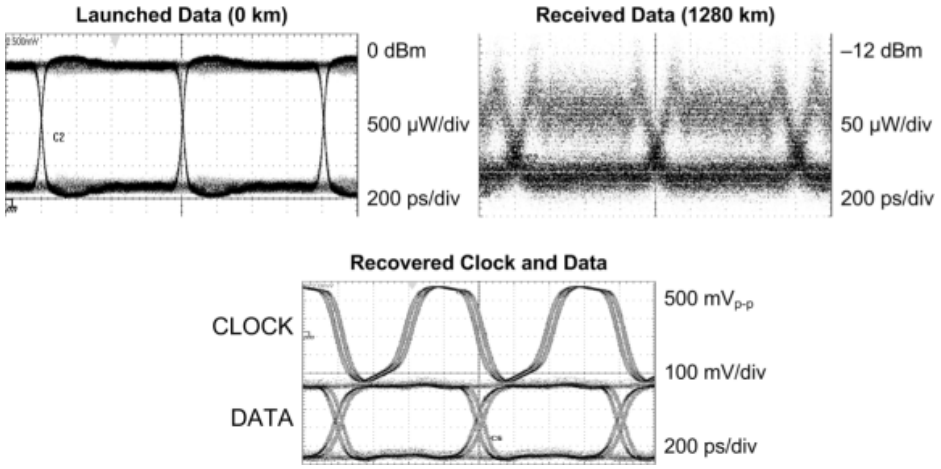
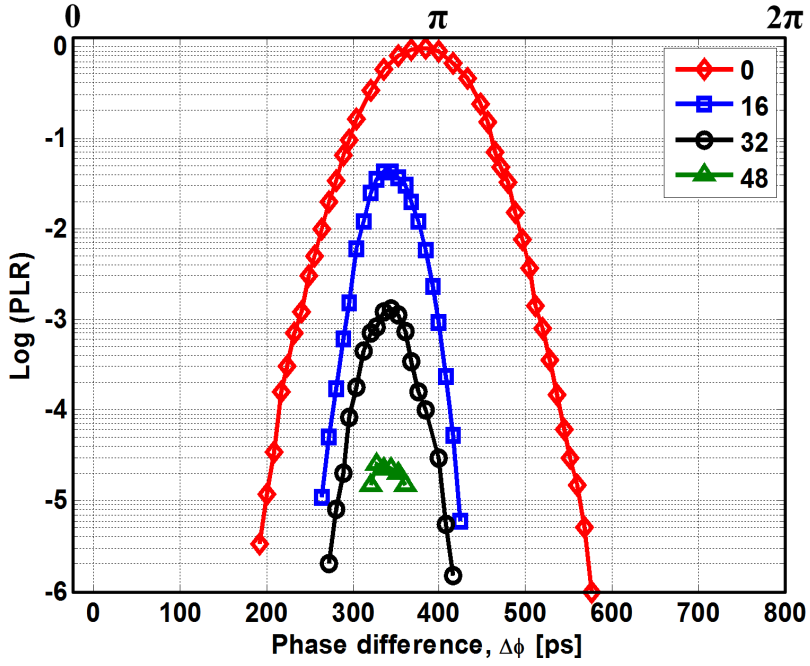
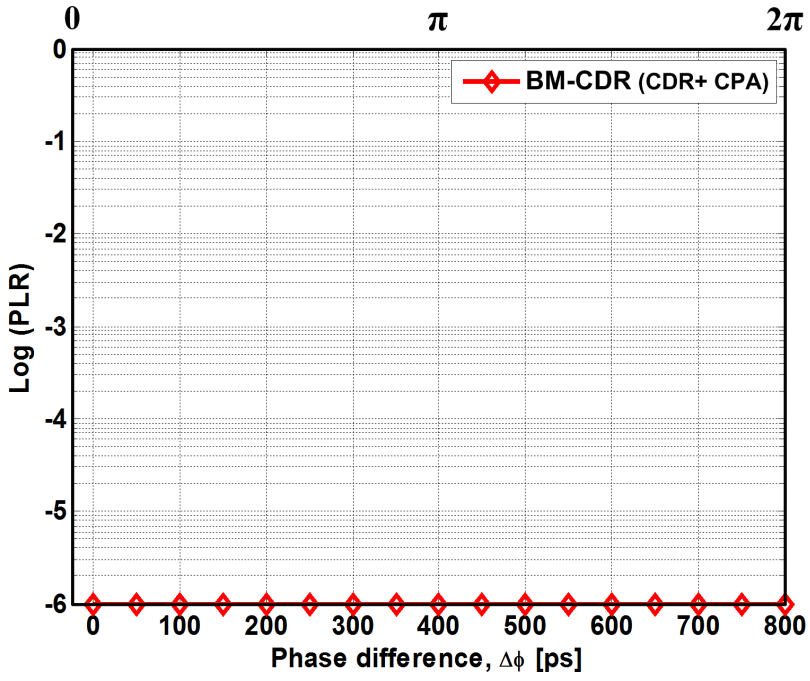


Fig. 6.26 Eye diagrams of the launched data (0 km), received data (1300 km), and the recovered clock and data by the receiver.



(a)

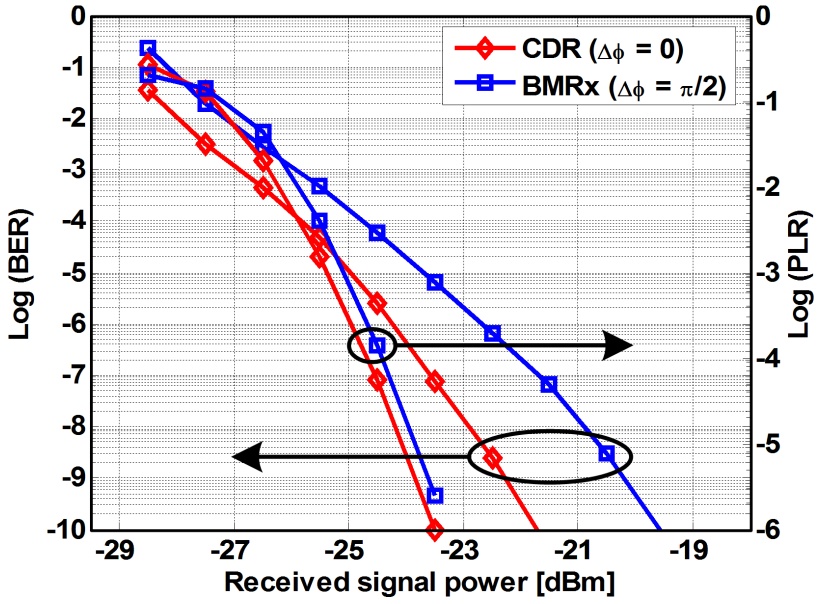


(b)

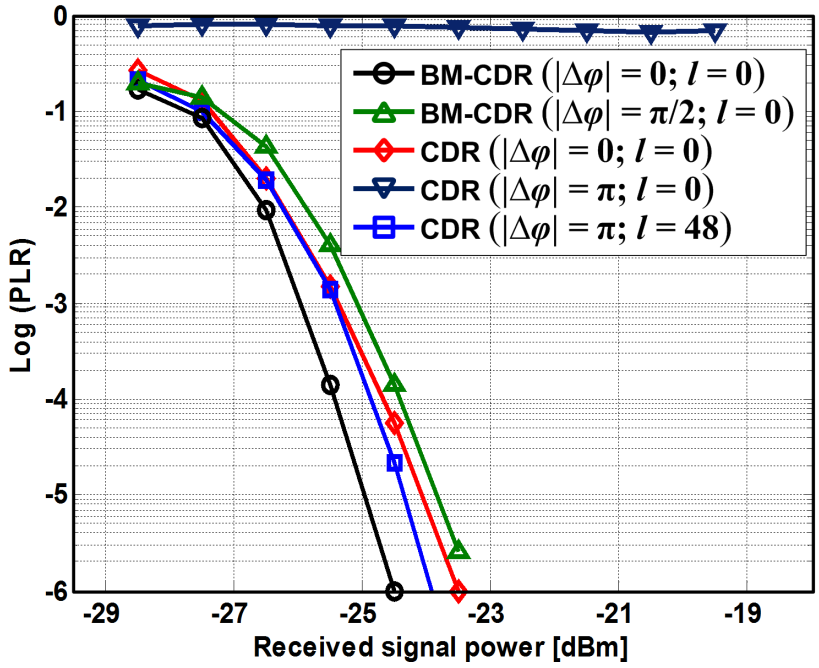
Fig. 6.27 PLR versus phase difference between consecutive packets. (a) CDR performance with different preamble lengths. (b) BM-CDR performance with no preamble bits.

in the PLR. At least 49 preamble bits are required for error-free operation for any phase step. However, the use of the preamble reduces the effective throughput and increases delay. By switching ON the burst-mode functionality of the receiver with the CPA as shown in Fig. 6.27(b), we observe error-free operation for any phase step with *no* preamble bits, allowing for instantaneous phase acquisition. It should be noted that whereas $\Delta\varphi = \pi$ rad represents the worst-case phase step for the CDR sampling at the bit rate, $\Delta\varphi = \pi/2$ rad phase step is the worst-case scenario for the BM-CDR as it is based on an oversampling CDR at $2\times$ the bit rate.

We note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [26]. However, by reducing the phase acquisition time as demonstrated in this work, the burst-mode sensitivity penalty can be reduced. Alternatively, with the reduced number of preamble bits, more bits can be left for the payload, thereby increasing the information rate. To further illustrate this, consider the experimental results in Fig. 6.28 which shows the BER and PLR performance of the receiver as a function of the received signal power for different phase steps and preamble lengths. Note that the abscissa is the received signal power, that is, the optical power contributed at the photodiode. To determine the burst-mode penalty of the receiver, the performance of the CDR sampling continuous data ($\Delta\varphi = 0$ rad) at the bit rate is compared to the performance of the BM-CDR sampling bursty data with a worst-case phase step ($\Delta\varphi = \pi/2$ rad) as shown in Fig. 6.28(a). Both measurements are made for a 0-bit preamble. Due to the $2\times$ oversampling (faster electronics) and the phase picking algorithm, we observe a 2-dB and a 0.5-dB power penalty for the BER and PLR performance, respectively. It can also be observed that for the worst-case phase step in the link, the BMRx accomplishes sensitivities of -23 dBm and -19.5 dBm, to achieve BER $= 10^{-10}$ and PLR $= 10^{-6}$, respectively. Note that when the BM-CDR samples continuous data, we actually notice a 1-dB improvement in the PLR performance over the CDR due to the CPA as depicted in Fig. 6.28(b). The CDR will not be able to recover any packets if there exists a worst-case phase step ($\Delta\varphi = \pi$ rad) between the consecutive packets, regardless of the received signal power, resulting in a PLR ~ 1. However, if a 48-bit preamble is complied with, the PLR performance of the CDR is then comparable to the PLR performance obtained by the CDR with zero preamble bits and no phase steps. Hence, for the worst-case phase steps in the link, there is a tradeoff between the sensitivity penalty obtained by employing the BM-CDR over the CDR and the number of pream-



(a)



(b)

Fig. 6.28 BER and PLR versus received signal power for different preamble lengths and phase steps between consecutive packets.

ble bits required without the BM-CDR. Since random silence periods in a live link are inevitable, the power penalty may be a small price to achieve error-free operation.

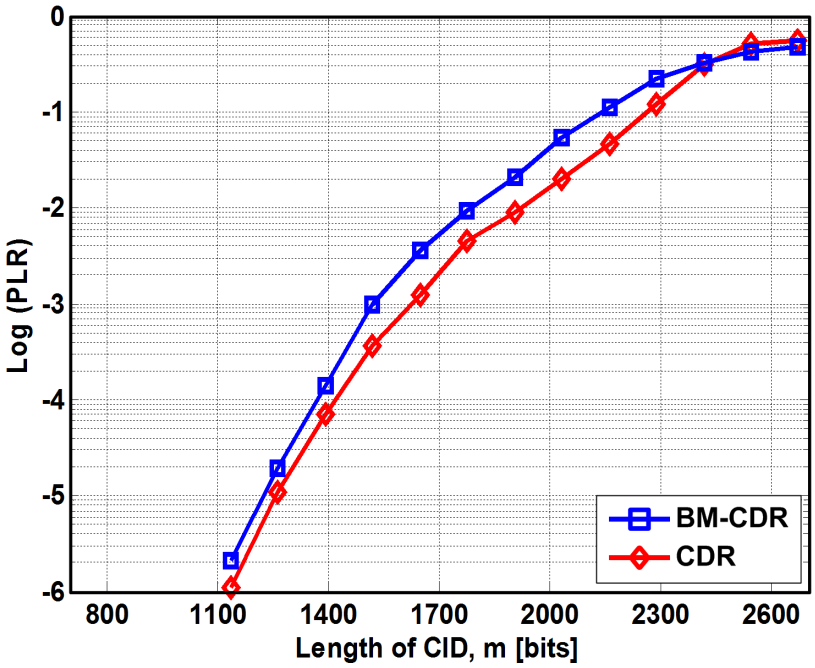


Fig. 6.29 PLR versus CID immunity of BM-CDR and CDR.

We measure the CID immunity of the receiver by zeroing bits at the end of packet 1 until error-free operation can no longer be maintained on packet 2. The immunity of the BM-CDR and the CDR to CIDs is depicted in Fig. 6.29. The received signal power is kept at -18 dBm, with the phase step and the preamble length both set to zero for this measurement. As shown, both the BM-CDR and the CDR can support ∼1100 CIDs with error-free operation. This CID immunity is significantly greater than current state of the art BM-CDR—32 bits [50], and 7 bits in [51]. It should be noted that in addition to CIDs, if a worst-case phase step is introduced between consecutive packets, the CDR regardless of its CID immunity will result in a PLR $\sim$ 1. This is not the case with the BM-CDR, which as demonstrated, is immune to any phase steps between consecutive packets.

Finally, to measure the dynamic range of the receiver, recall that we fix the amplitude of packet 1 and increase until the BM-CDRs can no longer maintain error-free operation on packet 2. Again, the phase step and the preamble length are both set to zero for this measurement. The worst-case scenario is when a low amplitude packet follows a high

amplitude packet [33]. The dynamic range of the receiver is measured to be 3 dB. This relaxes the requirements of the output voltage swings/fluctuations from a front-end at high data rates. The dynamic range can easily be increased to more than 15 dB with a front-end consisting of a burst-mode amplitude recovery circuit [31].

Using (4.40), we theoretically predict the PLR performance, of the RISQ network as a function of the received signal power, with a pattern correlator having an error-resistance of $z = 0$ bits, and compare the results experimentally in Fig. 6.30. The theoretical and experimental results concur.

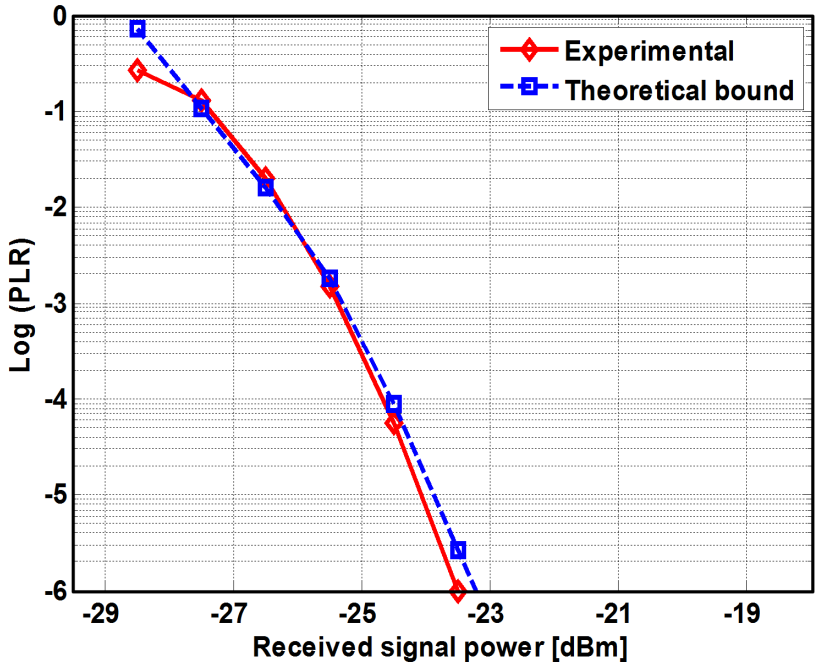


Fig. 6.30 Comparison of the theoretical and measured PLR performances versus signal power.

6.5.5 Conclusion

We experimentally investigated the effect of real-world channel impairments on the performance of the BM-CDR based on time domain semiblind oversampling, at 1.25 Gb/s in a 1300-km fiber link that spans from Montreal to Quebec City and back. We quantified the results in terms of the BER and PLR performance of the system.

In summary, the BM-CDR receiver achieves a PLR $< 10^{-6}$ and PLR $< 10^{-10}$ while featuring instantaneous (0 preamble bit) phase acquisition for any phase step ($\pm 2\pi$ rad)

between packets, a sensitivity of −19 dBm, a CID immunity of 1100 bits, and a 3-dB dynamic range. The price to pay is faster electronics and a burst-mode penalty of 2-dB and 0.5-dB in the BER and PLR performance, respectively. On the other hand, the 1.25 Gb/s BM-CDR inherits the low jitter transfer bandwidth (2 MHz) and the low jitter peaking (0.1 dB) of the oversampling CDR at 2.5 Gb/s. Hence, this BM-CDR could also find applications in future OPSN, which may require a cascade of BMRx that each consumes some of the overall jitter budget of the system.

Author's Contribution

The author of this thesis: (1) designed and implemented the BM-CDR employed for this study; (2) built the Montreal side of the experimental setup; and (3) carried out all the experiments, analyzed the results, and characterized the BM-CDR.

Acknowledgment

This work was a collaborative effort with Prof. Leslie A. Rusch and Prof. Sophie LaRochelle at the Center of Optic, Photonic, and Laser (COPL), Laval University. The author would like to acknowledge the following individuals for their respective contributions. Ms. Yousra Ben M'Sallem, Ph.D. candidate, characterized the deployed fiber link, built the Quebec side of the experimental setup, and participated in all the experiments. Mr. Nicholas Zicha and Ms. Ming Zeng, M.Eng. students, provided technical assistance during the lab prototype experiments. Mr. Serge Doucet, Research Associate, built the the lab prototype test bed to characterize the link. Mr. Charles Allaire, Senior Network Administrator, provided timely support on the 1300-km link on the RISQ network.

6.6 622 Mb/s SAC-OCDMA PON 20-km Uplink Experiments

We experimentally investigate burst-mode reception at 622 Mb/s in a 7-user 20-km incoherent spectral amplitude-coded optical code-division multiple access PON uplink. We consider two network architectures, namely, local sources and centralized local sources, and study their relative merits in a two-feeder topology. The receiver employed in this study is variant of the BM-CDR based on semiblind time domain oversampling (see Section 3.3) with a Reed-Solomon RS(255,239) forward-error correction decoder. The work presented in this section is a result of the research published in [27, 52–54].

6.6.1 Introduction

An alternative to TDM PONs and WDM PONs presented in Sections 6.3 and 6.4, respectively, is the use of optical code-division multiple-access (OCDMA) to upgrade existing PONs. OCDMA is receiving considerable attention because it combines the large bandwidth of the fiber medium with the flexibility of the CDMA technique to achieve high-speed connectivity [55]. As there are no standards or commercial systems for OCDMA networks, the question of the best implementation, and indeed the suitability of OCDMA for PONs remains open.

In this section we focus on incoherent spectral amplitude-coded optical code-division multiple-access (SAC-OCDMA) as a solution for PONs, because of its ability to cancel multiple access interference (MAI), and to permit the use of low speed electronics operating at the bit rate [56,57]. Furthermore, advances in writing fiber Bragg gratings (FBGs) make possible the design of low cost and compact passive encoders/decoders well adapted to PONs [56, 58]. In our work we examine several PON physical architectures, namely, the use of local sources at each ONU versus the use of a single light source housed at the central office. An inexpensive incoherent light source is placed either at each ONU or at the OLT, for the local sources (LS) architecture or the centralized light sources (CLS) architecture, respectively. In order to manage uplink (from users to OLT) and downlink (from OLT to users) traffic, we consider both two-feeder and single-feeder approaches [59]. Much research into OCDMA focuses on optical design, while assuming the availability of high-speed electronics [55,56,60,61]. Emerging research is concerned with the electronic design of receivers for optical multi-access networks, featuring post-processing functionalities [4, 50]. Previous electronic receivers were reported in the literature for fast-frequency hop (FFH)

OCDMA and PON systems [33, 62]. FFH-OCDMA (or λ-t OCDMA) requires electronics that operate at the chip rate rather than the data rate. SAC-OCDMA has the advantage of operating at the data rate, and enjoys excellent MAI rejection with balanced detection.

In this section we demonstrate experimentally burst-mode reception of an incoherent SAC-OCDMA PON uplink supporting seven asynchronous users at 622 Mb/s (FFH results were at 155 Mb/s data rate). Our receiver—BM-CDR based on time semiblind oversampling—has no global clock (i.e., synchronization), instead exploiting a commercial synchronous optical network (SONET) CDR. Reed Solomon RS(255,239) forward-error correction (FEC) is also implemented on a FPGA. The receiver features CPA and includes a custom BERT implemented on the FPGA.

The LS and CLS SAC-OCDMA PON architectures are tested experimentally, and BER and PLR are measured. The immunity of the CDR in terms of CID is also measured. We simulate the BER with FEC in order to validate our measurements. We quantify the increase in soft capacity via FEC, while working with a nonideal recovered clock that provides realistic, achievable sampling.

6.6.2 SAC-OCDMA PON Architectures

Tree architectures are widely used for FTTH, or the so called "last mile" market. Such networks referred to as PONs employ only passive components (couplers, circulators, etc.) in the optical distribution network (ODN) and at the remote node (RN), and they have low installation and management costs. Different PON architectures have been proposed by different research groups [16, 36, 38, 59, 63–66], including both two-feeder and single-feeder architectures to multiplex uplink and downlink traffic. In two-feeder architectures, uplink and downlink traffic are sent independently on separate feeders; a single-feeder architecture carries both uplink and downlink on one fiber. Although single-feeder topologies reduce infrastructure and maintenance costs, they suffer from Rayleigh back-scattering if the same wavelength is used for upstream and downstream. Two-feeder architectures give the flexibility to use the same wavelength band for upstream and downstream, making the design easier. Although our OCDMA PON architectures offer the flexibility of adopting both two-feeder and single-feeder architectures, we test only the two-feeder architecture for experimental convenience. The effects of Rayleigh back-scattering, which are reduced in such architectures, are then not addressed.

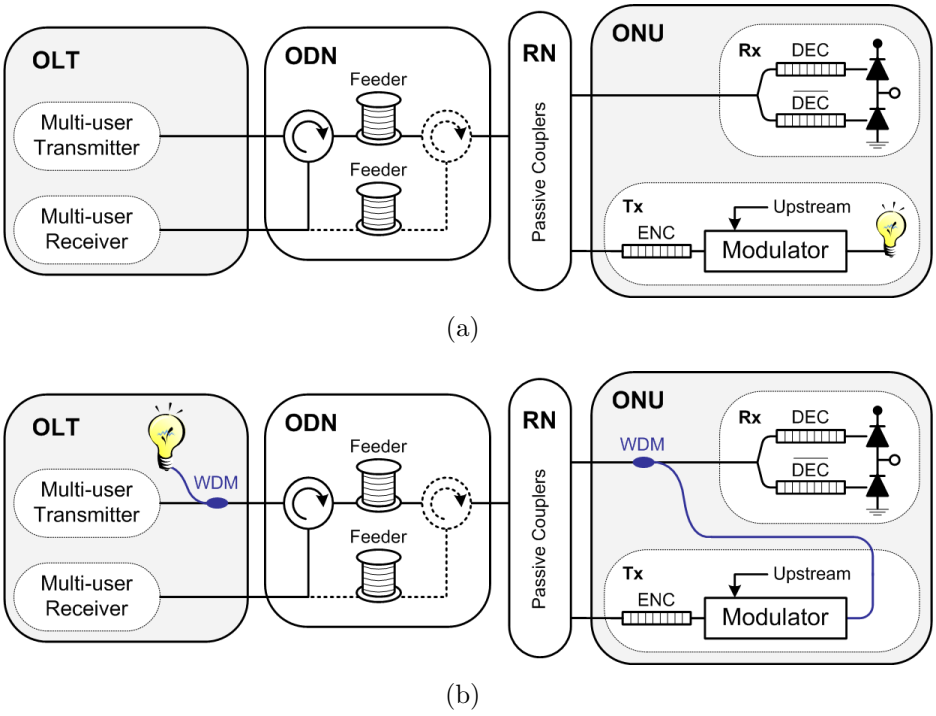


Fig. 6.31 SAC-OCDMA PON physical architecture depicting the: (a) LS architecture; and (b) CLS architecture.

In [27,53] we propose four different architectures for SAC-OCDMA PONs as illustrated in Fig. 6.31; both LS architectures (Fig. 6.31(a)); and CLS architectures (Fig. 6.31(b)) can exist with two-feeder and single-feeder topologies (shown within the ODN). We analyze both architectures with each feeder topology in terms of power budget, but we experimentally test only the two-feeder topology. Although our architectures provide full-duplex communications, we focus on the design of the ONU side, as it is one of the most challenging factors in PON design [14–16, 33]. More specifically, we focus on the design of the ONU transmitter (uplink transmitter). The optimum receiver for a SAC-OCDMA PON at both the OLT and ONU is the conventional balanced receiver because of its ability to suppress first order MAI. The structure of such a receiver for the ONU is given in Fig. 6.31, including a 1×2 coupler, a decoder (DEC), a complementary decoder ($\overline{\text{DEC}}$), and a balanced photodiode (PD). Fiber Bragg gratings working in transmission are used as the encoders/decoders because of their good group delay performance, which is vital in SAC-based OCDMA systems [56]. Fig. 6.31(a) shows the proposed LS SAC-OCDMA PON; in that case an inexpensive directly modulated light emitting diode (LED) or a

broadband erbium-based source is externally modulated and located at each ONU. On the other hand, the proposed CLS SAC-OCDMA PON, shown in Fig. 6.31(b), places a single powerful source at the OLT with remote external modulation of that source at each ONU. In CLS architecture coarse WDM filters are needed at the OLT and ONU, as shown in Fig. 6.31(b), to separate the continuous wave light for the uplink from the modulated downlink. Such filters can be replaced by passive couplers if the same wavelength band is used for both downlink and uplink. The RN, the ODN, and the OLT multi-user transmitter/receiver are similar for the two architectures. The RN consists of passive combiners and splitters, as in existing TDM PONs, so there is no need to upgrade the PON infrastructure; for WDM PONs the couplers must be replaced by arrayed waveguide gratings (AWGs). The RN serves as a connection between the ONUs and the ODN. Users are connected to the RN through short length fibers ($\sim$1 km) called distribution drop fibers. The ODN, composed of feeder fibers ($\sim$20 km) and passive optical circulators, can adopt a two-feeder (the second feeder with its corresponding circulator shown in dotted in Fig. 6.31) or a single-feeder architecture. At the OLT a multi-user transceiver is used to communicate with all the users in both directions. The OLT should contain optical amplifiers to compensate for the losses through the network and also for the combining and splitting losses of the multi-user transmitter and receiver when implemented all optically (same design as ONUs in Fig. 6.31). Note that electronic implementation of OLT transceivers could help reduce the loss budget significantly by eliminating the optical couplers. Furthermore, all pre-processing and post-processing functionalities could be easily handled in electronics.

The uplink power budget of the proposed PON architectures in Fig. 6.31 is mainly affected by the RN and the ODN adopted. In LS architectures (see Fig. 6.31(a)), the uplink signal travels only in one direction, from the ONU to the OLT. For N ONUs (corresponding to a $1 : N$ splitting ratio) we have $10\log(N)$ dB splitting losses, in addition to the propagation losses through one feeder and the insertion losses of a 3-port circulator. These observations are valid for both the two-feeder or the single-feeder topology. In the CLS architecture, shown in Fig. 6.31(b), for uplink the unmodulated source travels from the OLT to the ONU and after modulation returns to the OLT. Therefore, a CLS PON experiences twice the ODN and RN losses (splitting losses + propagation losses + insertion losses) as a similar LS PON, again whether the two-feeder or the single-feeder topology is used.

6.6.3 Experimental Setup

According to the PON standards, a continuous downlink in the wavelength band of 1480-1500 nm carries TDM data, or OCDMA encoded data in our case, from the OLT towards multiple ONUs. A burst-mode link in the 1310 nm window collects all ONUs upstream traffic toward the OLT as variable-length packets at the same rate. Because of the bursty nature of the upstream, the OLT receives packets from active ONUs with different amplitude levels and phases. In Class B PONs, the average signal level may vary 21 dB in the worst case from packet to packet [33]. These packets are of variable length and are interleaved with a guard time of only 4 bytes as specified by the physical medium dependent (PMD) layer [19, 33].

A typical burst-mode uplink signal that complies with PON standards is used as a test signal in our experiments and is shown in Fig. 6.32. Packet 1 serves as a dummy packet to force the burst-mode CDR to lock to a certain phase before the arrival of packet 2. A silence period including m CIDs and a phase step $\Delta\varphi$ is inserted between the two packets. This idle period also represents the asynchronous nature of OCDMA due to the random phase step $-2\pi \leq \Delta\varphi \leq 2\pi$ rad between the two packets. The PLR measurements and their corresponding BER measurements are performed only on packet 2, which consists of n preamble bits, 20 delimiter bits, $2^{15}-1$ payload bits, and 48 comma bits. The preamble and the delimiter bits correspond to the physical layer upstream burst-mode overhead at 622 Mb/s, as specified by the ITU-T G.984.2 standard [19]. The preamble bits are used to perform phase recovery. The delimiter is a unique pattern indicating the start of the packet to perform byte synchronization. Similarly, the comma is a unique pattern to indicate the end of the payload. The payload is simply a $2^{15}-1$ PRBS. The BER and PLR are measured for the payload bits only. The lock acquisition time corresponds to the number of bits (n) in front of the delimiter in order to get a zero PLR for over three minutes at 622 Mb/s ($> 10^6$ packets received, that is, PLR $< 10^{-6}$), a BER $< 10^{-10}$, and for any phase step ($\Delta\varphi \leq 2\pi$ rad) between consecutive packets. We will demonstrate that even at $n = 0$, that is, no preamble bits, our phase picker gives excellent results. To generate alternating packets with adjustable phase, as in Fig. 6.32, we combined two programmable ports from the HP80000 pattern generator using a radio frequency (RF) power combiner. The phase steps between the consecutive packets can be set anywhere between ± 2 ns on a 2-ps resolution, corresponding to a ± 1.25 unit interval (UI) at 622 Mb/s. Note that 1 UI

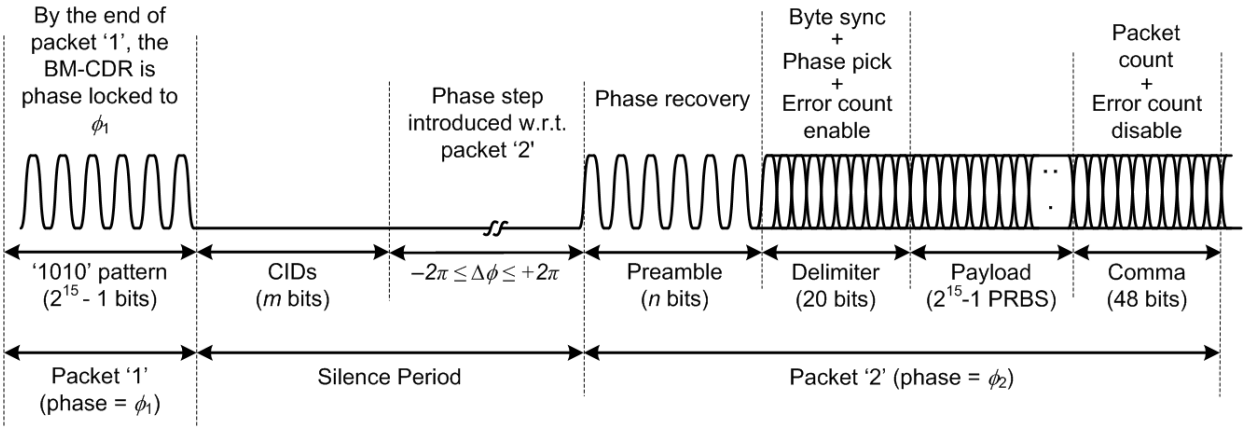


Fig. 6.32 Typical burst-mode uplink test signal used to test the phase acquisition time of the clock phase aligner.

corresponds to 1-bit period.

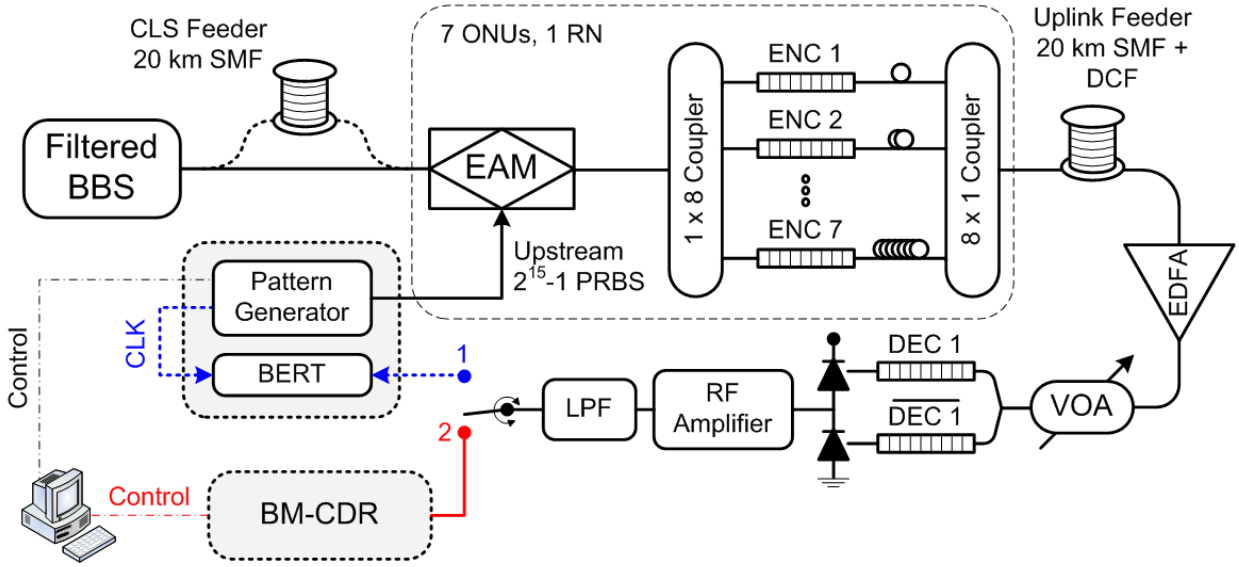


Fig. 6.33 Experimental setup for a 7 × 622 Mb/s SAC-OCDMA PON uplink (BERT: BER tester; CLK: clock, DEC: decoder; and ENC: encoder).

The experimental setup illustrated in Fig 6.33 is used to test the uplink of the LS and CLS SAC-OCDMA PON architectures shown in Fig 6.31. Fig. 6.34 shows a photograph of the experimental setup built in the lab. A single incoherent broadband source (BBS) is filtered around 1542.5 nm using two cascaded FBG band-pass filters providing a 9.6 nm band, and serves to test both the CLS and LS architectures. An non-return to zero (NRZ)

Fig. 6.34 Photograph of the 20-km SAC-OCDMA PON uplink experimental setup to test the BM-CDR in LS and CLS architectures.

$2^{15} - 1$ PRBS is input to a single polarization independent electro-absorption modulator (EAM) that, in conjunction with appropriate decorrelating delay lines, represents independent data streams each modulated externally at a distinct ONU. For the CLS architecture, the single powerful BBS is sent over the 20 km CLS/downlink feeder and is then split by the first 1×8 coupler representing the RN. For the LS architecture, the 20 km single mode fiber (SMF-28) is not present and the first 1×8 coupler is not part of the network, but rather an experimental trick to emulate eight separate, low power incoherent sources. The balance of the setup is interpreted as seven ONUs each with a distinct CDMA encoder, followed by the second 1×8 coupler representing the RN and a 20 km SMF for the uplink in the two-feeder architecture. We did not use the circulators and the WDM filter in Fig 6.31, as we were only testing the uplink; these components would only contribute to insertion losses.

At the OLT an appropriate dispersion compensation fiber (DCF) is used, and the signal is amplified by an erbium-doped fiber amplifier (EDFA) and detected in a balanced receiver. A variable optical attenuator (VOA) serves to control the received power level. A balanced detection scheme similar to that in Fig 6.31 is then used to decode user 1. To ensure good detection and MAI cancellation, the optical lengths of the two branches of the receiver are perfectly adjusted; furthermore, the power at both arms due to MAI is controlled using another VOA (not shown in Fig 6.33) that accounts also for the splitting ratio of the 1×2 coupler as in [56]. After decoding, each arm goes into one of the two separate inputs of an 800 MHz balanced photodiode from New Focus (model 1617). The electrical signal is then amplified (MITEQ, 0.01–500 MHz) and low-pass filtered by a fourth-order Bessel-Thomson filter (Picosecond, 467 MHz) to remove the out-of-band high-frequency electrical noise. Such a filter reduces intensity noise from the incoherent broadband source [56], while keeping inter-symbol interference to a minimum. Measurements are then performed with either a global clock, or through our OCDMA burst-mode receiver, corresponding to switch position 1 or 2, respectively. The desired information rate per user is 622 Mb/s; an RS(255,239) code introducing 15/14 overhead leads to an aggregate bit rate of 666.43 Mb/s. The spectral coding is achieved by FBGs working in transmission; balanced incomplete block design (BIBD) codes with length 7 and weight 3 are used as in [56].

6.6.4 Experimental Results

In this section we present the system performance in terms of BER, PLR and the CID immunity for the back-to-back configuration (without fiber link), and the LS and the CLS SAC-OCDMA PON architectures. The experimental results are presented in Figs. 6.35–6.42, except for Fig. 6.39 which shows simulation versus measurement results. We present also the power and link budget for the different architectures that were tested. BER measurements are reported for continuous upstream traffic, while PLR is reported for packet data, based on the burst-mode BERT results. PLR measurements use bursty traffic (similar to that in Fig. 6.32) with packets of $2^{15} - 1$ bits length and zero preamble length; use of a preamble would improve PLR, but at the cost of reduced throughput. PON standards provide for a certain preamble length to allow the receiver enough time to recover the clock, adjust the phase, and control the gain. The operation of the CDR and its ability to provide a clock signal with a $2\times$ oversampling which is used by the phase picking algorithm,

is explained in Section 3.3.

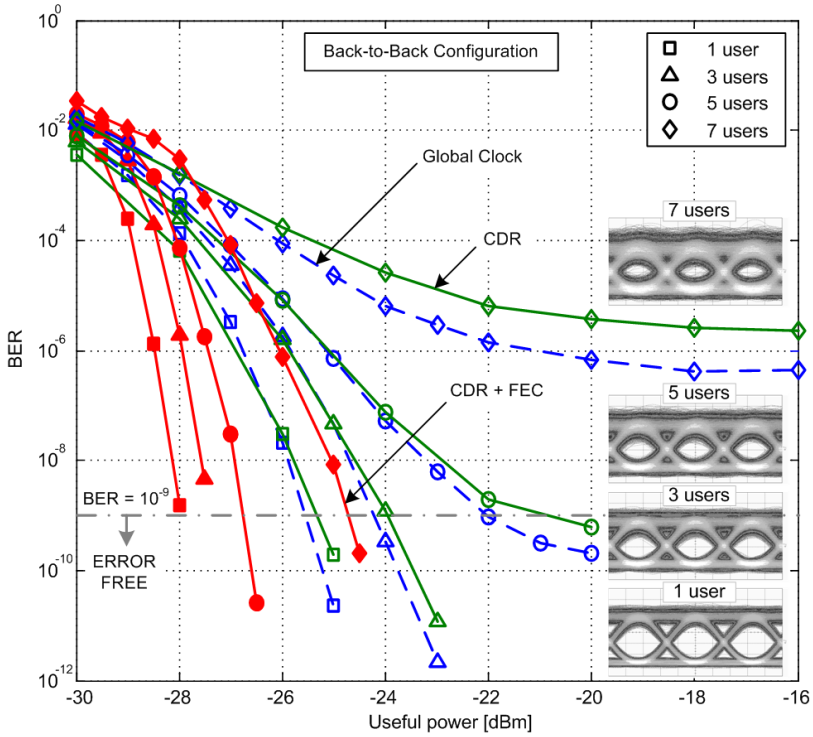


Fig. 6.35 BER versus useful power for back-to-back configuration (dashed lines for global clock; solid lines and unfilled markers for CDR; solid lines and filled markers for CDR with FEC).

In Fig. 6.35 we present the BER versus power for the back-to-back configuration. The horizontal axis represents the useful power; that is, the received power from the desired user. Curves are presented for a single user system up to a fully loaded system of seven users. Ignoring for a moment the solid curves with filled markers (FEC results), we focus our attention on the set of curves for the global clock (dashed) and for the CDR module (solid + unfilled markers). Starting from a single user we see a classic waterfall curve; as we go to a fully charged system of seven users BER floors begin to appear, starting from five users. The penalty when using the CDR unit is not significant (less than 0.25 dB), as we can see by the proximity of the CDR and global clock curves. When adding the FEC to the CDR operation, we see that all BER floors disappear and we return to the classic waterfall close to the single user performance. Eye diagrams measured at -18 dBm are included as insets in Fig. 6.35. The single-user eye diagram is very open, while the fully loaded system with seven users has a severely closed eye. Despite the eye closure, the FEC

allows us to return to error free performance.

Similar curves for the LS and CLS PON architectures are presented in Figs. 6.36 and 6.37, respectively. The same trends are observed, except for the case of seven users for the LS PON architecture. In that case, we note a slight improvement in the performance with the CDR compared to the global clock measurement, despite the nonideal sampling of the CDR. This improvement is related to the threshold adjustment, as in [62]. At small power levels we were able to manually control the decision threshold [using a direct current (dc) power supply] to great accuracy for the CDR measurements, while we were limited by the automated decision threshold in the commercial BERT for global clock measurements. The manual optimization explains the slight improvement in the performance when using the recovered clock especially at lower power levels; this explains the crossings of the global clock curves with the CDR curves at around −26 dBm for the three measurement configurations in Figs. 6.35–6.37.

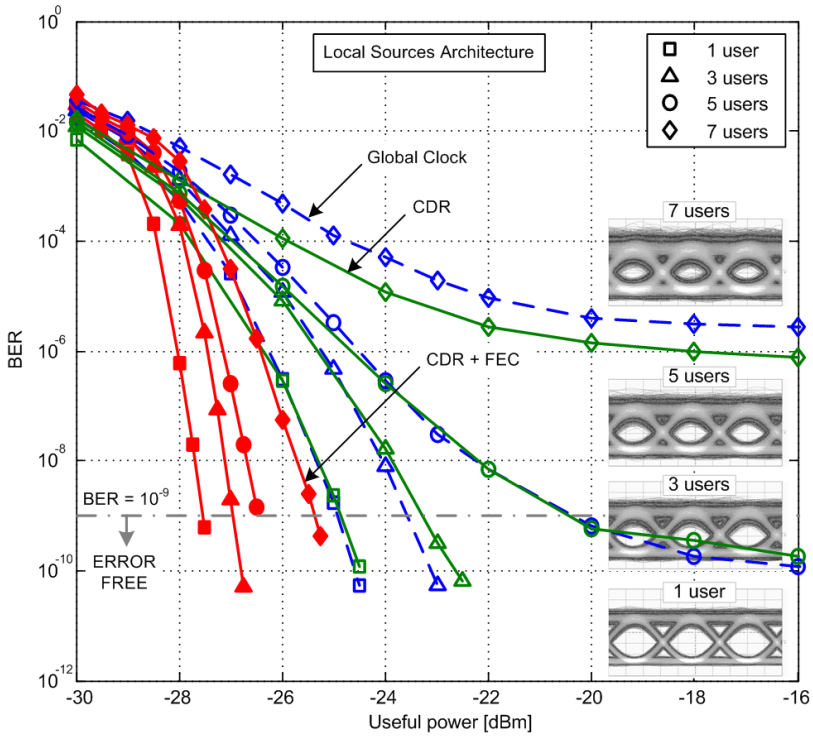


Fig. 6.36 BER versus useful power for LS architecture (dashed lines for global clock; solid lines and unfilled markers for CDR; solid lines and filled markers for CDR with FEC).

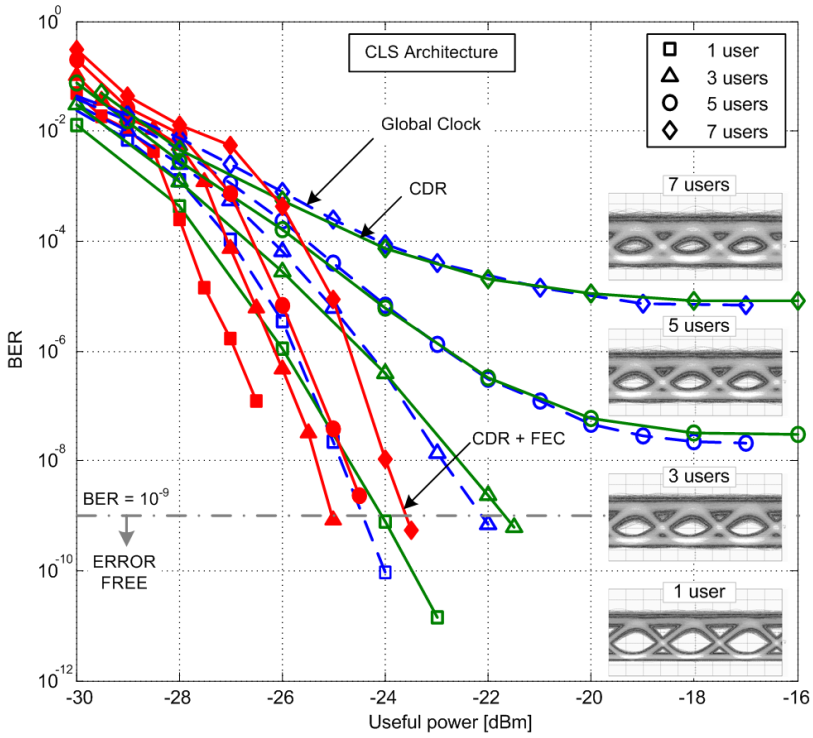


Fig. 6.37 BER versus useful power for CLS architecture (dashed lines for global clock; solid lines and unfilled markers for CDR; solid lines and filled markers for CDR with FEC).

For easier comparison of the back-to-back configuration and the two PON architectures, we plot in Fig. 6.38 the single user and fully loaded (seven users) systems BER curves. We consider the performance using our burst-mode receiver when the FEC module is OFF (curves with unfilled markers), and when it is ON (curves with filled markers). A coding gain of more than 2.5 dB (measured at BER $= 10^{-9}$) is observed for a single user for the three architectures. Furthermore, the penalty from a back-to-back configuration to the LS PON is negligible (less than 0.25 dB), as well as the one from a LS PON to the CLS PON architecture. Results are consistent with the that in [56] for a back-to-back configuration and a 20 km communication link. For the seven users case, we see clearly all BER floors are eliminated by the FEC. Operating at a relatively low power (-23 dBm received power) we obtain error free transmission (BER $\ll 10^{-9}$) for the three architectures. Therefore, we were able to demonstrate for the first time to our knowledge an error free 7×622 Mb/s uplink of an incoherent SAC-OCDMA PON (LS and CLS architectures were tested) using a standalone burst-mode receiver with CDR and FEC.

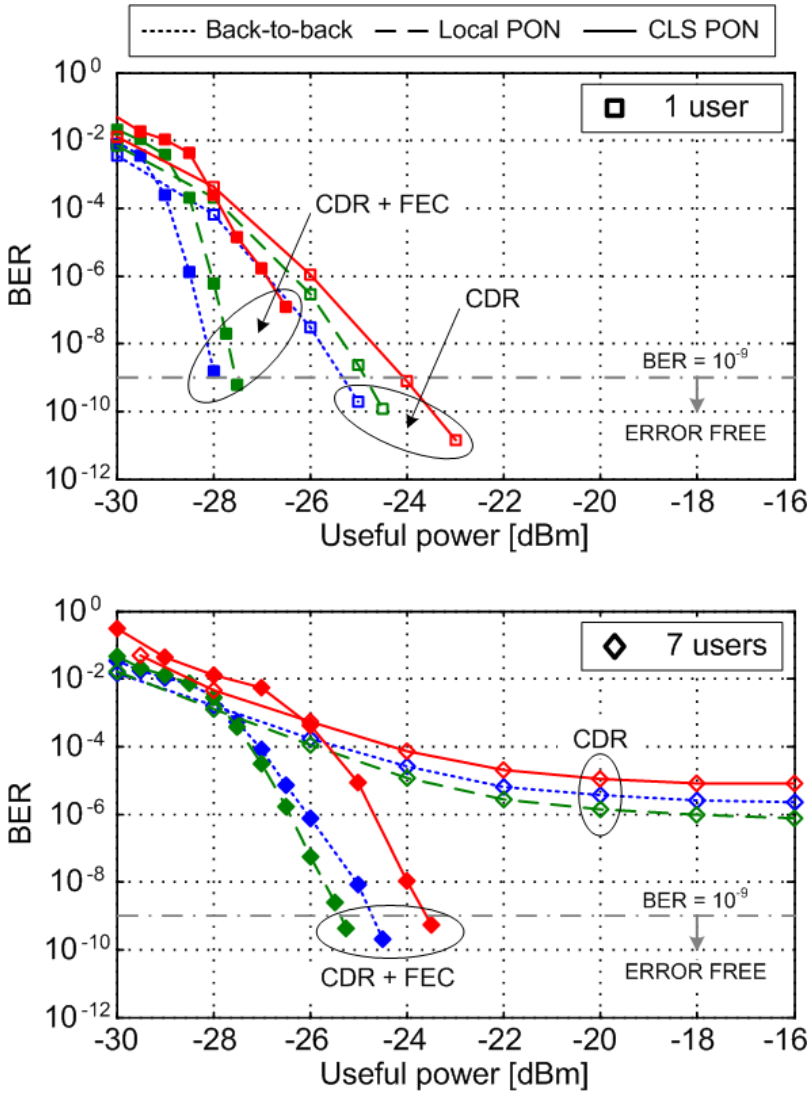


Fig. 6.38 BER versus useful power for a single user and fully-loaded systems (dotted lines for back-to-back; dashed lines for LS architecture; solid lines for CLS architecture).

Finally, in Fig. 6.38 we can compare the performance of LS and CLS architectures under our assumption of an 8:1 ratio of the relative power of the centralized to the local sources. A penalty of less than 2 dB was measured for LS at a BER of 10^{-9} when FEC and CDR were in use. Recall that this penalty is for the particular instance of a network of eight users, and an 8:1 ratio of relative power. We refer the reader to [27] for the analysis on how to generalize these results.

Simulation versus measurement of the BER using FEC for the three different configurations is shown in Fig. 6.39. Let P_e be the measured BER without FEC in Fig. 6.35, Fig. 6.36, and Fig. 6.37 for the various scenarios. Organizing the bits in symbols of m bits yields an equivalent symbol error rate of P_S, under the assumption of purely random bit errors, as

$$P_S = 1 - (1 - P_e)^m. \tag{6.4}$$

The RS(n, k) = RS(255,239) block-based FEC code divides a codeword of n symbols into 8-bit symbols and k data (uncoded) symbols, yielding in a memoryless channel, a symbol error rate after FEC P_e^{FEC} of [67]

$$P_e^{\text{FEC}} \approx \frac{1}{2^m - 1} \sum_{j=t+1}^{2^m-1} j \binom{2^m - 1}{j} P_S^j (1 - P_S)^{2^m-1-j} \tag{6.5}$$

where t is the symbol error correcting capability of the code given as

$$t = \left\lfloor \frac{n-k}{2} \right\rfloor \tag{6.6}$$

Note that $\lfloor x \rfloor$ represents the largest integer not to exceed x. Again, assuming a memoryless channel, the BER after FEC P_e^{FEC}, is about one half this symbol error rate, as we using orthogonal signaling (ON–OFF keying). We plot the memoryless channel prediction for P_e^{FEC} and our measurement in Fig. 6.39. There is one order of magnitude mismatch between simulation and measurements; our predictions are too optimistic. This is more likely due to the memory added to the channel through the BBS (intensity noise), the CDR, and other components.

In Fig. 6.40 we plot the PLR versus the phase difference between packets for the three configurations under test when using the SONET CDR without the phase picking algorithm. The power level was kept at -18 dBm for these and all subsequent measurements. Bursty traffic identical to that in Fig. 6.32 with zero preamble bits is generated for all users. We will demonstrate that our phase picker does not require any preamble bits for phase acquisition. We consider that all packets are correctly received when PLR $< 10^{-6}$, corresponding to a BER $< 10^{-10}$. We have restricted the horizontal axis to values from 0 to 1600 ps, corresponding to 0 to 2π rad phase difference at the desired bit rate ($\sim$622 Mb/s).

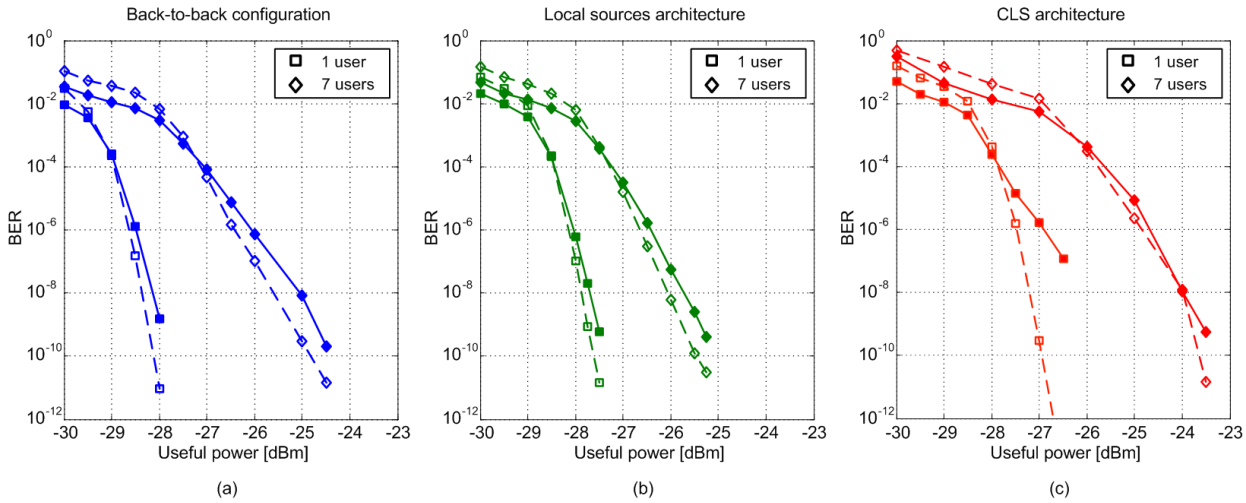


Fig. 6.39 Simulated and measured BER versus useful power for different configurations (dashed lines for simulated BER; solid lines for measurements): (a) back-to-back configuration, (b) LS architecture, (c) CLS architecture.

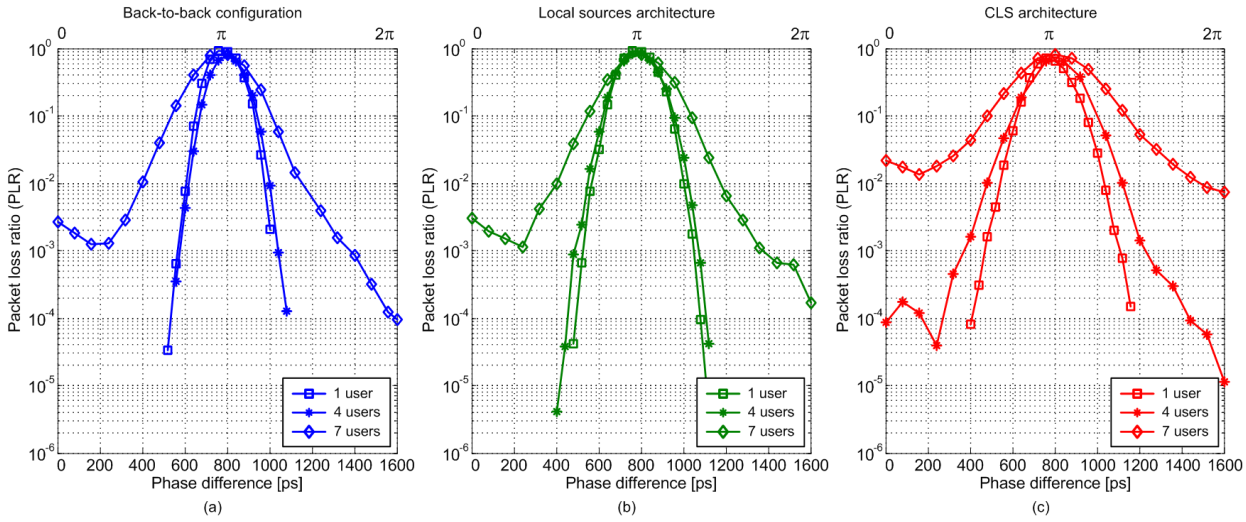


Fig. 6.40 PLR versus phase difference without CPA for different number of users: (a) back-to-back configuration, (b) LS architecture, (c) CLS architecture.

We did not consider the interval from -2π to 0 rad, because it gives theoretically the same performance as the positive interval. We observe bell-shape curves for PLR centered around 800 ps which corresponds to a phase shift of π rad, that is, the worst case. Jitter would have led to the worst case phase (π rad) being displaced from 800 ps, hence we conclude that jitter is not significant in our measurements. At relatively small phase shifts (near 0 or 2π rad), we note that for a single user system we can easily achieve zero PLR with the CPA module disabled, because the CDR is almost sampling at the middle of each bit. By comparing the curves on the same subplot, that is, for each configuration, we note the degradation in performance passing from a single user system to a fully loaded network of seven users. There is also a penalty when passing from the back-to-back configuration to the LS PON and then to the CLS PON, when comparing curves on different subplots. The degradation in the PLR can be explained by the corresponding degradation in the BER. As the BER performance degrades, there is a higher chance of having erroneous bits in the packet delimiter. With the delimiter not being correctly detected, a packet is declared lost, hence contributing to the packet loss count.

In order to show the improvement that can be achieved using the CPA functionality of our SAC-OCDMA burst-mode receiver, we have plotted in Fig. 6.41 the worst case PLR; that is, the maximum PLR value that occurs at π rad phase shift, against the number of users for the three configurations, with and without CPA. In the case of CDR without CPA, the worst case PLR is near 1 (see Fig. 6.40), as it corresponds to the receiver sampling at the edge of the eye diagram. In contrast, the phase picking algorithm samples each bit twice, within the eye, and significantly enhances the performance. With the CPA no packets are for lost up to four users for the three different architectures (PLR $< 10^{-6}$). Increasing the number of users beyond four deteriorates the BER and thus the PLR. For a fully loaded PON of seven users, the CPA algorithm can improve the performance by more than two orders of magnitudes.

The immunity of the CDR to silence periods is examined in terms of the CID length in Fig. 6.42, showing the PLR for the single user case for the back-to-back configuration, and the LS and CLS architectures. Recall that the useful power is still kept at -18 dBm and that the packets do not contain any preamble bits. The maximum length of CIDs can reach roughly 400, 600, and 800 bits for the CLS, LS, and the back-to-back configurations, respectively. A maximum of 200 bits of CIDs would guarantee zero packet loss for the three configurations; therefore our SAC-OCDMA burst-mode receiver meets all existing

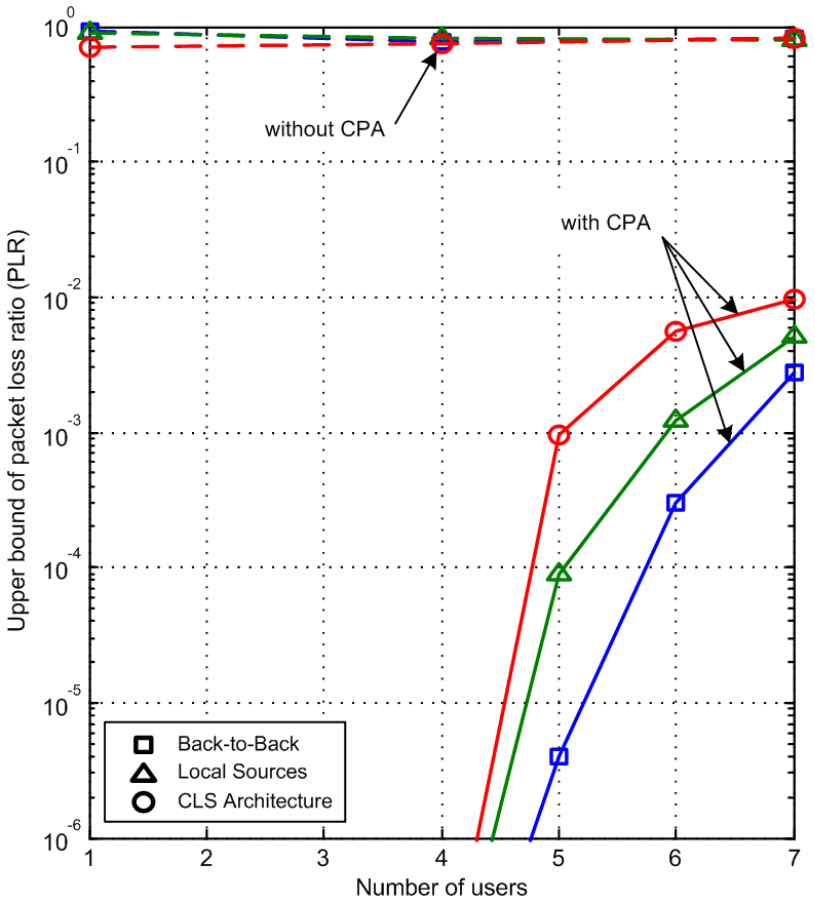


Fig. 6.41 PLR versus number of users for different PON architectures (dashed lines for the system without CPA; solid lines for the system with CPA).

PON standards.

6.6.5 Conclusion

We experimentally demonstrated different incoherent SAC-OCDMA PON physical architectures using a standalone burst-mode receiver at the OLT side. Local sources and centralized sources architectures have been examined. For experimental convenience, we examined only the two-feeder architecture; therefore, the effects of Rayleigh back-scattering are not addressed. Continuous and bursty upstream traffic for seven asynchronous users at 622 Mb/s were considered for the BER and the PLR measurements, respectively. We performed measurements at a bit rate of 666.43 Mb/s when using FEC to account for its

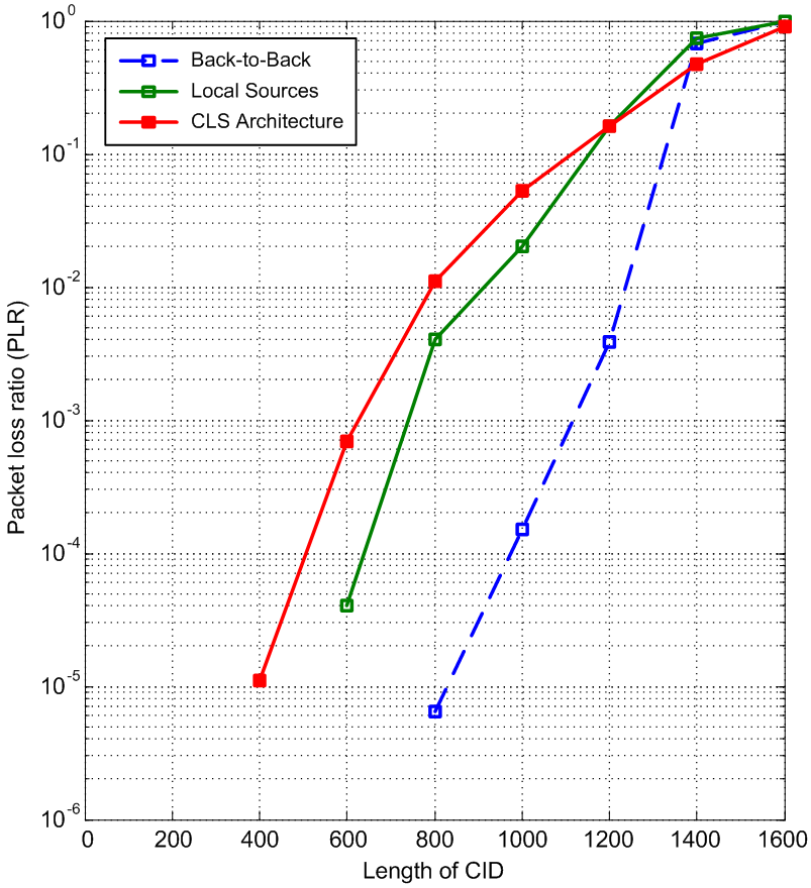


Fig. 6.42 PLR versus length of CID for different PON architectures.

overhead. Furthermore, we analyzed the power budget and the relative merits of LS versus CLS architectures. A small penalty of 2 dB added to the CLS with respect to the LS architecture was measured at a BER of 10^{-9}.

The OLT receiver we designed features automatic detection of payload, clock-and-data recovery, instantaneous (0 preamble bit) phase acquisition for any phase step, and FEC with a RS(255,239) decoder. Furthermore, the receiver significantly reduced the intensity noise of the BBS, and other impairments, by quantizing. We have also shown that the penalty added by the global clock due to the nonideal sampling is negligible. Error free transmission (uplink) was achieved for a fully loaded system of seven users for LS and CLS architectures. A coding gain of more than 2.5 dB at BER = $10^{-9}$was reported and BER floors for five users (only for the CLS PON) and seven users were eliminated with FEC. The FEC had one order of magnitude worse performance than that predicted for a memoryless

channel.

When using the CPA we have reported a zero PLR for up to four simultaneous users (for any phase difference between packets), and more than two orders of magnitude improvement for a fully loaded system (compared to using only the CDR without CPA) for the worst phase shift between packets. Our burst-mode SAC-OCDMA receiver proved to have a good immunity to silence periods in the sense that it can support several hundreds of CIDs at 622 Mb/s; therefore it is suitable for PON applications because the standards restrict the maximum CIDs to only 72 bits [33].

Author's Contribution

The author of this thesis designed and implemented the BM-CDR employed for this study, participated in all the experiments, analyzed the results, and characterized the BM-CDR.

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6.7 Summary

In summary, we first verified the functionalities of the proposed BM-CDRs based on semiblind time and space domain oversampling at the targeted bit rates of 5 Gb/s and 10 Gb/s, respectively, in Section 6.2. We also proposed two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition. Table 6.2 summarizes the performance of our BM-CDRs, and compares it to the state of the art BM-CDRs reported in literature.

In Section 6.3, we experimentally studied burst-mode reception at 5 Gb/s in a 20-km TDM GEPON uplink. The BM-CDR based on semiblind time domain oversampling is

Table 6.2 Performance summary of the proposed BM-CDRs compared to previous work

	Previous Work						This Work	
	[50]	**[68]**	**[69]**	**[70]**	**[71]**	**[72]**	**[3]**	**[1]**
Data Rate	2.488 Gb/s	10.3 Gb/s	10.3 Gb/s	10 Gb/s	10 Gb/s	10.3 Gb/s	5 Gb/s	10 Gb/s
BER	N/A	$< 10^{-12}$	$< 10^{-12}$	N/A	$< 10^{-12}$	$< 10^{-3}$	$< 10^{-10}$	$< 10^{-11}$
PLR	N/A	N/A	N/A	N/A	N/A	N/A	$< 10^{-6}$	N/A
Phase Acq. Time	100 bits	N/A	1 bit	32 bits	5 bits	1 bit	0 bits	0 bits
Freq. Lock Range	N/A	160 MHz	N/A	N/A	N/A	N/A	242 MHz	N/A
CID Tolerance	32 bits	N/A	160 bits	7 bits	31 bits	N/A	3100 bits	N/A

utilized in this work. The BM-CDR features: (1) BER and PLR sensitivities of −24.2 dBm and −25.4 dBm, respectively; (2) negligible burst-mode sensitivity penalty of 0.8 dB; (3) CID immunity of 3100 bits; and (4) frequency acquisition range of 242 MHz.

In Section 6.4, we experimentally showed burst-mode reception at 2.5 Gb/s in a 20-km O-SCM WDM PON uplink. The receiver employed in this study is a variant of the BM-CDR based on semiblind space domain oversampling. Our receiver provides more than 4 dB improvement in Q factor and guarantees error-free-operation due to its instantaneous phase picking.

In Section 6.5, we experimentally demonstrated burst-mode reception at 1.25 Gb/s in a 1300-km deployed fiber link that spans from Montreal to Quebec City and back. The BM-CDR based on semiblind time domain oversampling is utilized in this study. The receiver achieves: (1) BER and PLR sensitivities of −23 dBm and −19.5 dBm, respectively; (2) negligible burst-mode sensitivity penalty of 0.5 dB; (3) CID immunity of 1100 bits; and (4) low jitter transfer bandwidth of 2 MHz with low jitter peaking of 0.1 dB.

In Section 6.6, we experimentally investigated burst-mode reception at 622 Mb/s in a 7-user 20-km incoherent SAC-OCDMA PON uplink. We considered two network architectures, namely, LS and CLS, and studied their relative merits in a two-feeder topology. The receiver employed in this study is variant of the BM-CDR based on semiblind time domain oversampling with a Reed-Solomon RS(255,239) FEC decoder. The receiver provides: (1) a zero packet loss ratio for up to four simultaneous users; (2) more than two orders of magnitude (300-fold) improvement in the PLR for fully loaded PON system; and (3) more than 2.5 dB coding gain for a single-user system with BER floors completely eliminated.

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Chapter 7

Conclusions

OPTICAL multiaccess networks, and more specifically passive optical networks (PONs) are considered to be one of the most promising technologies for the deployment of fiber-to-the-premises/cabinet/building/home/user (FTTx) to solve the problem of limited bandwidth in local area networks (LANs). PONs achieve this with a low-cost solution and with a guaranteed quality of service (QoS). In a PON, multiple users share the fiber infrastructure in a point-to-multipoint (P2MP) network topology. This is in contrast to current access technologies, including asymmetric or very-high-bit-rate digital subscriber link (xDSL) and cable, which use a point-to-point (P2P) network topology. The nature of P2MP networks introduce optical path delays which inherently cause the data packets to undergo amplitude and phase variations—bust-mode traffic. Consequently, this creates unique challenges for the design and testing of optical receivers. The research presented in this thesis provided both, theoretical and experimental demonstrations of BM-CDRs. While the theoretical work laid the foundations for analyzing novel BM-CDR architectures, the experimental expositions were designed to illustrate the application potential of these BM-CDRs in various optical testbeds.

Through the proposed research, we anticipate a significant impact in research—a major contribution to the overall existing body of knowledge of BM-CDRs—benefiting the scientific and engineering disciplines through key findings. The outcomes of this research will have substantive significance on the optical communications infrastructure by the leading optical networking industries. More specifically, the studies will also bring forward new paradigms for test and measurement (T&M), benefiting T&M suppliers to forecast new

requirements. The physical layer performance results will provide network suppliers with the long-awaited solution needed to enable mass rollout of PONs. In the service provider domain, the optical budget studies will enable new services using FTTx. The unique solutions provided by our work will also translate into new specifications for next generation products, positively affecting the system vendor market.

In this chapter, we provide an overview of the journey through this thesis. We also summarize and reiterate the central ideas in this work. Finally, we give the direction for future work and other research opportunities.

7.1 Overview

In Chapter 1, we motivated the research presented in this thesis, detailed the problem statement putting our work on BM-CDRs in context, outlined the research objectives that demarcate the course of this research, and summarized our original contributions.

Chapter 2 provided the background necessary for the design and challenges of BMRx and BM-CDR circuits. We reviewed existing BMRx solutions present in the literature, with the prime focus being on state-of-the-art BM-CDRs along with their respective shortcomings.

Within this context, in Chapter 3 we demonstrated two novel BM-CDR architectures based on semiblind oversampling in both the time and space domain. The architectures are based on a hybrid topology, composed of a feedback (phase-tracking) CDR and a feedforward CPA. We detailed the high-level architecture, the phase picking algorithm, and the hardware implementation of the proposed BM-CDRs. These BM-CDRs have been designed to achieve error-free operation (BER $< 10^{-10}$) while featuring instantaneous (0 preamble bit) clock phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts.

In Chapter 4, we developed a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$ oversampling CDRs. The theoretical model quantitatively explains the performance of these circuits in terms of the BER and PLR.

Based on the probabilistic model, Chapter 5 quantitatively analyzed the performance of our proposed BM-CDRs by performing a comprehensive theoretical analysis. That is, we investigated the BER and PLR performance of the BM-CDRs to assess the tradeoffs between various parameters.

Finally, in Chapter 6 we first verified the functionalities of the proposed BM-CDRs based

on semiblind time and space domain oversampling at the targeted bit rates of 5 Gb/s and 10 Gb/s, respectively. We also proposed two burst-mode setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition. We then experimentally demonstrated and analyzed the BM-CDR architectures in various optical test beds including: (1) 5 Gb/s time-division multiplexing (TDM) gigabit ethernet PON (GEPON) 20-km uplink; (2) 2.5 Gb/s overlapped subcarrier-multiplexing (O-SCM) wavelength-division multiplexed (WDM) PON 20-km uplink; (3) 1.25 Gb/s 1300-km deployed fiber link spanning from Montreal to Quebec City and back; and (4) 622 Mb/s in a 7-user incoherent spectral amplitude-coded optical code-division multiple access (SAC-OCDMA) 20-km PON uplink. In particular, we validated the developed probabilistic theory of BM-CDRs with the experimental results, and studied the effect of channel-impairments on burst-mode reception in these test beds. Furthermore, we note that these experimental expositions were designed to illustrate the application potential of these BM-CDRs—"a solution looking for problems".

7.2 Summary

Fig. 7.1 summarizes our original contributions. Each contribution belongs to one of two proposed research areas: (1) BM-CDR circuits for PONs; and (2) probabilistic theory of BM-CDRs. We summarize the contributions for each of these research topics respectively. Our contributions to these topics are all novel and have not been previously demonstrated. The evidence of our original scholarship to the overall existing body of knowledge of BM-CDRs is manifested by the 22 peer-reviewed publications that have so far resulted from the research presented in this thesis: journal articles [1–6] and conference proceedings [7–21] including two invited conference papers [9, 10].

7.2.1 BM-CDR Circuits for PONs

We demonstrated two novel BM-CDR architectures based on oversampling in both the time and space domain. These BM-CDRs achieve error-free operation [BER $< 10^{-10}$] while providing instantaneous (0 preamble bit) clock phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts. Instantaneous phase acquisition can be used as follows: (1) improve the physical efficiency of the upstream PON traffic; (2) reduce the burst-mode sensitivity penalty; and (3) increase the effective throughput of the system by increasing the information rate. Our eloquent solution is to leverage the design of

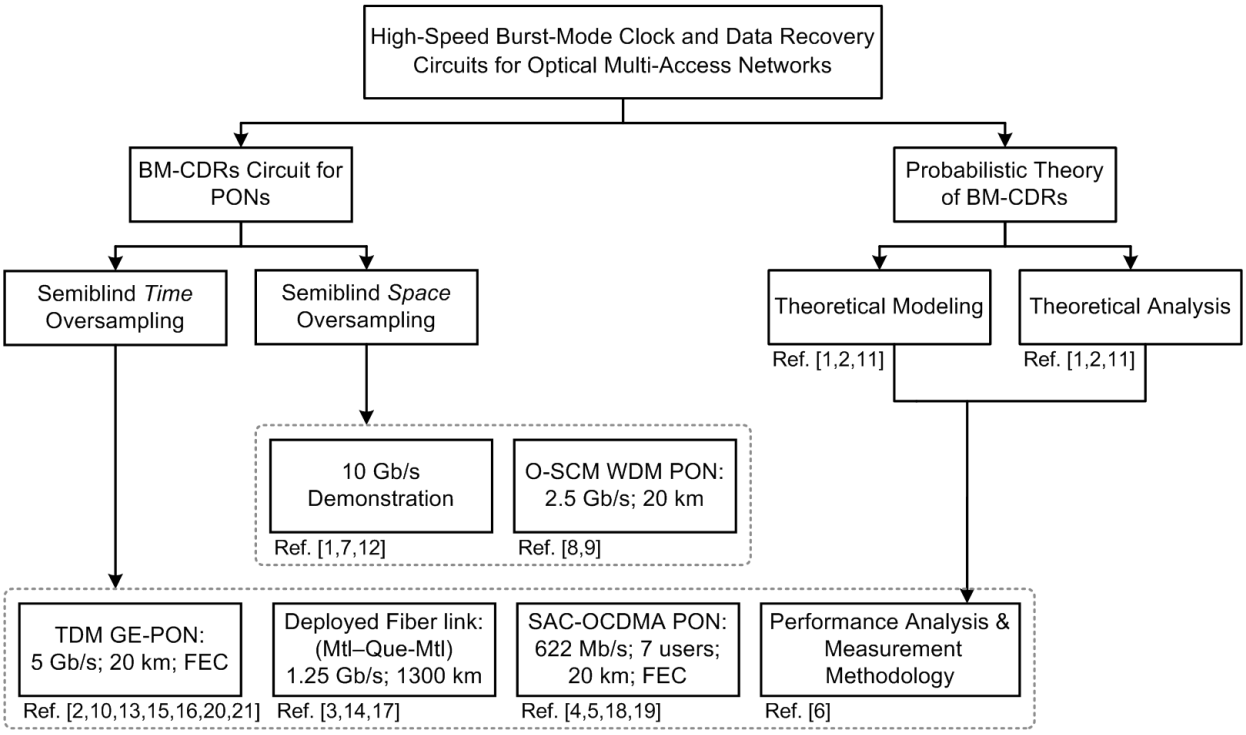

Fig. 7.1 Summary of the original research contributions reported in this thesis.

components for long-haul transport networks using low-complexity, commercial electronics providing a cost-effective solution for PON BM-CDRs. These components are typically a generation ahead of the components for multiaccess networks. Thus, our solution will scale with the scaling for long-haul networks.

BM-CDR Based on Semiblind Oversampling in Time Domain

- Designed and implemented a BM-CDR for PONs based on semiblind time domain oversampling in. The BM-CDR is based on a phase-tracking CDR circuit operated at 2× the bit rate and a CPA that makes use of a phase picking algorithm. We experimentally demonstrated the BM-CDR operation at 5 Gb/s.

- Experimentally demonstrated burst-mode reception at 5 Gb/s in a 20-km TDM GEPON uplink. We carried out a detailed set of experiments to investigate the effect of silence period, including phase step and the length of consecutive identical digits (CIDs), between successive upstream PON bursts from independent ONUs,

received signal power, and finite frequency offset between the sampling clock and desired bit rate, on the BER and PLR performance of the BM-CDR. Consequently, we characterized the BM-CDR in terms of the phase acquisition time, CID immunity, burst-mode sensitivity penalty, dynamic range, and frequency acquisition range.

The BM-CDR features: (1) BER and PLR sensitivities of -24.2 dBm and -25.4 dBm, respectively; (2) negligible burst-mode sensitivity penalty of 0.8 dB; (3) CID immunity of 3100 bits; and (4) frequency acquisition range of 242 MHz.

- Experimentally studied burst-mode reception at 1.25 Gb/s in a 1300-km deployed fiber link that spans from Montreal to Quebec City and back. We investigated the effects of channel impairments on the performance of BM-CDR in terms of the PLR and BER, and quantify it as a function of the phase step between consecutive packets, received signal power, and CID immunity. We also assessed the tradeoffs in preamble length, power penalty, and pattern correlator error-resistance. These results will help refine theoretical models of receivers employed in the optical packet switched networks (OPSNs), and provide input for establishing realistic power budgets.

  The receiver achieves: (1) BER and PLR sensitivities of -23 dBm and -19.5 dBm, respectively; (2) negligible burst-mode sensitivity penalty of 0.5 dB; (3) CID immunity of 1100 bits; and (4) low jitter transfer bandwidth of 2 MHz with low jitter peaking of 0.1 dB.

- Experimentally investigated burst-mode reception at 622 Mb/s in a 7-user 20-km incoherent SAC-OCDMA PON uplink. The receiver employed in this work is variant of the BM-CDR based on semiblind time domain oversampling with a Reed-Solomon RS(255,239) forward-error correction (FEC) decoder. We considered two network architectures, namely, local sources (LS) and centralized LS (CLS), and studied their relative merits in a two-feeder topology. The LS and CLS architectures were tested experimentally, and BER and PLR were measured. The immunity of the CDR in terms of CID was also measured. We simulated the BER with FEC in order to validate our measurements. We quantify the increase in soft capacity via FEC, while working with a nonideal recovered clock that provides realistic, achievable sampling.

  The receiver provides: (1) a zero packet loss ratio for up to four simultaneous users; (2) more than two orders of magnitude (300-fold) improvement in the PLR for fully

loaded PON system; and (3) more than 2.5 dB coding gain for a single-user system with BER floors completely eliminated.

- Developed a performance analysis approach and a practical measurement methodology to correctly and completely characterize any device under test (DUT) including synchronous optical network (SONET) CDRs, BMRx, BM-CDRs, and frequency synthesizers. This methodology is based on both BER and PLR measurements. In our burst-mode test setup, we can set the amplitude and relative phase of the packets, the preamble length, the length of CIDs, and control the received signal power. We characterized the proposed BM-CDR in terms of the phase acquisition time, burst-mode sensitivity penalty, frequency lock range, CID immunity, and dynamic range, while also assessing the tradeoffs in preamble length, burst-mode sensitivity penalty, and pattern correlator error resistance. We also proposed two burst-mode test setups to test BM-CDRs for either the inter-packet or intra-packet phase acquisition.

BM-CDR Based on Semiblind Oversampling in Space Domain

- Designed and implemented a BM-CDR for PONs based on semiblind space domain oversampling. The BM-CDR is based on a phase-tracking CDR circuit with multiphase clocks at the bit rate and a CPA that makes use of a novel phase picking algorithm. In contrast to the BM-CDR based on semiblind time domain oversampling, this BM-CDR uses electronics operated at the bit rate with *no a priori* knowledge of the packet delimiter, leading to a more efficient power consumption and being truly modular across application testbeds, respectively. We experimentally demonstrated the BM-CDR operation at 10 Gb/s.

- Experimentally showed burst-mode reception at 2.5 Gb/s in a 20-km O-SCM WDM PON uplink. The receiver employed in this work is a variant of the BM-CDR based on semiblind space domain oversampling.

  Our receiver provides more than 4 dB improvement in Q factor and guarantees error-free-operation due to its instantaneous phase picking.

7.2.2 Probabilistic Theory of BM-CDRs

We provided for the first time to our knowledge, a theoretical framework to model and analyze BM-CDRs. This coupled with the experimental results will refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets.

Theoretical Modeling of BM-CDRs

- Developed a unified probabilistic theory of BM-CDRs based on semiblind oversampling techniques in either the time or space domain. This theory has also been generalized for conventional CDRs and $N\times$-oversampling CDRs. The theoretical model quantitatively explains the performance of these circuits in terms of the BER and PLR. The model accounts for the following parameters: (1) silence periods, including phase steps and the length of CIDs between successive upstream PON bursts from independent ONUs; (2) finite frequency offset between the sampling clock and desired bit rate; (3) packet preamble length; (4) jitter on the sampling clock; and (5) pattern correlator error-resistance.

Theoretical Analysis of BM-CDRs

- Analyzed quantitatively the performance of the proposed BM-CDRs by performing a comprehensive theoretical analysis. That is, we evaluated the BER and PLR performance of the BM-CDRs to assess the tradeoffs between various parameters, and compared the results experimentally to validate the theoretical model. Specifically, we investigated the following: (1) effect of phase step between consecutive packets from independent ONUs; (2) effect of the packet preamble length; (3) effect of RMS jitter on the recovered sampling clock; (4) effect of pattern correlator error-resistance; and (5) effect of finite frequency offset between the local oscillator (LO) and desired bit rate.

7.3 Future Research Avenues

Although the objectives of this research have been achieved, probing deeper, there are still other research opportunities to be investigated. Below, we propose directions for future research that could be derived from the work we presented in this thesis.

7.3.1 BM-CDR Circuits for PONs

1) Target Higher Bit Rates: Taking into account the increasing trends of bandwidth requirements, optical receivers for multiaccess networks must support higher data rates. In this thesis we demonstrated a 5-Gb/s and 10-Gb/s BM-CDRs based on semiblind oversampling in time and space domain, respectively. These BM-CDRs exploit the design of components for long-haul networks which are typically ahead of the components for PONs. Currently, PONs support a maximum data rate of 10 Gb/s, whereas 40 Gb/s and 100 Gb/s is currently mainstream for long-haul networks. Assuming this holds true in the future, with the scaling of components for long-haul networks, our solution will also have to scale.

2) Dual-rate BM-CDRs: 10G-EPON task force has recently standardized the physical specifications to attain a total bandwidth of 10 Gb/s [22]. The current line rates of GEPON [23] and GPON [24] are 1.25 Gb/s and 2.488 Gb/s, respectively. From an upgrade and cost point of view, 10G-EPON will need to support 10 Gb/s and lower line-rates concurrently. This can be achieved in the downstream direction by using separate wavelength bands. However, in the upstream direction a BM-CDR capable of receiving multiple line-rates will be essential to terminate both 10 Gb/s and legacy 1.25/2.5 Gb/s users at the central office (CO). Our BM-CDRs, with additional circuitry, can be upgraded to support multiple line-rates.

3) System on Chip Design: The current design of the BM-CDRs was to demonstrate the proof-of-concept. Thus, they were built from commercially available off-the-shelf components and therefore rather bulky. If this system is to be viable as a commercial product with the expected mass roll-out and deployment of PONs in the near future, then one of the goals is to scale the design down to an application specific integrated circuit (ASIC) for easy device integration. One could target the current state-of-art in silicon technology in CMOS for the next generation products.

4) Holistic Solution: The task of amplitude recovery is handled by the BMRx which also performs an optical-to-electrical (OE) conversion. The work presented in this thesis, assumes that an effective front-end is supplied. Thus, the focus was on the BM-CDRs which provide solutions to the phase alignment problem. To promote a full burst-mode solution with both amplitude and phase recovery—holistic solution—the BM-

CDR should be integrated and tested with a BMRx.

5) *Concatenate FEC Codes:* The receiver employed for the 622-Mb/s SAC-OCDMA 20-km PON uplink experiments is a variant of the BM-CDR based on semiblind time domain oversampling with a RS(255,239) FEC decoder. Block codes (RS codes) and convolutional codes (Viterbi codes) can be combined to work together. This is achieved by using the convolutional codes to first detect and correct errors, and then allow the block codes to correct the errors made by the convolutional decoder. In literature, this has shown to be a very effective technique. Thus, the RS(255,239) decoder in the receiver, can be replaced by such a "concatenated" coding scheme to achieve higher coding gains, further relax the requirements and/or increase the optical link budget PONs, and support more number of users.

6) *Nonlinear vs. Linear Phase Detector:* In the experiments involving 2.5 Gb/s O-SCM WDM 20-km uplink in Section 6.4, a proof-of-concept receiver based on a *bang-bang* (nonlinear) Alexander phase detector [25] was used to test the principle for $\pm\pi/2$ rad phase steps. We showed that the receiver is able to track the instantaneous phase variations and to achieve efficient SCM down-conversion. To make the receiver able to instantaneously track phase variations over a full 0 to $\pm\pi$ rad range, we propose replacing the Alexander phase detector with a linear Hogge phase detector [26]. In this case, the output of the phase detector would simply control a phase shifter that adjusts the phase of the clock before being passed to the clock divider and the radio frequency (RF) mixer.

7) *BM-CDR Based on Blind Oversampling:* The BM-CDR based on semiblind space domain oversampling employs a hybrid topology of a feedback CDR and feed-forward CPA. The novel phase picking algorithm can in principle work without the CDR. This will make the BM-CDR based on a feed-forward *only* architecture, that is, blind oversampling. This will provide an even more cost-effective solution.

7.3.2 Probabilistic Theory of BM-CDRs

1) *Deterministic jitter:* The proposed probabilistic theory of BM-CDRs is for data in non-return to zero (NRZ) format, and it is independent of the bit rate and pulse shape,

as long as the channel remains limited by Gaussian noise. Random jitter (RJ), approximated to a Gaussian probability distribution, is included in the model. The effect of deterministic jitter (DJ) is to shrink the data eye by a finite amount and will only further deteriorate the performance of the device under test. Thus, in order to simplify the mathematical modeling, DJ was ignored. However, with scaling of data rates the channel will no longer be Gaussian noise limited, in which case the effect of DJ should also be included in the theoretical model.

2) Jitter Analysis: The jitter transfer bandwidth, jitter peaking, and jitter tolerance of BM-CDRs based on semiblind time domain oversampling has been theoretically studied in [27]. These results should be extended to investigate the jitter characteristics of BM-CDRs based on semiblind space domain oversampling. This will enable one to study the relative merits of both the BM-CDR architectures. Furthermore, these theoretical results should be compared to experimental results—a jitter analyzer will be required for these measurements.

3) Behavioral Simulation Platform for BM-CDRs: It will be beneficial to develop a behavioral simulation platform for BM-CDR tools. This software will allow one to: (1) build fast and accurate behavioral models for novel BM-CDR architectures; (2) test these architectures under burst-mode test setups; and (3) simulate and derive theoretical performance of these BM-CDRs including jitter transfer bandwidth and jitter tolerance.

The results we reported in this thesis provide a strong foundation for future work. In this section, we just presented some suggestions and examples for future work.

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