Growing Silicon Thin–Films Laterally Over Amorphous Substrates Using the Vapor–Liquid–Solid Technique

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DEDICATION

To everyone I have lost or left behind chasing these dreams.

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ABSTRACT

A new technique for growing two–dimensional, laterally grown silicon crystals has been developed. This research borrows from previously reported crystal growing techniques such as Bridgman–Stockbarger growth, epitaxial layer overgrowth, and the vapor–liquid–solid method. Reviews of these technologies are presented. To achieve laterally growth of silicon films, a variant of the vapor–liquid–solid method was utilized, along with equipment and materials traditionally used for microelectronics, to fabricate test structures know as micro–crucibles. These test structures are templates of amorphous materials which confine gold catalyst to a specified geometry. Upon the introduction of a reactive, silicon–containing gas, which diffuses into the micro–crucible and preferentially cracks at the confined gold catalyst, the vapor–liquid–solid process takes place and two–dimensional silicon crystals are nucleated from supersaturated gold–silicon alloys within the confines of the micro–crucible. The experimental techniques used to fabricate the micro–crucibles and analyze the silicon growth are described, and new theories on the mechanics of vapor–liquid–solid growth within the micro–crucible test structures are discussed. Semiconducting films grown laterally from micro–crucibles are potential enablers of photovoltaic, optical interconnect, three–dimensional transistor and silicon/III–V on–chip integration technologies, and micro–crucibles are as useful research tools for fundamental studies on grain boundary and solidification theory.

ABRÉGÉ

Une nouvelle technique pour faire croître des cristaux deux-dimensionnels de silicone, crûs latéralement, a été développée. Cette recherche prête des techniques rapportées antérieurement, tel que la croissance Bridgman–Stockbarger, la surcroissance épitaxiale par couches et la méthode vapeur–liquide–solide. Ces techniques sont révisées et discutées en détails. Pour obtenir des pellicules de silicone crues latéralement, une variation de la méthode vapeur–liquide–solide a été utilisée avec de l'équipement et des matériaux utilisés surtout dans des microélectroniques. Des structures tests, appelées des micro–creusets, ont donc été fabriquées. Ces structures tests sont des modèles de matériaux amorphes qui confinent un catalyseur d'or à une géométrie spécifique. Pendant l'introduction d'un gaz contenant de la silicone réactif, qui diffuse dans le micro–creuset et fend préférentiellement au catalyseur d'or confiné, le procédé vapeur–liquide–solide prend place et il y a une nucléation des cristaux de silicone deux–dimensionnels surgissant des alliages sursaturés d'or et de silicone dans les confines du micro–creuset. Les techniques expérimentales utilisées pour fabriquer les micro–creusets et pour analyser la croissance du silicone sont décrites, et de nouvelles théories sur les mécanismes de la croissance vapeur–liquide–solide dans les micro–creusets sont discutées. Les pellicules semi–conductrices crues latéralement sont des facilitatrices potentielles de photovoltaiques, d'interconnexions optiques, de transistors trois–dimensionnels et de technologies intégratrices de puces silicone/III–V. Les micro–creusets sont aussi des outils de recherche utiles pour des études fondamentales sur les fonds de grains et la théorie de solidification.

PREFACE

This thesis is presented in the manuscript-based form offered to PhD candidates at McGill University, with Sections 3.1, 3.2 and 3.3 being published, or in the process of being published though peer–reviewed journals. These sections are largely unaltered from their originally submitted manuscripts, and thus include abstracts and experimental sections with overlapping subject matter.

CONTRIBUTIONS OF AUTHORS

All manuscripts have been submitted with Prof. N. J. Quitoriano, as a co–author, with the manuscripts of Sections 3.2 and 3.3 also including N. Brodusch and Prof. R. Gauvin as co–authors. The papers that form these sections are as follows:

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LeBoeuf, J.L., Brodusch, N., Gauvin, R., Quitoriano, N.J. (2014). "Lowtemperature, vapor–liquid–solid, laterally grown silicon films using alloyed catalysts", *Materials Research Express*, *Accepted*. (Section 3.3)

I hereby give copyright clearance for the inclusion of the above papers, of which I am a co–author, into the PhD dissertation of Jerome LeBoeuf.

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Date

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Signature

Date

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1
Research Motivations and Literature Review

With the ever increasing demands for digitization, automation, telecommunication and energy production witnessed in the past half century, there is an impetus for the development of semiconducting materials and a mandate from modern societies to have scientists and engineers research new methodologies and establish new techniques to provide for these demands. Through the use of semiconductors, unimaginable progress in all fields of science and technology have been made, resulting in what is collectively known as the digital or information age. Developing processes which produce larger, higher quality semiconductor crystals at lower costs is the foundation on which this continuous technological progression sits, and in this work, a novel semiconductor growth process will be outlined with a potential to bring new applications to classes of semiconducting materials which have been traditionally been perceived as being too expensive for mass production.

The semiconducting material which has defined this digital age has been silicon grown using the Czochralski process [1]. Because of the low cost and the robustness of the process, boules of high–quality silicon are grown to diameters 450 millimeters commercially. These boules grown by the Czochralski process are diced into silicon wafer substrates for the current generation of complementary metal–oxide–semiconductor (CMOS) technologies, with which the majority of modern microelectronic devices are fabricated. Because the cost of silicon is essentially fixed due it

its abundance on Earth, Dr. Gordon Moore [2] made the economic prediction in 1965 that, for a given manufacturing cost, the only way to lower the price of a silicon microelectronic good is to fabricate more of it over a given substrate size. This prediction has been the business model of the integrated circuit industry since, and has resulted in the miniaturization of silicon microelectronics by orders of magnitude over the previous decades. Because there is a marginal cost difference, namely in the capital equipment investment, between fabricating one hundred integrated circuits on a 100 millimeter substrate and one thousand integrated circuits on a 450 millimeter substrate, reliable production of larger crystals and thus larger substrates has been as important as miniaturization with regards to the cost reduction of silicon microelectronic goods.

Unfortunately not all semiconducting materials of technological interest can be produced with the low cost Czochralski process, particularly the one which hold the most promise for photovoltaic, telecommunications, optics and laser applications. Typically, the III–V and II–IV semiconductors required for these applications are grown using more expensive processes like vapor–phase epitaxy (VPE) or metalorganic vapor–phase epitaxy (MOVPE) on latticed mismatched substrates like gallium arsenide or germanium, which themselves are grown using more expensive, less mass–producible processes [3]. The defects and impurities associated with VPE and MOVPE [4], as well as the dislocations associated with growth on lattice matched substrates [5] [6] [7] [8] makes commercial production of III–V and II–IV semiconductors significantly more difficult and expensive, and the current state–of–the–art for

these technologies limits the size of substrates which can be used. The difficulties associated with growing non–silicon high–quality crystals for semiconductor substrates and the limited producible substrate sizes for these materials drives up the costs of photovoltaic, telecommunications, optics and laser devices.

Currently, the majority of commercially produced, high–quality semiconducting substrates are grown using variations on the Czochralski or Bridgman-Stockbarger processes [9] [10], or with vapor phase epitaxy using either chemical vapor deposition (CVD) or molecular beam epitaxy (MBE). However, research on how to integrate high–quality growth onto preexisting, low cost substrates like Czochralski grown silicon or glass has been attempted since the beginning of microelectronics miniaturization, and relevant to this research is a technique known as epitaxial layer overgrowth (ELO) [11]. Using ELO, a high–quality, semiconducting thin–film is grown over a seeding substrate which is masked using an amorphous thin–film. Originally the semiconducting thin–films were seeded using homoepitaxy, that is from a substrate which is chemically and crystallographically the same as the thin–film growing over the amorphous layer, but once heteroepitaxy techniques were developed [12], ELO became a much more versatile and cost effective way to integrate high–quality growth on to inexpensive substrates. The vapor–liquid–solid (VLS) technique, first reported by Wagner and Ellis in 1964 [13], is another integrable growth technique which yields high–quality semiconductor crystals on inexpensive substrates and has received considerable amounts of attention with the realization that VLS growth is a key enabler of nanotechnologies [14]. The VLS technique is the primary inspiration for the research presented in this work and the understandings of the process will

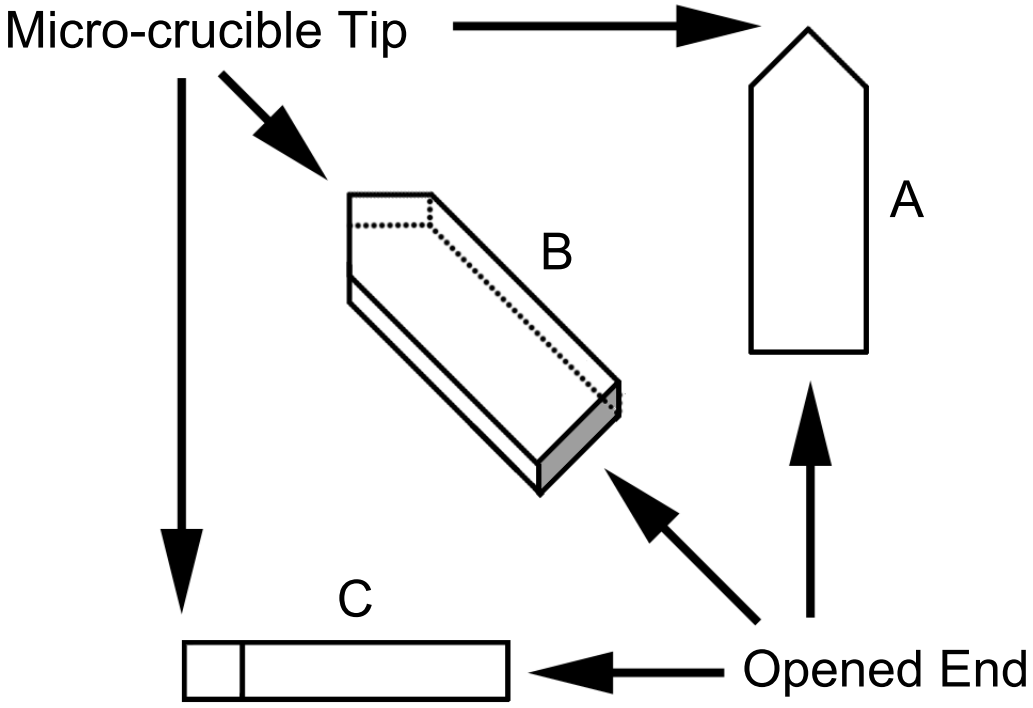

Figure 1–1: Plan (A), isometric (B) and cross–sectional views (C) of the micro–crucible structure used to experimentally produce high–quality semiconducting crystals. A gold catalyst is located at the tip of the micro–crucible, and opening opposite the tip allows gaseous semiconducting precursors to diffuse to the catalyst and preferentially crack at its surface, thus resulting in a VLS reaction and crystal growth within the crucible.

be discussed at length in Section 1.2. Most recently there has been a push in the research to develop spatially controlled, confined growth [15], and lateral growth [16], i.e. growth parallel to the substrate, of high–quality semiconducting materials using techniques which synthesize the lessons learned from the ELO, VLS and Bridgman-Stockbarger techniques, and it is here where this research attempts to contribute original knowledge to the field.

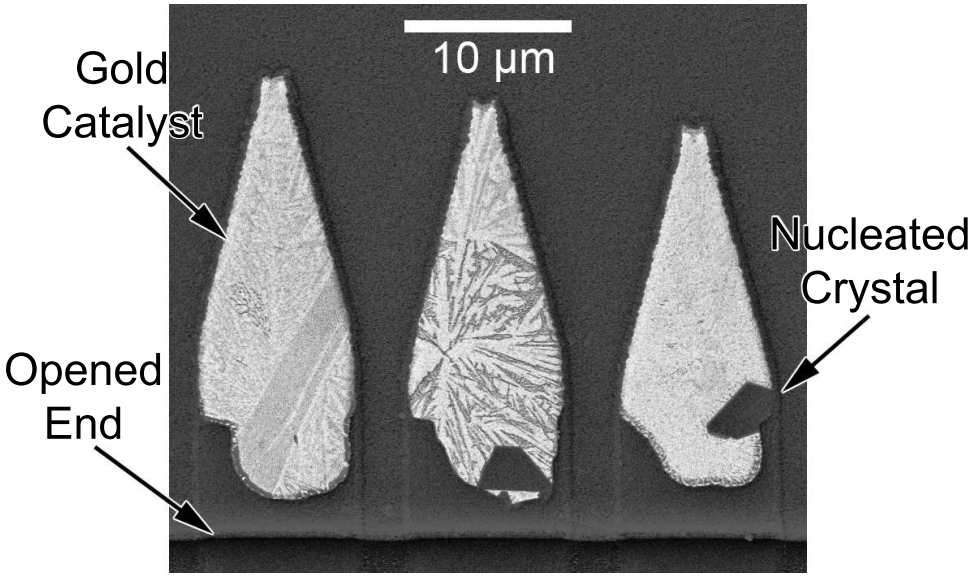

Figure 1–2: A plan–view backscatter electron micrograph of three neighboring micro–crucibles, the middle and rightmost crucibles have nucleated semiconductor crystals during a CVD process using the VLS technique. The crystals are confined to morphology of the amorphous micro–crucible and grow laterally as they grow larger.

To investigate the lateral growth of spatially controlled, semiconducting thin–films, an amorphous template has been designed and fabricated using CMOS technologies on thermally oxidized silicon and glass substrates. The amorphous template used in this work has been termed a micro–crucible, as it functions much like the crucibles used for the Bridgman-Stockbarger technique, but its dimensions are on the order of microns. Figure 1–1 depicts a plan–view (A), isometric view (B), and cross–sectional view (C) of the typical micro–crucible geometry. These micro–crucibles promote growth in spatially controlled, confined areas on the substrate by taking advantage of VLS research, and selectively depositing a gold catalyst at the micro–crucible tip, marked in Figure 1–1. Allowing a gaseous semiconductor precursor to diffuse, using a CVD process, to the catalyst through the opening in the micro–crucible causes the vapor–liquid–solid process to occur within the crucible and results in the nucleation of a high–quality semiconducting crystal. Unlike the vapor–liquid–solid growth associated with nanowire research, the semiconducting crystals grown within micro–crucibles, as imaged in Figure 1–2, nucleated from critically supersaturation solutions, where there is enough free energy in the solution to over come the energy barriers associated with forming the solid–liquid phase boundary of the new phase [17] [18] [19]. The newly nucleated crystals are grown laterally, within the micro–crucible, over the amorphous substrate as long as the CVD process continues and the crystals can be engineered into a number of morphologies defined by the confining structure. It is in this work that questions on micro–crucible fabrication, diffusion of semiconductor species within the micro–crucible, nucleation and growth

of high–quality semiconductor crystals within micro–crucibles, and crystalline defections associated with VLS growth in micro–crucible will be addressed.

A larger goal of this work is to provide a technological platform, which lowers the cost of production of III–V and II–IV semiconductor substrates, particularly for photovoltaic applications. To enable third–generation photovoltaic technologies [20], high–quality thin–films of germanium, gallium arsenide and its allied III–IV compounds need to be produced cheaply to maximize solar energy conversion and minimize cost. This can be done using multi–junction solar cells, but in order to fabricate multi–junction, III–V solar cells, lattice matched substrates of germanium and gallium arsenide are used to mitigate the conversion–lowering effects of lattice–mismatched dislocations and grain boundaries. These substrates are expensive and the technology using them does not convert solar electricity at prices which are competitive with traditional energy sources used for large scale electric grids. Semiconductor growth using the VLS process and amorphous micro–crucibles is potentially enabling because high–quality semiconducting seeds are produced without the need of an expensive seeding substrate, and substrates such as glass, which is inexpensive and the substrate of choice for current thin–film photovoltaic manufacturers, are easily integrated into the micro–crucible fabrications process. Ideally, semiconducting silicon crystals grown in micro–crucibles will be used to seed larger crystals grown from VPE and MOVPE processes to produce substrates similar to the one depicted in Figure 1–3, where a large grained III–V substrate has been seeded by micro–crucible grown crystals over an amorphous silicon oxide thin–film. Outside of photovoltaics and in more traditional integrated circuit technologies, semiconducting films grown

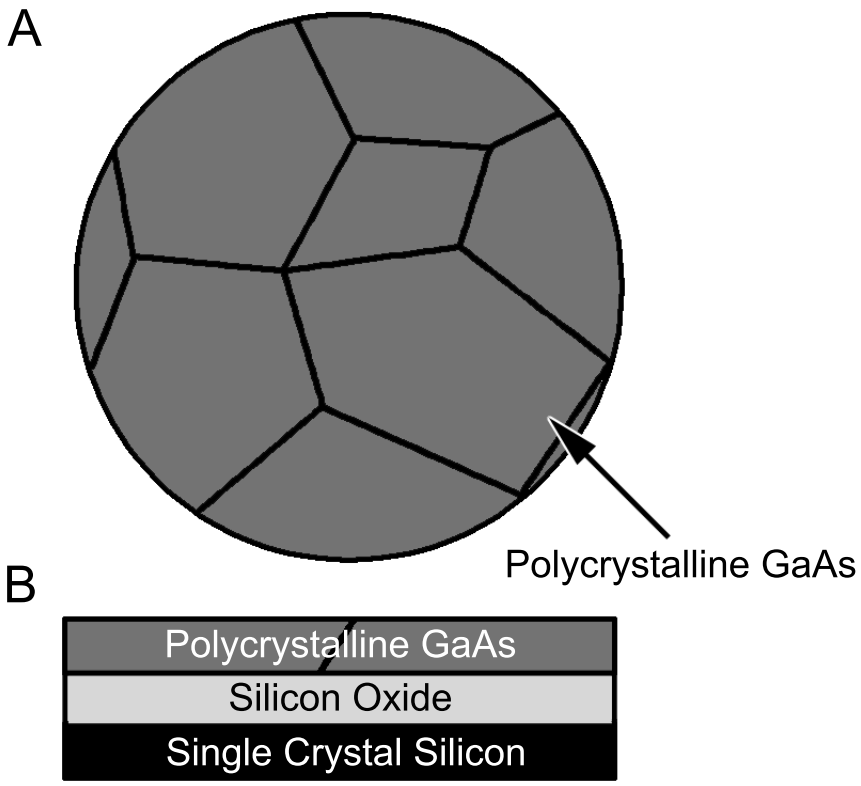

Figure 1–3: A larger goal of this work is to provide a technology which lowers the cost of high efficiency photovoltaics. Here a large grained GaAs substrate is depicted as being produced by thermally oxidizing a silicon substrate, fabricating micro–crucibles (not pictured) on the substrate, and growing GaAs seeds in the micro–crucibles using the VLS process. The seeded substrate is placed into a VPE or MOVPE deposition process where the larger GaAs grain pictures in Figure 1–3A nucleate at sites where the previously grown micro–crucible seeds were located. After nucleating, the larger GaAs grains grew laterally over the amorphous silicon oxide substrate until covering the entire surface and impinging one another.

laterally from micro–crucibles can be used to enable optical interconnects, three–dimensional transistors and silicon/III–V on–chip integration.

1.1 Gold–Silicon Research and Technology

The history of integrating gold into semiconducting materials is as old as the first point contact transistor [21]. Indeed the first metal contacts on that germanium transistor were gold, most likely due the widespread use of gold in the laboratory. Owing to its nobility, its ease of forming, its ease of purifying, its good conductivity and its heat conduction properties, gold is typically the first material used when an experiment calls for a "metal". Unfortunately for silicon microelectronics, gold acts as a deep–level electronic defect between the valence and the conduction bands of the silicon band gap, which reduces electron minority carrier lifetimes and inhibits electron mobility in the material and thus leaves gold unusable for commercial applications of silicon semiconducting technologies. This has not inhibited the use of gold and silicon with regards to fundamental research and growth studies, which is fortunate as gold and gold–silicon alloys offer some unique advantages to this field.

Figure 1–4 is an equilibrium gold–silicon phase diagram where the x–axis is taken to be the atomic percent of silicon in the gold–silicon alloy. The gold–silicon system is a simple binary with limited solid–state solubility of both gold in silicon and silicon in gold. Thermodynamic investigations of the gold–silicon system [22] [23] [24] [25] [26] [27] suggests insignificant solubility of gold in silicon, with exception to concentrations which effect the electrical properties of silicon. Silicon in gold is less studied and upwards of 2% silicon solubility [22] [27] could be possible, but has not been experimentally reported. In addition to the limited solid–state solubility of gold in silicon and silicon in gold, the gold–silicon systems lacks thermodynamically stable

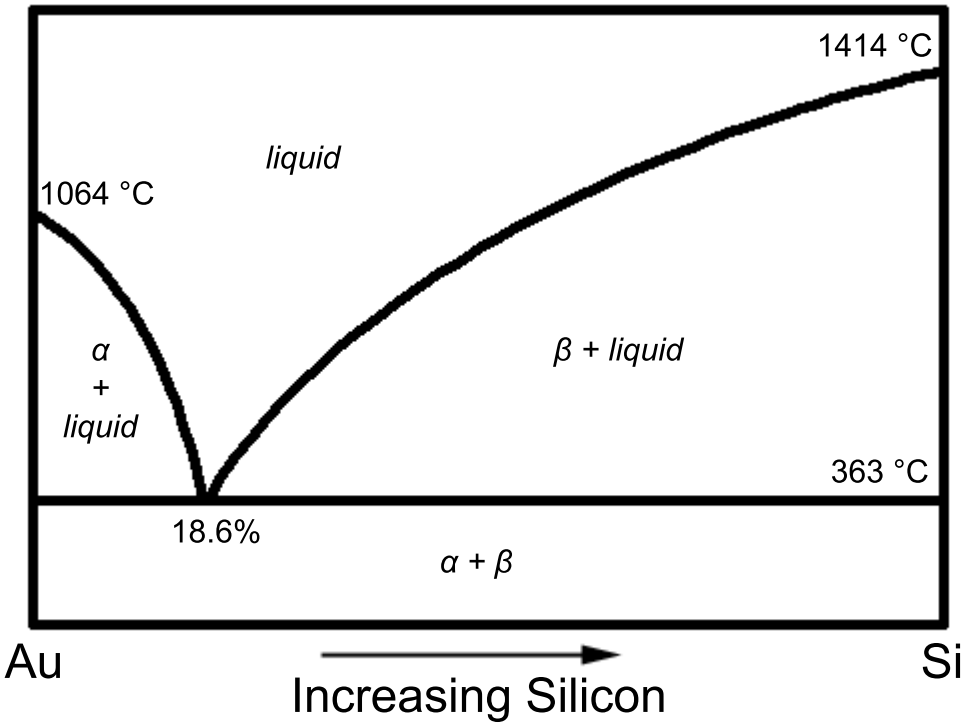

Figure 1–4: Equlibrium Au–Si phase diagram in atomic percent with the relevant temperatures and compositions labeled.

gold silicide intermediate phases [22], which simplifies metallurgical analysis of solidified gold–silicon alloys further. Desirable to gold–silicon research and technology is the significant reduction of gold (1064 °C) and silicon (1414 °C) melting temperatures to the eutectic melting temperature (363 °C) when alloyed. This low eutectic temperature is one of the key advantages of VLS process and a motivation for its integration into microelectronic technologies. Other alloys like aluminum–silicon, silver–silicon, gold–germanium, aluminum–germanium and silver–germanium are analogous [28], but none posses the lack of solid–state solubility, lack of thermodynamically stable intermediate phases and the significant reduction in melting temperature that gold–silicon does. These properties coupled with nobility, malleability and purity of gold have made gold–silicon alloys a relevant and well studied material system.

Many properties of the gold–silicon system can be inferred from the analogous, more rigorously studied aluminum–silicon system, which aids and complements gold–silicon research. While studies on grain refinement, mechanical processing and thermal processing of aluminum–silicon alloys are less useful, as gold–silicon is not a structural material, work on microstructure characterization [29] [30], directional solidification [31] [32] [33], microstructure alteration via micro–alloying additions [34] [35] [36], and primary phase nucleation [37] [38] [39] have been useful when interpreting the gold–silicon microstructures analyzed in this work. Fundamental phenomenon such as rapid solidification/glass formation [40] [41] [42] [43], short–range order in liquids [44] [45] and thin–film surface energetics [46] [47] are often studied using the gold–silicon system because of its favorable qualities, and the ease of

using technologies adopted from semiconductor electronics industry to study these materials.

Gold–silicon interfaces are used as the prototypical interface to study the unique atomic interactions between metals and semiconductors. Metal–induced crystallization (MIC) [48] [49] [50] [51] is a commercially adopted technique to produce high–quality, large grain polycrystalline silicon thin–films which takes advantage of a unique semiconductor–metal interface phenomenon. The MIC process utilizes the ability of silicon to diffuse through gold and other metal layers, normally via grain boundary diffusion [52] [53] [54] [55], at room temperature to a free surface on the other side of the metal (Figure 1–5). When this diffusion occurs through the gold and other metal layers in vacuum, the silicon forms a polycrystalline silicon film which isolates the metal layer from the free surface. This polycrystalline film can be engineered to have a large grain structure and is useful for integrating silicon films fabricated in this method into CMOS processes. When this diffusion occurs through gold and other metal layers in atmosphere, the silicon at the surface will react with oxygen and form a silicon oxide film [56] [57] [58] [59], potentially microns thick, which isolates the metal layer from the atmosphere. The formation of silicon oxide at gold–atmosphere interfaces has been observed in this work for micro–crucible grown silicon which had been exposed to atmosphere after the growth step.

From a technological standpoint, gold is not used in commercial MIC processes due to the detrimental effect it has on electron mobility in silicon, and aluminum is normally used instead. Eutectic bonding is a commercial technology which takes advantage of the the gold–silicon system [60] [61] [62]. Because of the lower eutectic

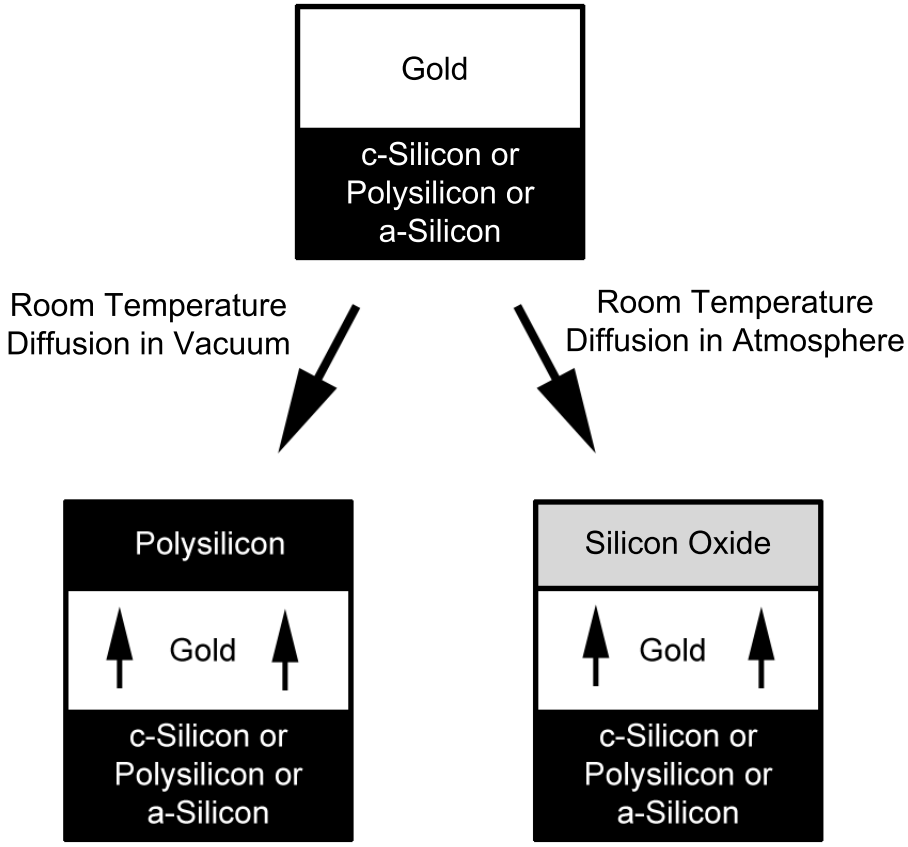

Figure 1–5: Gold–silicon interface where a single crystal of silicon film (c-Silicon), a polycrystalline silicon film (Polysilicon) or a amorphous silicon film (a-Silicon) has diffused across a gold thin–film to the free surface at room temperature. In vacuum, the diffused silicon forms a polycrystalline silicon film at the free surface, on top of the gold film. In atmoshpere, the diffused silicon forms a silicon oxide film at the free surface, on top of the gold film.

temperature of gold–silicon, which is attractive for thermal budget management of integrated circuits, eutectic bonding of gold and silicon thin–films is used when two substrates need to be bonded together, typically for microelectromechanical systems (MEMS) and flip–chips. Also relevant to gold–silicon technology are the nanostructures grown by the vapor–liquid–solid method with gold–silicon catalyst. While not fully commercialized, precision control of nanowires remains a goal for the international technology roadmap for semiconductors, and gold–silicon the research is the foundation on which nanowires are understood.

1.2 Vapor–Liquid–Solid Nanowires

Fundamental to this work is the pioneering research on the vapor–liquid–solid growth done by Wagner and Ellis [13] at Bell Labs in 1964. Their work [63] [64] [65] is the most analogous and comprehensive study on VLS growth using gold–silicon systems which are not at the nano–scale. The most useful reference on understanding and controlling micro–scale VLS growth, which is what occurs when silicon is grown in micro–crucibles, is Wagner's chapter in A. P. Levitt's *Whisker Technology* [66] published in 1970. The contribution sums up the earlier published results of Wagner, as well as demonstrates common defects associated with the growth mechanism and their root causes. The majority of the work by Wagner and Ellis quantified and qualified silicon wires grown using a gold catalyst from silicon {1 1 1} substrates, although Ellis went on to do the some of the initial work on III–V VLS growth [67], which did not mature as a field to the level of the original silicon VLS work until the 1990s [68] [69].

Figure 1–6 describes the basic growth mechanics observed during the initial VLS experiments. Figure 1–6A is of a silicon {1 1 1} wafer which has been cleaned of all native silicon oxide, after which some gold has been patterned on top by any number of deposition techniques, including: electron beam induced deposition [70], effusion cell evaporation [71] [72] [73], thermal evaporation [74] [75] [76], gold nanoparticle colloid deposition [77] [78] [79] [80] [81] [82], ion implantation [83], plasma sputtering [84] [85], and electron beam evaporation [86]. The patterned gold on the oxide–free silicon {1 1 1} substrate is heated to gold–silicon eutectic temperature, at which the silicon substrate and pattered gold liquefy, forming a gold–silicon liquid alloy

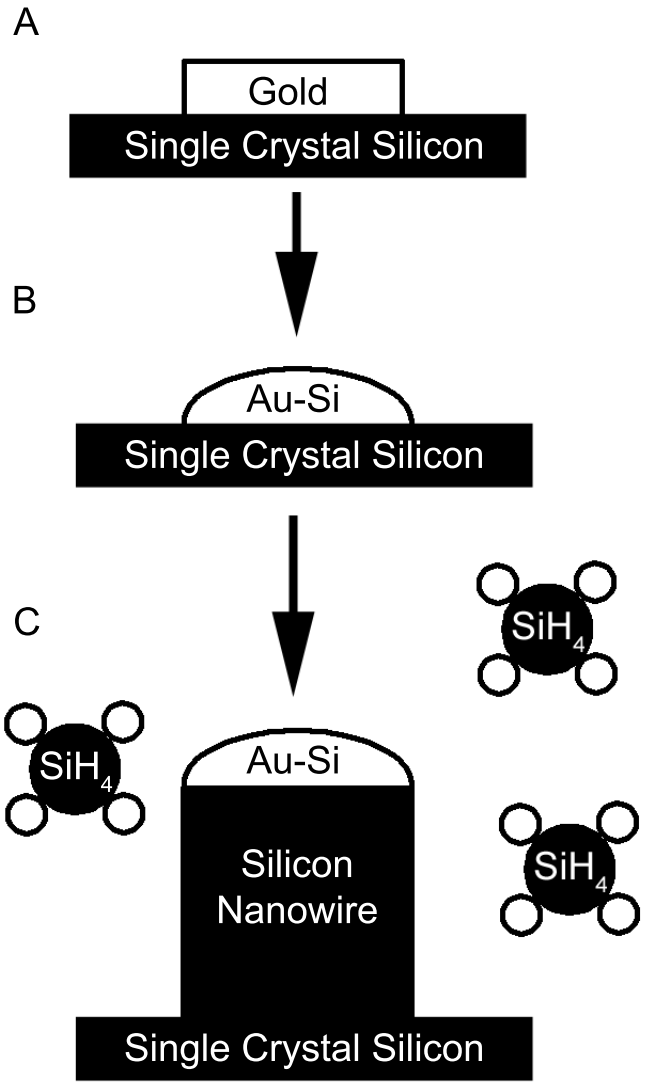

Figure 1–6: (A) A Si {1 1 1} wafer which has had its native oxide layer removed and a thin Au film deposited on to its surface. (B) The Si wafer has been heated above the Au–Si eutectic temperature and the Au film has formed a liquid Au–Si alloy with Si dissolved from the substrate. (C) A gaseous Si precursor (SiH_4) has been introduced to the wafer, which preferentially cracks at the gold–vapor interface and deposits Si atoms into the Au–Si alloy. The alloy supersaturates and deposits the excess Si atoms on the silicon wafer on which it sits. A highly crystalline Si wire grows from underneath the Au–Si alloy as more Si is deposited into the Au–Si alloy.

as depicted in Figure 1–6B. The liquid gold–silicon alloy takes the composition for which it is in thermodynamic equilibrium for a given temperature, and the substrate is etched back slightly to provide silicon for the liquid alloy. A gaseous silicon precursor, typically silane (SiH_4) for modern studies but in the original work it was silicon tetrachloride ($SiCl_4$), is introduced to the liquid gold–silicon alloy through a CVD process, as depicted in Figure 1–5C, and the silicon precursor preferentially cracks at the liquid alloy surface, dissolving the gaseous silicon into the liquid gold–silicon. The increase in concentration in the liquid gold–silicon is not in equilibrium with the processing conditions, and it is thermodynamically favorable for the supersaturated gold–silicon alloy to reject its excess silicon. This rejected silicon finds its lowest energy configuration at the crystalline silicon surface on which the gold–silicon alloy rests, and redeposits itself there in a manner which is highly ordered and free of dislocation defects. Because the deposited silicon starts in the vapor phase, transforms into a liquid intermediate and is incorporated into a highly crystalline solid, the vapor–liquid–solid method was given its appropriate name. Silicon is continuously deposited at the liquid–solid interface of the alloy and the crystal as long as the CVD process continues, and a wire–like crystal grows up from the substrate in a one–dimensional fashion with a hemispherical metal catalyst at its tip, because the surface tension between the alloy and the crystals does not allow the allow the metal catalyst to wet the surface. Interesting to note is the difference between the initial VLS studies and the more modern ones, where the choice in gaseous precursor not only effects the temperatures at which the VLS process takes place, but the residual

products of the gas decomposition reactions, such as HCl and Cl_2 for $SiCl_4$, appeared to have etched VLS catalysts [87] [88] during the CVD process.

The initial VLS research also noted that metal catalyst other than gold could be used [13], but much of the following VLS work continued to use gold as the predominate catalyst, as it has a very large processing temperature range at which controllable VLS growth will occur, in addition to the other desirable characteristics mentioned in Section 1.1. The other catalysts known to successfully grow silicon wires using the VLS technique have been reported as follows: platinum [89] [13] [90], palladium [91] [13] [90], silver [91] [89] [13], aluminum [88] [92] [93], nickel [94] [89] [90], iron [14] [63], copper [91] [89], gallium [87] [95] [88], indium [87] [96] [97], and tin [97]. Interesting for gallium, indium, and tin, which have low melting points and would appear to be ideal candidates for low temperature VLS growth, is that they are reported to be dependent on the experimental CVD conditions for successful growth [91] [71]. In the case of indium, silicon nanowires have been grown successfully at 900 °C - 1050 °C using $SiCl_4$ [87], and with plasma–enhanced chemical vapor deposition (PECVD) assisted growth at 300 °C - 500 °C using SiH_4 [97] [96] [98], but unsuccessful using $SiCl_4$ at 800 °C [91] and at 550 °C using physical vapor deposition of silicon [71]. Gallium, indium, and tin all share a particular phase diagram type with silicon [99] [100] [101], where the eutectic composition of the respective alloys is very close to pure gallium, indium and tin. With no reasonable concentration range where both silicon and the respective low melting temperature solvents are fully miscible in the liquid phase, it is entirely possible that the vapor–liquid–solid transformations cannot occur at sufficiently low temperatures for these

catalysts, and VLS growth needs to occur at temperatures where both species are miscible in the liquid phase for a sufficiently large concentration range, as observed with the indium used in gallium arsenide [102] and germanium [103] nanowire growth at 500 °C - 550 °C.

Following the initial observations by Wagner and Ellis, silicon wire/nanowire growth proved to be a useful research platform for fundamental growth phenomenon and one–dimensional electronic properties. The first questions asked after the initial work were on the mechanics of mass transfer [91] [104]. Givargizov [90] in 1975 observed a diameter dependence on the growth rates of nanowires, which was attributed to the Gibbs–Thomson effect, and described the mass transfer of the VLS process in four steps: (1) Mass–transport in the gas phase, (2) Chemical reaction on the vapor–liquid interface, (3) Diffusion into the liquid, and (4) Incorporation of the material in a crystal lattice, thus defining the widely believed, fundamental mass transfer steps for the VLS method. Of these steps, Givargizov stated that (2) and (4) were the potential growth limiting steps and concluded that the incorporation of the material into the crystalline lattice was the mass transfer limiting step. It was not until 2006 when Kodambaka [73], observing *in situ* silicon nanowire growth using transmission electron microscopy (TEM) that the VLS theories of Givargizov were disproven, and that the silicon nanowire growth rates were not dependent on the diameter of the silicon nanowire, but only the dissociative adsorption of the silicon precursor at the catalyst surface determined nanowire growth rates. For a long time after the reports on mass transfer in the VLS system in the early 1970s, vapor–liquid–solid research

was largely not explored further until Lieber [105] [106] [107] [108] started to advocate for the integration nanowires into micro–electronics. After the realization that the VLS technique was a key enabler of nanoscience, an explosion of high–quality research on the silicon VLS growth has since been publish, particularly in the fields of silicon growth on a crystalline surface from a supersaturated metallic droplet [109] [95] [110] [111] [112], preferred growth direction of nanowires [113] [107] [106], incubation time/critical supersaturation required to nucleate a silicon crystal in a metallic droplet [114] [110] [115], undercooling observed in gold–silicon alloy droplets [116], integrating nanowires into transistors [80] [74] [108], and integrating nanowires into photvoltaics [117] [98]. Readers interested in learning more about the state of the art in nanowire technology are directed to reviews by Ross [118], Schmidt [119], and Dick [120].

1.3 Bridgman–Stockbarger Growth

It was originally thought that the Bridgman–Stockbarger technique [9] [10] would have many analogs to lateral growth of semiconducting films within micro–crucibles. Unfortunately the principle engineering parameter used to enable Bridgman–Stockbarger growth, controlled thermal gradients over the length of the crucible [121] [122], was not applicable to the micro–crucible structure due to the inability to engineer thermal gradients at the micro–scale. Other Bridgman–Stockbarger growth techniques like magnetic mixing of the melt [123] [124] and engineered dewetting of the melt from the crucible [125] could be applied to growth within micro–crucibles, but not with the current state of understanding of the phenomenon or equipment. Of the considerations taken from Bridgman–Stockbarger growth was the design of seedless crucibles to promote nucleation at particular location in the crucible [126] and the integration of a necked region, which is designed to prohibit defects such as dislocations from propagating across the grown crystal, and which promotes the growth of a single crystal. Examples of experimental crucibles shapes used are given in Figure 1–7.

Although they cannot be engineered, the thermal gradients defining the Bridgman growth technique are analogous to the chemical gradients believed to be present during VLS growth in micro–crucibles. Because the gaseous silicon precursor must react at the gold–vapor interface, like it must in VLS nanowire growth, and the solutionized silicon in the gold–silicon liquid will be driven to diffuse from the high concentration at the gold–vapor interface towards the rear of the micro–crucible,

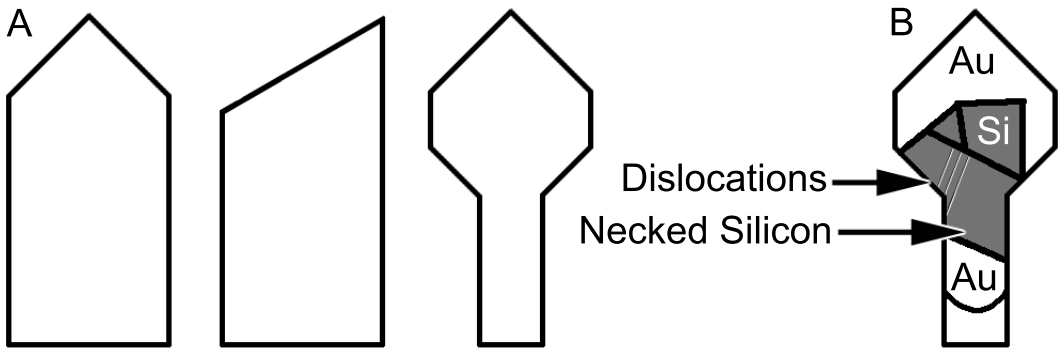

Figure 1–7: Plan–view depictions of some of the micro–crucible designs for this work. Figure 1–7B depicts one of the designs which has necked out polycrysalline growth and dislocations.

which is not true for epitaxial, VLS nanowire grow as the catalyst is already pre–saturated with silicon from the substrate, a concentration gradient develops across the gold–silicon alloy confined within the micro–crucible during the initial stages of VLS growth. The dynamics of this concentration gradient have been touched upon by Kalache [114] and will be further explained in Section 3.3.5, but much like the thermal gradient controls where the initial seed will nucleate in seedless Bridgman–Stockbarger growth, concentration gradients across the gold–silicon alloy in the micro–crucibles determine where the initial nucleation event will occur within the crucible. Concentration gradients and diffusion profiles, which are believed to occur in micro–crucibles during a CVD process, are not well studied in the nanowire or Bridgman growth research, and the solid–vapor mass transfer literature of fluidized bed reactors [127] may prove to be a better source of information and guidance for studying this phenomenon.

1.4 Epitaxial Layer Overgrowth

Like VLS grown silicon nanowires, epitaxial layer overgrowth is a technique which was established in the 1960s [11], but did receive deeper investigation until the early 1980s [128]. Unlike VLS nanowire research, ELO research did not experience a renewal upon its rediscovery, but rather has maintained a constant research effort since, and has been applied commercially [129] to engineer lower cost germanium and III–V substrates. ELO is a versatile research technique which can utilize vapor phase epitaxy [130], molecular beam epitaxy [131] or liquid phase epitaxy (LPE)[132] and which has been used to engineer high–quality semiconductor crystals. Of primary concern to lateral growth within amorphous micro–crucibles is ELO as a proof of concept. High–quality single crystals of silicon, germanium and III–V semiconductors can be grown laterally without dislocation defects over amorphous oxides using ELO, thus high–quality semiconducting crystals can be grown over amorphous oxides within micro–crucibles without dislocation defects using the VLS technique. This theory was initially tested using seeded, laterally grown nanowires[133] [134] [79] and resulted in high–quality interfaces between the VLS grown crystals and the silicon oxide substrates.

Figure 1–8 depicts a typical setup for ELO growth. A crystalline silicon wafer is thermal oxidized producing a high–quality amorphous silicon oxide at the surface of the silicon crystal. Windows are etched into the silicon oxide (Figure 1–8A) exposing a selected area of the silicon crystal and allowing selective area deposition to occur there. The thermally oxidized silicon wafer with etched regions is exposed to a VPE, MBE or LPE growth process, or a combination of the processes [12], and a dissimilar

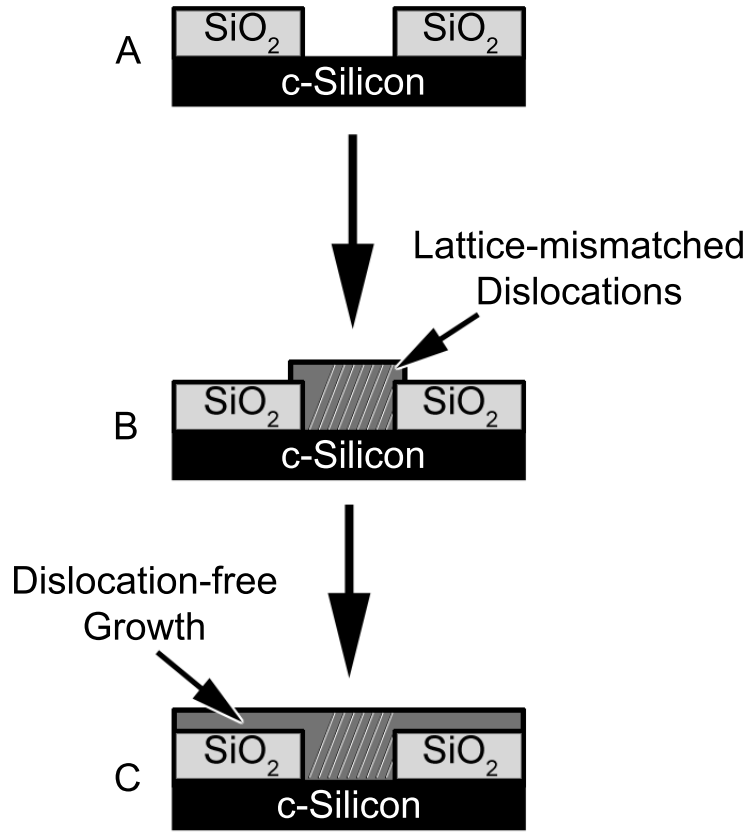

Figure 1–8: (A) A silicon substrate which has been selectively masked with a thermal oxide. (B) The initial epitaxial growth nucleates where the silicon oxide mask has been selectively etch. The initial growth has dislocations which start at the interface of the silicon substrate and the dissimilar semiconducting film growing on top of it. (C) The dissimilar semiconducting grows laterally over the silicon oxide with the dislocations concentrated in the interfacial regions of the silicon substrate and the dissimilar semiconducting film.

semiconducting material is selectively, epitaxially grown at the exposed regions of the silicon crystal (Figure 1–8B). Misfit dislocations propagate from the interface of the heterstructure due to the lattice mismatch of the two dissimilar semiconducting materials and the need for the stain energy at the interface to be relieved. If the silicon oxide is thick enough, the lattice–mismatched dislocations can be necked out, functioning much like the necks used in Bridgman–Stockbarger growth. Upon growing out of the oxide windows, the dissimilar semiconducting material will grow over the silicon oxide masking layer, which can be as two–dimensional growth, as imaged in Figure 1–8C, or as three–dimensional growth depending on the material system used and the experimental conditions. The semiconducting material which has grown over the amorphous silicon oxide tends to be free of dislocations and can be integrated into semiconducting devices requiring high–quality crystalline material.

1.5 Confined Lateral Growth

Confined lateral growth is a recent evolution of high–quality semiconductor growth techniques which reflects demands in microelectronics for the on–chip integration of nanotechnology and optoelectronics. To achieve this goal, chemical vapor deposition, vapor–liquid–solid and crystallization research has been combined in creative ways to produce semiconducting thin–films using amorphous, confining templates to control the morphology of the growth. The first confined lateral growth experiment reported was by Shan [16], where nanowire–like crystals, which were named nanoribbons, were grown laterally by depositing gold patterns over a thermally oxidized substrate, encapsulating the pattern with PECVD silicon nitride, and selective etching out the gold from the encapsulated structures using potassium iodide based gold wet etchant. The gold films used an adhesion layer of 1.5 nanometers of titanium and were 20 nanometers thick. The resulting silicon films were grown at 500 °C in a low-pressure chemical vapor deposition (LPCVD) reactor. Shan found that there was a limit to how far the silicon dissolved into the liquid would diffuse from the initial gold–vapor interface before a silicon crystal would nucleate.

After the initial work of Shan, Lew reported on the activation energy associated with VLS silicon nanowire growth, the mechanics of vapor–phase diffusion of the gaseous semiconductor precursor in confined templates [15], and the crystalline quality [135] of silicon nanowires grown within porous, amorphous aluminum oxide templates. Using work rooted in chemical process engineering [136] [137], it was found for sufficiently low pressures(i.e. LPCVD processing pressures) sufficiently low temperatures(which for diffusing SiH_4 was calculated to be 500 °C), pores on the

order of $3 \times 10^{-2}\,\mu m^2$, and diffusion distances of 25 microns, that there would be no parasitic reactions of the precursor on the inner surface of the amorphous pore, and thus the concentrations at the mouth of the pore and at gold–vapor interface are the same. Buttard [138] [139] followed up on the work of Lew by confirming the activation energy calculation and the vapor–phase diffusion model with similar work, but used gold nanoparticles in addition to electrolytic deposition to controllably deposited a gold catalyst within the aluminum oxide pores.

The first report on two–dimensional semiconducting materials using the confined VLS technique was reported by Lecestre [140] [141] in 2009. In this work, silicon nanoribbons were grown laterally over thermally grown oxide with an encapsulation layer of PECVD silicon oxide. The gold layers (50 nanometers) were deposited on the silicon oxide without the aid of adhesion layer using a lift–off technique, and germanium thin–films in addition to the gold were used to defined the geometry of the amorphous template. The germanium was removed sacrificially using H_2O_2 prior to CVD growth, which was conducted in a LPCVD reactor at 500 °C. Electron backscatter diffraction (EBSD) was used to qualify the crystallinity of the nanoribbons grown, most of which were polycrystalline and did not fill the entire volume of the amorphous template. The nanoribbons were fabricated into thin–film transistors and their electron mobilities were found to be around $50\,cm^2/Vs$. The diffusion limit of silicon into the gold catalyst is clearly visible in the published electron micrographs, and reported silicon nucleation events occurred less than 200 nanometers from the initial gold–vapor interface.

The most successful reporting of using the VLS technique to grow high–quality silicon crystals inside of amorphous confined templates was published by Pevzar [142] in 2011. The work outlined the process of growing confined silicon and germanium nanowires in arbitrary morphologies over thermally grown silicon oxide as well as kapton tape. Titanium (1.5 nanometers) was used as an adhesion layer, the gold was deposited 50 nanometers thick, and the PECVD silicon oxide encapsulation layer was deposited with an inductively coupled plasma PECVD system. Growth took place in a LPCVD reactor at temperatures between 420 °C and 460 °C. The nanowire quality was analyzed using EBSD, where nanowires with 90 degree kinked morphologies appeared to still have the same Kichuchi diffraction pattern across the whole of their growth. The I–V characteristics of the of the kinked sections of the nanowires appear to have lower electron mobilities than the straight sections, but there are no details on how a PN junction was formed using the nanowires in the report. Pevzar, like Shan and Lecestre, also reported a maximum diffusion distance from initial gold–silicon interface at which the crystalline silicon phase is formed.

Techniques not using the VLS method to laterally grow semiconducting crystals within confined geometries have most recently been reported. McComber [143] encapsulated an amorphous silicon seed in an amorphous oxide template to seed germanium growth at 450 °C for 4 to 16 hours using conventional CVD. The germanium nucleated preferentially at the amorphous silicon seed and grew laterally as a polycrystal. It was believed that eventually the quick growth direction would come to occupy the complete volume of the template, as the slower growth directions would be overgrown by the faster, but the reported amorphous oxide templates were

not fabricated long enough and a growth dominated by fast–growth crystals was not demonstrated. Leung [144], building off the work of McComber, has reported work in which GaN thin–films were seeded from pre–deposited AlN encapsulated in a amorphous oxide template. To further engineer the growth, necks were incorporated into the templates to more quickly select the fast–growth crystal, effectively making growth beyond the neck single crysalline. Growth was conducted in a metal–organic LPCVD reactor at temperature between 900 °C and 1070 °C. The crystalline quality of the growth was analyzed with EBSD and focused ion beam (FIB) TEM cross sections.

Lateral crystallization of thin–films, which does not use CVD or MBE reactors for growth, has been reported [145] [146] and is a potential enabling technology for large area, high–quality semiconducting materials. Titled lateral liquid–phase epitaxy by its inventors, this research uses germanium stripes, upwards of 2 microns wide and 100 nanometers thick, patterned over a thermal oxide which has had a small window etched at the end of the stripe, at which the germanium contacts the crystalline substrate. The stripe is completely encapsulated in a PECVD amorphous oxide and is subjected to a rapid thermal anneal of 1000 °C for one second. In this second, the germanium is liquefied and quickly recrystallizes using the window to the crystalline substrate as the initial nucleation site, at which the solid–liquid interface propagates laterally over the amorphous oxide. The resulting single crystal is similar to ELO grown crystals, as mismatch dislocations from the germanium–silicon interface are necked out as the germanium crystal grows laterally.

The lateral growth of silicon thin–films in micro–crucibles using the VLS technique differentiates itself from the previous confined lateral growth work in a number of ways. When compared to the previously reported lateral growth techniques using the VLS method [16] [142] [140], the work reported here is on a two–dimensional scale and enables the growth of silicon films with significantly larger surface areas. It also incorporates new design features such as the crucible neck and attempts to control the initial nucleation site of the silicon crystal within the confined geometry. As to the published lateral growth in confined templates which use conventional CVD [143] [144], growth in micro–crucibles using the VLS method occurs at much lower temperatures for a wider classes of semiconducting materials, thus keeping VLS growth within the thermal budget for a larger number of microelectronics and making the VLS technique the more versatile. Lateral recrystallization [145] [146], like ELO, requires a crystalline substrate to seed high–quality films, whereas inexpensive, amorphous substrates such as glass are compatible with micro–crucible technology.

1.6 Electron Beam Analysis

Throughout the work presented here, the principle tool for analyzing lateral film growth with micro–crucibles using the VLS technique has been electron beam analysis in the forms of scanning electron microscopy (SEM), transmission electron microscopy (TEM), energy-dispersive x–ray spectroscopy (EDS), electron backscatter diffraction (EBSD), or transmission electron forward scatter diffraction (t–EFSD). Scanning electron microscopy was the workhorse of this research and hundreds of individuals micro–crucibles were imaged so that silicon crystal growth could be measured, the microstructures of the solidified gold–silicon could be analyzed, and the general growth condition inside the micro–crucible could be interpreted. One particular applications of the SEM in this work was backscatter imaging, which was used to identify the gold and silicon phases. Because there are no intermediate phases in the gold–silicon system and almost no solid–state solubility of gold in silicon or silicon in gold, backscatter images of gold–silicon micro-structures should have well define phase separation, and limited gray regions when imaged using a backscatter detector. It was found however that there were gray areas (Figure 1–9) in the microstructure and a straightforward investigation with the EDS detector available in the SEM revealed that this potential third phase showed characteristic x–ray peaks associated with both silicon and gold.

Transmission electron microscopy aided in qualifying and quantifying process parameters and growth conditions which could only be inferred from SEM results, particularly with regards to adhesion layers and their effect on silicon nucleation withing the micro–crucible. Adhesion layers and their effect on lateral growth in

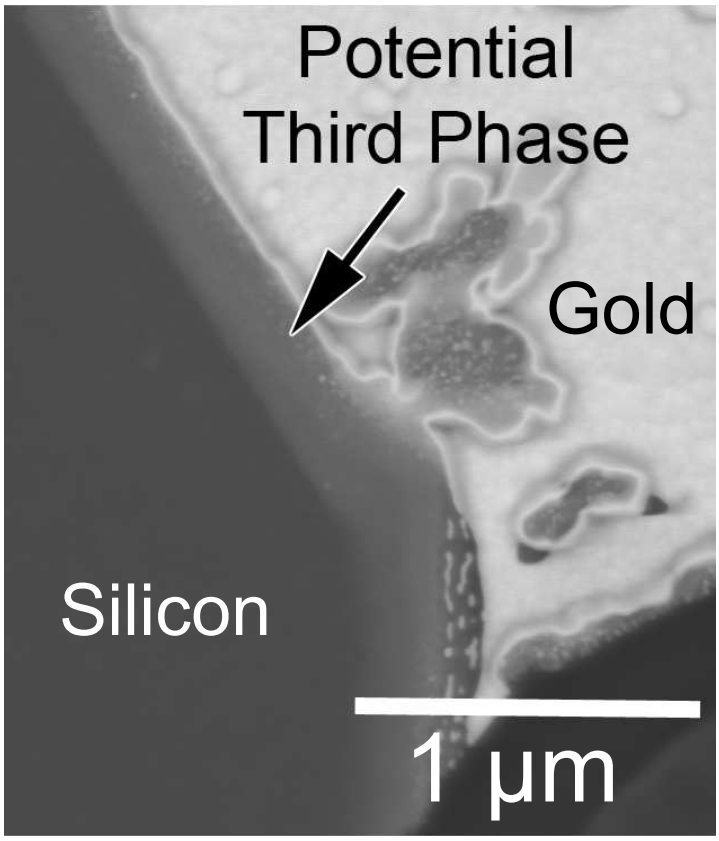

Figure 1–9: Observed gray area and potential third phase in a micro–crucible at the interface of the facet crystal and lamellar gold–silicon phases.

micro–crucibles composes a large amount of the original research presented in this work (see Sections 3.1 and 3.3). EDS was an invaluable addition to TEM analysis as the chemical signatures from the adhesion layers used in this experiment were not strong enough to produce reliable signals in SEM analysis, and developing techniques for preparing micro–crucibles on TEM grids for plan–view observations advanced the state of the research significantly.

Figure 1–10 is of a micro–crucible prior to growth which has been imaged with a scanning TEM (STEM) using high–angle annular dark–field (HAADF) imaging. Using a STEM with HAADF capability allowed for an EDS map over a select area of the micro–crucible, which is represented by the square box in Figure 1–10A. Prior to STEM analysis, it was not known if the adhesion layer, chromium, used for this particular micro–crucible was present or not after fabrication. This was not able to be determined using EDS in a SEM as the 150 nanometers of gold and 5 nanometers of chromium used for the experiment required acceleration voltages of less than 5 keV to be used so as to collect x–rays from the surface. At such low voltages, chromium characteristic x–ray peaks overlapped with the characteristic peaks of oxygen and the presence of chromium could not be discerned reliably. Gold and chromium characteristic x–rays were relatively easy to collect and identify once the micro–crucible was prepared for TEM examination and Figure 1–10C clearly shows that chromium is present and concentrated down the center of the micro–crucible after fabrication.

More traditional uses of transmission electron microscopy were also employed in this research to determine the crystalline quality and orientation relationships

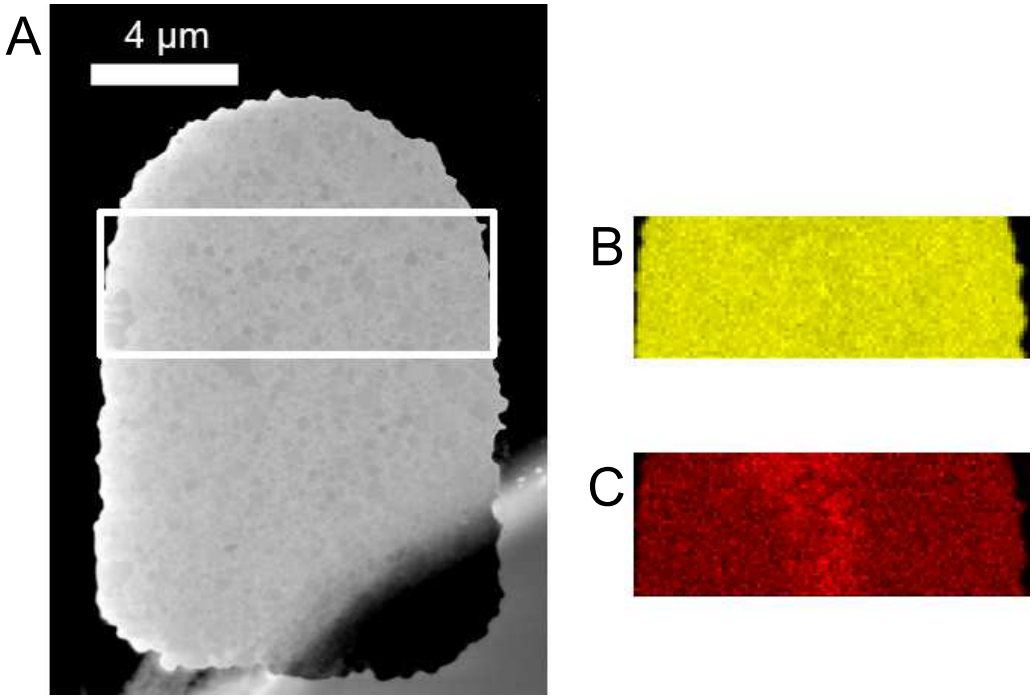

Figure 1–10: (A) A HAADF image of a micro–crucible prior to the CVD step. (B) An EDS map of Au. (C) An EDS map of Cr showing that it is concentrated in the center of the crucible.

of silicon growth within micro–crucibles. Bright–field imaging and selective area electron diffraction (SAED) in the two–beam condition were used to determine the crystalline quality of the grown silicon and to determine if dislocations were present in the growth, which they were not. High–resolution transmission electron microscopy (HRTEM) was used at grain boundaries and gold–silicon interface to determine the orientation relationship neighboring grains shared, and to observe if any stacking faults were present at the boundaries. Figure 1–11 is an example of the bright–field, SAED, and HRTEM used to analyze silicon growth in this work. Because of the unique TEM sample preparation method (Section 2.2.7) used on silicon wafers with micro–crucibles, hundreds of square microns are electron transparent, allowing for entire micro–crucibles to be imaged at once, as shown in Figure 1–11A. Figure 1–11B points to a potential twin boundary observable in the bright–field image and a region which could be related to the marked in Figure 1–9. A close–up of the potential third phase in Figure 1–11C shows that the gray area in the SEM micrographs is a two phase region with a dispersion of particulates which are smaller than 10 nanometers when viewed in a TEM. The HRTEM image in Figure 1–11D is of the potential twin grain boundary and shows that the atomic planes of the grains run parallel to each other. The SAED pattern of the HRTEM image area 1–11E shows the characteristic double diffraction pattern of twin boundaries, thus giving strong evidence that these two grains are twinned.

The other two electron beam techniques mentioned, EBSD or t–EFSD, are modern techniques and active areas of research. EBSD is especially powerful at determining preferred orientation of textured film, as well as the orientation relationships

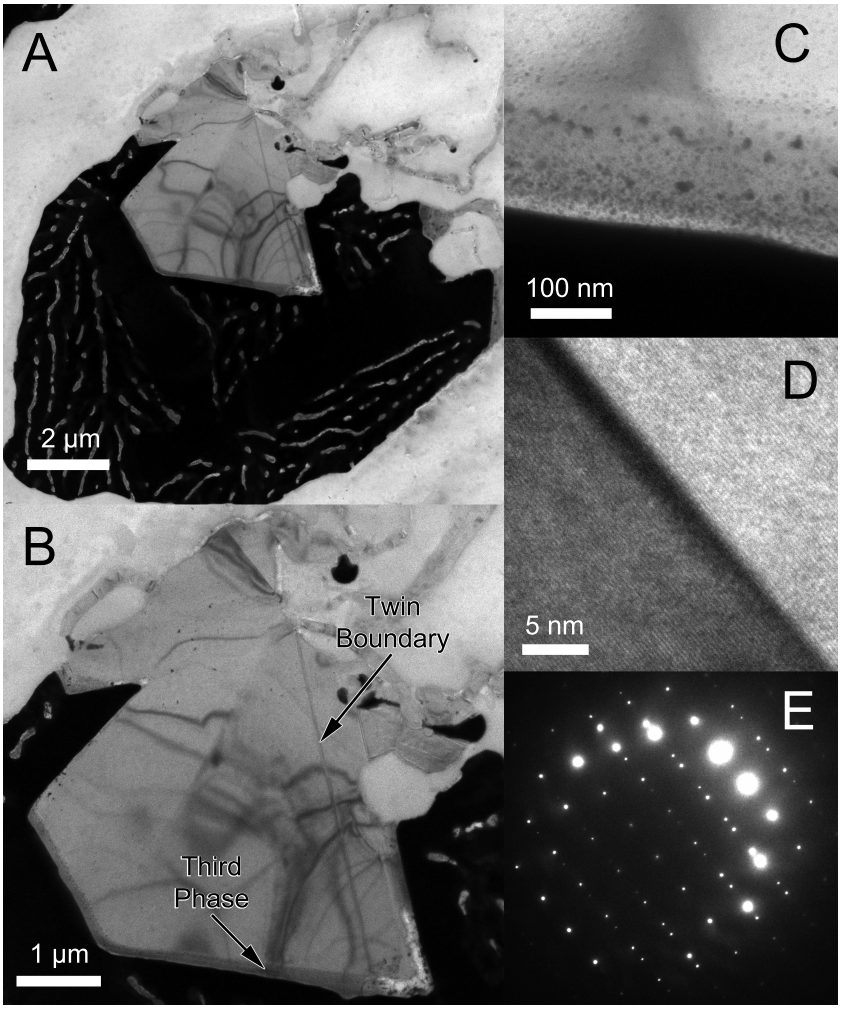

Figure 1–11: A set of progressive TEM images analyzing a micro–crucible which has nucleated a twinned crystal. Figure 1–11A is a image of the whole micro–crucible. Figure 1–11B is magnified image of the faceted crystal. Figure 1–11C is a high magnification image of the interface between facet crystal and lamellar gold–silicon phases. This interface is believed to be the same imaged with a SEM in Figure 1–9. Figure 1–11D is a HRTEM image of the twin boundary between two neighboring grains and Figure 1–11E is the SAED pattern of the twin boundary.

between a large numbers of grains. Its power lies in that it lends itself to statistical analysis. Transmission electron forward scatter diffraction is a recently invented derivative of EBSD analysis which takes advantages of a scanning electron microscope operating in transmission electron mode. Transmission electron operations in a SEM offer much of the same functionality of a STEM, but have the benefit of the ease of use associated with SEMs, and t–EFSD further proves the point that tasks, like orientation analysis for thin–film samples, are more efficiently executed in a SEM than a STEM. Both EBSD or t–EFSD, and their respective literatures will be discussed further.

1.6.1 Electron Backscatter Diffraction

Electron backscatter diffraction is an electron beam technique traditionally associated as a SEM technique which has greatly contributed to grain boundary research. Prior to EBSD, the TEM was the primary tool to study grain boundaries and the orientation relationships shared by neighboring grains, but because it is difficult to observe a large number of grain boundary relationship using TEM analysis, the mathematical models and descriptions of grain boundaries varied from study to study [147] [148] [149]. As EBSD grew and become more widely accepted as a tool for large area grain boundary analysis [150], the literature began to converge on a mathematical description of grain boundary orientation relationships, namely the coincident site lattice (CSL) model [151] [152] [153] [154]. The CSL model, which is a simple geometric model, uses the visual concept of two interpenetrating lattices of different orientations, where the parameter Σ has the value of the reciprocal density of lattice sites which the two interpenetrating lattices hold in common. This sigma

notation has become prevalent in newer grain boundary literature [155] [156] [157], but the fundamental understand of it remains questionable in many studies which use it. While CSL model does not completely describe the nature of the relationship between two grains [158] [159], gain boundary findings using EBSD in this research were described using CSL notation so as to communicate the information as easily and as broadly as possible.

In addition to the grain boundary relationships, EBSD is more well know for determining crystallographic orientation in textured films [160]. EBSD mapping was used extensively with laterally grown silicon films in this research to determine the crystalline quality of the growth and to establish if there was a preferred orientation in which films nucleated in micro–crucibles grow. Other VLS research [142] [141] [161] [162] has used EBSD analysis for similar purposes.

1.6.2 Transmission Electron Forward Scatter Diffraction

Transmission electron imaging in a SEM is essentially a low voltage STEM, and it provides analysis which is comparable to the results of bright–field TEM imaging. Figure 1–12 is a series of images which compare bright–field TEM imaging to transmission electron SEM imaging for the same faceted silicon growth in a micro–crucible. Advantages that the transmission electron SEM imaging over its TEM equivalent are the ability to imagine in secondary electron mode and obtain topographical information from samples (Figure 1–12C), the easier to use / easier to maintain experimental setup of a SEM, and the ability to perform orientation mapping of thin–film samples with significantly less expensive equipment.

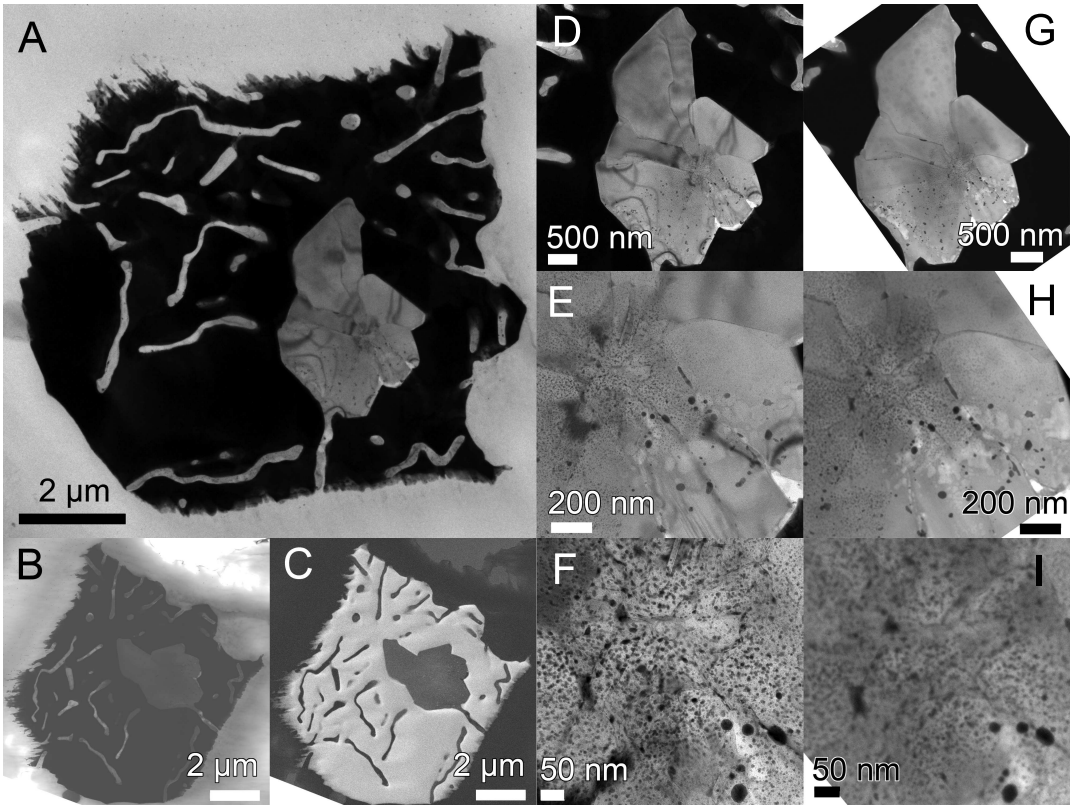

Figure 1–12: Micrographs comparing bright–field imaging in a conventional TEM and transmission electron imaging in a SEM. Figure 1–12A is a TEM bright–field image of micro–crucible with a nucleated faceted crystal. Figures 1–12B and C image the same micro–crucible in 1–12A, but imaged using transmission SEM mode and secondary electron mode respectively. Figures 1–12D through F, and G through I image the same region of the nucleated crystal at progressively higher magnifications, using bright–field imaging TEM imaging and transmission SEM imaging respectively.

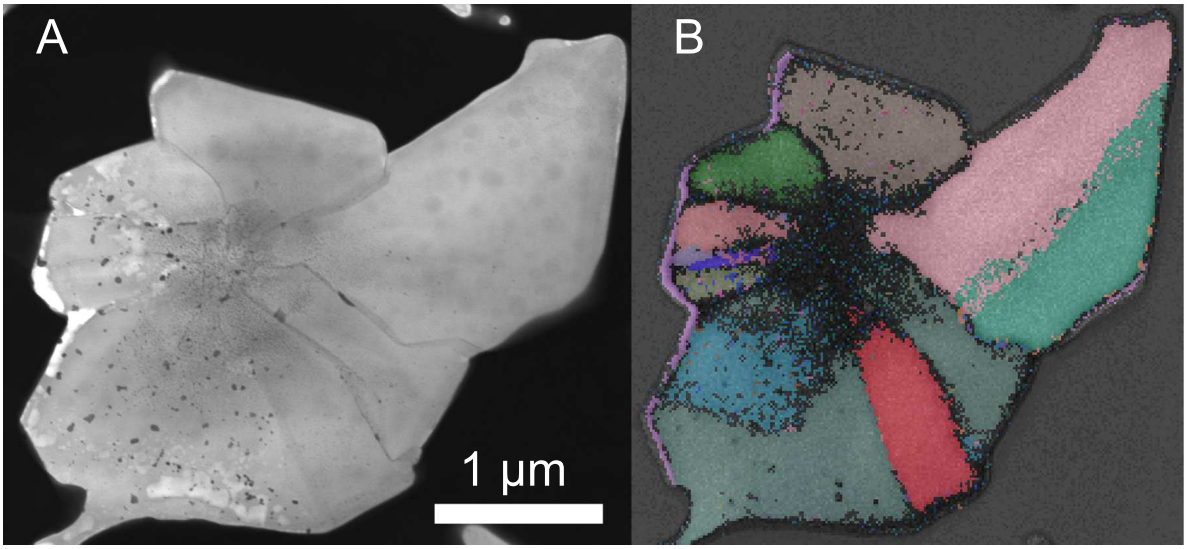

Figure 1–13: The faceted crystal of Figure 1–12 which has been mapped using t-EFSD.

This orientation mapping using transmission electron signals in a SEM is achieved though a currently developing technique called transmission electron forward scatter diffraction [163] [164] [165] [166]. A major limitation of conventional EBSD is the resolution limits of mapped orientations due to the interaction volume backscatter electrons have with tilted samples. To produce the desirable, higher resolution orientation maps, TEMs can be fitted with Kikuchi pattern detecting equipment [167], but at a cost as demand for such equipment is not high. Transmission electron forward scatter diffraction has been found to produce orientation maps with resolutions comparable to TEM maps [164], but uses the fairly common and less expensive EBSD detector and software, thus enabling a new, cost effective method to analyze nanomaterials. Figure 1–13 maps the orientation of the polysilcon crystal imaged in Figure 1–12, where some of the grains are too small for conventional EBSD analysis.

Most useful with regards to implementing t-EFSD into micro–crucible research is the significant amount of time saved identifying the orientation of crystals prepared for TEM analysis, as a STEM with Kikuchi pattern mapping capability is not available for this work, and identification of the multiple SAED patterns needed for polycrystalline samples is time consuming. With t-EFSD, all of the orientation and grain boundary relationships can be collected in a single SEM session, and future TEM sessions can be focused on identifying stack faults and dislocations defects.

CHAPTER 2
Experimental Procedures

2.1 List of Materials

The fabrication process of micro–crucible lateral growth templates takes over thirty unique processing steps to start from a substrate and end with an analyzable, well grown silicon crystal. Here each material used to fabricate micro–crucibles will be described and their function in the process briefly described.

2.1.1 Substrates

Fused silica substrates were the first substrates to be tested, and were also the most difficult to handle. Fused silica is a fully amorphous glass which is composed of only of silicon dioxide. Fused silica substrates proved too difficult to work with due their transparency and lack of cleavage planes, but offer unique advantages not available with silicon substrates. Using transparent substrates causes the topside of the wafer to be ambiguous, especially when working with smaller sections of a wafer which are easily flipped, causing the loss of the topside orientation. While it may seem like a nuisance, not knowing what side of the wafer is being worked upon affects all aspects of the fabrication process and can easily result in costly fabrication missteps. Automated fabrications tools like the Applied Materials Precision Reactive Ion Etcher have difficulties positioning fused silica substrates using its laser detectors, which causes the machine to fault but this issue can be worked around by crystal bonding a fused silica substrate to silicon substrates before insertion into the

tool. Lacking cleavage planes makes sectioning fused silica wafers more difficult and precision cuts of the substrate need to be made on a dicing saw instead of at the workbench with diamond scribe and glass breaking pliers.

Advantages of fused silica substrates are that transparency allows for viewing of the underside of the fabrication layer, which is useful for observing adhesion layer removal in the later–described wet etch definition approach. Owing that they are fully amorphous, fused silica wafers are the only substrates which allow for x-ray diffraction data to be collected from the VLS-grown silicon crystals, because sharp substrate–dependent silicon peaks will be present in diffraction scans of silicon substrates. Fused silica has a low coefficient of thermal expansion, which is an added engineering benefit when trying to minimize encapsulation layer stresses and deformation.

Thermally oxidized silicon substrates are a low cost and versatile substrate. Silicon wafers of any orientation can have conformal, thermally grown, arbitrarily thick oxide deposited by reacting hydrogen and oxygen gases at high temperatures (above 1100 °C) at the wafer surface, known as the wet oxidation process, or just reacting oxygen gas, known as the dry oxidation process. The biggest advantage of thermally oxidized wafers is the large amount of photolithographic literature available for silicon substrates. Photolithography on more exotic substrates does not behave in the same way as silicon wafers and the vendors photolithographic tools and equipment rarely give documentation about their products with substrates other than silicon. This means most processes and recipes need to be customized for substrates other than silicon. Additional advantages of thermally oxidized silicon substrates is their

ease of cleaving and ability to be imaged with a scanning electron microscope without the deposition of conductive layers for sufficiently thin oxide layers (less than one micron).

2.1.2 Photoresists

Shipley 1813 positive photoresist from MicroChem was the primary resist used to define the micro–crucible lateral growth template for the wet etch and undercut fabrication technique. Shipley 1813 was the most robust, simplest to process photoresist used in this work. Being a positive photoresist, Shipley 1813 will only develop in its developer, Microposit MF-319, where the resist had been exposed to ultraviolet radiation. The typical deposition, soft bake, exposure and development of Shipley 1813 was as follows: While spinning at 100 RPM deposited enough Shipley 1813 to cover the substrate, ramp the speed to 500 RPM and maintain for 10 seconds so that the resist uniformly covers the substrate, ramp the speed to 4000 RPM and maintain the speed for 30 seconds to achieve an approximately 1.4 micron uniform film, soft bake the deposited resist at 115 °C for 60 seconds, expose the resist to 60 mJ/cm^2 of ultraviolet radiation and develop the resist in MF-319 for one minute. Shipley 1813 is removed aggressively in acetone and more gently in Microposit Remover 1165. Oxygen plama etching of Shipley 1813 tends to burn the resist at powers over 200 Watts for cleaning times longer than 3 minutes.

AZ 5214-E image reversal photoresist from AZ Electronic Materials was a secondary photoresist used to get the negative photoresist of photomask designs without needing to purchase a second photomask, and the primary resist of the later-described lift–off definition approach. AZ 5214-E was particularly difficult to work

with and the resolution of features when compared to the Shipley 1813 process could not be reliably repeated due to variations in the processing equipment. One major issue encountered was the use of AZ 5214-E which had expired or been contaminated, where features would develop, but the resist would not be fully removed and the bare substrate was not exposed. This issue was resolved by purchasing new bottles of the resist. The typical deposition, soft bake, exposure, reverse bake, flood exposure and development of AZ 5214-E was as follows: While spinning at 100 RPM deposited enough AZ 5214-E to cover the substrate, ramp the speed to 500 RPM and maintain for 10 seconds so that the resist uniformly covers the substrate, ramp the speed to 4000 RPM and maintain the speed for 30 seconds to achieve an approximately 1.4 micron uniform film, soft bake the deposited resist at 110 °C for 60 seconds, expose the resist to 20 mJ/cm^2 of ultraviolet radiation, reverse bake the resist at 120 °C for two minutes, flood expose the reverse baked resist with 280 mJ/cm^2 of ultraviolet radiation and develop the resist in AZ Electronic Materials AZ 726 MIF for one minute. If the features looked underdeveloped under a microscope, the resist was developed for an additional 10-20 seconds. AZ 5214-E is removed aggressively in acetone and more gently in Microposit Remover 1165. Oxygen plasma etching of AZ 5214-E tends to remove it very rapidly and etchs of 200 Watts for 3 minutes can strip the resist.

Lift-off resist 3A (LOR 3A) from MicroChem was experimented with and was successfully used with both Shipley 1813 and AZ 5214-E processes. LOR 3A was not found to be necessary as the structure of the mirco–crucibles was large for

photolithography (tens of microns) and there was not a noticeable difference in the yield for thin metal lift–off.

2.1.3 Thin Metal Films

Gold of 99.99% purity was the catalyst used to promote VLS growth and the sacrificial metal used to define the micro–crucible lateral growth template. Gold was deposited using an electron beam evaporator in vacuums of 5.5×10^{-6} Torr to thicknesses between 50 and 150 nanometers. Electron beam evaporated gold deposits easily as long as there is a critical amount of gold in the crucible. The current to deposit gold at 1 Å/sec was typically between 160 mA and 280 mA. Recently filled crucibles and less diffuse electron beams cause gold to deposit at lower currents. Gold was etched by Transene Gold Etchant TFA or 3:1 35% HCl:70% HNO_3 aqua regia solutions. Gold is a deep–level electronic defect in silicon semiconductors.

Titanium was the first adhesion layer used in the experiments and the most difficult to remove. Gold will not adhere to silicon oxide or silicon nitride surfaces and adhesion promoters are needed to fabricate gold structures on the amorphous materials. Titanium was deposited using an electron beam evaporator in vacuums of 5.5×10^{-6} Torr and successfully used as an adhesion layer with thicknesses as low as 1 nanometer. Electron beam evaporated titanium deposits easily are rates of 1 Å/sec with 50 mA of current.

An issue with titanium as an adhesion promoter is that it is etched by H_2O_2:H_2SO_4 piranha solution, which is used to clean the wafers prior to encapsulation, and causes the gold structures it is adhering to the surface of the substrate to lift–off. More importantly regarding the etching of titanium is that titanium oxides are not soluble in

piranha solution. These oxide residues litter the surface of the gold structures when placed in piranha solution and make reliable VLS growth impossible. Titanium and its oxides have been successfully removed using a Cl_2:Ar physical plasma etch, but it was very aggressive and sputtered away both the protective photoresist and some of the gold structure as well. Titanium is not a deep–level electronic defect in silicon semiconductors.

Chromium was the easiest adhesion promoter to remove due to the selectivity of its etchants and the ease of its oxide removal. Chromium was deposited using an electron beam evaporator in vacuums of 5.5×10^{-6} Torr and successfully used as an adhesion layer with thicknesses as low as 1 nanometer. Electron beam evaporated Chromium is difficult to deposit because it prefers to sublimate at high vacuums and causes the pressure in the electron beam evaporator to spike uncontrollably. Chromium must be evaporated manually and the power must be increased very slowly. There is a large initial spike in the pressure when the electron beam first hits the metal and crucibles with large surface areas of chromium often fall out of high vacuum when initially heated. Once stabilized chromium begins to sublimate at 1 Å/sec at currents around 60 mA, but upon sublimation the pressure oscillates rapidly up and down for about the first 30 seconds, after which the rate and pressure are stable and the deposition reliable.

In addition to use as an adhesion promoter, chromium also seconds as a etch mask due to good corrosion resistance against most dry and wet etches. For these experiments there was an option to use chromium as the mask for the etch which selective removes the micro–crucible encapsulation layer. Chromium was easily etched

using Transene Chromium Etchant 1020 at room temperature if freshly deposited, and slowly if exposed to plasmas prior to the etch [168]. Chromium is a deep–level electronic defect in silicon semiconductors.

Aluminum was an alternative adhesion promoter which has good solid state solubility with gold at low temperatures and similar performance as a VLS catalyst. Aluminum was deposited using an electron beam evaporator in vacuums of 5.5×10^{-6} Torr and successfully used as an adhesion layer with thicknesses as low as 1 nanometer. Aluminum is moderately difficult to deposit because of the high temperate required for its evaporation and the rate at which it evaporates. Aluminum needs to be deposited manually for nanometer thick films and will deposit at a rate of 2 Å/sec at 320 mA of current.

Like the other adhesion promoters aluminum oxidizes readily when exposed to air, however aluminum oxide is soluble in both piranha solution and aqua regia. Aluminum is a p–type dopant in silicon semiconductors

2.1.4 Wet Chemicals

Deionized water or DI water was used after all wet chemical treatments. Rinsing with DI water removes debris and dissolves residues on the substrate. DI water can aid in the determination if the surface of a substrate is hydrophobic or hydrophilic after a surface treatment, such as the hydrophobic response of hydrogen terminated silicon after a hydrofluoric acid dip. Substrates were rinsed in running DI water for at lease 20 seconds before being dried with nitrogen.

Isopropyl alcohol or IPA was used after acetone cleaning and before a DI water rinse. IPA is a solvent which aids in the removal of acetone residues and will dissolve photoresists slowly.

Acetone is a chemical solvent which was used to aggressively attack the photoresists used in this work as well as any organic residues. Acetone is volatile at room temperature and leaves a residue when it evaporates thus substrates were quickly cleaned with IPA after being cleaned with acetone.

Piranha solution was typically mixed into ratios of 3:1 H_2O_2 : 97% H_2SO_4 and heated to 80 °C. The oxidizer (H_2O_2) was always added slowly to the acid to prevent its concentration from being above 50%. High concentrations of H_2O_2 in piranha solution risks boil over or explosions. The solution was heated to 80 °C to maintain constant light bubbling and chemical action. The piranha solution self–heats rapidly upon introduction of the oxidizer and substrates that are to be cleaned should be placed in the solution after the initial self–heating step has subsided. Adding water to the solution causes it to self–heat again and proper disposal of piranha solution involves resting the solution for at least an hour which lets the reaction complete and the solution cool, or slowly adding at least three times as much water to the initial solution so as to cool and dilute it.

The piranha solution attacks almost all organics and many metals, and is one of the few chemical etchants which can dissolve elemental carbon into solution. Relevant to micro–crucible lateral growth template fabrication, piranha solution was used to clean substrates, prepare substrates for encapsulation, remove residual adhesion layer

metals as the final cleaning step before substrates were placed into the quartz tube furnace.

Microposit MF-319 was used to develop Shipley 1813 resists. MF-319 is a Tetramethylammonium Hydroxide (TMAH) based developer that will irritant the eyes, lungs and skin if exposed.

AZ 726 MIF was used to develop AZ 5214-E resists. AZ 726 MIF is a TMAH based developer. It is unknown if MF-319 and AZ 726 MIF can be interchanged with one another, but their TMAH concentrations vary by 0.5% (2.5% and 2.0% respectively).

Transene Gold Etchant TFA is a iodine/potassium iodine based solution used to selectivly etch gold. The solution is relatively safe and will irritate and stain any skin exposed to it. Transene Gold Etchant TFA loses its potency over time and needs to be replace periodically to maintain consistent etch results. Gold etchant was used to define the micro–crucible geometry using the wet etch and definition approach and to remove gold out from the micro–crucible test structure during the second gold etch.

Aqua regia was mixed in 3:1 35% HCl : 70% HNO_3 solutions by volume and used to etch gold, as well as clean aluminum residues. It is a self-heating solution which fumes chlorine and nitrosyl chloride gases upon mixing and should be handled with care. Titanium and chromium are resistant to aqua regia etches. Aqua regia used to etch gold out of the micro–crucible during the second gold etch step tends to result in a less planar gold interface than Gold Etchant TFA because the solution was

not ultrasonically agitated while etching. Ultrasonically agitated aqua regia posses health and safety risks.

Transene Chromium Etchant 1020 is a nitric acid solution with ceric ammonium nitrate. Being a strong acid, Transene Chromium Etchant 1020 should be handled with care and gives off fumes if heated above 50 °C. For processing micro–crucible test structures, Chromium Etchant 1020 was used to undercut the chromium adhesion layer using the wet etch definition approach fabrication technique, to remove any excess chromium in the micro–crucibles during the overnight clean prior to CVD growth and to remove chromium hard masks.

Remover 1165 from Micropoist is a mixture of pure organic solvents specifically formulated to remove Shipley photoresists which have been exposed to high temperatures, strong etchants and other harsh processing procedures. Remover 1165 was used to remove AZ5214-E during the lift–off definition approach. Acetone was used instead of Remover 1165 during wet etch defintion approach because Remover 1165 did not aggressively attack the Shipley 1813 photoresist and caused the patterned gold structures to deform if the solution was agitated.

Sulfuric acid (H_2SO_4) with a concentration of 97% was used as a titanium and aluminum etch as well as a photoresist stripper. Processed micro–crucibles structures were left in H_2SO_4 overnight to remove any residual metals as well as soft masks prior to CVD growth.

Buffered oxide enchant (BOE) of a 6:1 40% NH_4F : 49% HF concentration was used to remove the micro–crucible test structure encapsulation layers and allowed for high–resolution scanning electron microscope imaging. On silicon LPCVD nitride

substrates, BOE allowed for great etch selectivity if the encapsulation layer was PECVD silicon oxide and good selectivity if the layer was PECVD silicon nitride. There was a 20:1 selectivity etch ration between PECVD and LPCVD silicon nitride using BOE. BOE was also used to chemically thin LPCVD silicon nitride and silicon TEM samples.

Potassium Hydroxide (KOH) was used in solutions with DI water at concentrations of 30%. The solution was heated to 50 °C to controllably etch the backside of silicon substrates, which took between 2 to 4 hours, when preparing them for transmission electron microscopy. The solution needed to be covered as it evaporated at 50 °C as evaporating water caused the concentration of KOH to increase and a reduced silicon etch rate. The solution had a tendency to boil over if its temperature was near 100 °C.

Trichloroethylene is chemical solvent which was used to remove Apiezon Wax W residue after TEM sample preparation. Trichloroethylene was heated to 80 °C in a small Erlenmeyer flask and allowed to vaporize. The vapor would condense on TEM tweerzers holding the TEM grid when place in the flask, over the solution, and would clean the sample of the KOH resistant wax as the solvent dripped off.

2.1.5 Reactive Gases

Oxygen Plasma was used to descum photoresists after they were developed and as surface treatment before the PECVD encapsulation layer was deposited. Descums were typically done for 30 seconds with 150 Watts of power so as to not burn the photoresist. Oxygen plasma was also useful for removing all of the moisture from the surface of the substrate.

Sulfur hexafluoride (SF_6) is a non-toxic, non-flammable, potent greenhouse gas which was used as the dry etching gas for silicon oxide and silicon nitride using a reactive ion etcher. A typical etch recipe used 25 sccm of SF_6 at 100 Watts of power and at 20 mTorr. The etch rate for PECVD and thermal oxides was around 0.67 nm/s and the etch rate for PECVD and LPCVD nitride was around 1.4 nm/s. SF_6 aggressively etches silicon and any etch involving the removal of the encapsulation later post–CVD growth must be under–etched so as not to destroy the growth. Both gold and chromium do not etch quickly when exposed to SF_6 and can be used effectively as hard masks.

Fluoroform (CHF_3) is a Trihalomethane commercially know as Freon 23. It is a potent greenhouse gas which is know to cause central nervous system damage with prolonged exposure. Fluoroform is used in reactive ion etching to selectively etch silicon oxide. A typical recipe used 40 sccm CHF_3, 70 sccm Ar and 7 sccm CF_4 (Tetrafluoromethane) at 720 Watts of power and 100 mTorr. This recipe selectively etched silicon oxide over silicon and silicon nitride and was used to etch the encapsulation layer of micro–crucibles when wet etching would damage features and details from the growth step. Over etching with this recipe will cause gold features to be sputtered away.

Argon (Ar) was used for ion milling of prepped TEM samples as a final thinning step. Argon was typically energized to 4.5 kV and the gas flow rate was adjusted so that the milled samples would receive 5-12 mA per ion burst. Ion milling with argon also aided in the removal of any residues and salts which remained on the TEM sample from the wet chemical processing.

2.1.6 Encapsulation and Adhesive Materials

PECVD silicon oxide was used as the encapsulation layer deposited over gold structures that were defined using the lift–off definition approach or the wet etch definition approach. Prior to PECVD deposition the surface of the substrate must be cleaned of all photoresist residue or else the PECVD oxide layer will be low quality and likely to delaminate. PECVD oxide appeared to have residual compressive stresses and was not mechanically robust enough to withstand the capillary forces of wet etchants after it had been selectively opened, thus additional layers were deposited with the PECVD oxide for mechanical support such as PECVD silicon nitride.

PECVD silicon nitride was used as an alternative encapsulation layer. PECVD silicon nitride is more mechanically robust than PECVD silicon oxide, but residual compressive stresses are a more pronounced problem with nitrides. PECVD silicon nitride was used both as a the only encapsualtion layer, and as a secondary encapsulation layer where it was deposited over a PECVD silicon oxide layer to give more mechanical integrity to the encapsulation structure. Stresses in PECVD nitrides films can be engineered by varying RF frequencies and gas ratio [169], or by post–deposition heat treatments.

PECVD polysilicon was deposited by accident when experimenting with PECVD silicon nitride as a secondary encapsulation layer. The PECVD silicon nitride recipe used by the McGill Nanotools Microfab implemented a short pre–deposition step using 2000 sccm of N_2 and 20 sccm of SiH_4 to aid in the adhesion and growth of the following PECVD silicon nitride deposition step. Typically this

pre–deposition step was 5 seconds long, but by accidentally changing the the step to 60 seconds, a thicker polysilicon film was deposited over the initially deposited PECVD silicon oxide encapsulation layer, but prior to the PECVD silicon nitride secondary films. Micro–crucibles fabricated in the fashion showed outstanding robustness and were rarely mechanically damaged by the capillary forces associated with etching the gold out of the micro–crucibles.

Crystal Bond 509 is a thermoplastic mounting compound used to secure wafer pieces to a carrier wafer for reactive ion etching, and to secure TEM samples to the cylindrical mount of the Gatan Model 623 disk grinder. Crystal bond readily dissolves in acetone and will soften at 71 °C.

Apiezon Wax W or black wax is a thermoplastic used as a high vacuum sealing wax and a masking wax for chemical etchants such as hydrofluoric acid, nitric acid, potassium hydroxide, tetramethylammonium hydroxide, ethylenediamine pyrocatechol and sodium hydroxide. The wax softens between 80 and 90 °C and is not soluble in alcohols like IPA and ethanol, or ketones like acetone. Black wax may be removed with aromatic hydrocarbon solvents like toluene or chlorinated hydrocarbons like trichloroethylene.

2.2 Fabrication Processes

To effectively use and analyze the gold–silicon VLS technique with regards to its applications in producing laterally grown silicon films on amorphous substrates, a robust test structure must be fabricated. Procedures on how to fabricate a micro–crucible, what was successful, and what was not successful will be highlighted in this section. The critical fabrication steps will be identified, and the reasoning behind their significance explained. While not exhaustively investigated, a brief reference will be given for chemical vapor deposition process parameters and an ideal growth regime for silicon growth in micro–crucibles suggested. A new technique for fabricating Transmission electron microscopy (TEM) samples with thousands of square microns of electron transparent area will be documented.

There were two processes developed to define a micro–crucible on an amorphous substrate, one using a selective wet etch of the gold film, hereafter referred to as wet etch definition approach, and one using a photoresist lift–off techniques to remove excess metal, hereafter referred to as the lift–off definition approach. After the micro–crucibles were defined, the two techniques shared the same process flow of plasma–enhanced chemical vapor deposition (PECVD) encapsulation, etching of gold catalyst out of the micro–crucible, sample preparation prior to growth, and chemical vapor deposition. Samples which had successfully nucleated and grown silicon films laterally within the micro–crucible were further prepared for electron beam investigations.

2.2.1 Micro–crucible Definition through Wet Etching

Metal was deposited directly onto the cleaned substrate surface for the wet etch definition approach. Test substrates were cleaned with 1:3 by volume H_2O_2:H_2SO_4 solution at 80 °C for 10 minutes followed by a low power oxygen plasma clean for 5 minutes prior to sample placement in the metal deposition chamber. Both electron beam evaporation and radio frequency sputter tools were used in these experiments, but due to the unavailability of chromium, the poor uniform coverage for very thin layers (5-10 nanometers), and the lack of an *in situ* measurement crystal, this research utilized electron beam evaporation deposition almost exclusively. The cleaned substrates were placed into the evaporation chamber, which was pumped down to a pressure of at least 5.5×10^{-6} Torr before deposition was started. Because of the reactivity of adhesion layers with oxygen, gold must be deposited over the adhesion layers while remaining under vacuum for electron beam deposition. For radio frequency sputter coating, experiments showed that adhesion layers exposed to oxygen could be etched with an argon plasma to remove the contaminated adhesion layer and gold would adequately adhere to the cleaned surface.

Adhesion layers were typically between 1 - 5 nanometers thick and their thickness affected the alloy composition of the gold catalyst. Initially, silicon was experimented with as an adhesion layer, but after 24 hours the thin–film was found to have blisters and upon further research [56] [57] [58] [59] it was found that silicon will react with gold a room temperature and diffuse though to the surface. Alloying the gold catalyst with adhesion promoters affects many aspects of micro–crucible fabrication

and silicon crystal nucleation within micro–crucibles during growth and will be discussed in Chapter 3. Thicker adhesion layers with thicknesses of 50 nanometers were tested, but this caused the gold catalyst to break up into many smaller globules because the volume of the micro–crucible was not filled. The initial adhesion layer used with the wet etch definition approach was 5 nanometers of titanium, but it was observed that titanium left a dark residue of particulates when etched with piranha solution which was detrimental to the controlled nucleation of silicon crystallites. Chromium was found to be a better adhesion layer due to it ease of removal using Transene Chromium Etchant 1020, and was used for the majority of the experiments using the wet etch definition approach. Gold was deposited over the adhesion layer with thicknesses of 50 to 150 nanometers. The amount of gold deposited affected the geometry of the crucibles and the initial volume of the catalyst. Gold film with thicknesses of 150 nanometer were not electron transparent in the TEM, but silicon crystallites nucleated in 150 nanometer micro–crucibles were, although they were still quiet thick and strong Kikuchi patterns were present in selective area electron diffraction (SAED) patterns.

For wafers which had their micro–crucibles defined through wet etching, the standard cleaning procedures prior to photoresist spin coating was with an immediate spin-coat deposition of the photoresist after removal of the substrate from the electron beam or plasma sputtering chambers, or an acetone/IPA/DI water rinse followed by a low power (100 - 200 Watts) oxygen plasma clean for five minutes. The photoresist used was MicroChem Shipley 1813 positive photoresist with a thickness

of 1.4 microns. The deposited photoresist was soft baked and exposed to UV radiation as prescribed by the manufacturer. There was no difference observed between using a metallized substrate or a thermally oxidized/LPCVD nitride deposited wafer with regards to the finest feature resolved using Shipley 1813. Exposed wafers were developed in Microposit MF-319 developer for a minute at room temperature and rinsed in DI water immediately after removal from the developer. The photoresist was observed in the microscope to see if it had been underdeveloped, and if so placed back in the developer for 10 - 20 seconds. The final step for a wafer undergoing the wet etch approach to mirco–crucible definition was a 30 - 60 seconds in a low power oxygen plasma clean which descummed any of the remaining exposed photoresist which was not removed using the developer.

The gold films were etch using concentrated Transene Gold Etchant TFA and were hand agitated in the solution for 30 to 45 seconds. The substrate were removed when the test structures became visible and submerged in DI water to stop etching. The etch gold films can be inspected in the microscope to see if any residual gold remained in the areas between the patterned photoresist, and etched further if any is present. Following the gold etch, the substrates which used chromium adhesion layers were placed in a concentrated solution of Transene Chromium Etchant 1020 and hand agitated for 1 to 2 minutes in order to remove most of the underlying adhesion layer. If etched for too long the gold features would lift–off the substrate. Removing the chromium allows for VLS grow in micro–crucibles using nominally pure gold catalysts. Gold structures without an adhesion layer are sensitive to capillary

forces and deform easily, and thus the photoresist on top of the structures must be removed carefully prior to PECVD encapsulation.

2.2.2 Micro–crucible Definition through Photoresist Lift–Off

For substrates using the lift–off definition approach, fabrication began with a substrate which has been cleaned in a 1:3 by volume H_2O_2:H_2SO_4 piranha solution for 10 minutes at 80 °C followed by a low power oxygen plasma clean for 5 minutes. Electronic Materials AZ 5214-E image reversal photoresist was spun to a thickness of 1.4 microns and was soft baked as per the manufacturer's recommendation. Using a lift–off resist was not found to be necessary as the structure of the mirco–crucibles is large for conventional photolithography and there was not a noticeable difference in the results, but lift–off resists were experimented with and the MicroChem LOR 3A process was found to work well with the AZ 5214-E resist. The photoresist was exposed to UV radiation, after which it underwent the prescribed reverse image bake and flood exposure. Processed wafers were developed in AZ Electronic Materials AZ 726 MIF developer for a minute at room temperature and rinsed in DI water immediately after removal from the developer. If the resist was observed to be underdeveloped, it was placed back into the AZ 726 MIF solution for an additional 10-20 seconds and rinsed again. Once the features of the photoresist were found to be acceptable, the substrates were descummed in a low oxygen power plasma.

Before metal deposition, the substrate was dry etched back 20-50 nanometers using a reactive ion etch (RIE) of SF_6, utilizing the lift–off photoresist as an etch mask. These etched back trenches allowed for better TEM resolution of silicon growth in the micro–crucible structure, and allowed for reactive adhesion layers such

as titanium and aluminum to be deposited without concern that they would oxidize as they would be encapsulated in the trench by gold. After the RIE etch, the wafer was placed in the electron beam evaporation chamber where adhesion layer thicknesses of 1 nanometer and gold thicknesses of 50 and 150 nanometers were deposited. The gold needed to be as thick as the trench was deep, or else the gold would not fill the entire volume of the micro–crucible once encapsulated. After deposition the excess metal was lifted off in an agitated bath of Microposit Remover 1165 for 10 minutes at 60 °C and resulted in only the photomask pattern remaining attached to the substrate. Because the AZ 5214-E resist had been exposed to ionized plasma during the wafers cleaning and x-rays during the metal deposition, it was difficult to remove and a piranha strip of 10 minutes or greater was required to remove all of the resist, after which the wafer was conditioned for encapsulation.

2.2.3 PECVD Encapsulation Layers

Once gold had been successfully patterned into micro–crucible pre–structures on an amorphous substrate, the structures must be carefully encapsulated using a PECVD silicon oxide or nitride. Encapsulation was one of the more critical steps in the process, and if done incorrectly then the fabrication effort up to this point could not be salvaged. The most important factor to deposition a PECVD encapsulation layer was that it adhered well to the substrate, which required that the substrates be cleaned of all chemical and water residues before being encapsulated.

For the lift–off definition approach, one could simply place the wafer into piranha solution before encapsulation, because the patterned gold was well attached to the substrate with an adhesion layer, and the adhesion layer was protected from the

piranha solution by being encapsulated with gold in the etched trenches. For the wet etch definition approach, one must be very careful with the patterned gold structures once they were undercut. It was best to clean off the photoresist in successive, room temperature, unagitated baths of acetone, Microprosit Remover 1165, IPA and DI water for periods of 10 to 20 minutes per bath. Care was taken to not allow capillary forces to damage the patterned gold structures when transferring the wafers from one bath to the next. The wafers were left submerged in their solutions until it was sure that the photoresist was stripped and all residues cleaned. Wafers using the wet etch definition approach were carefully dried using light pressure from the dry nitrogen gun positioned 20 centimeters directed above the wafer before being placed in the PECVD chamber. Alternatively, a photoresist strip using a reactive ion dry etch was attempted on wafers using the wet etch definition approach, but an optimized oxygen plasma recipe was not found. Once placed in the RIE/PECVD tool, wafers employing both the lift–off definition and wet etch definition approach were cleaned for a last time in a low power oxygen plasma to remove any remaining residuals and water beads. Lift–off definition wafers were cleaned for 30 seconds while wet etch definition wafers were cleaned for 10 minutes.

Using PECVD silicon oxide as the sole encapsulation layer was found not to work, as it was not mechanically robust enough would break apart as the micro–crucible structures were further processed. PECVD nitride was found to be robust enough to withstand later processing, but had issues with compressive stresses and would deform and alter the geometry of the micro–crucible after the gold was partially etched out. Heat treating PECVD–nitride–only encapsulation layers at 400 °C for

6 hours resulted in PECVD silicon nitride films which displayed less deformation associated compressive stresses, but also resulted in pin holes developing in the film, which were visible after etching the encapsulated micro–crucibles in Transene Gold Etchant TFA.

PECVD nitirde films were used as a mechanical aid for initially deposited PECVD oxide encapsulation layers reduced the number of micro–crucibles which were damaged by the capillary forces associated with partially wet etching the gold out of a fabricated crucible, but the yield remained undesirably low. Any recipe that used separate PECVD deposition steps required the substrate to be removed from the PECVD chamber, and for the chamber to be cleaned between each consecutive deposition step, or else debris from the prior step would be lodged into the currently depositing film and defects would be visibly present over the substrate.

The most robust, least deformed encapsulation layer used in this experiment was a triple PECVD layer structure of initially deposited PECVD silicon oxide, followed by a layer of PECVD polysilcion and topped with a layer of PECVD silicon nitride. The polysilicon deposition step was achieved by altering the McGill Nanotools NITRIDE DEP 300 deposition recipe so that the pre–deposition step ran for 60 seconds instead of 5 seconds. The processing conditions for the PECVD oxide (OX DEP 300), polysilicon and nitride (NITRIDE DEP 300 Deposition) are given in Table 2–1. The only process used for the triple stacked PECVD encapsulation layer was 60 seconds of the OX DEP 300 recipe, followed by 60 seconds of the NITRIDE DEP 300 Pre–deposition recipe, and 17 seconds of the NITRIDE DEP 300 Deposition recipe.

Table 2–1: Process Parameters for PECVD Encapsulation Layer Deposition

Recipe Name	Pressure	Power	Gas Flow Rates	Temperature	Distance to Susceptor
OX DEP 300	2.8 Torr	125 Watts	60 sccm SiH_4 1200 sccm N_2	300 °C	350 mils
NITRIDE DEP 300 Pre–deposition	4.5 Torr	350 Watts	30 sccm SiH_4 2000 sccm N_2	300 °C	600 mils
NITRIDE DEP 300 Deposition	4.5 Torr	450 Watts	180 sccm SiH_4 75 sccm NH_3 2000 sccm N_2	300 °C	600 mils

2.2.4 Etching Gold Out of Micro–crucibles

Assuming the PEVCD encapsulation layer was robust enough to withstand the capillary forces of gold wet etchants, there were multiple ways to partially etch gold out of the micro–crucibles. The best technique found was to heat Transene Gold Etchant TFA to 50 °C and allow the samples to rest at the bottom of the solution. Also experimented with was ultrasonicating the gold etchant and holding the samples with tweezers in the solution, which worked well too, but dropping the sample to the bottom of the solution cause the sample to vibrate directly on the glassware and destroyed some of the micro–crucibles. Aqua regia was experimented with and found to work similarly to heated gold etchant. Diluting the gold etching with water

caused the etch rate to decrease, as well as causes the gold–vapor interface to be more planar.

2.2.5 Sample Preparation Prior to Growth

Partially etched samples were cleaned before being placed into the CVD reactor for the growth step. The samples were placed in a concentrated acid overnight in an attempted to remove any remaining organics or adhesion metal residues from within the micro–crucible. Sulfuric acid was used for micro–crucibles with titanium and aluminum adhesion layers, and chromium etchant was used for chromium adhesion layers. Other acids could be experimented with to see if the results are affected. It is not known if the overnight soak is necessary, as experiments were never conducted without the overnight step.

Immediately before being placed in the reactor, the samples to be tested were placed in a 1:3 by volume 35 % H_2O_2 : 97 % H_2SO_4 piranha solution for 10 minutes. If titanium of aluminum adhesion layer were used, the samples were dipped in a 1:3 by volume 70% HNO_3 : 35% HCl aqua regia solution for 30 seconds prior to the piranha clean in an attempt to remove the disperse, discontinuous gold particles at the gold–vapor interface. Samples were dried and arranged on a quartz boat so that all of the micro–crucibles of the various samples were oriented the same way. It is not known if sample orientation in the reactor affected deposition and growth.

2.2.6 Chemical Vapor Deposition Process Parameters

Experimental variation of the chemical vapor deposition step was not rigorously investigated and the majority of the experiments were conducted at 450 °C, with a pressure of 600 mTorr and gas flow rates of 150 sccm of SiH_4 and 1800 sccm of N_2.

Experiments conducted between 500 °C and 600 °C nucleated faceted silicon in less than 30 minutes, but the micro–crucibles were always blocked with nanowire growth and there was uncatalyzed polysilicon deposition everywhere on the samples. The nitrogen flow rate was reduced to 900 sccm of N_2 for some experiments in an attempt to speed up the reaction by increasing the partial pressure of SiH_4, but results did not vary significantly. It is known that the position of the samples in the CVD reactor was an important parameter which varied the growth results significantly. For all experiments, the samples were placed in the area of the reactor labeled as "Load Boat".

The operable range for growing silicon thin–films in micro–crucibles was between 400 °C and 500 °C. At 400 °C growth was slow, taking more than 3 hours to produce similar results to the 450 °C tests run for 1 hour. At 500 °C, growth was fast and sometimes had nanowire growth blocking the micro–crucible. For growths longer than 1 hour at 500 °C, uncatalyzed polysilicon deposition was visible on the amorphous surfaces of the micro–crucible.

2.2.7 Preparing Samples for Transmission Electron Microscopy

An accomplishment of note in this work is a new technique for preparing TEM samples of micro–crucible growth which are electron transparent for areas up to a square millimeter. The process required the use of silicon wafer substrates which have an amorphous LPCVD silicon nitride layer, preferable 100 nanometers thick or less. Samples, which had been through the CVD step, first needed to have their encapsulation layers removed. This was done using a BOE wet etch so as not to remove the LPCVD silicon nitride layer. Dry etching using CHF_3 chemistries created holes

in the underlying LPCVD silicon nitride layer, which made the samples mechanically unstable during thinning. After removal of the encapsulation layer, the sample were re–encapsulated with 20 nanometers of PECVD silicon nitride to protect the silicon crystals in the micro–crucibles. PECVD silicon nitride layers thicker than 20 nanometers caused the thinned, electron transparent films to bend, break and curl, rendering the areas not viewable with a TEM. After the encapsulation steps, the samples with silicon crystal growth in micro–crucibles were sectioned into 2 by 2 millimeter squares. If the substrate was a {1 0 0} silicon wafer, this could be done using glass breaking pliers, but if the substrate was {1 1 1} silicon, then a dicing saw was needed to section wafers into the proper sized squares.

The sectioned wafers were glued, device side down to a nickel TEM grid with a circular hole of 1 millimeter, which was been coated with Apiezon Wax W black wax on one side. The black wax was best applied by first smearing some of it across a heated glass slide, and then sliding the TEM grid through the smeared black wax so that one side of the grid was coated with wax. The TEM grid was flipped so that the wax coated side was up and the 2 by 2 millimeter sectioned wafer sample was positioned so that the area of interest was in the center of the TEM grid hole. After gluing the sectioned wafer to the grid, the grid and sample were transferred onto the cylindrical mount of the Gatan Model 623 Disc Grinder, where a dab of crystalbond was placed at the center of the cylindrical mount. Immediately after transfering the glued sample/grid to the cylindrical mount, the mount was removed from heat and the sample/grid had a downward pressure applied to them so that they were as flush

with the surface of the cylindrical mount as possible. Blowing on the cyclindrical mount helped cool and set the crystal bond faster.

After being mounted, the sample was progressively thinned using the disc grinder and 320, 500 and 1200 grit emery paper. The sample/grid was polished to 500 mircons using the 320 grit, after which it was polished to 250 micron using the 500 grit. At 250 microns, the 1200 grit paper was used to polish the sample to 150 microns, after which the specimen was inspected to make sure the edges of the sample were not polished away, and the sample had not cracked during the polishing process. The position of the disc grinder was progressively decreased by 10 microns and inspected until the sample/gird specimen was 80 microns thick, after which the cylindrical mount was removed and rinsed in water.

The cylindrical mount was heated to remove the sample/grid specimen. Because crystal bond softens at a slightly lower temperature that the black wax, it was possible to slide the grid off of the cylindrical mount without disturbing the adhesion of the sample to the gird. The removal must be done immediately after the crystalbond softens. The removed sample/grid specimen was then attached to the Pyrex specimen mount of the Gatan Model 656 Dimple Grinder using crystalbond. With the dimple grinder, the center of the polished sample was further thinned for four minutes using the copper grinding wheel and diamond paste. To reliably find the center of the sample/grid specimen the grinding wheel must be placed on the specimen for a short time and afterward inspected. If the initial dimple was not in the center of the specimen, the position of the wheel was adjusted and the dimple/inspection process repeated until it was centered. After four minutes of dimpling, the sample

was sufficiently thin for chemical etching in KOH. There should not be a visible hole in the center of the sample after dimpling.

The specimen was removed from the Pyrex specimen mount the same way it was removed from the cylindrical mount. The sample/grid was gripped with a pair of gold coated, self–closing tweezers and submerged in acetone and IPA baths to remove and excess crystalbond. Using a black wax "paint brush", the underside of the sample/gird was coated in a thick layer of black wax, to prevent hot KOH from attaching the device side of the glued sample. Back wax "paint brushes" were made by slicing a small chuck of black wax from the stick and placing it on a glass slide. The chunk melted into a bead as it was heated and by sticking a tooth pick into the a the freshly melted bead and pulling it out, a long, pointed tip of black wax can be deposited to the end of the tooth pick, which acts as a useful tool for selectively applying black wax.

The sample/gird specimen, held in gold plated tweezers and coated in black wax on the device side, was placed into a bath of 30% KOH heated to 50 °C. Etching was faster at high temperatures, but the black wax also softened at these higher temperatures, causing the sample to unglue from the grid and fall to the bottom of the KOH solution. It took 2–4 hours of etching in the 30% KOH 50 °C solution to thin the backside of a polished silicon {1 0 0} wafer sample to the device layer. After 1 hour the specimen should be checked every 30 minutes so as not to destroy the sample by over etching it. The gold in the micro–crucibles became visible in a stereo microscope once etched through to the device layer, and it only took 10 minutes of continued etching to make the hole significantly larger once one was already present.

Nickel grids were used as they are resistant to KOH attacks, whereas copper and molybdenum grids were not.

To remove the excess black wax, the sample/gird specimen, remaining held by gold plated tweezers was positioned over a boiling solution of trichloroethylene, which condensed on the sample and removed the blackwax as the solvent dripped off. Care should be taken not to clean the sample/gird specimen for too long, as the sample will come unglued from the grid if all of the black wax is removed. This can be remedied by securing the sample to the grid after the KOH thinning using a hard setting epoxy. Once the black wax is removed, the TEM sample was ion polished on both sides for 5 minutes at 30 ° incident angles using the Gatan 695 Precision Ion Polishing System. This ion polished removed any chemical residues left in the electron transparent areas.

CHAPTER 3
Manuscripts

The following manuscripts summarize the research done on laterally grown silicon thin–films using micro–crucibles, and the scientific observations and conclusions drawn from the work. The manuscripts represent a chronological evolution of the work, where preceding manuscripts build off the work of the pervious ones. The first section, "Nucleation and solidification of laterally grown silicon micro-films on amorphous substrates using the VLS mechanism" was published under that title in the Journal of Crystal Growth, vol. 391, 2014. This published work outlines the initial observations of the effect adhesion layers have on silicon growth in micro–crucibles, and discusses the mechanics of undercooling in the micro–crucibles as a function of adhesion layer contamination. The second and third sections are manuscripts in the process of being published. The second manuscript details a new technique for fabricating micro–crucibles without the use of adhesion promoting materials and observes preferred orientations of silicon thin–films nucleated in micro–crucibles, and orientation relationships between different grains present in these silicon thin–films. The third manuscript details a second technique for fabricating micro–crucibles which allows for the use of VLS catalysts and adhesion promoters which would normally be oxidized and left unsuitable for VLS growth if fabricated with the techniques from the previous manuscripts. Varying the adhesion layer had significant effects on micro–crucible fabrication and silicon growth within, and these effects are described here.

Proven is the ability to grow large single crystals laterally within micro–crucibles, and theorized is the evolution of silicon as it leaves the gas phase, diffuses into the solid phase, transforms into the liquid phase, and nucleates at a critical supersaturate concentration. The second and third manuscripts could not have been written without the aid and resources of Nicolas Brodusch and Prof. Raynald Gauvin of McGill University, and they will be listed as second and third authors in the upcoming publications.

3.1 Nucleation and solidification of laterally grown silicon micro–films on amorphous substrates using the VLS mechanism

3.1.1 Abstract

A new technique for nucleating and observing silicon crystallites in confined geometries over amorphous substrates has been demonstrated using the vapor–liquid–solid (VLS) mechanism. Unlike the originally proposed VLS nanowire growth mechanism on a silicon substrate, confined growth within amorphous structures does not have an available source of silicon to saturate the catalyst prior to deposition or to control crystal orientation during growth. Silicon crystallites were nucleated in confined geometries of amorphous materials at 450 °C, with a silane partial pressure of 46 mTorr and a growth time of 60 minutes. Crystallites with planar areas upwards of 17 μm^2 were grown. It was found that there were two distinct solid lamellar morphologies present in the various test structures and that these morphologies affected the calculated growth rates, volumetric distributions and morphologies of the nucleated crystallites. The distribution of crystallite volumes for the two populations was measured and average growth rates were found between $3.17 \times 10^{-2}\,\mu m^3/min\,\mu m^2$ and $2.30 \times 10^{-2}\,\mu m^3/min\,\mu m^2$, where the area in the denominator represents the initial gold–vapor interface area. It is believed that the different gold–silicon lamellar morphologies can be attributed to residue of the chromium adhesion layer which increased the lamellar spacing due to decreased undercooling of the liquid gold–silicon solution. Undercooling was estimated to be 130 °C from the eutectic temperature in the samples believed to have had their chromium adhesion layers completely removed.

3.1.2 Introduction

Recently lateral growth of semiconducting materials within confined geometries over amorphous substrates [142, 140] has been successfully achieved using the vapor–liquid–solid (VLS) technique. Lateral growth of unseeded high–quality semiconductors on amorphous substrates is of particular importance for the development of low–cost, high–efficiency, third generation photovoltaics as they can be used as the seeding materials for large area thin–films when complemented with the vapor [130] and liquid [132] phase epitaxial layer overgrowth techniques already developed. Because of the interest of using VLS grown semiconducting materials in three–dimensional integrated CMOS circuits [140], as building blocks for electronic/optoelectronic devices [142] and as seeding materials for large–area semiconducting substrates, the authors have fabricated a novel test structure made of amorphous materials for lateral growth of silicon crystals in a confined geometry, which has been termed as micro–crucible (Figure 3–1).

The work carried out by Wagner [66] used gold film deposited on silicon wafers, which when heated formed microscopic liquid gold–silicon eutectic alloy islands on the surface of the wafer. When attempting similar research on amorphous substrates (like silicon oxide and nitride), a key difference from the original work is that the silicon from the cracked vapor diffuses into a solid gold catalyst and dissolves in the solid state until a solid to liquid phase transformation occurs. Also unlike the original work, confined growth on amorphous substrates does not have a seeding crystalline substrate to facilitate the deposition of silicon from the liquid to the solid phase, but must nucleate crystallites from supersaturated gold–silicon solutions.

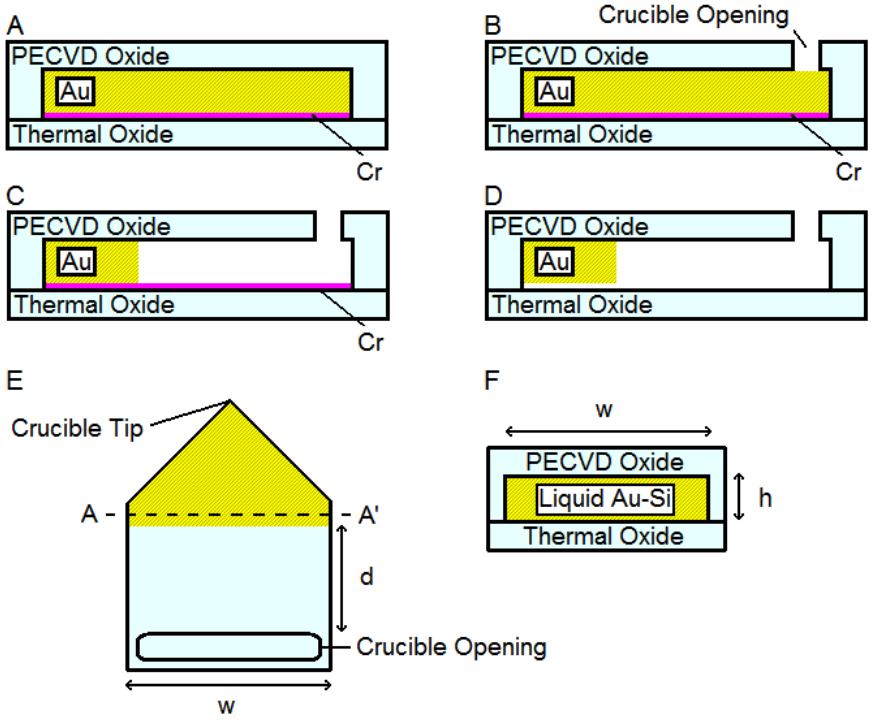

Figure 3–1: Structure and fabrication process of micro–crucibles. (A) PECVD oxide encapsulated micro–crucible with film thickness of 150 nm Au and 5 nm Cr. (B) Opening of the micro–crucible using a dry etch. (C) Timed gold etch to control solid gold catalyst amount. (D) H_2SO_4 etch to remove residual Cr and organics. (E) Planar diagram of finished micro–crucibles with d representing the silane diffuse distance. (F) A cross–section through the dotted line A–A' in Figure 3–1E of the assumed gold–vapor interface where the solid catalyst has transformed into a liquid.

Furthermore, VLS experiments are typically conducted with only gold and silicon, whereas deposition of gold on silicon dioxide often requires the use of an adhesion layer [142] which, as the authors will show here, adds complexity to the system. These divergences from the traditional VLS mechanism have prompted the study of nucleation of silicon crystallites in confined geometries of amorphous materials.

The authors of a previous nano–scale TEM study [115] of the gold–silicon system on an amorphous substrate found no significant difference between the catalytic effects of the surface of solid or liquid gold when using disilane. It was also noted that, once supersaturated, silicon nucleated heterogeneously. These similarities between solid and liquid gold catalysts during VLS growth implies that for particular geometries, i.e. an adequately large surface to volume ratio and short diffusion lengths, there should be no difference between solid and liquid gold catalysts used for confined growth. The finding that heterogeneous nucleation occurred on amorphous substrates implies that the supersaturation needed for nucleation of silicon crystallites will depend on the substrate/encapsulation material and composition of the catalyst. Keeping a catalyst of pure gold was more straightforward in the original VLS work, but the composition of the catalyst or cleanliness of the catalyst–amorphous substrate interface may be affectedwhen working with titanium and chromium adhesion promoters associated with gold on silicon dioxide, thus affecting the critical supersaturation needed for nucleation. Observations indicate that these adhesion promoters effect how saturated gold–silicon solutions nucleate silicon crystallites and form lamellar solids after processing. The effects of these adhesion promoters on (1) nucleation, (2) growth of silicon crystallites and (3) solidification

of gold–silicon lamellar structures during the initial and final phases of VLS growth in confined geometries of amorphous materials will be discussed further here.

3.1.3 Experimental

Starting with silicon {111} wafers with 900 nanometers of thermal oxide, two metallic films (5 nanometers of chromium followed by 150 nanometers of gold) were deposited using an electron beam evaporator at a pressure of 5.5×10^{-6} Torr. A 1.4 micrometer layer of S1813 (MicroChem Newton, MA) photoresist was deposited, patterned with micro–crucible test structures, exposed and developed. Following a 30 second descum in an oxygen asher, the wafers were placed in a bath of 1:3 gold etchant (Gold Etchant TFA, Transene Company, Danvers, MA) to the water solution, where they were agitated by hand until the gold micro–crucible test structures were clearly visible, which took 2–3 minutes. After the structures were defined, the wafers were wet–etched for 60 seconds in Chromium Cermet Etchant TFE (Transene Company, Danvers, MA). Once the remaining adhesion layer between the test structures was etched, the S1813 was removed in a 10 minute ultrasonically agitated acetone bath followed by an IPA/DI water rinse and dried with pressurized nitrogen. The cleaned gold micro–crucible test structures were encapsulated using a layer of plasma–enhanced chemical vapor deposition (PECVD) silicon oxide (about 500 nm) (Figure 3–1A).

A second photoresist of AZ 5214E (Clariant GmbH, Wiesbaden, Germany) was patterned and developed on top of the wafers with the objective of removing selected areas of the encapsulation layer. These areas were removed using a reactive ion dry–etch and effectively became the openings for the micro–crucible structures (labeled

in Figure 3–1B and E). The opened structures were placed in a timed, ultrasonically agitated gold–etch (Gold Etchant TFA), where the etch time determined how much gold catalyst would remain at the tip of the micro–crucible (Figure 3–1E). The wafer was then submerged in acetone for 5–10 minutes to remove the photoresist. Prior to catalyzed growth the wafers were left in concentrated H_2SO_4 overnight to remove the remaining chromium and organics from the micro–crucible (Figure 3–1D).

Just before being placed in the CVD chamber, the wafers were cleaned in a self–heated 1:3 H_2O_2:H_2SO_4 piranha solution for 2 minutes. The wafers were processed in a hot–walled, low–pressure chemical vapor deposition (LPCVD) quartz tube for 60 minutes, at a temperature of 450 °C, a pressure of 600 mTorr and gas flow rates of 150 sccm of SiH_4 and 1800 sccm of N_2 (10 mTorr pp_{SiH_4}). After deposition the quartz boat holding the wafers was directly removed from the 450 °C furnace and allowed to cool in air. The remaining encapsulation layer over the gold and deposited silicon was removed for improved resolution during scanning electron microscopy (SEM) examination and encapsulated again using a 100 nanometer PECVD nitride film to produce a transmission electron microscopy (TEM) specimen using a similar technique discussed elsewhere [115].

3.1.4 Results

Figure 3–2 depicts the same neighboring micro–crucibles before (Figure 3–2A) and after (Figure 3–2B) deposition. The gold etch appears to have been successful as no metal particles are observed in the channel in Figure 3–2A and no isolated nanowires appear in Figure 3–2B; however, the chromium etch appears to have been unsuccessful in some of the crucibles, as indicated by the labeled dark

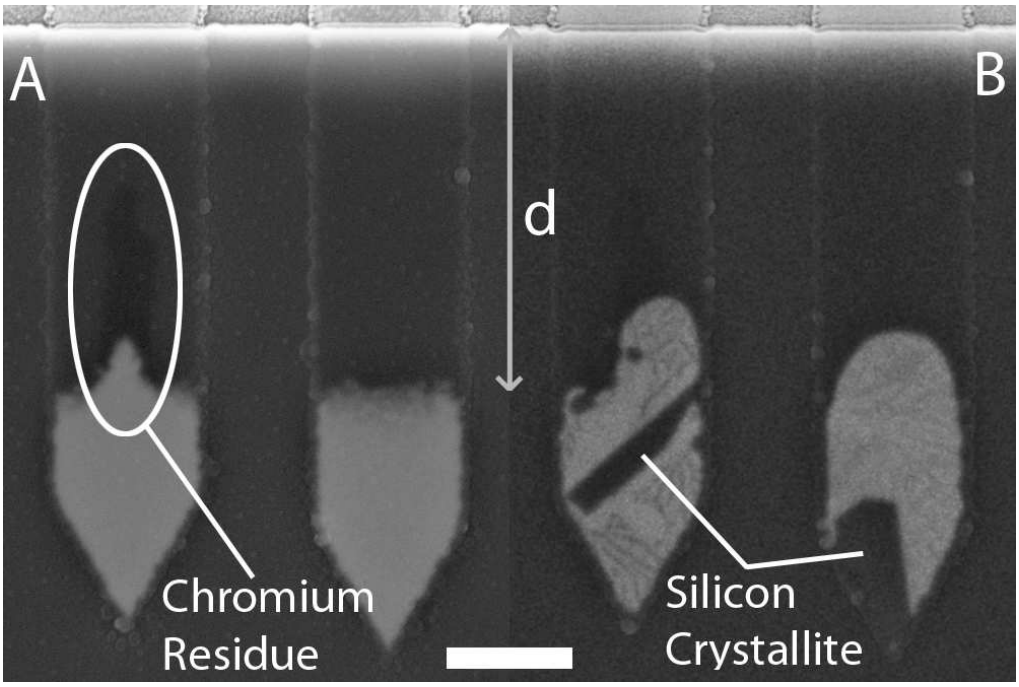

Figure 3–2: Secondary electron images of neighboring micro–crucibles before (A) and after (B) the growth step. Dimension d represents the distance the silane diffused within the crucible to reach the gold–vapor interface. The scale bar represents 6 µm.

patch in Figure 3–2A. Using a TEM in scanning transmission electron microscopy (STEM) mode, micro–crucibles have been analyzed using energy–dispersive X-ray spectroscopy (EDS) prior to deposition and have shown the presence of chromium atoms after being exposed to chromium etchants (Figure 3–3). By multiplying the area of the planar crystallites in the micro–crucibles by the catalyst thickness, an approximation of silicon crystallite volume has been attributed to each crucible. The crystallites in Figure 3–4 have areas of 7.4 and 11.5 μm^2, and approximate volumes of 1.2 and 1.9 μm^3 for the left and the right crucible, respectively.

It appeared that all of the gold was transformed into a gold–silicon liquid during processing because of the even distribution of silicon within the gold–silicon lamellar solid (Figure 3–2B & 4). The gold–silicon solid with irregular lamella in the micro–crucibles has taken two visibly distinct lamellar morphologies, fine and coarse (Figure 3–4). These two morphologies are due to different eutectic freezing and were distributed in the micro–crucibles across the wafer. When taken as two different populations the crystallite volume in micro–crucibles with a fine lamellar solid had a mean value of 2.01 μm^3 (13.00 μm^2) with a standard deviation of 0.30 μm^3 (1.94 μm^2), whereas the crystallite volume in micro–crucibles with a coarse lamellar solid had a mean value of 1.45 μm^3 (9.35 μm^2) with a standard deviation of 0.39 μm^3 (2.52 μm^2). Both populations appeared to be normally distributed; Figure 3–5 depicts the distribution of crystallite volumes in micro–crucibles with fine lamella. The linearity of the data in the normal Q–Q plot indicates a strong correlation between crystallite volumes in crucibles with fine eutectic microstructures and a normal distribution. These values correspond to an average crystallite growth rate of $3.17 \times 10^{-2}\,\mu m^3/\min\,\mu m^2$

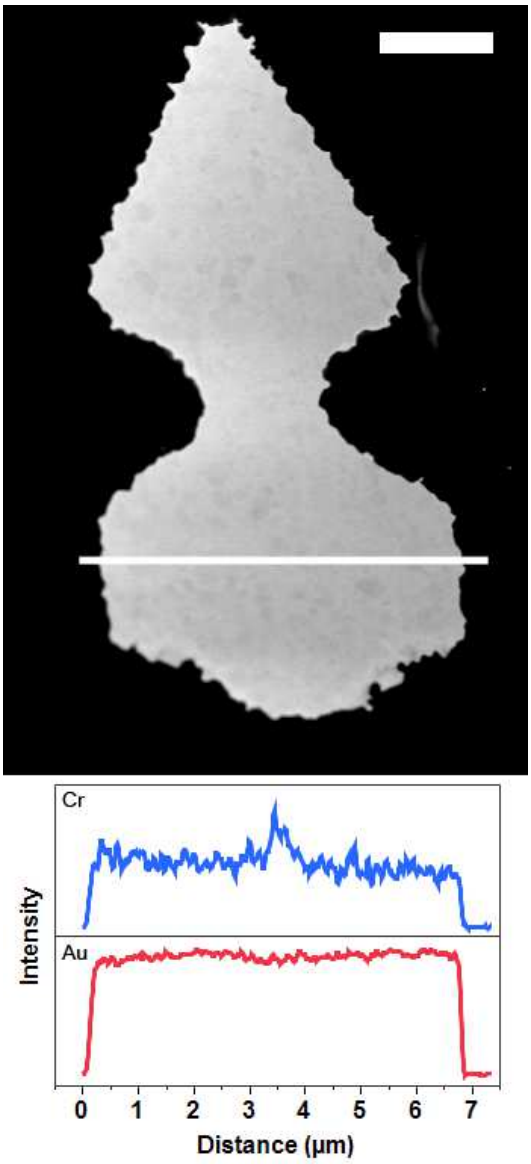

Figure 3–3: High–angle annular dark–field (HAADF) image of a micro–crucible before deposition. The white line across the crucible represents the line scanned to determine the Au and Cr EDS profiles. The scale bar represents 2 µm.

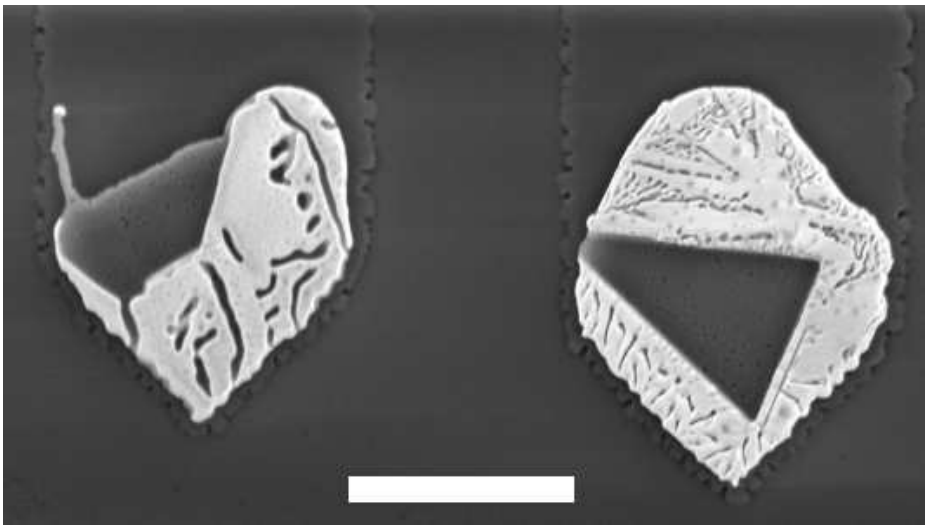

Figure 3–4: Secondary electron image of neighboring micro–cubicles with the PECVD oxide encapsulation layer removed. The left and right crucibles display coarse irregular and fine irregular lamella, respectively. The scale bar represents 5 µm.

for crucibles with fine structured lamella and $2.30 \times 10^{-2}\,\mu m^3/min\,\mu m^2$ in the denominator of the growth rates used to normalize the data was the initial gold–vapor interface of a liquid catalyst in the micro–crucible (Figure 3–1F) and was assumed to be a rectangle with a height of the metal stack (155 nanometers) and the measured width of the micro–crucibles, which varied from crucible to crucible due to the uneven even etching of gold across the wafer during the crucible definition step. The gold–vapor interface was assumed continuous from the top of the crucible to the bottom once the solid catalyst had transformed to liquid completely.

In this study two populations were engineered with different silane diffusion distances, d (Figures 3–1E and 3–2), to observe whether there would be a significant difference in the silicon deposition rate between them. The two distances were

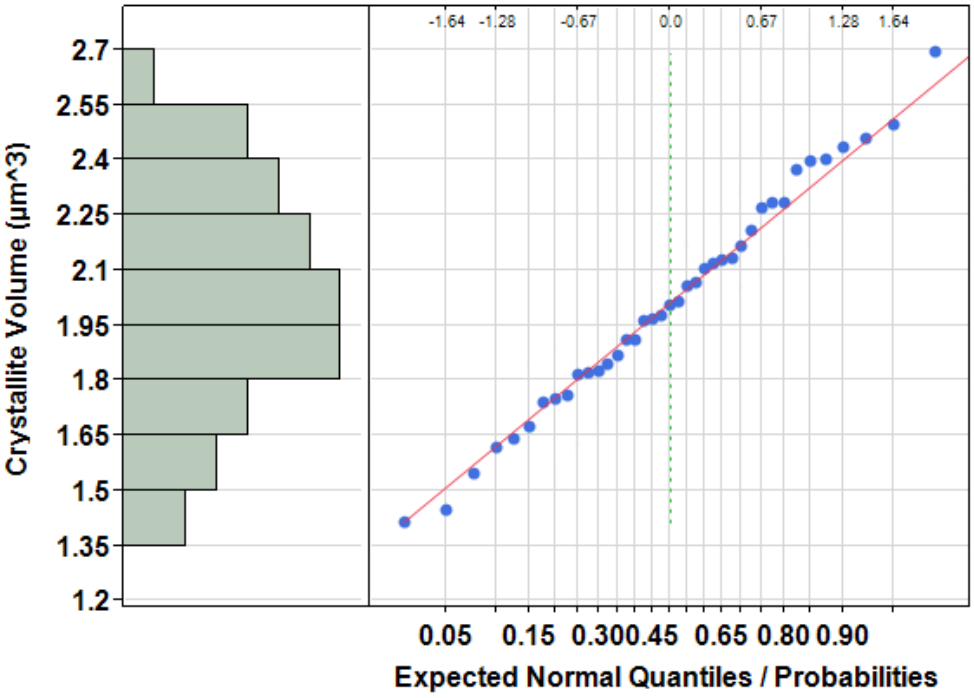

Figure 3–5: Histogram and normal quantile (Q–Q) plot of crystallite volume for crystallites nucleated in micro–crucibles with fine eutectic microstructures. The counts from each bin in the histogram can be seen in the vertical divisions of the Q–Q plot. N = 39.

approximately 17.5 and 25.5 micrometers. In the crucibles which had fine lamellar solids no significant difference in silicon crystallite volume was observed between the longer and shorter diffusion distances.

3.1.5 Discussion

Initially it appeared that the crystallite volumes in the micro–crucibles did not fall into a Gaussian distribution, for which it was believed they would if their fabrication was well controlled. Upon closer inspection it was found that the two distinct fine and coarse lamellar morphologies distributed throughout the crucibles had the expected normal distributions individually. In thermodynamically and microstructurally similar hypereutectic aluminum–silicon alloys [28], fine irregular lamella is associated with greater undercooling of the aluminum–silicon liquid before freezing [32, 33]. Typically this undercooling is attributed to thermal gradients or impurities, and since it is highly unlikely that there is a significant thermal gradient experienced by the neighboring micro–crucibles in Figures 3–2B and 4, it is believed that the variations in the gold–silicon lamellar structure can be attributed to residual chromium compounds, which act as nucleation sites for the lamellar structures, in some of the micro–crucibles. This is supported by the observed dark patch in Figure 3–2A, the measured chromium spike at the center of the scanned crucible in Figure 3–3 and the realization that the concentrated H_2SO_4 does not etch chromium, but instead facilitates the formation of passive chromium compounds [170]. The micro–crucibles which froze with fine structured lamella did so because the chromium adhesion layer had already been completely removed by completely undercutting the mirco–crucible

structure during the initial chromium etching step. The undercut for this particular experiment was about 3 micrometers, or about half the width of the crucible, and many of the micro–crucibles were lifted off the substrate due to the undercut immediately after the chromium etch step.

The varying silicon compositions of the gold–silicon liquid catalyst during growth and nucleation of silicon crystallites from the gold–silicon system in the micro–crucibles can be described using Figure 3–6. The growth process in micro–crucibles starts with pure, solid gold at the processing temperature (T_p) just before silane is introduced into the system. As the gas flows and cracks at the gold surface, silicon dissolves into the gold, the silicon concentration in the gold–silicon catalyst increases, the solid gold partially liquefies and the silicon concentration increases along the blue dotted line to the right. As the blue dotted line crosses the gold liquidus curve the micro–crucible contents completely transform into a liquid and the silicon concentration continues to increase until reaching the silicon liquidus curve. Upon reaching the silicon liquidus curve, it is thermodynamically favorable for the dissolved silicon to form a faceted crystalline phase, but first must overcome the energy barrier required to form a second phase. This is accomplished by supersaturating the eutectic liquid (the red dashed line in Figure 3–6) to the critical supersaturation concentration (X_{crt}), at which a silicon crystallite nucleates [17]. Excess silicon, represented by the red dashed line, in the gold–silicon liquid is incorporated into the crystalline silicon phase when the crystallite nucleates and the liquid phase returns to its equilibrium composition, which is represented in Figure 3–6 as point E. The crystallite continues

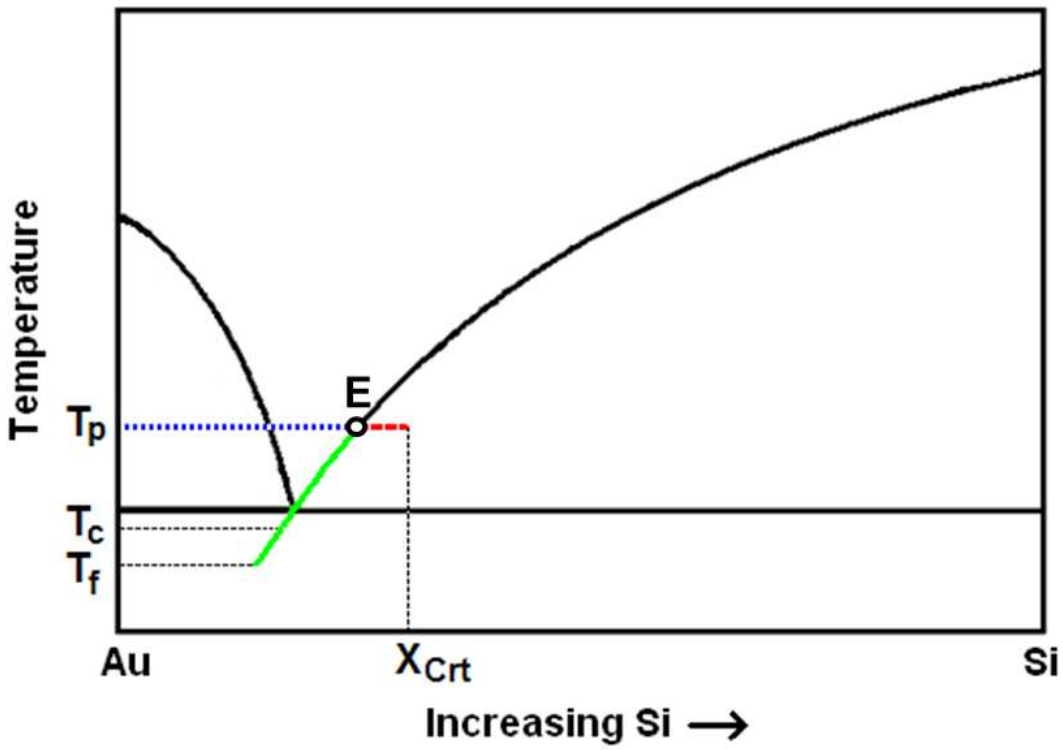

Figure 3–6: A schematic of the Au–Si phase diagram which depicts the compositional variations in the micro–crucibles with fine and coarse lamellar structures as they are processed. The dotted blue line represents the gradual increase in Si concentration in the Au catalyst during deposition. The dashed red line represents the additional supersaturation required in the Au–Si liquid solution to nucleate a Si crystallite. The concentration at which a Si crystallite is nucleated is the critical supersaturation (X_{crt}). Point E represents the steady state composition after the faceted crystallite phase has nucleated. The solid green line represents the composition of the liquid Au–Si solution as it cools from the processing temperature (T_p) to its final undercooled temperature. The different temperatures at which the Au–Si liquid solutions solidify with fine and coarse lamella (T_f and T_c respectively) and their respective silicon concentrations determine the ΔV between Si crystallites in micro–crucibles with coarse and fine lamellar morphologies.

to grow at a given rate until the silane flow is stopped. Upon cooling the composition of the liquid follows the silicon liquidus curve, represented by the solid green line, and the excess silicon from the liquid phase is incorporated into the crystalline silicon phase due to the changing equilibrium concentration at cooler temperatures. At some amount of undercooling the liquid gold–silicon phase will freeze and form irregular lamella of nearly pure gold and silicon phases.

The micro–crucibles with fine lamella have a larger average silicon crystallite volume and a smaller standard deviation than the crucibles with coarse lamella, which makes them more reproducible and useful for nucleation analysis. The normal distribution spread in Figure 3–5 can be explained through varying catalytic surface areas. As silicon is incorporated into the gold catalyst and crystallites nucleate, the catalyst is displaced within the crucible and the geometry of the gold–vapor interface changes from a planar to a bowed surface (seen in the right crucible of Figure 3–2B). This change in surface geometry can vary the rate of silicon dissolving into the gold up to $\pi/2$ times the initial planar surface for an assumed semi–circular gold–vapor surface. Another source of statistical variation is the different incubation times [115, 110] required before the initial silicon nucleation event which is related to the different catalyst volumes. Larger initial volumes of gold require more silicon to achieve critical supersaturation. This delays the initial nucleation and growth of silicon crystallites for a constant deposition rate, traps more of the deposited silicon in the liquid gold–silicon phase and thus skews the silicon crystallite volume measurements to smaller values for larger initial gold volumes.

The difference in the average silicon crystallite volumes ($2.01\,\mu m^3$ vs $1.45\,\mu m^3$) for fine and coarse lamellar structures can be understood through the greater undercooling experienced by gold–silicon liquids which solidified with fine lamella. It has been shown that for gold–silicon alloys there is a decrease in the solubility of silicon in the liquid at greater undercoolings and that gold–silicon liquids can be significantly undercooled before solidifying [116]. An undercooled liquid is generally assumed to take the composition of the solute liquidus line extrapolated as it is cooled into the two–phase, gold plus silicon field [171], which is represented in the gold–silicon system by the extrapolated solid green silicon liquidus line shown in Figure 3–6.

Because of the limited solid–state solubility of silicon in gold and gold in silicon, the undercooling of a micro–crucible with a fine lamellar solid relative to a micro–crucible with a coarse lamellar solid can be estimated simply with three assumptions. The first assumption is that the number of atoms of gold in the micro–crucibles with fine and coarse lamella is equal and that each micro–crucible has received the same dosage of silicon through the chemical vapor deposition process i.e. the total number of silicon atoms is equal in the micro–crucibles associated with both microstructures. This is not an entirely accurate assumption, but through the use of statistics the difference between the two can be averaged. The second assumption is that prior to the liquid solidifying, crucibles with fine or coarse lamella have achieved critical supersaturation (Figure 3–6) and have nucleated faceted crystallites of equal size (Figure 3–7A1 and B1). The third assumption is that the composition in the liquids in both the fine and coarse crucibles is the same at eutectic temperature. The difference in the final size of faceted silicon phase in the different micro–crucibles

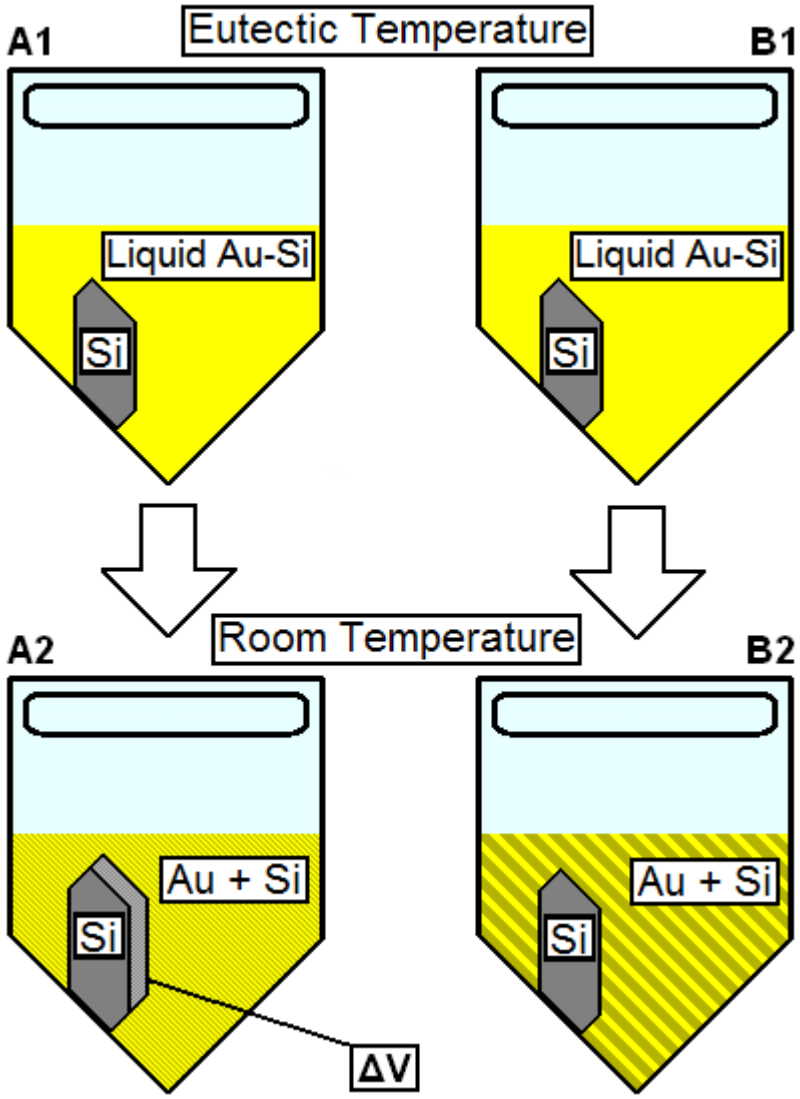

Figure 3–7: Diagram of the effects of relative undercooling on silicon crystallite size. The averaged micro–crucible with fine (A) and coarse (B) lamella starts off with the same initial conditions (A1 and B1). Upon cooling, the additional rejected silicon atoms from the more undercooled liquid in the crucible with fine lamella deposit themselves onto the silicon crystallite and give it additional volume (ΔV).

arises when the micro–crucibles are undercooled from the eutectic point into the gold plus silicon, two–phase region and the crucible with fine lamella experiences a greater undercooling, solidifying at T_f, while the crucible with coarse lamella solidifies at T_c (Figure 3–6). This causes more silicon atoms in the liquid of the fine lamella crucibles to deposit onto the already nucleated crystallite than silicon atoms in the liquid eutectic of the coarse lamella crucibles in an attempt to equilibrate the system at its undercooled temperature. Upon solidification there is a difference in the number of silicon atoms in fine and coarse silicon lamella as well as in their faceted crystalline silicon phase due to the different equilibrium silicon concentrations at their respective undercooling temperatures (Figure 3–6). With the aforementioned assumptions in mind, the difference in the amount of silicon atoms in the faceted crystalline silicon phase between crucibles with fine and coarse lamella corresponds to the difference in volume between the silicon crystallites nucleated in the crucibles with fine and coarse lamella (ΔV in Figure 3–7A2) and is given by the following equation:

$$\Delta V = V_{fine} - V_{coarse} = \Delta N_{Si}^{La} \times \rho_{Si} \tag{3.1}$$

where V_{fine} and V_{coarse} are the volumes of the silicon crystallite from the micro–crucibles with fine and coarse structured lamella, respectively, ΔN_{Si}^{La} is equal to the difference in the number of silicon atoms in the gold–silicon lamellar solid at room temperature for micro–crucibles with fine and coarse eutectic lamella and ρ_{Si} is the atomic density of silicon. Seeing that ΔV is measured and ρ_{Si} known, ΔN_{Si}^{La} can be

calculated for the micro–crucibles. Knowing the difference in the number of silicon atoms in the fine and coarse lamellar solids allows one to calculate the change in silicon concentrations ($\Delta at\%_{Si}^{La}$) of the lamellar solid between micro–crucibles with fine and coarse structured lamella using the following equations:

$$at\%_{Si_{fine}}^{La} = N_{Si_{fine}}^{La}/(N_{Au} + N_{Si_{fine}}^{La}) \tag{3.2}$$

$$at\%_{Si_{coarse}}^{La} = N_{Si_{coarse}}^{La}/(N_{Au} + N_{Si_{coarse}}^{La}) \tag{3.3}$$

$$\Delta N_{Si}^{La} = N_{Si_{coarse}}^{La} - N_{Si_{fine}}^{La} \tag{3.4}$$

$$\begin{aligned} \Delta at\%_{Si}^{La} &= at\%_{Si_{coarse}}^{La} - at\%_{Si_{fine}}^{La} \\ &= N_{Si_{coarse}}^{La}/(N_{Au} + N_{Si_{coarse}}^{La}) - N_{Si_{fine}}^{La}/(N_{Au} + N_{Si_{coarse}}^{La} - \Delta N_{Si}^{La}) \end{aligned} \tag{3.5}$$

where $at\%_{Si_i}^{La}$ is the atomic percentage of silicon of the i$^{\text{th}}$ (fine or coarse) species in the lamellar solid, $N_{Si_i}^{La}$ is the number of silicon atoms in the gold–silicon lamellar solid at room temperature for the i$^{\text{th}}$ species and N_{Au} is the number of initial gold atoms. Equations 3.2 and 3.3 are the equations for atomic percentage and Equation 3.4 is the definition of ΔN_{Si}^{La}. The $\Delta at\%_{Si}^{La}$ term is the atomic percent of silicon in the lamellar solid of a micro–crucible with a coarse structured lamella minus that in the fine lamellar micro–crucible defined by Equation 3.5. Assuming ΔN_{Si}^{La} is small compared to $N_{Au} + N_{Si_{coarse}}^{La}$, Equation 3.5 simplifies to:

$$\Delta at\%_{Si}^{La} = \Delta N_{Si}^{La} / (N_{Au} + N_{Si_{coarse}}^{La}) \tag{3.6}$$

Using the observed ΔV in this experiment ($0.56\,\mu m^3$), one can calculate the $\Delta at\%_{Si}^{La}$ between the micro–crucibles with fine and coarse structured lamella, which was 4.2 percent in this experiment. The small value for $\Delta at\%_{Si}^{La}$ validates the assumption that ΔN_{Si}^{La} is small compared to $N_{Au} + N_{Si_{coarse}}^{La}$. Assuming the lamellar solids with coarse lamella underwent insignificant undercooling and have a composition very close to the eutectic of 18.6 75% [22], the value for $\Delta at\%_{Si}^{La}$ results in an estimated fine structured composition of 14.4 at% silicon, which corresponds to a freezing temperature for micro–crucibles with the fine lamellar structure of about 235 °C when extrapolated along the silicon liquidus line of the gold–silicon system, and an undercooling of at least 130 Celcius from the eutectic temperature. While this may seem like a large undercooling, 120 Celcius was reported for gold–silicon freezing on a silicon {111} surface [116].

In addition to understanding how faceted silicon crystallites are nucleated, understanding how the gas phase diffuses into the micro–crucibles is critical for controlled lateral growth of silicon thin–films. Similar crystallite volumes found in the two populations which had different silane diffusion distances (17.5 and 25.5 micrometers) are supported by previously published works [15, 137] where there appeared to be no significant difference between silane concentrations at the mouth of the micro–crucible and at the gold–vapor interface for LPCVD processes for distances

up to 25 micrometers for 200 nanometer diameter pores. The crucibles with fine eutectic structures were used to determine the diffusion distance results due the smaller standard deviation and the low number of crucibles which had coarse lamellar morphologies at 25.5 micrometer diffusion lengths. As there was no measurable difference between crystal growth with diffusion distances 17.5 and 25.5 micrometers for crucibles with fine eutectic structures, there is a strong likelihood that silane reactions at the gold–vapor surface are surface reaction limited, and not gas phase transport for the used experimental conditions.

3.1.6 Conclusions

A new technique for nucleating and observing silicon crystallites in confined geometries over amorphous substrates has been demonstrated. These crystallites act as the seeds for the laterally grown films within the confined geometries. It was shown that through proper engineering of the micro–crucible structure, consistent measurements on nucleation, crystal growth and solidification can be made. An interesting result of the experiment was the effect the residual chromium adhesion layer had on the solidification of the gold–silicon lamellar structure in the micro–crucibles, where different undercoolings for similar micro–crucibles are believed to have occurred due to the residual chromium. Statistical analysis of crystallite volumes shows Gaussian distributions, but careful sampling needs to be used so as to not have the data skewed by the varying crystallite nucleation incubation periods associated with the varying volumes of gold catalyst present in the micro–crucible populations. Using the average difference in silicon crystalline volume between micro–crucibles with fine and

coarse lamellar structures, an estimated undercooling from the eutectic temperature of 130 Celcius was calculated in the crucibles with fine lamella.

3.1.7 Acknowledgments

The authors would like to thank McGill University and NSERC for funding this research, Dr. Manas Paliwal for a useful conversation on non–equilibrium solidification and Dr. David Liu for aid with TEM imaging.

3.2 Observations on the preferred orientation of laterally grown silicon films over amorphous substrates using the VLS process

3.2.1 Abstract

A novel method has been optimized so that adhesion layers are no longer needed to reliably deposit patterned gold structures on amorphous substrates. Using this technique allows for the fabrication of amorphous oxide templates known as micro–crucibles, which confine a vapor–liquid–soild catalyst of nominally pure gold to a specific geometry. Within these confined templates of amorphous materials, faceted silicon crystals have been grown laterally. The novel deposition technique, which enables the nominally pure gold catalyst, involves the undercutting of an initial chromium adhesion layer. It was found that silicon nucleated in these micro–crucibles were 30% single crystals, 45% potentially twinned crystals and 25% polycrystals for the experimental conditions used. Single, potentially twinned, and polycrystals all had an aversion to growth with the {1 0 0} surface parallel to the amorphous substrate. Closer analysis of grain boundaries of potentially twinned and polycrystalline samples revealed that the overwhelming majority them were of the 60° $\Sigma 3$ coherent twin boundary type. The large amount of coherent twin boundaries present in the grown, two–dimensional silicon crystals suggest that lateral VLS growth occurs very close to thermodynamic equilibrium. It is suggested that free energy fluctuations during growth or cooling, and impurities were the causes for this twinning.

3.2.2 Introduction

Integrating non–standard CMOS channel materials onto silicon substrates such as III–V and germanium thin–films remains a long term goal of the International Technology Roadmap for Semiconductors. A potential enabler of such technology is

high–quality lateral growth of non-classical materials over an amorphous substrate using the vapor–liquid–solid (VLS) technique [133], where high–quality semiconductors can be selectively grown on regions of silicon wafers which have oxide films. One particular aspect of lateral growth, and it integration into CMOS technology, is controlling the crystallographic orientation of the grown films, which is not a straight forward task when these films are grown unseeded.

For VLS grown silicon nanowires on silicon substrates it is known that there is a distribution of crystallographic directions in which the nanowires grow epitaxially from a substrate surface and that this distribution is dependent on the size of the initial gold catalyst [113] [107] [106]. While useful to understand, typically it is more useful when integrating nanowires into electronic devices to control the spatial location of nanowire growth [16] [142] [74] [80] rather than the crystallographic orientation of the nanowires. This is not the case for high–quality two–dimensional VLS growth, as crystallographic orientation will affect the electronic properties of integrated devices [140] and the epitaxial growth using the two–dimensional lateral growth as a seed [172]. Here investigations of the orientation and quality of spatially controlled, two–dimensional, laterally grown silicon films using the VLS technique will be further explored and explained.

To enable lateral, two–dimensional growth over amorphous substrates a specialized amorphous test structure, termed a micro–crucible [172], has been developed using standard microfabrication techniques. Two micro–crucibles have been fabricated for this work, one with a single opening (Figures 3–8A1 and A2) and one with two openings (Figures 3–8B1 and B2). General fabrication of these crucibles is done

by patterning a gold film on of an amorphous substrate and encapsulating it with PECVD silicon oxide (Figures 3–8A1 and B1). Areas of the encapsulation layer are selectively etched so that the encapsulated gold and can be partially etched out of the micro–crucible templates using wet chemistries (Figures 3–8A2 and B2).

Two–dimensional growth is achieved when the micro–crucible test structure is processed using chemical vapor deposition (CVD), where, at an elevated temperature, a reactive gas, which for these experiments was silane, diffuses into the micro–crucible and preferentially reacts at the gold catalyst surface exposed to the vapor phase. Silane continues to react at the gold–vapor interface and the concentration of the silicon in VLS catalyst continues to increase until a critical silicon concentration is reached and a faceted silicon phase is formed within the confines of the micro–crucible. The geometry of the micro–crucible restricts the growth to two dimensions and the faceted silicon phase continues to grow laterally until the flow of reactive silicon precursor is turned off and the gold–silicon system equilibrates at room temperature.

The most accurate way to determine orientation of semiconductor growth on amorphous substrates is through x-ray diffraction, but because of the out–of–plan growth associated with VLS growth techniques, it is seldom used for analyzing nanowires. Instead, nanowire growth and orientation are analyzed using transmission electron microscopy (TEM) due to their intrinsic electron transparency and high growth density, but with the requirement that the wires are typically removed from their substrate to facilitate imaging. As an alternative to TEM for analyzing VLS growth, electron backscatter diffraction (EBSD) techniques have been developed for

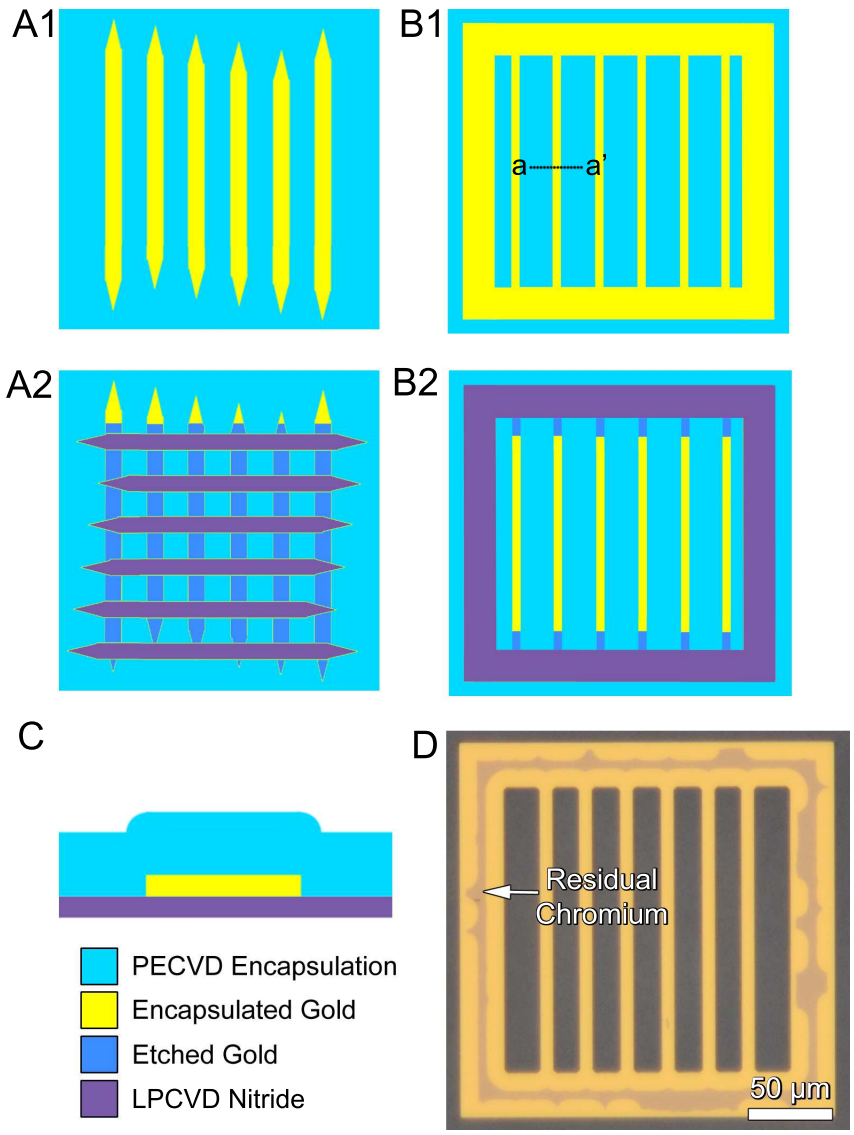

Figure 3–8: A1 and A2 are diagrams of the single sided micro–crucible pre–structure and of the micro–crucible geometry after the selective removal of gold respectively. B1 and B2 are diagrams of the doubled sided micro–crucible pre–structure and of the micro–crucible geometry after the selective removal of gold respectively. Figure 3–8C is a cross section of the micro–crucible structure at location a–a' as depicted in Figure 3–8B1. Figure 3–8D is an optical image showing the successful undercut etching of Cr from a micro–crucible pre–structure. The residual chromium ring around the central structure secures the gold structure to the amorphous substrate. Figure 3–8D was taken from the backside of a fused silica wafer.

nanowire growth [161] [162] which give crystallographic orientation information and allows the grown nanowires to be imaged attached to their substrates. These EBSD techniques have been extended to laterally grown nanowires [142] and films [140] to determine the single–crystalline quality of the growth and here the authors use of EBSD to determine the quality and the preferred orientation of laterally grown two–dimensional silicon films.

While offering the benefits of the ease of use that a scanning electron microscope (SEM) offers, EBSD has some limitations when compared to TEM and x-ray diffraction techniques when determining crystallographic orientation and acts somewhat as an intermediate between the two [160]. Notable for this experiment was the inability to collect x-ray diffraction data due to the sparseness of the nucleated faceted silicon phase on the surface of the substrates and the larger interaction volume of the x-rays with the substrate compared to the 100 nanometer thick device layer, resulting in strong peaks associated with the silicon substrate. Thus EBSD analysis was used to determine the orientation og grown lateral crystals, but EBSD angular resolution error, which for this experiment was believed to be $\pm 1^{\circ}$, is greater than the error associated with x-ray diffraction. This error with EBSD measurements is not detrimental to preferred orientation calculations, but causes ambiguity when measuring the misorientation between neighboring grains and changes the interpretation of the nature of the grain boundary between the two crystals significantly. More exact misorientation measurements from individual grains and direct observation of the grain boundary can be achieved with high resolution TEM and convergence beam electron diffraction, but require difficult sample preparation, specialized software to interpret

the diffraction/Kikuchi patterns, and the number of observable misorientated grains would be statistically irrelevant.

For this experiment, silicon crystals were grown in previously reported micro–crucible designs [172], as well as newly designed double ended micro–crucible test structures, which are similar to the templates used by Shan et al. [16], but optimized to control two-dimensional growth. The purpose of the new design is to provide a more reliable technique for depositing patterned gold on to an amorphous substrate without the use of adhesion layers like chromium or titanium, which have been shown to change the nucleation characteristics of silicon in micro–crucibles [172].

3.2.3 Experimental

Silicon {111} substrates with 100 nanometers of low–pressure chemical vapor deposition (LPCVD) low–stress nitride were cleaned in a 1:3 by volume 35 % H_2O_2 : 97 % H_2SO_4 piranha solution for 10 minutes at 80 °C, rinsed in deionized (DI) water and dried. In a vacuum of at least 5.5×10^{-6} Torr, 5 nanometers of a chromium adhesion layer followed by 150 nanometers of gold were deposited on the substrates with an electron beam evaporator.

Following the metal deposition, a 1.4 micron layer of MicroChem S1813 photoresist was deposited, patterned with micro–crucible test structures the shape of Figures 3–8A1 and B1, exposed and developed. The patterned substrates were placed into concentrated Transene Gold Etchant TFA and solution was hand agitated for 30 to 45 seconds and the substrate removed when the test structures became visible. Following the gold etch, the substrates were placed in a concentrated solution of

Transene Chromium Etchant 1020 and hand agitated for 1 to 2 minutes in order to remove most of the underlying adhesion layer.

The photoresist was stripped in successive, room temperature baths of acetone, Microprosit Remover 1165, IPA and DI water for 10, 10, 5 and 5 minutes respectively. The solvents were not agitated so as not to damage the sensitive micro–crucible test structures. Before being encapsulated with 500 nanometers of PECVD silicon oxide, the substrates were oxygen plasma cleaned for 30 seconds at 150 Watts.

A layer of AZ5214-E photoresist was spun on top of the encapsulated substrate and processed as per the manufacturer's instructions. This photoresist defined the areas of the substrate where the encapsulation over the gold structures was selectively removed to open the micro–crucibles using a low power SF_6 reactive ion etch, which allowed for the partial etching of the encapsulated gold. The opened structures were etched in a 50 °C Transene Gold Etchant TFA bath until the desired amount of gold remained in the micro–crucible amorphous growth templates (Figures 3–8A2 and B2).

The micro–crucible test structures were left overnight prior to chemical vapor deposition growth in concentrated H_2SO_4 to remove any hydrocarbons and residual photoresist. Just before being placed in the CVD chamber, the substrates were cleaned in a self-heated 1:3 piranha solution for 10 minutes for one last cleaning. The wafers were processed in a hot–walled, low–pressure chemical vapor deposition (LPCVD) reactor for 60 and 180 minutes, at temperatures of 450 °C and 475 °C, a pressure of 420 mTorr and gas flow rates of 150 sccm of SiH_4 and 900 sccm of N_2

(20 mTorr pp_{SiH_4}). After deposition the quartz boat holding the wafers was directly removed from the furnace at the processing temperature and allowed to cool in air.

The remaining encapsulation layer was removed by a combination of reactive dry etching with CHF_3 and wet etching with a 1:6 Buffered Oxide Etchant, which allowed for high resolution scanning electron microscope imaging and electron backscatter diffraction analysis of the growth which occurred in the micro–crucible templates. The Euler angles of the known silicon substrate were used to correct for any misalignment in the EBSD components.

3.2.4 Results

The pre–structures of single and double sided micro–crucibles are depicted in Figures 3–8A1 and B1. The micro–crucible structure after the gold has been selectively etched out of the micro–crucible is depicted in Figures 3–8A2 and B2. The purpose of the 1 to 2 minute chromium etch in the Chromium Etchant 1020 bath was to produced a device structure which did not have a chromium adhesion layer underneath the gold catalyst layer, as depicted in Figure 3–8C. The results of the chromium undercut etch are imaged in Figure 3–8D, where it appeared that chromium adhesion layer was successfully undercut from beneath the central portion of the patterned gold leaving a nominally pure gold catalyst for VLS growth. The removal of the chromium layer was more reliable in the double sided micro–crucible because the special design of the pre–structures, which anchored the micro–crucibles to the substrate with a ring of chromium residue (Figure 3–8D). Single sided micro–crucibles tended to lift off when the chromium undercut was too aggressive. There was no

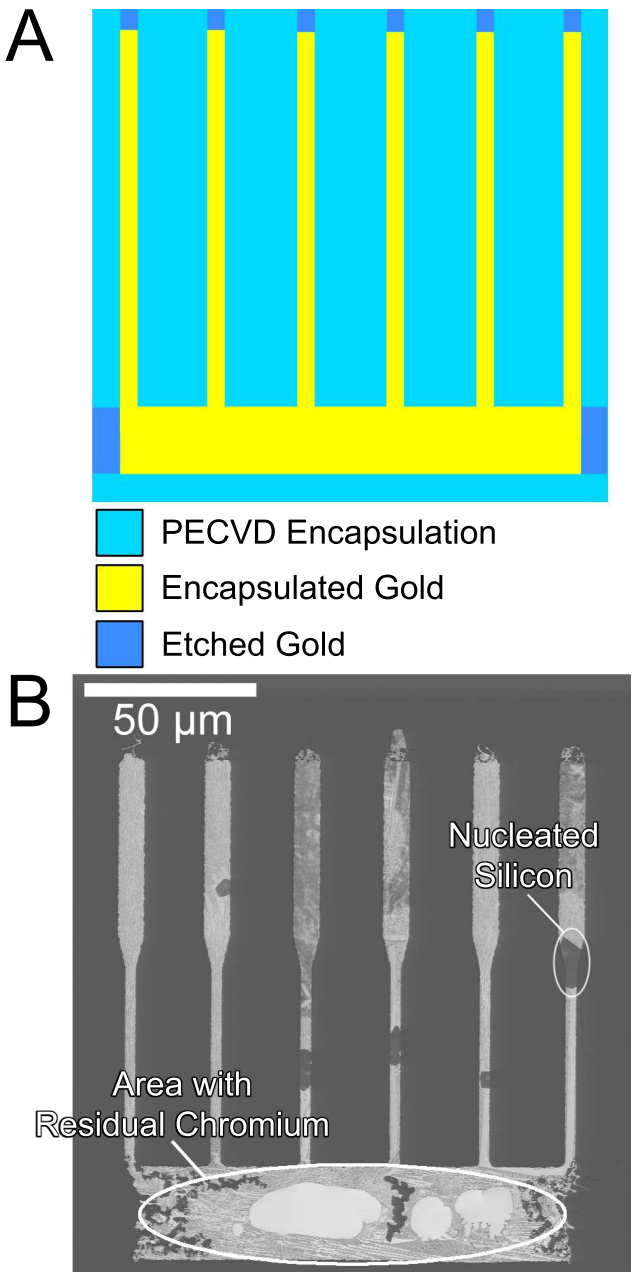

Figure 3–9: (A) A plan view diagram of the double ended micro–crucible test structure with an altered geometry used for the 475° C, 180 minute growth and (B) a backscattered electron image the results of the growth showing nucleated crystals conforming to the micro–crucible.

appearance of deformation in the pre–structure patterned gold films after being encapsulated with PECVD oxide when observed in a dark field microscope, allowing for reliable partial wet etching of the gold films out of the micro–crucible.

Figure 3–9A depicts a structure used for the experimental growths at 475 °C for 180 minutes and Figure 3–9B images the results of such an experiment. Crystals nucleated preferentially in the thinner, necked region of the double sided micro–crucible in Figure 3–9B. All of the faceted silicon crystals in Figure 3–9B appeared to have nucleated heterogeneously at the interface between the LPCVD nitride substrate and the PECVD oxide encapsulation layer within the bulk of the VLS catalyst.

Figure 3–10A is a high resolution image of the silicon growth circled in Figure 3–9B, with Figures 3–10B and 3–10C depicting the potential twinning of the silicon growth from Figure 3–10A with an EBSD band contrast map (Figure 3–10B) and an EBSD band contrast map overlayed with the Euler angle map (Figure 3–10C). The band contrast map is a measurement of the sharpness/indexing confidence of the Kikuchi patterns of a scanned area. White represents a well defined crystalline area and black represents an amorphous region or an area which had multiple or undefined Kikuchi patterns, such as grain boundaries. The Euler angle map is colored to highlight grains of different orientations with respect to an arbitrary reference orientation. Upon closer inspection with electron backscatter imaging (Figure 3–10D) there appeared to be some kind of impurity or defect present at the triple point of the grains labeled i, ii and iii.

Silicon crystals which were grown for 60 minutes at 450 °C in single sided micro–crucibles were analyzed using EBSD and were classified as either being single crystal,

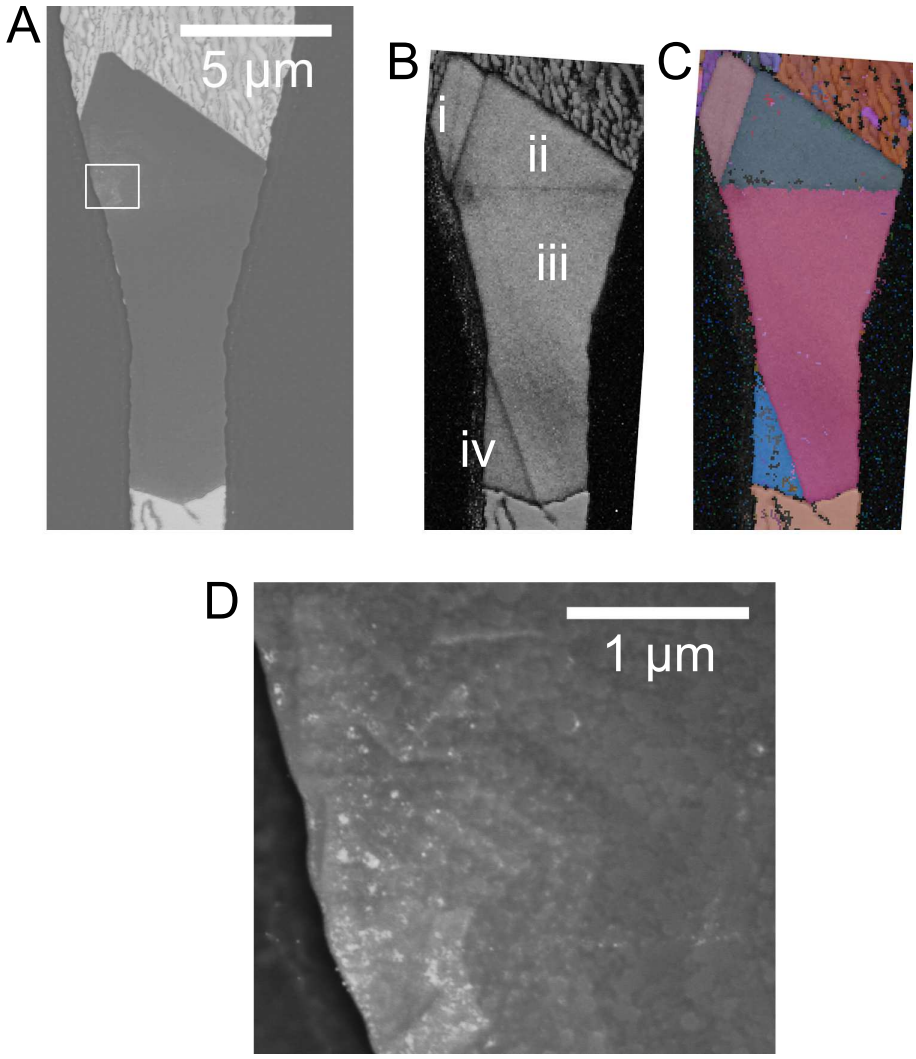

Figure 3–10: Growth of a faceted silicon phase confined within the micro–crucible circled in Figure 3–9B. Figure 3–10A is backscatter electron micrograph of the region of interest. Figures 3–10B and 3–10C image the twinned silicon growth from 3–10A with an EBSD band contrast map and an EBSD band contrast map overlayed with the Euler angle map respectively. Figure 3–10D is a high magnification image of the area boxed in Figure 3–10A. The orientations of the grains labeled i, ii , iii and iv in Figure 3–10B are slightly off the {2 1 1}, slightly off the {2 1 1}, the {4 1 1} and slightly off the {1 1 0} planes respectively. All angle/axis pairs were found to be $60°/\langle 1\ 1\ 1\rangle$.

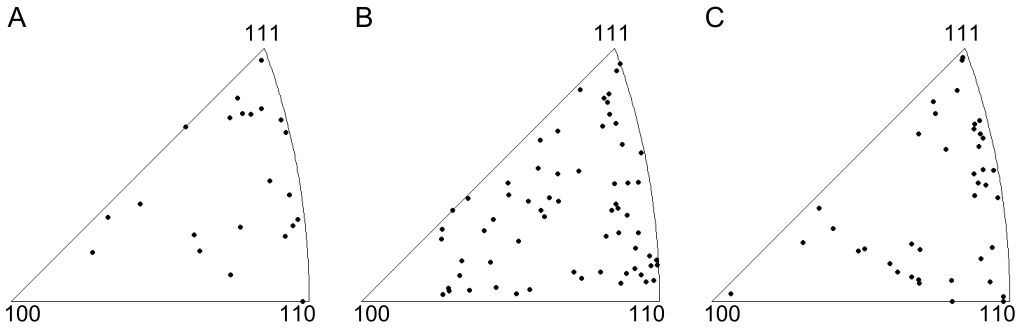

Figure 3–11: Inverse pole figures of observed orientation of nucleated silicon crystals with respect to the normal of the substrates for (A) single, (B) potentially twinned and (C) polycrystals.

potentially twinned or polycrystals. Of the 68 independently nucleated crystals observed, 30% were single crystals, 45% were potentially twinned crystals and 25% were polycrystals. Single crystals were classified as such when a micro–crucible had one faceted silicon nucleation event and that crystal was of a single orientation. Potentially twinned crystals were classified as such when a micro–crucible had one faceted silicon nucleation event and crystalline grains were of multiple orientations, typically two, but had continuous and geometric relations to one another i.e. symmetry or parallel boundaries. Polycrystals were classified as such when a micro–crucible had multiple faceted silicon nucleation events and/or crystalline grains of multiple orientations were nucleated without symmetry.

All of the crystal classifications had an aversion to growing with the {1 0 0} orientation parallel to the substrate (Figure 3–11) and a preference for growth between the {1 1 1} and {1 1 0} orientations was observed for single and polycrystals (Figure 3–11A and C). Due to an over aggressive CHF_3 dry etch to removed the encapsulation layer, the micro–crucibles imaged in Figures 3–12, 3–13 and 3–14 have had

their gold–rich phases removed. Figure 3–12A, 3–13A and 3–14A are backscattered electron micrographs where the the gold–vapor interface is found on the left side of the image and tapered end of the micro–crucible on the right. The tapered ends of single sided micro–crucibles are depicted as the top points in on the top of Figure 3–8A. The typical morphology of a grown single crystal is depicted in Figure 3–12C, where the faceted growth was six sided and the orientation of the crystal surface parallel to the amorphous substrate was close to $\{1\ 1\ 1\}$. Twinned crystals were found to have multiple morphologies, two of which are depicted in Figures 3–13C and 3–14C. Figure 3–13C represents twinned growth which formed with a major grain which accounts for the majority of crystal, and a minor grain. Figure 3–14C represents twinned growth which formed with without a major grain. Single crystals were found to have almost exclusively nucleated at the gold–vapor interface or enveloped by the gold–rich phase, near the interface of the LPCVD nitride substrate and PECVD oxide encapsulation layer around the perimeter of the micro–crucible.

The most frequent for misorientation angles observed between neighboring grains were the angle/axis pairs $60°/\langle 1\ 1\ 1\rangle$, $70.5°/\langle 1\ 1\ 0\rangle$, $131.8°/\langle 2\ 1\ 0\rangle$, $146.4°/\langle 3\ 1\ 1\rangle$, and $180°/\langle 2\ 1\ 1\rangle$. The most frequently observed angle/axis pairs correspond to $\Sigma 3$ grain boundaries [151] in coincident site lattice (CSL) terminology. The CSL model uses the visual concept of two interpenetrating lattices of different orientations, where the parameter Σ has the value of the reciprocal density of lattice sites which the two interpenetrating lattices hold in common. When crystallographic symmetry is taken into account, the minimum of all equivalent misorientation angles can be computed [153], and this minimized misorientation is typically retitled as disorientation so as

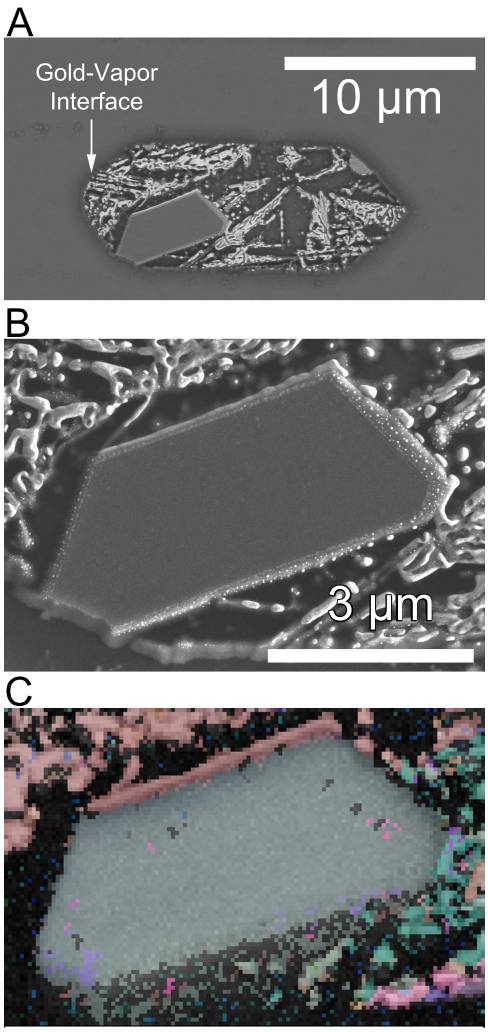

Figure 3–12: Typical single crystal growth after 60 minutes of deposition. Figure 3–12A represents twinned growth which formed with a major grain which accounts for the majority of crystal, and a minor grain. Figure 3–12B is a high magnification backscatter image of the nucleated crystal. Figure 3–12C is a composite image of the EBSD band contrast map with the Euler angle map superimposed over it. The orientation of the imaged crystal facet is slightly off from the {3 2 2} plane.

not to confused it with generalized misorientation. A distribution of the observed disorientation between all observed grain boundaries was obtained using the MTEX quantitative texture analysis toolbox for MATLAB and is reported in Figure 3–15. Eighty–six percent of the computed disorientations for the observed grain boundaries for crystals grown for 60 minutes at 450 °C and for 180 minutes at 475 °C resolved to be $60°/\langle 1\ 1\ 1\rangle$ coherent twin grain boundaries. $60°/\langle 1\ 1\ 1\rangle$, otherwise known as $60°\ \Sigma 3$, boundaries are classified as coherent twin boundaries because the boundary plane is a mirror plane between the two lattices and it is believed that no dislocations or dangling bonds are present at their interface [173].

3.2.5 Discussion

As can be seen in Figure 3–8D, by using a novel design, micro–crucibles which contain gold that has not been alloyed with its adhesion layer can be successfully fabricated. Unfortunately due to the slow growth attributed to the necessary experimental conditions, the design had to be altered from the ideal double ended micro–crucible layout (Figure 3–8B2) to a geometry which maximized the initial gold–vapor interface to gold volume ratio (Figure 3–9A). This geometrical change was accomplished by shifting the alignment of the photomask. The maximization was needed so as to dissolve enough silicon into the gold catalyst to create a critical silicon supersaturation condition of the gold–silicon solution and promote the formation of the faceted silicon phase. Tests using the ideal structure in Figure 3–8B2 with similar experimental conditions resulted in no nucleation of the faceted phase. Because the deposition process lies in the surface reaction limited regime, attempts

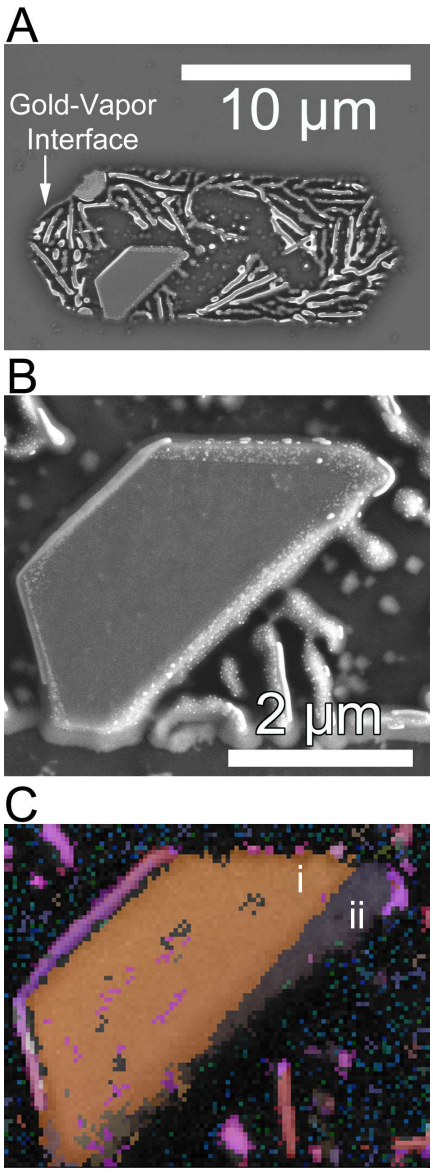

Figure 3–13: Typical twinned crystal growth after 60 minutes of deposition where one grain is significantly larger than the other. Figure 3–13A is a backscatter electron micrograph depicting the condition of the micro–crucible in which the crystal nucleated. Figure 3–13B is a high magnification backscatter image of nucleated crystal. Figure 3–13C is a composite image of the EBSD band contrast map with the Euler angle map superimposed over it with areas of different colors/shades representing grains of different orientations. The orientations of the larger and smaller twinned grains are the {7 7 1} and sightly off the {10 3 1} planes respectively. Their angle/axis pair was measured to be $60°/\langle 1\ 1\ 1\rangle$.

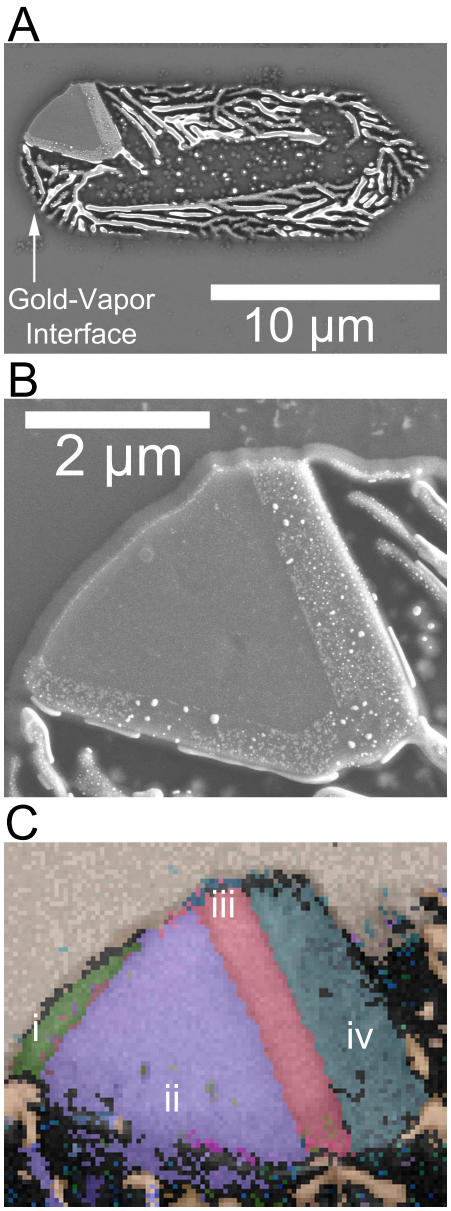

Figure 3–14: Typical twinned crystal growth after 60 minutes of deposition where no grain was significantly larger than the others. Figure 3–14A is a backscatter electron micrograph depicting the condition of the micro–crucible in which the crystal nucleated. Figure 3–14B is a high magnification backscatter image of nucleated crystal. Figure 3–14C is a composite image of the EBSD band contrast map with the Euler angle map superimposed over it with areas of different colors/shades representing grains of different orientations. The orientations of the grains labeled i, ii , iii and iv are slightly off the $\{5\ 5\ 1\}$, the $\{7\ 7\ 1\}$, slight off the $\{5\ 2\ 2\}$ and the $\{7\ 6\ 5\}$ planes respectively. All angle/axis pairs were found to be $60°/\langle 1\ 1\ 1\rangle$ except between the grains labeled i and ii, which was one of the two $38.9°/\langle 1\ 1\ 0\rangle$ $\Sigma 9$ grain boundaries observed in this experiment.

to increase the silicon growth rate by increasing the temperature resulted in the uncontrolled growth of nanowires within the micro–crucible and uncatalyzed growth. This uncatalyzed growth blocked silane from diffusing into the micro–crucible and reacting at the gold–vapor interface.

Changing the micro–crucible structure from the ideal geometry introduced chromium contamination into the gold VLS catalyst from chromium residue ring pictured in Figure 3–8D. It known the chromium contamination effects the solidification of the gold–silicon catalysts and the final morphology of the faceted silicon phase [172], but here it can also be seen that the residual chromium does not induce nucleation as there are no faceted crystals near where the chromium residue was located (Figure 3–9B). What did appear to affect faceted nucleation was the presence of an impurity or surface defect which can be seen in Figures 3–10A and 3–10D. This proposed impurity or defect was located at the triple point of grains i, ii and iii as labeled in Figure 3–10B. Closer inspection of Figures 3–10B and C shows linear defects in grains i and iii which emanated from proposed impurity/defect site. Because these linear defects do not change the orientation of the grain, it is suggestive that these are stacking faults. The grain boundaries between crystals i, ii and iii in Figure 3–10, which were generated by the potential impurity or defect, were all of the $60°/\langle 1\ 1\ 1\rangle$ coherent twin type. This suggests that even with the presence of impurities or surface defects, two–dimensional lateral growth of silicon films using the VLS process occurred slowly enough and close enough to thermodynamic equilibrium that lowest energy grain boundary configurations could be achieved in perturbed systems.

The presence of the {1 1 1} and {1 1 0} preferred orientations and an aversion to the {1 0 0} orientation found in Figure 3–11 was not surprising as their respective surface energies for silicon are 1.237×10^{-4}, 1.515×10^{-4}, and 2.142×10^{-4} J/cm^2 [174] and thus, for two–dimensional growth of silicon crystals, there appears to be an incentive for the crystals to grow with orientations where the planes of lowest surface energy are parallel to the substrate, minimizing the free energy of the system.

The crystals nucleated in Figures 3–12B, 3–13B and 3–14B all appear to be in contact with either the gold–vapor surface or the interface of the LPCVD nitride substrate and the PECVD oxide encapsulation layer around the perimeter of the micro–crucible. There were no observed faceted silicon phases which nucleated in the bulk of the VLS catalyst which did not also contact one of these surfaces. This suggests that all events which resulted in the nucleation of stable facet silicon crystals are heterogeneously nucleated. For nucleation rates as slow as the ones observed in the VLS lateral growth of two–dimensional silicon films, homogeneous nucleation is not expected, but the patterns observed where crystals tend to nucleate at higher energy surfaces indicate that there should be different critical silicon supersaturations required for different heterogeneous nucleation events. As observed in these experiments, there are three predicted, distinct heterogeneous nucleation events, namely nucleation a the gold–vapor interface (Figure 3–12B), nucleation in the bulk of the VLS catalyst at the interface of the LPCVD nitride substrate and the PECVD oxide encapsulation layer (Figure 3–13B) and nucleation induced by an impurity or surface defect (Figure 3–10D). Unfortunately the current experiment is not sophisticated enough to determine the energy barrier needed to be overcome for

these different heterogeneous nucleation events to occur, but it can be concluded that the energy difference between nucleation at the gold–vapor surface and nucleation in the bulk of the VLS catalyst at the interface of the LPCVD nitride substrate and the PECVD oxide encapsulation layer is minimal, as both are present in neighboring micro–crucibles, which have undergone the same experimental conditions.

The crystal surface parallel to the amorphous substrate imaged in Figure 3–12C is orientation close to the {1 1 1} plane, suggesting that crystals which have low energy orientations growing parallel to the substrate are less likely to twin when growing laterally from their heterogenous nucleation site. The crystal of Figure 3–13C is twinned, but the grain labeled i in the figure is significantly larger than the grain labeled ii. For growth termed potentially twinned, the presence of a larger, major grain and a smaller, minor grain was observed about half of the time. Assuming that the major grain was the first to nucleated, because for this particular case, it is the one in contact with the potential heteogenous nucleation site, it is suggestive that the minor grain did not form under the steady–state CVD conditions, but formed towards the end of the growth or possibly when the micro–crucible cooled from the processing temperature to room temperature. Thus some of the observed twinning which can be characterized as major grain/minor grain can be attributed to perturbations and free energy fluctuations at the end of growth, and did not occur during the steady–state VLS growth of two–dimensional silicon micro–films. This means that for some silicon thin–films categorized as potentially twinned, they would essentially grow as a single crystal for sufficiently long growth times. Twinned crystals such as the one imaged in Figure 3–14C were less common and are more difficult

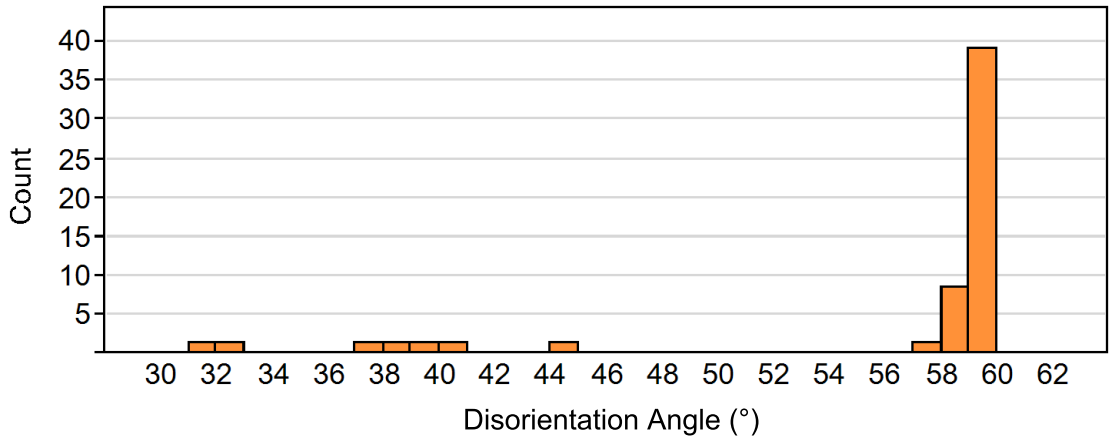

Figure 3–15: Distribution of disorientation angles between grain boundaries for all observed nucleation events. The 60° Σ3 coherent twin grain boundary was present in the overwhelming majority of observations.

to explain. One possible explanation is an instability during the growth of crystals, which have nucleated and grown along the higher energy gold–vapor interface. This extended amount of crystal surface at a higher energy interface could have provided the free energy needed for the crystal in Figure 3–14C to twin multiple times as it grew.

Figure 3–15 indicates that the overwhelming majority of grain boundaries observed in the faceted silicon phase were 60° Σ3 coherent twin boundaries. Boundaries of this type have been observed to have special electronic properties where electron mobility is expected to be degraded minimally [173] [157], and, theoretically, carrier lifetime should be preserved across them. EBSD experiments characterizing cast polysilicon microstructures [155] showed similar distributions of 60° Σ3 gain boundaries in the material, but the percentage of high energy, electrically parasitic boundaries was much higher and coherent grain boundaries only accounted for 20

percent of those observed. The most likely explanation for the difference between this 86 percent $\Sigma 3$ grain boundaries observed in this experiment and the 20 percent reported is that the cast polycrystalline silicon had multiple heterogeneous nucleation events and the grains grew together, impinging each other and creating high energy boundaries at triple points, whereas the silicon films grown in micro–crucibles most likely had one heterogeneous nucleation event from which the crystal grew, and the observed twin grain boundaries are a result of perturbations at the surface of the crystal while growing. The large amount of 60° $\Sigma 3$ boundaries again suggests that lateral VLS growth of two–dimensional silicon micro–films occurs close to thermodynamic equilibrium and defects present are restricted to low energy 60° $\Sigma 3$ twinned crystals.

3.2.6 Conclusion

Using a novel chromium undercut microfabrication technique, micro–crucibles with a nominally pure gold catalyst which promote the lateral growth of two–dimensional silicon mirco–films have been reliably fabricated. It was found that a proper ratio between initial gold volume and initial gold–vapor interface was required to grow silicon crystals of significant size. VLS growth of silicon films in micro–crucibles has a limiting upper temperature threshold of 475 °C, above which the uncontrolled growth of nanowires occurs within the crucibles and halts the VLS process.

Growth of faceted silicon phases within the micro–crucible geometry was found to be single crystalline in nature 30% of the time, twinned in nature 45% of the time and 25% polycrystalline for the experimental conditions used. Single, potentially

twinned and polycrystals all had an aversion to growth with the {1 0 0} surface parallel to the amorphous substrate. Probable reasons for the twinning of the faceted silicon phase have been conjectured to be due to impurities in the VLS catalyst, the free energy associated with the temperature gradients when quenching the faceted silicon phase from the processing temperature to room temperature, and energy fluctuations present when the faceted silicon phase grows along high energy boundaries such as the gold–vapor interface.

The grain boundaries observed in twinned and polycrystalline silicon growth were overwhelming found to be of the 60° Σ3 coherent twin type. This type of grain boundary has superior electrical properties and the degradation of electron mobility across the boundary is expected to be minimal. The large amount of 60° Σ3 boundaries suggests that lateral VLS growth of two–dimensional silicon micro–films occurs close to thermodynamic equilibrium and that it is very robust, as 60° Σ3 still form even when nucleation is suspected to be initiated by an impurity or surface defect.

3.2.7 Acknowledgments

The authors would like to thank McGill University and NSERC for funding this research, and the McGill Nanotools Microfab team for the generous use of their equipment and technical expertise.

3.3 Alloyed catalysts and their effect on lateral, vapor–liquid–solid grown thin–films

3.3.1 Abstract

Using amorphous oxide templates known as micro–crucibles which confine a vapor–liquid–soild catalyst to a specific geometry, two–dimensional silicon thin–films of a single orientation have been grown laterally over an amorphous substrate. The vapor–liquid–solid catalysts consisted of nominally of 99% gold and 1% titanium, chromium, or aluminum, and each alloy affected the processing of micro–crucibles and growth within them significantly. It was found that chromium additions inhibited the catalytic effect of the gold catalysts, titanium changed the morphology of the catalyst during processing and aluminum stabilized a potential third phase in the gold–silicon system upon cooling. Through experimenting with catalyst compositions, the fundamental mechanisms which produce concentration gradients across the gold–silicon alloy within a given micro–crucible have been proposed. Using the postulated mechanisms, micro–crucibles were designed which promote high–quality, single crystal growth of semiconductors.

3.3.2 Introduction

Vapor–liquid–solid (VLS) lateral growth of nanowires and two–dimensional thin–films over amorphous substrates is a potentially enabling technology for grown–on–chip optical interconnects [142] and integrated three–dimensional transistors [140], but for reliable production of theses technologies, fabrication methods need to be developed which are robust, which can control the spatial location of the lateral growth, and which produce high–quality semiconductor crystals. In this work a test structure known as a micro–crucible has been designed and fabricated [172] to control the

growth of two–dimensional thin–films over amorphous substrates. Micro–crucibles (Figure 3–16) are amorphous oxide templates which allow a buried gold catalyst to nucleate silicon crystals within their confined geometry and promote lateral growth of the nucleated crystals during chemical vapor deposition (CVD) processing. Similar structures have been used to laterally grow high–quality, two–dimensional, semiconducting thin–films [143] [144], but without the low temperature processing advantages which the VLS technique enables. One key obstacle to the development of lateral growth of semiconducting materials over amorphous substrates with the VLS technique is manipulating the VLS catalyst to adhere to the amorphous substrate, so that standard fabrication processes such as photolithography and wet etching can be preformed on substrates on which the catalysts have been deposited. Here, techniques for processing VLS catalysts on amorphous substrates will be detailed and the resulting lateral growth investigated.

Gold has traditionally been used as the VLS catalyst in the academic research environment. VLS growth has been successfully achieved using metal catalysts other than gold such as platinum [89] [13] [90], palladium [91] [13] [90], silver [91] [89] [13], aluminum [88] [92] [93], nickel [94] [89] [90], iron [14] [63], copper [91] [89], gallium [87] [95] [88], and indium [87] [96] [103], but the larger process window of gold and the experimental variability associated with these metals keeps gold the catalyst of choice. Indeed the challenge of working with catalysts which readily oxidize in ambient conditions has inhibited experimentation with many of the other potential catalysts. Work on alloying gold catalysts with other VLS capable catalyst has also

been preformed [76] [75], primarily to engineer interface abruptness in heterostructures [78] [175], or to mitigate the diffusion of the gold catalyst [176], but there are few investigations on how alloying gold affects VLS growth beyond the nanoscale. Because of the unique challenges encountered when trying to adhere gold to amorphous substrates when using VLS techniques to grow two–dimensional thin–films, gold is often undesirably alloyed with the adhesion layers used to keep it on the substrate. A greater understanding of the effects of alloying gold catalysts with their respective adhesion layers is desirable, as robust fabrication and large scale integration of lateral growth using the VLS technique will more than likely require the use of alloyed catalysts.

In the following described experiments, the traditional gold adhesion promoters titanium and chromium, as well as the nontraditional promoter, aluminum, will be alloyed with gold, and lateral growth using these alloyed catalysts will be described. The growth results using different adhesion promoters, as well as growth not using adhesion promoters [172], varied signifantly from each other. Through the experiments, an understanding of how silicon concentration gradients develop within the micro–crucible has been proposed, with which design and experimental considerations have been taken to controllably grow high–quality, laterally grown, two–dimensional thin–films of silicon.

3.3.3 Experimental

Silicon {100} substrates with a layer of 100 nanometers of low–pressure chemical vapor deposition (LPCVD) silicon nitride were cleaned in a 1:3 by volume

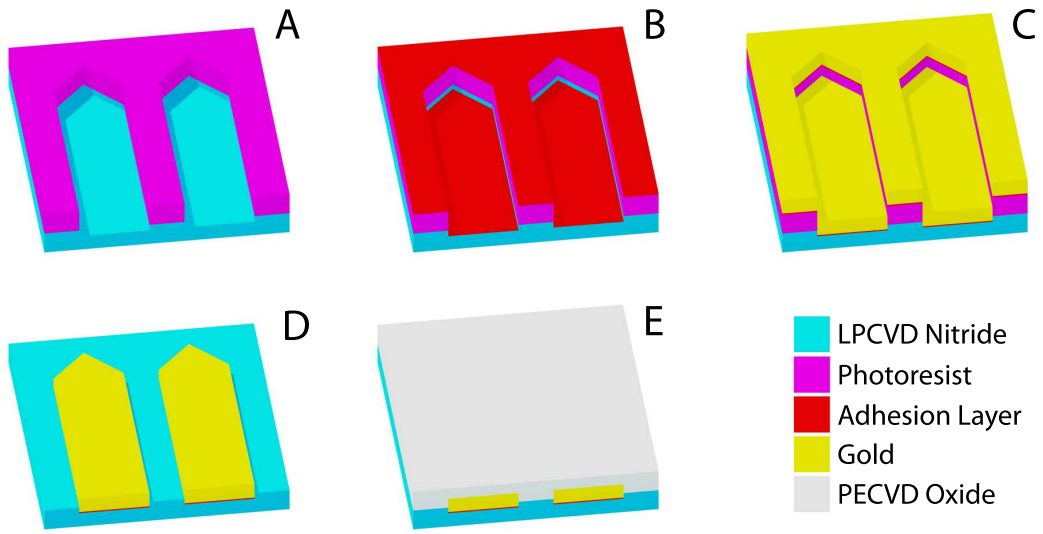

Figure 3–16: Steps used to fabricate for a micro–crucible with a buried adhesion layer. Figure 3–16A depicts a LPCVD silicon nitride substrate which has been patterned with photoresist and has been etched back 20 nm using a SF_6 reactive ion etch. Figure 3–16B depicts the deposition of a 1 nm thick adhesion layer over the patterned and etched structure. Figure 3–16C depicts the Au catalyst layer being deposited over the adhesion layer. Figure 3–16D depicts the structure after the metal deposited on the photoresist had been lifted off. Figure 3–16E depicts the gold patterns being encapsulated with PECVD silicon oxide, effectively defining the geometry of the micro–crucible.

35% H_2O_2 : 97% H_2SO_4 piranha solution for 10 minutes at 80 °C and rinsed in deionized (DI) water. AZ Electronic Materials AZ 5214-E image reversal photoresist was spun to the substrates with a thickness of 1.4 micron and was baked, exposed and developed as the per the recommendations of the manufacturer.

The LPCVD nitride film on the substrates was etched back 20 nanometers using a low power SF_6 reactive ion etch, utilizing the photoresist as an etch mask (Figure 3–16A). After etching, the substrates were placed in the electron beam evaporation chamber where adhesion layers of chromium, titanium or aluminum with thicknesses of 1 nanometer were deposited (Figure 3–16B). While remaining under vacuum, gold thicknesses of 50 or 150 nanometers were deposited over the adhesion layers (Figure 3–16C). All metal films were deposited in a vacuum of at least 5.5×10^{-6} Torr.

After deposition,s metal on the photoresist was lifted off in an agitated bath of Microposit Remover 1165 for 10 minutes at 60 °C. The substrates were further cleaned in a self–heated 1:3 piranha solution for 10 minutes to remove additional photoresist which has been hardened during the electron beam evaporation process (Figure 3–16D). After cleaning, 500 nanometers of plasma–enhanced chemical vapor deposition (PECVD) silicon oxide was deposited on to the substrates to encapsulate the gold structures (Figure 3–16E).

A second layer of AZ5214-E photoresist was spun on top of the encapsulated substrate and processed as before. This photoresist defined the areas of the substrate where the encapsulation over the gold structures was selectively removed using a low

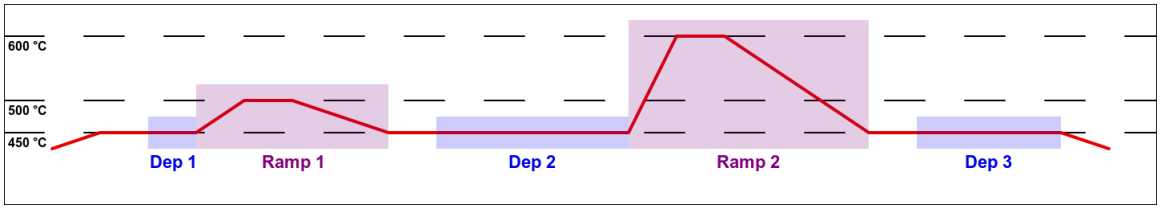

Figure 3–17: The thermal heat treatment profile used to control and condition the alloyed gold catalyst during the growth step.

power SF_6 reactive ion etch. The opened structures were then etched in concentrated Transene Gold Etchant TFA heated to 50 °C until the desired amount of gold remained micro-crucible amorphous growth templates.

The micro–crucible test structures were left overnight prior to CVD growth in concentrated H_2SO_4, if the adhesion layer was titanium or aluminum, or left in Transene Chromium Etchant 1020 overnight, if the adhesion layer was chromium, to remove any residual adhesion promoting materials. Just before being placed in the CVD chamber, the substrates were dipped in a 1:3 by volume 70% HNO_3 : 35% HCl aqua regia solution for 30 seconds and cleaned in an 80 °C 1:3 piranha solution for 10 minutes, so as to clean the micro–crucibles on last time before growth. The wafers were processed in a hot–walled, LPCVD quartz tube for 60, 120 and 180 minutes, at temperatures of 425 °C, 450 °C and 475 °C, at a of pressure of 420 mTorr and gas flow rates of 150 sccm of SiH_4 and 900 sccm of N_2 (20 mTorr pp_{SiH_4}). Some of the wafers were thermal processed, as depicted in Figure 3–17, during grow to enhance growth stability. These heat treatments involved a short 15 minute SiH_4 deposition (Dep 1 in Figure 3–17), followed by a ramp to 500 °C held for 30 minutes (Ramp 1), a second deposition for 60 minutes (Dep 2), followed by a second ramp to 600 °C

held for 30 minutes (Ramp 2), and an arbitrary long third deposition step (Dep 3) to finalize the growth. After deposition the quartz boat holding the wafers was directly removed from the furnaces at process temperature and allowed to cool in air.

The remaining encapsulation layer was removed by a combination of reactive dry etching with CHF_3 chemistry and wet etching with 1:6 buffered oxide etch (BOE), which allowed for high resolution scanning electron microscope (SEM) and electron backscatter diffraction (EBSD) imaging of the growth which occurred in the micro–crucible templates.

3.3.4 Results

The 20 nanometer LPCVD nitride etch back step prior to metal deposition appeared to successfully isolate the adhesion layer from the atmosphere and prevent oxidation during microfabrication due to the ability to clean the substrates in piranha solution for longer than 20 minutes prior to the PECVD silicon oxide encapsulation of the fabricated gold structures without the structures lifting off. This means that liquids could not diffuse underneath the patterned gold and selectively etch the aluminum, titanium, or chromium.

It was found for micro–crucibles using aluminum or titanium as an adhesion layer that Transene Gold Etchant TFA was not as effective at partially etching gold out of the opened structures when compared to micro–crucibles fabricated without adhesion layers [172]. The partial etching step defines the location of the initial gold–vapor interface, at which silane will react and diffuse into the solid catalyst. Ideally the interface is smooth, continuous, and planar, and it is undesirable to have a gold–vapor interface which is discontinuous and dispersed into differentiated gold

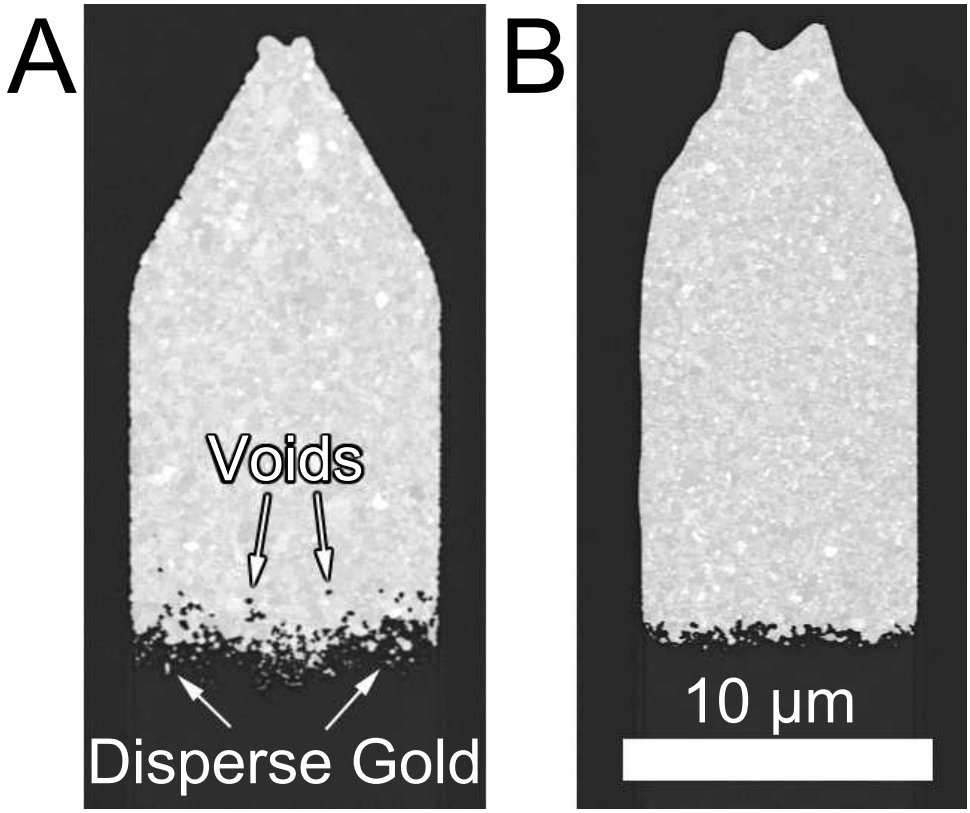

Figure 3–18: Initial conditions prior to the CVD growth of the VLS catalysts with 150 nm of Au after being partially etched using Transene Gold Etchant TFA heated to 50 °C. Figure 3–18A used a 1 nm thick adhesion layer of Al and Figure 3–18B used a 1 nm thick adhesion layer of Ti. Both Figures 3–18A and 3–18B show a discontinuous gold–vapor interface with dispersed, differentiated gold particles remaining in front of the bulk of the VLS catalyst after the partial etching step. Al adhesion layers also had observable voids in the bulk of the VLS catalyst.

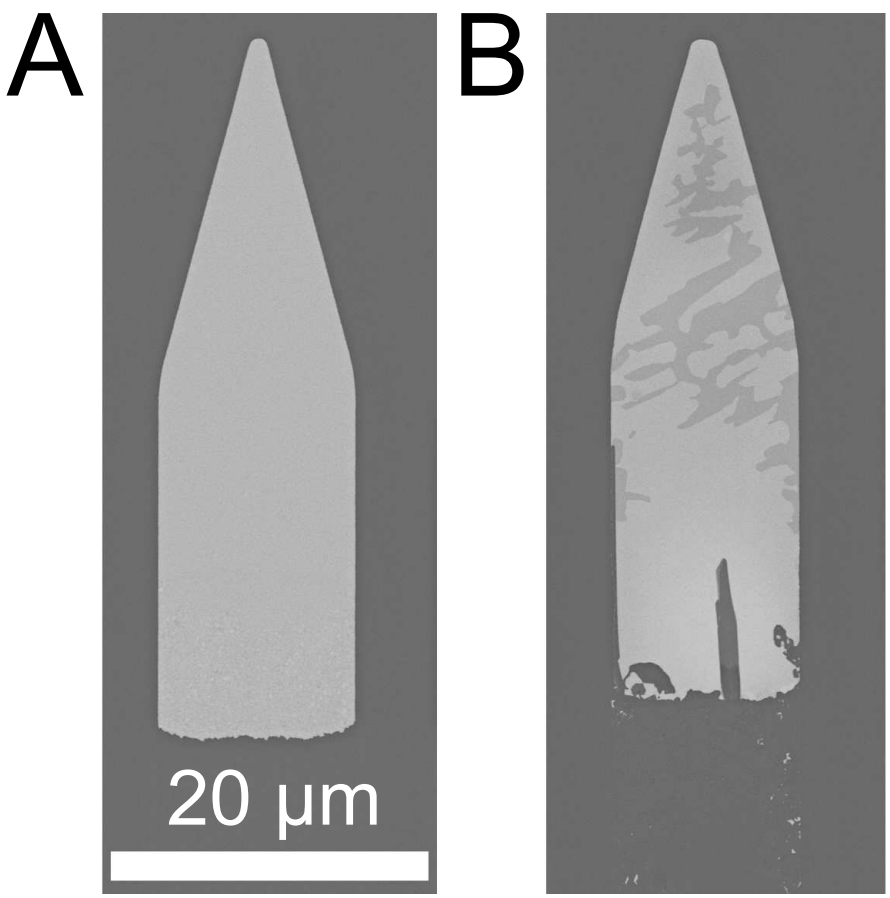

Figure 3–19: Electron backscatter micrographs of two different micro–crucibles using 1 nm of Cr and 50 nm of Au. Figure 3–19A is of a micro–crucible before the growth step and shows a VLS catalyst which has a continuous, planar gold–vapor interface after the gold had been partially etched. Figure 3–19B shows micro–crucible which did not nucleated faceted silicon phase after growth at 475 °C for 3 hours.

particles. Figure 3–18 depicts the initial gold–vapor interfaces of micro–crucibles with 150 nanometers of gold using aluminum (Figure 3–18A) and titanium (Figure 3–18B) adhesion layers after being partially etched in 50 °C heated gold etchant. Partially etched gold catalysts which used aluminum as an adhesion layer consistently had a finer and more dispersed, discontinuous gold–vapor interface than catalysts with titanium adhesion layers. No technique experimented with was capable of producing smooth, continuous gold–vapor interfaces for partially etched gold catalysts which used either of the adhesion layers. Catalysts using aluminum adhesion layers had voids present in their bulk, away from the gold–silicon interface (Figure 3–18A), which were not obsevered in catalysts with titanium adhesion layers. The heated Transene Gold Etchant TFA treatment was found to be the most effective at minimizing the size of the disperse, discontinuous gold–vapor interface. Micro–crucibles using chromium adhesion layers etched very well (Figure 3–19A), and had a gold–vapor interface which was continuous and lacked differentiated gold particles. However, after a 180 minutes CVD growth at 475 °C (Figure 3–19B) there was little silicon deposition or growth of a faceted silicon phase in micro–crucibles which used chromium as an adhesion layer, unlike that of micro–crucibles with aluminum and titanium adhesion layers.

Silicon crystals in crucibles with titanium or aluminum adhesion layers nucleated similarly to crystals nucleated in micro–crucibles without adhesion layers [172]. Figure 3–20 images a micro–crucible with a 150 nanometers gold film utilizing titanium as an adhesion layer and had undergone thermal processing during growth as depicted in Figure 3–17. Frequently, nanowires were found in front of the bulk of

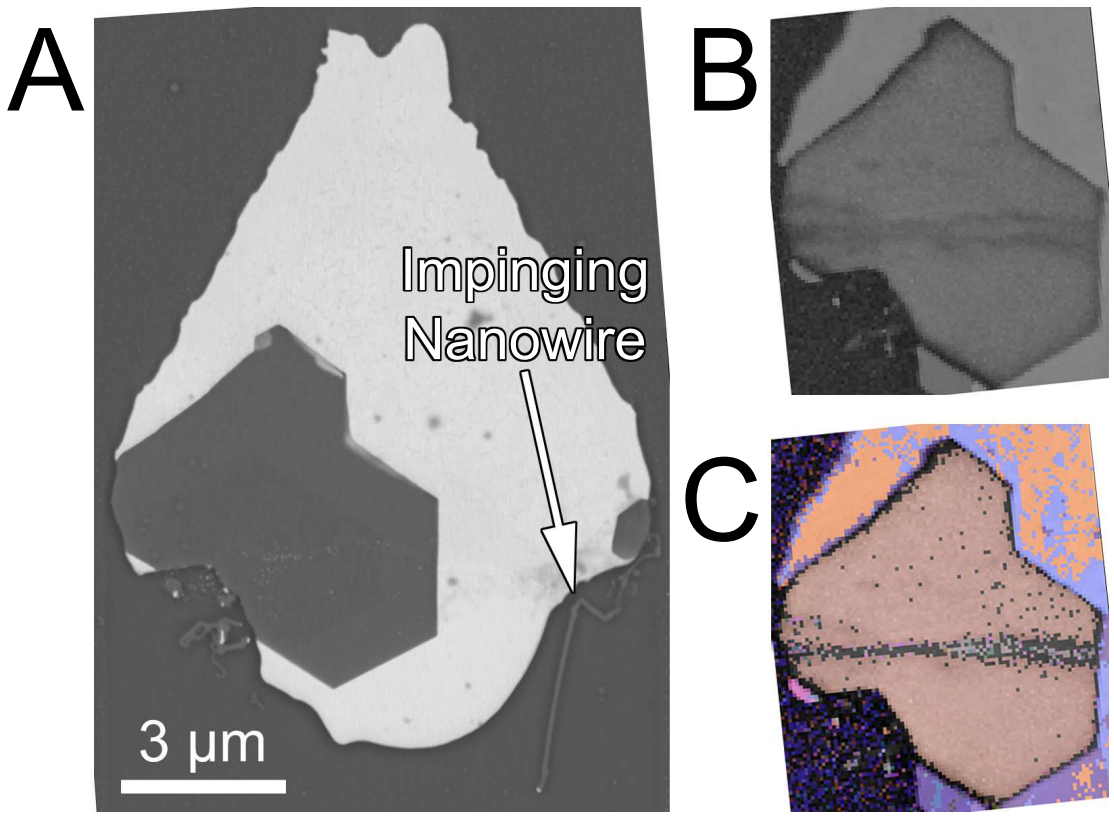

Figure 3–20: Growth from a 150 nm Au crucible with 1 nm of Ti as an adhesion layer using the thermal profile depicted in Figure 3–17. Figure 3–20A depicts a crucible which has had impinging nanowires nucleate in front of the bulk catalyst. Figure 3–20B is an EBSD contrast map of the faceted silicon phase and Figure 3–20C is a contrast map overlayed with a Euler angle map so that different crystallographic orientations of the faceted silicon phase can be observed.

gold catalyst as imaged in Figure 3–20A. Infrequently, micro–crucibles using a titanium as an adhesion layer had a gold–silicon liquid catalyst which solidified without any visible lamellar structures, also shown in Figure 3–20A. The band contrast map (Figure 3–20B), and the band contrast map overlayed with an electron backscatter diffraction (EBSD) Euler angle map (3–20C) aid with determining the crystalline quality of the nucleated faceted silicon phase. Band contrast maps are a measurement of the sharpness/indexing confidence of the Kikuchi patterns of backscatter electrons of a scanned area. White represents a well defined crystalline area and black represents an amorphous region, or an area of multiple or undefined Kikuchi patterns. Euler angle maps are colored to highlight grains of different orientations with respect to an arbitrary reference orientation. The faceted crystal in Figure 3–20 is of a single orientation, but with an area running through the center of it which was not indexable by the EBSD software.

The thermal treatment depicted in Figure 3–17 was successful at reducing the amount of nanowires which nucleated in front of the bulk VLS catalyst. Figure 3–21 shows two micro–crucibles with a 150 nanometers gold film utilizing titanium adhesion layers. Figure 3–21A was processed with 120 minutes of silane deposition at 450 °C without using a multi–deposition thermal profile, whereas Figure 3–21B was processed with 120 minutes of silane deposition at 450 °C using the thermal profile of Figure 3–17. The silicon nucleated near the gold–vapor interface in Figure 3–21A is a mixture of a faceted silicon and silicon nanowires which have grown into each other. The bell shape of the gold–vapor interface in Figure 3–21B was found in nearly all of micro–crucibles with titanium adhesion layer lacking nanowire

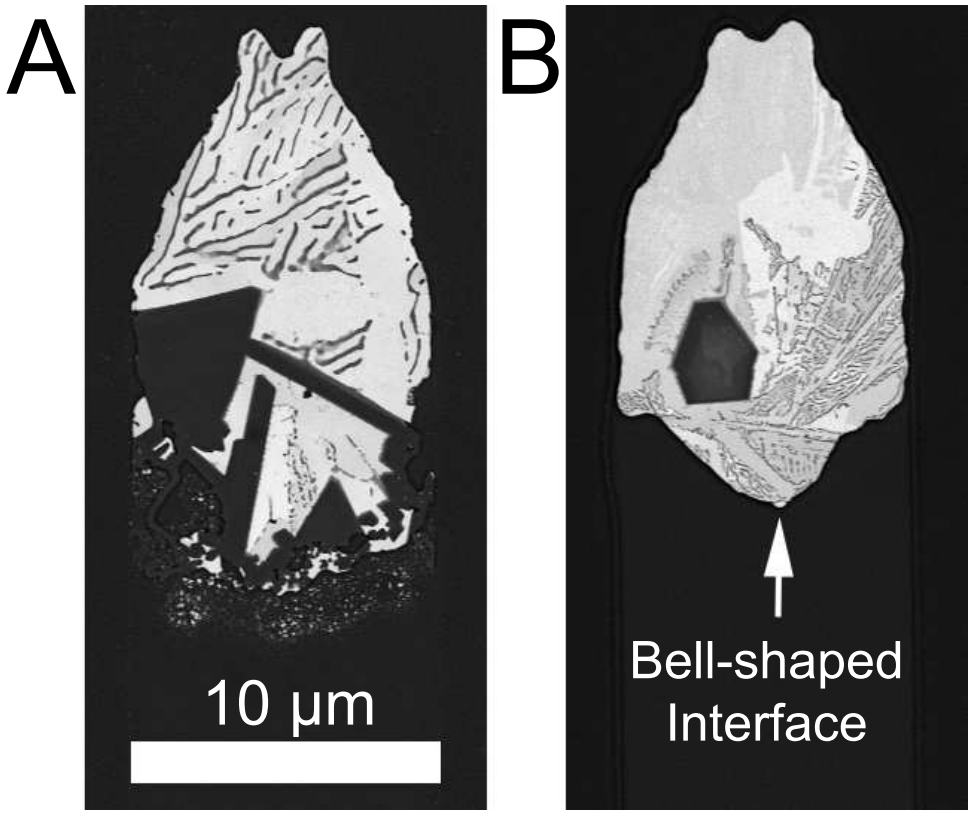

Figure 3–21: Faceted silicon phase nucleation and growth in two micro–crucibles with a 150 nm film of Au using 1 nm of Ti as an adhesion layer. Figure 3–21A was not grown with a multi–step deposition process while Figure 3–21B was processed with the thermal treatment depicted in Figure 3–17. The bell–shaped gold–vapor interface was regularly observed in micro–crucibles with Ti adhesion.

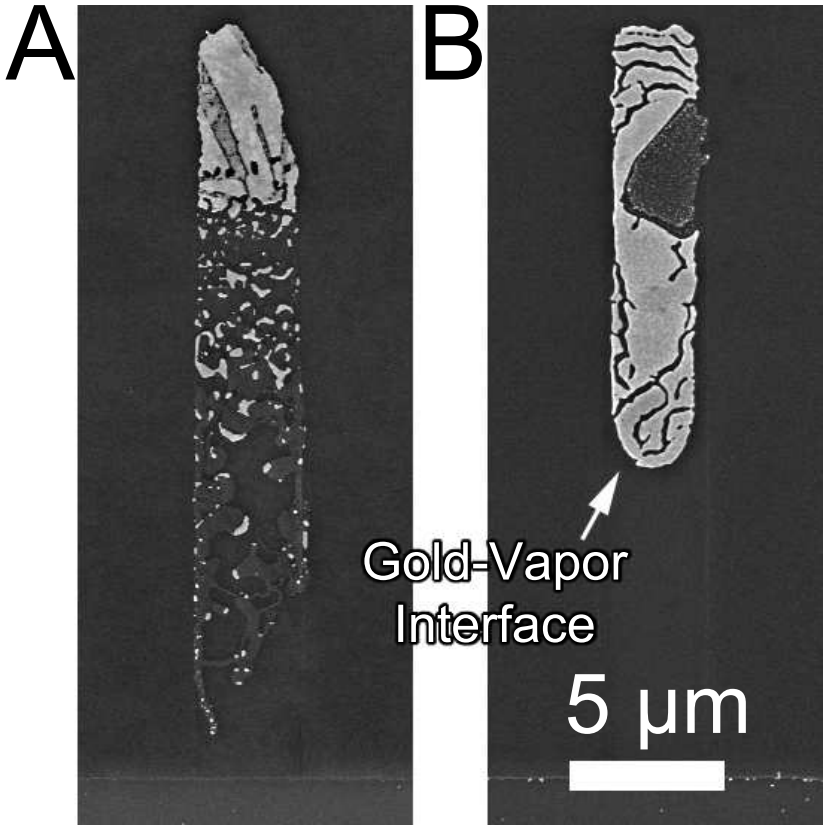

Figure 3–22: Growth in 50 nm Au micro–crucibles using 1 nm of Al as an adhesion layer at 475 °C for 60 minutes in Figure 3–22A and at 425 °C for 180 minutes in Figure 3–22B.

growth. Nanowire growth in micro–crucibles was significantly reduced by lowering the processing temperature from 475 °C to 425 °C . Figure 3–22 shows two micro–crucibles with a 50 nanometer gold film using 1 nanometer of aluminum as the adhesion layer. The crucible in Figure 3–22A had a CVD step of 60 minutes at 475 °C, while the crucible in Figure 3–22B had a CVD step of 180 minutes at 425 °C. Low temperature growth in micro–crucibles with aluminum adhesion layers produced hemispherical gold–vapor interfaces, as imaged in Figure 3–22B.

Some micro–crucibles were designed to neck out crystalline defects and multiple orientations. Figure 3–23A is a backscatter electron micrograph of a necked micro–crucible with a 150 nanometer gold film utilizing aluminum as the adhesion layer. The growth conditions for this sample were 120 minutes at 475 °C. Figure 3–23B shows an image at higher magnification of the crystal which had grown into the crucible neck. Figure 3–23C is an EBSD band contrast map reveling that there was a twinned grain running down the center of the faceted silicon phase which had been necked out. Figure 3–23D is a map of the Euler angles of the mapped crystal superimposed over the band contrast map and shows that the two crystallographic orientations on either side of the necked–out twinned grain are the same orientation.

A possible third, intermediate phase between pure gold and pure silicon, or an ultra fine gold–silicon lamellar structure, was observed in micro–crucibles with aluminum as the adhesion layer. Figure 3–24A is a backscatter electron micrograph of a necked micro–crucible with a 150 nanometer gold film utilizing aluminum as the adhesion layer which was grown for 120 minutes at 475 °C. Figure 3–24 magnifies the three phase region near the neck of the crucible where energy-dispersive x–ray spectroscopy (EDS) was preformed. Figure 3–24 shows that Area 1 has both peaks associated with the silicon (1.74 kV) in Area 2 and the gold (2.13 kV) in Area 3. In addition to the fact that there are both silicon and gold peaks in Area 1, where both gold and silicon are immiscible with each other at room temperature, further evidence to support the presence of a third phase is that the material readily etched in BOE, whereas neither gold nor silicon do.

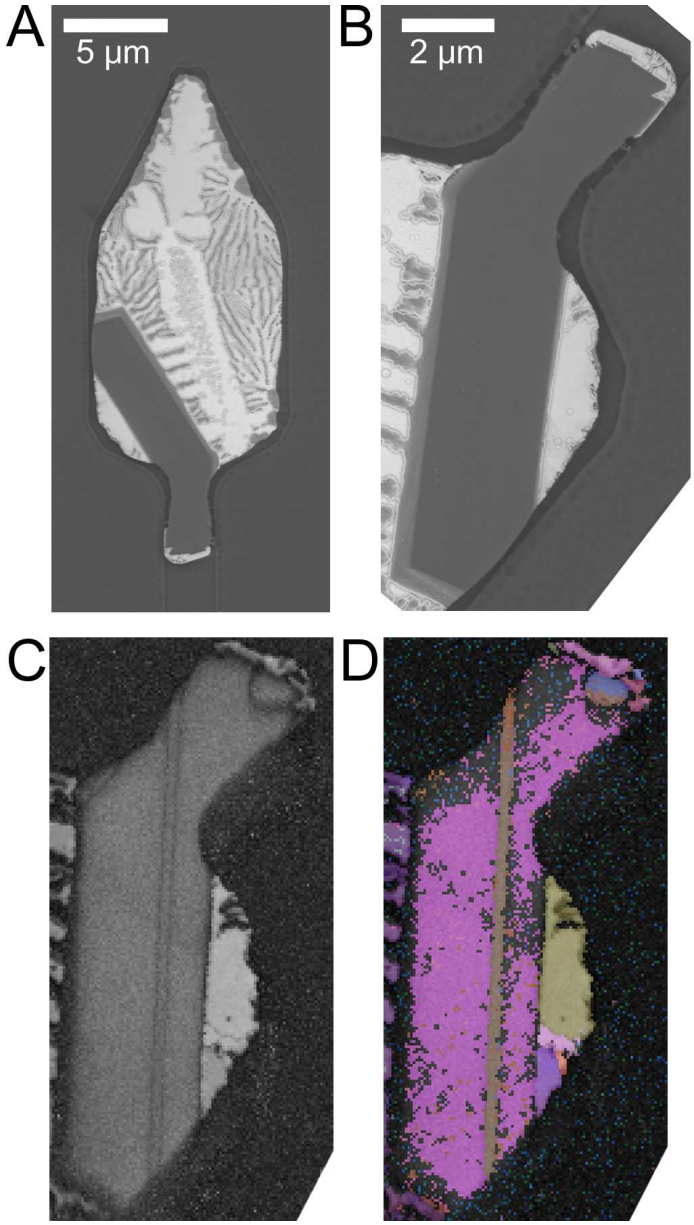

Figure 3–23: A micro–crucible with a 150 nm Au film using 1 nm of Al as an adhesion layer which has had a neck design implemneted. Figure 3–23A depicts a faceted silicon crystal which had grown into the neck after 120 minutes of growth at 475 °C. Figure 3–23B is a higher magnification image of the necked growth. Figure 3–23C is an EBSD contrast map of the faceted silicon phase showing that a twinned grain was necked out and Figure 3–23D is a contrast map overlayed with a Euler angle map showing the crystallographic orientations on either sided of the necked out grain are the same orientation.

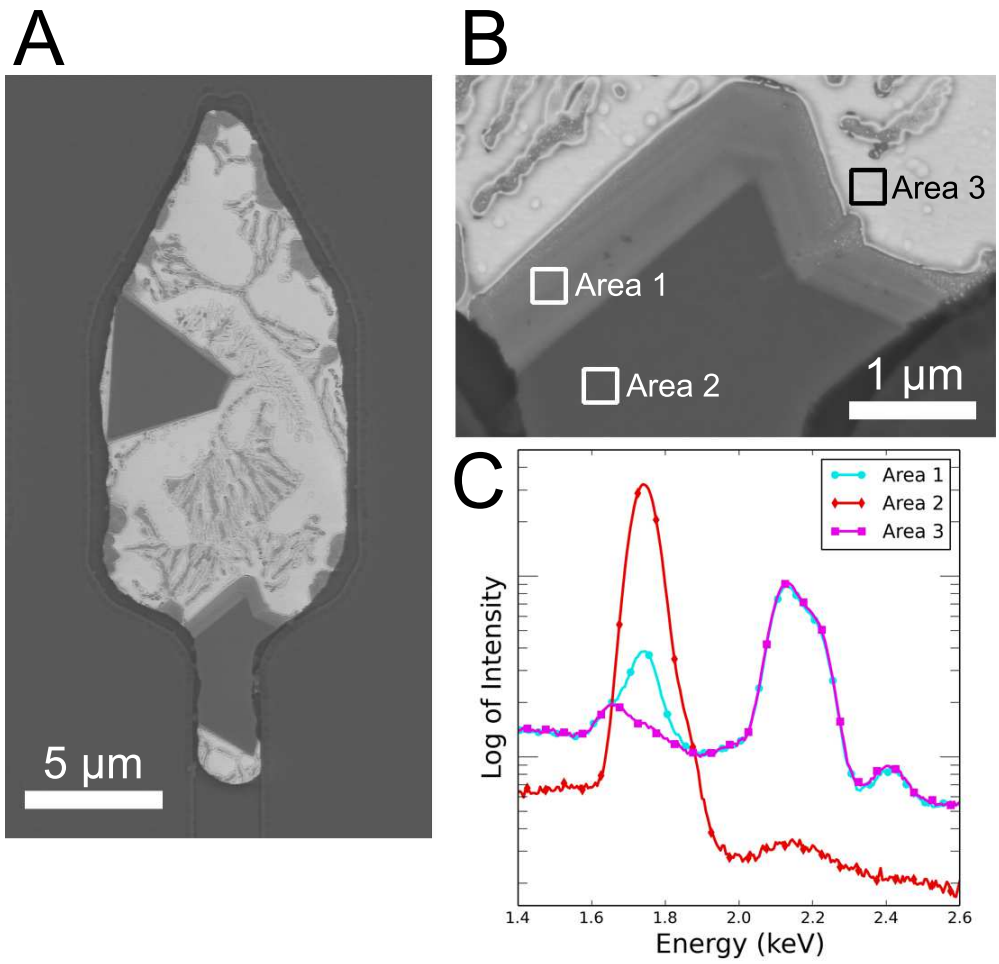

Figure 3–24: Backscatter micrographs and EDS scans of a 150 nm Au film in a crucible using 1 nm of Al as an adhesion layer which had nucleated a faceted silicon phase. Figure 3–24A depicts a faceted silicon crystal growth which occurred after 120 minutes at 475 °C. A potential third gray phase (labeled Area 1 in Figure 3–24B) was regularly observed in micro–crucibles which used Al as an adhesion layer. An EDS (Figure 3–24C) scan of the faceted silicon phase (Area 2), the gold–silicon alloy which had solidified (Area 3) and the gray area revealed that the gray area contains EDS peaks for both Si (1.74 kV) and Au (2.13 kV).

3.3.5 Discussion

The overnight H_2SO_4 and Transene Chromium Etchant 1020 treatments were attempts to leach any of the adhesion layer near the initial gold–vapor interface of the micro–crucible into solution and it is not believed that any aluminum or titanium oxide products were regularly present in the crucibles during growth through the regular observation of faceted silicon instead of polycrystalline or irregular growth. Crucibles utilizing chromium as an adhesion layer (Figure 3–19) did not catalyze silane as well as crucibles utilizing aluminum or titanium, and any silicon rich phase that nucleated in chromium micro–crucibles was not faceted. Using the thermodynamic modeling package FactSage [177], it was predicted that solid chromium silicide would be stable in gold–silicon–chromium alloys at the temperatures used in this experiment and it is believed that the lack of silicon growth in micro-crucibles utilizing chromium as an adhesion layer can be attributed to a thin barrier of chromium silicide, which formed at the gold–vapor interface when silane was introduced to the system. There, chromium silicide would effectively prohibit silane from cracking at the catalyst surface and result in limited silicon deposition. Chromium oxides could also cause such a phenomenon if formed at the gold–vapor interface, but the overnight chromium etch should have etched away any reactive chromium species from the interface.

During growth, the disperse, discontinuous gold catalyst at the gold–vapor interface, as imaged in Figure 3–18, resulted in nanowire growth in front of the bulk of the gold catalyst (Figure 3–21A) for micro–crucibles with titanium and aluminum adhesion layers. The inability to partially etch gold out of a micro–crucible cleanly

is believed to be a result of the alloying of the adhesion layer with the gold catalyst. Transene Gold Etchant TFA is designed to selectively etch gold, but the alloyed catalysts used in this experiment were nominally 99% gold, 1% adhesion layer, and for each adhesion layer used, unpredicted responses were observed during the processing of the micro–crucibles and growth within them, such as the inability to grow a faceted silicon phase in micro–crucibles with a chromium adhesion layer (Figure 3–19B).

Unique to samples with titanium adhesion layers was the solidification of the gold–silicon alloy without any lamellar structures, as imaged in Figure 3–20A, and the bell–shaped gold–vapor interface, imaged in Figure 3–21B. Micro–crucibles using titanium adhesion layers which solidified without lamellar structures were not common and were not reproducible run to run. Because of the lack of lamellar gold–silicon phase, it is suggestive that these crucibles with titanium adhesion layers underwent significant undercooling before fully solidifying [172]. The inability to reproduce the results suggests that there is currently some uncontrolled factor while processing titanium adhesion layer wafers from the partial gold etch step to the post–CVD cool down step which is unique to titanium chemistry, as wafers with aluminum adhesion layers which underwent the same processing steps reproduced the same results every time. The area running through the middle of the faceted silicon phase in Figure 3–20C, which was not indexed well by EBSD mapping, is typical of grains which are mechanically stressed and is suggestive of a more extreme solidification process than is typically seen in other micro–crucible growth.

Bell–shaped gold–vapor interfaces, such as the one imaged in Figure 3–21B, were consistently observed in crucibles using titanium adhesion layers. These geometric features can be attributed to the "sticky" nature of titanium. By studying the gold–titanium phase diagram [178], it can be observed that 1% titanium in gold is not soluble at any of the temperatures used in this experiment. Through the repeated observations of the bell–shaped gold–interface, it is believed that titanium adhesion layer residues provided an extra adhesive force not observed in crucibles without adhesion layers, which kept the liquid gold–silicon alloy in its initial location within the crucible and prevented the liquid gold–silicon alloy from dewetting the amorphous micro–crucible walls during the early growth stage of the faceted silicon phase.

Unlike titanium, micro–crucibles with aluminum adhesion layers allowed the gold–silicon liquid catalyst to dewet the micro–crucibles walls much like the liquid gold catalysts without adhesion additions [172]. The aluminum–gold phase diagram [179] shows that aluminum adhesion layers used for these experiment should be completely soluble in gold at room tempurature, suggesting that the adhesive properties of aluminum are temporary, and thus once the aluminum is solutionized in the gold, the catalyst no longer readily adheres to the amorphous surfaces and dewets during growth. Aluminum solubility in gold could also be a source for the observed voids (Figure 3–18A) in the solid gold catalyst with aluminum adhesion layers, which were consistently observed prior to growth. Due to solid state diffusion of aluminum into gold, the voids could be the result of a volume reduction in the alloyed gold–aluminum with respect to the pure gold and aluminum metal stack initially deposited. The voids could also be attributed to the selective etching of

the gold enchant, but the voids sometimes appear microns away from the gold–vapor interface and it is hard to understand how a liquid etchant could penetrate so deeply.

While the unique characteristics of each adhesion layer affect the reliable growth of silicon crystals within micro–crucibles, the most detrimental and unexpected result for the reliable growth of faceted silicon in crucibles with titanium or aluminum adhesion layers was the discontinuous, disperse and differentiated gold particulates at their gold–vapor interface, which agglomerated during growth into discrete gold nanoparticles and caused nanowire growth in micro–crucibles. Because the surface–to–volume ratios of the particulates are much higher than the bulk VLS catalyst, the disperse, noncontinuous, individual gold–silicon microsystems supersaturate and nucleate faceted silicon phases in the form of nanowires much faster than the bulk catalyst. These nanowires grow in all directions, impinge the bulk catalyst and eventually obstruct the gas diffusion into the crucible (Figure 3–21A). Nanowires which impinged the bulk gold catalyst can provide a crystalline silicon seed for heterogenous nucleation of faceted silicon crystals in the micro–crucible, such as the one labelled in Figure 3–20A.

Attempts to mitigate nanowire growth from a disperse catalyst had mixed results. An attempt to etch the gold catalyst in dilute 20:1 by volume DI water to Transene TFA Gold Etchant planarized the gold–vapor interface well, but it was still discontinuous and the disperse gold particulates were still present in front of the bulk catalyst. Changing the gold etch chemistry to 1:3 by volume 70% HNO_3 : 35% HCl aqua regia improved results in micro–crucibles using titanium adhesion layers, but only by reducing the number of disperse gold particles, not eliminating them. The

best etching practice for minimizing the amount of disperse gold catalyst was found to be a hot Transene Gold Etchant TFA primary etch followed by a short aqua regia etch just before placing the samples into the LPCVD furnace.

The best technique for controlling nanowire nucleation from the disperse catalyst was found to be the use of heating and deposition treatments, like the one depicted in Figure 3–17, which resulted in micro–crucibles like the one imaged in Figure 3–21B. The thermal treatments worked in theory by taking advantage of increase solubility of silicon in gold at higher temperatures and the thermal expansion of the gold–silicon alloy upon heating. The initial silane deposition step (Dep 1 in Figure 3–17) was short and was intended to liquefy the disperse gold particles by alloying them with silicon, as well as introduce silicon in the bulk gold catalyst. Ideally, during the first temperature ramp step (Ramp 1 in Figure 3–17) the bulk catalyst liquefied into a gold–silicon alloy and absorbed the already liquefied disperse gold particles into the bulk of the catalyst, thus eliminating the potential growth sites for nanowires within the micro–crucibles. Because of the considerable amount of time it takes to raise and lower the temperature of a hot–walled reactor, the initial ramp was only to 500 °C.

The second ramp step (Ramp 2) was an attempt to solutionize all the silicon deposited into the micro–crucible from the first and second (Dep 2) silane deposition steps, in hopes that any unwanted silicon nanowire growth missed during the first ramp would be dissolved in the gold–silicon alloy. A silicon dose was estimated from previous work [172] for one hour and fifteen minutes worth of growth, and it was calculated that at 600 °C, 150% of the predicted silicon dose would be soluble for

the initial volumes of gold used for this experiment. The solutionizing of the silicon also had the benefit of homogenizing the silicon concentration within the gold–silicon alloy, and allowed the faceted silicon phase to nucleate in areas away from the gold–vapor interface of the micro–crucibles, such as in the near center of the catalyst as imaged in Figure 3–21B, upon cooling from the ramp temperature or during the deposition step following the ramp. This homogenization is important as silicon concentration gradients across the liquid catalyst within the micro–crucible dictate how stable the silicon growth will be and where the faceted silicon nucleates.

Figure 3–22 shows the progression and morphology of silicon growth in micro–crucibles using a 50 nanometer gold film and 1 nanometer of aluminum as an adhesion layer when processed at different temperatures. The micro–crucible in Figure 3–22A was grown at 475 °C for 60 minutes and depicts a micro–crucible where nanowires have nucleated from the gold–vapor interface and completely blocked silane from diffusing to the bulk of the catalyst. Unlike the nanowires which nucleated from the disperse, discontinuous gold particulates at the gold–vapor interface in Figures 3–20A and 3–21A, the nanowires in 3–22A are a result of an unstable gold–vapor interface due to a flux of silicon atoms associated with silane cracking at the interface which was greater than the flux of silcon atoms diffusing from the interface into the bulk of the catalyst. The micro–crucible in Figure 3–22B was processed at 425 °C for 180 minutes. Here the cracking flux at the gold–vapor interface was less than the diffusional flux of silicon into the crucible, creating a stable interface during growth. This allowed for a faceted silicon phase to nucleate far away from the gold–vapor interface and let the gold–silicon alloy to form a hemispherical gold–vapor interface.

Controlling the concentration gradient of silicon across the gold–silicon alloy during silane deposition is the one of the fundamental steps which determines the quality and the nucleation location of the faceted silicon phase within micro–crucibles which have been properly fabricated. Assuming that the flux of silicon from the cracking of silane at the gold–vapor interface is sufficiently less than the flux of silicon diffusing into the bulk of the gold–silicon alloy from the interface, and that the catalytic effects of gold–silicon are not reduced as the concentration of silicon increases, the concentration gradient of silicon across the gold–silicon alloy is a function of time, temperature, surface–area–to–volume ratio of the catalyst in the micro–crucible and partial pressure of silane. The believed evolution of the silicon concentration gradient over time (t) and the subsequent nucleation of a faceted silicon phase within micro–crucibles is depicted in Figure 3–25 and is described as follows:

1. Upon introduction of silane, but prior to cracking at the catalyst (Figure 3–25 at $t = t_0$), the concentration of silicon in the vapor phase (C_V) is constant and the silicon concentration in the solid gold catalyst is zero. The silane must diffuse across a boundary layer (BL) before it can crack at the catalyst surface [15] [137].
2. A liquid gold–silicon phase forms upon the initial cracking of the silane at the gold–vapor interface (Figure 3–25 at $t = t_1$). The newly formed liquid–solid interface propagates towards the opposite end of the micro–crucible as more silicon is dissolved into the catalyst, until the entire catalyst has become a liquid gold–silicon alloy (Figure 10 at $t = t_2$).

3. Upon melting, a concentration gradient (ΔC) forms between the gold–vapor interface and the advancing liquid–solid interface in the micro–crucible. This concentration gradient extends to the opposite end of the micro–crucible once the solid catalyst has been completely transformed into a gold–silicon alloy.
4. Once the silicon concentration at the gold–vapor interface reaches the silicon liquidus equilibrium concentration (C_E) it becomes thermodynamically favorable for a faceted silicon phase to nucleate at the gold–vapor interface (Figure 3–25 at $t = t_2$), but the concentration still needs to reach one of the critical supersaturation (C_{crt}) points associated with different heterogeneous nucleation events to nucleate a faceted silicon phase, because of the extra free energy required to overcome the surface energy of a new phase [17].
5. Faceted silicon nucleation occurs when one of the critical supersaturation (C_{crt}) concentrations for one of the heterogeneous nucleation events is localized somewhere within the supersaturated gold–silicon alloy of the micro–crucible. The localized region is represented as the gray box in Figure 3–25 at $t = t_3$. After nucleation the concentration of the gold–silicon alloy nominally returns to the silicon liquidus equilibrium concentration (C_E).
6. Growth of a faceted silicon phase continues as long as silane is introduced into the system, where the silane cracks at the gold–vapor surface and the silicon atoms diffuses some length from the gold–vapor interface to the faceted silicon crystal.
7. Growth of the faceted silicon phase stops when the flow of silane is halted, but as the gold–silicon system is cooled from the processing temperature to room

temperature, silicon is rejected from the gold–silicon alloy and the faceted silicon phase acts as a sink for the rejected silicon, growing larger until room temperature equilibrium is reached [172].

Similar diffusion observations have been described for nanowires [114]. It has been observed in micro–crucibles with initial surface–to–volume ratios of 0.030 grown at similar experimental conditions, that silicon diffuses through the grain boundaries of the solid catalyst from the gold–vapor interface towards the rear of the micro–crucible. For the micro–crucibles used in this experiment, with averaged initial surface–to–volume ratios of 0.075, catalyst were entirely liquefied within 15 minutes of deposition at 425 °C. It is not believed that for micro–crucibles which have widths smaller than ten microns that the catalyst solid–to–liquid transformation plays a significant role in nucleation of the faceted silicon phase, but for sufficiently small surface–to–volume ratios and large cracking flux rates, the soild to liquid transformation will have not propagated to the rear of the micro–crucible before the faceted silicon phase nucleates.

As the gold–vapor surface reaches the silicon liquidus equilibrium concentration it becomes energetically favorable to nucleate the faceted silicon phase (silicon liquidus equilibrium concentrations for 425 °C, 450 °C and 475 °C are approximately 20.8, 21.5 and 22.3 atomic weight percent respectfully [22]). Once the silicon liquidus equilibrium concentration is reached at the interface, the region of the gold–silicon catalyst where the silicon concentration is at least equal to the silicon liquidus equilibrium concentration propagates towards the rear of the micro–crucible, much like the solid–liquid interface did before it. Depending on the flux of the cracking silane

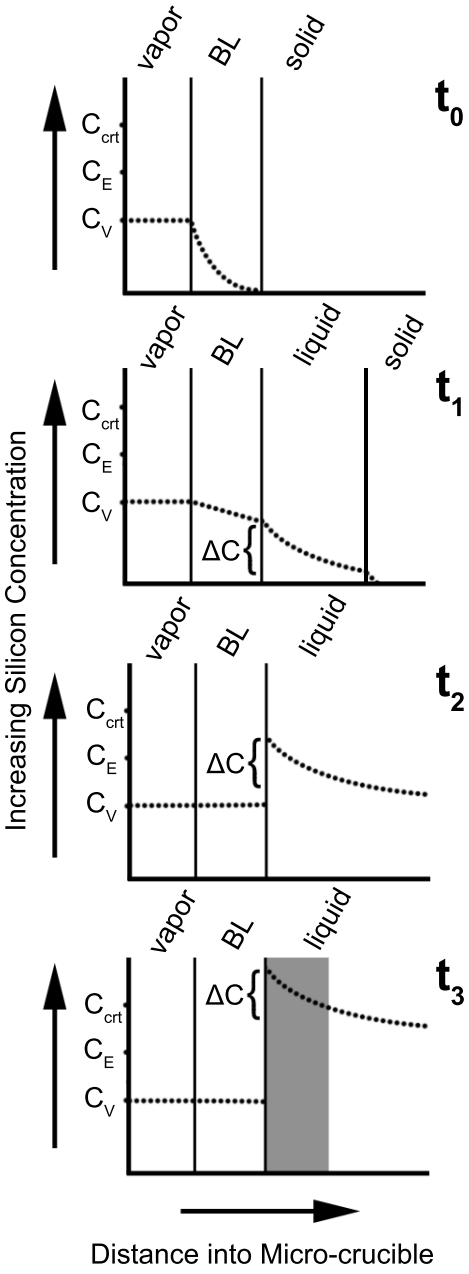

Figure 3–25: Diagrams of the evolution of the silicon concentration versus distance into the micro–crucible from the gold–vapor interface. At t_0 the vapor phase has a constant concentration (C_V) and silane has yet to react with the catalyst. At t_1 the silane has diffused across the boundary layer (BL) and cracked at the surface of the catalyst. A solid–liquid interface has formed where the concentration of the silicon in the gold catalyst is greater than zero, and a silicon concentration gradient (ΔC) can be measured between the gold–vapor interface and the farthest distance the silicon has diffused into the liquid phase. At t_2 the entire gold catalyst has transformed into a gold–silicon alloy and the silicon concentration at the gold–vapor interface is greater than the silicon liquidus equilibrium concentration (C_E), thus making it thermodynamically favorable to nucleate a faceted silicon phase there. At t_3 the area in the gray box has a concentration above one of the critical supersatruation concentrations (C_{crt}) required for a heterogeneous nucleation event. It is in the region defined by this gray box that a faceted silicon phase will first nucleate and grow.

and the diffusion of silicon into the liquid, the concentration at the gold–vapor interface can increase much faster than the the concentration in the bulk of the catalyst, giving rise to a large concentration gradient across the gold–silicon alloy, and resulting in silicon growth similar to that depicted in Figure 3–26. In this figure, the area immediately adjacent to the gold–vapor interface has reached the critical supersaturation required to nucleate a faceted silicon crystal (Figure 3–26B), which in this case it was the supersaturation required to heterogeneously nucleate the crystal on the gold–vapor interface. Spontaneous nucleation of nanowires at the gold–vapor interface has been observed and documented in VLS nanowire growth already for systems with high silicon concentration gradients across the gold–silicon alloy [66]. This spontaneous growth is undesirable for two–dimensional micro–crucible growth as it causes the gold catalyst at the gold–vapor interface to lose its hemispherical morphology and to break up into smaller gold–silicon systems, thus resulting in the run away nanowire growth in front of the bulk of the catalyst as imaged in Figures 3–22A and 3–26A.

Because the whole of the liquid gold–silicon catalyst can at least have a silicon concentration equal to the silicon liquidus equilibrium concentration for a sufficiently slow silane cracking flux, the area of the gold–silicon catalyst where it is energetically favorable to nucleate faceted silicon phase can be extended from the gold–vapor interface to the opposite end of the micro–crucible. Nucleation occurs at localized regions within the micro–crucible where the silicon concentration has reached one of the critical concentrations required for a heterogeneous nucleation event. The gray boxes in Figures 3–25 at $t = t_3$ and 3–26B represent the regions in their respective

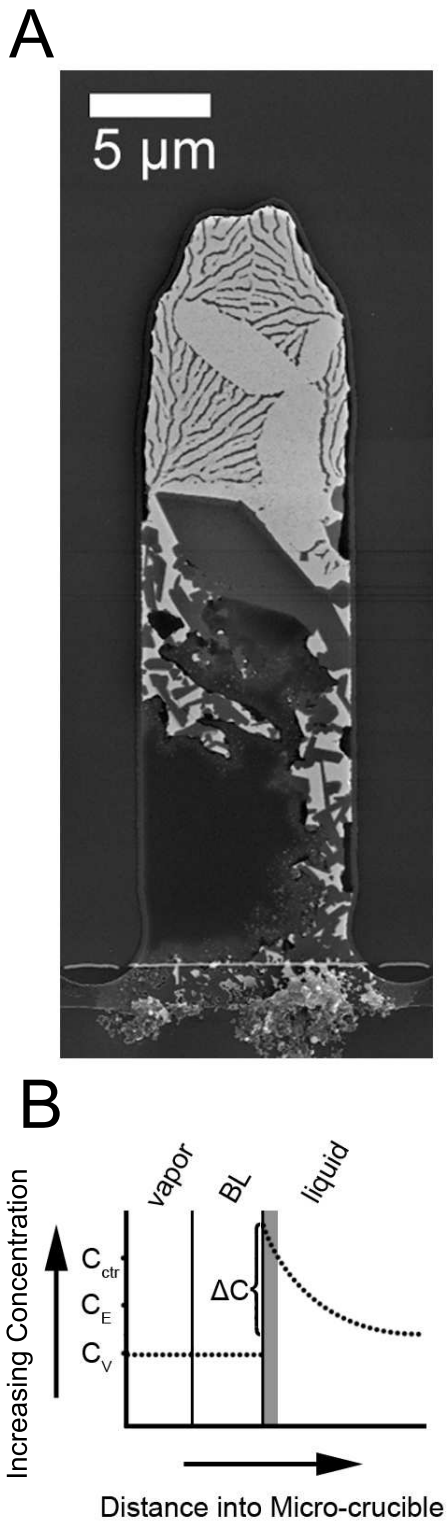

Figure 3–26: A micro–crucible with a 150 nm Au film utilizing 1 nm of Ti as an adhesion layer that was grown at 450 °C for 180 minutes. Figure 3–26A images faceted silicon growth which occurred at the gold–vapor interface due to a large silicon concentration gradient (ΔC) present in the micro–crucible, and subsequent nanowire growth due to the gold–silicon interface becoming unstable and breaking up into discontinuous gold catalysts. Figure 3–26B depicts the silicon concentration profile needed to produce results similar to Figure 3–26A.

micro–crucibles where a heterogeneous nucleation event requiring a critical concentration of C_{crt} could occur. Through experimentation, four specific heterogeneous nucleation locations have been observed: (1) on the gold–vapor interface, (2) at the interface where PECVD silicon oxide encapsulation layer meets the LPCVD silicon nitride amorphous substrate around the perimeter of the micro–crucible, (3) on an impurity in the alloy, or (4) at the gold–vapor interface where a silicon nanowire has impinged upon the liquid catalyst. An impinging nanowire has the lowest supersaturation required to nucleate silicon growth within the bulk of the catalyst and its value should be just slightly above the silicon liquidus equilibrium concentration. Nucleation at the gold–vapor interface and at the interface of the encapsulation layer and the amorphous substrate has been observed in neighboring micro–crucibles [172], suggesting that the critical concentrations required for one or the other are similar. Nucleation from an impurity has been observed in micro–crucibles where the neighboring micro–crucibles do not have nucleated crystals, suggesting a smaller critical supersaturation concentration than the ones required for nucleation at the gold–vapor interface or at the interface of the encapsulation layer and the amorphous substrate.

Once the mechanics of nucleation of the faceted silicon phase in micro–crucibles have been determined, design and geometric factors can be considered to optimized controlled growth of high–quality, two–dimensional silicon films in micro–crucibles. Figure 3–23 shows the growth a faceted silicon crystals in a micro–crucible designed with a neck. The design successfully necked out the twinned grain running down the center of faceted crystal, effectively creating a single crystalline substrate in

the necked region on which semiconducting devices can be fabricated. Successfully engineering growth of spatially controlled, single crystalline semiconductors will most likely always require a necked region in the micro–crucible. How wide the neck can be depends on how well the gold catalyst wets the amorphous walls of the crucible, and rate of growth, so as to keep the catalyst geometry in the neck as stable as possible. For these experiments, the gold catalysts were not able to wet neck widths beyond 7 microns. Crucible widths larger than 7 microns typically resulted in the VLS catalyst breaking up into two separate catalysts, because the gold was not able to wet the entire width continuously.

When aluminum was used as the adhesion layer, large areas of a gray colored third phase were regularly observed around the periphery of the faceted silicon phase, as can be seen in the necked faceted crystal in Figure 9C, Area 1. EDS analysis of this area revealed that both silicon and gold are present in the gray region, suggesting that this phase is one of the metastable gold–silicon phases documented in the literature [22], or an ultra fine gold–silicon eutectic structures. In crucibles where silicon was nucleated without an adhesion layer [172], the gray area was not observed, and it appears this phenomenon is a result of VLS growth with alloyed catalysts. This gray phase has been observed to be more prominent on silicon facets which are adjacent to larger areas of the lamellar gold–silicon phase(Figure 3–24A), suggesting that the metastable, or ultra fine lamellar phase grows as silicon is being rejected from the gold–silicon solution during cooling. This phase also appears to nucleate on preferred orientations of the faceted silicon phase, as it was not conformally deposited on various facets adjacent the lamellar gold–silicon phase. A dry–etch–only preparation

technique needed to be used on samples with the gray phase, as the regions would be quickly etched away by BOE when using wet etchants to remove the encapsulation layer. The chemical reactivity of the gray regions gives more support that this area is one of the metasable phases present in the gold–silicon system rather than a gold–silicon lamellar structure.

3.3.6 Conclusion

By burying the adhesion promoters in a trench etched into the amorphous substrate and encapsulating the adhesion promoter with gold, adhesion layers and alloy compositions can be used to investigate VLS growth which normally would have been impossible due to oxidation issues. Based on the significant difference in results observed using titanium, chromium and aluminum, other VLS capable catalysts such as nickel, copper or indium could provide significantly more reliable results with regards to cleanly etching the alloyed gold catalyst out of the micro–crucible, wetting the surfaces of the micro–crucible, stabilizing the gold–vapor interface during growth or engineered solutionizating of the adhesion layer into the gold catalyst.

The most important design consideration for reliable growth of two–dimensional thin–film growth in micro–crucibles is the elimination of the gold particle dispersion in front of bulk catalyst, which results in undesirable nanowire nucleation. This can be accomplished though further optimization of the wet etch chemistry, novel electrochemical etches [180] [181], or choosing an alloy chemistry which etches cleanly and does not inhibit the catalytic effects of the gold. Nanowires which grow in the micro–crucible due to catalyst instabilities at the gold–vapor interfaces can be controlled by the slow and controlled deposition of silane.

Understanding how the silicon concentration gradient develops in micro–crucibles over time, and at which interfaces faceted silicon phases are most likely to nucleate will aid in the future design of micro–crucibles, where geometric features and thermal treatments will dictate where and how a semiconducting crystal grows. Incorporating necking crucibles allows for the reliable production of single crystalline semiconductors in the necked region.

Precision control of alloy compositions, made possible by this micro–crucible design, enables very detailed studies of solidification phenomenon, such as the unexpected potential third phase observed gold–silicon alloys with aluminum alloying additions. Micro–crucibles are not limited to gold–silicon alloys and could be applied to research concerning microstructures of thin–films [182] [183]. A large number of substances, which can be deposited using electron beam evaporation or magnetron sputtering, can be thermally treated, solutionized, liquefied and cooled at rates which vary by orders of magnitude in micro–crucibles. The semi–electron transparent nature of the encapsulation layer even allows for *in situ* observation of micro–structure evolution using scanning electron microscopy, making the micro–crucible a useful tool for fundamental research.

3.3.7 Acknowledgments

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3.4 Summery of Manuscripts

As can be read in the preceding manuscripts, the initial design considerations and techniques for micro–crucible fabrication has been described in great detail, initial deposition rates of silicon into the gold catalyst have been calculated, a comprehensive model on silicon crystallite growth and lamellar freezing has been proposed, a thorough investigation on preferred orientation and crystalline quality of micro–crucible growth has been conducted, and a comprehensive model on mass transfer and phase transformations in micro–crucibles explained. Due to the difficulty of removing adhesion layers from the micro–crucible fabrication process, two new micro–crucible designs were implemented, one which used a chromium undercut to remove adhesion layers where silicon growth was designed to occur, and one which alloyed the adhesion layer with gold catalyst prior to growth, which resulted in unexpected variations in processing and growth in micro–crucibles. Preliminary silicon growth rates were found to be between $3.17 \times 10^{-2}\,\mu m^3/\min \mu m^2$ and $2.30 \times 10^{-2}\,\mu m^3/\min \mu m^2$, where the area in the denominator represents the initial gold–vapor interface area. Observing the lamellar structure of the gold–silicon which froze after growth gave insight into the processing and initial conditions of the growth, and the results were considered for future experiments. Using EBSD showed that crystals had an aversion to growth with the $\{1\ 0\ 0\}$ surface parallel to the amorphous substrate, and the majority of the grain boundaries observed in the crystals had a special $\Sigma 3$ relationship. After observing thousands of nucleation events in micro–crucibles, it was determined that four specific nucleation events were responsible for all all faceted growth, and with this knowledge, a model describing the diffusion of gas into the micro–crucible,

the transformation of the solid catalyst into a liquid catalyst and the location of the nucleation event of the silicon crystal could be described.

CHAPTER 4
Conclusions and Future Work

4.1 Conclusions

Through this work it has been shown that micro–crucibles are a viable technology to control the growth silicon thin–films form semiconductor applications. Micro–crucibles are a potential enabler of photovoltaics and integrated circuit technologies, and semiconducting films grown laterally from micro–crucibles can be used to enable optical interconnects, three–dimensional transistors and silicon/III–V on–chip integration. Through the use of electron beam analysis, it was found that the crystalline quality of the growth was suitable for seeding CVD, MOCVD, or LPE growth, and potentially can be integrated into high performance electronics; the question remaining being how does the doping from the catalytic melt affect electron mobility and carrier lifetime within the grown crystals. One way to mitigate the effects of doping would be to engineering the catalysts with more benign metals with regards to electronic traps, but this would also require more specialized processing equipment. Engineered catalysts also offer an avenue to control the growth process within micro–crucibles, such as enhanced wetting of the amorphous sidewalls. Through observing growth in micro–crucibles, it was also noted that successful growth requires precision control of the deposition rate, and by extension, the processing temperature. Further progress in the field of semiconductor growth with micro–crucibles will require some

custom processing tools to address the issues associated specifically with fabrication of and growth within micro–crucibles.

4.2 Future Work

The immediate next step for research involving the lateral growth of semiconducting materials within amorphous micro–crucibles is the drafting of a manuscript to be published on the transmission microscopy work outlined in Section 1.6. Silicon crystal morphology, grain boundary relationships, dislocation analysis, nucleation mechanisms, comparisons between bright–field TEM imaging and transmission electron imaging in scanning electron microscopes, applications for t–EFSD, and specimen preparation techniques can all be expanded upon and included in the manuscript. A summation of these findings would be the fourth publication taken from this original work and represents completion of the peer review process for all its major findings.

Practically, further work needs to be done on the fabrication of micro–crucibles so that more of the CVD growth results are more consistent and controllable, which is a requirement for the electronic integration and testing of micro–crucible grown silicon. As outlined in Section 2.2.3, the encapsulation layer determines the robustness of the micro–crucible test structure with regards to the yield of micro–crucibles capable of growing silicon film laterally i.e. not broken or deformed, and the integrity of the experimental assumption that the semiconductors grow laterally only i.e. do not deform the original, predefined volume of the micro–crucible as they grow. Experiments and literature reviews should be conducted to understand the maximum width a PEVCD deposited silicon oxide or silicon nitride membrane can have when

only supported from both ends. Deformation of these membranes at high temperatures should be looked into as well. Section 3.3.5 describes the difficulty of removing gold from the micro–crucible by wet etching, particularly when the gold has been alloyed with it adhesion layer. An optimization between catalyst alloy composition and etching technique needs to be reached if reliable growth is to be achieved, and novel electrochemical etches [180] [181] should be looked into. Using reactive carrier gases such as HCl could also be a way to clean the micro–crucibles for unwanted metal residues and promote more controlled growth.

Experimentally the next logical step would be to understand the electrical properties of silicon thin–films growth within microcrucibles, particularly an analysis of a PN junction would be more a fundamental study of electron minority carrier lifetime within VLS grown films, and more applicable to photovoltaic devices. Also interesting to observe would be the dependency of electronic properties on VLS catalyst choice. It is well know that gold is detrimental to electron minority carrier lifetime in silicon, but finding an alternative catalyst or an alloying addition that mitigates this effects would a significant advantage for VLS research, as the deep–level electronic defects associated gold in silicon are the primary drawback of the technique.

Of course the continued experimentation on VLS catalyst composition can continue using micro–crucibles, as any metal which can be reliably deposited as a thin–film and selectively etched using wet chemistry, or even gas phase chemistry, is a candidate for micro–crucible fabrication. The thermodynamics of micro–alloyed and tertiary systems are the primary candidates for study, and investigations into the

processing condition dependency of low melting point alloys, like the indium example given in Section 1.2, can be investigated further. Also of interest would be how changes in the gas chemistry, for example silicon tetrachloride ($SiCl_4$) or disilane (Si_2H_6) and their higher reaction temperatures, change the solubility silicon in VLS catalyst solutions and alter the energetics of silicon nucleation within micro–crucibles. Understanding the etching effect chlorides have on VLS catalyst during growth, which is questionable [87] [88] [77] and understudied, would lead to additional research projects which vary the gas chemistry of VLS growth as well.

Because transmission electron microscopy samples have been prepared so that micro–crucible growth can be easily imaged, laterally grown silicon films from the micro–crucibles are a potential platform from which grain boundaries in silicon can be studied. Particularly useful is the large viewable areas achievable using micro–crucible grown films as TEM specimen, where a larger variety of grain boundaries can be studied when compared to conventional thinning techniques. This means that coherent and incoherent $\Sigma 3$ boundaries, as well as higher energy $\Sigma 5$ and $\Sigma 9$, can be easily found and observed, ideally with HRTEM. Recent modeling work on grain boundary mobility [184] would be complemented by experimental observations of grain boundary motion of laterally grown films, heated with a special stage and observed with either a TEM or a SEM operating in transmission mode. Also interesting is a series of works [185] [186] which analysis electrical activity of silicon grain boundaries using electron-beam-induced current (EBIC) and could be applied to lateral growth either in a STEM or a SEM operating in transmission mode. Using

EBIC, it has been shown that metals like iron can accumulate at the Σ3 gain boundaries of polycrystalline silicon [186], making the parasitic effects of grain boundaries on electron mobility even more pronounced. It can be observed if the VLS catalyst has an effect like this for laterally grown crystals with grain boundaries, and if so, can it be optimized with catalyst choice.

Lastly, the stated goal of this research was to create large area semiconductor substrates, and thus proving the concept by using VLS grown silicon in micro–crucibles as seed crystals for vapor phase or liquid phase epitaxial growth is of significant interest. This would require new micro–crucible designs to be developed and a dedicated, long–growth CVD reactor to be acquired. Once seeding from micro–crucible grown crystals has been proven, work on applying the micro–crucible growth technique should be preformed on other semiconductors like germanium or the III–Vs. It is from this work that the stated goal of developing low cost substrates for photovoltaic materials would be achieved.

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