# Reducing Measurement Uncertainty in a DSP-Based Mixed-Signal Test Environment

*by*

*Chris Taillefer, B.Eng. 2000*

Department of Electrical and Computer Engineering

McGill University, Montréal

March 15th, 2003

---

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Master of Engineering.

*Your file Votre référence*
*ISBN: 978-0-494-32642-8*
*Our file Notre référence*
*ISBN: 978-0-494-32642-8*

# Acknowledgements

The enthusiasm, dedication, and understanding of Professor G.W. Roberts have made this degree enjoyable, intellectually stimulating, and rewarding. The skills and experiences that I have acquired through his leadership and guidance will be the greatest asset for all my future endeavors. For this I extend my deepest gratitude towards Dr. Roberts.

I would like to offer my appreciation to all members of the MACS lab for their friendship and support. Collectively, they are a tremendous pool of knowledge for which I could not have succeeded without. Specifically, I would like to thank Mohamed Hafed for all his advice and technical support.

I would like to thank my Mother for all her support throughout my degree (and my life). She has facilitated every opportunity offered to me, supported every decision that I made, and encouraged me towards success.

Being a student is stressful and at times emotionally challenging. I am incredibly grateful to all my family and friends who brought social balance into my life.

Finally, I would like to acknowledge the financial support of NSERC and Micronet, and the facilities offered by the Canadian Microelectronics Corporations (CMC), which were essential to complete this work.

# Abstract

FFT-based tests (e.g. gain, distortion, SNR, etc.) from a device-under-test (DUT) exhibit normal distributions when the measurement is repeated many times. Hence, a statistical approach to evaluate the accuracy of these measurements is traditionally applied. The noise in a DSP-based mixed-signal test system severely limits its measurement accuracy. Moreover, in high-speed sampled-channel applications the jitter-induced noise from the DUT and test equipment can severely impede accurate measurements.

A new digitizer architecture and post-processing methodology is proposed to increase the measurement accuracy of the DUT and the test equipment. An optimal digitizer design is presented which removes any measurement bias due to noise and greatly improves measurement repeatability. Most importantly, the presented system improves accuracy in the same test time as any conventional test.

An integrated mixed-signal test core was implemented in TSMC's 0.18 μm mixed-signal process. Experimental results obtained from the mixed-signal integrated test core validate the proposed digitizer architecture and post-processing technique. Bias errors were successfully removed and measurement variance was improved by a factor of 5.

# Résumé

Les analyses basées sur le FFT (ex. SNR, distorsion, etc.) effectués sur un dispositif de test (DUT) démontrent une distribution normale lorsque les mesures sont répétées plusieurs fois. A cet effet, une méthode statistique est traditionnellement utilisée afin d'évaluer la precision de ces mesures. Le bruit dans un système de test est un facteur qui limite sévèrement la précision d'une mesure. En outre, dans des applications d'échantillonnage haute-vitesse d'un signal analogique, le bruit de l'incertitude de temps (jitter) provenant du DUT et de l'équipement de test peut entraver sérieusement la précision des mesures.

Afin d'améliorer la précision des mesures du DUT ainsi que de l'équipement utilisé pour l'analyse, une nouvelle structure du convertisseurs analogique-numérique ainsi qu'une méthode de traitement de données sont proposés. Cette thèse présente une architecture optimal de convertisseurs analogique-numérique qui permet d'éliminer toute erreur de tension causée par le bruit lors des mesures et permet aussi d'obtenir des résultats consistant dans le temps. Cet architecture du système est exécutée dans le même laps de temps que tout autre test conventionnel.

Un système de test pour les circuits intégrés mixtes a été conçu et fabriqué dans un procédé de TSMC 0.18 μm. Les résultats obtenus des expériences faites sur ce circuit valide l'architecture de convertisseurs analogique-numérique présenté ainsi que la technique de traitement de donné proposé. Les erreurs de tension ont été éliminées avec succès et la variance des mesures a été améliorée d'un facteur de 5.

# Table of Contents

# List of Figures

# Chapter 1: Introduction

## *1.1 - Motivation*

System-on-Chip (SoC) is one of the main driving forces that have been re-shaping the consumer electronics industry. The SoC alternative to conventional systems design is growing in popularity as the device packing density escalates due to the evolution of semiconductor technology. Moreover, the decrease in semiconductor feature size is permitting the increase of clock frequencies and component operating speed. These advancements necessitate the integration of system components due to package parasitics and lengthy interconnect. Furthermore, SoC devices offer a cheaper and compact solution to the consumer electronics industry.

The amalgamation of digital, analog, and mixed-signal components into a single integrated circuit (IC) presents test engineers with tremendous difficulties. Typically, the designers of SoC devices iterate through several manufacturing runs to produce a high performance and robust device. From each IC fabrication run of the SoC the test engineers must quickly feedback to the designers any design faults and the performance characteristics. Full production of a SoC begins once the design performance is satisfactory. Further test requirements, known as production testing, are imposed to ensure that each device is free from defects and meets the required specifications. Often the design characterization and production testing are done by different groups thus increasing the cost and time-to-market.

Mixed-signal components are traditionally tested using a digital-signal-processing (DSP) based test environment, as shown in Figure 1.1. The device under test (DUT) could be the arbitrary waveform generator (AWG), analog channel, digitizer, or any subcomponent or combination thereof. The DSP-based test technique implements signal stimulation from a waveform source memory and captures test results into a digital waveform capture memory.

The accuracy and precision of measurements taken in a DSP-based test environment are severely limited by the measurement uncertainty of the test equipment. In a production test environment, test limits are selected based on the combined performance of the DUT, test apparatus, and process variability. In order to ensure a high quality product, guardbands are chosen to be very conservative (e.g., $6\sigma$). Large guardbands will inherently decrease yield, as good parts will be discarded.

Test equipment measurement uncertainty arises from various independent noise sources including thermal noise, quantization noise, jitter-induced noise, power supply noise, distortion, and electromagnetic interference (EMI). This in turn causes the repeatability to decrease. In addition, if an attribute of noise is the measurement parameter of interest, an inherent measurement bias will be introduced by the test equipment.

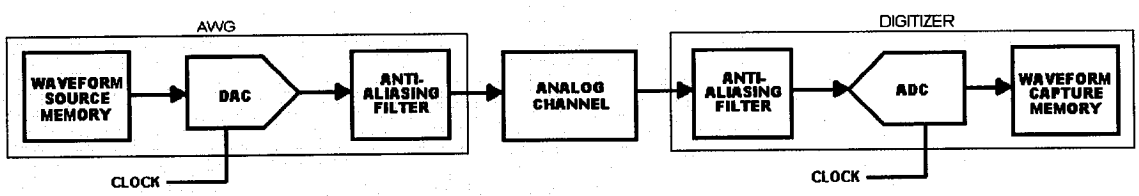



**Figure 1.1: DSP-Based Test Environment**

In critical test situations, employing high performance test equipment is the obvious solution. However, in very high-speed applications even the best measurement instruments will be limited by jitter effects in the sampling process [1]. Figure 1.2 demonstrates a fundamental threshold that jitter-induced noise imposes on analog-to-digital converters (ADCs). This survey clearly indicates that jitter (or aperture uncertainty) is the limiting contributor on ADC dynamic performance. To make matters worse, jitter-induced noise is also frequency dependent. Hence, measurement accuracy and precision will degrade as clock frequency and test signal frequencies increase.

Measurement precision may be improved by taking more samples of the test parameter. Undesirably, this will increase test time. Furthermore, in the case of noise measurements, more samples will not eliminate or reduce the measurement bias introduced by the test equipment.

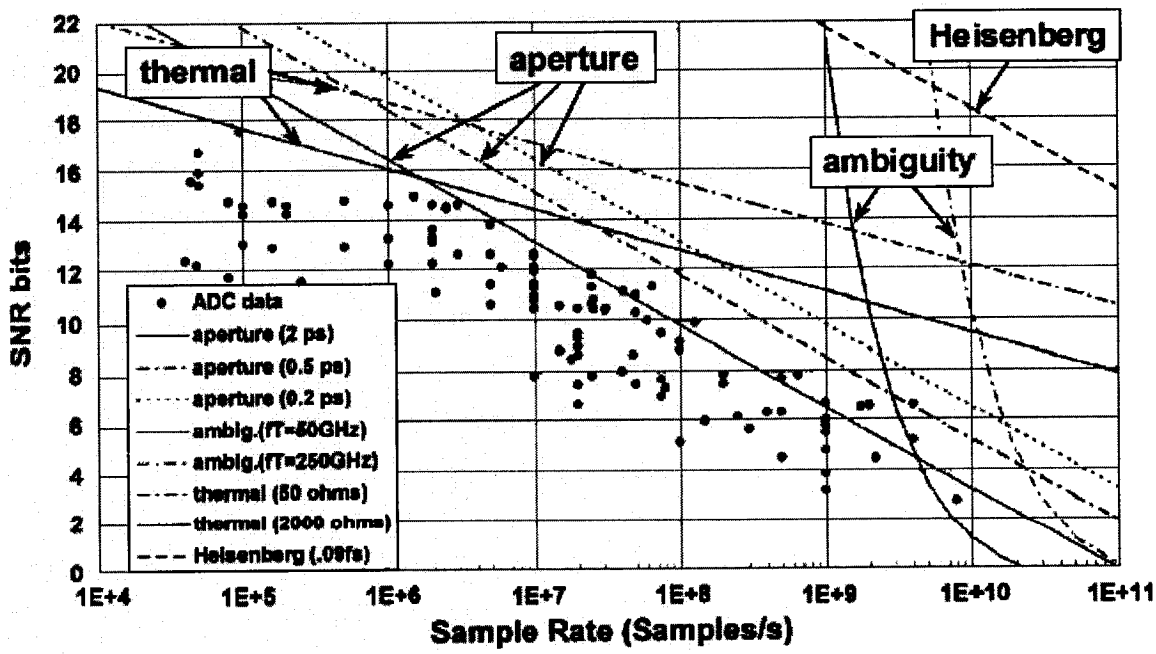



**Figure 1.2: ADC Performance Limiters Due to Aperture Uncertainty, Thermal Noise, and Comparator Ambiguity [1]**

The characterization and production testing of mixed-signal SoCs is becoming more challenging as SoC operating speed and design complexity increase. The requirements of the conventional test approach using automated test equipment (ATE) are increasing in cost and development time [2]. Moreover, the ATE performance is proving inadequate due to the relationship between operating speeds and the inherent noise resulting from interconnection and packaging issues [3].

The current mixed-signal ATE test solutions involve off chip stimulus and measurement through SoC package pins or IC probes. Thus, a huge number of package I/O pins are required for test [4]. The tradeoffs between test development time, device test time, ATE requirements and SoC design constraints (e.g. I/O pads) is one of the greatest challenges facing the test engineering paradigm.

The integrated mixed-signal test core [5] provides an alternative to conventional test of mixed-signal ICs. This work proposes that the test apparatus be integrated within the mixed-signal SoC. Test requirements of mixed-signal circuits are extremely diverse. As such, the test core incorporates an arbitrary waveform generator (AWG) for signal stimulus and a digitizer to capture analog results.

The test core solution boasts many advantages. By integrating the test equipment many interconnect and packaging problems are resolved, the number of test I/O pins is reduced, and parallel testing is facilitated. Another advantage is that the characterization and production testing can be performed by the same test core. In short, the test core approach offers the ability to improve product time-to-market and reduce cost as the constraints on development and test time are relaxed and the ATE requirements are moderated.

In order to reduce costly silicon area, a very small, mostly digital, digitizer architecture was developed to implement the test core. One of the most significant tradeoffs of this compact digitizer design is an increase in test time. The digitization algorithm, known as the multipass method, is responsible for the time-intensive capture of analog information.

This thesis presents a new digitizer architecture and processing techniques that can reduce the measurement uncertainty and remove the test equipment bias error. Moreover, the proposed processing unit can remove the effects of jitter from dynamic noise measurements. Most importantly, this approach does not add any more time to the test. A multi-digitizer mixed-signal test core was constructed as a means to demonstrate the effectiveness of the proposed measurement uncertainty reduction technique.

## *1.2 - Thesis Outline*

Chapter 2 introduces the DSP based test environment and the effects of noise on measurement uncertainty. The DUT measurement uncertainties taken in a noiseless test environment are discuss first in order to gain insight into the types of measurements and their precisions (or repeatability) that will be obtained in a DSP-based test system. The additive effects of test equipment uncertainty are then presented.

A new digitizer architecture to remove bias errors and improve repeatability is presented in Chapter 3. These improvements are achieved by incorporating multiple digitizers while operating in a time-interleaved or simultaneously-sampling approach. Simulation results are demonstrated to show the validity of the processing methodology.

A particular application is revealed in Chapter 4 which demonstrates that the crippling effect of jitter may be separated for measurement of a sampled-channel device such as a digital-to-analog-converter (DAC) or ADC.

The test core was implemented in a time-interleaved quintuple-digitizer configuration using the 0.18 $\mu$m mixed-signal CMOS process from Taiwan Semiconductor Manufacturing Corporation (TSMC). This design will show a method to reduce a measurements precision error. A second device, the simultaneously-sampling dual-digitizer, was fabricated to demonstrate a technique for bias removal. Chapter 5 introduces the mixed-signal test core and documents the implementation of these two devices. The performance of the test core components are demonstrated through post-extracted HSPICE simulation results.

The experimental setup and results from the implemented test core are presented in Chapter 6. A characterization of the test core is presented. The effectiveness of the bias removal and uncertainty reduction processes are emphasized.

Finally, Chapter 7 summarizes the thesis and draws conclusions on the work presented. The extensibility of the noise reduction technique is discussed and future works are also proposed.

# Chapter 2: Measurement Uncertainty in a DSP-Based Test Environment

## *2.1 - Introduction*

The objective of any mixed-signal IC test is to acquire information about the DUT in the absence of all errors (e.g. gain), or in the presence of DUT errors (e.g. signal-to-noise ratio). Every measurement that is taken of a DUT is not 100% repeatable. In other words, there is a certain degree of error among repeated measurement. If a measurement is repeated, then the data collection of that measurement may be used to generate a probability distribution function (PDF). From the PDF we may obtain the mean value and a measure of the spread (i.e. standard deviation) of the tested parameter. Using the mean and standard deviation, a judgment of the accuracy of the test may be concluded.

The device to be tested will experience noise from various sources, which will affect the test parameter. The noise itself is assumed to be normally distributed having a mean value of zero. In a DSP-based test system, the DUT output is collected into digital memory. Most test parameters are extracted in the frequency domain by first applying a Fast-Fourier Transform (FFT). FFT-based measurements may modify the distribution of the noise in the test parameter. Depending on the type of measurement, the RMS value of the complex FFT result may generate Gaussian, Rayleigh, or Ricean distributions [6].

In a noiseless test environment, the DUT noise will yield measurements with uncertainty. In a practical test environment the noise of the test equipment will also produce an additive uncertainty to the measurement. In order to gain a better understanding of the measurement uncertainty of the DUT, Section 2.2 introduces the various DUT measurements and their distributions taken in a noiseless DSP-based test environment. Realistically, all test equipment exhibit noise characteristics, especially when operating at high-speeds and high-resolutions. Hence, the additive effects of test equipment uncertainty are discussed in Section 2.3.

## *2.2 - DSP-Based Measurement Uncertainty with Noiseless Test Equipment*

### 2.2.1. System Model

The most general DSP-based test system for characterizing an arbitrary mixed-signal device (called the device-under-test or DUT) is illustrated in Figure 2.1. Such a test station consists of an arbitrary analog waveform generator (AWG), a source memory (SMEM) for exciting the digital port of a mixed-signal device, a digitizer (DIG) that samples an analog waveform, and a capture memory (CMEM) for collecting digital data from a digital output port.

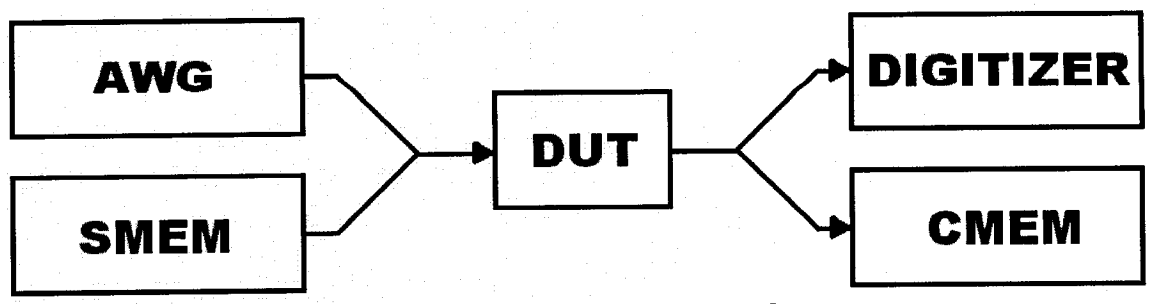



**Figure 2.1: Generic DSP-Based Test System**

Without loss of generality, there are four possible signal paths involving the four components of the DSP-based test system: (i) AWG-DUT-DIG, (ii) AWG-DUT-CMEM, (iii) SMEM-DUT-DIG, and (iv) SMEM-DUT-CMEM. Regardless of the test configuration, by definition, a mixed-signal test path will always include a DAC and an ADC in its signal path. Hence all measurements will be subject to sampling effects.

The noise properties for a typical DSP-based test configuration, in the absence of test equipment noise, may be generalized with the model shown in Figure 2.2. Here the DUT is modeled as an arbitrary analog channel device with gain and additive noise. It should be noted that the following discussion applies equally if the DUT is a sampled-channel device such as a DAC or ADC. The input and output signals of the system are denoted $v_{IN}(t)$ and $v_O(t)$, respectively. The noise generated by the DUT is modeled by a noise source $n_C(t)$. In addition, the DUT may have a gain other than unity and is therefore denoted by its impulse response $h_C(t)$.

The test equipment (i.e. the DAC and ADC) are assumed to be free from all noise sources, including quantization. For simplicity, we will also assume that the test instruments have a unit impulse response (i.e., unity gain).

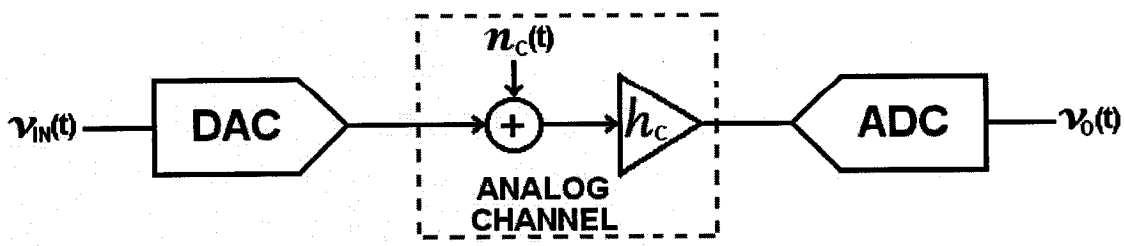



**Figure 2.2: Analog Channel Device Tested in a Noiseless DSP-Based Test Environment**

### 2.2.2. FFT-Based Calculation Distributions

In a DSP-based test system we are often interested in collecting N samples from the DUT, performing a FFT to map the information into the frequency domain, and finally determining the gain, noise and distortion metrics for the DUT. However, in the presence of the noise generated by the DUT itself, the metrics will vary with the sample set. In turn, we do not obtain a single value for each metric, but rather a distribution of measured values.

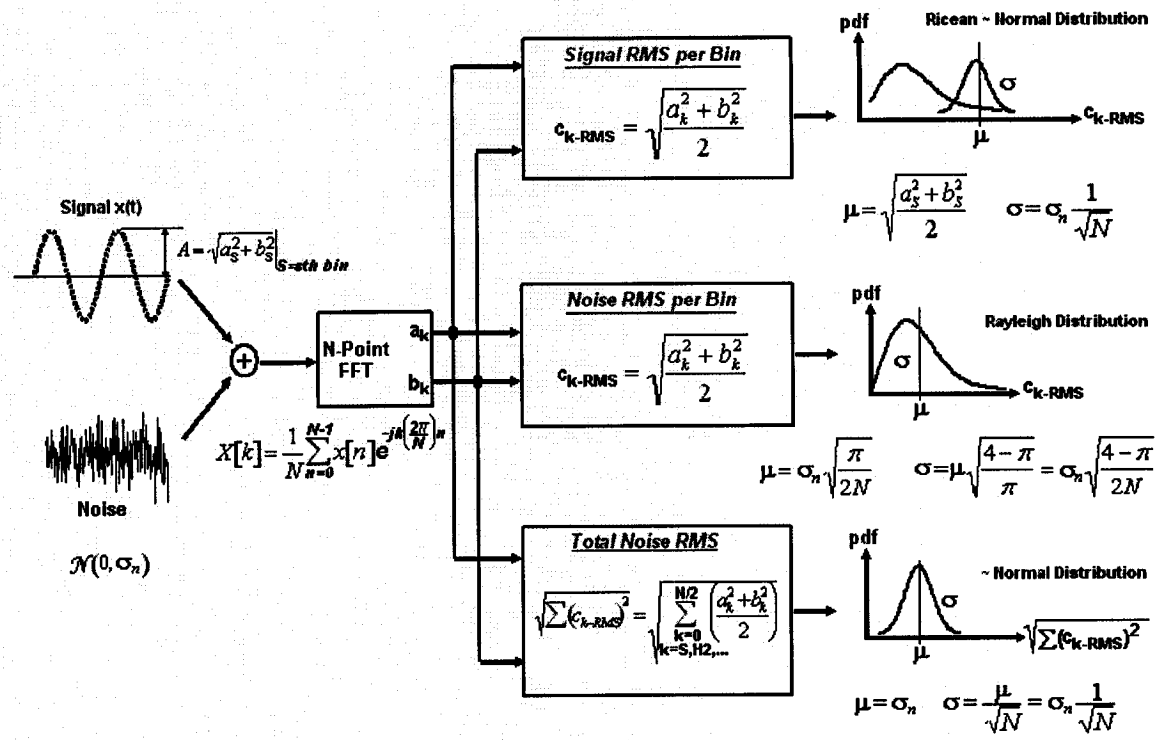
To quantify this effect, consider a sample set consisting of N samples. If a FFT is performed on this set, the real and imaginary parts from the k-*th* bin of the FFT, denoted $a_k$ and $b_k$, can be used to compute the RMS value of the signal level present in that bin according to

$$c_{k-RMS} = \sqrt{\frac{a_k^2 + b_k^2}{2}}. \tag{2.1}$$

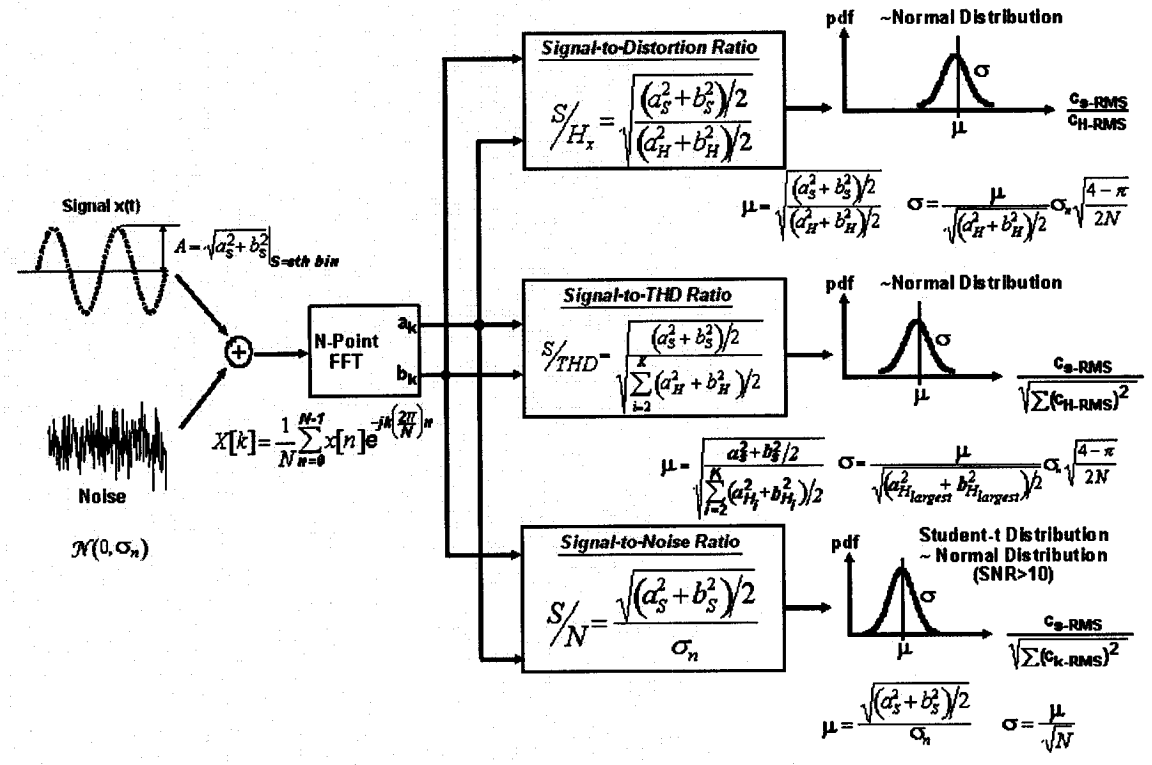
If we assume that the sample set was obtain in the presence of Gaussian noise with standard deviation $\sigma_n$, then the RMS value of the s-th signal component will have a Ricean probability density function [6] with mean and standard deviation given by

$$\mu = \sqrt{\frac{a_S^2 + b_S^2}{2}} \qquad \sigma = \sigma_n \frac{1}{\sqrt{N}}. \tag{2.2}$$

Clearly, the larger the size of the sample set N, the tighter the distribution. Fortunately, from a mathematical perspective, when $\mu/\sigma >> 10$, the Ricean distribution can be approximated by a Gaussian or normal distribution with mean and standard deviation given by Equation (2.2).




**(a) RMS Signal Calculations**




**(b) Ratio Calculations**

**Figure 2.3: Spectral Measurement PDFs Obtained from an FFT in the Presence of Gaussian Noise**

When no component of the signal is present in a FFT bin, then the RMS value of that bin will have a Rayleigh distribution [6] with parameters

$$\mu = \sigma_n \sqrt{\frac{\pi}{2N}} \qquad \sigma = \sigma_n \sqrt{\frac{4-\pi}{2N}}. \tag{2.3}$$

Here the mean value of a noise-per-bin measurement is directly dependent on the amount of noise present in the measurement. When all such noise bins are combined we obtain the total RMS noise value [7] according to

$$Noise = \sqrt{\sum_{\substack{k=0, \\ k \neq S, H2, \ldots}}^{N/2} \left( \frac{a_k^2 + b_k^2}{2} \right)}, \tag{2.4}$$

whose PDF can be approximated by a normal distribution with mean and standard deviation given by

$$\mu = \sigma_n \qquad \sigma = \sigma_n \frac{1}{\sqrt{N}}. \tag{2.5}$$

The three PDFs are depicted in Figure 2.3(a). In part (b) of the same figure, the PDFs related to several ratio-type measurements; signal-to-distortion, signal-to-total-harmonic-distortion, and signal-to-noise ratio are also shown. In all three cases, the PDFs are very well approximated by normal distributions with the parameters listed in Figure 2.3(b).

## 2.3 - Additive Measurement Uncertainties

### 2.3.1. Noise Model

Realistically, DSP-based test equipment such as DACs and ADCs will be riddled with noise components arising from thermal, quantization and jitter-induced effects. A noise model depicting a practical DSP-based test system is illustrated in Figure 2.4. The noise components of the DAC and ADC are modeled by noise sources $n_{DAC}(t)$ and $n_{ADC}(t)$, respectively. The analog channel continues to be represented by noise source $n_C(t)$ and impulse response $h_C(t)$. It is assumed that the gains of the DAC and ADC are either unity or have been calibrated within the bandwidth of interest.

### 2.3.2. Measurement Distributions

As demonstrated in Section 2.2, repeated measurements of a DUT taken in a DSP-based test system exhibit normally distributed results having a mean value, $\mu$, and standard deviation, $\sigma$. When test equipment noise is injected into the system (Figure 2.4) then the mean and deviation of the DUT will differ from those observed at the test system output (i.e. ADC output).

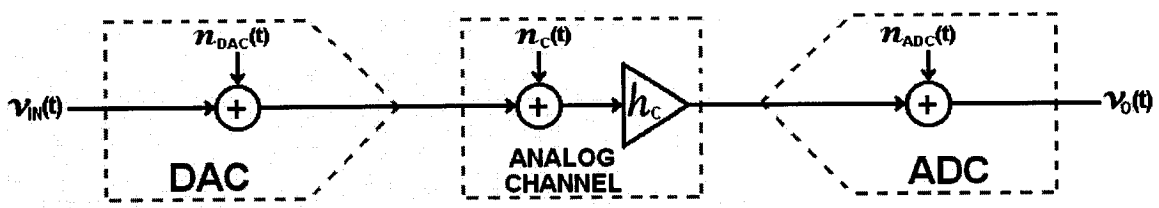



**Figure 2.4: Noise Model for a Generic DSP-Based Test**

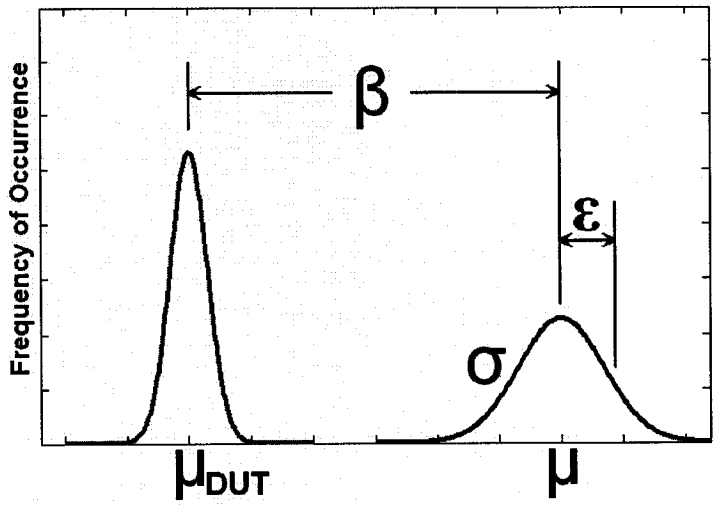



**Figure 2.5: Bias and Precision Errors in a Repeated Test Parameter Measurement**

There are two types of error mechanisms that contribute to the reduced accuracy of a test system: bias error, and precision error. These are illustrated in Figure 2.5. When a repeated measurement is observed, the bias error, β, given by

$$\beta = \mu - \mu_{DUT}, \tag{2.6}$$

is the difference between the true mean value of the DUT and the actual mean value obtained at the ADC output.

For many test parameters (e.g., gain and level tests) the bias error is systematic and may be eliminated by calibration. However, when the test metric involves a parameter of noise then it is impossible to eliminate the measurement bias by simply increasing the size of the sample set.

The precision error, denoted by ε, for a single test parameter sample is the difference between the sampled value and the biased output mean value, μ. If

the measurement is repeated N times, then the standard deviation, σ, of the precision errors is given by

$$\sigma = \sqrt{\frac{1}{N}\sum_{n=1}^{N}\varepsilon^2}. \tag{2.7}$$

We normally employ confidence intervals to establish a measure of accuracy of a measurement. Hence, the percentage accuracy of a measurement is the bias error plus-minus the level of uncertainty associated with the spread in the measurement value. For example, a 95% accurate measurement may be quantified by the following:

$$Accuracy_{95\%} = \beta \pm 2\sigma. \tag{2.8}$$

Hence, to improve accuracy we must reduce the bias error to zero and minimize the standard deviation of the measurement.

If a measurement is repeated many times, then the collection of test parameter results, $X_O$, will have a mean, μ, and a standard deviation, σ. Let us assume for an arbitrary test parameter that the mean value contributions of the DAC, analog channel, and ADC are respectively $\mu_{DAC}$, $\mu_{DUT}$, and $\mu_{ADC}$. In the case of a RMS signal level parameter, based on the analysis of Section 2.2, together with the assumption that the noise distributions are all Gaussian, one can show that the mean value of $X_O$ may be expressed as an additive sum of individual mean values assuming the gain of the DUT is unity, i.e.,

$$\mu = \mu_{DAC} + \mu_{CH} + \mu_{ADC}\ . \tag{2.9}$$

However, in the case of a noise parameter, the mean value of $X_O$ is the square-root of the sum of squares of individual means, i.e.,

$$\mu = \sqrt{\mu_{DAC}^2 + \mu_{CH}^2 + \mu_{ADC}^2} \ . \tag{2.10}$$

The standard deviation of $X_O$ for both a RMS signal parameter and noise parameter, is simply the square-root of the sum of individual variances, i.e.,

$$\sigma = \sqrt{\sigma_{DAC}^2 + \sigma_{CH}^2 + \sigma_{ADC}^2} \ . \tag{2.11}$$

## *2.4 - Summary*

The measurements of a DUT parameter, such as gain and signal-to-noise ratio, are subject to the noise inherent in the DUT. The accuracy of a repeated DUT measurement in a noiseless test environment will reveal an accurate measure of the mean value. However, the precision of the measurement will depend on the DUT noise.

In a practical DSP-based test environment, a repeated DUT measurement will combine the noise of the DUT and test apparatus. Hence, the accuracy of the measurement may be biased while the precision reduced.

In order to obtain a better measure of the DUT, the test equipment uncertainty should be reduced. Furthermore, for some test parameters, a reduction in DUT uncertainty would also be appreciated.

# Chapter 3: New Digitizer Architecture for Reducing Measurement Uncertainty

## *3.1 - Introduction*

A typical mixed-signal DSP-based test environment incorporates test equipment such as a DAC and ADC, as shown in Figure 3.1. The measurement of the DUT, whether it is the DAC, ADC, or analog channel device, will always be influenced by the noise of the DUT combined with that of the test equipment. This was presented Chapter 2.

If a repeated measurement is taken from the system output (i.e. the ADC output captured into memory), then a FFT analysis may be performed to obtain the test parameter of interest. It was shown in Chapter 2 that the actual distribution of a repeated test measurement may not be exactly Gaussian, however, for large signal levels the PDFs of the test parameter are approximately normally distributed.

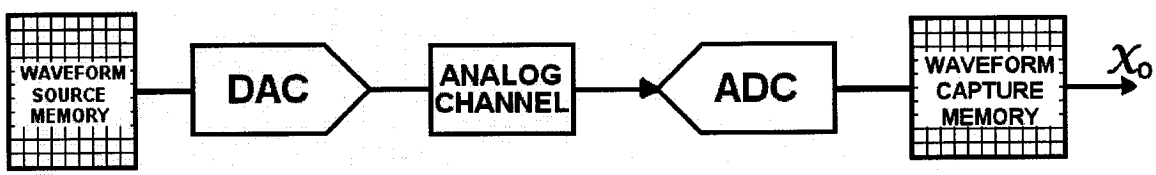



**Figure 3.1: Mixed-Signal DSP-based Test Environment**

Hence, the output of the DSP-based test system, $X_O$, will be have mean value,

$$\mu = \frac{1}{N}\sum_{n=1}^{N} X_O(n), \tag{3.1}$$

and standard deviation,

$$\sigma = \sqrt{\frac{1}{N}\sum_{n=1}^{N}[X_O(n)-\mu]^2}. \tag{3.2}$$

Recall from Chapter 2 that the mean and deviation of a measurement may be increased due to the bias and precision error introduced by the measurement equipment noise. A new digitizer architecture is proposed to reduce precision error and remove bias error from measurements in a DSP-based test environment. In section 3.2, the digitizer architecture and post-processing technique is described to reduce precision errors. This method incorporates an interleaving ADC capture algorithm. A simultaneously-sampling processing technique to remove bias errors from a measurement is presented in Section 3.3. An optimal design utilizing a combination of simultaneously-sampling and time-interleaving ADCs is revealed in Section 3.4. Finally, MATLAB simulations proving the legitimacy of the proposed concepts are demonstrated in Section 3.5.

## *3.2 - Interleaving ADC Measurement*

Many test parameters taken with a DSP-based test system have a bias error that is either negligible or easily calibrated (e.g. DC offset and gain error). For these tests, measurement accuracy can only be improved by reducing the measurement precision.

An obvious solution to reduce the noise variance is to obtain more samples of the test parameter. However, to reduce the variance (the square of the standard deviation) by a factor of 2 the test time would have to be doubled.

In order to reduce the measurement standard deviation, additional ADCs may be used, operating in a time-interleaved fashion to capture the data. Note, however, that each sample is not collected in the tradition time-interleaved approach, as this would only make the problem worse due to ADC mismatch [8].

The interleaved dual-ADC architecture consists of two ADCs (denoted as ADC A and ADC B) in the digitizer path of the DSP-based test system, as shown in Figure 3.2. After the waveforms from both ADCs are captured into memory, FFTs are applied and the same test parameter is extracted independently from both ADC outputs (denoted as $X_{OA}$ and $X_{OB}$). Next, a third test parameter $X_O$ is create by averaging $X_{OA}$ and $X_{OB}$, according to

$$X_O = \frac{X_{OA} + X_{OB}}{2} . \tag{3.3}$$

Assuming $X_{OA}$ and $X_{OB}$ are normally distributed independent random variables with means, $\mu_{OA}$ and $\mu_{OB}$ and standard deviations, $\sigma_{OA}$ and $\sigma_{OB}$, the new random variable $X_O$, will have a mean value of

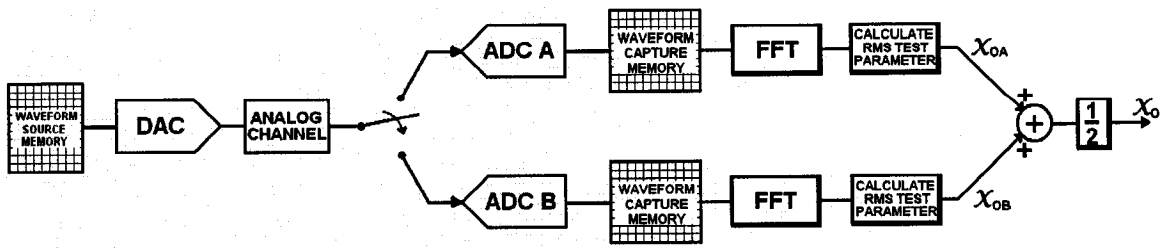



**Figure 3.2: Two Time-Interleaved ADC Method and Post-Processing Algorithm**

$$\mu = \frac{\mu_{OA} + \mu_{OB}}{2}, \tag{3.4}$$

and a standard deviation given by

$$\sigma = \sqrt{\frac{\sigma_{OA}^2 + \sigma_{OB}^2}{4}}. \tag{3.5}$$

Since the set $X_{OA}$ and $X_{OB}$ have roughly the same standard deviation, the overall standard deviation may be approximated as

$$\sigma \approx \frac{\sigma_{OA}}{\sqrt{2}} \approx \frac{\sigma_{OB}}{\sqrt{2}}. \tag{3.6}$$

Hence, the standard deviation of the data collected from a single ADC is reduced by a factor of 1.414.

Extending this idea to include K interleaved ADCs can be shown to reduce the total measurement standard deviation by the factor $\sqrt{K}$. This of course assumes that the noise sources are all uncorrelated; a condition that is usually satisfied in practice.

## *3.3 - Simultaneous ADC Measurement*

Any measurement of a noise metric (e.g. total RMS noise) will be subject to a non-zero bias error caused by the noise generated by the measurement equipment itself. To circumvent this loss of precision, a similar digitizer architecture to the one used in the time-interleaved architecture of Figure 3.2 may be used. However, unlike the time-interleaved approach, each ADC is made to sample the input signal at exactly the same time. In this way, the noise

bias error can be eliminated. A schematic diagram illustrating this approach is shown in Figure 3.3. Note that the time-interleaving and the simultaneous sampling approach have identical components, only the digital clock generation circuit is different.

The idea behind this approach is derived from the method described in [9] and [10], albeit, the method developed here is more time efficient.

Both ADCs simultaneously sample the input signal and record their data in the waveform capture memory. A FFT analysis is then performed on each data set (denoted $X_{OA}$ and $X_{OB}$), and the noise metric is derived. If the test equipment is noiseless, then these two noise metrics should be identical (i.e., $X_{OA}=X_{OB}$). Of course, the difference between these sets of data represents the noise added by the two ADCs. Taking the difference of these two data sets, which can be performed directly in the frequency domain using the complex spectral coefficients obtained from each FFT output, we obtain a third signal described by

$$FFT\{v_{OAB}(t)\} = FFT\{v_{ADCA}(t)\} - FFT\{v_{ADCB}(t)\}. \tag{3.7}$$

Subsequently, a third noise metric can be computed from this new data set, which we denote as $X_{OAB}$.

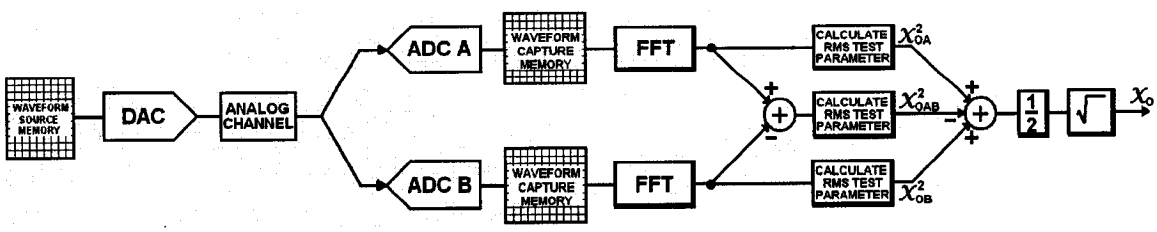



**Figure 3.3: Simultaneously-Sampling Dual-ADC Method and Post-Processing Algorithm**

Statistically, $X_{OA}$, $X_{OB}$ and $X_{OAB}$ will be approximately Gaussian with the following mean values:

$$\mu_{OA} = \sqrt{\mu_{DAC}^2 + \mu_{CH}^2 + \mu_{ADCA}^2} \tag{3.8}$$

$$\mu_{OB} = \sqrt{\mu_{DAC}^2 + \mu_{CH}^2 + \mu_{ADCB}^2} \tag{3.9}$$

$$\mu_{OAB} = \sqrt{\mu_{ADCA}^2 + \mu_{ADCB}^2} \tag{3.10}$$

Furthermore, the corresponding standard deviations for the three measurements are

$$\sigma_{OA} = \sqrt{\sigma_{DAC}^2 + \sigma_{CH}^2 + \sigma_{ADCA}^2} \tag{3.11}$$

$$\sigma_{OB} = \sqrt{\sigma_{DAC}^2 + \sigma_{CH}^2 + \sigma_{ADCB}^2} \tag{3.12}$$

$$\sigma_{OAB} = \sqrt{\sigma_{ADCA}^2 + \sigma_{ADCB}^2} \ . \tag{3.13}$$

Assuming that $X_{OA}$, $X_{OB}$ and $X_{OAB}$ are independent random variables, then any linear combination of these variables will yield the same linear combination in their mean values ($\mu_{OA}$, $\mu_{OB}$, and $\mu_{OAB}$). Hence, the bias error introduced by the ADCs may be removed by mapping the three random variables into a forth one as follows:

$$X_O = \sqrt{\frac{X_{OA}^2 + X_{OB}^2 - X_{OAB}^2}{2}} \ . \tag{3.14}$$

The derivation of this expression follows closely the development in [10].

The mean and standard deviation of the newly create random variable, $X_O$, which represents the desired or corrected measured value, are as follows:

$$\mu = \sqrt{\mu_{DAC}^2 + \mu_{CH}^2} \tag{3.15}$$

and

$$\sigma = \sqrt{\frac{\sigma_{DAC}^2 + \sigma_{CH}^2 + \sigma_{ADCA}^2 + \sigma_{ADCB}^2}{2}} \tag{3.16}$$

which reduces to

$$\sigma \approx \sqrt{\frac{\sigma_{DAC}^2 + \sigma_{CH}^2}{2} + \sigma_{ADCA}^2} \tag{3.17}$$

as $\sigma_{ADCA}^2 \approx \sigma_{ADCB}^2$.

From Equation (3.16), it is apparent that the mean value of the ADCs has been removed from the mean value of the measurement variable $X_O$. The same, unfortunately, cannot be said for its standard deviation as is evident from Equation (3.17). Here the noise of the ADC continues to plays a significant role.

It is interesting to note that by interchanging the roles of $X_{OA}$ and $X_{OAB}$ in Equation (3.14) we obtain a new random variable, i.e.,

$$X_O = \sqrt{\frac{X_{OA}^2 + X_{OAB}^2 - X_{OB}^2}{2}}, \tag{3.18}$$

which has mean value

$$\mu = \mu_{ADCA}, \tag{3.19}$$

and a standard deviation given by Equation (3.17). Similarly, the mean value of ADC B may be determined by reversing the roles of $X_{OA}$ and $X_{OAB}$ in Equation (3.14) and repeating the analysis.

The method of simultaneous-sampling has been shown to be capable of isolating various noise sources in a DSP-based test system with no bias error.

## *3.4 - An Optimum ADC Measurement Arrangement*

A optimum digitizer architecture, such as that shown in Figure 3.4, could be employed so that multiple simultaneously-sampling dual-ADCs could be arranged to capture data in a time-interleaved manner. If K-pairs of simultaneously-sampling dual-ADCs are interleaved, then the mean value of measurement will be the same as that described by Equation (3.15), however the standard deviation would become

$$\sigma \approx \frac{1}{\sqrt{K}}\sqrt{\frac{\sigma_{DAC}^2 + \sigma_{CH}^2}{2} + \sigma_{ADCA}^2}\,. \tag{3.20}$$

Hence, the variance will decrease by a factor of K and the bias error will be eliminated.

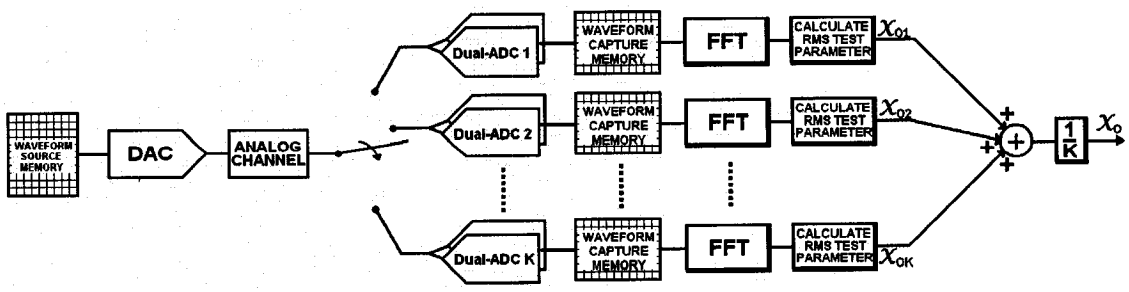



**Figure 3.4: Optimized Digitizer Architecture to Remove Bias Errors while Improving Repeatability of a Measurement**

## *3.5 - MATLAB Simulations*

MATLAB was used to simulate the three architectures proposed in Section 3.3: interleaved, simultaneous, and optimized ADC designs. Each design was simulated separately. The simulation setup and the results are presented in following sections.

### 3.5.1. Simultaneously-Sampling Dual-ADC Simulation

The simultaneously-sampled dual-ADC design was simulated with the MATLAB Simulink model shown in Figure 3.5. The noisy AWG was created by generating a sinusoid with programmed coherency added to a normally distributed random number. Each noisy digitizer was modeled by summing the input signal with a normal distributed random number. This noisy signal was quantized and recorded in memory. The post-processing illustrated in Figure 3.3 was performed in software.

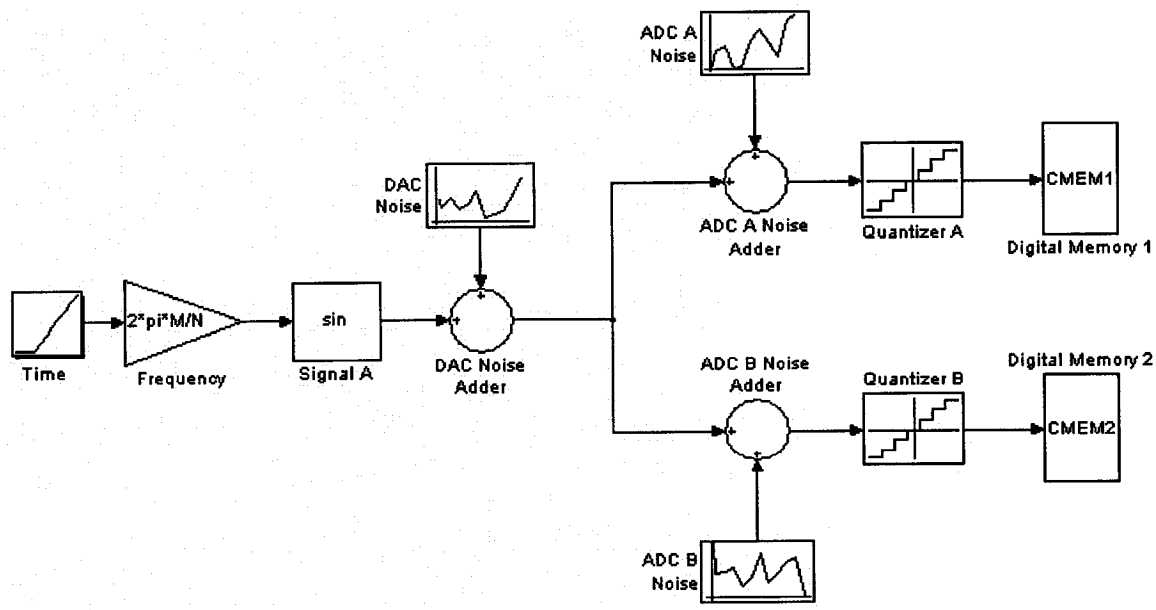
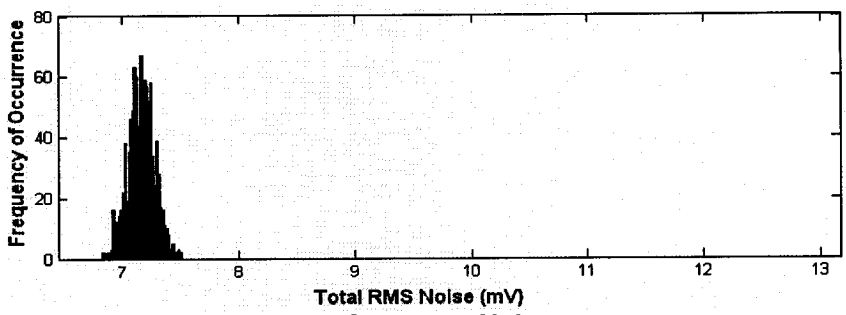



**Figure 3.5: MATLAB Simulink Model for the Simultaneously-Sampling Dual-ADC Simulation**

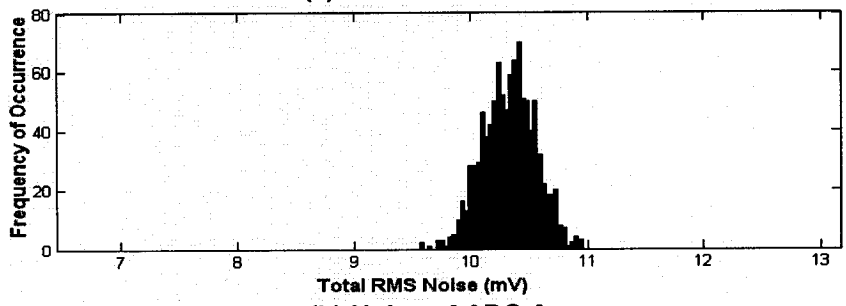
One simulation is presented to demonstrate all aspects of the functionality, as described in Section 3.3. Figure 3.6 reveals the simulation results when total RMS noise was the extracted test parameter. One thousand repeated measurement were taken and the numerical results of the mean and standard deviation are summarized in Table 3.1. The total RMS DAC and ADC noises are shown in Figure 3.6(a) and (b), respectively. These results were extracted independently to be used as a comparison. Figure 3.6(c) shows the output of one ADC when both noise sources are combined. After applying the processing methodology described in Section 3.3, the distribution of the ADC noise and DAC noise were derived. It may be seen from their results of Figures 3.6(d) and (e) that the bias from both DAC and ADC has been successfully removed.

**Table 3.1: Numerical Results from Simulation of Figure 3.6**

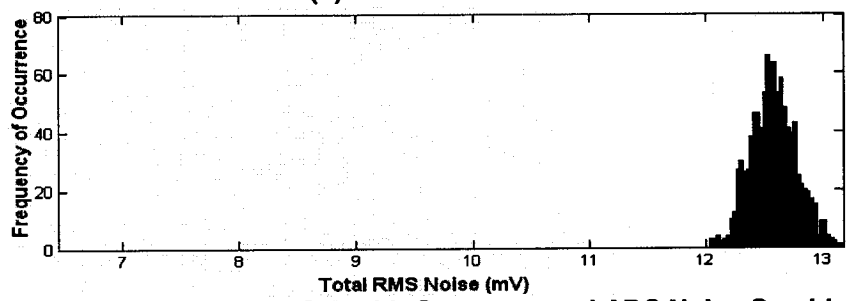
| | Ideal DAC Noise | Ideal ADC Noise | DAC - ADC Output | Corrected DAC Value | Corrected ADC Value |
|---|---|---|---|---|---|
| **Mean** | 7.2 mV | 10.3 mV | 12.6 mV | 7.2 mV | 10.3 mV |
| **Std. Dev.** | 113 μV | 226 μV | 195 μV | 261 μV | 158 μV |



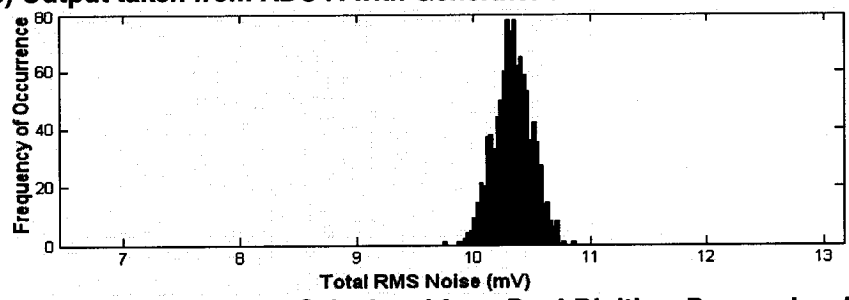

(a) Generator Noise



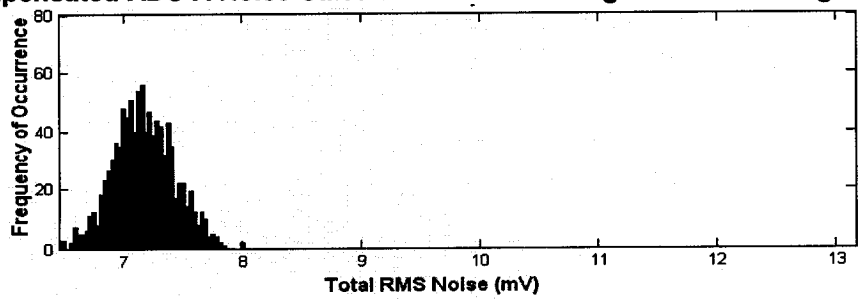

(b) Noise of ADC A




(c) Output taken from ADC A with Generator and ADC Noise Combined




(d) Compensated ADC A Noise Calculated from Dual-Digitizer Processing Algorithm




(e) Compensated Generator Noise Calculated from Dual-Digitizer Processing Algorithm

**Figure 3.6: Simulation Results for a Simultaneously-Sampling Dual-ADC Design Demonstrating The Bias Removal Technique**

### 3.5.2. Interleaved ADC Simulation

The simulation for the interleaved architecture used five ADCs sourced by the same DAC and each contributing an independent normally distributed noise source. The MATLAB Simulink model for this example is given in Figure 3.7.

The data was captured in an interleaved fashion whereby every alternate fifth point was transferred to each ADC via the demultiplexer. Figure 3.8 summarizes the results from this simulation. The DAC output, used as a comparison, is shown in part (a) of the figure. The output of one ADC is illustrated in Figure 3.8(b). Figure 3.8(c) demonstrates the effect of the average five ADC results.

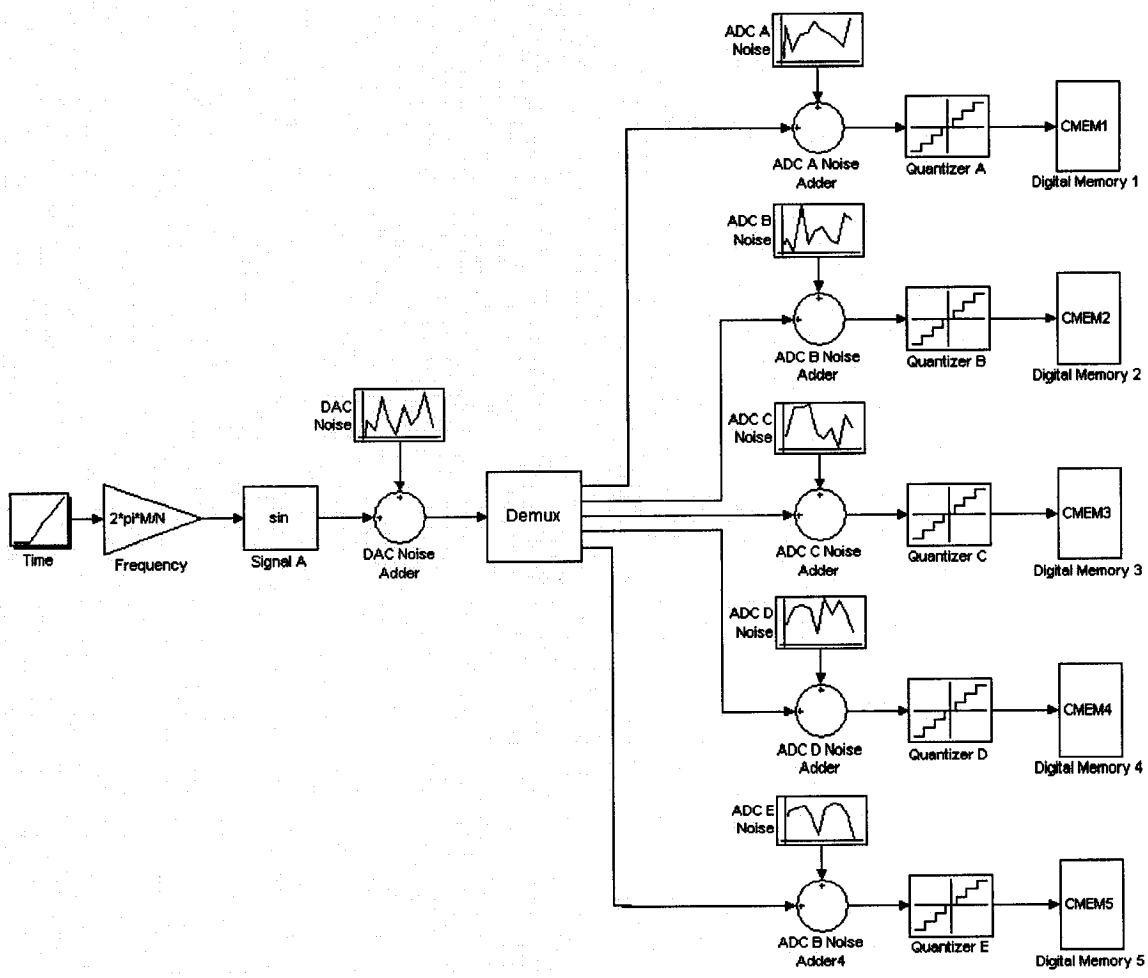
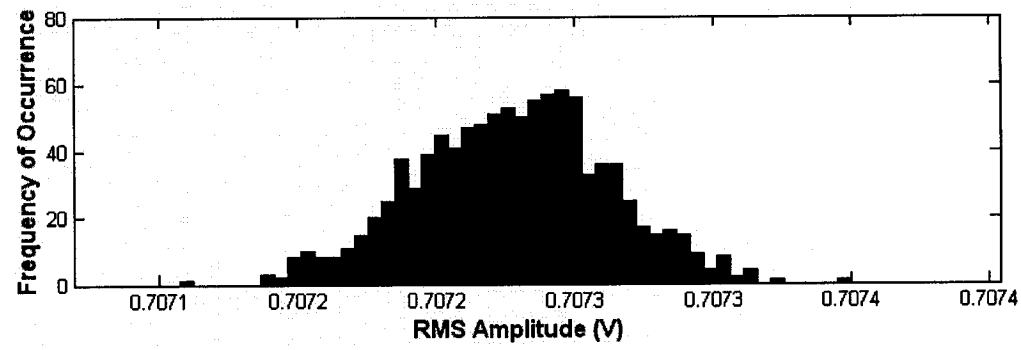



**Figure 3.7: MATLAB Simulink Model for the Interleaved Sampling 5-ADC Simulation**

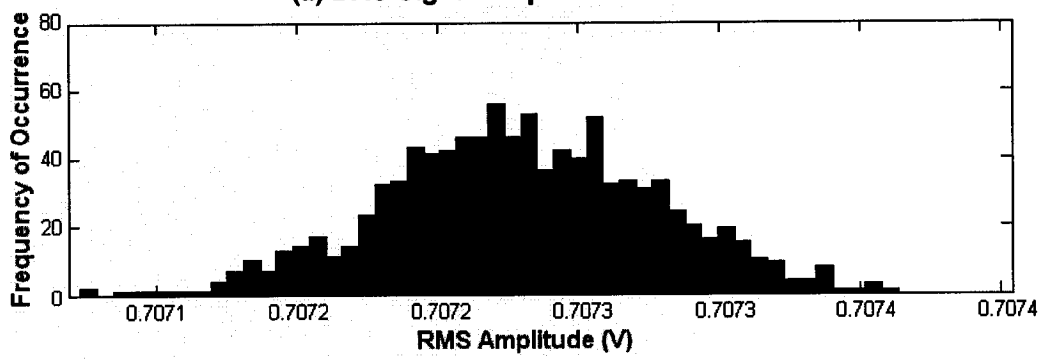
The numerical results from these simulations are summarized in Table 3.2. From this simulation we may conclude that the standard deviation improved by a factor of $\sqrt{5.1}$.

**Table 3.2: Numerical Results from Simulation of Figure 3.8**

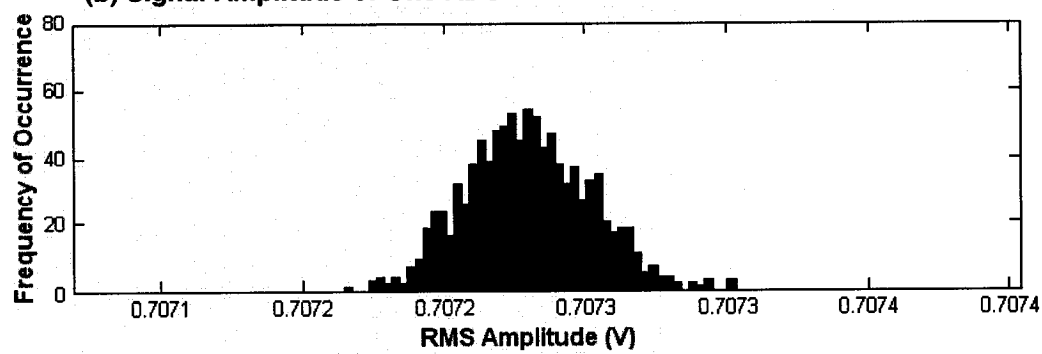
| | Ideal DAC Noise | DAC - ADC Output | Averaged Output of 5 ADCs |
|---|---|---|---|
| **Mean** | 0.70728 V | 0.70728 V | 0.70728 V |
| **Std. Dev.** | 34.5 μV | 49.6 μV | 21.9 μV |




**(a) DAC Signal Amplitude with Noise**




**(b) Signal Amplitude of One ADC with DAC and ADC Noise Combined**




**(c) Average Signal Amplitude of Five Interleaved ADCs**

**Figure 3.8: Simulation Result for a Interleaved 5-ADC Digitizer**

### 3.5.3. Optimized Digitizer Simulation

To demonstrate the effectiveness of the optimized design, six pairs of simultaneously-sampling dual-ADC were implemented to remove the bias error from a total RMS power measurement. The MATLAB Simulink model is shown in Figure 3.9. The results of the optimum ADC design are displayed in Figure 3.10 and the numerical results are summarized in Table 3.3.

From these results it may be concluded that the bias of the generator was certainly removed. Moreover, the standard deviation from using a single dual-digitizer pair was improved by a factor of $\sqrt{5.6}$. The theoretical improvement should be $\sqrt{6}$. Most impressively, the overall standard deviation reduced by a factor of $\sqrt{67.5} = 8.2$!

**Table 3.3: Numerical Results from Simulation of Figure 3.10**

| | Mean | Standard Deviation |
|---|---|---|
| **Ideal DAC Noise** | 7.157 mV | 113 μV |
| **DAC - ADC Output** | 1.122 mV | 859 μV |
| **Corrected DAC from 1 Dual-ADC** | 7.164 mV | 248 μV |
| **Corrected DAC from 2 Dual-ADC** | 7.160 mV | 176 μV |
| **Corrected DAC from 4 Dual-ADC** | 7.155 mV | 127 μV |
| **Corrected DAC from 6 Dual-ADC** | 7.156 mV | 105 μV |

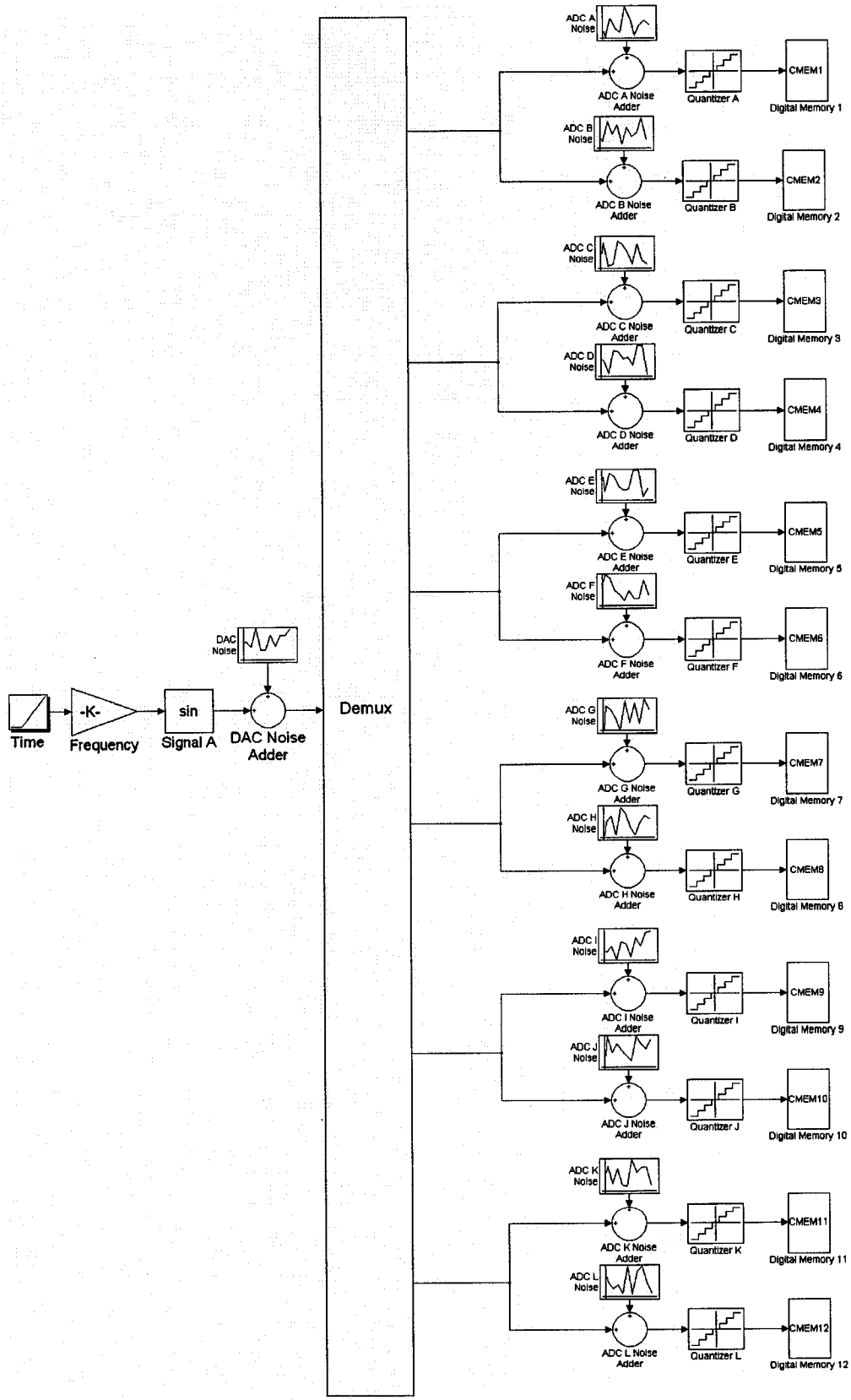
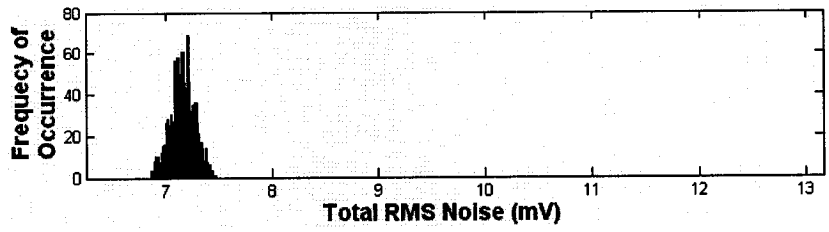
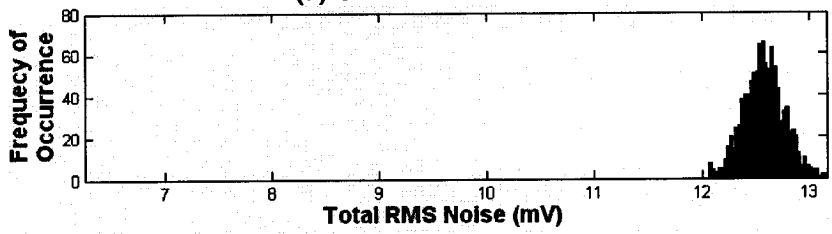


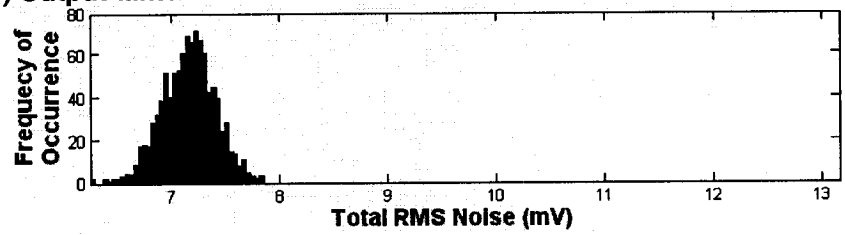

**Figure 3.9: Simulink Model for an Optimized Hex-Interleaved, Dual-Digitizer Design**



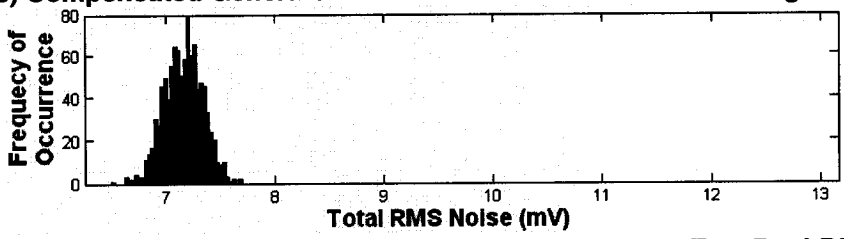

(a) Generator Noise



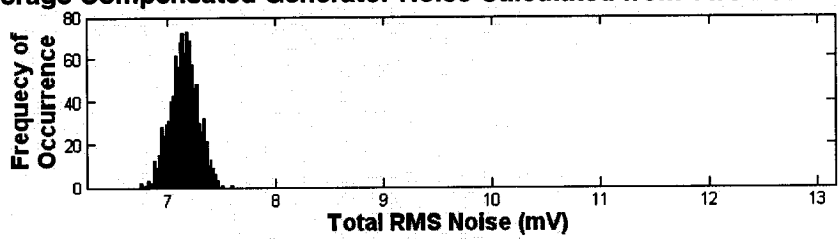

(b) Output taken from ADC A with Generator and ADC Noise Combined



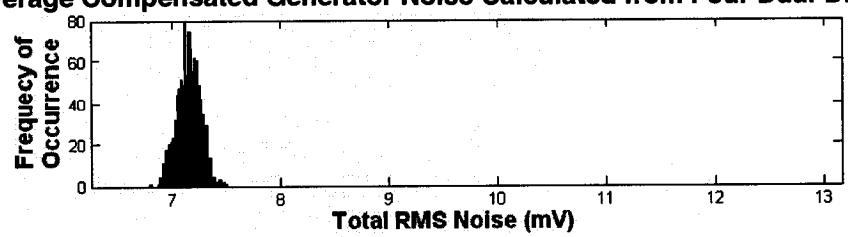

(c) Compensated Generator Noise Calculated from one Dual-Digitizer




(d) Average Compensated Generator Noise Calculated from Two Dual-Digitizer




(e) Average Compensated Generator Noise Calculated from Four Dual-Digitizer




(f) Average Compensated Generator Noise Calculated from Six Dual-Digitizer

**Figure 3.10: Simulation Results for an Optimized Hex-Interleaved Dual-Digitizer Design**

## *3.6 - Other Applications*

The proposed digitizer architecture may be extended to other applications without increasing the complexity of the hardware configuration. Two such applications are time-interleaved ADCs and concurrent ADCs, described in the following two sections.

### 3.6.1. Time-Interleaved Analog-to-Digital Conversion

The sampling frequency of an ADC is limited by circuit constraints and the tradeoffs between resolution and operating speed. Moreover, the input signal bandwidth of an ADC may be restricted by the maximum sampling frequency (i.e. Nyquist principle). Time-interleaved data conversion is an attractive method to increase the sampling frequency of ADCs. Time-interleaved ADC systems implement multiple ADCs each sampled at alternate instants of time. Hence, for every additional time-interleaved ADC the sampling frequency may be increased proportionally. Furthermore, each ADC is clocked at its specified operating speed maintaining the performance characteristics of the individual ADC.

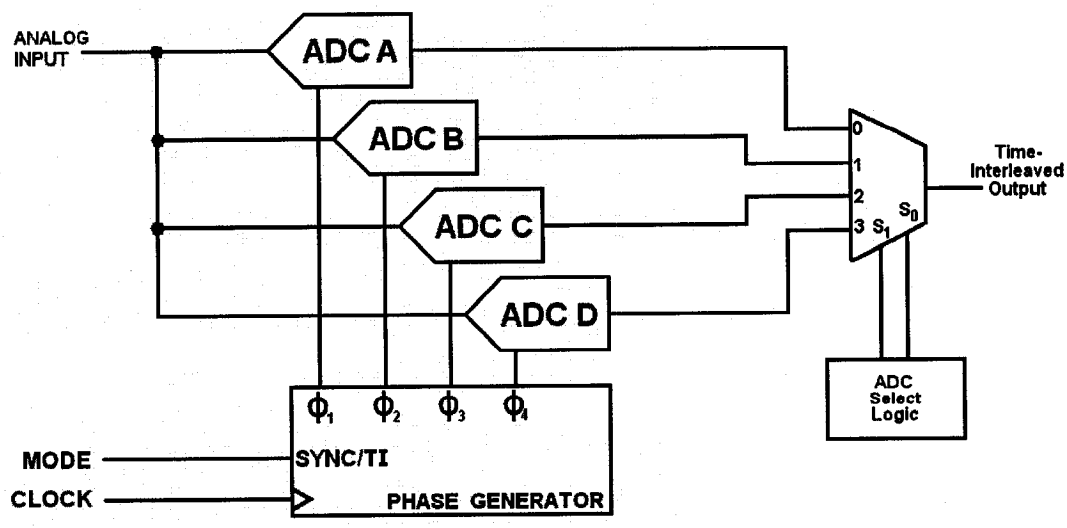



**Figure 3.11: Example of Time-Interleaved Quad-ADC to Increase Throughput**

The disadvantage of the multiple-ADC time-interleaved architecture is the mismatch errors between ADCs. Each ADC will produce different DC offsets, gain errors, and clock skews resulting in an increased noise and possible spurious tones. However, research has demonstrated that these errors can be compensated or corrected for through concurrent or post-processing techniques, as described in [11] and [12]. Other research proposes a randomization sampling technique to reduce spurious tones [13].

The proposed digitizer is already configured to capture data in the time-interleaved method. It would require only a multiplexer to select the proper ADC output for every instant of time. An example of such a system with four time-interleaved ADCs is shown in Figure 3.11.

### 3.6.2. Concurrent Analog-to-Digital Conversion

Another application of the proposed digitizer architecture is in concurrent testing. In other words, the analog inputs of each ADC may be routed to capture different signals. An example of this type of configuration is displayed in Figure 3.12. The clocks could be in phase (i.e. simultaneously-sampling) or out of phase (e.g. time-interleaving). Moreover, the ADC output data may be multiplexed, as in Figure 3.11.

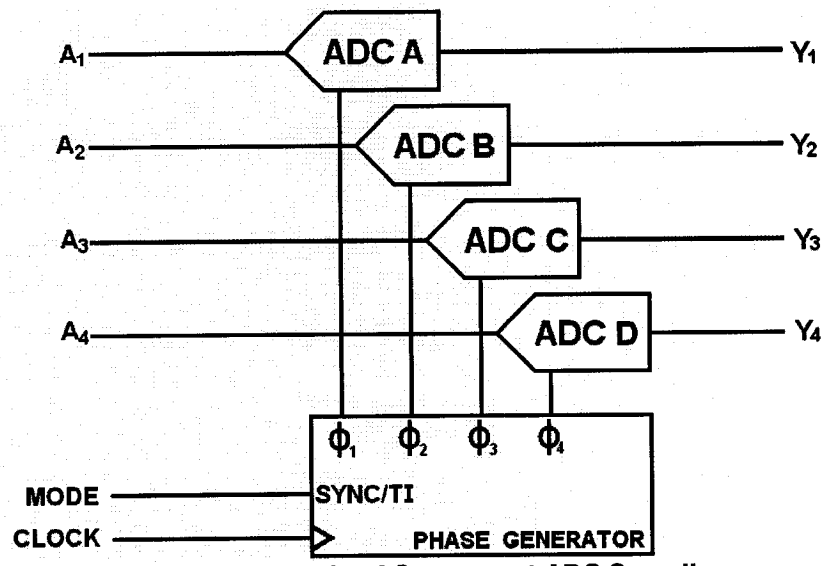



**Figure 3.12: Example of Concurrent ADC Sampling**

## *3.7 - Summary*

A new digitizer architecture was proposed to improve the accuracy and precision of test measurements in a DSP-based test environment. By time-interleaving K ADCs, the measurement variance may be improved by a factor of K. A simultaneously-sampling dual-ADC configuration may be employed to remove any bias error from the measured test parameter. It was also demonstrated that a hybrid optimized configuration may be used to remove any bias error and increase repeatability. Furthermore, the difference between each configuration relies only on the clocking strategy, hence one architecture could be constructed to execute all possible calculations. Most importantly, regardless of the configuration, no extra test time is required to achieve these improvements. MATLAB simulations were used to demonstrate that the statistics and manipulations of the random variables produced the desired results.

# Chapter 4: Improving Sampled-Channel SNR Measurements

## 4.1 - Introduction

Clock jitter effects in a sampled-channel test system severely limit its measurement accuracy. This is especially acute in high-frequency sampling systems. It is most often the case (e.g. production test) that a single measurement of a DUT's performance is taken to dictate its overall behavior. In the presence of system noise, these one-time measurements may not be accurate enough. It was shown in Chapter 3 that the bias error in a noise measurement may be removed using the simultaneously-sampling dual-digitizer approach. This chapter extends the dual-digitizer concept to improve noise measurements by extracting and separating the effects of thermal noise from those induced by clock jitter.

The noise properties of a sampled-channel test system can be modeled as shown in Figure 4.1. The input and output signals of the DAC-ADC combination are denoted $v_{IN}(t)$ and $v_O(t)$, respectively. The gains of the DAC and ADC are denoted $G_G$ and $G_A$, respectively. In addition, the DAC and ADC will contribute both thermal noise ($n_G(t)$ and $n_A(t)$) and jitter-induced noise ($j_G(t)$ and $j_A(t)$).

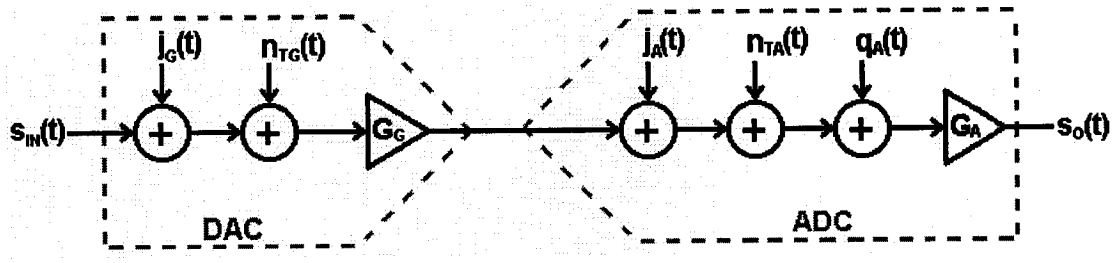



**Figure 4.1: Sample-Channel Noise Model**

The ADC also introduces a quantization noise component, denoted $q_A(t)$ as shown in Figure 4.1. The power spectral density (PSD) of the output signal may be written in terms of the PSD of the various inputs as follows

$$S_O(\omega) = |G_A(\omega)|^2 \left(S_{JA}(\omega) + S_{NA}(\omega) + S_{QA}(\omega)\right) + |G_G(\omega)G_A(\omega)|^2 \left(S_{JG}(\omega) + S_{NG}(\omega) + S_{IN}(\omega)\right). \quad \textbf{(4.1)}$$

The average power of the test system output for a single measurement, denoted by $p_x$, is

$$p_O = p_{IN} + p_{JA} + p_{NA} + p_{QA} + p_{JG} + p_{NG}, \quad \textbf{(4.2)}$$

where the individual terms are derived from the following:

$$p_{QA} \approx \frac{V_{LSB}^2}{12}, \quad \textbf{(4.3)}$$

$$p_{IN} = \frac{1}{2\pi}\int_0^{F_S} |G_A(\omega)G_G(\omega)|^2 S_{IN}(\omega)d\omega, \quad \textbf{(4.4)}$$

$$p_{JA} = \frac{1}{2\pi}\int_0^{F_S} |G_A(\omega)|^2 S_{JA}(\omega)d\omega. \quad \textbf{(4.5)}$$

The remaining terms have a form very similar to Equations (4.4) or (4.5) and are left for the reader to derive. If repeated measurements are taken, then $p_x$ will converge onto the mean value $\mu_x$, as described in Chapter 3.

In the case of a sinusoidal excitation, the signal-to-noise ratio (SNR) of the test system output is the ratio of the signal bin power to the sum of all the non-harmonically related bin powers obtained from the PSD and is represented by

$$SNR = \frac{p_{IN}}{p_{JA} + p_{NA} + p_{QA} + p_{JG} + p_{NG}}. \quad \textbf{(4.6)}$$

Here we see that the measurement includes the noise from the DAC and the ADC, as well as two jitter-induced noise components.

When the DUT is a DAC, the SNR should only include the thermal-induced noise of the DAC, i.e.

$$SNR_{DAC} = \frac{p_{IN}}{p_{NG}}. \quad \textbf{(4.7)}$$

Conversely, when the DUT is an ADC, the SNR metric should be based on the following,

$$SNR_{ADC} = \frac{p_{IN}}{p_{NA} + p_{QA}}. \quad \textbf{(4.8)}$$

It is therefore the objective of this chapter to present a method that isolates the various noise components from a noise measurement thus enabling a more accurate SNR calculation for a DAC or ADC.

An outline of the chapter is as follows: Section 4.2 introduces the dual-digitizer method that is applied regardless of which device, the DAC or the ADC, is under test. The calculation of the SNR parameters for the DAC will be presented in Section 4.3. Section 4.4 will describe how to extract the SNR metrics when the DUT is an ADC. MATLAB simulation results proving the legitimacy of the proposed technique are revealed in Section 4.5. Finally, the proposed technique is summarized in Section 4.6.

## 4.2 - The Dual-Digitizer Noise Model

A noise model that includes the normalization and subtraction operation of the ADC outputs is shown in Figure 4.2. The normalization factors, $K_A=G_A(\omega_{IN})G_G(\omega_{IN})$ and $K_B=G_B(\omega_{IN})G_G(\omega_{IN})$, are acquired from the ratio of the output signal amplitude to the input signal amplitude at the input test signal frequency $\omega_{IN}$. Detailed analysis (which accounts for the correlated DAC input) reveals that the PSD of the three outputs are as follows:

$$S_{OA}(\omega)=\left|\frac{G_A(\omega)}{K_A}\right|^2\left(S_{JA}(\omega)+S_{NA}(\omega)+S_{QA}(\omega)\right)+\left|\frac{G_G(\omega)G_A(\omega)}{K_A}\right|^2\left(S_{JG}(\omega)+S_{NG}(\omega)+S_{IN}(\omega)\right), \tag{4.9}$$

$$S_{OB}(\omega)=\left|\frac{G_B(\omega)}{K_B}\right|^2\left(S_{JB}(\omega)+S_{NB}(\omega)+S_{QB}(\omega)\right)+\left|\frac{G_G(\omega)G_B(\omega)}{K_B}\right|^2\left(S_{JG}(\omega)+S_{NG}(\omega)+S_{IN}(\omega)\right), \tag{4.10}$$

and

$$\begin{aligned}S_{OAB}(\omega)=&\left|\frac{G_A(\omega)}{K_A}\right|^2\left(S_{JA}(\omega)+S_{NA}(\omega)+S_{QA}(\omega)\right)+\left|\frac{G_B(\omega)}{K_B}\right|^2\left(S_{JB}(\omega)+S_{NB}(\omega)+S_{QB}(\omega)\right)\\&+\left|\left(\frac{G_A(\omega)}{K_A}-\frac{G_B(\omega)}{K_B}\right)\cdot G_G(\omega)\right|^2\left(S_{JG}(\omega)+S_{NG}(\omega)+S_{IN}(\omega)\right).\end{aligned} \tag{4.11}$$

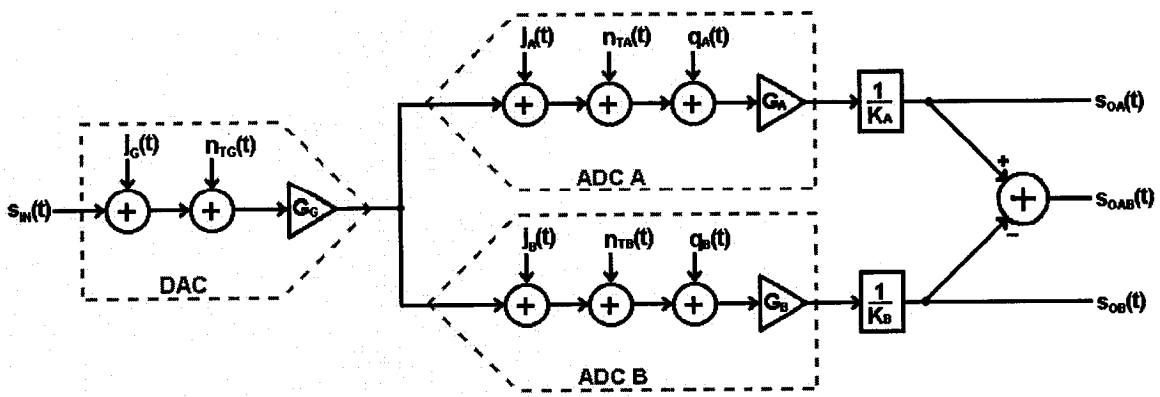



**Figure 4.2: Noise Model of the Simplified Double-ADC Method**

Experience shows that a large mismatch in frequency response results in a small error in SNR measurement. Therefore, for all practical applications we may assume that the ADC gains are frequency independent.

Using the same average power notation as in Equations (4.3)-(4.5), we may obtain the average noise power of the output $S_{OA}(\omega)$ as:

$$p_{OA} = \frac{p_{JA} + p_{NA} + p_{QA} + p_{JG} + p_{NG} + p_{IN}}{K_A^2}. \tag{4.12}$$

Since our normalization factors are related by $G_A/K_A = G_B/K_B$, the average power of the outputs $S_{OB}(\omega)$ and $S_{OAB}(\omega)$ may be derived as:

$$p_{OB} = \frac{p_{JB} + p_{NB} + p_{QB} + p_{JG} + p_{NG} + p_{IN}}{K_A^2}, \tag{4.13}$$

and

$$p_{OAB} = \frac{p_{JA} + p_{NA} + p_{QA}}{K_A^2} + \frac{p_{JB} + p_{NB} + p_{QB}}{K_A^2}. \tag{4.14}$$

Equations (4.12)-(4.14) may be considered as a system of three simultaneous equations in three unknowns, $p_{JA}+p_{NA}+p_{QA}$, $p_{JB}+p_{NB}+p_{QB}$ and $p_{JG}+p_{NG}$, from which the following may be obtain:

$$p_{JA} + p_{NA} + p_{QA} = K_A^2 \frac{p_{OA} + p_{OAB} - p_{OB}}{2}, \tag{4.15}$$

and

$$p_{JG} + p_{NG} = K_A^2 \frac{p_{OA} + p_{OB} - p_{OAB}}{2}. \quad (4.16)$$

We have obtained separate measures for the average noise powers of the ADC and the DAC given in expressions (4.15) and (4.16), respectively. Equations (4.15) and (4.16) are similar to Equations (3.14) and (3.18) derived for repeated measurements. The jitter induced noise components ($p_{JA}$ and $p_{JG}$) in Equations (4.15) and (4.16) may also be separated. When the DUT is a DAC, the process is outlined in Section 4.3. The process is illustrated for the ADC case in Section 4.4.

## *4.3 - The DAC is Under Test*

The test environment shown in Figure 4.3 is implemented when the DAC is the DUT. The noise generated by the test equipment (i.e. the ADCs) has been successfully removed from the DAC SNR calculation when the ratio of output signal bin power to (4.16) is applied,

$$SNR_{DAC} = \frac{p_{IN}}{p_{JG} + p_{NG}}. \quad (4.17)$$

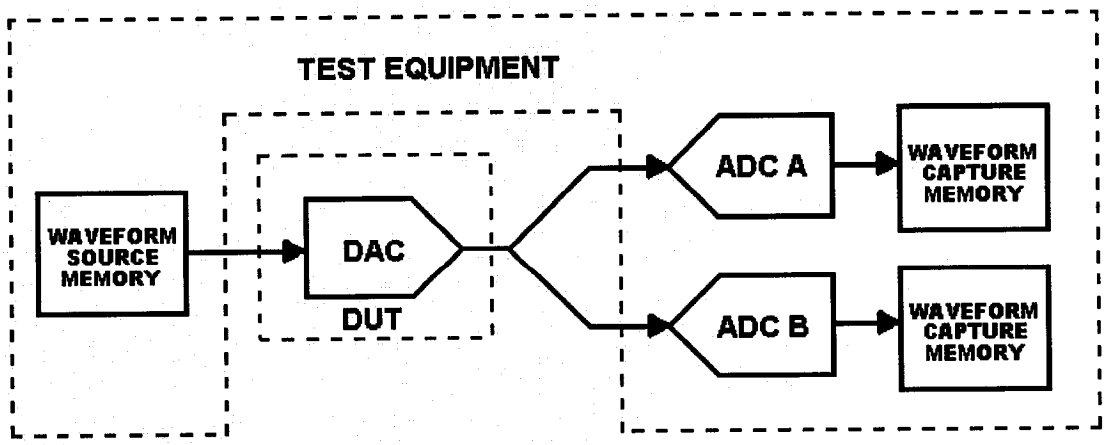



**Figure 4.3: Test Scenario when the DAC is the Device Under Test**

We can remove the jitter-induced noise power ($p_{JG}$) from the SNR measure of Equation (4.17) by exploiting its frequency dependency. The average power of jitter-induced noise of a DAC may be approximated [7] by

$$p_{JG} \approx \tfrac{1}{2} A_o^2 \omega_o^2 J_{RMS} T_S, \tag{4.18}$$

where $A_O$ is the test signal amplitude, $\omega_o$ is the test signal frequency, $T_S$ is the DAC's sampling period and $J_{RMS}$ is the RMS jitter in seconds. Thermal noise is assumed to be white and is not dependent on the input test frequency.

The procedure requires that the dual-digitizer method is run twice at two different input test signal frequencies, say $\omega_1$ and $\omega_2$. The DAC average noise power from each test, denoted $N_{G1}$ and $N_{G2}$, are obtain from Equation (4.16) as follows:

$$N_{G1} = p_{JG1} + p_{NG} \tag{4.19}$$

and

$$N_{G2} = p_{JG2} + p_{NG}. \tag{4.20}$$

The average jitter-induced noise power from the first test period ($p_{JG1}$) may be expressed in terms of the other ($p_{JG2}$) by using Equation (4.18) as shown by the relationship

$$p_{JG1} = \frac{\omega_1^2}{\omega_2^2} p_{JG2}. \tag{4.21}$$

The system of equations formed by Equations (4.19), (4.20) and (4.21) contain three unknowns: $p_{JG1}$, $p_{JG2}$, and $p_{NG}$. Solving for the average thermal noise power component yields

$$p_{NG} = \frac{(N_{G1}) - \frac{\omega_1^2}{\omega_2^2}(N_{G2})}{1 - \frac{\omega_1^2}{\omega_2^2}}. \tag{4.22}$$

Hence, the SNR of the DAC under test without jitter-induced noise is obtained by dividing the input signal power by Equation (4.22) as follows,

$$SNR_{DAC} = \frac{p_{IN}}{p_{NG}} = \frac{p_{IN}\left(1 - \frac{\omega_1^2}{\omega_2^2}\right)}{(N_{G1}) - \frac{\omega_1^2}{\omega_2^2}(N_{G2})}. \tag{4.23}$$

## *4.4 - The ADC is Under Test*

When the ADC is the DUT there are two test possibilities; either the DUT may be duplicated, or only one DUT is available. The first test scenario is commonly employed for discrete component testing. The latter scenario is more typical for integrated circuit testing. Each scenario will be discussed separately in following two sections.

### 4.4.1. Two DUT Scenario

When the DUT may be duplicated, as shown in Figure 4.4, we have already determined the required parameters for removing test equipment (i.e. DAC) noise from our SNR measurement. The ratio of input signal power to Equation (4.15) yields

$$SNR_{ADC} = \frac{p_{IN}}{p_{JA} + p_{NA} + p_{QA}}. \tag{4.24}$$

Under many testing situations the jitter induced noise power ($p_{JA}$) may not be desirable in the SNR measurement of Equation (4.24). By running the dual-digitizer test twice at two different test signal frequencies ($\omega_1$ and $\omega_2$), we may obtain an SNR quantity without jitter-induced error.

The average jitter-induced noise power in an ADC may be approximated [7] as

$$p_{JA} \approx \tfrac{1}{2} A_o^2 \omega_o^2 J_{RMS}^2, \tag{4.25}$$

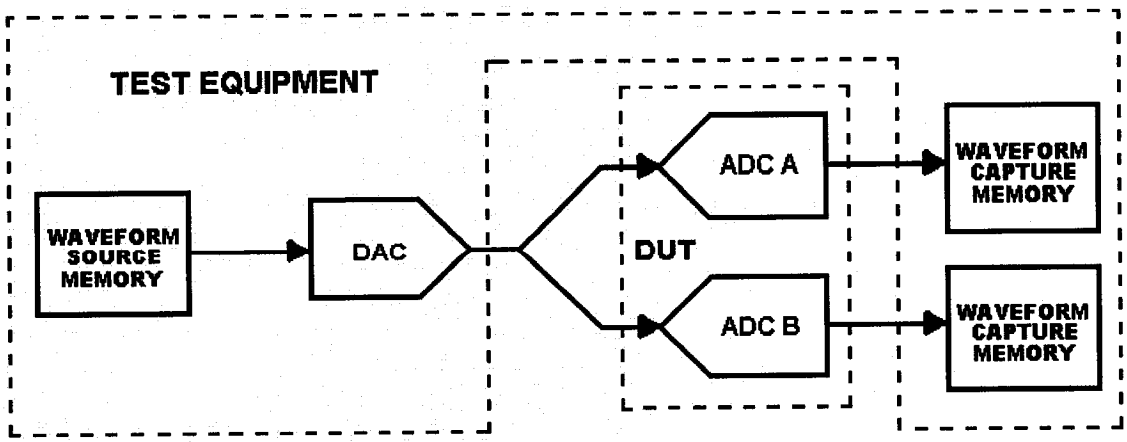



**Figure 4.4: Test Scenario when the ADC Under Test May Be Duplicated**

where $\omega_o$ is the ADC input test signal frequency, $A_O$ is the ADC test signal amplitude and $J_{RMS}$ is the RMS jitter from the sampling clock. Similar to the case described in Section 4.3, the average noise powers of ADC A are

$$N_{A1} = p_{JA1} + p_{NA} + p_{QA} \tag{4.26}$$

and

$$N_{A2} = p_{JA2} + p_{NA} + p_{QA}, \tag{4.27}$$

where $N_{G1}$ and $N_{G2}$ are obtain from Equation (4.15) while running the dual-digitizer test twice using two different frequencies.

A relationship between the frequency dependent jitter-induced noise components ($p_{JA1}$ and $p_{JA2}$) may be acquired from Equation (4.25) given by

$$p_{JA1} = \frac{\omega_1^2}{\omega_2^2} p_{JA2}. \tag{4.28}$$

Using Equations (4.26)-(4.28) we may determine the average noise power of the thermal and quantization noise to be

$$p_{NA} + p_{QA} = \frac{(N_{A1}) - \frac{\omega_1^2}{\omega_2^2}(N_{A2})}{1 - \frac{\omega_1^2}{\omega_2^2}}. \tag{4.29}$$

Hence, the SNR of the ADC without the influence of jitter-induced noise is calculated by dividing the input test signal average power by Equation (4.29) producing

$$SNR_{ADC} = \frac{p_{IN}}{p_{NA} + p_{QA}} = \frac{p_{IN}\left(1 - \frac{\omega_1^2}{\omega_2^2}\right)}{(N_{A1}) - \frac{\omega_1^2}{\omega_2^2}(N_{A2})}. \quad (4.30)$$

### 4.4.2. One DUT Scenario

In the case where there can only be one ADC under test, it is required to implement two identically designed ADC test structures, as illustrated in Figure 4.5. The dual-digitizer test is performed on the test equipment and the SNR of the DAC results in Equation (4.17).

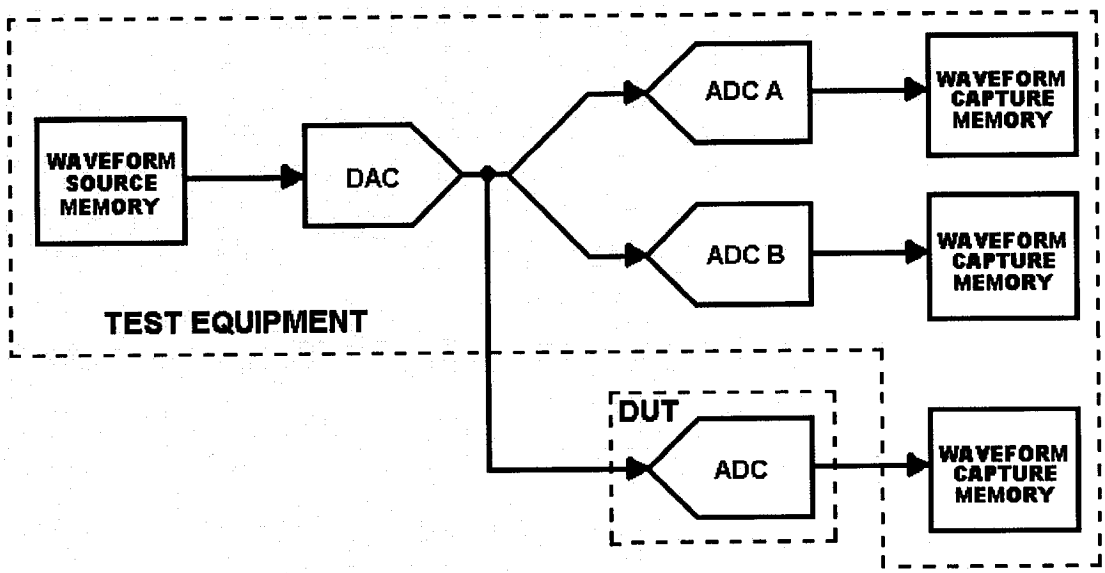



**Figure 4.5: Test Scenario when the ADC Under Test Cannot Be Duplicated**

The DUT is then exercised by the same test signal and the SNR of the DUT output, $SNR_{OUT}$, incorporating the DAC and ADC noise is calculated. Using these two measurements, the SNR of the ADC under test, $SNR_{DUT}$, may be obtained as follows,

$$SNR_{DUT} = \frac{p_{IN}}{p_{JDUT} + p_{NDUT} + p_{QDUT}} = \frac{SNR_{DAC} \cdot SNR_{OUT}}{SNR_{DAC} - SNR_{OUT}}, \tag{4.31}$$

where $p_{IN}$ is redefined to be the average power of the input signal obtained from the DUT output.

The jitter-induced noise component may be removed from Equation (4.31) by running the dual-digitizer test twice using two distinct test signal frequencies, $\omega_1$ and $\omega_2$. From each test the SNR metric of the DAC, Equation (4.17), is obtained. The DUT is stimulated with the same two test signals and the SNR of the DUT is obtained from Equation (4.31), denoted $SNR_{ADC1}$ and $SNR_{ADC2}$.

Using the property from equation (4.28), we may solve for the SNR of the ADC without jitter-induced noise given by

$$SNR_{DUT} = \frac{p_{IN}}{p_{NDUT} + p_{QDUT}} = \frac{SNR_{ADC1} \cdot SNR_{ADC2}\left(1 - \frac{\omega_2^2}{\omega_1^2}\right)}{SNR_{ADC1} - \frac{\omega_2^2}{\omega_1^2} SNR_{ADC2}}. \tag{4.32}$$

## *4.5 - Jitter Removal Simulations*

A MATLAB simulation was performed using the MATLAB Simulink model shown in Figure 4.6. The DAC signal output with jitter was fabricated by adding a normally distributed random number to a time variable, multiplying it by a radial frequency and then taking the sine, illustrated in Figure 4.6. A 20% gain error between the ADC paths was applied. Each ADC was designed to have a 10-bit resolution. Table 4.1 presents the simulation parameters including signal and RMS noise source amplitudes.

Table 4.2 provides the SNR measurements of the DAC and ADC. The first column shows the actual SNR values for each device. The second column presents the results of the proposed method of compensation. For comparison, the last column presents the SNR metrics that would be obtained from the test system without compensation.

**Table 4.1: MATLAB Simulation Parameters**

| Parameter | Value |
|---|---|
| N | 1024 |
| M | 133 |
| Fs | 200 MHz |
| $G_A$ | 1.02 V/V |
| $G_B$ | 0.98 V/V |
| RMS Jitter | 200 ps |
| Signal Amplitude | 1 V |
| $n_{TQ}$ (RMS) | 0.79 mV |
| $n_{TG}$ (RMS) | 2.03 mV |
| $j_G$ (RMS) | 4.40 mV |
| $j_A$ (RMS) | 0.21 mV |

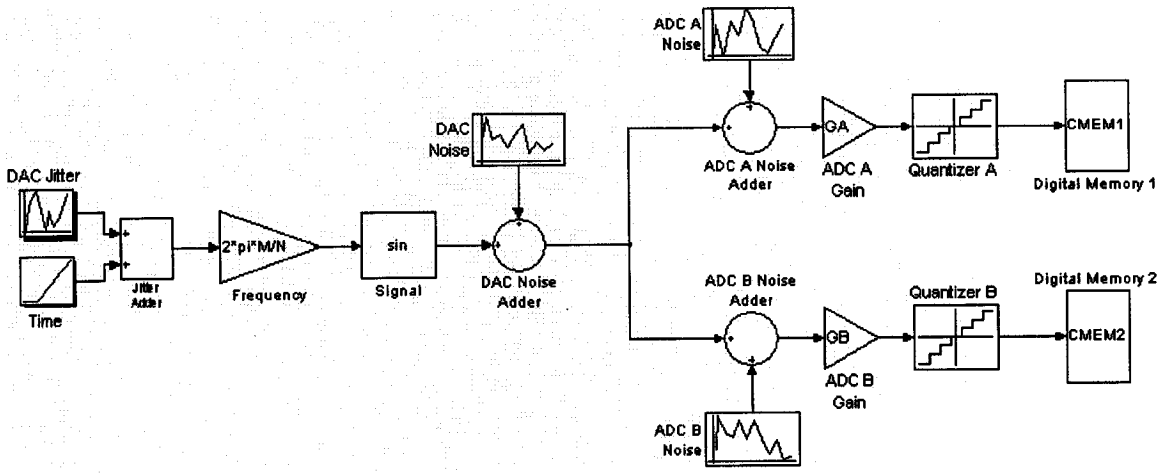



**Figure 4.6: MATLAB Simulink Model Incorporating DAC Jitter**

It is obvious from the results presented in Table 4.2, that the SNR measurement of a DUT would be masked by the test equipment noise, without the proposed compensation method.

A second simulation was performed at a different frequency in order to remove the jitter-induced noise from out SNR measurements. Table 4.3 presents the simulation results.

The comparison of the DAC results between Tables 4.2 and 4.3 show that the clock jitter contributes to 8 dB of performance degradation. Furthermore, this noise does not dictate the performance of the DAC itself.

**Table 4.2: MATLAB Simulation Results**

| | Actual SNR | Proposed Method SNR | DAC-ADC Path SNR |
|---|---|---|---|
| **DAC** | 43.2dB | 43.2dB | 41.1dB |
| **ADCA** | 57.3dB | 57.4dB | 41.1dB |
| **ADC B** | 57.5dB | 57.4dB | 41.1dB |

**Table 4.3: MATLAB Simulation Results Removing Jitter-Induced Noise**

| | Actual SNR | Proposed Method SNR |
|---|---|---|
| DAC | 51.1 dB | 49.1 dB |
| ADC A | 57.6 dB | 57.7 dB |

## *4.6 - Summary*

This chapter described a methodology that may be implemented in a sampled-channel DSP-based test environment to extract the average random noise powers of individual test devices. Moreover, the amplitude noise (thermal) and the frequency dependant noise (jitter) may be separated. As a result, the SNR of the DUT is a more accurate measure of its performance.

# Chapter 5: Mixed-Signal Test Core Implementation

## *5.1 - Introduction*

The integrated test core [5, 14] is a robust system for stimulating and extracting time and frequency measurements of analog and mixed-signal integrated components. It boasts the capability to source arbitrary analog waveforms and digitize arbitrary periodic test signals implemented within a small silicon area. The test core architecture is constructed mainly of digital components with the exception of reconstruction filters and a comparator. The digitization technique employed is called the multipass method [15]. In terms of hardware, this method of digitization requires a programmable DC reference source and a comparator.

The multi-digitizer solution to improve measurement uncertainty which was present in Chapter 3 will be demonstrated by the mixed-signal test core approach. Hence, multipass simultaneously-sampling and time-interleaved test cores were designed. These circuits were fabricated in TSMC's 0.18 μm CMOS process.

An outline of this chapter is as follows: The mixed-signal test core and multipass method of digitization are introduced in Section 5.2. The main

component utilized in the multi-digitizer test core architectures is the comparator. Therefore, the implementation and HSPICE simulation results of the comparator will be thoroughly documented in Section 5.3. The simultaneously-sampling dual-digitizer design is presented in Section 5.4. Finally, the implementation of the time-interleaved quintuple-digitizer circuit is presented in Section 5.5.

## *5.2 - The Mixed-Signal Test Core and Multipass Method of Digitization*

### 5.2.1. The Multipass Method

The multipass analog-to-digital conversion method operates on the premise that a periodic waveform of a known frequency is to be digitized. The frequency of the input signal is set by the coherency principle such that $F_T = MF_S/N$, where $F_T$ is the input waveform frequency, $F_S$ is the sampling frequency, N is the number of samples per input waveform period and M is the number of input waveform periods to be captured within a unit test period (UTP). A UTP is the time it takes to collect N samples of the input waveform (i.e. $UTP = M/F_T = N/F_S$). For coherency, M and N should be relatively prime integers.

The multipass system, illustrated in Figure 5.1, uses a 1-bit quantizer to compare $2^D-1$ DC reference levels to all points on the periodic input waveform, where D is the number of bits that the converter can resolve. For each input waveform pass (or UTP), one reference level is established and compared to all N points of the test signal. The test signal waveform is reconstructed by summing all the digital outputs from each UTP that correspond to the same sampled instant on the waveform.

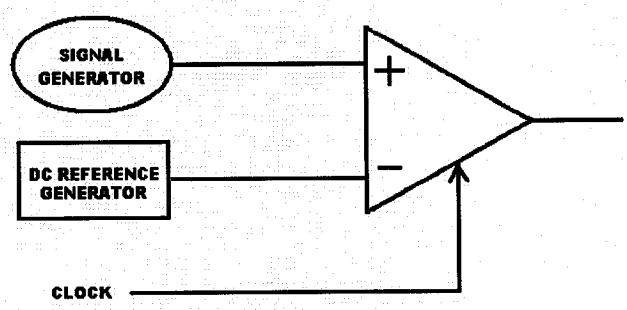



**Figure 5.1: ADC Multipass Conversion Architecture**

For Example, Figure 5.2 illustrates the test signal and DC reference for a complete digitization cycle when D=3, M=1 and N=16. Within each UTP the test signal is sampled 16 times and compared with a single reference level. The digital result from each sample is stored in memory. The output from a complete conversion may be conceptually rearranged, as shown in Figure 5.3, to reveal the test signal waveform. The signal is reconstructed by summing the columns of Figure 5.3, as seen by the sinusoidal overlay. Alternatively, the output could be interpreted as a thermometer code.

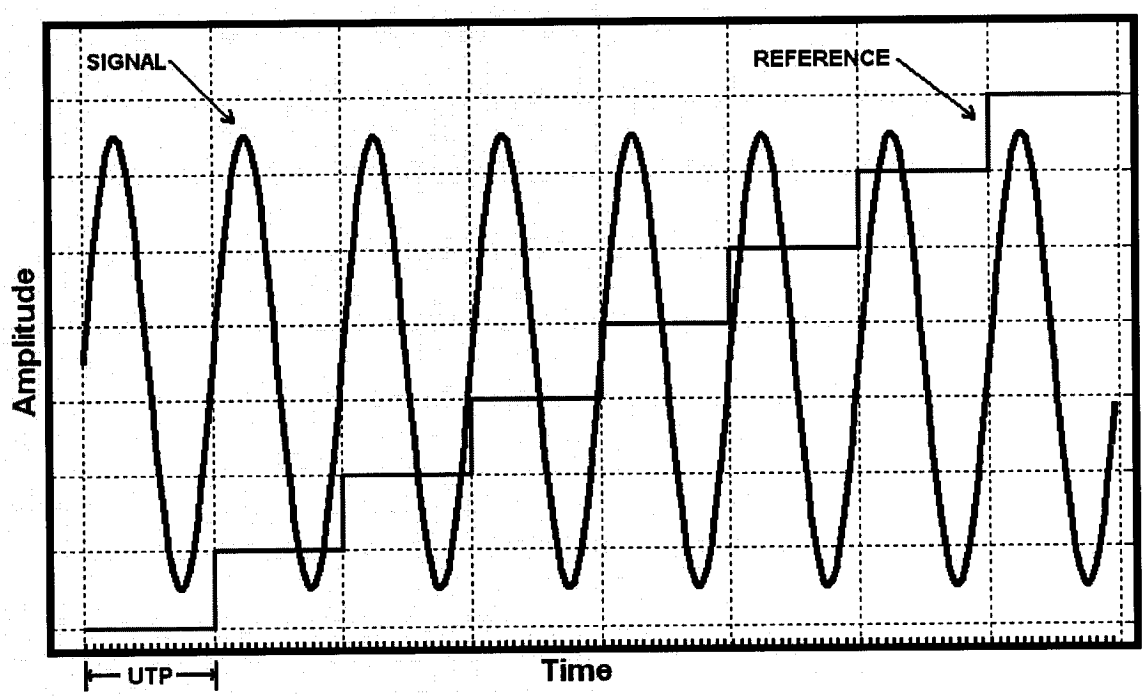



**Figure 5.2: Input Test Signal and Reference for a Complete 3-Bit Multipass Digitization**

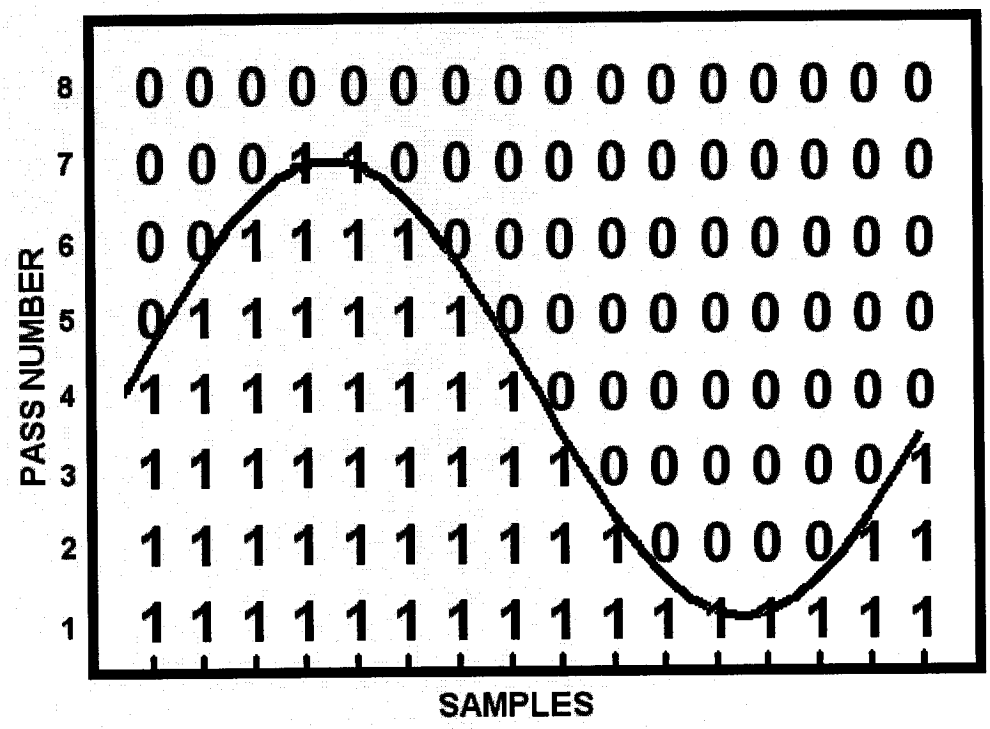



**Figure 5.3: Rearranged Multipass Digital Output**

### 5.2.2. Test Core Architecture

The test core architecture is constructed from several components: an arbitrary waveform generator (AWG), a DC reference generator, a comparator, a clock source, and a DSP engine, as illustrated in Figure 5.4. The AWG is responsible for exciting the device under test (DUT). The purpose of the DC generator is to provide the $2^D$-1 reference levels that the multipass method requires. The comparator is used to compare the DUT output with the DC reference voltage. The clock source is necessary to maintain coherency between the samples taken and the input test signal. Finally, the DSP engine is needed to gather the multipass output bits and reconstruct the waveform signal. Each component will be described briefly.

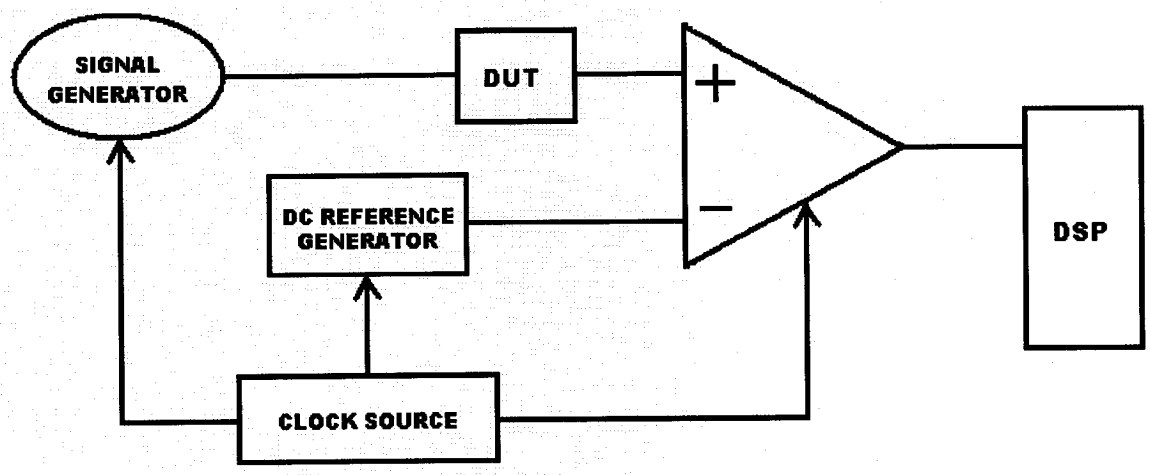



**Figure 5.4: Mixed-Signal Test Core Architecture**

The arbitrary waveform generator is composed of an all-digital implementation [16] whereby a pulse-density modulated (PDM) signal (i.e. sigma-delta modulated signal) is loaded into a shift register, as illustrated in Figure 5.5. At the start of the test the bits of the PDM signal are loaded into the register. Optionally, the test signal may be hard-coded into the set and reset pattern of the registers. Once loading is complete the bits are rotated through the register. The DUT may require that the bit stream be filtered to reduce the shaped quantization noise.

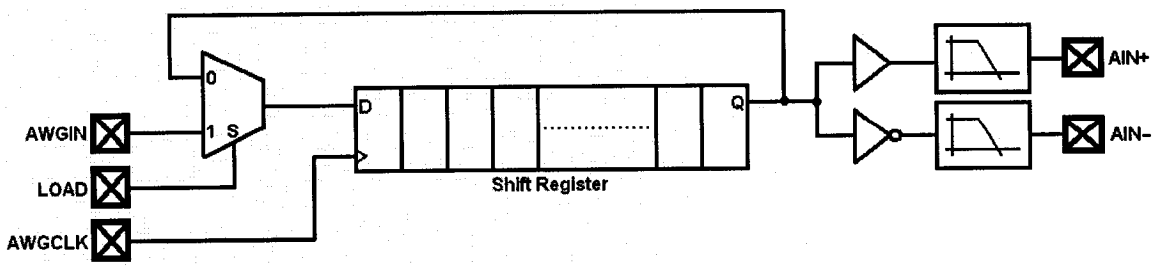



**Figure 5.5: Arbitrary Waveform Generator and DC Generator Topology**

The DC generator uses a similar DSP technique to the AWG signal generation [17]. Using the same register configuration as shown in Figure 5.5, a DC value is encoded, preferably using PDM. The DC value is loaded into the register, and then rotated through the shift register. The DC value must pass through an adequate DC filter. The constraints on the DC filter are based on the permissible AC ripple at the filter output. Generally, the amplitude of the AC ripple must be less than half of an LSB. Aside from the DC filter, the AC ripple is dependent on several factors: the register operating speed, register size, and encoded DC signal type.

The DC signal is best encoded in a higher order single-bit sigma-delta modulation. Simulations have shown that for a finite bit-stream length for a single DC value, there is no predetermined sigma-delta modulation order that gives superior results. Optimal performance is obtained by selecting the best bit-stream from various modulation orders for each individual DC value.

The operating speed of the shift register is equivalently the sampling frequency of the bit-stream. Increasing the sampling frequency has the tendency to push the quantization noise higher into the frequency spectrum. Hence, increasing the operating speed relaxes the requirements on the DC filter.

The resolution of a sigma-delta modulated DC signal is directly dependent on the number of bits capturing the encoding. Furthermore, there is a discontinuity between the first and last bit loaded into the register. Since these bits are rotated through the shift register, this discontinuity will generate unwanted noise. This noise may also be reduced by increasing the bit-stream length.

Further constraints are imposed on the DC filter. The conversion time of digitization process is dependent on the settling time of the DC filter. A UTP

conversion can only be performed once the DC generator has settled to its reference value. Hence, it is desirable to build a quick settling filter.

The test core comparator is required to achieve a significant resolution such that the correct decision can be made from the difference between the DC reference and test signal value. In order to maintain the value and appeal of the integrated solution, this component should be realized with the smallest possible silicon area. Further requirements pertain to sampling frequency. Many DUTs will dictate or constrain the sampling period. Finally, for obvious reasons, the noise from this apparatus should be forced to a strict minimum.

## *5.3 - Comparator Implementation*

It was desired to construct the comparator such that it could resolve 10-bits (i.e. D=10). Furthermore, the comparator was to complete its decision making within 100 ns (i.e. operate at 10 MHz).

The comparator circuit was designed using a combination of circuit components taken from difference publication. There are two principle comparator topologies: cascaded open-loop and the pre-amplifier and latch combination. The cascaded open-loop comparator offers the benefit of high resolution but reacts slowly due to the required timing of the multiple stages. This comparator offers the ability to reduce input referred offset. The pre-amp and latch model contributes high speed but suffers from low resolution. The comparator design herein incorporates both topologies to increase speed and reduce output-referred offset, while maintaining a high-resolution.

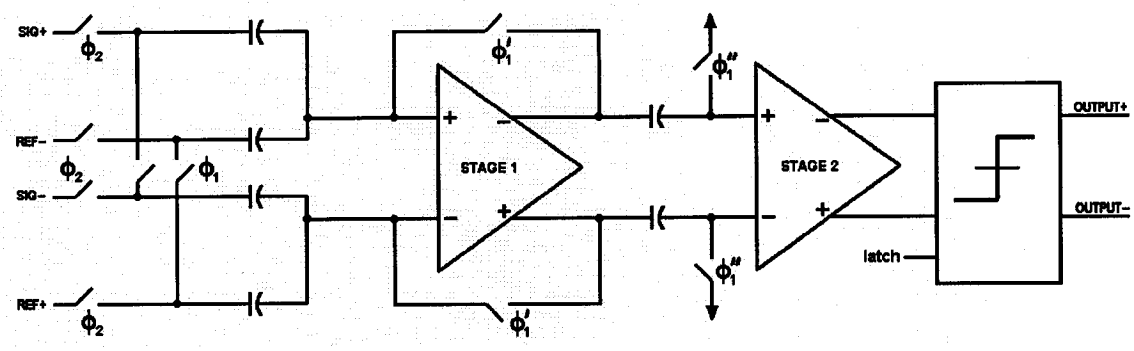



**Figure 5.6: Arbitrary Waveform Generator and DC Generator Topology**

Figure 5.6 illustrates the designed comparator. The first amplifier is a single stage of a cascaded open-loop comparator providing some offset cancellation. The second stage is a classic amplifier and latch combination.

Other components that required design consideration were the switches, sample-and-hold (S/H) input circuitry, capacitors, and clock generation network. The clocking scheme and generation circuit is presented in Section 5.3.1. Section 5.3.2 describes the switch requirements and design. The differential sample-and-hold circuit is described in Section 5.3.3. A brief description and the requirements of the capacitors are presented in Section 5.3.4. Sections 5.3.5 and 5.3.6 describe the first amplifier stage and second amplifier stage with the latch, respectively.

### 5.3.1. The Clock Generation Circuit

The comparator in Figure 5.6 was designed implementing a two-phase non-overlapping clock scheme with same-phase time delayed clocks. A clocking network adapted from [18] was used to generate these clocks and is shown in Figure 5.7. This digital circuit was built from a 0.18 $\mu$m standard cell library provided by Virtual Silicon Technology Incorporated (VSTI). Table 5.1 presents the propagation delays for each of the components in Figure 5.7.

**Table 5.1: VSTI's Standard Cell Propagation Delay on the Rising and Falling Input Signals**

| Cell | Rising (ps) | Falling (ps) |
|---|---|---|
| BUFBD8 | 167 | 160 |
| NOR2D4 | 55 | 28 |
| INVD4 | 28 | 18 |

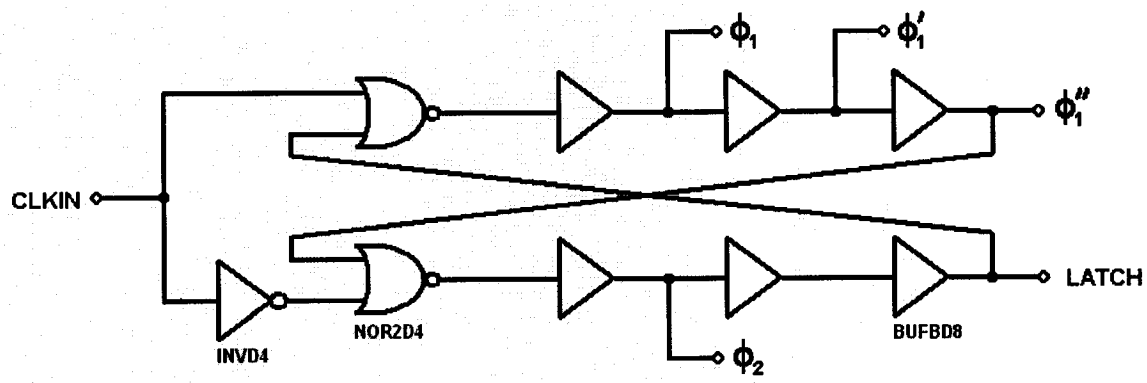



**Figure 5.7: Comparator Clock Generation Circuits**

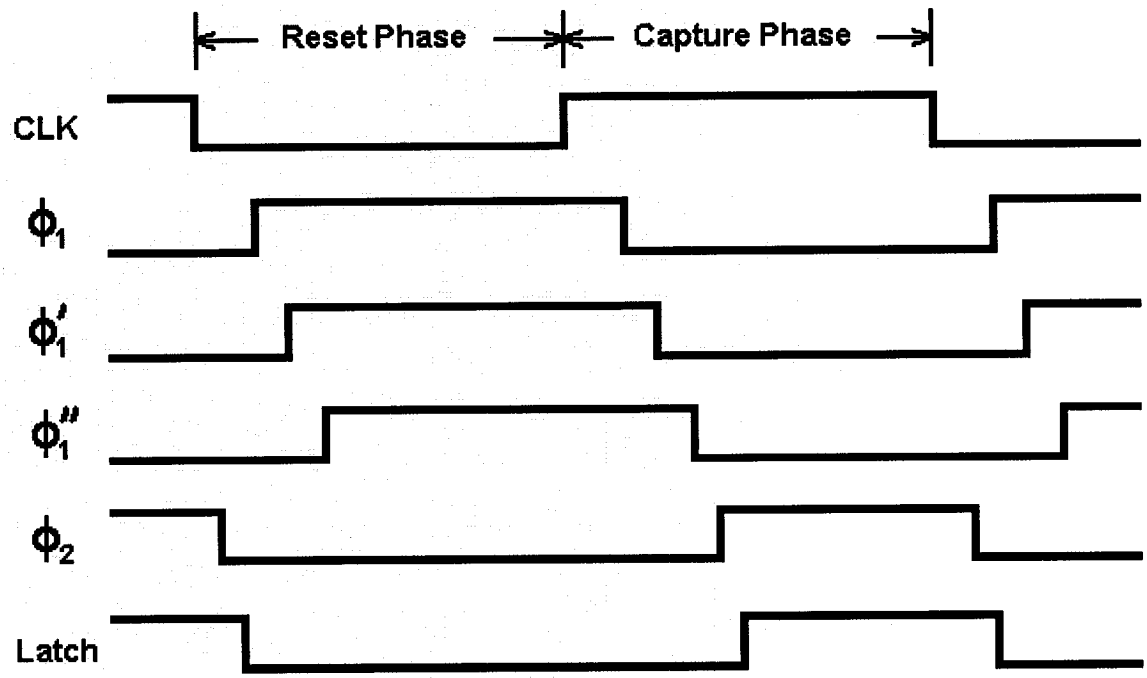



**Figure 5.8: Timing Diagram for the Comparator Clock Generator Circuit**

The timing diagram generated from the clock generation circuit is illustrated in Figure 5.8. During the reset phase the input nodes to the sample and hold circuit is set to analog ground, the first amplifier stage is storing its own offset, the second amplifier stage's inputs are set to analog ground, and the latch is reset. The timing and sequence of events is critical throughout the capture phase. The first action in the capture phase is to open the S/H reset switches so that any charge injection due to these transistors will not affect the input nodes of the first amplifier stage. The next action is to open the offset cancellation switches on the first amplifier stage. With the inputs to stage 2 tied to analog ground the charge injection, offset and non-linearity due to stage 1 will be stored on the bypass capacitors. The inputs of stage 2 are then disconnected from analog ground. The differential signal and reference inputs are sampled and subtracted (see Section 5.3.3). The difference between the signal and reference is amplified through both stages and a seed is set for the latch. Given sufficient time for the inputs to settle, the latch uses the amplified differential voltage to choose the correct single-bit digital value.

### 5.3.2. The Switches

The comparator switches were required to resolve greater than 10-bits while sampling at 10 MHz. The most critical switches are those at the inputs of the signal and reference. Note that the system is differential, which will reduce the even order harmonic distortion. The designed switch is a transmission gate as shown in Figure 5.9. The transmission gate was designed with both NMOS and PMOS transistors having equal dimensions of W/L = 30 μm/0.18 μm. There are also two dummy switches to aid in the reduction of charge injection. Each dummy switch was designed to be half the width of transmission gate.

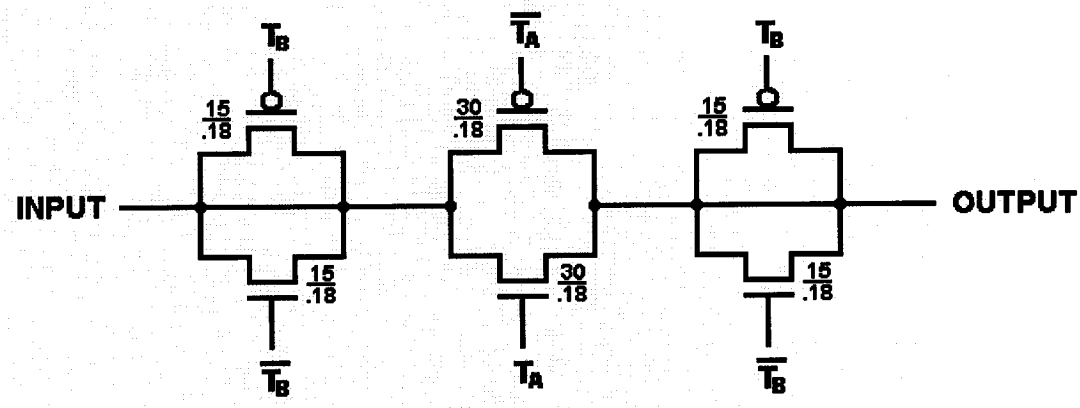



**Figure 5.9: Comparator Switch Design**

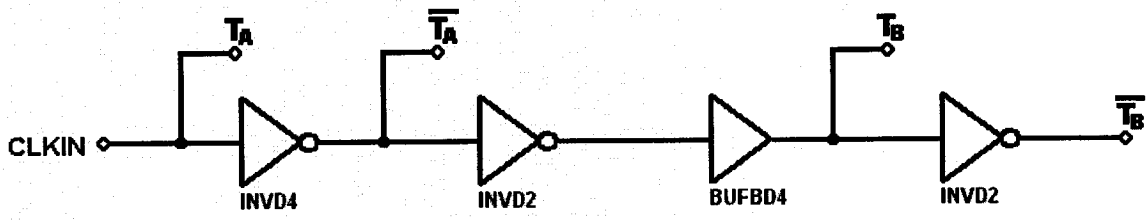



**Figure 5.10: Switch Clocking Network**

The switches are clocked with the network shown in Figure 5.10. The buffer and inverters were implemented using VSTI's 0.18 $\mu$m standard cell library. Table 5.2 presents the timing data for each gate provided by VSTI.

The differential performance of the switch was determined while operating at the extreme conditions such that sampling was performed at 100 MHz and the input signal amplitude was selected to be 0.5 V. The HSPICE post-extracted power spectral density plot is shown in Figure 5.11. The resulting signal-to-noise-and-distortion ratio was determined to be 61.2 dB.

**Table 5.2: VSTI's Standard Cell Propagation Delay on the Rising and Falling Input Signals**

| Cell | Rising (ps) | Falling (ps) |
|---|---|---|
| BUFBD4 | 146 | 134 |
| INVD2 | 30 | 20 |
| INVD4 | 28 | 18 |

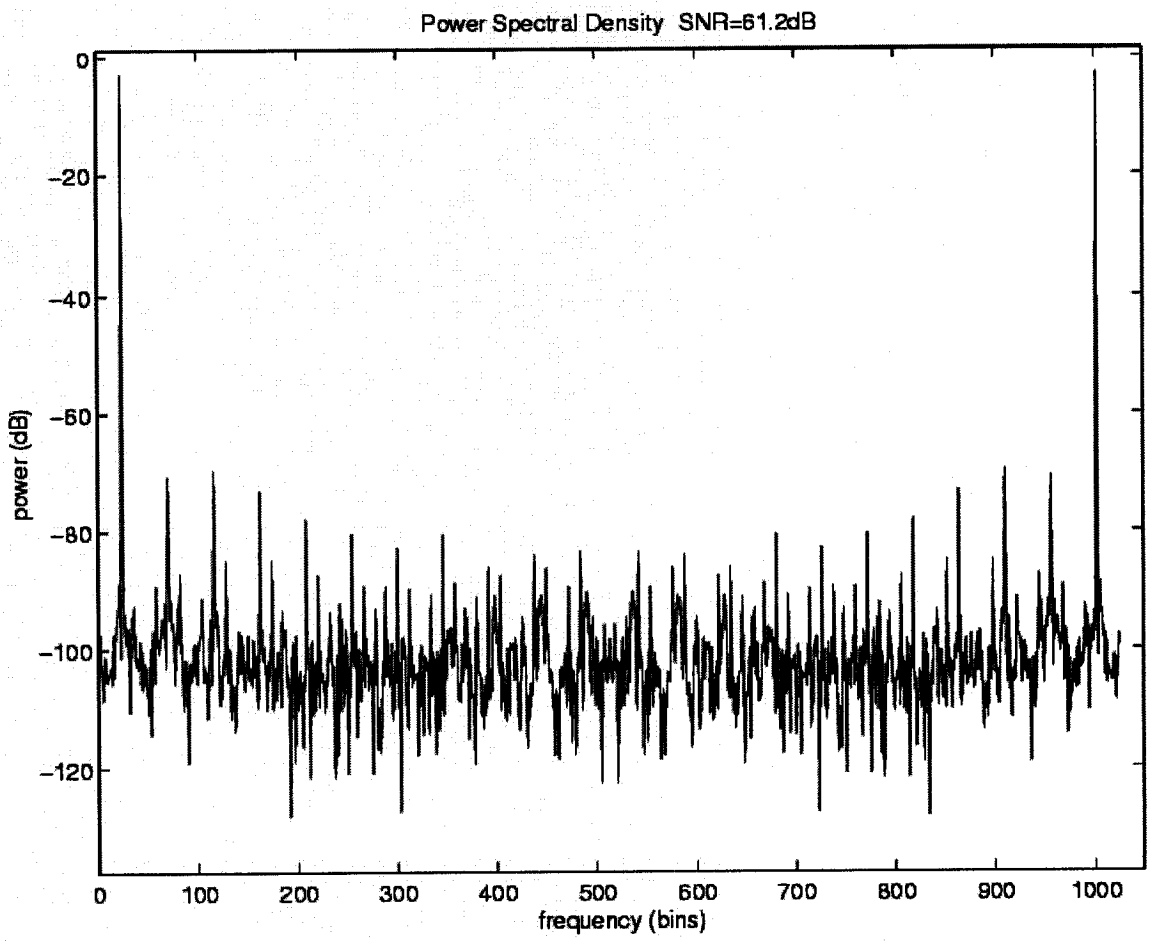



**Figure 5.11: Post-Extracted HSPICE Simulation Power Spectral Density of the Switch in Figure 5.9 when a 0.5 V, 2.2 MHz Input Signal was Sampled at 100 MHz**

### 5.3.3. The Differential Sample and Hold Circuit

The differential sample-and-hold circuit implemented is shown in Figure 5.12 [19]. This circuit operates in two non-overlapping phases. In the first phase ($\phi_1$) the sampling nodes, *IN1* and *IN2*, are reset to analog ground such that

$$V_{IN1+} = V_{IN1-} = V_{AGND} \tag{5.1}$$

and

$$V_{IN2+} = V_{IN2-} = V_{AGND} \cdot \tag{5.2}$$

The output nodes (*OUT+* and *OUT-*) are reset to a common mode voltage of the following amplifier ($V_{CM}$), such that

$$V_{OUT+} = V_{CM+} \tag{5.3}$$

and

$$V_{OUT-} = V_{CM-} \cdot \tag{5.4}$$

In the second phase ($\phi_2$) The *OUT+* and *OUT-* nodes are disconnected from the common-mode voltage and are left floating. The input signals are exposed to the sampling capacitors such that $V_{IN1+}$ = SIG+, $V_{IN1-}$ = SIG-, $V_{IN2+}$ = REF-, and $V_{IN2-}$ = REF+. The positive signal (*SIG+*) is added to the negative reference (*REF-*) generating a voltage change at the *OUT+* node. Similarly, the negative signal (*SIG-*) is added to the positive reference (*REF+*) generating an equal but opposite voltage change at the *OUT-* node.

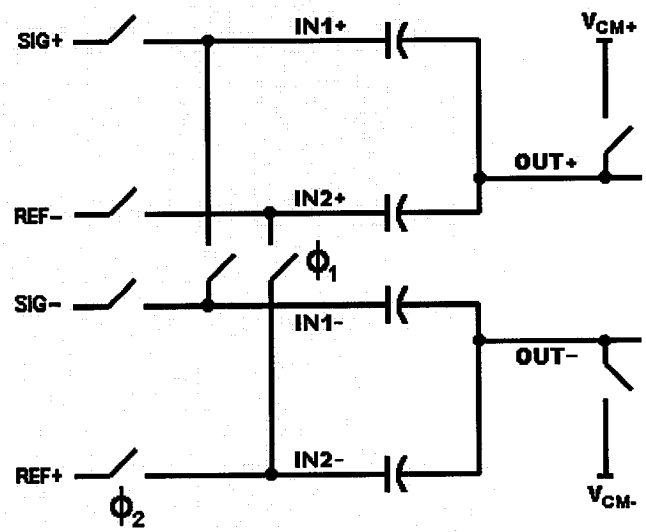



**Figure 5.12: Differential Sample-and-Hold Comparator Input Stage**

Using a differential amplifier, these two signals are subtracted and multiplied by the open-loop gain ($A$) to produce either a positive or negative voltage change at the amplifier output ($\Delta V_{AMP}$):

$$\begin{aligned}\Delta V_{AMP} &= A(V_{OUT+} - V_{OUT-}) = A[(V_{SIG+} - V_{REF-}) - (V_{SIG-} - V_{REF+})] \\ &= A(V_{SIG+} - V_{SIG-} + V_{REF-} - V_{REF+}).\end{aligned} \tag{5.5}$$

### 5.3.4. Capacitor Selection

The capacitor values in the comparator were selected based on two factors; thermal noise rejection and capacitor voltage division. The thermal noise was required to be significantly below the LSB of the digitizer. Mathematically, the thermal noise requirements are

$$V_{Thermal} \le \frac{V_{FS}}{2^D - 1} = \frac{1.8V}{2^{10} - 1} = 1.7595 \text{ mV}. \tag{5.6}$$

Furthermore, the thermal noise in a system is related by

$$V_{Thermal} = \sqrt{\frac{kT}{C}}. \tag{5.7}$$

Hence, in order to maintain the thermal noise below one LSB the capacitors should be greater than 1.34 fF, obtained as follows:

$$C \ge \frac{kT}{V_{Thermal}^2} = \frac{kT}{3.0959x10^{-6}} = \frac{(1.38x10^{-23} J/K)(300K)}{3.0899x10^{-6}} = 1.337 \text{ fF}. \tag{5.8}$$

The capacitor voltage division issue is of greater importance. Figure 5.13 demonstrates this problem with an illustration of the input stages of the comparator. The first stage amplifier was designed to detect and amplify at least an LSB voltage change at its inputs. This voltage change, as described in Section 5.3.3 is generated from the addition of SIG+ and REF- (or SIG- and REF+). This voltage change, however, is shared across the parasitic capacitance $C_P$ at the internal node. Hence, the capacitors C must be significantly greater than $C_P$ such that the minimum difference between signal and reference will still be reflected at the amplifier inputs.

The capacitor values selected were 900fF. This value is coincidently the maximum single-dimension capacitor available in TSMC's 0.18 µm mixed-signal process.

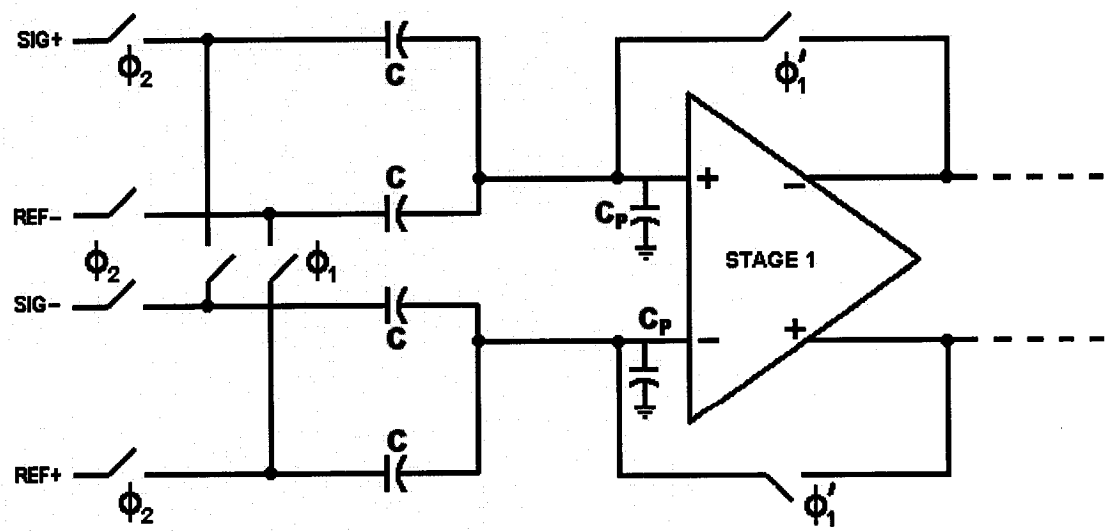



**Figure 5.13: Illustration of the Capacitor Voltage Division Problem**

### 5.3.5. First Amplifier Stage

The first amplifier stage (i.e. pre-amplifier stage) was required to amplify the least significant step size from the input sample-and-hold circuit described in Section 5.3.3. Since the desired comparator resolution is 10-bits, this implies that the initial amplifier stage must resolve at least 1.7578 mV from a 1.8 V supply voltage. An open-loop architecture [20] was selected for this amplifier stage as it has high resolution and good offset cancellation characteristics.

Figure 5.6 shows the relationship of the amplifier within the comparator. During the reset phase of regular operation, the differential amplifier is configured with unity gain. During the capture phase, the amplifier switches are opened and the input change from the sample-and-hold output is amplified.

The transistor level circuit of Figure 5.14 illustrates the design of the pre-amplifier stage. The dimensions of the design transistors are shown in the figure. This design is simply an actively-loaded differential pair with a common-mode feedback circuit [18] controlled by a bias voltage $V_{BIAS}$. The bias voltage would normally be adjusted to analog ground (i.e. 0.9 V).

This circuit was simulated using HSPICE while implementing TSMC's 0.18 µm process models. The post-layout extracted results are summarized in Table 5.3. The frequency response of this amplifier is shown in Figure 5.15.

**Table 5.3: Performance Parameters of the Post-Extracted First-Stage Amplifier**

| | |
|---|---|
| DC Gain | 67.5 V/V |
| 3 dB Bandwidth | 112 MHz |
| Phase Margin | 76° |
| Slew | 1.2 V/ns |

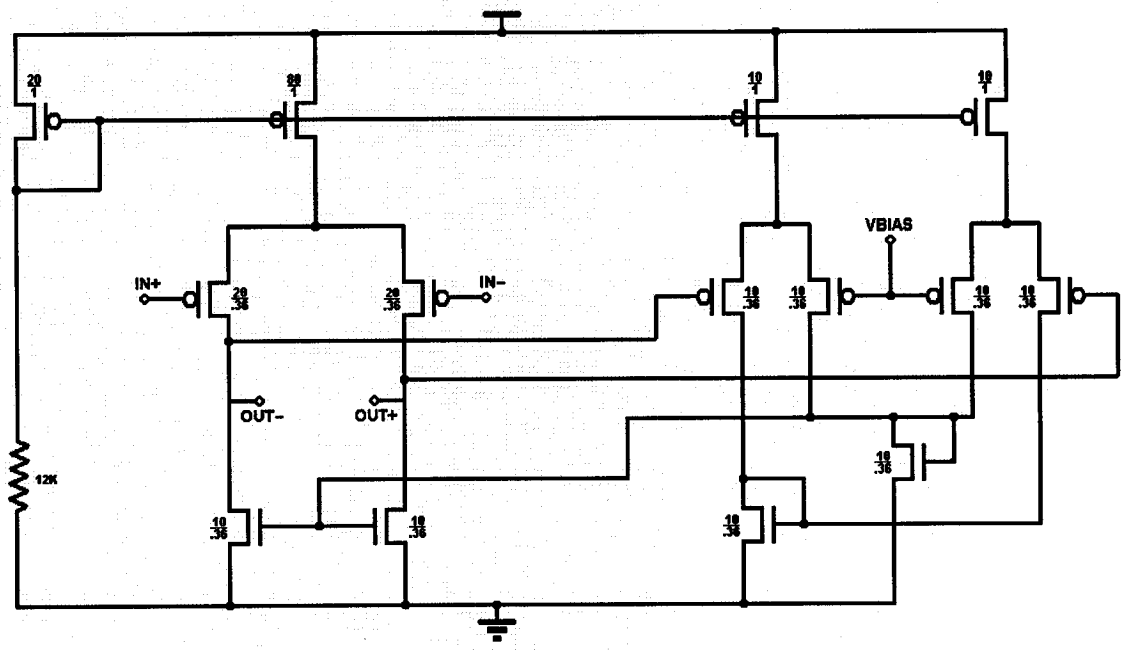



**Figure 5.14: Transistor Level Circuit Design of the Comparator's First Amplifier Stage**

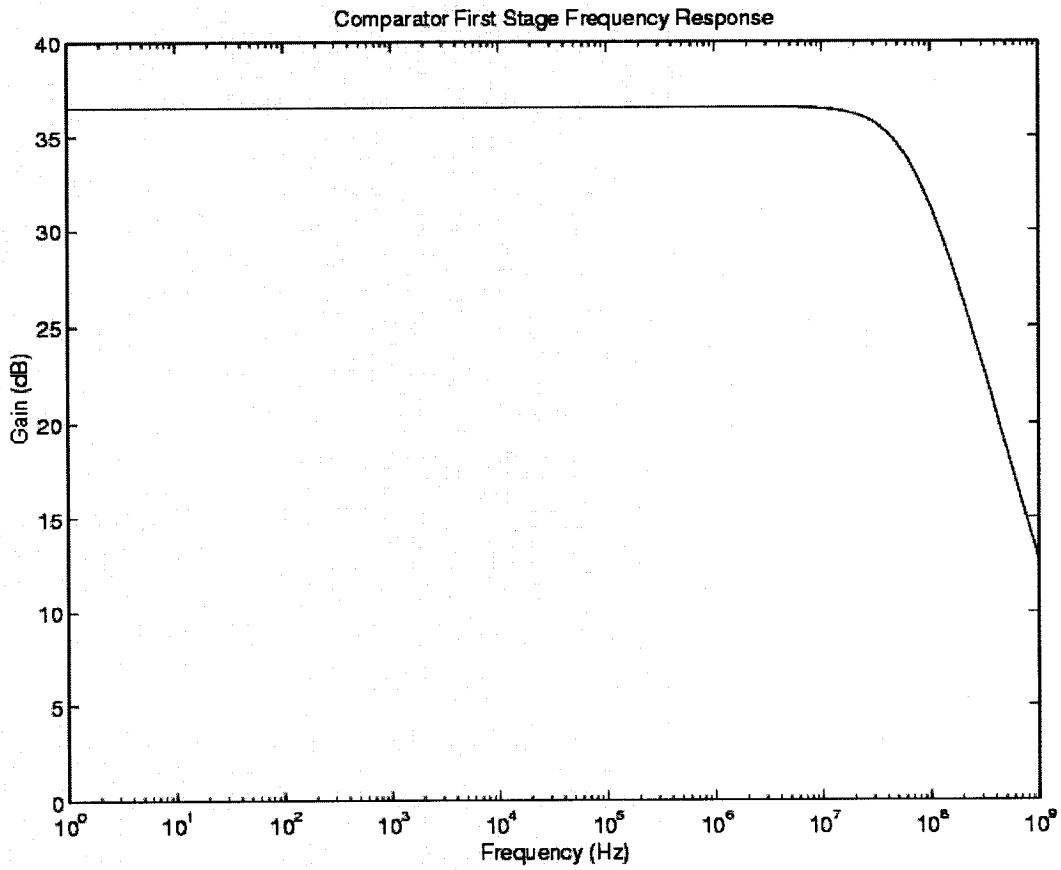



**Figure 5.15: Frequency Response of the Comparator's First Stage**

### 5.3.6. Second Amplifier Stage with Latch

The circuit shown in Figure 5.16 demonstrates the transistor level diagram of the second stage amplifier and latch of the comparator of Figure 5.6. This design was adopted and modified from [21].

This circuit operates in two overlapping phases. Each phase, controlled by the latch signal, is generated by the clocking circuitry in Section 5.3.1. During the latch='1' phase the amplifier is sensing the differential input and is generating a "seed" for the latching transistors which are temporarily disconnected from ground. In the second phase (i.e. latch='0') the latching transistors are reconnected to ground and a positive feedback loop forces O+ and O- towards opposite power supplies.

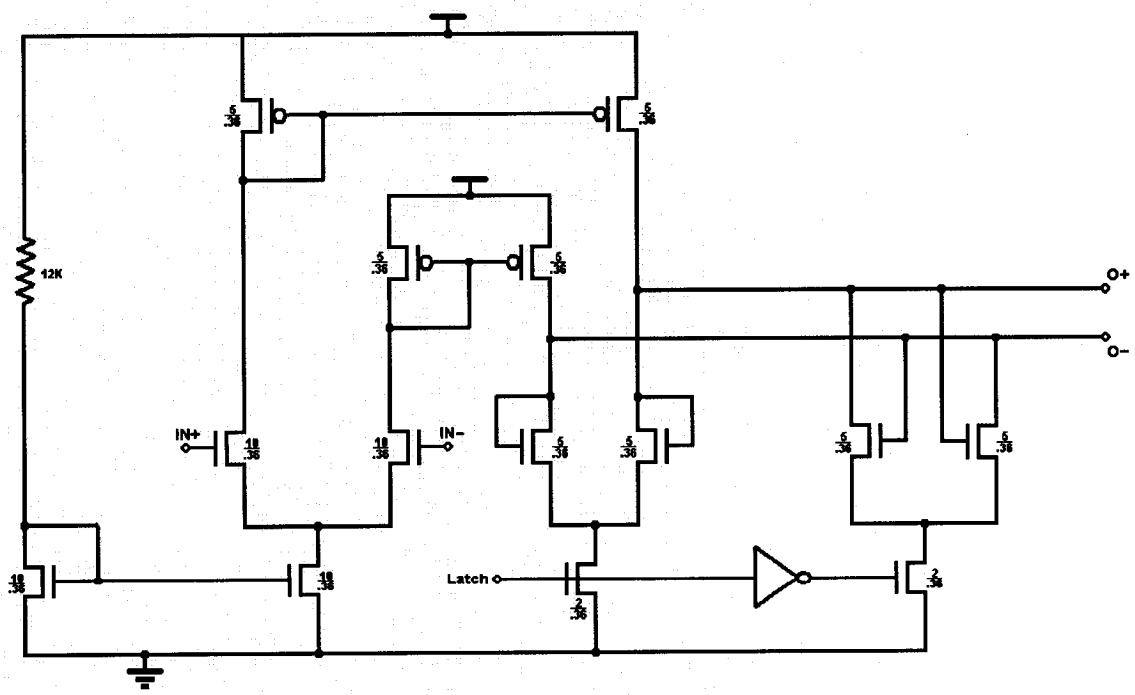



**Figure 5.16: Transistor Level Circuit Design of the Comparator's Second Amplifier with Latch Stage**

The latch sensitivity is mainly influenced by transistor mismatch. In other words, the gain of the first and second stages combined must produce a seed that can overcome any mismatch in the latch. The circuit in Figure 5.16 was simulated with a 20% mismatch between the latching transistors. The results indicated that the minimum differential input voltage to generate the correctly digital output is 6mV. The first amplifier stage will guarantee that this minimum input difference is produced in response to an LSB input difference. The frequency response characteristic for the second stage is shown in Figure 5.17.

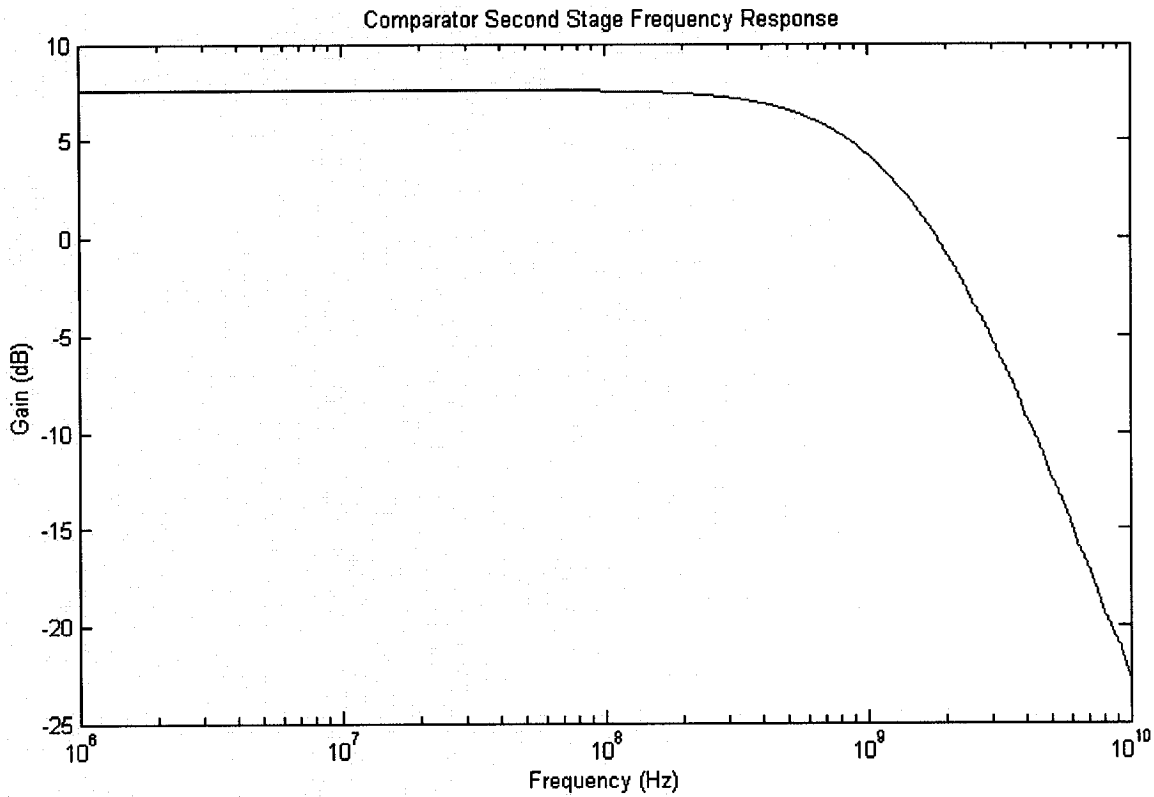



**Figure 5.17: Frequency Response of the Comparator's Second Stage**

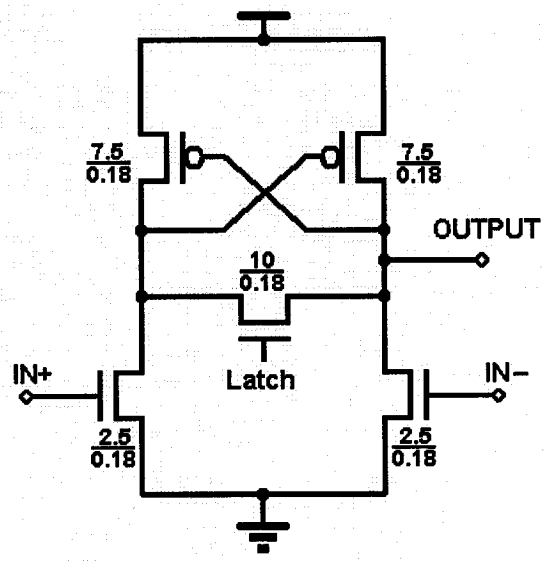
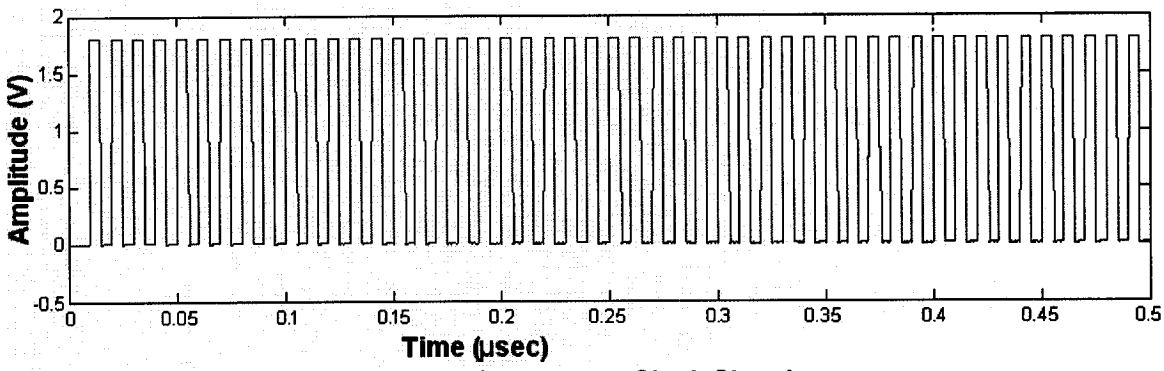



**Figure 5.18: Transistor Level Circuit Design of the Comparator's Second Amplifier Latch**

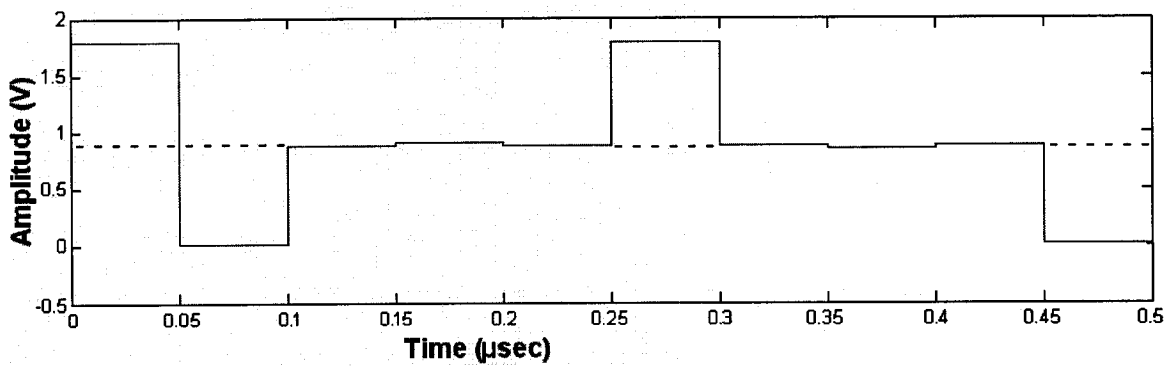
A second latch, shown in Figure 5.18, was added to the outputs of the amplifier to aid in latching time, to hold the latched signal for longer duration, and to decouple the amplifier nodes from other loading circuits. The output from this point forward was taken single ended.

### 5.3.7. Simulation Results of the Comparator Design

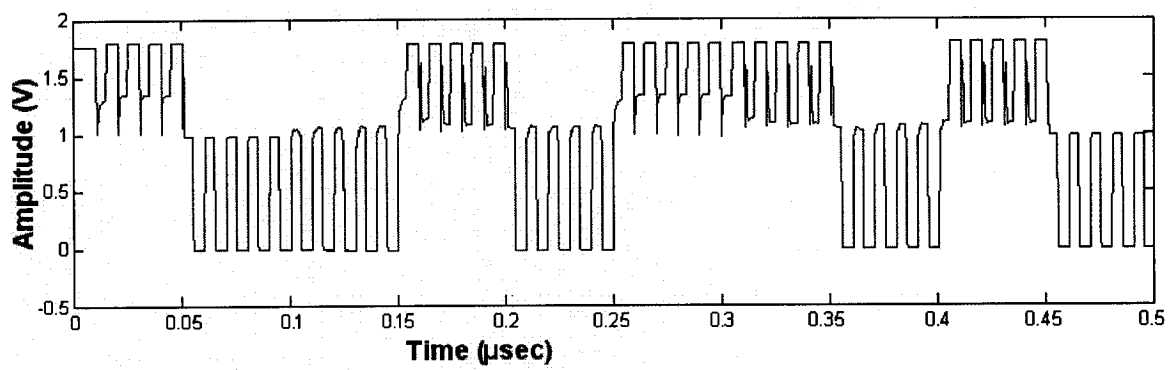
A test to exercise the post-extracted layout of the comparator was performed using the HSPICE simulator. The comparator was clocked at a rate of 10 MHz. With a reference of half the power supply (i.e. analog ground), a differential, multi-step input waveform was forced at the inputs. Figure 5.19 illustrates (a) the comparator clock, (b) one input waveform and (c) the output from the comparator. From the input waveform, it may be observed that whenever the signal voltage crosses the reference (0.9 V) the output signal changes polarity as expected.




(a) Comparator Clock Signal




(b) Comparator Input Signal (Reference voltage = 0.9V)




(c) Comparator Output

**Figure 5.19: Dynamic Test Simulation for the Post-Extracted Comparator**

## *5.4 - Simultaneously-Sampling Dual-Digitizer Implementation*

The simultaneously-sampling dual-digitizer design was implemented as shown in Figure 5.20. Both comparators are clocked from the same external source. The digitization is performed using the multipass method. The required 1024 DC reference levels, outlined in section 5.4.1, were generated using a programmable DC voltage generator. Due to the test equipment limitations, the single-bit outputs from both digitizers were converted to 4-bit parallel outputs using a shift register with parallel outputs. This device is presented in Section 5.4.2.

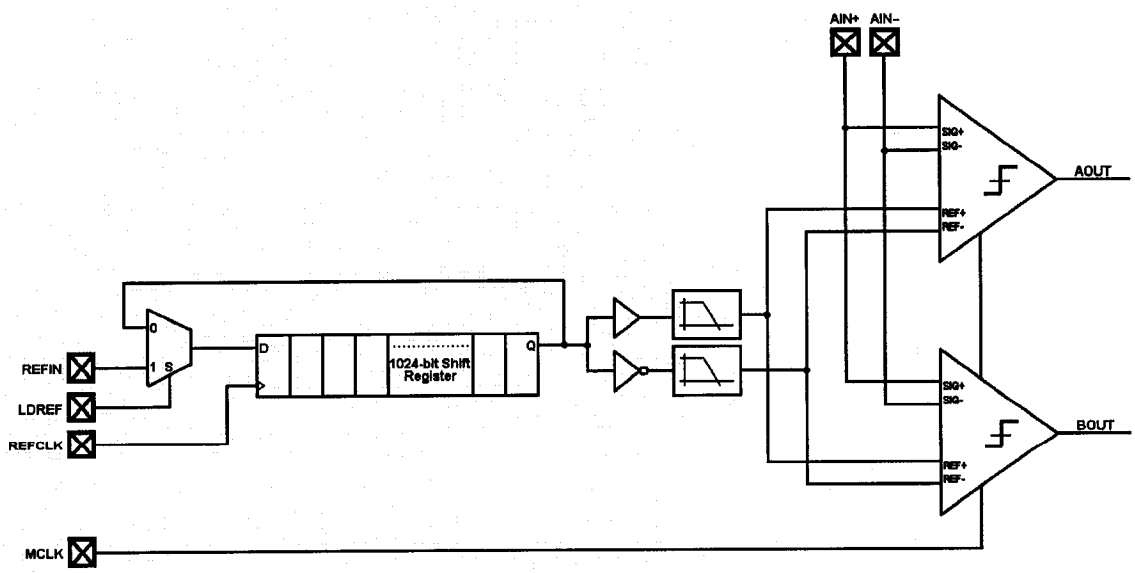



**Figure 5.20: Simultaneously-Sampling Dual-Digitizer Implementation**

### 5.4.1. DC Generator

The multipass method of digitization requires $2^D$-1 reference levels to compare with the input signal, where D is the ADC resolution. These references were generated by filtering pulse-density (i.e. sigma-delta) modulated DC values. Each DC value is serially loaded into the 1024-bit shift register by asserting the *LDREF* signal and shifted the data in with respect to the *REFCLK* clock signal. When all values have been loaded, the *LDREF* signal goes low and the shift register rotates the bits around the register through the multiplexer, at the rate of *REFCLK*.

The bit stream is also inverted to produce a differential reference voltage. Each bit-stream is passed through a DC filter, shown in Figure 5.21, to remove most of the AC components. Thus, the requirements on the DC filter are such that the ripple in the output DC value must be less than half of an LSB. The DC filter coefficients were selected based on MATLAB simulations.

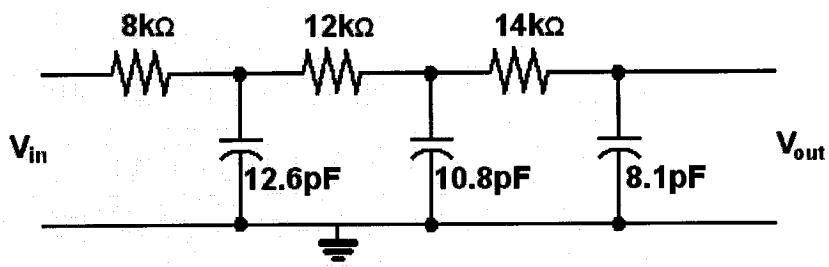



**Figure 5.21: DC Filter**

### 5.4.2. Serial-to-Parallel Conversion

The device was to be tested on a Teradyne A567 ATE. The maximum digital capture clock speed of the ATE is 25 MHz. Moreover, the capture memory is limited to 1 MB. In order to increase the clock speed and ensure that sufficient memory is available, the serial data from the digitizers were converted to 4-bit parallel data. The circuit used to convert the serial data to 4-bit parallel data is given in Figure 5.22.

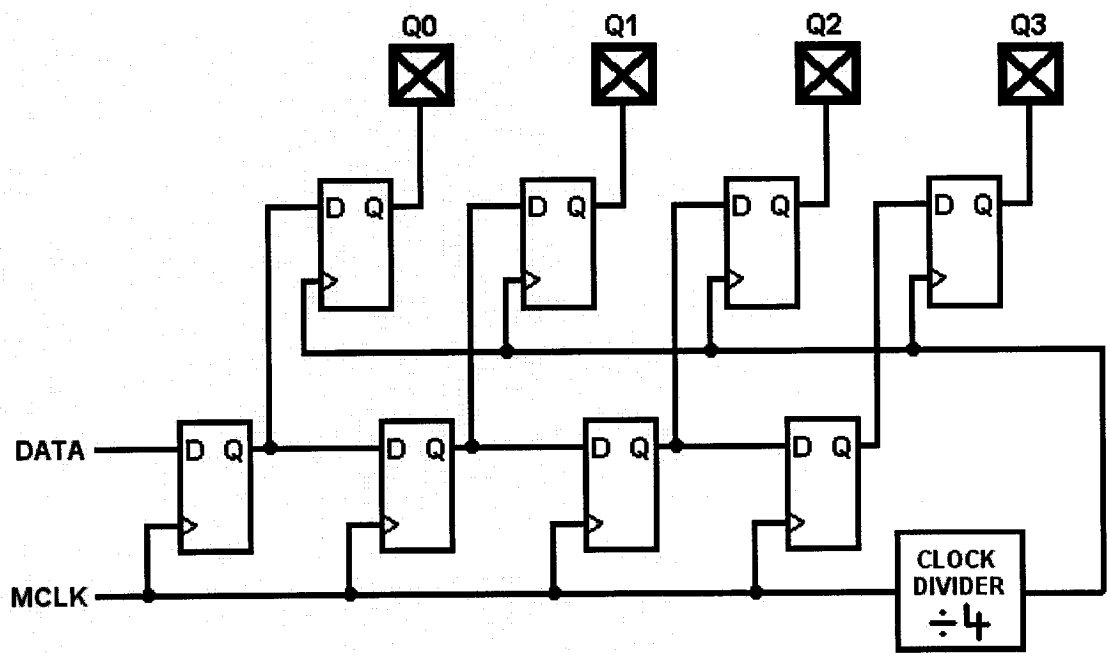



**Figure 5.22: Serial to Parallel Conversion at the Digitizer Outputs**

## 5.5 - Time-Interleaved Quintuple-Digitizer Implementation

The time-Interleaved quintuple-digitizer design was implemented using five comparators. Each comparator, described in the Section 5.3, was sourced by the same DC reference generator and external test signal. The schematic diagram is shown in Figure 5.23. The DC reference generator and filter were described in Section 5.4.1.

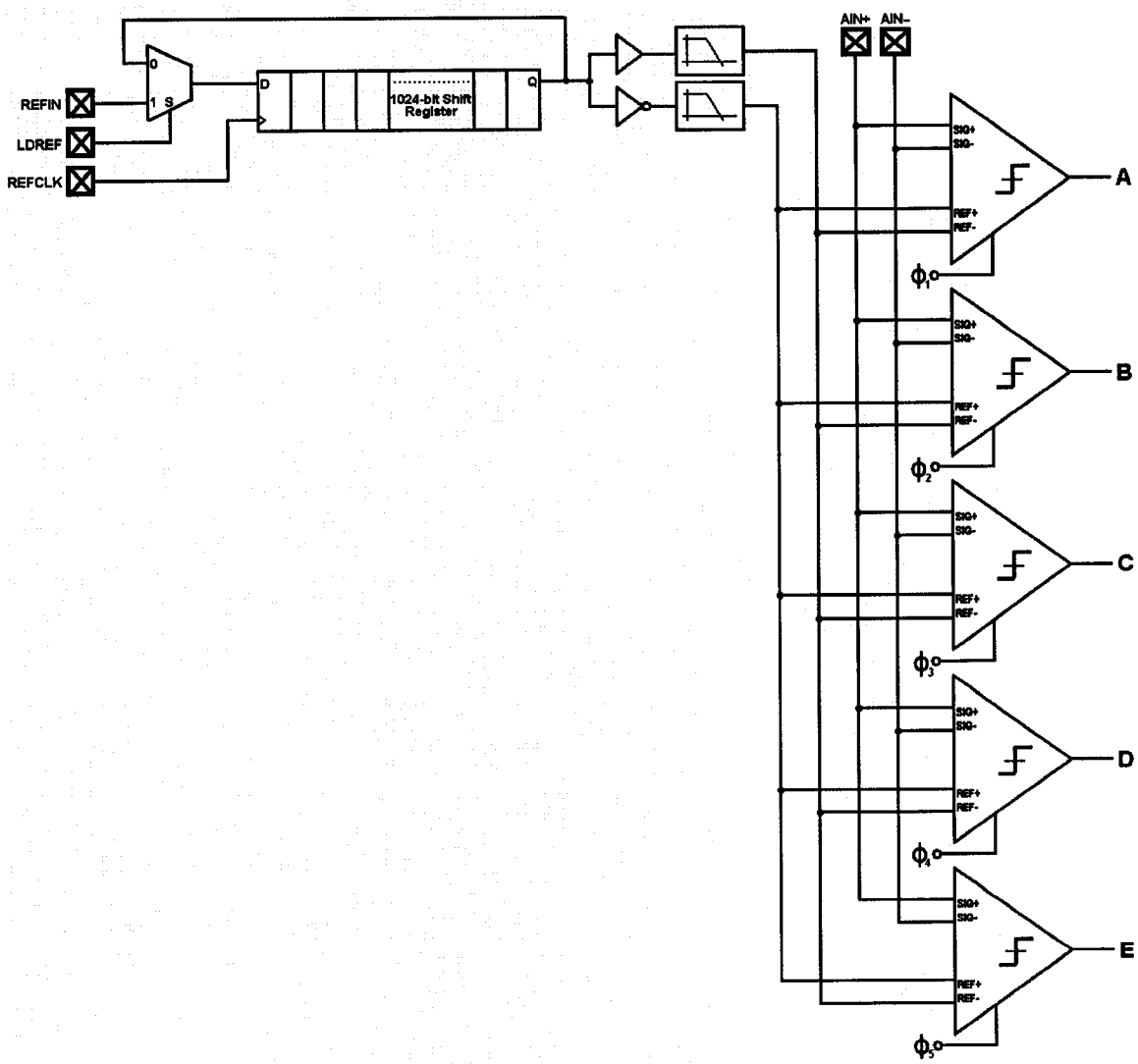



**Figure 5.23: Time-Interleaved Quintuple-Digitizer Implementation**

Each comparator was required to be clocked in one-fifth the clock period. In order to easily create a phase generator without implementing a PLL, the circuit of Figure 5.24 was designed. When the flip-flops are reset, the first three are cleared (i.e. $\Phi_1\Phi_2\Phi_3 = 000$), while the last two are set (i.e. $\Phi_4\Phi_5 = 11$). After a reset the clock will circularly shift the five bit pattern $\Phi_1\Phi_2\Phi_3\Phi_4\Phi_5$. Hence, the rising edge of the output phases will only occur for one output every clock cycle.

The outputs of the five comparators needed to be multiplexed to the output pins. In order to maintain the correct timing for the comparator data, the circuit of Figure 5.25 was designed to generate the multiplexer select encoding based on the clock phases. The multiplexed serial comparator outputs were passed through an 8-bit serial-to-parallel register in order to operate at high speeds while accommodating the A567 ATE clock limits and memory constraints. The circuit diagram of 5.26 demonstrates the interaction between the comparator multiplexer, control logic, and serial-to-parallel converter.

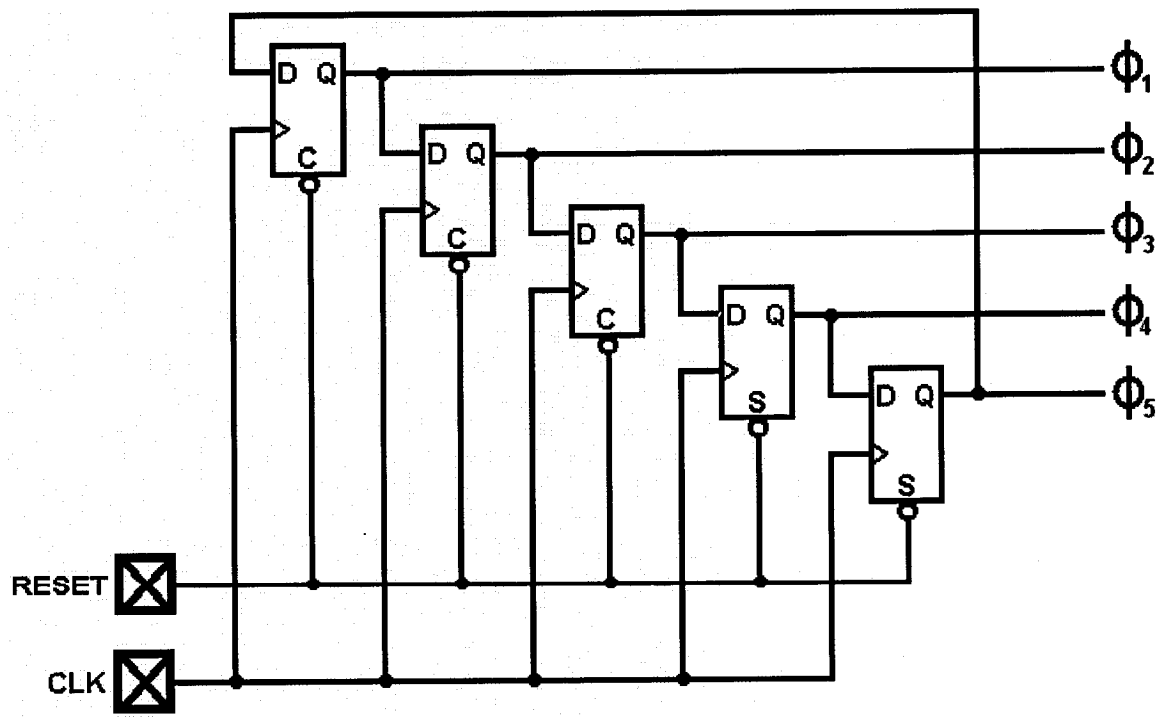



**Figure 5.24: Five-Phase Time-Interleaved Clock Generator**

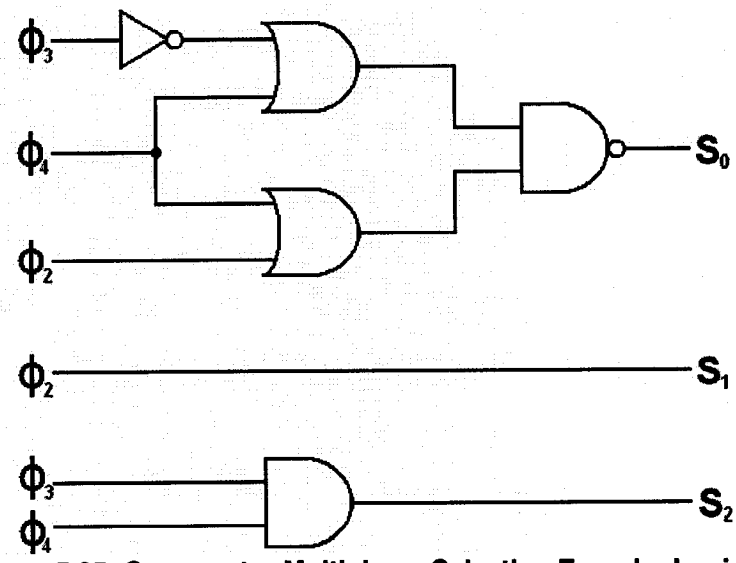



**Figure 5.25: Comparator Multiplexer Selection Encoder Logic**

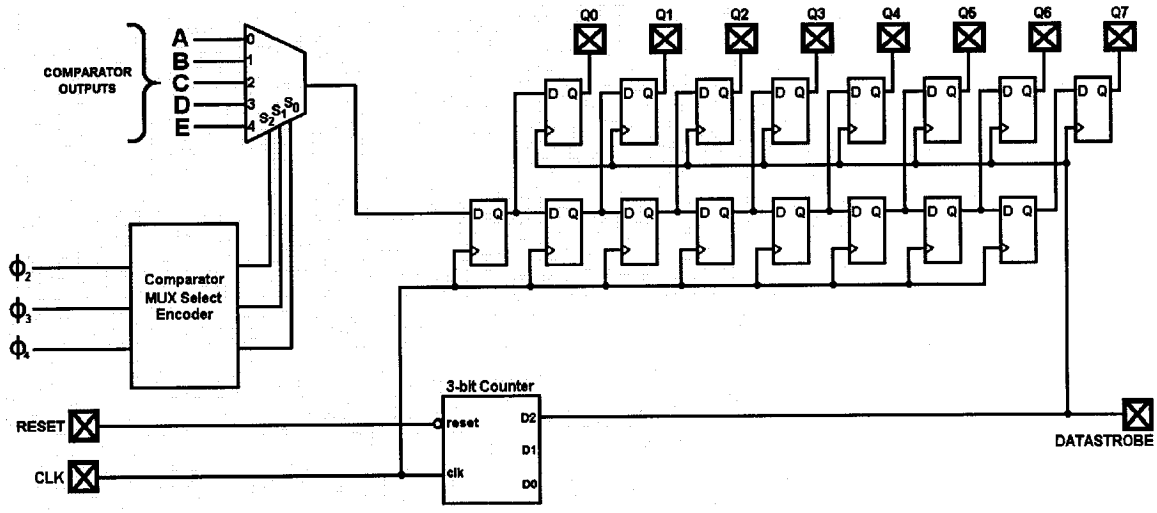



**Figure 5.26: Output Block Diagram for the Time-Interleaved 5-ADC Design**

## *5.6 - Summary*

The implementation of the simultaneously-sampling dual-ADC and time-interleaved quintuple-digitizer designs were presented in this chapter. The basic building block for both designs is a comparator. Hence, the comparator design was described in great detail. A micrograph of the integrated circuit is illustrated in Figure 5.27. The die dimensions are 3 mm x 3 mm. The area of each comparator amounts to 0.0184 $mm^2$. The DC generator and filters occupy a silicon area of 0.144 $mm^2$.

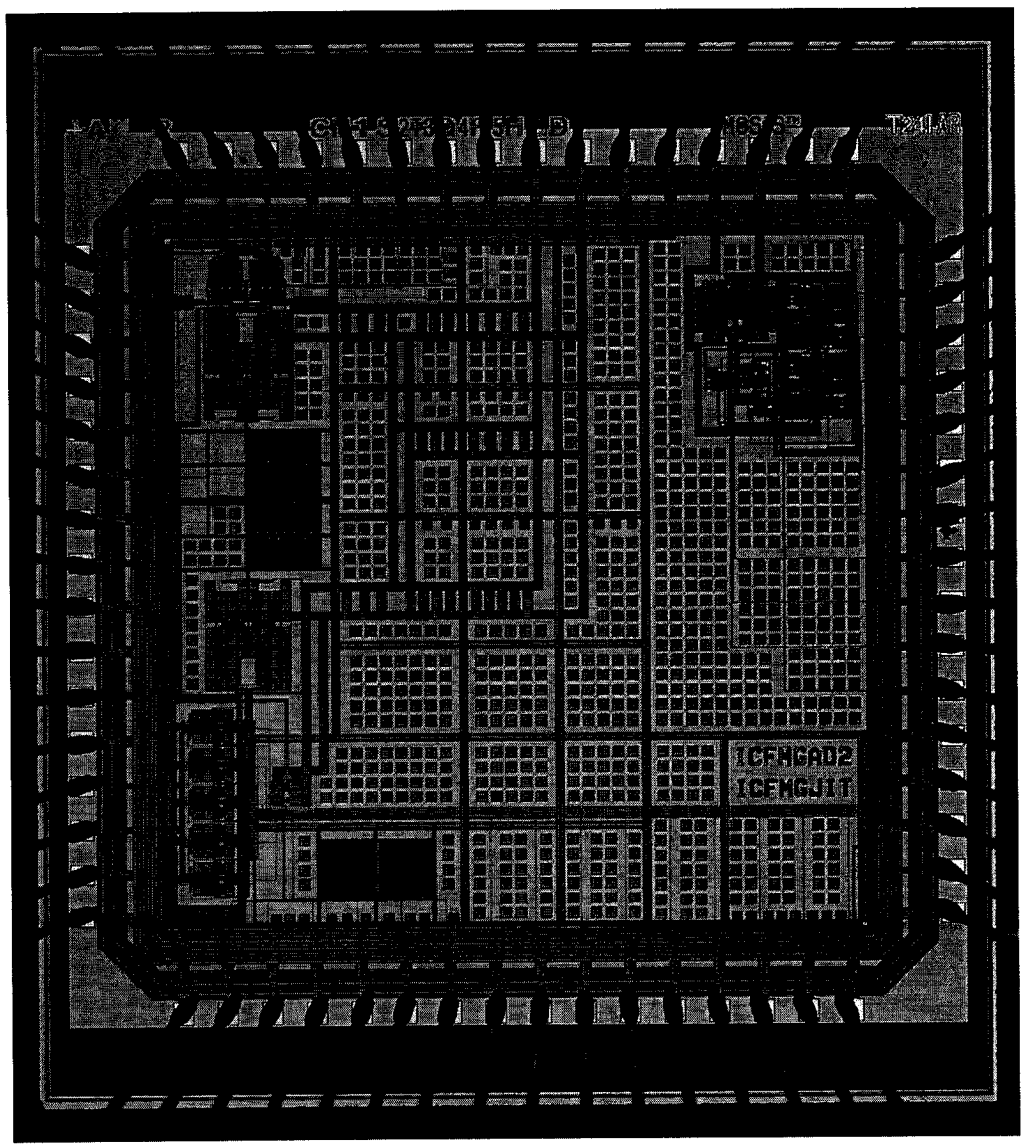


**Figure 5.27: Micrograph of the Two Digitizer Designs Integrated into a Single Die**

# Chapter 6: Experimental Setup and Results

## 6.1 - Introduction

The time-interleaved quintuple-digitizer design and the dual-channel simultaneously-sampling digitizer design, described in Chapter 4, were experimentally tested using a Teradyne A567 ATE. The test setup for both designs is described in Section 6.2. Characterization of a single test core digitizer is presented in Section 6.3. The results of the dual-channel simultaneously-sampling digitizer and the application of the bias removal technique are presented in Section 6.4. Section 6.5 reveals the experimental results of the time-interleaved digitizer.

## 6.2 - Test Setup

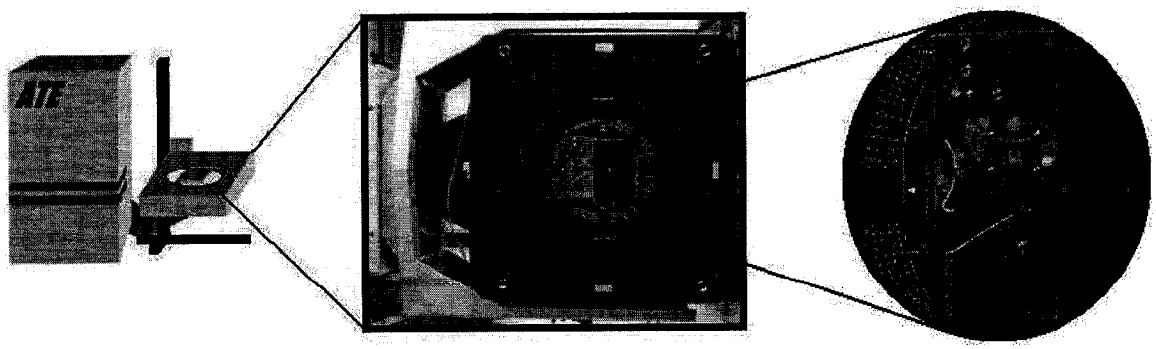
All tests were performed using a Teradyne A567 ATE. The A567 has a maximum digital clocking speed of 25 MHz, and is equipped with 16 digital I/O cards, four DC sources, two high-current DC sources, one precision low-frequency source (PLFSRC) and one precision low-frequency digitizer (PLFDIG). The PLFSRC has a maximum bandwidth of 500 kHz. The PLFDIG has a maximum bandwidth of 100 kHz.

A two-layer printed circuit board (PCB) was fabricated to interface a device interface board (DIB) with straight 2-row headers. Figure 6.1 illustrated the test setup whereby an ATE illustration is depicted and the actual A567 testhead and the designed PCB are shown. The PCB was designed with a digital ground plane on the bottom surface.

The required power supply voltages (3.3 V, 1.8 V, and 0.9 V) were set using the various A567 sources. The analog stimulus was generated differentially by the PLFSRC. The digital control signals and digital data were set and captured via the A567 digital I/Os. To increase the clocking rate of the DC reference generator, the reference clock was multiplexed such that an A567 clock (25 MHz) was used to load the DC data and an external clock (~200 MHz) was used, through an SMA connector, to run the generator.

## *6.3 - Single Digitizer Characterization*

A single digitizer was characterized to identify the performance of the test core. The transfer curve, illustrated in Figure 6.2, was obtained by sweeping the input dynamic range and collecting the digital output for each input value. A portion of the curve is enlarged to illustrate step function behavior.




**(a) ATE** **(b) Testhead with DIB** **(c) PCB on DIB**

**Figure 6.1: Test Setup Illustration**

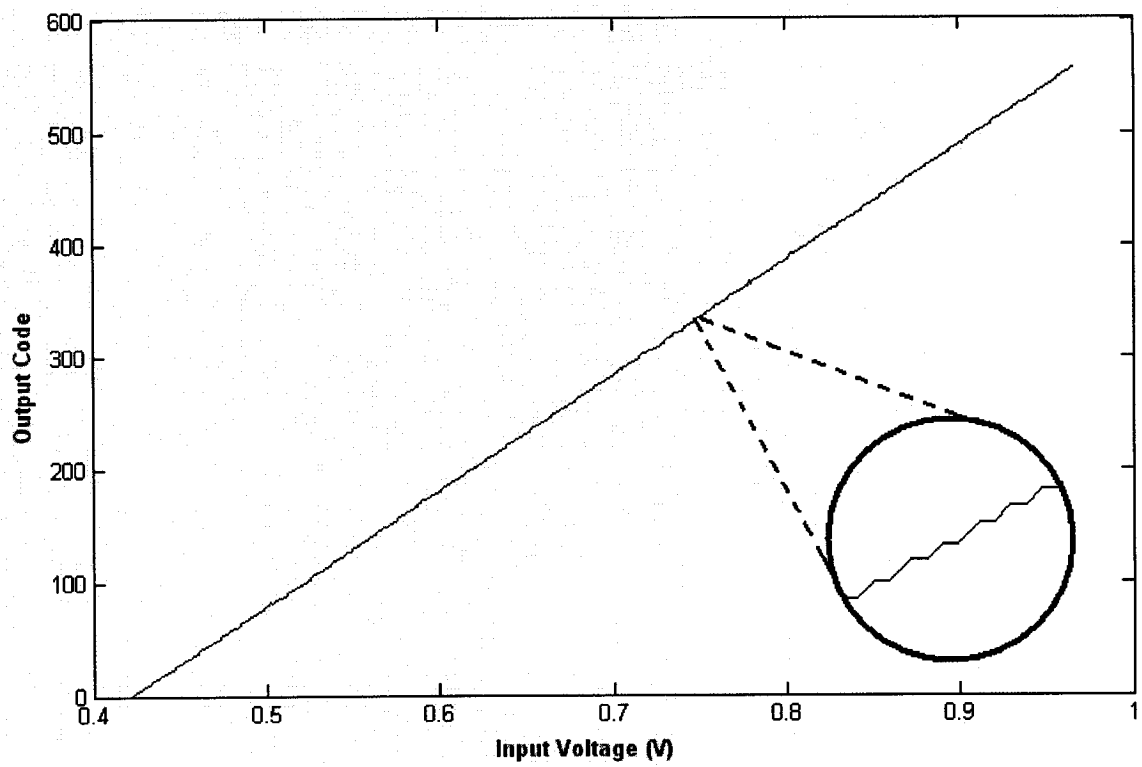



**Figure 6.2: Transfer Curve of a Single Test Core Digitizer**

The integral non-linearity (INL) plot was calculated by differencing the transfer curve with a line-of-best-fit. The resulting difference was normalized to an LSB step size. Figure 6.3 represents the INL plot for a single digitizer. From this data we may conclude that the digitizer is linear to within ±0.8 LSB.

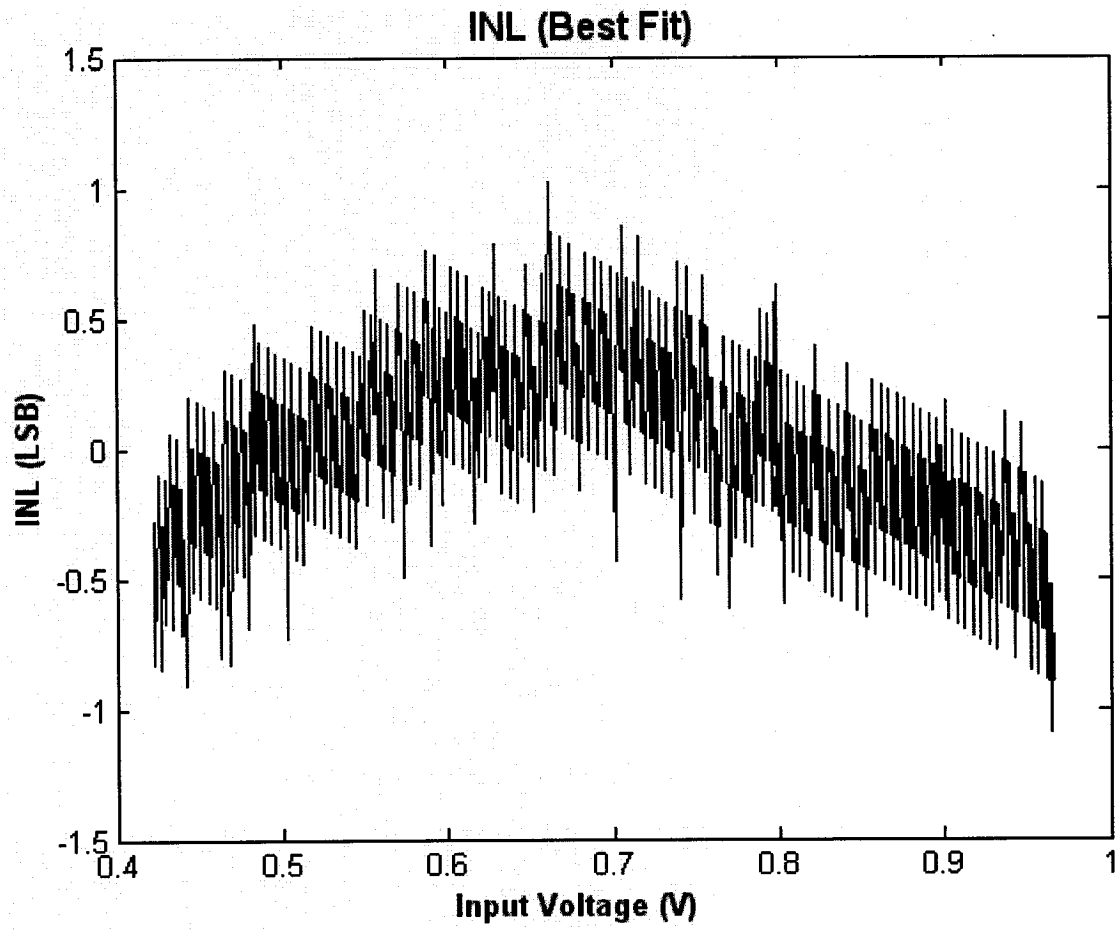



**Figure 6.3: INL of a Single Test Core Digitizer**

Dynamic behavior was characterized by stimulating the digitizer with a coherent sinusoidal test signal. The resolution of the stimulus signal was extracted using the PLFDIG and was determined to have a 16-bit resolution. A dynamic range test was performed to determine the optimal signal amplitude range. The results were extracted using a 100 kHz input test signal, while collecting 4096 points and sampling at 2 MHz. The results are given in Figure 6.4. From these results we may conclude that that optimum input signal should have an amplitude of 0.56 V.

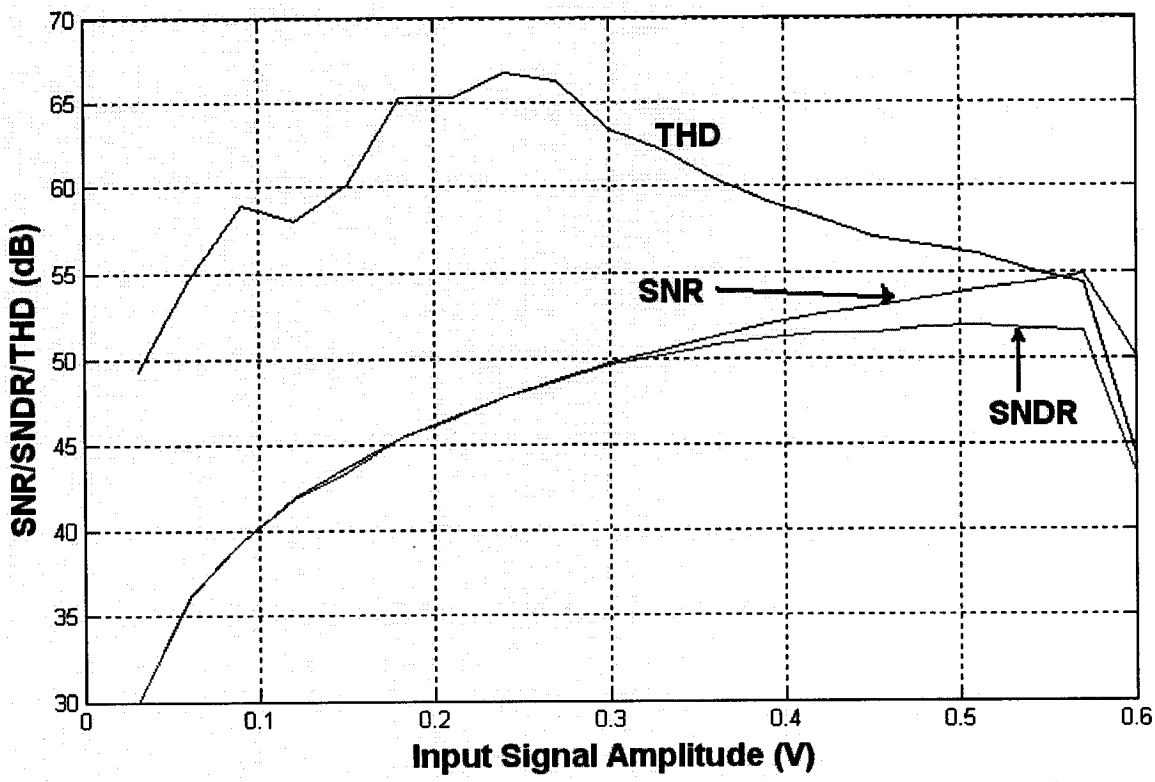



**Figure 6.4: Dynamic Range Plot for a 100 kHz Input Signal Sampling at 2 MHz**

A second dynamic test was performed to demonstrate the effective resolution of the ADC or various input frequencies. Figure 6.5 presents the results of SNR, SNDR, and THD for a 0.5 V input signal sampling at 2 MHz. It may be seen that the effective-number-of-bits (ENOB) is in the order of 8.3-bits.

Finally, an example of a captured time domain waveform and its PSD are shown in Figure 6.6. The input signal in this demonstration was a 1 Vp-p, 100 KHz sinusoid. The ADC was sampling at 2 MHz. The SNDR from this example is 51 dB.

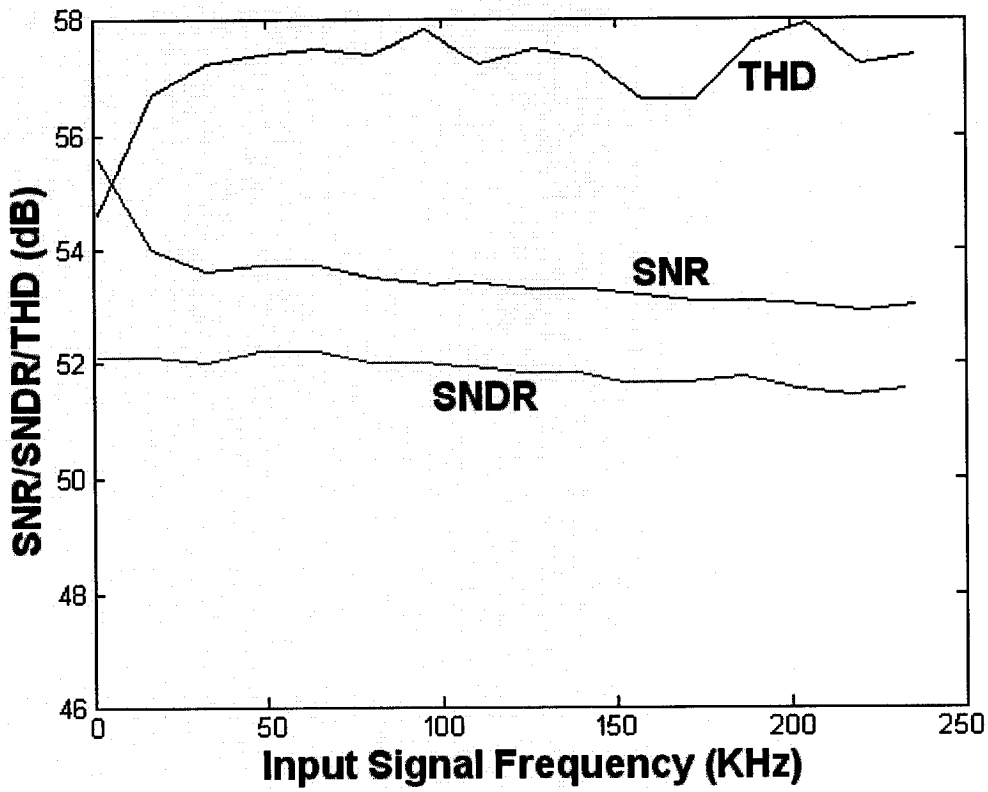
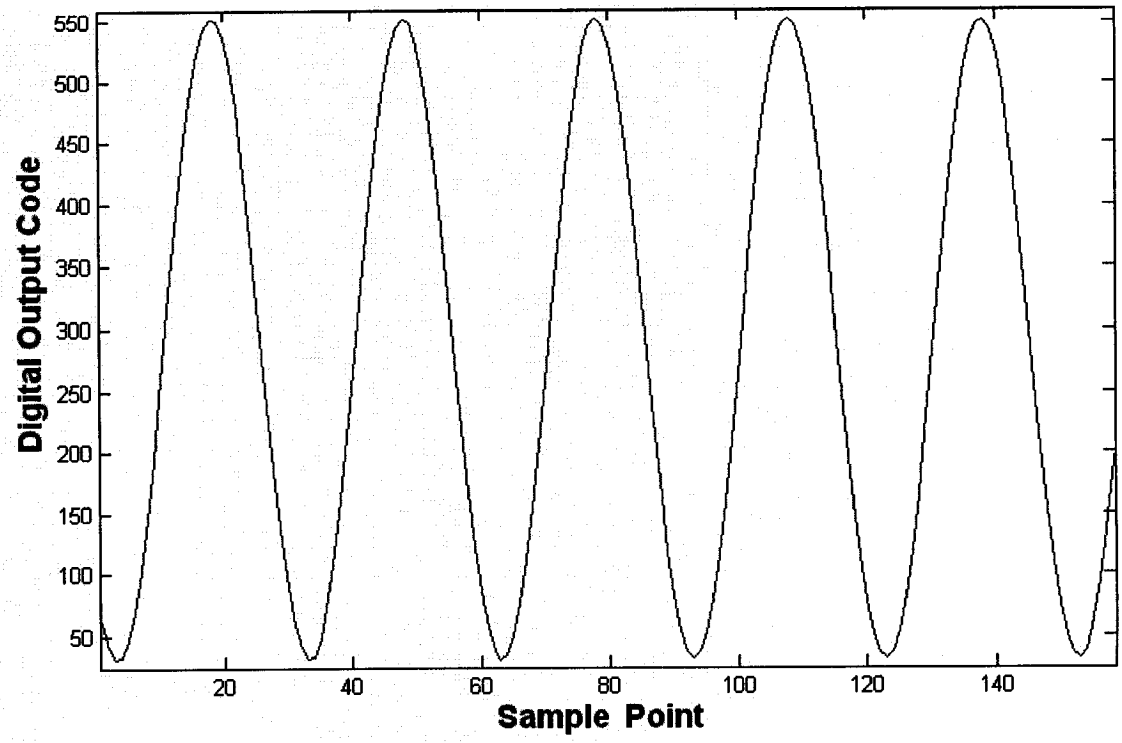
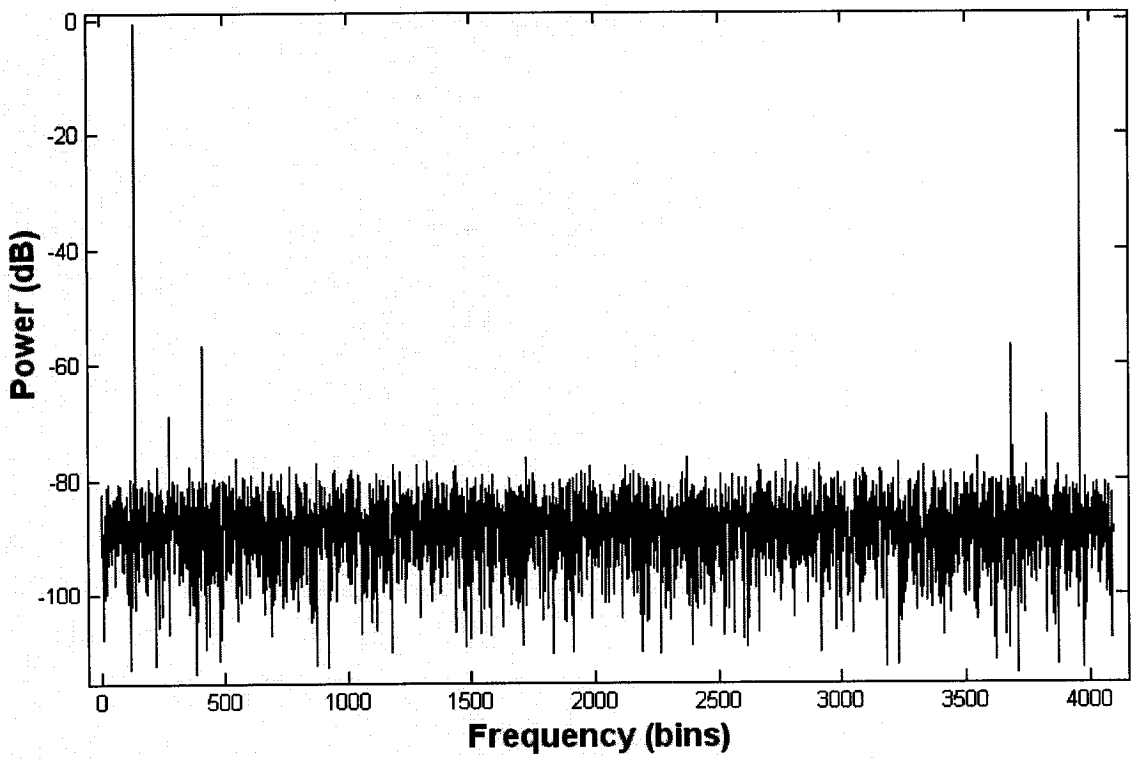



**Figure 6.5: Transmission Parameters as a Function of Input Frequency**




**(a) 100 KHz Input Signal Sampled at 2 MHz**




**(b) Power Spectrum of a 100 KHz Input Signal Sampling at 2 MHz**

**Figure 6.6: Captured Signal and its Power Spectrum**

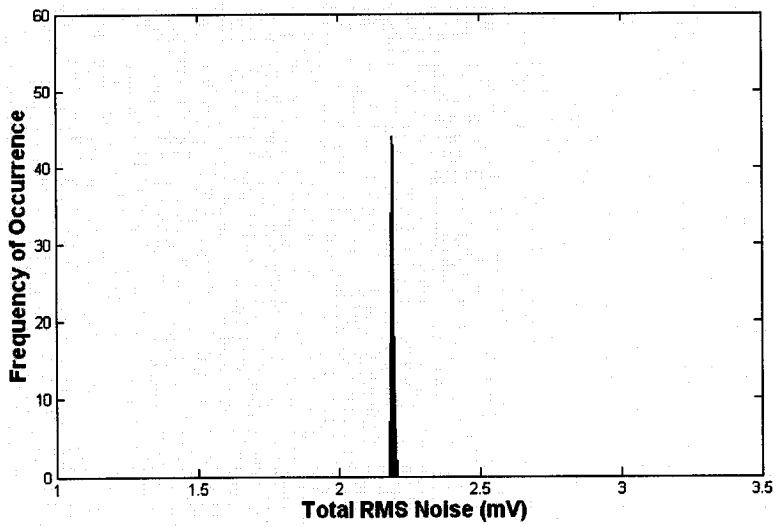
## *6.4 - Simultaneously-Sampling Dual-Digitizer Experimental Results*

The simultaneously-sampling dual-channel test core digitizer described in Chapter 4 was constructed in TSMC's 0.18 μm CMOS technology. The circuit was tested using a Teradyne A567 ATE.

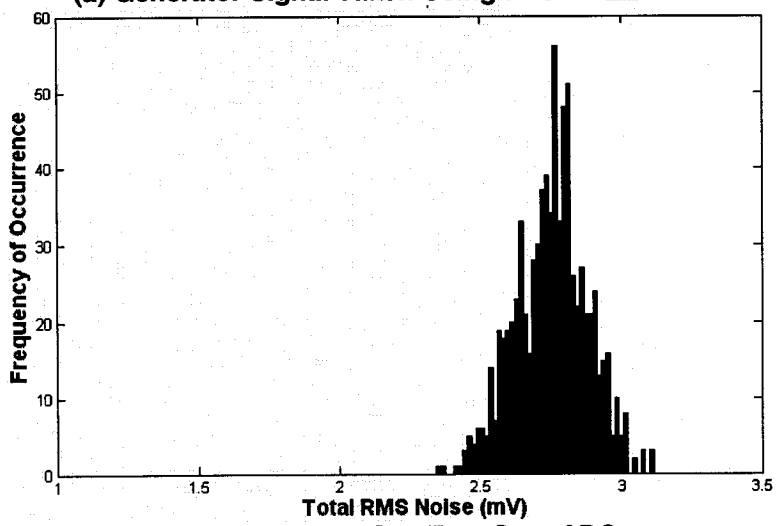
In order to show that the simultaneously-sampled dual-digitizer can remove bias error from measurements, a repeated experiment was performed to capture total RMS noise. The dual-channel test core was exercised with a 1 Vp-p, 100 kHz input test signal while sampling at 2 MHz. A thousand data samples were collected from each ADC output. Figure 6.7(a) shows the distribution of generator signal collected using a 23-bit precision low-frequency digitizer (PLFDIG) equipped on the A567 ATE. This data is a representation of the ideal measurement result. The repeated noise power measurement from the output of one ADC is shown in Figure 6.7(b). Subsequently, Figure 6.7(c) reveals the result of applying the bias error removal technique. A summary of the measured results is listed in Table 6.1. As is evident, the mean value correlates quite closely with the result obtained from the 23-bit ADC, thus allowing us to conclude that the bias of the ADC was successfully removed. No improvement to the standard deviation of the ADC output was observed or expected.

**Table 6.1: Numerical Results from Figure 6.7**

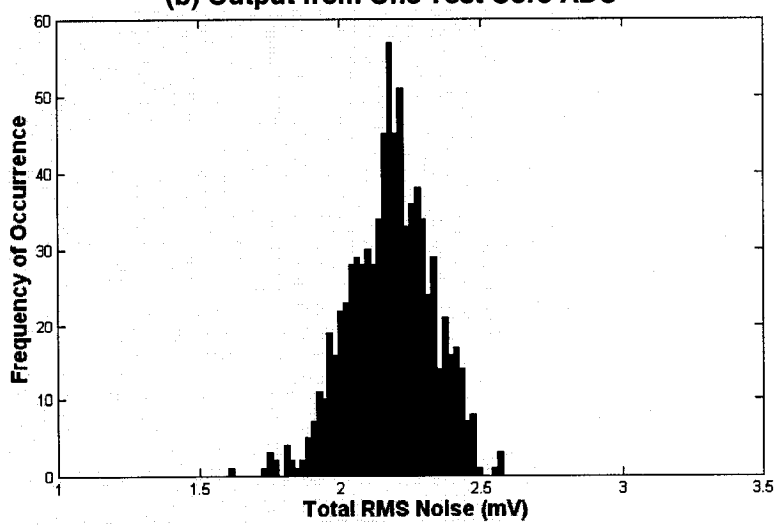
| | Generator | ADC Output | Corrected Value |
|---|---|---|---|
| **Mean** | 2.20 mV | 2.82 mV | 2.20 mV |
| **Std.Dev.** | 4.5 μV | 128 μV | 146 μV |




(a) Generator Signal Taken Using a 23-bit ΣΔ ADC




(b) Output from One Test Core ADC




(c) ADC Mean Removed from Measurement

**Figure 6.7: Total RMS Noise Power Measurement Using Simultaneously-Sampling Dual-ADC Approach**

## *6.5 - Time-Interleave Quintuple-Digitizer Experimental Results*

The quintuple-channel time-interleaved integrated design was used to capture five sets of data from a precision low-frequency signal generator (PLFSRC) from the ATE. The digitizers were stimulated with a 1 Vp-p, 100 kHz input test signal sampling at 10 MHz. The acquired test parameter was total RMS noise.

The measurements were repeated 500 times. Fig. 6.8(a) demonstrates the use of one digitizer capturing 500 samples. The mean and deviation from one ADC was $\mu$ = 438 $\mu$V and $\sigma$ = 32 $\mu$V. The use of five ADCs yielded a mean and deviation of $\mu$ = 439 $\mu$V and $\sigma$ = 15 $\mu$V, as shown in Fig. 6.8(b). Hence, the variance was improved by a factor of 4.7, very close to the theoretical improvement of 5.

A second metric, signal amplitude, was extracted from the same data set just obtain. Figure 6.9(a) demonstrated the signal RMS amplitude measured from one ADC. Figure 6.9(b) reveals the results after averaging the signal amplitudes from the five ADCs. In this case, the variance was improved by a factor of 4.8.

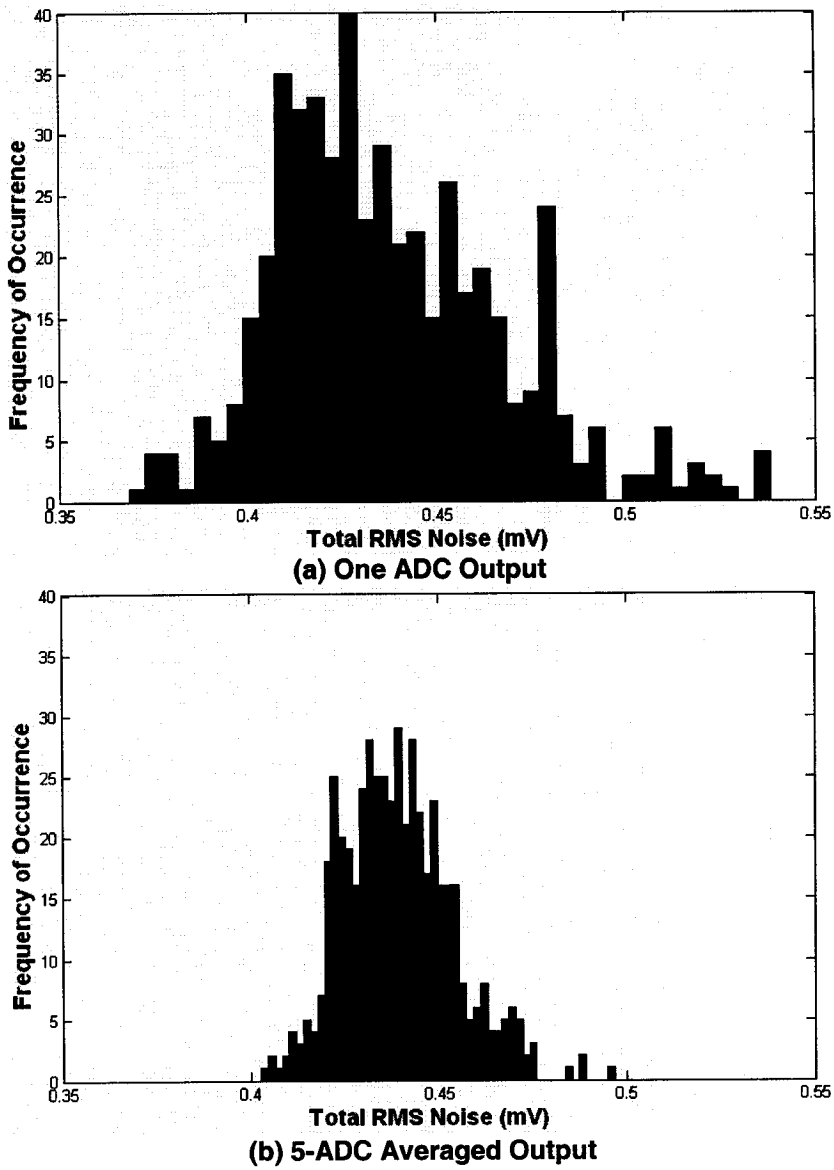
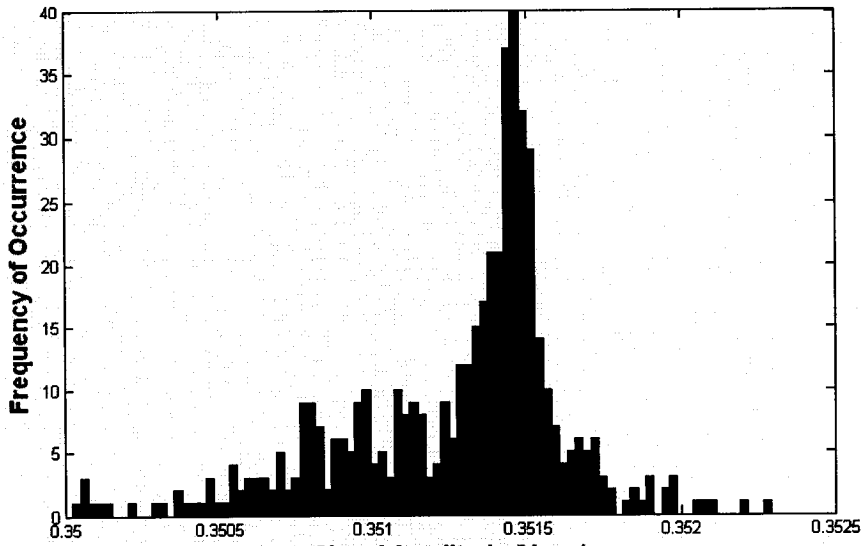
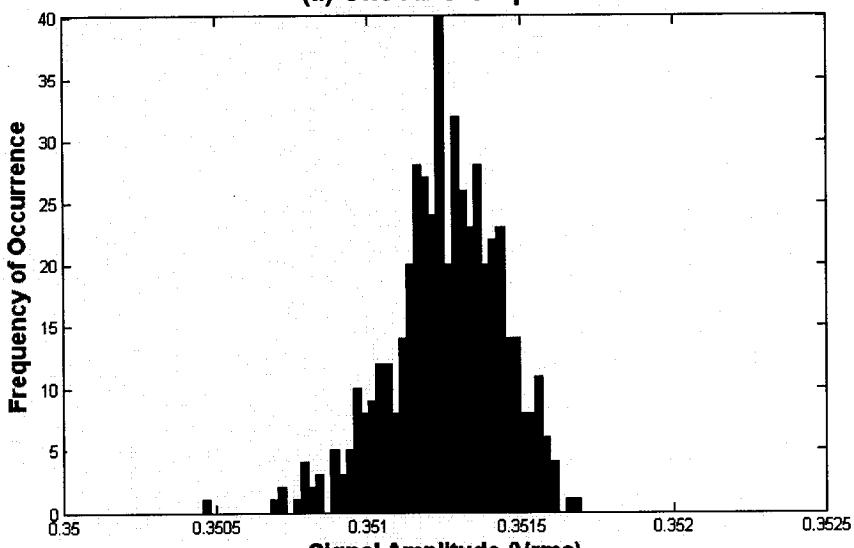



**Figure 6.8: Total Noise Power Measurement Using Quintuple-Channel Time-Interleaved ADC Approach**




(a) One ADC Output




(b) 5-ADC Averaged Output

**Figure 6.9: Signal Amplitude Measurement Using a Quintuple-Channel Time-Interleaved ADC Approach**

## 6.6 - *Time-Interleaved Multi-Digitizer Test Core*

In Chapter 4, additional applications of the proposed digitizer were presented. One of these applications was the ability to increase ADC sampling frequency by collectively capturing the multiple ADC data in a time-interleaved manner. It was also mentioned that time-interleaving may produce spurious tones and added noise due to the mismatch between ADCs.

Hence, the throughput of the quintuple-channel test core digitizer may be increased by a factor of five by time-interleaving the data capture. More interestingly, the multipass method inherently offers the ability to average out all mismatch effects between digitizers.

A single-comparator multipass A-to-D conversion would distribute the comparator's DC offset, gain, and non-linear distortion to all points in a single pass of the DC reference, and for all DC reference passes.

A time-interleaved multi-comparator multipass A-to-D conversion would distribute its mismatch error to every alternate point in a single pass. If a particular comparator is used to capture the same point for every DC reference level, then the mismatch will produce spurious tones and added noise. However, if different comparators are used to capture the same point for every DC reference level, then the mismatch will be distributed over all points. Hence, the mismatch is effectively averaged out.

Simulation results validating this argument are displayed in Figure 6.10. The quintuple-digitizer circuit was used to capture a 160 KHz input signal while sampling at 10 MHz. Using the same comparator to capture the same waveform point for all DC reference levels resulted in Figure 6.10(a). On the other hand, when different comparators were used to capture the same waveform point for all

DC reference levels, then Figure 6.10(b) was obtained. The dynamic performance results of Figure 6.10 are presented in Table 6.2.

It is obvious from Figure 6.10 that many spurious tones were reduced. In this example, nearly 3 dB of improved performance is achieved by rotating the comparators in the multipass method. These effect are similar the randomized time-interleaving approach proposed in [13].

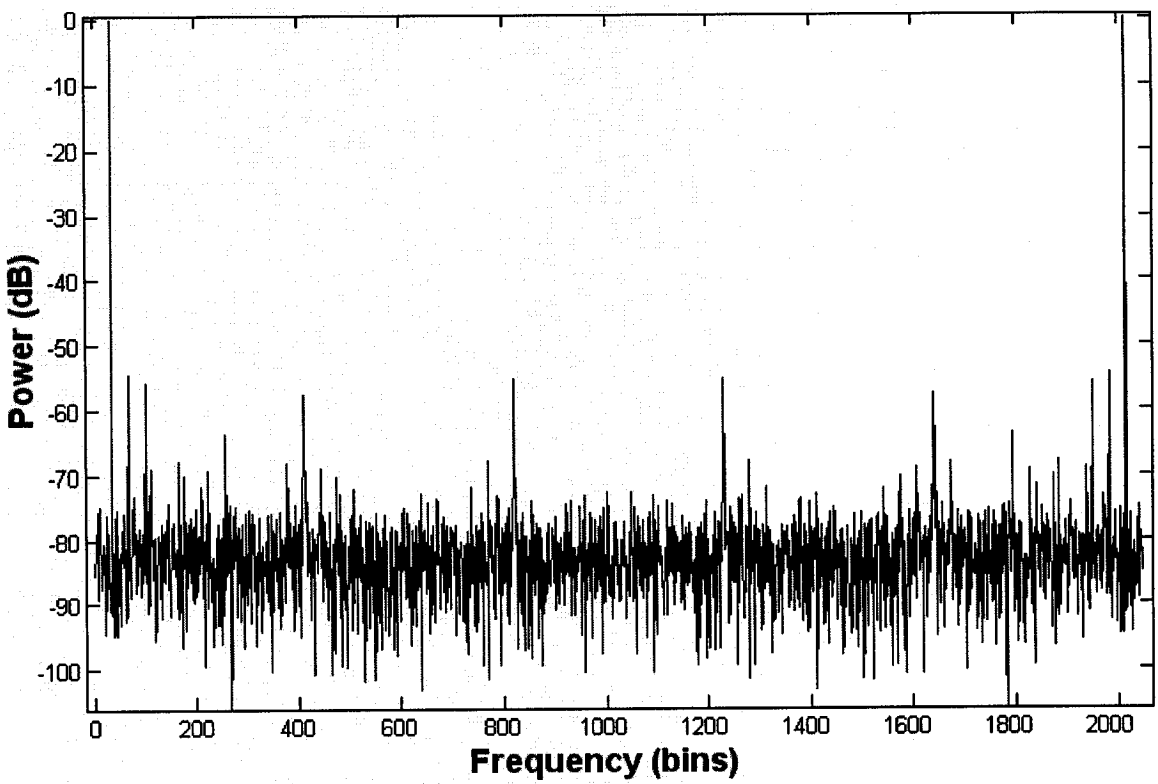
**Table 6.2: Comparison of Figure 6.10 (a) and (b) Dynamic Performance Results**

| | Figure 6.10(a) | Figure 6.10(b) |
|---|---|---|
| **SNR** | 48.0 dB | 51.1 dB |
| **SNDR** | 46.5 dB | 48.0 dB |

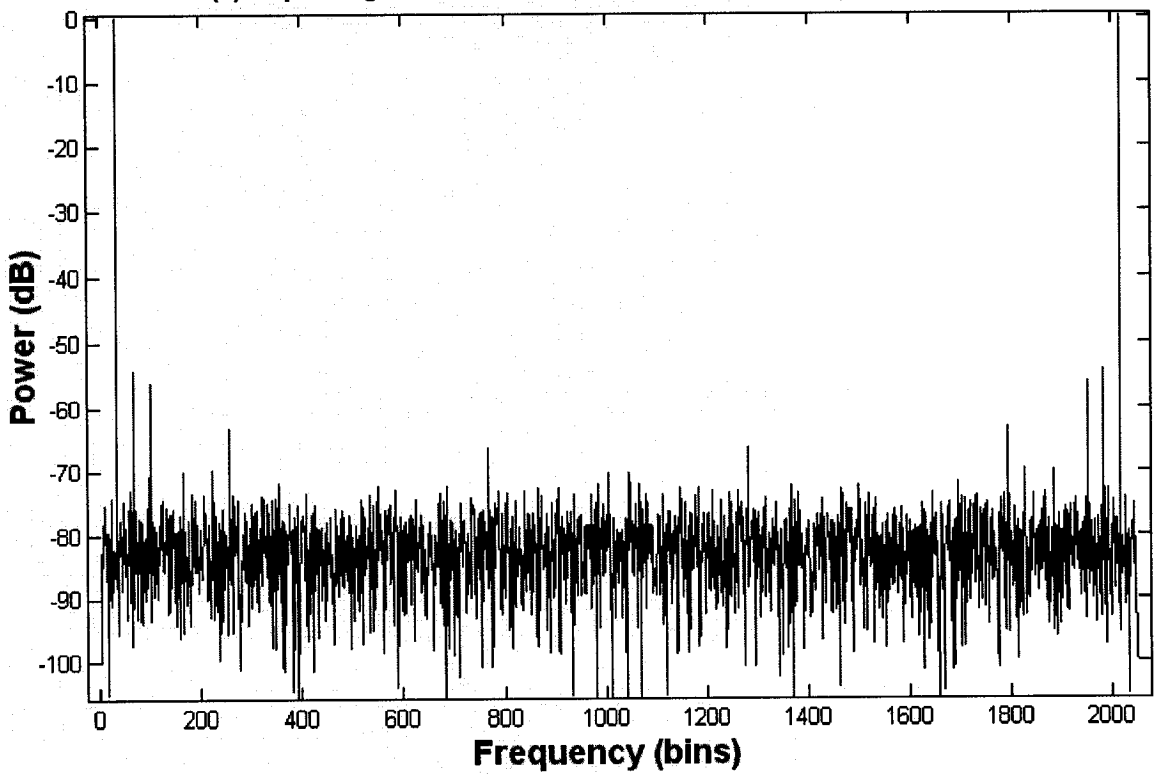
## *6.7 - Summary*

Two novel mixed-signal integrated test core topologies were implemented in TSMC's 0.18 μm technology. The first architecture was a simultaneously-sampling dual-digitizer. The second design was a quintuple-channel time-interleaved digitizer. The single digitizer, which is the building block for both designs, was characterized.

It has been demonstrated that the precision of a repeated measurement may be increased by using multiple digitizers in a time-interleaved manner. It was also demonstrated that the bias error in noise measurements may be removed using a simultaneously-sampling dual-ADC approach.




**(a) Repeating the Same Comparator to Capture Each Point**




**(b) Rotating Different Comparators to Capture Each Point**

**Figure 6.10: PSD for a Time-Interleaved Quintuple-ADC Capture for two Methods of Data Collection**

# Chapter 7: Conclusion

## *7.1 - Thesis Summary*

Mixed-signal integrated circuit production testing is crucial for the electronics industry in order to maintain the high-quality products that customers expect. Production test limits that dictate the acceptance or failure of every device under test are set with regards to measurement uncertainty. Test limits are greatly inflated by guardbands to insure that bad parts do not get passed. These guardband are increased when test equipment measurement uncertainty is increased.

This thesis presented a new digitizer architecture that will reduce measurement uncertainty of a DUT and the measurement uncertainty of the test equipment in a DSP-based test environment. The proposed digitizer offers the ability to remove measurement bias caused by noise. Furthermore, improvements to measurement repeatability are also observed.

In Chapter 2 the concepts of measurement uncertainty was introduced by first discussing the types of FFT-based measurements and their probability distribution behavior in the present of DUT noise and in the absence of test equipment noise. The practical case where test equipment noise contributes to

the measurement uncertainty was also presented and two error mechanisms, bias error and precision error, were suggested.

A new multi-digitizer architecture was proposed in Chapter 3 that boasts the ability to reduce measurement uncertainty. A simultaneously-sampling algorithm revealed that the bias error in a measurement due to test equipment noise could be removed. Furthermore, a time-interleaved sampling approach was recognized as a means to reduce precision errors. These architectures and post-processing techniques were validated using MATLAB simulations.

Two multi-digitizer mixed-signal test cores were designed and fabricated to provide experimental proof of the concepts presented. The first design was a simultaneously-sampling dual-digitizer used to validate the bias removal technique. The second design was a time-interleaved quintuple-digitizer used to demonstrate the reduction in noise variance. Chapter 4 introduced the test core and documented the fabricated designs. Post extracted simulations were also provided to justify the design choices.

Jitter-induced noise in sampled-channel measurements is severely crippling. A specific application of jitter removal in the SNR measurements of sampled-channel devices was demonstrated in Chapter 5. It was shown that the jitter-free performance of a DAC or ADC in the presence of jitter-induced noise may be accurately observed.

Finally, the experimental setup and results were demonstrated in Chapter 6. The single digitizer test core was characterized. It was shown that the simultaneously-sampling dual-digitizer successfully removed bias errors from the calculation of total RMS noise. The time-interleaved process of noise reduction was also confirmed using the interleaved quintuple-digitizer.

## *7.2 - Future Works*

Several assumptions were made throughout the measurement uncertainty modeling and analysis. Firstly, the gains of the DAC and ADC in the path of a DSP-based test system were assumed to have a constant gain or one that may be calibrated in the bandwidth of interest. Further analysis to the impact of non-zero frequency dependent gain is of interest. Furthermore, any mismatch between the multiple-ADCs could also impact the results and should be investigated. The noise between multiple-ADCs was assumed to be uncorrelated. This too may undesirably alter the results.

The proposed technique is a mathematical method to reduce the spread or variance of a repeated measurement. It was recognized that this approach may also be applied in timing measurements. Further exploration in this area is forthcoming.

# References


[1] R.H. Walden, "Analog-to-Digital Converter Survey and Analysis", *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, April 1999.

[2] M. Burns, "Test in Mixed Signal SOCs", *International Test Conference*, pp. 1132, 1998.

[3] M. d'Arbreu, "Noise – Its Sources, and Impact on Design and Test of Mixed Signal Circuits", *IEEE International Workshop on Electronic Design, Test and Applications*, 2002.

[4] R. Dorsch, R.H. Rivera, H-J. Wunderlich, and M. Fischer, "Adapting an SoC to ATE Concurrent Test Capabilities", *International Test Conference*, pp. 1169, 2002.

[5] M.M. Hafed, N, Abaskharoun, and G.W. Roberts, "A Stand-Alone Integrated Test Core for Time and Frequency Domain Measurements", *International Test Conference*, pp. 1190-1199, 2001.

[6] A. Papoulis, *Probability, Random Variables, and Stochastic Processes*, McGraw-Hill, 3rd Ed., 1991.

[7] M. Burns and G.W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, Oxford Press, 2001.

[8] N. Kurosawa et al., "Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems", *IEEE Transaction on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 48, no. 3, pp. 261-271, March 2001.

[9] Y. Langard, J-L. Balat and J. Durant, "An Improved Method of ADC Jitter Measurement", *International Test Conference*, 1994.

[10] P. Cauvet and L. Hamonou, "An Improving the Dynamic Measurements of ADC's using the 2-ADC Method", *Teradyne Users Group*, 2001.

[11] J-E. Eklund, F. Gustafsson, "Digital Offset Compensation of Time-Interleaved ADC using Random Chopper Sampling", *IEEE International Symposium on Circuits and Systems*, pp. 447-450, 2000.

[12] M.K. Rudberg, "Calibration of Mismatch in Time Interleaved ADCs", *The 8th IEEE International Conference on Electronics, Circuits and Systems*, pp. 845-848, 2001.

[13] M. Tamba, A. Shimizu, H. Munakata, and T. Komuro, "A Method to Improve SFDR with Random Interleaved Sampling Method", *International Test Conference*, pp. 512-520, 2001.

[14] A. Hajjar and G.W. Roberts, "A High Speed and Area Efficient On-Chip Analog Waveform Extractor", *International Test Conference*, pp. 688 -697, 1998.

[15] A. Hajjar and G.W. Roberts, "A Multi-Pass A/D Conversion Technique for Extracting On-Chip Analog Signals", *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 280 -283, 1998.

[16] B. Dufort and G.W. Roberts, "On-Chip Analog Signal Generation for Mixed-Signal Built-In Self-Test", *IEEE Journal of Solid State Circuits*, vol. 34, no. 3, pp. 318 -330 March 1999.

[17] M.M. Hafed, S. Laberge, and G.W. Roberts, "A Robust Deep Submicron Programmable DC Voltage Generator", *IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 5 -8, 2000.

[18] D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, pp. 312, 1997.

[19] T. Shih, L. Der, S.H. Lewis, and P.J. Hurst, "A Fully Differential Comparator Using a Switched-Capacitor Differential Circuit with a Common-Mode Rejection", *IEEE Journal of Solid State Circuits*, vol. 32, no. 2, February 1997.

[20] B. Razavi, "Design Techniques or High-Speed, High-Resolution Comparators", *IEEE Journal of Solid State Circuits*, vol. 27, no. 12, December 1992.

[21] B. Song, H.S. Lee, and M. Tompsett, "A 10-b 15-MHz Recycling Two-Step A/D Converter", *IEEE Journal of Solid State Circuits*, vol. 25, no. 6, pp. 1328-1338, 1990.