Low-Power High-Speed High-Resolution Delta-Sigma Modulators for Digital TV Receivers in nanometer CMOS

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Abstract

The continuing advance in portable digital communication services is fuelling interest in analog-to-digital converters (ADCs) with high speed and high resolution. Moreover, the use of high-speed high-resolution ADCs allows part of the signal processing to be done in the digital domain allowing for higher system integration and cheaper fabrication. Becoming more in use, hand-held devices have low-power requirements to allow for longer battery life. Furthermore, designing ADCs in nanometer digital CMOS technologies make them more integrable with digital processing blocks and cheaper.

This thesis aims at designing a high-speed (16MS/s conversion rate) high-resolution ($\approx$12bits) $\Delta\Sigma$ modulator with low-power consumption in nanometer digital CMOS. $\Delta\Sigma$ modulators can achieve a high resolution in low and medium speed applications. For higher speed applications, the oversampling ratio (OSR) will have to be kept low to avoid power-inefficient design. However, lowering the OSR requires special care in the design starting from the architecture until the full circuit implementation. In nanometer CMOS technologies, analog properties, such as intrinsic gain, degrade which might result in a higher power consumption. Moreover, the low nominal supply voltages associated with such technologies adds more challenges to the design of a low distortion power-efficient $\Delta\Sigma$ modulator. Targeting a specific resolution, lowering the voltage supply usually results in a higher power consumption. This thesis suggests possible solutions to achieve low power consumption while targeting high-speed applications in nanometer low-voltage-supply environment.

This thesis presents a low-power Discrete-Time (DT) $\Delta\Sigma$ modulator making use of a single-loop multibit DT digital input-feedforward $\Delta\Sigma$ architecture. The main feature of this architecture is the reduced signal swings at the output of the integrators which allows the use of a low voltage supply. The low-power Switched-Capacitor (SC) implementation is ensured by using a novel opamp switching technique, optimizing simultaneous opamp's settling in cascaded nondelaying SC integrators, and using non-overlapping clock phases with unequal duty-cycles. The novel opamp switching technique is based on a current-mirror opamp with

switchable transconductances. The current-mirror opamp works with full current during the charge-transfer phase while the output current is partially switched during the sampling phase. Power saving can be achieved while ensuring that the opamp output is available during both phases. The simultaneous settling of series opamps in a two cascaded nondelaying SC integrators scheme is looked at as a two-pole system where power optimization is necessary to ensure minimum power consumption while meeting the settling requirements. The use of clock phases with unequal duty-cycles gives the designer an extra degree of freedom to further power optimize the design.

The experimental $\Delta\Sigma$ ADC is a 4^{th}-order 5.5bits single-loop $\Delta\Sigma$ modulator with an OSR of 8. The design starts with the structural-level aspects in which system-level decisions are made and simulations are carried-out with behavioral models to find the suitable circuit parameters. Circuit-level design in then considered to design each block and simulate the full-system. Fabricated in 1V 65nm CMOS, the $\Delta\Sigma$ modulator prototype occupies an active area of 1.2mm^2. Although the targeted resolution is about 12bits, the experimental results shows a dynamic range (DR) of 66dB ($\approx$11bits) over an 8MHz bandwidth while consuming 26mW and a peak SNR/SNDR of 64/58.5dB. The proposed opamp switching technique brings the total power consumption from 29mW to 26mW without affecting the performance (SNDR stays at 58.5dB). The deviation in experimental performance, from simulations, in thought to be due to higher parasitic capacitance requiring higher bias currents which results in drop of opamp dc gain. Compared to state of the art high-speed high-resolution $\Delta\Sigma$ modulators operated from 1V supply and fabricated in CMOS, it achieves a reasonable Figure-of-Merit.

Résumé

La progression des services de communication numériques portables augmente l'intérêt dans les convertisseurs analogique-numérique (CAN) à haute vitesse et à haute résolution. En outre, l'utilisation de CAN à haute vitesse et à haute résolution permet à une partie du traitement du signal d'être accompli dans le domaine numérique permettant une meilleure intégration du système et un cout de fabrication moins élevé. De plus en plus utilisés, les appareils portatifs ont des exigences de faible consommation pour permettre une plus longue durée de vie de batterie. En plus, la conception CAN en technologies CMOS numériques les rendent plus intégrable avec les blocs de traitement numérique et les rendent moins cher.

Cette thèse vise à concevoir un modulateur $\Delta\Sigma$ à haute vitesse (taux de conversion de 16MS/s) et à haute résolution ($\approx$12bits) et aussi à faible consommation d'énergie tout en étant fabriqué en technologie CMOS nanomètrique. Les modulateurs $\Delta\Sigma$ peuvent atteindre une résolution élevée dans les applications de basse et de moyenne vitesse. Pour les applications plus rapides, le taux de suréchantillonnage devra être maintenu bas pour éviter une conception inefficace. Toutefois, la réduction du taux de suréchantillonnage nécessite un soin particulier à la conception depuis l'architecture jusqu'à la mise en œuvre complète du circuit. Dans les technologies CMOS nanométriques, les propriétés analogiques, telles que le gain intrinsèque, se dégradent ce qui pourrait se traduire à une consommation d'énergie plus élevée. En outre, les tensions d'alimentation nominales basses associées à ces technologies ajoutent de nouveaux défis à la conception d'un modulateur $\Delta\Sigma$ à distorsion faible et consommation faible. Pour une résolution spécifique, l'abaissement de la tension d'alimentation se traduit généralement à une consommation plus élevée. Cette thèse suggère des solutions possibles pour atteindre une faible consommation tout en ciblant les applications à haute vitesse en milieu nanomètrique avec une alimentation à basse tension.

Cette thèse présente un modulateur $\Delta\Sigma$ à faible consommation utilisant une architecture multi-bits à entrée "feedforward" numérique. La principale caractéristique de cette architecture est la réduction de la dynamique de signal à la sortie des intégrateurs, ce qui permet

l'utilisation d'une alimentation à basse tension. La mise en œuvre du circuit à condensateurs commutés (SC) à faible consommation est assurée par l'utilisation d'une nouvelle technique de commutation pour l'amplificateur opérationnel (opamp), l'optimisation de la stabilisation simultanée des intégrateurs SC sans délais en cascade, et l'utilisation des phases d'horloge à rapports cycliques inégaux. La technique nouvelle de commutation de l'opamp est basée sur un opamp à miroir de courant avec transconductances commutables. L'opamp à miroir de courant fonctionne en plein courant pendant la phase de transfert de charge tandis que le courant est partiellement commuté pendant la phase d'échantillonnage. Cette technique réduit la consommation et peut être réalisée tout en s'assurant que la sortie de l'opamp est disponible pendant les deux phases. La stabilisation simultanée des opamps en série dans le cas de deux intégrateurs SC sans délais en cascade est traitée comme un système à deuxième ordre où l'optimisation de puissance est nécessaire pour assurer une consommation minimale tout en répondant aux exigences de stabilisation. L'utilisation de phases d'horloge avec rapports cycliques inégaux donne au concepteur un degré de liberté supplémentaire pour optimiser la consommation de la conception.

Le modulateur expérimental de cette thèse est un modulateur $\Delta\Sigma$ de 4^{e} ordre avec 5.5bits et un taux de suréchantillonnage égal à 8. La conception commence avec les aspects structurels dans lequel des décisions au niveau du système sont prises et des simulations sont rapportées sur des modèles comportementaux pour trouver les paramètres de circuit appropriés. La conception au niveau circuit est examinée pour concevoir chaque bloc et simuler l'ensemble du système. Fabriquée en 65nm CMOS à 1V, ce prototype occupe une surface active de 1,2 mm^2. Bien que la résolution ciblée est de 12bits, les résultats expérimentaux montrent une gamme dynamique (DR) de 66dB ($\approx$ 11bits) sur une bande de 8MHz tandis que la consommation est de 26mW et le SNR/SNDR maximal est 64/58.5dB. L'écart de performance semble être dû à l'augmentation des condensateurs parasites nécessitant des courants plus élevés, ce qui entraîne la chute de gain de l'opamp. Par rapport aux modulateurs $\Delta\Sigma$ à haute vitesse et à haute résolution des travaux de pointe opérés à partir d'1V et fabriqués en technologies CMOS, le prototype réalise une figure-de-mérite raisonnable.

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I would like to dedicate this work to the memory of Mohamed El Shanawany, victim of oppression, and to the memory of all victims of oppression all over the world.

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List of Acronyms and Abbreviations

ADC	analog-to-digital converter
AFF	analog-feedforward
BW	bandwidth
CMFB	common-mode feedback
CMOS	complementary metal-oxide-semiconductor
CT	continuous-time
DAC	digital-to-analog converter
DEM	dynamic element matching
DFF	digital-feedforward
DS	double sampling
$\Delta\Sigma$	delta-sigma
DT	discrete-time
DR	dynamic range
DWA	data weighted averaging
FIR	finite impulse response
FoM	figure of merit
IFF	input-feedforward
LSB	least significant bit
NTF	noise transfer function
OSR	oversampling ratio
PCB	printed circuit board
PSD	power spectral density
PSO	partially switched-opamp
SO	switched-opamp
SC	switched-capacitor
SNDR	signal-to-noise-and-distortion ratio
SNR	signal-to-noise- ratio
SQNR	signal-to-quantization-noise ratio
SR	slew rate
STF	signal transfer function

Chapter 1

Introduction

The proliferation of broadband digital communications is stimulating the research towards high-speed (few to tens MS/s conversion rate) analog-to-digital converters (ADCs). Examples of broadband digital communication applications include digital TV such as DVB-T (4MHz), DMB-T (4MHz), ISDB-T (3-4MHz) and LTE standards (5-10-20MHz). The software-defined radio concept is encouraging the transfer of some analog processing to the digital domain for more programmability. This requires high-resolution (10 bits and more of dynamic range) ADCs. The ADCs provide the interface between the digital processing and the analog receiver front-end.

1.1 Motivation

With the current advance in digital mobile applications many digital TV services have been adopted in mobile services such as DVB-H (4MHz), DMB-H (4MHz). The ADCs used in these digital TV receivers for hand-held devices have low-power requirements (few mW to tens of mW) to allow for longer battery lifetimes.

The design of ADCs in modern nanometer digital CMOS processes (such as 65nm CMOS) allows higher system-integration with digital circuitry and lower fabrication cost. This comes at the expense of poor analog properties, such as intrinsic gain, and low supply voltages in such processes.

Although the shrinkage of supply voltage has a desirable effect on power consumption in digital circuits, it is not the case in the analog domain. To explain the idea, let us consider a

Discrete-Time (DT) Delta-Sigma ($\Delta\Sigma$) modulator with switched-capacitor (SC) implementation with some targeted signal-to-noise-ratio (SNR). The direct effect of supply shrinkage is the lower signal swing which limits the maximum input signal allowed in the system. To meet the targeted SNR, and assuming kT/C thermal noise domination in the $\Delta\Sigma$ modulator, the sampling capacitor (C) has to be increased to bring the thermal noise down. This, in turn, requires more opamp bandwidth, and hence, more opamp bias current. It can be shown, quantitatively, that lowering the supply voltage results, in this case, in the increase of power consumption to maintain the same SNR [Ham04a]. Another result of lowering the supply voltage in SC circuits is the limited overdrive voltage for the MOS switches since the NMOS and PMOS threshold voltage shrinkage is less than the supply voltage shrinkage. This requires additional circuitry (such as bootstrapping) to maximize signal swing and maintain a good linearity.

$\Delta\Sigma$ ADCs combine oversampling with noise shaping to achieve high resolution. They can achieve high resolution in low and medium speed applications. Recent research has shown interest in extending the $\Delta\Sigma$ signal bandwidth for high-speed applications while maintaining low power consumption in low-voltage-supply nanometer CMOS processes.

1.2 High-Speed High-resolution $\Delta\Sigma$ ADCs

A wide range of high-speed high-resolution $\Delta\Sigma$ ADCs can be found in the literature. Table 1.1 lists state-of-the-art $\Delta\Sigma$ ADCs with signal bandwidth $\geq$ 2MHz and dynamic range (or SNR) $\geq$ 62dB (10bits). The survey focuses on $\Delta\Sigma$ modulators fabricated in modern CMOS and operated from a power supply $\leq$ 1.2V. It was last updated in April 2013.

The table shows the signal bandwidth (f_{BW}) and the sampling frequency (f_S). The performance metrics used for comparison are the dynamic range (DR), the signal-to-noise ratio (SNR), and the signal-to-noise-and-distortion ratio (SNDR) (all defined in the next chapter). The power consumption is also listed as well as the supply voltage (V_{DD}). The table also lists the CMOS processes in which the $\Delta\Sigma$ ADCs were fabricated and the area it occupies. The architecture used for the $\Delta\Sigma$ modulator is shown and the implementation, Continuous-Time (CT) or Discrete-Time (DT), is also listed.

Table 1.1: High-speed (f_{BW} $\geq$ 2MHz) high-resolution (DR or SNR $\geq$ 62dB (10bits)) state-of-the-art CMOS $\Delta\Sigma$ ADCs operated from power supplies V_{DD} $\leq$1.2V (last updated in April 2013).

Reference	f_{BW} (MHz)	f_S (MHz)	DR (dB)	SNR (dB)	SNDR (dB)	Power (mW)	V_{DD} (V)	CMOS Process	Area (mm^2)	Input DT/CT	Architecture order(bit)
Potential	8	128	80	78	74	20	1	65nm		DT	4(5.5b)
[Ke10]	2	128	75		72	3.6	1	90nm	0.4	CT	4(2b)
	4	192	72		69	4.9					
[Pre11]	20	640	63	63	61	7	1	65nm	0.08	CT	3(1b)
[Mat10b]	4	140		70.2	69.8	3.6	1	65nm	0.09	CT	3(3b)
[Car11]	5	400	71		69	28	1.05	32nm	0.13	CT	DI MASH
	10		68		65						
	20		66		63						
[Mat10a]	10	300	70.2	68.2	62.5	5.32	1.1	110nm	0.32	CT	5(3b)
[Kwo09]	3.125	100	68	65	64	11	A:1.1 D:1.2	65nm	0.6	CT/DT Hybrid	3(4b)
	5	160	67	63	61						
[Mor10]	2	120	66		63.3	8	1.2	90nm	0.66	DT	2(1.5b)-2(1.5b)
	4		62		59.1						
[Hua09]	2	128	80	79.1	79.07	4.52	1.2	65nm	0.084	CT	3(3b)
[Yam12]	2.5	40	71.3		70.4	3.73	1.2	65nm	0.43	DT	4 x 1(2b)
[Mal08]	2.5	420		78		12.1	1.2	90nm	1	DT	2(4b)
	5			77		15.7					2(4b)-0(3b)
	10			75		20.3					2(4b)-1(3b)
	20			67	64	20.3					2(4b)-1(3b)
	20			72	70	27.9					2(4b)-2(3b)
[Cro10]	4	512	72		70	5.5	1.2	90nm	0.4	CT	3(1b)
	10	640	67		65	6.8					
[Oh12]	5	80	71.6	71	70.7	8.1	1.2	90nm	0.37	DT	2(5b)
[Chr10]	5	160	75.4	72.2	70.9	13.6	1.2	130nm	0.27	DT	3(1.5b)
	10	240	71	68.7	66	20.2					3(3.5b)
	20	400	70.4	66.9	64.4	34.7					3(3.5b)
[Ran11]	5	160	76	74.5	69.5	6	1.2	130nm	0.56	CT	3(4b)
[And12]	9	288	72	71	69	7.5	1.2	65nm	0.08	CT	3(3b)
[Kim09]	10	250	71	68	65	18	1.2	130nm	1.35	CT	3(3.5b)
[Str08]	10	950		86	72	40	1.2	130nm	1.7	CT	3(5b)
[Jo10]	20	640	68	67.9	63.9	58	1.2	130nm	1.17	CT	3(4b)
[Mit06]	20	640	80	76	74	20	1.2	130nm	8.6	CT	3(4b)
[Bos10]	2	80	66		65	6.83	1.2	90nm	0.076	DT	2(1.5b)-1(1.5b)
[Kau11]	25	500	70	64.5	63.5	8	1.2	90nm		CT	3(4b)
[Wit12]	25	500	72	69.1	67.5	8.5	1.2	90nm	1.7	CT	2(4b)
[She12]	25	3600	86	80.2	73.3	15	1.2	90nm	0.12	CT	4(1b)
	36		83	76.4	70.9						
[Zan12]	5	130	78	75.8	75.7	16	1.2	130nm	1.6	DT	2(4b)-2(4b)

It is worth mentioning that two thirds of the $\Delta\Sigma$ modulators listed in Table 1.1 are CT $\Delta\Sigma$ modulators. Although the table does not put limits on power consumption, CT implementation is preferred over DT implementation for high-speed applications for their low-power advantage (explained in details in Section 2.2). Figure 1.1 shows the distribution of the $\Delta\Sigma$ modulators listed in Table 1.1 over f_{BW} and DR_{bits} variations, where DR_{bits} is given by $DR_{bits} = (DR - 1.76)/6.02$ in bits. Figure 1.2 depicts the distribution of the $\Delta\Sigma$ modulators listed in Table 1.1 over f_{BW} and Figure-of-Merit (FoM) variations, where FoM is given by FoM $= Power/(2f_{BW} \times 2^{DR_{bits}})$ in (pJ/step).

1.3 Thesis Scope and Research Goals

The goal of this thesis is the design of a high-speed (8MHz bandwidth, 16MS/s conversion rate) $\Delta\Sigma$ ADC suitable for Digital TV receivers. A high resolution ($\geq$ 12bits) is targeted to allow part of the analog processing to be done in the digital domain. The implementation of this $\Delta\Sigma$ ADC is meant to be in 65nm digital CMOS process for high system-integration and low cost. The design will assume a single low-voltage supply, 1V for this process, which will increase the power consumption as was explained earlier. The DT implementation, for the advantages listed in Section 2.2, is chosen for the scope of this thesis. Targeting 8MHz bandwidth, the DT implementation adds more challenge to the power consumption. The main challenge of this thesis will be the power consumption. The low power consumption will be achieved by means of:

1. Exploring low-power SC integrator techniques and proposing a novel opamp switching technique based on a current-mirror opamp with switchable transconductances. The proposed current-mirror opamp works with full current during the charge-transfer phase while the output current is partially switched during the sampling phase. Power saving can be achieved while ensuring that the opamp output is available during both phases.

2. Investigating the simultaneous settling of series opamps in a two cascaded nondelaying SC integrators scheme, and developing a power optimization procedure to ensure minimum power consumption while meeting the settling requirements.

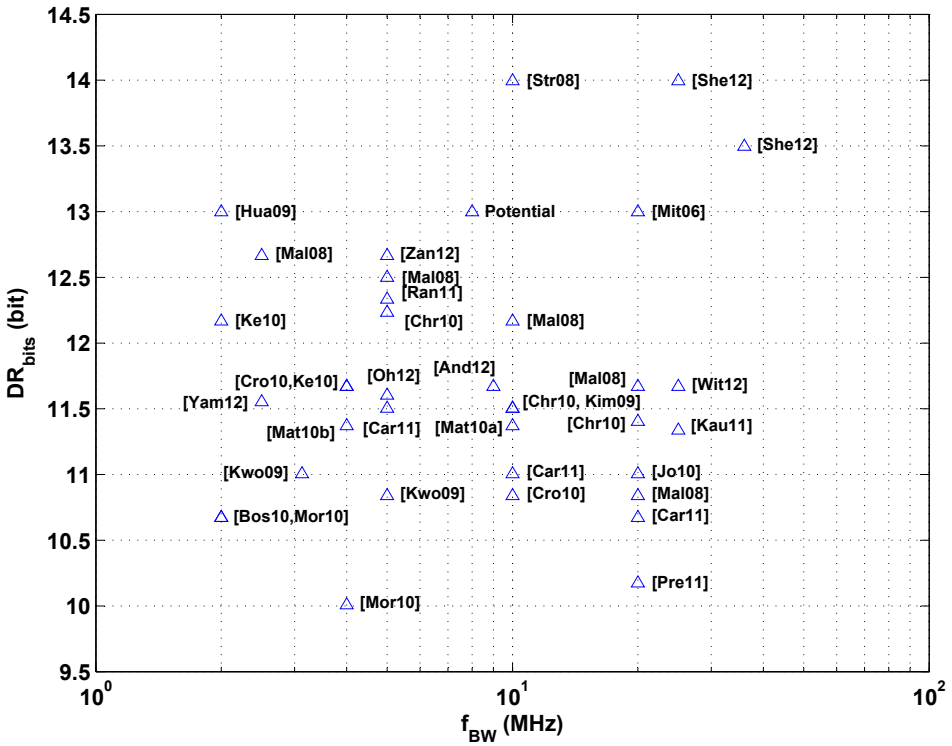


Figure 1.1: Distribution of the $\Delta\Sigma$ modulators listed in Table 1.1 over f_{BW} and DR_{bits} variations.

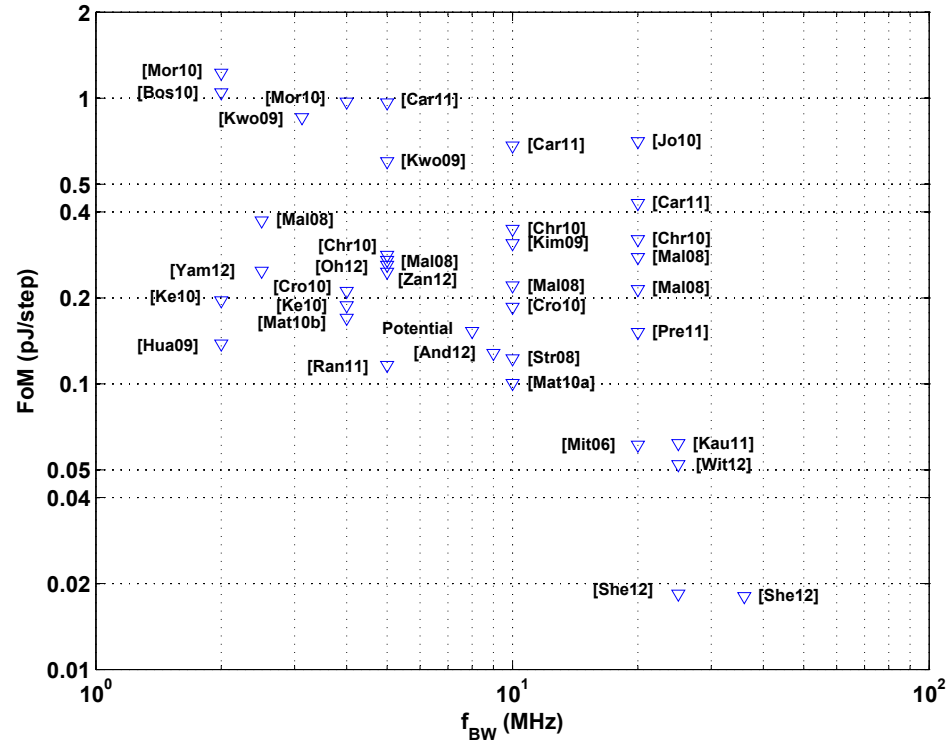


Figure 1.2: Distribution of the $\Delta\Sigma$ modulators listed in Table 1.1 over f_{BW} and FoM variations.

3. Examining the possible use of non-overlapping clock phases with unequal duty-cycles (rather than both about 50 %) which would give the designer an extra degree of freedom to further power optimize the design.

The potential performance thought to be achievable by the experimental $\Delta\Sigma$ modulator in this thesis is listed in the first row of Table 1.1. The power consumption is expected to be about 20mW from behavioral and circuit simulations. The potential performance is also depicted in both Figure 1.1 and Figure 1.2.

1.4 Thesis Outline

This dissertation is organized in eight chapters including the introduction. The thesis outline is as follows:

Chapter 2 explores low-power techniques suitable for efficient discrete-time (DT) $\Delta\Sigma$ modulators design on different levels. On the SC implementation level, some low-power SC integrator circuit techniques are explored, outlining the various advantages and disadvantages of each technique. On the system-level, various low-power DT $\Delta\Sigma$ architectures are listed with the different aspects related to each architecture. Finally, the feedback timing issue is focused on, along with previously suggested solutions.

Chapter 3 introduces a novel switchable-opamp for the low-power design of SC integrators as part of the low-power DT $\Delta\Sigma$ modulator design. It is based on a current-mirror opamp with output transconductances that can be switched off during the sampling phase . It can be used in the design of SC integrators with both *half-delay* and *full-delay*. Furthermore, since its input transconductance is on at all times, it doesn't suffer from operation-speed limitations found in previous designs. Simulation results are presented and confirm that power reductions of up to 30% can be achieved in SC integrators by using the proposed switchable-opamp, compared to having the current-mirror opamp fully active at all times.

Chapter 4 focuses on the design of two nondelaying cascaded SC integrators as part of the low-power design of DT $\Delta\Sigma$ modulators. A design method is proposed which optimizes the power consumption for a given settling accuracy. Another issue is also addressed concerning a

possible excitation case that might lead to settling "hesitation" in two nondelaying cascaded SC integrators which affects settling accuracy. Finally, circuit simulations are presented to confirm the analytical methods and simulations.

Chapter 5 presents a design procedure for the system-level design of the experimental $\Delta\Sigma$ modulator, starting from choosing an architecture, until deciding on various circuit parameters for the circuit design. Structural-level (SC implementation) aspects are addressed and structural simulations (SC) are presented. Using behavioral simulations, a Figure of Merit based design procedure is developed to find circuit parameters for an efficient $\Delta\Sigma$ modulator design.

Chapter 6 presents the design procedure of the various circuit building blocks of the experimental $\Delta\Sigma$ modulator in 1V 65nm CMOS process. The chapter presents the design of the opamps, the SC comparator, the sampling switches, and the digital circuitry. The implementation of the switchable-opamp, presented in Chapter 3, is shown in this chapter. Circuit simulations of the main building blocks are performed to verify their functionality. Full-system circuit simulations are carried out as a final verification before preparing a prototype for fabrication.

Chapter 7 explores the experimental results of a prototype built for the experimental $\Delta\Sigma$ modulator. Starting from silicon-level (in 65nm General Purpose GP Standard CMOS process) aspects, the chapter also sheds some light on the test set-up used for the experimental prototype. This chapter presents and summarizes the experimental results of the $\Delta\Sigma$ prototype and compares it with state-of-the-art $\Delta\Sigma$ modulators.

Chapter 8 summarizes the thesis, highlights the key research contributions, and suggests topics for future research.

Chapter 2

Low-Power Discrete-Time Delta-Sigma Modulators: from Integrator to Architecture

Oversampling ΔΣ modulators offer a trade-off in ADC design by achieving a high resolution using low accuracy analog components but require higher sampling rates and more digital circuits [Ham04b]. This chapter explores low-power circuit techniques suitable for efficient Discrete-Time (DT) ΔΣ modulators design as well as low-power DT ΔΣ modulator architectures.

Section 2.1 starts with a brief introduction about the fundamentals of ΔΣ modulators. Section 2.2 clarifies the reasons behind choosing the DT implementation over Continuous-Time (CT) implementation. Section 2.3 goes through various low-power switched-capacitor (SC) circuit techniques. Section 2.4 then explores different ΔΣ architectures suitable for low-power design especially in a low-voltage-supply environment. Section 2.5 addresses the feedback timing issue in the ΔΣ architectures of interest.

2.1 ΔΣ Modulation Fundamentals

This section outlines the fundamentals of the ΔΣ modulation. We start by the operation concepts in Section 2.1.1 then we summarize the main performance metrics in Section 2.1.2.

2.1.1 ΔΣ Modulation Operation Concepts

The operation of ΔΣ modulation relies on quantization, oversampling , and noise-shaping. The quantization is the main process in any Analog-to-Digital Converter (ADC) in which a signal with infinite amplitude resolution is transformed into a signal with finite amplitude resolution. The quantizer usually operates on a uniform step size (Δ) and a uniform sampling rate (f_S). A quantization error is introduced due the quantization process. Assuming uniform probability density function, the mean square of that error can be found to be $\frac{\Delta^2}{12}$. Under white noise assumption, this noise creates a uniform noise spectral density from 0 to $f_S/2$ as depicted in Figure 2.1 (a). The signal-to-quantization-noise ratio (SQNR) is defined as the ratio of the input-signal power to the quantization noise power in the signal band.

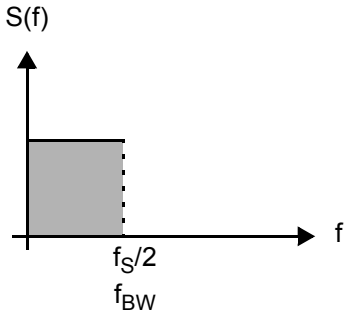
In Nyquist-rate ADCs, the sampling frequency (f_S) is set as twice the signal bandwidth (f_{BW}). In oversampling ADCs, f_S is set to a much larger value than $2f_{BW}$. We define the oversampling ratio as

$$\text{OSR} = \frac{f_S}{2f_{BW}} \tag{2.1}$$

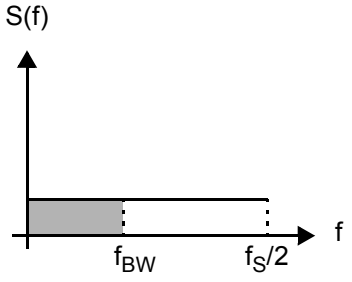
Due to oversampling, the quatization noise is spread out and the SQNR increases because the in-band quantization noise is reduced as shown in Figure 2.1 (b).

By making use of the negative feedback concept, the SQNR can be further improved. Combining oversampling and noise-shaping gives ΔΣ modulation. Figure 2.2 depicts a single-loop ΔΣ modulator. The linear model of the ΔΣ modulator is shown in Figure 2.3, where the quantization error Q(z) is assumed to be additive white noise.

We can define the noise transfer function (NTF) and the signal transfer function (STF) as



(a) Nyquist ADC.



(b) Oversampling ADC.

Figure 2.1: Power spectral density of quantization error.

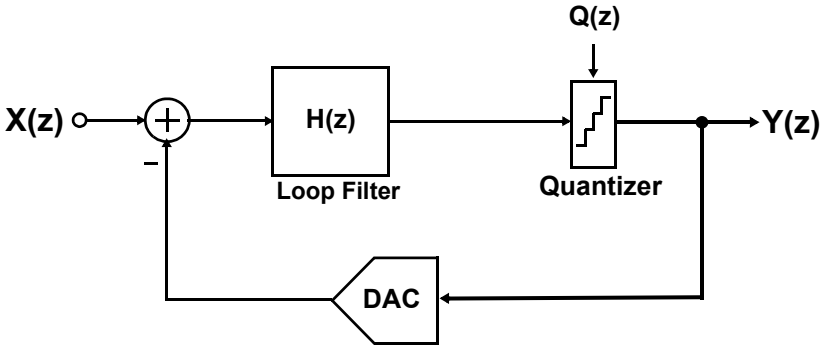


Figure 2.2: Block diagram of a single-loop ΔΣ modulator.

$$\mathrm{NTF(z)} \equiv \left.\frac{Y(z)}{Q(z)}\right|_{X(z)=0} = \frac{1}{1+H(z)} \tag{2.2}$$

$$\mathrm{STF(z)} \equiv \left.\frac{Y(z)}{X(z)}\right|_{Q(z)=0} = \frac{H(z)}{1+H(z)} \tag{2.3}$$

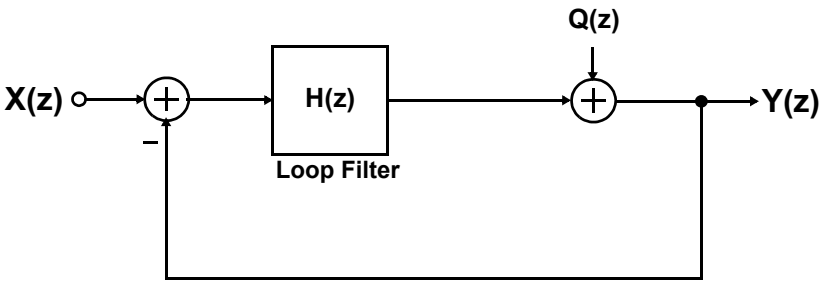


Figure 2.3: Linear model of a single-loop $\Delta\Sigma$ modulator.

The NTF shapes the quantization error and pushes the quantization error from signal band to outside the band which further increases the SQNR. The loop filter ($H(z)$) order determines the noise shaping order.

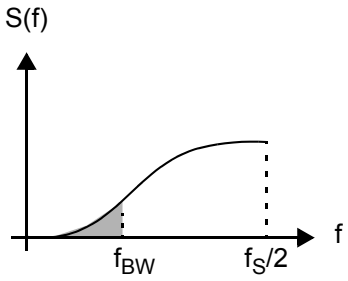


Figure 2.4: Power spectral density of quantization error in oversampling noise shaping ($\Delta\Sigma$) ADC.

2.1.2 $\Delta\Sigma$ Modulators Performance Metrics

This section lists the main performance metrics used in this thesis to evaluate the performance of the $\Delta\Sigma$ modulator.

Signal-to-Quantization-Noise Ratio

The signal-to-quantization-noise ratio (SQNR) is the ratio of the input-signal power (P_s) to the in-band quantization noise power ($P_{q,BW}$) expressed as

$$\text{SQNR} \equiv 10\log_{10}\left(\frac{P_s}{P_{q,BW}}\right) \qquad \text{(dB)} \tag{2.4}$$

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of the input-signal power (P_s) to the total in-band noise power ($P_{n,BW}$) expressed as

$$\text{SNR} \equiv 10\log_{10}\left(\frac{P_s}{P_{n,BW}}\right) \qquad \text{(dB)} \tag{2.5}$$

Signal-to-Noise-and-Distortion Ratio

The signal-to-noise-and-distortion ratio (SNDR) is the ratio of the input-signal power (P_s) to the sum of the in-band noise power ($P_{n,BW}$) and the overall distortion (caused by the ADC nonlinearity) (P_d) expressed as

$$\text{SNDR} \equiv 10\log_{10}\left(\frac{P_s}{P_{n,BW}+P_d}\right) \qquad \text{(dB)} \tag{2.6}$$

Dynamic Range

The Dynamic Range (DR) is the ratio of the maximum input-signal power ($P_{s,max}$) to the minimum input-signal power ($P_{s,min}$) expressed as

$$\text{DR} \equiv 10\log_{10}\left(\frac{P_{s,max}}{P_{s,min}}\right) \qquad \text{(dB)} \tag{2.7}$$

where ($P_{s,min}$) is the minimum input-signal corresponding to an SNR of 0dB while ($P_{s,max}$) corresponds to the input-signal power causing the SNR to drop by 3dB from its peak value.

Figure-of-Merit

The Figure-of-Merit (FoM) expression used in this thesis reflects the energy efficiency of the ADC for the reason of comparison. It can be expressed as

$$\text{FoM} = \frac{P_{total}}{2f_{BW}.2^{\frac{\text{DR}-1.76}{6.02}}} \qquad \text{(pJ/step)} \tag{2.8}$$

where P_{total} is the total power consumption of the ADC and f_{BW} is its input-signal bandwidth.

2.2 Discrete-Time vs. Continuous-Time ΔΣ Modulators

Although the first ΔΣ ADCs implementation used Continuous-Time (CT) loop filter, Discrete-Time (DT) ΔΣ modulators became more attractive, compared to their CT counterpart, for their coefficient accuracy and good linearity when implemented using SC circuits [Sch05b]. Switched-capacitor circuits are well known for their good accuracy since the coefficient accuracy depends on capacitor ratios rather than absolute time constant values in CT circuits. Consequently, CT circuits need calibration for their time-constants.

Moreover, the noise-transfer function (NTF) of a SC ΔΣ modulator scales naturally with the sampling frequency and the modulator coefficients are independent of the sampling frequency while the CT ΔΣ modulator is only designed for one unique sampling frequency and the modulator coefficients change with the sampling frequency. On the other hand, due to the settling requirements in SC circuits, the CT modulator can run at a clock frequency 2-4 times greater than its SC counterpart [Sch05b]. This makes CT designs more power-efficient for high-speed moderate-resolution applications while SC designs are more suited for moderate-speed high-resolution applications.

Targeting both high-speed and high-resolution applications we should either choose CT implementation and develop ways to improve the resolution or choose DT implementation and work on power reduction while increasing the speed. In this thesis, we will be focusing on DT ΔΣ modulators with the challenge of achieving a power-efficient design while operating at a high speed. In the following sections, we will explore how the low-power implementation of DT ΔΣ modulators can be achieved.

2.3 Low-Power Switched-Capacitor Circuit Techniques

The coefficient accuracy and adequate linearity of SC circuits make it the best way, up-to-date, for DT ΔΣ implementation [Sch05b]. The power-efficient switched-capacitor circuit implementation plays an important role in achieving a good figure-of-merit (FoM) for any DT ΔΣ modulator. SC circuits principles can be found in [Joh97]. The SC integrator (Figure 2.5) is the main building block of low-pass DT ΔΣ modulators where the signal bandwidth is centred around DC. The basic operation of a SC integrator relies on sampling the input signal

during a sampling phase (ϕ_1) on a sampling capacitor (C_S) then performing the integration, by accumulating the charge from the sampling capacitor onto another capacitor (C_F), during another phase often called the charge-transfer phase (ϕ_2). The SC integrator operation is explained in more details in Chapter 3. ϕ_1 and ϕ_2 are non-overlapping clock phases.

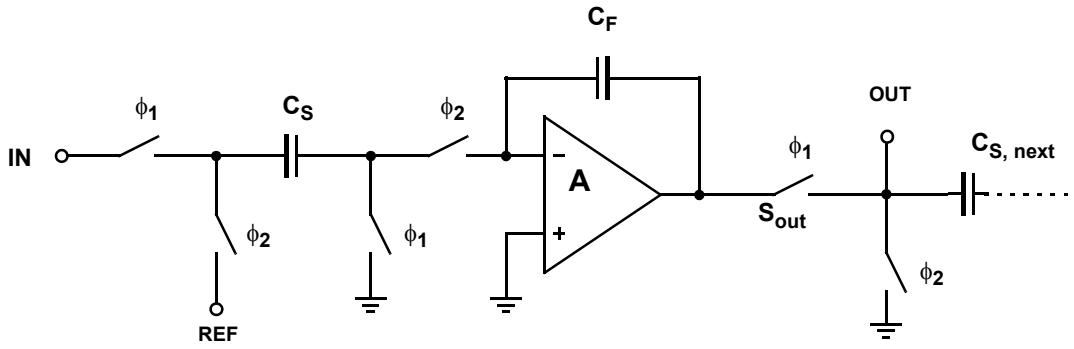


Figure 2.5: A switched-capacitor integrator with the loading effect of its next sampling stage capacitor $C_{S,next}$.

The SC integrator has been subject to a lot of innovative low-power circuit techniques to save some of the consumed power in the power-hungry opamps used to build the SC integrators (80% of power consumption of the $\Delta\Sigma$ modulator in [Nam05]). Most of these techniques look into saving or using the opamp power (current) wasted when not used during operation. Among these techniques we can mention:

1. **Double-Sampling (DS) technique [Hur90, Yan12]:**

   The Double-sampling technique in a SC integrator relies on sampling the input signal and processing it during both clock phases by means of two parallel sampling circuits (paths), to utilize the available resources (opamp) in a more efficient way [Hur90]. The effective sampling rate ends up being double the clock rate. The main disadvantage of the DS technique is the out-of-band noise folding near $f_S/2$ into the signal band due to the mismatch between the two different DS paths. One of the suggested solutions to overcome this problem is adding an extra zero at $f_S/2$ in the NTF [Rom03], but this will not necessarily maximize the SQNR that can be otherwise achieved by optimum zero placement [Sch05b]. It is important to note that none of the DT $\Delta\Sigma$ modulators listed in Table 1.1 uses the DS technique.

2. **Switched-Opamp (SO) technique [Cro94, Xu11]:**

   This technique was originally proposed as a low-voltage solution. Here, the integrator's opamp is fully switched off during the sampling phase and left on during the charge-transfer phase. The output floating switch (S_{out} in Figure 2.5) can be eliminated since the opamp output is in a high-impedance state during the sampling phase. This can improve the integrator's linearity, especially in low-voltage-supply designs.

   In terms of the power savings, this scheme can save up to 50% of the power consumption, compared to conventional designs with opamps fully active at all times [Che03]. However, this can limit the operation speed, due to the time required to turn on the opamp. Moreover, the SO method can only be employed in SC integrators with *half delay* (half a clock-cycle delay), thereby restricting their use to specific DT $\Delta\Sigma$ modulator or SC filter architectures [Pel98] (explained in details in Chapter 3). Furthermore, these opamps require special common-mode feedback (CMFB) circuits, since the opamp output is off during the sampling phase [Sin08]. None of the DT $\Delta\Sigma$ modulators listed in Table 1.1 uses the SO technique.

3. **Partially-Switched-Opamp (PSO) technique [Bas97, Che03, Kuo10]:**

   As a variant of the SO technique, a two-stage opamp is used here and only its output stage is switched off during the sampling phase. By keeping the opamp's input stage on at all times, a faster turn-on time and, hence, operation speed can be achieved, compared to a SC integrator with an SO design (explained in details in Chapter 3). Furthermore, since the input stage may burn 1/4 of the opamp's total power consumption, power reductions of 40% can be typically achieved with a PSO design [Che03]. Like the SO technique, the PSO has the same low-voltage advantage while suffering from the same disadvantages of being limited to SC integrators with *half delay* and requiring special CMFB circuitry [Pel98, Sin08]. We can notice that none of the DT $\Delta\Sigma$ modulators listed in Table 1.1 uses the PSO technique.

4. **Dynamic biasing technique [Kas99, Wan08]:**

   The dynamic biasing scheme is based on a dynamically biased amplifier to adapt the biasing current according to the required slew-rate and settling accuracy. Some of these early proposed schemes have limited signal bandwidth and large distortion [Kas99]. In [Wan08], the implementation is based on sensing the differential input signal during the sampling phase and adjusting the bias current proportionally for the charge-transfer phase. By designing a fast current detection circuit, the opamp can run at high clock rates. Combining this technique with low-distortion architectures, a good linearity could be achieved. Nonetheless, this scheme does not allow capacitor sharing between the input path (IN in Figure 2.5) and the feedback path (REF in Figure 2.5). In a typical situation, the sampling capacitor can be shared between the input signal path and the feedback path to minimize kT/C thermal noise contribution and avoid possible capacitor mismatch. Moreover, not sharing the sampling capacitor adds time constraints on the feedback path since it has to be sampled simultaneously with the input during the sampling phase. It is important to note that none of the DT ΔΣ modulators listed in Table 1.1 uses the dynamic biasing technique.

In the next chapter (Chapter 3) we will look into the proposed low-power SC circuit technique based on a current-mirror opamp with switchable transconductances. It avoids some of the drawbacks of the aforementioned techniques while saving considerable percentage of opamp power consumption. The proposed technique does not necessarily have all the previous advantages but does not have the same speed limitations found in some of the previously listed techniques.

2.4 Low-Power Discrete-Time ΔΣ Modulators Architectures

The ΔΣ modulator architecture selection is a key factor in the design of a power efficient system. In the following, we will explore some ΔΣ modulator architectures to give a justification on which architecture can be selected for the rest of the work in this thesis in a low-voltage-supply environment whilst targeting high-speed high-resolution applications.

2.4.1 Input-Feedforward (IFF) Topology

In the input-feedforward (IFF) topology [Ben93], as shown in Figure 2.6, an input-feedforward path (dashed in Figure 2.6) is added by which the input signal is summed, at the input of the quantizer, to the output of the loop filter in order to cancel any signal flowing through the loop filter, which results in low-distortion [Sil01] design due to reduced swings. The reduced swings at the output of the opamps make this topology suitable for low-voltage-supply environment.

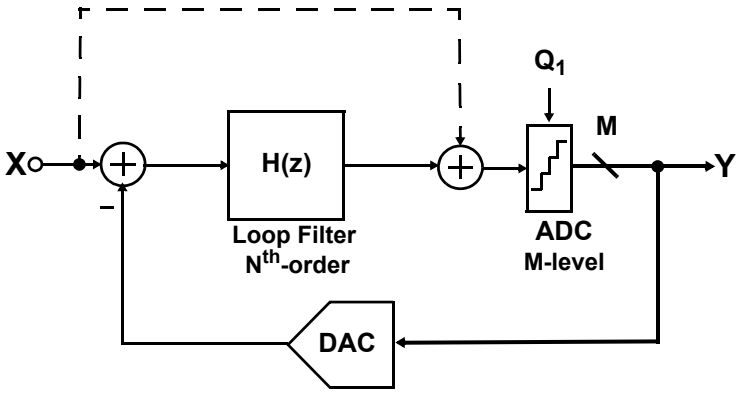


Figure 2.6: Block diagram of a single-loop $\Delta\Sigma$ modulator with a single DAC feedback and an input feedforward (IFF) path (dashed line).

Moreover, allowing the input signal to flow through the IFF path instead of the loop filter maximizes the maximum input signal and hence allows decreasing the sampling capacitor value as more kT/C noise can be tolerated (assuming thermal-noise limited design) which leads to a lower power consumption. In $\Delta\Sigma$ modulators without IFF, the quantizer reference (V_{ref}) is chosen to be equal to the available analog swing at the output of the last integrator ($V_{o,sat}$) and the maximum input signal ends up being limited by $V_{o,sat}$ in the loop filter $H(z)$. In a $\Delta\Sigma$ modulator with IFF, V_{ref} is independent of $V_{o,sat}$ which allows increasing the quantizer reference and making the maximum input signal independent of $V_{o,sat}$.

The IFF path can be implemented using either analog input-feedforward (AFF) implementation [Nam05, Fuj06], or digital input feedforward (DFF) implementation [Kwo06, Gha05, Ham08b, Gha09]. The implementation of both AFF and DFF architecture has practical challenges especially in multi-bit schemes where DAC linearization is necessary and has to be performed within the timing constraints of the architecture as will be explained in Section 2.5 in details.

2.4.2 Analog-Feedforward (AFF) Implementation

In an AFF implementation, the IFF path addition occurs in the analog domain. This addition requires either an active adder [Lee09] or a passive SC adder [Nam05, Fuj06, Kan06]. The use of an active adder increases the power consumption and limits the signal swing. To overcome these problems, a passive SC adder can be used, but in turn, it introduces gain loss due to charge sharing depending on the number of paths in the addition, leading to the scaling down of the signal handed to the quantizer. This signal scaling down tightens the offset requirements of the comparator(s) [Ham04b]. In a multi-bit quantizer, the SC adder network should be replicated in front of each comparator which increases the complexity of the system.

In most AFF structures, the signal-transfer function STF=1 which implies that no signal at all flows through the loop filter in a single DAC feedback architecture as depicted in Figure 2.7. In a multiple DAC feedback architecture (Figure 2.8), multiple IFF paths have to be added to cancel the signal throughout the loop filter. Another advantage of STF=1 is to further relax the anti-aliasing filtering requirements since the out-of-band interferers are not boosted compared to a typical STF with out-of-band gain. But, because of the delay-free IFF path, it puts some complications in the feedback timing as will be explained in Section 2.5.

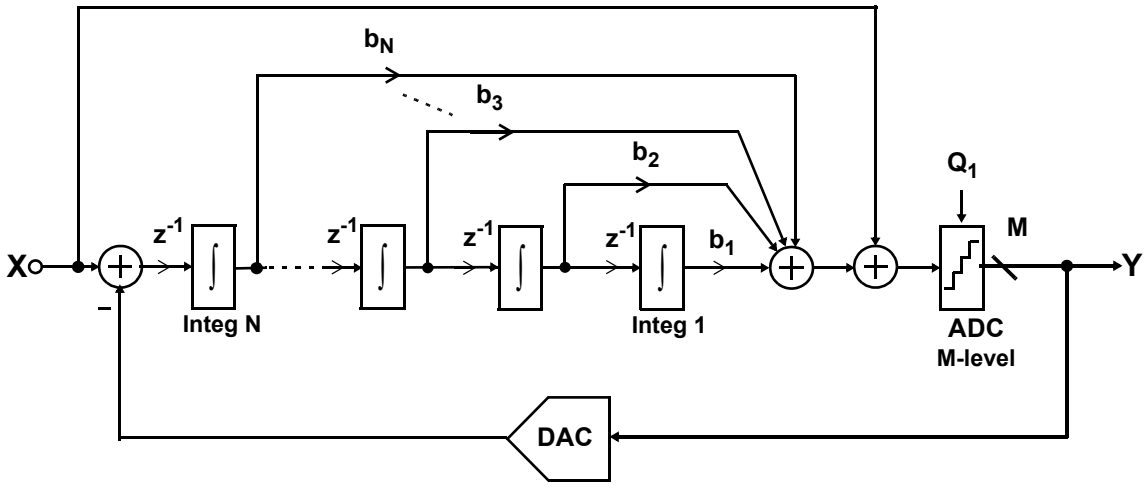


Figure 2.7: Analag feedforward (AFF) implementation in an N^{th}-order single DAC feedback architecture. [Sil01, Ham04b]. Here, the nondelaying integrator symbol $\int \equiv 1/(1-z^{-1})$.

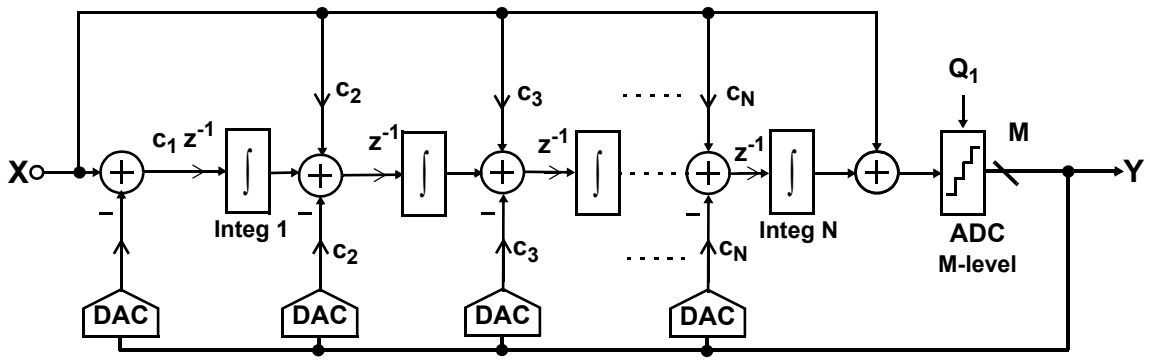


Figure 2.8: Analag feedforward (AFF) implementation in an Nth-order multiple DAC feedback architecture. [Gag04, Ham04b]. Here, the nondelaying integrator symbol $\int \equiv 1/(1-z^{-1})$.

2.4.3 Digital-Feedforward (DFF) Implementation

The DFF implementation [Kwo06, Gha05, Ham08b, Gha09] allows the implementation of the addition of the IFF path in the digital domain. Although an extra quantizer is required, the total number of comparators can be maintained the same given the extremely reduced swing at the input of the main quantizer. The quantization noise from the extra quantizer has to be cancelled to avoid performance degradation. Although the STF can't be unity in such designs, an |STF|=1 can still be achieved [Ham08a] to maintain the advantage of anti-aliasing filtering relaxation. Since most DFF architectures do not rely on a delay-free IFF path, the feedback timing is more relaxed than in AFF architectures.

In [Kwo06], as shown in Figure 2.9, an additional AFF path is added to lower the signal swing at the output of the first integrator due to the multiple DAC feedback structure. In the architecture of [Ham08b], depicted in Figure 2.10, the signal component is highly suppressed at the output of the last integrator (input of the main quantizer) by the input DFF path. Although a signal component is still present at the output of the other integrators, the single DAC feedback architecture [Ham06] (versus multiple DAC feedback architecture) ensures that the signal components are highly suppressed at the output of the rest of the integrators. Having a single DAC feedback, the architecture in [Ham08b] looks more attractive for high-order $\Delta\Sigma$ modulators.

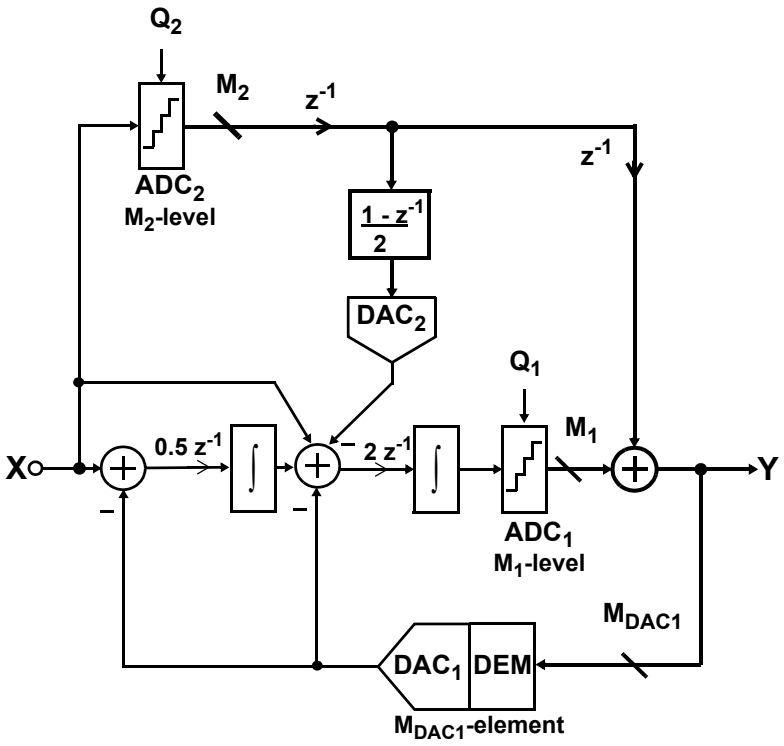


Figure 2.9: Digital feedforward (DFF) implementation in an 2[nd]-order multiple DAC feedback architecture. [Kwo06]. Here, $\int \equiv 1/(1-z^{-1})$.

The maximum input signal swing in the DFF architectures is determined by the overload of the extra quantizer as long as the DAC can handle this signal swing. The proper design of the quantizers' references ensures more power savings. In some cases, overloading the extra quantizer can be tolerated as long as the quantization noise from the extra quantizer can still be cancelled and the feedback loop subtraction is properly performed [Gha09, Kwo09].

Many DT ΔΣ modulators listed in Table 1.1 uses AFF architectures [Mor10, Oh12, Yam12, Zan12]. In [Kwo09], in Table 1.1, a DFF architecture is used along with some AFF paths like [Kwo06]. Due to the maximum signal swing advantage as well as the easier addition implementation, DFF architecture sounds preferable. In this thesis, we will focus on the DFF implementation of a single DAC feedback architecture (Figure 2.10 [Ham08b]) because of its reduced swings advantage.

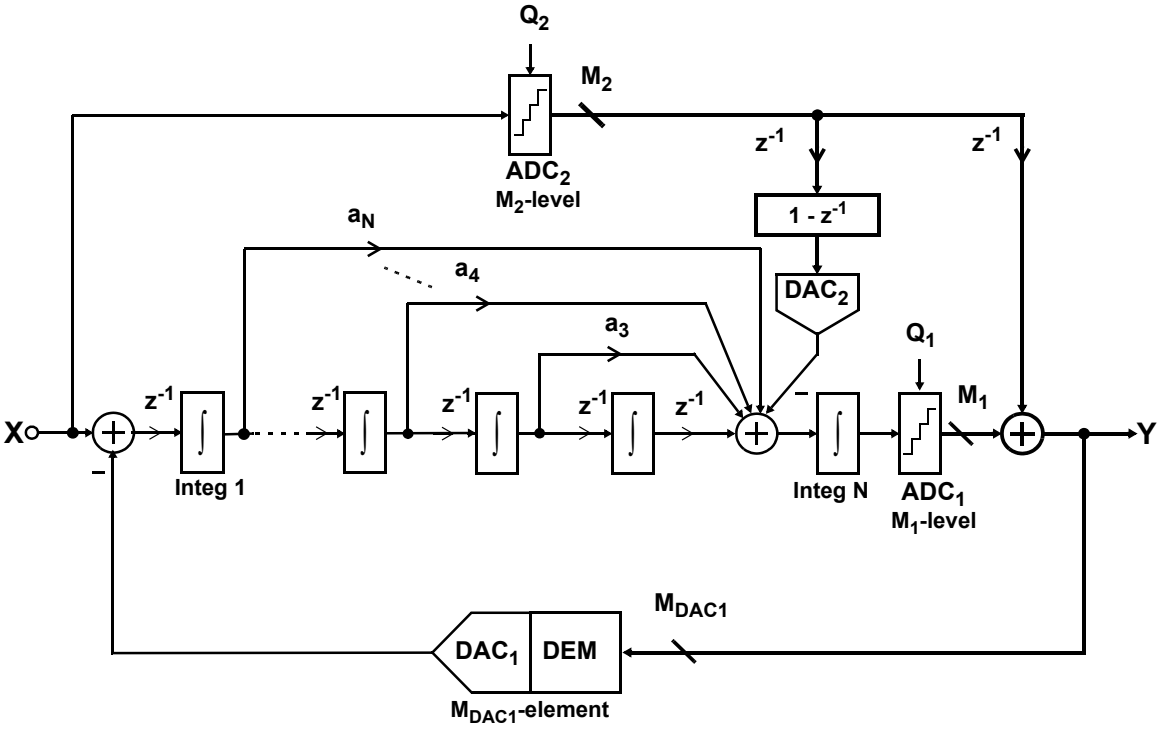


Figure 2.10: Digital feedforward (DFF) implementation in an N$^{\text{th}}$-order single DAC feedback architecture. [Ham08b]. Here, $\int \equiv 1/(1-z^{-1})$.

2.5 Feedback-Timing Relaxation Techniques

It is of critical importance to make sure that, while looking into various $\Delta\Sigma$ architectures, the feedback timing requirements can be met on the implementation level. Looking into the feedback path, there is always a constraint on when the feedback signal should be ready for processing (DAC, subtract, and integrate). This is more important in multi-bit designs where most likely dynamic-element-matching (DEM) techniques must be used for DAC linearization. We are assuming here that the $\Delta\Sigma$ modulator is operated from the standard two non-overlapping clock phases ϕ_1 and ϕ_2 necessary for proper SC circuits operation (Figure 2.11 and Figure 2.12).

In most AFF $\Delta\Sigma$ architectures, where STF=1, the delay-free input feedforward path implies that the quantization and DEM processing (if applicable) has to be performed within the non-overlapping time, as explained in [Gha06], which might severely limit the operation speed (Figure 2.11). Several solutions have been suggested to solve this problem and relax the DEM timing. In [Fuj06] and [Gha06] a half delay is added in the signal path in front of the loop filter to give an extra half-delay for the DEM processing. The SC implementation is based on double sampling the input signal on two sampling capacitors. The obvious cost is the added kT/C switch noise and the noise folding due to path mismatch. The noise folding problem can be alleviated by not sharing the two sampling capacitors between the signal path and the feedback path and using a separate capacitor for the feedback path which adds more kT/C noise and consumes more power. This idea can be extended for more DEM timing relaxation by using triple sampling instead of double sampling to add a full delay (clock cycle) in the signal path and giving in turn a complete clock cycle for DEM processing [Kan06, Fuj09].

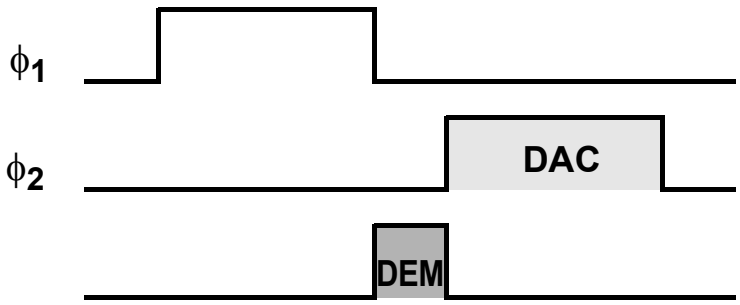


Figure 2.11: Timing diagram and available time for DEM in most AFF $\Delta\Sigma$ architecture with STF=1 [Kwo07].

In most DFF $\Delta\Sigma$ architectures [Kwo06, Ham08b], the input feedforward path is not delay-free, which inherently relaxes feedback timing as shown in Figure 2.12. Nonetheless, [Kwo07] suggests a scheme to further relax DEM timing for high speed applications. The idea is based on splitting the feedback signal (and DAC) into a main critical DAC path that processes quantization noise only and that does not need DEM and another non-critical DAC path that processes the full signal and that needs DEM. In the DFF architecture presented in [Gha05], also named as 0-L MASH architecture in [Gha09], a DEM timing relaxing is needed since there exists a delay free path that does not leave enough time for DEM processing.

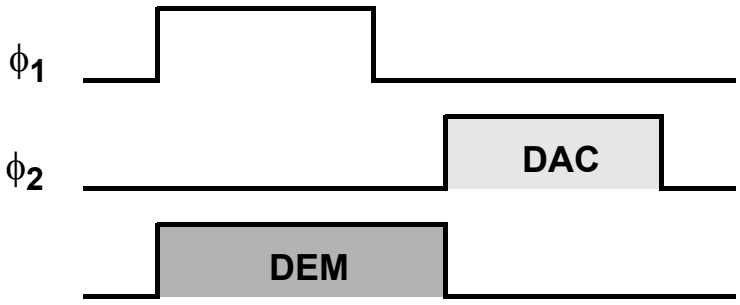


Figure 2.12: Timing diagram and available time for DEM in most DFF $\Delta\Sigma$ architecture [Kwo07].

In this work, we will look into the optimized utilization of the available timing in a more inclusive way. The target is to give enough timing for feedback processing (DEM and other) without wasting time especially considering the fact that digital circuitry can run at fast rates in nanometer CMOS (such as 65nm process in this thesis). This is based on: first, using non-overlapping clock phases with unequal duty cycles to better exploit the available time in the different phases and give one more degree of freedom to allow for a more power-efficient design (see Chapter 5); second, as will be explained in details in Chapter 4, optimizing the simultaneous settling that might occur in the implementation of the chosen DFF $\Delta\Sigma$ architecture [Ham08b].

2.6 Conclusion

This chapter reviewed low-power DT $\Delta\Sigma$ modulators on different levels. On the SC implementation level, some low-power SC integrator circuit techniques have been explored outlining the various advantages and disadvantages of each technique. In the next chapter, Chapter 3, we will present a novel low-power SC technique based on a current-mirror opamp with switchable transconductances. On the system-level, various low-power DT $\Delta\Sigma$ architectures have been listed with the different aspects related to each architecture. Finally, the feedback timing issue has been focused on, along with previously suggested solutions. Based on that, a specific DFF $\Delta\Sigma$ architecture is selected for the scope of this thesis. Its low-power performance is ensured by optimized simultaneous settling (Chapter 4) and unequal clock phases (Chapter 5).

Chapter 3

A Switchable-Opamp for Low-Power Switched-Capacitor Integrator Design

The switched-capacitor (SC) integrator is the basic building block of various SC filters, especially the loop filter of discrete-time (DT) $\Delta\Sigma$ modulators. Depending on the output sampling phase, a SC integrator can have either a full delay (Figure 3.1) or a half delay (Figure 3.2) as explained in details in Section 3.1. During the sampling phase ϕ_1, the integrator input is sampled on the sampling capacitor C_S, while the integrator output from the previous clock phase is held on the feedback capacitor C_F. Since the integrator output does not change during ϕ_1, the opamp can be turned off during this sampling phase, in order to save power. During the charge-transfer phase ϕ_2, the charge sampled on C_S during the previous clock phase is transferred to C_F. Therefore the opamp must be fully operational during this charge-transfer phase.

This chapter presents a switchable-opamp for the low-power design of SC integrators [Har13a] as part of the low-power DT $\Delta\Sigma$ modulator design as explained in Chapter 2. It is based on a current-mirror opamp [Joh97], but with output transconductances that can be switched off during the sampling phase (Section 3.2). It can be used in the design of SC integrators with both *half-delay* and *full-delay*. Furthermore, since its input transconductance

is on at all times, it doesn't suffer from operation-speed limitations found in previous designs. Simulation results confirm that power reductions of up to 30% can be achieved in SC integrators by using the proposed switchable-opamp (Section 3.5), compared to having the current-mirror opamp fully active at all times.

Section 3.1 starts with an overview of the previously proposed switchable-opamps. Section 3.2 illustrates the switchable-opamp technique. Section 3.3 then describes its circuit realization. Section 3.4 goes over the power savings that can be achieved. Section 3.5 presents circuit simulation results to confirm the functionality and the performance advantages of the technique in SC integrators and DT $\Delta\Sigma$ modulators.

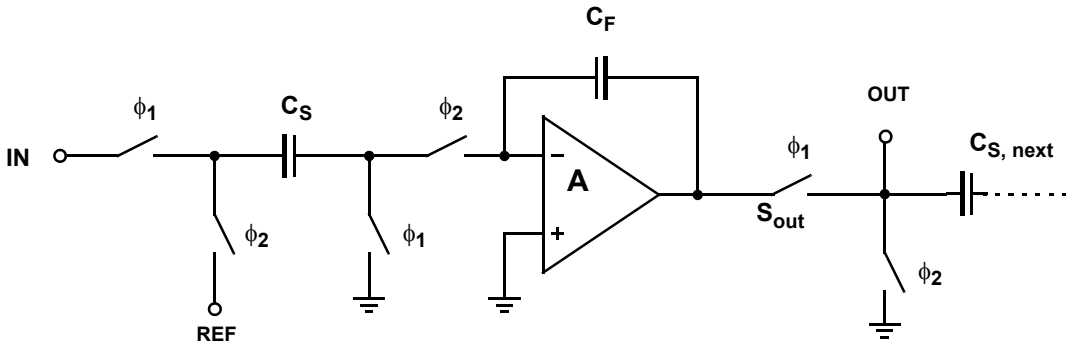


Figure 3.1: A *full-delay* SC integrator with the loading effect of its next sampling stage capacitor $C_{S,next}$.

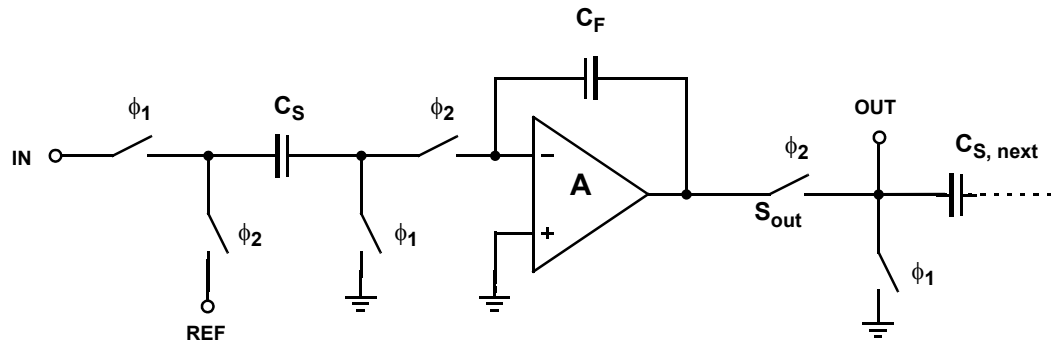


Figure 3.2: A *half-delay* SC integrator with the loading effect of its next sampling stage capacitor $C_{S,next}$.

3.1 Overview and Previous Work

During the sampling phase ϕ_1 of a full-delay SC integrator, the integrator's input is sampled on the sampling capacitor C_S (Figure 3.3), while the integrator's output from the previous clock phase is held on the feedback capacitor C_F and sampled by the next stage sampling capacitor $C_{S,next}$. Since the integrator's output does not change during ϕ_1, the opamp can be *partially* turned off during this sampling phase, in order to save power. During the charge-transfer phase ϕ_2, the charge sampled on C_S during the previous clock phase is transferred to C_F (Figure 3.4). Therefore the opamp must be *fully* operational during this charge-transfer phase.

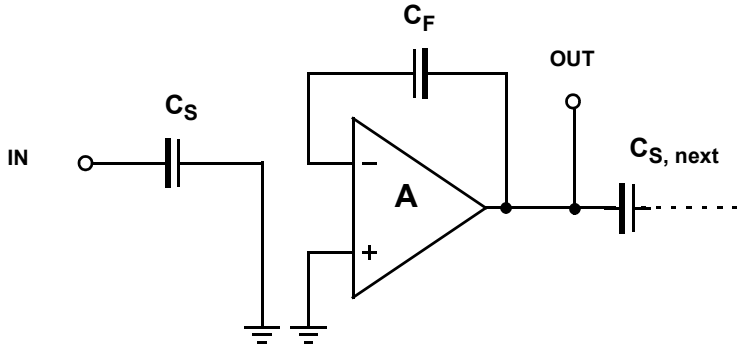


Figure 3.3: A full-delay SC integrator during its sampling phase ϕ_1.

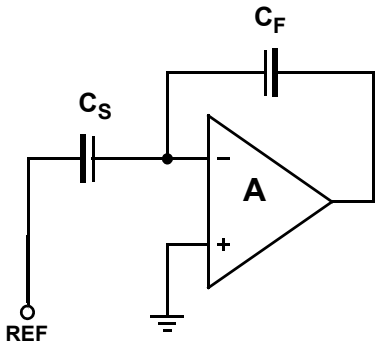


Figure 3.4: A full-delay SC integrator during its charge-transfer phase ϕ_2.

During the sampling phase ϕ_1 of a half-delay SC integrator, the integrator input is sampled on the sampling capacitor C_S (Figure 3.5), while the integrator's output from the previous clock phase is held on the feedback capacitor C_F. Since the integrator's output does not change during ϕ_1, the opamp can be *completely* turned off during this sampling phase, in order to save power. During the charge-transfer phase ϕ_2, the charge sampled on C_S during the previous clock phase is transferred to C_F while the output is sampled on the next stage

sampling capacitor $C_{S,next}$(Figure 3.6). Therefore the opamp must be *fully* operational during this charge-transfer phase.

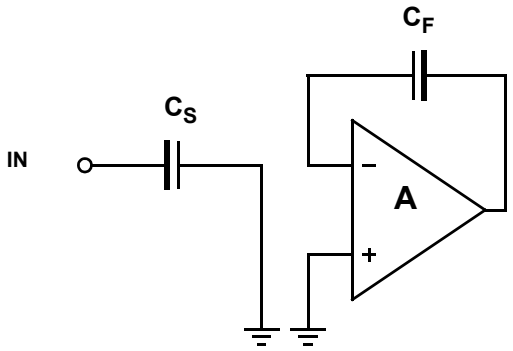


Figure 3.5: A half-delay SC integrator during its sampling phase ϕ_1.

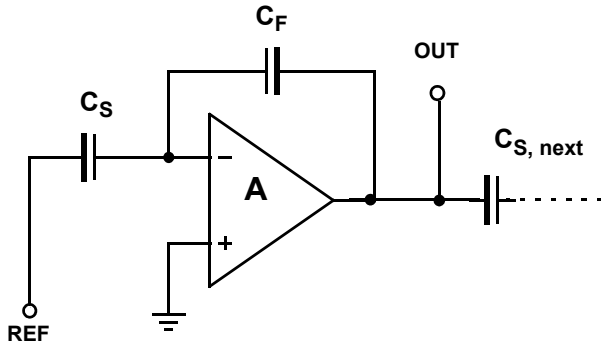


Figure 3.6: A half-delay SC integrator during its charge-transfer phase ϕ_2.

Several switchable-opamp methods have been proposed to reduce the power dissipation in the integrators in SC filters and DT $\Delta\Sigma$ modulators. These include:

1. **Switched-Opamp (SO) method [Cro94, Xu11]:** Here, the integrator's opamp is fully switched off during the sampling phase and on during the charge-transfer phase (Figure 3.7). This can save up to 50% of the power consumption, compared to conventional designs with opamps fully active at all times [Che03]. However, this can limit the operation speed, due to the time required to turn on the opamps.

2. **Partially-Switched-Opamp (PSO) method [Kuo10, Che03, Bas97]:** Here, a two-stage opamp is used and only its output stage is switched off during the sampling phase and on during the charge-transfer phase (Figure 3.8). By keeping the opamp's input stage on at all times, a faster turn-on time and, hence, operation speed can be

achieved, compared to a SC integrator with an SO design. Furthermore, since the input stage may burn 1/4 of the opamp's total power consumption, power reductions of 40% can be typically achieved with a PSO design [Che03].

Another advantage of the SO and PSO methods is that the floating switch (S_{out} in Figure 3.2) can be eliminated, since the opamp output is in a high-impedance state during ϕ_1. This can improve the integrator linearity, especially in low-voltage-supply designs. However, the associated disadvantage is that both the SO and PSO methods can only be employed in SC integrators with *half delay*, thereby restricting their use to specific DT $\Delta\Sigma$ modulator or SC filter architectures [Pel98]. Furthermore, these opamps require special common-mode feedback (CMFB) circuits, since the opamp output is reset during the sampling phase [Sin08].

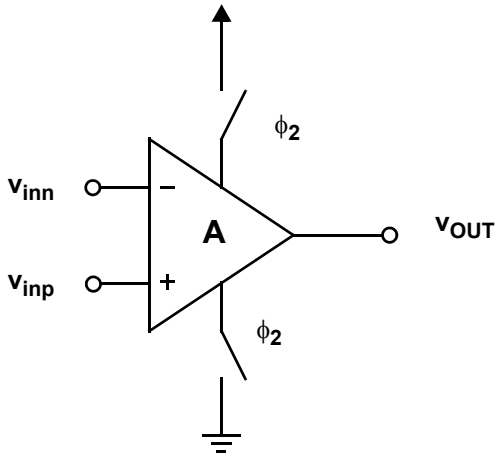


Figure 3.7: The conceptual diagram of the switched-opamp method.

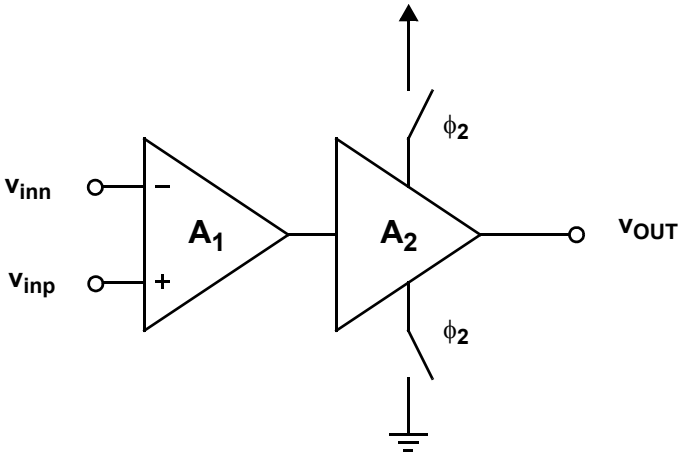


Figure 3.8: The conceptual diagram of the partially-switched-opamp method.

3.2 A Current-Mirror Opamp with Switchable Transconductances

Consider the conceptual diagram of the current-mirror opamp shown in 3.9 [Har13a]. It has an input transconductance G_m, and a total output transconductance KG_m, where K is the current gain from the input to the output sides of the opamp. The total output transconductance and its load are split into two parts with a ratio α to $(1-\alpha)$. The α part of the total transconductance and its load are switched off during the sampling phase ϕ_1 and on during the charge-transfer phase ϕ_2, while the $(1-\alpha)$ part remains on at all times. Accordingly, the proposed opamp in Figure 3.9 has the following advantages:

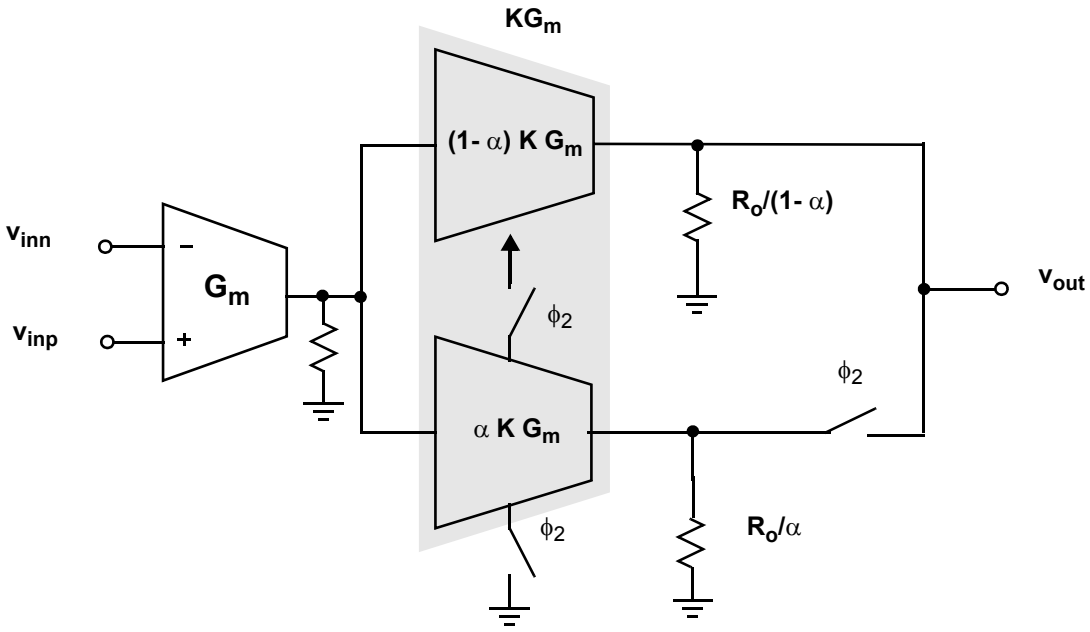


Figure 3.9: The conceptual diagram of the proposed switchable-opamp [Har13a].

1. Since the opamp output is available during both clock phases, this opamp can be used to realize both full-delay (Figure 3.1), and half-delay (Figure 3.2) SC integrators. Furthermore, classical SC common-mode feedback (CMFB) circuits can be used with this opamp with no need for special circuitry.

2. During the charge-transfer clock phase ϕ_2, the opamp is operated at its full output transconductance KG_m, in order to maximize the unity-gain bandwidth ω_t and, hence, achieve the targeted settling accuracy. However, the opamp does not need a high ω_t during the sampling clock phase ϕ_1, as its output does not change during ϕ_1 and the feedback factor β is close to unity . Therefore, by turning off part of the opamp's output transconductance during ϕ_1, power savings can be achieved. It is important to note that, for a full-delay integrator (Figure 3.1), sampling the output on $C_{S,\ next}$ during ϕ_1, puts an upper limit on the value of α.

3. Since the opamp's input transconductance and part of its output transconductance are on at all times, this opamp doesn't suffer from the operation speed limitations found in SO and PSO designs.

3.3 Circuit Design

The current-mirror opamp topology is one of the common choices when driving on-chip capacitive loads [Joh97]. Consider a fully-differential classical current-mirror opamp with cascode current-mirrors and bias current sources (the circuit in Figure 3.10 with no switching) having a current gain (from input to output) of K [Joh97]. At a given total bias current (power dissipation), if the unity-gain bandwidth is limited by the load capacitance, increasing K increases both the unity-gain bandwidth and the slew-rate, at the expense of a decrease in phase margin and an increase in the input-referred thermal noise. A practical upper limit on K might be around 5 [Joh97]. In order to realize the switchable-opamp in Figure 3.9, the output transistors of the current-mirror opamp in Figure 3.10 are split with a ratio of α to $(1-\alpha)$. The α part is switched on during ϕ_2 and switched off during ϕ_1. The output current is switched from KI_B during ϕ_2 to $(1-\alpha)KI_B$ during ϕ_1. Transistor-fingering layout techniques enable realizing various values of α. The only extra layout area required is for the switches used to control the gate of the switching transistors.

It is worth noting that the cascode transistors in the output stage should be switched along with the rest of the transistors to switch the output resistance and hence maintain a constant opamp DC gain.

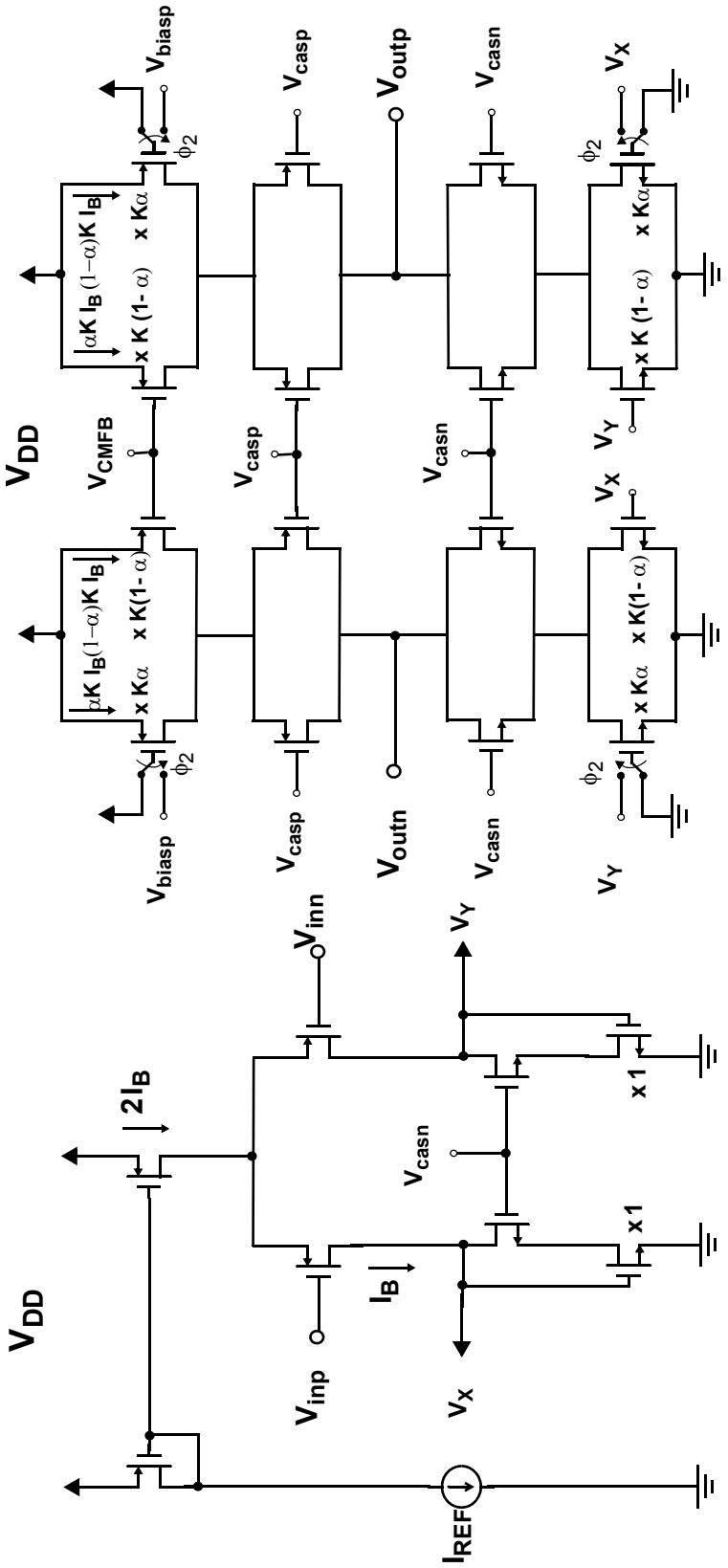


Figure 3.10: The circuit diagram of the switchable-opamp [Har13a].

One simplified alternative is to keep the cascode transistors on all the time in full width (Figure 3.10) and adjust the biasing conditions such that the DC gain does not change much with switching or at least the DC gain variation does not generate undesired distortion.

3.4 Power Savings Analysis

The supply current in a classical current-mirror opamp (the circuit in Figure 3.10 with $\alpha = 0$) is given by (neglecting bias circuit current):

$$I_{DD_{classical}} = 2I_B + 2KI_B \tag{3.1}$$

Where $2I_B$ is the input differential-pair bias current (Figure 3.10). Assuming a clock duty cycle of 50%, the supply current (averaged over a clock period) in the proposed opamp (Figure 3.10) is given by:

$$I_{DD,avg_{proposed}} = 2I_B + (2-\alpha)KI_B \tag{3.2}$$

Therefore, the reduction in supply current, achieved by the proposed switchable-opamp technique, is

$$\Delta I_{DD,avg} \equiv I_{DD_{classical}} - I_{DD,avg_{proposed}} = \alpha K I_B \tag{3.3}$$

This results in a relative power-dissipation saving of

$$\frac{\Delta I_{DD,avg}}{I_{DD_{classical}}} = \frac{\alpha/2}{1+1/K} \tag{3.4}$$

Figure 3.11 plots the relative power-dissipation saving in (3.4) versus the switching ratio α, for various current gains K. A power saving of 30% can be achieved for a switching ratio α of 0.75 in a current-mirror opamp with $K = 4$.

Assume a particular system design problem where either a half-delay or a full-delay SC integrator can be employed. In the case of a half-delay integrator, it is an obvious design choice to apply the SO technique and save about 50% of the power compared to a non-switching opamp in a half-delay integrator. Whereas in a full-delay integrator, the presented current-mirror opamp with switchable-transconductances would be the suitable choice with power

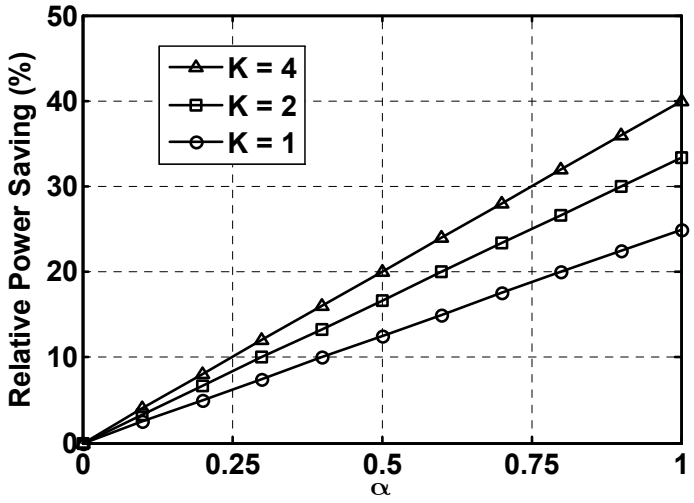


Figure 3.11: Relative power-dissipation saving, achieved using the proposed switchable-opamp (Figure 3.10) vs. switching ratio α, for various current gains K.

savings reaching about 30% compared to a non-switching opamp in a full-delay integrator. Although we would intuitively assume a lower average power consumption in the case of a half-delay integrator with SO, detailed comparison considering the different loading could reveal a different conclusion. In a half-delay integrator (Figure 3.6), the output is sampled on $C_{S,next}$ during the charge transfer phase ϕ_2 which adds more loading compared to a full-delay integrator during its charge transfer phase (Figure 3.4). Assuming that we are targeting the same settling accuracy (error) of the output sampled on $C_{S,next}$, let us compare the average current consumption required in each case.

Assume that C_S, C_F and $C_{S,next}$ are equal in both cases and $K_I = \frac{C_S}{C_F}$ is the integrator's gain. Also, assume an infinite opamp DC gain to focus on the settling errors due to finite bandwidth which is in turn linked to the current consumption. Assume also that a current-mirror opamp, with a transconductance G_{mh} and G_{mf} for the half-delay and full-delay integrators respectively, is used in both cases for the sake of the comparison. Neglecting the parasitic capacitances, the feedback factors β during ϕ_1 and ϕ_2 for both half-delay and full-delay integrators are:

$$\beta_1 = \frac{C_F}{C_F} \tag{3.5}$$

$$\beta_2 = \frac{C_F}{C_F + C_S} \tag{3.6}$$

For the half-delay integrator, the load capacitance during ϕ_2 is expressed as:

$$C_{Lh2} = \frac{C_S C_F}{C_F + C_S} + C_{S,next} = \beta_2 C_S + C_{S,next} \tag{3.7}$$

While the closed loop time-constant can be found to be:

$$\tau_{h2} = \frac{C_{Lh2}}{\beta_2 G_{mh}} \tag{3.8}$$

The output sampled on $C_{S,\ next}$ at the end of the charge-transfer phase ϕ_2 for an available settling time T_{set} and in response to an input step $V_{in,step}$ (representing the input voltage sampled on C_S) can be expressed as:

$$V_{out\ h,sampled} = K_I V_{in,step}(1 - e^{-\frac{T_{set}}{\tau_{h2}}}) \tag{3.9}$$

From which, The relative settling error can be expressed as

$$\epsilon_h = e^{-\frac{T_{set}}{\tau_{h2}}} = e^{-\frac{T_{set}\beta_2 G_{mh}}{C_{Lh2}}} \tag{3.10}$$

For the full-delay integrator, the load capacitance during both phases can be expressed as:

$$C_{Lf2} = \frac{C_S C_F}{C_F + C_S} = \beta_2 C_S \qquad\qquad C_{Lf1} = C_{S,next} \tag{3.11}$$

While the closed loop time-constant can be found to be:

$$\tau_{f2} = \frac{C_{Lf2}}{\beta_2 G_{mf2}} \qquad\qquad \tau_{f1} = \frac{C_{Lf1}}{\beta_1 G_{mf1}} \tag{3.12}$$

Where:

$$G_{mf2} = G_{mf} \qquad\qquad G_{mf1} = (1 - \alpha) G_{mf} \tag{3.13}$$

The output at the end of the charge transfer phase ϕ_2 for an available settling time T_{set} in response to an input step $V_{in,step}$ (representing the input voltage sampled on C_S) can be expressed as:

$$V_{out\ f} = K_I V_{in,step}(1 - e^{-\frac{T_{set}}{\tau_{f2}}}) \tag{3.14}$$

The output sampled on $C_{S,next}$ at the end of the sampling phase ϕ_1 is given by:

$$V_{out\ f,sampled} = V_{out\ f}(1 - (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}}{\tau_{f1}}}) \tag{3.15}$$

$$V_{out\ f,sampled} = K_I V_{in,step}(1 - e^{-\frac{T_{set}}{\tau_2}})(1 - (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}}{\tau_1}}) \tag{3.16}$$

From which, the relative settling error can be expressed as:

$$\epsilon_f = e^{-\frac{T_{set}}{\tau_{f2}}} + (\frac{C_{S,next}}{C_F + C_{S,next}})(1 - e^{-\frac{T_{set}}{\tau_{f2}}})e^{-\frac{T_{set}}{\tau_{f1}}} \tag{3.17}$$

Assuming that $\tau_{f1}, \tau_{f2} < 3T_{set}$, then:

$$\epsilon_f \approx e^{-\frac{T_{set}}{\tau_{f2}}} + (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}}{\tau_{f1}}} \tag{3.18}$$

$$\epsilon_f \approx e^{-\frac{T_{set}\beta_2 G_{mf_2}}{C_{Lf2}}} + (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}\beta_1 G_{mf_1}}{C_{Lf1}}} \tag{3.19}$$

To give a numerical example, assume now that $C_F = C_S$ and $C_{S,next} = \frac{C_S}{2}$ in both cases, then for both cases:

$$\beta_1 = 1 \tag{3.20}$$

$$\beta_2 = \frac{1}{2} \tag{3.21}$$

For the half-delay integrator:

$$C_{Lh2} = \frac{C_S}{2} + C_{S,next} = C_S \tag{3.22}$$

$$\tau_{h2} = \frac{2\ C_S}{G_{mh}} \tag{3.23}$$

$$\epsilon_h = e^{-\frac{T_{set}G_{mh}}{2\ C_S}} \tag{3.24}$$

While for the full-delay integrator:

$$C_{Lf2} = \frac{C_S}{2} \qquad C_{Lf1} = \frac{C_S}{2} \tag{3.25}$$

$$\tau_{f2} = \frac{C_S}{G_{mf2}} \qquad \tau_{f1} = \frac{C_S}{2\ G_{mf1}} \tag{3.26}$$

$$\tau_{f2} = \frac{C_S}{G_{mf}} \qquad \tau_{f1} = \frac{C_S}{2\ (1-\alpha)G_{mf}} \tag{3.27}$$

$$\epsilon_f \approx e^{-\frac{T_{set}G_{mf}}{C_S}} + \frac{1}{3}\ e^{-\frac{2T_{set}(1-\alpha)G_{mf}}{C_S}} \tag{3.28}$$

The problem now is to solve for G_{mh}, G_{mf} and α that ensures that the relative errors given by (3.24) and (3.28) are equal and meet the targeted error to be designed for. Assume that the targeted error is:

$$\epsilon_h = \epsilon_f = e^{-5} \tag{3.29}$$

Then from (3.24) and (3.29):

$$e^{-\frac{T_{set}G_{mh}}{2\ C_S}} = e^{-5} \tag{3.30}$$

$$\frac{T_{set}G_{mh}}{2\ C_S} = 5 \tag{3.31}$$

$$G_{mh} = 10\ \frac{C_S}{T_{set}} \tag{3.32}$$

And from (3.28) and (3.29):

$$e^{-\frac{T_{set}G_{mf}}{C_S}} + \frac{1}{3}\ e^{-\frac{2T_{set}(1-\alpha)G_{mf}}{C_S}} = e^{-5} \tag{3.33}$$

The last equation (3.33) is not as easy to solve as (3.30) as it has two unknowns: G_{mf} and α. To make the comparison easier, let us assume that $C_S = 1pF$ and $T_{set} = 1ns$.

As previously assumed, the opamp topology is the current-mirror opamp in both cases. The current consumption (neglecting bias circuit) can be written as:

$$I_{DD} = C\ G_m\ \frac{(1+K)}{K} \tag{3.34}$$

to add the current consumption of the input part. Where C is a circuit design constant. Assume now that $C = 1V^{-1}$ and $K = 4$ to simplify calculations. This gives the results shown in Table 4.1 for the half-delay integrator with SO.

Table 4.2 lists the corresponding transconductances and current consumption for the full-delay integrator for different values of α resulting from solving equation (3.33).

It is clear from the comparison between Table 4.1 and Table 4.2 that the current-mirror opamp with switchable-transcoinductances in the full-delay integrator ends up consuming less average current (for $\alpha = 0.25$ and $\alpha = 0.5$) than the switched-opamp in the half-delay

Table 3.1: The transconductance and current consumption in both ϕ_2 and ϕ_1 phase for the *half-delay* integrator employing the SO method.

G_{mh2} (mS)	G_{mh1} (mS)	I_{DDh2} (mA)	I_{DDh1} (mA)	$I_{DDh,avg}$ (mA)
10	0	12.5	0	6.25

Table 3.2: The transconductance and current consumption in both ϕ_2 and ϕ_1 phase for the *half-delay* integrator employing the switchable-transconductances technique for different values of α.

α	G_{mf2} (mS)	G_{mf1} (mS)	I_{DDf2} (mA)	I_{DDf1} (mA)	$I_{DDf,avg}$ (mA)
0	5	5	6.25	6.25	6.25
0.25	5.05	3.8	6.3	4.75	5.53
0.5	5.3	2.65	6.63	3.3	5
0.75	8	2	10	2.5	6.25

integrator although it is assumed to be completely switched off during ϕ_1. The reason behind that, as previously mentioned, is the capacitive load that is split on two phases in the full-delay case compared to the half-delay case where the load capacitance is grouped in one phase. The listed results in Table 4.2 shows that an α of 0.5 gives a lower current consumption than the case of $\alpha = 0.25$ and $\alpha = 0.75$, which means that there is always an optimum value of α that achieves the minimum average current consumption for a given targeted settling error.

Although this was a numerical example based on specific, but realistic, assumptions, the general conclusion is that the comparison between the SO technique (in a half-delay integrator) and the proposed switchable-opamp technique (in a full-delay integrator) should be based on the absolute power consumption rather than the relative saved power consumption. All this with the assumption that the system requirements are identical in both designs and that both full-delay and half-delay integrators can be employed in the system.

3.5 Circuit Simulation Results

The proposed switchable-opamp (Figure 3.10) was designed in a 1V 65nm CMOS process, with a current gain of $K = 4$, to achieve the following specifications when $\alpha = 0$ (i.e. for a classical current-mirror opamp configuration):

- DC gain $A_0 = 165V/V$.
- Unity-gain bandwidth $f_T = 725MHz$ (at a 1pF load).
- Phase-margin $PM = 80^o$(at a feedback factor of 0.5).

The opamp specifications, when $\alpha = 0.75$, change to:

- DC gain $A_0 = 160V/V$.
- Unity-gain bandwidth $f_T = 200MHz$ (at a 1pF load).
- Phase-margin $PM = 88^o$(at a feedback factor of 0.5).

The above opamp was used to realize a full-delay SC integrator (Figure 3.1) with:

- Sampling frequency $f_S = 128MHz$.
- Sampling capacitor $C_S = 1.5pF$.
- Integrator gain $K_I = C_S/C_F = 1$.
- Next-stage sampling capacitor $C_{S,next} = 0.5pF$.

The SC integrator was then simulated, in order to demonstrate how using the proposed switchable-opamp can impact the performance of a SC integrator.

3.5.1 Gain Error of the SC integrator

When a step voltage of height $V_{in,step}$ is applied at the input of an ideal SC integrator, the resulting change at the output is $K_I V_{in,step}$, where $K_I = C_S/C_F$ is the integrator gain.

Therefore, the gain error of the SC integrator can be expressed as [Ham06]:

$$\epsilon \equiv \frac{|K_I V_{in,step}| - |V_{out,sampled}|}{|K_I V_{in,step}|} = \epsilon_g + \epsilon_{sett} \tag{3.35}$$

where $V_{out,sampled}$ is the integrator's output sampled at the end of ϕ_1, ϵ_g is the integrator's gain error due to the opamp's finite DC gain, and ϵ_{sett} is the integrator's gain error due to opamp dynamics (finite bandwidth and slew rate) [Ham06]. For the SC integrator specified above, $\epsilon_g = 0.015$ and $\epsilon_{sett} = e^{-5}$ (0.007) with no switching ($\alpha = 0$) and for a small input step (linear settling) which results in an ϵ of 2.2%.

Table 3.3: SC integrator's gain error ϵ and the achievable power savings using the proposed switchable-opamp for various values of the opamp switching ratio α, at a 50mV and 250mV input steps.

α	Gain error ϵ (%)		$I_{DD,avg}(mA)$	Power saving (%)
	50mV step input	250mV step input		
0 (no switching)	2.2	2.5	1.35	0
0.25	2.2	2.5	1.21	10.3
0.5	2.2	2.5	1.09	19.2
0.75	2.4	3	0.96	28.8

Step response transient simulations were carried out and the gain error was calculated from the results for different cases. Table 3.3 reports the gain error ϵ of the SC integrator and the achievable power savings using the proposed switchable-opamp for various values of the opamp's switching ratio α, for a small and a large input step. Observe that ϵ remains approximately constant until α reaches 0.75. It then increases by about 8% for a small input step (20% for a large input step). Accordingly, while there is a power accuracy trade-off in the choice of α, an $\alpha = 0.75$ results in about 30% reductions in power dissipation without significantly affecting the integrator's gain error (especially, for small input steps).

The settling accuracy degradation is primarily due to the incomplete output sampling on $C_{S,next}$ during ϕ_1 as α increases as shown in the conceptual Figure 3.12. As depicted, while an α of 0 leads to power waste during ϕ_1, an α of 0.75 might leave the opamp with not enough power for proper output sampling during ϕ_1. Although, the value of the next stage

sampling capacitor $C_{S,\ next}$ is a determined by the system requirements (SC filter coefficients, thermal noise requirements), it is a key factor in this design trade-off. The optimum value of α depends primarily on the value of $C_{S,\ next}$. The other, less important, reason for the settling degradation, with the increase of α, is the time that the opamp needs to restore its full current at the beginning of ϕ_2. As α increases, the opamp needs more time to restore its full current, which directly affects the settling gain error.

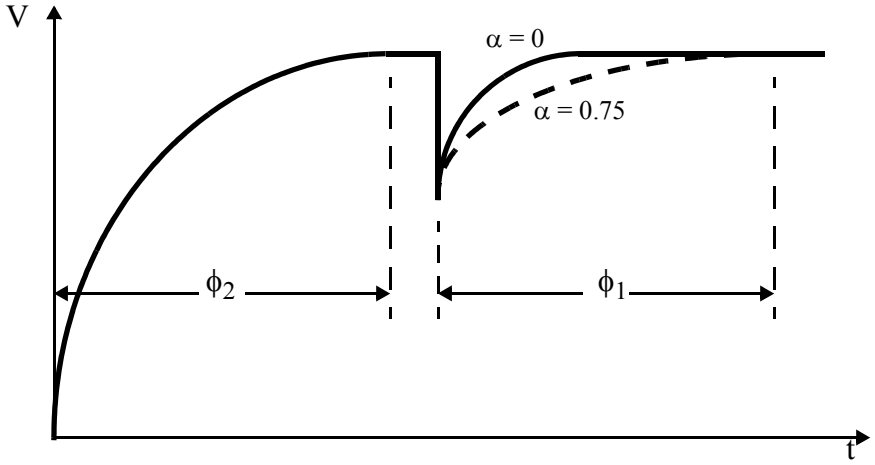
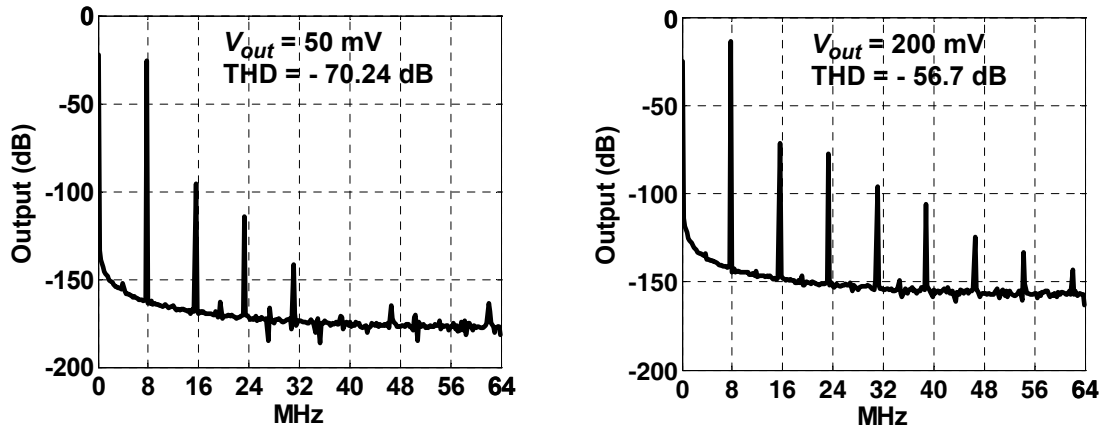


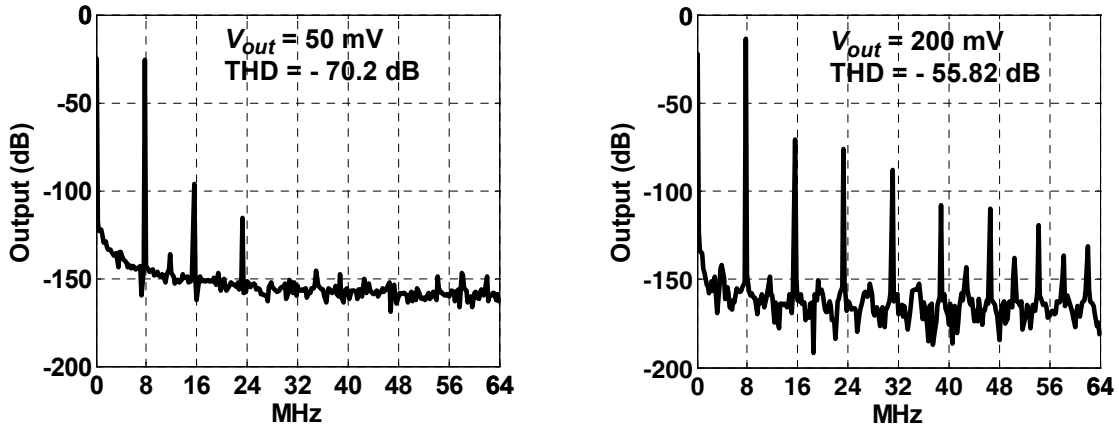
Figure 3.12: Effect of switching on output sampling on $C_{S,\ next}$.

3.5.2 Linearity of the SC integrator

A 7.75MHz sinusoid with amplitudes of $V_{in} = 20mV$ and $80mV$ is applied at the input of the SC integrator. A transient simulation is carried-out and results in a sinusoid at the output with amplitudes of $V_{out} = 50mV$ and $200mV$. A threshold-voltage mismatch of $\pm 3mV$ is added between the switching transistors on the positive and negative output sides of the opamp. A PSD is estimated from the sampled output waveform to evaluate the linearity. Figure 3.13 shows the integrator's output PSD when $V_{in} = 20mV$ ($V_{out} = 50mV$) and $V_{in} = 80mV$ ($V_{out} = 200mV$), when: a) $\alpha = 0$; and b) $\alpha = 0.75$. The difference in total harmonic distortion (THD) between the two cases ($\alpha = 0$ and $\alpha = 0.75$) is less than 1dB, at both output levels ($V_{out} = 50$ and $200mV$). Note that the PSD floor in Figure 3.13 is irrelevant as long as it is well below the harmonics of interest. A power saving of around 28.6% in power dissipation is achieved when $\alpha = 0.75$.



(a) α = 0



(b) α = 0.75

Figure 3.13: The output spectrum of the SC integrator with a $20mV$, and an $80mV$ input sinusoid, resulting in an output sinusoid having $V_{out} = 50mV$ and $V_{out} = 200mV$. Two cases are considered for the switching ratio of the integrator's opamp: (a) $\alpha = 0$ (No switching), and (b) $\alpha = 0.75$.

3.5.3 Performance of a DT ΔΣ Modulator

A second-order 3-bit ΔΣ modulator with analog input-feedforward as shown in Figure 3.14 [Ham04b, Bos88] is simulated for an OSR of 32. The proposed switchable-opamp technique is used in both full-delay integrators with a sampling frequency of 128MHz to see how the performance of a ΔΣ modulator is affected by the presented technique. A transient simulation is performed then the PSD of the sampled output is estimated.

Figure 3.15 shows the output spectrum of the $\Delta\Sigma$ modulator for a -1.4dBFS input sinusoid at 334.75kHz, when opamps with $\alpha = 0$ and $\alpha = 0.75$ are used. The difference in SNDR between the two cases is less than 1dB, over a 2MHz bandwidth, while a reduction of around 28.6% in the power dissipation of each integrator is achieved when $\alpha = 0.75$.

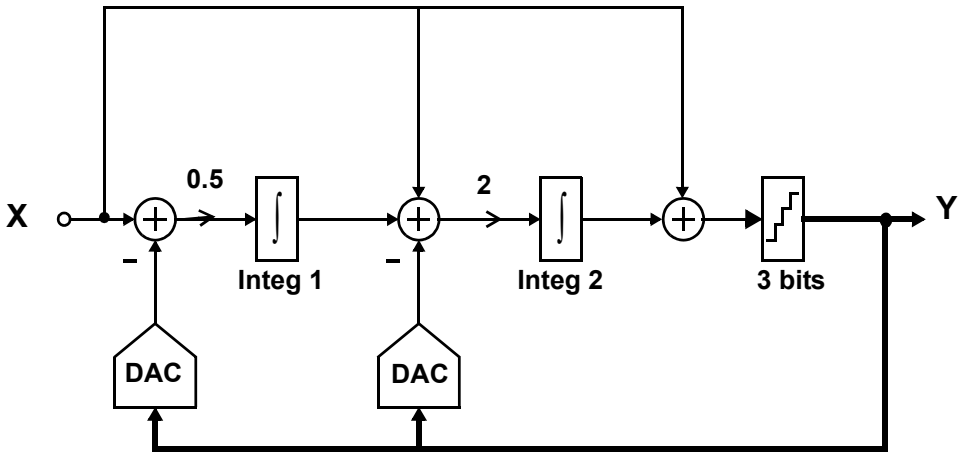


Figure 3.14: The simulated second-order 3-bit $\Delta\Sigma$ modulator.

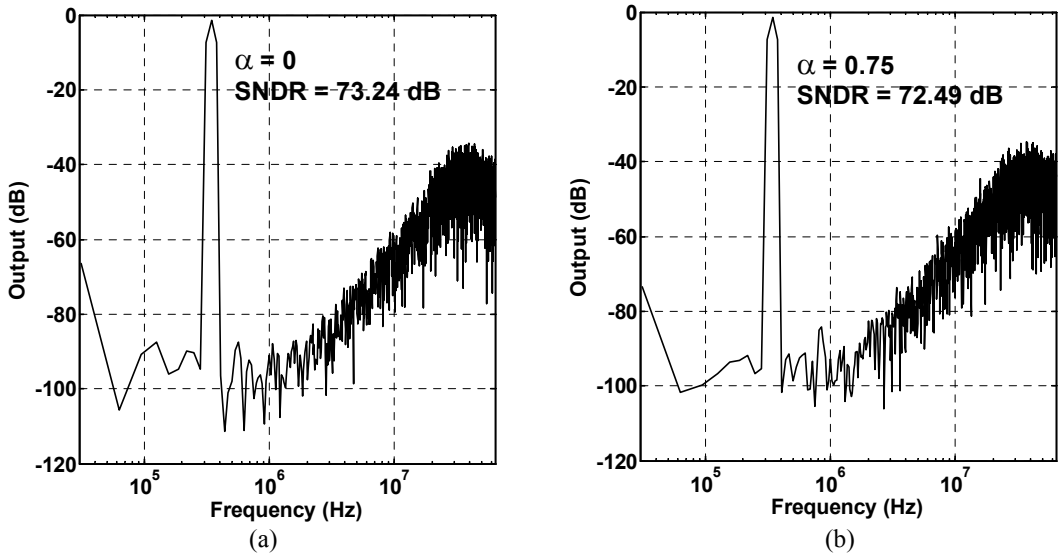


Figure 3.15: The output spectrum of the $\Delta\Sigma$ modulator in Figure 3.14, when the opamps have a switching ratio of: (a) $\alpha = 0$ (no switching); and (b) $\alpha = 0.75$.

3.6 Conclusion

A switchable-opamp technique was presented in this chapter for the low-power design of SC integrators as part of the low-power design of DT $\Delta\Sigma$ modulators as explained in Chapter 2. Compared to previous opamp-switching methods, the proposed technique is applicable to SC integrators with both full delay and half delay. Furthermore, it does not limit the operation speed of the SC integrator and does not require a special CMFB circuit while achieving reasonable power savings. Circuit Simulations confirmed the functionality and examined the performance of the proposed technique in SC integrators and DT $\Delta\Sigma$ modulators. In the next chapter, Chapter 4, we will continue in low-power SC solutions by looking into the power optimization of cascaded nondelaying SC integrators. The switchable-opamp technique proposed in this chapter will be implemented in the circuit-level design of the experimental $\Delta\Sigma$ modulator, presented in this thesis, in Chapter 6.

Chapter 4

Settling of Nondelaying Cascaded Switched-Capacitor Integrators

THE GOOD SETTLING of switched-capacitor SC integrator output is crucial for proper and linear operation. In the design of DT $\Delta\Sigma$ modulators, such as the one to be presented in this thesis, the proper settling is critical for the performance of the whole system. In most cases, each SC integrator stage is allocated at least half a clock cycle to settle properly, then its output is sampled by the subsequent stage. In some cases, nondelaying cascaded SC integrators might have to settle simultaneously. This can happen in closed-loop systems (i.e. delta-sigma modulators). While cascading more than two nondelaying SC integrators is not recommended to avoid the settling of more than two opamps in series [Ham04b], cascading two nondelaying SC integrators is a possible design decision. In addition to the loading effect the second SC integrator stage has on the first one, cascading two systems, each modeled by a single-pole filter, results in a two-pole system that needs to be power-optimized.

This chapter focuses on the design of two nondelaying cascaded SC integrators[Har13b] as part of the low-power design of DT $\Delta\Sigma$ modulators as presented in Chapter 2. A design method is proposed which optimizes the power consumption for a given settling accuracy. Another issue is also addressed concerning a possible excitation case that might lead to settling "hesitation" in two nondelaying cascaded SC integrators which affects settling accuracy. Circuit simulations confirm the analytical methods and simulations. The proposed analytical equations can be easily embedded into behavioral models used for large system's simulations

in early design stages. Section 4.1 starts with an overview of the problem to be discussed in this chapter. Section 4.2 then reassesses the way to tackle the design of two nondelaying cascaded SC integrators. Section 4.3 focuses on the glitch problem and suggests a solution to this issue. Section 4.4 presents a circuit design example to validate the results based on analytical equations.

4.1 Overview

Figure 4.1 depicts two cascaded SC integrators. If switches S_x, S_y, and S_z are controlled by the same clock phase (ϕ_2), then both integrators perform the charge-transfer simultaneously and they have to settle within the allocated settling time. Figure 4.2 shows a simplified representation of both integrators during the charge-transfer phase (ϕ_2) assuming a nondelaying cascaded configuration. The step shown at input V_1 represents a possible reference signal V_{ref} or the charge previously sampled on sampling capacitor C_{S1}. Both V_2 and V_3 suffer from some settling errors (discussed in Section 3.5.1) at the end of the allocated settling time. Since ensuring the required accumulated settling accuracy at the output of the second stage V_3 automatically ensures it also at the output of the first stage V_2, we will focus on the accumulated settling error at V_3.

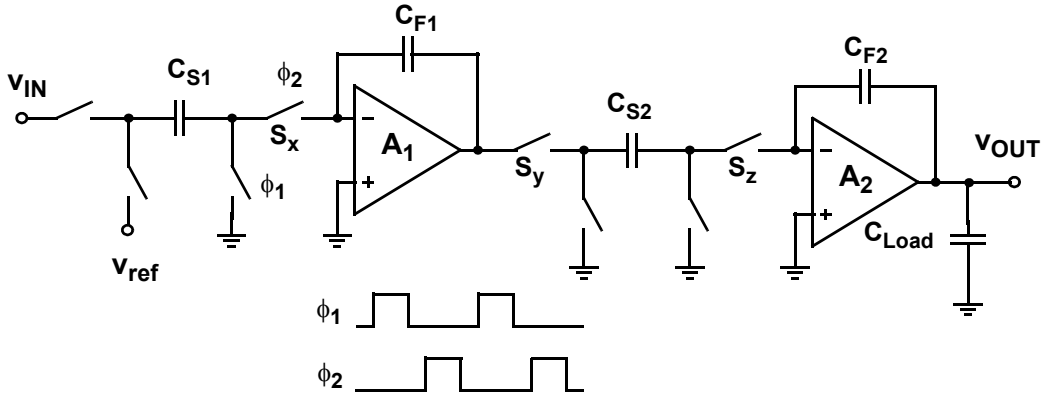


Figure 4.1: Two cascaded SC integrators with their non-overlapping clock phases (ϕ_1) and (ϕ_2).

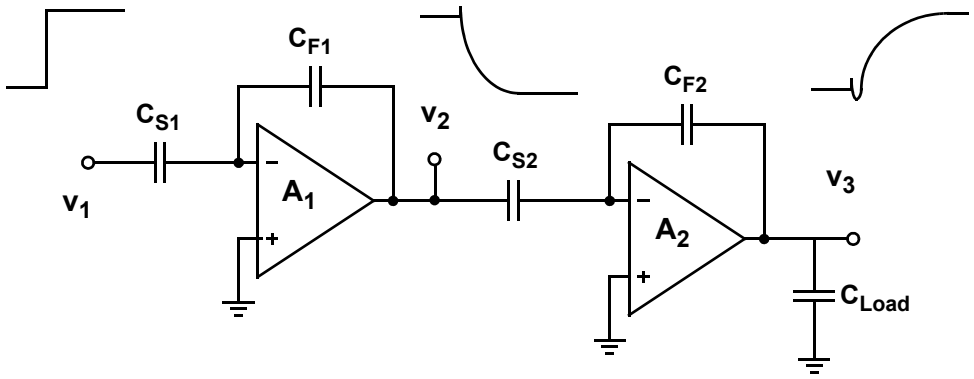


Figure 4.2: Two nondelaying cascaded SC integrators during the charge-transfer phase (ϕ_2) and the corresponding voltage waveforms for a step input.

4.2 Power Optimization of two cascaded nondelaying SC integrators

Typically, the design of SC integrators is carried out stage by stage to achieve a given settling accuracy in each and every stage. Using a simple single-pole model for the SC integrator [Rio00, Mal03], and assuming a targeted accumulated settling accuracy of 95% at the output of the second integrator V_3, a 3.75τ (τ being the closed-loop time constant) settling time should be allocated for both integrators to achieve 97.7% settling accuracy for each stage separately. This approach is only correct if settling occurs independently. But, for two nondelaying cascaded integrators (Figure 4.2), a two-pole system should be considered to account for the simultaneous settling. Quick analytical calculations for such a system, with each pole located as above (3.75τ available settling time), result in a settling accuracy of 89% instead of the targeted 95% at V_3.

Consider the model described in [Ham06] for each integrator in Figure 4.2 with the following assumptions:

1. **Opamp:**
   - Single-stage with one dominant pole.
   - Infinite DC gain (to focus on settling errors due to dynamic effects).

- Short-circuit transconductance $G_{mi} = KI_{DDi}$, $i = 1, 2$.
- Finite unity-gain bandwidth $\omega_{ti} = (\frac{G_{mi}}{C_{Li}})$, $i = 1, 2$.
- Infinite slew-rate (for simplicity).

where K is a constant depending on the opamp design, I_{DDi} is the opamp's current consumption, and C_{Li} is the equivalent open-loop capacitive load.

2. **SC integrator:**

   - Single-pole (integrator's 3dB bandwidth) $\omega_{3dBi} = \beta_i\ (\frac{G_{mi}}{C_{Li}})$, $i = 1, 2$.
   - Right-hand-plane zero $\omega_{Zi} = (\frac{G_{mi}}{C_{Fi}})$
   - Integrator gain $K_{Ii} = -(\frac{C_{Si}}{C_{Fi}}) = -1$, $i = 1, 2$. (for simplicity),

     where $\beta_i = \frac{C_{Fi}}{C_{Fi}+C_{Si}}$ for $i = 1, 2$ is the integrator's feedback factor, C_{Fi} is the integrator's feedback capacitor, and C_{Si} is the integrator's sampling capacitor.

     We have:

$$N_{\tau i} = \frac{T_{set}}{\tau_i}, \quad i = 1, 2. \tag{4.1}$$

$$N_{\tau i} = T_{set}\ \omega_{3dBi}, \quad i = 1, 2. \tag{4.2}$$

$$N_{\tau i} = T_{set}\ \beta_i\ (\frac{G_{mi}}{C_{Li}}), \quad i = 1, 2. \tag{4.3}$$

   where $N_{\tau i}$ is the number of time-constants available for settling, T_{set} is the available settling time for each opamp, and τ_i is the closed-loop (integrator's) time constant.

In the design of the opamp to be used in the two SC integrators (Figure 4.2), choosing the opamps short-circuit transconductance (G_{mi}) is directly linked to the closed-loop bandwidth (ω_{3dBi}) required to achieve a given settling accuracy. The design problem comes down to what is the minimum power (current) consumption required to achieve the targeted settling accuracy (or error). The settling error, in response to an input step, can be calculated analytically from the linear equations of a two-pole two-zero system. The relative settling error at V_3 is found to be a function of $N_{\tau i}$ and $(\omega_{3dBi}/\omega_{Zi})$ ratio of both integrators.

Figure 4.3 depicts a 3D plot showing how the relative settling error changes with respect to both $N_{\tau 1}$ and $N_{\tau 2}$ assuming that $(\omega_{3dBi}/\omega_{Zi}) = 0.2$ for both integrators.

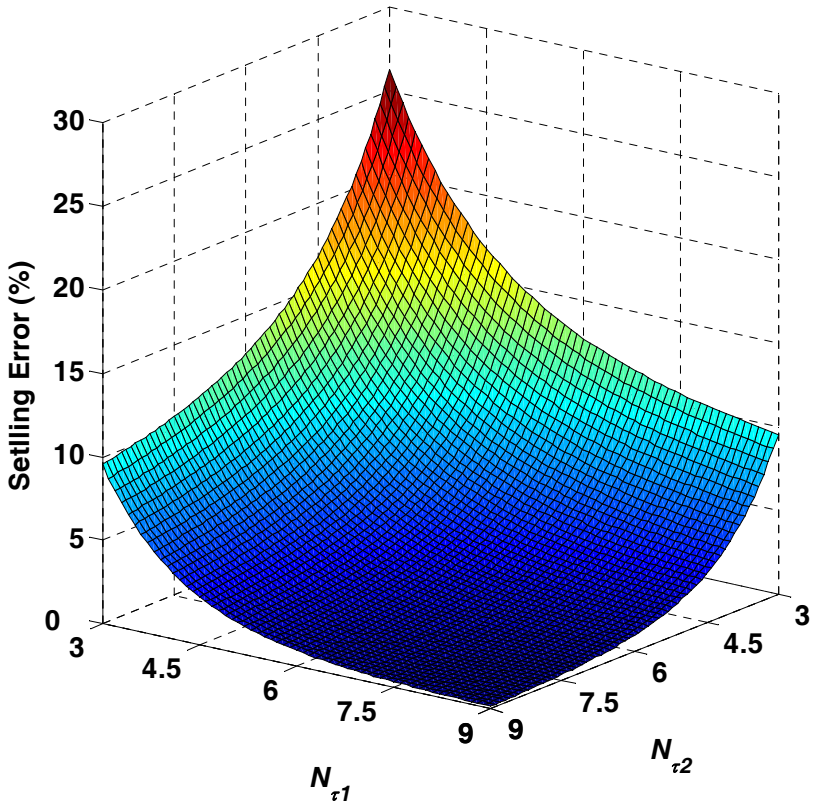


Figure 4.3: A 3D plot showing how the V_3 relative settling error, for a unit step in cascaded SC integrators, changes with $N_{\tau 1}$ and $N_{\tau 2}$.

Looking into the contours of the 3D plot shown now in Figure 4.4, each curve represents the possible combinations of ($N_{\tau 1}$, $N_{\tau 2}$) that give the same settling error with the same assumptions used for Figure 4.3.

Assuming that the two opamps share identical topologies and that the transistor widths in each opamp are scaled proportionally with the required currents to keep the DC gain constant, finding the optimum short-circuit transconductance G_{m1} and G_{m2} is not straightforward as both β_i and C_{Li} are assumed to be different for each opamp. The design goal is to get the minimum total opamps current consumption $I_{DD_{total}}$ that achieves the required settling error.

Starting from the total current consumption:

$$I_{DD_{total}} = I_{DD1} + I_{DD2} \tag{4.4}$$

$$I_{DD_{total}} = \frac{G_{m1}}{K} + \frac{G_{m2}}{K} \tag{4.5}$$

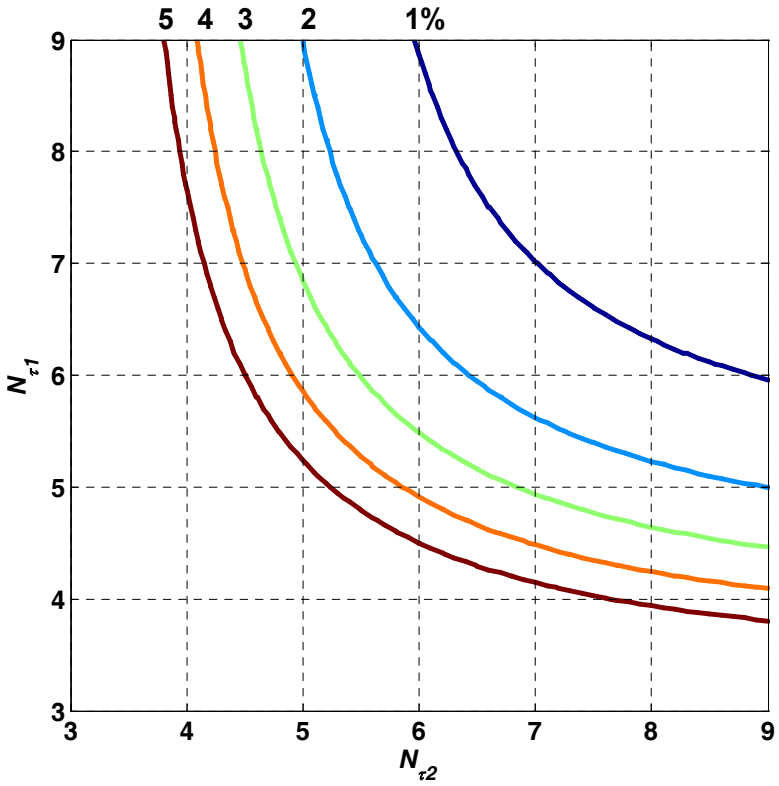


Figure 4.4: Contour lines representing constant V_3 percentage error (1-5%) for various ($N_{\tau 1}$, $N_{\tau 2}$) combinations.

$$KI_{DD_{total}} = \omega_{3dB1}(\frac{C_{L1}}{\beta_1}) + \omega_{3dB2}(\frac{C_{L2}}{\beta_2}) \tag{4.6}$$

$$KI_{DD_{total}} = (\frac{N_{\tau 1}}{T_{set}})(\frac{C_{L1}}{\beta_1}) + (\frac{N_{\tau 2}}{T_{set}})(\frac{C_{L2}}{\beta_2}) \tag{4.7}$$

$$KT_{set}I_{DD_{total}} = N_{\tau 1}\ (\frac{C_{L1}}{\beta_1}) + N_{\tau 2}\ (\frac{C_{L2}}{\beta_2}) \tag{4.8}$$

Solving for $N_{\tau 1}$:

$$N_{\tau 1} = N_\tau - N_{\tau 2}\ (\frac{a_2}{a_1}) \tag{4.9}$$

where

$$N_\tau = \frac{KT_{set}I_{DD_{total}}}{a_1} \tag{4.10}$$

and

$$a_i = (\frac{C_{Li}}{\beta_i}), \quad i = 1, 2. \tag{4.11}$$

The capacitor values are usually set by the thermal noise requirements in the system and by the system coefficients to be implemented. Given that the values of β_i and C_{Li} are already

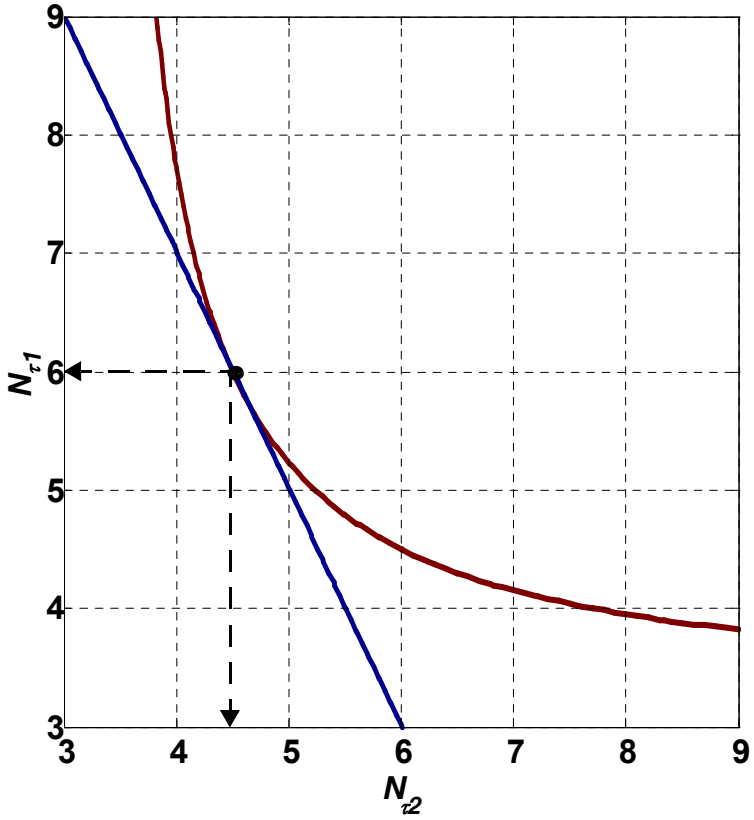


Figure 4.5: Intersection of contour line for 5% error with constant total current $I_{DD,total}$ line at $N_{\tau 1} = 6$ and $N_{\tau 2} = 4.5$.

set, the goal now is to get the minimum N_τ (i.e $I_{DD_{total}}$) in the linear equation given by (4.9) that gives a ($N_{\tau 1},\ N_{\tau 2}$) point which lies on the targeted error contour.

After picking the targeted error contour (5% for example as shown in Figure 4.5), we superimpose the line given by (4.9) with the given slope ($\frac{a_2}{a_1} = 2$ is assumed in this example) that is just tangent with the targeted error contour (i.e closest to the origin) to minimize N_τ (i.e $I_{DD_{total}}$). The intersection (tangent) point ($N_{\tau 1} = 6$ and $N_{\tau 2} = 4.5$ in this example) corresponds to the optimum solution. Then we can work backward from $N_{\tau i}$ to get G_{mi} and I_{DDi} for each opamp.

Considering the special case where both opamps see the same load and have equal feedback factors, then for a targeted settling error, one has to design very close to the case where $N_{\tau 1} = N_{\tau 2}$. This implies that both opamps should be designed to have equal closed-loop bandwidth (ω_{3dBi}) and hence equal short-circuit transconductances (G_{mi}).

4.3 Settling Glitch "Hesitation"

Typically, during the design for good settling, a unit step, with the maximum actual value in the system, is assumed to account for the worst case scenario. When designing two nondelaying cascaded SC integrators (Figure 4.2), there are cases that should be considered in the design. In closed-loop systems, such as delta-sigma modulators, the system feedback signal tends to track the system input signal which leads to a difference signal that has an oscillatory nature that reverses polarity frequently.

When considering the initial state of the first SC integrator V_2 to be non-zero (more specifically with opposite polarity), a settling "hesitation" can occur in the second SC integrator which leads to a glitch at its output V_3.

The analytical equations used in Section 4.2 to calculate V_3 settling error can be adjusted to account for the initial state of V_2. Figure 4.6b shows an example of this case where the initial state of V_2 is assumed to be 1 (normalized). With an input step of 2 at V_1, V_2 changes from 1 to -1 (integrator gain is assumed to be -1). Regardless of the initial state of the second integrator (assumed here to be 0), V_3 initially starts to move towards -1 (integrator gain is assumed to be -1). But, V_2 dynamically changes towards -1 which leads to a significant glitch in V_3 before reaching 1. This settling "hesitation" consumes some time which directly affects the final settling error and can lead to distortion since the error is dependent on the first integrator's initial state.

Figure 4.6a shows the various waveforms for a standard input step with no "hesitation". It is clear that V_3 settling error, sampled at $2ns$ in this example, in the hesitation case (9.4%) is higher than in the standard step case (5.1%). Although the probability of occurrence of this special case might not be high, it can limit the linearity of nondelaying cascaded SC integrators as being the worst case settling scenario.

Increasing the opamp's G_m, and hence the opamp's current consumption, might be necessary to decrease the V_3 settling error in this case. Taking finite slew-rate (SR) into account, the settling might become worse if slewing happens due to this glitch, which might force the designer to further increase the opamp's SR, and hence the current consumption, to avoid distortion in this particular case.

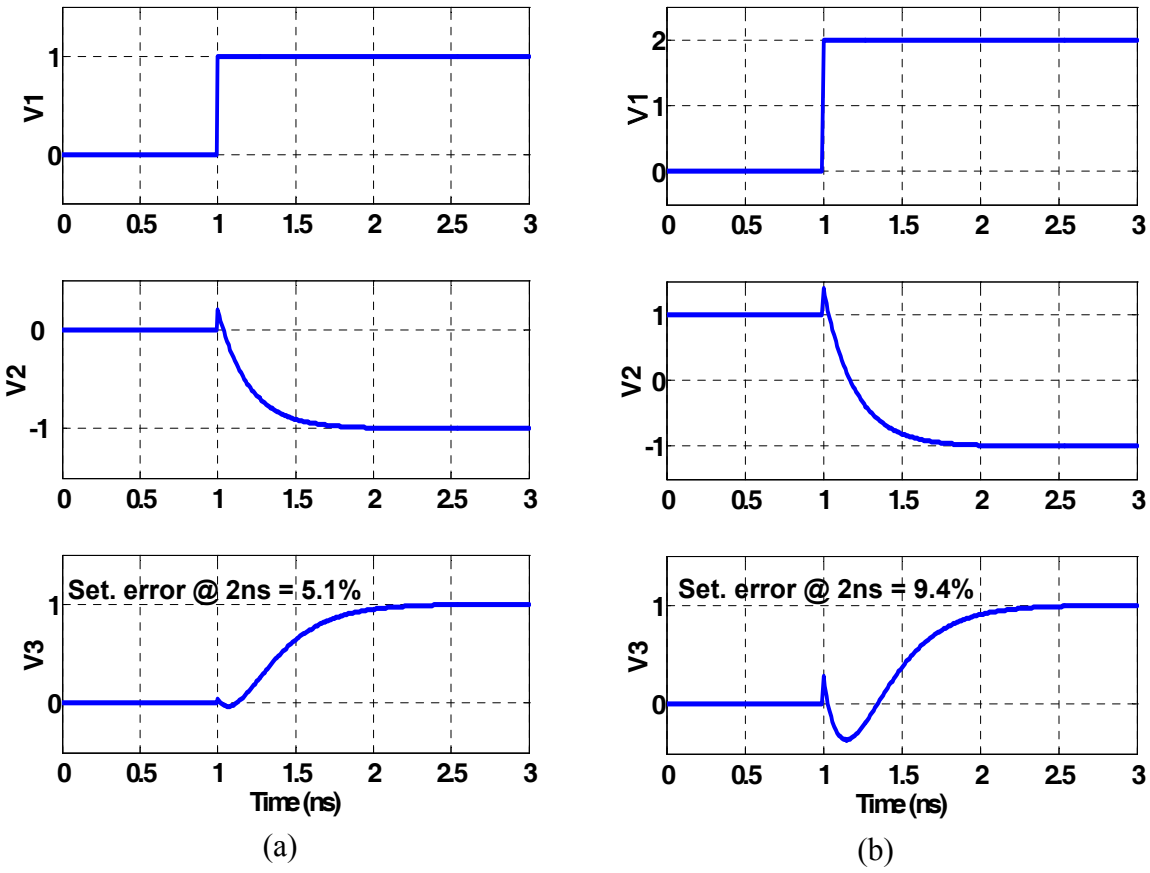


Figure 4.6: The nondelaying cascaded SC integrators waveforms V_1, V_2, and V_3 with: (a) standard input step; (b) excitation creating the "hesitation" at V_3

One possible solution to avoid increasing the opamp's current consumption much is to introduce some delay between the first and second integrator to allow for the output of the first integrator to adjust polarity to avoid the "hesitation" of the second stage. Figure 4.7 depicts how a small delay can eliminate most of this glitch and hence decrease the error. It is important to note that the normal excitation step (with no hesitation) should be checked after adding the delay to know the effect of this delay on the settling in the normal case.

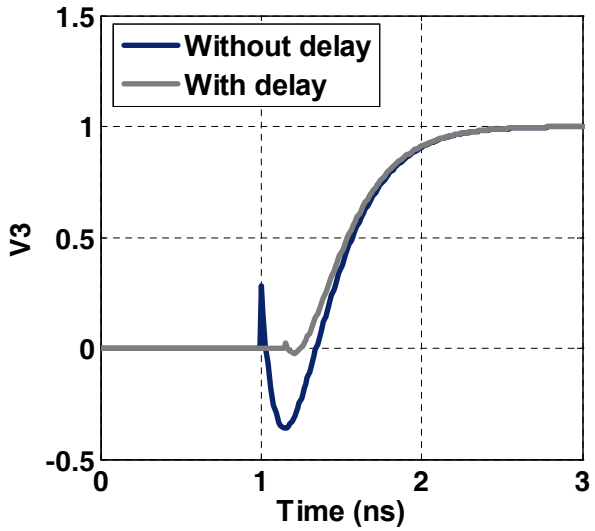


Figure 4.7: Effect of delay introduced between integrators on the settling of V_3 when "hesitation" occurs (Matlab simulations).

4.4 Circuit Design Example

To strengthen the discussions presented in the two previous sections, we will consider a circuit design example for two nondelaying cascaded SC integrators (Figure 4.2). Assume that from a higher system level design, we have:

$$C_{S1} = C_{F1} = C_{S2} = C_{F2} = 8pF \tag{4.12}$$

$$C_{load} = 2pF \tag{4.13}$$

$$T_{set} = 4.5ns \tag{4.14}$$

Then we have:

$$K_{I1} = K_{I2} = -1 \tag{4.15}$$

$$\beta_1 = \beta_2 = 0.5 \tag{4.16}$$

$$C_{L1} = \frac{C_{S1}C_{F1}}{C_{S1} + C_{F1}} + C_{S2} = 12pF \quad \text{and} \quad C_{L2} = \frac{C_{S2}C_{F2}}{C_{S2} + C_{F2}} + C_{load} = 6pF \tag{4.17}$$

$$(\omega_{3dB1}/\omega_{Z1}) = 0.33 \quad \text{and} \quad (\omega_{3dB2}/\omega_{Z2}) = 0.66 \tag{4.18}$$

Assume that the targeted V_3 settling error due to dynamic effects (finite BW) is 2%. A fully-differential current-mirror opamp [Joh97], designed in 1-V 65-nm process, is going to be used. It has an input to output current mirror ratio of 4 and a DC gain of $180V/V$. The short-circuit transconductance $G_m = 32mS$ for a supply current $I_{DD} = 7.2mA$ when all the transistor widths are scaled by a factor $n = 6$. All currents should be scaled proportionally with all widths to keep the DC gain constant and scale G_m up and down in steps.

Following the analytical design procedure given in Section 4.2, we have to design such that $N_{\tau 1} = 5.9$ and $N_{\tau 2} = 7.7$. This corresponds to $G_{m1} = 31.5mS$ abd $G_{m2} = 20.5mS$. Moving to actual circuit simulations, with a setup as shown in Figure 4.2 and applying a unit step of $100mV$, we see a static settling error (due to finite DC gain) [Ham04b] of about 2% at output V_3 in addition to the settling error due to finite opamp BW. We will extract the settling error due to dynamic effects (finite BW) only. The opamps' current scale ratios that meet the 2% targeted settling error and with (G_{m1}/G_{m2}) ratio close to the one suggested by analytical design method are listed in Table 4.1:

Table 4.1: Opamps' scale ratios, transconductances, and current consumptions.

	n	$G_m(mS)$	$I_{DD}(mA)$
Opamp 1	7	37.3	8.4
Opamp 2	5	26.7	6

The G_m values concluded from the circuit simulations are higher than the ones suggested by the analytical method to account for some circuit nonidealities. Circuit simulation shows a settling error of 1.98% for the opamp specifications listed in Table 4.1 which gives a total current consumption $I_{DD_{total}} = 14.4mA$.

To further check that this is the optimum solution, we can check other possible combinations keeping the total current $I_{DD_{total}} = 14.4mA$ and checking the corresponding errors. Table 4.2 reports the settling error variation for different current scales for both opamps given that $I_{DD_{total}} = 14.4mA$. It is clear that the solution listed in Table 4.1 gives the minimum settling error (optimum solution).

Table 4.2: V_3 Settling error variation, from circuit simulations, for different current scales with constant $I_{DD_{total}}$.

n_1	n_2	$G_{m1}(mS)$	$G_{m2}(mS)$	error (%)
5	7	26.7	37.3	3.05
6	6	32	32	2.22
7	5	37.3	26.7	1.98
8	4	42.7	21.3	2.25
9	3	48	16	3.5

Now assuming the excitation (described in Section 4.3) that creates the "hesitation" at the output of the second stage, the error jumps from about 2% to 2.3%. Applying a delay between the first and second stage of about 7% of the settling time ($0.3ns$), the error drops again just below 2%. Figure 4.8 depicts the circuit simulation results for the "hesitation" case without and with the $0.3ns$ delay applied.

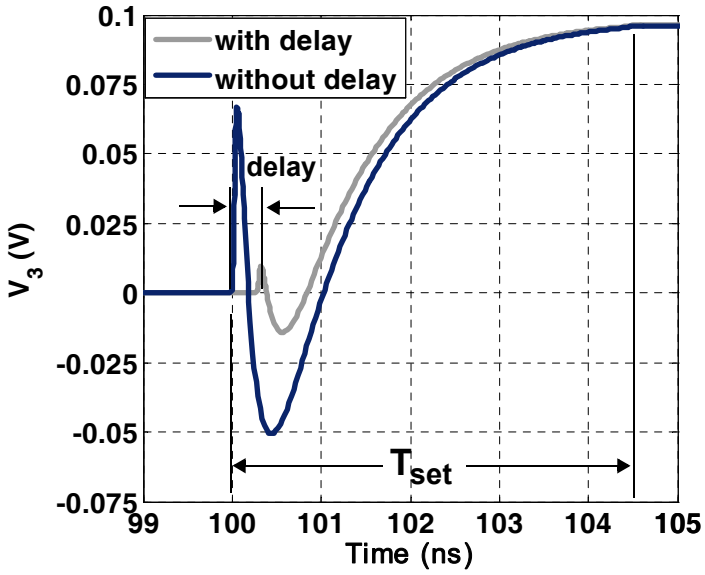


Figure 4.8: Circuit simulation results (1-V 65-nm CMOS process) showing the effect of adding $0.3ns$ delay between integrators on settling "hesitation".

This delay can be created by applying a delayed and narrower version of ϕ_2 on switch S_y (Figure 4.1). This modified ϕ_2 clock phase can easily be generated by simple logic circuits. It is worth noticing that this little delay fixes the error in the "hesitation" case while almost not having any effect on the error in the regular step case (remains below 2%).

4.5 Conclusion

A design method was presented in this chapter for two nondelaying cascaded SC integrators. Circuit simulation results validate the analytical method. These analytical equations can be easily modeled and used in behavioral simulations for larger systems. Moreover, the chapter addressed an important issue, confirmed by circuit simulations, that affects the design of two nondelaying cascaded SC integrators. In the low-power design of the DT $\Delta\Sigma$ modulator discussed in Chapter 5, we will encounter cascaded nondelaying SC integrators and we will follow the guidance presented in this chapter for a power-efficient design.

Chapter 5

System-Level Design of the Experimental $\Delta\Sigma$ Modulator

The low-power design of a $\Delta\Sigma$ modulator starts with the proper system-level design that allows a low-power implementation (by implementing for instance what was proposed in Chapter 3 and Chapter 4) while achieving the targeted specifications. The experimental $\Delta\Sigma$ modulator presented in this thesis is meant to digitize 8MHz baseband signals for digital TV applications fabricated in 1V 65nm CMOS process. Although the required resolution does not exceed 10 bits [Li05], a higher resolution relaxes other parts of the receiver.

This chapter presents a design procedure for system-level design, starting from picking an architecture, explored in Chapter 2, until deciding on various circuit parameters for the circuit design in the next chapter (Chapter 6). In this chapter we will also see how we can make use of the previously presented design procedure in Chapter 4 concerning cascaded nondelaying SC integrators.

Section 5.1 starts with the system-level design with ideal simulations. Section 5.2 explores the switched-capacitor structural-level aspects of the $\Delta\Sigma$ modulator under design. Section 5.3 then goes through the behavioral simulations carried-out incorporating various noise sources and circuit nonidealities and the procedure to determine the circuit design parameters.

5.1 System-Level Design

The input digital-feedforward (DFF) architecture in [Ham08b] is selected for the design of the required ΔΣ modulator for its potential low-power low-voltage-supply implementation in 1V 65nm CMOS digital process as explained in Section 2.4.1 and illustrated in Figure 2.10. Figure 5.1 depicts the experimental high-order multibit ΔΣ modulator with input DFF. With an 8MHz targeted bandwidth and 12-13 bits targeted resolution, a signal-to-quantization-noise ratio SQNR $\geq$ 86dB (14 bits) should be initially achieved assuming ideal components. The optimization design procedure, explained in Section 5.3.1, will confirm that the quantization noise should be well below ($\approx$ 10dB) the other noise sources (namely: thermal noise).

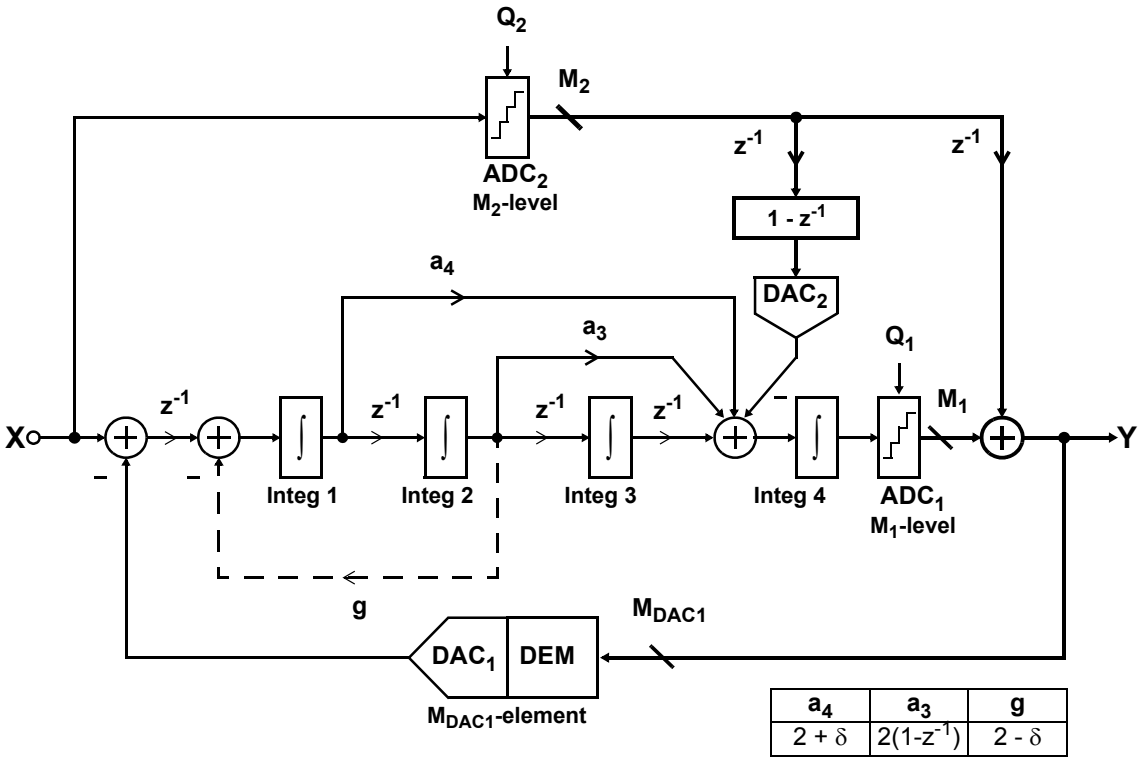


Figure 5.1: The experimental 4$^{\text{th}}$-order multibit digitally-enhanced ΔΣ modulator and the corresponding coefficient values for an FIR NTF. Here, the nondelaying integrator symbol $\int \equiv 1/(1-z^{-1})$.

This targeted SQNR can be achieved by:

- Oversampling ratio OSR = 8 which results in a 128MHz sampling rate. The OSR is selected to be on the low side to avoid settling complications due to high sampling rates (given the targeted bandwidth) and hence ensure efficient design in 65nm technology.

- Loop filter order N = 4. which gives about 8dB increase in SQNR compared to an order of 3. The real cost of a 4^{th}-order design compared to a 3^{rd}-order one is the added integrator 3 which consumes the least power due to sampling capacitor scaling while the first and last integrators are found to be the most power-hungry ones.

- Main quantizer ADC_1 internal resolution B $\geq$ 5 bits to ensure stability and achieve a high SQNR at low OSR. In this architecture, since ADC_1 is not processing the full signal swing and given the available signal swing at the output of the last integrator ($\approx 0.5V$ for a single stage opamp with cascode transistors with a 1V supply), $V_{ref,ADC1}$ is initially chosen to be $0.5V$. Observing the trade-off in choosing the number of levels M_1 in terms of the added complexity and the tightened comparator offset requirements, M_1 is chosen to be 24 which has an equivalent resolution of 5.5bits (for a 1V reference) resulting in a differential step size $\Delta_1 = 2\frac{V_{ref,ADC1}}{M_1} = 41.67mV$.

- Finite impulse response (FIR) noise-transfer-function (NTF) with optimum zero placement $(1-\delta z^{-1}+z^{-2})(1-z^{-1})^2$ [Ham04b, Sch05b], which increases the SQNR by about 10 dB for a $\delta = 1.9$ in Figure 5.1 compared to leaving all zeros at DC with an NTF of $(1-z^{-1})^4$. The addition of the g feedback path (dashed in Figure 5.1), to implement the optimum zero placement, has minimal kT/C noise contribution and minimal added loading effect on the first opamp. The coefficient values for an FIR NTF implementation are listed in Figure 5.1.

The extra quantizer ADC_2 reference voltage $V_{ref,ADC2}$ has to be maximized to maximize the input signal swing. Thus, $V_{ref,ADC2}$ is chosen to be 1V (V_{DD}). For correct digital addition, both quantizers are chosen to be mid-tread quantizers with step sizes related by $\Delta_2 = 2^k\Delta_1$,

for some integer k. Note that ADC_2 ends up working as a coarse quantizer and ADC_1 as a fine one. Setting $\Delta_2 = \Delta_1$ results in a total of 72 comparators and a low Q_2 that is easy to cancel. On the other hand, setting $\Delta_2 = 4\Delta_1$ results in a total of only 36 comparators and a potential leakage in Q_2 at the output of the ΔΣ modulator. It is a good decision to have $\Delta_2 = 2\Delta_1$ [Kwo06] which results in a total of 48 comparators. Hence, $M_2 = 24$ and $\Delta_2 = 2\frac{V_{ref,ADC2}}{M_2} = 83.33mV$.

DAC_1 step size Δ_{DAC1} has to be the smallest of Δ_1 and Δ_2 in order to conserve the resolution. Thus, $\Delta_{DAC1} = \Delta_1 = 41.67mV$. The DAC_1 reference voltage $V_{ref,DAC1}$ has to be maximized to maximize the feedback signal swing and hence the input signal swing. Thus, it would normally be set to 1V (V_{DD}) and $M_{DAC1} = 2\frac{V_{ref,DAC1}}{M_{DAC1}} = 48$. On the other hand, after the digital addition, without truncating any bits, the effective swing to be handled by DAC_1 implies that $V_{ref,DAC1} = V_{ref,ADC1} + V_{ref,ADC2} = 1.5V$ ($M_{DAC1} = 72$). Since the quantization noise from ADC_2 is cancelled in the addition, the actual required swing is less. Moreover, behavioral simulations show an actual maximum swing at the input of ADC_1 (shaped quantization noise) of about $0.3V$. $V_{ref,DAC1} = 1.33V$ ($M_{DAC1} = 64$) ensures that DAC_1 starts to saturate about the same time that ADC_2 starts overloading which also saves on DAC elements. This choice extends the maximum input signal amplitude from 0.8V (-2dBFS) to about 1V (0dBFS). The switched-capacitor implementation of such a reference voltage, exceeding V_{DD}, is explained in the next section.

DAC_2 step size Δ_{DAC2} has to be equal to Δ_2 for transparent operation. Thus, $\Delta_{DAC2} = \Delta_2 = 83.33mV$. DAC_2 reference voltage $V_{ref,DAC2}$ has to be equal to $V_{ref,ADC2}$ which is 1V (V_{DD}).

Table 5.1 summarizes the main design parameters of the experimental ΔΣ modulator. Figure 5.2 depicts the PSD for an ideal 4^{th}-order 5.5 bits ΔΣ modulator with DFF with an OSR = 8 and with the design details explained above for a 1V (0dbFS) amplitude sinusoid with 1.465MHz frequency simulated by SIMULINK®.

Table 5.1: Design parameters summary of the experimental ΔΣ modulator.

Parameter		Value
Sampling Frequency	f_S	128MHz
Input-Signal Bandwidth	f_{BW}	8MHz
Oversampling Ratio	OSR	8
Loop Filter Order	N	4
Internal resolution	B	5.5bits
ADC_1 Reference Voltage	$V_{ref,ADC1}$	0.5V
ADC_1 Levels	M_1	24
ADC_2 Reference Voltage	$V_{ref,ADC2}$	1V
ADC_2 Levels	M_2	24
DAC_1 Reference Voltage	$V_{ref,DAC1}$	1.33V
DAC_1 Levels	M_{DAC1}	64
DAC_2 Reference Voltage	$V_{ref,DAC2}$	1V
DAC_2 Levels	M_{DAC2}	24
Supply Voltage		1V
Maximum Input		2Vpp

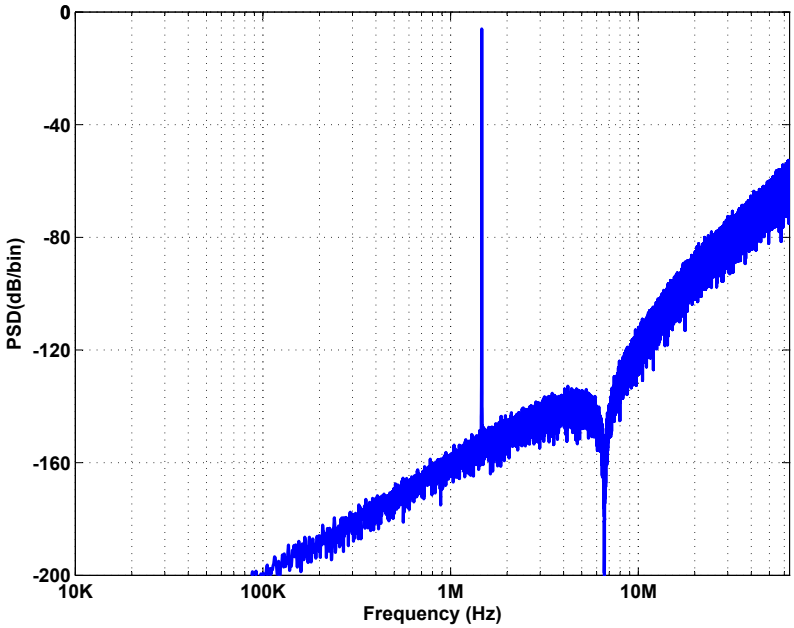


Figure 5.2: The PSD of the ideal 4^{th}-order 5.5 bits ΔΣ modulator for a 0dbFS 1.465MHz sinusoid simulated by SIMULINK.

5.2 Structural-Level Design

We will notice that there exists a critical path in the ΔΣ modulator shown in Figure 5.1. This path comprises the first (Integ_1) and last (Integ_4) integrators and is formed by Integ_1, a_4 feedforward path, Integ_4, ADC_1, the digital addition and dynamic element matching (DEM) in the feedback path and ending by DAC_1 which is part of Integ_1. All these blocks have to sequentially complete processing within one sampling period (shown as z^{-1} in front of Integ_1. In the light of what was discussed in Section 2.5, there are two possible approaches in this case, assuming the standard two non-overlapping clock phases:

1. Allocate a half-delay ($z^{-\frac{1}{2}}$) for each of Integ_1 and Integ_4 allowing them to settle independently and leave the addition and DEM processing to be completed in the non-overlapping period before sampling the feedback signal by DAC_1 (within Integ_1) (see Figure 2.11). In this case, although both integrators would have relaxed settling conditions, the non-overalpping time might not be enough for the digital processing especially at 128MHz sampling rate.

2. Force Integ_1 and Integ_4 to settle simultaneously in the same half-cycle and allocate the other half-cycle for the digital processing (see Figure 2.12). In this case, the time allocated for the digital processing might be overdesigned and wasted while the settling requirements are tightened on the integrators Integ_1 and Integ_4.

In both approaches the pre-amplification within ADC_1 is assumed to be done with Integ_4 settling and the latching within ADC_1 is done with the digital processing (addition and DEM). The second approach will be followed in this work, with unequal clock phases and optimized simultaneous settling for a more power-efficient design, as will be explained shortly.

5.2.1 Low-Power SC Implementation

Figure 5.3 depicts the full-system SC implementation of the experimental 4^{th}-order 5.5 bits ΔΣ modulator of Figure 5.1 in 1V 65nm digital CMOS process. The SC structure is operated by two non-overlapping clock phases, ϕ_1 and ϕ_2 and their delayed versions ϕ_{1d} and ϕ_{2d}. The SC circuit makes use of switch sharing to simplify the circuit and minimize the switch thermal

noise contribution. The figure also shows the main digital blocks (addition and DEM) as well as the two quantizers (ADC_1 and ADC_2).

The low-power SC implementation is ensured by two specific techniques; unequal clock phases, and optimized opamp simultaneous settling (Chapter4) [Har13b]:

1. **Unequal duty cycles for clock-phases:**

   Observing the SC loop filter in Figure 5.3, it is clear that A_1 and A_4 settle simultaneously during ϕ_2 while A_2 and A_3 settle independently during ϕ_1. Moreover, the digital addition and the DEM processing has to be performed during ϕ_1 and the non-overlapping time to ensure that the digital feedback signals are ready by ϕ_{2d} edge (Figure 5.3). Making ϕ_2 duty cycle (originally about 45%) greater than ϕ_1 duty cycle (originally about 45%) allows more settling time for A_1 and A_4 while making the ϕ_1 duty cycle just enough for digital processing. In this design, the ϕ_2 duty cycle was made twice as large as (now about 60%) the ϕ_1 duty cycle (now about 30%) which saves on A_1 and A_4 power consumption with a slight increase in A_2 and A_3 power consumption while making sure that the digital processing works fine. Given that A_1 and A_4 end up consuming more that 50% of the total modulator power consumption in this design (as will be shown in details in Chapter 6), this technique saves about 15% of the total modulator power consumption. The duty cycle could be optimized to reach the minimum overall power consumption. Although the modified duty-cycle was not optimized at this design stage, an external duty-cycle control and bias-current control, as will be explained in Chapter 6, can be used to achieve more power reduction (optimization).

2. **Optimized two-opamps simultaneous settling:[Har13b]**:

   The simultaneous settling of A_1 and A_4 in the cascaded nondelaying integrators scheme (a_4 feedforward path in Figure 5.1) has to be carefully designed. Instead of designing the settling of each opamp (A_1 and A_4) separately, one should look at it as a two-pole system that needs power optimization to get the targeted settling accuracy at A_4 output with the minimum power consumption (A_1 and A_4) as was explained in details in Chapter 4. This can be easily incorporated into the models and accounted for in behavioral simulations.

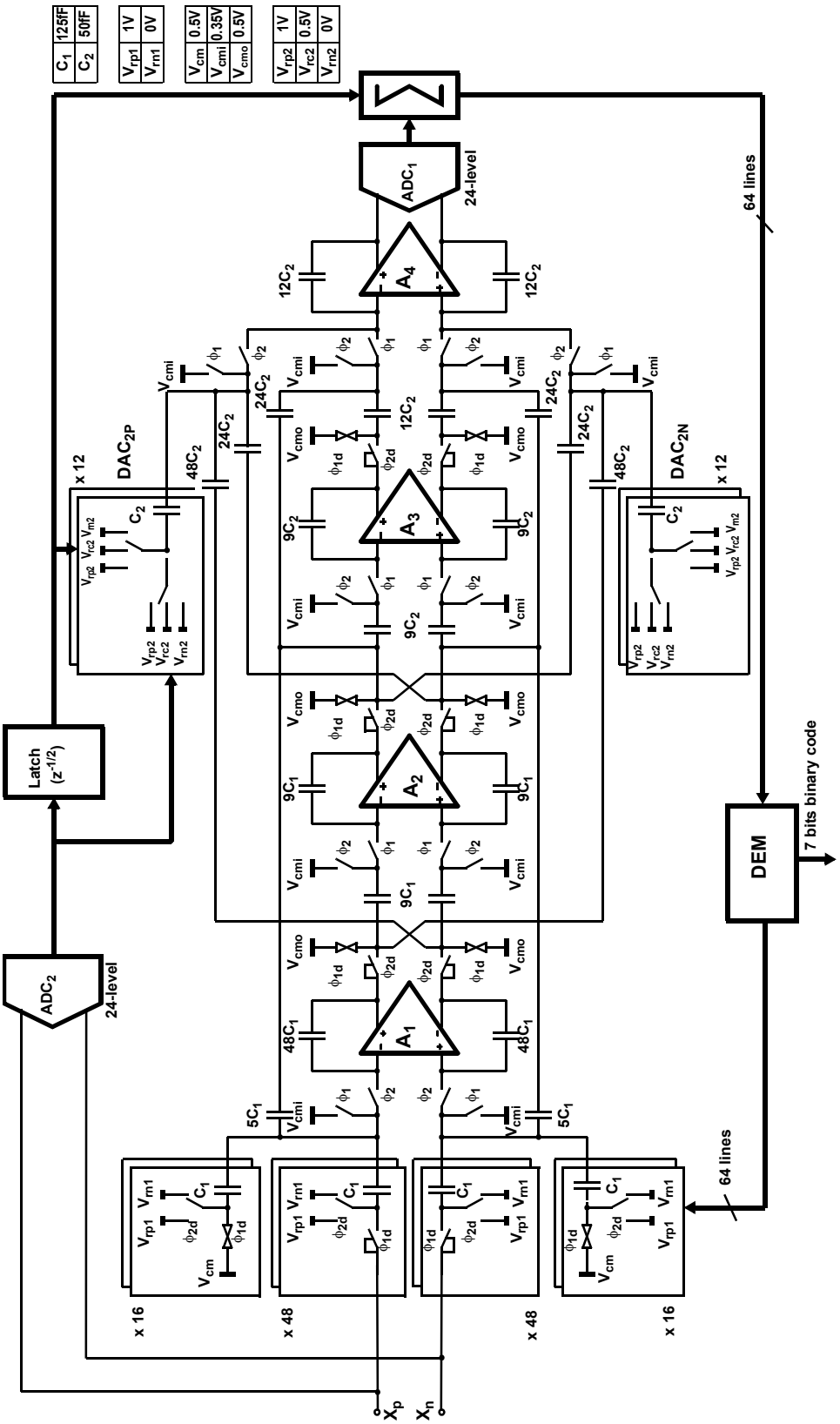


Figure 5.3: The full-system SC implementation of the experimental 4^{th}-order 5.5 bits $\Delta\Sigma$ modulator with DFF with the corresponding reference voltage and unit capacitor values.

Figure 5.3 shows the SC implementation of DAC_1 with a 16-element extra DAC that samples the feedback thermometer bits during ϕ_{2d} and samples zero-signal (V_{cm}) during ϕ_{1d} while the main 48-element DAC samples the feedback thermometer bits during ϕ_{2d} and samples the input signal during ϕ_{1d}. The equivalent $V_{ref,DAC1}$ of this implementation is $1V(\frac{48+16}{48}) = 1.33V$. This scheme extends the dynamic range (DR) by about 2dB. The added cost is a 1.24dB increase in kT/C thermal noise of the input switches of the first integrator and about 15% increase in the power consumption of the first opamp. The DAC_1 unit capacitor C_1 is set by kT/C noise requirements of the first integrator where $C_1 = C_{S1}/48$.

DAC_2 was implemented using 1.5-bit DAC elements for compact implementation and to allow for a larger DAC_2 unit capacitor to avoid mismatch problems. It uses 12 DAC elements to represent 24-level DAC. The DAC_2 unit capacitor C_2 is initially chosen to be 50fF (for good matching) putting a lower limit on C_{S4} of 0.6pF.

5.2.2 Structural-Level Simulations:

To make sure that the switching scheme as shown in Figure 5.3 is correct and achieves the loop transfer function correctly, structural-level simulations were carried-out using the SWITCAP® tool for linear switched capacitor networks. Figure 5.4 depicts the noise-transfer function (NTF) while Figure 5.5 shows the signal-transfer function(STF). They are both as expected; the NTF shows the noise shaping and a zero around 6MHz, and The STF with flat response (0dB) through the signal bandwidth.

5.3 Behavioral Simulations

SIMULINK® is used to perform behavioral simulations of the $\Delta\Sigma$ modulator with various circuit nonidealities and noise sources. The design problem now is to find the circuit parameters that achieve the targeted specifications. Ideal models are used for all the blocks then proper models incorporating nonidealities are used.

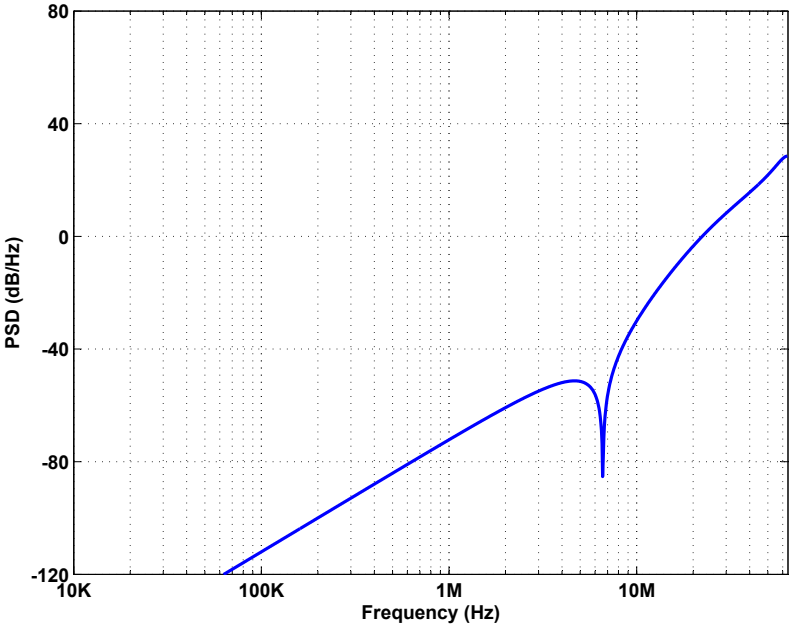


Figure 5.4: The NTF simulated by SWITCAP.

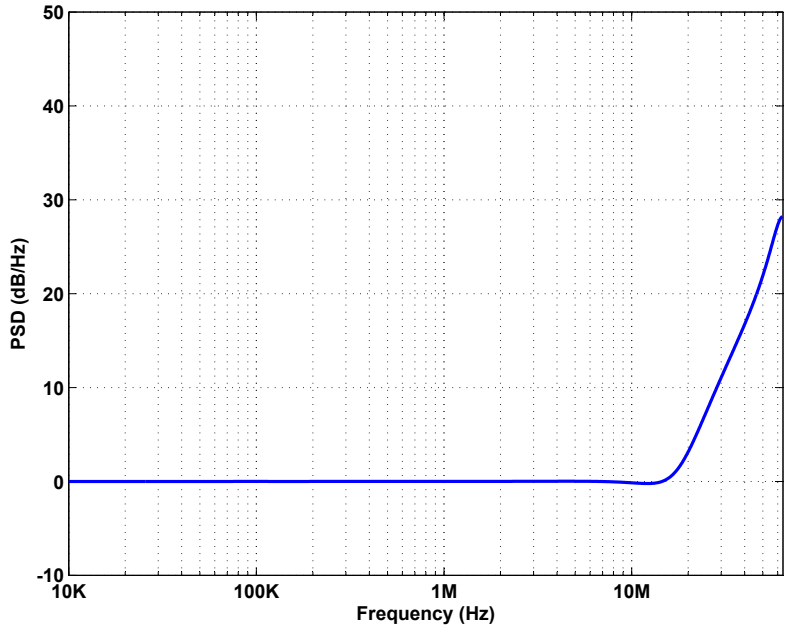


Figure 5.5: The STF simulated by SWITCAP.

5.3.1 Design Procedure

We will look now at the design procedure to find the circuit parameters that achieve the targeted specifications in the most power-efficient way possible.

1. Using ideal integrators models, we carry-out simulations to explore the signal swings at the output of the integrators (opamps):

   From the histogram of the integrators' output samples, Table 5.2 lists the maximum signal swings at the output of the opamps which is dominated by quantization noise.

   Table 5.2: Opamps' maximum output swing.

Opamp	1	2	3	4
Signal swing (mV)	±150	±100	±125	±300

2. Using integrators models with the effect of finite opamp DC gain (or nonlinear opamp DC gain), we run simulations to find the minimum required opamp DC gain for all the integrators:

   Table 5.3 lists the minimum required DC gain for the opamps. It is worth mentioning that the last integrator requires a slightly higher opamp DC gain for proper Q_2 cancellation. Q_2 cancellation that occurs in the digital addition relies on the good matching between the digital filter $(1 - z^{-1})$ and the SC integrator transfer function of the last integrator that is affected by its opamp DC gain.

   Table 5.3: Opamps' minimum required DC gain.

Opamp	1	2	3	4
Opamp DC gain (V/V)	100	100	100	125

3. Based on the signal swings and the required opamp DC gain, we decide on the suitable opamp topology for various integrators:

From Table 5.2 and Table 5.3 we can tell that a single-stage opamp would be enough since the gain requirement is not high and also the swing requirements allow cascoding transistors in 1V power-supply. The swing requirement of the last integrator is higher than the rest of the integrators, but the possible errors, due to distortion, at the output of the last integrator are shaped by the NTF and can be tolerated. Behavioral simulations with nonlinear opamp gain models should confirm the suitability of the selected topology. We prepare the models for finite bandwidth/slew-rate and thermal noise for the selected topology. Finite bandwidth and slew rate models are based on [Ham06] while the thermal noise (switch noise and opamp) models are based on [Sch05a]. From the models estimate the power consumption (as a function of the opamp BW) and model the power consumption of the rest of the system: ADCs and the digital blocks.

4. We perform a Figure-of-Merit (FoM) (given by 5.1) based optimization procedure that solves for the sampling capacitor values as well as the required opamp unity-gain bandwidth (bias currents) that gives the minimum FoM given that the resolution is $\geq$ 13bits (allowing more than 1bit room for circuit and real silicon nonidealities):

$$FoM = \frac{P_{total}}{2 \times f_{BW} \times 2^{(SNDRdB-1.76)/6.02}} \quad \text{(pJ/step)} \tag{5.1}$$

where P_{total} is the power consumpltion in mW, f_{BW} is the signal bandwidth in Hz, and $SNDRdB$ is the SNDR in dB.

   (a) Assuming that the system will be thermal noise dominated by the first opamp, we estimate C_{S1} by hand calculations given the targeted SNDR (SQNR with nonlinear gain models -6dB).

   (b) From the targeted initial FoM, we estimate the total power consumption. We put an initial power budget in which we allocate 1/3 of the power to the first opamp.

   (c) We add both finite bandwidth/slew-rate (BW/SR) and thermal noise models for the first opamp into the behavioral simulations. The first integrator load capacitance includes C_{S2} and C_{S4}. We assume that $C_{S2} = C_{S1}/2$ and C_{S4} =0.6pF (as explained in Section 5.2.1). Then, we sweep both C_{S1} and I_{BIAS1} until we get the optimum value for C_{S1} and the corresponding I_{BIAS1} that achieves the targeted SNDR (defined in step (a)).

(d) We add finite bandwidth/slew-rate and thermal noise models for the second opamp into the simulations and start sweeping C_{S2} from $C_{S1}/2$ and I_{BIAS2} from $I_{BIAS1}/2$ until we get the optimum value for C_{S2} and the corresponding I_{BIAS2} that achieves the targeted SNDR -0.3dB (6.67% drop in SNDR).

(e) We add finite bandwidth/slew-rate and thermal noise models for the third opamp into the simulations and start sweeping C_{S3} from $C_{S2}/2$ and I_{BIAS3} from $I_{BIAS2}/2$ until we get the optimum value for C_{S3} and corresponding I_{BIAS3} that achieves the targeted SNDR -0.6dB (another 6.67% drop, now 13% drop in SNDR).

(f) We add finite bandwidth/slew-rate and thermal noise models for the fourth opamp into the simulations. Then, we sweep C_{S4} $\geq$0.6pF and I_{BIAS4} and until we get the optimum value for $C_{S4} \geq$ 0.6pF and corresponding I_{BIAS4} that achieves the targeted SNDR - 1dB (another 6.67% drop, now 20% drop in SNDR).

(g) We estimate the total power consumption (opamps + ADCs + digital). We sweep I_{BIAS4} and C_{S4} $\geq$0.6pF independently then again by keeping I_{BIAS4}/C_{L4} constant until we get the minimum FoM value from the simulated SNDR as given by (5.1).

(h) We sweep I_{BIAS3} and C_{S3} independently then again by keeping I_{BIAS3}/C_{L3} constant until we get the minimum FoM.

(i) We sweep I_{BIAS2} and C_{S2} independently then again by keeping I_{BIAS2}/C_{L2} constant until we get the minimum FoM.

(j) We sweep I_{BIAS1} and C_{S1} independently then again by keeping I_{BIAS1}/C_{L1} constant until we get the minimum FoM.

(k) We repeat: Sweep I_{BIAS2} and C_{S2} independently then again by keeping I_{BIAS2}/C_{L2} constant until we get the minimum FoM.

(l) We repeat: Sweep I_{BIAS3} and C_{S3} independently then again by keeping I_{BIAS3}/C_{L3} constant until we get the minimum FoM.

(m) We sweep I_{BIAS4} and C_{S4} $\geq$0.6pF independently until we get the minimum FoM.

(n) Starting from the set of C_S and I_{BIAS} we have now, we sweep all C_S values (except C_{S4}) and change I_{BIAS} accordingly so that I_{BIAS}/C_L remains constant and get I_{BIAS4} for each set that gives the minimum FoM.

(o) Finally, we pick the solution that gives the minimum FoM from previous step. Steps from (j) to (m) can be repeated for more accurate results.

The accuracy of the results reached by this design procedure relies completely on the accuracy of the models used in the behavioral simulations. It is very important to capture all the major opamp nonidealities and noise sources. It is also of critical importance to accurately model the power consumption of the other components in the system (ADCs, digital blocks) as they affect the FoM calculation.

Table 5.4 shows the sampling capacitor values suggested by behavioral simulations as well as the required opamp short-circuit transconductance values for proper settling. Note that the simultaneous settling of A_1 and A_4 was modelled into the behavioral simulations. Although the analytical analysis given in Chapter 4 gives a hint that $G_{m1} = 1.2\ G_{m4}$ for optimum simultaneous settling, considering the whole system in the power optimization procedure is enough to get optimum values for both G_{m1} and G_{m4} given that the simultaneous settling is modelled (here $G_{m1} = 1.17\ G_{m4}$). Moreover the values suggested by the design procedure in this section are higher than what is suggested by Chapter 4 procedure due to the consideration of the switches equivalent on-resistance in this chapter.

Table 5.4: Integrators' sampling capacitor values and required opamp short-circuit transconductance values.

Opamp	1	2	3	4
C_S (pF)	6	1.125	0.45	0.6
G_m (mS)	35	5	2.5	30

Figure 5.6 shows the PSD for the designed ΔΣ modulator with thermal noise models as well as finite BW/SR models for a 0dBFS input at 1.465MHz. Both SNR and SNDR are 87.6dB over the 8MHz bandwidth. The bump in the shaped quantization noise in Figure 5.6 compared to Figure 5.2 is due to the extra settling errors in a_4 path compared to a_{31} path and also due to nonlinear gain models.

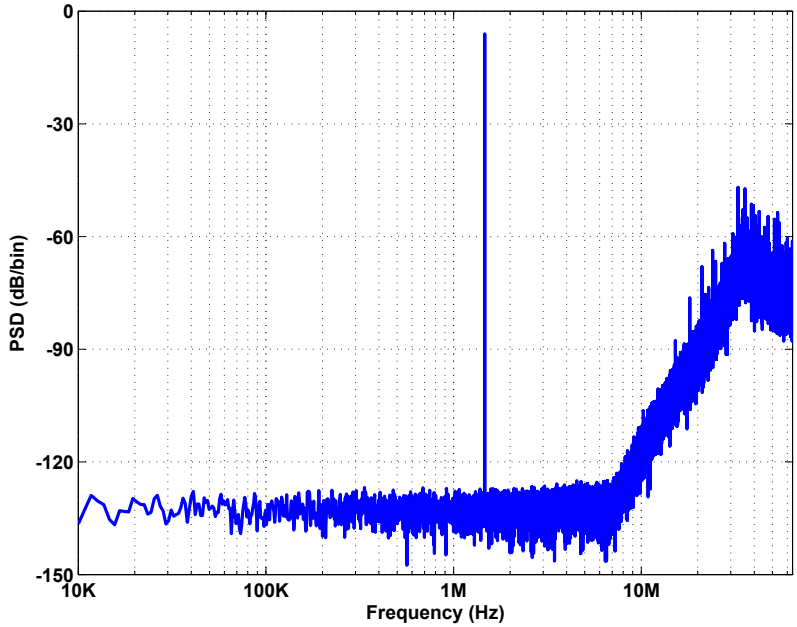


Figure 5.6: The output PSD of the $\Delta\Sigma$ modulator with thermal noise and finite BW/SR models for an input with 0dBFS at 1.465MHz.

5.3.2 DAC Nonlinearity

DAC capacitor mismatch was considered in behavioral simulations based on technology parameters. The TSMC 65nm GP 9M1P technology specifications give the standard deviation of the percentage mismatch between two metal-insulator-metal (MIM) capacitors in proximity as: $\sigma(\delta C/C)(\%) = 0.86/\sqrt{(Area)}$ where $Area$ is the capacitance area in μm^2. It also states that $C(\text{fF}) = 2(\text{fF}/\mu\text{m}^2) \times Area(\mu\text{m}^2)$, so that $\sigma(\delta C/C)(\%) = 1.22/\sqrt{(C(\text{fF}))}$. For the 125fF DAC_1 unit capacitor, the mismatch is 0.11%. To account for the distance between DAC elements, it will be assumed to reach 0.5% for DAC_1. Figure 5.7 shows the average PSD for a 50 run Monte-Carlo simulation with the capacitor mismatch assuming nonlinear opamp models for the integrators. As expected, DAC_1 needs DAC linearization. Among dynamic-element-matching (DEM) techniques, data-weighted-averaging (DWA) was found to be sufficient for proper DAC linearization as shown in Figure 5.8 depicting the average PSD for a 50 run Monte-Carlo simulation with DWA applied.

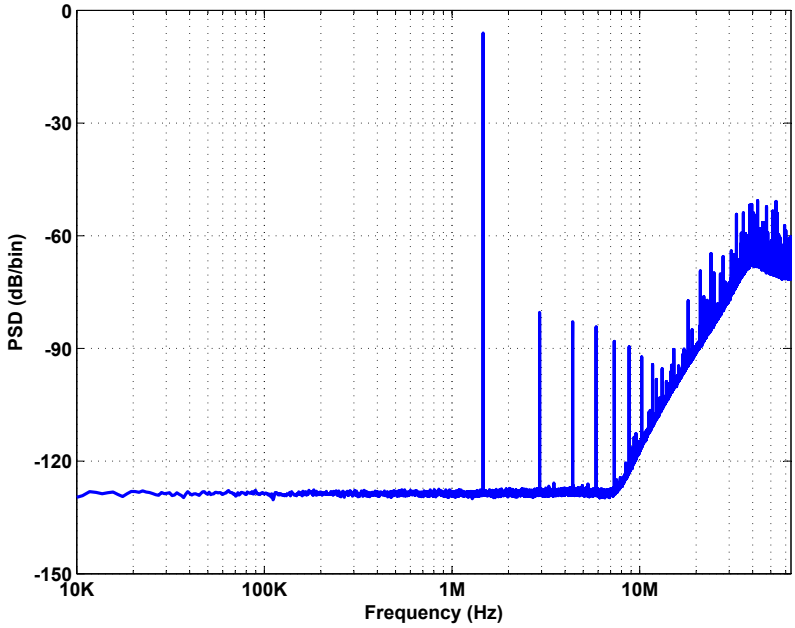


Figure 5.7: The average PSD for a 50 run Monte-Carlo simulation with 0.5% capacitor mismatch in DAC_1 assuming nonlinear opamp models.

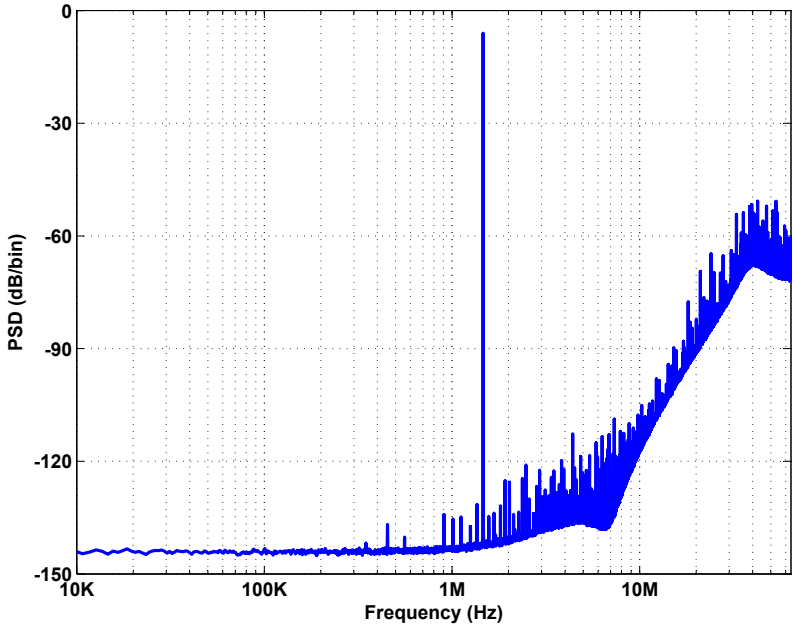


Figure 5.8: The average PSD for a 50 run Monte-Carlo simulation with 0.5% capacitor mismatch in DAC_1 assuming nonlinear opamp models with DWA applied.

DAC_2 has a 50fF unit capacitor, which gives 0.17% mismatch for two capacitors in proximity. Given that DAC_2 spans a smaller length than DAC_1, mismatch will be considered to be about 0.5%. As expected, DAC_2 mismatch is shaped by the loop filter and hence is found to have no effect on system performance. As a result, there is no need for any DAC linearization for DAC_2.

Figure 5.9 depicts the average PSD for 50 runs Monte-Carlo simulations for the designed $\Delta\Sigma$ modulator with the effect of various noise sources and circuit nonidealities, modelled in these behavioral simulations, for a maximum input sinusoid of 0dBFS at 1.465MHz. These behavioral simulations give an SNDR of 86.5dB over the 8MHz bandwidth. The estimated power consumption is about 22mA which leads to a FoM of 0.08pJ/step. Although this resolution at this design stage is around 14 bits, a margin is left for other circuit nonidealties that might arise in circuit level design as well as real silicon nonidealities so that we can achieve 12-13 bits resolution in the final measurements.

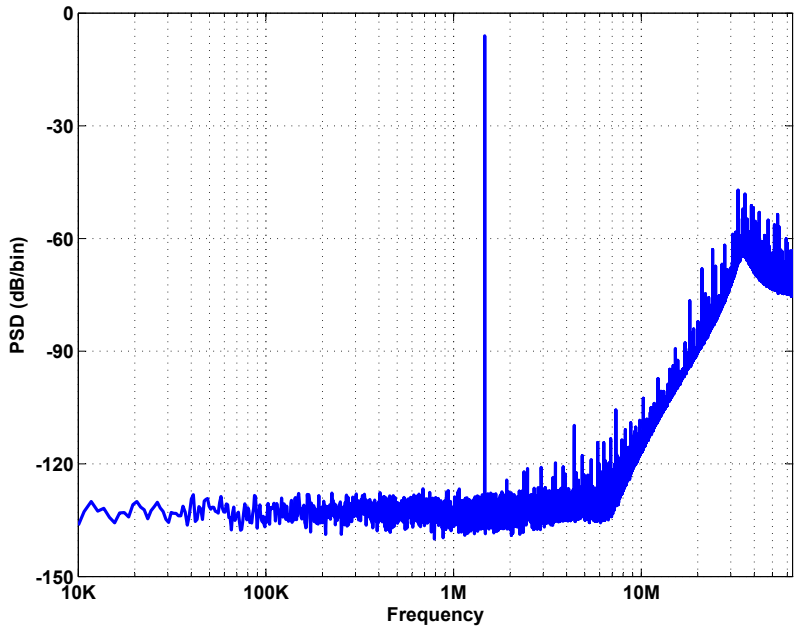


Figure 5.9: The average PSD for a 50 run Monte-Carlo simulation with 0.5% capacitor mismatch in DAC_1 and various nonidelaties and noise sources with DWA applied.

5.4 Conclusion

In this chapter, we explored both system-level and structural-level design procedures. Starting from system topology, we ended up with specific circuit parameters values (C_S, G_m, etc ...) passing by various design decisions including OSR, loop-filter order, internal resolution and other structural-level design decisions. We made use of what was presented in Chapter 4 concerning the settling of two cascaded nondelaying SC integrators. In the next chapter, we will take the design into the circuit-level design stage. Knowing initial values for the opamp required parameters, circuit simulations time can be saved.

Chapter 6

Circuit-Level Design of the Experimental $\Delta\Sigma$ Modulator

THE LOW-POWER DESIGN of a $\Delta\Sigma$ modulator relies on a power-efficient circuit-level design. Achieving the required specifications in a low-voltage-supply environment (1V) is the key challenge in the transistor-level design. In nanometer CMOS processes (65nm in this thesis), the analog properties of the transistors, such as intrinsic gain, becomes poorer due to technology scaling.

This chapter presents the design procedure of the various circuit building blocks in 1V 65nm CMOS process. Starting from the structural-level design addressed in the previous chapter (Chapter 5), this chapter will deal with the transistor-level design of the experimental $\Delta\Sigma$ modulator shown in Figure 5.3. Circuit simulations of the main building blocks are essential to verify their functionality. The implementation of the opamp-switching technique, presented in Chapter 3, is carried out in this chapter. Full-system circuit simulations can be carried out as a final verification before preparing a prototype for fabrication.

In Figure 5.3, the output common-mode voltage (V_{cmo}) is set to 0.5V ($V_{DD}/2$) to maximize the opamps output swing. The input common-mode voltage (V_{cmi}) is chosen to be 0.35V for proper biasing. The main analog components are the opamps, the comparators and the various switches. The main digital blocks are the adder, the Data-Weighted-Averaging (DWA) processor and the clock generator.

Section 6.1 starts with the design of the most power-hungry blocks: the opamps. Section 6.2 then goes over the design of the flash ADCs including the comparators and the resistor ladder. Section 6.3 addresses the design of the sampling switches as well as the DAC switches. Section 6.4 explores the design of the digital circuitry: the digital adder, the DWA processor, and the clock generator. Section 6.5 ends with full-system circuit simulations.

6.1 Operational Amplifier Design

The current-mirror opamp, depicted in Figure 6.1, is one of the common choices when driving on-chip capacitive-only loads [Joh97]. As a single stage opamp (along with the folded-cascode topology), the main disadvantage of the current-mirror opamp is the swing limitation due to cascode devices stacked for gain enhancement. Compared to the folded-cascode topology, the current-mirror opamp provides higher bandwidth and slew-rate for the same supply current at the expense of larger input referred noise [Joh97]. The current gain from input side to output side K (refer to Figure 6.1) provides a trade-off between speed and input-referred thermal noise without affecting the DC gain. Moreover, the opamp switching technique proposed in Chapter 3 is based on a current-mirror opamp [Har13a]. Given the swing reduction of the selected DFF ΔΣ architecture [Ham08b] and the power savings that could be achieved by the proposed switching technique, the current mirror opamp is selected for the design of the four opamps in this design. An initial estimate of the available output swing in a fully-differential current-mirror opamp operated from a $1V$ supply is about $\pm V_{DD}/2$ ($\pm 500mV$) which suits the required signal swings in Table 5.2. The design will be carried out by first not applying the switching technique, then the switching technique will be implemented with the proper switching ratio α maintaining the required performance while achieving power reduction.

The input differential-pair (M_1 in Figure 6.1) is chosen to be implemented as PMOS devices to minimize flicker ($1/f$) noise [Joh97]. The current-mirrors are implemented as wide-swing cascode current-mirrors (M_2, M_3, M_4, M_5 and M_{16}, M_{17}, M_6, M_7) to maximize the signal swing at the opamp output. The current-gain K value is a trade-off. Assuming a dominant pole at the opamp output due to large capacitive load, for a given total supply current I_{DD}, increasing K increases both the unity-gain bandwidth and the slew-rate while

it decreases the phase-margin and increases the input-referred thermal noise [Joh97]. In this design a K of 4 will be chosen, as will be explained shortly, to maximize both the unity-gain bandwidth and slew-rate for a good settling while making sure that the phase margin and the input-referred thermal noise are in their targeted (tolerated) ranges. The phase margin is actually tested by open-loop AC circuit simulations and step-response transient circuit simulations. The input-referred thermal noise density is calculated by circuit simulations and then checked by behavioral simulations.

Behavioral simulations and the design procedure carried-out in Section 5.3.1 concluded the required specifications as well as the loading conditions for all four opamps. The circuit design procedure for each opamp is as follows (given that the topology is already selected as a current-mirror opamp as explained earlier):

1. From the DC gain A_0 and the short-circuit transconductance G_m requirements, we use hand calculations with the equations in [Joh97] to estimate the required K, overdrive voltage V_{eff} for the input differential-pair and the differential-pair tail biasing current $2I_B$ (Figure 6.1).

2. Choosing initial transistor lengths as $2.5L_{min}$ for all except bottom and top current mirrors/sources transistors (for which we pick $1.5L_{min}$), we set and simulate the DC biasing with the biasing current from hand calculations.

3. We start simulating for DC gain, unity-gain bandwidth, phase margin, input-referred thermal noise, and output swing while watching the current consumption and using ideal biasing.

4. We adjust the DC gain to the targeted value with some margin (here about 150V/V) by proper sizing without changing currents. This can be done by increasing the cascode transistors length to increase the output resistance or by increasing input differential-pair transistors width.

5. To get the targeted G_m (or unity-gain bandwidth), we scale the biasing current everywhere along with the transistor widths. G_m is directly proportional to the biasing current in the output side.

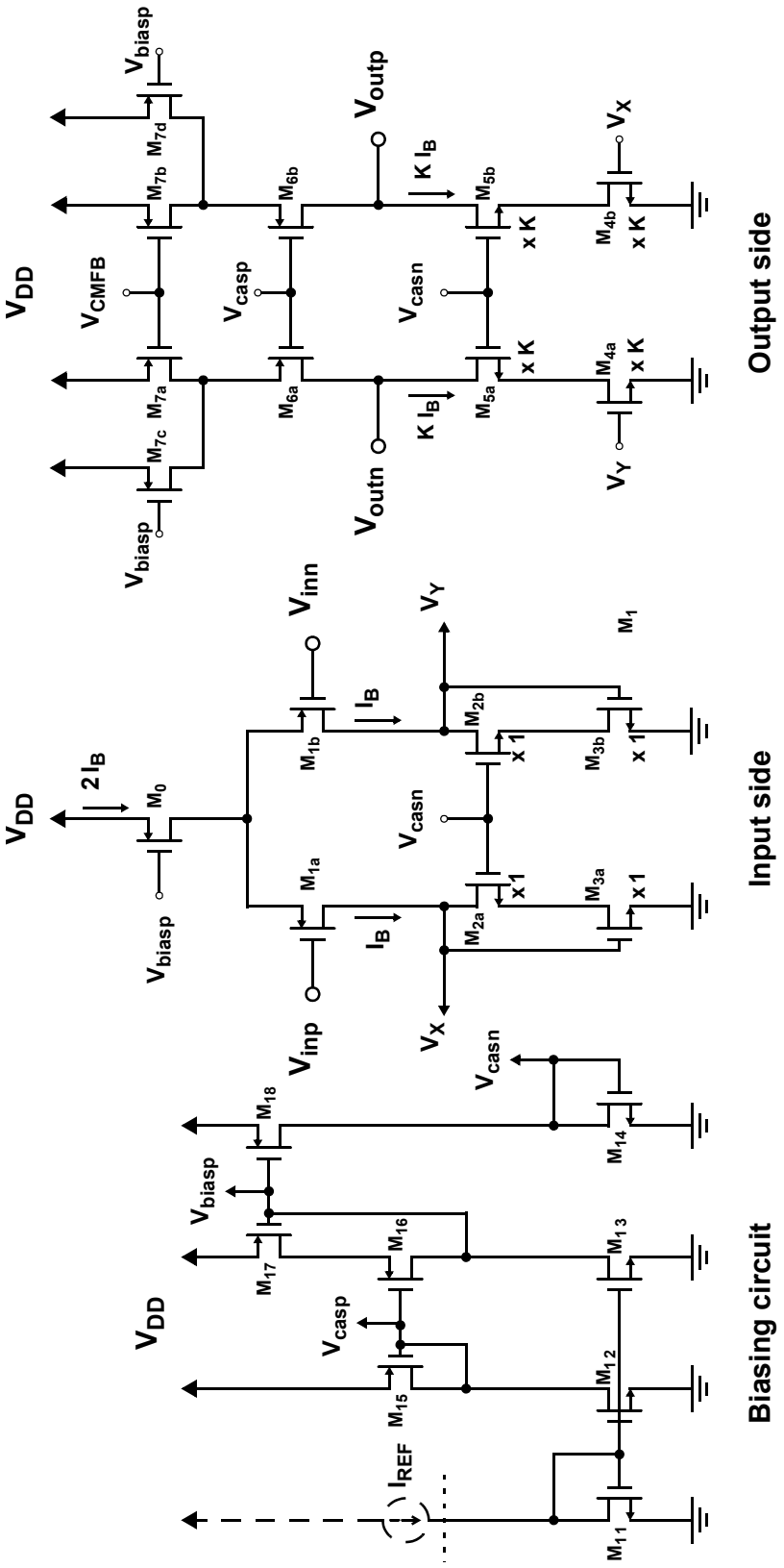


Figure 6.1: The used current-mirror opamp and the used biasing circuit. The common-mode feedback circuit is not shown in this figure. I_{REF} is implemented as an external biasing resistor and a current-mirror near the chip pads. V_{biasp}, V_{casn}, and V_{casp} connect from the biasing circuit to both sides of the opamp. V_x and V_y connect from the input side to the output side.

6. We watch and adjust the phase-margin by moving away the non-dominant pole to get at least 75^0 phase-margin. This can be done by changing the transistor lengths of the top and bottom current-mirrors/sources and by changing the current gain K.

7. We have to watch the input-referred thermal noise and insert it into the behavioral simulations to make sure it is acceptable. The opamp thermal noise (especially for the first integrator) adds to the switches thermal noise and other noise sources and determines the achievable SNR.

8. We can reiterate to get better solution while watching the current consumption. If we have more than one solution meeting the specifications, we should pick the one with the lower current consumption.

9. We then design the actual biasing circuit (Figure 6.1), and repeat the performance simulations for the different (process variation) corners making sure that the specifications stays in the targeted ranges.

10. Finally, we have to check the step response with the actual maximum swings for each opamp and watch the settling behavior as well as the settling error within the allocated settling time T_{set}. The settling error from circuit simulations can be compared to the settling error from behavioral simulations. The effect of the switches on-resistance R_{on} can be added to estimate the required R_{on}.

The transistor sizes of the different opamps are listed in Table 6.1 and the transistor sizes of the biasing circuits in Table 6.2. Both opamp 1 and 4 are designed to be the same to save design time. Opamp 2 ends up being designed as a scaled-down version of opamp 1 by a factor of about 4.5 due to sampling capacitor scaling from 6pF to 1.125pF. Opamp 3 is a scaled down version of opamp 2 by a factor of about 2. The simulated opamp specifications and current consumptions are listed in Table 6.3.

As we can see in Figure 6.1, M_7 is split in two halves; M_{7a} and M_{7b} are controlled by V_{CMFB} for common-mode feedback adjustments while M_{7c} and M_{7d} are controlled by constant bias voltage V_{biasp} to optimize transient response. The common-mode feedback (CMFB) circuit is implemented as a switched-capacitor (SC) CMFB circuit, as depicted in Figure 6.2

Table 6.1: Transistor sizes of the current-mirror opamps in Figure 6.1.

		M_0	M_1	M_2	M_3	M_4	M_5	M_6	M_7
opamp 1 and 4	$N_{fingers}$	30	40	9	7	28	36	80	34
	W $[\mu m]$	5	5	2.5	2.5	2.5	2.5	5	5
	L $[\mu m]$	0.12	0.15	0.15	0.12	0.12	0.15	0.15	0.12
opamp 2	$N_{fingers}$	14	8	2	2	8	8	16	8
	W $[\mu m]$	2.5	5	2.5	2.5	2.5	2.5	5	5
	L $[\mu m]$	0.12	0.15	0.15	0.12	0.12	0.15	0.15	0.12
opamp 3	$N_{fingers}$	13	8	2	2	8	8	16	8
	W $[\mu m]$	1.25	2.5	1.25	1.25	1.25	1.25	2.5	2.5
	L $[\mu m]$	0.12	0.15	0.15	0.12	0.12	0.15	0.15	0.12

Table 6.2: Transistor sizes of the opamp biasing circuits in Figure 6.1.

		M_{11}	M_{12}	M_{13}	M_{14}	M_{15}	M_{16}	M_{17}	M_{18}
opamp 1 and 4	$N_{fingers}$	2	2	2	1	1	5	4	4
	W $[\mu m]$	2.5	2.5	2.5	1.2	3.3	5	5	5
	L $[\mu m]$	0.15	0.15	0.15	0.15	0.15	0.15	0.12	0.12
opamp 2	$N_{fingers}$	1	1	1	1	1	6	5	5
	W $[\mu m]$	2.5	2.5	2.5	0.8	2	2.5	2.5	2.5
	L $[\mu m]$	0.15	0.15	0.15	0.15	0.15	0.15	0.12	0.12
opamp 3	$N_{fingers}$	1	1	1	1	1	6	5	5
	W $[\mu m]$	1.25	1.25	1.25	0.5	1	1.25	1.25	1.25
	L $[\mu m]$	0.15	0.15	0.15	0.15	0.15	0.15	0.12	0.12

to ovoid signal swing limitations and power dissipation found in continuous-time CMFB circuits. Capacitor sizes are listed in Table 6.4. The CMOS switch used in the CMFB circuit is designed to have about $1k\Omega$ on-resistance at 0.5V with the transistor sizes listed in Table 6.5.

The opamp switching technique proposed and explained in details in Chapter 3 is then implemented on the opamps by simply splitting transistors M_4 as shown in Figure 3.10 with a switching ratio α and adjusting M_7 split ratio to match the switching ratio α for simplicity.

Table 6.3: Opamps' loading conditions (capacitive load and feedback factor) and the simulated specifications.

Opamp	1	2	3	4
C_L (pF)	8.5	1.4	0.66	2.7
β	0.5	0.5	0.5	0.15
A_0 (V/V)	162	160	154	162
G_m (mS)	35	5.7	3.1	35
f_t (MHz)	667	749	732	1700
PM (^{0})	83	83	82	85
I_{DD} (mA)	7.3	1.6	0.7	7.3

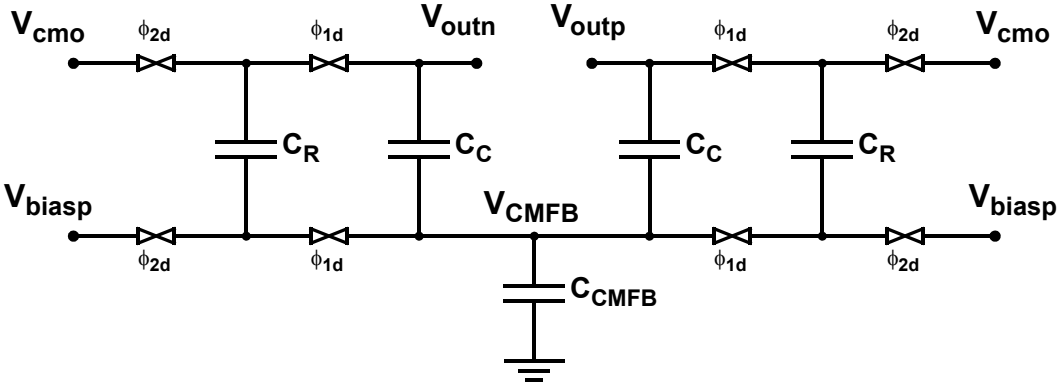


Figure 6.2: The used SC common-mode feedback (CMFB) circuit.

Table 6.4: Capacitor sizes in the SC CMFB circuits.

	Opamp1 and 4	Opamp 2	Opamp 3
C_C $[pF]$	1	0.5	0.25
C_R $[pF]$	0.25	0.125	0.0625
C_{CMFB} $[pF]$	0	0.125	0.0625

Table 6.5: Transistor sizes of the CMOS switch used for the CMFB circuit.

	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$R_{on}[\Omega]$
M_n	1	1.5	0.06	1000
M_p	3	1.5	0.06	

The cascode transistors M_5 and M_6 are not switched with M_4 and M_7 for simplicity and simulations prove that linearity is not affected. As listed in Table 6.6, an α of 0.5 is chosen for all opamps except for opamp 2 an α of 0.25 is chosen as it sees quite a big load during its sampling phase. The table also lists the current consumption in all opamps with no switching and the average current consumption when switching is implemented. A 16 % power saving is achieved in the total opamps currents without affecting the performance. A CMOS switch is used to connect V_{biasp} to the switching part of M_7 while a simple PMOS switch is used to switch it off. A CMOS switch is used to connect V_x and V_y to the switching part of M_4 while a simple NMOS switch is enough to turn it off. Component sizes used in the design of these switches are listed in Table 6.7.

Table 6.6: Power savings in opamps by implementing switching technique.

	Opamp1	Opamp 2	Opamp 3	Opamp 4	Total
α	0.5	0.25	0.5	0.5	
I_{DDNoSw} $[mA]$	7.3	1.6	0.7	7.3	16.9
$I_{DDSwAvg}$ $[mA]$	6.1	1.44	0.56	6.1	14.2

Table 6.7: Transistor sizes of the switches used to implement the switching technique.

		Opamp 1 and 4			Opamp 2 and 3		
		$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$
M_7	PMOS M_p	1	4	0.06	1	1	0.06
	CMOS M_p	3	4	0.06	4	1	0.06
	CMOS M_n	3	4	0.06	4	1	0.06
M_4	CMOS M_p	2	1.5	0.06	3	0.5	0.06
	CMOS M_n	2	1.5	0.06	3	0.5	0.06
	NMOS M_n	1	1.5	0.06	1	0.5	0.06

6.2 Flash ADCs Design

The flash ADC consists of a group of comparators and a resistive ladder to generate the comparator reference levels. The design focuses on meeting the offset requirements of the designed comparator and selecting a proper value for the unit resistance in the resistive ladder. In order to save design time, the same flash ADC designed for ADC_1 is reused for ADC_2 with only the ladder unit resistance value modified.

We use a differential switched-capacitor latched comparator with input-offset-storage (IOS) [Gre99]. It consists of a preamplifier, a regenerative latch, and a simple SR latch. As shown in Figure 6.3, the reference voltages and input-referred offset are sampled on C during one phase and the input signal is passed to the preamplifier during the other phase after subtracting the reference value and cancelling the offset (both stored on C). The preamplifier is reset during the reference-sampling phase by means of a unity-feedback connection. The preamplifier ensures attenuating the latch's input-referred offset [Gre99] as well as preventing kickback noise of the latch from entering the comparator's driving circuitry [Raz95]. The regenerative latch is usually a bistable multivibrator that tracks the amplified difference of the comparator and provides a large and fast output. The SR latch holds the digital output for the clock-cycle long even when the output of the regenerative latch is reset.

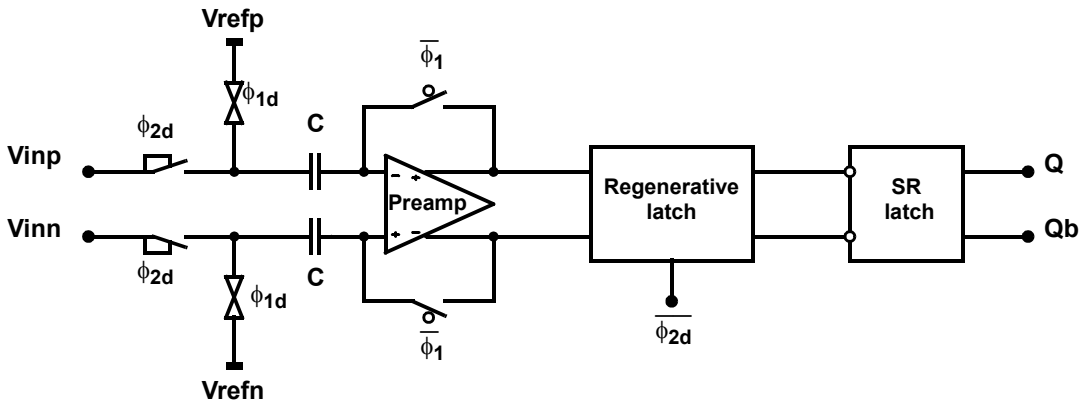


Figure 6.3: The differential SC latched comparator used in both ADCs with the corresponding clock phases for ADC_1.

CMOS switches are used for reference sampling while PMOS switches are used to reset the preamplifier. The floating switch passing the input signal is implemented as a bootstrap

switch (explained in the next section). The capacitor C is chosen to be 125fF. The preamplifier used in this design is a source-coupled gain block with diode-connected active loads and with gain enhancement via controlled positive feedback [Gre99, All82] as depicted in Figure 6.4. The transistor sizes are listed in Table 6.8. The preamplification gain is about 4V/V.

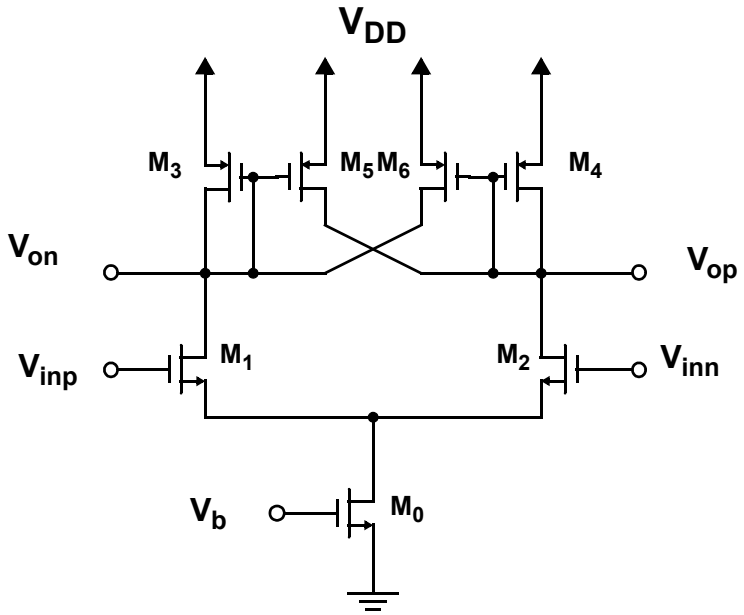


Figure 6.4: The preamplifier [Gre99].

Table 6.8: Transistor sizes of the preamplifier.

	M_0	M_1, M_2	M_3, M_4	M_5, M_6
$N_{fingers}$	3	1	1	1
W $[\mu m]$	0.5	1.5	1.125	1.875
L $[\mu m]$	0.15	0.15	0.15	0.15

The used regenerative latch [Kob93] is shown in Figure 6.5. When the **Latch** signal is high, the latch is enabled but it resets (outputs are both high) when **Latch** is low. The transistor sizes are listed in Table 6.9. Monte-Carlo simulations were carried out to determine the input-referred offset due to transistor mismatch for the whole SC comparator. The 3σ of the mismatch was found to be 6mV which is well below 0.5LSB or $\Delta/2$ (20.8mV) for proper operation [Gre99].

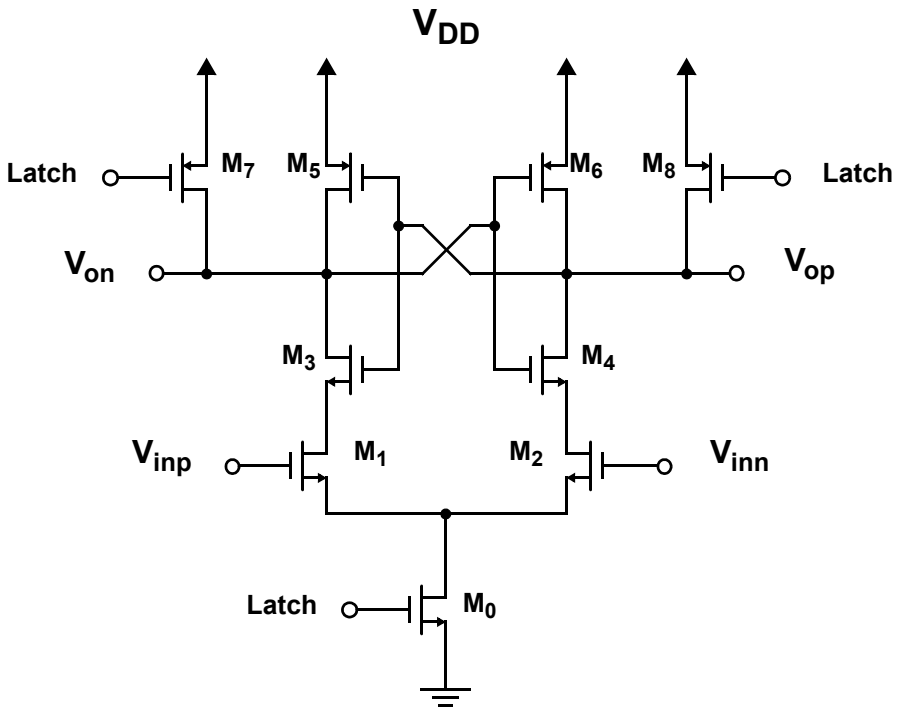


Figure 6.5: The regenerative latch [Kob93].

Table 6.9: Transistor sizes of the regenerative latch.

	M_0	M_1, M_2	M_3, M_4	M_5, M_6	M_7, M_8
$N_{fingers}$	1	2	1	1	1
W $[\mu m]$	2	2.5	1	3	3
L $[\mu m]$	0.06	0.15	0.06	0.06	0.06

The selection of the unit resistance value in the resistive ladder is a trade-off. A large resistance ensures less static power consumption as well as better matching between resistors. On the other hand, a small resistance is required to ensure small time-constants at the ladder taps to settle due to switching activities during the reference-sampling phase. The unit resistance is 40Ω for ADC_1 and 80Ω for ADC_2 because the reference-sampling occurs during ϕ_1 for ADC_1 and ϕ_2 for ADC_2 and ϕ_2 duty cycle is about double ϕ_1.

6.3 Sampling and DAC Switches Design

As shown in Figure 5.3, different types of switches are used depending on the voltage to connect to given that $V_{DD} = 1V$ (Figure 6.6). All floating switches, connecting to a variable voltage, are implemented as bootstrapped switches which ensure a constant resistance over the signal swing of operation [Abo99, Des01]. Connecting to constant reference voltages, simple MOS switches can be used. NMOS switches are used to connect to $V_{cmi} = 0.35V$ while CMOS switches are used to connect to $V_{cmo} = 0.5V$ and $V_{cm} = 0.5V$.

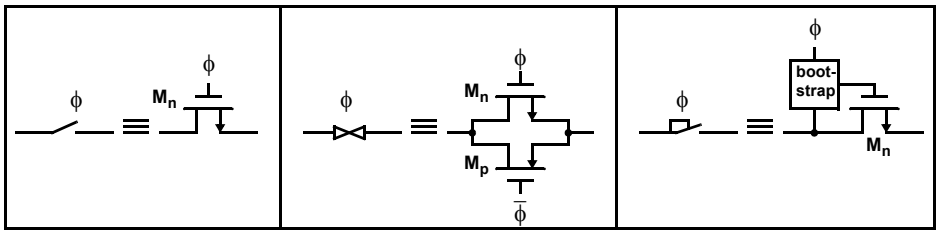


Figure 6.6: The different types of switches used in the design.

The used bootstrapped switch [Abo99, Des01] is depicted in Figure 6.7. The operation is based on pre-charging C by V_{DD} during $\phi = 0$ and connecting it through the gate-source of the main NMOS switch M_0 (in dashed box in Figure 6.7) when $\phi = 1$ to maintain a constant V_{GS} across M_0 and hence constant switch on-resistance which improves linearity as well as signal swing. A 25Ω switch is designed for the floating switches at the output of the first and second integrators while a 50Ω switch is designed for the floating switches at the output of the third integrators. The component sizes are listed in Table 6.10. Input switches within DAC_1 are implemented using distributed bootstrapped switches driven by 2 bootstrap circuits each controlling 24 NMOS switches. Each NMOS switch is $(0.6\mu m/0.06\mu m)$. The same distributed bootstrapped switches are used for ADC_1 and ADC_2, with one bootstrap circuit controlling 24 NMOS switches in each ADC. The component sizes are listed in Table 6.11.

A 25Ω NMOS switch is designed for the input switches of first, second and fourth integrators while a 50Ω switch is designed for the input switches of the third integrator. Transistor sizes are listed in Table 6.12. A 25Ω CMOS switch is designed for all integrators due to switch sharing. Transistor sizes are listed in Table 6.13. The 16-element extra DAC within DAC_1 uses CMOS switches with sizes listed in Table 6.14 along with the CMOS switches used for reference sampling in $ADC_{1,2}$.

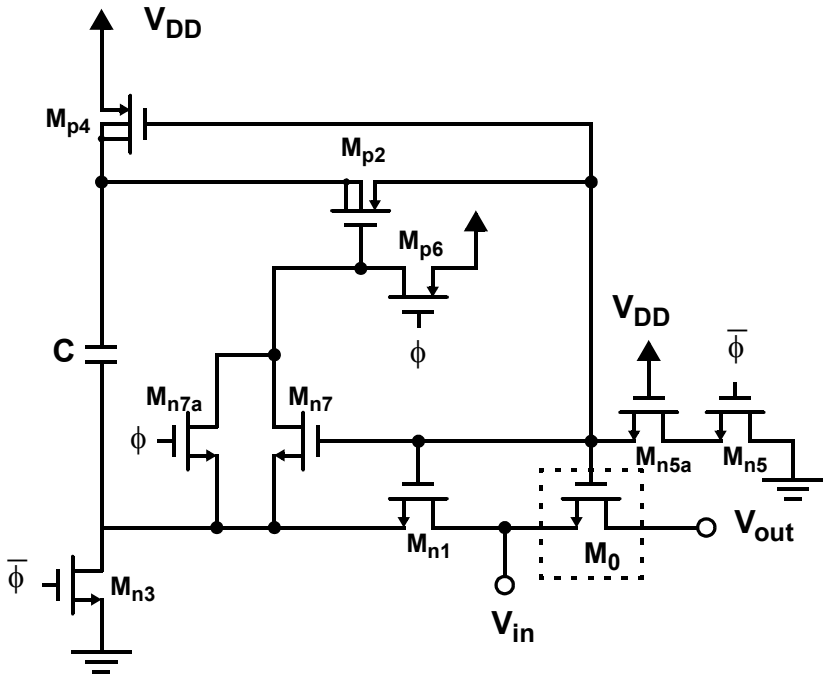


Figure 6.7: Bootstrap switch [Abo99, Des01].

Table 6.10: Transistor sizes of the bootstrapped switches.

	M_0	M_{n1}, M_{n3}, M_{n5}, M_{n7}, M_{n7}	M_{n5a}	M_{p2}, M_{p4}, M_{p6}	C $[pF]$	$R_{on}[\Omega]$
$N_{fingers}$	6	1	1	1	0.8	25
W $[\mu m]$	2.5	1	1	1		
L $[\mu m]$	0.06	0.06	0.09	0.06		
$N_{fingers}$	3	1	1	1	0.4	50
W $[\mu m]$	2.5	0.6	0.6	0.6		
L $[\mu m]$	0.06	0.06	0.09	0.06		

Table 6.11: Transistor sizes of the bootstrapped switches used in DAC_1 and $ADC_{1,2}$.

	M_0	M_{n1}, M_{n3}, M_{n5}, M_{n7}, M_{n7}	M_{n5a}	M_{p2}, M_{p4}, M_{p6}	C $[pF]$	$R_{on}[\Omega]$
$N_{fingers}$	24	1	1	1	1.2	25
W $[\mu m]$	0.6	1	1	1		
L $[\mu m]$	0.06	0.06	0.09	0.06		

Table 6.12: Transistor sizes of the NMOS switches.

	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$R_{on}[\Omega]$	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$R_{on}[\Omega]$
M_n	16	2.5	0.06	25	8	2.5	0.06	50

Table 6.13: Transistor sizes of the CMOS switches.

	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$R_{on}[\Omega]$
M_n	20	2.5	0.06	25
M_p	36	5	0.06	

Table 6.14: Transistor sizes of the CMOS switches used in DAC_1 and $ADC_{1,2}$.

	DAC_1			$ADC_{1,2}$		
	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$
M_n	1	2.5	0.06	1	1.5	0.06
M_p	3	2.5	0.06	3	1.5	0.06

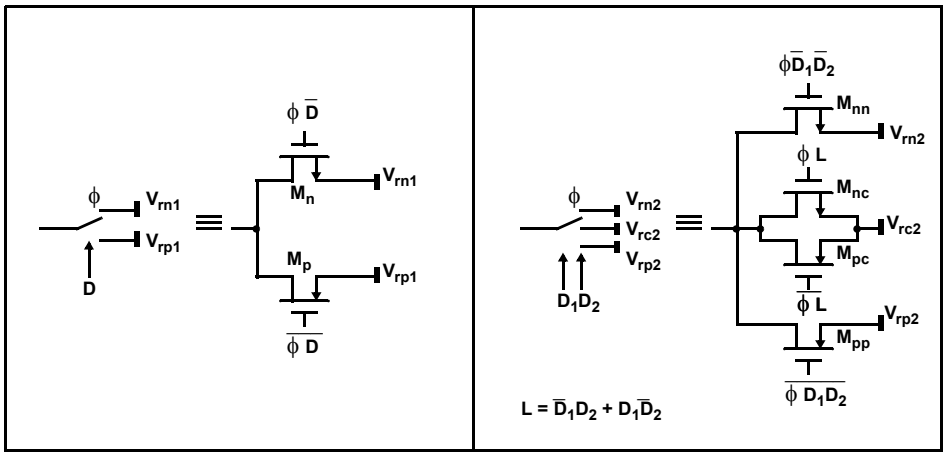


Figure 6.8: DAC switches.

As depicted in Figure 6.8, DAC_1 data switches are CMOS switches. PMOS switch for V_{rp1} sampling and NMOS switch for V_{rn1} sampling. This works as a double-through single-pole switch. DAC_2 switches are more like triple-through single-pole switches as shown in

Figure 6.8. It has an extra CMOS switch compared to DAC_1 switches to sample $V_{rc2} = 0.5V$. Transistor sizes are listed in Table 6.15.

Table 6.15: Transistor sizes of the switches used in DAC_1 and DAC_2 .

	DAC_1			DAC_2		
	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$	$N_{fingers}$	W $[\mu m]$	L $[\mu m]$
M_n/M_{nn}	1	0.6	0.06	1	0.8	0.06
M_p/M_{pp}	3	0.6	0.06	3	0.8	0.06
M_{nc}				4	0.8	0.06
M_{pc}				12	0.8	0.06

6.4 Digital Circuits Design

The digital circuit design in 65nm CMOS digital process should be a simple task especially if the system clock is only 128MHz. The main task is to achieve a functional design in which delays are minimized for proper operation within the allowed time constraints. Moreover, an efficient design should minimize power consumption. In the following, we will go over the design of the main digital blocks, namely, the digital thermometer-code adder, the Data-Weighted-Averaging (DWA) processor, and the clock generator.

6.4.1 Digital Addition

The digital addition of the outputs of ADC_1 and ADC_2, shown in Figure 5.3, can be implemented in two different schemes. The first scheme relies on performing a thermometer-to-binary encoding for both codes and then perform a standard binary addition. But then, we will have to decode the binary-coded sum into thermometer code for shifting within the DWA before passing it to DAC_1. The binary-coded sum will still be useful for pointer generation inside the DWA. The other scheme allows the addition to take place on the thermometer codes and get a thermometer-coded sum ready to be passed to DWA shifting. A thermometer-to-binary encoding will be required within the DWA to generate the pointer but this has a

complete clock-cycle and not time-critical. Circuit simulations show that the second scheme has a delay of about half the first one which gives a good reason to choose it.

The implementation of the thermometer-code addition can be done in various ways. In this work, we chose to implement it by a barrel-shifter [Rab02] using NMOS pass transistors. The 24-line thermometer code from ADC_1 represents a swing of $\pm 0.5V$ with a step Δ_1. The 24-line thermometer code from ADC_2 represents a swing of $\pm 1V$ with a step $\Delta_2 = 2\Delta_1$. For proper addition, the ADC_1 code has to be padded with 12 ones and 12 zeros before or within the addition. Furthermore, ADC_2 code has to be multiplied by 2 before or within the addition. This way, we are effectively adding two 48-line thermometer codes to get 96-line output. But since we already padded ADC_1 code with 12 ones and 12 zeros, which will show up at the sum, the output is actually a 72-line thermometer code. Only 64 lines are taken and 4 lines from each sides are dropped which have the effect of a saturation block. As explained in Chapter 5, this decision simplifies the DWA and DAC_1 design.

The ADC_2 code is transformed in to 1-out-of N code which inherently includes error correction. This code is used to shift ADC_1 code, by controlling the gates of the NMOS pass transistors, in steps of 2 to perform the multiplication. For example, a code of 7 shifts by 14. From ADC_1 code to the output code each line passes through one pass transistor only. At the output, level-restoration is used before buffering the bits for proceeding stages. The NMOS pass transistors form an array of 25 by 36 transistors each is $(0.24\mu m/0.06\mu m)$. Any bubble errors in ADC_1 code are dealt with in the DWA processing. The adder was simulated to check its functionality, make sure that the delay throughout the whole adder is within the allowed range, and get an estimate of power consumption.

6.4.2 Data Weighted Averaging

The DWA processing comprises three main blocks as shown in Figure 6.9. The 64-line DAC elements selection which shifts the thermometer code from the adder and delivers it to DAC_1. The shifter is a 6-stage logarithmic shifter controlled by a 6-bit pointer [Rab02]. Each stage consists of 2×64 NMOS pass transistors each with size $(0.24\mu m/0.06\mu m)$. Level restorations is added after second, fourth, and last stage. The second block is the pointer generation

logic which is based on a 6-bit ripple-carry adder which works as modulo-64 adder. The full-adder cell is implemented as a mirror adder [Rab02]. The third block is the thermometer to binary encoder which transforms the 64-lines thermometer code into a 7-bit binary code. The encoder have inherent error correction. The bits are taken to the output buffers of the $\Delta\Sigma$ modulator. These bits, except the MSB, are taken to the pointer generation logic, An enable is added to the pointer to enable/disable the shifting in the logarithmic shifter. The DWA block was simulated to check its functionality, make sure that the delay throughout the whole block is within the allowed range, and to get an estimate of power consumption.

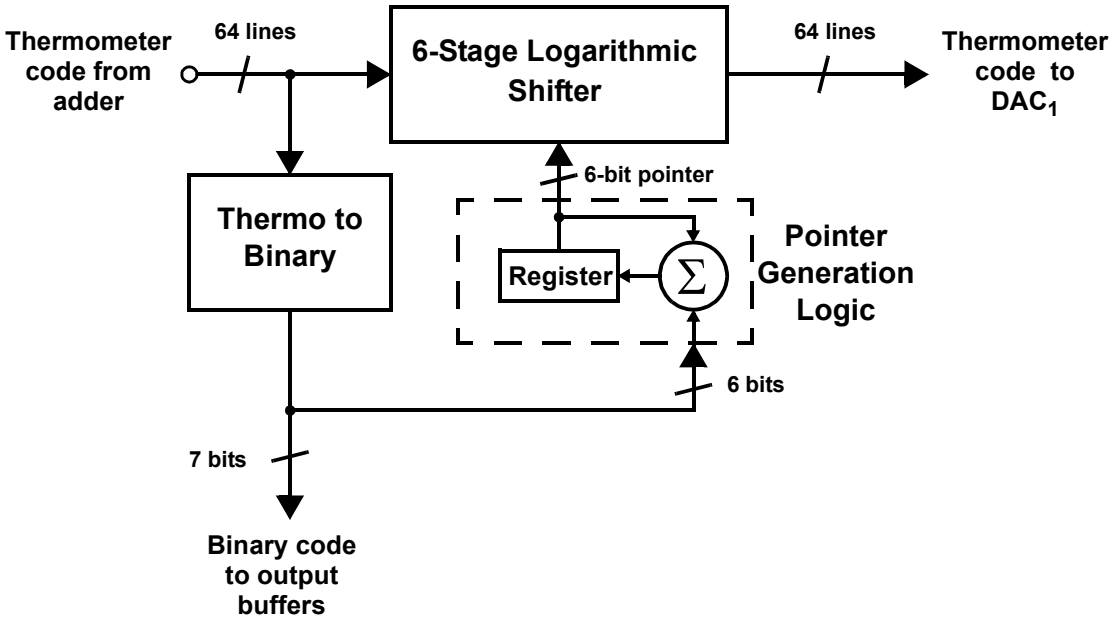


Figure 6.9: Conceptual block diagram of the DWA.

6.4.3 Clock Generation and Duty-Cycle Control

The system is fed by a standard 50% duty-cycle clock. The clock generator circuit generates the two non-overlapping versions ϕ_1 and ϕ_2 as well as the delayed versions ϕ_{1d} and ϕ_{2d}. The inverted versions are also generated so that each clock is distributed with its inverted version to minimize cross-talk and substrate noise coupling. All 8 clock signals are then buffered to a clock distribution network.

As explained in Chapter 5, the modulator uses unequal clock phases. The delay block in Figure 6.10 controls the duty-cycle of the two clock phases. It is designed as a variable delay controlled by two bits to give four different duty-cycle values. This delay block is composed of four delay units in series with tapped outputs. A multiplexer chooses one out the four tapes. Simulations shows a variation in ϕ_1 duty-cycle from 27% up to 34% and a variation in ϕ_2 duty-cycle from 64% down to 57%. This range gives some flexibility during testing. The D block is another delay block that determines the non-overlapping period which is about 9% in this design.

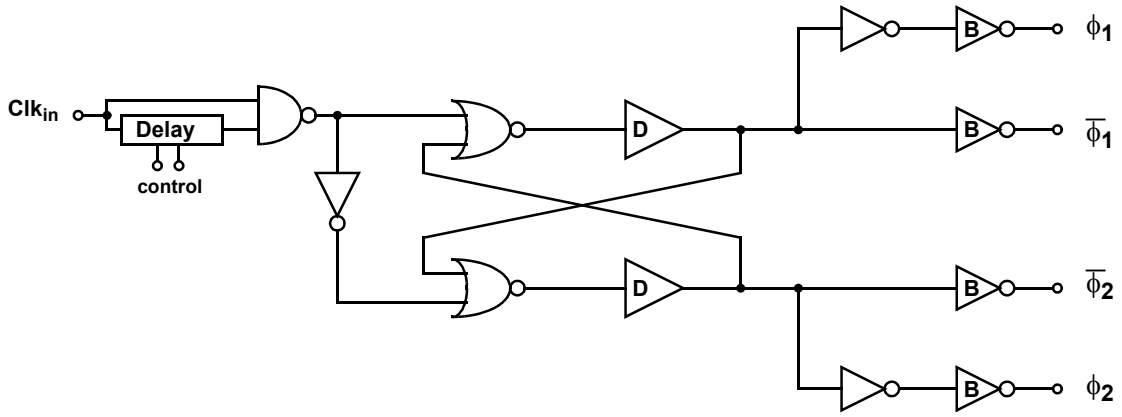


Figure 6.10: Non-overlapping clock generator with duty-cycle control (delayed clock phases are not shown for simplicity).

6.5 Circuit Simulations Results

After simulating individual blocks, the full-system was simulated. It was simulated first with ideal blocks to test the full set-up, then real circuit blocks were introduced gradually. Starting with the opamps, the simulations proved the functionality. Real ADCs and DACs were added and finally all digital blocks wee added. A transient simulation is run and the output bits are sampled and processed to estimate the PSD. As shown in Figure 6.11, an input signal of 1.5MHz with 0dBFS is applied. The PSD was estimated by a 2^8 Hann FFT. The SFDR is about 86dB and the SNDR about 84.75dB (without thermal noise and DAC nonlinearity). The average power consumption was simulated to be about 18mW which leads to an FoM of

0.08pJ/step. Combined with the thermal noise and DAC nonlinearity, the SNDR is estimated to go down to about 80dB (13 bits) which corresponds to an FoM of 0.14pJ/step. With other silicon nonidealities, the SNDR is expected to go down to around 12bits.

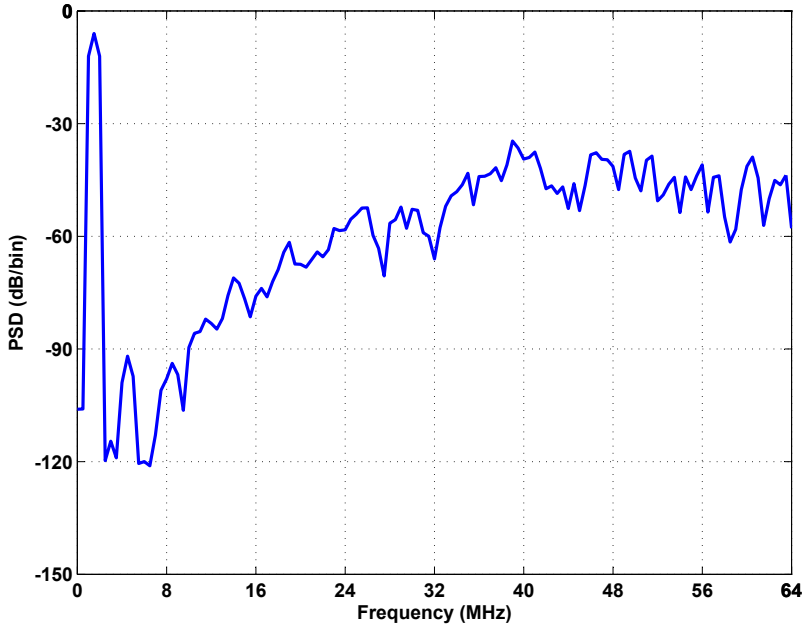


Figure 6.11: The output PSD for the full-system circuit simulations for a 1.5MHz input sinusoid with 0dBFS amplitude.

6.6 Conclusion

This chapter presented the circuit design steps for the different building blocks of the $\Delta\Sigma$ modulator that was discussed in the previous chapter. Starting with the main analog circuit blocks, the opamp design was discussed in details. The flash ADC design was then presented. The main issues in the switch design were discussed. An overview of the digital circuits was then presented. Full-system circuit simulations proved that the system is ready for silicon implementation and fabrication. In the next chapter, the experimental results will be presented and discussed.

Chapter 7

Experimental Results of the $\Delta\Sigma$ Modulator Prototype

An experimental prototype is essential for the verification of any circuit design especially in modern nanometer technologies for which the circuit models are still limited. This chapter explores the experimental results of a prototype built for the experimental $\Delta\Sigma$ modulator designed and discussed in Chapter 5 and Chapter 6. Starting from silicon-level aspects, the chapter also sheds some light on the test set-up.

Section 7.1 starts with the chip layout and the general guidelines followed for a good layout. Section 7.2 then goes over the test set-up prepared to experimentally test the prototype. Section 7.3 presents the experimental results measured from the prototype. Section 7.4 compares the experimental results with state-of-the art CMOS $\Delta\Sigma$ modulators operated form a 1V supply.

7.1 Chip Layout

The experimental prototype was fabricated in 65nm GP 1-poly 9-metal digital CMOS process with metal-insulator-metal (MIM) capacitor option. The chip micrograph is depicted in Figure 7.1 .The main blocks as well as the pad names are shown in the figure. The chip has an active area of 1.2mm^2 and a total area, with pads, of 2.34mm^2. The die was packaged in an 80-pin ceramic quad flat pack (CQFP) package.

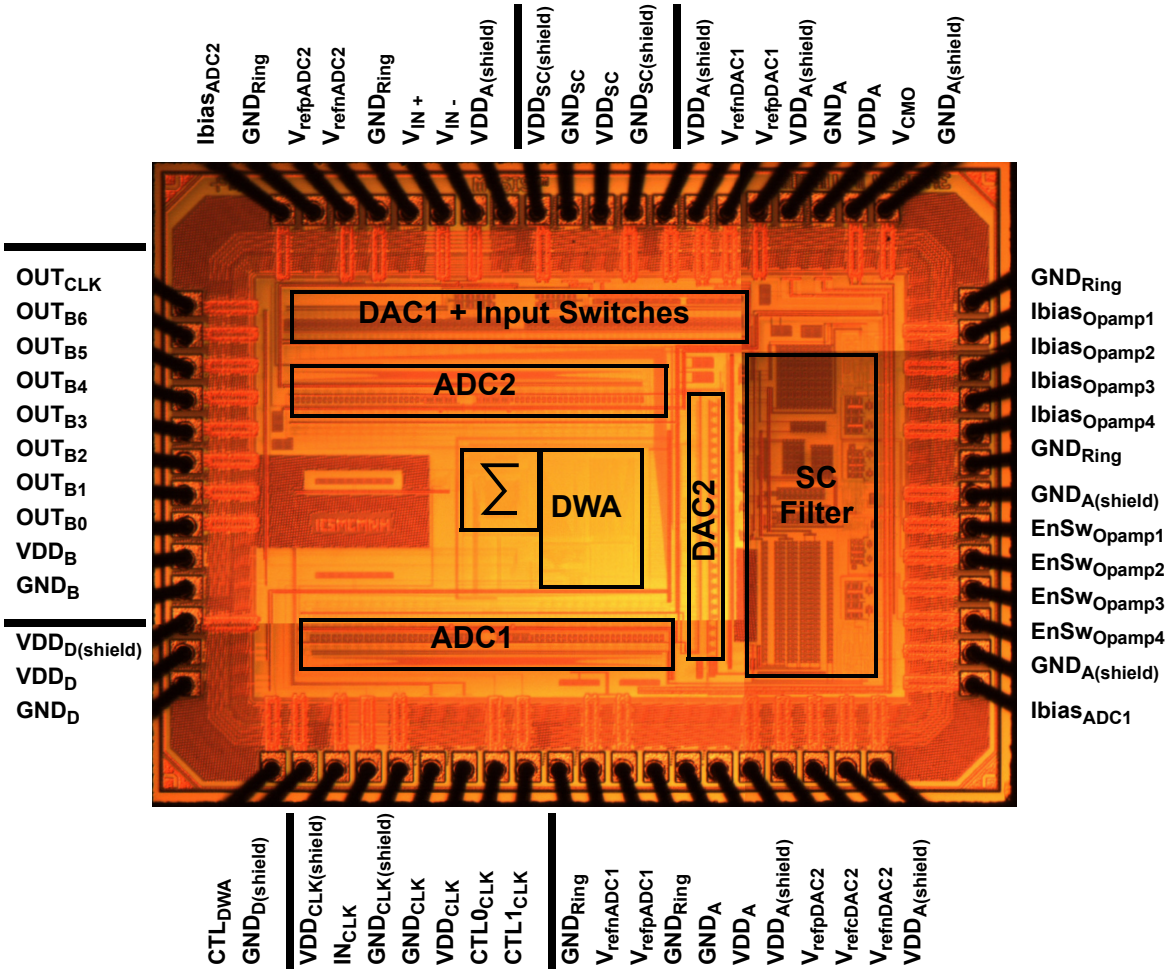


Figure 7.1: Chip micrograph of the experimental ΔΣ modulator.

Due to the mixed-signal nature of the $\Delta\Sigma$ modulator, separate supply and ground lines were used for analog (VDD_A, GND_A), digital (VDD_D, GND_D), switched-capacitor (VDD_{SC}, GND_{SC}), clock (VDD_C, GND_C), and output buffers (VDD_B, GND_B) circuits. The main purpose is to prevent switching noise to couple into the sensitive analog supplies. Power cuts were introduced in the pad ring (positions showed in thick lines in Figure 7.1) to avoid connecting the supplies on chip. Guard rings were used for circuit isolation to minimize substrate noise coupling. Sensitive signals were routed over n-well to minimize substrate noise coupling. Separate shield supply and ground lines where used for this purpose. Decoupling capacitors were added on-chip for all supply lines as well as reference lines to bypass high-frequency noise.

The first fabricated prototype showed a significant DC offset at the output when the DEM is switched off which would increase when sampling rate increases. Although this offset would almost disappear when the DEM is turned ON, the SNR would deteriorate. After investigating, this was thought to be due to the wire resistance of the main DAC taps. The second prototype, tested in this chapter, was laid-out more carefully to minimize the parasitic resistance of the interconnects while watching the parasitic capacitance. The output buffers were also redesigned to insure a better waveform at the output.

7.2 Test Set-Up

A four-layer printed-circuit board (PCB) was designed and fabricated to test the prototype. The two middle layers are used as ground and supply planes. Each is split into 5 different domains representing the five different supply lines (analog, digital, switched-capacitor, clock, and buffer). The PCB provides capacitive decoupling for the supply and reference lines. It also provides switches for logic control to enable/disable DWA (CTL_{DWA} in Figure 7.1), to control the duty-cycle (CTL_1,CTL_0 in Figure 7.1), and to enable/disable switching in the four opamps ($EnSW_{Opamp1\text{-}4}$). Off-chip bias resistors are mounted on the PCB as potentiometers to provide control over the opamp bias currents for opamps ($Ibias_{Opamp1\text{-}4}$) and for the ADCs ($Ibias_{ADC1\text{-}2}$). 1Ω resistors are connected in series with all supplies to measure the current consumption, and hence the power consumption.

The full test set-up is shown in Figure 7.2. The signal generator (SMA100A) provides the input sinusoid. Its single-ended line is filtered to attenuate harmonics and then split (0° and 180°) to provide a differential input. The differential signal is biased properly on the PCB. The clock signal is provided by the clock generator (CG635). Separate DC supplies (E3620A and 3617A) are used to provide the reference voltages as well as the supplies. The output clock and data are captured by the logic analyzer (TLA7012). The data sampled and collected from the logic analyzer is then passed to a computer (off-line) for processing.

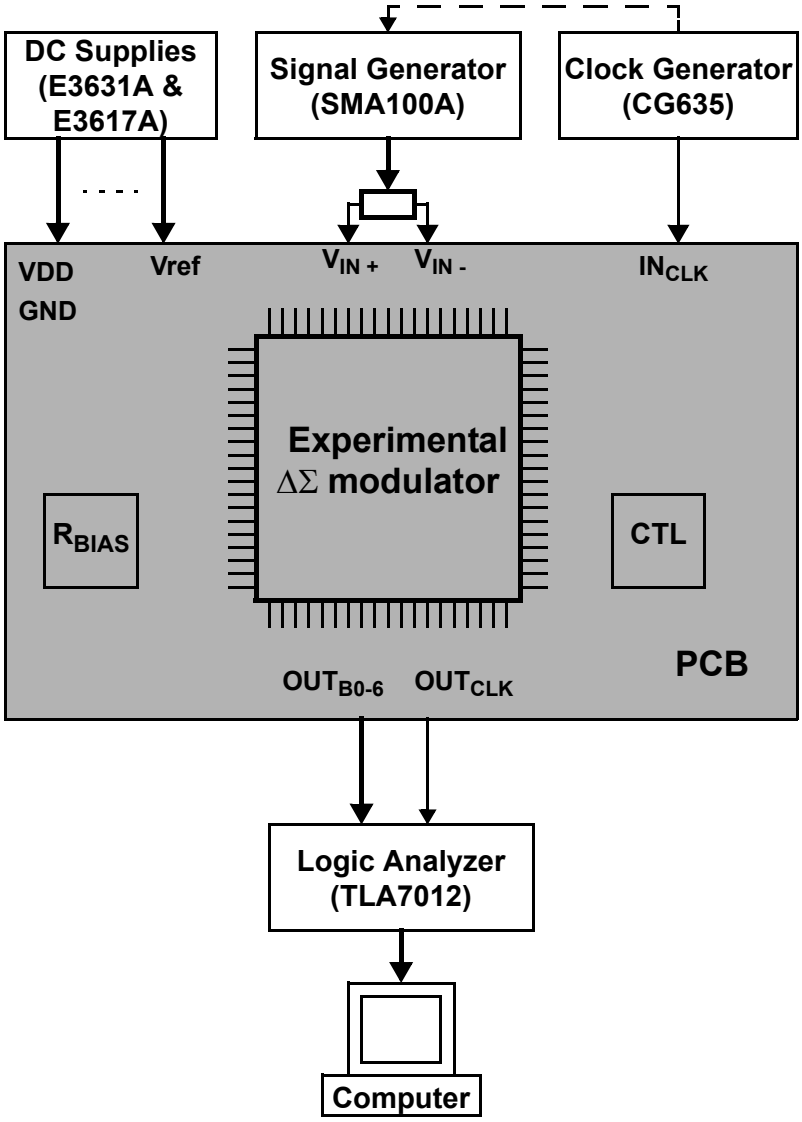


Figure 7.2: Experimental test set-up.

7.3 Measured Performance

The test set-up shown in Figure 7.2 was used to perform a single-tone test for the experimental prototype. Although the experimental $\Delta\Sigma$ modulator was designed to run at a 128MHz sampling rate, we started testing at lower sampling rates (32, 64, and 96MHz) and then increased the rate until reaching 128MHz. The bandwidth used to verify the performance is scaled with the sampling rate.

Figure 7.3 shows the variation of both SNR and SNDR, measured over an 8MHz bandwidth, with the input level in dBFS (dB Full-Scale) for a 1.465MHz single tone at a sampling rate of 128MHz. The peak SNR is found to be 64dB at -2dBFS while the peak SNDR is 58.5dB at -7dBFS. The DR can be calculated to be 66dB as shown in Figure 7.3. Figure 7.4 depicts the measured output PSD for a -7dBFS 1.465MHz single tone when opamp switching is enabled while Figure 7.5 depicts the output PSD when opamp switching is disabled. It is clear that the linearity is not affected by switching. The SFDR is about 67dB in both cases.

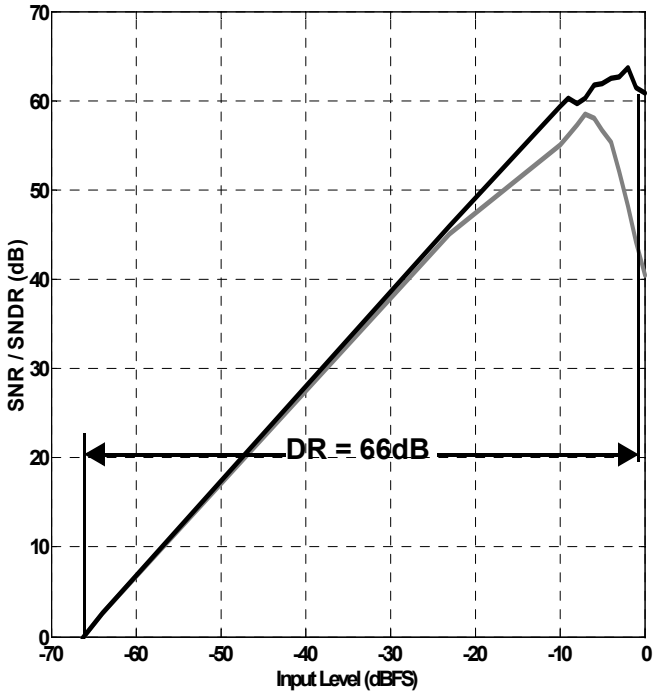


Figure 7.3: SNR and SNDR versus Input level (dBFS) with switching enabled.

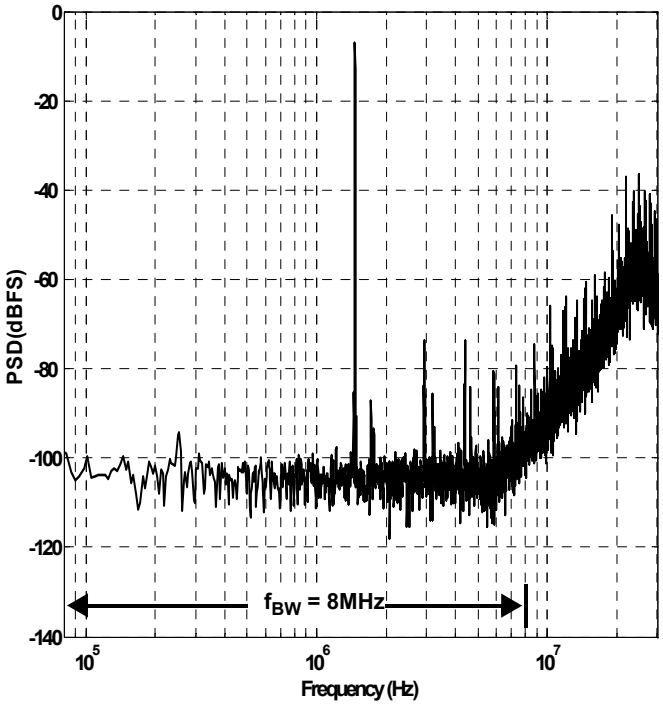


Figure 7.4: The measured output spectrum for -7dBFS 1.465MHz input sinusoid (switching enabled).

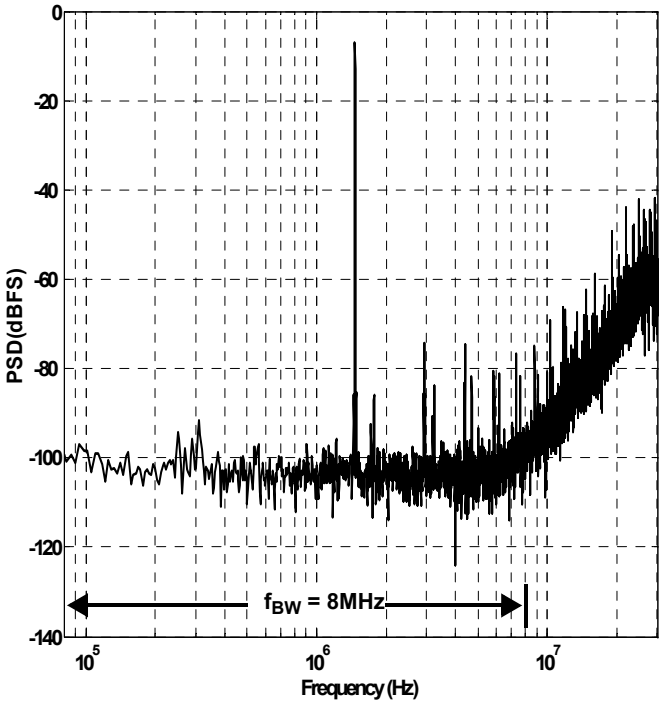


Figure 7.5: The measured output spectrum for -7dBFS 1.465MHz input sinusoid (switching disabled).

The shown results are measured from a single chip. Although switching from one chip to another was necessary because of what seemed to be a partial failure after some time, the measured performance was continuous from one chip to another. Which means, that after switching to anther chip, the measured results were very close to the last seemingly correct result of the previous chip before the failure. The failure is thought to be due to ESD(Electro Static Discharge).As shown in Figure 7.6, the scattered results from two chips are close to the continuous results of the last chip with switching disabled. Two more chips were tested at 96MHz sampling rate. As listed in Table 7.1, the measured results at -5dBFS are very close.

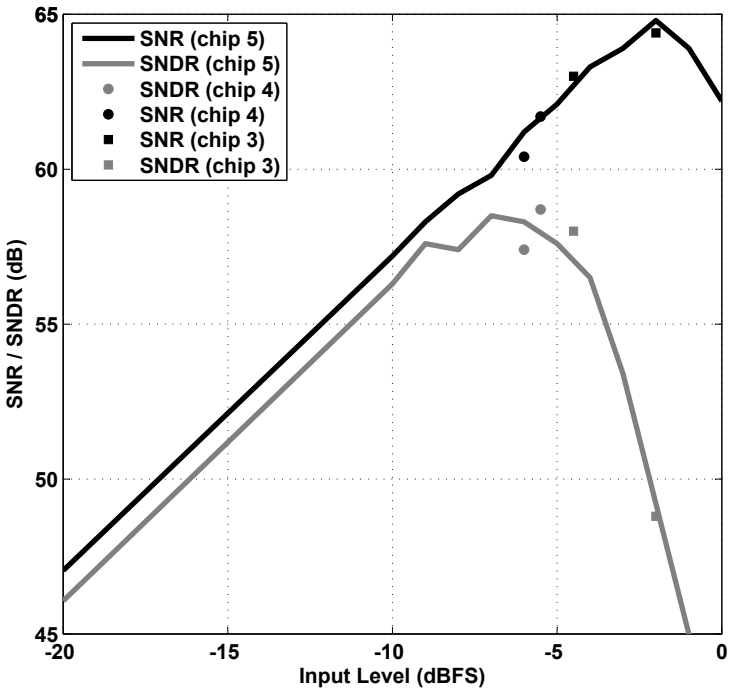


Figure 7.6: SNR and SNDR versus Input level (dBFS) for multiple chips at 128MHz sampling rate (opamp switching disabled).

Table 7.1: Measured Performance comparison between two tested chips for an input level of -5dBFS at 96MHz sampling rate (switching disabled).

Parameter	Input Level	Chip 1	Chip 2
SNR (dB)	-5dBFS	64.3	64.9
SNDR (dB)		57.5	57.6

Table 7.2: Measured Performance summary of the experimental prototype (switching enabled).

Parameter		Value	
Sampling Frequency	f_S	128MHz	64MHz
Input-Signal Bandwidth	f_{BW}	8MHz	4MHz
Dynamic Range	DR	66dB	75dB
Peak SNR		64dB	74dB
Peak SNDR		58.5dB	63dB
Analog Power		24mW	17mW
Digital Power		2mW	1mW
Total Power	P_{total}	26mW	18mW
Supply Voltage		1V	
Active Area		$1.2mm^2$	
Process		65nm GP 1P9M	

Table 7.3: Measured Performance comparison between opamp switching enabled and disabled.

Parameter		Switching Disabled	Switching Enabled
Peak SNDR		58.5dB	58.5dB
Total Power	P_{total}	29mW	26mW

Table 7.2 summarizes the main performance metrics measured at both 64 and 128MHz. For a 128MHz sampling rate, the DR /peak SNR / peak SNDR are found to be 66dB / 64dB / 58.5dB respectively while for a 64MHz sampling rate, the DR / peak SNR / peak SNDR are found to be 75dB / 74dB / 63dB respectively. The total power consumption is 26mW for 128MHz sampling rate while 18mW for 64MHz sampling rate. Table 7.3 compares between the two cases when the opamp switching is disabled and enabled. As we can see, the peak SNDR (at -7dbFS) remains at 58.5dB while the power consumption drops from 29mW to 26mW when switching is enabled. The power reduction here is only 10% because it is for the overall system and for the pupose of this prototype the switching ratios were not pushed to the limit. The highest ratio is 0.5.

There is a clear deviation between the measured results and the expected ones from circuit simulations (Section 6.2) as well as the behavioral simulations (Section 5.3). The main reason is thought to be the parasitic capacitance, that was underestimated, loading the last opamp which required a dramatic increase in its biasing current to meet the settling requirements. However, increasing the bias current drops the DC gain which in turn causes coefficient mismatch. The coefficient mismatch of the last integrator directly affects the NTF and causes Q_2 leakage (quantization noise from ADC_2) due to transfer function mismatch between the analog domain and digital domain. The bias current is adjusted for the best result in SNDR. At 64MHz sampling rate, the last opamp bias current problem is alleviated because less current is required to meet the settling accuracy requirements.

Full-system Cadence circuit simulations, with a large parasitic capacitance at the output of the last integrator, shows a significant deterioration in performance as the capacitance increases. Also, the excessive increase of the bias current of the last integrator, to accommodate for the large parasitic capacitance, deteriorates the performance as the NTF gets affected. As shown in Table 7.4, doubling the lumped parasitic capacitance, significantly drops the SNR at the nominal biasing reference current (150μA). Doubling the reference current (300μA) helps recover the SNR with only about 3dB drop from the nominal case. It is also clear that the excessive increase in reference current (450μA) has a negative effect as explained earlier. We see also that for the doubled parasitic capacitance, the 300μA gives the best SNR which is very close to testing results of 320μA.

Table 7.4: Measured Performance comparison between opamp switching enabled and disabled.

Parasitic	Reference bias current		
Capacitance	150μA	300μA	450μA
C_p	80dB	80dB	77dB
$2C_p$	43dB	77.5dB	68dB

The clear deterioration in linearity, after investigation, is thought to be due to systematic mismatch between DAC_1 elements caused by possible process gradient. This problem is thought to be significant because the DAC elements are spread over about 1mm, which means that the spacing between DAC capacitors reaches about 1mm. Although DWA alleviates this mismatch (non-linearity), it has limited shaping capability (first-order shaping only).

Simulink simulations were carried out modelling a possible linear gradient in DAC_1 unit capacitors. The actual layout array is $(C_{p1}\ C_{n1})\ \ (C_{n2}\ C_{p2})$ .... $(C_{p63}\ C_{n63})\ \ (C_{n64}\ C_{p64})$. A mismatch of $\pm$ 5% with a standard deviation of 3%, produces a DC offset of about -30dB when the DWA is OFF which is very close the test results. When the DWA is turned ON, simulations predict an SFDR of about 68dB at -7dBFS input level which is close to the measured value of 67dB. This mismatch could be alleviated by a common-centroid layout in which each unit element is split into two halves and the array $(C_{p1}/2\ C_{n1}/2)\ \ (C_{n2}/2\ C_{p2}/2)$ .... $(C_{p63}/2\ C_{n63}/2)$ $(C_{n64}/2\ C_{p64}/2)$ is laid out side by side with the array $(C_{p64}/2\ C_{n64}/2)\ \ (C_{n63}/2\ C_{p63}/2)$ .... $(C_{p2}/2\ C_{n2}/2)\ \ (C_{n1}/2\ C_{p1}/2)$ to average out the linear gradient.

The selected architecture (DFF explained in Section 2.4.3) is thought to not have any contribution to the performance degradation since the performance is much better at 64MHz sampling rate. This means that the redesign of the opamp bandwidth (especially the last integrator) should fix the performance. It is worth mentioning that the opamp switching technique proves to be working without negative effect of the performance (SNDR) while achieving some power reduction. More specifically, the opamp switching is not causing the performance deviation from the expected results since this deviation is still there even if the switching is disabled as listed in Table 7.3.

7.4 Performance Comparison

Table 7.5 (last updated April 2013) compares the measured performance with state-of-the-art LP high-speed ($f_{BW}\ \geq$ 2MHz) high-resolution (DR or SNR $\geq$ 62dB (10bits)) ΔΣ modulators fabricated in CMOS process and operated from 1V supply. Despite the performance deviation explained in the last section, the FoM (calculated by (2.8)) is within the FoM range of the ΔΣ modulators listed in the table.

It is worth mentioning that the experimental prototype is the only Discrete-Time (DT) $\Delta\Sigma$ modulator that falls in that range of performance (speed and resolution) while operated from a 1V supply. Although the measured performance of this DT prototype does not surpass the other CT modulators in the table, it could compete with the other CT modulators. This is thought to be due to the careful architecture selection, the proposed low-power techniques and the followed design procedure. Few design and layout ameliorations could make the performance better.

Table 7.5: Comparison with state-of-the-art high-speed ($f_{BW} \geq$ 2MHz) high-resolution (DR or SNR $\geq$ 62dB (10bits)) $\Delta\Sigma$ modulators fabricated in CMOS process and operated from 1V supply.

Reference	f_{BW} (MHz)	f_S (MHz)	DR (dB)	SNR (dB)	SNDR (dB)	Power (mW)	CMOS Process	Input DT/CT	FoM
[Mat10b]	4	140		70.2	69.8	3.6	65	CT	0.17
[Ke10]	2	128	75		72	3.6	90	CT	0.2
	4	192	72		69	4.9			0.19
[Car11] V_{DD}=1.05V	5	400	71		69	28	32	CT	0.97
	10		68		65				0.68
	20		66		63				0.43
[Pre11]	20	640	63		61	7	65	CT	0.15
This work	8	128	66	64	58.5	26	65	DT	0.99
	4	64	75	74	63	18			0.49

7.5 Conclusion

This chapter presented the experimental results of the $\Delta\Sigma$ prototype. Starting with highlights of the chip layout, we looked then into the PCB and the test set-up. The experimental results then shows a DR of 66dB over an 8MHz signal bandwidth at a 128MHz sampling rate. The peak SNR/SNDR where found to be 64/58.5dB while consuming 26mW. The opamp switching technique proves to be working without affecting the peak SNDR (58.5dB) while reducing power consumption from 29mW to 26mW. Comparing the experimental results with state-of-the-art $\Delta\Sigma$ modulators operated from 1V supply and with signal bandwidth $\geq$ 2MHz and DR (or SNR)$\geq$ 62dB, shows that the FoM falls in their FoM range.

Chapter 8

Conclusion and Closing Remarks

THIS CHAPTER summarizes the work accomplished in this thesis and lists the key research contributions. The chapter concludes by offering suggestions for future research as a continuation of this thesis.

8.1 Thesis Summary

This thesis tackled the design of DT $\Delta\Sigma$ modulators for high-speed high-resolution applications. The design adheres to the low-power requirements of hand-held devices while fabricated in nanometer digital CMOS process for high system integration. The thesis started by exploring several low-power SC integrator techniques as well as low-power DT $\Delta\Sigma$ modulator architectures suitable for low-voltage-supply environment.

A novel switchable-opamp for low-power SC integrators was proposed. It is based on a current-mirror opamp with switchable transconductances. The proposed current-mirror opamp works with its full output current during the charge-transfer phase while the output current is partially switched during the sampling phase. Power saving can be achieved while ensuring that the opamp output is available during both phases.

The issue of simultaneous settling for series opamps in nondelaying cascaded SC integrators was investigated. A design procedure was developed for the power-efficient design of two cascaded nondelaying SC integrators while achieving the required settling accuracy.

An experimental $\Delta\Sigma$ modulator was then designed. Starting from system-level, an architecture was selected and the main design parameters (loop filter order, internal resolution, OSR, ...) were chosen. The SC implementation was then addressed with its various aspects and simulated to confirm the SC structure. Using behavioural simulations incorporating various noise sources and nonidealities, a design procedure was followed to find the circuit parameters (sampling capacitors, opamp gain, opamp bandwidth, ...) that achieves the targeted speed (8MHz bandwidth) and resolution ($\geq$12bits). This procedure is Figure-of-Merit (FoM) based to ensure a power-efficient design.

The SC circuit implementation of the experimental $\Delta\Sigma$ modulator was then addressed in 1V 65nm CMOS process. The different building blocks were designed and simulated separately. Then, the full-system was simulated to confirm the functionality and performance. A layout was designed and fabricated for the prototype chip. The experimental prototype was tested by means of a custom PCB and test equipments.

The measured experimental results showed a dynamic range of 66dB over an 8MHz signal bandwidth at a 128MHz sampling rate. The peak SNR/SNDR were found to be 64/58.5dB while consuming 26mW. The opamp switching technique proved to be working without affecting the peak SNDR (58.5dB) while reducing the power consumption from 29mW to 26mW. The comparison of the experimental results with state-of-the-art $\Delta\Sigma$ modulators operated from 1V supply and with signal bandwidth $\geq$2MHz, showed a reasonable FoM.

The deviation of the SNR from what was expected is thought to be mainly due to higher parasitic capacitances (especially at the output of the last integrator). This was confirmed by circuit simulations. A more accurate quantification of the parasitics followed by a redesign of the opamp's bandwidth (especially the one used in the last integrator) should help getting closer results to what was expected. The deterioration in linearity is thought to be due to the systematic DAC capacitors mismatch due to process gradient. Although the DWA is shaping this distortion, as expected, it does not eliminate all the distortion. Simulink simulations confirmed this hypothesis. A common-centroid layout [Joh97] should solve this issue.

8.2 Research Contributions

The key research contributions accomplished in this thesis can be summarized as follows:

1. **A current-mirror opamp with switchable transconductances [Har13a]:**

   A switchable-opamp technique was presented in this thesis for the low-power design of SC integrators as part of the low-power design of DT $\Delta\Sigma$ modulators. It is based on a current mirror opamp with switchable transconductnaces. The current-mirror opamp works with full current during the charge-transfer phase while the output current is partially switched during the sampling phase. Compared to previous opamp-switching methods, the proposed technique is applicable to SC integrators with both full delay and half delay. Furthermore, it does not limit the operation speed of the SC integrator and does not require a special CMFB circuit while achieving reasonable power savings (up to 30%).

2. **A design procedure for nondelaying cascaded SC integrators [Har13b]:**

   A design method was presented in this thesis for the power-efficient design of two nondelaying cascaded SC integrators. Circuit simulation results validates the analytical method. These analytical equations can be easily modelled and used in behavioral simulations for larger systems. Moreover, the thesis addressed an important issue, confirmed by circuit simulations, that affects the design of two nondelaying cascaded SC integrators.

3. **A power-efficiency (Figure-of-Merit) based system-level design procedure:**

   Behavioral simulations were employed along with noise and nonidealities models to solve for the various circuit parameters by optimizing the power-efficiency.

4. **The use of clock phases with unequal duty cycles:**

   The use of nonoverlapping clock phases with unequal duty-cycles was proposed in this thesis. It gives the designer an extra degree of freedom to further power optimize the design. In this design, the ϕ_2 duty cycle was made twice as large as (now about 60%

and originally 45%) the ϕ_1 duty cycle (now about 30% and originally 45%) which saves about 15% of the total modulator power consumption.

5. **Low-Voltage SC circuit implementation:**

   The SC circuit implementation of the experimental $\Delta\Sigma$ modulator in 1V 65nm was presented in this thesis. The prototype allowed the verification of the proposed low-power solutions, especially the switchable-opamp technique.

8.3 Future Research Suggestions

There are several research areas than can be further addressed in future work, namely:

- The proposed switchable-opamp technique could be further analysed to improve its power reduction advantage. Further improvements could be made to extend the operable speed (sampling rate). The combination of this technique with other low power SC techniques, such as dynamic biasing, could also be investigated.

- In the design procedure, presented in Chapter 4, for the design of two cascaded nondelaying SC integrators, some nonidealities, such as switch on-resistance, were not considered. More accurate models could be used in future research to give more accurate results.

- A more general optimization procedure could be developed for the use of clock phases with unequal duty cycles. The procedure should find the optimum duty cycle that gives the minimum total power consumption while ensuring the proper operation of the whole $\Delta\Sigma$ modulator.

- A better layout could be developed for the main DAC to alleviate the systematic offset due to process gradient. A more optimized layout floor plan could also be designed to minimize parasitic capacitances at critical nodes.

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