Integration and Characterization of an MSM Array for Free-Space Optical Backplanes

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Abstract

Future high performance digital computing systems will demand extremely high throughput and connection-intensive backplanes. Free-space optical interconnects have the potential to meet these demands. This thesis explores the application of a two-dimensional array of metal-semiconductor-metal (MSM) photodetectors in a free-space photonic backplane. In particular, two-dimensional smart pixels are presented as a means of achieving a large communications space-bandwidth product. It is argued that a system based on such devices can overcome several physical limitations experienced by electrical interconnects of current printed circuit board based electronic backplanes. As a means to this end, a review of MSM photodetector technology is then conducted.

The layout and design of the optical receiver is presented. The effects of misalignments, optical power variations, and device non-uniformity on receiver performance are considered. With these design parameters in mind, the construction of a receiver assembly is described from the first step of packaging the photodetector array to the last interconnecting cable connection. Specific packaging challenges that are discussed include power dissipation, connectivity, and electrical isolation as related to receiver performance. The method and results of characterization are presented in relation to its meeting the requirements of a receiver array in a free-space optical backplane. Future areas for improvement are then considered.

Résumé

Les ordinateurs numériques à haute performance du futur nécessiteront des fonds de panier ("backplanes") à débit extrêmement élevé afin de répondre aux immenses besoins en bande passante requises par les cartes de processeur. Les interconnections optiques à l'air libre possèdent le potentiel de répondre à de tels besoins.

Cette thèse explore l'utilisation d'une matrice bi-dimensionnelle de photodétecteurs Métal-Semiconducteur-Métal (MSM) dans un fonds de panier photonique utilisant des liens de communication fonctionnants à l'air libre. L'utilisation de matrices bi-dimensionnelles de pixels "intelligents" ("smart pixels") est défendue comme offrant la possibilité d'obtenir de grandes valeurs de produits bande passante-espace physique requis. Il est alors démontré qu'un système utilisant de tels matrices de pixels pourrait surmonter plusieurs des limitations physiques associées aux interconnections électriques utilisées actuellement pour interconnecter les plaquettes de circuit imprimé. La technologie des MSM est aussi passée en revue.

Le design du récepteur optique est présenté. L'effet de défauts d'alignement, de variations de puissance optique et la non-uniformité de la performance de la surface du détecteur sont pris en compte pour évaluer ses performances. Avec ces contraintes de design en tête, la construction du récepteur depuis la mise en boîtier jusqu'à la pose du dernier câble est présentée. Les défis de mise en boîtier qui sont abordés incluent la dissipation de puissance, la connectivité et l'isolation électrique tous des paramètres qui affecteront la performance du détecteur. La méthode de caractérisation du détecteur est présentée. Les résultats obtenus sont alors confrontés aux besoins d'une matrice des détecteurs dans un fonds de panier photonique. En conclusion, des avenues d'amélioration futures sont également explorées.

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Introduction and Motivation

1.1 Introduction

Current and future high performance digital electronic systems that address applications for real-time image processing and pattern recognition, neural networks, massively parallel processing computer systems, asynchronous transfer mode (ATM) and video switching are pushing the limits of current electronic interconnection technologies. In the last decade, the clock speed of high performance processors have increased rapidly year after year. Clock rates of 200 MHz have been attained by low cost RISC microprocessors and supercomputers have already achieved rates of 500 MHz. Simultaneously, in order to achieve higher degrees of integration, the density and complexity of integrated circuits continue to grow. As a result, the interconnection requirements between discrete components have become more demanding in the development of larger architectures and more sophisticated systems. High pinouts arising from high functionality components having large gate counts lead to increased interconnection density. Further coupled with a trend towards compact, high density packaging of several memory and processing elements in order to minimize latency, skew, and signal degradation, interconnection bottlenecks arise. These bottlenecks will occur where the bandwidth and interconnection density are the most limited: the backplane[1][2]. As packet based switching technology becomes more prevalent in the telecommunications industry, switching networks will require switching nodes that are comparable to the processing elements in computers and inherit the associated interconnection constraints. Further, the advances in high speed optical fiber communications has reached the stage to which Japan and the United States have embarked on programs to bring fiber to the home (FTTH) or to the curb (FTTC) respectively. In support of such aggressive programs, several gighertz of bandwidth on a single fiber are now commonplace in today's commercial telecommunication systems, and the effective bandwidth carried by a single fiber can potentially reach hundreds of giga-

hertz using wavelength division multiplexing (WDM). The combination of several of these fibers together to form fiber ribbon cables results in terahertz aggregate bandwidths. Using methods such as time-division multiplexing (TDM), code-division multiple access (CDMA), time-division multiple access (TDMA) and packet switching, several digital channels of voice, data, and video are carried and ultimately demultiplexed at the receiving end of the fiber[3]. At such large aggregate bandwidths, the routing and processing of all the channels through an electronic backplane becomes a tremendous and impracticable undertaking.

1.2 Electrical backplane limitations

In a metal interconnection based electrical backplane, connections between printed circuit boards (PCBs) are formed by the physical contact of metal traces or pins with parallel metal trace lines as shown in Figure 1.1. While high bandwidth metal interconnects

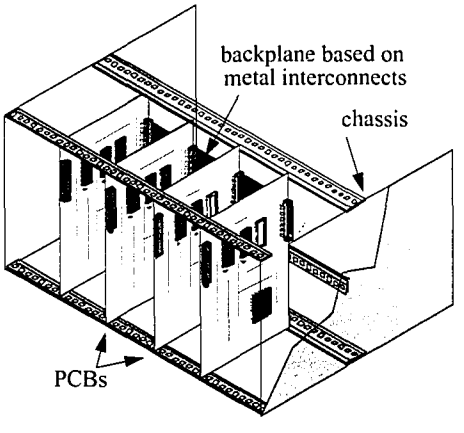

Figure 1.1 - Conventional electronic backplane based on metal interconnects.

using different metal-based technology standards such as Rambus, Ramlink, and Scalable Coherent Interface (SCI) have been proposed and implemented for parallel metal inter-

c. ...ects to meet clock speeds up to 500 MHz, they are limited by the intrinsic characteristics of the technology they employ, and show no indication that the bandwidth and connectivity are scalable for high-speed board and backplane interconnections needed for future processor systems[2]. Its limitations are the result of the following intrinsic characteristics of high speed electrical interconnects:

- Limited connection density

  High performance PCB backplane connectors require ground pins between signal carrying pins in order to limit crosstalk to acceptable levels. Although novel interconnection technology using flex circuitry, Button, and High Density Connectors (HDC) have been proposed and produced to increase connection density, signal contacts significantly more than 250 per linear inch of PCB edge are still unrealizable[4]. Thus, a ten inch PCB still cannot conceptually support much more than 2500 pin-outs.

- Large power consumption and dissipation

  Emitter coupled logic (ECL) is one of the fastest logic circuit families and typically used in very high bandwidth applications. However, ECL logic gates dissipate about 25mW to 40mW of power[5], and a typical ECL backplane line driver can consume up to 134 mW[6]. Hence, a 1000 line backplane will dissipate 134W on line drivers alone. Further, to minimize switching (ΔI) noise, several large and well regulated power supplies wll be needed to handle large current swings with minimum changes in supply voltage[7][8].

- Signal reflections and skew

  Signals can only travel a distance of 25 cm or less at 1 GHz before multiple signal reflections appear and the metal traces characterized with a distributed model[7]. Significant waveform distortion of greater than 25% and multiple reflections limit backplane-level interconnect lengths to less than 200 cm at a maximum bandwidth of 500 MHz[2]. For a given pitch between boards in a chassis, this limits the maximum number of interconnectable PCBs. In addition, to ensure that each load on the bus receives transition pulses at approximately the same time, the allowable variance in line lengths and hence interconnect delays in a bus becomes more stringent at higher bandwidths.

- Capacitive and inductive coupling of lines

  In high bandwidth systems with very short rise times, the inductive and capacitive coupling between lines increase in tandem with the line density.

- Limited simultaneous connection

  Since all the PCBs in the chassis share the same bus, only one PCB can communicate to the other PCBs at any given instant.

1.3 Free-space optical backplane

In contrast, free-space optical interconnects overcome the physical limitations experienced by metal interconnects[9][10][11]. Each optical channel is established by linking two optoelectronic transceivers through free-space using optical components. The development of the transceivers with processing electronics results in smart pixels having multifunctional capabilities. Two-dimensional arrays of smart pixels can thus perform a variety of parallel optical processing functions on arrays of optical input data[12]. The free-space interconnection of several of these arrays can form a photonic backplane having enormous processing and interconnection abilities and is illustrated in Figure 1.2. In

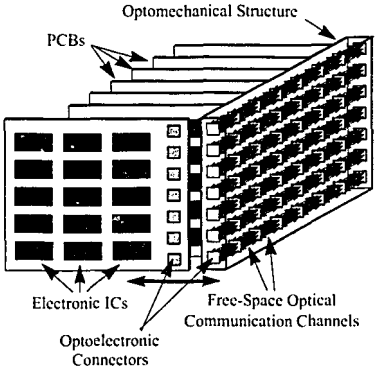

Figure 1.2 - Concept of a free-space photonic backplane[1].

addition, the smart pixels should also be dynamically reconfigurable to allow the rapid programming of the backplane to form a real-time reconfigurable three-dimensional interconnection network. The potential benefits has resulted in research efforts into architectures such as the Hyperplane, Hypercube, and the three-dimensional extended generalized shuffle (EGS) that can take advantage of the dynamically reconfigurable interconnects[6][13]. As an example, the physical size of large systems such as the Cray T3D Supercomputer can be significantly reduced by embedding its network topology into that

of an optical backplane[14].

The network can be fabricated to be very compact and have a very large density of optical interconnections using conventional low cost, high volume, high reliability monolithic integration techniques. The compact nature of the smart pixel array minimizes chip size, power consumption, and on-chip electrical interconnections. Therefore, overall timing delay and skew across a large array of interconnections are readily reduced. Furthermore, the massive connectivity and high bandwidth of photonic devices enhance and complement the processing power of current and developing electronic technology. By using the well advanced infrastructure already established by electronic technology, the performance of a backplane can be considerably improved by integrating optics and optoelectronics to create a high performance photonic layer in a conventional backplane chassis.

1.4 Smart pixel technology

The challenges facing the successful implementation of an intelligent optical backplane are very much dependent upon which smart pixel technology is employed. These technologies can be categorized as being based upon either modulator or emitter type devices. Modulator type devices impress signals onto an external light source in response to an electrical input whereas the latter creates its own optical signals and thus eliminates the need for an external optical source. Examples of modulator based smart pixels are AT&T's system demonstrators from 1988 to 1993[15][16]. They utilize GaAs field-effect transistors (FET) integrated with multiple-quantum-well (MQW) self-electro-optic effect devices (SEED) to form FET-SEED smart pixels. Despite high processing rates, FET-SEED smart pixels lack the functionality of current electronic processors. To overcome this limitation, MQW SEED modulators have been flip-chip-bonded to complementary metal-oxide-semiconductor (CMOS) circuitry. CMOS is unquestionably one of the best technologies for low current and power operation.

Among the emitter-based devices, vertical-cavity surface-emitting lasers (VCSELs) are one of the most promising. Large one and two dimensional arrays are pos-

sible. VCSELs, however, are an emerging technology and have yet to be integrated with large scale and highly dense transistor logic. Nevertheless the technology is rapidly evolving, and VCSELs have been monolithically integrated with a few GaAs MESFETs and MSMs[17].

1.5 Motherboard and daughterboard concept

Free-space optics and optoelectronics are better suited for interconnection distances of a few inches or less. Where dispersion effects become significant and the physical routing of the optical signal complex as for longer interconnect distances, guided wave structures such as fibers are a more appropriate solution. Excellent examples of such an application are fiber optics for long distance telecommunications and more recently, for multiple high speed cabinet to cabinet parallel links[18][19]. In short interconnection applications, free-space optics offers significant advantages. The integration and alignment of the transmission medium (free-space) to the optics and optoelectronics can be dismissed. Thus, the optical components and optomechanical support structure of the photonic backplane can be made relatively simple. In addition, the density of interconnections is not limited by the guided wave structure (such as cladding for fibers) and makes possible the realization of the large space-bandwidth product of the optoelectronic devices[20].

The defining question is where the smart pixels are integrated. They can be packaged onto the PCB with all the other processing and memory ICs (mohterboard) or physically decoupled and packaged onto a separate PCB (daughterboard) and electrically connected to the motherboard with ribbon cables or flexible PCB. While the former approach seems advantageous in that the smart pixels and electronics can be integrated altogether onto a single PCB, it suffers from two important considerations. Motherboards usually have a large number of ICs and connectors and thus tend to be relatively large and heavy. The repeated extraction and insertion of these PCBs to within the tight alignment tolerances required to interconnect the high bandwidth high density smart pixel arrays of neighbouring boards is a difficult if not unattainable goal. Secondly, the removal of a

board with its associated smart pixels results in a discontinuity of the backplane. Thus, where ever boards have been removed, the optical components would have to be sufficiently sophisticated to relay the signals across these gaps in the backplane. Furthermore, the optics would have to accompllish this task without significant attenuation or loss of signal. This invariably results in increased complexity of the optical components and also becomes an immense undertaking. Both complications are avoided by using the motherboard/daughterboard concept illustrated in Figure 1.3. By using high speed microstrip rib-

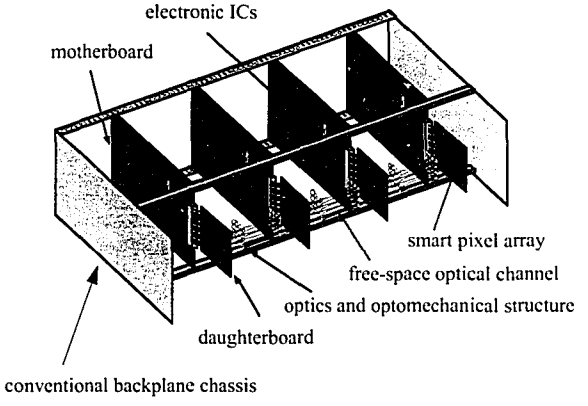

Figure 1.3 - Motherboard/daughterboard concept of a free-space optical backplane.

bon cables or flexible PCBs to mechanically decouple the motherboard from the daughterboard, the alignment and relay integrity of the photonic backplane formed by the daughterboards are preserved. As illustrated in Figure 1.4, multiple board to board communication across the entire backplane is possible. Since the interconnection length between the daughterboards and motherboards can be made very short (much less than 25 cm), high bandwidths of several gigahertz are easily achieved. In turn, bandwidths many orders of magnitude larger are supported by the photonic layer.

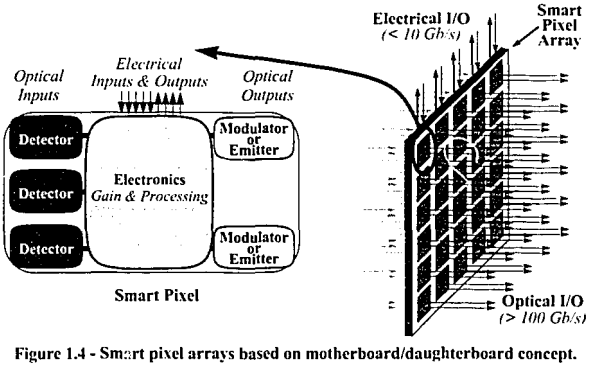

Figure 1.4 - Smart pixel arrays based on motherboard/daughterboard concept.

1.6 Project Overview

The Photonics Systems Group of McGill University, with the support of the Canadian Institute for Telecommunication Research and Nortel Technologies, is investigating the potential of free-space photonic backplane systems. Through the design, construction, and testing of yearly demonstrators that show a proof of concept, the long term objective of the group is the implementation of a representative portion of a large scale ATM switching system within a photonic backplane. Both the architectural and the hardware aspects of the free-space optical backplane are being investigated. The first demonstrator, *Phase I*, was based on modulator (FET-SEED) technology and was constructed on a slotted baseplate. The second demonstrator, *Phase II*, shown in Figure 1.5 employs VCSEL and MSM photodetector technology and represents a move to emitter based smart pixels within a conventional electronic chassis. The authors contribution was in the design, implementation and characterization of the receiver assembly of the Phase II demonstrator system.

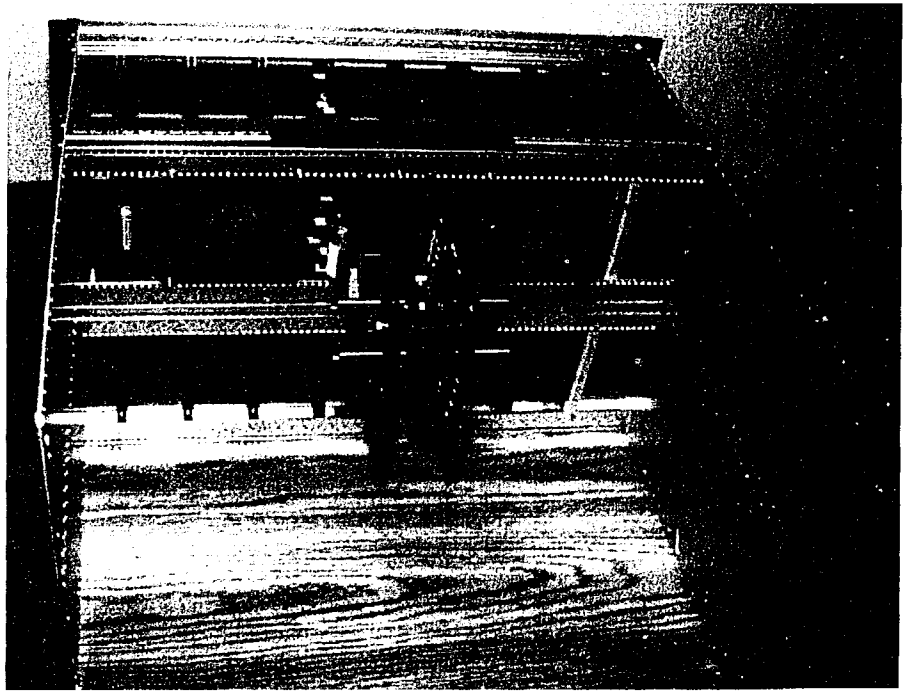

Figure 1.5 - VCSEL-MSM free-space optical backplane demonstrator.

1.7 Thesis organization

Following an introduction to the concept and motivation for free-space optical backplanes, the subsequent chapters are organized as follows. Chapter two discusses the basic requirements of a photodetector by describing the operation of metal-semiconductor-metal (MSM) photodetectors and reviewing the current technology used to enhance their performance. In chapter three, the current status of the integration of the MSM photodetector to form an optoelectronic receiver circuit is investigated for the GaAs material system by addressing integrated structures, common pre-amplifier designs, and performance issues. This leads to a detailed decription in chapter four of the design and construction of the receiver part of the Phase II VCSEL/MSM system. Following a description of the test assembly and environment, the characterization of the receiver assembly in the controlled environement and in the demonstrator system is presented in Chapter five. To conclude, chapter six summarizes the constraints, limitations, and areas for improvement in future systems.

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Chapter 2

Metal-semiconductor-metal optoelectronic receiver

2.1 Introduction

In a free-space optical backplane, the photodetector plays the fundamental role of detecting the modulated light passing across the optical interconnects. The semiconductor properties of the devices are exploited to convert the optical signals to electrical signals. Once converted, the information is interpreted and processed using conventional circuit technologies. The realization of this function in a properly working optical backplane places stringent demands on the photodetector. To achieve large aggregate bandwidths within such a media, the photodetector must have short response times, be well isolated from one another, and be monolithically or hybridly integrated with low-noise preamplifiers to form highly functional optoelectronic integrated circuits (OEIC).

As will be seen, metal-semiconductor-metal (MSM) photodetectors may have an advantage over p-i-n photodiodes in such future systems. The p-i-n photodiode is currently one of today's most commonly used semiconductor photodetectors. It is formed by creating an intrinsic, i-region, between two heavily doped p and n contact layers. The dark current arising from doping centers is also suppressed since the intrinsic layer contains fewer defects. Its popularity stems from having the flexibility to tailor the thickness of the absorption region to optimize either the quantum efficiency in order to collect as much incident light as possible, or the frequency response in order to detect faster modulated light signals. However, as the absorption region is made thicker to improve quantum efficiency, the carrier transit time will increase and thus lower the photodetector's frequency response. The bandwidth of the photodiode may also be limited by its junction capacitance. Given that the layers are typically arranged one on top of another, the capacitance can be approximated as that formed from a parallel plate capacitor:

$$C = \frac{\varepsilon_S \varepsilon_O \cdot A}{d} \tag{2.1}$$

where ε_s is the permittivity of the semiconductor between the doped layers; ε_0, the permittivity of free space; A, the photodiode area, and d, the photodiode absorption layer thickness. Hence, the capacitance is seen to vary linearly with the area, and for circular or square devices, in quadrature with the radius or side length respectively. Large area p-i-n photodiodes therefore suffer in speed performance, and must be made very small to reduce the RC time constant, which is the product of the equivalent resistance and the photodiode junction capacitance.

The problem is that the performance of such high speed semiconductors cannot be realized unless they are properly packaged. As will be seen in the following chapter, this involves critical optical alignments of the photodetector to the input optical signal, and can form a significant, if not limiting, portion of the OEIC cost. These requirements can be greatly relaxed by using MSM photodetectors that have been fabricated with large active light collection areas without significant bandwidth degradation. Such detectors are being explored and aggressively researched to realize Japan's fiber-to-the home (FTTH) and the United States' fiber-to-the-node (FTTN), or fiber-to-the-curb (FTTC) communications systems where alignment of a small p-i-n photodiode to an 8-10 μm diameter long haul single-mode fiber may be too costly[1]. Critical alignment issues can be even more challenging for a free-space optical backplane, and arises from aligning two-dimensional arrays of receivers to a two-dimensional array of optical input signals to achieve large aggregate bandwidths. In such applications, large area high performance MSM photodetectors may have an advantage over conventional p-i-n photodetectors.

The following section will qualitatively discuss the basic physical operation of the MSM photodetector. An expression for the capacitance is presented and compared to that of the p-i-n photodiode. Section 2.3 describes the advantages of using MSM photodetectors in high performance optomechanically sensitive systems. In comparison to mature p-i-n photodiode technology, MSM photodetector technology, however, is evolving. Section 2.4 reviews the disadvantages of employing MSM photodetectors and the methods by which these difficulties are currently being overcome. Then the last section reviews three commonly used types of preamplifier configurations and their respective performance tradeoffs.

2.2 Characteristics

The study of MSM structures began in the early 1970's and consists of back-to-back Schottky diodes formed by interdigitated metal fingers on top of a semiconductor[2]. Each set of interdigitated fingers connect to a pad for connection to an external circuit. The active light absorption layer is formed by the semiconductor material and is sensitive to the wavelength of interest. The low dispersion and high transparency of optical fibers at wavelengths of 1300 and 1500 nm requires InP-based alloys, and in particular InGaAs material is used[5][6]. For short-haul lightwave applications, GaAs is typically used for wavelengths of 830 to 850 nm[7][8][9]. The photons are detected by collecting electric signals generated by photoexcited electrons and holes in the semiconductor that drift under an applied electric field between the fingers. Thus, the fingers act as electrodes for collecting carriers. The holes drift to the negative electrode and the electrons to the positive electrode. As the carriers travel to the fingers, a displacement current registers in the external circuit. Figure 2.1 illustrates the electric field lines in the semiconductor below the elec-

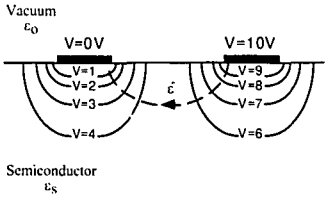

Figure 2.1 - Equipotential electric field lines below two representative electrodes of an MSM photodetector[10]

trodes. The generated photocurrent in the external circuit ceases when the last electron or hole reaches the fingers. However, even without an incident optical signal, a small amount of dark current is generated by the MSM photodetector. The dark current results from thermally created electron-hole pairs within the semiconductor's active region, and from carriers which overcome the Schottky barrier height. Figure 2.2 shows an energy band diagram depicting the Schottky barrier heights of two representative fingers of an

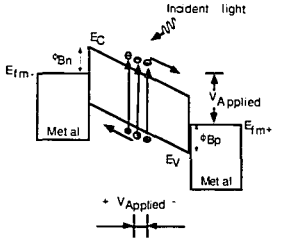

Figure 2.2 - Energy band diagram of an MSM photodetector showing the Schottky barriers (ϕ_{Bn} and ϕ_{Bp}) of both metal-semiconductor junctions[1].

MSM photodiode under bias. The Fermi levels of the metals are represented by E_{fm-} and E_{fm+}, and that of the valence and conduction bands of the semiconductor by E_V and E_C respectively. From Figure 2.2, the Schottky diode's potential barrier (ϕ) is determined by the metal and semiconductor work functions whereas the potential barrier of a p-n junction is determined only by the semiconductor's doping concentration. The rectified I-V characteristic of the Schottky diode is similar to the one-sided abrupt p^+-n junction, but instead occurs at the metal-semiconductor junctions. Further, since one diode is always reverse biased, the MSM photodetector has no preferred direction of bias, and the I-V characteristic is symmetrical about the origin. Another key difference is that under forward bias the Schottky diode is primarily a majority carrier device, with little minority carrier storage in the semiconductor. For an n-type semiconductor, on both sides of the junction, the electrons are the majority carriers. Since the majority carriers respond at roughly the dielectric relaxation time of the material, the depletion capacitance is independent of frequency up to very high frequencies, and in addition, compared to the p-n junction, it also has negligible diffusion capacitance[3]. The capacitance of the interdigitated metal electrodes of the MSM structure can be estimated using conformal mappings[11]. Assuming total depletion of the semiconductor epitaxial layer, the capacitance may approximated as a function of the finger width and spacing:

$$C = C_o \cdot \frac{A}{p} \qquad (2.2)$$

where A is the detection area of the photodetector; p, the center to centre finger spacing or pitch, and C_o, the capacitance per finger length given by:

$$C_o = \frac{\varepsilon_o(1+\varepsilon_r)K}{K'} \tag{2.3}$$

K and K' are the elliptic integrals defines as:

$$K = K(k') = \int_0^{\frac{\pi}{2}} \frac{d\theta}{\sqrt{1-k^2\sin^2\pi}} \text{ where } K' = K(k'),\ k' = \sqrt{1-k^2} \text{ and } k = \tan^2\frac{\pi w}{4p}$$

and w is the finger width. The capacitance per unit finger length for MSM photodetectors on GaAs and Si versus the ratio of finger width to pitch was examined and used to develop photodetectors with an f_{3dB} bandwidth of 510 GHz on low-temperature GaAs[12]. It was also experimentally shown that the detection area could be increased from 10x10 μm^2 to 20x20 μm^2 with only a slight decrease in bandwidth by varying the finger width and pitch. Thus, for a fixed window area, the MSM photodetector has the advantage of being able to minimize its capacitance by choosing an optimal finger width to pitch ratio[13]. As manufacturing technology continues to improve, higher performance MSM photodetectors can be attained.

2.3 Advantages

MSM photodetectors are fabricated using standard growth techniques such as molecular beam epitaxy (MBE), metal-organic-chemical-vapor deposition (MOCVD), liquid-phase epitaxy, and metal organic vapor phase epitaxy (MOVPE). As a result of its simple structure, the MSM photodetector has the following fundamental advantages:

1) planarity,

2) simplicity of fabrication,

3) low capacitance, and

4) process compatibility with transistor technology

First, the inherent planarity of the detector means that it requires only a single pho-

tolithographic step for fabrication in which the interdigital fingers and contacts are deposited. Thus, by simply duplicating the same structural layout, large one and two dimensional arrays for switching and optical backplane applications can be easily designed and fabricated without requiring additional photolithographic steps.

The MSM photodetector structure results in an inherently low capacitance, and can thus be fabricated with large light collection areas, or windows, without sacrificing bandwidth. This facilitates optomechanical coupling and alignment to multimode fibers[14][15][16], single thread or bundles of single mode fibers for FTTH, FTTN, and FTTC mentioned earlier, and microlenses[17] or other microoptics for multi-channel free-space and guided wave interconnects. Ironically, packaging issues can form a disproportionate portion of the total cost of an OEIC system, and especially in those requiring critical optical alignments. Interestingly, it is by using optics to transfer bit signals directly from one device to another, and thus circumventing the packaging layers of a carrier, printed circuit board and connectors[18], that extremely large aggregate bandwidths of a multichannel optical backplane are realized[19]. Proper coupling of the optical signal to the receiver forms a distinct packaging challenge of its own. If the package is designed improperly, the performance achieved from directly optically linking devices will not be attained. Since large active area MSM photodetectors can be made without significant speed penalty, they enable critical optical alignments to be greatly relaxed and the packaging constraints to be more palpable, which ultimately reduces the high cost of the OEIC system[1]. With a reduction in the cost, aggressive systems such as photonic switches, FTTH, and optical backplanes can become reality in the near future.

A significant and growing trend is the monolithic and hybrid integration of optoelectronic devices to meet the high degree of functionality required in OEIC systems. To detect an optical signal, not only must the light be collected, but also converted to a usable electrical signal. This usually entails one or more amplifiers, and may include an equalizer for removing signal distortions, and a filter for maximizing signal-to-noise ratio. Such functions are performed by transistors. Interconnecting the MSM photodetector with the amplifier circuity as discrete components using arbitrarily long wires suffers from large parasitic inductances and capacitances[20][21]. At high speeds, the signal becomes

distorted and the system is limited to relatively low bandwidths. In addition, the packaging of each individual component requires more surface area and decreases component density. For a given area, this limits the potential functionality of the system. Through monolithic or hybrid integration, however, devices can be placed tightly together. Long line length parasitics are reduced, and potential system functionality is simultaneously improved. The I-V characteristic of MSM photodetectors strongly resembles the output characteristics of a GaAs field-effect transistor (FET), and thus the design techniques used for FET circuit can often be directly applied to MSM photodetectors that are used in analogous circuit configurations[22]. Integration of MSM photodetectors with the FET is also straightforward since the interdigitated fingers of the MSM photodiode and the gate fingers of a FET can be defined with the same photolithographic step and then deposited with the same metallization. As an indication of the commercial viability of the process, Vitesse Semiconductor currently sells 1 GHz MSM photodetectors integrated with GaAs FET circuitry. Even in the 1.3 to 1.5 μm wavelength range where several steps are required using a technique such as heteroepitaxial growth for matching structural differences of commonly used devices such as FET's, HEMT's, and HBT's to InP-based materials, the development of an InGaAs-transferred-electron devices with Schottky gate-electrode (STED) reduces the required number of photolithographic steps to four, and only requires two epitaxial layers for the whole receiver[23]. The simplicity of the integrated circuit indicates that future high functionality InP based monolithic OEIC systems may soon be a reality.

2.4 Disadvantages

There are a number of drawbacks of MSM photodetectors, and only by overcoming these obstacles has MSM photodetectors become a viable alternative to conventional photodetectors. MSM photodetectors tend to[1]:

1) require fine feature sizes,

2) suffer from low responsivities, and

3) have non-uniform metal-semiconductor interfaces

To reduce the capacitance and transit time of carriers, MSM photodetectors typically need finger width and spacings of a couple of microns or less. These feature sizes are smaller than that normally found with p-i-n photodiodes, and in comparison, have been more difficult to fabricate reliably. Recent advances in electron-beam lithography and photolithography, however, has made sub-micron feature sizes more commonplace in both academia and industry. For example, feature sizes as small as 0.35 μm are already featured in today's dynamic RAM and microprocessor chips, and are projected to become even smaller in the decade ahead[24].

As a result of reflections from the metal interdigitated fingers, responsivities of traditional MSM photodetectors tend to be lower than that of p-i-n photodiodes. Also, the finite carrier lifetimes caused by surface recombination currents and deep traps within the semiconductor serve to decrease the photogenerated current seen by the external circuit[1][4]. Several innovative methods have been researched to improve the absorption efficiency of the photodetector. Buried Bragg reflector stacks have been used to improve absorption efficiency without increasing the thickness of the active layer for bandwidths in excess of 39 GHz, and reported internal quantum efficiencies as high as 82% for a 5V bias[25]. Reflections off the interdigitated fingers have been minimized by using transparent conductors such as indium tin oxide (ITO) and cadmium tin oxide (CTO) instead of the standard Ti-Au electrodes for particular wavelengths of interest. ITO has been used to almost double responsivities to 0.76 A/W at a wavelength of 1.3 μm[26], and with the addition of a thin WSi_x film, to 0.44 A/W at 1.55 μm[27]. Semi-transparent contacts have met with similar success with reported responsivities of 0.65 A/W at 840 nm[28] and 0.7 A/W at 1.55 μm[29] using tungsten and extremely thin gold contacts respectively. Some small improvements (5%) were also found by depositing SiN_x antireflection coating between the fingers[30]. The largest responsivity improvement so far was obtained by constructing a thin film inverted MSM in which the fingers were deposited on the bottom of the device and bonded to a Si host substrate to achieve a record 95% external quantum efficiency at 1.3 μm with a 5.9 GHz bandwidth[31].

In all of the above approaches, the absorption region was kept relatively thin.

From Figure 2.1, it can be seen that carriers created deep within the active area must first slowly diffuse to the junction edge. Upon reaching the electric field lines created by the applied voltage, the carriers can then drift to the electrodes at the saturation velocity. Therefore, increasing the thickness of the absorption layer to improve absorption efficiency results in a reduction in the photodetector speed response. However, despite maintaining a relatively thin absorption layer, using ITO electrodes to improve responsivity still results in a reduction of the bandwidth. This is due to the longer transit time of the carriers generated beneath the higher resistivity ITO electrodes[8]. Nevertheless, bandwidths in excess of 5GHz were still achieved.

In arrays of MSM photodetectors, the removal of unwanted semiconductor can prevent carriers from being created outside the electric field lines of the active area. This mesa etch is a common technique for electrically isolating one device from another on top of a semi-insulating substrate. Further electrical isolation improvements were found by using a ground plane that was monolithically integrated with a photoconductive array[32]. One of the most challenging problems with MSM photodetectors is that a significant amount of charge can build up on the surface and pin the semiconductor Fermi level[1][36]. Thus, the actual Schottky barrier heights will fall short from theoretically designed values. This dampens the rectification characteristics of the metal-semiconductor junction, and for narrow bandgap materials like InGaAs, small signals are lost in the excessive dark current. Furthermore, slight imbalances in the Schottky barrier heights and charge accumulation can lead to poorer MSM detector isolation[33]. The charge accumulation arises from free atomic bonds on a clean semiconductor surface. To lower their potential, these bonds react readily with oxygen and other elements in the air, and as a result accumulate charge. To prevent this from occurring, silicon nitride, sulfur and plasma passivation have been found to be effective in decreasing the dark current two to three orders of magnitude less than non-treated photodetectors to achieve dark current densities of less than 0.1 pA/μm^2 for a 5 V bias[34][35][36][37]. The process also has the benefit of producing very reliable and reproducible devices[38][39]. For InGaAs in particular, another technique that works well is to incorporate a thin lattice matched large bandgap (E_g=1.5 eV) InAlAs layer between the metal and low band gap region to increase the effective Schottky barrier

height[5][40].

The aforementioned difficulties, however, are not unique to MSM photodetectors in particular, and occur when fabricating metal semiconductor field effect transistors (MESFETs)[41][42] and high electron mobility transistors (HEMTs)[39]. Fabrication and manufacturing technology refinements of these devices in these areas will also lead to similar improvements for the MSM photodetector as they together become more commercially available.

2.5 Amplifier design and performance

For optical interconnects to attain high aggregate bandwidth, each photoreceiver must be compact and have low power requirements in order to obtain high connection densities. Therefore, it is of interest to explore means for designing very compact photoreceiver circuits that do not require an extensive amplifier system. By using monolithic integrated circuit technology, and using as few devices as possible, the power consumption can be very low and is generally not a limiting factor of the design. Three amplifier designs will be discussed: resistor terminated, high impedance, and transimpedance amplifiers. Often, the limiting factor in each of the above cases is obtaining a sufficiently large voltage signal swing at the output such that it can directly drive the input to a logic gate while maintaining a large bandwidth.

2.5.1 Resistor terminated

Many of the earliest OEIC receivers used a simple resistor terminated design shown in Figure 2.3. A buffer amplifier is often coupled for impedance matching. The necessary condition for this design is that the resistive load is an order of magnitude smaller than the MSM resistance during dark operation such that the output is pulled to ground, and under illumination operation, the resistance of the MSM must fall to an order of magnitude smaller than the load such that the output is pulled to the power rail. The bandwidth is determined by the RC time constant of the input, where R is the biasing

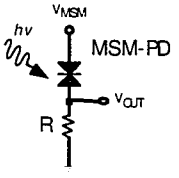

Figure 2.3 - MSM photodetector with resstive load.

resistance and C is the sum of the photodetector and the voltage-gain amplifier input capacitances. Thus for small values of R, the bandwidth can be quite large, but at the expense of signal gain, which is determined by the input logic gate. Further, the small biasing resistor dominates the input noise, leading to poor receiver sensitivity. Nevertheless, this configuration is the easiest to monolithically integrate, requiring only a resistor and a FET, and has been demonstrated to operate at low gigahertz frequencies[22][44].

2.5.2 High impedance amplifier

The high impedance (HZ) amplifier design replaces the above resistance with an active load such as a FET and is capable of giving the absolute minimum noise and has demonstrated exceptional bandwidth of 8 GHz with MESFETs[45] and 16 GHz with HEMTs[46]. As in the resistance terminated design, buffered logic is often used for impedance matching and voltage level shifting. The impedance of the active load can be changed as the operating point of the device switches with the illumination level. When under dark operation, the MSM conducts very little current and the FET active load is placed into the non-saturating current range, which gives it a very low impedance and hence the output is pulled to ground. When illuminated, the MSM resistivity drops, current flows, placing the FET active load into the saturating current range where its differential output resistance is greatly increased. This change in the differential output resistance of the load requires less than one decade of change in the resistance of the MSM[22]. As a result, the use of active loads can achieve greater output voltage swings, a greater regener-

ation of the digital signal, and thus establish a more distinct switching threshold for the input signal. Active loads can be easily fabricated with the photodetector in the same way as they are for any other logic gate by using either depletion or enhancement mode FET's. In the configuration of Figure 2.4a), with the MSM connected to the positive power sup-

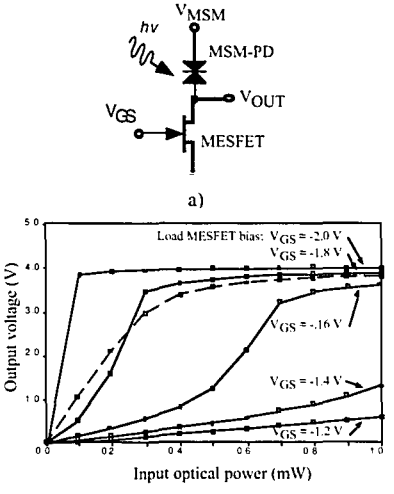

Figure 2.4 - a) MSM photodetector with active load. b) Meaured output voltage of MSM photodetector with varying gate bias. Dashed line is for a 50 kΩ resistive load[22].

ply, maximizing the output voltage swing then requires that the MESFET be able to produce a larger saturated current than that of the MSM detector, which is much less of a restriction with a fixed optical power supply. In comparison, for the case where the MSM and MESFET positions were reversed, the photodetector would have to produce the greater power supply. Furthermore, the switching threshold can be easily tuned by applying a reverse bias to the gate, resulting in a reduced MESFET saturated current. Conversely, it is more difficult to increase the input power from the optical source. The above described input stage consisting of an MSM and MESFET active load produces a sufficient output voltage signal swing and current to switch the input of a standard MESFET

logic gate[22]. Figure 2.4b) illustrates the output power for a varying optical power and gate source voltages of the active load. As an example of the tuning capability of the amplifier, note that the change in the gate bias of the FET active load from -2.0 V to -1.6 V changes the optical threshold from 0.05 to 0.60 mW. Such control allows for automatic compensation of a fading optical signal power, or for controlling the gating of the input electric signal. Nevertheless, HZ amplifiers still suffer from a few shortcomings. First the amplifiers may need to be individually equalized with feedback resistors due to their inherent sensitivity to device and temperature variations, and further, the front end of the high impedance reduces the dynamic range of the amplifier compared to the transimpedance amplifier[47].

2.5.3 Transimpedance amplifier

The transimpedance (TZ) amplifier is the most commonly used amplifier design in OEIC receivers due to its wide bandwidth and dynamic range of operation. The amplifier consists of an inverting voltage amplifier (T1, T2) made from enhancement and depletion MESFETs with resistive feedback from output to input as illustrated in Figure 2.5. The

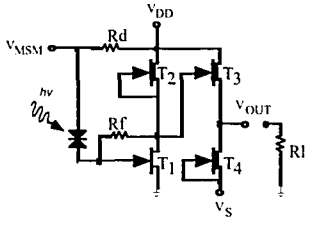

Figure 2.5 - Transimpedance OEIC receiver where R_f=800 kΩ, R_d=50Ω, and R_l=50Ω[49].

output buffer stage (T3, T4) is used for impedance matching. In practice, the noise performance is not as good as that achieved from a HZ amplifier; however, at high bit rates, the noise performance gap decreases[47][48]. The performance of the amplifier can be quanti-

fied. The highest sensitivity (lowest noise) of a transimpedance amplifier is obtained by maximizing the ratio g_m/C^2 where g_m is the transconductance of the input transistor and C the total input capacitance of the FET gate and photodetector[49]. This figure of merit reveals three methods for improving the TZ amplifier sensitivity. First, by reducing the capacitance of the input node through monolithic integration of high performance electronic devices; second, by reducing the capacitance of the photodetector; and third, by increasing the transit frequency of the input transistor:

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{3.4}$$

by using devices such as sub-micrometer MESFETs with a short gate length. Furthermore, the bandwidth of the amplifier can be determined. The transimpedance gain Z_T of the amplifier can be approximated at low frequencies to be:

$$Z_T = -\frac{R_F}{1 + \frac{1}{A_V}} \tag{3.5}$$

where R_F is the feedback resistance and A_V is the open loop voltage gain, assuming that the conductances of the photodetector and FET are negligible to $1/R_F$[48]. Also, the 3-dB frequency of the transimpedance amplifier with a single dominant pole is given by:

$$f_{3dB} = \frac{A_V + 1}{2\pi R_F (C_{in} + C_F (1 + A_V))} \tag{3.6}$$

where C_{in} is the input capacitance to the FET voltage amplifier and C_F is the parasitic shunt capacitance across the feedback resistor. Thus, to achieve wide bandwidth and low noise, the open-loop voltage A_V must be very large such that R_F can be kept high for noise reduction[47]. Recall that the resistor terminated design suffered from comparatively high noise due to its low terminated resistance in order to maintain a high bandwidth. Further note however, that even if A_V were to approach infinity, the bandwidth would still limited by the R_FC_F time constant. A useful figure of merit is the transimpedance gain-bandwidth product (TZBW), which is independent of the feedback resistance:

$$TZBW = Z_T \cdot f_{3dB} = \frac{A_{1'}}{2\pi C_{tot}} \tag{3.7}$$

where

$$C_{tot} = C_{in} + C_F(1 + A_{1'}) \tag{3.8}$$

With the objective of maximizing the TZBW, improvements in the amplifier design is can thus be related directly to maximizing the open-loop voltgae gain through amplifier design and device structure. This can be accomplished in the MESFET case by increasing the g_m/g_d ratio where g_m is the transconductance of transistor T1 and g_d is the sum of the output conductances of transistors T1 and T2. This can be accomplished using thin channels and a buried p-layer in MESFETs, and device scaling to minimize total input capacitance. This has been demonstrated using MESFET technology to achieve a bandwidth of 5.2 GHz[49]. Comparatively, a MODFET based photoreceiver achieved a bandwidth of 8.2 GHz[48]. Of all the three designs, the TZ design consumes the most power as a result of having both a comparatively large chip area and power supply current, since they must constantly operate each device at a large quiescent current to achieve class A amplification[22][50]. For instance, the transimpedance design of Figure 2.5 dissipates 75 mW, two thirds of which is dissipated in the source follower, at an operating voltage of 2.5 V. For a large number of such discrete photoreceivers, as would be required in a connection intensive optical interconnect, the cumulative power consumption can be considerable, and is the main drawback in the TZ design. Monolithic integration of multichannel receivers can provide a remedy. As demonstrated in the low 2 W receiver power consumption of a high-density 32-channel optical link, with the monolithic integration of multichannel receivers, devices can be made more compact and power consumption can be significantly reduced.

2.6 Conclusion

Owing to the ease of fabrication, simplified packaging, and monolithic or hybrid integration of MSM photodetectors with current and developing technologies, these photodetectors are beginning to find a presence in today's marketplace. Large window sizes

coupled with inherently low capacitances make MSM photodetectors an ideal choice for alignment critical OEIC systems. Due to its simple structure, MSM photodetectors requiring as few as six photolithographic steps with GaAs MESFETs[42] and four with InGaAs STEDs[23] have been demonstrated. Although certain manufacturing refinements still need to be addressed, highly functional MSM photodetector based OEIC receivers can soon be expected in the marketplace.

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Chapter 3

Design and construction of receiver assembly

3.1 Introduction

A measure of the fidelity of an optical communications system is the signal-to-noise ratio (SNR) and bit error rate (BER) for analog and digital systems respectively. The fundamental goal in the design of an optical receiver is to minimize the amount of optical power needed by the receiver to achieve a target performance figure. This optical power is commonly known as the sensitivity of the receiver. In optical backplanes, minimizing optical power requirements become even more important as higher speeds, and larger connectivies through higher smart pixel densities are pursued. However, in practical systems, other competing considerations influence the design of the system, and can result in a receiver with less than optimal sensitivity.

One such factor that will be examined is achieving a wide dynamic range for reliable optical to electrical data conversion. The dynamic range quantifies the range of optical power levels within which a target BER or SNR is ensured. This becomes particularly important in systems where the spread of possible detected optical powers is broad.

This chapter begins with a description of a 4x4 MSM photodetector array layout used in the receiver of the VCSEL/MSM system. The dependency of the photodetector active area dimensions on the misalignment tolerances and optical power coupling characteristics of the system is then analyzed. This approach leads to developing a minimum acceptable receiver dynamic range in terms of the optomechanical alignment tolerances, maximum optical power variations, and key characteristics of the photodetector and receiver amplifier. From this expression, the system's optomechanical stability will be seen to place boundary conditions on the allowable extent of the receiver's dynamic range. From these parameters, the chapter concludes with a two phase approach to the design and construction of a 16 channel hybrid MSM/transimpedence smart pixel receiver.

3.2 MSM photodetector array layout

The layout of the MSM photodetector array was accomplished through a consideration of the MSM fabrication technology at the Center for Electrophotonic Materials and Devices at McMaster University (CEMD), the physical characteristics of the transmitter array, a 4x4 array of 850 nm vertical cavity surface emitting lasers fabricated by VIXEL Inc., and the optical system used to relay the light signals to the MSM photodetectors. These constraints resulted in a 4x4 layout with each MSM photodetector having a finger width of 2 μm and spacing between fingers of 2 μm over a 50x50 μm^2 active area. The finger width and spacing dimensions were chosen for reproducibility and ease of fabrication using standard photolithographic techniques. To maximize the best possible signal to noise ratio and preserve signal integrity, it was determined that it would be desirable to trade off the frequency response against optical signal coupling of the photodetector by selecting a relatively large active area. It will be seen that the choice of active area was the largest possible given the centre to centre spacing requirements of the photodetectors and minimum trace widths and spacing, and yet the design still resulted in small photodetector capacitance. The gain in optical power coupling and misalignment tolerance due to the large active area will be considered in the following section.

To match the center to center spacing of each of the VCSELs, the MSM photodetector centers were spaced 125 μm apart in x and y respectively. The layout is shown in Appendix A. Around the periphery of the central 4x4 array are additional photodetectors and passive devices that were used in alignment experiments, and will not be discussed in this text. The 10 μm wide trace lines were limited to a single layer, and thus connected each MSM photodetector of the array to the nearest bond pad without any crossovers. A minimum spacing of 10 μm between trace lines was also maintained. From these constraints, it was found that all the MSMs in a column had to share a common contact, or bias rail, to minimize the number of trace lines and for all of them to be routable to a bond pad. This is particularly evident in the center of the array. As a result, the trace line width and spacing, and center to center spacing of the photodetectors set an upper limit on the active area size and is demonstrated from the following example. The five detectors in the second column required at least three trace lines to be routed to the top side of the chip.

With 10 μm widths and spacings, and including the trace line for the bias rail of the first column, 70 μm of lateral space is thus occupied by trace lines between the centers of the photodetectors. For 125 μm center to center spacing between the photodetectors, this then leaves 55 μm for the two half active areas of the photodetectors in column one and two. Equivalently, each square photodetector can thus have a maximum of 55 μm on a side. For power coupling considerations discussed in the following section, 50 μm was chosen. The sharing of bias lines thus required only four bias lines into the chip. Additional unconnected bond pads were added for testing and calibrating the wirebonder. After delivery of the layout, the detector array was fabricated and optimized by CEMD for 840 nm[1]. A photograph of the MSM detector array and a drawing of the MSM layer structure are shown in Figure 3.1. The capacitance of each of the MSMs of the array were measured using an HP 4277A LCZ meter to be 0.3 pF or less for a bias voltage greater than 3V[1]. This was found to be sufficient in the receiver designs discussed in this chapter.

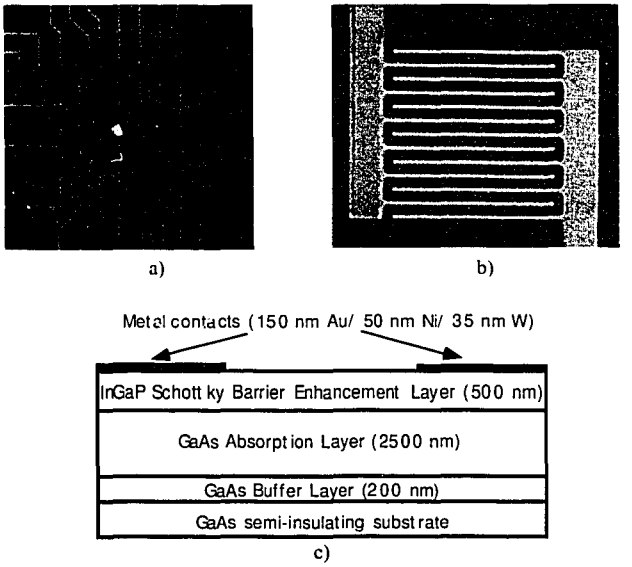


Figure 3.1 - Photograph of a) 4x4 MSM detector array fabricated by CEDM b) close up of a MSM photodetector, and c) MSM photodetector layer structure.

3.3 Coupled optical power

Based on maximizing the received signal power introduced in the previous section, the physical characteristics of the VCSELs, and the manner in which the laser beams were relayed and focused onto the MSM photodetector array will be shown to determine a range of optimal dimensions for the photodetector active area. From this range, an active area size was chosen. To illustrate the process in determining this feature, a review of the optical relay system is introduced, followed by the derivation of an expression for power coupling, and then the effects of spot size variations and misalignments on optical signal power coupling are discussed.

3.3.1 Optical system

The optical system used in the demonstrator is illustrated in Figure 3.2. Due to the VCSELs large full angle at half maximum (FAHM) of 10° to 15°, and a maximum 30 nm

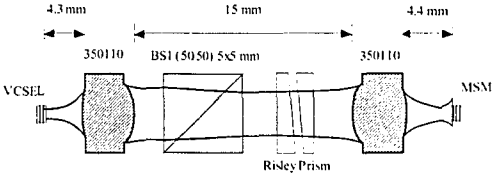


Figure 3.2 - Optical system used in the demonstrator to relay optical signals from the VCSEL array to the MSM photodetector array.

wavelength variation across the transmitter array[2], Thor Labs 350110 aspheric lenses having an f-number of 1.67 were used to collimate and focus the array of laser beams. The 4-f telecentric system formed by the bulk lenses permitted the convenient addition of a beamsplitter for illuminating and imaging the photodetector array, and Risley beam steerers to finely position the incident laser beams. To reduce the coupling of reflections from the MSM photodetectors back to the VCSELs, the photodetector array was slightly defocused from its image plane, and resulted in a calculated spot radius, ω, of 9.1 μm on each of the MSM photodetectors when assuming a Gaussian irradiance distribution[3].

This optical signal from the VCSEL and optical relay system formed the input to the receiver array and will be seen from the following sections to set a lower limit on the photodetector active area.

3.3.2 Expression for coupled power

The following analysis will provide a theoretical basis for quantifying the effects of different spot sizes and MSM photodetector active areas on the fractional coupled power. This consideration futher leads to the following section where the effects of misalignments on optical power coupling at the receiver are quantified. To begin, let the MSM photodetector array lie in the xy plane with the z axis pointing towards the incident optical beams. Further, let the spot be centered at x=0 and y=0, and to have a gaussian irradiance given by:

$$I(x,y) = I_o e^{-2\left((x^2+y^2)/w_o^2\right)} \tag{3.1}$$

where w_o is the spot radius. If the active area A of the photodetector is defined by the boundaries $x=x_1$ to $x=x_2$, and $y=y_1$ to $y=y_2$ where $x_1<x_2$, and $y_1< y_2$, then the total coupled light power within this area is then given by:

$$P_c = I_o\int_{x_1}^{x_2}\int_{y_1}^{y_2} e^{-2(x^2+y^2)/w_o^2}\,dxdy = I_o\int_{x_1}^{x_2} e^{-2x^2/w_o^2}\,dx\int_{y_1}^{y_2} e^{-2y^2/w_o^2}\,dy \tag{3.2}$$

Substituting $u = \dfrac{\sqrt{2}x}{w_o}$ and $v = \dfrac{\sqrt{2}y}{w_o}$ yields

$$P_c = \frac{I_o w_o^2}{2}\int_{\frac{x_1\sqrt{2}}{w_o}}^{\frac{x_2\sqrt{2}}{w_o}} e^{-u^2}\,du\int_{\frac{y_1\sqrt{2}}{w_o}}^{\frac{y_2\sqrt{2}}{w_o}} e^{-v^2}\,dv \tag{3.3}$$

$$= \frac{I_o w_o^2\pi}{8}\left[erf\left(\frac{x_2\sqrt{2}}{w_o}\right)-erf\left(\frac{x_1\sqrt{2}}{w_o}\right)\right]\left[erf\left(\frac{y_2\sqrt{2}}{w_o}\right)-erf\left(\frac{y_1\sqrt{2}}{w_o}\right)\right]$$

The total power is found to be $\dfrac{I_o w_o^2\pi}{2}$ for an infinitely large detector area. Therefore, the

fraction of the total power coupled by the finite active area A leads to:

$$\frac{P_c}{P_{total}} = \frac{1}{4}\left[erf\left(\frac{x_2\sqrt{2}}{w_o}\right) - erf\left(\frac{x_1\sqrt{2}}{w_o}\right)\right]\left[erf\left(\frac{y_2\sqrt{2}}{w_o}\right) - erf\left(\frac{y_1\sqrt{2}}{w_o}\right)\right] \tag{3.4}$$

From equation 3.4, Figure 3.3 illustrates that to capture the maximum incident optical

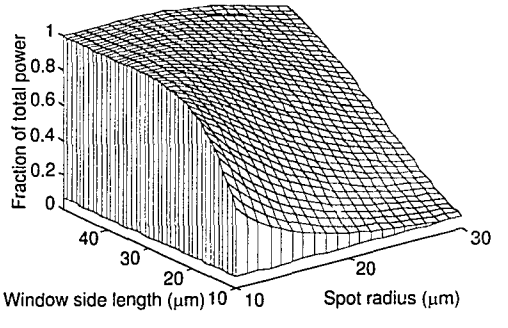


Figure 3.3 - Fraction of total power coupled for varying active area sizes and spot radii.

power having a spot radius of approximately 10 μm would require a photodetector with a square active area greater than 25 μm (97.5% coupling) on each side.

3.3.3 Misalignment tolerance

Misalignments result from vibrations, shock, mechanical stress, and thermal effects that are ever present in the optomechanical nature of the optical system in a backplane environment[4]. Hence, misalignments between the receiver assembly and the optical system will occur and will result in deviations from certain design parameters. Most importantly, the relayed light beams may stray from their exact intended positions on the photodetectors, which would result in less coupled power. To compensate, the photodetector active area can be increased. From the analysis to follow, the consequences of translational misalignments in x, y, and z, and rotation about z will be derived and subse-

quently quantified in terms of the fractional coupled power onto the photodetector. An increase in the lower limit of the photodetector active area from the previous section will then be concluded from a discussion of the results.

Misalignments in the z direction, or equivalently a defocus of the photodetector array from the light beams, results in an increase in the spot radius[5]:

$$w = w_o\sqrt{1+\left(\frac{\lambda\Delta z_e}{\pi w_o}\right)^2} \tag{3.5}$$

where λ is the wavelength of the light used, and w_o is the smallest radius of the spot and occurs at the beam waist for a perfectly aligned system. Thus, the effects of z misalignment on power coupling can be obtained by combining equation 3.4 and 3.5.

For Δx and Δy translational misalignments in the photodetector array, the fraction of the total coupled power is seen to be given by:

$$\frac{P_c}{P_{total}} = \frac{1}{4}\left[erf\left(\frac{\sqrt{2}}{w_o}\left(x_2-\Delta x\right)\right)-erf\left(\frac{\sqrt{2}}{w_o}\left(x_1-\Delta x\right)\right)\right]\left[erf\left(\frac{\sqrt{2}}{w_o}\left(y_2-\Delta y\right)\right)-erf\left(\frac{\sqrt{2}}{w_o}\left(y_1-\Delta y\right)\right)\right] \tag{3.6}$$

and explicitly relates the spot radius w_o, the location of the active area with respect to the beam, and translational x and y misalignments to the fractional coupled total power.

Assuming the center of the photodetector array coincides with the optic axes of the system, and adopting the photodetector array axes as the reference frame, then a rotational misalignment of the detector array can be equivalently mapped as a translation in x and y of the spot array as seen in Figure 3.4. For the following consideration, the corner spots initially lying on the x=y axis are of the most interest as they are the farthest from the origin and will move the greatest distance, $r\Delta\theta$, for a given rotation $\Delta\theta$ where $r=187.5\sqrt{2}$ for a 125 μm separation between spots. The equivalent translation for these corner spots are:

$$\Delta x = \frac{r}{\sqrt{2}}\left(\cos\Delta\theta-\sin\Delta\theta-1\right) \tag{3.7}$$

$$\Delta y = = \frac{r}{\sqrt{2}}\left(\cos\Delta\theta+\sin\Delta\theta-1\right) \tag{3.8}$$

Combining these two equations with equation 3.6 relates the rotational misalignment to

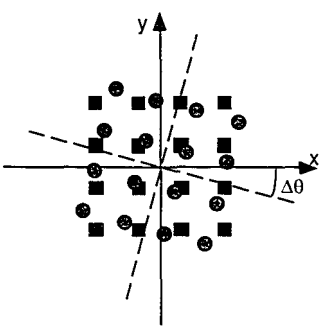
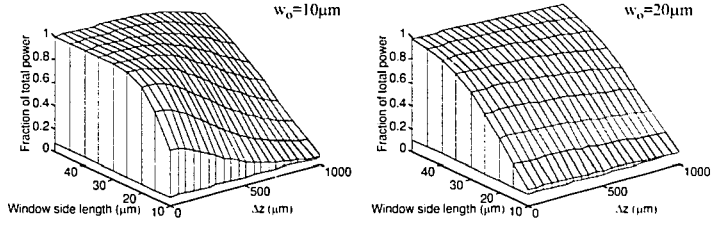


Figure 3.4 - Translation resulting from a rotation in the photodetector array.

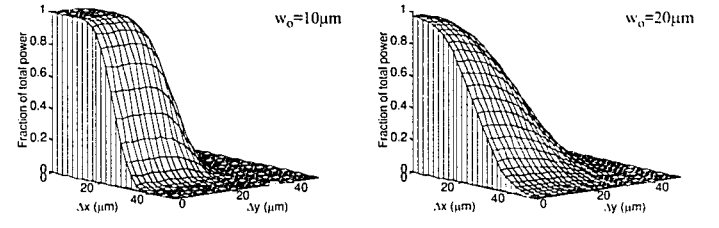
the power coupling for these corner photodetectors.

The results of each of these misalignments are quantified in Figure 3.5 for different square photodetector window side lengths and spot sizes of w_o=20 μm and w_o=10 μm in order to find a lower bound on the MSM photodetector active area. In the best case, the w_o of the spots relayed through the optical system would approximately reach the designed value of 9.1 μm. In the worst case, and to be conservative, it was assumed that the resulting w_o of the system demonstrator incident beams could have doubled and would not have been noticed on the CCD camera due to the limited resolution and contrast of the imaging and illumination system, or would be perceived, but could not be reduced to less than twice the target value of 9.1 μm because of alignment constraints. When misalignments are considered, it is evident that using 25 μm as the lower bound initially determined in Section 3.3.2 results in considerably less coupled power. This is particularly the case if w_o were to increase to 20 μm. Also, from Figure 3.5a) and c), the coupled power is seen to drop more abruptly for larger misalignments when the spot size is small. This is particularly noticeable for even small rotational misalignments of 0.1 rad (5.7°). In this situation, constant and reliable operation of the receiver for such power variations would thus require a design with very wide dynamic range. The wide dynamic range requirement can be relaxed by reducing the possible power coupling variations due to this misalignment in two ways. The first is to intentionally use a spot with a large w_o. This results

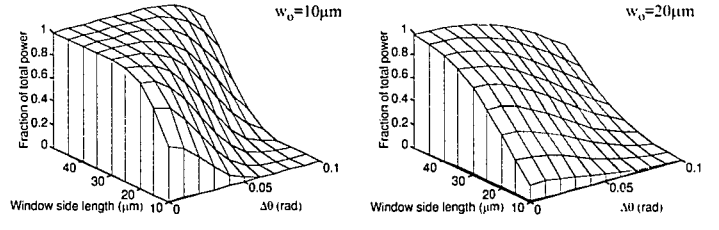
in gradual coupled power variations for a fixed window size and varying misalignments.



a)



b)



c)

Figure 3.5 - Fraction of total power coupled for misalignments in a) z direction, b) x and y directions for a 50x50 μm² window, and c) rotation by Δθ for spot radii w_o=10 μm and w_o=20 μm.

A significant drawback is that the coupled power is significantly reduced, and would then require a receiver with high sensitivity. This tradeoff is avoided by instead increasing the

window size such that for the equivalent misalignments considered before, both high fractional and gradual variations in coupled power are both maintained. With only trace lines surrounding each MSM photodetector, a near maximum active area of 50x50 μm^2 both maximizes coupled power for improved sensitivity, and relaxes the required dynamic range by minimizing the extent of coupled power variations due to the misalignments.

Furthermore, it is worth noting that increasing the active area size does not lead to significant leakage of optical signals onto adjacent photodetectors of the array. This is true for even large misalignments. For example, from the equations considered earlier, a deviation of up to 50 μm of an w_o=20 μm spot results in less than 0.001% optical power coupling on its nearest 50x50 μm^2 photodetector neighbour. Thus, optical coupling onto adjacent photodetectors will be assumed to be negligible in future discussions.

In the demonstrator, the placement and fastening of the optics inside a custom barrel piece shown Figure 3.6 provided good optomechanical stability and allowed the

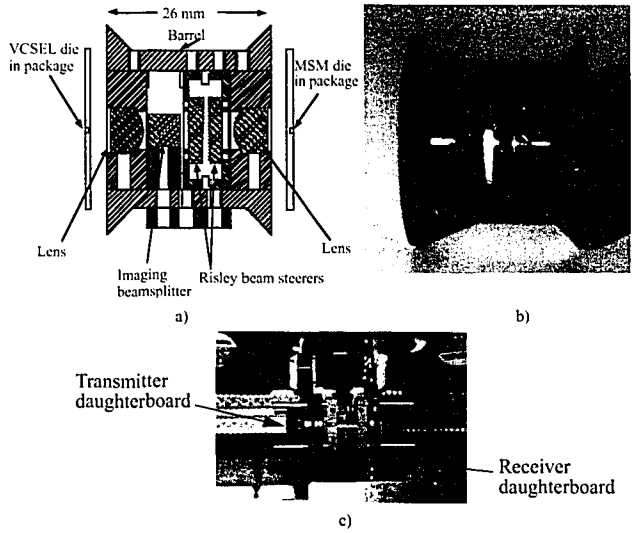


Figure 3.6 - Barrel optomechanics used to position the optics and fasten the transmitter and receiver daughterboards.

receiver daughterboard to be mechanically coupled using a Spindler&Hoyer plate. The complete assembly provided x, y, and z axis translations and rotations for aligning the daughterboards. After the boards were fastened, a less than 2 μm misalignment drift was discernible over a three week time period.

3.4 Dynamic range

An optical receiver will have both a minimum optical input power below which it cannot detect signals and a maximum optical input power above which the output will have unacceptable levels of distortion. The dynamic range is defined as the ratio of the these maximum to minimum input optical power signals and expressed in dBm. A knowledge of the receiver's dynamic range is thus crucial in predicting if the relayed optical signals will be correctly interpreted by the receiver circuit. Since the transimpedance amplifier forms the front end of the receiver, its performance characteristics will fundamentally determine its dynamic range. The analysis of this section will formulate an expression for the dynamic range, which can then be used in the following sections to quantify the effects of MSM photodetector dark current, amplifier performance figures, and optomechanical misalignments of the receiver daughterboard.

Assuming a Gaussian noise distribution, which is sufficiently accurate for design purposes in estimating the receiver's sensitivity to within 1 dB of a more precise analysis[6], and an equal probability of a zero or a one bit transmission, then the probability of an error in interpreting the received bit is given by:

$$P(e) = \frac{1}{2} erfc\left(\frac{SNR_{opt}}{2\sqrt{2}}\right) \tag{3.9}$$

where the optical signal to noise power ratio (SNR_{opt}) is given by[7]:

$$SNR_{opt} = \frac{i_{sig}}{i_{nRMS}} \tag{3.10}$$

where i_{sig} is the peak signal current, and $i_{nRMS}=\sqrt{\overline{i_n^2}}$ the root mean square (rms) input

noise current. Therefore, to achieve a probablity of error P(e)=10^{-9}, or equivalently, a bit error rate (BER) of 10^{-9}, an SNR_{opt} of at least 12 to 1 at the input of the transimpedance amplifier is needed[7]. Thus, to achieve this BER, the average worst case minimum peak input power, can be estimated in terms of the following variables[8]:

a) the input spectral noise current of the amplifier, i_{SNCamp},
b) the input resistance of the amplifier, R_{IN},
c) the input capacitance of the amplifier, C_{amp},
d) the maximum input current to the amplifier, i_{MAXamp},
e) the rms MSM photodetector dark current, $i_{MSMdark}$,
f) the MSM photodetector capacitance, C_{MSM}, and
g) the responsivity of the MSM photodetector Rsp_{MSM}.

To begin, the bandwidth of the input stage is given by:

$$f_{3dB} = \frac{1}{2\pi R_{in}\left(C_{amp} + C_{MSM}\right)} \tag{3.11}$$

and thus the rms noise current of the transimpedance amplifier is then

$$i_{Namp} = \sqrt{\left(i_{SNCamp}\right)^2 \cdot f_{3dB}} \tag{3.12}$$

where $i_{SNCamp}$is a measure of the shot and thermal noise of the input stage, and is limited by the bandwidth as determined above. Geometrically combining the rms MSM photodetector dark current then leads to the total input referred noise current as:

$$i_n = \sqrt{\left(i_{Namp}\right)^2 + \left(i_{MSMdark}\right)^2} \tag{3.13}$$

For an optical SNR_{opt}=12, $i_{sig}=12i_{nRMS}$, and hence the minimum peak optical signal input power, also defined as the receiver's sensitivity, is found to be:

$$P_{min} = \frac{i_{sig}}{Rsp_{MSM}} \tag{3.14}$$

As a result of assuming an equal probability of a one or zero optical bit transmission, the receiver's average sensitivity is half P_{min} and is also sometimes quoted. Future references

to receiver sensitivity will refer to P_{min} and not the average value. The maximum optical input power is determined by the transimpedance amplifier's maximum input signal current and photodetector responsivity:

$$P_{max} = \frac{I_{MAXamp}}{Rsp_{MSM}} \tag{3.15}$$

Thus, the optical dynamic range is then

$$D_{opt} = P_{max} - P_{min} \quad \text{dBm} \tag{3.16}$$

However, to recall from Section 3.3.3, the misalignment tolerances of the optical system predetermines the absolute minimum required dynamic range of the receiver:

$$D_{optomech} = P_{Max}(\Delta x_{min}, \Delta y_{min}, \Delta z_{min}) - P_{Min}(\Delta x_{max}, \Delta y_{max}, \Delta z_{max}) \quad \text{dBm} \tag{3.17}$$

where $P_{Max}(\Delta x_{min},\Delta y_{min},\Delta z_{min})$ is the maximum and $P_{Min}(\Delta x_{max},\Delta y_{max},\Delta z_{max})$ the minimum coupled power (dBm) resulting from respective minimum and maximum spot misalignments on the receiver board. If the power variations of the light source is known, then a more explicit expression from equations 3.5 and 3.6 follows:

$$P_{Min}\left(\Delta x_{max}, \Delta y_{max}, \Delta z_{max}\right) = \frac{P_c\left(\Delta x_{max}, \Delta y_{max}, \Delta z_{max}\right)}{P_{total}} \cdot P_{Lmin} \quad \text{(dBm)} \tag{3.18}$$

$$P_{Max}\left(\Delta x_{min}, \Delta y_{min}, \Delta z_{min}\right) = \frac{P_c\left(\Delta x_{min}, \Delta y_{min}, \Delta z_{min}\right)}{P_{total}} \cdot P_{Lmax} \quad \text{(dBm)} \tag{3.19}$$

where P_{Lmin} and P_{Lmax} are the respective minimum and maximum optical powers for a high bit incident on the photodetector. Thus, the range of coupled optical signal power onto the photodetector must completely fall within the receiver's dynamic range to achieve a minimum BER. From equations 3.14, 3.15, 3.18, and 3.19, these boundary conditions are equivalently expressed as:

$$P_{Min}\left(\Delta x_{max}, \Delta y_{max}, \Delta z_{max}\right) > P_{min} \tag{3.20}$$

$$P_{Max}\left(\Delta x_{min}, \Delta y_{min}, \Delta z_{min}\right) < P_{max} \tag{3.21}$$

If the misalignment tolerances are too loose for a chosen photodetector's dark current such that the aforementioned ranges only partially overlap or not at all, the receiver system will not be capable of reliably achieving the minimum targeted BER. Thus, if a given photodetector's dark current, receiver amplifier's input spectral noise current, and optical system's misalignments are all unavoidably large or intractable, then an increase in the minimum optical input power, P_{Lmin}, is required to preserve received signal integrity measured in terms of a BER. It is also interesting to note from the above, that an alternate, possible solution is to tradeoff amplifier bandwidth. However, as is evident from equations 3.12 and 3.13, no amount of bandwidth reduction will negate the deleterious effects of a large photodetector dark current if a good first stage amplifier with extremely low spectral noise current is used. The point at which bandwidth reductions will no longer have an effect may be quantified as when:

$$\left(i_{MSMdark}\right)^2 \gg \left(i_{SNCamp}\right)^2 \cdot f_{3dB} \tag{3.22}$$

where f_{3dB} defines the bandwidth of the amplifier. Hence, bandwidth reduction is not always a panacea, nor is it usually desirable in high aggregate bandwidth systems.

As described in Section 3.3.3, the VCSEL/MSM demonstrator was tolerant to relatively large misalignments due to the choice of large photodetector active areas, and in practice, experienced less than a 2 μm drift which in turn placed minimal receiver dynamic range requirements. Assuming an w_o=20 μm spot and a 2 μm translational misalignment in each of the x, y, and z directions from a perfectly aligned position thus results from equations 3.5 and 3.6 in a required dynamic range of 0.0156 dBm (97.18% misaligned optical coupling vs. 97.53% maximum coupling). Further, as an indication of the stability of the system, the required dynamic range would only increase to 0.494 dBm if each of the misalignments were quintupled to 10 μm. Both cases fall well within the designed receiver optical dynamic ranges of larger than 20 dBm for a BER 10^{-9} to be considered in the following sections. These results, however, cannot be used to interpret that the receiver was over designed for the following three reasons. First, power fluctuations of the individual VCSELs during single channel operation, and in particular between discrete VCSELs of the array during parallel channel operation was unknown and not

accounted for. These power fluctuations can be substantial, and must also fall within the receiver's dynamic range for reliable optical to electrical signal conversion. Second, as will be seen in Chapter 5, a similar phenomenon occurs with the MSM photodetector array in that the addition of leakage currents from surrounding photodetectors during parallel channel operation will increase each of the MSM photodetector's input noise current. These leakage currents can severely reduce the receiver's optical dynamic range by increasing the minimum required optical input power. Lastly, even if the effects of the previous two considerations were minimized through improved device isolation and fabrication processes, a lower BER than 10^{-9} may be required. While a BER of 10^{-9} may be sufficient for digital speech transmission, an error occuring in for example computer data communications may pose severe problems, and it would be necessary to incorporate error detecting and correcting circuits. In this case, a much lower BER ($<10^{-14}$) would be desirable[9].

3.5 Phase I: Rapid prototyping speed-wire board

In order to simplify and reduce assembly time, the design was implemented on VERO speed wire boards. Despite the obvious drawbacks such as limited bandwidth and large electrical crosstalk from large exposed pins and wires, its reusability and ready reconfigurability made it a more appropriate choice than custom printed circuit boards in designing a first phase receiver assembly.

3.5.1 Design

The first receiver design used Philips Semiconductors' NE5212A low power, 140 MHz transimpedance amplifiers to convert the MSM's small photogenerated currents into usable voltage signals. These signals were then converted to TTL levels by companion NE5217 fiber optic postamplifiers, and the wiring diagram is illustrated in Figure 3.7. Besides its large bandwidth, the transimpedance amplifier was chosen because it provided low input spectral noise differential of $2.5 pA/\sqrt{Hz}$, low input and output impedances of 110 Ω and 30 Ω respectively, a maximum input current of 120 μA, and a significant differential transresistance, $R_T=V_{out}(diff)/I_{in}$, of 14.4 kΩ[10]. From these performance values, and MSM photodetector parameters, the dynamic range of the transimpedance amplifier

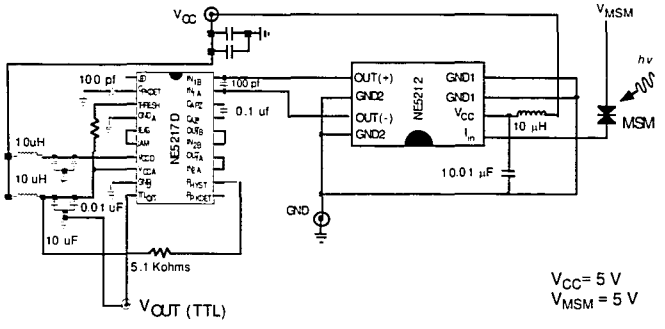
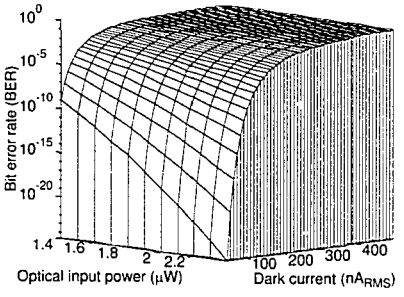


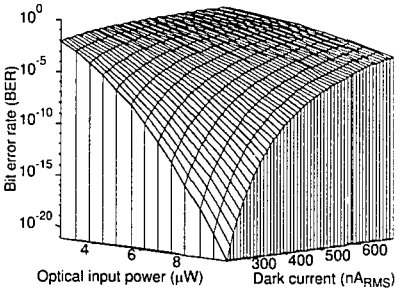
Figure 3.7 - Wiring schematic of one of four equivalent channels of the Phase I receiver circuit.

can be estimated using a signal-to-noise ratio based on the optical power coupled to the receiver as described in the previous section. For the NE5212A transimpedance amplifier using an MSM photodetector with Rsp_{MSM}=0.5 A/W, C_{MSM}=0.3 pF, and $i_{MSMdark}$=50 nA_{RMS} as described in Chapter 5, the optical dynamic range, D_{opt}, is calculated from Section 3.4 to be 22.3 dBm with a P_{min}=1.4 µW. As would be expected and is illustrated in Figure 3.8 for this receiver, as the photodetector's dark current increases, the bit error rate derived from the previous section increases. To compensate, the minimum coupled optical signal power would need to be raised, which in turn would reduce the dynamic range of the receiver. A particularly significant issue seen from the figure is that an increase in the dark current in the order of nanoamperes results in a required increase in optical signal power in the order of microwatts. In the lab environment, this is a severe problem in which radiation noise can easily produce several millivolts into a long lead 50 Ω load to generate several microamps of noise current. In this instance, the photodetector noise current would swamp the input spectral noise current of the amplifier at even low bandwidths, and a significant increase in the coupled optical signal power would be required. For the NE5212A transimpedance amplifier, an MSM photodetector noise current of 10 μA_{RMS} reduces the dynamic range to 0 dBm for a BER of 10^{-9}.

The NE5217 postamplifier system formed the decision making portion of the circuit, and consisted of eight amplifier blocks to provide up to 60 dB of gain to bring milli-



a)



b)

Figure 3.8 - Bit error rate vs. optical input power from a)1.4 μW to 2.8 μW and b) 2.8 μW to 9.6 μW for varying MSM photodetector dark current for the NE5212A.

volt signals up to TTL levels. DC coupling to the first stage having an input impedance of 1200 Ω was possible with a built in auto-zero loop that pulled out low frequency DC wander due to changes in the data pattern and the DC offset of the NE5212A transimpedance amplifier[11]. With a nominal 20% - 80 % rise time of 1.3 ns, and additional features such as an adjustable decision making threshold, hysteresis, and decay times, the NE5217 post amplifier was particularly suitable for capturing high speed low level signals in a noisy environment.

3.5.2 Construction

To implement the daughterboard/motherboard concept, the motherboard was of VME size 6U, and through a standard computer ribbon cable, was linked to a VME 3U daughterboard using 60 channel dual-in-line connectors. Optical signals received at the daughterboard were then relayed electrically to the motherboard. The output signals were then read from the motherboard using an AMP 50 Ω shielded cable assembly that terminated to 25 SMA connectors on one end, and a dual-in-line connector on the other. Through a female receptacle, the motherboard connected to the dual-in-line connector end of the AMP assembly. Figure 3.9 shows a photo of the complete daughterboard and motherboard assembly with interconnecting cables.

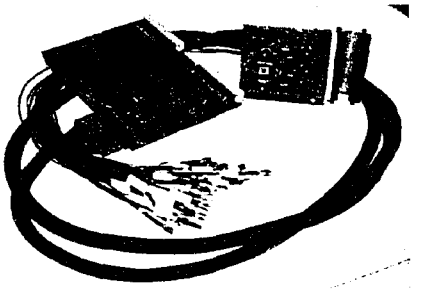


Figure 3.9 - Speed-wire daughterboard/motherboard assembly with interconnecting cables

The MSM photodetector array was packaged in an 18 pin dual-in-line (DIP) carrier using ball bonding. The carrier itself was surrounded by a Spindler & Hoyer mounting plate used to optomechanically fasten the daughterboard to the optical system. Together with constrained daughterboard dimensions for optomechanical stability as illustrated in an enlarged photograph of the daughterboard in Figure 3.10, only four transimpedance amplifiers could be placed both near the MSM photodetector package and the connector leading to the postamplifiers. The limited working area precluded the placement of the post amplifiers on the daughterboard. To reduce as much as possible any coupled radiative noise as well as parasitic resistance and capacitance, all four post amplifiers were placed on the motherboard as close as possible to the connector that interfaced to the daughterboard. Also, since the post amplifiers were only available in surface mount pack-

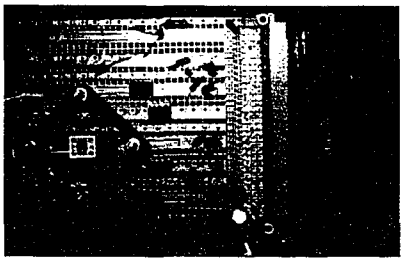


Figure 3.10 - MSM package and optomechanical plate on speed-wire receiver daughterboard.

ages, surface mount to pin adapters from Emulation Technologies were employed. The 100 pF capacitor between the differential inputs of the postamplifer shown in Figure 3.7 was placed on the motherboard side to reduce noise having an f_{3dB} above 54 MHz from the output signal from the transimpedance amplifier and noise coupled from the interface, and yet still permit a 50 Mb/s NRZ bit rate[8]. Although a well-regulated power supply, an HP 6235A, was used for each of the V_{CC}, and V_{MSM} power lines, they traversed relatively long distances to reach the receiver daughterboard, and RF chokes and bypass capacitors shown in Figure 3.7 were placed as close to the transimpedance and postamplifier package supply pins as possible. Potentiometers of ranges from 1 kΩ to 10 kΩ and 1kΩ to 100 kΩ were initially used at the postamplifiers's R_{HYST} and THRESH pins respectively. This was done in order to adjust the threshold decision and hysteresis voltage levels. These were later replaced with 5.1 kΩ and 47 kΩ resistors to give a threshold level of 12 mV and hysteresis of 3 mV. The four TTL outputs from the post amplifiers were then each wired to separate motherboard output pins. Similarly, each of the twelve unamplified outputs from the rest of the MSM photodetector array were wired straight from the daughterboard across the ribbon cable to separate motherboard output pins.

3.5.3 Test

The speed-wire receiver assembly described in the previous two sections was tested using the optical setup described in Section 5.2. The output from the motherboard was displayed on an HP 54120B digitizing oscilloscope using an HP 54124A DC to 50

GHz sampling unit. The measurement of the receiver included the daughterboard, motherboard, and interconnecting ribbon and AMP cable assemblies. The results shown in Figure 3.11 was obtained by shining an optical bit stream onto each of the MSM photodetectors one at a time. The naming convention corresponds to the MSM photodetector's row and column position within the array. The amplified outputs from MSM photodetectors 11, 14, 34, and 42 showed a full voltage swing of 2 V while the unamplified channels showed a voltage swing of less than 10 mV into a 50 Ω load. The particular four amplified photodetector outputs were chosen as a result of the corresponding VCSEL transmitters having realtively higher bandwidth during individual operation and large distances between them for heat dissipation[12]. It was found that the 2V swing from the amplified outputs into a 50 Ω load had reached the maximum output current specifications of the postamplifier. The typical high TTL output voltage of 3.4 V was seen when viewed on a high impedance input oscilloscope. In testing the complete VCSEL/MSM speed-wire assembly, these signals will be used as a controlled baseline. Since a 1 Mb/s 50% duty cycle square wave was chosen as the input waveform to the electrooptic modulator, a common time base of 500 ns/div was used. No signal was found on MSM 31. In front of the daughterboard, an optical low bit of 150 μW and an optical high bit of 400 μW was measured using a Newport 1835c power meter with an 818-ST/CM detector head. Since the optical output from each transmitter of the VCSEL transmitter array showed duty cycles that varied widely from 50%, and widely different rise and fall times[12], the light power of the low optical bit was intentionally increased from optimum to test the thresholding and hysteresis capability of the postamplifier thresholding circuit. The output waveforms of each of the amplified outputs are very uniform, showing 20% - 80% rise times of less than 20 ns (f_{3dB}=11 MHz). These rise times are considerably larger than the specified postamplifier rise times of 1.3 ns[11]. The unamplified MSM photodetector waveforms show very sharp rising edges that indicate a very wide f_{3dB} bandwidth which correlates well with the extremely small MSM photodetector capacitance mentioned earlier.

After testing the speed-wire receiver assembly, the receiver daughterboard was integrated into the optical system and aligned. The receiver motherboard was inserted into

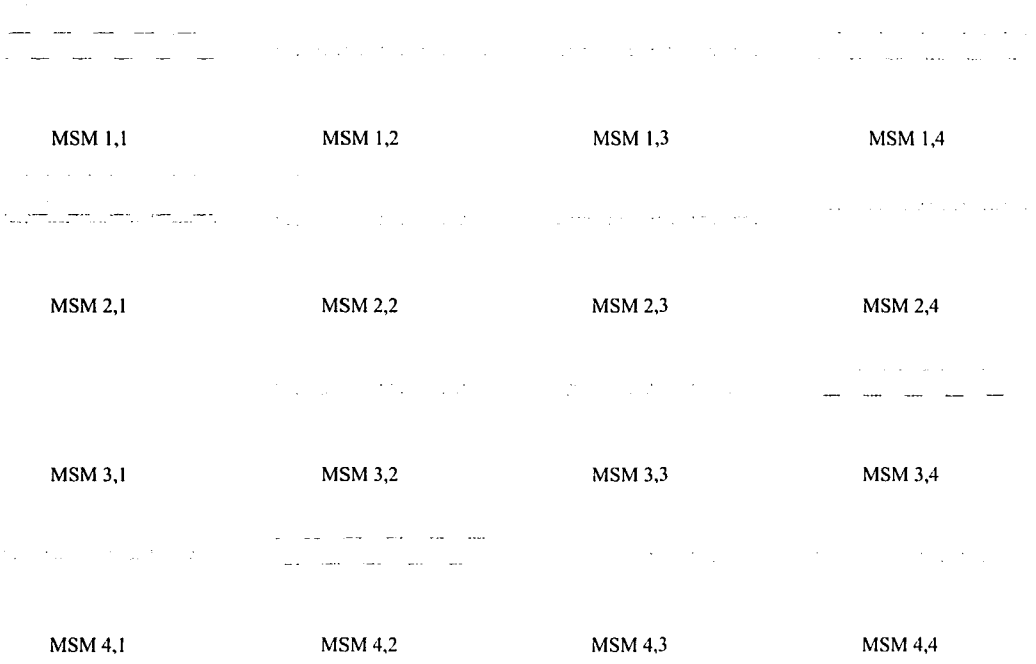


Figure 3.11 - Modulation of individual channels of the speed wire MSM assembly.

the chassis, and connected to the daughterboard via ribbon cable, and the parallel operation of the entire system tested. In this case, a 1 Mb/s 50% duty cycle square wave from the HP 80000 data generator system drove the VCSEL transmitter array. The four amplified receiver motherboard output signals were displayed on the digitizing scope. With the exception that the 20-80% rise times were found to increase to approximately 100 ns (f_{3dB}=2.2 MHz), the signals were found to correspond well to the modulated signals generated in the controlled test of each receiver channel. A diagram of the test layout and receiver output signals are shown in Figure 3.12. Despite its low performance rates, the

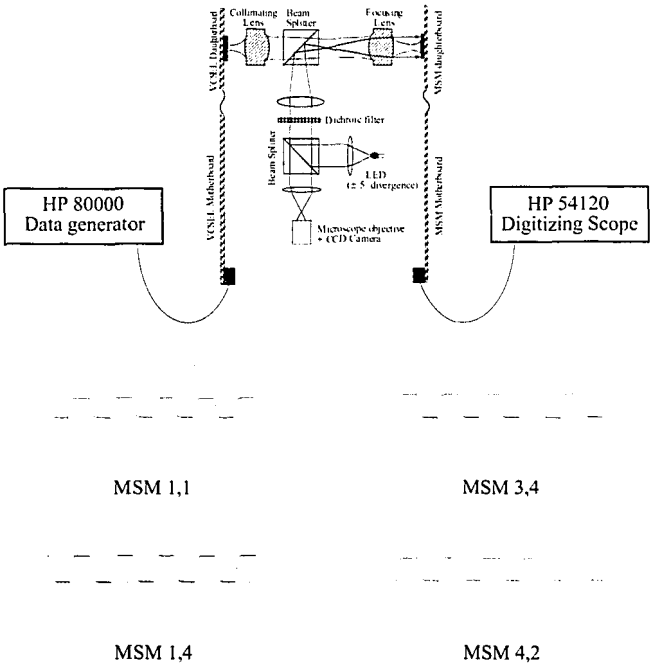


Figure 3.12 - Amplified receiver channels of the VCSEL/MSM speed wire system.

speed-wire boards permitted rapid prototyping and testing of the receiver electronics, optics, and optomechanics. The system showed good mechanical stability, and resulted in

low optomechanical dynamic range requirements that allowed the reliable operation of the system without realignment for extended periods. In addition, the Phase I prototype design, construction, and testing process helped identify key improvements.

3.6 Phase II: Impedance controlled printed circuit board

The integrity of a signal depends upon the medium through which it propagates. At high signal bandwidths, the electrical interconnect can no longer be treated as a short, or lumped load, and must be considered electrically active and modeled as a network of transmission lines with distributed capacitance, inductance, and resistance. As a common rule of thumb, this analysis is required when the rise time is less than five times the propagation time[13]. For example, a signal having a 2 ns rise time travelling in FR4, a commonly used material in printed circuit boards (PCB), could only travel along a conductor of approximately 14 cm before it must be characterized by a distributed model[14]. This critical length decreases to approximately 2 cm and less for signals generated by high speed devices having bandwidths greater than 1 GHz. In order to take advantage of the inherent high bandwidths of the MSM photodetectors, such devices were used in the receiver upgrade from Phase I, and thus required impedance controlled printed circuit boards for mounting and interconnecting devices.

3.6.1 Design

Two receiver designs were tested on a prototype PCB to determine which one should be used for the final receiver board assembly. The first was Philips Semiconductors' SA5222 and NE5224 chip set, and the second was modeled after Hewlett Packard's (HP) single channel *G-Link Optical Receiver* using their ITA-06300/ITA-06318 (prepackaged option) and IVA-05208 MagIC silicon bipolar MMIC chips. The SA5222 and NE5224 were slightly higher bandwidth and lower noise successors of the NE5212A and NE5217 pair, and had essentially the same circuit schematic described in the Phase I design. The HP set, however, had much larger bandwidths of 1.5 GHz, and the ITA-06300 transimpedance amplifiers came unpackaged. One of the constraints discussed in the Phase I design was the limited daughterboard space and the requirement that the transimpedance amplifiers be placed as close as possible to the photodetector to minimize parasitic capacitance, inductance, and noise. This resulted in the amplification of only four of

sixteen photodetector channels to usable TTL logic levels. As will be discussed in the following section, the amplification of all sixteen MSM photodector currents was achieved through hybridly packaging the HP transimpedance amplifier chips with the 4x4 MSM photodetector array; furthermore, the prototype board was also found to support the devices' high bandwidths. Thus, the HP chip set was chosen for Phase II, and the functional block diagram and circuit schematic for one of the sixteen receiver channels is shown in Figure 3.13. The ITA-06300/ITA-06318 1.5 GHz transimpedance amplifier

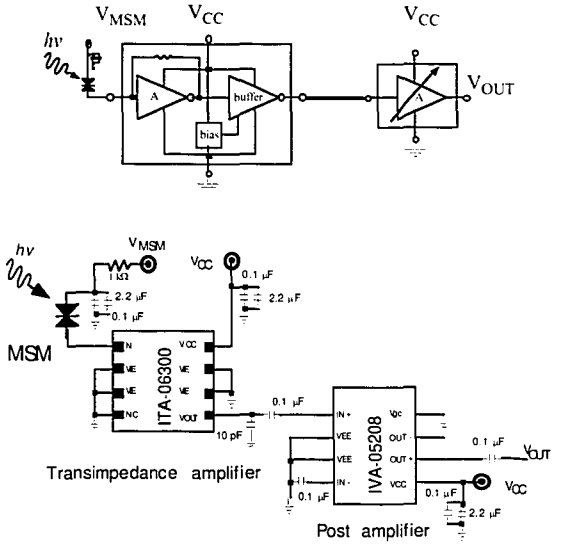


Figure 3.13 - Block diagram and corresponding wiring schematic of one of sixteen equivalent Phase II receiver channels.

provided a gain of 2800 Ω (69 dB) with an input spectral noise current of $7pA/\sqrt{Hz}$ at 1.5 GHz with a relatively low power consumption of 170 mW[15][16]. The IVA-05208 variable gain amplifier set in a limiting configuration was used as the postamplifier to provide differential ECL logic levels[17][22]. Despite the lower gain and higher input spectral

noise current of the transimpedance amplifier from that of the Phase I receiver, a high dynamic range was still obtained from a higher maximum input current of 450 μA. The dynamic range can be similarly estimated from Section 3.4 by using a signal-to-noise ratio based on the optical power coupled to the receiver. Assuming the same MSM photodetector with Rsp_{MSM}=0.5 A/W, C_{MSM}=0.3 pF, and $i_{MSMdark}$=50 nA_{RMS} as described in Chapter 5, the optical dynamic range, D_{opt}, is calculated to be 21.3 dBm with a P_{min} of 6.6 μW.

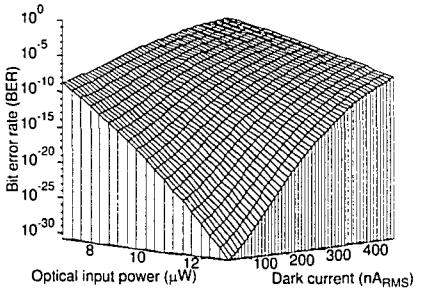


Figure 3.14 - Bit error rate vs. optical input power from 6.5 μW to 13 μW for varying MSM photodetector dark current

Comparing Figure 3.14 to Figure 3.8, as the photodetector's dark current increases, the bit error rate similarly increases, and can also be compensated by increasing the coupled optical input power, which in turn reduces the dynamic range. There are two notable differences. As described previously, the sensitivity is lower and hence requires a higher minimum optical input power. Secondly, the BER does not deteriorate as quickly with respect to increases in the MSM photodetector dark current. This is the result of a higher noise contribution from the transimpedance amplifier and an increased maximum acceptable input current before signal distortion occurs. As a comparison of the Phase I and II transimpedance amplifiers, Figure 3.15 shows the calculated BER for which the dynamic range is reduced to 0 dBm as a result of large photodetector dark currents. For a BER of 10^{-9}, a reduction of the dynamic range to 0 dBm requires an MSM photodetector noise current of 37.5 μA_{RMS}, and hence shows more tolerance to photodetector noise compared

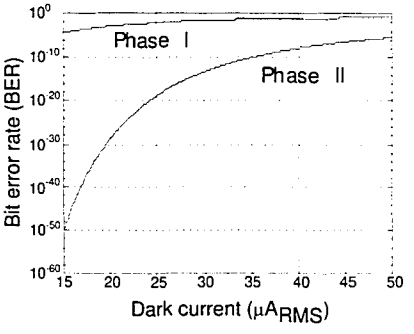


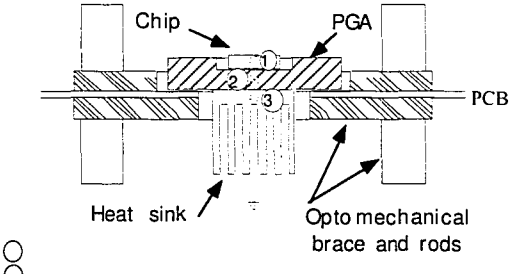
Figure 3.15 - Bit error rate vs the photodetector dark current for which the dynamic range is reduced to 0 dBm.

to the 10 μA_{RMS} found for the NE5212A transimpedance amplifier. The compromise, however, is an increase in the minimum amount of coupled optical input power.

A drawback in using transimpedance amplifiers is its constant power consumption, regardless of the presence or absence of an input signal. Even though each transimpedance amplifier has a relatively low power consumption of 170 mW, power from all of the 14 amplifiers (2.4 W) will be dissipated as heat within the package. This heat will cause an increase in the junction temperature of the amplifiers, and the temperature between the MSM contacts of the photodetector aray. If the temperature becomes too high, significant thermal noise effects will degrade signal fidelity[18], and permanent damage to the devices may occur. To monitor the temperature, a small glass thermistor was epoxied to the pin grid array package (PGA), and a heat sink used to help dissipate heat. Since the nature of the optoelectronic package required that the top be clear of obstructions, the heat sink was mounted in the back of the PGA through a hole in the PCB and affixed with silicon grease. The relationship between power dissipation and amplifier junction temperature rise above ambient is given by:

$$Q = \frac{T_j - T_a}{R_{jc} + R_{cs} + R_{sa}} \tag{3.23}$$

where Q is the dissipated power (W), T_j the junction temperature (°C), T_a the ambient air temperature (°C), and R_{jc}, R_{cs}, and R_{sa} are given by Figure 3.16. The thermal resistances of the conductive epoxy used to mount the chips to the PGA, and of the silicon grease



1 Thermal resistance from junction to semiconductor case, R_{jc} (°C/W).
2 Thermal resistance from semiconductor case to heat sink, R_{cs} (°C/W).
3 Thermal resistance from surface of heat sink to ambient air, R_{sa} (°C/W).

Figure 3.16 - Thermal resistances of the hybrid receiver package.

were negligible and not factored into equation 3.23. The amplifier chip had an R_{jc} of 25 °C/W[15], and the PGA a calculated spreading resistance R_{cs} of 40 °C/W[15][19][20]. Assuming an ambient air temperature T_a of 50 °C, from equation 3.23, Figure 3.17 shows

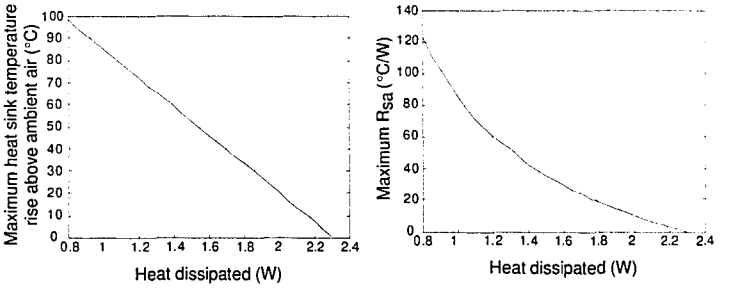


Figure 3.17 - Heat sink requirements for Phase II hybrid package power dissipation.

the heat sink requirements that would be needed to safely dissipate power generated at the

surface of each transimpedance amplifier and maintain a maximum junction temperature of 200°C. As a result of the close placement of several amplifiers together and a worst case consideration, the required power dissipation was taken to be 10 to 15 times more than that of an individual amplifier. To satisfy the above power dissipation needs, a Wakefield 658-60AB pin fin heat sink with an R_{sa} of less than 15 °C/W for dissipated powers of less than 2.5 W was used. This sink to ambient thermal resistance drops to less than 5 °C/W for a forced convection of more than 100 feet/minute (0.5 m/s)[21]. Thus, to improve power dissipation, a fan was used in testing the receiver assembly, and as described in Chapter 5, a package temperature of less than 45°C was maintained.

The post amplifier and decision making portion of the circuit was formed by the limiting function of the IVA-05208 1.5 GHz variable gain amplifier. With a nominal gain of 30 dBm, the single ended output voltage of the amplifier hard limits to 450 mV for an input power of -28 dBm, or a voltage of 9 mV, up to 1GHz of operation[22][23]. AC coupling using a 0.1 μF capacitor to the first stage was necessary to remove the transimpedance amplifier's fixed DC offset voltage. This blocking capacitor formed a high pass filter that introduced a low frequency cutoff of $1/(2\pi \cdot 0.1\ \mu F \cdot 50\Omega)$, or 32 kHz, which was well below the receiver's intended minimum data rate of several megabits per second. In addition, a 10 pF capacitor was inserted to cutoff wideband noise above an f_{3dB} of approximately 320 MHz into the post amplifier. The outputs of the post amplifier could then be fed into HP's G-link HDMP-1014 to form the receiver end of a gigabit rate fiber-optic link[24]. For the purposes of constructing a representative portion of an optical backplane, the post aplifier's positive single-ended output for each of the sixteen receiver channels was displayed onto an oscilloscope.

3.6.2 Construction

Similar to Phase I, the daughterboard and motherboard concept was again implemented with a VME size 3U daughterboard and VME size 6U motherboard, but with PCBs instead of speed-wire board. The PCBs were four layer double sided boards with impedance controlled microstrip lines. The two middle layers consisted of the ground and power planes, and the outer two layers the signal planes. The signal trace line widths were 8 mil (203 μm) wide, and the dielectric thickness between the ground and signal plane of 6

mil (152 μm) to obtain a characteristics impedance of 50 Ω[25]. The link between daughterboard and motherboard was perserved with minimal loss of bandwidth using a high speed flexible 40 channel 50 Ω impedance matched microstripline connector[26]. Optical signals received at the daughterboard were then similarly relayed electrically to the motherboard with the important difference that all of the electronics were contained on the daughterboard, the backplane layer. On the processing layer, the motherboard was left bare. The output signals were read onto from an SMA populated custom interface PCB board that connected to the motherboard using a high speed flexible 80 channel 50 Ω impedance matched microstripline connector[26]. Figure 3.9 shows a photo of the com-

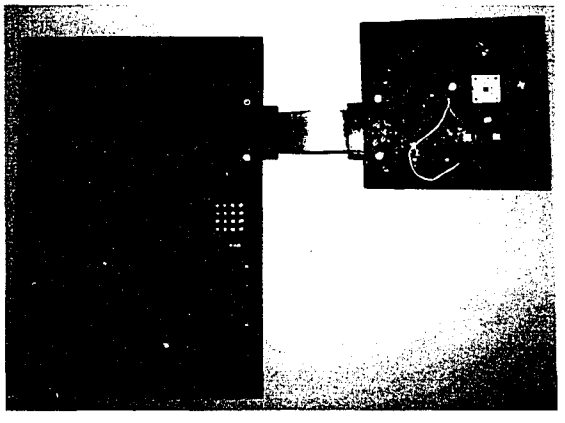
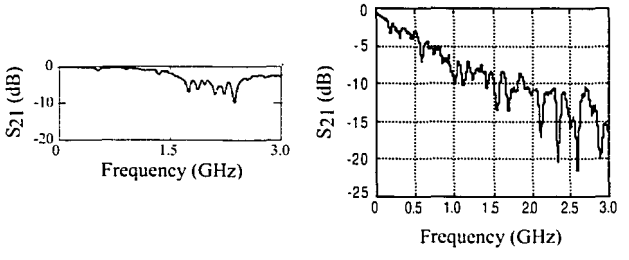


Figure 3.18 - Phase II daughterboard/motherboard PCB assembly with high speed connector.

plete Phase II daughterboard and motherboard reciever assembly with interconnecting high speed cable.

The 4x4 MSM photodetector array was hybridly packaged with fourteen transimpedance amplifiers. To accomodate the large number of devices in a single carrier, a 12x12 mm^2 wide cavity 68-pin grid array (PGA) was used. To ensure that the package and the PCBs supported the bandwidth required by the devices, frequency measurements

of a PGA package on a 50 Ω line board, and of a PGA and complete daughterboard/moth-



a) b)

Figure 3.19 - S_{21} parameter of a) PGA on a high speed board, and b) Phase II daughterboard/motherboard assembly[25]

erboard assembly was done with a network analyzer and shown in Figure 3.19 The results are adjusted to reflect that the measurements were done for a path to the package and back out, and show a -3 dB point of approximately 1.6 GHz for the PGA package and 300 MHz for the entire board assembly. To preserve bandwidth, care was taken in the packaging and positioning of components. Wirebonds have been estimated to contribute a 1 nH/mm inductance per length[27]. To minimize long wirebonds and unwanted inductive and capacitive parasitics, Figure 3.20 shows the 14 transimpedance amplifier chips mounted as close as possible adjacent to the central 4x4 MSM photodetector array. A

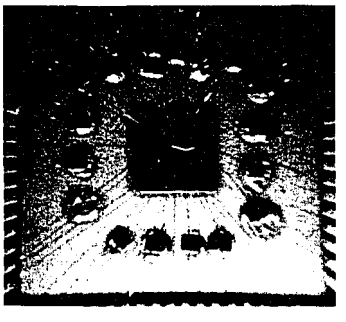


Figure 3.20 - Hybrid package of 4x4 MSM photodetector array and transimpedance amplifiers.

thermosonic K&S wedge wirebonder was used to interconnect the bond pads of the MSM photodetector array, transimpedance amplifiers, and carrier cavity fingers for each of the 14 receiver channels outlined in the schematic of Figure 3.13. Due to the small 50x50 μm^2 transimpedance amplifier bond pads, 0.7 mil (18μm) gold wire was used. To avoid peaking in the gain response and ensuing oscillations from a drop in frequency of the critical pole, it was essential that each of the transimpedance amplifiers be well grounded with the shortest possible inductance path. For the transimpedance amplifiers, an extremely low common lead inductance of less than 0.5 nH was needed[28]. To address this, approximately one third of the PGA pins were bonded to the bottom of the PGA cavity and connected directly to the ground plane of the PCB to create a ground plane underneath all of the devices. Ground connections to each of the transimpedance amplifiers were subsequently wire bonded from the bottom of the PGA cavity. The outputs of the transimpedance amplifier chips were then wire bonded to designated PGA output pins. Two prepackaged ITA-06318 transimpedance amplifiers were used. In this case, the package cases had a much lower inductance path than the ground leads, and the case bottom was used as a primary ground connection by sodering it to three ground vias directly underneath it. As a note, thick boards were not used since the inductance through a via hole increases by the square of the board thickness. Hence, while a via through a 31 mil (800 μm) board adds about 0.12 nH, a via through a 62 mil (1600 μm) board adds nearly 0.5 nH[28][29]. To minimize switching noise, decoupling capacitors were placed near the PGA and each of the post amplifiers, and where space permitted, regularly positioned throughout the board to provide the best possible signal ground. With the exception of the PGA, all electronic components were surface mounted to decrease conductor line lengths and achieve a greater component density on the relatively small 4.6" (11.68 cm) by 4.1" (10.4 cm) four-layer double-sided daughterboard. Figure 3.21 shows a photo of the top view of the 16 channel receiver daughterboard. The increase in component density permitted all of the electronics to be confined to the daughterboard, and hence the optical interconnect layer.

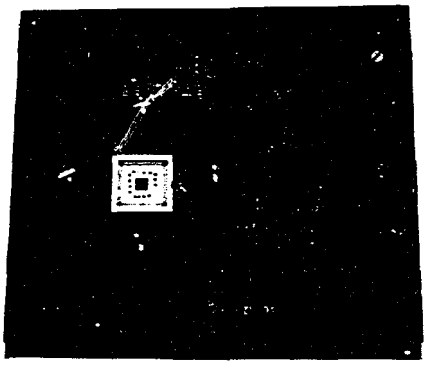


Figure 3.21 Phase II integrated receiver daughterboard with hybrid package and optomechanics.

3.7 Conclusion

The receiver system requirements were analyzed from a dynamic range consideration. It was seen from an analysis of the coupled optical power onto the receiver's photodetector windows that the optical output from the system resulted in limited optical dynamic range, and could be quantified in terms of optomechanical misalignment tolerances and transmitter optical output power fluctuations. These key system characteristics were then seen to set the minimum sensitivity and dynamic range requirements for the optical receiver. Based on receiver Gaussian noise and equal mark and space transmission probability assumptions, the sensitivity and dynamic range of the receiver was estimated in terms of key photodetector and font end amlifier performance figures. From both of these expressions, it was found that the suitability of a particular receiver for a free-space optical system could then be measured.

The design and construction of the receiver assembly in a progression of two phases were discussed. It was found that a novel 4x4 MSM photodetector array combined with mature fiber optic electronic receiver technology allowed high aggregate bandwidths with wide dynamic range using a stable and simple optomechanical support assembly.

The discussion on hybrid packaging and power dissipation techniques used in the construction of the Phase II receiver point to low power integrated photodetector arrays, or smart pixels, as a means of further increasing optical channel density of future systems.

To conclude this chapter, important characteristics such as transmitter and receiver array uniformity were not known and not specifically accounted for in the design. As will be seen in the following chapter in testing the Phase II receiver assembly, these factors can be substantial and serve to degrade signal integrity.

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Chapter 4

Performance of the MSM receiver assembly

4.1 Introduction

This chapter begins with a description of a high speed optical setup used to characterize the 4x4 MSM photodetector array and test the final receiver assembly described in the previous chapter. The construction and properties of the setup are reviewed. With support of an additional test rig, characteristics of the photodetector array were subsequently investigated. With an understanding of the fundamental characteristics of the photodetector array, the complete receiver assembly was tested and characterized within the controlled test rig, and finally, within the system itself and a comparison made.

4.2 Experimental setup

Before any such testing can begin, a complete characterization of the input is required. For the device and receiver system under consideration, important factors are those affecting the conversion of optical to electrical signals at the photodetector. An SEO tunable Ti:sapphire laser arranged in a ring configuration pumped by a coherent argon laser was used as the input light source. With a nominal linewidth of 50 MHz and a tunable wavelength range of 780 nm to 900 nm, the wavelength was measured using an Anritsu MF9630A wavelength meter, and subsequently tuned to 850 nm. The light power from the argon pumped Ti:sapphire laser was measured to vary by as much as 1.7% from mean value during an hour of operation after the laser had been on for one hour. This is due to slight thermal shifts within the argon and Ti:sapphire lasers, and arises from active thermal stabilization provided by the water cooling system. Figure 4.1 illustrates a sample of the power variations against duration of operation. Note that from the start, an hour of warm up was necessary to stabilize power output. These variations in light power can

introduce sources of error and must be taken into consideration in future measurements.

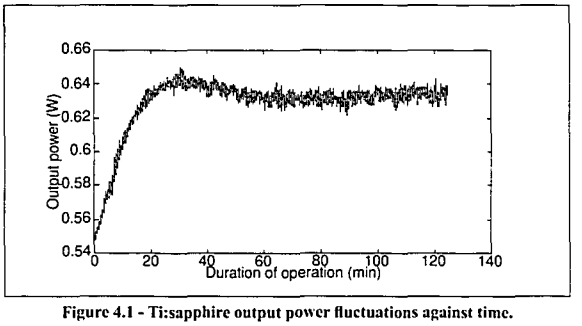


Figure 4.1 - Ti:sapphire output power fluctuations against time.

This light was coupled into an optical fiber, and refocused onto the device plane of a 4f system with lenses of focal lengths 25 mm and 50 mm. This is illustrated in Figure 4.2. The choice of lenses was determined by a required spot size of approximately 20 μm on the device plane, optomechanics and availability of components. The optomechanics used were Spindler & Hoyer components, and facilitated in the alignment of the test rig. Due to the compactness of the system, a custom Spindler & Hoyer compatible beamsplitter holder was designed and fabricated to permit the convenient addition of a second beamsplitter and input beam. The holder, or platform, was designed for 10 mm, 25 mm, or a combination of the two beamsplitters, and could be base or side mounted. A ridge on the top face allowed for quick and easy alignment of the beamsplitters with respect to each other, and one degree of freedom of movement. The technical drawing is shown in Appendix A. With the exception of the top ridge, the dimensional tolerances of the component is not critical and was not tighter than 0.1 mm. However, the ridge was constrained to within 0.1 mm, and a high degree of flatness was required for the top face. The separate beamsplitter platform resulted in a modular test rig in which components within each module were separately aligned, and then each module aligned with respect to each other using irises as alignment apertures. This modularization optomechanically decouples sets of components from each other while preserving a convenient method of aligning one set of components or module to another. Where much time can be spent aligning or

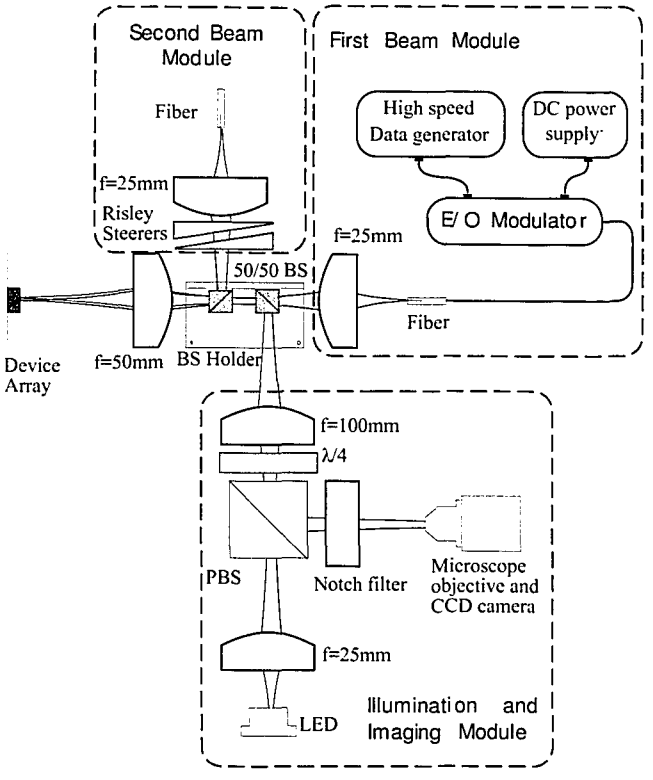


Figure 4.2 - Optical test rig to test device array and receiver system.

re-aligning components, this divide and conquer approach was found to be effective.

Spot positioning of the first beam on the device plane was done by moving the receiver assembly relative to the optical system. The second beam module incorporated Risley steerers to move the second beam relative to the first. To view the device plane, an LED based illumination and 4f imaging system was incorporated into the setup. A 100 mm lens was chosen to relay and magnify by two the device plane to the objective and CCD. Compared to a unity gain magnification relay, this halves the microscope objective magnifica-

tion needed for an equivalent sized CCD image and relaxed the alignment positioning of the CCD camera and microscope objective assembly.

The 4f relay from the input to the device plane provided a calculated spot radius, ω_o, of 5.1 μm, an f number of approximately 3, and a Raleigh range of 61 μm. To characterize the spot size, the output beam profile of the test setup was measured using Merchantek's PC-Beamscope Profiler with a Series 3 Probe syle head. Table 4.1 shows the measured spot diameter (e^{-2} power) $2\omega_o$, percent gaussian fit, and standard deviations for 34 samples at various optical powers.

	X			Y		
Power (mW)	Gaussian fit (%)	Diameter (μm)	Standard deviation	Gaussian fit (%)	Diameter (μm)	Standard deviation
1	96.2	17.85	0.23	96.6	17.88	0.06
2	96.4	18.06	0.14	96.3	18.03	0.07
3	96.4	18.57	0.21	96.4	18.54	0.05
4	96.4	18.79	0.24	96.2	18.84	0.16
5	96.0	18.92	0.31	96.1	18.93	0.33

Table 4.1- Test rig spot characteristics

As can be seen, the spot sizes are measured to be much larger than that calculated and deviate from a perfect Gaussian profile. This largely results from the effects of optical aberrations, and misalignments between components and modules. As was considered in the misalignment considerations of the previous chapter, the relatively large increase in spot radius from the calculated value still results in 99.9999% power coupling within the 50x50 μm^2 MSM for an ω_o of 10 μm.

The optical bit stream was provided by incorporating a modulator in the first beam module, and using an HP80000 data generator having a 200 ps rise time as input. The modulator used was a UTP Mach-Zehnder amplitude modulator with a nominal 3-dB electrical bandwidth of 12 GHz. An HP 6235A power supply was used to provide the correct DC bias for continuous wave and modulated operation. For maximum coupling, a polarizer was positioned in front of the fiber coupler to align the linear polarized light to the modulator. A maximum -30 dBm contrast between off and on states as well as an

overall CW throughput of approximately 20% from fiber coupler to the output of the modulator was measured. An Antel ARX-SA avalanche photodiode with less than a 210 ps risetime was used as a detector to obtain the eye diagrams shown in Figure 4.3 These eye diagrams can be used as a baseline for comparing different receiver eye diagrams to be obtained from this test-rig.

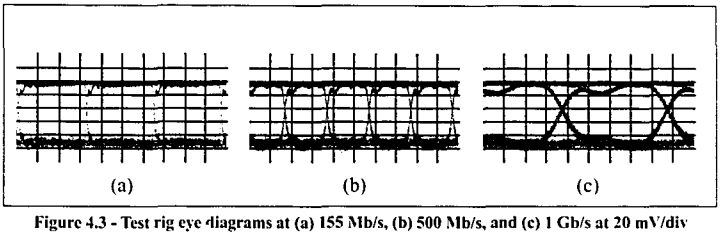


Figure 4.3 - Test rig eye diagrams at (a) 155 Mb/s, (b) 500 Mb/s, and (c) 1 Gb/s at 20 mV/div

4.3 MSM array characteristics

In a multiple receiver system, particularly in an integrated or hybrid receiver array, good uniformity of the photodetectors across the array is often desirable. Unlike a single optical link in which the receiver electronics can be designed and tuned to the particular characteristics of a single photodetector, a receiver array system requires that it be tuned to the entire photodetector array. To achieve predictable and similar optical channel performace throughout the link, each receiver must be designed to the particular characteristics of its photodetector, or alternatively, a common receiver design can be used, with the proviso that good photodetector array uniformity is established. Even in small 2x2 arrays the former method is time consuming, cumbersome, and scales exponentially with the array dimension. Further, determining the particular characteristics of each photodetector prior to integration can compound the difficulties in such an approach. The latter method of fabricating a uniform photodetector array is conceptually more readily achievable and practical, especially with recent advances in photolithographic and device growth technology. As described in Chapter 3, this method was used. The performance of the receiver

board discussed in later sections is better understood after determining and quantifying certain characteristics of the MSM photodetector array.

4.3.1Dark currents

The dark current is referred to as the portion of the photocurrent not directly related to the incident signal, and includes current generated from stray light. This current introduces noise at the photodetector level, which along with the signal current is subsequently amplified in the later receiver stages. Since this unwanted current distorts the signal at the source, the level of dark current is critical in achieving a good signal to noise ratio. The dark current of the MSM array was measured by covering the PGA package with a black ceramic lid and sealing all edges with black electrical tape. This was done to control unknown variations in the background light. To simulate the transimpedance amplifier loads, each of the MSMs in the 4x4 array were then connected to ground terminated 50±2Ω resistors. The four bias rails described in Chapter 4 were biased to 5.0 V and the current through each load resistor was then separately monitored using an HP 4145b parameter analyzer. Table 4.2 summarizes the dark currents that were measured for each

		MSM Column			
		1	2	3	4
MSM Row	1	1.68 nA	1.44 nA	4.21 nA	1.74 nA
	2	1.60 nA	0.47 nA	3.09 nA	45.9 nA
	3	0.896 nA	3.87 nA	11.28 nA	41.7 nA
	4	6.89 nA	11.5 nA	11.77 nA	33.9 nA

Table 4.2 - MSM dark currents at different locations.

MSM in the array. Although the dark current varied widely over the array and even differed by as much as two orders of magnitude (MSM 2,2 compared to MSM 2,4), the absolute maximum dark current is of more interest as it sets the minimum detectable light signal. For instance, realizing two orders of magnitude signal to dark current on MSM 2,4 would require approximately 10 μW of incident light power when assuming a responsivity

of 0.5 A/W. From this example, the maximum dark current and responsivity of the photodetector are clearly key factors in determining the optical power requirements of the transmitter.

4.3.2Responsivity dependence on bias voltage

A figure of merit in the discussion of photodetectors is the responsivity, which is the ratio of the photocurrent to the incident optical power[1]:

$$R = \frac{I_{ph}}{P_{opt}} \tag{4.1}$$

where I_{ph} is the photogenerated current for an incident optical power P_{opt}. The responsivity of the MSM array was measured at 850 nm for bias voltages ranging from 0 to 5.5V. This was done to verify the responsivity uniformity of the MSMs throughout the array for small variations in the applied bias voltages. The MSM package described in the previous section was mounted in the test rig and aligned such that the incident beam was focused to the smallest perceivable spot size within the MSM window viewed from the CCD. The incident optical power was measured using a Newport 1835c power meter with an 818-ST/CM detector head before each voltage sweep. All four bias rails were voltage swept with and without the incident beam, and the resulting dark and total current monitored using an HP 4145B parameter analyzer. The responsivities were calculated using Equation 4.1 after subtracting the dark from the total current to obtain the current only arising from photogenerated electron hole pairs. The data is plotted in Figure 4.4. The peaks and dips across the surface when scanning along the row axis and voltage axis for each column indicate the variations in the responsivity with respect to each variable. From the figure, with the exception of MSM 2,2 and MSM 2,4 having slightly lower responsivities compared to their neighbors, the array is seen to be very uniform. This is particularly true for a voltage bias between 4 and 5.5 V. The responsivity is also highest within this range and a convenient bias voltage of 5.0 V was chosen for the final system.

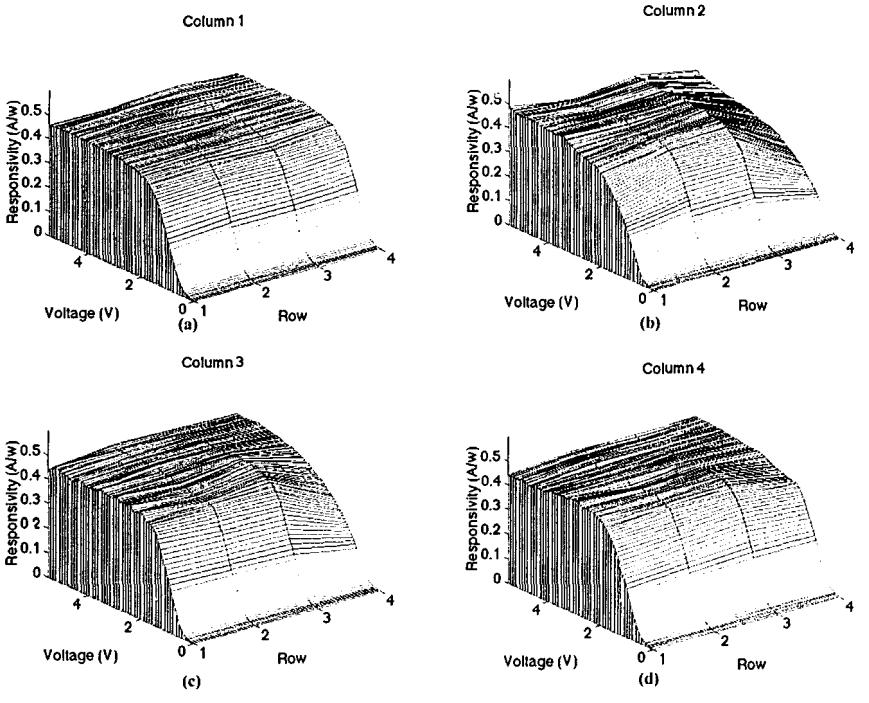


Figure 4.4 - Responsivity against voltageof the MSM array at 850nm.

4.3.3Responsivity dependence on wavelength

The MSM array's uniformity and tolerance to variances in the incident optical wavelength was measured as the respective change in responsivity. This characteristic can be very important in systems where the optical source is far from ideal and have wide linewidths, experience large wavelength drift during the course of operation, or possess poor wavelength uniformity across the transmitter array. Due to the relatively narrow tunable wavelength range of the light source in the previous test rig, an additional setup used to measure the responsivity's dependence on wavelength and is diagrammed in Figure 4.5. The MSM package was mounted on an XYZ translation stage and positioned in the center of the wide, uniform monochromatic beam of the spectrophotometer. An advantage of using this light source is the resulting relaxed tolerances on positioning the device. The entire MSM array was initially biased to 5V, and the current of each MSM recorded using an HP 4145A parameter analyzer for wavelengths ranging from 600 nm to 1050 nm. All measurements were performed in darkness. For each wavelength, the incident optical power was determined by measuring the light intensity using a calibrated silicon photodetector. The resulting responsivity for each MSM at 850 was calculated to be much higher than that measured perviously using the Ti:sapphire laser test rig and is due to leakage currents from neighboring illuminated detectors. A more detailed discussion of leakage currents is discussed in the following section. To isolate the MSM detector of interest from the rest of the array, its signal line was biased to 5V, and all other lines were terminated to

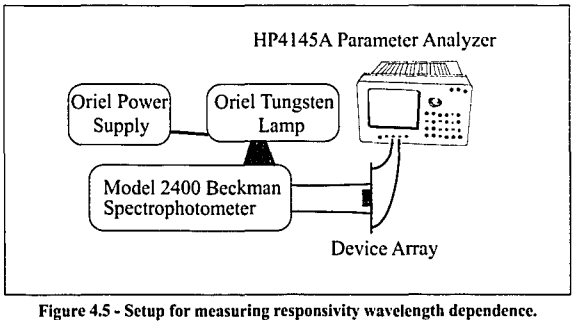


Figure 4.5 - Setup for measuring responsivity wavelength dependence.

ground. This was possible since the individual MSM photodetectors have no preferred direction of bias[2]. This prevents potential from building up across the array except at the contacts of the detector of interest, and ensures that the measured photocurrent is only the result of swept electron hole pairs between these contacts. The measurements were then repeated with the current monitored from the supply side. As before, for each iteration, dark currents were measured and subtracted from the total current to arrive at the photogenerated current in determining the MSM's responsivity. At 850 nm, the responsivities closely matched those obtained previously, and its wavelength dependence is plotted in Figure 4.6. For the system's operating wavelength of interest, from 840 nm to 860 nm, Table 4.3 illustrates small deviations in responsivity across the array, and hence a good tolerance to transmitter wavelength variations. The responsivity is seen to drop steeply after approximately 870 nm. This is in good agreement with the theoretical long-wavelength, λ_c, cutoff of 873 nm for an intrinsic photoconductor, assuming a bandgap, E_g, of 1.42 eV for GaAs. For incident radiation with wavelengths less than λ_c, and hence with energies greater than E_g, the detector generates photocurrent. This is reflected in the responsivity values for wavelengths of 800 nm down through the visible spectrum to 600 nm. Despite taking measurements in darkness, variations in the background radiation, particularly in the visible spectrum from 384 to 770 nm contribute sources of error in the measurement and may be a factor in the non-uniform responsivity over the visible wavelength region. In any case, the consistently high responsivity values over wavelengths such as the visible spectrum points to shielding the photodetector array from background radiation to improve optical signal detection.

4.3.4Leakage currents

Leakage currents occur between MSMs because of the finite resistance between them. This type of crosstalk is particularly noticeable on adjacent devices, and may limit

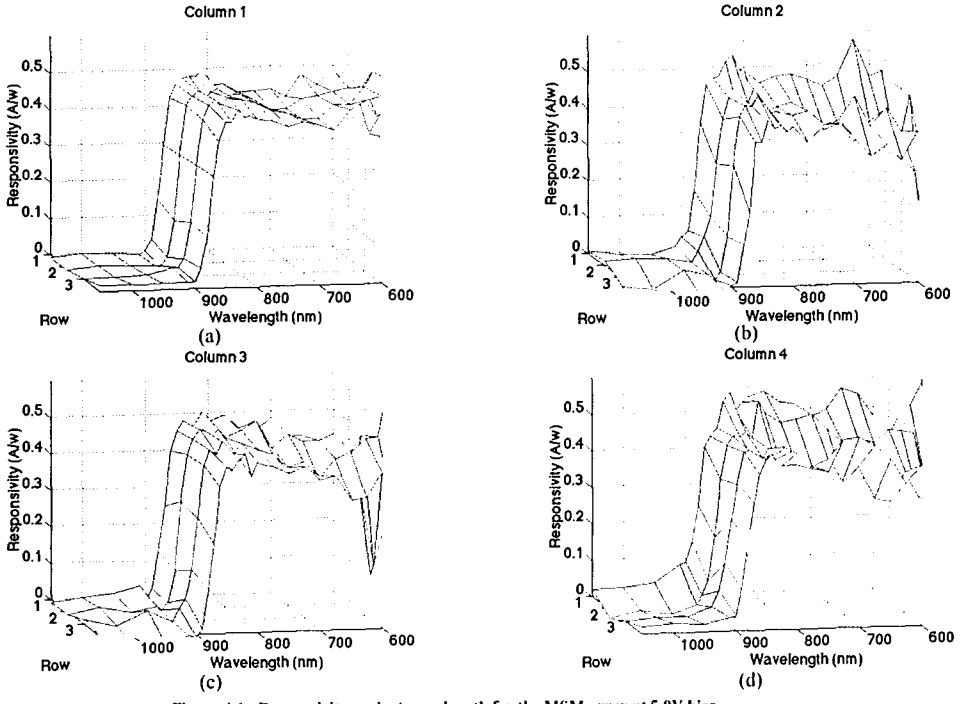


Figure 4.6 - Responsivity against wavelength for the MSM array at 5.0V bias.

Wavlength (nm)	Responsivity (A/W)			Standard Deviation
	Mean	Minimum	Maximum	
810	0.4779	0.4265	0.5573	0.0353
820	0.4746	0.4349	0.536	0.0243
830	0.4735	0.387	0.5464	0.0355
840	0.4692	0.4156	0.5211	0.0228
850	0.4572	0.3989	0.4726	0.0169
860	0.4226	0.3935	0.4533	0.0189
870	0.3035	0.2053	0.3993	0.0498

Table 4.3 - Responsivity dependence on wavelength statistics.

the operation of all channels simultaneously. To measure the extent of this effect, the experimental setup of Figure 4.2 was used to shine a 500 μW 850 nm beam on MSM 4,4. As before with this setup, to simulate the conditions of the device in the system, 5V was applied to all bias rails and all MSM signal traces were connected to ground terminated 50±2Ω resistors. As a representative example, the package was aligned to achieve the smallest spot size on MSM 4,4. In darkness and with constant monitoring of the optical power, the currents of MSM 4,4 and each of the MSMs of the 4x4 array were iteratively measured with and without the incident beam. Dark currents were subtracted, and the resulting leakage currents were then normalized to the mean current of 218 μA of MSM 4,4 and plotted in Figure 4.7 . The result shows a maximum coupling with neighboring

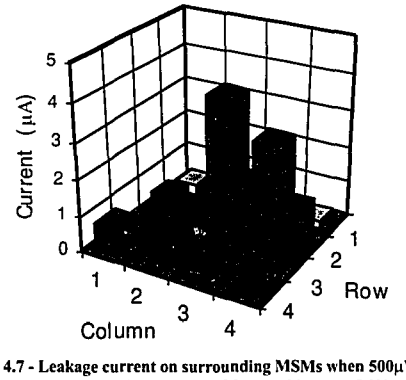


Figure 4.7 - Leakage current on surrounding MSMs when 500μW is shone on MSM 4,4 with the MSM array biased at 5.0V.

MSM 3,3 (1.7%) followed by MSM 3,4 (1.5%), and then MSM 4,3 (0.8%). The relative amount of coupling between these MSMs is not surprising when the closeness of the devices and respective signal traces are considered in the layout in Appendix A. The lower coupling of MSM 4,3 is likely due to the shielding effects from MSM 4,4 of MSM 3,3's parallel signal trace line, which is also the reason for MSM 3,3's high coupling percentage. The average coupling drops with successive neighbor separation, resulting in 0.2% one device away, and 0.18% two devices away. While the coupling is relatively low between individual devices, significant cumulative effects will result from the parallel operation of the entire array simultaneously.

The 50 Ω load resistors employed in the previous measurements varied by as much as 2 Ω. The effect of variances in the load resistance of an active receiving photodetector on neighboring passive photodetector leakage currents was investigated. To measure this, the previous measurement was repeated with the end of the 50 Ω line of MSM 4,4 voltage swept from 0 to 1 V using the HP 4145b parameter analyzer. The equivalent load resistance seen by MSM 4,4 is then determined to be $50 + \left(V_{sweep} / I_{sweep} \right) \Omega$. The results are plotted in Figure 4.8. Linear interpolations of the data summarized in Table 4.4 show that not only are the leakage currents higher for neighboring MSMs as indicated by the y intercepts, but are also more sensitive to changes in the load resistance as indicated by the slope. From these results, a key parameter is to keep the load impedance small such that any load variances across the array will have negligible effects on increasing the leakage currents. The hybrid integration of low impedance HP ITA06300 transimpedance chip amplifiers in the receiver assembly is thus ideal for meeting this requirement.

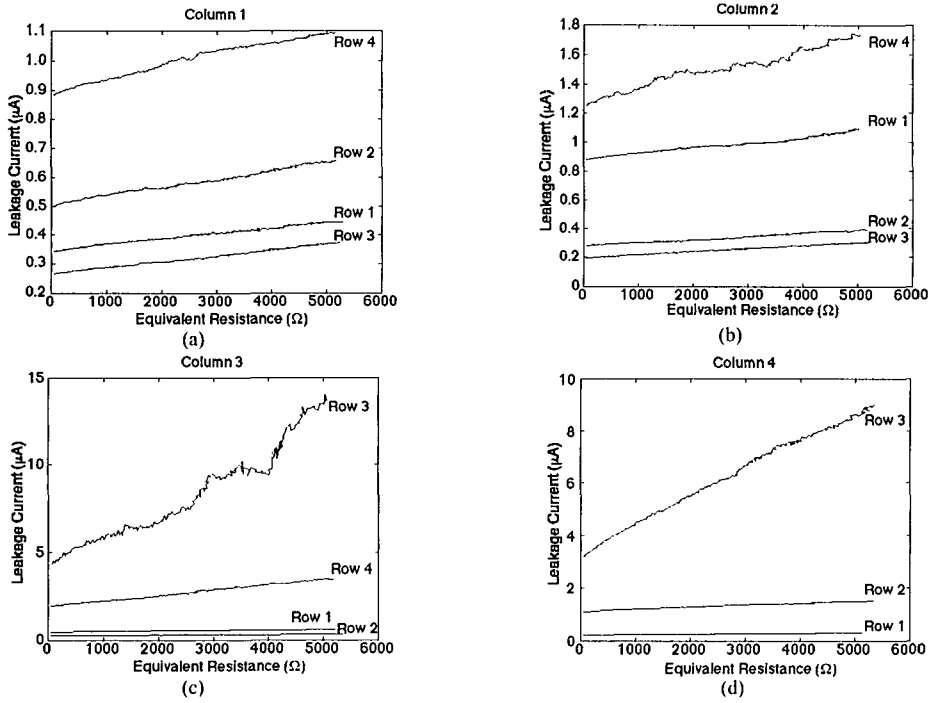


Figure 4.8 - Leakage currents on neighboring MSMs for a 500 μW beam and different resistive loads on MSM 4,4.

MSM Row \ MSM Column	1	2	3	4
1	$0.020R_{eq}$ + 0.35 μA	$0.038R_{eq}$ + 0.88 μA	$0.034R_{eq}$ + 0.49 μA	$0.018R_{eq}$ + 0.23 μA
2	$0.029R_{eq}$ + 0.51 μA	$0.023R_{eq}$ + 0.28 μA	$0.020R_{eq}$ + 0.27 μA	$0.073R_{eq}$ + 1.16 μA
3	$0.021R_{eq}$ + 0.27 μA	$0.022R_{eq}$ + 0.20 μA	$1.74R_{eq}$ + 3.86 μA	$1.07R_{eq}$ + 3.36 μA
4	$0.041R_{eq}$ + 0.90 μA	$0.087R_{eq}$ + 1.29 μA	$0.317R_{eq}$ + 1.92 μA	

Table 4.4 - Linear interpolation of the leakage currents on neighboring MSMs for a 500 μW beam and different resistive loads, R_{eq}(kΩ), on MSM 4,4.

4.4 Receiver board

The optical test rig described in Figure 4.2 was used to test and measure the bandwidth of the final receiver board. The tested assembly included the daughter/mother/interface assembly with interconnecting high speed AMP connectors. The MSM hybrid package was cooled with an ETRI model 125DH fan placed behind the daughterboard. By monitoring the thermistor, the temperature was maintained at approximately 42°C. The HP 80000 data generator was configured for a NRZ 2^{23}-1 pseudo-random bit stream, and the receiver output eye patterns displayed on an HP 54120B digitizing oscilloscope using an HP 54124A DC to 50 GHz sampling unit. From Chapter 3, it was calculated that approximately 500 μW of incident light was required for a high bit, and that lower powers would result in reduced signal swing. This is confirmed in the eye patterns of MSM 1,1 in Figure 4.9 displayed with a persistence of 10 seconds. With 500 μW set as the required incident light power for a high bit, the eye patterns at data rates of 155 Mb/s, 250 Mb/s and 500 Mb/s for the single operation of each of the receivers of the 4x4 array are shown in Figure 4.10 a) to c) with a display persistence of 10 seconds. The labelling format corresponds to which row and column MSM of the array is receiving. From the figure, the 10% to 90% rise times of a 250 mV swing can be seen to vary from approximately 1.5 ns (f_{3dB}=233 MHz) of MSM 2,4 to almost 2 ns (f_{3dB}=174 MHz) of MSM 2,1 across the array. Although the amount of noise can be seen to vary somewhat from receiver to receiver, each is very tolerant to timing error in that the jitter in the received zero or

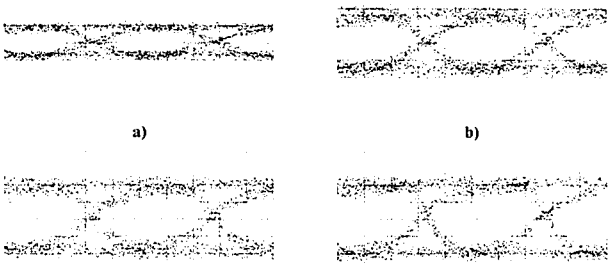


Figure 4.9 - MSM 1,1 eye patterns generated from 2^{23}-1 pseudo-random NRZ bit stream at 500 Mb/s for incident optical powers of a) 100 μW, b) 150 μW, c) 250 μW, and d) 500 μW.

threshold crossings is minimal, leading to open eyes and a low bit error rate ($< 10^{-9}$)[4][5]. Keeping in mind the wide f_{3dB} bandwidths of the individual devices and components in the development of the receiver assembly discussed in Chapter 3, the discrepancies in the comparably low bandwidth and noise levels can be attributed mostly to the result of cumulative variations in the electrical isolation and layout of the respective components and devices for each receiver. These differences occur at the first two levels of packaging: the chip and the chip carrier. While every effort was made to minimize wire bond lengths, the hand placement of a relatively large density of chips within the cavity still resulted in wirebonds of 1mm and introduces additional inductance. Further, improved performance could be achieved by selecting higher bandwidth chip carriers such as ball grid arrays or quad flat packs, or through a chip on board approach. By removing the carrier layer between the chips and the board, direct mounting onto the printed circuit board would have proved ideal in significantly reducing signal line capacitive and chip to ground plane inductive loading. Also, the ability for closer placement of decoupling capacitors would reduce switching noise at the source supply of the transimpedance amplifiers. These combined improvements could achieve larger bandwidths and swing[3]. However, the height requirements of the chip carrier was essential in this system, and was constrained to the use of PGAs. The second level of packaging addresses the placement and interconnection

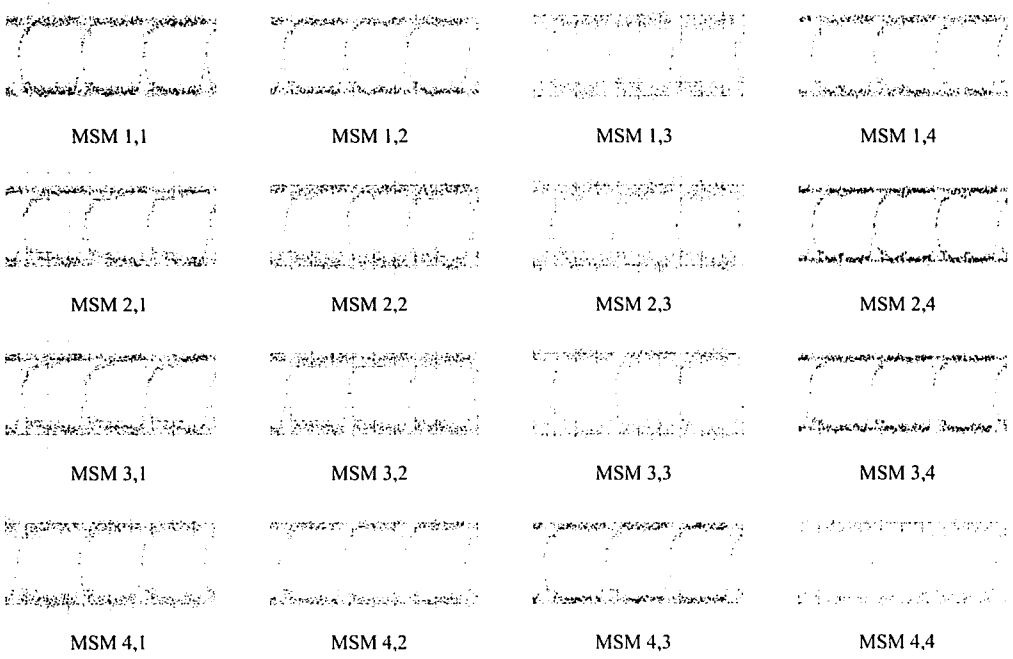


Figure 4.10 a) - Eye patterns generated from a 2^{23}-1 pseudo-random NRZ bit stream at 155Mb/s.

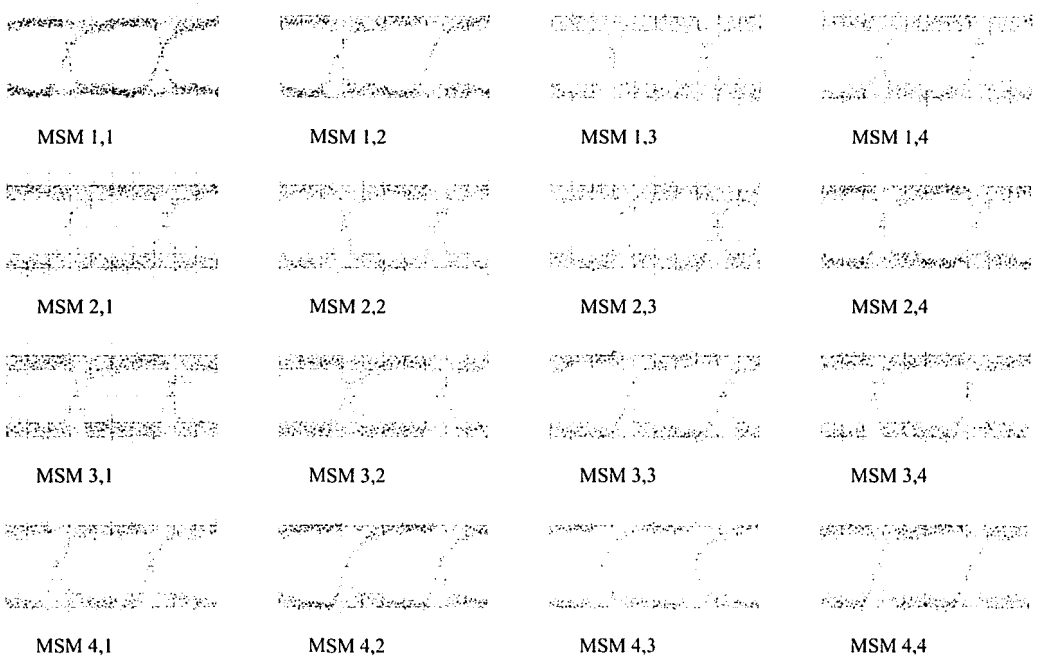


Figure 4.10 b) - Eye patterns generated from a 2^{23}-1 pseudo-random NRZ bit stream at 250Mb/s.

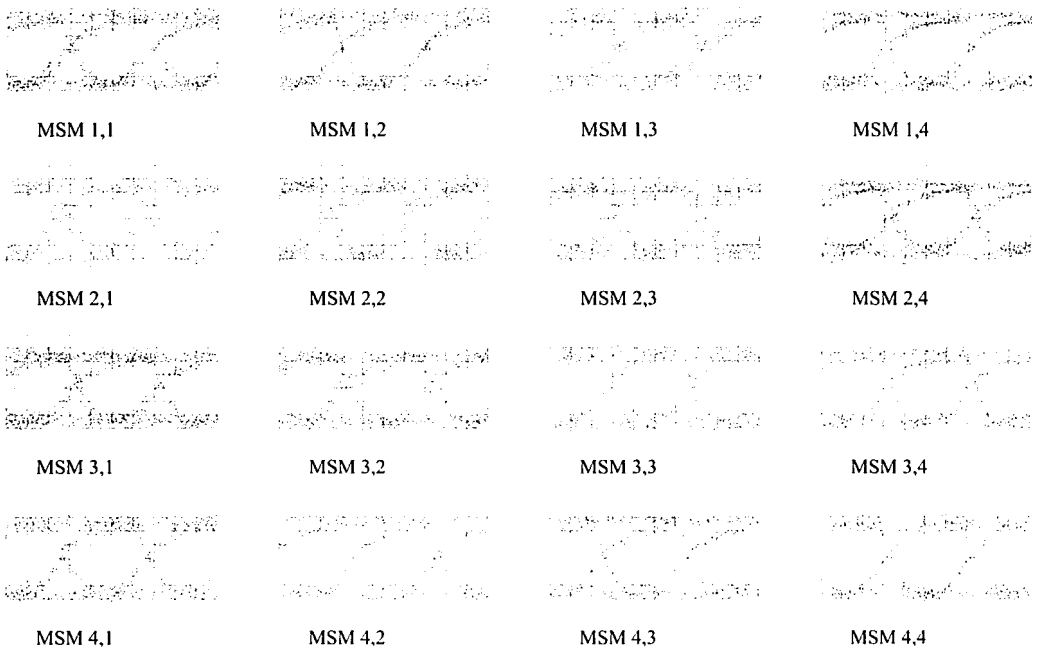


Figure 4.10 c) - Eye patterns generated from a 2^{23}-1 pseudo-random NRZ bit stream at 500Mb/s.

of the chip carriers on the printed circuit board. It was recognized that trace lines longer than half the rise time and that nearby traces can significantly affect signal integrity. In some instances, trace lines longer than 1.5 inches on the daughterboard were necessary to route to the connector. This translates to the trace lines in FR4 material being able to support at most a 0.5 ns rise time (f_{3dB}=700 MHz) and still be considered as a lumped load[6]. Also, in order to simplify the routing of the board for the time of construction of the system, a large number of vias were used, but unfortunately each can add additional parasitic inductance to the lines of approximately 0.5 nH for a 1/16" board. Signal integrity is lost by reflection, switching and coupled noise and is most affected by the length, parallelism and density of the trace lines on the daughter board. Improvements in signal integrity could thus be achieved by increasing the size of the daughterboard and decreasing the density of trace lines. Finally, added parasitic capacitances and inductances from the straight through traces of the motherboard, cables, and connectors increase the rise time and potential for signal distortion.

4.5 System results

The complete receiver assembly was inserted into the system and tested by generating an eye pattern for each VCSEL transmitter to MSM receiver link. The HP 80000 data generator drove each VCSEL transmitter separately with a 2^{23}-1 pseudo-random bit stream at a bit rate of 155 Mb/s. The single operation of each link was displayed on the HP 54120B digitizing scope with a display persistence of 9 seconds and the eye patterns illustrated in Figure 4.11. A comparison of these eye diagrams with that of Figure 4.10 a) indicate that the VCSELs introduce additional noise and timing jitter on the signal. The parallel operation of the channels was then similarly tested at a bit rate of 155 Mb/s, but with 8 different distinctive 16 bit patterns that were permutations of the following bit sequence: 111, 000, 11, 00, 1, 1, 1, 0, 0, 0. This was done to ensure that each link was transmitting and receiving the correct sequence, and not from adjacent links. It was found that the simultaneous operation of more than 11 channels was not possible due to signal distortion of introducing additional channels. The resulting patterns are displayed in Fig-

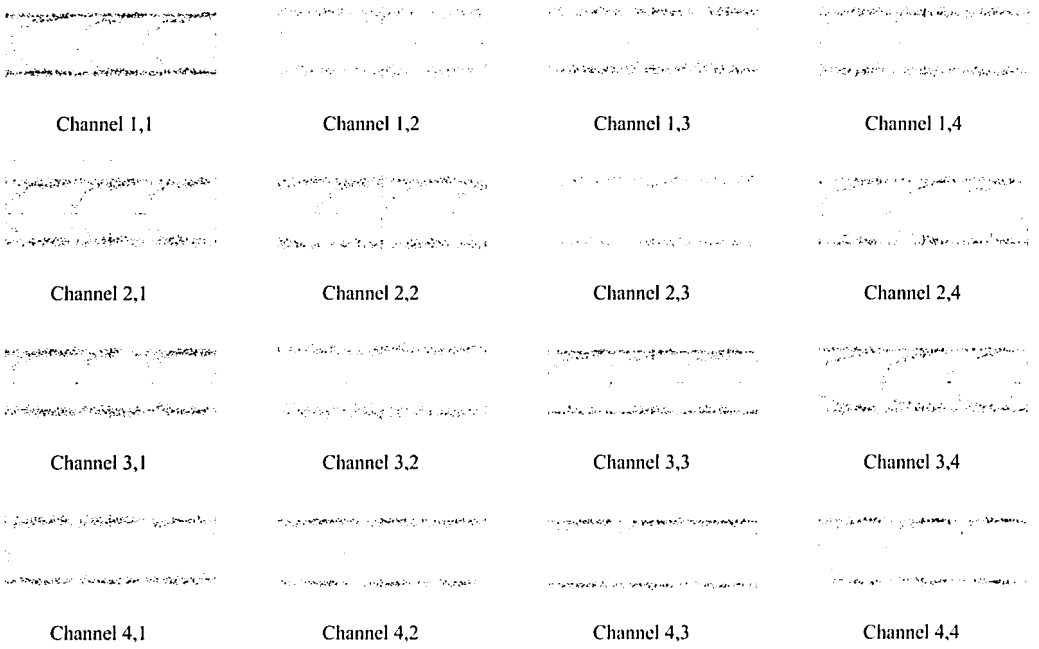
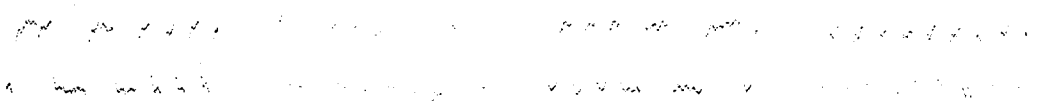
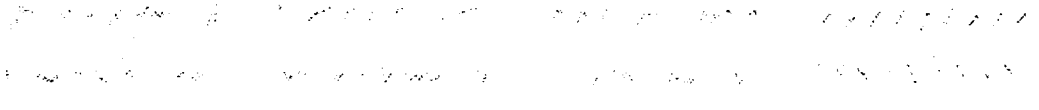


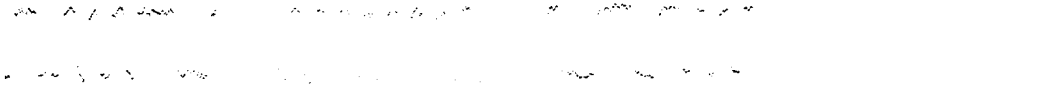
Figure 4.11 - System eye patterns generated from a 2^{23}-1 pseudo-random NRZ bit stream at 155Mb/s.



Channel 1,1 Channel 1,3 Channel 1,4 Channel 2,1



Channel 2,4 Channel 3,1 Channel 3,2 Channel 3,4



Channel 4,2 Channel 4,3 Channel 4,4

Figure 4.12 - System parallel operation of 11 channels showing 16 bit patterns at 155Mb/s.

ure 4.12. From the previous section, it was seen that the receiver channels in the middle of the array had more noise, and were also more susceptible to leakage currents from surrounding channels as discussed in Section 4.3.4. Similar effects were also seen from the transmitter assembly[7]. These cumulative effects thus resulted in the parallel operation of only the periphery channels where the isolation was found to be sufficient. Future systems must thus address a means of improving this characteristic if the full potentional of two dimensional high speed high performance device arrays are to be used in achieving high aggregate bandwidth.

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Chapter 5

Conclusions and future directions

5.1 Review

This thesis has presented a proof of concept of integrating a two-dimensional array of MSM photodetectors within the receiver assembly of a representative section of a free-space photonic backplane. First, the need for complementing current electronic backplane technology with optics and optoelectronics was discussed. Then the motivation for using MSM over conventional p-i-n photodetectors was investigated. With this planar photodetector technology, common methods of integration were reviewed and where possible compared. Common preamplifier designs were considered with an emphasis on integration to create smart pixels arrays. Then the design, fabrication, testing and characterization of the receiver assembly were described.

In the design of the receiver assembly, the system's optomechanical stability and optical transmitters' output power fluctuations were seen to place constraints on the receiver's sensitivity and dynamic range. In particular, to achieve low bit error rates of less than 10^{-15} that would be needed for commercial optical backplanes to be realized, optomechanical tolerances in the order of a several microns would be needed. In the system, over a three week period, only a two micron drift was measured. To avoid the long design and fabrication cycle of custom ICs, components off the shelf were chosen to fulfill the design constraints. The construction of the receiver assembly was then described as a progression of two phases.

A test rig was designed and built to characterize the MSM photodetector array and receiver assembly. Characteristics of the MSM photodetector array were investigated. The completed receiver assembly was then tested and as a measure of performance eye diagrams captured at different bit rates. Subsequently, the assembly was integrated into a standard VME 6U chassis, and the first representative free-space VCSEL/MSM backplane using an existing electronic backplane frame was demonstrated. All sixteen channels were

individually operated to 155 Mb/s and 250 Mb/s with clean and open eye diagrams. Eleven channels were simultaneously operated at 155 Mb/s with permutations of a sixteen bit pattern. These results indicate that practical optical backplane systems may be achievable in the near future.

5.2 Future work

The results and discussions of the previous chapters helped identify certain areas that need to be addressed in order for free-space optical backplanes to be fully functional in comparison to current electronic backplanes. Throughout the development cycles in the years to come, not only must these areas provide cost effective short term solutions for the near future, but also strong growth and development potential for continued improvements and enhancements. The following sections discuss important areas for future study.

5.2.1 Smart pixel intelligence

While the VCSEL/MSM demonstrator showed unidirectional data flow, bidirectionality between boards is essential. Thus, the smart pixels must be able to transmit as well as receive optical data signals. This can be accomplished by integrating VCSELs together with MSM photodetectors either through hybrid or multichip module packaging, or through monolithic integration of the two devices. The technology required to fabricate large, uniform, high density, high-yield, and low-cost VCSELs and MSM photodetectors still need several years of development and refinement. The additional task of monolithically integrating the two devices together with processing logic such as MESFETs to form smart pixel arrays is a challenging and worthy long term goal having great potential. For current and near future needs, however, the hybrid integration (for example, flip-chip bonding) of transmitter and receiver arrays with well developed silicon technology such as CMOS logic can be exploited to create highly intelligent smart pixels. Today's commercial CMOS technology found in today's workstations and personal computers has already and continues to address problems arising from increasing density of transistors. Heat dis-

sipation is extremely low and uniformity of devices is kept to within a strict tolerance to achieve high yields acceptable for the current competitive commercial market. The promise of integrating well developed electronic technology with the interconnection advantages of optoelectronic receivers to develop fully functional photonic backplanes is realizable in the near future.

5.2.2 Scalability

Several factors contribute to the scalability of the system. In order for the system to remain compact and competitive, the pitch between boards must be less than or comparable to that of existing electronic backplanes. This was achieved for a 4x4 array with a center to center pitch of 125 μm by using off the shelf bulk optics. An important point to consider, however, is that as the backplane grows and board capacity increases, the aggregate bandwidth needed to support several simultaneous board to board communications also increases. One method by which this is accomplished is by taking advantage of the large space-bandwidth product and increasing the number of optical channels by employing larger arrays of smart pixels. Keeping the board pitch constant, the optics must be able to relay large arrays of optical data with minimal aggravation in aberrations, packaging, and misalignment tolerances. Research into designing and fabricating arrays of diffractive and refractive microlenses that scale easily with larger smart pixel arrays can be more realistic and cost effective than custom made bulk optics. Because diffractive microlenses are severely affected by the potential wavelength variations of the light source (VCSEL), refractive microlens arrays seem to be the most promising component for relaying large arrays of optical data signals in the near future. Clearly, as smart pixel arrays grow in size, continued research in microlens arrays will be needed.

As discussed at the beginning of this thesis, free-space photonic backplanes do not suffer from line loading experienced from their electronic counterpart. Therefore, the PCB carrying capacity of photonic backplanes is much larger and not limited by the interconnection technology it employs. This advantage, however, comes at the expense of increased optoelectronic packaging challenges. To optically interconnect more than two

boards, the smart pixels need to be packaged on both sides of the daughterboards. Since fin-type heat sinks can no longer by attached to the bottom of the smart pixel package, this places constraints on the daughterboard's ability to dissipate heat. Nevertheless, a simple and commonly used solution for which heat sinks cannot be placed at the location of interest is to sandwich a highly heat conductive layer within the middle of the PCB. This layer serves as a heat sink for the components across the entire board. The heat is dissipated from this layer by fin-type heat sinks placed at more convenient locations (for example, along the edges of the board). Thermoelectric coolers can also be used to facilitate heat dissipation.

Another aspect of the packaging challenge is the stability and optomechanical alignment of the smart pixels with the optics. As the system grows to accommodate additional PCBs, the optical alignment of signals becomes a critical issue as optomechanical stability becomes dependent on several daughterboard stages. An approach that worked well and described in the testing and characterization chapter is a divide and conquer approach. Where possible, prealignments prior to successive integration cycles must be permanently fixed in place. For instance, the tight micron alignment tolerances of the microlens arrays to the smart pixels can be achieved by growing or depositing the relay optics directly onto the VCSELs and MSM photodetectors. This approach can remove many possible sources of misalignment errors and allows the interrogation of critical system parameters.

5.2.3 Additional Issues

The most critical requirement in the design, integration, and testing of a complex system is the identification and accessibility of critical system parameters. Otherwise, confirmation of correct system functionality is not possible. Perhaps a more subtle result stemming from the above requirement is that each of these parameters must be mutually independent. This allows sources of error to be readily located. As an example, suppose the misalignment parameter needs to be determined. First, in what manner can this be measured (identified) needs to be determined. Second, can this method of measurement

be applied when necessary (accessibility) also needs to be confirmed. In either instance, should the answer depend on other unknown and possibly varying critical system parameters, new solutions should be investigated. if none are available, the system design and integration cycle must be re-examined. The implementation of the VCSEL/MSM demonstrator used a two phase approach in which as many as possible unknown parameters were identified and methods of access determined in the first phase. With confirmation of these parameters (such as system alignment and optical power), the second phase mostly entailed technology enhancements and improvements. As system demonstrators grow in functionality and complexity, research into system development will be of benefit.

Appendix A

MSM mask drawing

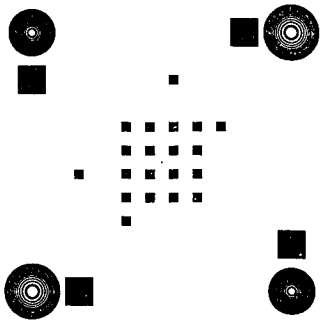

Figure A.1 - MSM mask drawing.

Appendix B

Beam holder platform drawing

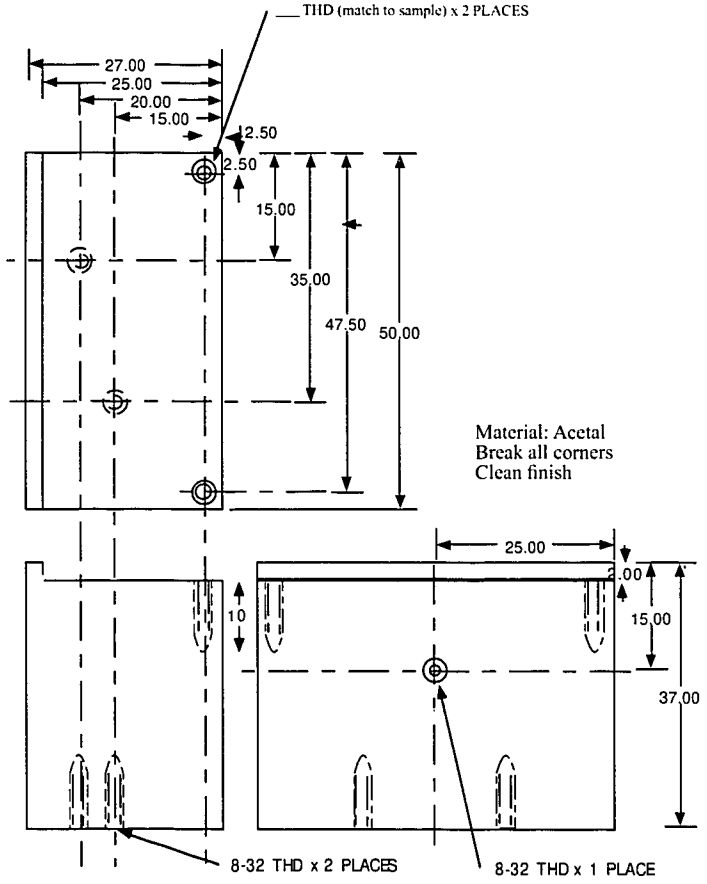

Figure B.1 - Beam splitter platform used to hold 10mm and 20 mm beam splitter combinations for testing of the detector and receiver board.