Analog Test Bus Structure for Wide-Bandwidth High-Frequency Measurements

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Abstract

Analog test buses facilitate the testing of analog components in integrated circuits through dedicated test ports and switches. IEEE 1149.4 is the established analog test bus standard, but has had limited adoption due to the low maximum measurement frequency of existing implementations. A common approach to accurately measure high-frequency signals is to use high-speed test equipment, such as vector network analyzers (VNA), which employ a detailed calibration procedure. To extend the measurement bandwidth of an analog test bus, this thesis proposes a buffer-based structure that uniquely applies the VNA calibration methodology to de-embed the effects of the test bus components. Calibration reference resistors were integrated into the test bus constructed of voltage and current buffers that characterize the systematic errors present. The proposed test bus structure was tested and compared with the 1149.4 test bus using a discrete component PCB simulation and experiment aimed at measuring a transimpedance amplifier (TIA). The simulation showed the proposed test bus exactly measuring the TIA's performance, while the 1149.4 test bus deviated at higher frequencies. The experimentally measured results echoed the simulation, with the proposed test bus more closely tracking the ideal performance while the 1149.4 test bus became inaccurate. An additional simulation tested the performance of the proposed test bus in a high-speed on-chip implementation with a BiCMOS transistor-level design. The on-chip simulation again showed that the proposed test bus successfully measured the TIA with little error, even with induced process and mismatch variations. These results verified the ability of the proposed test bus to characterize and extract high-frequency errors, extending the measurement bandwidth.

Résumé

Les bus de test analogiques facilitent le test des composants analogiques dans les circuits intégrés grâce à des ports de test et des commutateurs dédiés. IEEE 1149.4 est la norme de bus de test analogique établie, mais son utilisation a été limité en raison de la faible fréquence de mesure maximale des implémentations existantes. Une approche courante pour mesurer avec précision les signaux à haute fréquence consiste à utiliser des équipements de test à haute vitesse, tels que les analyseurs de réseaux vectoriels (VNA), qui emploient une procédure d'étalonnage détaillée. Afin d'étendre la largeur de bande de mesure d'un bus de test analogique, cette thèse propose une structure basée sur un tampon qui applique de manière unique la méthodologie d'étalonnage des VNA afin de supprimer les effets des composants du bus de test. Des résistances de référence pour l'étalonnage ont été intégrées dans le bus de test constitué de tampons de tension et de courant qui caractérisent les erreurs systématiques présentes. La structure du bus d'essai proposé a été testée et comparée au bus d'essai 1149.4 à l'aide d'une simulation de circuit imprimé à composants discrets et d'une expérience visant à mesurer un amplificateur à transimpédance (TIA). La simulation a montré que le bus d'essai proposé mesurait exactement les performances de l'amplificateur de transimpédance, alors que le bus d'essai 1149.4 s'en écartait à des fréquences plus élevées. Les résultats des mesures expérimentales ont fait écho à la simulation, le bus d'essai proposé se rapprochant davantage des performances idéales, tandis que le bus d'essai 1149.4 devenait imprécis. Une simulation supplémentaire a testé les performances du bus de test proposé dans une implémentation sur puce à grande vitesse avec une conception au niveau des transistors BiCMOS. La simulation sur puce a de nouveau montré que le bus de test proposé mesurait avec succès le TIA avec peu d'erreur, malgré les variations induites de processus et de désadaptation. Ces résultats ont vérifié la capacité du bus de test proposé à caractériser et à extraire les erreurs à haute fréquence, en élargissant la bande passante de mesure.

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List of Abbreviations

ATE	Automated Test Equipment
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BIST	Built-In Self-Test
BJT	Bipolar Junction Transistor
Cal1	Calibration Reference 1
Cal2	Calibration Reference 2
Cal3	Calibration Reference 3
CMOS	Complementary Metal-Oxide-Semiconductor
DfT	Design for Test
DIP	Dual In-line Package
DUT	Device Under Test
ECal	Electronic Calibration
ISS	Impedance Standard Substrate
LRM	Line-Reflect-Match
LRRM	Line-Reflect-Reflect-Match
M-TRL	Multiline Through-Reflect-Line

mmWave . . . . . Millimeter Wave

S-Parameters . . . . . Scattering Parameters

SOLT . . . . . Short-Open-Load-Through

TIA . . . . . Transimpedance Amplifier

TRL . . . . . Through-Reflect-Line

VNA . . . . . Vector Network Analyzer

Chapter 1

Introduction

1.1 Motivation

Testing is a critical step of the integrated circuit manufacturing process. Before a chip can be sent to a customer, it must be thoroughly tested to ensure that it behaves as expected and meets its specifications. An individual die is first tested while it is still part of the wafer and again after it is diced and packaged. Automated Test Equipment (ATE) is used to hold the chip/wafer, interface with the pins/pads, and conduct an extensive sequence of tests.

In the volumes and complexity associated with semiconductor manufacturing, testing can represent a significant proportion of manufacturing cost. The test systems are complicated and require a large engineering effort in their own right to effectively test a chip. ATE testers are an expensive and limited resource where it is best to maximize their throughput. The testing time of an individual chip is an important metric that directly influences its cost. Therefore, it is now standard practice to design the chip with knowledge of how it will be tested and to add circuitry to improve test time, accuracy, and coverage [1].

Digital IC test strategies are a mature field compared to their analog and mixed-signal counterparts. Analog and mixed-signal testing is orders of magnitude more complex and costly due to the difficulty in accessing, accurately measuring, and collecting all the rele-

vant performance parameters. This cost is again multiplied as the analog and mixed-signal systems increase in speed. Circuits that operate in the RF and millimeter wave (mmWave) frequency ranges require expensive and carefully configured equipment to test accurately.

Testing and validation are the key components of manufacturing high-frequency chips. Quite a lot of quality research is being conducted to create better analog circuits that will ultimately improve the speed, cost, and reliability of critical communication systems used in the world today. New technologies do not mean anything if they cannot be tested economically in a production environment.

The standard analog test strategy is to simply use the ATE tester and its connection to the chip's ports to measure the analog components. This limits the number of ports to only the final inputs and outputs of the chip. These ports can give a good view of the overall performance but lack insight into individual components. That is, unless an internal node is given a dedicated test port for the purpose of expanding the test abilities. The availability and number of ports are typically tightly controlled, so many dedicated test ports are not feasible.

Design-for-Test (DfT) and Built-In Self-Test (BIST) strategies include dedicated on-chip test circuitry to facilitate better analog testing. Many different types of DfT and BIST exist to best suit their application and goal. The advantages of these strategies include lowering the test cost, increased fault coverage, diagnostics and characterization, and system-level diagnostics [1]. Some of the general types of DfT include analog test buses with switches, loopback modes, on-chip sampling, and DC to RF performance correlation [1].

DfT and BIST tend to be very application specific, with every class of analog circuit having unique implementations of test circuits. There is also a trade-off between the test circuitry and the silicon area. Ideally, one wants to enable test functionality in the least amount of area possible. DfT and BIST are also less accurate compared to the equivalent measurement made with external equipment. Test equipment uses the fastest and most accurate version of the measurement hardware because it is not limited by space. They also

have traceability to established standards so that measurements are known to be accurate.

Analog test buses are a DfT strategy that is an extension of the popular digital test bus scan chain. Through a standardized test port, test equipment can interface with the IC and different test signals are sent to different parts of the IC through a series of analog switches (transmission gates). Analog test buses are a general structure that can be used in many different applications. IEEE 1149.4 [2] is the established analog test bus standard that defines the test bus interface and topology. The major limitation of analog test buses is the maximum measurement frequency, which has prevented its use in RF and mmWave applications. The poor high-frequency measurement is the result of significant parasitic capacitance on the test bus due to the amount and size of the analog switches.

RF and mmWave circuits are typically characterized using high-quality test equipment such as a Vector Network Analyzer (VNA). A major reason VNAs can accurately measure high-frequency signals is because of their calibration procedure. Systematic errors caused by defects and parasitic elements in the equipment's cables and probes corrupt the signal. By measuring calibration references, which are circuits with known behavior, the VNA can characterize the errors. Then after measurement of the device under test (DUT), the true DUT performance can be de-embedded from the errors, resulting in an accurate measurement.

Combining the high-frequency measurement capabilities of a VNA with an analog test bus would expand its maximum test frequency and make the test bus strategy viable in new applications. Continuing to use the high-quality external VNA would keep the measurements accurate and traceable. The calibration references could be integrated within the test bus on-chip to extract errors caused by the test bus itself. Therefore, allowing the effects of the test bus to be de-embedded from DUT measurements giving accurate results across the bandwidth of the DUT.

1.2 Research Goals

This thesis proposes a high-frequency wide-bandwidth analog test bus structure that uses VNA-style calibration to improve the test and validation of an IC's high-frequency analog components. The components of the test bus are evaluated and optimized to increase their maximum operating frequency. VNA-style calibration references are integrated into the test bus to allow for extraction of the test bus systematic errors. Multiple test bus structures are considered to create strong signal paths.

The VNA calibration procedure is adapted and expanded to be compatible with the test bus. Unique calibration references are created that can be integrated on-chip with the test bus. The calibration algorithm is altered with a 4-port to 2-port conversion and unique calibration references. Common problems that affect VNA calibration are evaluated in the test bus context.

A discrete component PCB experiment of the test bus structure is constructed and measured to compare its performance with the prior art. Multiple simulations are presented to demonstrate ideal performance and challenges in integrating the test bus in an IC.

1.3 Structure of Thesis

The remainder of this thesis is organized as follows.

Chapter 2 contains a review of the literature on key topics related to the analog test bus and VNA calibration. The chapter begins by analyzing the established IEEE 1149.4 analog test bus, its published implementations, and its high-frequency measurement limitations. Then background on VNA measurements and scattering parameters (S-parameters) is given to provide context for the next section on VNA calibration. A step-by-step derivation of the calibration procedure used in this thesis is given. Next, an in-depth review of VNA calibration references is presented, including on-chip and electronic calibration references.

Chapter 3 presents the design of the proposed analog test bus topology and its important structural requirements. The proposed analog test bus design is described in detail while providing context for the decisions. A 4-port and 2-port version of the test bus are presented, and the structural differences between them and the IEEE 1149.4 test bus are compared. An example simulation is used to show the performance difference between ideal low-frequency measurements and high-frequency measurements with errors.

Chapter 4 documents the details of the calibration algorithm that are unique to the proposed test buses. First, how S-parameters are converted to circuit parameters, such as voltage or current gain, is recorded as background information. Then the 4-port to 2-port conversion required to use the 4-port test bus is derived using a signal flow diagram. The proposed calibration references are created using load resistors that can be characterized with a low-frequency measurement. The 2-port test bus needs a specific requirement with respect to the buffers in order to enable calibration. An example simulation is used to highlight the theoretical performance and difference compared to the IEEE 1149.4 test bus.

Chapter 5 presents the main experiment of the thesis in which the proposed 4-port test bus is built on a PCB using discrete components. An IEEE 1149.4 test bus PCB is also constructed out of the exact same components to provide a comparison of their structure and calibration ability. The DUT for both test buses is a transimpedance amplifier (TIA) circuit where the goal is to accurately measure the transimpedance at all frequencies.

Chapter 6 investigates the challenges in applying the proposed test bus to a high-frequency IC application. The proposed 4-port and 2-port test buses are implemented in a high-speed BiCMOS process. Special design decisions are required to create buffers with power on/off ability and calibration references that integrate into the test buses. The proposed test buses are simulated and compared against an 1149.4 implementation using a Monte Carlo simulation to induce mismatch variations.

Chapter 7 summarizes the key results of the thesis and ends with recommendations for future work.

Chapter 2

Literature Review

There are many works in the literature that report on the performance of existing analog test buses. VNA calibration is an even more extensive field with many different approaches catering to a multitude of applications. This chapter begins by analyzing the currently published work on the IEEE 1149.4 analog test buses. The gain calibration of the 1149.4 test bus is presented, and the high-frequency performance limitations are closely inspected. The general background on VNA measurements and S-parameters is then given before going into detail on the VNA calibration algorithm. An extensive review of VNA calibration references is documented, going into specific detail with on-chip and electronic calibration.

2.1 Digital Test Bus

Digital test buses and scan chains have become a common approach to testing digital components. The idea of a digital test bus is to provide a mechanism to apply arbitrary bit sequences to a digital block and read the resulting bits. The test bits are applied through a dedicated test port on the IC and moved around the chip through the use of a scan chain. This common testing infrastructure can test any digital block connected to the scan chain. The digital test bus eliminates the need to probe and connect individually to each input and output of a digital block to test it.

IEEE 1149.1 [2] defines the standard for creating a test access port and a boundary-scan architecture. The standard focuses on creating a boundary scan which places the scan chain at the perimeter of a chip between its pins and internal circuitry. This facilitates the testing of the interconnections between two ICs on the same PCB. The boundary scan can also be used to test the internals of the IC.

Other digital test bus implementations can create a more complete scan of the internal digital components and not just the boundary by routing the scan to smaller internal blocks. This more fine-grained approach gives greater insight into the chip.

2.2 Analog Test Bus

IEEE 1149.4 [3] is the mixed-signal extension to IEEE 1149.1 to add support for analog testing. The purpose of the standard is to provide a structure for analog interconnect, parametric, and internal tests. To accomplish this, 1149.4 uses switches to connect the DUT, test buses, and test ports along with the digital scan chain and interconnect test.

Fig. 2.1 shows the high-level 1149.4 extension, which includes new analog test infrastructure and a normal digital test bus. AT1 and AT2 are the analog test ports that interface the outside test equipment to the chip. The Test Bus Interface Circuit connects the test ports to the internal analog test buses (AB1 and AB2) with switches and supports basic calibration. Connected to the analog test buses are the Analog Boundary Modules (ABM) which connect the test buses to the DUT and contain interconnect test circuitry. The normal 1149.1 blocks include the Test Control Block with the digital test ports (TDI and TDO) and the boundary scan chain that traverses the Test Bus Interface Circuit, ABMs, and digital scan blocks.

The focus of this thesis is on the internal DUT test performance of the test bus. Fig. 2.2 shows a simplified 1149.4 schematic of only the analog signal paths and components used to test an internal DUT. The two primary components of the test bus are the current and voltage buffers that act as switches to connect the ports and buses to the DUT. Important

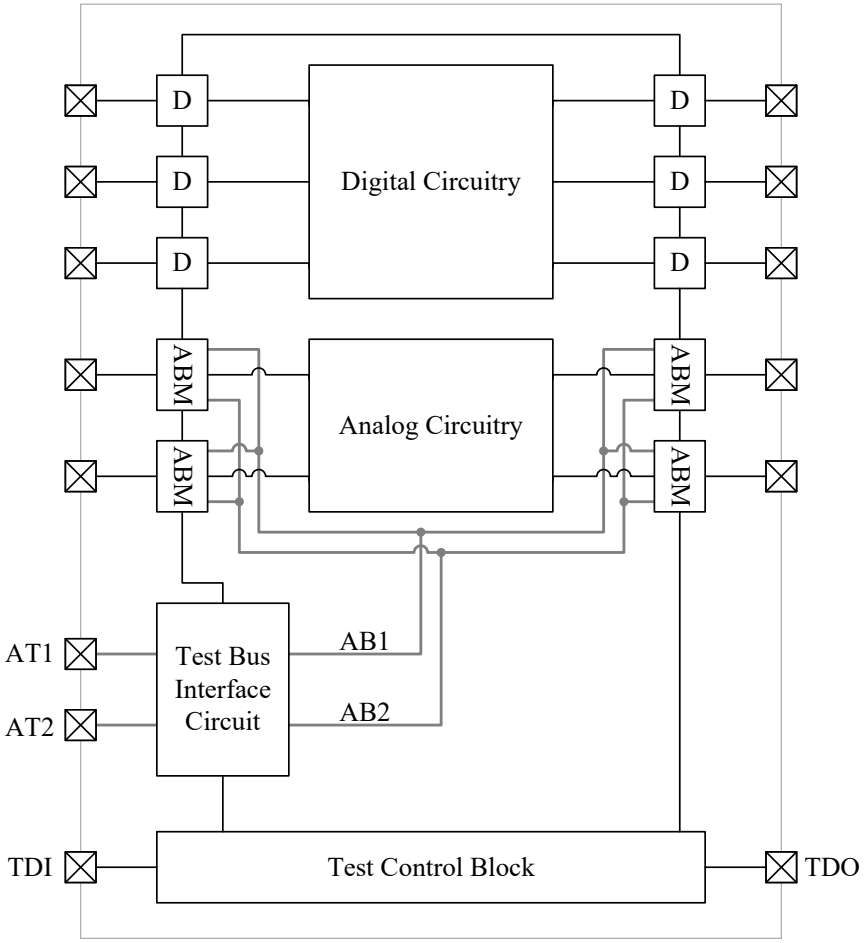


Figure 2.1: High-level diagram of IEEE 1149.1 with the mixed-signal extension IEEE 1149.4 [2, 3].

to note is the fact that 1149.4 does not specify how the switches are implemented. In most cases using a CMOS process, transmission gates would be used. Alternatively, in a bipolar process, 1149.4 suggests using buffers because of the lack of transmission gates. In some cases, the switches are conceptual and can be implemented in more creative ways, such as cutting off power to circuit blocks.

2.2.1 High-Frequency Performance

A major limitation of 1149.4 is its maximum operating frequency. Technically, the standard does not specify a maximum operating frequency, but the reported bandwidths have

been limited. Hannu et al. [4] identified the lack of support for RF testing as one of the reasons why adoption of 1149.4 is slow. The 1149.4 test bus can simply only measure DC or low-frequency signals.

This low bandwidth is the result of large series resistance and shunt capacitance of the switches and bus [5, 6]. Test bus switches implemented using CMOS transmission gates can have significant series resistance depending on the size of transistors used. Parker [7] provides some basic specifications for the test bus, saying that the total series resistance from the test port to the DUT should be less than 10 kΩ. Sunter et al. [6] gives an example resistance of 1 kΩ and a total capacitance on and off the chip of 100 pF. This example says a voltage source could be monitored with a bandwidth of 1.6 MHz. The alternative 1149.4 implementation uses buffers instead of switches, which reduces the series resistance and generally allows for higher operating frequency. Sunter et al. [6] presents a 1149.4 design using buffers that improved the measurement frequency to 30 MHz.

Evidently from the above examples, using the 1149.4 test bus to conduct high-frequency signals in RF applications is not feasible. A different approach combining RF circuits and 1149.4 commonly found in the literature involves using 1149.4 to relay information at DC or low frequencies. Shrivastava and Banerjee [8] present an analog probe that interfaces with 1149.4 with the sole purpose of reading the DC voltages of the internal analog components. They position this work saying that improvements have been made in predicting RF performance with only DC voltages. Similarly, Zivkovic et al. [9] present an analog test bus design that measures DC voltages inside a CMOS transceiver. The design provides information on power and ground voltage, band-gap references and other biasing, and the DC component of signals.

Alternatively, the test bus can be used to send information about RF signals. Syri et al. [10] use RF power detectors to convert the RF signal strength to a DC voltage that is then read through an analog test bus. They also briefly present a frequency detector that produces a DC voltage proportional to the signal frequency. Hakkinen et al. [11] converts

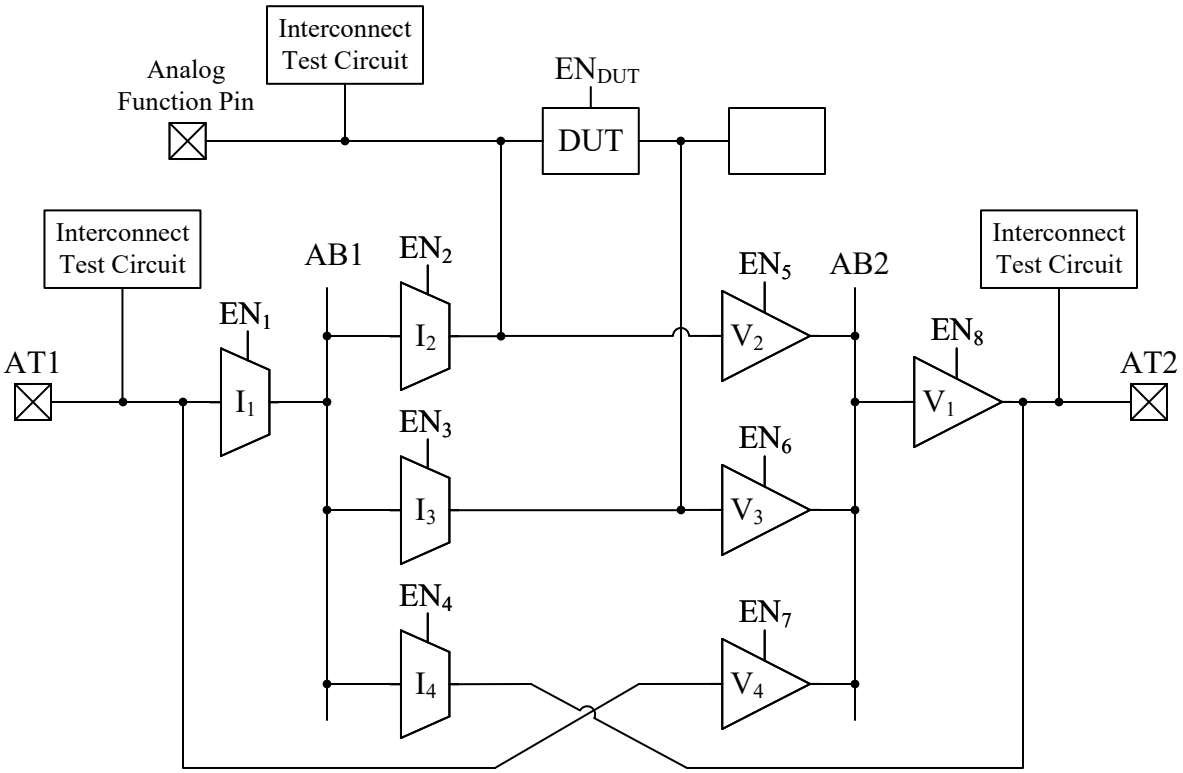


Figure 2.2: Schematic of the IEEE 1149.4 analog test bus structure constructed with voltage and current buffers for an internal DUT measurement [3].

the RF signal to a sufficiently low frequency using frequency mixing and sub-sampling to send it out on the test bus.

These existing RF analog test bus approaches are incomplete and are only necessitated by the fact that a typical analog test bus cannot support high frequencies. Measurement of many DC voltages inside an analog component has the advantage of proving some information about the circuit's functionality. These low impact test points can also be placed in many locations. DC voltages do not prove the RF performance. It is an indirect measurement that can only predict performance. Adding additional circuitry to detect the RF power or convert the signal to low-frequency adds complexity and cost. Ideally, an analog test bus would be capable of performing accurate direct measurements through a simple and standardized structure.

2.2.2 Gain Calibration

1149.4 provides a simple way to calibrate for non-ideal gain from the ports, bus, and switches/buffers. This is done by providing two additional calibration paths off the test bus to directly measure the calibration path gain. Referencing Fig. 2.2 again, I_4 and V_4 are the buffers that perform calibration by connecting directly to the opposite test port. To characterize the current buffers, only I_1 and I_4 are enabled, and the current gain is measured across the test ports. Similarly, to characterize the voltage buffers, only V_1 and V_4 are enabled, and the voltage gain is measured across the test ports. Using the measured buffer gains, their effects can be de-embedded from the DUT measurement.

A block diagram representation of 1149.4 measuring a transimpedance DUT is shown in Fig. 2.3 and consists of three different transfer function blocks. The current and voltage buffer gain, $A_I(s)$ and $A_V(s)$, are measured by the dedicated calibration paths

$$A_I(s) = \frac{I_{cal\_out}(s)}{I_{cal\_in}(s)} \qquad A_V(s) = \frac{V_{cal\_out}(s)}{V_{cal\_in}(s)} \tag{2.1}$$

where $I_{cal\_in}(s)$ is the input current, $I_{cal\_out}(s)$ is the output current, $V_{cal\_in}(s)$ is the input voltage, and $V_{cal\_out}(s)$ is the output voltage. Similarly, the test bus measured transimpedance, $Z_M(s)$, is measured by the test bus path

$$Z_M(s) = \frac{V_M(s)}{I_M(s)} \tag{2.2}$$

where $V_M(s)$ is the output voltage, $I_M(s)$ is the input current. The transfer function system can be written as

$$Z_M(s) = A_I(s) \cdot Z_{DUT}(s) \cdot A_V(s) \tag{2.3}$$

and rearranged to solve for the de-embedded DUT transimpedance

$$Z_{DUT}(s) = \frac{Z_M(s)}{A_I(s) \cdot A_V(s)}. \tag{2.4}$$

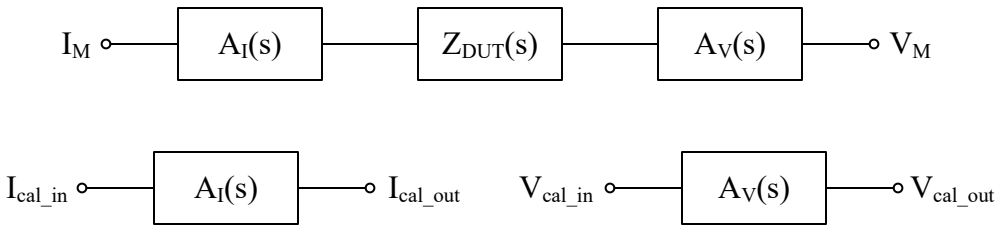


Figure 2.3: Block diagram of IEEE 1149.4 calibration using transfer functions Z_{DUT}, A_I, and A_V.

The 1149.4 calibration approach assumes that the buffers measured as part of the calibration perform exactly the same as the buffers in the DUT measurement. The buffers are physically different and therefore rely on their behavior matching. Su and Chen [12] inspect the 1149.4 calibration procedure and its ability to remove the parasitic effects of the test bus. The authors find that using buffers instead of transmission gates improves the calibration performance because it lessons the loading differences between the DUT and the calibration measurements. One must ensure that the loading on the calibration path measurements is similar to the loading the switches/buffers will experience connected to the DUT.

1149.4 calibration is still limited to only account for the buffer gain. The load matching that was discussed aims to increase the time the buffer gain is the dominant factor. Loading can still impact the calibration performance, and this is especially true if the interfaces between the DUT and buffer have similar impedances. 1149.4 also fails to account for other high-frequency effects from the port and bus.

2.3 High-Frequency Measurements Using S-Parameters

The established way to measure high-frequency analog components is by using high-quality external test equipment, such as a Vector Network Analyzer (VNA) [13, 14]. Vector refers to the fact that both magnitude and phase of a signal is measured and network analyzer refers to the fact that it measures network parameters. The type of network parameters measured by a VNA are the scattering parameters (S-parameters) because the technology

was developed around directional couplers that can directly extract the S-parameters.

2.3.1 S-Parameter Background

The fundamentals of S-parameters are summarized in this section to provide background for the next sections on calibration and test bus calibration. S-parameters are derived from transmission line theory and the concept of traveling waves. The theory in this section is adapted from Gonzalez [15].

The voltage at a position along a lossless transmission can be written as

$$V(x) = Ae^{-j\frac{2\pi}{\lambda}x} + Be^{j\frac{2\pi}{\lambda}x} \tag{2.5}$$

where A and B are complex constants, x is the distance from one edge, and λ is the wavelength. Inspecting (2.5) shows that the voltage is the sum of two different wave components. An important value of a transmission line is the characteristic impedance, which for a lossless transmission line is defined as

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.6}$$

where L and C are the inductance and capacitance per unit length, respectively. The notation for the two waves in a transmission line is then written as

$$a(x) = \frac{Ae^{-j\beta x}}{\sqrt{Z_0}} \tag{2.7}$$

and

$$b(x) = \frac{Be^{j\beta x}}{\sqrt{Z_0}}. \tag{2.8}$$

Fig. 2.4 shows a 2-port network system with transmission lines and their traveling waves driven by a source and load signal. The S-parameters of the center 2-port network are defined by the traveling waves as the edges of the transmission line closest to the network block.

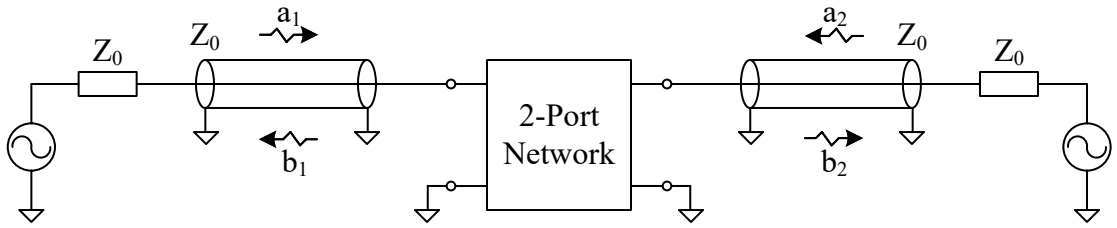


Figure 2.4: S-parameter theory derived from traveling waves in transmission lines.

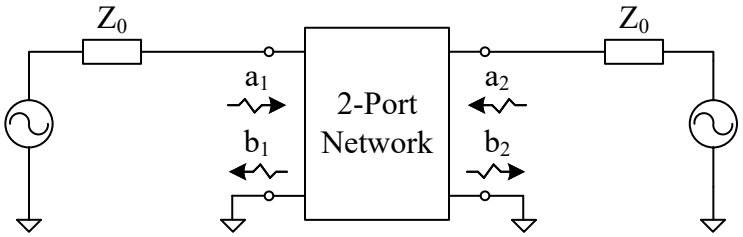


Figure 2.5: S-parameter theory simplification using zero length transmission lines to define S-parameter of a 2-port network.

Transmission lines are not necessary to use S-parameters to describe circuit blocks. The S-parameters stop representing physical values of waves through transmission lines but work well as general network parameters. They can be derived by assuming transmission lines of zero length with characteristic impedance Z_0. Repeating (2.5), (2.7), and (2.8) with $x = 0$ gives

$$V = A + B \tag{2.9}$$

$$a = \frac{A}{\sqrt{Z_0}} \tag{2.10}$$

$$b = \frac{B}{\sqrt{Z_0}}. \tag{2.11}$$

Fig. 2.5 shows a 2-port network system with no transmission lines and the wave notation at the nodes around the network block. The S-parameters are defined by ratios of reflected and transmitted waves when applying a signal to only one port such as

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}. \tag{2.12}$$

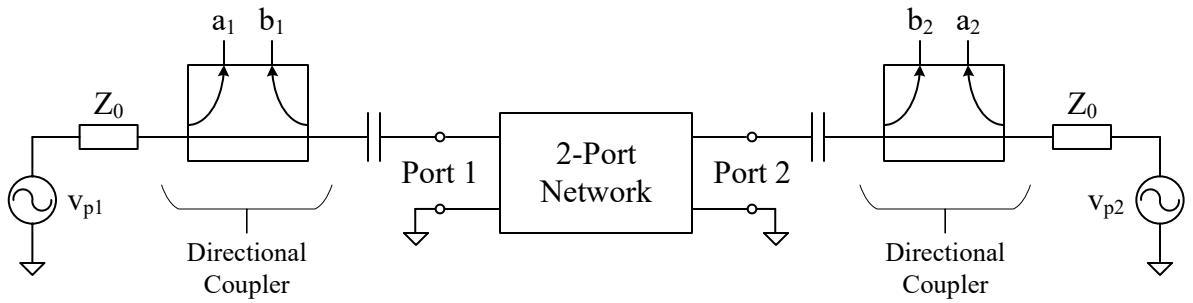


Figure 2.6: High-level internal structure of a VNA with the directional couplers used to measure the incident and reflected waves.

The S-parameters written in matrix form is then

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.13}$$

and the S-parameter matrix is usually written as a single variable

$$\mathbf{S} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}. \tag{2.14}$$

2.3.2 Directional Coupler and Schematic

A VNA measures the S-parameter traveling waves using two directional coupler components. Fig. 2.6 shows a high-level internal VNA schematic with directional couplers and signal sources. S-parameter are measured in two stages. First, v_{p1} is turned on and v_{p2} is set to zero. This means that a_2 is zero and s_{11} and s_{21} are extracted by the directional couplers. Next, during the second stage, v_{p2} is turned on and v_{p1} is set to zero, resulting in s_{22} and s_{12}.

2.4 Vector Network Analyzer Calibration

A VNA can accurately measure high-frequency signals due to its calibration procedure, which accounts for systematic errors in the probe cable, probe contact, and measurement

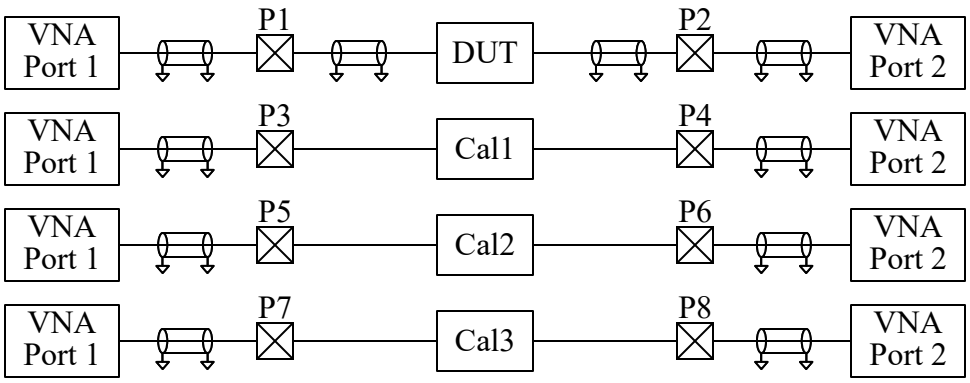


Figure 2.7: Typical VNA measurement setup showing separate measurements of the DUT and three calibration references (Cal1, Cal2, and Cal3).

setup. Knowing these systematic errors, the true DUT can be de-embedded from the DUT measurement. Fig. 2.7 shows the typical VNA setup with the calibration measurements. A transmission line and port symbol are used to represent the parasitic circuit elements that exist between the VNA port, DUT, and calibration references.

The established VNA calibration procedure is presented in this section because it forms the basis for the new proposed analog test bus. The relevant error model is first chosen and the manipulation of the S-parameter matrices to extract the DUT is documented. Details on the importance of calibration references is also provided.

2.4.1 Procedure Details

The first step in performing the VNA calibration is to choose an appropriate model for the system, including the errors. The most common error model, and the model chosen for the proposed test bus, is the 8-term error model shown in Fig. 2.8. The system is described by a cascade of three 2-port networks where the middle 2-port network is the DUT. Surrounding the DUT are the error parameter 2-port networks.

Alternate error models include the 12-term and 16-term models [13, 16]. The additional error terms are mainly used to describe signal paths that bypass across the DUT and to obtain a more accurate model. Additional error terms increase the complexity and cost of

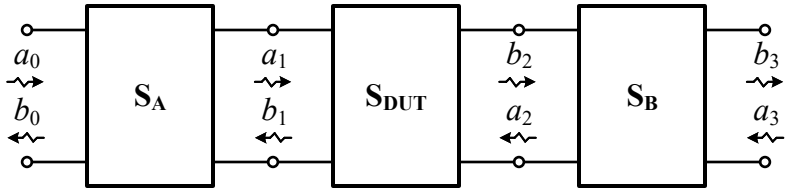


Figure 2.8: 2-port network diagram of the 8-term VNA calibration model.

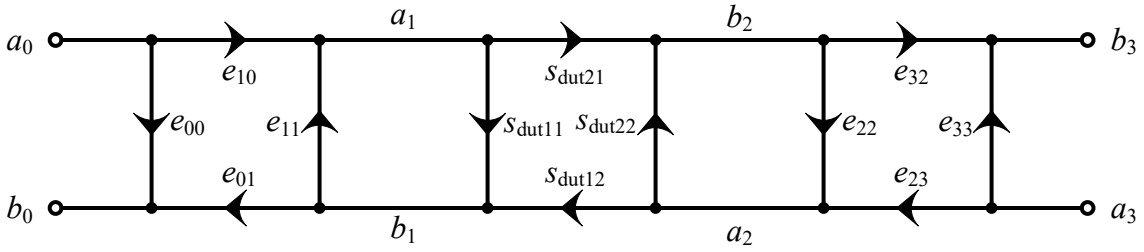


Figure 2.9: Signal flow diagram of the 8-term VNA calibration model.

the calibration due to the need for more measurements and quality references. The 8-term error model was chosen for simplicity and the assumption that signal paths across the DUT are insignificant and eclipsed by the other error parameters.

S-parameters are the 2-port network parameter of choice for VNA calibration because they are directly measured. Therefore, a convenient way to represent the calibration problem is through a signal flow diagram using S-parameters. The calibration model signal flow diagram is shown in Fig. 2.9. The S-parameter matrices in Fig. 2.8 expanded to the individual parameters in Fig. 2.9 are given the notation

$$\mathbf{S_A} = \begin{bmatrix} e_{00} & e_{01} \\ e_{10} & e_{11} \end{bmatrix} \qquad \mathbf{S_{DUT}} = \begin{bmatrix} s_{dut11} & s_{dut12} \\ s_{dut21} & s_{dut22} \end{bmatrix} \qquad \mathbf{S_A} = \begin{bmatrix} e_{22} & e_{23} \\ e_{32} & e_{33} \end{bmatrix}. \tag{2.15}$$

The three series 2-port networks make up a larger 2-port network with the input at port 0 (a_0 and b_0) and the output at port 3 (a_3 and b_3). This S-parameter matrix, which is measured, is denoted as

$$\mathbf{S_{M\_dut}} = \begin{bmatrix} s_{m11} & s_{m12} \\ s_{m21} & s_{m22} \end{bmatrix}. \tag{2.16}$$

The following calibration methodology was first described by Ferrero et al. [17] and the

more recent notation presented by Wollensack et al. [18] is used for its improved readability. This formulation is the fundamental calibration algorithm that is used and built off of in this thesis. It provides a relatively easy-to-understand view of the steps, and the final equations are exactly how they are implemented in the calibration program.

Ferrero et al. [17] showed that the signal flow diagram in Fig. 2.9 can be written as

$$\mathbf{S_{M\_dut}} = \mathbf{E_{00}} + \mathbf{E_{01}} \left(\mathbf{I} - \mathbf{S_{DUT}}\mathbf{E_{11}}\right)^{-1} \mathbf{S_{DUT}}\mathbf{E_{10}} \tag{2.17}$$

where

$$\mathbf{E_{00}} = \begin{bmatrix} e_{00} & 0 \\ 0 & e_{33} \end{bmatrix} \quad \mathbf{E_{10}} = \begin{bmatrix} e_{10} & 0 \\ 0 & e_{23} \end{bmatrix} \quad \mathbf{E_{01}} = \begin{bmatrix} e_{01} & 0 \\ 0 & e_{32} \end{bmatrix} \quad \mathbf{E_{11}} = \begin{bmatrix} e_{11} & 0 \\ 0 & e_{22} \end{bmatrix}. \tag{2.18}$$

This formulation of the signal flow diagram is convenient as it allows the equations to be easily rearranged to isolate the error parameters into a linear system of equations

$$\mathbf{S_{M\_dut}}\mathbf{E_{10}^{-1}} - \mathbf{E_{00}}\mathbf{E_{10}^{-1}} - \mathbf{S_{M\_dut}}\mathbf{E_{10}^{-1}}\mathbf{E_{11}}\mathbf{S_{DUT}} + \left(\mathbf{E_{00}}\mathbf{E_{10}^{-1}}\mathbf{E_{11}} - \mathbf{E_{01}}\right)\mathbf{S_{DUT}} = 0. \tag{2.19}$$

Fully multiplying (2.19) through and writing in matrix form results in the system

$$\begin{bmatrix} s_{m11} & 0 & 1 & 0 & s_{dut11}s_{m11} & s_{dut21}s_{m12} & s_{dut11} & 0 \\ s_{m21} & 0 & 0 & 0 & s_{dut11}s_{m21} & s_{dut21}s_{m22} & 0 & s_{dut21} \\ 0 & s_{m12} & 0 & 0 & s_{dut12}s_{m11} & s_{dut22}s_{m12} & s_{dut12} & 0 \\ 0 & s_{m22} & 0 & 1 & s_{dut12}s_{m21} & s_{dut22}s_{m22} & 0 & s_{dut22} \end{bmatrix} \begin{bmatrix} 1/e_{10} \\ 1/e_{23} \\ -e_{00}/e_{e10} \\ -e_{33}/e_{23} \\ -e_{11}/e_{10} \\ -e_{22}/e_{23} \\ (e_{01}e_{10} - e_{00}e_{11})/e_{10} \\ (e_{23}e_{32} - e_{22}e_{33})/e_{23} \end{bmatrix} = 0. \tag{2.20}$$

With knowledge of how to set up the system of equations, measurements of calibration references are used to fill in the left-hand matrix with known values. For the 8-term error model, three calibration references are needed to solve the system. The 2-port network

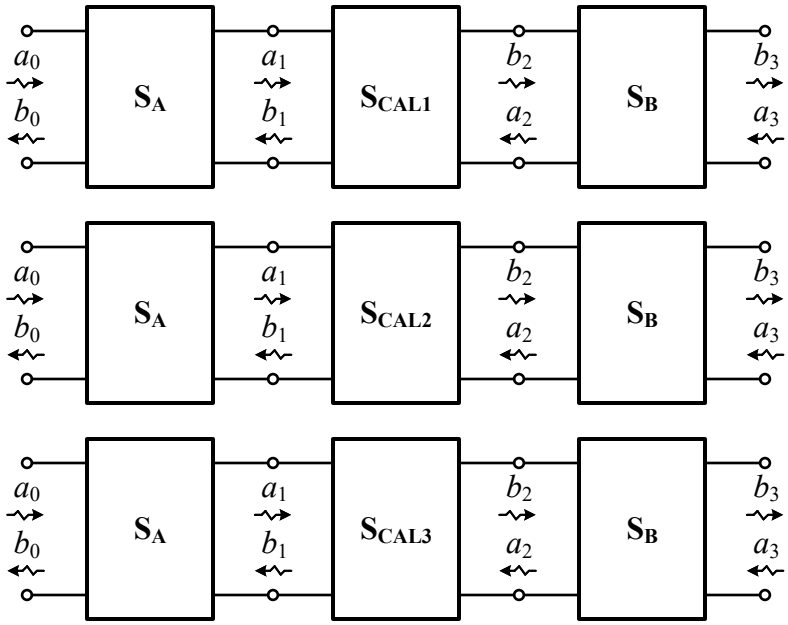


Figure 2.10: 2-port network diagram of the three calibration references.

diagram of the calibration reference system is shown in Fig. 2.10 and the equivalent signal flow diagram is shown in Fig. 2.11. The S-parameter matrices and individual parameters are given the notation

$$\mathbf{S_{CAL1}} = \mathbf{K} = \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} \qquad \mathbf{S_{CAL2}} = \mathbf{U} = \begin{bmatrix} u_{11} & u_{12} \\ u_{21} & u_{22} \end{bmatrix}$$
$$\mathbf{S_{CAL3}} = \mathbf{W} = \begin{bmatrix} w_{11} & w_{12} \\ w_{21} & w_{22} \end{bmatrix}. \tag{2.21}$$

The overall S-parameters of the three networks measured from port 0 (a_0 and b_0) to port 3 (a_3 and b_3) are given the notation

$$\mathbf{S_{M\_cal1}} = \mathbf{K_M} = \begin{bmatrix} k_{m11} & k_{m12} \\ k_{m21} & k_{m22} \end{bmatrix} \qquad \mathbf{S_{M\_cal2}} = \mathbf{U_M} = \begin{bmatrix} u_{m11} & u_{m12} \\ u_{m21} & u_{m22} \end{bmatrix}$$
$$\mathbf{S_{M\_cal3}} = \mathbf{W_M} = \begin{bmatrix} w_{m11} & w_{m12} \\ w_{m21} & w_{m22} \end{bmatrix}. \tag{2.22}$$

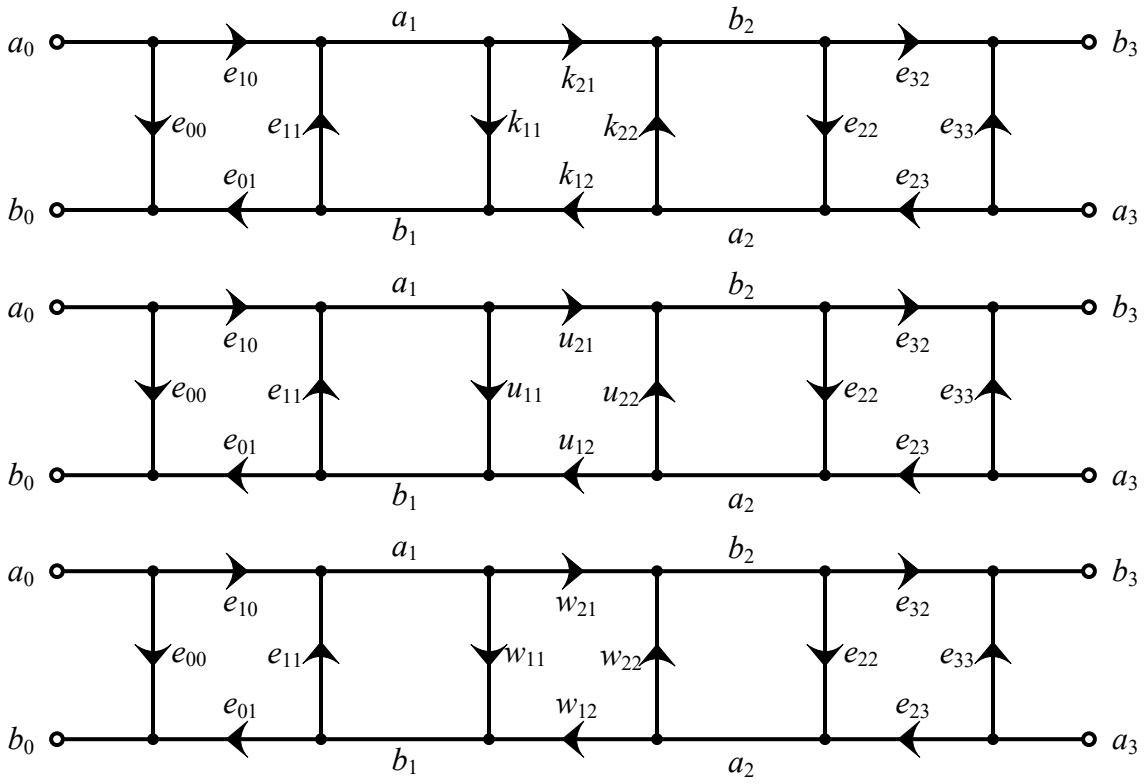


Figure 2.11: Signal flow diagram showing of the three calibration references.

Analyzing and rearranging the signal flow diagram results in

$$\mathbf{K_M E_{10}^{-1}} - \mathbf{E_{00} E_{10}^{-1}} - \mathbf{K_M E_{10}^{-1} E_{11} K} + \left(\mathbf{E_{00} E_{10}^{-1} E_{11}} - \mathbf{E_{01}}\right)\mathbf{K} = 0 \tag{2.23}$$

$$\mathbf{U_M E_{10}^{-1}} - \mathbf{E_{00} E_{10}^{-1}} - \mathbf{U_M E_{10}^{-1} E_{11} U} + \left(\mathbf{E_{00} E_{10}^{-1} E_{11}} - \mathbf{E_{01}}\right)\mathbf{U} = 0 \tag{2.24}$$

$$\mathbf{W_M E_{10}^{-1}} - \mathbf{E_{00} E_{10}^{-1}} - \mathbf{W_M E_{10}^{-1} E_{11} W} + \left(\mathbf{E_{00} E_{10}^{-1} E_{11}} - \mathbf{E_{01}}\right)\mathbf{W} = 0 \tag{2.25}$$

which can be expanded and written in the matrix form

$$\left[\begin{array}{cccccccc}
k_{m11} & 0 & 1 & 0 & k_{11}k_{m11} & k_{21}k_{m12} & k_{11} & 0 \\
k_{m21} & 0 & 0 & 0 & k_{11}k_{m21} & k_{21}k_{m22} & 0 & k_{21} \\
0 & k_{m12} & 0 & 0 & k_{12}k_{m11} & k_{22}k_{m12} & k_{12} & 0 \\
0 & k_{m22} & 0 & 1 & k_{12}k_{m21} & k_{22}k_{m22} & 0 & k_{22} \\
\hline
u_{m11} & 0 & 1 & 0 & u_{11}u_{m11} & u_{21}c_{m12} & u_{11} & 0 \\
u_{m21} & 0 & 0 & 0 & u_{11}u_{m21} & u_{21}c_{m22} & 0 & u_{21} \\
0 & u_{m12} & 0 & 0 & u_{12}u_{m11} & u_{22}u_{m12} & u_{12} & 0 \\
0 & u_{m22} & 0 & 1 & u_{12}u_{m21} & w_{22}w_{m22} & 0 & u_{22} \\
\hline
w_{m11} & 0 & 1 & 0 & w_{11}u_{m11} & w_{21}w_{m12} & w_{11} & 0 \\
w_{m21} & 0 & 0 & 0 & w_{11}u_{m21} & w_{21}w_{m22} & 0 & w_{21} \\
0 & w_{m12} & 0 & 0 & w_{12}u_{m11} & w_{22}w_{m12} & w_{12} & 0 \\
0 & w_{m22} & 0 & 1 & w_{12}u_{m21} & w_{22}w_{m22} & 0 & w_{22}
\end{array}\right]
\left[\begin{array}{c}
1/e_{10} \\ 1/e_{23} \\ -e_{00}/e_{e10} \\ -e_{33}/e_{23} \\ -e_{11}/e_{10} \\ -e_{22}/e_{23} \\ (e_{01}e_{10}-e_{00}e_{11})/e_{10} \\ (e_{23}e_{32}-e_{22}e_{33})/e_{23}
\end{array}\right] = 0. \quad (2.26)$$

Note that (2.26) is a homogeneous system of equations, and to solve, one of the dependent variables must be defined in order to rearrange the equation. Typically, setting $e_{10} = 1$ to rearrange the equation for solving

$$\left[\begin{array}{cccccccc}
k_{m11} & 0 & 1 & 0 & k_{11}k_{m11} & k_{21}k_{m12} & k_{11} & 0 \\
k_{m21} & 0 & 0 & 0 & k_{11}k_{m21} & k_{21}k_{m22} & 0 & k_{21} \\
0 & k_{m12} & 0 & 0 & k_{12}k_{m11} & k_{22}k_{m12} & k_{12} & 0 \\
0 & k_{m22} & 0 & 1 & k_{12}k_{m21} & k_{22}k_{m22} & 0 & k_{22} \\
\hline
u_{m11} & 0 & 1 & 0 & u_{11}u_{m11} & u_{21}c_{m12} & u_{11} & 0 \\
u_{m21} & 0 & 0 & 0 & u_{11}u_{m21} & u_{21}c_{m22} & 0 & u_{21} \\
0 & u_{m12} & 0 & 0 & u_{12}u_{m11} & u_{22}u_{m12} & u_{12} & 0 \\
0 & u_{m22} & 0 & 1 & u_{12}u_{m21} & w_{22}w_{m22} & 0 & u_{22} \\
\hline
w_{m11} & 0 & 1 & 0 & w_{11}u_{m11} & w_{21}w_{m12} & w_{11} & 0 \\
w_{m21} & 0 & 0 & 0 & w_{11}u_{m21} & w_{21}w_{m22} & 0 & w_{21} \\
0 & w_{m12} & 0 & 0 & w_{12}u_{m11} & w_{22}w_{m12} & w_{12} & 0 \\
0 & w_{m22} & 0 & 1 & w_{12}u_{m21} & w_{22}w_{m22} & 0 & w_{22}
\end{array}\right]
\left[\begin{array}{c}
1/e_{23} \\ -e_{00}/e_{e10} \\ -e_{33}/e_{23} \\ -e_{11}/e_{10} \\ -e_{22}/e_{23} \\ (e_{01}e_{10}-e_{00}e_{11})/e_{10} \\ (e_{23}e_{32}-e_{22}e_{33})/e_{23}
\end{array}\right] =
\left[\begin{array}{c}
-k_{m11} \\ -k_{m21} \\ 0 \\ 0 \\ \hline -u_{m11} \\ -u_{m21} \\ 0 \\ 0 \\ \hline -w_{m11} \\ -w_{m21} \\ 0 \\ 0
\end{array}\right]. \quad (2.27)$$

Equation (2.27) is a general system of equations that can be easily solved to obtain the matrix of error parameters. Now knowing the error parameters and the test bus measured

DUT S-parameters, (2.17) can be rearranged to solve for the DUT S-parameters

$$\mathbf{S_{DUT}} = \frac{\mathbf{S_{M\_dut}E_{10}^{-1}} - \mathbf{E_{00}E_{10}^{-1}}}{\mathbf{S_{M\_dut}E_{10}^{-1}E_{11}} - \left(\mathbf{E_{00}E_{10}^{-1}E_{11}} - \mathbf{E_{01}}\right)}. \tag{2.28}$$

2.4.2 Calibration References

Many different kinds and arrangements of calibration references are used for VNA calibration. This is because there are many different applications for VNAs and each type of calibration references as its own trade-offs.

Calibration references have traditionally been integrated on standalone calibration substrates. Usually referred to as an impedance standard substrate (ISS). In this context, the VNA probes are physically moved between the references and measured one at a time. Then the VNA can measure the DUT and de-embed its S-parameters. The types of references used can include short, open, load, transmission line, and through. For example, two common standards are through-reflect-line (TRL) and line-reflect-reflect-match (LRRM). Fig. 2.12 shows a schematic representation of these two standards.

Generally, calibration references are built out of physical structures that, when ideal, have known S-parameters. These S-parameter are known because they are based on the definition of S-parameters with incident and reflected waves. In a reflect-type reference (short or open) all of the incident wave is reflected and the reflection coefficient is 1. In a through-type reference, there are no reflections and unity transmission. A match-type reference using the characteristic impedance of the system gives zero reflections and zero transmission. Therefore, the quality is a function of their physical construction and the S-parameter are inherently known and do not need to be measured.

Equation (2.27) is the critical system of equations that must be solved for calibration. Inspecting the system reveals seven variables and twelve equations, which means that the system is over-defined for the number of variables. This leaves space to strategically ignore equations or add variables to the system. What variables and equations are ignored or

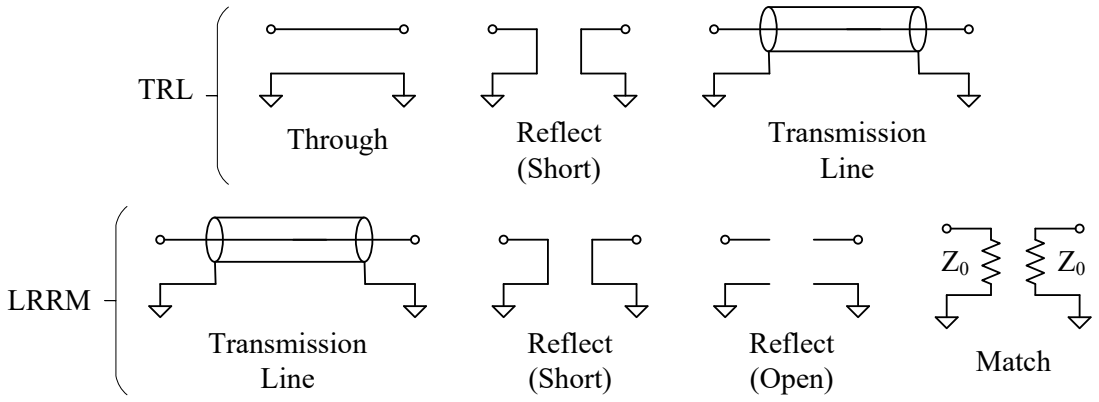


Figure 2.12: Example through-reflect-line (TRL) and line-reflect-reflect-match (LRRM) calibration standards.

added is what really differentiates the many different types of standards available for VNA calibration. Some aspects of the calibration references may not be as accurate as others, so those can be ignored. Using a reflection-type standard with zero transmission automatically removes two equations because any through measurements will be zero.

Adding variables fundamentally changes the system of equations. One is essentially adding a variable to the coefficient matrix and the whole system needs to be rearranged to be solved. The algorithm presented in Section 2.4.1 is the most generic formulation with all the reference S-parameters known. Each calibration standard presented in the literature has a completely different solving algorithm geared to their set of variables. Sometimes using different notation and conventions.

TRL was first presented by Engen and Hoer [19] and does not require that all standards be fully known. The reflect reference and propagation constant of the line reference can be unknown and still allow error terms to be calculated [20]. An extension of TRL, multiline TRL (M-TRL), adds multiple line references to cover a greater bandwidth and increase accuracy [21]. LRRM allows the reflect type standards to be unknown [22].

An important concept in error calibration is the calibration/reference plane. Essentially what parts of the physical circuit are included in either the error blocks or DUT. Looking back at Fig. 2.8, the calibration plane is the boundary between the error blocks ($\mathbf{S_A}$ and

$\mathbf{S_B}$) and the DUT block. In a traditional VNA calibration with the dedicated calibration substrate, the calibration plane is located at the probe tips. This calibration approach does not account for any errors that may be located between the probe tips and the DUT. Differences in the pad parasitic elements and the on-chip interconnect to the DUT are errors not captured in the calibration.

On-Chip Calibration References

Moving the calibration references to the same chip as the target DUT helps move the calibration plane closer to the DUT. On-chip or on-wafer calibration are terms used describing references built in the same process as the DUT. With the on-chip references, the pad and interconnect better match those in the DUT measurements and ideally move more parasitic elements into the error blocks.

On-chip references have become an established technique to improve calibration performance at high frequencies with many books and guidelines written on the subject. Shang et al. [23] outline a guide to making planar S-parameter measurements at mmWave frequencies. It gives high-level pros and cons of references such as SOLT, TRL, LRM, LRRM, and multiline TRL and practical advice on setting up the VNA. Rumiantsev's [24] detailed book describes the design of calibration references for high-performance mmWave devices. Williams et al. [25] presents design guidelines for mmWave on-chip TRL.

TRL or multiline TRL is the generally recommended on-chip calibration reference. Rumiantsev et al. [26] present a comparison of on-wafer multiline TRL and LRM to typical off-wafer SOLT reference. The on-wafer references outperformed the off-chip references in the frequency range of 1 to 110 GHz. Williams et al. [27] perform a similar experiment comparing on-wafer TRL to off-wafer SOLT and LRRM. The experiment again finds a performance improvement for TRL in the mmWave frequencies. The advantages of moving the calibration plane closer to the DUT only become important at mmWave frequencies as this is when the parasitic element difference becomes large.

Other new on-wafer calibration standards have also been investigated. Huang et al. [28] present an extension to TRL with an additional transmission line. Huang et al. [29] present an on-chip reference for production test applications up to 110 GHz. Wei et al. [30] present a general 4-port CMOS calibration references for 1 to 110 GHz. Yau et al. [31] compare open-short, split-through, and TRL de-embedding techniques for on-wafer DUT measurement for frequencies DC up to 170 GHz.

On-chip references are essentially the same as off-chip references except they are optimized for different processes and form factors. They are still mostly passive circuits with their own pads that must be probed and measured individually. The only advantage they provide is to extend the calibration bandwidth into the mmWave frequency range.

Electronic Calibration References

An established alternative to using physical calibration substrates is using an electronic calibration (ECal) module. ECal uses active electronic components to switch between the calibration references of a standard. This means that a single connection is made to the ECal block instead of having to physically move the probes between the references like on a substrate standard. After using the ECal module, the DUT is measured separately as normal.

ECal modules are a popular offering due to their quality, capability, and convenience [13]. ECal modules usually communicate directly with the VNA, allowing the entire calibration procedure to be automated [32, 33]. A single button press measures all the calibration references and saves the data. In contrast to the multistep process to measure all the calibration references of a substrate standard. In all but the most demanding applications, ECal has been verified as an accurate way to calibrate a VNA [34, 35, 36].

Original ECals used a transmission line shunted by PIN diodes along its length. Forward biasing the diodes shorts the transmission line different lengths from the ports which creates the different references [13]. Abramowicz and Lewandowsk [37] present a different an ECal

created from micro-electromechanical system (MEMS) switches that works from DC to 8 GHz.

A logical extension for ECal is to integrate it on-chip alongside the DUT, like what was done with normal calibration substrate standards. This will move the calibration plane closer to the DUT while still having the ECal benefit of not having to reposition probes between the reference measurements. A variety of techniques exist to create electronic references on-chip.

Xie et al. [38] present an ECal that uses Schottky diodes as calibration references which are varied by changing the biasing voltages applied through the wafer probes. The paper aimed at significantly increasing the operating frequency to the submillimeter-wave band (325-500GHz). However, it first relies on a characterization step using TRL to obtain the reference S-parameters.

There are a series of papers from the same author that present multiple ECal standards that are created using CMOS transistors. Three CMOS transistors in a pi network arrangement are used to create the references [39, 40, 41]. The transistors are either turned on/off as switches or have their gate bias voltage varied to create different impedances. A low-frequency measurement is used to characterize the references. Chien and Niknejad [42] then use a single CMOS transistor that creates a LRRM-type standard by varying the gate bias voltage and disconnecting the wafer probes. Chien [43] uses a transmission line loaded with 20 distributed CMOS switches.

Integrated ECal modules show promise in providing the same convenience of standalone ECal modules while moving the calibration plane closer to the DUT. A difficult part of integrated ECal is accurately knowing the reference S-parameters and being able to ignore or account for parasitic elements that impact the references. Less of the references are based off physical structures with defined reflections. Additionally, most ECal implementations are not independent modules and rely on DC biasing sent in on the measurement probes.

2.5 Summary

The current implementations of the IEEE 1149.4 analog test bus standard are limited in the maximum measurement frequency they can obtain. Their gain calibration does a poor job of accounting for errors that can occur at higher frequencies. VNAs, in contrast, do an excellent job at measuring high-frequency signals by employing a detailed calibration procedure. The procedure measures multiple calibration references, which characterizes the systematic errors present in the measurement setup. Knowing the errors, the true DUT performance can be de-embedded. There are many types of calibration references, each geared for different applications. Of note are the on-chip and electronic calibration reference categories. On-chip calibration references move the calibration plane closer to the DUT and account for errors but are still based on the large physical structures used in normal VNA substrate standards. Electronic calibration references allow the VNA probes to remain stationary while measuring the references by changing them with active components. On-chip electronic calibration references combine these advantages but are more difficult to characterize and manipulate.

Chapter 3

Proposed Analog Test Bus Structure

Using the literature review background on analog test buses, VNA calibration, and calibration references, an analog test bus structure that can accurately de-embed high-frequency errors is proposed. The proposed structure is split into two variations: a 4-port and 2-port test bus. The 4-port test bus is the primary structure, and its design is described in detail first. Calibration references are added to the test bus and the structure is informed by the requirement to consistently fit an error block calibration model. A comparison with 1149.4 to highlight the high-frequency measurement performance is presented with a simulated example. The 2-port test bus requires a specific condition with the reverse signal in order to be accurate. The 2-port test bus structure is described and added to the simulated example to compare with the other designs.

As discussed in the literature review section, the 1149.4 test bus has poor high-frequency performance and limited calibration ability. These problems have prevented 1149.4 from being used in high-frequency applications. VNAs on the other hand, are an established high-frequency tool with comprehensive calibration ability. VNAs are not a replacement for an analog test bus applications because they require dedicated ports for each analog block to be tested.

Combining the benefits of an analog test bus with a VNA style calibration procedure

would extend the measurement bandwidth and open up new test bus applications. To accomplish this, VNA-style calibration references are integrated within the test bus, and the test bus structure is altered to facilitate this.

The backbone of the proposed test bus structure are voltage and current buffers capable of being turned on/off to act as switches and route signals to/from circuits connected to the test bus. Buffers are used instead of transmission gates because buffers offer a greater frequency bandwidth. This fact is the same for 1149.4, as was discussed in the literature review Section 2.2.

The switching buffers allow the system to move between three distinct operation modes: mission, test, and calibration. Mission mode is the default state when the DUT operates normally and the entire test bus is disabled. Test mode uses the VNA and first buffer group to measure the DUT. Calibration mode uses the three other buffer groups separately to measure the calibration references.

3.1 4-Port Test Bus

The high-level structure of the 4-port test bus is shown in Fig. 3.1 and will be referenced throughout this section. The 4-port test bus gets its name from the 4 external analog test ports it uses. At the top and center of the diagram is the DUT with its normal operation connections, in this case, its input connected to an external pin and its output connected to an arbitrary next circuit stage. Also connected below to the DUT input/output is the test bus.

The four test ports (AT1 - 4) are each connected to an internal test bus (AB1 - 4) that is then connected to the buffers. The voltage and current buffers are labeled with V_n and I_n being the nth buffer, respectively. AT1 and AT2 are input ports that connect to the test signal source (VNA Source 1 and 2) and current buffers to drive the signal to the DUT or calibration references. AT3 and AT4 are output ports that connect to the voltage buffers to

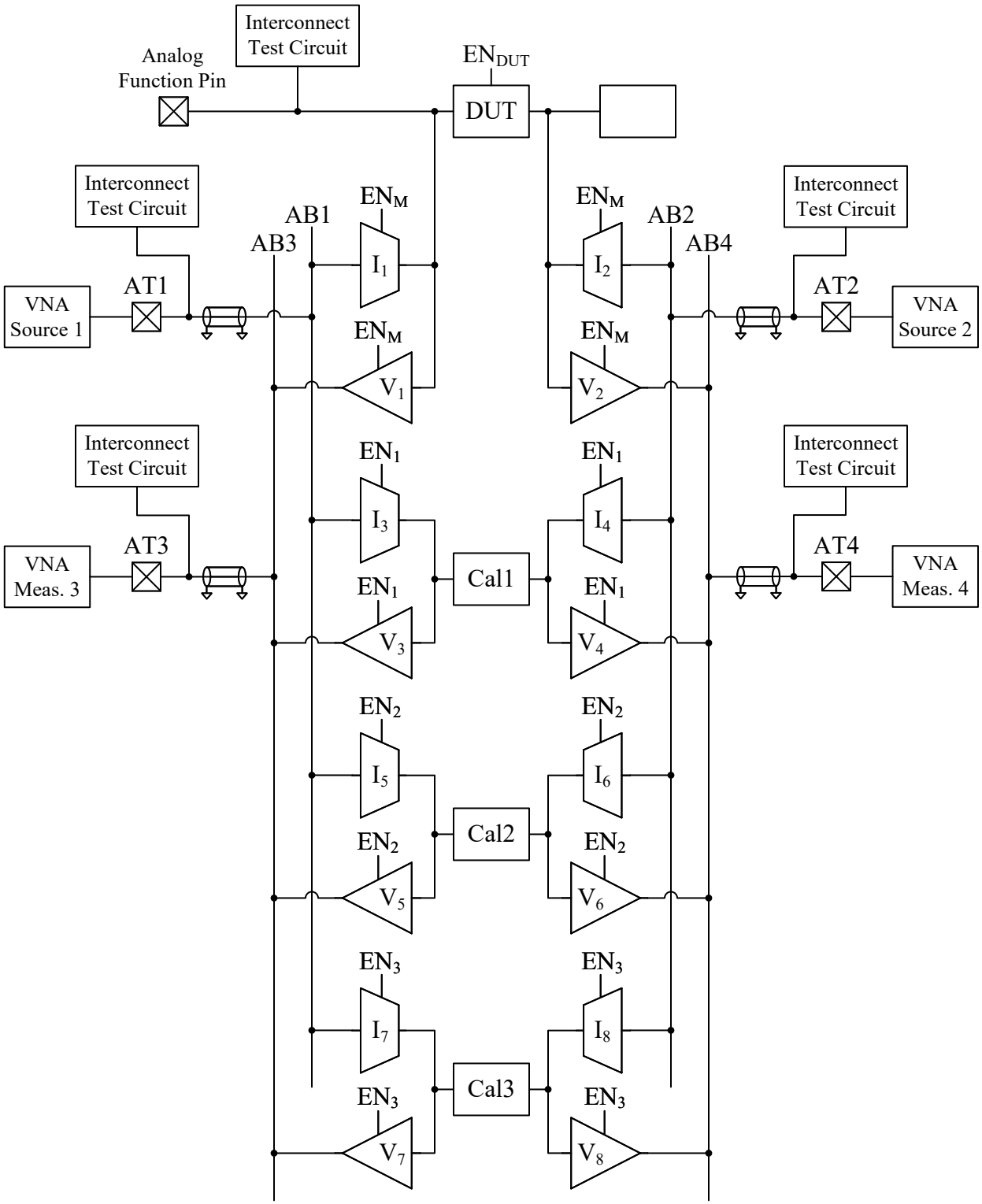


Figure 3.1: Proposed 4-port analog test bus.

relay the test signal off-chip (VNA Meas. 3 and 4). Near the test ports are the Interconnect Test Circuit blocks which would perform basic port connection testing as in 1149.4, although they are not used during test bus measurements. Transmission lines between the test ports and buffers represent parasitic elements from long traces/interconnects that are accounted for during calibration.

The Cal1, Cal2, and Cal3 blocks represent three different calibration references much like those included in a typical VNA calibration. The exact internals of the calibration references will be discussed in Section 4.3. The ability of the voltage and current buffers to switch on or off is labeled with an enable pin at the top of the symbols. The three calibration references create three different zones controlled through EN_1, EN_2, and EN_3.

EN_M controls the test bus connection to the DUT. When switched off, the buffers should have little influence on the performance of the DUT. An optional enable pin, EN_{DUT}, is included to turn on and off the DUT when the test bus is in calibration mode. Large signals from an active DUT may leak through the buffers and contaminate the calibration.

3.1.1 High-Frequency Errors

Given ideal buffers and interconnects, both the 4-port and 1149.4 test buses can accurately measure an analog circuit's performance. As has been discussed repeatedly, the question becomes: What is the maximum frequency of the test bus and can calibration extend the bandwidth? Any test bus has a frequency limit at which it stops being accurate due to high-frequency effects such as parasitic capacitance, which starts to attenuate and shift the signal through the test bus.

To more closely analyze the errors, Fig. 3.2 (a) shows a detail of the signal path from the DUT output to the test port. The gain transfer function has a low-pass characteristic, where the gain decreases at higher frequencies past the cutoff. In addition, the buffers have input and output impedances that start to change as frequencies increase. Focusing on the DUT and V_3 connection, if Z_{od} and Z_{i3} have comparable magnitudes a voltage divider effect

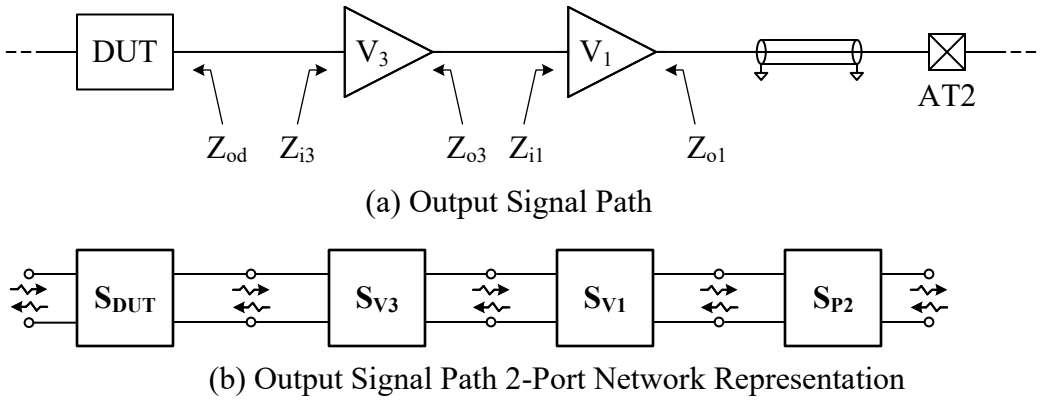


Figure 3.2: Output signal path represented with (a) circuit schematic and (b) general 2-port networks.

will affect the gain.

Fig. 3.2 (a) also shows a transmission line and port symbol to represent the long interconnect and chip pad. The parasitic elements of these components become significant at high frequencies with the interconnect becoming an electrically long device. This could produce reflections causing phase shifts across the device.

This more detailed look at the errors that can affect test bus measurements begins to explain the complicated factors that impact measurements. It by no means includes every high-frequency error that could occur. One important effect to emphasize is the fact that not only does gain across the test bus signal path decrease, there is an interaction between the DUT and buffer input/output impedances. Given how complicated and intertwined high-frequency circuits are, it makes sense why S-parameters are a popular way to represent RF circuits. It is more convenient to represent circuit blocks with generic S-parameter 2-port networks. The 2-port model gives a generalized model of the system that does not assume anything about its performance. Continuing that logic, Fig. 3.2 (b) shows the test bus signal path replaced with S-parameter 2-port networks. Conceptualizing the test bus as a group of generic 2-port networks helps explain why the 4-port test bus is structured the way it is, as will be discussed.

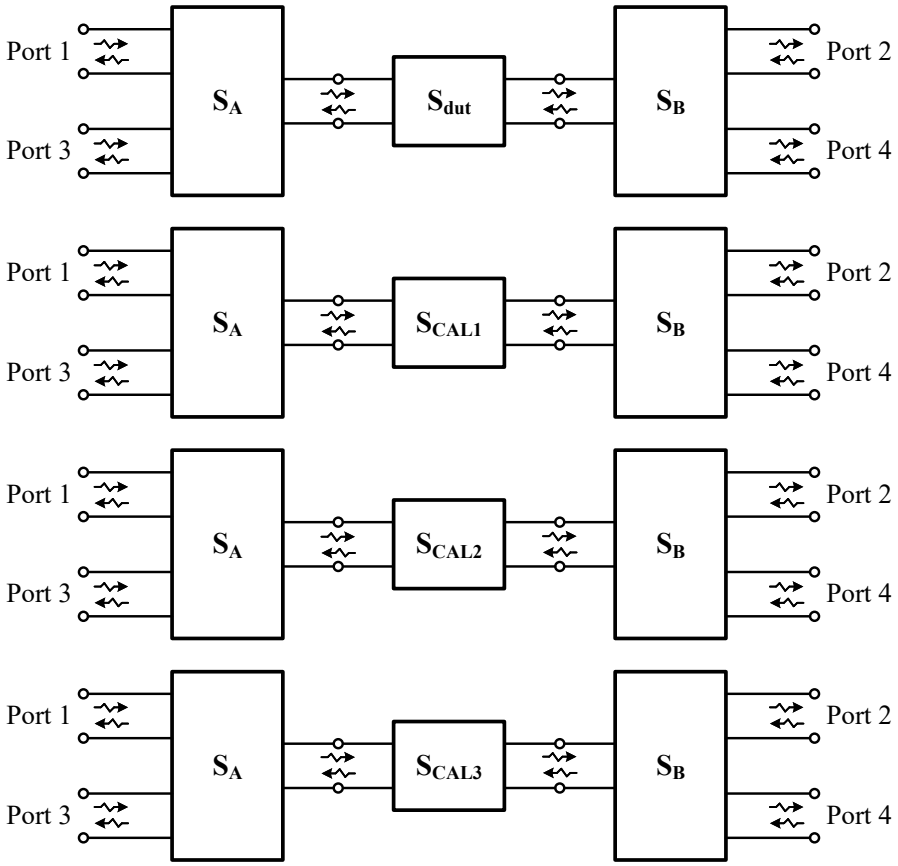


Figure 3.3: 4-port test bus calibration model with 3-port input and output error blocks.

3.1.2 Structural Requirement to Enable Calibration

The structure of the 4-port test bus is informed by the requirement to fit the VNA calibration model. The S-parameter network model of the calibration system is shown in Fig. 3.3. As discussed in Section 2.4.1, a common VNA error model consists of two separate error blocks, one at the input of the DUT and a second at the output. The 4-port test bus conforms to the two error block system. The only difference is that the 4-port test bus error blocks contain an additional port making then 3-port networks. Exactly how the error terms of the error blocks are calculated will be discussed later in Section 4.2. For now, the high-level idea of VNA calibration remains. The 3 calibration references are used to calculated the contents of the error blocks to then be able to de-embed their effects from a DUT measurement.

The error block calibration model requires that the test bus components (buffers and ports) stay consistent between each measurement of the DUT and calibration references. Knowing the calibration model provides context for the structural differences between the 4-port and 1149.4 test buses, which are examined further in the following section.

3.2 4-Port and 1149.4 Test Bus Structural Comparison

Compared to the 1149.4 schematic as shown previously in Fig. 2.2, the 4-port test bus has one fewer buffer in the signal path and two additional test ports/buses. These differences are necessary to facilitate the VNA calibration approach and increase the frequency bandwidth.

In 1149.4, a buffer is placed between the test port and the test bus to give the option to disconnect the port from the bus. This buffer is part of the test bus interface circuit, which in a switch-based implementation allows both test ports and test buses to be connected interchangeably with each other. This is not included in a buffer-based implementation because the buffers are unidirectional. Making the signal cross 4 buffers increases the capacitance on the path and reduces its bandwidth. Additionally, the task of disconnecting the test bus and port is not strictly necessary, and a similar effect can be achieved by turning off all buffers connected to the bus. The proposed 4-port test bus removes this extra buffer for these reasons and directly connects the test port to the bus.

Adding two additional test ports and buses increases the robustness of the design and the accuracy of the calibration. The dedicated input and output ports avoid having to share resources and produce changing load conditions. For the proposed 4-port test bus, all buffers are turned on and remain turned on for the duration of the measurements. 1149.4 requires turning on or off different buffers to set up the different measurements. This is because the output signals need to share the output bus and port.

Fig. 3.4 shows the 4-port and 1149.4 test buses in 2-port network form for two different measurements. For an 1149.4 forward through measurement, I_1, I_2, V_3, and V_1 are turned on.

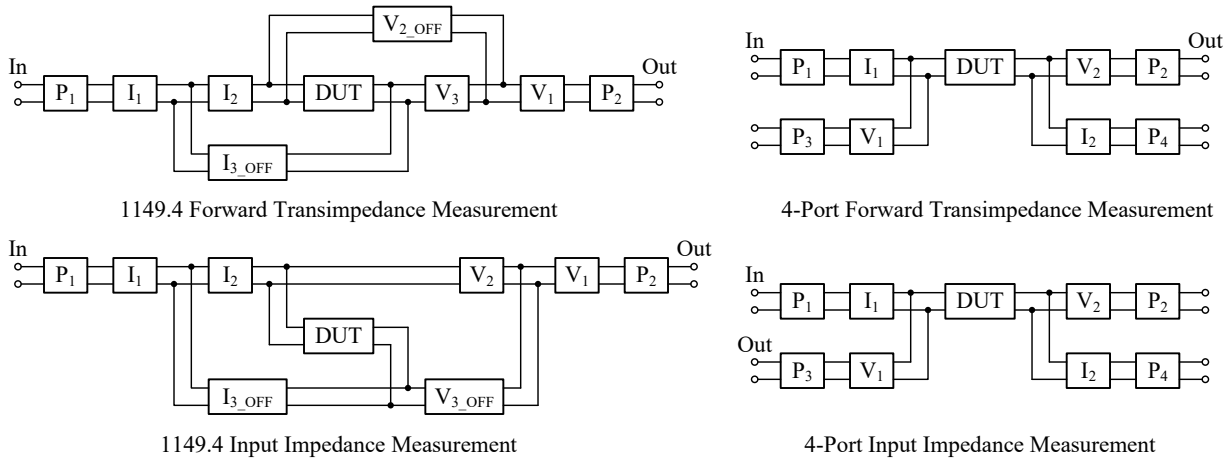


Figure 3.4: 2-port network diagrams comparing the 1149.4 and 4-port test buses measuring transimpedance and input impedance.

For an 1149.4 forward reflection measurement, I_1, I_2, V_2, and V_1 are turned on. Therefore, the first error box changes from including a turned off V_2 to a turned on V_2 passing the signal. The 1149.4 error boxes are not consistent and do not meet the VNA calibration requirement. That contrasts with the 4-port test bus consistent symmetry between measurements.

An additional consideration for 1149.4, if any of the buffers while turned off have a noticeable amount of leakage signal through, measurement will be severely inaccurate. This again changes the error box and corrupts the measured signal. The 4-port test bus does not rely on a single turned off buffer to block signals and instead gives dedicated paths for each.

3.2.1 Highlighting the High-Frequency Limitations

To illustrate the performance of the 4-port and 1149.4 test bus, a numerical example is presented in this section. The example highlights the difference between low-frequency measurements with close-to-ideal components and high-frequency measurements with errors present in the components.

In this section only simple direct measurements with the test bus are covered. Fig. 3.5 shows the simulation setup of both test buses. Consistent with the rest of this thesis, the target is the DUT transimpedance. Therefore, a current source is used to apply the input

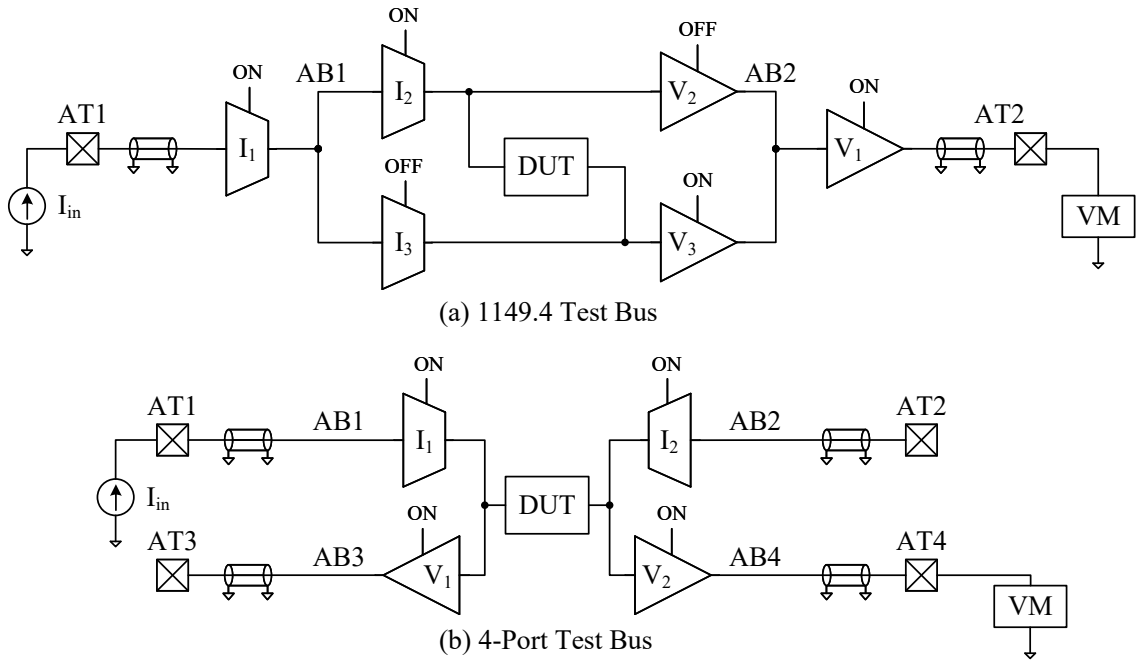


Figure 3.5: (a) IEEE 1149.4 and (b) 4-port test bus setup for direct DUT measurement.

signal at the input port and the output voltage is read at the output port with a voltmeter.

The performance parameters of the current buffers, voltage buffers, DUT, and transmission lines are captured in Tables 3.1 and 3.2. Each component has two sets of performance parameters, one for low-frequency ideal and one for high-frequency with errors. This allows one to easily evaluate the test bus accuracy between low-frequency and high-frequency measurements.

The resulting test bus measured transimpedance is summarized in Table 3.3. With the low-frequency ideal components, both the 4-port and 1149.4 test buses can accurately measure the DUT transimpedance. However, the high-frequency test gives inaccurate results, though the amount of deviation is reduced with the 4-port test bus.

Clearly, calibration is required to extract a more accurate measurement of the DUT. This numerical example will be continued later in Section 4.4 applying the calibration algorithm.

Table 3.1: Current and voltage buffer component values used for the example.

Component		*Gain*	Z_{in}	Z_{out}	Z_{leak}
Current Buffer	Ideal Low-Freq.	1 A/A	10 Ω	20 kΩ	∞ Ω
	High-Freq. Errors	0.98 A/A	30 Ω	2 kΩ	7 kΩ
Voltage Buffer	Ideal Low-Freq.	1 V/V	30 kΩ	100 Ω	∞ Ω
	High-Freq. Errors	0.92 V/V	2 kΩ	90 Ω	7 kΩ
DUT		1000 V/A	30 Ω	60 Ω	∞ Ω

Table 3.2: Transmission line component values used for the example.

Component		Z_0	Normalized Length
Transmission Line	Ideal Low-Freq.	N/A	0
	High-Freq. Errors	50	0.25

Table 3.3: Directly measured (no calibration) DUT transimpedance results through the 4-port and 1149.4 test bus.

Test Bus		**Gain**	**Error**
Reference		1000 V/A	-
Low-Freq	1149.4	991.1 V/A	0.89 %
	4-Port	989.0 V/A	1.1 %
High-Freq	1149.4	619.1 V/A	38.09 %
	4-Port	681.2 V/A	31.88 %

3.3 2-Port Test Bus

The main downside of the 4-port test bus over 1149.4 is the additional test ports. Any additional ports taken away from an IC's main functionality and moved to be exclusively for testing is expensive. There are a limited number of ports available, and each is carefully considered.

A simplification of the 4-port test bus is to reduce the number of test ports to a 2-port test bus, but this depends on specific buffer conditions to be met. Fig. 3.6 shows the high-level 2-port test bus structure, which largely follows the 4-port test bus description except

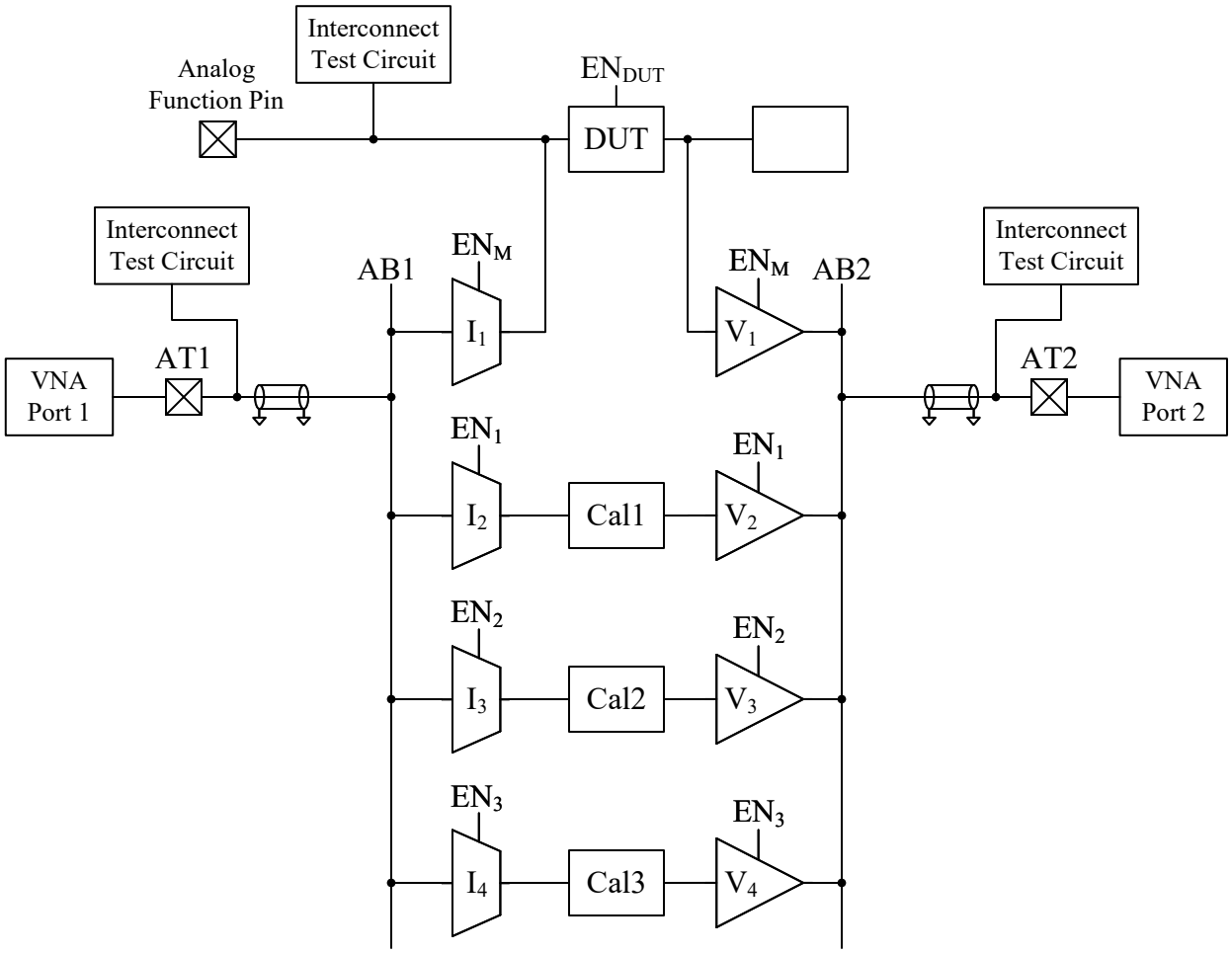


Figure 3.6: Proposed 2-port analog test bus.

that half the test ports, buses, and buffers have been removed. The 2-port test bus has two test ports (AT1 and AT2) and two internal test buses (AB1 and AB2) each connected to a port of a 2-port VNA. Branching off AB1 are the current buffers and branching off AB2 are the voltage buffers.

The 2-port test bus calibration model is the same error block model used for the 4-port test bus and typical VNA calibration. The only difference being that the 4-port test bus 3-port error blocks have been replaced with the normal 2-port error blocks. The 2-port calibration model is repeated here in Fig. 3.7. Conforming to the calibration model is a requirement of the 2-port test bus structure to support accurate calibration.

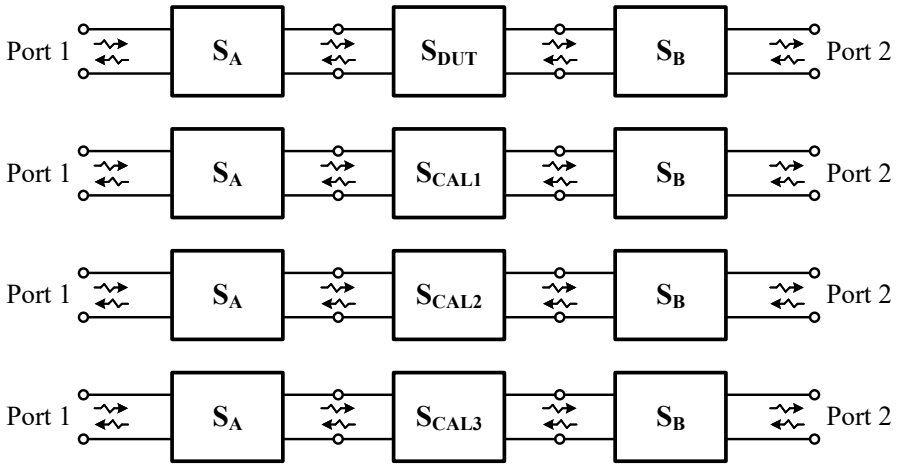


Figure 3.7: 2-port test bus calibration model with 2-port input and output error blocks.

3.4 2-Port, 4-Port, and 1149.4 Test Bus Structural Comparison

The 2-port test bus removes all unnecessary buffers to have the bare minimum to support a test bus. Only a single current buffer is used to apply a signal to the input of the DUT. Then a single voltage buffer is used to read the output of the DUT.

The buffers placed between the test port and bus in 1149.4 are removed for the same reasons as for the 4-port test bus. One does not need to be able to disconnect the port and bus. A similar effect can be achieved by turning off all buffers connected to the bus.

The ability to apply and read signals from both the input and output of the DUT has also been removed. Removing this ability greatly simplifies the test bus and reduces the number of components connected to the bus. Simplifying the test bus increases its potential maximum frequency by reducing the number of parasitic components. The 2-port test bus aims to provide the most direct way to apply a stimulus and read its result.

The 2-port test bus also improves on the 4-port test bus by cutting the number of ports in half to match 1149.4. This comes at the cost of requiring specific conditions on the buffers to allow an accurate calibration.

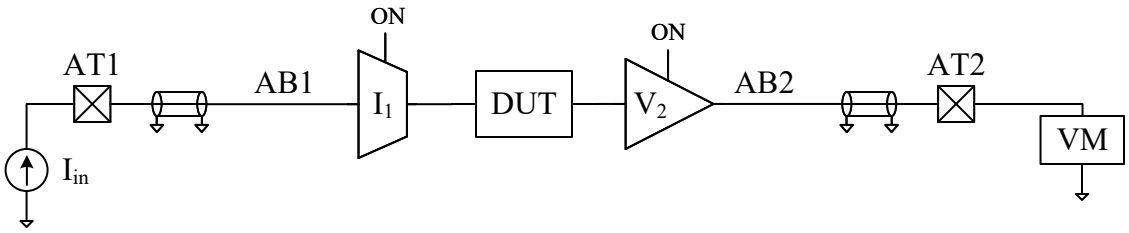


Figure 3.8: 2-port test bus setup for direct DUT measurement.

Table 3.4: Directly measured (no calibration) DUT transimpedance results through the 2-port, 4-port, and 1149.4 test bus.

Test Bus		**Gain**	**Error**
Reference		1000 V/A	-
Low-Freq	1149.4	991.1 V/A	0.89 %
	4-Port	989.0 V/A	1.1 %
	2-Port	995.0 V/A	0.5 %
High-Freq	1149.4	619.1 V/A	38.09 %
	4-Port	681.2 V/A	31.88 %
	2-Port	741.5 V/A	25.85 %

3.4.1 Highlighting the High-Frequency Limitations

To further establish the impact high-frequency errors have on the 2-port test bus accuracy, the same numerical example as that of the 4-port test bus is performed. Fig. 3.8 shows the simulation setup of the test bus to measure the DUT transimpedance. Each component of the test bus is implemented with the same high-level parameter used in the 4-port example summarized in Tables 3.1 and 3.2.

The results of the simulation are captured in Table 3.4 and show that the 2-port test bus behaves the same as the 4-port and 1149.4 test bus. The ideal low-frequency components result in an accurate transimpedance value measured from the test bus. The high-frequency component simulation is less accurate due to errors in the components. This is still only a preliminary example that will continue in Section 4.5.1 by applying the calibration algorithm.

3.5 Summary

The proposed analog test bus uses a combination of techniques from the 1149.4 test bus and normal VNA measurements to create a high-frequency test bus. To apply VNA-style calibration to the proposed test bust, the structure must conform to the error block calibration model. 4-port and 2-port variations of the proposed test bus are described, which are based on the same current and voltage buffers. The structural differences between the 1149.4, 4-port, and 2-port test buses are highlighted using a simulated numerical example. All test buses accurately measure a transimpedance DUT when the test bus behaves ideally at low frequencies. At high frequencies with errors present in the test buses, both structures fail to measure the DUT accurately. Advanced calibration is needed to account for the complicated errors created by the buffers and their interface with the DUT.

Chapter 4

Enhancing High-Frequency Measurement Accuracy with Calibration

The calibration algorithm for the proposed 4-port and 2-port test buses is based on the algorithm presented previously in Section 2.4.1 of the literature review. The calibration algorithm uses measurements of the on-chip calibration references to calculate the errors and de-embed the performance of the DUT. The 2-port test bus can directly apply the standard procedure, while the 4-port test bus needs a conversion to work. The most important part of the calibration algorithm is the design of the on-chip calibration references.

This chapter starts by documenting the conversion from the S-parameters to voltage and current. Then the 4-port test bus conversion is presented, allowing it to fit in the calibration algorithm. A detailed section on the calibration references is then presented. With all the background on the proposed test buses established, a numerical example is presented. Minor sections are added at the end to briefly discuss the 2-port test bus reverse signal requirement and error block matching.

4.1 Converting S-Parameters to Voltage and Current

After measuring and calibrating S-parameter measurements in RF and high-frequency applications, the results are typically kept in S-parameters or converted to power gain. This simply depends on what information is desired about the DUT and most RF and high-frequency applications want S-parameters or power measurements. The proposed test buses can also be aimed at applications where one is more interested in gain in terms of voltage and current, which is the application investigated in this thesis. The author could not find voltage, current, or transimpedance gain clearly stated in terms of VNA measured S-parameters and therefore this section steps through the derivation of the gain equations from S-parameter fundamentals.

After determining the DUT S-parameters, they can be converted to circuit values such as voltage gain, current gain, and transimpedance gain through an additional calculation step. A general derivation is given to apply any possible DUT. Fig. 4.1 shows a general signal flow of a 2-port network with a source and load impedance where

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S - Z_0} \qquad \Gamma_L = \frac{Z_L - Z_0}{Z_L - Z_0}. \tag{4.1}$$

Inspecting the signal flow diagram in Fig. 4.1 (b), four equations can be written to relate the nodes and S-parameters

$$\begin{aligned} b_1 &= s_{11}a_1 + s_{12}a_2 \qquad & a_1 &= \Gamma_S b_1 + b_S \\ b_2 &= s_{21}a_1 + s_{22}a_2 \qquad & a_2 &= \Gamma_L b_2. \end{aligned} \tag{4.2}$$

From the definition of S-parameters, the voltage and current are related to the forward and reflected waves according to [15]

$$V = \sqrt{Z_0}(a + b) \tag{4.3}$$

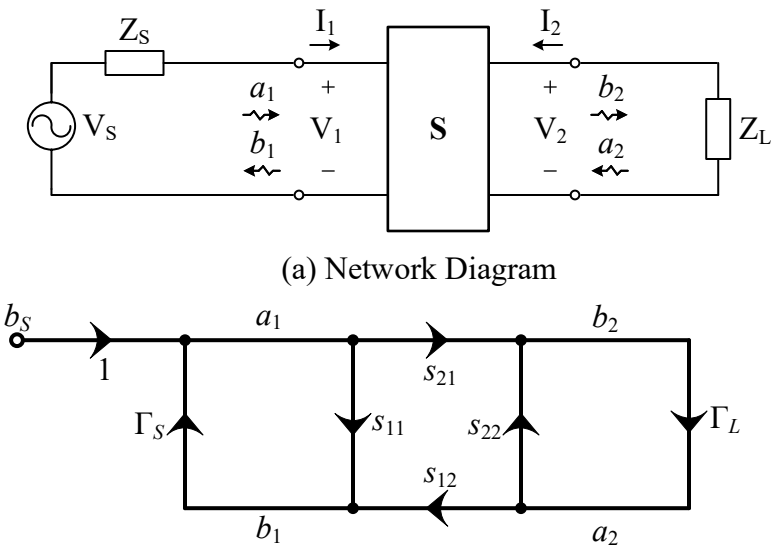


Figure 4.1: General (a) 2-port network with load and source impedance represented with a (b) signal flow diagram.

$$I = \frac{1}{\sqrt{Z_0}}(a - b). \tag{4.4}$$

The transimpedance, voltage, and current gain from node 1 to 2 are therefore

$$Z_T = \frac{V_2}{I_1} = Z_0 \frac{(a_2 + b_2)}{(a_1 - b_1)} \tag{4.5}$$

$$A_V = \frac{V_2}{V_1} = \frac{(a_2 + b_2)}{(a_1 + b_1)} \tag{4.6}$$

$$A_I = \frac{I_2}{I_1} = \frac{(a_2 - b_2)}{(a_1 - b_1)}. \tag{4.7}$$

Using (4.2), the gain equations can be rearranged to be in terms of S-parameters and the load reflection giving the final equations

$$Z_T = \frac{Z_0 s_{21}(\Gamma_L + 1)}{1 - s_{11} - s_{22}\Gamma_L + s_{11}s_{22}\Gamma_L - s_{12}s_{21}\Gamma_L} \tag{4.8}$$

$$A_V = \frac{s_{21}(\Gamma_L + 1)}{1 + s_{11} - s_{22}\Gamma_L - s_{11}s_{22}\Gamma_L + s_{12}s_{21}\Gamma_L} \tag{4.9}$$

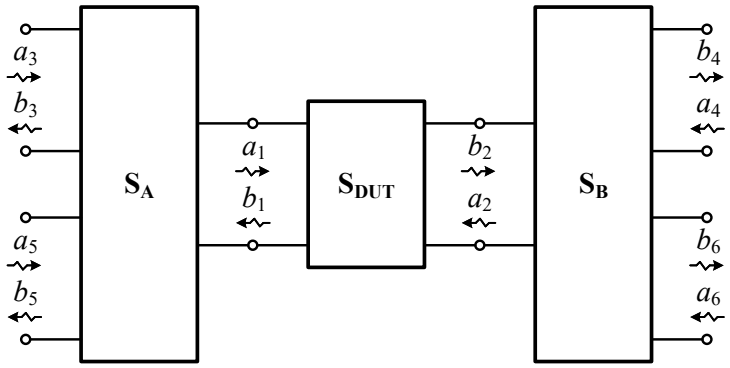


Figure 4.2: Network diagram of the 4-port test bus created with 2-Port and 3-Port networks.

$$A_I = \frac{s_{21}(\Gamma_L - 1)}{1 - s_{11} - s_{22}\Gamma_L + s_{11}s_{22}\Gamma_L - s_{12}s_{21}\Gamma_L}. \tag{4.10}$$

4.2 4-Port Test Bus to 2-Port Conversion

The 4-port test bus can be modeled with a combination of 2-port and 3-port networks as shown in Fig. 4.2. For example, port 3 is the current buffer input, port 5 is the voltage buffer output, and port 1 is the input to the DUT.

A signal flow diagram of the 4-port test bus model is shown in Fig. 4.3 and contains 18 error parameters in total. Solving for all 18 error parameters would require prohibitively more calibration references and measurements compared to the typical VNA calibration 8-term error model presented in Section 2.4. The model can be simplified by recognizing that not all error parameters are used or necessary to extract from the DUT measurement. Firstly, no signal is applied to port 5 and therefore $a_5 = a_6 = 0$. Secondly, the transmitted waves b_3 and b_4 do not provide any new information not already contributed by b_5 and b_6. Removing those waves and the attached error parameters results in the simplified signal flow diagram shown in Fig. 4.4. The simplified signal flow model has 8 error parameters and can now be used with the established 8-term calibration procedure.

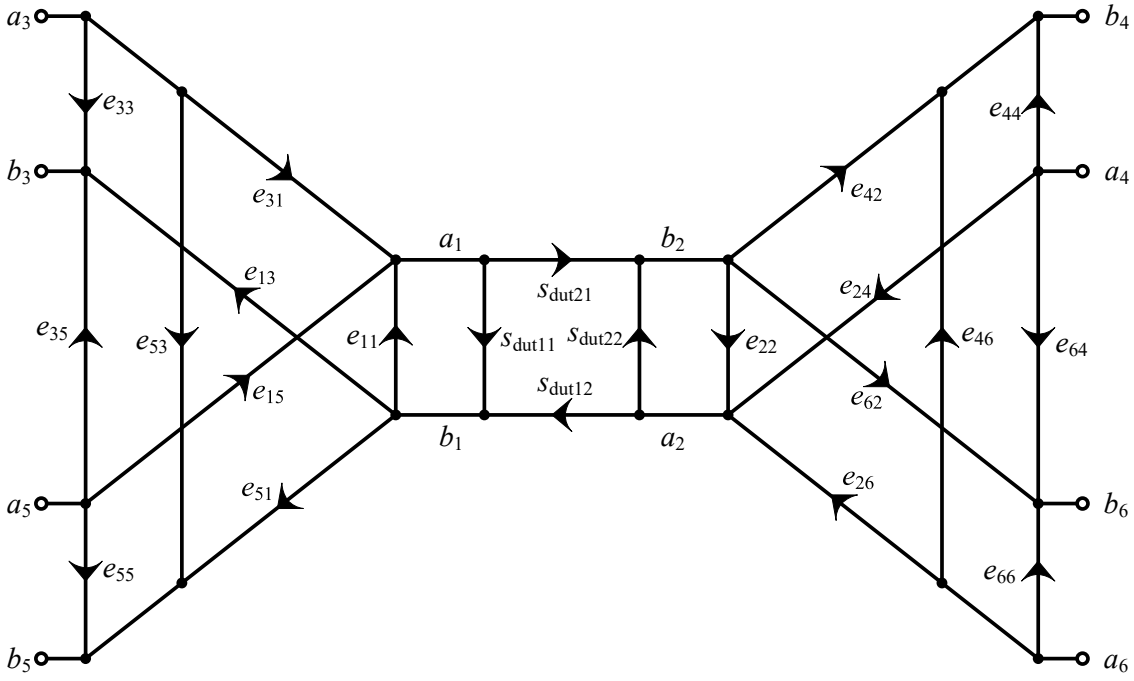


Figure 4.3: Signal flow diagram of the complete 4-port test bus.

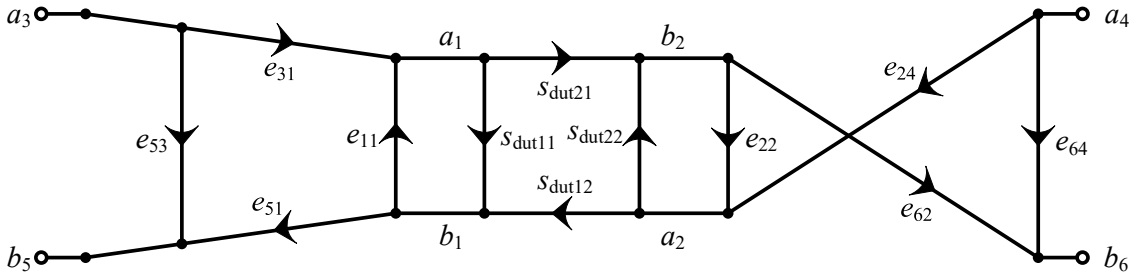


Figure 4.4: Signal flow diagram of the 4-port test bus simplified to eight error terms by setting $a_5 = a_6 = 0$.

4.3 Calibration References

Integrating calibration references with the test bus comes with unique requirements not seen for typical VNA calibration references. Therefore, a different approach is needed for the test bus. Existing calibration references were discussed in Section 2.4.2 of the literature review. Upon first glance, existing on-chip or electronic calibration references may work with the test bus.

The two main on-chip calibration reference, TRL and LRRM, as introduced in Section

2.4.2, both use a transmission line standard. This standard is fundamentally an electrically long device that occupies a lot of area. Even at mmWave frequencies, the transmission line length needs to be tens of millimeters long, and that is a significant area on-chip. Therefore, these large references are not suitable to be built along with the test bus.

References between buffers must ensure that the DC bias voltage is maintained. The side of both buffers facing the reference is high-impedance and not typically capable of establishing the DC voltage. A short or open standard will affect the DC biasing of the buffers. In the best case, this only shifts the performance of the buffers. In the worst case, it renders the buffer inoperable.

Electronic calibration references, such as the CMOS one presented by Chien and Niknejad [42], could feasibly integrate well with the test bus. Varying the gate voltage of the single transistor would create different references. These CMOS electronic calibration standards rely on an off-chip DC voltage applied through the probe. This is not possible to achieve using the proposed test bus buffers. There is no input voltage buffer to pass on the biasing voltage, only input current buffers.

Therefore, the requirements of the calibration references to be integrated in the proposed test bus are as follows:

- Sets the DC voltage biasing point of the buffer. Ideally, at a voltage similar to the one set by the DUT.
- Created with physically small components that minimize the occupied silicon area.
- Either has intrinsically known S-parameters or the S-parameters can be characterized using a low-frequency measurement.
- Stable S-parameters across the frequency range of interest.

The calibration references identified that fulfill the outline requirements are load resistors as shown in Fig. 4.5. The first two standards are through-type standards and the third is a reflect-type standard similar to that of the TRL [23]. By knowing the resistance, the 2-port

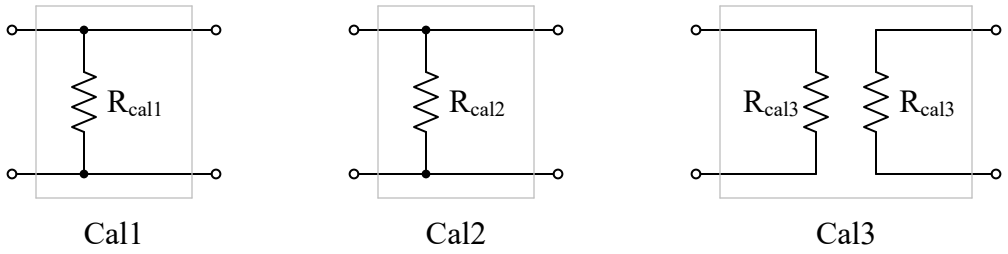


Figure 4.5: Calibration references integrated within the proposed test bus.

S-parameters of the references are known. The load resistors in Fig. 4.5 are only the small signal behavior. Exactly how they are implemented can vary, depending on the application. As will be seen in the coming chapters, the references are implemented two different ways between the PCB experiment and BiCMOS simulation.

4.3.1 Reference Resistor Low-Frequency Measurement

The value of the reference resistors needs not be known beforehand and can be measured with a low-frequency test signal assuming that the voltage and current buffers are ideal at low frequencies, as shown in Fig. 4.6. A known current is applied to the input that travels through the current buffer and resistor, generating a voltage that is then repeated on the output port by the voltage buffer.

The current buffer to load resistor to voltage buffer is a unique arrangement that allows the characterization of the resistor. One needs a current and voltage buffer to be able to measure the resistance. The unique arrangement becomes obvious if one tries to develop a way with only two voltage buffers or two current buffers. It is difficult to know both the current and the voltage to calculate the resistance. A load resistor versus a series resistor is also an important subtly. A series resistor also has no way to extract both voltage and current. The reason why measuring the on-chip resistance requires a specific setup is because of the need to obtain an accurate measurement using off-chip equipment.

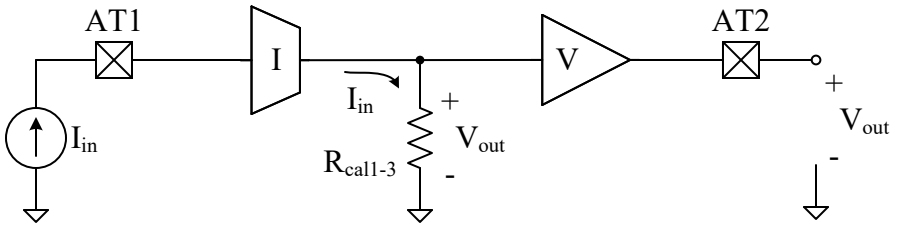


Figure 4.6: R_{cal1-3} low frequency measurement setup equivalent circuit.

4.3.2 Derivation of Resistor S-Parameters

After the resistance value of the calibration resistor is known, their S-parameters can be directly calculated. This section steps through the conversion of resistance to S-parameter. The S-parameter are needed because that is the form used in the main calibration system of equations.

One way to derive the exact S-parameter is to write the waves in terms of the voltages and resistors. First by definition, the incident wave is equal to half the source voltage

$$a_1 = \frac{1}{2}\frac{V_s}{\sqrt{Z_0}}. \tag{4.11}$$

The reflected wave is then

$$b_1 = \frac{V_1}{\sqrt{Z_0}} - a_1 \tag{4.12}$$

and the voltage at the resistor is a voltage divider of the source

$$V_1 = V_s \frac{R//Z_0}{Z_0 + R//Z_0}. \tag{4.13}$$

Using (4.11), (4.12), and (4.13) and the definition of s_{11}, s_{11} can be written in terms of the reference resistor

$$s_{11} = \frac{b_1}{a_1} = \frac{\frac{V_1}{\sqrt{Z_0}} - a_1}{a_1} = \frac{-Z_0}{2R + Z_0}. \tag{4.14}$$

The same is true for s_{21} written in terms of the reference resistor

$$s_{21} = \frac{b_2}{a_1} = \frac{\frac{V_2}{\sqrt{Z_0}} - a_2}{a_1} = \frac{2R}{2R + Z_0}. \tag{4.15}$$

The reference resistors are symmetrical, so s_{22} and s_{12} are the same as s_{11} and s_{21}, respectively. Knowing the four S-parameters, the calibration reference S-parameter matrices can be populated. Cal1 and Cal2 introduced in Fig. 4.5 therefore have the complete S-parameter matrices

$$\mathbf{S_{CAL1}} = \frac{1}{2R_{cal1} + Z_0} \cdot \begin{bmatrix} -Z_0 & 2R_{cal1} \\ 2R_{cal1} & -Z_0 \end{bmatrix} \tag{4.16}$$

$$\mathbf{S_{CAL2}} = \frac{1}{2R_{cal2} + Z_0} \cdot \begin{bmatrix} -Z_0 & 2R_{cal2} \\ 2R_{cal2} & -Z_0 \end{bmatrix} \tag{4.17}$$

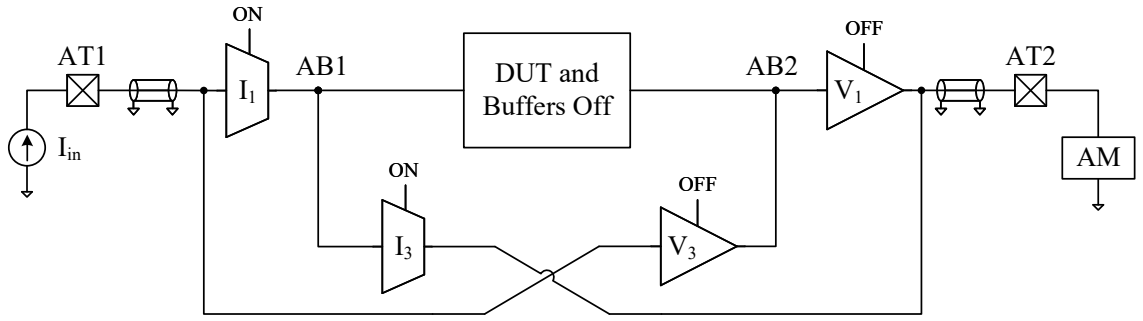
where R_{cal1} and R_{cal2} are the resistor values. Cal3's S-parameter matrix, being two simple load resistors without a through connection, is the classic impedance to wave reflection equation

$$\mathbf{S_{CAL3}} = \frac{R_{cal3} - Z_0}{R_{cal3} + Z_0} \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{4.18}$$

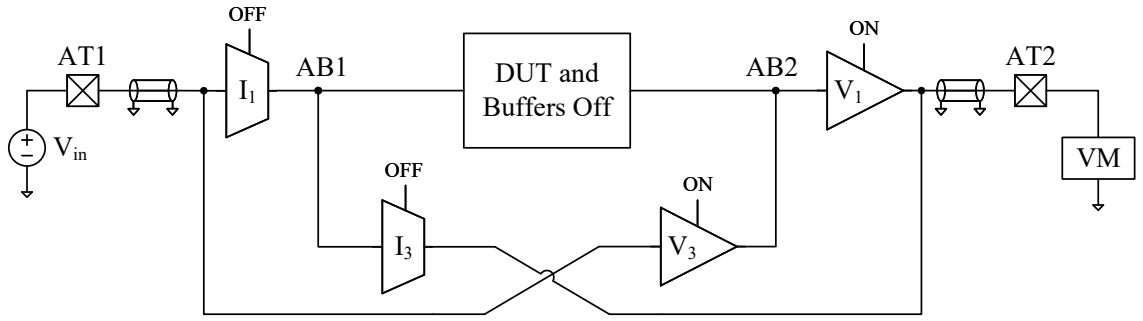
where R_{cal3} is the resistor value.

4.4 Comparison of 4-Port and 1149.4 Test Bus

To help illustrate the 4-port test bus calibration performance, a numerical example is presented and compared to a calibrated 1149.4 measurement. This example is a continuation of the one introduced in the previous chapter in Section 3.2.1, where test bus measurements are performed without calibration. For consistency, the same component parameters for the buffers, transmission lines, and DUT are used that were captured in Tables 3.1 and 3.2. Two sets of component parameters are used again, one with ideal low-frequency performance and the other with high-frequency performance errors, to demonstrate the differences between the test buses.



(a) 1149.4 Current Buffer Calibration Measurement Setup



(b) 1149.4 Voltage Buffer Calibration Measurement Setup

Figure 4.7: 1149.4 test bus calibration measurement setup of both the (a) current buffers and (b) voltage buffers.

4.4.1 1149.4 Test Bus Example

IEEE 1149.4 contains a simple calibration mechanism that uses extra current and voltage buffers to bypass directly to the opposite test port, as discussed in the literature review in Section 2.2.2. Fig. 4.7 shows the simulation setup to measure the gain of the current and voltage buffers. The gain is used as a correction factor for the test bus measured DUT transimpedance.

First, the 1149.4 test bus constructed out of the ideal low-frequency component parameters is tested. Measurement of the current and voltage buffer calibration path gain gives

$$A_I = \frac{I_{cal\_out}}{I_{cal\_in}} = 0.9994\ A/A \qquad A_V = \frac{V_{cal\_out}}{V_{cal\_in}} = 0.9966\ V/V \tag{4.19}$$

and then measuring the gain of the DUT through the test bus gives

$$Z_M = \frac{V_M}{I_M} = 991.0533\ V/A. \tag{4.20}$$

The de-embedded DUT transimpedance can then be solve for by

$$Z_{DUT} = \frac{Z_M}{A_I \cdot A_V} = 995.1024\ V/A. \tag{4.21}$$

These steps were repeated again, but with the 1149.4 test bus constructed out of the high-frequency error components. The results are captured in Table 4.2.

4.4.2 4-Port Test Bus Example

To perform a measurement using the 4-port test bus, the ports are each connected to their own VNA port. Fig. 4.8 shows the simplified simulation setup with the 4-port VNA. The schematic has been generalized to save space. The measurement setup between the DUT and calibration references is the same and is logically grouped together. The schematic only shows the buffers turned on during a measurement, and not the turned off buffers connected to the test buses.

The calibration reference parameters are captured in Table 4.1. Round resistor values were chosen for convenience and assumed to be known without the need for a low-frequency characterization. Using the resistance-to-S-parameter conversions (4.16), (4.17), and (4.18) derived in Section 4.3.2, the resulting calibration reference S-parameters are

$$\mathbf{S_{CAL1}} = \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} = \begin{bmatrix} -0.2 & 0.8 \\ 0.8 & -0.2 \end{bmatrix} \qquad \mathbf{S_{CAL2}} = \begin{bmatrix} u_{11} & u_{12} \\ u_{21} & u_{22} \end{bmatrix} = \begin{bmatrix} -0.1111 & 0.8889 \\ 0.8889 & -0.1111 \end{bmatrix}$$

$$\mathbf{S_{CAL3}} = \begin{bmatrix} w_{11} & w_{12} \\ w_{21} & w_{22} \end{bmatrix} = \begin{bmatrix} 0.6 & 0 \\ 0 & 0.6 \end{bmatrix} \tag{4.22}$$

Table 4.1: Calibration references (Cal1, Cal2, and Cal3) component parameters used in the example.

Parameter	**Cal1**	**Cal2**	**Cal3**
R_{cal}	200 Ω	100 Ω	100 Ω

First, each calibration reference is measured individually. As for any measurement using the 4-port, only the S-parameters between the input and output ports are saved, as was shown in the 4-port to 2-port conversion in Section 4.2. Using the Cal1 measurement as an example, the 4-port S-parameters saved to construct the 2-port S-parameters are

$$\mathbf{S_{M\_cal1}} = \begin{bmatrix} s_{31} & s_{32} \\ s_{41} & s_{42} \end{bmatrix} = \begin{bmatrix} k_{m11} & k_{m12} \\ k_{m21} & k_{m22} \end{bmatrix} = \begin{bmatrix} -1.0678 & -1.0678 \\ -1.0678 & -1.0678 \end{bmatrix} \tag{4.23}$$

where $\mathbf{S_{M\_cal1}}$ is the test bus measured S-parameter matrix of Cal1, s_{31} is the transmission from VNA port 1 to 3, s_{32} is the transmission from VNA port 2 to 3, s_{41} is the transmission from VNA port 1 to 4, and s_{42} is the transmission from VNA port 2 to 4. Repeating the measurement for Cal2 and Cal3 gives

$$\begin{aligned} \mathbf{S_{M\_cal2}} &= \begin{bmatrix} u_{m11} & u_{m12} \\ u_{m21} & u_{m22} \end{bmatrix} = \begin{bmatrix} -2.1011 & -2.1011 \\ -2.1011 & -2.1011 \end{bmatrix} \\ \mathbf{S_{M\_cal3}} &= \begin{bmatrix} w_{m11} & w_{m12} \\ w_{m21} & w_{m22} \end{bmatrix} = \begin{bmatrix} -2.1355 & 0 \\ 0 & -2.1355 \end{bmatrix} \end{aligned} \tag{4.24}$$

where $\mathbf{S_{M\_cal2}}$ and $\mathbf{S_{M\_cal3}}$ are the test bus measured S-parameter matrix of Cal2 and Cal3, respectively. Finally, the measurement of the DUT gives

$$\mathbf{S_{M\_dut}} = \begin{bmatrix} s_{m11} & s_{m12} \\ s_{m21} & s_{m22} \end{bmatrix} = \begin{bmatrix} -0.3357 & 0 \\ -10.7373 & -1.0873 \end{bmatrix} \tag{4.25}$$

where $\mathbf{S_{M\_dut}}$ is the test bus measured S-parameter matrix of the DUT. With all the test bus measurements collected, the next step is to apply the calibration algorithm and de-embed the DUT.

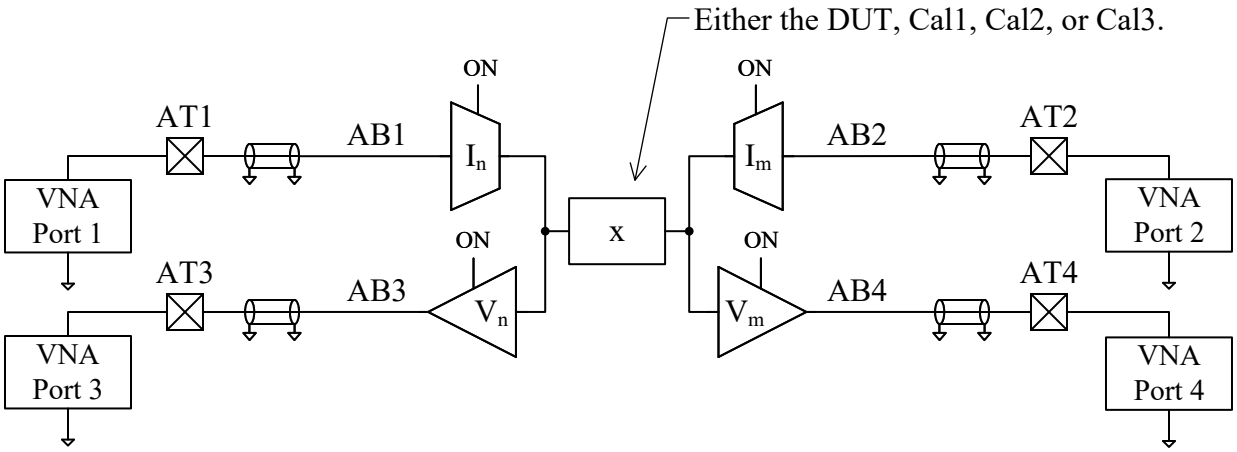


Figure 4.8: General 4-port test bus measurement setup with the center block switching between the DUT, Cal1, Cal2, and Cal3.

The individual S-parameters in (4.22), (4.23), and (4.24) are used to populate the coefficient and constant matrices of (2.27) and solve for the error parameters. Equation (2.27) is a general system of equations that can be represented in the general form

$$\mathbf{Ax} = \mathbf{b} \tag{4.26}$$

where $\mathbf{A}$ and $\mathbf{b}$ are the coefficient and constant matrices (constructed from the values in (4.22), (4.23), and (4.24)) and $\mathbf{x}$ is a matrix of the error parameters. Solving for $\mathbf{x}$ gives

$$\mathbf{x} = \begin{bmatrix} 1/e_{23} \\ -e_{00}/e_{e10} \\ -e_{33}/e_{23} \\ -e_{11}/e_{10} \\ -e_{22}/e_{23} \\ (e_{01}e_{10} - e_{00}e_{11})/e_{10} \\ (e_{23}e_{32} - e_{22}e_{33})/e_{23} \end{bmatrix} = \begin{bmatrix} 1 \\ 0.5405 \\ 0.5405 \\ -0.9917 \\ -0.9917 \\ 0.5405 \\ 0.5405 \end{bmatrix}. \tag{4.27}$$

With the error parameters in $\mathbf{x}$ and test bus measured DUT S-paramters in (4.25), the DUT

Table 4.2: Calibration extracted DUT transimpedance obtained with the 4-port and 1149.4 test bus using either the ideal low-frequency or high-frequency test bus components.

Test Bus		Gain	Error
Reference		1000 V/A	-
Ideal Low-Freq.	1149.4	995.1 V/A	0.49 %
	4-Port	1000 V/A	0 %
High-Freq. Errors	1149.4	0.9355 V/A	99.9 %
	4-Port	1000 V/A	0 %

S-parameters are de-embedded using (2.28) and gives

$$\mathbf{S_{DUT}} = \begin{bmatrix} -0.2346 & 0 \\ 8.1759 & 0.3377 \end{bmatrix}. \tag{4.28}$$

The final step is to take the DUT S-parameters and convert them to the more readable transimpedance gain to be able to compare them to the expected value. Equation (4.8) uses $\mathbf{S_{DUT}}$ and assumes a high-impedance load ($\Gamma_L = 1$) to give the final transimpedance

$$Z_T = 1000\ V/A. \tag{4.29}$$

This 4-port test bus example is repeated again instead using the high-frequency error component parameters. All final transimpedance values are captured in Table 4.2.

This simple simulation shows that, under ideal conditions, the 4-port test bus can perfectly extract the DUT S-parameters. The 1149.4 calibration failed to fully account for the errors present.

4.5 2-Port Test Bus Reverse Signal Requirement

A requirement of the 8-term error model is that all eight terms are nonzero. This raises questions about applying the 8-term error model to the 2-port test bus, since ideal buffers only convey signals in one direction. The 4-port test bus, by contrast, provides a defined

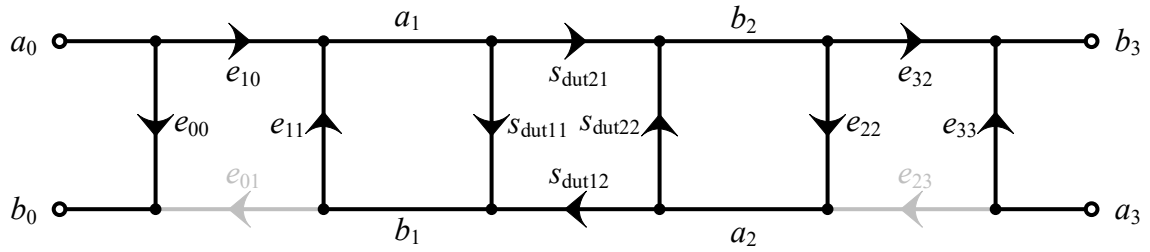


Figure 4.9: Signal flow diagram of the 2-port test bus with weak reverse error signals (e_{01} and e_{23}).

buffer for applying a test signal and a defined buffer for reading out the test signal. The 2-port test bus is reliant on the fact a non-ideal buffer will leak signals backward to fulfill the calibration requirement.

To demonstrate the need for a reverse signal through the buffers, the 8-term error model calibration signal flow diagram is shown in Fig. 4.9 with the reverse error terms grayed out (e_{01} and e_{23}). Without the reverse error terms, the s_{00}, s_{33}, and s_{03} measurements do not provide information about the DUT because the DUT does not affect them. Calibration can then not be performed because the system is ill-conditioned.

Buffers in the 2-port test bus can have enough reverse signal leakage depending on their design. One way is to have simple buffer designs that depend on the parasitic leakage signal, which typically increases at higher frequencies. The reverse signal grows large enough to allow calibration at frequencies where calibration is most likely needed. Therefore, the 2-port test bus is a viable test bus option, but care must be taken to ensure strong reverse signals.

4.5.1 Comparison of 2-Port Test Bus

To further illustrate the operation of the 2-port test bus, the 4-port test bus example is continued in this section. Fig. 4.10 shows the simulation setup of the 2-port test bus. The schematic is generalized in the same way as the 4-port test bus test setup schematic, with the turned-off buffers ignored to simplify the diagram. The overall structure stays the same

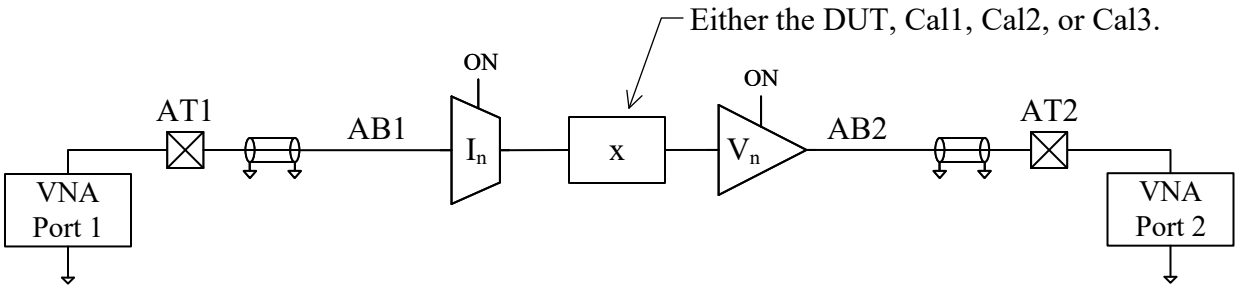


Figure 4.10: General 2-port test bus measurement setup with the center block switching between the DUT, Cal1, Cal2, and Cal3.

Table 4.3: New current buffer component parameters used in the 2-port test bus example.

Component		*Gain*	Z_{in}	Z_{out}	Z_{leak}
Current Buffer	High-Freq. Errors	0.98 A/A	30 Ω	2 kΩ	7 kΩ
	High-Freq. Errors Zero Reverse	0.98 A/A	30 Ω	2 kΩ	∞ Ω

as you move between the measurements of the DUT and calibration references. Being a 2-port system, test bus measurements are performed with a 2-port VNA. Therefore, there is no need to do the 4-port to 2-port conversion as is required for the 4-port test bus.

As discussed in the previous section on the reverse signal requirement, the buffers must have a reverse signal path that travels backward through the buffers. In this example system, the reverse is provided by the Z_{leak} parameter. The high-frequency version of the current and voltage buffers both have $Z_{leak} = 7\ k\Omega$. An additional version of the current buffer is created for this example with zero reverse signal by setting $Z_{leak} = \infty\ \Omega$. Table 4.3 contains the new buffer parameters used for the 2-port test bus example.

After measuring the calibration references and DUT, the error parameters are solved for and de-embedded from the DUT measurement. Converting the S-parameter to transimpedance gives the final values which are captured in Table 4.4. The 2-port test bus calibration perfectly extracted the DUT's high-frequency gain. When the current buffer with zero reverse signal leakage was used instead, the calibration algorithm failed and gave zero.

This ideal simulation verified the calibration procedure math and showed that the 2-

Table 4.4: Calibration extracted DUT transimpedance obtained with the 2-port test bus using either the ideal low-frequency, high-frequency, or zero reverse signal high-frequency test bus components.

Test Bus		**Gain**	**Error**
Reference		1000 V/A	-
Ideal Low-Freq.	1149.4	995.1 V/A	0.49 %
	4-Port	1000 V/A	0 %
High-Freq. Errors	1149.4	0.9355 V/A	99.9 %
	4-Port	1000 V/A	0 %
	2-Port	1000 V/A	0 %
	2-Port Zero Reverse	1.3×10^{-13} V/A	100 %

port test bus can exactly extract the DUT transimpedance given that the reverse signal requirement is met. When the current buffer reverse signal is set to zero, the algorithm fails.

4.6 Practical Error Block Consideration

An important assumption made in the VNA calibration approach is that the error terms remain consistent between measurements. To illustrate this, Fig. 4.11 shows the proposed test bus 2-port calibration model with a notation difference between the error blocks. The input error blocks are labeled $\mathbf{S_{A\_dut}}$, $\mathbf{S_{A\_cal1}}$, $\mathbf{S_{A\_cal2}}$, and $\mathbf{S_{A\_cal3}}$ and the output error blocks are labeled $\mathbf{S_{B\_dut}}$, $\mathbf{S_{B\_cal1}}$, $\mathbf{S_{B\_cal2}}$, and $\mathbf{S_{B\_cal3}}$. Referencing back to the 4-port test bus schematic in Fig. 3.1, physically different buffers are used in each calibration and DUT measurement. These buffers contribute to the error blocks and the fact that these buffers are different means that there will always be some amount of difference between them.

A more accurate model acknowledges the difference between the error blocks. The mismatch will result in an inaccurate calibration because the calibration algorithm assumes that the errors are consistent. Assuming the error blocks are consistent is fundamental to setting up the calibration problem. Without it, the goalposts are constantly moving and the structure of the calibration falls apart.

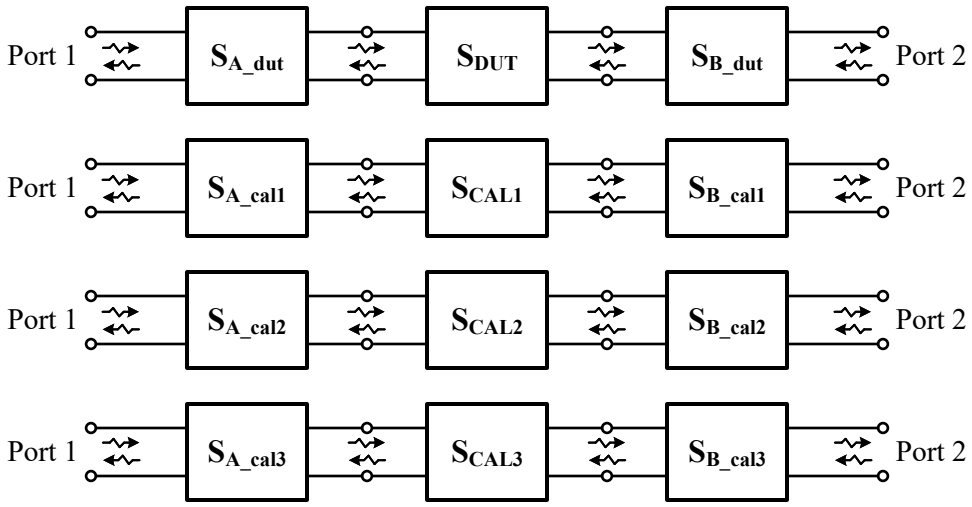


Figure 4.11: Network diagram of the proposed test bus calibration model with error block matching emphasized.

The idea of matching error blocks is a known consideration in traditional VNA calibration. In a traditional VNA calibration procedure, the probes are moved between measuring the calibration references and DUT. Each time the probes are moved, the cables may shift positions or the probe may land on the pad differently. These differences can result in error block mismatches. VNA measurement guidelines include ways to mitigate these effects and report typical impacts [44].

Error block mismatch becomes a more significant consideration in the proposed test buses due to the inclusion of active buffers in the error blocks. Ensuring the buffers match as closely as possible will give the most accurate calibration results. Matching can be fulfilled on an IC because of the processes intrinsic ability to match between components nearby. Extra attention can be paid during the design to not create a circuit sensitive to process differences and to lay out the components close by.

Putting the matching assumption into an equation, the input and output error blocks of Fig. 4.11 must be approximately equal across the four measurements

$$\begin{aligned} \mathbf{S_{A\_dut}} &\approx \mathbf{S_{A\_cal1}} \approx \mathbf{S_{A\_cal2}} \approx \mathbf{S_{A\_cal3}} \\ \mathbf{S_{B\_dut}} &\approx \mathbf{S_{B\_cal1}} \approx \mathbf{S_{B\_cal2}} \approx \mathbf{S_{B\_cal3}} \end{aligned} \tag{4.30}$$

to enable accurate calibration. Hence, the error blocks are simply referred to as $\mathbf{S_A}$ and $\mathbf{S_B}$ in the previous calibration sections.

4.7 Summary

The calibration of the proposed test buses is based on the established general algorithm from the literature. S-parameters are the final result of a VNA measurement, which can be directly converted to voltage and current knowing the load impedance. The 4-port test bus requires an extra 4-port to 2-port conversion to work with the established algorithm. Calibration references that can be integrated with the test bus are critical to calibration success. A load resistor is identified as meeting test bus requirements and can be characterized using low-frequency measurement in conjunction with the current and voltage buffers. A numerical simulation showed the 4-port test bus's performance improvement over 1149.4 at high frequencies. The 2-port test bus calibration requires a reverse signal path and the calibration performance is again demonstrated with a numerical simulation. With ideal calibration references and perfectly matched error blocks, the 4-port and 2-port can perfectly extract the DUT's performance.

Chapter 5

PCB Test Bus Experiment

To first test the high-level topology and calibration methodology of the proposed analog test bus, a discrete component implementation was assembled on a PCB. This PCB experiment takes the first steps in quantifying the real-life performance of the proposed 4-port test bus without the need of an expensive and time-consuming tape out. The eventual use case of the proposed analog test bus is integrated within a chip like IEEE 1149.4.

As shown in the previous chapter's theory and ideal simulations, the 4-port test bus can accurately extract the high-frequency DUT performance compared to IEEE 1149.4 due to its VNA-style calibration. To test this hypothesis with a physical implementation, both the 4-port and 1149.4 test buses were built on PCBs using the same components and measuring the same DUT. Controlling for differences in the buffer and DUT performance isolated the performance improvement from the different structures and calibration. A performance difference should be evident at higher frequencies when buffer errors and parasitic elements become significant.

Three separate PCBs were constructed as part of the test. Two of the PCBs were the 4-port and IEEE 1149.4 test buses. Constructing both allows for a direct comparison while controlling variables. The third PCB was constructed of only the DUT to provide a reference DUT measurement to compare the test bus measurements. The test bus's were first

simulated using models of the PCB construction and then physically built and measured.

5.1 Design of Experiment

The 1149.4 and 4-port test bus PCB implementations remain consistent with the structures originally captured in Fig. 3.1 and Fig. 2.2. The voltage buffers, current buffers, calibration references, and DUT were created with discrete components that meet the performance requirements as described in the previous two chapters. A simplified schematic of the PCB implementation of the 4-port test bus is shown in Fig. 5.1 and the 1149.4 test bus is shown in Fig. 5.2. Both test bus schematics represent the DUT with a high-level block because they use the same transimpedance amplifier (TIA) circuit. This common circuit is detailed separately in Fig. 5.3. To be clear, each test bus PCB has its own TIA built on the PCB. These schematics show in greater detail exactly how the DUT, calibration references, ports connections, and switches were implemented for the PCB experiment.

The exact same components were used to construct both test buses on separate four-layer PCBs with similar layouts. High-accuracy passive components were also used to reduce the likelihood of matching errors. This ensures that any performance differences are a result of the structure and calibration instead of being related to the limitations of the discrete components and PCB layout.

The voltage and current buffers were built from Texas Instruments OPA861 transconductance amplifiers. The OPA861 is a versatile component that can also operate as a current conveyor. This versatility means that, depending on how the OPA861 is connected, it can behave as a voltage or current buffer. Figs. 5.1 and 5.2 may show the voltage and current buffers as different symbols, but they are both created by the OPA861 connected in their different arrangements. Discrete current buffer ICs are not a typical product category and therefore required the use of OPA861. The OPA861 chip includes a quiescent current adjust pin that was connected to a high-accuracy resistor to ensure that all buffers would have the

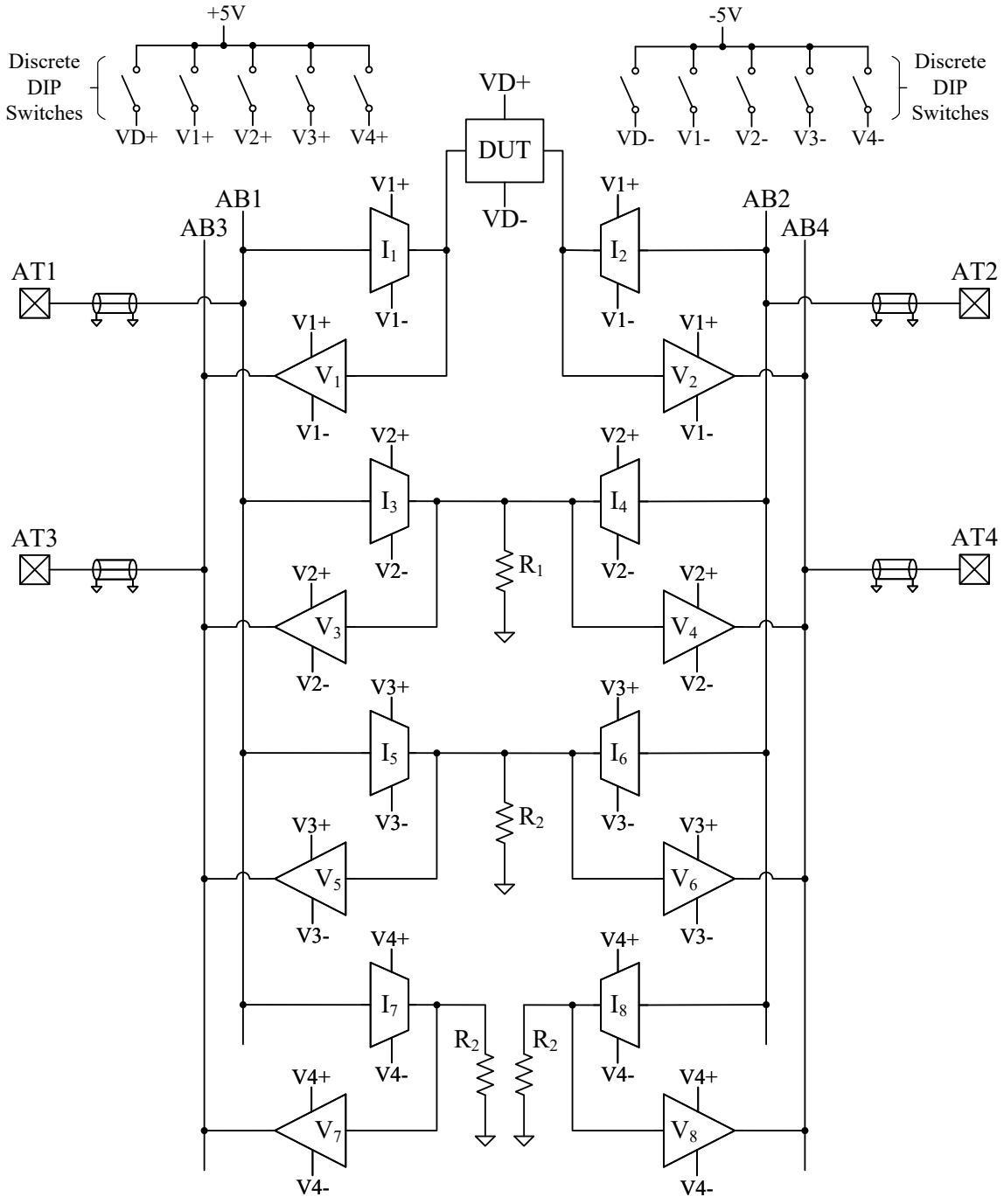


Figure 5.1: 4-port test bus PCB experiment schematic.

same quiescent current. The ability to adjust the OPA861 performance is less important than matching all the buffers. The exact resistor value for the test bus implementations was 250 $\Omega \pm 0.1\%$.

To switch on/off the buffers and DUT, discrete dual in-line package (DIP) switches were

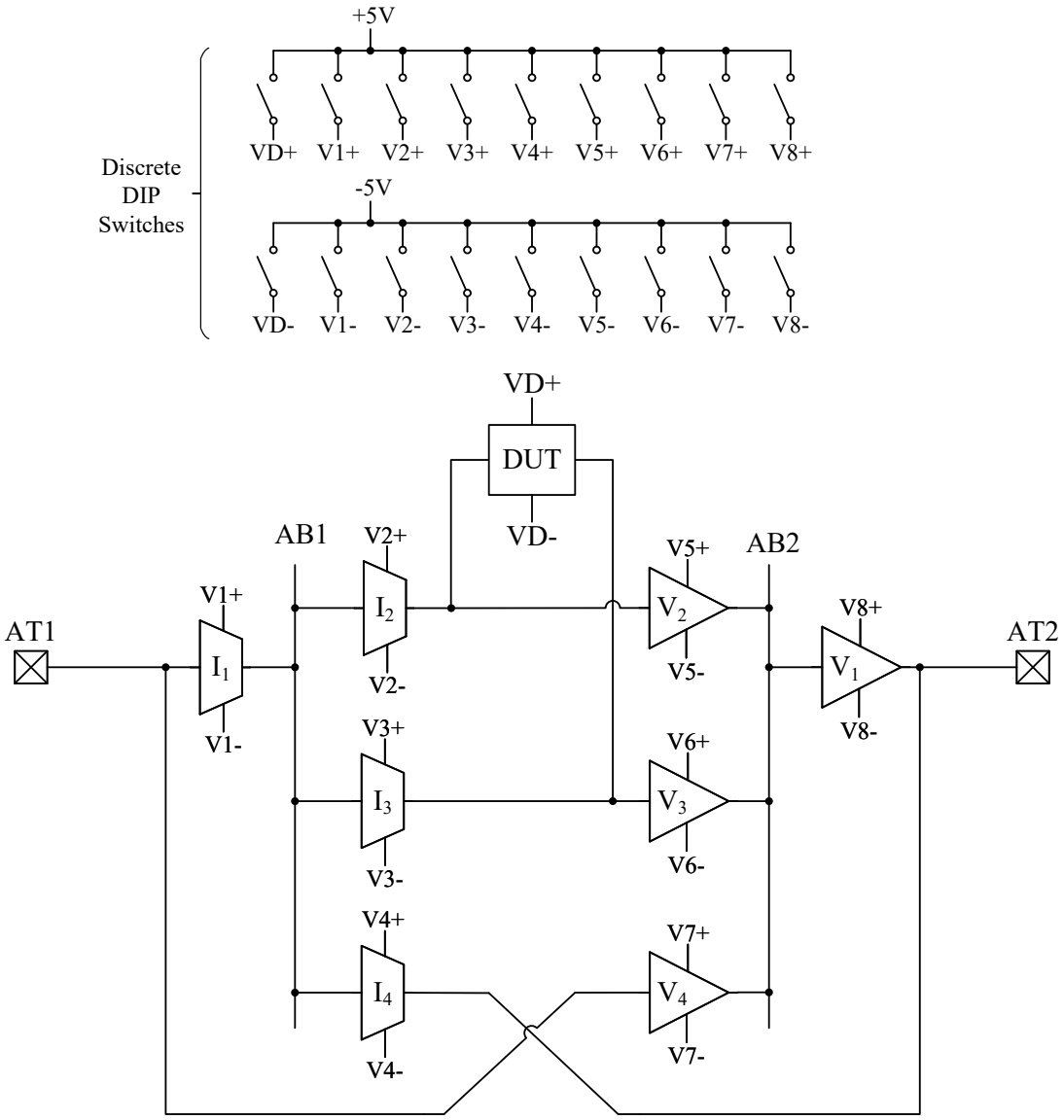


Figure 5.2: IEEE 1149.4 test bus PCB experiment schematic.

inserted on the power traces to cut power to the components. These DIP switches were manually controlled during the testing process. The buffers and DUT are powered by +5 V and -5 V and therefore required two DIP switches for each component/group.

The Interconnect Test Circuit block seen previously in the high-level structure of the 4-port and 1149.4 test buses was not included in the PCB implementation. This block contains extra functionality for testing the continuity between port connections and is irrelevant to test bus measurements of an internal DUT. Therefore, the Interconnect Test Circuit was

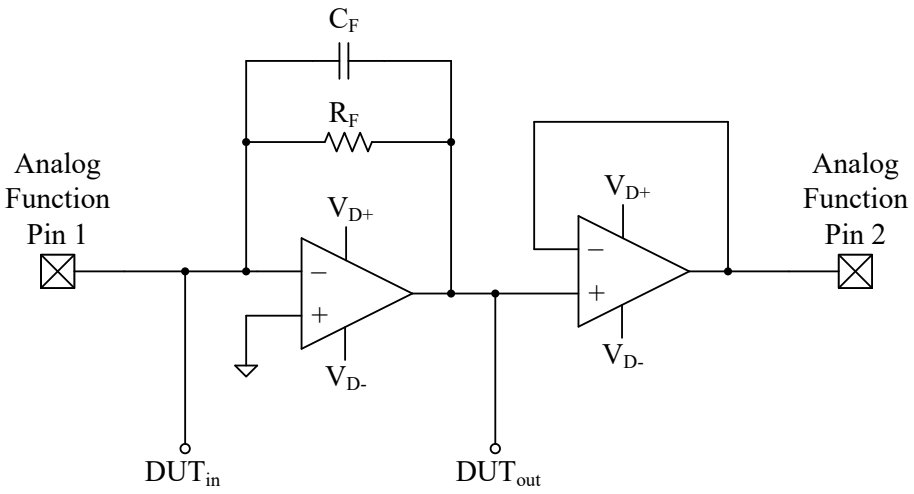


Figure 5.3: Schematic of TIA DUT circuit used in the 4-port and 1149.4 test bus PCBs.

omitted from PCB experiment for simplicity and focus on the test bus structure.

The 4-port test bus calibration references were built with ±0.1 % accurate resistors $R_1 = 100\ \Omega$ and $R_2 = 200\ \Omega$. These resistors were simply placed between the buffers and provided a relatively low resistance load to the high-resistance current buffer output and voltage buffer input.

The DUT connected to the test buses are the same typical TIA circuit built using the Texas Instruments LMH6609 op-amp shown in Fig. 5.3. The transimpedance is determined by the feedback resistor, in this case chosen to be $R_F = 500\ \Omega$ and therefore $Z_T \approx 500\ V/A$. The stage after the TIA is the op-amp acting as a buffer to drive the output port. The feedback capacitor is used to shape the TIA frequency response and ended up being tuned to $C_F = 3.3\ pF$. R_F and C_F were adjusted together to achieve a TIA frequency response that avoided clipping distortion and preserved high-frequency peaking behavior.

Fig. 5.4 shows a close-up photograph of the final 4-port and 1149.4 test bus PCBs. The layout of the components closely follows the arrangement seen in the test bus schematics. The DUT is located at the top with the analog function ports close by. Below the DUT are the test bus buffers and ports positioned in a consistent and symmetrical manner. The power connection and DIP switches are placed around the perimeter.

An additional copy of the DUT was built unconnected to any test bus to provide a

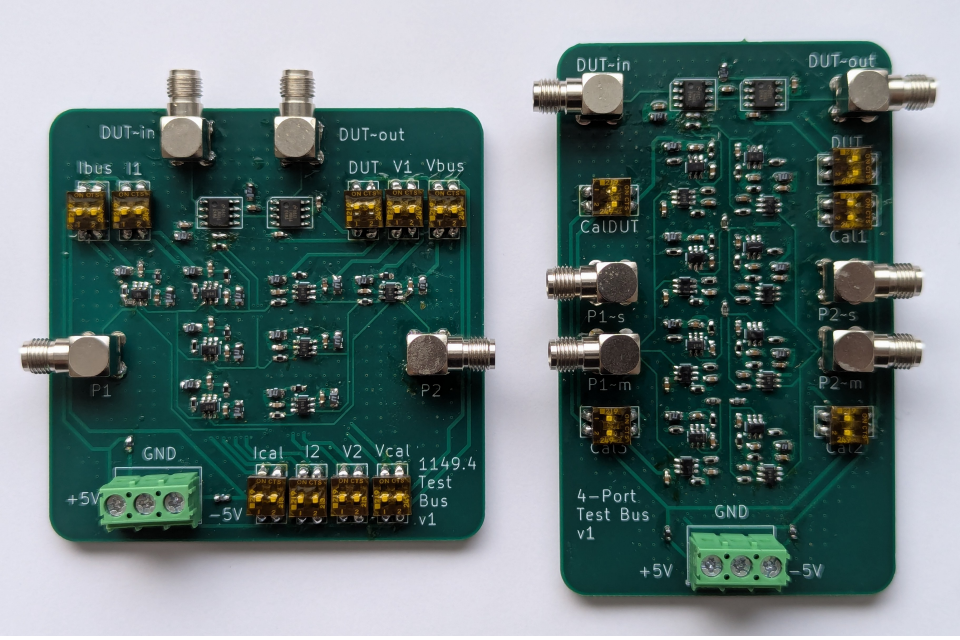


Figure 5.4: Photograph of the final 1149.4 (left) and 4-port (right) test bus PCBs.

directly measured reference transimpedance. Evaluating the performance of the test bus and comparing comparable values is difficult. There is a difference between measuring the transimpedance across Analog Function Pin 1 and 2 versus measuring only across the TIA. That is why a third PCB was built to recreate a DUT measurement looking up from the test bus. Fig. 5.5 shows the schematic of the reference DUT PCB and Fig. 5.6 shows a photograph of the PCB. The TIA circuit is position exactly the same as on the test bus PCBs.

5.2 Simulation Results

The PCB experiment was first simulated to verify that the setup would demonstrate a performance difference between the 4-port and 1149.4 test bus. The simulation was constructed using PSPICE models provided by Texas Instruments for the OPA861 and LMH6609. Calibration resistors were modeled with ideal resistors. Ports were modeled with a capacitive and inductive Pi model. The simulation measured the exact S-parameters at the ports. The reference DUT performance was extracted from the simulation as the transimepedance as seen

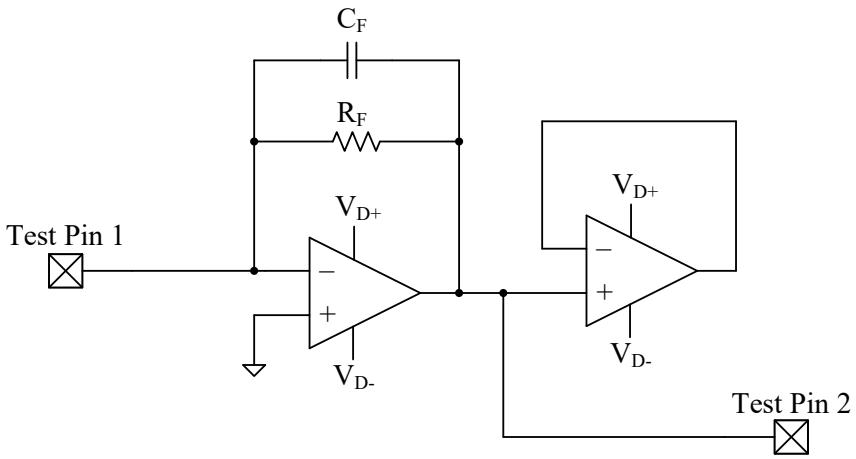


Figure 5.5: Reference TIA DUT PCB schematic to compare performance of 4-port and 1149.4 test buses.

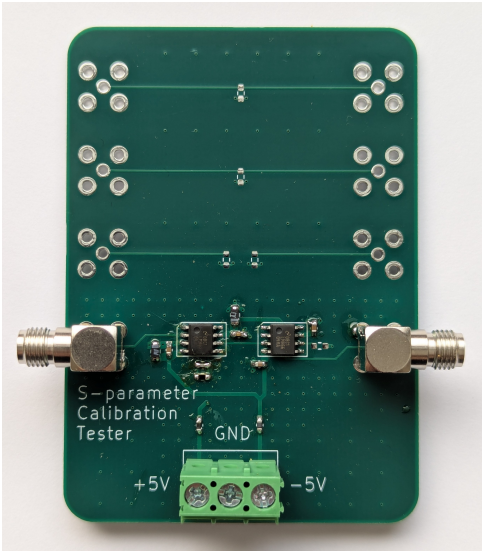


Figure 5.6: Photograph of the final reference TIA DUT PCB.

from the test bus connections. This provides an ideal comparison for what transimpedance the test bus measures.

Fig. 5.7 shows the results of the SPICE simulation. The 4-port test bus tracked the reference DUT transimpedance exactly across all frequencies, while the 1149.4 measured transimpedance peaks higher and rolls off earlier. This error in the 1149.4 result is probably due to the loading effects and resonance between the buffers and DUT not captured during the simple 1149.4 calibration. For example, the calibration current buffer with an

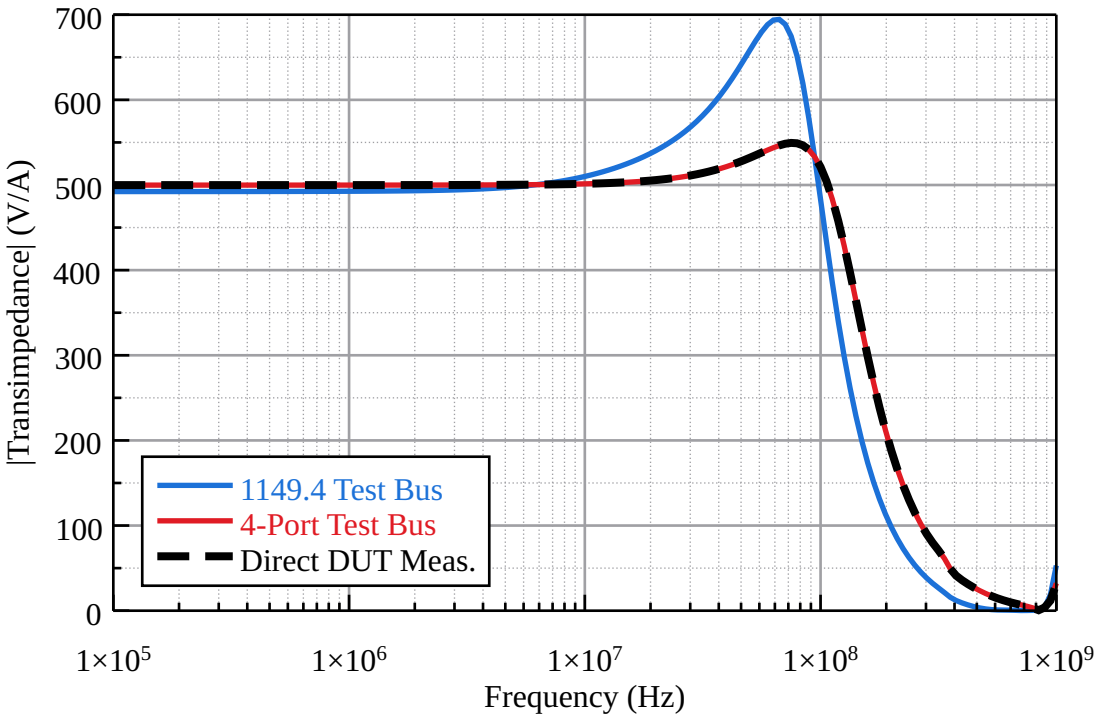


Figure 5.7: Simulation results comparing the transimpedance measured from the proposed 4-port and 1149.4 test bus to a direct measurement of the DUT.

ideal zero-impedance load performs differently from the current buffer loaded by the DUT. The simulation results confirm a significant difference in accuracy between the test buses beginning at 10 MHz.

5.3 Measured Results

A Keysight E5063A ENA Vector Network Analyzer performed the S-parameter measurements, and a photo of the benchtop test setup is shown in Fig. 5.8. The 4-port test bus was measured by moving the 2-port VNA connections between the ports to only collect the required measurements. The unconnected test ports were terminated with 50 Ω resistors to prevent floating nodes. With the connections made, the DIP switches were manually changed to measure the DUT and calibration references.

Before any test bus measurements were made, an initial VNA calibration was performed

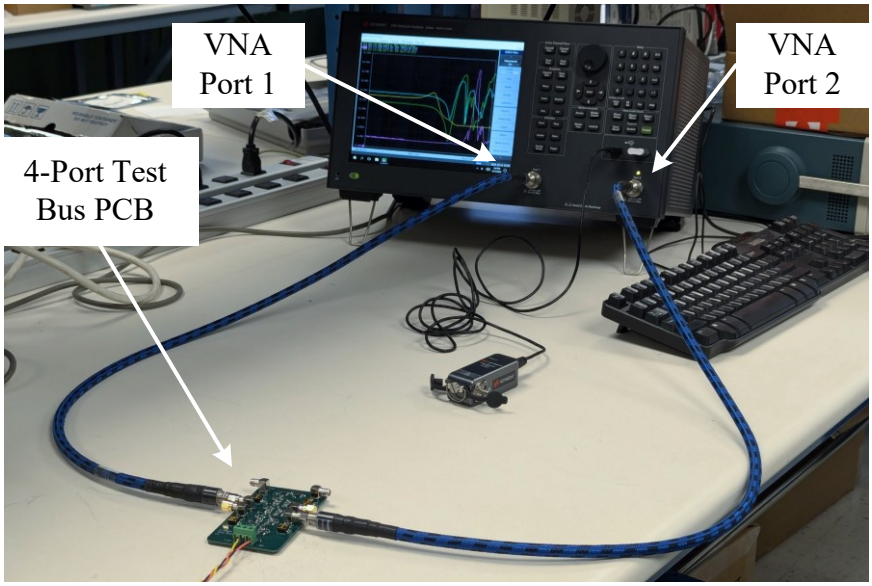


Figure 5.8: Photo of VNA test setup measuring the proposed 4-port test bus.

using the provided electronic calibration module. This calibration step moves the calibration reference plane to the end of the cables and calibrates the VNA reference impedance.

Fig. 5.9 shows the PCB experimental results of both test buses compared to the directly measured reference DUT. Both test buses accurately measured the low-frequency transimpedance of 500 V/A. The 1149.4 test bus starts deviating at 30 MHz while the 4-port test bus tracks the reference DUT measurement up to 150 MHz. Above 150 MHz the 4-port test bus predicts additional resonating not seen in the reference DUT measurement.

5.3.1 Discussion

The difference between the 4-port test bus and the direct DUT result could be explained by mismatches in the calibration paths or DUTs. As discussed in Section 4.6, mismatches between buffers will cause errors in the final results, and these mismatches are amplified at high frequencies. Additionally, the reference DUT and test bus DUT performance may not match exactly, and therefore the test bus result would not match exactly.

As indicated by the simulations, when the 4-port test bus has ideal buffer matching and is compared to an ideal reference DUT measurement, it can exactly de-embed the

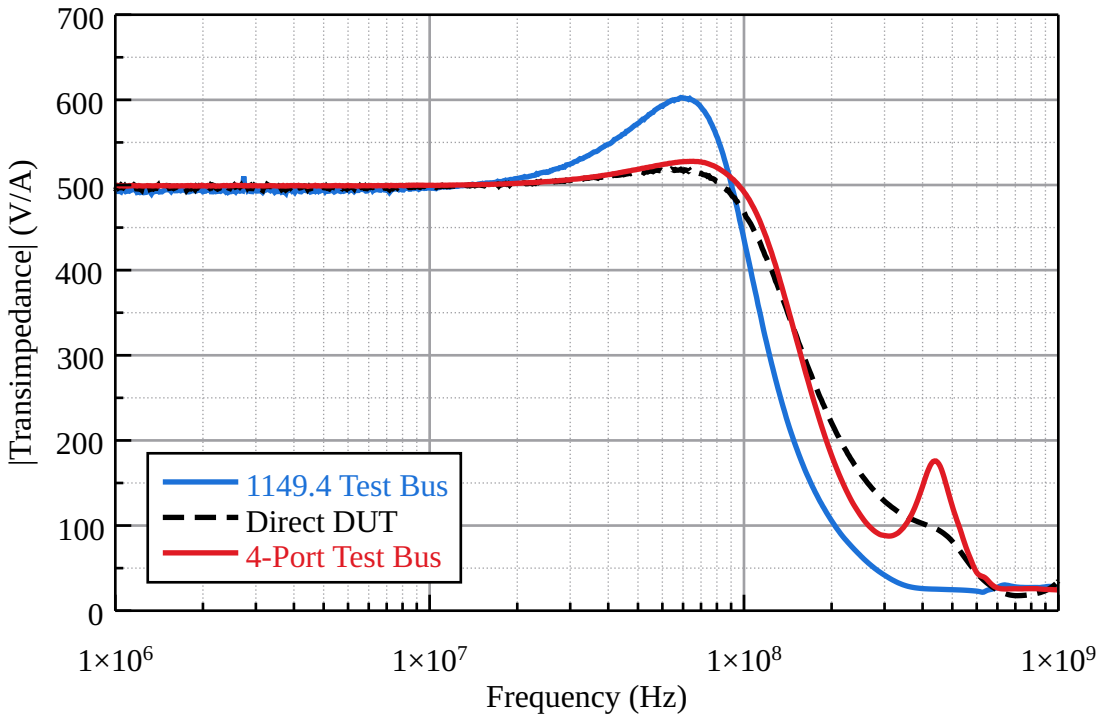


Figure 5.9: Experimental results comparing the proposed 4-port and 1149.4 test bus to a direct measurement of the DUT.

transimpedance. Implementing the 4-port test bus with discrete components comes with the challenge of closely matching the measurement paths and obtaining a reference DUT measurement that mirrors what the test bus sees. Precautions were taken when designing the PCB to minimize these effects by using high-accuracy passives, symmetrical layout, and creating a separate reference PCB. Additionally, their is an inherent bandwidth limitation building on a PCB due to the large PCB parasitic elements.

Integrating the 4-port test bus on-chip would improve the matching between the buffers and extend the measurement bandwidth. Circuits located on the same chip, especially close together, are known to match very closely and is a property commonly taken advantage of in analog circuit design. On-chip circuits are also closer together compared to a PCB meaning there are less electrically long interconnects between components with significant parasitic elements.

To the best of the authors' knowledge, VNA calibration has not been used in applications

where the error blocks include active components. VNA calibration is usually only used to account for errors occurring from transmission lines and probe/pad parasitic elements. As long as the components making up the error blocks can be represented using S-parameters, VNA calibration should work. Therefore, the proposed test bus experiment also demonstrates a unique application of VNA calibration that includes active components in the error blocks.

The 4-port test bus to 2-port conversion demonstrates an interesting idea that not all the S-parameters of a system are needed to extract the DUT from the middle. The flow simplification of the signal flow graph shown in Section 4.2 can be conceptualized as applying a known signal and measuring the effect of that signal influenced by the DUT. It does not matter whether the influence is measured by the reflected wave on the same input port or a separate port whose signal is proportional to the influence. This also eliminates the challenge of measuring the forward and reflected waves with a directional couple. The measurement system could be simplified with only a source and a 50 Ω loaded signal measurement.

5.4 Summary

The 4-port and 1149.4 test buses were implemented on PCBs to test and compare the performance of their structures and calibration. Discrete current and voltage buffer ICs were used to create the test buses and measure the same TIA DUT. The components are switched off using DIP switches connected to the power traces running to each IC. The simulation results demonstrate the 4-port test bus's ability to precisely extract the DUT performance under ideal conditions. The 1149.4 test bus measurement, on the other hand, became inaccurate at the edge of the TIA's bandwidth. The experimental measurement confirmed these results, showing that the 4-port test bus more accurately tracks the reference transimpedance across the bandwidth. Errors between the 4-port test bus and reference transimpedance are present and are likely due to mismatch between buffers and DUTs.

Chapter 6

Extending the Test Bus to the IC

The main advantage of the proposed test bus structures is the extended measurement bandwidth afforded by the calibration procedure. This opens the possibility of using analog test buses in applications not previously feasible, such as integrated RF and mmWave circuits. In addition, analog test buses are used to provide on-chip analog testing capabilities, and therefore it is critical to examine how the proposed test buses translate to the IC. This section presents the design and simulation of the 4-port and 2-port test buses in a high-speed BiCMOS process aimed at a wide-bandwidth TIA DUT. The major challenges with IC integration are highlighted with additional simulations.

6.1 Challenges of IC Integration

The high-level structure presented in Chapter 3 is again used to construct the integrated test buses. This experiment will implement both the 4-port and 2-port test buses. An 1149.4 test bus is also created to provide a performance comparison. Like the PCB experiment, all test buses are constructed of the same fundamental components: voltage buffer, current buffer, switches, and TIA DUT. The process technology used is the Global Foundries 90nm BiCMOS SiGe 9HP.

Integrating the proposed test bus design presents unique considerations compared to the

PCB implementation with discrete components. No standard buffer design is available for the implementation of voltage and current buffers. Ideal DIP switches are not available on-chip and therefore require a different approach to turn off the buffers. Creating an on-chip calibration reference also has additional requirements.

6.1.1 Buffers with Power On/Off Ability

The current and voltage buffers are built from the same current conveyor circuit block. A current conveyor design was necessary to create a simple current buffer. Conveniently, a current conveyor can also be used as a simple voltage buffer and was therefore used for the test bus voltage buffers.

Fig. 6.1 shows the single-ended current conveyor design which is based on the design first presented by Seguin et al. [45]. Creating a current conveyor in a BiCMOS process has the constraint of not having PNP BJTs available. Therefore, NMOS and PMOS current mirrors are used to establish biasing of the NPN BJT current conveyor pair. The input/output nodes are labeled with conventional current conveyor node notation X, Y, and Z. Depending on the connections to the X, Y, and Z nodes, the current conveyor block behaves as a voltage or current buffer. The arrangements are shown in Fig. 6.2. V_{bias1} and V_{bias2} are voltage sources that create 400 mV and 2 V, respectively. Cntrl is a digital control signal that turns the buffer on or off. I_{in} and I_{out} are the input and output of the current buffer. V_{in} and V_{out} are the input and output of the voltage buffer.

Turning off the buffers, so that no signal can travel through the buffers, is done through switches located in the biasing current mirror and internal base node. S1 and S2 disconnect the reference current and set the gate to ground, turning off M5-7 and M1-3. To help ensure that no signal can leak through Q2 or Q3, S3 is included to connect the bases to ground. Switches are built out of transmission gates.

Ideally, there is zero signal transmission through the switched off buffers, although some amount of signal leakage is expected due to capacitive coupling. Fig. 6.3 shows the results of

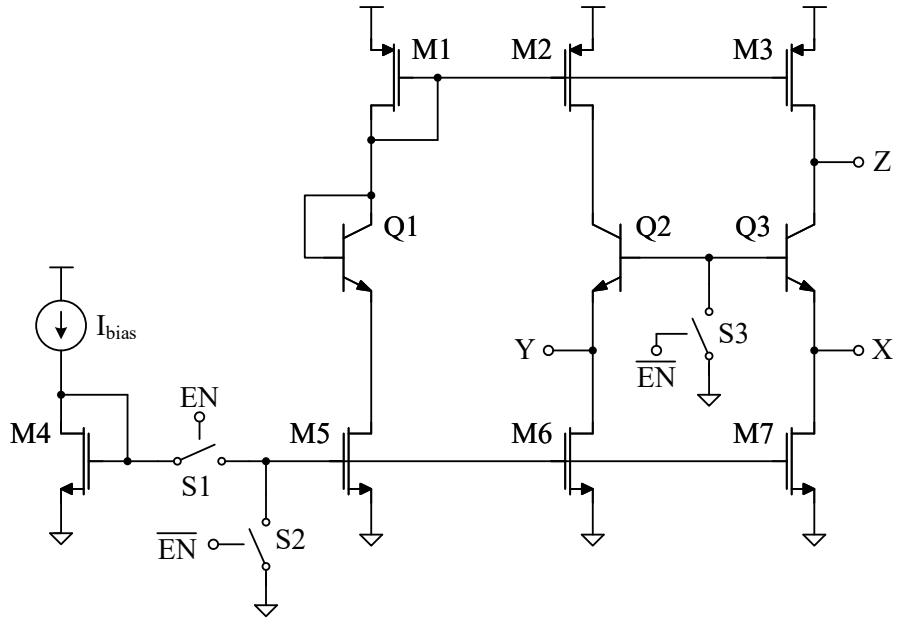


Figure 6.1: Current conveyor (CCII) [45] with power off switches S1-3.

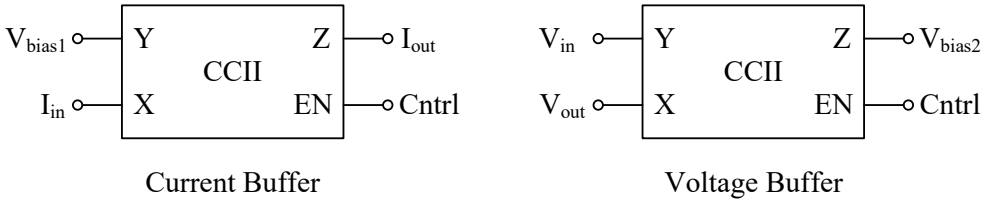


Figure 6.2: Current and voltage buffer arrangements of the current conveyor.

a simulation measuring the forward transmission S-parameter (s_{21}) through a switched off voltage and current buffer. Each buffer's s_{21} is presented with and without S3 present in the current conveyor circuit. The figure shows that the overall s_{21} magnitude stays small and the current conveyor with S3 produces a slight decrease in the leakage signal. With no other downsides observed of using S3, the current conveyor with S3 was used for the experiment.

An alternative approach to turning off a circuit block is to disconnect the power source (Vdd) from the circuit block. This is the approach taken in the PCB experiment presented in Chapter 5 because it was the only way to disable the discrete components. Following the power source switch train of thought would suggest using the same approach for the on-chip BiCMOS current conveyor. The power switches are transmission gates located between the

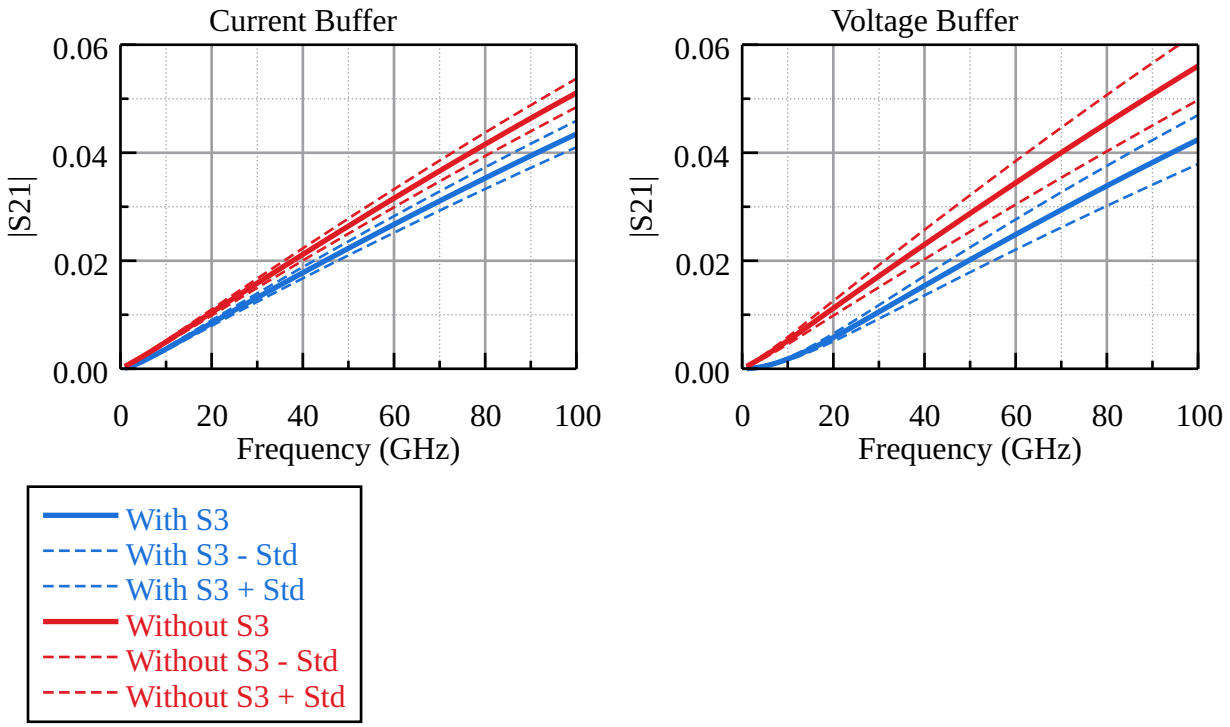


Figure 6.3: Comparison of buffers turned off with and without the presence of S3 connecting internal base to ground. Monte Carlo simulation with the average and standard deviation (Std) plotted.

source terminals of M1-3 and Vdd. Only disconnecting the power source is not sufficient to completely disable the current conveyor. Switches to disconnect the current mirror (S1 and S2) are required to completely turn off M5-6. Otherwise, the gate voltage will remain high and draw current.

Knowing that a current mirror disconnect is required raises the question of whether power switches improve switched-off performance. Fig. 6.4 shows the results of an experiment that compared the $|s_{21}|$ leakage signal through a current and voltage buffer with different arrangements of S3 and power switches. Including power switches in the current conveyor did not provide an advantage over the S3 switch. In addition, power switches have the disadvantage that they need to be large devices to sufficiently reduce their resistance. Therefore, the current conveyor design did not include the power switches and only used S1-3.

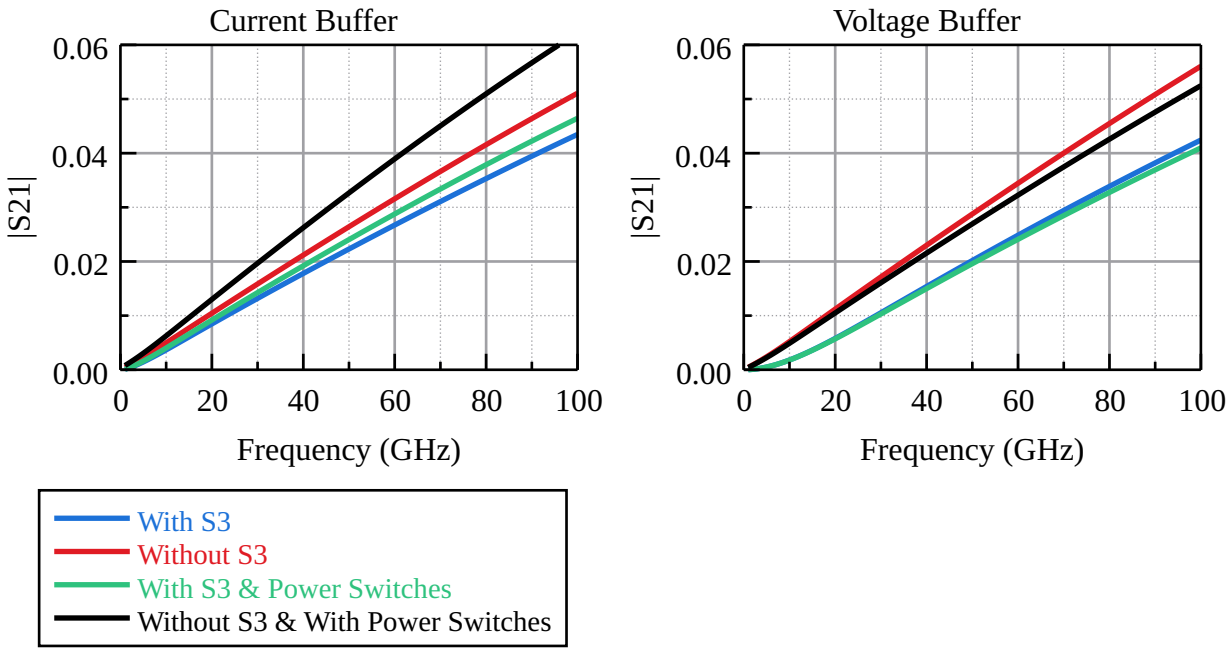


Figure 6.4: Comparison of buffers turned off with the four combinations of S3 and power switches present or not. Monte Carlo simulation with only the average plotted.

6.1.2 Buffers with Reverse Signal Transmission

The 2-port test bus can be applied to the BiCMOS experiment unlike the PCB implementation because the buffers feature enough reverse signal transmission to properly measure the calibration references and perform the calibration. Fig. 6.5 shows the reverse signal transmission (s_{12}) through the current and voltage buffer. The reverse signals start near zero and grow to more than 0.1. Below 2 GHz the 2-port calibration will fail due to the small and inaccurate reverse signal. Therefore, a different calibration approach could be used like simple gain calibration.

The current conveyor facilitates enough reverse signal transmission using a simple design. The signal only needs to be capacitively coupled through a maximum of two transistors. This contrasts other buffer design options using op-amps that would need to travel through multiple transistors and large circuit blocks.

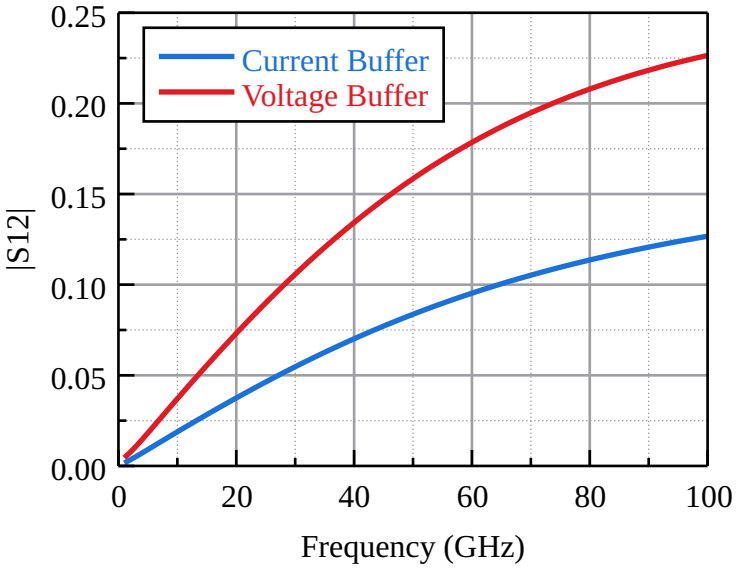


Figure 6.5: Reverse signal transmission through switched on current and voltage buffer. Monte Carlo simulation with only the average plotted.

6.1.3 On-Chip Calibration References

The calibration references only need to behave as a resistor load in a small-signal equivalent circuit. The best calibration reference is one that can integrate well with the buffers and provide a stable small signal reference across the frequency bandwidth. A simple load resistor to ground does not work for this application because it does not establish a DC voltage biasing point on the buffers similar to the DUT. Unlike the PCB implementation, a midpoint voltage source is not provided on-chip. Creating an on-chip voltage source with very low resistance adds significant overhead. Therefore, diode voltage drops are used to establish the DC point and set the calibration resistance.

A schematic of the on-chip calibration references is shown in Fig. 6.6. The resistors R_1 to R_4 are the only component that changes between the references and are implemented as basic n-diffusion resistors. The diode-connected transistors provide voltage drops that help reduce the current draw and resistor sizes. These resistors are sized so that the ratio sets the center node to 1.11 V. Table 6.1 provides a summary of the resistor values chosen and

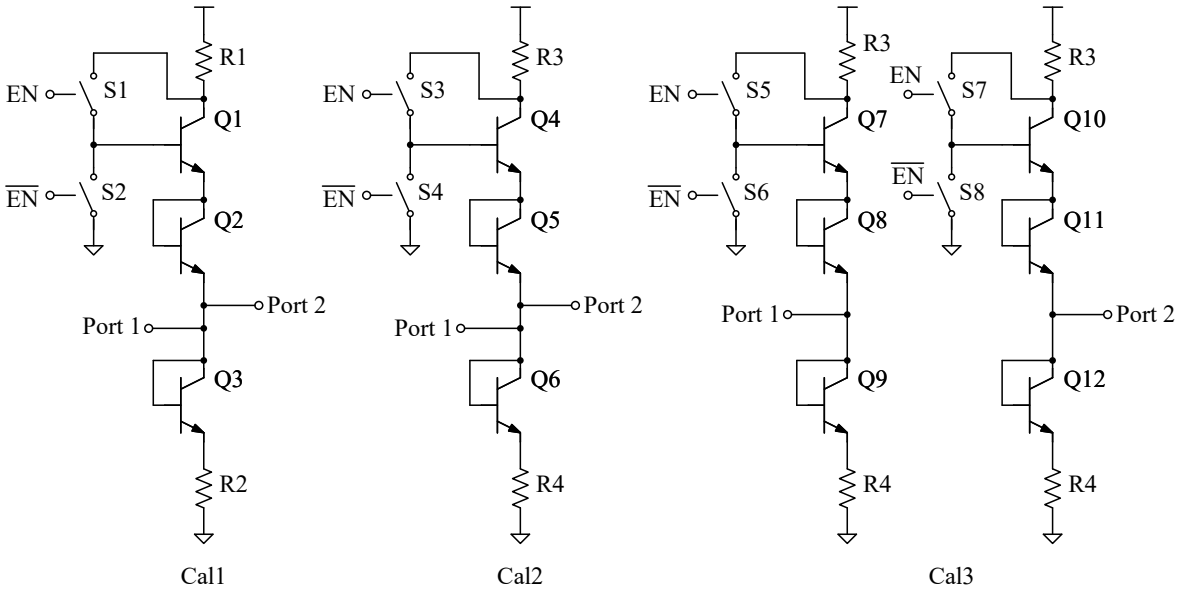


Figure 6.6: 2-port and 4-port test bus calibration references.

Table 6.1: Calibration reference's component values.

Parameter	Value
R1	243 Ω
R2	125 Ω
R3	582 Ω
R4	300 Ω
r_{cal1}	104 Ω
r_{cal2}	230 Ω
r_{cal3}	230 Ω

the equivalent small-signal resistance for calibration.

Included with the calibration references are switches to disable the transistors and stop current consumption when the references are not in use. The switches are located in the base - collector connection of the uppermost diode connected transistor. When the reference is enabled and operating normally, the base - collector connection is shorted, and when the reference is disabled, the base is connected to ground, turning off the transistor and preventing current from flowing.

The calibration references are tested separately to prove that they provide consistent

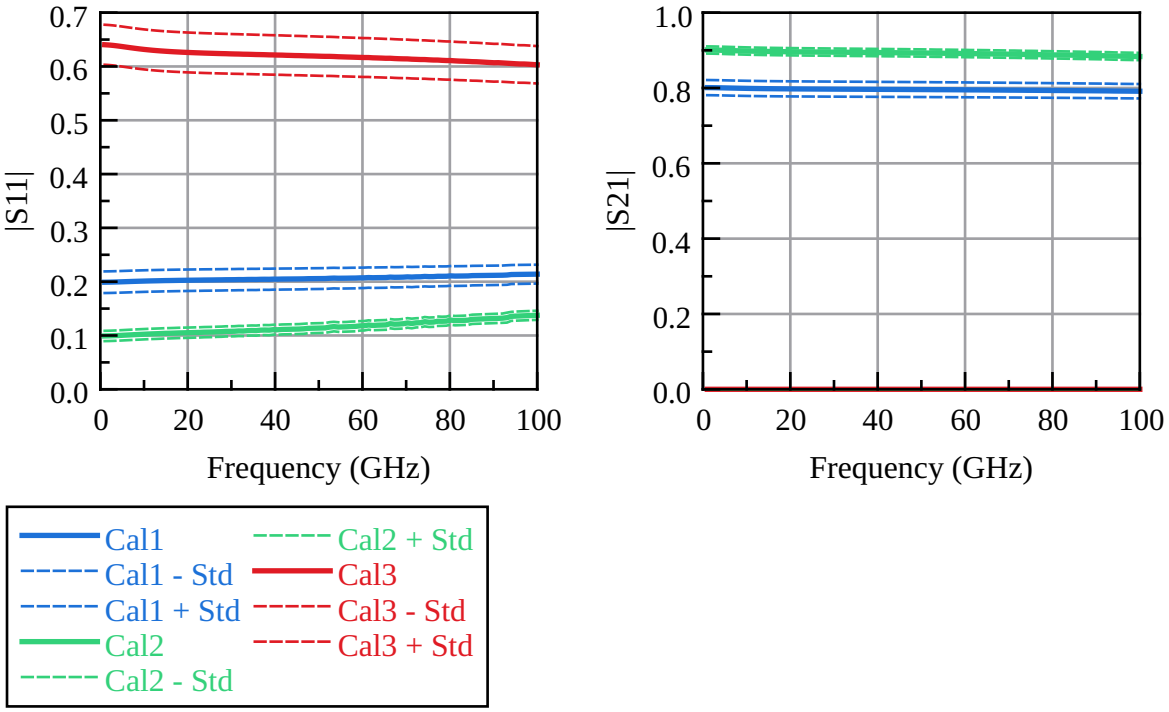


Figure 6.7: Calibration reference (Cal1, Cal2, and Cal3) S-parameter performance. Monte Carlo simulation with the average and ± standard deviation (Std) plotted.

S-parameters across the bandwidth of interest. As an example, Fig. 6.7 shows Cal1 S-parameters with variation from a Monte Carlo simulation. The S-parameters remain consistent across the bandwidth.

Using diode-connected BJTs has advantages over simply creating a voltage divider with resistors. Less voltage drop across the resistors means that, for a given resistance, less current is drawn. In addition, the bias voltage is maintained more consistently. For example, performing a Monte Carlo simulation of Cal1 and recording the DC voltage value of the center node, gives an average value of 1.08 V and standard deviation of 12.3 mV. Compared to only using a voltage divider created from two resistors which has an average value of 1.12 V and a standard deviation of 58.0 mV. Having the center bias voltage be as consistent as possible is important for the calibration references to match each other both in the differential paths and between calibration references. It is also important to consistently bias the buffers at the same point and not induce mismatches between the buffers.

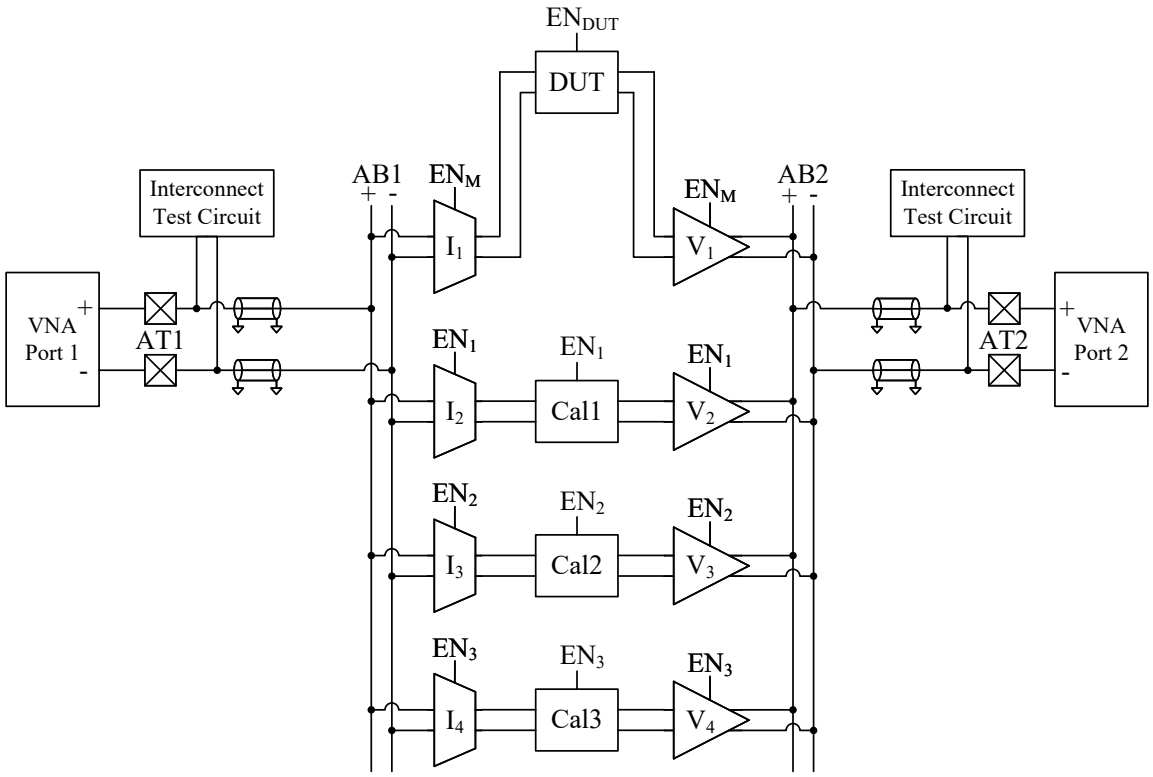


Figure 6.8: Differential 2-Port Proposed Test Bus.

6.2 BiCMOS Test Bus High-Level Schematic

The proposed 2-port test bus implemented differentially for the BiCMOS experiment is shown in Fig. 6.8 and the 4-port test bus is shown in Fig. 6.9. The buffers and calibration references are implemented as shown previously in Figs. 6.1 and 6.6, respectively. Ports and transmission lines are included in the simulation using the provided models from the BiCMOS process. Electrostatic discharge (ESD) diodes were added as part of the port model. In addition, the interconnect test circuit is included to model its parasitic elements. This includes two open transmission gates and the input of a comparator.

The DUT of the BiCMOS experiment is a high-gain wide-bandwidth TIA as shown in Fig. 6.10 consisting of a TIA, amplifier, and output buffer. Nodes DUT_{in} and DUT_{out} are connected to the test bus. The high-speed wide-bandwidth TIA and amplifier circuits were provided by Babar [46].

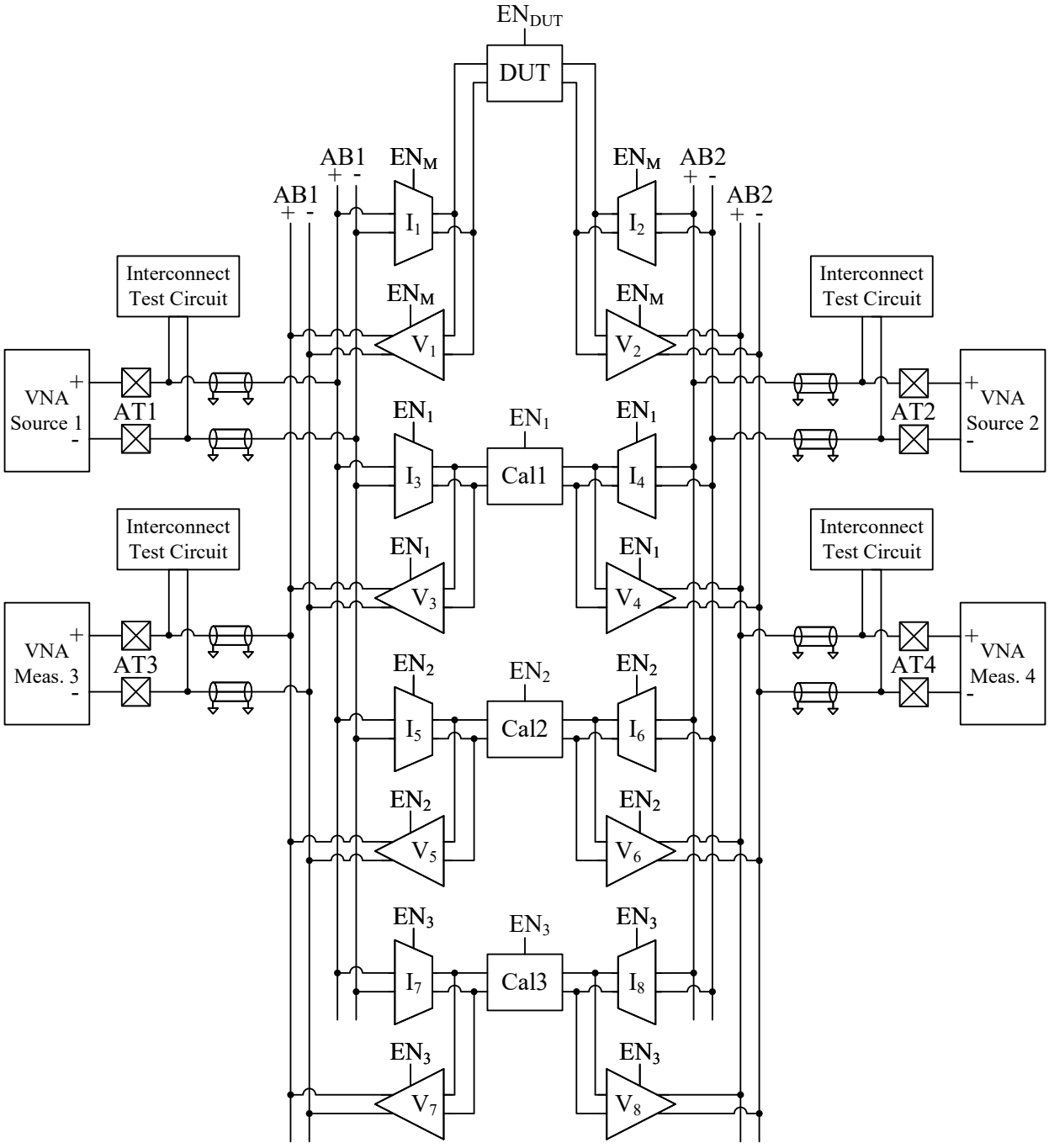


Figure 6.9: Differential 4-Port Proposed Test Bus.

A differential IEEE 1149.4 was also implemented in the BiCMOS process using the same buffers, DUT, and port modeling as the 2-port and 4-port test buses. Another high-level schematic of the 1149.4 test bus is not included because of the similarities to the 2-port and 4-port figures already presented. Refer to Fig. 2.2 for a reminder of the high-level structure

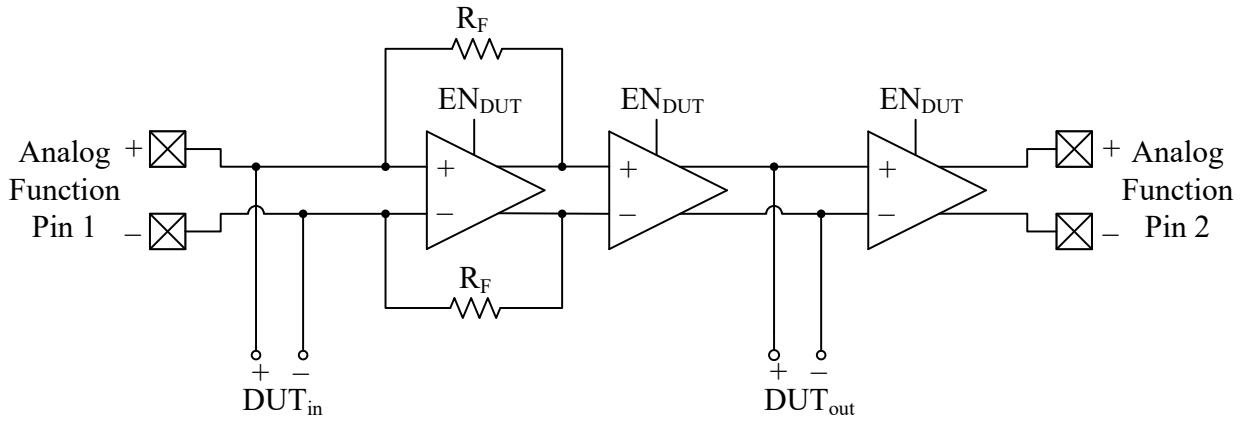


Figure 6.10: High-level schematic of the BiCMOS experiment TIA DUT showing the TIA, amplifier, buffer, and port connections.

of the 1149.4 test bus.

6.3 Simulation Results

When simulating the test buses and evaluating their performance, it is important to perform a Monte Carlo simulation to induce process variation and mismatches between components. If simply simulating with ideal components, the buffers will match perfectly and give unrealistically accurate results. Each iteration of the Monte Carlo simulation varies the overall process parameters and creates mismatches between the individual components. Mismatches between buffers on a given simulation iteration are of the most consequence. The proposed test buses should easily account for consistent changes across all components. Process variation is expected to affect the performance of the DUT. This new performance becomes the goal of the test bus to extract accurately.

The best performance test evaluates how close the test bus extracted transimpedance of a given Monte Carlo iteration is to the DUT transimpedance of that same Monte Carlo iteration. How far the test bus extracted transimpedance is to the DUT transimpedance will be referred to as the transimpedance difference. If the test bus worked perfectly, then the transimpedance difference would be zero. The Monte Carlo simulation gives a set of

transimpedance differences which can be statistically evaluated to get the average transimpedence difference and the standard deviation.

Firstly, Fig. 6.11 shows the average transimpedance extracted from the three different test buses along with the ideal average transimpedance extracted directly from SPICE. This figure gives an indication of on average how close the test bus extracted transimpedance is to the ideal SPICE extracted value.

Fig. 6.12 shows the transimpedance difference, as previously defined, of the three test buses. The 4-port and 2-port test buses are close to zero across the bandwidth of interest. The 2-port test bus varies around the 0 dB mark at frequencies above 60 GHz compared to the more consistent 4-port test bus. At low frequencies, the 1149.4 test bus is as accurate as the other test buses, but at the 20 GHz point it starts to increase in error significantly. In addition, the 4-port test bus maintains the smallest standard deviation even into the high frequencies, meaning less variation in the error.

6.3.1 Discussion

These simulation results demonstrate that the 2-port and 4-port test buses improved the measurement bandwidth over the 1149.4 test bus. The calibration methodology is capable of extracting errors that affect the test bus performance at very high frequencies.

This simulation provides confidence that the proposed test bus structure can translate to the IC from the theory and PCB results presented previously in this thesis. The on-chip voltage buffers, current buffers, and calibration references successfully fulfilled their requirements to facilitate high-frequency calibration. In particular, the 2-port test bus buffers had a sufficient amount of reverse signal leakage to allow the extraction of the error parameters.

The Monte Carlo simulation played a critical role in evaluating the performance of the test buses. This is because the calibration algorithm assumes identical matching between components in the test bus structure, which is not realistic for a manufactured IC. Therefore, the Monte Carlo simulation induces matching and process variations and evaluates the

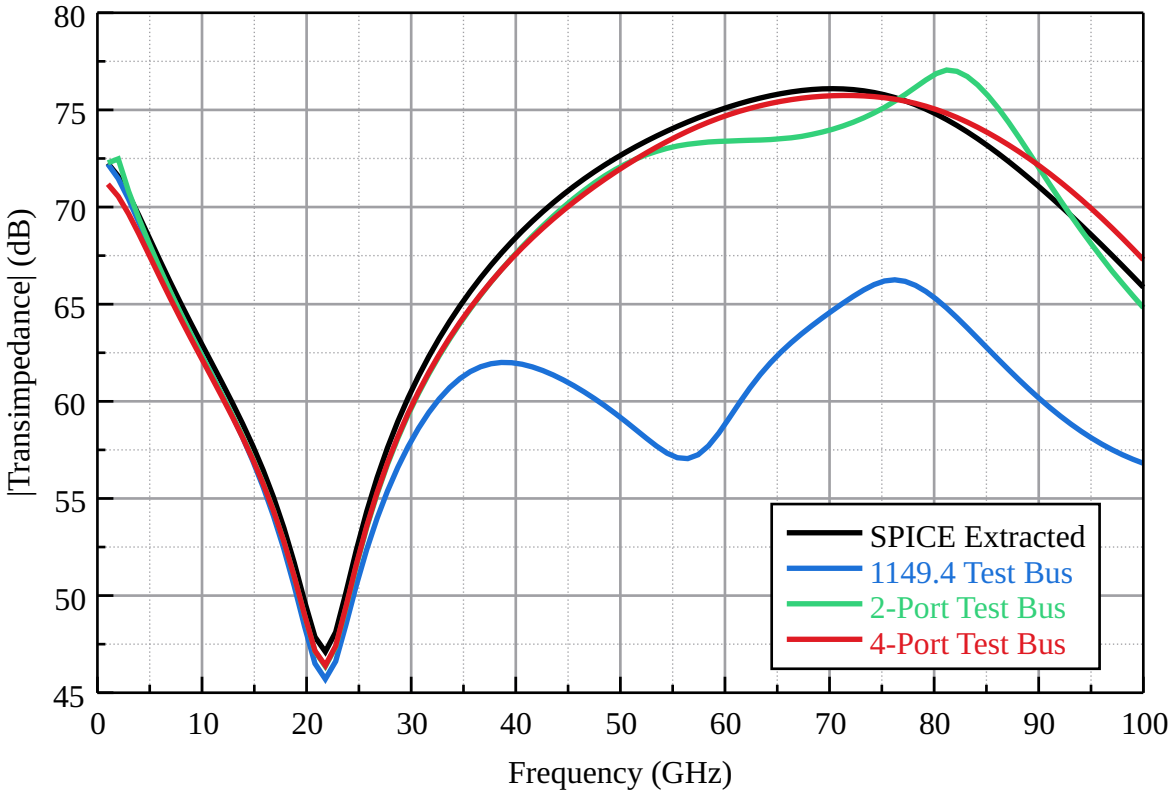


Figure 6.11: Monte Carlo simulation showing the average transimpedance measured by the 1149.4, 2-Port, and 4-Port test buses. Exact SPICE extracted transimpedance is included as a reference.

robustness of the test bus design.

Although the 4-port and 2-port test buses improved the high-frequency measurement performance, they did not perfectly extract the reference value. This is likely due to mismatches in the test bus or deviation of the calibration from their measured values over frequency. Upon replacing the calibration references with an ideal resistor and simulating without mismatches or variations, the 4-port and 2-port test buses perfectly extract the reference transimpedance. This is consistent with the PCB simulation in Section 5.2 that showed the 4-port test bus exactly overlapping the reference. Therefore, the difference seen in the Monte Carlo simulation must come from the variation or non-ideal calibration references. Improving these aspects should improve the overall accuracy of the proposed test buses.

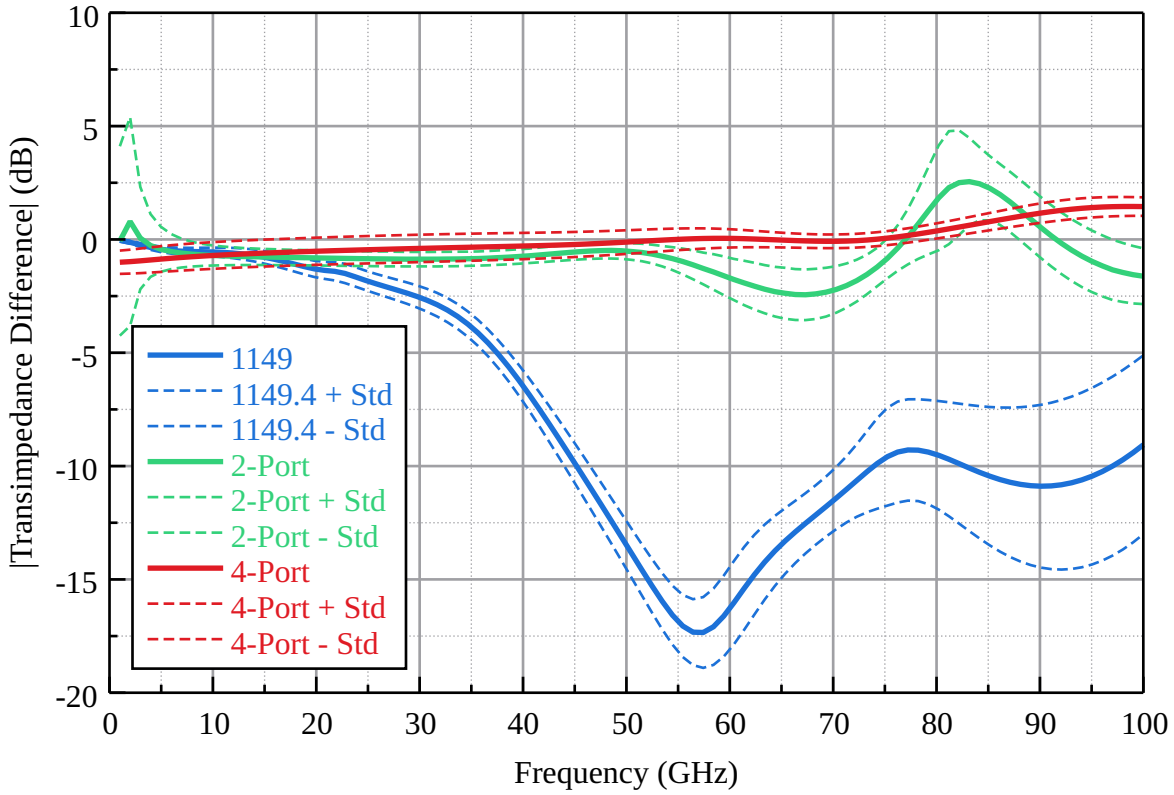


Figure 6.12: Monte Carlo simulation results of the difference between the test bus measured and ideal SPICE extracted transimpedance. Each result is plotted with the average value and ± the standard deviation (Std).

The parts of the proposed test buses that are the most difficult to implement are the calibration references and buffers. The buffers must have close to ideal low-frequency gain to allow the characterization of the calibration references and have good matching between each other. It is difficult to match the DUT buffers with the others because of the ways in which the DUT can affect the buffers differently compared to the references. The calibration references are a very sensitive component to create on-chip. Reducing the resistance of the transistors requires increasing the current, while being careful not to exceed the maximum current rating of the integrated resistors. The calibration references therefore draw a significant amount of power when turned on.

6.4 Summary

With the ability to de-embed any high-frequency errors, it is possible to create an analog test bus that works into the RF and mmWave frequency range. To investigate the high-frequency on-chip implementation, the proposed test buses are designed and simulated in a high-speed BiCMOS technology. Integrating the proposed test buses comes with a unique set of challenges in facilitating the calibration procedure. Current and voltage buffer circuits are powered on/off using carefully placed transmission gates in the biasing circuitry. A sufficient amount of reverse signal is maintained for the 2-port test bus design using a simple topology. The on-chip calibration references use diode-connected BJTs to create a low-impedance reference that also establishes the bias voltage. Monte Carlo simulations that induced process and mismatch variation showed the 4-port and 2-port test buses outperforming 1149.4 at frequencies above 20 GHz.

Chapter 7

Conclusion

The proposed analog test bus theory, simulations, and experiments covered in this thesis are summarized in the following section. Lastly, a detailed discussion on future work is given, including recommendations on future experiments and circuit improvements.

7.1 Summary

Testing is a critical part of the semiconductor manufacturing process to ensure that ICs meet the specifications promised to the customer. Analog and mixed-signal circuit testing is the most difficult, time consuming, and costly type of testing that needs to be performed. Many different test strategies exist for analog and mixed-signal circuits, usually relying on quality test equipment, DfT and BIST strategies, or both. Analog test buses are a simple and versatile strategy that feeds test signals throughout an IC with built-in switches and buses. All previous analog test bus implementations found in the literature are limited in their maximum operating frequency. This problem has prevented analog test buses from being widely adopted and used in high-frequency applications. High-speed test equipment, such as a VNA, is capable of measuring very high-frequency circuits, partly because of their excellent calibration procedure that accounts for errors in the measurement setup.

This thesis proposed an analog test bus structure that integrates calibration references

within the test bus to fully account for the measurement errors introduced by the test bus. Characterizing and de-embedding these errors extends the measurement bandwidth of the test bus. This is possible because the calibration uses a generic 2-port network to model the errors, which means it accounts for not only gain, but also reflections and reverse transmission. The test bus topology is based on current and voltage buffers arranged symmetrically around the DUT and calibration references. The ability to turn the current and voltage buffers on or off determines what the test bus is measuring. 4-port and 2-port versions of the proposed test bus were created, with the 4-port version being the most robust with dedicated input and output ports.

The established VNA calibration algorithm was applied to the proposed test bus to extract the error parameters. To make the 4-port test bus compatible with the algorithm, a conversion was presented and verified to simplify the 4-port error model to the standard 8 error parameters. Part of the proposed test bus structure are the proposed calibration references that integrate within the test bus. A load resistor small-signal equivalent topology is proposed that can be characterized with a low-frequency measurement. An example simulation under ideal conditions showed that 4-port and 2-port test buses can exactly measure the DUT transimpedance even in the presence of high-frequency errors. In contrast, the 1149.4 test bus and its simple gain calibration procedure failed to measure the DUT transimpedance. The simulation verified that with exactly known calibration references and perfectly matching buffer circuits with strong signals, the proposed test bus can extract the high-frequency behavior of the DUT.

To test the proposed test bus, an experiment was designed that implemented the 4-port and 1149.4 test buses on a PCB using discrete components. The goal was to accurately measure the transimpedance of a TIA across the entire frequency range. DIP switches were used to turn on/off the buffer components and the calibration references were created using simple resistors. The test buses were measured using a 2-port VNA and compared to a reference PCB of just the TIA circuit. After measuring and applying the calibration algorithms,

the 4-port test bus more closely tracked the reference measurement for all frequencies. The 1149.4 test bus accurately measured the low-frequency transimpedance, but reported the resonance and roll-off earlier than the 4-port test bus. The experiment verified the ability of the 4-port test bus to correct for high-frequency errors at the edge of the TIA's bandwidth. The results did not match perfectly with the reference measurement due to a practical limitation in matching between buffers and the consistency of the calibration references.

Additional challenges are presented when building the proposed test bus on-chip. A transistor-level design of the proposed test bus in a high-speed BiCMOS process was simulated to evaluate the integration challenges and performance. The current and voltage buffers were created with the same current conveyor circuit that can be turned on/off using transmission gate switches located in the bias circuitry. The buffers met the 2-port test bus reverse signal requirement by keeping the buffer circuit simple and using the coupling capacitance. Diode-connected transistors were used to create the calibration references. These references provided voltage biasing for the buffers and created a stable low-resistance path with as little current consumption as possible. A Monte Carlo simulation was used to induce process and mismatch variations to test performance under non-ideal conditions. The simulation results showed the 4-port and 2-port test bus with errors less than 2.5 dB across the frequency range 0 - 100 GHz. 1149.4 error grows larger than 2.5 dB at the 30 GHz mark. These simulations again verified the ability of the proposed test bus to calibrate for high-frequency errors more accurately than 1149.4 even under mismatch uncertainty.

7.2 Future Work

The content of this thesis is the first time the proposed analog test bus has been built and tested. Given that this is the first time, the scope was kept small and focused on evaluating the test bus's critical ideas. Therefore, there is much potential future work to test the proposed analog test bus in larger experiments and in different applications. In addition,

through this initial experiment, many potential improvements were found that need to be further investigated.

The next practical experiment is to tape-out the proposed analog test bus with multiple DUTs connected to it and experiment with the real-life implementation. The IC simulations in Chapter 6 demonstrate that the proposed test bus can extend the measurement bandwidth up to 100 GHz. One could start with a less extreme frequency requirement with the first tape-out. If the goal is to demonstrate an improvement over 1149.4, one only needs a DUT that will showcase the different calibration procedures and that does not need to be at mmWave frequencies.

This thesis focused on measuring the transimpedance of a TIA. The next experiments should use other kinds of DUTs and measure other parameters such as voltage gain. This will require special attention at the input of the DUT where the current buffer injects the test signal. For the 4-port test bus at low frequencies, the voltage buffer can be used to measure the applied voltage signal. The 2-port test bus does not have this ability and needs the high-frequency calibration to calculate the voltage.

There are multiple potential improvements to the proposed test buses to investigate. Creating accurate and consistent on-chip calibration references is difficult. One could look into calibration references that do not require as much current to obtain a low resistance. Maybe it is best to add a dedicated reference voltage test port so that a simple resistor calibration reference can be used like the PCB experiment.

Further experiments on the ideal calibration reference resistance values are needed. This thesis chose to use 100 - 400 Ω small-signal equivalent values. Low values near the characteristic impedance of the system (50 Ω) were observed to give greater differences in the S-parameter values and better results. Having values go up to 400 Ω was a practical trade-off to be able to build them. A more thorough analysis could find what the idea resistor values are and which combination of them gives the best results.

There is a potential to use an integrated electronic calibration reference instead of the

calibration reference resistors. The proposed test bus would be simplified by only needing a single connection from the test bus for the calibration instead of the three needed now. The most promising strategy is one similar to that presented by Chien and Niknejad [42]. A CMOS transistor is essentially used as a variable load resistor by varying the gate voltage. This strategy would reduce the silicon area of the test bus and the mismatch errors between buffers by removing half of them.

In addition, a more advanced VNA-style calibration technique could be employed that allows for unknown parameters in the calibration error model. This could decouple the parasitic elements that have the greatest impact on the calibration reference performance. Many existing VNA calibration algorithms use this technique to rely on the most accurate parts of their calibration structures.

One of the next experiments should also be a completely CMOS implementation of the proposed analog test bus. The IC simulation in Chapter 6 used a BiCMOS process to push the limits of the test bus to demonstrate its use in potential RF and mmWave applications. There is no reason why the high-level structure could not be used in CMOS applications to extend the measurement bandwidth. A CMOS implementation could use transmission gates instead of buffers as the test buses switchable elements. Creating on-chip calibration references would need to be re-evaluated since the BiCMOS references do not translate directly.

Lastly, there is potential to take advantage of the 4-port to 2-port conversion of the proposed calibration procedure and apply it to some new test structures. Since one does not use a directional coupler to get the incident and reflected signals, maybe the test signal generator and measurement can be moved on-chip.

References

[1] G. W. Roberts, F. Taenzler, and M. Burns, *An Introduction to Mixed-Signal IC Test and Measurement*. The Oxford series in electrical and computer engineering, New York: Oxford University Press, 2nd ed ed., 2012.

[2] "IEEE standard for test access port and boundary-scan architecture," *IEEE Std 1149.1-2013 (Revision of IEEE Std 1149.1-2001)*, pp. 1–444, 2013.

[3] "IEEE standard for a mixed-signal test bus," *IEEE Std 1149.4-2010 (Revision of IEEE Std 1149.4-1999)*, pp. 1–116, 2011.

[4] J. Hannu, J. Häkkinen, J.-V. Voutilainen, H. Jantunen, and M. Moilanen, "Current state of the mixed-signal test bus 1149.4," *Journal of Electronic Testing*, vol. 28, pp. 857–863, Dec. 2012.

[5] S. Sunter, "The P1149.4 mixed signal test bus: costs and benefits," in *Proceedings of 1995 IEEE International Test Conference (ITC)*, (Washington, DC, USA), pp. 444–450, Int. Test Conference, 1995.

[6] S. Sunter, K. Filliter, W. Joe, and P. McHugh, "A general purpose 1149.4 IC with HF analog test capabilities," in *Proceedings International Test Conference 2001 (Cat. No.01CH37260)*, pp. 38–45, Nov. 2001. ISSN: 1089-3539.

[7] K. P. Parker, *The Boundary-Scan Handbook*. Cham: Springer International Publishing, 2016.

[8] A. Shrivastava and G. Banerjee, "Analog probe module (APM) for enhanced IC observability: From concept to application," *IEEE Transactions on Very Large Scale In-*

tegration (VLSI) Systems, vol. 32, pp. 2355–2367, Dec. 2024. Conference Name: IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

[9] V. A. Zivkovic, F. Van Der Heyden, G. Gronthoud, and F. De Jong, "Analog test bus infrastructure for RF/AMS modules in core-based design," in *2008 13th European Test Symposium*, (Verbania), pp. 27–32, IEEE, May 2008.

[10] P. Syri, J. Hakkinen, and M. Moilanen, "IEEE 1149.4 compatible ABMs for basic RF measurements," in *Design, Automation and Test in Europe*, (Munich, Germany), pp. 172–173, IEEE, 2005.

[11] J. Hakkinen, P. Syri, J.-V. Voutilainen, and M. Moilanen, "A frequency mixing and subsampling based RF-measurement apparatus for IEEE 1149.4," in *2004 International Conferce on Test*, (Charlotte, NC, USA), pp. 551–559, IEEE, 2004.

[12] Chauchin Su and Yue-Tsang Chen, "Intrinsic response extraction for the removal of the parasitic effects in analog test buses," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, pp. 437–445, Apr. 2000.

[13] J. P. Dunsmore, *Handbook of Microwave Component Measurements: With Advanced VNA Techniques*. Hoboken, NJ: John Wiley & Sons, Inc, 2nd ed., 2020.

[14] N. Shoaib, *Vector Network Analyzer (VNA) Measurements and Uncertainty Assessment*. PoliTO Springer Series, Cham: Springer International Publishing, 2017.

[15] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. Upper Saddle River, NJ: Prentice Hall, 2nd ed., 1997.

[16] D. Rytting, "Network analyzer error models and calibration methods," Sept. 1998.

[17] A. Ferrero, F. Sampietro, and U. Pisani, "Multiport vector network analyzer calibration: a general formulation," *IEEE Transactions on Microwave Theory and Techniques*,

vol. 42, pp. 2455–2461, Dec. 1994. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[18] M. Wollensack, J. Hoffmann, D. Stalder, J. Ruefenacht, and M. Zeier, "VNA tools II: Calibrations involving eigenvalue problems," in *2017 89th ARFTG Microwave Measurement Conference (ARFTG)*, (Honololu, HI, USA), pp. 1–4, IEEE, June 2017.

[19] G. Engen and C. Hoer, "Thru-Reflect-Line: An improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, pp. 987–993, Dec. 1979. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[20] A. Rumiantsev and N. Ridler, "VNA calibration," *IEEE Microwave Magazine*, vol. 9, pp. 86–99, June 2008.

[21] D. Williams, C. Wang, and U. Arz, "An optimal multiline TRL calibration algorithm," in *IEEE MTT-S International Microwave Symposium Digest, 2003*, vol. 3, pp. 1819–1822 vol.3, June 2003. ISSN: 0149-645X.

[22] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM calibrations with automatic determination of load inductance," in *36th ARFTG Conference Digest*, vol. 18, pp. 57–63, Nov. 1990.

[23] X. Shang, N. M. Ridler, J. Ding, and M. Geen, "Introductory guide to making Planar S-parameter measurements at millimetre-wave frequencies," tech. rep., National Physical Laboratory, Jan. 2021.

[24] A. Rumiantsev, *On-Wafer Calibration Techniques Enabling Accurate Characterization of High-Performance Silicon Devices at the mm-Wave Range and Beyond.* New York: River Publishers, 1 ed., Sept. 2022.

[25] D. F. Williams, P. Corson, J. Sharma, H. Krishnaswamy, W. Tai, Z. George, D. Ricketts, P. Watson, E. Dacquay, and S. P. Voinigescu, "Calibration-kit design for millimeter-wave silicon integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, pp. 2685–2694, July 2013.

[26] A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," in *2008 72nd ARFTG Microwave Measurement Symposium*, (Portland, OR, USA), pp. 132–136, IEEE, Dec. 2008.

[27] D. F. Williams, P. Corson, J. Sharma, H. Krishnaswamy, W. Tai, Z. George, D. S. Ricketts, P. M. Watson, E. Dacquay, and S. P. Voinigescu, "Calibrations for millimeter-wave silicon transistor characterization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, pp. 658–668, Mar. 2014. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[28] C.-C. Huang, H.-H. Hsu, and G. C. Guu, "CMOS device de-embedding without impedance standard substrate calibration for on-wafer scattering parameter measurements," in *2012 Asia Pacific Microwave Conference Proceedings*, (Kaohsiung, Taiwan), pp. 959–961, IEEE, Dec. 2012.

[29] C.-C. Huang, "Accurate and efficient self-calibration algorithm of broadband on-wafer scattering-parameter measurements for production test applications up to 110 GHz," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, pp. 990–998, June 2017.

[30] Xiaoyun Wei, Guofu Niu, S. Sweeney, Qingqing Liang, Xudong Wang, and S. Taylor, "A General 4-Port Solution for 110 GHz On-Wafer Transistor Measurements With or Without Impedance Standard Substrate (ISS) Calibration," *IEEE Transactions on Electron Devices*, vol. 54, pp. 2706–2714, Oct. 2007.

[31] K. H. K. Yau, I. Sarkas, A. Tomkins, P. Chevalier, and S. P. Voinigescu, "On-wafer S-parameter de-embedding of silicon active and passive devices up to 170 GHz," in *2010 IEEE MTT-S International Microwave Symposium*, (Anaheim, CA, USA), pp. 600–603, IEEE, May 2010.

[32] "User Characterization: Electronic Calibration Feature Allows Users to Customize to Specific Needs - White Paper," tech. rep., Keysight Technologies, 2014.

[33] "Electronic vs. Mechanical Calibration Kits: Calibration Methods and Accuracy - White Paper," tech. rep., Keysight Technologies, 2014.

[34] D. Williams, A. Lewandowski, D. LeGolvan, R. Ginley, C.-M. Wang, and J. Splett, "Use of electronic calibration units for vector-network-analyzer verification," in *2009 74th ARFTG Microwave Measurement Conference*, (Broomfield, CO, USA), pp. 1–8, IEEE, Nov. 2009.

[35] J. A. Jargon, D. F. Williams, T. M. Wallis, D. X. LeGolvan, and P. D. Hale, "Establishing traceability of an electronic calibration unit using the NIST Microwave Uncertainty Framework," in *79th ARFTG Microwave Measurement Conference*, pp. 1–5, June 2012.

[36] J. Stenarson, C. Eio, and K. Yhland, "A calibration procedure for electronic calibration units," in *84th ARFTG Microwave Measurement Conference*, (Boulder, CO), pp. 1–6, IEEE, Dec. 2014.

[37] M. Abramowicz and A. Lewandowski, "Electronic calibration unit for DC-8 GHz vector-network-analyzer measurements," in *2016 21st International Conference on Microwave, Radar and Wireless Communications (MIKON)*, (Krakow, Poland), pp. 1–4, IEEE, May 2016.

[38] L. Xie, M. F. Bauwens, S. Nadri, A. Arsenovic, M. E. Cyberey, A. W. Lichtenberger, N. S. Barker, and R. M. Weikle, "Electronic Calibration for Submillimeter-Wave On-

Wafer Scattering Parameter Measurements Using Schottky Diodes," *IEEE Transactions on Terahertz Science and Technology*, vol. 10, pp. 583–592, Nov. 2020.

[39] Chien, Jun-Chau and A. M. Niknejad, "A single-element CMOS-based electronic de-embedding technique with TRL level of accuracy," in *2015 IEEE MTT-S International Microwave Symposium*, (Phoenix, AZ, USA), pp. 1–4, IEEE, May 2015.

[40] J.-C. Chien, A. Arbabian, and A. M. Niknejad, "A Single- Element VNA Electronic Calibration in CMOS," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, (Philadelphia, PA), pp. 1304–1307, IEEE, June 2018.

[41] J.-C. Chien, A. Arbabian, and A. M. Niknejad, "A dual-element VNA electronic calibration in CMOS," in *2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, (Anaheim, CA), pp. 71–74, IEEE, Jan. 2018.

[42] Chien, Jun-Chau and Niknejad, Ali M., "A Single-Element CMOS-LRRM VNA Electronic Calibration Technique," in *2022 99th ARFTG Microwave Measurement Conference (ARFTG)*, (Denver, CO, USA), pp. 1–4, IEEE, June 2022.

[43] J.-C. Chien, "Millimeter-wave VNA Calibration using a CMOS Transmission Line with Distributed Switches," in *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 283–286, June 2022. ISSN: 2375-0995.

[44] Markus Zeier, Djamel Allal, and Rolf Judaschke, "Guidelines on the evaluation of vector network analysers (VNA)," *EURAMET Calibration Guide*, vol. 3, 2018.

[45] F. Seguin, B. Godara, F. Alicalapa, and A. Fabre, "2.2 GHz All-n-p-n Second-Generation Controlled Conveyor in Pseudoclass AB Using 0.8-/spl mu/m BiCMOS Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, pp. 369–373, July 2004.

[46] M. B. Babar, *Techniques for Simultaneous Optimization of Transimpedance Gain and Bandwidth for the Development of High-Speed, Low-Noise and Area-Efficient Transimpedance Amplifier Designs*. M.Eng., McGill University (Canada), Canada – Quebec, CA, 2023. ISBN: 9798342119207 Publication Title: ProQuest Dissertations and Theses.