# The Design of Low-Voltage High-Frequency CMOS LC-Based Oscillators

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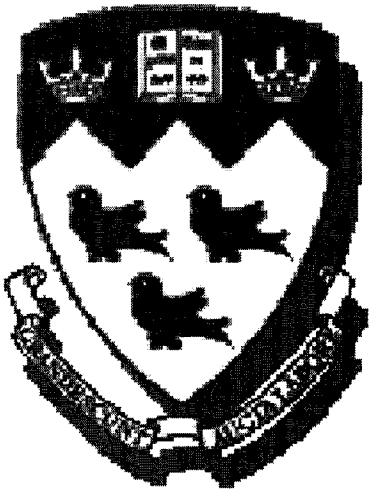

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# Abstract

With the rapidly accelerating world of communications, there has been an increased interest in monolithic integration. CMOS technology has become a natural candidate for system integration being the technology of choice for digital circuit implementation.

This thesis presents several LC-based CMOS voltage controlled oscillators, demonstrating the capability and benefits of the technology in high-frequency designs. Through optimization of a simple LC oscillator, a 4 GHz circuit operating at a supply voltage as low as 0.85 V was implemented and measured. Optimization of a symmetric LC oscillator realized frequencies of 10 and 12.5 GHz. A novel oscillator architecture combining both high-frequency and low-voltage operation is also proposed in this thesis. This new oscillator structure allows for two tuning mechanisms, thus increasing the tuning range of the oscillator. The optimization of these designs was made without sacrificing other essential requirements of the oscillators such as phase noise. This is demonstrated by achieving comparable results to those reported in state-of-the-art publications.

# Résumé

À cause de la croissance rapide au monde de communication, il y a eu un intérêt accru pour l'intégration monolithique des circuits. La technologie CMOS est devenue une candidate naturelle pour l'intégration de ces systèmes étant la technologie universellement choisie pour l'implementation des circuits digitales.

Cette thèse présente plusieurs oscillateurs LC contrôlés par potentiel électrique et fabriqués en CMOS, montrant les pouvoirs et les bénéfices de la technologie dans la conception des circuits à haute fréquence. En optimisant un simple oscillateur LC, un circuit à 4 GHz qui nécessite un potentiel aussi bas que 0.85 V a été conçu et mesuré. Et en optimisant un oscillateur LC symétrique, des oscillations de 10 et 12.5 GHz ont été obtenus. Une nouvelle architecture qui combine l'opération à haute fréquence ainsi que l'opération à bas potentiel électrique est proposée dans cette thèse. Ce nouveau oscillateur permet deux mécanismes indépendants pour contrôler la fréquence, et en conséquence la bande de fréquence adaptable est augmentée. L'optimisation de ces circuits a été fait sans avoir sacrifier les autres exigences du oscillateur, tel le bruit de phase.

# Acknowledgments

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CHAPTER 1

# Introduction

## 1.1 Motivation

Data communication is now replacing the standards of the traditional voice and video networks. The latter have simply become integrated types of data that benefit from the tremendous growth in today's broadband data communication systems. As data transfer rates continue to soar, the mandate to build faster and more efficient networks is driving the research in areas such as wireless and optical communications. In the wireless domain, trends such as low cost and higher bandwidth solutions are clearly observed through the latest literary publications [1]-[27]. The need for low cost solutions is manifested in the interest in monolithic integration of the Radio Frequency (RF) front ends alongside the digital cores in standard CMOS processes, whereas the quest for higher bandwidth is achieved by increasing the frequency of operation of the wireless systems in question. Over the last few years, wireless applications were developed at the 900 MHz and 1.8 GHz bands [1][8], then followed by ones at 2.4 GHz [3][12], and the continuous increase in communications

speed has recently motivated the design and implementation of RF circuits in the 5-6 GHz range [2][4], for applications such as the wireless LAN systems in the US (IEEE 802.11a standard for the FCC unlicensed national information infrastructure, the U-NII band), and the European High Performance Radio LAN (HIPERLAN), which allow a higher bandwidth and data rates for wireless data networks. New wireless applications targeting the last mile data distribution in WAN (Wide Area Networks) are also being deployed, such as MMDS (Multi-channel Multi-point Distribution Service) and LMDS (Local Multi Point Distribution Service). The latter makes use mainly of millimeter-wave frequencies ranging from 23 to 43 GHz in North America.

The Voltage Controlled Oscillator (VCO) is a critical building block in communication systems: It is used for frequency synthesis, and up and down-conversion in transceivers (transmitters-receivers), where it is known as the Local Oscillator (LO). LC-based oscillators are predominantly used for RF applications due to their lower phase noise in comparison to ring and relaxation oscillators. In the millimeter-wave range, other resonators are commonly used, such as DRO's and CRO's (dielectric resonators and coaxial resonators).

In the past few years, VCO's have become a very popular topic of research as the move to monolithic system implementation is progressively being enabled by the technological progress of CMOS processes. The limiting factor in monolithic CMOS VCO implementations remains the phase noise. This is mainly due to the low quality factors (Q) of the achievable LC-tanks in a standard CMOS process, which is in fact predominantly limited by the performance of the integrated spiral inductors [28][31]. Integrated inductors exhibit losses at many levels, which makes modeling of these

passive devices a very challenging task. Several solutions have been reported to improve the phase noise in CMOS VCO's: (i) Cascading of resonators in a ring like architecture, thus increasing the order of the resonator/filter which performs the noise shaping [13]; (ii) using symmetric topologies which tend to minimize the upconverted flicker noise [12]; (iii) and optimizing the integrated inductor layout, which is essential in all designs. Other parameters such as increasing the tuning range and reducing the power consumption are also topics of interest in the implementation of CMOS VCO's.

This thesis will present several high frequency VCO's implemented completely in standard CMOS processes, demonstrating their performance and proving their feasibility using CMOS technologies. A novel architecture, considerably reducing the required power supply voltage for high frequency CMOS VCO's, will also be presented, once again iterating a performance advantage of the CMOS implementation. The obtained results encourage the concept of full system integration on a single chip. This is the ultimate industrial target for several reasons, some of them being: reducing assembly cost, improving yield, reducing the size and weight of wireless products, and minimizing the power consumption of battery operated devices.

## 1.2 Technology Assessment

The goal of several semiconductor suppliers is to permit the integration of the RF front end with the digital baseband on a single chip. This would allow the delivery of a single radio on chip to the world of communications. CMOS technology is slowly moving up the frequency ladder with the shrinking device features and the smaller device parasitics [19]. The technology is attractive from integration, power, and

cost stand points. With CMOS geometries scaling below 0.18 μm, RF solutions are moving away from the multiple technology approach towards a single, low-cost, high-volume process. Different foundries are starting to provide processes which are specifically tailored for RF design and production.

The effort to tailor CMOS processes for RF integration is being driven by the telecommunications and wireless applications which are continually demanding more functionality from smaller spaces without draining battery power or penalizing the user with reduced performance. The technology has already proved its viability in the low gigahertz range of the RF spectrum, taking away some of the market share from GaAs and Bipolar technologies. Currently, it is being pushed to compete for applications reaching 6 GHz in operation [14][15]. It is important to note however that CMOS technology is facing serious competition in the low gigahertz range for system integration by another silicon based technology: BiCMOS SiGe (Silicon Germanium) is rapidly evolving and showing significant potential in terms of performance, integration, and cost. In the past ten years it has evolved into a reliable process, comparable in simplicity of fabrication to current CMOS processes with the exception of a few extra processing steps. It possesses direct advantages over CMOS technology such as its low $1/f$ noise, which is critical for the design of low phase noise oscillators, as well as the availability of deep trench isolation which permits the integration of different circuits on the same die.

High quality passive elements (resistors, capacitors, and inductors) which are required for transistor biasing and monolithic impedance matching networks are key to realizing a viable RF and microwave circuit. High quality passives are increasingly

being demonstrated in silicon. Precision resistors with nearly zero-temperature coefficient and low parasitic capacitance can be made from heavily doped polysilicon on oxide. High quality factor (Q) precision capacitors can be made using the upper level of multi-level metallization in a metal-insulator-metal (MIM) structure. High Q inductors are the most challenging passives to build in silicon, but significant progress has been made through careful design and optimization [29]. Recent addition of low-resistance copper for interconnects shows promise for improving the low frequency losses.

For higher frequency microwave and millimeter-wave systems, low-loss transmission lines are clearly required. The lack of suitable transmission lines in silicon technology is a major show stopper for realizing silicon-based MMIC's (Monolithic Microwave Integrated Circuits). After all, a semi-insulating silicon substrate at room temperature does not exist, and high-resistivity silicon is difficult to make, costly, and significantly complicates conventional silicon fabrication. However, recent work indicates that thick (e.g. >10μm) benzo-cyclo-butene (BCB) polymers deposited directly on top of the processed silicon wafer and followed by gold interconnect deposition can yield high-quality transmission lines [18]. This does not come for free, but it clearly provides a path for integrating SiGe technology with future microwave and millimeter-wave transmission systems. Issues such as signal isolation between the power amplifier at the output and the low-noise amplifier at the input still add significant complexity to full monolithic integration.

This thesis does not cover the issues of complete integration on a CMOS substrate, but it demonstrates the capability of the technology to support the production

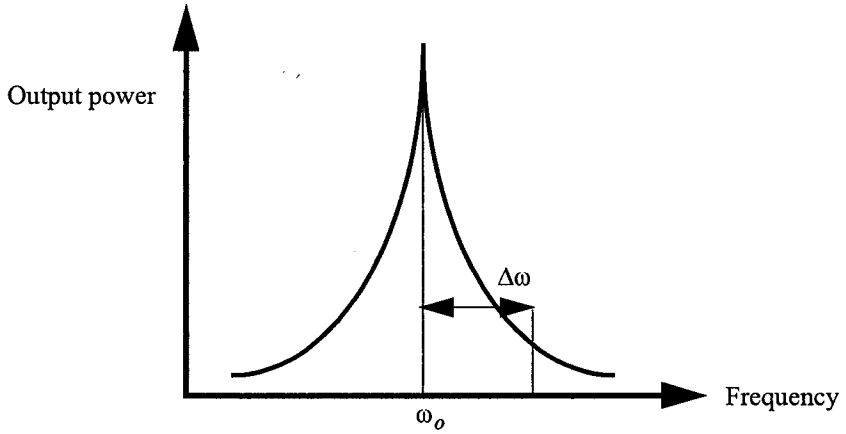


**Fig. 1-1:Frequency domain output showing carrier tone with sidebands.**

of high frequency (up to 12.5 GHz) integrated oscillators [25].

## 1.3 VCO Performance Metrics

Several parameters define the performance of a VCO, the most critical one being the oscillator phase noise around the center frequency. Oscillator phase noise needs to be minimized to avoid corrupting the mixer-converted signals by close interfering tones. The other key specifications are tunability, power consumption, the power supply required, and the frequency of oscillation.

### 1.3.1 Phase noise

Ideally, the spectral output of an oscillator would take on the shape of a Dirac impulse, where the output voltage of an ideal oscillator operating at a frequency $\omega_o$ can be expressed as $V_{out}(t) = A \times \sin(\omega_o t + \theta)$, where $A$ is the amplitude and $\theta$ is a fixed phase reference. In reality, however, neither $A$ nor $\theta$ are fixed: Both parameters vary as a function of time, which results in an output governed by $V_{out}(t) = A(t) \times \sin(\omega_o t + \theta(t))$. Due to the time variations of those parameters,

rather than all of the power being concentrated at a single frequency, some power is distributed in frequency bands on both sides of $\omega_o$, known as side-bands, as shown in Fig. 1-1. Note that, in high quality, well designed oscillators, the amplitude is kept constant, thus the variation in $A$ is small and most of the phase noise can be attributed to the change of $\theta$ with respect to time.

Phase noise is determined by examining a unit bandwidth at a frequency offset $\Delta\omega$ from the carrier $\omega_o$. The noise power in the band is calculated, and the result is divided by the carrier power. This is known as the Single Side Band (SSB) spectral noise density which is quantified in dB with respect to the carrier per Hertz [dBc/Hz]:

$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{\text{noise power in a 1-Hz bandwidth at } \omega_o + \Delta\omega}{\text{carrier power}}\right). \qquad (1.1)$$

Phase noise is of critical importance in a LO used to downconvert a signal in the receive path, as well as to upconvert a signal in the transmit path. The reasoning is

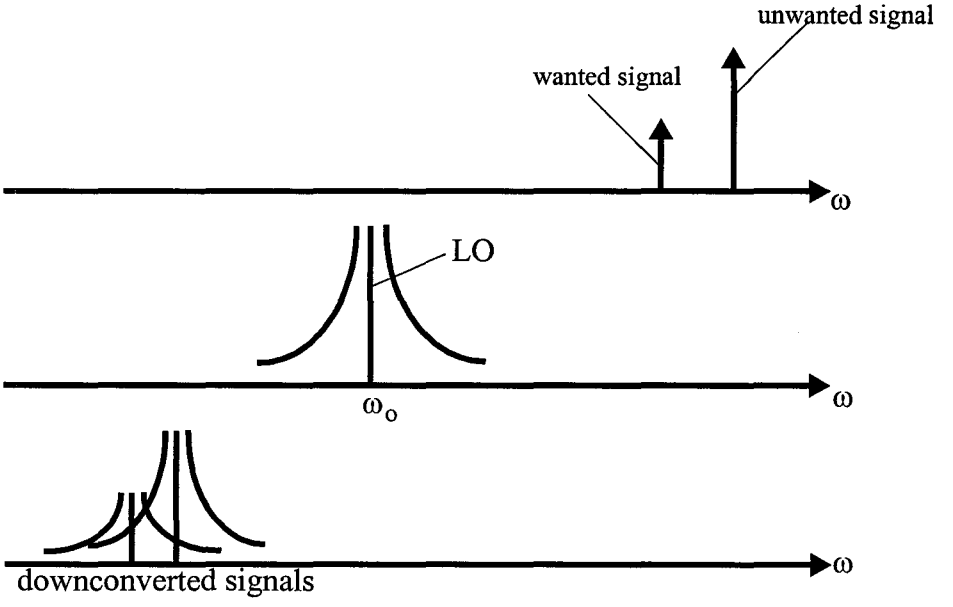


**Fig. 1-2:Effect of oscillator phase noise in a receiver.**

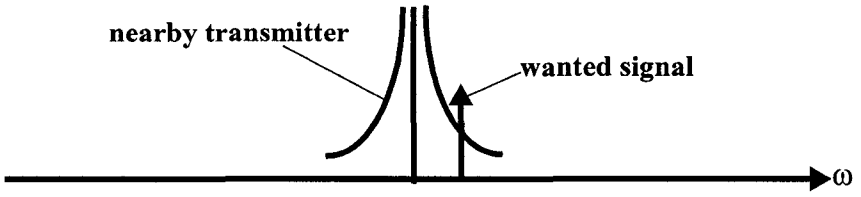


**Fig. 1-3:Effect of oscillator phase noise in a transmitter.**

slightly different in each case. In the receiver, as a multitude of signals may exist in the spectrum, the desired signal may be present at a small power level, while a close by interferer might be present at a larger power level. When the two signals are downconverted, they will overlap causing the signal of interest to be largely masked by the sideband of the unwanted signal, as shown in Fig. 1-2. The acceptable phase noise level for each system varies depending on the weakest anticipated signal of interest, the expected highest power of an unwanted signal in an adjacent channel, as well as the required SNR (Signal to Noise Ratio) required for the application's modulation scheme. In a transmitter, the LO should ideally produce a signal with the power concentrated at a single frequency. The sidebands of a strong signal would corrupt weaker close by signals of interest to other receivers, as shown in Fig. 1-3.

### 1.3.2 Tuning range and linearity

The tuning range is the amount of change in frequency that can be achieved by the oscillator on either side of the nominal oscillation frequency. A tuning range is not necessarily needed or available in all oscillators; some are operated only at a fixed frequency, such as crystal oscillators. Tuning can be used for covering the frequency range of an application (i.e. different channels), as well as for compensating for frequency drifts caused by variations in the manufacturing process or temperature. It

can be achieved through different mechanisms depending on the range required. Some applications might use several oscillators to cover the entire frequency band of interest. Ring oscillators (section 2.2.3) might use some logic and switches to vary the length of the inverter chain to modify the frequency of operation. Others, might use trimmable capacitors, if a fixed frequency is the goal of the implementation. Other mechanisms of tuning in integrated oscillators include varactors which are capacitors that vary based on a biasing control voltage, and current tuning which varies the parasitics of the devices used in the oscillator and results in a change in frequency. The work presented in this thesis makes use of several types of varactors, and the novel architecture proposed in chapter 4 employs two tuning mechanisms to increase the tuning range.

Finally, the tuning linearity describes how proportional is the frequency change to the variation performed to the tuning mechanism (current/voltage). Wide linearity simplifies the design of phase locked loops (PLL), where the VCO gain should be constant.

### 1.3.3 Power consumption

DC power consumption is a function of the voltage supply and of the total current used to bias the oscillator. The main motivation for reducing the power consumption is prolonging the lifetime of a battery in a mobile device. Reducing either the DC voltage or current in oscillators might have several consequences on a design such as a loss of the output power of the produced signal, which in turn might affect the phase noise of the oscillator, or can result in a smaller dynamic range, which would result in an increased distortion and harmonics. Therefore, power consumption is a

major issue in highly integrated systems. This thesis presents several designs and architectures that are optimized to minimize power consumption while maintaining a performance level comparable to conventional implementations.

### 1.3.4 Complete integration

Traditionally, the front end of a wireless system is implemented using an analog process such as Bipolar or GaAs (Galium Arsenide), whereas the digital IF (Intermediate Frequency) functionality is designed using a standard CMOS process suitable for high integration of digital circuits. To satisfy the stringent requirements of telecommunication applications, one has to use very high quality resonators such as crystal resonators or DRO's. These methods force a board-level solution where an IC, containing the active circuitry, would have to be connected to the external resonator. Although this provides the required performance, it becomes very costly in manufacturing. The placement of the magnetic resonator, also known as the puck, in a DRO requires high mechanical accuracy, and the tuning of the puck to settle on the frequency of interest is a time consuming process. Other solutions can eliminate the need for a board level implementation: The use of trimmable capacitors is one option which requires very expensive equipment to trim away parts of the capacitor plate. The use of bonding wires between circuit nodes, or the use of package bond wires as inductors forming part of the resonator, also offers a single chip solution, but suffers from the problem of repeatability. Today, research is proving that a single chip solution on silicon might be possible with the use of new circuit design techniques which enhance the quality of the integrated resonators [29]. For the RF components, this

requires pushing the capabilities of the active devices of the technology to its limits; but what seems more difficult is managing the design and modeling of the non-ideal passive structures on the lossy silicon substrate.

Although this trend towards higher integration makes the design of the front end more challenging, it provides advantages in terms of system architecture, and more importantly, significant cost reduction in manufacturing and assembly. Hence, the industry of high volume wireless products targets complete integration of RF and digital building blocks, which puts stringent demands on the performance and consistency of both active and passive components of CMOS technologies.

## 1.4 Thesis Outline

Through the different designs presented in the thesis, it will be shown that state-of-the-art standard CMOS processes can permit high frequency of operation, as well as low voltage usage. This chapter detailed the motivation behind the work to be presented and it discussed the technology requirements for the viability of CMOS in the world of RF applications. It also discussed the main performance/characteristic requirements of an oscillator as well as their impact on different design and implementation issues.

The second chapter of this thesis introduces the basic principles of oscillator functionality: The different configurations of integrated oscillators are presented, and the different design approaches are discussed. Finally, details of phase noise considerations in the design of LC oscillators is covered. The third chapter presents the design methodology and optimization of several oscillators that range from 4-12.5 GHz

in frequency. The chapter focuses on optimization for achieving both high frequency and very low voltage operation. The fourth chapter presents a novel architecture for an LC CMOS VCO that is capable of very high frequency operation at sub-1 volt supply. The conception of the new architecture is discussed, as well as its main advantages and limitations. The measured results of two prototypes at 9 and 10 GHz frequencies are also be presented in this chapter. Finally, a conclusion summarizing the work done and the main achievements of the implemented oscillators are given in a concluding chapter.

## 1.5 List of Contributions

### 1.5.1 Low voltage VCO's

Two circuits optimized for low supply voltage were implemented in 0.25 and 0.35 μm CMOS processes. The VCO's were measured at 4 and 5 GHz using 0.85 and 1 volt power supplies, respectively. The VCO's function at the lowest supply voltages within their frequency range (at the time of publication). The results were published as part of the following papers:

1- A. H. Mostafa, M. N. EL-Gamal, and R. A. Rafla, "CMOS 5-10 GHz Oscillators for Low Voltage RF Applications," *MidWest Symposium on Circuits and Systems (*MWSCAS), August 2000.

2- A. H. Mostafa and M. N. EL-Gamal, "A Fully Integrated Sub-1V 4 GHz CMOS VCO, and a 10.5 GHz Oscillator," *European Solid State Circuits Conference (ESSCIRC)*, September 2000.

3- A. H. Mostafa, M. N. EL-Gamal, and R. A. Rafla, "CMOS 4-12.5 GHz Oscillators for Low Voltage RF Applications," *Transactions on Circuits and Systems*, submitted October 2000 (invited paper).

### 1.5.2 High frequency VCO's

Two VCO designs were optimized for high frequency operation and implemented in a 0.35 μm CMOS process. The VCO's were measured at frequencies of 10 and 12.5 GHz. The 12.5 GHz VCO was reported as the highest frequency CMOS VCO (at the time of publication) in the following publication:

1- A. H. Mostafa and M. N. EL-Gamal, "A 12.5 GHz Back-Gate Tuned CMOS Voltage Controlled Oscillator," *IEEE International Conference on Electronics, Circuits and Systems (*ICECS), December 2000.

### 1.5.3 A new architecture for high frequency and low voltage VCO's

A novel VCO architecture was developed to allow high frequency operation, while considerably reducing the supply voltage required. Two prototypes were designed and implemented in a 0.18 μm CMOS process. The prototypes were measured to operate at 9 and 10 GHz from a 1 V supply. This was reported in the following publication:

1- A. H. Mostafa and M. N. EL-Gamal, "A CMOS VCO Architecture Suitable for Sub-1 Volt High-Frequency (8.7-10 GHz) RF Applications," *International Symposium on Low Power Electronics and Design ISLPED'01*, August 2001.

*Note: In all the mentioned co-authored publications, Mr. Rafla contributed in the inductor design and optimization, Dr. El-Gamal supervised the work and the author of this thesis was responsible for the design, implementation and testing of the VCO's.*

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CHAPTER 2

# Oscillator Theory

## 2.1 Introduction

Oscillators are used extensively in electronic systems. Their requirements vary significantly depending on their application. The targeted frequency of operation and the required phase noise have a large impact on the choice of oscillator topology as well as on the design approach and implementation of the oscillator. For example a lower frequency design (i.e. below 1GHz) can be implemented using ring or relaxation oscillators, whereas, LC type oscillators are generally used at higher frequencies. However, with the continuously shrinking channel length, higher frequencies are achievable with the non-LC type oscillators, but the LC type oscillators are still preferred in communication systems due to their better phase noise characteristics. This chapter presents different known types of oscillators, then it presents the general theory of LC oscillator design and the different design approaches in LC oscillator design. Finally, the last section of this chapter identifies the noise sources in LC oscillators and a known method for noise estimation in these commonly used circuits.

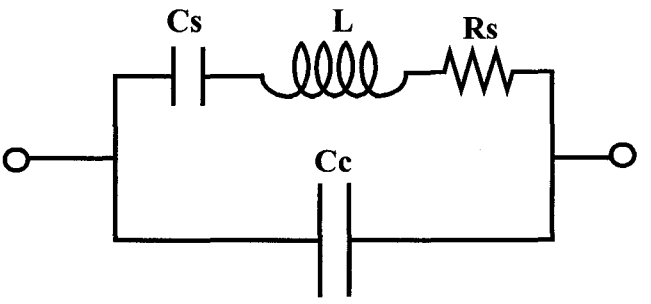


**Fig. 2-1:Electrical model of a crystal oscillator.**

## 2.2 Oscillator Types

### 2.2.1 Crystal oscillators

Crystal oscillators are the best known and most stable oscillators. Their low noise and good stability make them suitable to be used as the reference signal source in a frequency synthesizer. Their resonance is based on the characteristics of a crystal. The electric model of a crystal is shown in Fig. 2-1, and a plot showing the impedance of a crystal versus frequency is given in Fig. 2-2. It has two resonance frequencies: The series resonance occurs first when $C_s$ and L cancel each other out, resulting in a very low overall impedance. This happens at frequency $\omega_s$ given by:

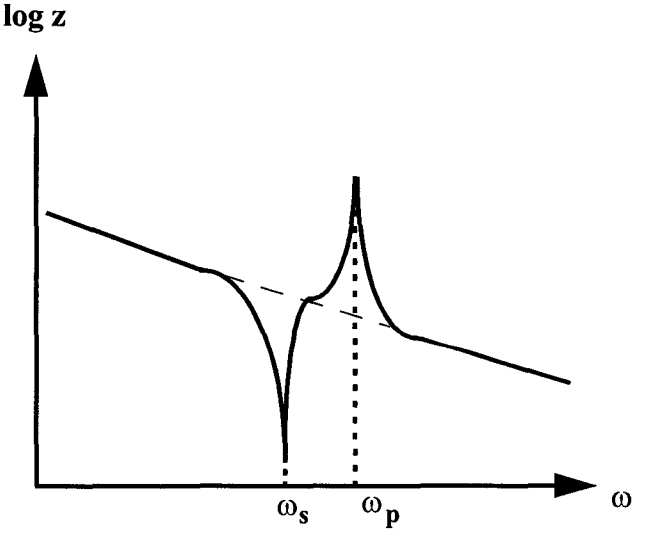


**Fig. 2-2:Impedance of crystal oscillator with respect to frequency.**

$$\omega_s = 1/(\sqrt{LC_s}).$$

Parallel resonance takes place when the impedance of $C_c$ is exactly the complex conjugate of the impedance provided by L and $C_s$. The total impedance of the resonator is infinite in this case, and the resonance frequency $\omega_p$ is given by:

$$\omega_p = (1/(\sqrt{LC_s})) \cdot \sqrt{1 + C_s/C_c}.$$

Using a single transistor as the active element, only two oscillator configurations are possible: The first configuration is the one-pin oscillator, where the crystal is placed between the gate of the device and ground, thus requiring only a single external pin. This configuration is favored in large chips where pin count should be minimized. The second configuration is known as the Pierce oscillator, which has the crystal placed between the gate and the drain of the active device. Although the circuit requires two separate pins, it is known to provide better frequency stability [1].

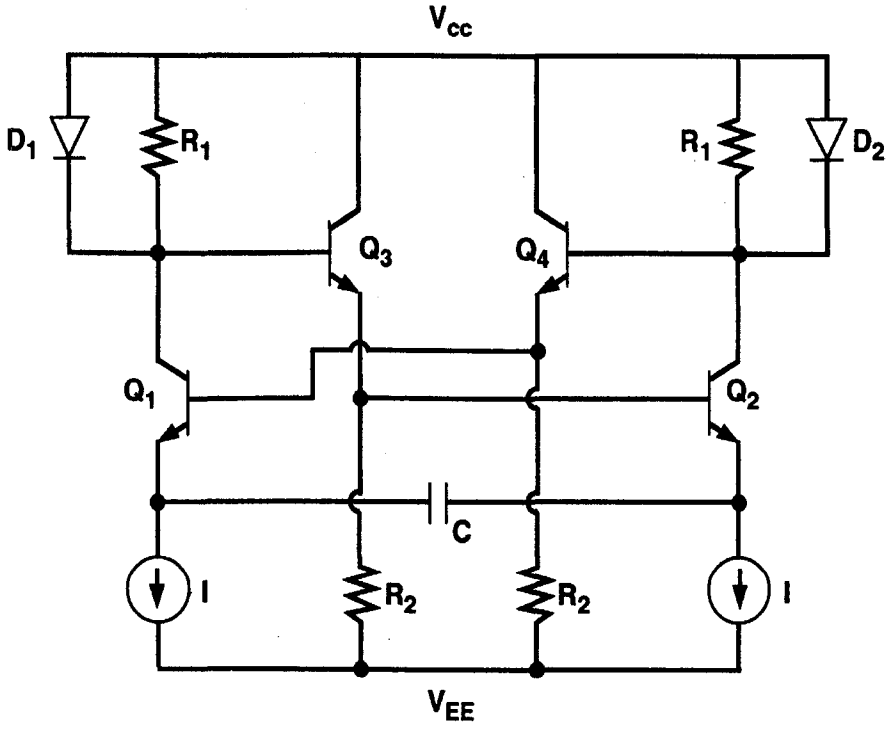


**Fig. 2-3:Emitter coupled multivibrator VCO [10].**

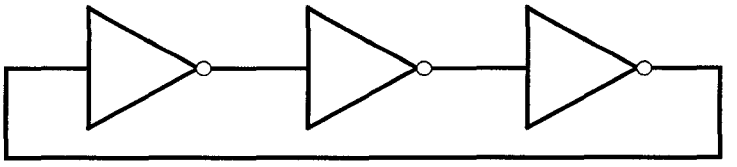

**Fig. 2-4:Basic ring oscillator: three inverters.**

### 2.2.2 Relaxation oscillators

Relaxation oscillators are mainly used in monolithic implementations. They are capable of relatively high frequency of operation, but are limited in terms of their phase noise performance. The basic circuit for a relaxation oscillator is that of an emitter coupled multivibrator [2-3] (Fig 2-3). A CMOS implementation was demonstrated in [4]. Its concept of operation relies on the switching of two transistors connected at their emitters using a timing capacitor that is charged and discharged by two current sources. Wide tuning ranges are achievable through varying the magnitude of the charging currents. Typical performance specifications for relaxation oscillators are an oscillation frequency in the hundreds of MHz range, and a phase noise of -120 dBc/Hz at a 1 MHz offset [5-7].

### 2.2.3 Ring oscillators

Ring oscillators are very common in integrated circuits due to their simplicity. They are used in many PLL frequency synthesizer and clock recovery designs. The simplest configuration makes use of three cascaded inverters as shown in Fig. 2-4. The oscillation period is set by $2n.T_d$, where $n$ is the number of inverters in the chain and $T_d$ is the delay of one inverter. The number of inverters in a loop must be odd and greater than one; therefore three is the minimum number of inverters that can be used to implement a ring, which therefore sets an upper limit on the maximum

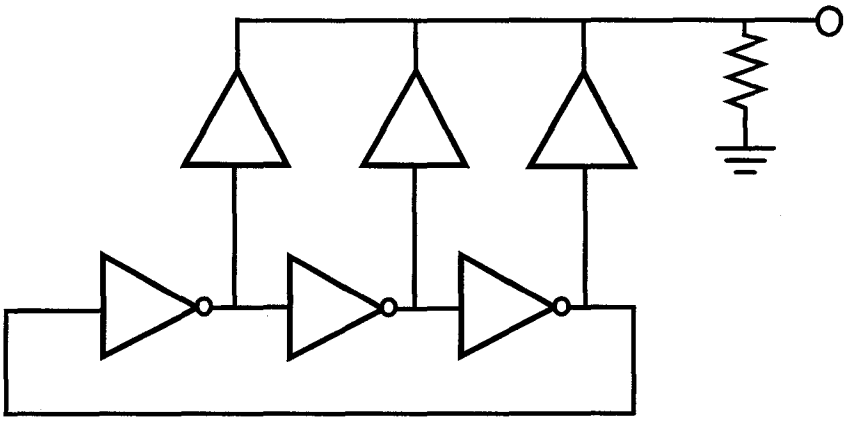

**Fig. 2-5:Ring oscillator providing a period equal to that of a single delay cell.**

frequency achievable for a given $T_d$. However, combining the three available signals of the three inverters as shown in Fig. 2-5, an output with a signal period equal to that of a single inverter can be obtained. Differential inverters can reduce the minimum number of stages to two as shown in Fig.2-6. Although a speed enhancement is not guaranteed due to the increased complexity of the circuit, a distinct advantage is the availability of quadrature signals [8].

Although ring oscillators are capable of operating in the GHz frequency range, it has been shown that they suffer from bad phase noise characteristics due to the switching action of the inverters, and to the fact that they do not benefit from the same bandpass characteristic as an LC-tank based oscillator, which reduces phase noise considerably. A wide tuning range can be achieved in ring oscillators either through varying the bias current of the inverters, or by electrically adjusting the number of

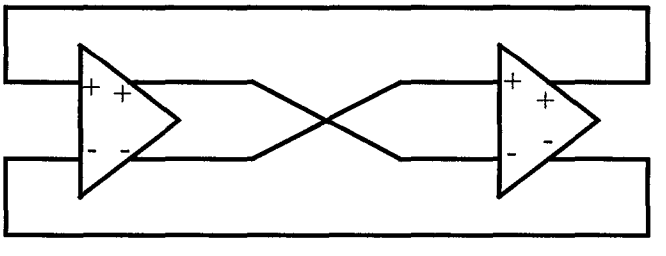


**Fig. 2-6:Ring oscillator using differential inverters.**

inverters in the chain (using short and open circuits).

### 2.2.4 LC-based oscillators

The LC-based oscillator, Fig. 2-7, is the only alternative to ring and relaxation oscillators that can potentially provide better phase noise performance in a monolithic implementation. The resonance of an inductor and a capacitor is the basis of all LC oscillators. The negative resistance, required to maintain oscillation, can be provided by several active devices, but more commonly the transconductance (Gm) of an amplifier as shown in Fig. 2-7. Since the oscillation is determined by passive elements, the spectrum of LC oscillators should be pure. The phase noise of these oscillators depends on the details of the implementation, and on the quality factors of the passive elements forming the resonant tank. Typically, a 20 dB improvement in phase noise is possible over the phase noise of ring and relaxation oscillators. In addition, higher frequency of operation is possible, as will be demonstrated through the results presented in subsequent chapters of this thesis.

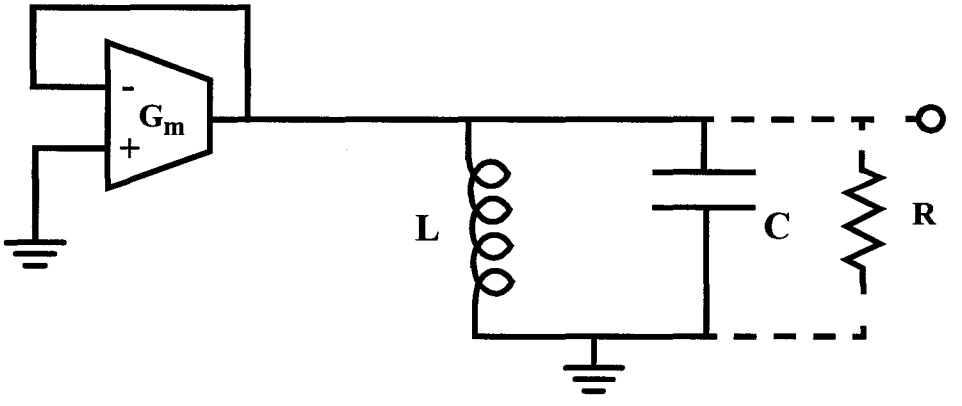


**Fig. 2-7:LC-based oscillator.**

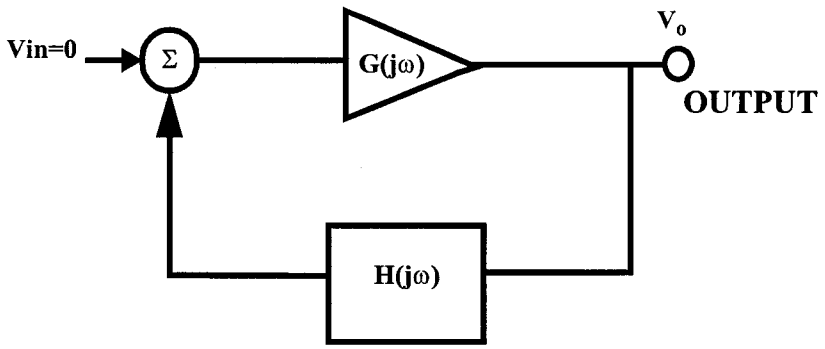


**Fig. 2-8:Generic block diagram of an oscillator.**

## 2.3 LC Oscillator Basic Principles

An oscillator is a device that converts DC power into a periodic output signal (AC power). It is inherently a nonlinear component. Although the nonlinearity results in some distortion of the signal, linear analysis techniques are normally used and yield satisfactory approximation to the performance of LC based systems. Fig. 2-8 shows the typical building blocks that make up an oscillator. It consists of an amplifier with a frequency dependent forward loop gain *G(jω)*, and a frequency-dependent feedback network *H(jω)*. The output voltage is given by:

$$V_o = \frac{V_{in} \cdot G(j\omega)}{1 - G(j\omega) \cdot H(j\omega)} \tag{2.1}$$

To operate as an oscillator, $V_o$ should be non zero even if the input signal $V_{in} = 0$. This can be achieved only if the forward loop gain is infinite, or if the denominator $1 - G(j\omega) \cdot H(j\omega) = 0$, at some frequency $\omega_o$. This leads to the well known condition for oscillation, the Barkhausen criterion, where at some frequency $\omega_o$, $G(j\omega_o) \cdot H(j\omega_o) = 1$ . This means that the magnitude of the open loop transfer function is 1, and that the total phase shift around the loop is 360°: $\arg[G(j\omega) \cdot H(j\omega)] = 360^o$.

The system will be stable (i.e. no oscillations) if either one of these conditions is not satisfied; both must be met in order to induce oscillation in the system.

## 2.4 LC Oscillator Design Approaches

Although the fundamental theory of operation behind all LC oscillators is the same, several points of view can be used in the oscillator design/analysis process:

1-S-parameter approach (most common for microwave implementations) [10][12].

2-Large-signal analytical approach [11].

3-Compressed smith chart (series and parallel resonances) [12].

4-Feedback analysis approach (common feedback structures) [10].

5-Small-signal negative resistance approach obtained using an active device (wideband VCO's) [11].

### 2.4.1 Oscillator design using S-parameters

S-parameters are mostly used in microwave designs, where there is more of a focus on the frequency domain attributes of networks. Consider the two-port oscillator consisting of a resonator, an active device, and possibly a load matching network as shown in Fig. 2-9. $\Gamma_G$ and $\Gamma_L$ are the passive terminations at the generator and at the load of the two-port network. The input reflection coefficient of the two-port is $S'_{11}=b_1/a_1$, where $b_1$ is the input port reflected wave and $a_1$ is the input port incident wave, and $\Gamma_1= S'_{11}$. The output reflection coefficient is $S'_{22}= d_1/c_1$, where $d_1$ is the output port reflected wave and $c_1$ is the output port incident wave, as shown in Fig. 2-9. There are

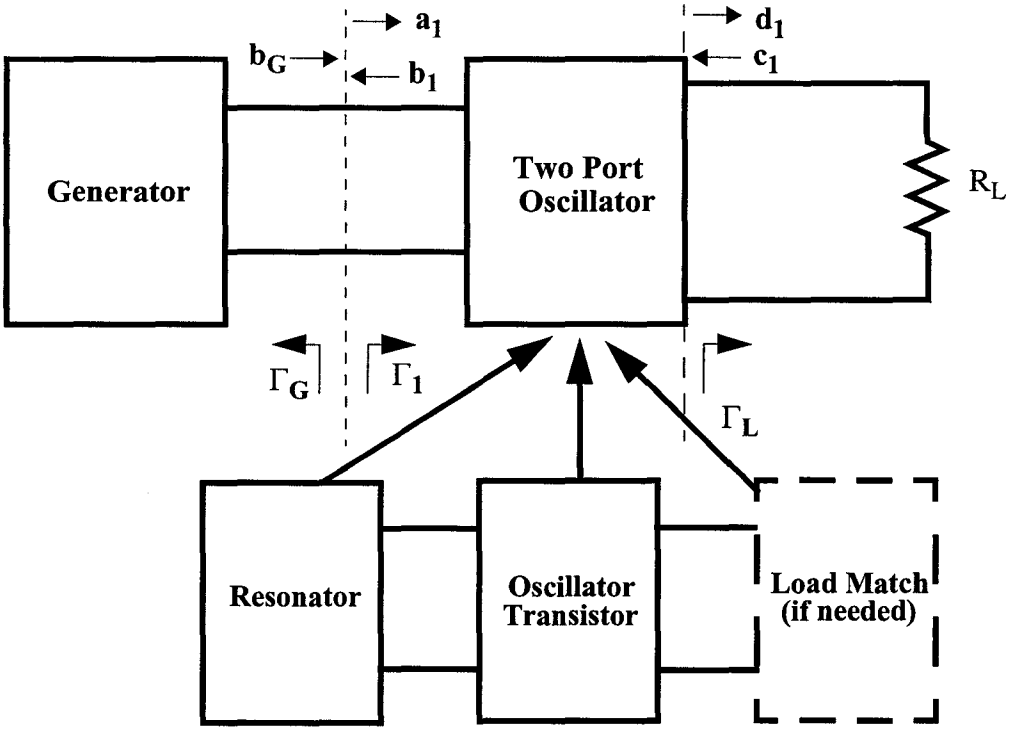


**Fig. 2-9:Two port oscillator connected to a generator and a load.**

three conditions necessary to ensure oscillation:

1- $k < 1$ (where k is known as the Rollet stability factor)

2- $\Gamma_G S'_{11} = 1$ 3- $\Gamma_L S'_{22} = 1$

Where k, the stability factor in terms of S parameters is given by:

$k = (1-|S_{11}|^2 - |S_{22}|^2 + |D|^2)/(2|S_{12}S_{21}|)$, where $D = S_{11} S_{22} - S_{12} S_{21}$.

Note that: $S_{11}' = (S_{11} - D\Gamma_L)/(1-S_{22}\Gamma_L)$, and $S_{22}' = (S_{22} - D\Gamma_G)/(1-S_{22}\Gamma_G)$

Where $\Gamma_L = c_1/d_1$, and $\Gamma_G = a_1/b_1$

Both the input and output ports must resonate at the frequency of oscillation, which is satisfied by conditions 2 and 3 above. Since $|\Gamma_G|$ and $|\Gamma_L|$ are less than unity then, from conditions 2 and 3, $|S'_{11}|$ and $|S'_{22}|$ must be greater than 1. A compressed Smith chart that includes reflection coefficients greater than unity is needed to plot the S-parameters of such a network (Fig.2-11).

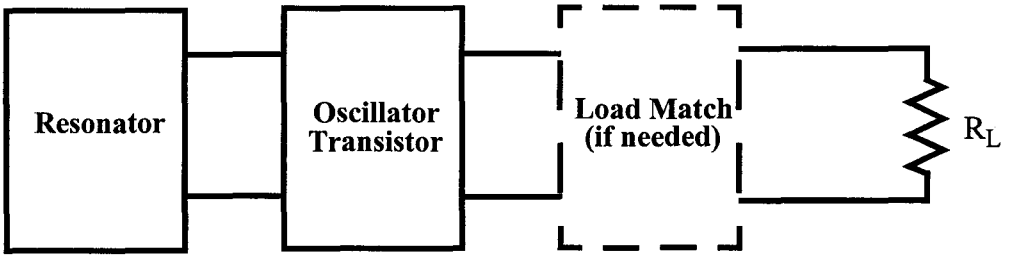


**Fig. 2-10:Oscillator connected to a load.**

It can further be shown that: $b_1/b_G = S'_{11}/(1- \Gamma_G S'_{11})$

This describes the fact that the reflected wave $b_1$ is dependent on $b_G$, $\Gamma_G$, and $S'_{11}$. If condition 2 is satisfied, then $b_G$ must be zero. If $b_G$ is zero, then there is in fact no input from the generator, thus the two-port is sustaining oscillation by itself. Fig. 2-9 can be reduced to the simpler network of Fig. 2-10, which excludes the generator. Normally, only parasitic resistances (i.e. lossless termination) will be present at the resonating port, since a high-Q resonant tank is desirable for minimizing oscillator noise.

The two-port oscillator design using the S-parameters approach can be divided into 4 steps:

1-A transistor with sufficient gain and output power at the desired frequency of operation is selected.

2-A topology that yields $k<1$ at the frequency of interest is chosen, such as a common-base /common-gate circuit topology. If $k>1$, then feedback should be considered.

3-An output load matching circuit that results in $|S'_{11}|>1$ over the targeted frequency range is computed to ensure instability (In the simplest case the output load is 50Ω).

4-The input port should resonate with a lossless termination so that

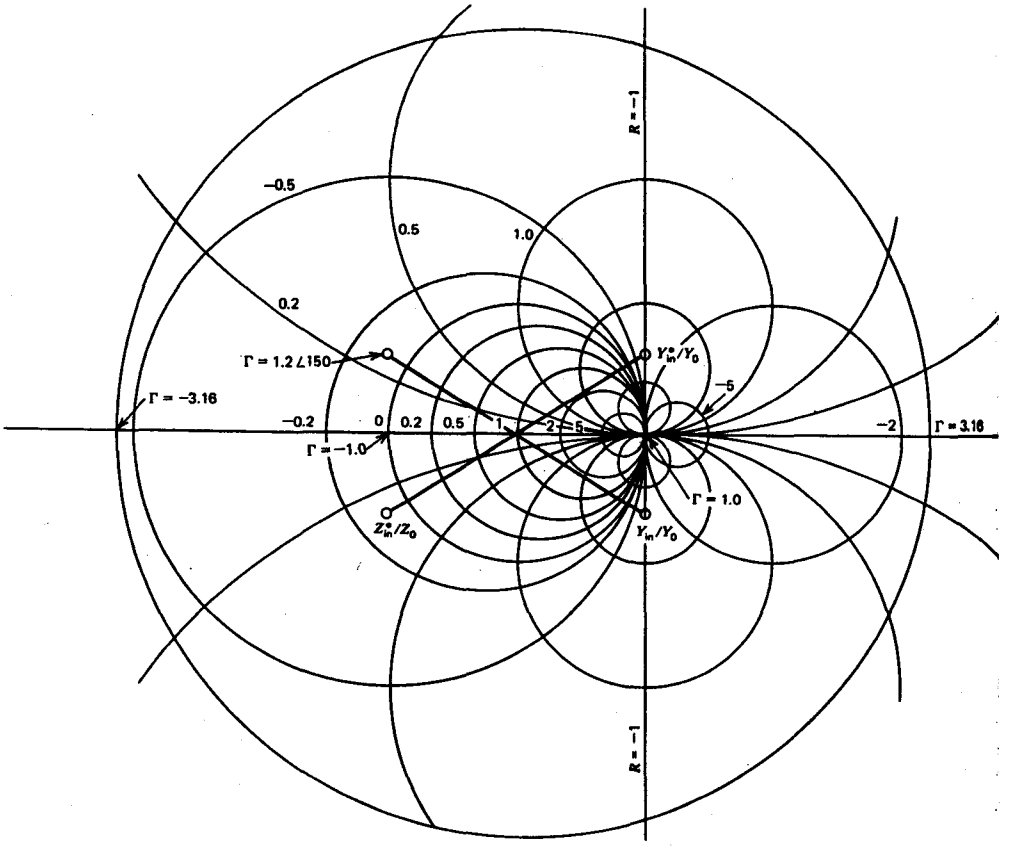


**Fig. 2-11:Example of a compressed smith chart [10].**

$\Gamma_G S'_{11} = 1$. The lossless termination is required for two reasons: the first is to achieve a high-Q resonator, and the second is to reduce the required gain of the active device which compensates for circuit losses. $S'_{22}$ will be greater than unity when the input is properly resonated.

## 2.4.2 Oscillator design using large-signal S-parameters

Oscillators often operate at large output powers, and therefore small signal parameters might not be accurate for precise design. For this reason, some designers use the large signal parameters. The most significant change with large-signal parameters is a magnitude reduction in the value of $S'_{21}$ and changes in the value of $S'_{22}$.

### 2.4.3 The compressed Smith chart

The compressed Smith chart (example shown in Fig. 2-11) is often used in the design of oscillators. It is used for plotting the variations in $S'_{11}$ and $S'_{22}$, the input and output reflection coefficients of a two port oscillator respectively (section 2.4.1), over frequency. The following characteristics of the compressed Smith chart are used in the design process:

1-Resonance requires that the circuit's imaginary impedance term be equal to zero (thus located on the real axis).

2-If the impedance resonance is on the left-hand side of the real axis, then it is series resonance, otherwise (i.e. on the right-hand side) it is parallel resonance.

### 2.4.4 Feedback-based oscillator design

Feedback oscillators have been extensively used in RF systems. The most commonly known oscillators using feedback are the Hartley and Colpitts oscillators. These circuits are based on the Π and T-type feedback loops shown in Fig. 2-12.

Taking the Π-network as an example, the transfer function of the feedback loop can be easily found, assuming high impedances at both the input and output terminals, giving

$$H_F(\omega) = \frac{V_1}{V_{out}} = \frac{Z_1}{Z_1 + Z_3}. \tag{2.2}$$

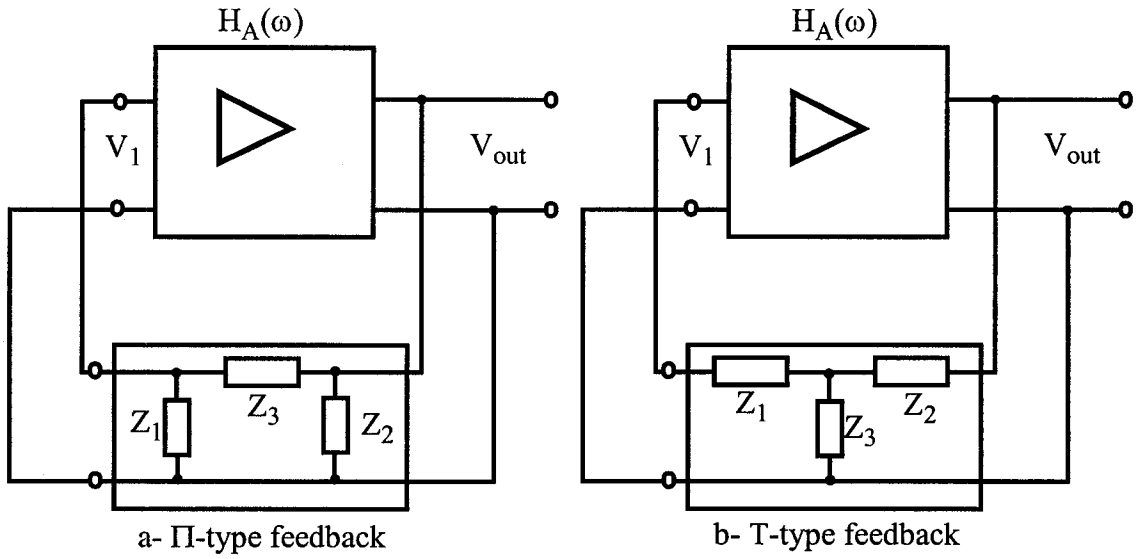


**Fig. 2-12:Circuits with Π- and T- type feedback loops.**

$H_A(\omega)$ depends on the active element and on its equivalent model. Using a simplified FET model, i.e. the FET is replaced by voltage gain source $\mu_v$ in series with an output resistance $R_B$, in a Π-network configuration as shown in Fig. 2-13, the transistor model feedback loop equation is $\mu_v V_1 + I_B R_B + I_B Z_C = 0$, where $\frac{1}{Z_C} = Y_C = 1/Z_2 + 1/(Z_1 + Z_3)$. Solving the loop equation for $I_B$ and multiplying by $Z_C$, $V_{out}$ is obtained, from which the voltage gain $H_A(\omega)$ can be shown to be $H_A(\omega) = -\mu_v/(Y_C R_B + 1)$. The loop transfer function is therefore given by

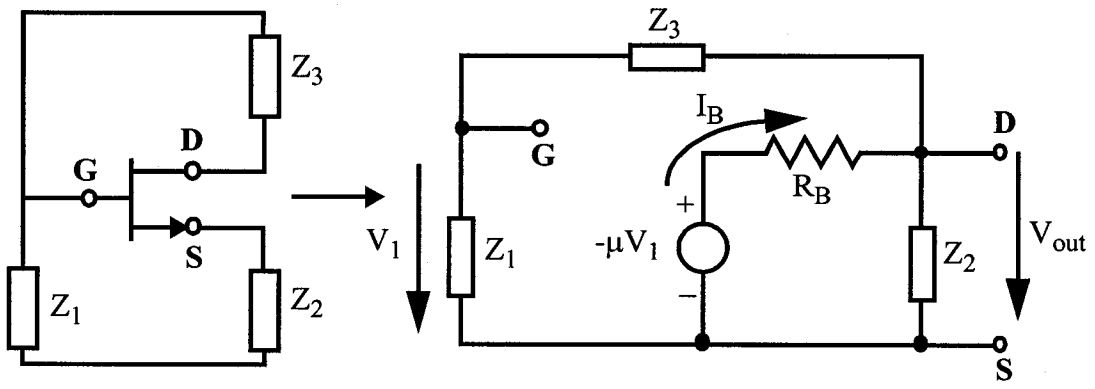


**Fig. 2-13:Feedback oscillator using FET equivalent model.**

$$H_F(\omega)H_A(\omega) = \frac{-\mu_v Z_1 Z_2}{Z_1 Z_2 + Z_3 Z_2 + R_B(Z_1 + Z_2 + Z_3)} = 1. \qquad (2.3)$$

The above transfer function can be used to design numerous types of oscillators, depending on the choice of the three impedances in the feedback loop. Since resistive losses degrade oscillator performance, the impedances are chosen to be purely reactive, i.e. $Z_i = jX_i$ (i=1,2,3). This guarantees that the numerator is a real number. Also, to ensure that the denominator is real, $X_1 + X_2 + X_3$ must equal zero. For the three reactive elements to cancel each other, one must have a negative value that cancels the sum of the two others. Note that inductors have positive reactive impedances, whereas capacitors have negative reactive impedances. The realization of a Hartley oscillator assumes that $X_1$ and $X_2$ are formed by an inductive impedance ($X_1=\omega L_1$, $X_2= \omega L_2$), and that $X_3$ is a capacitive one ($X_3=1/\omega C_3$). The elements of the Colpitts oscillator have the exact opposite signs, i.e. $X_1$ and $X_2$ being capacitive and $X_3$ being inductive. Note that several variations in the type of elements are possible, as well as variations in the active element topology (e.g. common gate, common source, or common drain), which results in multiple implementation possibilities of oscillators of this sort.

### 2.4.5 Design using the negative resistance obtained using a transistor

An oscillator can be viewed as an amplifier with positive feedback (Fig. 2-14). Positive feedback dictates that a portion of the output signal is fed back to the input and in phase to the input signal. In oscillators, there is no input signal, instead the initial signal is generated by noise and energy from the DC bias setup. This is the basis

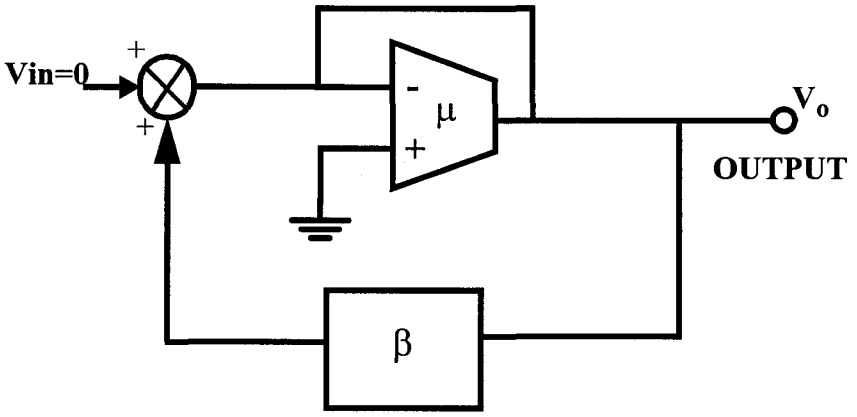


**Fig. 2-14:Oscillator made of an amplifier in a positive feedback configuration.**

on which LC oscillators are designed.

This type of oscillator is composed of an active device and a frequency selective block. The active device, represented by the amplifier symbol in Fig. 2-14, is responsible for generating the negative resistance, while the resonant circuit formed by a combination of device parasitics and other elements (e.g. microstrips, DRO's and lumped elements), is the frequency selective block represented in the feedback path of Fig. 2-14.

The concept of negative resistance can be explained by examining a simple series resonance circuit, such as the one shown in Fig 2-15, consisting of a capacitance C, an inductance L, and a resistance R which represents the losses through the parasitics of the circuit. The input to this circuit is a current-controlled voltage source

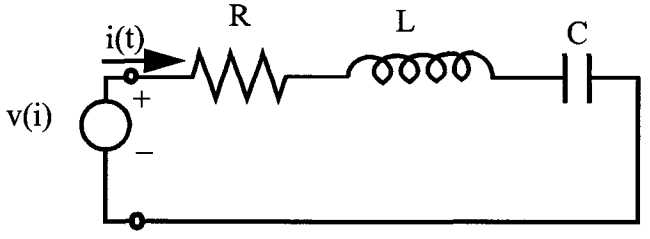


**Fig. 2-15:Series resonance circuit with current-controlled source for loss compensation.**

which represents the output of the active device. The loop current equation through this circuit is given by:

$$L\frac{d^2}{dt}i(t) + R\frac{d}{dt}i(t) + \frac{1}{C}i(t) = -\frac{d}{dt}v(i) \quad . \tag{2.4}$$

The steady state solution for a constant voltage amplitude has the standard format:

$$i(t) = e^{\alpha t}\left(I_1 e^{\omega Q^t} + I_2 e^{-\omega Q^t}\right) \tag{2.5}$$

where $\alpha = -R/2L$ and $\omega_Q = \sqrt{(1/(LC)) - (R/(2L))^2}$, and $I_1$ and $I_2$ are constant current values. Since $\alpha$ is a negative number, the response of the resonant circuit to any excitation is damped with time to reach zero as time progresses. The goal of an active element in the oscillator is to compensate for the resistive loss, thus acting as a negative resistance.

The approach is to select a nonlinear device that will have a voltage-current characteristic response $v(i) = v_o + R_1 i + R_2 i^2 + \ldots$, then adjust the terms to compensate for R. Substituting the first two terms of the above expansion into equation 2.4, we obtain

$$L\frac{d^2}{dt}i(t) + R\frac{d}{dt}i(t) + \frac{1}{C}i(t) = -\frac{d}{dt}v(i) = -R_1\frac{d}{dt}i(t) \, . \tag{2.6}$$

Combining the coefficients of the first derivative, we aim at meeting the condition $R + R_1 = 0$ as a requirement to set the damping coefficient to zero. In addition, to get oscillations to start up, a positive attenuation coefficient will be

required, thus the active device must introduce a resistance $R_1$ which more than cancels out the resistance in the circuit. In other terms, $|R_1|$ must be greater than $|-R|$.

For the oscillators studied in this thesis, the negative resistance is provided by different combinations of CMOS devices, either using an all NMOS design or a hybrid that uses both NMOS and PMOS devices to provide the energy required to maintain oscillation. Brief explanations on the exact functionality of the active devices will be presented along with the different configurations examined in the following chapters.

## 2.5 Phase Noise in LC Oscillators

Phase noise is important in transceivers because, as mentioned previously, it determines the sensitivity of the receiver and the purity of the transmitter (Chapter 1, section 1.3.1). It is possible to analyze phase noise either in the frequency domain or in the time domain. Both analyses are equivalent due to the duality of the two domains, however the choice of the domain of characterization depends on the implementation of the oscillator. For example, ring oscillators are based on a cascade of delay times, and thus the notion of phase noise in such an implementation is naturally translated to its time domain dual, known as jitter. Jitter is the time difference between the zero crossing of the actual oscillator and that of an ideal oscillator oscillating at the same frequency. As another example, the frequency domain is more intuitive when dealing with LC-based oscillators since, in this case, it is the LC combination that provides the information necessary in computing the oscillation frequency, in contrast with delay cells.

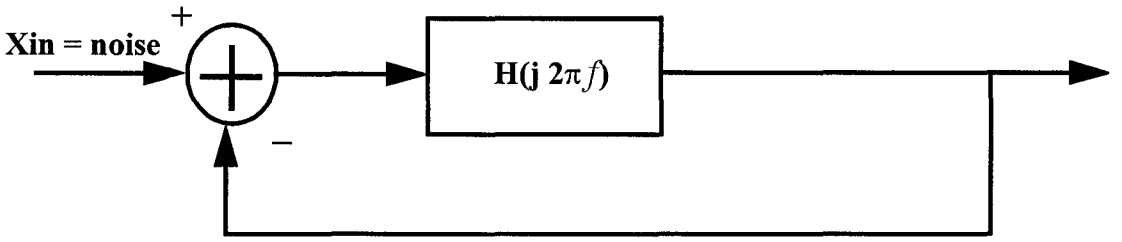


**Fig. 2-16:An oscillator with negative feedback seen as an active filter.**

### 2.5.1 Additive vs. multiplicative noise

Noise sources in an oscillator can be classified into two main categories: The additive noise and the multiplicative noise. The additive noise accounts for all the noise sources whose frequencies appear directly around the carrier frequency. The oscillator can be modeled as an active filter (a frequency dependent gain block) in a negative feedback loop as shown in Fig. 2-16. Each noise source is an input to this system, and is further shaped by the transfer function of the oscillator as shown in Fig. 2-17. The most important parameter of the filter's transfer function is its $Q$ (the quality factor of the tank) which, in a fully monolithic implementation, would be primarily dependent on $Q_L$ (the quality factor of the inductor used). The higher the Q, the more attenuated the input noise would be at some offset $\Delta f$ from the carrier frequency. Since the phase noise is a relative measure of noise with respect to the amplitude of the main signal, an increase in the carrier power would result in a reduction of the phase noise caused by additive noise sources (this can be viewed as a direct increase in the signal-to-noise ratio). Additive noise is the noise generated only by the different components that make up the oscillator, and would exist even in the absence of oscillation.

Multiplicative noise, on the other hand, appears close to the carrier frequency as a result of the frequency conversion process caused by the non-linear active devices

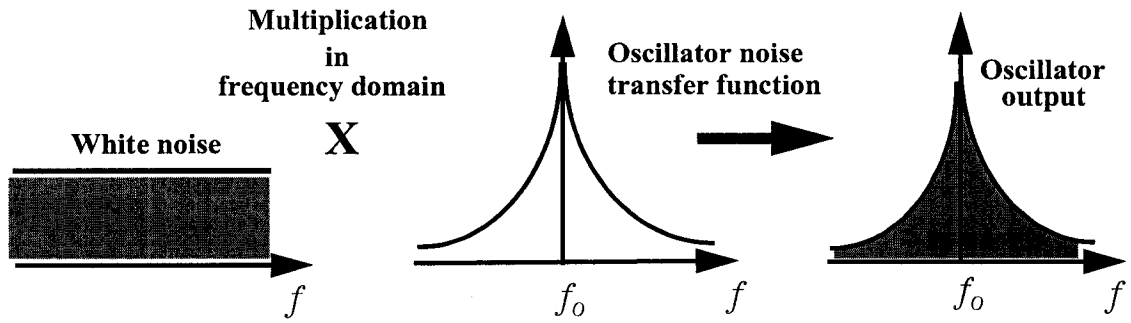


**Fig. 2-17:Noise shaping performed by an oscillator.**

used in the circuit. These devices behave as mixers, or frequency multipliers, due to their non-linear characteristics. Hence, noise sources existing at frequencies $nf_o + \Delta f$ result in equal side bands at $f_o \pm \Delta f$. Through this mixing function, there will be low frequency noise upconverted around the carrier, as well as some high frequency noise that will be downconverted around the carrier. In CMOS, the low frequency noise is particularly important since the high $1/f$ noise of CMOS devices is upconverted around the carrier.

## 2.5.2 Phase noise estimation

It is difficult to analytically predict the phase noise with high accuracy.

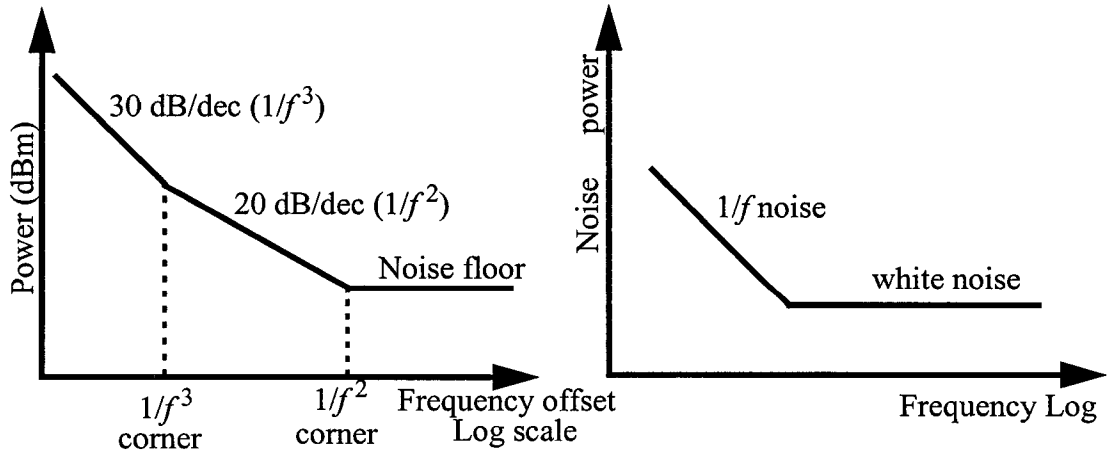


**Fig. 2-18:(a) Slope of single sideband phase noise, and (b) upconverted 1/f noise power.**

Leeson's model gives a good approximation of the phase noise in LC-based oscillators [9]. In general terms, the phase noise of any LC oscillator may be expressed as $L(\Delta f) = L_o + a_2/(\Delta f^2) + a_3/(\Delta f^3)$, where $\Delta f$ is the offset frequency from the carrier, and $a_i$ are the coefficients of the different terms. The close-in phase noise is mainly determined by $a_3/\Delta f^3$, where the phase noise has a slope of -30 dB per decade, as shown in Fig. 2-18. The slope of the sideband phase noise gradually goes from -30dB/dec to -20dB/dec, and finally levels off far off from the carrier frequency, reaching a constant value $L_o$ corresponding to the white noise floor of the system. The ratio of $a_3/a_2$ defines the $1/f^3$ corner frequency of the oscillator: The larger the ratio, the larger is the -30dB/dec frequency range. The ratio of the two coefficients is set by the corner frequency of the $1/f$ noise which gets upconverted: The higher the ratio, the higher the $1/f$ corner frequency.

When replacing the coefficients $a_i$ of the previous equation by their respective noise sources, the following form is obtained as an expression for the phase noise:

$$L(\Delta f) = \frac{v_n^2}{2A^2}\left[1 + \frac{1}{\Delta f^2}\left(\frac{f_o}{2Q}\right)^2\left(1 + \frac{f_\alpha}{\Delta f}\right)\right], \qquad (2.7)$$

Where $L(\Delta f)$ is the phase noise expressed in dBc/Hz, $\Delta f$ is the frequency offset from the carrier $f_o$, $v_n$ is the noise density, $A$ is the amplitude of oscillation, $Q$ is the quality factor of the loaded tank (mostly determined by $Q_L$, the quality factor of the integrated inductor), and $f_\alpha$ is the residual flicker noise corner frequency. The $f_\alpha$ parameter is difficult to predict, and hence is generally a fitting parameter that is determined after

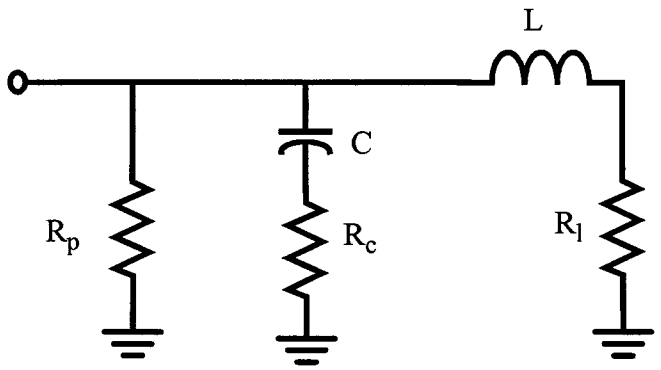


**Fig. 2-19:Tank equivalent circuit.**

measurements are obtained. It depends on the amount of $1/f$ upconversion generated by the non-linear characteristics of the components making up the circuit. The first term, $\frac{v_n^2}{2A^2}$, is the inverse of the signal to noise ratio of the oscillator. It emphasizes the importance of having a large oscillation amplitude to reduce the effect of the additive noise. The most significant variable in the equation is Q; It is generally limited by the passive structures available in silicon-based technologies, thus it is important not to degrade it further with poor design and choice of transistors.

Breaking down the terms from the previous equation to a more specific form of LC-based oscillators, we obtain the following more common expression:

$$L(\Delta f) = \frac{k \cdot T \cdot R_{eff} \cdot (1 + N_A)}{P_{signal}} \left[ \left( \frac{f_o}{\Delta f} \right)^2 \left( 1 + \frac{f_\alpha}{\Delta f} \right) \right], \qquad (2.8)$$

Where $k$ is the Boltzman constant ($k$=1.38x10$^{-23}$J/K), $T$ is the absolute temperature, $P_{signal}$ is the power of the carrier signal, and $N_A$ is the excess noise factor due to the active devices. If we consider the tank circuit shown in Fig. 2-19, the equivalent (or effective) series resistance $R_{eff}$ is given by $R_{eff} = R_c + R_l + \frac{1}{R_p (2\pi f_o C)^2}$, where $R_p$ is the output resistance of the active device(s), and $R_c$ and $R_l$ correspond to the parasitic

resistive elements of C and L respectively.

Since the $1/f$ noise corner frequency is usually lower than 100KHz, the last factor, $1+\frac{f_\alpha}{\Delta f}$, can be discarded to evaluate the phase noise at higher offset frequencies.

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CHAPTER 3

# CMOS 4-12.5 GHz Oscillators for Low Voltage RF Applications

## 3.1 Introduction

As mentioned earlier, the continuous increase in communications speed has motivated the design and implementation of RF circuits in the 2-6 GHz range, such as the wireless LAN systems in the US (IEEE 802.11a standard for the FCC unlicensed national information infrastructure, the U-NII band), and the European High Performance Radio LAN (HIPERLAN). As CMOS technology scales down, the transconductance-current ratio ($g_m / I$) becomes comparable to that of the bipolar technology, making standard CMOS processes a cost efficient solution for complete integration of analog, RF, and digital circuits on a single chip.

A number of performance requirements have to be met to make a VCO suitable for wireless applications. Most importantly, low phase-noise is required to avoid corrupting the mixer-converted signal by close interfering tones. Low power consumption and tunability are also two important aspects that define the performance of a VCO.

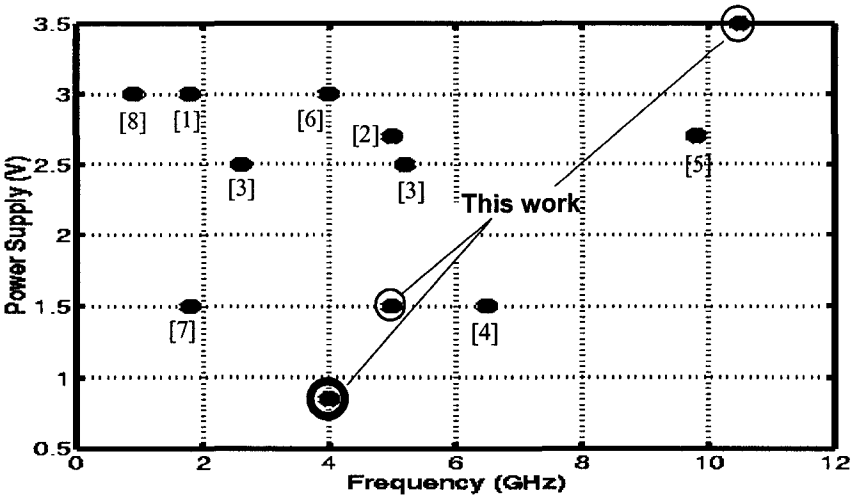


**Fig. 3-1:Comparison of voltage supplies versus frequency.**

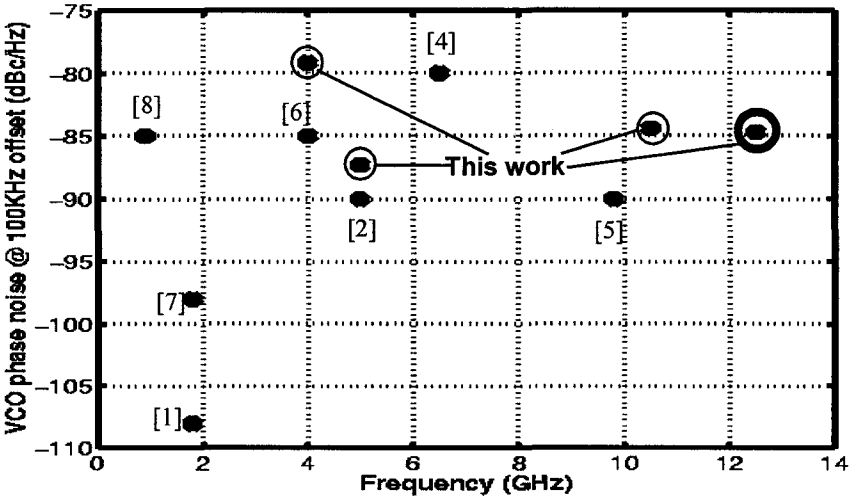


**Fig. 3-2:Comparison of phase noise to other reported VCO's @100 KHz offset versus frequency.**

The frequency range of CMOS RF oscillators published to date is 900 MHz - 10 GHz [1]-[8]. This chapter presents the design steps, optimization, and performances of four CMOS VCO's ranging from 4 to 12.5 GHz [9-11]. The 4 GHz circuit is implemented in a 0.25 μm standard CMOS process and the design is mainly optimized to operate from a supply voltage as low as 0.85 V, in order to minimize power consumption. This is the lowest supply voltage reported to date at this frequency (Fig 3-1).

The second VCO is implemented in a 0.35 μm process reaching a maximum center frequency of 5 GHz using a 1.5 Volt supply. It was designed to offer a wide tuning range of 10%. The third and fourth VCO's were optimized for speed. While they reached the maximum oscillating frequency of 10.55 GHz and 12.5 GHz, the highest reported for a CMOS VCO when this work was first published, their phase noise remains comparable to other circuits operating at much lower frequencies (Fig 3-2). These VCO's are implemented in a 0.35μm standard CMOS process and they employ a stacked NMOS and PMOS cross-coupled differential pairs along with a differentially excited integrated inductor. No varactor is used in this circuit: instead, tuning is achieved through the back-gate voltage of the PMOS devices.

The following sections will detail the modeling of integrated inductors, as well as the design equations and trade-offs. Section 3.3 discusses the circuit optimization options, section 3.4 details a few of the layout issues. Finally, section 3.5 presents the measurement results.

## 3.2 Circuitry and Design Equations

The four circuits presented in this chapter are based on two variations of LC oscillators. The 4 and 5 GHz circuits are implemented using the topology shown in Fig. 3-3, whereas the 10.5 and 12.5 GHz circuit topology is shown in Fig. 3-4. The frequency-tuning varactor implementations are different in each one of the three designs as will be detailed later.

Three fundamental building-blocks constitute the core of the LC oscillators: (i) In both topologies, the cross-coupled differential amplifiers, M1 and M2, provide

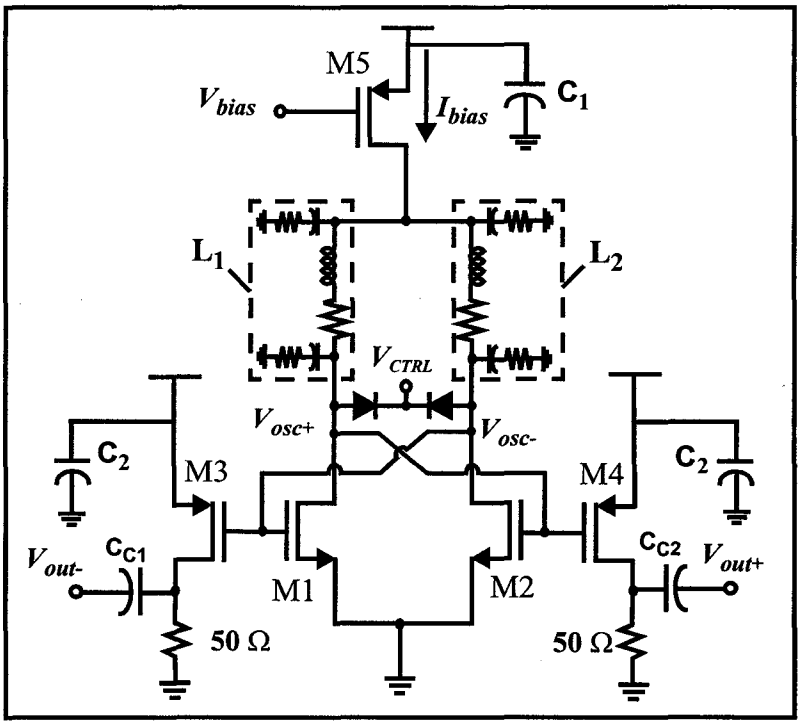


**Fig. 3-3:LC-based VCO with varactor tuning.**

the negative impedance necessary to maintain steady oscillation. In the topology of Fig. 3-4, M3 and M4 form another PMOS cross-coupled differential amplifier which additionally contributes to the overall negative impedance of that circuit. (ii) The tuning varactors. (iii) The integrated inductors, $L_1$ and $L_2$ in Fig. 3-3, and L in Fig. 3-4. The remaining components are for biasing purposes and for driving the 50 Ω impedances of the measurement equipment.

### 3.2.1 Phase noise

As detailed in the previous chapters, the performance of an integrated VCO is mainly evaluated by the phase noise in the vicinity of its center frequency $f_o$. The output phase noise at an offset $\Delta f$ from $f_0$ can also be approximated by the following relationship [1]-[2]

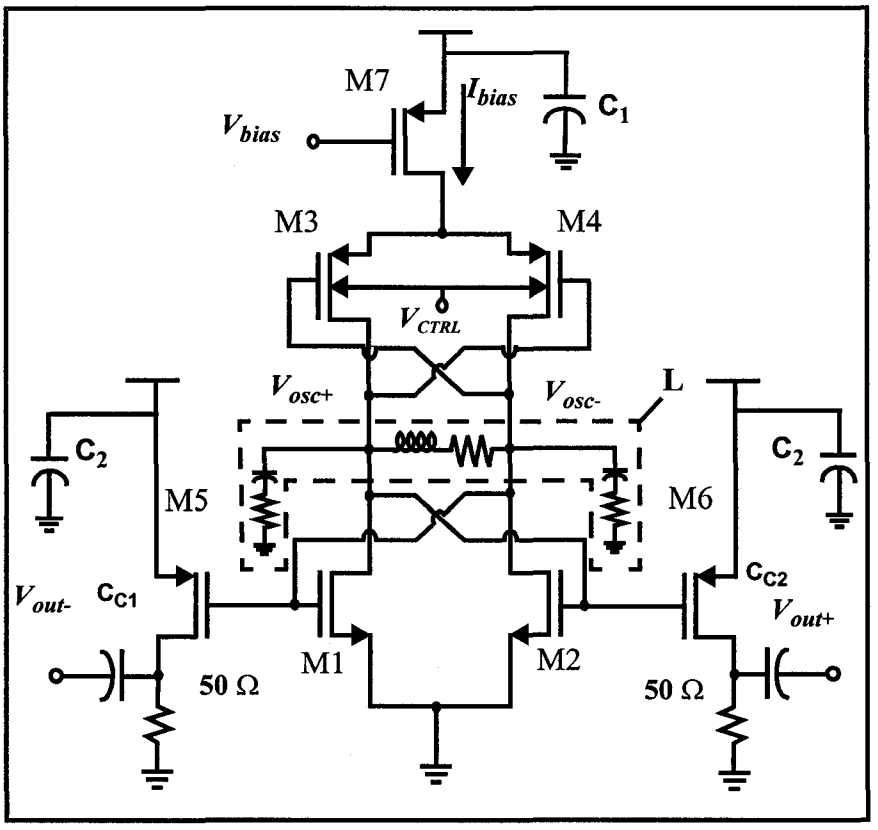


**Fig. 3-4:LC-based VCO with PMOS back-gate tuning.**

$$L\{\Delta f\} = kT(1+A)\,Z_o \frac{1}{Q_{tank}} \left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{V^2_{rms}}, \tag{3.1}$$

where $kT$ is the product of the Boltzman constant by the absolute temperature, $A$ is the noise factor safety margin necessary to ensure oscillation start-up, $V_{rms}$ is the root mean square voltage at the oscillation nodes, and $Z_o = \sqrt{(L/C_{tank})}$ and $Q_{tank}$ are the tank characteristic impedance and quality factor, respectively. The value of $Q_{tank}$ can be computed as a function of the quality factor of the inductor ($Q_L$), and the quality factors of the different capacitors ($Q_{Ci}$), that make up the tank capacitance ($C_{tank}$) [2]

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} \div \left(\sum_i \left(\frac{1}{Q_{Ci}}\right) \cdot \left(\frac{C_i}{C_{tank}}\right)\right). \tag{3.2}$$

The inverse square relationship with $V_{rms}$ in (3.1), outlines well the noise-power trade-off. Maximizing the quality of the resonant tank would improve the noise performance considerably. However, as will be discussed in the following section, this could come at the cost of both tunability and oscillator power consumption.

### 3.2.2 Integrated inductors

Critical devices in the design of a fully integrated VCO are the on-chip inductors, as phase noise is primarily dependent on their quality factor. Inductors exhibit high-frequency losses at many levels, e.g. substrate losses and skin-effect, which need to be accurately modeled and accounted for. Although several inductor modeling tools exist, e.g. ASITIC from Berkeley, an in-house tool was developed at McGill (MIND: McGill INDuctor modeler)[14][15]. Besides the inductance $L$, two figures of merit determine the viability of an inductor for a specific design: the quality factor $Q_L$, and the self-resonant frequency $f_{self}$. The latter should be considerably higher than the targeted frequency of operation.

### 3.2.3 The LC tank resonator

Each LC tank in the circuit of Fig. 3-3 is composed of an inductor (L1 or L2) in parallel with a total capacitance composed of: (i) $C_L$, the inductor's parasitic capacitance, (ii) $C_{var}$, the varactor's tunable capacitance, and (iii) the transistors' total drain and gate capacitors to ground $C_d$ and $C_g$. The transistor capacitors exhibit a relatively constant quality factor [2], higher than that of an integrated inductor. Therefore, in order to avoid degradation in $Q_{tank}$, it is desirable to use large transistors allowing the higher quality parasitic capacitors to make up the major part of $C_{tank}$. The

remaining portion of the tank capacitance is dedicated to the varactor's tunable capacitor which usually represents 10 to 20% of the total tank capacitance.

The LC tank of the circuit in Fig. 3-4 is composed of inductor L in parallel with a total capacitance composed of the drain-gate capacitances $C_{dg}$ and gate-source capacitances $C_{gs}$ of M1-M4 (Fig. 3-6). All the capacitances related to M1 and M2 form the fixed component of the tank capacitance, whereas those of M3 and M4 form the variable part which is tuned through the biasing of the bulk of the PMOS transistors.

Two different types of inductors are used for each VCO. The 10 GHz circuit was designed using a square spiral inductor, whereas the 12.5 GHz circuit was designed using a smaller octagonal spiral inductor in order to achieve a better quality factor at a higher frequency.

The first set of tank design equations are those of the center frequency

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{tank}}}, \text{ where} \tag{3.3}$$

$$C_{tank} = C_L + C_{var} + C_{dM1,M2} + C_{gM2,M1} + C_{gM3,M4}, \text{ where (Fig. 3-4)} \tag{3.4}$$

Cd and Cg are the total drain and gate capacitances to the substrate. The term $C_{dM1,M2}$ designates the total drain capacitance of either M1 in the case of one resonant

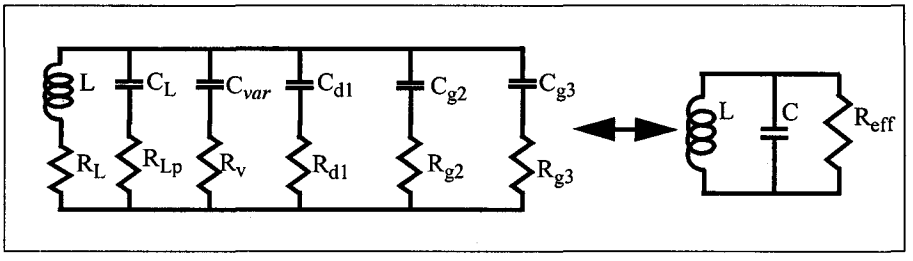


**Fig. 3-5:Resonant tank components for the circuit in Fig. 3-3.**

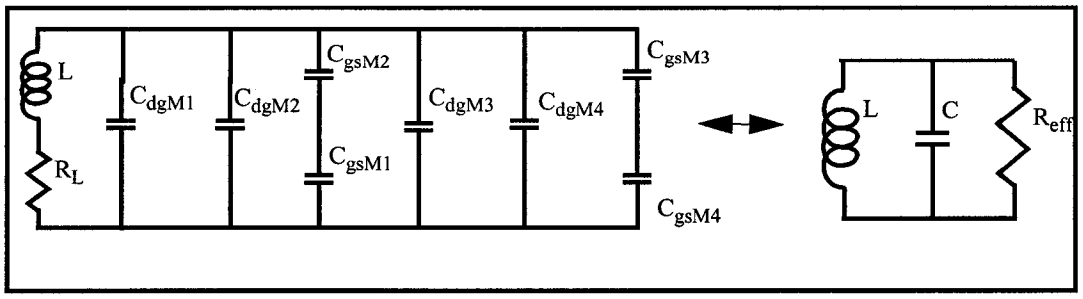


**Fig. 3-6:Resonant tank components for the circuit in Fig. 3-4.**

tank and the total drain capacitance of M2 in the case of the other resonant tank. The same applies for $C_{gM2,M1}$, which refers to the gate of M2 or M1 and $C_{g3,M4}$, which refers to the gate of M3 or M4.

$$C_{tank} = C_{dgM1} + C_{dgM2} + \frac{\langle C_{gsM1} + C_{gsM2} \rangle}{C_{gsM1} \cdot C_{gsM2}} + C_{dgM3} + C_{dgM4} + \frac{\langle C_{gsM3} + C_{gsM4} \rangle}{C_{gsM3} \cdot C_{gsM4}} \quad \text{(Fig. 3-4).} \qquad (3.5)$$

The second design equation for the LC tank describes the amplitude of oscillation

$$V_{osc} = Z_{tank} I_{bias}, \qquad (3.6)$$

where $Z_{tank}$ is the equivalent impedance of the tank at the resonance node. As this impedance is proportional to $L$, a larger amplitude of oscillation can be achieved for the same bias current by using a larger inductor, resulting in a reduction of phase noise. However, the use of a larger inductor would require a smaller tank capacitance to maintain the same operational frequency; this would result in the use of a smaller varactor, thus reducing the tuning range of the VCO. A reasonable compromise between both performance parameters, noise and tuning, must be reached to determine

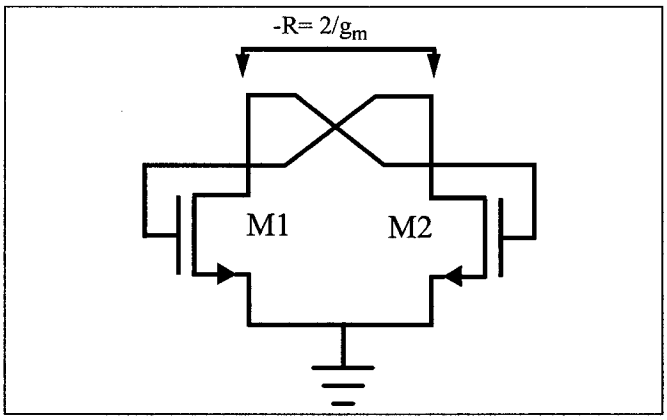


**Fig. 3-7:Negative resistance provided by M1-M2.**

a suitable inductor value [3].

### 3.2.4 The cross-coupled amplifier

The resonator of an LC oscillator cannot maintain steady oscillation by itself due to the energy lost per cycle through the parasitic resistances of the LC tank. For a narrow band of frequencies, the parasitic resistances of the inductor and of the various capacitors can be summed up into a single parallel resistance $R_{eff}$ (as shown in Figs. 3-5 and 3-6). Since, as in most fully integrated cases, the inductor exhibits the lowest quality factor, the tank effective series resistance $R_{eff}$ can be approximated to be equal to the inductor's series resistance $R_L$. Applying series-shunt transformation, the equivalent real parallel impedance of a tank can be shown to be

$$R_{shunt} \approx Q_{\text{tank}}^2 R_L \approx Q_L^2 R_L . \tag{3.7}$$

It can also be shown that the cross-coupled amplifier (Fig. 3-7) provides a negative resistance, $-R = 2/g_m$, which is used to replenish the lost energy and sustain indefinite periodic oscillation. For the circuit of Fig. 3-4, two cross-coupled amplifiers contribute to the negative resistance, thus $-R = 2/(g_{m12} + g_{m34})$, where

$g_{m12}$ is the transconductance provided by either M1 or M2 depending on which one is on and which is off and $g_{m34}$ is similarly the transconductance of either M3 or M4. To ensure that the circuit produces stable oscillation, the total transconductance $G_m$ must be chosen to satisfy

$$G_m \geq \frac{2}{Q_L^2 R_L} = \frac{2R_L}{(\omega_o L)^2}, \tag{3.8}$$

where $G_m = g_{m12}$ (for Fig. 3-3), or

$G_m = g_{m12} + g_{m34}$ (for Fig. 3-4).

Note that to ensure start-up of oscillation, it is recommended to have a safety factor in the estimate of the expected transconductance of the transistors. A safety factor of two is usually sufficient to ensure start-up. For the high frequency circuit presented here, we used a safety factor of 1.5 in order to minimize the transistor sizes.

The tank impedance along with the biasing current determine the amplitude of oscillation. Once the tank impedance is set, a trade-off between the power consumption and the amplitude of oscillation must be resolved, which results in a compromise between reducing the bias current and improving the phase noise of the VCO. This is due to the fact that the phase noise is inversely proportional to the square of the signal amplitude at the node of oscillation, (as observed in equation 3.1). However, increasing the current beyond a certain point results in worsening the phase noise once again, as the signal amplitude reaches an upper limit while the device noise figure continues to increase.

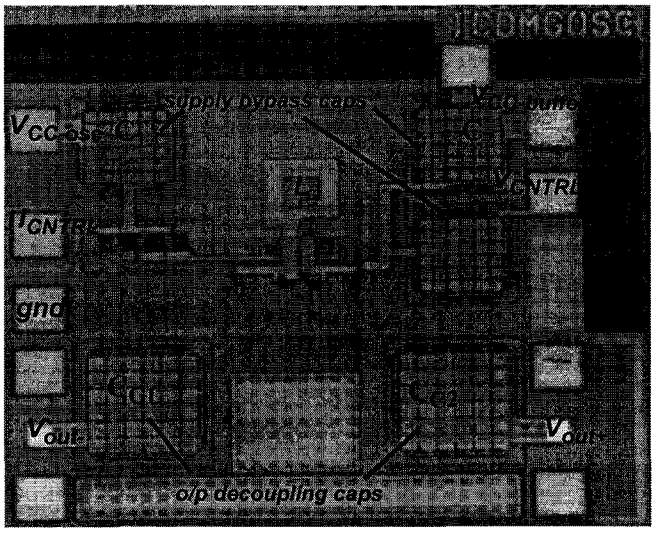


**Fig. 3-8:Photomicrograph of the 10 GHz VCO.**

## 3.2.5 The varactors

The variable capacitor needed for frequency tuning can be implemented in a number of ways. Each circuit presented in this paper uses a different type of varactor. The one used in the 4 GHz circuit is an NMOS transistor over an Nwell, which makes use of the gate capacitance of the transistor [12]-[13]. This structure has been reported to provide a wider tuning range and a better quality factor in comparison to other varactors based on PN or $P^+N$ junctions, while providing capacitances of the same order of magnitude.

The 5 GHz VCO makes use of a PMOS $P^+$ drain/source diffusion in an Nwell. Note that in order to avoid current leakage, and thus $Q_{tank}$ degradation, the voltage across the $P^+N$ junction, $V_{osc}$ -$V_{CTRL}$, should remain negative at all times in order to always keep the junction reverse-biased.

The varactor used in the 10 and 12.5 GHz circuits is similar in principle to the latter one, since the junction capacitance is dependent on the biasing of the Nwell surrounding the PMOS transistors. The main difference is that the tuning in this circuit

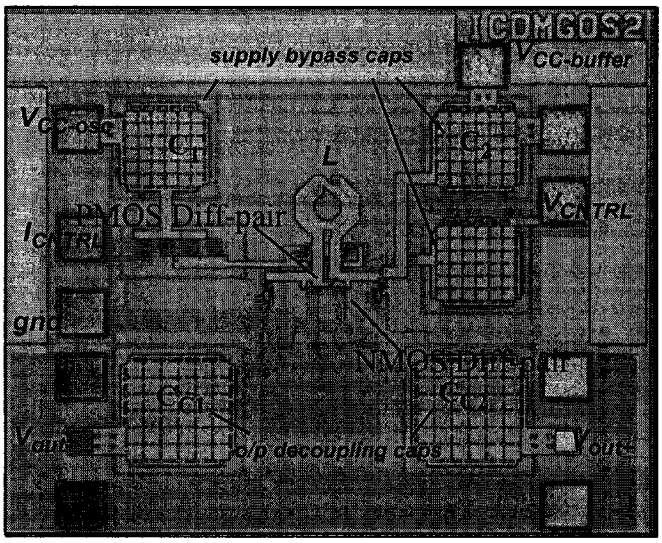


**Fig. 3-9:Photomicrograph of the 12.5 GHz VCO.**

is not a direct result of the variation in the junction capacitance, but is due to the varying sizes of the drain and source to gate capacitances. It is in fact the change in the sizes of the depletion regions around the source and the drain that varies $C_{dg}$ and $C_{gs}$ of M3 and M4 of Fig. 3-4.

## 3.3 Circuit Optimization

The 4 GHz oscillator was optimized for low voltage operation by maximizing the sizes of the transistors used in the cross-coupled differential amplifier. The large transistors provide the $G_m$ necessary to ensure oscillation start-up while requiring a small gate to source voltage $V_{gs}$. To oscillate at the relatively high 4 GHz frequency, small inductors are used to compensate for the overly large tank capacitance, which results in a reduction in the tank impedance and thus a reduced amplitude of oscillation, and in consequence an increase in the phase noise of the VCO. Also, small varactors have to be used, which reduces the tuning range, compared for

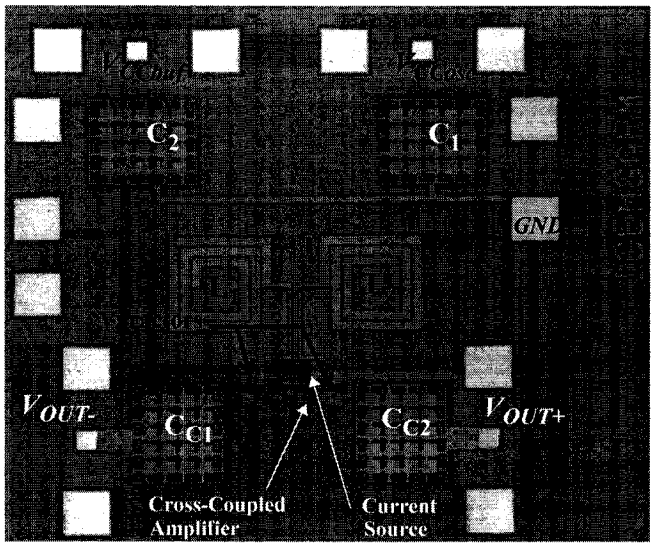


**Fig. 3-10:Photomicrograph of the 4 GHz VCO.**

example to the 10% tuning range achieved by the 1.5 V, 5 GHz VCO.

The 10.5 and 12.5 GHz circuits were optimized for speed by appropriate sizing of the cross-coupled amplifiers and of the integrated inductor. This specific circuit topology minimizes the tank capacitance by using a cross coupled PMOS differential pair which simultaneously provides part of the $G_m$ required for oscillation, and the variable capacitance for tuning. The $g_m$ contributed by each individual device can be small, and therefore small devices can be used resulting in a minimized tank capacitance. The LC tank is further optimized by using a small inductor. Since the transistors used are small, large $V_{gs}$ drops are necessary to achieve the required overall $G_m$ , which explains the larger supply voltage used. The use of small devices for tuning also results in a considerably reduced tuning range of the VCO.

## 3.4 Layout Issues

Photomicrographs of the 4, 5, 10.5 and 12.5 GHz circuits are shown in Fig. 3-

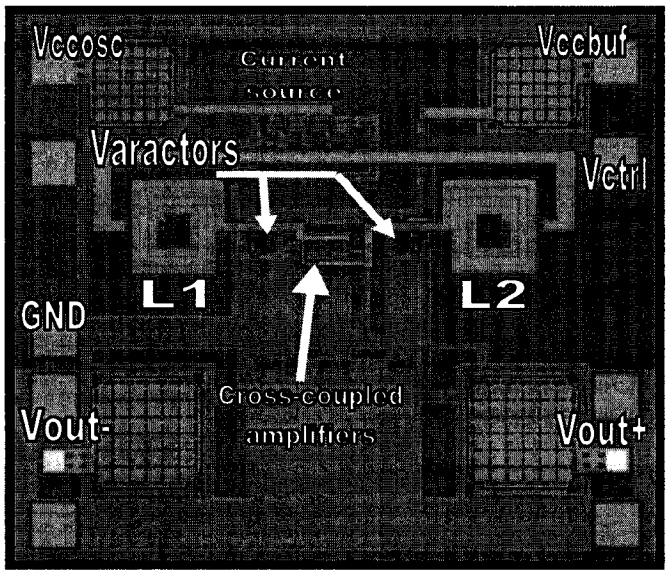


**Fig. 3-11:Photomicrograph of the 5 GHz VCO.**

8 to Fig. 3-11. The layouts are centered around the nodes of oscillation. All connections to these nodes are minimized to avoid the degradation of the quality factor of the resonator tanks and to avoid varying the frequency of oscillation. The windings of the inductors are made particularly wide to minimize the series resistance of the inductors. The PMOS varactor has multiple parallel finger connections to reduce its series resistance.

Grounded guard rings surround the active devices in order to reduce

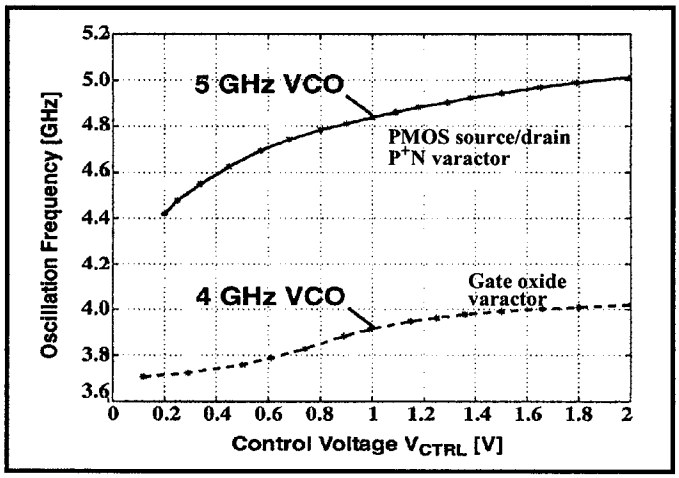


**Fig. 3-12:Tuning of the 4 GHz and 5 GHz VCO's.**

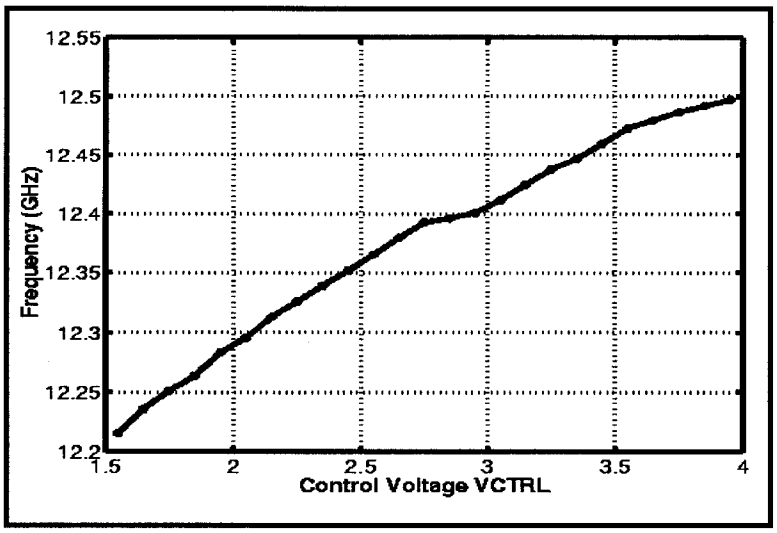


**Fig. 3-13:Frequency tuning of the high-frequency VCO.**

substrate noise and to avoid latching. DC ground lines are kept thin while AC grounds are made wide. The wide ground lines reduce the ground inductance and ensure low resistance paths to ground for the high frequency signals.

## 3.5 Measurement Results

The tuning ranges for the 4 and 5 GHz circuits are 8.75% and 10%

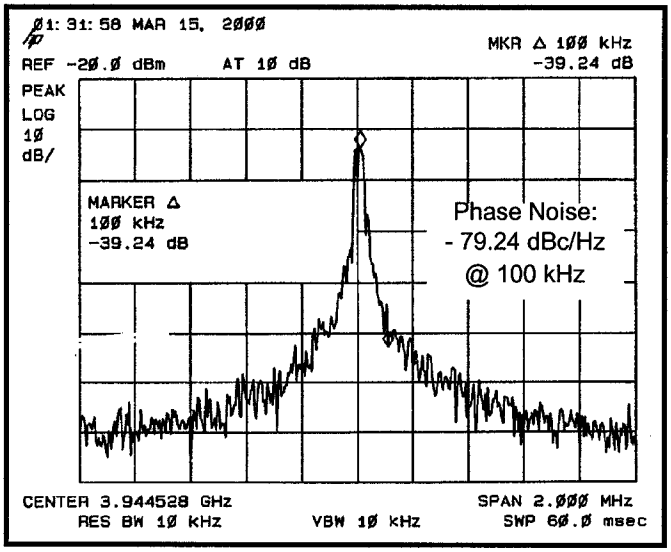


**Fig. 3-14:Output of the 4 GHz VCO.**

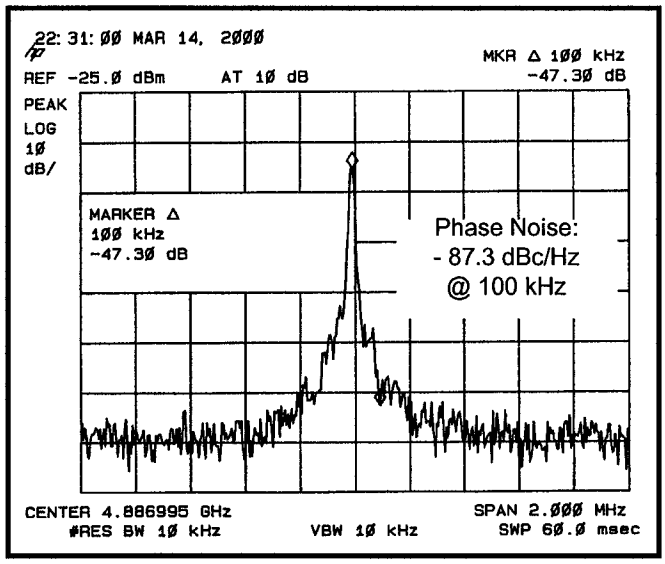


**Fig. 3-15:Output of the 5 GHz VCO.**

respectively, as shown in Fig. 3-12. The difference in the tuning behavior is due to the different nature of the varactors used in both circuits as explained earlier. The 12.5 GHz VCO tuning behavior is shown in Fig. 3-13. The tuning range is 300 MHz, allowing the oscillator center frequency to move from 12.2 GHz to 12.5 GHz. This amounts to a 2.4% tuning range, which is not an impressive absolute figure of merit. However, this 300 MHz tuning range is quite comparable to those published for VCO's

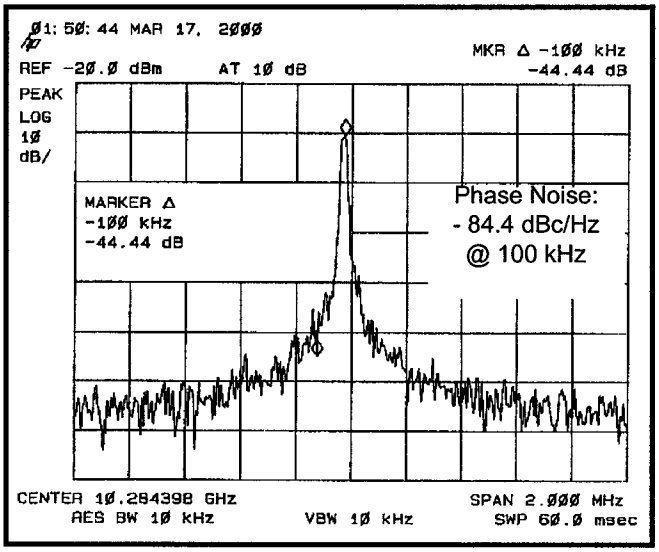


**Fig. 3-16:Output of the 10 GHz VCO.**

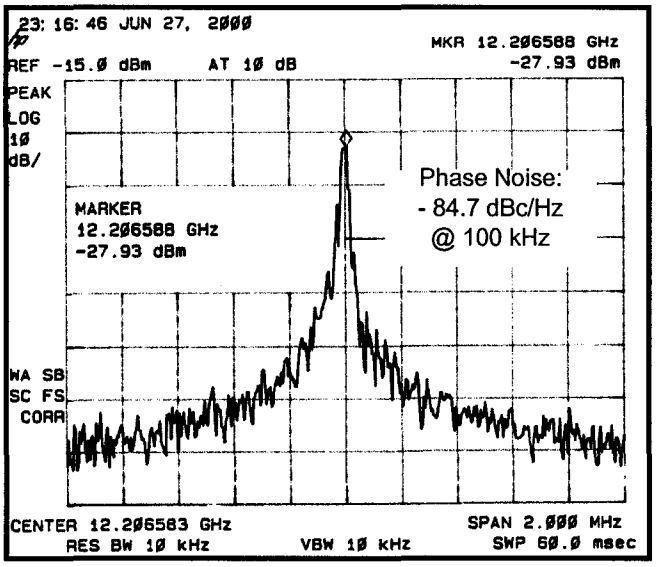


**Fig. 3-17:Output of the 12.5 GHz VCO.**

operating at lower frequencies. The tuning behavior for the 10 GHz oscillator is identical to the one shown in Fig 3-13, except that the range it covers is from 10.25 to 10.55 GHz.

Although the varactor of the 4 GHz VCO (gate oxide capacitance) is known to have a high quality factor, the phase noise in that circuit was dominated by the low quality factor of the integrated inductors used, resulting in a better overall phase noise for the 5 GHz VCO using a PMOS source/drain junction varactor. The oscillators' measured phase noises are -79.2, -87.3, -84.4 and -84.7 dBc/Hz at 100 kHz offset for the 4, 5, 10.5 and 12.5 GHz circuits, respectively. Figs. 3-14-3-17 show the measured spectral outputs for the 4 to 12.5 GHz circuits. Although the 12.5 GHz VCO is operating at a higher frequency than the 10 GHz one, its measured phase noise is slightly better. This can be explained by the difference in the inductors used in the 2 VCO's. The 10 GHz design uses a square spiral inductor, whereas the 12.5 GHz one makes use of a smaller octagonal inductor. The smaller inductance permits the higher frequency of operation, while its octagonal shape improves its quality factor around the

frequency of oscillation, thus resulting in a better phase noise. The phase noises of the four oscillators compare well with other published work (Fig. 3-2). The results of circuit measurements are summarized in Table 1.

## 3.6 Conclusion

Low-voltage and high frequency VCO's were presented. The circuits range in frequency from 4 to 12.5 GHz. The 4 GHz circuit was optimized for low voltage operation, achieving the lowest operational voltage for its frequency range. The high frequency VCO achieved a maximum frequency of 12.5 GHz, the highest frequency of oscillation for a CMOS VCO to be reported at the time of publication.

**TABLE 1. VCO's Performances**

| Technology | CMOS 0.25μm | CMOS 0.35μm | CMOS 0.35μm | CMOS 0.35μm |
|---|---|---|---|---|
| Power supply | 0.85 V | 1.5 V | 3.5 V | 3.5 V |
| Maximum frequency | 4 GHz | 5 GHz | 10.55 GHz | 12.5 GHz |
| Phase noise @ 100 KHz offset | -79.2 dBc/Hz | -87.3 dBc/Hz | -84.4 dBc/Hz | -84.7 dBc/Hz |
| Tuning range | 3.65-4 GHz (350 MHz) | 4.5-5 GHz (500 MHz) | 10.25-10.55 GH (300 MHz) | 12.2-12.5 GHz (300 MHz) |
| Tuning% | 8.75 % | 10 % | 3 % | 2.4 % |
| Bias current | 4.8 mA | 6 mA | 8 mA | 8 mA |
| Power Consumption (w/o o/p buffer) | 4.08 mW | 9 mW | 28 mW | 28 mW |

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CHAPTER 4

# A New CMOS VCO Architecture for Sub-1 Volt High-Frequency (8.7-10 GHz) RF Applications

## 4.1 Introduction

Driven by the reduction of the power consumption of digital circuits and the scaling of modern technologies, the supply voltages of integrated circuits continue to decrease towards sub-1V. New circuit architectures are needed, especially for analog signal processors, to cope with this trend [1]. In chapter three we reported oscillations with frequencies as high as 10 and 12 GHz that have been achieved using standard digital CMOS processes [2], [3]. The structure of those VCO's employed stacked PMOS and NMOS transistors sharing the same DC current, and therefore requiring relatively high supply voltages (2.7-3.5V).

The new VCO topology introduced in this chapter considerably reduces the supply voltage requirement, and consequently the power consumption. This is done by altering the structure of the conventional "complementary differential LC" topology shown in Fig. 4-2(a) [2], [3]. In addition to maintaining the features of the original

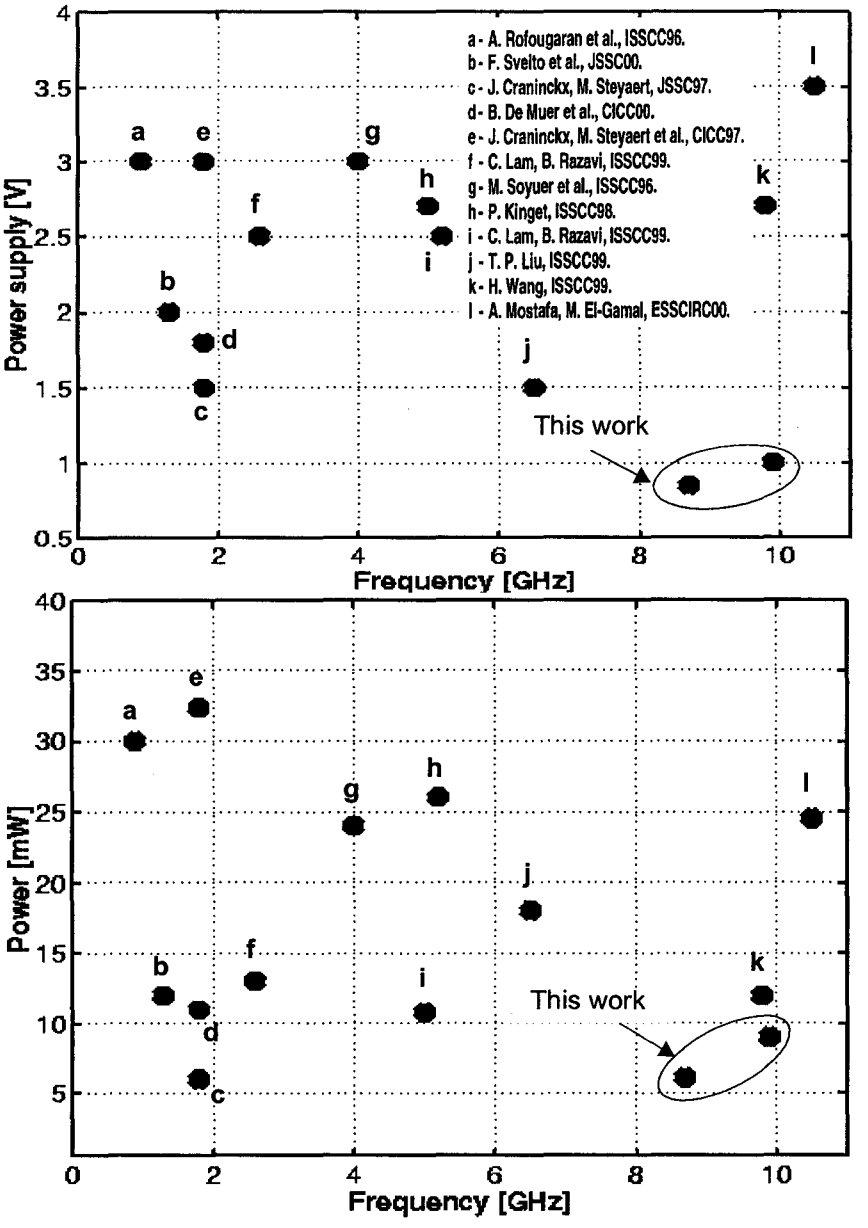


**Fig. 4-1: Comparison of supply voltage and power consumption versus frequency to state-of-the-art VCO's.**

topology (Section 4.2), the proposed architecture offers additional design flexibility and provides an alternative to overcome the limited tuning range of back-gate tuning (Section 4.3). The detailed circuitry and design guidelines of the new circuit are presented in Section 4.4.

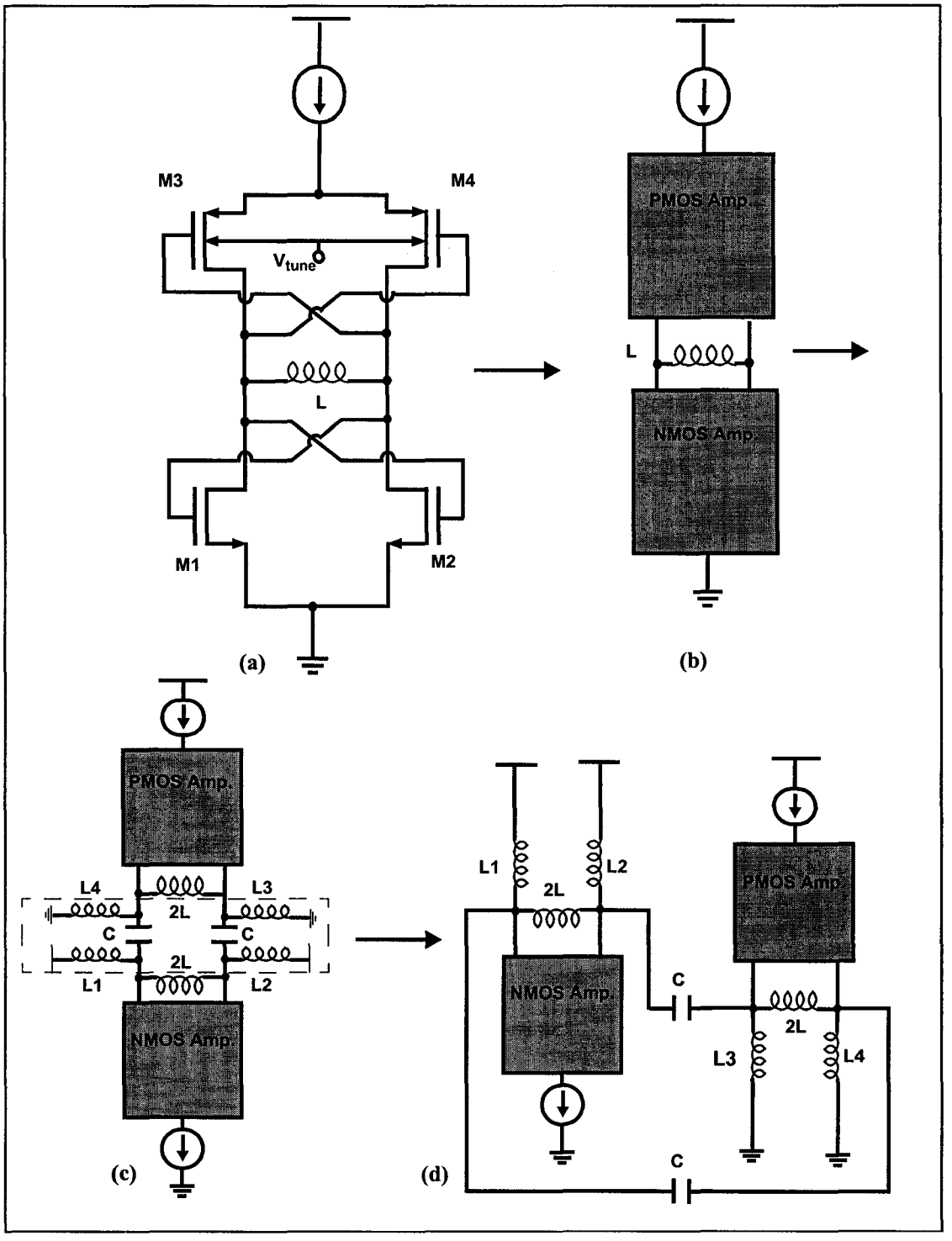


**Fig. 4-2:(a) Symmetric LC VCO structure. (b)-(d) Progression towards a low-voltage topology.**

Two test VCO prototypes were implemented in a standard 0.18 μm CMOS process. They operate using 0.85 and 1-Volt power supplies, which is approximately *one*

*third* the supply voltage needed by the original topology (Fig. 4-1). This is achieved while satisfying other requirements such as low phase noise, low power consumption (Fig. 4-1), and a reasonable tuning range. Measured results are reported and discussed in Section 4.5.

## 4.2 Original Circuit Structure

The complementary differential back-gate tuned VCO in Fig. 4-2(a), has been shown to allow very high frequencies of oscillation (9.8 - 12.5 GHz) [3], [4]. It uses NMOS and PMOS cross-coupled amplifiers along with a differential inductor $L$. The resonant tank is formed by the inductor and the parasitic capacitances of both amplifiers. The frequency tuning is performed by controlling the PMOS transistors' back gate voltages. This configuration has several desirable features:

1) The differential excitation of integrated inductors yields higher *effective* quality factor [5]. This results in an improvement in the VCO's phase noise.

2) The PMOS devices are used for frequency tuning by controlling their back-gate voltages, thus eliminating the need for varactors, which tend to degrade the tank quality factor at high frequencies [6].

3) Dispensing of the varactors allows for higher frequency of oscillation.

4) The tank resonator is formed in a loop configuration (i.e. none of its elements are ground referenced), making the frequency of oscillation less sensitive to transistor and inductor parasitics to the substrate (refer to Section 4.4.1).

The main drawbacks of this topology are the relatively high voltage supply required, and the limited tuning range provided by back-gate tuning.

## 4.3 New Circuit Architecture

The progression of the circuit structure towards a low-voltage topology is shown in Fig. 4-2. Capacitors are inserted between the PMOS and NMOS sections to decouple their DC bias, without affecting the AC interaction between the two tanks (Section 4.4.2). Inductors *L1-L2* are then added to ensure a DC path from the power supply to the NMOS tank, while presenting a high impedance to AC signals (Section 4.4.3). Similarly, inductors *L3-L4* secure a DC path for the PMOS tank to ground.

The resulting topology significantly reduces the voltage supply required by splitting the DC path of the PMOS and the NMOS cross-coupled amplifiers, while maintaining the characteristics of the original circuit. A second advantage is gained by decoupling the DC biasing of the two tanks: Tuning can now be done either using the back-gate voltage of the PMOS tank, or via its DC bias. Combining both tuning mechanisms results in a wider tuning range (Section 4.5, Fig 4-10).

## 4.4 Circuitry and Design Guidelines

Fig. 4-3 shows the complete transistor-level VCO circuit. In the following subsections, we briefly highlight the main design issues related to the new structure.

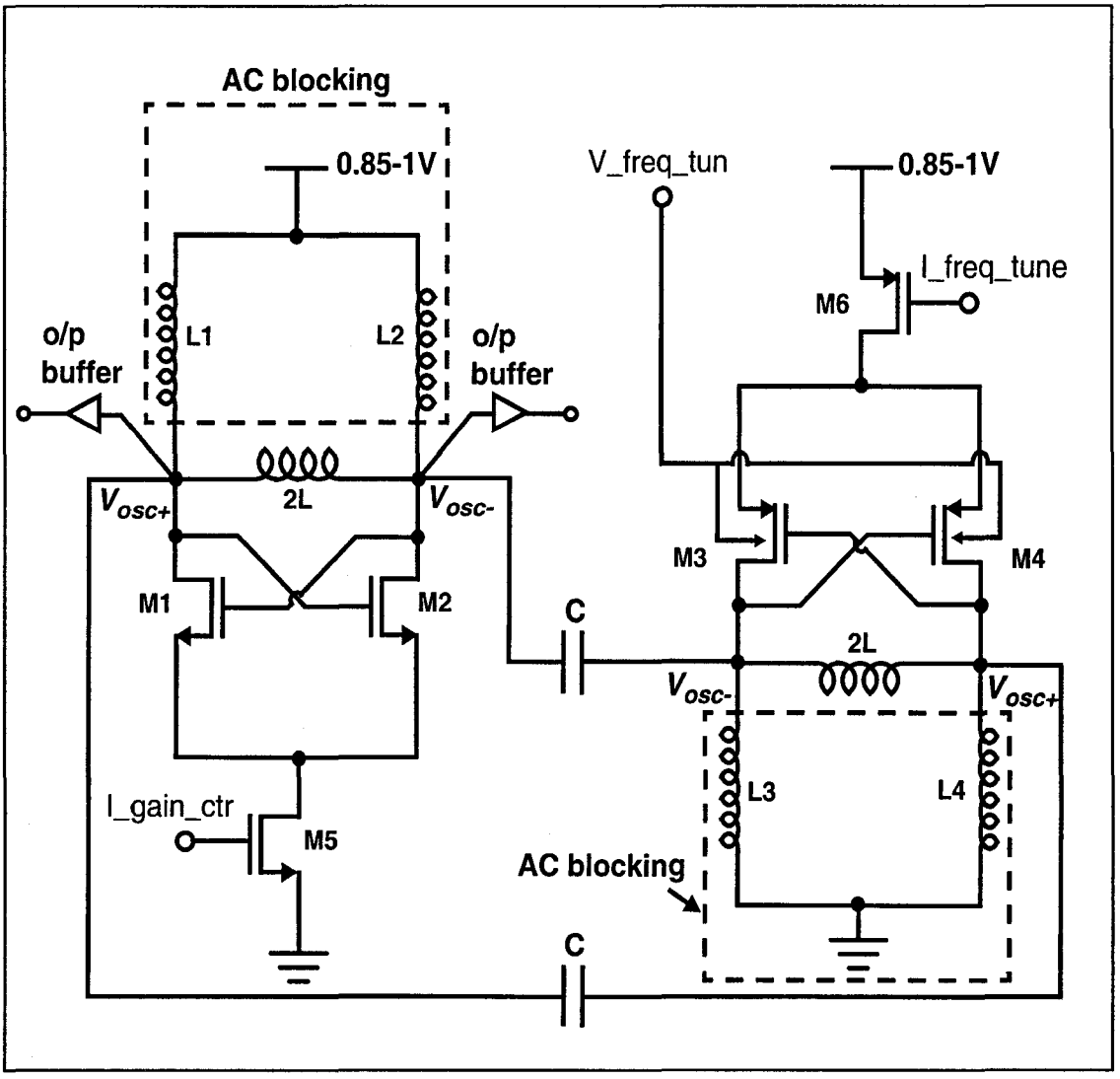


**Fig. 4-3: Circuit of the proposed VCO using capacitively coupled NMOS-PMOS LC tanks. The output buffers are on chip PMOS transistors with 50 Ω resistor loads.**

### 4.4.1 The LC tank resonator

Figure 4-4 shows the AC equivalent circuit of the LC-tanks of the VCO in Fig. 4-3. It is composed of two differential inductors, *2L*, in parallel with a total capacitance composed of the drain-gate capacitances $C_{dg}$ and gate-source capacitances $C_{gs}$ of *M1-*

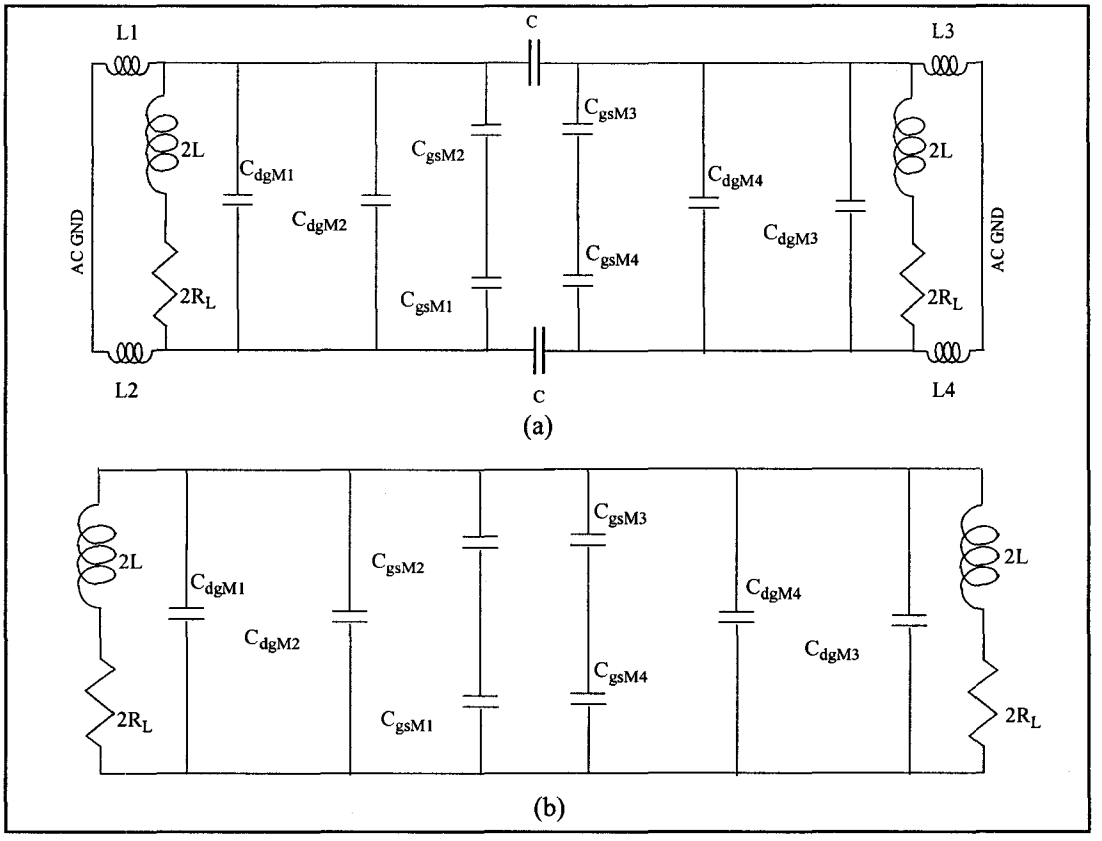


**Fig. 4-4: (a) Tank components, and (b) high frequency equivalent circuit.**

*M4*. All the capacitances related to *M1* and *M2* form the fixed component of the tank capacitance, whereas those of *M3* and *M4* form the variable part. The design requirements of the DC-blocking capacitors *C*, and the AC-blocking inductors *L1-L4*, are discussed in subsequent sections. In the high-frequency equivalent circuit (Fig. 4-4(b)), the coupling capacitors are treated as short circuits, and *L1-L4* as open circuits. The oscillator frequency is given by $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{\tan k} \cdot C_{tank}}}$, where

$$C_{tank} = C_{dgM1} + C_{dgM2} + \frac{\langle C_{gsM1} + C_{gsM2} \rangle}{C_{gsM1} \cdot C_{gsM2}} + C_{dgM3} + C_{dgM4} + \frac{\langle C_{gsM3} + C_{gsM4} \rangle}{C_{gsM3} \cdot C_{gsM4}}, \quad (4.1)$$

and $L_{\tan k} = 2L \,||\, 2L = L$.

### 4.4.2 Coupling capacitors

The sizes of the capacitors $C$ need to be chosen to ensure they present a low impedance path to the RF signal between the PMOS and NMOS tanks, at the frequency of oscillation. For this, the following condition must be satisfied,

$$2C \gg C_{\tan k}. \tag{5}$$

We used two 2.5 pF high quality metal-insulator-metal (MIM) capacitors, which represent approximately 7-8 Ω of resistance at $f_o$.

### 4.4.3 AC-blocking inductors

The role of *L1-L4* is to prevent the tank's energy from being wasted into the voltage supplies. They should act as AC-blocking impedances. The impedance of each one of those inductors at $f_o$, $Z_{Lblock}$, needs to be significantly larger than the tank impedance $Z_{tank}$. It can be shown that this condition is ensured when the following relations are satisfied

$$\frac{Z_{Lblock}}{2} \gg Z_{L_{\text{tank}}} \,||\, Z_{C_{\text{tank}}}, \tag{5.1}$$

$$L_{block} \gg \frac{2.L_{\text{tank}}}{1 + \left(4.\pi^2 \cdot f_o^2 \cdot L_{\text{tank}} \cdot C_{\text{tank}}\right)}. \tag{5.2}$$

In our prototypes, each one of the blocking inductors is made up of a combination of an integrated spiral inductor in series with the bonding inductance of the packaging, with a total of approximately 3.5 nH.

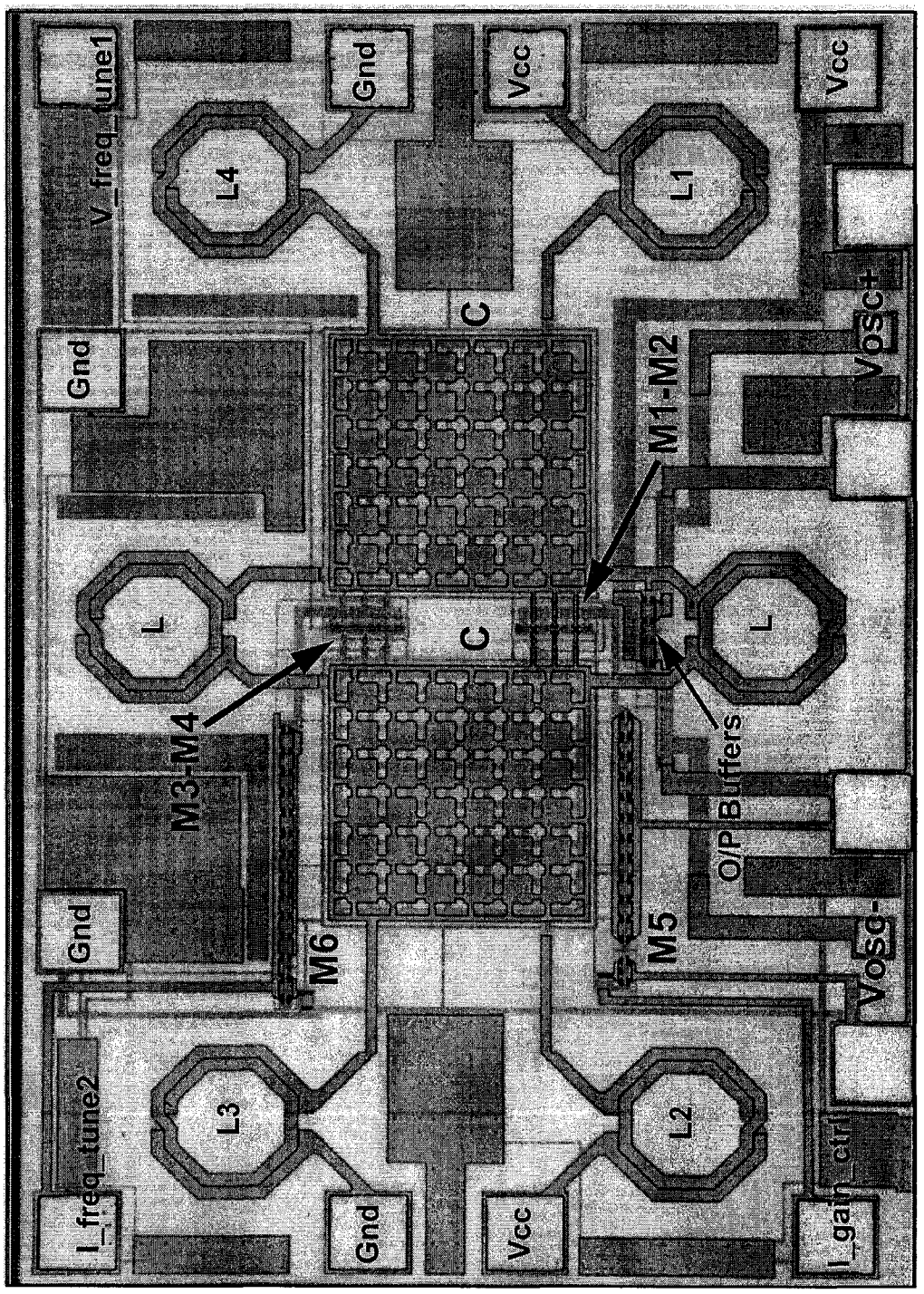


**Fig. 4-5: Photomicrograph of the 8.7 GHz VCO.**

## 4.5 Measurements and Performance

Photomicrographs of the 8.7 and 10 GHz chips are shown in Fig. 4-5 and Fig. 4-6. The two layouts are identical except for the inductors L, and the PMOS differential

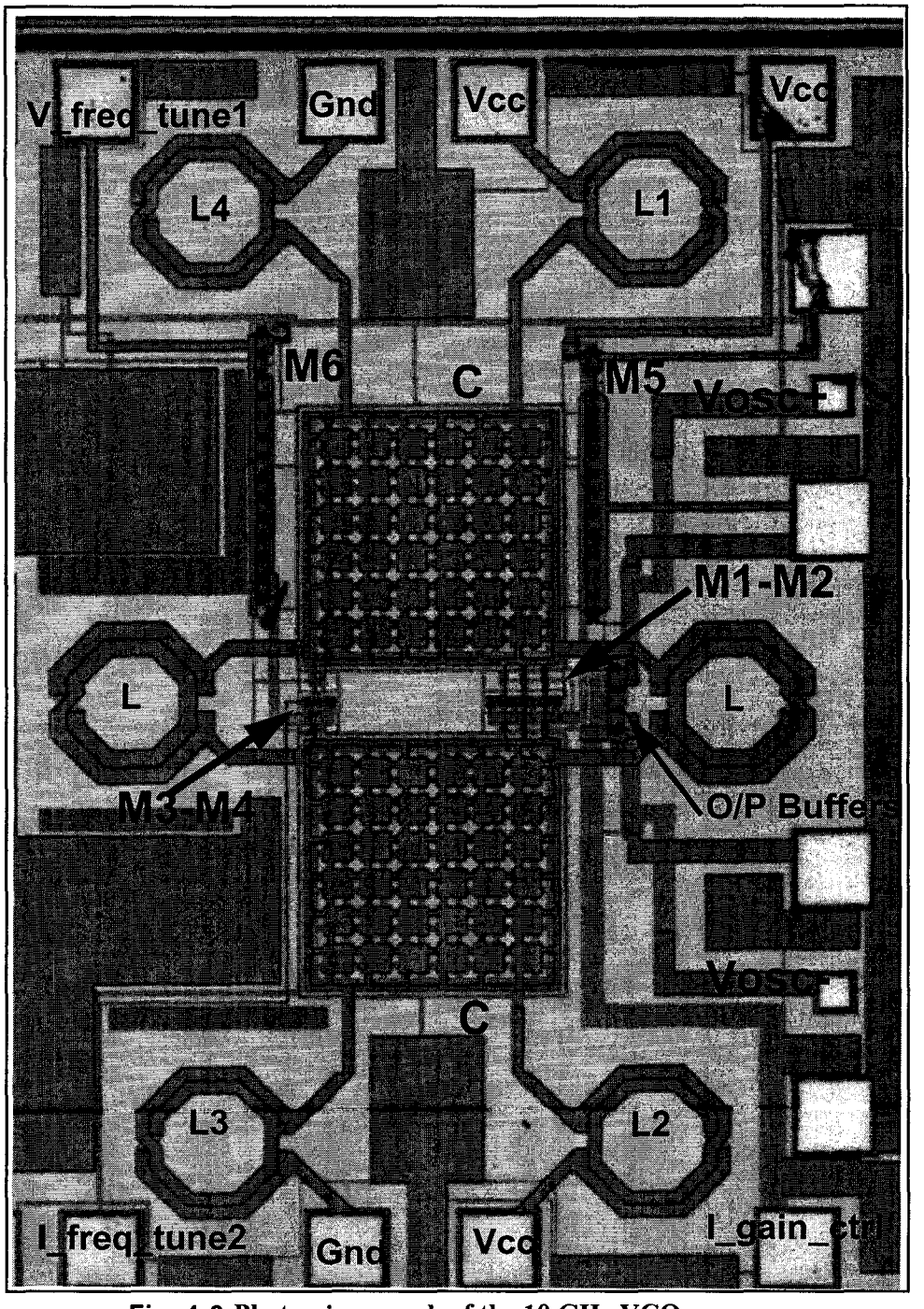


**Fig. 4-6: Photomicrograph of the 10 GHz VCO.**

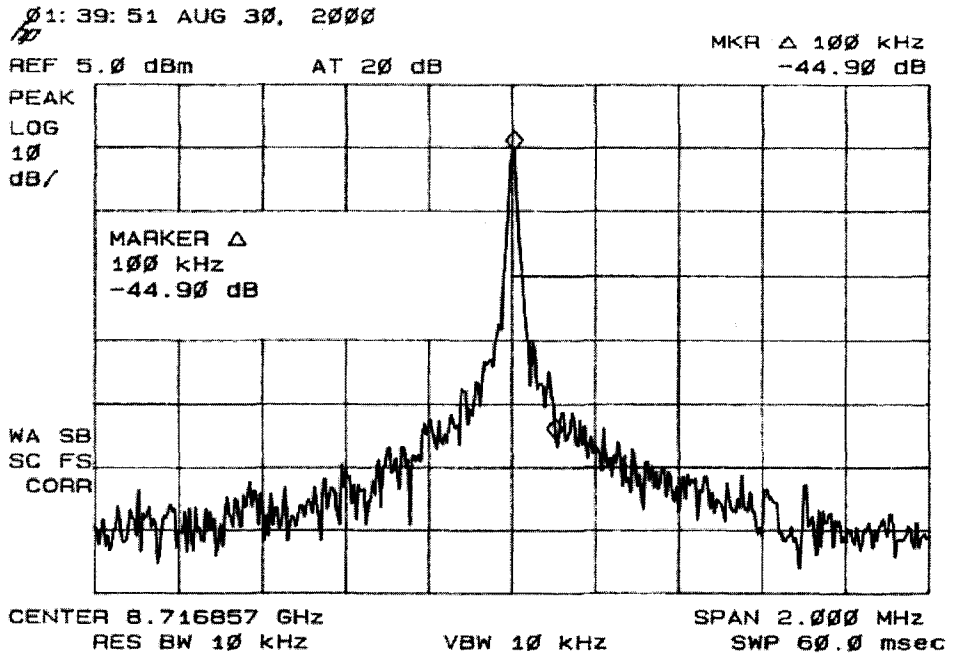


**Fig. 4-7:Measured single-ended output of the 8.7 GHz VCO.**

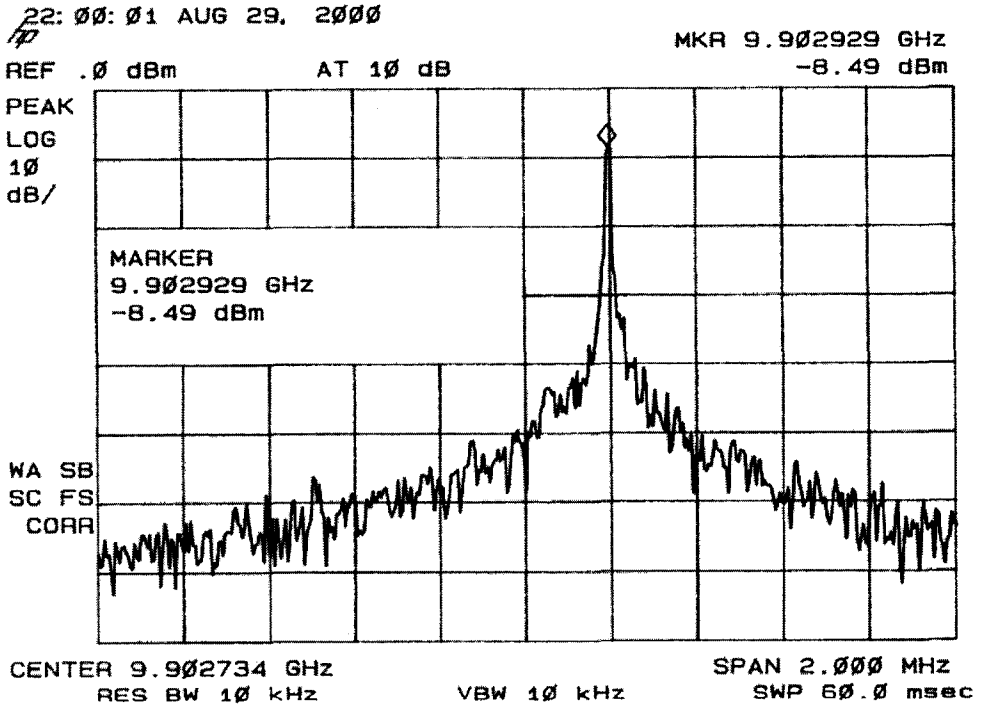


**Fig. 4-8:Measured single-ended output of the 10 GHz VCO.**

pair (M3 and M4) which are smaller in the 10 GHz circuit. Symmetry is conserved throughout the entire layout. All control nodes are bonded for packaging, while ground-

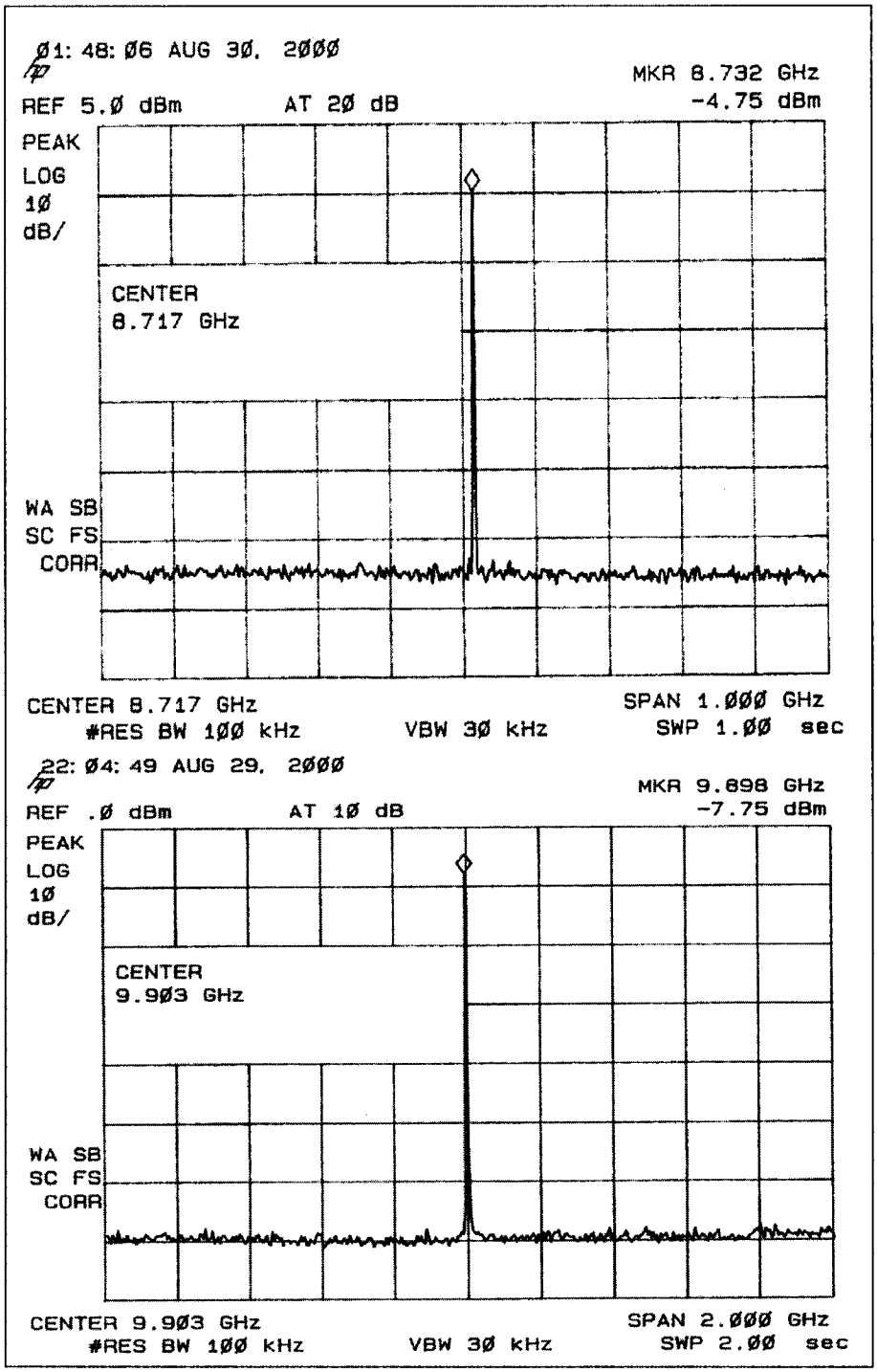


**Fig. 4-9:A wider span is used to measure the power of the output signal of the 8.7 and 10 GHz VCO's.**

signal-ground pads were used for on-chip probing the RF output. The tank's coupling capacitors are built using the top three metal layers only, in order to avoid signal leakage

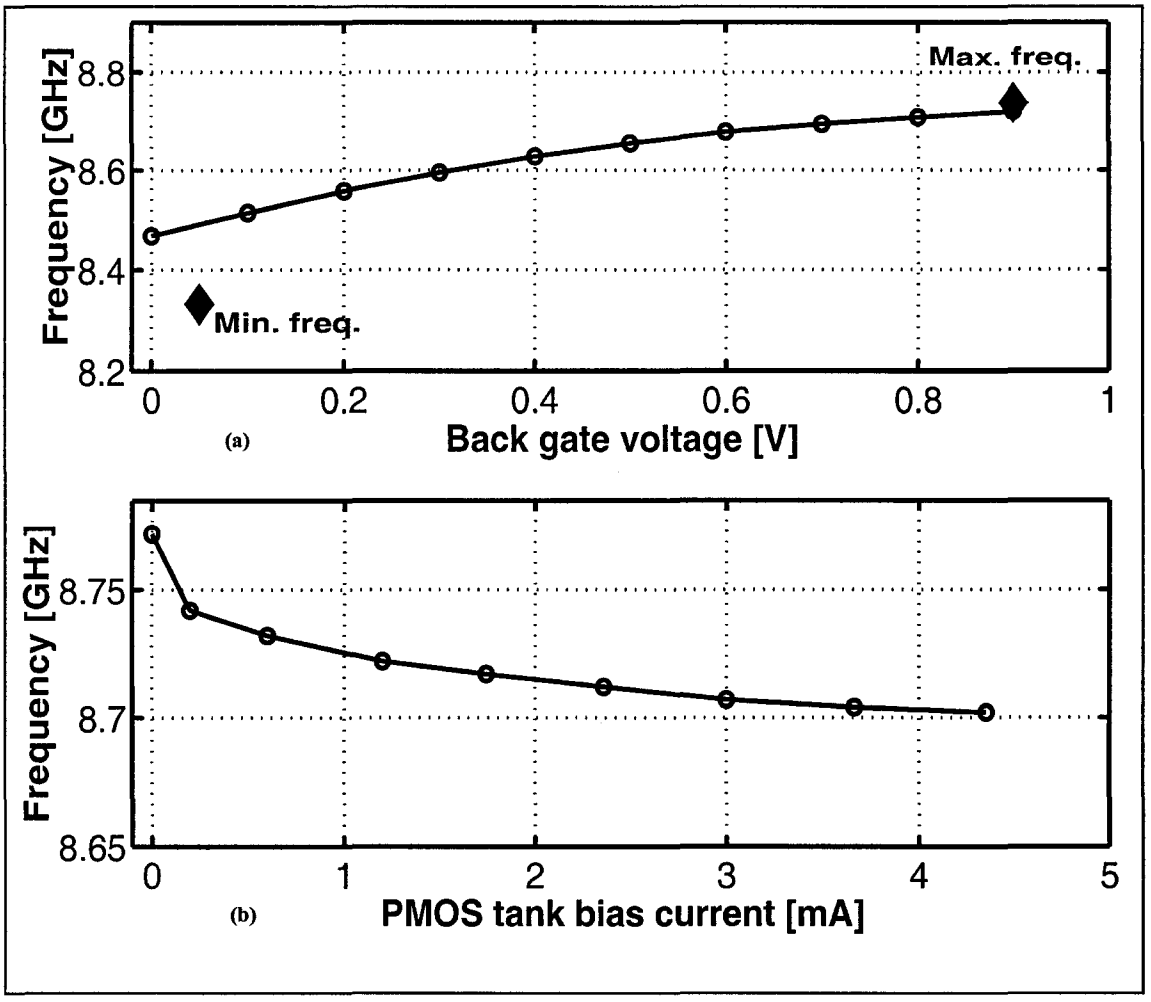


**Fig. 4-10: Frequency tuning versus back-gate voltage (top plot), and versus PMOS tank bias current (bottom plot), for the 8.7 GHz prototype.**

to the substrate. Line widths are set according to RF design guidelines, keeping DC lines thin and AC connections wide and as short as possible.

The measured single-ended output spectrums for the 8.7 and 10 GHz circuits are shown in Figs. 4-7 and 4-8, and were used to directly estimate the phase noise. The latter was -86dBc/Hz and -82dBc/Hz at a 100 KHz offset for the 8.7 and 10 GHz VCO's respectively. Note that the average power of the signal is underestimated due to the narrow span and the resolution bandwidth of the spectrum analyzer. In estimating the phase noise, the signal power was measured using a wider span [7], as shown in Fig 4-9.

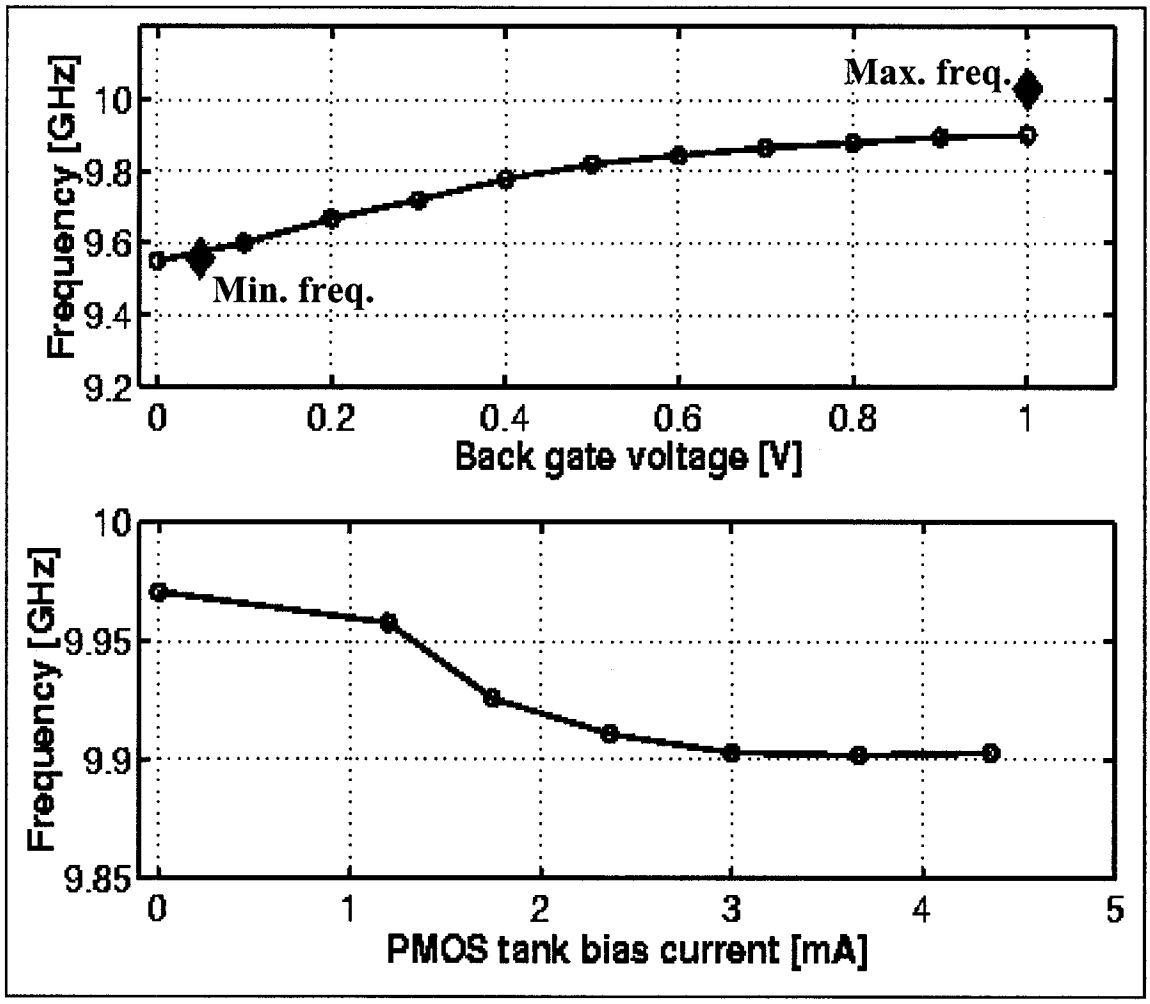


**Fig. 4-11: Frequency tuning versus back-gate voltage (top plot), and versus PMOS tank bias current (bottom plot), for the 10 GHz prototype.**

Two tuning mechanisms can be used to vary the oscillators' frequencies. Fig. 4-10 (top plot) shows the frequency tuning using the back gate voltages of the PMOS tank at a constant bias current of 2.36 mA. Fig. 4-10 (bottom plot) shows frequency tuning using the bias current of the PMOS tank at a constant back gate voltage of 0.85 V for the 8.7 GHz VCO. The two diamond points in the top figure show the minimum and maximum achievable frequencies, when both tuning approaches are combined. A maximum tuning range of 400 MHz is measured for the 8.7 GHz prototype.

Fig. 4-11 (top plot) shows the frequency tuning using the back gate voltages

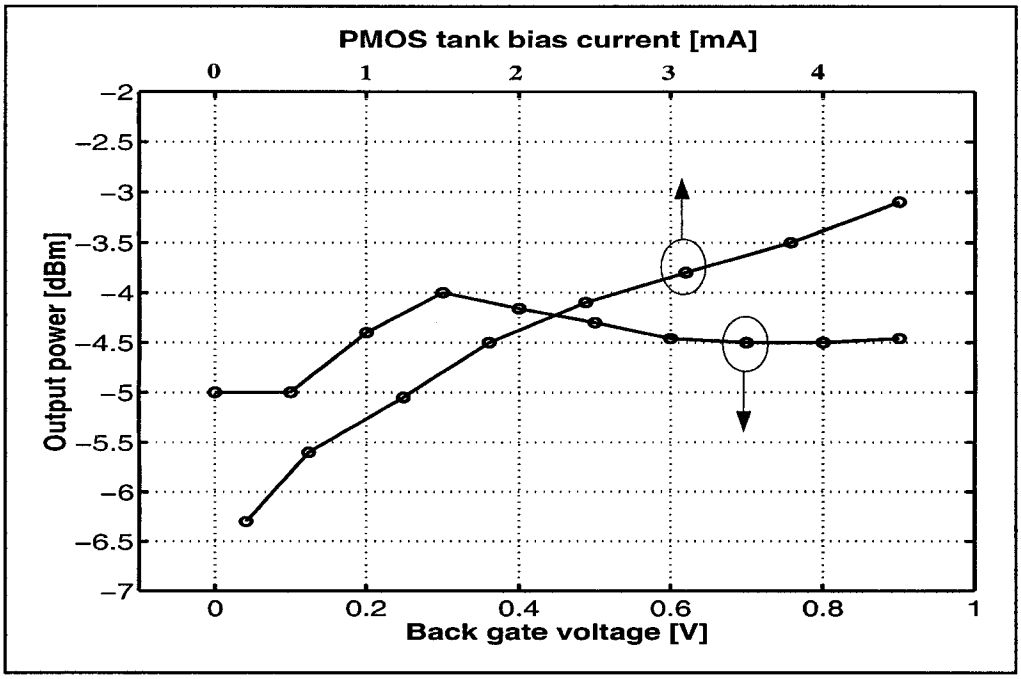


**Fig. 4-12: Measured output power of the 8.7 GHz VCO versus the back gate voltage and the PMOS tank bias current.**

of the PMOS tank at a constant bias current of 3 mA for the 10 GHz VCO. Fig. 4-11 (bottom plot) shows frequency tuning using the bias current of the PMOS tank at a constant back gate voltage of 1 V. The two diamond points in the top figure show the minimum and maximum achievable frequencies, when both tuning approaches are combined. A maximum tuning range of 450 MHz is measured for the 10 GHz prototype.

One added advantage of the proposed topology is that the output amplitude is not very sensitive to the PMOS tank bias current since the $G_m$ is mainly provided by the NMOS tank, and relatively lower current is used in the PMOS tank. Fig. 4-12 shows the measured output power of the VCO's as both the back gate voltage and bias current of the PMOS transistors are varied. The measurements indicate that as the PMOS tank bias current varies from almost 0 mA to 4mA, there is only a 3.5 dBm variation in the output

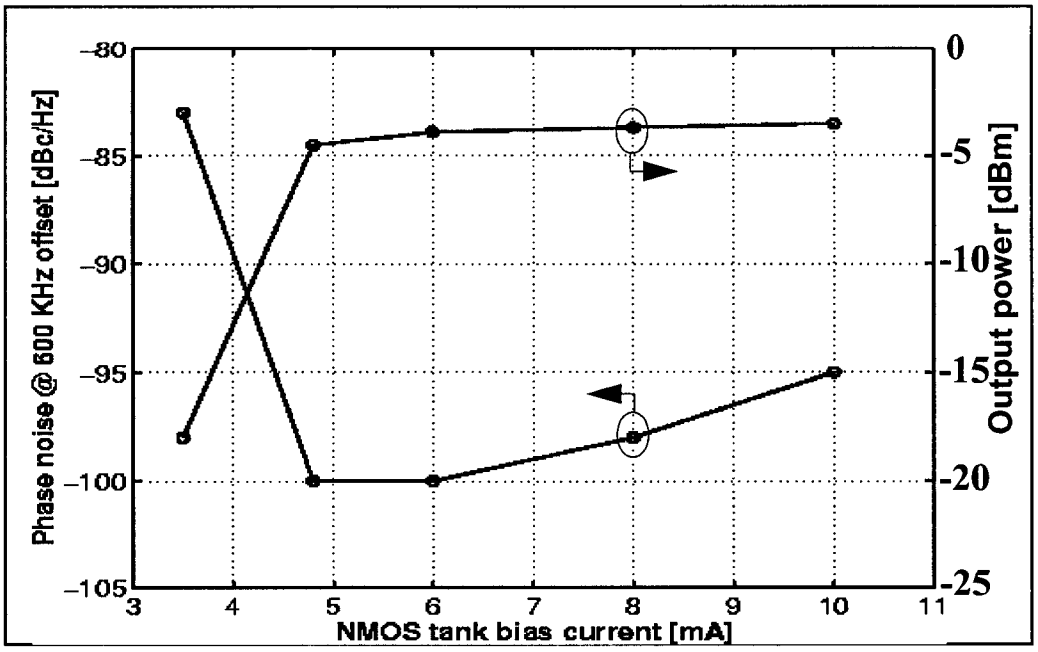


**Fig. 4-13:Measured phase noise @ 600 KHz offset from the 8.7 GHz carrier as function of the NMOS tank bias current, along with the respective measured output power of the signal.**

power for the 8.7 GHz VCO which can be a worthy trade-off for the increased tuning range.

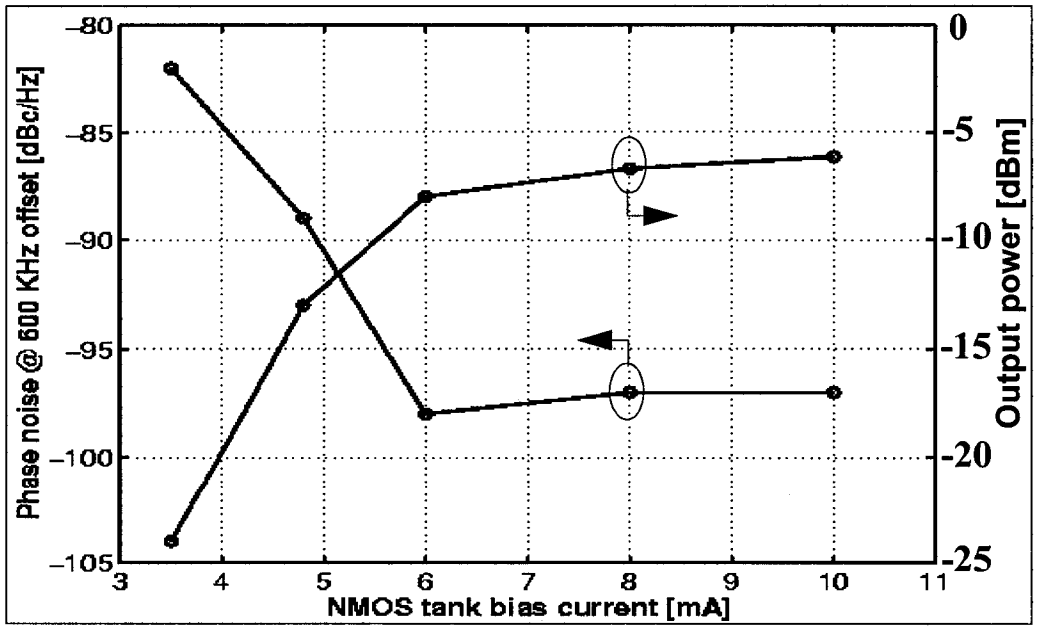


**Fig. 4-14:Measured phase noise @ 600 KHz offset from the 10 GHz carrier as function of the NMOS tank bias current, along with the respective measured output power of the signal.**

The measured phase noise @ 600 KHz offset from the 8.7 and 10 GHz carriers as function of the NMOS tank bias current, along with the respective measured output power of the signal are shown in Figs. 4-14 an 4-13. The VCO output power and phase noise are initially very sensitive to the NMOS current biasing. After power saturation is achieved, increasing the bias current causes a degradation in the phase noise as the devices' channel noise becomes a more prominent noise source.

Table 1 summarizes the characteristics and performance of the presented prototypes.

**Table 1. Summary of the process characteristics, and performances of the two VCO's.**

| | Prototype 1 [8.7 GHz] | Prototype 2 [10 GHz] |
|---|---|---|
| **Technology** | 0.18 μm, 6 metal standard CMOS | 0.18 μm, 6 metal standard CMOS |
| **Substrate resistivity** | 10 Ω/cm | 10 Ω/cm |
| **Thickness of top metal** | 0.99 μm | 0.99 μm |
| **Differential inductor** | 1 nH | 0.85 nH |
| **Estimated quality factor of inductor at $f_o$** | 4 | 5 |
| **Size of M1-M2** | 100 μm | 100 μm |
| **Size of M3-M4** | 100 μm | 50 μm |
| **Size of PMOS buffer** | 50 μm | 50 μm |
| **Area** | 1.5 mm x 1.1 mm | 1.5 mm x 1.1 mm |
| **Supply voltage** | 0.85 V | 1V |
| **Supply current** | 7.1 mA | 9 mA |
| **Power consumption** | 6.0 mW | 9 mW |
| **Phase noise @ 100 kHz offset**<br>**Phase noise @ 600 kHz offset**<br>**Phase noise @ 1 MHz offset** | -86 dBc/Hz<br>-100 dBc/Hz<br>-103 dBc/Hz | -82 dBc/Hz<br>-98 dBc/Hz<br>-101 dBc/Hz |
| **Tuning range** | 400 MHz | 450 MHz |
| **Tuning sensitivity** | 470.6 MHz/V | 450 MHz/V |

## 4.6 Conclusion

A new CMOS VCO structure suitable for high-frequency, low-voltage, and low-power applications was proposed. It maintains the advantages of the original complementary differential LC structure, such as good phase noise and high frequency of operation, while significantly reducing the supply voltage. Two prototypes were built for proof of concept. As shown from Fig. 4-1, they require the lowest voltage supply (0.85-1V) and consume the lowest power (6-9 mW) compared to other oscillators with similar frequencies [1-11].

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# CHAPTER 5 Conclusion

The growing demands in the domain of communications have resulted in the creation of many applications requiring higher frequency of operation, and the nature of mobile communication devices requires low power consumption in order to extend the life time of the batteries used. CMOS has emerged as the reliable and cost efficient technology for the continually increasing complex digital circuits. With its rapid evolution, CMOS technology has also become a contender for RF applications offering the possibility for system integration on a single chip, and providing a common platform for both the front end and the base-band processing. This thesis presented the design procedures and measurements of several LC CMOS voltage controlled oscillators to demonstrate the capability of the CMOS technology in terms of frequency and supply voltage.

Chapters one and two focused on the general requirements of oscillators and the fundamentals in oscillator design. From a technology point of view, the advantages and disadvantages of the CMOS technology as an RF technology were discussed. CMOS, a reliable technology with high yields, is being modified to provide better

passive elements to provide new high frequency capabilities. Although these modifications already made it a serious candidate for RF system implementation, it can only be considered for the lower gigahertz range due to its low resistivity substrate, which increases signal loss and limits its performance in the upper gigahertz range. As discussed throughout this thesis, the most crucial parameter in oscillator design is phase noise; so far, the poor quality factor of inductors on CMOS substrates, which heavily degrades the phase noise of an LC oscillator, is the most difficult obstacle to overcome in the implementation of CMOS VCO's. On the other hand, CMOS offers great advantages in terms of power consumption and system architecture improvements in monolithic system integration.

Chapter three of this thesis presented several circuits optimized for high frequency operation. The results reported in this chapter were published in [1], [2] and [3] and won the award for best student paper at the Midwest Symposium for Circuits and Systems 2000 (MWSCAS'2000). That work was further invited for publication in a special edition of the Transactions on Circuits and Systems (TCAS) [4]. The 4 GHz circuit, optimized for low voltage, operates at 0.85 V, the lowest supply voltage reported at the time of publication. Also, the 10 and 12.5 GHz circuits, which were optimized for high frequency operation, achieved the highest frequencies for CMOS oscillators when published. The optimizations were made while maintaining reasonable performance in terms of phase noise and tuning, in comparison to other state-of-the-art publications (as shown in Figs.3-1, 3-2, 3-12, and 3-13).

Chapter four introduced a novel architecture that allows optimization both in terms of low voltage operation and of high frequency of oscillation. This design

demonstrates the potential of the CMOS technology for low voltage high frequency operation. The design also makes use of a special attribute of the CMOS technology by providing tuning through the biasing of the PMOS devices' substrate, as well as through current tuning. The novel architecture was able to achieve 9 and 10 GHz frequency of oscillation, operating at a 1 V supply. The other aspects of the oscillators are once again very similar to state-of-the-art published work. This work was recently presented in [5].

This thesis proves that there is great potential for standard CMOS processes in the design of high frequency VCO's, especially with the continuous research in improving the quality of the passive elements in the CMOS process. This work did not address the problems of system integration in the CMOS platform, which is of great industrial interest. The European HIPERLAN and the 802.11 standard is driving RF CMOS system integration at the 5-6 GHz range, a very challenging task, which seems to be slowly met through circuit innovations.

## 5.1 References

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