ELECTRONIC ANALOG MULTIPLICATION USING TRANSISTORS

by

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TABLE 1-1

LIST OF PRINCIPAL SYMBOLS

C	:	capacitance of the ramp charging capacitor
E	:	charging current supply voltage
e_a	:	pulse width modulating voltage
E_A	:	pulse width modulating voltage bias
e_b	:	pulse amplitude modulating voltage
e_c	:	voltage across capacitor C
i	:	charging current of capacitor C
i_b	:	base current of bidirectional switch
i_c	:	collector current of bidirectional switch
i_D	:	diode reverse current
i_e	:	emitter current of bidirectional switch
i_L	:	current from E through R and L
i_o	:	i at $t = 0$
i_{Lo}	:	i_L at $t = 0$
$i_L(t_1)$	:	i_L at $t = t_1$
$i_L(t_2)$	:	i_L at $t = t_2$
$i_L(\uparrow)$	:	i_L at $t = \uparrow$
L	:	inductance of current source inductor
R	:	resistance of current source resistor
R_T	:	transformer equivalent resistance
t	:	time

t_1 : start of clipping period

t_2 : start of restoration period

$\uparrow$: end of cycle; repetition period of pulse carrier

v : $e_a + E_A$

α : one half of damping factor

α : emitter to collector current gain

α_1 : collector to emitter current gain

β : resonant frequency

β_0 : $\sqrt{\alpha^2 + \beta^2}$, undamped resonant frequency

PART I

ELECTRONIC ANALOG MULTIPLICATION USING TRANSISTORS

Introduction

An investigation of the solution of a problem by analog computation consists of examining the behavior of a particular physical system conceived in such a way that the different variables which describe it develop according to laws analogous to those which describe the system under study.

Machines which use the laws governing electrical phenomena as analogs have an advantage over other machines in that very rapid operation is possible, which permits condensing into a short time a long operation, and the expansion of rapid phenomena to cover relatively long times.

It is possible to develop electrical analogs for a number of elementary mathematical operations, including addition, subtraction, multiplication, division, differentiation, and integration. An electronic analog computor consists of many such units connected together in such a way that either the voltages or the currents of the system obey electrical laws analogous to the natural laws of the system under study. The voltage or current at a particular point in the system will then contain information analogous to the behavior of the analogous variable of the system under study.

Time is usually the analogy of the independent variable of the system under study because electrical phenomena may be conveniently expressed as a function of time.

The six basic mathematical operations mentioned above may be performed with varying ease. Addition, subtraction, integration, and differentiation are relatively simple, all four being linear operations. However multiplication and division are non-linear operations. The basic laws of passive electrical circuitry containing only bilateral linear devices such as resistors, inductors, and capacitors are linear, and so are incapable of providing an analog of a non-linear phenomenon such as multiplication. Multipliers must therefore employ non-linear devices, such as switches, rectifiers, magnetic saturable reactors, or active devices which may have non-linear characteristics.

Multipliers are of course not made up of one such device, but a suitable combination of non-linear and linear devices, both active and passive. The use of transistors as active devices, both linear and non-linear, has considerable merit. Transistors are of small physical size, and work at very low power levels relative to vacuum tubes. They also have a considerably longer lifetime, and far greater reliability than vacuum tubes. This combination of small size and low power levels enables much smaller units to be built with less worry about thermal dissipation problems. The lifetime and reliability advantages are invaluable in today's complex and large installations.

However, many of the linear and some of the non-linear characteristics of transistors are strong functions of temperature and are disposed to change as the transistor ages, necessitating careful compensation against such changes in characteristics.

Transistors in Analog Computation

It is possible with transistors to construct current amplifiers whose input impedance is negligible compared to their output impedance. This makes it possible to use current as an analog. (1) The output of any amplifier will appear to be a current source as seen by subsequent stages, regardless of how many are connected in series to the output. If the output current of an amplifier is a function of the number of stages which it drives, and if this current represents some dynamic variable at that point, the analogy will not be true, and errors will be introduced.

It is also possible with transistors to construct voltage amplifiers whose input impedance is large compared to their output impedance. Such devices may be used with the standard voltage analog techniques developed for vacuum tube computors. (2)

Either type of amplifier will inherently suffer from considerable drift if it is direct coupled. (3) This is the major disadvantage of transistor computor amplifiers. One possible way to overcome this is to use high frequency choppers in conjunction with amplifiers which are not direct coupled (4), and then demodulate to recover the input information, either with a second synchronous chopper or by other means.

The question of amplifier drift is of secondary importance if the voltage or current analog is alternating. Alternating current computors are not very practical, however, since the phase shift in amplifiers and connecting wires must be

rigidly controlled, and since the high gain amplifiers used have a tendency to pick up extraneous signals at carrier frequency from adjoining components. Direct voltages and current analogs seem to offer more promise of accurate results if the drift problem can be controlled.

The control of the drift problem may be considered in two ways. The most obvious is to build better amplifiers and transistors and enclose the units in thermally insulated containers [4]. At the present state of the art, it is the transistors themselves which limit the amount of improvement possible by these means. The characteristics of transistors are very strong functions of temperature, and even a change of a few micro-amperes in the collector current of the first stage of a high gain amplifier may result in a drift so large that the output transistor will either be saturated fully on or cut completely off, reducing the amplification of the amplifier to the point where it is virtually useless. Higher dissipation at high signal levels can easily cause a change of the order of magnitude mentioned.

A second way to control the drift problem is to limit the time during which the computor generates a solution. If the time of computation is fairly short it may be assumed that the average dissipation in the stages is small, and the drift will not be nearly so important. One practical way to do this is to generate a solution repetitively, that is, the computor generates a solution, resets itself to the initial conditions, and generates another solution, and so on. The output of a computor of this

type is much more difficult to read than for a standard computor. It may be displayed on a cathode ray tube, but practical writing recorders are generally far too slow to follow the output. One advantage of this type of computor is that the observer may see the solution change on the cathode ray tube as a function of various parameters far more rapidly than he could arrive at the same results with standard computors.

Multiplication

Requirements for a multiplier for a repetitive transistor analog computor include high enough frequency response to handle the solution and any higher harmonics which may be present due to the repetitive processing, the ability to accept input signals of either polarity (four quadrant operation), an accuracy of multiplication sufficient to ensure that significant errors are not introduced into the solution due to the multiplication process, and drift-free operation.

Since cathode ray oscilloscopes are voltage sensitive devices, it is convenient to use voltage as the analog variable. A voltage analog multiplier may be converted to current analog operation by providing each input with an amplifier of low input and output impedance .

The perfect multiplier will accept two input signals of any polarity and give an output which is precisely the product of these signals. Any deviation from this ideal by a practical multiplier constitutes an error, usually expressed as a percentage of the true product value.

Analog computors have limits to the magnitude to which a voltage may rise before overloading one or more of their components. This magnitude is termed the dynamic range of the components, and a multiplier should not limit the dynamic range of a system unduly.

Out of many possible methods of multiplication, only a limited number are suitable for transistor repetitive analog computor use. All mechanical and electro-mechanical devices are unsuitable because of their poor frequency response due to the inertia of mechanical parts. Multipliers employing cathode ray tubes are suitable, but are large and power consuming, which does not make them attractive for use with transistors. The remaining possibilities are completely electronic.

(1) Multipliers Based on Mathematical Relations

Multiplication may be based on the relation

$$e_a e_b = \frac{(e_a + e_b)^2 - (e_a - e_b)^2}{4}$$

The error and dynamic range of the square law characteristic of the device or devices which perform the squaring in this type of design determine the error and dynamic range of the result. A multi-segment diode function generator is perhaps the best squaring device yet developed, but at voltage levels possible in transistor circuitry it is not very accurate. Other squaring devices suffer from a poor dynamic range. In addition,

almost all these devices are unilateral, so that they will accept inputs of only one polarity, which causes grave difficulties if the multiplier is to be operated in all four quadrants.

Another mathematical relation which makes it possible to multiply is

$$\log_n e_a e_b = \log_n e_a + \log_n e_b \quad .$$

Since the logarithm of a negative number is not defined, this relation would apply only to single quadrant operation. All the logarithmic devices used would have to operate on the same base, and three would be required, although switching could conceivably reduce this number.

(2) Multipliers Incorporating Saturable Magnetic Cores

A multiplier may be constructed using the non-linear properties of rectangular loop magnetic cores and switching transistors [6]. The operation of a multiplier which works only for one polarity of each input voltage (single quadrant operation) will be described. This multiplier may be expanded to four quadrant operation [7]. The circuit of the single quadrant multiplier is given in figure 1-1, taken from Milne [6], as is the following description of the operation of the circuit.

"In the half cycle when diode D_2 blocks the drive voltage V_{AC} from the circuit, the signal voltage V_1 resets the core flux from $+ \phi_s$ (where it was driven by V_{AC}) to ϕ_1 according to the relation

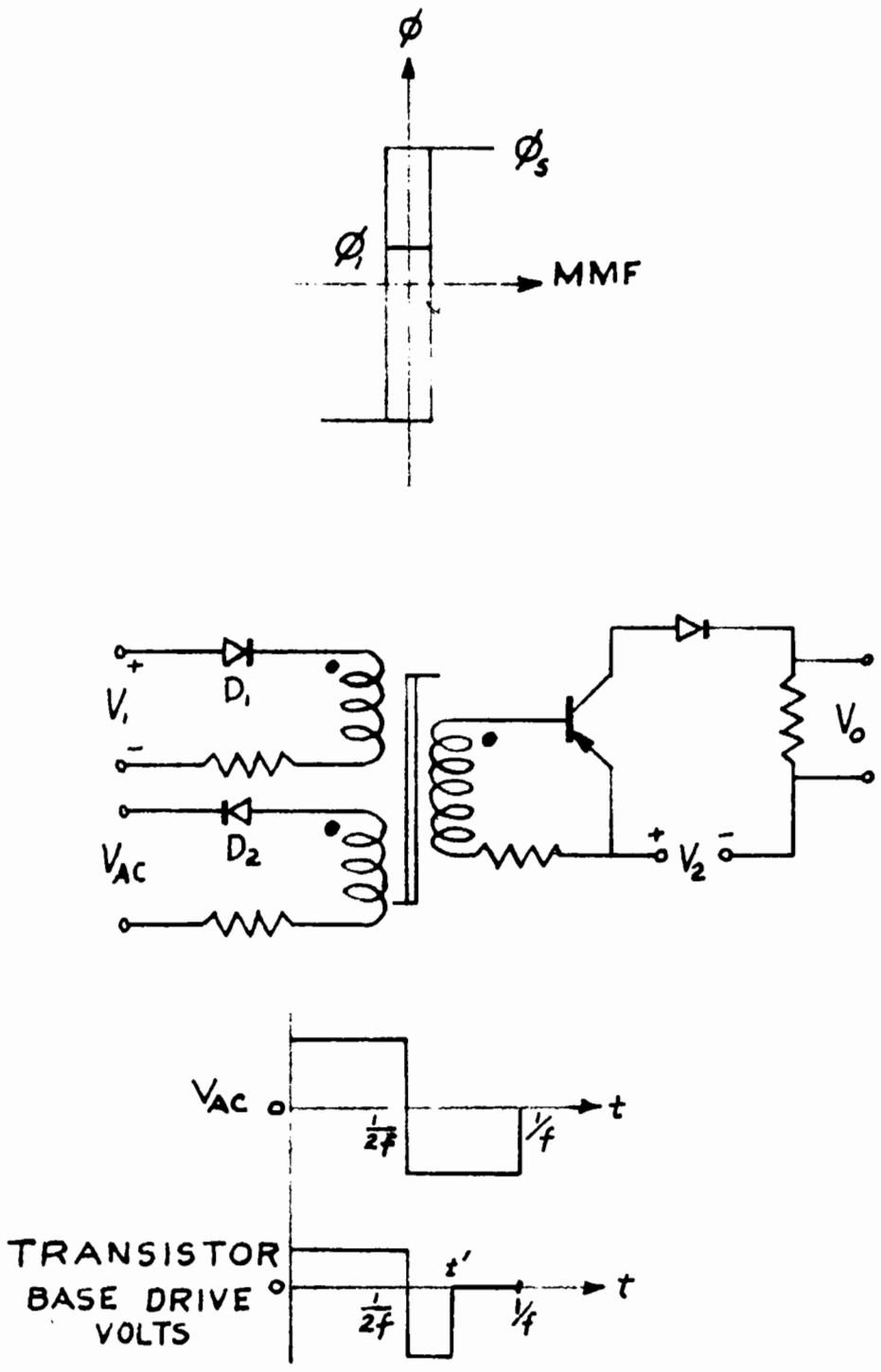


FIG. 1-1
MULTIPLYING CIRCUIT USING MAGNETIC CORE

$$\phi_s - \phi_1 = \int_0^{\frac{1}{2}f} V_1 dt = \frac{V_1}{2f} \qquad (1)$$

In the next half cycle the drive voltage returns the flux to ϕ_s, but because $V_{AC} > V_1$, the operation is completed in a period $\frac{1}{2f}$ to t', where

$$V_{AC}\,(t' - \tfrac{1}{2f}) = \phi_s - \phi_1 \qquad (2)$$

and so from equation (1) and (2)

$$t' - \tfrac{1}{2f} = \frac{V_1}{2V_{AC}} \frac{1}{f} \quad . \qquad (3)$$

"While the flux is changing from ϕ_1 to ϕ_s the base circuit voltage bottoms the transistor and the second signal V_2 appears as output voltage. The mean output voltage over a complete cycle is therefore

$$V_o = \frac{V_2\,(t' - \frac{1}{2f})}{1/f} \qquad (4)$$

whence from equation (3)

$$V_o = \frac{V_1 V_2}{2V_{AC}}$$

Thus the mean output voltage depends on the product of the two

signal voltages." "With a four quadrant version of this circuit handling voltages of 5 - 50 volts Van Allen [7] reports an overall accuracy of about 2%. Switching frequencies of up to 5 KC/S have been successfully used."

This circuit would be suitable for analog computor operation, except when V_1 must pass through zero, when the errors would be expected to be rather large due to the width and departure from rectangularity of the core characteristic. The circuit as it stands could be converted to two quadrant operation by removing the diode in the collector lead of the switching transistor, converting it to a bidirectional switch, as described in detail in section two of this thesis.

Switching frequencies of 5 KC/S imply that the frequencies of V_1 and V_2 must be small compared to 5 KC/S. This limits the high frequency response of the circuit to the region of 50 cps, which is rather low for repetitive operation.

(3) Variable Gain Devices [8]

An amplifier whose gain is a linear function of an input voltage may be used to multiply. In figure 1-2 the amplifier gain A may be defined by $e_o = Ae_1$. If $A = ke_2 + k_o$ where k and k_o are constants then

$$e_o = ke_1e_2 + k_oe_1.$$

The term k_oe_1 must be subtracted from the output to give the desired relation $e_o = ke_1e_2$.

If the gain is a monotonic but not necessarily linear function of e_2, and if two identical units can be constructed,

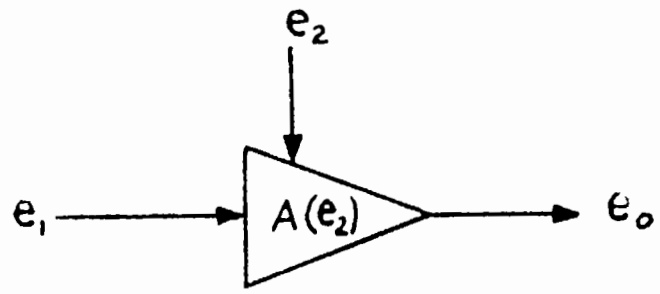


FIG 1-2

LINEAR VARIABLE GAIN AMPLIFIER

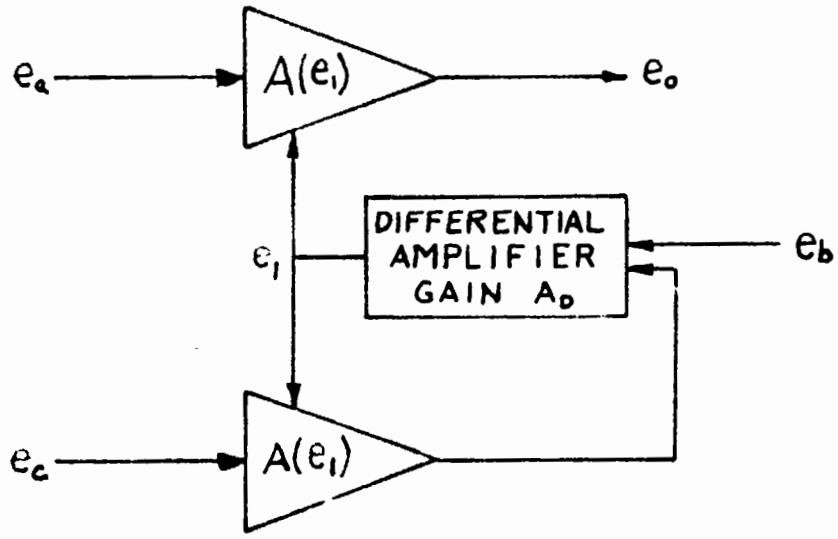


FIG 1-3

MULTIPLICATION WITH NON-LINEAR AMPLIFIERS

it is possible to obtain an accurate product output [9]. The circuit for this method of multiplication is shown in figure 1-3.

The equations describing this circuit are

$$e_1 = A_D \left(e_c \, A(e_1) - e_b \right)$$

$$e_o = e_a \, A(e_1)$$

which may be combined to yield

$$e_o = \frac{e_a e_b}{e_c} + \frac{e_a e_1}{A_D e_c} \quad .$$

If A_D is very large, e_o will be proportional to the product $e_a e_b$.

The grounded base current gain of a junction transistor is very nearly equal to the four-pole parameter h_{21} if the load resistance is small [10]. A junction tetrode transistor has a second base connection through which current may be introduced into the base, and the four pole parameter h_{21} is a function of the magnitude of this current. Published curves [11] show that the variation of h_{21} with the second base current I_{b2} is essentially linear over a large portion of its range. Assuming a law of the form

$$h_{21} = \frac{I_2}{I_1} = h_{21}(o) - mI_{b2},$$

the output current I_2 of the device is then

$$I_2 = h_{21}(o)I_1 - mI_{b2}I_1 ,$$

where $h_{21}(o)$ is the value of h_{21} at zero base two current, and m is the slope of the h_{21} variation with I_{b2}. This output contains the desired product term and a second term involving the input current I_1, which must be subtracted to leave only

$$I_2 = -mI_{b2}I_1$$

The major disadvantage of this device is the difficulty of obtaining four quadrant operation. To do so both I_1 and I_{b2} would have to be biassed in the center of their characteristic and then the unwanted direct current and signal frequency terms subtracted at the output. With two such biases in operation it is likely that drift would be a serious problem unless, with balanced operation, one of the subtractions is performed automatically. This type of operation requires carefully balanced units, which are difficult to keep in their balanced condition due to temperature effects and aging.

(4) Time Division Methods

If either the duty ratio or the repetition rate of a train of rectangular pulses is a linear function of one input variable, and the amplitude of the pulses is a linear function of a second input variable, the spectrum of the pulse train contains a component proportional to the product of the two variables.

The pulse train shown in figure 1-4a, which is duty-ratio modulated, has a repetition period T, so that the leading edges of the sequence of pulses are at

$$t = mT$$

and the trailing edges at

$$t = kmT + mT \; ; \quad 0 \leq k < 1$$

where m may be any positive integer, and k, which may be a function of time, represents the duration of the pulse.

Assuming k to be constant, the Fourier series of the sequence of pulses is [13]

$$f(t) = k + \frac{1}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sin 2\pi mk \cos \frac{2\pi mt}{T}$$

$$+ \frac{1}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} (1 - \cos 2\pi mk) \sin \frac{2\pi mt}{T}$$

Consideration of the form of the expansion shows that it is also a valid representation of the sequence of pulses for k a function of time [13]. So if

$$k = \frac{a}{2} (1 + b \cos 2\pi f_1 t)$$

where $0 \leq a < 1$, $0 \leq b < 1$,

substituting in f(t) and performing considerable simplification

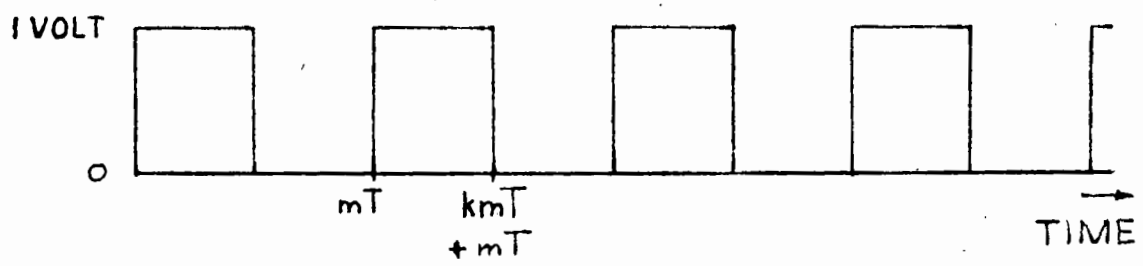


FIG 1-4a

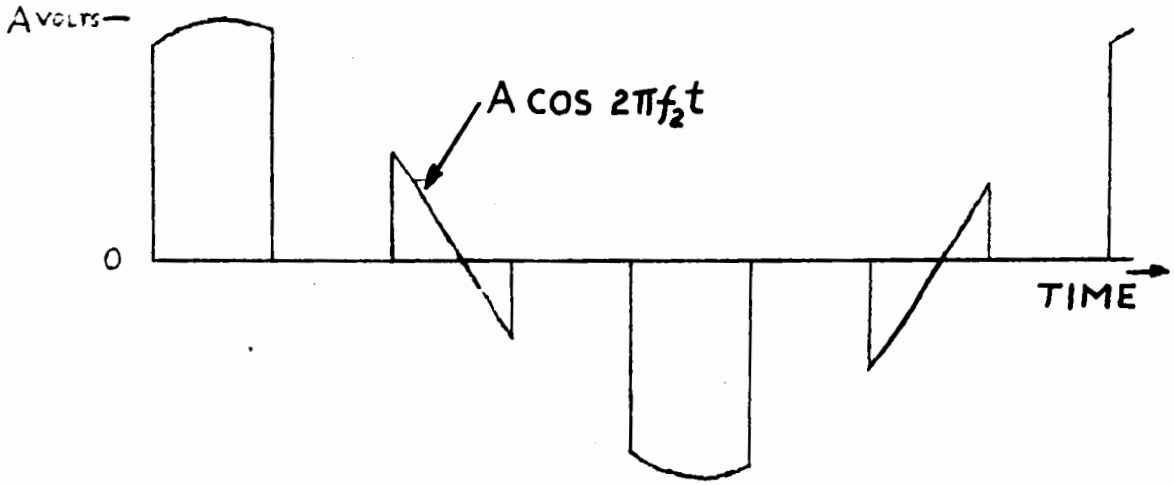


FIG 1-4b

PULSE WAVEFORMS

gives the result [13]

$$f(t) = \frac{a}{2}(1 + b\cos 2\pi f_1 t) + \frac{1}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sin\frac{2\pi mt}{T}$$

$$+\frac{1}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{|n|}(mab\pi)\sin(ma\pi + |n|\frac{\pi}{2})$$

$$\cos 2\pi(\frac{m}{T} + nf_1)t$$

$$+\frac{1}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{|n|}(mab\pi)\cos(ma\pi + |n|\frac{\pi}{2})$$

$$\sin 2\pi(\frac{m}{T} + nf_1)t$$

If the set of pulses of figure 1-4a is amplitude modulated as in figure 1-4b, the modulation may be described mathematically by multiplying the original rectangular pulse function by a modulating factor of the form $A\cos 2\pi f_2 t$. Since the rectangular pulse function and the Fourier series are completely equivalent, the series may be used instead of the rectangular pulse function to obtain an expression for the complete output [14]. After simplification the result is

$$f(t) = \frac{a}{2}A\cos 2\pi f_2 t + \frac{a}{2}(b\cos 2\pi f_1 t)(A\cos 2\pi f_2 t)$$

$$+\frac{1}{\pi}\sum_{m=1}^{\infty}\frac{A}{2m}\left(\sin 2\pi(\frac{m}{T} + f_2)t + \sin 2\pi(\frac{m}{T} - f_2)t\right) +$$

$$+\frac{1}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{A}{2m}J_{|n|}(mab\pi)\sin(ma\pi+|n|\frac{\pi}{2})$$

$$\left(\cos 2\pi(\frac{m}{T}+nf_1+f_2)t+\cos 2\pi(\frac{m}{T}+nf_1-f_2)t\right)$$

$$+\frac{1}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{A}{2m}J_{|n|}(mab\pi)\cos(ma\pi+|n|\frac{\pi}{2})$$

$$\left(\sin 2\pi(\frac{m}{T}+nf_1+f_2)t+\sin 2\pi(\frac{m}{T}+nf_1-f_2)t\right).$$

The first term of this expression is at the pulse amplitude modulating frequency and must be subtracted. The second term is the desired product term, and the other terms are at frequencies involving the repetition rate of the pulse train, which may be large with respect to the modulation frequencies.

If both the modulation frequencies are much less than the carrier frequencies, a low pass filter will remove all terms but the desired product term and the term at amplitude modulation frequency, with the exception of some terms at frequencies involving higher harmonics of the duty ratio modulation frequency. The coefficients of these higher harmonic terms are high order Bessel functions, and consequently they are of small size.

If the modulating frequencies are kept much smaller than the carrier frequency, the accuracy of a time division multiplier should depend only on the linearity of the modulation characteristics, the ability of the circuitry to generate and

handle rectangular pulses, and the low-pass filter characteristics.

There is no doubt that this system of multiplication is considerably more involved than any of those mentioned previously. However, the frequency response is limited only by the carrier frequency, which may be in the tens of kilo-cycles in practical units. Drifts in the transistor parameters cause little effect on the output with this system, since most of them are employed as switches. There is no restriction on either waveform passing through zero with practical circuitry, so that four quadrant operation with no great loss of accuracy if one of the inputs is small may be achieved.

PART II

A MULTIPLIER DESIGN

Introduction

A multiplier has been constructed utilizing the time division principle mentioned previously. The reasons for employing this particular configuration are two-fold: first, it is one of the most promising of the possibilities; and second, it permits the examination in some detail of some pulse circuitry which is unique to the transistor art.

Since frequency response limitations of the transistors would make it quite difficult to have high enough a repetition rate to permit variation of that parameter, the repetition rate of the basic pulse train remains constant in this design, and the duty ratio is varied. This permits somewhat simpler circuitry.

The operation of the multiplier is as follows. A pulse generator drives a simple pulse-width modulator which supplies pulses whose amplitude is very nearly independent of their width, but whose width is a linear function of a pulse width modulating voltage. These pulses drive a bidirectional switch, the output of which is a train of pulses in which the width characteristic of the driving pulse train is preserved. The envelope of this pulse train is proportional to a second modulating voltage.

The pulse train is inverted in an amplifier and passed through a low-pass filter to remove the higher frequency components, leaving only the desired product term, and a term

proportional to the pulse amplitude modulating voltage.

This latter term arises due to the method of pulse amplitude modulation, which does not suppress the modulating voltage. This term is subtracted at the output of the filter, leaving as output the desired product term.

The Pulse Width Modulator

For purposes of analysis the pulse generator is considered to be a part of the pulse width modulator.

A multivibrator is used as the pulse generator. As can be seen from figure 2-1, the configuration used in standard[15], although the frequency of operation is considerably affected by the non-linear and partly reactive load presented by the following transistor and its coupling network. In order to assure the desired constancy in the repetition rate of the pulse train, the multivibrator is triggered by a point-contact sinusoidal oscillator operating at a multiple of the repetition rate of the multivibrator. This point-contact oscillator is a standard "negative resistance" type of circuit [16]. This precaution is necessary due to the sensitivity of subsequent circuitry to the repetition rate of the driving pulse train.

The output of this pulse generator as seen at the base of the following transistor is shown in figure 2-2. The repetition period of the positive pulse is 72 microseconds, and its width is 15 microseconds. The peak-to-peak amplitude of the pulse train is approximately 2 volts.

This input to the following transistor will cause it

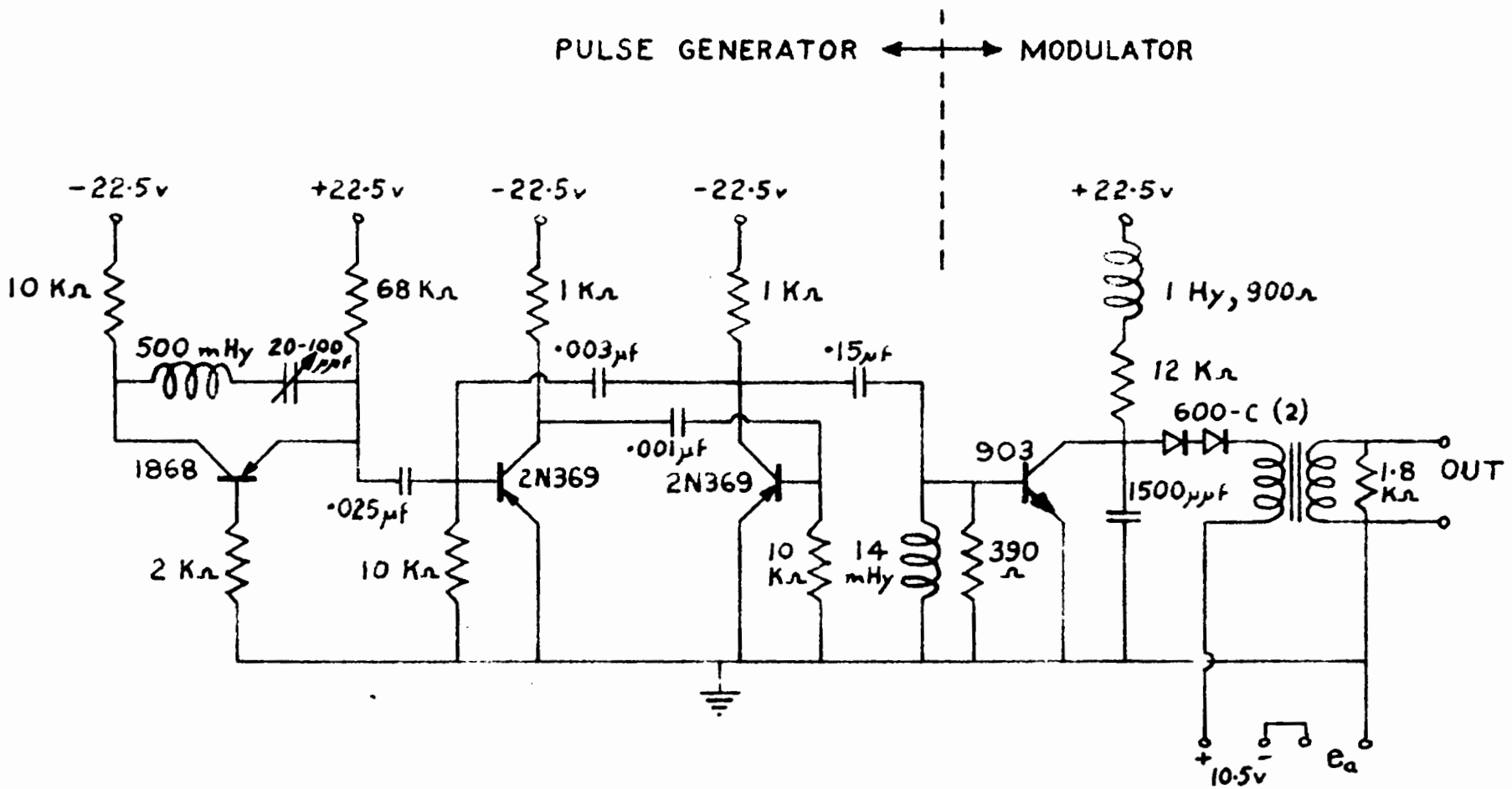
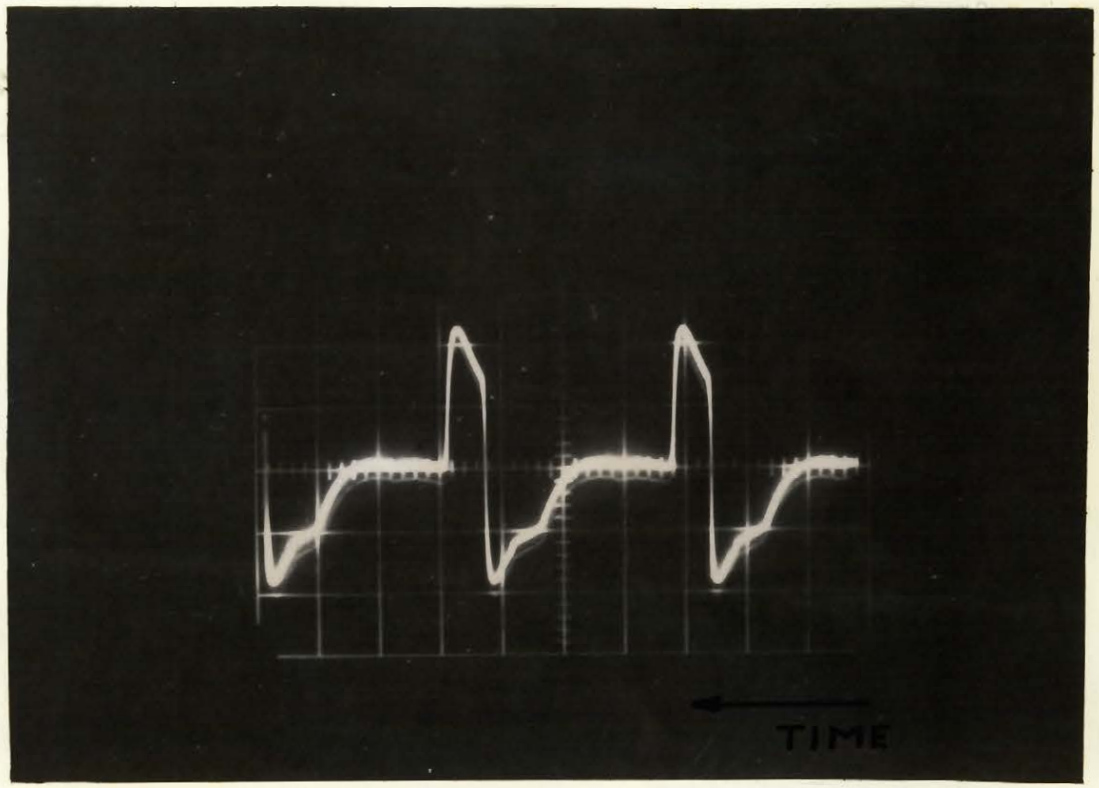


FIG 2-1
PULSE WIDTH MODULATOR



Horizontal : 20 μsec./div.

Vertical : 0.5 v./div.

FIG. 2 - 2

MULTIVIBRATOR OUTPUT

to act as a switching transistor, presenting an impedance of several megohms for 57 microseconds, and then a few ohms for 15 microseconds to circuits connected between its collector and emitter.

Figure 2-3 represents an equivalent circuit of the pulse width modulator, in which the switching transistor has been replaced by a perfect switch, the diode D_1 by a perfect diode bypassed with a current source, and the transformer by an assumed resistive equivalent load R_T.

Since just before the start of a cycle the switch is closed, e_c, the voltage appearing across the condenser, will start at zero. Because of the large dynamic impedance of the resistance-inductance combination in series with the battery E of figure 2-3, the condenser will charge up as if it were being charged from a constant current source. This results in a linear ramp of voltage appearing across the condenser.

If the condenser is charged through a resistance alone, a linear ramp will also result, but as is shown in subsequent analysis, the presence of the inductor tends to considerably reduce error terms, and to permit the ramp to rise above the value of the supply E, permitting the use of a smaller source.

At time t_1 the voltage across the condenser reaches the value $v = e_a + E_a$, where e_a is the pulse width modulating voltage and E_a the bias in series with it. At this time diode D_1, which has been in its high resistance state, switches to its low resistance state and the charging current from battery E flows through the diode, transformer primary, and the two series

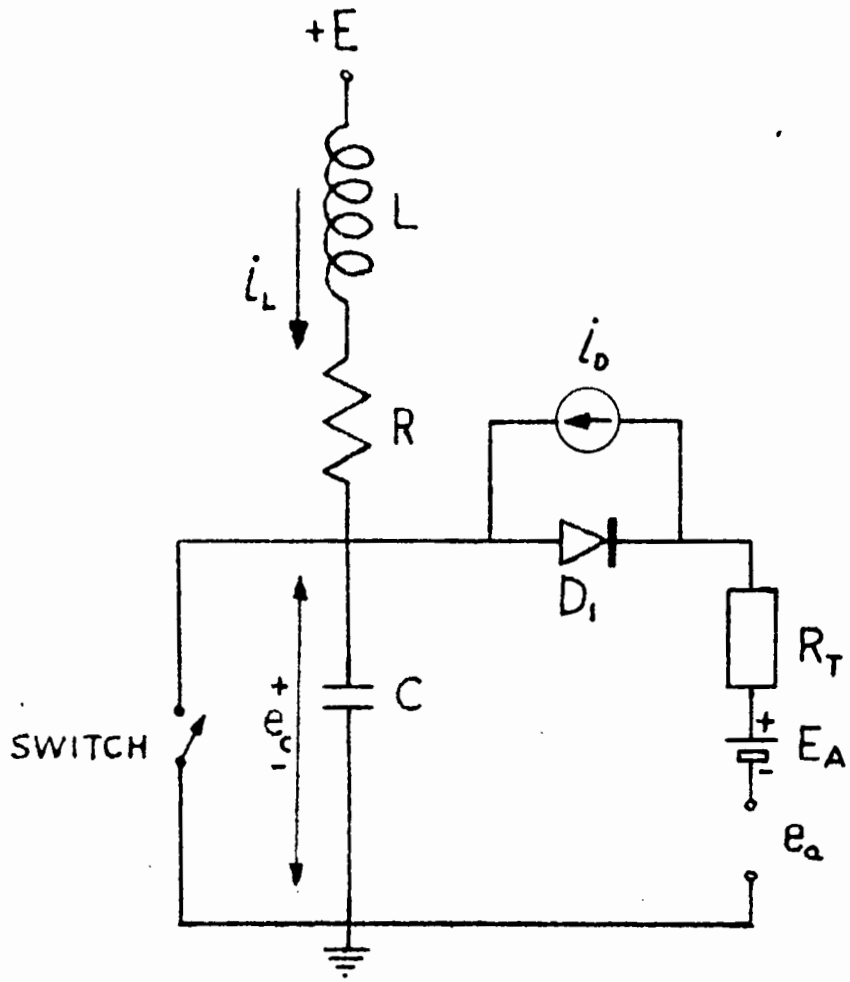


FIG 2-3
PULSE WIDTH MODULATOR
EQUIVALENT CIRCUIT

supplies. Since this path is quite low resistance, the voltage e_c levels off at a voltage essentially equal to v. The almost constant current flowing through the transformer primary causes a rectangular pulse to appear across its secondary. 57 microseconds after the cycle started, the switch is closed by the positive pulse from the multivibrator, e_c drops to zero, the diode resumes its high resistance state, the voltage at the secondary of the transformer drops to zero, and the charging current flows through the switch.

The output at the secondary of the transformer is a pulse when the diode is conducting and zero otherwise. The diode will be conducting only between the times t_1 and 57 microseconds. But because the slope of e_c is linear, t_1 is a linear function of the voltage v, which assumes the role of a clipping voltage. Hence the width of the pulse at the transformer output is a linear function of voltage v, and hence of the voltage e_a.

If the series resistance-inductance constant current source is not ideal, so that the current charging the capacitor is not constant, errors are introduced in the slope of the ramp, and hence in the pulse width. This effect is discussed in the detailed analysis which follows.

From the characteristic curves for junction transistors it is seen that when this type of transistor is saturated "on" the collector emitter resistance is of the order of a few ohms, while when "cut off" this resistance rises as high as several megohms [17]. So the switching transistor may be replaced by a perfect switch with little error.

It is sufficient to represent the transformer with an equivalent load since in the subsequent analysis no detailed calculations are to be made which would involve the transformer input impedance. To do such calculations would be rather difficult, since equivalent circuits valid for pulse circuitry would have to be used, and since the transformer load is the base of a grounded emitter switching transistor in parallel with 1.8 Kilohms, a non-linear load.

The diode approximation assumes that the diode may be represented by a current source in parallel with an ideal diode. This implies that the diode is a perfect short circuit in its forward direction, and conducts a constant current in its reverse direction regardless of the reverse voltage. These considerations are sufficiently valid in this case, as when conducting in the forward direction the diode is in series with the series resistance-inductance stimulated current source, while when conducting in the reverse direction, junction diodes display constant current characteristics to a first approximation over a large portion of their range.

The circuit has three modes of operation:

(1) Sawtooth buildup - switch open, $e_c < v$

(2) Clipping - switch open, $e_c = v$

(3) Restoration - switch closed, $e_c = 0$

(1) Sawtooth Buildup

This period extends from zero time to time t_1, where times are relative to the start of the cycle. The series

resistance-inductance current source is charging up the capacitor. A small reverse current from the diode also contributes to the charging current.

Table 1-1 on page iv contains a list of symbols used in this and subsequent analysis and their definitions.

During the sawtooth buildup the equations of the circuit are

$$E = Ri_L + L\frac{di_L}{dt} + \frac{1}{C}\int i\,dt \tag{1}$$

$$\frac{i}{C} = \frac{de_c}{dt} \tag{2}$$

$$e_c\Big|_{t=0} = 0 \tag{3}$$

$$\frac{de_c}{dt}\Big|_{t=0} = \frac{i_o}{C} \tag{4}$$

The current i_o is the current flowing through the inductor at zero time, and since zero time is also the end of the previous cycle, i_o is the current at the end of previous cycle.

Putting $i_L = i - i_D$ and rearranging, equation (1) becomes

$$E + i_D R = iR + L\frac{di}{dt} + \frac{1}{C}\int i\,dt \tag{5}$$

where the derivative of i_D with respect to time is zero, as the back current of the diode is constant in time.

Substituting in equation (5) for i from equation (2)

$$\frac{d^2e_c}{dt^2} + \frac{R}{L}\frac{de_c}{dt} + \frac{1}{LC}e_c = \frac{E + Ri_D}{LC} \qquad (6)$$

which has the solution, after applying conditions (3) and (4),

$$e_c = e^{-\alpha t}\left(\frac{i_o - \alpha C(E + i_D R)}{C}\sin\beta t - (E + i_D R)\cos\beta t\right)$$

$$+ (E + i_D R) \qquad (7)$$

where

$$\alpha = \frac{R}{2L}$$

$$\beta^2 = \frac{1}{LC} - \frac{R^2}{4L^2}$$

By expanding the transcendental and exponential factors to terms involving the third power of the time, and neglecting higher powers of time, and defining

$$\beta_o^2 = \alpha^2 + \beta^2 = \frac{1}{LC}$$

the condenser voltage becomes

$$e_c \approx \frac{i_o t}{C} + \left(\frac{\beta_o^2(E + i_D R)}{2} + \frac{\alpha i_o}{C}\right)t^2$$

$$+ \left(\frac{\alpha\beta_o^2(E + i_D R)}{3} - \frac{(3\beta_o^2 - 4\beta^2)i_o}{6C}\right)t^3 + \cdots \qquad (8)$$

The ratio of the terms involving higher powers of time to the linear term gives a measure of the departure from linearity of the condenser voltage as a function of time. After substituting for α, β, and β_o the ratio of the square and cubic terms to the linear term become respectively

$$\left(\frac{E}{i_o} + R\left(\frac{i_D}{i_o} + \frac{1}{2}\right)\right)\frac{t}{L}$$

and $$\left(\frac{R(E + i_D R)}{L^2 i_o} + \frac{1}{LC} - \frac{R^2}{L^2}\right)\frac{t^2}{6} \quad .$$

By inspection of these expressions, it is seen that if L is large, for short periods the waveform of e_c is a linear ramp. It is difficult to obtain numerical answers from these expressions since, as will be subsequently shown, i_o is an involved function of the pulse width modulating voltage. However it is apparent that for small times they are much less than one, and for these times the departure from linearity is insignificant, and e_c may be approximated by the linear term

$$e_c = \frac{i_o t}{C} \quad . \tag{9}$$

The variation of i_L with time may be obtained by substituting equation (7) in equation (2):

$$i_L = i - i_D = i_o\, e^{-\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right) + \frac{\beta_o^2}{\beta}(E + i_D R)C\, e^{-\alpha t}\sin\beta t - i_D \tag{10}$$

(2) Clipping Period

At time t_1 when $e_c = v$ the circuit changes to the clipping mode. This time is given by equation (9) as

$$t_1 = \frac{Cv}{i_o} .$$

The current from the series resistance-inductance source will flow in a different path after t_1, but it must be continuous at t_1, so by equation (10),

$$i_L(t_1) = i_o e^{-\alpha t_1} (\cos\beta t_1 - \frac{\alpha}{\beta} \sin\beta t_1)$$

$$+ \frac{\beta_o^2}{\beta} (E + i_D R) C e^{-\alpha t_1} \sin\beta t_1 - i_D \qquad (11)$$

During this period the diode is conducting and i_D does not flow. The equations of the circuit are

$$e_c = v$$

$$E - v = Ri_L + L \frac{di_L}{dt} + R_T i_L \qquad (12)$$

Solving (12) with condition (11),

$$i_L = \frac{E-v}{R+R_T} \left(1 - e^{-\frac{R+R_T}{L}(t-t_1)}\right) + i_L(t_1) e^{-\frac{R+R}{L}(t-t_1)} \qquad (13)$$

(3) Restoration Period

During the restoration period the switch is closed, diode D_1 is reverse-biased, $e_c = 0$ and i_L is flowing through the switch. At the start of the restoration period at t_2 i_L is given by equation (13)

$$i_L(t_2) = \frac{E-v}{R_T+R}\left(1 - e^{-\frac{R_T+R}{L}(t_2-t_1)}\right) + i_L(t_1)e^{-\frac{R_T+R}{L}(t_2-t_1)} \qquad (14)$$

The equations of the circuit are

$$e_c = 0$$

$$E = i_L R + L\frac{di_L}{dt} \qquad (15)$$

This equation has the solution, subject to condition (14),

$$i_L = \frac{E}{R}\left(1 - e^{-\frac{R}{L}(t-t_2)}\right) + i_L(t_2)\, e^{-\frac{R}{L}(t-t_2)} \qquad (16)$$

At time ↑ when the cycle repeats itself,

$$i_L(\uparrow) + i_D = i_o \qquad (17)$$

From equation (16)

$$i_L(\uparrow) = \frac{E}{R}\left(1 - e^{-\frac{R}{L}(\uparrow -t_2)}\right) + i_L(t_2)e^{-\frac{R}{L}(\uparrow -t_2)}$$

and substituting in (17)

$$i_o = \frac{E}{R}\left(1 - e^{-\frac{R}{L}(\uparrow - t_2)}\right) + i_L(t_2)e^{-\frac{R}{L}(\uparrow - t_2)} + i_D \qquad (18)$$

It is apparent that i_o is a function of v. By equation (9) the slope of the sawtooth will be a function of v. This will introduce a non-linearity in the pulse width modulation. For the modulation to be linear the slope of the sawtooth must be a linear function of time independent of v, the clipping voltage.

There are two conditions when i_o will not be a function of v. These are

$$L \ll R$$

$$\text{and} \quad L \gg R.$$

In the first case examination of the previously developed equations in the limit that L approaches zero reveals that i_o approaches $\frac{E}{R} + i_D$ as would be expected from elementary inspection. The law governing the buildup of e_c would then be

$$e_c = (E + i\,R)\left(1 - e^{-t/RC}\right) = (E + i_D R)\left(\frac{t}{RC} - \frac{t^2}{2R^2C^2} + \frac{t^3}{6R^3C^3} - \ldots\right).$$

The error terms in this expression are very much larger than those of equation (8) so that this would apply only for very short times or for large values of RC. Also it is evident that

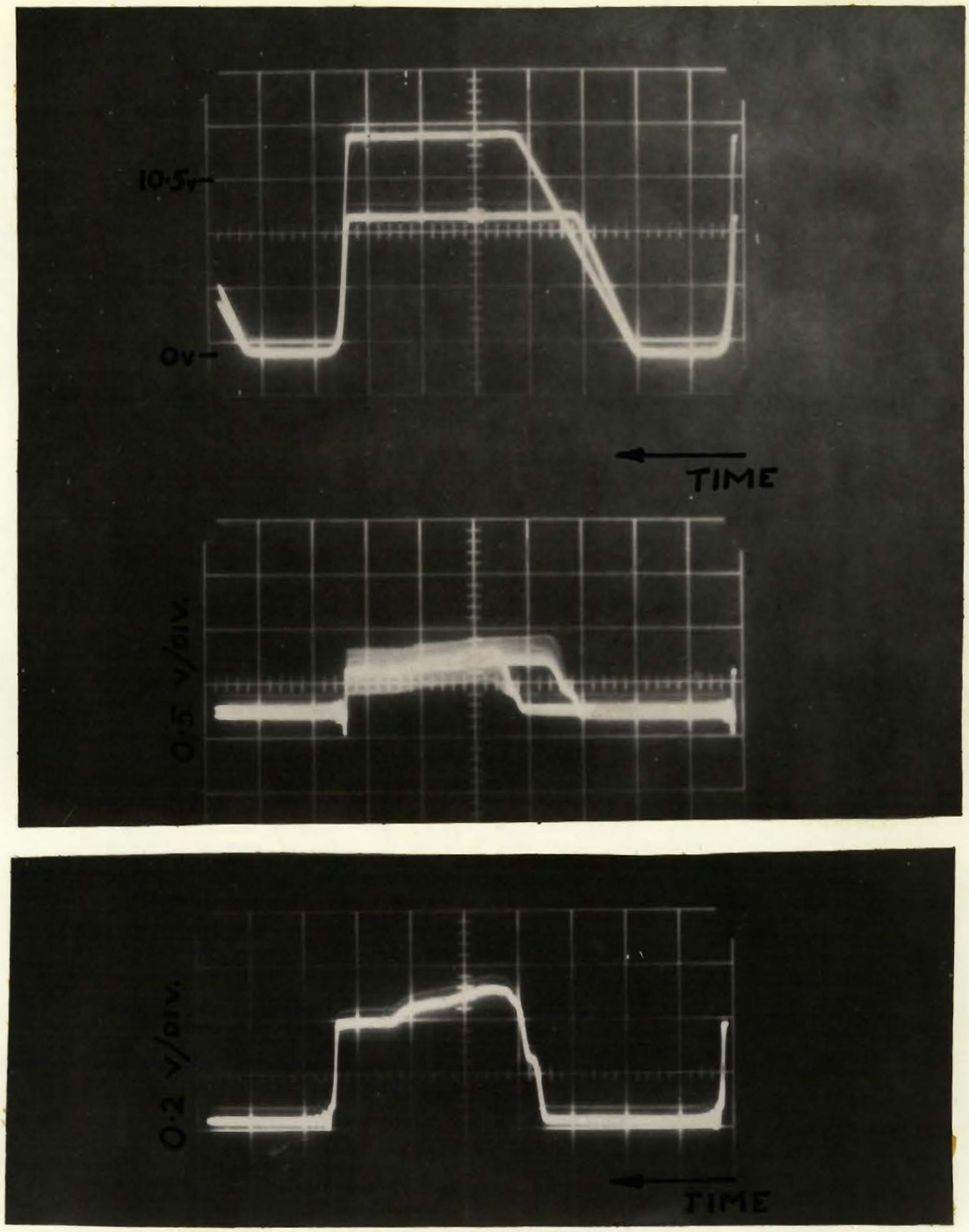
in this case if i_D is small compared to E/R, e_c will never be larger than E.

In the second case the time constant of all the periods has been made very long, so that there will be a very small variation in i_o over the cycle. Making L large reduces the error term of e_c to a small value, permitting e_c to exceed E by several times without introducing serious error in the linearity of the sawtooth [18].

Hence of the two possibilities the second is more suitable, for it is desired to obtain as linear a sawtooth of as great an amplitude as possible.

Of course a long restoration period would accomplish the same result, by permitting i_L to return to the same value at the start of each cycle regardless of the value of $i_L(t_2)$. It would not be practical to rely on this alone, since the restoration period would have to be prohibitively long, and in practice a combination of moderately high inductance and a moderately long restoration period seems to be the best solution.

The variation in slope of the sawtooth with v may be clearly seen in figure 2-4, taken from an oscillograph of e_c in the actual circuit used. Since it was desired to use as high a repetition rate as possible, the restoration time is somewhat shorter than it should be for the value of inductance used, which was quite small. Increasing the inductor to a few hundred henries would in all probability remove the error completely, and at the same time would not



Top: Fig. 2-4, Condenser Voltage
Middle: Fig. 2-6a, Transformer Output } 70 cps. Modulation

Bottom: Fig. 2-6b, Transformer Output, Zero Modulation

Horizontal : 10 μsec./div.

affect the slope of the sawtooth, since this is dependent only on the resistance and capacitance.

Figure 2-5 on page 36 shows the variation of e_c with t over a complete cycle for approximate values of the components used in the circuit.

Figure 2-6a shows the pulse appearing at the secondary of the transformer for a clipping voltage e_a of 7.5 volts peak to peak square wave, and figure 2-6b is the same voltage for zero modulation.

The transformer used was wound with two sections, 6 layers each, 100 turns per layer, #37 DCC wire on a C-core with two mil Hypersil laminations. The cross-sectional area of the core was 0.188 square inches and the mean length of the magnetic path was 7 inches. The windings were connected such that primary and secondary layers alternated in position relative to the core. The turns ratio was one to one.

The pulse width as a function of e_a, the pulse width modulating voltage, is nearly linear. It is assumed that the tangent to this function at the point e_a equals zero is the ideal behavior. Errors introduced by the various limitations mentioned in the analysis cause deviations from this tangent. The two curves of figure 2.6c may be drawn illustrating this process. The output and the error in the output are plotted against e_a. Included is the line tangent to the output at e_a equals zero from which the errors were calculated.

The readings from which these curves are calculated were obtained by using an amplifier-clipper to make the output

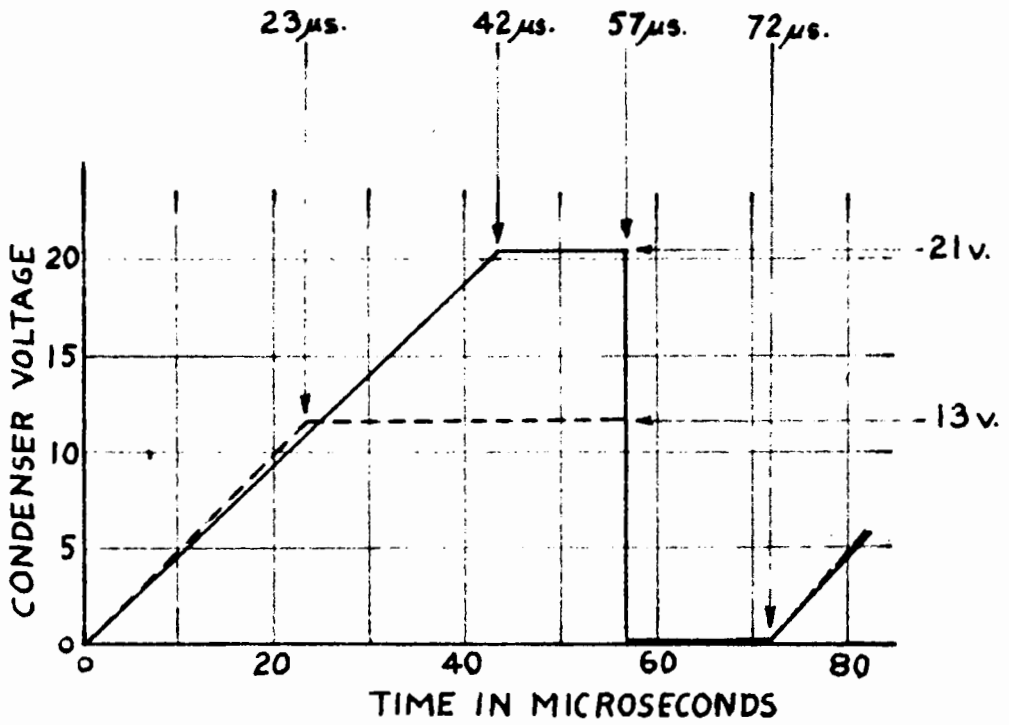


FIG 2-5

CONDENSER VOLTAGE FOR
21 AND 13 VOLT CLIPPING SUPPLIES

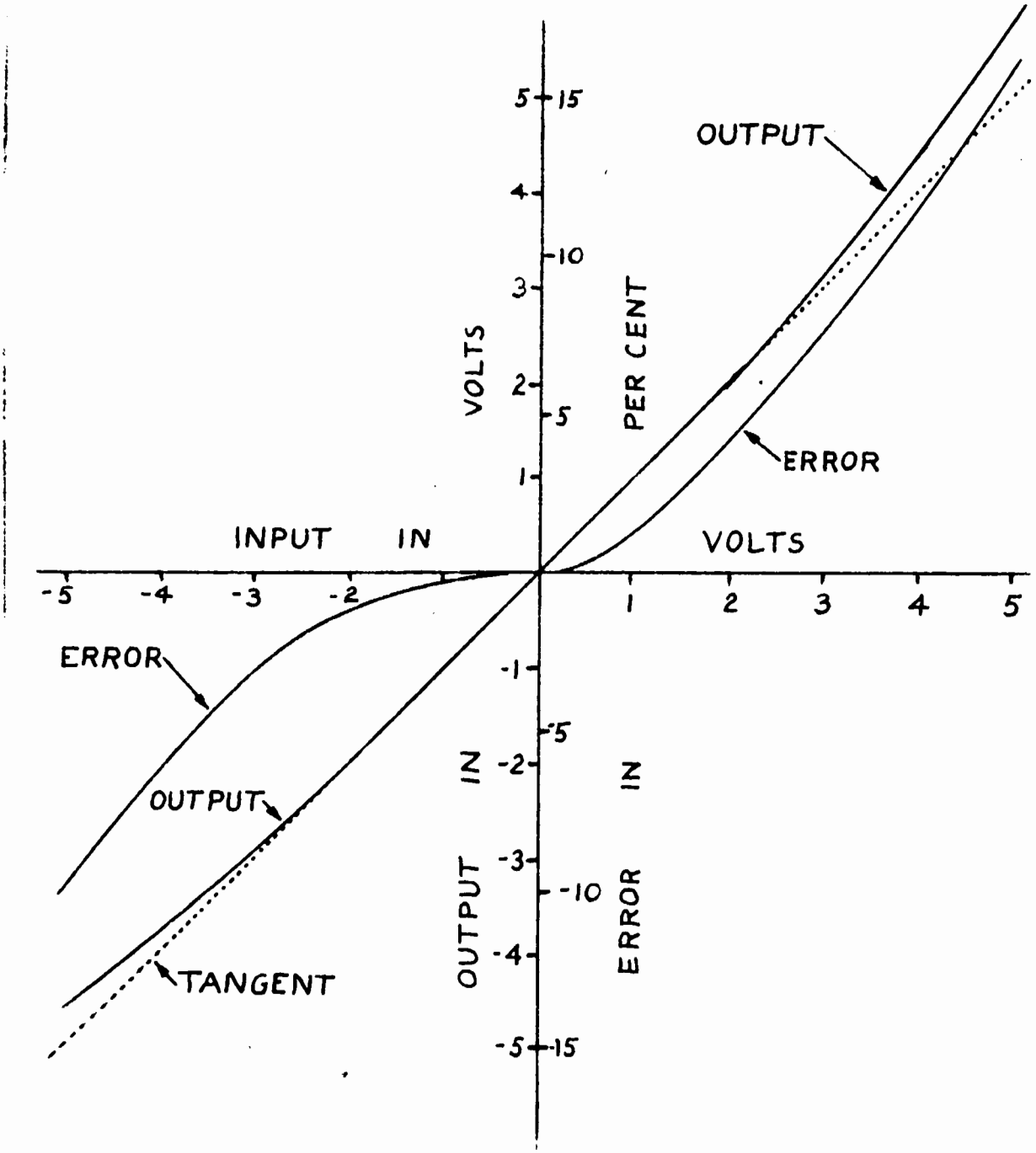


FIG 2-6c

PULSE WIDTH MODULATOR
PERFORMANCE

of the transformer of constant amplitude, and then measuring the average D.C. value of the output. This average value was set at zero when E_a was 10.5 volts. As stated previously, most of the error is due to the small value of inductance used in the simulated current source.

The Pulse Amplitude Modulator

The output of the pulse width modulator, appearing at the secondary of the transformer, drives a bidirectional switch, which serves as an amplitude modulator.

The operation of the bidirectional switch depends on the symmetrical properties of collector and emitter. If a transistor is made PNP, either P region may be used as the emitter, the other functioning as the collector. In most transistors the grounded base current gain in one direction is considerably larger than in the other. It is possible, however, to construct junction transistors in which the grounded base current gain is the same regardless of which terminal is functioning as collector and which as emitter [20]. Such transistors are referred to as symmetrical transistors. One of the two symmetrical terminals is designated emitter for purposes of reference regardless of its function, the other being the collector.

The circuit of the bidirectional switch is shown in figure 2-7. The output of the transformer is loaded with 1.8 kΩ and drives the base of a grounded emitter symmetrical transistor. The collector voltage is supplied through a voltage dropping network and a 470 ohm load resistor. The output

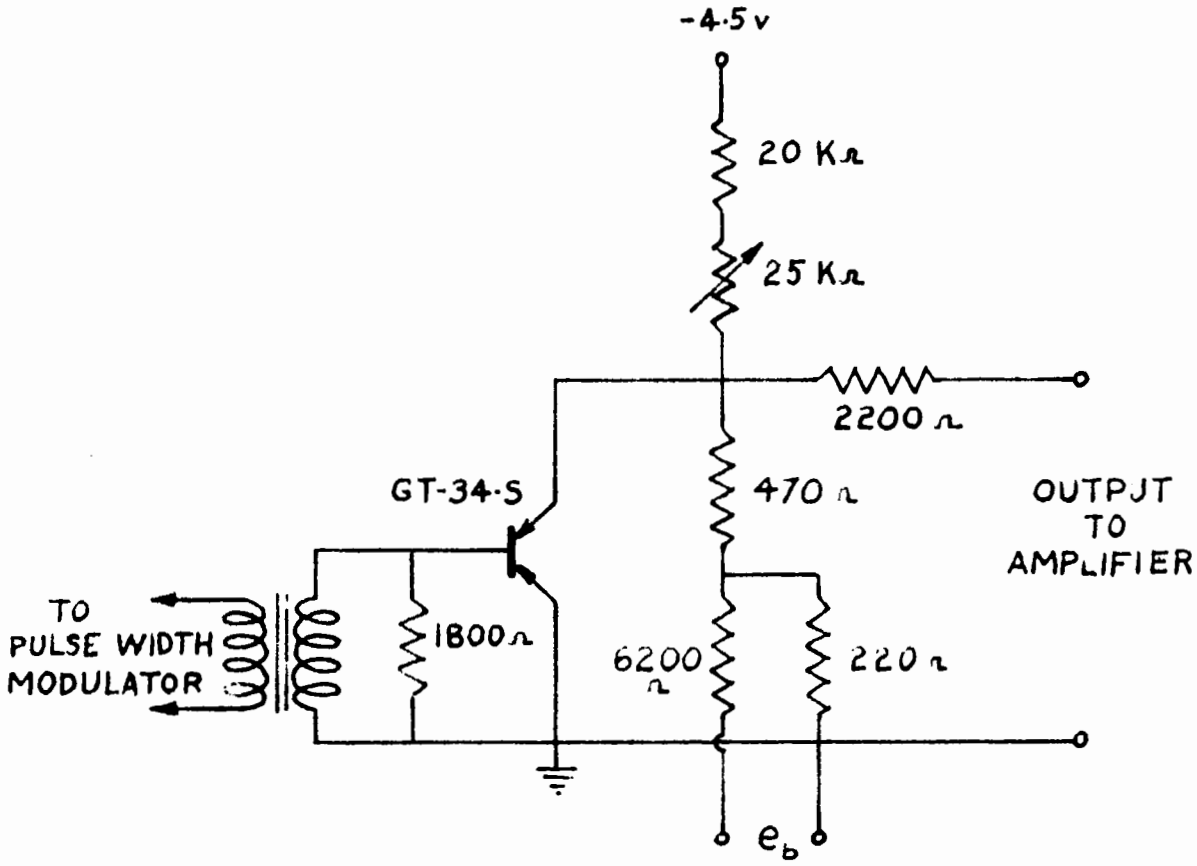


FIG 2-7

PULSE AMPLITUDE MODULATOR

to the next stage flows through a 2.2 kΩ resistance to that stage. Since there is a small voltage on the collector of the symmetrical transistor due to feed through of a bias voltage from the following stage, a small bias voltage of opposite polarity is supplied to the collector to neutralize this voltage, which would produce output for zero e_b, where e_b is the pulse amplitude modulating voltage.

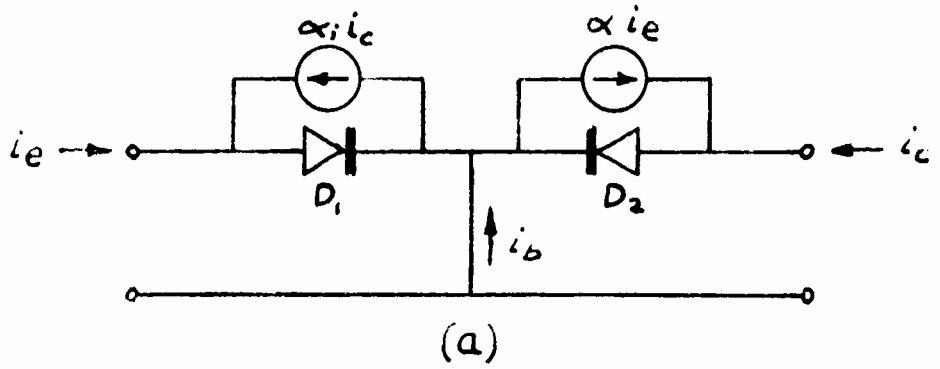
Ebers and Moll [19] have derived a large signal equivalent circuit for junction transistors (figure 2-8a). Inverting this circuit to grounded emitter operation, one obtains figure 2-8b. The bidirectional switch may be analysed with the aid of this equivalent circuit.

Kirchoff's current law applies to the transistor as a whole, that is $i_e + i_b + i_c = 0$. Figure 2-8b may then be redrawn as in figure 2-8c, putting $i_e = -(i_b + i_c)$, and adding a collector supply E_c, a load resistance R_L, a base supply E_b and a series resistance R_b.

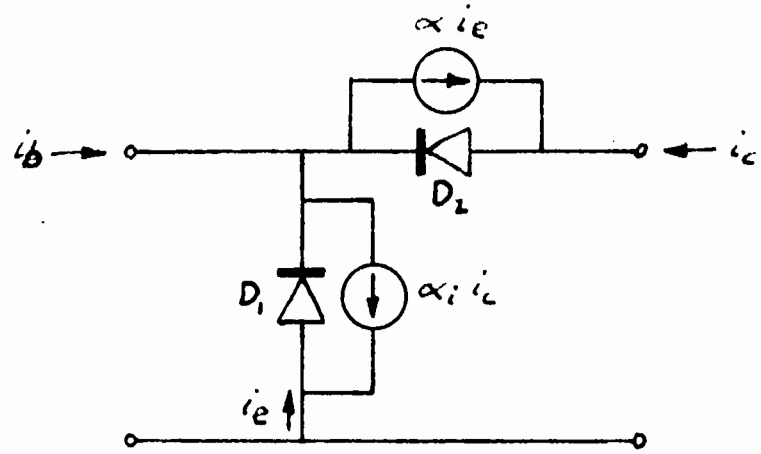
R_L is so chosen that it is large compared to the collector-emitter impedance of a saturated "on" transistor, and small compared to the "cut off" collector-emitter impedance, which may be of the order of megohms.

It is desired to obtain an expression for the output voltage e_o as a function of E_c and E_b. To do this it is necessary to examine the conditions for which the two junctions of the transistor are cut off and saturated on.

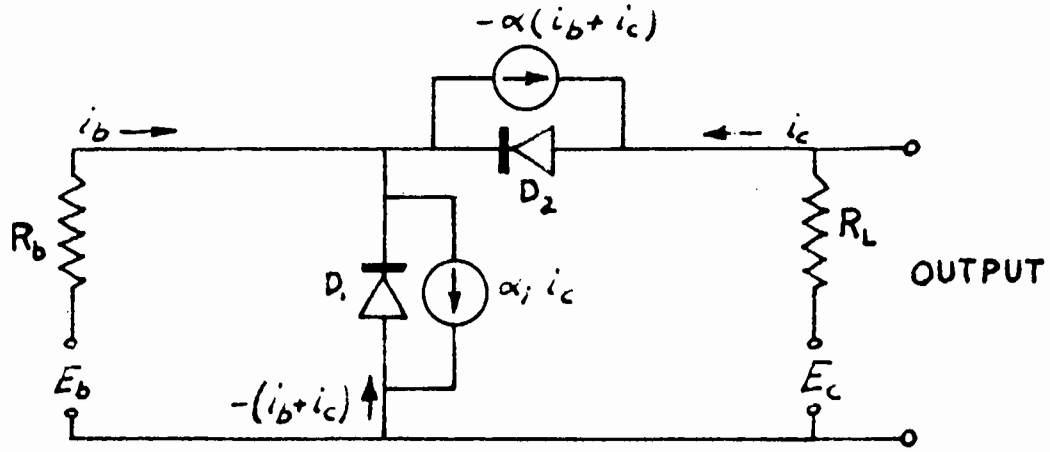
From the equivalent circuit of figure 2-8c it may be seen that diode D_2 will be conducting when



(a)



(b)



(c)

FIG 2-8

BIDIRECTIONAL SWITCH EQUIVALENT CIRCUIT

$$-\alpha(i_b + i_c) + i_c > 0$$

or $$i_c > \frac{\alpha}{1-\alpha} i_b \qquad (19)$$

and diode D_1 will be conducting when

$$-(i_b + i_c) + \alpha_i i_c > 0$$

or $$i_c < -\frac{1}{1-\alpha_i} i_b \qquad (20)$$

where α is the emitter-collector current gain and α_i is the collector-emitter current gain.

There are four states of operation of the circuit corresponding to i_b positive and negative, and i_c positive and negative. Table 2-1 lists the mode of operation of each diode for these four states.

Table 2-1

Diode Operation

i_c	Diode D_1		Diode D_2	
	i_b pos.	i_b neg.	i_b pos.	i_b neg.
pos.	cut off	cut off except when $i_c < -\frac{1}{1-\alpha_i} i_b$	cut off except when $i_c > \frac{\alpha}{1-\alpha} i_b$	conducting
neg.	cut off except when $i_c < -\frac{1}{1-\alpha_i} i_b$	conducting	cut off	cut off except when $i_c > \frac{\alpha}{1-\alpha} i_b$

Since α and α_i are both slightly less than one, the coefficients of i_b in inequalities 19 and 20 are quite large. Further, if the transistor is symmetrical, α and α_i are equal, and so these coefficients are very nearly equal in magnitude.

If the limits

$$|i_c| < \left|\frac{\alpha}{1-\alpha} i_b\right|$$

$$|i_c| < \left|\frac{1}{1-\alpha_i} i_b\right| \qquad (21)$$

are placed on i_c, table 2-1 is simplified as shown in table 2-2. The two limits of (21) are much the same since the coefficients of i_b are very nearly equal.

Table 2-2

Switch Operation

i_c	Diode D_1		Diode D_2	
	i_b pos.	i_b neg.	i_b pos.	i_b neg.
pos.	cut off	conducting	cut off	conducting
neg.	cut off	conducting	cut off	conducting

Hence if conditions (21) are satisfied, a change in sign of i_b switches both the diodes from one state to the other. That is, the current i_b controls the impedance presented to external circuitry by the collector of the transistor, regardless of the direction of i_c.

Figure 2-8d shows the result of this switching on the transfer characteristic E_{OUT} versus E_c. If the transistor is conducting E_c appears across R_L and the output is zero. If the transistor is cut off E_c appears across the transistor, and the output is E_c.

The switching of i_b from positive to negative independent of E_c may be assured by providing a voltage source base drive. Only a half volt or so is required to hold i_b positive or negative for the desired range of i_c. For i_b negative the voltage from base to emitter is held at this value by the low resistance of the base-emitter junction.

The linearity of this device is so good that, in the one built, errors are not noticeable when equipment of 2% precision is used to attempt to measure them. It is thought that, when the pulse amplitude modulator is used such that the limitations of figure 2-8d are satisfied, the accuracy possible is better than ½%.

Using the output of the pulse width modulator to drive this stage, the output consists of a train of pulses whose duty ratio is proportional to one input voltage, and whose envelope is a reproduction of a second input voltage.

This output waveform contains, apart from terms involving the repetition rate frequency of the pulses, two lower frequency terms. One is the desired product term. The other arises from the pulse amplitude modulation process and is proportional to the pulse amplitude modulating signal. Since the output of the pulse amplitude modulator is a series of pulses

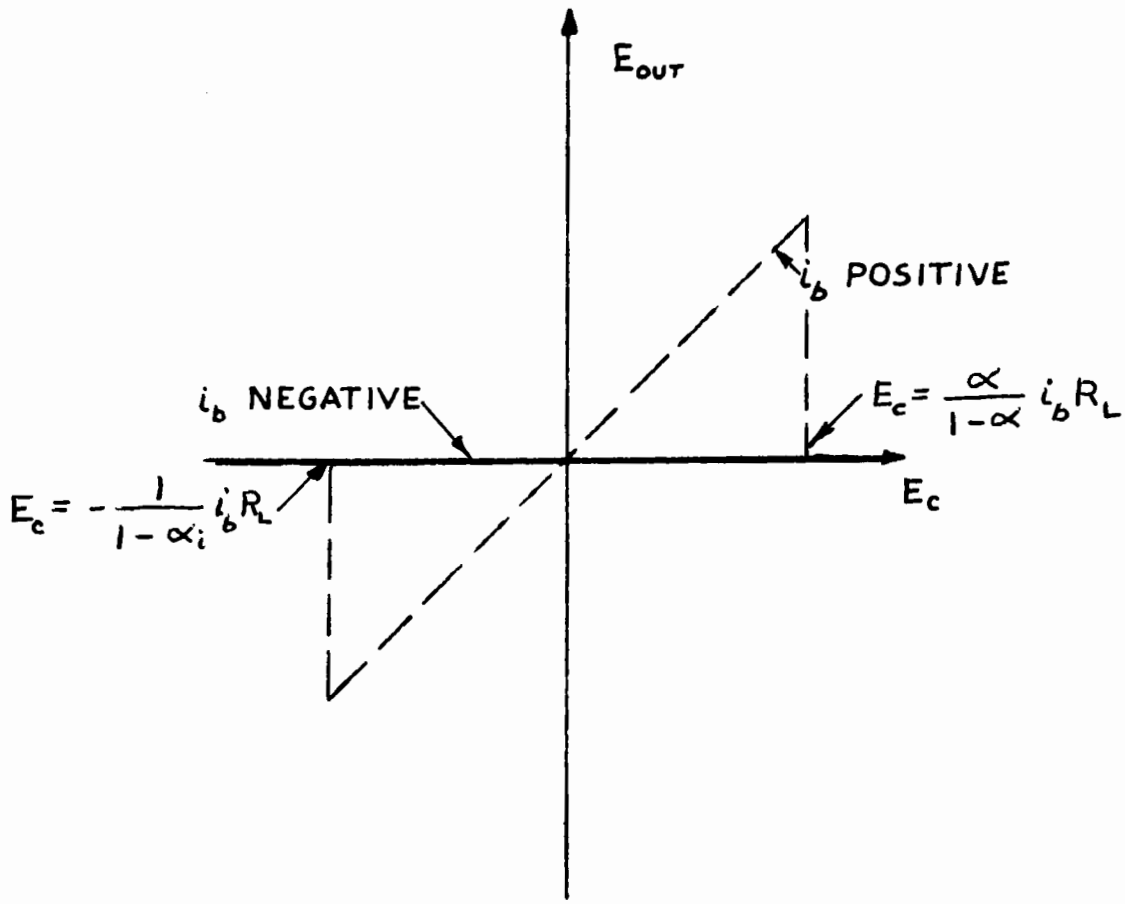


FIG 2-8d

SWITCH OPERATION

whose amplitude is equal to the modulating voltage, the output contains a modulating voltage component. This term must be subtracted from the output, leaving only one low frequency component, the desired product term.

Subtraction and Filtering

One of the modulating voltage or the modulated pulse output must be inverted to accomplish the subtraction, since the modulating voltage and the component of the modulated pulse output which must be subtracted are in phase.

Since some isolation must be provided between the point of subtraction and the output of the modulator some type of isolating amplifier must be driven by the pulse amplitude modulator output. It is convenient to incorporate the inversion process in this isolation amplifier, and so accomplish the isolation and inversion with the same circuitry.

The requirements on this amplifier are rather severe. It must be direct coupled, capable of passing a rectangular pulse train of repetition rate of 12 kilocycles/sec., and accepting an input amplitude about one volt peak to peak. It must have negligible direct current drift, and a stable gain, and it must provide zero output for zero signal input.

The circuit of such an amplifier is shown in figure 2-9. It is constructed of a cascade of three transistors, the first NPN, the second PNP, and the third NPN. The three types used have frequency cutoffs of the common base current gain in excess of one megacycle.

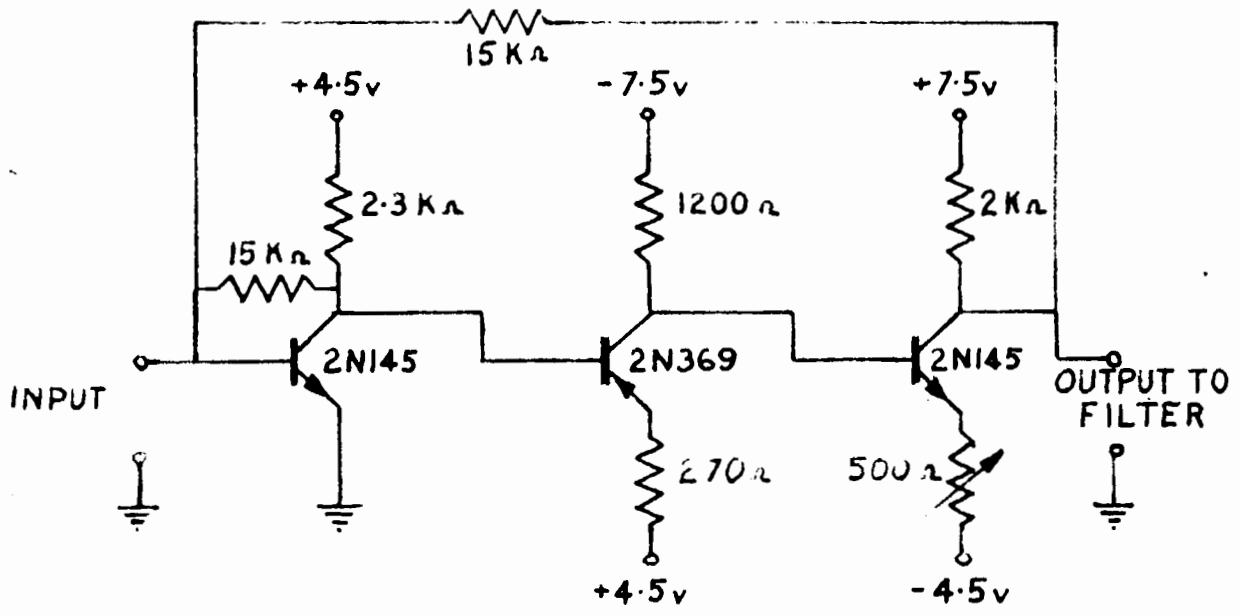
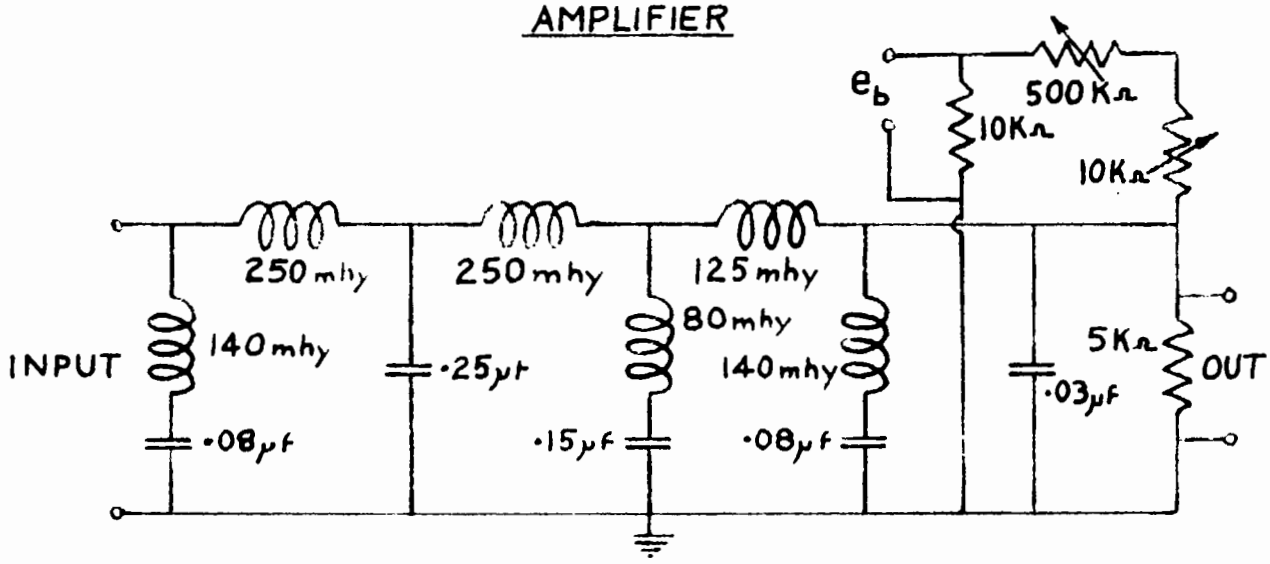


FIG. 2-9

AMPLIFIER



DESIGN VALUES

f_c = 1·2 KC/S

f_∞ = 1·43 KC/S

R = 1 KΩ

FIG 2-10

FILTER AND SUBTRACTION NETWORK

Because of the cascading of alternate types of transistors, it is possible to obtain zero output for zero input [20]. Stable gain at all frequencies is provided by internal negative voltage feedback around the first stage and around the entire amplifier, and by internal negative current feedback in the form of emitter resistors in the second and third stages. The emitter resistor of the output stage is variable to provide a direct current output level adjustment.

The voltage gain of this amplifier from the base of the first transistor to the output was measured as 63, and the maximum output before non-linearity becomes a problem is 2 volts RMS. To reduce the gain to about two a 2.2 kilohm resistor was added in series with the base of the first transistor. The drop in gain was necessary to enable the stage to handle the full input of about one volt peak to peak from the amplitude modulator.

The voltage gain of the amplifier as a function of frequency is constant for frequencies less than about 350 kilocycles, sufficient to pass the 12 kilocycle signal with no apparent distortion except for some ringing at the corners of the square wave.

The amplifier as designed requires four bias supplies. It is probable that with some drop in gain, which is not a problem here, it could be redesigned without elaborate revisions to require only two supplies. To do this it would be necessary to increase the load resistor of the first stage and the two emitter resistors, and supply these points with 7.5 volts rather than the 4.5 volts of this design.

Since the emitter of the first transistor is grounded, the base input lead is at a small potential above ground. A small bias voltage must be supplied to the amplitude modulator collector to cancel the effect of this voltage.

The output of the amplifier is supplied directly to a filter. The circuit of the filter with nominal values of components is shown in figure 2-10, on page 47.

This filter is a standard ladder filter composed of one constant-K T section and one M-derived T section in series, matched to source and load by M-derived half sections [21]. As shown in figure 2-11 the frequency of maximum attenuation is at about 42 kilocycles, and the attenuation at carrier frequency of 12 kcs is about 46 db. Cutoff frequency is about one kilocycle.

These figures are not particularly close to design values, since standard available components were used to construct the filter. Tolerances on these components were not good, and despite precautions in mounting, considerable mutual inductance is present between the various inductors used, making calculation of the theoretical performance to be expected rather difficult.

The output of the filter is loaded with five times its design load resistance, 5000 ohms. At this point the high frequency components have been reduced by about 40 db. from their value at the filter input. The two dominant terms remaining are the desired product and the term at pulse amplitude modulating frequency. This latter term is subtracted by supplying the pulse amplitude modulating voltage through a large

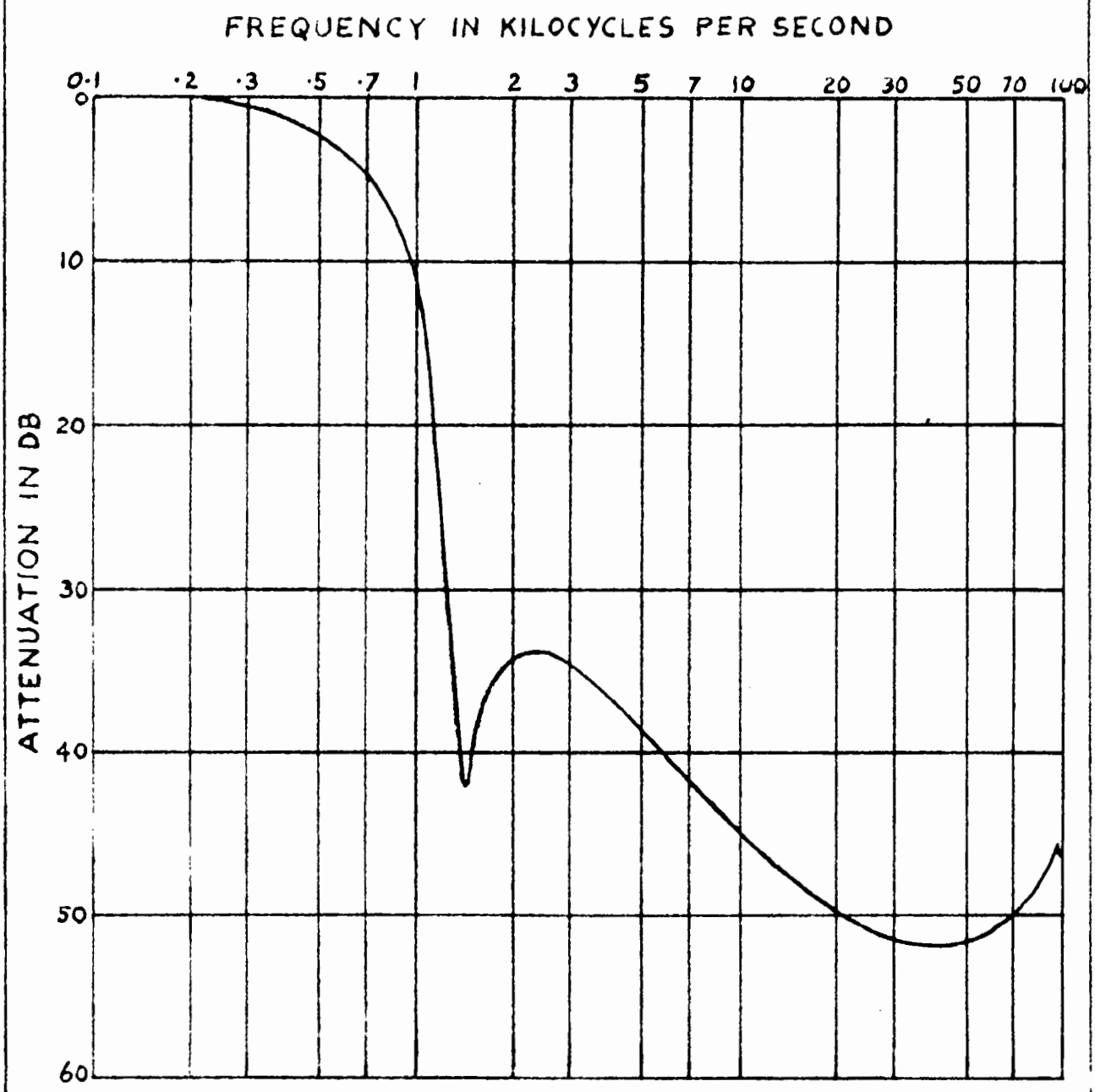


FIG. 2-11

FILTER CHARACTERISTIC

dropping resistor to the filter output.

The desired product term appears at the filter output, and when the device is properly adjusted, it is the only significant voltage term appearing there.

This term is quite small (about 20 millivolts) so that in practice it would have to be amplified considerably before it could be used in any computor. This operation will only affect the multiplier as far as amplifier defects will affect the accuracy of the device. An amplifier with a low frequency gain of 250 would bring the output level to about five volts, which is the order of magnitude of the input voltages, but would in all probability introduce some non-linearity and considerable direct current drift of the output.

Operation

A complete circuit diagram of the multiplier is shown in figure 2-12. Because of its simplicity, this circuit is quite easy to operate.

To adjust initially both modulating voltages are reduced to zero and their input terminals are shorted. Steps in the adjustment, after the batteries are connected and a warmup period of a half hour has passed, are

(1) The direct current output is zeroed by varying the emitter resistor in the third stage of the amplifier section.

(2) With an alternating current voltage supplied to the pulse width modulator, but the pulse amplitude modulation voltage still zero, the AC

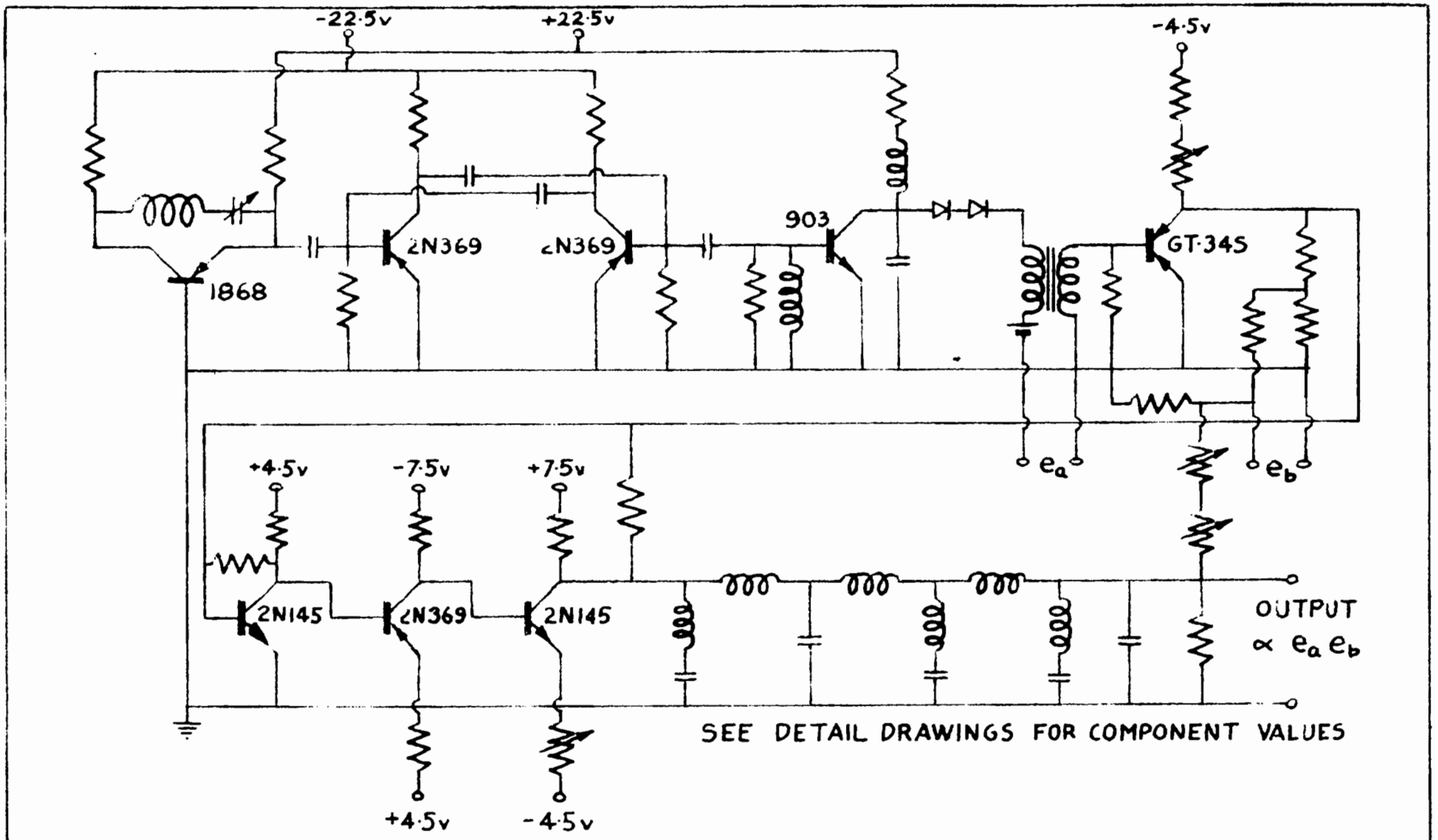


FIG 2-12

COMPLETE MULTIPLIER

output is zeroed by varying the small negative bias supply on the collector of the amplitude modulator.

(3) With the pulse width modulator terminals short circuited, and an AC pulse amplitude modulating voltage, the AC output is zeroed by varying the subtraction voltage supplied to the filter output.

It may be necessary to repeat these steps several times, for the adjustments are not independent.

The circuit is now ready for operation. A voltage e_a applied to the pulse width modulating circuit, and a voltage e_b applied to the pulse amplitude modulating circuit will result in an output voltage proportional to the product $e_a \cdot e_b$.

Results

The accuracy of this multiplier is not as good as anticipated due to a number of factors.

The non-linearity of the pulse width modulation is the important source of error. As mentioned in the section dealing with this component of the multiplier, it could be substantially improved by substitution of a larger inductor in the constant-current supply.

The filter cut-off frequency is somewhat high and the attenuation of the carrier components not sufficient to remove them completely, causing carrier terms to appear in the output. These terms cause some errors to arise in the output waveform. The best remedy for this defect would be to increase the carrier

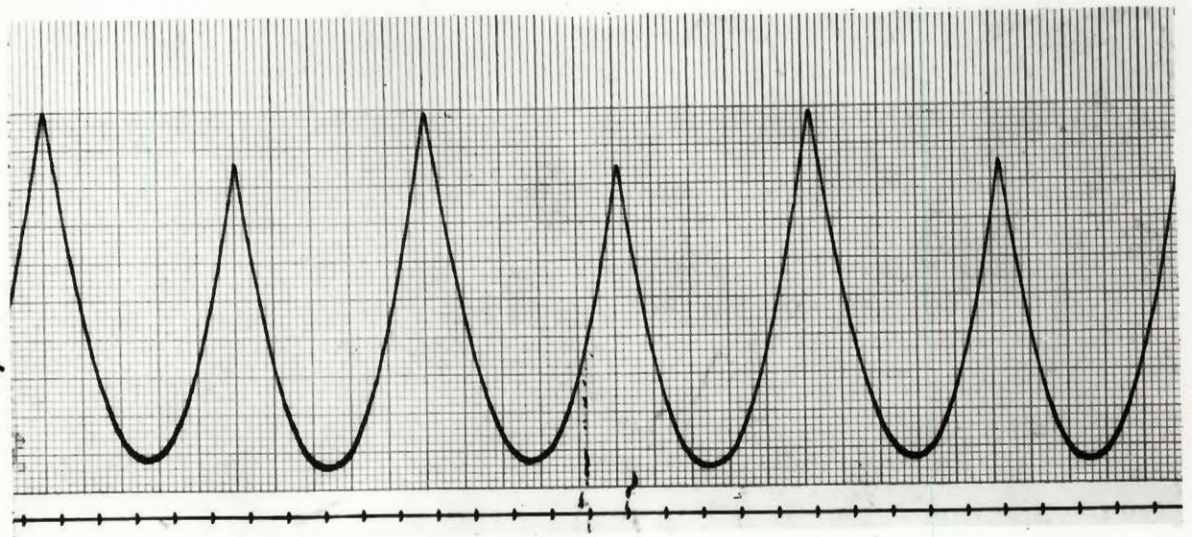
frequency to perhaps twice its present value, so that a filter with better characteristics which is not physically large in size can be made. This should result in some improvement of frequency response in the multiplier. The present design has constant characteristics for multiplicands of up to about 100 cycles per second. Above this frequency sidebands of the carrier extend into the passband, causing considerable error.

The pulse-amplitude modulation is linear, and the amplifier characteristics do not introduce additional errors in the output.

For lower frequencies (below 100 cps) the accuracy of the multiplier is the same as the accuracy of the pulse width modulation process. At higher frequencies the accuracy deteriorates due to the filter characteristic. So that for frequencies less than 100 cps, and if the pulse amplitude modulating voltage is within its linear limits, the error of the multiplier (defined as the percentage departure from the true product) is within 1% of the true product for the pulse width modulating voltage less than 1/10 full scale, 6% for less than 1/2 full scale, and 16% for full scale, for all values of the pulse amplitude modulating voltage.

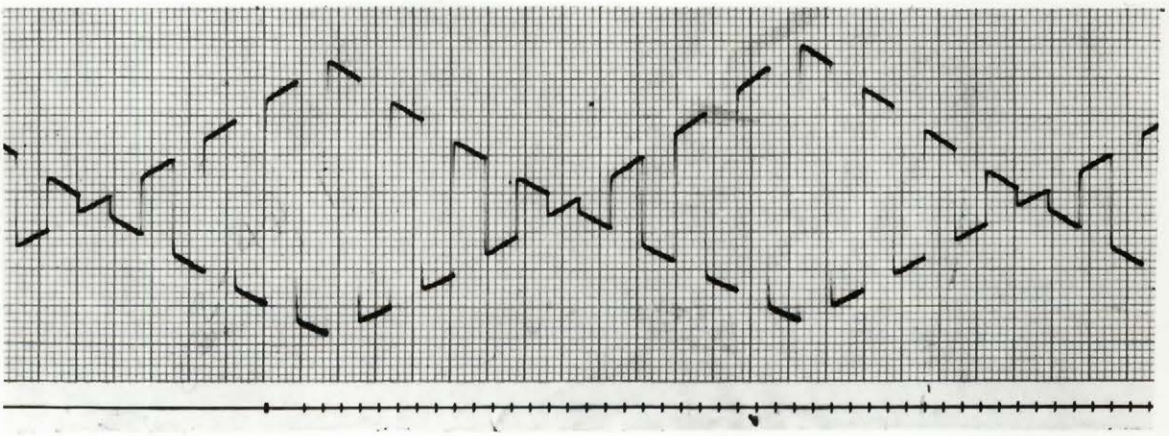
Various output waveshapes are shown in figure 2-13. The effect of the pulse width modulator non-linearity shows clearly on the triangular wave of figure 2-13a, where the square wave was the pulse amplitude multiplicand.

The square of a triangular wave is shown in figure 2-13b. The peaks alternate in amplitude because of a small



0·1 CPS. TRIANGULAR WAVE SQUARED

(b)



VERTICAL SCALES 10 MILLIVOLTS/CM.

0·3 CPS. SQUARE WAVE (PAM) TIMES

0·02 CPS. TRIANGULAR WAVE (PWM)

(a)

FIG 2-13

MULTIPLIER OUTPUT

direct current level superposed on the triangular wave. The direct current level is inherent in the signal generator used.

Conclusions

Various methods of multiplication suitable for use with transistors in repetitive analog computors are reviewed. Of the four methods, the time division method is adjudged the most promising. A multiplier is designed and constructed using this principle.

The multiplier was found to be able to accept multiplicands up to 100 cycles per second without appreciably affecting the accuracy.

The pulse amplitude modulation process was found to be very accurate (within 1/2%).

The error in the multiplier below 100 cps is ascribed wholly to the pulse width modulating process, and methods for improving this operation are stated in detail.

The overall accuracy of the multiplier is found to be better than 16% for the pulse width modulating voltage full scale, better than 6% for 1/2 full scale and better than 1% for 1/10 full scale, for all values of the pulse amplitude modulating voltage.

There seems to be no difficulty in achieving four quadrant operation with this type of multiplier, and no inherent errors are introduced when either input voltage crosses zero. Hence the time division technique has some considerable advantages over other means of multiplication while suffering from the disadvantages of complexity and low output voltage.

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