Double-Sampled Digital-Feedforward Second-Order Delta-Sigma Modulator

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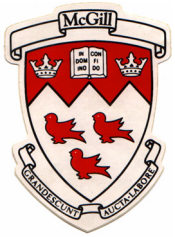

A thesis submitted to McGill University in partial fulfilment of the requirements of the degree of Master of Engineering

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ABSTRACT

A 12-bit 2.8-MHz $\Delta\Sigma$ modulator intended for ADSL applications is presented in this thesis. The design process evolved over two stages, namely, a system-level design stage followed by a circuit-level design stage. During the first phase of the design, the system-level parameters are selected and analog-circuit specifications are derived. The circuit-level stage involved the design of analog circuitry such as operational amplifiers capable of meeting the system-level specifications. The circuit design was carried out in 1-V 65-nm CMOS technology. Double-sampling was employed to make the switched-capacitor circuits more power efficient. Input-signal feedforward was used to lower the signal swing at the output of the opamps. Digital input feedforward is used and presented as an alternative to analog input feedforward.

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RÉSUMÉ

Un modulateur ΔΣ 12-bit 2.8-MHz conçu pour des applications ADSL est présenté dans ce mémoire. Le processus de conception est décrit en deux phases: la conception au niveau du système suivie de la réalisation au niveau du circuit. Lors de la première phase, les paramètres du système sont choisis et les spécifications analogiques du circuit sont dérivées. La phase de l'implémentation du circuit impliquait la conception de circuits analogiques tels que amplificateurs opérationnels respectant les spécifications du système. La conception du circuit a été réalisée sur la technologie 1-V 65-nm CMOS. Le double-échantillonnage a été employé afin que les circuits de condensateurs-commutés soient plus économiques en terme de puissance. La technique d'action directe (feedforward) a été utilisée sur le signal d'entrée afin de réduire l'amplitude à la sortie des amplificateurs. La technique d'action directe digitale sur le signal d'entrée est utilisée et présentée comme une alternative à son homologue analogique.

Acknowledgements

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Chapter 1

Introduction

1.1 Overview

The design of analog-to-digital converters (ADCs) has become more challenging due to several factors. These mainly include the demanding requirements imposed by modern broadband digital communication applications. Examples include high-speed wired communication services such as ADSL [Conroy, ISSCC99]. High-speed and high-resolution ADCs are critical to meet those communication standards. Low-power operation is also critical for portable applications. In addition to that, these ADCs must be built in standard digital CMOS processes for higher system integration and lower fabrication costs [Hamoui 04]. Two special design techniques are used in this work which are:

1) double sampling.

2) input digital feedforward.

1.2 Thesis Outline

This thesis presents the design of discrete-time $\Delta\Sigma$ modulators with digital feedforward (DFF) using double-sampled switched-capacitor (SC) circuits with 12-bit resolution and over 2-MHz bandwidth in 1-V 65-nm CMOS technology. The thesis is broken down as follows:

Chapter 2: Double-Sampling Switched-Capacitor Integrators

In this chapter, the motivation for using double-sampled SC integrators is discussed. Their performance gain is assessed. A model for a SIMULINK double-sampled SC integrator is derived. In addition to that, the noise-folding due to capacitance mismatches is discussed and some solutions are reviewed. Finally, in the simulation section, the performance of double sampling $\Delta\Sigma$ modulators is studied with respect to modulator order.

Chapter 3: Digital-Feedforward Delta-Sigma Modulators

In this chapter, the motivation for using DFF $\Delta\Sigma$ modulators is discussed. The DFF architecture utilized in this thesis is explained in detail. Finally, in the simulation section, the performance of the DFF $\Delta\Sigma$ modulator utilized in this thesis is studied and compared to analog input feedforward (AFF) architectures, and to DFF architectures.

Chapter 4: Architectural-Level Design

In this chapter, a 2^{nd}-order DFF $\Delta\Sigma$ modulator is designed and its SC circuit specifications are derived. Details of the integrator models used are explained. Finally, a noise budget scheme for the $\Delta\Sigma$ modulator is presented along with all the circuit-level specifications needed.

Chapter 5: Double-Sampling Switched-Capacitor Circuit Implementation

Chapter 5 presents the SC circuit-level design of the simulated ΔΣ modulator in a 1-V 65-nm digital CMOS process with no options for low threshold voltages. Detailed description is presented for the design of the various circuit blocks in this SC ΔΣ modulator, including its bootstrapped sampling switches, and the folded-cascode opamps. In the end, the ΔΣ loopfilter is simulated for linearity and the output spectrum is plotted for various input frequencies.

Chapter 6: SUMMARY

Chapter 6 summarizes the thesis and highlights its research contribution.

Chapter 2

Double-Sampling Switched-Capacitor Integrators

Double sampling is a low-power design technique which effectively doubles the sampling frequency of switched-capacitor (SC) integrators without increasing their clock frequency. The idea here is that, during the sampling phase of an SC integrator, the opamp is idle. Therefore, to optimize circuit usage at seemingly* the same power consumption, the opamp is used in the sampling phase to integrate a charge stored previously on a different set of capacitors. A single-

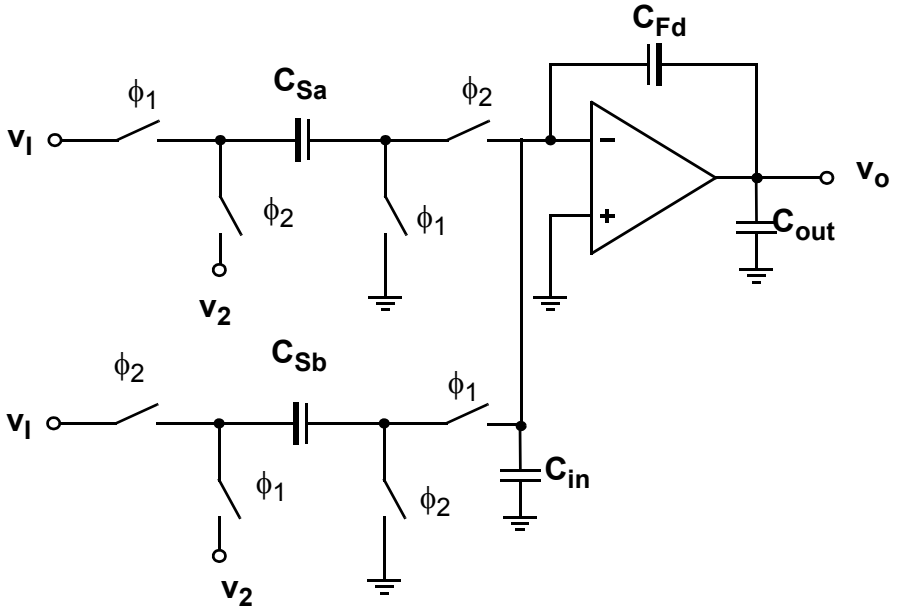

Figure 2.1 Double-sampling SC integrator. Here, capacitors C_{in} and C_{out} represent the total capacitances, including any parasitic, at the input and output nodes of the opamp, respectively.

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* Section 2.2 gives more insight into the performance advantages of double-sampling SC integrators.

ended double-sampling integrator is shown in Figure 2.1. During ϕ_1, capacitor C_{Sa} samples the input signal, while the opamp is integrating the charge stored in the previous phase ϕ_2 on capacitor C_{Sb}. During ϕ_2, the opposite is performed. Thus, the output is being updated during both clock phases, and, therefore, an effective doubling of the sampling frequency is achieved.

2.1 Nonideal Performance of Double-Sampled SC ΔΣ Modulators

The performance of double-sampled SC ΔΣ modulators is limited severely by:

1) sampling-capacitor mismatches.

2) systematic clock jitter.

2.1.1 Sampling-Capacitor Mismatch

The output of the double-sampled SC integrator in Figure 2.1 can be derived as follows.

Time Domain Analysis

- During ϕ_1 ($t = n \cdot \frac{T_S}{2}$), where T_S is the sampling period:

  The charges stored on the capacitors are:

$$Q_{Csa}(n) = v_1(n) \cdot C_{Sa} \tag{2.1}$$

$$Q_{Csb}(n) = v_2(n) \cdot C_{Sb} \tag{2.2}$$

$$Q_{Cf}(n) = v_o(n) \cdot C_{Fd} \tag{2.3}$$

- During ϕ_2 ($t = (n+1) \cdot \frac{T_S}{2}$):

  The charges stored on the capacitors are:

$$Q_{Csa}(n+1) = v_2(n+1) \cdot C_{Sa} \tag{2.4}$$

$$Q_{\mathrm{Csb}}(n+1) = v_1(n+1) \cdot C_{\mathrm{Sb}} \tag{2.5}$$

$$Q_{\mathrm{Cf}}(n+1) = v_o(n+1) \cdot C_{Fd} \tag{2.6}$$

The charge transfer between capacitors results in (2.7)

$$[Q_{\mathrm{Csa}}(n+1) - Q_{\mathrm{Csa}}(n)] + [Q_{\mathrm{Cf}}(n+1) - Q_{\mathrm{Cf}}(n)] = 0$$

$$\Rightarrow (v_1(n) - v_2(n+1)) \cdot C\mathrm{s}_{\mathrm{a}} = (v_o(n+1) - v_o(n)) \cdot C_{Fd} \tag{2.8}$$

- During ϕ_1 $(t = (n+2) \cdot \frac{T_S}{2})$:

  The charges stored on the capacitors are:

$$Q_{\mathrm{Csb}}(n+2) = v_2(n+2) \cdot C_{\mathrm{Sb}} \tag{2.9}$$

$$Q_{\mathrm{Csa}}(n+2) = v_1(n+2) \cdot C_{\mathrm{Sa}} \tag{2.10}$$

$$Q_{\mathrm{Cf}}(n+2) = v_o(n+2) \cdot C_{\mathrm{F}d} \tag{2.11}$$

The charge transfer between capacitors results in

$$[Q_{\mathrm{Csb}}(n+2) - Q_{\mathrm{Csb}}(n+1)] + [Q_{\mathrm{Cf}}(n+2) - Q_{\mathrm{Cf}}(n+1)] = 0 \tag{2.12}$$

$$\Rightarrow (v_1(n+1) - v_2(n+2)) \cdot C\mathrm{s}_{\mathrm{b}} = (v_o(n+2) - v_o(n+1)) \cdot C_{Fd} \tag{2.13}$$

To account for the mismatch between the sampling capacitors C_{Sa} and C_{Sb}, define

$$C_{\mathrm{Sb}} \equiv C_S - \frac{\Delta C}{2} \tag{2.14}$$

$$C_{\mathrm{Sa}} \equiv C_S + \frac{\Delta C}{2} \tag{2.15}$$

where ΔC is the mismatch between the two sampling capacitors C_{Sa} and C_{Sb}, and C_S is the nominal sampling capacitance. Substituting equations (2.14) and (2.15) into (2.8) and (2.13) results in the following expressions:

$$v_o(n+1)C_{Fd} \tag{2.16}$$
$$= (v_1(n) - v_2(n+1))C_S + (-1)^2(v_1(n) - v_2(n+1))\frac{\Delta C}{2} + v_o(n)C_{Fd}$$

$$v_o(n+2)\cdot C_{Fd} \tag{2.17}$$
$$= (v_1(n+1)-v_2(n+2))\cdot C_S + (-1)^1\cdot(v_1(n+1)-v_2(n+2))\cdot\frac{\Delta C}{2} + v_o(n+1)\cdot C_{Fd}$$

Define the input error voltage as:

$$v_e(n) \equiv v_1(n-1) - v_2(n) \tag{2.18}$$

The double-sampled SC integrator output can then be expressed, using (2.16)-(2.18), as:

$$v_o(n) = \begin{cases} v_e(n)\left(\frac{C_S}{C_{Fd}}\right) - v_e(n)\left(\frac{\Delta C}{2C_{Fd}}\right) + v_o(n-1), & \text{for n = odd} \\ v_e(n)\left(\frac{C_S}{C_{Fd}}\right) + v_e(n)\left(\frac{\Delta C}{2C_{Fd}}\right) + v_o(n-1), & \text{for n = even} \end{cases} \tag{2.19}$$

The expressions in (2.19) can be combined as:

$$v_o(n) = \left(\frac{C_S}{C_{Fd}}\right)v_e(n) + (-1)^n\left(\frac{\Delta C}{2C_{Fd}}\right)v_e(n) + v_o(n-1) \tag{2.20}$$

Define the nominal integrator gain as:

$$K_I = \frac{C_S}{C_{Fd}} \tag{2.21}$$

Then, using (2.14)(2.15)(2.20) and (2.21), the integrator output can be simplified as:

$$v_o(n) = K_I v_e(n) + (-1)^n K_I\left(\frac{\Delta C}{2C_S}\right)v_e(n) + v_o(n-1) \tag{2.22}$$

Z-Domain Analysis

When using the double-sampled SC integrator in Figure 2.1 as the first integrator at the input of an SC $\Delta\Sigma$ modulator, the error signal $v_e(n)$ in equation (2.18) represents the difference between the delayed input sample and the feedback-DAC signal. Figure 2.2 depicts the resulting spectrum of $V_e(z)$ and $V_e(-z)$.

In equation (2.22), signal $v_e(n)$ is multiplied by $(-1)^n$, which is equivalent to an amplitude modulation with a cosine sampled at a frequency of $f_s/2$. In the *Z*-domain, this corresponds to replacing z with $-z$ and, hence, to a translation by $f_s/2$ towards dc [Rombouts, JSSC03]. The equivalent *Z*-domain expression of equation (2.22) is therefore:

$$V_o(z) = \left(\frac{K_I}{1-z^{-1}}\right)\left(V_e(z) + V_e(-z)\left(\frac{\Delta C}{2C_S}\right)\right) \tag{2.23}$$

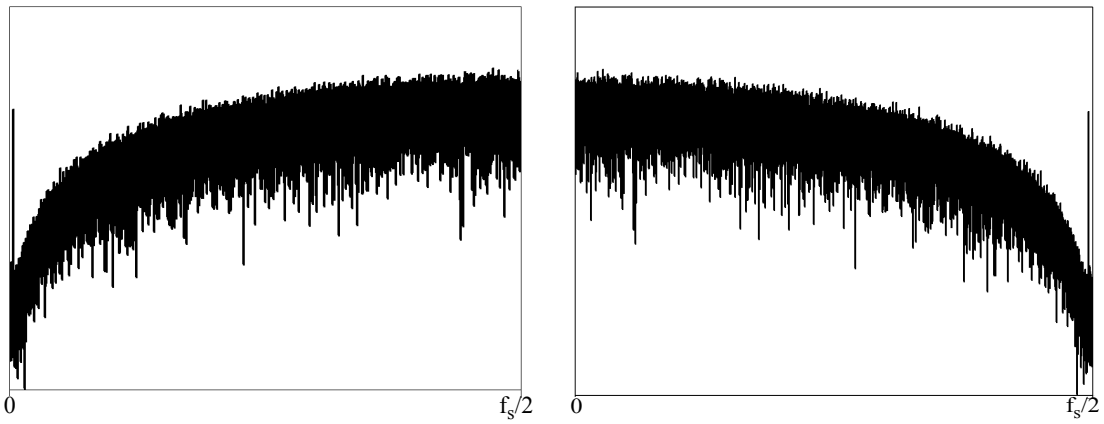


Figure 2.2 Spectrum of a) $V_e(z)$ and b) $V_e(-z)$ when the double-sampled SC integrator in Figure 2.1 is used as the first integrator at the input of an SC $\Delta\Sigma$ modulator.

Accordingly, the integrator output is corrupted by the term $V_e(-z)\left(\frac{\Delta C}{2C_S}\right)$, due to sampling-capacitor mismatches. This phenomenon, referred to as *quantization noise folding* [Rombouts, TCAS04], severely limits the resolution of $\Delta\Sigma$ modulator with double-sampled SC integrators.

2.1.2 Systematic Clock Jitter

Systematic clock jitter arises from the fact that the periods of clock phases ϕ_1 and ϕ_2 may vary due to circuit nonidealities. Let T_{S1} and T_{S2} denote the periods of clock phases ϕ_1 and ϕ_2 with:

$$T_{S1} = T_S\left(1 + \frac{\Delta T}{2}\right) \tag{2.24}$$

$$T_{S2} = T_S\left(1 - \frac{\Delta T}{2}\right) \tag{2.25}$$

where ΔT is the mismatch in the periods of the clock phases.

For an input signal $V_i(t) = A\cos(\omega \cdot t + \theta)$, the resulting input samples are [Burmas, JSSC96]

$$V_i(nT_S) = A\cos(\omega \cdot nT_S + \theta)\cos\left(\omega \cdot \frac{\Delta T}{2}\right) - A\sin(\omega \cdot nT_S + \theta)(-1)^n \sin\left(\omega \cdot \frac{\Delta T}{2}\right) \tag{2.26}$$

The first term in equation (2.26) is the nominal input sample scaled by $\cos\left(\omega \cdot \frac{\Delta T}{2}\right)$. Since $\frac{\Delta T}{2}$ is small, the cosine scaling factor is close to unity. However, the second term in equation (2.26) is a shifted version of the input modulated by a cosine sampled at $f_s/2$. In oversampling converters, this means that the input will be modulated to high frequencies near $f_s/2$ and, hence, it will not corrupt the bandwidth of interest, as it will get highly attenuated by the proceeding low-pass digital filter.

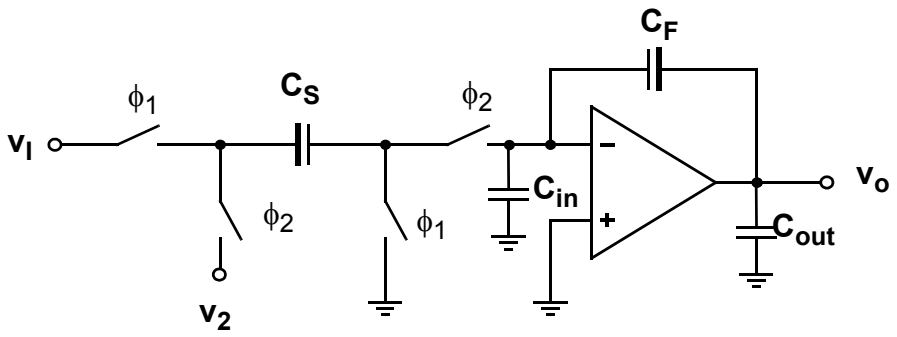


Figure 2.3 Single-sampling SC integrator. Here, capacitors C_{in} and C_{out} represent the total capacitances, including any parasitic, at the input and output nodes of the opamp, respectively.

2.2 Performance Comparison

Consider the double-sampling SC integrator in Figure 2.1. To achieve the same $\frac{kT}{C}$ noise and path gain as the single-sampling SC integrator in Figure 2.3, it must be designed with [Hamoui 04] :

$$C_{\mathrm{Sa}} = C_{\mathrm{Sb}} = 2C_S \tag{2.27}$$

$$C_{\mathrm{Fd}} = 2C_F \tag{2.28}$$

The impact of this design on the integrator characteristics is summarized in Table 2.1.

Term	Double-Sampling	Single Sampling	Comments
Sampling Capacitor	$C_{Sa} = C_{Sb} = 2C_S$	C_S	C_{Sa} and C_{Sb} have to be double the size of C_S for the same kT/C noise.
Total kT/C noise	$\frac{2 \cdot 2kT}{OSR \bullet (2C_S)}$	$\frac{2kT}{OSR \bullet C_S}$	
Feedback Capacitor	$2C_F$	C_F	C_{Fd} has to be double the size of C_F for the same integrator gain K_I.
Feedback Factor β	β_d	β_s	$\beta_s = \frac{C_F}{C_F + C_{in} + C_S}$ and $\beta_d = \frac{2C_F}{2C_F + C_{in} + 2C_S}$
Load Capacitance C_L	C_{Ld}	C_{Ls}	$C_{Ls} = C_{out} + \frac{(C_S + C_{in})C_F}{C_F + C_{in} + C_S}$ $C_{Ld} = C_{out} + \frac{(2C_S + C_{in})(2C_F)}{2C_F + C_{in} + 2C_S}$
Opamp Bandwidth ω_{3dB}	$\omega_{3dB,d}$	$\omega_{3dB,s}$	$\omega_{3dB,s} = \beta_s \cdot \frac{G_M}{C_{Ls}}$ $\omega_{3dB,d} = \beta_d \cdot \frac{G_M}{C_{Ld}}$

Table 2.1 Comparison between single and double-sampled SC integrators with the same kT/C noise and integrator gain.

For the same power consumption (same short circuit transconductance G_M), the improvement in terms of speed achieved through double sampling can be expressed in terms of the ratio of opamp bandwidth [Burmas, JSSC96] as:

$$Speed\ gain = \frac{2 \cdot \omega_{3dB,\,d}}{\omega_{3dB,\,s}} \tag{2.29}$$

Substituting for $\omega_{3dB,\,d}$ and $\omega_{3dB,\,s}$ (Table 2.1) in equation (2.29) and simplifying the expression results in the following equation:

$$Speed\ gain = 4 \bullet \left(\frac{C_F C_{in} + C_S C_F + C_{out} C_S + C_{in} C_{out} + C_F C_{out}}{2C_F C_{in} + 4C_S C_F + 2C_{out} C_S + C_{in} C_{out} + 2C_F C_{out}} \right) \tag{2.30}$$

2.3 SIMULINK Model

Consider the fully-differential double-sampling SC integrator in Figure 2.4. Let

$$v_{1P} = \frac{v_I}{2} \tag{2.31}$$

$$v_{1N} = -\frac{v_I}{2} \tag{2.32}$$

$$v_o = v_{oP} - v_{oN} \tag{2.33}$$

where v_I and v_o are the integrator's differential input and output signals. Following an analysis similar to that in Section 2.1.1, the differential integrator output can be expressed as:

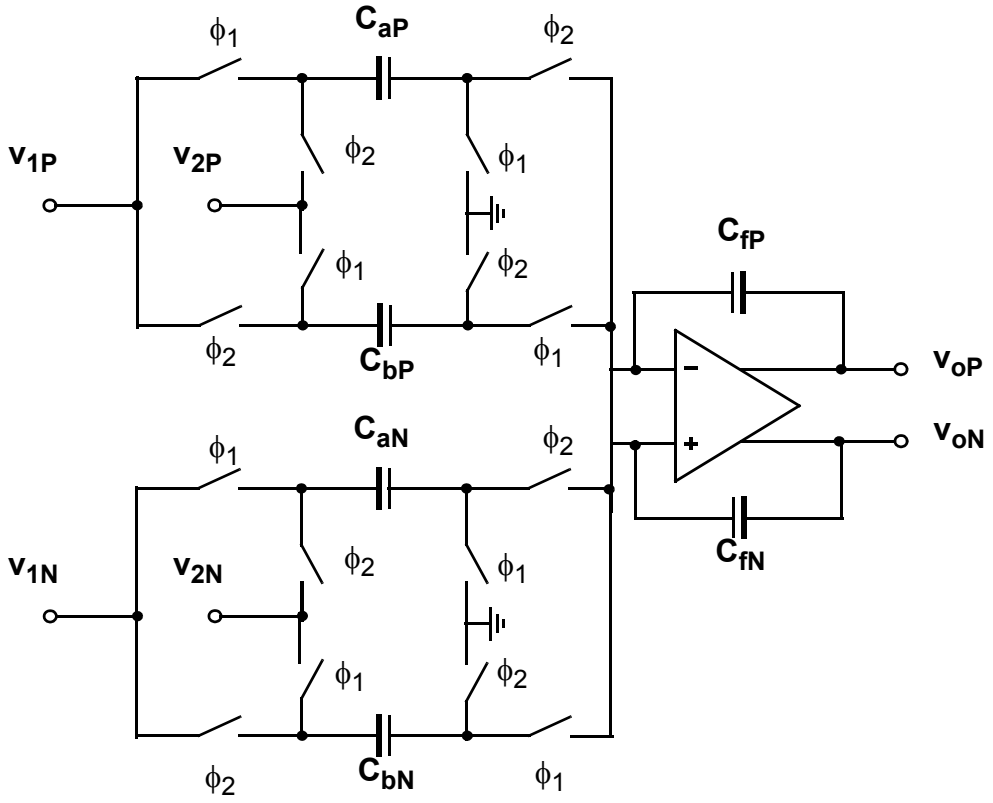


Figure 2.4 Fully-differential double-sampling SC integrator.

Term	Expression
K_{aP}	$\frac{C_{aP}}{C_{fP}}$
K_{aN}	$\frac{C_{aN}}{C_{fN}}$
K_{bP}	$\frac{C_{bP}}{C_{fP}}$
K_{bN}	$\frac{C_{bN}}{C_{fN}}$

Table 2.2 Integrator Gain expressions

- During ϕ_1:

$$v_o(n) = v_I(n-1)\left(\frac{K_{aN}+K_{aP}}{2}\right) - (v_{2P}(n)K_{aP} - v_{2N}(n)K_{aN}) + v_o(n-1) \tag{2.34}$$

- During ϕ_2:

$$v_o(n) = v_I(n-1)\left(\frac{K_{bN}+K_{bP}}{2}\right) - (v_{2P}(n)K_{bP} - v_{2N}(n)K_{bN}) + v_o(n-1) \tag{2.35}$$

where the integrator-gain coefficients are summarized in Table 2.2.

Based on expressions (2.34) and (2.35), the fully-differential double-sampling SC integrator in Figure 2.4 can be modelled in SIMULINK as shown in Figure 2.5. Here, the *MUX* block multiplexes between the two clock phases (the two gain paths) and emulates the double-sampling process.

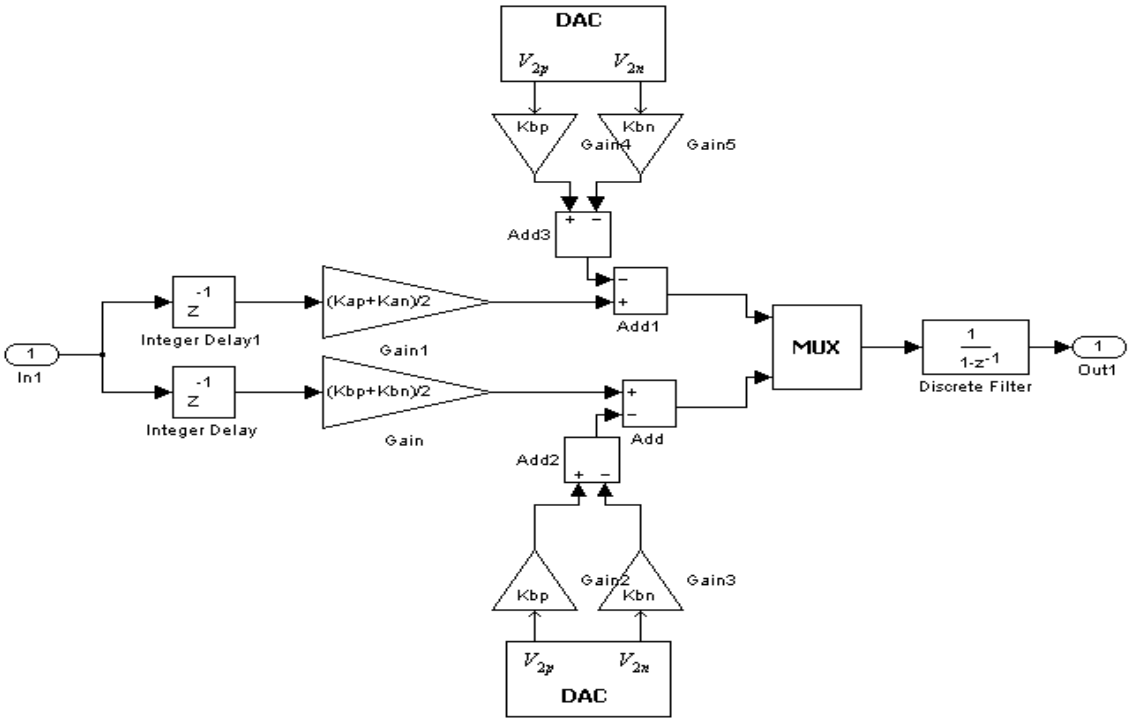


Figure 2.5 SIMULINK Model of a fully-differential double-sampling SC integrator

2.4 Mitigating Capacitor-Mismatch Effects

2.4.1 Overview

Several techniques have been proposed in the literature to alleviate the problem of quantization noise folding in double-sampled SC $\Delta\Sigma$ modulators, those include: fully-floating implementation [Senderowicz, JSSC 97], single-capacitor realization of DAC paths [Koh, ISSC05] and placing a zero in the NTF at $f_s/2$ [Rombouts, JSSC03]. The latter technique will be considered and studied in this work.

Quantization-noise folding from $f_s/2$ severely corrupts the output of the $\Delta\Sigma$ modulator and limits the achievable resolution. Placing a zero in the NTF at $f_s/2$ reduces the noise and, hence, reduces the noise folding back to dc. For an FIR NTF with the zeroes placed across the band [Schreier, TCAS93], the overall NTF can be written as [Yavari, TCAS06]:
For an even-order modulator:

$$NTF(z) = (1+z^{-1}) \bullet \prod_{i=1}^{N/2} (1 - \delta_i \bullet z^{-1} + z^{-2}) \tag{2.36}$$

where N is the modulator order and $(1+z^{-1})$ accounts for the zero at $f_s/2$.

For an odd-order modulator:

$$NTF(z) = (1-z^{-1})(1+z^{-1}) \bullet \prod_{i=1}^{(N/2)-1} (1 - \delta_i \bullet z^{-1} + z^{-2}) \tag{2.37}$$

$$\delta_i = 2\cos\left(\frac{\pi}{OSR} \cdot \frac{f_{0,i}}{f_{\mathrm{BW}}}\right) \tag{2.38}$$

where $f_{0,i}$ is the location of the inband zero.

2.4.2 Behavioral Simulations

This section compares the performance of 2nd, 3rd, 4th and 5th-order double-sampled and single-sampled $\Delta\Sigma$ modulators.

Figures 2.6 and 2.7 outline the results achieved under different settings. The results are computed for a quantizer resolution of 5 bits (B = 5) and repeated for a 6 bit resolution (B = 6). The following system parameters are used:

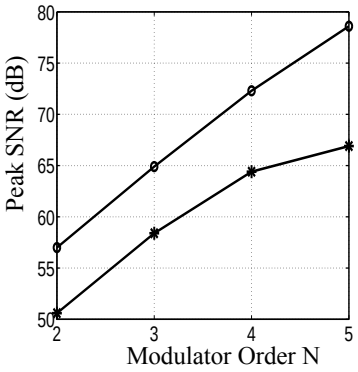
1) Quantizer reference voltage (V_{ref}) is 1 V.

2) The bandwidth is $\frac{100MHz}{4} = \frac{200MHz}{8} = 25MHz$.

3) The source of noise folding is the mismatch between the capacitors and it is assumed to be 0.1% (10 bits matching).

4) Inband zeroes are optimized and placed according to [Schreier, TCAS93].

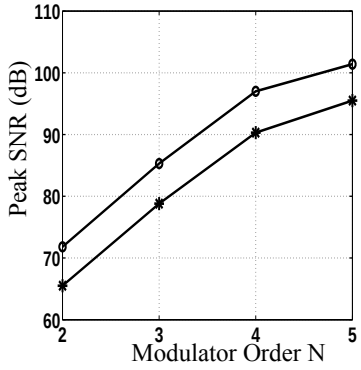
5) A unity-gain STF is used.



	X_{max}(V)	
N	**B=5**	**B=6**
2	1.00	0.98
3	0.90	0.94
4	0.70	0.86
5	0.36	0.70

f_s	**100 MHz**
OSR	4

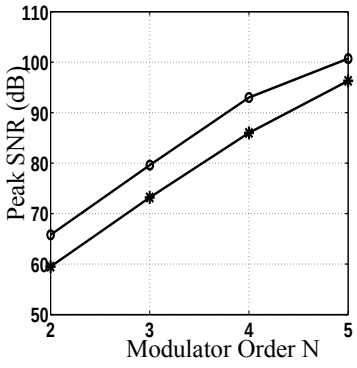
(a) OSR = 4, f_s = 100 MHz.



	X_{max}(V)	
N	**B=5**	**B=6**
2	0.97	0.98
3	0.89	0.92
4	0.68	0.83
5	0.26	0.63

f_s	**200 MHz**
OSR	8

(b) OSR = 8, f_s = 200 MHz.

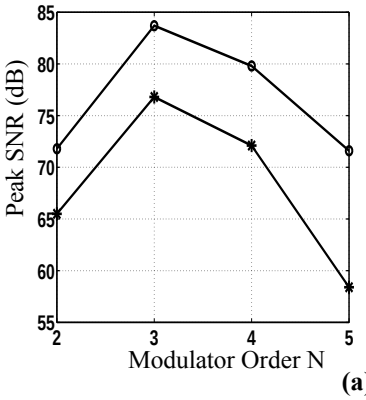


	X_{max}(V)	
N	**B=5**	**B=6**
2	0.95	0.97
3	0.93	0.95
4	0.83	0.91
5	0.61	0.81

f_s	**200 MHz**
OSR	8
Zero at $f_s/2$	Yes

(c) OSR = 8, f_s = 200 MHz, with an NTF zero at $f_s/2$.

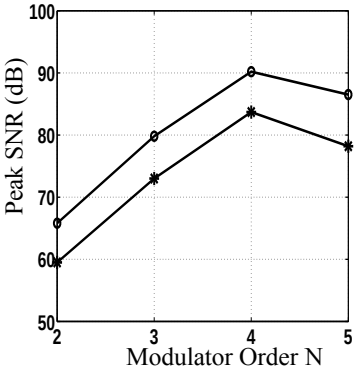
Figure 2.6 SNR vs. modulator order N for a single-sampled ΔΣ modulator with a B-bit quantizer. Here, _o_: B = 6 bits, _*_ : B = 5 bits, X_{max} is the modulator input at peak SNR.



	X_{max}(V)	
N	**B=5**	**B=6**
2	0.94	0.96
3	0.90	0.95
4	0.68	0.83
5	0.28	0.63

f_s	**200 MHz**
OSR	8

(a) OSR = 8, f_s = 200 MHz.



	X_{max}(V)	
N	**B=5**	**B=6**
2	0.96	0.97
3	0.92	0.96
4	0.84	0.92
5	0.61	0.80

f_s	**200 MHz**
OSR	8
Zero at $f_s/2$	Yes

(b) OSR = 8, f_s = 200 MHz, with an NTF zero at $f_s/2$.

Figure 2.7 SNR vs. modulator order N for a double-sampled ΔΣ modulator with a B-bit quantizer. Here, _o_: B = 6 bits, _*_ : B = 5 bits, X_{max} is the modulator input at peak SNR.

2.4.3 Conclusions

The following conclusions can be inferred from the simulations in Figures 2.6 and 2.7.

1) Adding a zero at $f_s/2$ stabilizes the $\Delta\Sigma$ modulator and this is manifested in the increase in $X_{\max}$ (Figures 2.6a and 2.6c). This is because a zero at $f_s/2$ decreases the out of band-gain of the NTF.

2) Quantization-noise folding has a less detrimental effect on the SNR in the low-order $\Delta\Sigma$ modulators (2^{nd} and 3^{rd}). This can be attributed to the fact that in high order $\Delta\Sigma$ modulators (4^{th} and 5^{th}), due to the high out of band gain and low inband quantization noise, noise folding dominates and severely affects the SNR (Figures 2.6b and 2.7a).

3) Implementing a $\Delta\Sigma$ modulator without doubling sampling and running it at a clock frequency of $f_s/2$ (Figure 2.6a) achieves a lower performance in terms of SQNR than running it at a clock frequency of $f_s/2$ with double-sampling (Figure 2.7b).

4) Placing a zero at $f_s/2$ has two opposing effects: a) It mitigates the noise at $f_s/2$ and hence reduces the amount of noise folding and improves the overall SQNR. b) It increases the inband noise by around $20\log(1+1) \cong 6dB$. The second effect outweighs the first one in the case of low-order $\Delta\Sigma$ modulators (2^{nd} and 3^{rd}). However, in higher order $\Delta\Sigma$ modulators, the first effect dominates the second one and this is the reason for the net increase in SQNR achieved after placing a zero at $f_s/2$. This can be observed in Figures 2.7a and 2.7b.

5) In the case of a 5^{th} order $\Delta\Sigma$ modulator, adding a zero at $f_s/2$ even without double sampling improves $X_{\max}$ and maintains a high SNR (Figures 2.6b and 2.6c). This is attributed to the fact that $X_{\max}$ is higher and hence compensates for the loss in gain due the

zero at $f_s/2$.

6) Double-sampling 2nd $\Delta\Sigma$ modulators can be used without having the need to use Noise folding reduction techniques. This can be observed in Figures 2.6b and 2.7a, where the SNR of 2nd order $\Delta\Sigma$ modulators does not change even after double sampling and hence having quantization noise folding.

In conclusion, 2nd order $\Delta\Sigma$ modulators are suitable for double sampling and will be used in this thesis to implement the final circuit. Details of the architecture will be discussed in the next chapter.

Chapter 3

Digital-Feedforward Delta-Sigma Modulators

Electronics technology is drifting towards miniaturization, in which the channel length of MOS transistors shrinks down to nanometer levels. This in turn introduces new design constraints, which include the scaling down of the maximum supply voltage. Hence, the maximum swing available at the output of opamps in switched-capacitor (SC) circuits is limited. One solution to this problem in SC ΔΣ modulators is to utilize input feedforward paths [J.Silva, LETT01] [Hamoui, TCAS04]. This technique involves the addition of the input signal before the quantizer as shown in Figure 3.1. Consequently the integrators in the loopfilter only process shaped quantization noise and, hence, the limited swing problem is solved [Hamoui, TCAS04].

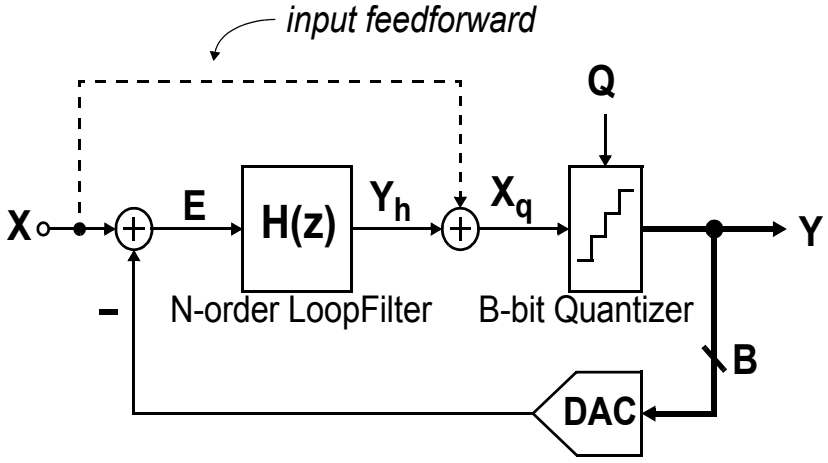


Figure 3.1 Linear model of a single-stage ΔΣ modulator with an input feedforward path (dashed line) implemented in the analog domain.

However, an addition before the quantizer introduces some problems that severely limit the implementation of input feedforward paths in practise. The addition can be implemented in an active or a passive manner. The implication of each case is as follows:

1) The adder can be realized as an SC passive adder. However, this scheme implies that the quantizer input (Figure 3.1) will be $(X + Y_h)/2$. To maintain the same resolution, the reference voltage of the flash ADC has to be $V_{\text{ref}}/2$, which means that the comparators must have smaller offset voltages. This is problematic in low-voltage multibit $\Delta\Sigma$ modulators [Hamoui, TCAS04].

2) If the adder is realised as an active design [Fujimoto, CICC06], which involves using an amplifier to make $X_q = (X + Y_h)$. This amplifier has to have a large output swing to be able to accommodate X_q, this in turn defeats the purpose of using input feedforward. In addition to that, the need of active components implies an increase in the power dissipation.

Hence, to get rid of this problem, the input signal has to be added somewhere else in the $\Delta\Sigma$ modulator. The next section discusses an alternative method to feedforward the input signal.

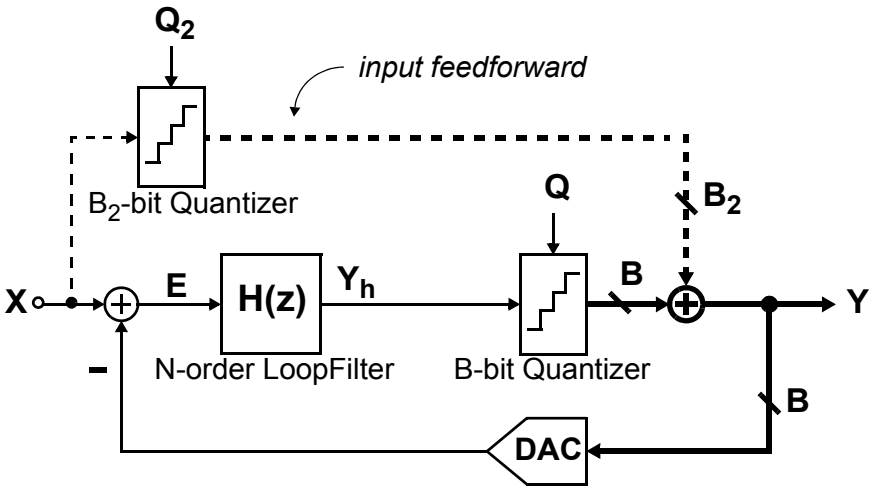


Figure 3.2 Linear model of a single-stage ΔΣ modulator with an input feedforward path (dashed line) implemented in the digital domain.

3.1 Delta-Sigma Modulators with Input Feedforward

Figure 3.1 depicts a $\Delta\Sigma$ modulator with the input feedforward implemented using an analog feedforward (AFF) path. An alternative way to AFF is to feedforward the input signal using a digital feedforward (DFF) path. This is accomplished by adding the input after the quantizer in the digital domain, this is depicted in Figure 3.2. Before being able to add the input signal in the digital domain, it has to get quantized. Quantizing the input adds an extra quantization noise factor to the $\Delta\Sigma$ modulator. As shown in Figure 3.2, this extra noise is denoted by Q_2. To preserve the performance, the final output of the $\Delta\Sigma$ modulator should not contain this Q_2 term. The DFF $\Delta\Sigma$ modulator used in this thesis, eliminates the Q_2 term from the final output through digital cancellation. This will be discussed in Section 3.1.2.

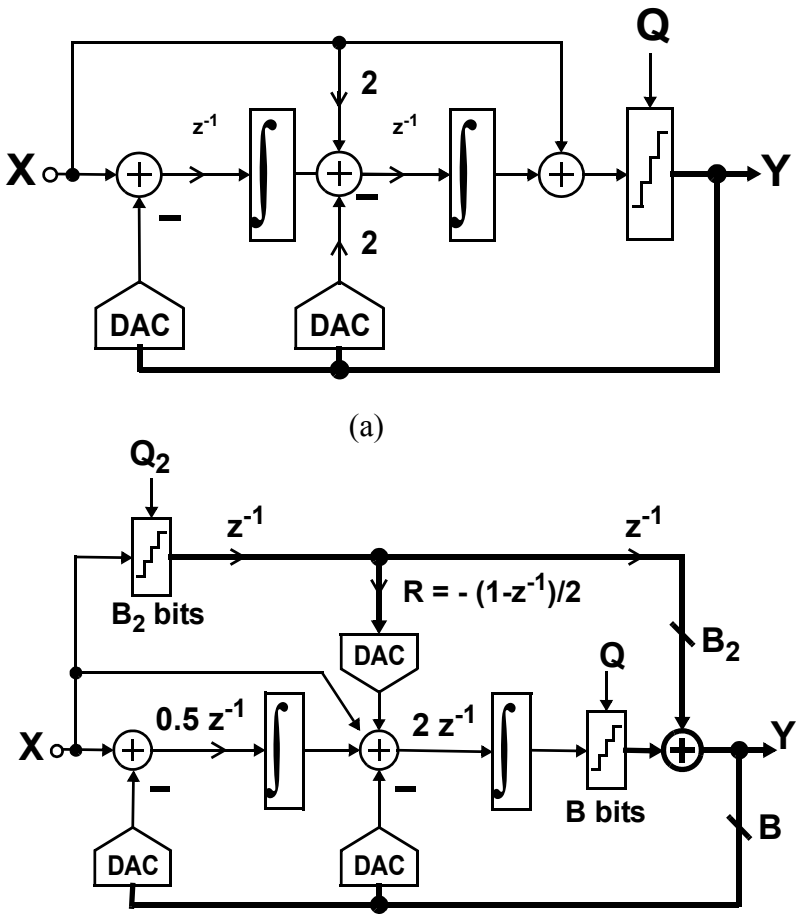


Figure 3.3 2^{nd}-order distributed-DAC-feedback ΔΣ modulators with: a) analog feedforward, $\mathbf{NTF} = (\mathbf{1} - z^{-1})^2$, and $\mathbf{STF} = \mathbf{1}$ [Benabes, LETT93]. b) digital feedforward (DFF), $\mathbf{NTF} = (\mathbf{1} - z^{-1})^2$, and $\mathbf{STF} = \mathbf{1} - \mathbf{NTF}$ [Kwon, ISCAS04]; Here $\int \equiv 1/(1 - z^{-1})$.

3.1.1 Second-Order Feedforward ΔΣ Modulators

The signal and noise transfer functions of a ΔΣ modulator (Figures 3.1 and 3.2) are defined, respectively, as:

$$STF \equiv \left.\frac{Y}{X}\right|_{Q=0} \tag{3.1}$$

$$NTF \equiv \left.\frac{Y}{Q}\right|_{X=0} \tag{3.2}$$

The 2nd-order AFF $\Delta\Sigma$ modulator proposed in [Benabes, LETT93] (shown here in Figure 3.3a) has:

$$NTF = (1 - z^{-1})^2 \tag{3.3}$$

$$STF = 1 \tag{3.4}$$

The 2nd-order DFF $\Delta\Sigma$ modulator proposed in [Kwon, ISCAS04] (shown here in Figure 3.3b) has :

$$NTF = (1 - z^{-1})^2 \tag{3.5}$$

$$STF = 1 - NTF \tag{3.6}$$

3.1.2 Second-Order DFF $\Delta\Sigma$ Modulator with STF=1

To realize a DFF $\Delta\Sigma$ modulator with STF = 1, the $\Delta\Sigma$ modulator architecture in Figure 3.4 was proposed in [Hamoui, ISCAS08]. Here, to process the additional quantization noise Q_2 without affecting the STF, the difference between the output of the extra B_2-bit quantizer and the output of the $\Delta\Sigma$ modulator is applied at the output of the loopfilter integrators. The loop filter is

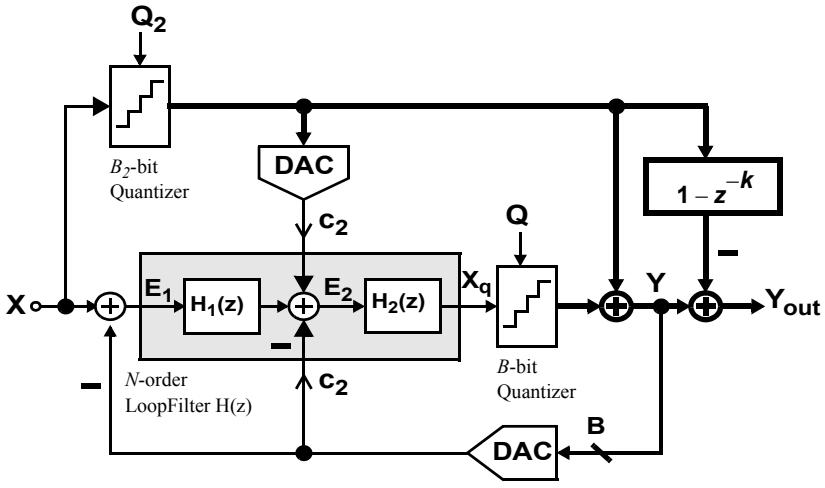


Figure 3.4 Architecture for a $\Delta\Sigma$ modulator with digital input feedforward (DFF) and unity-gain STF (STF = 1), as proposed in [Hamoui, ISCAS08].

then designed such that the modulator output is

$$Y = X + (1 - z^{-1})^N Q + (1 - z^{-K})\, Q_2 \tag{3.7}$$

where N is the order of the loopfilter and K is a design parameter. Next, to cancel the additional quantization noise Q_2 at the modulator output, the output $(X + Q_2)$ of the extra B_2-bit quantizer is multiplied by $(1 - z^{-K})$ and subtracted from the output of the main quantizer in the digital domain. Thus, the overall output of the delta-sigma modulator is then given by

$$Y_{\text{out}} = STF \cdot X + NTF \cdot Q \tag{3.8}$$

where $STF = z^{-K}$ and $NTF = (1 - z^{-1})^N$. Accordingly, the DFF $\Delta\Sigma$ modulator can be designed for an FIR NTF and a unity-gain STF ($|\text{STF}| = 1$).

Observe that the DFF $\Delta\Sigma$ modulator architecture in Figure 3.4 has an additional quantization noise component $(1 - z^{-K}) \cdot Q_2$ in the feedback signal Y (as per equation (3.7)). The choice of K has the following implications on the behavior of the $\Delta\Sigma$ modulator:

1) Reducing the value of K (ideally K=1) reduces the noise power contributed by $(1 - z^{-K}) \cdot Q_2$ and, hence, lowers the swing in the loopfilter integrators (Section 3.3).

2) Due to the presence of circuit nonidealities such as nonlinear opamp dc gain and capacitor mismatches, the cancellation of Q_2 at the modulator output Y_{out} will not be perfect and will result in some of noise leaking (similar to the noise leakage at the output of MASH $\Delta\Sigma$ modulators [Vleugels 02]). Hence, selecting K=1 results in the least noise leakage, as any noise leakage will be first-order shaped by $(1 - z^{-1})$, (as derived in Section 3.3 and simulated in Section 3.2).

Low-Voltage Operation

Consider the DFF $\Delta\Sigma$ modulator proposed in Figure 3.4. The signals at the input of filters $H_1(z)$ and $H_2(z)$ can be expressed as:

$$E_1 = -Q_2(1-z^{-K}) - NTF \cdot Q_1 \tag{3.9}$$

$$E_2 = E_1 \cdot H_1(z) + Q_2 \cdot z^{-K} \cdot c_2 - NTF \cdot Q_1 \cdot c_2 \tag{3.10}$$

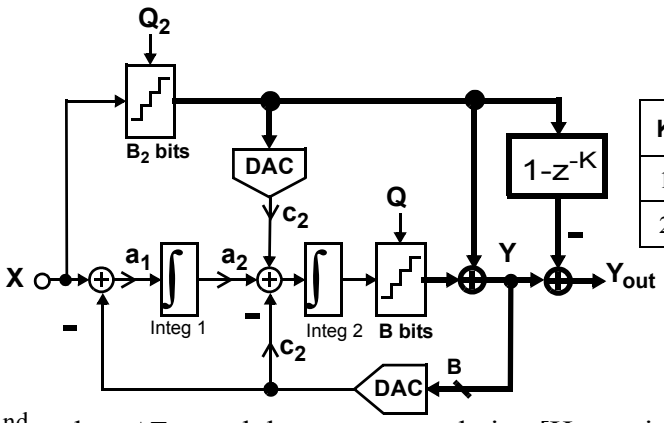
Furthermore, the signal at the input of the main quantizer is given by:

$$X_q = E_2 \cdot H_2(z) \tag{3.11}$$

Accordingly, the main quantizer and SC integrators inside $H_1(z)$ and $H_2(z)$ only process shaped quantization noise. Hence, voltage-swing reduction is achieved.

3.1.3 Proposed 2nd Order Delta-Sigma Modulators

Figure 3.5 shows the 2nd-order realization of the $\Delta\Sigma$ modulator architecture in Figure 3.4, as proposed in [Hamoui, ISCAS08]. Observe that this realization has no delays in any quantizer path and, hence, latched comparators cannot be used to implement the quantizers. However, in low-voltage multibit $\Delta\Sigma$ modulators (like the one used in this thesis), the quantizer's step size is very small, thereby requiring latched comparators to achieve small offset voltages. Therefore, to enable the use of latched comparators, the 2nd-order DFF $\Delta\Sigma$ modulator (with K=1) in Figure 3.5 can be realized as shown in Figure 3.6, where delays are incorporated in the quantizer paths.



K	a_1	a_2	c_2
1	1	z^{-1}	z^{-1}
2	z^{-1}	z^{-1}	$2z^{-1}$

Figure 3.5 2nd-order ΔΣ modulator proposed in [Hamoui, ISCAS08] with digital feedforward (DFF), $\boldsymbol{NTF} = (\mathbf{1}-z^{-1})^{\mathbf{2}}$, and $\boldsymbol{STF} = z^{-K}$ $(\boldsymbol{K} = \mathbf{1}, \boldsymbol{K} = \mathbf{2})$. The corresponding feedforward coefficients are given in the table. Here $\int \equiv 1/(1-z^{-1})$.

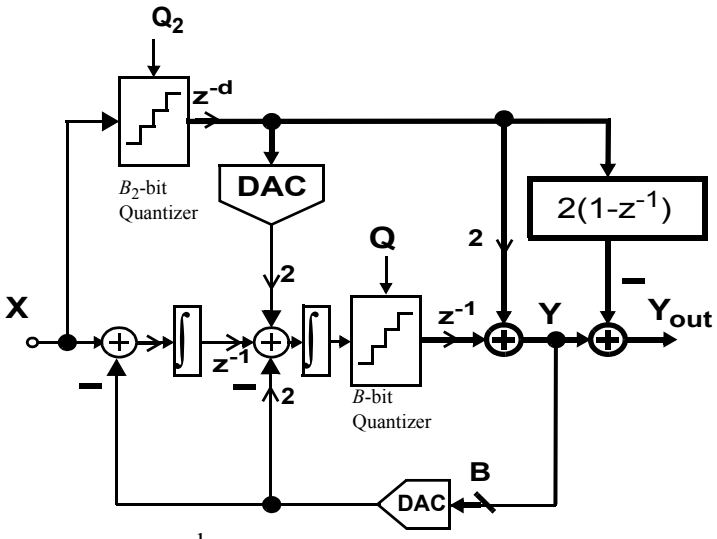


Figure 3.6 Realization of the 2nd-order DFF ΔΣ modulator in Figure 3.5 (K=1) with a unit-delay z^{-1} at the main-quantizer output and an arbitrary delay z^{-d} at the extra-quantizer output. Here $\int \equiv 1/(1-z^{-1})$.

3.2 Behavioral Simulations

The ΔΣ modulators in Figures 3.3 and 3.5 were simulated in SIMULINK for the following design specifications:

- 32-level mid-tread quantizers ($B = B_2 = 5$ bits) and OSR = 32.
- The quantizer reference voltage is normalized to $V_{\text{REF}} = 1$ V.
- The amplitude of the sinusoidal input signal is $V_{\text{in}} = 0.5$ V (-6 dBFS).
- The input-signal frequency is set to $f_{\text{in}} = f_S/(8 \cdot \text{OSR})$, so that the first 4 input-signal harmonics fall within the signal band.

The SIMULINK behavioral simulations accounted for the following loopfilter nonidealities:

1) Opamp Nonidealities: The integrators in the ΔΣ loopfilter are modeled as described in [Hamoui, ISLPED06] to account for the finite dc gains, the nonlinear dc-gain variations, and the output saturation voltages of the opamps in practical SC integrators. These opamps are assumed to have a **maximum dc gain** $\boldsymbol{A_{0\text{max}}}$ = 150V/V (43 dB) and an output saturation voltage V_{Osat} = 1 V. This is to account for the low dc gains of the opamps in nanometer CMOS technologies.

2) Modulator Coefficients: To account for variations in modulator coefficients, the signal-to-noise-plus-distortion ratio (SNDR) values reported correspond to the minimum SNDR values found over 50 simulations in which each modulator coefficient is assumed to have a **uniformly-distributed random error** in the range $\pm \boldsymbol{e_{\text{coeff}}}$ = 1%.

Table 3.1 Comparison between the 2nd-order ΔΣ modulators with input feedforward in Figures 3.4 and 3.5.

Configuration	**AFF modulator (Figure 3.3a)** B **= 5 bits**	**Previous DFF modulator (Figure 3.3b)** $B = B_2 = 5$ **bits**	**Proposed DFF modulator with STF=1 (Figure 3.5)** $B = B_2 = 5$ **bits**	
			$K = 1$	$K = 2$
SNDR at V_{in} = - 6dBFS with A_{0max} = 150V/V $\pm e_{coeff}$ = 1%	82.9	80.5	85	80
1st-integrator Output Swing (absolute maximum)	0.06	0.03	0.10	0.08
2nd-integrator Output Swing (absolute maximum)	0.09	0.12	0.11	0.11
Quantizer Input Swing (absolute maximum)	0.58	0.12	0.11	0.11
No. of Comparators in Main Quantizer	32	4	4	4
No. of Comparators in Extra Quantizer	0	32	32	32
Total No. of Comparators	32	36	36	36

Table 3.1 summarizes the behavioral simulation results. Accordingly, the DFF ΔΣ modulators achieve a comparable SNDR and output-swing reduction, as the AFF ΔΣ modulator. However, observe that the signal swing at the quantizer input is much more reduced in the DFF ΔΣ modulators, compared to AFF ΔΣ modulator. This is because, in the AFF ΔΣ modulator, the full-swing input signal appears at the quantizer input. Whereas, in the DFF ΔΣ modulator, no input-signal component appears at the input of the main quantizer and only shaped quantization noise is processed by the main quantizer (equation (3.11)). Owing to this swing reduction (shown in Table 3.1), the number of comparators needed in the main quantizer of the DFF ΔΣ modulators can be reduced from 32 to 4. Accordingly, the total number of comparators required in the main and the extra quantizers of the DFF ΔΣ modulators is only increased by 4, relative to that required in the AFF ΔΣ modulator.

Figure 3.7 shows the swing distribution at the output of each integrator in the loopfilter. Accordingly, the swing reduction in the DFF ΔΣ modulators is comparable to that in the AFF modulator.

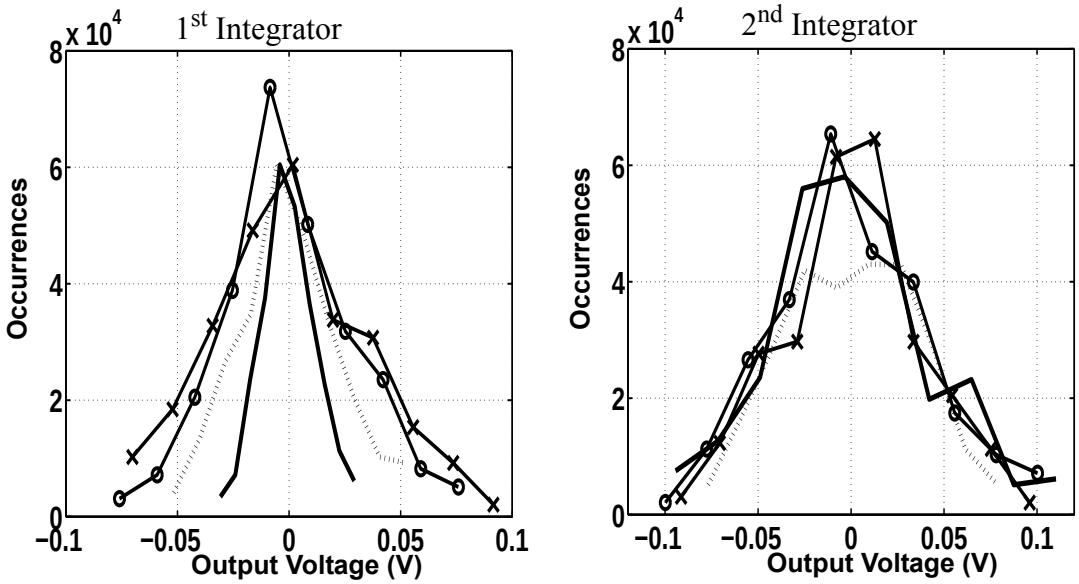


Figure 3.7 Signal swing at the integrator outputs. Here:_o_ = DFF ΔΣ modulator with STF=1 and *K*=1 in Figure 3.5, _X_ = DFF ΔΣ modulator with STF=1 and *K*=2 in Figure 3.5, ___ = DFF ΔΣ modulator in Figure 3.3a, and ---- = AFF ΔΣ modulator in Figure 3.3b.

Figure 3.8a shows the SNDR versus the maximum dc gain $A_{0\max}$ of the opamps in the SC integrators of the loopfilter, assuming an error of e_{coeff} = 1% in the modulator coefficients. Accordingly, the sensitivity of the DFF ΔΣ modulators to opamp dc gains is comparable to that of the AFF ΔΣ modulator. Furthermore, the DFF ΔΣ modulator with STF=1 can achieve a high resolution and linearity (SNDR > 13 bits at V_{in} = –6 dBFS), using opamps with only moderate dc gains (less than 100 V/V).

Figure 3.8b shows the SNDR versus gain coefficient error e_{coeff} in the modulator coefficients, assuming a maximum dc gain $A_{0\max}$=150V/V (43 dB) for the opamps. Accordingly, the DFF ΔΣ modulators with STF=1 in Figure 3.5 can tolerate a 2% variation in their loopfilter coefficients with only 2-dB and 3-dB drop in SNDR for *K*=1 and *K*=2, respectively. However, the SNDR of the AFF ΔΣ modulator and the DFF ΔΣ modulator in Figure 3.3 drop by 2 dB and 6 dB, respectively.

Observe that the sensitivity of the DFF ΔΣ modulators with STF=1 to the finite dc gains of the opamps and to the variations in loopfilter coefficients (Table 3.1 and Figure 3.8) is reduced by designing the modulator with $K = 1$, rather than $K = 2$ (Figure 3.5). This performance improvement

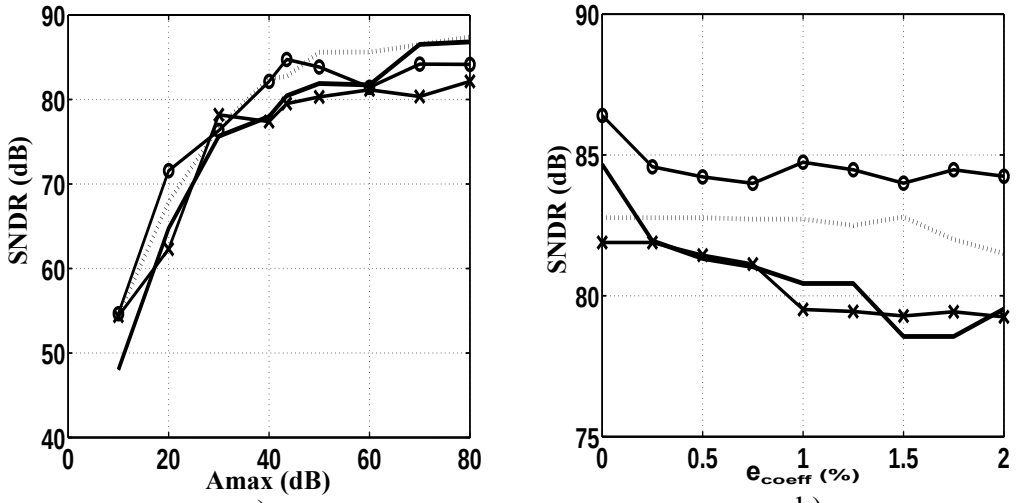


Figure 3.8 SNDR vs. a) maximum opamp dc gain $A_{0\max}$ at a gain coefficient error e_{coeff}=1%. b) gain coefficient error e_{coeff} at an $A_{0\max}$ of 150 V/V. Here: _o_ = DFF $\Delta\Sigma$ modulator with STF=1 and K=1 in Figure 3.5, _X_ = DFF $\Delta\Sigma$ modulator with STF=1 and K=2 in Figure 3.5, ___ = DFF $\Delta\Sigma$ modulator in Figure 3.3a, and ---- = AFF $\Delta\Sigma$ modulator in Figure 3.3b.

is a result of the 1st-order shaping $(1-z^{-1})$ of the quantization-noise leakage at the modulator output, when K=1 (as discussed in Section 3.1).

3.3 Appendix: Mathematical Derivations

In this appendix, the noise power of $Q_2(1-z^{-K})$ (in equation (3.7)) will be quantified and it will be proven that the smaller the *K* value (ideally 1) the lower the noise power. The delay term z^{-K} (where *K* is a positive integer) can be approximated within the signal band [0, f_{BW}] as:

$$z^{-K} = e^{-j\cdot\frac{2\pi f}{f_s}\cdot K} \cong 1 - j\cdot\frac{2\pi f}{f_s}\cdot K \tag{3.12}$$

assuming $OSR \gg K\cdot\pi \quad\Leftrightarrow\quad K\cdot\dfrac{2\cdot\pi\cdot f_{\mathrm{BW}}}{f_s} \ll 1$.

Assume white quantization noise with power spectral density $\overline{Q_2^{\,2}}$ at the input of a filter $1-z^{-K}$. Then, the inband quantization-noise power at the filter output can be approximated, using (3.12), as:

$$P_Q \equiv 2\cdot\int_0^{f_{\mathrm{BW}}}\overline{Q_2^{\,2}}\cdot\left|1-z^{-K}\right|^2 df = 2\cdot\overline{Q_2^{\,2}}\cdot\int_0^{f_{\mathrm{BW}}}\left|1-e^{-j\cdot\frac{2\pi f}{f_s}\cdot K}\right|^2 df \tag{3.13}$$

$$= \frac{2}{3}\cdot K^2\cdot\frac{\pi^2}{OSR^2}\cdot\overline{Q_2^{\,2}}\cdot f_{\mathrm{BW}}$$

In conclusion, to minimize noise power, the DFF $\Delta\Sigma$ modulator in Figure 3.4 has to be designed for a small *K* (ideally 1).

Chapter 4

Architectural-Level Design

This chapter describes the architectural-level design of the proposed 2^{nd}-order digital-feedforward $\Delta\Sigma$ modulator with 5-bit quantizers in Figure 3.5 with K=2. Observe that a slightly better performance can be achieved with K=1 compared to K=2 (as described in Section 3.2). However, the DFF $\Delta\Sigma$ modulator is more complex to implement with K=1 because its first integrator is non-delaying. Therefore, a DFF $\Delta\Sigma$ modulator with K=2 is considered in this thesis. The targeted specifications are a signal bandwidth of $f_{\mathrm{BW}} = 2.8\,\mathrm{MHz}$ and a signal-to-noise-plus-distortion ratio of SNDR = 12 bits (74 dB). A double-sampling switched-capacitor (SC) circuit implementation is assumed, with an effective sampling frequency* of $f_s = 200\,\mathrm{MHz}$ and an oversampling ratio of OSR = 35. Later, Chapter 5 will describe the circuit-level implementation of this $\Delta\Sigma$ modulator in a 1-V 65-nm CMOS technology.

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* For a double-sampled modulator, f_s refers to the *effective* sampling frequency, with $f_s = 2f_{\mathrm{CLK}}$ where f_{CLK} is the clock frequency.

4.1 Behavioral Model of an SC ΔΣ Modulator

4.1.1 SC Integrator Nonidealities

The behavioral model proposed in [Hamoui, ISLPED06] was utilized to simulate practical SC integrators in SIMULINK. It models the effects of the following opamp nonidealities on the transfer function of an SC integrator (Figure 4.1), during its charge-transfer phase [Hamoui, ISLPED06]:

1. Finite dc gain A_0.
2. Nonlinear variations in dc gain A_0 with output voltage v_O.
3. Limited output-signal (output saturation voltage V_{Osat}).
4. Dynamic effects (finite bandwidth ω_{3dB} and slew rate *SR*).
5. Parasitic capacitances (C_{in} and C_{out}).
6. Feedforward transmission of feedback capacitor C_F.

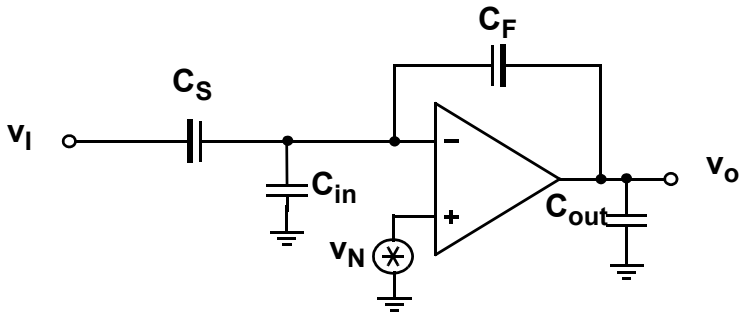

Figure 4.1 Switched-capacitor integrator during its charge-transfer phase. Here, capacitors C_{in} and C_{out} represent the total capacitances, including any parasitic, at the input and output nodes of the opamp, while v_N represents the input-referred noise voltage of the opamp.

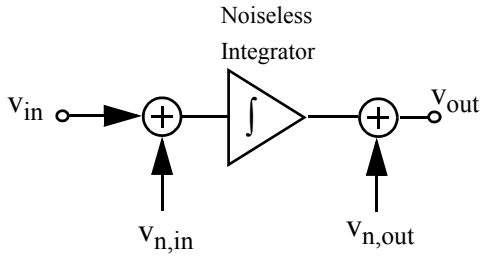

Figure 4.2 Noise model of a *single-sampled* SC integrator in SIMULINK.

4.1.2 Noise Model of a Double-sampled SC Integrator

According to [Schreier, TCAS05], the thermal noise model of a single-sampled SC integrator can be modeled using input and output referred sources, as depicted in Figure 4.2. Assuming no input parasitic capacitance ($C_{in} = 0$), the input-referred thermal noise $v_{n,\,in}$ of an SC integrator with a single-ended input can be expressed as [Schreier, TCAS05]:

$$v_{n,\,in} = \sqrt{\frac{kT}{C_S}} + \sqrt{\frac{kT/C_S}{1 + 1/(2 \cdot G_m \cdot R_{ON})}} + \sqrt{\frac{\overline{V^2_{opamp,\,T}}}{4 \cdot \left(\frac{C_S}{G_m} + 2 \cdot R_{ON} \cdot C_S\right)}} \tag{4.1}$$

where C_S is the sampling capacitor, G_m is the opamp's transconductance and $\overline{V^2_{opamp,\,T}(f)}$ is the power spectral density of the opamp's input-referred thermal noise and R_{ON} is the on resistance of each switch. The first term in equation (4.1) accounts for the switch thermal noise during the sampling phase. The second and third terms account for, respectively, the switch thermal noise and the opamp's thermal noise during the charge-transfer phase.

The output referred thermal noise $v_{n,\,out}$ (Figure 4.2) accounts for the opamp's thermal noise during the sampling phase, and can be expressed as [Schreier, TCAS05]:

$$v_{n,\,out} = \sqrt{\frac{G_m \cdot \overline{V^2_{opamp,\,T}}}{4 \cdot C_{S,\,next}}} \tag{4.2}$$

where $C_{S,\,next}$ is the load capacitor of the integrator during the sampling phase (i.e., the sampling capacitor of the next integrator).

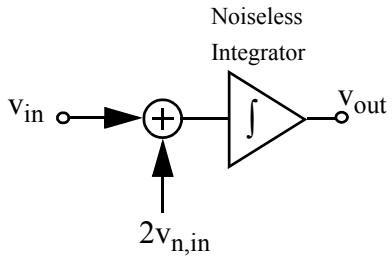

Figure 4.3 Noise model of a *double-sampled* SC integrator in SIMULINK.

In a double-sampled SC integrator, the opamp is in a charge-transfer mode during both the sampling and charge-transfer clock phases. Therefore, $v_{n,\,out}$ should not be included in the noise model of a double-sampled SC integrator, as it accounts for the opamp thermal noise during the sampling phase. Furthermore, in a double-sampled SC integrator, both sampling and integration occur during each clock phase. Therefore, since one clock cycle in the SIMULINK model combines the two clock phases (sampling and charge transfer), all noise will be doubled in one clock cycle in the SIMULINK model. Accordingly, the model in Figure 4.3 must be used for the noise simulation of a double-sampled SC integrator in SIMULINK.

Note that a SIMULINK model for flicker noise was not derived. However, relevant FFT bin values from circuit-level flicker-noise simulations were incorporated into the final system-level simulations.

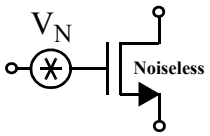

Figure 4.4 Noise model for a MOSFET operating in the active region.

4.1.3 Noise Model of a MOS Transistor

In a MOS device operating in the active region, the power spectral density of the gate-referred voltage noise (Figure 4.4) can be expressed as [Johns 97]:

$$\overline{V_N^2}(f) = \overline{V_{N,T}^2}(f) + \overline{V_{N,f}^2}(f) \tag{4.3}$$

where $\overline{V_{N,T}^2}(f)$ and $\overline{V_{N,f}^2}(f)$ are the power spectral densities of, respectively, the thermal and the flicker noise in the MOS transistor with:

$$\overline{V_{N,T}^2}(f) = 4kT\gamma_T\frac{1}{g_m} \tag{4.4}$$

$$\overline{V_{N,f}^2}(f) = \frac{\gamma_f}{WLC_{ox}f} \tag{4.5}$$

Here, g_m is the short-circuit transconductance, C_{ox} is the gate-oxide capacitance per unit area, W is the transistor's width, and L the transistor's length. The values of the empirical constants γ_T and γ_f depend on the MOS technology and on the characteristics and sizes of the MOS transistor.

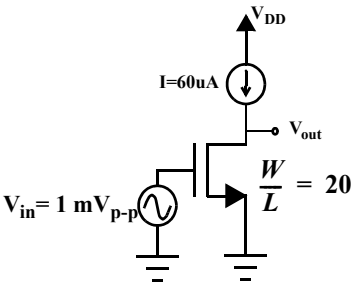

Figure 4.5 Test set-up used to approximate the value of γ_T in 65 *nm*.

To determine the value of γ_T in the 65-nm CMOS technology under consideration, the power spectral density $\overline{V_{N,T}^2}$ of the thermal noise in the MOS transistor of the test circuit in Figure 4.5 was simulated and γ_T was approximated as:

$$\gamma_T = \frac{g_m \overline{V_{N,T}^2}(f)}{4 \cdot k \cdot T} \tag{4.6}$$

The value γ_T was found to be approximately 10 in the frequency range of 200 MHz to 1 GHz.

4.1.4 Clock Jitter

In a low-pass discrete time $\Delta\Sigma$ modulator, the effect of random clock jitter in the input S/H can be modelled as an additive output error with a white power spectral density [Tao, TCASII99]:

$$\overline{V_{jitter}^2}(f) = \frac{1}{8} \cdot A^2 \cdot \left(\frac{1}{OSR^2}\right) \cdot \sigma_{\Delta t}^2 \cdot f_s \tag{4.7}$$

where A is the amplitude of the input signal and $\sigma_{\Delta t}^2$ is the variance of the clock jitter.

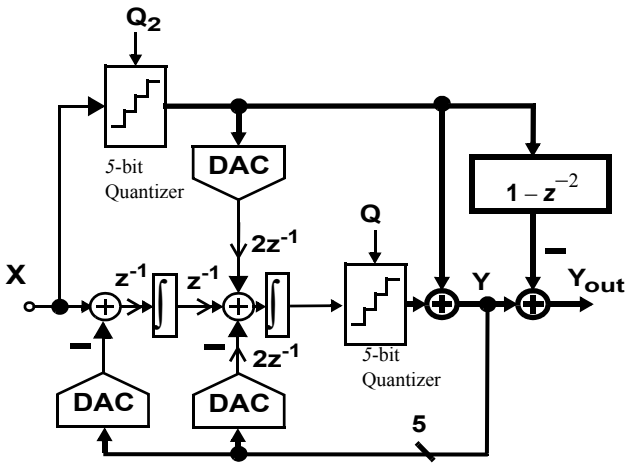

Figure 4.6 Digital-feedforward 2nd order ΔΣ modulator proposed in Figure 3.5 (with K =2). Here, $\int \equiv 1/(1-z^{-1})$.

4.2 Modulator Noise Budget

SIMULINK simulations of the proposed digital-feedforward 2nd-order ΔΣ modulator in Figure 3.5 (redrawn in Figure 4.6) were performed using the behavioral models outlined in Section 4.1. The *minimum* opamp specifications (including the integrator sampling capacitors) required to achieve an SNDR = 13 bits (80 dB) were determined, thus ensuring minimum power dissipation when the ΔΣ modulator is implemented. These opamp specifications are summarized in Table 4.1. The corresponding noise budget for the ΔΣ modulator is summarized in Table 4.2. Note that the ΔΣ modulator is designed to have a 1-bit higher SNDR than the targeted SNDR, in order to account for circuit nonidealities that were not fully modeled at the architectural level.

To compare the performance of the proposed ΔΣ modulators in Section 3.1.3, the ΔΣ modulator in Figure 3.6 (redrawm in Figure 4.7) was also simulated using the opamp specification in Table 4.1. The resulting noise budget for the ΔΣ modulator is summarized in Table 4.3. Accordingly, under the same conditions, both proposed ΔΣ modulators in Figures 4.6 and 4.7 achieve approximately the same performance (Tables 4.2 and 4.3).

Specification	First Opamp	Second Opamp
Total sampling capacitance in all integrator input branches	2.4 pF	2.4 pF
Short-circuit transconductance of input differential pair (g_{m1})	4m A/V	1.5 m A/V
Input voltage swing	450 mV	400 mV
DC gain (A_ϕ)	100 V/V	100 V/V
Unity-gain frequency (f_t)	265 MHz	99 MHz
Slew rate (SR)	120 V/μs	80 V/μs
Input-referred thermal noise ($\overline{V^2_{opamp,T}}$)	$1 \times 10^{-16} V^2/Hz$	$3 \times 10^{-16} V^2/Hz$

Table 4.1 Minimum opamp specifications.

Error Source (Vin = 0.9V_{REF}; V_{REF} = 1 V; OSR = 35; f_{in} = 200 KHz; f_S = 200 MHz)	**SNDR (dB)**
Ideal Case (quantization noise only)	95.7
Additional Error Sources	
DAC capacitor mismatch ($\sigma = 0.2\%$) with DWA	91.4
$\frac{kT}{C}$ noise from the sampling switches ($C_S = 2.4pF$)	86
Opamp input-referred noise ($\overline{V^2_{opamp,T}}(f) = 1.0 \times 10^{-16} V^2/Hz$)	83.2
Opamp nonlinear dc gain ($A_\phi = 100V/V$)	81.1
Opamp bandwidth ($f_t = 265MHz$) and Slew rate (SR=120 $\mu V/s$)	84
Jitter Noise ($\sigma_{\Delta\tau} = 2ps$) @ $f_s = 200MHz$	95.5
Modulator including all non-idealities	79.3

Table 4.2 Noise budget for the SC double-sampled circuit implementation of the ΔΣ modulator in Figure 4.6.

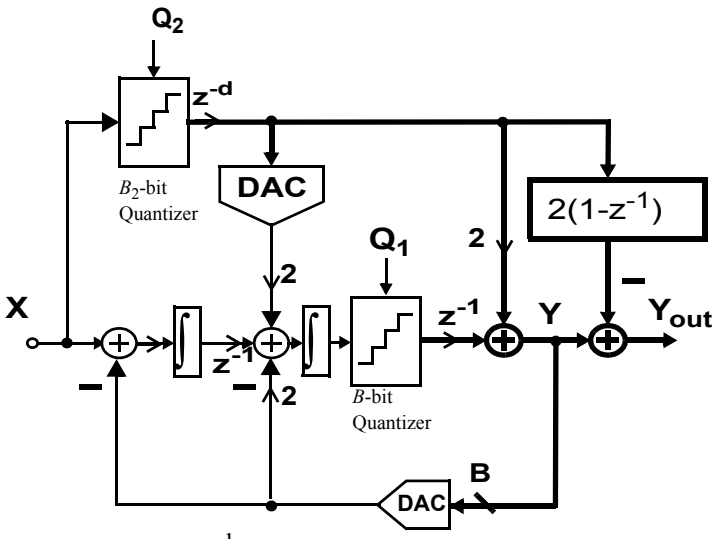

Figure 4.7 Digital-feedforward 2nd-order ΔΣ modulator proposed in Figure 3.6 (with *d*=1). Here, $\int \equiv 1/(1-z^{-1})$.

Error Source (Vin = 0.9V_{REF}; V_{REF} = 1 V; OSR = 35; fin = 200 KHz; fs = 200 MHz)	**SNDR (dB)**
Ideal Case (quantization noise only)	95.5
Additional Error Sources	
DAC capacitor mismatch ($\sigma = 0.2\%$) with DWA	90.9
$\frac{kT}{C}$ noise from the sampling switches ($C_S = 2.4pF$)	85.6
Opamp input-referred noise ($\overline{V^2_{opamp,T}(f)} = 1.0 \times 10^{-16} V^2/Hz$)	83.8
Opamp nonlinear dc gain ($A_\phi = 100V/V$)	80.3
Opamp bandwidth ($f_t = 265MHz$) and Slew rate (SR=120 $\mu V/s$)	83.5
Jitter Noise ($\sigma_{\Delta\tau} = 2ps$) @ $f_s = 200MHz$	95.5
Modulator including all non-idealities	78.9

Table 4.3 Noise budget for the SC double-sampled circuit implementation of the ΔΣ modulator in Figure 4.7

Chapter 5

Double-Sampling Switched-Capacitor Circuit Implementation

This chapter presents the double-sampling switched-capacitor (SC) circuit-level design (in a 1-V 65-nm CMOS technology) of the loopfilter $H(z)$ of the 2^{nd}-order $\Delta\Sigma$ modulator with 5-bit quantizers in Figure 5.1. The architecture-level design of this $\Delta\Sigma$ modulator was presented in Section 4.2 (Figure 4.6).

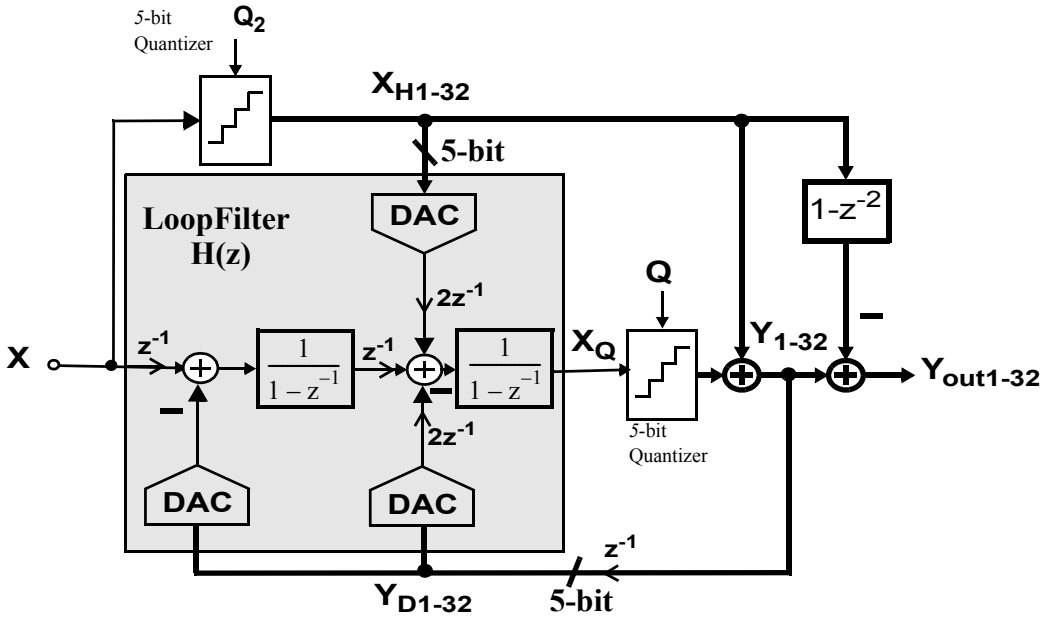

Figure 5.1 Architecture of the $\Delta\Sigma$ modulator. Its architectural-level design was presented in Section 4.2 (Figure 4.6). The circuit-level design of the loopfilter $H(z)$ is presented in this chapter.

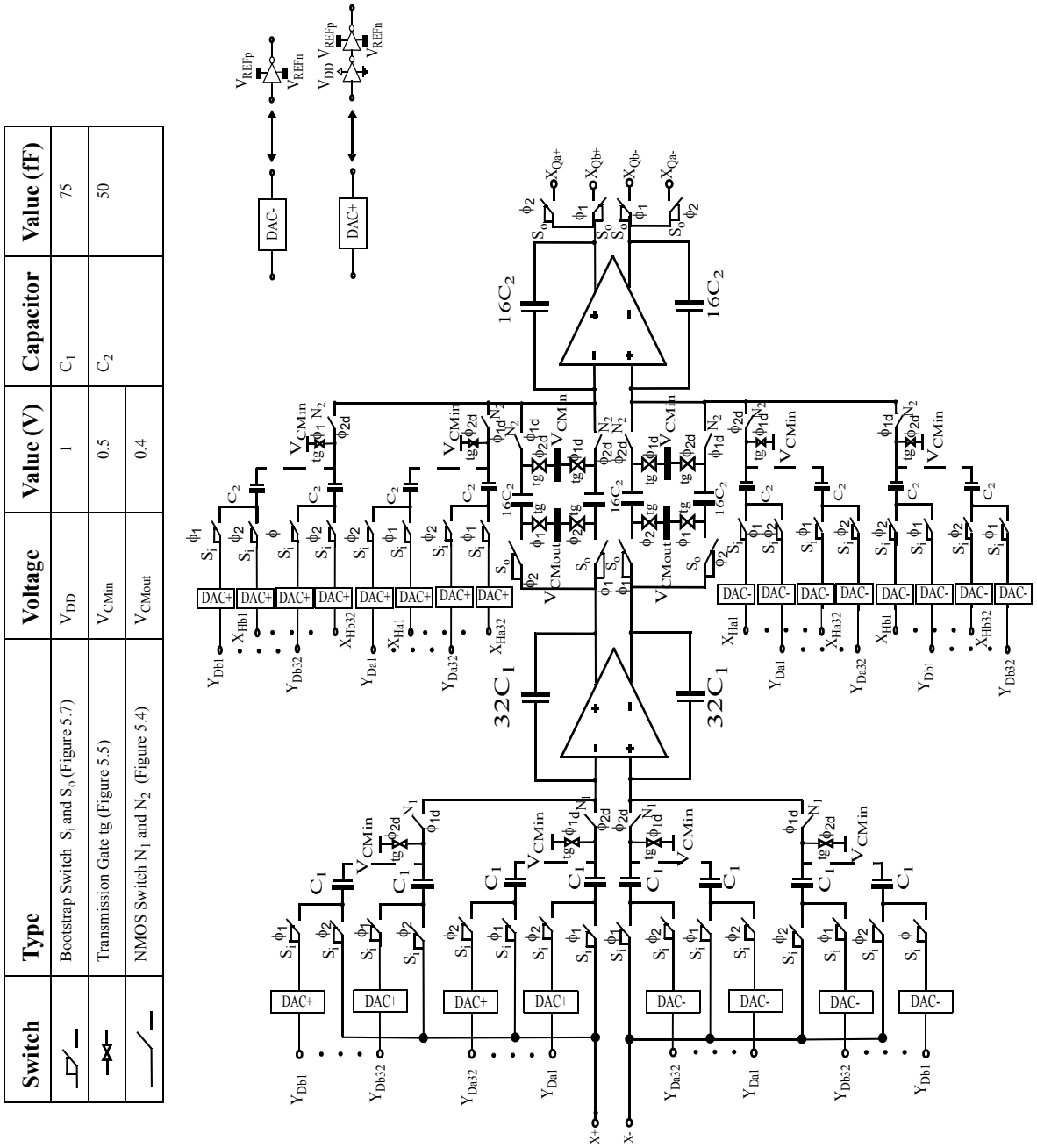

Figure 5.2 Fully-differential double-sampling SC implementation of the loopfilter of the ΔΣ modulator in Figure 5.1.

5.1 Switched-Capacitor Circuit

Figure 5.2 depicts the fully-differential double-sampling circuit implementation of the loopfilter of the $\Delta\Sigma$ modulator in Figure 5.1. Here, subscripts *a* and *b* are used to distinguish between the double-sampling paths.

To implement the 5-bit (32-level) DACs, the sampling capacitors of the 1st and 2nd integrators are divided into 32 unit capacitors C_1 and C_2, respectively. A $C_1 = 2.4\text{pf}/32 = 75\text{pf}$ is selected to meet the kT/C noise requirements (Section 4.2). The size of C_2 has a smaller contribution to the overall kT/C noise of the $\Delta\Sigma$ modulator. A $C_2 = 50\text{pf}$ is selected to save on power dissipation and circuit area, while ensuring adequate matching between the DAC unit capacitors.

5.2 Signal and Noise Transfer Functions

The $\Delta\Sigma$ modulator in Figure 5.1 has the following transfer functions and corresponding maximum instantaneous gains.*

- Signal transfer function from X to Y_{OUT} :

$$\mathrm{STF} = 1 \text{ and } |\mathrm{STF}|_{max} = 0 \text{ dB} \tag{5.1}$$

- Noise transfer function from Q to Y_{OUT} :

$$\mathrm{NTF} = (1 - z^{-1})^2 \text{ and } |\mathrm{NTF}|_{max} \cong 12 \text{ dB} \tag{5.2}$$

- Noise transfer function from Q_2 to Y_{OUT} :

$$\mathrm{NTF}_2 = 1 - z^{-2} \text{ and } |\mathrm{NTF}_2|_{max} \cong 6 \text{ dB} \tag{5.3}$$

To verify the functionality of the SC loopfilter in Figure 5.2, the $\Delta\Sigma$ modulator was simulated in SWITCAP using the SC loopfilter in Figure 5.1 and assuming ideal DACs. The magnitude responses of its transfer functions were then plotted in Figure 5.3. These simulated magnitude responses and their maximum instantaneous gains agree with the derived transfer functions in (5.1) - (5.3), thereby confirming the functionality of the SC loopfilter in Figure 5.2.

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*The maximum instantaneous gain $|\mathrm{TF}|_{max}$ of transfer function $\mathrm{TF}(z)$ is equal to the $1 - \mathrm{norm}||\mathrm{tf}||_1$ of the impluse sequence $\mathrm{tf}(n)$ for $\mathrm{TF}(z)$, where $||\mathrm{tf}||_1 = \sum_{n=0}^{\infty} |\mathrm{tf}(n)|$.

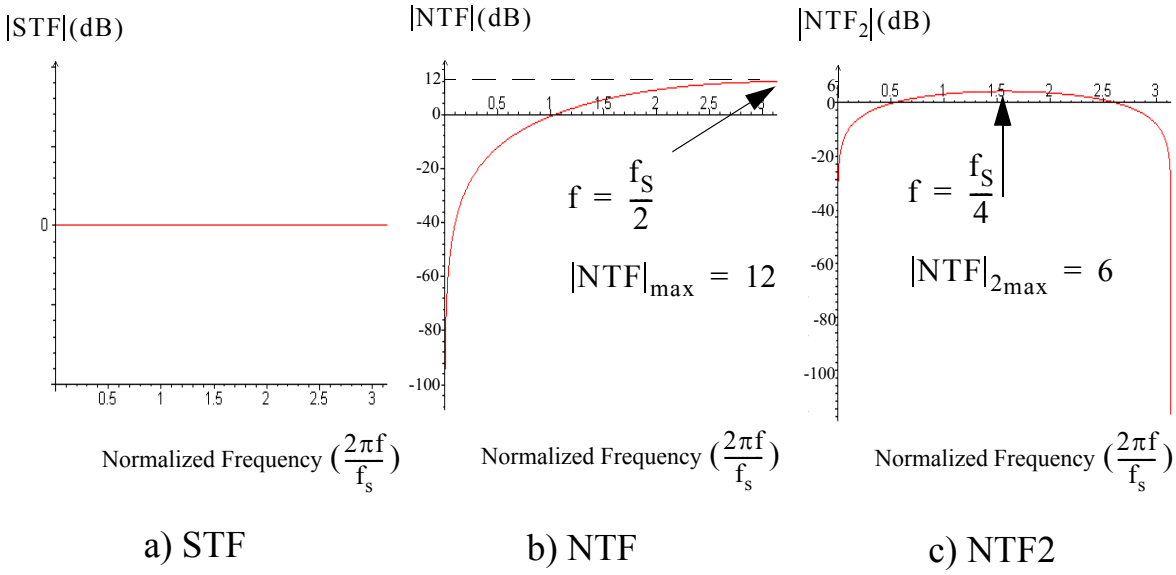


Figure 5.3 Magnitude responses of the transfer functions of the ΔΣ modulator in Figure 5.1, simulated in SWITCAP using the SC loopfilter in Figure 5.2 and assuming ideal DACs. a) signal transfer function from X to Y_{OUT}; b) noise transfer function from Q to Y_{OUT} ; and c) noise transfer function from Q_2 to Y_{OUT}.

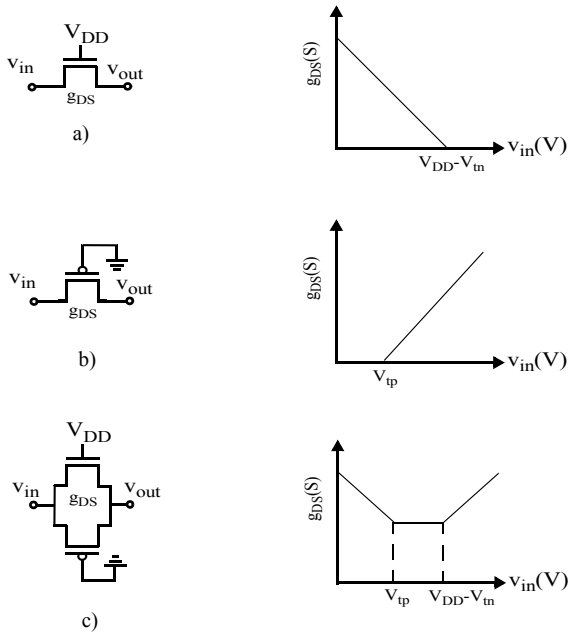


Figure 5.4 Conductance versus input-signal amplitude of a) NMOS switch; b) PMOS switch; and c) transmission gate [Abo, JSSC99].

5.3 Sampling Switches

The sampling switches can limit both the speed and resolution of an SC circuit. This section describes the sampling switches used in the design of the SC loopfilter in Figure 5.2.

5.3.1 MOS Switch

Figure 5.4 depicts the switch conductance g_{DS} versus the input-signal amplitude v_{IN} for NMOS and PMOS switches. The NMOS switch is on for $v_{\mathrm{IN}} < V_{DD} - V_{tn}$, while the PMOS switch is on for $v_{\mathrm{IN}} > V_{t\mathrm{p}}$. Sizing the NMOS and PMOS switches with $W_p / W_n \cong \mu_{\mathrm{n}} / \mu_{\mathrm{p}}$ and combining them to form a transmission gate (as shown in Figure 5.4c), results in a relatively constant conductance for $V_{t\mathrm{p}} < v_{\mathrm{IN}} < V_{DD} - V_{tn}$ [Abo, JSSC99]. Therefore, the input-signal swing in this constant-conductance region is limited to $V_{DD} - (V_{tn} + V_{tp})$. In low-voltage technologies, $V_{tn} + V_{tp}$ is comparable to V_{DD}, thereby limiting the input-signal swing. In 1-V

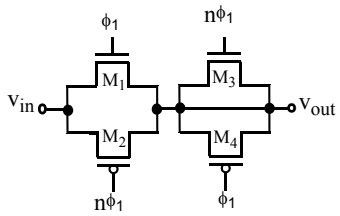


Figure 5.5 Transmission gate $M_{1\text{-}2}$, with dummy devices $M_{3\text{-}4}$ (with $W_3 = W_1/2$ and $W_4 = W_2/2$) to minimize charge-injection errors [Razavi 2001].

65-nm CMOS, $V_{tn} + V_{tp}$ is greater than 800 mV, which leaves less than 200 mV for input-signal swing. Hence, transmission gates are not suitable for full scale input signals and bootstrapped switches have to be used. However, transmission gates will be used to pass mid-rail voltages, such as the input and output common-mode voltages.

5.3.2 Transmission Gate

Figure 5.5 depicts the transmission gate structure used [Razavi 2001]. Devices M_1 and M_2 constitute the main transmission gate, while devices $M_{3\text{-}4}$ (with $W_3 = W_1/2$ and $W_4 = W_2/2$) act as dummy structures to minimize the charge-injection and clock-feedthrough errors. When $M_{1\text{-}2}$ turn off, $M_{3\text{-}4}$ turn on, thus absorbing the charge injected by $M_{1\text{-}2}$.

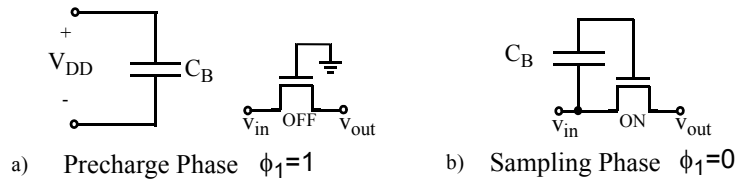


Figure 5.6 Conceptual diagram depicting the operation of a bootstrap switch during: a) precharge phase and b) sampling phase

5.3.3 Bootstrapped Switch

A conceptual diagram of the operation of a boostrapped switch is shown in Figure 5.6. During the precharge phase, a capacitor (C_B) is pre-charged to V_{DD}. During the sampling phase, this capacitor is then connected between the gate and source terminals of the bootstrapped switch. Thus, during the sampling phase, a bootstraped switch has a constant gate-to-source voltage v_{GS} and. hence, an approximately constant on resistance.

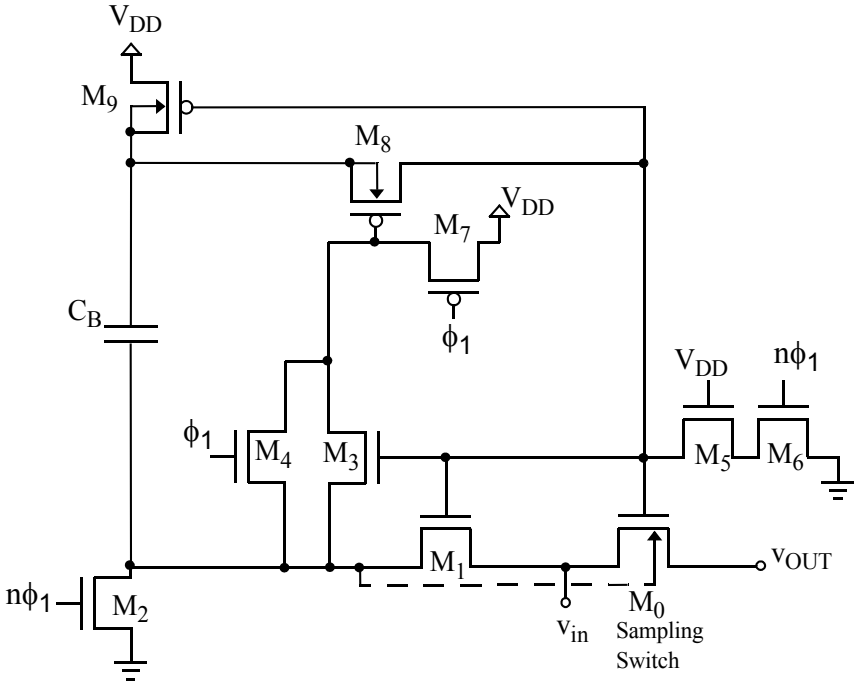


Figure 5.7 Circuit implementation of an NMOS bootstrapped switch [Dessouky, JSSCC01].

In the circuit implementation of the SC loopfilter in Figure 5.2, the bootstrapped switches are designed based on the circuit implementation proposed by [Dessouky, JSSCC01], as shown in Figure 5.7.

5.3.4 Switch Sizing

Table 5.1 summarizes the sizes of all the switches utilized in the SC loopfilter in Figure 5.2. To verify the achievable linearity using these switch sizes, the $\Delta\Sigma$ modulator in Figure 5.1 is simulated in SPECTRE using the SC loopfilter in Figure 5.2 and assuming ideal quantizers. Since the double-sampled loopfilter (Figure 5.2) has 2 output paths, its output time points were interleaved into one output sequence and a discrete Fourier transform is then performed to generate the output spectrum. For a 1.7-$V_{p\text{-}p}$ 480-khz sinusoidal input signal sampled at 200-Mhz, the output spectrum of the $\Delta\Sigma$ modulator has the 3rd harmonic 85 dB below the input-signal tone and a total harmonic distortion (upto the 7th harmonic) of -78 dB.

Bootstrapped Switch (Figure 5.7)	**C_B** (fF)	**W_0** (μm)	**W_1** (μm)	**W_2** (μm)	**W_3** (μm)	**W_4** (μm)	**W_5** (μm)	**W_6** (μm)	**W_7** (μm)	**W_8** (μm)	**W_9** (μm)
S_i	50	2	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12
S_o	500	20	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12

Transmission Gate (Figure 5.4)	**W_1** (μm)	**W_2** (μm)	**W_3** (μm)	**W_4** (μm)	**NMOS Switch**	**W_0** (μm)
tg	10	25	5	12	N_1	20
					N_2	10

Table 5.1 Sizes of the switches in the SC loopfilter in Figure 5.2 (L=60nm).

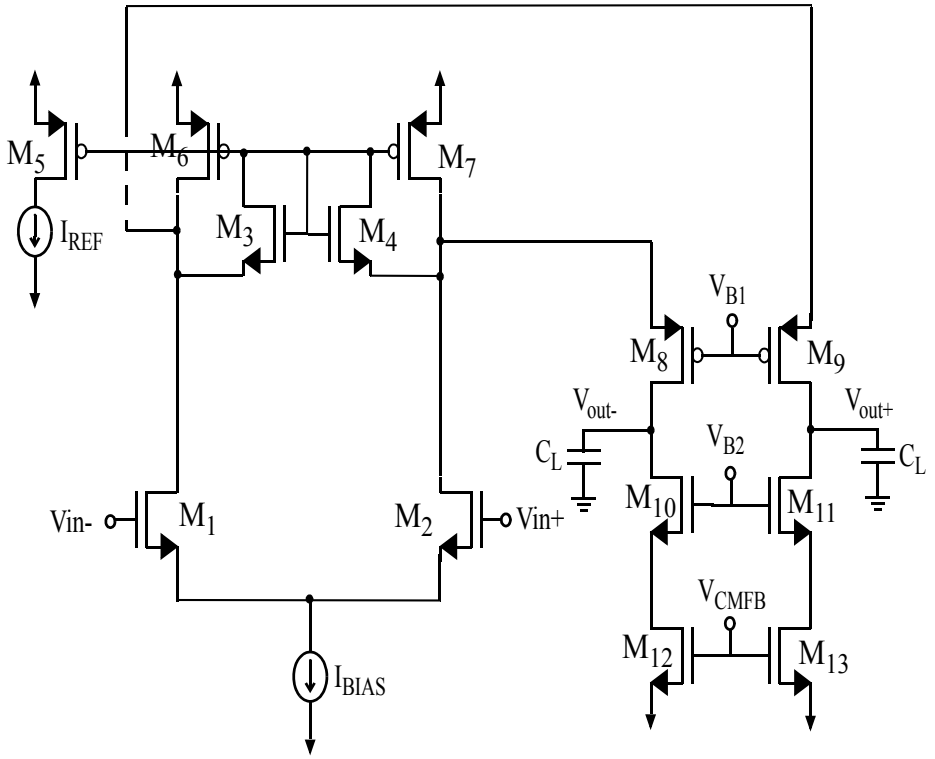


Figure 5.8 Folded cascode opamp. The CMFB circuit shown in Figure 5.9 controls the opamp's common-mode output voltage and provides the necessary compensation capacitors.

5.4 Operational Amplifier

5.4.1 Opamp and CMFB Circuits

The fully-differential opamps of the SC loopfilter of Figure 5.2 were designed using the folded-cascode opamp in Figure 5.8 [Johns 97]. Here, to improve the slewing behaviour the output cascode transistors are biased at the same current level as in the input-stage transistors [Johns 97]. To a first-order approximation (assuming a square-law MOSFET model with all transistors in saturation), the following expressions can be derived for the folded-cascode opamp in Figure 5.8 [Razavi 2001]:

- *Slew Rate :*

$$SR = \frac{I_{\text{BIAS}}}{C_L} \tag{5.4}$$

- *Output Resistance* :

$$R_{\text{OUT}} = (g_{m8,9} \cdot r_{o8,9} \cdot (r_{o6,7} /\!/ r_{o1,2})) /\!/ ((g_{m10,11} \cdot r_{o10,11} \cdot r_{o12,13})) \tag{5.5}$$

- *DC Gain* :

$$A_0 = g_{m1,2} \cdot R_{\text{OUT}} \tag{5.6}$$

- *Equivalent 1st Pole :*

$$\omega_{p1} = \frac{1}{R_{\text{OUT}} \cdot C_L} \tag{5.7}$$

- *Equivalent 2nd Pole* :

$$\omega_{p2} = \frac{g_{m8,9}}{C_{sb8,9} + C_{gs8,9} + C_{db1,2} + C_{db6,7}} \tag{5.8}$$

- *Unity Gain Frequency :*

$$\omega_t = \frac{g_{m1,2}}{C_L} \tag{5.9}$$

- *Phase Margin :*

$$PM = 90^{\circ} - arctan\left(\frac{\omega_t}{\omega_{p2}}\right) \tag{5.10}$$

- *Power Spectral Density of Input-Referred Thermal Noise :*

$$\overline{V^2_{\text{opamp, T}}}(f) = \frac{16 \cdot k \cdot T \cdot \gamma_T}{3} \cdot \left(\frac{1}{g_{m1,2}} + \frac{g_{m6,7}}{g^2_{m1,2}} + \frac{g_{m12,13}}{g^2_{m1,2}} \right) \tag{5.11}$$

- *Power Spectral Density of Input-Referred Flicker Noise :*

$$\overline{V^2_{\text{opamp, }\frac{1}{f}}}(f) = \frac{2}{C_{ox} f} \left(\frac{\gamma_{fn}}{W_{1,2} L_{1,2}} + \frac{\gamma_{fp}}{W_{6,7} L_{6,7}} \frac{g^2_{m6,7}}{g^2_{m1,2}} + \frac{\gamma_{fn}}{W_{12,13} L_{12,13}} \frac{g^2_{m12,13}}{g^2_{m1,2}} \right) \tag{5.12}$$

The SC common-mode-feedback (CMFB) circuit in Figure 5.9 [Senderowicz, JSSC82][Castello, JSSC85] was used to set the common-mode output voltages and provide load-compensation for the opamp in Figure 5.8. Here, capacitor C_C acts as a compensation capacitor, while capacitor C_R is a refreshing capacitor whose value is not critical to circuit performance and can be set smaller than C_C [Johns 97].

Tables 5.2 and 5.3 summarize the design parameters for the opamp and CMFB circuits used to realize the SC loopfilter in Figure 5.1. The corresponding opamp specifications are summarized in Table 5.4. These specifications meet the targeted opamp specifications in Table 4.1, imposed by the noise budget in Section 4.2.

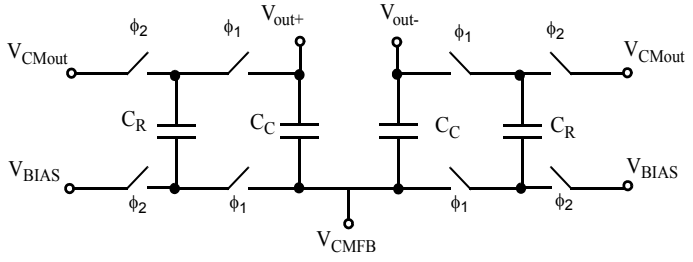


Figure 5.9 SC common mode feedback (CMFB) circuit.

Design Parameter	**1st Opamp**	**2nd Opamp**
W_{1-2}	50 µm	50 µm
W_{3-4}	1 µm	1 µm
W_{5-6}	3 µm	3 µm
W_{7}	30 µm	30 µm
W_{8-9}	60 µm	80 µm
W_{10-11}	45 µm	10 µm
W_{12}	20 µm	20 µm
W_{13}	20 µm	20 µm
L_{1-13}	0.18 µm	0.18 µm
I_{BIAS}	550 µA	250 µA
I_{REF}	55 µA	25 µA
V_{B1}	400 mV	590 mV
V_{B2}	580 mV	690 mV
C_L	2.7pF	1.5 pF

Table 5.2 Design parameters for the opamps (Figure 5.8) used in the SC loopfilter in Figure 5.2.

	C_C (fF)	C_R (fF)	V_{CMout} (V)	V_{BIAS} (V)
1st Opamp	400	100	0.40	0.47
2nd Opamp	200	100	0.43	0.39

Table 5.3 Design parameters for the CMFB circuits (Figure 5.9) used in the opamps (Figure 5.1) of the SC loopfilter in Figure 5.2.

Specification	1st Opamp	2nd Opamp
Short circuit transconductance ($g_{m1,2}$)	3.9m A/V	1.7m A/V
Output Swing	450 mV_{p-p}	430 mV_{p-p}
DC gain (A_ϕ)	125 V/V	175 V/V
Unity gain frequency (f_t)	239 MHz	180 MHz
Slew Rate (SR)	120 V/μs	80 V/μs
Phase Margin (PM)	77°	82°
Feedback Factor (β)	0.5	0.25
Input referred thermal noise PSD $\overline{V^2_{opamp,T}}(f)$	$1 \times 10^{-16} V^2/Hz$	$1.7 \times 10^{-16} V^2/Hz$
Power Dissipation	1.5 mW	0.66 mW
Technology	1-V 65-nm CMOS	

Table 5.4 Opamp circuit specifications achieved using the design parameters in Tables 5.2 and 5.3.

In the opamp designs, the following special measures were taken to meet the targeted specifications:

1. The length of the transistors were adjusted to 180 nm,which is 3 times the minimum feature size (60 nm). The primary reason for this choice was to be able to get a DC gain A_ϕ of around 40 dB. Another advantage of this choice is that it reduces the flicker noise contribution from each transistor, as evident from equation (5.13).
2. Due to the low supply voltage (1 V), the input transistors $M_{1\text{-}2}$ are operating in weak inversion with $v_{GS} < V_t$, where v_{GS} is the gate-source voltage and V_t is the threshold voltage. However, to make $M_{1\text{-}2}$ operate at a v_{GS} of about 50 mV below the strong/weak inversion boundary ($v_{GS} = V_t$), the bulk of $M_{1\text{-}2}$ is biased at around 500 mV to lower V_t and make it comparable to v_{GS} [Adachi, VLSI06][Kinget, EDSSC05].

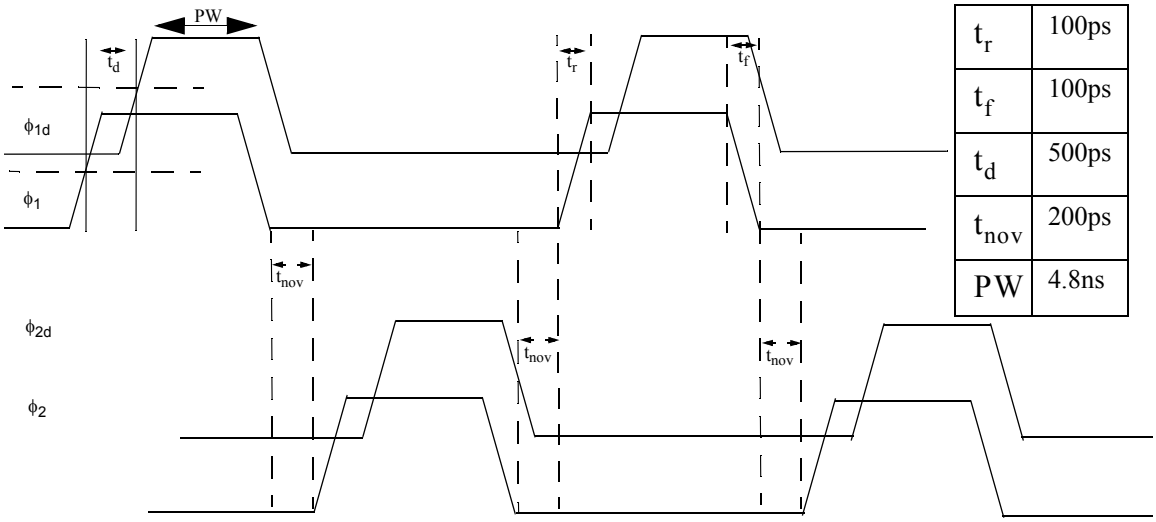


Figure 5.10 Two phase non-overlapping clocking scheme.

5.5 Clocking Scheme

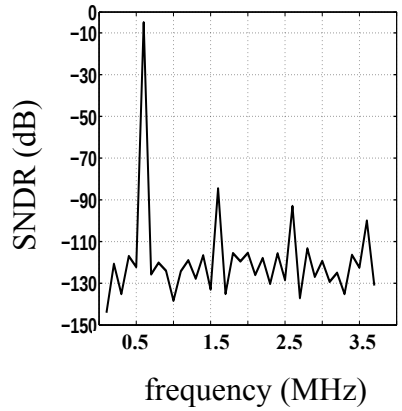
A two phase non-overlapping clocking scheme (Figure 5.10) is used in the simulations of the SC loopfilter (Figure 5.2). Delayed versions of ϕ_1 and ϕ_2 are generated to minimize charge-injection errors [Johns 97].

Clock Frequency	100 MHz
Effective Sampling Frequency (f_s)	200 MHz
Signal Bandwidth	2.8 MHz
Maximum Input Signal	1.7 V_{p-p}
THD @ f_{in} = 2.8MHz	-73.5 dB
THD @ f_{in} = 2.2MHz	-75.3 dB
THD @ f_{in} = 480KHz	-78.1 dB
Oversampling ratio (OSR)	35
Power Consumption	3 mW
Technology	1-V CMOS 65 nm

Table 5.5 Performance Summary

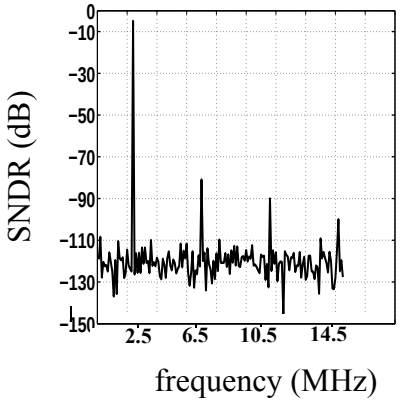
5.6 Simulation Results

To test the achievable linearity using the designed opamps (Table 5.4), the $\Delta\Sigma$ modulator (Figure 5.1) is simulated in SPECTRE using the SC loopfilter in Figure 5.2. and assuming ideal quantizers. Since the double-sampled loopfilter (Figure 5.2) has 2 output paths, its output time points were interleaved into one output sequence and discrete Fourier transform is then performed to generate the output spectrum. For a 1.7-V_{p-p} sinusoidal input signal sampled at 200-MHz, the output spectrum of the $\Delta\Sigma$ modulator is plotted in Figure 5.11 for various input frequencies f_{in}. Accordingly for $f_{in} \le 2.8$ MHz, the $\Delta\Sigma$ modulator can achieve a total harmonic distortion (up to the 7^{th} harmonic) of THD = -73.5 dB, which is equivalent to the targeted 12-bit linearity.



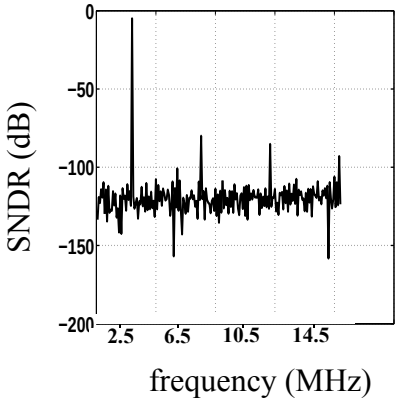
Harmonic #	Power (dB)
3rd	-84.6
5th	-93.0
7th	-100.0
THD	-78.1

a) f_{in}= 480 KHz



Harmonic #	Power (dB)
3rd	-81.0
5th	-90.0
7th	-100.0
THD	-75.3

b) f_{in}= 2.25 MHz



Harmonic #	Power (dB)
3rd	-80.0
5th	-85.2
7th	-93.0
THD	-73.5

c) f_{in}= 2.8 MHz

Figure 5.11 Output spectrum of the ΔΣ modulator for different input frequencies: a)f_{in} = 480KHz b)f_{in} = 2.25MHz c)f_{in} = 2.8MHz

Chapter 6

SUMMARY

The design of analog-to-digital converters (ADCs) has become more challenging due to several factors. These mainly include the demanding requirements imposed by modern broadband digital communication applications. Examples include high-speed wired communication services such as ADSL [Conroy, ISSCC99]. High-speed and high-resolution ADCs are critical to meet those communication standards. Low-power operation is also critical for portable applications. In addition to that, these ADCs must be built in standard digital CMOS processes for higher system integration and lower fabrication costs [Hamoui 04]. This thesis presented the design of a discrete-time $\Delta\Sigma$ modulator with digital feedforward (DFF) using double-sampled switched-capacitor (SC) circuits with 12-bit resolution and over 2- MHz bandwidth in a 1-V 65-nm CMOS technology. Two special design techniques were used to acheive a high-speed high-resolution A/D conversion at a moderate power consumption:

1) **double sampling**: this is a low-power design technique which effectively doubles the sampling frequency of SC integrators without increasing their clock frequency. The idea here is that, during the sampling phase of an SC integrator, the opamp is idle. Therefore, to optimize circuit usage at seemingly the same power consumption, the opamp is used in the sampling phase to integrate a charge stored previously on a different set of capacitors.

2) **input digital feedforward**: this involves the addition of the input signal after the quantizer in the digital domain. Consequently the analog integrators in the $\Delta\Sigma$ loop-filter only process shaped quantization noise and, hence, their output signal swing is reduced [Hamoui, ISCAS008], thereby enabling the implementation of the $\Delta\Sigma$ loop-filter in a low-voltage technology.

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