An Architecture for Multibit Log-Domain Delta-Sigma Modulators and Low-Power CMOS Implementation Targeting 10-12 bit Resolution

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August 2014

A thesis submitted to McGill University in partial fulfilment of the requirements for the degree of Doctor of Philosophy.

Abstract

BIOPOTENTIAL SENSORY INTERFACES IN biomedical devices require high-resolution analog-to-digital converters (ADCs) operating at low-to-medium speeds. Additionally, the low-power and low-supply voltage requirements of such systems are critical and are increasingly stringent. Low-power operation is necessary in order to increase the battery life of implantable devices. Lowering of supply voltages is driven by the increasing reliance on digital processing in computationally-extensive implantable and portable biomedical devices; as supply voltages are lowered, digital power consumption is reduced. Moreover, to extend the battery life, these devices must be capable of operating from supply voltages ranging from the nominal VDD down to the end-of-life (EOL) battery voltage.

This thesis explores new techniques for the design of low-power low-voltage ADCs for high-resolution biomedical signal acquisition in portable devices. Subthreshold circuit design techniques, and in particular log-domain circuit techniques in $\Delta\Sigma$ modulators, are utilized to realize these design objectives. Specifically, this work investigates the following:

1. Multibit Log-Domain $\Delta\Sigma$ Modulators: Previously reported log-domain $\Delta\Sigma$ modulators were limited to 1-bit quantization and hence could not benefit from the advan-

tages associated with multibit quantization (namely, reduced in-band quantization noise, and increased modulator stability). This thesis explores the challenges of multibit quantization and digital-to-analog conversion in the log-domain, and presents a novel multibit log-domain $\Delta\Sigma$ modulator, practical for CMOS implementation. It demonstrates the equivalence of the designed system to classical, internally-linear modulators. Furthermore, SIMULINK models of log-domain $\Delta\Sigma$ modulator circuits are proposed, and the effects of various circuit non-idealities on the performance of the proposed multibit log-domain $\Delta\Sigma$ modulator architecture are investigated.

2. Low-Distortion Low-Noise Loop-Filter Circuit Implementation: The realization of log-domain $\Delta\Sigma$ modulators targeting high-resolution applications necessitates a minimization of distortion and noise in the log-domain loop-filter. In this work, low-distortion log-domain circuit blocks are presented. Furthermore, the design trends of log-domain circuits are investigated and a noise-optimization method is proposed to meet the targeted high-resolution performance while maintaining low-power operation. The necessity of the low-distortion log-domain circuits and the design tradeoffs are validated through circuit-level simulations. Additionally, a low-noise current output DAC is proposed for the log-domain $\Delta\Sigma$ modulator. A class AB multibit log-domain $\Delta\Sigma$ modulator prototype was designed and fabricated in 0.13 μm CMOS technology. In simulation, the proposed modulator achieves 10.47-bit signal-to-noise-and-distortion-ratio (SNDR) over a 10 kHz bandwidth with a 0.84 V_{pp} differential signal input, while operating from a 0.8 V supply and consuming a total power of 46.7 μW. Results of the fabricated prototype indicate dc-bias instability within the $\Delta\Sigma$ modulator's integrator outputs and, through testing of individual components, validates the operation of various circuits within the modulator.

By proposing a novel multibit log-domain $\Delta\Sigma$ modulator architecture and low-distortion log-domain circuits, and by presenting the first class AB implementation of log-domain $\Delta\Sigma$ modulators, the presented modulator achieves low-power high-resolution operation at aggressively low supply voltages and with one of the largest reported input-signal-swing to

supply-voltage ratios. Furthermore, by presenting an optimization procedure for the various design parameters involved, this work aims at easing the incorporation of log-domain circuit techniques in $\Delta\Sigma$ modulator applications.

Résumé

Les interfaces sensorielles biopotentielles en dispositifs biomédicaux ont besoin de convertisseurs analogique-numérique (CAN) à haute résolution fonctionnant à faibles moyennes vitesses. En outre, les exigences de faible puissance et de basse tension d'alimentation de ces systèmes sont essentielles et sont de plus en plus strictes. Le fonctionnement à faible puissance est nécessaire pour augmenter la durée de vie des batteries des dispositifs implantables. L'abaissement de la tension d'alimentation est entraîné par l'utilisation croissante de traitement numérique dans les dispositifs implantables à calculs extensives et les dispositifs biomédicaux portables; que les tensions d'alimentation sont abaissés, la consommation électrique numérique est réduite. De plus, pour prolonger la vie des batteries, ces dispositifs doivent être capables de fonctionner à des tensions d'alimentation allant de la tension nominale VDD jusqu'à la tension de fin de vie (EOL) de la batterie.

Cette thèse explore de nouvelles techniques pour la conception de CAN à faible puissance, à basse tension, et à haute résolution pour l'acquisition des signaux biomédicaux dans les dispositifs portables. Des techniques de conception de circuits infraliminaires, et en particulier les techniques de circuits en domaine log (log-domain) dans les modulateurs

$\Delta\Sigma$, sont utilisés pour réaliser ces objectifs de conception. Plus précisément, ce travail explore ce qui suit:

1. Les modulateurs $\Delta\Sigma$ multibit en domaine log (log-domain): Les modulateurs $\Delta\Sigma$ en domaine log précédemment rapportés ont été limitées à une quantification d'1-bit et, par conséquent, ne pouvaient pas bénéficier des avantages liés à la quantification multibit (à savoir, la réduction de bruit de quantification intra bande, et l'augmentation de stabilité du modulateur). Cette thèse explore les défis de la quantification multibit et de la conversion numérique-analogique en domaine log, et présente un nouveau modulateur $\Delta\Sigma$ multibit en domaine log qui est pratique pour la realisation CMOS. Il démontre l'équivalence du système conu pour les modulateurs classiques intérieurement linéaires. De plus, des modèles Simulink pour les circuits du modulateur $\Delta\Sigma$ en domaine log sont proposés, et les effets des non-idéalités divers de circuit sur la performance de l'architecture du modulateur $\Delta\Sigma$ multibit en domaine log sont étudiées.

2. La réalisation du circuit du filtre de boucle à faible distorsion et à faible bruit: La réalisation des modulateurs $\Delta\Sigma$ en domaine log ciblant des applications à haute résolution nécessite la minimisation de la distorsion et du bruit dans le filtre de boucle en domaine log. Dans ce travail, des blocs de circuits en domaine log à faible distorsion sont presentés. En outre, les tendances de conception de circuits log-domain sont examinées et une méthode d'optimisation du bruit est proposée pour répondre à l'objectif de rendement à haute résolution tout en conservant fonctionnement à faible puissance. La nécessité des circuits log-domain à faible distorsion et les compromis de conception sont validés par des simulations au niveau du circuit. En outre, un convertisseur numérique-analogique (CNA) de sortie à courant ayant faible bruit est proposé pour le modulateur $\Delta\Sigma$ en log-domain. Un prototype du modulateur $\Delta\Sigma$ multibit de classe AB en domaine log a été conu et fabriqué en 0,13 μm technologie CMOS. Dans la simulation, le modulateur proposée atteint 10.47-bit de rapport signal-sur-bruit-et-distorsion (SNDR) sur une largeur de bande de 10 kHz avec un signal d'entrée différentiel de 0,84 V_{pp}, tout en fonctionnant à partir d'une alimentation

de 0,8 V et en consommant une puissance totale de 46.7 μW. Les résultats du prototype fabriqué indiquent l'instabilité du biais dc dans les sorties des intégrateurs du modulateur $\Delta\Sigma$, et, au moyen des tests des composants individuels, valident le fonctionnement des différents circuits à l'intérieur du modulateur.

En proposant une nouvelle architecture du modulateur $\Delta\Sigma$ multibit en domaine log et des circuits en domaine log à faible distorsion, et en présentant la premire mise en oeuvre de modulateurs $\Delta\Sigma$ de classe AB en domaine log, le modulateur présenté foctionne à faible puissance et à haute résolution et à partir de tensions agressivement faibles et avec un des plus grands rapports d'excursion de signal d'entrée sur tension d'alimentation rapportés. Par ailleurs, en présentant une procédure d'optimisation pour les paramètres de conception divers, ce travail vise à faciliter l'intégration des techniques de circuit en domaine log dans les applications de modulateur $\Delta\Sigma$.

Acknowledgements

This dissertation would not have been possible without the guidance and assistance of many who have imparted their knowledge and supported me through the years.

Foremost, I wish to express my sincere gratitude to my supervisors - The late Prof. Anas Hamoui, who shared his guidance with me in the early stages when the ideas in this dissertation were being developed; Prof. Yvon Savaria, who was with me throughout and provided me with a wealth of technical and industry experience; and Prof. Fabrice Labeau, who stepped in under unfortunate circumstances to guide me through the last stages. Their assistance and guidance have enabled me to overcome the many challenges encountered in the course of this dissertation.

I also wish to extend my deep thanks to Prof. Gordon Roberts and Prof. Thomas Szkopek, who were on my proposal committee, and provided me with invaluable feedback and advice towards the completion of this dissertation.

I would like to sincerely thank the many Professors at McGill who have shared with me their knowledge through the years - Prof. Mourad El-Gamal, who supervised and guided me through my Masters degree; and Professors Nicolas Rumin and Roni Khazaka, who

also imparted their knowledge.

I would like to express my very great appreciation to my lab colleagues through the years - Phil Chopp, Mostafa Nashaat, Mohamed Taherzadeh-Sani, Mohammad Al-Ghamdi, Pavel Peev, Aniroodh Mehta, Mohamed Sukhon, and Furrookh Sibtain, for their advice and companionship.

I am particularly grateful to the ECE system administrators, technicians, and the Graduate Office staff at McGill university who have assisted me through the years. I wish to extend my appreciation to the staff and technicians at École Polytechnique de Montréal for their assistance. I also wish to extend my thanks to the support staff at CMC, who have provided me with much assistance. This work was supported in part by the Fonds Québécois de la Recherche sur la Nature et les Technologies (FQRNT) and by Le Regroupement Stratégique en Microsystèmes du Québec (ReSMiQ). My sincere thanks go out to them.

I wish to thank all of my friends for their support and encouragement over the past few years.

I am indebted to my father Abdalla, my mother Somaya, and my brother and dearest friend Khaled, for the wisdom they've imparted, and their love and encouragement through the years. I owe them more than words can describe.

I would like to thank my sons Daoud and Ayoub, whose smiles fill my heart and push me on, although they may not yet know it.

Finally, I would like to thank my wife and soulmate Noha, Without her love, encouragement, and support, this dissertation would not have been completed.

Preface & Contribution of Authors

THE MAIN IDEAS PRESENTED IN THIS THESIS are the author's. The author was mainly responsible for the concept development, derivations, design, and testing.

Prof. Yvon Savaria and Prof. Anas Hamoui contributed to this work through discussions and review of designs and reports. After Prof. Hamoui's passing in 2011, Prof. Fabrice Labeau contributed to the work through editorial discussions and reviews.

The key contributions of this thesis are:

- At the architecture-level, the first multibit log-domain $\Delta\Sigma$ modulator is proposed, and behavioural models are developed to investigate the performance of the modulator and several key non-idealities [Sha14b].
- At the circuit-level, a low-distortion class AB log-domain loop-filter is developed to realize high-resolution ($>$ 10-bit) performance through modifications to previous circuits and the development of new ones.
- The design tradeoffs of log-domain circuits are derived, and an optimization technique for the selection of a log-domain loop-filter's various design parameters is proposed.

- A novel current-output DAC is proposed to achieve low-noise performance in the log-domain $\Delta\Sigma$ modulator feedback path [Sha14a].

- The proposed techniques are employed in the design of a low-power ($< 50\ \mu$W) low-voltage (0.8 V) $\Delta\Sigma$ modulator CMOS implementation targeting the 10-12 bit resolution range.

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CHAPTER 1

Introduction

1.1 Motivation

DESPITE THE increasing reliance on digital signal processing in electronics, much of the signals that individuals encounter on a daily basis, and that are generated in biological systems, are analog. Therefore analog-to-digital conversion remains essential for interfacing the analog world, and digital signal processors in electronic devices. Figure 1.1 demonstrates the general structure of a portable biomedical system.

Analog-to-Digital Converters (ADCs) targeting biopotential sensory interfaces in biomedical devices require varying design specifications, dependent on the nature of the biopotential signals of interest. Table 1.1 summarizes the varying specifications of analog-to-digital converters targeting biomedical applications. Attempts to improve the resolution of even well-established applications continue: in hearing-aids and cochlear implants, increasing

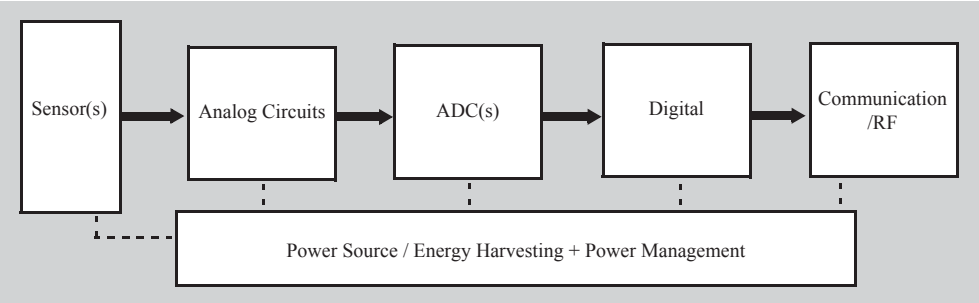


Figure 1.1: Block-diagram of a typical portable biomedical system.

Table 1.1: General specifications for various biopotential acquisition devices [Cha08].

Application	Biopotential-signal Bandwidth	Device Power	ADC Resolution
Pacemakers	500 Hz	$< 10\,\mu$W	8 bits
Hearing aids	8 kHz	100 - 2000 μW	12 bits
Neural recording	50 kHz	1 - 10 mW	8 bits - Multiple channels
Body-area monitoring	500 Hz	140 μW	12 bits

ADC resolutions have the potential for patients to move beyond hearing conversations to appreciating music.

In biopotential sensory interfaces, the low-power and low-supply voltage requirements are critical and are increasingly stringent. Low-power operation is necessary in order to increase the battery life of implantable devices. Lowering of supply voltages is driven by the increasing reliance on digital processing. Figure 1.2 demonstrates the projection of CMOS supply voltages, as reported by the International Technology Roadmap for Semiconductors (ITRS) in 2013, predicting supply voltages of 0.75 V by 2020, and 0.64 V by 2030. The lowering of supply voltages poses a particular challenge to analog and mixed-signal designers, as the design of analog circuits becomes increasingly challenging with decreasing supply voltages. Developing innovative low-power low-voltage techniques in the design of ADCs will address the challenge facing full system-on-chip integration.

Subthreshold circuit-design has gained increasing attention as a useful low-power low-voltage design technique, due to the maximization of transconductance-efficiency and the

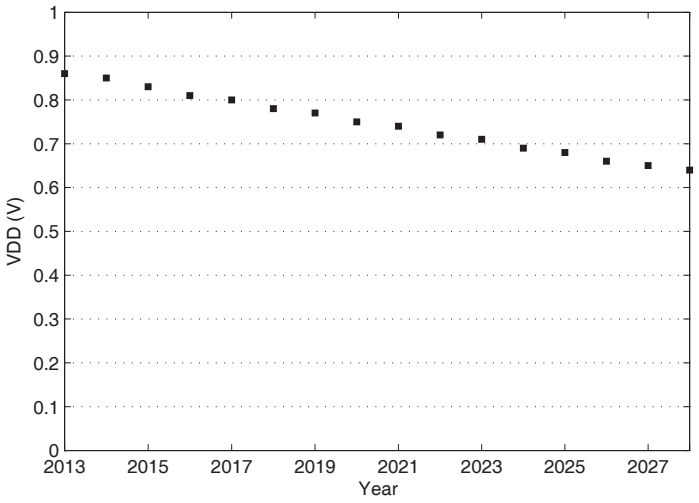


Figure 1.2: Projection of CMOS supply voltages, as reported by the International Technology Roadmap for Semiconductors (ITRS).

lowering of supply-voltage requirements in the CMOS weak-inversion region [Sar10] [Cha08]. Additionally, log-domain design techniques - which employ weak-inversion devices to realize logarithmic compression at the input and exponential expansion at the output - result in the lowering of internal signal swings and further easing of low-voltage design. Log-domain circuits have recently emerged in the design of Delta-Sigma ($\Delta\Sigma$) ADCs [Ser02] [Red07].

Despite their low-power low-voltage advantage, several challenges limit the use of log-domain circuits in the realization of high-resolution $\Delta\Sigma$ ADCs:

- So far, only single-bit (with a 1-bit internal quantizer) log-domain $\Delta\Sigma$ modulator architectures have been proposed [Ser02] [Red07]. The lack of multibit quantization hinders the achievable resolution in $\Delta\Sigma$ modulators; increased number of quantization-bits improves the resolution by lowering the quantization error, and by improving the stability of $\Delta\Sigma$ modulator loop-filters. If log-domain circuits are to be employed in high-resolution ($>$ 10-bit) $\Delta\Sigma$ ADCs, a multibit log-domain $\Delta\Sigma$ architecture must be developed at the architecture-level.

- Compared to their active RC and Gm-C counterparts, log-domain integrators are

more prone to linearity issues stemming from second-order CMOS non-idealities [Ort06]. Accordingly, at the circuit-level, low-distortion analog circuits are needed to enable the realization of high-resolution log-domain $\Delta\Sigma$ modulators.

- The realization of log-domain $\Delta\Sigma$ ADCs involves balancing several design factors. In order to arrive at an optimum performance for a targeted design criterion, an optimization procedure is required to assist designers.

1.2 Thesis Contributions

This thesis will explore and propose techniques for the realization of high-resolution multibit log-domain $\Delta\Sigma$ modulators. The target specification of these circuits was derived from requirements of biomedical applications. Specifically, the key contributions of this thesis are:

- At the architecture-level (Chapter 4), the first multibit log-domain $\Delta\Sigma$ modulator is proposed, and behavioural models are developed to investigate the performance of the modulator and several key non-idealities [Sha14b].

- At the circuit-level (Chapter 5), a low-distortion class AB log-domain loop-filter is developed to realize high-resolution ($>$ 10-bit) performance through modifications to previous circuits and the development of new ones [Sha14b].

- The design tradeoffs of log-domain circuits are derived, and an optimization technique for the selection of a log-domain loop-filter's various design parameters is proposed (Chapter 5).

- A novel current-output DAC is proposed (Chapter 6) to achieve low-noise performance in the log-domain $\Delta\Sigma$ modulator feedback path [Sha14a].

- The proposed techniques are employed in the design of a low-power ($<$ 50 μW)

low-voltage (0.8 V) $\Delta\Sigma$ modulator CMOS implementation targeting the 10-12 bit resolution range (Chapter 7).

The $\Delta\Sigma$ modulator was fabricated in 0.13 μm CMOS technology. Results of the fabricated prototype indicate proper operation of several of the presented circuits, and indicate that differential mismatch in Class AB log-domain loop-filters results in instability in the targeted log-domain $\Delta\Sigma$ modulator. Circuit-level and behavioural simulations indicate an expected signal-to-noise-and-distortion-ratio (SNDR) performance of 10.47-bit over a 10 kHz bandwidth with a 0.84 V_{pp} differential signal input, while operating from a 0.8 V supply and consuming a total power of 46.7 μW.

Segments of this research have been published in:

[1] M. A. Shaheen, Y. Savaria, and A. A. Hamoui. Design and modeling of high- resolution multibit log-domain $\Delta\Sigma$ modulators, in *Journal of Analog Integrated Circuits and Signal Processing*, vol. 79, no. 3, pp. 569-582, June 2014.

[2] M. A. Shaheen, A. A. Hamoui, and Y. Savaria. A current-output DAC for low-power low-noise log-domain $\Delta\Sigma$ modulators, in *Proc. IEEE NEWCAS Conference*, June 2014, pp. 281-284.

1.3 Thesis Outline

The next two chapters provide an overview of the thesis background, while later chapters discuss the architecture and circuit-level design of the proposed modulator, and the CMOS implementation. Specifically, this thesis is organized as follows:

- Chapter 2 provides a brief background on analog-to-digital conversion for biopotential signal acquisition and discusses the suitability of $\Delta\Sigma$ modulators for high-resolution applications. The fundamentals of $\Delta\Sigma$ modulators are introduced and a literature review of low-power low-voltage techniques employed in the design of $\Delta\Sigma$ modulators targeting biomedical applications is presented.

- Chapter 3 introduces the fundamentals of log-domain circuit design, provides a brief overview of the development of log-domain circuits in prior literature, and describes design challenges in the design of log-domain circuits.

- Chapter 4 presents an analysis of quantization and digital-to-analog conversion in the log-domain, and demonstrates the challenges in implementing multibit log-domain $\Delta\Sigma$ modulators. A novel multibit log-domain $\Delta\Sigma$ modulator architecture suitable for high-resolution applications and practically implementable in CMOS is proposed. Behavioural modeling of the proposed modulator is presented, including several key non-idealities. The effects of the non-idealities on the performance of the proposed modulator are explored.

- Chapter 5 presents the circuit-level realization of the proposed modulator's loop-filter, and demonstrates low-distortion log-domain analog blocks to enable the design of higher-resolution log-domain $\Delta\Sigma$ modulators. The chapter explores the design tradeoffs of log-domain $\Delta\Sigma$ modulators and proposes an optimization procedure for log-domain loop-filters. The chapter concludes with circuit-level simulations of the proposed loop-filter, and simulations validating the design tradeoffs and the low-distortion advantage of the presented circuits.

- Chapter 6 presents a novel low-noise current-output DAC suitable for incorporation in multibit log-domain $\Delta\Sigma$ modulators.

- Chapter 7 presents the implementation of a 3^{rd}-order 3-bit log-domain $\Delta\Sigma$ modulator targeting the 10-12 bit resolution range and the 10 kHz bandwidth range. The layout of the fabricated prototype, and the results of the fabricated prototype are demonstrated.

- Chapter 8 concludes the thesis with an overview of the thesis contributions, and suggestions for future research.

CHAPTER 2

Overview of ADCs for Biomedical Signal Acquisition

DUE TO the varying characteristics of biopotential signal types, the range of biopotential signal frequencies and amplitudes that need to be processed can vary considerably [Goe05]. Additionally, the ADC resolution and power requirements for processing such signals can also vary considerably [Cha08]. Since the presented work will target high-resolution portable applications, the choice of ADC architecture is paramount to the realization of the design targets.

Section 2.1 discusses two of the most prevalent architectures in the implementation of ADCs for biomedical applications, and outlines why $\Delta\Sigma$ ADCs are the preferred choice for low-bandwidth high-resolution applications. Section 2.2 reviews the basics of $\Delta\Sigma$ modulators. Section 2.3 compares continuous-time and discrete-time $\Delta\Sigma$ modulator implemen-

tations, and argues that continuous-time implementations are more suitable for the targeted application. Finally, Section 2.4 reviews techniques presented in prior literature to realize low-power low-voltage $\Delta\Sigma$ ADCs targeting biomedical applications.

2.1 Delta-Sigma ADCs vs. SAR ADCs

Figure 2.1 illustrates the resolution and conversion-frequency ranges for selected ADCs. As illustrated, successive-approximation-register (SAR) ADCs and delta-sigma ($\Delta\Sigma$) modulators are widely used in the implementation of ADCs for portable biomedical applications.

Successive-approximation-register ADCs (Fig. 2.2) perform a binary search algorithm to determine the closest digital equivalent to the input signal [Joh97], requiring m steps in order to perform an m-bit conversion. Due to their low circuit complexity, SAR ADCs can achieve high power efficiency.

Delta-Sigma modulators (Fig. 2.3) also offer an attractive option for the design of low-power high-resolution ADCs. Through oversampling and noise shaping they can achieve high-resolution conversions using a low-resolution ADC. Combined with relaxed linearity of the integrators used, this makes $\Delta\Sigma$ modulators highly power efficient [Cha08].

Although SAR ADCs are highly power efficient, for high resolution analog-to-digital conversions, SAR ADCs necessitate the use of larger capacitor ratios, resulting in increased power dissipation [Mat08]. As shown in Fig. 2.1, SAR ADCs are prevalent for medical application resolutions below 10 bits. At resolutions exceeding 10-12 bits, $\Delta\Sigma$ ADCs are more widely used for medical applications. A drawback of $\Delta\Sigma$ implementations is the reliance on high oversampling ratios to realize high resolutions; at high bandwidths this can become a severe challenge in implementing low-power designs due to the need to operate at very high sampling frequencies. However, the signal bandwidth for most medical applications does not exceed a few kHz, alleviating the need to drive the converter at high sampling frequencies.

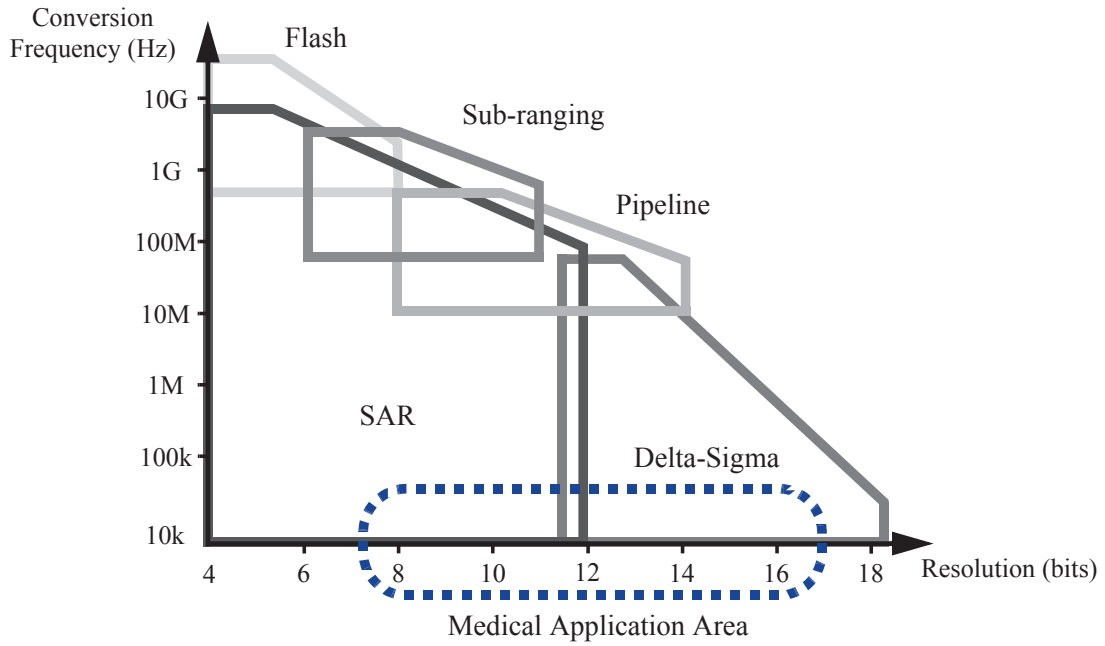


Figure 2.1: Operating regions for selected ADCs and medical application region [Matsuzawa, ISSCC10 Forum Presentations].

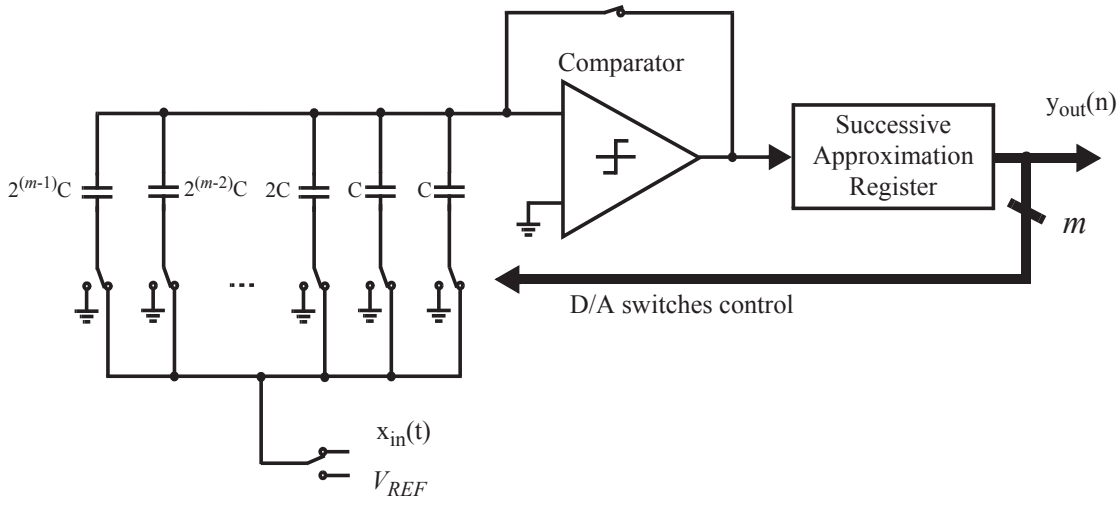
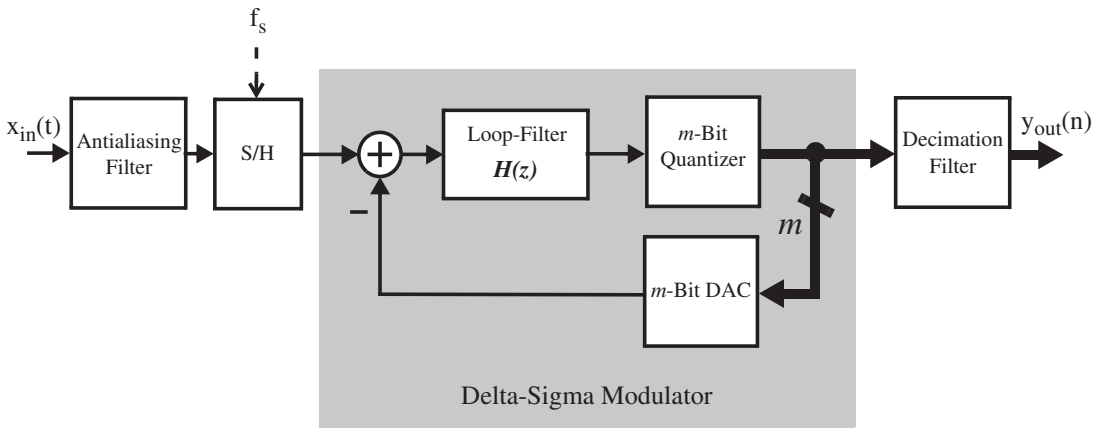
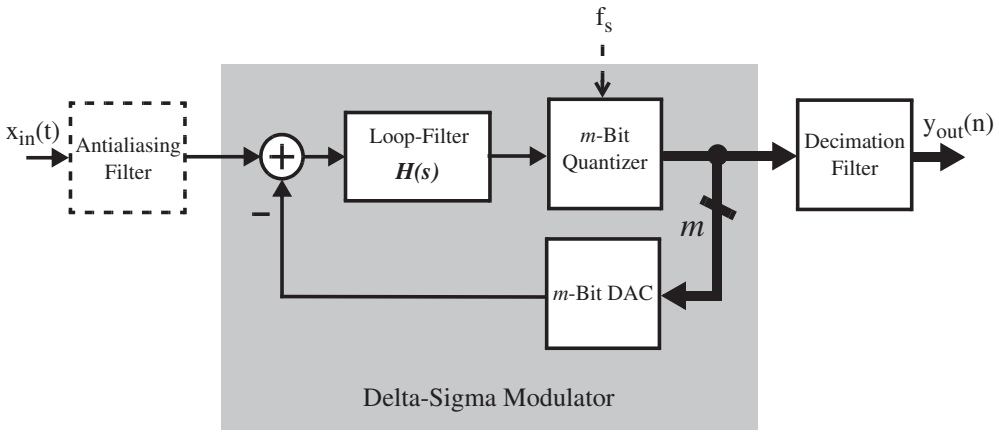


Figure 2.2: Successive-Approximation-Register (SAR) ADC.



(a) Discrete-Time implementation.



(b) Continuous-Time implementation.

Figure 2.3: Delta Sigma ($\Delta\Sigma$) ADC.

Figure 2.4 compares the bandwidth and resolution of state-of-the-art SAR ADCs and $\Delta\Sigma$ modulator implementations. The plot demonstrates the prevalence of $\Delta\Sigma$ ADC implementations for resolutions exceeding 10 bits. Since the intended ADC is expected to target high-resolution applications, $\Delta\Sigma$ architectures will be the focus of the discussion moving forward.

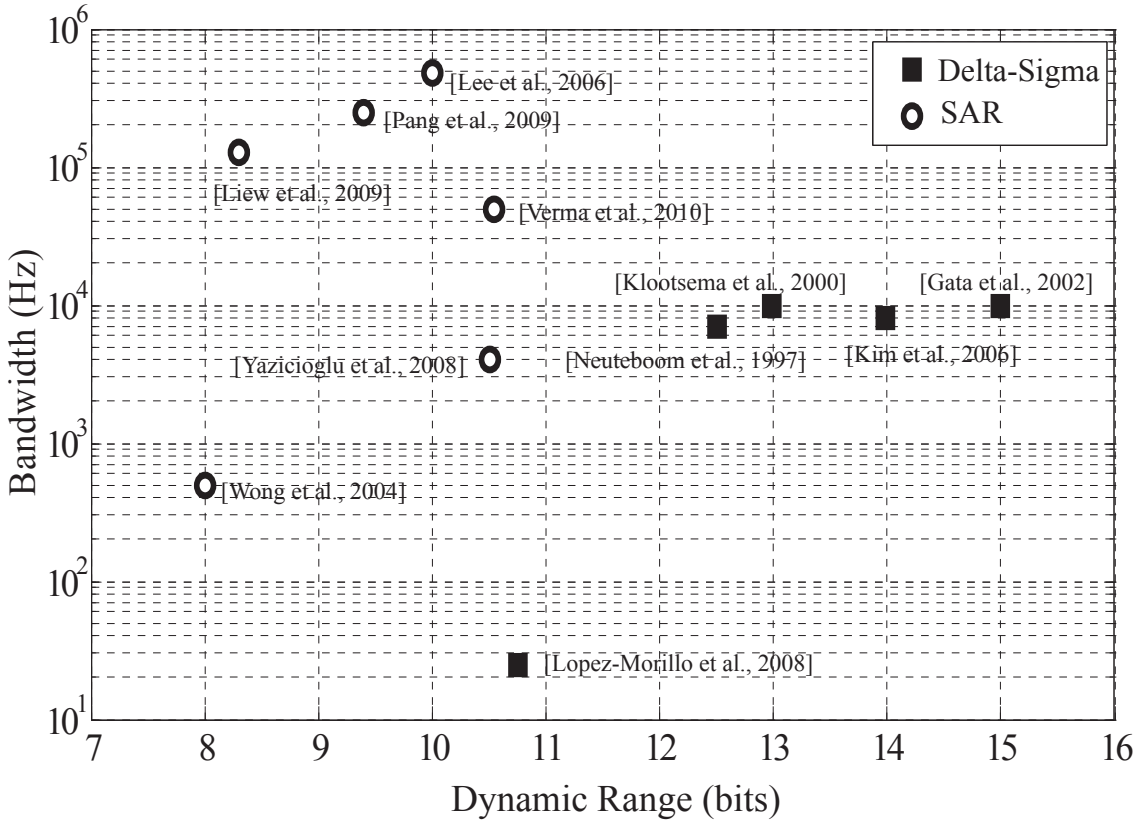


Figure 2.4: Dynamic range and bandwidth of state-of-the-art SAR ADCs and $\Delta\Sigma$ modulators for biomedical applications ($>$ 8 bits).

2.2 Delta-Sigma Modulator Basics

To ease the analysis of $\Delta\Sigma$ modulators, it is customary to linearize the system in Fig. 2.3(a), as shown in Fig. 2.5. This approach is needed as the internal quantization is a non-linear process in an otherwise linear system. The noise $Q(z)$, referred to as the *quantization noise*, now appears as an addition within the $\Delta\Sigma$ modulator loop, and is approximated as an input-independent additive white noise [Gra97][1].

[1] For further details on the assumptions and limitations of the input-independent additive white noise approximation, the reader is referred to [Gra97].

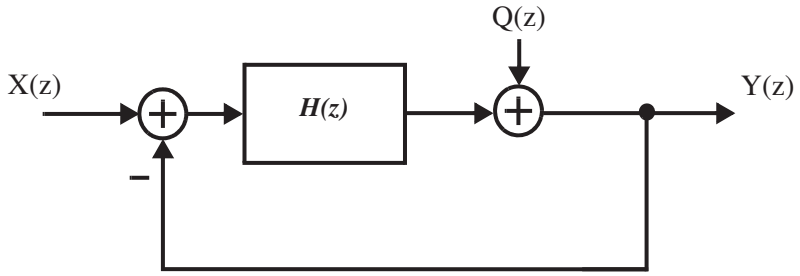


Figure 2.5: Linear model of a $\Delta\Sigma$ modulator assuming an ideal DAC.

The output of the modulator can now be expressed as:

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z) \quad (2.1)$$

$$= STF(z)\cdot X(z) + NTF(z)\cdot Q(z) \quad (2.2)$$

where $STF(z)$ is referred to as the *signal transfer function*, and $NTF(z)$ is referred to as the *noise transfer function*. Here, $H(z)$ is the loop-filter transfer function.

As discussed in the previous section, $\Delta\Sigma$ modulators (Fig. 2.3) achieve high-resolution conversions using a low-resolution internal ADC. This is accomplished through three separate techniques, highlighted in the following subsections:

1. Oversampling.

2. Noise shaping.

3. Multibit internal quantization in multibit implementations.

Note that for the purpose of the following discussion, a discrete-time implementation will be considered. All the concepts discussed in this section apply similarly to continuous-time implementations.

2.2.1 Oversampling

In $\Delta\Sigma$ ADCs, the quantizer is commonly oversampled. The *oversampling ratio* (OSR) is given by

$$OSR \equiv \frac{f_S}{2f_{BW}} \tag{2.3}$$

where f_S and f_{BW} are the sampling frequency and signal bandwidth, respectively.

Oversampling results in the quantization noise, uniform across the sampling bandwidth f_S, to be spread over a larger spectrum with respect to the signal bandwidth, resulting in a reduction in the quantization noise within the signal bandwidth. The decimator at the output of the $\Delta\Sigma$ modulator (Fig. 2.3), which reduces the frequency of the high-frequency output, filters the out-of-band noise. The result is that for every doubling of the OSR, the quantization noise is halved, and the signal-to-noise (SNR) ratio increases by 3 dB.

2.2.2 Noise Shaping

To observe how noise shaping reduces the noise in the signal bandwidth, we revisit (2.1) and (2.2). If the loop-filters are designed such that $H(z) \gg 1$ within the modulator bandwidth, then $STF(z)$ and $NTF(z)$ reduce to

$$STF(z) \cong 1 \tag{2.4}$$

$$NTF(z) \cong \frac{1}{1+H(z)} \ll 1 \tag{2.5}$$

within the signal bandwidth.

A simple loop-filter can be designed using a simple integrator with $H(z) = 1/(z-1)$. In such a case the NTF reduces to

$$NTF(z) = 1 - z^{-1} \tag{2.6}$$

which results in a zero at DC and the noise being shaped away from DC. A higher order loop-filter results in more noise shaping and increased SNR. For a *N*th-order $\Delta\Sigma$ modulator with a NTF given by

$$NTF(z) = (1 - z^{-1})^N \tag{2.7}$$

the SNR improves by $(2N+1)\cdot 3$ dB for every doubling of the OSR [Can92]. A drawback of increased loop-filter order is reduced stability: as the loop-filter order increases beyond two, the modulator becomes susceptible to instability, necessitating careful design. Additionally, the increase in out-of-band noise as the loop-filter order increases places more demanding design requirements on the decimator.

2.2.3 Multibit Quantization

Multibit quantization within a $\Delta\Sigma$ modulator loop has several advantages:

1. Multibit quantization increases the achievable resolution due to the lowering of the in-band quantization noise.

2. Multibit quantization increases the stability of the modulator, enabling the design of more robust higher-order $\Delta\Sigma$ modulators, further increasing resolution.

3. When the modulator OSR is lowered, the ability of higher-loop-filter-orders to increase the Signal-to-Quantization-Noise-Ratio (SQNR) is diminished, while the SQNR resulting from adding quantization bits remains intact at approximately 6 dB [Ham04b]. This enables the design of high-resolution $\Delta\Sigma$ modulators at low OSRs.

Multibit quantization does introduce complications, however, as it necessitates multibit digital-to-analog conversion in the feedback path. While single-bit DACs are inherently linear, multibit DACs suffer from unit-element mismatch errors which can result in significant distortion, as they add directly to the input of the modulator and are thus not noise

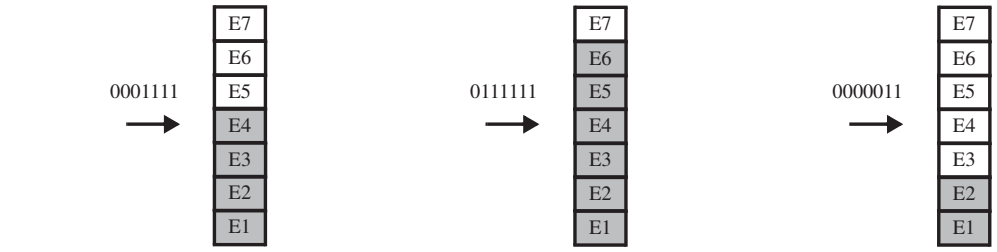
shaped. Therefore the use of a multibit quantizer and DAC requires the use of linearization techniques in the feedback path [Car97].

Dynamic-Element-Matching (DEM) techniques rely on an algorithm that determines the selection sequence of the DAC unit-elements for each DAC sample. The result of DEM techniques is a shifting of the generated mismatch-errors from DC to higher frequencies. The order of the high-pass filtering is dependent on the DEM selection algorithm employed.

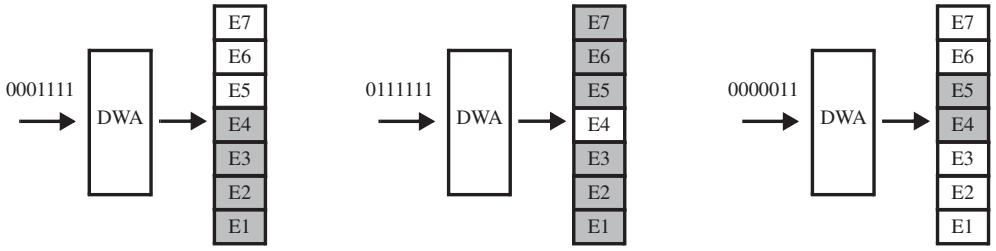
One widely used DEM technique is Data-Weighted-Averaging (DWA) [Bai95]. The DWA algorithm relies on a rotation among DAC unit-elements, such that the first unit-element employed in the generation of a DAC output is the element following the last unit-element employed in the generation of the previous DAC output. This concept is demonstrated in Fig. 2.6, which outlines the unit-elements selected to generate the DAC output over three sampling periods for two scenarios: a DAC with no unit-element linearization technique, and a DAC employing the DWA algorithm. The DWA algorithm results in a first-order high-pass shaping of the DAC mismatch errors [Nys96].

2.3 Continuous-Time vs. Discrete-Time $\Delta\Sigma$ Modulators

The first design choice encountered when designing a $\Delta\Sigma$ modulator for a targeted application, is whether to employ a discrete-time (Fig. 2.3(a)) or continuous-time (Fig. 2.3(b)) architecture. Since the choice of architecture is dependent on the targeted specifications, it is beneficial to explore the advantages and disadvantages of both implementations. This can be performed by comparing both architectures under the following criteria: sampling, loop-filter implementation, and errors introduced due to timing errors. The following discussion will demonstrate the advantage of continuous-time architectures in the implementation of low-power low-voltage $\Delta\Sigma$ ADCs targeting biomedical applications



(a) No DEM technique.



(b) DWA selection technique.

Figure 2.6: DAC unit-element selection over 3 sampling periods for; a) No DEM technique; and b) DWA selection technique. Highlighted in grey are the DAC unit-elements selected at each sampling period.

2.3.1 Sampling

In order to generate the sampled input fed into the discrete-time loop-filter of a discrete-time $\Delta\Sigma$ modulator, the sampling operation is performed at the input of the $\Delta\Sigma$ modulator (Fig. 2.3(a)), resulting in the sampling non-idealities adding directly to the input signal. Accordingly, highly-linear switches are required at the input of the modulator, with specifications that match the linearity of the overall system. This task is complicated in low-voltage implementations, where additional techniques such as bootstrapping [Ste99] may be required to ensure high sampling linearity.

In contrast, the sampling operation in continuous-time modulators is performed prior to the quantizer, as shown in (Fig. 2.3(b)). Therefore, the non-idealities generated by the sampling operation are noise-shaped by the loop-filter, relaxing the linearity requirements of the sampling switch.

The resulting noise-shaping of the sampling operation in continuous-time modulators also performs a degree of anti-alias filtering of the input signal. This eases the specification of the anti-aliasing filter at the input of continuous-time modulators, which can be omitted altogether in some circumstances [Can85] [Zwa96] [Che00], resulting in power savings.

2.3.2 Loop-Filter Implementation

Discrete-time integrators, implemented through the use of switched-capacitor integrators, require operational transconductance amplifiers (OTAs) with high bandwidth in order for the charge transfer to settle to the required accuracy. The required bandwidth is several orders of magnitude of the sampling rate. These settling restrictions do not apply to continuous-time integrators, where the same charge transfer occurs, but is performed over the entire clock cycle [Zwa96]. Therefore, continuous-time op-amps can operate at much lower gain-bandwidth products than their discrete-time counterparts, resulting in lower power consumption.

Additionally, the virtual grounds of amplifiers in continuous-time modulators are less susceptible to glitches than their discrete-time modulator counterparts, generated in the latter by large switching transients [Che00].

A drawback of continuous-time implementations is the increased error in the realization of the integrator gain. In switched-capacitor implementations the integrator gains are determined by a capacitor ratio, where only relative mismatch between the capacitors contributes to the gain error. The resulting low relative mismatch, which can be in the order of 0.1 % [Ort06], results in high integrator-gain mismatch immunity. The integrator gain in continuous-time implementations is implemented as an *RC* or *gmC* product (or LC product in the case of LC resonators for bandpass noise-shaping), resulting in significantly larger process-dependent gain errors. Additionally, techniques such as correlated-double-sampling, used to reduce flicker (*1/f*) noise, can only be employed in switched-capacitor integrator implementations.

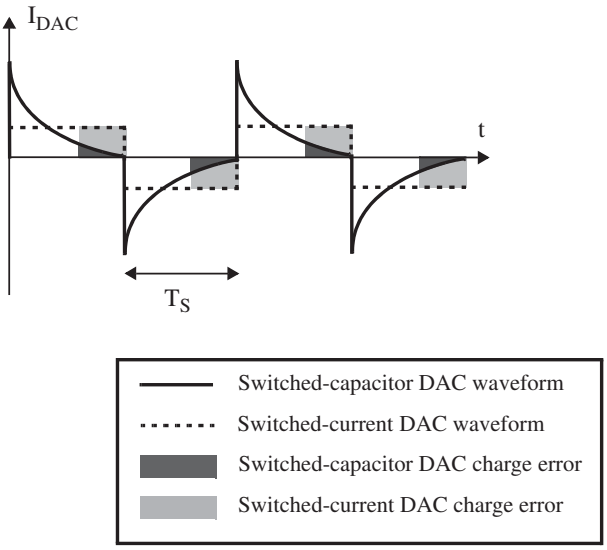


Figure 2.7: Clock-jitter effects on switched-capacitor and switched-current DAC implementations.

2.3.3 Time-Induced Errors

As shown in Fig. 2.7, in discrete-time modulators, most of the charge transfer in a switched-capacitor DAC occurs at the beginning of the clock cycle. Hence, clock jitter results in little error in the amount of charge transferred. In contrast, the charge-transfer rate of a switched-current DAC employed in continuous-time modulators is constant throughout the clock cycle, making continuous-time implementations more susceptible to clock-jitter errors [Che99] [Zwa96]. This is particularly significant as DAC errors add directly at the input of the modulator and are therefore not subjected to noise shaping, as discussed earlier. Several methods exist to reduce the errors introduced by clock jitter in continuous-time modulators, such as the use of non-rectangular DAC pulses [Ort06], and multibit quantization. Each of these techniques introduces its own set of challenges [Ham04a].

Furthermore, in continuous-time modulators, the sampling of the quantizer, and the conversion of the DAC cannot be performed simultaneously. The time needed between the sampling of the quantizer and the switching of the DAC in continuous-time modulators, referred to as *excess loop delay*, alters the loop-filter transfer function [Gos88] [Gos90]. In

high-speed continuous-time modulators, excess-loop-delay becomes a significant fraction of the clock cycle, and the loop-filter transfer function needs to be altered to account for its effects.

2.3.4 Summary

As outlined earlier, a primary design objective for ADCs targeting biomedical applications is minimizing the power consumption. Continuous-time implementations achieve higher power-efficiency than their discrete-time counterparts, and thus are more suitable for the targeted application. Additionally, the low conversion frequency requirements for biomedical signals results in the minimization of clock-jitter and excess-loop-delay effects in continuous-time implementations targeting biomedical applications.

The following section outlines several low-power low-voltage techniques utilized in the design of discrete and continuous-time $\Delta\Sigma$ ADCs. Although the discussion in ensuing chapters will be devoted solely to the proposed continuous-time $\Delta\Sigma$ modulator design, discrete-time implementations are included in the following discussion to provide a complete overview of techniques employed in $\Delta\Sigma$ ADCs targeting biomedical applications.

2.4 Prior Art: Low-Power Low-Voltage $\Delta\Sigma$ ADCs for Biomedical Applications

Several techniques have been employed in the design of low-power low-voltage $\Delta\Sigma$ ADCs targeting biomedical applications. These techniques facilitate the lowering of supply voltages, result in a reduction of dissipated power, or achieve both. The following subsections outline the most common of these techniques, and their implementation in the literature. Section 2.4.1 and Section 2.4.2 present techniques that are strictly low-power or low-voltage. Section 2.4.3 presents techniques that have been utilized to both reduce power, and facilitate low-voltage operation. Section 2.4.4 discusses the application of log-domain

techniques in the design of $\Delta\Sigma$ ADCs.

2.4.1 Low-Power Techniques

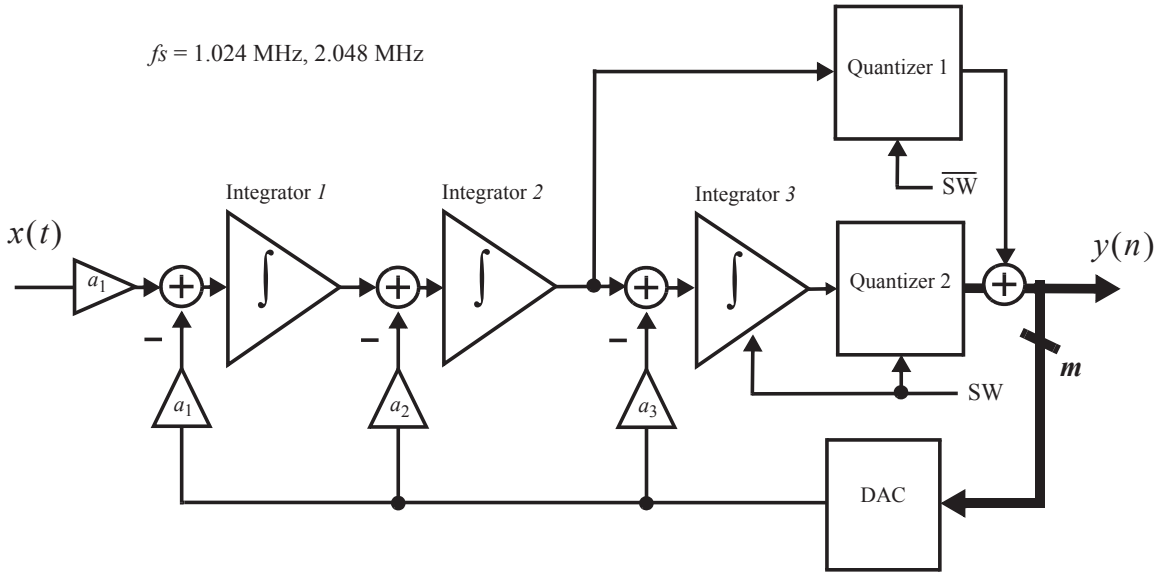
Variable Resolution Systems

The resolutions at which biomedical signals need to be processed vary with the varying nature of the signals themselves. During periods of low signal activity or inactivity, the signal need not be processed at high resolution. Additionally, in hearing aids, higher amplitude signals can be processed at lower resolutions than their lower-amplitude counterparts. In such cases, significant power reduction can be achieved by lowering the resolution of the ADC at times when high-resolution acquisition is not needed. This technique has been used in biomedical SAR ADCs [Li07], as well as $\Delta\Sigma$ modulators. The remainder of this section will focus on $\Delta\Sigma$ ADC variable-resolution implementations.

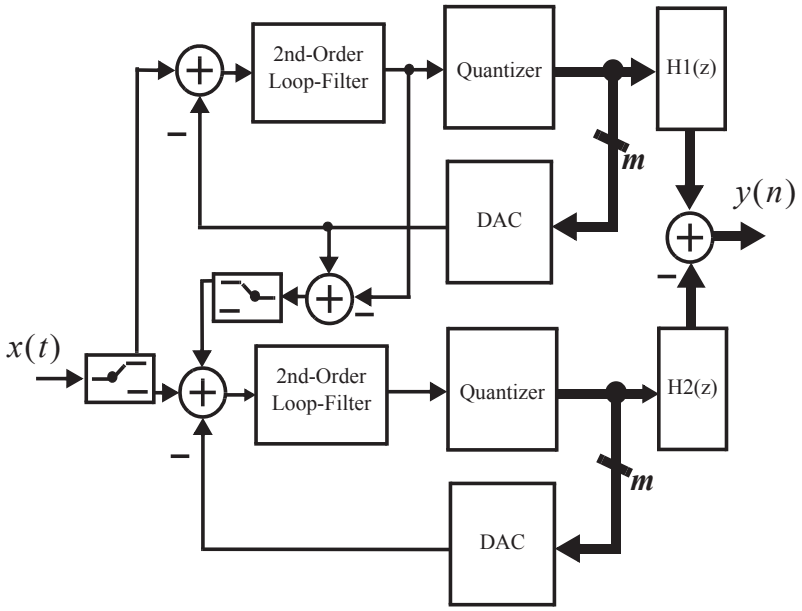
In [Kim06], an adaptive SNR $\Delta\Sigma$ ADC was proposed for a hearing aid. The span of the input signal amplitude was divided into four ranges, with the SNR of the modulator varying according to the applied input range. Variable resolution was achieved by varying the modulator order and/or OSR; the ADC was designed to operate as a 2^{nd} or 3^{rd}-order $\Delta\Sigma$ modulator with a sampling frequency of 1.024 MHz or 2.048 MHz (Fig. 2.8(a)). The resulting ADC achieves four resolution configurations, spanning 72 dB to 86 dB, with the resulting power ranging from 26.4 μW to 36.7 μW.

In [Hsu07], a variable resolution ADC is implemented to process a wide range of biopotentials, with resolutions spanning 10 - 16 bits. Similar to [Kim06], variable resolution was achieved by varying the modulator order and sampling frequency. Here, a 2+2 MASH $\Delta\Sigma$ modulator architecture was used (Fig. 2.8(b)). The order of the modulator was lowered by disconnecting the MASH connection and utilizing a single 2^{nd}-order loop-filter path.

While the aforementioned techniques result in power reduction during low-resolution operation, they do not result in power-reduction across the range of operating resolutions, and come at the expense of additional switching and increased digital-processing complex-



(a) Variable resolution implementation in [Kim06].



(b) Variable resolution implementation in [Hsu07].

Figure 2.8: Variable resolution ΔΣ modulator implementations.

ity.

Circuit Reduction Techniques

In the previous section, the lowering of the $\Delta\Sigma$ modulator order represents a particular case of achieving power savings through circuit-reduction techniques. In general, circuit reduction techniques can be employed without varying the modulator order. In addition to the power savings resulting from the variable resolution of the ADC in [Hsu07], the ADC employs a single-phase integrator technique in order to reduce circuit complexity, substrate noise and area [Goe05]. The single-phase integrator technique enables disabling of the first and second integrator interchangeably in each of the 2^{nd}-order paths, resulting in power savings. In contrast to variable resolution techniques, the single-phase integrator technique achieves power reduction across the resolution span of the ADC. However, the technique results in reduced integrator accuracy.

2.4.2 Low-Voltage Techniques

One of the challenges faced in the design of discrete-time $\Delta\Sigma$ modulators is the implementation of the floating switches at the output of switched-capacitor integrators. It is desired that these switches, usually implemented as CMOS switches comprised of a parallel combination of an NMOS and PMOS transistor, maintain constant linear conductance as the input signal is varied. As the supply voltage is lowered and approaches the sum of the NMOS and PMOS threshold voltages, the conductance of the switch varies over the input signal range.

A technique used to overcome the variation of switch conductance at low supply voltages is clock voltage boosting (Fig. 2.9), where the voltage at the gates of the switching transistors is boosted to 2 x VDD [Gri96]. In [Klo00], clock boosting was employed for switches in the signal paths of a discrete-time 2^{nd}-order $\Delta\Sigma$ modulator. The resulting ADC operates from a supply voltage of 0.9 V, with a resolution of 13 bits while consuming a power of 72 μW. In [Gat02], locally boosted supply voltages are used to drive NMOS

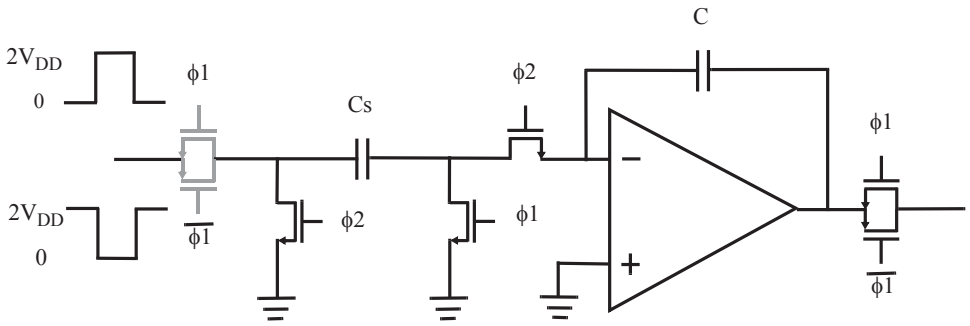


Figure 2.9: Clock voltage boosting technique.

gates in a 3rd-order ΔΣ modulator and its preceding input compression limiter. The resulting ADC operates from a supply voltage of 1.1 V, achieving a resolution of 15 bits while dissipating a power of 72.6 μW. Finally, in [Goe05], a mixed clock-boosting and switched op-amp technique is used in the implementation of a 2nd-order ΔΣ modulator, where clock-boosting is applied to the modulator's input-path switches. The discussion of the switched op-amp technique, and its implementation in the ΔΣ modulator in [Goe05] is deferred to the next section.

Unfortunately, the high voltage applied to the gates of voltage-boosted clocking transistors can result in transistors being prone to gate-oxide breakdown. As device dimensions shrink in advanced CMOS technologies, the use of clock voltage boosting becomes increasingly difficult.

2.4.3 Low-Power Low-Voltage Techniques

Switched Op-Amp (SO) Technique

Another technique used to overcome the implementation of floating switches at discrete-time integrator outputs is the switched op-amp technique. First introduced in [Ste93], the switched op-amp technique facilitates the realization of low-voltage switched-capacitor integrators by eliminating the floating switch at the integrator outputs, and instead switching on and off the output stage of the integrator op-amp (Fig. 2.10).

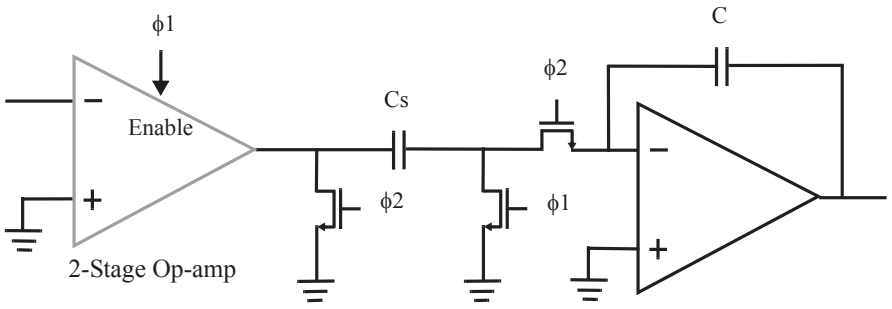


Figure 2.10: Switched op-amp technique.

In [Goe05], switched op-amp techniques were used in the implementation of a 2nd-order $\Delta\Sigma$ modulator. Two half-delay integrators are implemented using a two-stage topology: Both share the same amplifier, followed by two output stages operating in opposite phases, a technique suggested in [Che02]. This results in not only overcoming the low-voltage limitations on the floating switch, but also a significant reduction in power. Similarly, in biomedical devices such as [Ger05] [Bon04], power consumption is reduced by switching off the op-amp output stage during part of the signal transfer cycle.

A problem in employing the switched op-amp technique is the inability of applying it at the input of the first integrator, where the input switch is not preceded by an amplifier. Additionally, the implementation of the switched op-amp in subsequent integrators results in a reduction of circuit speed, as the second stage of each integrator needs to be powered on and off. While this reduction in speed may not limit operation in low-medium bandwidth biomedical applications, the challenge of implementing the input switch persists.

Subthreshold Design

Biasing transistors in the weak-inversion region, commonly referred to as the subthreshold region, can result in significant power savings and facilitate low-voltage design:

- The transistor transconductance-to-current ratio, or transconductance efficiency (g_m/I_D), is maximized, enabling the realization of highly power-efficient circuits.

- The transistor gate-to-source voltage (V_{GS}) is biased below the threshold voltage V_T, lowering the voltage headroom requirements.

- The transistor drain-to-source saturation voltage ($V_{DS,sat}$) is minimized, further lowing the voltage headroom requirements.

A drawback of using weak-inversion devices is their limited bandwidth [Bin08]. However, in low-medium bandwidth applications such as biomedical interfaces, this limitation is circumvented. In such applications, the low-signal bandwidth of the input signals, combined with the high power efficiency of weak-inversion transistors, makes weak-inversion $\Delta\Sigma$ ADCs particularly attractive.

Weak-inversion design techniques have been widely used in the design of low-power low-voltage ADCs. In [Lóp08] [Ger05], weak-inversion biasing is applied to the design of integrators within the $\Delta\Sigma$ modulator. A particular application of weak-inversion devices is the design of log-domain circuits, which rely on the exponential characteristics of bipolar-junction-transistors (BJTs), or weak-inversion MOS devices. The design of log-domain circuits, and their implementation to date in the design of $\Delta\Sigma$ modulators, is discussed in the following subsection.

2.4.4 Log-Domain $\Delta\Sigma$ Modulators

Log-domain circuit techniques have previously been proposed as a low-power low-voltage technique in the design of continuous-time (CT) $\Delta\Sigma$ modulators [Ser02] [Red07]. In part, the maximizing of the transconductance-to-current ratio in weak-inversion results in log-domain implementations achieving higher power efficiency than their active RC and gm-C counterparts [Ort06]. In contrast to traditional internally-linear implementations, log-domain systems rely on compression of the signal at the input and expansion of the signal prior to the output, resulting in internally-nonlinear signals while maintaining a linear input-output relationship. Therefore, in addition to the advantages of weak-inversion de-

vices noted in Section 2.4.3, log-domain circuits offer the additional low-power low-voltage advantages:

- The low internal voltage swings lower the voltage headroom requirements, enabling designs with very low supply voltages [See90].
- As will be discussed in the next chapter, the extension of the dynamic range due to the compressed nature of the internal signals offers the possibility of increased power savings in log-domain modulators.

Implementation of log-domain $\Delta\Sigma$ modulators has so far been restricted to utilization of single-bit internal quantizers [Ser02] [Red07], and no implementation utilizing a multi-bit internal quantizer has been presented to date. As discussed in Subsection 2.2.3, multibit quantization offers several advantages in the design of $\Delta\Sigma$ modulators. The next chapter will outline the fundamentals of log-domain systems, before the presentation of the proposed multibit log-domain $\Delta\Sigma$ modulator in Chapter 4.

CHAPTER 3

Fundamentals of Log-Domain Circuits

SINCE the introduction of log-domain filtering, the technique has garnered interest as a low-power low-voltage circuit technique. The development of log-domain circuits has evolved since then to encompass various design approaches, and with the increased proliferation of CMOS design with technology scaling, has evolved from its bipolar-transistor beginnings to predominantly CMOS implementations. Although the implementation of log-domain circuit techniques continues to be demonstrated in various applications, its utilization has failed to gain widespread use among designers.

In this chapter an overview of log-domain circuit design is presented, with emphasis on issues that continue to hinder the wide use of log-domain circuits. In Section 3.1 companding systems are discussed as a precursor to the discussion of log-domain circuits in Section 3.2. Section 3.3 presents a summary of the development of log-domain integrator design. Finally, challenges in the design of log-domain circuits are examined in Section 3.4.

3.1 Companding Systems

The concept of companding has long been considered in the areas of transmission and storage, as well as audio recording [Tsi97]. The benefits of employing companding in signal processing were outlined in [Tsi90], and the relationship of companding within the larger category of externally linear, time-invariant systems that may be internally time-variant and/or non-linear was discussed in [Tsi97].

Companding involves compressing the signal at the input, processing it, and expanding the signal at the output, as demonstrated in Fig. 3.1. Here, the varying gain factor c is signal dependent and is determined by measuring a signal or a set of signals within a signal processor. Companding allows the internal analog signal processor to operate within a small dynamic range, while achieving a significantly larger dynamic range at the output. Since the degrees of compression and expansion are signal dependent, the process is internally non-linear.

As demonstrated in Fig. 3.1, companding results in a relaxation of the noise requirements of the internal signal processor. Note that for the purposes of Fig. 3.1, the input is assumed to be noiseless, which is a reasonable assumption since the input noise is expected to be lower than the noise introduced by the internal signal processor. Additionally, the compressor is assumed to be noiseless, in order to clearly demonstrate the noise advantage of the filter core. In reality, the compressor will introduce noise, which will benefit from the increased threshold for noise in the compressed domain.

In addition to the acquired noise advantage, companding results in a relaxation of the overload level within the internal signal processor, when compared to the external overload level restrictions (Fig. 3.1). This advantage takes further significance in systems where the external signals appear as currents, offering the potential for signals unrestricted by external overload levels, as will be discussed in Section 3.2.

Dynamic range improvements in companding systems are not only attributed to the

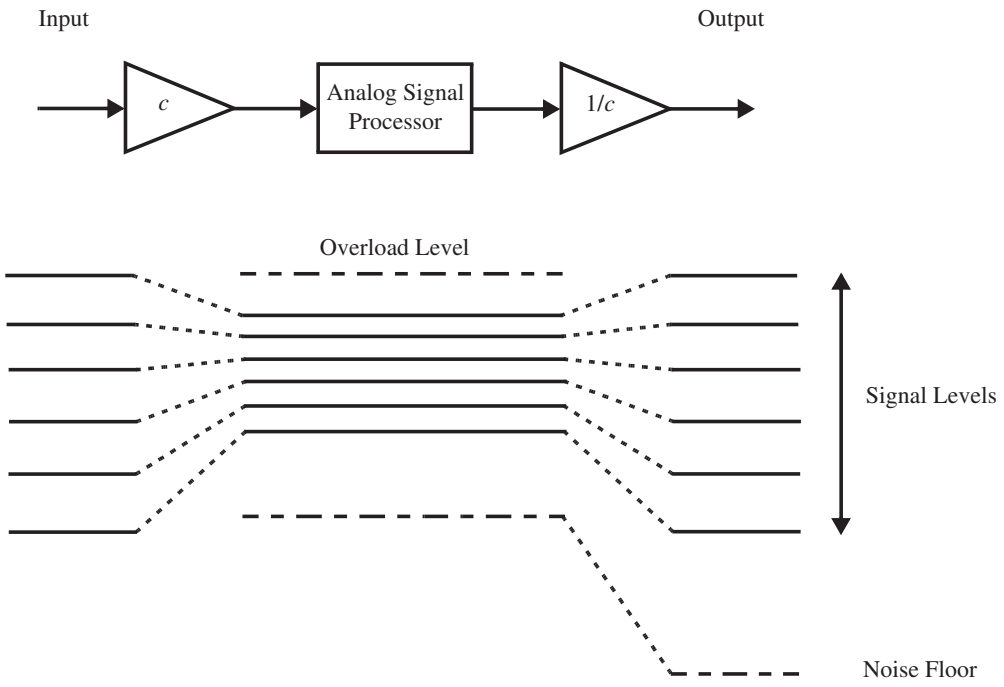


Figure 3.1: Companding principle [Tsi97]. Here the gain factor c varies and is signal dependent.

compression and expansion of the signal; the non-linearity of the internal signals allows it to be no longer bound by the small-signal restrictions in linear circuits. In conventional linearly behaving circuits, linear behaviour is established by restricting the signal swing around a bias point, thus ensuring that the signal is not affected by the non-linearity of active components. This small-signal restriction results in minimal current swing when compared to the potential for high signal-swings offered by the significantly larger bias current, severely limiting the achievable dynamic range. By abandoning these restrictions, such as in the case of companding systems, the achievable signal swing can increase drastically, resulting in a further increase in dynamic range.

The control signal employed to alter the gain at the input and output of a companding system can vary. In syllabic companding systems, the gains are controlled by a reading of the average power of one of the signals. Conversely, instantaneous companding systems rely on the instantaneous value of a signal when determining the compressing and

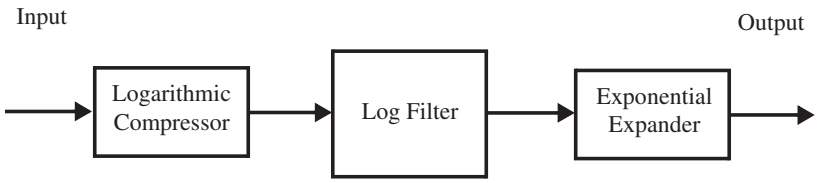


Figure 3.2: Log-domain principle.

expanding gains [Tsi90] [Tsi95]. Log-domain signal processors, a subset of instantaneous companding systems, are outlined next.

3.2 Log-Domain Filters

Among the various algorithms employed by instantaneously companding systems, one approach is to logarithmically compress the signal at the input, and to expand it exponentially at the output, as shown in Fig. 3.2. The resulting filter is referred to as a log-domain filter. To demonstrate the operation of log-domain filters, and demonstrate the externally-linear, internally-non-linear behaviour, the simple log-domain filter in Fig. 3.3 is analyzed.

The compression of the signal is performed by utilizing the exponential relation of a weak-inversion CMOS transistor; by keeping the source/gate at signal-ground, and driving an input current through the transistor, an exponentially related signal appears at the gate/source of the transistor. The method of choice is dependent on the design constraints, including the external circuit-architectures interfacing with the input stage.

For the purposes of Fig. 3.3, the sources of the compressor (M_C) and expander (M_E) are kept at signal-ground. Assuming the compressor and expander are biased with the bias currents I_{Comp}, and I_{Exp}, respectively, the 1st-order response of the log-domain filter can be deduced through the analysis below.

Neglecting second-order effects, the total drain current i_D of a MOS transistor in weak-

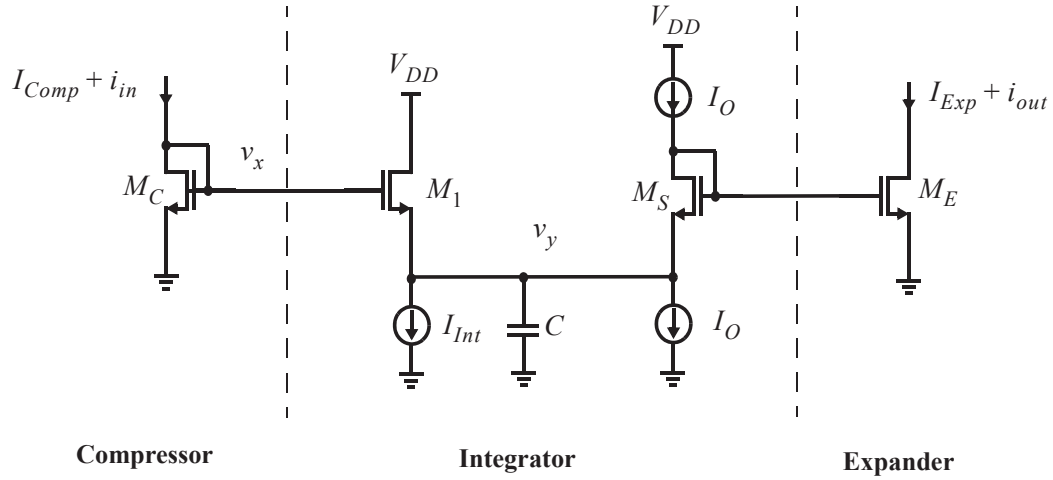


Figure 3.3: First-order log-domain filter example.

inversion biased in saturation ($V_{DS} > V_{DS,sat}$) is given by

$$i_D = 2\,\eta\,\mu\,C_{ox}\,U_T^2\left(\frac{W}{L}\right) e^{\frac{v_{GS}-V_T}{\eta\,U_T}} \tag{3.1}$$

where η, μ, C_{ox}, U_T, W, L, and V_T are, respectively, the transistors substrate factor, mobility, gate-oxide capacitance, thermal potential, channel width, channel length, and threshold voltage, and v_{GS} is the total voltage across the gate-source terminals.

The above equation can be rearranged to separate the signal and bias components of the drain current and gate-source voltage

$$i_D = I_D + i_d \tag{3.2}$$

$$= I_D\, e^{\frac{v_{gs}}{\eta\,U_T}} \tag{3.3}$$

where the integrator's bias current is defined as

$$I_D = 2\,n\,\mu\,C_{ox}\,U_T^2\left(\frac{W}{L}\right) e^{\frac{V_{GS}-V_T}{\eta\,U_T}} \tag{3.4}$$

Now the equation relating the compressor input current i_{in} and the compressed voltage v_x can be deduced from 3.2 and 3.3 as

$$v_x = \eta U_T \ln(1 + i_{in}/I_{Comp}) \tag{3.5}$$

Rearranging

$$i_{in} = I_{Comp}\,(e^{v_x/\eta U_T} - 1) \tag{3.6}$$

Transistor M_S acts as a level-shifter, transferring the integrator output-signal v_y to the base of the expanding transistor M_E. Therefore, the voltage-current relationship of the expander can be derived as

$$i_{out} = I_{Exp}\,(e^{v_y/\eta U_T} - 1) \tag{3.7}$$

The current in the integrating capacitor can be expressed as

$$I_{Comp} = C\,\frac{dv_y}{dt} = I_{Int}\,e^{\frac{v_x - v_y}{\eta U_T}} - I_{Int} \tag{3.8}$$

Multiplying (3.8) by $e^{v_y/\eta U_T}$

$$C\,\frac{dv_y}{dt}\,e^{v_y/\eta U_T} = I_{Int}\,e^{\frac{v_x}{\eta U_T}} - I_{Int}\,e^{\frac{v_y}{\eta U_T}} \tag{3.9}$$

Differentiating (3.7)

$$\frac{di_{out}}{dt} = \frac{I_{Exp}}{\eta U_T}\,e^{v_y/\eta U_T}\,\frac{dv_y}{dt} \tag{3.10}$$

Inserting (3.6), (3.7) and (3.10) into (3.9), generates the following

$$\frac{C\,\eta\,U_T}{I_{Exp}}\,\frac{di_{out}}{dt} \;=\; I_{Int}\,\frac{i_{in}}{I_{Comp}} - I_{Int}\,\frac{i_{out}}{I_{Exp}} \tag{3.11}$$

which can be rearranged to arrive at the following 1st-order externally-linear filter response

$$i_{in} \;=\; \frac{C\,\eta\,U_T}{I_{Int}}\,\frac{I_{Comp}}{I_{Exp}}\,\frac{di_{out}}{dt} + \frac{I_{Comp}}{I_{Exp}}\,i_{out} \tag{3.12}$$

Although, traditionally, the compressor bias current and expander bias current are kept equal, the above derivation does not assume that this is necessarily the case. From (3.12), it can be seen that if $I_{Comp} \neq I_{Exp}$, the filter is subjected to a gain I_{Comp}/I_{Exp}. However, no external non-linearity results from the compressor-expander bias inequality. It will be demonstrated in Chapter 4 that, in the case of log-domain $\Delta\Sigma$ modulators, that is not the case.

As mentioned in the last section, companding systems theoretically have the potential to be unrestricted by overload levels. This is particularly the case for class AB implementations of log-domain systems, where the input and output current signals can be significantly larger than the bias current. This concept was demonstrated for current-mode circuits operating in class AB in [See90]. Restated, in order to fully harness the potential for dynamic range extension offered by companding systems, the designed system needs to process signals significantly larger than the bias currents at which they are biased, making class AB log-domain operation particularly advantageous [Enz97] [Pun97]. Here the advantage of companding, which results in low internal voltage swings and a relaxation of the internal overload level, is extended by the unrestricted external overload level of class AB current-mode circuits.

Figure 3.4 demonstrates class AB operation in log-domain systems. It was demonstrated in [Enz97] [Pun97] that the noise of a log-domain integrator is dominated by the integrator bias current for $I_{sig} \ll I_{Bias}$, where I_{sig} and I_{Bias} are the input signal and inte-

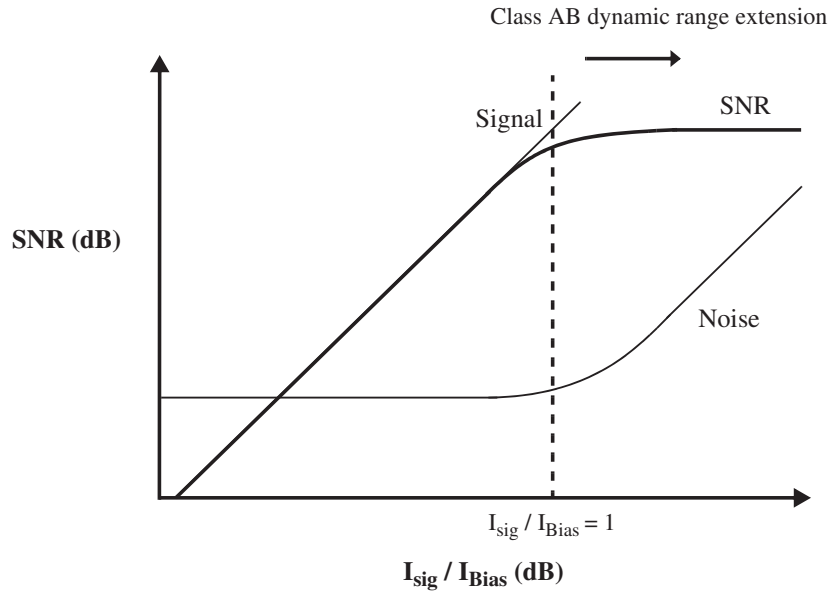


Figure 3.4: Class AB log-domain operation [Enz97].

grator bias current, respectively. This results in a constant noise for $I_{sig} \ll I_{Bias}$, and in turn, increasing SNR with input. As I_{sig} exceeds I_{Bias}, the output becomes increasingly dependent on I_{sig}, resulting in increasing noise and the levelling of the SNR curve, resulting in a constant SNR in class AB systems for $I_{sig} \gg I_{Bias}$. Although the SNR levels off, class AB log-domain systems benefit from the significantly extended dynamic range. In practice, however, I_{sig} cannot increase indefinitely with respect to I_{Bias}, since rising distortion and the Signal-to-Noise-and-Distortion Ratio (SNDR) requirements will limit the increase of I_{sig}.

3.3 Log-Domain Circuits Literature Overview

The introduction of log-domain theory has spurred several research avenues. Since a wide range of log-domain circuits have been proposed, and since the performance of log-domain systems is highly dependent on the circuit architectures employed in the design of the ana-

log components, this section will highlight the development of log-domain analog circuits in particular. Early literature focused on the development of log-domain theory. Further research investigated the realization of log-domain circuit synthesis techniques and circuits, first using bipolar technology, then increasingly employing CMOS devices. An overview of these topics is presented in this section. A discussion of the noise performance of log-domain circuits is deferred to the next section, where it is examined in detail.

3.3.1 Early Development

Filtering in the log-domain was first introduced in [Ada79], by presenting a log-filter composed of a diode, capacitor, and current source.

Motivated by a desire to achieve high frequency performance through the use of current-mode circuits [Rob89], a current-mode integrator implemented through use of the translinear principle [Gil75] was presented in [See90]. Additionally, the latter introduced class AB current-mode design, resulting in extended dynamic range in current-mode circuits.

In [Fre93], the first synthesis procedure for current-mode log-domain filtering was developed, based on the concepts introduced in [Ada79]. Although the resulting integrator is similar in concept to that presented in [See90], the paper presented a generalized design procedure for development of such filters. The proposed design procedure was based on transforming a state-space realization of a transfer function into a circuit realization. In [Fre94] the class AB current-mode approach in [See90] was utilized to realize a class AB implementation of the filter presented in [Fre93]. This paper suggested that the extended dynamic range resulting from the introduction of class AB current-mode filters raises the possibility of using current-mode filters, which had initially targeted high-frequency applications, for low-frequency applications.

3.3.2 Synthesis of BJT and BiCMOS Log-Domain Circuits

A new synthesis procedure for the design of log-domain filters was presented in [Per95] [Per96], based on operational simulation of LC ladders. Instead of relying on a set of non-linear equations to generate a log-domain filter, a signal-flow-graph (SFG) is generated from the LC representation of a filter, and transformed to a log-domain SFG through a set of proposed steps. Circuit-blocks were developed to implement the modified log-domain SFG. These proposals were extended in [ElG97], where a new integrator circuit was introduced to overcome potential DC instability issues when implementing some filter topologies.

The distortion introduced by the non-zero base currents resulting from the finite β of BJT transistors, as well as a desire to lower the minimum supply voltage of log-domain circuits, represent significant challenges in the implementation of BJT log-domain integrators. In [Pun95] [Pun96], architectures were presented to address these issues; similar to [See90], the former utilized the translinear principle to construct the proposed filter, but employed a folded-multiplier architecture rather than the stacked base-emitter architecture in [See90]. The proposed architecture resulted in a reduction of base-current-induced non-idealities, as well as a lower minimum supply voltage. In [Pun96], an alternate translinear loop, and base-current cancellation circuitry, were presented to minimize BJT base currents. In both designs, the base-current cancellation is at the expense of additional circuits, which necessitate accurate matching to achieve error-free cancelation.

An alternative, translinear-based architecture was presented in [Ser97]. Although the proposed integrator achieves low-voltage operation, it relies on a voltage follower within the integrator, resulting in increased circuit complexity.

In [ElG99] [ElG02], an all-NPN log-domain integrator was proposed in order to facilitate high-frequency operation. The proposed design achieves a lower minimum supply voltage than in [See90], which had also exclusively employed NPN transistors in the signal path. Class AB implementation of the proposed integrator was demonstrated in [ElG99]. However, as in other BJT-implemented designs, the effect of the non-zero base current

introduces distortion.

3.3.3 Synthesis of CMOS Log-domain Circuits

Implementation of log-domain integrators through the use of CMOS transistors biased in weak inversion has been motivated in part by the increased reliance on digital processing, as well as a desire to overcome the distortion introduced by base-currents in BJT implementations. CMOS implementations do however pose design challenges: namely, distortion introduced by threshold-voltage mismatch, lower-frequency operation resulting from operating in weak-inversion, and the potential for distortion introduced by the body-effect.

CMOS implementation of log-domain filters was first presented in [Tou94]; utilizing the log-domain synthesis procedure suggested in [Fre93], this paper harnessed the exponential characteristics of weak-inversion transistors in the design of log-domain filters. In [Pyt96], using a proposed CMOS translinear multiplier implemented through the use of bulk-driven CMOS transistors, the first all-CMOS implementation of a companding integrator was presented. The authors outlined how the small variation of the voltages at the nodes of the integrating capacitors, a result of the compressed nature of the internal signals, allowed the use of the non-linear parasitic capacitances of CMOS transistors in the implementation of the integrating capacitors of log-domain integrators. In [Fri96], an alternative bulk-driven CMOS log-domain integrator was presented. However, both bulk-driven designs presented in [Pyt96] and [Fri96] necessitate the use of separated transistor wells.

An alternative filter-synthesis approach was presented in [ElM99], which presented a universal CMOS log-domain biquad that can generate a low-pass, band-pass, high-pass, notch, and all-pass characteristic. However, the design exhibits poor low-voltage performance. Additionally, the proposed biquad can only be employed in the design of even-ordered high-order filters

In [Pyt99] [Pyt01] a CMOS log-domain integrator that is unaffected by the body-effect was presented, overcoming the need for separating CMOS transistors in separate wells.

Furthermore, the authors discussed the behaviour of the integrator as the level of channel-inversion of the CMOS transistor varies from weak- to moderate-inversion. In [Pyt01], a Class AB CMOS-transistor implementation was presented, using a CMOS implementation of a BJT-implemented class AB signal-preconditioner previously presented in [Fre94]. A drawback of the presented preconditioner is its reliance on stacking two gate-source voltages, necessitating a higher supply voltage than the accompanying integrator.

A technique to realize low supply-voltage CMOS translinear loops, immune to the body effect, was presented in [See00]; by introducing non-saturated CMOS devices in the translinear path, a cancellation of the transistors' body effects was demonstrated for several translinear models while lowering supply voltages. The proposed technique was applied to the CMOS implementation of the translinear-based integrator presented in [See90]. While this technique achieves the desired objectives, the lack of a systemic approach for its implementation makes the realization of high-order filters complex.

A generalized approach of generating CMOS log-domain circuits through the translinear principle was presented in [Ser00] and [Ser05]. It was demonstrated that device differences between BJT and CMOS devices hinder the direct mapping of bipolar log-domain implementations to CMOS technology. To overcome the effect of non-local substrates, exclusively gate-drive, or source-driven, transistor pairs are used. The tradeoffs of each design choice were outlined, as well as the proposal of auxiliary circuits for each of the two design approaches. The gate-driven integrator design presented here results in the same CMOS integrator proposed in [Pyt99] [Pyt01]. Class AB realizations of the CMOS compressor, integrator, and expander in [Ser00] were presented in [Red05]. Furthermore, a full realization of a Class AB CMOS band-pass filter was demonstrated.

In [Rod04], an alternative design aimed at eliminating the body-effect in CMOS implementations was proposed. Here, the use of a floating-gate CMOS (FGMOS) integrator was proposed to eliminate the use of the transistor bulk terminal. The drawback of this technique is the additional complexity of fabrication in CMOS technology.

One of the challenges faced in the implementation of all-MOS structures, discussed earlier in [Pyt96], is the non-linearity of MOS-implemented capacitors. In [Ser01], this non-linearity was discussed, and the use of capacitance or transconductance compensation was proposed to address the resulting distortion. In [Red04], a tuning-current compensation approach was proposed to address the capacitor non-linearity.

3.4 Log-Domain Design Challenges

The introduction of log-domain circuits has spurred research into addressing several challenges to the wide-adoption of log-domain circuits as a low-power low-voltage alternative. This research has included exploring and addressing the potential of some log-domain circuits to possess multiple operating points [Fox99], and a study of the unique noise-behaviour of log-domain systems.

In this section, two particular challenges in the design of high-resolution log-domain $\Delta\Sigma$ modulators are outlined: optimization of the noise generated within the modulator to meet a set of targeted requirements, and minimization of distortion introduced by variations in the operating equations of log-domain components.

3.4.1 Noise in Log-Domain Circuits

The internally non-linear nature of log-domain circuits results in signal-dependent noise at the output, generated by the non-linear transfer function relating each internal noise source to the output. The resulting intermodulation can be derived by observing Figure 3.5, where the drain-referred noise of each of the transistors in Fig. 3.3 is included. Employing the translinear principle [Gil75], the resulting translinear equation [Mul97] [Mul99] demonstrates the intermodulation of the signal (i_{in}, i_{out}) and noise ($i_{n,c}$, $i_{n,1}$, $i_{n,s}$, $i_{n,e}$) components

$$(I_{Comp} + i_{in} + i_{n,c})\,(I_O + i_{n,s}) \;=\; (I_{Int} + i_c + i_{n,1})\,(I_{Exp} + i_{out} + i_{n,e}) \qquad (3.13)$$

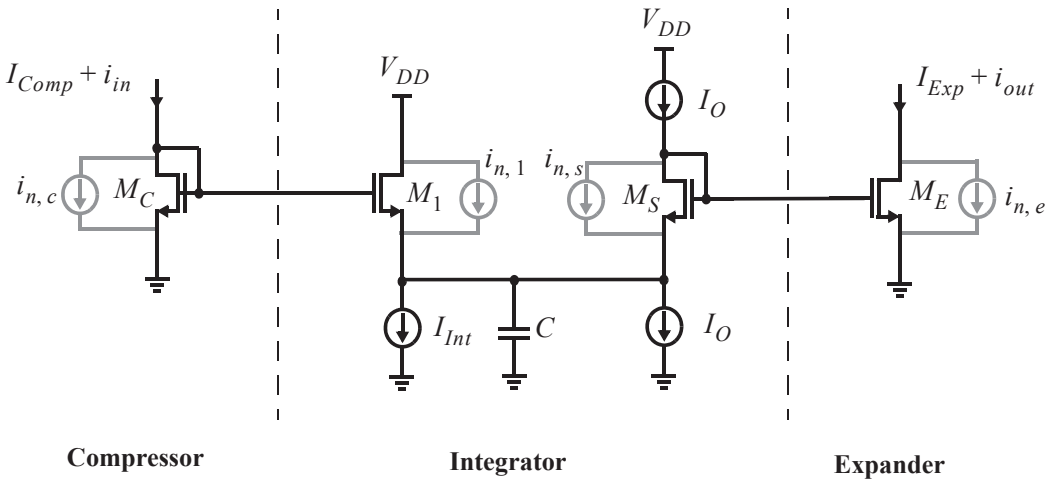


Figure 3.5: First-order log-domain filter and accompanying drain-referred noise sources ($i_{n,c}$, $i_{n,1}$, $i_{n,s}$, $i_{n,e}$), based on the representation in [Mul99].

Furthermore, the power spectral densities of noise sources in log-domain circuits are signal dependent [Mul97][Tot98].

It is worth noting that signal $\times$ noise intermodulation in log-domain circuits results in log-domain circuits being prone to the intermodulation of noise into the passband by large out-of-band signals [Mul97]. Therefore, special attention must be paid to the full spectrum applied at the input of log-domain filters.

Several techniques have been presented to evaluate the noise in log-domain circuits. A demonstration of noise evaluation for log-domain circuits is presented in [Pun97], where the noise within an individual integrator is translated to the output through its associated transfer function. Here, to ease the evaluation, the input signal variation is assumed to be slow.

In [Mul98] [Mul99], a technique is presented where the noise sources are included in the translinear equations characterizing a log-domain circuit, and approximations are made by neglecting noise cross products. In [Tot00], a noise analysis method is presented that relies on modifying the state-space response of externally-linear internally non-linear systems to include the effects of perturbations. By deriving the state-space equations in response to

perturbations, and by introducing signal-dependent noise contributions as perturbations to the system, the response of the system to noise sources is derived. In contrast to the method presented in [Mul98] [Mul99], the noise analysis presented in [Tot00] can be performed in the absence of translinear loops.

In [Ng02], the noise contribution of individual noise sources within significantly more complex log-domain architectures are translated to the output through their individual signal-dependent transfer function, without the need for combining noise sources. The modulated noise Power Spectral Density (PSD) of a noise source is expressed as a time-averaged stationary noise PSD modulated by the normalized signal power. In all the presented noise analysis methods, the noise was assumed to be small enough that approximations can be made to simplify the resulting noise derivations.

In this work, a noise optimization approach will be be proposed that combines both the noise relationships of individual log-domain components and SpectreRF simulations to arrive at the design parameters of our log-domain $\Delta\Sigma$ modulator. The objective is to provide log-domain designers with a streamlined, simulation-based approach, to ease the realization of log-domain $\Delta\Sigma$ modulator architectures meeting a set of design requirements.

3.4.2 Distortion Limitations

Ideally, when a MOSFET device operates in saturation, the device's drain current is independent of the drain-to-source voltage bias. In reality, channel length modulation when V_{DS} exceeds V_{DSsat} results in drain-current dependancy on V_{DS}, with the drain current increasing with increasing V_{DS}.

Disparity between the drain-to-source voltages of a differential pair results in a variation of the generated drain current. It will be demonstrated in Chapter 5 that differential-input log-domain integrators are prone to differences in the drain-to-source voltages of input pairs. The resulting disparity in differential inputs introduces significant distortion at the output. The same result can be deduced in differential-input compressors and expanders,

where the differential paths are subjected to different bias conditions.

The resulting distortion from drain-to-source voltage variations in differential paths is a dominant force hindering the achievable signal-to-noise-and-distortion ratio (SNDR) of a log-domain $\Delta\Sigma$ modulator, limiting the realization of high-resolution ADCs. Development of low-distortion differential log-domain building blocks raises the potential of log-domain circuits for high-resolution applications, including high-resolutions ADCs. In Chapter 5, the development of such low-distortion blocks is presented.

3.5 Summary

In Chapter 2, ADCs for biomedical applications, and the fundamentals of low-power low-voltage $\Delta\Sigma$ modulators were outlined. In this chapter, the fundamentals of log-domain circuit theory were presented. Furthermore, a summary of the development of log-domain architectures was presented, and relevant challenges to the proliferation of log-domain realizations in complex high-resolution applications were outlined.

The next three chapters will present various elements of a robust low-distortion multibit log-domain $\Delta\Sigma$ modulator targeting low-power high-resolution applications. Chapter 4 addresses the architecture-level design: it outlines the challenges of implementing multibit log-domain implementations and presents a novel architecture realizing the first multibit implementation of a log-domain $\Delta\Sigma$ modulator. Furthermore, behavioural models are developed to ease the optimization of log-domain $\Delta\Sigma$ modulators. Chapter 5 presents the circuit-level design of the log-domain loop-filter, and Chapter 6 presents a novel current-output DAC.

CHAPTER 4

Multibit Log-Domain $\Delta\Sigma$ Modulator Design: Architecture-Level

In CHAPTER 2, the advantages of multibit quantization in $\Delta\Sigma$ modulators were outlined. Furthermore, it was noted that previously proposed log-domain $\Delta\Sigma$ modulators were limited to single-bit quantization.

This chapter explores the challenges of multibit quantization and digital-to-analog conversion in log-domain $\Delta\Sigma$ modulators, and presents a novel multibit log-domain $\Delta\Sigma$ modulator design. The proposed implementation is the first multibit log-domain $\Delta\Sigma$ modulator to have been reported in the literature [Sha14b]. Furthermore, this chapter presents the behavioural modeling of various non-idealities, and investigates their impact on log-domain $\Delta\Sigma$ modulators. In Section 4.1, the challenges of designing a multibit log-domain $\Delta\Sigma$ modulator are presented, and equations are derived to demonstrate that unlike classical $\Delta\Sigma$

modulators, the transformation from single to multibit internal quantization is not straightforward. In Section 4.2, the proposed class AB multibit log-domain $\Delta\Sigma$ modulator design is presented, and it is demonstrated that the noise transfer function (NTF) is equivalent to its classical, internally-linear, counterpart. In Section 4.3, SIMULINK log-domain blocks are proposed to enable behavioural simulations of the proposed modulator, and the effects of various non-idealities are modeled. In Section 4.4, SIMULINK simulation results verify the proposed modulator's operation, and demonstrate the effects of the introduced circuit non-idealities. A summary of the work presented in this chapter is published in [Sha14b].

4.1 Challenges in the Design of Multibit Quantizers and DACs for Log-Domain $\Delta\Sigma$ Modulators

Figure 4.1 with $m = 1$ depicts a classical $\Delta\Sigma$ modulator with a 1-bit quantizer and DAC. This architecture can be directly mapped to a log-domain $\Delta\Sigma$ modulator [Ser02] as demonstrated in Fig. 4.2. Here, V_{REFp} denotes the positive input-reference voltage of the log-domain quantizer and the output-reference voltage of the log-domain DAC, while V_{REFn} denotes the negative input-reference voltage of the log-domain quantizer and the output reference voltage of the log-domain DAC. Note that the signal $v_y(t)$ at the input of the 1-bit log-domain quantizer in Fig. 4.2 is a logarithmically scaled signal. Therefore, in order for the threshold voltage V_M of the quantizer's comparator to match the dc-bias of the compressed signal $v_y(t)$ at the quantizer's input, V_M must be shifted towards V_{REFp}, rather than being at $(V_{REFp} + V_{REFn})/2$ as in a classical 1-bit quantizer. Furthermore, V_{REFp} and V_{REFn} need to be scaled logarithmically, such that the DAC outputs match the compressed nature of the modulator internal signals.

The mapping of a classical $\Delta\Sigma$ modulator with a multibit quantizer and DAC (Fig. 4.1 with $m > 1$) to a log-domain $\Delta\Sigma$ modulator is depicted in Fig. 4.3. Here it will be demonstrated that such direct mapping is impractical to implement. This is because the

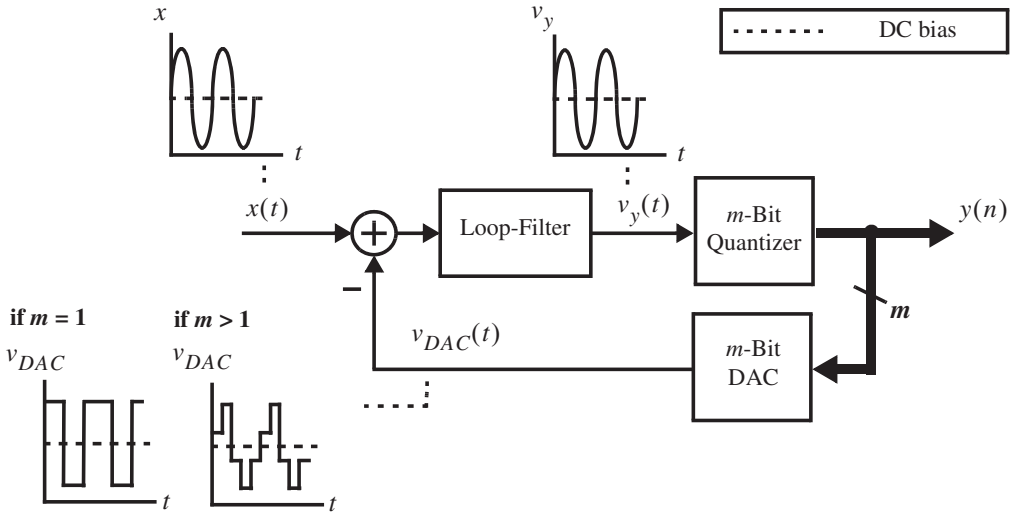


Figure 4.1: A classical $\Delta\Sigma$ modulator, with an m-bit quantizer and DAC.

signal $v_y(t)$ at the quantizer's input in Fig. 4.3 is a logarithmically scaled signal, thereby requiring a multibit quantizer with nonuniform step-sizes and a multibit feedback DAC with nonuniformly-spaced output-voltage levels. The complexity of the implementation in Fig. 4.3 is demonstrated by deriving the step-size between two consecutive quantizer input-threshold levels $V_{Q,c}$ and $V_{Q,c+1}$ (or, equivalently, between two consecutive DAC output-voltage levels).

To determine the quantization and D/A conversion step-size in the log-domain, we first consider the level of compression of a series of equally spaced inputs.

Similar to (3.5) in Section 3.2, a compressed voltage input $v_{in,log}$ can be expressed as

$$v_{in,log} = \eta\, U_T\, \ln(1 + i_{in}/I_{Comp}) \tag{4.1}$$

$$= \eta\, U_T\, \ln\left(1 + \frac{v_{in}}{R_{VI}\, I_{Comp}}\right) \tag{4.2}$$

where $i_{in} = v_{in}/R_{VI}$ is the compressor input current and v_{in} and R_{VI} are, respectively, the input voltage to be compressed, and the voltage-to-current conversion resistor needed to

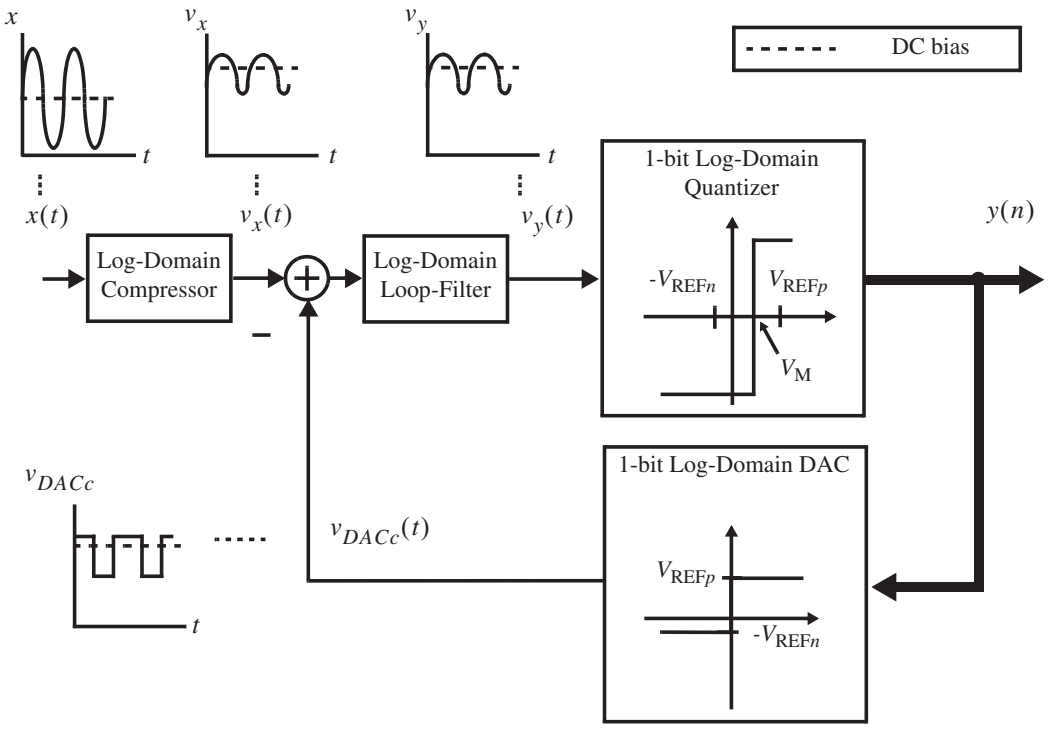


Figure 4.2: A log-domain ΔΣ modulator, with a 1-bit quantizer and DAC.

convert v_{in} to the compressor input current i_{in}.

The step-size Δ_c, defined as the step-size between quantizer/DAC levels c and $c-1$ can now be derived as

$$\begin{aligned}\Delta_c &= \eta U_T \ln\left(1+\frac{v_{lin,min}+c\,\Delta_{lin}}{R_{VI}\,I_{Comp}}\right) \\ &\quad - \eta U_T \ln\left(1+\frac{v_{lin,min}+(c-1)\,\Delta_{lin}}{R_{VI}\,I_{Comp}}\right) \\ &\qquad\qquad c=1,...,M\end{aligned} \tag{4.3}$$

Here Δ_{lin} is the step-size between the linear inputs, and is defined as

$$\Delta_{lin} = \frac{v_{lin,max}-v_{lin,min}}{M} \tag{4.4}$$

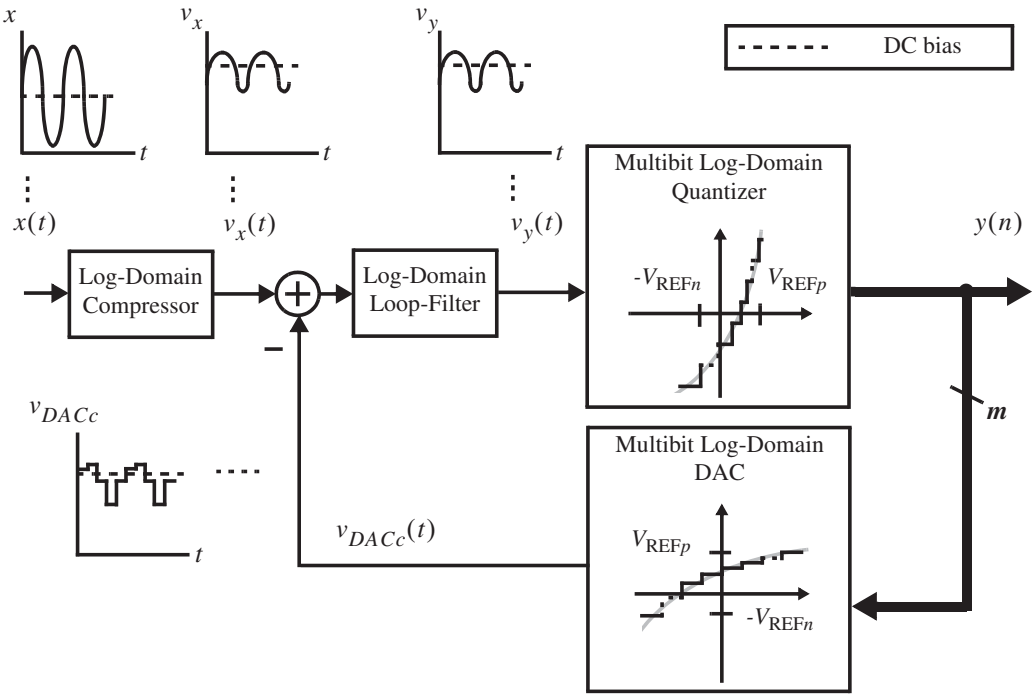


Figure 4.3: A log-domain ΔΣ modulator, with a multibit quantizer and DAC.

and $v_{lin,max}$ and $v_{lin,min}$ are the maximum and minimum linear input, respectively. Here, $M \equiv 2^m - 1$ is the number of input-threshold levels in the m-bit quantizer (number of output levels in the m-bit DAC).

Rearranging (4.3)

$$\Delta_c = \eta U_T \ln \left(\frac{1 + \frac{v_{lin,min}}{R_{VI} I_{Comp}} + \frac{c\,\Delta_{lin}}{R_{VI} I_{Comp}}}{1 + \frac{v_{lin,min}}{R_{VI} I_{Comp}} + \frac{(c-1)\,\Delta_{lin}}{R_{VI} I_{Comp}}} \right) \qquad (4.5)$$

$$c = 1, ..., M$$

Using (4.2), the reference voltages V_{REFp} and V_{REFn} can be derived as

$$V_{REFp} = \eta U_T \ln\left(1 + \frac{v_{lin,max}}{R_{VI} I_{Comp}}\right) \tag{4.6}$$

$$-V_{REFn} = \eta U_T \ln\left(1 + \frac{v_{lin,min}}{R_{VI} I_{Comp}}\right) \tag{4.7}$$

Rearranged

$$v_{lin,max} = R_{VI} I_{Comp} \left(e^{\frac{V_{REFp}}{\eta U_T}} - 1 \right) \tag{4.8}$$

$$v_{lin,min} = R_{VI} I_{Comp} \left(e^{\frac{V_{-REFn}}{\eta U_T}} - 1 \right) \tag{4.9}$$

Finally, substituting (4.4), (4.8), and (4.9) into (4.5), and simplifying

$$\Delta_c = \alpha \ln \left(\frac{e^{\frac{-V_{REFn}}{\alpha}} + \frac{c}{M}(e^{\frac{V_{REFp}}{\alpha}} - e^{\frac{-V_{REFn}}{\alpha}})}{e^{\frac{-V_{REFn}}{\alpha}} + \frac{c-1}{M}(e^{\frac{V_{REFp}}{\alpha}} - e^{\frac{-V_{REFn}}{\alpha}})} \right) \qquad c = 1, ..., M \tag{4.10}$$

where $\alpha = \eta U_T$ is a technology dependant parameter.

The resulting step-sizes can be re-expressed as

$$\Delta_c = \alpha \ln \left(\frac{\gamma_n + \frac{c}{M}(\gamma_p - \gamma_n)}{\gamma_n + \frac{c-1}{M}(\gamma_p - \gamma_n)} \right) \qquad c = 1, ..., M \tag{4.11}$$

where

$$\gamma_p = e^{\frac{V_{REFp}}{\alpha}} \qquad \gamma_n = e^{\frac{-V_{REFn}}{\alpha}} \tag{4.12}$$

Observing (4.6) - (4.7) and (4.11) - (4.12), the following quantization and digital-to-

analog-conversion requirements are derived for mapping of classical $\Delta\Sigma$ modulator architectures to the log-domain:

1. Scaling of the quantizer and DAC reference voltages by logarithmic factors, as described in (4.6) and (4.7).

2. Generating the required step-sizes:

   (a) In single-bit designs (Fig. 4.2), generating a single non-uniform quantizer and DAC threshold voltage V_M.

   (b) In multibit designs (Fig. 4.3), generating non-uniform quantizer step-sizes and nonuniform DAC output-level spacing, as described in (4.11) and (4.12).

As illustrated in Fig. 4.2 for a single-bit modulator, by carefully selecting V_{REFp} and V_{REFn}, and the threshold voltage V_M, a single-bit log-domain $\Delta\Sigma$ modulator architecture satisfies the first and second requirements.

In contrast, multibit log-domain $\Delta\Sigma$ modulators necessitate realization of the significantly more challenging last condition. To realize a multibit quantizer having the nonuniform step-sizes in (4.11), or a multibit DAC having the nonuniform output-level spacing in (4.11), non-uniformly-sized resistors or current sources are required. Implementing components related by the logarithmic nature in (4.11) makes the relative sizes of these nonuniform components highly sensitive to process and temperature variations. Additionally, fabrication layout techniques proposed to minimize the component mismatch errors resulting from process variations are only effective for uniformly-sized components.

Accordingly, in the following section, a novel architecture is proposed to realize a log-domain $\Delta\Sigma$ modulator with a multibit quantizer and DAC, having reduced sensitivity to process variations and, hence, practically implementable in standard CMOS processes.

4.2 Proposed Multibit Log-Domain ΔΣ Modulator

In Section 4.2.1, a multibit log-domain ΔΣ modulator architecture is proposed that overcomes the challenges demonstrated in Section 4.1. A class AB log-domain ΔΣ modulator loop-filter realization is presented in Section 4.2.2.

4.2.1 Architecture

To overcome the challenges demonstrated in the previous section, Fig. 4.4 proposes a multibit log-domain ΔΣ modulator whose multibit quantizer and DAC can be practically implemented in standard CMOS processes. Here, compared to Fig. 4.3, a log-domain expander is inserted at the output of the log-domain ΔΣ loop-filter. Thus, the log-domain quantizer in Fig. 4.3 can be realized using a classical quantizer with uniform step-sizes, as shown in Fig. 4.4. Similarly, a log-domain compressor is inserted in the ΔΣ feedback path. Thus, the log-domain DAC in Fig. 4.3 can be realized using a classical multibit DAC with uniformly-spaced output levels, as shown in Fig. 4.4.

Observe that, together, the uniform multibit quantizer and the expander in Fig. 4.4. can be viewed to form a multibit log-domain quantizer (i.e., a quantizer with logarithmically-spaced input threshold voltages). Similarly, together, the uniform multibit DAC and the compressor in Fig. 4.4. can be viewed to form a log-domain multibit DAC (i.e., a DAC with logarithmically-spaced output-levels).

Alternatively, the log-domain loop-filter in Fig. 4.4., together with the compressor and the expander inside the ΔΣ feedback loop, can be viewed as a classical (linear) ΔΣ loop-filter.

The proposed architecture satisfies the 1st and 2nd design requirements outlined in Section 4.1 for multibit log-domain ΔΣ modulators; by selecting the upper and lower limits of the uniform multibit quantizer based on the ΔΣ modulator requirements and implementing the quantizer and DAC using uniform-sized elements, the realization of V_{REFp}, V_{REFn}, and

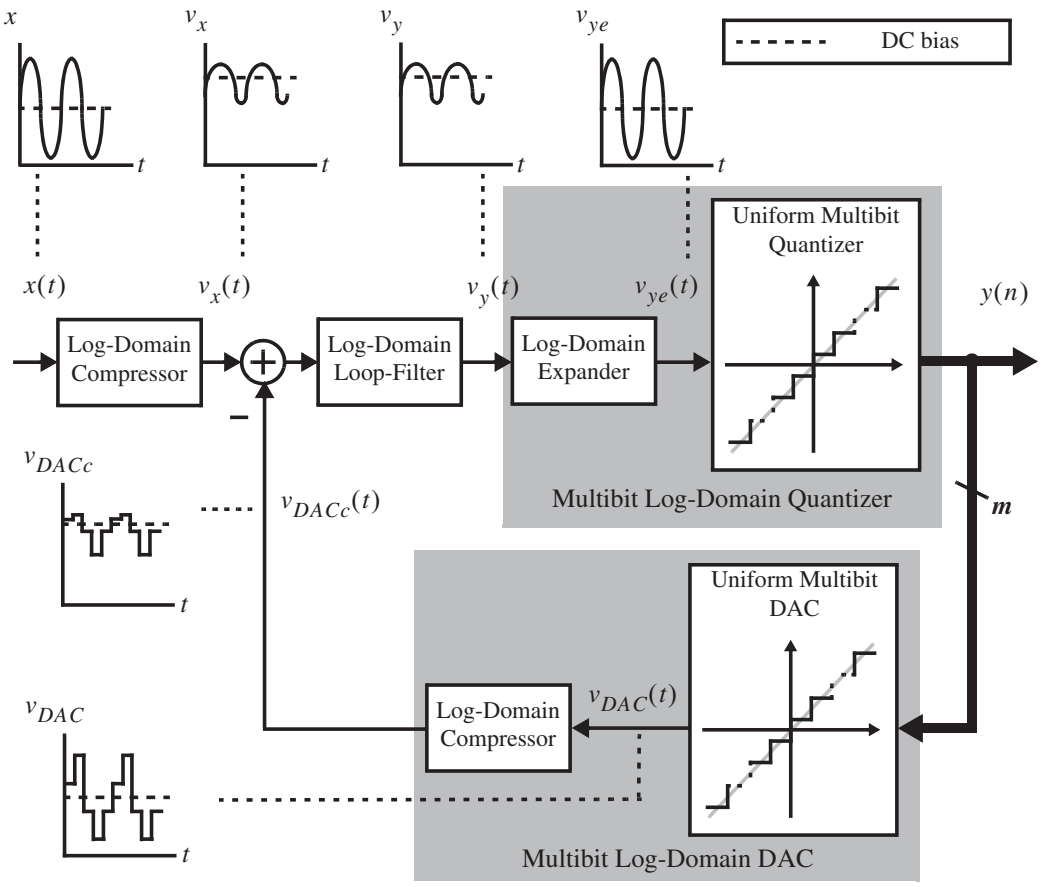


Figure 4.4: Proposed multibit log-domain ΔΣ modulator, using a classical (uniform) multibit quantizer and DAC.

the step-sizes is easily achieved and with significantly increased accuracy.

4.2.2 Proposed Class AB Loop-Filter Realization

As outlined in Section 3.2, class AB operation is particularly advantageous in log-domain systems. In this section, the first architecture-level design of a class AB log-domain ΔΣ modulator is presented.

Figure 4.5 depicts a classical realization of a 3rd-order multibit distributed-feedback ΔΣ modulator, described by the loop-filter transfer function (from the DAC output to the

quantizer input) [Ort06]

$$LF = -\left(\frac{a_3\, f_s}{s} + \frac{a_2\, f_s^2}{s^2} + \frac{a_1\, f_s^3}{s^3}\right) \tag{4.13}$$

where f_s represents the sampling frequency of the quantizer.

Figure 4.6 depicts the proposed class AB log-domain realization, based on the proposed architecture (Fig. 4.4) for multibit log-domain $\Delta\Sigma$ modulators. The presented loop-filter architecture is the first class AB realization of a log-domain $\Delta\Sigma$ modulator.

In Fig. 4.6, the voltage-to-current (V/I) and current-to-voltage (I/V) conversions can be performed using a simple resistor. The compressors and expander are characterized by the operating equations (3.5) and (3.7), respectively. Here, the class AB integrator is characterized by the following operating equations

$$\begin{aligned} i_{Cp} &= C\frac{dv_{Cp}}{dt} \\ &= I_{Int}\,(e^{\frac{v_{inA}-v_{Cp}}{\eta\, U_T}} - e^{\frac{v_{fbA}-v_{Cp}}{\eta\, U_T}}) \\ &\quad -I_{Int}\,(e^{\frac{v_{inB}-v_{Cp}}{\eta\, U_T}} - e^{\frac{v_{fbB}-v_{Cp}}{\eta\, U_T}}) \end{aligned} \tag{4.14}$$

$$\begin{aligned} i_{Cn} &= C\frac{dv_{Cn}}{dt} \\ &= I_{Int}\,(e^{\frac{v_{inB}-v_{Cn}}{\eta\, U_T}} - e^{\frac{v_{fbB}-v_{Cn}}{\eta\, U_T}}) \\ &\quad -I_{Int}\,(e^{\frac{v_{inA}-v_{Cn}}{\eta\, U_T}} - e^{\frac{v_{fbA}-v_{Cn}}{\eta\, U_T}}) \end{aligned} \tag{4.15}$$

where I_{Int} is the bias current of the integrator, and i_C and v_C respectively denote the signal current through, and voltage signal across, the integrating capacitor. The signal v_{in} represents the positive integrator input, while v_{fb} represents the feedback input, as indicated in Fig. 4.6. Here, the subscripts p and n denote the differential nodes in the architecture.

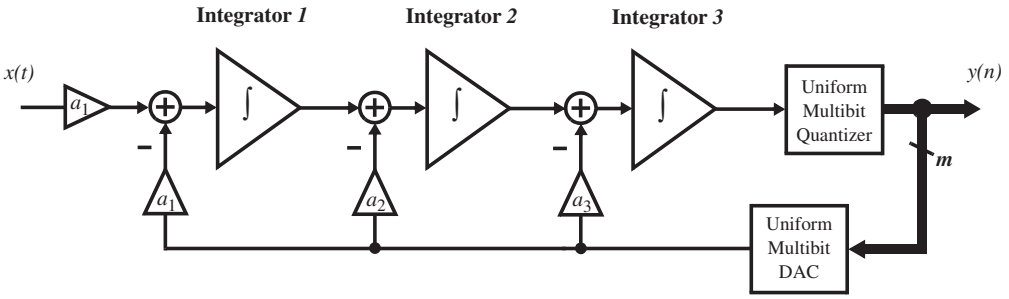


Figure 4.5: Third-order classical distributed-feedback ΔΣ modulator.

In the following subsections, the design procedure to generate a log-domain ΔΣ modulator is presented. Specifically, the following design steps are outlined:

- Derivation of the log-domain ΔΣ modulator loop-filter transfer function, and confirmation of the input-output linearity of the proposed loop-filter.
- Derivation of the relationship relating the log-domain loop-filter coefficients to their classical continuous-time counterparts.
- Evaluation of the coefficients of the log-domain loop-filter for a targeted NTF.

Derivation of the Loop-Filter Transfer Function

Assuming a 3rd-order ΔΣ modulator as shown in Fig. 4.6 with the first, second, and third integrator biased at currents I_{Int1}, I_{Int2}, and I_{Int3} respectively, and an expander and compressors biased at currents I_{Exp}, I_{Comp1}, I_{Comp2}, the loop-filter transfer function (from the DAC output v_{DAC} to the quantizer input v_{ye}) of the log-domain ΔΣ modulator in Fig. 4.6 can be derived as follows. Here, C_1, C_2, and C_3 represent the integrating capacitors of the log-domain integrators in Fig 4.6.

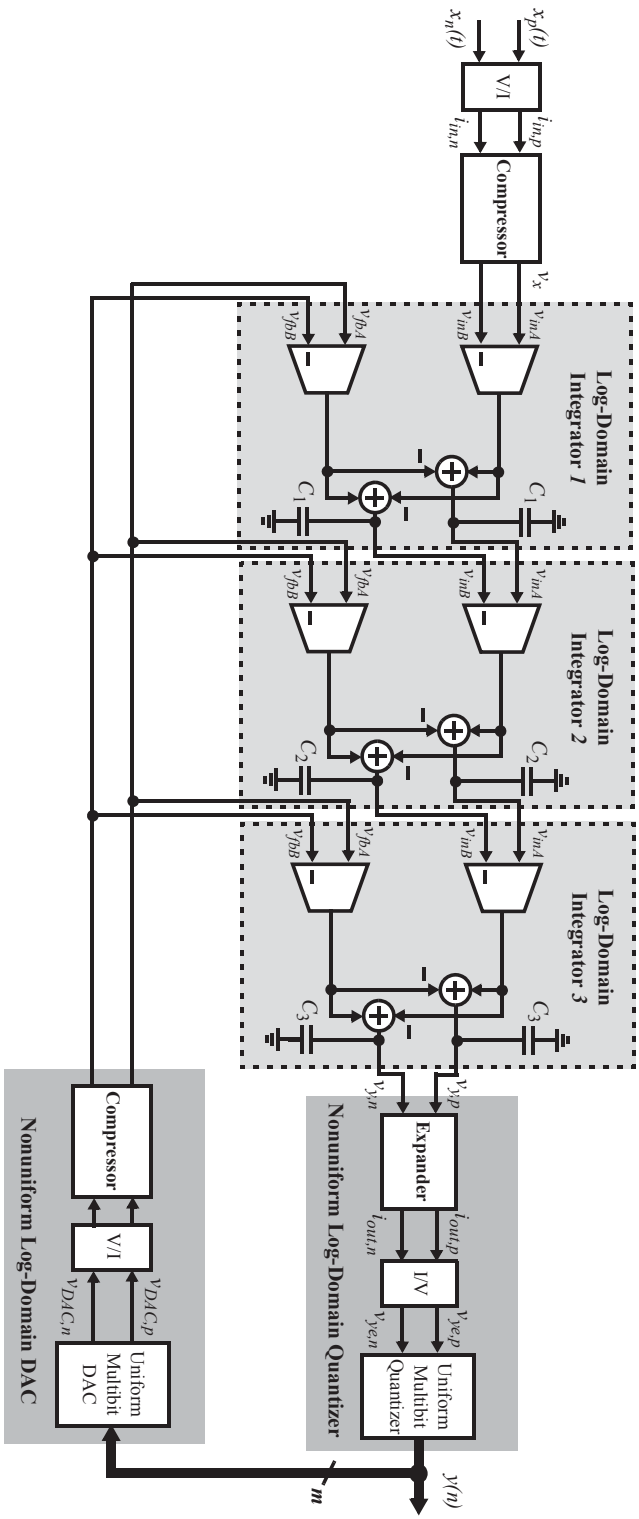


Figure 4.6: Third-order class AB multibit log-domain ΔΣ modulator based on the proposed architecture (in Fig. 4.4).

The current signals appearing at the outputs of the 1st integrator are given by

$$\begin{aligned} i_{C1p} &= C_1 \frac{dv_{C1p}}{dt} \\ &= I_{Int1}\,(-e^{\frac{v_{Comp2p} - v_{C1p}}{\eta\, U_T}}) \\ &\quad -I_{Int1}\,(-e^{\frac{v_{Comp2n} - v_{C1p}}{\eta\, U_T}}) \end{aligned} \tag{4.16}$$

$$\begin{aligned} i_{C1n} &= C_1 \frac{dv_{C1n}}{dt} \\ &= I_{Int1}\,(-e^{\frac{v_{Comp2n} - v_{C1n}}{\eta\, U_T}}) \\ &\quad -I_{Int1}\,(-e^{\frac{v_{Comp2p} - v_{C1n}}{\eta\, U_T}}) \end{aligned} \tag{4.17}$$

Similarly, for the 2nd and 3rd integrators

$$\begin{aligned} i_{C2p} &= C_2 \frac{dv_{C2p}}{dt} \\ &= I_{Int2}\,(e^{\frac{v_{C1p} - v_{C2p}}{\eta\, U_T}} - e^{\frac{v_{Comp2p} - v_{C2p}}{\eta\, U_T}}) \\ &\quad -I_{Int2}\,(e^{\frac{v_{C1n} - v_{C2p}}{\eta\, U_T}} - e^{\frac{v_{Comp2n} - v_{C2p}}{\eta\, U_T}}) \end{aligned} \tag{4.18}$$

$$\begin{aligned} i_{C2n} &= C_2 \frac{dv_{C2n}}{dt} \\ &= I_{Int2}\,(e^{\frac{v_{C1n} - v_{C2n}}{\eta\, U_T}} - e^{\frac{v_{Comp2n} - v_{C2n}}{\eta\, U_T}}) \\ &\quad -I_{Int2}\,(e^{\frac{v_{C1p} - v_{C2n}}{\eta\, U_T}} - e^{\frac{v_{Comp2p} - v_{C2n}}{\eta\, U_T}}) \end{aligned} \tag{4.19}$$

$$\begin{aligned} i_{C3p} &= C_3\frac{dv_{C3p}}{dt} \\ &= I_{Int3}\,(e^{\frac{v_{C2p}-v_{C3p}}{\eta\,U_T}} - e^{\frac{v_{Comp2p}-v_{C3p}}{\eta\,U_T}}) \\ &\quad -I_{Int3}\,(e^{\frac{v_{C2n}-v_{C3p}}{\eta\,U_T}} - e^{\frac{v_{Comp2n}-v_{C3p}}{\eta\,U_T}}) \end{aligned} \tag{4.20}$$

$$\begin{aligned} i_{C3n} &= C_3\frac{dv_{C3n}}{dt} \\ &= I_{Int3}\,(e^{\frac{v_{C2n}-v_{C3n}}{\eta\,U_T}} - e^{\frac{v_{Comp2n}-v_{C3n}}{\eta\,U_T}}) \\ &\quad -I_{Int3}\,(e^{\frac{v_{C2p}-v_{C3n}}{\eta\,U_T}} - e^{\frac{v_{Comp2p}-v_{C3n}}{\eta\,U_T}}) \end{aligned} \tag{4.21}$$

Multiplying (4.20) through by $e^{\frac{v_{C3p}}{\eta\,U_T}}$, and (4.21) through by $e^{\frac{v_{C3n}}{\eta\,U_T}}$

$$\begin{aligned} C_3\frac{dv_{C3p}}{dt}\,e^{\frac{v_{C3p}}{\eta\,U_T}} &= I_{Int3}\,(e^{\frac{v_{C2p}}{\eta\,U_T}} - e^{\frac{v_{Comp2p}}{\eta\,U_T}}) \\ &\quad -I_{Int3}\,(e^{\frac{v_{C2n}}{\eta\,U_T}} - e^{\frac{v_{Comp2n}}{\eta\,U_T}}) \end{aligned} \tag{4.22}$$

$$\begin{aligned} C_3\frac{dv_{C3n}}{dt}\,e^{\frac{v_{C3n}}{\eta\,U_T}} &= I_{Int3}\,(e^{\frac{v_{C2n}}{\eta\,U_T}} - e^{\frac{v_{Comp2n}}{\eta\,U_T}}) \\ &\quad -I_{Int3}\,(e^{\frac{v_{C2p}}{\eta\,U_T}} - e^{\frac{v_{Comp2p}}{\eta\,U_T}}) \end{aligned} \tag{4.23}$$

The signals at the input of the quantizer, $v_{ye,p}$ and $v_{ye,n}$ are derived from the expanded signals, $i_{out,p}$ and $i_{out,n}$, respectively, at the output of the third log-domain integrator. Assuming I/V conversion resistors R_{IV} at the outputs of the expander, and utilizing the ex-

pander equation (3.7), then

$$v_{ye,p} = R_{IV}\, i_{out,p} = R_{IV}(I_{Exp}\, e^{\frac{v_{C3p}}{\eta U_T}} - I_{Exp}) \tag{4.24}$$

$$v_{ye,n} = R_{IV}\, i_{out,n} = R_{IV}(I_{Exp}\, e^{\frac{v_{C3n}}{\eta U_T}} - I_{Exp}) \tag{4.25}$$

Differentiating and rearranging (4.24), the following equation relating v_{C3p} to $v_{ye,p}$ is derived

$$e^{\frac{v_{C3p}}{\eta U_T}}\, \frac{dv_{C3p}}{dt} = \frac{\eta\, U_T}{R_{IV}\, I_{Exp}} \left(\frac{dv_{ye,p}}{dt} \right) \tag{4.26}$$

Similarly, differentiating and rearranging (4.25)

$$e^{\frac{v_{C3n}}{\eta U_T}}\, \frac{dv_{C3n}}{dt} = \frac{\eta\, U_T}{R_{IV}\, I_{Exp}} \left(\frac{dv_{ye,n}}{dt} \right) \tag{4.27}$$

The signals at the outputs of the 2nd compressor are derived from the signals at the uniform-step DAC outputs, $v_{DAC,p}$ and $v_{DAC,n}$. Assuming V/I conversion resistors R_{VI} at the inputs of the 2nd compressor, and utilizing the compressor equation (3.5), then

$$i_{Comp2,inp} = \frac{v_{DAC,p}}{R_{VI}} \tag{4.28}$$

$$v_{Comp2p} = \eta\, U_T\, ln \left(1 + \frac{i_{Comp2,inp}}{I_{Comp2}} \right) \tag{4.29}$$

Inserting (4.28) into (4.29)

$$v_{Comp2p} = \eta\, U_T\, ln \left(1 + \frac{v_{DAC,p}}{I_{Comp2}\, R_{VI}} \right) \tag{4.30}$$

Rearranging and applying the exponential function results in the following equation relating

v_{Comp2p} to $v_{DAC,p}$

$$e^{\frac{v_{Comp2p}}{\eta\, U_T}} = 1 + \frac{v_{DAC,p}}{I_{Comp2}\, R_{VI}} \tag{4.31}$$

Similarly

$$e^{\frac{v_{Comp2n}}{\eta\, U_T}} = 1 + \frac{v_{DAC,n}}{I_{Comp2}\, R_{VI}} \tag{4.32}$$

Inserting (4.26), (4.31), and (4.32) into (4.22)

$$\begin{aligned} C_3 \left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}}\right)\left(\frac{dv_{ye,p}}{dt}\right) &= I_{Int3}\, e^{\frac{v_{C2p}}{\eta\, U_T}} - I_{Int3}\, e^{\frac{v_{C2n}}{\eta\, U_T}} \\ &\quad - I_{Int3}\left(1 + \frac{v_{DAC,p}}{I_{Comp2}\, R_{VI}}\right) \\ &\quad + I_{Int3}\left(1 + \frac{v_{DAC,n}}{I_{Comp2}\, R_{VI}}\right) \end{aligned} \tag{4.33}$$

Similarly, inserting (4.27), (4.31), and (4.32) into (4.23)

$$\begin{aligned} C_3 \left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}}\right)\left(\frac{dv_{ye,n}}{dt}\right) &= I_{Int3}\, e^{\frac{v_{C2n}}{\eta\, U_T}} - I_{Int3}\, e^{\frac{v_{C2p}}{\eta\, U_T}} \\ &\quad - I_{Int3}\left(1 + \frac{v_{DAC,n}}{I_{Comp2}\, R_{VI}}\right) \\ &\quad + I_{Int3}\left(1 + \frac{v_{DAC,p}}{I_{Comp2}\, R_{VI}}\right) \end{aligned} \tag{4.34}$$

Differentiating (4.33) and (4.34)

$$\begin{aligned} C_3 \left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}}\right)\left(\frac{dv^2_{ye,p}}{dt}\right) &= \frac{I_{Int3}}{\eta\, U_T}\left(e^{\frac{v_{C2p}}{\eta\, U_T}}\frac{dv_{C2p}}{dt} - e^{\frac{v_{C2n}}{\eta\, U_T}}\frac{dv_{C2n}}{dt}\right) \\ &\quad - \frac{I_{Int3}}{I_{Comp2}\, R_{VI}}\left(\frac{dv_{DAC,p}}{dt} - \frac{dv_{DAC,n}}{dt}\right) \end{aligned} \tag{4.35}$$

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,n}^2}{dt}\right) = \frac{I_{Int3}}{\eta\,U_T}\left(e^{\frac{v_{C2n}}{\eta\,U_T}}\frac{dv_{C2n}}{dt} - e^{\frac{v_{C2p}}{\eta\,U_T}}\frac{dv_{C2p}}{dt}\right) - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,n}}{dt} - \frac{dv_{DAC,p}}{dt}\right) \quad (4.36)$$

Multiplying (4.18) through by $e^{\frac{v_{C2p}}{\eta\,U_T}}$, and (4.19) through by $e^{\frac{v_{C2n}}{\eta\,U_T}}$

$$C_2\frac{dv_{C2p}}{dt}\,e^{\frac{v_{C2p}}{\eta\,U_T}} = I_{Int2}\left(e^{\frac{v_{C1p}}{\eta\,U_T}} - e^{\frac{v_{C1n}}{\eta\,U_T}}\right) - I_{Int2}\left(e^{\frac{v_{Comp2p}}{\eta\,U_T}} - e^{\frac{v_{Comp2n}}{\eta\,U_T}}\right) \quad (4.37)$$

$$C_2\frac{dv_{C2n}}{dt}\,e^{\frac{v_{C2n}}{\eta\,U_T}} = I_{Int2}\left(e^{\frac{v_{C1n}}{\eta\,U_T}} - e^{\frac{v_{C1p}}{\eta\,U_T}}\right) - I_{Int2}\left(e^{\frac{v_{Comp2n}}{\eta\,U_T}} - e^{\frac{v_{Comp2p}}{\eta\,U_T}}\right) \quad (4.38)$$

Rearranging (4.37) and (4.38), and inserting into (4.35) and (4.36)

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,p}^2}{dt}\right) = \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,\eta\,U_T}\left(e^{\frac{v_{C1p}}{\eta\,U_T}} - e^{\frac{v_{C1n}}{\eta\,U_T}}\right) - \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,\eta\,U_T}\left(e^{\frac{v_{Comp2p}}{\eta\,U_T}} - e^{\frac{v_{Comp2n}}{\eta\,U_T}}\right) - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,p}}{dt} - \frac{dv_{DAC,n}}{dt}\right) \quad (4.39)$$

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,n}^2}{dt}\right) = \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,\eta\,U_T}\left(e^{\frac{v_{C1n}}{\eta\,U_T}} - e^{\frac{v_{C1p}}{\eta\,U_T}}\right) - \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,\eta\,U_T}\left(e^{\frac{v_{Comp2n}}{\eta\,U_T}} - e^{\frac{v_{Comp2p}}{\eta\,U_T}}\right) - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,n}}{dt} - \frac{dv_{DAC,p}}{dt}\right) \tag{4.40}$$

Differentiating (4.39) and (4.40)

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,p}^3}{dt}\right) = \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,(\eta\,U_T)^2}\left(e^{\frac{v_{C1p}}{\eta\,U_T}}\,\frac{dv_{C1p}}{dt} - e^{\frac{v_{C1n}}{\eta\,U_T}}\,\frac{dv_{C1n}}{dt}\right) - \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,(\eta\,U_T)^2}\,e^{\frac{v_{Comp2p}}{\eta\,U_T}}\,\frac{dv_{Comp2p}}{dt} + \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,(\eta\,U_T)^2}\,e^{\frac{v_{Comp2n}}{\eta\,U_T}}\,\frac{dv_{Comp2n}}{dt} - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,p}^2}{dt} - \frac{dv_{DAC,n}^2}{dt}\right) \tag{4.41}$$

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,n}^3}{dt}\right) = \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,(\eta\,U_T)^2}\left(e^{\frac{v_{C1n}}{\eta\,U_T}}\,\frac{dv_{C1n}}{dt} - e^{\frac{v_{C1p}}{\eta\,U_T}}\,\frac{dv_{C1p}}{dt}\right) - \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,(\eta\,U_T)^2}\,e^{\frac{v_{Comp2n}}{\eta\,U_T}}\,\frac{dv_{Comp2n}}{dt} + \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,(\eta\,U_T)^2}\,e^{\frac{v_{Comp2p}}{\eta\,U_T}}\,\frac{dv_{Comp2p}}{dt} - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,n}^2}{dt} - \frac{dv_{DAC,p}^2}{dt}\right) \tag{4.42}$$

Multiplying (4.16) through by $e^{\frac{v_{C1p}}{\eta U_T}}$, and (4.17) through by $e^{\frac{v_{C1n}}{\eta U_T}}$

$$C_1 \frac{dv_{C1p}}{dt} e^{\frac{v_{C1p}}{\eta U_T}} = -I_{Int1} \left(e^{\frac{v_{Comp2p}}{\eta U_T}} - e^{\frac{v_{Comp2n}}{\eta U_T}} \right) \tag{4.43}$$

$$C_1 \frac{dv_{C1n}}{dt} e^{\frac{v_{C1n}}{\eta U_T}} = -I_{Int1} \left(e^{\frac{v_{Comp2n}}{\eta U_T}} - e^{\frac{v_{Comp2p}}{\eta U_T}} \right) \tag{4.44}$$

Differentiating (4.31) and (4.32), and rearranging

$$e^{\frac{v_{Comp2p}}{\eta U_T}} \frac{dv_{Comp2p}}{dt} = \frac{\eta U_T}{I_{Comp2} R_{VI}} \frac{dv_{DAC,p}}{dt} \tag{4.45}$$

$$e^{\frac{v_{Comp2n}}{\eta U_T}} \frac{dv_{Comp2n}}{dt} = \frac{\eta U_T}{I_{Comp2} R_{VI}} \frac{dv_{DAC,n}}{dt} \tag{4.46}$$

Inserting (4.43), (4.44), (4.45), and (4.46) into (4.41) and (4.42)

$$\begin{aligned} C_3 \left(\frac{\eta U_T}{I_{Exp} R_{IV}} \right) \left(\frac{dv_{ye,p}^3}{dt} \right) = & -\frac{4 I_{Int3} I_{Int2} I_{Int1}}{C_2 C_1 (\eta U_T)^2} e^{\frac{v_{Comp2p}}{\eta U_T}} \\ & + \frac{4 I_{Int3} I_{Int2} I_{Int1}}{C_2 C_1 (\eta U_T)^2} e^{\frac{v_{Comp2n}}{\eta U_T}} \\ & - \frac{2 I_{Int3} I_{Int2}}{C_2 I_{Comp2} R_{VI} \eta U_T} \left(\frac{dv_{DAC,p}}{dt} - \frac{dv_{DAC,n}}{dt} \right) \\ & - \frac{I_{Int3}}{I_{Comp2} R_{VI}} \left(\frac{dv_{DAC,p}^2}{dt} - \frac{dv_{DAC,n}^2}{dt} \right) \end{aligned} \tag{4.47}$$

$$
\begin{aligned}
C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,n}^3}{dt}\right) &= -\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,(\eta\,U_T)^2}\,e^{\frac{v_{Comp2n}}{\eta\,U_T}} \\
&\quad +\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,(\eta\,U_T)^2}\,e^{\frac{v_{Comp2p}}{\eta\,U_T}} \\
&\quad -\frac{2\,I_{Int3}\,I_{Int2}}{C_2\,I_{Comp2}\,R_{VI}\,\eta\,U_T}\left(\frac{dv_{DAC,n}}{dt}-\frac{dv_{DAC,p}}{dt}\right) \\
&\quad -\frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,n}^2}{dt}-\frac{dv_{DAC,p}^2}{dt}\right)
\end{aligned}
\tag{4.48}
$$

Differentiating (4.47) and (4.48)

$$
\begin{aligned}
C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,p}^4}{dt}\right) &= -\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,(\eta\,U_T)^3}\,e^{\frac{v_{Comp2p}}{\eta\,U_T}}\,\frac{dv_{Comp2p}}{dt} \\
&\quad +\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,(\eta\,U_T)^3}\,e^{\frac{v_{Comp2n}}{\eta\,U_T}}\,\frac{dv_{Comp2n}}{dt} \\
&\quad -\frac{2\,I_{Int3}\,I_{Int2}}{C_2\,I_{Comp2}\,R_{VI}\,\eta\,U_T}\left(\frac{dv_{DAC,p}^2}{dt}-\frac{dv_{DAC,n}^2}{dt}\right) \\
&\quad -\frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,p}^3}{dt}-\frac{dv_{DAC,n}^3}{dt}\right)
\end{aligned}
\tag{4.49}
$$

$$
\begin{aligned}
C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv_{ye,n}^4}{dt}\right) &= -\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,(\eta\,U_T)^3}\,e^{\frac{v_{Comp2n}}{\eta\,U_T}}\,\frac{dv_{Comp2n}}{dt} \\
&\quad +\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,(\eta\,U_T)^3}\,e^{\frac{v_{Comp2p}}{\eta\,U_T}}\,\frac{dv_{Comp2p}}{dt} \\
&\quad -\frac{2\,I_{Int3}\,I_{Int2}}{C_2\,I_{Comp2}\,R_{VI}\,\eta\,U_T}\left(\frac{dv_{DAC,n}^2}{dt}-\frac{dv_{DAC,p}^2}{dt}\right) \\
&\quad -\frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC,n}^3}{dt}-\frac{dv_{DAC,p}^3}{dt}\right)
\end{aligned}
\tag{4.50}
$$

Inserting (4.45) and (4.46) into (4.49) and (4.50)

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv^4_{ye,p}}{dt}\right) = -\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,I_{Comp2p}\,R_{VI}\,(\eta\,U_T)^2}\left(\frac{dv_{DAC,p}}{dt}-\frac{dv_{DAC,n}}{dt}\right) - \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,I_{Comp2}\,R_{VI}\,\eta\,U_T}\left(\frac{dv^2_{DAC,p}}{dt}-\frac{dv^2_{DAC,n}}{dt}\right) - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv^3_{DAC,p}}{dt}-\frac{dv^3_{DAC,n}}{dt}\right) \tag{4.51}$$

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv^4_{ye,n}}{dt}\right) = -\frac{4\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,I_{Comp2n}\,R_{VI}\,(\eta\,U_T)^2}\left(\frac{dv_{DAC,n}}{dt}-\frac{dv_{DAC,p}}{dt}\right) - \frac{2\,I_{Int3}\,I_{Int2}}{C_2\,I_{Comp2}\,R_{VI}\,\eta\,U_T}\left(\frac{dv^2_{DAC,n}}{dt}-\frac{dv^2_{DAC,p}}{dt}\right) - \frac{I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv^3_{DAC,n}}{dt}-\frac{dv^3_{DAC,p}}{dt}\right) \tag{4.52}$$

Subtracting (4.52) from (4.53), and recognizing that $d/dt(x) - d/dt(y) = d/dt(x-y)$

$$C_3\left(\frac{\eta\,U_T}{I_{Exp}\,R_{IV}}\right)\left(\frac{dv^4_{ye}}{dt}\right) = -\frac{8\,I_{Int3}\,I_{Int2}\,I_{Int1}}{C_2\,C_1\,I_{Comp2p}\,R_{VI}\,(\eta\,U_T)^2}\left(\frac{dv_{DAC}}{dt}\right) - \frac{4\,I_{Int3}\,I_{Int2}}{C_2\,I_{Comp2}\,R_{VI}\,\eta\,U_T}\left(\frac{dv^2_{DAC}}{dt}\right) - \frac{2\,I_{Int3}}{I_{Comp2}\,R_{VI}}\left(\frac{dv^3_{DAC}}{dt}\right) \tag{4.53}$$

where $v_{ye} = v_{ye,p} - v_{ye,n}$ and $v_{DAC} = v_{DAC,p} - v_{DAC,n}$. Rearranging (4.53), and dividing through by $\frac{C_3\,\eta\,U_T}{I_{Exp}\,R_{IV}}$

$$\frac{dv^4_{ye}}{dt} = -\frac{2\,I_{Int3}\,I_{Exp}\,R_{IV}}{\eta\,U_T\,C_3\,I_{Comp2}\,R_{VI}}\left(\frac{dv^3_{DAC}}{dt}\right) - \frac{4\,I_{Int3}\,I_{Int2}\,I_{Exp}\,R_{IV}}{(\eta\,U_T)^2\,C_3\,C_2\,I_{Comp2}\,R_{VI}}\left(\frac{dv^2_{DAC}}{dt}\right) - \frac{8\,I_{Int3}\,I_{Int2}\,I_{Int1}\,I_{Exp}\,R_{IV}}{(\eta\,U_T)^3\,C_3\,C_2\,C_1\,I_{Comp2}\,R_{VI}}\left(\frac{dv_{DAC}}{dt}\right) \tag{4.54}$$

Applying the Laplace transform to both sides of (4.54), and rearranging

$$\begin{aligned} LF &\equiv \frac{V_{ye}(s)}{V_{DAC}(s)}\Bigg|_{x=0} \\ &= -\frac{2\,I_{Int3}\,I_{Exp}\,R_{IV}}{\eta\,U_T\,C_3\,I_{Comp2}\,R_{VI}}\left(\frac{1}{s}\right) \\ &\quad -\frac{4\,I_{Int3}\,I_{Int2}\,I_{Exp}\,R_{IV}}{(\eta\,U_T)^2\,C_3\,C_2\,I_{Comp2}\,R_{VI}}\left(\frac{1}{s^2}\right) \\ &\quad -\frac{8\,I_{Int3}\,I_{Int2}\,I_{Int1}\,I_{Exp}\,R_{IV}}{(\eta\,U_T)^3\,C_3\,C_2\,C_1\,I_{Comp2}\,R_{VI}}\left(\frac{1}{s^3}\right) \end{aligned} \tag{4.55}$$

The loop-filter transfer function, LF, of the class AB log-domain $\Delta\Sigma$ modulator described by (4.55) can be expressed as

$$\begin{aligned} LF &\equiv \frac{V_{ye}(s)}{V_{DAC}(s)}\Bigg|_{x=0} \\ &= -\left(\frac{b_3}{s}+\frac{b_2}{s^2}+\frac{b_1}{s^3}\right) \end{aligned} \tag{4.56}$$

where

$$\begin{aligned} b_1 &= \frac{8\,I_{Int3}\,I_{Int2}\,I_{Int1}}{(\eta\,U_T)^3\,C_3\,C_2\,C_1}\left(\frac{I_{Exp}\,R_{IV}}{I_{Comp2}\,R_{VI}}\right) \\ &= \frac{8\,I_{Int3}\,I_{Int2}\,I_{Int1}}{(\eta\,U_T)^3\,C_3\,C_2\,C_1} \qquad \text{when} \quad I_{Exp}\,R_{IV} = I_{Comp2}\,R_{VI} \end{aligned} \tag{4.57}$$

$$\begin{aligned} b_2 &= \frac{4\,I_{Int3}\,I_{Int2}}{(\eta\,U_T)^2\,C_3\,C_2}\left(\frac{I_{Exp}\,R_{IV}}{I_{Comp2}\,R_{VI}}\right) \\ &= \frac{4\,I_{Int3}\,I_{Int2}}{(\eta\,U_T)^2\,C_3\,C_2} \qquad \text{when} \quad I_{Exp}\,R_{IV} = I_{Comp2}\,R_{VI} \end{aligned} \tag{4.58}$$

$$\begin{aligned} b_3 &= \frac{2\,I_{Int3}}{\eta\,U_T\,C_3}\left(\frac{I_{Exp}\,R_{IV}}{I_{Comp2}\,R_{VI}}\right) \\ &= \frac{2\,I_{Int3}}{\eta\,U_T\,C_3} \qquad \text{when} \quad I_{Exp}\,R_{IV} = I_{Comp2}\,R_{VI} \end{aligned} \tag{4.59}$$

Derivation of the Log-Domain $\Delta\Sigma$ Modulator Coefficients

The loop-filter transfer function in (4.56) - (4.59) demonstrates that the log-domain $\Delta\Sigma$ modulator in Fig. 4.6 is input-output linear. Furthermore, this loop-filter transfer function is equivalent to that of the classical (internally-linear) third-order $\Delta\Sigma$ modulator in Fig. 4.5, provided that the loop-filter integrator coefficients (4.57) - (4.57) are selected such that (4.56) is equal to (4.13). Accordingly, the proposed architecture in Fig. 4.4 enables realizing a multibit log-domain $\Delta\Sigma$ modulator whose NTF is equivalent to that realized by its classical internally-linear counterpart.

Specifically, observing (4.13) and (4.56) - (4.59), for the 3rd-order classical distributed-feedback continuous-time $\Delta\Sigma$ modulator (Fig. 4.5), a 3rd-order class AB log-domain $\Delta\Sigma$ modulator (Fig. 4.4) achieves an equivalent loop-filter response if the log-domain integrators are designed such that

$$\frac{I_{Int1}}{C_1} = \frac{a_1}{a_2}\frac{f_s}{2}\eta\, U_T \tag{4.60}$$

$$\frac{I_{Int2}}{C_2} = \frac{a_2}{a_3}\frac{f_s}{2}\eta\, U_T \tag{4.61}$$

$$\frac{I_{Int3}}{C_3} = a_3\frac{f_s}{2}\eta\, U_T \tag{4.62}$$

assuming $I_{Exp}\, R_{IV} = I_{Comp2}\, R_{VI}$.

Evaluation of the Log-Domain Coefficients

The architectures proposed and the relationships derived so far in this chapter can now be employed to construct a 3rd-order class AB log-domain $\Delta\Sigma$ modulator. First, a 3rd-order discrete-time $\Delta\Sigma$ modulator with a high-pass NTF with three transmission zeros at DC is

considered [1]

$$NTF(z) \;=\; (1-z^{-1})^3 \tag{4.63}$$

As outlined in [Ham04b], a discrete-time $\Delta\Sigma$ modulator with distributed feedback realizes (4.63) if the discrete-time integrator gains are set such that

$$g_1 = 1/3, \quad g_2 = 1, \quad g_3 = 3 \tag{4.64}$$

where $g_k (k = 1, ..., N)$ denotes the discrete-time integrator gains in [Ham04b].

The impulse-invariant transformation described in [Ort06] is utilized to determine the continuous-time coefficients (a_1, a_2, and a_3) of Fig. 4.5, needed to realize an equivalent continuous-time $\Delta\Sigma$ modulator NTF. In continuous-time $\Delta\Sigma$ modulators, the resulting coefficients are also dependant on the shape of the feedback DAC waveform. For a 3rd-order distributed feedback continuous-time modulator with a non-return-to-zero (NRZ) DAC waveform (similar to the switched-current DAC waveform in Fig. 2.7), the coefficients in Fig. 4.5 are derived through the following relationships, outlined in [Ort06].

$$a_1 \;=\; g_1\, g_2\, g_3 \;=\; 1 \tag{4.65}$$

$$a_2 \;=\; \frac{g_1\, g_2\, g_3}{2}\left(\frac{2}{g_1} - 2\right) = \; 2 \tag{4.66}$$

$$a_3 \;=\; \frac{g_1\, g_2\, g_3}{12}\left(-8 + \frac{6}{g_1} + \frac{12}{g_1}\left(\frac{1}{g_2} + g_1 - 1\right)\right) = \; 1.833 \tag{4.67}$$

[1] In continuous-time $\Delta\Sigma$ modulators, where the input signal is in continuous-time and the output signal is in discrete time, the modulator NTF cannot be defined directly as in discrete-time $\Delta\Sigma$ modulators [Ort06]. Therefore, equivalency of the proposed class AB log-domain modulators and traditional continuous-time modulators was demonstrated through the equivalent loop-filter transfer functions. Here, through outlining the design process, we demonstrate the proposed log-domain $\Delta\Sigma$ modulator's adherence to an equivalent discrete-time NTF.

Finally, for a sampling frequency f_s = 320 kHz, (4.60) - (4.60) are employed to determine the log-domain $\Delta\Sigma$ modulator parameters [2]

$$\frac{I_{Int1}}{C_1} = 2800, \quad \frac{I_{Int2}}{C_2} = 6109.09, \quad \frac{I_{Int3}}{C_3} = 10266.67 \tag{4.68}$$

4.3 Behavioural Modeling of Log-Domain $\Delta\Sigma$ Modulators

The first step in the design procedure of $\Delta\Sigma$ modulators has traditionally been behavioural modeling. This allows the designer to arrive at the design criteria (OSR, quantization and DAC bits, and loop-filter order) needed to achieve the targeted modulator resolution. Furthermore, by simulating the impact of circuit non-idealities, the design constraints of the circuit blocks are determined. Preliminary design through the use of high-level behavioural tools results in significant reduction in simulation time when compared to circuit-level simulations.

To investigate the behaviour of log-domain $\Delta\Sigma$ modulators in SIMULINK, models of the log-domain components that include various non-idealities are proposed. Figure 4.7 summarizes the SIMULINK model of the multibit log-domain $\Delta\Sigma$ modulator, as well as its individual blocks. The modeling details are presented in the following subsections.

4.3.1 Behavioural Model Coefficients

In a classical continuous-time $\Delta\Sigma$ modulator, the integrators in Fig. 4.5 are simply modeled as $1/s$ blocks (similarly, in discrete-time $\Delta\Sigma$ modulator modeling, the discrete-time integrators are implemented as $1/(1-z^{-1})$ blocks). These integrator blocks are readily available in the SIMULINK toolbox. In contrast, the implementation of log-domain components in SIMULINK necessitates the development of custom models which, as described in (4.14) and (4.15), are significantly more complex.

[2] In weak-inversion, the substrate factor η = 1.4 [Bin08]. The thermal potential U_T = 25 mV.

Differential-output discrete and continuous-time $\Delta\Sigma$ modulators are usually modeled behaviourally as single-ended systems to reduce model complexity and simulation time. The results of a single-ended behavioural simulation can easily be extended to a differential-output implementation as long as all components, including the quantizer and DAC, are implemented differentially during circuit-level realization. However, single-ended behavioural modeling of differential-ended systems requires an adjustment of the coefficients.

In this subsection, the objective is to re-interpret the differential-output results derived in (4.60) - (4.62) to achieve an equivalent loop-filter transfer function for a single-ended behavioural model.

The single-ended implementation of the integrator can be described by

$$\begin{aligned} i_C &= C\frac{dv_C}{dt} \\ &= I_{Int}\,(e^{\frac{v_{in}-v_C}{\eta\,U_T}} - k\,e^{\frac{v_{fb}-v_C}{\eta\,U_T}}) \end{aligned} \tag{4.69}$$

As derived in Appendix A, the resulting loop-filter transfer function of an equivalent single-ended system is described by

$$\begin{aligned} LF &\equiv \left.\frac{V_{ye}(s)}{V_{DAC}(s)}\right|_{x=0} \\ &= -\left(\frac{b_3}{s} + \frac{b_2}{s^2} + \frac{b_1}{s^3}\right) \end{aligned} \tag{4.70}$$

where

$$\begin{aligned} b_1 &= \frac{I_{Int3}\,I_{Int2}\,I_{Int1}}{(\eta\,U_T)^3\,C_3\,C_2\,C_1}\left(\frac{I_{Exp}\,R_{IV}}{I_{Comp2}\,R_{VI}}\right) \\ &= \frac{I_{Int3}\,I_{Int2}\,I_{Int1}}{(\eta\,U_T)^3\,C_3\,C_2\,C_1} \qquad \text{when} \quad I_{Exp}\,R_{IV} = I_{Comp2}\,R_{VI} \end{aligned} \tag{4.71}$$

Table 4.1: Integrators setup for the proposed 3rd-order class AB log-domain $\Delta\Sigma$ modulator and its equivalent behavioural model.

Differential-Output Log-domain Integrator	Single-Ended Behavioural Equivalent
$\frac{I_{Int1}}{C_1} = \frac{a_1}{a_2}\,\frac{f_s}{2}\,\eta\,U_T$	$\frac{I_{Int1}}{C_1} = \frac{a_1}{a_2}\,f_s\,\eta\,U_T$
$\frac{I_{Int2}}{C_2} = \frac{a_2}{a_3}\,\frac{f_s}{2}\,\eta\,U_T$	$\frac{I_{Int2}}{C_2} = \frac{a_2}{a_3}\,f_s\,\eta\,U_T$
$\frac{I_{Int3}}{C_3} = a_3\,\frac{f_s}{2}\,\eta\,U_T$	$\frac{I_{Int3}}{C_3} = a_3\,f_s\,\eta\,U_T$

$$\begin{aligned} b_2 &= \frac{I_{Int3}\,I_{Int2}}{(\eta\,U_T)^2\,C_3\,C_2}\left(\frac{I_{Exp}\,R_{IV}}{I_{Comp2}\,R_{VI}}\right) \\ &= \frac{I_{Int3}\,I_{Int2}}{(\eta\,U_T)^2\,C_3\,C_2} \qquad \text{when} \quad I_{Exp}\,R_{IV} = I_{Comp2}\,R_{VI} \end{aligned} \tag{4.72}$$

$$\begin{aligned} b_3 &= \frac{I_{Int3}}{\eta\,U_T\,C_3}\left(\frac{I_{Exp}\,R_{IV}}{I_{Comp2}\,R_{VI}}\right) \\ &= \frac{I_{Int3}}{\eta\,U_T\,C_3} \qquad \text{when} \quad I_{Exp}\,R_{IV} = I_{Comp2}\,R_{VI} \end{aligned} \tag{4.73}$$

Similar to the analysis presented in the last section, the integrator coefficients can be derived for the single-ended behavioural model. Table 4.1 summarizes the integrator setup for the proposed differential-output log-domain modulator and its equivalent single-ended behavioural model.

4.3.2 Modeling Varying Levels of Inversion

It has been assumed so far that the CMOS transistors generating the exponential equation in (3.1) are biased in weak-inversion. In reality, between weak-inversion operation characterized by (3.1) and strong-inversion operation characterized by the classical CMOS operating equation, a transistor may be biased in moderate-inversion [Tsi82]. To ease the analysis of CMOS devices over varying degrees of channel-inversion, the level of CMOS

channel-inversion can be characterized by a the fixed-normalized *inversion coefficient* IC approximation [Bin08]

$$IC = \frac{I_D}{2\,\eta_0\,\mu_0\,C_{ox}\,U_T^2\,\left(\frac{W}{L}\right)} \tag{4.74}$$

where η_0 and μ_0 are, respectively, the transistor's substrate factor in moderate inversion, and the transistor's low-field mobility.

For a CMOS transistor, the operating region can be summarized approximately as follows [Tsi82]: $IC < 0.1$ for weak-inversion performance, $0.1 < IC < 10$ for moderate-inversion performance, and $IC > 10$ for strong-inversion performance. A CMOS device biased in weak-inversion is prone to leaving the weak-inversion region and operating in the moderate-inversion region. This would result in a loss of the exponential relationship characterizing log-domain performance, introducing distortion.

While equations are available to characterize the performance of the CMOS transistor for each of the various operating regions, a CMOS transistor equation valid for all operating regions [Enz95] can be employed to describe the log-domain CMOS devices. This was demonstrated in [Pal03] for single-bit log-domain $\Delta\Sigma$ modulators. For CMOS devices in saturation, and using the source terminal as the reference instead of the substrate [Bin08]

$$i_D\,(\mathrm{WI}-\mathrm{SI}) = 2\,\eta\,\mu\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)\left(\ln\left(1+e^{\frac{v_{GS}-V_T}{2\,\eta\,U_T}}\right)\right)^2 \tag{4.75}$$

To model the effect of the transistor inversion-level on the performance of the proposed log-domain $\Delta\Sigma$ modulator, (4.75) was employed to re-derive the compressor, expander, and integrator operating equations for all regions of operation. The output of the compressor

block in Fig. 4.7 for all regions of operation is derived as

$$v_{comp}\,(\mathrm{WI}-\mathrm{SI}) \;=\; 2\,\eta\,U_T \ln\left(e^{\sqrt{\dfrac{i_{in}+I_{Comp}}{2\,\eta\,\mu\,C_{ox}\,U_T^2\left(\dfrac{W}{L}\right)}}}-1\right)-(V_{GS,Comp}-V_T) \tag{4.76}$$

The output of the expander in Fig. 4.7 is derived as

$$i_{exp}\,(\mathrm{WI}-\mathrm{SI}) \;=\; 2\,\eta\,\mu\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)\left(\ln\left(1+e^{\dfrac{v_{in}+(V_{GS,Exp}-V_T)}{2\,\eta\,U_T}}\right)\right)^2-I_{Exp} \tag{4.77}$$

Finally, the output voltage of the integrator in Fig. 4.7 is modeled by rearranging (4.75) and applying the Laplace transform, and is derived as

$$\begin{aligned} v_{C,Int}\,(\mathrm{WI}-\mathrm{SI}) \;=\; & \frac{1}{s\,C}\left(2\,\eta\,\mu\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)\left(\ln\left(1+e^{\dfrac{v_{in}-v_C+(V_{GS,Int}-V_T)}{2\,\eta\,U_T}}\right)\right)^2\right) \\ & -\frac{1}{s\,C}\left(2\,\eta\,\mu\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)\left(\ln\left(1+e^{\dfrac{v_{fb}-v_C+(V_{GS,Int}-V_T)}{2\,\eta\,U_T}}\right)\right)^2\right) \end{aligned} \tag{4.78}$$

The SIMULINK variables defined by the designer, and the variables in (4.76) - (4.78) evaluated within the SIMULINK blocks, are summarized in Table 4.2.

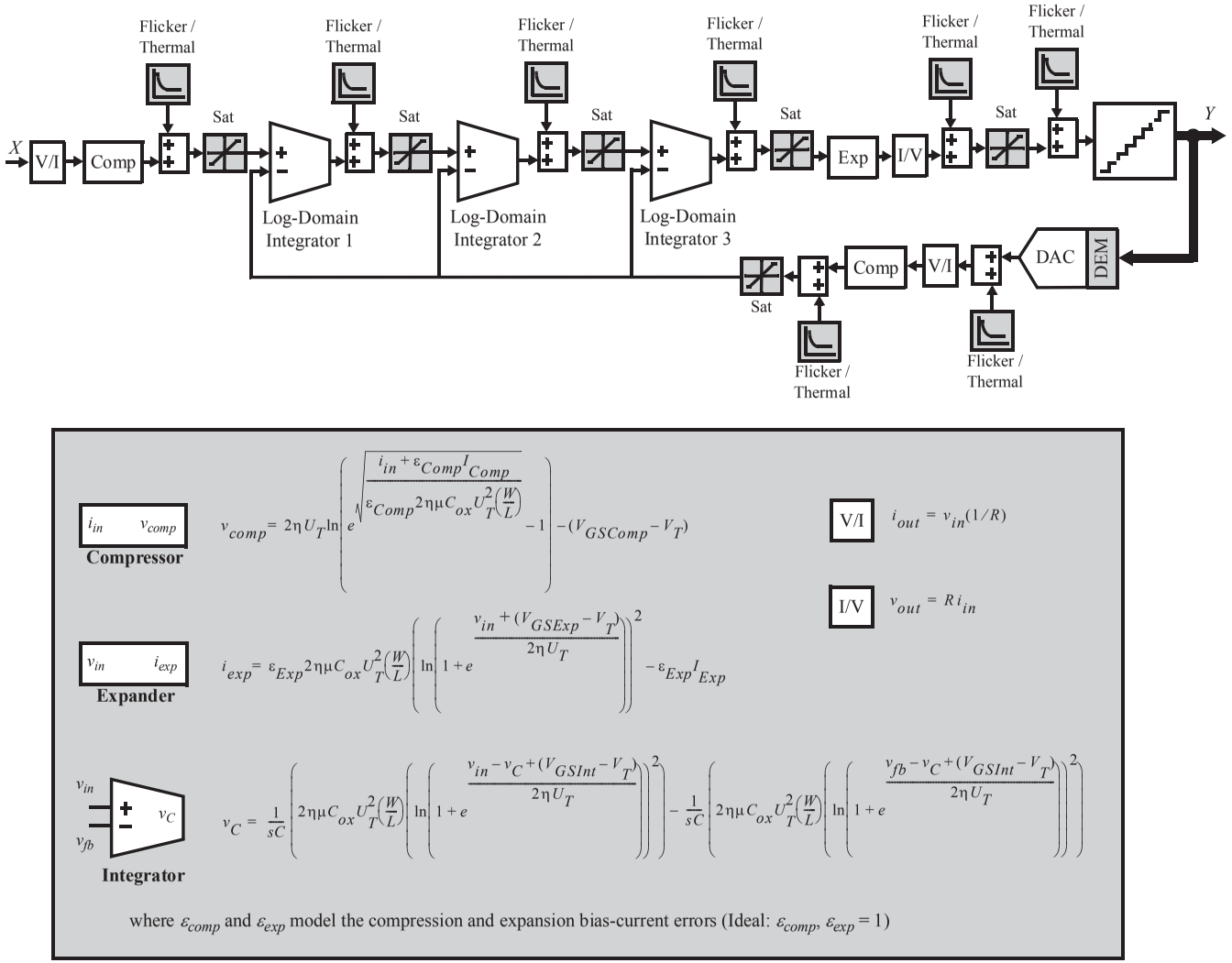


Figure 4.7: Block diagram for the SIMULINK model of the proposed third-order multibit log-domain ΔΣ modulator including the modeling of non-idealities and DEM.

Table 4.2: Variables defined by designer and variables evaluated within SIMULINK model at initialization for the log-domain behavioural models in Fig. 4.7

SIMULINK variables defined by designer	SIMULINK variables evaluated within SIMULINK model at initialization
Technology Parameters	$\frac{W}{L}_{Comp,Exp} = \frac{I_{Comp,Exp}}{2\,\eta\,\mu\,C_{ox}\,U_T^2\,IC}$
η	$\frac{W}{L}_{Int1,2,3} = \frac{I_{Int1,2,3}}{2\,\eta\,\mu\,C_{ox}\,U_T^2\,IC}$
μ	$V_{GS,Comp,Exp} = V_T + 2\,\eta\,U_T\,\ln\left(e^{\sqrt{\frac{I_{Comp,Exp}}{2\,\eta\,\mu\,C_{ox}\,U_T^2\,W/L_{Comp,Exp}}}} - 1\right)$
C_{ox}	$V_{GS,Int1,2,3} = V_T + 2\,\eta\,U_T\,\ln\left(e^{\sqrt{\frac{I_{Int1,2,3}}{2\,\eta\,\mu\,C_{ox}\,U_T^2\,W/L_{Int1,2,3}}}} - 1\right)$
U_T	$C_1 = I_{Int1}\,\frac{C_1}{I_{Int1}}$
V_T	$C_2 = I_{Int2}\,\frac{C_2}{I_{Int2}}$
Design Parameters	$C_3 = I_{Int3}\,\frac{C_3}{I_{Int3}}$
$R_{VI} = R_{IV}$	
$I_{Comp} = I_{Exp}$	
$\frac{I_{Int1}}{C_1}$, $\frac{I_{Int2}}{C_2}$, $\frac{I_{Int3}}{C_3}$	
$I_{Int1}, I_{Int2}, I_{Int3}$	
IC	

4.3.3 Compression/Expansion Mismatch

It was demonstrated in (4.57) - (4.59) that a mismatch between the ratio of the compression and expansion factors (I_{Exp}/I_{Comp2}), and the voltage-to-current and current-to-voltage conversion factors (R_{IV}/R_{VI}) results in errors in the loop-filter coefficients b_1, b_2, and b_3. These errors, in turn, introduce distortion. In weak-inversion, bias-current mismatch is dominated by V_T process variations.

The effects of bias-current mismatch are investigated in this work by introducing errors

in the compression and expansion factors, ε_{Comp} and ε_{Exp}, as shown in Fig. 4.7. Ideally, $\varepsilon = 1$, with $\varepsilon > 1$ representing a positive deviation from the compression or expansion factor, and $\varepsilon < 1$ representing a negative deviation.

4.3.4 Circuit Noise

Here, an approach to modeling noise is presented that is circuit-architecture independent. The developed models introduce a noise source of the designer's choice into selected nodes, allowing the designer to vary the noise while observing its effect at the output node. The noise of the components whose noise effects are being investigated is first evaluated through circuit-level simulations as discussed in Chapter 5, then inserted at the appropriate node in Fig. 4.7.

In SIMULINK, models for the simulation of thermal noise are readily available, in contrast to flicker noise. To generate flicker noise, the technique presented in [Sch08] is employed: a filter is applied to a thermal noise source, the poles and zeros of the former having been positioned in pairs equidistantly on the log scale from 1 Hz to the corner frequency. The gain of the filter is evaluated from the targeted thermal noise at the corner frequency. The MATLAB code developed, based in part on the model presented in [Sch08], is presented in Appendix B.

Figure 4.7 demonstrates the introduction of the filter and thermal noise block at various nodes within the multibit log-domain $\Delta\Sigma$ modulator. For completeness, Fig. 4.7 illustrates the possibility of behaviouraly modeling the circuit noise of all the analog components. In Chapter 5 and Chapter 7, it will be highlighted that for the presented log-domain $\Delta\Sigma$ modulator implementation, the circuit noise introduced by the log-domain analog components will be evaluated through circuit-level simulations, and behavioural modeling will be employed to evaluate the effect of the quantizer and DAC's noise contributions.

4.3.5 DAC Mismatch and Linearization

As discussed in Section 2.2.3, a DWA algorithm is employed for linearization of the multi-bit DAC unit-elements. To simulate the DWA algorithm, a model is introduced in Fig. 4.7 that allows for the introduction of mismatch in the DAC unit-elements, and allows for generation of a DAC output through the application of the DWA algorithm [Bai95] to a series of mismatched unit-elements [3].

4.3.6 Limited Output Voltage Swing

To account for the limited voltage swing at the output of the modulator analog components (integrators, compressors, and expander), saturation (limiter) blocks with saturation levels of $\pm V_{SAT}$ were placed at the output of these components in the SIMULINK model, as shown in Fig. 4.7.

4.4 Behavioural Simulation Results

In the previous section, modeling of relevant non-idealities for log-domain $\Delta\Sigma$ modulators was presented. Here, non-idealities unique to log-domain $\Delta\Sigma$ modulators are investigated through behavioural simulations, demonstrating their effects on performance. Specifically, the NTF of the log-domain $\Delta\Sigma$ modulator is verified, and the effects of inversion-coefficient variation, matching of the compressor and expander, and DAC unit-element errors and DWA correction are demonstrated. The designer-defined variables employed in all behavioural simulations are summarized in Table 4.3.

[3] The author extends his thanks to Philip Chopp for providing the continuous-time DWA SIMULINK model.

Table 4.3: Summary of the behavioural simulation variables for the proposed 3rd-order 3-bit multibit log-domain $\Delta\Sigma$ modulator modeled in Fig. 4.7. Remaining variables evaluated within SIMULINK model according to Table: 4.2

Design Parameter	**Simulation**			
	NTF Verification (Fig. 4.8)	Inversion-Coefficient Variation (Fig. 4.9 & 4.10)	Compressor-Expander Mismatch (Fig. 4.11)	DAC errors and correction (Fig. 4.12(a) & 4.12(b))
OSR	16	16	16	16
f_{in} (kHz)	2.866	2.866	2.866	2.866
f_{BW} (kHz)	10	10	10	10
M	7	7	7	7
V_{REF} (V)	1	1	1	1
V_{SAT} (V)	1	1	1	1
$R_{VI} = R_{IV}$ (kΩ)	800	800	800	800
$I_{Comp} = I_{Exp}$ (nA)	450	450	450	450
$\frac{I_{Int1}}{C_1}$	5600	5600	5600	5600
$\frac{I_{Int2}}{C_2}$	12218.18	12218.18	12218.18	12218.18
$\frac{I_{Int3}}{C_3}$	20533.33	20533.33	20533.33	20533.33
I_{Int1} (nA)	728	728	728	728
I_{Int2} (nA)	464	464	464	464
I_{Int3} (nA)	257	257	257	257
IC	0.001	0.001, 0.025, 0.05, 0.1, 10	0.025	0.025
$\varepsilon_{Exp}, \varepsilon_{Comp2}$	1	1	1, 0.95, 1.05	1
ε_{Comp2}	1	1	1, 0.95, 1.05	1
DAC Errors	No Errors	No Errors	No Errors	2% std. dev., 2% std. dev. + DWA

4.4.1 Noise Transfer Function Verification

A classical $\Delta\Sigma$ modulator (Fig. 4.5) and a log-domain $\Delta\Sigma$ modulator based on the proposed multibit log-domain architecture (Fig. 4.6) were simulated with SIMULINK for the following design specifications:

- Third-order loop filter and OSR = 16.
- Input frequency $f_{in} = 2.866$ kHz, modulator bandwidth $f_{BW} = 10$ kHz, and sampling frequency $f_s = 320$ kHz.
- 7-level (3-bit) quantizer.
- The quantizer reference voltage is normalized to V_{REF} = 1 V.
- The saturation (limiter) blocks are normalized to V_{SAT} = 1 V.
- The log-domain transistors are biased deep in weak-inversion, such that IC = 0.001 and η = 1.4.
- The integrator coefficients in (4.68) are adjusted for the SIMULINK model according to Table 4.1 such that: I_{Int1}/C_1 = 5600, I_{Int2}/C_2 = 12218.18, I_{Int3}/C_3 = 20533.33.
- The voltage-to-current conversion resistor and current-to-voltage conversation resistor are $R_{VI} = R_{IV}$ = 800 kΩ [4].
- The compressor and expander bias currents are $I_{Comp} = I_{Exp}$ = 450 nA [5].
- The integrator bias currents are setup such that I_{Int1} = 728 nA, I_{Int2} = 464 nA, I_{Int3} = 257 nA [6].

[4] The values of R_{VI} and R_{IV} are a result of applying the optimization process described in Chapter 5.
[5] The values of I_{Comp} and I_{Exp} are a result of applying the optimization process described in Chapter 5.
[6] The values of I_{Int1}, I_{Int2}, and I_{Int3} are a result of applying the optimization process described in Chapter 5.

Figure 4.8 shows the simulated Signal-to-Quantization-Noise-Ratio (SQNR) versus input voltage for both modulator designs. Note that the curves approximately match. Accordingly, the proposed multibit log-domain $\Delta\Sigma$ modulator can achieve NTFs equivalent to those of its classical counterpart.

Let X_{MAX} denote the modulator's maximum input-signal amplitude which will not overload the quantizer. As per Fig. 4.8, the maximum SQNR of the ideal log-domain and classical $\Delta\Sigma$ modulators is 73.5 dB, at an X_{MAX} of 0.7 V.

4.4.2 Variation of the Inversion Coefficient

It was demonstrated in [Pal03] that operation of the log-domain components in moderate inversion introduces tones in the output spectrum of the log-domain $\Delta\Sigma$ modulator. Here, we investigate the degree of performance loss as the level of channel inversion is varied.

Figure 4.9 shows the simulated Signal-to-Noise-and-Distortion-Ratio (SNDR) versus input range of a log-domain $\Delta\Sigma$ modulator simulated for the design specifications in the previous subsection, while varying the inversion coefficient IC as follows: IC = 0.001 (η = 1.4), 0.025 (η = 1.4), 0.05 (η = 1.4), 0.1 (η = 1.4), 1 (η = 1.35), 10 (η = 1.3) [7].

As per Fig. 4.9, an *IC* variation of 0.025 to 0.1 results in approximately a 1.7 dB SNDR loss. Accordingly, a log-domain $\Delta\Sigma$ modulator does not suffer from a significant loss in performance if the *IC* remains in the weak-inversion region. However, performance quickly deteriorates in moderate-inversion, with a 7.9 dB SNDR loss as the *IC* is varied from 0.1 to 1. Figure 4.10 demonstrates the output spectrum for the biasing of weak-inversion devices at *IC* = 0.025.

[7] In weak-inversion, the substrate factor η = 1.4. In moderate-inversion η = 1.35. In strong-inversion η = 1.3 [Bin08].

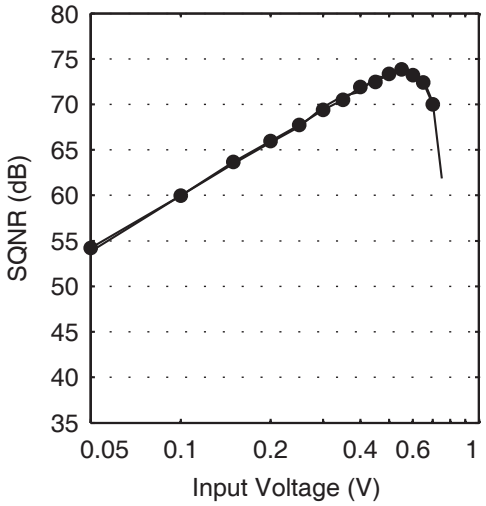


Figure 4.8: SQNR versus input voltage for a 3rd-order classical and log-domain $\Delta\Sigma$ modulator with 3-bit-quantizer. **Here: — = classical; and -•- = log-domain modulator realization with *IC* $\ll$ 0.01.**

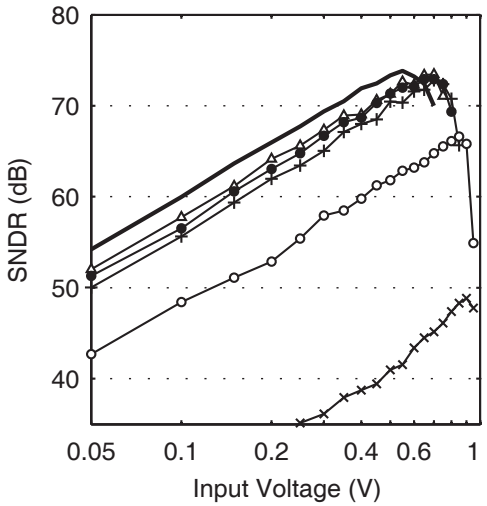


Figure 4.9: SNDR versus input voltage variation of the multibit log-domain $\Delta\Sigma$ modulator for a variation of the compressor, expander, and integrator *IC*. **Here: — = *IC* $\ll$ 0.01; $\triangle$ = *IC* = 0.025; • = *IC* = 0.05; + = *IC* = 0.1; ○ = *IC* = 1; and $\times$ = *IC* = 10.**

4.4.3 Matching of Log-Domain Transistors

Figure 4.11 shows the SNDR versus input range as the expansion factor is varied relative to the ideal value, and as the compression factor of compressor 2 is varied relative to the ideal value. Figure 4.11 indicates little variation in the maximum SNDR and X_{MAX} as the expansion mismatch factor varies from -5% (ε_{Exp} = 0.95) to 5% (ε_{Exp} = 1.05). As the compression/mismatch factor of compressor 2 reaches -5% (ε_{Comp2} = 0.95), the maximum SNDR drops to 67.4 dB, at an X_{MAX} of 0.65 V.

In practice, the mismatch for a transistor pair in 0.13 μm technology can be evaluated. For a transistor pair biased in weak-inversion with submicron current (I_{BIAS} is assumed to be 0.5 μA) and $L = 4 \times L_{min}$, bias-current mismatch (1σ) is calculated to be 5.3%. The transistor V_T mismatch (1σ) is calculated to be 1.8 mV [8].

[8] For further details, the reader is referred to the bias-current and V_T mismatch equations in [Bin08] (p. 236, 248), and the technology parameters in [Pel98]. The transistor inversion coefficient (IC) is assumed to be 0.02.

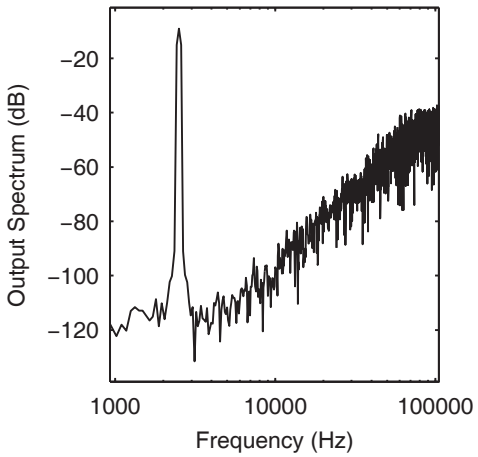


Figure 4.10: Output spectrum of the 3rd-order log-domain ΔΣ modulator with 3-bit-quantizer, at an input voltage of 0.7 V, weak-inversion devices biased at $IC = 0.025$, and $V_{REF} = V_{SAT} = 1$ V.

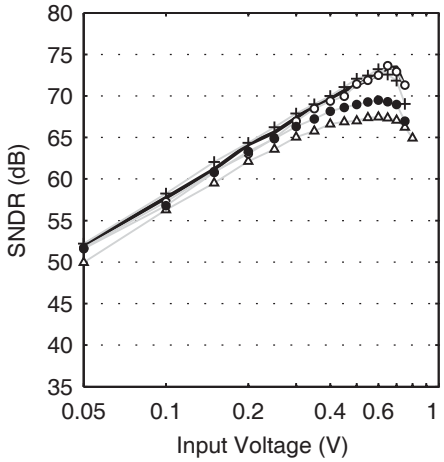
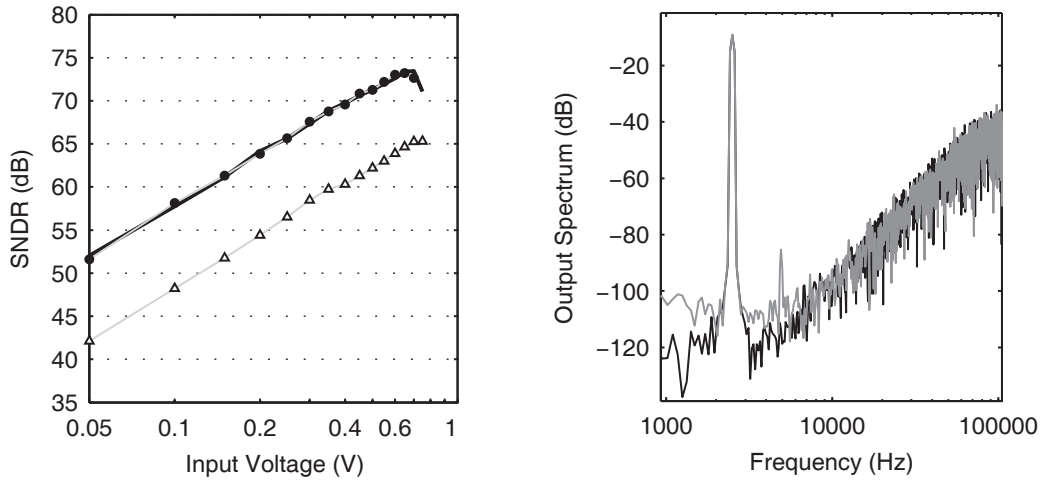


Figure 4.11: SNDR versus input voltage for the 3rd-order log-domain ΔΣ modulator with 3-bit-quantizer, weak-inversion devices biased at $IC = 0.025$, and $V_{REF} = V_{SAT} = 1$ V. **Here: — = no mismatch; △ = -5% compression factor mismatch; • = 5% compression factor mismatch; + = -5% expansion factor mismatch; and ○ = 5% expansion factor mismatch.**

4.4.4 DAC Unit-Element Mismatch Correction

As noted in Chapter 2, unit-element mismatch errors in multibit DACs can result in significant distortion, and therefore require the use of linearization techniques in the feedback path [Car97]. The implementation of the proposed multibit log-domain DAC using uniform-sized elements rather than logarithmically-sized elements allows for utilization of Dynamic-Element-Matching (DEM) in the feedback path. Figures 4.12(a) and 4.12(b) demonstrate the degradation of performance due to DAC unit-element mismatch errors, and the linearization performed by a Data-Weighted-Averaging (DWA) algorithm [Bai95] (Fig. 2.6) to restore performance.



(a) (b)

Figure 4.12: Effects of DAC unit-element mismatch of 2%, and the effects of DWA linearization on the implemented modulator. a) SNDR versus input voltage variation, where △ = DAC unit-element errors; and • = DWA linearization. b) Output spectrum, where the grey spectrum reflects the impact of DAC unit-element mismatch, and the dark spectrum reflects the impact of DWA linearization.

4.5 Summary

This chapter investigated the design challenges, and the architecture-level design, of log-domain $\Delta\Sigma$ modulators. A multibit log-domain $\Delta\Sigma$ modulator architecture and class AB loop-filter realization were proposed. Furthermore, behavioural models of the log-domain analog components and various circuit non-idealities were developed. A 3rd-order class AB log-domain loop-filter realization was presented, and the performance and the effects of various non-idealities were demonstrated through behavioural simulations.

In Chapter 5, the circuit-level implementation of the preceding class AB log-domain loop filter will be presented.

CHAPTER 5

Multibit Log-Domain $\Delta\Sigma$ Modulator: Loop-Filter Circuit Implementation

IN THIS chapter, the circuit-level realization of the class AB multibit log-domain $\Delta\Sigma$ loop-filter proposed in Chapter 4 is presented. The implementation of the log-domain analog components is considered in the context of the log-domain equations presented earlier, and with special attention to minimizing distortion introduced by second-order effects.

Furthermore, the various trends involved in the design of log-domain circuits are explored, and an optimization procedure is proposed to arrive at the targeted performance. Circuit-level simulation results verifying the various design trends, and demonstrating the performance of the proposed log-domain loop-filter, are presented.

5.1 Low-Distortion Loop-Filter Circuit Implementation

5.1.1 Low-Distortion Class AB Integrator

The differential-input differential-output integrator in Fig. 5.1 [Red05] is considered for the implementation of the proposed class AB $\Delta\Sigma$ modulator. The integrator realizes the class AB integrator operating equations presented in Section 4.4, and repeated here

$$\begin{aligned} i_{Cp} &= C\frac{dv_{Cp}}{dt} \\ &= I_{Int}\,(e^{\frac{v_{inA}-v_{Cp}}{\eta\,U_T}} - e^{\frac{v_{fbA}-v_{Cp}}{\eta\,U_T}}) \\ &\quad -I_{Int}\,(e^{\frac{v_{inB}-v_{Cp}}{\eta\,U_T}} - e^{\frac{v_{fbB}-v_{Cp}}{\eta\,U_T}}) \end{aligned} \tag{5.1}$$

$$\begin{aligned} i_{Cn} &= C\frac{dv_{Cn}}{dt} \\ &= I_{Int}\,(e^{\frac{v_{inB}-v_{Cn}}{\eta\,U_T}} - e^{\frac{v_{fbB}-v_{Cn}}{\eta\,U_T}}) \\ &\quad -I_{Int}\,(e^{\frac{v_{inA}-v_{Cn}}{\eta\,U_T}} - e^{\frac{v_{fbA}-v_{Cn}}{\eta\,U_T}}) \end{aligned} \tag{5.2}$$

Observing (5.1) and Fig. 5.1, transistors M_1 - M_2 realize the current difference at the output v_{Cp} resulting from the differential input signals v_{inA} and v_{inB}, while transistors M_7 - M_8 implement the current difference resulting from the differential feedback signals v_{fbA} and v_{fbB}. Transistors M_5, M_6 and the bias current I_{Int} act as an ac-signal level shifter [Pyt01], transferring the signal voltage v_{Cp} at the output node to the source of M_1, M_2, M_7, and M_8. Transistors M_7 - M_{16} perform the inverse of the aforementioned transistors generating the output v_{Cn}, described by (5.2).

Class AB architectures necessitate the use of common-mode-feedback (CMFB) circuits to sense fluctuations in the bias of the differential outputs and to adjust the bias accordingly,

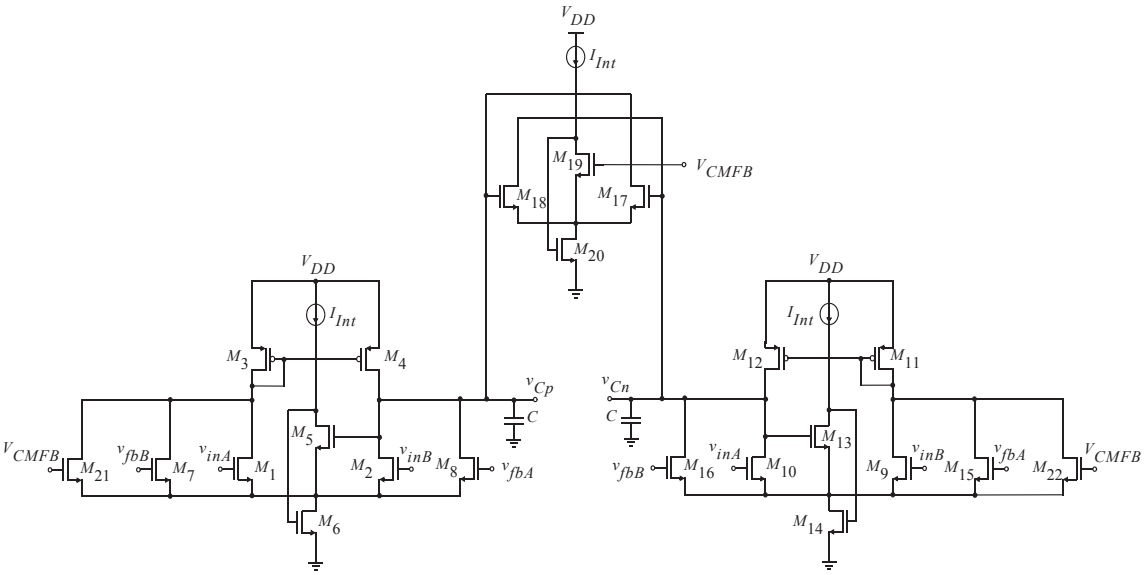


Figure 5.1: Differential-input differential-output log-domain integrator implementing (5.1) and (5.2) [Red05].

maintaing equal bias across the output nodes. The log-domain CMFB circuit is realized by transistors M_{17} - M_{22} in Fig. 5.1.

In class AB integrators, the differential nature of each signal path results in the attenuation of even-order harmonics at each of the integrator outputs v_{Cp} and v_{Cn}, and reduced susceptibility to voltage-supply noise. Furthermore, this reduction in distortion and noise within the $\Delta\Sigma$ modulator nodes reduces overload within the modulator, improving stability.

Integrator Distortion Minimization

In Chapter 3, it was outlined that a significant challenge in the design of log-domain $\Delta\Sigma$ modulators targeting high-resolution applications is the distortion resulting from circuit non-idealities. Observing Fig. 5.1, for transistors M_1-M_2, M_7-M_8, M_9-M_{10}, and M_{15}-M_{16}, a mismatch in the respective drain-to-source voltage V_{DS} of the transistors results in mismatch between, and deviation from, the bias current I_{Int}. This introduces significant variation in the log-domain operating equation described by (5.1) and (5.2), and, in turn,

the loop-filter transfer-function described by (4.56) - (4.59).

To minimize distortion, the following relationship should be maintained

$$V_{D,1} = V_{D,2} = V_{D,7} = V_{D,8} = V_{D,9} = V_{D,10} = V_{D,15} = V_{D,16} \tag{5.3}$$

where $V_{D,n}$ is the voltage bias at the drain of transistor M_n.

Observing Fig. 5.1, the voltage bias at the drains of M_2, M_8, M_{10}, and M_{16}, which constitute the two integrator output nodes, is dictated by the CMFB circuit, such that

$$V_{D,2} = V_{D,8} = V_{D,10} = V_{D,16} = V_{CMFB} \tag{5.4}$$

which is commonly set to equal the bias at the integrator input and feedback nodes, v_{in} and v_{fb}, to ease the cascading of integrators.

In contrast, the voltage at the drains of transistors M_1, M_7, M_9, and M_{15} is dictated by the supply voltage V_{DD} and the gate-to-source voltage of transistors M_3 and M_{11}, such that

$$V_{D,1} = V_{D,7} = V_{D9} = V_{D,15} \quad = \quad V_{DD} - V_{GS,3} \quad = \quad V_{DD} - V_{GS,11} \tag{5.5}$$

where $V_{GS,n}$ is the gate-to-source voltage of transistor M_n.

Figure 5.2 proposes the introduction of several cascodes to ensure equal drain-to-source voltage (V_{DS}) biasing for each differential-transistor pair, and equal V_{DS} biasing across each mirroring-transistor pair. Specifically, transistors M_{23} and M_{26} are introduced to set the voltage bias at the drain of the input transistors independently of the supply voltage. The voltage V_{BIASa} is selected such that

$$V_{BIASa} \quad = \quad V_{CMFB} + V_{GS,23} \quad = \quad V_{CMFB} + V_{GS,26} \tag{5.6}$$

To improve the accuracy of current mirrors M_3-M_4 and M_{11}-M_{12} the simple current mirrors in Fig. 5.1 are replaced by wide-swing cascode current mirrors, as shown in Fig.

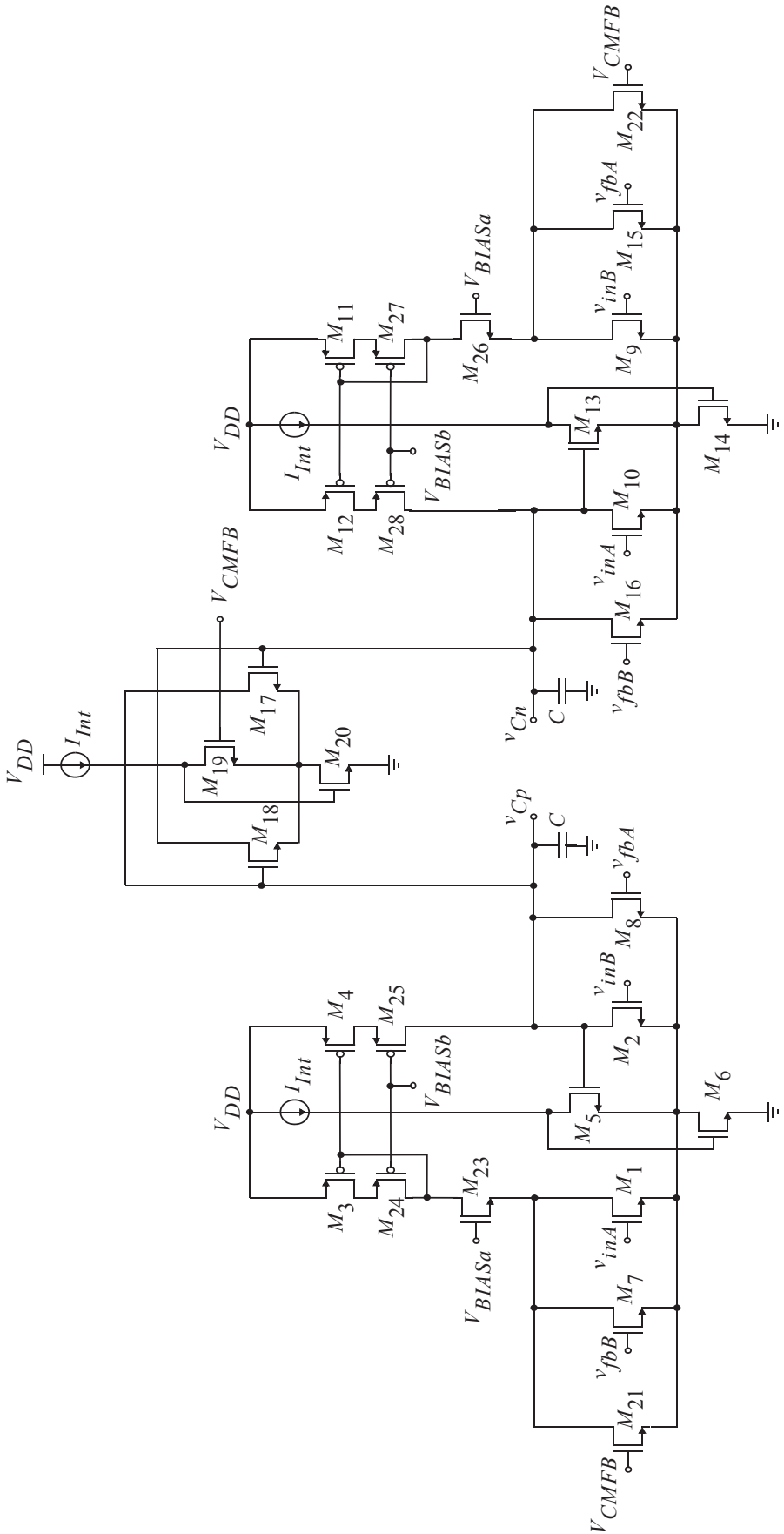


Figure 5.2: Proposed low-distortion differential-input differential-output integrator, with CMFB.

5.2.

Minimum Voltage Supply

In addition to increased circuit complexity, one drawback of the proposed approach is the resulting voltage-headroom penalty. Observing Fig. 5.2, the minimum voltage headroom required between the voltage-supply and ground, $V_{DD,min}$, is determined to be

$$V_{DD,min} = V_{GS,3} + V_{DS,sat,23} + V_{DS,sat,1} + v_{Cp,PP} + V_{DS,sat,6} \quad \text{(Fig. 5.2)} \tag{5.7}$$

where $v_{Cp,PP}$ is the peak-to-peak swing of the output signal v_{Cp}, which appears at the source of M_1 through the dc-level shifting performed by transistor M_5. The compressed nature of the internal log-domain signals results in a low $v_{Cp,PP}$. The voltage $V_{DS,sat,n}$ is the drain-to-source voltage V_{DS} at which transistor M_n enters saturation.

Since for low-distortion performance, the V_{DS} of transistors M_1 (and M_7) and M_2 (and M_8) are matched ($V_{D,1} = V_{D,7} = V_{D,2} = V_{D,8}$), a voltage of $V_{GS,5}$ is expected across the drain and source terminals of M_1 and M_7. Accordingly, for low-distortion $V_{DS,1} > V_{DS,sat,1}$ and (5.7) is re-interpreted to reflect the requirements for low-distortion performance

$$\begin{aligned} V_{DD,min} &= V_{GS,3} + V_{DS,sat,23} + V_{DS,1} + v_{Cp,PP} + V_{DS,sat,6} \quad \text{(Fig. 5.2, low distortion)} \\ &= V_{GS,3} + V_{DS,sat,23} + V_{GS,5} + v_{Cp,PP} + V_{DS,sat,6} \end{aligned} \tag{5.8}$$

In the proposed low-distortion log-domain ΔΣ modulator in Fig. 5.2, the log-domain input and feedback transistors (M_1, M_2, M_7, M_8, M_9, M_{10}, M_{15}, and M_{16}), the level-shift transistors (M_5, M_6, M_{13}, and M_{14}), and the CMFB transistors (M_{17}-M_{22}) are biased in weak-inversion. The current mirror transistors (M_3, M_4, M_{11}, and M_{12}) are biased in moderate-inversion.

Table 5.1: Comparison of current consumption and minimum supply-voltage for the integrator in [Red05] and the proposed low-distortion realization.

Integrator Realization	Current Consumption	Minimum Voltage Supply
Class AB [Red05]	$I_{Total} \cong 15\, I_{Int}$	$V_{DD,min} = V_{GS,3} + V_{DS,sat,1} + v_{Cp,PP} + V_{DS,sat,6}$
Proposed low-distortion class AB [Sha14b]	$I_{Total} \cong 15\, I_{Int}$	$V_{DD,min} = V_{GS,3} + V_{DS,sat,23} + V_{GS,5} + v_{Cp,PP} + V_{DS,sat,6}$

Table 5.1 summarizes the differences between the integrator in [Red05] and the low-distortion integrator presented in this section, where I_{Total} represents the total current drawn from the supply voltage [1]. Observing Table 5.1, the low-distortion circuit suffers from no additional power penalty. However, $V_{DD,min}$ increases by an additional V_{GS} compared to the circuit in [Red05].

5.1.2 Low-Distortion Compressor

The ability of class AB log-domain circuits to process signals larger than the bias current, and the advantages of doing so, were highlighted in Section 3.2.

To ensure that the total current flowing through the compressing transistors remains positive in class AB log-domain operation, two positive 180^o out-of-phase signals need to be generated. Employing rectifiers would result in highly distorted signals with sharp transitions. Accordingly, a common approach to generate the two positive 180^o out-of-phase signals is through the geometric-mean function, described by the following relationships [Fre94]

$$I_{Comp}^2 = i_p\, i_n \tag{5.9}$$

$$i_{in} = i_p - i_n \tag{5.10}$$

[1] Not all paths draw the exact current I_{Int}, due to differing V_{DS} biasing across the devices.

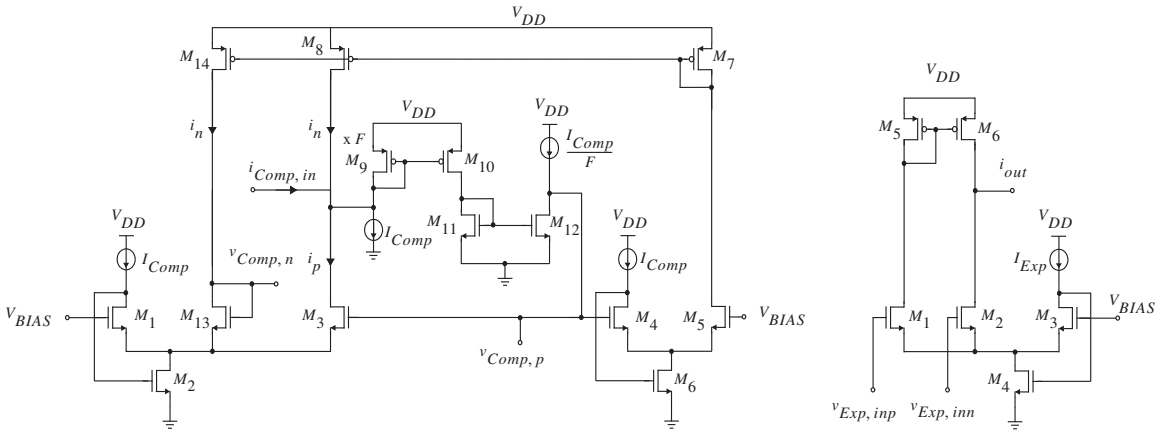


Figure 5.3: Class AB compressor and expander proposed in [Red05]: a) Differential output compressor; and b) Single-ended output expander.

where I_{Comp} is the compressor bias current, i_{in} is the differential current sum, and i_p and i_n are the resulting split currents.

A CMOS implementation of a class AB log-domain geometric-mean differential-signal generator and log-domain compressor was proposed in [Red05] (Fig. 5.3(a)), based on the compressor presented in [Ser00]). Transistors M_1, M_3-M_5 and transistors M_1, M_{13}, M_4, M_5 split the input signals into their respective i_p and i_n signals [2]. The split currents are then compressed according to (3.5), which is restated here for the case of the compressor in Fig. 5.3(a).

$$v_{Comp-p,n} \quad = \quad \eta\, U_T\, \ln(1 + i_{p,n}/I_{Comp}) \tag{5.11}$$

Transistors M_9-M_{12} maintain low input-impedance, and bias the input node [Red07].

Although the circuit in Fig. 5.3(a) realizes the geometric-mean relationship described by (5.9) and (5.10), and the compression described by (5.11), it suffers from significant differential distortion resulting from unequal V_{DS} across the differential compressing tran-

[2] The current splitting operation described by (5.9) and (5.10) can be deduced from Fig. 5.4 by observing the summation of currents i_p and i_n at the differential inputs, setting i_{in} in (5.10) to $I_{Comp,in(p,n)}$, and considering the translinear principle [Gil75] to relate the product of currents in (5.10).

sistors M_3 and M_{13}. The resulting deviation from I_{Comp}, and mismatch between transistors M_3 and M_{13}, causes varying degrees of compression between the two differential signals i_p and i_n. In turn, the differential distortion hinders the targeted high-resolution performance. Specifically, in Fig. 5.3(a), $V_{D,3}$ is dictated by M_9

$$V_{D,3} = V_{DD} - V_{GS,\,9} \qquad \text{(Fig. 5.3(a))} \tag{5.12}$$

while the voltage at the drain of M_{13} is observed to be

$$\begin{aligned} V_{D,13} &= V_{BIAS} - V_{GS,\,1} + V_{GS,\,13} \qquad \text{(Fig. 5.3(a))} \\ &\approx V_{BIAS} \quad (\text{since } M_1 \text{ and } M_{13} \text{ ideally biased at } I_{Comp}) \end{aligned} \tag{5.13}$$

To overcome this drawback, the low-distortion class AB geometric-mean generator and log-domain compressor in Fig. 5.4 is employed. Here, elements of the design in [Red05] are replicated to generate the second differential compressed voltage. Symmetric paths ensure that compressing transistors M_3 and M_{15} are biased at equal V_{DS}, such that

$$V_{D,3} = V_{D,15} \;=\; V_{DD} - V_{GS,11} \;=\; V_{DD} - V_{GS,23} \qquad \text{(Fig. 5.4)} \tag{5.14}$$

Furthermore, to improve accuracy, wide-swing cascode current mirrors are introduced to perform the current mirroring.

Transistors M_1, M_3-M_5 and transistors M_1, M_{15}-M_{17} split the input signals into their respective i_p and i_n signals, such that

$$I_{Comp}^2 = i_p\, i_n \tag{5.15}$$

$$i_{Comp,inp} = i_p - i_n \tag{5.16}$$

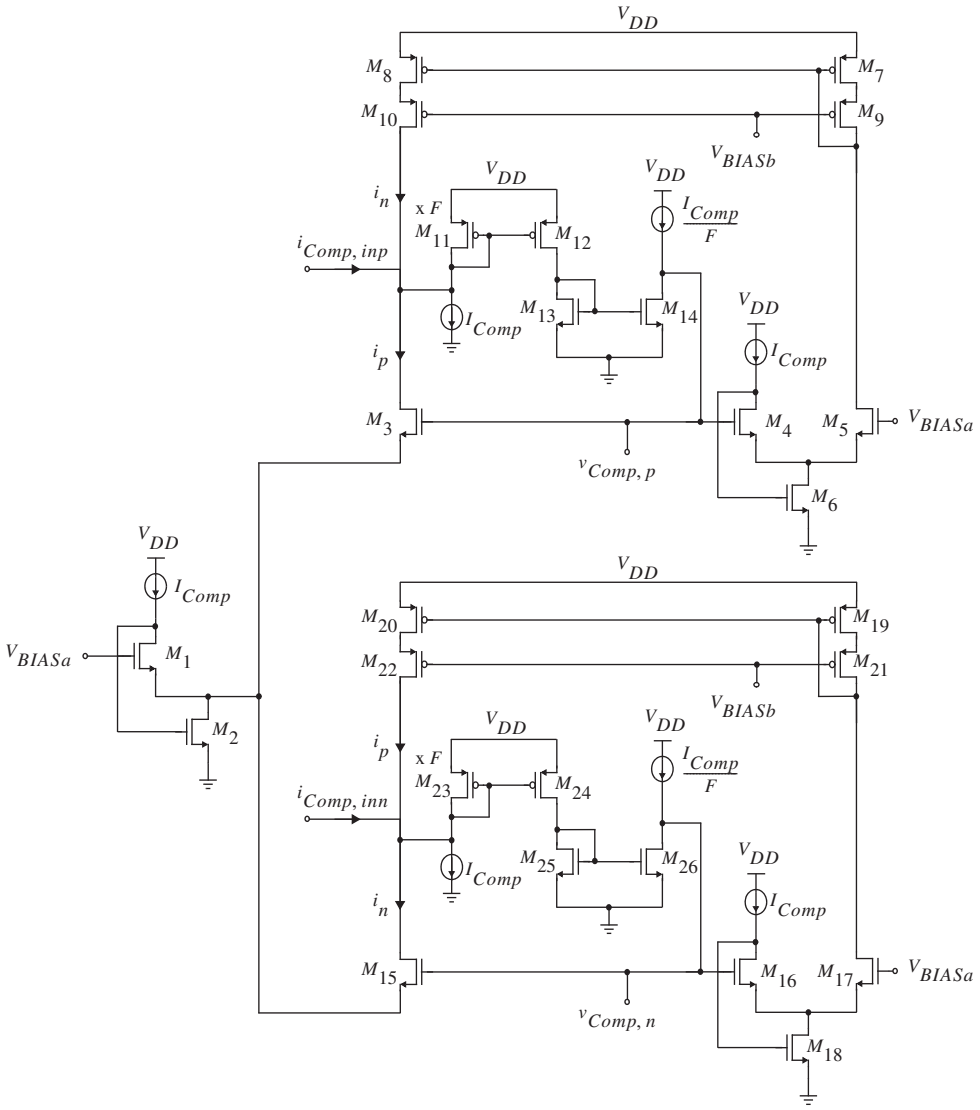


Figure 5.4: Low-Distortion class AB geometric-mean generator and log-domain compressor.

$$i_{Comp,inn} = i_n - i_p \tag{5.17}$$

The compressed outputs are generated at the gate of the compressing transistors M_3 and M_{15} according to (5.11).

The low-distortion compression in Fig. 5.4 comes at the expense of increased power consumption. Observing Fig. 5.3(a) and Fig. 5.4, the current I_{Total} for both realizations is

approximately [3]

$$I_{Total} \cong 6\,I_{Comp} + 2\,\frac{I_{Comp}}{F} \qquad (\text{Fig. } 5.3(\text{a})) \tag{5.18}$$

$$I_{Total} \cong 9\,I_{Comp} + 4\,\frac{I_{Comp}}{F} \qquad (\text{Fig. } 5.4) \tag{5.19}$$

Assuming that the factor F in Fig. 5.4 and Fig. 5.3(a) is set such that $F > 4$, the proposed low-distortion realization in Fig. 5.4 consumes a little over 50% additional power when compared to the circuit in Fig. 5.3(a).

It is noted that the differential paths share the level-shifter comprised of M_1 and M_2, avoiding the need for an additional level-shifter, and conserving power. This sharing is possible since the voltage generated at the drain of transistor M_1 is a signal-independent voltage bias, which can be harnessed in both current splitters.

Table 5.2 summarizes the differences between the compressor in [Red05] and the low-distortion compressor in Fig. 5.4. Here, $v_{Comp,p,PP}$ and $v_{Comp,n,PP}$ are the peak-to-peak swing of the output signals $v_{Comp,p}$ and $v_{Comp,n}$, which appear at the source of transistors M_3 and M_4 (through the dc-level shifting performed by transistor M_4) in both Fig. 5.3(a) and Fig. 5.4. The compressed nature of the internal log-domain signals results in a low $v_{Comp,p,PP}$ and $v_{Comp,n,PP}$.

5.1.3 Low-Distortion Expander

The differential input signals $i_{Comp,inp}$ and $i_{Comp,inn}$ applied at the input of the geometric-mean generator and compressor in Fig. 5.4 are sinusoidal. Accordingly, the expander is expected to expand the internally-compressed signals and regenerate two sinusoidal differential outputs.

In [Red05] (Fig. 5.3(b)), an expander that utilizes two differential inputs to generate a

[3] Not all paths draw the exact current I_{Comp}, due to differing V_{DS} biasing across the devices.

Table 5.2: Comparison of current consumption and minimum supply-voltage for the compressor in [Red05] and the proposed low-distortion realization.

Integrator Realization	Current Consumption	Minimum Voltage Supply
Class AB [Red05]	$I_{Total} \cong 6\, I_{Comp} + 2\, \frac{I_{Comp}}{F}$	$V_{DD,min} = V_{DS,sat,14} + V_{GS,13} + v_{Comp,n,PP} + V_{DS,sat,2}$
Proposed low-distortion class AB [Sha14b]	$I_{Total} \cong 9\, I_{Comp} + 4\, \frac{I_{Comp}}{F}$	$V_{DD,min} = V_{GS,7} + V_{DS,sat,5} + v_{Comp,p,PP} + V_{DS,sat,6}$

single-ended current output is proposed. However, a second differential output is required for the proposed class AB ΔΣ modulator. Furthermore, the design in Fig. 5.3(b) suffers from unequal V_{DS} across the expanding transistors M_1 and M_2, resulting in varying levels of expansion, and introducing distortion.

To generate two class AB differential outputs while minimizing distortion, the novel low-distortion class AB expander in Fig. 5.5 is proposed. Transistors M_1 and M_2 perform expansion of the two compressed voltage signals, and the expanding transistors are subjected to the same V_{DS} biasing conditions, imposed by M_5 and M_{11}

$$V_{D,1} = V_{D,2} \;=\; V_{DD} - V_{GS,5} \;=\; V_{DD} - V_{GS,11} \qquad \text{(Fig. 5.5)} \tag{5.20}$$

The current at the drains of M_1 and M_2 are governed by (3.7), reproduced here

$$i_d \;=\; I_{Exp}\,(e^{v_{Exp,in-p,n}/\eta U_T} - 1) \tag{5.21}$$

Through two opposing current-mode mirroring paths with respect to the output, two differential outputs are generated. Similar to the low-distortion integrators and compressors presented earlier, wide-swing current mirrors are employed to improve mirroring accuracy.

It is worth noting that differential class AB expansion could have been realized through replicating the design in [Red05] (Fig. 5.3(b)), although the resulting circuit would continue

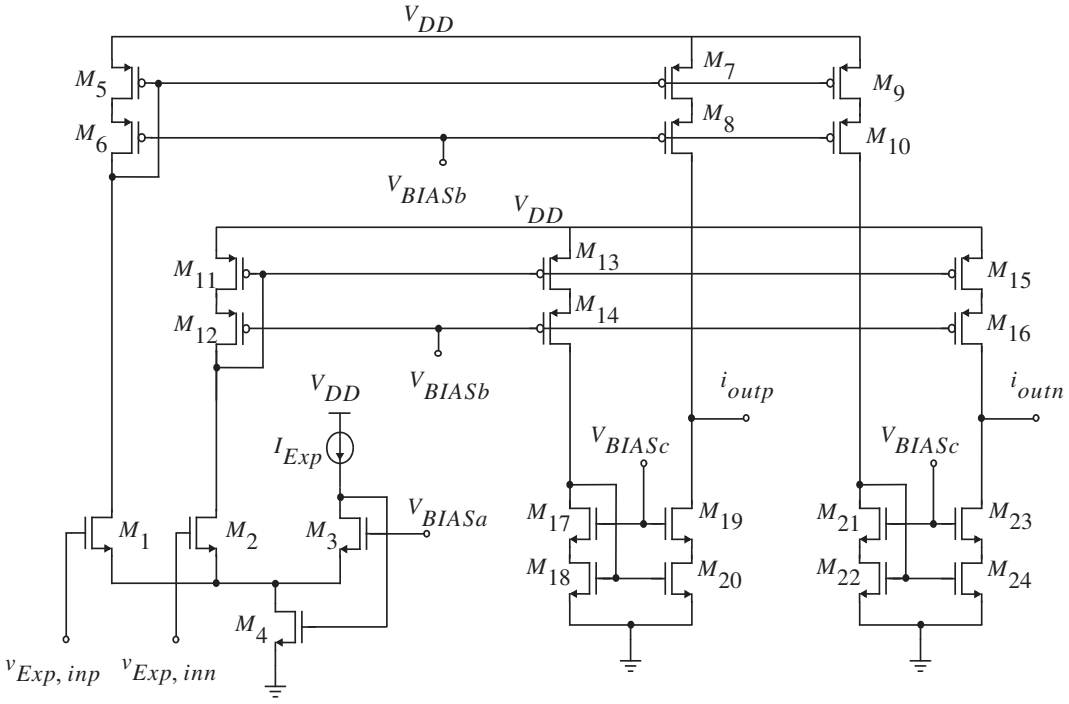


Figure 5.5: Proposed low-distortion class AB expander and sinusoidal regenerator.

to suffer from the aforementioned distortion. Observing Fig. 5.3(b) and Fig. 5.5, the total current I_{Total} drawn from the supply for such a realization, and the proposed realization (Fig. 5.5), is approximately [4]

$$I_{Total} \cong 6\, I_{Exp} \qquad (\text{Two paths of Fig. } 5.3(\text{b})) \tag{5.22}$$

$$I_{Total} \cong 7\, I_{Exp} \qquad (\text{Fig. } 5.5) \tag{5.23}$$

Significant power is saved in the proposed expander by sharing the current paths comprised of M_1-M_6, M_{11}-M_{12} in the generation of both differential outputs. The result is a low-distortion differential-output expander with only an additional bias-current path, when compared to a differential-output expander generated through the replication of the design

[4] Not all paths draw the exact current I_{Exp}, due to differing V_{DS} biasing across the devices.

Table 5.3: Comparison of current consumption and minimum supply-voltage for the expander in [Red05] and the proposed low-distortion realization.

Integrator Realization	Current Consumption	Minimum Voltage Supply
Class AB [Red05] ($2 \times$ [Red05])	$I_{Total} \cong 6\, I_{Exp}$	$V_{DD,min} = V_{GS,5} + V_{DS,sat,1} + V_{DS,sat,4}$
Proposed low-distortion class AB [Sha14b]	$I_{Total} \cong 7\, I_{Exp}$	$V_{DD,min} = V_{DS,sat,15} + V_{DS,sat,16} + V_{DS,sat,23} + V_{DS,sat,24}$

in [Red05], the latter suffering from expansion mismatch.

A comparison of both expander realizations is summarized in Table 5.3.

5.1.4 Voltage-to-Current and Current-to-Voltage Conversion

Voltage-to-current (V/I) conversion of the voltage signals at the log-domain $\Delta\Sigma$ modulator inputs ($x_p(t)$ and $x_n(t)$ in Fig. 4.6) to the currents $i_{in,p}$ and $i_{in,n}$ applied to the input of the geometric-function generator, is performed by employing the voltage-to-current convertor in Fig. 5.6(a) [Pyt01] at each input. Here, the transimpedance amplifier sets a virtual ground at the inverting input, and a resistance of magnitude R_{VI} performs the conversion. The current-to-voltage (I/V) conversion of the expanded signals, performed prior to quantization, is performed by a resistor of magnitude R_{IV} across a transimpedance amplifier, as shown in Fig. 5.6(b). The voltage V_{CM} is adjusted to equal $V_{DD}/2$ to maximize the signal swing range at the modulator's input (in the case of the V/I converter) and expander's (in the case of the I/V converter) output.

A two-stage Miller-compensated op-amp (Fig. 5.7) [Joh97] is employed to realize the amplifier in Fig. 5.6(a) and Fig. 5.6(b). The common-gate transistor in Fig. 5.6(a) feeds the converted current signal to its corresponding input in Fig. 5.4.

Gain and low-voltage considerations resulted in the selection of the two-stage Miller-compensated op-amp

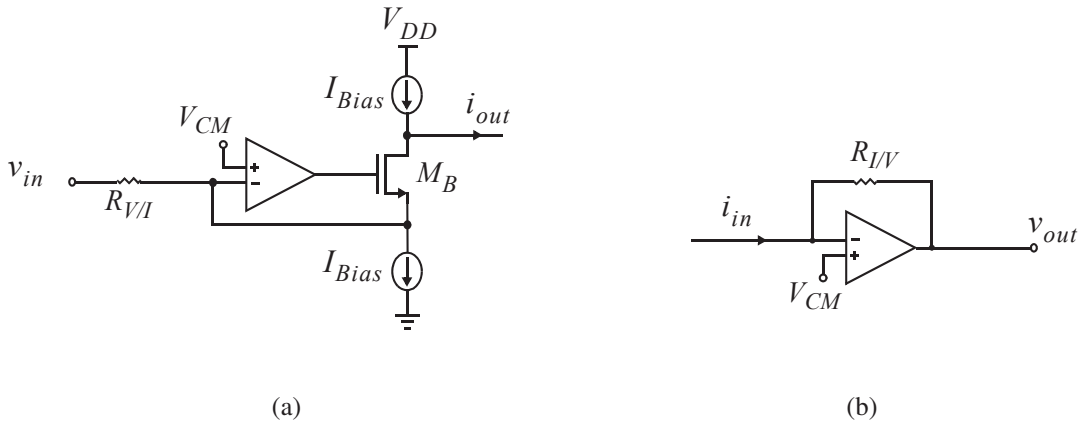


Figure 5.6: a) Voltage-to-current conversion [Pyt01] of $\Delta\Sigma$ modulator input signals. b) Current-to-voltage conversion preceding the quantizer.

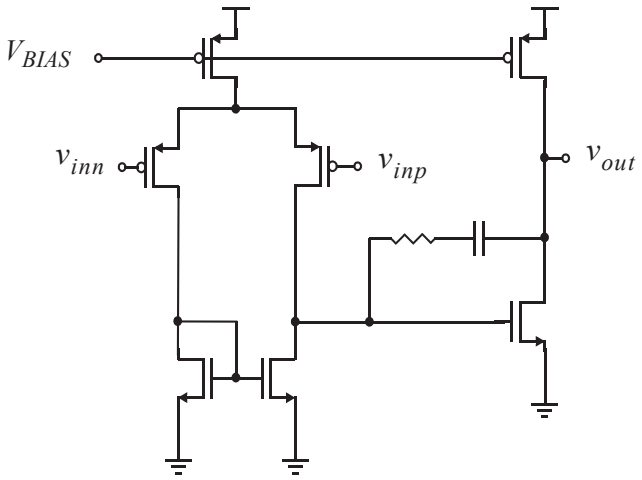


Figure 5.7: Two-stage Miller-compensated op-amp [Joh97].

- The two gain stages ensure that sufficient gain is provided to ensure a strong virtual ground, while Miller compensation performs pole splitting to improve stability.
- The use of a two-stage architecture, in contrast to increasing gain through the use of cascodes in a single-stage architecture, significantly improves signal-swing at the amplifier's output, required for low-voltage operation.

Additionally, the current buffers (M_B in Fig. 5.6(a)) needed to buffer the generated current signal to the compressors, process full-range sinusoidal swings, as the current signals

Table 5.4: Amplifier and current buffer circuit-simulation results.

Design Parameter	Value
Technology	0.13 μm CMOS
Amplifier (0.7 pF load)	
Gain	50.35 dB
Unity-gain frequency	4.84 MHz
Phase margin	44.31°
Slew rate	3.11 V/μS
Input-offset voltage	26 μV
Power Consumption	1.41 μW
Current Buffer (M_B)	
I_{Bias}	0.704 μA
Power Consumption	0.56 μW

have yet to be processed by the geometric-function generators. Therefore, I_{Bias} through M_{B1} must exceed the maximum expected swing, such that $I_{Bias} > i_{Comp,inp} = i_{Comp,inn}$.

The circuit-level simulation results of the amplifier and current buffer, tested individually, are summarized in Table 5.4. Here, the results reflect the evaluated capacitive load of 0.7 pF. The amplifier was initially designed to achieve a phase margin of approximately 50°. However, the capacitive load was underestimated during the initial design stage.

5.1.5 Summary

In this section, a series of modifications were introduced to previously proposed log-domain circuits to facilitate the low-distortion performance required for high-resolution $\Delta\Sigma$ modulators. Additionally, a novel differential-input differential-output expander is proposed. Observing Table 5.1, Table 5.2, and Table 5.3, while low-distortion compression comes at a power penalty, no additional power consumption is expected within the integrator, and a slight increase occurs in the case of the expander. The largest voltage-headroom penalty occurs within the integrator (V_{GS}).

The circuit-level simulation results of the loop-filter, and a comparison of the distortion

performance of the circuits in [Red05] and the low-distortion circuits presented here, is deferred to Section 5.3, following the loop-filter optimization procedure proposed in the next section.

5.2 Loop-Filter Performance Optimization

This section outlines the design of the class AB log-domain loop-filter to meet the targeted $\Delta\Sigma$ modulator design requirements. The optimization procedure presented relies on a combination of analytical analysis and circuit-level simulations

- **Analytical analysis** are required to derive the design trends and tradeoffs governing the relationships employed in the optimization procedure. A thorough understanding of the impact of the various parameters on the noise and distortion of the log-domain circuits is required to allow informed decisions while developing the optimization procedure.

- **Circuit-level simulations** allow for the speedy evaluation of the noise and distortion of complex circuits. Furthermore, the ability of SpectreRF simulations to evaluate the noise of individual components allows for quick identification of those components that require most attention, and ensures that the best design tradeoffs are implemented at the transistor level. To ensure that design parameters are not varied randomly during circuit-level simulations, an optimization procedure is required.

Accordingly, in this section the following is addressed

1. **Derivation of the performance trends and design tradeoffs:** A thorough investigation of the noise-power-distortion tradeoffs involved in log-domain $\Delta\Sigma$ modulators is presented in Section 5.2.1, Section 5.2.2, and Section 5.2.3. The purpose of the presented noise analysis is not to derive the exact relationships describing the noise, but to identify the trends in noise behaviour, allowing the derivation of the optimization process proposed in Section 5.2.4. It is noted that in the presented derivations,

all noise is referred to the $\Delta\Sigma$ modulator input $x(t)$ in Fig. 4.6. The resulting noise at the output is governed by the same trends, since the input-referred noise is subjected to the same transfer function as the input signal ($STF \approx 1$). The derived trends are confirmed in circuit-level simulations in Section 5.3.

2. **Proposal of an optimization procedure:** An optimization procedure is proposed in Section 5.2.4 that accounts for the impact of each design parameters on several performance measures as it is varied. The procedure accounts for the following performance measures: noise, distortion, power, speed, voltage-headroom, and area.

Implementing the optimization procedure involves circuit-level simulations to evaluate the noise (through SpectreRF PNoise analysis) and the distortion (through evaluation of the Total-Harmonic Distortion).

The factors determining the speed, voltage-headroom, and area, are well documented in the literature [Bin08], and are summarized in Table 5.5. Here, I_D, IC, L, and W are, respectively, the transistor's bias current, inversion-coefficient, length, and width. The changes in Table 5.5 are performed under the following conditions

- The transistor I_D is increased while maintaining constant IC and L by proportionally increasing W according to (4.74).

- The transistor IC is increased while maintaining content I_D and L by proportionally decreasing W according to (4.74).

- The transistor L is increased while maintaining constant I_D and IC by proportionally increasing W according to (4.74).

Table 5.5: CMOS transistor trends as the bias current I_D, inversion-coefficient IC, and transistor length L are varied [Bin08]. (WI: weak-inversion, MI: mild-inversion, SI: strong-inversion).

Parameter	**Increase in I_D** (IC and L constant)	**Increase in IC** (I_D and L constant)	**Increase in L** (I_D and IC constant)
Transistor bandwidth: $f_{BW,T}$	Does not vary	Increases in WI and MI Constant in SI with vel. sat.	Decreases
Transistor effective voltage: $V_{GS} - V_T$	Does not vary	Increases	Constant in WI and MI Decreases in SI with vel. sat.
V_{DS} at which transistor enters saturation: $V_{DS,sat}$	Does not vary	Does not vary in WI Increases in SI	Does not vary
Transistor area: WL	Increases	Decreases	Increases

5.2.1 Performance Trends: Compressors, Expander, and V/I - I/V Conversion Resistors

Distortion Resulting from Moderate Inversion

In Section 4.4.2 (Fig. 4.9), this work demonstrated the severe degradation in performance as log-domain devices leave the weak-inversion operating region.

In particular, even if a CMOS device is biased in weak-inversion, the large-signal nature of log-domain circuits raises the potential of log-domain devices deviating from weak-inversion performance as the signals reach their maximum amplitude. This concept is best demonstrated by observing the inversion coefficient equation, restated here for convenience

$$IC = \frac{i_D}{2\,\eta_0\,\mu_0\,C_{ox}\,U_T^2\,\left(\frac{W}{L}\right)} \tag{5.24}$$

Here, to reflect the large-signal nature of log-domain devices, I_D in (4.74) has been replaced

by the total current flowing through the transistor i_D, such that

$$i_D = I_D + i_d \tag{5.25}$$

The amplitude of the signal i_d is now expressed as a ratio of the bias current I_D through the factor λ, such that

$$i_{d,max} = \lambda I_D \tag{5.26}$$

where λ is the ratio of the maximum amplitude of the signal through the device to the device's bias current. The maximum IC that the device reaches at a given bias current I_D can now be expressed as

$$IC_{max} = \frac{I_D(1+\lambda)}{2\,\eta_0\,\mu_0\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)} \tag{5.27}$$

Accordingly, when $\lambda > 1$ such that $i_{d,max} > I_D$, the inversion coefficient more than doubles. As $i_{d,max}$ increases further beyond I_D, the inversion coefficient increases further, potentially resulting in the device deviating from weak-inversion operation. Accordingly, exponentially-behaving devices in class AB log-domain applications should be biased deep in weak-inversion. Furthermore, for high-resolution applications where aggressive low-distortion performance is required, the amplitude of the signals cannot be increased significantly beyond the bias currents.

Applying the relationship in (5.27) to the compressing transistors M_3 and M_{15} in Fig. 5.4, one gets

$$IC_{max} = \frac{I_{Comp}\left(1+\frac{i_{p,n-max}}{I_{Comp}}\right)}{2\,\eta_0\,\mu_0\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)} \tag{5.28}$$

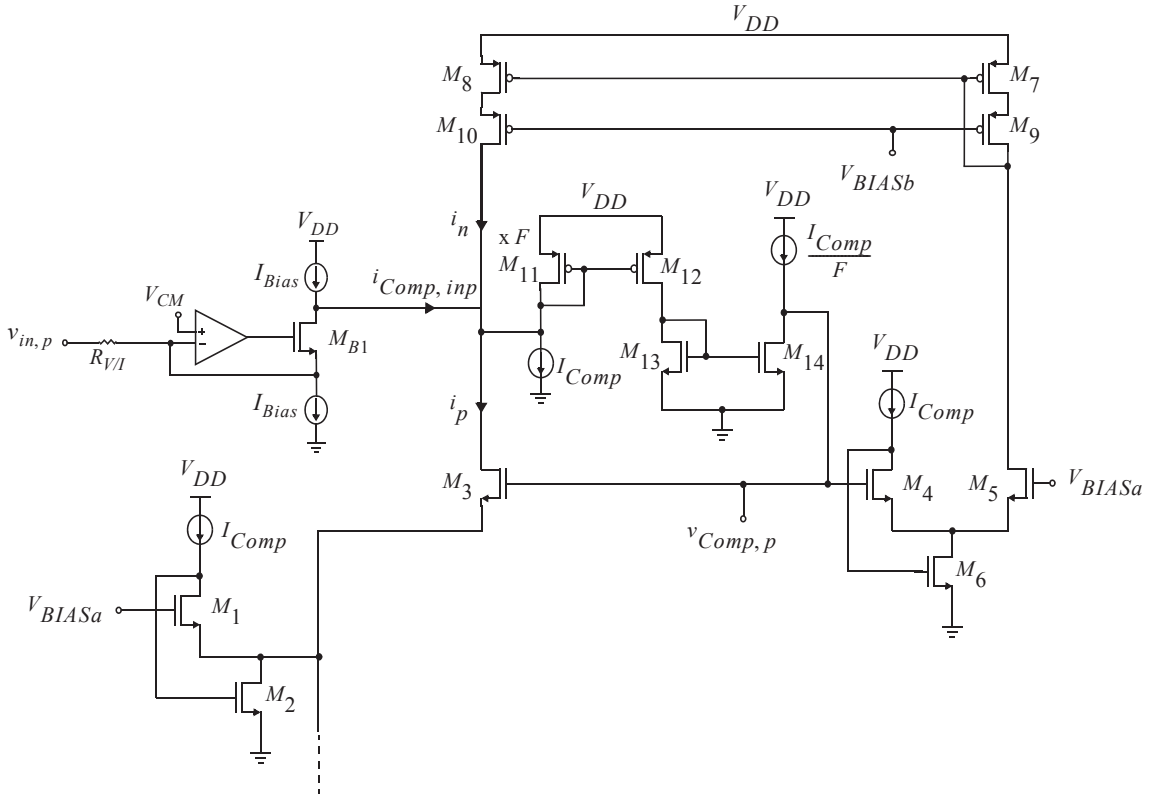


Figure 5.8: Positive-input path of the log-domain $\Delta\Sigma$ modulator, including the V/I conversation stage in Fig. 5.6(a) and the compressor in Fig. 5.4.

The signals $i_{p,n-max}$ are the maximum amplitude of signals $i_{p,n}$ (Fig. 5.4), the geometric-mean signals described by (5.15), (5.16) and (5.17).

To gain insight into the effect of R_{VI} and I_{Comp} on potential distortion resulting from moderate-inversion, it is desirable to express (5.28) in terms of R_{VI} and I_{Comp}. Figure 5.8 illustrates the positive input path of the log-domain $\Delta\Sigma$ modulator, comprised of the V/I conversation stage in Fig. 5.6(a) and the compressor in Fig. 5.4.

Considering the positive signal path, the current i_p can be derived by substituting (5.16) into (5.15) and solving for i_p

$$i_p = \frac{i_{Comp,inp} \pm \sqrt{i_{Comp,inp}^2 + 4I_{Comp}^2}}{2} \tag{5.29}$$

Next, the following relationship is established between the maximum of $i_{Comp,inp}$ and I_{Comp}

$$i_{Comp,inp-max} = \rho I_{Comp} \tag{5.30}$$

where $i_{Comp,inp-max}$ is the maximum amplitude of $i_{Comp,inp}$, and ρ is the ratio between the maximum amplitude and the bias current I_{Comp}. The maximum amplitude of signal i_p can now be expressed as

$$i_{p-max} = \frac{i_{Comp,inp-max} + \sqrt{i^2_{Comp,inp-max} + 4\left(\frac{i_{Comp,inp-max}}{\rho}\right)^2}}{2} \tag{5.31}$$

Simplifying (5.31)

$$i_{p-max} = i_{Comp,inp-max}\left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{1}{\rho^2}}\right) \tag{5.32}$$

In the latter equation, $i_{Comp,inp-max}$ can be expressed in terms of the voltage-to-current converting resistor R_{VI} preceding the compressor (Fig. 5.8)

$$i_{Comp,inp-max} = \frac{v_{in,p-max}}{R_{VI}} \tag{5.33}$$

where $v_{in,p-max}$ is the maximum voltage applied at the positive input of the $\Delta\Sigma$ modulator. Accordingly, (5.32) can now be expressed as

$$i_{p-max} = \frac{v_{in,p-max}}{R_{VI}}\left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{1}{\rho^2}}\right) \tag{5.34}$$

The dependance of i_{p-max} on ρ (and consequently I_{Comp}) can be determined by plotting the relationship in (5.34), as shown in Fig. 5.9. Observing Fig. 5.9, (5.34) is rearranged to

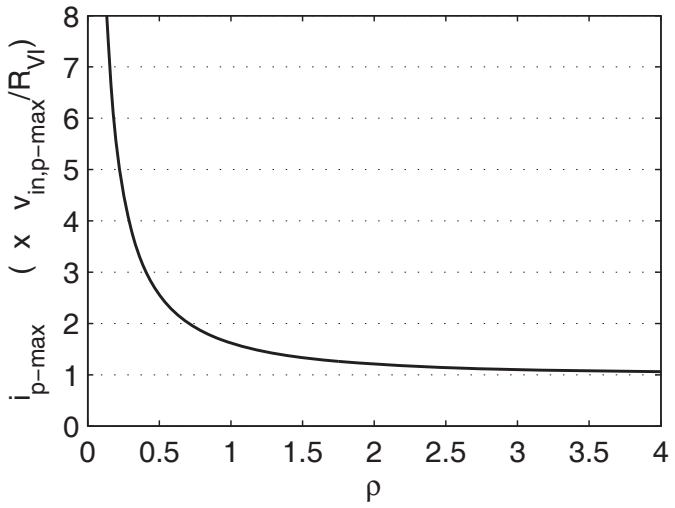


Figure 5.9: Input to compressing transistor $M3$ (Fig. 5.4) as a function of $\rho = i_{Comp,inp-max}/I_{Comp}$.

ease the optimization process, such that

$$i_{p-max} = \frac{v_{in,p-max}}{R_{VI}}\,\vartheta \tag{5.35}$$

where

$$\vartheta = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{1}{\rho^2}} \tag{5.36}$$

and ϑ is approximated as follows

$$\begin{aligned} \vartheta \approx 2 \quad &\text{for} \quad 0.5 < \rho = \frac{i_{Comp,inp-max}}{I_{Comp}} < 1 \\ \vartheta \approx 1.5 \quad &\text{for} \quad 1 < \rho = \frac{i_{Comp,inp-max}}{I_{Comp}} < 2 \\ \vartheta \approx 1 \quad &\text{for} \quad 2 < \rho = \frac{i_{Comp,inp-max}}{I_{Comp}} \end{aligned} \tag{5.37}$$

Substituting (5.35) into (5.28)

$$IC_{max} = \frac{I_{Comp}\left(1+\frac{v_{inp-max}}{R_{VI}\,I_{Comp}}\,\vartheta\right)}{2\,\eta_0\,\mu_0\,C_{ox}\,U_T^2\left(\frac{W}{L}\right)} \tag{5.38}$$

Observing (5.38), the following two conclusions are deduced:

1. The choice of R_{VI} and I_{Comp} determines the level of distortion resulting from variation in weak-inversion performance: if transistors M_3 and M_{15} are biased at a fixed IC (by fixing the ratio $I_{Comp}/(W/L)$), IC_{max} decreases as R_{VI} or I_{Comp} are increased.

2. IC_{max} remains approximately constant when R_{VI} or I_{Comp} are varied, as long as the product $R_{VI}\,I_{Comp}\,(1/\vartheta)$ is kept constant, and $I_{Comp}/(W/L)$ is fixed to maintain the transistor IC.

Noise

In this section, the noise trends of the log-domain $\Delta\Sigma$ modulator are identified as I_{Comp} and R_{VI} are varied. The selection of I_{Comp} and R_{VI} dictates I_{Exp} and R_{IV}, since, as noted in Chapter 4, $I_{Comp} = I_{Exp}$ and $R_{VI} = R_{IV}$. In contrast to the noise of the compressors and R_{VI}, which appear at the input of the modulator or feedback path, the noise of the expander and R_{IV} are heavily attenuated by the loop-filter. Therefore, the noise of the compressor and R_{IV} are only considered moving forward.

Observing Fig. 5.4 and Fig. 5.8, when referring the noise generated within the compressor to the compressor's input, designated here by the term $S_{Comp}^{Comp,in}(f)$, the resulting noise is dominated by the drain-referred noise of the various devices. The drain-referred

noise of an individual transistor can be described by the relationship in [Bin08].

$$\begin{aligned} S_{ID}(f) &= 4\,k\,T\frac{\Gamma\,I_{Comp}}{U_T\,\sqrt{IC+0.25}+0.5} \\ &\quad +2\left(\frac{IC}{L^2}\right)\left(\frac{I_{Comp}}{(\sqrt{IC+0.25}+0.5)^2}\right)\left(\frac{\mu_0\,C_{ox}}{\eta}\right)\frac{K'_{FO}}{f^{AF}}\left(1+\frac{2\,\eta\,U_T\,\sqrt{IC}}{V_{KF}}\right)^2 \end{aligned} \tag{5.39}$$

where the first term represents the thermal noise, and the second term represents the flicker noise. Here K'_{FO} is a flicker noise factor, V_{KF} is a voltage describing the dependancy of K'_{FO} on the level of channel inversion, η is the substrate factor, and AF is the flicker noise slope (which varies between 0.7 and 1.2, depending on CMOS technology and the choice of NMOS or PMOS device). Γ is a thermal noise factor that can be described by [Bin08]

$$\Gamma = \frac{1}{1+IC}\left(\frac{1}{2}+\frac{2}{3}IC\right) \tag{5.40}$$

and is approximately equal to one-half in weak-inversion, and two-thirds in strong-inversion.

In Fig. 5.8, the compressor's noise referred to the compressor's input, $S_{Comp}^{Comp,in}(f)$, can now be translated to the input of the $\Delta\Sigma$ modulator through the following relationship

$$S_{Comp}^{\Delta\Sigma,in}(f) = S_{Comp}^{Comp,in}(f) \times R_{VI}^2 \tag{5.41}$$

where $S_{Comp}^{\Delta\Sigma,in}(f)$ represents the noise of the compressor referred to the input of the $\Delta\Sigma$ modulator (between $v_{in,p}$ in Fig. 5.8 and its differential counterpart $v_{in,n}$).

The relationships in (5.39) and (5.41) provide insight into the noise behaviour of the compressors: Assuming IC of the transistors is kept constant, an increase of I_{Comp} or R_{VI} results in an increase of $S_{Comp}^{\Delta\Sigma,in}(f)$.

Finally, the resistors R_{VI} introduce thermal noise proportional to the value of R_{VI}

$$S_{R_{VI}}^{\Delta\Sigma,inp}(f) = 4kTR_{VI} \tag{5.42}$$

5.2.2 Integrators

The noise of the integrator in Fig. 5.2 referred to the integrator's input, $S_{Int}^{v,in}(f)$, is a function of the gate-referred noise of the integrator's transistors. The gate-referred noise of a transistor can be described by the following relationship [Bin08]

$$\begin{aligned} S_{VG}(f) &= 4kT\,U_T\,\eta^2\,\Gamma\left(\frac{(\sqrt{IC+0.25}+0.5)}{I_{Int}}\right) \\ &\quad +\frac{K'_{FO}I_0}{f}\left(\frac{IC}{L^2 I_{Int}}\right)\left(1+\frac{2\eta U_T\sqrt{IC}}{V_{KF}}\right)^2 \end{aligned} \tag{5.43}$$

where the first term represents the thermal noise, and the second term represents the flicker noise.

The integrator's noise referred to its input, $S_{Int}^{v,in}(f)$, is manifested at the outputs of the compressor (at the compressor-integrator junction, labelled $v_{Comp,p}$ and $v_{Comp,n}$ in Fig. 5.8). Observing Fig. 5.4 and Fig. 5.8, the noise can be referred to the input of the $\Delta\Sigma$ modulator through the transconductance g_m of the compressing transistors M_3 and M_{15}, and through the resistors R_{VI}, such that

$$\begin{aligned} S_{Int}^{\Delta\Sigma,in}(f) &= S_{Int}^{v,in}(f)\ \times\ g_m^2 \times\ R_{VI}^2 \\ &= S_{Int}^{v,in}(f)\ \times\ \left(\frac{I_{Comp}}{\eta\,U_T}\right)^2 \times\ R_{VI}^2 \end{aligned} \tag{5.44}$$

where $S_{Int}^{\Delta\Sigma,in}(f)$ is the noise of the first integrator referred to the input of the $\Delta\Sigma$ modulator, and $g_m = I_{Comp}/\eta U_T$ is the transconductance of a transistor biased in weak-inversion [Bin08]. Subsequent integrators are governed by the same trends, since the transfer function of preceding integrators is fixed by their respective I_{Int}/C ratios (4.60 - 4.62).

Accordingly, assuming the IC of all transistors is kept constant

1. An increase in I_{Int} results in the lowering of $S_{Int}^{\Delta\Sigma,in}(f)$.

2. An increase in I_{Comp} and R_{VI} results in an increase in $S_{Int}^{\Delta\Sigma,in}(f)$.

Table 5.6 summarizes the distortion and noise performance of a log-domain $\Delta\Sigma$ modulator as the various parameters of the compressor, expander, integrators, and V/I and I/V conversions are varied.

5.2.3 Design Tradeoffs and Limitiations

The proposed optimization procedure is dependant on the various tradeoffs involved, which are presented first.

Distortion-Noise-Power Tradeoffs: R_{VI} and I_{Comp}

Observing (5.39), (5.41), (5.42), (5.43), and (5.44), it can be deduced that a decrease in $R_{VI} = R_{IV}$, and a proportional increase in $I_{Comp} = I_{Exp}$ (such that $R_{VI}\, I_{Comp}$ remains approximately constant [5]) results in a decrease of $S_{Comp}^{\Delta\Sigma,in}(f)$ and $S_{R_{VI}}^{\Delta\Sigma,inp}(f)$ and no variation in $S_{Int}^{\Delta\Sigma,in}(f)$. However, the overall reduction in noise comes at the expense of increased power, due to the increase in $I_{Comp} = I_{Exp}$. Conversely, an increase $R_{VI} = R_{IV}$ and proportional decrease in $I_{Comp} = I_{Exp}$ improves the power performance at the expense of noise.

As noted in Section 5.2.1, the choice of $R_{VI} = R_{IV}$ and $I_{Comp} = I_{Exp}$ dictates the level of distortion resulting from inversion-coefficient variation. Observing (5.38), to lower such distortion, either R_{VI} or I_{Comp} can be increased (given the IC of the compressor's transistors remain fixed). Since a reduction in distortion comes at the expense of additional noise (increased R_{VI}) or additional power (increased I_{Comp}), an objective of the design procedure is not expend noise or power to reduce distortion beyond the targeted requirements. Therefore, the value of IC_{max} is arrived at early in the design process and kept constant throughout. The parameters $R_{VI} = R_{IV}$ and $I_{Comp} = I_{Exp}$ are then adjusted to achieve the targeted noise performance. The result is that minimum power is dissipated within the compressor and expander for the targeted noise and distortion performance.

[5] To simplify the presented analysis, it is assumed that $\rho > 0.5$ in (5.36). Final design parameters require slight modifications to adjust for the approximation.

Table 5.6: Distortion and noise performance of the log-domain $\Delta\Sigma$ modulator as parameters of the compressor, expander, integrators, and VI and IV conversion stages are varied.

Design Parameter	**Increase in** $R_{VI} = R_{IV}$	**Increase in** $I_{Comp} = I_{Exp}$ **(**IC **and** L **fixed)**	**Increase in** I_{Int} **(**IC **and** L **fixed)**	**Increase in** L **of Compressor/Expander transistors (**IC **and** I_D **fixed)**	**Increase in** L **of Integrator transistors (**IC **and** I_D **fixed)**
R_{VI} and R_{IV} noise	Increases	Does not vary	Does not vary	Does not vary	Does not vary
Compressor noise	Increases	Increases	Does not vary	Decreases when flicker noise dominates, becomes constant as thermal noise dominates	Does not vary
Possibility of distortion at compression due to moderate inversion	Decreases	Decreases	Does not vary	Does not vary	Does not vary
Integrator noise	Increases	Increases	Decreases	Does not vary	Decreases when flicker noise dominates, becomes constant as thermal noise dominates

Noise-Power Tradeoff: I_{Int}

As demonstrated in (5.43), an increase in I_{Int} results in a lowering of $S_{Int}^{\Delta\Sigma,in}(f)$. However, the improved noise performance comes at the expense of additional power. Additionally, since the noise of the integrator is also dependant on $R_{VI} = R_{IV}$ and $I_{Comp} = I_{Exp}$, the latter are arrived at first.

Speed-Area-Sizing Limitiations: L **and** W

Observing (5.39) and (5.43), an increase in the sizing of L (and proportional increase in W to maintain a constant IC) results in a lowering of the flicker noise. However, the improved noise performance results in a reduction in transistor speed and an increase in implementation area (Table 5.5). Additionally, the length and width of the devices may be limited by the device modeling within the circuit-design environment. Accordingly, L of the various devices is increased until thermal noise is dominant, or until the increase is limited by speed, area, or modeling restrictions.

5.2.4 Proposed Optimization Procedure

Employing the derived trends and tradeoffs presented in the previous sections, an optimization procedure is presented in this section. The implementation of the optimization procedure involves circuit-level simulations to evaluate the distortion and noise at each of the relevant design steps.

The following optimization procedure is proposed:

1. The IC of the compressor and expander's transistors are set to the desired value. This results in the fixing of $I_{Comp}/(W/L)$ in (5.38).

2. The resistances $R_{VI} = R_{IV}$ and bias-currents $I_{Comp} = I_{Exp}$ that result in the distortion requirements being met are determined. This results in an IC_{max}, according to (5.38).

3. The length L of critical transistors within the compressor and expander are increased (accompanied by a proportional increase in W according to (5.24) to maintain constant IC) until thermal noise dominates, or until the increase is limited by speed, area, or modeling restrictions.

4. The resistances $R_{VI} = R_{IV}$ and currents $I_{Comp} = I_{Exp}$ are varied to arrive at the targeted noise performance, while maintaing a constant $R_{VI}\, I_{Comp}\, (1/\vartheta)$ product such that IC_{max} in (5.38) remains constant, and while altering the widths W of the compressor and expander's transistors such that the inversion coefficients IC in (5.24) remain constant [6].

5. The inversion coefficients IC of the first integrator's transistors are set to the desired value.

6. The length L of the critical transistors within the integrator are increased (accompanied by a proportional increase in W to maintain constant IC) until thermal noise dominates, or until the increase is limited by speed, area, or modeling restrictions.

7. The bias-current I_{Int} is varied to arrive at the targeted noise performance of the integrator, while the width W of the various transistors is altered to maintain constant inversion coefficients IC of the various transistors. The capacitance C is also adjusted, to ensure that I_{Int}/C remains constant and satisfies (4.60).

8. Step 5, 6, and 7, are repeated for subsequent integrators.

Figure 5.10 provides a detailed representation of the proposed optimization procedure, including the selection sequence of the design parameters.

[6] If the increase in W is limited by area restrictions, W/L is increased by a factor κ by increasing W by a factor of $\sqrt{\kappa}$ and decreasing L by a factor of $\sqrt{\kappa}$, such that the area WL remains constant. If the increase in L is limited by speed restrictions, the increase in W does not result in degradation of the transistor's intrinsic bandwidth$f_{BW,T}$, since as noted in Table 5.5, increasing I_D while maintaining constant IC does not alter $f_{BW,T}$.

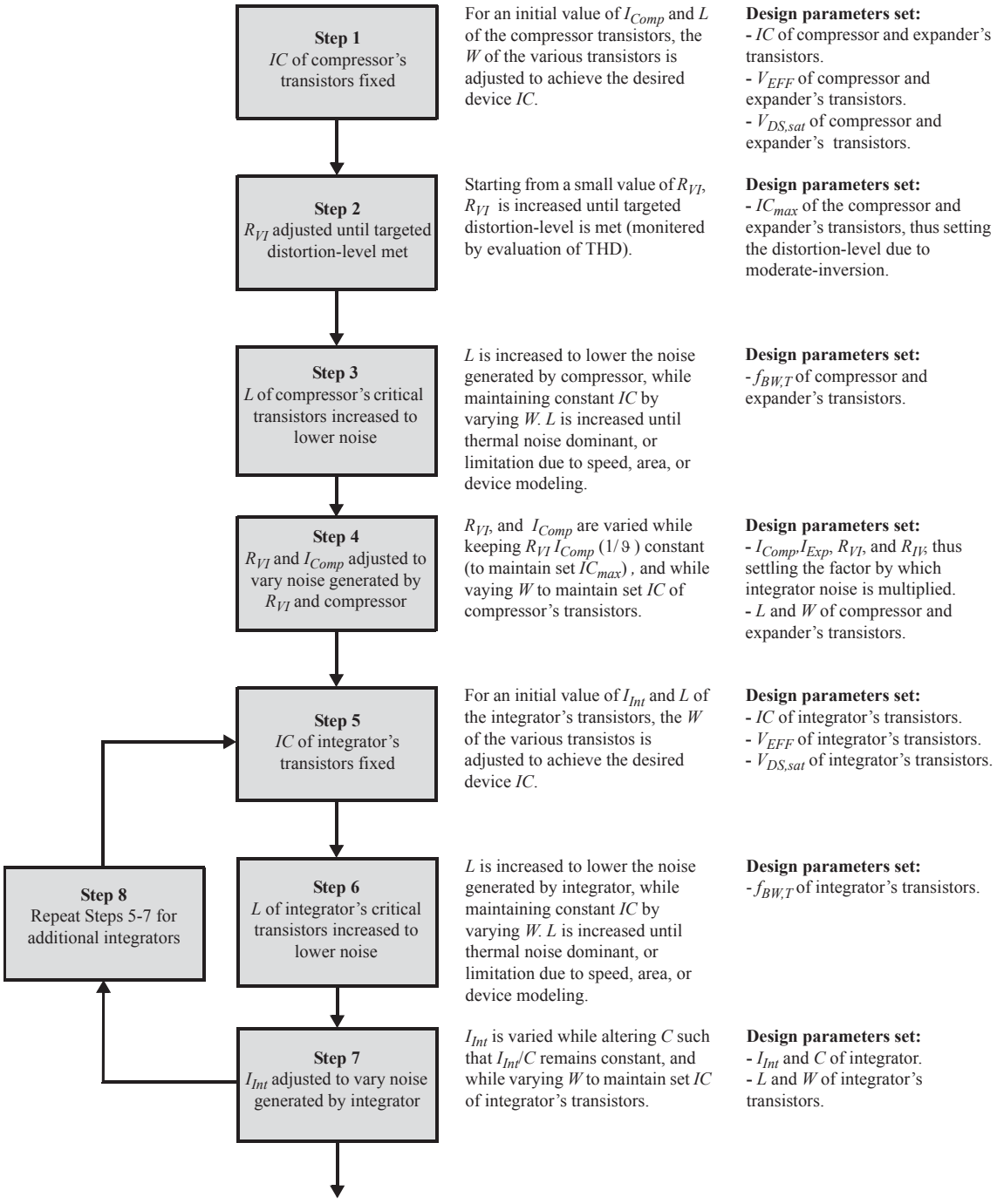


Figure 5.10: Proposed optimization procedure for log-domain $\Delta\Sigma$ modulator loop-filters.

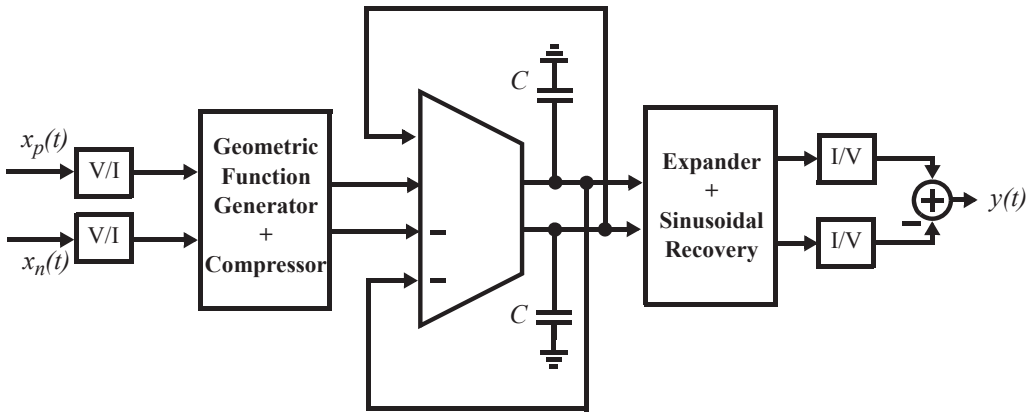


Figure 5.11: Setup for the evaluation of the noise of the compressor, expander, integrator, and V/I and I/V conversion resistors.

5.3 Simulation Results

In [Ng02], linear-periodic-time-varying analysis performed by the periodic-noise (PNoise) analysis in the SpectreRF simulator were utilized in the simulation of log-domain circuits; the results of the SpectreRF simulations were compared to the evaluation of derived noise expressions, and were demonstrated to be approximately equal.

Here, in addition to employing the SpectreRF PNoise analysis, the following simulations benefit from the noise-separation tool within the PNoise analysis to identify the trends of the individual log-domain components.

5.3.1 Noise Trends

The setup in Fig. 5.11 facilitates the evaluation of the noise of the compressor, expander, integrator, and the V/I and I/V conversion resistors as $R_{VI} = R_{IV}$, $I_{Comp} = I_{Exp}$, and I_{Int} are varied. Here the geometric function generator and compressor is implemented using the circuit in Fig. 5.4, the expander is implemented using the circuit in Fig. 5.5, the integrator is implemented using the circuit in Fig. 5.2, and the V/I and I/V conversion stages are implemented using the circuits in Fig. 5.6(a) and Fig. 5.6(b) respectively. Table

Table 5.7: Initial parameter values for the circuit-level simulations of the setup in Fig. 5.11.

Parameter	Value
V/I and I/V Conversion	
$R_{VI} = R_{IV}$	200 kΩ
Compressor and Expander	
$I_{Comp} = I_{Exp}$	2.2 μA
Compressing, expanding, and level-shift transistors	
IC	0.033
L	2.4 μm
Current-mirror and cascode transistors	
IC	0.65
L	1.2 μm
Current-sink transistors	
IC	1.5
L	1.2 μm
Integtrator	
I_{Int}	2.2 μA
Integrating, level-shift, and CMFB transistors	
IC	0.033
L	1.2 μm
Current-mirror and cascode transistors	
IC	0.65
L	1.2 μm
Current-sink transistors	
IC	1.5
L	1.2 μm

5.7 summarizes the initial values of the parameters employed in the simulations described by the results in Fig. 5.12, Fig. 5.13, and Fig. 5.14.

Figure 5.12 demonstrates the variation of the noise generated by R_{VI} and R_{IV}, the compressor, and the integrator as the magnitude $R_{VI} = R_{IV}$ is varied. Figure 5.13 demonstrates the variation of the noise generated by the compressor and integrator as $I_{Comp} = I_{Exp}$ is varied (IC kept constant). Finally, Fig. 5.14 demonstrates the variation of the integrator noise as I_{Int} is varied (IC kept constant). The circuit-level simulations confirm the noise trends derived in Section 5.2.1.

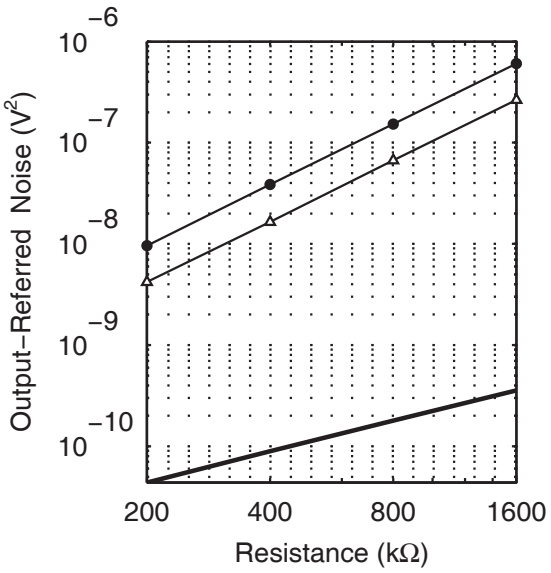


Figure 5.12: Integrated output-referred noise as $R_{VI} = R_{IV}$ is varied (f_{BW} = 10 kHz). **Here: — = R_{VI} noise; △ = compressor noise; and -●- = integrator noise.**

5.3.2 Proposed 3rd-order class AB loop-filter

The optimization procedure proposed in Section 5.2.4 is employed to generate a 3rd-order class AB $\Delta\Sigma$ modulator loop filter in 0.13 μm CMOS technology, demonstrated in Fig. 5.15. Similar to Fig. 5.11, the geometric function generators and compressors are implemented using the circuit in Fig. 5.4, the expander is implemented using the circuit in Fig. 5.5, the integrators are implemented using the circuit in Fig. 5.2, and the V/I and I/V conversion stages are implemented using the circuits in Fig. 5.6(a) and Fig. 5.6(b) respectively. In the setup, the feedback V/I conversion resistors are assumed to be noiseless, since it will be demonstrated in Chapter 6 that they are eliminated by employing a proposed current-output DAC. The elimination of the V/I conversion resistors in the feedback results in the halving of the R_{VI} noise contributions of the loop-filter.

The selected bias currents and sizing of the various devices in the resulting implementation are summarized in Table 5.8. The following is noted:

- The length of critical devices was increased to lower flicker noise, reaching a maxi-

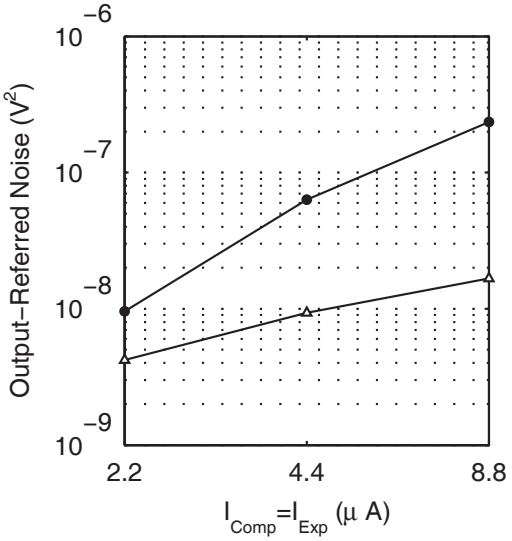


Figure 5.13: Integrated output-referred noise as $I_{Comp} = I_{Exp}$ is varied (f_{BW} = 10 kHz). **Here: △ = compressor noise; and -●- = integrator noise.**

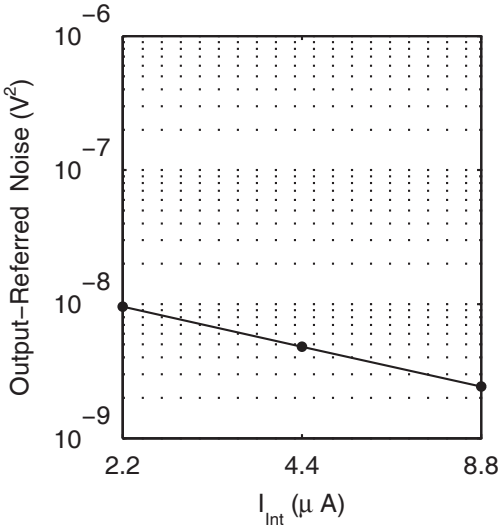


Figure 5.14: Integrated output-referred noise as I_{Int} is varied (f_{BW} = 10 kHz).

mum L of 4.8 μm. The limitation is imposed by the diminished accuracy of model extraction in 0.13 μm technology beyond that limit [7].

- The compressing, expanding, CMFB, level-shift, and integrating transistors [8] are biased deep in weak-inversion ($IC \ll 0.1$) to minimize deviation of the transistor's operating equation from the exponential relationship.

- The current mirrors and cascode transistors [9] are biased in mild-inversion ($0.1 \leq IC \leq 1$) instead of strong inversion. This results in a lowering of the gate and drain-referred flicker noise dominant in the targeted low-bandwidth application (f_{BW} = 10 kHz).

[7] The reader is referred to the IBM CMRF8SF Model Reference Guide. Ver: Nov. 22, 2010. Model: V1.8.0.0.

[8] Figure 5.4: M_1, M_3, M_4, M_5, M_{15}, M_{16}, M_{17}. Figure 5.5: M_1, M_2, M_3. Figure 5.2: M_1, M_2, M_5, M_7, M_8, M_9, M_{10}, M_{13}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{21}, M_{22}.

[9] Figure 5.4: M_7, M_8, M_{19}, M_{20}, M_9, M_{10}, M_{21}, M_{22}, M_{11}, M_{12}, M_{23}, M_{24}. Figure 5.5: M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}. Figure 5.2: M_3, M_4, M_{11}, M_{12}, M_{23}, M_{24}, M_{25}, M_{27}, M_{28}.

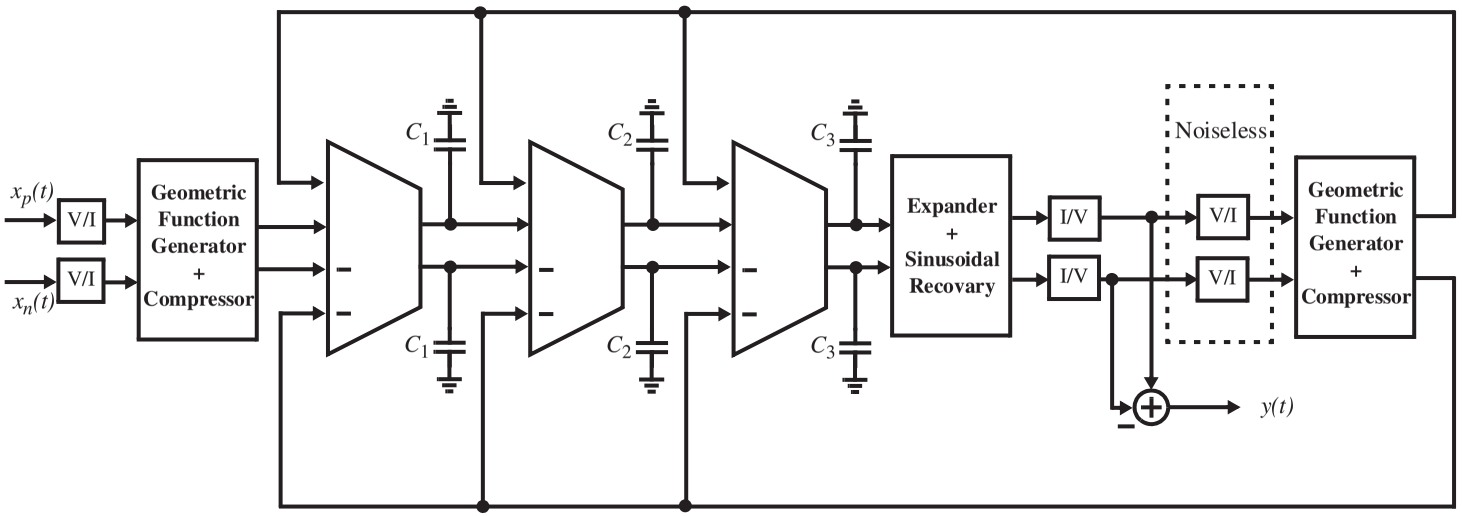


Figure 5.15: Proposed 3rd-order class AB log-domain ΔΣ modulator loop-filter. The geometric function generators and compressors are implemented using the circuit in Fig. 5.4, the expander is implemented using the circuit in Fig. 5.5, the integrators are implemented using the circuit in Fig. 5.2, and the V/I and I/V conversion stages are implemented using the circuits in Fig. 5.6(a) and Fig. 5.6(b) respectively. Optimized design parameters are listed in Table 5.8.

- The length of all transistors is large to reduce flicker noise. The exception are the cascode devices, due to the lowering of their noise through source degeneration.

- It is noted that the magnitude of C_1, C_2, and C_3 is significantly large. Observing (4.60) - (4.62), the ratio I_{Int}/C is dependant on the coefficients a_1, a_2, and a_3, and the sampling frequency f_s, of the equivalent continuous-time modulator in Fig. 4.5. As noted in (4.65) - (4.67), the coefficients of traditional continuous-time $\Delta\Sigma$ modulators are typically the same order of magnitude. Therefore, the magnitude of the ratio I_{Int}/C is determined primarily by the sampling frequency f_s. Accordingly for a given bandwidth f_{BW}, one of the methods to reduce the capacitances C is through a larger OSR [10]. This comes at the expense of more stringent performance requirements on the digital components. This relationship was observed after fabrication of the experimental prototype described by the values in Table 5.8.

- The current-sinking transistors [11] are biased close to strong inversion to maintain a large V_{GS}. This is required to provide sufficient voltage-headroom across two devices (in the case of M_2 in Fig. 5.4, $V_{GS,2} > V_{DS,sat,1} + V_{DS,sat,2}$). The same principle is applied to the current-sinking transistors in the expander and compressor.

- Integrator 2 requires less bias current I_{Int} than integrator 1, since the noise generated by integrator 2 is subjected to more aggressive noise shaping. Integrator 3, in turn, requires less I_{Int} than integrator 2. The result of more aggressive noise shaping is also reduced transistor L in integrators 2 and 3.

- The final IC of some transistors reported in Table 5.8 deviate from the initial design values. This is attributed to layout considerations, and the use of common layout cells to implement various components.

[10] The OSR is defined in (2.3) as $OSR = f_s/(2 \times f_{BW})$.
[11] Figure 5.4: M_2, M_6, and M_{18}. Figure 5.5: M_4. Figure 5.2: M_6, M_{14}, M_{20}.

Table 5.8: Parameter values for the 3rd-order class AB log-domain $\Delta\Sigma$ modulator loop-filter.

Parameter	Value
V/I and I/V Conversion	
$R_{VI} = R_{IV}$	800 kΩ
Compressor (Fig. 5.4)	
I_{Comp}	450nA
M_1, M_3, M_4, M_5, M_{15}, M_{16}, M_{17}	
IC / L / W	0.015 / 4.8 μm / 192 μm
M_7, M_8, M_{19}, M_{20}	
IC / L / W	0.1 / 4.8 μm / 12 μm
M_9, M_{10}, M_{21}, M_{22}	
IC / L / W	0.5 / 1.2 μm / 6 μm
M_{11}, M_{12}, M_{23}, M_{24}	
IC / L / W	0.35 / 3.6 μm / 4.5 μm
M_{13}, M_{14}, M_{25}, M_{26}	
IC / L / W	0.015 / 3.6 μm / 28.8 μm
M_2, M_6, M_{18}	
IC / L / W	4.85 / 4.8 μm / 1.4 μm
Expander (Fig. 5.5)	
I_{Exp}	450nA
M_1, M_2, M_3	
IC / L / W	0.015 / 4.8 μm / 192 μm
M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}	
IC / L / W	0.5 / 1.2 μm / 9 μm
M_{17}, M_{18}, M_{19}, M_{20}, M_{21}, M_{22}, M_{23}, M_{24}	
IC / L / W	1.1 / 3.6 μm / 1.8 μm
M_4	
IC / L / W	4.6 / 4.8 μm / 1.4 μm
Integrator 1 (Fig. 5.2)	
I_{Int1} / C_1	728 nA / 260 pF
M_1, M_2, M_5, M_7, M_8, M_9, M_{10}, M_{13}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{21}, M_{22}	
IC / L / W	0.012 / 4.8 μm / 384 μm
M_3, M_4, M_{11}, M_{12}	
IC / L / W	0.2 / 4.8 μm / 86.4 μm
M_{24}, M_{25}, M_{27}, M_{28}	
IC / L / W	0.2 / 1.2 μm / 21.6 μm
M_{23}	
IC / L / W	0.08 / 1.2 μm / 36 μm
M_6, M_{14}, M_{20}	
IC / L / W	5.2 / 1.4 μm / 1.4 μm
Integrator 2 (Fig. 5.2)	
I_{Int2} / C_2	464 nA / 76 pF
M_1, M_2, M_5, M_7, M_8, M_9, M_{10}, M_{13}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{21}, M_{22}	
IC / L / W	0.007 / 1.2 μm / 96 μm
M_3, M_4, M_{11}, M_{12}, M_{24}, M_{25}, M_{27}, M_{28}	
IC / L / W	0.5 / 1.2 μm / 6 μm
M_{23}	
IC / L / W	0.18 / 1.2 μm / 12 μm
M_6, M_{14}, M_{20}	
IC / L / W	13.6 / 5.6 μm / 1.4 μm
Integrator 3 (Fig. 5.2)	
I_{Int3} / C_3	257 nA / 26 pF
M_1, M_2, M_5, M_7, M_8, M_9, M_{10}, M_{13}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{21}, M_{22}	
IC / L / W	0.004 / 1.2 μm 96 μm
M_3, M_4, M_{11}, M_{12}, M_{24}, M_{25}, M_{27}, M_{28}	
IC / L / W	0.27 / 1.2 μm / 6 μm
M_{23}	
IC / L / W	0.1 / 1.2 μm / 12 μm
M_6, M_{14}, M_{20}	
IC / L / W	7.94 / 5.6 μm / 1.4 μm

Table 5.9: Log-domain $\Delta\Sigma$ loop-filter simulation results.

Design Parameter	Value
Technology	0.13 μm CMOS
Order	3rdorder low-pass $\Delta\Sigma$ loop-filter
Supply voltage	0.8 V
Maximum differential input amplitude	0.6 V
SNDR (at 0.42 V differential input amplitude, 10 kHz bandwidth)	65.4 dB
THD	- 68.9 dB
Power consumption	
Geometric function generators and compressors	7.78 μW
Expander	2.92 μW
Integrator 1	8.94 μW
Integrator 2	5.67 μW
Integrator 3	3.14 μW
Amplifiers (4 V/I amplifiers and 2 I/V amplifiers, Table 5.4)	8.49 μW
Current Buffers (4 V/I buffers, Table 5.4)	2.25 μW
Total	**39.19 μW**

Figure 5.16 shows the output spectrum of the loop-filter evaluated through circuit-level simulations. Table 5.9 summarizes the circuit-level simulation results. The loop-filter achieves a maximum SNDR of 65.4 dB at a differential input amplitude of 0.42 V, and a Total Harmonic Distortion (THD) of -68.9 dB. The total loop-filter power consumption is found to be 39.19 μW. Observing Table 5.9, the majority of power is consumed in the V/I and I/V converters' amplifiers, the compressors and expander, and the first integrator. Successive integrators consume less power due to the increased noise-shaping at later stages of the loop-filter. The power consumption in the V/I and I/V converters, and the compressors and expanders, is dictated by the distortion performance of the loop-filter, where it is necessary to provide sufficient bias-current to allow low-distortion class AB log-domain operation.

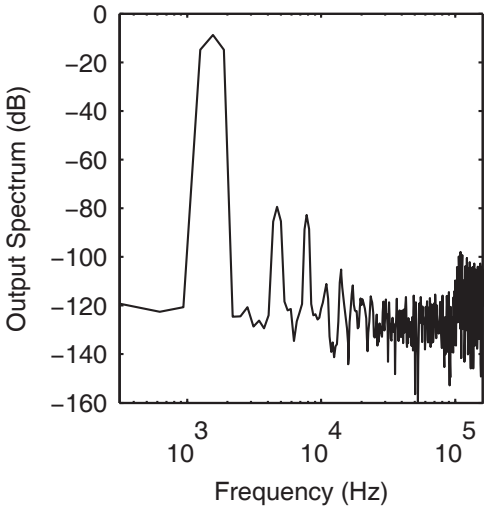


Figure 5.16: Output spectrum (circuit-level simulations) of the proposed low-distortion log-domain loop-filter. **THD = -68.9 dB**.

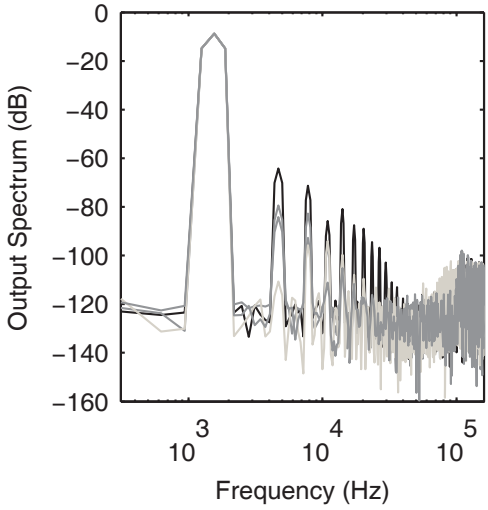


Figure 5.17: Output spectrum (circuit-level simulations) of the proposed low-distortion log-domain loop-filter as $I_{Comp} = I_{Exp}$ is varied. **Here: light grey = $I_{Comp} = I_{Exp}$ = 900 nA; grey = $I_{Comp} = I_{Exp}$ = 675 nA; ; charcoal = $I_{Comp} = I_{Exp}$ = 450 nA; ; black = $I_{Comp} = I_{Exp}$ = 225 nA.**

5.3.3 Distortion Trends

To demonstrate the distortion trends discussed in this chapter, the following changes were introduced to the proposed loop-filter in Section 5.3.2

- The effect of altering IC_{max} (5.38) of the compressing and expanding transistors was explored by varying $I_{Comp} = I_{Exp}$ while altering the width of transistors to maintain constant IC.

- The advantages of the proposed low-distortion log-domain components in Section 5.1 were demonstrated by selectively substituting some of the components in the proposed log-domain loop-filter with their counterparts proposed in [Red05].

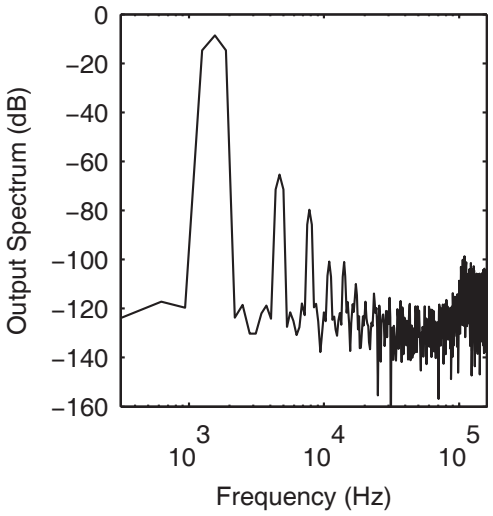


Figure 5.18: Output spectrum (circuit-level simulations) of a log-domain loop-filter with the low-distortion compressor and expander presented here (Fig. 5.4 and Fig. 5.5), and the integrator in [Red05] (Fig. 5.1). **THD = -56.7 dB**.

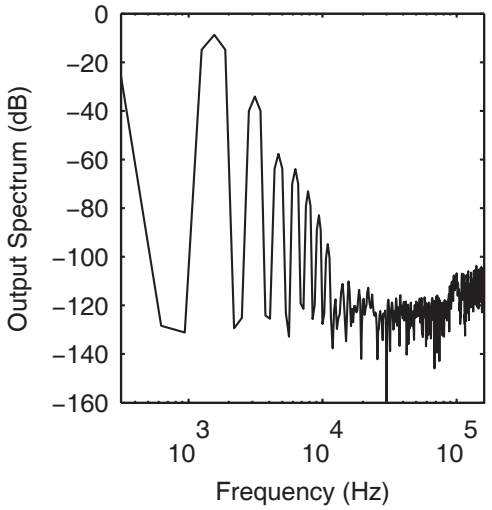


Figure 5.19: Output spectrum (circuit-level simulations) of a log-domain loop-filter with the compressor in [Red05] (Fig. 5.3(a)), and the low-distortion integrator and expander presented here (Fig. 5.2 and Fig. 5.3(b)). **THD = -25.3 dB**.

Figure 5.17 demonstrates the variation of the output spectrum as $I_{Comp} = I_{Exp}$ (and consequently IC_{max}) is varied. The THD of the loop filter is -54.6 dB, -68.9 dB, -74.9 dB, and -86.8 dB as $I_{Comp} = I_{Exp}$ is adjusted to equal 225 nA, 450 nA, 675 nA, and 900 nA respectively. The results demonstrate that at a given $R_{VI} = R_{IV}$ the loop-filter's THD performance benefits from an increase in $I_{Comp} = I_{Exp}$. However, this results in increased power consumption, and as demonstrated in Fig. 5.13, increased noise.

Figure 5.18 demonstrates the loop-filter performance resulting from substituting the low-distortion integrators in Fig. 5.2 with the integrator proposed in Fig. 5.1 [Red05] (the wide-swing cascode current mirrors introduced in Fig. 5.2 are retained). Removal of the cascode transistors (M_{23} and M_{26} in Fig. 5.2) results in a degradation of the distortion performance, with a resulting THD of -56.7 dB.

Figure 5.19 demonstrates the loop-filter performance resulting from substituting the low-distortion compressor in Fig. 5.4 with the compressor proposed in 5.3(a) [Red05]

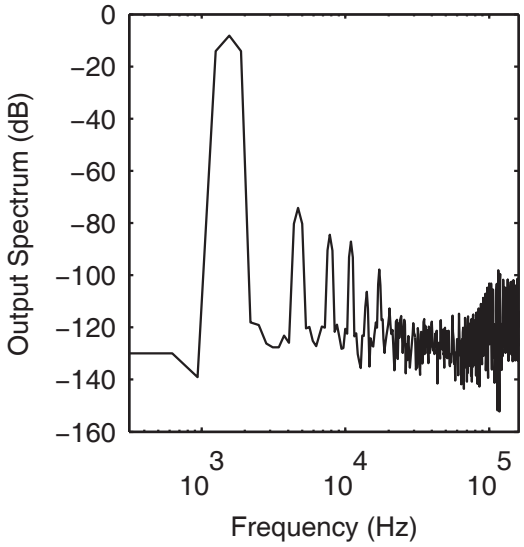


Figure 5.20: Output spectrum (circuit-level simulations) of a log-domain loop-filter with the expander in [Red05] (Fig. 5.3(b)), and the low-distortion compressor and integrator presented here (Fig. 5.4 and Fig. 5.2). **THD = -65.7 dB**.

(the wide-swing cascode current mirrors introduced in Fig. 5.4 are retained). The results (THD = -25.3 dB) demonstrate a severe degradation of performance resulting from the non-symmetrical compression differential paths in [Red05]. In addition to the increase in magnitude of odd-ordered harmonics, even-ordered harmonics are introduced. The results demonstrate the necessity of symmetrical compression paths in low-distortion log-domain applications.

Figure 5.20 demonstrates the loop-filter performance resulting from substituting the proposed low-distortion expander in Fig. 5.5 with the expander in 5.3(b) [Red05] (the wide-swing cascode current mirrors introduced in Fig. 5.5 are retained). The results (THD = -65.7 dB) demonstrate a 3.2 dB degradation of the THD when compared to the low-distortion realization presented here (Fig. 5.16). The loss in THD performance is not as severe as in the case of the compressor (Fig. 5.19) due to the noise and distortion generated by the expander being shaped by the loop-filter transfer function. It is noted however, that in $1^{st}$and 2^{nd}-order log-domain $\Delta\Sigma$ modulators, and in classical log-domain filters, the expander in [Red05] would be expected to result in significant distortion.

Table 5.10: Comparison of the distortion performance of various class AB log-domain loop-filters employing the low-distortion log-domain circuits presented in this work [Sha14b] and the log-domain circuits presented in [Red05].

Test Setup	Integrators	Compressors	Expander	Output Spectrum	THD
1 (proposed loop-filter)	**[Sha14b]**	**[Sha14b]**	**[Sha14b]**	**Fig. 5.16**	**-68.9 dB**
2	[Red05]	[Sha14b]	[Sha14b]	Fig. 5.18	-56.7 dB
3	[Sha14b]	[Red05]	[Sha14b]	Fig. 5.19	-25.3 dB
4	[Sha14b]	[Sha14b]	[Red05]	Fig. 5.20	-65.7 dB

Table 5.10 summarizes the distortion performance of the various circuit configurations discussed.

5.4 Summary

In this chapter, the development of a low-distortion class AB log-domain loop-filter that realizes the targeted design specifications was outlined. Adjustments to the compressor and integrator in [Red05] to allow low-distortion performance were presented. Additionally, a novel differential-input differential-output expander was proposed that realizes low-distortion performance without a significant increase in power consumption. Circuit-level simulation results demonstrate the necessity of the proposed modifications in the realization of the targeted performance.

Furthermore, trends involved in the design of log-domain circuits were demonstrated through theoretical derivations and circuit-level simulations. The complexity of optimizing log-domain circuits is apparent in the dual role of some design parameters, as their variation not only alters the inherent noise of their associated component, but, as demonstrated, also alters the relationship of other noise sources with respect to the $\Delta\Sigma$ modulator input and output. A novel optimization procedure that accounts for the complexity of the various fac-

tors was proposed. The concepts developed here and the optimization procedure proposed can be extended to other log-domain circuit applications.

CHAPTER 6

Current-output DAC for low-noise feedback

IN THE loop-filter proposed in Section 5.3.2 (Table 5.8), the resistors $R_{VI} = R_{IV}$ are significantly larger ($\times$ 4), and the currents $I_{Comp} = I_{Exp}$ are significantly smaller (approximately $\times$ 1/5), than those employed in the derivation of the performance-trends (Table 5.7). Furthermore, the length of critical devices has has also been increased (when compared to Table 5.7), lowering transistor flicker noise in the integrators and compressors. Therefore the noise of the resistors represents a significant contribution to the overall noise budget (when compared to the trends reported in Fig. 5.12). In this chapter, a novel current-output DAC is proposed that eliminates the R_{VI} conversion resistors in the $\Delta\Sigma$ modulator feedback path, thus reducing by one-half the noise contribution of the V/I conversion resistors in the log-domain $\Delta\Sigma$ modulator. The chapter demonstrates how appropriately

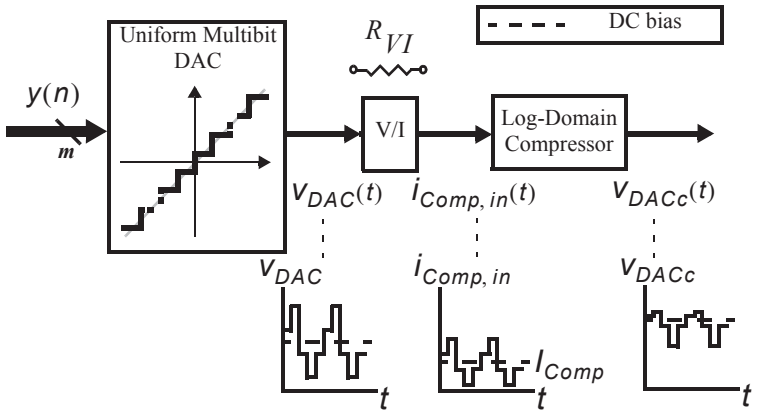


Figure 6.1: An implementation of the m-bit log-domain DAC in Fig. 4.3, with an embedded voltage-to-current conversion stage.

scaled switched-current elements and the introduction of additional current sources enable the realization of a full current swing at the proposed DAC output, and evaluates the design parameters required to achieve the required signal swing within a $\Delta\Sigma$ modulator loop. Analysis and simulation of the various design tradeoffs involved is presented, and it is demonstrated that the proposed current-output DAC is suitable for very low-power applications with low-to-medium speed requirements.

6.1 Digital-to-Analog Conversion in Log-Domain $\Delta\Sigma$ ADCs

As outlined in Chapter 4, a practical realization to generate the step-sizes described by (4.11) and (4.12) is the placement of a compressor following a uniform-step-size DAC. The feedback path in Fig. 4.6 is highlighted in Fig. 6.1. Since it is necessary to deliver an input current ($i_{Comp,in}$ in Fig. 5.8 and Fig. 6.1) into the log-domain compressor, the use of traditional voltage-output DACs in the feedback path would necessitate a voltage-to-current conversion stage prior to the compressor (R_{VI} in Fig. 6.1).

Similar to the V/I conversion resistor prior to the compressor at the input of the log-domain $\Delta\Sigma$ modulator (Fig. 5.8), a conversion resistor R_{VI} introduces $4kTR$ thermal

noise at the input of the feedback compressor, which appears unattenuated at the output of the $\Delta\Sigma$ modulator. Observing Fig. 4.6 and Fig. 6.1, the noise contribution of resistor R_{VI} at the modulator output y is found to be

$$\begin{aligned} S^{y}_{R_{VI}}(f) &= 4kTR_{VI}\left(\frac{LF}{1+LF}\right)^2 \\ &\cong 4kTR_{VI} \qquad 0 \leq f \leq f_{BW} \end{aligned} \tag{6.1}$$

Here LF is large ($LF \gg 1$) within the signal bandwidth f_{BW}, as is typical in $\Delta\Sigma$ modulator implementations, which allows for the approximation in (6.1).

Observing (6.1), the noise contribution of the feedback V/I conversion stage is proportional to R_{VI}, which, as demonstrated in (5.38), may be increased to minimize IC_{max} without increasing I_{Comp}. Eliminating R_{VI} and realizing a current-output DAC in the feedback path eliminates the associated R_{VI} noise in the feedback path.

6.2 Circuit Implementation

Traditionally, various architectures have been employed to generate voltage-output DACs [Joh97]. Particularly, current-steering DACs rely on current-steering unit-elements and resistors to generate voltage-output step-sizes [Mik86].

Figure 6.2 proposes a mutlibit current-output DAC that eliminates the need for a conversion resistor R_{VI} by employing switched-current unit-elements commonly employed in current-steering DACs. Here, instead of applying the unit-elements to a resistor to generate an output voltage [Mik86], the unit-elements are scaled to generate the required current step-sizes.

In Fig. 6.2, common-gate transistors M_{Gp} and M_{Gn} feed the input signals to the feedback splitter-compressor. The amplifiers ensure that the voltage bias at the output of the current-steering architecture is not left floating. Employing the amplifiers and common-gate transistors does not result in an additional power penalty when compared to the im-

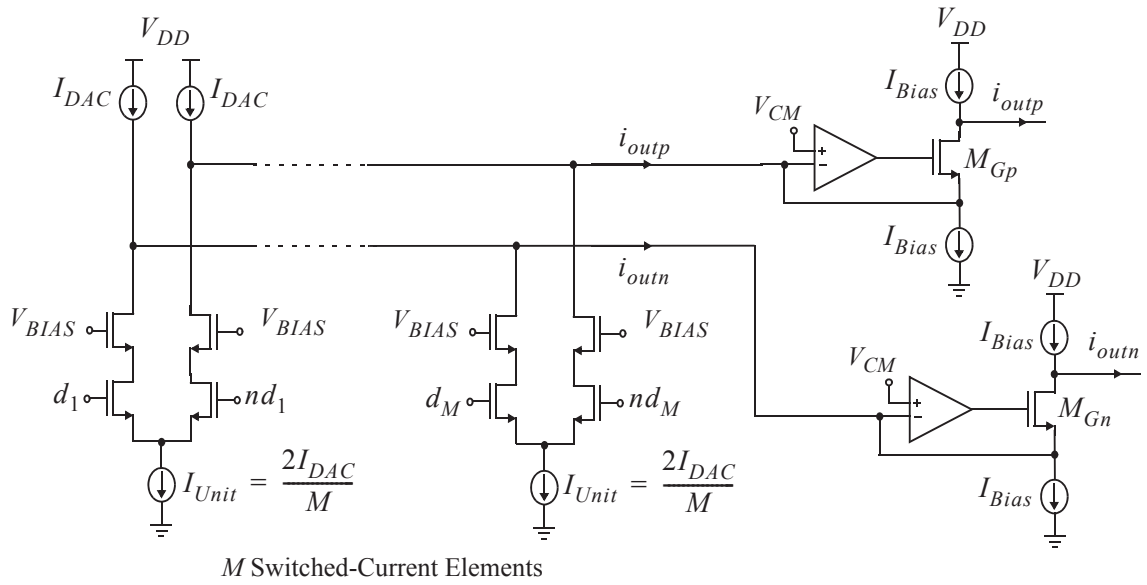


Figure 6.2: Proposed current-output DAC with differential-output amplitude I_{DAC}, eliminating voltage-to-current conversion resistor R_{VI} in Fig. 6.1.

plementation in Fig. 6.1, as a similar amplifier and common-gate stage is required when a voltage-to-current conversion stage precedes a compressor (Fig. 5.8).

The current-sources I_{Unit}, I_{DAC}, and I_{Bias} are implemented using wide-swing cascode current-mirrors. The op-amps employ a traditional two-stage Miller-compensated architecture [Joh97]. The current I_{Bias} is selected to allow the maximum amplitude of $i_{outp,n}$ (equivalent to I_{DAC}) to flow through the common gate transistors, such that $I_{Bias} > I_{DAC}$.

6.3 Generation of the DAC Transfer Curve

To determine the required step-sizes, Δ_{DAC}, and the individual current-steering bias-currents, I_{Unit}, in Fig. 6.2, both the quantization and digital-to-analog conversion processes within the multibit log-domain $\Delta\Sigma$ modulator have to be considered together (Fig. 6.3(a)). Since quantization and digital-to-analog conversion within a $\Delta\Sigma$ modulator are ideally inverse processes[1], the differential-ended DAC step size, $\Delta_{DAC,diff}$ is tied to the differential quan-

[1] The additive white noise model assumes no variation in gain when quantization noise is introduced [Gra97].

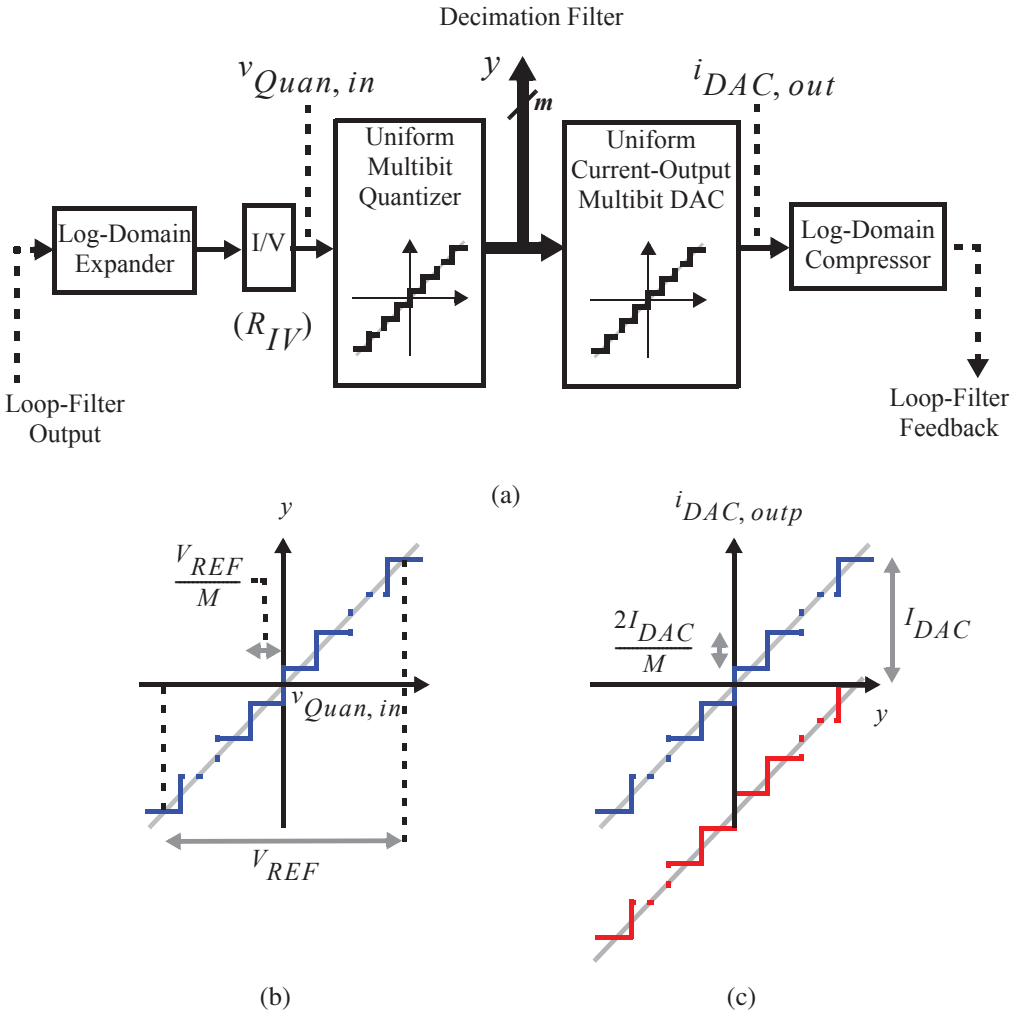


Figure 6.3: Realization of the proposed current-output DAC transfer curve, eliminating the voltage-to-current conversion resistor R_{VI} in Fig. 6.1. a) Quantizer and DAC path, b) Quantizer transfer curve, c) Proposed DAC single-ended transfer curve with (blue) and without (red) I_{DAC} in Fig. 6.2.

tizer step-size $\Delta_{Quan,diff}$ through the desired current-to-voltage conversion factor prior to the quantizer (dictated by resistor R_{IV} in Fig. 6.3(a), applied across the transimpedance amplifier as in Fig. 5.6(b)), such that

$$\Delta_{DAC,diff}(i) \;=\; \frac{\Delta_{Quan,diff}}{R_{IV}} \;=\; \frac{2\,V_{REF}}{R_{IV}\,M} \tag{6.2}$$

Here V_{REF} is the single-ended quantizer reference voltage. Figure 6.3(b) demonstrates the quantizer transfer curve.

Since $\Delta_{DAC,diff} = 2\,\Delta_{DAC}$, where Δ_{DAC} is the single-ended DAC current step-size, and by observing Fig. 6.2, where $\Delta_{DAC} = 2\,I_{DAC}/M$, then

$$\frac{4\,I_{DAC}}{M} = \frac{2\,V_{REF}}{R_{IV}\,M} \tag{6.3}$$

and

$$I_{DAC} = \frac{V_{REF}}{2\,R_{IV}} \tag{6.4}$$

The M switched-current elements facilitate the sinking of current from the compressor stage during negative signal swings of i_{outp} or i_{outn}. However, the current-output DAC is expected to generate both positive and negative signal swings. By applying a current source I_{DAC} at the drain of the M switched-current elements in Fig. 6.2, both positive and negative signal swings can be generated at the output, which is set to a maximum of $\pm I_{DAC}$ in (6.4) by employing unit-elements with a weight of $2\,I_{DAC}/M$. Figure 6.3(c) illustrates the shift of the DAC transfer curve through the introduction of the current source I_{DAC}, and the generated step-sizes. The resulting transfer curve is described by

$$i_{outp} = I_{DAC} - \left(nd_1 \frac{2I_{DAC}}{M} + ... + nd_M \frac{2I_{DAC}}{M} \right) \tag{6.5}$$

$$i_{outn} = I_{DAC} - \left(d_1 \frac{2I_{DAC}}{M} + ... + d_M \frac{2I_{DAC}}{M} \right) \tag{6.6}$$

Here, signals d_1 ... d_M and their inverse nd_1 ... nd_M are the DAC logic inputs, and are either high (1) or low (0).

6.3.1 Design Tradeoffs

A primary design objective in the proposed DAC is the minimization of noise. The gate-referred noise (thermal and flicker) of the transistors in Fig. 6.2 can be expressed by (5.43), re-expressed here for the DAC

$$\begin{aligned} S_{VG}(f) &= 4kT\,U_T\,n^2\,\Gamma\left(\frac{(\sqrt{IC+0.25}+0.5)}{I_{Unit}}\right) \\ &\quad +\frac{K'_{FO}I_0}{f}\left(\frac{IC}{L^2 I_{Unit}}\right)\left(1+\frac{2nU_T\sqrt{IC}}{V_{KF}}\right)^2 \end{aligned} \tag{6.7}$$

where I_{Unit} is the bias of the switched-current elements in Fig. 6.2.

Observing (6.7), it is apparent that as I_{DAC}, and subsequently I_{Unit}, are lowered to suit the needs of low-power applications, the noise of the DAC increases. Accordingly, for low-power applications, it is necessary to bias the DAC transistors in moderate-to-weak inversion (to decrease IC), and increase their physical dimensions L and W. The increase in the transistors' dimensions also results in improved transistor matching, and hence reduced distortion in the $\Delta\Sigma$ modulator feedback path. The reduced current-bias and increased physical dimensions do result in a reduction of the DAC speed. However, due to the inherent high-speed of current-steering DACs, the lower speed resulting from large transistor sizes does not result in significant degradation of the performance in low-power low-bandwidth applications.

6.4 Circuit Simulation Results

In this section, the proposed DAC performance is evaluated as multiple design parameters are varied. Specifically, the response of the DAC speed and noise performance is investigated as the bias current of the DAC unit-elements, the level of channel inversion, and the length of the transistor are varied.

The DAC in Fig. 6.2 was designed using a 0.13 μm CMOS technology. The circuit was

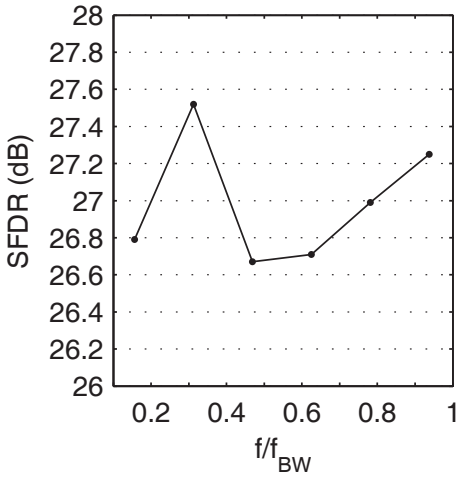


Figure 6.4: SFDR variation as a function of the input signal frequency, over the span of the $\Delta\Sigma$ modulator bandwidth (f_{BW} = 10 kHz).

optimized for very low power systems targeting low-frequency biomedical applications. Specifically, the resulting DAC was designed to meet the following specifications

- 7-level (3-bit) quantizer and DAC.
- $\Delta\Sigma$ Modulator bandwidth f_{BW} = 10 kHz. sampling frequency f_s = 320 kHz.
- Quantizer V_{REF} = 600 mV, and current-to-voltage conversion factor (R_{IV}) = 800 kΩ (I_{DAC} = 375 nA).

Figure 6.4 demonstrates the variation of the DAC SFDR as a function of the signal frequency. The complete DAC simulation results are summarized in Table 6.1. The DAC was tested by applying an ideal 3-bit quantized sine-wave at the input.

Table 6.1 corresponds to the best trade-off for the targeted application [2]. Other applications may require different specifications. Thus, to demonstrate the variation in dynamic and noise performance as the design parameters are varied, the optimized DAC (Table 6.1) was resimulated as the bias-current I_{Unit}, the inversion-coefficients, and the lengths of the multiple devices comprising the M switched-elements was varied by an equal factor.

[2] The quantization process performed prior to the tested DAC, reflected in the SFDR in Table 6.1, is noise-shaped by the $\Delta\Sigma$ modulator loop.

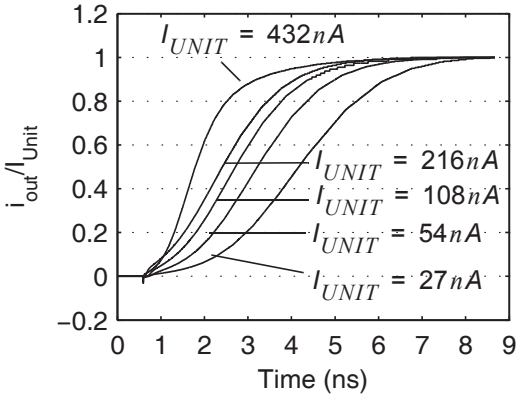


Figure 6.5: Normalized step-response variation as the switched-elements current bias I_{UNIT} is varied.

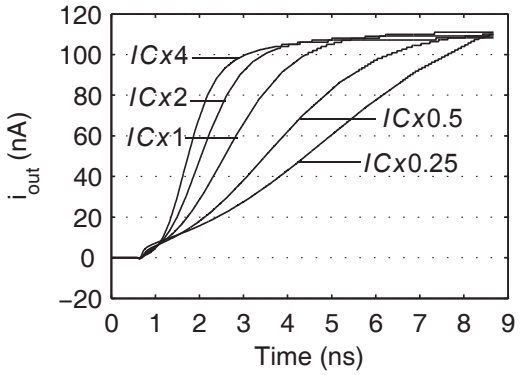


Figure 6.6: Step-response variation as the inversion coefficient IC of the devices comprising the switched-elements are scaled by an equal factor.

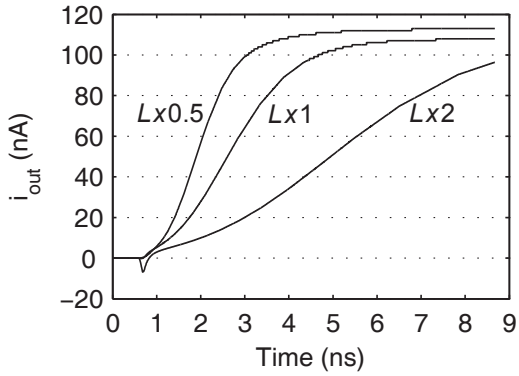


Figure 6.7: Step-response variation as the length L of the devices comprising the switched-elements are scaled by an equal factor (W/L kept constant).

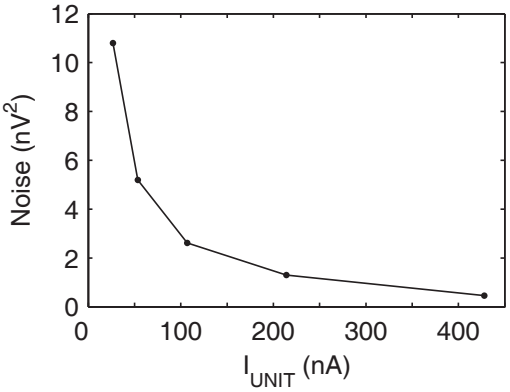


Figure 6.8: Integrated noise variation (f_{BW} = 10 kHz) as the switched-elements current bias I_{UNIT} is varied.

Figures 6.5 and 6.8 explore the variation of the DAC's settling-time and input-referred noise as I_{Unit} is varied. If I_{Unit} is reduced to target lower power applications, the settling-time of the DAC and the gate-referred transistor noise increases. In contrast, increasing the transistors' inversion-coefficients through the decrease of the transistors' widths (Fig. 6.6 and Fig. 6.9), or decreasing the transistor lengths (Fig. 6.7 and Fig. 6.10) results in improved dynamic performance at the expense of noise. Accordingly, once the selection of I_{Unit} is performed for a particular $\Delta\Sigma$ log-domain ADC architecture (the choice of which is

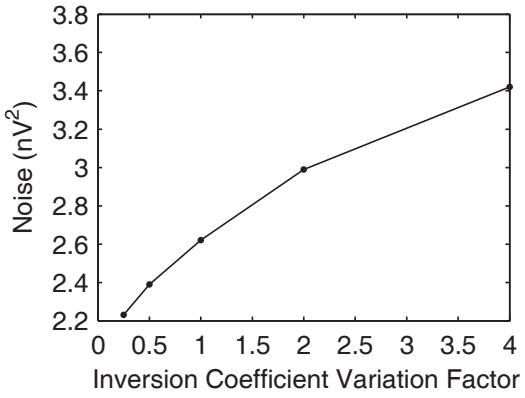


Figure 6.9: Integrated noise variation (f_{BW} = 10 kHz) as the inversion coefficient IC of the devices comprising the switched-elements are scaled by an equal factor.

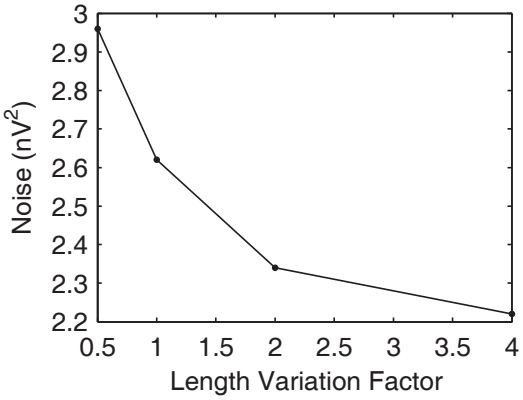


Figure 6.10: Integrated noise variation (f_{BW} = 10 kHz) as the length L of the devices comprising the switched-elements are scaled by an equal factor (W/L kept constant).

Table 6.1: DAC circuit-simulation results.

Design Parameter	Value
Technology	0.13 μm CMOS
Single-ended amplitude I_{DAC}	375 nA
Number of quantization levels M	7 (3-bit)
DAC unit-element size ($2\,I_{DAC}/M$)	107 nA
Differential step size	214 nA
Update rate	320 kHz
DAC input-referred noise	Floor: 2.66e^{-13} V^2/Hz
	1/F corner: 1 kHz
Delay (250 ns clock rise time)	5.11 ns
SFDR (over 10 kHz bandwidth range)	$>$ 26.7 dB
Supply Voltage	800 mV
Power consumption	
M switched-current elements	600 nW
Amplifiers and current buffers	3.92 μW

dependant on the power requirements, quantizer V_{REF}, and R_{IV}), the inversion coefficient and length of the various devices are altered to arrive at the required noise-speed tradeoff (dictated by the ADC resolution and bandwidth).

6.5 Summary

A novel low-power low-noise current-output DAC suitable for multibit log-domain $\Delta\Sigma$ modulators is presented. The selection of the DAC design parameters was demonstrated in light of the $\Delta\Sigma$ modulator architecture requirements, enabling full signal swings while eliminating the use of a voltage-to-current conversion stage and its associated noise in the feedback path. Realizing the targeted power-resolution-speed tradeoff was explored in light of the multiple design variables. The presented work and design approach can be extended to other applications requiring current-output DACs.

CHAPTER 7

Implementation and Results

THIS chapter presents the circuit-level realization and simulation results of the overall $\Delta\Sigma$ modulator, the layout of the fabricated prototype, and the experimental results of the fabricated prototype. Section 7.1 presents the design specifications of the 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator, including an overview of the quantizer and digital circuits. In Section 7.2, the simulation results in Chapter 4, Chapter 5, and Section 7.1, are employed to evaluate the performance of the proposed modulator. The layout of the fabricated prototype is presented in Section 7.3, and the experimental results are presented in Section 7.4. A comparison of the performance of the proposed $\Delta\Sigma$ modulator with previously reported state-of-the-art implementations is discussed in Section 7.5.

7.1 Implementation of 3rd-order 3-bit Class AB Log-Domain $\Delta\Sigma$ Modulator

The implemented modulator targets high-resolution ($>$ 10 bits) ADCs suitable for biomedical applications, and is expected to operate with a bandwidth f_{BW} = 10 kHz while minimizing power consumption. A 3rd-order 3-bit architecture was selected to provide adequate noise shaping without significantly suffering from degraded stability performance observed in high-order $\Delta\Sigma$ modulators. An OSR of 16, and subsequently a sampling frequency f_s = 320 kHz[1], was selected to relax the speed requirement of the digital circuits and to reduce the effects of clock-jitter and excess-loop-delay. A 3-bit internal quantizer ensures sufficient SQNR performance for the targeted application, and improves the stability of the 3rd-order loop-filter. Figure 7.1 summarizes the circuit implementation of the $\Delta\Sigma$ modulator, employing the loop-filter and DAC presented in Chapter 5 and Chapter 6, and including the quantizer and digital circuits presented in this section.

7.1.1 Maximum Amplitude and SNDR

An advantage of log-domain circuits is the inherent ability to maximize signal swing while operating at low supply voltages. Accordingly, the proposed modulator was designed to achieve an aggressive maximum-input-amplitude to supply-voltage ratio $v_{in,max}/V_{DD}$, while operating at aggressively low V_{DD}.

The largest voltage signal-swing occurs at the output of the V/I and I/V converter stage, where the expanded voltage swing of the log-domain $\Delta\Sigma$ modulator is generated. Accordingly, the I/V conversion amplifier in Fig 5.6(b) is critical in determining the $V_{DD,min}$ of the modulator. The two-stage Miller-compensated op-amp (Fig. 5.7) employed in the V/I and I/V conversion stages has a maximum output signal-swing of $V_{DD} - 2\,V_{DS,sat}$. Therefore, biasing the associated transistors in weak-to-mild inversion (with a $V_{DS,sat}$ of approxi-

[1] The OSR of a $\Delta\Sigma$ modulator was outlined in Section 2.2.1 and defined in (2.3).

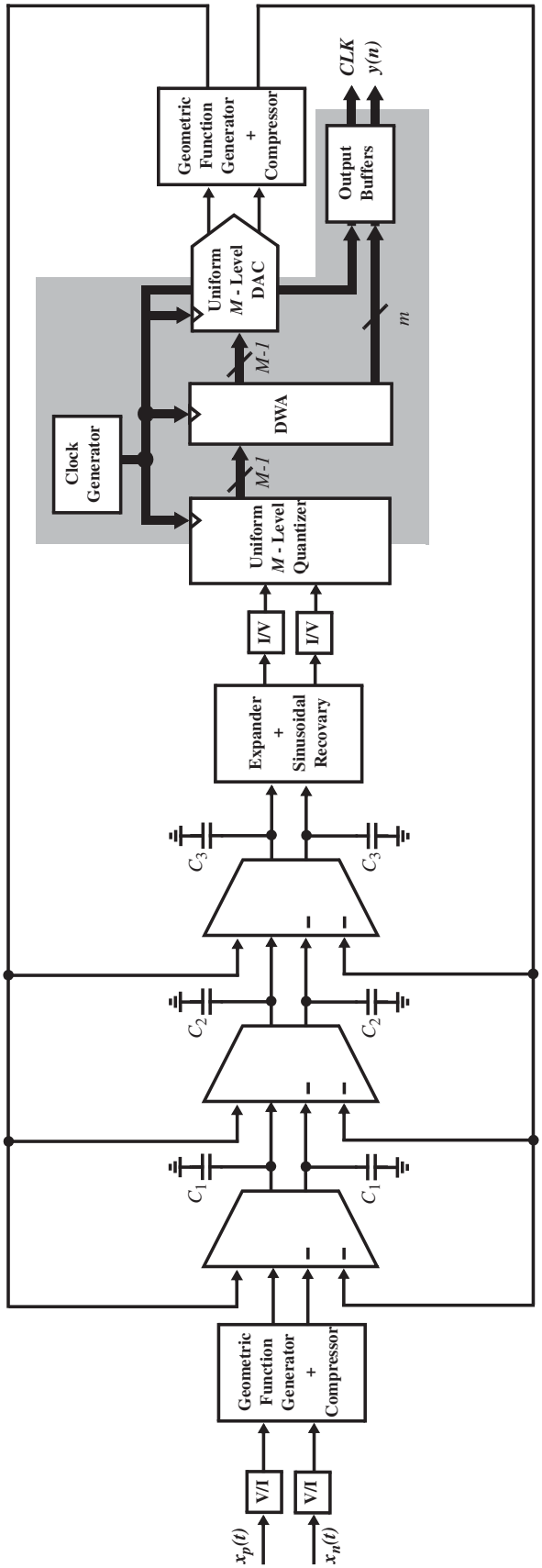


Figure 7.1: Block-diagram of the proposed multibit log-domain ΔΣ modulator. Areas highlighted in grey indicate digital processing.

mately [2] 0.1 V), and selecting $V_{CM} = V_{DD}/2$ in Fig. 5.6(b), results in a maximum signal swing of approximately $V_{DD} - 0.2$ V. For an aggressively low supply voltage of 0.8 V, the resulting single-ended signal swing can reach as high as 0.6 V.

7.1.2 Quantizer Implementation

A flash ADC, comprised of $M \equiv 2^m - 1$ comparators for a m-bit quantizer, can be employed in the quantization of the expanded output signal, as shown in Fig. 7.2 (the DAC is shown preceded by the I/V conversion stage in Fig. 5.6(b)). Here, a resistor ladder of $M + 1$ resistors generates the reference voltages applied to the differential comparators. Defining $V_{REF} = V_{REFp} - V_{REFn}$, the *differential* step-size (evaluated between the two differential quantizer outputs) between two consecutive quantizer threshold levels is given by

$$\Delta_{Quan,diff} = \frac{V_{REFp} - V_{REFn}}{2^m - 1} = \frac{2\,V_{REF}}{2^m - 1} \tag{7.1}$$

The latched comparators in Fig. 7.2 are each comprised of a preamplifier and a latch, shown in Fig. 7.3. Use of a preamplifier prior to the latch reduces the kickback noise from the latch to the comparator's inputs. For multibit flash ADCs operating at low V_{DD}, decreasing $\Delta_{Quan,diff}$ results in increasingly demanding preamplifier input-offset requirements.

In order to increase the differential-pair transconductance, an amplifier featuring additional current sources at the drain [Gre99] was employed, resulting in high-gain preamplifiers, as depicted in Fig. 7.3. Figure 7.3 also depicts the latch circuit implementation. Particular care was taken in sizing the clocking transistors since larger sizing of the transistors results in increased kickback noise.

The choice of the quantizer's reference voltages V_{REFp} and V_{REFn} (Fig. 7.2) is dependent on the $\Delta\Sigma$ modulator's maximum signal swing, and is set to equal the maximum tolerable signal swing at the loop-filter output. This design choice results in the utilization

[2] For a CMOS transistor biased in weak-inversion, the V_{DS} at which the CMOS transistor enters saturation can be approximated by $V_{DS,sat} = 4\,U_T$, independent of L and I_D [Bin08].

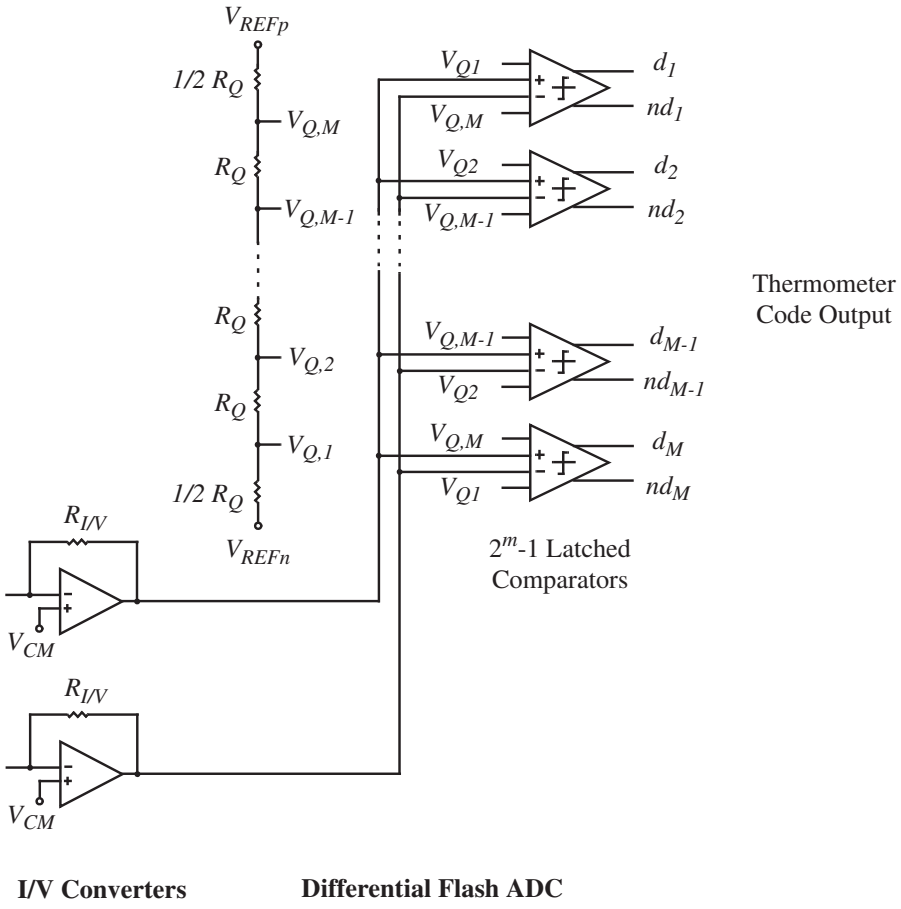


Figure 7.2: Circuit Implementation of current-to-voltage conversion (Fig. 5.6(b)) and quantizer.

of all the quantizer's threshold-levels at the maximum signal swing, while ensuring that the quantizer is not overloaded by the maximum swing generated by the analog circuits. Additionally, it is desirable to select the quantizer's input common-mode voltage V_{CM} such that the signal swing is maximized.

As outlined in Section 7.1.1, the maximum signal swing at the output of the I/V converter is 0.6 V, achieved when the output of the I/V converter is biased at $V_{DD}/2$. Accordingly, V_{CM} (Fig. 7.2) is adjusted to 0.4 V and V_{REFp} and V_{REFn} are adjusted to 0.7 V and 0.1 V, respectively.

The circuit-level simulations of the quantizer are summarized in Table 7.1.

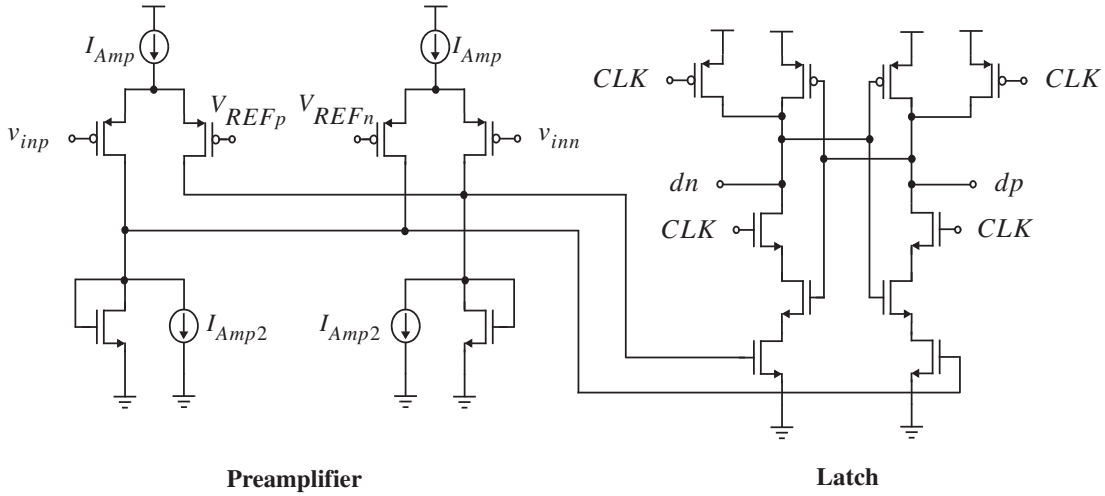


Figure 7.3: Circuit implementation of latched comparator comprised of preamplifier and latch.

Table 7.1: Quantizer circuit-simulation results.

Design Parameter	Value
Single-ended resistor string V_{REF}	0.6 V
Number of quantization levels M	7
Differential step size $\Delta_{Quan,diff}$ ($2\,V_{REF}/M$)	171 mV
Input common-mode bias	0.4 V
Differential comparator offset voltage (1σ)	8.4 mV (4.2 mV single-ended)
Latch kickback on preamplifier	9.7 mV
Preamplifier input-referred noise	Floor: 2.57e^{-13} V^2/Hz 1/F corner: 10 kHz
Preamplifier DC gain	5.84 dB
Preamplifier power	500 nW
Resistance ladder resistance	60 kΩ
Resistor String Power	1.43 μW
Total power consumption (7 preamplifiers and resistor string)	4.93 μW

7.1.3 Digital Logic

The digital logic (highlighted in grey in Fig. 7.1) includes the DWA logic, the clock generator, and output buffers. Figure 7.4 shows the implementation of the DWA algorithm. A 3-bit logarithmic shifter shifts the quantizer's 7-level thermometer code output (d), determined by a 3-bit pointer (ptr) evaluated during the previous clock sample. A thermometer-to-

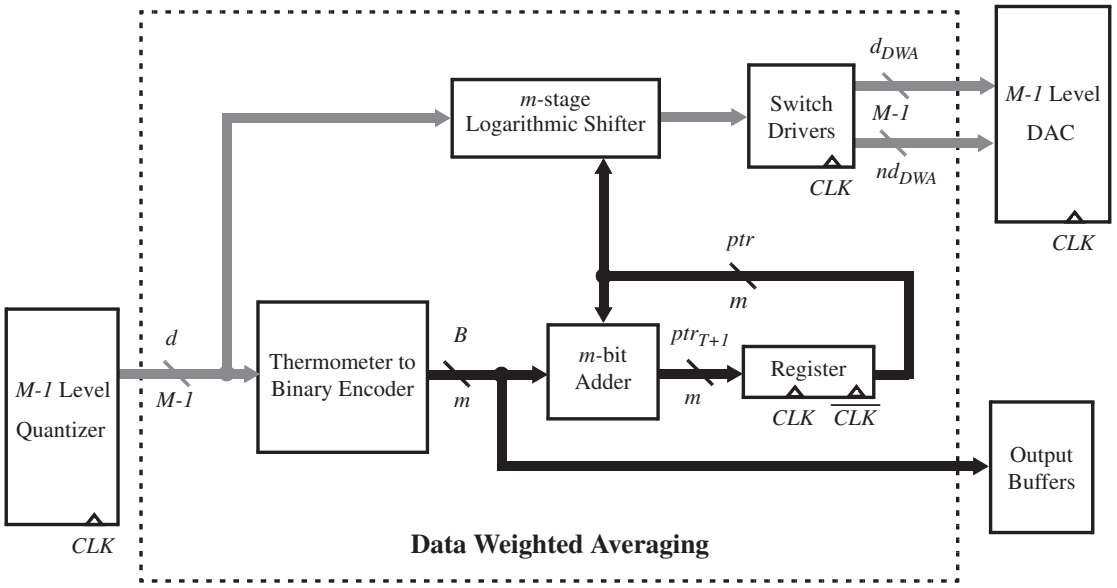


Figure 7.4: Data-Weighted-Averaging (DWA) implementation for *m*-bit $\Delta\Sigma$ modulator ($M = 2^m - 1$) (Signals in grey are thermometer coded, while signals in black are binary coded).

binary encoder generates a 3-bit binary output (B) from the 7-level thermometer code d. The binary code (B), representing the output of the $\Delta\Sigma$ modulator, is sent off-chip through the output buffers. A 3-bit carry-around adder computes the position of the pointer for the next cycle by performing a carry-around addition of the previous pointer (ptr_{T+1}) and the present sample's binary output (B). Switch drivers ensure the logarithmic shifter correctly drives the current-steering DAC transistors.

Standard digital algorithmic blocks are employed in the realization of the circuits in Fig. 7.4. Since the $\Delta\Sigma$ modulator operates at low speeds, the speed requirements of the DWA blocks are significantly relaxed.

Since continuous-time $\Delta\Sigma$ modulators do not require the complex non-overlapping clock signals needed in their discrete-time switched-capacitor counterparts, the on-chip clock signal in Fig. 7.1 was generated by applying the external clock input to an inverter chain, with an effective fan-out designed to ensure the generated clock signal can drive the

load of all digital logic. When needed, the inverse of the clock signal was generated locally within the associated algorithmic block.

7.2 Log-Domain $\Delta\Sigma$ Modulator Simulations Performance Summary

To accurately utilize the circuit-simulation results of the loop-filter to evaluate the performance of the log-domain $\Delta\Sigma$ modulator, it is necessary to measure the loop-filter's SNDR at the maximum input signal amplitude that is found not to overload the quantizer in the behavioural simulations. As noted in Section 7.1.1, the maximum tolerable swing of the analog components is dictated by the signal at the output of the I/V converter, and for the employed two-stage op-amp, the equivalent maximum swing is $V_{DD} - 2\,V_{DS,sat}$.

Observing the behavioural simulations in Section 4.4, the maximum SQNR is achieved at 0.7 V, a factor of 0.7 $\times V_{REF}$. Setting the quantizer's V_{REF} equal to the maximum tolerable swing of the analog components (0.6 V at a supply voltage of 0.8 V), the log-domain $\Delta\Sigma$ modulator's performance can be derived by equating the loop-filter's differential input voltage to 0.7 $\times$ 0.6 V = 0.42 V.

Due to the large-signal non-linear nature of the loop-filter internal signals, and the high-order of the presented loop-filter, a significantly large number of iterations are required to simulate the loop-filter in conjunction with the quantizer and DAC, resulting in the eventual overload of the simulator. Accordingly, the overall performance of the proposed log-domain $\Delta\Sigma$ modulator is derived from the circuit-level simulation results in Table 5.9 and the behavioural simulations in Section 4.4. To evaluate the impact of the quantizer comparators' and DAC's noise, the circuit noise of the quantizer (Table 7.1) and DAC (Table 6.1) were applied to their respective nodes in the behavioural model in Fig. 4.7 in Chapter 4, ensuring that the noise does not alter the reported SNDR (73.5 dB) in Section 4.4.

The overall SNDR, evaluated from the behavioural and circuit-level simulation results,

Table 7.2: Third-order 3-bit log-domain ΔΣ modulator expected performance from combined SpectreRF and behavioural simulation results.

Modulator Parameter	Value
Design Parameters	
Supply Voltage	0.8 V
Maximum differential Input Voltage	0.84 V
Bandwidth	10 kHz
OSR	16
Sampling Frequency	320 kHz
Circuit Layout	
Active Area	1.63 mm^2
Technology	0.13 μm
Simulated Results	
Analog Power (Loop-filter, quantizer, and DAC)	46.4 μW
Digital Power (DWA and Clock)	0.3 μW
Loop-Filter SNDR (at 0.42 V differential input)	65.4 dB
Quantization SNDR (at 0.42 V differential input)	73.5 dB
Calculated Performance	
Modulator Peak SNDR	64.8 dB
Figure-of-Merit	1.64 pJ/step

is determined from the following relationship [Ham04a] relating the signal to the total noise and distortion introduced by the loop-filter and quantizer

$$\mathrm{SNDR}_{\mathrm{Modulator}} = \left(\frac{1}{\mathrm{SNDR}_{\mathrm{LF}}} + \frac{1}{\mathrm{SNDR}_{\mathrm{Behavioural}}}\right)^{-1} \tag{7.2}$$

where SNDR_{LF} is the SNDR of the loop-filter and $\mathrm{SNDR}_{Behavioural}$ is the SNDR of the behavioural simulations, accounting for quantization noise and quantizer and DAC circuit noise.

The resolution of an ADC is defined by its Effective Number of Bits (ENOB)

$$\mathrm{ENOB} = \frac{\mathrm{SNDR}_{\mathrm{max,dB}} - 1.76}{6.02} \tag{7.3}$$

where $\mathrm{SNDR}_{max,dB}$ is the maximum SNDR of the modulator.

Employing the SNDR of the loop-filter in Table 5.9 ($SNDR_{LF}$ = 65.4 dB), and the SNDR of the behavioural simulations in Section 4.4.1 ($SNDR_{Behavioural}$ = 73.5 dB), the resulting SNDR is evaluated to be 64.8 dB, equivalent to a resolution of 10.47 bit. The expected behaviour of the proposed log-domain $\Delta\Sigma$ modulator is summarized in Table 7.2. The analog power consumption reported in Table 7.2 is comprised of the total loop-filter power consumption reported in Table 5.9, the quantizer power consumption reported in Table 7.1, and the power consumption of the DAC's unit-elements reported in Table 6.1. The power consumption of the DAC's amplifiers and currents buffers in Table 6.1 is already accounted for in the loop-filter power consumption reported in Table 5.9. The modulator achieves a Figure-of-Merit (FOM) of 1.64 pJ/step [3].

7.3 Fabricated Prototype Layout

A previous iteration of the $\Delta\Sigma$ modulator, fabricated in 0.13 μm standard CMOS technology, did not generate the expected output. Due to the inability to monitor the behaviour of the internal nodes, it was challenging to troubleshoot the design. Accordingly, the prototype presented here, summarized in Fig. 7.5 and Table 7.3 and implemented in 0.13 μm standard CMOS technology, was composed of two systems as follows

1. The 3rd-order $\Delta\Sigma$ modulator described so far in this thesis was implemented with the outputs of the log-domain components connected to bonding pads (TP1 - TP10) to allow observation of the internal nodes during testing.

2. In order to ease troubleshooting of the design, sections of the $\Delta\Sigma$ modulator were isolated, to allow testing of select groupings of the components. Fabrication area limitations constricted the number of components that could be separated, due to the necessity of additional bonding pads with each additional level of separation. The

[3] The Figure-of-Merit is defined as $Power/(2^{ENOB} \times 2\, f_{BW})$ where ENOB is the Effective-Number-of-Bits.

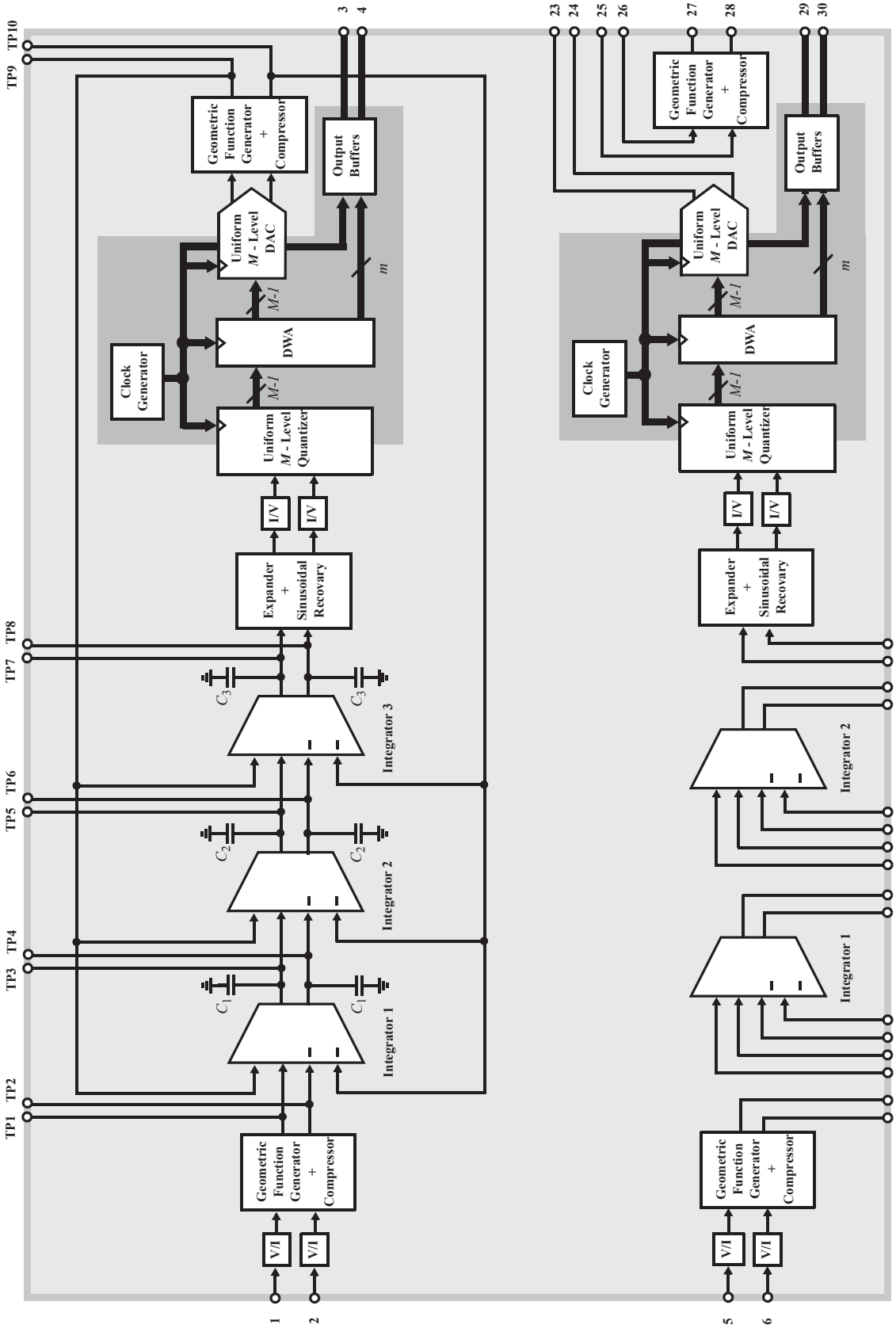


Figure 7.5: Summary of fabricated prototype and input/output and test nodes (supply-voltage, shielding, and reference-voltage nodes, not shown). Input/output and test nodes are listed in Table 7.3.

Table 7.3: Input/output and test nodes of the fabricated prototype in Fig. 7.5.

Bonding pad	Description
3rd-order 3-bit log-domain $\Delta\Sigma$ modulator	
1, 2	Modulator differential input
3	Modulator CLK output
4	Modulator 3-bit digital output
TP1, TP2	Test points: Input-compressor differential output
TP3, TP4	Test points: Integrator 1 differential output
TP5, TP6	Test points: Integrator 2 differential output
TP7, TP8	Test points: Integrator 3 differential output
TP9, TP10	Test points: Feedback-compressor differential output
Segmented Blocks	
5, 6	V/I differential input
7, 8	Compressor differential output
9, 10, 11, 12	Integrator 1 differential input and feedback input
13, 14	Integrator 1 differential output
15, 16, 17, 18	Integrator 2 differential input and feedback input
19, 20	Integrator 2 differential output
21, 22	Expander differential input
23, 24	DAC differential output
25, 26	Compressor differential input
27, 28	Compressor differential output
29	CLK output
30	3-bit digital output

sizing of the devices of all the separated components conforms to those of the 3rd-order log-domain $\Delta\Sigma$ modulator.

The following sections outline details of the prototype layout.

7.3.1 Transistors Layout

Matching of transistors is critical to the low-distortion performance of the $\Delta\Sigma$ modulator. To that effect, layout techniques that reduce the effect of process variations and boundary conditions [Joh97] are employed.

Matching of the compressing and expanding transistors of the $\Delta\Sigma$ modulator is particularly critical due to

1. Variation in the relative sizing of the differential compression transistors M_3 and M_5

in Fig. 5.4 results in variation of the differential compression factors.

2. Variation in the relative sizing of the aforementioned compressing transistors and expanding transistors results in a variation of the I_{Comp}/I_{Exp} factor in the loop-filter transfer function described in (4.56) - (4.59) [4].

Accordingly, the four compressing and two expanding transistors are setup in a common-centroid configuration to reduce the gradient effects. Additionally, dummy devices are included at the edges to mitigate the effects of boundary conditions. Figure 7.6 demonstrates a segment of the layout of the compressing and expanding transistors, achieving a common-centroid configuration. The layout is repeated vertically and horizontally to realize the full transistors' width. Additionally, to prevent latch-up, connections to the substrate are incorporated between the six interdigitated transistor rows in Fig. 7.6.

Another set of transistors that require precision matching are the eight transistors at the class AB integrator's input, shown in Fig. 5.2. The transistors M_1-M_2, M_7-M_8, M_9-M_{10}, and M_{15}-M_{16} generate the various components of the currents in (4.14) and (4.15). To achieve a common-centroid configuration, the layout in Fig. 7.7 is employed, with the demonstrated section repeated horizontally and vertically to realize the full width of the transistors. Similar to the layout of the compressing and expanding transistors, dummy devices at the edges of the rows, and substrate connections between the eight rows, are incorporated.

The same common-centroid, dummy-device placement, and substrate connection techniques were employed to realize the DAC unit-element current sources I_{Unit} in Fig. 6.2. Additionally, throughout, the techniques were employed to realize the transistor pairs in the current-mirrors, cascode-pairs, CMFB inputs, and amplifier inputs.

[4] The effect of varying W/L results in a variation of the bias current of the associated transistor, according to (3.4).

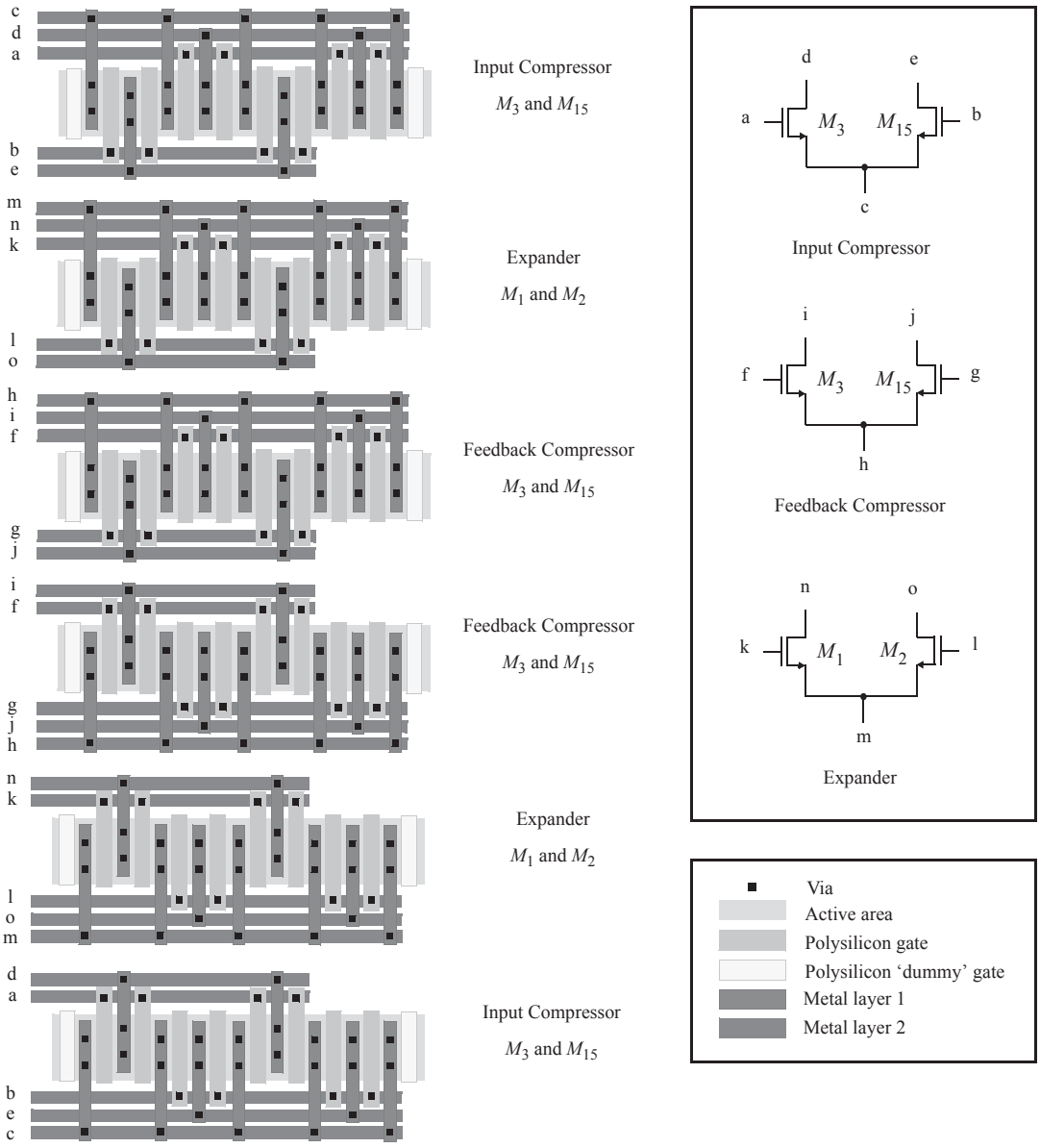


Figure 7.6: Segment of common-centroid layout of the compressing and expanding transistors in Fig. 5.4 and Fig. 5.5 (not to scale).

7.3.2 Capacitors and Resistors Layout

To implement capacitances C_1, C_2, and C_3 in Table 5.8, capacitors with large capacitance-to-area density are required. Large capacitance density is available in metal-insulator-metal (MIM) capacitors. Dual metal-insulator-metal (dual MIM) capacitors double the achievable capacitance by adding an additional dielectric and electrode layer. The latter requires

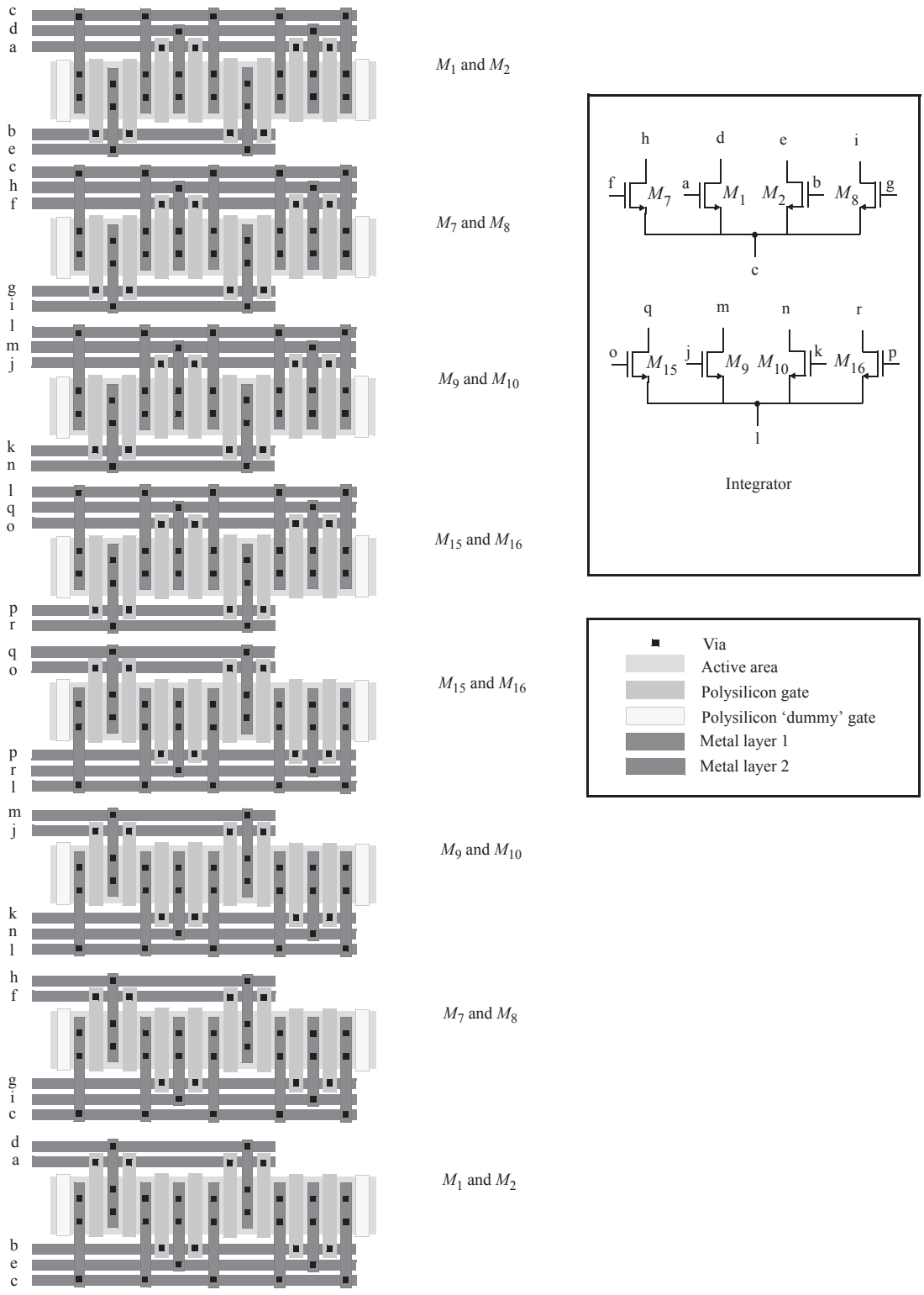


Figure 7.7: Segment of common-centroid layout of the integrator's differential input and feedback transistors in Fig. 5.2 (not to scale).

an optional mask, which was available during fabrication. Accordingly, the integrators' capacitances were implemented as dual MIM capacitors.

Each of the two capacitors at the differential outputs of each integrator (Fig. 7.1) require precision matching. Accordingly, each capacitor pair was implemented in a common-centroid configuration.

The V/I and I/V conversion resistors R_{VI} and R_{IV} are implemented through the use of polysilicon resistors with high sheet-resistance. Interdigitation of the differential resistor pairs ensures adequate matching of the devices.

7.3.3 Bonding Pads and Shielding

To minimize the coupling of noise across the fabricated prototype, the prototype was divided into four sections

1. **Analog:** This section contains the V/I and I/V converters, compressors, expanders, integrators, quantizer's preamplifiers, and DAC.

2. **Digital:** This section contains the quantizer's latches and DWA circuit.

3. **Clock:** This section contains the clock generator.

4. **Output buffers:** This section contains the digital output buffers.

Sectioning is performed to reduce the coupling of noise between the various components during transitions within the digital, clock, and output buffer stages. The digital, clock, and particularly the output buffer stages can introduce significant glitches as the digital signals transitions from one state to the next.

For each of the four sections, the following techniques were employed

1. Each section was designated unique supply-voltage V_{DD} and supply-ground V_{SS} bonding pads. Additionally, each section was designated unique $V_{DD,Shield}$ and $V_{SS,Shield}$ bonding pads to provide the bias for the substrate and n-well connections.

2. Each of the four sections was encased by guard rings consisting of both substrate and well connections. The biasing of each sections' substrate and n-well connections is provided by the dedicated $V_{DD,Shield}$ and $V_{SS,Shield}$ bonding pads associated with the particular section.

3. N-well connections, biased by the associated $V_{DD,Shield}$, are placed below lengthy interconnects to shield the connections from substrate noise.

7.3.4 Summary

The prototype was fabricated in 0.13 μm standard CMOS technology. The chip micrograph is shown in Fig. 7.8, with the 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator highlighted, and the additional segmented components included. The 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator consumes an active area of 1.63 mm^2.

7.4 Experimental Results

7.4.1 3rd-Order 3-Bit Log-Domain $\Delta\Sigma$ Modulator

The test-setup of the 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator is shown in Fig. 7.9. Table 7.4 summarizes the parameters setting the bias voltage at the input and output of the log-domain components. Observing Fig. 5.2, Fig. 5.4, and Fig. 5.5, the values in Table 7.4 are expected to generate approximately equivalent bias at the output of their respective log-domain component. A signal with a differential amplitude of 0.6 V and frequency f_{in} = 9.12 kHz was applied at the input[5].

Testing of the modulator did not result in the expected signal swing at the output (node 4 in Fig. 7.9). To determine the cause of the signal absence, the bias at the internal nodes (TP1 - TP10) within the modulator was measured, as summarized in Table 7.5.

[5] The input signal can not be reduced beyond f_{in} = 9 kHz due to the minimum frequency of the signal generator.

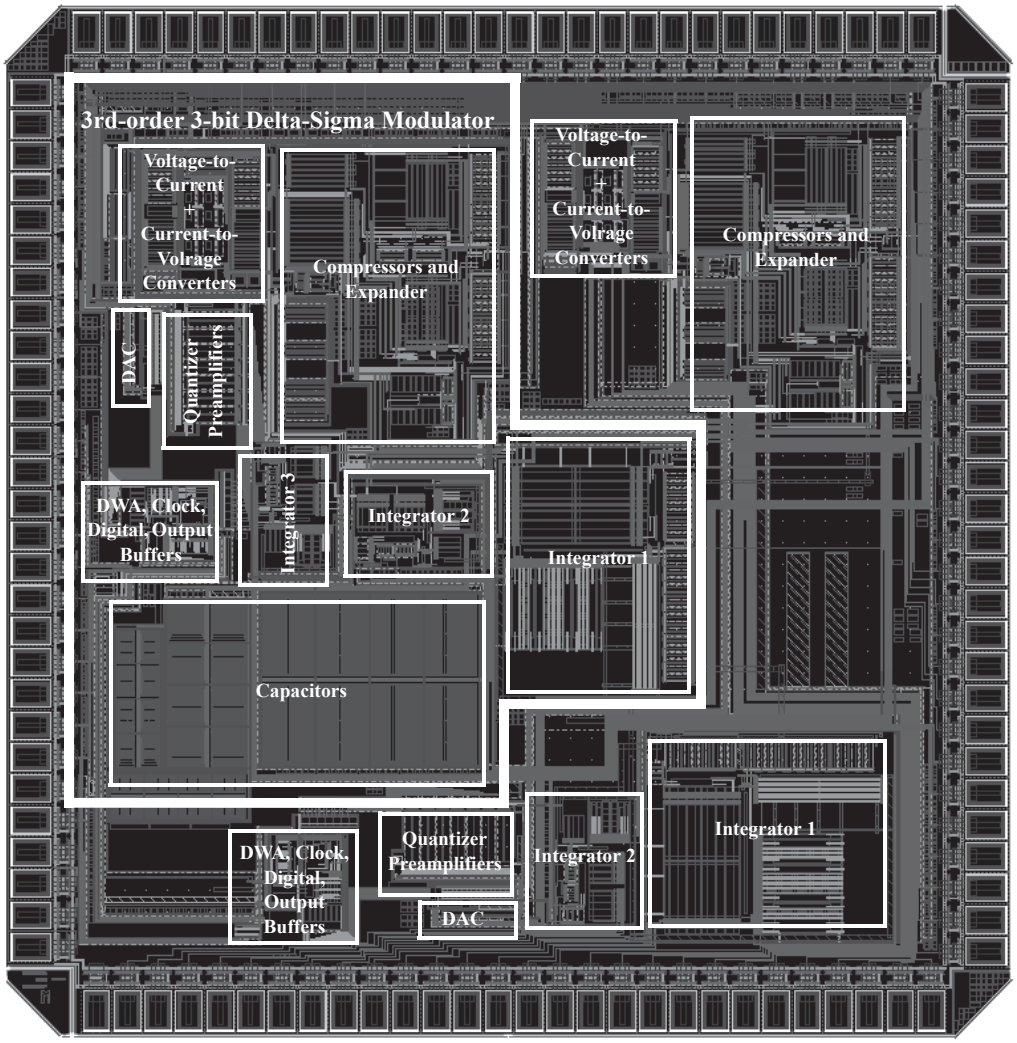


Figure 7.8: Chip micrograph of the fabricated prototype, indicating the various components of the fabricated prototype. The dimensions of the chip are 2.2 mm $\times$ 2.2 mm.

The results at the output of the compressors (TP1 - TP2, TP9 - TP10) demonstrate that the dc behaviour of the compressors is as expected. However, the discrepancy of the integrator outputs (TP3 - TP8) from the expected 0.3 V bias, and the mismatch between the bias of each integrator's differential nodes, indicates that loop-filter instability within the modulator results in the loss of the signal at the output.

In the following section, the separated sections highlighted in Fig. 7.5 are configured to test the behaviour of individual components, and investigate the cause of the observed loop-filter instability.

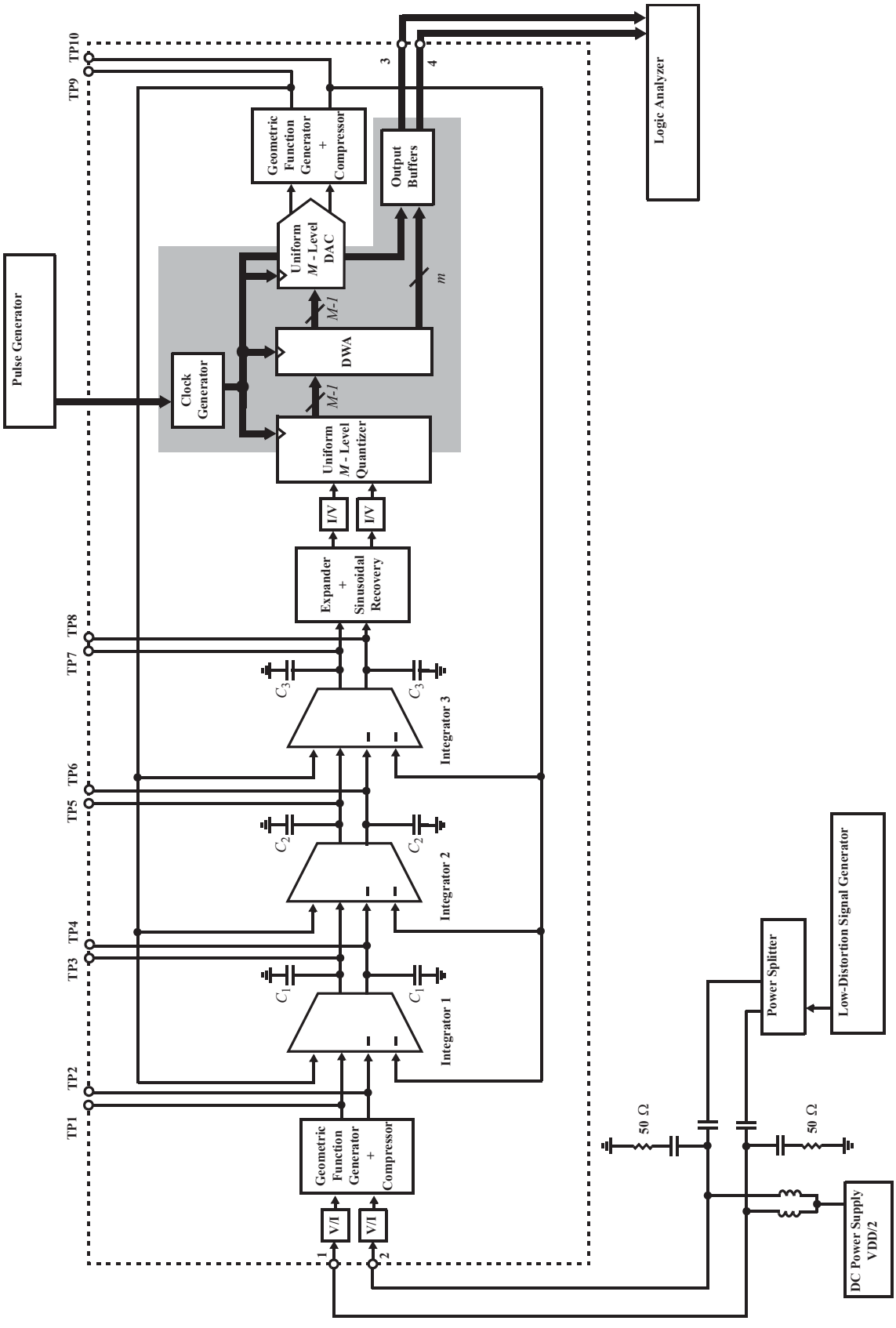


Figure 7.9: Test setup for the 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator. Elements in dashed boxes are implemented on chip (supply-voltage, shielding, and reference-voltage nodes, not shown).

Table 7.4: Parameters setting the bias voltage at the input and output of the log-domain components.

Parameter	Value
Geometric-mean generator and log-domain compressor (Fig. 5.4)	
V_{BIASa}	300 mV
Expander and sinusoidal regenerator. (Fig. 5.5)	
V_{BIASa}	300 mV
Integrator (Fig. 5.2)	
V_{CMFB}	300 mV

Table 7.5: Voltage bias of the test points in Fig. 7.9 for V_{BIASa} = V_{CMFB} = 0.3 V in Fig. 5.2, Fig. 5.4, and Fig. 5.5.

Bonding pad	Voltage Bias (mV)
TP1, TP2	298, 298
TP3, TP4	310, 315
TP5, TP6	362, 396
TP7, TP8	414, 445
TP9, TP10	297, 297

7.4.2 Compressor, Expander, V/I-I/V Conversion, Quantizer, DWA, and Output Buffers

To verify the functionality of the compressor, expander, V/I-I/V conversion, quantizer, DWA, and output buffers, the separated segments of the fabricated prototype in Fig. 7.5 have been employed in the test setup shown in Fig. 7.10. The bias parameters are as listed in Table 7.4.

Table 7.6 summarizes the resulting bias at the outputs of the various nodes. The results indicate that the voltage bias at the outputs of the compressors (nodes 7 and 8, and nodes 27 and 28) approximately conform to the expected bias. Furthermore, the voltage bias at the inputs of the second compressor (nodes 25 and 26) approximately conform to the expected bias, described by (5.20) in Chapter 5.

Due to the inability to observe the analog swing at the output of the I/V converter in Fig.

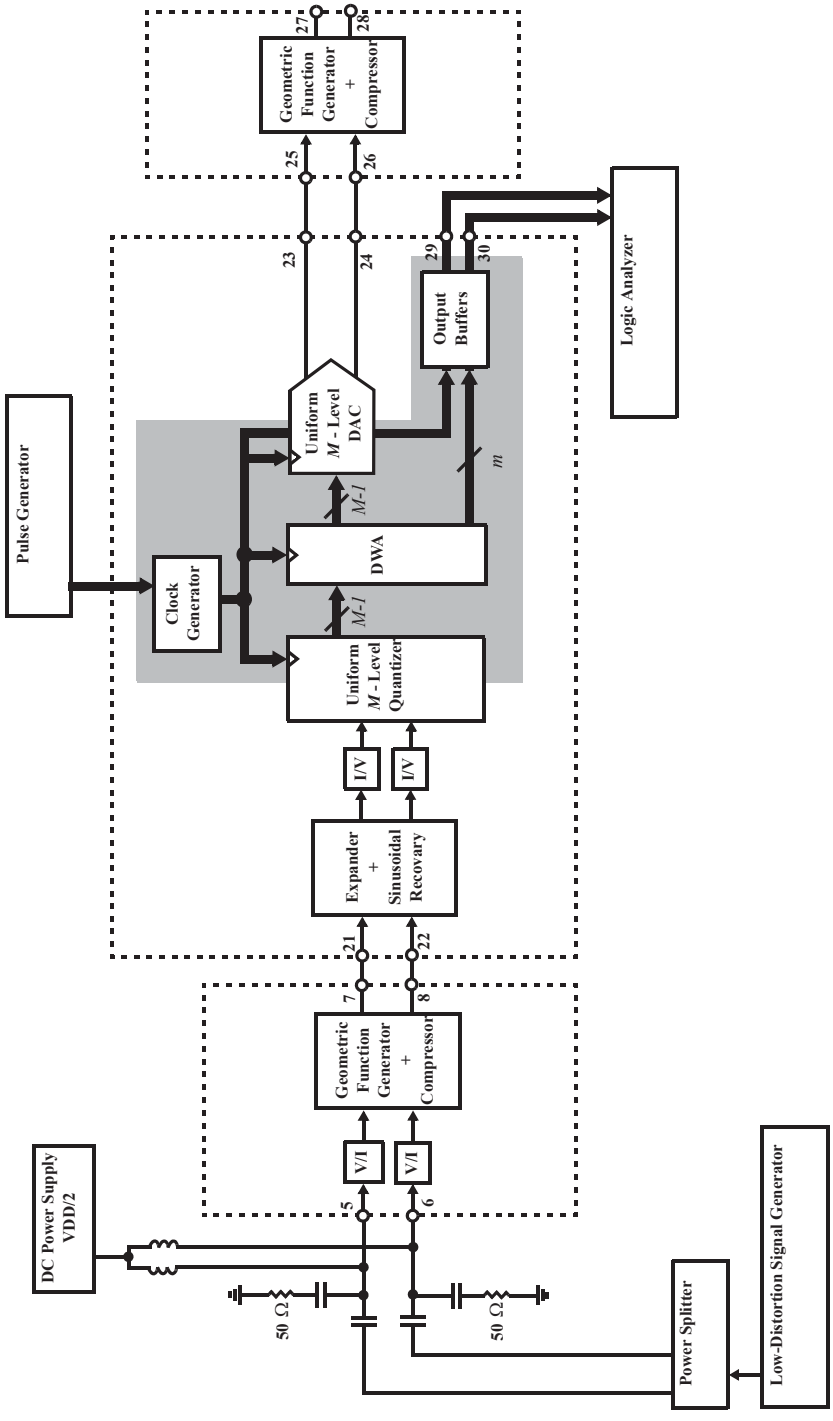


Figure 7.10: Test setup for the compressor, expander, V/I-I/V conversion, quantizer, DWA, and output buffers (supply-voltage, shielding, and reference-voltage nodes, not shown). Elements in dashed boxes are implemented on chip.

Table 7.6: Voltage bias of the points in Fig. 7.10 for V_{BIASa} = V_{CMFB} = 0.3 V in Fig. 5.2, Fig. 5.4, and Fig. 5.5.

Bonding pad	Voltage Bias (mV)
7, 21	297
8, 22	297
23, 25	608
24, 26	608
27	295
28	295

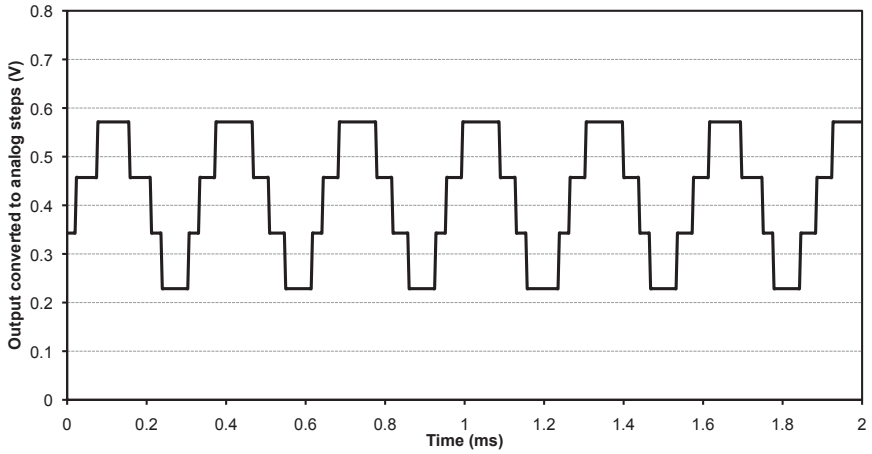


Figure 7.11: Post-processed output (node 30) for the test setup in Fig. 7.10, representing the binary output as a thermometer code normalized to full signal-swing of 0.8 V.

7.10 (resulting from the limited number of available bondpads on the fabricated prototype), the compression and expansion were validated by observing the quantized signal, generated at node 30 in Fig. 7.10. Figure 7.11 demonstrates the post-processed output of the test setup in Fig. 7.10, measured for a differential input amplitude of 0.65 V and an input frequency of 13.98 kHz. The waveform in Fig. 7.11 was generated by converting the 3-bit binary output of the fabricated prototype to a 7-level thermometer code, and normalizing to a full signal-swing of 0.8 V.

The approximate equivalence of the bias points to the expected value of 0.3 V, and the signal swing generated at the output, validate the functionality of the compressor, expander, V/I-I/V conversion, quantizer, DWA, and output buffers.

7.4.3 1st-order Log-Domain Low-Pass Filter

Operation of the integrator was validated by configuring the separated segments of the fabricated prototype in Fig. 7.5 to generate a 1st-order log-domain low-pass filter. The resulting test setup is shown in Fig. 7.12. The bias parameters are as listed in Table 7.4.

For an integrator bias current of I_{Int} = 728 nA and an integrating capacitor C = 150 pF in Fig. 7.12, the expected low-pass cutoff frequency is expected to be f_{cutoff} = 44.2 kHz [6].

Table 7.7 summarizes the resulting bias of the various nodes in Fig. 7.12. The voltage bias at the outputs of the compressors, expander, and I/V conversion stages conform with those expected. Additionally, the bias output of the integrator is set correctly by the V_{CMFB} voltage in Table 7.4.

Validation of low-pass filter operation was confirmed by applying a differential input signal of amplitude 0.65 V at two differing input frequencies, 13.98 kHz, and 100 kHz. Figure 7.13(a) and Fig. 7.13(b) demonstrate the post-processed output measured at node 30 in Fig. 7.12. Attenuation of the signal beyond the targeted cutoff frequency confirms the expected low-pass filter operation, and by extension the integrator's operation.

Table 7.7: Voltage bias of the points in Fig. 7.12 for V_{BIASa} = V_{CMFB} = 0.3 V in Fig. 5.2, Fig. 5.4, and Fig. 5.5.

Bonding pad	Voltage Bias (mV)
7, 10	297
8, 11	297
13, 21	300
14, 22	300
23, 25	608
24, 26	608
27	295
28	295

[6] The cutoff frequency of the 1st-order log-domain low-pass filter in Fig. 7.12 is derived using a similar method to the derivations presented in Section 4.2.2 and Appendix A, and is described by $f_{cutoff} = 2\,I_{Int}/(C\,\eta\,U_T)$.

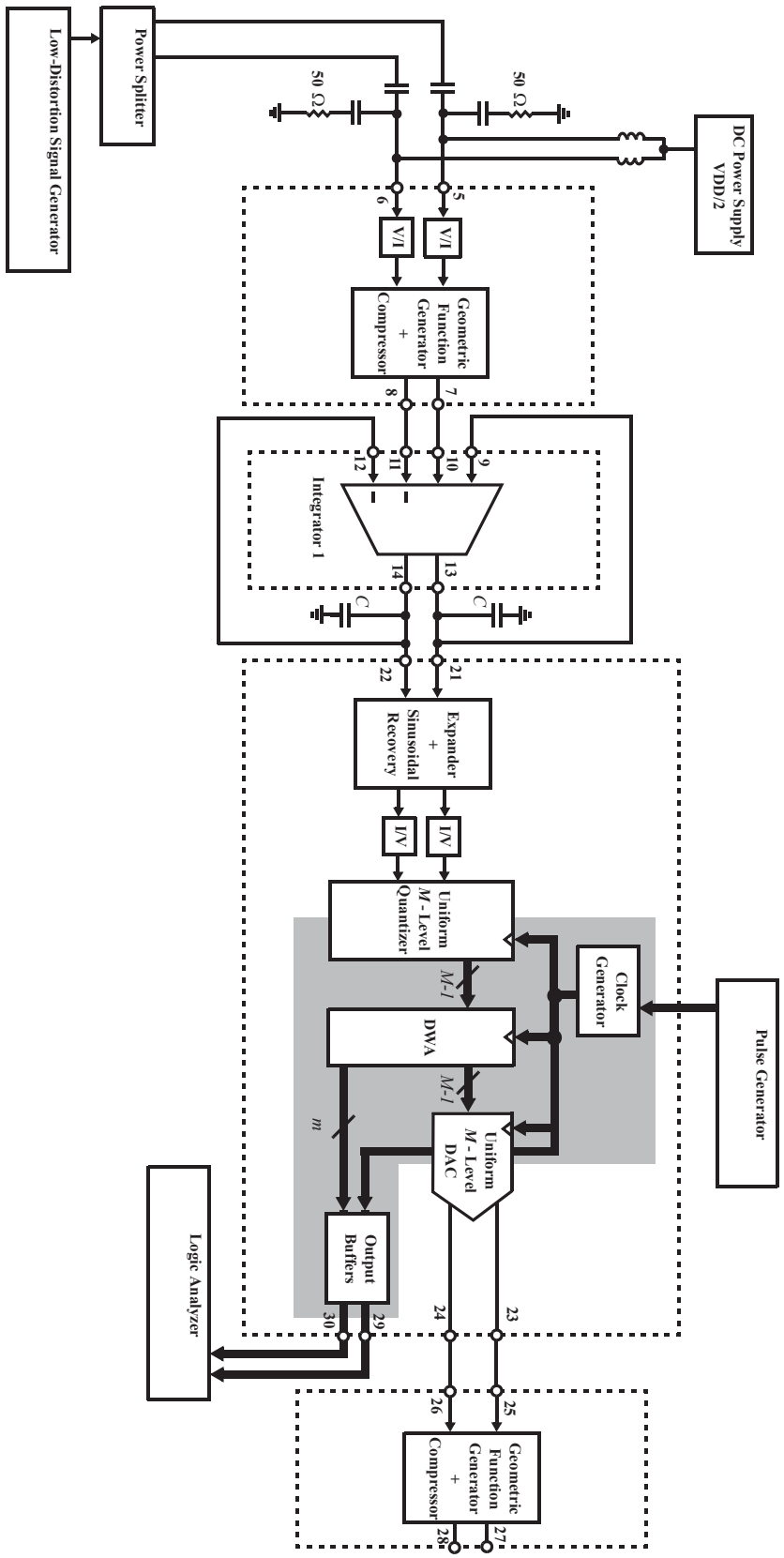
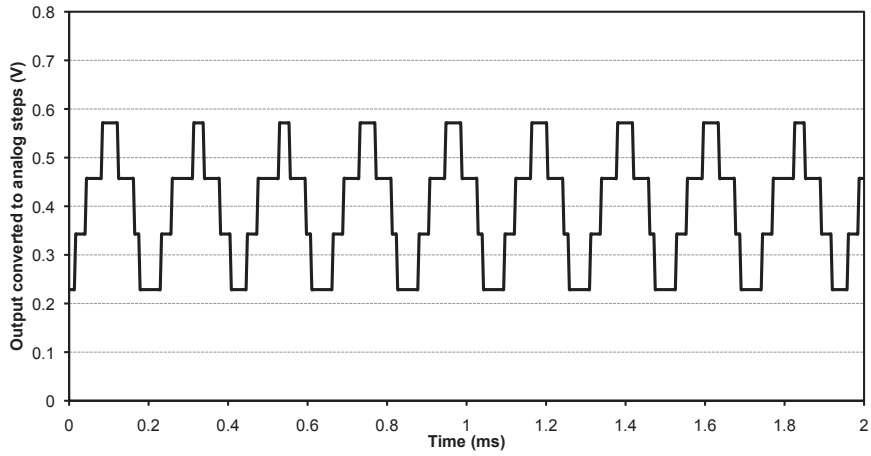
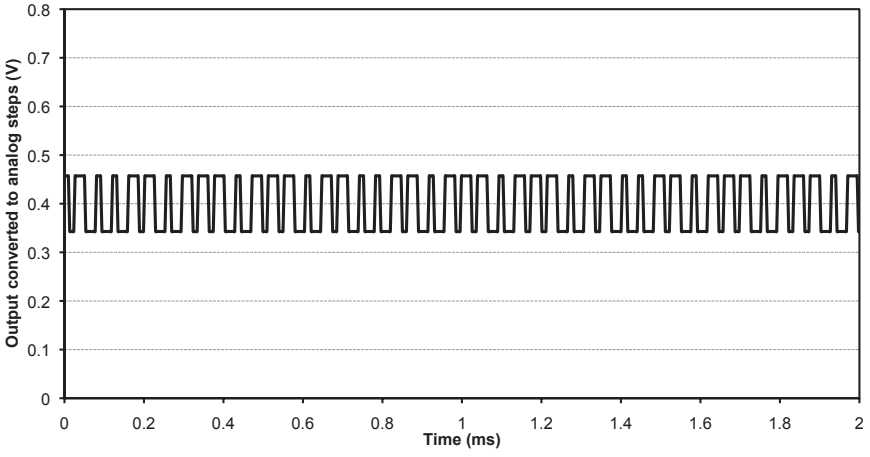


Figure 7.12: Test setup for a 1st-order log-domain low-pass filter (supply-voltage, shielding, and reference-voltage nodes, not shown). Elements in dashed boxes are implemented on chip.



(a)



(b)

Figure 7.13: Post-processed output (node 30) for the test setup in Fig. 7.12, representing the binary output as a thermometer code normalized to full signal-swing of 0.8 V. a) Input-signal frequency f_{in} = 13.98 kHz. b) Input-signal frequency f_{in} = 100 kHz.

7.4.4 1st-order 3-bit Log-Domain $\Delta\Sigma$ Modulator

Following the validation of the functionality of all the fabricated individual components, presented in Section 7.4.2 and Section 7.4.3, a 1st-order log-domain $\Delta\Sigma$ modulator test-setup is constructed, as shown in Fig. 7.14. Compared to the 3rd-order $\Delta\Sigma$ modulator (Section 7.4.1), the 1st-order modulator presented in Fig. 7.14 is less susceptible to loop-filter instability, easing the identification of the source of instability in the former. The

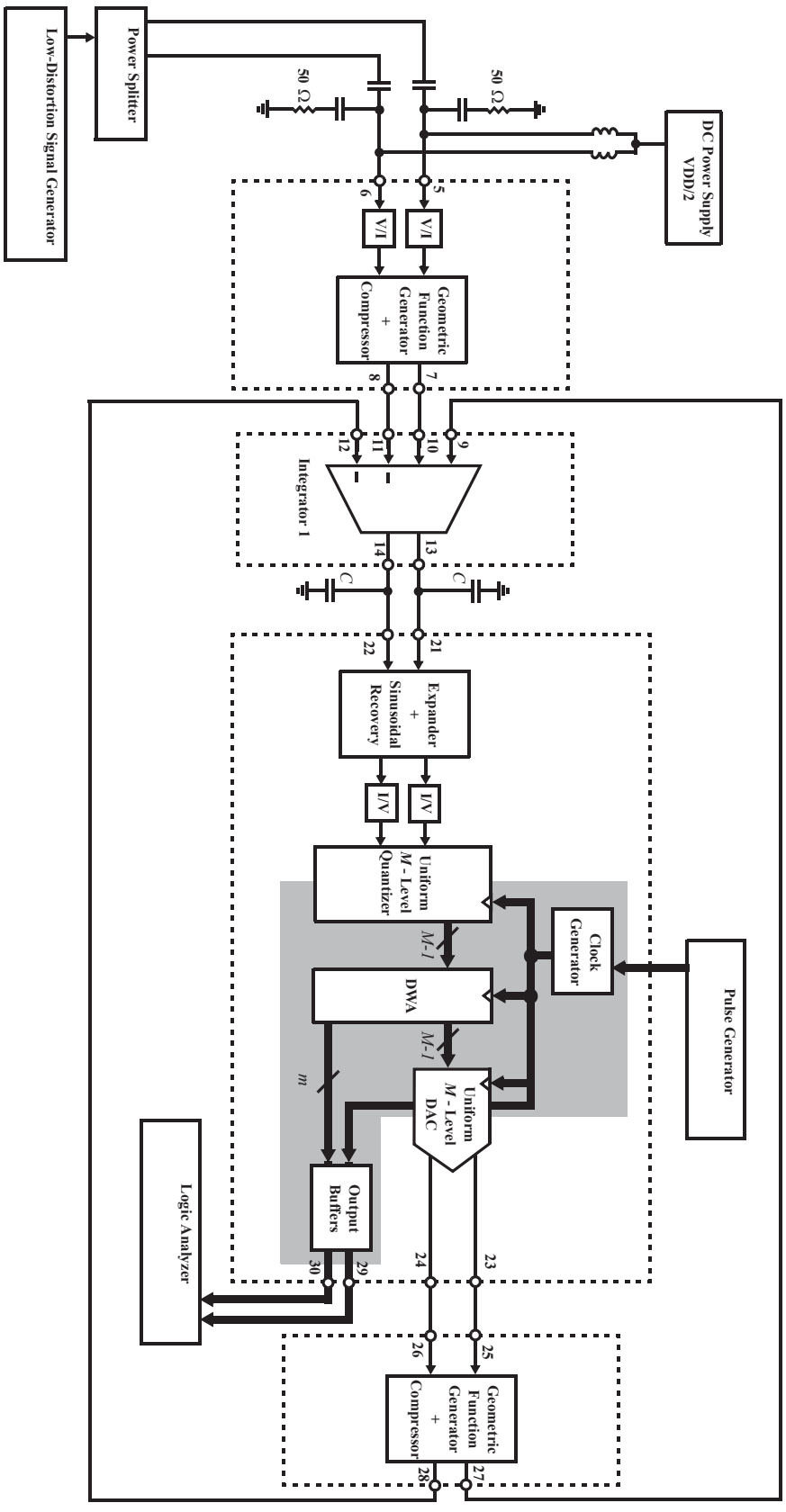


Figure 7.14: Test setup for a 1st-order 3-bit log-domain $\Delta\Sigma$ modulator (supply-voltage, shielding, and reference-voltage nodes, not shown). Elements in dashed boxes are implemented on chip.

Table 7.8: Parameters for the 1st-order 3-bit log-domain $\Delta\Sigma$ modulator test setup in Fig. 7.14.

Parameter	Value
Input signal	
f_{in}	9.12 kHz
Differential amplitude	0.6 V
Integrator	
I_{Int}	840 nA
C	150 pF
Quantizer and DAC	
f_s	320 kHz
OSR	16

selection of parameters for the 1st-order 3-bit log-domain $\Delta\Sigma$ modulator is summarized in Table 7.14 [7].

Table 7.9 demonstrates that the voltage bias at the output of the log-domain stages of the 1st-order 3-bit $\Delta\Sigma$ modulator conform with the expected bias. Accordingly, the modulator is stable and a signal swing is generated at each of the stages and at the modulator output. Table 7.10 summarizes the amplitude of the signals at the outputs of the compressors and integrator. Observing Table 7.9, a significant differential mismatch occurs at the output of each of the stages. Figure 7.15 shows the output spectrum of the modulator. The differential mismatch results in significant distortion and the introduction of even-ordered harmonics, resulting in a THD of -19.5 dB. The distortion results in a folding of the out-of-band noise into the signal bandwidth, significantly deteriorating the SNR within the signal bandwidth (SNR = 22.1 dB).

[7] The input signal can not be reduced beyond f_{in} = 9 kHz due to the minimum frequency of the signal generator.

Table 7.9: Voltage bias of the points in Fig. 7.14 for V_{BIASa} = V_{CMFB} = 0.3 V in Fig. 5.2, Fig. 5.4, and Fig. 5.5.

Bonding pad	Voltage Bias (mV)
7, 10	297
8, 11	297
13, 21	300
14, 22	300
23, 25	608
24, 26	608
27, 9	295
28, 12	295

Table 7.10: Voltage swing at the differential outputs of log-domain components in Fig. 7.14.

Component	Voltage swing P	Voltage swing N
Compressor 1	15.7 mV (bondpad 7, 10)	12.8 mV (bondpad 8, 11)
Integrator	21.4 mV (bondpad 13, 21)	18.1 mV (bondpad 14, 22)
Compressor 2	15.9 mV (bondpad 27, 9)	13.1 mV (bondpad 28, 12)

7.4.5 Discussion

The results in Section 7.4.2 and Section 7.4.3 demonstrate the functionality of the log-domain components presented in Chapter 5 at an aggressively low supply voltage of 0.8 V. Furthermore, the amplitude of the signal swing at the outputs of the feedback compressor approximately conform with those expected from circuit-level simulations, validating the functionality of the proposed current-output DAC presented in Chapter 6.

Observing the differential mismatch in Table 7.10 and the resulting tones in Fig. 7.15 for the 1st-order 3-bit log-domain $\Delta\Sigma$ modulator, it can be concluded that distortion and noise-folding result in the instability observed in the 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator presented in Section 7.4.1. It was demonstrated in Chapter 5, that a differential error in compression (Fig. 5.19) results in significant distortion, when compared to the attenuated distortion resulting from a differential error within the integrator or expander. Accordingly,

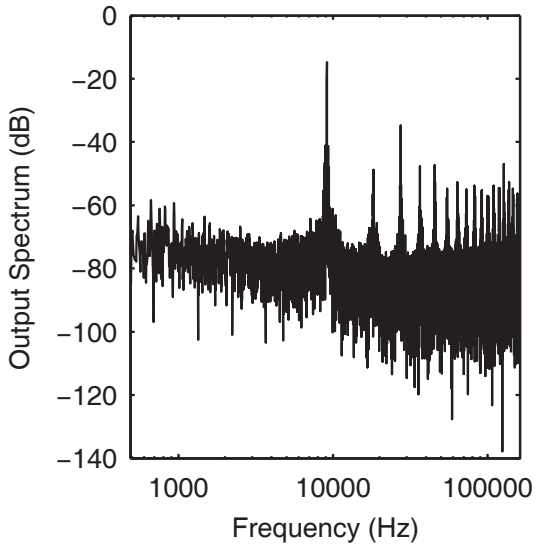


Figure 7.15: Output spectrum of the fabricated 1st-order 3-bit log-domain $\Delta\Sigma$ modulator in Fig. 7.14.

it can be deduced that the differential signal-swing mismatch at the outputs of the compressors observed in Table 7.10 is the main source of distortion and noise folding in log-domain $\Delta\Sigma$ modulators.

In Chapter 5, low-distortion circuit architectures were developed to reduce differential drain-to-source voltage mismatch across the compressing, integrating, and expanding transistors. However, threshold-voltage mismatch within the differential devices may still result in differential bias-current mismatch, and subsequently, differential-mismatch within the compressor and expander. In [Pel98], it is shown that the standard deviation of the threshold voltage-mismatch for minimum-sized devices at the 0.13 μm technology node is larger than that of minimum-sized devices at the 0.35 μm technology node by more than a factor of three.

The results suggest that for class AB log-domain architectures to be effectively employed in log-domain $\Delta\Sigma$ modulators, the modulator should be realized at less aggressive technology nodes, where the matching of devices is significantly improved. It is worth noting that at less aggressive technology nodes, low-power ADCs targeting biomedical appli-

cations benefit from reduced leakage due to increased V_T. Alternatively, it is suspected that if the presented multibit log-domain $\Delta\Sigma$ modulator architecture and circuits are employed in class A log-domain $\Delta\Sigma$ modulators, the absence of errors introduced by differential mismatch, and the subsequent relaxation of device-matching requirements, would allow log-domain $\Delta\Sigma$ modulators to be employed at aggressive technology nodes.

7.5 Performance Comparison

A comparison of the simulated performance of the implemented modulator with state-of-the-art $\Delta\Sigma$ ADCs targeting high-resolution biomedical applications ($>$ 10 bits) and the single-bit log-domain $\Delta\Sigma$ modulator [Red07] is summarized in Table 7.11 [8]. Here, the effective-number-of-bits (ENOB) is evaluated using (7.3) and the modulator's figure-of-merit (FOM) is defined as

$$\text{FOM} = \frac{P}{2^{ENOB} \times 2\, f_{BW}} \tag{7.4}$$

The proposed modulator achieves high-resolution analog-to-digital conversion at very low supply voltages. Additionally, it achieves the largest reported maximum-signal-swing to supply-voltage ratio (1.05) when compared to the state-of-the-art $\Delta\Sigma$ modulators targeting high-resolution applications in Table 7.11. The low internal signal-swing nature of log-domain $\Delta\Sigma$ modulators enables the reported high-signal swing.

Comparing the FOM of the multibit $\Delta\Sigma$ modulator (simulated) proposed here (FOM = 1.64) to the single-bit implementation in [Red07] (FOM = 9.77), it is apparent that the techniques introduced in this thesis significantly increase the efficiency of log-domain $\Delta\Sigma$ modulators. Specifically

- The modulator presented here while employing a 3$^{\text{rd}}$-order loop-filter achieves a

[8] For the $\Delta\Sigma$ modulator in [Lóp08], the performance in Table 7.11 is calculated using both the noise and distortion of the modulators, to ensure a fair comparison of all the modulators in Table 7.11.

Table 7.11: Comparison with state-of-the-art $\Delta\Sigma$ modulator implementations for high resolution medical applications ($>$ 10 bits) and previous log-domain $\Delta\Sigma$ modulator implementations.

Reference	Bandwidth (kHz)	Power (μW)	ENOB	FOM (pJ/step)	Supply (V)	Max. Sig. Swing (V)	Max. Sig. Swing / Supply	Tech.
[Neu97]	7	236.5	12.5	0.291	2.15	0.04	0.02	0.8 μm
[Klo00]	10	72	12.99	0.49	0.9	0.23	0.26	0.35 μm
[Gat02]	10	72.6	14.99	0.12	1.1	-	-	0.6 μm
[Kim06]	8	36.7	13.99	0.14	0.9	-	-	0.25 μm
[Lóp08]	0.025	0.14	10.13	2.5	1.2	0.724	0.6	0.5 μm
[Cha09]	20	36	13.16	0.098	0.7	-	-	0.18 μm
[Xu10]	1	20	14.62	0.396	1.5	-	-	0.35 μm
[Can11]	0.256	13.3	11.67	7.98	1.4	1.4	1	0.18 μm
[Red07] (single-bit, log-domain)	8	160	10	9.77	1.2	-	-	0.35 μm
Simulated								
This work [Sha14b]	10	46.7	10.47	1.64	0.8	0.84	1.05	0.13 μm

higher ENOB than the modulator in [Red07] employing a fourth-order loop filter. This is a result of multibit quantization. It is noted that the stability of a $\Delta\Sigma$ modulator worsens with increasing loop-filter order, and that multibit quantization improves the stability of $\Delta\Sigma$ modulators.

- The multibit $\Delta\Sigma$ modulator presented here employs a lower oversampling ratio (OSR = 16) and sampling frequency (f_s = 320 kHz) when compared to the single-bit implementation in [Red07] (OSR = 64, f_s = 1 MHz), while achieving a larger bandwidth. This, in turn, relaxes the requirements of the digital circuits following the modulator.

- The low-distortion circuit techniques presented, and the optimization procedure employed to improve linearity and noise performance, result in a competitive ENOB while lowering power consumption.

Accordingly, the techniques proposed in this thesis demonstrate the potential of log-domain circuit-techniques to compete with state-of-the-art $\Delta\Sigma$ modulators.

CHAPTER 8

Concluding Remarks

THIS CHAPTER presents a summary of the thesis and the research contributions in Section 8.1. Suggestions for future research are proposed in Section 8.2.

8.1 Thesis Summary and Contributions

Recognizing the low-power low-voltage potential of log-domain circuit techniques, this thesis sought out to investigate the application of log-domain circuits in $\Delta\Sigma$ modulators with resolutions exceeding 10 bits. In doing so, two potential challenges were identified:

1. No architecture suitable for multibit log-domain $\Delta\Sigma$ modulators had been proposed to date, significantly hindering the achievable resolution of log-domain $\Delta\Sigma$ modulators.

2. High-resolution $\Delta\Sigma$ modulators require low-distortion analog components, as well

as the development of a design procedure for the optimization of the linearity and noise of log-domain circuits.

The primary contributions of this thesis are summarized below:

1. **Architecture-Level Design of a Multibit Log-Domain $\Delta\Sigma$ Modulator:** The challenges of multibit quantization in log-domain $\Delta\Sigma$ modulators were investigated and a novel multibit log-domain $\Delta\Sigma$ modulator architecture was proposed. The equivalence of the proposed class AB modulator to classical $\Delta\Sigma$ modulator realizations, and the selection of coefficients, were demonstrated through derivations of the loop-filter transfer function. A behavioural model of the multibit log-domain $\Delta\Sigma$ modulator, including critical non-idealities, was developed. The behavioural performance of a 3rd-order 3-bit log-domain $\Delta\Sigma$ modulator, in addition to the effect of several non-idealities, including variation of the transistors' level of channel-inversion, and compression-expansion mismatch, was demonstrated.

2. **Development of Low-Distortion Log-Domain Circuits and Demonstrating their Necessity in High-Resolution Applications:** This work introduced modifications to previously proposed log-domain analog blocks, enabling the realization of high-resolution log-domain $\Delta\Sigma$ modulators. Additionally, a novel low-distortion class AB expander that generates differential outputs while sharing current-mode paths to achieve power-savings is proposed. The power consumption and voltage headroom penalty of the low-distortion circuits was demonstrated. Circuit-level simulations confirm the necessity of the presented low-distortion circuits through comparisons with previously proposed circuit implementations.

3. **Analysis of Log-Domain Design Trends and Proposal of a Design Optimization Procedure for Log-Domain $\Delta\Sigma$ modulators:** This work presented an analysis of the distortion resulting from variations in weak-inversion operation in class AB log-domain circuits. Additionally, the design trends and tradeoffs involved in the design

of log-domain circuits, and the multiple noise and distortion implications associated with each of the design parameters, was derived. A design-optimization procedure that facilitates the realization of a targeted linearity and noise performance while minimizing power consumption is derived and employed in the circuit-level realization of a 3rd-order 3-bit Class AB log-domain loop-filter. Circuit-level simulations demonstrate the performance of the proposed modulator and confirm the derived design trends. The derived design tradeoffs and proposed optimization procedure can be extended to alternative log-domain applications.

4. **Low-Noise Current Output DAC:** A novel low-power low-noise current-output DAC suitable for multibit log-domain $\Delta\Sigma$ modulators is presented. Selection of the design parameters to meet the $\Delta\Sigma$ modulator architecture requirements was demonstrated, enabling full signal swings while eliminating the use of a voltage-to-current conversion stage and its associated noise in the feedback path.

5. **Implementation of a Fabricated Prototype:** Circuit-level simulations of the proposed modulator indicate 10.47-bit SNDR operation for a 10 kHz signal bandwidth and 0.84 V_{pp} input signal swing, while consuming a total power (analog and digital) of 46.7 μW. The log-domain $\Delta\Sigma$ modulator and additional segments of the modulator were fabricated in 0.13 μm CMOS technology. The functionality of the presented circuits at the targeted low supply voltage was demonstrated by testing various architectures in the fabricated prototype. It was demonstrated that differential mismatch at the outputs of the log-domain compressors in the fabricated prototype is a significant challenge in class AB log-domain $\Delta\Sigma$ modulators.

Segments of the research contributions have been published in:

[1] M. A. Shaheen, Y. Savaria, and A. A. Hamoui. Design and modeling of high- resolution multibit log-domain $\Delta\Sigma$ modulators, in *Journal of Analog Integrated Circuits and Signal Processing*, vol. 79, no. 3, pp. 569-582, June 2014.

[2] M. A. Shaheen, A. A. Hamoui, and Y. Savaria. A current-output DAC for low-power low-noise log-domain $\Delta\Sigma$ modulators, in *Proc. IEEE NEWCAS Conference*, June 2014, pp. 281-284.

8.2 Suggestions for Future Research

In the presented work, several potential factors affecting the performance of the presented log-domain $\Delta\Sigma$ modulator were encountered. Investigation of these factors would provide a thorough understanding of the limitations of log-domain $\Delta\Sigma$ modulators when compared to alternative $\Delta\Sigma$ modulator architectures.

1. It was demonstrated in the experimental results presented in Section 7.4 that device mismatch significantly deteriorates the performance of the proposed class AB architecture. The resulting distortion and folding of out-of-band noise into the signal bandwidth, hindered the evaluation of the performance of the fabricated log-domain $\Delta\Sigma$ modulators. It was noted that differential device mismatch can be reduced by fabricating the design using a less aggressive technology node, or can be eliminated by redesigning the log-domain modulator as a Class A system. Investigation of these two venues is required in order to effectively evaluate the potential of multibit log-domain $\Delta\Sigma$ modulators for high-resolution low-power applications.

2. To reduce flicker noise in the proposed modulator, the length of the compressing, expanding, and integrator-input transistors is significantly large (4.8 μm). In simulation, no problems were encountered due to the large length of the devices. However, despite the potential for further reductions in noise (and improved FOM), the transistors' dimensions were not increased beyond the length at which the IBM CMRF8SF Model Guide guarantees accuracy of model extraction in 0.13 μm technology. To develop a full understanding of the limits of log-domain $\Delta\Sigma$ modulators when compared to alternative continuous-time implementations, the sizing limits of the tran-

sistors require investigation to determine the severity of modeling errors and any additional restrictions beyond the expected speed and fabrication-area penalty.

3. It is noted in Section 5.3.2 that for the log-domain $\Delta\Sigma$ modulator architecture proposed, based on the distributed-feedback architecture, the sampling frequency f_S primarily determines the magnitude of integrating capacitors. However, for a given bandwidth, an increase in OSR (to increase f_S) results in increasingly stringent design constraints on the digital circuits and the decimation filter. Investigation of alternatives to the distributed-feedback architecture or the incorporation of feedforward paths may result in alternative loop-filter transfer functions with larger I_{Int}/C ratios (and, in turn, smaller capacitances) for a given f_S.

4. Observing Table 5.9 and Table 7.2, the conversion amplifiers consume approximately 18 % of the overall $\Delta\Sigma$ modulator power. Investigation of alternative low-power low-voltage amplifier architectures can result in a reduction of the overall power, and improvement of the FOM.

5. It was demonstrated in this work that low-distortion class AB operation in log-domain circuits is limited by the degradation of the exponential relationship as the IC of the CMOS devices varies. Accordingly, the bias-currents of the compressors and expander had to be of sufficient magnitude to ensure limited IC variation at the maximum amplitude of the current signal. However, in biomedical applications, the amplitude of the input signal can decrease drastically during extended idle time or periods of low-amplitude biopotential signals. The reduction of bias currents at such times through the employment of dynamic biasing techniques [Kri01] can significantly reduce power dissipation.

Appendices

APPENDIX A

Loop Filter derivation of a Single-Ended 3rd-order Log-domain $\Delta\Sigma$ Modulator

ASSUMING a 3rd-order $\Delta\Sigma$ modulator with the first, second, and third integrator biased at currents I_{Int1}, I_{Int2}, and I_{Int3} respectively, and an expander and compressors biased at currents I_{Exp}, I_{Comp1}, I_{Comp2}, the following derivation of the NTF is obtained.

The signal current appearing at the output of the 1st integrator is given by

$$\begin{aligned} i_{C1} &= C_1 \frac{dv_{C1}}{dt} \\ &= I_{Int1}\,(-e^{\frac{v_{Comp2} - v_{C1}}{\eta\, U_T}}) \end{aligned} \tag{A.1}$$

Similarly, for the 2nd and 3rd integrator

$$\begin{aligned} i_{C2} &= C_2 \frac{dv_{C2}}{dt} \\ &= I_{Int2}\,(e^{\frac{v_{C1}-v_{C2}}{\eta\, U_T}} - e^{\frac{v_{Comp2}-v_{C2}}{\eta\, U_T}}) \end{aligned} \tag{A.2}$$

$$\begin{aligned} i_{C3} &= C_3 \frac{dv_{C3}}{dt} \\ &= I_{Int3}\,(e^{\frac{v_{C2}-v_{C3}}{\eta\, U_T}} - e^{\frac{v_{Comp2}-v_{C3}}{\eta\, U_T}}) \end{aligned} \tag{A.3}$$

Multiplying (A.3) through by $e^{\frac{v_{C3}}{\eta\, U_T}}$

$$C_3 \frac{dv_{C3}}{dt}\, e^{\frac{v_{C3}}{\eta\, U_T}} = I_{Int3}\,(e^{\frac{v_{C2}}{\eta\, U_T}} - e^{\frac{v_{Comp2}}{\eta\, U_T}}) \tag{A.4}$$

The signal at the input of the quantizer, v_{ye} is derived from the expanded signal i_{out} at the output of the third log-domain integrator. Assuming a I/V conversion resistor R_{IV} at the output of the expander, and utilizing the expander equation (3.7), then

$$v_{ye} = R_{IV}\, i_{out} = R_{IV}(I_{Exp}\, e^{\frac{v_{C3}}{\eta U_T}} - I_{Exp}) \tag{A.5}$$

Differentiating (A.5) and rearranging

$$e^{\frac{v_{C3}}{\eta\, U_T}} \frac{dv_{C3}}{dt} = \frac{dv_{ye}}{dt} \frac{\eta U_T}{R_{IV}\, I_{Exp}} \tag{A.6}$$

The signal at the output of the 2nd compressor is derived from the signal at the uniform-step DAC output, v_{DAC}. Assuming a V/I conversion resistor R_{VI} at the input of the 2nd com-

pressor, and utilizing the compressor equation (3.5), then

$$i_{Comp2,in} = \frac{v_{DAC}}{R_{VI}} \tag{A.7}$$

$$v_{Comp2} = \eta\, U_T\, ln\left(1 + \frac{i_{Comp2,in}}{I_{Comp2}}\right) \tag{A.8}$$

Inserting (A.7) into (A.8)

$$v_{Comp2} = \eta\, U_T\, ln\left(1 + \frac{v_{DAC}}{I_{Comp2}\, R_{VI}}\right) \tag{A.9}$$

Rearranging and applying the exponential function results in the following equation relating v_{Comp2} to v_{DAC}

$$e^{\frac{v_{Comp2}}{\eta\, U_T}} = 1 + \frac{v_{DAC}}{I_{Comp2}\, R_{VI}} \tag{A.10}$$

Inserting (A.6) and (A.10) into (A.4)

$$\begin{aligned} C_3\left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}}\right)\frac{dv_{ye}}{dt} &= I_{Int3}\, e^{\frac{v_{C2}}{\eta\, U_T}} \\ &\quad -I_{Int3}\left(1 + \frac{v_{DAC}}{I_{Comp2}\, R_{VI}}\right) \end{aligned} \tag{A.11}$$

Differentiating (A.11)

$$\begin{aligned} C_3\left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}}\right)\frac{dv_{ye}^2}{dt} &= \frac{I_{Int3}}{\eta\, U_T}\, e^{\frac{v_{C2}}{\eta\, U_T}}\, \frac{dv_{C2}}{dt} \\ &\quad -\frac{I_{Int3}}{I_{Comp2}\, R_{VI}}\frac{dv_{DAC}}{dt} \end{aligned} \tag{A.12}$$

Multiplying (A.2) through by $e^{\frac{v_{C2}}{\eta U_T}}$

$$C_2 \frac{dv_{C2}}{dt} e^{\frac{v_{C2}}{\eta U_T}} = I_{Int2} \left(e^{\frac{v_{C1}}{\eta U_T}} - e^{\frac{v_{Comp2}}{\eta U_T}} \right) \tag{A.13}$$

Inserting (A.13) into (A.12)

$$\begin{aligned} C_3 \left(\frac{\eta U_T}{I_{Exp} R_{IV}} \right) \frac{dv_{ye}^2}{dt} &= \frac{I_{Int3} I_{Int2}}{C_2 \eta U_T} \left(e^{\frac{v_{C1}}{\eta U_T}} - e^{\frac{v_{Comp2}}{\eta U_T}} \right) \\ &\quad - \frac{I_{Int3}}{I_{Comp2} R_{VI}} \frac{dv_{DAC}}{dt} \end{aligned} \tag{A.14}$$

Differentiating (A.14)

$$\begin{aligned} C_3 \left(\frac{\eta U_T}{I_{Exp} R_{IV}} \right) \frac{dv_{ye}^3}{dt} &= \frac{I_{Int3} I_{Int2}}{C_2 (\eta U_T)^2} e^{\frac{v_{C1}}{\eta U_T}} \frac{dv_{C1}}{dt} \\ &\quad - \frac{I_{Int3} I_{Int2}}{C_2 (\eta U_T)^2} e^{\frac{v_{Comp2}}{\eta U_T}} \frac{dv_{Comp2}}{dt} \\ &\quad - \frac{I_{Int3}}{I_{Comp2} R_{VI}} \frac{dv_{DAC}^2}{dt} \end{aligned} \tag{A.15}$$

Multiplying (A.1) through by $e^{\frac{v_{C1}}{\eta U_T}}$

$$C_1 \frac{dv_{C1}}{dt} e^{\frac{v_{C1}}{\eta U_T}} = -I_{Int1} e^{\frac{v_{Comp2}}{\eta U_T}} \tag{A.16}$$

Differentiating (A.10), and rearranging

$$e^{\frac{v_{Comp2}}{\eta U_T}} \frac{dv_{Comp2}}{dt} = \frac{\eta U_T}{I_{Comp2} R_{VI}} \frac{dv_{DAC}}{dt} \tag{A.17}$$

Inserting (A.16) and (A.17) into (A.15)

$$\begin{aligned} C_3 \left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}} \right) \frac{dv_{ye}^3}{dt} &= -\frac{I_{Int3}\, I_{Int2}\, I_{Int1}}{C_2\, C_1\, (\eta\, U_T)^2} e^{\frac{v_{Comp2}}{\eta\, U_T}} \\ &\quad -\frac{I_{Int3}\, I_{Int2}}{C_2\, I_{Comp2}\, R_{VI}\, \eta\, U_T} \frac{dv_{DAC}}{dt} \\ &\quad -\frac{I_{Int3}}{I_{Comp2}\, R_{VI}} \frac{dv_{DAC}^2}{dt} \end{aligned} \tag{A.18}$$

Differentiating (A.18)

$$\begin{aligned} C_3 \left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}} \right) \frac{dv_{ye}^4}{dt} &= -\frac{I_{Int3}\, I_{Int2}\, I_{Int1}}{C_2\, C_1\, (\eta\, U_T)^3} e^{\frac{v_{Comp2}}{\eta\, U_T}} \frac{dv_{Comp2}}{dt} \\ &\quad -\frac{I_{Int3}\, I_{Int2}}{C_2\, I_{Comp2}\, R_{VI}\, \eta\, U_T} \frac{dv_{DAC}^2}{dt} \\ &\quad -\frac{I_{Int3}}{I_{Comp2}\, R_{VI}} \frac{dv_{DAC}^3}{dt} \end{aligned} \tag{A.19}$$

Inserting (A.17) into (A.19)

$$\begin{aligned} C_3 \left(\frac{\eta\, U_T}{I_{Exp}\, R_{IV}} \right) \frac{dv_{ye}^4}{dt} &= -\frac{I_{Int3}\, I_{Int2}\, I_{Int1}}{C_2\, C_1\, I_{Comp2}\, R_{VI}\, (\eta\, U_T)^2} \frac{dv_{DAC}}{dt} \\ &\quad -\frac{I_{Int3}\, I_{Int2}}{C_2\, I_{Comp2}\, R_{VI}\, \eta\, U_T} \frac{dv_{DAC}^2}{dt} \\ &\quad -\frac{I_{Int3}}{I_{Comp2}\, R_{VI}} \frac{dv_{DAC}^3}{dt} \end{aligned} \tag{A.20}$$

Rearranged, and divided through by $\frac{C_3\, \eta\, U_T}{I_{Exp}\, R_{IV}}$

$$\begin{aligned} \frac{dv_{ye}^4}{dt} &= -\frac{I_{Int3}\, I_{Exp}\, R_{IV}}{C_3\, I_{Comp2}\, R_{VI}\, \eta\, U_T} \frac{dv_{DAC}^3}{dt} \\ &\quad -\frac{I_{Int3}\, I_{Int2}\, I_{Exp}\, R_{IV}}{C_3\, C_2\, I_{Comp2}\, R_{VI}\, (\eta\, U_T)^2} \frac{dv_{DAC}^2}{dt} \\ &\quad -\frac{I_{Int3}\, I_{Int2}\, I_{Int1}\, I_{Exp}\, R_{IV}}{C_3\, C_2\, C_1\, I_{Comp2}\, R_{VI} (\eta\, U_T)^3} \frac{dv_{DAC}}{dt} \end{aligned} \tag{A.21}$$

Applying the Laplace transform to both sides of (A.21), and rearranging

$$\begin{aligned} LF &\equiv \left.\frac{V_{ye}(s)}{V_{DAC}(s)}\right|_{x=0} \\ &= -\frac{I_{Int3}\, I_{Exp}\, R_{IV}}{\eta\, U_T\, C_3\, I_{Comp2}\, R_{VI}} \left(\frac{1}{s}\right) \\ &\quad -\frac{I_{Int3}\, I_{Int2}\, I_{Exp}\, R_{IV}}{(\eta\, U_T)^2\, C_3\, C_2\, I_{Comp2}\, R_{VI}} \left(\frac{1}{s^2}\right) \\ &\quad -\frac{I_{Int3}\, I_{Int2}\, I_{Int1}\, I_{Exp}\, R_{IV}}{(\eta\, U_T)^3\, C_3\, C_2\, C_1\, I_{Comp2}\, R_{VI}} \left(\frac{1}{s^3}\right) \end{aligned} \tag{A.22}$$

APPENDIX B

MATLAB Code Generating a Flicker-Noise Filter

The presented code models the thermal-and-flicker noise sources introduced in Fig. 4.7.

```
% "FLICKER NOISE GENERATOR" SCRIPT
% ------------------------------------------------------
% Sets up the flicker noise source by calculating the gain, poles, and
% zeros of the filter applied after a thermal noise source.
%
% Methadology:
% Poles and Zeros are placed in pairs equidistantly on the log scale to
% realize a 1/f function, which is then applied to a thermal noise source.
%
% The gain is calculated using the following methodology:
%
% Author: Mohamed Shaheen
% Date: 17th January 2011
%
```

```
% Code based in part on the coding concepts by Hanspeter Schmid


%% INPUTS
DivisionsperDecade = 8;         % Setup the number of divisions per decade for poles/zeros
fCorner = 1e6;                  % Setup the 1/f Corner Frequency


%% CALCULATE POLES AND ZEROS

Wzeros = [];                    % Initialize Wzeros matrix
Wpoles = [];                    % Initialize Wpoles matrix

NSteps = floor(log10(fCorner)*DivisionsperDecade);
% Calculate the total number of divisions for poles/zeros

for k=1:2:(NSteps-1)
% Setup loop for calculating the poles and zeros. (NSteps-1) used instead of NSteps to
% ensure that final zero does not exceed fmax.

    fpole = 10^((k)/DivisionsperDecade);            % Pole in Hz for iteration
    wpole = 2*3.142*(10^((k)/DivisionsperDecade));  % Pole in rad/sec for iteration
    Wpoles=[Wpoles -wpole];                         % Store wpole in Wpoles vector

    fzero = 10^((k+1)/DivisionsperDecade);              % Zero in Hz for iteration
    wzero = 2*3.142*(10^((k+1)/DivisionsperDecade));    % Zero in rad/sec for iteration
    Wzeros=[Wzeros -wzero];                             % Store wzero in Wzeros vector
end


%% CALCULATE GAIN OF THE FILTER

WzerosProduct = 1;              % Initialize WzerosProduct
WpolesProduct = 1;              % Initialize WpolesProduct

% Calculate the product of all the zeros
for i=1:length(Wzeros)
    WzerosProduct = WzerosProduct * Wzeros(i);
end

% Calculate the product of all the poles
```

```
for i=1:length(Wpoles)
    WpolesProduct = WpolesProduct * Wpoles(i);
end

% Calculate Voltage Gain of filter
Vgain = sqrt(fCorner)*abs(WpolesProduct)/abs(WzerosProduct);
```

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