Vacuum Packaging at the Wafer Level for the Monolithic Integration of MEMS and CMOS

Dominique Lemoine
Department of Electrical and Computer Engineering
McGill University, Montréal, Canada
June 2009

A thesis submitted to McGill University in partial fulfillment
of the requirements of the degree of Master of Engineering.

Abstract

A novel vacuum (< 20 mTorr) encapsulation technology for the packaging of micro-electromechanical systems (MEMS) at the wafer level is presented. Because of its low temperature budget (< 350°C), as well as material and chemical compatibility, it supports monolithic integration with CMOS electronics for system-on-chip (SoC) designs. The packaging flow is also suitable for a large range of surface micromachining processes. Hermetic device encapsulation is performed by anodic wafer bonding, while bulk-etched transverse through-wafer vias are used to connect electrically with the encapsulated system. Silicon carbide (SiC) is successfully utilized as a means to membrane stress cancellation and hermeticity improvement.

Experimental results are presented, and the versatility of the technology proposed in this work is illustrated through a comparison with various other state-of-the-art wafer-level packaging technologies. Other applications of the technology beyond packaging, i.e. film bulk acoustic resonators (FBAR) and pressure sensors, are also discussed.

Sommaire

Une nouvelle technologie sous vide (< 20 mTorr) au niveau de la tranche pour l'encapsulation de systèmes microélectromécaniques (MEMS) est présentée. Grâce à son faible budget thermique (< 350°C), ainsi que sa compatibilité tant au niveau chimique que des matériaux, elle convient pour l'intégration monolithique avec de l'électronique de type CMOS, afin de réaliser des systèmes mono-puce (SoC). La séquence d'encapsulation est compatible avec une grande variété de procédés de micromachinage en surface. L'encapsulation hermétique des dispositifs est accomplie par collage anodique de tranches, alors qu'on utilise la gravure en profondeur pour la création de vias à travers la tranche, afin d'établir un contact électrique. Du carbure de silicium (SiC) est utilisé avec succès pour minimiser les contraintes mécaniques des membranes et améliorer leur herméticité.

On présente les résultats expérimentaux, tout en soulignant l'utilité de la technologie développée lors de ce travail en la comparant avec d'autres technologies récentes pour l'encapsulation au niveau de la tranche. D'autres applications de la technologie au delà de l'encapsulation sont également présentées, soit le FBAR et le capteur de pression.

Acknowledgements

I wish to thank my project supervisor Prof. Mourad N. El-Gamal for his unrelenting support as well as the opportunity to work on a very interesting topic. I also want to deeply thank my friend Mr. Paul-Vahé Cicek for working with me throughout this project, revising this thesis, encouraging me, and always providing valuable advice. Special thanks also to Mr. Frederic Nabki for being my mentor and offering countless hours of help.

I am grateful to all the members of the McGill Nanotools Lab who assisted me in my work: Mr. Matthieu V. Nannini, Mr. Donald W. Berry, Mr. Vito Logiudice, Mr. Neal G. Lemaire and Mr. Pierre A. Huet. My thanks also to Prof. Srikar Vengallatore, who very kindly advised me, and to Mr. Laurent Mouden of the LASEM, for very courteous service.

I would like to thank all the members of the RFIC lab that helped make my Master's degree an enjoyable experience: Mr. Thomas Dusatko, Mr. Karim Allidina, Ms. Sareh Mahdavi, Mr. Kuan-Yu Lin, Mr. Faisal Ahmad, Ms. Jane Yu, Dr. Nicolas Constantin, Mr. Guillaume St-Yves, Mr. Ali Taghvaei and Mr. Ali Gorji.

Table of Contents

Abstract — ii

Sommaire — iii

Acknowledgements — iv

List of Figures and Tables — vii

1 • Introduction — 9

1.1 Review of MEMS Applications — 10
1.1.1 Pressure sensors — 11
1.1.2 Inertial sensors — 13
1.1.3 RF-MEMS — 15
1.1.4 MOEMS — 18

1.2 Motivation : A Fully-Integrated PLL — 18
1.2.1 The Filtering Problem — 18
1.2.2 MEM Resonators — 20
1.2.3 Integrated Frequency Generation — 22

1.3 MEMS Packaging — 24
1.3.1 Chip-Level Packaging — 24
1.3.2 Wafer-Level Packaging — 26
1.3.3 Review of Existing WLP Implementations — 28

1.4 References — 30

2 • Description of the Technology — 35

2.1 Features of the technology — 35

2.2 Process Flow — 37
2.2.1 Overview — 37
2.2.2 Description — 38
2.3 Photolithography and Alignment Considerations — 40
2.3.1 Preserving the Alignment Marks — 40
2.3.2 Aligning Patterns with the Wafers — 41
2.3.3 Adjusting the Position of the Wafers for Bonding — 43
2.3.4 Spray Coating Photoresist — 45

2.4 Wafer Bonding Considerations — 45
2.4.1 Altering the Order of the Process Sequence — 45
2.4.2 Changing the Wafer Bonding Method — 46

2.4.3 Adapting the Pre-Bond Cleaning Procedure — 46
2.4.4 Removing SiO_2 Before Anodic Bonding — 48
2.4.5 Protecting the Front of the Active Wafer — 48

2.5 Material and Structural Considerations — 48
2.5.1 Minimizing Chromium Residual Stress — 48
2.5.2 Protecting the Aluminum from RIE of SiO_2 — 49
2.5.3 Masking the Lid Wafer for RIE — 49

2.6 References — 49

3 • Results and Analysis — 51

3.1 Transverse Feedthroughs — 51
3.1.1 Fundamentals of Wet Anisotropic Etching — 51
3.1.2 Design of the Shape of the Feedthroughs — 51
3.1.3 Inspection of the Fabricated Feedthroughs — 52
3.1.4 Electrical Conductivity of the Fabricated Feedthroughs — 53

3.2 Sealing Membranes — 53
3.2.1 Stress Compensation of the Sealing Membranes — 53
3.2.2 Vacuum Confirmation by Membrane Deflection — 55

3.3 Wafer Bonding — 56
3.3.1 Silicon Direct Bonding — 57
3.3.2 Anodic Bonding — 60

3.4 References — 62

4 • Conclusion — 64

4.1 Applications Beyond Packaging — 64

4.1.1 Film Bulk Acoustic Resonator (FBAR) — 64
4.1.2 Piezoresistive Pressure Sensor — 67
4.1.3 Capacitive Pressure Sensor — 68

4.2 Summary — 69

4.3 References — 70

List of Figures and Tables

Figures

Figure 1-1 : SEM micrograph of a MEM pressure sensor. — 11
Figure 1-2 : SEM micrograph of a MEM microaccelerometer. — 14
Figure 1-3 : SEM micrograph of a MEM gyroscope. — 15
Figure 1-4 : SEM micrograph of MEM variable capacitor. — 15
Figure 1-5 : SEM micrograph of a MEM tunable inductor. — 16
Figure 1-6 : SEM micrograph of a MEM switch. — 17
Figure 1-7 : SEM micrograph of a MEM beam resonator. — 17
Figure 1-8 : SEM micrograph of a MEM optical switch. — 18
Figure 1-9 : Illustration of the parameters used in evaluating the Q-factor. — 19
Figure 1-10 : (a) A beam resonator, (b) its first flexural mode, and (c) its electrical equivalent. — 21
Figure 1-11 : Power transmission of a beam resonator in air (left) and in vacuum (right). — 22
Figure 1-12 : Micrograph of a PLL chip, related in size to a MEM resonator. — 23
Figure 1-13 : Typical chip-level packaging. — 24
Figure 1-14 : Chip-level packaging for system-in-package integration. — 25
Figure 1-15 : Batch processing at the wafer level. — 26
Figure 1-16 : Direct surface mounting of a wafer-level package. — 27

Figure 2-1 : Color legend for process materials. — 35
Figure 2-2 : WLP with CMOS/MEMS monolithic integration. — 35
Figure 2-3 : Direct surface mounting of WLP chip on a PCB. — 36
Figure 2-4 : WLP chip featuring optical accessibility. — 36
Figure 2-5 : Fabrication process flow. — 37
Figure 2-6 : Cross-section of the wafer showing the preserved alignment marks. — 41
Figure 2-7 : Lithographic procedure for front-to-back alignment. — 42
Figure 2-8 : Incorrectly centered patterns on wafers resulting in misaligned wafers. — 43
Figure 2-9 : Wafer alignment procedure prior to bonding. — 44
Figure 2-10 : Separation flags properly placed between the two wafers. — 44

Figure 3-1 : TMAH etching of <100> silicon. — 51
Figure 3-2 : Dimensions for TMAH etching <100> silicon. — 52
Figure 3-3 : SEM cross-section of feedthrough, overall (left) and close-up (right). — 53
Figure 3-4 : Residual stress of the sealing membrane constituent materials. — 54
Figure 3-5 : Membrane (a) before SiO_2 removal, (b) after back Al sputter, (c) after back SiC sputter. — 54

Figure 3-6 : SEM cross-section of a SiC reinforced sealing membrane. 55
Figure 3-7 : Membrane deflection caused by a pressure difference. 55
Figure 3-8 : The razor blade crack test technique. 57
Figure 3-9 : Hydrated silicon wafers. 58
Figure 3-10 : Dehydration and creation of silanol bonds. 58
Figure 3-11 : High-temperature annealing. 59
Figure 3-12 : Crack test performed on Si-Si direct bonded wafers. 59
Figure 3-13 : Voids at the bond interface of Si-Si direct bonded wafers. 60
Figure 3-14 : Anodic bonding by electrical displacement of the Na^+ ions. 61
Figure 3-15 : Voids at the bond interface of Si-Pyrex anodically bonded wafers. 61

Figure 4-1 : Color legend for process materials. 64
Figure 4-2 : Stress response of the AlN crystalline structure. 65
Figure 4-3 : Stress field amplitude of the piezoelectric material at resonance. 65
Figure 4-4 : FBAR implementation. 66
Figure 4-5 : Piezoresistive pressure sensor implementation. 67
Figure 4-6 : Capacitive pressure sensor implementation. 68

Tables

Table 1-1 : Comparison between chip level and wafer level packaging. 28
Table 1-2 : Comparison of lateral and vertical interconnects. 29
Table 1-3 : Comparison of different works on WLP 30

Table 3-1 : Measured dimensions with TMAH etching. 52

1 Introduction

The deployment of micro-electromechanical systems (MEMS) has experienced a significant growth in recent years, and is expected to maintain this trend for many years to come. Electronics are often combined with MEMS for sensing and control applications. There is a pressing need for full monolithic integration of circuits and MEMS within one process flow, in order to reduce size, cost, and improve performance.

The vast majority of MEM devices require hermetic packaging, many in a vacuum environment. For example, while the quality (Q)-factor of a given MEM resonator could reach a maximum of 100 under atmospheric pressure, the same resonator can reach Q-factors higher than 1000 in high vacuum environments [1]. Packaging is, in general, of critical importance for the successful commercialization of MEMS-based solutions.

Vacuum packaging can be performed at the chip level, where each MEMS chip, or IC+MEMS chip, is individually enclosed in a hermetically sealed package. Recently, however, wafer-level packaging (WLP) has emerged as a promising substitute to chip-level packaging (CLP), offering many benefits related to cost, size, and performance.

In this work, we propose a novel WLP technology for the encapsulation of MEMS in vacuum [2], for which a provisional patent was filed [3]. The technology was initially designed to complement the low-temperature fabrication process detailed in [4], but it can, in practice, be applied to various other surface micromachining MEMS processes, to achieve hermetic or even vacuum sealing.

The process flow developed in this work uses silicon carbide-reinforced membranes as a novel method to enable vacuum sealing at the wafer level with transverse feedthroughs. A key feature of the process is that it is fully CMOS-compatible, both in terms of the processing temperatures involved and the chemicals used, so as to allow for

monolithic integration of MEM devices directly on top of CMOS electronics [5]. To the knowledge of the author, in literature, no other WLP process with transverse feedthroughs offers CMOS compatibility. Once packaged and diced, the encapsulated dies can be directly affixed to a printed circuit board (PCB) using standard surface mounting techniques, thus significantly reducing the physical system size and parasitic effects inherent to conventional chip-level packaging solutions.

The process was experimentally developed and tested in the McGill Nanotools Laboratory, with partial runs on over 150 substrate wafers for selected steps, and with the complete process sequence on more than 150 wafers. All the tests were performed without CMOS or MEMS, although that constitutes the next step in the evolution of this research.

In the remainder of this chapter, we review some of the important applications of MEMS, followed by an overview of the larger project that drove the development of the technology described in this work. Next, we discuss the superiority of WLP over CLP and detail some of the WLP technologies developed throughout literature. Chapter 2 presents the features of the technology developed here and details the process flow, and then underlines the design decisions made during process development. In chapter 3, we present and discuss the experimental results. Finally, in chapter 4, we conclude and present some alternative applications of the technology.

1.1 Review of MEMS Applications

Microelectromechanical systems consist of miniature mechanical devices controlled by electrical signals, which can be either used for sensing or actuation purposes. Sensor devices are used to measure various parameters, whereas actuators cause an action, usually mechanical. By definition, a MEMS has at least one of its dimensions in the micrometer range. At that scale, classical physics may behave differently than intuition would usually suggest. Since a MEMS has a very small mass, the impact of gravity is mostly negligible. On the other hand, surface effects such as air

resistance, wetting and electrostatics play a major role, because of the large area-to-volume ratios involved.

In addition to the decrease in size and cost achieved through batch production, scaling down devices to brings about several benefits including shorter response times and a significant decrease in power consumption [5]. Also, because MEMS processes were first inspired by semiconductor integrated circuit (IC) manufacturing techniques, many micromachine applications have the potential for direct integration with electronics, and thus for extending the functionalities that can be included on a single die, as described for example in [6]-[12].

MEMS processes can be divided into *surface micromachining*, where devices are built by layering and patterning materials on top of the substrate, and *bulk micromachining*, where structures are made by etching into the substrate. In this chapter, we present some of the most common surface micromachined MEMS that constitute prime candidates for hermetic packaging: pressure sensors, inertial sensors, RF MEMS and MOEMS.

1.1.1 • Pressure Sensors

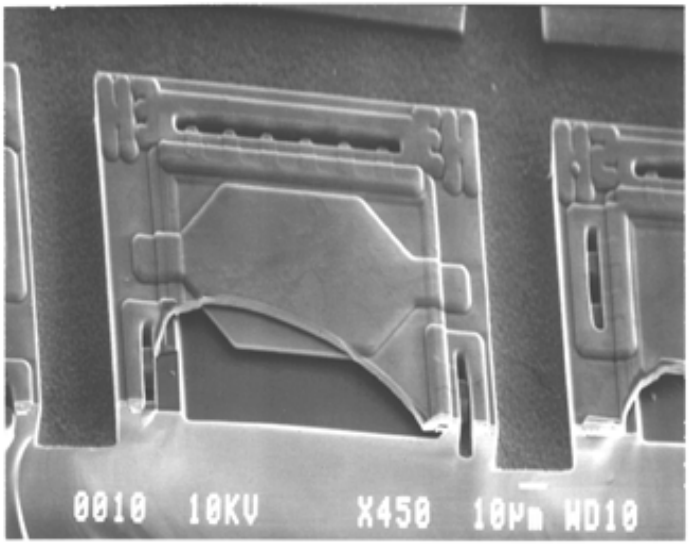

Figure 1-1 : SEM micrograph of a MEM pressure sensor [13].

Pressure sensors constitute one of the largest market for MEM sensors [14] and are used in various applications including tire pressure measurement, disposable blood pressure sensing, and near-vacuum applications. In most cases for greater-than-atmospheric pressure, sensing is performed by a deformable diaphragm separating two regions of different pressure. The ensuing deflection of the diaphragm is related to the pressure difference between the two regions. For a diaphragm experiencing low intrinsic stress and small deflections (i.e. less than half the diaphragm thickness), diaphragm deflection is directly proportional to the applied pressure [15]. To translate this deflection into a pressure measurement value, different types of sensing can be used, namely piezoresistive, piezoelectric and capacitive.

In piezoresistive sensing, the membrane supports a piezoresistor, whose resistance varies with deformation. Hence, an appropriate electronic circuit can output the value of the pressure from the variation in the resistivity of the piezoresistor arising from the membrane deflection.

Piezoelectric sensing is similar to the piezoresistive method, with the difference that the membrane deflection generates an electric potential rather than a variation in resistivity, due to the presence of a piezoelectric material on the membrane. Pressure can conveniently be computed from this generated potential.

In capacitive sensing, the diaphragm acts as one of the plates of a capacitor, with a matching static parallel plate fabricated just across. Therefore, a deflection of the membrane modifies the capacitance between the two plates, which can then easily be related to the pressure.

Measuring vacuum with high sensitivity is often better accomplished by using other means than diaphragms. The two most common methods are the Pirani gauge [16] and the resonator sensor [17].

The Pirani gauge consists of a suspended electrically-conductive filament through which a constant direct current flows. The higher the vacuum in the environment, the fewer air particles are present to cool down the filament. Depending on the temperature

caused by power dissipation, the resistivity of the filament is modulated, through which the pressure can be inferred.

One can also use a resonator (operation detailed in section 1.2.2) as a pressure sensor, by monitoring its resonant frequency versus pressure. Contrarily to diaphragm-based methods, resonant pressure sensors require more elaborate electronics to monitor a frequency rather than an amplitude. However, they present numerous advantages in vacuum conditions, namely higher accuracy, sensitivity and resolution [17]-[19].

1.1.2 • Inertial Sensors

Like pressure sensors, microaccelerometers currently constitute one of the largest commercial applications for MEMS. They are used to measure accelerations in common applications such as air bag release, transportation stabilization and navigation systems. Recently, they have been included, with much public interest, into personal electronic devices to increase usability and entertainment value.

Fundamentally, a MEM accelerometer is composed of an inertial mass attached to flexural supports, and can be modeled as a linear second-order mass-damper-spring system [21]. An external acceleration, in proportion to its intensity, causes the mass to deflect a certain distance from its rest position. An in-plane MEM accelerometer senses acceleration in the plane of the die, while an out-of-plane accelerometer senses acceleration perpendicular to the die. The combination of two perpendicular in-plane and one out-of-plane accelerometers allows for three-dimensional accelerometric sensing. The magnitude of the displacement caused by acceleration can be sensed through various methods, two of the most common being capacitive and piezoresistive.

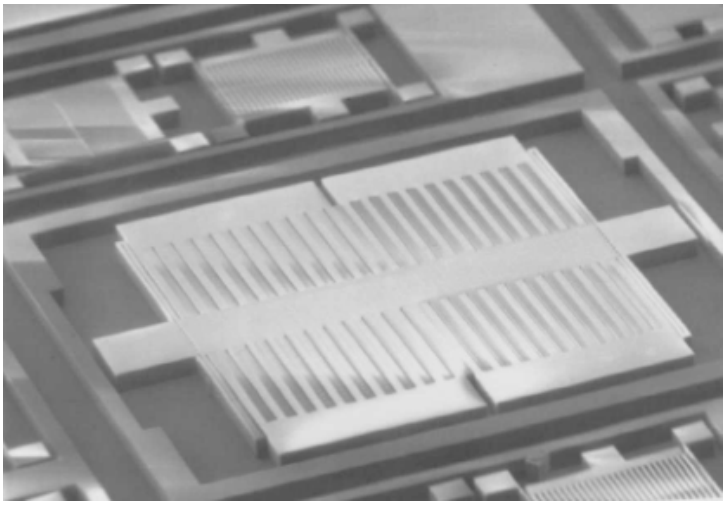

Figure 1-2 : SEM micrograph of a MEM microaccelerometer [20].

In capacitive-based accelerometers, the variation in the capacitance is measured between a fixed electrode and the inertial mass acting as the other electrode. With an out-of-plane MEM accelerometer, both electrodes are parallel to the die, so the measurable range of accelerations is relatively small before the plates come into contact. In fact, the maximum detectable acceleration is limited by the distance between the two plate electrodes. The in-plane accelerometer also consists of a fixed electrode and an inertial-mass. However, their separation lies in the plane of the die, which makes it worthwhile to use interdigital comb structures to maximize capacitive coupling without significantly increasing the required area on the die.

In a piezoresistive accelerometer, the inertial mass is attached between two piezoresistive springs. Under acceleration, the mass is forced to move to one side, thus compressing one spring and stretching the other. The springs' deformations cause variations in their resistivity, from which the acceleration can determined.

Analogously to MEM accelerometers, MEM gyroscopes can be used to sense rotational movements.

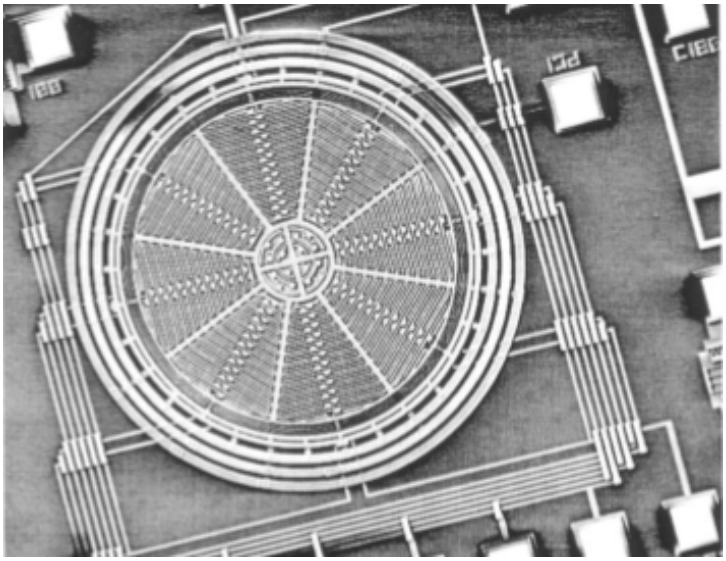

Figure 1-3 : SEM micrograph of a MEM gyroscope [22].

1.1.3 • RF MEMS

RF MEMS serve to substitute traditional components in radio-frequency (RF) electronic systems. They present tremendous appeal, as they often allow to replace bulky off-chip electronic components (e.g. capacitors, inductors, quartz crystals), while achieving similar or even superior performance.

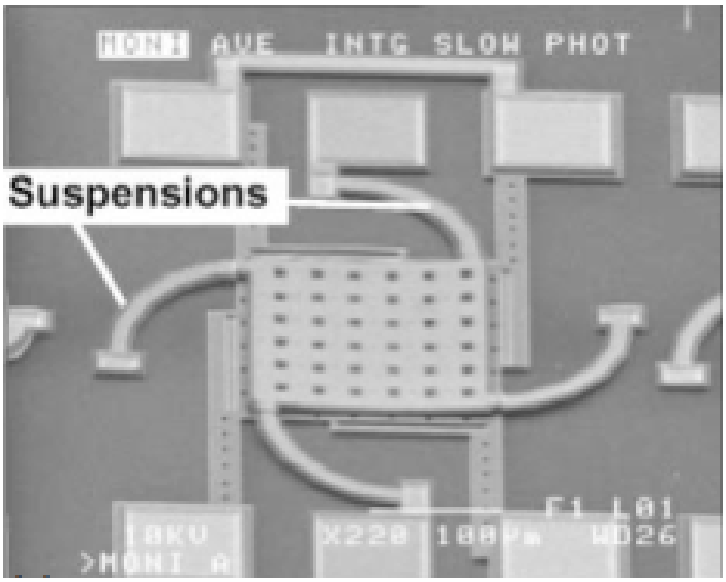

Figure 1-4 : SEM micrograph of MEM variable capacitor [23].

A MEM variable capacitor (varicap) implements a capacitance whose value can be adjusted through a DC actuation voltage. The varicap is composed of two parallel plates, one of them mobile with spring suspensions. The distance between these two plates is determined by the actuation voltage, which causes an electric force to attract them together. With increasing voltage, the separation between the plates, d, decreases, thereby increasing the capacitance, C, according to:

$$C = \frac{k\varepsilon_0 A}{d}, \tag{1.1}$$

where k is the dielectric constant of the medium between the plates, ε_0 is the permittivity of free space and A is the overlap area of the two plates. Customarily, tunable capacitances are implemented on ICs by the use of varactors (p-i-n or field-effect-transistor diode), which exhibit a highly non-linear behavior with respect to control voltage as well as frequency [24]. Replacing the varactor with a varicap eliminates these non-linearities, while offering the potential for integration on semiconductor chips.

MEMS technology also permits the fabrication of integrated tunable inductors, which is unachievable by conventional methods. A tunable inductor can be implemented by harnessing the mutual inductance of electrostatically displaceable coils.

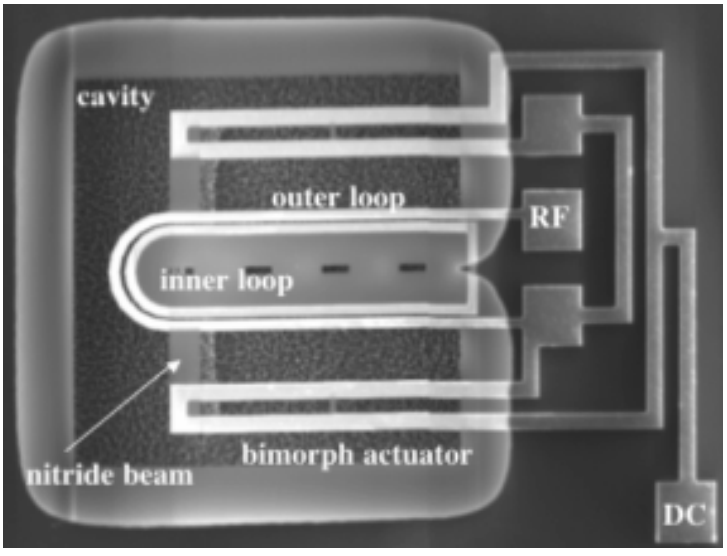

Figure 1-5 : SEM micrograph of a MEM tunable inductor [25].

Micro-switches may also be fabricated through RF MEMS processes, to allow either transimission or blocking of an electrical signal. A suspended structure is usually made to collapse on an electrode by an electrostatic voltage, so as to make a contact for transmission.

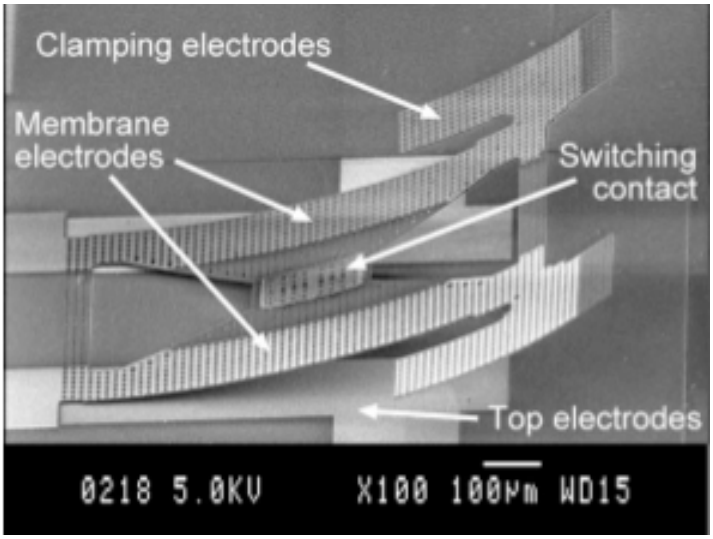

Figure 1-6 : SEM micrograph of a MEM switch [26].

MEM resonators are structures that harness mechanical resonance to filter an electrical signal in the frequency domain (more details in section 1.2.2). Resonators are of particular interest for frequency generation applications, as a replacement for the omnipresent (and bulky) off-chip quartz resonators.

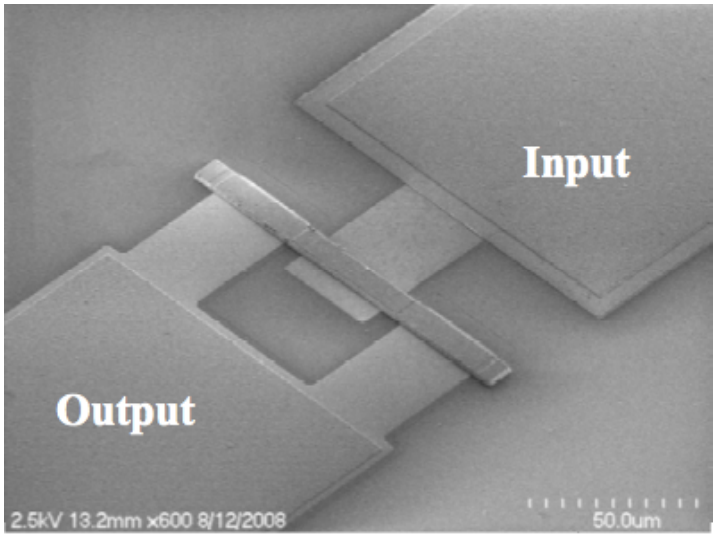

Figure 1-7 : SEM micrograph of a MEM beam resonator [27].

1.1.4 • MOEMS

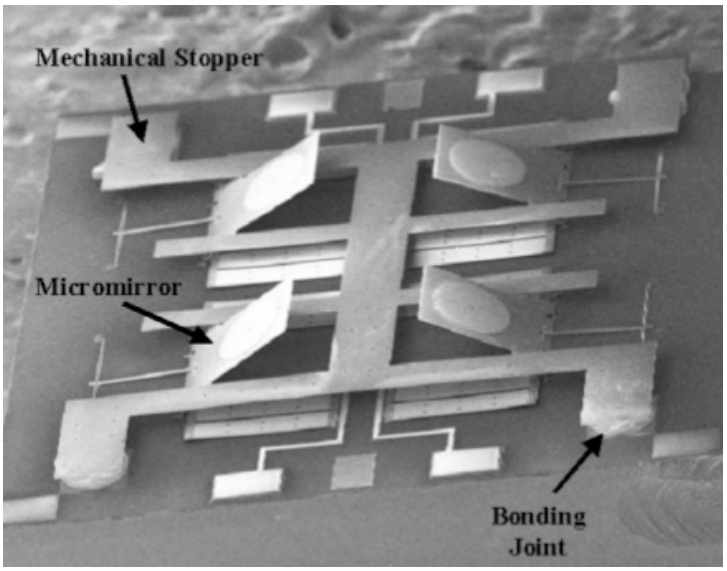

Figure 1-8 : SEM micrograph of a MEM optical switch [28].

Micro-opto-electromechanical systems (MOEMS) are used to manipulate optical signals at a small scale, with devices such as optical switches, cross-connects and microbolometers [29]. One of the fundamental building blocks of MOEMS is the micromirror, which is used to reflect light in a desired direction. Through a DC actuation voltage, the orientation of the micromirror can be varied. The Digital Micromirror Device (DMD) chip used in a Digital Light Processing (DLP) display projector is a current commercial application of micromirrors. Each micromirror on the DMD chip corresponds to one pixel of the image to project, and it can be oriented to either send light out for projection or not.

1.2 Motivation : A Fully-Integrated PLL

1.2.1 • The Filtering Problem

In the design of electronic systems, filters are quite often used as fundamental building blocks, with the purpose of modifying a signal by removing the unwanted frequency content and preserving the frequency bands of interest. For radio frequency (RF) applications in particular, it is imperative that most passive elements have the highest possible quality (Q)-factor, so as to attain the best possible electrical performance

in terms of gain, bandwidth, noise and power consumption [30]. The Q-factor expresses the ability of a device to operate exclusively in a narrow bandwidth around a chosen center frequency. It is defined as the resonant frequency divided by the half-power bandwidth (or 3 dB bandwidth), or equivalently as the ratio of the energy stored to the energy dissipated per cycle:

$$Q = \frac{f_{res}}{f_2 - f_1} = 2\pi \frac{E_{stored}}{E_{dissipated}}. \tag{1.1}$$

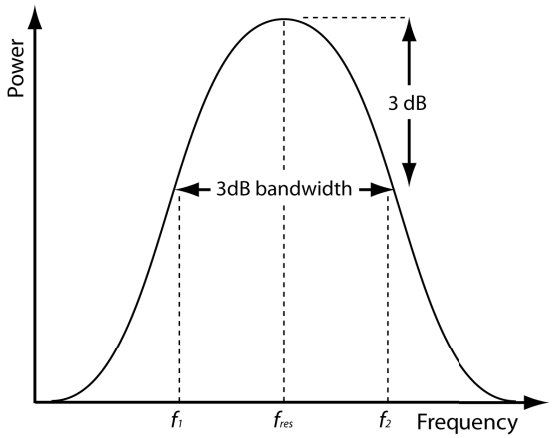

Figure 1-9 : Illustration of the parameters used in evaluating the Q-factor.

Typically, high quality filtering in the electrical domain is performed either by using off-chip surface-acoustic wave (SAW) filters or several off-chip capacitors and inductors, with both solutions being markedly bulky. Nowadays, with the demand for ever increasing performance and miniaturization, off-chip components appear especially unattractive because of their considerable physical size and detrimental electrical parasitic effects. Indeed, the combined size of the off-chip components required for filtering can lie in the same order of magnitude as the chip containing all the rest of the electronics for the entire system. Furthermore, because of the interconnections required for signal transfer between the chip and the external components, parasitic effects are introduced, causing significant signal degradation that must be addressed in some way. Often, this forces the circuit designer to accept a more severe tradeoff on the performance of the system, e.g. higher power consumption, than would normally be the case without the parasitics.

We must note that filters can be realized on-chip with the use of integrated spiral inductors and capacitors (e.g. metal-insulator-metal). In some cases, this solution enables a reduction in the size of the complete system as well as the parasitic effects, compared to an implementation based on external components. However, this method is not generally suitable for high selectivity filtering, since the Q-factor of an integrated spiral inductor usually lies in the 10 to 20 range [31], which is orders of magnitude lower than the typical requirement for high quality filtering. On-chip filtering is also not adequate for low frequencies, due to the prohibitive sizes of the inductors and capacitors needed.

It is possible and highly advantageous to perform filtering in a system by replacing the passive elements with MEMS. Indeed, MEM devices surpass their external counterparts because of their smaller size, their lower power consumption and their potential for monolithic integration with the electronics, while maintaining comparable Q-factors. A variety of MEMS can be used for filtering purposes, such as tunable capacitors, inductors, switches and resonators.

1.2.2 • MEM Resonators

Among all types of MEM actuators that can be used for filtering, we specifically examine the flexural-mode resonator in greater detail, as it constitutes a central piece of the larger project for which this packaging work was first initiated. The resonator is a specific type of MEMS that very conveniently implements narrow bandpass filtering. It is designed to convert an electrical signal into mechanical energy, perform the required filtering mechanically, then convert the signal back to the electrical domain. Hence, we benefit from Q-factors that are much higher in the mechanical realm than in a purely electrical system [32].

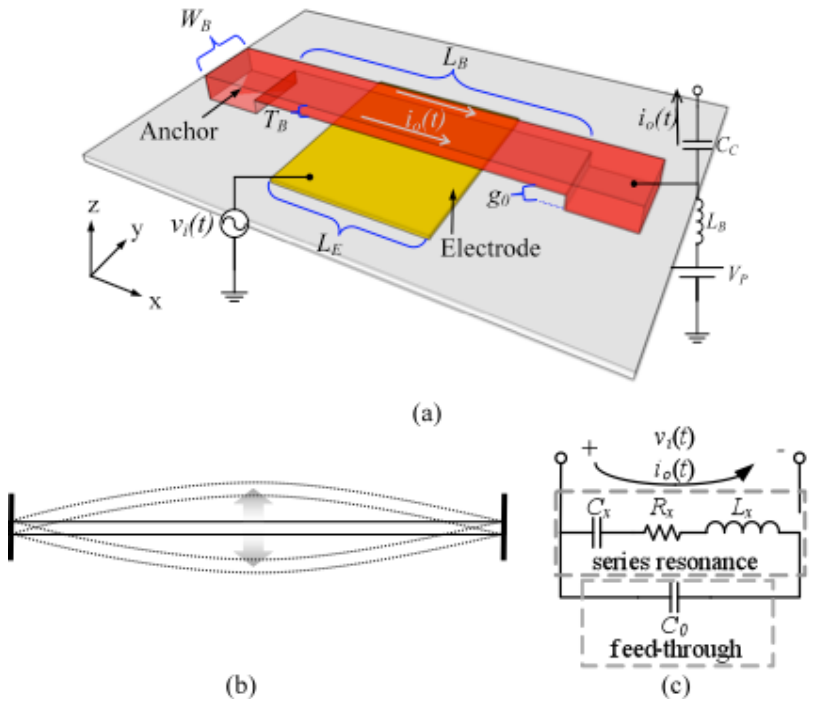

Figure 1-10 : (a) A beam resonator, (b) its first flexural mode, and (c) its electrical equivalent [33].

In its simplest form, the MEM resonator is composed of a single fixed-fixed cantilever beam, i.e. anchored at both ends, with an actuation electrode lying underneath. Both the beam and electrode are electrically conductive, in order to permit capacitive coupling and electrostatic actuation. For device operation, both a DC static voltage and an AC electrical signal are applied between the electrode and the beam. The DC voltage serves to activate the resonator, i.e. to enable it to vibrate when excited by the proper AC signal. Indeed, if the AC signal has a frequency component with sufficient power near the resonance of the beam, the resonator vibrates at that particular frequency, dampening all other incoming frequencies. The filtered signal can be converted back to the electrical domain, through the variation in capacitance between the conductive plates formed by the electrode and the beam [32].

The Q-factor of a MEM cantilever resonator is strongly related to the gaseous pressure in its environment, because of the squeeze film damping effect [34]. Indeed, in such structures where a very thin gap exists underneath the vibrating beam, the thin layer of gas molecules accentuate the damping phenomenon, thus degrading the achieved Q-factor. Since we target the highest achievable Q-factor for narrowband filtering, we

attempt to have the devices operate under the highest possible vacuum conditions (i.e. lowest possible pressure). Figure 1-11 compares the operation of a MEM beam resonator fabricated with [4] in air and in high vacuum (1.35 mTorr). Performance is obviously superior in vacuum conditions.

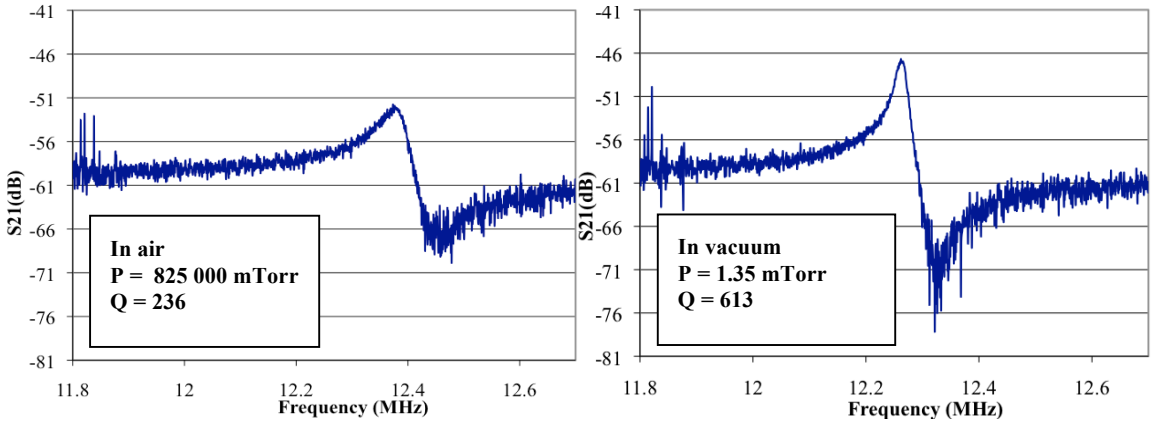

Figure 1-11 : Power transmission of a beam resonator in air (left) and in vacuum (right).

Understandably, encapsulating devices in vacuum poses considerable challenges during the packaging stage of production. Indeed, the selected package must provide a hermetic seal to allow the retention of a very low pressure inside the cavity surrounding the MEM resonators. Additionally, one must ensure that there is minimal long-term leaking of the pressure, which would inevitably cause performance degradation of the devices over time.

1.2.3 • Integrated Frequency Generation

MEM resonators are currently gathering interest as a convenient means of generating a reference frequency, e.g. [35]. They can be used as a substitute for the omnipresent quartz crystals in electronic systems, with the key advantage of a size footprint orders of magnitude tinier. Furthermore, contrarily to crystals, MEMS have the potential for monolithic integration onto an electronic chip, opening the door to full system-on-chip (SoC) implementations and lower costs.

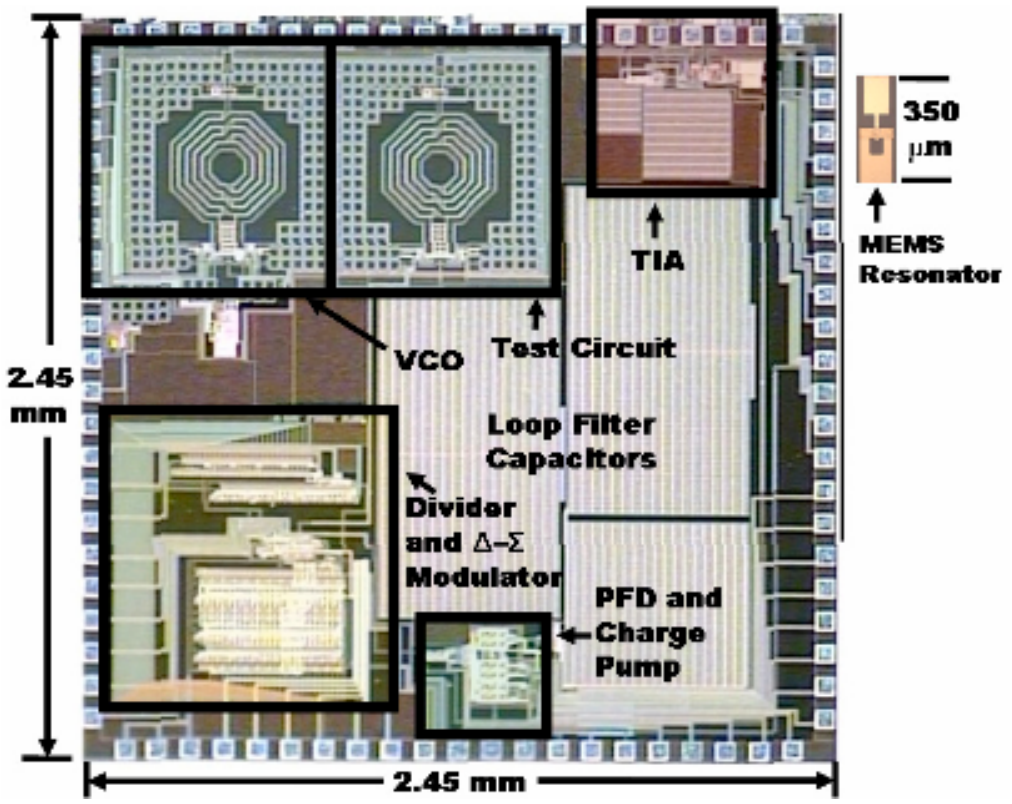

Figure 1-12 : Micrograph of a PLL chip, related in size to a MEM resonator [35].

Stable reference frequencies are essential to frequency synthesis, precision timing applications and RF transceivers in general. The packaging process proposed here was first undertaken with the objective of encapsulating a complete phase-locked loop (PLL) circuit for the generation of a stable frequency in the gigahertz range, using an integrated MEM resonator, rather than a conventional quartz crystal, to produce the initial reference frequency [35].

Despite numerous benefits, monolithic integration of electronics and MEMS imposes significant constraints on the packaging of the system. Since both the electronic devices and MEM devices are present on the system chip, the encapsulation process must never exceed the thermal budget tolerable by the semiconductor nor the MEMS technology – a limit which is often imposed by the presence of doping profiles and metals, such as aluminum. Furthermore, the materials and chemicals used for packaging must all be compatible with those used for the fabrication of the electronic and MEM devices [36]. For a system comprising RF MEMS, the packaging methodology must ensure sufficient vacuum for satisfactory long term operation.

1.3 MEMS Packaging

1.3.1 • Chip-Level Packaging

Chip-level packaging is the typical method used in the production of commercial integrated circuit semiconductors, where, after the electronic devices are fabricated, the wafer is diced into individual chips to be each inserted into a package. The pads of the IC chip are subsequently wire bonded to the appropriate package pins, and the package is then covered. These packages can then be mounted onto a PCB.

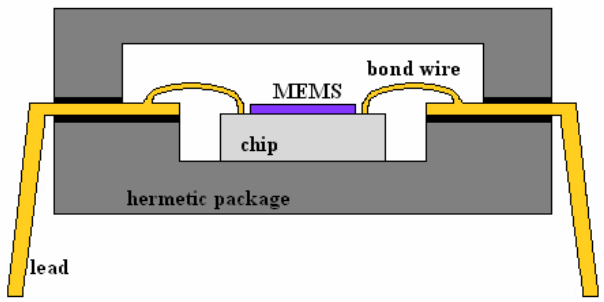

Figure 1-13 : Typical chip-level packaging.

Although MEMS fabrication techniques are very similar to those used for semiconductors, the mechanical nature of the micro-structures imposes additional packaging requirements. MEMS tend to be quite fragile, due to their operation based on movement, and therefore require adequate protection from the environment. Some types of MEMS also present particular issues. For instance, MEM resonant devices can benefit from a vacuum environment to minimize squeeze-film damping effects that degrade their Q-factors [34]; bioMEMS for implantation in the human body require biocompatibility to prevent rejection [37]; MOEMS necessitate optical accessibility so that they are able to interact with light signals; microsystems in general benefit from being sealed from dust and debris in a hermetic cavity.

Therefore, specialized hermetic cavity packages must be used to encapsulate MEMS in accordance with their particular needs. The packages are usually composed from either plastic, ceramic or metal. In all cases, they are significantly more expensive than standard IC packages, even more so when hermetic vacuum packaging is desired,

because of the non-trivial sealing procedure involved. In fact, the costs of using CLP for hermetic packaging can often significantly exceed all the other costs involved in the manufacturing of a system comprising MEMS. As stated by Varadan, "for a standard integrated circuit, the packaging process can take up to 95% of the total manufacturing cost. Issues in MEMS packaging are much more difficult to solve because of stringent requirements in processing, handling and the nature of fragile microstructures; the diversity also complicates the packaging problem." [38]

Currently, a prevalent trend is to integrate all components of a system as tightly as possible. In the case of a system combining electronics and MEMS, multiple chips can be included in a cavity package and wire bonded together, resulting in a system-in-package (SiP) implementation.

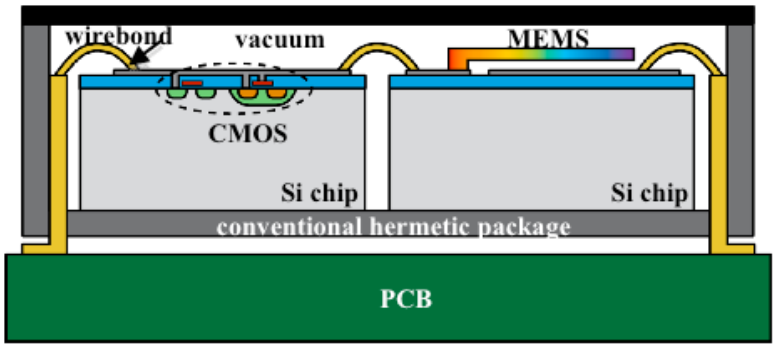

Figure 1-14 : Chip-level packaging for system-in-package integration.

Even though it is currently the leading packaging method in industry, CLP presents significant drawbacks that make it both costly and functionally non-optimal:

1) Very expensive hermetic packages are required.

2) The chips must be encapsulated individually rather than by means of a batch process, increasing lead time and elevating costs.

3) The fragile MEM devices are not protected during dicing and wire bonding, which has a negative impact on yield, thus incurring greater costs.

4) Significant capacitive and inductive parasitic elements are introduced by means of package pins and wire bonds, with adverse effects for most applications, e.g. radio frequency systems.

As such, research and development are rapidly shifting toward the development of wafer-level packaging processes to alleviate the issues arising from CLP.

1.3.2 • Wafer-Level Packaging

Whilst a WLP process is more complex to develop than CLP, it does present various worthwhile advantages [39]. First, it allows batch encapsulation at the wafer scale, so the encapsulation of MEM devices effectively becomes a part of the micro-fabrication flow, rather than a post-process operation. Therefore, the different chips on a wafer do not need to be enclosed individually, because they are all processed simultaneously. This makes such a WLP process more efficient as well as cheaper for mass production, resulting in improved performance and cost.

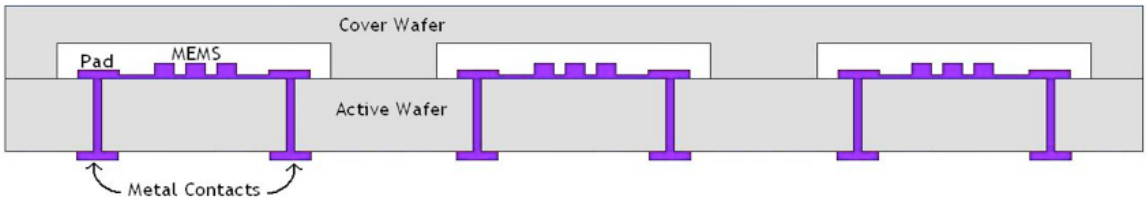

Figure 1-15 : Batch processing at the wafer level.

After the WLP process is complete, the encapsulated chips can still be packaged in a conventional manner if desired. However, the external package is then neither responsible for hermetically preserving a vacuum environment nor ensuring the fine mechanical protection of the MEMS: all of this is performed by the WLP encapsulation. The only potential purpose of this package (if used at all) is to provide coarse mechanical protection and an electrical interface. Hence, inexpensive standard packages can be used instead of customized CLP solutions. Alternatively, an attractive option is to surface mount the WLP-encapsulated MEMS chip directly to the PCB, totally circumventing the need for an external package.

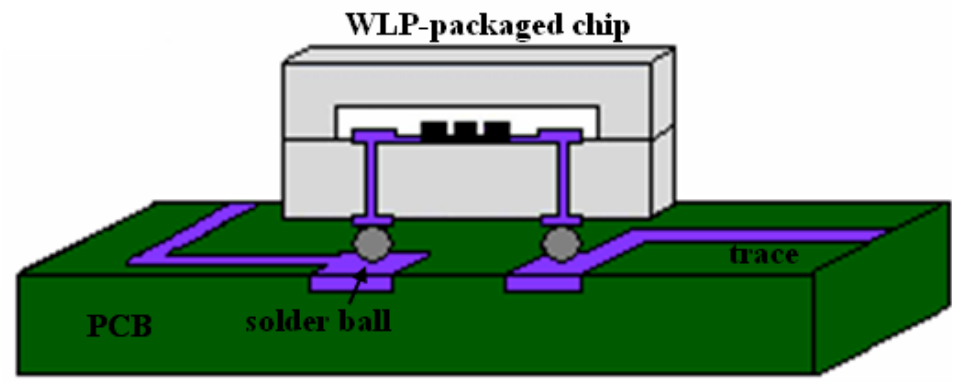

Figure 1-16 : Direct surface mounting of a wafer-level package.

Additionally, because the MEMS are protected at an earlier stage of the microfabrication flow with WLP, the overall device yield improves, thereby lowering cost. The released devices are therefore encapsulated before the chips are even diced, which prevents some of the fragile structures from being damaged by dust and debris.

Furthermore, a WLP process can be advantageous in terms of electrical testability. MEM devices requiring a particular gaseous environment to operate satisfactorily must be encapsulated before electrical testing can be performed. With CLP, expensive enclosures are wasted to test faulty devices, since each die must be fully packaged before it can be verified. On the other hand, WLP allows devices to be tested at the wafer-level using a probe station without the need for any test fixture, since the devices are already encapsulated in vacuum. Therefore, malfunctioning devices can be conveniently singled out, so that only the operational devices are further processed.

In this work, we present a WLP technology designed to minimize the processing temperatures involved, so as to provide maximum compatibility with a large number of custom MEMS processes, even when low melting point metal interconnects such as aluminum are present. Most importantly, these low processing temperatures open the door to packaged integration of MEMS with CMOS semiconductor processes, to achieve monolithic system-on-chips.

Table 1-1 : Comparison between chip level and wafer level packaging.

	CLP	WLP
Development Effort	**Low**	High
Processing methodology	Each chip encapsulated separately	**Batch encapsulation**
Commercial package required	Expensive, custom-built	**None**
Device protection	After dicing and wire bonding	**Before dicing and wire bonding**
Parasitics	High	**Low**
Testability	At package level	**At wafer level**
Final size	Large	**Small**

1.3.3 • Review of Existing WLP implementations

In this work, we are focused on designing a wafer-level packaging suitable for monolithic integration of CMOS and MEMS. Therefore, the CMOS compatibility of the process is of the utmost importance, and is conditional on several process criteria, i.e. maximum temperature reached, materials used and chemicals used. In most cases, the highest temperature in a process is applied during wafer bonding for device encapsulation, and should ideally be kept below 350 °C, which eliminates glass frit bonding, and severely limits the efficiency of silicon direct bonding and many types of eutectic bonding. If anodic bonding is used, it must be optimized to decrease its operating temperature as much as possible. Also, the MEMS must obviously be fabricated on a silicon substrate for CMOS compatibility.

Another principal requirement in this work is that the packaging process be suitable for high-vacuum encapsulation. This implies that adhesive bonding is not an option, due to the high polymer outgassing in vacuum. Also, the interconnects should ideally not traverse the bond interface, as that could lower the hermeticity of the seal. Hence, vertical feedthrough interconnects are preferred. Table 1-2 outlines the impacts of using either lateral or vertical interconnects. Despite the added complication to the

fabrication process, vertical feedthroughs are preferred, because they can improve hermeticity and reduce the electrical parasitic effects. In [45], an original method is presented that eliminates the need for physical interconnects, by using electromagnetic coupling. However, this technique applies only for GHz-range signals, and would therefore not be suitable for DC actuation.

Table 1-2 : Comparison of lateral and vertical interconnects.

	Lateral Interconnects	Vertical Interconnects
Fabrication	**surface micromachining**	bulk micromachining
Wafer Robustness	**higher**	lower
Photoresist Application	spin coater	spray coater
Wafer bonding method	adhesive / eutectic / frit glass	**any**
Hermeticity	more leakage	**less leakage**
Electrical Parasitics	higher	**lower**

Another objective in this work is to provide optical accessibility to the interior of the encapsulation environment, so as to permit the inclusion of MOEMS. For this to be possible, the lid wafer must be optically transparent.

Table 1-3 compares several wafer-level packaging technologies from literature, highlighting the advantages of each, according to the objectives of this thesis. From this analysis, one can clearly see the need for a low-cost CMOS-compatible process for vacuum encapsulation, a goal which the process developed in this work aims to accomplish.

Table 1-3 : Comparison of different works on WLP

	Substrate wafer	Lid wafer	Inter-connects	Bonding method	Max temp.	High vacuum (< 20 mTorr)	CMOS compatible
[40]	**Si**	**glass**	**vertical**	adhesive	**210 °C**	no	**YES**
[41]	glass	Si	lateral	eutectic	**180 °C**	***maybe***	no
[42]	glass	Si	**vertical**	**anodic**	<400 °C	**YES**	no
[43]	glass	Si	**vertical**	**anodic**	<400 °C	**YES**	no
[44]	**Si**	Si	lateral	eutectic	390 °C	***maybe***	***maybe***
[45]	**Si**	**glass**	E-M	**anodic**	<400 °C	**YES**	**YES**
[46]	**Si**	Si / **glass**	**vertical**	frit glass	400 °C	**YES**	***maybe***
[47]	**Si**	**glass**	**vertical**	**anodic**	400°C	**YES**	***maybe***
This work	**Si**	**glass**	**vertical**	**anodic**	**350 °C**	**YES**	**YES**

1.4 References

[1] C. T.-C. Nguyen, "Vibrating RF MEMS for Next Generation Wireless Applications", *Proc. Custom Integrated Circuits Conference*, pp. 257-264, Oct. 2004.

[2] D. Lemoine, P.-V. Cicek, F. Nabki, and M. N. El-Gamal, "MEMS wafer-level vacuum packaging with transverse interconnects for CMOS integration," *Proceedings of the Custom Integrated Circuits Conference*, pp. 189-192, September 2008.

[3] D. Lemoine, P. Cicek, F. Nabki, and M. N. El-Gamal, "Low-Temperature Vacuum Wafer-Level Packaging for MEMS Devices," patent # PCT/CA2009/000292, Mar. 2009.

[4] F. Nabki, T. Dusatko, S. Vengallatore, and M. N. El-Gamal, "Low Temperature (<300°C) Low-Stress Silicon Carbide Surface Micromachining Fabrication Technology," *Proc. Solid-State Sensors, Actuators and Microsystems Workshop*, Hilton Head Island, pp. 216-219, June 2008.

[5] M. Madou, "Fundamentals of Microfabrication", CRC Press LLC, Florida, USA, 1997.

[6] D. Ruffieux, J. Chabloz, C. Muller, F.-X. Pengg, P. Tortori, and A. Vouilloz, "A 2.4 GHz MEMS-based transceiver," *Digest of Technical Papers of the IEEE International Solid State Circuits Conference*, pp. 522-523, February 2008.

[7] A. v. Bezooijen, M. A. d. Jongh, C. Chanlo, L. C. H. Ruijs, F. v. Straten, R. Mahmoudi, and A. H. M. v. Roermund, "A GSM/EDGE/WCDMA adaptive series-LC matching network using RF-MEMS switches," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 10, pp. 2259-2268, October 2008.

[8] K. Sundaresan, G. K. Ho, S. Pourkamali, and F. Ayazi, "Electronically temperature compensated silicon bulk acoustic resonator reference oscillators," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1425-1434, June 2007.

[9] P. Ancey, "Above IC RF MEMS and BAW filters: fact or fiction?," *Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 1-5, October 2006.

[10] G. K. Fedder and T. Mukherjee, "Tunable RF and analog circuits using on-chip MEMS passive components," *Digest of Technical Papers of the IEEE International Solid State Circuits Conference*, pp. 390-391, February 2005.

[11] D. Saias, S. Boret, P. Robert, C. Billard, P.-L. Charvet, G. Bouche, B. Diem, J.-B. Quoirin, P. Berruyer, M. Laurens, J.-C. Grasset, M. Aid, D. Belot, and P. Ancey, "An above-IC RF-MEMS switch," *Digest of Technical Papers of the IEEE International Solid State Circuits Conference*, pp. 206-207, February 2003.

[12] E.-C. Park and E. Yoon, "A 13 GHz CMOS distributed oscillator using MEMS coupled transmission lines for low phase noise," *Digest of Technical Papers of the IEEE International Solid State Circuits Conference*, pp. 300-301, February 2004.

[13] P. Melvas et al., "A surface-micromachined resonant-beam pressure-sensing structure," *Journal of Microelectromechanical Systems*, vol. 10, iss. 4, pp. 498-502, Dec. 2001.

[14] P.J. French, "MEMS/MOEMS technology capabilities and trends," *MEMS and MOEMS Technology and Applications*, SPIE Press, Bellingham, USA, pp. 1-40, 2000.

[15] W.P. Eaton and J.H. Smith, "Micromachined pressure sensors: review and recent developments," *Smart Mater. Struct.*, vol. 6, pp. 530–539, 1997.

[16] P. K. Weng and J-S. Shie, "Micro-Pirani vacuum gauge," *Review of Scientific Instruments*, vol. 65, Feb. 1994.

[17] C. J. Welham, J. W. Gardner, and J. Greenwood, "A laterally driven micromachined resonant pressure sensor," *Sensors and Actuators A: Physical,* vol. 52, pp. 86-91, 1996.

[18] K. Petersen, F. Pourahmadi, J. Brown, P. Parsons, M. Skinner, and J. Tudor, "Resonant beam pressure sensor fabricated with silicon fusion bonding," in *Solid-State Sensors and Actuators, Digest of Technical Papers, TRANSDUCERS*, 1991, pp. 664-667, 1991.

[19] F. Shangchun and L. Man Hyung, "The frequency characteristics of the beam resonator of the thermal excited silicon resonant pressure sensor," in *Proc. of the Advanced Intelligent Mechatronics*, vol.1, pp. 460-464, 2003.

[20] "Multi-Degree-of-Freedom Simulation of Micro-machined Sensor under mixed signal control," *ASME International Mechanical Engineering Congress and Exposition*, Boston, Massachusetts, USA, Nov. 2008.

[21] J. W. Judy, "Microelectromechanical systems (MEMS): fabrication, design and applications," *Smart Mater. Struct.*, vol. 10, pp. 1115-1134, 2001.

[22] C. C. Painter and A. M. Shkel, "Active structural error suppression in MEMS vibratory rate integrating gyroscopes," *Sensors Journal*, vol. 3, iss. 5, pp. 595-606, Oct. 2003.

[23] T. K. Tsang, M. N. El-Gamal, W. S. Best, and H. J. De Los Santos, "Wide tuning range RF-MEMS varactors fabricated using the PolyMUMPS foundry," *Microwave Journal*, pp.22-44, August 2003.

[24] J. Edward and L. Zhou, "Nonlinear effects in varactor-tuned resonators," *Trans. on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 53, iss. 5, pp. 853-861, 2006.

[25] I. Zine-El-Abidine, M. Okoniewski and J. G. McRory, "RF MEMS tunable inductor using bimorph microactuators," *Proc. of Int. Conf. on MEMS, NANO and Smart Systems*, pp. 436-437, July 2005.

[26] J. Oberhammer and G. Stemme, "Low-voltage high-isolation DC-to-RF MEMS switch based on an S-shaped film actuator," *IEEE Trans. on Electron Devices*, vol 51, iss 1, pp. 149-155, Jan. 2004.

[27] F. Nabki, T. A. Dusatko, and M. N. El-Gamal, "Frequency tunable silicon carbide resonators for MEMS above IC," *Proceedings of the Custom Integrated Circuits Conference*, pp. 185-188, September 2008.

[28] Y.-C. Lin, J.-C. Chiou, W.-T. Lin, Y.-J. Lin and S.-D. Wu, "The design and assembly of surface-micromachined optical switch for optical add/drop

multiplexer application," IEEE Trans. on Advanced Packaging, vol. 26, iss. 3, pp. 261-267, Aug. 2003.

[29] P. R. Choudhury et al., "MEMS and MOEMS Technology and Applications," SPIE Press, Bellingham, USA, 2000.

[30] G. M. Rebeiz, "RF MEMS: theory, design and technology," *John Wiley and Sons*, 2003.

[31] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2001.

[32] F. Nabki, T. Dusatko and M. N. El-Gamal, "Microelectromechanical Resonators for RF Applications," Emerging Wireless Technologies: Circuits, Systems and Devices, CRC Press/Taylor & Francis, pp. 591-629, 2007.

[33] F. Nabki, K. Allidina, F. Ahmad, P.-V. Cicek and M. N. El-Gamal, "A highly integrated 1.8 GHz frequency synthesizer based on a MEMS resonator," *IEEE Journal of Solid-State Circuits*, accepted, 2009.

[34] C. Zhang, G. Xu and Q. Jiang, "Characterization of the squeeze film damping effect on the quality factor of a microbeam resonator," *Journal of Micromechanics and microengineering*, vol. 4, iss. 10, pp. 1302-1306, 2004.

[35] F. Nabki, F. Ahmad, K. Allidina, and M. N. El-Gamal, "A compact and programmable high-frequency oscillator based on a MEMS resonator," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 337-340, September 2008.

[36] K. R. Williams et al., "Etch rates for micromachining processing-Part II," *Journal of Microelectromechanical Systems*, vol. 12, iss. 6, pp. 761-778, Dec. 2003.

[37] A. C. R Grayson et al., "A BioMEMS review: MEMS technology for physiologically integrated devices," *Proc. of the IEEE*, vol. 92, iss. 1, pp. 6-21, Jan. 2004.

[38] V. K. Varadan et al., "RF MEMS and their applications," John Wiley and Sons, 2003.

[39] S. F. Bart, "RF and optical packaging in telecommunications and other applications," *MEMS Packaging*, INSPEC IET, 2003.

[40] J. Oberhammer and G. Stemme, "Incrementally etched electrical feedthroughs for wafer-level transfer of glass lid packages," *Proc. Int. Conf. Solid-State Sens. Act. (Trans.)*, pp. 1832–1835, Boston, MA, 2003.

[41] Q. Wang et al., "Low temperature, wafer level Au-In bonding for ISM

packaging," *Int. Conf. Electr. Packaging Technology*, pp. 1-5, August 2006.

[42] J. Chae, J. Giachino and K. Najafi, "Fabrication and characterization of a wafer-level MEMS vacuum package with vertical feedthroughs," *J. MEMS*, vol. 17, no. 1, pp. 193–200, February 2008.

[43] T. F. Marinis, J. W. Soucy, J. G. Lawrence and M. M. Owens, "Wafer level vacuum packaging of MEMS sensors," *Conf. Electronic Components and Technology*, pp.1081-1088, Cambridge, MA, 2005.

[44] J. Mitchell, G. R. Lahiji and K. Najafi, "Encapsulation of vacuum sensors in a wafer level package using a gold-silicon eutectic," *Proc. Int. Conf. Solid-State Sens. Act. (Trans.)*, pp. 928-931, June 2005.

[45] A. Phommahaxay et al., "Via-free interconnection in quasi-hermetic wafer-level packaging for RF-MEMS applications and 3D integration," *Proc. Int. Conf. Solid-State Sens. Act. (Trans.)*, pp. 2063-2066, Lyon, France, June 2007.

[46] C. S. Premachandran, S. C. Chong, S. Liw and R. Nagarajan, "Design, fabrication and testing of wafer level vacuum package for MEMS device," *Conf. Electronic Components and Technology*, pp. 1136-1140, Singapore, 2006.

[47] H.-C. Chuang, D. Z. Anderson and V. M. Bright, "The fabrication of through-wafer interconnects in silicon substrates for ultra-high-vacuum atom-optics cells," *J. of Micromechanics and microengineering*, Boulder, CO, February 2008.

2 Description of the Technology

2.1 Features of the Technology

In this work, we propose a complete technology for hermetically packaging micro-electromechanical systems at the wafer level. Throughout this chapter, the cross-sectional diagrams follow the color legend shown in Figure 2-1.

Figure 2-1 : Color legend for process materials.

The process has the following features of interest:

1. *Vacuum encapsulation*: The developed process is capable of enclosing MEMS in sealed cavities at very low pressure, in order to improve the performance of various devices, e.g. beam resonators.

2. *Monolithic integration*: The technology is fully CMOS-compatible, in terms of processing temperature as well as material and chemical limitations, thus allowing the inclusion of both semiconductor devices and MEMS on the same silicon chip.

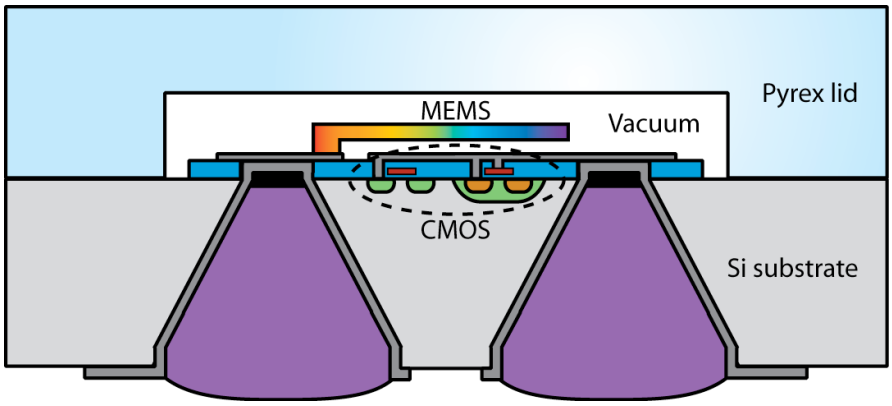

Figure 2-2 : WLP with CMOS/MEMS monolithic integration.

3. *Reduced electrical parasitic effects*: The use of vertical feedthrough interconnections through the thickness of the wafer results in lower electrical parasitic impedances than for the commonly used lateral interconnects, by lowering the routing complexity on the front of the wafer and connecting directly to the bonding pads. Furthermore, the packaged chip can be attached to a PCB by surface mounting, further reducing the parasitics compared to ordinary wire bonding.

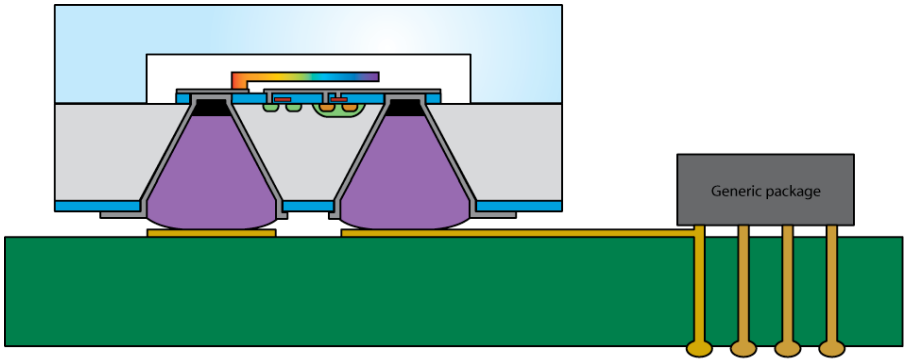

Figure 2-3 : Direct surface mounting of WLP chip on a PCB.

4. *MOEMS compatibility*: The encapsulated devices are optically accessible through the use of a transparent boro-silicate cover wafer. Since the electrical pads are on the backside of the device wafer (via transverse feedthrough interconnects), the chip can be surface mounted right side up, so that the devices are not cut off from optical signals.

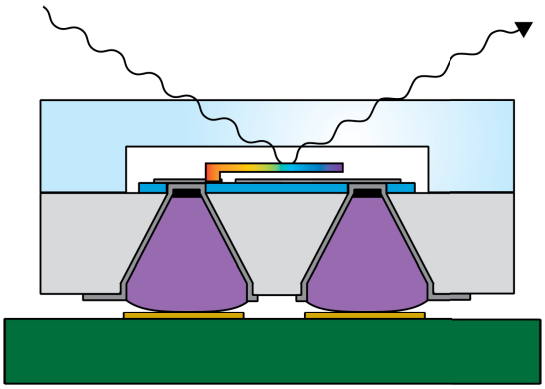

Figure 2-4 : WLP chip featuring optical accessibility.

In addition to the specific benefits just described, the technology presented here benefits from all the advantages usually associated with encapsulation at the wafer level, i.e. batch processing, enhanced device protection, improved electrical testability and reduced costs.

2.2 Process Flow

2.2.1 • Overview

The process flow of the proposed technology can be decomposed into four main stages:

1) A silicon wafer, *the active wafer*, which may hold previously fabricated CMOS devices, is pre-processed with transverse feedthrough interconnects to allow for electrical interfacing from the back of the substrate (Figure 2-5 (a)-(d)).

2) MEM devices are fabricated on the frontside of the substrate, utilizing a suitable surface micromachining process (Figure 2-5 (e)).

3) Cavities are etched in a Pyrex boro-silicate wafer, *the lid wafer*, and a getter is patterned inside the cavities if required (Figure 2-5 (f)).

4) The active and lid wafers are attached by anodic bonding, hermetically enclosing the MEM devices in vacuum as a result (Figure 2-5 (g)).

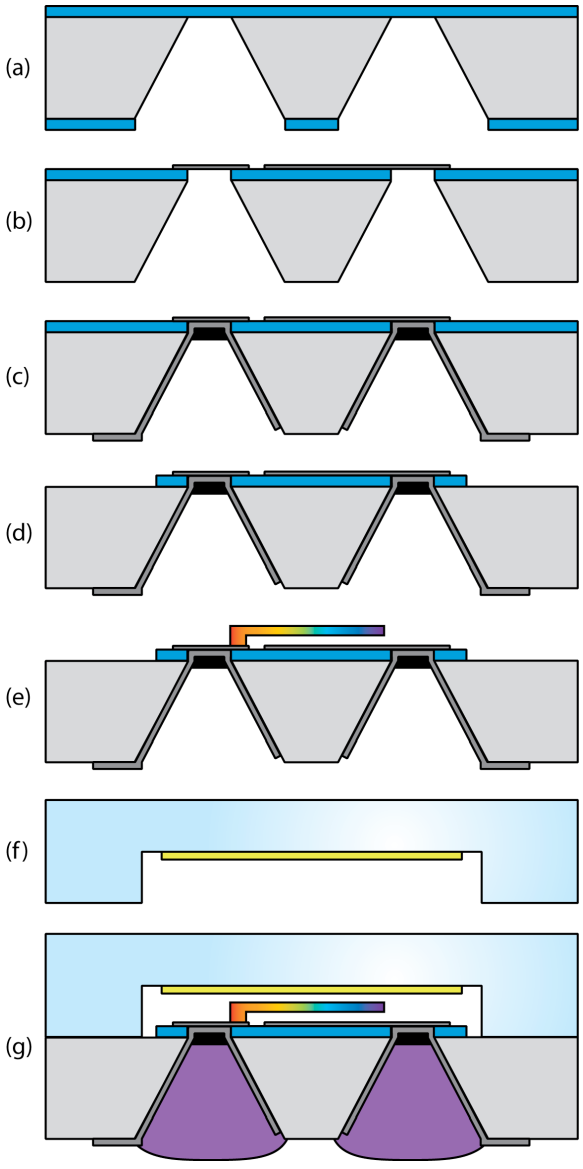

Figure 2-5 : Fabrication process flow.

2.2.2 • Description

We start with a six-inch single-side-polished silicon wafer of crystalline orientation <100>, since it represents the standard type of wafers used in CMOS semiconductor processes. The wafer may hold previously fabricated CMOS semiconductor devices on its frontside, e.g. transistors. If the wafer does not include CMOS electronics, we grow a 2.5 µm-thick layer of thermal silicon dioxide (SiO_2) on both sides using a thermal oxidation furnace, which will eventually serve as hardmasks for subsequent steps. However, if we are working with a CMOS wafer, the customary SiO_2 passivation layer will be used as hardmask on the frontside instead.

The first step is to create feedthroughs, which serve to electrically connect the devices on the frontside of the wafer to pads on the backside. Therefore, even though they are to be hermetically encapsulated, the MEMS will be electrically accessible from outside the cavity. We make these feedthroughs by bulk etching through the entire thickness of the silicon wafer, using tetramethylammonium hydroxide (TMAH), a wet anisotropic etchant that results in pyramidal holes with a 54.74° sidewall angle relative to the wafer surface [1].

Because etching through the entire thickness of a wafer with TMAH is considerably long (approximately 30 hours to go through a 675 µm-thick substrate), we need a strongly resistant hardmasking material. TMAH is highly selective to silicon oxide [2], hence the thermal SiO_2 that was grown earlier on both sides of the active wafer. We pattern this SiO_2 by reactive ion etching (RIE) using a mixture of CHF_3, CF_4 and Ar gases, opening windows at the desired feedthrough locations. Eventual devices on the front of the wafer need to be precisely aligned with the feedthroughs, hence TMAH must not be allowed to affect the lithographical alignment marks formed in the SiO_2 on the backside of the wafer. We achieve this by preserving a thinned-down SiO_2 layer on the alignment marks, which shields them from TMAH, while making them visible for future use.

Once the hardmask is complete, we place the wafer in TMAH for the appropriate duration (Figure 2-5 (a)). The very low etch rate of TMAH on SiO_2 circumvents the issue

of timing, since the bulk etching is stopped by the frontside SiO_2 layer, forming as a result a 2.5 µm-thick SiO_2 membrane diaphragm at the frontside extremity of the feedthrough.

Subsequently, to produce the electrical interconnect wires on the frontside of the wafer, we DC sputter 200 nm of aluminum, and pattern it by wet etching with a phosphoric-acetic-nitric (PAN) solution. The layer must ensure complete coverage of the diaphragm membranes, so that we can next remove the backside SiO_2 by RIE, with CHF_3, CF_4 and Ar, resulting in membranes composed solely of aluminum at this stage (Figure 2-5 (b)).

To form an electrical contact to these conducting membranes, we DC sputter and wet pattern 1 µm of Al on the back of the wafer (PAN etch), resulting in thicker 1.2 µm aluminum membranes, and in a metallic interconnection from the membranes to the backside of the feedthroughs.

For structural reinforcement and hermeticity improvement of the membranes, we DC sputter a 2 µm-thick layer of amorphous silicon carbide (*a*-SiC) on the backside of the wafer, due to the very desirable mechanical and tribological properties of that material [2]. To pattern this SiC, we DC sputter on top of it a temporary chromium (Cr) hardmask, which is itself patterned by wet etching with CR-14. Thanks to the stronger protection offered by this hardmask, the exposed SiC can be removed by RIE using NF_3 plasma (Figure 2-5 (c)).

The regions of the wafer destined to come into contact with the lid wafer must first be freed of any material other than pure silicon, to achieve successful anodic bonding. Hence, in order to prepare the frontside of the wafer for bonding, we remove by RIE the SiO_2 on the frontside of the wafer using a plasma composed of CHF_3, CF_4 and Ar. However, SiO_2 is preserved as an electrical insulation layer in the close neighborhood of the MEM and CMOS devices, so as to minimize signal leakage through the substrate (Figure 2-5 (d)).

At this stage, we proceed with the fabrication of the desired MEMS using any suitable surface micromachining process, according to our particular needs. Once the MEMS are released, work on the active wafer is complete (Figure 2-5 (e)).

To finalize packaging, we must make cavities on another wafer, with the purpose of hermetically encapsulating the MEMS. We use RIE with SF_6 to pattern 6 μm-deep cavities on a Pyrex boro-silicate wafer [3]. To perform this etch, we use a Cr hardmask for enhanced selectivity compared to a photoresist mask. If high vacuum is a requirement, we can optionally deposit and pattern a getter material (e.g. barium) inside the cavities to counter eventual outgassing, which will otherwise cause the pressure to rise over time (Figure 2-5 (f)) [4].

In order to seal the MEMS inside hermetic cavities, we attach the silicon and Pyrex wafers together. To achieve this goal, we resort to anodic bonding, which ensures high bond strength at CMOS compatible temperatures [5]. We perform anodic bonding at 350°C, with an applied voltage of 600 V, and a minimal ambient pressure of 0.75 mTorr. If high vacuum is desired inside the cavities, we perform a lengthy degassing bake prior to bonding for evacuation of the potential outgassing agents on the wafers, e.g. polymers (Figure 2-5 (g)).

Once sealing is finalized, the feedthroughs are filled by soldering metal or electroplating to provide coarse mechanical reinforcement [6]. Subsequently, the individual chips are diced.

2.3 Photolithography and Alignment Considerations

2.3.1 • Preserving the Alignment Marks

The alignment marks on the back of the active wafer must be preserved after the TMAH bulk feedthrough etch because these need to be precisely aligned with the devices on the front of the wafer. In other words, two slightly different SiO_2 hardmask patterns need to be superimposed on the back of the active wafer. The first pattern defines the feedthrough openings as well as the alignment marks. Before soaking the wafer in

TMAH, the feedthrough openings must be free of all SiO_2, so as to expose the bulk Si to the etchant. However, the alignment mark regions must be covered by enough SiO_2 to sustain the complete TMAH etch, but less SiO_2 than the surrounding area for visibility. Hence, after a partial etch of the SiO_2 thickness with the pattern of the applied mask, a modified version of the same pattern is used to completely remove the SiO_2 at the feedthrough openings, while leaving the alignment mark SiO_2 unaffected.

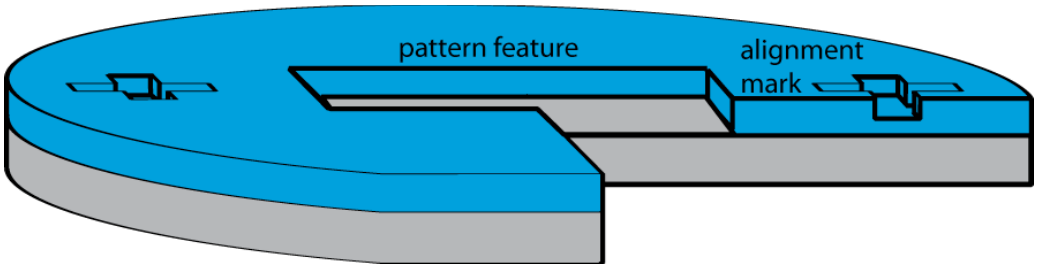

Figure 2-6 : Cross-section of the wafer showing the preserved alignment marks.

2.3.2 • Aligning Patterns with the Wafers

In this process, there are three different surfaces where alignment of lithographical masks is required for patterning: i) the front of the active wafer, where the MEM devices are built, ii) the back of the active wafer, where the feedthroughs and pads are made, and iii) the front of the lid wafer, where the encapsulation cavities are produced.

A challenging aspect of this process lies in that patterns on each of these three surfaces must be aligned together. In the following, we detail the procedures to ensure adequate alignment between patterns on the different sides of the same wafer and between different wafers.

The first concern is that the feedthrough mask on the back of the active wafer must be precisely aligned with the first device mask on the front of this same wafer, which is the first aluminum interconnect pattern in this case. Alignment ensures that the feedthrough contacts are properly connected electrically with the front circuitry and devices. We start by locating the alignment marks on the lithographical mask consisting of the first front layer using microscopes looking from underneath, and register the

position of the marks (Figure 2-7 (a)). Then, we find the alignment marks belonging to the feedthrough mask on the back of the wafer, again using the bottom microscopes (Figure 2-7 (b)), and we align them with the recorded position of the marks of the front mask (Figure 2-7 (c)). Once both patterns are properly aligned, we expose the front of the wafer through the mask (Figure 2-7 (d)). From then on, we can align every subsequent front mask to this first front pattern.

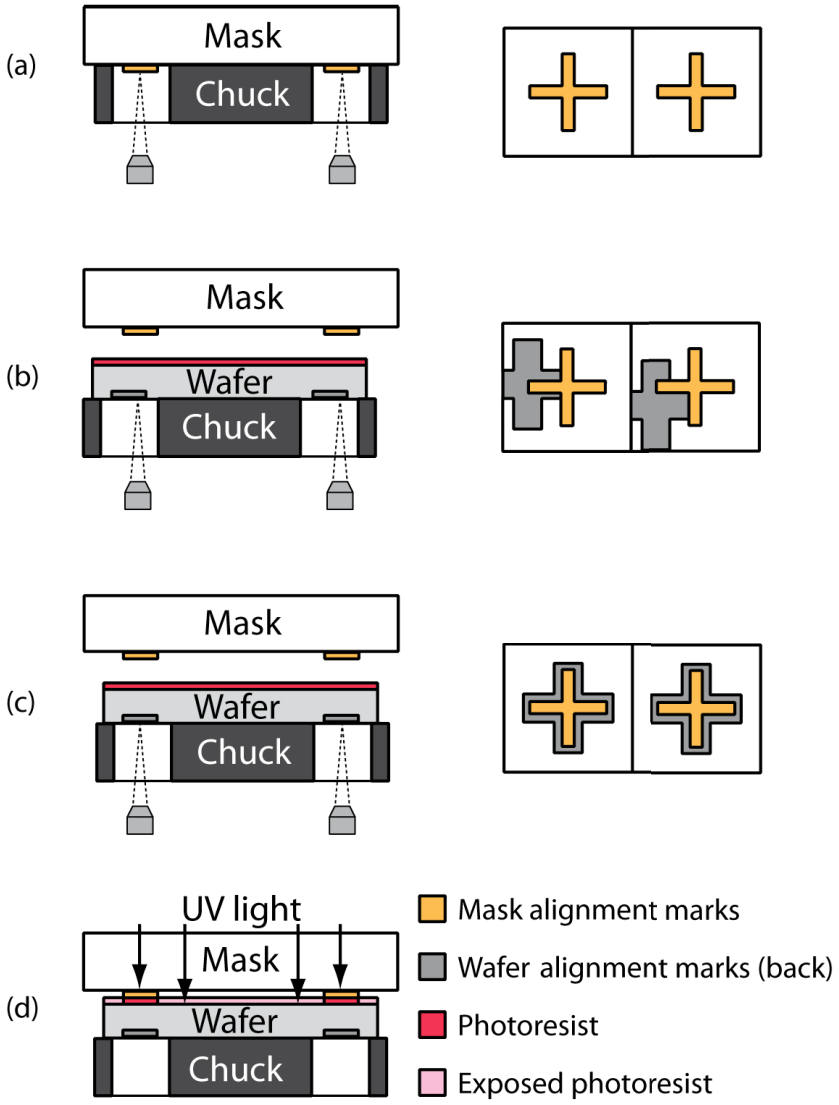

Figure 2-7 : Lithographic procedure for front-to-back alignment [1].

Equally important is that the masks on the active and lid wafers must be centered exactly the same way relatively to the edge of their respective wafer, with a tolerance of about half a millimeter. This is important so that there is no misalignment of the wafer edges when the wafers are bonded together with properly aligned patterns. To ensure matched centering, the microscopes are kept stationary between the patterning of the feedthroughs on the back of the active wafer and the patterning of the first mask on the front of the lid wafer (cavities). In each case, we adjust the mask position so that the alignment marks are placed right under the microscopes. The wafers are then inserted for exposure and left unmoved from the position of origin. This results in patterns that are similarly positioned with respect to the edge of both wafers. Wafer misalignment is illustrated in Figure 2-8.

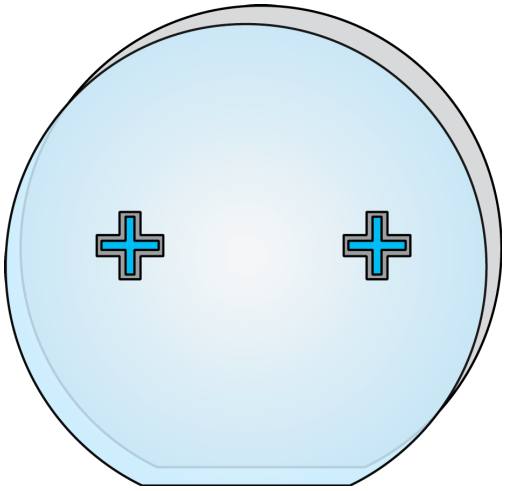

Figure 2-8 : Incorrectly centered patterns on wafers resulting in misaligned wafers.

2.3.3 • Adjusting the Position of the Wafers for Bonding

During wafer bonding, vacuum is created inside the process chamber before the wafers are brought into contact, so that a low-pressure can be preserved inside the cavities after encapsulation. In preparation for bonding, the wafers are aligned (Figure 2-9 (a)-(c)) and clamped on a bonding chuck (Figure 2-9 (d)). This chuck holds the aligned wafers with a slight separation, with help from three built-in separation flags.

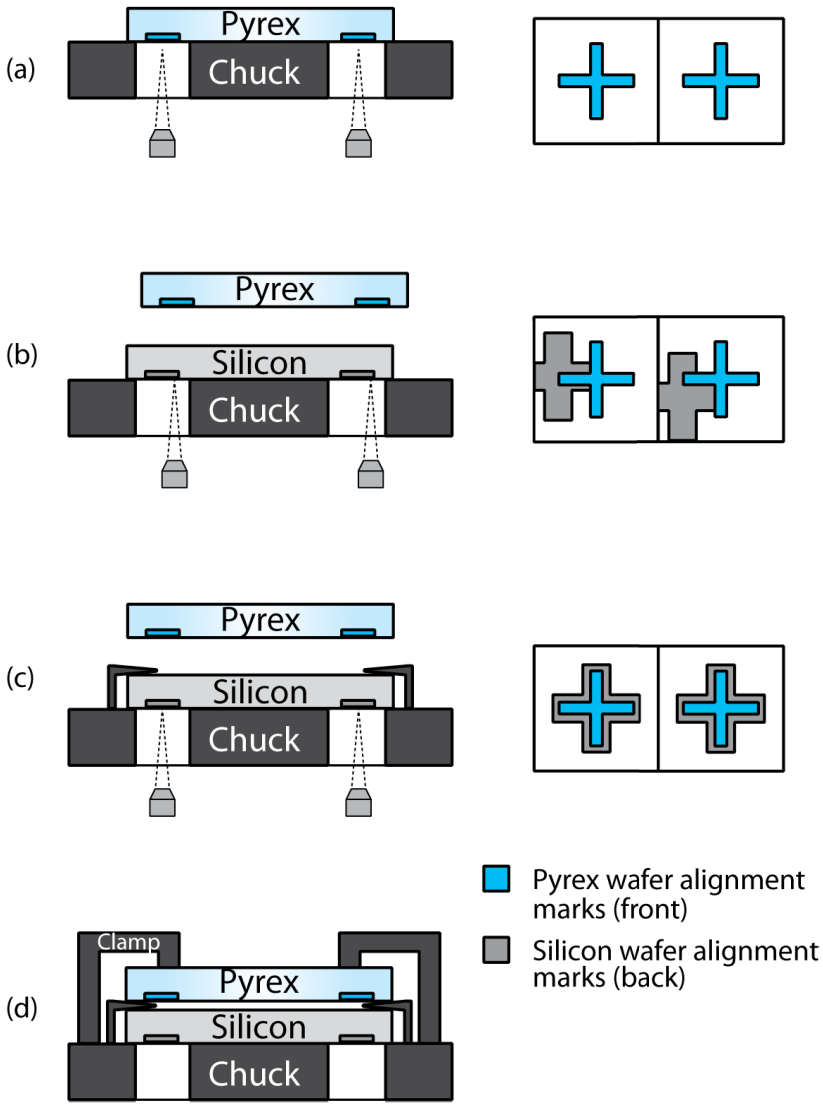

Figure 2-9 : Wafer alignment procedure prior to bonding [1].

Wafers must not only be well aligned together but also adequately centered on the chuck. This ensures that the three flags are equally inserted at the wafer interface, as shown in Figure 2-10, so that they can be withdrawn with success prior to bonding.

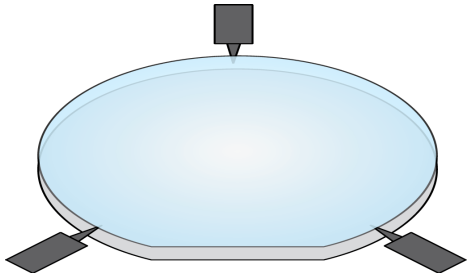

Figure 2-10 : Separation flags properly placed between the two wafers.

2.3.4 • Spray Coating Photoresist

There exist two distinct methods for photoresist application: spin coating and spray coating. In spin coating, a viscous liquid solution of photoresist is dispensed on the wafer, which is then spun rapidly, forming a very uniform layer of resist. In spray coating, the resist is rather sprayed onto the wafer, allowing for a more conformal layer, suitable for covering high aspect ratio geometries.

Since spin coating is the standard and simplest method for applying photoresist, it was utilized during the initial development of the process. However, when patterning the back of the active wafer, due to the high aspect ratios involved, the conformality of the resist inside the feedthroughs was unsatisfactory, and the formation of large streaks prevented further processing. To alleviate these issues, the spinning speed was reduced, but resulted in thick bumps of resist near the feedthroughs, which spoiled the pattern. Furthermore, with the spin coater utilized, the wafer is held in place by vacuum suction. Between the two steps of bulk etching, i.e. the formation of the feedthroughs, and the reinforcement of the membranes with SiC, the thin diaphragm membranes are very fragile and some can break under the influence of the vacuum suction. When this happens, photoresist can pass through the feedthrough to the other side of the wafer and disrupt the pattern.

After extensive optimization of the spin coating, the results were still unsatisfactory. Therefore, we decided to use spray coating throughout the process, which is better suited for high aspect ratio features. Furthermore, in the coater used, the wafers are not held by vacuum but rather mechanically, which prevents membrane rupture.

2.4 Wafer Bonding Considerations

2.4.1 • Altering the Order of the Process Sequence

In earlier versions of the process, bonding was performed before TMAH bulk etching of the feedthroughs. However, with that sequence of steps, we observed that TMAH infiltrated the bonding interface and deteriorated the bond. It was necessary to

somehow modify the process to solve this problem. Therefore, we considered three different options:

i) *Use a seal ring to prevent the TMAH from infiltrating the bond interface from the sides of the wafer.* This was not implemented because TMAH could still reach the bond interface in the case of one of the membranes being ruptured, allowing the etchant through the opening.

ii) *Use an alternative etching method to make the feedthroughs, so as to avoid placing the bonded wafers in a wet etchant.* This was not implemented because deep reactive-ion etching (DRIE), the only viable alternative for etching through the complete thickness of a silicon wafer, was not available within our facilities.

iii) *Modify the process sequence so that feedthrough etching is performed before anodic bonding.* We decided to use this option because it allows performing wafer bonding as one of the last steps in the process sequence, thus eliminating the need of placing the bonded wafers in TMAH.

2.4.2 • Changing the Wafer Bonding Method

In the first iterations of the process, wafer attachment was performed by direct silicon-to-silicon bonding, due to the simplicity of using two silicon wafers instead of different types. However, because of the low temperature budget dictated by CMOS compatibility, direct bondings were observed to exhibit unbonded voids and unsatisfactory bonding strength. To achieve stronger bonds at desired CMOS-compatible temperatures, we decided to use anodic bonding of the silicon active wafer with a Pyrex lid wafer [5]. This bond is much stronger than silicon direct bonding at the selected temperatures and has the additional advantage of providing optical accessibility for MOEMS devices through the Pyrex lid.

2.4.3 • Adapting the Pre-Bond Cleaning Procedure

Cleaning the wafers before wafer bonding is crucial to prevent dust particles and other contaminants from disrupting the quality and strength of the bond. The typical

cleaning sequence can be divided into four main steps: solvent clean, RCA1, hydrofluoric acid (HF) dip and RCA2 [5].

The purpose of solvent cleaning is to remove oil and organic residues from the surfaces to bond. The wafer is soaked in acetone, followed by isopropyl alcohol (IPA) for degreasing. To enhance efficiency, the beakers containing the solvents can be placed in the ultrasonic bath. Unfortunately, the ultrasonic vibrations can potentially damage the thin diaphragm membranes as well as the MEM devices. Therefore, the ultrasonic bath cannot be used for the active wafer.

The RCA1 clean is also used to remove organic residues from silicon wafers. The solution used is a mix of hydrogen peroxide (H_2O_2), ammonium hydroxide (NH_4OH) and deionized water. Unfortunately, this clean was found to attack aluminum, which is present on the active wafer. Therefore, this clean cannot be used for the active wafer. As for the Pyrex lid wafer, the more aggressive piranha solution is used instead of RCA1 to remove the organic residues. The piranha solution is made from a mix of concentrated sulfuric acid (H_2SO_4) and H_2O_2.

The HF dip serves to remove the native SiO_2 on a silicon wafer so as to encourage bonding. Since HF attacks aluminum, which is present on the silicon active wafer, and since there is no native oxide on a Pyrex wafer, the HF dip cannot be used for the purposes of this process.

The RCA2 clean is used to remove metallic ions on the wafers to be bonded. The chemicals involved are H_2O_2, hydrochloric acid (HCl) and water. Since metals are present on the active wafer, and since we do not wish to remove them, this clean is not used.

In summary, only a solvent clean without ultrasonic activation can be performed on the active wafer. On the lid wafer, we perform solvent clean with ultrasonic activation as well as a piranha clean. Because we carry out many process steps on the wafers before bonding, but few of the typical cleaning steps can be performed, all manipulations prior

to bonding must be performed with extreme care, in order to minimize contamination and scratching of the wafers.

2.4.4 • Removing SiO_2 Before Anodic Bonding

Successful anodic bonding of the wafers requires the removal of SiO_2 on the front of the active wafer. This is performed by RIE. Because we wish to preserve SiO_2 in the vicinity of the electronic and MEM devices for electrical insulation, certain areas of the wafer must be protected from this RIE by a chromium mask. SiO_2 must however be removed from all other areas on the active wafer, which will come into contact with the lid wafer to make the bond.

Since bonding requires a highly smooth surface for success, we aim to minimize roughing the silicon surface of the active wafer caused at the end of the SiO_2 RIE. Hence, we adjust the RIE etching to become progressively milder when approaching the final nanometers of the SiO_2 layer. This way, the RIE has much less impact on the roughness of the silicon surface, thereby improving the quality of the bond.

2.4.5 • Protecting the Front of the Active Wafer

Many steps in the process require the active wafer to be placed face down on a working surface. To avoid scratching of the wafer during these manipulations, which could compromise the quality of wafer bonding, we apply a temporary protective photoresist layer on the front of the active wafer whenever possible in the process sequence.

2.5 Material and Structural Considerations

2.5.1 • Minimizing Chromium Residual Stress

Chromium is used temporarily for either hardmasking or barrier purposes at various stages in the process, e.g. when etching silicon carbide. Even though this chromium stays on the wafer only temporarily, if its residual stress is too high, it can

adversely affect the underlying layer by causing peeling. Therefore, we work to optimize the deposition process parameters of this film in order to minimize its stress.

2.5.2 • Protecting the Aluminum from RIE of SiO_2

The RIE recipe used to etch SiO_2 has a significant etch rate on aluminum. Therefore, when clearing the SiO_2 layer on the front of the active wafer for bonding, we must ensure to protect the aluminum of the interconnects and the membranes. To provide this protection, we use a temporary chromium hardmask.

2.5.3 • Masking the Lid Wafer for RIE

In order to etch relatively deep (6 μm) micro-cavities into the Pyrex lid wafer by RIE, we use SF_6 plasma for a prolonged period of about 30 minutes [3]. Due to the high strength and length of the recipe, a simple photoresist mask can not withstand the etching. Hence, we use chromium as a hardmask, since it is not attacked substantially by the etching recipe devised.

However, such a prolonged etch time does affect the surface of the chromium mask by hardening it and making it very difficult to remove by wet etching only. Therefore, before wet etching, we use O_2 plasma to help remove the hardened surface of the chromium layer.

2.6 References

[1] W. Sonphao and S. Chaisirikul, "Silicon anisotropic etching of TMAH solution," *Proc. IEEE Int. Symp. on Industrial Electronics*, vol. 3, pp. 2049–2052, June 2001.

[2] K. R. Williams et al., “Etch rates for micromachining processing-Part II,” *Journal of Microelectromechanical Systems*, vol. 12, iss. 6, pp. 761-778, Dec. 2003.

[3] X. Li, T. Abe, and M. Esashi, “Deep reactive ion etching of pyrex glass using SF6 plasma,” *Sensors and Actuators A:Physical*, vol. 87, no. 3, pp. 139-145, Jan. 2001.

[4] D. Sparks, S. Massoud-Ansari and N. Najafi, “Reliable vacuum packaging using NanoGetters and glass frit bonding,” *Proc. of SPIE*, vol. 5343, pp. 70-78, Jan. 2004.

[5] T. R. Hsu and J. Clatterbaugh, “Joining and bonding technologies,” *MEMS Packaging*, INSPEC IET, 2003.

[6] J. Chae, J. Giachino and K. Najafi, "Fabrication and characterization of a wafer-level MEMS vacuum package with vertical feedthroughs," *J. MEMS*, vol. 17, no. 1, pp. 193–200, Feb. 2008.

[7] M. Madou, “Fundamentals of Microfabrication”, CRC Press LLC, Florida, USA, 1997.

3 Results and Analysis

3.1 Transverse Feedthroughs

3.1.1 • Fundamentals of Wet Anisotropic Etching

In this technology, we use TMAH wet anisotropic etching to form transverse feedthroughs traversing the whole thickness of the active wafer. With wet anisotropic etching, the etch rate is much faster in certain directions than in others, exposing the slowest etching crystal planes as etch time progresses, usually the <111> planes in the case of silicon [1]. For CMOS and MEMS, the most widely used type of wafer has the <100> crystalline orientation. On such a wafer, with a square pattern defined by a SiO_2 hardmask, TMAH etches pyramidal holes into the bulk silicon with a sidewall angle of 54.74°, as illustrated in Figure 3-1.

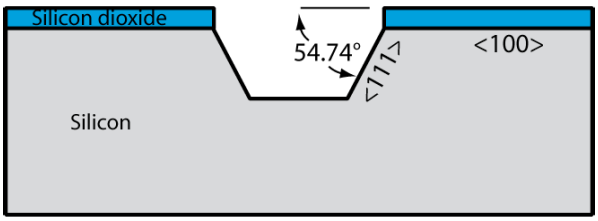

Figure 3-1 : TMAH etching of <100> silicon [1].

The measured etch rate of silicon in 25% TMAH at 85°C is about 25 μm/min, whereas SiO_2 is attacked at about 1 nm/min, hence the use of SiO_2 as an effective hardmask [2].

3.1.2 • Design of the Shape of the Feedthroughs

The shape of the transverse feedthroughs is an important consideration. Having a working metallic electrical connection all the way to the sealing membranes would present a considerable challenge if feedthroughs were too narrow. Conversely, if they were too wide, the sealing membranes would be excessively large, rendering them

mechanically weaker. Therefore, the transverse feedthrough must ideally be wide at the opening, i.e. at the interface to the PCB, but narrow closer to the sealing membrane. This simultaneously allows for an effective interconnection interface and a sturdy sealing membrane. To achieve this goal, TMAH, modified so that it is CMOS-compatible, as detailed in [3], is selected to etch the feedthroughs anisotropically with the desired pyramidal profile.

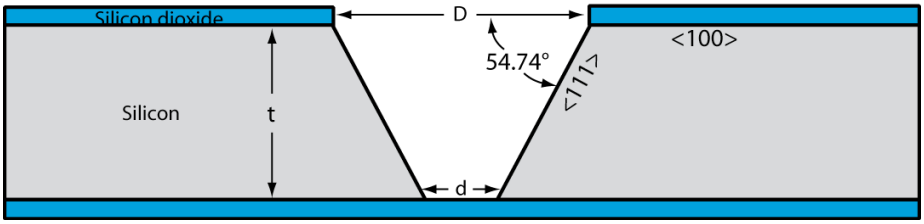

Figure 3-2 : Dimensions for TMAH etching <100> silicon.

Referring to Figure 3-2, for a Si wafer of thickness t and an SiO_2 hardmask square opening width D on one side of the wafer, the expected width d of the ensuing oxide membrane on the other side of the wafer can be computed using

$$d = D - \frac{2t}{\tan(54.7°)}. \tag{3.1}$$

3.1.3 • Inspection of the Fabricated Feedthroughs

To verify the behavior of TMAH experimentally, we made transverse feedthroughs with various hardmask opening sizes D, as outlined in Table 3-1. One immediately notices that the measured membrane widths d are all larger than theoretically expected from (3.1). This is caused by the progressive enlargement of the hardmask opening through the action of TMAH.

Table 3-1 : Measured dimensions with TMAH etching.

Initial Hardmask Width *D* (µm)	Final Hardmask Width *D* (µm)	Membrane Width *d*	
		Theory (µm)	Measured (µm)
900	1023	not reached	not reached
950	1074	not reached	87
1000	1120	44	183
1050	1187	94	211
1100	1234	144	270
1150	1281	194	312
1200	1316	244	392

According to theory, the membrane for a 675 µm-thick wafer with an initial square hardmask opening of 100 µm on the back of the wafer should have a width *d* of about 44 µm, while the measured width is 183 µm, as illustrated on Figure 3-3.

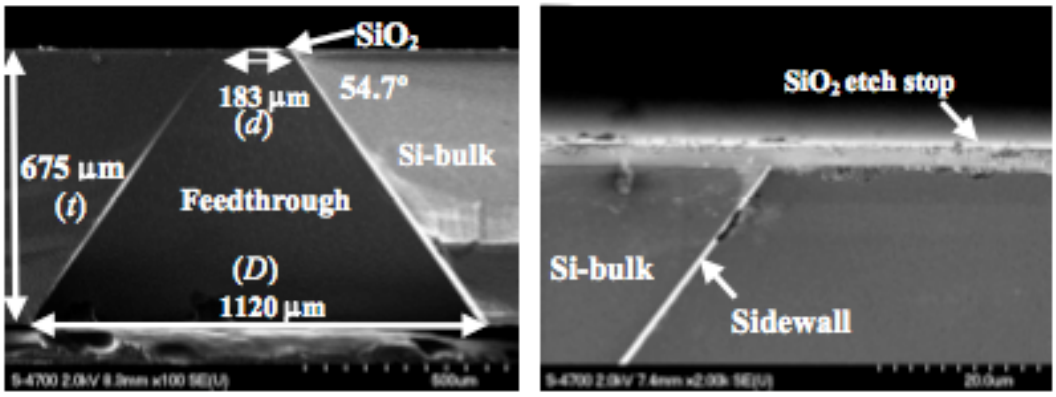

Figure 3-3 : SEM cross-section of feedthrough, overall (left) and close-up (right).

3.1.4 • Electrical Conductivity of the Feedthrough Contacts

As discussed earlier, in order to provide an electrical contact by means of the transverse feedthrough, aluminum is sputtered on the frontside over the SiO_2 etch stop membrane, and the SiO_2 is then etched away from the backside. Al is then sputtered on the backside, forming a connection with the front Al. The parasitic resistance of a single feedthrough is measured to be 0.69 ± 0.23 Ω before solder ball filling. Since the processed chips are directly surface-mountable, reduced parasitics are expected, compared to conventional packaging solutions.

3.2 Sealing Membranes

3.2.1 • Stress Compensation of the Sealing Membranes

When vacuum is established inside the cavities by wafer bonding, the sealing membranes must mechanically withstand a significant pressure difference. Hence, we use low-stress amorphous silicon carbide to reinforce the membranes. SiC has very desirable mechanical and tribological properties in comparison to other materials accessible in a microfabrication environment [4]-[10], while its potential for successful vacuum sealing has already been demonstrated in [11]. Figure 3-4 shows that the overall residual stress of

the membranes can be minimized by tuning the ambient argon (Ar) gas pressure during a-SiC DC sputtering. The residual stresses were obtained through a thin film wafer curvature measurement system. For an Ar pressure of 4.1 mTorr, the stress of the SiC layer is optimized so as to compensate for the high tensile stress of the Al. This results in an important improvement in the membrane structural resistance to applied pressures.

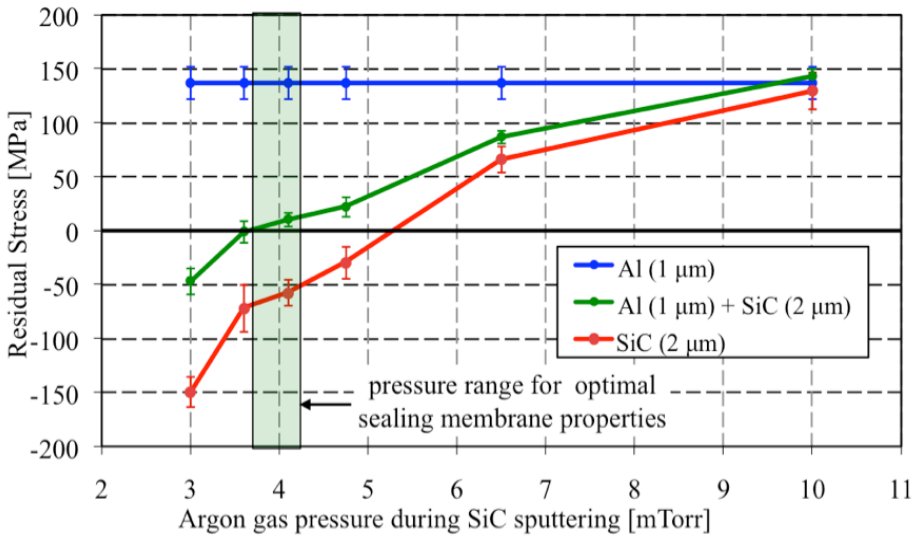

Figure 3-4 : Residual stress of the sealing membrane constituent materials.

Figure 3-5 displays pictures of the sealing membrane at different stages of the process flow. When the membranes are first composed only of SiO_2, they exhibit significant compressive stress, as can be observed from its plaited appearance indicative of buckling (Figure 3-5 (a)). In contrast, when the membrane is composed solely of Al (after SiO_2 removal), it has a highly tensile stress, indicated by a very taut surface (Figure 3-5 (b)). The shape of an optimized membrane composed of Al and SiC shows that its stress is properly balanced, as no significant warping is observed (Figure 3-5 (c)).

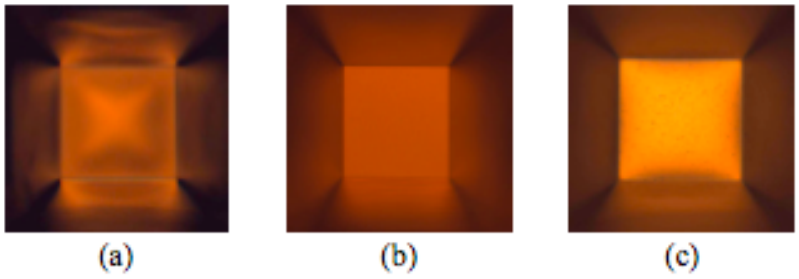

Figure 3-5 : Membrane (a) before SiO_2 removal, (b) after back Al sputter, (c) after back SiC sputter.

Figure 3-6 shows a scanning-electron microscope (SEM) cross-section at the edge of the SiC-reinforced diaphragm, where the membrane is composed of a stack of two conductive layers of aluminum and one structural layer of SiC.

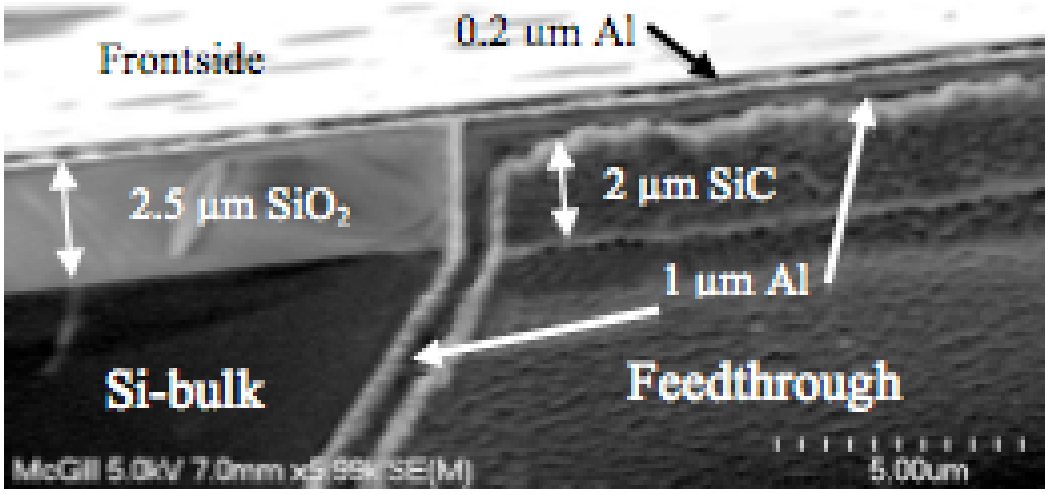

Figure 3-6 : SEM cross-section of a SiC reinforced sealing membrane.

3.2.2 • Vacuum Confirmation by Membrane Deflection

With the hermetic sealing procedure, a low-pressure environment is established inside the encapsulation micro-cavities. When the samples are brought out of the bonding chamber in a room-pressure environment, the vacuum is retained inside by the sealing diaphragm membranes. Due to the pressure difference between the sealed environment and the room, a force is exerted on the membranes, causing a deflection, as shown on Figure 3-7.

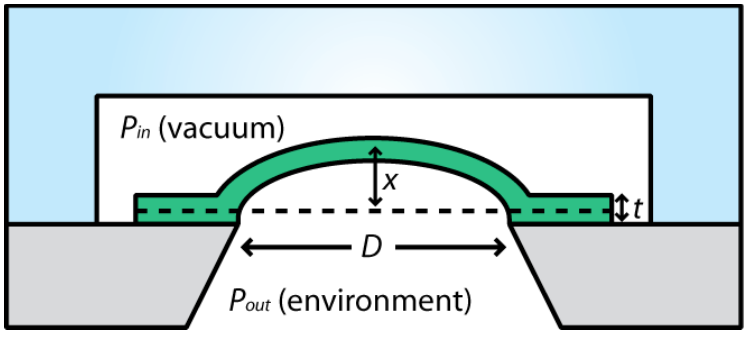

Figure 3-7 : Membrane deflection caused by a pressure difference.

We can calculate the deflection displacement x by (3.2), where k is a material constant, D is the diameter of the square membrane, t is the thickness of the membrane, P_{in} is the pressure inside the cavity and P_{out} is the environing pressure:

$$x = \frac{kD^4}{t^3}\left(P_{out} - P_{in}\right) \text{ [12].} \tag{3.2}$$

From the diaphragm deflection displacement, the actual level of vacuum in the sealed cavities can be estimated using

$$P_{in} = P_{out} - \frac{t^3}{kD^4}x\,. \tag{3.3}$$

Evidently, this method gives only a coarse approximation of the pressure difference, but is sufficient to determine whether vacuum encapsulation is generally successful or not. Alternatively, when we assume that the internal pressure is very low (close to zero), we expect to observe a membrane deflection displacement x_{exp} given by:

$$x_{\exp} \approx \frac{kD^4}{t^3}P_{out}\,. \tag{3.4}$$

Using an optical profiler or a simple optical microscope, the actual deflection of the membranes can be measured and compared with the expected value, so as to determine whether vacuum is indeed successfully enclosed.

3.3 Wafer Bonding

In this technology, wafer bonding is instrumental in hermetically sealing the MEMS under vacuum in micro-cavities. To ensure general compatibility with most CMOS and MEMS processes, the encapsulation methodology must be performed at low enough temperatures. For a common maximum processing temperature of 400°C, we compared the characteristics of Si-Si direct bonding and Si-Pyrex anodic bonding. These

bonding methods are the only two low-temperature options that require neither adhesive nor intermediary layers.

We can evaluate the quality of a wafer bond from i) *the bond surface energy*, quantifying the force binding the wafers together, and ii) *the void density*, conveying the bond uniformity at the interface between the wafers. The crack test technique introduced in [13] is used here to calculate the bond surface energy, as illustrated in Figure 3-8.

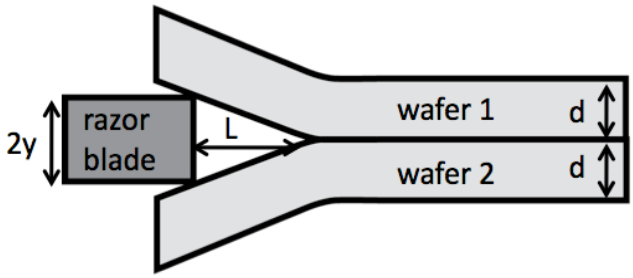

Figure 3-8 : The razor blade crack test technique.

Indeed, we insert a thin razor blade of thickness *2y* between the two bonded wafers, each with thickness *d* and Young's modulus *E*. We measure *L*, the length of the resulting crack, by observation under an infrared (IR) camera, so as to obtain the bond surface energy,

$$\gamma = \frac{2Ed^3y^2}{32L^4}. \tag{3.5}$$

As for the void density, we can evaluate its magnitude by simple inspection, because voids at the bond interface appear very clearly under the IR camera.

3.3.1 • Silicon Direct Bonding

We investigated the possibility of using a silicon wafer as the lid for encapsulation, which entails the utilization of silicon direct bonding for wafer attachment [14]. Silicon direct bonding is performed by means of an hydration process, where both wafers are inserted into a solution of H_2SO_4 and H_2O_2, so that silanol bonds, composed of oxygen (O) and hydrogen (H), can join with the silicon atoms of each wafer (Figure 3-9).

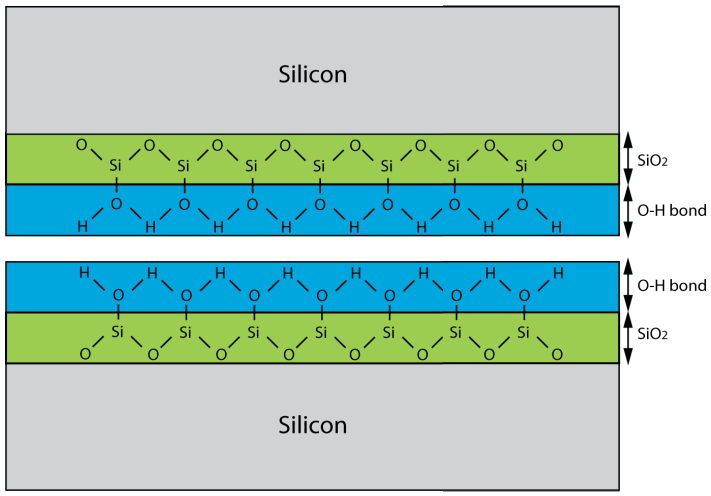

Figure 3-9 : Hydrated silicon wafers.

When the wafers are brought together, dehydration occurs, resulting in the liberation of water vapor. Meanwhile, the excess oxygen remains at the bond interface, forming a chemical bond between the two wafer surfaces (Figure 3-10).

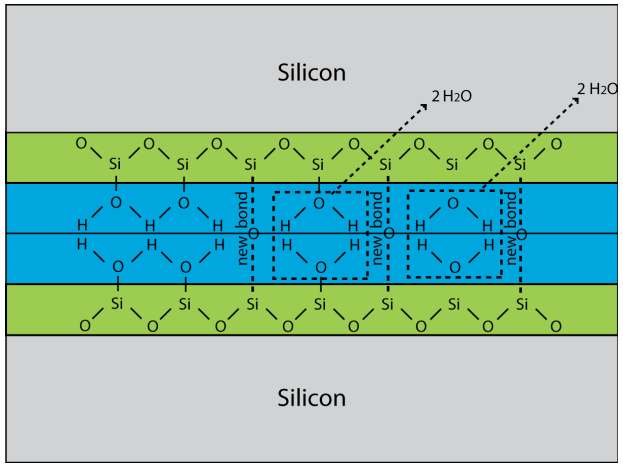

Figure 3-10 : Dehydration and creation of silanol bonds.

High-temperature annealing is essential for improving the strength of the bond by further liberating water vapor, thus increasing the quantity of Si-O-Si chemical bonds (Figure 3-11).

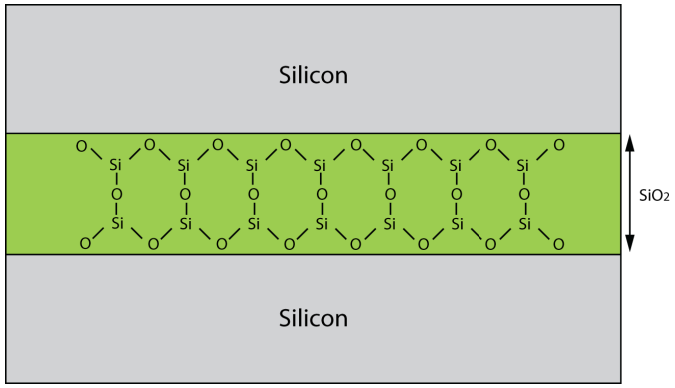

Figure 3-11 : High-temperature annealing.

For successful bonding, the surface of the wafers must be both very flat and very smooth. Indeed, the root-mean-square (RMS) roughness of each surface must be less than 4 nm for satisfactory bonding [14].

As a test, we joined two silicon wafers by silicon direct bonding, with a maximum annealing temperature budget of 400°C. To evaluate the quality of the bond, we performed a crack test and a void examination, repeated for 20 iterations. As illustrated on Figure 3-12 with a representative case, and using (3.5), the crack test yielded a bond surface energy of 0.118 J / m^2.

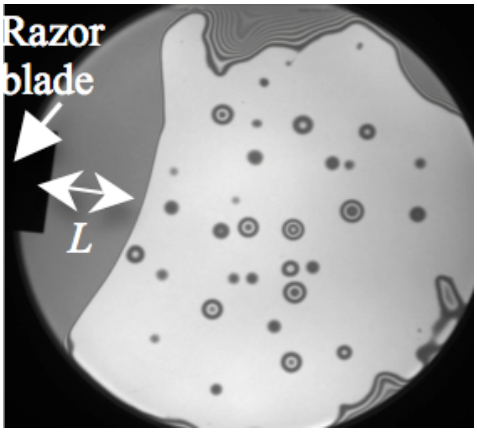

Figure 3-12 : Crack test performed on Si-Si direct bonded wafers.

Figure 3-13 shows the void density as observed under the IR camera for this same representative silicon direct bonding test case. One can easily observe that the density of voids is highly unsatisfactory.

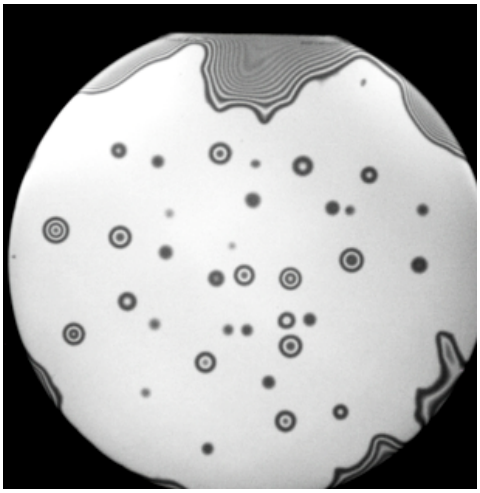

Figure 3-13 : Voids at the bond interface of Si-Si direct bonded wafers.

3.3.2 • Anodic Bonding

Anodic bonding has been shown to provide reliable hermetic sealing [14], which is a prime requirement for enclosing MEMS in high vacuum. Its main advantage over silicon direct bonding is that significantly lower temperatures are needed for similarly strong bonds, i.e. 180°C to 400°C versus over 700°C. Lower bonding temperatures allow for CMOS compatibility and also result in lower risk of residual stress due to thermal mismatch, which could eventually lead to wafers cracking in extreme cases. Another notable advantage of anodic bonding is that the surface flatness requirement is much less stringent, with an RMS roughness of 1µm as opposed to 4 nm for silicon direct bonding.

In this case, we investigate the anodic bond of a Pyrex 7740 wafer to a silicon wafer, but anodic bonding can also be used to bond diverse materials such as glass-to-glass, glass-to-metal, silicon-to-silicon and GaAs-to-silicon. Anodic bonding is performed by the following sequence of steps. The vacuum is first created. Then, a piston applies a force of 200 N to ensure a good contacting pressure between the wafers and the temperature of the chamber is raised to 350°C. A 600 V DC voltage is then applied with the cathode contacting the Pyrex and the anode touching the silicon. As a result, sodium ions (Na^+) in the Pyrex glass are electrostatically attracted towards the cathode, leaving a Na^+ depleted zone with dioxide ions ($O^{2=}$) close to the bonding surface. These $O^{2=}$ ions can chemically bond with the contacting Si^+, creating a layer of SiO^2 at the wafer

interface. The temperature is then slowly ramped down to avoid that the slightly different expansion coefficients between glass and silicon cause stress and potentially cracking. The anodic bonding process is presented in Figure 3-14.

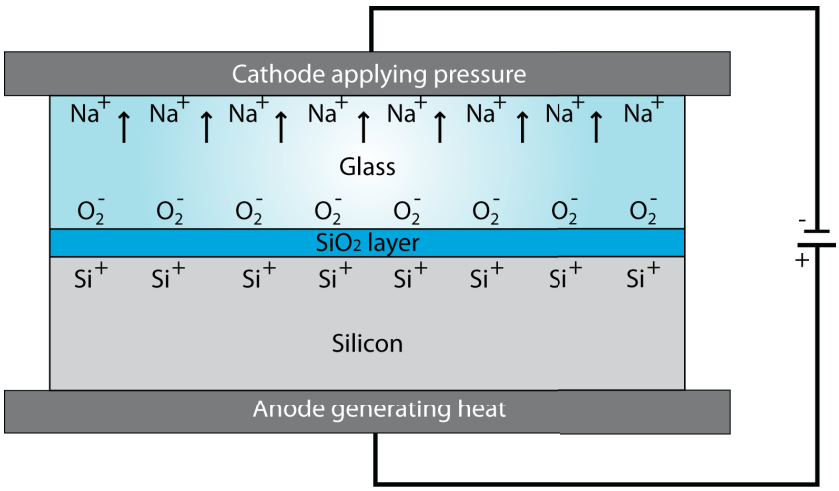

Figure 3-14 : Anodic bonding by electrical displacement of the Na^+ ions.

We attempted to use the crack test technique to measure the strength of the anodic Si-Pyrex bond, but were unable to do so because the Pyrex wafer broke before the razor blade could even be slightly introduced into the interface. Still, that behavior is indicative of the high strength of the anodic bond, which has a typical surface energy of around 1 J/m^2 [15] – a full order of magnitude stronger than measured for the Si-Si direct bond.

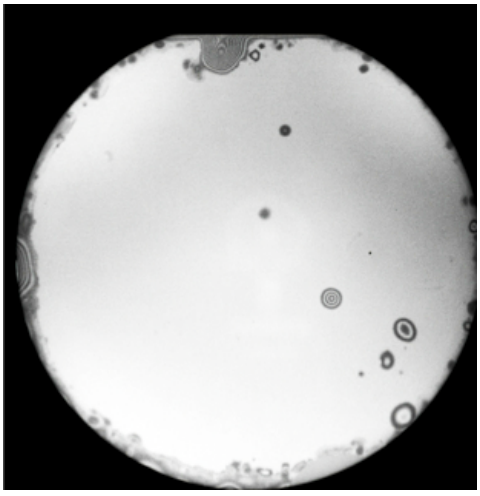

Figure 3-15 : Voids at the bond interface of Si-Pyrex anodically bonded wafers.

The void density was also inspected under IR, as illustrated with a representative case in Figure 3-15. With anodic bonding, the quality of the bonding interface is superior to that of direct bonding, as implied by the reduced number of voids compared to Figure 3-13.

In summary, anodic bonding exhibits better adhesion and interface uniformity than silicon direct bonding at 400°C, justifying its use for encapsulation with this technology. As an additional benefit, the transparency of the lid provides optical access to eventual MOEMS encapsulated devices.

3.4 References

[1] W. Sonphao and S. Chaisirikul, "Silicon anisotropic etching of TMAH solution," *Proc. IEEE Int. Symp. on Industrial Electronics*, vol. 3, pp. 2049–2052, June 2001.

[2] K. R. Williams et al., "Etch rates for micromachining processing-Part II," *Journal of Microelectromechanical Systems*, vol. 12, iss. 6, pp. 761-778, Dec. 2003.

[3] N. Fujitsuka, K. Hamaguchi, H. Funabashi, E. Kawasaki, and T. Fukada, "Silicon anisotropic etching without attacking aluminum with Si and oxidizing agent dissolved in TMAH solution," *Proceedings of the International Conference on Solid-State Sensors Actuators*, pp. 1667-1670, Boston, MA, 2003.

[4] P. M. Sarro, "Silicon Carbide as a new MEMS technology," *Sensors and Actuators A*, vol. 82, no. 1, pp. 210-218, May 2000.

[5] Y. T. Yang, K. L. Ekinci, X. M. H. Huang, L. M. Schiavone, M. L. Roukes, C. A. Zorman, and M. Mehregany, "Monocrystalline silicon carbide nanoelectromechanical systems," *Applied Physics Letters*, vol. 78, no. 2, pp. 162-164, January 2001.

[6] J. M. Melzak, "Silicon carbide for RF MEMS," *IEEE MTT-S International Microwave Symposium*, vol. 3, pp. 1629-1632, June 2003.

[7] S. Roy, R. G. DeAnna, C. A. Zorman, and M. Mehregany, "Fabrication and characterization of polycrystalline SiC resonators," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2323-2332, December 2002.

[8] M. C. Scardelletti, C. A. Zorman, and D. R. Oldham, "RF MEMS switches with SiC microbridges for improved reliability," *Antennas and Propagation Society International Symposium*, pp. 1-4, July 2008.

[9] S. Vengallatore, "Analysis of thermoelastic damping in laminated composite micromechanical beam resonators," *Journal of Micromechanics and Microengineering*, vol. 15, pp. 2398-2404, September 2005.

[10] G. L. Harris, Properties of Silicon Carbide, London, Inspec/IEE, 1995.

[11] D. G. Jones, R. G. Azevedo, M. W. Chan, A. P. Pisano, and M. B. J. Wijesundara, "Low temperature ion beam sputter deposition of amorphous silicon carbide for wafer-level vacuum sealing," *Proceedings of the International MEMS Conference*, pp. 275–278, Kobe, Japan, Jan. 2007.

[12] Y. Xiang, X. Chen and J. J. Vlassak, "The mechanical properties of electroplated Cu thin films measured by means of bulge test technique", *Materials Research Society*, vol. 695, L4.9, 2002.

[13] W. P. Maszara, "Silicon-on-insulator by wafer bonding: a review," *Journal of Electromechanical Society*, vol. 138, no. 1, pp. 341-347, Jan. 1991.

[14] T. R. Hsu and J. Clatterbaugh, "Joining and bonding technologies," *MEMS Packaging*, INSPEC IET, 2003.

[15] R. Knechtel, M. Knaup, and J. Bagdahn, "A test structure for characterization of the interface energy of anodically bonded silicon-glass wafers", *Microsystem Technologies*, vol. 12, no. 5, pp. 462-467, Apr. 2006.

4 Conclusion

4.1 Applications Beyond Packaging

Although this wafer-level technology was primarily developed for packaging purposes, it presents interesting potential to be extended to other applications with only slight modifications. Throughout this chapter, the cross-sectional diagrams follow the color legend shown in Figure 4-1.

Figure 4-1 : Color legend for process materials.

4.1.1 • Film Bulk Acoustic Resonator (FBAR)

The process developed in this work can be extended to fabricate film bulk acoustic resonators (FBAR), that have a similar filtering purpose but a different operation mechanism than the flexural mode beam resonators discussed in chapter 1. Whereas beam resonators exploit the longitudinal acoustic waves traveling across the length of the beam, FBARs function by the transverse transmission of acoustic waves across the thickness of a thin piezoelectric membrane.

The physical principle exploited by FBARs is that piezoelectric materials act as two-way transducers: they convert electrical energy into mechanical energy, and vice versa. Aluminum nitride (AlN) is an example of a layer material that can be used, which is piezoelectric in one of its crystallographic orientations. Figure 4-2 shows how the crystal responds to stress along this particular direction by creating an electric field proportional to the stress. Conversely, applying an electric field in the same direction induces stress in the crystal [1].

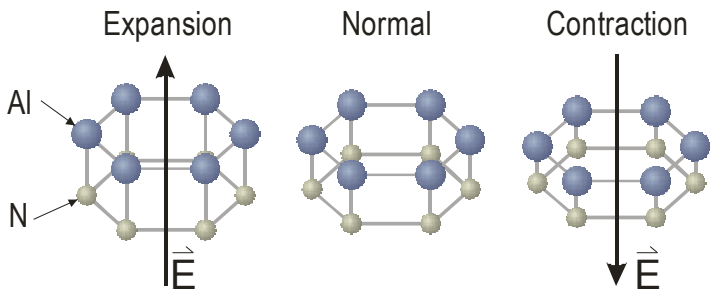

Figure 4-2 : Stress response of the AlN crystalline structure.

By sandwiching a film of piezoelectric material between two thin electrodes with the piezoelectric crystallographic direction along the thickness, mechanical stress can be induced by a voltage applied across the electrodes, as can be seen from Figure 4-3. Conversely, this arrangement can act as a sensor to detect the average stress within the piezoelectric material.

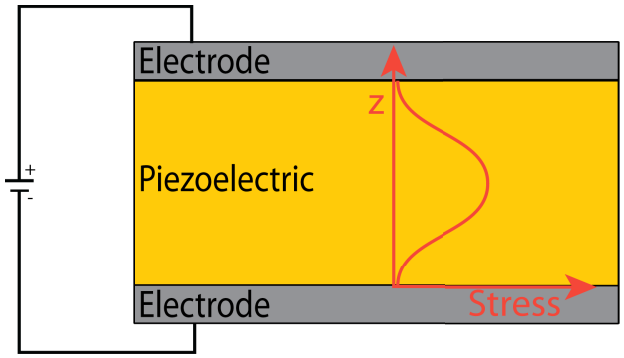

Figure 4-3 : Stress field amplitude of the piezoelectric material at resonance.

Naturally, the signal transfer through the piezoelectric film depends on the frequency of the signal and the thickness of the film. The concept of mechanical filtering relies on varying the thickness, in order to maximize the transfer of a chosen frequency. If surrounded by air or vacuum, the acoustic impedance at the boundary between the membrane and the surrounding medium causes large reflections, and therefore makes the structure act as an acoustic cavity, trapping energy inside. This cavity will resonate in its fundamental mode when the wavelength is twice the thickness of the film, by setting up a coherent standing wave [2]. Meanwhile, other nearby wavelengths will get dampened out. Therefore, the output voltage will be highly selective to the chosen frequency. The advantage of filtering in the mechanical domain is that piezoelectric materials have

intrinsically high Q-factors, whereas high-Q filtering in the electrical domain requires the construction of many bulky capacitors and inductors.

The bulk-micromachined nature of the wafer-level technology developed for this work, as well as its SiC-reinforced membranes, render it highly suitable for building FBARs. Indeed, we can use the SiC / Al membranes of the WLP process as the support for the electrode-piezoelectric-electrode sandwich required for film bulk filtering. The FBAR layered structure can be added to the standard WLP membranes by DC sputtering aluminum in a nitrogen ambient to deposit piezoelectric AlN, followed by the DC sputter deposition of a top metal electrode. Of course, other piezoelectric (e.g. zinc oxide) and electrode (e.g. gold) materials could equally be used.

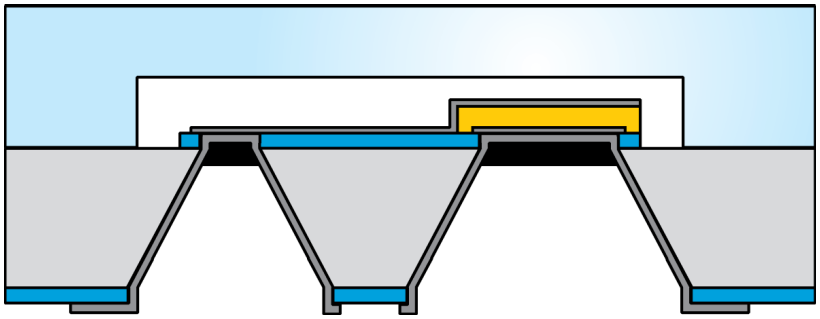

Figure 4-4 : FBAR implementation.

The thickness of the piezoelectric film must be of the same order of magnitude as the acoustic wavelength of the filtered signal, which corresponds to a few microns for signals in the gigahertz range. This is a perfectly suitable size for implementation on the membranes of the developed wafer-level process with the processing techniques available. To limit acoustic losses to the substrate, and therefore reduction of the Q-factor, it is greatly beneficial that the membranes in the developed process are entirely suspended, with nothing lying beneath or above [3]. The void created by the anisotropic etch of the back of the silicon substrate is instrumental in isolating the acoustic energy within the device itself, precluding it from being radiated into an underlying substrate, and thereby incurring losses to the device.

Fabricating FBARs using the developed wafer-level technology is beneficial in that it allows the integration with both conventional surface-micromachined MEMS and

CMOS semiconductor devices, without any additional size overhead, since the FBAR can be built on top of one of the electrical feedthrough interconnects.

4.1.2 • Piezoresistive Pressure Sensor

Most pressure sensor implementations require a deflecting diaphragm separating two zones of different pressures. Thanks to the SiC-reinforced membranes sealing the cavities from the feedthrough interconnects, a slightly modified version of the wafer-level process can be used to fabricate a pressure sensor by the addition of a piezoresistive material. This piezoresistive material, e.g. polysilicon, metal, is used to form a stress-sensitive element on the front side of the diaphragm membranes. Figure 4-5 presents the piezoresistive implementation of a pressure sensor based on the developed wafer-level process.

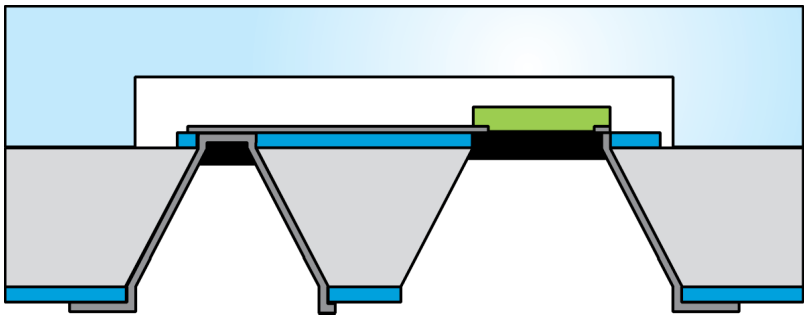

Figure 4-5 : Piezoresistive pressure sensor implementation.

A constant gas pressure can be obtained inside the cavity by controlling the surrounding pressure when the seal is made. During device operation, the resulting pressure differential between the interior of the cavity and the environmental pressure will cause the membrane to deflect, thereby affecting the stress of the piezoresistive material, and thus its resistivity. The use of silicon carbide to reinforce the diaphragm allows the sensor to sustain harsher environments and survive larger pressure differences, therefore enhancing the range of applications for this system.

These pressure sensors can be conveniently implemented on a monolithic chip comprising other MEM and semiconductor devices, without compromising the ability to package the system at the wafer-level by the technology presented in section 4.2.

4.1.3 • Capacitive Pressure Sensor

We can also implement pressure sensors by using a capacitive sensing method, which uses the basic membrane of the wafer-level process formed of SiC and aluminum as the pressure diaphragm. For this method, a suspended square electrode is required over the diaphragm, so that the capacitance between the diaphragm and the electrode can be measured. With the deflection of the membrane arising from the pressure difference between the interior of the cavity and the external environment, the capacitance between the membrane and the suspended electrode will vary according to the distance between the two. The measured capacitance can therefore be related to the absolute pressure in the environment, provided the internal pressure is known.

The electrode must be electrically conductive (e.g. aluminum) for proper coupling, and can be conveniently built using typical surface micromachining techniques. The gap between the membrane and the electrode can be realized by releasing a sacrificial material (e.g. polyimide), provided there are sufficient release holes in the electrode for the etchant to reach through. Afterwards, during device operation, the holes will be equally useful, as they will ensure that pressure is identical on both sides of the electrode; this prevents undesirable deformations of the electrode and unwanted variations in the measured capacitance. Figure 4-6 presents a possible implementation based on the developed WLP technology.

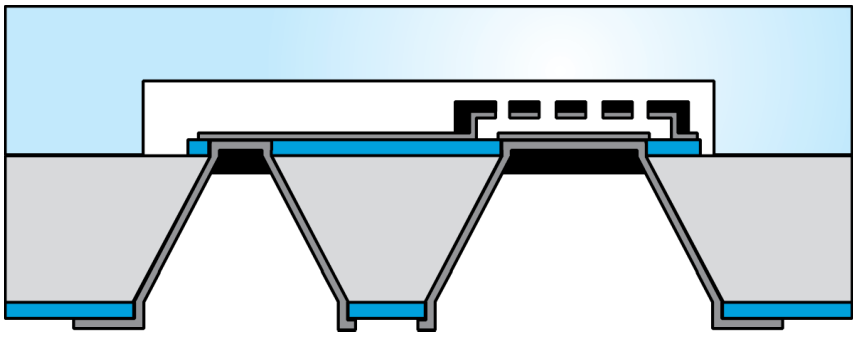

Figure 4-6 : Capacitive pressure sensor implementation.

Just like piezoresistive pressure sensing, this capacitive sensing method is readily compatible with integration to chips holding combined electronics and MEMS, and does not diminish the ability to perform successful hermetic wafer-level encapsulation.

4.2 Summary

In this thesis, we reviewed various applications of MEMS, taking a closer look at pressure sensors, inertial sensors, MOEMS and RF-MEMS. We also presented our initial motivation for undertaking the design of a novel packaging process, namely the potential of monolithically integrating a phase-locked loop electronic system with MEM resonators, for enhanced performance and reduced cost and size. We then examined different possible solutions for packaging, demonstrating the benefits of wafer-level compared to the customary chip-level, i.e. batch processing efficiency, superior device protection and improved electrical properties. Subsequently, we detailed the entire fabrication flow of the developed packaging technology for vacuum encapsulation, which allows monolithic integration through low-temperature processing and CMOS compatibility. We followed-up by discussing the issues encountered during process development, and how they were solved. We then presented and discussed experimental results arising from the development of this work, demonstrating its practical viability. Finally, based on the designed technology, we presented interesting applications other than for packaging purposes, such as pressure sensors and film-bulk acoustic wave resonators.

In future work, the level of vacuum inside the encapsulating cavities will have to be quantitatively determined, either through the use of Pirani pressure gauges or by the actual integration of MEM resonators and analysis of their resonant frequency and Q-factor. After this last experimental step, the process will be fully qualified for high vacuum encapsulation, although it is already ready for hermetic encapsulation. The integration of a getter, when developed, will help achieve even higher vacuum. Additionally, we expect few challenges to be encountered in the extension of the technology for the implementation of pressure sensors and film-bulk acoustic wave resonators as portrayed in this work.

4.3 References

[1] R. Aigner, "Volume manufacturing of BAW-filters in a CMOS fab," *Journal of 2nd International Symp. On Acoustic Wave Devices for Future Mobile Comm. Systems,* Chiba University, Japan, pp. 129-134, 2004.

[2] K. Wang et al., "Micromachined bulk acoustical-wave RF filters," *Proc. of 7th Solid-State and Int. Circ. Tech*, San Jose, California, vol. 3, pp. 1687-1690, Oct. 2004.

[3] S. Mishin et al., "Sputtering processes for bulk acoustic wave filters," Semiconductor International, March 2003.