Burst-Mode Clock and Data Recovery with FEC for Passive Optical Networks

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Your file Votre référence
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To Maa and Paa with all my love

&

To my beloved Ishana

Abstract

Optical multiaccess networks, and more specifically passive optical networks (PONs) are considered to be one of the most promising technologies for deploying fiber-to-the-building/home/curb (FTTx). PONs are expected to solve the problem of limited bandwidth, the so called "first and last mile problem", that remains the bottleneck between the backbone network and high-speed local area networks (LANs). PONs provide a low-cost solution and a guaranteed quality of service (QoS) to enable new multimedia services. In a PON, multiple users share the fiber infrastructure in a point-to-multipoint (P2MP) network topology. This is in contrast to current access technologies, including DSL, VDSL, and cable, which use a point-to-point (P2P) network topology. The P2MP nature of networks introduces optical path delays which inherently cause the data packets to undergo amplitude, phase, and frequency variations - burst-mode trafic. This consequently creates new challenges for the design of optical receivers.

Optical receivers, and in particular, burst-mode receiver front-ends (BM-RXs) and burst-mode clock and data recovery circuits (BM-CDRs), must adapt to burst-mode traffic, where data bursts originate from various sources and travel different distances. The amplitude and phase of successive packets may therefore vary anywhere between $0-20$ dB and $-\pi$ to $+\pi$ rads. The research objective of this thesis is to design, test, and enhance performance requirements of BM-CDRs for PONs.

We design and experimentally demonstrate a 622/1244 Mb/s BM-CDR with forward error correction (FEC) using Reed-Solomon (R-S(255, 239)) codes for Gigabit PONs (GPONs). We measure a coding gain of approximately 5 dB at bit error ratio (BER) of 10^{-10}. The coding gain obtained verifies the claim of the increased link budget specified by ITU-T G.984.3 standard.

We also develop a novel technique for fast burst-error correction for bursty channels. This is achieved by employing FEC on BM-CDRs with fast phase acquisition time. We demonstrate this with our custom built bit error rate tester/analyzer (BBERT/A).

Finally, we develop a small-signal modeling technique for characterizing photodiodes. This technique is based on the measurement of S_{11} parameters. We demonstrate our idea with a 10 GHz 1310/1550 nm InGaAs/InP PIN photodiode.

Résumé

Les réseaux optiques à accès multiple, et plus spécifiquement les réseaux optiques passifs (PONs - "passive optical networks"), sont considérés comme l'une des technologies les plus prometteuses pour déployer la fibre optique jusqu'au domicile, à l'immeuble, ou au trottoir (FTTx). On s'attend à ce que les réseaux optiques passifs résolvent le problème de la largeur de bande passante qui demeure le goulot d'étranglement entre le réseau de base et les réseaux locaux à grande vitesse (LANs). Les PONs fournissent une solution peu coûteuse et une qualité garantie de service (QoS) pour permettre de nouveaux services de multimédia. Dans un réseau optique passif, plusieurs utilisateurs partagent la même infrastructure de fibre jusqu'à la centrale en utilisant une liaison point à multipoint du réseau (P2MP). Ceci est contraire aux technologies d'accès courantes, comprenant le DSL, le VDSL et le câble, qui utilisent un point pour diriger la topologie du réseau (P2P). La liaison point à multipoint des réseaux présente des délais entre les paquets de données. Ces délais font subir des changements d'amplitude, de recouvrement et de variations de fréquence aux paquets de données. Ceci crée par conséquent de nouveaux défis pour la conception des récepteurs optiques.

Les réseaux optiques, en particulier les circuits pouvant rétablir l'amplitude (circuits BM-RX - "burst-mode receiver front-ends") et les circuits pouvant rétablir rapidement les impulsions d'horloge et les données (circuits BM-CDR - "burst-mode clock and data recovery circuits") doivent s'adapter au trafic fonctionnant par paquets ("burst-mode traffic"), où les paquets proviennent de sources diverses et parcourent des distances différentes.

L'amplitude et la phase des paquets successifs peuvent donc changer entre $0 - 20$ dB et $-\pi$ à $+\pi$ rads. L'objectif de recherche de cette thèse est de concevoir, examiner et augmenter les conditions d'exécution des circuits BM-CDRs pour les PONs.

Nous concevons et démontrons expérimentalement un circuit BM-CDR de 622/1244 Mb/s avec la correction d'erreurs sans voie de retour (FEC - "forward error correction") en utilisant des codes Reed-Solomon (R-S(255, 239)) pour des GPONs ("gigabit PONs"). Nous mesurons un gain de codage d'approximativement 5 dB correspondant à un BER de 10^{-10}. Le gain de codage obtenu, vérifie la réclamation du budget de lien accru indiqué par le standard ITU-T G.984.3.

Nous développons également une technique nouvelle pour la correction rapide d'erreurs pour des chaînes transportant des données par paquets. Ceci est réalisé en utilisant FEC

sur les circuits BM-CDRs avec un recouvrement rapide de l'horloge. Nous démontrons ceci avec notre appareil de contrôle pour mesurer le taux d'erreurs sur les bits.

Finalement, nous développons une technique modelant le "small-signal" pour caractériser des "photodiodes". Cette technique est basée sur la mesure des paramètres S_{11}. Nous démontrons cette idée avec un "10 GHz 1310/1550 nm InGAs/InP PIN photodiode".

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Om Shree Ganeshayah Namah

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I am indebted to Julien Faucher, from whose research, this thesis has been possible. I thank him for proposing the idea of employing FEC in BM-CDRs for GPON and for his guidance. I would also like to thank my friends and colleagues who have contributed to my research: Ming Zeng, for playing an important role in the design of the R-S$(255, 239)$ decoder; Ishana M. Gopaul, for providing assistance during the testing and characterization of the receiver; Bharathram Sivasubramanian, for our useful discussions on bursty channels and error-correcting codes; Mustansir Mukadam, for helping out at the critical stages with valuable suggestions; and Wei Tang for training me in the lab and for the technical advice.

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My sister, Ami has played an influential role in my life. She has made me believe in myself in times when I have lost hope. I cannot imagine myself without her. You have not only taken me as a brother, but also as a friend and a son. Thank you, Ami, for all your prayers and blessings.

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Jai Shree Radhe-Krishna

Bhavin J. Shastri
May 2007

Associated Publications and Contribution of Authors

The work presented in this thesis has been published in the form of conference proceedings [1][2], an invited workshop [3], and a technical report [4]. The author of this thesis designed

- the burst-mode clock and data recovery (BM-CDR) with forward error correction (FEC) for gigabit-capable passive optical networks (GPONs) [1], [2];
- the technique for burst-error correction in bursty channels with fast phase acquisition CDRs and FEC in [1], [2];
- the four-step photodiode modeling technique in [4];
- the burst-bit error rate tester and analyzer (BBERT/A) for characterizing burst-channels in [1], [2], [3].

The receiver presented in this thesis is built from the experimental setup assembled by Julien Faucher, Mustansir Y. Mukadam, and Alan Li, for testing and characterizing their work on burst-mode clock phase aligners (BM-CPA).

Julien Faucher proposed the idea of employing FEC in BM-CDRs for GPON. The author of this thesis implemented the idea and gave an experimental demonstration of such a system. The author of this thesis further demonstrated that this technique can be used to eliminate burst-errors in bursty channels to give accurate, predictable, and reliable burst bit error ratios (BBERs).

Ming Zeng contributed to the design of the BM-CDR with FEC. In particular, she participated in the implementation of the R-S$(255, 239)$ decoder. Ishana M. Gopaul and Ming Zeng provided assistance during the testing and characterization of the BM-CDR with FEC. Bharathram Sivasubramanian was involved in useful discussions on bursty-channels and error-correcting codes. He provided valuable suggestions on the BBERT/A. The original design of the BBERT was proposed by Julien Faucher.

Wei Tang developed the four-step photodiode modeling technique. The author of this thesis contributed in the simulations and experiments for modeling the photodiode.

Conference Papers

1. **B. J. Shastri**, J. Faucher, M. Zeng, and D. V. Plant, "622/1244 Mb/s burst-mode clock and data recovery for gigabit passive optical network uplink," *IEEE LEOS 18th*

Annual Workshop on Interconnects within High Speed Digital Systems, May 2007.

2. **B. J. Shastri**, J. Faucher, M. Zeng, and D. V. Plant, "Burst-mode clock and data recovery with FEC and Fast Phase Acquisition for Burst-Error Correction in GPONs," *IEEE 50th Int'l Midwest Symposium on Circuits & Systems/IEEE 5th Int'l Northeast Workshop on Circuits & Systems*, accepted for publication, Aug. 5-8, 2007.

Invited Workshop & Technical Reports

3. **B. J. Shastri**, J. Faucher, M. Zeng, M. Y. Mukadam, and D. V. Plant, "Burst-mode clock phase aligner for GPON OLT applications," *Canadian Microelectronics Corporation (CMC) TEXPO Annual Symposium*, Ottawa, Canada, Oct. 23-24, 2006.

4. **B. J. Shastri**, W. Tang, and D. V. Plant, "EMCORE 10GHz 1310/1550nm PIN photodiode (MR030) Test Report," EMCORE and McGill Univ., Montréal, Canada, Tech. Rep., 2006.

Other publications and technical reports not directly related to this thesis

5. **B. J. Shastri** and M. D. Levine, "Face recognition using localized features based on non-negative sparse coding," *Machine Vision and Applications*, vol. 18, no. 2, pp. 107-122, April 2006.

6. Wei Tang, **B. J. Shastri**, and D. V. Plant, "Experimental results of cross-talk power penalty measurement in a 3.125 Gb/s parallel optical receiver," *Agile All-Photonic Networks (AAPN) Annual Research Meeting*, Ottawa, Canada, July 2006.

7. **B. J. Shastri**, D. V. Plant, and H. Hinton, "Resonator design for rhodamine-6G dye-laser in continuous-wave mode," Tech. Rep., McGill Univ., May 2005.

8. **B. J. Shastri**, D. V. Plant, and H. Hinton, "Analysis for rhodamine-6G dye-laser in continuous-wave mode," Tech. Rep., McGill Univ., Mar. 2005.

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List of Acronyms

APON	Asynchronous transfer mode passive optical netwotk
ARQ	Automatic request repeat
ASIC	Application specific integrated circuit
ATM	Asynchronous transfer mode
AWGN	Additive white Gaussian noise
BERT	Bit error rate tester
BBERT	Burst bit error rate tester
BER	Bit error ratio
BBER	Burst bit error ratio
BM-CDR	Burst-mode clock and data recovery
BM-CPA	Burst-mode clock phase aligner
BM-PG	Burst-mode packet generator
BM-RX	Burst-mode receiver
BM-TS	Burst-mode test setup
BPON	Broadband passive optical network
CDR	Clock and data recovery
CO	Central office
CIDs	Consecutive identical digits
EPON	Ethernet passive optical network
FEC	Forward error correction
FSAN	Full-service access network
FTTH	Fiber-to-the-home
ISI	Intersymbol interference
ITU-T	International Telecommunication Union -

	Telecommunication Standardization Sector
LA	Limiting amplifier
LANs	Local access networks
MLM	Multi-longitudinal mode
MPN	Mode partition ratio
NRZ	Non-return-to-zero
OC	Optical communication
ODN	Optical distribution network
OE	Optical-to-electrical
OLT	Optical line terminator
ONT	Optical network termination
ONU	Optical network unit
P2MP	Point-to-multipoint
P2P	Point-to-point
PC	Power combiner
PLL	Phase-locked Loop
PLR	Packet loss ratio
PMD	Physical-media-dependent
PON	Passive optical network
PRBS	Pseudo-random bit sequence
PS	Power splitter
R-S	Reed-Solomon
RZ	Return-to-zero
SNR	Signal-to-noise ratio
SONET	Synchronous optical network
TC	Transmission convergence
TDM	Time division multiplexing
TDMA	Time division multiple access
TIA	Transimpedance amplifier
VCO	Voltage controlled oscillator
WDM	Wavelength division multiplexing
QoS	Quality of service

Chapter 1

Introduction

There is always a way to do it better... find it!
– Thomas A. Edison

1.1 Motivation

The desire for higher bandwidth is increasing rapidly with the growth in demand for multimedia services. The two questions that stem from this statement are: (1) How rapid is the increase of bandwidth? and (2) What is the rate of growth of demand for multimedia services? To answer these questions, let us first take a look at what has spurred the demand for bandwidth.

Consider the case of traffic sent over the Internet. Prior to the last decade, Internet traffic was largely text-based information with file transfer and email being the most popular services. However, during the last decade, the surge of the Internet was largely due to the graphical nature of the World Wide Web (WWW) [1]. This comes as no surprise as the saying goes "A picture is worth a thousand words!" This is also true from the perspective of the digital domain, as graphical based image information generally consists of many more bits than text based information. Consequently, to transfer large graphical image files with sufficiently small delay, a much broader bandwidth is needed than that required for the transfer of text files.

To get a quantitative feel of the trends in global bandwidth requirements, consider the Internet. Bandwidth requirements increase by a factor of 50 to 100 every five to seven years. This statement implies that the volume of data transported over the Internet backbone

increases with the exponential growth in the number of Internet users [2]. Based on the current bandwidth trends, it can be projected that by 2010 to 2015, the global Internet backbone will have to handle bandwidths higher than 1000 Tb/s!

Optical fibers have extremely high bandwidths and the lowest cost as a transmission medium of data over long distances when compared to other available transmission media that include copper wires for twisted pair and coaxial cable technologies.

Clearly, the fiber is the most flexible and "future proof" medium for providing multimedia services such as interactive video, voice, and fast Internet, commonly known as the "triple play" services, which have now become the way of life.

Hence, with the adequate demand for services and maturing of technology, a point has been reached where it is becoming cost effective to deliver these services [3]. From this discussion, it should be clear that the million, or rather the billion dollar question is not "If" but rather "When will this happen?"

This thesis addresses the latter question by providing novel solutions at the receiver level.

1.2 Problem Statement

Passive optical networks (PONs) are an emerging optical multiaccess network based on all-optical core. A PON is a point-to-multipoint (P2MP) network where multiple users share the same fiber infrastructure with no active elements in the field. All active components reside either in the central office (CO), operated by service providers, or at users' end. PONs provide a low-cost solution of deploying fiber-to-the-premises/cabinet/building/home (FTTx) which is an effective solution to enable new multimedia services. Consequently, PONs are expected to solve the so called "first and last mile problem", that remains the bottleneck between the backbone network and high-speed local area networks (LANs).

PONs offer a mixture of distributive and interactive services to a large number of subscribers, with guaranteed quality of service (QoS). By removing electronic regenerators, amplifiers, and grooming mechanisms from the fields, PONs are simple to deploy and cost effective because they decrease the real estate of the CO, the labor cost involved in fiber access deployment, and length of fiber plant to maintain [3].

The P2MP network topology of PONs creates optical path differences. This is in contrast to the current access technologies, including DSL, VDSL, and cable, that use a point-

to-point (P2P) network topology. Thus, the PON architecture inherently causes the packets of data to vary in phase, frequency, and amplitude - burst-mode traffic. This consequently creates new challenges for the design of optical receivers.

Optical receivers, and more specifically, burst-mode receiver front-ends (BM-RXs) and burst-mode clock and data recovery circuits (BM-CDRs), must adapt to burst-mode traffic, where data bursts originate from various sources and travel different distances. The amplitude and phase of successive packets may therefore vary anywhere between $0 - 20$ dB and $-\pi$ to $+\pi$ rads, respectively [4].

The research objective of this thesis is to design, test, and enhance performance requirements of BM-CDRs for PONs and mutiaccess networks in general.

1.3 Passive Optical Networks (PONs)

1.3.1 PON System Overview

The full-service access network (FSAN[1]) PON consists of an optical line terminator (OLTs), optical network units (ONUs) or optical network terminations (ONTs) - a maximum of 64, and an optical distribution network (ODN). Fig. 1.1 shows a topology of a PON architecture.

[1]The FSAN study group, a forum for world's leading telecommunications service providers and equipment suppliers to work towards a common goal of truly broad-band access networks, initiated PON standardization via recommendations for the physical-media-dependent (PMD) layer and the transmission convergence (TC) layer [5].

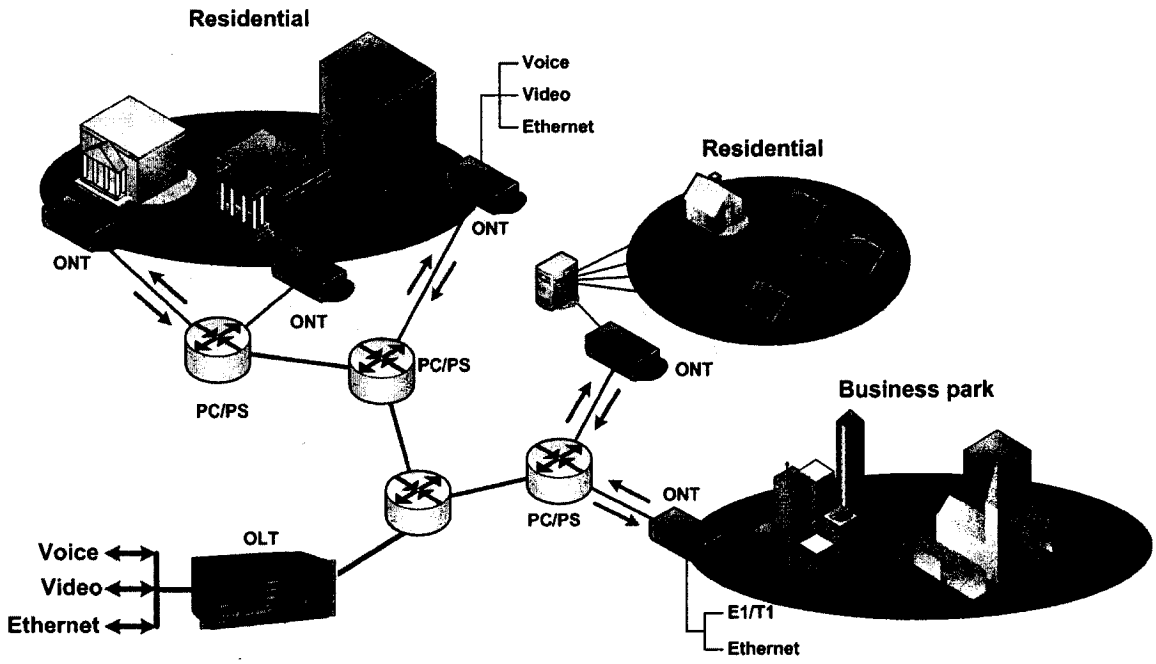

Fig. 1.1 Passive optical network. PS: power splitter; PC: power coupler; OLT: optical line terminator; ONT: optical network terminator.

ONTs/ONUs provide the interface between the customer equipment and the PON. The OLT which interfaces with the metro network, is located as the CO. The main functionality of the OLT is to adapt the data traffic from or to the metropolitan rings into or from the PON transport layer. The ODN is the optical network connecting OLT and ONTs/ONUs. It mainly consists of passive splitters (PS) or passive couplers (PC) and optical fibers.

A multiple access method is needed to avoid collisions and share the bandwidth across all users. Two possible methods that exist are time division multiplexing (TDM) and wavelength division multiplexing (WDM). WDM can be used in conjunction with or independently of TDM.

1.3.2 TDM PONs and WDM PONs

TDM PONs and WDM PONs create their own set of challenges for the design and testing of CDRs because of their unique characteristics. Currently, the most popular multiple access method that is used in conjunction with the various existing types of PON, is time

division multiple access (TDMA) [5]. This thesis will focus on the receiver design and testing challenges for TDM PONs.

WDM PONs

WDM technology can be deployed to achieve high performance. In a WDM PON, each ONU is assigned dedicated wavelengths for upstream and downstream transmissions. Wavelength multiplexing/demultiplexing components, usually realized with arrayed waveguide grating (AWG), must be deployed in the field to securely route each wavelength. WDM PONs create P2P links between the CO and each user, so no sharing is needed. However, dedicated transceivers with accurate wavelength control result in significant installation and maintenance expenses. WDM PONs are high performance but expensive access solutions today. As the demand for bandwidth increase and the cost of optical components decrease, WDM PONs will become practical and consequential.

TDM PONs

In the CO, an OLT broadcasts downstream traffic to subscribers and manages upstream traffic from subscribers. ONUs are deployed close to subscribers' homes for communication with the OLT. A feeder fiber connects the CO with the residential area. One or more passive couplers split or combine the optical power of the downstream or upstream traffic respectively. TDM PONs enjoy low installation and maintenance costs, however, they do not exploit the huge bandwidth of optical fibers.

1.3.3 TDMA PON Protocols

PONs come in a number of flavors. The first PON standard was asynchronous transfer mode (ATM) PON (APON), which used ATM encapsulation of the transported data and was aimed primarily at business applications. APON was quickly followed by ITU-T[2] G.983 series broadband PON (BPON) [6] that is also an ATM-based system but has superior features.

The IEEE[3] 802.3ah EPON [7], which was developed to exploit the advantages of Ethernet technology, is major TDMA PON protocol to be standardized. EPONs aim at converg-

[2]International Telecommunication Union - Telecommunication Standardization Sector.
[3]Institute for Electrical and Electronic Engineers.

ing the low cost equipment and simplicity for Ethernet and the low-cost fiber infrastructure of PONs. EPONs are a promising solution to provide sufficient bandwidth for emerging services such as videoconferencing, distributed gaming, IP telephony, and video on demand.

The second FSAN TDMA PON protocol is the ITU-T G.984 series Gigabit PON (GPON) [8], the successor of BPON and built on the experiences of EPON. Recently, GPONs have been attracting considerable attention from both industry and academia. GPON is able to support traffic other than ATM, such as, telephony and Ethernet, in its native format by using TDM partitions and generic framing procedure (GFP) formats. This offers a clear migration path for adding services onto the PON without disrupting existing equipment or altering the transport layer in any way while ensuring simplicity and scalability when dealing with new and emerging services. Table 1.1 summarizes the features of the TDMA PON protocols.

Table 1.1 Feature summary of the TDMA PON protocols [3]. US: upstream; DS: downstream; NRZ: non-return to zero; GEM: GPON encapsulation method; CES: circuit emulation service; VoIP: voice over Internet protocol; GTC: GPON transmission convergence; R-S: Reed-Solomon; AES: advanced encryption standard; OAM: operation, administration, and maintenance

Feature	BPON	GPON	EPON
Responsible standards body	FSAN and ITU-T SG15 (G.983 series)	FSAN and ITU-T SG15 (G.984 series)	IEEE 802.3 (802.3ah)
Data rate	155.52 Mb/s US 155.52 or 622.08 Mb/s DS	1.244 Gb/s US 2.488 Gb/s DS	1 Gb/s US/DS
Split ratio (ONUs/PON)	1:64	1:64	1:64
Line code	Scrambled NRZ	Scrambled NRZ	8B/10B
Number of fibers	1 or 2	1 or 2	1
Wavelengths	1310 nm US/DS or 1490 nm DS/1310 nm US	1310 nm US/DS or 1490 nm DS/1310 nm US	1490 nm DS/ 1310 nm US
Maximum OLT to ONU distance	20 km	10 and 20 km	10 and 20 km
Protection switching	Support multiple protection config.	Support multiple protection config.	None
Data format (encapsulation)	ATM	GEM and/or ATM	None
TDM support	via ATM	direct (via GEM or ATM or CES)	CES
Voice support	via ATM	via TDM or VoIP	VoIP
Multiple QoS levels	Yes (Mix of free, assured, and best effort bandwidth assignments)	Yes (Mix of free, assured, and best effort bandwidth assignments)	Yes (802.1Q priority levels)
FEC	None	R-S(255,239)	R-S(255,239)
Encryption	AES - 128 bit key	AES - 128 bit key req. 192 & 256 optional	None
OAM	ATM	GTC frame fields and ATM/GEM OAM	802.3ah Ethernet OAM frames

If we assume similar cost figures for the different TDMA PON protocols, then efficiency is the most dominant factor when determining the cost per bit or the amount of "revenue bits" that can be extracted from the network [1]. The overall PON efficiency for the different protocols is summarized in Table 1.2. These efficiencies are based on a traffic model analysis by FSAN.

Table 1.2 Efficiency comparison of the TDMA PON protocols [1].

	BPON	GPON	EPON
Total bandwidth	622 Mb/s DS 155 Mb/s US	2.5 Gb/s DS 1.25 Gb/s US	1.25 Gb/s DS 1.25 Gb/s US
Efficiency	72%	94%	49%
Revenue throughput	448 Mb/s DS 112 Mb/s US	2.36 Gb/s DS 1.18 Gb/s US	612 Mb/s DS 612 Mb/s US

From Table 1.2, it is clear that GPON offers exceptionally higher efficiency that leads to more "revenue bits" when compared to BPON and EPON. In addition, GPON also offers multiple-service support with the richest set of operation, administration, and maintenance (OAM) features. Consequently, GPON is the most advanced PON protocol in the access network today.

1.4 GPON System Architecture

GPON access networks have a passive tree structure. Fig. 1.2 illustrates the GPON access system. The ODN consists of passive optical elements such as splitters, fibers, connectors, and splices forming an optical path [5].

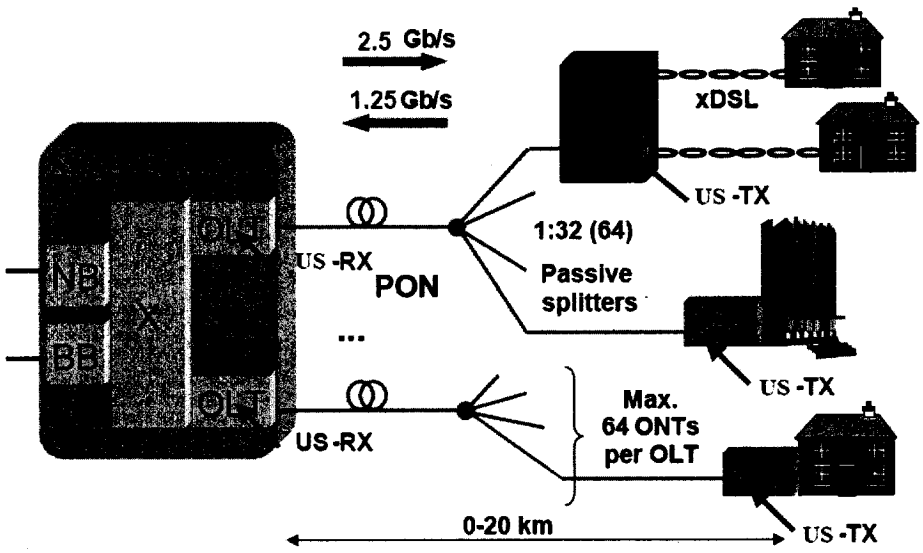

Fig. 1.2 GPON network architecture for FTTx scenarios [5]. From a single OLT at an access node, it connects a maximum of 64 ONUs/ONTs at the customer's premises via shared media of the ODN, which mainly contains a maximum of 20 km fiber and one or more passive optical splitters. NB: narrow-band; BB: broad-band; US-RX: upstream receiver; US-TX: upstream transmitter; OLT: optical line terminator; ONT: optical network terminator; ONU: optical network unit; xDSL: assymetric/very-high speed subscriber lines.

In the downstream direction (downlink), the network is P2P: continuous 2.488 Gb/s data is broadcasted from a single OLT to multiple ONUs (maximum of 64) using TDM in the wavelength band of $1480 - 1550$ nm. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous mode integrated circuits (ICs). The challenge in the design of a chip set for PONs comes from the upstream data path.

In the upstream direction (uplink), the network is P2MP: using TDMA, multiple ONUs transmit 1.244 Gb/s bursty data in the 1310 nm window to the OLT in the CO. Because packets can vary in phase and amplitude due to optical path differences, the OLT requires a BM-RX and a BM-CDR. Within the OLT, the BM-RX is responsible for amplitude recovery[4], whereas the BM-CDR is responsible for phase recovery.

The GPON access system has two distinct layers: the physical-media-dependent (PMD) layer and the transmission convergence layer (TC). Fig. 1.3 depicts the GPON physical layer as a set of PMD building blocks.

[4]BM-RX can sometimes refer to a receiver handling both amplitude and phase recovery.

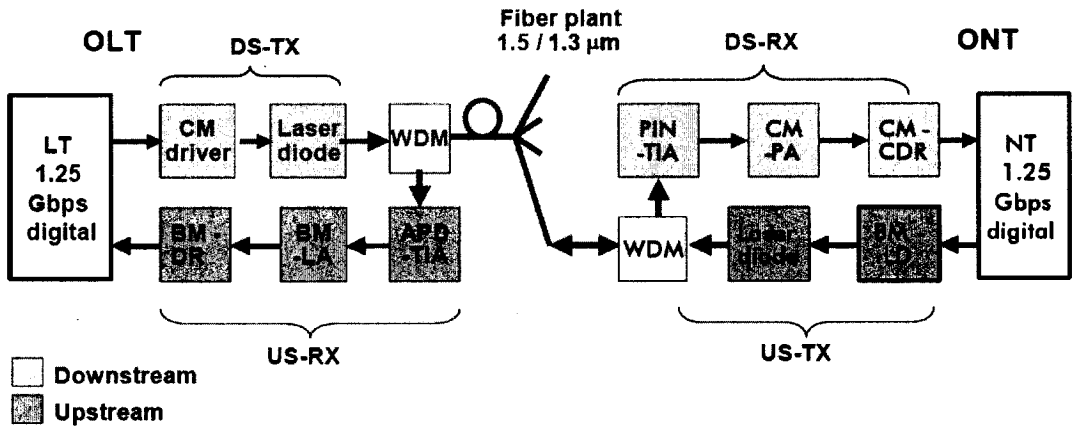

Fig. 1.3 GPON PMD functional building blocks [5] consist of a downstream transmitter (DS-TX) and an upstream receiver (US-RX) at the optical line terminator (OLT); a downstream receiver (DS-RX) and an upstream transmitter (US-TX) at the optical network terminator (ONT). The US-TX contains a laser diode and a burst-mode laser diode driver (BM-LDD), and the US-RX contains an avalanche photodiode/transimpedance amplifier (APD/TIA) and a burst-mode receiver (BM-RX) for amplitude recovery. Phase recovery is performed by a burst-mode clock phase aligner (BM-CPA).

The upstream transmitter (US-TX), in the uplink, is comprised of a laser diode and a burst-mode laser diode driver (BM-LDD). The upstream receiver (US-RX) contains an avalanche photodiode/transimpedance amplifier (APD/TIA) and a BM-RX for amplitude recovery. The task of phase recovery is performed by a burst-mode clock phase aligner (BM-CPA)[5] after the US-RX.

In the downlink, the downstream transmitter (DS-TX) is comprised of a laser diode and a continuous mode (CM) laser driver. The downstream receiver (DS-RX) consists of a PIN/TIA, a CM post amplifier (CM-PA), and a CDR.

Table 1.3 lists the GPON PMD layer key specifications in the upstream direction (for 622 Mb/s and 1.244 Gb/s) as defined in the ITU-T Recommendation G.984.2.

[5]BM-CPA is a synonym of BM-CDR.

Table 1.3 Key PMD parameters of GPON 622 Mb/s and 1244 Mb/s upstream.

Items	Unit	622 Mb/s	1244 Mb/s
Bit rate	Mb/s	622.08	1244.16
Wavelength	nm	1260 – 1360	1260 – 1360
Mean launched power - min	dBm	−2	−2
Mean launched power - min	dBm	+4	+3
Max. Tx enable	bit	8	16
Max. Tx disable	bit	8	16
Extinction ratio	dB	> 10	> 10
Min. sensitivity	dBm	−27 at BER=10^{-10}	−28 at BER=10^{-10}
CID immunity	bit	> 72	> 72
Bit error ratio	-	< 10^{-10}	< 10^{-10}
Overhead length	bytes	8	12
Guard time	bytes	2	4

1.5 Thesis Research Challenges

1.5.1 Receiver Design Challenges

Conventional optical receivers are designed for continuous data streams with constant optical power. These receivers are not suitable for P2MP burst mode operation because they cannot instantaneously react to packets arriving in bursts.

In TDMA PONs, multiple ONUs transmit bursty data to the OLT in the CO. Each ONU is assigned a dedicated time slot. Due to optical path differences, packets can vary in phase and amplitude. To deal with these variations, the OLT requires a BM-RX and a BM-CDR. The BM-RX is responsible for amplitude recovery, whereas the BM-CDR is responsible for phase recovery. Amplitude recovery and phase recovery are two processes that must repeat on a packet-by-packet basis at the beginning of every packet. Hence, the main challenge for BM-RXs and BM-CDRs is to provide fast level recovery and instantaneous phase recovery. This is especially critical for networks using short packets. By reducing the number of preamble bits required for the physical layer overhead functions like amplitude, phase, and frequency recovery, more bits are left for the payload to increase the information rate.

1.5.2 Receiver Testing Challenges

Burst-Mode Packet Generation

The difficulty in generating test signals is a problem for the testing of BM-RXs and BM-CDRs. This in turn complicates the testing, debugging, and characterization of the receivers before their use in a system demonstrator or a real application.

The requirement of customizing conventional test equipment is essential in testing the of BM-RXs and/or BM-CDRs. On the transmit side, the pattern generator should be able to produce amplitude and phase steps desired for testing. On the receive side, the error detector (ED) should be able to perform burst bit error ratio (BER) measurements on a device under test (DUT) that never really reaches steady state [9].

Burst Bit Error Rate Tester

Commercially available bit error rate testers/analyzers (BERT/As) are designed specifically to handle continuous mode data for synchronous optical networks with P2P links. However, for PONs where the traffic is bursty in nature, these BERTs lose pattern synchronization while the sampling clock is being recovered by the CDR. More specifically, commercial BERTs require: (1) a continuous alignment between the incoming pattern and the reference pattern, and (2) milliseconds to acquire synchronization.

It is therefore essential to design a burst bit error rate tester (BBERT) that does not require a fixed synchronization between the incoming pattern and the reference pattern of the ED. Synchronization should happen instantaneously at the beginning of every packet (non-continuous, bursty data), therefore enabling burst BER (BBER) measurements, error characterization, and amplitude/frequency/phase acquisition time measurements, all with good accuracy (ideally one bit).

1.5.3 Photodiode Modeling and Measurement

The photodiode parasitic capacitance C_{PD} is one of the most important parameters related to receiver designs. Due to its relatively big size, typically falling in the range of 0.1 pF to 1 pF, a dominant pole is formed at the receiver input that limits the receiver bandwidth. Therefore, it is important to know the value of C_{PD} while designing the receiver for a specific bandwidth. In addition, a photodiode model that includes the parasitic resistances

and capacitances associated with the bond pads is also necessary for accurate simulations. However, measuring C_{PD} and other parasitics is not straightforward and these parasitics can only be acquired by indirect measurements [10]. A simple method for accurate small-signal modeling is required for characterizing photodiodes.

1.6 Thesis Objectives

The objective of this thesis is to provide solutions for the problems enumerated above. In particular, we designed

- a BM-CDR with forward error correction (FEC) for TDMA networks;
- a technique of burst-error correction in bursty channels with FEC and BM-CDRs with fast phase acquisition times;
- a four-step photodiode modeling technique;
- a burst-mode test solution for characterizing bursty-channel errors.

The problem that this thesis does not address is the design of a BM-RX for amplitude recovery. This is because existing solutions are relatively mature, leaving less room for innovations. Instead, we choose to concentrate on enhancing the performance of BM-CDRs, one of the most critical blocks of a PON according to [11].

In order to contribute to the field, the research objective of the thesis is to design BM-CDRs with FEC to improve the coding gain and eliminate burst-errors in bursty-channels.

1.7 Thesis Overview

This thesis is organized as follows:

- **Chapter 2: Review of the State of the Art**

  In this chapter, we review existing BM-RXs solutions present in the literature, with the prime focus being on BM-CDRs. This chapter provides the necessary background information, and introduces terminology relevant to the design and challenges

of continuous-mode (conventional) CDRs, in the pursuit of BM-CDRs. A comprehensive analysis and design from an architecture level to the circuit level is followed throughout the chapter.

- **Chapter 3: Forward Error Correction for Digital Communications**

  The concept and theory of FEC techniques and in particular we review a class of nonbinary cyclic block codes called Reed-Solomon (R-S) codes is presented in this chapter. We also discuss how the optical link budget of GPONs can be increased by applying FEC with R-S codes in BM-CDRs.

- **Chapter 4: Experimental Demonstration of FEC in Burst-Mode CDRs with Instantaneous Phase Acquisition for Burst-Error Correction in GPONs**

  This chapter presents the implementation details of a 622/1244 Mb/s BM-CDR with FEC using Reed-Solomon (R-S) codes for GPONs. The coding gain obtained verifies the claim of the increased link budget specified by ITU-T G.984.3 standard. A novel technique for fast burst-error correction for bursty channels is also presented. This is achieved by employing FEC on BM-CDRs with fast phase acquisition time. We demonstrate this with our custom built BBERT.

- **Chapter 5: 10 GHz 1310/1550 nm PIN Photodiode Characterization**

  A standard procedure for accurate photodiode modeling is presented in this chapter. A commercial photodiode is tested using the proposed method. The results are compared with the specifications from the manufacturer to verify the effectiveness of this measurement procedure. More specifically, we present the characterization and analysis of a 10 GHz 1310/1550 nm InGaAs/InP PIN photodiode available from *EMCORE*. In total, four sets of experiments are performed to test the photodiode. The geometry features of the photodiode are verified. The dark current of the photodiode is measured. The photodiode parasitic capacitance is acquired indirectly from the measured results of the S_{11} parameter. And the responsivity is tested at wavelengths of 1310 nm and 1550 nm for different incident optical power and biasing conditions.

- **Chapter 6: Conclusions & Future Work**

  The last chapter concludes the thesis with a brief review of the main contributions of

the research presented in the preceding chapters. Some general remarks concerning the advantages and potential of the novel approaches are presented. We also propose future research directions.

1.8 Original Contributions

- Design and experimental demonstration of a 622/1244 Mb/s BM-CDR with FEC for GPONs with R-S(255, 239) decoding. The coding gain can be used to reduce the minimum and maximum transmitter power or increase the minimum receiver sensitivity by the same amount. Alternatively, this effective coding gain can be used to achieve a longer physical reach or a higher split ratio when using a multi-longitudinal mode (MLM) laser in the ONU. In this case, FEC is used to reduce the penalty due to mode partition ratio (MPN).

- Development of a methodology for burst-error correction in bursty channels. Our methodology is based on employing FEC with BM-CDRs with instantaneous phase acquisition for any phase step ($\pm 2\pi$ rad). This technique gives accurate and reliable BERs for bursty-channels.

- Burst-error characterization with a custom built BBERT that achieves instantaneous synchronization with the incoming pattern. Error characterization indicates whether errors are bursty, determines the lengths of burst errors with an accuracy of one bit, and flags when the error correcting capability of the FEC is reached.

- Development of a four-step photodiode modeling technique. The experimental results on a commercial photodiode match the manufacturer's specifications.

The work presented in this thesis has been published in the form of conference proceedings [12] [13], an invited workshop [14], and a technical report [15].

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Chapter 2

Review of the State of the Art

In this chapter, we review existing burst-mode receiver (BM-RX) solutions present in the literature, with the prime focus being on burst-mode clock and data recovery (BM-CDR). This chapter provides the necessary background information, and introduces terminology relevant to the design and challenges of conventional CDRs (CM-CDRs), in the pursuit of BM-CDRs. A comprehensive analysis and design from an architecture level to the circuit level is followed throughout the chapter.

2.1 Generic Optical Communication Systems

The goal of an optical communication (OC) system is to carry large volumes of data across a long distances [1]. An OC consists of three essential components: (1) an electro-optical transducer (for example a semiconductor laser diode) which converts the electrical data to optical signals to be transmitted over the fiber, (2) a fiber to guide the light, and (3) a photodetector (for example a photodiode) which senses the light at the end of the fiber and converts it to an electrical signal. Fig. 2.1 depicts a generic OC network.

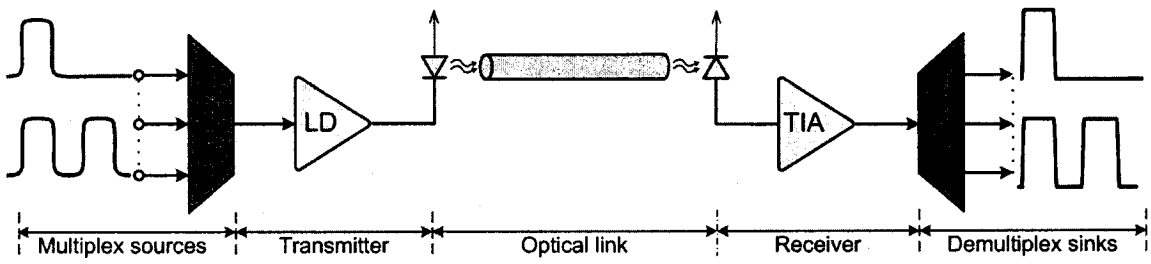

Fig. 2.1 Generic optical communication system [1]. MUX: multiplexer; LD: laser driver; TIA: trans-impedance amplifier; DEMUX: demultiplexer.

The standard components of an OC network include the following: the intensity of the light output from the laser must be high, the photodiode must exhibit high sensitivity, and the electrical signal generated by the photodiode must be amplified with a low noise. The reason for having these characteristics is attributed to the fact that despite the unique transmission capabilities of optical fibers, data gets distorted as it travels through the fiber, mostly because of fiber dispersion and attenuation due to the long physical reach of these networks. Attenuation causes the signal amplitude to be reduced due to loss throughout the fiber. Distortion leads to the closure of the data eye. Consequently, the system performance in terms of the bit error ratio (BER), defined as the average probability of incorrect bit identification, will degrade due to the signal-to-noise ratio (SNR) sustained by the data [2]. Hence, the transducer is generally driven by the laser driver to deliver large currents to the transducer and a transimpedance amplifier (TIA) follows the photodetector to amplify the output with low noise and sufficient bandwidth.

Multiple users share the same fiber infrastructure to transmit data over this optical link. Thus, the transmitter (TX) must be able to perform a parallel-to-serial conversion which is aided by the multiplexer (MUX). At the receiver (RX), serial-to-parallel conversion is performed by a demultiplexer (DEMUX) to reproduce the original parallel channels. The design of receivers is the scope of this thesis.

2.2 Optical Receivers

A general anatomy of an optical receiver is shown in Fig. 2.2. An optical receiver has two distinct blocks: a front-end and a clock and data recovery circuit.

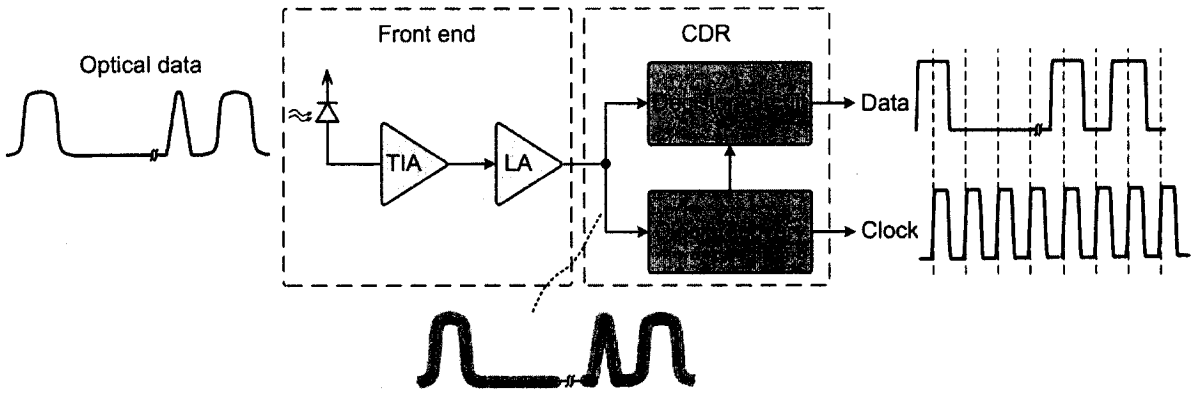

Fig. 2.2 General anatomy of an optical receiver. TIA: trans-impedance amplifier; LA: limiting amplifier; CDR: clock and data recovery.

2.2.1 Receiver Front-End

The main function of the front-end is to perform optical-to-electrical (OE) conversion of the data signal. The photodiode achieves this by converting the optical signal into an electric current. The TIA amplifies the output current from the photodiode into a voltage signal. The front-end must make sure that the OE signal conversion and amplification is achieved by introducing as low noise as possible. The component that follows the TIA is a limiting amplifier (LA) which is a high-gain amplifier. Its function is to compensate for the limited output swing of the TIA which may not be sufficient to provide logic levels.

2.2.2 Clock and Data Recovery

Due to the inherent presence of additive noise, introduced by the front-end, and intersymbol interference (ISI), it is necessary to interpose a decision circuit between the LA and the DEMUX to clean up the data signal. To perform this operation, the decision circuit needs a clock. However, in most practical systems, a global clock from the TX end is not provided. There are two apparent reasons for this. Firstly, adding an extra channel to transmit the clock signal from the TX to RX is costly due to the large physical reach of OC networks. Secondly, even if the cost is to be endured, this extra channel may well be used for transmitting data instead and therefore support more bandwidth in the network. Thus, the clock must be generated locally by a clock recovery circuit.

This clock must bear a well defined phase relationship with respect to the received

data so that the decision circuit samples the high and low levels *optimally*, that is, the rising edge of the generated clock falls in the midpoint of each bit. This is because, at this optimum sampling point, the signal level difference between logical one and logical zero is the largest. The other condition that must be met simultaneously is that the frequency of the generated clock signal must be equal to the data rate.

Satisfying these two conditions, as shown in Fig. 2.3, is called synchronized sampling. Since the SNR is dependent on the choice of the sampling instance, synchronized sampling ensures that the output SNR is high. The task of generating such a clock from the incoming data is called clock recovery. The overall operation of clock recovery and data cleanup is called clock and data recovery (CDR).

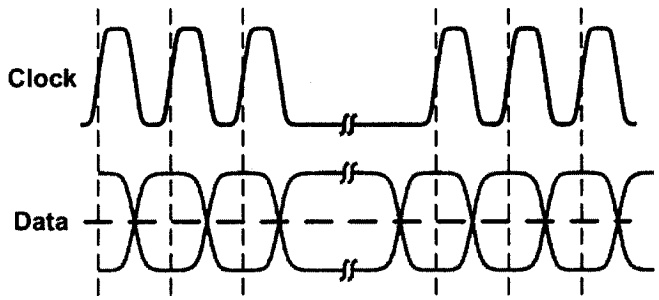

Fig. 2.3 Synchronized sampling by a clock and data recovery circuit.

The front-end directly impacts both the sensitivity and the speed of the overall system. This is due to the noise, gain, and bandwidth of the TIA and the LA, and the non-idealities introduced by the photodiode. The CDR must provide high data rates, tolerate long runs of ones and zeros known as consecutive identical digits (CIDs), and satisfy jitter and bandwidth.

2.2.3 Design Considerations

Some of the important design issues for CDRs include data format, jitter, line coding, speed, power dissipation, supply scaling, and fabrication technology, to name a few. While most of these design challenges are geared towards ASIC [1] design, we wish to draw the reader's attention to the design issues due to data format, jitter, and line coding (from a system level perspective).

[1] Application specific integrated circuit.

Data Format

The data format employed in most high-speed applications is the binary sequence non-return to zero (NRZ) data. This type of waveform is preferred to a popular data format - return to zero (RZ), for which the reason shall become apparent. As depicted in Fig. 2.4, each bit of RZ data consists of two parts. The first part assumes a value that represents the bit value whereas the second part is always equal to logical zero [1].

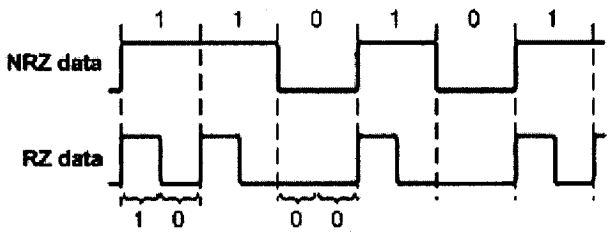

Fig. 2.4 NRZ and RZ data formats. NRZ: non-return to zero; RZ: return-to-zero.

As expected, RZ data exhibits a high transition density and therefore produces a spectral component (an impulse) at the bit rate frequency which simplifies the task of generating a clock at the same frequency. This is in contrast to NRZ data which lacks such a spectral component and may contain a large number of CIDs. The spectra of NRZ and RZ data formats are shown in Fig. 2.5.

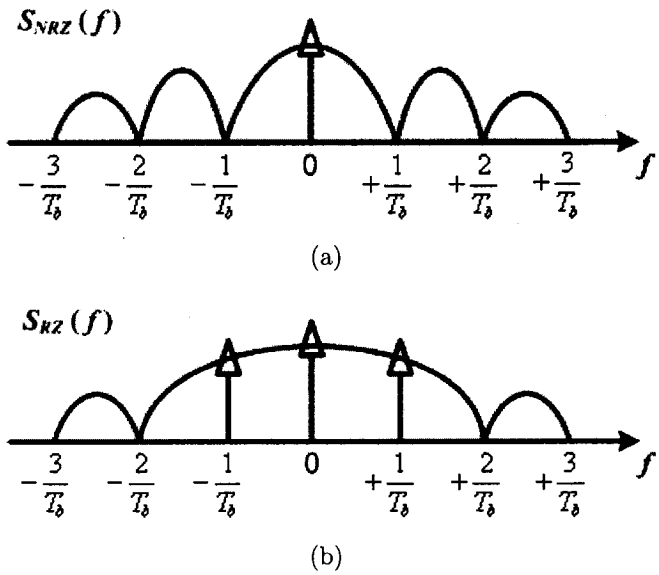

Fig. 2.5 Spectrum of (a) NRZ data format and (b) RZ data format [1]. NRZ: non-return to zero; RZ: return-to-zero; T_b: bit period; f: frequency; $S_{NRZ}(f)$: power spectral density of NRZ data in logarithmic scale; $S_{RZ}(f)$: power spectral density of RZ data in logarithmic scale.

From this discussion, we can draw the conclusion that the task of clock recovery is easier in the case of the RZ data format than that of the NRZ data format. There are two reasons behind this. Firstly, if a data stream contains a large number of CIDs, the clock generated by the CDR may start to drift in phase and frequency due to the absence of data transitions for reference. Secondly, the absence of a spectral component at the bit rate frequency and the presence of nulls at integer multiples of the bit rate frequency in the spectrum of NRZ data format poses a problem. The CDR can lock to these spurious signals instead of the bit rate frequency or not at all [3].

However, the main drawback of RZ data format is its inefficient use of bandwidth. In fact, the RX data format uses twice as much bandwidth as the NRZ data, intensifying the trade-offs in circuit design [1].

Jitter

Jitter is defined as a measure of the short term time variations of the significant instances of a digital signal from its ideal position in time [4]. OC systems inherently introduce jitter

with the prime sources being optical line generators and digital multiplexers - each containing CDRs. If the jitter is not suppressed, the data can undergo heavy SNR degradation and thereby poor BERs. Hence, CDRs in addition to their primary task, must minimize the jitter in a system.

Jitter can be measured as the rms value of the difference of the interval between two consecutive zero crossings of the signal and a constant time period (cycle jitter), or the rms value of the difference of two consecutive samples of such interval (cycle-to-cycle jitter) [2].

The SONET standard specifies three measures of jitter performance in a receiver to maintain an acceptable jitter in the system [2]. These measures are jitter generation, jitter transfer, and jitter tolerance, which are all strongly inter-related.

- **Jitter generation** is a measure of the maximum allowable jitter generated by a system. In CDRs, jitter is mainly generated by noise in the local oscillator (see Section 2.4.1) and the ripple in its control lines.

- **Jitter transfer** is a parameter specifying the amount of jitter suppressed from the input signal to the output signal. It is defined as the ratio of output jitter to input jitter at a specific jitter frequency [5]. Jitter transfer is used to specify the performance of CDRs.

- **Jitter tolerance** is a measure of the ability of a receiving device to correctly detect incoming data. It can be defined as the amplitude of the incoming jitter that causes the BER of the recovered data to exceed a specified limit [5]. From the perspective of CDRs, jitter tolerance quantifies the ability of the CDRs to respond to changes in data phase by quickly and effectively altering the phase of the clock signal from synchronized sampling [3] (see Fig. 2.3).

Line Coding

Random data can contain long sequences of CIDs. As stated earlier, this creates problems for the CDR as the local oscillator starts to drift in phase and frequency, thereby generating jitter. Also, CIDs exhibit nonzero "running average" (a nonzero dc component) which is blocked by high-pass filtering, creating difficulties in ac coupling stages [1].

Line coding techniques can be used to encode the random data so as to prevent long periods of low transition density. Some popular line coding schemes include 8B/10B, 6B/8B,

4B/5B, and Manchester-encoding, to name a few. The cost associated with these line coding schemes is bandwidth. Nonetheless, it has been accepted for reliable communications. For example, 8B/10B is employed in SONET OC-48.

2.3 Continuous-Mode Receivers

A large number of optical communication systems are based on synchronous optical networking with point-to-point (P2P) optical links for communicating information. In synchronous networking, the exact rates that are used to transport the data are tightly synchronized across the entire network which is made possible by atomic clocks [6]. The undeniable advantage of this is that the amount of buffering required between each element in the network is greatly reduced.

The most widely employed standards for synchronous optical networking include the synchronous optical networks (SONET) or synchronous digital hierarchy (SDH); SONET in the U.S. and Canada, SDH in the rest of the world.

Today's standard optical receivers are designed to recover data from P2P optical links in SONET and SDH, which are digital in nature and use on-off keying (OOK) - binary modulation to represent digital data as the presence or absence of a carrier wave. In OOK, a binary one is represented as the presence of a carrier for a specific duration while a binary zero is represented by the absence of the carrier for the same duration. Although attractive for its simplicity, OOK is not spectrally efficient due to the abrupt changes in amplitude of the carrier wave [7].

As shown in Fig. 2.1, optimum bandwidth efficiency is achieved by massively multiplexing data from many sources by means of time division multiplexing (TDM) or wavelength division multiplexing (WDM). The synchronicity and network topology of SONET/SDH networks underline their three main characteristics namely: (1) continuous transmission of data, (2) same source used to generate data transmitted over the link, and (3) same P2P link used for data communication. The first characteristic gives the continuous wave nature to the optical data seen by the receiver, while the latter two give the received data two distinct features making it continuous mode [3].

Since the data is generated by the same source, it is consistent in phase from bit-to-bit and the transmitted power at the source is the same for all data. Furthermore, as the data travels over the same optical link, the data undergoes the same amount of attenuation or

amplification. Also, the data undergoes equal delay over the link so that the phase of the received data never varies significantly. The overall outcome of these effects leads to: (1) the data does not have any phase variations, and (2) the data has the same optical power levels at the receiver indicating a logical one or a logical zero - no amplitude variations.

Given these two characteristics, continuous-mode optical receivers (CM-RXs) are optimized by design for specific power levels and phase.

2.3.1 Continuous Mode Clock and Data Recovery

There exists a large amount of literature on different architectures for CM-CDR. The two most common groups of CM-CDR architectures include open-loop CDRs and phase-locking CDRs.

Open-Loop CDR Architectures

As discussed in Section 2.3.1, the spectrum of NRZ data lacks a spectral component at the data rate. However, techniques exist to extract the frequency of the data from the spacing between data transitions (rising and falling edges). Fig. 2.6 shows a CDR based on an open-loop architecture.

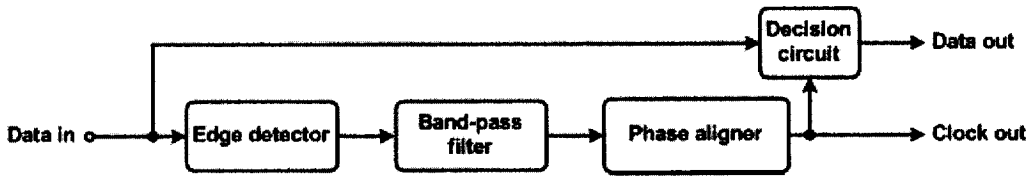

Fig. 2.6 Spectral line clock and data recovery [2].

The input data signal is fed to an edge detector. Within the edge detector, the data signal is passed through a delay circuit. The XOR gates operates on the data signal and its delayed replica. The output waveform of the XOR gate contains the information about the edges of the input data signal. The edge-detected waveform is passed through a band-pass filter that is tuned to the clock frequency. It is essential that the filter has very high selectivity to suppress the unwanted data-dependent signal that results in amplitude and phase modulation in order to suppress jitter [2].

The recovered clock signal is obtained from the output of the band-pass filter. To recover the data, the recovered clock can be used to sample the input signal in conjunction with a decision circuit. However, to ensure that the output clock signal samples the data at its optimum point, the recovered clock must be fed to a phase aligner.

Although the low complexity associated with open-loop CDRs makes them attractive, there are two main associated drawbacks with this architecture. Firstly, this technique provides limited phase tracking ability and therefore poor jitter tolerance. Secondly, the highly selective nature of the band-pass filter at high frequencies is not easy to achieve during fabrication - calling for an off-the-chip implementation. This is not acceptable for high speed applications due to the high loss and latency associated with it.

Phase locking CDR Architectures

A very popular method for CDR is based on phase-locked loops (PLLs). PLLs are popular because of their versatile and self-sufficient nature. Fig. 2.7 shows a generic representation of a PLL based CDR architecture.

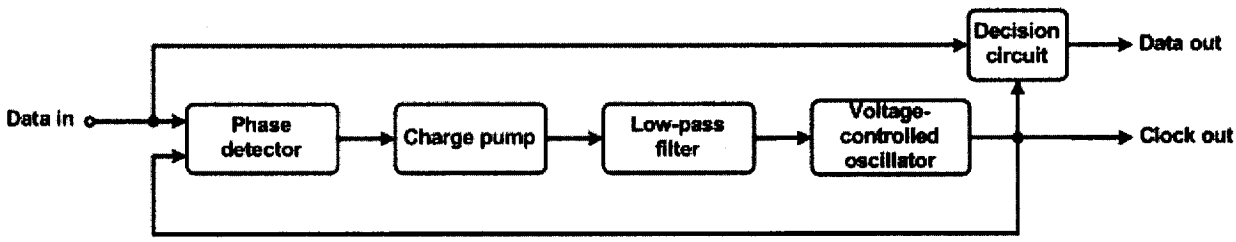

Fig. 2.7 Generic phase-locking recovery CDR architecture.

Clock and data recovery is accomplished by synchronizing the phase and frequency of the input data to a clock signal generated by a voltage-controlled oscillator (VCO) embedded within a feedback control loop. The phase detector compares the phase and frequency of the clock to that of the incoming data. This error signal is passed through a charge pump and a low-pass filter (LPF) to set the voltage required by the VCO to oscillate at the frequency of interest.

The idea of this system is based on negative feedback. The phase detector compares the edge of the input data with respect to the clock edge. If the data leads the clock, an error signal is generated such that the VCO frequency and thus the clock is sped up.

If the data lags the clock, an error signal of opposite polarity is generated such that the VCO frequency and therefore the clock is slowed down. Hence, frequency 'jumps' in the input can be replicated in the PLL if they are within the frequency capture range of the device [3]. The loop is said to be in "phase-lock" (steady-state) when the clock and data phase are at predetermined small constant offset [2]. Under this condition, the derivatives of their phases (frequencies) are equal. For synchronized sampling as shown in Fig. 2.3, the ideal phase offset is π rads, with clock transitions in the middle of the data eye for maximum SNR.

2.4 Burst-Mode Receivers

We stimulate the discussion on this topic by first presenting the key differences between conventional CM-RXs and BM-RXs which are based on the type of data formats they are designed to handle. This will drive the discussion on the design challenges and the possible solutions for next generation BM-RXs. We then present different design architectures for BM-RX front-ends and BM-CDRs.

2.4.1 Burst-Mode Challenges

Continuous-mode versus Burst-Mode

In general, there are three types of signal formats in digital communication systems as shown in Fig. 2.8. These include the continuous-mode data, the burst-mode data, and the burst and packet-mode data.

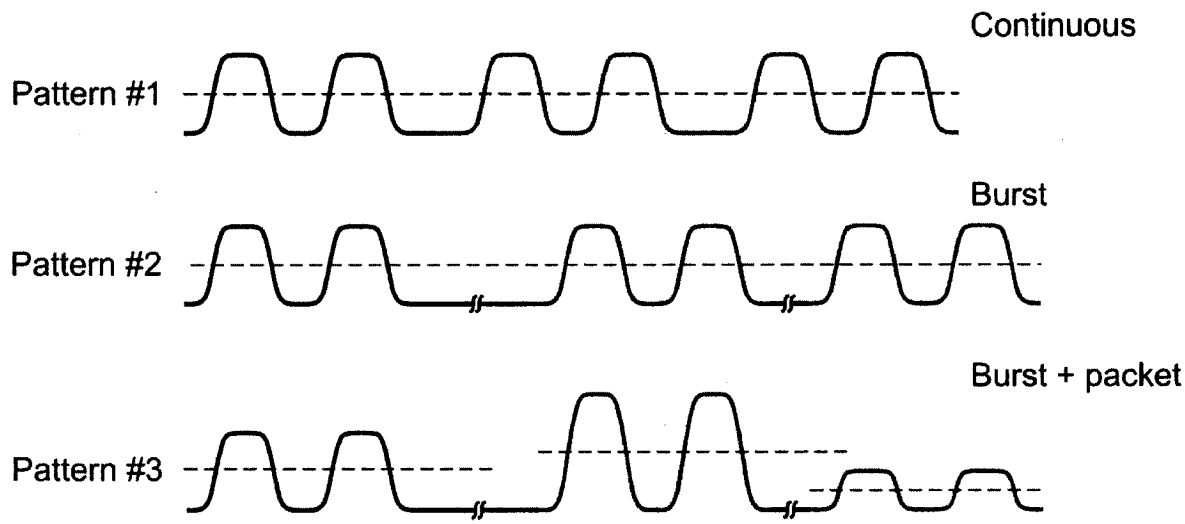

Fig. 2.8 Three data formats in digital communication: continuous-mode data, burst-mode data, and burst and packet-mode data [8].

Data in continuous-mode signal format is a binary sequence with an approximately balanced ratio of ones and zeros and where the interval between any two logic transitions is strictly limited. In burst-mode data, the sequences have the same amplitude for the same logic symbols with no restriction on the intervals between the logic transitions. The ratio of ones to zeros is also not constrained. These types of data formats have applications in P2P data links.

The data format that arises in multiaccess networks is the burst and packet mode. The main characteristics of this data format are that the signal amplitude may vary from packet to packet and the intervals between the packets can be arbitrary.

Conventional CM-RXs are designed to recover data in the continuous-mode format. On the other hand, the task of the BM-RX is to recover data in the burst-mode and burst and packet-mode formats. The objective of this thesis is focused on BM-RXs. For simplicity, we will refer to pattern #1 and pattern #2 as simply "burst-mode data".

There are two main attributes that differentiate CM-RXs and BM-RXs. These attributes arise from the type of data format that each one is inherently designed for. Firstly, the main difference is that in BM-RXs, dc-coupling is used whereas CM-RXs are ac-coupled [8]. The reason behind this is that BM-RXs must adapt to the amplitude of the received signal (in a very short time) by allowing the threshold setting of the receiver

circuitry to change accordingly.

This is not the case for CM-RXs where the finite charge and discharge times of the capacitors place the constraint that the average amplitude of the received data not vary rapidly with time. Since ac-coupling is employed in CM-RXs, they in general have a higher sensitivity than that of BM-RXs.

Secondly, the task of clock and phase recovery by a BM-CDR must be performed very quickly due to the varying phases of the packets and the large number of CIDs in each burst. This is not a critical requirement for CM-RXs where the data has a set phase variation and an equiprobable data transition density. The key differences between CM-RXs and BM-RXs are summarized in Table 2.1.

Table 2.1 Comparison of continuous-mode receivers and burst-mode receivers [8].

	Continuous-mode	Burst-mode
Signal coupling	ac	dc
Threshold setting	Fixed	Adaptive
Amplitude and clock recovery	μs	ns
Access time for receiver	μs	ns

Burst-Mode Problem & Solution

Optical multiaccess network based on all-optical core have a point-to-multipoint (P2MP) topology. These networks have two main characteristics: (1) they support multiple users who share the same fiber infrastructure, and (2) the P2MP optical links create optical path differences. It follows that data bursts originate from various sources and travel different distances, inherently causing the packets of data to vary in phase, frequency, and amplitude - burst-mode traffic. The amplitude and phase of successive packets may therefore vary anywhere between $0 - 20$ dB and $-\pi$ to $+\pi$ rads, respectively. This consequently creates new challenges for the design of optical receivers. The task of amplitude recovery is handled by the BM-RX front-end as shown in Fig. 2.9(a), whereas the BM-CDR performs the task of phase and frequency recovery as depicted in Fig. 2.9(b).

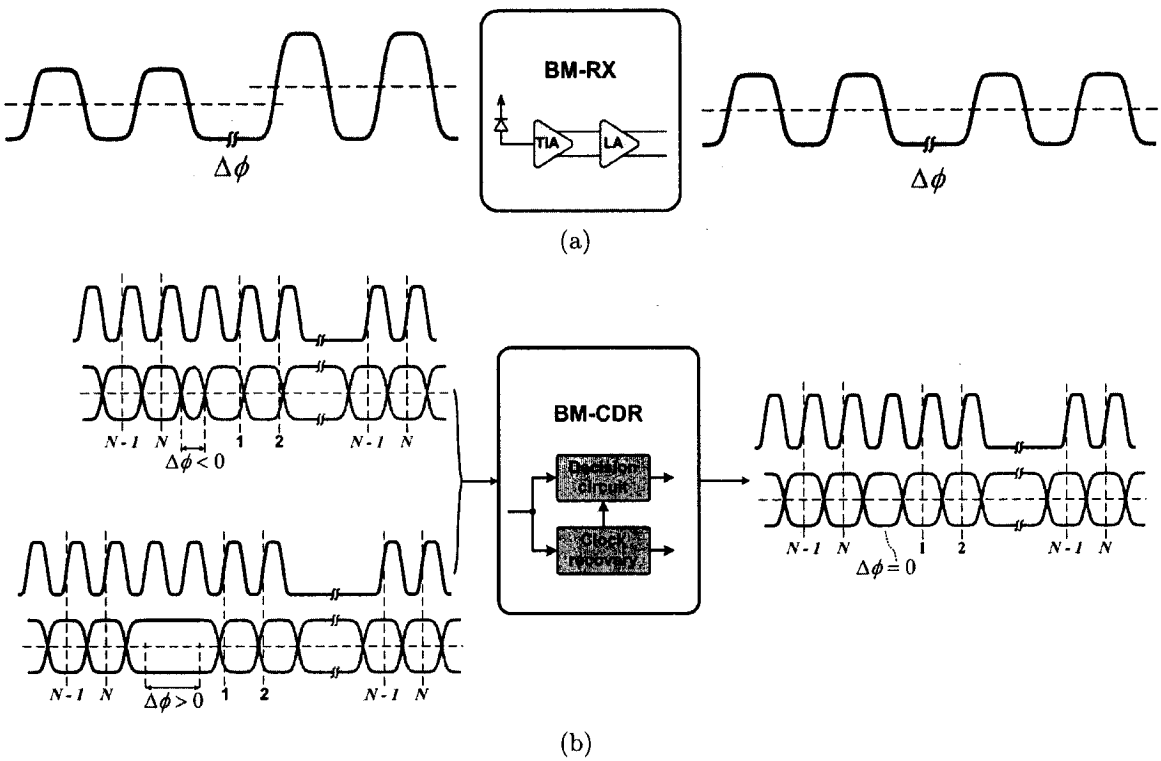

Fig. 2.9 Burst-mode solution. (a) Front-end handling the task of amplitude recovery. (b) Burst-mode clock and data recovery handling the task of phase and frequency recovery.

2.4.2 Burst-Mode Receiver Front-Ends

Over the past decade, researchers have presented impressive BM-RX front-ends [9] - [13]. These front-ends have been classified according to the way the threshold is set. They are categorized under two main types: feedback architectures [9] and feedforward architectures [12]. Examples of these two types are shown in Fig. 2.10.

In front-ends employing the feedback, the threshold is determined completely from the preamble field and held constant in the data field [12], [13]. This is not the case with feedfoward type front-end architectures, where the threshold is adaptively determined according to the input data signal [9] - [11].

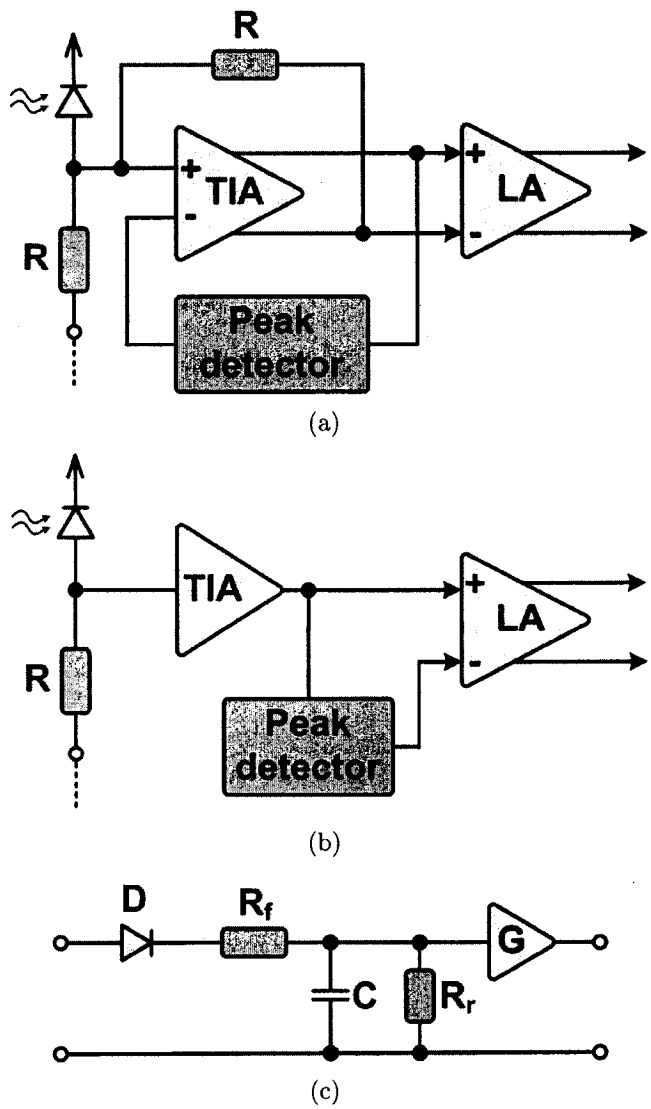

Fig. 2.10 Two types of front-ends for burst-mode receivers [8]. (a) Feedback type front-end. (b) Feedforward type front-end. (c) Peak detection circuitry. TIA: trans-impedance amplifier; LA: limiting amplifier.

Feedback Front-End Architecture

In the feedback type front-end architecture, amplitude recovery is done in the TIA. The architecture uses a differential input/output TIA with a peak detection circuit forming a feedback loop. The peak detector circuit determines the instantaneous detection threshold of the incoming data signal. Further amplification to drive the CDR circuit is achieved by the LA which is the dc-coupled output of the TIA.

This architecture is inherently more stable than the feedforward type since the feedback loop enables the receiver to work more reliably [8]. However, the drawbacks associated with this architecture are: (1) the design complexity at the circuit level associated with it, and (2) the fact that the TIA has to be differential at the input and output implying more power. The differential input/output TIA also ensures that the additive noise introduced in the signal by the circuitry is minimized due to a better common-mode rejection ratio, consequently, making the task of the CDR easier.

Feedforward Front-End Architecture

In the feedforward front-end architecture, amplitude recovery is done in the LA. In this architecture, the first stage is comprised of a conventional dc-coupled TIA. After the preamplification, the signal is fed into a peak detection circuitry to extract the amplitude information of the received packets. The threshold level is set adaptively for the LA which is dc-coupled at the output of the TIA. Stability is the main issue of feedforward front-ends and therefore the circuitry needs to be carefully designed to prevent oscillations [8].

2.4.3 Burst-Mode Clock and Data Recovery

Over the last decade, a number of impressive techniques for BM-CDRs with short phase acquisition times in point-to-multipoint systems have been proposed [12] - [21].

The first approach is based on a correlation algorithm [12] where phase acquistion is achieved by correlating phase-delayed versions of a local oscillator against the phase of the incoming data. This technique achieves lock within three bits, assuming a predefined unique preamble. It also has the ability for high jitter rejection. However, due to limited phase correlation depending on the granularity of the design, sampling at the optimum point is not guaranteed. This gives rise to unpredictable variations in BER from one burst of packet to the other.

The second approach is based on gated oscillators or some kind of gating circuit [16] - [18]. These BM-CDRs perform clock phase alignment by triggering the local clock on each transition of the input. Although the phase acquisition is instantaneous, this solution does not filter out input jitter and is susceptible to pulse distortions.

The third approach is PLL-based CDRs that reduce the settling time by increasing the bandwidth. However, the disadvantages include stability issues, jitter peaking, and limited jitter filtering [14], [15]. It has been suggested that one workaround consists in using dynamic loop bandwidth. This entails that the bandwidth is increased while the CDR is acquiring lock and restored to its original value for the rest of the packet to minimize output jitter [15]. However, this workaround is based on the assumption that an additional control logic or a reset signal is acceptable [22].

The last approach is based on over sampling either in time or space [19] - [21]. Over sampling in the time domain is achieved by sampling the input data at a higher frequency than the bit rate. This requires faster electronics. Over sampling in space is achieved by making use of multiple phase of the local clock. However, it has to be guaranteed that there is low skew between the multiple phases of the clock.

In the following sections, we present and discuss these well-known designs in detail.

Correlation Algorithm Based Burst-Mode CDRs

A clock recovery technique for burst-mode systems based on a correlation algorithm was first proposed in [12]. The idea is based on correlating phase-delayed versions of the local oscillator against the phase of the incoming data and using phase that provides the best match. This technique assumes that the preamble contains a specific 3-bit '0 1 0' pattern in each burst cell, and therefore used as a signature. Each of the generated clock phases are used to sample the data. The first clock phase to successfully recover the 3-bit '0 1 0' pattern is considered to sample the data in the center of the eye and thus used to recover the remaining burst.

The correlation algorithm is shown in Fig. 2.11(a). The block diagram for the burst-mode clock recovery system based on the use of a correlation algorithm is depicted in Fig. 2.11(b).

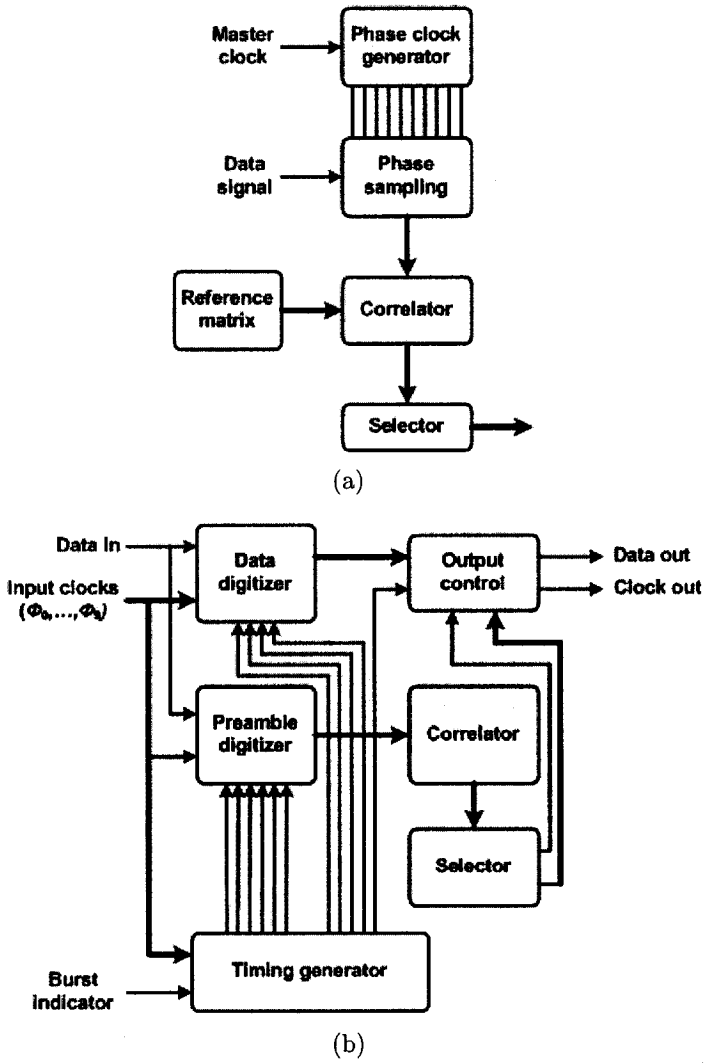

Fig. 2.11 Burst-mode CDR based on correlation algorithm [12]. (a) Correlation algorithm. (b) Block diagram for clock recovery system based on the use of a correlation algorithm.

A number of techniques have been proposed in the literature to generate multiple clock phases required for data sampling. These techniques include tuned or untuned tapped delay lines, multiple phase PLLs, or ring oscillators [23], [24]. The technique used with the correlation algorithm is based on external (LC) passive untuned tapped delay lines. This technique allows testing to be performed at various frequencies. The test setup for characterizing clock phase recovery characteristics of the clock phase correlator is shown in Fig. 2.12.

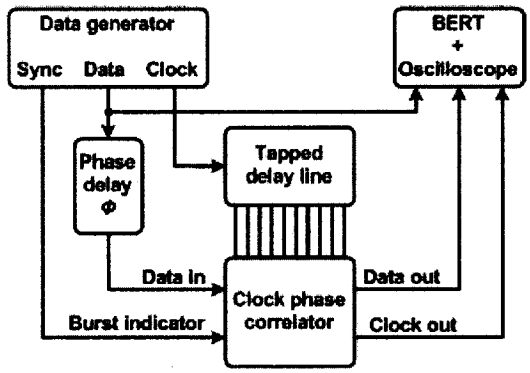

Fig. 2.12 Clock phase correlator test setup for characterizing clock phase recovery [12]. BBERT: burst bit error rate tester.

There is a tradeoff involved with the number of clock phases and the system performance in terms of BER. Although, operation with a few number of clock phases (down to three clocks) is possible with some loss in performance, the correlation algorithm is designed for operation with approximately ten evenly spaced clock phases. To generate multiple clock phases required by the algorithm, an external passive tapped delay line is used.

There are two undeniable advantages offered by this BM-CDR. Firstly, the clock phase alignment (CPA) field of the preamble is just three bits for phase recovery. Secondly, this technique achieves high jitter rejection because the data is retimed by a local oscillator. The main disadvantage of this BM-CDR is that the SNR and thus the BER of the device varies unpredictably from one burst of packet to the other burst of packet. This drawback arises from the limited phase correlation depending on the granularity of the design. Thus, sampling at the optimum point is not guaranteed but a phase error for sampling of data is assumed [3].

Gated Oscillators Burst-Mode CDRs

CDRs based on gated oscillators were first proposed in [18]. Since then, it has been adopted into BM-CDRs by many researchers [17], [25], [26]. This technique boasts instantaneous phase locking and tracking without the need of the CPA field of the data burst preamble. An application of clock recovery scheme using matched gated oscillators is shown in Fig. 2.13(a).

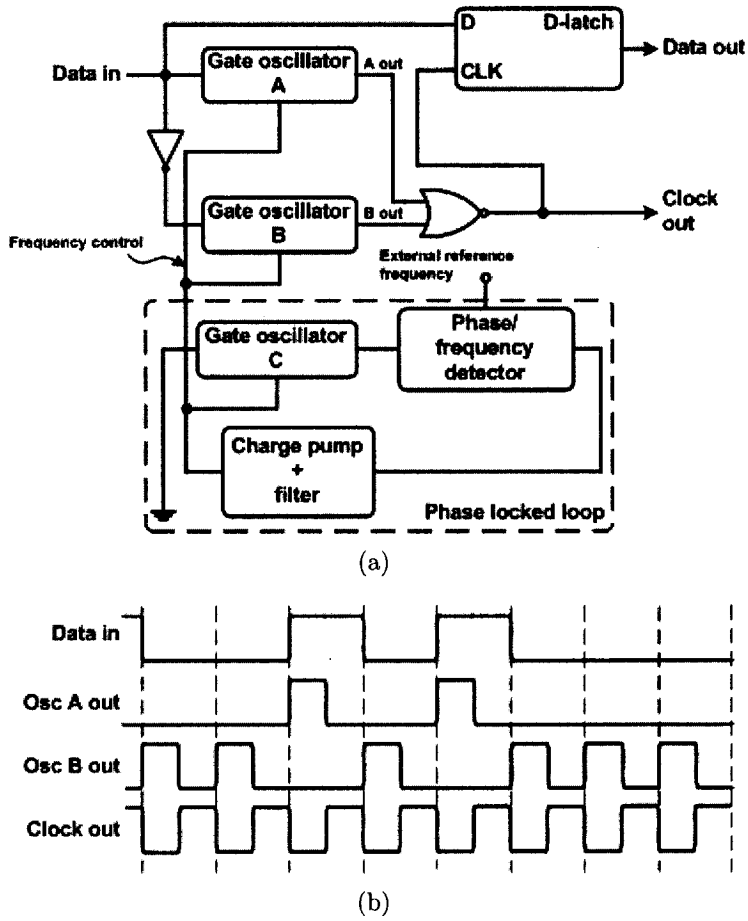

Fig. 2.13 Clock recovery scheme using matched gated oscillators [18].

The system contains two identical gated square-wave-oscillators. These oscillators have their output frequency matched to a good degree to the transmission rate of the incoming data signal. The oscillators are started and stopped successively by the input data signal

so that only one operates at a particular time. Fig. 2.13(b) shows an ideal response of the system for a typical input data bit stream. Each time an oscillator is started, the initial phase of oscillation is forced into phase synchronization with the input data signal. The recovered clock is generated by adding the outputs of the gated oscillators by a NOR gate. Data retiming is achieved by an output D-latch. The overall result is that the phase of the local oscillator is forcibly synchronized to that of the input data signal each time a transition occurs at the input data signal.

If there is a good match between the oscillator output frequency and the data rate, the output clock signal will hold a valid phase during the time between data transitions. This is also true even if large number of CIDs are present in the input data signal. If there is a small difference between the frequency of the oscillators and the data rate, the temporary phase errors that accumulate in the output clock signal are discarded when the oscillators are stopped. In the presence of errors, only a finite number of CIDs can be transmitted without making an error.

The role of the PLL as shown in Fig. 2.13(a), is to tune the gated oscillators with respect to a fixed external reference signal using a master-and-slave approach. To this end, the three identical oscillators are made frequency variable. The third matched oscillator (the master) is allowed to run continuously. It is connected inside the PLL which locks its output frequency to an external fixed reference signal. Since the same frequency control signal is shared by the slave oscillators, implementing the clock recovery system, the output frequency of all oscillators are at desired values.

Broad-Band Phase-Locked Burst-Mode CDRs

A very effective way to make CM-CDRs (based on PLL architecture) highly resistant to jitter caused by phase variations, is to design the PLLs with narrow bandwidths. This is why SONET CDRs are specified with a narrow PLL bandwidth in order to minimize jitter accumulation through long repeater chains in long-haul networks [4]. However, this comes at a price of other abilities: suppression of internal jitter from the VCO, frequency capture range, and phase/frequency acquisition time [14]. For example, the phase acquisition time of a commercially available SONET OC-48 CDR is measured at 1400 bits ($\pm\pi$ rad phase steps) [27] - clearly, not a solution for burst-mode applications.

In [14], it has been argued that fast phase acquisition can be obtained by modifying

the PLL parameters in a SONET CDR by increasing the loop bandwidth. The reason for the restriction on the narrow loop bandwidth can be relaxed, based on the fact that, in multiaccess networks that are typically deployed in metropolitan areas, there are few or no repeaters (minimal jitter accumulation). Fig. 2.14 shows a BM-CDR based on a broad-band PLL with a half-rate architecture.

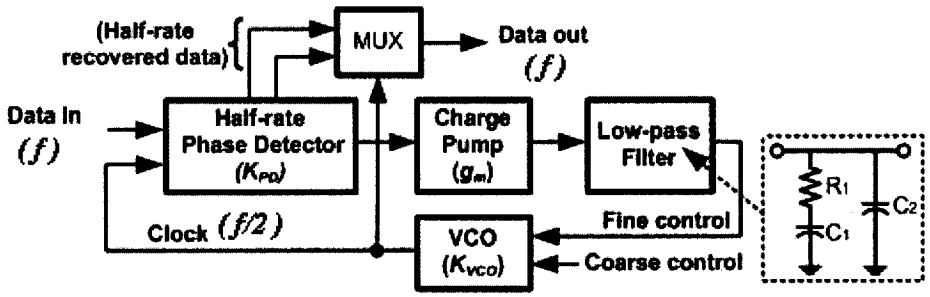

Fig. 2.14 Broad-band phase-locked loop with half-rate clock and data recovery architecture [14].

This solution achieves a phase acquisition time of 100 bits for $\pm\pi$ rad phase steps. This is more than a ten-fold improvement over corresponding SONET CDRs. It also has the added benefits of increasing the CDR's frequency capture range and suppression of internal jitter, as the PLL behaves as a high-pass filter for jitter generated by the VCO [28].

The drawbacks from this design spring from the fact that PLLs are: (1) unable to distinguish a true phase-step from cycle-to-cycle data jitter, and (2) more prone to clock drift when receiving data with low transition density. The associated drawbacks are: (1) increasing the loop bandwidth simultaneously increases the jitter transfer bandwidth, and (2) the need for a high transition density with line coding to eliminate low frequency components.

Over sampling Burst-Mode CDRs

A BM-CDR based on sampling the data at twice the bit rate (over sampling in time) with a novel picking algorithm has been proposed in [29], [30]. Fig. 2.15 shows a block diagram of such a BM-CDR.

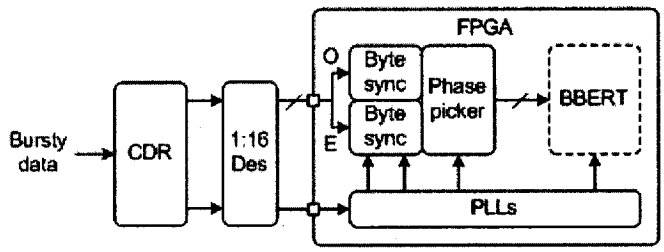

Fig. 2.15 Burst-mode clock and data recovery based on 2× over sampling and phase picking algorithm [29]. CDR: clock and data recovery; Des: deserializer; PLLs: phase-locked loops; BBERT: burst bit error rate tester.

The phase picking algorithm employed in this BM-CDR is based on a simple idea. More specifically, the algorithm uses the symmetry introduced by sampling at twice the bit rate. This allows the data bits to be sampled on odd samples or even samples. The odd bits of the recovered data from the CDR output are forwarded to path O and the even bits are forwarded to path E. The byte synchronizer is responsible for detecting the start of a packet (delimiter). The phase picking algorithm replicates the byte synchronizer twice in an attempt to detect the delimiter on the odd and even samples of the data respectively. The phase picker uses feedback from the byte synchronizers to select the right path. The overall result is that this BM-CDR achieves instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rad).

Since this design is built upon a CM-RX (SONET CDR), the BM-CDR inherits the excellent jitter characteristics that include: low jitter transfer bandwidth (1 MHz) and low jitter peaking (0.1 dB) [29].

2.5 Summary

The stringent specifications defined by optical standards pose difficult challenges to designers at the system level and the circuit level. These challenges are further aggravated by the problems introduced by the various network topologies. The continuous nature of data in P2P optical links require CM-RXs and CM-CDRs, whereas in P2MP links, the data is burst-mode, requiring BM-RXs and BM-CDRs. The research focus of this thesis is on BM-CDRs.

The BM-CDRs solutions that have demonstrated short phase acquisition times include:

correlation algorithm based CDRs, gated oscillators CDRs, broad-band PLL CDRs, and over sampling CDRs with phase picking algorithm. Table 2.2 summarizes the performance of the discussed BM-CDR solutions from system level perspective.

Table 2.2 Comparison of BM-CDR solutions with short phase acquisition times.

Performance	Correlation algorithm [12]	Gated oscillator [18]	Broad-band phase-locked [14]	2× oversampling algorithm [29]
Acquisition	3 bits	0 bits	~100 bits	0 bits
Complexity	high	simple	moderate	simple
Jitter rejection	medium	none	Low	high
Line coding	none	None	required	none
Sampling	not optimum	optimum	optimum	optimum
Tracking	limited	limited	good	excellent

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Chapter 3

Forward Error Correction for Digital Communications

The increasing demand of bandwidth for multimedia services has accelerated the need for large-scale, high-speed optical networks for the exchange, processing, and storage of digital information. However, information communicated from one point to another can be corrupted due to physical channel impairments (noise). Hence, there is a need for reliable communication. Error control coding (ECC) can help improve the reliability of the system but at the cost of bandwidth, making the network less efficient. In general, there is a tradeoff between efficiency and reliability of digital data transmission.

In this chapter, we present the concept and theory of forward error correction (FEC) techniques and in particular, review a class of nonbinary cyclic block codes called Reed-Solomon (R-S) codes. We also argue how the optical link budget of passive optical networks (PONs) can be increased by applying FEC with R-S codes in burst-mode clock and data recovery (BM-CDR) circuits for such networks.

3.1 Introduction to Communication

Claude Shannon in his pioneering work, "A Mathematical Theory of Communication" [1], stated that the fundamental problem of communication is that of reproducing at one point A either exactly or approximately a message selected at another point B.

The central paradigm of classic information theory is the engineering problem of transmission of information over a noisy channel. A communication system as depicted in

Fig. 3.1 consists of essentially six parts [1]:

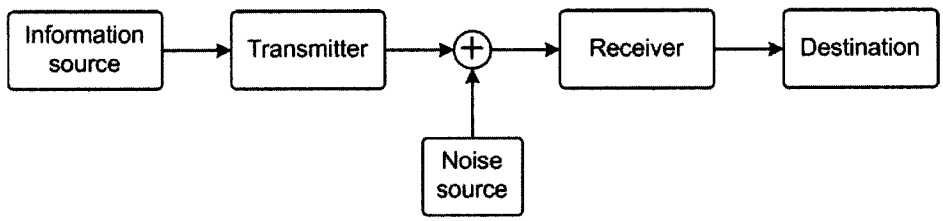

Fig. 3.1 Schematic of a general communication system.

1. An information source which creates or produces the information needed to be communicated.

2. A transmitter which in addition to transmitting the data, 'prepares' the information needed to be sent over a channel. The transmitter may encode the information before modulating and sending over a channel.

3. The channel which is a medium used to transmit the data from the transmitter to a receiver.

4. A noise source which though is not intended to be part of a communication system, inherently does become part of it. For example, a channel may introduce additive noise to the transmitted signal - Additive Gaussian Noise (AWGN).

5. The receiver which in addition to receiving the data, 'un-does' the operation (done by the transmitter) on the data, so that it is in a format understandable by the destination. This means that it demodulates the corrupted information which a decoder then processes to retrieve the original information.

6. The destination could simply be a user/system for whom the information is intended for.

Communication theory in itself is based on two giant pillars, namely, information theory and coding theory.

3.2 Information Theory

Information theory is concerned with the quantification of data with the overall objective of enabling as much data as possible to be *reliably* stored on a medium and/or communicated over a channel. The most fundamental results of communication theory are [2]:

- **Shannon's source coding theorem**, which establishes that, on average, the number of bits needed to represent the result of an uncertain event is given by its entropy. Information entropy is a measure of data and it is expressed by the average number of bits needed for communication or storage.
- **Shannon's noisy-channel coding theorem**, which states that reliable communication is possible over noisy channels provided that the rate of communication is below a certain threshold called the channel capacity. The channel capacity can be approached by using appropriate encoding and decoding systems.

Information theory has a number of important applications across a wide variety of fields. The applications include the feasibility of mobile phones, the development of Internet, the invention of the CD, the Voyager missions to deep space, the study of linguistics and of human perception, the understanding of black holes, musical composition, statistics, information retrieval, and numerous other fields [2]. The most important application of information theory is in the field of coding theory.

3.3 Coding Theory

Coding theory is involved with finding explicit methods, called codes, of increasing the efficiency and reducing the net error rate of data communication over a noisy channel to near the limit that Shannon proved is the maximum possible for that channel [3].

The two contrasting coding techniques, source coding (entropy encoding) and channel coding (error control coding), are the fundamental concerns of coding theory. In source coding, redundancy is removed (from data) to achieve higher *efficiency*, whereas in channel coding, redundancy is added (to data) to improve *reliability*. Clearly, there is a tradeoff between efficiency and reliability.

3.3.1 Source Coding

The basic idea behind source coding is that of data compression in order to transmit the data more efficiently. In its simplest form, data compression is achieved by reducing the redundancy present in the source and then representing the source with fewer bits that can carry more information.

Entropy of a source is the measure of information. Various techniques used by source coding schemes try to achieve the limit of entropy of the source [3]

$$C(x) \geq H(x) \tag{3.1}$$

where $H(x)$ is entropy of source (bitrate), and $C(x)$ is the bitrate after compression. In particular, no source coding scheme can be better than the entropy limit of the symbol.

An important application of source coding is to reduce the Internet network load by making file sizes smaller (for example "zip" data compression).

3.3.2 Channel Coding

The principle behind error correction is to add extra data bits, called redundancy bits, to make the transmission of data more robust to disturbances present on the transmission channel. There are fundamentally two categories of techniques for improving reliability in a communication system, namely, forward error correction (FEC) or automatic repeat request (ARQ). The block diagram in Fig. 3.2 depicts a digital communication process with channel coding.

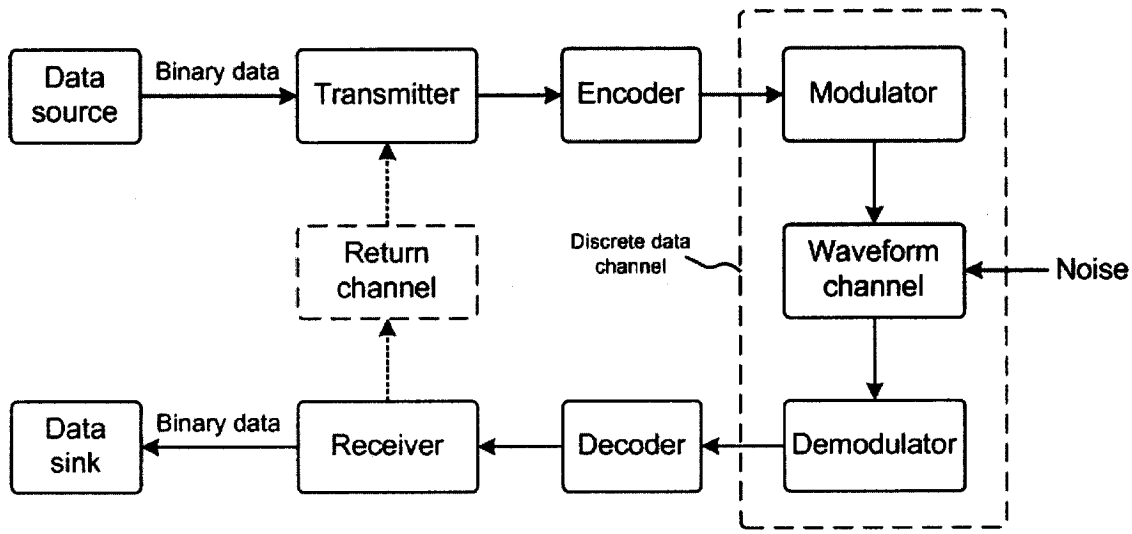

Fig. 3.2 Digital communication process using error correction [4]: automatic repeat request (with the return channel) and forward error correction (without the return channel).

Automatic Repeat Request

In a communication system employing ARQ, error detection and 'correction'[1] (at receiver) is achieved by acknowledging the receipt of correct data or by requesting for retransmission in case of corrupted data, via a "return channel" from the receiver to transmitter - feedback path.

More specifically, the data (block/packet) sent over the channel, is stored at the source until an acknowledgment or a retransmission request is received. If there are no discrepancies, the block is delivered to the data destination and the receiving terminal notifies the ending terminal, through a suitable return channel, that the block has been correctly received. However, if discrepancies exist, the sending terminal is so notified and the block is retransmitted [4].

The advantage of ARQ over FEC is that error detection requires much simpler decoding equipment than does error correction. Another plus point of ARQ is its adaptive nature that makes it an attractive technique for channel coding as retransmission of information only

[1] In systems with ARQ, strictly speaking, errors are not corrected but the information is resent if errors are detected.

occurs in case of errors. However, the major drawback of ARQ arises when the channel error rate is high. In this case, frequent retransmissions are required, hence, lowering the system throughput[2] considerably. In these circumstances, FEC becomes a preferred candidate for channel coding.

Forward Error Correction

In Fig. 3.2, if the return channel is removed, the system becomes a one-way system - transmission is strictly in one direction, from transmitter to receiver with no feedback. Error correction for a one-way system must be accomplished using FEC, that is, by employing error-correcting codes that automatically correct errors detected at the receiver.

The concept behind FEC is to "average noise" present in the channel. This is achieved by making use of a predetermined algorithm when adding redundancy to the transmitted information. In this way, each redundant bit added is invariably a complex function of many original information bits making each data bit affect many transmitted symbols. Consequently, the corruption of some symbols by noise allows the original user data to be extracted from the other, uncorrupted received symbols that also depend on the same user data. This so called "risk-pooling" effect, makes digital communication systems that use FEC, work perfectly above a certain minimum signal-to-noise ratio (SNR) and not at all below it. This tendency becomes even more pronounced as stronger codes are used that more closely approach the theoretical limit imposed by the Shannon limit [5].

The family tree depicted in Fig. 3.3 shows the different types of FEC codes. In literature, the two categories that are most widely discussed, are the linear block codes and the convolution codes. While block codes work on fixed-size blocks (packets) of bits or symbols of predetermined size, convolutional codes work on bit or symbol streams of arbitrary length.

[2]Rate at which newly generated messages are correctly received [4].

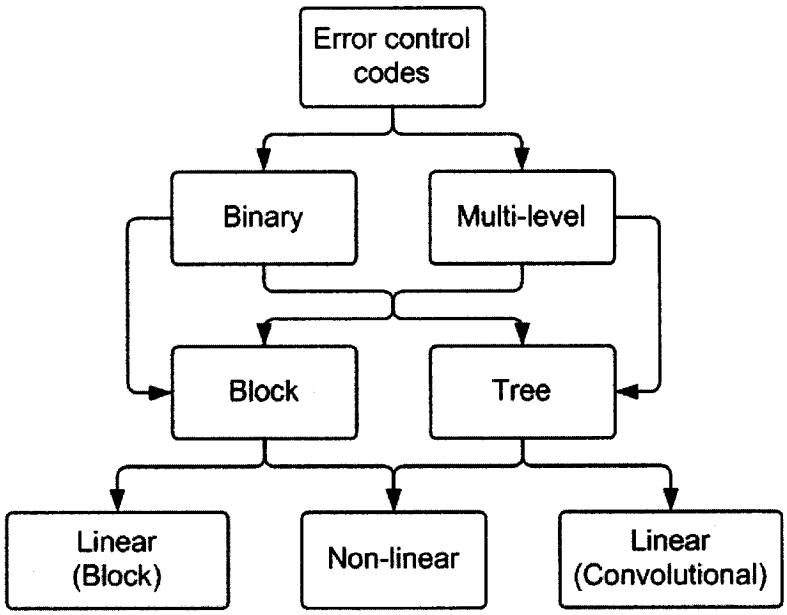

Fig. 3.3 Family tree of error correcting codes [6].

There are many types of block codes including Hamming codes [7], Bose-Chaudhuri-Hocquenghem (BCH) codes [8], [9], and Reed-Solomon (R-S) codes [10]. While the BCH and Hamming codes are binary, R-S codes are multi-level. R-S codes have great power and utility with numerous applications including data storage systems, high-definition TV, CD and DVD players, data transmission, and satellite transmission (Voyager) [11].

3.4 Reed-Solomon Codes

R-S codes are nonbinary cyclic codes, and are a special case of BCH codes. R-S codes operate on blocks of data in which information is divided into frames/blocks (see Fig. 3.4) with symbols made up of m-bit sequences, where integer $m \geq 2$. R-S(n, k) codes on m-bit symbols exist for all n and k for which [12]

$$0 < k < n < 2^m + 2 \tag{3.2}$$

where k is the number of information symbols (input per block) being encoded, and n is the total number of code symbols in the encoded block (that the encoder outputs). For

most conventional R-S(n, k) code [12],

$$(n, k) = (2^m - 1, 2^m - 1 - 2t) \tag{3.3}$$

where t is the symbol-error correcting capability of the code, with $2t$ being the number of parity symbols given by

$$2t = n - k \tag{3.4}$$

The structure of a typical R-S(n, k) codeword is shown in Fig. 3.4. The R-S(n, k) codeword is often referred to as a systematic code because the data is left unchanged and the parity symbols are appended.

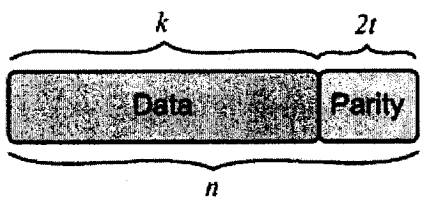

Fig. 3.4 Structure of a Reed-Solomon codeword – R-S(n, k) with k data symbols, $2t$ parity check symbols, and n the number of encoded symbols in the block.

Hamming distance, the minimum distance, d_{min} between two codewords, is defined as the number of symbols in which the sequences differ. R-S codes achieve the *largest possible* code minimum distance for any linear code with the same encoder input and output block lengths. For R-S codes, the code minimum distance is given by [13]

$$d_{min} = n - k + 1 \tag{3.5}$$

The code is capable of correcting any combination of t or fewer errors, where t can be expressed as [12]

$$t = \left\lfloor \frac{d_{min} - 1}{2} \right\rfloor = \left\lfloor \frac{n - k}{2} \right\rfloor \tag{3.6}$$

where $\lfloor x \rfloor$ means the largest integer not to exceed x. Equation (3.6) illustrates that for the case of R-S codes, correcting t symbols requires no more that $2t$ parity symbols. Hence,

for each error, one redundant symbol is used to locate the error, and the other redundant symbol is used to find its correct value.

The erasure- correcting capability, ρ, of the code is [12]

$$\rho = d_{min} - 1 = n - k \tag{3.7}$$

Any linear code is capable of correcting $n-k$ symbol erasure patterns if the $n-k$ erased symbols all happen to lie on the parity symbols. However, R-S codes have the remarkable property that they are able to correct *any* set of $n-k$ symbol erasures within the block. R-S codes can be designed to have any redundancy. However, the complexity of a high-speed implementation increases with redundancy. Thus, the most attractive R-S codes have high code rates (low redundancy) [12].

3.5 FEC with R-S Codes for PON Burst-Mode Receivers

The PON infrastructure can be regarded as a communication channel. There are two main issues that need to be addressed: (1) the bit error ratio (BER) performance of the PON that is set by the SNR of the data signal at the decision circuit, (2) the maximum physical reach of the optical link from an optical network unit (ONU) to the central office (CO) and also the upper bound on the split ratio (number of ONUs supported from one power splitter/combiner). We discuss the two issues briefly.

The BER is degraded by errors introduced by intrinsic effects and/or extrinsic effects in the channel. The extrinsic effects are due to various physical channel impairments, such as, fiber attenuation and dispersion, to name a few. Intrinsic effects arise due to random Gaussian noise which is always present at the receiver that affects the determination of the decision threshold and introduces sensitivity penalty for the receiver. AWGN also affects the transitions of the data, translating to jitter. This affects the sampling instance of the BM-CDR and thereby the zero/one decision. The other intrinsic effect that degrades the BER performance is the finite charging/discharging time of the adaptive threshold circuitry in the BM-RX [14].

Current PON systems employ Fabry-Perot (FP) laser, a multi-longitudinal mode (MLM) device, at the ONU. The reasons for this is that FP lasers provide the most cost effective solution for meeting the PON requirements - the optical power required for a 20 km reach

PON system in the 1310 - 1550 nm range [15]. However, performance of the optical fiber system may be severely impaired by the mode partition ratio (MPN) [16], [17] of a FP laser coupled with the chromatic dispersion that exists in the transmission fiber. Thus, MPN introduces a limitation in the length of the optical link.

The above mentioned issues can be addressed by employing FEC in PONs. The advantage of FEC is that retransmission of data can be avoided as in ARQ, and is therefore applied in situations where transmissions are relatively costly or impossible (as in PONs). Consequently, the solution is provided by the resulting coding gain.

Coding gain is defined as the measure in the difference between the SNR levels between the uncoded system and coded system required to reach the same BER levels when used with an error correcting code. However, coding gain is obtained at the expense of higher bandwidth.

Another interesting concern is the presence of *burst-errors* in PONs. Burst-errors arise during the finite phase acquisition process by BM-CDRs for bursty and packet mode data. It is well known that R-S codes are extremely well suited for burst-error correction, making them an attractive choice for application in PONs.

The reason why R-S codes perform well against burst-noise is based on its clever encoding/decoding algorithms. An R-S(n, k) code can correct up to t symbol errors as given by (3.6) present *anywhere* in the codeword. That is, the R-S decoder will correct by replacing a corrupted symbol with a correct one, whether the error was caused by one bit being corrupted or all bits in the symbols being corrupted. Thus, if a symbol is wrong, it might as well be wrong in all of its bit positions. This gives an R-S codes a tremendous burst-noise advantage over binary codes [12].

3.6 Summary

In a noisy channel, the information communicated from point A to point B, can be encoded by adding 'additional' information, that can be used to detect, and correct errors in transmission. However, the more 'additional' information we add, the more *reliably* we can detect and correct errors, but the less *efficient* we become at transmitting and therefore receiving the 'actual' information. Hence, there is a tradeoff between the reliability (source coding) and efficiency (channel coding), which in itself forms the basis of communication.

FEC implementation with R-S codes can help increase the optical link budget of GPONs

by: (1) improving the system performance at a targeted SNR, (2) reducing the penalty due to MPN when using MLM lasers in ONUs, and thus increasing the split ratio, (3) achieving longer physical reach between ONUs and the CO, and (4) eliminating burst-errors making the BERs independent of the phase difference between successive packets (see Chapter 4).

As the hardware costs decrease and as the system complexities increase, coding schemes in general, will be routinely employed in digital communication links. There are three main reasons suggested for this [18]:

1. Phenomenal decrease in the cost of digital electronics.
2. Significant improvements in various decoding algorithms.
3. Much slower (or no) decrease in the cost of analog components, such as power amplifiers, antennas, to name a few.

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Chapter 4

Experimental Demonstration of FEC in Burst-Mode CDRs with Instantaneous Phase Acquisition for Burst-Error Correction in GPONs

We demonstrate experimentally for the first time the impact of forward error correction (FEC) on the performance of 622/1244 Mb/s burst-mode clock and data recovery (BM-CDR) with instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rads) for gigabit-capable passive optical network (GPON) optical line terminator (OLT) applications with (255,239) Reed-Solomon (R-S) decoding. Our design is based on commercially available SONET CDRs operated in 2× over sampling mode. This burst-mode receiver (BM-RX) provides a 5 dB coding gain at a bit error ratio (BER) of 10^{-10}. We also show how our solution, using R-S codes and a BM-CDR with fast phase acquisition, gives reliable and predictable BERs for bursty channels. We demonstrate this with our novel burst bit error rate tester (BBERT) that achieves instantaneous synchronization with the incoming pattern. The BM-RX meets the GPON physical media dependent layer (PMD) specifications and transmission convergence layer (TC) specifications defined in International Telecommunication Union-Telecommunication Standardization Sector (ITU-T) recommendations G.984.2 and G.984.3 standards, respectively. The 5 dB improvement in coding gain can be used to reduce the minimum and maximum transmitter power by 5 dB or increase the

minimum receiver sensitivity by the same amount. Alternatively, this effective coding gain can be used to achieve a longer physical reach or a higher split ratio when using a multi-longitudinal mode (MLM) laser in the optical network unit (ONU). In this case, FEC is used to reduce the penalty due to mode partition ratio (MPN).

4.1 Introduction

Passive optical networks (PONs) are an emerging optical multiaccess network technology based on all-optical core. PONs provide a low-cost solution, with guaranteed quality of service (QoS) of deploying fiber-to-the-premises/cabinet/building/home/user (FTTx), which is an effective solution to enable new multimedia services such as interactive video, voice, image, audio, and fast Internet. PONs are expected to solve the so called "first and last mile problem", that remains the bottleneck between the backbone network and high-speed local area networks (LANs).

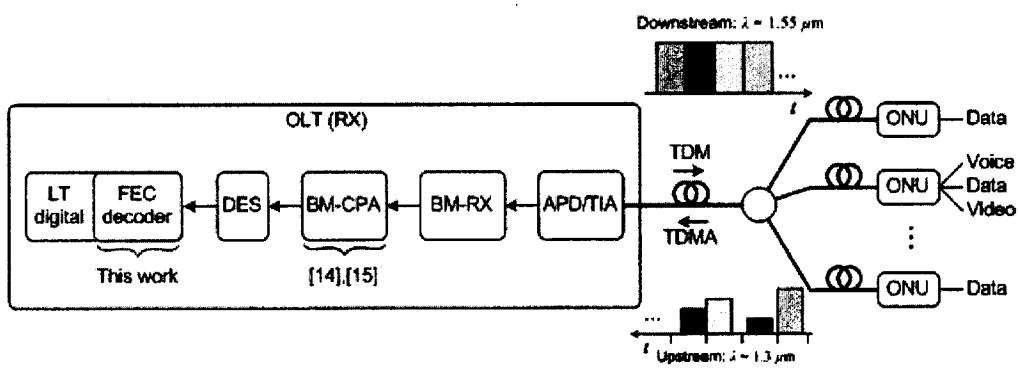


Fig. 4.1 Generic GPON network architecture for FTTx scenarios showing the work in context. OLT: optical line terminator; RX: receiver; LT: line terminator; FEC: forward error correction; DES: deserializer; APD: avalanche photodiode; TIA: transimpedance amplifier; TDM: time division multiplexing; TDMA: time division multiple access; ONU: optical network unit.

Fig. 4.1 shows an example of a PON network. In the downstream direction, the network is point-to-point: continuous data is broadcast from the optical line terminator (OLT) to the ONUs using time division multiplexing (TDM) in the wavelength band of $1480 - 1550$ nm. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous mode ICs. The challenge in the design of a chip set for PONs comes from the

upstream data path. In the upstream direction, the network is point-to-multipoint: using time division multiple access (TDMA), multiple ONUs transmit bursty data in the 1310 nm window to the OLT in the central office (CO). To use the shared medium effectively, the ONUs require a burst-mode transmitter with a short turn-on/off delay [1]. Because packets can vary in phase and amplitude due to optical path differences, the OLT requires a burst-mode receiver (BM-RX) and a burst-mode clock and data recovery (BM-CDR). Within the OLT, the BM-RX is responsible for amplitude recovery, whereas the BM-CDR is responsible for phase recovery.

Avalanche photodiode (APD) receivers or forward error correction (FEC) schemes can be used to overcome or reduce the impact of these errors and thus improve the BER. Receivers implementing APDs can easily meet the sensitivity requirements. However, the associated cost is high, as APDs are expensive, require high-voltage biasing, and require temperature compensation. FEC is used by the transport layer in communication systems. It is based on transmitting the data in an encoded format which introduces redundancy but also allows the decoder to detect and correct the transmission errors. With FEC, data transmission with low error rate can be achieved, and retransmissions are avoided. FEC is the cheaper option than APDs even though some complexity is associated with it [3].

Burst-errors (clustered bit errors [1].) inherently arise in GPON channels because of the phase acquisition process by BM-CDRs for bursty and packet mode data. This makes the BER measurements unreliable and unpredictable, and therefore not a true BER representation. What do we mean by a *reliable* and a *predictable* BER? There are two comments on this. Firstly, at a particular SNR, the BER does not converge because of the presence of burst-errors from packet to packet. Thus, the BER will change from measurement to measurement for the same SNR. Secondly, the BER will also vary for packets with different phases at the same SNR. This is because the phase acquisition time of the CDR is a function of the relative phase between two packets.

FEC with Reed-Solomon (R-S) codes is useful for burst error correction [5]. Defined as R-S(n, k), R-S codes are block based as they divide a codeword of n symbols into m-bit symbols with k symbols of data and $2t = (n - k)$ symbols of parity. By definition, an R-S(n, k) code has an error correcting capability of t symbol errors. The most common R-S

[1] A burst-error is defined as an n-bit sequence that contains clustered bit errors. Two erroneous bits always mark the first and last bits of the sequence, and there can be any number of errors, up to $(n - 2)$, in between them [4]

code is the R-S(255, 239) and it is recommended by the international telecommunication union-telecommunication standardization sector (ITU-T) G.984.3 standard [6] for GPON BM-RXs. R-S(255, 239) is used in the ITU-T G.975 and G.709 recommendations.

However, there is no guarantee that the length of burst-errors will be less than the code's error correcting capability. Burst-error correcting codes have been demonstrated for bursty channels [7]- [13], but these codes are complex and introduce latency at the circuit level implementation. Our simple solution, using FEC with R-S codes and a BM-CDR with fast phase acquisition, is a work around this problem. We have shown that this solution gives reliable and predictable BERs.

The ITU-T G.984.3 standard suggests that FEC can result in an increased link budget by $\sim 3-4$ dB. In this paper we experimentally verify this claim. We also show how FEC is useful for making reliable BER measurements with our novel bit error rate tester/analyzer (BBERT/A) that achieves instantaneous synchronization with the incoming pattern. This is unlike commercial BERTs that require continuous alignment between the incoming pattern and the reference pattern, and milliseconds to acquire synchronization.

We experimentally demonstrate for the first time the impact of FEC on the performance of 622/1244 Mb/s BM-CDR with instantaneous phase acquisition (for any phase step, $\pm 2\pi$ rads) for GPON OLT applications with G.709 R-S (255, 239) decoding. To account for the $(n/k) = 15/14$ FEC overhead, the BM-CDR is operated at 664/1327 Mb/s. Our receiver is built upon the novel burst-mode clock phase aligner (BM-CPA) designed by Faucher et. al [14], [15] which achieves instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rads). The BM-CPA is based on commercially available SONET CDRs operated in $2\times$ over sampling mode. With the increased link budget as shown in this paper, higher bit rate and longer distance from the OLT to the ONUs can be supported, as well as higher number of splits per single PON tree.

Although the receiver demonstrated in this chapter could be built upon any BM-CDR with short phase acquisition times [16]- [20], these BM-CDRs have their associated disadvantages. Specifically, PLL-based CDRs reduce the settling time by increasing the bandwidth, but have inherent stability issues, jitter peaking, and limited jitter filtering [16], [17]. BM-CDRs based on gated oscillators perform clock phase alignment by triggering the local clock on each transition of the input [18]- [20]. Although the phase acquisition is instantaneous, this solution does not filter out input jitter and it is susceptible to pulse distortions.

Thus, we choose to base our receiver on the BM-CDR proposed in [14], [15] which does

not suffer from any of the mentioned drawbacks associated with BM-CDRs with short phase acquisition times. This solution inherits the low jitter transfer bandwidth (1 MHz) and the low jitter peaking (0.1 dB) of the 1244 Mb/s CDR from which it is built. The end result is a BM-CPA with instantaneous phase acquisition (0 bit) and the very good jitter characteristics of a SONET CDR. Hence, the BM-CPA could also find applications in burst/packet switched networks, which may require a cascade of BM-CPAs that each consumes some of the overall jitter budget of the system.

The rest of the chapter is organized as follows. In Section 4.2, we describe the experimental burst-mode test setup that we use to characterize the receiver. The design of the BM-CDR with FEC and R-S decoding is presented in Section 4.3. This section also details the integration of all the hardware components. We present and discuss the experimental results in Section 4.4. Finally, Section 4.5 concludes the chapter.

4.2 Burst-Mode Test Setup (BM-TS)

To test BM-CDR with FEC and R-S decoding, we used the custom burst-mode test setup (BM-TS) [14], [15] as depicted in Fig. 4.2. The BM-TS can only go up to 1 Gb/s. This limitation, which comes from the pattern generator, *HP80000*, explains why the design of the BM-CDR with FEC can only be experimentally verified at 622.08 Mb/s. The BM-TS has two main functionalities. First, it can generate alternating packets with adjustable amplitude and phase to emulate PON traffic. Second, it can perform burst bit error ratio (BBER) and characterize the channel by analyzing the errors (see Section 4.2.2). Consequently, the BBER measurements can also be used to determine the amplitude/phase/frequency acquisition times, and the number of consecutive identical digits (CIDs) supported by the BM-CDR.

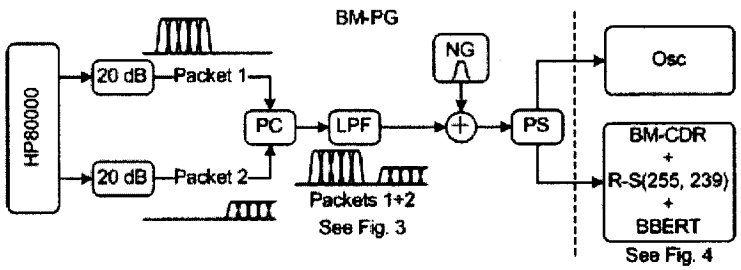


Fig. 4.2 Burst-mode packet generator. The burst-mode packet generator is on the left of the dashed line. When performing the BBER measurements, the two packets are set to have the same amplitude. BM-PG: burst-mode pattern generator; PC: power combiner; LPF: low-pass filter (4th order Bessel-Thomson); NG: Gaussian noise generator; PS: power splitter; Osc: oscilloscope; BBERT: burst bit error rate tester.

The importance of the BM-TS is attributed to the limitations associated with conventional test equipment. For example, since the characterization of SONET CDRs does not require the generation of phase steps, this feature is therefore not supported by commercially available pattern generators known to the authors. Also, commercial BERTs lose pattern synchronization while the sampling clock is being recovered by the CDR.

4.2.1 Burst-Mode Packet Generator (BM-PG)

The BM-PG generates the upstream traffic shown in Fig. 4.3. Packet #1 serves as a dummy packet to force the BM-CDR to lock to a certain phase (ϕ_1) before the arrival of packet #2. The BBER measurements (and if required, amplitude/phase/frequency acquisition times measurements [14], [15]) are on packet #2, which consists of guard bits (16), preamble bits (0 to 2^{15}), delimiter bits (20), payload bits (2^{15}), comma bits (48), and a '1010$\cdots$' pattern that can be circularly shifted in front of the delimiter to increase the preamble length. The guard, preamble, and delimiter bits correspond to the physical-layer upstream burst-mode overhead specified by the ITU-T G.984.2 standard [21]. The guard bits provide distance between two consecutive packets to avoid collisions. The preamble is used to perform amplitude and phase recovery. The delimiter is a unique pattern indicating the start of the packet to perform byte synchronization. Likewise, the comma is a unique pattern to indicate the end of the payload. The payload is an RS encoded $2^{15} - 1$ PRBS with a zero appended at the end. The packet loss ratio (PLR) and the BBER are measured on the

payload bits only. The lock acquisition time corresponds to the number of bits that need to be circularly shifted in front of the delimiter in order to get a PLR of zero for over three minutes at 622.08 Mb/s ($> 10^6$ packets received) and a BBER $< 10^{-10}$ [14].

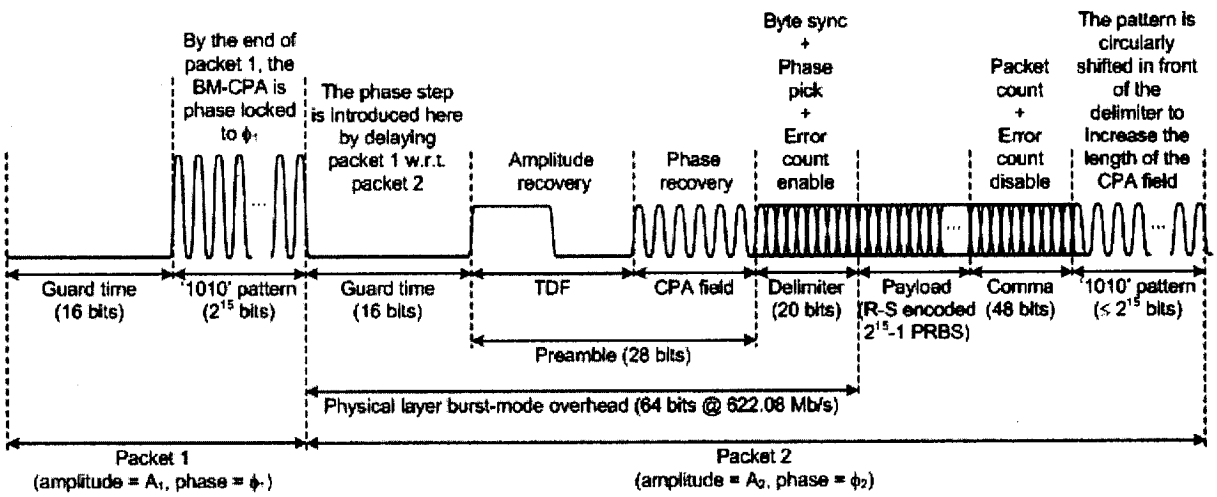


Fig. 4.3 Test signal and specification of the upstream burst-mode overhead at 622.08 Mb/s. When performing BBER measurements and testing the phase acquisition time, the two packets are set to have the same amplitude. TDF: threshold determination field; CPA: clock phase alignment; PRBS: pseudo-random binary sequence.

It has been specified in the G.984.2 standard that the overhead length at 622.08 Mb/s should be 8 bytes. This implies that the GPON complaint OLT should require no more than 28 bits in the preamble. Nevertheless, the BM-TS supports any length between 0 and 2^{15} its for amplitude and phase acquisition. The preamble of the data is split into two fields, a threshold determination field (TDF) for amplitude recovery and a CPA field for clock-phase recovery. This is shown in Fig. 4.3. If the CPA field can be reduced, more bits are available for amplitude recovery. Consequently, the burst-mode sensitivity penalty is reduced. This is because sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet. The interested reader is referred to [2].

In order to generate the pattern of Fig. 4.3, we used two ports of an *HP80000* pattern generator (see Fig. 4.2). The two packets are combined on the same line using an RF power combiner, which emulates the optical power combiner of a PON network (see Fig. 4.1).We

used 20-dB attenuators to control the maximum amplitude of the packets and minimize reflections [22]. To test the FEC and BM-CDR under stringent conditions, we stressed the input pattern in two different ways. First, we slowed down the edges of the input pattern with a 4th-order Bessel-Thomson filter having a -3-dB bandwidth of 467 MHz (0.75×622 MHz) (see the LPF block in Fig. 4.2). Second, we added a random noise generator after the filter. The noise generator consists of a transimpedance amplifier (TIA) powered by a supply voltage approximately 1 V lower than the nominal voltage of 3.3 V. The thermal noise generated by the TIA has a Gaussian distribution, which translates into 63 ps of random jitter.

In this setup, the amplitude (thus the SNR) and the relative phase of the packets, the preamble length, and the number of CIDs, can be all be set. The BM-PG has an 18 dB dynamic range, which would be more than sufficient to reach the limits of most BM-RX. The phase step between packets #1 and #2 can be set anywhere between ± 2 ns on a 2 ps resolution. This corresponds to ± 1.25 UI at 622 Mb/s, and ± 2.5 UI at 1244.16 Mb/s.

4.2.2 Burst Bit Error Rate Tester/Analyzer (BBERT/A)

The BBERT/A design, is based on [14]. The BBERT/A designed can be used to characterize errors, that is, indicate whether errors are bursty or not, determine the lengths of burst-errors with an accuracy of one bit, and flag when the error correcting capability of the FEC is reached. The BBERT/A can also be used to keep track of the PLR and the BER by counting the number of errors in the deserialized data, in order to monitor the number of packets received, the number of bits received, and the number of packets lost.

In order to selectively perform BBER measurements on the payload of packet #2, the delimiter and the comma are used as gating signals for the error counters. The incoming data is compared with an internally generated $2^{15} - 1$ PRBS.

The novelty of the BBERT/A is that it does not require a fixed synchronization between the incoming pattern and the reference pattern of the error detector. Synchronization happens instantaneously at the beginning of every packet, therefore enabling BBER measurements, error characterization, and amplitude/frequency/phase acquisition time measurements with an accuracy of one bit on non continuous, bursty data. This is unlike conventional BERT/As, which require 1) a continuous alignment between the incoming pattern and the reference pattern, and 2) milliseconds to acquire synchronization.

4.3 Burst-Mode CDR with FEC and R-S Decoding

The main building blocks of the BM-CDR with FEC, as depicted in Fig. 4.4, are a SONET CDR, a byte synchronizer, a phase picker, phase-locked loops (PLLs), and a R-S(255, 239) decoder. The multirate CDR is from *Analog Devices* (part $\#ADN2819$). The deserializer is from *Maxim-IC* (part $\#MAX3885$). Its main function is to parallelize the data as the R-S(255, 239) decoder accepts one symbol (8-bit) data block every clock cycle. The parallel data and the divided clock are then brought onto a FPGA from *Xilinx* ($Virtex-IIPro$) for further processing. The phase picker, byte synchronizer, PLLs, and R-S(255, 239) decoder, are implemented on the FPGA, alongside the BBERT/A.

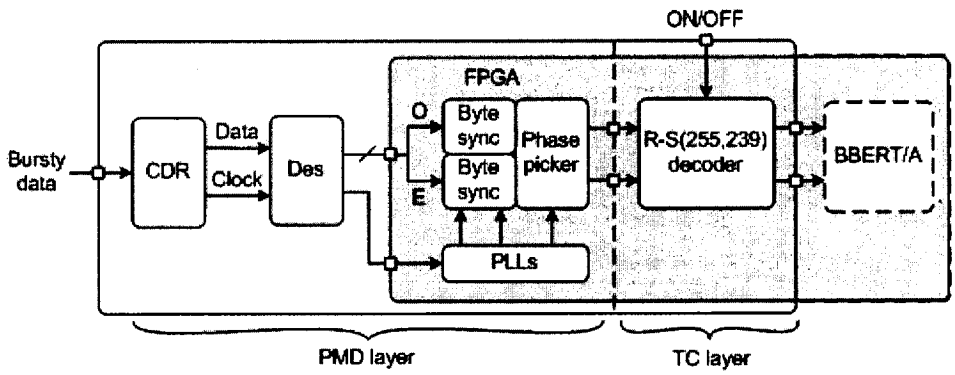


Fig. 4.4 Block diagram of the GPON BM-CDR with FEC. CDR: clock and data recovery; Des: deserializer; PLLs: phase-locked loops; R-S: Reed-Solomon; BBERT/A: burst bit error ratio tester/analyzer; PMD: physical dependent media; TC: transmission convergence; O: odd bits output of the deserializer; E: even bits output of the deserializer. Odd and even bits are a result of sampling the bursty input at t_{odd} and t_{even} sampling instants respectively.

4.3.1 Hardware Integration

For more details on the hardware, implementation details, and component integration, the interested reader is referred to [23] from which this experimental setup is built. Here we summarize the hardware and implementation details.

Fig. 4.5 shows the experimental setup in the lab. The BM-CDR with FEC consists of three discrete integrated circuits (CDR, 1:16 deserializer, and FPGA) mounted on three

evaluations boards. The CDR is mounted on the front most PCB, the deserializer is mounted on the rightmost vertical PCB, and the FPGA is mounted on the horizontal PCB.

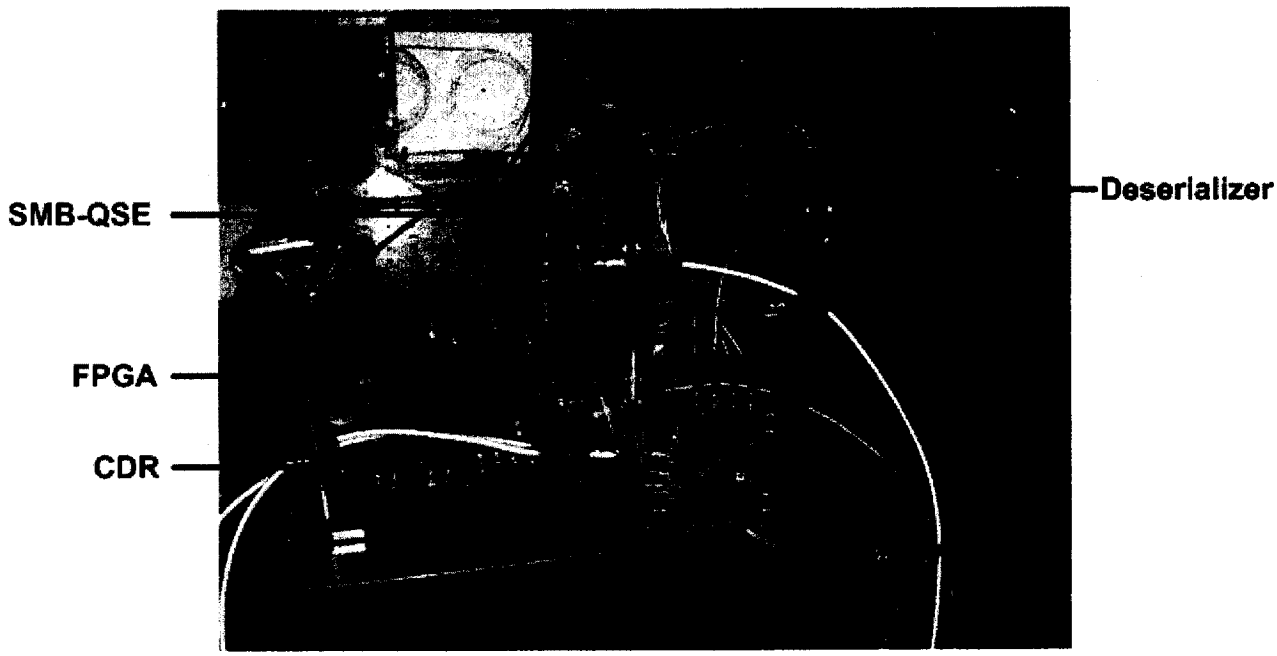


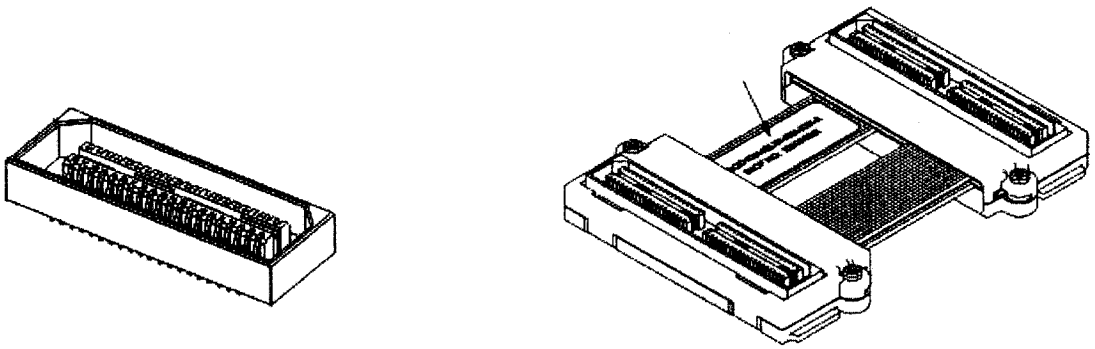
Fig. 4.5 Experimental setup of the BM-CDR with FEC.

The multirate CDR supports the following frequencies of interest for a 622.08/1244.16 Mb/s BM-CDR with FEC: 622.08/1250 Mb/s for the conventional mode and 1250/2488.32 Mb/s for the 2× over sampling and burst modes, and 664/1327 Mb/s for the FEC overhead.

The deserializer is rated at 2488.32 Mb/s and its main function is to reduce the bit rate by parallelizing the data. The maximum data rate supported by the LVDS buffers of the FPGA is 840 Mb/s (420 MHz).

The parallel data and the recovered clock are brought onto the FPGA using a high-speed QSE connector from *Samtec* as shown in Fig. 4.6(a). However, the deserializer evaluation board uses SMB connectors. Since the outputs of the deserializer and the inputs of the FPGA both use LVDS logic, no conversion other than a connector conversion is needed at the interface between the two. The two vertical PCBs next to the FPGA serve as SMB-to-QSE connector converters.

To connect the deserializer outputs to the QSE-to-SMB interface PCB, we use 34 six-inch SMB cables (16-bit differential data + 1 differential clock) and a high-speed parallel cable (see Fig. 4.6(b)) to complete the connections to the FPGA. The QSE connector is rated at 8 GHz (differential signaling), and its mating cable is rated at 1.74 GHz.



(a) (b)

Fig. 4.6 (a) QSE connector from *Samtec* (part $\#QSE-040-01-L-D-A$). (b) Mating cable, also from *Samtec* (part $\#EQCD-040-06.00-TTR-TBL-1$)

4.3.2 Burst-Mode Clock Phase Aligner (BM-CPA)

This receiver architecture is built upon the novel burst-mode clock phase aligner (BM-CPA) [14], based on commercially available SONET CDRs operated in 2× over sampling mode, which achieves instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rads). The idea behind the BM-CPA is based on a simple, fast, and effective algorithm. The odd bits of the recovered data from the CDR output are forwarded to path O and the even bits are forwarded to path E. The byte synchronizer is responsible for detecting the delimiter. The idea behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on the odd, t_{odd}, and even, t_{even}, samples of the data respectively. The phase picker uses feedback from the byte synchronizers to select the right path. A graphical depiction of the odd and even samples is shown in Fig. 4.7.

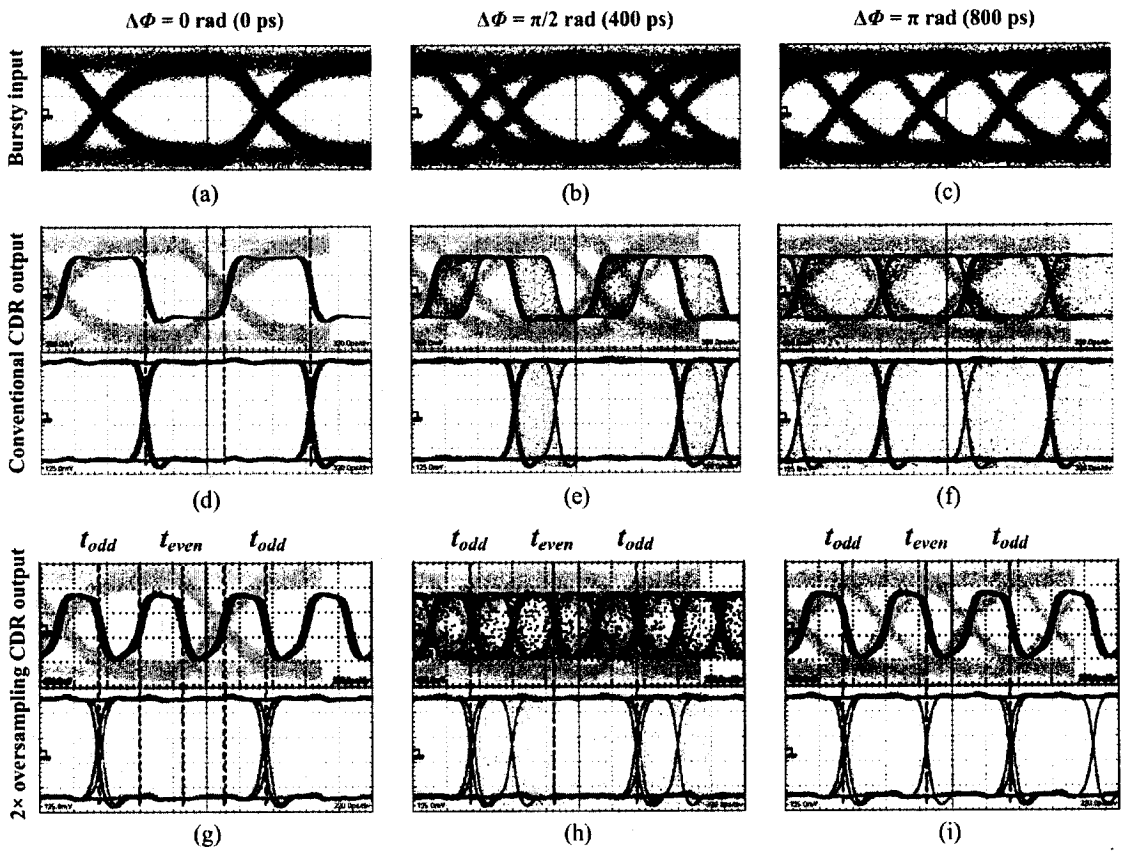
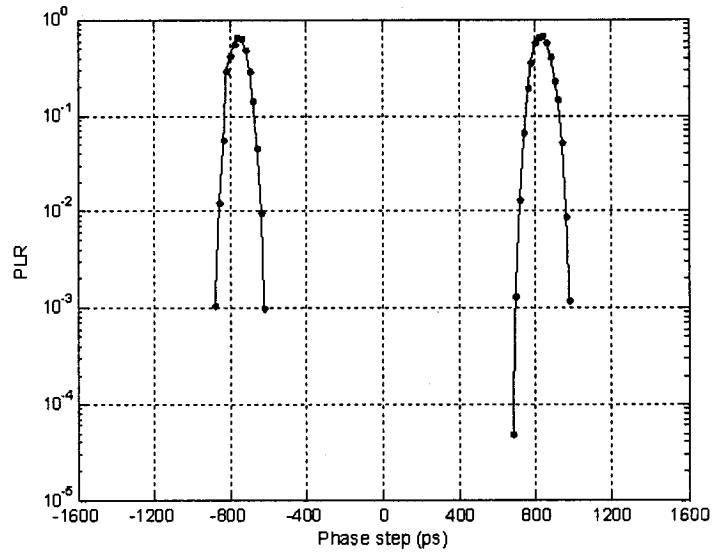


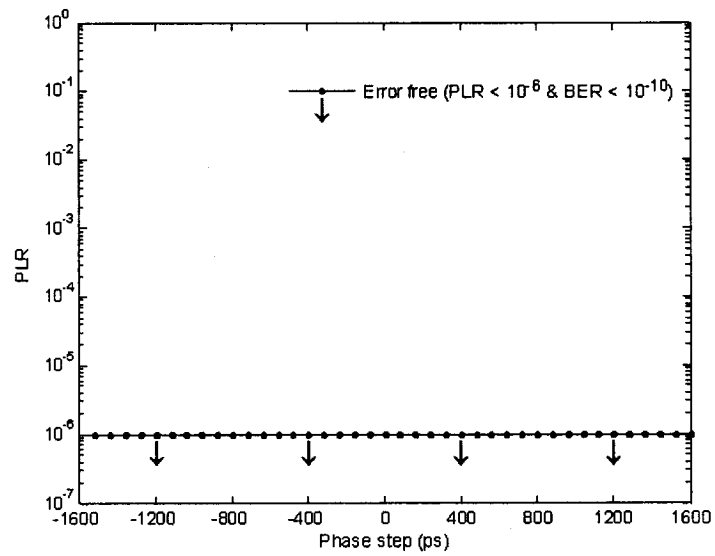
Fig. 4.7 Graphical depiction of odd and even samples [14]. (a)-(c) BM-CPA input signal for 0, $\pi/2$ and π rad phase steps respectively. The jitter is 63 ps RMS. To demonstrate the phase alignment of the recovered clock relative to the phase of the input data, Figs. (a)-(c) reappear in gray under the clock signals of Figs. (d)-(i). (d)-(f) Clock and data recovered by the BM-CPA operated in conventional mode. (g)-(i) Clock and data recovered by the BM-CPA operated in 2× over sampling and burst modes. Bits resulting from the t_{odd} and t_{even} sampling instants are forwarded to the odd and even path respectively (see Fig. 4.4). The pattern dependent jitter (PDJ) that appears in the clock and data patterns of Figs. (d)-(i) [although less obvious in (d)-(f)] is one of many subtypes of deterministic jitter. PDJ, also known as intersymbol interference (ISI), is due to a pattern change from a clock like square wave ('1010$\cdots$' pattern) to a non clock-like pattern (PRBS) in the overall pattern shown in Fig. 4.3. In (i), it is clear that the recovered data associated with packet #1 does not exhibit PDJ (see the transition aligned with t_{even}). This is explained by the fact that packet #1 is made of a '1010$\cdots$' pattern exclusively. On the other hand, the recovered data associated with packet #2 does exhibit PDJ (see the transitions aligned with t_{odd}). This is explained by the fact that packet #2 is made of a 2^{15} PRBS followed by a 2^{15} '1010$\cdots$' pattern.

Figs. 4.8(a) and 4.8(b) show plots of the PLR vs. phase step for the BM-CDR operated in conventional mode (SONET CDR) and burst-mode respectively. In both figures, the preamble length is set to zero.

At 622.08 Mb/s, a 800 ps phase step corresponds to half a bit period (π rad). As expected, this corresponds to the worst case phase step for the conventional mode (see 4.8(a)). As shown in Fig. 4.9, 40 preamble bits are necessary to obtain error free operation for any phase step. For the 2× over sampling mode (not shown), the worst-case phase step is 400 ps ($\pi/2$ rad). As shown in Fig. 4.8(b), 2× over sampling, combined with the phase picking algorithm, turns the conventional CDR into a BM-CDR (also called a BM-CPA) with instantaneous phase acquisition (no preamble bits).



(a)



(b)

Fig. 4.8 PLR vs. phase step [14]. (a) CDR (conventional SONET CDR). (b) BM-CDR (SONET CDR + 2× over sampling + phase picker enabled). The bit rate, preamble length, and jitter of the input signal are 622.08 Mb/s, 0 bits, and 63 ps RMS, respectively.

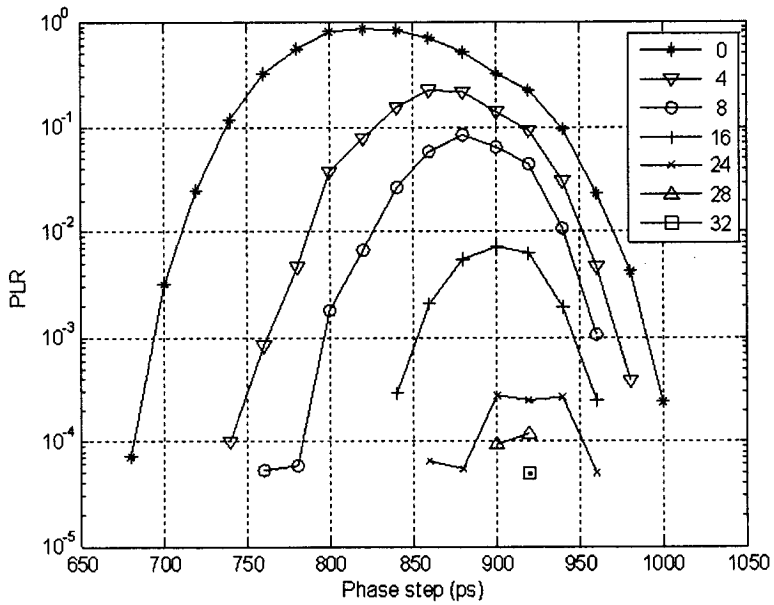


Fig. 4.9 PLR vs. phase step for a conventional 622.08 Mb/s CDR [14]. As expected, the worst-case phase step is around π rad, or 800 ps. The legend shows some of the preamble lengths tested. A preamble length of 40 bits gave error free operation (PLR $< 10^{-6}$ and BER $< 10^{-10}$).

4.4 Experimental Results and Discussion

To study the impact of FEC on GPON BM-RXs, BBER measurements are performed on the $2^{15} - 1$ PRBS payload of packet #2 (see the upstream traffic shown in Fig. 4.3) with and without FEC. The BM-CDR rated at 622/1244 Mb/s is operated at 664/1327 Mb/s to account for the $(n/k) = 15/14$ FEC overhead.

The plots in Fig. 4.10 show the waterfall curve - BBER as a function of the input signal power when FEC is disabled and enabled. It can be observed that at an input power, P_o, of -32.5 dBm, the BBER without FEC is 10^{-4} while error free operation is obtained with FEC (for same P_o). This is as expected from theory as FEC with R-S$(255, 239)$ codes are effective after BBER $< 10^{-4}$.

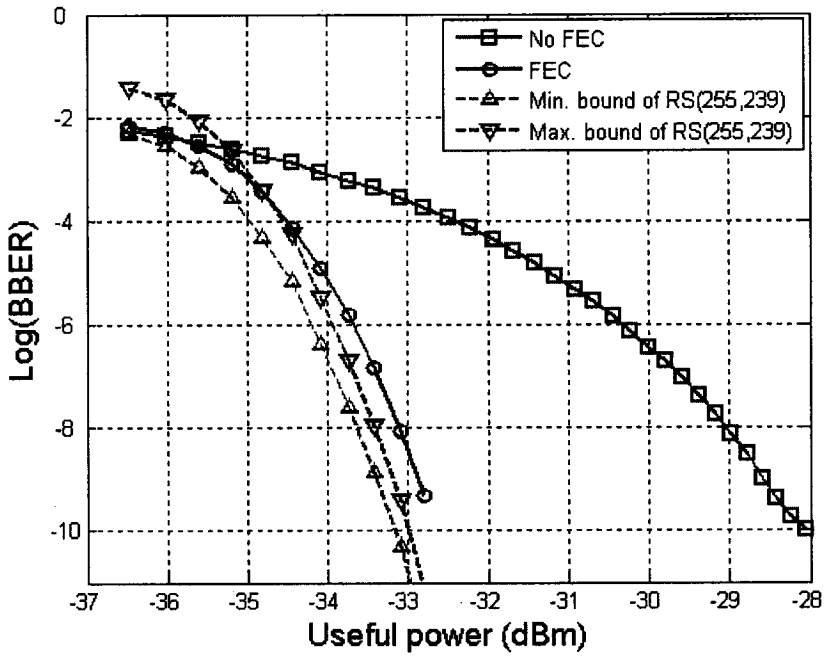


Fig. 4.10 BBER performance comparison of a GPON BM-CDR with FEC (red curve) and without FEC (blue curve). The theoretically obtained minimum and maximum bounds with FEC based under the assumption of purely random bit errors, are shown as well. The experimental FEC curve does not fall between these bounds based on the fact that the bit errors are not purely random and deterministic jitter is the dominating factor.

According to the ITU-T G.984.2 standard, the FEC coding gain, G, is defined as the difference input power at the receiver with and without FEC, for a BBER of 10^{-10}. We report a coding gain of $G = 5$ dB at BER of 10^{-10} verifying the claim of the increased link budget in ITU-T G.984.3.

Burst-errors inherently arise in GPON channels because of the phase acquisition process by BM-CDRs for bursty and packet mode data, making the BBER measurements unreliable and unpredictable, and therefore not a faithful representation of the true BBER. R-S codes are particularly useful for burst-error correction but there is no guarantee that the length of burst-errors will be less than the codes error correcting capability. We show in the following example that this condition can be relaxed with a BM-CPA and R-S decoding. At the same time, we also show how we achieve reliable and predictable BBER

With FEC disabled and the BM-CPA turned off, from Fig. 4.11(a) ($P_o = -28$ dBm), it can be seen that there are bursts of errors. This effect is worsened if there exists any phase step, $-2\pi \leq \phi \leq +2\pi$ rads, between the packets, with worst being for $\phi = \pm 2\pi$ rads. However, with FEC enabled and BM-CPA turned on, instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rads) is achieved, consequently eliminating burst-errors and obtaining error free operation (for the same SNR) as shown in Fig. 4.11(b).

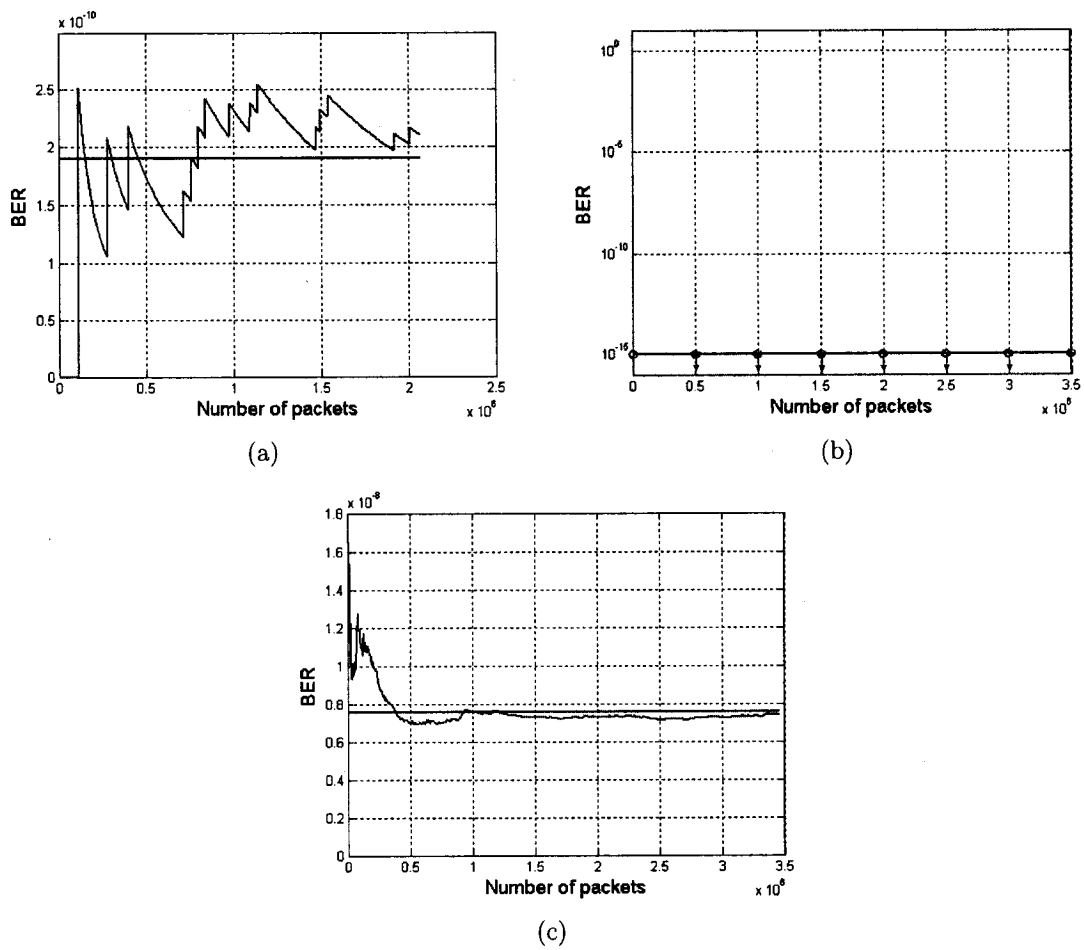


Fig. 4.11 BBER as a function of time (number of packets received by the BM-CDR). (a) Without FEC and BM-CPA disabled. (b) With FEC and BM-CPA enabled for the same input power, $P_o = -28$ dBm as (a). (c) With FEC and BM-CPA enabled for a lower SNR ($P_o = -33$ dBm). The red line shows the average BER over the period of packet reception.

To further illustrate the elimination of burst-errors, we consider the following case: For a lower SNR when error free operation is not obtained with FEC, for example at $Po = -33$ dBm, it can be observed from Fig. 4.11(c) that burst-errors have been eliminated with the BBER curve converging to the *true* and *predictable* value.

To verify this claim, we measured the waterfall curves for packets with different phases from -2π to $+2\pi$ rads. In accordance to our prediction, the waterfall curve shown in Fig. 4.10 is the same for any phase step between the packets. Our measurements were made on packets with no preamble bits. To achieve the same results with a SONET CDR, 40 preamble bits are necessary as also demonstrated in [14] and shown in Fig. 4.9.

To compare the experimental results with theory, consider the R-S $(n, k) = (255, 239)$ code that divides an n symbol codeword into m-bit symbols and k symbols of data. It has a decoded symbol-error probability, P_E, which can be written in terms of the channel symbol-error probability, p [5]:

$$P_E \approx \frac{1}{2^m - 1} \sum_{j=t+1}^{2^m-1} j \begin{pmatrix} 2^m - 1 \\ j \end{pmatrix} p^j (1-p)^{2^m-1-j} \tag{4.1}$$

where $t = (n - k)/2$ is the symbol-error-correcting capability of the code. Under the assumption of purely random bit errors,

$$p = 1 - (1 - \varepsilon)^m \tag{4.2}$$

where ε is the channel BER without FEC as measured in Fig. 4.10 (blue curve). The upper and lower bounds for the channel BER with FEC, $\varepsilon_{RS(n,k)}$, as depicted in Fig. 4.10, are calculated using (1) and

$$\varepsilon_{RS(n,k)} = P_E \times \frac{s}{m} \tag{4.3}$$

where $s = m$ errors/symbol for the upper bound and $s = 1$ for the lower bound.

It can be observed from Fig. 4.10 that the experimental BBER with FEC lies within these bounds for BBER $< 10^{-4}$ and lies outside these bounds for BBER $> 10^{-4}$. The reason for this is based on the fact the BBER performance is a function of intrinsic and extrinsic effects of the channel, that is, the presence of random and deterministic jitter will affect the error correcting capability of the R-S codes. Since (2) and (3) assume *purely random* bit errors, the channel BER with FEC is overestimated for BBER $> 10^{-4}$. This is attributed

to the fact that as the SNR is increased, the presence of random jitter is attenuated relative to the presence of deterministic jitter. Consequently, for BBER $> 10^{-4}$, deterministic jitter is the dominating factor.

The $G = 5$ dB improvement in coding gain can be used to reduce the minimum and maximum transmitter power by 5 dB or increase the minimum receiver sensitivity by the same amount. Alternatively, this effective coding gain can be used to achieve a longer physical reach or a higher split ratio when using a multi-longitudinal mode (MLM) laser in the ONU. In this case, FEC is used to reduce the penalty due to mode partition ratio (MPN).

4.5 Conclusion

In conclusion, we have successfully implemented a 622/1244 Mb/s BM-CDR with FEC and R-S codes that meets the G.984.2 and G.984.3 specifications. The coding gain obtained verifies the claim of the increased link budget specified by the G.984.3 standard. A novel technique for fast burst-error correction for bursty channels is also presented. This is achieved by employing FEC on BM-CDRs with fast phase acquisition time. We demonstrate this with our custom built BBERT.

Table 4.1 summarizes the specifications of our receiver and compares them against the G.984.2 and G.984.3 specifications.

Table 4.1 Key receiver parameters compared with G.984.2 and G.984.3 requirements.

Item	Units	BM-CDR + FEC (this work)	ITU-T G.984.2/3
Bursty data bit rate	Mb/s	664(with FEC)	622.08
Guard time	bit	16	16
Preamble time	bit	0	< 28
Delimiter time	bit 20	20	
Bit error ratio	-	$< 10^{-10}$	$< 10^{-10}$
Min. sensitivity	dBm	$\sim$-32.5 at BER=10^{-10}	-27 at BER=10^{-10}
Coding gain	dB	$\sim$5	> 3
Jitter (RMS) of input signal	ps	62.64	N/A
CID immunity	bit	590	> 72

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Chapter 5

10 GHz 1310/1550 nm PIN Photodiode Characterization

A procedure for accurate photodiode modeling is presented in this chapter. A commercial photodiode is tested using the proposed method. The results are compared with the specifications from the manufacturer to verify the effectiveness of this measurement procedure. In particular, we present the characterization and analysis of a 10 GHz 1310/1550 nm InGaAs/InP PIN photodiode available from *EMCORE* (MR030). In total, four sets of experiments are performed to test the photodiode. The geometry features of the photodiode are verified. The dark current of the photodiode is measured. The photodiode parasitic capacitance (C_{PD}) is acquired indirectly from the measured results of the S_{11} parameter. And the responsivity is tested at both 1310 nm and 1550 nm wavelengths for different incident optical power and biasing conditions.

5.1 Introduction

An optical receiver for passive optical networks has to deal with data packets that vary in amplitude and phase. The task of amplitude recovery is handled by the burst-mode receiver (BM-RX) which also performs an optical-to-electrical (OE) conversion. The work presented in Chapter 4, assumes that an effective front-end is supplied. Thus, the focus is on the burst-mode clock and data recovery (BM-CDR) which provides solutions to the phase alignment problem. As demonstrated, this can be performed purely in the electrical domain, with the electrical traffic 'emulating' an optical network. To promote a holistic

solution with both amplitude and phase recovery, the receiver must be tested with an 'actual' optical testbed.

In this chapter, we focus on the OE conversion problem which has a direct impact on the receiver bandwidth. In particular, it is the size of the diode junction capacitance that causes this limitation and thus the most important parameter in a PIN photodiode model. The parasitic parameters associated with the substrate and photodiode bond pads also need to be modeled carefully for two reasons: 1) the geometry size of the photodiode continues to shrink; 2) the data rate continues to increase beyond 10 Gb/s. Both these trends make the effects of small parasitic parameters more prominent [1], [2].

To emphasize the latter point, consider the following explanation [3]. The receiver presented in this thesis exploits the design of components for long-haul networks which are typically ahead of the components for gigabit-capable passive optical networks (GPONs). Currently, GPONs support a maximum data rate of 2.5 Gb/s, whereas 10 Gb/s is currently mainstream for long-haul networks. Assuming this holds true in the future, with the scaling of components for long-haul networks, our solution will also have to scale.

The rest of the chapter is organized as follows. Section 5.2 details the description of the experimental setups and the test techniques for the different experiments. The experimental results obtained are also presented and analyzed in this section. Section 5.3 concludes this chapter.

5.2 Photodiode Characterization

5.2.1 Geometry Scan

The geometry features of the PIN photodiode can be accurately determined with the interferometer profiler [4] and the optical profiler program that implements Enhanced Vertical Scanning Interferometry (EVSI) which can be used to profile smooth or rough surfaces that vary in height from a few nm to 80 μm. Fig. 5.1 shows the experimental setup for the three-dimensional (3D) geometry scan of the photodiode and the interferometer profiler.

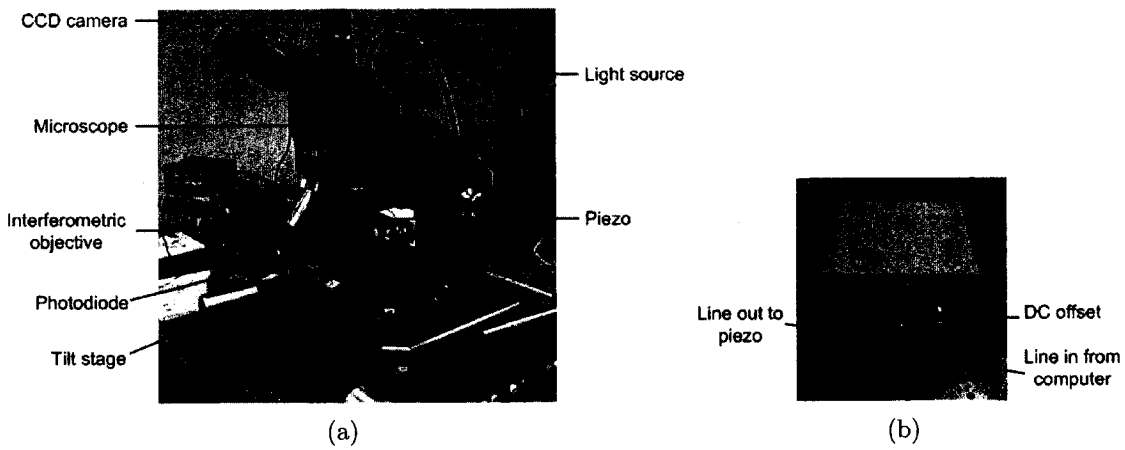


Fig. 5.1 Interferometer profiler. (a) Optical profiler setup for obtaining the 3D geometry of the PIN photodiode. (b) Piezo controller.

The 3D scan of the photodiode can be acquired by running an interference scan over the bare die with all the x-y-z distances clearly shown as in Fig. 5.2. The cross-sections of the important regions (active region and bonding pads) of the photodiode are extracted to show the relative height difference and to decipher accurate measurements[1].

[1]The small dip of ~ 0.3 μm that appears on the anode pad is the probing mark on the received samples from *EMCORE*.

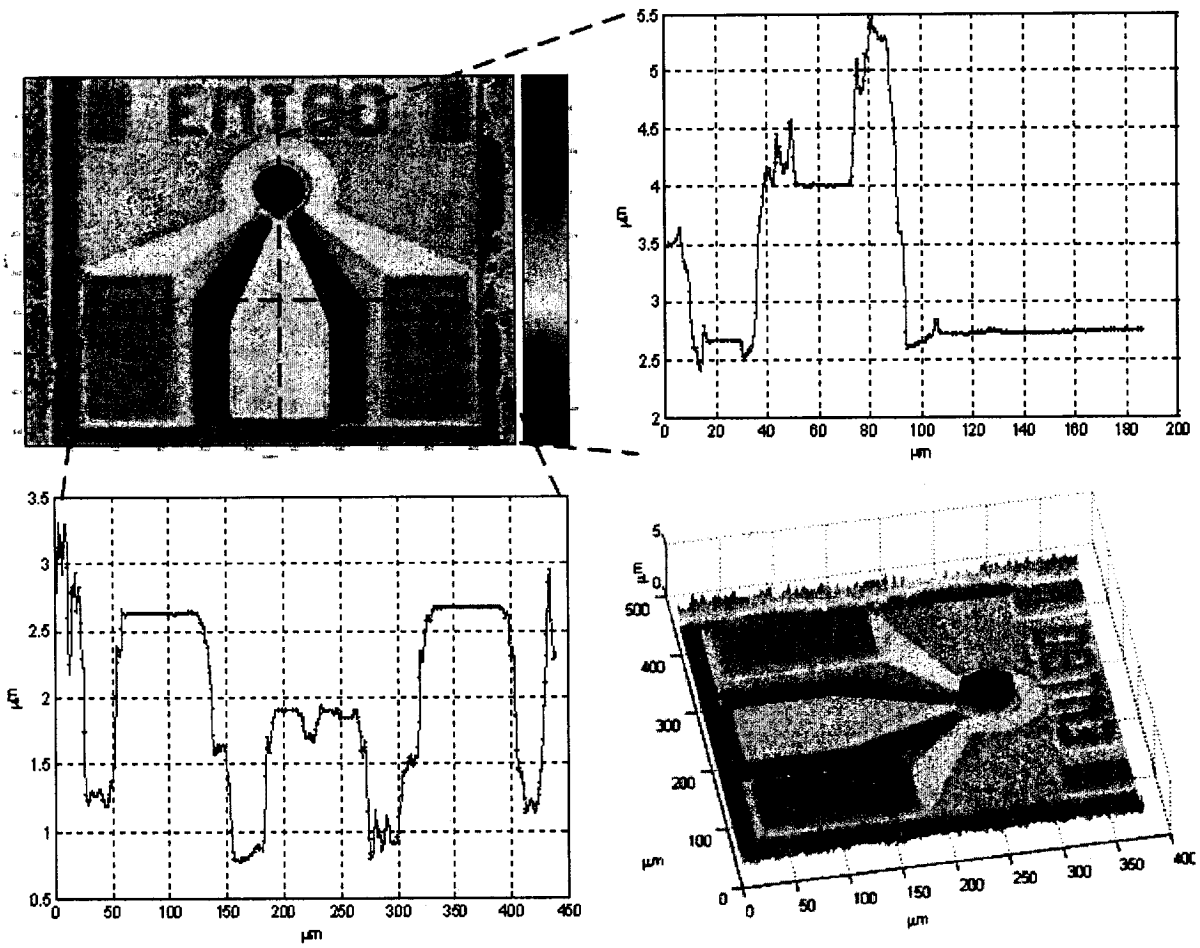


Fig. 5.2 Photodiode geometry features. *Up-left:* 2D top-view of the photodiode; *Top-right:* active region cross-section showing the relative height difference; *Bottom-left:* cathode and anode and pad cross-section; *Bottom-right:* 3D profile of the PIN photodiode.

The photodiode geometry with the important dimensions obtained from our analysis is shown in Fig. 5.3(a). For comparison purposes, the dimensions obtained by *EMCORE*, are depicted in Fig. 5.3(b). Table 5.1 summarizes the measured physical dimensions of the PIN photodiode.

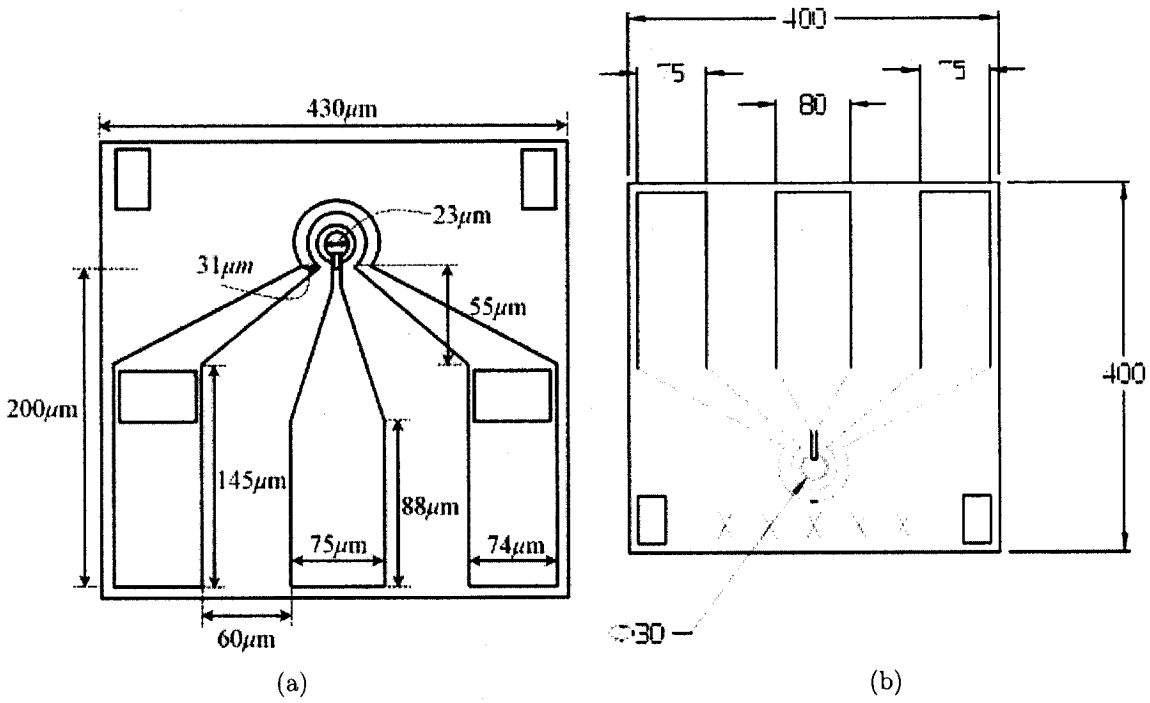


Fig. 5.3 PIN photodiode geometry. (a) Important dimensions from our interferometric scan. (b) Dimensions provided by *EMCORE*. Note that the figures are not to scale.

Table 5.1 Summary of the important physical dimensions of the photodiode.

Physical Parameters	Dimensions
Active area diameter	23 μm
Anode bond pad size	75 μm × 88 μm
Cathode bond pad size	74 μm × 145 μm

From these extracted geometries, the areas of the anode pad and the cathode pad can be calculated by making approximations and reasonable assumptions about the shapes. It is found that the ratio of the area of a single cathode pad to that of the anode pad is approximately 1.1. Thus, it can be inferred that the parasitic bond pad capacitances have the following relationship: $C_{BPA} \leq C_{BPC}$. Assuming the sheet resistance dominates the bond pad parasitic resistances, we have $R_{BPA} \leq R_{BPC}$ since the aspect ratio of the anode pad is smaller than that of the cathode pad.

5.2.2 Dark Current Test

In order to perform the dark current test, a photodiode sample is glued to the center of a ceramic chip carrier. The cavity is wire-bonded to provide ground connections. Around five to six wires are used on each side to form a good ground plane.

Two DC probes are used for the experiment. The first probe is used to provide the biasing voltage, V_{BIAS}, as shown in the schematic in Fig. 5.4, whereas the second probe that is connected to the anode pad is used to monitor the current, I_{ANODE}, with the aid of the *HP4145B Semiconductor Parameter Analyzer* (SPA) while the voltage at the anode is swept from 0 V to 3.5 V to measure the dark current under different working conditions.

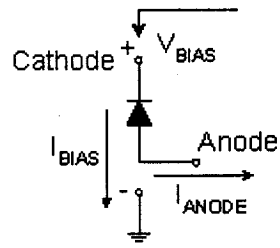
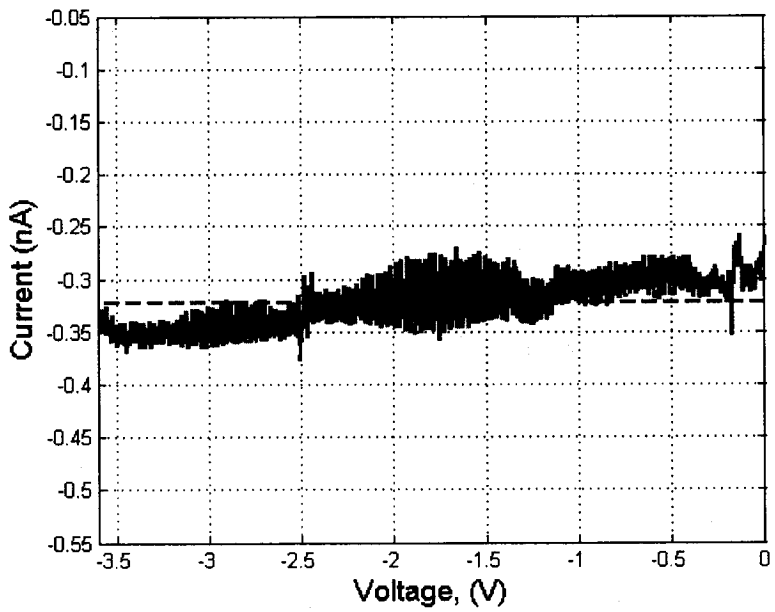
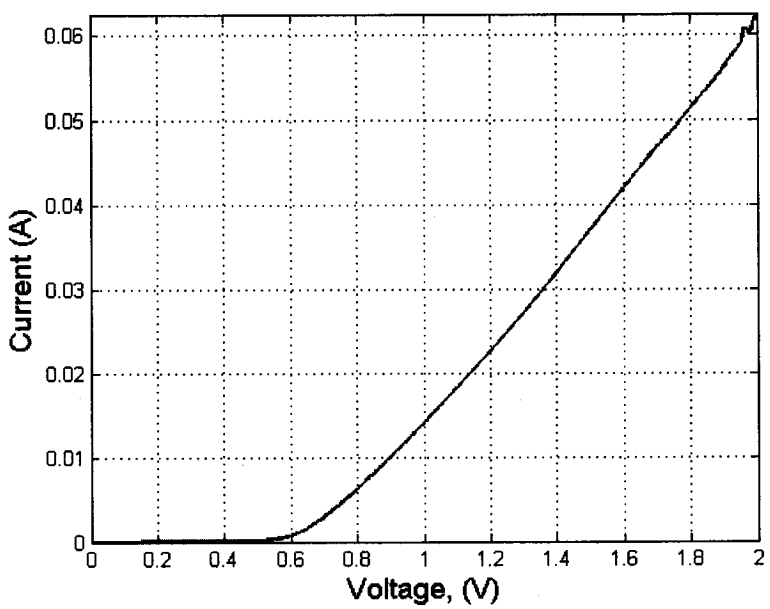


Fig. 5.4 Dark current measurement test setup.

The plot of the measured dark current as a function of the potential difference across the photodiode junction is shown in Fig. 5.5(a). The dashed red line on the plot depicts the dark current averaged over the entire voltage range and it is found to be $\sim$ 0.33 nA. In addition to the dark current test, the *I-V* graph of the photodiode under forward bias conditions is plotted in Fig. 5.5(b). The exponential nature of the plot depicts a typical diode characteristic. Under forward biasing, illumination from the active region can be observed on the CCD camera.



(a)



(b)

Fig. 5.5 DC characteristics of the PIN photodiode. (a) Dark current under reverse bias condition and (b) forward bias I-V characteristic of the photodiode.

5.2.3 S_{11} Parameter Test

The proposed small-signal circuit model for the PIN photodiode is depicted in Fig. 5.6, where C_{PD} is the diode junction capacitance, R_{SH} is the diode shunt resistance, C_{BPA} and C_{BPC} are the bond pad capacitances for the anode and cathode pads respectively, and R_{BPA} and R_{BPC} are the bond pad parasitic resistances for the anode and cathode respectively. The reason for having a scale factor of two for C_{BPC} and 0.5 for R_{BPC}, in the model, is to account for the two cathode bond pads that appear in parallel (when probed).

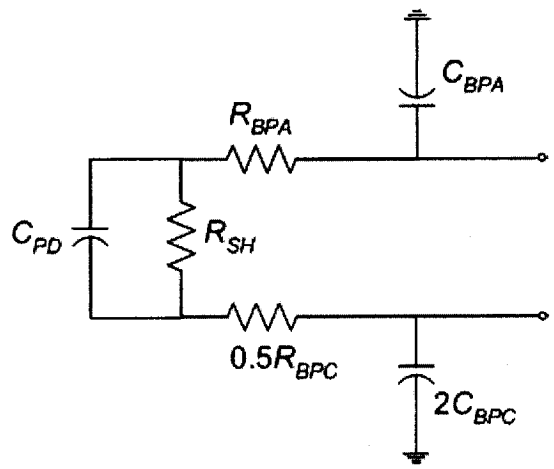


Fig. 5.6 Proposed small-signal circuit model for the PIN photodiode.

The small-signal parameters and more importantly the C_{PD} value can be easily and accurately determined by performing a pure electrical test. An indirect way to obtain the values of the small-signal parameters is by first measuring the input reflection coefficient, the S_{11} parameter, over a wide range of frequencies. The photodiode small-signal parameters can then be extracted by performing a curve-fitting optimization to 'best-fit' the experimental data using the *Agilent Advanced System Design* (ADS) circuit simulator. Hence, a small-signal model for the PIN photodiode can be built based on the S_{11} parameter measurement results.

The experimental setup to extract the S_{11} parameters is shown in Fig. 5.7. The S_{11} parameters are measured with the *Agilent 8703B Lightwave Component Analyzer* (LCA) from 50 MHz to 20.05 GHz with linear incremental steps of 12.5 MHz. A *Cascade Microtech* RF Probe is used to apply/collect the input/reflected RF power to/from the PIN photo-

diode. The RF probe tip has a ground-signal-ground (G-S-G) configuration with 150 μm separation. The LCA is calibrated prior to the S_{11} parameter testing to take into account the signal attenuation through the RF cable and signal reflection from interconnects.

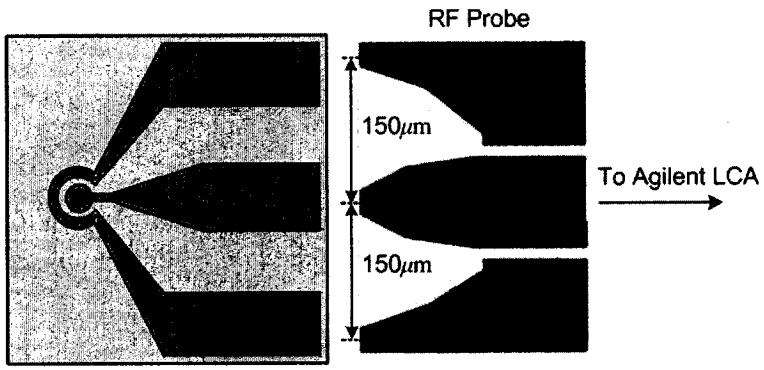


Fig. 5.7 S_{11} parameter measurement test setup.

The photodiode model is constructed in *Agilent* ADS and the measured S_{11} parameter data sets are averaged and imported in ADS as the optimization target. Three goals are setup for the optimization problem:

1. $\|S_{11_{experimental}} - S_{11_{fitted}}\| \leq 0.01$ dB
2. $R_{BPA} \leq R_{BPC} \leq 1.5R_{BPA}$
3. $0.8C_{BPC} \leq C_{BPA} \leq C_{BPC}$

The latter two are based on the geometry consideration of the photodiode as explained in Section 5.2.1. However, since the area calculation is just an approximate as it excludes the semi-circular cathode region surrounding the active region, the scaling factors of 0.8 and 1.5 are introduced as compensation for goal #2 and goal #3 rather than just $C_{BPA} \leq C_{BPC}$ and $R_{BPA} \leq R_{BPC}$ respectively.

The proposed range of values for the photodiode model parameters for the optimization process is listed in Table 5.2. These values are chosen (the order of magnitude) to ensure that the convergence space indeed reflects the true nature of the solution.

Table 5.2 Range of values specified for the optimization process.

Photodiode model circuit parameter	Parameter value optimization range
Photodiode depletion capacitance, C_{PD}	5 fF $\sim$ 500 fF
Shunt resistance, R_{SH}	1 MΩ $\sim$ 1000 MΩ
Parasitic capacitance of the cathode bond pad, C_{BPC}	5 fF $\sim$ 500 fF
Parasitic capacitance of the anode bond pad, C_{BPA}	5 fF $\sim$ 500 fF
Parasitic resistance of the cathode bond pad, R_{BPC}	1 Ω $\sim$ 1000 Ω1
Parasitic resistance of the anode bond pad, R_{BPA}	1 Ω $\sim$ 1000 Ω1

Two optimization algorithms are taken into consideration; these include the random- and the gradient algorithm. The optimization process is repeated 20 times for the random algorithm with 100 iterations at each frequency. The reason for performing curve-fitting with two different algorithms is to verify the true nature of the extracted parameters. That is, the values of the parameters have indeed converged in the same space.

To ensure the validity of the obtained results and the model, the S_{11} parameters are simulated from the extracted model parameters with the *Spectre* simulator in *Cadence Analog Environment.* The simulated curves from *ADS* and *Spectre* are both compared with the experimental data as shown in the plots in Fig. 5.8.

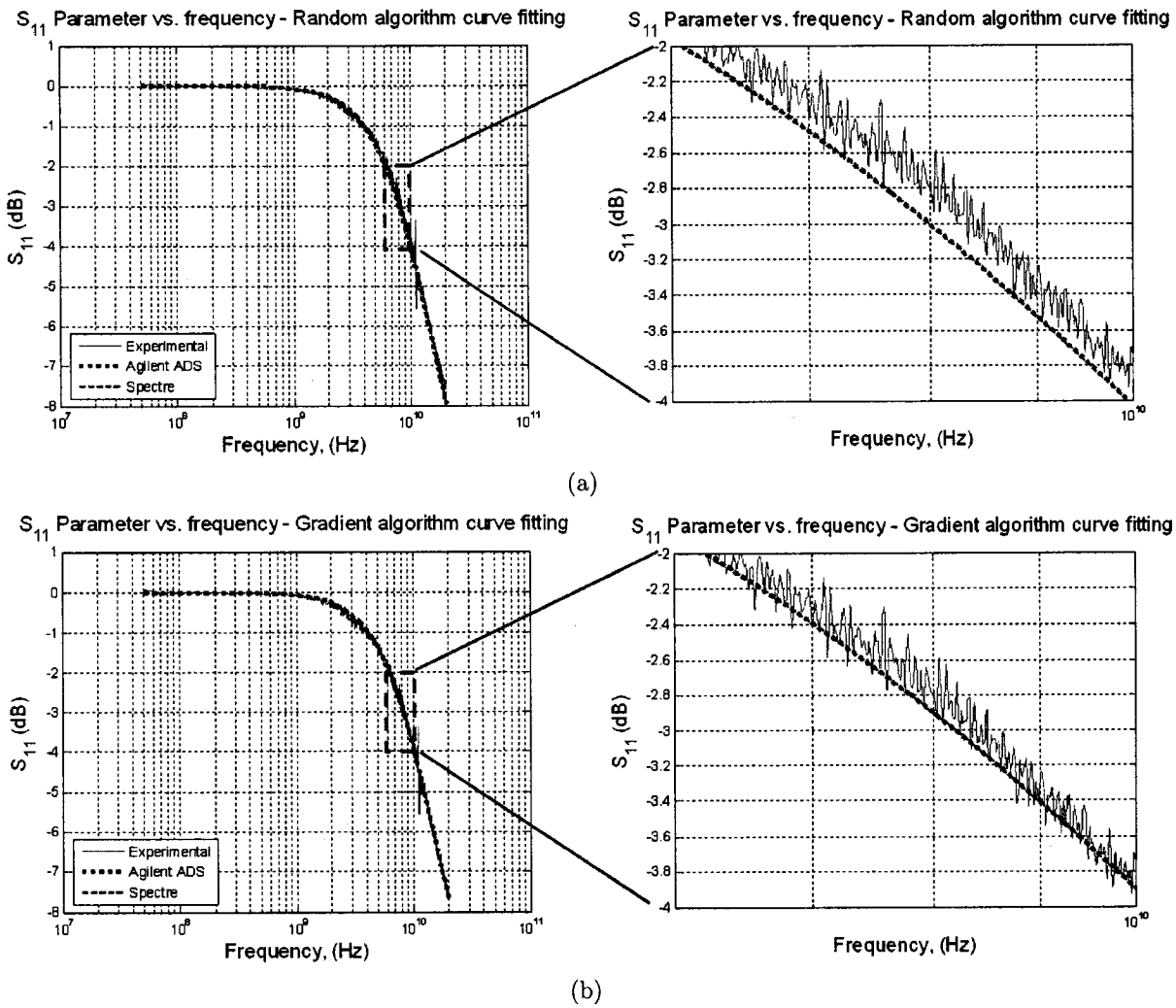


Fig. 5.8 S_{11} parameter as a function of frequency. The solid (blue) curve depicts the experimental data obtained (after calibration) with the *Agilent 8703B Lightwave Component Analyzer* (LCA), while the dotted (black) and dashed (red) best-fit curves obtained with *Agilent ADS* and *Cadence Spectre* respectively, after the determination of the PIN photodiode model circuit parameters with (a) random optimization algorithm and (b) gradient optimization algorithm.

From the curves, it can be observed that both the optimization algorithms fit the experimental data well especially for frequencies lower than 5 GHz and higher than 10 GHz. However, for frequencies in the range of 5 GHz to 10 GHz, the gradient algorithm is superior to the random algorithm which can easily be seen in the 'zoomed' version of the plots. These discrepancies can be attributed to the rather 'randomized' nature of the random algorithm and also to the fact that the curve is steep in this region and thus small variations in the x-axis cause large variations in the y-axis.

Table 5.3 summarizes the final averaged values of the photodiode model circuit parameters obtained after the curve fitting with the random optimization algorithm and the gradient optimization algorithm. Also, the L_2-metric, known as the Euclidean norm between the simulated and experimental S_{11} parameters is 0.022 (a.u.) with the random optimization algorithm and 0.019 (a.u.) with the gradient optimization algorithm.

Table 5.3 The averaged values of the photodiode model parameters obtained through the curve fitting algorithms.

Photodiode model circuit parameter	Final averaged value after curve fitting	
	Random algorithm	Gradient algorithm
Photodiode depletion capacitance, C_{PD}	181.56 fF	191.37 fF
Shunt resistance, R_{SH}	495 MΩ	372.6 MΩ
Parasitic capacitance of the cathode bond pad, C_{BPC}	12.25 fF	15.93 fF
Parasitic capacitance of the anode bond pad, C_{BPA}	10.55 fF	18.58 fF
Parasitic resistance of the cathode bond pad,R_{BPC}	44.60 Ω	33.58 Ω
Parasitic resistance of the anode bond pad, R_{BPA}	39.86 Ω	38.74 Ω

Two photodiode samples are tested and the results obtained are consistent. Fig. 5.9 shows the comparison of the S_{11} parameter curves obtained for both the samples after curve fitting with the gradient algorithm. From the plot, it can be seen that both the curves are indeed close to one another.

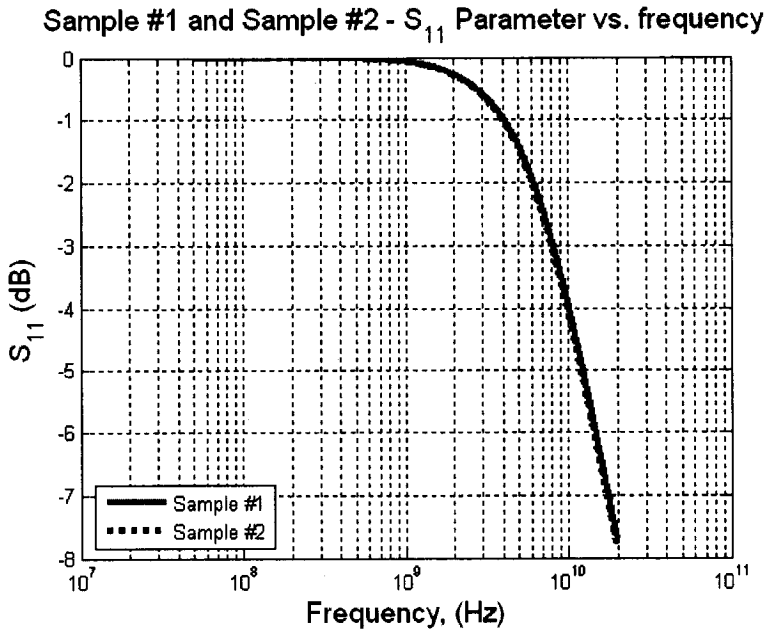


Fig. 5.9 Comparison of the S_{11} parameters curves obtained for two photodiode samples after curve fitting with the gradient algorithm.

5.2.4 Responsivity Test

The responsivity of the PIN photodiode is defined as,

$$R = \eta \frac{I_{PD}}{P_o} \tag{5.1}$$

where η is the quantum efficiency, I_{PD} is the photon current, P_o is the incident optical power.

The quantum efficiency is defined as,

$$\eta = \frac{r_e}{r_{ph}} \tag{5.2}$$

where r_{ph} is the photon injection rate and r_e is the rate at which the electrons are collected inside the material. We also have the following relationship,

$$r_{ph} = \frac{P_o}{h\nu} \tag{5.3}$$

$$r_e = \eta \times r_{ph} \tag{5.4}$$

$$I_{PD} = r_e \times q \tag{5.5}$$

where q is the electron charge.

Substituting (5.3)-(5.5) into (5.1), we can derive a simple equation for responsivity,

$$R = \frac{\eta \cdot \lambda \cdot p}{h \cdot c} \tag{5.6}$$

The quantum efficiency for InGaAs in the 1.3 μm/1.55 μm range is close to 85%. At 1.3 μm wavelength, η is slightly higher than at 1.55 μm. The theoretical values of the responsivity are summarized in Table 5.4.

Table 5.4 Calculated responsivity for InGaAs PIN photodiode.

			1310 nm	1537 nm
Quantum Efficiency	η		~85%	~80%
Responsivity	R	A/W	0.90	0.99

The schematic of the test setup for responsivity measurement is shown in Fig. 5.10. The photon current I_{PD} flows through the 1 kΩ resistor and thus generates a voltage drop V_{PD}. This voltage is measured by a *BK-Precision* 5360 digital volt meter. The 1 kΩ resistance provides enough amplification to make sure that V_{PD} is not too weak to measure. V_{bias} is the photodiode reverse biasing voltage.

The test bench is illustrated in Fig. 5.11. A *Cascade Microtech* lightwave probe (LWP) is used to deliver the light to the photodiode. An insertion loss of 0.2 dB is assumed for the LWP. Careful alignment in the x-y-z axes is necessary to ensure maximum coupling of the light from the SMF to the photodiode active region.

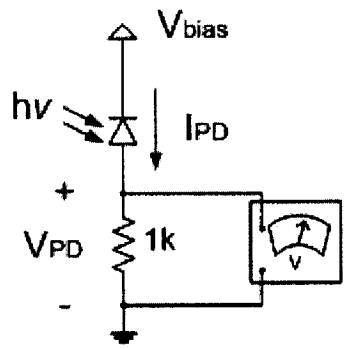


Fig. 5.10 Schematic of the test setup for responsivity measurement.

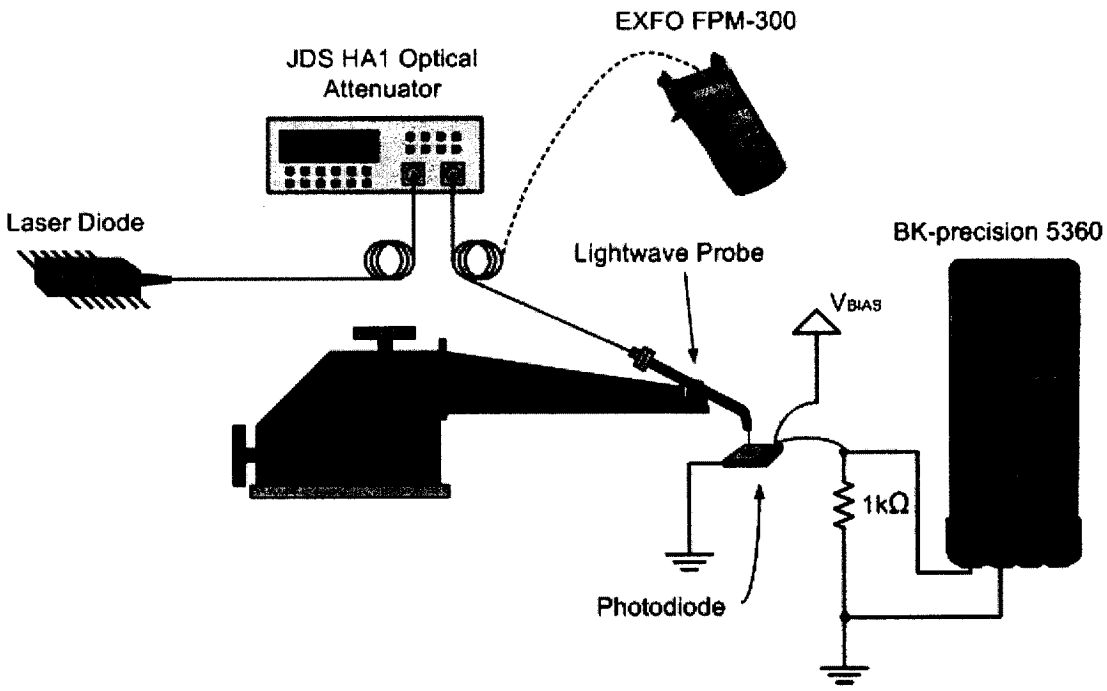
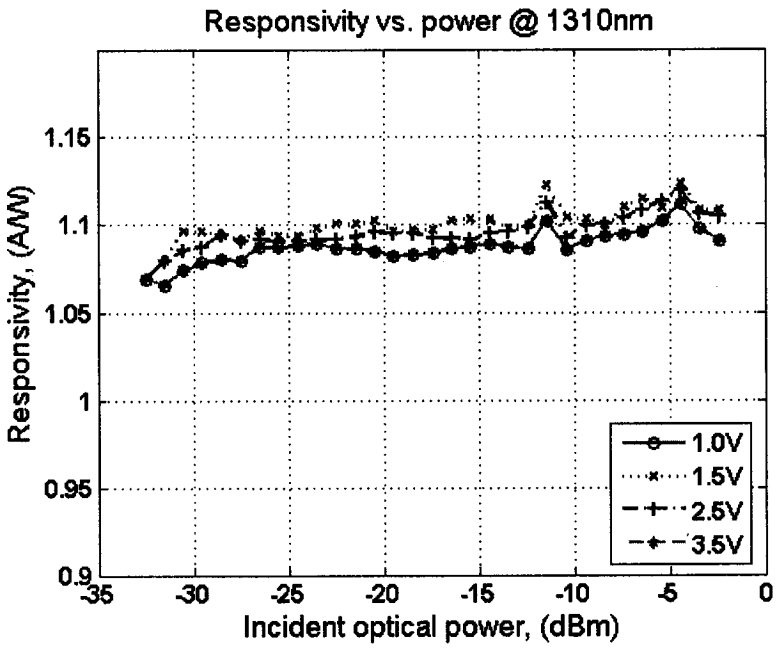
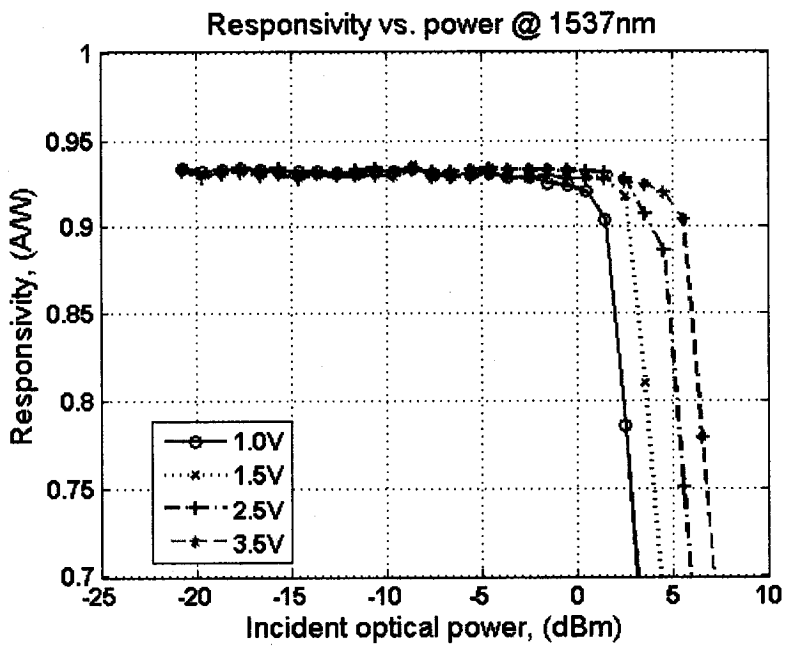


Fig. 5.11 The test bench for the responsivity test.

The responsivity of the PIN photodiode is measured under different biasing conditions and at two wavelengths: 1310 nm and 1537 nm. Two continuous wave lasers are used to provide the 1310 nm and 1537 nm wavelengths. The measurement results are shown in Fig. 5.12. The input power before the LWP is measured with an *EXFO FPM-300* handheld power meter.



(a)



(b)

Fig. 5.12 Responsivity curves for two photodiode samples (reverse biased at −3.5 V) at 1310 nm and 1537 nm wavelengths. The bias voltage is varied from 1 V to 3.5 V.

The incident optical power from the 1537 nm laser is varied from −20.45 dBm to 9.78 dBm. The roll-off of the curves at high incident power is due to the fact that the anode voltage rises higher than the biasing voltage V_{bias}. Therefore, the photodiode is forward biased and thus is not biased at its normal operation region. The responsivity of the photodiode is about 0.93 A/W.

We are limited by the highest output power from the 1310 nm laser, so the range of the incident optical power is from −32.3 dBm to −2.18 dBm. We do not observe the roll-off of the responsivity curve simply because lack of higher incident optical power. The responsivity is around 1.1 A/W range for all biasing voltages. This value is higher than expected for a normal PIN photodiode, typically less than 1 A/W. The possible explanations could be that the incident power is underestimated at 1310 nm.

5.3 Conclusion

In this chapter, we have presented the detailed experimental work to characterize a 10 GHz 1310/1550 nm PIN photodiode. The geometry features are verified and compared with the data acquired from the vendor - the results are very consistent. The dark current is less than 0.5 nA under different biasing conditions up to −3.5 V. We have also presented an easy and effective method to build a small-signal model for the photodiode through measured S_{11} parameters. The results are verified with *Spectre* simulator in *Cadence Analog Environment*. The simulated S_{11} data fits the measured experimental data very well. The photodiode parasitic capacitance C_{PD} value is also very close to what is specified in the *EMCORE* datasheet. The photodiode responsivities have been tested at both 1310 nm and 1550 nm.

References

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[3] J. Faucher, "Burst-mode clock and data recovery circuits for optical multiaccess netowrks," Ph.D. dissertation, Dept. Elect. Eng., McGill Univ., Montréal, Canada, 2006.

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Chapter 6

Conclusions & Future Work

Optical multiaccess networks, and more specifically passive optical networks (PONs) are considered to be one of the most promising technologies for the deployment of fiber-to-the-home/building/curb (FTTx) to solve the problem of limited bandwidth in local access networks. PONs achieve this with a low-cost solution and with a guaranteed quality of service. In a PON, multiple users share the fiber infrastructure in a point-to-multipoint (P2MP) network topology. This is in contrast to current access technologies, including DSL, VDSL, and cable, which use a point-to-point (P2P) network topology. The nature of P2MP networks introduce optical path delays which inherently cause the data packets to undergo amplitude, phase, and frequency variations - bust-mode traffic. Consequently, this creates unique challenges for the design and testing of optical receivers.

This chapter concludes the thesis with a brief review of the main contributions of the research presented in the preceding chapters. Some general remarks concerning the advantages and potential of the novel approaches are presented. We also propose future research directions.

6.1 Summary

In this thesis, we identified some key research problems regarding the design and testing of burst-mode receivers (BM-RX) and burst-mode clock and data recovery circuits (BM-CDRs) in Chapter 1. We reviewed existing BM-RXs solutions present in the literature, with the prime focus being on BM-CDRs with short phase acquisition times.

In Chapter 3, we presented the concept and theory of forward error correction (FEC)

techniques and in particular reviewed a class of nonbinary cyclic block codes called Reed-Solomon (R-S) codes. We argued the need for FEC with R-S codes to increase the optical link budget of Gigabit PONs (GPONs). The coding gain can be used to: (1) improve the system performance at a targeted signal power, (2) achieve longer physical reach of the optical links present between the optical network units (ONUs) to the central office (CO) and, (3) reduce the penalty due to mode partition ratio (MPN) when using multi-longitudinal mode (MLM) lasers in ONUs, and thus increase the split ratio (number of ONUs supported from one power splitter/combiner).

In Chapter 4, we demonstrated experimentally for the first time the impact of FEC on the performance of 622/1244 Mb/s BM-CDR with instantaneous phase acquisition (0 bit) for any phase step ($\pm 2\pi$ rads) for GPON optical line terminator (OLT) applications with R-S$(255, 239)$ codes. Our design is based on commercially available SONET CDRs operated in $2\times$ over sampling mode. We measured a coding gain of approximately 5 dB at a bit error ratio (BER) of 10^{-10}. The coding gain can also be used to reduce the minimum and maximum transmitter power by 5 dB or increase the minimum receiver sensitivity by the same amount.

Burst-errors inherently arise in GPON channels because of the phase acquisition process by BM-CDRs for bursty and packet mode data. This makes the BER measurements unreliable and unpredictable, and therefore not a true BER representation. The unreliability is based on the fact that at a particular signal to noise ratio (SNR), the BER does not converge because of the presence of burst errors from packet to packet. Thus, the BER will change from measurement to measurement for the same SNR. The unpredictability stems out from the observation that BERs also vary for packets with different phases at the same SNR. This is because the phase acquisition time of the CDR is a function of the relative phase between two packets.

Our novel technique, using FEC with R-S codes with BM-CDR with fast phase acquisition, gives a solution for burst-error correction in bursty-channels with reliable and predictable BERs. This solution is a simple workaround of other burst-error correcting codes that have been demonstrated for bursty channels, but are far too complex and introduce latency at the circuit level implementation.

We demonstrated our results with a custom designed burst bit error rate tester (BBERT) that can be used to characterize errors, that is, indicate whether errors are bursty or not, determine the lengths of burst-errors with an accuracy of one bit, and flag when the error

correcting capability of the FEC is reached. The BBERT can also be used to keep track of the packet loss ratio (PLR) and the BER by counting the number of errors in the deserialized data, monitor the number of packets received, the number of bits received, and the number of packets lost. This BBERT achieves instantaneous synchronization with the incoming pattern. This is unlike commercial BERTs that require continuous alignment between the incoming pattern and the reference pattern, and milliseconds to acquire synchronization.

The BM-RX meets the GPON physical media dependent layer (PMD) specifications and transmission convergence layer (TC) specifications defined in ITU-T recommendations G.984.2 and G.984.3 standards, respectively.

In Chapter 5, we developed a practical four-step method to accurately build small-signal models of photodiode. This technique is based on extracting the most relevant PIN photodiode parasitic parameters from the measured S_{11} parameters by executing a curve-fitting algorithm. We experimentally demonstrated our idea with a 10 GHz 1310/1550 nm InGaAs/InP PIN photodiode available commercially. The experimental results matched the manufacturer's specifications confirming our theory.

6.2 Future Research

In this section, we propose directions for future research that could derive from the work presented in this thesis.

6.2.1 System on Chip Design

The current design of the BM-CDR was to demonstrate the proof of concept. Thus, it is built from commercially available off-the-shelf components and therefore rather bulky. If this system is to be viable as a commercial product with the expected mass roll-out and deployment of PONs in the near future, then one of the goals is to scale the design down to an application specific integrated circuit (ASIC). There are two main reasons for this. Firstly, the high cost associated with the level of power consumption is a major financial restraint on consumers. Thus, designing this system-on-chip will reduce the costs associated with power consumption. Secondly, the components must be small in size for easy device integration. The current state-of-art in silicon technology is the CMOS-90nm process. One could target this technology for the next generation products.

6.2.2 Scale the BM-CDR with FEC to Higher Data Rates

Taking into account the increasing trends of bandwidth requirements, optical receivers for multiaccess networks must support higher data rates. A 622/1244 Mb/s BM-CDR with FEC is demonstrated in this thesis. This receiver exploits the design of components for long-haul networks which are typically ahead of the components for GPONs. Currently, GPONs support a maximum data rate of 2.5 Gb/s, whereas 10 Gb/s is currently mainstream for long-haul networks. Assuming this holds true in the future, with the scaling of components for long-haul networks, our solution will also have to scale. In order to scale to 5/10 Gb/s, one will have to use a 10 Gb/s (OC-192) SONET CDR and a 10 Gb/s deserializer.

6.2.3 Demonstrate the BM-CDR with BM-RX

The task of amplitude recovery is handled by the BM-RX front-end which also performs an optical-to-electrical (OE) conversion. The work presented in this thesis, assumes that an effective front-end is supplied. Thus, the focus was on the BM-CDR which provides solutions to the phase alignment problem. As demonstrated, this can be performed purely in the electrical domain, with the electrical traffic 'emulating' an optical network. To promote a holistic solution with both amplitude and phase recovery, the receiver must be tested under a 'real' optical network. This will demonstrate a full burst-mode solution for both amplitude and phase recovery.

6.2.4 Demonstrate an OCDMA Receiver with Burst-Mode Capabilities

The current burst-mode receiver design is for time division multiple access (TDMA) traffic in PONs. Optical code division multi-access (OCDMA) is a promising technology for PONs. To date, there has been no OCDMA system that is tested under burst-mode (amplitude and phase fluctuations) conditions, despite the fact that in a real P2MP OCDMA network, packets will travel different distances and arrive asynchronously at the receiver. One could design and demonstrate an OCDMA receiver that will support amplitude steps (achieve automatic threshold adjustment), and support phase steps (acquire phase lock as close to instantaneously as possible).

6.2.5 Concatenate FEC Codes

Block codes (R-S codes) and convolutional codes (Viterbi codes) can be combined to work together. This is achieved by using the convolutional codes to first detect and correct errors, and then allow the block codes to correct the errors made by the convolutional decoder. In literature, this has shown to be a very effective technique. Thus, the R-S$(255, 239)$ decoder in the receiver, can be replaced by such a "concatenated" coding scheme to achieve higher coding gains and further relax the requirements and/or increase the optical link budget of GPONs.