Analog-to-Digital Conversion via Time-Mode Signal Processing

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Abstract

Conventional voltage-mode analog-to-digital converters use voltage amplifiers, voltage comparators, and switch capacitor networks to perform their signal processing. When compared to digital circuitry, these analog circuit blocks consume significant power, occupy large silicon areas, and operate at relatively slow data processing speeds. A signal processing methodology is proposed that performs analog-to-digital conversion on voltage signals while implementing all the circuits in a digital CMOS logic style. This methodology, called *time-mode signal processing*, uses time-difference variables as an intermediate signal between the input voltage and digital output. The resulting silicon devices offer very compact, low power, high-speed, and robust analog-to-digital converter alternatives.

There are five main analog-to-digital converter topologies: flash, successive-approximation, pipeline, delta-sigma, and integrating converters. Each converter topology is presented in the context of the time-mode signal processing methodology. The circuits that implement each time-mode data converter are described and when appropriate system-level, transistor-level, and experimental results are revealed.

Three integrated circuits (IC) were fabricated in a 0.18-μm CMOS technology to demonstrate the feasibility of the time-mode ADC methodology. The first IC

implemented the time-mode comparator and a time-mode flash ADC. The time-mode delta-sigma ADC design was demonstrated in the second IC. Two circuits were implemented in the third IC: a differential-input time-mode delta-sigma ADC and a cyclic (or algorithmic) ADC.

Résumé

Les convertisseurs conventionnels pour changer la tension analogique à une tension numérique emploient les amplificateurs de tension, les comparateurs de tension, et les résaux de condensateur sélectionable pour acquir leur traitement de signal. En comparaison le circuit des modules analogues vis-à-vis le circuit numérique nous constatons une augmentation de puissance, une superficie de silicium moins compacte, et un traitement de données beaucoup plus lent. Une méthodologie est proposée pour le traitement du signal qui établi la conversion analogue à numérique sur les signaux de tension et tout en mettant en oeuvre tous les circuits dans un format numérique de type circuit à semiconducteur oxyde-métal à symétrie complémentaire (CMOS). Cette méthodologie reconnue sur le nom de *technique-temporelle* donne un traitement de signal par domaine temporel en employant la variance de cadence entre les temps comme un signal intermédiare entre la tension d'entrée et la tension de sortie numérique. Les formats numériques de type circuit semiconducteur nous offrent une alternative en temps convertisseur d'analogue à numérique avec l'avantage d'une unité compact, robuste, un coût de puissance réduit, et une haute-vitesse efficace.

Il existe cinq topologies principales dans les convertisseurs analogiques à numérique: flash, approximations successives, pipeline, delta-sigma, convertisseurs intégrés. Dans chacune des topologies mentionnées ci-dessus, le traitement de signal par technique-temporelle est une méthode réconnue.

Les circuits employés par chaque convertisseur de donnée par technique-temporelle sont décrits lorsque le niveau du système est approprié, le niveau du transitor, et les données expérimentales sont identifiés.

Trois circuits intégrés (CI) ont été conçus et fabriqués, avec une technologie de 0,18-µm CMOS pour démontrer la possibilité de la méthodologie du technique-temporelle convertisseur analogique-numérique (CAN). Le premier CI emploie le technique-temporelle comparateur et Flash CAN. La conception de technique-temporelle delta-sigma CAN a été démontrée avec le deuxième CI. Deux circuits ont été conçus et fabriqués dans le troisième CI. Une entrée différentielle technique-temporelle delta-sigma CAN et un CAN à cyclique (ou algorithmique).

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Claim of Originality

The contributions of this dissertation are described as follows:

- The concept of time-mode signal processing (TMSP) is utilized in Chapter 3 whereby time-difference variables are used as an intermediate processing variable in the conversion of analog voltages into digital signals. The merits and limitations of analog-to-digital conversion via TMSP are investigated. Specifically, TMSP offers the advantages of compact, low power, and high-speed operation through a digital implementation of the analog-to-digital processing. However, resolution and linearity are sacrificed due to limited linear input voltage range.

- The circuit building blocks to convert voltage-to-time, process time, and convert time-difference variables into digital data are presented in Chapter 3. A critical building block, known as the voltage-to-time converter (VTC), is developed. The VTC is composed of two voltage-controlled delay circuits and two CMOS implementations are revealed. Other TMSP blocks are described such as voltage-to-time adders, voltage-to-time integrators, time-amplifiers, time comparators, and time-to-digital converters. The implementations of these circuits and their limitations are described in detail. Signal-processing blocks which are not easily realizable are also described.

- A comparator constructed from TMSP blocks is presented in Chapter 4. Using a VTC and a time comparator a very simple and compact voltage comparator is realized, called a *time-mode comparator*. Using only digital circuitry, a calibration mechanism is introduced to remove the mismatch effects that would otherwise result in input-referred voltage offsets. Furthermore, the calibration circuitry is incorporated in the regular operation of the comparator and thus compensates for its own error contribution. An integrated circuit was fabricated implementing a time-mode comparator with calibration and the experimental results are presented in Section 4.4.

- Two flash ADC architectures are presented in Chapter 5 which take advantage of TMSP. The first flash ADC topology using a VTC followed by a time-to-digital converter. The advantages and limitations of this circuit are investigated. The second flash ADC design is built conventionally using 2^N-1 time-mode comparators and a resistor voltage divider circuit. A 7-bit flash ADC was fabricated in an integrated circuit and its experimental results are presented in Section 5.4.

- The design of first-order delta-sigma ADCs is explained in Chapter 6. It is constructed from two VTCs and a time comparator which offers an incredibly compact, low power, and high-speed design. Both single-ended-input and differential-input time-mode delta-sigma ADC designs are described in detail and they were fabricated in two separate integrated circuits. Their experimental results are presented in Section 5.4. Higher-order modulation and multi-bit quantization are discussed along with there implementations and limitations.

- The design of pipeline and cyclic ADCs using TMSP are presented in Chapter 7. They are constructed from VTCs, time-amplifiers, time-comparators, and digital logic. The time amplifier was modified from the circuit reported in [29] to provide the appropriate gain. An integrated circuit incorporating a cyclic

ADC was fabricated and the experimental results are presented in Section 7.3.

- The design of integrating and successive approximation register (SAR) ADCs using the TMSP methodology are discussed in Chapter 8. The time-mode SAR ADC is implemented with a time-mode comparator, a DAC, a sample-and-hold, digital control logic, and a register. The time-mode integrating ADC is composed of a time-mode integrator and digital logic. Although they were not fabricated, these designs are discussed along with MATLAB simulations to illustrate their operation.

Some of the work described in this thesis was presented at international conferences. Specifically, the time-mode comparator along with its calibration mechanism was presented at the 2006 International Symposium on Circuits and Systems. The single-ended input time-mode delta-sigma ADC was presented at the 2007 International Symposium on Circuits and Systems. This paper was awarded the second prize in the Best Student Paper competition which resulted in two invitations to journal publications in the Transactions on Circuits and Systems I.

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List of Acronyms

A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
ATE	Automated Test Equipment
CMOS	Complimentary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DLL	Delay-Locked Loop
DNL	Differential Nonlinearity
DR	Dynamic Range
DSP	Digital Signal Processing
EMI	Electromagnetic Interference
ENOB	Effective Number of Bits
FIB	Focused Ion Beam
FM	Frequency Modulation
FoM	Figure of Merit
HDL	Hardware Description Language
IC	Integrated Circuit
IF	Intermediate Frequency
INL	Integral Nonlinearity
LSB	Least Significant Bit

MiM	Metal-insulator-Metal
MSB	Most Significant Bit
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
PSD	Power Spectral Density
RF	Radio Frequency
RMS	Root-Mean-Square
S/H	Sample and Hold
SAR	Successive Approximation Register
SDA	Serial Data Analyzer
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise and Distortion Ratio
SoC	System-on-Chip
SR	Slew Rate
THD	Total Harmonic Distortion
TMΔΣADC	Time-Mode Delta-Sigma Analog-to-Digital Converter
TAMP	Time Amplifier
TMSP	Time-Mode Signal Processing
TMVC	Time-Mode Voltage Comparator
VCDU	Voltage-Controlled Delay Unit
VCO	Voltage-Controlled Oscillator
VDL	Vernier Delay Line
VLSI	Very Large Scale Integration
VTC	Voltage-to-Time Converter

Chapter 1: Introduction

1.1 - Motivation

An analog-to-digital converter (ADC) is a very popular circuit that transforms real world continuous-time analog information into a digital representation to be processed and stored in the digital domain. Digital signal processing (DSP) is dominating the processing, transport, and storage of analog information as it has been proven to be fast, accurate, reliable, and relatively inexpensive. A conventional analog data processing system, as illustrated in Figure 1.1, consist of an ADC, followed by a DSP, followed by a storage memory or a digital-to-analog converter (DAC) to supply the processed data to a real-world user interface or transmission medium.

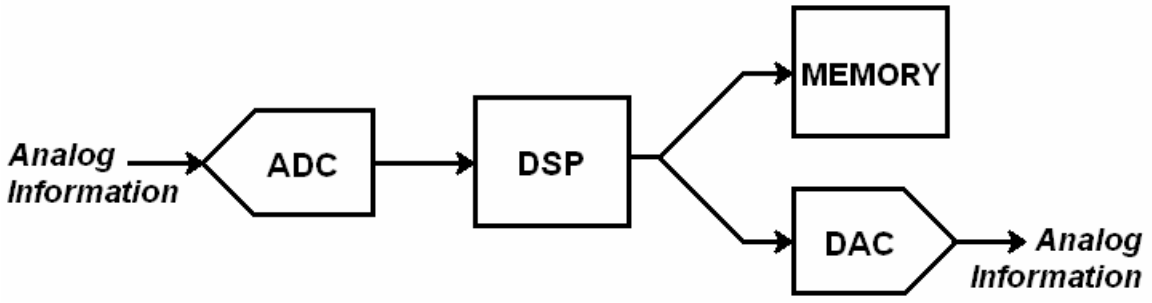


Figure 1.1: Conventional analog data processing system with DSP, storage memory, and DAC for analog re-transmission.

ADC circuits can be found in a wide range of applications such as communication systems, sensor networks, imaging and video applications, test and measurement apparatus, data acquisition systems, and consumer electronics such as cellular telephones, DVDs, digital cameras, and MP3 players. Each application requires ADCs with different performance specifications resulting in a wide range of commercially available ADC circuits. Selection of an ADC design is based on two main criteria: resolution and speed. The resolution of an ADC dictates how accurately the analog input will be represented by its digital output data. The speed of an ADC refers to the input signal bandwidth for which the analog-to-digital (A/D) conversion will maintain its quoted resolution. Two other important ADC criteria are power and area. ADC power consumption may be critical in battery operated devices or embedded systems such as system-on-chip (SoC) [1]. Silicon area usage may also be a serious concern in SoC designs.

Digital design is the driving force for the rapidly emerging deep submicron CMOS technologies. As such, CMOS processes are typically optimized for the needs of digital circuitry. In other words, CMOS technologies are being developed to improve digital switching speeds, lower the supply voltages, and reduce transistor geometries to increase the packing density of digital circuits. These pursuits have pushed the processing of digital information into the gigahertz frequency range. The need for digital, analog, and mixed-signal circuits to be integrated on a single die (i.e. SoC) is escalating as companies struggle to drive down cost, boost productivity, and create lower power and smaller devices.

There are many challenges in integrating analog and mixed-signal circuits in state-of-the-art digital CMOS technologies. As emerging CMOS technologies reduce feature size dimensions, transistor gate oxide thickness reduces forcing the system voltage to decrease. This negatively impacts analog and mixed-signal circuit performance by exercising transistors at non-optimal operating points and permitting currents to leak through transistor gates [2]. This dilemma results in

reduced input voltage swings and linearity problems for the processing of analog voltage signals. To upset the design challenge even further, area and power budgets are at best being preserved if not reducing. Additional implementation challenges are imposed when analog and mixed signal processing functions must coexist with digital circuits. The switching noise [3] from the digital circuitry may couple into the analog blocks thus corrupting analog information.

In order to offset some of the ADC design challenges imposed by digitally-driven deep submicron CMOS processes, a potential candidate to replace conventional voltage signal processing is being investigated, referred to as *time-mode signal processing* or TMSP. Although the concept of TMSP is fairly new, several works have begun to investigate its potential in many applications including A/D conversion [4] – [11]. The A/D conversion process using the TMSP methodology is depicted in Figure 1.2. Since most information begins in the form of a voltage, a voltage-to-time converter (VTC) is employed to convert the input signal into a time signal. The time signal is then processed by various circuits resulting in an output time signal. Finally, the processed time signal is transformed into a digital representation using a time-to-digital converter (TDC).

The circuits involved in the time-mode ADC processing are comprised of a digital CMOS construction. Therefore, this system offers all the benefits of the digital CMOS technology. Specifically, TMSP circuits will operates at high speeds, consume low power, and occupy small silicon area. Moreover, these performances specifications will improve with newer and smaller digitally-driven CMOS technologies.

Figure 1.2: Analog-to-digital conversion process via time-mode signal processing.

1.2 - Thesis Scope

The research described in this thesis aims to address the growing need for innovative circuit design techniques that will permit and continue the integration of high-performance analog-to-digital converters in emerging state-of-the-art digital CMOS technologies. This broad objective is narrowed down to a classification of circuits and signal processing techniques referred to as time-mode signal processing or TMSP.

The primary discovery goal is achieved by first defining the TMSP methodology and then describing its signal processing circuits in the context of analog-to-digital conversion. Several experimental circuits were designed and fabricated to demonstrate the feasibility of the proposed TMSP circuit design technique. Specifically, this thesis reveals that the TMSP methodology, when used in analog-to-digital conversion, can achieve high sampling speed and low power circuit designs while occupying very little silicon area. It should be noted, however, that the experimental ADCs designed herein demonstrate only mediocre effective resolutions due to the non-linearity of some of the CMOS circuits involved. Nevertheless, the proposed methodology offers an interesting alternative to conventional ADC design techniques with great potential.

1.3 - Thesis Overview

This thesis is organized into eight chapters excluding this introduction. Each chapter is described as follows.

Chapter 2 presents the concept of analog-to-digital (A/D) conversion. The theoretical and mathematical basis of A/D conversion is explained. ADC design specifications are presented along with performance metrics used to characterize

ADCs. The five main ADC architectures are introduced while offering insight into their application space.

The concept of time-mode signal processing as it applies to A/D conversion is explored in Chapter 3. Various system blocks and transistor circuits to implement the TMSP functions, which will be used throughout this work, are described.

A time-mode voltage comparator design is presented in Chapter 4. The design was incrementally modified to compensate for process variation using an all-digital calibration scheme. The time-mode comparator with calibration was fabricated in 0.18-μm CMOS technology and its experimental results are presented.

Chapter 5 outlines the use of TMSP to construct flash ADCs. Two flash architectures are described. An integrated circuit was manufactured incorporating a 7-bit time-mode flash ADC. Its design and experimental results are also presented.

Chapter 6 describes a delta-sigma (ΔΣ) A/D conversion technique using the TMSP blocks presented in Chapter 3. First-order single-bit ΔΣ designs were explored in depth for both single-ended and differential inputs. Multi-bit and higher-order designs are investigated. Each of these ΔΣ circuit variants were modeled and simulated in MATLAB and HSPICE. The first-order single-bit single-ended and differential input ΔΣ ADCs were fabricated in a standard 0.18-μm CMOS technology and the experimental results are revealed in Chapter 6.

Pipeline and cyclic A/D conversion is described in Chapter 7, again in the context of TMSP. The TMSP circuit blocks that comprise the time-mode cyclic ADC are described in detail. The design was fabricated in a 0.18-μm CMOS technology, and the experimental results are presented.

For completeness, the time-mode implementation of successive approximation register and integrated ADCs are described in Chapter 8. MATLAB system level simulations were performed to aid in the discussion and understanding of these time-mode ADC topologies.

Finally, this dissertation is concluded in Chapter 9 where the work is summarized, strengths and weaknesses are highlighted, and future advancements of this work are offered.

Chapter 2: Analog-to-Digital Conversion

An analog-to-digital converter (ADC) is a circuit that samples continuous-time analog information and converters it into a discrete digital representation. Analog-to-digital (A/D) conversion may be viewed as a two-step process. Figure 2.1 demonstrates the ADC process where in the first step a continuous-time analog input signal is sampled at discrete instances of time. In the second step the sampled analog amplitude is quantized. The error between the true input analog value and the quantized digital output value is known as the quantization error ε_q.

Figure 2.2(a) displays a block diagram of an ADC. The continuous-time analog input, typically a voltage signal, can be any value between zero and the full-scale

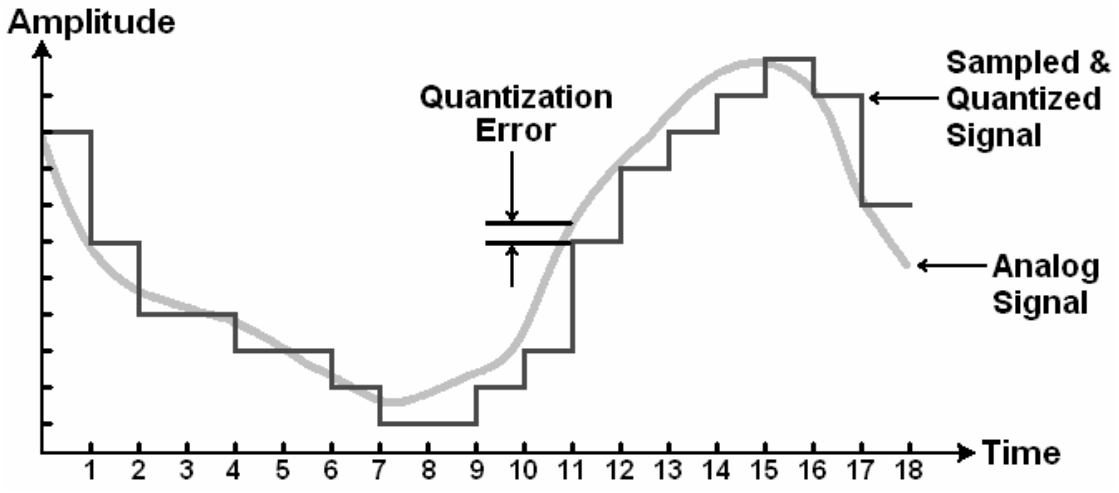


Figure 2.1: Analog-to-digital conversion process example.

amplitude A_{FS}. The digital output is a binary number where the number of digits (i.e. bits) dictates the converter's resolution. The ADC resolution is defined by the smallest analog input change that will result in a least significant bit (LSB) digital output code change. If there are N output bits, then the ADC may resolve 2^N analog levels. The digital output is represented as

$$D_{OUT} = d_{N-1}d_{N-2}d_{N-3}...d_2d_1d_0\,, \tag{2.1}$$

where d_{N-1} is the most significant bit (MSB) and d_0 is the LSB. The input analog value A_{IN}, digital output bits D_{OUT}, and quantization error ε_q are related by the expression

$$A_{IN} = A_{FS}\left(\frac{d_{N-1}}{2^N} + \frac{d_{N-2}}{2^{N-1}} + ... + \frac{d_1}{2^2} + \frac{d_0}{2^1}\right) + \varepsilon_q\,. \tag{2.2}$$

An example transfer characteristic of an ADC is offered in Figure 2.2(b). In this case the ADC has a 3-bit resolution (i.e. N=3) and the LSB is given by

$$LSB = \frac{A_{FS}}{2^N - 1}\,. \tag{2.3}$$

In a perfect ADC the quantization error is bounded between ±LSB/2. If it is assumed that the quantization error signal is uncorrelated with the input signal and that it is uniformly distributed within ±LSB/2 then we may approximate the

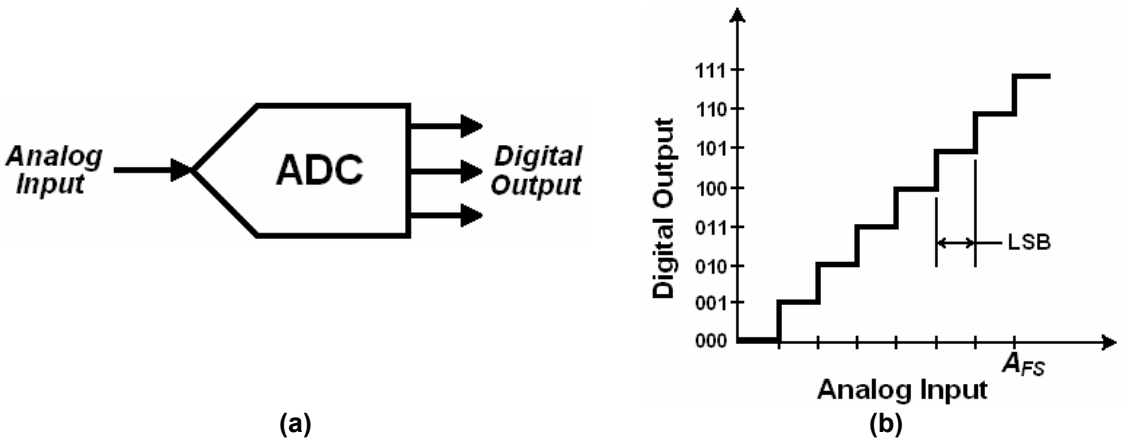


Figure 2.2: Analog-to-digital converter (ADC) (a) block diagram; (b) transfer characteristic.

power of the quantization noise as

$$P_{\varepsilon} = \frac{LSB^2}{12} = \frac{\left(\frac{A_{FS}}{2^N - 1}\right)^2}{12}. \tag{2.4}$$

There are two classifications of ADC based on their conversion rate: Nyquist rate and oversampled. Nyquist-rate data converters sample the input at a frequency which is greater than two times that of the input signal bandwidth (i.e. at the Nyquist frequency). Flash, pipeline, SAR, and integrating ADCs all participate in this category. Oversampled ADCs process the input signal at a much higher conversion rate. Delta-sigma ADCs fulfill this classification.

There are many applications for ADCs with varying performance criteria. For example, measurement systems require high-resolution converters, video processing applications need high-speed ADCs, and battery operated devices use lower power designs. Therefore Section 2.1 is dedicated to the design specifications used to measure and compare ADCs. Section 2.2 presents the performance metrics and figure of merits of ADCs. There are five fundamental ADC processing algorithms and circuit topologies: flash ADCs, pipeline ADCs, successive approximation register ADCs, delta-sigma ADCs and integrating ADCs. Each of these conversion strategies are described in Section 2.3.

2.1 - ADC Design Specifications

There are many design requirements when selecting an ADC topology and implementing its circuitry. They are: signal bandwidth or sampling rate, resolution, distortion, power, area, noise immunity, dynamic range, and latency. Each of these specifications will be described separately in the following subsections.

2.1.1. Signal Bandwidth or Sampling Rate

The signal bandwidth of an ADC is typically defined as the frequency range over which the ADC will maintain its quoted resolution. Signal bandwidth and clock sampling rate of an ADC are related by the Nyquist criterion. In other words, the sampling rate is at least twice the signal bandwidth. There are many applications requiring A/D conversion some of which are presented in Table 2.1 along with their required sampling rates. The information in Table 2.1 was compiled from the data sheets found in [12], [13], and [14]. It may be seen that applications span and overlap almost the entire frequency spectrum up to 4 GHz.

Table 2.1: ADC applications and their intended bandwidths and required resolutions.

Application	Sampling Rate	Resolution (bits)
Sensors Energy monitoring Motor-control	1 – 100 Hz	16 – 24
Audio market (computer audio, CD, FM stereo, digital audio tape, DVD audio)	48 – 192 kHz	12 – 16
Data acquisition systems Instrumentation applications ATE	500 kHz – 5 MHz	12 – 18
Medical Imaging	5 – 200 MHz	10 – 16
Communication (IF sampling, base stations)	30 – 100 MHz	10 – 14
Instrumentation (digital oscilloscopes, spectrum analyzers)	5 – 100 MHz	10 – 14
Consumer electronics (digital cameras, display electronics, DVD, HDTV)	5 – 75 MHz	10 – 12
Digital Video	29 – 100 MHz	12 – 14
Software Defined Radio	125 – 500 MHz	12 – 14
Test & Measurement Direct RF Down conversion High-Speed Data Acquisition	0.5 – 4 GHz	6 – 8

2.1.2. Resolution

Resolution of an ADC is a measure of how accurately the digital output will represent the analog input. It may be defined as the smallest analog input change that will results in an LSB change in the digital output code. Resolution is often expressed in number of bits N in the digital output. Hence, there are 2^N digital output possibilities. Table 2.1 presents several applications and their required resolutions. Note that resolution and sampling rate are generally inversely related.

Quantization error is related to the resolution of an ADC and generates a noise floor in the power spectral density of an ADC's output. The power of this noise floor may be approximated by Equation (2.4).

2.1.3. Distortion

The nonlinearity of semiconductor devices and the mismatch between identical circuit components may produce distortion in the output of an ADC. Layout techniques [15] such as common centroid configurations may be implemented to reduce mismatch. Many calibration mechanisms have been reported to compensate for mismatch, such as laser-trimming, offset cancellation [16], dynamic element matching (DEM) [17], and calibration look-up tables [18]. Regardless of these efforts distortion is a rapidly growing problem in the integration of analog and mixed-signal CMOS circuits designed in state-of-the-art digital CMOS processes.

2.1.4. Dynamic Range

As emerging CMOS technology scales down, the transistor gate oxide thickness reduces which forces the supply voltage to decrease. Consequently, the linear operating region of a transistor circuit decreases thus reducing the usable input voltage signal swing of an ADC. The dynamic range of an ADC is loosely

defined as the range of input amplitudes which are larger than the noise and distortion from the system. Therefore, the dynamic range of an ADC will suffer if the signal swing is reduced, or if the noise or distortion is increased.

2.1.5. Power

An important goal in any circuit design is to minimize its power consumption. In large VLSI systems where digital, analog, and mixed-signal components are integrated together, the maximum power dissipation is often stipulated and governed by circuit reliability issues and power supply restrictions (e.g. battery-powered devices). As such, a power budget is allocated to an ADC. The control of power dissipation is achieved with architectural selection and circuit design techniques.

2.1.6. Area

When a design is laid out in a silicon-based technology it inevitably occupies an area. Cost of silicon grows proportionally with area. Moreover, CMOS processes are subject to defects within the technology. Statistically the density of these defects will affect larger circuits. Therefore, minimizing area will reduce cost and decrease the probability that a circuit fails due to defects.

2.1.7. Noise Immunity

All electronics circuits are subjected to random environmental and external noise sources such as thermal noise, flicker noise, cross talk, power supply noise, clock jitter, and electromagnetic interference (EMI). Thermal noise may be reduced significantly by circuit design techniques while cross talk may be eliminated with layout techniques. Power supply noise and clock jitter are external influences to an ADC and will seriously affect its performance if the supply and clock source are not designed with care.

2.1.8. Latency

Latency in ADCs refers to the number of clock cycles between the sampling of the analog input signal and the instance when the digital data is presented to the ADC output. Latency is an important design consideration for real-time data conversion systems.

2.2 - ADC Performance Metrics and Figures of Merit

Metrics and figures of merit are used to evaluate the performance, characterize, and compare ADCs. The most widely used measurements are described in the following subsections.

2.2.1. Gain and Offset Error

ADCs are typically designed with a unity gain such that the full scale input voltage range maps uniformly to the 2^N different digital output codes. In some cases, exemplified in Figure 2.3(a), the gain differs from unity. The input voltage range is decreased when the gain is greater than unity, however all digital codes

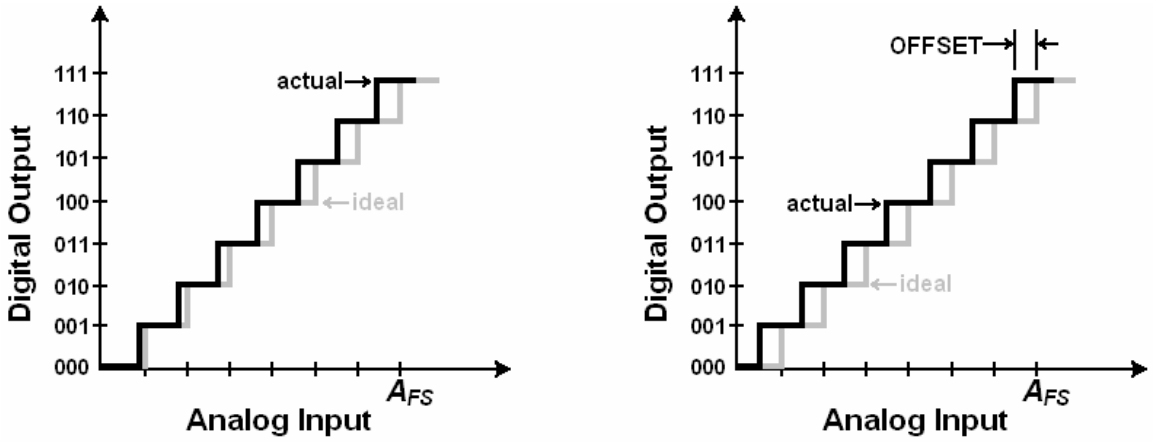


Figure 2.3: 3-bit examples of ADC (a) gain error and (b) offset error.

exist as shown in Figure 2.3(a). If the gain is reduced from unity then the most significant digital codes may never be exercised. Another result of ADC gain error is that the length of an LSB is modified such that

$$LSB = G\frac{A_{FS}}{2^N - 1}, \tag{2.5}$$

where *G* is the gain factor which deviated from unity.

Offset error is a common problem in some ADC designs resulting in the digital code transitions occurring at input voltages which are offset from the ideal ADC design, as illustrated in Figure 2.3(b). Offset is easily calibrated in many ADC designs.

2.2.2. Integral Nonlinearity

Integral nonlinearity (INL) is a measure of the deviation of an ADCs output transfer characteristic from a straight line. Figure 2.4(a) shows a 3-bit ADC example. The straight line may be drawn as a best fit line, as shown in the figure, or it may be drawn between the end points. INL is typically measured in the number or fraction of LSBs that the actual transitions occur from the straight line. A linear ADC must have its INL error bounded between ±0.5 LSBs.

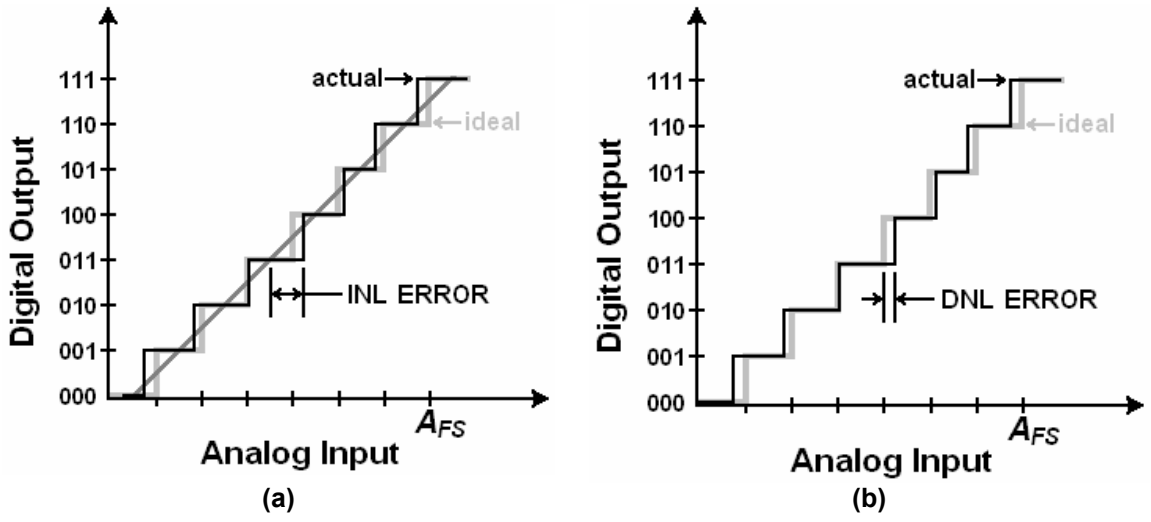


Figure 2.4: 3-bit ADC linearity error examples of (a) integral nonlinearity (INL); (b) differential Nonlinearity (DNL).

2.2.3. Differential Nonlinearity

The differential nonlinearity (DNL) error of an ADC is defined as the difference between the ideal step width and the width of an ideal LSB. Figure 2.4(b) shows an example of a 3-bit ADC with its DNL error. If the DNL error exceeds 1 LSB then there is a possibility that missing codes or non-monotonic behaviour will result.

2.2.4. Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of the RMS value of the input signal V_{INRMS} to the RMS value of the sum of all other spectral components (i.e. noise) $V_{NOISERMS}$ over a defined bandwidth excluding the harmonics and DC component. SNR is usually expressed in decibels using the formula

$$SNR = 20\log\left(\frac{V_{IN_{RMS}}}{V_{NOISE_{RMS}}}\right). \tag{2.6}$$

The noise information may be comprised of quantization, thermal, flicker, jitter-induced, power supply, or EMI noise. In the case where the noise is only due to quantization error, then the signal-to-quantization noise ratio (SQNR) is expressed as

$$SQNR = 20\log\left(\frac{V_{IN_{RMS}}}{V_{QN_{RMS}}}\right), \tag{2.7}$$

where V_{QNRMS} is the RMS quantization noise. An ADC's resolution, expressed in number of bits, may be deduced from the SQNR using

$$resolution = \frac{SQNR - 1.76}{6.02}. \tag{2.8}$$

2.2.5. Signal-to-Noise-and-Distortion Ratio

The signal-to-noise-and-distortion ratio (SNDR) is the ratio of the RMS value of the input signal V_{INRMS} to the RMS value of the sum of all other spectral

components over a defined bandwidth including noise $V_{NOISERMS}$ and distortion $V_{DISTORTIONRMS}$, but excluding the DC component. SNDR is usually expressed in decibels using the formula

$$SNDR = 20\log\left(\frac{V_{IN_{RMS}}}{V_{NOISE_{RMS}} + V_{DISTORTION_{RMS}}}\right). \quad (2.9)$$

2.2.6. Effective Number of Bits

An alternate expression for SNDR is to represent it in bit resolution, called the effective number of bits (ENOB). ENOB may be computed from SNDR using the expression

$$ENOB = \frac{SNDR - 1.76}{6.02}. \quad (2.10)$$

2.2.7. Total Harmonic Distortion

A measure of the ratio between the input signal RMS value and just the harmonically-related distortion components $V_{DISTORTIONRMS}$ is called total harmonic distortion (THD) and is expressed in decibels with the equation

$$THD = 20\log\left(\frac{V_{IN_{RMS}}}{V_{DISTORTION_{RMS}}}\right). \quad (2.11)$$

2.2.8. Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is defined as the ratio between the RMS values of the input signal V_{INRMS} to the RMS value of the greatest spurious tone in the output signal spectrum $V_{SPURRMS}$. It is conventionally expressed in decibels using the formula

$$SFDR = 20\log\left(\frac{V_{IN_{RMS}}}{V_{SPUR_{RMS}}}\right). \quad (2.12)$$

2.2.9. Figures of Merit

There are thousands of ADC designs which vary in circuit topology, technology, operating frequency, resolution, power consumption, and circuit area. In order to compare them fairly many authors use a figure of merit (*FoM*). For example, a very popular *FoM* [19] is using a measure of conversion step per unit energy

$$FoM_1 = \frac{2^{ENOB} \cdot 2 \cdot BW}{P}, \tag{2.13}$$

where *P* is the power dissipation and *BW* is the signal bandwidth of the ADC. Another variation of this *FoM* incorporates area per conversion step described by

$$FoM_2 = \frac{2^{ENOB} \cdot 2 \cdot BW}{P \cdot \left(A / 2^n\right)}, \tag{2.14}$$

where *A* is the circuit area and *n* is the converter's desired bit resolution.

2.3 - Conventional Analog-to-Digital Converters

There are five main ADC topologies: flash, pipeline, successive approximation register (SAR), delta-sigma, and integrating. Each of these architectures is best suited for particular applications based on sampling frequency, resolution, power, and area requirements. Figure 2.5 shows the intended operating region for each ADC topology in the context of Nyquist conversion speed versus resolution. Each of the five ADC designs is introduced in the following subsections.

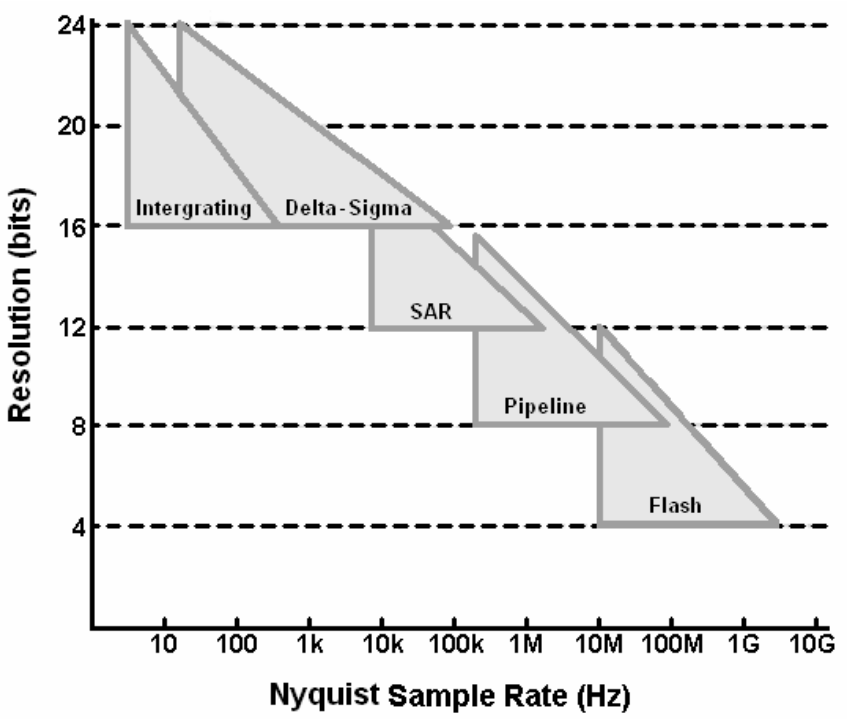


Figure 2.5: Comparison between five ADC topologies demonstrating their intended Nyquist sampling rates and their typical resolutions.

2.3.1. Flash Analog-to-Digital Conversion

The flash ADC uses comparators in parallel whereby each compares the analog input signal to a different analog reference value. A typical flash ADC architecture is depicted in Figure 2.6. An *N*-bit flash ADC would require 2^N-1 comparators. In this example, the reference voltages are generated by a resistor string voltage divider. The comparator outputs form a thermometer code which is encoded to generate a binary number.

Due to the parallelism the greatest benefit of a flash ADC is its extremely fast operating speed. Consequently, all other design specifications suffer. The resolution of the flash ADC is restricted by the power and area that the 2^N-1 comparators occupy. Typically, flash converters are limited to a resolution below 8-bits. Mismatch within each comparator, between all comparators, and between

resistors will result in non-linear distortion mechanisms that will severely cripple the flash ADC performance.

The comparator output is a thermometer code. This implies that there should be only one transition between logic 0 and logic 1 when traversing from the LSB to the MSB. However, it may happen that a logic 1 may appear between two logic 0 outputs. This is known as a bubble error. If the thermometer code is convertered directly with a priority encoder, then the wrong binary data may result. Therefore, it is also the responsibility of the encoder to remove bubble errors.

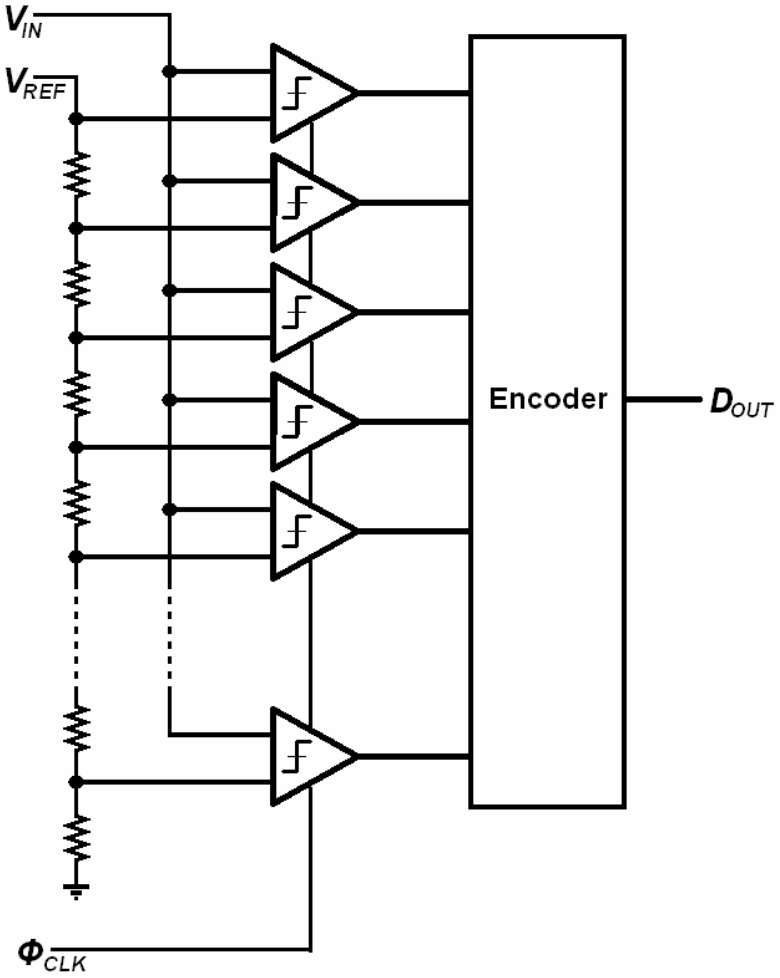


Figure 2.6: Flash ADC.

2.3.2. Pipeline and Cyclic Analog-to-Digital Conversion

A pipeline ADC is presented in Figure 2.7(a) and consists of *M* conversion stages and circuitry to digitally align the output. Each individual stage, shown in Figure 2.7(b), samples the analog input voltage V_{IN} using a sample-and-hold circuit, converts V_{IN} into a *b*-bit digital word using a flash ADC, and produces a residual voltage V_R. The residual voltage is the difference between the stage input voltage and the digital output converted into voltage via a DAC multiplied by a gain factor of 2^b. For example, if $b = 2$ then

$$V_R = 2^2\left(V_{IN} - V_{FS}\left(\frac{d_1}{2^2} + \frac{d_0}{2^1}\right)\right), \tag{2.15}$$

where V_{FS} is the full scale voltage of the input signal and consequently is used

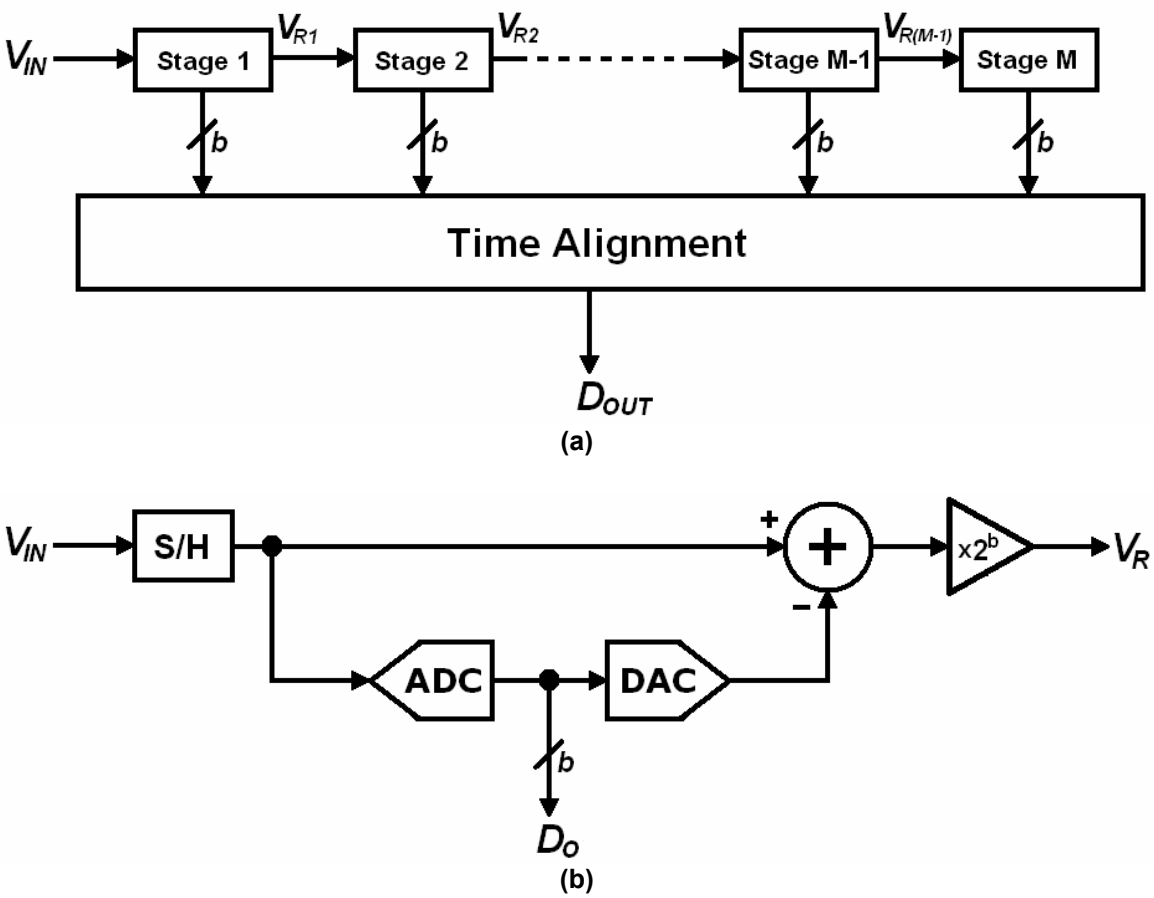


Figure 2.7: Pipeline ADC (a) complete design with M stages; (b) individual stage.

as the DAC reference voltage. Typically, the number of bits *b* is between one and four to relax the requirements of the ADC.

Once the first pipeline stage has completed its processing of an input sample, it is passed to the next stage. At the same time, the first stage begins to process the next input sample. This action is know as *pipelining* and accounts for the high data throughput since the entire converter may operated on *M* input samples simultaneously. The digital data corresponding to a single input sample is propagated through the pipeline resulting in misalignment of the data and data latency. Shift registers are used to perform time alignment on the data. However, the latency of the pipeline architecture is inevitable.

The flash ADC, DAC, and amplifier in each pipeline stage will be influenced by process variation thus limiting their accuracy. Error correction mechanisms are extensively implemented to reduce the ADC requirements. A popular correction scheme is to produce an extra bit from each pipeline stage while maintaining the amplifier gain. This overlapping bit provides sufficient redundancy such that comparator offsets in the flash ADCs will be compensated. However, the gain and linearity error in the DACs and amplifiers cannot be fixed by this error

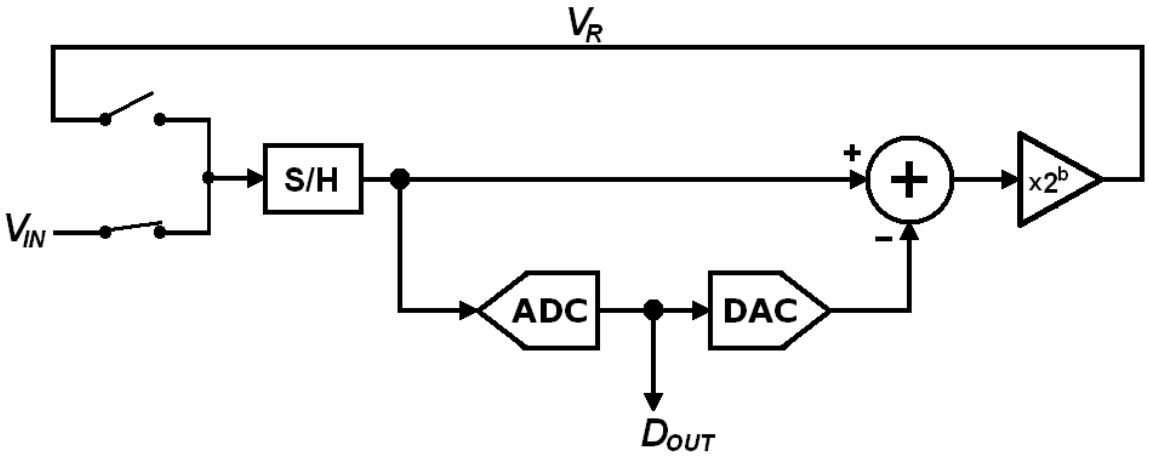


Figure 2.8: Cyclic or algorithmic ADC.

correction strategy. Hence, a calibration scheme would also need to be applied.

In order to minimize power and area consumption, the pipeline ADC may be converted into a cyclic or algorithmic architecture, as illustrated in Figure 2.8. This design uses only one pipeline stage and feeds back the residue voltage V_R through a switch to be processed by the same stage. The cyclic ADC no longer benefits from the speed of the pipelining, however it consumes significantly less power and occupies a much smaller silicon area. Furthermore, only one ADC, DAC and amplifier need to be calibrated. The data latency problem no longer exists for the cyclic design as it may only process one sample per clock period.

Pipeline ADCs are perhaps the most popular ADC conversion strategy as the offer the best compromise between speed and resolution.

2.3.3. Successive Approximation Register Analog-to-Digital Conversion

A successive approximation register (SAR) ADC operates by sampling the analog input voltage and performing a binary search to determine a digital word that will equal the input when converted into a voltage through a DAC. Figure 2.9 presents a typical SAR ADC architecture. The binary search is implemented by initiating the register output D_{OUT} to the mid-scale digital value. In other words, the MSB is set to logic 1 and all the remaining bits are set to logic 0, for example '1000 0000'. The digital output is convertered to voltage through a DAC and

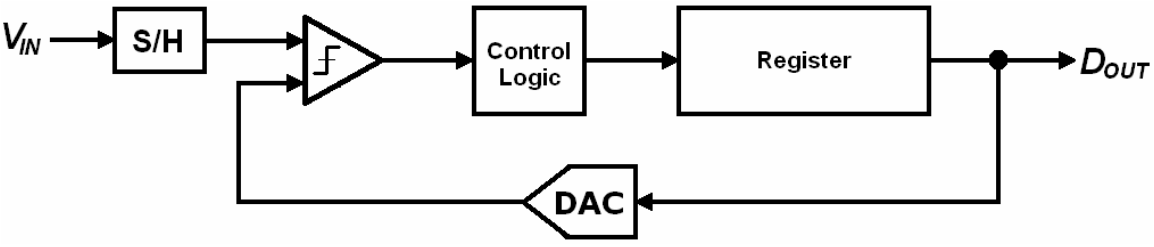


Figure 2.9: Successive approximation register (SAR) ADC.

compared to the sampled input. If the input is greater than the DAC output, then the MSB is kept and next significant bit is set to logic 1. If the DAC output is greater than the sampled input voltage, then the MSB is changed to logic 0 and the next significant bit is set to logic 1. The register output is converted back into a voltage and the comparisons continue until all register bits have been determined.

SAR ADCs offer a medium-to-high resolution solution at sampling speeds below a few megahertz. They are more commonly used in low power and small area applications. The accuracy and speed of the SAR ADC is highly dependant on the DAC and comparator components. More specifically, the performance of these components must be as accurate as the overall system.

2.3.4. Delta-Sigma Analog-to-Digital Conversion

Delta-sigma (ΔΣ) analog-to-digital conversion is a unique classification of data converter which uses the technique of oversampling and feedback to achieve high resolutions. The operation of a ΔΣ ADC is best described with the error-feedback model shown in Figure 2.10(a). The input value V_{IN} is converted to a digital signal D_{OUT} through a quantizer ADC block. The digital output is converter back into an analog value V_{OUT} using a DAC. V_{OUT} is subtracted from the current input V_{IN} to produce the error signal E_q, which represents the ADC's quantization error. The quantization error signal is subtracted from the next input value to be converted. A time-domain analysis of models in Figure 2.10 will reveal the difference equation

$$V_{OUT}(n) = V_{IN}(n-1) + \left[E_q(n) - E_q(n-1)\right]. \tag{2.16}$$

It may be observed from Equation (2.16) that the quantization error may be significantly reduced if the current error and previous error samples are close in magnitude. This would be the case since the input signal is sampled at a much

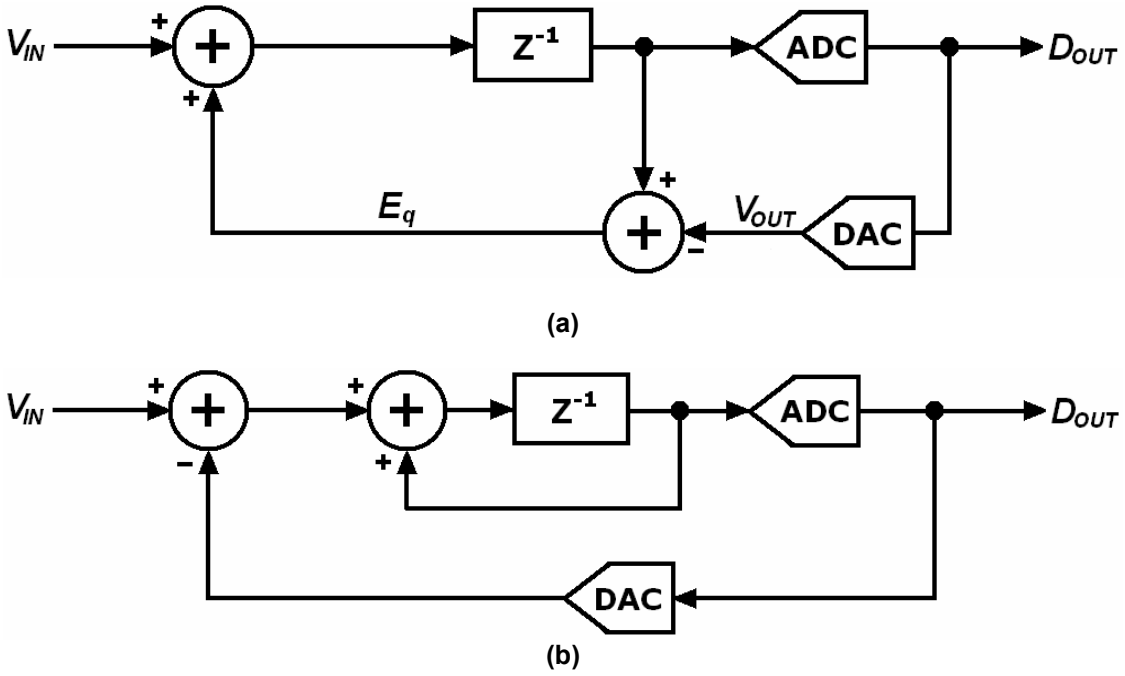


Figure 2.10: First-order delta-sigma ADC: (a) error-feedback model, (b) output-feedback model.

greater rate than its frequency (i.e. oversampled) and hence it changes relatively slowly with respect to the sampling clock frequency. As a result, the low frequency spectral content of the quantization noise is transformed into higher frequency components. This process is known as *noise-shaping*.

The Implementation of ΔΣ ADCs is commonly based on the output-feedback model, illustrated in Figure 2.10(b), which is formed by simply rearranging the error-feedback model. The internal positive feedback loop formed with the delay element is an analog integrator. The outer negative feedback loop requires an analog summation block. The most common ΔΣ ADC configurations use a single-bit quantizer (i.e. a comparator). This is because the use of a 1-bit quantizer would necessitate a 1-bit feedback DAC, which are both perfectly linear. Multi-bit quantizers are frequently used to reduce the quantization error feedback and are typically restricted to within one to four-bit resolutions.

The oversampling behaviour of a ΔΣ ADC gives rise to the term oversampling ratio (OSR). This quantity, expressed as

$$OSR = \frac{F_S}{2F_O}, \tag{2.17}$$

reflects how much greater the sampling frequency F_S is over the Nyquist rate $2F_O$, where F_O is largest input signal tone that would exercise the ADC.

The signal-to-quantization-noise ratio (SQRN) for a ΔΣ ADC [20] with a first-order integrator may be calculated with

$$SQNR = 6.02N + 1.76 + 10\log(OSR), \tag{2.18}$$

where N is the bit resolution of the quantizer ADC. Therefore, for a first-order design, the resolution of a ΔΣ ADC is governed by the quantizer's resolution and the oversampling ratio. Equation (2.18) along with technology constraints poses an upper bound on the performance of first-order ΔΣ ADC systems. As previously mentioned, the quantizer and feedback DAC should not exceed 4-bit resolution as the linearity of the overall system will be jeopardized. Moreover, the OSR will be constrained by an applications bandwidth and fastest sampling rate that a technology will permit.

Higher-order ΔΣ ADCs, which increase the number of integrators, offer significant SQNR improvements. For example, the SQNR for the second-order ΔΣ ADC in Figure 2.11 [20] may be expressed as

$$SQNR = 6.02N - 11.14 + 50\log(OSR). \tag{2.19}$$

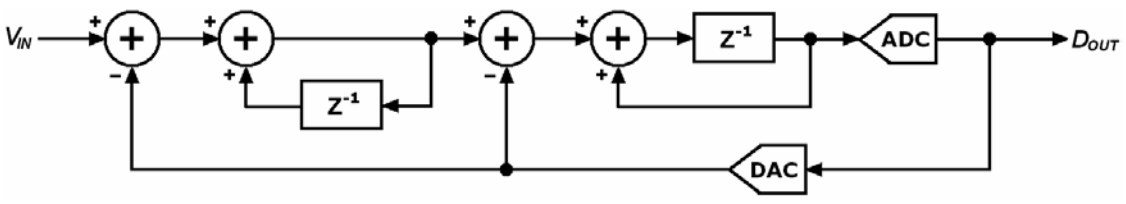
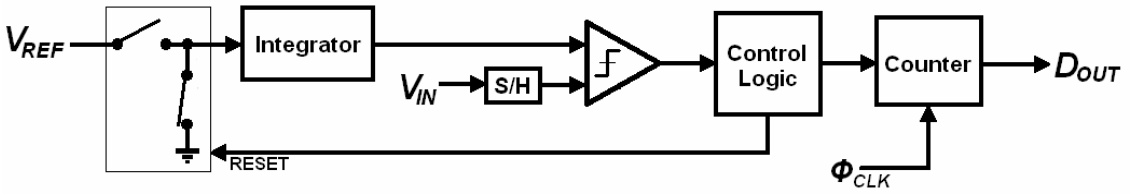


Figure 2.11: Second-order delta-sigma ADC.

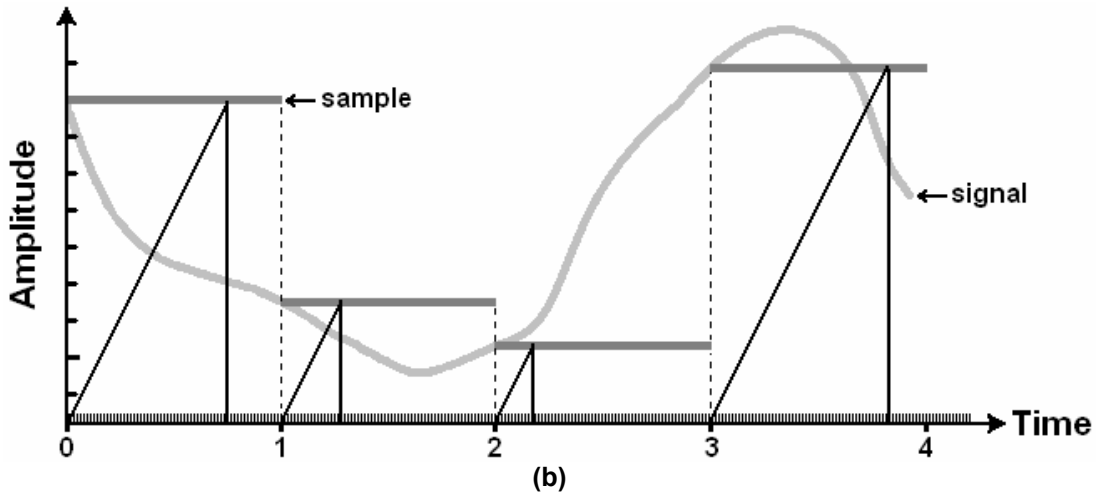
It may be inferred from Equations (2.18) and (2.19) that if the OSR is doubled for a first-order ΔΣ ADC, the SQNR improves by 0.5-bits of resolution. Whereas, the second-order ΔΣ ADC improves by 2.5-bits. Third and higher-order ΔΣ ADCs will offer even better SQNR performance. However, all ΔΣ ADCs with more than one integrator may become unstable and must be designed with care.

2.3.5. Integrating Analog-to-Digital Conversion

The integrating single-slope ADC block diagram is presented in Figure 2.12(a) and an example of its operation is illustrated in Figure 2.12(b). It operates by integrating a reference voltage V_{REF} to generate a linear voltage ramp. At the start of the ramp a digital counter is started. The ramp is compared to a sample of the input voltage V_{IN}. Once the comparator output switches the counter output



(a)

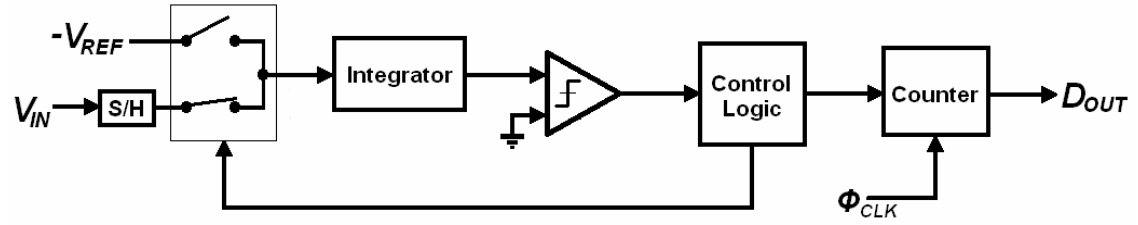


(b)

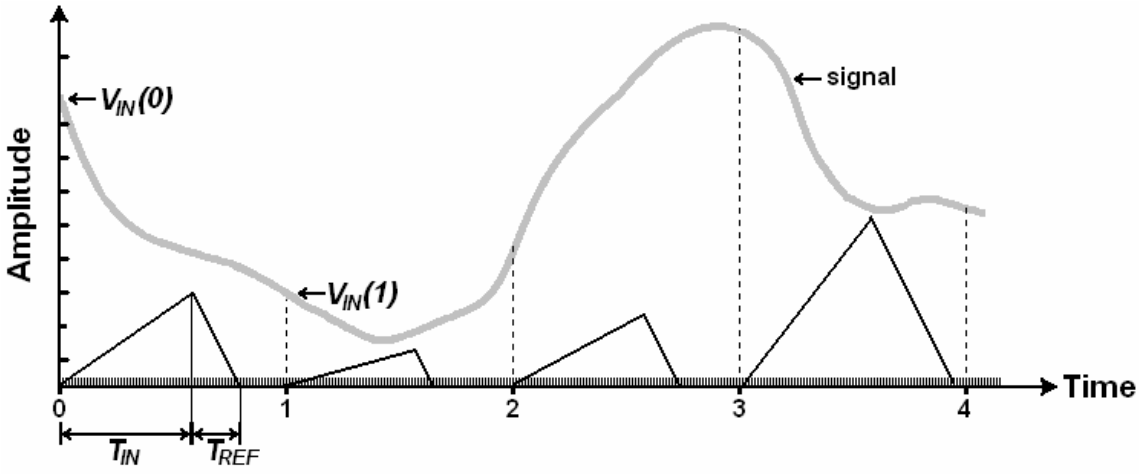
Figure 2.12: Integrating single-slope ADC (a) functional block diagram; (b) example operation.

represents the digitized input voltage and the design is reset for the next input sample.

The repeatability of the single-slope design is dependant on the integrator's accuracy. To overcome the integrator's sensitivity to process variation, a dual-slope architecture may be used. The integrating dual-slope ADC block diagram is illustrated in Figure 2.13(a) with its operation exemplified in Figure 2.13(b). It operates by first integrating the sampled input voltage V_{IN} for a fixed time interval T_{IN}. T_{IN} is calculated using a digital clock signal and counter circuit. At the end of T_{IN}, a de-integration is performed using a negative reference voltage ($-V_{REF}$). The time (i.e. the number of digital clock pulses) it takes for the integrator output to



(a)



(b)

Figure 2.13: Integrating dual-slope ADC (a) functional block diagram; (b) example operation.

return to analog ground is recorded as T_{REF}. Finally, the digital count T_{REF} is proportional to V_{IN} and is expressed as

$$T_{REF} = T_{IN} \frac{V_{IN}}{V_{REF}} . \tag{2.20}$$

Integrating ADCs offer very high resolutions when the integration process is slow thus permitting TREF to consist of many clock periods. For example, a 24-bit ADC being clocked at 1 GHz may be achieved if the signal bandwidth is below (1 GHz / 2^{24}) or 30 Hz. Therefore, integrating ADCs are used mainly for extremely low speed applications.

2.4 - Summary

The process of analog-to-digital conversion was introduced in this chapter. Analog-to-digital converter design specifications such as resolution, signal bandwidth, and power were described. Measurement and performance metrics such as signal-to-noise ratio, integral nonlinearity, and effective number of bits were presented. Finally this chapter described the five main ADC architectures: flash, pipeline, successive approximation register, delta-sigma, and integrating ADCs.

Chapter 3: Time-Mode Signal Processing Circuits

Time-mode signal processing (TMSP) may be defined as the detection, storage, and manipulation of sampled analog information using time-difference variables. Furthermore, we define a time-difference variable, ΔT, as the quantity of time between an event occurring with respect to a reference time or event. In the context of this work, a time-difference variable refers to the time interval between two digital clock edges. Figure 3.1 demonstrates two digital clock signals, ϕ_1 and ϕ_2, and the time-difference variable, ΔT, represented as the time interval between the two clock edge transition times t_1 and t_2. Note that time-difference variables are discrete samples of analog information. Time-difference variables will be synonymously interchanged with time-mode signals.

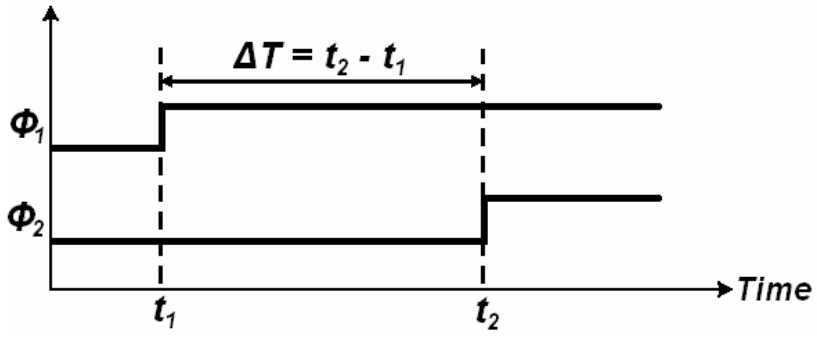


Figure 3.1: Timing diagram example demonstrating a time-difference variable ΔT as the difference between two digital clock rising edge transition times.

The process of converting analog voltages into digital information using time-mode signal processing as an intermediate step is illustrated in Figure 3.2. The input voltage signal is first converted into a time-mode signal using a voltage-to-time converter. The time-mode signal is processed and then converted into a digital representation using a time-to-digital converter. Each of these blocks and their associated circuits are described in the following sections.

3.1 - Voltage-to-Time Conversion

Voltage-to-time conversion is the process of sampling an analog voltage and converting it into an analog time-difference variable. This process is facilitated using a device called a *voltage-controlled delay unit*. The voltage-controlled delay unit and the CMOS circuits that implement them are described in the section 3.1.1. The voltage-to-time converter is presented in subsection 3.1.2.

3.1.1. Voltage-Controlled Delay Unit

A voltage-controlled delay unit (VCDU) is a circuit that proportionally delays an input time event (i.e. a clock edge) with respect to a sampled input voltage. The VCDU block diagram that will be used throughout this work is illustrated in Figure 3.3(a). Regardless of its implementation, a VCDU has two inputs; an initial or reference event ϕ_{CLK}, and the sampled input voltage $V_{IN}(n)$ that controls the delay of ϕ_{CLK}. There are two ways to interpret the output of the VCDU: physically or

Figure 3.2: Block diagram of the analog-to-digital conversion process via time-mode signal processing.

conceptually. The physical output of the VCDU $\phi_O(n)$ is a digital signal. The conceptual VCDU output is the time-difference variable $\Delta T_O(n)$. The time-difference variable $\Delta T_O(n)$ contains the signal information and will henceforth be used to describe the VCDU output. Figure 3.3(b) shows an example timing diagram of the VCDU operation. The VCDU output $\Delta T_O(n)$ is proportional to the input voltage $V_{IN}(n)$ with the voltage-to-time conversion factor G_ϕ.

The relationship which governs the linear conversion between voltage $V(t)$ and time t is given by

$$I(t) = C\frac{dV(t)}{dt}, \tag{3.1}$$

where C is some nodal capacitance and $I(t)$ is current. Equation (3.1) may be rearranged to obtain time as the dependant variable, such as

$$dt = \frac{C}{I(t)}dV(t). \tag{3.2}$$

Equation (3.2) suggests that there are two ways to generate time-mode variables: via voltage control or current control.

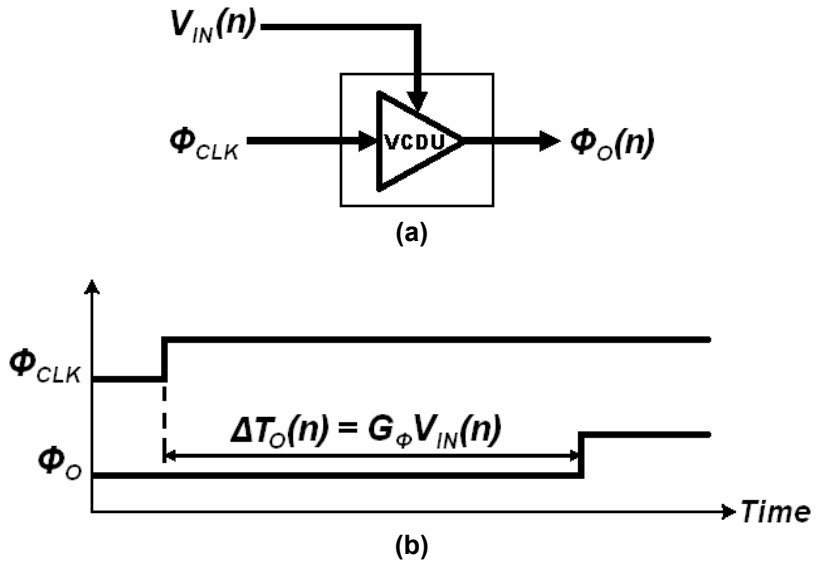


Figure 3.3: Voltage-controlled delay unit (VCDU): (a) block diagram; (b) example timing diagram.

Figure 3.4 demonstrates a general VCDU design to implement either strategy.

Direct Voltage-Controlled VCDU Strategy

Direct voltage-controlled delay is generated by forcing the charging of capacitor *C* using a constant current I_{IN}. Initially the capacitor is reset to zero volts while the digital clock signal ϕ_{CLK} is low. Charging begins with respect to the rising edge of the clock. The comparator output switches from logic 0 to logic 1 once the voltage on the capacitor reaches the desired input voltage $V_{IN}(n)$. Hence, the output time-difference $\Delta T_O(n)$ is the time interval between the input clock and comparator output switching times. The equation describing the conversion process is given by

$$\Delta T_O(n) = \frac{C}{I_{IN}} V_{IN}(n) = G_\phi V_{IN}(n), \tag{3.3}$$

where the voltage-to-time conversion factor G_ϕ is equal to C/I_{IN}.

The direct voltage-controlled VCDU strategy is directly realizable from Figure 3.4. In other words, a constant current source is implemented to charge a capacitor at the rate of C/I_{IN} sec/V. A comparator is incorporated to compare the ramping capacitor voltage with the controlling input voltage $V_{IN}(n)$.

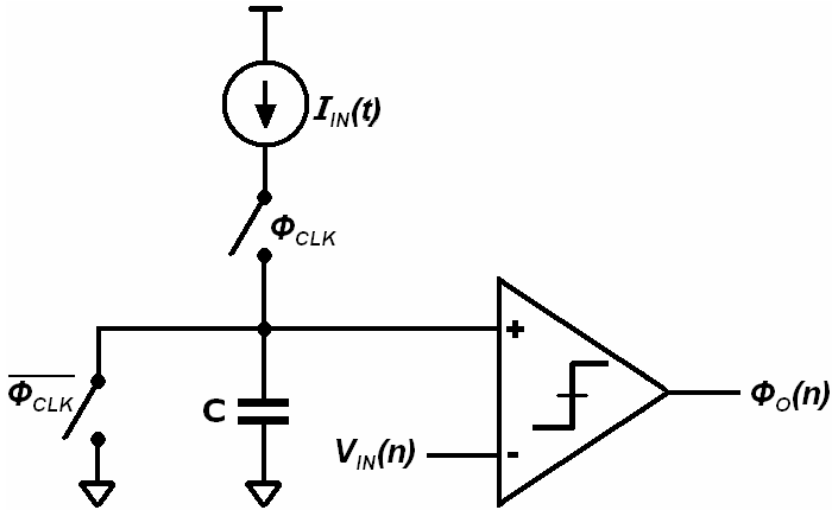
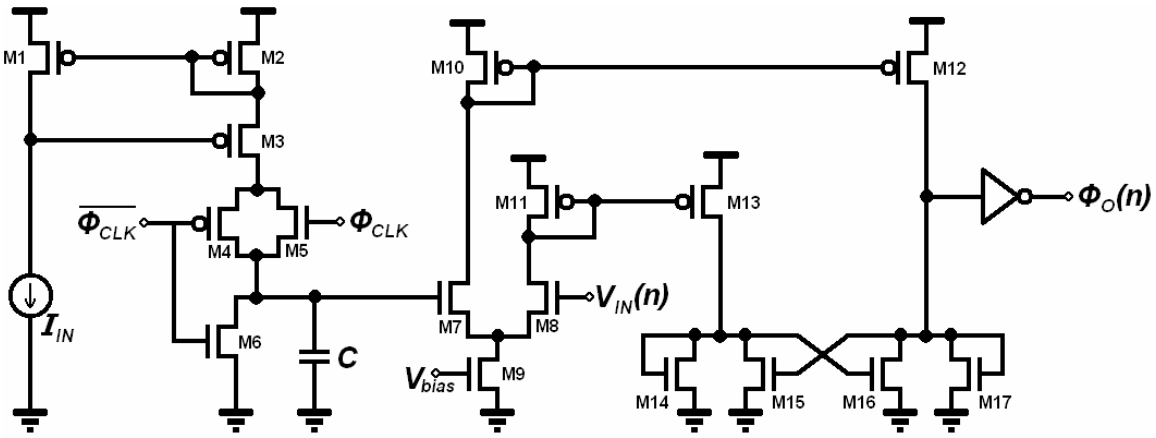
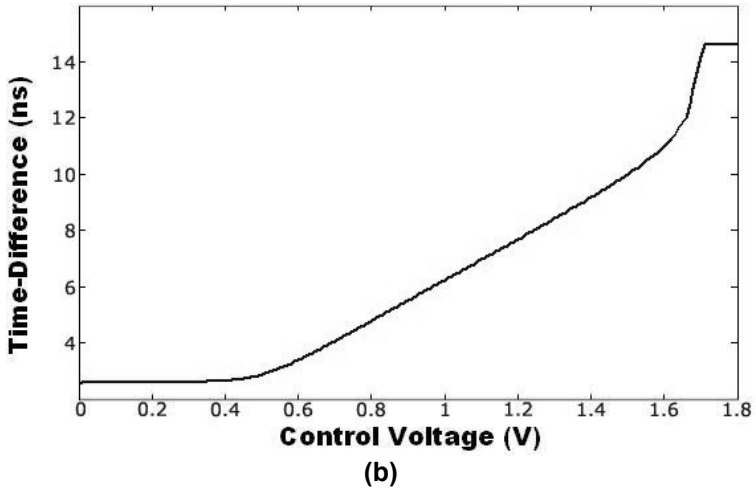


Figure 3.4: Voltage-controlled delay unit (VCDU) functional diagram.

An example CMOS transistor level schematic of a VCDU using the voltage control strategy is depicted in Figure 3.5(a). Transistor dimensions for all circuits are revealed in Appendix A. A Wilson current mirror, formed by transistors M1-M3, is used to generate the constant current reference I_{IN}. During the logic low phase of the clock ϕ_{CLK} the capacitor C is reset via transistor M6. Charging of the capacitor begins on the rising edge of the clock through the transmission gate switch formed by transistors M4 and M5. The current-steering amplifier, constructed by transistors M7-M13, senses the difference between the input voltage $V_{IN}(n)$ and the capacitor voltage permitting the output latching circuit



(a)



(b)

Figure 3.5: Direct voltage-controlled VCDU (a) transistor schematic; (b) transfer characteristic obtained through an HSPICE simulation.

(M14-M17) to make a logic decision.

The transfer characteristic for the circuit in Figure 3.5(a) was obtained through an HSPICE simulation and is presented in Figure 3.5(b). Note that all circuit simulations performed in this thesis were conducted with HSPICE using BSIM3 models for a standard 0.18-µm CMOS process proprietary to the Taiwan Semiconductor Manufacturing Corporation (TSMC). The data was collected by sweeping the input voltage across the entire 1.8-V input voltage range while calculating the time-difference between the output transition and input clock edge. The voltage-to-time conversion factor G_ϕ may be obtained by calculating the slope of the linear region of the transfer characteristic or by dividing the capacitor value C by the reference current I_{IN}. In either case G_ϕ was determined to be 7.2 ns/V. The linear operating region is within the voltage range of 0.6 V and 1.4 V with less than a ±0.1% linearity error. The maximum conversion time is approximately 10 ns limiting the operating frequency to below 100 MHz. According the simulation data, this circuit dissipates a power of 3.3 mW.

8.1.1.1 Current-Controlled VCDU Strategy

The second method to convert voltage signals into time-mode variables is by controlling the current source in Figure 3.4. In this case a voltage-controlled current source would be implemented while the comparator input voltage V_{IN} would be fixed. A common implementation for this classification of VCDU is often referred to as a current-starved inverter and is quite popular in the design of voltage-controlled oscillators [21] – [27]. These designs are very simplistic whereby the comparator is implemented by an inverter with its built-in threshold reference voltage.

A CMOS transistor schematic of a current-starved inverter VCDU is shown in Figure 3.6(a). When the input clock signal ϕ_{CLK} is low, the capacitor C is set to the supply voltage forcing the output $\phi_O(n)$ to reset. On the rising edge of the

clock the capacitor *C* begins to discharge through the NMOS transistors M3 and M4 at a rate that is governed by the input voltage $V_{IN}(n)$. The output inverter (M5 and M6) acts as the comparator and senses when the capacitor voltage has surpassed the inverter threshold voltage.

Although Equation (3.2) dictates that time and current are nonlinearly related, the current-starved inverter technique has a linear region in its transfer characteristic, as demonstrated by an HSPICE simulation and shown in Figure 3.6(b). The linear region for this device is between 0.8 V and 1.2 V, with a maximum linearity error of ±0.15%. The voltage-to-time conversion factor G_ϕ was determined to be

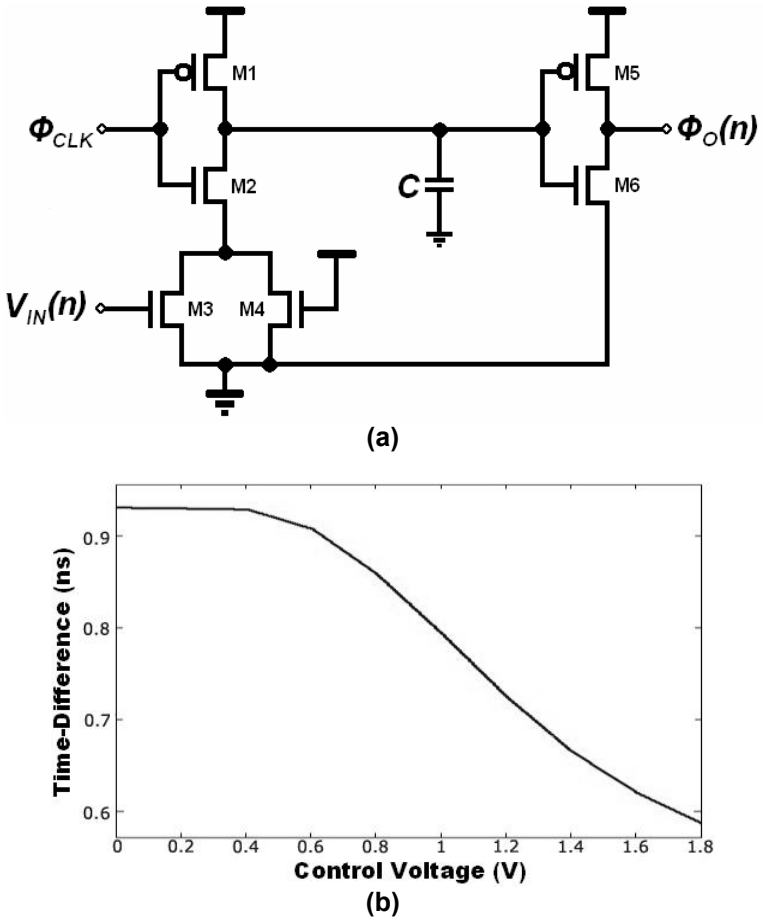


Figure 3.6: Current-starved inverter VCDU (a) transistor schematic; (b) transfer characteristic obtained through an HSPICE simulation.

-320 ps/V. The average power consumption was extracted as 136 μW. A maximum conversion time of 850 ps is observed resulting in a maximum operating frequency of 1.1 GHz. Appendix A provides the transistor dimensions for this design.

Control of the voltage-to-time gain factor, conversion time, and power is set by the capacitor value C and the size of the voltage-controlled NMOS transistor M3.

8.1.1.2 Comparison between Direct Voltage-Control and Current-Starved VCDUs

Like any other electronics component, the selection of a VCDU architecture will depend on its intended application. Table 3.1 summarizes the performance of both the direct-voltage control and current-starved inverter VCDUs. The direct voltage-control methodology offers the advantages of a higher voltage-to-time conversion factor G_ϕ and better linearity with a larger input voltage range. G_ϕ is an important parameter for the TMSP circuits that will follow the voltage-to-time

Table 3.1: Performance comparisons between the direct-voltage control and current-starved inverter VCDUs.

Metric	Direct Voltage-Control	Current-Starved Inverter
Voltage-to-Time Conversion Factor G_ϕ	**7.2 ns/V**	-320 ps/V
Linear Input Voltage Range	**0.6 V → 1.4 V**	0.8 V → 1.2 V
Linearity Error	**±0.1%**	±0.15%
Maximum Sampling Frequency	100 MHz	**1.1 GHz**
Power Consumption	3.3 mW	**136 μW**
Area[†]	480 μm^2	**14.5 μm^2**

[†] Circuit area is estimated by summing all transistor gate areas and capacitor area in the design. Capacitor area is calculated using metal-insulator-metal (MIM) capacitor dimensions.

converter as they must be able to detect and manipulate small time differences. The current-starved inverter approach boasts significantly better power consumption, silicon area usage, and a much higher operating bandwidth.

Sample-and-Hold Action

Sample-and-hold circuits are required in A/D conversion when the input voltage is a relatively high-frequency signal with respect to the ADC conversion process. Hence, a VCDU may act as a sampler provided its conversion time is sufficiently greater than the input frequency. We can determine when a sample-and-hold circuit may be omitted by observing a sinusoidal input voltage signal, as shown in Figure 3.7. The input sinusoidal voltage function may be expressed as

$$V_{IN}(t) = A\sin(2\pi f_{IN} t), \tag{3.4}$$

where A is the peak amplitude and f_{IN} is the signal frequency. The maximum slope is calculated at the zero crossing and is given by

$$\left.\frac{dV_{IN}}{dt}\right|_{\max} = 2\pi A f_{IN}. \tag{3.5}$$

Let T_C represent the maximum conversion time of the VCDU. That is, T_C is the

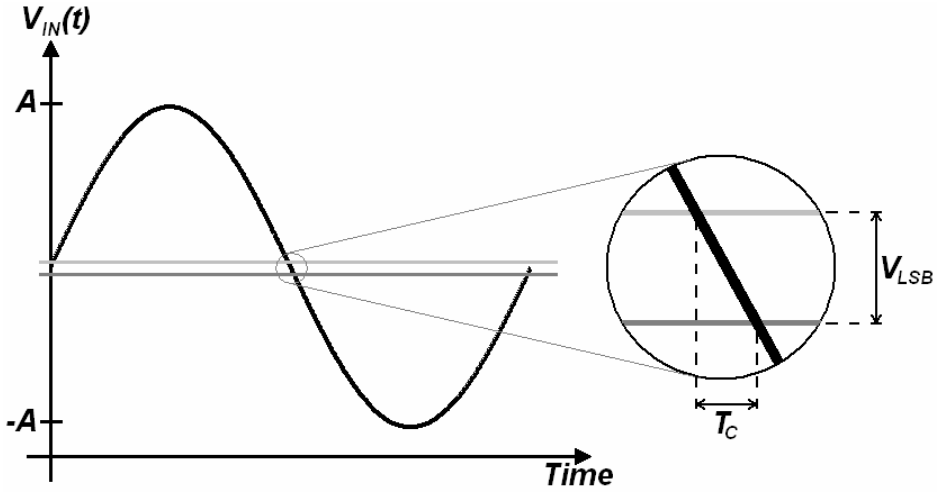


Figure 3.7: Analysis of sinusoidal input voltage to determine when a sample-and-hold is required.

largest time difference between the input and output digital edges for any input voltage. In order to avoid errors in the sampling, the input voltage cannot change more than one LSB step V_{LSB} within the conversion time T_C, as shown in the magnification in Figure 3.7. This imposes an upper limit on the maximum voltage change (i.e. maximum slope), such that

$$\frac{dV_{IN}}{dt} = 2\pi A f_{IN} \leq \frac{V_{LSB}}{T_C}. \tag{3.6}$$

The LSB voltage step that a converter is designed to detect may be expressed as

$$V_{LSB} = \frac{2A}{2^D - 1}, \tag{3.7}$$

where D is the number of bits the converter should resolve. Combining and rearranging Equations (3.6) and (3.7) results in the expression

$$f_{IN} \leq \frac{1}{\pi\left(2^D - 1\right)T_C}. \tag{3.8}$$

This inequality dictates whether or not a sample-and-hold circuit is required based on the desired resolution D, the maximum VCDU conversion time T_C, and input signal bandwidth f_{IN}.

Distortion may also result from using the VCDU as a sampler. The distortion occurs from the fact that the VCDU's conversion time is dependant on the input voltage amplitude. A formula describing this behaviour may be developed as follows. Let the input voltage $V_{IN}(t)$ be described by Equation (3.4). When sampled by a clock with period T_S the input voltage becomes

$$V_{IN}(n) = A\sin\left(2\pi f_{IN} n T_S\right). \tag{3.9}$$

The true sampling time is offset by the VCDU's voltage-dependent conversion time T_C given by the equation

$$T_C = G_\phi V_{IN}(n) + T_0\,, \tag{3.10}$$

where T_0 is the VCDU's conversion time with the input voltage set to analog ground. Therefore, the true sampled input voltage is given by

$$V_{IN}(n) = A\sin\left(2\pi f_{IN}\left(nT_S + G_\phi V_{IN}(n) + T_0\right)\right). \tag{3.11}$$

Applying the trigonometric identity $\sin(A+B) = \sin(A)\cos(B)+\cos(A)\sin(B)$, Equation (3.11) becomes

$$\begin{aligned} V_{IN}(n) = {} & A\sin\left(2\pi f_{IN}\left(nT_S + T_0\right)\right)\cos\left(2\pi f_{IN} G_\phi V_{IN}(n)\right) \\ & + A\cos\left(2\pi f_{IN}\left(nT_S + T_0\right)\right)\sin\left(2\pi f_{IN} G_\phi V_{IN}(n)\right) \end{aligned} \tag{3.12}$$

Although it is not immediately obvious, Equation (3.12) represents a harmonically distorted version of Equation (3.9). To obtain a manageable expression, it will be assumed that the VCDU's voltage-to-time gain factor G_ϕ is sufficiently small. Therefore, the series expansion of the sine and cosine terms involving G_ϕ may be truncated (i.e. *cos(x) = 1* and *sin(x) = x* when *x* is small). Consequently, Equation 3.12 will be reduced to

$$V_{IN}(n) = A\sin\left(2\pi f_{IN} nT_S\right) + A2\pi f_{IN} G_\phi V_{IN}(n)\cos\left(2\pi f_{IN} nT_S\right). \tag{3.13}$$

Note that this approximation has removed all but the second harmonic distortion component. Substituting Equation (3.9) into the right-hand side of (3.13) results in

$$\begin{aligned} V_{IN}(n) = {} & A\sin\left(2\pi f_{IN} nT_S\right) + \\ & A^2 2\pi f_{IN} G_\phi \sin\left(2\pi f_{IN} nT_S\right)\cos\left(2\pi f_{IN} nT_S\right). \end{aligned} \tag{3.14}$$

Using the trigonometric identity $2\sin(A)\cos(A) = \sin(2A)$ converts Equation (3.14) into

$$V_{IN}(n) = A\sin\left(2\pi f_{IN} nT_S\right) + A^2\pi f_{IN} G_\phi \sin\left(4\pi f_{IN} nT_S\right). \tag{3.15}$$

Equation (3.15) reveals that the input voltage consists of the original signal and a second harmonic component which has an amplitude of $A^2\pi f_{IN} G_\phi$. Therefore, the harmonic distortion is proportional to the input signal frequency and amplitude,

and the VCDU's voltage-to-time conversion factor. An estimation of the total harmonic distortion may be obtained using the expression

$$THD = 20\log\left(\frac{1}{A\pi f_{IN} G_{\phi}}\right). \tag{3.16}$$

It must be restated that Equation (3.15) is an approximation offering only the second harmonic. All other harmonics do exist and may be obtained by substituting the complete series expansions for the sine and cosine terms into Equation (3.12).

The VCDU circuits previously described were assumed to be exercised by a sampled analog input voltage $V_{IN}(n)$. There are circumstances, governed by Equations (3.8) and (3.16), where the VCDU itself may act as the sampler. For example, suppose that a 10-bit resolution is required. The previously described current-starved inverter VCDU design had a maximum conversion time of 0.9 ns. Therefore, according to Equation (3.8), if the signal bandwidth is smaller than 342 kHz, then the current-starved inverter will act as a sampler. Similarly, the maximum bandwidth for the direct voltage-control VCDU with a maximum conversion time of 10 ns is 31 KHz. Alternatively, a 10-bit resolution implies a THD requirement of 62 dB. If the current-starved VCDU has a voltage-to-time conversion factor of 320 ps/V and a maximum amplitude of 0.2 V then Equation (3.16) dictates that the maximum bandwidth of approximately 4 MHz. According to Equation (3.16) the voltage-control VCDU, with G_{ϕ} = 7.2 ns/V, would be restricted to 175 kHz. These numerical examples serve to illustrate that the measure in Equation (3.8) is far more conservative than the expression in Equation (3.16). Another advantage may be inferred from these examples. That is, the current-starved VCDU approach will act as a sampler for a larger input signal bandwidth than the direct-voltage control method.

3.1.2. Voltage-to-Time Converter

A voltage-to-time converter (VTC) is required to transform voltage information into time-mode signals. In all signal processing circuitry voltage signals are measured with respect to an analog ground voltage reference V_{REF}. Moreover, in single-voltage power supply technologies the analog ground is usually a voltage greater than zero. In order to convert voltage data into time-difference variables we employ two VCDUs, as shown in Figure 3.8(a). The top VCDU converts the input voltage $V_{IN}(n)$ into a time-difference variable which is measured with respect to the analog ground time reference ΔT_{REF} generated by the bottom VCDU.

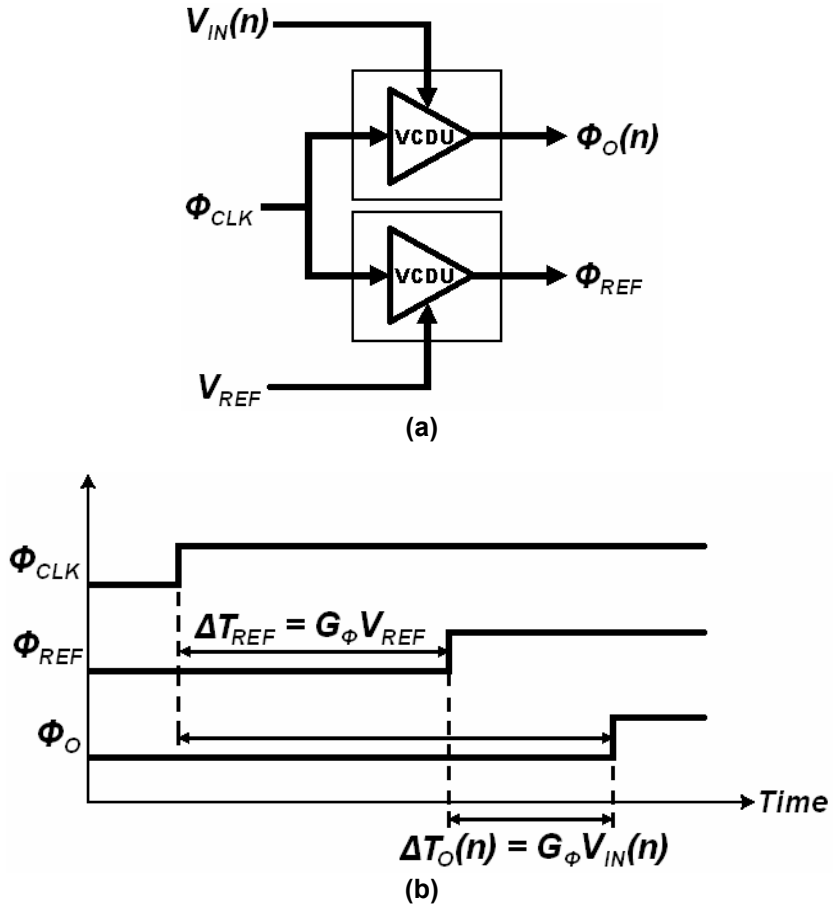


Figure 3.8: Voltage-to-time converter (VTC) (a) block diagram; (b) timing diagram illustrating the VTC operation.

The VTC operation is illustrated in the timing diagram of Figure 3.8(b) whereby the input clock event ϕ_{CLK} is delayed with respect to the input controlling voltages $V_{IN}(n)$ and V_{REF}, resulting in the respective VCDU outputs $\Delta T_O(n)$ and ΔT_{REF}. The output of the VTC, $\Delta T_O(n)$, is interpreted as the time difference measured with respect to the reference time ΔT_{REF}. The output time-difference variable may also be expressed in terms of the input voltage as

$$\Delta T_O(n) = G_\phi V_{IN}(n). \tag{3.17}$$

Similar to the conventional representation of voltage signals, the analog ground reference time is omitted or assumed to be zero in Equation (3.17).

Mismatch between VCDUs in a VTC will cause offset delay errors which manifest themselves as input-referred voltage offsets provided that the signals remain in the linear operating region of the VCDUs.

3.2 - Time-Mode and Mixed-Mode Signal Processing

Time signal processing circuits operate in two categories: either they manipulate time-difference variables directly, or they process time and voltage signals together. The latter circuits, referred to as mixed-mode circuits, comprise of adders and integrators. Direct time-mode signal processing blocks are time-amplifiers and delay circuits. Each of these components is described in the following subsections.

3.2.1. Voltage-to-Time Adder

Voltage-to-time conversion was demonstrated in the previous section where it was assumed that the VCDUs were exercised using an arbitrary clock signal. Figure 3.9 presents a voltage-to-time adder and timing diagram to demonstrate its operation. The process of adding time with voltage may be realized if it is assumed that the input clock $\phi_{IN}(n)$ to be delayed by $V_{IN}(n)$ has an initial time delay of $\Delta T_{IN}(n)$. The VTC output thus becomes

$$\Delta T_O(n) = \Delta T_{IN}(n) + G_\phi V_{IN}(n). \tag{3.18}$$

Again, by convention, the analog ground reference time is omitted from Equation (3.18).

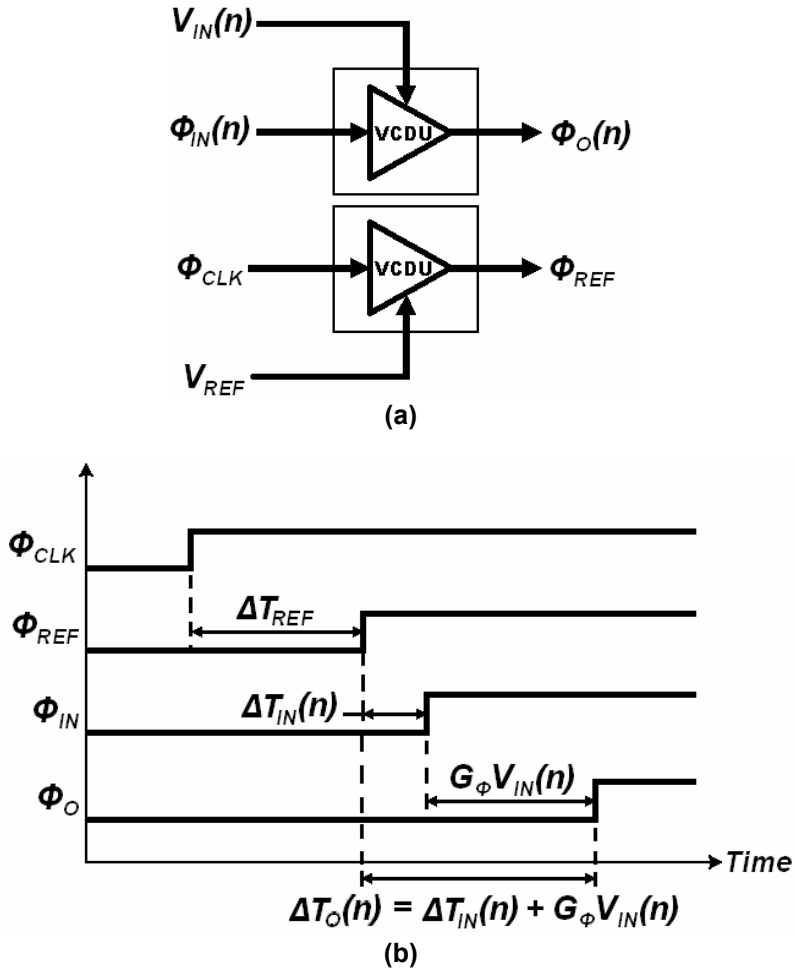


Figure 3.9: Voltage-to-time adder (a) block diagram; (b) timing diagram.

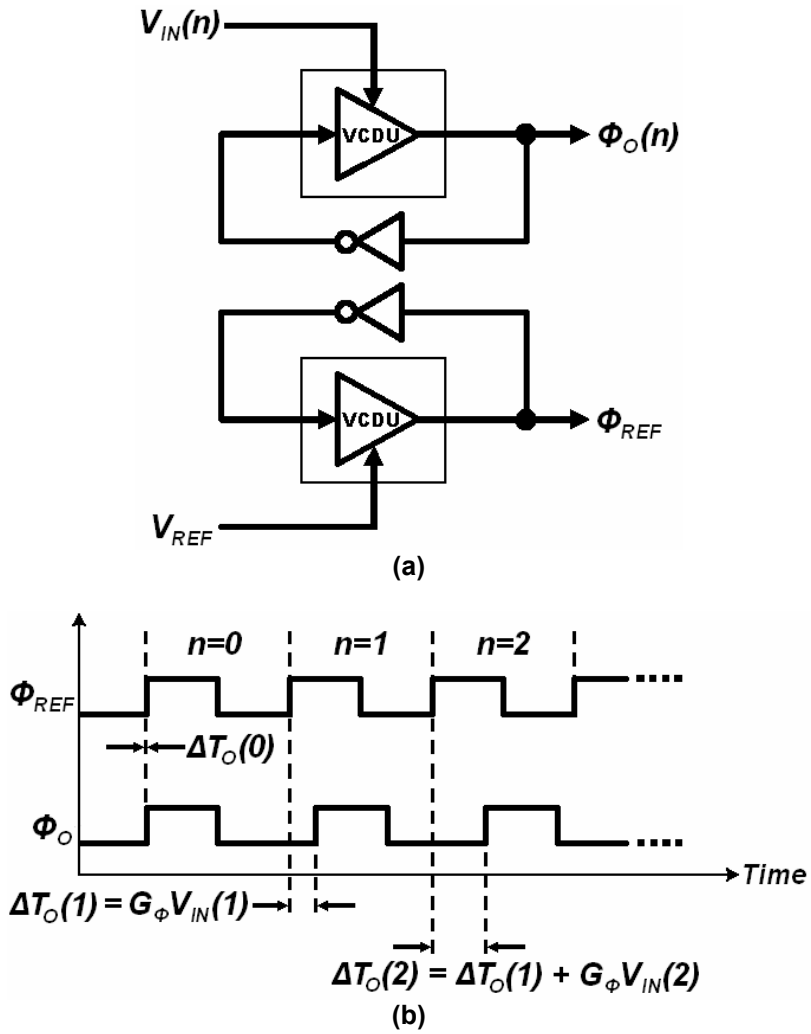


Figure 3.10: Voltage-to-time integrator (a) block diagram; (b) timing diagram.

3.2.2. Voltage-to-Time Integrator

Voltage-to-time integration may be implemented using a similar circuit to the voltage-to-time adder whereby the output is connected to the input through an inverter. This circuit is equivalent to a voltage-controlled ring oscillator and is depicted in Figure 3.10(a). Three samples demonstrating the operation of the voltage-to-time integrator is presented in Figure 3.10(b). The initial integrator output $\Delta T_O(0)$ is set to zero. The next output time-difference $\Delta T_O(1)$ is proportional to the input voltage at instance $n=1$. The proceeding output $\Delta T_O(2)$ is the sum of the previous output $\Delta T_O(1)$ and the input voltage $V_{IN}(2)$ scaled by G_ϕ.

Hence, the difference equation of the voltage-to-time integrator with respect to the reference time ΔT_{REF} is given by

$$\Delta T_O(n) = \Delta T_O(n-1) + G_\phi V_{IN}(n-1). \tag{3.19}$$

Note that there is no external clock signal in this design. In other words it is free-running or self-clocking. Control of the oscillation frequency is done by circuit design and the input voltages.

A dual-input or multi-input integrator may be created by including two or more VCDUs in the oscillating loops. Figure 3.11 illustrates a dual-input integrator with controlling voltages $V_{IN1}(t)$ and $V_{IN2}(t)$. A second oscillator, controlled by reference voltage V_{REF}, is included to generate the reference time.

A very important VCDU design constraint must be adhered to when they are used in voltage-to-time integrators. When a rising edge passes through a VCDU,

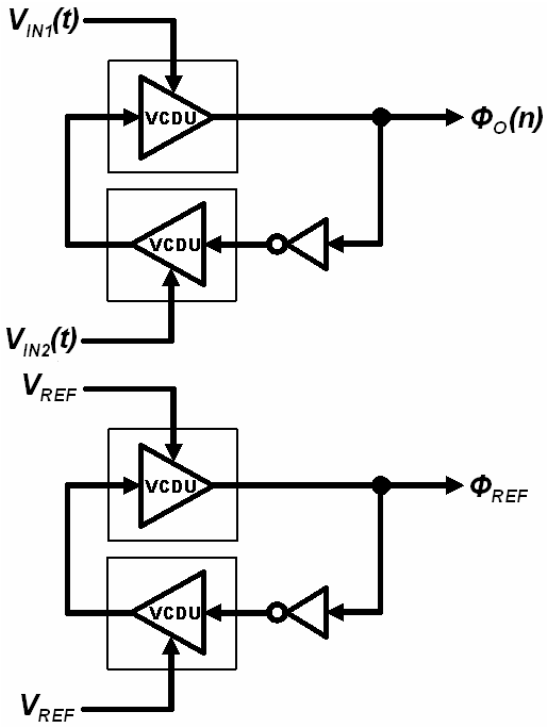


Figure 3.11: Block diagram of a dual-input voltage-to-time integrator.

it will sample the input controlling voltage and delay the rising edge proportionally. However, one of two things must occur when the falling edge is passing through the VCDU. Either the falling edge must be unaffected by the controlling voltage, or the falling edge must be delayed with respect to the controlling voltage. Offsets or distortion may result if either of these methods is unsuccessfully implemented. If the latter design method is used then the rising and falling edges must be delayed with the same voltage-to-time conversion factor. For this reason it is easier to design the VCDU such that the falling edge is unaffected by the controlling voltage. Regardless of the VCDU circuit topology this may be implemented with an AND gate. Figure 3.12 demonstrate the current-starved inverter VCDU with an AND gate used to ensure that the input falling edge of ϕ_{CLK} circumvents the VCDU.

It would be very desirable to cascade two integrators, however, this cannot be done with ease. Because time is not a physical quantity the summation of two time-difference variables cannot be done without first transforming them into an intermediate medium such as charge [5], thus forfeiting the advantages of TMSP.

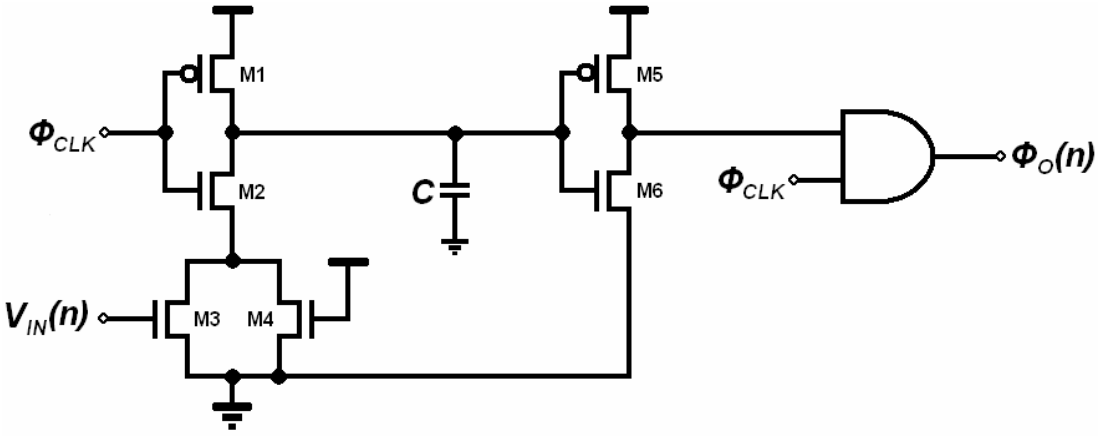


Figure 3.12: Current-starved inverter VCDU with an output AND gate to bypass the clock's falling edge.

3.2.3. Time Amplifier

Time amplification is the process of multiplying a time-difference variable by a scalar. A time amplifier (TAMP), depicted in Figure 3.13(a), has two inputs and two outputs. The time amplification process is exemplified in the timing diagram of Figure 3.13(b). The inputs are digital edges that represent a time-difference variable. The output ΔT_{OUT} is a time-difference variable that scales its input time-difference by the TAMP gain G_{TA} such that

$$\Delta T_O = T_{OUT2} - T_{OUT1} = G_{TA}\left(T_{IN2} - T_{IN1}\right). \tag{3.20}$$

Two such designs have been reported to date. The first design, described in [28], implements the time amplifier with two SR latches, two voltage arbiters, and two OR gates. Although the linearity of this device is good, its accuracy and repeatability are difficult to maintain as process variation cannot be controlled or calibrated in this design. Furthermore, the input time-difference is limited to a small range.

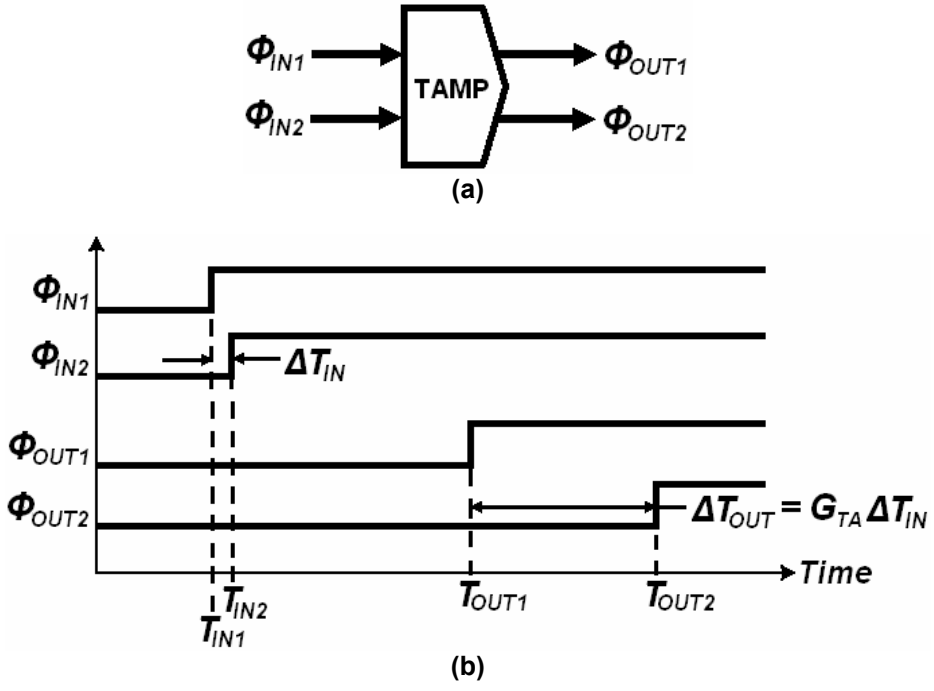


Figure 3.13: Time amplifier (TAMP (a) block diagram; (b) example timing diagram.

The CMOS transistor schematic of the TAMP reported in [29] is shown in Figure 3.14(a). It consists of two cross-coupled differential amplifiers with capacitive and resistive loads. The transfer characteristic of this device is given in Figure 3.14(b). It may be seen that for small input time differences ΔT_{IN} the output time difference ΔT_{OUT} is linearly related with a gain G_{TA} given by the slope of the curve.

This design can achieve gains exceeding several-hundred seconds-per-second and time-difference inputs can extend well into the nanosecond range. The gain

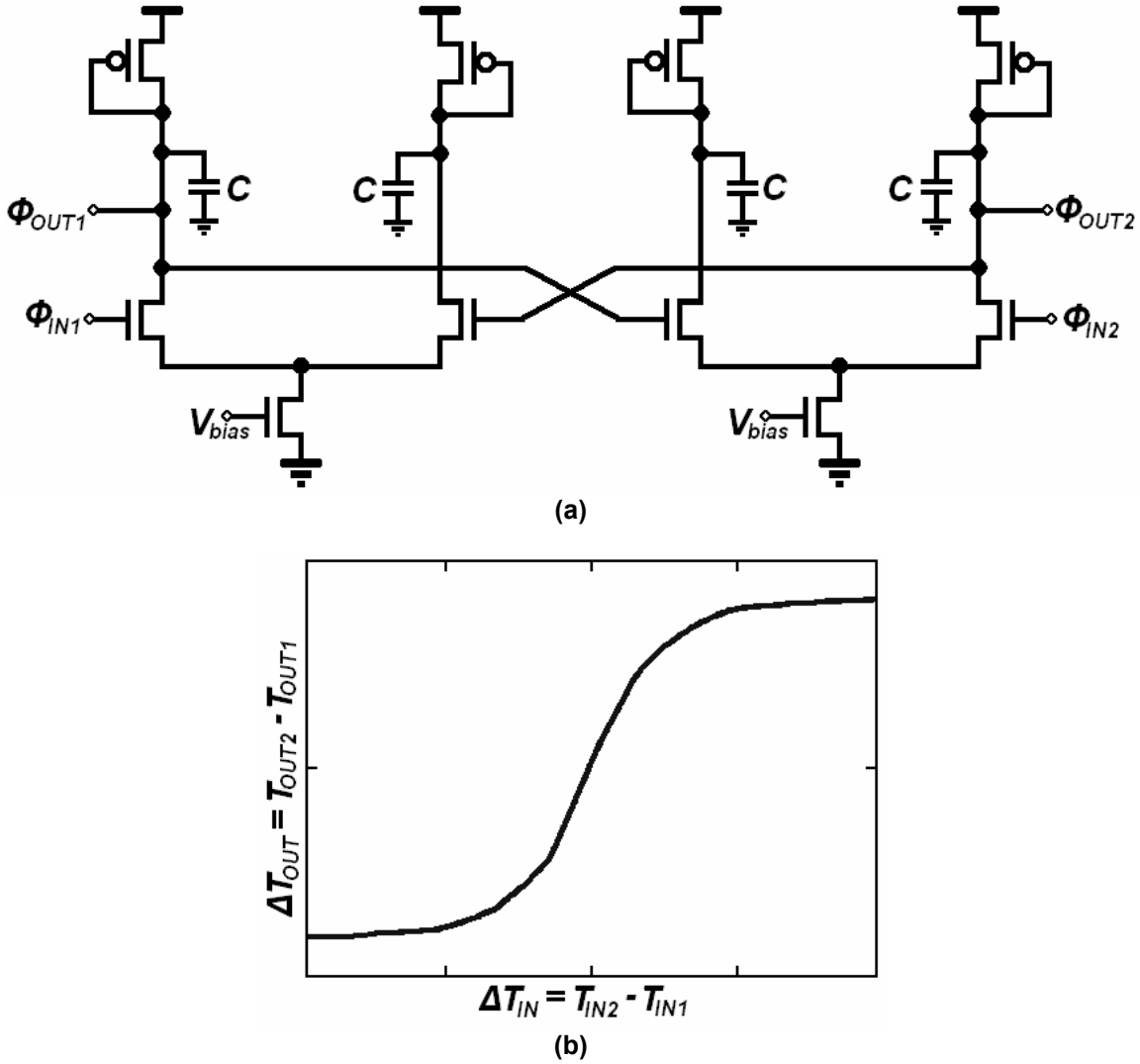


Figure 3.14: Time amplifier (a) transistor schematic; (b) transfer characteristic.

and input linear range is controlled by the biasing current, and the capacitive and resistive loading. The common tradeoff of gain versus linearity and gain versus speed remain a consistent challenge within TAMP design.

3.2.4. Delay Elements

There are some situations where time-difference information needs to be held or delayed. Under these circumstances digital delay elements or simple inverters may be used. Of course both the signal clock and reference clock need to be delayed by the exact same propagation time, hence matching inverters is very important.

3.3 - Time-to-Digital Conversion

The final step in the time-mode analog-to-digital process is to convert the time-difference variable into its digital representation. This may be accomplished with time comparators and time-to-digital converters, as described in following subsections.

3.3.1. Time Comparator

Comparisons of two clock events may be performed by a D-type edge-triggered flip-flop, as demonstrated in Figure 3.15(a). The input digital event $\phi_{IN}(n)$ is compared to a reference event signal ϕ_{REF}. If the edge of $\phi_{IN}(n)$ is leading ϕ_{REF} (i.e. $T_{IN}(n) > T_{REF}$), then the output $D_{OUT}(n)$ results in a logic 1. Otherwise the output results in logic 0.

Similar to a voltage comparator, flip-flop metastability is an issue when attempting to make the correct decision between two input clock events which are close together. A technique to reduce the influence of flip-flop metastability is

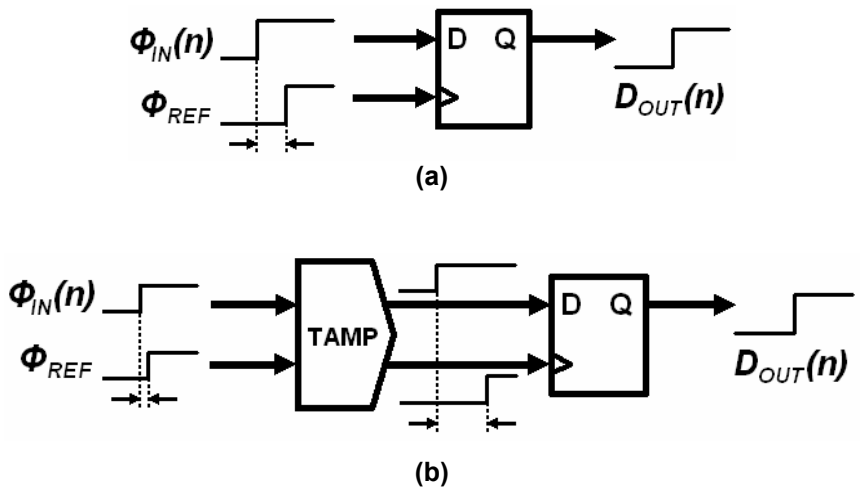


Figure 3.15: Time comparator implemented using a (a) edge-triggered D-type flip-flop (b) edge-triggered D-type flip-flop with a time amplifier (TAMP) used as a pre-amplifier.

to pre-amplify the input time-difference using a time amplifier, as demonstrated in Figure 3.15(b).

3.3.2. Time-to-Digital Converter

A time-to-digital converter (TDC) is responsible for converting a time interval between two clock edges into a digital number. A popular TDC, shown in Figure 3.16, is a flash architecture that uses a Vernier delay line [30]. It is constructed from two delay lines. The top delay line has buffers with delays that are slightly larger than the bottom delay line. Each stage contains a time comparator (i.e. a D-type flip-flop) that determines which edge is leading. The TDC operates by propagating the two input clock edges, $\phi_{IN}(n)$ and ϕ_{REF}, through the unmatched delay lines incrementing them one LSB time interval closer through each stage. The LSB is the delay difference between the fast and slow buffers. The flip-flop outputs represent a thermometer code digital word which is summed together to produce the binary data D_{OUT}. Mismatch between delay buffers and flip-flops will cause this converter to suffer from non-linearity errors. Therefore, careful design and layout techniques should be applied.

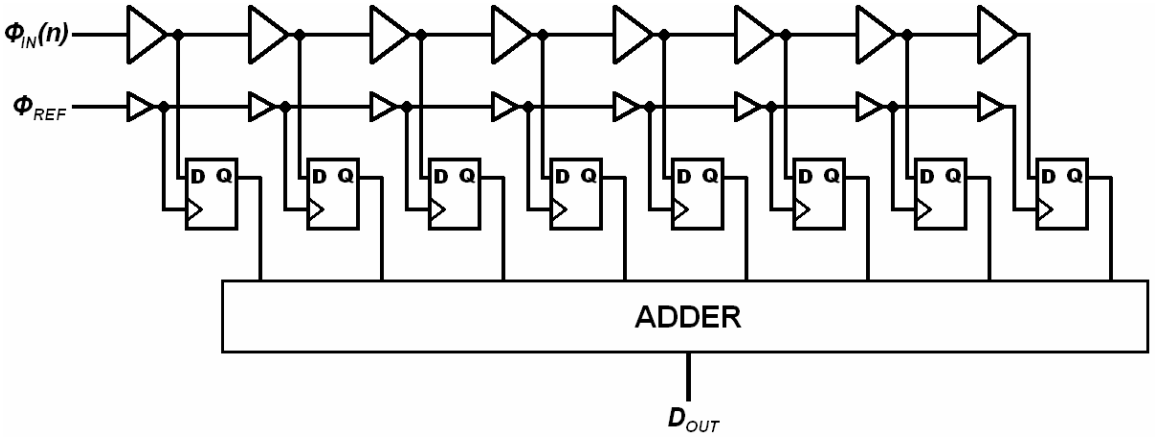


Figure 3.16: 3-bit time-to-digital converter using a Vernier delay line.

There are many other styles of TDC designs such as those described in [31], [32] and [33]. However, the Vernier delay line implementation is by far the simplest and offers adequate time resolution.

3.4 - Time-Mode Signal Processing Advantages and Disadvantages

The time-mode signal processing methodology processes time-difference variables. Time-difference variables are technology independent. In other words, they do not depend on technology constraints such as power supply. Therefore, the dynamic range of time-difference variables has no theoretical limitation. Practically however, increasing the dynamic range of time-difference variables will result in longer processing delays and hence slower circuit operation. Hence, a tradeoff between dynamic range and bandwidth is implied.

The basic building blocks of TMSP circuits are built with a digital CMOS logic style implementation. They offer the benefits of lower power, high speed, and small area. The power consumption will be low as mainly dynamic power is dissipated. These circuits will operate at very high speeds; potentially at

gigahertz clocking rates. Additionally, as technologies scale down the power, speed, and area of these digital circuits will improve.

A final advantage of TMSP circuits is that they can provide the sampling action using the VCDU such that no conventional sample-and-hold is required. However, there are limitations on the input signal bandwidth as described by Equation (3.9). Nevertheless, as technology scales down and the maximum conversion time of the VCDU reduces, this maximum signal bandwidth will increase.

The disadvantage of the TMSP circuits is their tradeoff between input dynamic range and linearity error. The VCDU in the current-starved inverter configuration is linear for a small input voltage range. Any circuit design that increases the voltage range and linearity will compromise its operating speed, power consumption, and increase circuit complexity.

3.5 - Summary

This chapter introduced the concept of time-mode signal processing and the various functional blocks and CMOS circuits that implement this methodology. These designs include circuits to convert and interface voltage signals into time-difference variables, process time-mode signals, and transform time-mode signals into digital words.

Several benefits can be extrapolated from the TMSP methodology. Specifically, time-difference variables are technology independent which means that their dynamic range will not be limited by technology constraints such as power supply voltage rails. Due to their digital implementation, TMSP circuits will consume low power, operate at fast speeds, and occupy small silicon area. Moreover, as

technologies scale down their performance over power, speed, and area will improve.

It will be shown in subsequent chapters that the proposed TMSP strategy and accompanying circuits may be used to implement analog-to-digital converters.

Chapter 4: Time-Mode Voltage Comparator

The basic building block of all conventional analog-to-digital converters is the analog comparator, as was demonstrated in Chapter 2. By itself a comparator is a single-bit ADC. A comparator implemented with time-mode signal processing circuits is presented in this chapter along with a calibration methodology to compensate for process variation resulting in input-referred voltage offsets. The proposed calibrated comparator was implemented in a standard CMOS technology and its experimental results are presented.

4.1 - Time-Mode Voltage Comparator

The proposed comparator without calibration, hereafter referred to as the time-mode voltage comparator (TMVC) is illustrated in Figure 4.1. It operates on the premise that the input analog voltage signal $V_{IN}(n)$ and reference voltage V_{REF} are converted into delayed versions of a digital clock signal ϕ_{CLK}. The delay on each signal is generated through a VTC composed of two VCDUs, as described in Chapter 3, and is proportional to its input control voltage. Thus, $\phi_O(n)$ and ϕ_{REF} are the clock signals delayed through the VCDU controlled by $V_{IN}(n)$ and V_{REF}, respectively. The delayed clock signals are compared using a time comparator; in this case an edge-triggered D-type flip-flop.

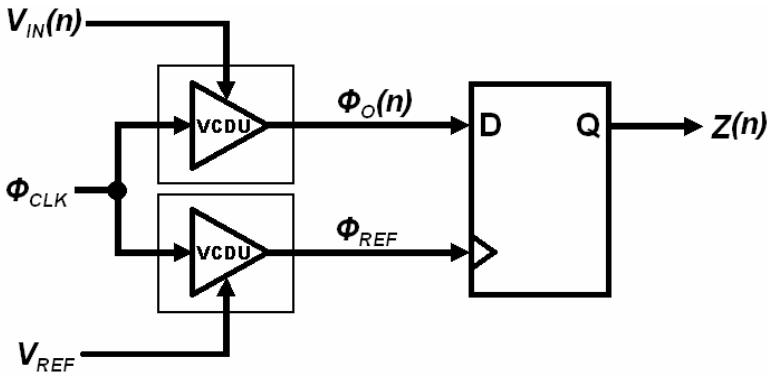


Figure 4.1: Time-mode voltage comparator (TMVC).

The transfer characteristic of the current-starved inverter VCDU described in Chapter 3 is similar to that shown in Figure 4.2(a), where the input control voltage V_C is plotted against the resulting delay time of its input clock. It will be temporarily assumed that both VCDUs are 100% matched (i.e. they both have exactly the same transfer characteristic). For all input voltages within the linear region, the clock delay T may be expressed as a function of control voltage V_C by the equation

$$T = -\left(\frac{dT}{dV_C}\right)V_C + T_0 = G_\phi V_C + T_0\,, \tag{4.1}$$

where T_0 is the VCDU's delay with a control voltage of 0-V, and G_ϕ is defined as the voltage-to-time gain given by $-dT/dV_C$. Hence, the input and reference VDCU delays are $T_{IN} = G_\phi V_{IN} + T_0$ and $T_{REF} = G_\phi V_{REF} + T_0$, respectively. The flip-flop input, ΔT_{IN} is related to the input voltage by

$$\Delta T_{IN} = T_{IN} - T_{REF} = G_\phi\left(V_{IN} - V_{REF}\right). \tag{4.2}$$

The flip-flop transfer characteristic with metastability window ΔT_{MW} is shown in Figure 4.2(b). When ΔT_{IN} is positive and greater than $\Delta T_{MW}/2$ then the flip-flop output is logic 1. When ΔT_{IN} is negative and less than $-\Delta T_{MW}/2$ the flip-flop output is set to logic 0. Otherwise, the flip-flop setup time is violated, and the output may be unpredictable.

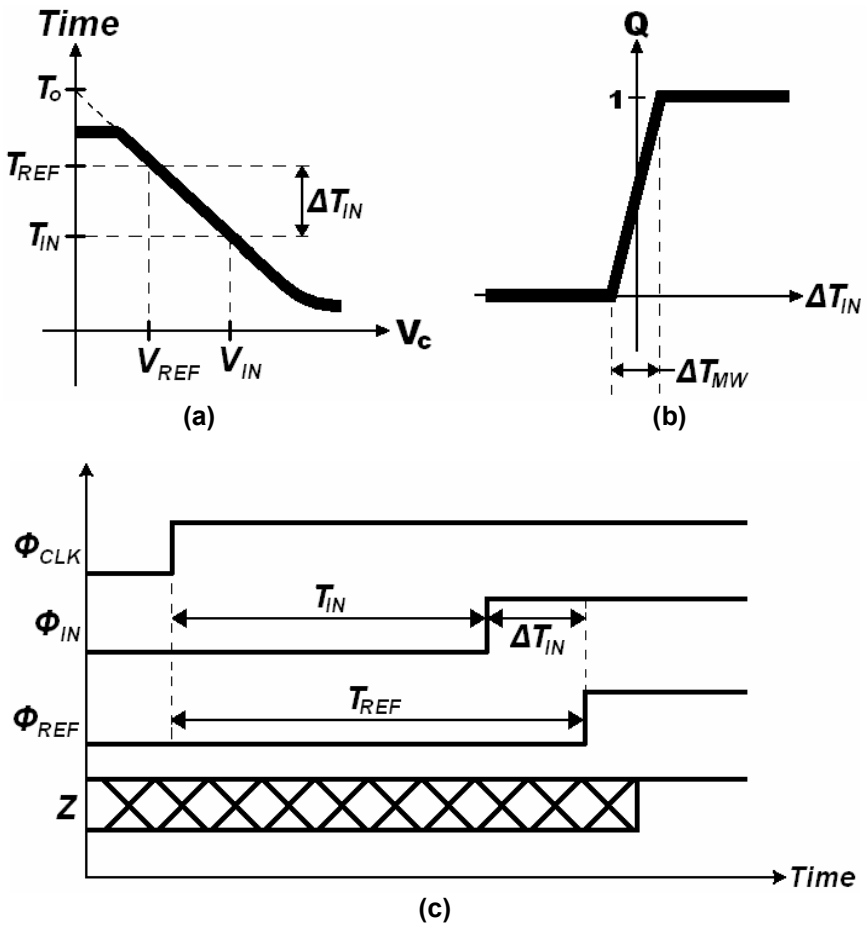


Figure 4.2: Time-mode voltage comparator (TMVC) (a) VCDU transfer characteristic; (b) D flip-flip transfer characteristic; (c) timing diagram.

The timing operation of the TMVC is demonstrated in Figure 4.2(c). Using the transfer characteristics from Figure 4.2(a) and (b) with $V_{REF} < V_{IN}$, the resulting delay of ϕ_{IN} is smaller than that of ϕ_{REF} (i.e. $T_{IN} < T_{REF}$). Assuming that ΔT_{IN} is larger than half the metastable window of the arbiter then the correct comparison will result at the flip-flop output *Z*. In this example, *Z* would be set to logic 1.

In order to ensure that the metastability of the arbiter is overcome, the VCDUs need to be designed with an adequate voltage-to-time gain G_ϕ. The resolution of a comparator is set by its desired minimum input voltage difference ΔV_{min}, given by

$$\Delta V_{\min} = \frac{V_{FS}}{2^D - 1}, \tag{4.3}$$

where V_{FS} is the full scale voltage and D is the number of bits that the comparator must resolve. The minimum delay difference, ΔT_{min}, may be obtained by substituting Equation (4.3) into (4.2), resulting in

$$\Delta T_{\min} = G_\phi\left(\Delta V_{\min}\right) = G_\phi\left(\frac{V_{FS}}{2^D - 1}\right). \tag{4.4}$$

The minimum delay difference should be greater than half the metastable window of the flip-flop in order to ensure that the correct decision is made (i.e. $\Delta T_{min} > \Delta T_{MW}/2$). Substituting Equation (4.4) into this inequality yields the minimum VCDU gain requirement of

$$G_\phi > \frac{\Delta T_{MW}}{2}\frac{\left(2^D - 1\right)}{V_{FS}}. \tag{4.5}$$

For example, suppose the full scale voltage V_{FS} is 1-V, an 8-bit resolution is desired, and a typical flip-flop metastability window is 30 ps. Substituting these design specifications into Equation (4.5) would necessitate a VCDU with a gain of 3.8 ns/V.

4.2 - Time-Mode Comparator with Calibration

It was assumed that the VCDUs in the TMVC have matched transfer characteristics. Realistically, the characteristics of two VCDUs will differ due to process variation. Figure 4.3(a) presents a typical transfer characteristic of two mismatched VCDUs. The top curve represents the characteristic of the VCDU controlled by V_{IN} and the bottom curve represents the characteristic of the VDCU controlled by V_{REF}. Following the same derivation for Equation (4.1), the input and reference delays would become

$$T_{IN} = G_{\phi_{IN}} V_{IN} + T_{0_{IN}} \tag{4.6}$$

and

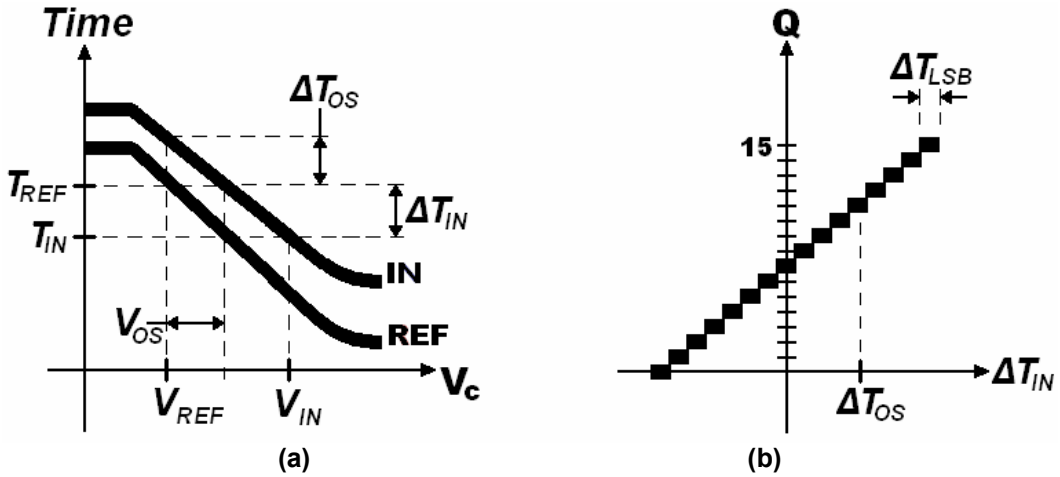


Figure 4.3: Transfer characteristics for the time-mode voltage comparator (TMVC) with calibration: (a) two mismatched VCDUs; (b) time-to-digital converter.

$$T_{REF} = G_{\phi_{REF}} V_{REF} + T_{0_{REF}} , \tag{4.7}$$

where $G_{\phi IN}$ and $G_{\phi REF}$ are the gains, and T_{0IN} and T_{0REF} are the delays with 0-V control voltage of the input and reference VCDUs, respectively.

At a given reference voltage V_{REF} there is an input-referred offset V_{OS} whereby the timing difference between the two VCDU paths will error if the input voltage V_{IN} is greater than V_{REF} but less than $V_{REF}+V_{OS}$. The input-referred offset voltage may be calculated by equating (4.6) and (4.7), resulting in

$$V_{OS} = \left(\frac{G_{\phi_{REF}}}{G_{\phi_{IN}}} - 1 \right) V_{REF} + \frac{T_{0_{REF}} - T_{0_{IN}}}{G_{\phi_{IN}}} . \tag{4.8}$$

The accuracy and reliability of the TMVC will be limited as a result of process variation. Furthermore, the VCDU offset voltage V_{OS} is dependent on the value of the reference voltage V_{REF}. The delay offset (i.e. VCDU output-referred offset) may also be calculated by setting $V_{IN} = V_{REF}$, and subtracting Equation (4.7) from (4.6) yielding

$$\Delta T_{OS} = \left(G_{\phi_{IN}} - G_{\phi_{REF}} \right) V_{REF} + T_{0_{IN}} - T_{0_{REF}} . \tag{4.9}$$

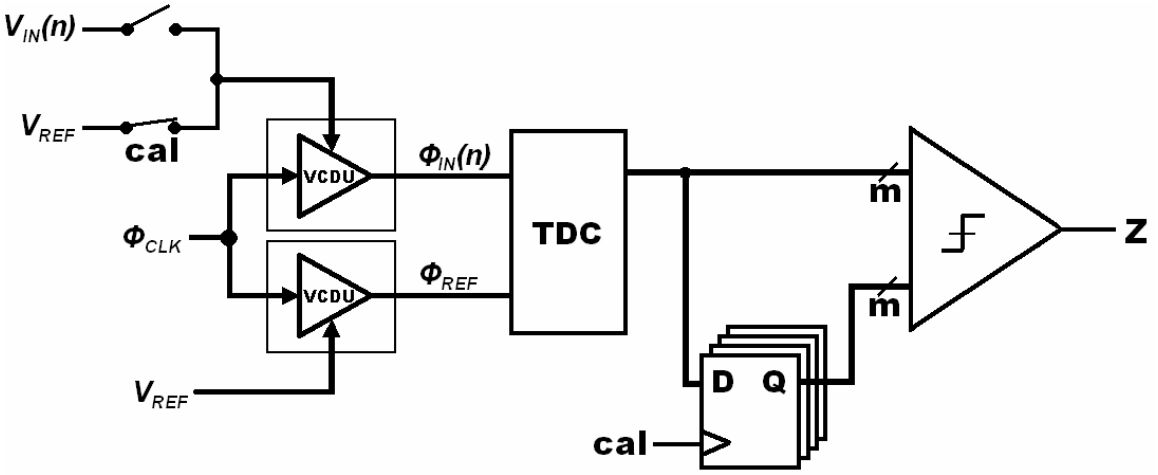


Figure 4.4: Time-mode voltage comparator (TMVC) with calibration.

To compensate for these offsets an all-digital calibration technique as developed and is illustrated in Figure 4.4. Two VCDUs are used to modulate a common clock signal with respect to the input voltage V_{IN} and reference voltage V_{REF}. The design operates in two phases: a calibration phase and normal operation phase. During the calibration phase, V_{REF} is controlling both VCDUs, either from an external source or via an analog multiplexer. The clock is pulsed, and the delay offset ΔT_{OS} from the mismatch VCDUs is captured with an *m*-bit time-to-digital converter (TDC). The *m*-bit digitization of ΔT_{OS}, called the *calibration data*, is stored in a register. Coincidently, the mismatch within the TDC will also be compensated by this calibration mechanism. During normal operation, the top VCDU is controlled by V_{IN} while the bottom VCDU is controlled by V_{REF}. After the rising clock edge ϕ_{CLK}, the resulting delay difference between ϕ_{IN} and ϕ_{REF} (i.e. T_{IN}–T_{REF}) is digitized by the TDC. The TDC digital output is compared to the calibration data using a digital comparator. If the TDC output is larger than the calibration data (i.e. $T_{IN} > T_{REF} + \Delta T_{OS}$) then the output *Z* will result in a logic 1. Otherwise, a logic 0 results at the output *Z* when the TDC output is smaller than the calibration data (i.e. $T_{IN} < T_{REF} + \Delta T_{OS}$).

Figure 4.3(b) illustrates the transfer characteristic of a 4-bit TDC with digital output Q and resolution ΔT_{LSB}. Similar to the derivation of Equation (4.5), the minimum gain requirement of the VCDUs for a given TDCs resolution D is

$$G_\phi > \Delta T_{LSB} \frac{\left(2^D - 1\right)}{V_{FS}}. \tag{4.10}$$

4.3 - Integrated Circuit Implementation

The time-mode voltage comparator with calibration, given in Figure 4.4, was implemented in a standard 0.18-µm CMOS technology. It is composed of five main components: the voltage-to-time converter (VTC), time-to-digital converter (TDC), analog multiplexer (i.e. switches), calibration data memory, and digital comparator.

The VTC used in this implementation is composed of the current-starved VCDUs described in Chapter 3. The VCDUs were designed to have a nominal voltage-to-time gain G_ϕ of 5 ns/V. The transistor dimensions for the VCDUs used in this design are given in Appendix A.

Monte Carlo HSPICE simulations were conducted while varying each transistors threshold voltage, oxide thickness, gate geometries, and all junction capacitances by 10% at 6σ. It was determined that the delay mismatch between two VCDUs varied within ±150 ps. Therefore, a TDC was designed with an input dynamic range of 300 ps. The TDC was implemented with a 15-stage Vernier delay line (VDL) architecture, as described in Section 3.3.2. Using Equation (4.10) it was determined that the TDC should have a resolution of 20 ps. A 4-bit output was generated by summing the 15-bit VDL output using the Wallace tree adder [34].

To demonstrate the calibration operation, Figure 4.5 presents an example of the

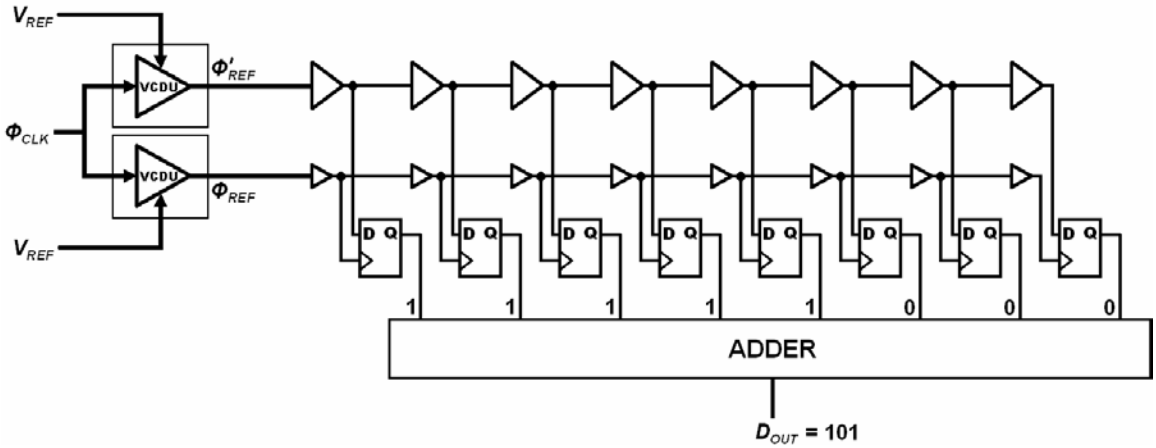


Figure 4.5: Illustration of the calibration mechanism for the time-mode voltage comparator (TMVC) incorporating the voltage-to-time converter (VTC) and the time-to-digital converter (TDC).

VCDUs and a 3-bit VDL combined during a calibration phase. In this example, the input is set equal to the reference voltage and the clock is pulsed. The time offset ΔT_{OS} is captured by the VDL revealing the thermometer code 11111000, resulting in a calibration data output of 5 or 101 in binary. Due to process variation, different calibration data should be obtained from one design to the next.

The calibration data memory was implemented with four edge-triggered D-type flip-flops. The digital comparator was generated using a hardware description language (HDL), synthesis and place-and-route tools.

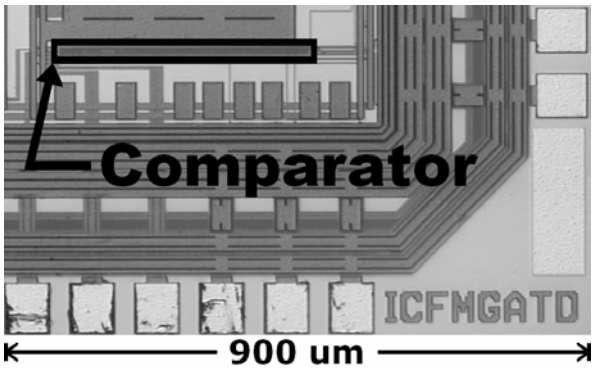


Figure 4.6: Microphotograph section of the integrated circuit test chip implementing a time-mode voltage comparator (TMVC).

A microphotograph of the fabricated test die is illustrated in Figure 4.6. The TMVC occupies a silicon area of 85-µm x 12-µm while the calibration circuitry occupies 285-µm x 12-µm. This surmounts to a total area of 4440-µm^2.

4.4 - Experimental Results

Five integrated circuit (IC) test dies were packaged in 44-pin ceramic quad flat packages. A custom two layer PCB, shown in Figure 4.7(a), was manufactured to interface the IC to the test equipment. A Teradyne A567 mixed-signal ATE was employed to perform all the testing, process the data, and store the results. Figure 4.7(b) shows the ATE testing environment with the PCB and IC affixed.

The performance of the comparator is summarized in Table 4.1. Each TMVC consumes approximately 0.9 mW of power while operating at the ATE's maximum digital signaling speed of 25 MHz. The smallest realizable LSB

(a) **(b)**

Figure 4.7: Experimental test setup (a) PCB designed to test the integrated circuit; (b) A567 ATE used to test the IC.

Table 4.1: Time-mode voltage comparator performance summary.

Parameter	Performance
Technology	0.18-μm CMOS
Supply	1.8 V
Resolution	8-bits
Power Consumption (@25 MHz)	900 μW
Area	370-μm x 12-μm
Maximum Sampling Frequency	200 MHz
Input Voltage Range	1 V

resulted in the comparator having a resolution of approximately 8-bits.

The calibration data at input reference voltages varying between 0.4-V and 1.4-V was extracted from the five sample ICs. The calibration data, shown in Figure 4.8(a), demonstrate that there is a significant difference in process variation between the identically designed devices. It also reveals that the calibration data changes with input reference voltage. The input-referred offset voltage of the five samples was determined for the same reference voltages. Figure 4.8(b) illustrates these test results, showing that all offsets stay within 1 mV of each other, and well within half a LSB from the reference voltage. Therefore, the comparator does compensate for mismatch and functions correctly within an 8-bit resolution.

4.5 - Conclusion

This chapter introduced a voltage comparator design based on the time-mode signal processing strategy described in Chapter 3. The proposed time-mode voltage comparator (TMVC) is implemented by two voltage-controlled delay units

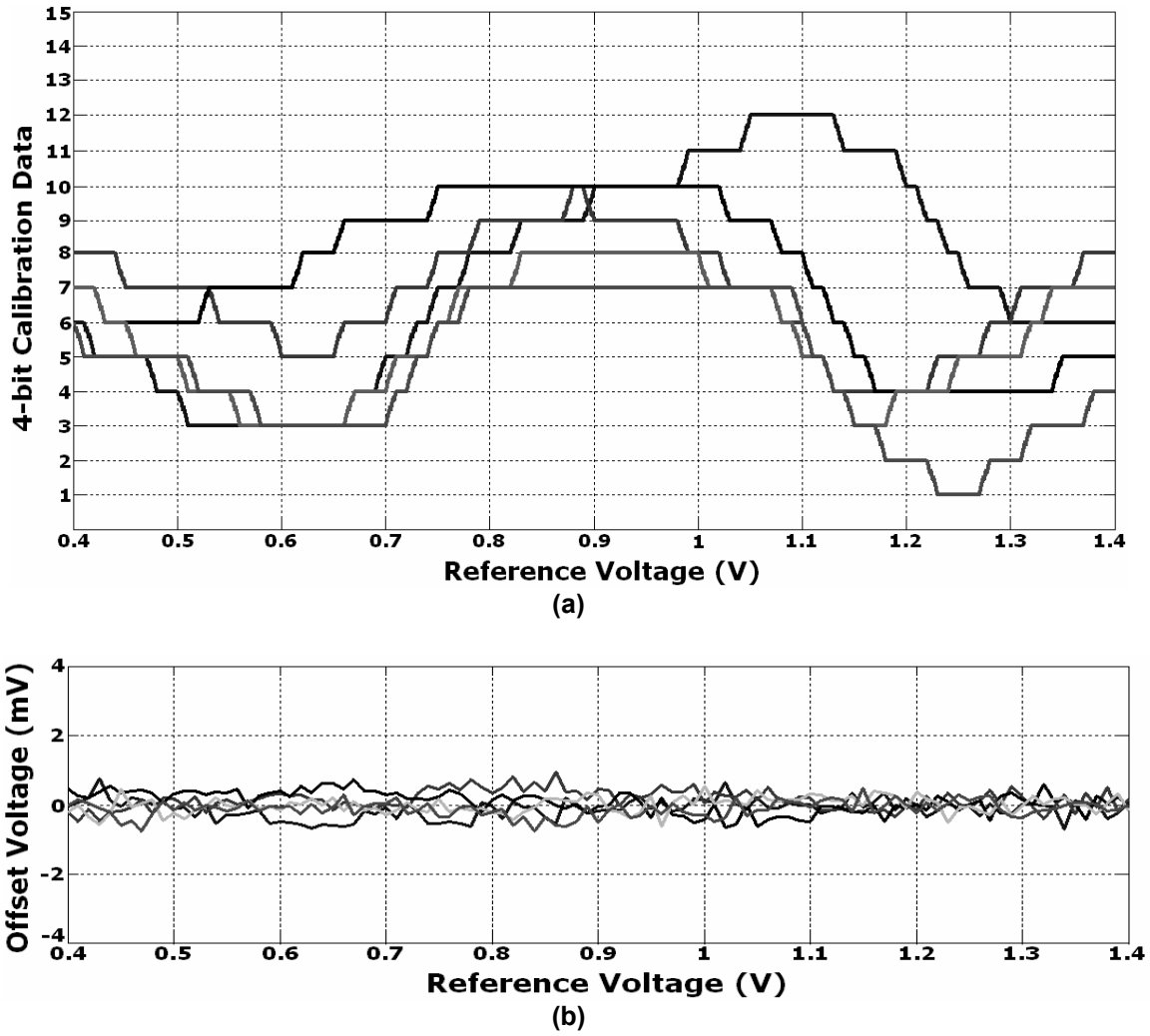


Figure 4.8: Experimental results for the time-mode comparator with calibration. (a) Calibration data of 5 chips collected over a 1-V input reference range. (b) Compensated input-referred offset voltage.

and a flip-flop used as a time comparator. This design approach produces a completely digital circuit which offers the advantages of low power, small area, and high speed comparisons. A methodology to calibrate the TMVC for process variation was presented. It is also constructed form digital circuitry thus offering the same advantages. Moreover, the calibration mechanism is incorporated into the normal operation of the comparator therefore compensating for the errors in the calibration circuitry as well.

The TMVC design is not without its limitations. It was noted that the offset between two VCDUs is input-voltage dependant. Hence, the comparator must be calibrated for every input reference voltage. Such a requirement makes the TMVC suitable for fixed reference voltage application such as flash ADCs. It was also noted that the resolution is limited by the combination of the voltage-to-time gain of the VCDUs and the time-comparator's metastability. It is expected that resolution and speed will improve with down-scaling technologies.

The TMVC was fabricated in a 0.18-um CMOS technology and its experimental results demonstrated that the TMVC could achieve an 8-bit resolution while sampling at the maximum ATE clock rate of 25 MHz. It was shown that mismatch does occur between five devices and that the calibration scheme successfully corrects for their mismatch-induced offset voltages.

Chapter 5: Time-Mode Flash ADC

There are two possible topologies to implement a flash analog-to-digital converter using the time-mode signal processing blocks. The first possibility is to use time-mode voltage comparators described in the previous sections. The second method is to use a VTC followed by a TDC. Both these methods are described in this chapter. A time-mode flash ADC was implemented in CMOS technology and its experimental results are presented.

5.1 - Time-Mode Flash ADC using Time-Mode Voltage Comparators

A conventional flash ADC architecture was introduced in Chapter 2 whereby a *D*-bit converter employed 2^D-1 comparators and a resistor voltage divider to generate 2^D-1 voltage references. Each comparator compares the input voltage V_{IN} with a different reference voltage, as shown in Figure 5.1. The collective outputs of all comparators form a thermometer code digital word which is summed or encoded to generate the digital binary output D_{OUT}.

A flash ADC using TMVCs is implemented by simply replacing the comparators in Figure 5.1 with TMVCs, such as the design offered in Chapter 4. A typical problem in the design of flash ADCs is the comparator mismatch which results in

voltage offsets. Using the TMVC design with calibration mechanism presented in Chapter 4, the entire flash converter may be calibrated with a single pulse of the clock ϕ_{CLK}. Recalibration would only need to be done if the circuit conditions were modified, such as temperature changes or voltage supply variations.

There are several sources in the time-mode flash ADC that may cause distortion. They are the resistor ladder, calibration switches, VTCs, and the TDCs. The resistor ladder used to generate the reference voltages is a common and serious concern in flash ADCs. Distortion will occur if the resistors are not matched, hence care must be taken in their design and layout. The calibration switches in the TMVC (Figure 4.4) will exhibit non-linear behaviour due to transistor threshold voltages being dependent on input voltage [35]. High performance CMOS switches are challenging to manufacture in state-of-the-art technologies,

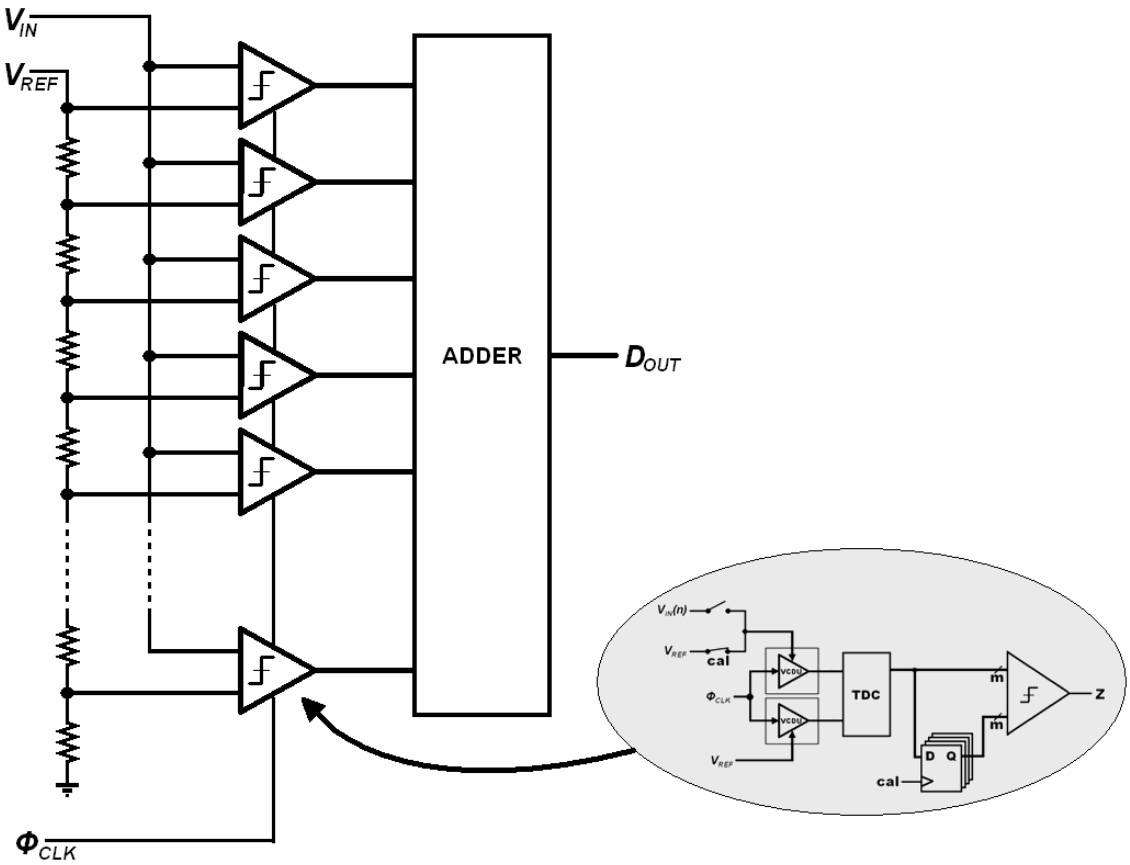


Figure 5.1: Time-mode flash ADC implemented with TMVCs.

hence they must be designed with great caution. The VTCs transfer characteristic is only linear for a small input voltage range as demonstrated in Chapter 3. The loss of gain outside the linear regions can degrade performance and cause distortion to occur. Therefore, it is imperative that the VTC is designed for an adequate gain in the linear operating region and that the input signal voltage be maintained within a reasonable operating range. Finally, the TDC may add nonlinearity due to its mismatch between Vernier delay line stages.

5.2 - Time-Mode Flash ADC using Voltage-to-Time Converter & TDC

A second strategy to implement a time-mode flash ADC, presented in Figure 5.2, is to follow a VTC with a TDC. The design requirements of the TDC are set by the maximum voltage-to-time conversion factor G_ϕ of the VTC. The input voltage must remain in the linear region of the VTC restricting the full scale input voltage range. The maximum time difference applied to the TDC input is $G_\phi V_{FS}/2$, where V_{FS} is input voltage range in its linear region. Note that the full scale voltage is divided by two because the maximum time difference is measured with respect to

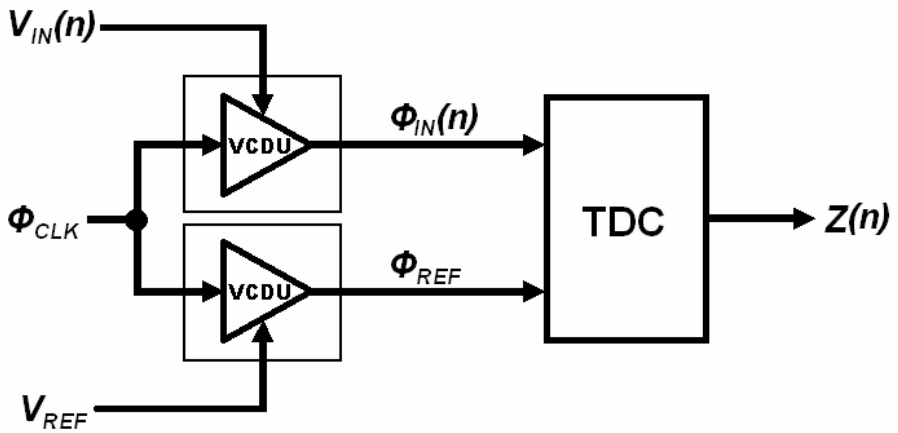


Figure 5.2: Time-mode flash ADC implemented with a VTC followed by a TDC.

a midpoint reference time (i.e. analog ground). Therefore, the TDC must have an input dynamic range of $G_\phi V_{FS}$ seconds, and a resolution of $G_\phi V_{FS}/(2^D-1)$.

The overall converter resolution will be limited by two factors. First, the VTC can produce a limited voltage-to-time conversion factor G_ϕ and the TDC can resolve a minimum input time difference ΔT_{LSB}. These limits are technology dependant and will improve as CMOS processes advance. Combining these two factors, according to Equation (4.10), restricts the resolution in number of bits to

$$D < \log_2\left(\frac{G_\phi V_{FS}}{\Delta T_{LSB}} + 1\right). \tag{5.1}$$

In order to gain further insight into the resolution limits, an example will be used. Recall from Chapter 3 that a direct voltage-control VCDU was designed with a voltage-to-time gain of 7 ns/V and a linear full scale voltage range of 800 mV. Assuming that a TDC can resolve a 10 ps input time difference [36] then Equation (5.1) dictates that the maximum achievable resolution is 9.1-bits.

The second limitation on resolution for this time-mode flash ADC is caused by distortion, which is generated by the nonlinearity of the VTC and the TDC. It was shown in Chapter 3 that the VCDU has a limited range of linearity with errors in the order of ±0.1%. Hence, if the input voltage exceeds the linear region then the time-difference output of the VTC will be severely distorted. The TDC will also contribute to the nonlinearity of the converter despite the design efforts to calibrate TDCs [37] – [39].

5.3 - Integrated Circuit Implementation

An integrated circuit prototype of a 7-bit time-mode flash ADC was fabricated in a 0.18-µm standard CMOS process implementing the converter architecture described in Section 5.1. A microphotograph of the test die is presented in Figure 5.3. The complete design occupies a silicon area of 868-µm x 790-µm.

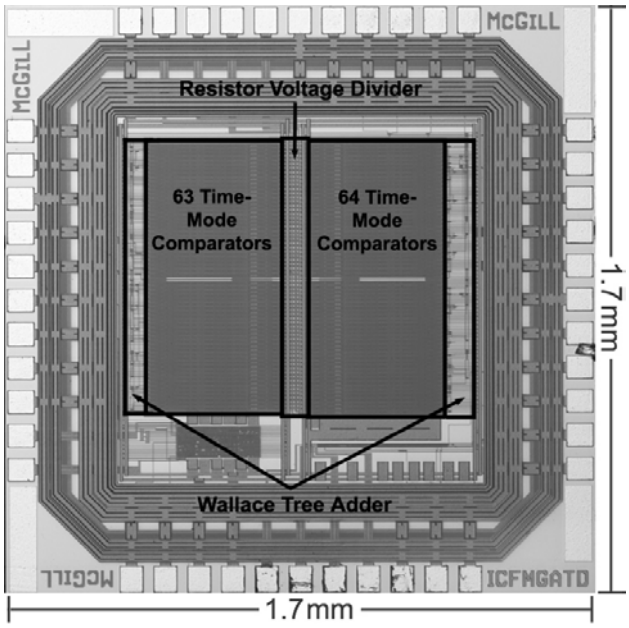
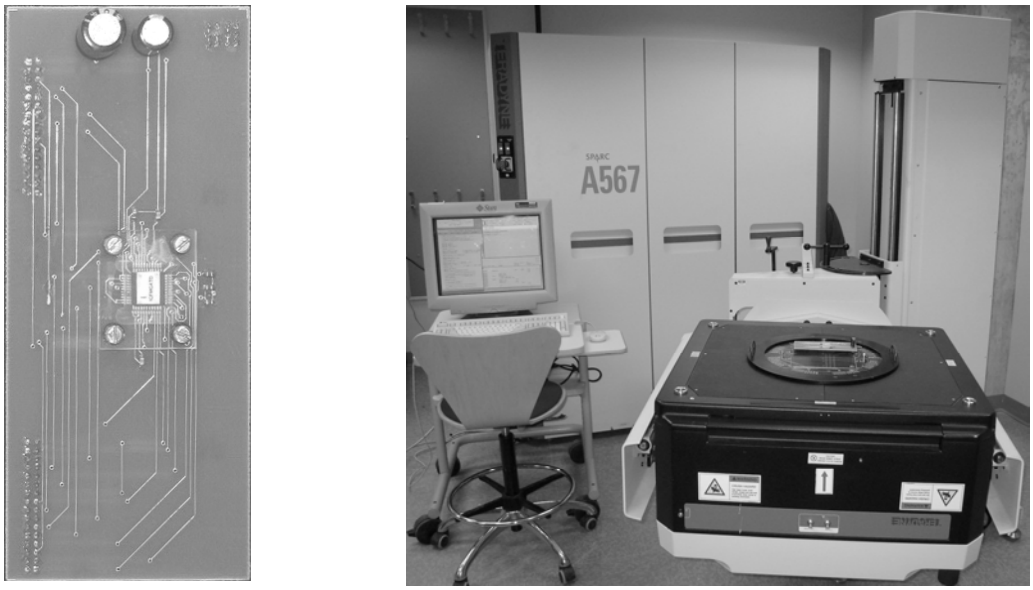


Figure 5.3: Integrated circuit microphotograph of a test chip implementing a 7-bit time-mode flash ADC using TMVCs.

It is composed of 127 time-mode comparators, a resistor divider to generate 127 voltage references, and an adder. The comparators were implemented with the TMVC with calibration described in Chapter 4. The voltage divider resistors were implemented with non-salicide p+ polysilicon and laid out in a shuffle pattern [40] to improve their matching. The comparator thermometer code output was encoded with a Wallace tree adder to avoid any missing codes from code bubbles. The adder was generated using HDL and laid out using automated place-and-route tools.

5.4 - Experimental Results

The IC was tested using a Teradyne A567 mixed-signal ATE which supplied the power supplies, precision low-frequency signal source, and digital signal source and data capture. A custom PCB was manufactured to affix to the ATE's device interface board. The PCB and test environment are displayed in Figure 5.4.



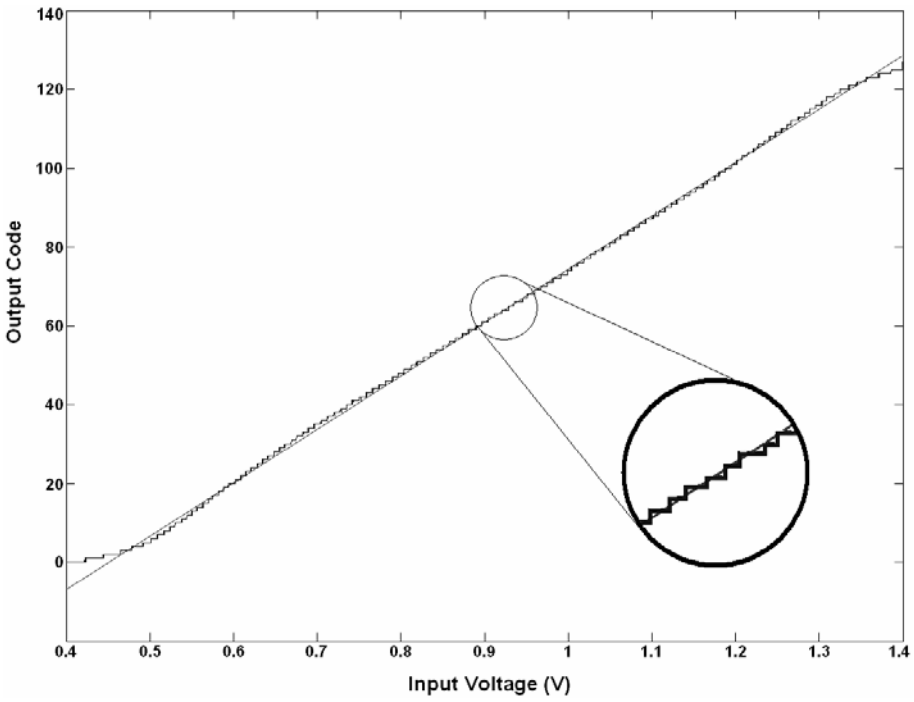
(a) (b)

Figure 5.4: Experimental test setup: (a) PCB designed to test the time-mode flash ADC integrated circuit; (b) Teradyne A567 ATE used to test the IC.

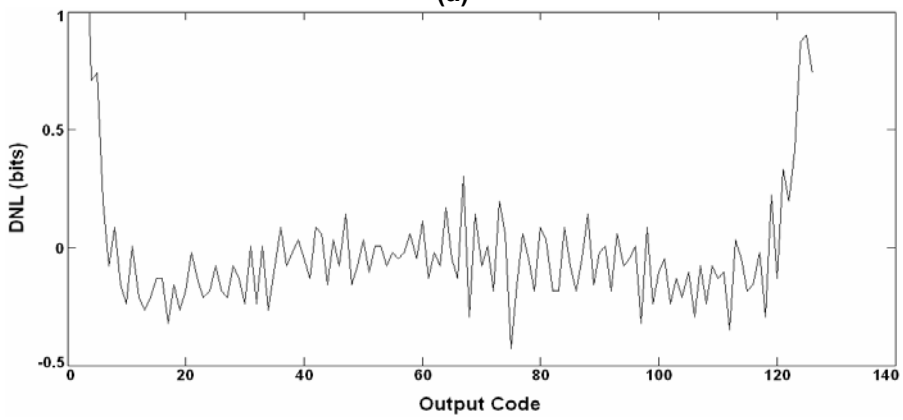
Because the flash ADC was designed for operation at modest speeds and mediocre resolutions the PCB was designed as a two layer board with signal traces on the top layer and a ground plane on the bottom.

The linearity of the time-mode flash ADC was obtained by sweeping the input voltage between 0.4 and 1.4 volts. The output digital data resulting from this test are presented in Figure 5.5(a). Using this data the differential nonlinearity, displayed in Figure 5.5(b), was discovered to be within ±0.35 LSBs within the linear input voltage range of 0.5 – 1.3 volts. The integral nonlinearity, displayed in Figure 5.5(c), was extracted with a best-fit line and was determined to be ±2 LSBs for an input voltage range of 0.5 – 1.3 volts.

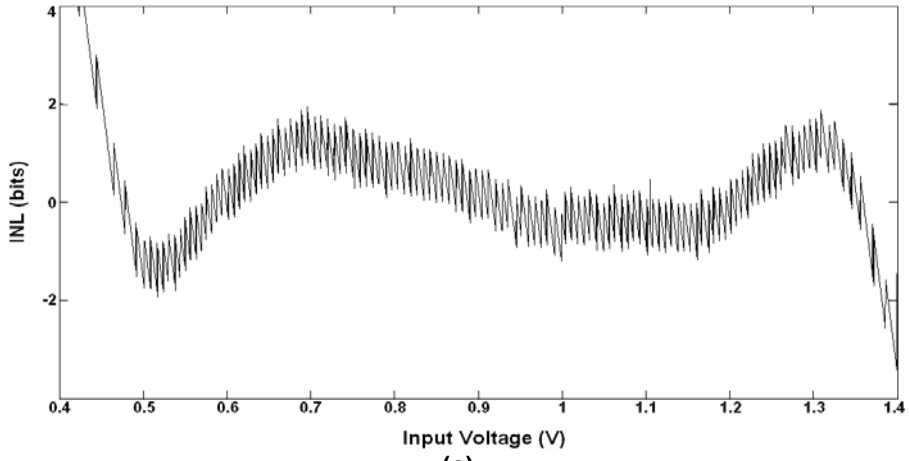
The time-mode flash ADC was exercised dynamically with a 0.8-V peak-to-peak 215-kHz input sinusoidal voltage while sampling at a frequency of 5-MHz. Figure 5.6 displays the power spectral density (PSD) of the ADC output. A SNR of 44.1



(a)



(b)



(c)

Figure 5.5: Experimental results for the time-mode flash ADC. (a) Output digital code and line-of-best fit. (b) Differential Nonlinearity (DNL), (c) Integral Nonlinearity (INL).

dB and a SNDR of 39.8 dB were achieved thus confirming the 7-bit accuracy of the converter.

A summary of the time-mode flash ADC's performance is given in Table 5.1. It should be noted that the ADC was sampled at a maximum conversion rate of 5 MHz. Theoretically, this converter should be able to process at 200 MHz as this is the limit imposed by the TMVCs. It was discovered during the testing phase that the Wallace tree adder circuitry has a maximum propagation delay of approximately 150 ns with unequal data path delays. As a result the adder is restricting the data rate to 5 MHz.

5.5 - Summary

The concept of flash A/D conversion using the TMSP methodology was investigated in this chapter. Two different styles of flash ADCs were presented; one implemented as a conventional flash ADC with the comparators replaced by

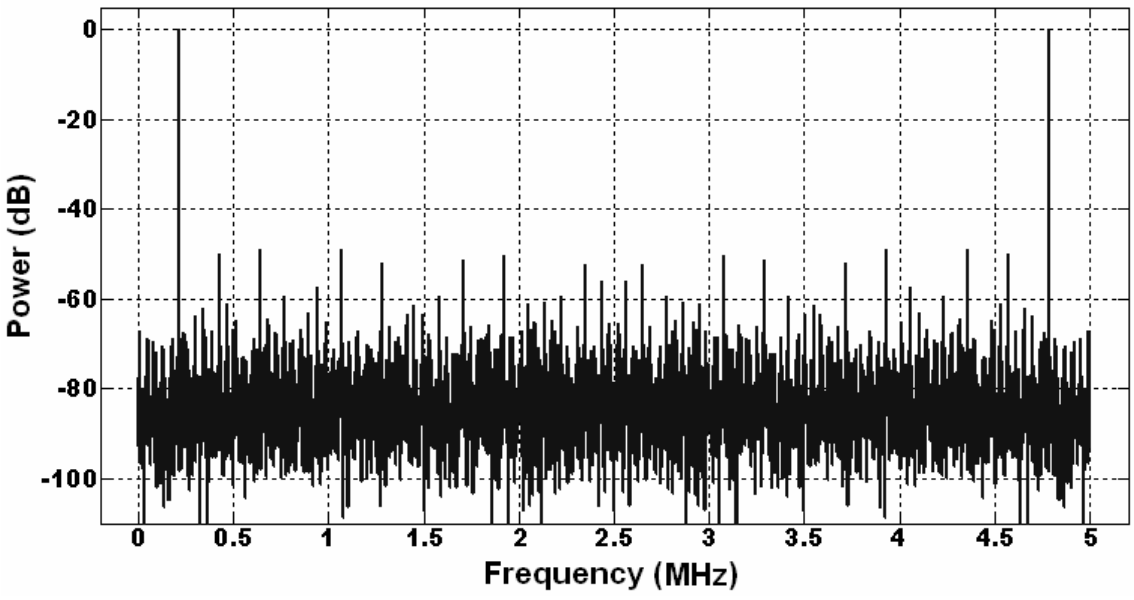


Figure 5.6: PSD for the time-mode flash ADC operating with a sampling frequency of 5 MHz and 215-kHz input test signal with a 1-V_{p-p} amplitude.

TMVCs and the other design implemented with a VTC followed by a TDC. The advantages and disadvantages of each architecture were discussed. A 7-bit time-mode flash ADC was fabricated and the IC was tested. The experimental results demonstrated that the flash ADC produced a 7-bit resolution with some distortion. Although the experimental circuit was restricted to a 5 MHz sampling rate, this design should be able to convert at a theoretical rate of 200 MHz, provided that the digital encoding circuitry is constructed with an adequate propagation delay.

Table 5.1: Time-mode flash ADC performance summary.

Parameter	Performance
Technology	0.18-μm CMOS
Supply	1.8 V
Area	0.686 mm^2
Resolution	7-bits
Maximum Sampling Frequency	5 MHz (experimental) 200 MHz (theoretical)
Input Voltage Range	0.8 V (peak-to-peak)
Differential Non-Linearity	±0.35 LSB
Integral Non-Linearity	±2 LSB

Chapter 6: Time-Mode Delta-Sigma ADC

Delta-sigma (ΔΣ) analog-to-digital conversion, introduced in Chapter 2, is one of the most popular data conversion strategies that has dominated the electronics industry for applications with high resolution and mediocre bandwidth requirements. The ΔΣ modulation techniques range in complexity from first-order and single-bit designs to eighth-order [41] and four-bit [42] architectures. This chapter presents a ΔΣ ADC design methodology that utilizes the TMSP blocks described in Chapter 3. The design will hereafter be referred to as the time-mode delta-sigma analog-to-digital converter or TMΔΣADC. Two IC prototypes were fabricated and their designs and results are presented in this chapter.

6.1 - Design Methodology

The conventional ΔΣ ADC was introduced in Chapter 2. The TMΔΣADC system is designed based on the error-feedback structure for a ΔΣ modulator, as reproduced in Figure 6.1. The system model in this configuration may be implemented with a dual-input integrator, a comparator, and a DAC. The loop formed by the two summation blocks and the delay element is a two-input integrator with inputs $V_I(n)$ and $V_O(n)$. The dual-input time-mode integrator was introduced in Section 3.3.2, and will be used as the core of the time-mode ΔΣ modulator design. The comparator block is implemented with the time

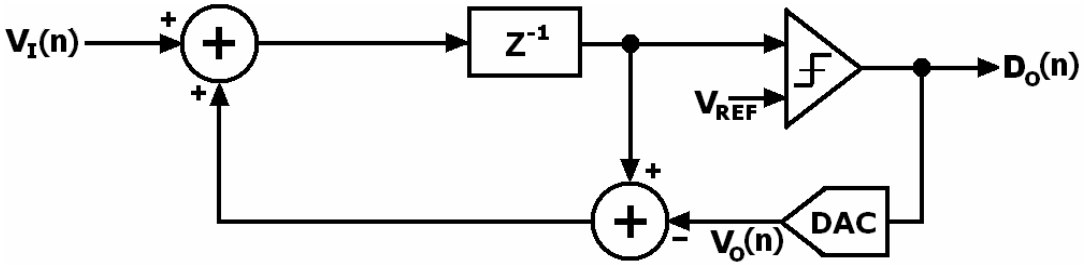


Figure 6.1: First-order single-bit delta-sigma analog-to-digital converter error-feedback model.

comparator as described in Chapter 3. If full scale voltages are being used then the DAC may be eliminated such that $V_O(n) = D_O(n)$. Otherwise, a single-bit DAC would be implemented consisting of a pair of analog switches. Recall from Chapter 3 that the summation block was implemented using a VCDU which incorporates the sample-and-hold action under certain frequency and resolution conditions governed by the equation

$$f_{IN} \leq \frac{F_S}{\pi\left(2^D - 1\right)}, \tag{6.1}$$

where F_S is the sampling frequency, D is the converter's resolution in number of bits, and f_{IN} is the largest input signal frequency (i.e. the bandwidth). If this inequality is not satisfied based on design requirements then a sample-and-hold would need to be incorporated into the design.

The complete system of the TMΔΣADC is presented in Figure 6.2 and consists of two dual-input integrators and a D-type edge-triggered flip-flop. The reference oscillator, i.e. the bottom dual-input integrator, provides the clock reference ϕ_{REF} generating the analog time reference T_{REF} with the secondary function of clocking the data out of the D-type flip-flop. The signal oscillator, i.e. the top integrator, sums the input voltage with the inverse of the digital output voltage producing the difference equation

$$\Delta T_O(n) - \Delta T_O(n-1) = G_\phi\left(V_{IN}(n-1) - D_O(n-1)\right), \tag{6.2}$$

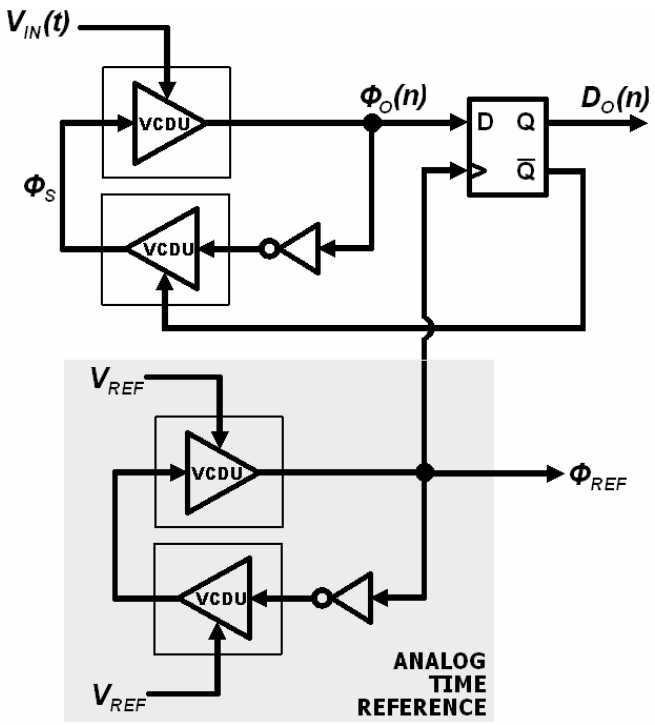


Figure 6.2: First-order single-bit delta-sigma time-mode delta-sigma analog-to-digital converter (TMΔΣADC).

where G_ϕ is the voltage-to-time conversion factor of the VCDUs and ΔT_O is measured with respect to the analog time reference T_{REF}. Note that this design is a discrete-time system since the analog input voltage is sampled by the VCDUs and converted into time-difference variables which are processed at discrete time intervals.

The error signal $T_\varepsilon(n)$ made by the flip-flop comparison with respect to the analog time reference T_{REF} may be expressed as the difference between the input time difference $\Delta T_O(n)$ and the digital output $D_O(n)$ scaled by G_ϕ, i.e.

$$T_\varepsilon(n) = G_\phi D_O(n) - \Delta T_O(n). \tag{6.3}$$

Substituting the flip-flop error model from Equation (6.3) into (6.2) reveals the first-order ΔΣ modulator difference equation

$$D_O(n) = V_{IN}(n-1) + \frac{1}{G_\phi}\left[T_\varepsilon(n) - T_\varepsilon(n-1)\right]. \tag{6.4}$$

Figure 6.3 presents an example timing diagram illustrating a 4-period sample of the modulator's operation. Note that the inverter and flip-flop delays were neglected for this exercise. The quantity T_{RESET} is defined as the time through both VCDUs during the reset phase (i.e. falling edge). T_{REF} is the delay through both VCDUs of the reference oscillator controlled by V_{REF} during a positive going edge. Hence, the sampling period is given by $T_{REF}+T_{RESET}$. The delay $T_I(n)$ through both VCDUs in the signal oscillator is controlled by $V_I(t)$ and the flip-flop output $V_O(n)$ during a positive going edge. It may be expressed as

$$T_I(n) = G_\phi V_I(n-1) - G_\phi V_O(n-1). \tag{6.5}$$

The output $\Delta T_O(n)$ during $n = 1$ may calculated from Figure 6.3 as

$$\Delta T_O(1) = \left[T_I(1) + T_{RESET}\right] - \left[T_{REF} + T_{RESET} - \Delta T_O(0)\right]. \tag{6.6}$$

Note that the polarity of ΔT_O is measured as a positive quantity when ϕ_{REF} leads ϕ_O. Equation (6.6) may be generalized as

$$\Delta T_O(n) = T_I(n) + \Delta T_O(n-1) - T_{REF}. \tag{6.7}$$

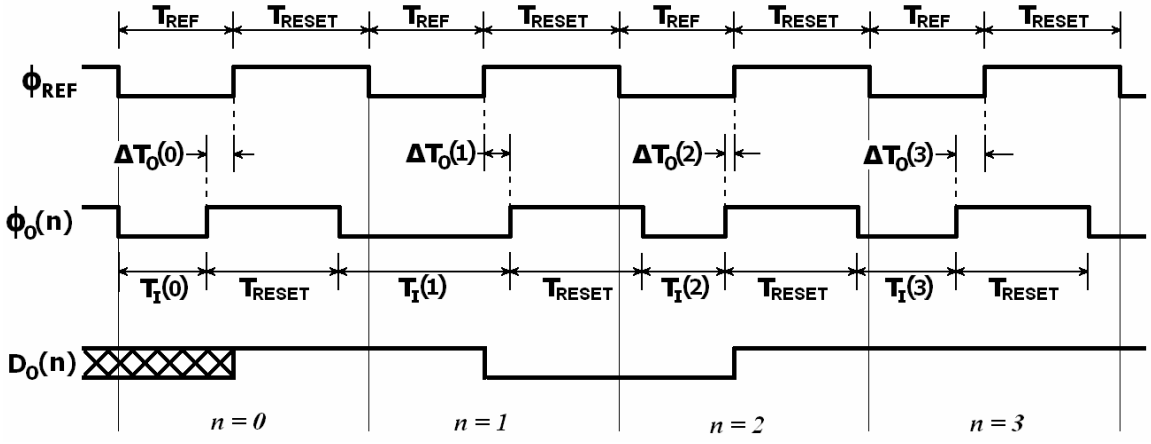


Figure 6.3: Example timing diagram for the first-order single-bit TMΔΣADC.

The reference time T_{REF} may be omitted as it is always assumed that $\Delta T_O(n)$ is measured with respect to the reference. Combining equations (6.3), (6.5), and (6.7), where $D_O(n) = V_O(n)$, results in the following formulation for the first-order ΔΣ modulator

$$V_O(n) = V_I(n-1) + \frac{1}{G_\phi}\left[T_\varepsilon(n) - T_\varepsilon(n-1)\right]. \tag{6.8}$$

6.2 - Implementation Issues

There are several implementation issues which are inherently part of the TMΔΣADC architecture. Moreover, there are some common concerns that affect all circuit designs. These issues are discussed in this section.

6.2.1. Non-Uniform Sampling

The sample-and-hold action is being performed by the VCDU with respect to the sampling clock ϕ_S, as indicated in Figure 6.2. The sampling clock edge measured with respect to the reference clock ϕ_{REF} is also the error signal $T_\varepsilon(n)$ which is assumed to be uniformly distributed [20] with an RMS value of

$$T_{S-RMS} = \frac{2G_\phi A}{\sqrt{12}}, \tag{6.9}$$

where A is the maximum peak amplitude of the input voltage $V_{IN}(t)$. Hence, the input voltage is sampled non-uniformly which imposes a limitation on the performance of the overall TMΔΣADC design. This sampling mimics the effects of clock jitter. Using a formula from [43], the RMS noise $v_{n\text{-}RMS}$ that will result from this non-uniform sampling can be estimated by

$$v_{n-RMS} \approx \frac{2\pi A f_O}{\sqrt{2}} T_{S-RMS} = \frac{2\pi G_\phi A^2 f_O}{\sqrt{6}}, \tag{6.10}$$

where f_o is the maximum frequency of the input signal. Although this noise is present, its magnitude is not predominant for low amplitudes or low frequencies. Furthermore, it may be controlled by the VCDU's voltage-to-time conversion factor G_ϕ. As an example, suppose the current-starved inverter VCDU described in Chapter 3 was used where G_ϕ is 320 ps/V and the input amplitude is 200 mV. With an input bandwidth of 1 MHz, the resulting RMS voltage noise $v_{n\text{-}RMS}$ is 65.7 μV. Using the formula for SNR described in Chapter 2, this example TMΔΣADC will provide a best-case SNR of 72.7 dB which translates to an almost 12-bit resolution.

6.2.2. Synchronization

The TMΔΣADC is a synchronous ADC, however, the sampling clock must be generated on chip as it is implicitly part of the oscillating integrator operation. Moreover, the reference clock must also be generated on chip which will oscillate at the same frequency as the sampling clock in order to provide the analog time reference ϕ_{REF}. An additional benefit of this design is that the reference clock ϕ_{REF} and modulator clock $\phi_O(n)$ will automatically lock phases due to the system's negative feedback.

6.2.3. Mismatch

If the signal and reference oscillators are mismatched then their frequencies may vary. Consequently either the reference time T_{REF} will be skewed or the reset times T_{RESET} will differ between the oscillators. Consider, for example, that the VCDU reset times differ such that the reference and signal oscillator reset times are T_{RESET1} and T_{RESET2}. Equation (6.7) would become

$$\Delta T_O(n) = T_I(n) + \Delta T_O(0) - T_{REF} + \left[T_{RESET2} - T_{RESET1}\right]. \tag{6.11}$$

Substituting Equations (6.3) and (6.5) into (6.11) produces the modulators difference equation

$$V_O(n) = V_I(n-1) + \frac{1}{G_\phi}\left[T_\varepsilon(n) - T_\varepsilon(n-1)\right] + \frac{1}{G_\phi}\left[T_{RESET2} - T_{RESET1}\right]. \tag{6.12}$$

Therefore, any mismatch which results from oscillator timing errors will manifest itself as a DC offset. In order to minimize this effect, two reference voltages are used to tune the analog time reference oscillator. Furthermore, a simple calibration scheme could be implemented which extracts the DC offset from the digital output and adjust the reference voltages accordingly.

6.2.4. Jitter Noise

Jitter noise on the sampling clock may arise from thermal noise, poor power and ground supplies, or EMI from external lines or devices. Consequently, jitter noise will manifest itself as an additive voltage noise source [43] with RMS value given by

$$v_{j-RMS} \approx \frac{2\pi A f_O}{\sqrt{2}} T_{j-RMS}, \tag{6.13}$$

where $T_{j\text{-}RMS}$ is the RMS value of the jitter induced noise, f_O is the input signal frequency, and A is the amplitude of the input signal.

6.2.5. Flip-Flop Metastability

Flip-flops have two stable states designated with logic 0 and logic 1. When the two input transitions edges are close together the flip-flop output may enter an unknown state, known as the metastable state. Given sufficient time the flip-flop output will reach one of the two stable states. However, noise may influence the flip-flop to make an incorrect comparison. Hence, metastability may result in the processing of an unknown logic state or an erroneous state. Although it was not used in this design, a technique to reduce the influence of flip-flop metastability is

to pre-amplify the input time-difference using a time-amplifier, as discussed in Chapter 3.

6.2.6. VCDU Non-Linearity

It was demonstrated in Chapter 3 that the VCDU circuits are linear within a limited input voltage range. Even within this range there remains some non-linearity in the order of ±0.1%. Therefore, the VCDUs may be the greatest factor in limiting the SNDR performance of the TMΔΣADC.

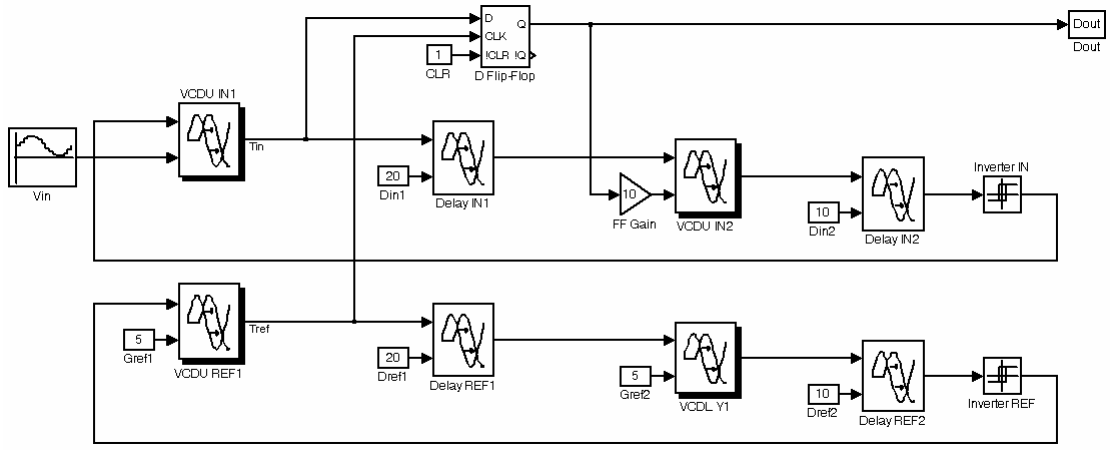
6.3 - Single-Ending Input Implementation

The first-order single-bit TMΔΣADC illustrated in Figure 6.2 may be modeled in MATLAB and designed in HSPICE, as presented in this section.

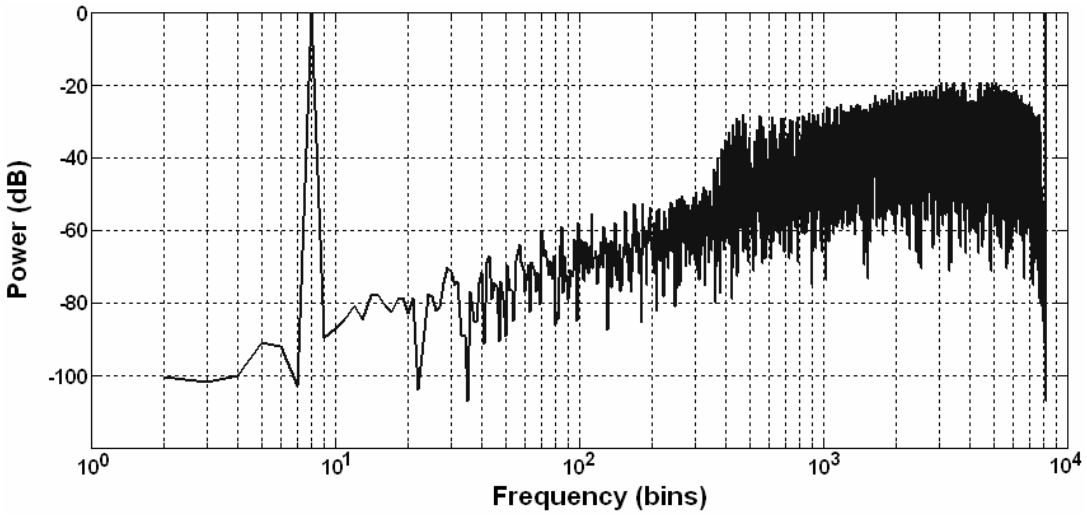
6.3.1. Mathematical Modeling with MATLAB and Simulink

The first-order single-bit TMΔΣADC was simulated in MATLAB using the Simulink modeling environment. The block diagram of the model is shown in Figure 6.4(a). VCDUs were implemented with transport delay blocks, a D flip-flop was used for the time comparator and the inverters were replaced with relay blocks. Some delay elements were incorporated to facilitate the processing time of the transport delay blocks. These delay blocks were also implemented using transport delay blocks controlled by constant delays.

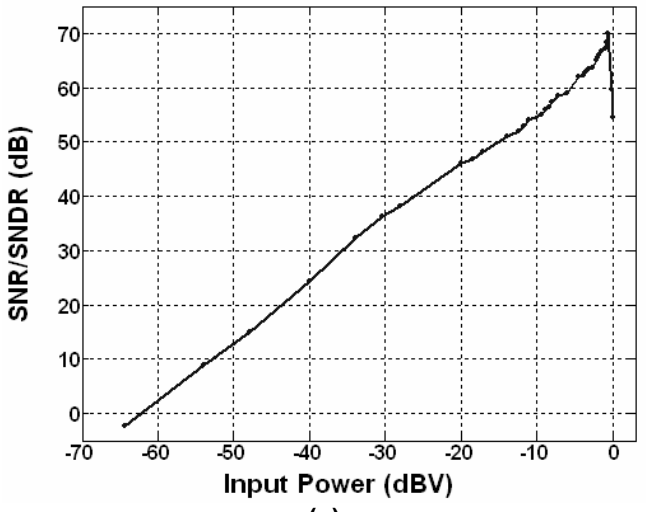
A simulation with 8192 points was collected and the PSD of the output is presented in Figure 6.4(b). At an oversampling ratio (OSR) of 585, the SNR is 88 dB. At an OSR of 195, the SNR is 70 dB. These data correspond to resolutions



(a)



(b)



(c)

Figure 6.4: Mathematical modeling of the TMΔΣADC: (a) MATLAB Simulink model diagram, (b) MATLAB simulation power spectral density (PSD) results, (c) dynamic range.

of over 14-bits and 11-bits, respectively. It may be seen from the PSD plot that the noise increases with frequency at a 20 dB/decade rate, as expected for a first-order modulator. The input dynamic range, shown in Figure 6.4(c), was determined by calculating the SNDR of the MATLAB simulation for various input levels. An OSR of 195 was used for the bandwidth measurements and the dynamic range was determined to be 63 dB.

6.3.2. Low-Speed TMΔΣADC Transistor Design and Simulation

The TMΔΣADC was designed in a 0.18-μm standard CMOS process and the complete transistor circuit is presented in Figure 6.5. The VCDUs were implemented using the current-starved inverter design as described in Chapter 3.

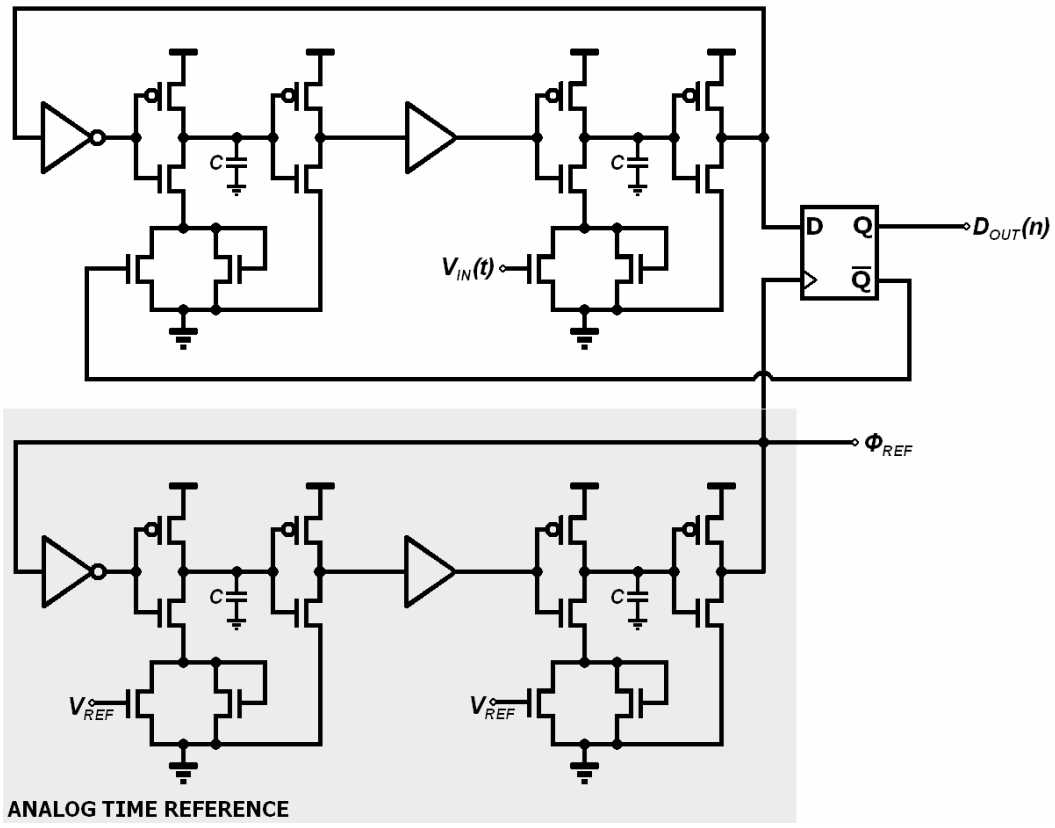


Figure 6.5: Transistor schematic for the low-speed first-order single-bit TMΔΣADC.

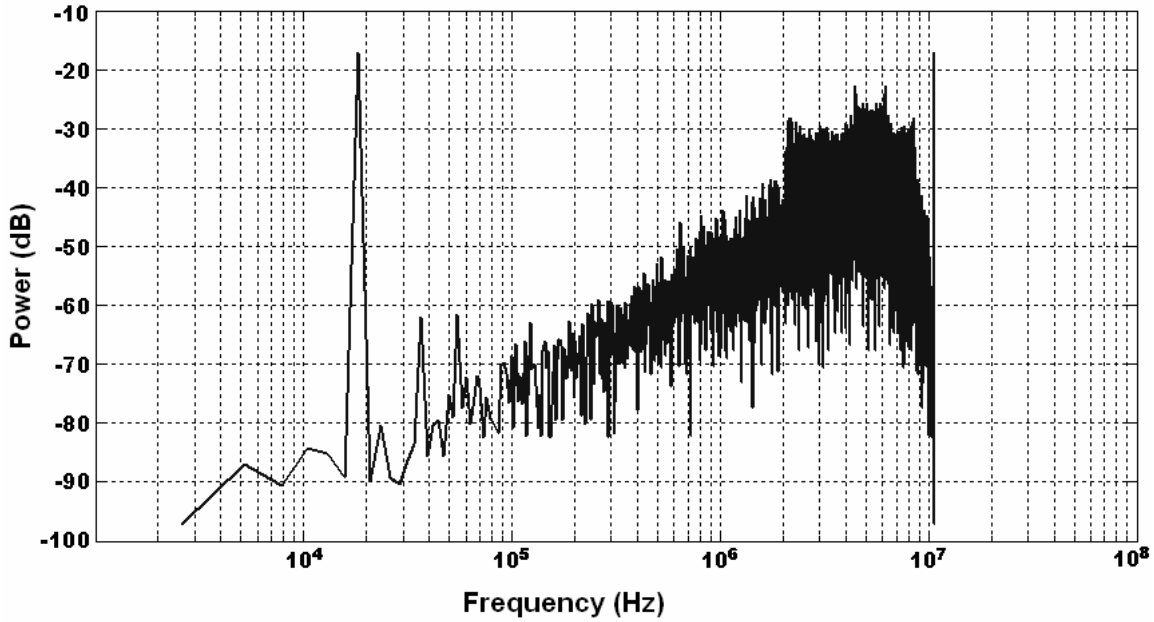


Figure 6.6: HSPICE simulation PSD results of the single-ended input first-order single-bit TMΔΣADC sampling at 10.7 MHz.

Appendix A presents the transistor dimensions for the complete design. 500 fF capacitors were included to increase the voltage-to-time gain factor of the VCDUs to 14.5 ns/V. The top oscillator is controlled by the input voltage $V_{IN}(t)$ and digital feedback voltage from the flip-flop. The bottom oscillator provides the analog time reference ϕ_{REF} and is controlled by two reference voltages V_{REF}. Note that no sample-and-hold is being implemented thus relying on the VCDUs to perform the sampling action. The flip-flop was implemented with a library standard cell. The inverters and buffers are implemented in the complementary logic style and are sized to add appropriate delays to the oscillators to ensure that the flip-flop output reaches a stable state before it is sampled by the VCDU.

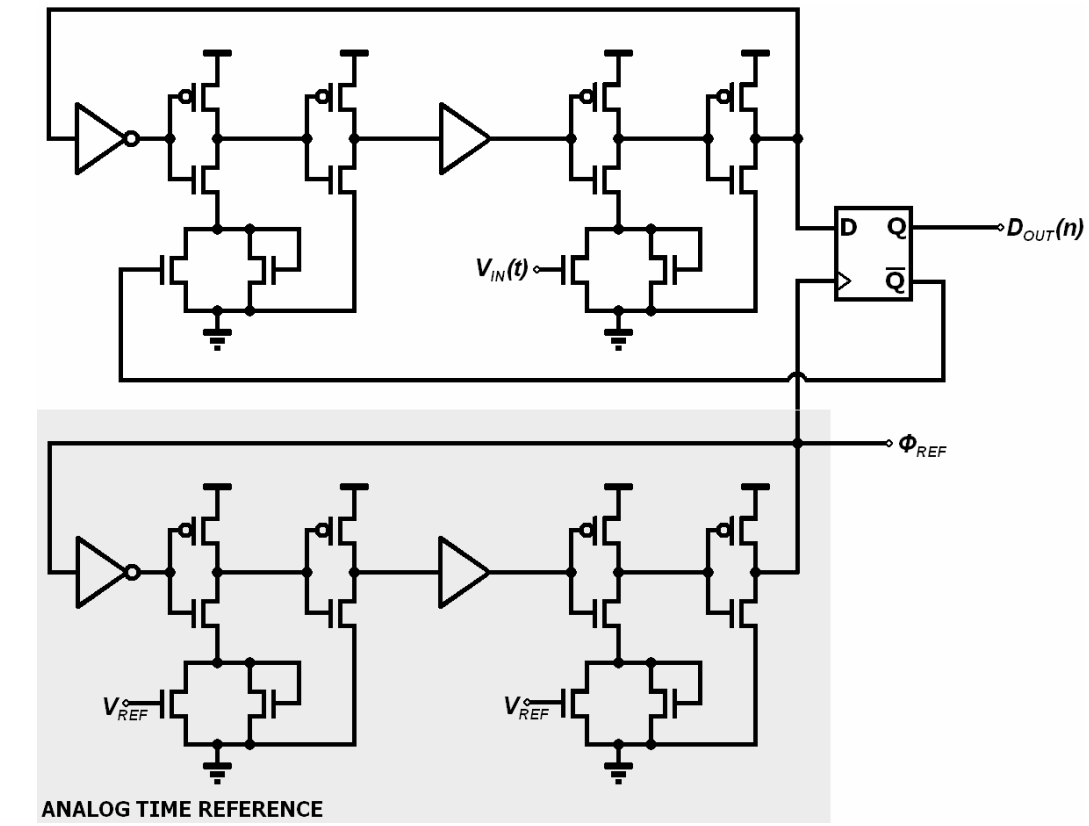
The circuit in Figure 6.5 was simulated using HSPICE. The reference oscillator was biased at 1-V and the input signal was a 18 kHz sinusoid with a 200-mV peak amplitude. The PSD result of the TMΔΣADC is presented in Figure 6.6. The sampling frequency was determined to be 10.7 MHz. The SNR in an 18-kHz bandwidth (i.e. OSR of 297) is 62 dB. The SNDR in a 55-kHz bandwidth (i.e. OSR of 97) is 45 dB. It may be observed that second and third harmonic distortion components are present.

6.3.3. High-Speed TMΔΣADC Transistor Design and Simulation

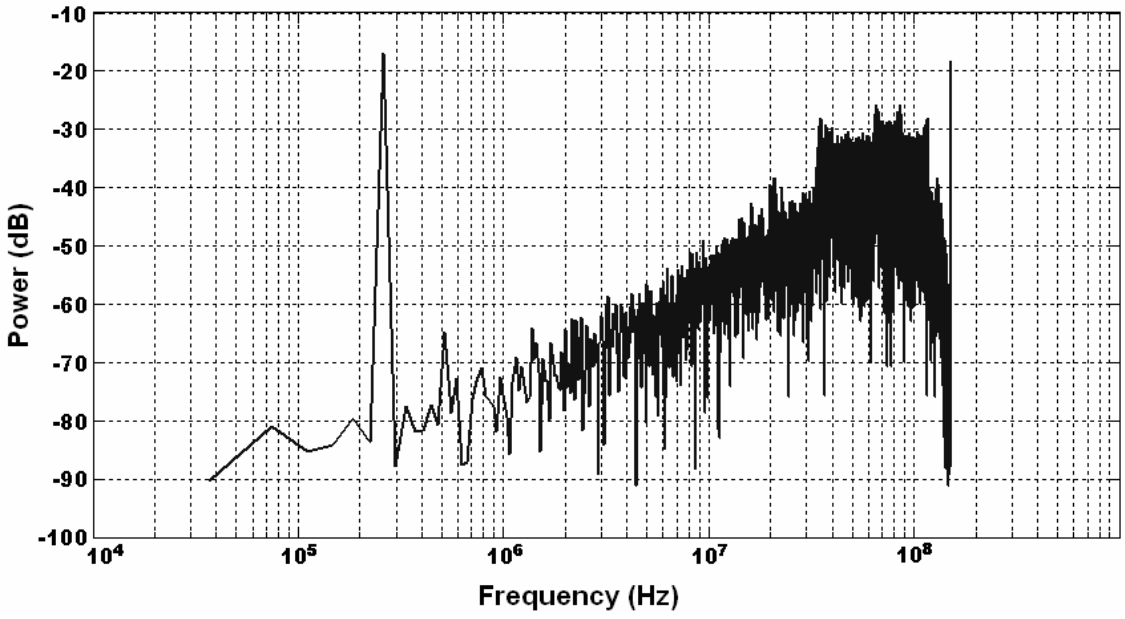
The circuit in Figure 6.5 may be transformed into a higher-speed design by omitting the capacitors in the VCDU, as presented in Figure 6.7(a). A PSD HSPICE simulation result for this circuit is shown in Figure 6.7(b). The reference oscillator was biased at 1-V permitting a sampling frequency of 150 MHz. The signal oscillator was exercised by a 100 kHz sinusoid biased at a DC offset of 1 V with a 400-mV peak-to-peak amplitude. The SNR in a 100-kHz bandwidth (i.e. OSR of 750) is 58 dB and the SNDR in a 400-kHz bandwidth (i.e. OSR of 188) is 48 dB.

This architecture offers many advantages over the slower-speed design. First, the sampling speed is higher which permits a greater OSR. This implies that the faster design may have a better resolution for the same bandwidth or a greater bandwidth with the same resolution. The second advantage is that the area is significantly reduced as capacitors occupy a relatively large silicon area.

Finally, it may be observed that distortion is much less in the higher-speed design. This is a direct result of the reduced voltage-to-time conversion factor in the faster VCDUs design.



(a)



(b)

Figure 6.7: First-order single-bit high-speed TMΔΣADC (a) transistor schematic; (b) HSPICE simulation PSD result.

6.4 - Differential-Input Implementation

The single-ended input first-order single-bit TMΔΣADC in Figure 6.2 may be converted into a differential design by connecting the non-inverting flip-flop output (i.e. $D_O(n)$) to the first reference oscillator VCDU input and changing the second reference oscillator VCDU input to the opposing differential input voltage. Figure 6.8 demonstrated the differential design with differential input voltages V^+_{IN} and V^-_{IN}. Biasing of the oscillators is set by the DC offset of the input voltages.

There are a few advantages to the differential design. First, the common-mode noise will be rejected. Second, the differential input offers a doubling of the signal amplitude resulting in a 0.5-bit or 3-dB improvement in the SNR. A third advantage is that the even-order harmonic distortion components caused by the VCDU non-linearity will be suppressed. Another advantage is that no reference

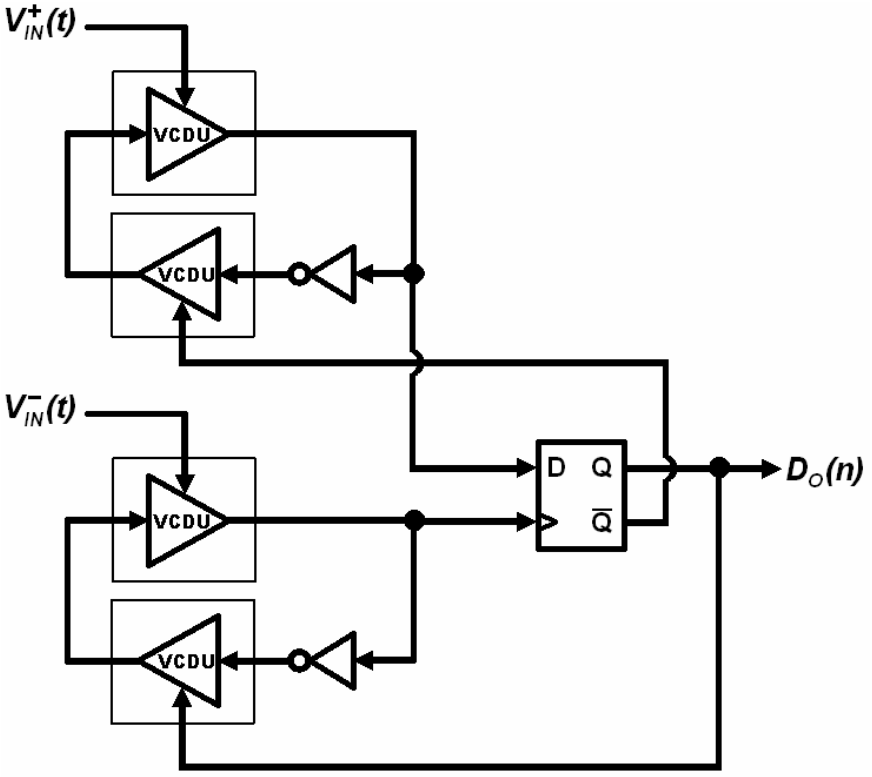


Figure 6.8: Differential-input first-order single-bit TMΔΣADC.

voltages are required for the design.

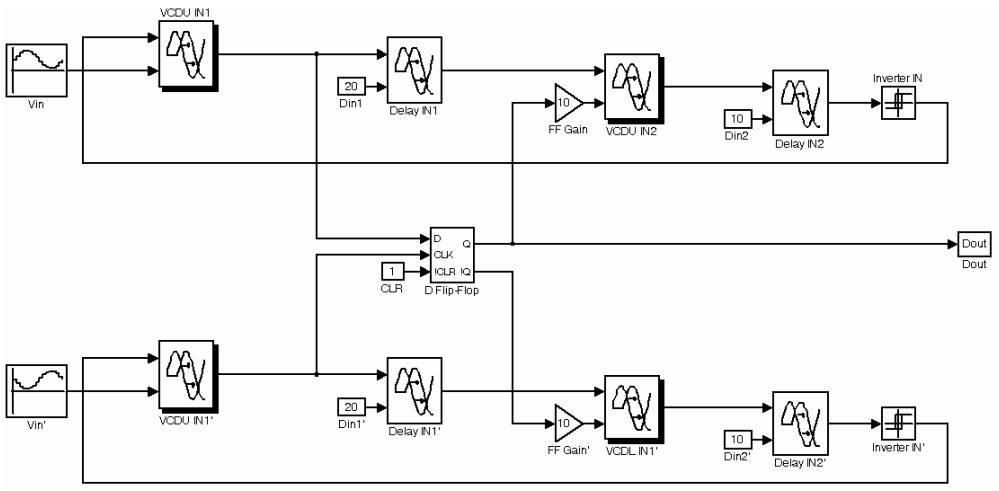
A disadvantage of this design is that the non-uniform sampling has doubled. Therefore, sample-and-hold circuits are not easily implemented as there is no regular clock signal such as the reference clock in the single-ended design.

6.4.1. Mathematical Modeling with MATLAB and Simulink

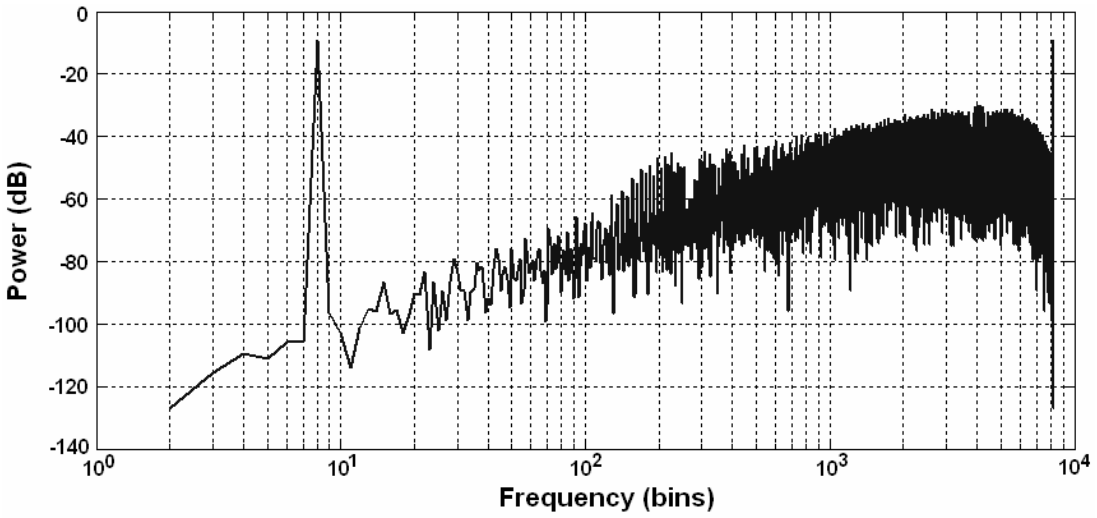
The differential-input TMΔΣADC design was simulated in MATLAB using the Simulink model shown in Figure 6.9(a). 8192-point PSD simulation results, shown in Figure 6.9(b), predict that the SNR at an OSR of 585 is 92 dB and the SNDR at an OSR of 195 is 73 dB. It is interesting to note that these metrics are 4-dB and 3-dB better than the respective MATLAB simulations performed for the single-ended input design. The input dynamic range data was also gathered using an OSR of 195 and is presented in Figure 6.9(c). This model offers a 62 dB range.

6.4.2. Transistor Schematic and Simulation

The transistor level schematic for the differential-input TMΔΣADC is illustrated in Figure 6.10(a) with its transistor dimensions provided in Appendix A. It was learned from the single-ended design that the VCDUs were modifying the time-difference variable during the negative transition edge. Therefore, the VCDUs have been outfitted with AND gates such that the negative-going edges bypass the VCDU, as described in Section 3.2.2.



(a)



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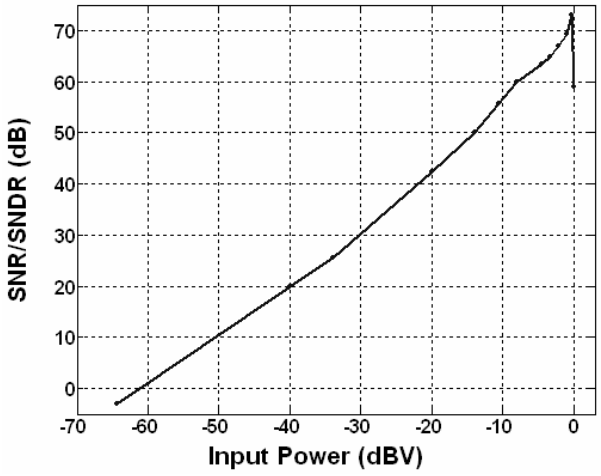
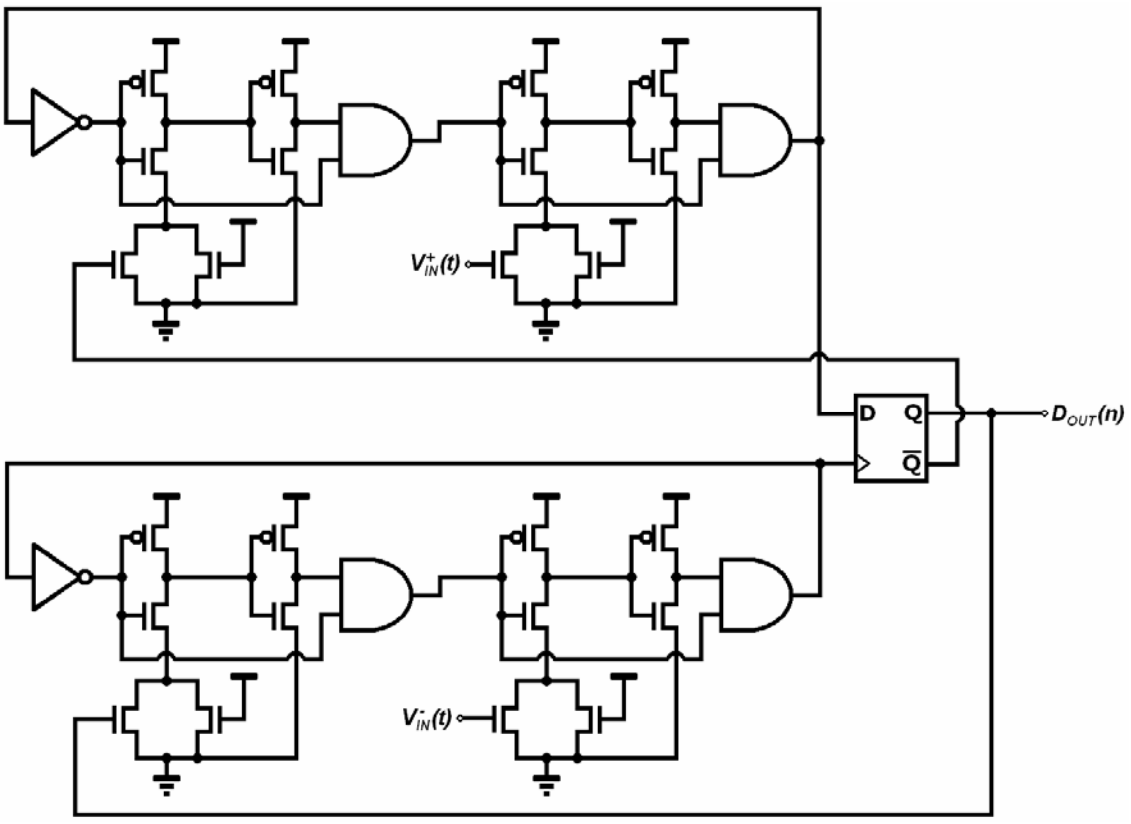
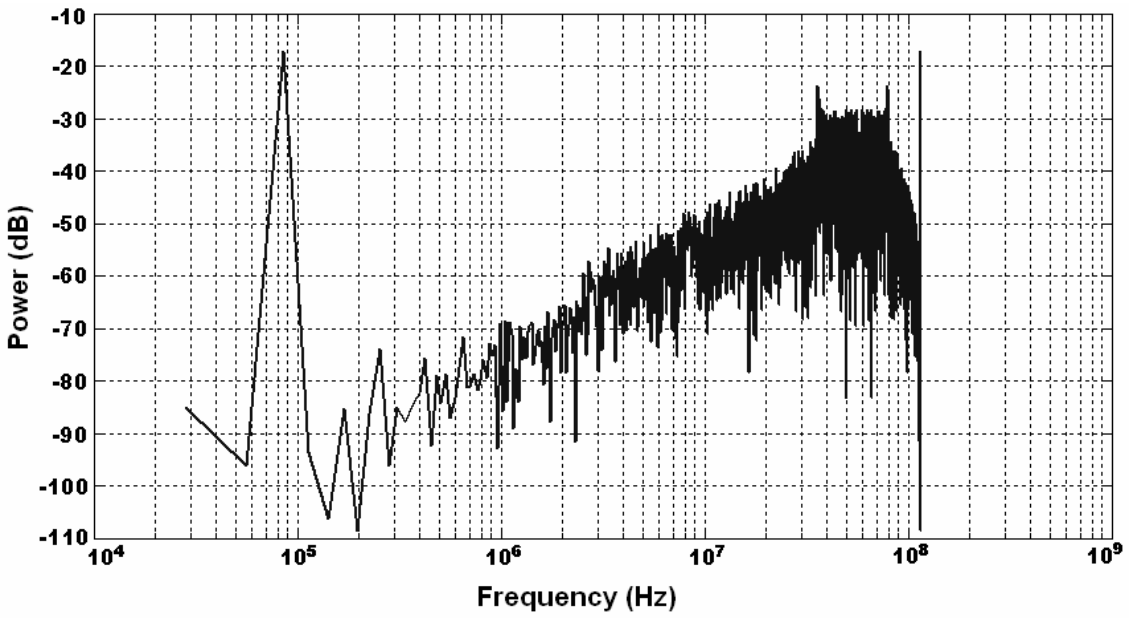


(c)

Figure 6.9: Mathematical modeling of the differential-input TMΔΣADC: (a) MATLAB Simulink model diagram; (b) MATLAB simulation PSD results, (c) dynamic range.



(a)



(b)

Figure 6.10: Differential-input first-order single-bit TMΔΣADC (a) transistor schematic; (b) PSD HSPICE simulation result.

The transistor design of Figure 6.10(a) was simulated with HSPICE and an example PSD results is presented in Figure 6.10(b). The oscillators were sampling at 116 MHz while being biased with the input voltage DC offsets set at 1 V. The SNR extracted within an 85 kHz bandwidth (i.e. OSR of 682) was 65 dB. The SNDR extracted within a 255 kHz bandwidth (i.e. OSR of 228) was 56 dB. It may be observed that the second harmonic is significantly suppressed due to the differential nature of the design.

6.5 - Higher-Order TMΔΣADCs

The construction of higher-order delta-sigma modulators using TMSP is not an easy task. It was discussed in Chapter 3 that the summation of two time-mode variables cannot be done directly without first converting them into physical intermediate variables. Since this opposes the advantages of TMSP, higher-order modulators will not be explored further.

6.6 - Multi-Bit TMΔΣADCs

A multi-bit TMΔΣADC design may be implemented by replacing the time comparator with a TDC and adding a DAC in the feedback path of the single-bit design described in Section 6.1. The complete multi-bit TMΔΣADC design is presented in Figure 6.11.

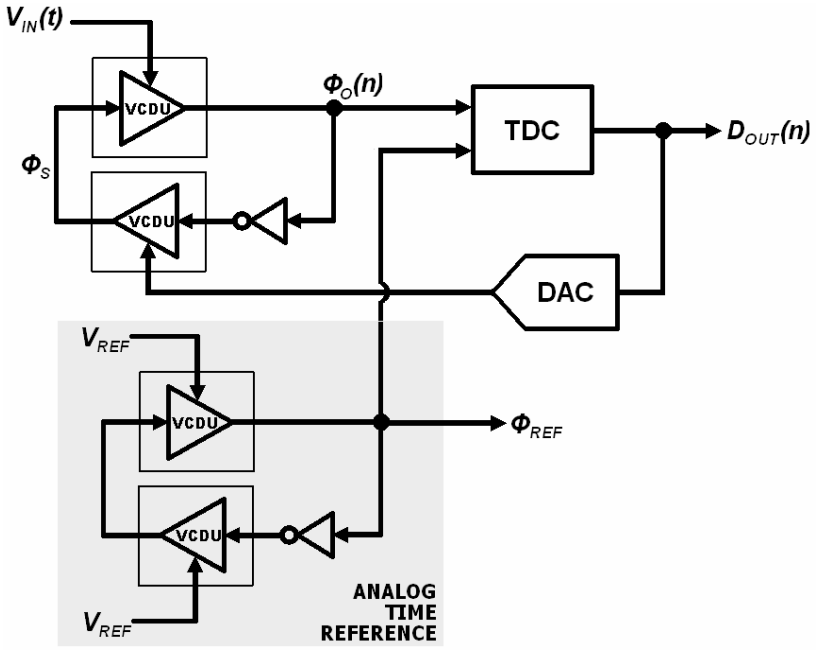
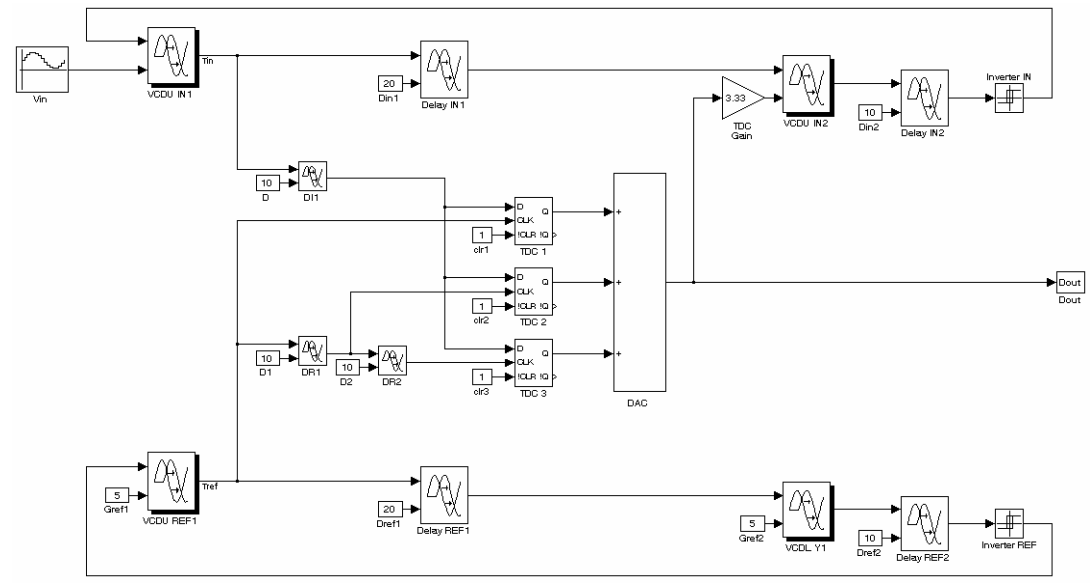


Figure 6.11: First-order multi-bit TMΔΣADC.

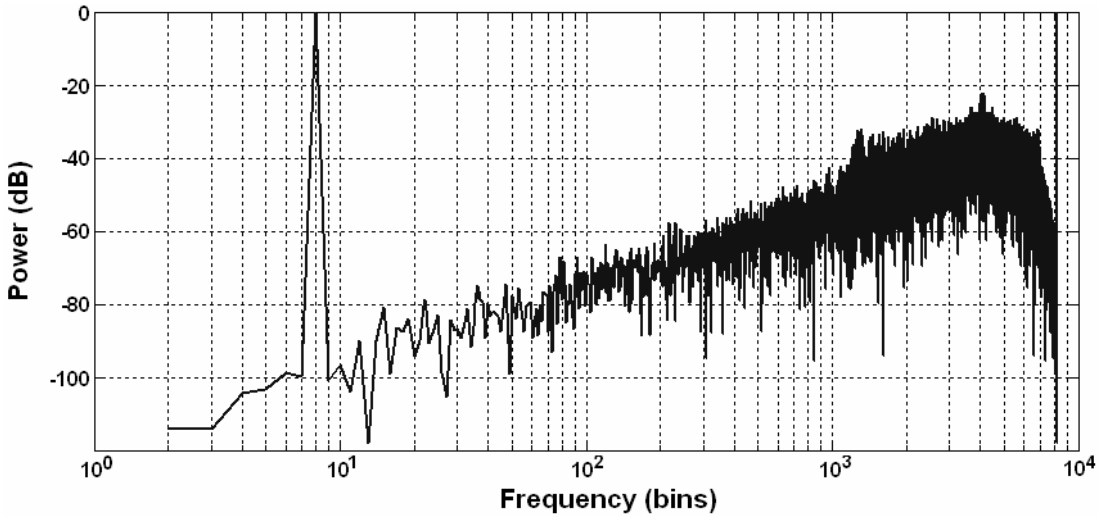
All the same implementation issues for the single-bit ADC described in Section 6.2 will apply to this design. However, the linearity of the TDC and DAC may become an issue.

A first-order 2-bit TMΔΣADC was modeled and simulated using MATLAB. The Simulink block diagram is illustrated in Figure 6.12(a). The D flip-flop that was used as a time-comparator is replaced by a simple three-stage delay-line TDC. A summation block, acting as the DAC, adds the TDC outputs to produce an analog output. The PSD of the system output is shown in Figure 6.12(b).

The output SNR results for OSRs of 585 and 195 are 94 and 76 dB, respectively. It may be observed that for the same input conditions as the single-bit design in Figure 6.4 the SNR output of the 2-bit design is 6 dB better. This result is expected when increasing the number of output bits by one.



(a)



(b)

Figure 6.12: Mathematical modeling of the first-order 2-bit TMΔΣADC: (a) MATLAB Simulink model diagram; (b) MATLAB simulation PSD result.

6.7 - Single-Ended Input IC Prototype and Experimental Results

6.7.1. Integrated Circuit Implementation and Experimental Setup

The single-ended input TMΔΣADC was implemented in a 1.8-V, 0.18-μm, single-poly, six-metal CMOS process. A microphotograph of the test die is shown in Figure 6.13(a). Two designs were fabricated on the same die running at different sampling frequencies: 10-MHz and 150-MHz. The 10-MHz design occupies an area of 0.0115 mm^2, while the 150-MHz TMΔΣADC has the dimensions of 15-μm x 25-μm which is an area of 0.000375 mm^2. The only difference between the two designs are the capacitors used to slow down the oscillations. Along with the ADC output bit $D_{OUT}(n)$ and reference clock ϕ_{REF}, several other internal test nodes were routed to output pins to aid in observability and debugging.

The IC was mounted on a custom two-layer PCB and was fastened with a custom-made IC clamp, as shown in Figure 6.13(b). Signals were routed from the IC to BNC connectors in order to interface the test equipment. The reference voltages were generated using voltage division through potentiometers. A voltage regulator and decoupling capacitors were incorporated on the power supply to aid in noise reduction.

The test environment consisting of a LeCroy 6000 Serial Data Analyzer (SDA), oscilloscope, signal generator, and dual power supply is demonstrated in Figure 6.13(c). The SDA was employed to capture the TMΔΣADC raw data output along with the reference clock ϕ_{REF}. The digital output data was oversampled and processed in MATLAB and the relevant parameters and test results were extracted.

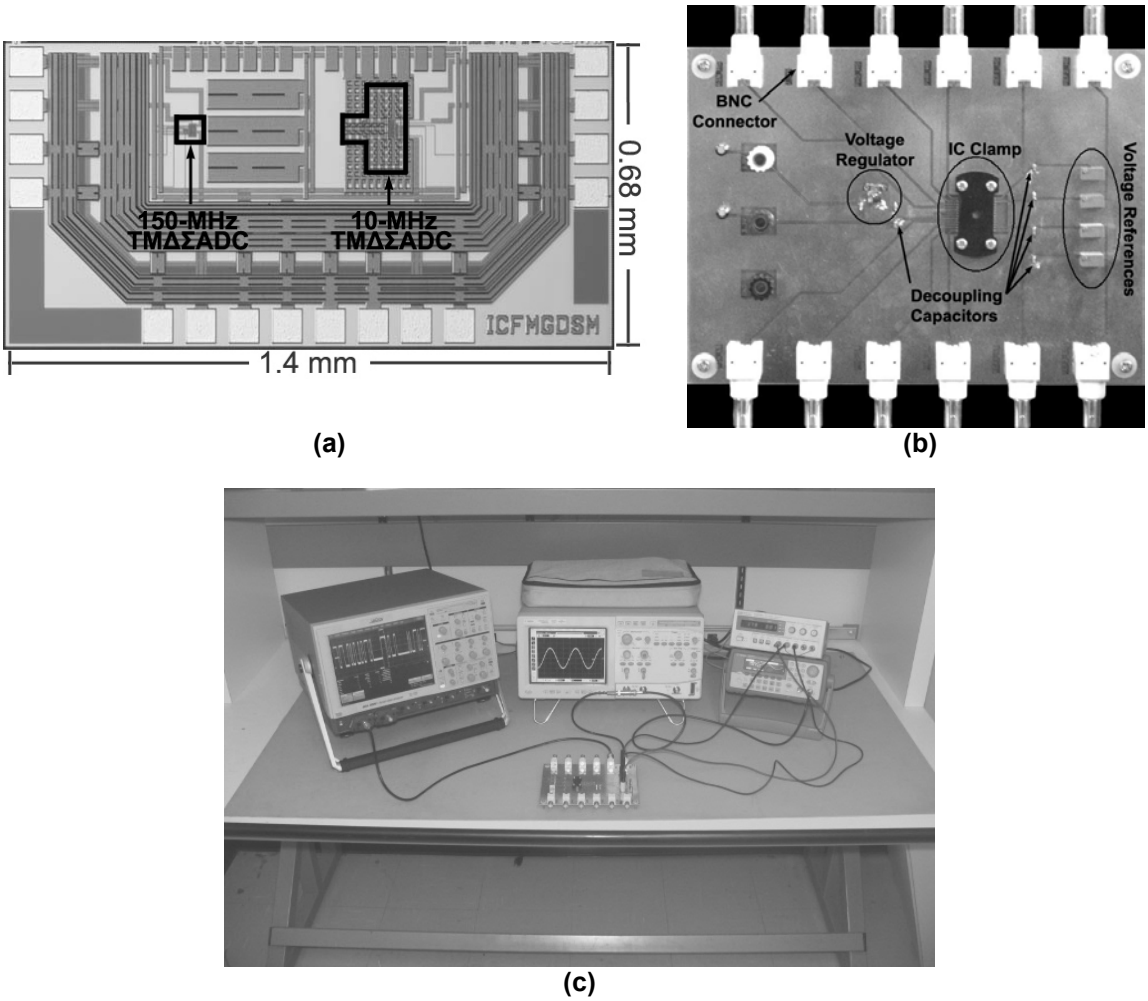
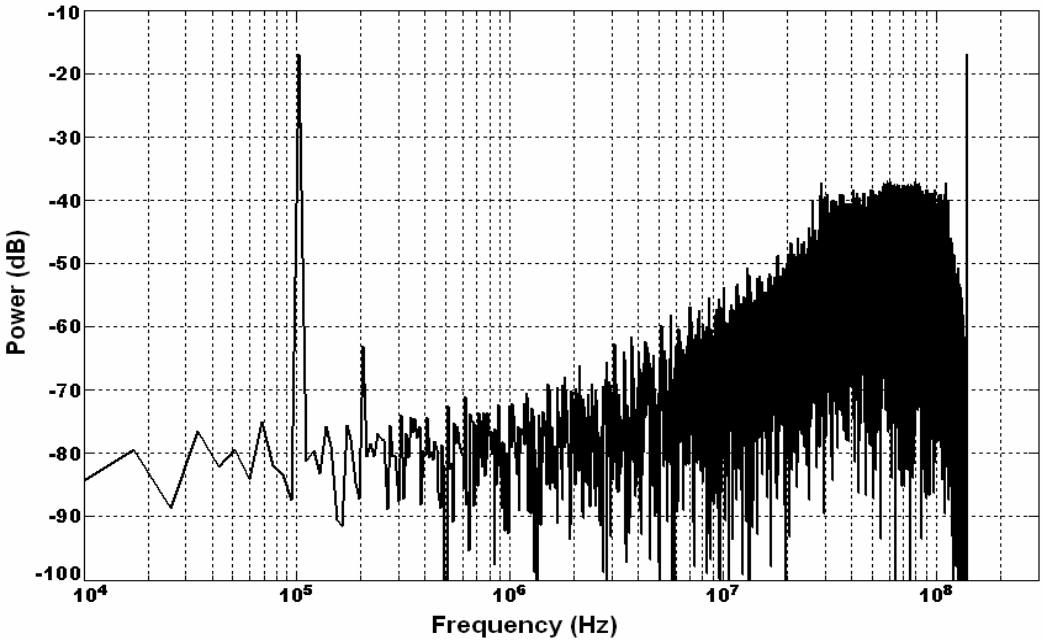


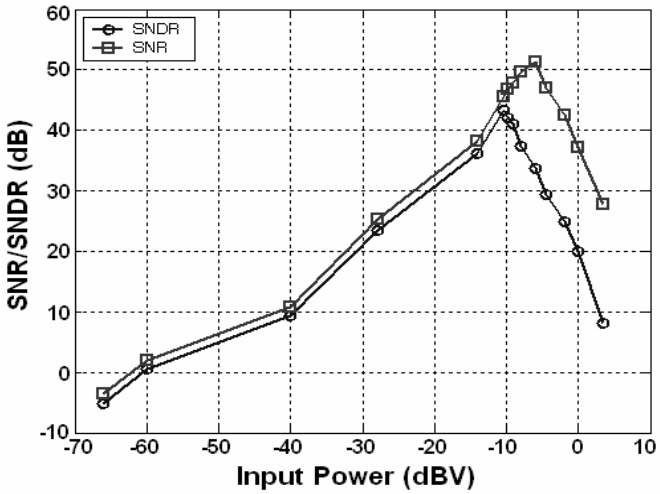
Figure 6.13: (a) Integrated circuit microphotograph of a test chip implementing two single-ended input time-mode delta-sigma ADCs. (b) PCB to interface the test chip to the test equipment. (c) Experimental setup.

6.7.2. High-Speed TMΔΣADC Experimental Results

The analog time reference oscillator was determined to operates at approximately 140-MHz with a reference voltage V_{REF} set at 1-V. The total power dissipation was found to be approximately 475-μW. The modulator was exercised with a 400-mV_{p-p} sinusoid at 100-kHz. 16384 points were collected and the experimental results showing the power spectral density of the modulator's output is presented in Figure 6.14(a). A SNR of 50.3 dB was acquired within a 100-kHz bandwidth and a SNDR of 42.2 dB was achieved within a 400-kHz bandwidth. These bandwidths correspond to over-sampling ratios of 700 and



(a)



(b)

Figure 6.14: Experimental results for the single-ended input high-speed time-mode delta-sigma analog-to-digital converter: (a) power spectral density; (b) dynamic range.

175, respectively. Post-layout HSPICE simulation predicts that the SNR should be 58 dB in a 100-kHz bandwidth, and the SNDR should be 48 dB with a 400-kHz bandwidth.

The input voltage level was swept and the dynamic range plot of Figure 6.14(b) was collected. Both SNDR and SNR were extracted to determine that the

dynamic range of this design is approximately 65 dB. The specifications and experimental results for the high-speed single-ended input design are summarized in Table 6.1.

Table 6.1: Design and experimental result summary for the high-speed single-ending input 1st-order single-bit time-mode delta-sigma ADC.

Technology	0.18-μm CMOS, single-poly, 6 metal
Supply Voltage	1.8 V
Core Area	15-μm x 25-μm
Power Dissipation	475 μW
Sampling Frequency	140 MHz
Output Nyquist Rate	400 kHz
OSR	175
Dynamic Range	65 dB
Peak SNR	51 dB
Peak SNDR	42 dB

6.7.3. Low-Speed TMΔΣADC Experimental Results

The slower 10-MHz TMΔΣADC design was tested using the same experimental setup described in Section 6.7.1. With a 1-V reference the integrators were oscillating at 10.2-MHz. The power dissipation of this circuit was evaluated at approximately 1.7 mW. In order to maintain coherency an input test signal was generated at 4.4 kHz with a 0.4-$V_{p\text{-}p}$ amplitude. 16384 samples of the TMΔΣADC output were acquired and its PSD is displayed in Figure 6.15. Over a 20 kHz bandwidth the best achievable SNR and SNDR from this design was 49 dB and 41.5 dB, respectively. It may be observed that a greater amount of distortion is exhibited from the lower-speed design.

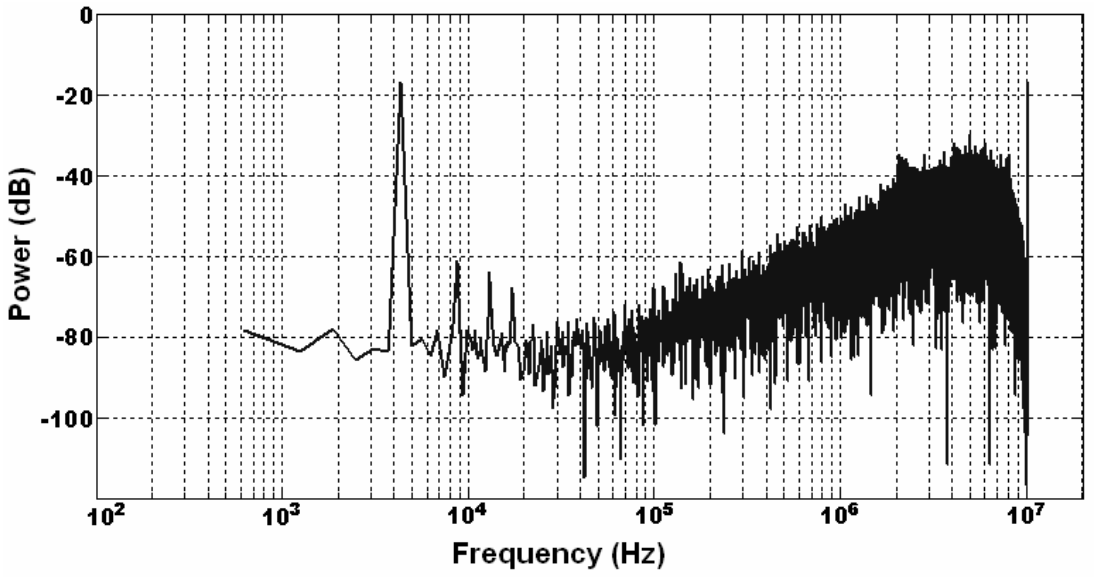


Figure 6.15: PSD experimental results for the single-ended input low-speed time-mode delta-sigma analog-to-digital converter.

Table 6.2: Design and experimental result summary for the low-speed single-ending input 1st-order single-bit time-mode delta-sigma ADC.

Technology	0.18-μm CMOS, single-poly, 6 metal
Supply Voltage	1.8 V
Core Area	0.0115 mm^2
Power Dissipation	1.7 mW
Sampling Frequency	10.2 MHz
Output Nyquist Rate	20 kHz
OSR	255
Peak SNR	49.2 dB
Peak SNDR	41.5 dB

6.8 - Differential-Input IC Prototype and Experimental Results

6.8.1. Integrated Circuit Implementation

The differential-input TMΔΣADC, given in Figure 6.10, was implemented in a 0.18-μm CMOS process. A microphotograph of the test die is shown in Figure 6.16. The complete ADC design occupies an area of 0.00256 mm^2. Each transistor in one time-mode integrator was matched with its equivalent transistor in the other integrator using an interdigitized finger layout technique [15].

A modification that was incorporated in the differential design was a cut-off switch which will shut down the modulator with a digital signal. Figure 5.11 demonstrates the simple CMOS inverter circuit that was be used to stop the modulator from oscillating. It may be implemented anywhere in the oscillator paths. When the digital signal $D_{ON/OFF}$ is low the oscillators will be ceased and when the $D_{ON/OFF}$ is high the oscillators will run. Although it is not required, an

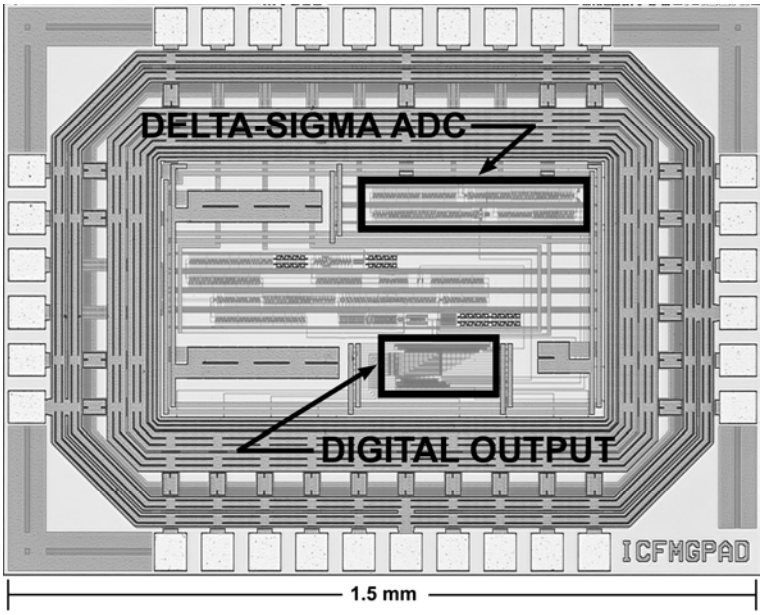


Figure 6.16: Microphotograph of the test chip implementing the differential-input TMΔΣADC.

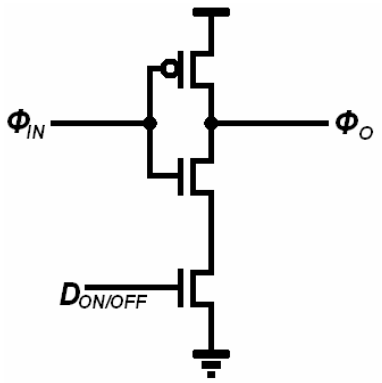


Figure 6.17: Inverter used to turn the TMΔΣADC oscillators on or off.

additional benefit is gained with this cutoff mechanism whereby the signal and reference oscillators will begin their oscillations in phase.

The Teradyne A567 mixed-signal tester can collect digital samples at a maximum rate of 25 MHz and has a limited digital memory depth of 1-million 20-bit words. In order to interface the TMΔΣADC to the tester the nominal output data rate of 116 MHz needed to be slowed down. This was achieved by a serial-to-parallel conversion. In order to maximize the data capture it was decided that the serial data would be converted into byte-sized parallel data. Consequently, this would reduce the output data rate to 14.5 MHz which is adequate for the A567 to capture. It would also permit 8-million bits to be captured, which is much more that is necessary. Figure 6.18 presents the serial-to-parallel digital output circuitry. The TMΔΣADC output D_O is passed into a shift register clocked by the TMΔΣADC time comparator clock signal. The bottom set of flip-flops form a ring counter which produces a data strobe signal every eight clock cycles. The ring counter is reset and started with the *ON/OFF* signal which is also used to turn the TMΔΣADC oscillators on or off. On each rising edge of the data strobe the shift register outputs are latched in parallel to the output registers (i.e. top row of flip-flops). The digital output circuit was also integrated on the test die and the data strobe signal was routed off the chip.

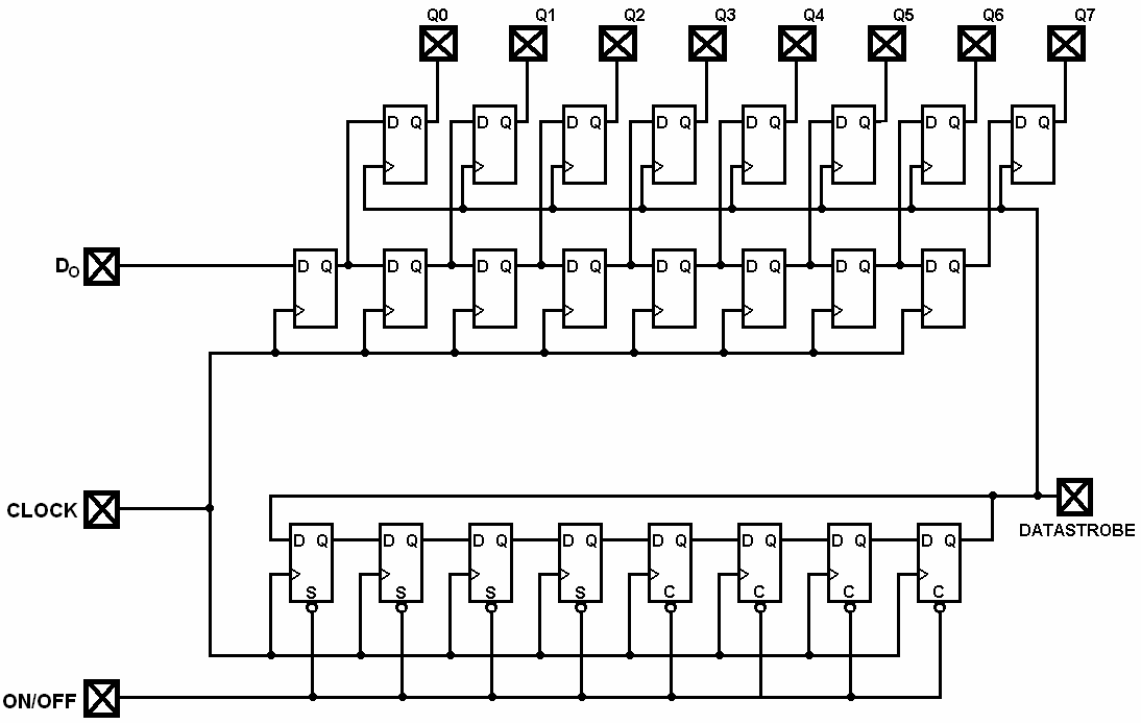


Figure 6.18: Serial-to-parallel digital output circuitry for the differential-input time-mode delta-sigma ADC.

6.8.2. Experimental Results

The differential-input TMΔΣADC was tested using a Teradyne A567 mixed-signal tester. A custom made PCB was manufactured to interface the test chip to the tester. The PCB is a 4-layer board incorporating two layers for digital and analog ground and a split plane for I/O power (3.3 V) and core power (1.8 V). The top layer is used for signaling. Both power supplies are regulated and many decoupling capacitors were included on all power supply pins to help minimize noise. A photograph of the PCB and test environment is illustrated in Figure 6.19. The modulator was dynamically stimulated with a 0.4 $V_{p\text{-}p}$ sine wave biased at 1-V which was generated by the precision low-frequency source offered by the ATE. It was determined from the data strobe signal that the modulator was oscillating at 87.2 MHz. In order to maintain coherency the test signal frequency was set to 24 kHz. 65536 data samples were collected and an example PSD plot of the ADC output is presented in Figure 6.20(a). Over a signal bandwidth of 125

(a) (b)

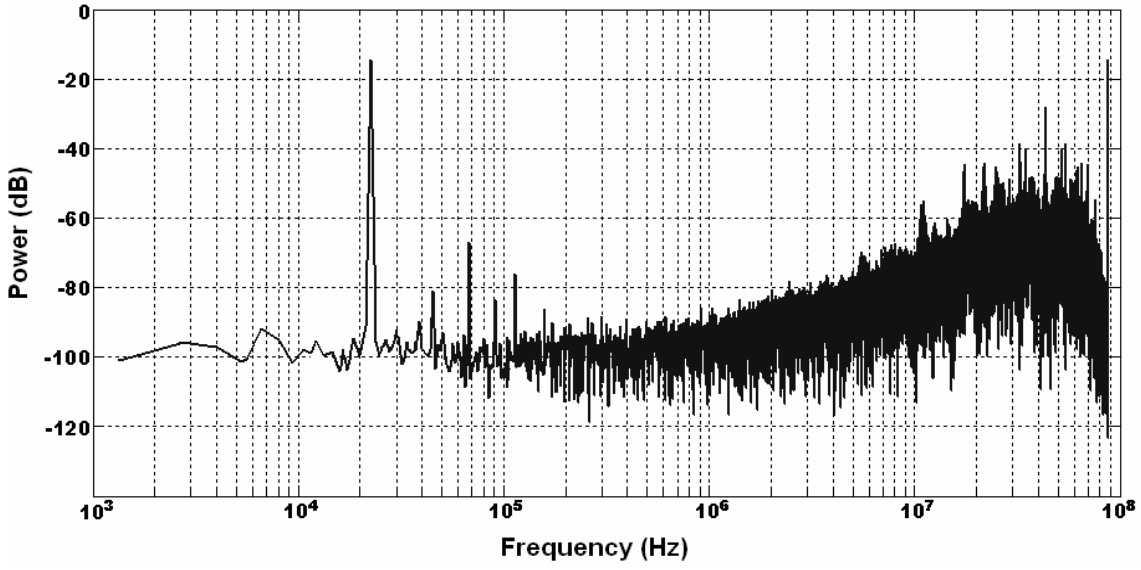
Figure 6.19: Experimental setup: (a) PCB used to interface the test chip to the Teradyne A567 tester. (b) Test environment with the IC, PCB, and A567 tester.

kHz the SNR and SNDR was determined to be 62.7 dB and 54.2 dB, respectively. It may be seen from the ADC's output spectrum that the even-order harmonics have been suppressed.

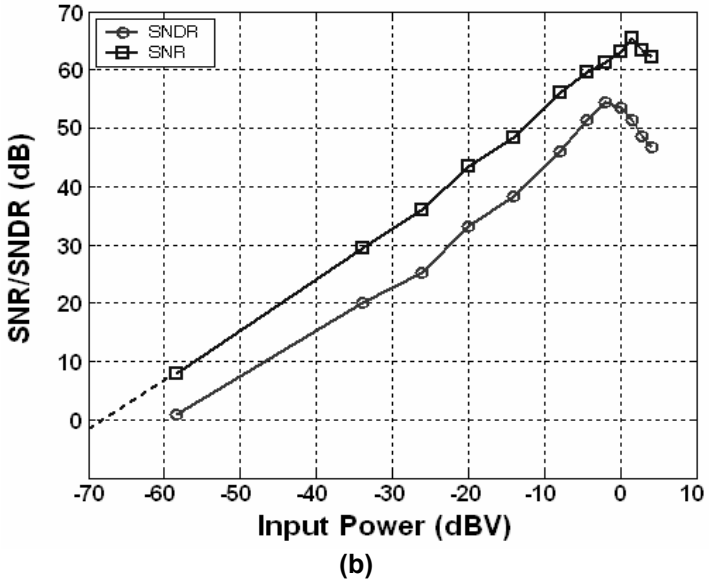
Table 6.3: Design and experimental result summary for the differential-input 1st-order single-bit time-mode delta-sigma ADC.

Technology	0.18-μm CMOS, single-poly, 6 metal
Supply Voltage	1.8 V
Core Area	2560 μm^2
Power Dissipation	780 μW
Sampling Frequency	87.2 MHz
Output Nyquist Rate	125 kHz
OSR	348
Dynamic Range	63 dB
Peak SNR	65 dB
Peak SNDR	54 dB

The input dynamic range was determined by incrementing the input signal amplitude while capturing the resulting SNR and SNDR data. Figure 6.20(b) presents the dynamic range data revealing that maximum achievable SNR and SNDR for this design is 65 dB and 54 dB, respectively. The input dynamic range for this design is approximately 63 dB. The design and experimental performance are summarized in Table 6.3.



(a)



(b)

Figure 6.20: Experimental results for the differential-input first-order single-bit TMΔΣADC: (a) PSD of the ADC output. (b) Dynamic range.

6.9 - Comparisons and Discussion

Three TMΔΣADC designs were fabricated in two separate ICs. Two of the designs are single-ended input ADCs while the third has differential inputs. These designs will be compared to each other and to their simulations results in the following subsections.

6.9.1. Single-Ended Input Design: High-Speed versus Low Speed Comparison

When comparing the high-speed and low-speed single-ended input designs, it is noted that the slower modulator exhibits significantly more distortion. This may be explained by the VCDU's conversion time dependency on the input voltage amplitude, as discussed in Chapter 3. Hence, designing the VCDU's with a small voltage-to-time conversion factor G_ϕ will minimize distortion. Consequently, it would also allow the modulators oscillate faster. However, a reduction of G_ϕ will decrease the time comparator's ability to accurately resolve the resulting small time-difference variables.

The power dissipated by the TMΔΣADCs is mainly dynamic thus governed by the equation

$$P_D = fCV_{DD}^2. \tag{6.14}$$

It was noted that the lower speed circuit consumed significantly more power than the high-speed design. This may be explained by observing the difference between the nodal capacitance and frequencies of the low and high speed modulators. The low-speed design has a total nodal capacitance 20 – 50 times greater than the high-speed design. It also operates 14 times slower. Since the capacitance increase is greater than the reducing factor of frequency, it stands to reason that the dynamic power will increase. On a final note, the lower speed design occupies a much greater area than the high speed design.

6.9.2. Single-Ended Input Design: MATLAB Model versus HSPICE Transistor Simulations

The generalized SNR performance in the MATLAB simulations will always be better as large-scale input signals may be used whereas transistor designs are limited by linearity regions and supply voltages. It may be observed from the simulation results that distortion is present in the HSPICE transistor simulations but not in the MATLAB simulation. The cause of this distortion is due to the VCDU non-linearity and the distortion caused by the VCDU's non-linear sampling action. Note that both the MATLAB and HSPICE simulations experience the non-uniform sampling phenomena.

6.9.3. Single-Ended Input Design: HSPICE Transistor Simulations versus Experimental Results

The error between simulation and experimental results may be explained by noise and mismatch. The SNR and SNDR determined through simulation are based solely on quantization noise and the distortion caused by the nonlinearity of the VCDUs. However, the experimental results are subjected to all other noise sources (e.g. power supply noise, clock jitter, and crosstalk), and circuit mismatches which result in other distortion mechanisms.

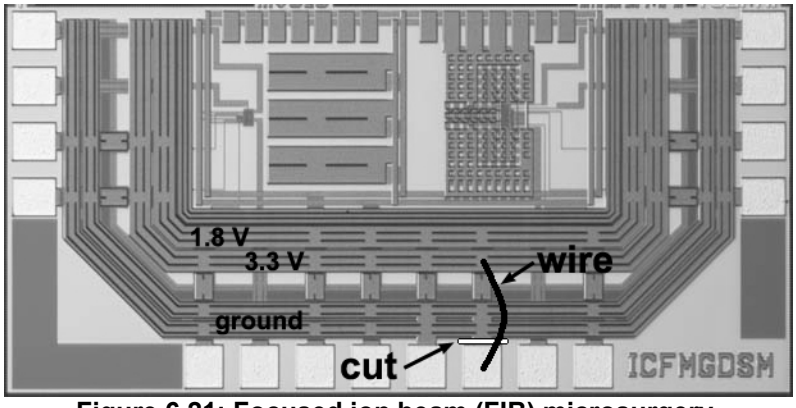


Figure 6.21: Focused ion beam (FIB) microsurgery.

The test chip that implemented the single-ended TMΔΣADCs was originally fabricated with a catastrophic design flaw. The CMOS process used for the implementation requires two supply voltages. A 1.8 V source is needed to supply power to the core circuit elements. A 3.3 V supply is used to power the input and output digital buffers. Each supply and respective ground is applied to the IC through their own pad. The IC was designed with a fault such that the 3.3 V supply pad was accidentally exchanged for a ground pad leaving no 3.3 V supply to power the digital output buffers. A focused ion beam (FIB) microsurgery [44] was performed on the IC to correct this problem. As shown in Figure 6.21, the ground bonding pad was severed from the routing wires using gas assisted etching. FIB vias were created on the bonding pad and the 3.3 V supply ring. A tungsten wire was deposited to join the bonding pad to the 3.3 V ring.

It is suspected that the IC design suffers from two power supply related problems. There is only one power and one ground pin for each supply. This may not be sufficient considering that there are six digital pads constantly switching. Moreover, the 3.3 V supply is being delivered through the wire created by the FIB which is highly inductive. The high-speed TMΔΣADC was designed to oscillate at 150 MHz, however, experimentally it could only achieve 140 MHz. This supports the suspicion as circuits will slow down if insufficient power is delivered.

6.9.4. Single-Ended versus Differential-Input Design

The differential-input TMΔΣADC is experimentally superior to the single-ended design. It was demonstrated that the differential design suppressed the even-order harmonic distortion. Several improvements were implemented in the differential design which may have enhanced its performance. However, the measurements from the single-ended circuits may have been corrupted by the insufficient power supplied to the chip.

6.9.5. TMΔΣADCs versus other Designs

The single-ended input and differential TMΔΣADCs presented in this chapter may be compared to many other state-of-the-art designs published in the literature. Figure 6.22 presents three graphs which compare the TMΔΣADCs with many other low-pass delta-sigma ADC designs recorded in [45] – [76]. One of the greatest advantages of the TMΔΣADC is the incredibly small area that these designs occupy. Figure 6.22(a) presents a comparison of peak SNDR performance versus area usage. It may be observed that the area requirement of the TMΔΣADCs is between two and five orders of magnitude less that all other reported designs. Figure 6.22(b) offers a comparison of power consumption plotted against SNDR. Again, it may be noted that the power requirement of the TMΔΣADCs is far less than most published results. A third graph of SNDR versus input signal bandwidth is offered in Figure 6.22(c) since all these designs record their performance at different input signal conditions. As shown in the figure, the TMΔΣADC designs demonstrate mediocre data conversion speeds. It should be noted that most of the published works are delta-sigma designs of higher-order (i.e. 2^{nd} – 6^{th}-order) and operate with multi-bit quantizers (i.e. 3 – 4-bit). As such, their performance is enhanced while sacrificing area and power. The TMΔΣADC experiences lower SNDR for several reasons. Primarily, the architecture is necessarily a first-order design which increases the quantization noise over all other designs. Moreover, the TMΔΣADCs were constructed with single-bit quantizers unlike most of the published works. It was demonstrated in Section 6.6 that augmenting the TMΔΣADC to a multibit design would increase its SQNR. Finally, the linearity of the front-end voltage-to-time converter is a large contributor to the distortion component of the SNDR. Therefore, improving the linearity of the VTC is crucial to increase the overall SNDR performance of the TMΔΣADC.

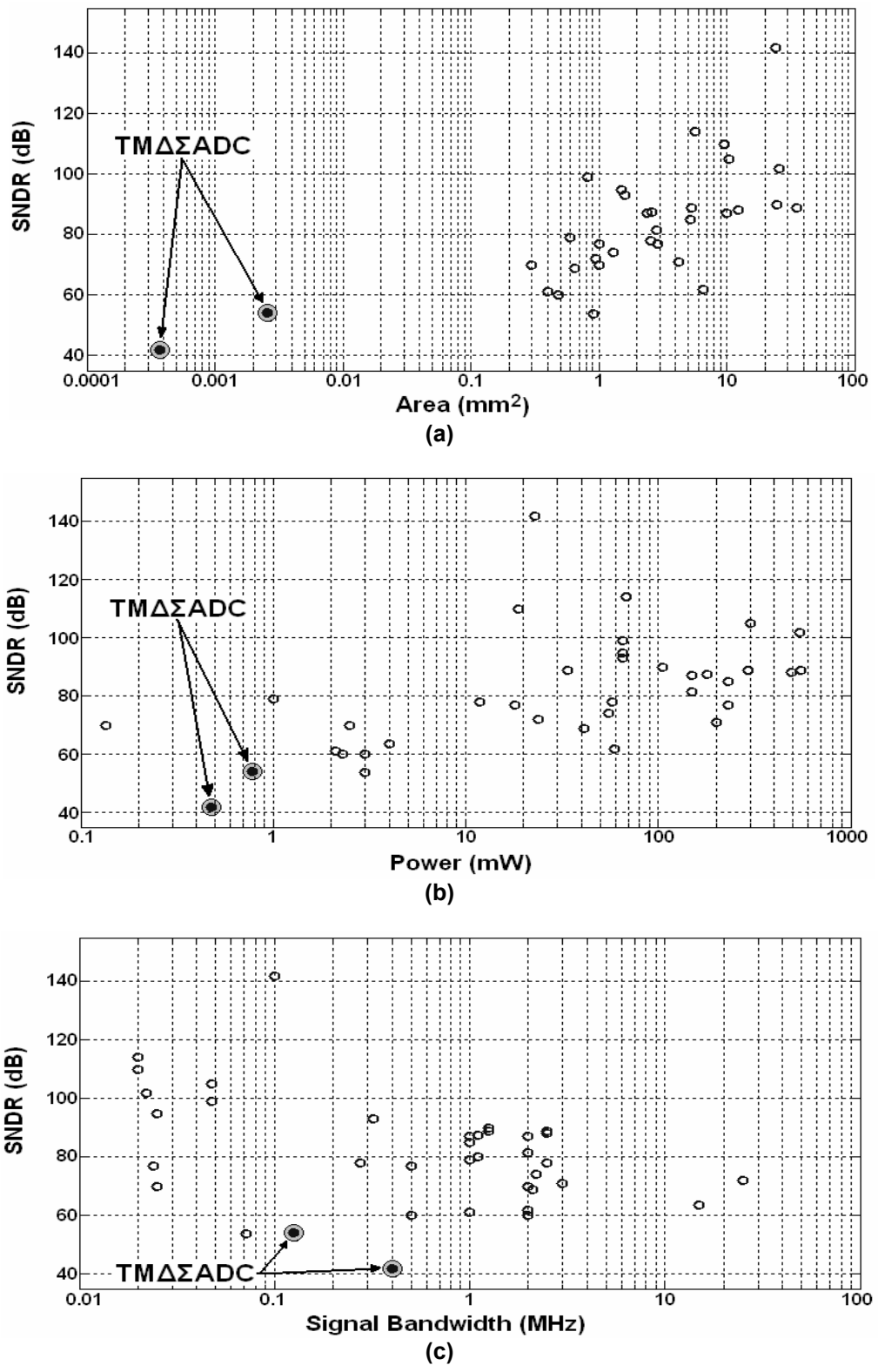


Figure 6.22: Comparison between TMΔΣADC designs and state-of-the-art designs recorded in the literature: (a) SNDR versus area, (b) SNDR versus power, (c) SNDR versus signal bandwidth.

6.10 - Conclusion

This chapter fully explored the design of ΔΣ ADCs utilizing the TMSP components described in Chapter 3. It was demonstrated that a first-order single-bit modulator could be designed from four VCDUs, a D-type flip-flop, and some digital inverters. Proof-of-concepts for single-ended input, differential-input, and multi-bit designs were offered through MATLAB simulations. The feasibility of there implementations were justified by transistor level simulations. Two IC were fabricated incorporating three TMΔΣADC designs, two of which are single-ended input designs and one is a differential-input design. The experimental results demonstrated that delta-sigma converters, offering 7 to 9-bits of effective resolution, may be constructed using the TMSP philosophy. These designs were shown to occupy very small silicon areas (372-μm^2 and 2560-μm^2) while consuming less than milliwatts of power.

Distortion was observed in all three designs. This was explained by the nonlinearity of the VTC's transfer characteristic and the nonlinear sampling mechanism of the VCDUs. A sample-and-hold circuit could be implemented to remove the latter distortion contribution.

The methodology proposed in this chapter offers a potential for ultra high speed (i.e. gigahertz range) delta-sigma A/D conversion which occupies incredibly small silicon area while consuming very low power. The operating speeds of these designs were not pushed to their upper limits. In order to achieve maximum speed, the TMΔΣADC circuits may be modified by reducing the VCDU's voltage-to-time gain, minimizing nodal capacitance, and reducing inverter delays through transistor sizing.

Chapter 7: Time-Mode Pipeline and Cyclic ADC

Pipeline ADCs are perhaps the most popular data conversion strategy. They offer the best all-around performance with good resolutions (e.g. 8 – 16-bits), fast data conversion (e.g. 1 MHz – 100 MHz) and low power operation. This chapter introduces the pipeline ADC design using the TMSP blocks described in Chapter 3. An IC prototype was fabricated and its design, implementation, and test results are also presented in this chapter.

7.1 - Pipeline Stages and Cyclic ADC

7.1.1. Pipeline ADC

The pipeline ADC was introduced in Chapter 2. Figure 7.1(a) shows a high level block diagram of a time-mode pipeline ADC with M stages. The input voltage V_{IN} is transformed into a time-difference variable ϕ_{IN} using a VTC. Each pipeline stage, depicted in Figure 7.1(b), accepts a time-difference variable input, and converts it into digital output data D_{OUT} using a TDC. The digital data is transformed back into a voltage using a DAC. Using a voltage-to-time adder, the DAC output voltage is subtracted from the input time-difference variable which is delayed through digital buffers so that the TDC and DAC are given sufficient time to complete their processing. The output of the voltage-to-time adder is scaled by

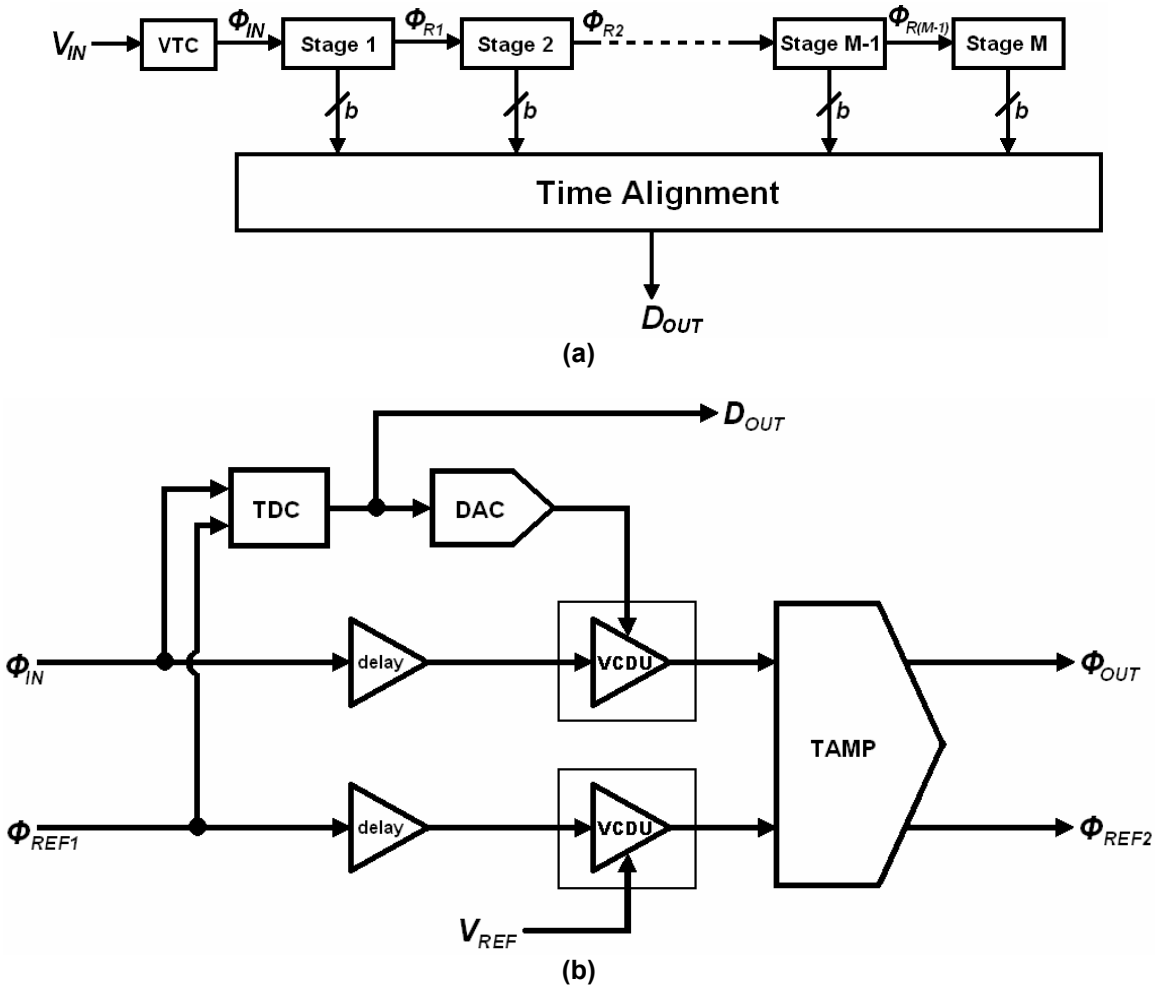


Figure 7.1: Time-mode pipeline ADC: (a) high-level block diagram of the complete ADC system, (b) single pipeline stage.

a time amplifier to produce the residue time-difference which is passed to the next pipeline stage.

The simplest and very common pipeline ADC, known as a radix-2 architecture, uses a single-bit-per-stage design methodology where a 1-bit quantizer (i.e. TDC) is used. This necessitates the use of a 1-bit DAC and a TAMP with a gain of two. Figure 7.2 demonstrates a radix-2 stage designed for a time-mode pipeline ADC. Note that the 1-bit TDC has been replaced with a time-comparator (i.e. a D-type flip-flop).

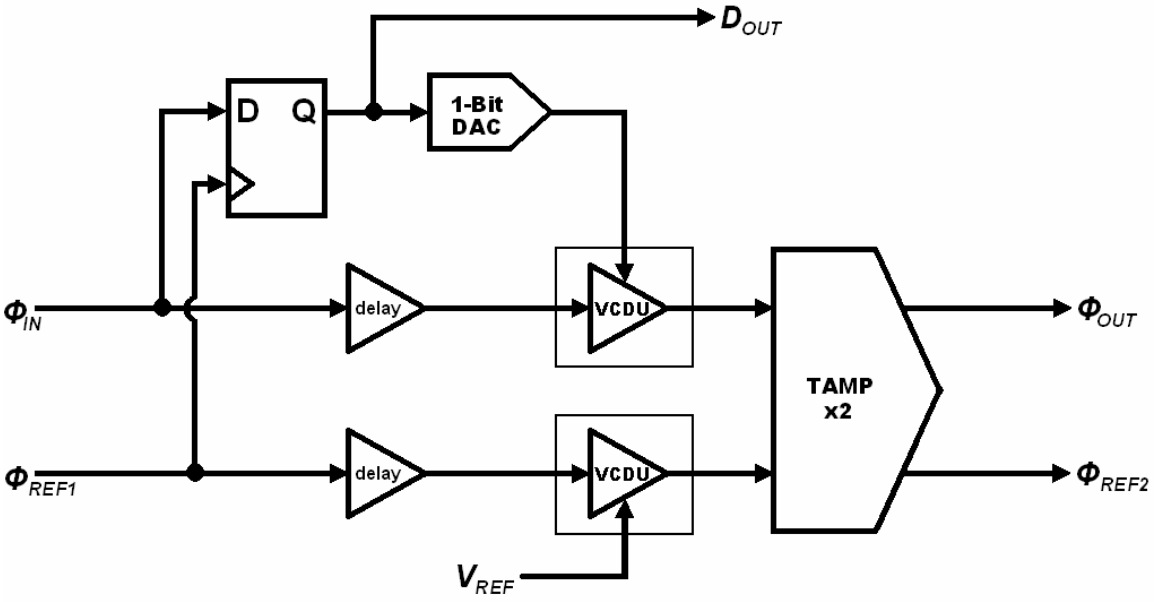


Figure 7.2: Single-bit stage for a radix-2 time-mode pipeline ADC.

7.1.2. Cyclic or Algorithmic ADC

The cyclic or algorithmic ADC was described in Chapter 2 where it was demonstrated that a single pipeline stage may be configured by feeding back the output residue to the input thus reusing the same stage. The advantages of this conversion architecture over the pipeline ADC are a reduction in power consumption and silicon area usage, and fewer components to calibrate. However, the processing speed of a cyclic design will be significantly less as pipelining cannot be performed.

The single-bit pipeline stage presented in Figure 7.2 may be transformed into a cyclic converter, as shown in Figure 7.3. A VTC is used to convert the input voltage V_{IN} into a time-difference variable ϕ_{IN} which is measured with respect to a reference time ϕ_{REF}. When the clock signal ϕ_{CLK} is low, the VTC output is also in a logic low state. Hence, the AND gate outputs are at logic 0 which forces the TAMP outputs to logic 1 through the inverters. Therefore, the circuit is in reset when ϕ_{CLK} is low. When ϕ_{CLK} transitions from low-to-high, the input voltage is sampled and the VTC's output rising edge initiates the A/D conversion process.

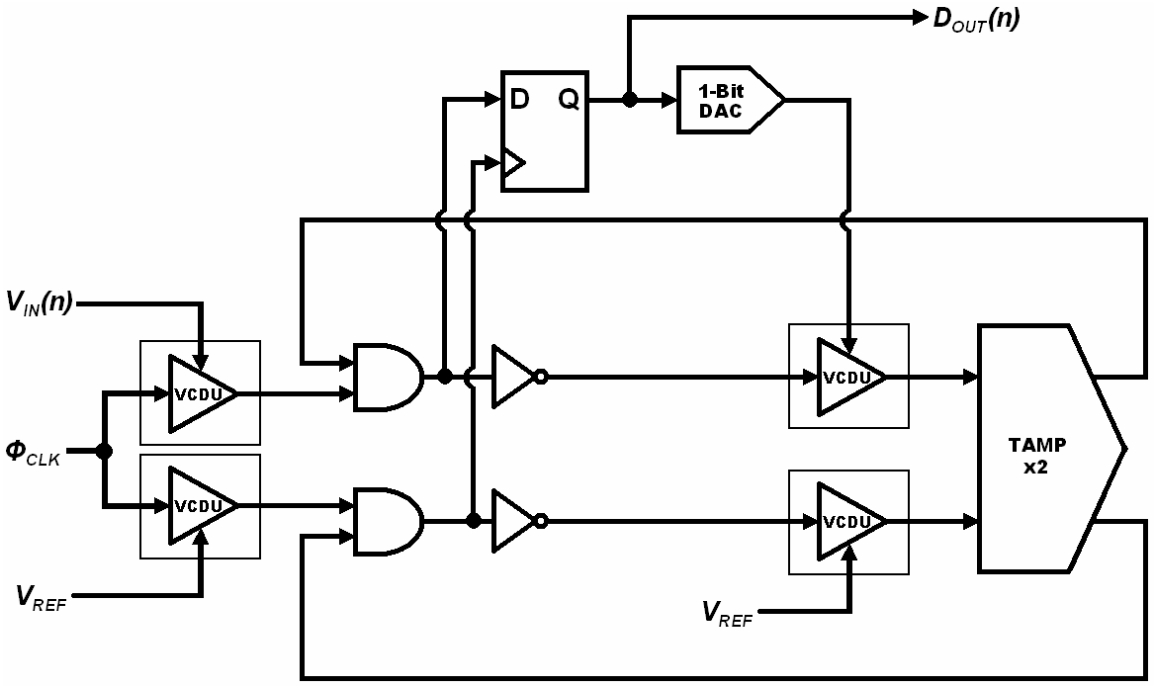


Figure 7.3: Time-mode cyclic ADC.

First, the AND gate outputs switch high and the time-comparator produces its first digital output. The digital output bit is transform back into a voltage using a 1-bit DAC. Meanwhile the voltage-to-time adder and TAMP are being reset thus permitting the flip-flop and DAC circuits to complete their processing. Once the TAMP output is reset its logic 0 output propagates through the AND gate. After passing through the inverter, the DAC output will be subtracted from the time-difference variable and then scaled by a factor of two by the TAMP. The TAMP output, which represents the residue, cycled back to the input to be processed again. This process will continue until the clock signal is brought back to its logic low state.

7.2 - Integrated Circuit Prototype and Implementation

The time-mode cyclic ADC was fabricated in a standard 0.18-um CMOS technology. A photograph of the die is given in Figure 7.4. The total silicon area occupied by the ADC is 0.013 mm^2. The implementation of each subcomponent is described in the following subsections. Note that the transistor dimensions of each component are offered in Appendix A.

7.2.1. Voltage-to-time Converters

Two VTCs were needed to implement the time-mode cyclic ADC and their designs should be identical. They were implemented using the current-starved inverter VCDUs described in Chapter 3 with a voltage-to-time gain factor of 320 ps/V. Matching of these components was done using an interdigitized finger layout strategy [15].

7.2.2. Time Amplifier

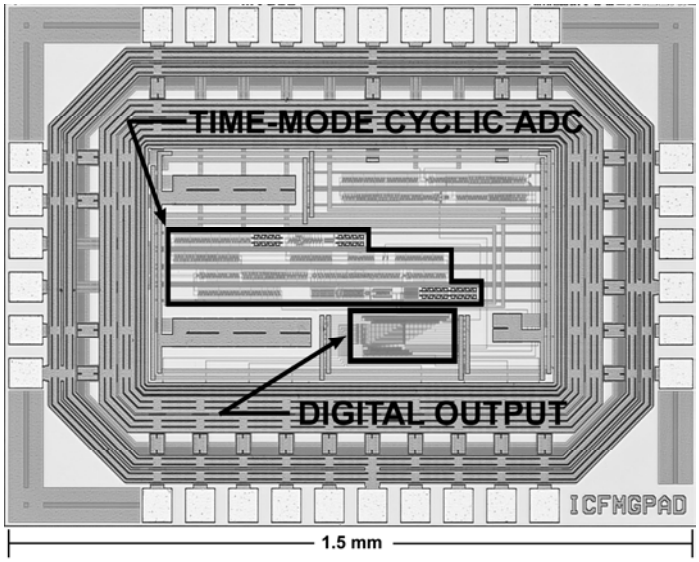
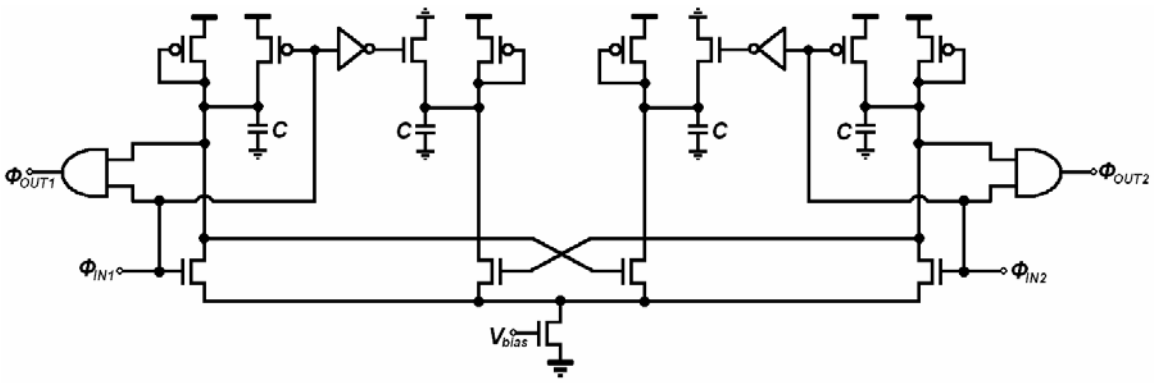
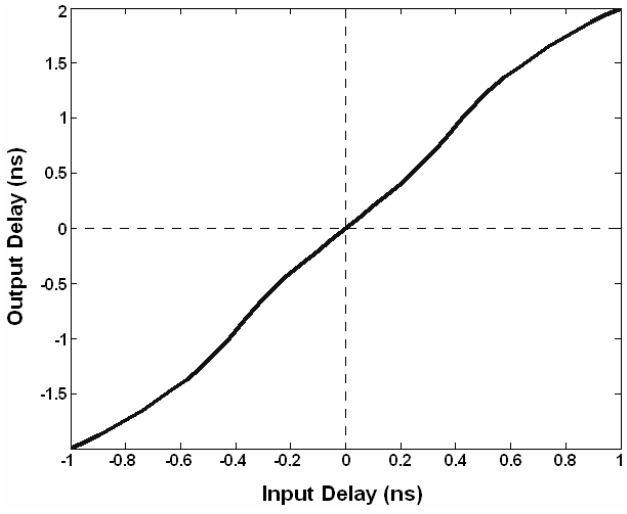


Figure 7.4: Microphotograph of the test chip implementing the time-mode cyclic ADC.

Implementations for a time amplifier were introduced in Chapter 3. The cyclic ADC with a 1-bit quantizer requires an amplifier with a gain of two. It was discovered that a gain of two was difficult to obtain using the TAMP design described in [29] (i.e. Figure 3.14(a)). Therefore, a simple modification was made whereby the source nodes of all the differential-pair transistors were shorted together, as shown in Figure 7.5(a). Although the transfer characteristic of the modified TAMP, displayed in Figure 7.5(b), differs from Figure 3.14(b), a gain of two is achievable. A critical problem with any TAMP design is that the gain varies with input time difference. For example, using the TAMP design in Figure 7.5(a), the gain variation is ±0.8% for input time differences below 200 ps. This will pose



(a)



(b)

Figure 7.5: Time-amplifier (TAMP) with a fixed gain of 2: (a) CMOS transistor schematic; (b) transfer characteristic.

a limitation on the overall performance of the time-mode cyclic ADC.

The TAMP circuit is included in the oscillator path. Moreover, the TAMP will process and modify its input time-difference variables during the rising input edges of ϕ_{IN1} and ϕ_{IN2}. However, the TAMP should not modify the input time-difference variables during their falling edges. Therefore, AND gates are incorporated in the TAMP design at the outputs ϕ_{OUT1} and ϕ_{OUT2} to ensure that the TAMP cannot influence the falling edges.

The reset time of the TAMP is relatively slow for the time-mode cyclic ADC design. Additional reset circuitry is included in the TAMP design to increase the reset speed. Specifically, PMOS and NMOS transistors are respectively used to set and reset the differential pair output nodes during the falling input edges.

7.2.3. Digital-to-Analog Converter

The 1-bit DAC with input D_{IN} was implemented using an analog multiplexer which uses two CMOS transmission gates permitting the selection of either a positive or negative reference voltage V_{REF} to be passed to the DAC output V_{OUT}. The transistor circuit is shown in Figure 7.6.

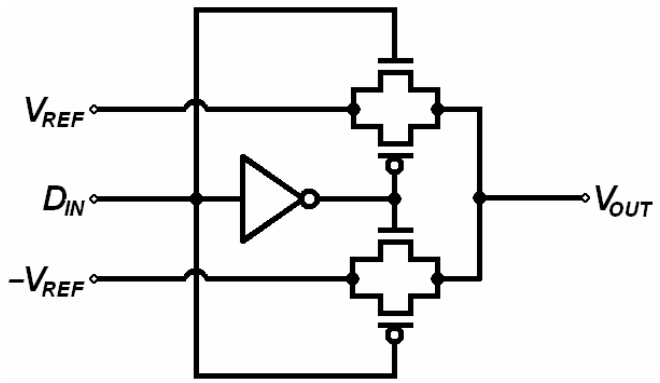


Figure 7.6: CMOS transistor schematic of a one-bit DAC.

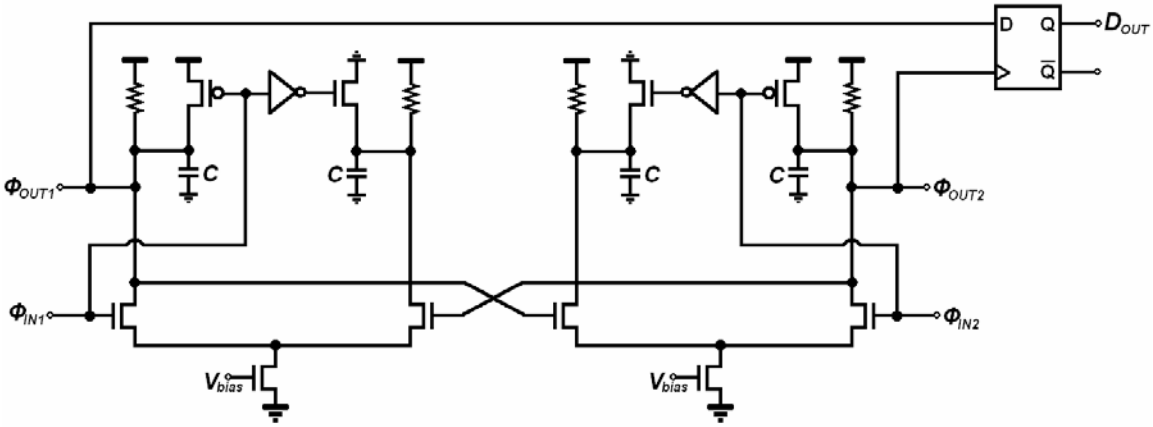


Figure 7.7: Time comparator with preamplifier.

7.2.4. Time Comparator

The time comparator is simply an edge-triggered D-type flip-flop. The metastability of this flip-flop will limit the overall resolution of this design. As such, a time amplifier will precede the flip-flop to relax the metastability constraints. Figure 7.7 demonstrates the complete time comparator design with pre-amplification. The amplifier linearity is irrelevant and it was designed to provide maximum gain. The bias voltage is routed off-chip to permit tuning of the amplifier gain. Reset circuitry is incorporated to ensure that the amplifier can reset within an adequate time. The D-type flip-flop design was taken from a standard cell library.

7.2.5. Digital Output Circuitry

The time-mode cyclic ADC was designed to oscillate at approximately 85 MHz. A Teradyne A567 ATE was selected to test and capture the data from the IC. The A567 can capture digital data at a maximum rate of 25 MHz. Therefore, the serial output data from the ADC was converted into parallel using the circuitry of Figure 7.8. A shift register is used to capture 10-bits of the cyclic output data. A second shift register is used as a counter to provide the data strobe. It is reset by

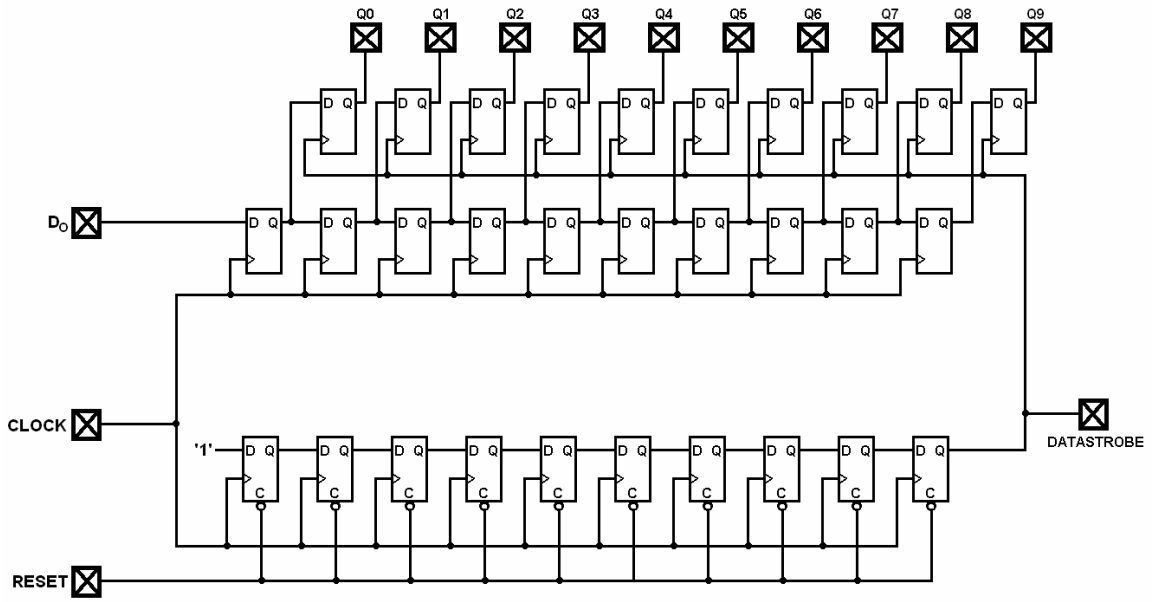


Figure 7.8: Digital output circuitry for the time-mode cyclic ADC.

the sampling clock and shifts a logic ‘1’ ten times for each cycle in a conversion. The 10-bit data is latched by the data strobe into a parallel register which is routed to the output pins.

7.3 - Experimental Results

The IC was mounted on a custom built PCB, shown in Figure 7.9(a), in order to be tested using a Teradyne A567 ATE. A photograph of the test environment is displayed in Figure 7.9(b). The DAC positive and negative reference voltages were set to 0.79 V and 1.21 V and the time comparator bias voltage was set at 0.8 V. In order to determine the TAMP bias that would set its gain at 2 s/s, the circuit was exercised dynamically to determine the optimal THD. It was discovered that a TAMP bias of 0.605 V produced the best results.

To demonstrate the dynamic performance of the time-mode cyclic ADC, it was exercised with a 202-kHz sinusoid with a DC bias of 1-V and a peak-to-peak amplitude of 0.4-V. 8192 points were captured at a sampling frequency of 4-MHz.

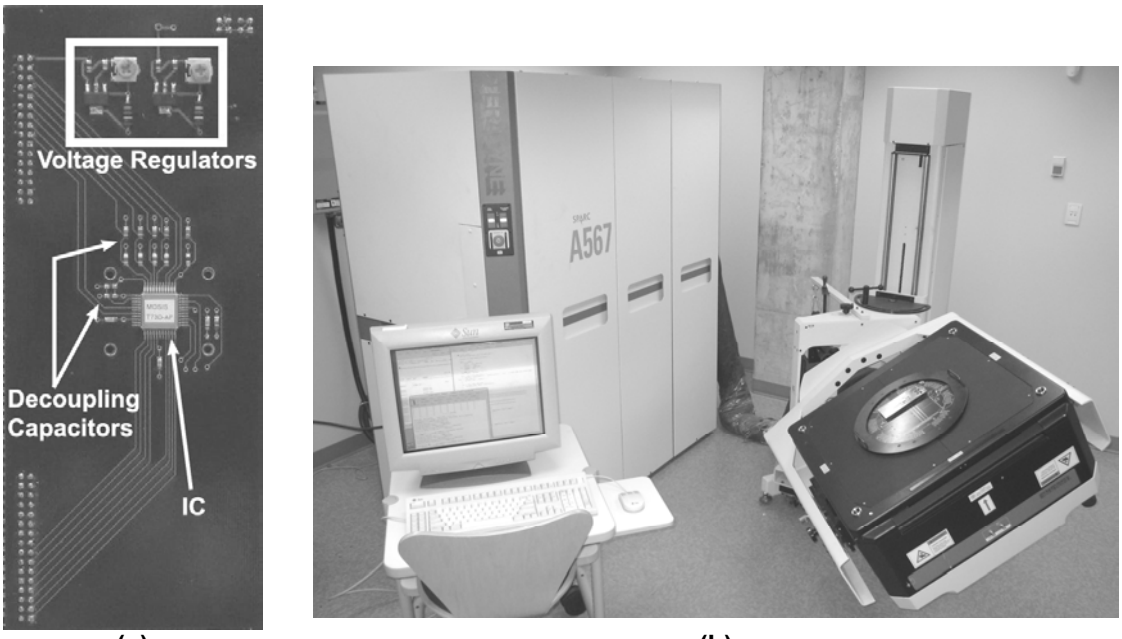


Figure 7.9: (a) PCB used to interface the test chip to the Teradyne A567 tester. (b) Test setup with the IC, PCB, and A567 tester.

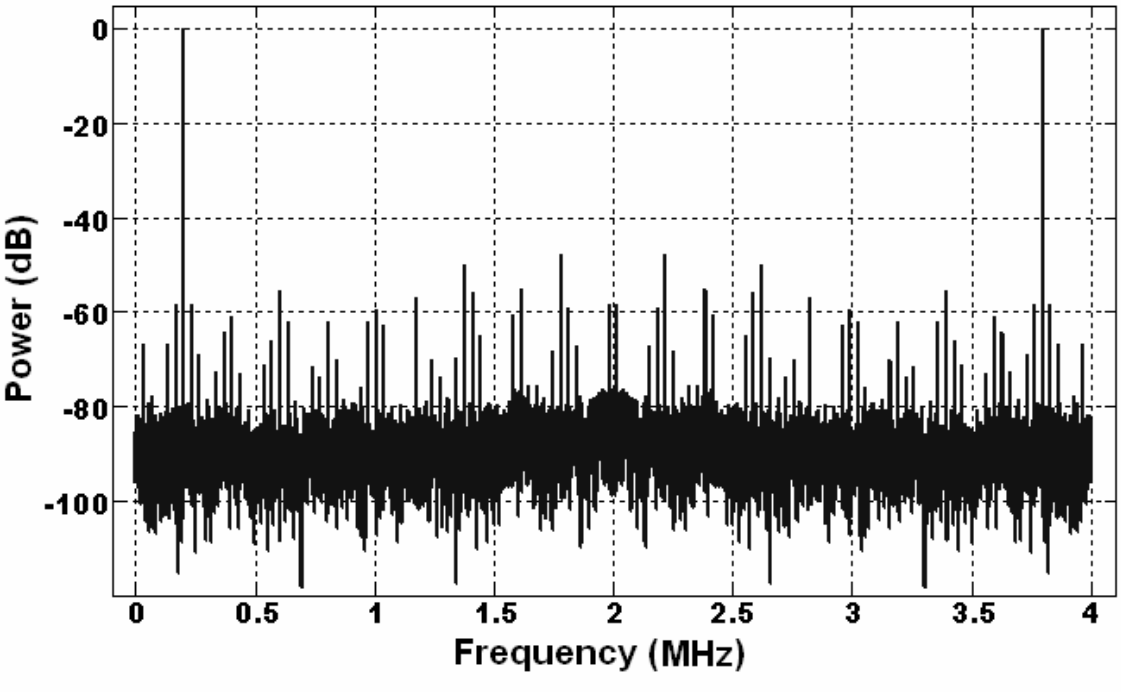


Figure 7.10: PSD experimental results for the time-mode cyclic ADC.

The power dissipation of this design was measured at approximate 4.4 mW. The PSD plot of the ADC output is provided in Figure 7.10. A SNR of 49.8 dB was measured indicating that this converter can achieve an approximate 8-bit resolution. However, with the distortion the SNDR was measured at 39.2 dB resulting in an ENOB of just over 6-bits. Table 7.1 summarizes the performance of the time-mode cyclic ADC.

Table 7.1: Design and experimental result summary for the time-mode cyclic ADC.

Technology	0.18-μm CMOS, single-poly, 6 metal
Supply Voltage	1.8 V
Core Area	0.013 mm^2
Power Dissipation	4.4 mW
Sampling Frequency	4 MHz
Time per Iteration	12.5 ns
SNR	49.8 dB
SNDR	39.2 dB
INL	±8 LSB
DNL	±0.5 LSB

A static linearity test was performed on the design. Using the same references and bias voltages described above, the input voltage was statically swept between 0.8 V to 1.2 V. For each input voltage step 16384 ADC output samples were averaged to reduce the effects of noise. The ADC's transfer characteristic plotting the input voltage versus the digital output code is presented in Figure 7.11(a). The DNL and INL data was extracted from the transfer characteristic and is revealed in Figure 7.11(b) and Figure 7.11(c), respectively. It may be seen that there are several occurrences where there are no code changes for input voltage regions. These regions correspond to the abrupt changes in the INL curve. It is believed that this phenomenon is created by the inconsistency of the TAMP gain.

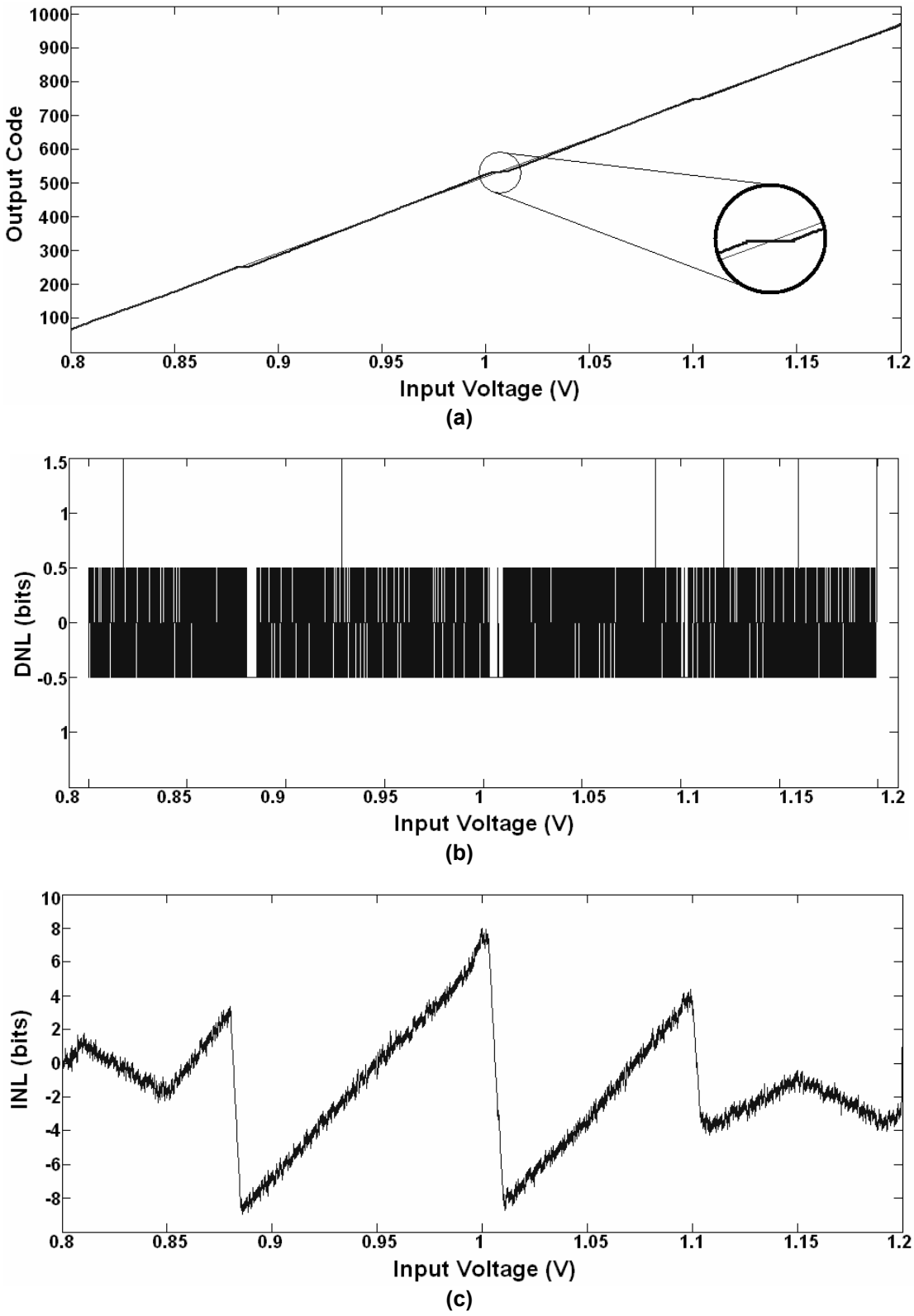


Figure 7.11: Experimental results for the time-mode cyclic ADC. (a) Output digital code and line-of-best fit. (b) Differential Nonlinearity (DNL), (c) Integral Nonlinearity (INL).

The processing time between iterations of the cyclic ADC was estimated by measuring the delay time between the input clock edge and the digital data arriving at the output pins. The digital output circuitry shifts data out every ten iteration cycles. Therefore, the measured delay was divided by ten to obtain the iteration time of approximately 12.5 ns. This information implies that implementing a pipeline architecture using this cyclic converter in the individual stages would result in a maximum sampling frequency of approximately 80 MHz.

7.4 - Conclusion

This chapter introduced the concept of pipeline A/D conversion using the TMSP methodology. It was shown that a single pipeline stage was easily transformed into a cyclic converter using digital components. Each time-mode pipeline stage or cyclic ADC incorporates a VTC, TDC, and TAMP circuit. An integrated circuit was fabricated to gain better insight into the feasibility of time-mode pipeline and cyclic ADCs. The IC implemented a 10-bit cyclic converter that could sample up to 4 MHz. The sampling speed limitation is directly related to the cyclic style of A/D conversion. It was experimentally determined that a pipeline architecture would permit a sampling rate of 80 MHz. However, a pipeline design would require significantly more area and power, and it would add latency to the output data. The power dissipation of the IC's core circuitry was found to be 4.4 mW. This is significantly more power than other TMSP ADCs discussed in previous chapters. The increased power consumption is due to the analog-based TAMP circuits.

Due to linearity limitations, the effective resolution of this ADC was limited to 6.2-bits. The linearity errors may be caused by several factors. First, the TAMP design does exhibit a non-linear gain. Moreover, achieving a gain of two with only the TAMP bias voltage may not be very accurate. The second error source is the comparator metastability which may also reduce performance as small residual

time difference may be incorrectly resolved. Finally, the VCDU nonlinearity poses a limitation on the overall linearity of the design. It is believed that the TAMP gain errors is the largest source of distortion. As such, the development of a calibration mechanism to compensate for the TAMP gain errors would greatly improve its performance.

Although the performance of the time-mode cyclic ADC is mediocre, this work is aimed at evaluating the last of the unexplored TMSP components described in Chapter 3. Specifically, the performance of the TAMP used in the context of time-mode ADCs.

Chapter 8: Successive Approximation and Integrating ADCs

Chapter 2 described the five main A/D conversion strategies: flash, delta-sigma, pipeline, successive approximation, and integrating ADCs. The implementation of flash, delta-sigma, and pipeline ADCs using TMSP are presented in Chapters 5, 6 and 7. The remaining two ADC designs unconditionally require a sample-and-hold circuit and were not implemented in silicon. Nevertheless, for completeness this chapter describes the successive approximation and integrating ADC designs in the context of TMSP.

8.1 Successive Approximation Register ADCs

The functional block diagram for a successive approximation register (SAR) ADC is reproduced in Figure 8.1(a). It consists of a sample-and-hold circuit, a voltage comparator, digital control logic, a digital register, and a DAC. The only component that may be replaced by its time-mode counterpart is the comparator, as shown in Figure 8.1(b). The sample-and-hold circuit is required due to the binary searching algorithm which must make successive comparisons to the same input voltage sample.

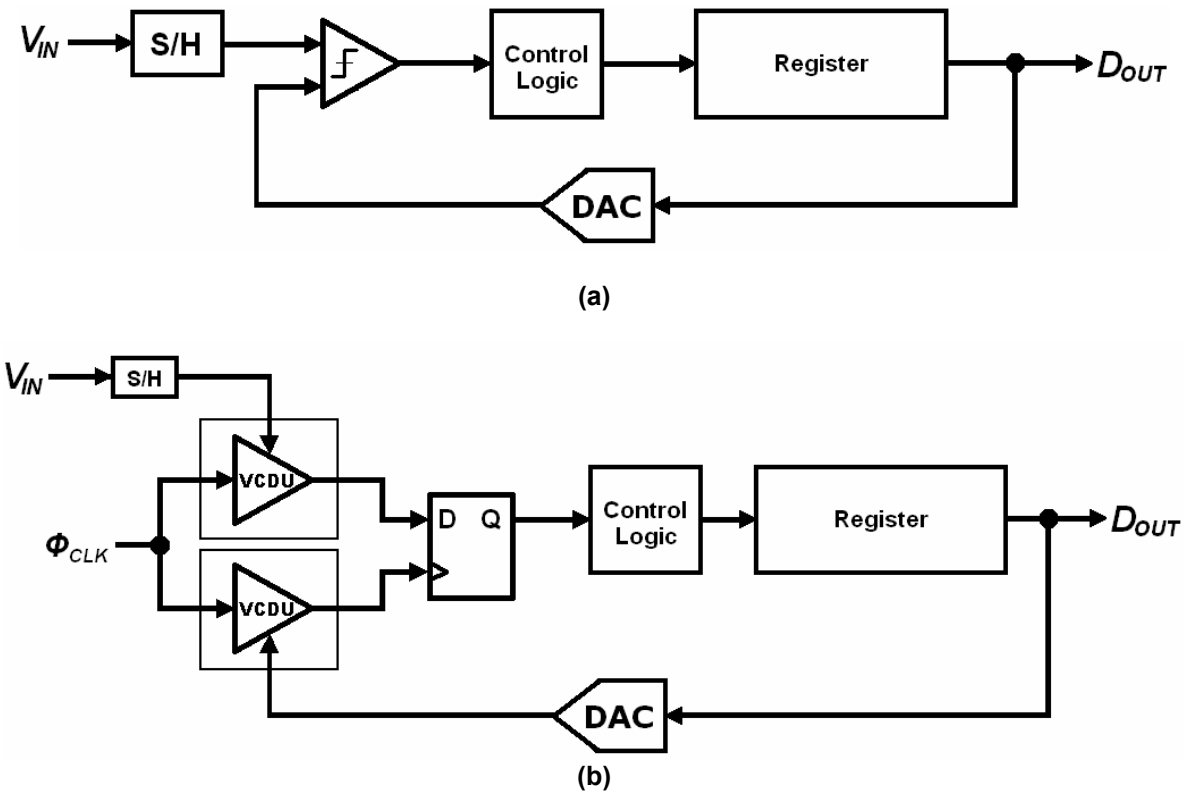


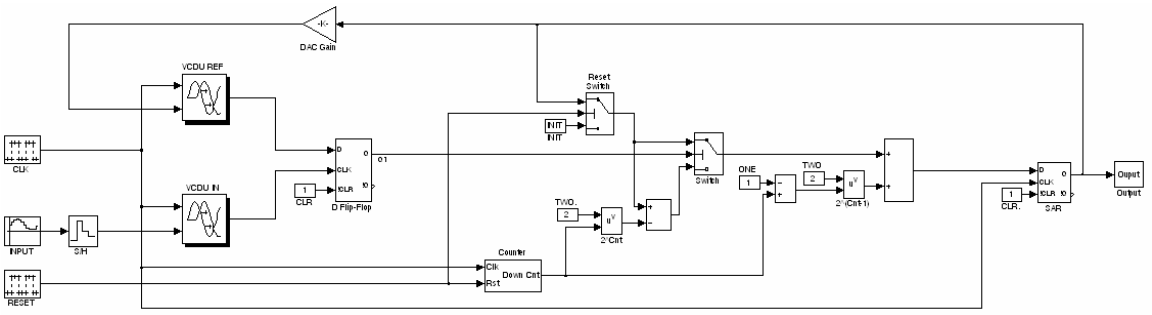
Figure 8.1: (a) Successive approximation register (SAR) ADC. (b) Time-mode SAR ADC.

Minimizing the comparator voltage offset is critical to the operation of a SAR ADC. Therefore, the all-digital calibration mechanism presented in Chapter 4 that may accompany the time-mode comparator is ideal for this ADC architecture.

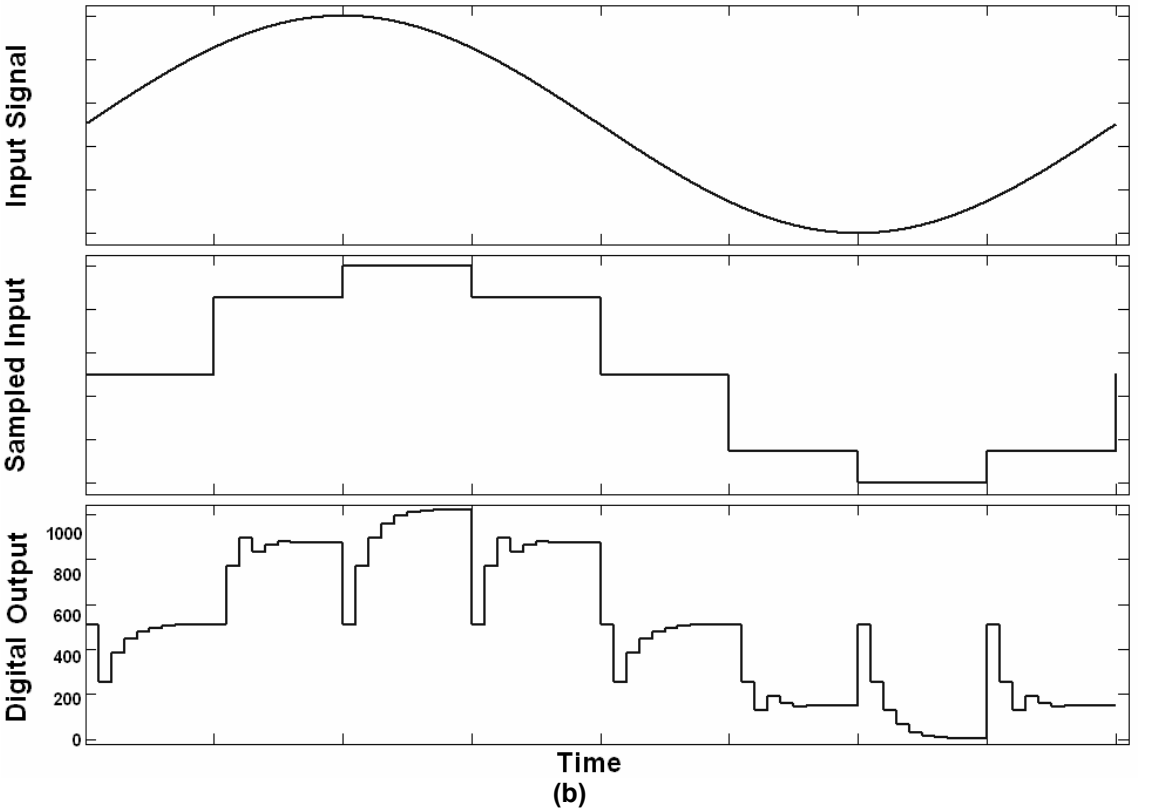
8.1.1 Time-Mode SAR ADC MATLAB Modeling and Simulation

The time-mode SAR ADC may be simulated in MATLAB using the simulink model presented in Figure 8.2(a). The time-mode comparator converts the input and feedback voltages into a time-difference using transport delay blocks and they are compared using a D-type flip-flop. The successive approximation register is also implemented with a single D-type flip-flop which can store real number values. The feedback DAC is simply a gain block as the digital data is already stored as an integer in the flip-flop. The digital control logic is implemented with a down counter, two switches, and several math function blocks. The simulation results gathered from a 10-bit ADC experiment are

displayed in Figure 8.2(b) in which eight samples were gathered from a sinusoidal input. The input signal was sampled and held for the duration of the binary search. The binary search output results are given in the figure.



(a)



(b)

Figure 8.2: Time-mode SAR ADC: (a) MATLAB Simulink model; (b) MATLAB simulation results.

8.1.2 Implementation Details and Practical Limitations

The DAC and comparator designs are the critical parts of any SAR ADC. The comparator must be able to detect voltage differences as small as the overall resolution of the converter. Moreover, voltage offset in the comparator must be calibrated. The DAC must also have a resolution and linearity equal to that of the desired ADC's resolution.

The proposed time-mode SAR ADC has a completely digital implementation, with the exception of the DAC and sample-and-hold circuit, thus offers the advantages of a very low power, compact and high speed (potentially hundreds of megahertz) design. Furthermore, it was shown in Chapter 4 that the time-mode comparator may be calibrated for voltage-referred offsets using an all-digital technique.

A sample-and-hold circuit is required for SAR ADCs and the time-mode equivalents design is no exception. As such, this would result in a significant silicon area increase.

8.2 Integrating ADCs

The integrating single-slope ADC architecture is illustrated in Figure 8.3(a). It operates by integrating the input voltage V_{IN} while comparing the integrator output to a fixed reference voltage using a comparator. The time interval between the start of integration and the comparator output transition is estimated by the count of a fast digital clock. This count is processed to generate a digital word D_{OUT} which represents the input analog sample.

An equivalent single-slope ADC can be designed using a TMSP strategy, as presented in Figure 8.3(b). The sampled input voltage V_{IN} is integrated and processed in time using a voltage-to-time integrator. The integrator is reset and

started using a NAND gate controlled by the ADC's clock signal ϕ_{CLK}. The total number of pulses from the integrator is counted within the fixed period of the clock pulse. The integrator oscillates with a period given by

$$T_{IN} = G_{\phi} V_{IN} + T_0 , \tag{8.1}$$

where T_0 is the oscillation period when the input voltage is zero and G_{ϕ} is the VCDU voltage-to-time conversion factor. T_0 represents the accumulated delay from the NAND gate and falling edge propagation through the VCDU. The total count *CNT* may be expressed with

$$CNT = \frac{T_{CLK}}{T_{IN}} , \tag{8.2}$$

where T_{CLK} is the width of the clock pulse. Substituting (8.1) into (8.2) reveals that the count is inversely proportional to the input voltage, i.e.

$$CNT = \frac{T_{CLK}}{G_{\phi} V_{IN} + T_0} . \tag{8.3}$$

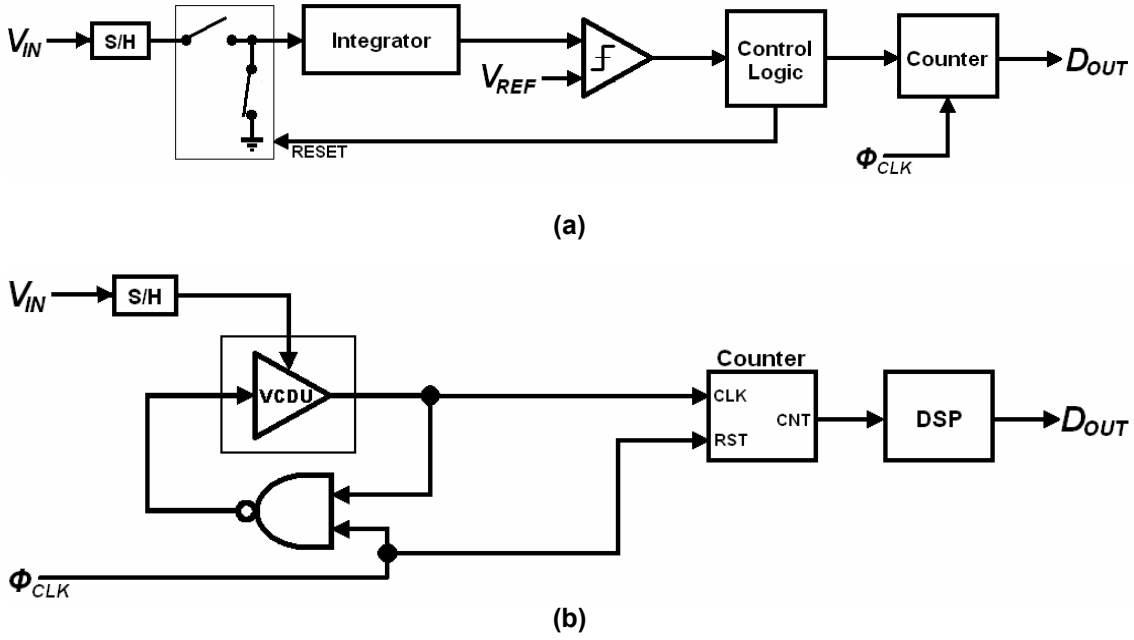


Figure 8.3: Integrating single-slope ADC (a) conventional block diagram; (b) time-mode Integrating ADC.

The digital representation of the input voltage may be obtained by rearranging equation (8.3), such as

$$V_{IN} = \frac{T_{CLK}}{G_\phi \cdot CNT} - \frac{T_0}{G_\phi}. \tag{8.4}$$

The precise determination of G_ϕ and T_0 will not be known as their values will differ from one design to the next due to process variation. Therefore a calibration scheme would need to be implemented. The minimum digital count can be acquired by setting the input voltage to zero volts, resulting in

$$CNT_{\min} = \frac{T_{CLK}}{T_0}. \tag{8.5}$$

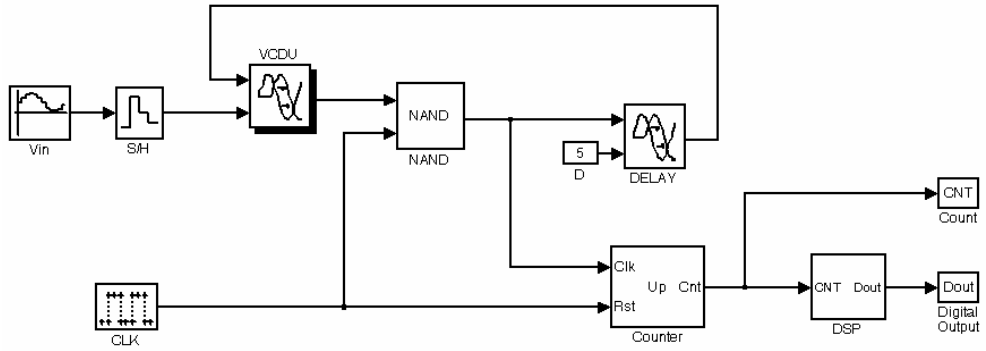
T_0 can be measured from Equation (8.5). The voltage-to-time conversion factor G_ϕ can be calculated by setting the input voltage to the full scale V_{FS} and obtaining the maximum output count dictated by

$$CNT_{\max} = \frac{T_{CLK}}{G_\phi V_{FS} + T_0}. \tag{8.6}$$

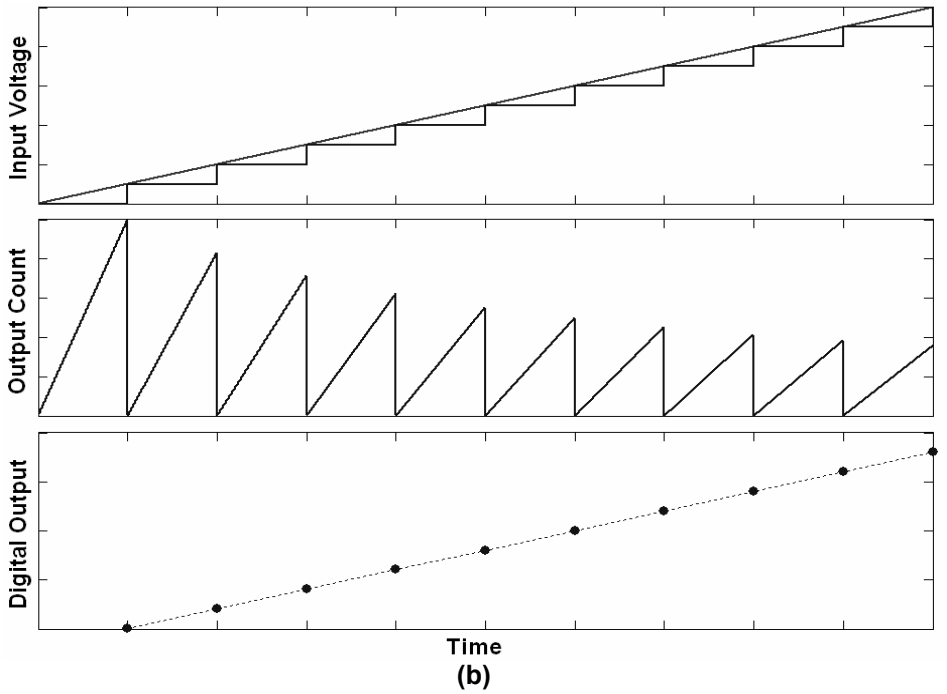
8.2.1 Time-Mode Integrating ADC MATLAB Modeling and Simulation

The time-mode integrating ADC shown in Figure 8.3(b) may be simulated in MATLAB using the model displayed in Figure 8.4(a). The VCDU is implemented with a transport delay block and the sample-and-hold is replaced a zero-order hold block. The NAND gate is implemented with a NAND function while its propagation delays are simulated with a constant delay. The digital output of the oscillator is counted using an Up-Counter with a clock input (*Clk*) and reset (*Rst*). The output of the counter is mathematically manipulated using Equation (8.4) to produce the digital output.

The MATLAB simulation results are presented in Figure 8.4(b). The input is swept with a constant slope and 10 uniform samples were taken. The counter output increments its count value for the duration of the clock pulse. Since the output count is inversely proportional to the input voltage, it reciprocal is taken to reveal digital output code.



(a)



(b)

Figure 8.4: Time-mode integrating single-slope ADC (a) MATLAB Simulink model; (b) MATLAB simulation results.

8.2.2 Implementation Details and Practical Limitations

The maximum sampling frequency that can be attained with this design may be approximated by

$$F_S \leq \frac{F_{OSC}}{2^D - 1}, \tag{8.7}$$

where F_S is the sampling frequency, F_{OSC} is the integrator's oscillating frequency, and D is the desired bit resolution of the converter. In a 0.18-μm CMOS process the voltage-controlled ring oscillator may achieve frequencies up to a few gigahertz. Therefore, the signal bandwidth that may be digitized will vary from a few hundred hertz for 20-bit resolutions to a megahertz range for 10-bit resolutions.

The linearity of the overall design will depend greatly on the VCDU. The design of the VCDU was described in Chapter 3 where it was shown that its linearity limits the input voltage range and could be adjusted by architectural choice. Therefore, the VCDU may once again be the component that limits the overall resolution of the ADC.

The time-mode integrating ADC described in Figure 8.3(b) is a completely digital circuit with the exception of the sample-and-hold circuit. Therefore, its power consumption will be quite low. Since a conventional sample-and-hold circuit is required for this design the silicon area will be significantly increased.

8.3 Summary

The time-mode SAR and integrating ADC were not fabricated due to their requirements for a DAC and sample-and-hold circuitry. Nevertheless, for completeness this chapter described the design and implementation of these ADCs in the context of TMSP.

The time-mode SAR ADC is simply designed by replacing the conventional voltage comparator with a time-mode comparator. Recall that the time-mode comparator offers the benefits of an all-digital implementation which implies low power operation using a small silicon area. Moreover, the time-mode comparator provides a digital calibration routine to compensate for voltage offsets caused by process variation. MATLAB simulations were presented to illustrate the operation of the time-mode SAR ADC.

The time-mode integrating ADC is implemented with a voltage-to-time integrator (i.e. voltage-controlled ring oscillator) and a digital counter. It offers the potential for high resolution at very slow sampling speeds. Moreover, it will be a very small design which would consume very little power. MATLAB simulations were performed to demonstrate the operation of the design. It should be noted that the linearity of this ADC configuration will be limited by the linearity of the VCDU.

Chapter 9: Conclusion

9.1 Thesis Summary

This thesis introduced the concept of time-mode signal processing (TMSP) and investigated its use in analog-to-digital conversion. Various TMSP circuit components were presented to convert voltage signals into time-difference variables, process these variables, and convert them into a digital representation. It was shown that the TMSP methodology could be used to implement voltage comparators and all five of the main ADC topologies: flash, SAR, pipeline (or cyclic), delta-sigma, and integrating ADCs. A time-mode comparator, flash ADC, cyclic ADC, and 3 delta-sigma ADCs were designed, fabricated, and tested.

The time-mode voltage comparator was implemented with a calibration mechanism to compensate for process variation. It was designed to compare large-scale input voltage, in the range of 0.4-V to 1.4-V with a 1.8-V supply. Experimental results demonstrate that this comparator could resolve voltages within an 8-bit resolution while operating at the test equipment's maximum rate of 25 MHz. Theoretically, a 200 MHz operation should be achievable. This device consumed a power of 900 μW. The calibration circuitry successfully demonstrated that mismatch between devices is calibrated to within the designed resolution.

A 7-bit time-mode flash ADC was implemented using 127 time-mode comparators with calibration. Due to a digital design limitation, the flash ADC could be clocked at a maximum of 5 MHz. The resolution was proven to be 7-bits with some distortion restricting its input voltage range to 0.8 V.

Three time-mode ΔΣ ADC were implemented in two separate ICs. Two of these ADCs were designed with single-ended inputs operating at different sampling frequencies. It was discovered that the higher-speed design offers the overall better performance as it samples at higher-speeds, generates less distortion, consumes less power, and occupies a smaller area. A 7-bit resolution was achieved with this design while dissipating less than 0.5 mW. The third time-mode ΔΣ ADC was constructed with differential-inputs. Improvements to this design were implemented having learned some of the shortcomings from the single-ended device. Experimentally, the differential ΔΣ ADC provided a 9-bit resolution while consuming 780 μW. These designs occupy a very small of 25-μm x 15-μm and 50-μm x 50-μm which is unprecedented throughout the literature.

A 10-bit cyclic ADC was developed using TMSP circuits. While sampling at 4 MHz a 6-bit effective resolution was obtained. The performance of this device is limited by the time-amplifier linearity and gain control. The power dissipated by this device was estimated at 4.4 mW, most of which is consumed by the time-amplifiers. If this design were implemented as a pipeline ADC it would offer a high-speed data conversion alternative, potentially into the hundreds of megahertz range.

The time-mode ADCs described in this work demonstrated the potential for high-sampling rates, low power consumption, and small silicon area usage. However, only mediocre resolutions were achieved. In all cases the voltage-controlled delay units, used to converter voltage signals into time-difference variables, were

a limiting factor on the linearity of the designs. In several cases a sample-and-hold circuit could have been used to improve performance.

With the exception of the time-mode pipeline/cyclic ADC, all the designs are constructed from digital circuitry. Hence, these circuits occupy small areas, consume low power, and operate at high clock speeds. Moreover, these devices would thrive if migrated to down-scaling technologies.

9.2 Future Works

The concept of time-mode signal processing is fairly new and at this stage of its development the possibilities seem endless. The work presented in this dissertation offers a foundation for understanding TMSP, recognizing its potential and limitations, and exemplifies some mixed-signal circuits built from this foundation. Other possibilities to advance and extend this work are:

1) The TMSP methodology is restricted to the application of A/D conversion because one crucial function is missing from the set of TMSP components. Specifically, the ability to perform the summation of two time-difference variables would extend TMSP into a general signal-processing tool. Therefore, one valuable research avenue is to exhaust the search for this TMSP function.

2) A crippling component of the time-mode ADCs is the VCDU. Its nonlinear behaviour has restricted the effective resolution of all designs to within 7 to 9-bits. Therefore, the linearization of the VCDU is an important advancement.

3) The time-mode delta-sigma ADCs are perhaps the greatest contribution of this work. They demonstrated the best overall performance out of all the time-

mode circuits investigated. They also offer many obvious areas of improvement and advancements. For example:

- The modulator designs could be modified to achieve gigahertz sampling rates. This may be achieved by reducing transistor sizes and minimizing buffer delay. The advantages of this are an increased signal bandwidth and a reduction in distortion by minimizing the VCDU's voltage-to-time conversion factor.

- A multi-bit design, as described in Chapter 6, could be implemented to achieve higher resolutions.

- If the summation of two time-difference variables ever becomes feasible, then higher-order modulators could be constructed by cascading integrators.

- It was shown that any mismatch between TMΔΣADC oscillators will result in a DC offset in the PDM output. A simple filter may be used to extract the DC offset from the PDM output and fed back to control the oscillators thus removing the offset.

- The TMΔΣADCs are influenced by the effects of jitter noise as they are built from ring oscillators. A PLL mechanism could be used to lock the signal and reference oscillators to a clean clock.

4) Without input voltage sample-and-hold circuitry the input signal bandwidth is limited by the conversion time of the VCDU. Therefore, incorporating input voltage sample-and-hold circuits may resolve some of the distortion problems at higher signal bandwidths.

5) Only three out of five ADC topologies were implemented in silicon. It would be interesting to observe the experimental performance of the time-mode SAR and integrating ADCs.

6) A final proposal for future work is to investigating the advantages and disadvantages of implementing these time-mode circuits into smaller technologies. This would offer some great insight as to their future value.

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Appendix A: Transistor Dimensions and Component Values for all Circuits

Appendix A offers all the transistor dimensions, component values, and bias conditions required to reproduce the designs presented in this dissertation. Each design that was simulated in HSPICE or experimentally tested is described in the following sections.

A.1 - Direct Voltage-Controlled VCDU

The direct voltage-controlled VCDU that was described in Section 3.1.1 is reproduced in Figure A.1. The transistor dimensions, capacitor value, and current and voltage biases are summarized in Table A.1.

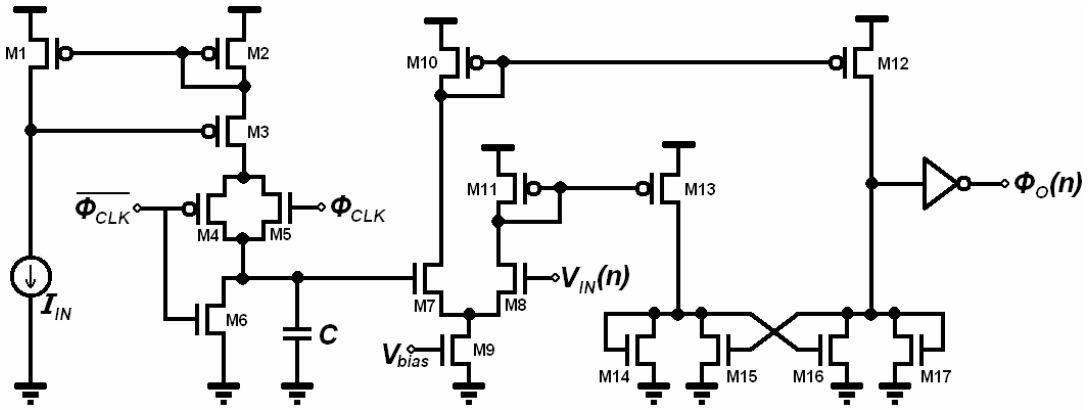

Figure A.1: Transistor schematic for the direct voltage-controlled VCDU presented in Figure 3.5(a).

Table A.1: Component values and bias conditions for the direct voltage-controlled VCDU presented in Figure A.1.

Component	Value
M1, M2	W / L = 60 µm / 0.18 µm
M3	W / L = 20 µm / 0.36 µm
M4, M4	W / L = 20 µm / 0.18 µm
M6, M7, M8	W / L = 10 µm / 0.18 µm
M9, M10, M11, M12	W / L = 25 µm / 0.18 µm
M14, M17	W / L = 1 µm / 0.18 µm
M15, M16	W / L = 2 µm / 0.18 µm
Output Inverter PMOS	W / L = 10 µm / 0.18 µm
Output Inverter NMOS	W / L = 10 µm / 0.18 µm
C	500 fF
I_{IN}	100 µA
V_{bias}	700 mV

A.2 - Current-Starved Inverter VCDU

The current-starved inverter VCDU that was described in Section 3.1.1 is reproduced in Figure A.2. The transistor dimensions and capacitor value are presented in Table A.2.

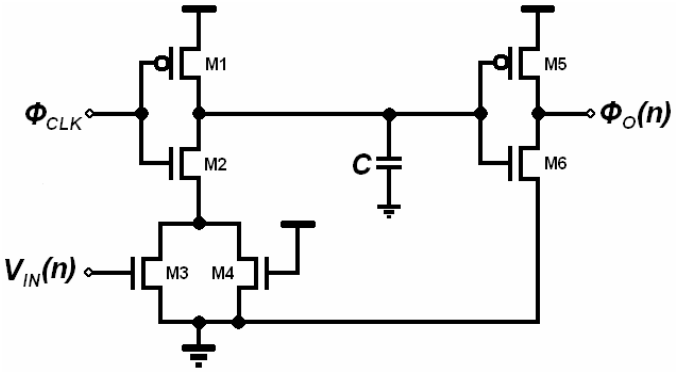

Figure A.2: Transistor schematic for the current-starved inverter VCDU presented in Figure 3.6(a).

Table A.2: Component values and bias conditions for the current-starved inverter VCDU presented in Figure A.2.

Component	Value
M1	W / L = 5 µm / 0.36 µm
M2	W / L = 2 µm / 0.36 µm
M3	W / L = 0.5 µm / 4 µm
M4	W / L = 1 µm / 0.5 µm
M5	W / L = 5 µm / 0.36 µm
M6	W / L = 2 µm / 0.36 µm
C	0 fF

A.3 - Time-Mode Comparator

The time-mode comparator is implemented with the VCDUs as shown in Figure A.2 and digital circuitry from standard cell libraries. Table A.3 summarizes the VCDU component values chosen to implement the comparator.

Table A.3: Component values for the VCDUs (i.e. Figure A.2) used in the time-mode comparator.

Component	Value
M1	W / L = 30 µm / 0.36 µm
M2	W / L = 10 µm / 1 µm
M3	W / L = 2 µm / 4 µm
M4	W / L = 5 µm / 1.2 µm
M5	W / L = 30 µm / 0.36 µm
M6	W / L = 10 µm / 0.36 µm
C	50 fF

A.4 - Single-Ended Input TMΔΣADC

The single-ended input TMΔΣADC that was described in Section 6.3 is illustrated in Figure A.3. It has been modified from Figure 6.5 converting the buffer into two inverters. Coincidently, the low-speed design (i.e. Figure 6.5) and high-speed design (i.e. Figure 6.7(a)) differ only by capacitor value. Table A.4 summarizes the transistor dimensions and capacitor values for both designs.

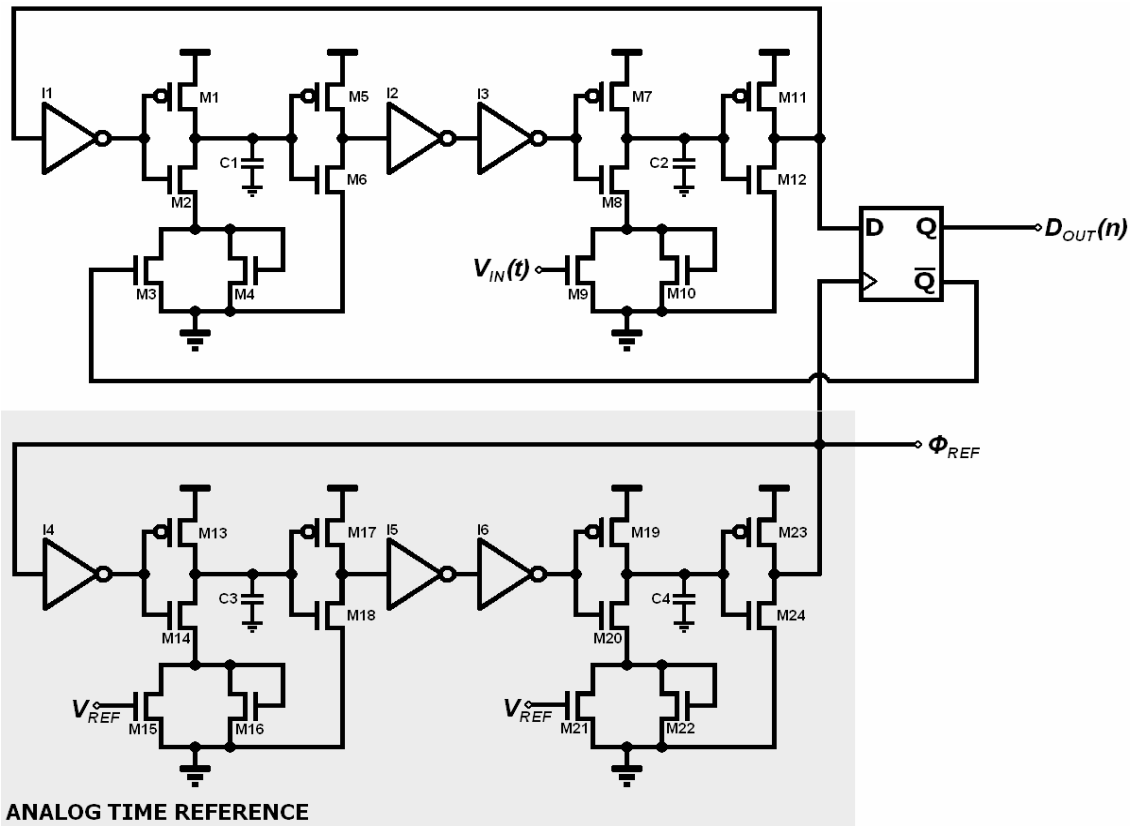

Figure A.3: Transistor schematic for the single-ended input first-order single-bit TMΔΣADC presented in Figure 6.5 and Figure 6.7(a).

Table A.4: Component values for the single-ended input first-order single-bit TMΔΣADC presented in Figure A.3.

Component	Value
M1, M7, M13, M19	W / L = 5 µm / 0.36 µm
M2, M8, M14, M20	W / L = 2 µm / 0.36 µm
M3, M9, M15, M21	W / L = 0.5 µm / 5 µm
M4, M10, M16, M22	W / L = 1 µm / 0.5 µm
M5, M11, M17, M23	W / L = 5 µm / 0.36 µm
M6, M12, M18, M24	W / L = 2 µm / 0.36 µm
Inverter I1 & I4 PMOS	W / L = 3.6 µm / 0.36 µm
Inverter I1 & I4 NMOS	W / L = 2 µm / 0.36 µm
Inverter I2 & I5 PMOS	W / L = 1 µm / 1 µm
Inverter I2 & I5 NMOS	W / L = 1 µm / 1 µm
Inverter I3 & I6 PMOS	W / L = 3.6 µm / 0.36 µm
Inverter I3 & I6 NMOS	W / L = 2 µm / 0.36 µm
C1, C2, C3, C4	Low-Speed Design: 500 fF High-Speed Design: 0 fF

A.5 - Differential- Input TMΔΣADC

Figure A.4 presents the differential-input TMΔΣADC reproduced from Figure 6.10(a) with component labels. Table A.5 lists the transistor dimensions that were used to implement this design. The AND gates A1, A2, A4 and A4 were implemented with the design shown in Figure A.5 with transistor dimensions outlined in Table A.6.

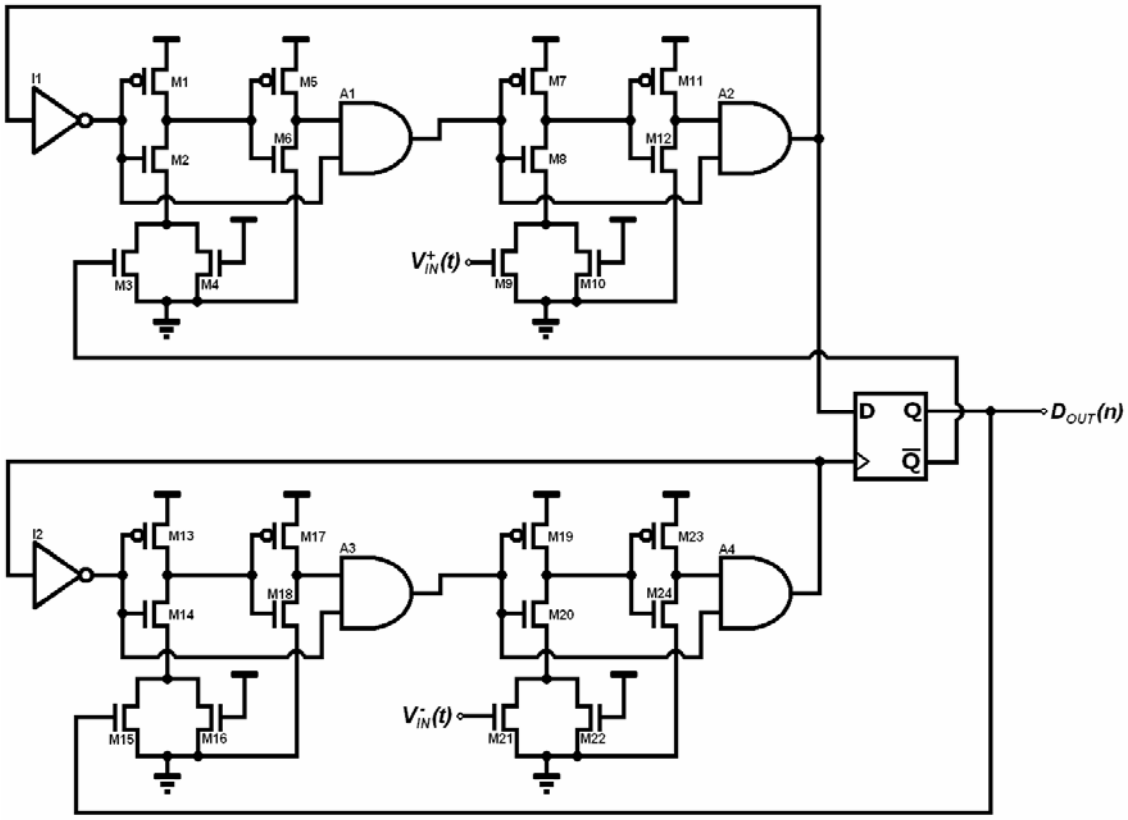

Figure A.4: Transistor schematic for the differential-input first-order single-bit TMΔΣADC presented in Figure 6.10(a).

Table A.5: Component values for the differential-input first-order single-bit TMΔΣADC presented in Figure A.4.

Component	Value
M1, M7, M13, M19	W / L = 10 µm / 0.36 µm
M2, M8, M14, M20	W / L = 2 µm / 0.36 µm
M3, M9, M15, M21	W / L = 0.5 µm / 5 µm
M4, M10, M16, M22	W / L = 0.5 µm / 1 µm
M5, M11, M17, M23	W / L = 10 µm / 0.36 µm
M6, M12, M18, M24	W / L = 10 µm / 0.36 µm
Inverter I1 & I2 PMOS	W / L = 20 µm / 0.36 µm
Inverter I1 & I2 NMOS	W / L = 10 µm / 0.36 µm

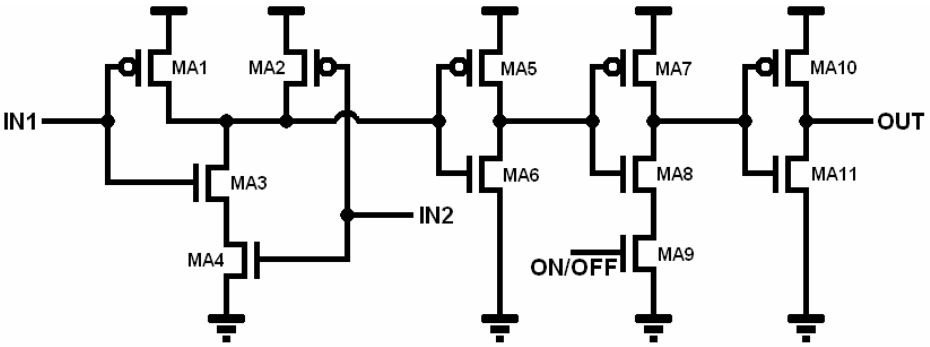

Figure A.5: Transistor schematic for the AND gates A1, A2, A3, and A4 shown in Figure A.4.

Table A.6: Transistor dimensions for the AND gate presented in Figure A.5.

Component	Value
MA1, MA2, MA3, MA4, MA5	W / L = 10 µm / 0.36 µm
MA6	W / L = 0.5 µm / 2 µm
MA7	W / L = 15 µm / 0.36 µm
MA8, MA9, MA11	W / L = 10 µm / 0.36 µm
MA10	W / L = 20 µm / 0.36 µm

A.6 - Time-Mode Cyclic ADC

The time-mode cyclic ADC was designed from several components for which their component values are given in the following subsections.

A.6.1. VCDU Design

The VCDU designs used in the time-mode cyclic converter are same architecture illustrated in Figure A.2. The transistor dimensions that were used are summarized in Table A.7.

Table A.7: Component values used to implement the VCDUs incorporated in the time-mode cyclic ADC.

Component	Value
M1	W / L = 10 µm / 0.36 µm
M2	W / L = 2 µm / 0.36 µm
M3	W / L = 0.5 µm / 5 µm
M4	W / L = 0.5 µm / 1 µm
M5	W / L = 10 µm / 0.36 µm
M6	W / L = 10 µm / 0.36 µm
C	0 fF

A.6.2. Time-Amplifier

Figure A.6 reveals the time amplifier design used in the time-mode cyclic ADC and Table A.8 presents the component values.

Table A.8: Component values used to implement the time-amplifier given in Figure A.6.

Component	Value
M1, M2, M3, M4	W / L = 2 µm / 2 µm
M5, M8	W / L = 20 µm / 0.18 µm
M6, M7	W / L = 10 µm / 0.18 µm
M9, M10, M11, M12	W / L = 10 µm / 1 µm
M13	W / L = 40 µm / 1 µm
Inverters I1 & I2 PMOS	W / L = 2.5 µm / 0.18 µm
Inverters I1 & I2 NMOS	W / L = 1.8 µm / 0.18 µm
AND gate A1 & A2 PMOS	W / L = 12 µm / 0.36 µm
AND gate A1 & A2 NMOS	W / L = 12 µm / 0.36 µm
C1, C2, C3, C4	250 fF

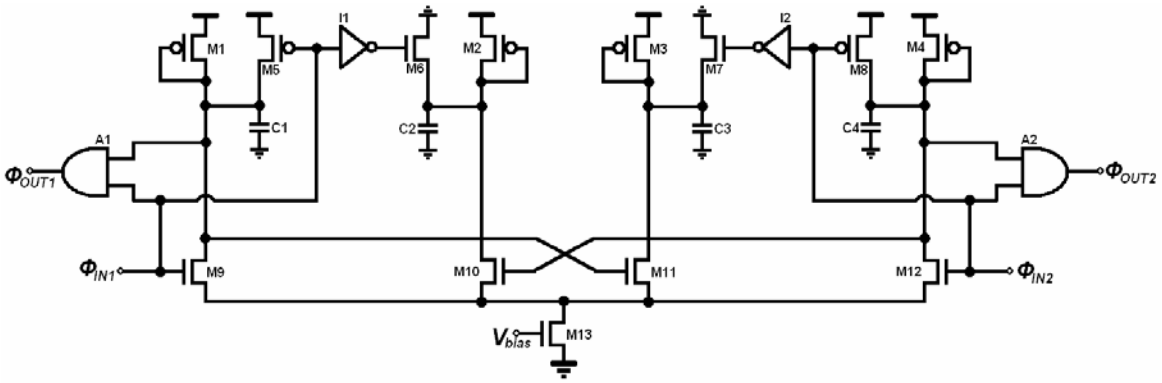

Figure A.6: Transistor schematic for the time amplifier used in the time-mode cyclic ADC.

A.6.3. Time Comparator with Pre-Amplifier

The time comparator with pre-amplifier implemented in the time-mode cyclic ADC is depicted in Figure A.7. Table A.9 presents the component values used in the design.

Table A.9: Component values used to implement the time comparator shown in Figure A.7.

Component	Value
M1, M2, M3, M4	W / L = 10 µm / 0.18 µm
M5, M6	W / L = 10 µm / 0.72 µm
M7, M8, M9, M10	W / L = 10 µm / 0.18 µm
Inverters I1 & I2 PMOS	W / L = 2.5 µm / 0.18 µm
Inverters I1 & I2 NMOS	W / L = 1.8 µm / 0.18 µm
R1, R2, R3, R4	10 kΩ
C1, C2, C3, C4	0 fF

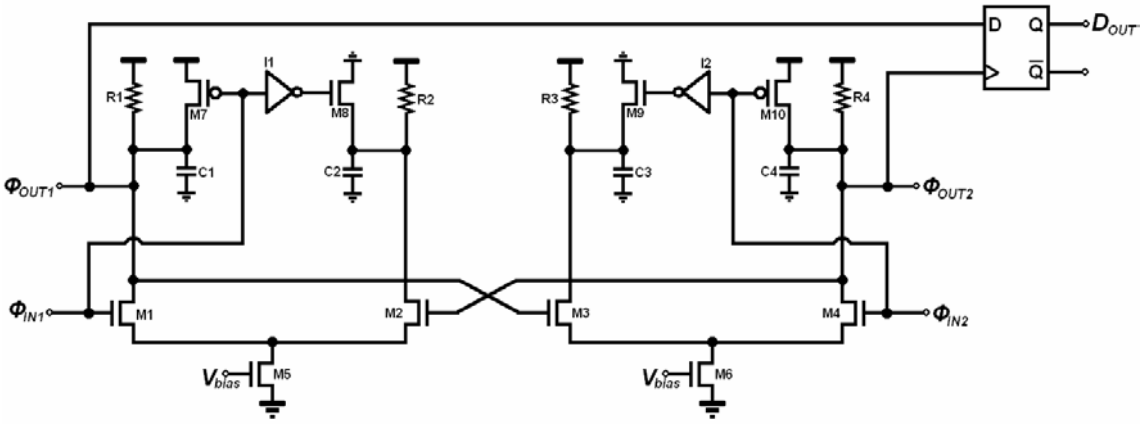

Figure A.7: Transistor schematic for the time comparator with pre-amplification.

A.6.4. DAC

The time-mode cyclic ADC incorporates a 1-bit DAC as shown in Figure A.8. Table A.10 presents the component values used for the DAC.

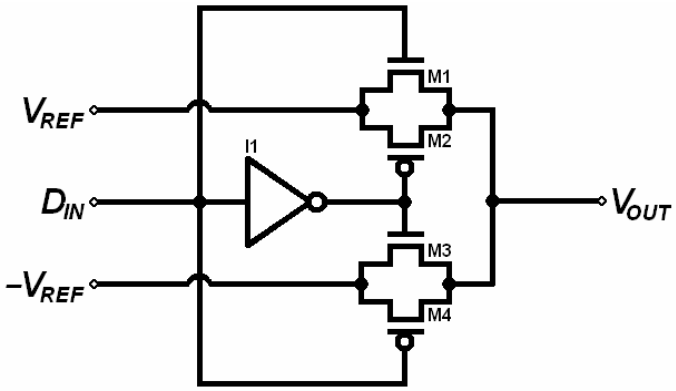

Figure A.8: Transistor schematic for the time comparator with pre-amplification.

Table A.10: Component values used to implement the time comparator shown in Figure A.8.

Component	Value
M1, M2, M3, M4	W / L = 10 µm / 0.18 µm
Inverter I1 PMOS	W / L = 2.5 µm / 0.18 µm
Inverter I1 NMOS	W / L = 1.8 µm / 0.18 µm