Digital Processing of Analog Information Adopting Time-Mode Signal Processing

Mohammad Ali Bakhshian

(***B.Sc. 2001, M.Sc. 2004***)

Department of Electrical and Computer Engineering

McGill University, Montréal

June 2012

A thesis submitted to the faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Doctorate of Philosophy

I dedicate this thesis to my father, ***Mohsen Ali Bakshian*** *who passed away a few hours after I passed my Ph.D. comprehensive exam.*

He made me understand by heart what the word “support” means. I would give up anything to hug him for just one more time.

Abstract

As CMOS technologies advance to 22-nm dimensions and below, constructing analog circuits in such advanced processes suffers many limitations, such as reduced signal swings, sensitivity to thermal noise effects, loss of accurate switching functions, to name just a few.

Time-Mode Signal Processing (TMSP) is a technique that is believed to be well suited for solving many of these challenges. It can be defined as the detection, storage, and manipulation of sampled analog information using time-mode variables. One of the important advantages of TMSP is the ability to realize analog functions using digital logic structures. This technique has a long history of application in electronics; however, due to lack of some fundamental functions, the use of TM variables has been mostly limited to intermediate stage processing and it has been always associated with voltage/current-to-time and time-to-voltage/current conversion. These conversions necessitate the inclusion of analog blocks that contradict the digital advantage of TMSP.

In this thesis, an intensive research has been presented that provides an appropriate foundation for the development of TMSP as a general processing tool. By proposing the new concept of delay interruption, a completely new asynchronous approach for the manipulation of TM variables is suggested. As a direct result of this approach, practical techniques for storage, addition and subtraction of time-mode variables are presented.

Abstract

To Extend the digital implementation of TMSP to a wider range of applications, the comprehensive design of a unity gain dual-path time-to-time integrator (accumulator) is demonstrated. This integrator is then used to implement a digital second-order delta-sigma modulator.

Finally, to demonstrate the advantage of TMSP, a very low power and compact tunable interface for capacitive sensors is presented that is composed of a number of delay blocks associated with typical logic gates. All the proposed theories are supported by experimental results and post-layout simulations.

The emphasis on the digital construction of the proposed circuits has been the first priority of this thesis. Having the building blocks implemented with a digital structure, provides the feasibility of a simple, synthesizable, and reconfigurable design where affordable circuit calibrations can be adopted to remove the effects of process variations.

Résumé

Les technologies CMOS progressant vers les procédés 22 nm et au delà, la abrication des circuits analogiques dans ces technologies se heurte a de nombreuses limitations. Entre autres limitations on peut citer la réduction d'amplitude des signaux, la sensibilité aux effets du bruit thermique et la perte de fonctions précises de commutation.

Le traitement de signal en mode temps (TMSP pour Time-Mode Signal Processing) est une technique que l'on croit être bien adapté pour résoudre un grand nombre de problèmes relatifs a ces limitations. TMSP peut être défini comme la détection, le stockage et la manipulation de l'information analogique échantillonnée en utilisant des quantités de temps comme variables. L'un des avantages importants de TMSP est la capacité à réaliser des fonctions analogiques en utilisant des structures logiques digitales. Cette technique a une longue histoire en terme d'application en électronique. Cependant, en raison du manque de certaines fonctions fondamentales, l'utilisation de variables en mode temps a été limitée à une utilisation comme étape intermédiaire dans le traitement d'un signal et toujours dans le contexte d'une conversion tension/courant-temps et temps-tension/courant. Ces conversions nécessitent l'inclusion de blocs analogiques qui vont a l'encontre de l'avantage numérique des TMSP.

Résumé

Cette thèse fournit un fondement approprié pour le développement de TMSP comme outil général de traitement de signal. En proposant le concept nouveau d'interruption de retard, une toute nouvelle approche asynchrone pour la manipulation de variables en mode temps est suggéré. Comme conséquence directe de cette approche, des techniques pratiques pour le stockage, l'addition et la soustraction de variables en mode temps sont présentées.

Pour étendre l'implémentation digitale de TMSP à une large gamme d'applications, la conception d'un intégrateur (accumulateur) à double voie temps- à -temps est démontrée. cet intégrateur est ensuite utilisé pour implémenter un modulateur delta-sigma de second ordre.

Enfin, pour démontrer l'avantage de TMSP, une Interface de très basse puissance, compacte et réglable pour capteurs capacitifs est présenté. Cette interface est composé d'un certain nombre de blocs de retard associés à des portes logiques typiques. Toutes les théories proposées sont soutenues par des résultats expérimentaux et des simulations post-layout.

L 'implémentation digitale des circuits proposés a été la première priorité de cette thèse. En effet, une implémentation des bloc avec des structures digitales permet des conceptions simples, synthétisable et reconfigurables où des circuits de calibration très abordables peuvent être adoptées pour éliminer les effets des variations de process.

Acknowledgements

I would like to express my deepest gratitude and respect towards my supervisor, Dr. Gordon W. Roberts. His one-of-a-kind personality, enthusiasm, dedication, and understanding have made my Ph.D. degree enjoyable, and intellectually stimulating. The support he provided to me during these years helped me to fix all the chaos happened in my personal life after the death of my father. When I started my Ph.D. study under his supervision in 2007, I could never imagine to what extent I would change after a few years. Now, I feel more optimistic, self-confident, and professional while I see my dramatically improved attitude towards everything in my life. He is a kind of personality pattern that I would never forget any time soon. For what he taught me in the past few years, I will always be indebted.

I would also like to thank my Ph.D. committee members, Dr. Vamsy Chodavarapu and Dr. Roni Khazaka for their invaluable support and advice.

To all the members of the MACS lab, present and past, I would like to offer my appreciation for their friendship and support. Collectively, they are a tremendous pool of friendship and knowledge for which I could not have succeeded without. Specifically, I would like to thank Mohammad Shahidzadeh-Mahani, Mourad Oulman, Omar Abdelfattah, Tsung-Ten Tsai, Azhar Ahmed Chowdhury, George Gal, Mohammad Taherzadeh-Sani, Ali Gorji, and Ali Ameri who made my stay at McGill an enjoyable experience.

A very special thank to my sister, Reyhaneh, who took on my family responsibilities after the unfortunate death of my father. Without her love and sacrifice, it would never ever be possible for me to stay at McGill and continue my study. I always felt in my heart how eager she was to see me following my dreams. I also want to thank my mother for her unconditional love and my other sisters Mahdiyeh, Haniyeh, and Nooshin for their love and support.

Last but not the least; I would like to thank my best friend, my lifetime partner, my love, my wife, Maryam. I cannot find the right words to describe all the support and love she gave to me. Being a student is stressful by itself. Being a Ph.D. student adds lots of contradictions and challenges to a student life. With her unbelievable patience and endless love, I was always motivated to overcome all the challenges; on any occasion, I felt free to satisfy my ambitions in a selfish way. During all my Ph.D. years, while she was suffering the pains of our long-distance relationship, she always kept encouraging and inspiring me. I believe this degree belongs to her not me.

Claim of Originality

The Contributions of this dissertation are described as follows:

- To provide a new foundation for the development of time-mode signal processing (TMSP) as a general processing tool, the new concept of delay interruption is introduced in Chapter 3. In addition, by adopting this new concept, digital techniques for storage, addition, and subtraction of time-mode variables are proposed.

- The circuit building blocks to implement the developed techniques for operation on time-mode variables are presented in Chapter 3. The circuit diagram for a new block, called switched-voltage-controlled delay unit (SDU), is presented. This block is used to implement the proposed delay-interruption technique. A critical building block, known as Time Latch (TLatch), is developed. The TLatch is composed of two SDUs together with some logic gates. This block is used to latch the time-difference between two digital rising edges at the input port. During the read mode of a TLatch, the latched TM variable can be combined with another TM variable applied to the second input of the TLatch to perform an addition or subtraction. Comprehensive analysis and simulation of the block are presented.

- In Chapter 4, a general asynchronous technique for direct processing of time-mode variables in time domain and without any time to voltage/current conversion is presented. As the rising edges representing the input TM variable are passed through two parallel paths, the output TM variable can change according to the variation of the propagation delay in each path. Combining this approach with the delay-interruption technique, different applications can be implemented in time domain. Specifically this approach is used to develop a digital technique for the integration (accumulation) of time-mode variables.

- A single-path time-to-time integrator constructed from TMSP blocks is presented in Chapter 4. It consists of a TLatch together with a number of SDUs and a combination of typical digital building blocks. Although the circuit diagram for the integrator is simple, the throughput of the integrator is limited by the instantaneous time intervals between each two successive outputs. To tackle this limitation, by adopting the queuing concept a dual-path time-to-time integrator is presented. In the dual-path structure, the sequence of input samples is forwarded to a queue with two positions. While the integrator is integrating the current TM input, the next input will be stored in the queue upon its arrival to be used within an appropriate timing. The dual-path structure works properly as long as the average input throughput of the integrator is equal to its average output throughput. To compensate for the errors induced by mismatch, a very affordable technique is presented as well. An integrated circuit was fabricated implementing a digital dual-path time-to-time integrator with calibration and the experimental results are presented at the end of Chapter 4.

- The structure for a modified voltage-controlled delay unit is presented in Chapter 5. By sampling the control voltage directly on a capacitor, a fixed-value current is used to discharge the capacitor and make the delay. Within

the operating voltage range of the switch, the output delay will be linearly controlled by the control voltage.

- A second-order time-mode delta-sigma modulator is presented in Chapter 5. The main building blocks of the modulator are the dual-path time-to-time integrator and the digital feedback network. All the delay blocks utilized in the modulator structure are composed of an identical CMOS part together with different capacitors. The design procedure consists of the steps to optimize the value of the capacitor for each delay unit in order to satisfy the design specs. To address the non-uniform sampling of the input voltage that occurs in most of VCO based data converters, a simulation-based approach is revealed. The feasibility of implementation and proof of concept for the proposed modulator is justified by post-layout simulation results.

- The design of a time-mode first order delta-sigma interface circuit for capacitive sensors is presented in Chapter 6. The application is best suited for lab-on-chip applications where a DC or low frequency output capacitance of a sensor is subject to measurement. The design utilizes standard digital cells in association with capacitive-controlled delay units. The circuit is tunable for different ranges of input capacitance as well as different sensitivities. The main advantage of the proposed circuit is its extremely low power consumption while occupying a very small footprint. Process-related mismatches would be corrected using the proposed digital tuning algorithm. An integrated circuit incorporating the interface circuit was fabricated and the experimental results are presented at the end of Chapter 6.

Part of the work described in this thesis was published in some well-distinguished journals. Specifically, part of the review presented in Chapter 2 was published in the *Transactions on Circuits and Systems II* [57]. The new technique for the storage, addition, and subtraction of time-mode variables has been filed as a US Patent (US 61/644,468) and it is published in *Electronic Letters* [78]. The content of Chapter 4 is published in the *Transactions on Circuits and Systems I* [79].

Finally, a brief description of the design proposed in Chapter 6 is presented at the 2009 International Symposium on Circuits and Systems [80]. The composed manuscript presenting the comprehensive description of the design is under revision to be published in the *Transactions on Circuits, and Systems I*. The job of preparing more publications to present the second-order time-mode delta-sigma modulator presented in Chapter 5 is still in progress.

Table of Contents

List of Figures

List of Tables

List of Acronyms

A/D	**Analog-to-Digital**
ADC	**Analog-to-Digital Converter**
CCDU	**Capacitance-Controlled Delay Unit**
CMOS	**Complimentary Metal Oxide Semiconductor**
DAC	**Digital-to-Analog Converter**
DLL	**Delay-Locked Loop**
DR	**Dynamic Range**
DSP	**Digital Signal Processing**
DTC	**Digital-to-Time Converter**
IC	**Integrated Circuit**
OSR	**Oversampling Ratio**
PCB	**Printed Circuit Board**
PLL	**Phase-Locked Loop**
PSD	**Power Spectral Density**
RMS	**Root-Mean-Square**
S/H	**Sample and Hold**
SDA	**Serial Data Analyzer**
SFDR	**Spurious-Free Dynamic Range**
SNR	**Signal-to-Noise Ratio**
SNDR	**Signal-to-Noise and Distortion Ratio**
SoC	**System-on-Chip**
SDU	**Switched voltage-controlled Delay Unit**
TDC	**Time-to-Digital Converter**

THD	**Total Harmonic Distortion**
TLatch	**Time Latch**
TM	**Time-Mode**
TMDS	**Time-Mode Delta-Sigma**
TMSP	**Time-Mode Signal Processing**
VCDU	**Voltage-Controlled Delay Unit**
VCO	**Voltage-Controlled Oscillator**
VDL	**Vernier Delay Line**
VLSI	**Very Large Scale Integration**
VTC	**Voltage-to-Time Converter**

Chapter 1: Introduction

1.0. Motivation

Digital design is the driving force for the rapidly emerging deep submicron CMOS technologies. As such, CMOS processes are typically optimized for the needs of digital circuitry. In other words, CMOS technologies are being developed to improve digital switching speeds, lower the supply voltages, and reduce transistor geometries to increase the packing density of digital circuits. These improvements have pushed the processing of digital information into the gigahertz frequency range. The need for digital, analog, and mixed-signal circuits to be integrated on a single die (i.e. SoC) is escalating as companies struggle to drive down cost, boost productivity, and create lower power and smaller devices.

There are many challenges in integrating analog and mixed-signal circuits in a state-of-the-art digital CMOS process. As emerging CMOS technologies reduce feature size dimensions, the thickness of the transistor gate oxide reduces forcing the system voltage to decrease. This negatively affects analog and mixed-signal circuit performance by exercising transistors at non-optimal operating points and permitting currents to leak through transistor gates [1]. This dilemma results in reduced input voltage swings and linearity problems for the processing of analog voltage signals. To upset the design challenge even further, area and power budgets are at best being preserved if not reducing. Additional implementation challenges are imposed when analog and mixed signal

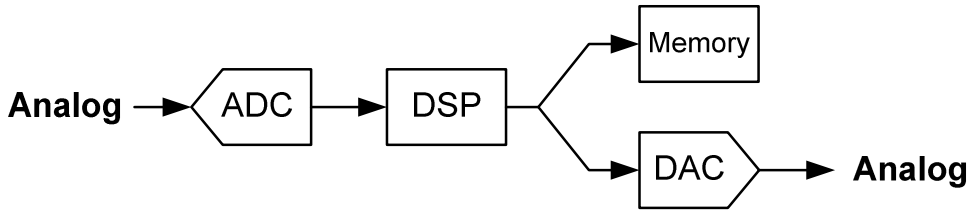


Fig. 1.1. The block diagram for a conventional analog data processing system with DSP

processing functions must coexist with digital circuits. The switching noise [2] from the digital circuitry may couple into the analog blocks thus corrupting analog information.

A conventional data processing system to perform the processing of analog information is illustrated in Fig. 1.1. Due to all the benefits associated with digital design, it is mostly desired to perform most of the processing in digital domain; consequently, a front-end analog-to-digital converter (ADC) is used to convert the input analog information into digital bits and continue the processing in digital domain. In order to offset some of the ADC design challenges imposed by digitally driven deep submicron CMOS processes, a potential candidate to replace conventional voltage signal processing is being investigated, referred to as time-mode signal processing or TMSP.

The idea behind TMSP is based on considering time as the variable under processing instead of conventional analog variables such as current or voltage. Any positive, negative or zero analog quantity can be corresponded to a positive, negative or zero time-mode variable respectively. A time-mode variable is defined as the time (phase) difference between two digital rising edges. Due to the digital nature of the signals representing a time-mode variable, the circuits involved in TMSP consist of a digital CMOS construction while the variable under processing, i.e. phase, is still an analog quantity. As a conclusion, in TMSP analog accuracy and digital advantage can be combined together.

The analog data processing using TMSP methodology is depicted in Fig.

Fig. 1.2. The pre-processing of analog information adopting TMSP and before conversion into digital domain

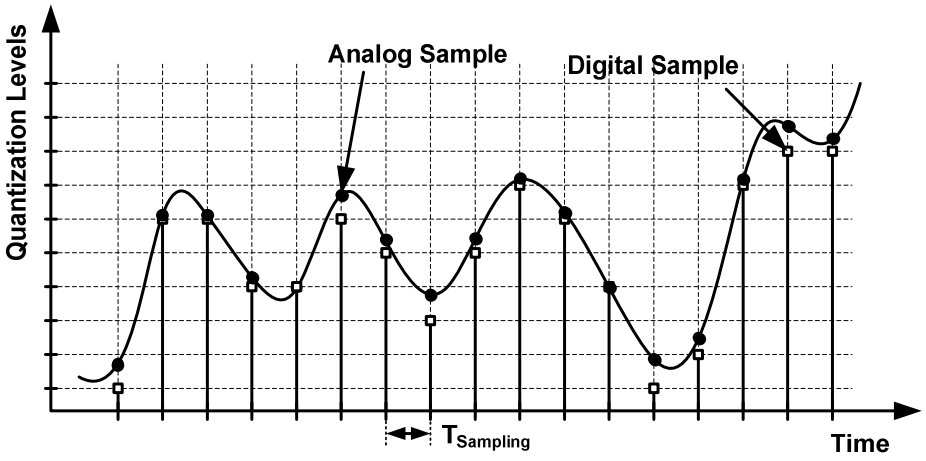


Fig. 1.3. Illustrating the difference between discrete analog (time-mode) samples and discrete digital samples of an identical input analog waveform.

1.2. Since analog information begins in the form of either a voltage or a current, a voltage/current-to-time converter (V/CTC) is employed to convert the input signal into a time-mode variable. The time-mode variable is then processed by various circuits resulting in an output time-mode signal. Finally, this signal is transformed into a digital representation using a time-to-digital converter (TDC) to continue the processing in a digital domain. As will be explained in the next chapter, most of the achievements reported by researchers and performed in TMSP are restricted to the implementation of fast ADCs or first-order delta-sigma modulators that limits the application of the block diagram in Fig. 1.2 to the implementation of the ADC block in Fig. 1.1. TMSP has never been considered as a general processing tool for manipulating analog information.

As the level of accuracy for the DSP block in Fig. 1.1 is a function of the resolution of the front-end ADC, the requirement of a higher precision increases the design cost for this ADC; also, as the resolution of the ADC increases, the area of the digital part increases exponentially. By considering TMSP as a comprehensive processing methodology, however, part of the post processing can be done in digital domain using analog variables (time-mode variables) and with a higher accuracy. For a sample analog signal as shown in Fig. 1.3, instead of processing the discrete quantized version of the analog input, the discrete

time-mode samples of the input waveform can be processed. By continuing the processing in time-mode, analog variables will be used while the building blocks are mostly designed in digital domain. Consequently, instead of performing for example a 12-bit addition between two operands, the corresponding time-mode version of the two operands can be added in time domain while only two digital signals are used to represent each one. This can dramatically decreases the area and save the precision of the results while this system offers all the benefits of a digital design. Therefore, TMSP circuits will operates at high speeds, consume low power, and occupy small silicon area. Moreover, these performance specifications will improve with newer and smaller digitally driven CMOS technologies and finally it can be synthesizable. However, it should be mentioned that the transient nature of the variable to be processed in a TMSP circuit, i.e. time, complicates the design of such circuits. As will be explained through the rest of this document, each time-mode variable will be available according to a specific timing. To develop any new building block, this special timing should be monitored carefully. In addition, it should be noticed that a trade-off would exist between the dynamic range and speed of a TMSP circuit. As a bigger time-mode variable needs a bigger time-span, longer processing time will be needed. This disadvantage, however, can be tackled with parallel structures as will be explained later.

1.1. Thesis Scope

The research described in this thesis aims to address the growing need for innovative circuit design techniques that will permit and continue the integration of high-performance analog processing circuits in emerging state-of-the-art digital sub-micron CMOS technologies. This broad objective is narrowed down to a classification of circuits and signal processing techniques referred to as time-mode signal processing or TMSP.

After reviewing the previously reported achievements in TMSP, the primary discovery goal is achieved by resolving one of the most fundamental obstacles in the development of TMSP, which is the addition or subtraction of two time-mode variables performed directly in time domain. Several additional

techniques and experimental circuits were designed and fabricated to demonstrate the feasibility of the proposed technique to extend the application of TMSP into the design of time-to-time integrators and higher orders of delta-sigma modulators. It is intended to show that by developing the techniques to implement basic arithmetic functions such as addition, subtraction, and integration of time-mode variables, TMSP can be used for a broader range of applications than the implementation of only front-end ADCs. Specifically, this thesis reveals that by adopting TMSP methodology a second-order delta-sigma modulator can be implemented using only digital building blocks. It is also shown that the application of TMSP can be extended more into the design of interface circuitry for CMOS sensors.

1.2. Thesis Overview

This thesis is organized into six chapters excluding this introduction. Each chapter is described as follows.

Chapter 2 starts by the definition of the concepts and the terms used in TMSP and it then follows by the review of the previously reported achievements in this methodology. Since a very wide range of designs may process time or phase as the variable under processing, the designs that consist of a digital construction are considered in this chapter. This chapter ends by outlining the obstacles restricting further development of TMSP.

The proposed techniques to implement the addition and subtraction of time-mode variables without any time to voltage/current conversion are presented in Chapter 3; also, a dynamic memory cell to latch and store time-mode variables is proposed in this chapter that adopts the proposed techniques for time-mode addition and subtraction.

Chapter 4 outlines a new asynchronous approach for the design of TMSP circuits where the achievements made in Chapter 3 are used to implement a time-to-time integrator. The time-to-time integrator was fabricated in 0.13-um IBM CMOS technology and its experimental results are presented.

The design of a second-order delta-sigma modulator using digital building blocks is presented in Chapter 5. By using identical CMOS delay units, the

modulator design procedure is outlined in a few steps. Following these steps, the values of the capacitors associated with each delay unit will be tuned.

To show other applications for TMSP, a very low power and compact tunable interface for capacitive sensors is presented in Chapter 6. The time-mode sensor interface circuit was fabricated in 90-nm ST CMOS technology and its experimental results are presented.

Finally, this dissertation is concluded in Chapter 7 where the work is summarized, strengths and weaknesses are highlighted, and future advancements of this work are offered.

Chapter 2: Time-Mode Signal Processing

2.0. Introduction

Time-Mode Signal Processing (TMSP) can be defined as the detection, storage, and manipulation of sampled analog information using time-mode variables. It provides a means to implement analog signal processing functions in any technology using the most basic element available, i.e., propagation delay. The delay in CMOS may be produced either by an arbitrary series of delay blocks, such as those shown in Fig. 2.1, or by a voltage-controlled delay unit (as will be explained later). While the propagation delay of a signal can be as low as the delay of a digital inverter (a few picoseconds), theoretically there is no upper

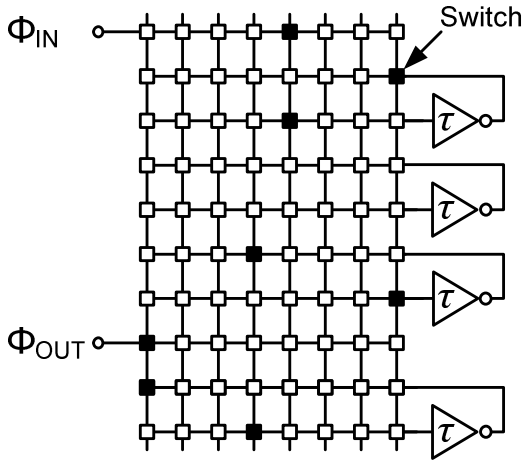


Fig. 2.1. A reconfigurable arbitrary set of delay elements to implement a desired delay value for TMSP

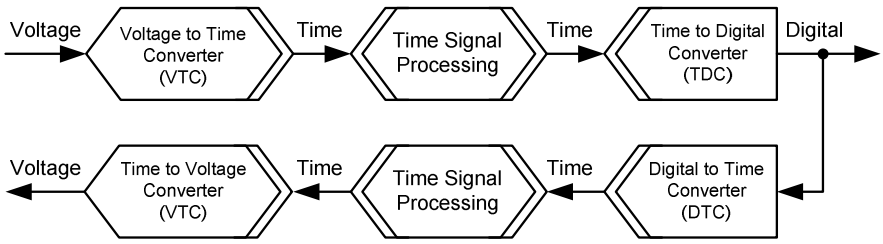


Fig. 2.2. Adopting TMSP for processing analog and digital signals

limit for that. Compared to any voltage-based analog design technique that limits the dynamic range of the input/output signal between the noise level (100's of micro-volts) and power supply, very promising results might be expected.

Time-mode variables are discrete samples of analog information. As long as we use time-mode (TM) parameters, the only applicable voltage values will be digital high and low levels; consequently, we can start from digital blocks and modify them to implement analog applications. In other words, TMSP enables computations using the timing of asynchronous events; so, any voltage or current value might be corresponded to an identical time or phase difference between two digital rising edges. In this new method, the nature of the variable under processing is analog while the tools to implement the processing will be digital.

Since most information begins in the form of a voltage, a Voltage-to-Time Converter (VTC) is employed to convert the input signal into a time-mode variable. The time signal is then processed by various circuits resulting in a time output. Finally, the processed time signal is transformed into a digital representation using a Time-to-Digital Converter (TDC). By adopting TMSP for the processing of analog time-mode variables, there will be no more need to multi-bit digital computations. This loop of voltage to digital conversion may be closed back in a reverse path by including Digital to Time Converters (DTC) as well as Time to Voltage Converters (VTC), as shown in Fig. 2.2.

In this chapter, the definitions and concepts associated with TMSP are defined and the previously reported building blocks relevant to this topic are listed and reviewed briefly. Although the emphasis in this document is to develop this method as a mostly digital technique, some analog circuitries related to this topic are included as well to give an overall view about the previous achievements

accomplished and the future progress intended.

2.1. The Definitions of the Basic Operations among TM Variables

2.1.1. Time-mode variable

A time-mode variable, ΔT, is defined as the quantity of time between an event occurring with respect to a reference time or event. It can be the differential time or phase difference between rising edges of two step-like digital signals (Fig. 2.3.a) where one of the signals is considered as the reference (Φ_{REF}) and the other one as the signal (Φ_{SIG}). According to this definition, a negative or positive variable is introduced when Φ_{SIG} leads or lags Φ_{REF} respectively. The second alternative to define ΔT is the duration of a single digital pulse, as shown in Fig. 2.3.b. This definition can be adopted to implement only positive quantities.

Taking the first definition, any positive or negative analog voltage or current value can be easily corresponded to an identical positive or negative time-mode variable. This way, a one-to-one relation might be established between variables in time domain and voltage/current domain.

2.1.2. Addition and Subtraction

Fig. 2.4 provides the illustrated definitions for addition and subtraction of two time-mode variables. As shown in the figure, any mathematical operation, including addition or subtraction, with more than one time variables can be done in two modes of synchronized or asynchronized. For asynchronized operation, as shown in Fig. 2.4.a, each time-mode input has its own reference signal; however, for synchronized operation, shown in Fig. 2.4.b, all the inputs share a common reference signal. As shown in Fig. 2.4.b, synchronized subtraction will be a non-

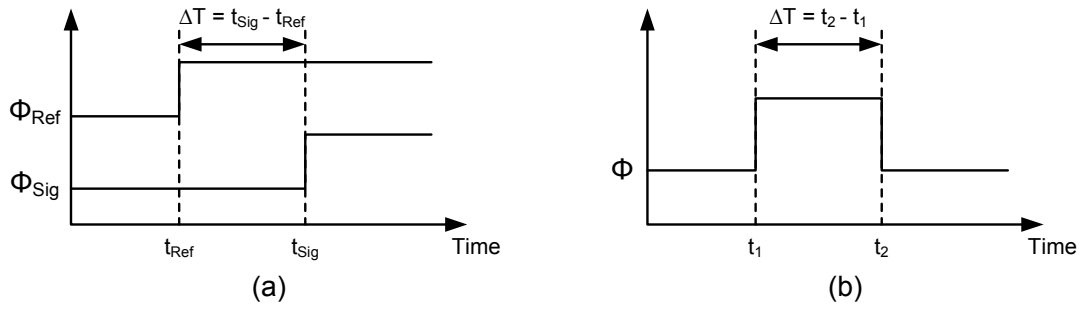


Fig. 2.3. Different definitions for Time-Mode variable ΔT (a) phase delay, (b) pulse width

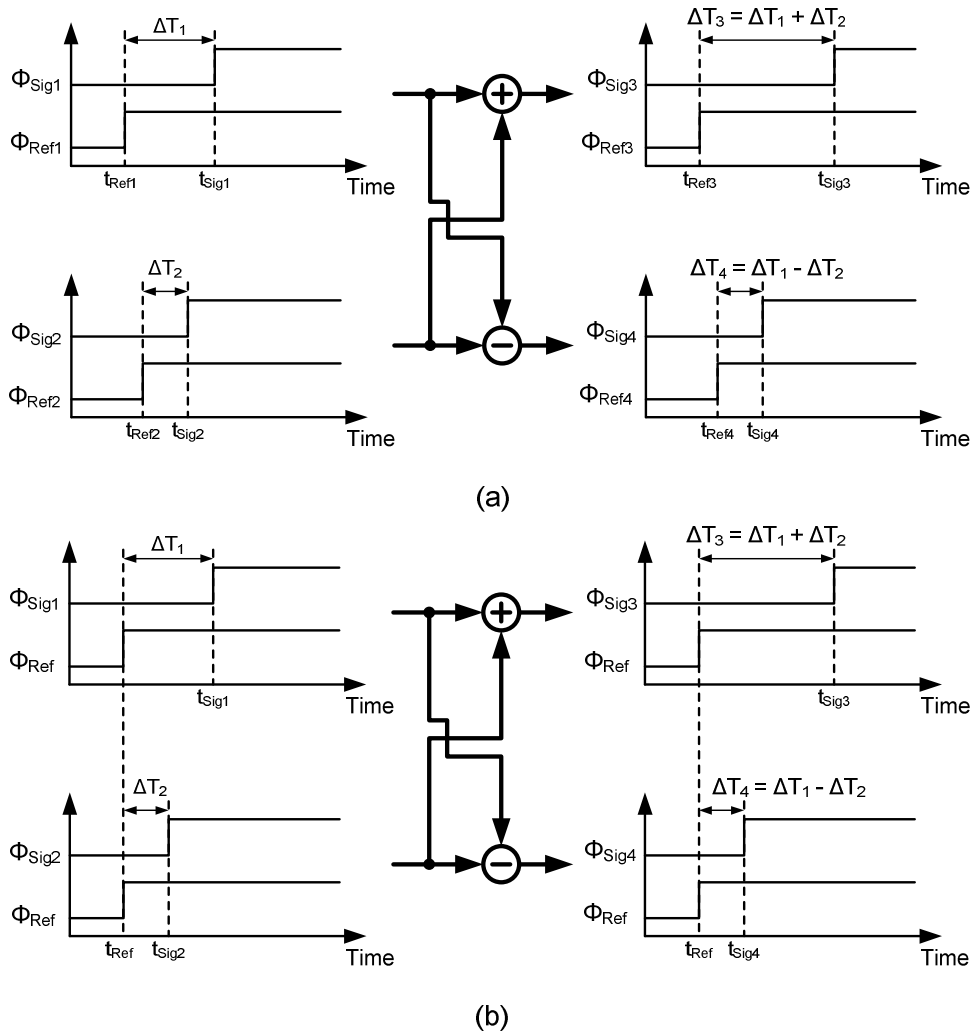


Fig. 2.4. Addition and subtraction of two TM variables (a) asynchronized (b) synchronized

causal phenomenon since the output should be predicted before the input is completely in (i.e. $t_{SIG4}<t_{SIG1}$). For the ease of implementation and application, we select asynchronized mode as the default mode of addition and subtraction among TM variables.

2.1.3. Scalar multiplication and division

Scalar multiplication and division are defined as the expansion and shrinkage of the input time variable by a factor of *K* respectively.

2.1.4. Integration

Integration, as a critical operation essential for the development of practical signal processing circuits, is defined as shown in Fig. 2.5. The phase or

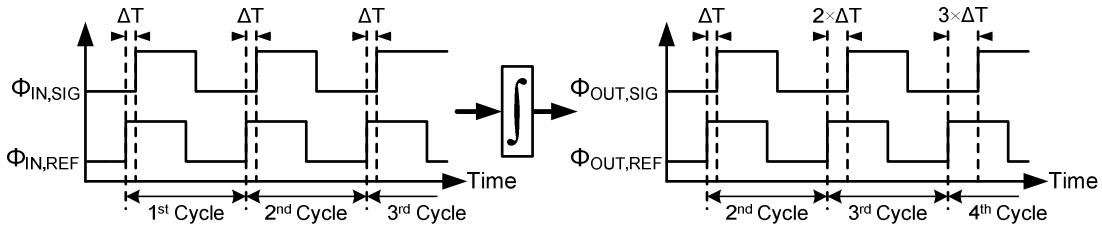


Fig. 2.5. Time-mode integration

time difference between waveforms $\Phi_{IN,SIG}$ and $\Phi_{IN,REF}$, the signal and the reference inputs in each cycle, is integrated into the time difference between $\Phi_{OUT,SIG}$ and $\Phi_{OUT,REF}$, according to

$$\begin{aligned} &\Delta T_{Out}[1] = \Delta T_{In}[0] \\ &\Delta T_{Out}[2] = \Delta T_{Out}[1] + \Delta T_{In}[1] \\ &\ldots \\ &\Delta T_{Out}[n] = \Delta T_{Out}[n-1] + \Delta T_{In}[n-1] \end{aligned} \tag{2.1}$$

Although the wider dynamic range compared to voltage domain is a strong motivation behind TMSP, a time integrator is subject to saturation like its voltage counterpart. The constraint resulting in the saturation of a time-mode integrator is the limited period of each signal. Although selecting the right strategy for the detection of saturation in an integrator depends on the method used to implement it, as a rule of thumb an extra edge on either the signal or the reference waveform, during the interval of each cycle makes good evidence that the output is saturated, as illustrated in Fig. 2.6.

2.1.5. Delay

Signal and reference waveforms incorporated in any TM variable pair are

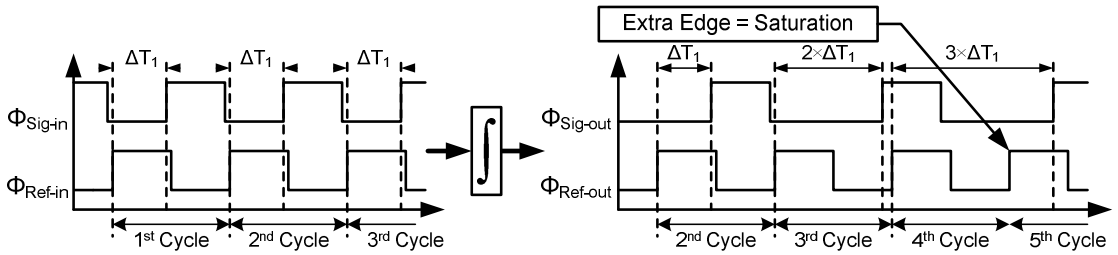


Fig. 2.6. Saturation in a TM integrator

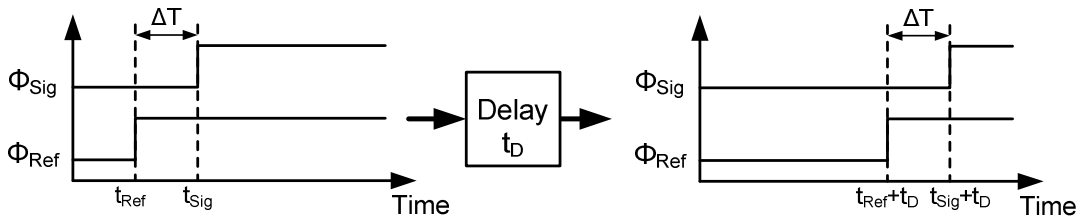


Fig. 2.7. The delay function

not stationary and the variable ΔT is ready when both rising edges of signal and reference waveforms arrive. As shown in Fig. 2.7, a delay block is used to postpone the arrival time of these edges for a time delay of t_D.

2.1.6. Memory

The memory block latches the time difference between the two input rising edges. After the memory cell is readout, two rising edges with the same time difference will be created at the output.

2.1.7. Comparison

A decision block (comparator) is necessary to facilitate the implementation of any conditional process in TMSP. The decision should be made based on which time input is greater or if the sign of the input time signal is positive or negative. For two TM inputs ΔT_1 and ΔT_2, output of the comparator is a logic 1 if and only if $\Delta T_1 > \Delta T_2$; also, for a single input ΔT, the output is logic 1 if and only if the rising edge at the signal waveform lags the rising edge at the reference waveform ($\Delta T > 0$).

2.2. Available Building Blocks for TMSP

As illustrated in Fig. 2.2, TMSP can be utilized for middle-stage processing during analog to digital or digital to analog conversion. In this section, different building blocks essential to understand and implement basic functions in time-mode signal processing will be reviewed.

2.2.1. Voltage-Controlled Delay Unit

A voltage-controlled delay unit (VCDU) is the fundamental block to facilitate the conversion of voltage into time. It proportionally delays an input time event (i.e. a rising edge) with respect to a sampled input voltage. As shown in

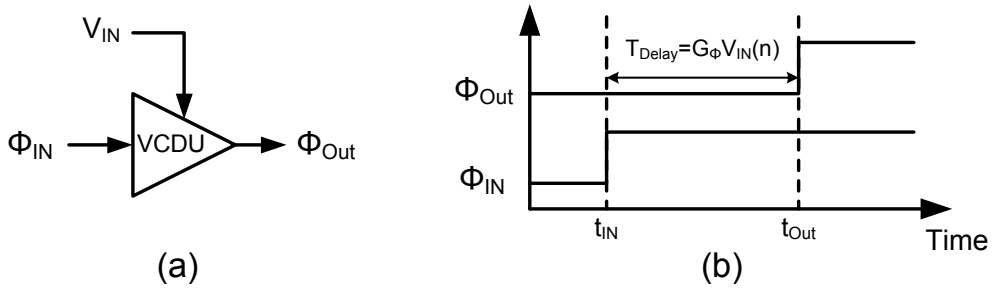


Fig. 2.8. VCDU block (a) the symbol (b) the signal representation

Fig. 2.8.a, a VCDU has two inputs; an input waveform Φ_{IN} that has a low-to-high transition at time t_{IN} and the sampled input voltage V_{IN} that controls the time of the low-to-high transition for the output waveform Φ_{OUT}, as shown in figure 2.8.b.

The relation which governs the linear conversion between voltage $V(t)$ and time is given by the charge and discharge of a linear capacitor as

$$I(t) = C\frac{dV(t)}{dt}, \tag{2.2}$$

where, C is some nodal capacitance and $I(t)$ is the current to discharge the voltage $dV(t)$ across the capacitor. Two strategies can be used to implement a VCDU, direct voltage-controlled strategy and current-controlled strategy.

In a direct voltage-controlled strategy, illustrated in Fig. 2.9, the delay is generated by forcing the capacitor C to be charged using a constant current I_{IN}. This capacitor is initially pre-reset to zero while the input signal Φ_{IN} is low. After the charging begins with respect to the rising edge of the input, the comparator output switches from logic “0” to logic “1” once the voltage on the capacitor reaches the desired input voltage V_{IN}; hence, the output time-difference T_{Delay} is

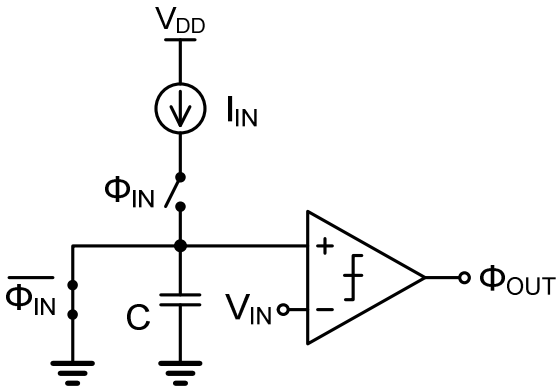
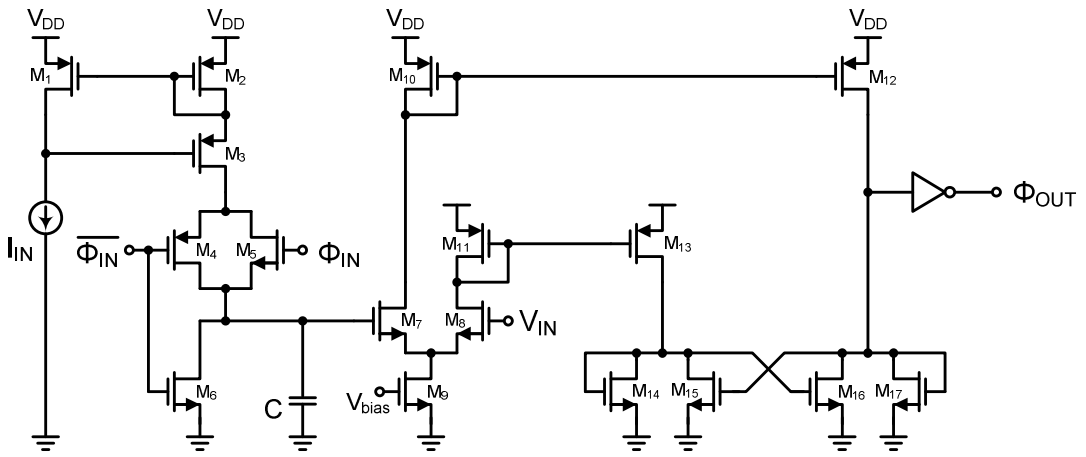
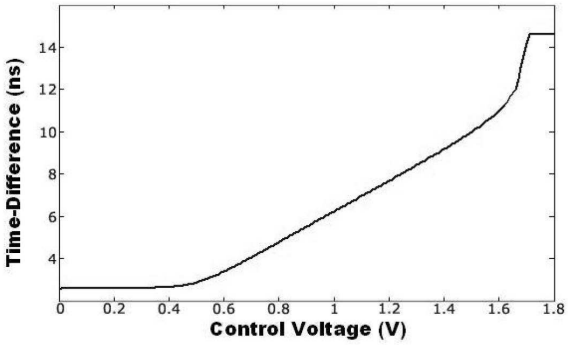


Fig. 2.9. Direct voltage controlled VCDU



(a)



(b)

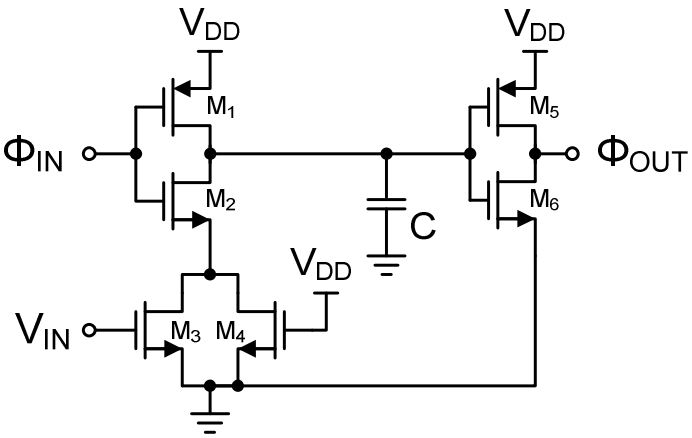
Fig. 2.10. (a) a CMOS transistor schematic of a direct voltage controlled VCDU (b) voltage-to-time transfer characteristic of the circuit in part (a)

the time interval between the input clock and the comparator output switching times. The equation describing the conversion process is given by the following equation

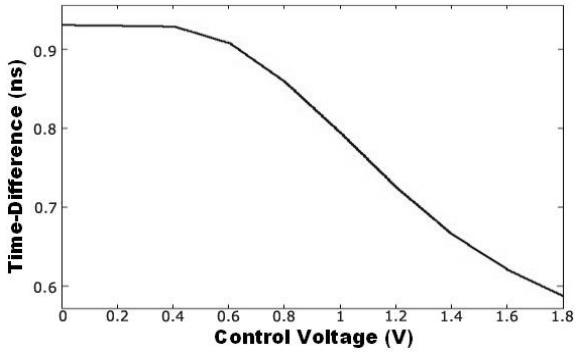
$$T_{Delay} = \frac{C}{I_{IN}} V_{IN} = G_{\phi} V_{IN}, \tag{2.3}$$

where, the voltage-to-time conversion factor G_{ϕ} is equal to $\frac{C}{I_{IN}}$.

In Fig. 2.10.a, a CMOS transistor schematic of a direct voltage controlled VCDU is presented [3]. A Wilson current mirror, formed by transistors M_1-M_3, is used to generate the constant current reference I_{IN}. During the logic low phase of Φ_{IN}, the capacitor C is reset via transistor M_6. The charging of the capacitor



(a)



(b)

Fig. 2.11 (a) a CMOS transistor schematic of a direct voltage controlled VCDU (b) Voltage-to-time transfer characteristic of the circuit in part (a)

begins on the rising edge of Φ_{IN} through the transmission gate switch formed by transistors M_4 and M_5. The current-steering amplifier, constructed by transistors M_7-M_{13}, senses the difference between the input voltage V_{IN} and the capacitor voltage permitting the output latching circuit (M_{14}-M_{17}) to make a logic decision. A sample transfer characteristic for the circuit, obtained through an HSPICE simulation, is presented in Fig. 2.10.b. The voltage-to-time conversion factor $G_{ø}$ may be obtained by calculating the slope of the linear region of the transfer characteristic. The linear operating region is limited within the voltage range of 0.6 V and 1.4 V with less than a ±0.1% linearity error. This limitation is a very important constraint to use VCDU blocks to make a conversion between voltage and time.

The second method to convert voltage waveforms into time-mode

variables is by controlling the current source in Fig. 2.9. In this case, a voltage-controlled current source would be implemented while the comparator input voltage, V_{IN}, is fixed. A common implementation for this class of a VCDU is often referred to as a current-starved inverter and is quite popular in the design of voltage-controlled oscillators [4–10]. These designs are very simplistic whereby the comparator is implemented by an inverter with its built-in threshold reference voltage.

A CMOS transistor schematic of a current-starved inverter VCDU is shown in Fig. 2.11.a. Upon the arrival of any falling edge at Φ_{IN}, the inside capacitor is charged to V_{DD} and Φ_{OUT} at the output is reset to zero. On the rising edge of the clock, the capacitor C begins to discharge through the NMOS transistors M_2, M_3 and M_4 at a rate that is governed by the input voltage V_{IN}. The output inverter (M_5 and M_6) acts as the comparator and senses when the capacitor voltage has surpassed the inverter threshold voltage. Based on HSPICE simulations, a sample voltage-to-time transfer characteristic of the circuit is shown in Fig. 2.11.b. Like Fig. 2.10.b, the linear range of operation for the input voltage is limited to a portion of power supply (i.e. from 0.8 V to 1.2 V). This constraint is the main obstacle for the input dynamic range of the circuits in TMSP.

Based on the information reported in [3], the direct voltage-control methodology offers the advantages of higher voltage-to-time conversion factor, $G_{ø}$, and better linearity with a larger input voltage range. The current-starved inverter approach boasts significantly better power consumption, silicon area usage, and a much higher operation bandwidth. The selection of a VCDU approach is strongly dependant on the design targets and the intended application.

2.2.2. Sample-and-Hold Action

Sample-and-hold (S&H) circuits are required in A/D conversion when the input voltage is a relatively high-frequency signal with respect to the ADC conversion process. A S&H block is a very expensive, power hungry and area consuming unit to implement. However, in TMSP circuits, a VCDU may act as a sampler provided its conversion time is sufficiently less than the period of the

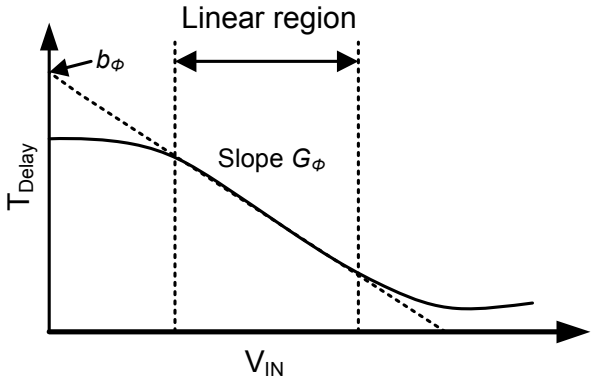


Fig. 2.12. The symbolic redraw of the voltage-to-time transfer characteristic shown in Fig. 2.11.b

input signal [11], i.e.

$$f_{IN} \le \frac{1}{\pi\left(2^D - 1\right)T_C} \tag{2.4}$$

where D, T_C, and f_{IN} represent desired resolution, maximum VCDU conversion time, and input signal bandwidth respectively. Any signal bandwidth violation from the above inequality equation will result in harmonic distortion.

2.2.3. Voltage-to-Time Converter and Adder

The voltage-to-time transfer characteristic shown in Fig. 2.11.b is re-drawn symbolically in Fig. 2.12. It is composed of linear and non-linear regions. Considering the linear region, the input-output delay behavior or time-difference is governed by the following equation:

$$T_{Delay} = t_{OUT} - t_{IN} = G_\phi V_{IN} + b_\phi \tag{2.5}$$

where, t_{OUT} and t_{IN} are arrival time for the output and input rising edges and $G_ø$ and $b_ø$ are the slope and the y-intercept of a line drawn through the linear region of the transfer characteristic. To make a linear relation between the input voltage and the input-output delay, the term $b_ø$ should be removed. A voltage-to-time converter (VTC) is required to transform differential voltage information into differential time-mode signals and cancel out the DC term, $b_ø$. Fig. 2.13.a presents the block diagram for a VTC. Mathematically, for a VTC configuration we can write the output equations as following:

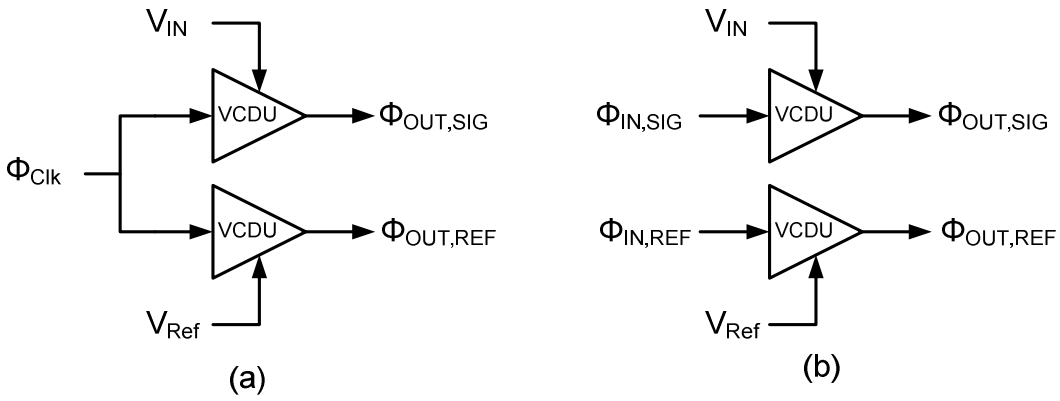


Fig. 2.13. (a) voltage-to-time converter, (b) voltage-to-time adder

$$t_{OUT,SIG} = t_{Clk} + G_\phi V_{IN} + b_\phi \tag{2.6}$$

$$t_{OUT,REF} = t_{Clk} + G_\phi V_{REF} + b_\phi \tag{2.7}$$

Defining the output of the differential VTC as ΔT_{OUT}, that is the time difference measured with respect to the reference time ($t_{OUT,REF}$), we subtract Eqn. (2.7) from Eqn. (2.6) to write

$$\Delta T_{OUT} = t_{OUT,SIG} - t_{OUT,REF} = G_\phi \left(V_{IN} - V_{REF}\right), \tag{2.8}$$

and

$$\Delta T_{OUT} = G_\phi \Delta V_{IN} . \tag{2.9}$$

Fig. 2.13.a might be easily converted to a voltage-to-time adder structure, as shown in Fig. 2.13.b. For a voltage to time adder configuration, Eqns. (2.6) and (2.7) change as follow

$$t_{OUT,SIG} = t_{IN,SIG} + G_\phi V_{IN} + b_\phi \tag{2.10}$$

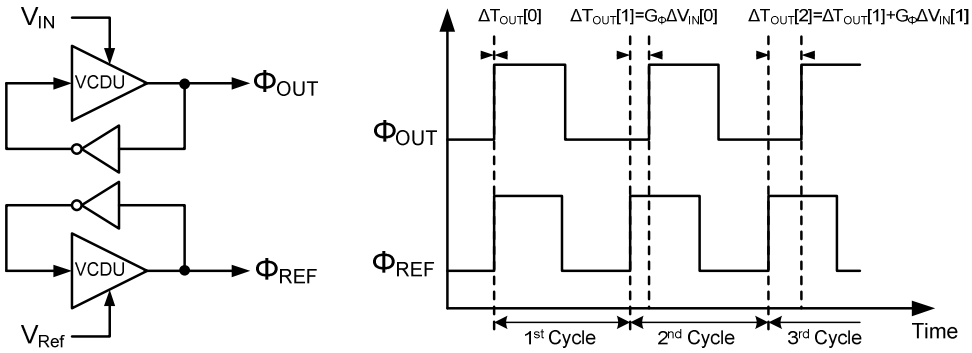
$$t_{OUT,REF} = t_{IN,REF} + G_\phi V_{REF} + b_\phi . \tag{2.11}$$

The time difference between the two output signals will be related to the time difference between the input signals as the following equation reveals,

$$\Delta T_{OUT} = t_{IN,SIG} - t_{IN,REF} + G_\phi \left(V_{IN} - V_{REF}\right) = \Delta T_{IN} + G_\phi \Delta V_{IN} . \tag{2.12}$$

2.2.4. Voltage-to-Time Integrator

By connecting the output of an adder to its input through an inverter, the voltage-to-time integration can be easily implemented. The result is the



(a) (b)

Fig. 2.14. Voltage-to-time integrator (a) circuit configuration, (b) signal representation

configuration of two ring oscillators as shown in Fig. 2.14.a. The frequency difference between the signal oscillator (top) and the reference one (bottom), due to $\Delta V_{IN}[n]$, is integrated into the phase difference between the two outputs of the oscillators as shown in Fig. 2.14.b and represented in [11] as following,

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + G_{\phi}\Delta V_{IN}[n-1]. \tag{2.13}$$

As a free-running or self-clocking system, no external clock is needed and just device sizing and input signal levels establish the oscillation frequency. As shown in Fig. 2.15, a dual-input or multi-input integrator may be created by including more VCDUs in the loop, controlled by voltages $V_{IN,1}[n], V_{IN,2}[n], \ldots, V_{IN,N}[n]$.

It would be very desirable to cascade two integrators, however, this cannot be done by the knowledge available in this field. Since a time-difference variable

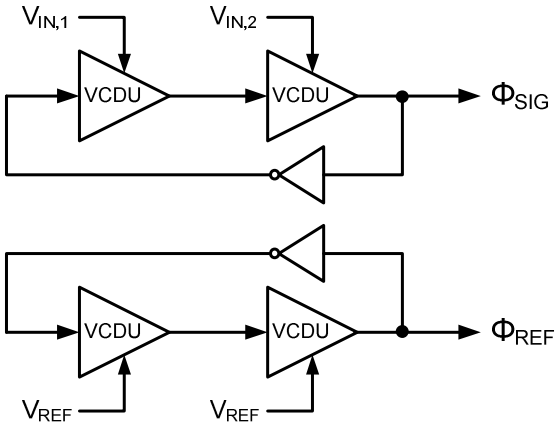


Fig. 2.15. A two-input time integrator

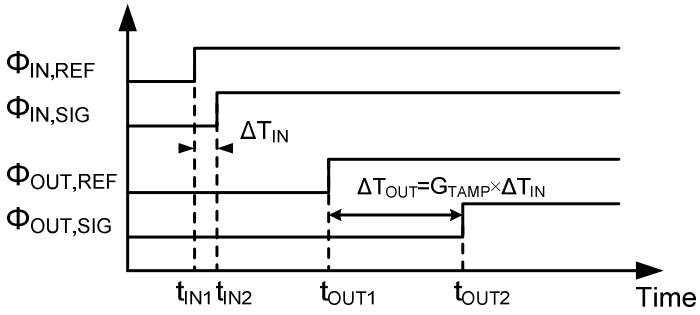


Fig. 2.16. A signal illustration of time-amplification

is not a physical stationary quantity, the summation of two time-difference variables cannot be done without first transforming them into an intermediate medium such as electrical charge. This constraint can forfeit some of the advantages of TMSP.

2.2.5. Time Amplifier

Time amplification is the process of scalar multiplication of a time-mode variable. It also can be interpreted as the expansion of the time difference between the two input rising edges. The signal illustration of time-amplification is shown in Fig. 2.16.

By now, two well-known designs for circuit implementations of time amplifiers have been reported. The first [12] is based on the mutual exclusive (MUTEX) circuit shown in Fig. 2.17. The cross-coupled NAND gates form a bi-stable circuit while the output transistors switch only when the difference in voltage between nodes V_1 and V_2, say ΔV, reach a certain value. The OR gate at the output is used to detect this switching action. Time amplification occurs when the input time difference is small enough to cause the bi-stable to exhibit meta-

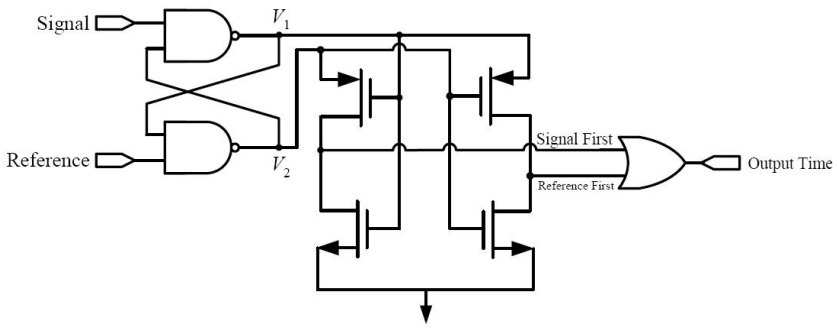


Fig. 2.17. A circuit implementation of time amplification

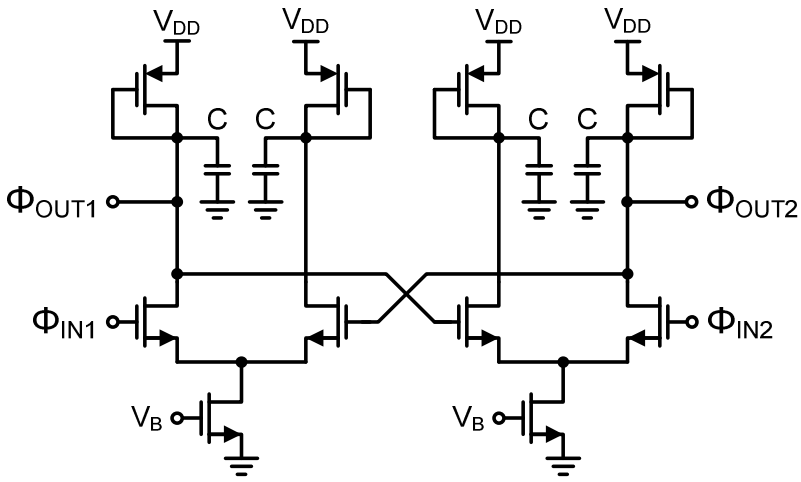


Fig. 2.18. The circuit scheme for a cross-coupled time-amplifier

stability. The transistors before the output OR gate form a positive feedback loop to increase the voltage difference between V_1 and V_2. This circuit is very compact, but its use is limited for very small input TM variables. Also, the accuracy and repeatability of this design are difficult to maintain due to process variation.

The second design, presented in Fig. 2.18 [13], consists of two cross-coupled differential amplifiers with capacitive and resistive loads. The design can achieve gains exceeding several-hundred s/s and the input time-difference can extend well into the nanosecond range. The input linear region is also controlled by the biasing current, and the capacitive and resistive loading. However, the common tradeoff of gain versus linearity and gain versus speed remain a consistent challenge within TAMP design.

2.2.6. Time Comparator

The comparison of two clock events can be easily performed by a D-type edge-triggered flip-flop (DFF), shown in Fig. 2.19.a, as following:

- If the rising edge at Φ_{IN} is leading the rising edge at Φ_{REF}, then the output D_{OUT} is logic 1.
- If the edge at Φ_{IN} is lagging the edge at Φ_{REF}, then the output D_{OUT} is logic 0.

The flip-flop meta-stability is an issue while attempting to make the correct

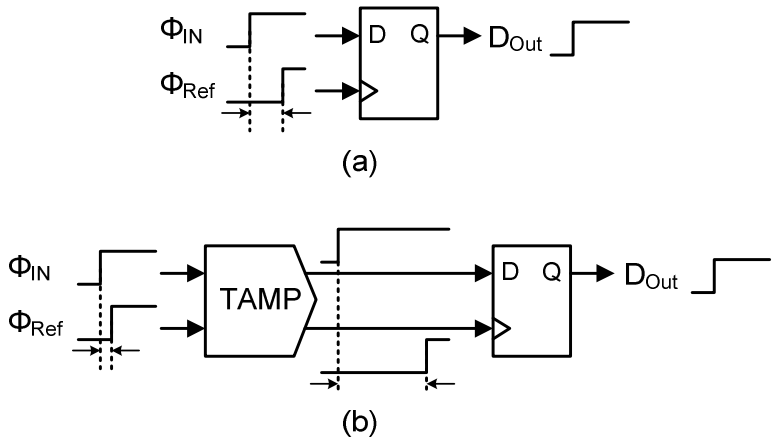


Fig. 2.19. (a) a D-Flip-Flop as a time comparator, (b) adopting time amplification to cover for DFF meta-stability

decision between two input clock events that are very close together. To reduce this non-ideality, time-amplifiers can be used to pre-amplify the input time-difference, as shown in Fig. 2.19.b, and eliminate the need for a DFF with a very sharp profile.

2.3. Time-Mode Analog-to-Digital Converters

The building blocks presented in the previous section can be utilized to develop practical circuits for applications such as data conversion. In this section, the previously reported designs to implement first-order delta-sigma modulation and VCO-based data converters will be reviewed.

2.3.1. First Order Time-Mode Delta-Sigma Modulator

Delta-sigma (ΔΣ) modulation is a unique and well-known technique in analog design and it has found its way into many applications [14]. The techniques to implement this kind of modulation range in complexity from first-order and single-bit designs to eighth-order [15] and four-bit [16] architectures. The operation of a first order single-bit ΔΣ modulator is best described with the error-feedback model shown in Fig. 2.20. At startup and considering zero initial conditions, the input value V_{IN} is converted into a digital signal through a comparator block. The digital output, D_{OUT}, is fed back and it is subtracted from the input V_{IN} to produce the error signal E_q, which will be added into the integrator output. By iteration and through the feedback loop, the error signal is minimized

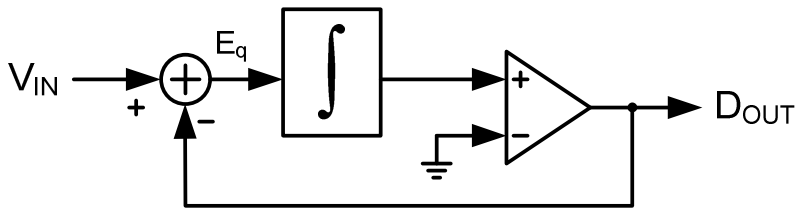


Fig. 2.20. The configuration of a first-order single-bit delta-sigma modulator

and the average value of D_{OUT} approaches V_{IN}. By adopting TMSP, the same functionality has been proved implemented using digital blocks [11]. The structure shown in Fig. 2.20 is composed of an integrator, a coarse quantizer, and an adder. In previous sub-sections, the counterparts of these building blocks in TMSP have been presented; by arranging these blocks, the structure of a first-order delta-sigma modulator is shown in Fig 2.21. The experimental results reported in [11] prove the superior advantages of TMSP as less area, less power and the digital nature of the circuitry.

Due to the constraints associated with the summation of two TM variables, it is not known how to cascade two integrators in order to implement higher orders of delta-sigma modulators. This topic as one of the main constraints of TMSP will be investigated more over the rest of this thesis.

2.3.2. VCO-Based Data Converters

VCO-based data converters utilize TMSP through frequency modulation to implement non-feedback noise-shaping architectures [17]. To explain how such a modulator works, we may start by looking at the block diagram of a discrete-time

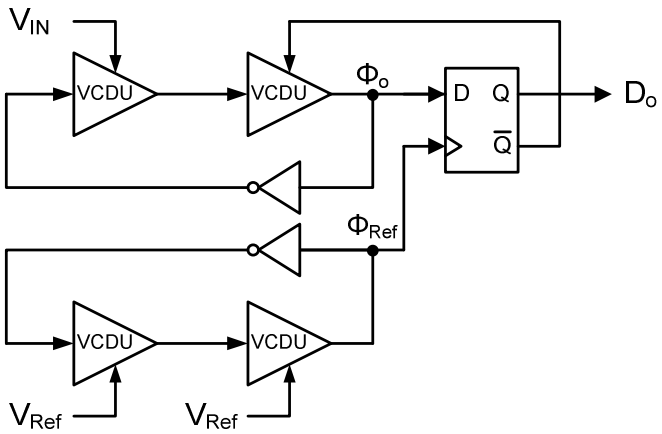


Fig. 2.21. The configuration of a first-order single-bit delta-sigma modulator

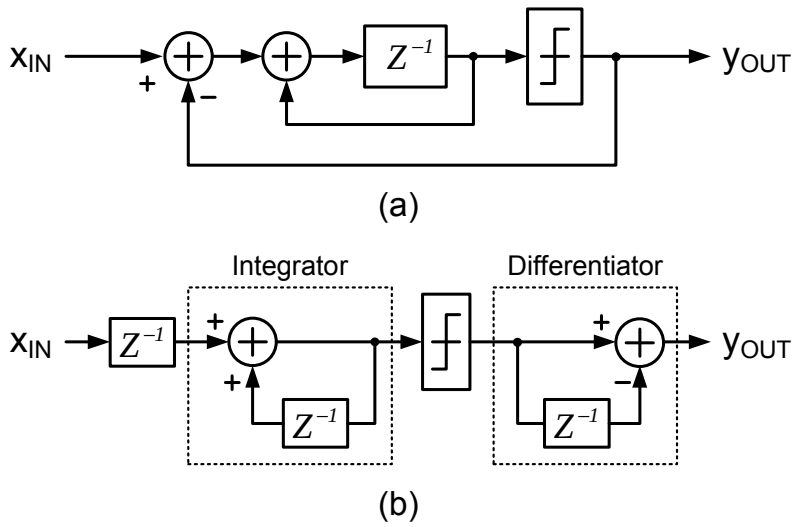


Fig. 2.22. The block diagram for a (a) discrete-time delta-sigma modulator, (b) non-feedback delta-sigma modulator

delta-sigma modulator shown in Fig. 2.22.a. The output may be expressed as

$$y_{OUT}[n] = q\left(\sum_{k=-\infty}^{n-1}\left(x_{IN}[k] - y_{OUT}[k]\right)\right); \tag{2.14}$$

where, $q(\ )$ represents the nonlinear quantizing function. Since $y_{OUT}[k]$ is already quantized, it may be resolved from the quantizing function and represented as

$$\sum_{k=-\infty}^{n} y_{OUT}[k] = q\left(\sum_{k=-\infty}^{n-1} x_{IN}[k]\right), \tag{2.15}$$

which is equivalent to

$$y_{OUT}[n] = q\left(\sum_{k=-\infty}^{n-1} x_{IN}[k]\right) - q\left(\sum_{k=-\infty}^{n-2} x_{IN}[k]\right). \tag{2.16}$$

The corresponding non-feedback equivalent block diagram is illustrated in Fig. 2.22.b. This structure illustrates the simple principle of the first-order non-feedback delta-sigma modulation. After the unit delay, the input signal is forwarded to an integrator followed by a quantizer. The output of the quantizer is then passed through a differentiator. Since the quantization error is not integrated, it will be differentiated while the input signal passes unchanged. *STF*(*z*) and *NTF*(*z*) of the non-feedback structure will follow the same pattern as expected from a first-order delta-sigma modulator.

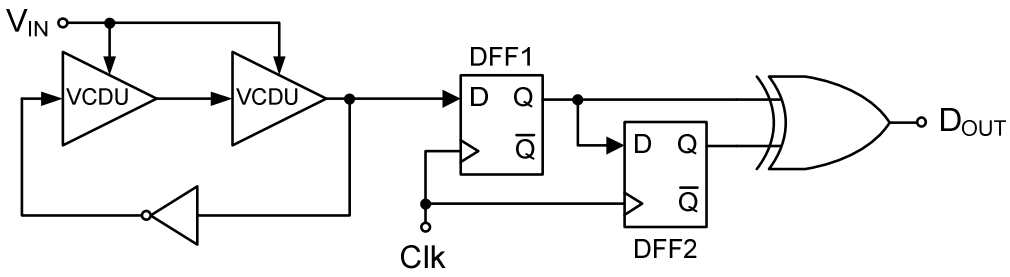


Fig. 2.23. First-order single-bit VCO-based ADC

A circuit diagram to implement a first-order single-bit VCO-based delta-sigma modulator is shown in Fig. 2.23. The integrator is implemented using a voltage to time integrator while DFF1 represents the quantizer. The differentiator is easily accomplished with another D-type Flip-Flop (DFF2) implementing the delay and a XOR gate performing the modulo-2 subtraction; so that, the equation for the digital differentiator is equal to

$$D(z) = \left(1 - z^{-1}\right). \tag{2.17}$$

The attractive architecture of the initial non-feedback structure (Fig. 2.23) has motivated some research on VCO-based data converters. In [18], an energy-efficient VCO-based architecture operating in the sub-threshold region was implemented; also, a comprehensive survey on the behavior and analysis of this kind of an ADC is presented in [19]. The digital implementation of non-feedback VCO-based ADCs, however, is limited to first order noise shaping. Any attempt to increase the number of the output bits has been associated with the inclusion of analog building blocks. For example, in [20] and [21], a third-order noise-shaping ADC is realized by employing a feedback loop using two current DACs and an op-amp.

In a first-order VCO-Based data converter, however, the main drawback is that due to the lack of feedback all non-idealities in the frequency modulator will be added directly to the signal. In addition, due to non-uniform sampling there will be strong harmonic components at the output of the modulator that necessitates adopting some calibration techniques to compensate for the accumulated nonlinearity [19].

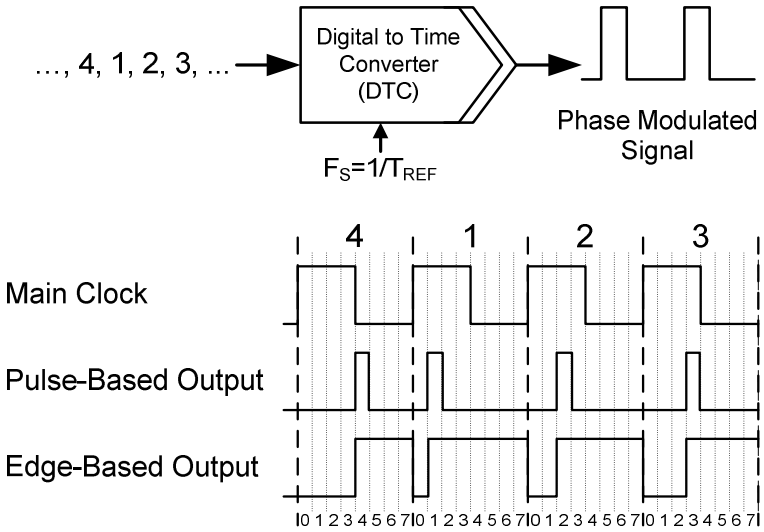


Fig. 2.24. The symbol and the signal waveform for both pulse-based and edge-based outputs due to the pre-specified digital inputs

2.4. Digital-to-Time Converter (DTC)

Data conversion is simply the process of working with signals in different number domains. As shown in Fig. 2.2, our numerical model includes the new domain of time that represents the domain of real numbers like analog quantities. The information in time domain is produced and handled by the basic building blocks previously presented in this chapter together with other typical logic cells; however, digital to time (DTC) and time to digital (TDC) converters are needed to make TMSP applicable to a variety of applications that necessitate the switching between different domains.

A digital-to-time converter takes a digital input and converts it to the form of a time instant, i.e. a pulse in a specific time slot. It might be considered equivalent to a phase modulated (PM) signal, as shown in Fig. 2.24. The phase difference between the output pulse and the clock signal will be the analog equivalent of the input digital code. As sequential logic is edge-based, we can replace the pulse with an edge placement as shown in the same figure as above.

2.4.1. Delay-Locked Loop (DLL)

A delay-locked loop (DLL) is a servomechanism in which a path of VCDUs

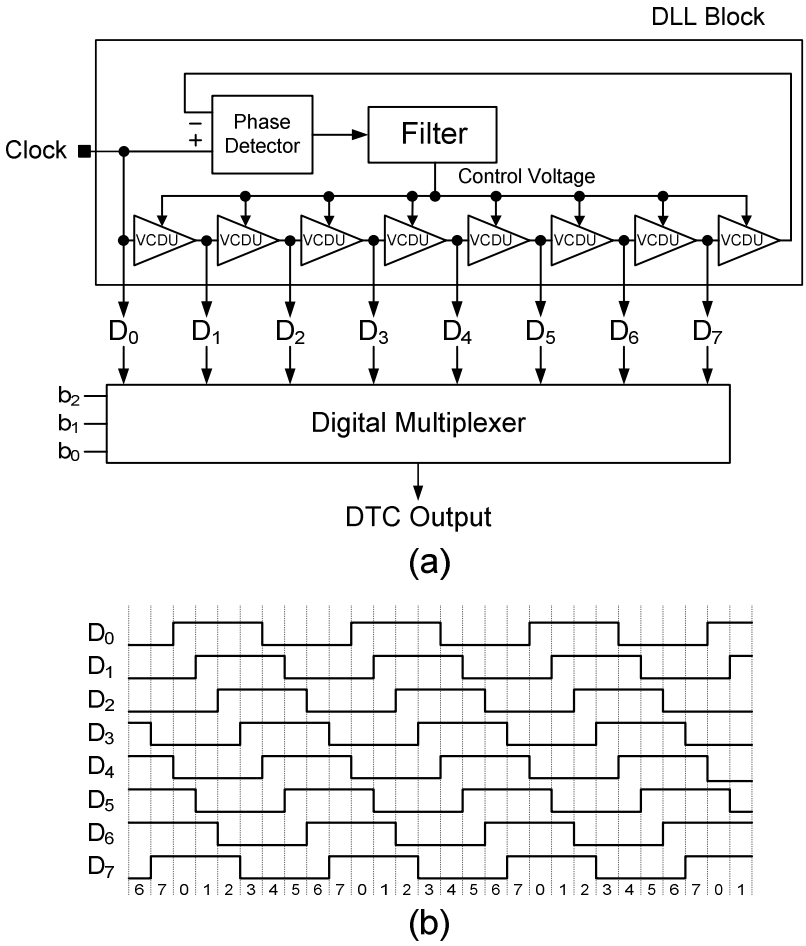


Fig. 2.25. (a) The block diagram for a DLL followed by a digital multiplexer, (b) the signal waveform of the output nodes of a DLL

is adjusted in order to produce a desired phase relationship between two signals [22-24]. Shown in Fig. 2.25.a, a chain of delays is used to delay the input clock signal. The delayed signal is compared to itself and the phase difference is extracted. The phase detector output is used to control the input voltage of the VCDUs in the delay chain through a negative feedback loop. Regarding the number of delays, each node presents the input clock delayed by a determined portion of the clock period, as shown in Fig. 2.25.b.

DLLs have been widely used as clock de-skewing circuits in radio frequency (RF) transceivers [25], inter-chip communication interfaces [26], and clock distribution networks to improve overall system timing [27]. Although these functions can also be performed with phase-locked loops (PLLs), DLLs are often preferred due to their ease of design, better immunity to on-chip noise, and

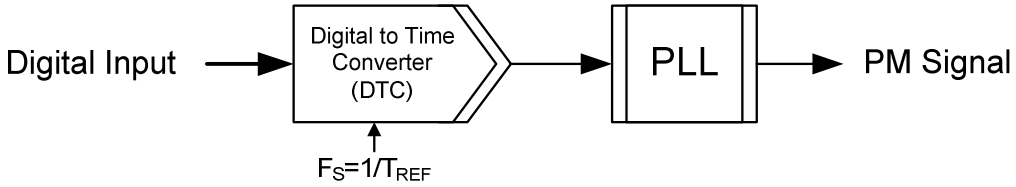


Fig. 2.26. Band limiting DTC output using a PLL

stability. A DLL incorporated with a digital multiplexer, as shown in Fig. 2.25.a, operates as a time-to-digital converter. For a 3-bit converter, the digital input selects one out of the eight delayed versions of the input clock. Since the delay is controlled through a feedback loop in the DLL, fine results are achieved.

2.4.2. Band limiting DTC Output

A digital signal has a periodic spectrum, i.e. it extends to infinity. The output of a DTC contains the periodic digital signal spectrum, sampled-and-held and convolved with the spectrum of the reference clock. As shown in Fig. 2.26, to limit the frequencies of interest to the Nyquist interval, the DTC output is passed through a Phase Locked Loop (PLL) with a desired bandwidth.

PLL is a control system [28], as shown in Fig. 2.27, that by using negative feedback generates an output signal with different frequency but in phase with the reference signal at the input; so, the phase of Φ_{IN} is supposed to be equal to that of Φ_{OUT}. A filter is required in the loop to configure the frequency response of the system (stability). Although locking transient is a non-linear phenomenon, any PLL might be approximated to a linear continuous time feedback system as shown in Fig. 2.28. The open loop transfer function of the feedback loop is modeled as following

$$H_O(s) = K_{PD} G_{LPF}(s) \frac{K_{VCO}}{s}; \tag{2.18}$$

where, K_{PD}, $G_{LPF}(s)$, and K_{VCO} are the gain of Phase Detector (V/rad), the transfer function of loop filter (V/V), and the gain of VCO (Hz/V) respectively. For a first-

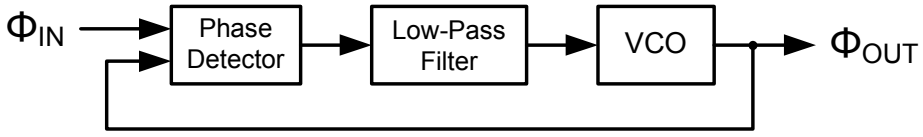


Fig. 2.27. Block diagram of a PLL

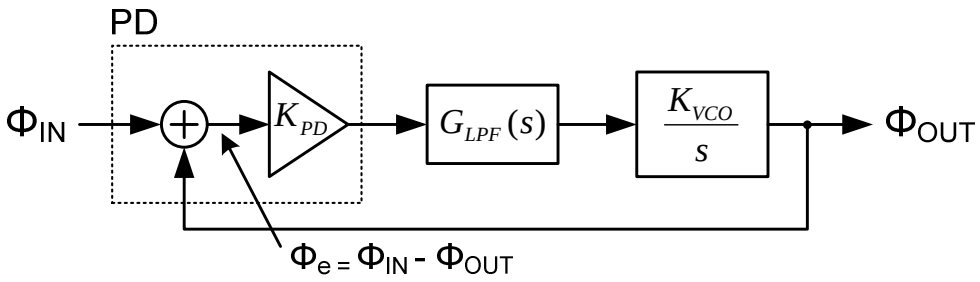


Fig. 2.28. The linear model for a PLL

order low-pass filter, the input-output transfer function will be

$$H(s)=\frac{H_O(s)}{1+H_O(s)}=\frac{\Phi_{OUT}(s)}{\Phi_{IN}(s)}=\frac{K_{VCO}K_{PD}}{\frac{s^2}{\omega_{LPF}}+s+K_{VCO}K_{PD}}. \tag{2.19}$$

So, $H(s)$ is a low-pass function. As s ($=j\omega$) approaches 0, i.e. slow phase changes, the response of the PLL gets close to unity and the phase change at the input is directly translated to the output. On the other hand, for fast phase changes in the input excess phase, the output excess phase varies more slowly. For the input reference signal at carrier frequency, ω_C, with phase noise φ_n [i.e. $x(t)=A\cos(\omega_C t+\varphi_n(t))$] and the locked output signal [$y(t)=A\cos(\omega_C t+\Phi_{out}(t))$], the noise transfer function will be the same as a typical PLL closed-loop transfer function as following

$$H(s)=\frac{\Phi_{OUT}(s)}{\varphi_n(s)}=\frac{\omega_n^2(1+s/\omega_z)}{s^2+2\zeta\omega_n s+\omega_n^2}. \tag{2.20}$$

Apparently, $H(s)$ is a low-pass function; where, the phase noise at the frequencies close to the carrier will be unaffected; however, the phase noise at frequencies far from the carrier frequency will be attenuated at the output.

The above analysis shows that a PLL can be used as a primary filter for time-mode variables. Since the initial motivation behind a PLL block is not TM filtering, this application accompanies some drawbacks. At first, there are several noise sources, like PD, loop filter, VCO, and frequency divider, to introduce phase noise at the output. The noise contribution by these sources will be transferred directly to the output phase. Although the phase noise is rejected outside the loop bandwidth, it will be unaffected within the bandwidth plus the

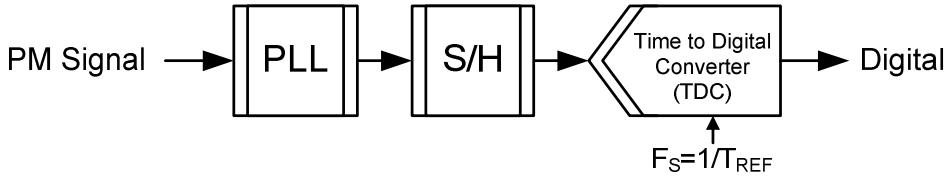


Fig. 2.29. The process of time to digital conversion including anti-aliasing filtering

additive extra noise from the PLL. Second, higher orders of filters are not practical yet and it necessitates more research; also, as a rule of thumb, a better time-mode filter needs a slower PLL; so, there is a critical trade-off between noise reduction and bandwidth.

2.5. Time to Digital Converters (TDC)

A TDC is responsible for converting a time interval between two rising edges into a digital number. As with all sampling processes, the continuous time signal must be band limited to prevent aliasing effects. To band limit the PM input signal, one method is through the application of a PLL (shown in Fig. 2.29), as explained in the previous section.

In the following sub-sections, previously reported topologies to implement a time-to-digital converter will be reviewed.

2.5.1. Single Counter

The simplest of the TDC architectures is the one shown in Fig. 2.30. In this converter, the input time interval, ΔT, between the rising edges of Φ_{Start} and Φ_{Stop} is measured by a counter running on a high-frequency reference clock. The AND gate ensures that the counter is enabled only when the input waveforms Φ_{Start}

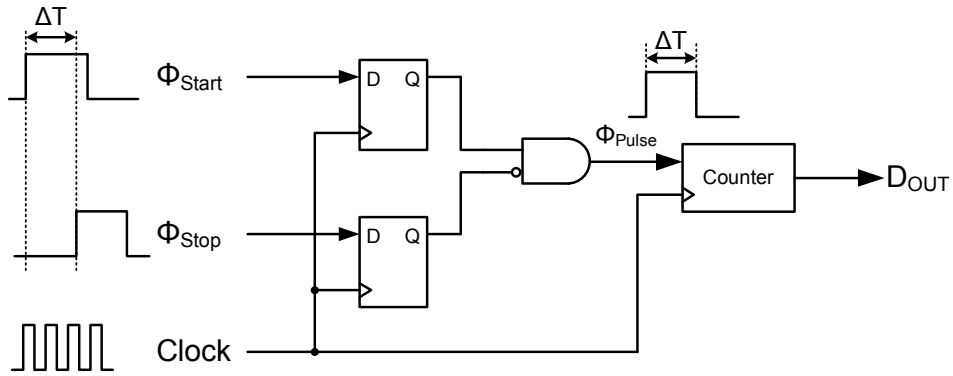


Fig. 2.30. Using a counter as the simplest TDC

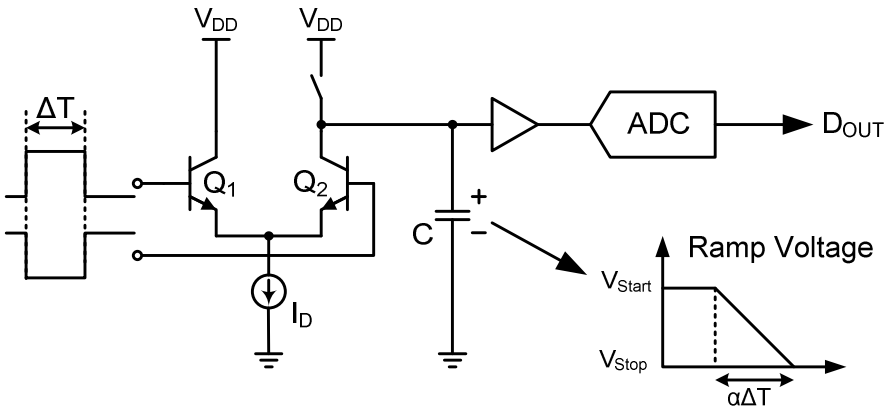


Fig. 2.31. The circuit diagram of an interpolating TDC

and Φ_{Stop} are logically different. The method is very simple to implement, however, the resolution attained by this method is largely dependant on the clock frequency and it can be no higher than a single clock, as presented by the following equation,

$$\Delta T = N \cdot T_{\mathrm{Clk}} = \frac{N}{f_{\mathrm{Clk}}}, \tag{2.21}$$

where T_{Clk} is the period of the running clock and N is the number of clock cycles during the ΔT.

2.5.2. Interpolating TDC

Interpolation is based on the discharge of a pre-charged capacitor using the constant current source I_D [29,30]. The final voltage on the capacitor, V_{Stop} in Fig. 2.31, is proportional to the duration of the input pulse ΔT; it controls how long current I_D is used to discharge the capacitor C. The ADC measures voltage difference on the capacitor. Based on the pre-known values for the discharging current (I_D) and the capacitor value (C) in addition to the measured value of V_{Stop}, the time difference ΔT can be estimated. This method can achieve a very wide dynamic range and a low-frequency ADC is needed; however, it relies on the absolute value of C and it requires a very high-resolution ADC.

A modification to the interpolating TDC is shown in Fig. 2.32 [31]. It does not rely on the actual capacitor value since the capacitor is now charged at a known rate and then it is discharged at a different but still known rate. In this method, pulse stretching is adopted to make the original pulse to be measured

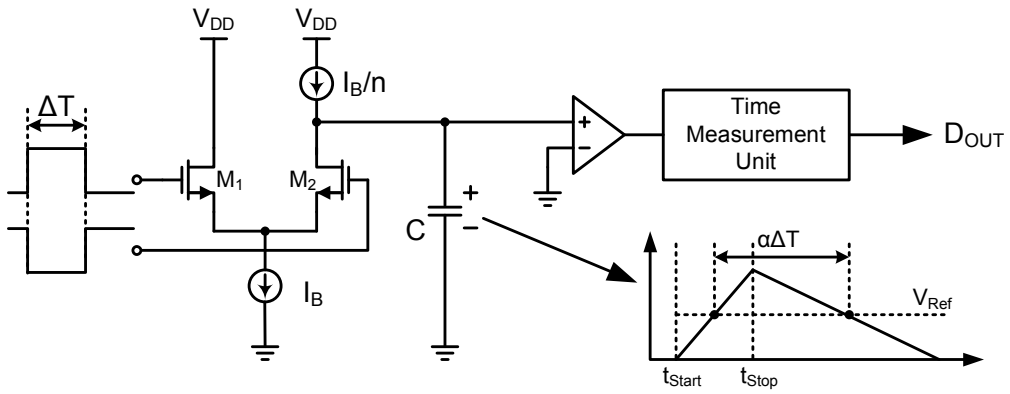


Fig. 2.32. The circuit diagram for an interpolating TDC insensitive to C value

much larger; also, it makes the task of quantization unit much easier. A 1-bit ADC, as simple as a comparator, might be used to detect the threshold crossing times; also, the time measurement unit (TMU) can be as simple as a counter. However, the structure is very power hungry for a narrow pulse width and the overall resolution is determined by the TMU.

2.5.3. Flash TDC

Flash TDCs are analogous to flash ADCs for voltage amplitude encoding. This kind of TDC compares a signal edge with respect to various reference edges all displaced in time. The elements that compare the input signal to the reference

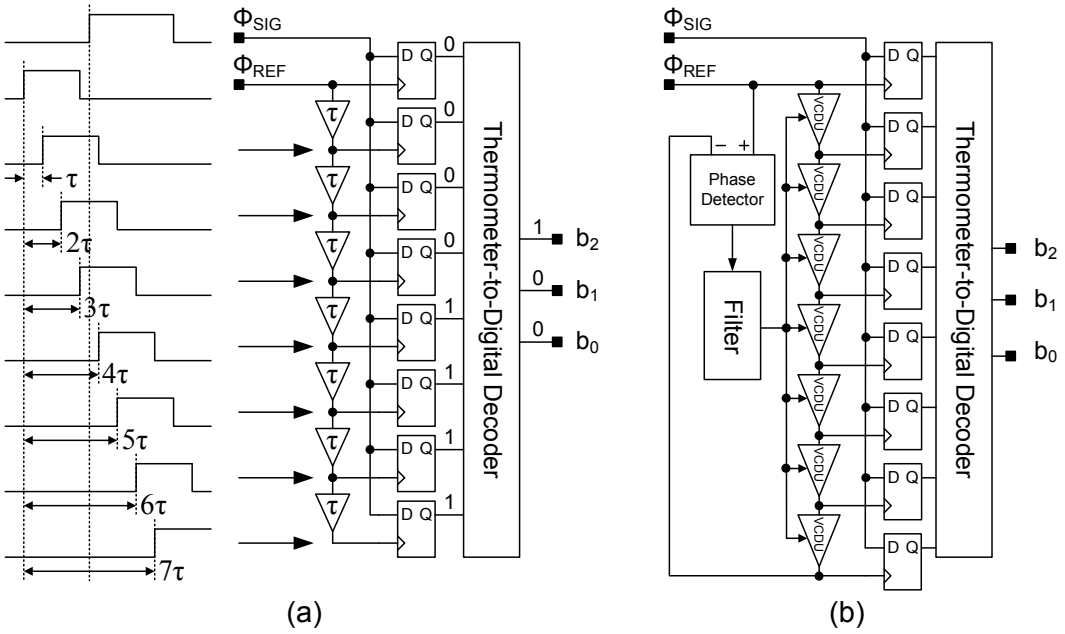


Fig. 2.33. The block diagram of (a) single delay chain flash TDC, (b) fine flash TDC adopting DLL

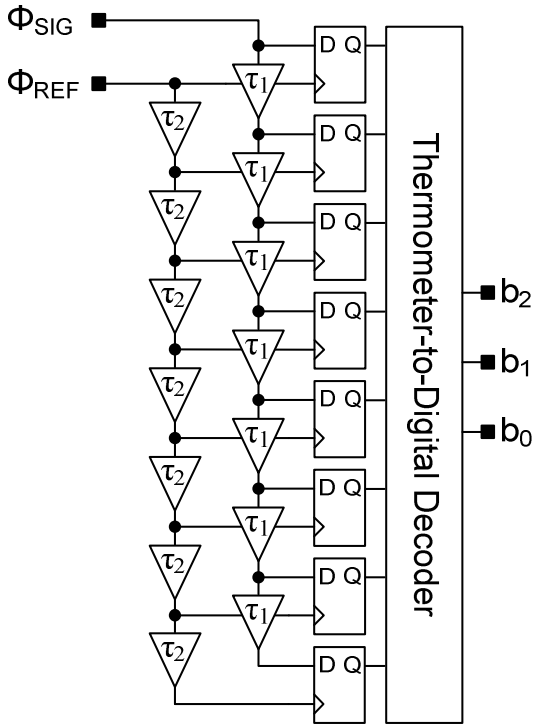


Fig. 2.34. Adopting Vernier delay line to refine the time resolution of a flash TDC

are usually D-type flip-flops. In the single delay chain flash TDC shown in Fig. 2.33.a, each buffer produces a delay equal to τ. To ensure that τ is known reasonably accurately, the delay chain is often implemented and stabilized by a DLL [32,33], as shown in Fig. 2.33.b.

To determine the time difference ΔT between the input rising edges Φ_{SIG} and Φ_{REF} by the 8-level delay chain converter in Fig. 2.33.a, each flip-flop compares the displacement in time of the delayed Φ_{REF} to that of Φ_{SIG} waveform. The thermometer-encoded output indicates the value of ΔT, assuming the flip-flops are given sufficient time to settle. The drawback to this implementation is that the temporal resolution can be no higher than the delay through a single gate in the semiconductor technology used. To achieve sub-gate temporal resolution, the flash converter can be constructed with a Vernier delay line [34,35] as shown in Fig. 2.34. This architecture achieves a resolution of τ_1-τ_2, where $\tau_1 > \tau_2$. Again, two individual DLLs should be implemented for each delay chain to make them reasonable accurate.

Flash TDCs are well suited for use in on-chip timing measurement

systems, because they are capable of performing a measurement on every clock cycle and can be operated at relatively high speeds. In addition, they can easily be constructed in any standard CMOS process, because they are composed of solely digital components.

2.5.4. Vernier Oscillator

A component-invariant Vernier oscillator TDC with phase detector shown in Fig. 2.35 is composed of two ring oscillators producing plesichronous square waves to quantize a time interval based on a very small frequency difference between the two oscillators; this difference is due to the different delays introduced by the VCDU in each oscillator [36-38]. The rising edges at Φ_{Start} and Φ_{Stop} enable the oscillators. The phase detector and the counter measure the time difference between these two rising edges by detecting the instant one edge catches up with the other. Due to its small size and relatively high temporal resolution, the Vernier oscillator is amenable for use in on-chip test systems. Phase locking the delay elements using a DLL can correct for any process variations and temperature effects in the delay of $VCDU_s$ and $VCDU_f$. In addition, the use of the oscillators reduces the matching requirements on the delay buffers used to quantize a time interval. This feature is used to overcome the temporal uncertainties caused by component variation in the delay lines of Vernier delay flash TDCs.

However, one negative aspect of this architecture is that it takes many cycles to complete a single measurement (i.e., has a long dead time). Compared

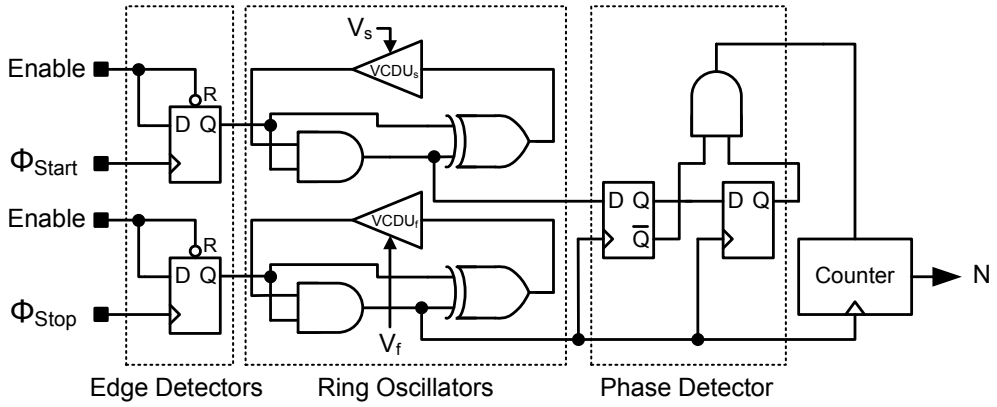


Fig. 2.35. The block diagram for a Vernier oscillator TDC

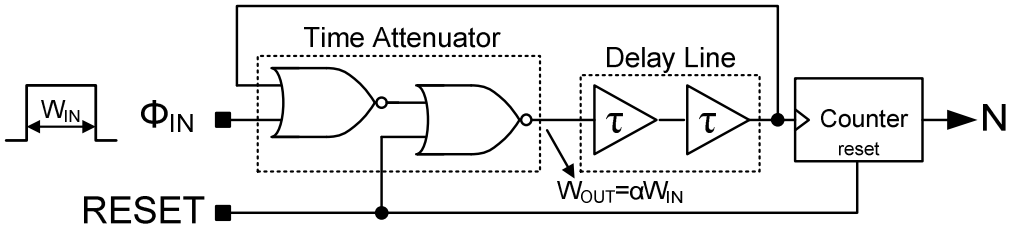


Fig. 2.36. The block configuration for a cyclic pulse-shrinking TDC

to flash converters that can make a measurement every cycle, the Vernier oscillator requires a long conversion time.

2.5.5. Cyclic Pulse-Shrinking TDC

Through the application of a time attenuator or pulse-shrinking circuit in a feedback loop, a TDC can be created [39], as shown in Fig. 2.36. An input pulse of width W_{IN} is reduced by some scale factor α as it propagates around the feedback loop; eventually, the pulse width disappears. As the rising edge of the pulse reaches the counter, a count is made until the pulse disappears. The inverter chain is used to set the feedback delay to be longer than the pulse duration, so that the pulse-shrinking element operates on only one signal at a time (i.e. the input on the first cycle and the feedback signal on all other cycles). Mathematically, we can write a difference equation of system behavior as:

$$W_{OUT}[n] = \alpha \times W_{OUT}[n-1] \tag{2.22}$$

where, $W_{OUT}[0]=W_{IN}$. The general solution can then be found as

$$W_{OUT}[n] = \alpha^{n} \times W_{IN} \tag{2.23}$$

The output counter counts until the final pulse width violate the hold time of the counter; so, the number counted by the counter will be a representative of the input pulse width. Similar to Vernier oscillator there is a long conversion time required for the cyclic pulse-shrinking TDC.

2.6. All Digital Phase Locked Loop (ADPLL)

PLL is a key block used for both up-conversion and down-conversion of radio signals. It has been traditionally based on a charge-pump structure [28], which is not easily amenable to scaled CMOS integration and suffers from high

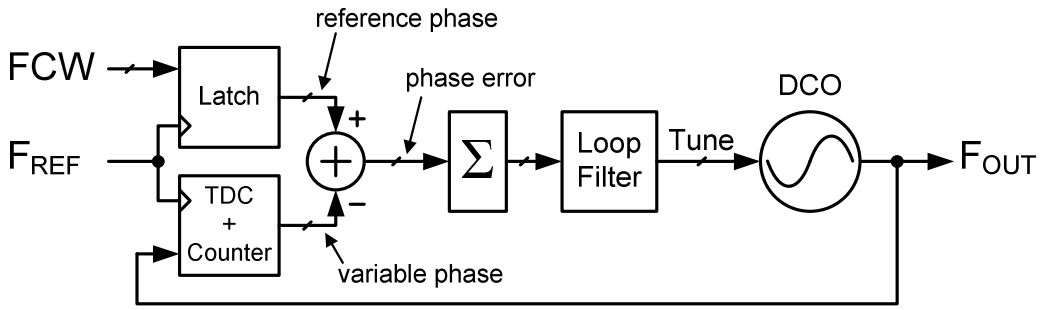


Fig. 2.37. The block diagram for an all-digital time-mode PLL based on TDC and DCO

level of reference spurs generated by the correlative phase detection method [40]. A digitally controlled oscillator (DCO), which deliberately avoids any analog tuning voltage controls, was proposed and demonstrated for Bluetooth [41] and GSM [42] applications. This allows a full digital implementation of PLL loop control circuitry as first was proposed in [43] and then it was demonstrated as a novel digital-synchronous phase-domain All-Digital PLL (ADPLL), as shown in Fig. 2.37, in commercial single-chip Bluetooth [44] and GSM [45] radios. Since the conventional phase/frequency detector and charge pump are replaced by a time-to-digital converter (TDC) [46], the phase-domain operation does not fundamentally generate any reference spurs thus allowing for the digital loop filter to be set at an optimal performance point between the reference phase noise and oscillator phase noise.

To explain how the ADPLL works, a new term called frequency command word (*FCW*) is introduced which is defined as

$$FCW = \frac{F_{OUT}}{F_{REF}}. \tag{2.24}$$

The operation of the block is dedicated to the comparison of the desired *FCW* together with the real ratio between the output and the reference frequencies. As shown in Fig. 2.37, a TDC is adopted to measure the phase difference between the rising edges of the reference and output signals. The normalized version of this phase difference will be compared to *FCW=1*. For greater values of *FCW*, the ratio of the frequencies includes integer and fractional parts. The integer part will be easily calculated as the number of the output rising edges during one period of

the reference clock and the fractional part is measured using the TDC. By detecting the difference between the measured frequency ratio and the intended *FCW*, a DCO is utilized for frequency modification of the signal at the output of the ADPLL and in a negative feedback configuration.

In the ADPLL, however, the digitally controlled oscillator (DCO) and TDC quantize the time and frequency tuning functions, respectively, which can lead to spurious tones and phase noise increase. As such, finite TDC resolution can distort data modulation and spectral mask at near integer-N channels, while finite DCO step size can add far-out spurs and phase noise; also, a major under-reported issue is an injection pulling of the DCO due to harmonics of the digital activity at closely spaced frequencies, which can also create spurs. In [47], the authors have addressed all these problems and RF performance matching that of the best-in-class traditional approaches. More challenging designs adopting ADPLL are reported in [48-51].

2.7. Additional Building Blocks Essential for TMSP

The previously reported circuitries adopting TMSP have been mostly restricted to the application of data conversion. This method has never been considered as a new monolithic methodology for analog design and, in most applications, TM variables are included just as some intermediate-stage variables. To extend the application of TMSP to implement other well-known analog topologies (such as second order delta-sigma modulators, filters, etc.), the lack of some key features is the most serious obstacle.

The lack of the crucial ability to perform the summation of two TM variables makes the main constraint to contemplate TMSP as a powerful processing tool. First valuable research avenue is to exhaust the search for this TMSP function in order to extend TMSP into a general signal-processing tool.

The other limitation is the non-stationary nature of the variables passing through the blocks. Since a TM variable is the time difference between two edges and any edge is a transient concept, to have a successful operation between two operands, it is essential to latch the first input operand and keep it until the other one arrives. To make this possibility available, the next priority should be

assigned to develop a memory cell dealing with TM variables. Without this feature, the synchronization of all the variables with a reference clock will be unavoidable which complicates the design procedure and makes it the main concern and disadvantage about TMSP.

The investigation and modification of VCDU as a crippling component in TMSP is the third priority to extend the application of TMSP into different areas. Since VCDU is the main block to perform the transformation from voltage domain into time domain, its nonlinear behavior restricts the effective resolution of all designs to within 7 to 9-bits [3]. To get more advantages, the linearization of the VCDU at the entry point will be an important advancement. Particularly at low-voltage power supplies, it is very critical to expand the linear range of VCDU as much as possible to maximize the dynamic range.

Satisfying the three above-mentioned milestones, an infrastructure will be available for the expansion of TMSP. Through this infrastructure, well-known topologies might be implemented adopting TMSP to take advantage of digital design while keeping a track of analog precision.

2.8. Summary

This chapter has briefly summarized the primary definitions, operating principles, and basic building blocks necessary to understand time-mode signal processing. The discussion applies to all DTCs and TDCs as well as typical designs operating with time-mode variables. DLLs and PLLs are reported for fine-tuning and band limiting of TM data converters. Due to the non-stationary nature of time, the summation of two time-mode variables is being considered as a serious constraint to develop the application of TMSP to more frequently used architectures like filters and delta-sigma modulators of higher orders.

The digital architectures of the reported circuitries emphasize on digital design simplicity and analog accuracy. It helps to re-design analog applications in a dramatically different environment. By adopting new techniques as cheap as digital routines, the digital background can also revolutionize the test methods used to verify the fabrication results for analog chips.

In subsequent chapters, additional techniques will be proposed to develop the application of TMSP as a strong monolithic processing tool for analog variables while all building blocks are being implemented in digital environment.

Chapter 3: Storage, Addition, and Subtraction of Time-Mode Variables

3.0. Introduction

Time-mode signal processing (TMSP) is a novel approach to manipulate and process analog information using digital blocks. Adopting this methodology, where conventional voltage and current variables are being replaced by time-mode (TM) variables, logic circuits can substitute the power hungry analog blocks. By moving to digital building blocks, the ease of digital design and the precision of analog processing will be integrated into affordable circuitries.

Because time is not a physical quantity, the summation and subtraction of two time-mode (TM) variables cannot be done without first transforming them into an intermediate medium such as voltage [52]. This transformation necessitates the adoption of analog blocks for signal processing thus forfeiting the digital advantage of TMSP. A recent development that attempts to circumvent this problem was presented in [53]. There, the authors claim a digital technique for time summation; however, the technique is limited to addition of a single TM variable together with the phase of a running oscillator and it cannot be considered as a general method.

In this chapter, an intensive research has been presented to introduce practical solutions for the implementation of basic functions among time-mode variables. Latching (storage), addition, and subtraction of TM inputs, as the most fundamental operations in any application-oriented topologies like delta-sigma modulators and filters, will be covered.

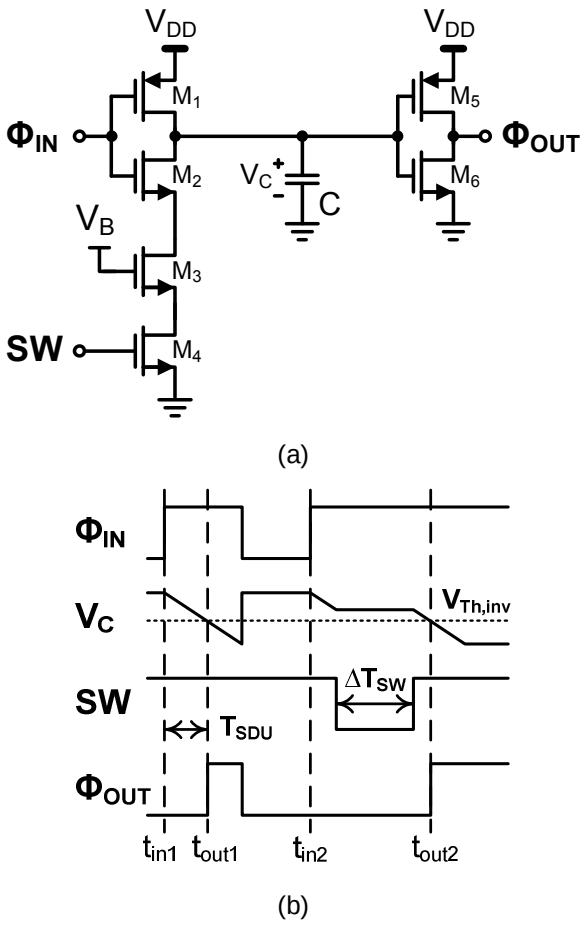


Fig 3.1. A switched-voltage delay unit (SDU): (a) schematic, (b) timing waveforms.

3.1. Switched Delay Unit (SDU)

Voltage-controlled delay units are frequently used in TMSP to introduce controlled delays. For the most part, such delays are realized by varying the time constant of a charging/discharging process [11]. In this chapter, the idea of a switched-delay unit (SDU) is used whereby the time-constant associated with the discharging process is kept constant but interrupted through the application of an on-off switch. The schematic for a switched delay unit (SDU) used in this work is shown in Fig. 3.1.a. Transistors M_1, M_2 and M_3 with capacitor C, form the core of a typical voltage-controlled delay cell and M_4 provides the on-off control of the discharging process. An additional inverter is used to buffer the discharging node from any loading effect at the output.

To gain an understanding of how this cell works, consider capacitor C is

pre-charged to V_{DD} and the input to the *SW* terminal is set to a logical high. On the arrival of a rising edge at Φ_{IN}, say at time t_{in1}, the voltage across C starts to discharge through transistors M_2-M_4. This, in turn, causes the output of the inverter Φ_{OUT} to trigger from a low to high state some later time, say at t_{out1}. The delay between the rising edges at Φ_{IN} and Φ_{OUT} (denoted as T_{SDU}) is fixed and equal to

$$T_{SDU} = \frac{C \times \left(V_{DD} - V_{Th,inv}\right)}{I\left(V_B\right)} \tag{3.1}$$

where $I(V_B)$ is the discharging current controlled by V_B. Here $V_{Th,inv}$ represents the threshold voltage of the output inverter.

The capacitor will again be pre-charged by returning the input Φ_{IN} to the logic low state. At the time of the next rising edge at Φ_{IN}, say at t_{in2}, the voltage across C will again start to discharge. However, if M_4 is switched off before the inverter is triggered, the discharge process will stop and the residual charge stored on C will be held indefinitely (neglecting any leakage effects). If the *SW* input to M_4 is returned high and the discharge process resumes, then on reaching the inverter threshold, the output will go high, say at time t_{out2}. As shown in Fig. 3.1.b, this interruption extends the input-output delay according to

$$t_{out2} - t_{in2} = T_{SDU} + \Delta T_{SW} \tag{3.2}$$

where ΔT_{SW} is the time that the signal *SW* remains low. During the time the discharge path is disconnected, the effective delay of the SDU increases to infinity.

To achieve an acceptable level of accuracy, the non-ideal switching behavior of a CMOS transistor should be monitored carefully. The charge

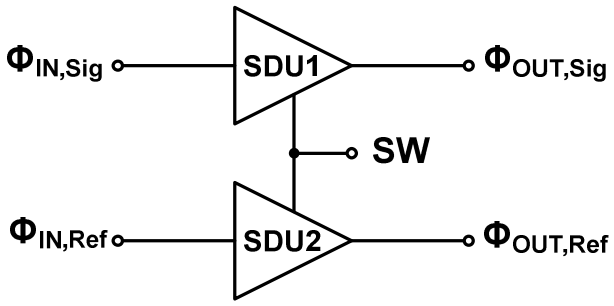


Fig 3.2. The differential SDU

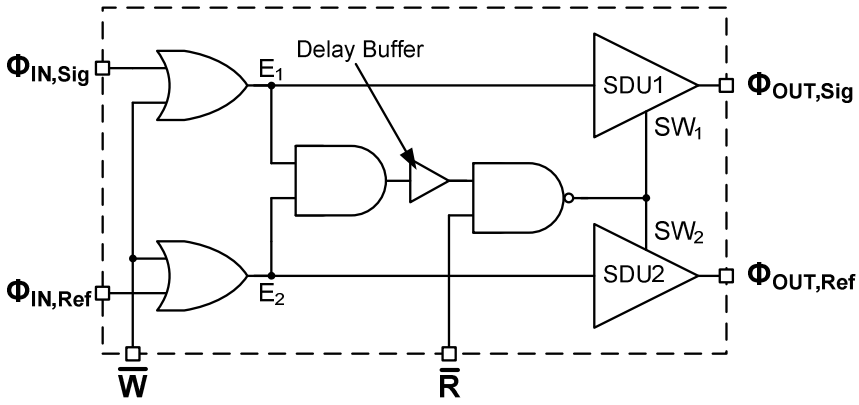


Fig. 3.3. The logic diagram of the proposed time latch (TLatch)

injection and the non-ideal behavior of the switches in the discharge path introduce an error term, T_{Error}, in Eqn. (3.2) as

$$t_{out2} - t_{in2} = T_{SDU} + \Delta T_{SW} + T_{Error} . \tag{3.3}$$

The charge injection, the drift current through the discharge path, the sub-threshold current induced by transistors $M_{1\text{-}2}$, and the gate drift currents of transistors $M_{5\text{-}6}$ are other sources of additional error terms while the discharge current is cut and the block is supposed to preserve the stored charge. Although small width for $M_{1\text{-}2}$ and small dimensions (both width and length) for $M_{5\text{-}6}$ can improve the results, the best remedy to tackle the problem will be a differential configuration as depicted in Fig. 3.2. This differential configuration dramatically reduces the errors.

3.2. Time Latch (Dynamic Analog Memory Cell)

Adopting discharge interruption in a delay unit together with some additional digital logic, a time memory cell called TLatch can be realized. As with other memories, a TLatch operates over three phases: write, idle and read. In the write phase, the two input signals are passed through two delay cells. After the arrival of both edges at the input, the propagation delays of both paths will be set to infinity to postpone the occurrence of the rising edges at the output of the memory cell until the read phase is initiated. As long as the delay lines are set in their open state (i.e., infinite delay), the TLatch is in its idle state. During the read phase, the delay in each path will be set back to its nominal value to deliver the

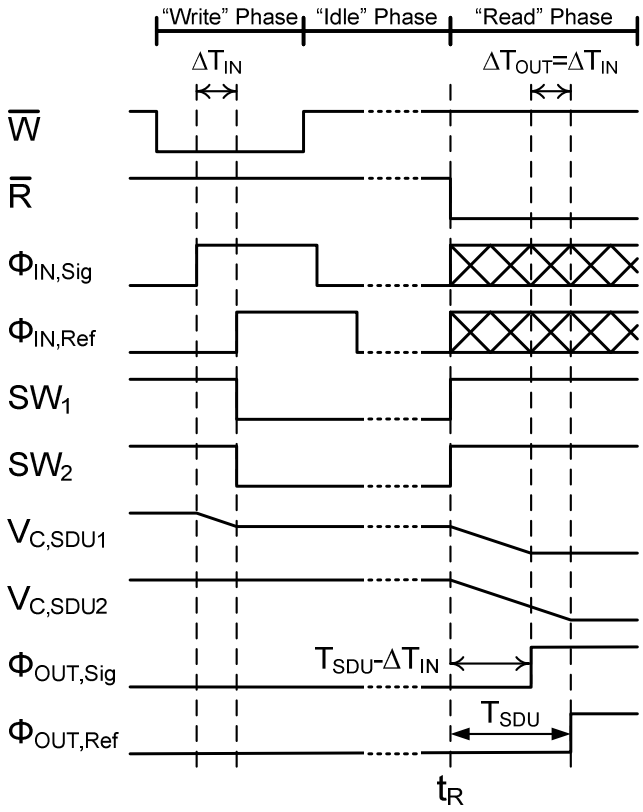


Fig. 3.4. The operational signals of a TLatch during "Write" and "Read" phases

rising edges at the output of the TLatch.

The schematic diagram for the proposed TLatch is shown in Fig. 3.3. The TLatch consists of two SDUs and some logic gates. With the write bit *W* set to logic "0", together with the read bit *R* set to a logic "1", and prior to the occurrence of the input rising edges at $\Phi_{IN,Ref}$ and $\Phi_{IN,Sig}$, the state of each SDU is pre-charged to V_{DD}. On arrival of the first edge, one of the SDUs begins to discharge towards ground while the other remains unchanged. On occurrence of the second edge, the *SW* inputs to both SDUs change to a logic "0", thereby forcing the SDU to hold the charge state of each capacitor indefinitely. The TLatch is now said to be memorizing the time-difference between the two rising edges of the input signals $\Phi_{IN,Ref}$ and $\Phi_{IN,Sig}$, i.e. ΔT_{IN}, where

$$\Delta T_{IN} = t_{IN,Ref} - t_{IN,Sig} \,. \tag{3.4}$$

Here $t_{IN,Ref}$ and $t_{IN,Sig}$ represent the time the rising edges at $\Phi_{IN,Ref}$ and $\Phi_{IN,Sig}$ arrive at the TLatch input. Changing the write signal *W* to a logic "1", places the

TLatch into an idle state whereby it is no longer affected by the input signals.

During a read phase and when the read signal, i.e. *R*, is set low, the two SDUs resume their discharge process (*SW* inputs are set high). Each SDU is left to discharge fully towards ground. On crossing the threshold of the inverter inside the SDU, the outputs of the TLatch change state. By applying the falling edge of signal *R* at time t_R, the rising edges at the output of the TLatch ($\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$) occurs at

$$t_{Out,Sig} = t_R + T_{SDU} - \Delta T_{IN} \tag{3.5}$$

and

$$t_{Out,Ref} = t_R + T_{SDU} . \tag{3.6}$$

By subtracting Eqn. (3.5) from Eqn. (3.6), the time difference between the output rising edges will be equal to

$$\Delta T_{OUT} = t_{Out,Ref} - t_{Out,Sig} = \Delta T_{IN} . \tag{3.7}$$

Eqn. (3.7) illustrates that the TM variable latched during the write phase has been restored at the output during the read phase. Since the TM variable under processing is the time-difference between the rising edges of two corresponding edges in two separate signal paths, no single element operates or senses this time difference; so, the proposed TLatch can handle any positive, negative, or zero TM input. To help clarify the order of these signals, the timing diagram shown in Fig. 3.4 is provided. The signals $V_{C,SDU1}$ and $V_{C,SDU2}$ in this figure represent the voltages across the capacitors inside SDU_1 and SDU_2, respectively.

It is important to mention that one buffer cell is included in Fig. 3.3 to introduce an arbitrary propagation delay. Taking advantage of this buffer, there would be an intentional delay between the time that the second rising edge at $\Phi_{IN,REF}$ arrives and the time that the discharge paths of the SDUs disconnect. It is very important that both SDUs experience the same number of OFF and ON transitions. By satisfying this precaution, some error terms will be canceled through the differential operation of the TLatch.

3.2.1. The Lower and Upper Limits for the Input of a TLatch

There are upper and lower limits for the TM variable to be captured at the

input of a TLatch. The maximum value of ΔT_{IN} is bounded by T_{SDU} associated with SDU of the TLatch; because, for any input greater than T_{SDU}, the capacitor inside one SDU will be completely discharged before the second rising edge is arrived. In other words, the output of one SDU is delivered in T_{SDU}- ΔT_{IN} seconds after the read signal R is applied, as shown by Eqn. (3.5). It should be evident that the maximum input phase difference must be less than T_{SDU} seconds to allow for a positive discharge time after applying R signal. By analyzing the operation of the TLatch in such an extreme condition, it can be concluded that any input TM variable greater than T_{SDU} would be stored as a TM variable equal to T_{SDU}.

On the other hand, the minimum detectable level for ΔT_{IN} is bounded by the jitter induced by the noise sources associated with the power supply and the discharge current of the SDUs inside the TLatch. Performing a straightforward noise analysis of the SDU, one finds the variation in the propagation delay of the SDU, denoted by $\sigma_{T_{SDU}}$, can be described by

$$\sigma_{T_{SDU}} = T_{SDU}\sqrt{\sigma_{V_{DD}}^2 / \left(V_{DD} - V_{Th,inv}\right)^2 + \sigma_I^2 / I^2\left(V_B\right)} \tag{3.8}$$

where $\sigma_{V_{DD}}$ and σ_I represent the standard deviation of the noise associated with the power supply and the discharge current of the SDUs, respectively. One can estimate the minimum rms value for the input will be equal to $\sigma_{T_{SDU}}$.

3.3. Addition and Subtraction of Time-Mode Variables

The need for addition and subtraction of two separate TM variables is central to most TMSP algorithms. The fact that the phase difference between any two sets of edges is not necessarily synchronized with respect to one another presents a significant problem for performing arithmetic operations on TM variables. The proposed TLatch can be used to tackle this problem, as explained below.

In Fig. 3.5.a, a modified configuration for the TLatch is presented where the timing diagrams for its operational signals is shown in Fig. 3.5.b. As shown in this figure, different R signals are introduced at different times of $t_{R,SIG}$ and $t_{R,REF}$, such that

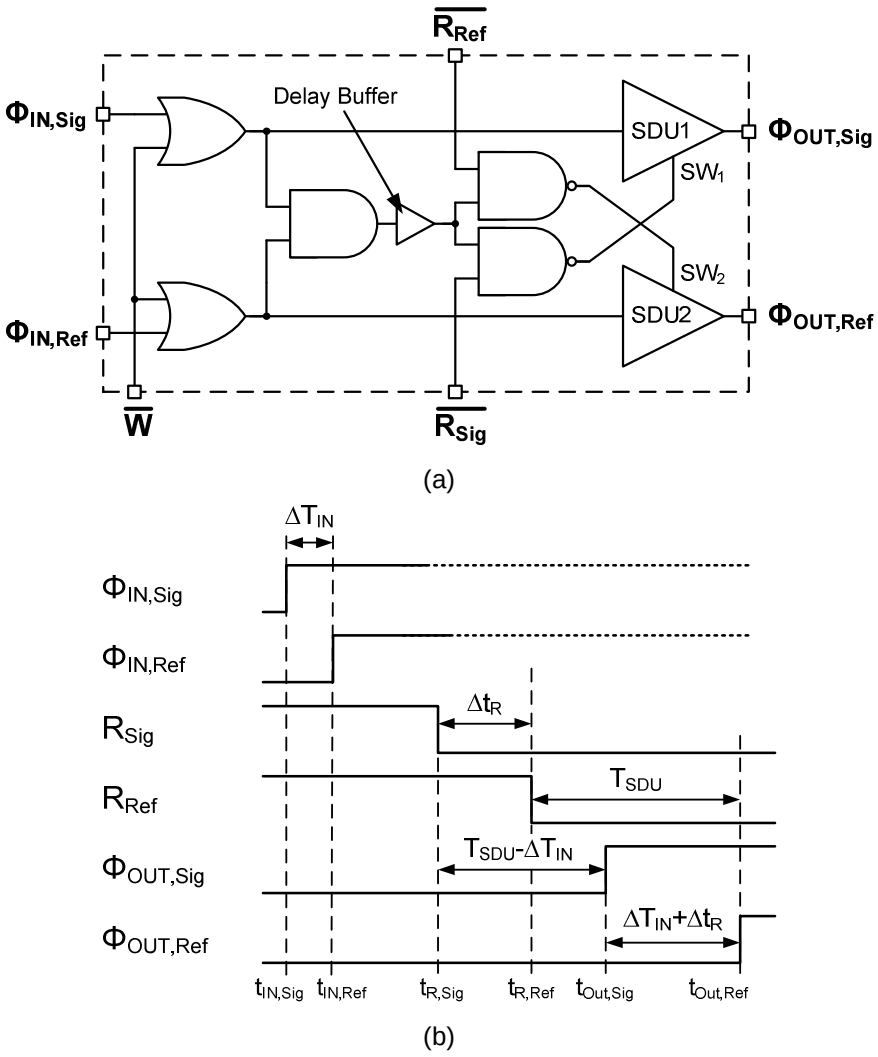


Fig. 3.5. (a) The circuit diagram for the modified TLatch, (b) The operational signals for the new configuration

$$\Delta T_R = T_{R,\mathrm{REF}} - T_{R,SIG}\,. \tag{3.9}$$

Rewriting the expressions for each SDU given previously in Eqns. (3.5) and (3.6) using the appropriate *R* signal, the time difference at the output of the TLatch changes according to

$$\Delta T_{OUT} = \Delta T_{IN} + \Delta T_R. \tag{3.10}$$

As it is evident, the phase difference at the output is the summation of two sets of independent time-differences. Consequently, a TLatch can be used in the configuration shown in Fig. 3.6.a to add together two signals ΔT_{IN1} and ΔT_{IN2}. After latching ΔT_{IN1} at the input, the TLatch will wait for the arrival of ΔT_{IN2} at the

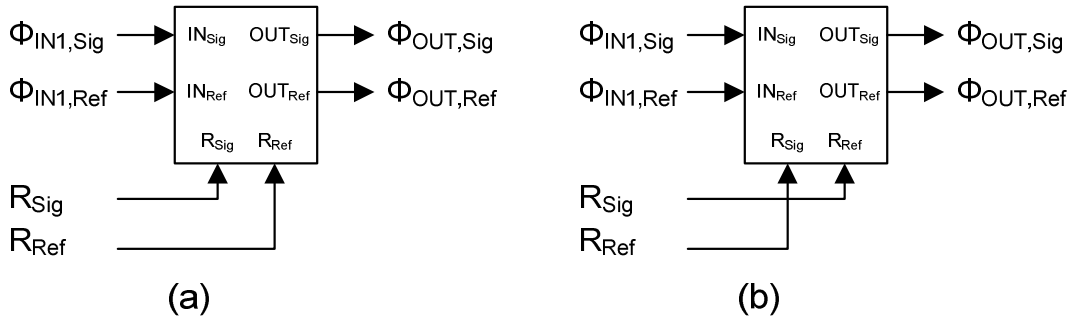


Fig. 3.6. Adopting a TLatch to perform (a) summation, (b) subtraction

R signals port as the second input to evaluate the summation of these two TM variables. By interchanging the connections for signals R_{SIG} and R_{REF} (as shown in Fig. 3.6.b), the time difference between *R* signals changes to $-\Delta T_{IN2}$ and the new configuration results in

$$\Delta T_{OUT} = \Delta T_{IN1} + (-\Delta T_{IN2}), \tag{3.11}$$

i.e. the subtraction of two TM variables.

Although the maximum value for ΔT_{IN1} is limited to T_{SDU}, theoretically there is no upper limit for the second TM operand, i.e. ΔT_{IN2}. Since the signals incorporating ΔT_{IN2} are used to control the *SW* inputs of the SDUs, any value of the phase difference between them will be added to the output eventually. If the output is higher than T_{SDU}, however, the leakage currents can slightly increase

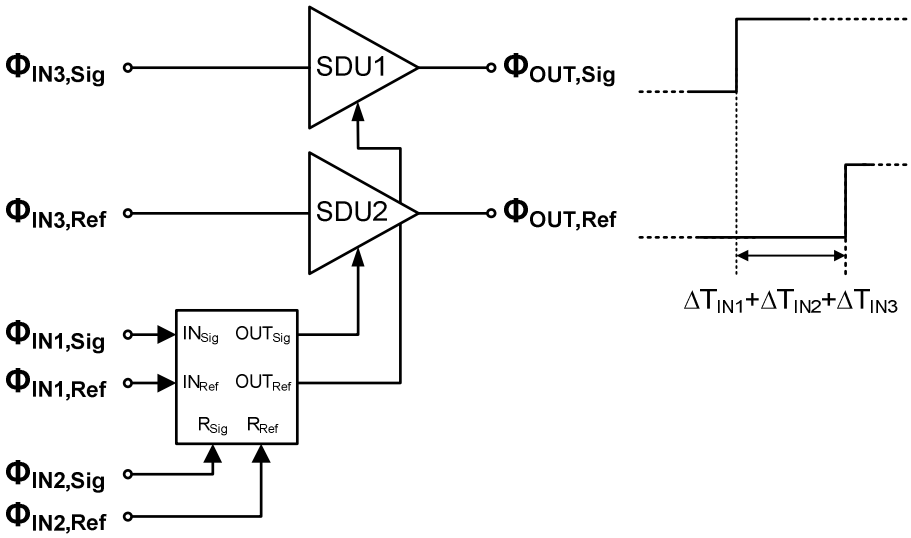


Fig. 3.7. The block diagram proposed for the summation of three TM variables

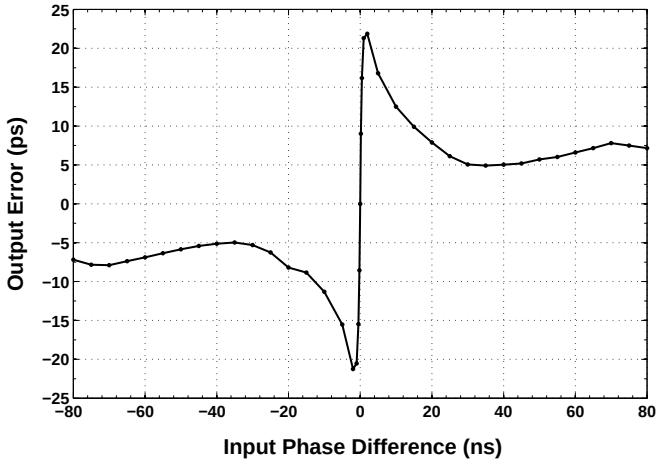


Fig. 3.8. The difference between the input and the latched TM value

the error associated with the output. In that case, one capacitor is discharged completely and the other one is still waiting for the reading signals; so, the residual charge in only one of the capacitors is subject to discharge by the leakage currents. This error will not be canceled out with any other corresponding error term on the other capacitor and it results in an increasing differential error term.

Using the block diagram shown in Fig. 3.7, this technique can be developed even further to add up to three TM variables. The output of the TLatch is connected to the *SW* inputs of two additional SDUs where the rising edges incorporating the third TM input, i.e. ΔT_{IN3}, are applied to their inputs. The output of the TLatch (i.e. $\Delta T_{IN1}+\Delta T_{IN2}$) is used to introduce additional delay to each SDU and the phase difference at the output of the SDUs will be the summation of all the three TM inputs. This method will be used to perform the integration of TM variables and it will be explained in Chapter 4.

3.4. Simulation Results

The circuit shown in Fig. 3.5.a was simulated in Cadence using the BSIM3v3 models of 1.2V 0.13-μm IBM CMOS technology.

While T_{SDU} of the SDU inside the TLatch was measured to be 86.6 ns, the TLatch was used to latch the phase difference of two digital signals. The TM variable applied to the input of the TLatch ranged from -84 ns up to 84 ns. By

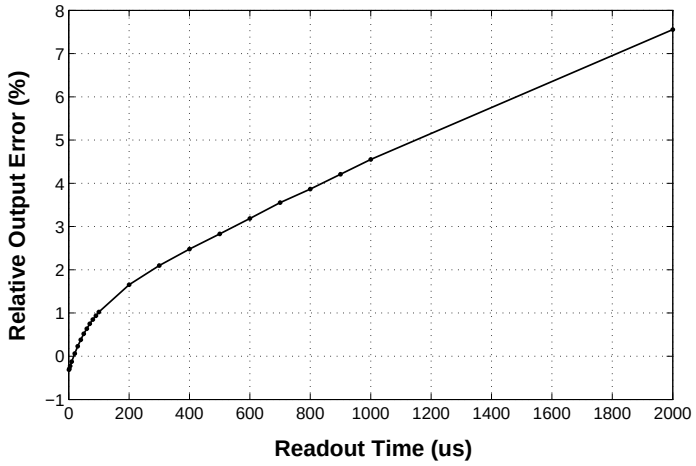


Fig. 3.9. The relative error for a 10 ns TM input read after different storage times

reading the latched information after 10 us, the difference of the stored TM variable and the input TM variable had a peak absolute value of no greater than 22 ps but no less than 5 ps, as shown in Fig. 3.8. The error increased for the input range from 0 up to 2ns. This increase was due to charge injection and capacitive coupling between the two input signals. However, for the inputs greater than 2 ns, the error changed in a nonlinear decreasing manner. The decrease was caused by the variation in the differential leakage currents due to the differences in the charge stored by each SDU. As simulations confirmed, the leakage current of the transistor M_1 in Fig. 3.1.a was dependant on the bias voltage of the transistor (i.e. voltage across the capacitor) which resulted in minor differences between the currents in each SDU. This non-linear differential current opposed the error created by the charge injection; so that, for input equal to 35 ns, the error was minimized.

By changing the readout time, the error induced by the differential leakage current changed as well. In Fig. 3.9, the relative error at the output of the TLatch for a TM input equal to 10 ns readout after different storage times is illustrated. It is evident as the storage time increases, the error increases as well. The leakage current opposes the error induced by charge injection and by canceling that, it can increase the error in the opposite direction. So, the dimensions of transistor M_1 in Fig. 3.1 should be optimized for the desired storage time.

Next, the addition and subtraction function of the TLatch was investigated with Cadence. Specifically, the configuration shown in Fig. 3.6.a was evaluated with an input time difference on Φ_{IN1} ranging from -84 ns to 84 ns, together with a second input on Φ_{IN2} ranging from 0 to 500 ns. It was evident that no extra error was introduced by the second input compared to the error reported in the previous paragraphs.

Finally, a similar experiment was conducted using the setup in Fig. 3.6.b for subtraction and results were identical to those found for addition, as expected.

3.5. Practical Considerations for Fabrication

3.5.1. Matching

The proposed technique presented in this chapter takes advantage of a differential structure. To extract the equations describing the operation of a TLatch, it was assumed that the two differential paths from the input pins to the outputs are completely matched. However, the CMOS implementation of the design encounters mismatches due to process variation and gate thickness gradient over the wafer [28]. To consider the proposed structure as a robust candidate to be adopted in highly efficient designs, the effect of mismatch should be investigated.

The structure shown in Fig. 3.5.a is composed of digital gates alongside a semi-digital block as SDU. Since the variable under processing in this block is the delay between the input and output signals, each digital gate may affect the signal by its own propagation delay. Due to the positive feedback embedded in typical digital gates (like Inverters, AND gates, and OR gates), the mismatch will not introduce any major difference in their propagation delay [54]. As a sample, the inverter gate adopted in the TLatch circuit was simulated individually. By introducing 10% mismatch between the transistor dimensions of two inverters, the delay of the block changed just 4% in the worst case. While the typical delay of the simulated inverter was 8.1 ps, the error induced by the mismatch was less than 400 fs.

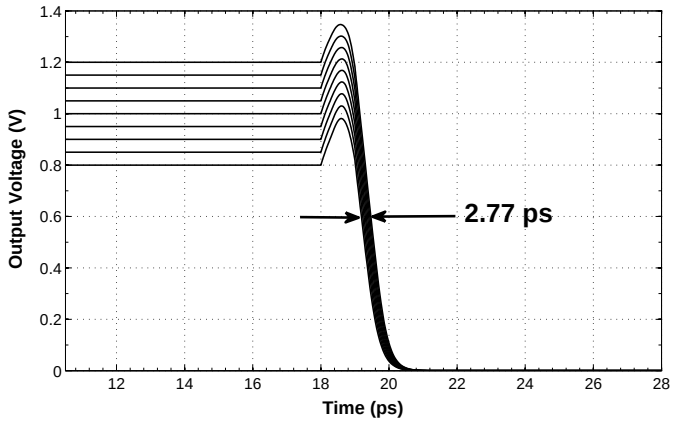


Fig. 3.10. The effect of power supply variation on the input-output delay of an inverter

Although the digital part of a TLatch is robust to mismatches, the SDU might be sensitive due to its discharge operation. The effect of any mismatches between SDU blocks can be summarized as the different T_{SDU} amounts for SDU_1 and SDU_2. Revising Eqns. (3.5) and (3.6) with different T_{SDU} values for each block, Eqns. (3.10) and (3.11) will be modified as

$$\Delta T_{OUT} = \Delta T_{IN} + \Delta T_R + (T_{SDU2} - T_{SDU1}) \tag{3.12}$$

and

$$\Delta T_{OUT} = \Delta T_{IN1} - \Delta T_{IN2} + (T_{SDU2} - T_{SDU1}) \tag{3.13}$$

where T_{SDU1} and T_{SDU2} are the delays of SUD_1 and SDU_2 respectively. The extra term added to each equation is a fixed value caused by mismatch and it is not correlated with the input signal. This analysis shows if there is any mismatch after considering typical layout techniques, the induced error term is a constant offset value that might be removed using simple numerical techniques.

3.5.2. Power Supply Noise

The digital nature of the proposed TLatch results in a noisier power supply. Due to digital charge and discharge of the parasitic capacitances distributed all over the circuit, an additive digital noise component will be added to the power supply as

$$V_{DD-\mathrm{Re}al} = V_{DD} + V_{Noise}\,. \tag{3.14}$$

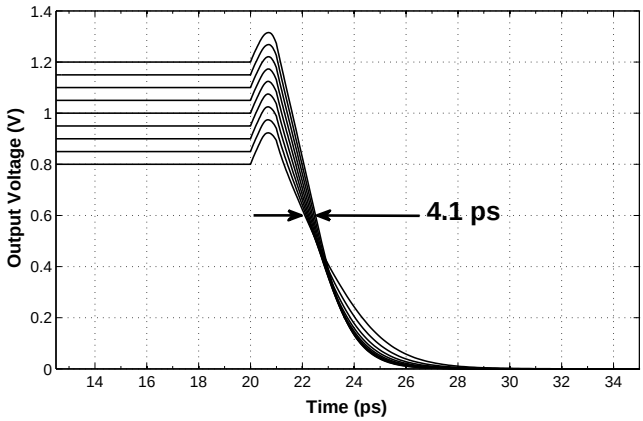


Fig. 3.11. The effect of power supply variation on the input-output delay of a digital NAND

It is important to investigate how the noisy power supply influences the performance of the circuit.

The amplitude of the digital noise may differ from one design to another one; however, it can be experimentally assumed less than 10% of the power supply. The performance degradation of a TLatch due to this noise and through digital gates is minor. As shown in Fig. 3.10 and based on simulations, the input-output delay of an inverter changes -2.77 ps (-27%) as the power supply changes from 1.2 V to 0.8 V (-33.33%). A change of 10% in power supply results in less than 1 ps change in the delay. If we consider the input of the TLatch within the range of nano-seconds, this change has minor effect on the dynamic range of the TLatch. This conclusion can be extended to other digital blocks like AND and OR gates. In Fig. 3.11, the change in the delay of a NAND gate configured in an inverter configuration is shown; for a -33% change in power supply, the delay changes -4.1 ps which is still a very minor change.

Considering the differential structure of a TLatch and the small amplitude of the delay variation induced by this noise, it can be concluded that the digital noise on the power supply has minor effects on the behavior of the digital gates included in a TLatch. The SDUs, however, may need more attention.

By replacing the value of the power supply in Eqn. (3.1) with the value denoted in Eqn. (3.14), the formula for T_{SDU} of each SDU block can be written as the sum of a noise-free term and a noise component, i.e.

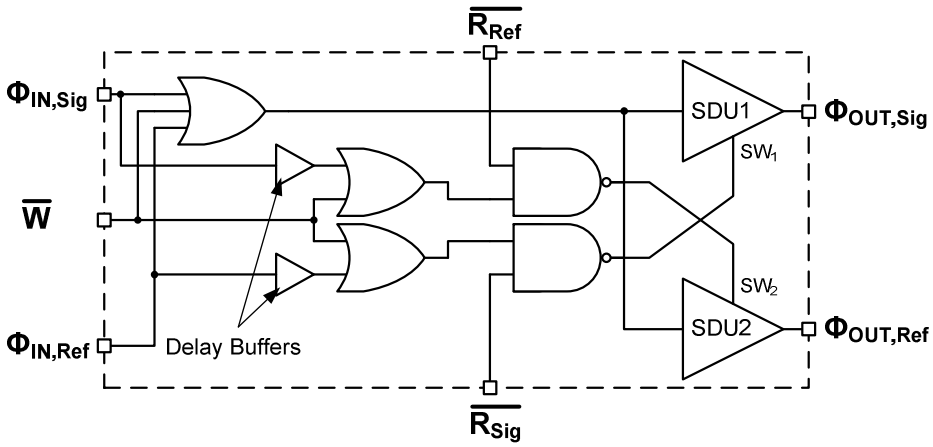


Fig. 3.12. The schematic of a TLatch robust to digital noise on the power supply

$$T_{SDU,Noise} = T_{SDU} + T_{Noise}, \tag{3.15}$$

where T_{Noise} is given by

$$T_{Noise} = \frac{C \times V_{Noise}}{I_D}. \tag{3.16}$$

The error term for each SDU maybe different due to different sampling times and the differential structure of a TLatch cannot remove it. However, the expected value of the error at the output is zero as it is zero for the digital noise voltage, V_{Noise}. Enough capacitors should be placed close to V_{DD} to filter the noise and control its influence on the output.

As previously explained, the Φ_{IN} input of the TLatch in Fig. 3.1.a and its *SW* input should be at digital high level to connect the discharge path of the capacitor inside the SDU. In the circuit diagram presented in Fig. 3.5.a, the *SW* inputs for both SDUs change at the same time while the main inputs to each SDU changes at different times; so, different values of V_{DD} will be sampled across each capacitor and the above-mentioned error will be produced. The schematic shown in Fig. 3.12 can be considered as a solution to tackle this problem. The principals of operation for the new architecture is the same as the previous one except for the fact that the main inputs of both SDUs are connected together; thus, they change from “0” to “1” at the same time and an individual amount of V_{DD} will be sampled on both capacitors. The rising edges at $\Phi_{IN,SIG}$ and $\Phi_{IN,REF}$ are used to interrupt the discharge paths of the SDUs through their *SW* inputs. The delay

buffers are included to guarantee the same number of ON and OFF transitions for both SDUs as explained for the initial design.

Simulation results confirm the proper operation of the new design. However, the amount of error induced by capacitive coupling between $\Phi_{IN,SIG}$ and $\Phi_{IN,REF}$ is measured slightly bigger compared to the previous TLatch circuit; also, mismatches between the delay-buffers may result in a fixed offset error at the output similar to the case for the mismatches between the SDUs.

3.6. Summary

In this chapter, digital techniques and blocks to implement storage, addition and subtraction among instantaneous time-mode variables are presented and simulations confirm the proposed theory. By developing switched-delay units and TLatch blocks, the phase difference between two rising edges can be easily latched and stored for future use. Addition and subtraction is one such example of its use, but other more advanced signal processing algorithms are envisioned using these blocks. Adopting the blocks and the techniques developed in this chapter, the integration of time-mode variables will be investigated in Chapter 4.

Chapter 4: A Digital Implementation of a Dual-Path Time-to-Time Integrator

4.0. Introduction

The need for processing analog signals is paramount in many of today's applications such as video-on-demand, web-browsing, remote sensing, high-definition and 3D television, navigation, etc. As CMOS technologies advance to 22-nm dimensions and beyond, constructing analog circuits in such advance processes suffer many limitations, such as reduced signal swings, sensitivity to thermal noise effects, loss of accurate switching functions, to name just a few. Time-Mode Signal Processing (TMSP) is a technique that is believed to be well suited for solving many of these challenges where one of its important advantages is the ability to realize analog functions using digital logic structures. TMSP has a long history of application in electronics from positron emission topography imaging in nuclear science [55], digital phase-locked loops in RF transmitters [56] and time-to-digital converters in various measuring instruments, such as digital oscilloscopes [57].

In most recently developed time-based structures like VCO-based data converters [18, 19], TMSP has been adopted to develop first-order quantization noise shaping to develop very affordable low power digital data converters. Attempts to increase the order of the modulator to improve its conversion resolution has been performed through the addition of analog signal processing

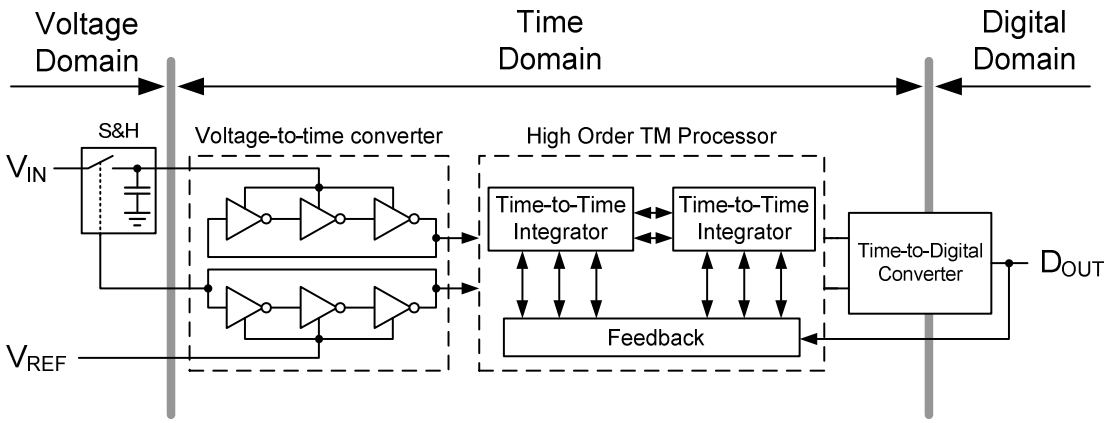


Fig. 4.1. Block diagram of a high-order analog signal processing system adopting TMSP

blocks, such as that reported in [58] for a second-order delta-sigma modulator and [21] for a third-order modulator. In [11], the authors developed a different digital topology for time-mode delta-sigma modulators where two ring-oscillators are utilized as a voltage-to-time integrator. Unfortunately, the technique is limited to a first-order topology as the addition of two or more time-mode signals was unknown at the time. This, in turn, prevents the cascade of integrators to realize high-order modulators. A third-order ΔΣ TDC has been recently reported in [53]; besides the presence of a few analog blocks within the design, the modulator is implemented in a 1-1-1 MASH structure avoiding the need for cascading integrators to achieve higher orders of modulation. While this approach is certainly a valid direction, other modulator topologies such as a leapfrog topology involving a cascade of integrators may offer additional performance advantages and need to be considered at this very early stage of time-mode circuits.

To extend the digital implementation of TMSP to a wider range of analog applications, at this time it is apparent that some of the most basic arithmetic operations are required. Blocks to perform addition and subtraction exclusively in the time-domain have been presented in Chapter 3. It is the objective of this chapter to adopt these techniques to develop a unity-gain time-to-time integration function using an all-digital implementation. This provides a consistent means to present both the input and the output signals in the form of a digital signal (i.e., step function) while performing an analog operation. An essential feature of the desired circuit is the ability to be placed in cascade so that high-order structures

can be realized. A block diagram of such a system is shown in Fig. 4.1. Here it consists of a front-end voltage-to-time converter that produces a sequence of TM variables proportional to the uniformly sampled input analog voltage. The input sequence is then forwarded to a high-order time-mode processor to solve a system of difference equations. Finally, a time-to-digital converter is used to change the results into a digital format.

The advantages of a digital approach for TMSP are multi-folded. The first is to construct analog circuits from a large class of digital blocks, such as Inverters, NAND, NOR, flip-flops, buffers, etc. A wealth of practical design knowledge is available for constructing such circuits. This includes low-noise/low-jitter realizations, test strategies, strategies to mitigate process variation effects, and so on. As a second advantage, this digital implementation of an analog function is synthesizable with computer-aided-design tools. This provides significant design productivity and quick time-to-market opportunities. A third advantage is the simplicity of circuit calibration to remove the effects of process variation.

The chapter is organized to begin by describing the synchronous and asynchronous modes of TMSP. Then by adopting the building blocks proposed in Chapter 3, the proposed single-path and dual-path time-to-time integrators are described. The rest of this chapter covers the practical concerns regarding the realization of the proposed dual-path integrator and the simulation results are provided. Finally, the experimental results relating to a CMOS prototype will be described at the end of this chapter.

4.1. Asynchronous vs. Synchronous

After converting the input uniformly sampled analog data into a sequence of TM samples, the processing in the time-domain is performed in a synchronous or asynchronous mode of operation. In a synchronous mode [59]-[61], the TM variables are synchronized with a reference clock. Arithmetic operations performed by synchronous TM systems have been implemented by converting the input TM samples into a separate charge or flux representations. These charge or flux-based signals are then combined in some analog way then

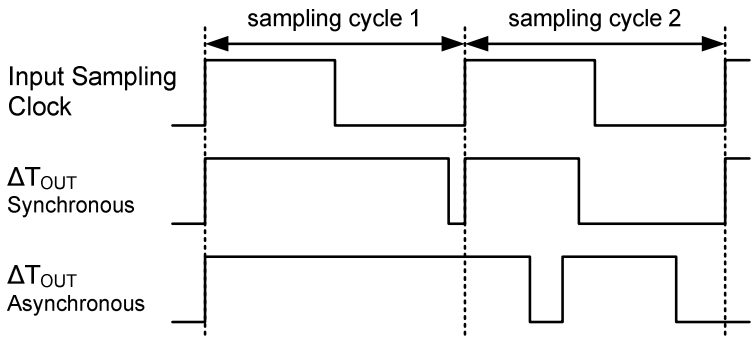


Fig. 4.2. A comparison of the upper limit for the TM output of a synchronous and asynchronous system operating at the same sampling frequency

converted back into a TM representation synchronized with respect to the reference clock. Although this approach eases the design procedure, it has some disadvantages; first, the inherent time-to-charge/flux conversion and its reverse conversion introduce signal-dependent errors. Second, to process the converted charge/flux representations, analog operations are involved that forfeits the desired digital advantage of TMSP. As a third limitation, the upper limit for a synchronous TM variable is bounded by the period of the reference clock.

In an asynchronous approach, however, the input and output TM signals are not necessarily synchronized with the reference clock. Taking such an approach, TM inputs can be processed as they come into the processor. No time-to-charge/flux conversion is necessary to perform the arithmetic operation or to synchronize the output TM variable with the reference clock (see Chapter 3).

In addition, the length of each processing cycle is flexible and it depends on the magnitude of consecutive output TM samples. This feature enables the system to have a larger upper limit for the TM variables when compared to an equivalent synchronous design operating under similar sampling rate conditions. To clarify the difference, the timing diagram for the TM output of a synchronous and asynchronous circuit is compared in Fig. 4.2. Also shown at the top of this diagram is the input sampling clock for the two systems. For the synchronous design (middle trace), the upper limit for the TM output (pulse width) is limited to a single period of the sampling clock. In the case of the asynchronous output signal, the first sample has a TM magnitude that exceeds a period of the sampling clock and the following sample has a magnitude that is less than a

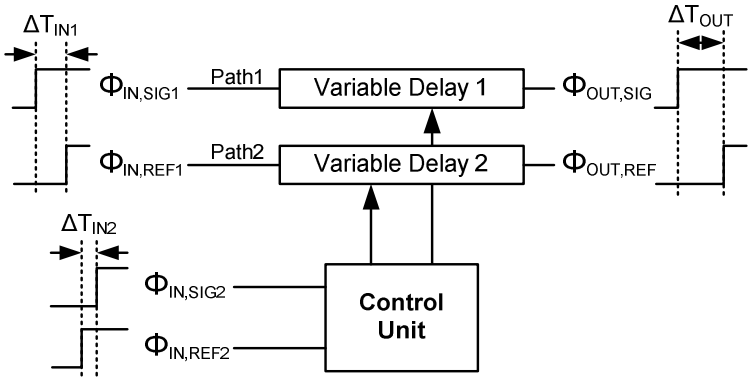


Fig. 4.3. A conceptual diagram of the proposed asynchronous TMSP technique

single period. In order for the system to operate correctly, the average of two successive output TM samples must be less than a single sampling period. This is necessary to equalize the rate of data at the input and output of the system, i.e. causality. In this simple case, it is evident that for the same sampling frequency (i.e., the same input rate), the asynchronous system can handle a larger upper signal limit (i.e., higher dynamic range) than the synchronous system.

In this chapter, a new asynchronous technique to process time-mode variables is proposed that is based on the block diagram shown in Fig. 4.3. Similar to Chapter 3, each asynchronous TM variable, for example ΔT_{IN1}, can be defined as the phase difference between the rising edges of two digital signals, denoted as $\Phi_{IN,SIG1}$ and $\Phi_{IN,REF1}$. For a $\Delta T_{IN1}>0$, the rising edge of $\Phi_{IN,SIG1}$ leads the rising edge of $\Phi_{IN,REF1}$. Similarly, for $\Delta T_{IN1}<0$, the rising edge of $\Phi_{IN,SIG1}$ lags the rising edge of $\Phi_{IN,REF1}$. In the case of a zero TM sample, the rising edges of $\Phi_{IN,SIG1}$ and $\Phi_{IN,REF1}$ occur at the same time. By passing the input rising edges through two separate paths with different propagation delays as shown in Fig. 4.3, the phase difference between the output rising edges will be equal to the sum of the phase difference at the input and the phase difference between the two delay paths. It will be shown that by controlling each variable delay by another TM variable such as ΔT_{IN2}, different processing functions like time-to-time integration can be realized in an asynchronous manner.

4.2. Single-Path Time-to-Time Integration

A discrete-time integrator is a basic building block of many electronic

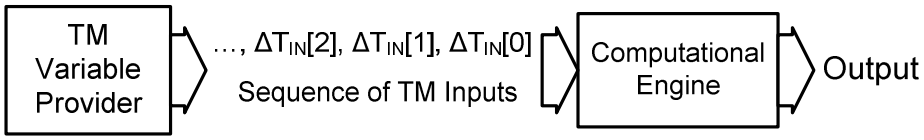


Fig. 4.4. Separating the TM variable extraction process from the integration process performed by a computational engine.

systems whereby its output is the recursive addition of a discrete input quantity. Assuming a unity-gain time-to-time integrator, the difference equation relating the output of the integrator to its input is given by

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + \Delta T_{IN}[n-1], \tag{4.1}$$

where $\Delta T_{IN}[n]$ and $\Delta T_{OUT}[n]$ represents the input and output time-mode (TM) variables and n represents the sample index. In this section by adopting the switched-delay unit (SDU) and the time memory cell (TLatch) proposed in Chapter 3, a description of a single-path integrator and its control logic will be provided. This section will conclude with a discussion about the limitations of the proposed single-path integrator.

4.2.1. The Logic Diagram

The TLatch described in Chapter 3 is the key element of an integrator whose input and output is a sequence of TM variables. In this work, the integrator is considered as the computational engine of Fig. 4.4 that captures the input samples in a sequential order and produces the output according to Eqn. (4.1). Each TM input that can be either the output of a uniformly sampled voltage-to-time converter or the output of a previous TMSP stage is defined as the phase difference between two rising edges and the index n will be used to indicate the order in which the TM samples arrive at the input of the integrator. To maintain the causality of the system, there should be a one-to-one correspondence between the inputs and outputs of the computational engine. For any new input, a new output should be computed and no input should be missed while doing so. For example, if the input sample sequence consists of the values {0, 10ns, -23ns, 32ns, -15ns, 62ns …}, the output sample sequence should appear as {0, 10ns, -13ns, 19ns, 4ns, 66ns …}. The means to extract a sequence of TM variables

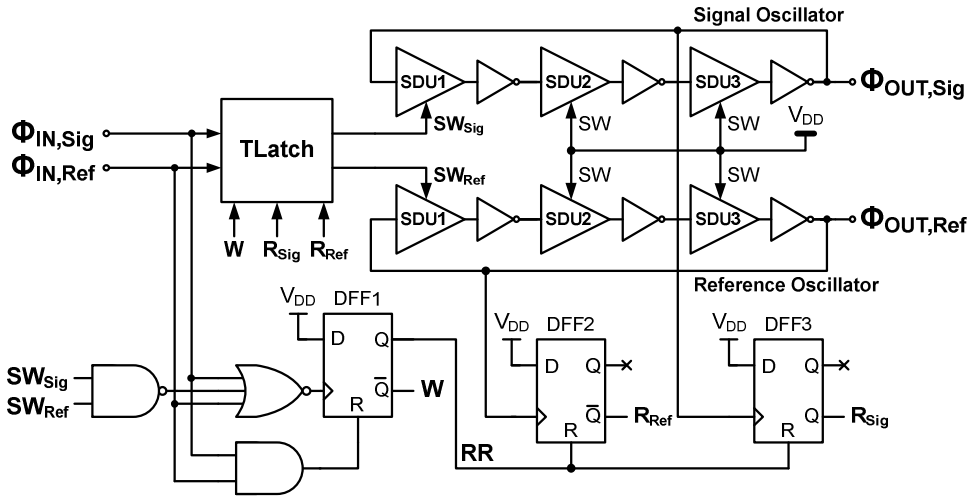


Fig. 4.5. A block/logic diagram of a single-path time-to-time integrator.

from some analog signal, such as a continuous-time voltage signal, is not the focus of this thesis. Fig. 4.4 provides an illustration of separation of the TM variable provider and integration operation performed by the computational engine.

The logic schematic proposed to implement a time-to-time integrator is shown in Fig. 4.5. The output of the integrator is the time difference between the two rising edges at the outputs of the two ring-oscillators (the signal and the reference oscillators), i.e.

$$\Delta T_{OUT} = t_{OUT,Ref} - t_{OUT,Sig}\,, \tag{4.2}$$

where $t_{OUT,Sig}$ and $t_{OUT,Ref}$ represent the time for the rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$, respectively. The maximum value for the output of this integrator is equal to the oscillation period of each oscillator. We consider this limit as the saturation level of the integrator.

The oscillation periods of the two ring oscillators are assumed the same. Any phase difference between them will be held constant from cycle-to-cycle. As will be explained shortly, the front-end TLatch shown in Fig. 4.5 captures the TM sample at the input port of the integrator and waits for the arrival of the rising edges from the output of the integrator ($\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$) at the read (R) ports of the TLatch. Adopting the same technique as shown in Fig. 3.6.a, the sum of these two TM variables is then passed as output from the TLatch and loaded

into the two ring-oscillators as the new integrator output value.

Through careful analysis of the ring oscillator in Fig. 4.5, its instantaneous period can be formulated as

$$T_{OUT} = T_{SDU1} + T_{SDU2} + T_{SDU3} + 6\,\tau_{inv} + 3\,\tau_{SDU}\,, \tag{4.3}$$

where T_{SDUx} represents the propagation delay of SDU_x for a rising edge, τ_{SDU} represents the delay of any SDU for a falling edge, and τ_{inv} represents the delay of the inverter. Eqn. (4.3) was formulated assuming the SW inputs for all SDUs are connected to V_{DD}. This assumption is true for SDU_2 and SDU_3 where they are used as fixed delays to set the timing (duty cycle) of the oscillators. In the case of SDU_1, its *SW* input will vary depending on the TLatch output. As shown in Fig. 4.5, the *SW* input to SDU_1 is connected to either SW_{Sig} or SW_{Ref}, depending on which ring oscillator it is in. Within the *n*-th cycle, if signals SW_{Sig} and SW_{Ref} go low and stay at this level until $\Delta T_{SW,Sig}[n]$ and $\Delta T_{SW,Ref}[n]$ seconds after the input rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$ arrive to the inputs of the two SDU1s, then the propagation delay for each SDU_1 will be modified according to Eqn. (3.2). As a result, the modified instantaneous period for the n-th cycle of the signal and reference oscillator can be written as

$$T_{OUT,Sig}[n] = T_{OUT} + \Delta T_{SW,Sig}[n] \tag{4.4}$$

$$T_{OUT,Ref}[n] = T_{OUT} + \Delta T_{SW,Ref}[n]. \tag{4.5}$$

Assuming the current TM output of the integrator, i.e. $\Delta T_{OUT}[n]$, is defined as the time difference between a pair of rising edges arriving at times $t_{OUT,Sig}[n]$ and $t_{OUT,Ref}[n]$, then the next pair of the rising edges will appear at

$$t_{OUT,Sig}[n+1] = t_{OUT,Sig}[n] + T_{OUT,Sig}[n] \tag{4.6}$$

$$t_{OUT,Ref}[n+1] = t_{OUT,Ref}[n] + T_{OUT,Ref}[n] \tag{4.7}$$

Using Eqns. (4.2), (4.4)-(4.7), a recursive difference equation representing the output of the integrator can be written as

$$\Delta T_{OUT}[n+1] = \Delta T_{OUT}[n] + \left(\Delta T_{SW,Ref}[n] - \Delta T_{SW,Sig}[n]\right). \tag{4.8}$$

As is evident from Eqn. (4.8), the next integrator output is a sum of the previous

output and the difference between the incoming low-level pulse widths applied to the *SW* input of each ring oscillator.

The *SW* signals in Fig. 4.5 are produced by the TLatch that, in turn, derives these signals from the main TM input to the integrator as shown on the left-most side of Fig. 4.5. After latching the TM input, the rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$ are used to initiate the falling edges at R_{Sig} and R_{Ref} inputs of the TLatch. The time that lapses from the falling edge of R_{Sig} to the time that the output SW_{Sig} goes high is denoted $\Delta T_{SW,Sig}$. Likewise, the time between the falling edge of R_{Ref} and the rising edge of SW_{Ref} is denoted $\Delta T_{SW,Ref}$. For a positive ΔT_{IN} captured by the TLatch together with Eqns. (3.5) and (3.6), $\Delta T_{SW,Sig}$ and $\Delta T_{SW,Ref}$ will be equal to

$$\Delta T_{SW,Sig}[n] = T_{SDU} - \Delta T_{IN}[n], \tag{4.9}$$

and

$$\Delta T_{SW,Ref}[n] = T_{SDU}\,. \tag{4.10}$$

Subsequently, substituting Eqns. (4.9) and (4.10) into Eqn. (4.8) leads to

$$\Delta T_{OUT}[n+1] = \Delta T_{OUT}[n] + \Delta T_{IN}[n]. \tag{4.11}$$

Eqn. (4.11) confirms that the proposed structure operates as a unity gain integrator. A similar procedure can be used to confirm the validity of this equation for a negative ΔT_{IN}.

In summary, the operation of the time-to-time integrator starts with the capture of a TM input using the TLatch. The integrator then waits for the arrival of the next pair of rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$ to read out the latched data. The sum of these two TM variables is then passed as output from the TLatch and loaded into the two ring-oscillators as the new integrator output value.

4.2.2. The Logic to Control the TLatch Operation

Included in Fig. 4.5 is some additional logic to control the read/write operation of the TLatch. To explain how the logic works, we start from the initial condition when *W*="0", *RR*="1" (DFF2 and DFF3 are reset, i.e. R_{Sig}=R_{Ref}="1") and SW_{Sig}=SW_{Ref}="1". Using the *W* signal as the write signal of the TLatch, the phase

difference between the next pair of input rising edges, ΔT_{IN}, will be captured by the TLatch. The outputs of the TLatch (SW_{Sig} and SW_{Ref}), which have been changed to "0" before arrival of the input rising edges, will keep their state until the TLatch is readout. Once the two input signals change to 1 (i.e., $\Phi_{IN,Sig}$=$\Phi_{IN,Ref}$="1"), DFF1 will be reset by the AND gate and *RR* will change to "0". Subsequently, on the arrival of the next pair of output rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$, the oscillation of each oscillator will stop due to the low state of SW_{Sig} and SW_{Ref} signals. On the other hand, these output edges will latch DFF2 and DFF3 into a new state, establishing a read phase for the TLatch through R_{Sig} and R_{Ref} signals. The outputs of the TLatch will be set to "1" sometime after the arrival of each *R* signal and the oscillation of the two output ring-oscillators continue into the next cycle. As soon as the data latched by the TLatch is readout completely (i.e. SW_{Sig}=SW_{Ref}="1"), *RR* will be set to "1" before the next rising edges at $\Phi_{IN,Sig}$ and $\Phi_{IN,Ref}$ arrive. Consequently, R_{Sig} and R_{Ref} will be set to "1" and *W* will be reset to "0" and the TLatch will be ready to capture the next TM input of the integrator upon the arrival of the rising edges at $\Phi_{IN,Sig}$ and $\Phi_{IN,Ref}$.

4.2.3. Integrator Speed Limitation

As previously mentioned, the input of the integrator is a sequence of TM variables. The integrator is ready to take the next TM input after the previous input is read out of the TLatch. The time needed to perform this readout places a minimum bound on the time between two successive inputs, i.e. it limits the input throughput. In the most optimistic situation, this limit is equal to T_{SDU} (the intrinsic delay of the SDU inside the TLatch). The optimistic situation arises when the rising edges for the output of the integrator arrive right after the TM input is captured by the TLatch. Assuming the time difference between these rising edges is zero, the readout of the newly captured input will start instantly after it is latched.

Due to the asynchronous operation of the integrator, every TM input must be followed by a TM output; at no time, two inputs can arrive in succession before an output is set. However, the rising edges of the output can occur at any time between two successive input samples. The time it takes for the output rising

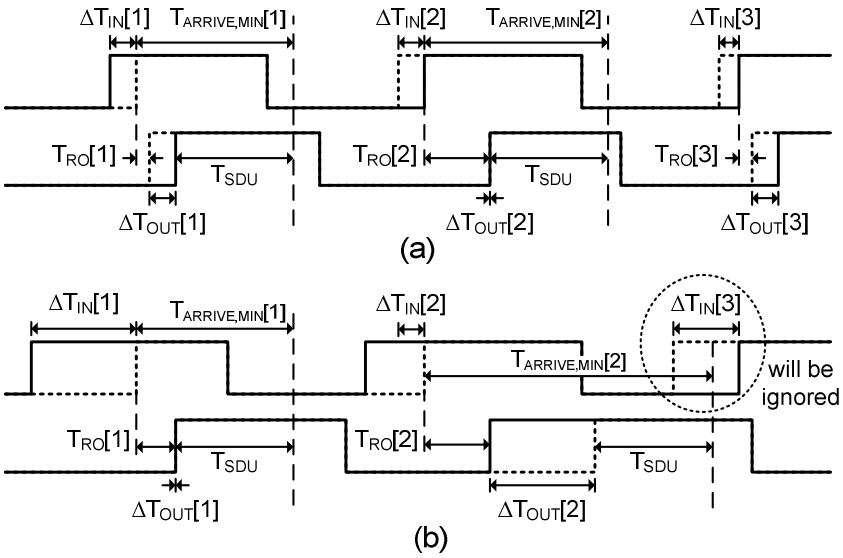


Fig. 4.6. Timing diagram of the input and output TM signals from the integrator. (a) Correct timing between two successive input samples. (b) Incorrect timing between two successive input samples.

edges to start the read-out of the latched data influences the minimum time needed between successive input samples. Defining T_{RO} as the time difference between the time the TM input is latched and the time the read signals (which are produced upon the arrival of the rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$) are applied to the *R* port of the TLatch, the instantaneous minimum available time needed between successive input TM samples can be expressed as

$$T_{ARRIVE,MIN}[n] = T_{RO} + \Delta T_{OUT}[n] + T_{SDU} \; . \tag{4.12}$$

For a realistic situation, $T_{ARRIVE,MIN}$ is generally larger than T_{SDU} and it can change between cycles. To clarify the situation, Fig. 4.6 illustrates two different cases. In Fig. 4.6.a, the instantaneous $T_{ARRIVE,MIN}$ for each two successive inputs is satisfied when each new input arrives at least T_{SDU} seconds after the output rising edges are set. Therefore, the inputs are properly accounted for based on the order they come in. In Fig. 4.6.b, however, due to the large magnitude of $\Delta T_{OUT}[2]$, the minimum arrival time $T_{ARRIVE,MIN}$ between input samples $\Delta T_{IN}[2]$ and $\Delta T_{IN}[3]$ is much larger than their actual time spacing, hence, a system violation occurs. More specifically, $\Delta T_{IN}[3]$ arrives before $\Delta T_{IN}[2]$ is read out of the TLatch and is therefore ignored.

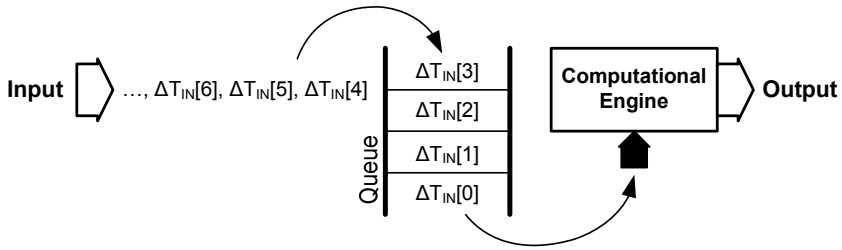


Fig. 4.7. Applying the input TM samples of the integrator to the input of the computational engine through a queuing process

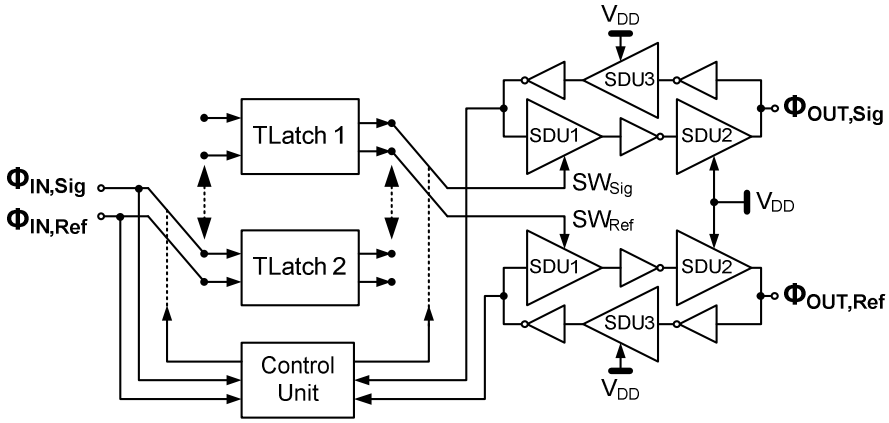


Fig. 4.8. A block diagram for dual-path time-to-time integrator

By limiting the input throughput of the integrator to the worse case so that no writing overlap occurs, the performance of the integrator dramatically drops. However, the asynchronous operation of the integrator supports the possibility of time borrowing, where the smaller times between successive input samples can be accounted for. In the following section, the single-path integrator will be modified to a dual-path integrator to improve the throughput of the integrator.

4.3. Dual-Path Time-to-Time Integrator

As mentioned previously, the minimum time interval necessary between successive TM inputs to the integrator changes from cycle to cycle. Due to the asynchronous nature of TMSP as well as the input and output amplitude, this minimum time can increase for two successive TM inputs, while for another two inputs it may decrease. A possible solution to improve the throughput of the integrator is to forward the input sequence of TM samples into a queue, as shown in Fig. 4.7. By placing the inputs in a first-in first-out queue, the incoming data will be read out of the queue at the proper time to perform the integration. As long as

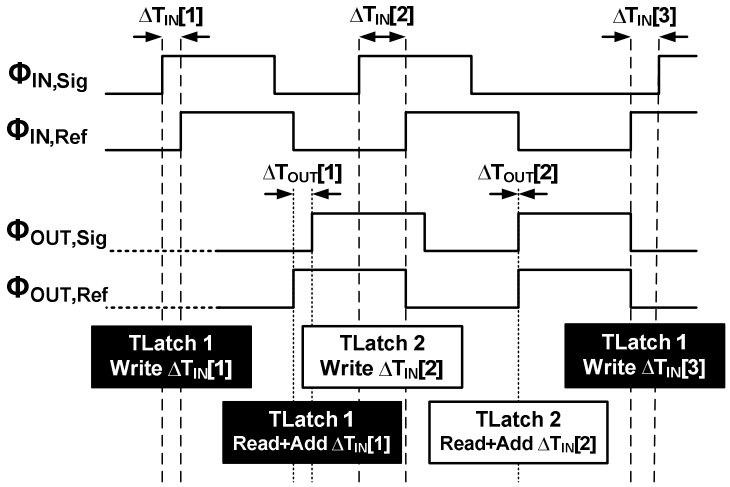


Fig. 4.9. Adopting two TLatches in parallel for dual-path integration

the average readout rate is equal to the average input arrival, no data will be overwritten or ignored. Adopting this approach, the integrator is made to handle the average $T_{ARRIVE,MIN}$ between input TM samples rather than the worst-case (largest).

The block diagram for a queue-based time-to-time integrator adopting a two-position queue is shown in Fig. 4.8. Two TLatches are included to implement the queue. The odd and even-numbered input TM samples are forwarded to $TLatch_1$ and $TLatch_2$ respectively. As illustrated in Fig. 4.9, $\Delta T_{IN}[1]$ is latched by $TLatch_1$ and is kept until the rising edges at the output of the integrator representing $\Delta T_{OUT}[1]$ arrive to initiate the readout of this TLatch; meanwhile, $TLatch_2$ tracks the input port to capture the next TM input, $\Delta T_{IN}[2]$, without any concern about the readout of $\Delta T_{IN}[1]$. The control unit in Fig. 4.8 is digital and it is responsible for routing the data into and out of the queue; this routing is done by the selection of the right TLatches for either write or read using the *R* and *W* signals of each TLatch.

For ease of reference, we call the architecture shown in Fig. 4.8 a dual-path integrator. Throughout the rest of this section, the details behind the digital control unit will be explained.

4.3.1. Switching Between Two TLatches

The digital control unit is supposed to forward the odd and even-numbered

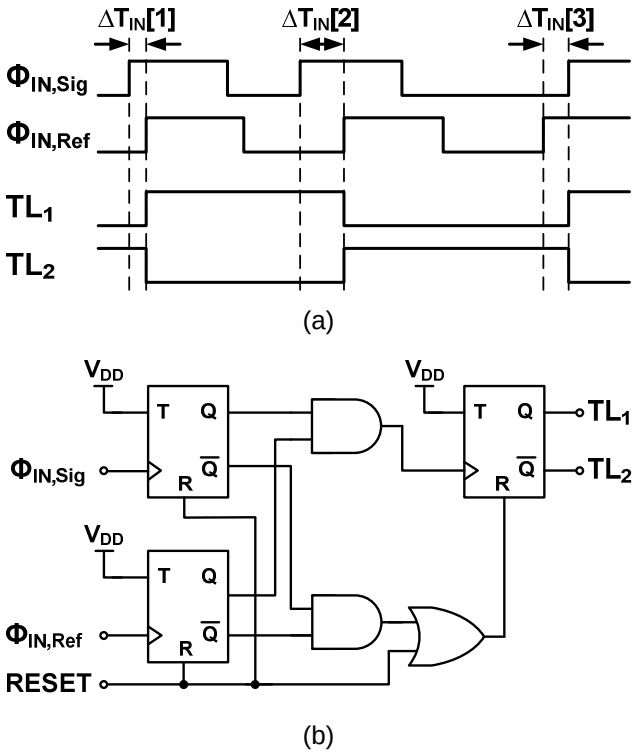


Fig. 4.10. (a) The signal scheme for two flag-bits TL1 and TL2, (b) The circuit schematic of the digital switch (DSwitch)

TM samples to $TLatch_1$ and $TLatch_2$ respectively. Two complementary flag-bits TL_1 and TL_2 are needed to represent the Odd and Even status of the input samples. As shown in Fig. 4.10.a, these bits change upon the complete arrival of any new input TM sample. An input TM variable might be considered completely arrived, if both rising edges incorporating the input phase difference have occurred. By connecting TL_1 and TL_2 to the *W* inputs of $TLatch_1$ and $TLatch_2$, respectively, the appropriate TLatch will be in write mode when the corresponding rising edges arrive at the input port of the integrator. For instance, any odd-numbered input is routed to $TLatch_1$ when TL_1="0" and TL_2="1". Once latched, the flag bits will toggle and the next even-numbered input will be forwarded to $TLatch_2$ for TL_1="1" and TL_2="0".

The proposed circuit diagram to produce TL_1 and TL_2 is presented in Fig. 4.10.b and we consider the whole circuit as a single block called a DSwitch. The T-Flip-Flop (TFF) with a "1" at the *T* input operates like a single-bit counter for the input rising edges. The additional AND and OR gates are used to detect "11" and

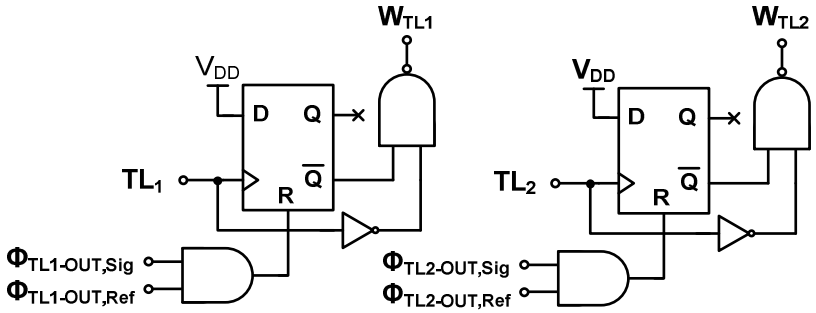


Fig. 4.11. Circuit schematic for producing the write *W* signals of each TLatch

"00" states to set and reset the output D-Flip-Flop which in turn sets TL_1 and TL_2. The *RESET* signal is a global signal and it is included for initial reset of the digital control unit whenever applicable.

The direct connection of TL_1 and TL_2 to the *W* inputs of the TLatches can result in error. To explain the problem, we consider the signal scheme presented in Fig. 4.10.a. After latching $\Delta T_{IN}[1]$ by $TLatch_1$, this data might be kept until $\Delta T_{IN}[3]$ arrives. However, as soon as $\Delta T_{IN}[2]$ is latched by $TLatch_2$, flag-bit TL_1 will change to "0". If this bit is used as the *W* input of $TLatch_1$, the input signals at $\Phi_{IN,Sig}$ and $\Phi_{IN,Ref}$ will be buffered to the inputs of the SDUs inside $TLatch_1$ (Fig. 3.5.a) and any falling edge at the input port will change the charge distribution inside the SDUs. In this situation, $\Delta T_{IN}[1]$ stored in this TLatch will be modified and the readout data will be subject to error. In order to ensure that the new data does not overwrite past data that has yet to be used, the circuit of Fig. 4.11 will be used to extract the W_{TL1} and W_{TL2} to control the *W* input of $TLatch_1$ and $TLatch_2$ respectively. When TL_1 changes to "1", $TLatch_1$ should be kept in the read phase until the data is read out completely (i.e., both $TLatch_1$ outputs are set high). A similar situation applies to $TLatch_2$.

4.3.2. Modifying the Output of the Integrator

In much the same way that the input data was routed to the two TLatches, the output of the TLatches must be routed to the output ring oscillators using a digital switching mechanism. The TLatch selection logic to modify the output of the integrator is synchronized with the arrival of the rising edges at the output of the integrator, i.e. $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$. This is in contrast to that which is

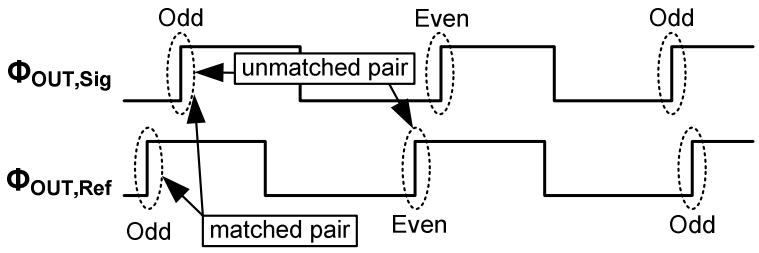


Fig. 4.12. The Illustrating the concept of matched and unmatched edge pairings

performed in TLatch selection logic for input storage where the switching action was synchronized with the arrival of the rising edges at the input of the integrator.

The output of the integrator is defined as the phase difference between two ring-oscillators. To synchronize the selection logic, a matched pair of rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$ should be taken into account. The sequence of oscillation cycles in both oscillators should be monitored carefully. Designating each cycle with an increasing number, the number of cycles incorporating the output pair of rising edges should be matched. In Fig. 4.12, a few cycles of each oscillator output are shown. If the selection logic tracks the wrong sequence of the rising edges, such as an odd edge of the signal oscillator with an even edge of the reference oscillator, the tracking will be in error. The circuit shown in Fig. 4.13 produces the flag bit *MState* to distinguish the corresponding rising edges. Again, each TFF operates like a single-bit counter and the XNOR gate sets *MState* to logic “1” when the input rising edges occur on either even or odd number. In other words, when *MState* is “1”, the next rising edge can be considered the first one of a matched pair. When this flag bit is “0”, the circuit is

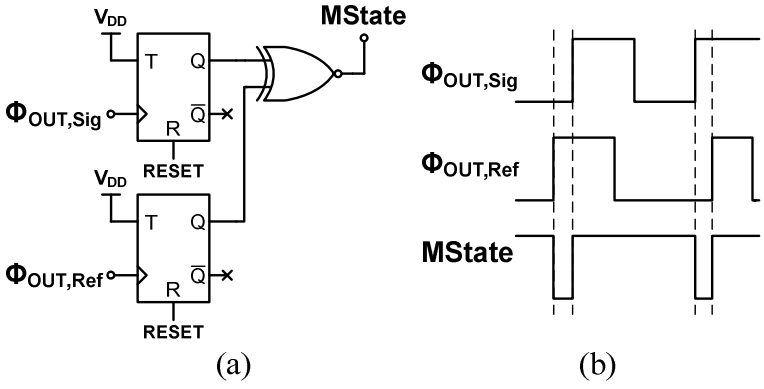


Fig. 4.13. Generating the *MState* flag bit signal: (a) circuit schematic, (b) signaling scheme

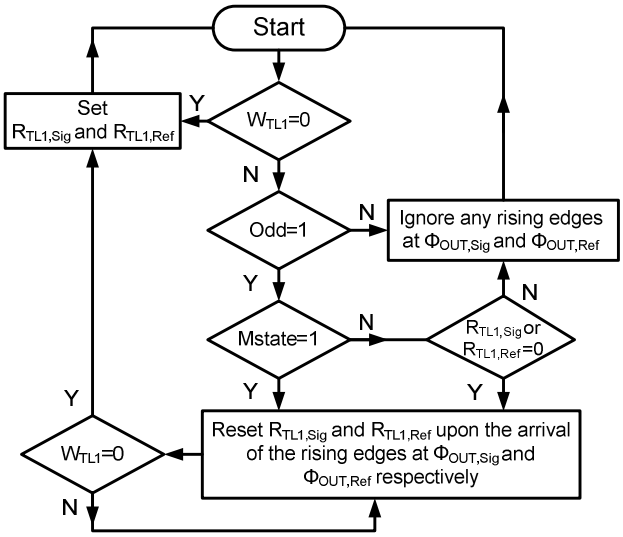


Fig. 4.14. The flow-chart to set and reset $R_{TL1,Sig}$ and $R_{TL1,Ref}$

waiting for the second rising edge of a matched pair.

Upon the arrival of a pair of rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$, the digital control unit responsible for the readout of the TLatches should activate one out of two pairs of signals $R_{TL1\text{-}Sig}$-$R_{TL1\text{-}Ref}$ or $R_{TL2\text{-}Sig}$-$R_{TL2\text{-}Ref}$ to read the input TM sample captured in $TLatch_1$ or $TLatch_2$, respectively. The flow chart shown in Fig. 4.14 shows the algorithm to set/reset $R_{TL1\text{-}Sig}$-$R_{TL1\text{-}Ref}$ signals and the digital circuit shown in Fig. 4.15 is used to implement the algorithm for both pair of $R_{TL1\text{-}Sig}$-$R_{TL1\text{-}Ref}$ and $R_{TL2\text{-}Sig}$-$R_{TL2\text{-}Ref}$ signals. During the time either W_{TL1} or W_{TL2} is "0", the corresponding TLatch is in "Write" phase and its R signals are set to "1" (using NAND1 in Fig. 4.15), so that no reading will be initiated in this phase. To keep a one-to-one correspondence between the input and output pairs of rising edges, each odd or even output should be added to an odd or even input time sample, respectively. At the arrival of an output pair of rising edges labeled with an odd number, the input time sample captured by $TLatch_1$ should be readout. An additional DSwitch block is included in the control unit to set two flag bits, *Odd* and *Even*, to specify the odd or even number of the output pair of rising edges. When W_{TL1}="1", the control unit checks for the *Odd* flag bit to make sure the correspondence between the input and output is satisfied (using AND). Unless there is a simultaneous pair of "11" for W_{TL1} and *Odd*, any rising edges at $\Phi_{OUT,Sig}$

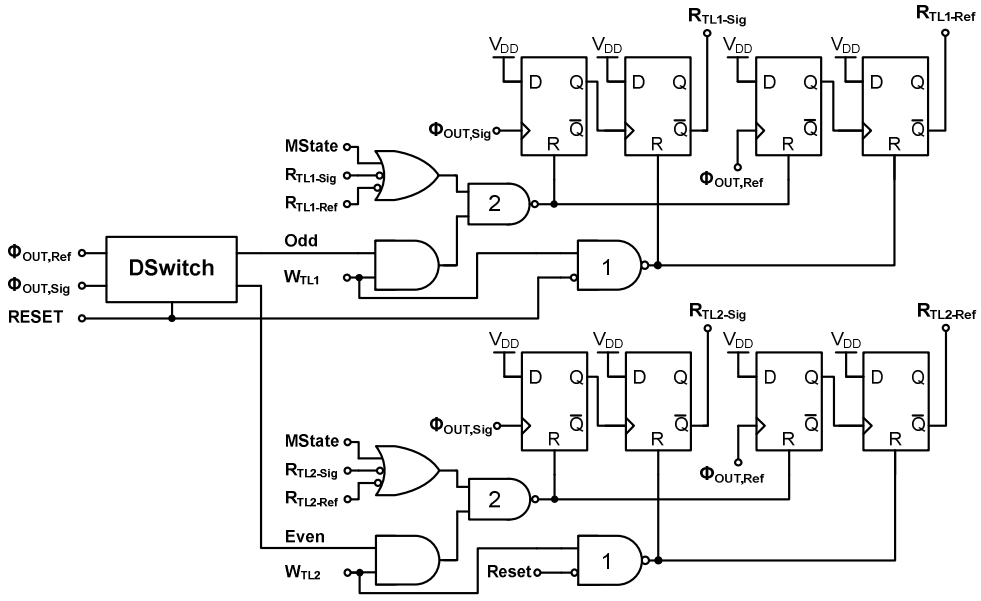


Fig. 4.15. The digital circuit used to generate the *R* reading signals

and $\Phi_{OUT,Ref}$ will be ignored (using AND and NAND2). Confirming the right input-output correspondence, the logic then checks if the pair of rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$ are a matched pair (using OR and NAND2). If *Mstate*="1", the algorithm proceeds to the next stage; otherwise, $R_{TL1,Sig}$ and $R_{TL1,Ref}$ will be checked to see if the first rising edge of the matched pair has been taken into account previously; so that the algorithm can proceed with the second edge. Finally $R_{TL1,Sig}$ or $R_{TL1,Ref}$ will be reset to "0" upon the arrival of the rising edges at $\Phi_{OUT,Sig}$ and $\Phi_{OUT,Ref}$ and the readout of $TLatch_1$ starts.

By starting the readout of the proper TLatch (the proper location in the queue), the circuit shown in Fig. 4.16 will be used to produce the SW_{Sig} and

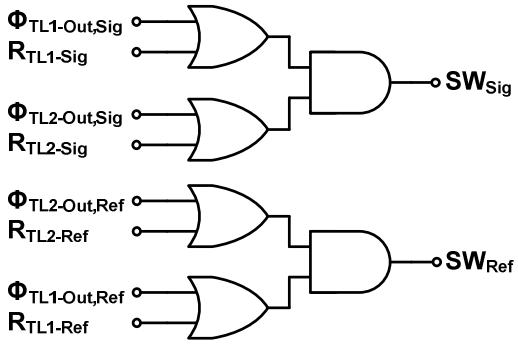


Fig. 4.16. Digital circuit used to control the *SW* signals of the two ring-oscillators in Fig. 4.8

SW_{Ref} signals in Fig. 4.8 and modify the output of the dual-path time-to-time integrator as explained for a single-path time-to-time integrator and according to Eqns. (4.8) and (4.11).

4.4. Practical Considerations

The dual-path time-to-time integrator proposed in section 4.3 deals with TM variables as its input and output. These TM variables are defined as the phase difference between pairs of running edges. While no mechanism is considered to lock the rising edges at the output to the rising edges at the input of the integrator, special attention should be paid to tune the average rate of output production to the average rate of input arrival. In addition, any mismatch between the signal and reference paths alongside the circuit results in different propagation delays for the rising edges in each path. This difference between the differential delays manifests itself as an offset error term. By ignoring this offset component, the output of the integrator might become saturated. In this section, these two subjects will be covered.

4.4.1. The Synchronization between the Input and Output Signals

As explained previously, to satisfy the input-output correspondence between two successive pairs of input edges, one and only one output pair of rising edges should be produced. Since the computational engine does not have any control over the rate of input arrival, the time between each two successive output samples, on average, should be set the same as that of two successive input TM samples. Practically speaking, while a PLL approach for locking the ring-oscillators to a fixed input frequency may be viable, here the integrator takes care of this situation automatically. Provided the maximum period of the output signals, expressed as

$$T_{OUT,Max} = T_{SDU,TLatch} + T_{OUT} \,, \tag{4.13}$$

where $T_{SDU,TLatch}$ represent the T_{SDU} of the SDU inside the TLatch, is less than the average period of the input, the error situation will be limited to the cases where only extra outputs are produced rather than contain both extra and missing output

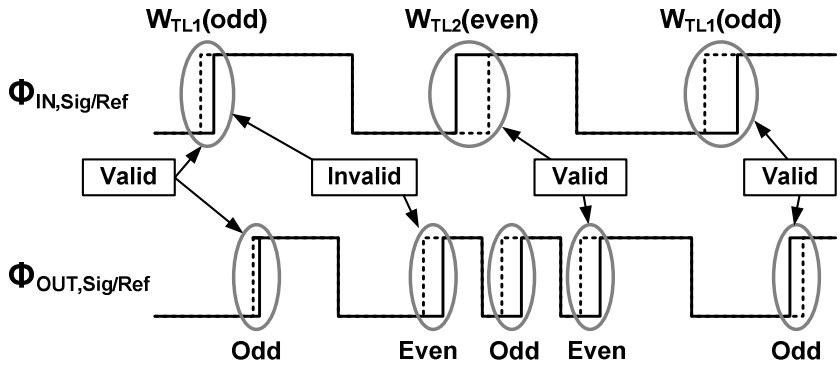


Fig. 4.17. The self-correction feature that compensates for frequency mismatch

pairs of edges. Assuming this condition is met, the integrator will automatically adjust and correct for the extra pair of edges.

As explained earlier, the flag bits W_{TL1}/W_{TL2} and *Even*/*Odd* in Fig. 4.15 are included to verify the odd-to-odd (W_{TL1} AND *Odd*="1") or the even-to-even (W_{TL2} AND *Even*="1") correspondence between the input and output samples. The occurrence of any extra output sample alters the flag bits and indicates a violation of the appropriate edge sequence. Consequently, the out-of-sequence edges will be ignored, as no read phase will be initiated. During the output cycles with no reading, $\Delta T_{SW,Sig}$ and $\Delta T_{SW,Ref}$ in Eqn. (4.8) will be equal to zero and the output TM value will remain the same. This mechanism implements a correction for the errors by pushing the unexpected pair of output rising edges forward and between the next two input samples.

To show how the circuit compensates for the error situation, a sample timing arrangement of the input and output rising edges is shown in Fig. 4.17. Starting from the left-hand side, the first set of edges is in the correct sequence, i.e., odd input and odd output. Next, at the output, an extra set of edges occurs that are designated as even. Subsequently, the integrator output will not be modified and the phase difference between the following set of output edges is identical to that of the previous output, regardless of the input condition. However, the next even output (4^{th} set of edges from the left) will match the even-to-even input-output condition and generate the correct output signal information. For all remaining sets of input and output edges, the situation is monitored and corrected in the same manner.

4.4.2. Mismatches and Calibration

The gate delay of a logic component forms the most basic element of the proposed time-to-time integrator as expected from any TMSP circuitry. Mismatches between signal and reference paths introduce time offsets. Signals associated with the output ring oscillators would be considered the most sensitive element of all where they directly contribute to the output. A similar effect is also present in the TLatches due to mismatches in the SDUs. Such mismatches have large effect on the operation of the integrator. Other signals, such as the signals associated with a TLatch read operation that is derived by a digital circuit without any SDU, are also dependent on mismatch-induced offset errors but on a much reduced scale. Signals associated with a write operation are not sensitive to time offsets at all, as the action associated with the input TM sample occurs long after W_{TL} signals are finalized.

Mismatches between any two corresponding SDUs in the pair of output ring-oscillators results in a signal independent error between the intrinsic oscillation periods of the two ring-oscillators, i.e.,

$$T_{OUT,Sig} = T_{OUT,Ref} + \Delta T_{mm,ring}\,, \tag{4.14}$$

where $\Delta T_{mm,ring}$ represents the algebraic sum of the all mismatches between the T_{SDU} of the corresponding SDUs of the two output ring oscillators. In addition, the mismatches between the SDUs inside each one of the TLatches result in different T_{SDU} values for each SDU and Eqn. (3.10) can be modified accordingly as

$$\Delta T_{OUT} = \Delta t_R + \Delta T_{IN} + \Delta T_{mm,TL}\,, \tag{4.15}$$

where $\Delta T_{mm,TL}$ represents the error between the T_{SDU} values of the two SDUs inside the corresponding TLatch. This error term also includes the minor errors induced during the read operation. Because two TLatches are included in the circuit, each one introduces a different offset component. Considering Eqns. (4.14) and (4.15) and revising Eqns. (4.4)-(4.10), Eqn. (4.11) will be modified as

$$\Delta T_{OUT}[2n] = \Delta T_{OUT}[2n-1] + \Delta T_{IN}[2n-1] + \Delta T_{mm,ring} + \Delta T_{mm,TL1} \tag{4.16}$$

and

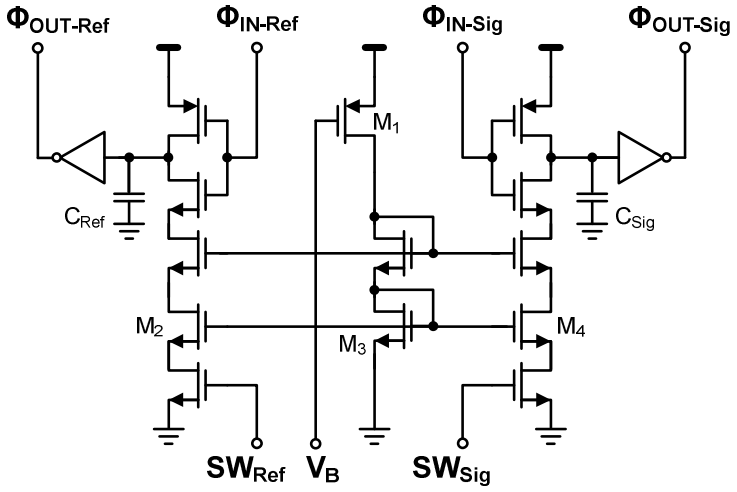


Fig. 4.18. The circuit diagram for a highly matched pair of SDUs

$$\Delta T_{OUT}\left[2n+1\right]=\Delta T_{OUT}\left[2n\right]+\Delta T_{IN}\left[2n\right]+\Delta T_{mm.ring}+\Delta T_{mm.TL2} \tag{4.17}$$

for even and odd-numbered output TM samples, respectively. As shown by Eqns. (4.16) and (4.17), the signal-independent offset error terms associated with the odd and even output samples are different. However, the accumulated error for two successive even and odd output samples is fixed and equal to

$$\Delta T_{offset.even+odd}=2\Delta T_{mm.ring}+\Delta T_{mm.TL1}+\Delta T_{mm.TL2}\,. \tag{4.18}$$

Eqn. (4.18), in turn, results in an average offset value of

$$\Delta T_{offset.mismatch}=\Delta T_{offset.even+odd}/2 \tag{4.19}$$

for each output TM sample.

The above-mentioned analysis confirms that the effect of mismatches between the signal and reference paths all over the integrator manifests itself as a single offset error term given by Eqn. (4.19). This offset can be modeled as an additive voltage component, $\Delta V_{Mismatch}$, associated with the power supply of one SDU (for example SDU_3) in the signal ring-oscillator (shown in Fig. 4.8) compared to the corresponding SDU in the reference oscillator while the rest of circuit is being considered completely matched. Based on Eqn. (3.1), the additive voltage component results in a difference between the propagation delays of the two corresponding delay blocks equal to

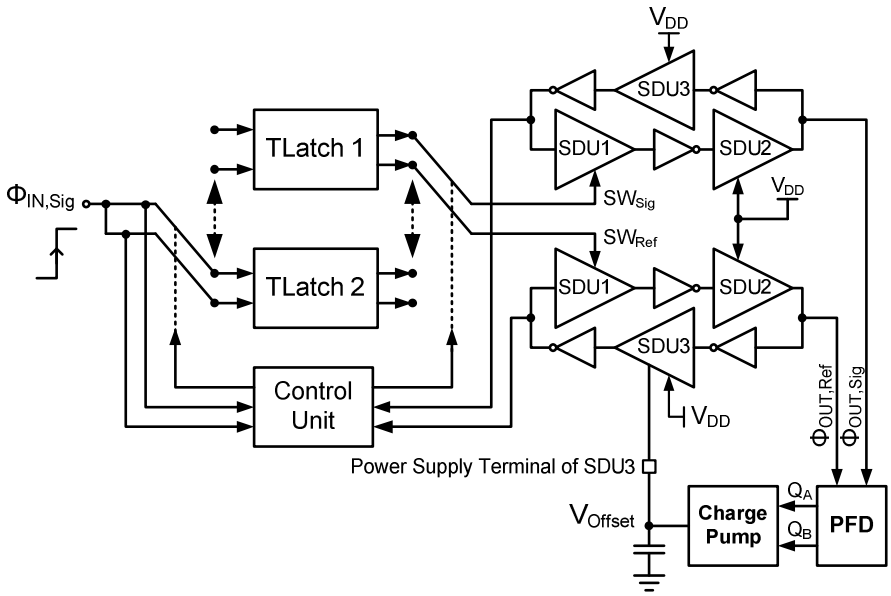


Fig. 4.19. The integrator in calibration configuration

$$\Delta T_{SDU\,3,Mismatch} = \frac{C \times \Delta V_{Mismatch}}{I(V_B)}. \tag{4.20}$$

Considering $\Delta T_{SDU3,Mismatch} = \Delta T_{offset,mismatch}$, the voltage offset representing the total mismatch of the integrator equals to

$$\Delta V_{Mismatch} = \frac{I(V_B) \times \Delta T_{offset,mismatch}}{C}. \tag{4.21}$$

To minimize $\Delta V_{Mismatch}$, layout techniques might be used to decrease the mismatch between the two output ring oscillators. In addition, a differential structure as shown in Fig. 4.18 can used to decrease the mismatches between the two SDUs inside each TLatch. Cascode current mirrors are used to neutralize the channel length modulation of transistors M_2 and M_4 affected by the voltage across the capacitors. This structure provides the possibility of sharing the same bias circuit for both paths and implementing the critical transistors as well as the capacitors with common-centroid or interdigitating structures.

Even after considering all the possible techniques to minimize circuit mismatches, some will be unavoidable. The power supply for SDU_3 in the reference oscillator might be modified to cancel the expected voltage offset, $\Delta V_{Mismatch}$, between the two SDU_3s. A sample calibration topology is shown in Fig.

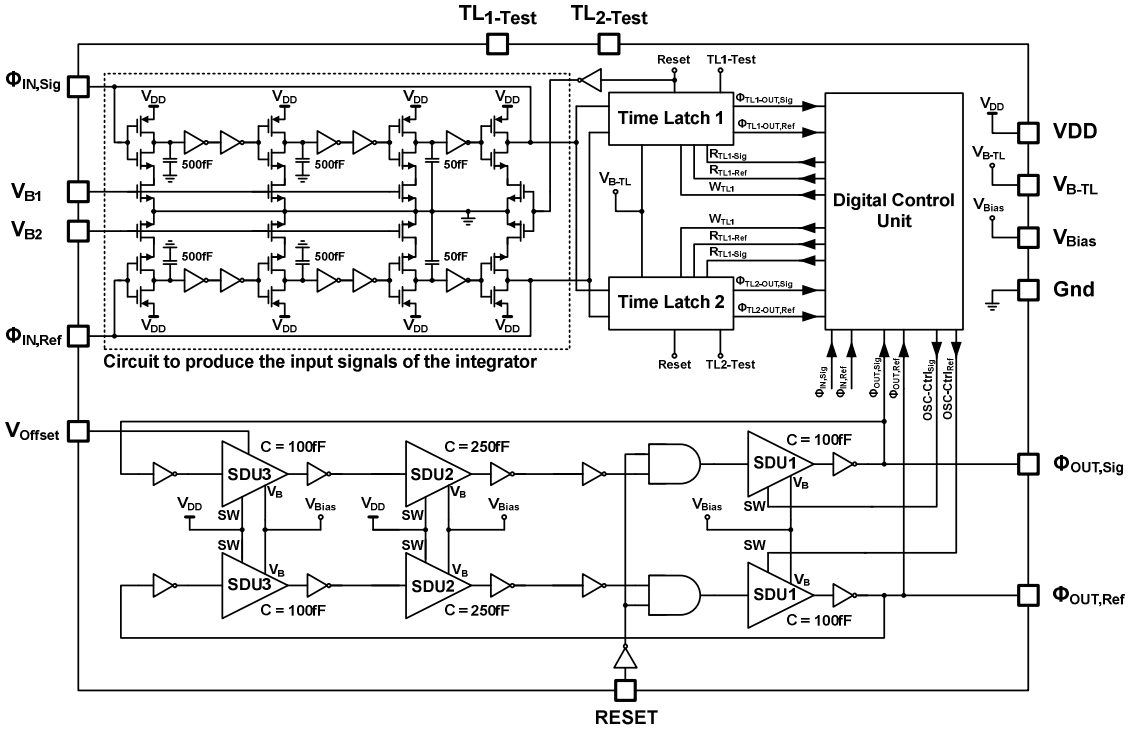


Fig. 4.20. The block diagram of the dual-path integrator fabricated in a 0.13-um IBM CMOS technology

4.19 that can compensate for the mismatches and set the output equal to zero for a zero input. During the calibration cycle, the $\Phi_{IN,Sig}$ and $\Phi_{IN,Ref}$ inputs of the integrator will be connected together to guarantee the input TM sample is equal to zero. With zero input TM samples captured by each TLatch, the average phase difference at the output of the integrator is produced by mismatches, i.e. $\Delta T_{offset,mismatch}$. A PFD (Phase/Frequency Detector) followed by a charge pump is used to produce the voltage V_{Offset} proportional to the output phase difference. Applying this voltage to power supply of SDU_3 in the reference ring oscillator (negative feedback configuration), a phase offset with negative sign will be intentionally imposed between the two ring oscillators to cancel $\Delta T_{offset,mismatch}$. After calibration, the inputs of the TLatches will be released to let the integrator run in its normal operational mode. During the operation of the integrator, calibration cycles should be run periodically to refresh the offset voltage.

4.5. Simulation Results

An integrated circuit prototype of the dual-path time-to-time integrator was

designed and layout in a 1.2V 0.13-μm IBM CMOS process implementing the architecture shown in Fig. 4.20. Transistor dimensions for all circuits are revealed in Appendix A. Two additional ring-oscillators are included on-chip to produce the input signals to the integrator. Through external pins V_{B1} and V_{B2}, the bias voltage for each oscillator is set independently so that there is an intentional frequency difference between the oscillators. The phase difference between these two oscillators is adopted as the asynchronous input to the integrator. The power supply to one of the SDUs in the output ring-oscillators at the lower part of the figure is connected to V_{Offset} to compensate for the mismatch-induced phase difference between the output oscillators of the integrator, as explained in the previous sections. On-chip capacitors are included as well to reduce any digital noise on the power supplies. In order to reduce the noise coupling between different parts of the circuit and control the noise behavior of the integrator, separate bias voltages are considered for each section. Also during the layout, symmetrical placement and routing between the components was performed meticulously.

For calibration purposes, two extra I/O pins were added and denoted as $TL_{1\text{-}Test}$ and $TL_{2\text{-}Test}$ (at the top of the Fig. 4.20). Applying a digital “0” at either one of these pins, will cause the differential input to the corresponding TLatch to be shorted together so that a zero input condition is realized. In addition, an input Reset pin is included to restore the initial conditions within the digital control unit whenever needed. This signal is also used to stop the oscillations in all oscillators. When the digital signal *RESET* is high, the oscillators are turned off and when this signal is low the oscillators run. This cutoff mechanism forces the corresponding oscillators to begin their oscillations in phase with one another. The output signals of both oscillators are buffered to I/O pins to facilitate the testing of the prototype.

To verify the behavior of the dual-path time-to-time integrator, the circuit of Fig. 4.20 was simulated with Spectre using post-layout extracted data. The TM variable input applied to the integrator was composed of two digital square-wave signals with slightly different periods of 435 ns and 436 ns (at frequencies of

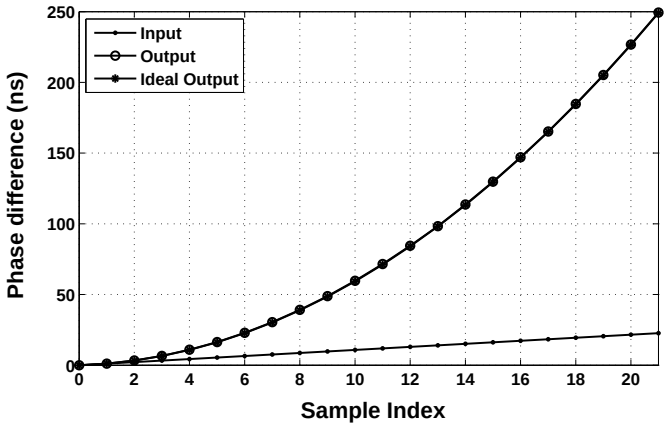


Fig. 4.21. The simulated phase difference at the input and output of the proposed time-to-time integrator

2.29885 MHz and 2.29357 MHz, respectively) resulting in an increasing phase difference between the two input signals with steps of 1 ns. The output response is shown in Fig. 4.21 and compared with the ideal or expected response (i.e., Eqn. (4.1)). As is evident, the simulated results agree with the theoretical result. A closer look reveals the maximum error between the simulated and the ideal response is no greater than 36 ps, resulting in a relative error of no larger than 0.014%. The output response is limited to 250 ns, as this is the period of the average frequency of the output signal of 4 MHz. This represents the upper limit of output operation for the integrator.

4.6. Experimental Results

The microphotograph of the integrated circuit prototype of the dual-path

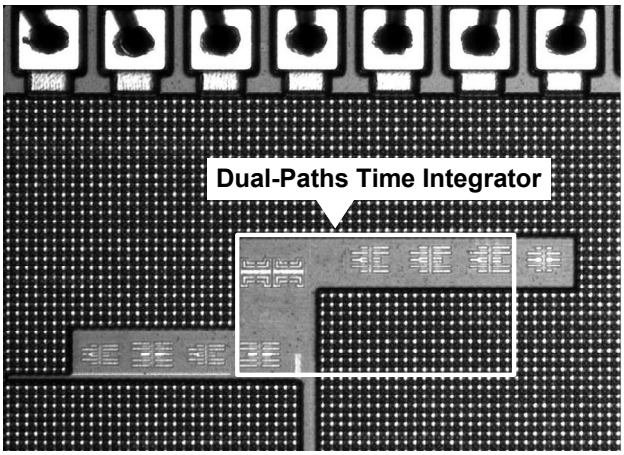
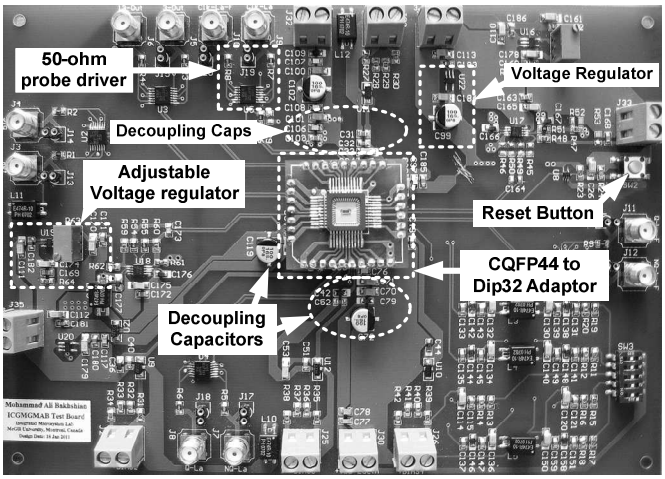
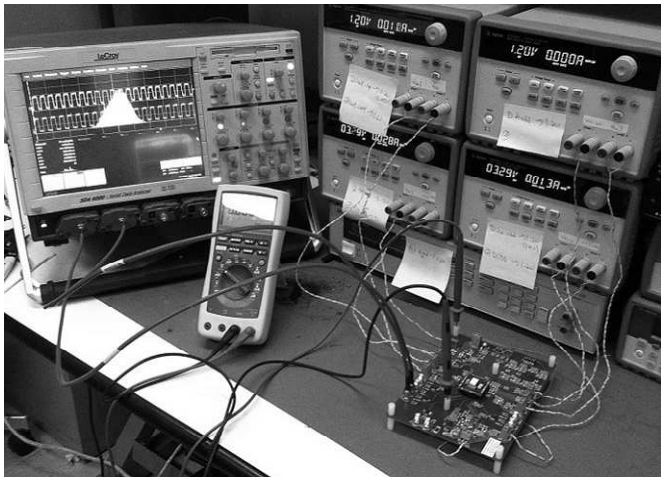


Fig. 4.22. Microphotograph of a test chip implementing a dual-path time-to-time integrator



(a)



(b)

Fig. 4.23. The customized board designed to test the integrator circuit, (b) the test environment setup

time-to-time integrator implemented in a 1.2V 0.13-µm IBM CMOS process is shown in Fig. 4.22. The integrator occupies an area of 320µm×160µm, while part of the circuit in the figure is covered by a passivation layer. Other circuits are also shown in the photograph; these are unrelated to the integrator and used for another purpose.

The IC was mounted on a custom two-layer PCB through a custom CQFP-to-DIP adaptor as shown in Fig. 4.23.a. The test board included extra features for testing other building blocks implemented on the same die with the integrator. Regarding the test of the integrator, separation of the digital and DC biasing

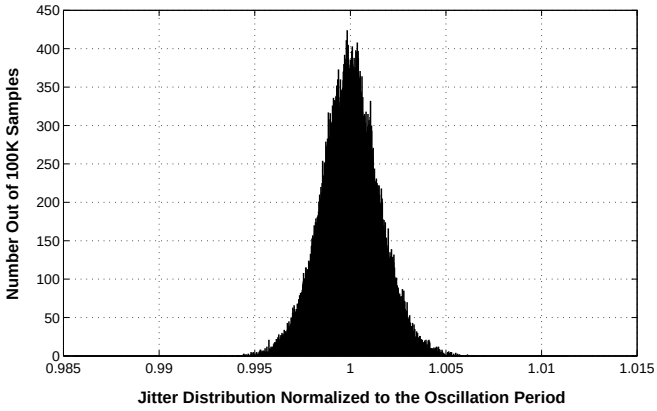


Fig. 4.24. The period jitter distribution at $\Phi_{OUT\text{-}Sig}$

tracks was considered carefully in order to avoid any possible coupling of the digital noise into the bias circuit. When separation was not possible, orthogonal crossovers were implemented. In addition to off-chip decoupling capacitors, LC chokes were used to block common-mode digital noise signals. Fixed and adjustable voltage regulators (Analog Devices ADP170/171) were used to provide different bias voltages needed to bias the integrator. Finally, non-inverting line drivers (74LV125) were used to drive off-chip digital signals to a digital scope through 50-ohm probes.

The test environment consisted of a LeCroy 6000 Serial Data Analyzer (SDA), Agilent (Infiniium 54830D) oscilloscope and DC voltage power supplies. The digital output data was analyzed and processed in MATLAB and the relevant parameters and test results were extracted. The test setup is shown in Fig. 4.23.b.

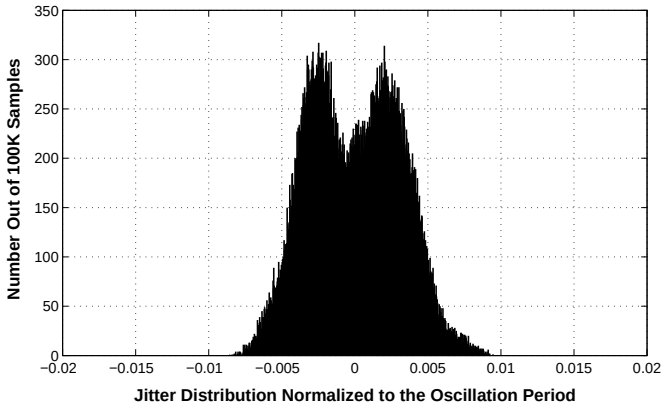


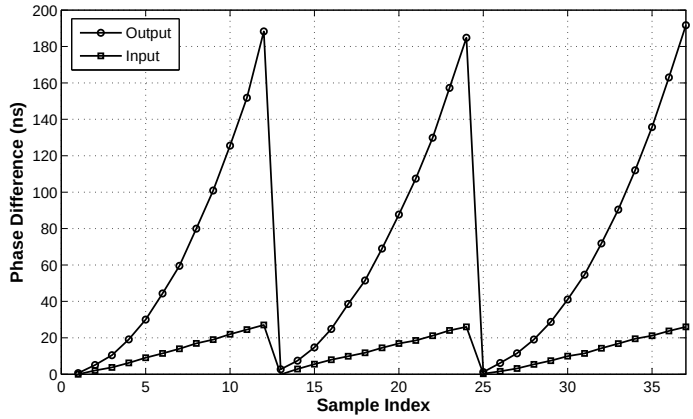
Fig. 4.25. Output distribution of the integrator after calibration for zero input

By setting the control voltage of the SDUs in the output ring-oscillators (i.e., using V_{Bias} in Fig. 4.20) at zero voltage, the oscillation frequencies of the output oscillators were set at its maximum value, close to 5 MHz. By letting the two output ring oscillators to operate in a free running mode without any interruption through the control unit, the jitter at the output of each oscillator followed a distribution that was similar to a Gaussian one, as shown in Fig. 4.24 for the signal oscillator. To calibrate for mismatches, the inputs to the two TLatches were shorted together by connecting digital pins $TL_{1\text{-}Test}$ and $TL_{2\text{-}Test}$ to Gnd. This established a zero input condition at the input of each TLatch so that the output time offset was expected to be measured zero for zero input. As explained in section 4.4.2, V_{offset} (in Fig. 4.20) was manually trimmed until the average value of the output phase difference became zero. It should be mentioned that the calibration procedure is not utilized to remove the noise (jitter); it will be used to set the average value of the noise equal to zero to avoid the saturation of the integrator output. Fig. 4.25 shows the distribution of the integrator output for 100K samples after calibration and while the input was set to zero. As is evident, the distribution of the output is multi-modal consisting of several Gaussian-like distributions. The authors believe that the multi-modal distribution is due to the different offset values for each TLatch and the fact that the jitter distribution at one oscillator is correlated with the jitter of the other oscillator. The correlation happens because the digital noise induced in one of the oscillators may couple to the other oscillator through the power supply and influence its jitter-induced error. It should be mentioned that the calibration procedure is not utilized to remove the noise (jitter); it will be used to set the average value of the noise equal to zero to avoid the saturation of the integrator output.

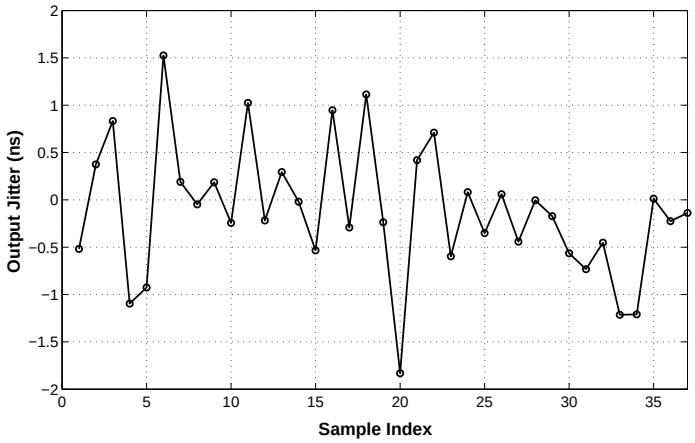
An input ramp with an average step of 2.43 ns/sample was applied to the input of the integrator to measure its input-output integration operation. This ramp was created through two additional front-end ring oscillators that beat at two different frequencies to create the ramp signal in time (see top left hand side of Fig. 4.20). Bias voltages V_{B1} and V_{B2} controlled the frequencies of each ring

oscillator. These voltages, of approximately 0.6V, were adjusted so that a beat frequency of 2.5 MHz was established. To avoid the output saturation, the integrator was reset once the output exceeded the saturation level. This avoided any residual or divergence effects to be carried forward into the next integration cycle.

The experiment was allowed to continue so that approximately 10,000 points could be collected for post-processing. Three cycles of the input and output collected data are illustrated in Fig. 4.26(a) on the same sample index. Adding any more cycle would simply clutter the diagram. As shown in the figure, the output of the integrator saturated at different levels before 200 ns, which is the period of the oscillating signals at the output of the two output ring oscillators



(a)



(b)

Fig. 4.26. Measured behavior of the integrator to a ramp input: (a) input-output instantaneous signal, (b) error between the experimental and theoretical output signals

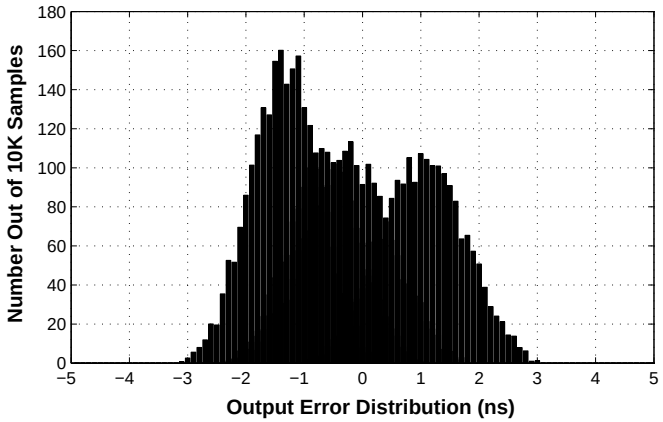


Fig. 4.27. Error between the experimental and theoretical output signals for close to one thousand cycles

(for the oscillation frequency equal to 5 MHz). Superimposing the ideal or expected output reveals little detail, as they are very similar. Instead, Fig. 4.26(b) illustrates their time difference as a function of the sample index. For the illustrated data, the error ranged from -1.9 ns to 1.5 ns. To get more insight into the error associated with the operation of the integrator, Fig. 4.27 shows the output error distribution for 10,000 output samples over the same input range. The error distribution appears multi-Gaussian with three main peaks bounded between ±3 ns, which are close to ±1.5% of the full range (200 ns). The error distribution is both positive and negative, indicating its source is due to noise, such as thermal noise, noise pick-up from poor power and ground supplies, or EMI from external lines or vias.

Finally, the experiments revealed that the static power consumed by the integrator was around 1 mW. It should be mentioned that this design was not optimized for power, as many of the flip-flops were held in a power hungry mode of reset.

4.7. Summary

In this chapter, time memory cells called TLatches were utilized to develop a dual-path time-to-time integrator using digital circuits. This is the first realization of a circuit that integrates an input time variable and produces a corresponding output variable in the same domain. Mismatch effects internal to the integrator

can be eliminated through a simple and effective digital-based calibration procedure. Essentially, calibration is performed by frequency aligning the outputs of two oscillators; hence, there is no need for trimming or any reference element. A circuit prototype was implemented in a 1.2-V 0.13-µm IBM CMOS process and it confirmed the operation of the integrator. The integrator performed with a peak error of 1.5% over full-scale. This circuit is expected to be the basis for other time-mode signal processing circuits, like high-order delta-sigma modulators and frequency-selective filter circuits.

Chapter5: The Implementation of a Second-Order Delta-Sigma Modulator in TMSP

5.0. Introduction

Delta-Sigma (ΔΣ) modulation [14] might be considered as one of the most widely used techniques in analog design. It has dominated the electronics industry in applications with high resolution and relatively low bandwidth requirements. Delta-sigma analog-to-digital conversion is a unique classification of data conversion that uses oversampling and feedback to achieve a high output ratio of the signal-to-noise. Although the output of such a modulator is a serial stream of digital bits, analog building blocks are the main components of this implementation. In this chapter, by taking advantage of time-mode signal processing (TMSP) and the time-to-time integrator proposed in Chapter 4, a digital architecture is proposed to implement a time-mode second-order delta-sigma modulator. It is believed by the author that the proposed technique is applicable to higher orders of ΔΣ modulators as well.

5.1. Delta-Sigma Modulators

The operation of a first-order ΔΣ modulator is best described with the error feedback model shown in Fig. 5.1.a. The input analog value V_{IN} assumed to be represented by a real number is converted to an output integer value D_{OUT} through a quantizer. Normally, D_{OUT} is formatted using a binary number representation. The digital output is converted back into an analog value V_{OUT}

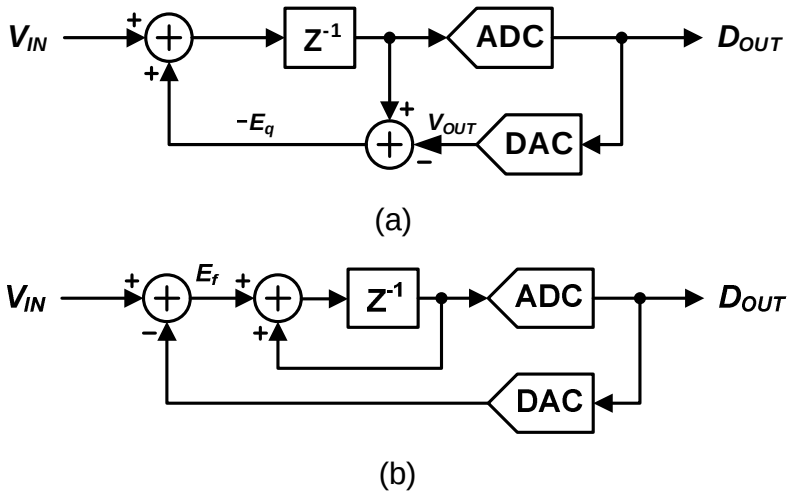


Fig. 5.1. The first order ΔΣ modulator (a) error-feedback and (b) output-feedback models

using a DAC and this voltage is subtracted from the current input V_{IN} to produce the error signal E_q, which represents the ADC's quantization error. The quantization error signal is subtracted from the next input value to be converted. A time-domain analysis of the model depicted in Fig. 5.1.a reveals the input-output difference equation given by

$$V_{OUT}[n] = V_{IN}[n-1] + \left(E_q[n] - E_q[n-1]\right), \tag{5.1}$$

Applying z-transform to both sides of Eqn. (5.1) results in

$$V_{OUT}(z) = z^{-1}V_{IN}(z) + \left(1 - z^{-1}\right)E_q(z). \tag{5.2}$$

As Eqn. (5.2) shows that an undistorted delayed version of the input voltage signal will be forwarded to the output; while, the second term reveals the quantization error $E_q(z)$ is multiplied by the term "$(1-z^{-1})$". For physical frequencies, i.e., $z=e^{j\omega}$, this term is near zero in magnitude at low frequencies, but increases to two as the frequency approaches one-half the sampling frequency. Hence, the low-frequency spectral content of the quantization noise is suppressed but its higher frequency components are magnified. This results in an increase of the signal-to-noise ratio (SNR) over a range of frequencies near DC. In addition, one can show that the quantization noise power over one-half the sampling frequency generated by the ΔΣ modulator is equal to the quantization noise generated by the quantizer without feedback and over the same range of

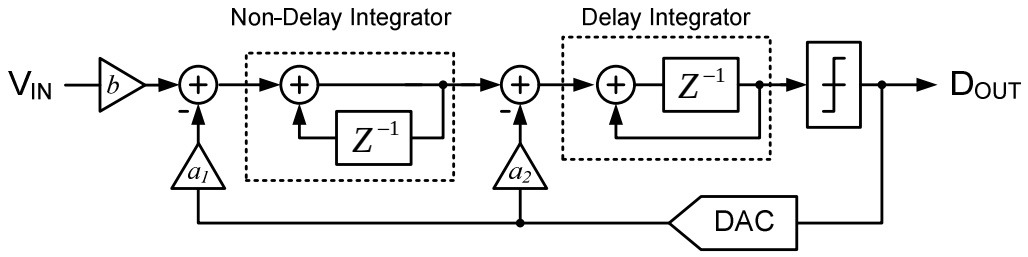


Fig. 5.2. Second-order delta-sigma modulator

frequency. Hence, ΔΣ modulation does not remove the quantization error but rather shifts it out of the frequency band of interest. This process is known as noise shaping [14].

The implementation of a first-order ΔΣ modulator is routinely based on the topology illustrated in Fig. 5.1.b, which is formed by simply rearranging the error-feedback model of Fig. 5.1.a. The internal positive feedback loop formed with the delay element is typically realized as an analog integrator. The outer negative feedback loop requires an analog summation block. The most common ΔΣ configurations use a single-bit quantizer (i.e., a comparator). This is because the use of a 1-bit quantizer would necessitate a 1-bit feedback DAC, which are both linear in nature.

The oversampling behavior of a ΔΣ modulator gives rise to the term oversampling ratio (OSR). This quantity is expressed as

$$OSR = \frac{F_S}{2F_{BW}} \tag{5.3}$$

which reflects how much greater the sampling frequency F_S is over the Nyquist rate of the incoming signal, i.e., $2F_{BW}$; where F_{BW} is the largest input signal frequency that the modulator would exercise. Provided the input signal to the output quantizer stays within its linear range, the maximum signal-to-noise ratio (SNR) for a first-order single-bit ΔΣ modulator [14] may be calculated as

$$SNR = 7.78 + 30\log(OSR). \tag{5.4}$$

Therefore, for a first-order design, the resolution of a ΔΣ modulator is governed by the oversampling ratio. Eqn. (5.4) along with technology constraints poses an upper bound on the performance of first-order ΔΣ modulators.

Higher-order delta-sigma modulators, which increase the number of integrators, offer significant SNR improvements. For example, the SNR for the second-order architecture [20] in Fig. 5.2 can be expressed as

$$SNR = 17.16 + 50\log(OSR). \quad (5.5)$$

It may be inferred from Eqns. (5.4) and (5.5) that if the OSR is doubled for a first-order ΔΣ modulator, the SNR improves by 1.5-bits of resolution. Whereas, a second-order ΔΣ modulator improves by 2.5-bits, third and higher-order ΔΣ modulators will offer even better SNR performance.

5.2. Time-Mode Delta-Sigma Modulator

As previously explained in Chapter 5, in most recently developed time-based structures like VCO-based data converters [18,19], TMSP has been adopted to develop first-order quantization noise shaping to develop very affordable low power digital data converters. Attempts to increase the order of the modulator to improve its conversion resolution has been through the inclusion of additional analog building blocks such as that reported in [58] for a second-order delta-sigma modulator and [21] for a third-order modulator. In [11], the authors have developed a different topology for a first-order time-mode delta-sigma modulator where two ring-oscillators are utilized as a voltage-to-time integrator. Unfortunately, the technique is limited to a first-order topology as the addition of two or more time-mode signals was not deeming possible at that time. This, in turn, prevents the cascade of several back-to-back integrators to create high-order modulators. A third-order ΔΣ TDC has been recently reported in [53]; however, the modulator is implemented in a 1-1-1 MASH structure avoiding the need for cascading integrators to achieve higher orders of modulation. While this approach is certainly a valid direction, the technique is not applicable to develop the classic second-order modulator or other topologies such as leapfrog architecture.

At this very early stage of time-mode circuits, it is necessary to establish a systematic approach to implement ΔΣ modulators of orders higher than one. To present the proposed solution, we start by a brief review of a previously reported

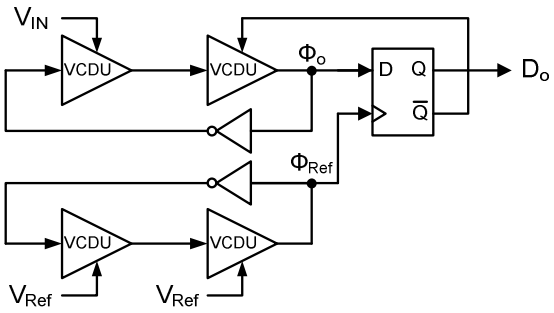


Fig. 5.3. First-order delta-sigma modulator

first-order ΔΣ modulator. Following that, by adopting the time-to-time integrator developed in Chapter 4 a digital technique to implement a second-order time-mode ΔΣ modulator is proposed. The technique used to implement this architecture might be used to design higher orders of such a modulator.

5.2.1. First-Order Time-Mode Delta-Sigma Modulator

As it was mentioned in Chapter 2, in [11] a compact structure to implement a first-order time-mode ΔΣ modulator was presented. As shown in Fig. 5.3, this modulator is composed of two voltage-controlled ring oscillators followed by a digital D-Flip-Flop. Any difference between the input analog voltage V_{IN} and the reference voltage V_{REF} will be integrated as the phase difference between the rising edges at Φ_O and Φ_{REF}, as it was explained for the voltage-to-time integrator in Chapter 2. The output DFF operates as a single-bit quantizer (comparator) to return a digital “0” or “1” based on the sign of the phase difference at the output of the voltage-to-time integrator. Finally, the digital output of the modulator, D_O with a voltage amplitude of v_O, is used as the control voltage for a VCDU in the signal ring-oscillator (top one in Fig. Fig. 5.3). The error signal $\Delta T_\varepsilon[n]$ made by the flip-flop comparison may be expressed as its output voltage amplitude from the DFF scaled by G_ϕ minus time difference of the rising edges of the outputs from the two ring oscillator, i.e.

$$\Delta T_\varepsilon[n] = G_\phi v_o[n] - \Delta T_O[n]. \tag{5.6}$$

Here, G_ϕ represents the voltage-to-time conversion coefficient of the VCDUs inside the ring-oscillators. Following the equations in [11], the relation between the input and output of the modulator can be extracted as

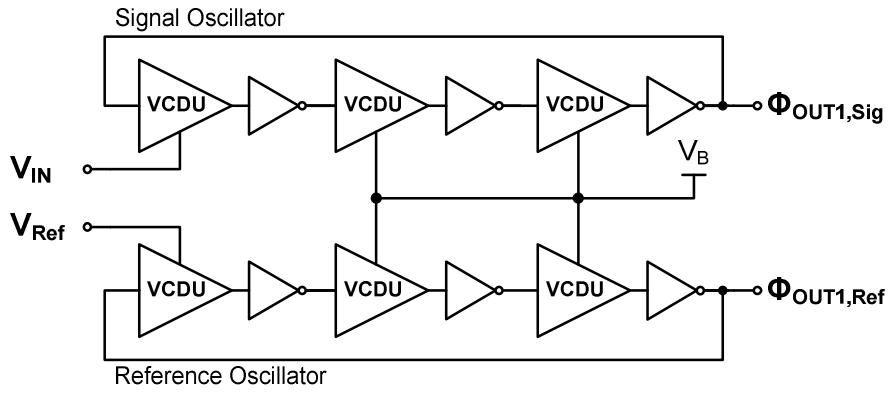


Fig. 5.4. The voltage-to-time integrator

$$v_o[n] = v_{in}[n-1] + \frac{1}{G_\phi}\{\Delta T_\varepsilon[n] - \Delta T_\varepsilon[n-1]\} \tag{5.7}$$

where $v_{in}[n]=V_{in}[n]-V_{REF}$. Eqn. (5.7) is similar to Eqn. (5.1) and reveals the first-order ΔΣ modulator difference equation.

5.2.2 Second-Order Time-Mode Delta-Sigma modulator

By taking advantage of the time-to-time integrator proposed in the previous chapter, it is possible to implement the cascade of two integrators in TMSP to increase the order of a delta-sigma modulator.

As shown in the previous section, a typical second-order ΔΣ modulator is composed of two integrators as shown in Fig. 5.2. It consists of a voltage input and a digital output. For a second-order ΔΣ modulator implemented using TMSP, the signals at the boundary of this modulator are the same. However, the intermediate signals internal to the ΔΣ modulator are made as time-mode signals. For instance, the first integrator block will integrate the difference between the input voltage and the feedback signal coming from the DAC to produce a time-mode output. This TM output becomes the input to the second integrator together with a time-mode feedback signal driven by the DAC. The output of this integrator is also TM signal. In other word, the first integrator is a voltage-to-time integrator while the second one is a time-to-time integrator.

The voltage-to-time integrator presented in Chapter 2 is shown in Fig. 5.4 and it might be used to implement the first integrator. Two ring-oscillators are included in the circuit and each loop is composed of voltage-controlled delay

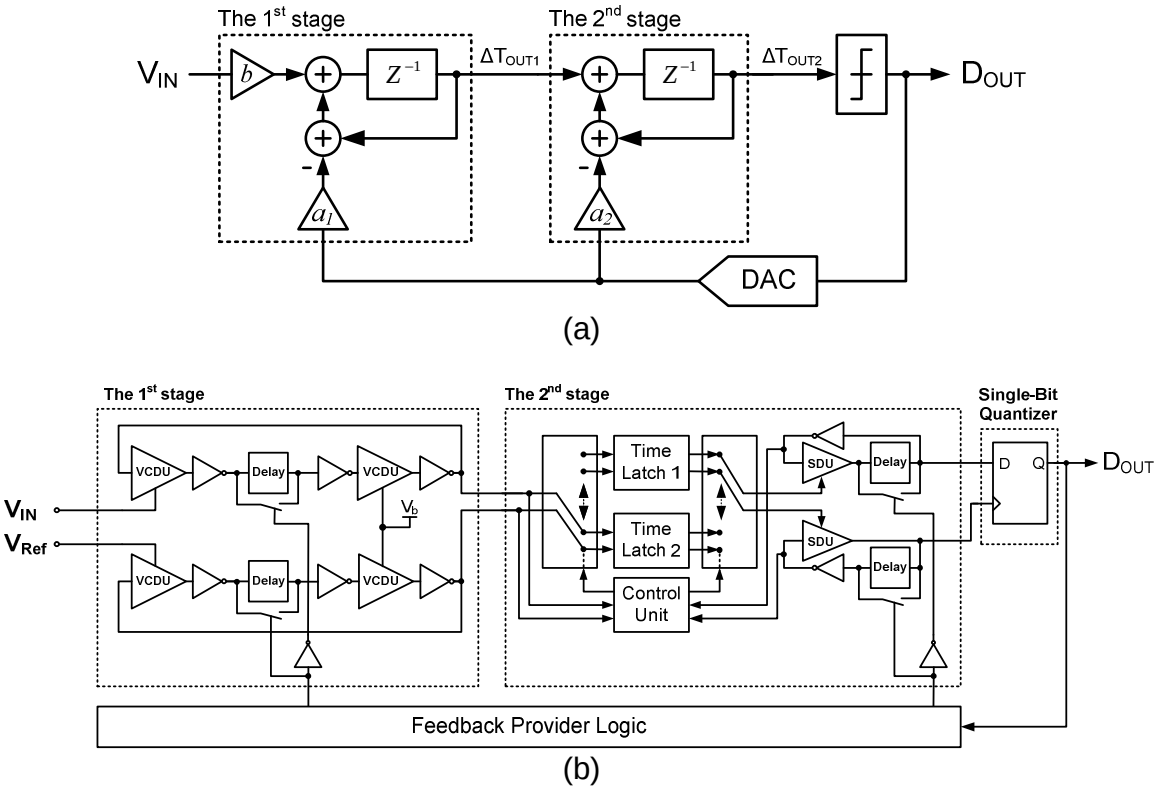


Fig. 5.5 (a) The Boser-Wooley second-order delta-sigma modulator, (b) The block diagram for a second-order TM delta-sigma modulator

units (VCDU) and digital inverters. A VCDU has the same structure as the SDU presented previously in Chapter 3 where the SW input to the delay unit is continuously connected to V_{DD} and the bias voltage V_B is used as an input to set the propagation delay T_{VCDU} of the VCDU, i.e.

$$T_{VCDU} = G_{\phi} V_B \tag{5.8}$$

where $G_{ø}$ is the voltage-to-time conversion factor of the VCDU. Following the equations presented in Chapter 2, the phase difference (i.e. ΔT_{OUT1}) between the rising edges at $\Phi_{OUT1,SIG}$ and $\Phi_{OUT1,REF}$ will be related to the differential input voltage according to

$$\Delta T_{OUT1}[n] = \Delta T_{OUT1}[n-1] + G_{\phi} v_{in}[n-1]; \tag{5.9}$$

where $v_{in}[n]=V_{in}[n]-V_{REF}$. Eqn. (5.9) shows that the circuit operates as a voltage-to-time integrator with a full delay having a transfer function given by

$$\Delta T_{OUT1}(z) = \frac{z^{-1}}{1 - z^{-1}} v_{in}(z). \tag{5.10}$$

The voltage-to-time integrator is cascaded with a time-to-time integrator that can be implemented using the architecture presented in Chapter 4. The transfer function for this integrator includes a full delay as well, i.e.,

$$\Delta T_{OUT2}(z) = \frac{z^{-1}}{1 - z^{-1}} \Delta T_{IN2}(z). \tag{5.11}$$

Noting that both integrators have a full delay term in their transfer function, the Boser-Wooley topology [14] should be adopted to implement the second-order modulator, as shown in Fig. 5.5.a. By replacing each integrator with its proper time-mode counterpart, the diagram shown in Fig. 5.5.b will be concluded for the second-order time-mode ΔΣ modulator; as shown in the figure, a D-type Flip-Flop is used as the output single-bit quantizer. To implement the feedback to each stage, one digitally controlled delay component is included within each ring-oscillator of both integrators. The input-output propagation delay for these feedback components, that are implemented using the SDU block developed in Chapter 3, can be bypassed by a digital signal. As explained in section 5.2.1 by activating the bypass input of the SDU, the input-output delay of the SDU will be shortened as low as a cascade of two digital inverters. By applying two complementary digital signals to the two SDUs of each integrator, an intentional phase difference will be added to the output phase difference of that integrator. This technique can be used to implement feedback to both integrators; however, as will be explained in the next section, some additional logic is needed to make sure the asynchronous operation of each integrator does not violate the causality condition of asynchronous operation.

To explain the operation of the modulator in more details, the symbolic illustration of the operating signals for the input and output of the modulator and the outputs of each integrator are shown in Fig. 5.6. As explained in the previous chapter, between each pair of TM samples at the output of the first integrator which is assumed as the input to the second integrator, one set of TM output is evaluated at the output of the second integrator. The output DFF in Fig. 5.5.b

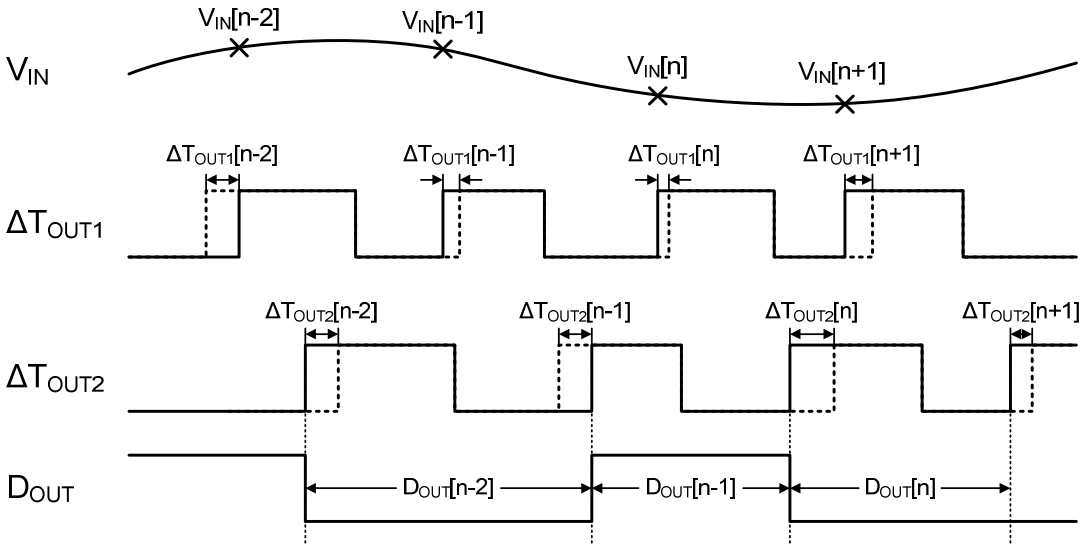


Fig. 5.6. The symbolic illustration of the operating signals for the modulator in shown in Fig. 5.5

produces the output digital bit D_{OUT} and this bit will be feedback to the input of both integrators through the feedback provider logic. The output of the second integrator, ΔT_{OUT2}, will be calculated as

$$\Delta T_{OUT2}[n] = \Delta T_{OUT2}[n-1] + \Delta T_{OUT1}[n-1] - a_2 \times D_{OUT}[n-1]. \tag{5.12}$$

Performing z-transform to both sides of Eqn. (5.12) results in

$$(1-z^{-1}) \times \Delta T_{OUT2}(z) = z^{-1}\Delta T_{OUT1}(z) - a_2 \times z^{-1} D_{OUT}(z). \tag{5.13}$$

The quantization error, ΔT_{ε}, associated with the output quantizer is defined as

$$\Delta T_{\varepsilon}[n] = D_{OUT}[n] - \Delta T_{OUT2}[n] \tag{5.14}$$

and substituting Eqn. (5.14) in Eqn. (5.13) results in

$$(1 - z^{-1} + a_2 z^{-1}) \times D_{OUT}(z) = (1-z^{-1})\Delta T_{\varepsilon}(z) + z^{-1}\Delta T_{OUT1}(z). \tag{5.15}$$

Considering $a_2=1$, Eqn. (5.15) represents a first-order delta-sigma modulation and the architecture shown in Fig. 5.5.b may be easily changed to a first-order delta-sigma modulator for TM inputs by removing the first integrator and its connections.

After modifying Eqn. (5.9) to introduce the feedback component, the equation to evaluate the output of the first integrator will be

$$\Delta T_{OUT1}[n] = \Delta T_{OUT1}[n-1] + b \times v_{in}[n-1] - a_1 \times D_{OUT}[n-1], \tag{5.16}$$

where $b=G_{ø}$. Again, by applying z-transform to both sides of Eqn. (5.16) the result will be

$$\Delta T_{OUT1}(z)=\frac{b\times z^{-1}}{1-z^{-1}}v_{in}-\frac{a_1\times z^{-1}}{1-z^{-1}}D_{OUT}(z). \tag{5.17}$$

By replacing $\Delta T_{OUT1}(z)$ in Eqn. (5.15) by Eqn. (5.17), the expression representing the relation between the input and output of the modulator shown in Fig. 5.5.b will be equal to

$$D_{OUT}(z)=\frac{(1-z^{-1})^2}{Den(z)}\Delta T_{\varepsilon}(z)+\frac{b\times z^{-2}}{Den(z)}v_{in}(z) \tag{5.18}$$

where,

$$Den(z)=1+(a_2-2)\times z^{-1}+(1+a_1-a_2)\times z^{-2}. \tag{5.19}$$

According to Eqn. (5.19), the signal transfer function (*STF*) and noise transfer function (*NTF*) is equal to

$$STF(z)=\frac{b\times z^{-2}}{Den(z)} \tag{5.20}$$

and

$$NTF(z)=\frac{(1-z^{-1})^2}{Den(z)} \tag{5.21}$$

respectively. To achieve $STF(z)=b\times z^{-2}$ and $NTF(z)=(1-z^{-1})^2$, the conditions $a_1=1$ and $a_2=2$ must be satisfied. Coefficient *b* is the input voltage-to-time conversion factor and should be set during the design of the VCDU block. In the next section, more information regarding the implementation of the second-order time-mode delta-sigma (TMDS) modulator will be provided.

5.3. Silicon Implementation

From a practical point of view, there are some issues regarding the silicon implementation of the above-extracted equations. As explained earlier, there is no timing synchronization between the oscillating signals at the outputs of the two integrators. The digital control unit, described in Chapter 4, only regulates the one-to-one correspondence between the pairs of rising edges at the output of the

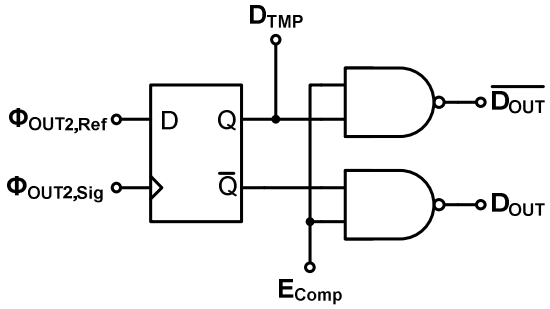


Fig. 5.7. The digital configuration to produce the digital output of the modulator

two integrators; i.e., one and only one odd (even) TM output should be produced at the output of the second integrator after an odd (even) TM output is produced at the output of the first integrator. Due to the asynchronous operation of the time-mode modulator, special care should be taken to apply the right feedback signal to each integrator; also, the timing characterization of the modulator is necessary to guarantee there would be no conflict between the arrival times of the rising edges at the output of the integrators. Moreover, the linear range of the input voltage-to-time converter and the non-uniform sampling at the input of this modulator are the other concerns that should be investigated. This section covers these issues in more details.

5.3.1. Feedback Implementation

The digital output of the modulator is produced through the sign detection of the TM variable at the output of the second integrator (i.e. $\Delta T_{OUT2}[n]$). By applying the rising edges at $\Phi_{OUT2,SIG}$ and $\Phi_{OUT2,REF}$ to the *Clock* and *D* inputs of a DFF, as shown in Fig. 5.7, the output of the DFF (D_{TMP}) will be set to “0” if the rising edge at the *Clock* input leads the rising edge at the *D* input. On the other hand, if the *Clock* edge lags the *D* edge, the output D_{TMP} will be set to “1”. D_{TMP} might be considered as a preliminary output of the modulator. When extra cycles are being produced to force the one-to-one correspondence between the two integrators, as explained in the previous chapter, the TM variable at the output of the second integrator should be preserved without any modification; so, no feedback should be applied. To satisfy this requirement, two NAND gates proceeds the outputs of the DFF to fix both feedback signals at the same level

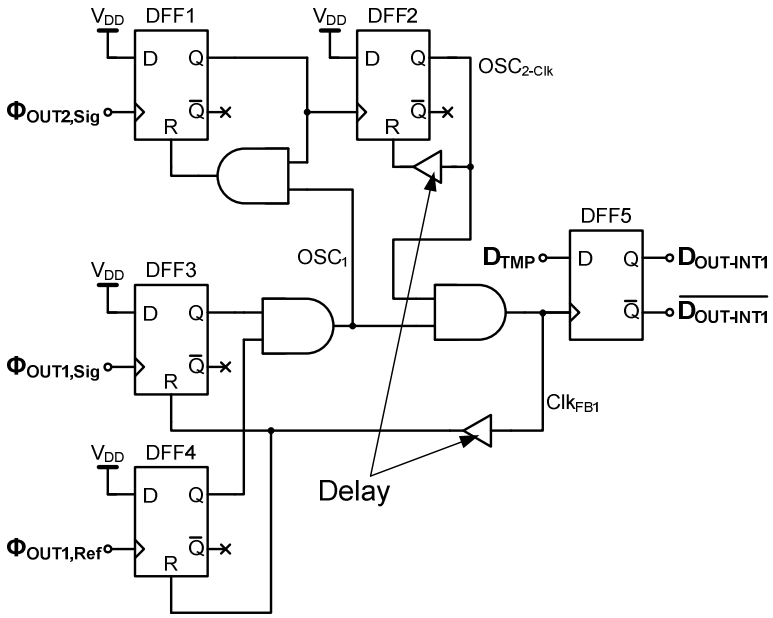


Fig. 5.8. The circuits to produce the feedback signal for the second integrator

(for example “1”) when E_{Comp} is “0”. E_{Comp} is the flag bit that determines the condition when extra cycles are in progress. D_{OUT} and $\overline{D_{OUT}}$ are the digital outputs of the modulator and they are applied directly to the second integrator.

Considering the timing diagram shown in Fig. 5.6, the n-th pair of the rising edges at the output of the second integrator (the signals representing $\Delta T_{OUT2}[n]$) arrives after the n-th pair of the rising edges at the output of the first integrator (the signals representing $\Delta T_{OUT1}[n]$) have arrived. To apply the right feedback to the first integrator, the n-th digital output of the modulator, i.e. $D_{OUT}[n]$, that is produced according to $\Delta T_{OUT2}[n]$ should be used to produce $\Delta T_{OUT1}[n+1]$. In other words, after the pair of rising edges for $\Delta T_{OUT1}[n]$ arrives at the output of the first integrator, the next D_{TMP} produced by the rising edges for $\Delta T_{OUT2}[n]$ should be latched to be feedback to the first integrator.

To implement this strategy, the circuit shown in Fig. 5.8 can be used. Starting from an initial reset condition, flag bit OSC_1 will set to “1” when an “11” state appears at the outputs of DFF3 and DFF4. This flag bit determines the full arrival of a matched pair of rising edges at the output of the first integrator (i.e. $\Delta T_{OUT1}[n]$). At the upper part of the figure, moreover, DFF1 and DFF2 configure a mono-stable circuit that sets $OSC_{2\text{-}Clk}$ to “1” upon the arrival of the rising edge at

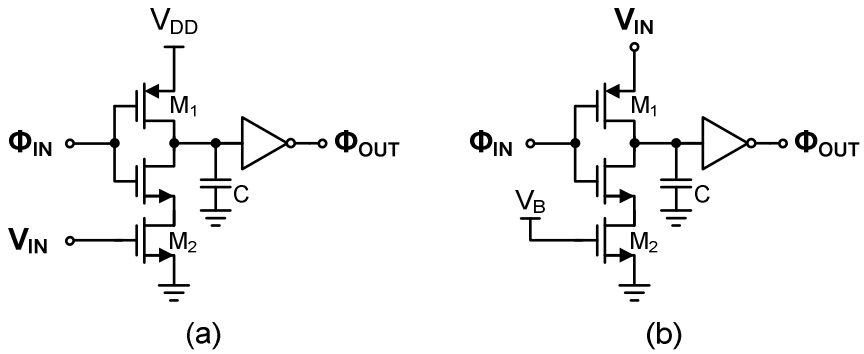


Fig. 5.9. The circuit configuration for (a) a typical VCDU, (b) the modified VCDU with improved linearity

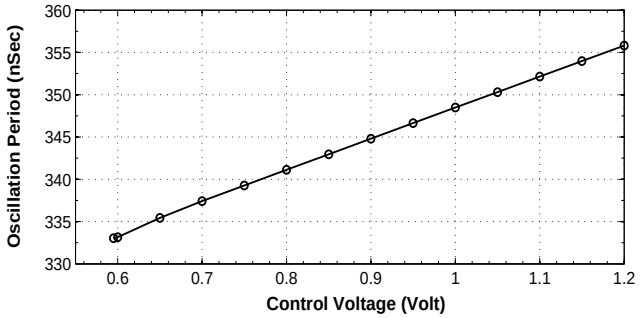
$\Phi_{OUT2,SIG}$. This mono-stable keeps the status of $OSC_{2\text{-}Clk}$ for a time equal to the delay of the buffer connected to the *R* input of DFF2. If the flag bit OSC_1 has been previously set to "1", by the arrival of the rising edge at $\Phi_{OUT2,SIG}$ and temporary setting of $OSC_{2\text{-}Clk}$, the rising edge at the clock input of DFF5 samples D_{TMP} signal to $D_{OUT\text{-}INT1}$ and $\overline{D_{OUT-INT1}}$. On the other hand, if OSC_1 is set to "1" after the temporary setting of $OSC_{2\text{-}Clk}$, the change at D_{TMP} will not be taken into account and the circuit waits for the next rising edge at $\Phi_{OUT2,SIG}$ to sample D_{TMP}. Digital bits $D_{OUT\text{-}INT1}$ and $\overline{D_{OUT-INT1}}$ will be used as the output feedback to the first integrator.

5.3.2. The Limited Input Range for Linear Operation of a VCDU

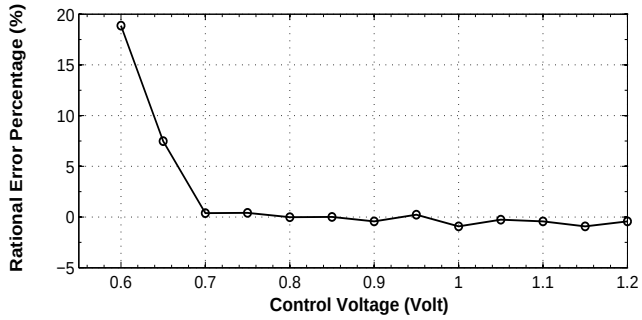
The main constraint to the linear operation of the first integrator is the limited input range of the VCDU block. As shown in Fig. 5.9.a for a typical VCDU, as explained in previous chapters, the input voltage is used to control the discharge current of the capacitor and to change the propagation delay of the block according to

$$T_{VCDU} = \frac{C}{I_D(V_{IN})}\left(V_{DD} - V_{Th,inv}\right). \tag{5.22}$$

Due to the quadratic relation between the gate-source voltage of a MOS transistor and its current, the linear range of operation for the VCDU is limited. As reported in [3], for a 1.8V power supply, the input range from 0.8V to 1.2V (i.e. 22% of the power supply) satisfies a linearity of ±0.1%. By modifying the circuit



(a)



(b)

Fig. 5.10. (a) The delay of the modified VCDU in terms of the input voltage, (b) the rational error percentage

as shown in Fig. 5.9.b, the linear range for the input signal dramatically increases. In the modified version, the input voltage is being sampled on capacitor C through transistor M_1. By fixing the bias voltage at V_B, the discharge current will be fixed at $I_D(V_B)$ and the delay of the block will be evaluated according to

$$T_{VCDU} = \frac{C}{I_D(V_B)}\left(V_{IN} - V_{Th,inv}\right). \tag{5.23}$$

It is evident that the delay of the modified block is linearly controlled by the input voltage V_{IN}. The experimental results for a prototype fabricated in 1.2V 0.13-um IBM CMOS technology is shown in Fig. 5.10.a. As shown in the figure, the linear range for the input signal is from 0.7V up to 1.2V for a 1.2V power supply (close to 42% of the power supply). As shown in Fig. 5.10.b, for input voltages smaller than 0.7V, the PMOS transistor does not operate as a perfect switch and the linearity degrades. For V_{IN} less than the threshold voltage of the output inverter (based on the experimental results $V_{Th,inv}=0.58V$), the VCDU does not pass the

input edge to its output and the propagation delay is not defined.

To develop a general diagram for a VCDU to be used in different applications, the above-mentioned modifications are applied to the SDU circuit that was proposed in Fig. 4.18. The concluded structure for the VCDU is shown in Fig. 5.11. The extra bypass switch is included to discharge the voltage across the capacitor instantly and reduce the propagation delay of the block where applicable. With this configuration, when a digital "1" is applied to V_{Bypass}, the propagation delay of the block will be as small as the cascade of two digital inverters. This circuit can be used for the implementation of both SDUs and VCDUs, as will be explained later.

5.3.3. Timing Characteristics of the Modulator

Due to asynchronous operation of the proposed TMDS modulator, there is no formulated timing between the outputs of the two integrators; however, the control unit guarantees an order to the output of each integrator. Specifically, it ensures the output of the second integrator follows that of the first integrator and the output of the first integrator follows that of the second integrator. Nonetheless, a system violation can occur if the average propagation delay of each integrator is unequal. Here we speak of the propagation delay of each integrator as the time difference between the arrival of the output TM signal and the corresponding

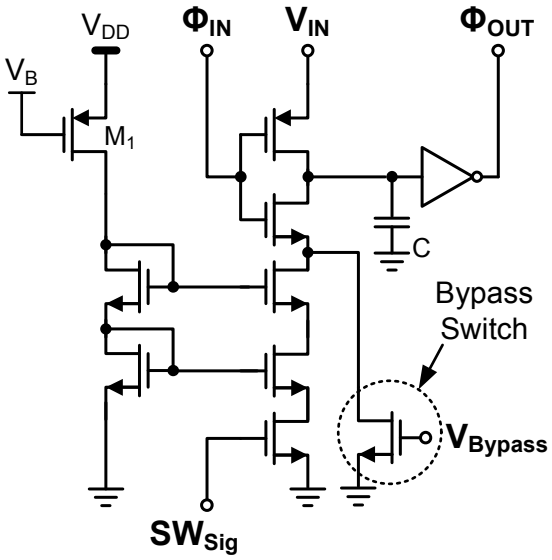


Fig. 5.11. The final circuit diagram used to implement a VCDU or SDU block

input TM signal. Of course, with a time-varying input, the propagation times will vary.

In the case of the first integrator, the instantaneous propagation delay T_{OSC1} is defined as the time difference between the time the input voltage is sampled and the time the next output edges occur. This is equal to the propagation time around the loop of a single ring oscillator, or equivalently, its oscillation period. This period can be described as

$$T_{OSC1}[n] = T_1 + G_{\phi} v_{IN}[n] - T_{FB1}[n-1], \tag{5.24}$$

where T_1 is a constant component and it is equal to the sum of the T_{VCDU} and T_{SDU} delays of all the VCDU and SDU blocks around the corresponding ring-oscillator. The term $G_{\phi}v_{IN}[n]$-$T_{FB1}[n-1]$ is the signal dependent component, where G_{ϕ} is the input voltage-to-phase conversion coefficient, and T_{FB1} is the time change caused by the feedback signal from the feedback provider logic.

In the case of the second integrator, the instantaneous propagation delay T_{OSC2} is defined as the time difference between the arrival of the input and output TM signals. Once again, this is equivalent to the oscillation period of one of the ring-oscillators that make up the second integrator. As explained in the previous chapter, after applying the reading signals to a TLatch, it can take up to $T_{TL,SDU}$ seconds before the stored data is readout and available at the output of the TLatch. The time $T_{TL,SDU}$ is the delay of the SDUs implemented inside each TLatch. Depending on the polarity of $\Delta T_{OUT1}[n-1]$ stored in each TLatch, the instantaneous period for the oscillating signals at the output of the second integrator can be described as

$$T_{OSC2}[n] = T_2 + \begin{pmatrix} T_{TL,SDU} - \left|\Delta T_{OUT1}[n-1]\right| \\ or \\ T_{TL,SDU} \end{pmatrix} - T_{FB2}[n-1], \tag{5.25}$$

where, again, T_2 is the constant component of the instantaneous period and it is equal to the sum of the T_{VCDU} and T_{SDU} delays of all the VCDU and SDU blocks around the corresponding ring-oscillator. Likewise, T_{FB2} is the time change caused by the feedback signal generated by the feedback provider logic.

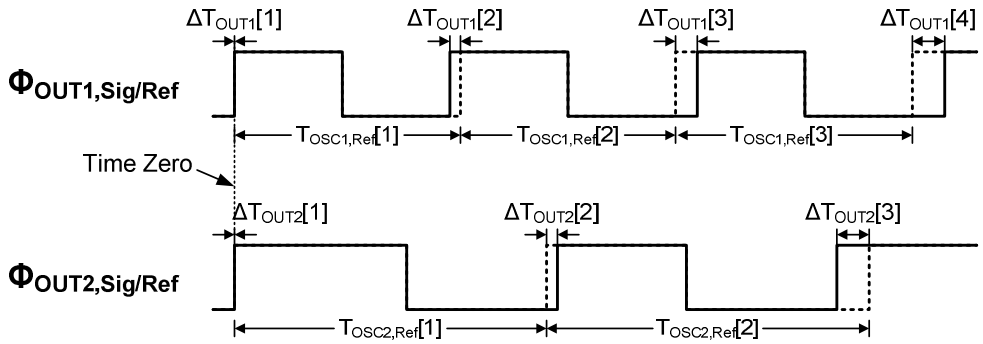


Fig. 5.12. Symbolic illustration of the timing for the output of each integrator

A symbolic representation of the signals at the output of each integrator is shown in Fig. 5.12. We assume that the very first rising edges at $\Phi_{OUT1,SIG/REF}$ and $\Phi_{OUT2,SIG/REF}$ as the outputs of the first and the second integrators, respectively, arrive at time zero. As explained in the previous chapter, after storing $\Delta T_{OUT1}[1]$ in TLatch_1, $\Delta T_{OUT1}[2]$ should be forwarded to TLatch_2. Following the same procedure, the next odd and even outputs of the first integrator should be latched on TLatch_1 and TLatch_2, respectively. To avoid any data storage conflict, the previous data saved on TLatch_1 (for example $\Delta T_{OUT1}[1]$) should have been read out before the next data for the same TLatch (for example $\Delta T_{OUT1}[3]$) arrives. So, during the time $\Delta T_{OUT1}[1]$ is latched and before any one of the rising edges related to $\Delta T_{OUT1}[3]$ occurs, at least one pair of rising edges at the output of the second integrator should have happened to initiate the readout of $\Delta T_{OUT1}[1]$.

To make sure $\Delta T_{OUT1}[1]$ is readout before $\Delta T_{OUT1}[3]$ arrives, the maximum instantaneous period of the first oscillation cycle of the second integrator, i.e. $T_{OSC2,REF}[1]$, should be $T_{TL,SDU}$ seconds shorter than the time for two oscillation cycles of the first integrator (as shown in Fig. 5.12). This is necessary to ensure that there is enough time for the readout of the stored information before $\Delta T_{OUT1}[3]$ arrives. This means

$$T_{OSC2,Ref}[1] \le T_{OSC1,Ref}[1] + T_{OSC1,Ref}[2] - T_{TL,SDU}\,. \tag{5.26}$$

Substituting Eqns. (5.24) and (5.25) in Eqn. (5.26), for the worst case results in

$$T_2 \le 2T_1 - 2T_{TL,SDU} + \left(G_\phi v_{in}[1] - T_{FB1}[0]\right) + \left(G_\phi v_{in}[2] - T_{FB1}[1]\right) + T_{FB2}[0]. \tag{5.27}$$

After storing $\Delta T_{OUT1}[3]$ in TLatch_1, $\Delta T_{OUT1}[4]$ should be forwarded to TLatch_2.

Again in order to avoid any conflict, $\Delta T_{OUT1}[2]$ previously stored on TLatch$_2$ should be read by a pair of rising edges at $\Phi_{OUT2,SIG/REF}$ before any one of the rising edges related to $\Delta T_{OUT1}[4]$ occurs. Subsequently, two cycles of the oscillating signals at $\Phi_{OUT2,REF}$ should finish $T_{TL,SDU}$ seconds before the third cycle of the oscillating signals at $\Phi_{OUT1,REF}$ is over, i.e.

$$T_{OSC2,Ref}[1]+T_{OSC2,Ref}[2]\le T_{OSC1,Ref}[1]+T_{OSC1,Ref}[2]+T_{OSC1,Ref}[3]-T_{TL,SDU}. \qquad (5.28)$$

Again, by substituting for the corresponding terms using Eqns. (5.24) and (5.25), the results will be

$$T_2 \le \frac{3}{2}T_1-\frac{3}{2}T_{TL,SDU}+\frac{1}{2}\sum_{k=1}^{3}\left(G_\phi v_{in}[k]-T_{FB1}[k-1]\right)+\frac{1}{2}\sum_{k=1}^{2}T_{FB2}[k-1]. \qquad (5.29)$$

Intuitively we can conclude that the upper limit for T_2 set by Eqn. (5.29) is smaller than the limit dictated by Eqn. (5.27). By following the same procedure and after n cycles, Eqn. (5.29) will change to

$$T_2 < \frac{n+1}{n}T_1-\frac{n+1}{n}T_{TL,SDU}+\frac{1}{n}\sum_{k=1}^{n+1}\left(G_\phi v_{in}[k]-T_{FB1}[k-1]\right)+\frac{1}{n}\sum_{k=1}^{n}T_{FB2}[k-1]. \qquad (5.30)$$

Since the delta-sigma modulation forces the output of the modulator to follow the input signal, it is expected that in the limit as n approaches infinity,

$$lim_{n\to\infty}\frac{1}{n}\sum_{k=1}^{n+1}\left(G_\phi v_{in}[k]-T_{FB1}[k]\right)=0. \qquad (5.31)$$

Also, to consider for the worst case, $T_{FB2}[k]$ values in Eqn. (5.30) should be considered all negative as

$$T_{FB2}[k]=-\left|T_{FB2}\right|. \qquad (5.32)$$

Adopting Eqns. (5.31) and (5.32) in Eqn. (5.30), the following relation should be satisfied by T_2 and T_1

$$T_2 < T_1-T_{TL,SDU}-\left|T_{FB2}\right| \qquad (5.33)$$

to guarantee no input data will be lost due to timing conflict between the input arrival and the readout of the TLatches. Simulation results will confirm the validity of this equation at the end of this Chapter.

5.3.4. Non-Uniform Sampling

As explained in section 5.3.2, upon the arrival of the rising edge at the input of the VCDU connected to the input voltage, the input continuous-time voltage V_{IN} will be sampled across the capacitor inside the VCDU. The sampled value will be used to modify the instantaneous oscillation period of the corresponding ring-oscillator in the first integrator. The next sampling of the input voltage happens after one oscillation cycle of the same ring-oscillator. By modifying the oscillation period according to the sampled input voltage and the output feedback, the oscillation (or sampling) period changes from cycle to cycle according to Eqn. (5.24). This phenomenon is referred to as non-uniform sampling and it results in harmonic distortion at the input of the modulator. This leads to spurious tones at the input of the modulator that will be transferred directly to the output. The complete and accurate analysis of non-uniform sampling is beyond the scope of this thesis and it can be studied more in [62]. Some authors have tried to address the effect of non-uniform sampling on the performance of VCO-based data converters using simplified methods [11, 17, 19]; however, the reported results do not seem comprehensive enough to be used as a general means for studying distortion in time-mode circuits. In this section, an experimental study of non-uniform sampling in VCO-based data converters based on the simulations performed in MATLAB/Simulink will be presented. This study starts by the investigation of the proposed TMDS modulator with a single-ended input and the simulation of the same modulator with a differential input will follow it.

5.3.4.1. Non-Uniform Sampling of the Single-Ended Input

For a typical synchronous delta-sigma modulator, the period of input sampling is constant and synchronized to a reference clock. Consider the input as a continuous-time signal being described as

$$v_{IN}(t) = A\sin(2\pi f_{IN} t) \tag{5.34}$$

where A and f_{IN} represent the amplitude and the frequency of the input sinusoid signal. Subsequently, the n-th sample of this input sampled through uniform

sampling is described as

$$v_{IN,Uniform}[n] = A\sin(2\pi f_{IN} nT_1). \tag{5.35}$$

where T_1 is the ideal sampling period.

For an asynchronous VCO-based data converter such as the second-order TMDS structure presented in this chapter, there is no reference clock. In the proposed TMDS modulator, the sample-and-hold operation is performed solely by the VCDU circuit connected to the input voltage. The instantaneous sampling period is generated by the signal oscillator circuit of the first integrator. As shown by Eqn. (5.24), this period is dependant on the sampled voltage as well as the feedback signal. The sequence of samples applied to the input of the TMDS modulator in a single-ended configuration can then be described as

$$v_{IN}[n] = A\sin\left\{2\pi f_{IN}\left(nT_1 + \sum_{k=1}^{n} G_\phi v_{IN}[k-1] - T_{FB1}[k-1]\right)\right\}. \tag{5.36}$$

This sequence deviates from a normal set of samples presented by Eqn. (5.35). As Eqn. (5.36) is difficult to handle by direct algebraic means, we shall study this equation more carefully using numerical methods. In the rest of this section, all the efforts are made to simplify Eqn. (5.36) in order to drive an experimental formula for the evaluation of the spurious-free dynamic range of the sequence of data sampled according to this equation. The extracted formula will be used as a measure of harmonic distortion introduced by non-uniform sampling. The MATLAB/Simulink simulations of the original mathematics will be used to verify the accuracy of the extracted formulas.

The established analysis method will be provided in three steps, whereby the modulation level of the sampling period changes in each one. The three steps are listed as:

(1) Sinusoidal phase modulated sampling process

(2) Accumulated phase-modulated sampling process

(3) Delta-Signal Modulated sampling process

Although the results extracted through the third step is applicable to the proposed TMDS modulator, the first two steps help to make the understanding of the overall analysis.

***Step 1: Sinusoidal phase modulated sampling process*:** we first consider a simplified version of Eqn. (5.36), written as

$$v_{IN}[n] = A\sin\left(2\pi f_{IN}\left\{nT_1 + G_\phi v_{IN}[n-1]\right\}\right). \tag{5.37}$$

Comparing the above expression to the one generated from an ideal sampling process captured by Eqn. (5.35), we see that in this situation the time between consecutive samples varies with the signal itself. Hence, the sampling process is non-uniform. Considering the series of samples specified by Eqn. (5.37) is a distorted version of the uniformly sampled sequence of data described by Eqn. (5.35), the resulting sequence when driven by a sinusoidal input signal can be formulated as a harmonic series described as follows:

$$v_{IN}[n] = A_1\sin\left(2\pi f_{IN} nT_1\right) + A_2\sin\left(4\pi f_{IN} nT_1\right) + A_3\sin\left(6\pi f_{IN} nT_1\right) + ... \tag{5.38}$$

Substituting Eqn. (5.38) into Eqn. (5.37) leads to

$$v_{IN}[n] = A\sin\left\{2\pi f_{IN}\left(nT_1 + G_\phi \times A_1\sin\left[2\pi f_{IN}(n-1)T_1\right] + \Delta T_{Harmonics}[n-1]\right)\right\}, \tag{5.39}$$

where

$$\Delta T_{Harmonics}[n] = G_\phi \times A_2\sin\left(4\pi f_{IN} nT_1\right) + G_\phi \times A_3\sin\left(6\pi f_{IN} nT_1\right) + ... \tag{5.40}$$

In practice, the harmonic term $\Delta T_{Harmonics}[n]$ is much smaller than the fundamental term, i.e., $G_\phi \times A_1 sin[2\pi f_{IN}(n-1)T_1]$. Hence, as a first-order approximation, $\Delta T_{Harmonics}[n-1]$ can be ignored and Eqn. (5.39) can be reduced to

$$v_{IN}[n] \approx A\sin\left(2\pi f_{IN}\left\{nT_1 + G_\phi \times A\sin\left[2\pi f_{IN} nT_1\right]\right\}\right). \tag{5.41}$$

Therefore, the sequence of the input sampled signal described by Eqn. (5.37) is equivalent to a set of samples derived by a sampling process whose clock edges have been phase modulated by a sinusoidal signal with the amplitude of $G_\phi \times A$. It is evident from this equation that during each cycle of the input signal, the non-uniform sampler samples the input signal at different sampling instants with a maximum sampling time offset of $G_\phi \times A$ from the ideal value (i.e. T_1).

As shown in Fig. 5.13, during the time between the ideal sampling at nT_1 and the actual non-uniform sampling at $nT_1 + \Delta T_{Sampling}$, the input signal changes so that the sampled values at these two times will be different. This change

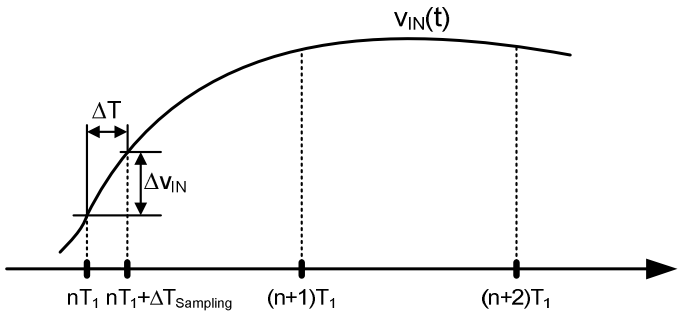


Fig. 5.13. Illustrating the change in the sample value due to variation in the sampling instant.

results in the harmonic distortion at the output of the non-uniform sampler characterized by Eqn. (5.37). We can consider amplitude of $\Delta v_{IN}/v_{IN}[nT_1]$ equal to

$$\frac{\Delta v_{IN}}{v_{IN}[nT_1]} \approx \frac{dv_{IN}}{dt}[nT_1] \times \frac{\Delta T_{Sampling}}{v_{IN}[nT_1]}, \tag{5.42}$$

and use it as a measure of distortion. So that, an increase in $\Delta v_{IN}/v_{IN}[nT_1]$ means the distortion level has increased. For a sinusoid input described by Eqn. (5.35), Eqn. (5.42) will change as following

$$\frac{\Delta v_{IN}}{v_{IN}[nT_1]} \approx 2\pi f_{IN} \times G_\phi \times A\cos(2\pi f_{IN} nT_1). \tag{5.43}$$

Based on Eqn. (5.42), it is expected that the harmonic distortion induced by the non-uniform sampler modeled by Eqn. (5.37) changes as $f_{IN} \times G_\phi \times A$ changes where $G_\phi \times A$ is $\Delta T_{Sampling,Max}$; also, it should be independent of the sampling period, i.e. T_1.

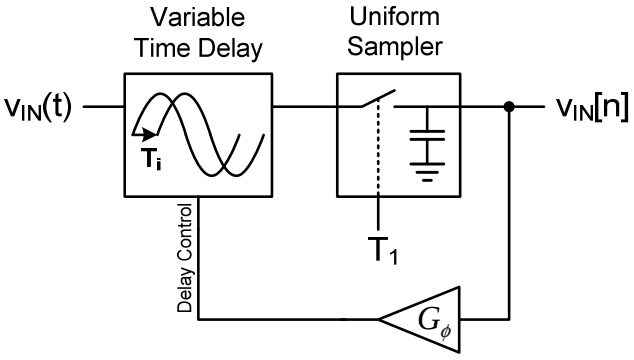


Fig. 5.14. The block diagram to model non-uniform sampling of Eqn. (5.37) in Simulink.

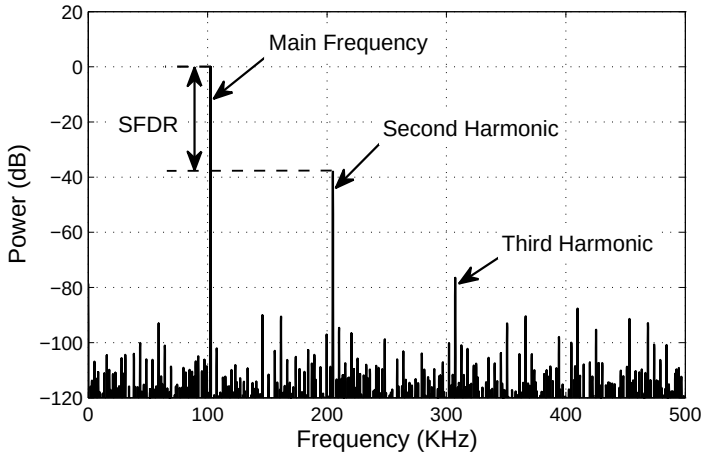


Fig. 5.15. Frequency spectrum at the output of the non-uniform sampler described by Eq. (5.37)

To verify the validity of the simplifications made to extract Eqn. (5.41), the original equation, i.e., Eqn. (5.37) was simulated in MATLAB/Simulink. To model the non-uniform sampling inherent in this equation, instead of phase modulating the sampling clock, the inverse phase shift was applied to the input signal using a "Variable Time Delay" block in Simulink. As shown in Fig. 5.14, the input voltage applied to a uniform sampler was delayed according to the previous sampled value of the input signal. Using this configuration, each input sample will be delayed with a different delay value. For T_1= 156.25 ns (6.4 MHz), $G_{ø}$×A= 40 ns, and f_{IN}=102.44 kHz, the frequency spectrum of the output of the sampler is shown in Fig. 5.15. As shown in this figure, the non-uniformly sampling introduces harmonics in the output spectrum. The strength ratio of the

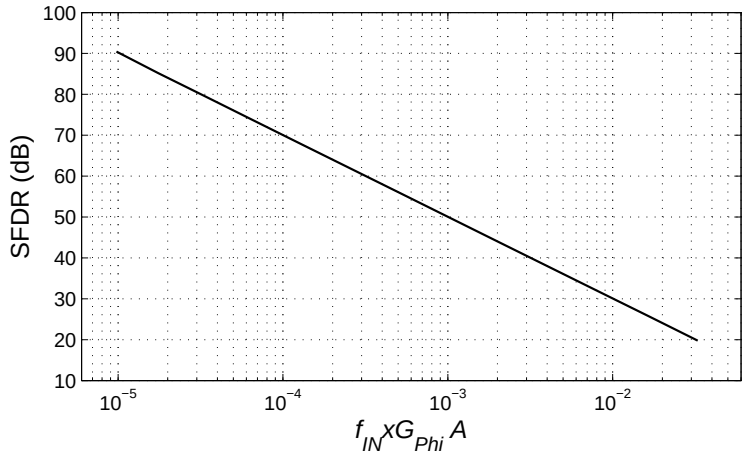


Fig. 5.16. Output SFDR of the non-uniform sampler of Eqn. (5.37) in terms of f_{IN}×$G_{ø}$×A

fundamental signal to the strongest spurious signal in the output spectrum (that in this case is the second harmonic) determines the maximum signal-to-noise ratio achievable from the non-uniformly sampler modeled by Eqn. (5.37). This ratio is also defined as Spurious-Free Dynamic Range (SFDR). As expected, by changing $f_{IN}\times G_{ø}\times A$ the output SDFR changes. As shown in Fig. 5.16, the SFDR changes with $f_{IN}\times G_{ø}\times A$ at a -20 dB/Dec rate. To see how the output SFDR changes in terms of T_1, f_{IN} and $G_{ø}\times A$ were fixed to 102.44 kHz and 40 ns respectively and T_1 was changed from 156.25 ns to 78.125 ns and 312.5 ns. The simulated results for the output SFDR does not show any noticeable difference and it confirms our initial assumption that the output SFDR is independent of T_1.

***Step 2: Accumulated phase-modulated sampling process*:** Now we investigate the output SFDR for a non-uniform sampler modeled by the following equation

$$v_{IN}[n]=A\sin\left(2\pi f_{IN}\left(nT_1+\sum_{k=1}^{n}G_{\phi}v_{IN}[k-1]\right)\right). \tag{5.44}$$

This equation is the modified version of Eqn. (5.36) where only the feedback term (T_{FB1}) is excluded. Following the same explanation mentioned for Eqn. (5.37), Eqn. (5.44) can be simplified by a first-order approximation as

$$v_{IN}[n]=A\sin\left(2\pi f_{IN}\left(nT_1+G_{\phi}\times A\times\sum_{k=1}^{n}\sin\left(2\pi f_{IN}\times(k-1)T_1\right)\right)\right). \tag{5.45}$$

By taking advantage of a large oversampling ratio, T_1 will be much smaller than $1/f_{IN}$. If we consider $T_1=dt$, the Σ term in Eqn. (5.45) can be approximated by an integral expression as following:

$$\sum_{k=1}^{n}\sin\left(2\pi f_{IN}(k-1)T_1\right)=\frac{1}{T_1}\sum_{h=0}^{n-1}\sin\left(2\pi f_{IN}hT_1\right)\times T_1\approx\frac{1}{T_1}\int_0^{(n-1)T_1}\sin\left(2\pi f_{IN}t\right)dt\,. \tag{5.46}$$

Solving the above integral results in

$$\frac{1}{T_1}\int_0^{(n-1)T_1}\sin\left(2\pi f_{IN}t\right)dt=\frac{1}{2\pi f_{IN}T_1}-\frac{1}{2\pi f_{IN}T_1}\cos\left\{2\pi f_{IN}(n-1)T_1\right\}. \tag{5.47}$$

By considering

$$-\cos x=\sin\left(\frac{3\pi}{2}+x\right), \tag{5.48}$$

Eqn. (5.47) can be modified and substituted in Eqn. (5.45), leading to the equation

$$v_{IN}[n] = A\sin\left(2\pi f_{IN}\left[nT_1 + \frac{G_\phi \times A}{2\pi T_1 \times f_{IN}}\sin\left(\frac{3\pi}{2} + 2\pi f_{IN}(n-1)T_1\right)\right] + \frac{G_\phi \times A}{T_1}\right). \quad (5.49)$$

The new equation includes a constant phase offset component equal to $G_{ø}\times A/T_1$. This phase offset and the phase offset associated with the *sin* term (i.e. $3\pi/2$) are independent of the sample index *n* and they do not influence the output SFDR. Ignoring the constant phase offsets, Eqn. (5.49) seems like a modified version of Eqn. (5.41); where, the deviation of the sampling period from its ideal value is equal to

$$\Delta T_{Sampling} = \frac{G_\phi \times A}{2\pi T_1 \times f_{IN}}\sin\left(\frac{3\pi}{2} + 2\pi f_{IN}(n-1)T_1\right). \quad (5.50)$$

Following the argument presented in Step 1, the relative error induced by non-uniform sampling can be extracted for the sampler modeled by Eqn. (5.49). It is easy to show that this error is proportional to

$$\frac{\Delta v_{IN}}{v_{IN}[nT_1]} \propto f_{IN} \times \Delta T_{Sampling,Max}. \quad (5.51)$$

As

$$\Delta T_{Sampling,Max} = \frac{G_\phi \times A}{2\pi T_1 \times f_{IN}}, \quad (5.52)$$

combining this equation with Eqn. (5.51) leads to

$$\frac{\Delta v_{IN}}{v_{IN}[nT_1]} \propto \frac{G_\phi \times A}{2\pi T_1}. \quad (5.53)$$

Consequently, for fixed values of $G_{ø}\times A$ and T_1, the amount of distortion (i.e. SFDR) at the output of the non-uniform sampler modeled by Eqn. (5.44) is expected to be independent of the input frequency f_{IN}.

To confirm the validity of the conclusions made in the previous paragraph, the system described by Eqn. (5.44) was simulated using MATLAB/Simulink. The model used in the first step was modified, as shown in Fig. 5.17, by including a discrete-time integrator before the variable time delay. The output SFDR were simulated and measured for fixed values of $G_{ø}\times A$= 40 ns and T_1=312.5 ns (3.2

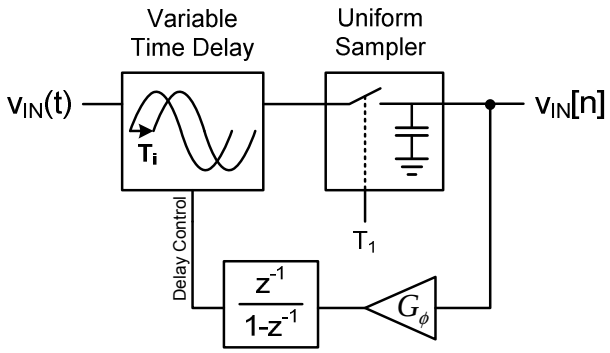


Fig. 5.17. The block diagram to model non-uniform sampling of Eqn. (5.44) in Simulink

MHz). The measured data in terms of the input frequency is shown in Fig. 5.18. It is evident that the output SFDR stays around 26 dB for input frequencies less than 300 kHz. As input frequency increases above 300 kHz, however, the output SFDR starts to fall off. This difference between the simulated model and the theoretical conclusions made in the above paragraph is a result of the decrease in the oversampling ratio; So that, Eqn. (5.45) cannot be substituted by an integral and the evaluated value for $f_{IN} \times \Delta T_{Sampling,Max}$ will not be a fixed constant anymore.

***Step 3: Delta-Signal Modulated sampling process*:** As the final step to analyze the non-uniform sampling at the input of the proposed TMDS modulator, we will now consider the whole expression seen in Eqn. (5.36). To simplify this equation, the Σ term included in this equation can be decomposed as following

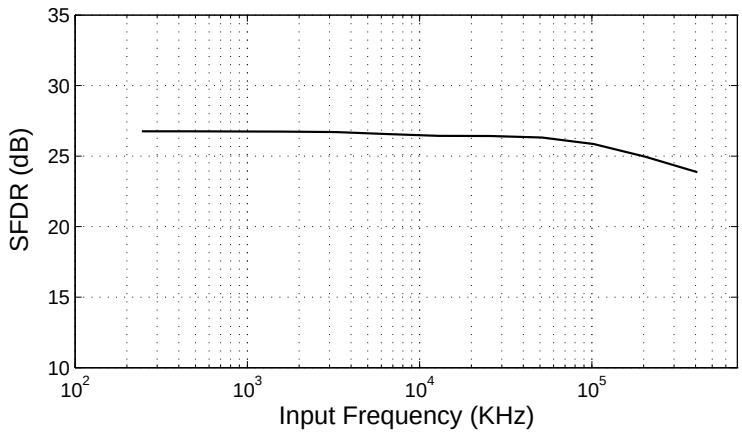


Fig. 5.18. Output SFDR of the sampler modeled by Eqn. (5.44) in terms of f_{IN}.

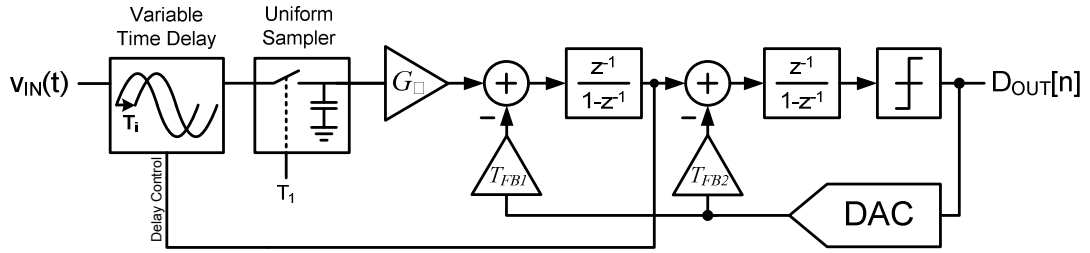


Fig. 5.19. The block diagram to model non-uniform sampling of Eqn. (5.36) in Simulink

$$\sum_{k=1}^{n} G_{\phi} v_{IN}[k-1] - T_{FB1}[k-1] = \sum_{k=1}^{n-1} \left(G_{\phi} v_{IN}[k-1] - T_{FB1}[k-1] \right) + G_{\phi} v_{IN}[n-1] - T_{FB1}[n-1] \quad (5.54)$$

Due to delta-sigma modulation, the average error between the feedback and the input signal is expected to approach zero as *n* increases, i.e.,

$$\lim_{n\to\infty} \sum_{k=1}^{n-1} G_{\phi} v_{IN}[k-1] - \sum_{k=1}^{n-1} T_{FB1}[k-1] \approx 0; \quad (5.55)$$

This, in turn, reduces Eqn. (5.36) to

$$v_{IN}[n] \approx A \sin\left\{ 2\pi f_{IN} \left(nT_1 + G_{\phi} v_{IN}[n-1] - T_{FB1}[n-1] \right) \right\}. \quad (5.56)$$

According to Eqn. (5.56), the maximum deviation of the sampling period for is equal to

$$\Delta T_{Sampling,Max} = Max\left(G_{\phi} v_{IN}[n-1] - T_{FB1}[n-1] \right) = G_{\phi} A + \left| T_{FB1} \right| \quad (5.57)$$

where $\left| T_{FB1} \right|$ can be treated as a constant. Thus, the maximum deviation of the sampling period increases as input amplitude increases. This behavior is similar to the sampler modeled in Step 1 above.

$$\frac{\Delta v_{IN}}{v_{IN}[nT_1]}\Big|_{Max} \propto f_{IN} \times G_{\phi} \times A \,. \quad (5.58)$$

Following the same explanations presented in Step 1, it can be concluded that the SFDR of the distortion made by the sampler in the proposed TMDS modulator should be dependent on $f_{IN} \times G_{\phi} \times A$ and it is expected to be independent of the ideal sampling period, i.e. T_1.

To verify the validity of the conclusions made in the previous paragraph, the behavior of the sampler modeled by Eqn. (5.36) was precisely simulated

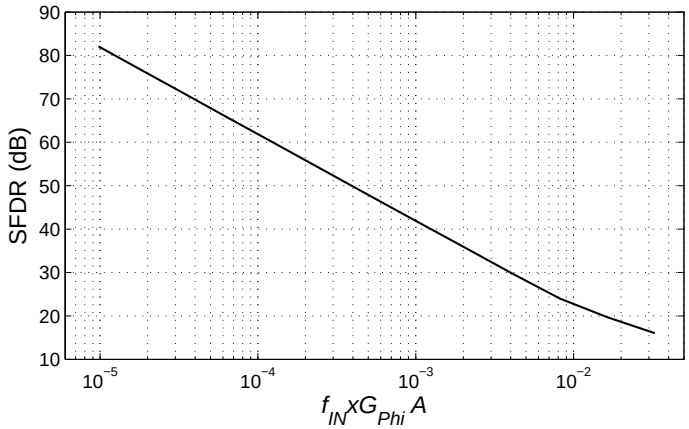


Fig. 5.20. Output SFDR of the sampler modeled by Eqn. (5.36) in terms of $f_{IN}\times G_{ø}\times A$

using MATLAB/Simulink. As shown in Fig. 5.19, the control input to the variable time delay block preceding the uniform sampler in the Simulink model is controlled by the error signal of a second-order delta-sigma modulator. The output SFDR were monitored and measured for $G_{ø}\times A$= 40 ns, T_1= 312.5 ns (3.2 MHz) and variable values of the input frequency. The results are illustrated in Fig. 5.20. Contrary to a non-feedback system (Fig. 5.18), the SFDR at the input of the TMDS modulator increases at a 20 dB/dec rate as the input frequency decreases (for a fixed value of $G_{ø}\times A$). As the input frequency increases, however, the change in the output SFDR deviates from a straight line. This deviation is due to the decrease of the oversampling ratio. As OSR decreases, the noise shaping performed through the modulator will be attenuated. This, in turn, increases the error between the input and output of the modulator and the assumption made by Eqn. (5.55) will not be valid anymore.

Based on these simulations, the SFDR at the input of the modulator is independent of the ideal sampling period, T_1, as well as the amplitude of the feedback signal (T_{FB1}); however, the decrease or increase of $G_{ø}\times A$ results in increase or decrease of the SFDR, respectively. For a fixed value of f_{IN}, the input SFDR increases at a 20 dB/dec rate as $G_{ø}\times A$ decreases. These results match the conclusions drawn for the very first sampler that was modeled by Eqn. (5.37). As it was confirmed by the simulation of Eqn. (5.36), it can be concluded that the SFDR at the input of the proposed TMDS modulator in a single-ended configuration can be formulated as

$$SFDR_{INPUT} \approx 20\log\left(\frac{\alpha}{\Delta v_{IN}/v_{IN}[nT_1]}\right) \approx 20\log_{10}\left(\frac{K}{f_{IN}\times G_{\phi}\times A}\right), \qquad (5.59)$$

where K represents an proportionality constant. Based on the data collected during simulation, K is equal to 0.1239 in this case.

Eqn. (5.59) predicts the harmonic distortion induced by the non-uniform sampling at the single-ended input of the proposed TMDS modulator. As it is evident, the output SFDR is independent of the sampling period (T_1) provided the OSR is high. In addition, by decreasing the input frequency or the voltage-to-phase conversion coefficient of the input voltage-to-delay converter the distortion decreases as well.

During the characterization of the TMDS modulator, the effect of non-uniform sampling should be considered carefully. If higher SNDR is desired, the utilization of a separate sample & hold at the input to the modulator is essential.

5.3.4.2. Non-Uniform Sampling of the Differential Input

The proposed TMDS modulator can be configured for a differential-input. In this mode, differential analog voltages $v_{IN,Sig}$ and $v_{IN,Ref}$ should be applied to the signal and the reference oscillators of the first integrator, so that for a sinusoid input

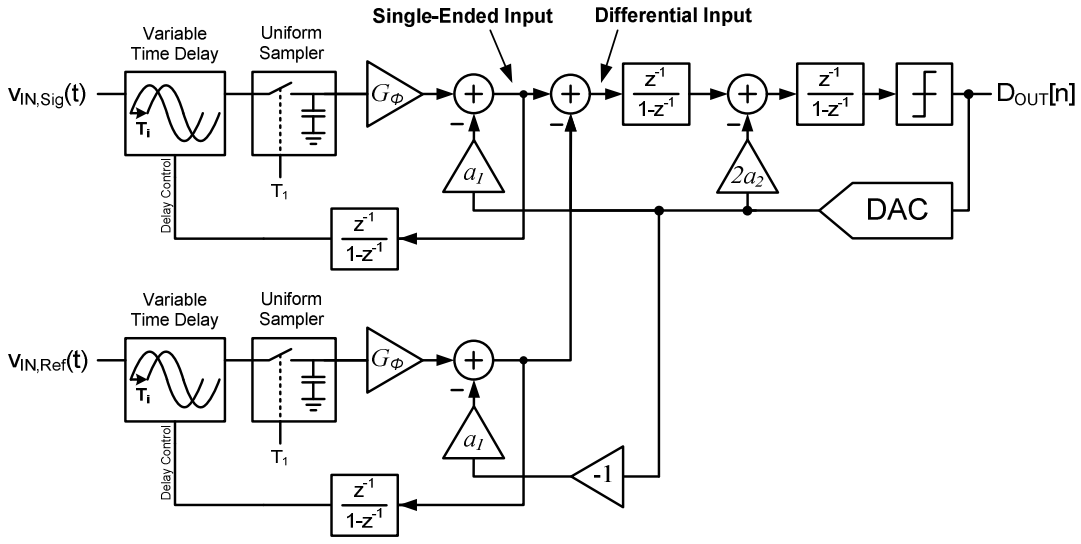


Fig. 5.21. The block diagram to model non-uniform sampling at the input of the proposed TMDS modulator and in a differential-input configuration

$$v_{IN,Sig}(t) = -v_{IN,\mathrm{Ref}}(t) = A\sin(2\pi f_{IN} t). \tag{5.60}$$

By modifying the instantaneous period of both oscillators, Eqn. (5.36) can be used to evaluate the sampled sequence of each input as

$$v_{IN,Sig}[n] = A\sin\left(2\pi f_{IN}\left(nT_1 + \Delta T_{Sampling}[n]\right)\right) \tag{5.61}$$

and

$$v_{IN,Ref}[n] = -A\sin\left(2\pi f_{IN}\left(nT_1 - \Delta T_{Sampling}[n]\right)\right), \tag{5.62}$$

where

$$\Delta T_{Sampling}[n] = \sum_{k=1}^{n} G_{\phi} v_{IN}[k-1] - T_{FB1}[k-1] \ , \tag{5.63}$$

and $v_{in}[k]=A\times sin(2\pi f_{IN} kT_1)$. Considering these equations, the output of the first integrator should be formulated as following

$$\Delta T_{OUT1}[n] = \Delta T_{OUT1}[n-1] + G_{\phi}\left(v_{IN,Sig}[n-1] - v_{IN,Ref}[n-1]\right) - 2T_{FB1}[n-1]. \tag{5.64}$$

It is evident that the effective differential input of the modulator is equal to

$$v_{IN,Diff}[n] = v_{IN,Sig}[n] - v_{IN,Ref}[n]. \tag{5.65}$$

As explained earlier, for a delta-sigma modulator $\Delta T_{Sampling}$ that is modeled by Eqn. (5.63) can be considered very small; so that,

$$v_{IN,Sig}[n] \approx v_{IN}(nT_1) + \left.\frac{dv_{IN}(t)}{dt}\right|_{t=nT_1} \times \Delta T_{Sampling}[n]. \tag{5.66}$$

A similar approximation can be made to Eqn. (5.62), so that Eqn. (5.65) might be written as

$$v_{IN,Diff}[n] \approx 2v_{IN}(nT_1). \tag{5.67}$$

Clearly, in an ideal situation, the harmonic distortion caused by non-uniform sampling might be canceled in the differential configuration; however, as the derivative of input signal approaches zero (at the positive and the negative peaks), Eqn. (5.66) will be violated. Also, the assumption that $\Delta T_{Sampling}$ is small is subject to approximation error. Consequently, the harmonic induced by the non-uniform sampling cannot be canceled completely. However, as it is expected

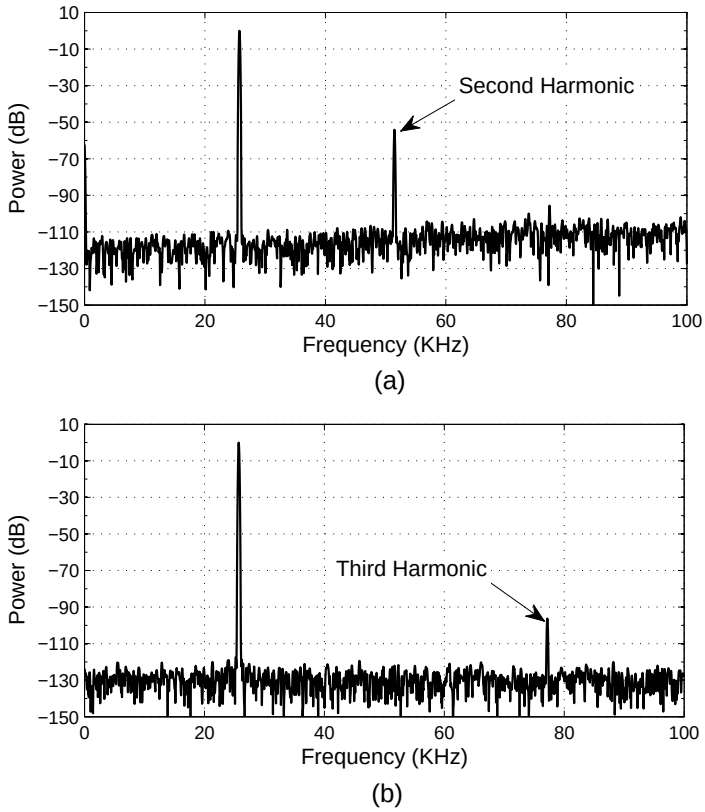


Fig. 5.22. The output SFDR of the sampler at the input of the proposed TMDS modulator for (a) a single-ended input, (b) a differential-ended input

from a differential structure, even-order harmonic distortion will be suppressed.

To simulate the differential non-uniform input sampler in Simulink, the differential model shown in Fig. 5.21 was used. The simulated spectrum for the output signal of the sampler (input to the modulator) for two cases of single-ended and differential modes are shown in Fig. 5.22. In Fig. 5.22.a, the PSD for the output of just one sampler as a single-ended input is shown. This spectrum consists of both even and odd harmonics that are induced due to non-uniform sampling, as explained in the previous sections. In Fig. 5.22.b. that corresponds to the spectrum of the differential voltage at the output of the two samplers, the even harmonics are removed while the strength ratio between the fundamental frequency and its third harmonic does not change. This ratio will be defined as the new SFDR measure and it is about 42 dB higher than the input SFDR of the single-ended modulator formulated by Eqn. (5.59). This improvement comes at

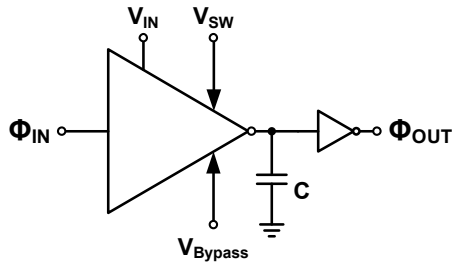


Fig. 5.23. The symbol for the controlled delay block either as a VCDU or as a SDU

the price of perfect matching between the two ring-oscillators of the first integrator.

At the presence of mismatches, however, a percentage of the second harmonic will be forwarded to the output of the modulator that will degrade the output SFDR. However, the output SFDR for a differential input will be larger even if mismatches exist, as the even harmonics will be attenuated.

5.4. Design Procedure for a 2nd-Order ΔΣ Modulator

In the previous sections, the equations and system level considerations for the design and characterization of the proposed second-order TMDS modulator were extracted. In this section, a practical procedure to design the modulator will be developed. This procedure is derived based on the formulas and conditions described in the previous sections. As the modulator consists of two integrator stages in cascade, each integrator is constructed with identical delay blocks with different sized capacitors, as dictated by the design constraints.

5.4.1. The Common Topology for VCDUs and SDUs

Each one of the integrators in the proposed second-order TMDS modulator is composed of two ring-oscillators. VCDU and SDU blocks are used to set the timing characteristics of the oscillating signals at the output of each oscillator. The delay block presented in Fig. 5.11 can be used either as a VCDU or as a SDU block depending on which bias voltage is being used as the control voltage. According to Eqn. (5.23), the delay of this block can be controlled either by the modification of the discharge current or by the modification of the pre-charged voltage across the capacitor or by changing the capacitor inside the

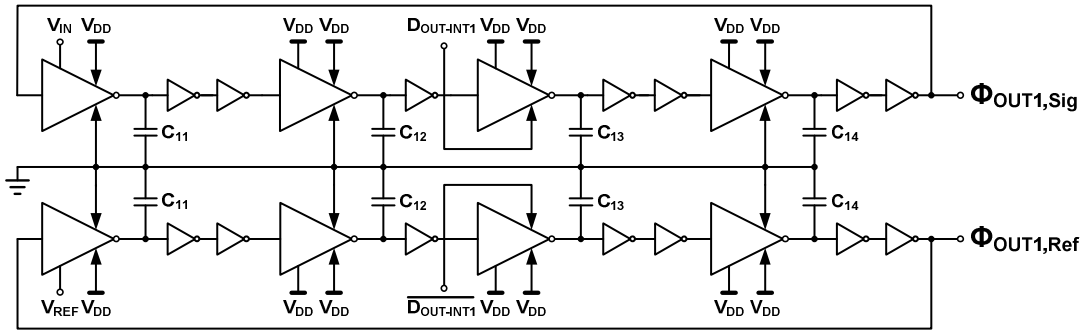


Fig. 5.24. The circuit diagram for the ring-oscillators included in the first integrator

block. To develop a simplified method for the design of the TMDS modulator, we illustrate this block with the symbol shown in Fig. 5.23. Here the capacitor is shown separate from the delay block, as this component will be used to establish different propagation delays using the same transistor cell. The voltage V_B used to bias the transistor that controls the discharge current is considered as an internal variable and it will not be used as a means of control.

For each VCDU, inputs V_{SW} and V_{Bypass} should be connected to V_{DD} and *Gnd*, respectively. The delay of the block in this configuration is given by

$$T_{VCDU} = f(V_B) \times C(V_{IN} - V_{Th}), \tag{5.68}$$

where $f(V_B)$ is the reciprocal discharge current as a function of V_B and V_{IN} is the input voltage. A form of this expression was first seen in Section 3.1. By connecting V_{IN} to V_{DD}, however, the block can be used in a SDU configuration with a delay equal to

$$T_{SDU} = g(V_B)C, \tag{5.69}$$

where

$$g(V_B) = f(V_B)(V_{DD} - V_{Th}). \tag{5.70}$$

In a SDU configuration, connecting V_{SW} to *Gnd* enhances the delay of the block as explained in Chapter 3. In addition, by connecting V_{Bypass} to V_{DD}, the total delay of the block will be bypassed and shortened to the delay of a single digital buffer.

In the rest of this section, an identical delay block topology with fixed $f(V_B)$ and $g(V_B)$ values will be used to implement the ring-oscillators included in each

integrator. Considering fixed values for $f(V_B)$ and $g(V_B)$, the design will be mostly concentrated on the value specification of the control capacitors connected to each delay block.

5.4.2. Characterization of the Integrators

In Fig. 5.24, the circuit diagram for the two ring-oscillators included in the first integrator is illustrated. The circuit is composed of some inverters alongside a number of delay blocks with the symbol shown in Fig. 5.23. Based on the signal configuration applied to each delay block, it is evident that the delay block connected to C_{11} is a VCDU where the other delay blocks are arranged as SDUs.

As explained in the previous chapter, the TM output of the first integrator is equal to the previous output plus the difference between the instantaneous periods of the signals at $\Phi_{OUT1,SIG}$ and $\Phi_{OUT1,REF}$, i.e.

$$\Delta T_{OUT1}[n] = \Delta T_{OUT1}[n-1] + T_{OUT1,SIG}[n] - T_{OUT1,REF}[n], \tag{5.71}$$

where $\Phi_{OUT1,SIG}$ and $\Phi_{OUT1,REF}$ are the outputs of the two ring-oscillators in Fig. 5.24. To proceed with the design flow, we consider the period of each signal composed of two terms as

$$T_{OUT1,SIG} = T_{OUT1,SIG-High} + T_{OUT1,SIG-Low}, \tag{5.72}$$

where $T_{OUT1,SIG\text{-}High}$ and $T_{OUT1,SIG\text{-}Low}$ represent the propagation delay of the rising and falling edges around the loop, respectively. In other words, $T_{OUT1,SIG\text{-}High}$ and $T_{OUT1,SIG\text{-}Low}$ represents the width of the High and Low level of the oscillating signal at $\Phi_{OUT1,SIG}$. For the configuration shown in Fig. 5.24,

$$T_{OUT1,SIG-High} = f(V_B)(V_{IN} - V_{Th,inv})C_{11} + g(V_B)C_{14} + 9\tau_{inv}, \tag{5.73}$$

where τ_{inv} is the propagation delay of a digital inverter. Likewise, the pulse width for the low-level signal at $\Phi_{OUT1,SIG}$ is equal to

$$T_{OUT1,SIG-Low} = g(V_B)C_{12} + (1 - D_{OUT-INT1})g(V_B)C_{13} + 9\tau_{inv}. \tag{5.74}$$

$D_{OUT\text{-}INT1}$ is the digital output of the modulator applied as the feedback to the first integrator. By ignoring the delay of the inverters as some minor components, the period of the oscillating signals according to Eqn. (5.72) can be approximated by

$$T_{OUT1,SIG} = f(V_B)(V_{IN} - V_{Th,inv})C_{11} + g(V_B)C_{12} + (1 - D_{OUT-INT1})g(V_B)C_{13} + g(V_B)C_{14}. \tag{5.75}$$

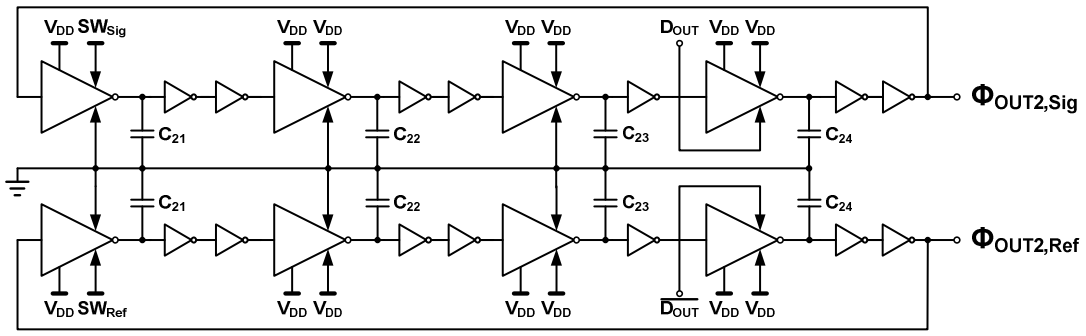


Fig. 5.25. The circuit diagram for the ring-oscillators included in the second integrator

This equation is composed of a signal independent term equal to

$$T_1 = f(V_B)(V_{REF} - V_{Th,inv})C_{11} + g(V_B)C_{12} + g(V_B)C_{14}, \tag{5.76}$$

a feedback term equal to

$$T_{FB1} = g(V_B)C_{13}, \tag{5.77}$$

and a signal component equal to

$$T_{v_{in}} = f(V_B)(V_{IN} - V_{REF})C_{11}. \tag{5.78}$$

As explained in Chapter 3, the maximum limit for $\Delta T_{OUT1}[n]$ is the maximum TM value that can be stored by a TLatch to be integrated into the second integrator output. We use the same SDU architecture as shown in Fig. 5.23 with a control capacitor of C_{TL} to develop the TLatch. So according to Eqn. (5.69), the $T_{TL,SDU}$ delay of the TLatch that is also the maximum limit for the output of the first integrator will be equal to

$$T_{TL,SDU} = g(V_B)C_{TL}. \tag{5.79}$$

With some minor modifications to the ring-oscillators of Fig. 5.24, the second integrator can be implemented as shown in Fig. 5.25. It is evident in the figure that the V_{SW} input of just one of the SDUs in each ring-oscillator is used to implement the time-to-time integration as explained in the previous chapter. The rest of delay blocks are utilized to set the duty cycle of the oscillating signal. Ignoring minor gate delays (τ_{inv}) in each loop, the pulse widths of the high-level and low-level output signal at $\Phi_{OUT2,SIG}$ can be evaluated as

$$T_{OUT2,SIG-High} = g(V_B)C_{21} + \Delta SW_{Sig} + g(V_B)C_{23} + (1 - D_{OUT})g(V_B)C_{24} \tag{5.80}$$

and

$$T_{OUT2,SIG-Low} = g(V_B)C_{22} \tag{5.81}$$

respectively, where D_{OUT} is the digital output of the modulator applied as the feedback to the second integrator. Consequently, the oscillation period for the oscillators of the second integrator is equal to

$$\begin{aligned} T_{OUT2,SIG} &= T_{OUT2,SIG-High} + T_{OUT2,SIG-Low} \\ &= g(V_B)C_{21} + \Delta SW_{Sig} + g(V_B)C_{23} + (1-D_{OUT})g(V_B)C_{24} + g(V_B)C_{22} \end{aligned}. \tag{5.82}$$

This equation consists of a constant term equal to

$$T_2 = g(V_B)C_{21} + g(V_B)C_{22} + g(V_B)C_{23} \tag{5.83}$$

and a feedback term equal to

$$T_{FB2} = g(V_B)C_{24}. \tag{5.84}$$

As explained earlier, the second integrator is the time-to-time integrator developed in the previous chapter. To guarantee the one-to-one correspondence between the inputs and outputs of this integrator, a self-correction algorithm was implemented through its digital control unit to tune the average time interval between each two successive samples at the output of the integrator to that of its input samples. To make the algorithm work, the following condition must be met:

$$T_1\big|_{V_{IN}=V_{IN,Min}=V_{Th,inv}} \geq 2T_2. \tag{5.85}$$

Substituting Eqns. (5.76) and (5.83) in Eqn. (5.85) results in

$$g(V_B)C_{12} + g(V_B)C_{14} > 2\times[g(V_B)C_{21} + g(V_B)C_{22} + g(V_B)C_{23}]. \tag{5.86}$$

To find a more manageable formula, we stick to our first assumption that all VCDUs and SDUs has the same transistor dimensions and V_B bias voltage that results in identical values for the $g(V_B)$ of all the delay blocks. Hence, Eqn. (5.86) can be simplified to the following

$$C_{12} + C_{14} \geq 2\times(C_{21} + C_{22} + C_{23}). \tag{5.87}$$

After evaluating the signals at the output of the second integrator, the rising edges at $\Phi_{OUT2,SIG}$ and $\Phi_{OUT2,REF}$ are directly applied to the *D* and *Clk* inputs of the output single-bit quantizer (DFF). To avoid any error, the maximum

value for the absolute phase difference between the two ring-oscillators should be equal to the minimum of $T_{OUT2,SIG\text{-}High}$ and $T_{OUT2,SIG\text{-}Low}$. Otherwise, the rising edge at the *Clk* input may sample a value of the signal at the *D* input, which belongs to the next or previous cycle of the oscillating signal at $\Phi_{OUT2,SIG}$.

Finally, as explained earlier, to avoid any loss of input information due to overwriting, the timing of the oscillating signals at the output of each integrator should satisfy Eqn. (5.33). By substituting Eqns. (5.76), (5.79), (5.83), and (5.84) in Eqn. (5.33), a new condition will be established as

$$g(V_B)C_{21}+g(V_B)C_{22}+g(V_B)C_{23}<f(V_B)(V_{REF}-V_{Th,inv})C_{11}+g(V_B)C_{12}+g(V_B)C_{14}-g(V_B)C_{TL}-g(V_B)C_{24} \quad (5.88)$$

that is a function of the capacitors used in each integrator block. Considering an identical value for the $f(V_B)$ and $g(V_B)$ of all the delay blocks, Eqn. (5.88) can be simplified to

$$C_{21}+C_{22}+C_{23}+C_{24}<\frac{V_{REF}-V_{Th,inv}}{V_{DD}-V_{Th,inv}}C_{11}+C_{12}+C_{14}-C_{TL}\,. \quad (5.89)$$

Eqn. (5.89) together with Eqn. (5.87) will be used to develop a simplified method for the design of the TMDS modulator that was initially introduced by the differential equations in Section 5.2.

5.4.3. Design Rules

Considering the block diagram of the Boser-Wooley modulator shown in Fig. 5.5.a together with the developed equations in section 5.4.2, Fig. 5.26.a illustrates the block diagram of the second-order TMDS modulator. The feedback coefficients and the input voltage-to-phase conversion coefficient are assigned by considering Eqns. (5.77), (5.84), and (5.78), respectively.

By using an identical set of transistor dimensions to implement the CMOS part of all the delay blocks (VCDUs and SDUs) included in the modulator, $g(V_B)$ can be considered as a fixed constant throughout the design. Consequently, the design of the TM modulator will be mostly dedicated to the value assigned to the capacitors connected to each delay unit. As shown in Fig. 5.26.b, by splitting a unity coefficient right before the output quantizer, two gain components, $g(V_B)$ and $1/\,g(V_B)$, will be added to the block diagram. The term $g(V_B)$ can be moved

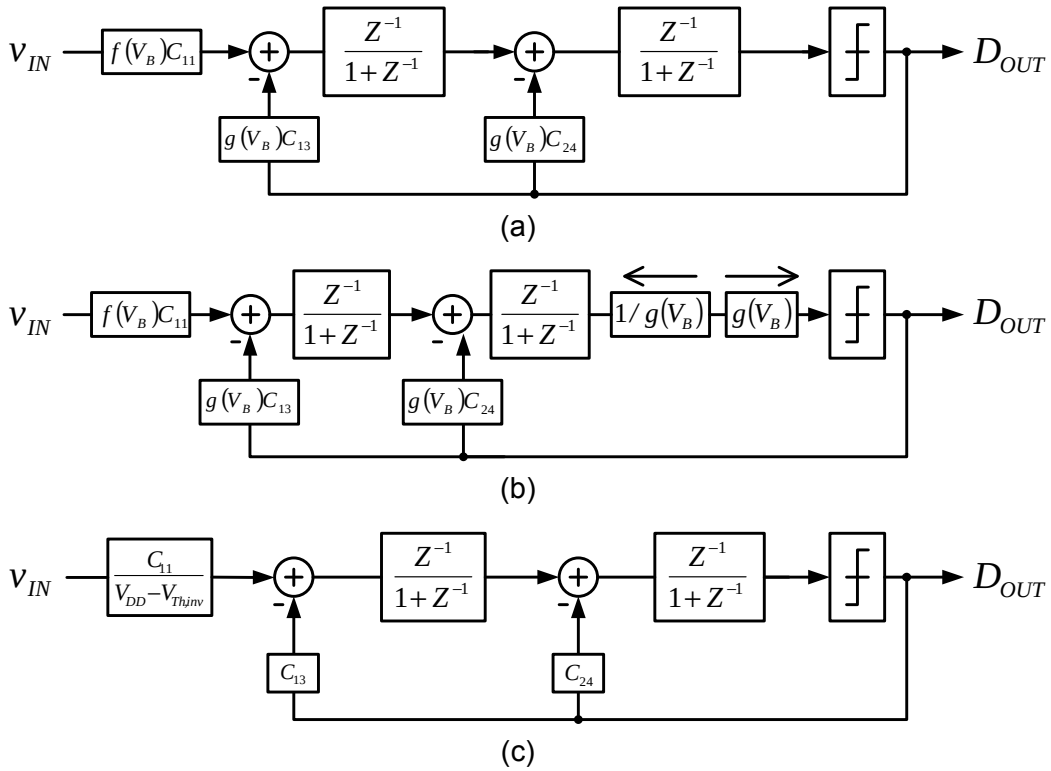


Fig. 5.26. (a) The block diagram of the proposed TMDS modulator, (b) The split of a unity gain, (c) The block diagram with normalized coefficients

into the output quantizer as a pre-amplifier. However, by moving *1/ g*(V_B) back to the input of the modulator, the coefficients of the block diagram will be modified as shown in Fig. 5.26.c. It should be noted that after dividing all the coefficients by *g*(V_B), all the signals across the modulator will be normalized to *g*(V_B) as well. After this normalization, the signals of the modulator shown in Fig. 5.26.c will be of capacitance type and fF will be used as the measurement unit.

The second-order operation of the concluded diagram is governed by three rules as following:

Rule 1: To achieve the desired second-order modulation, the coefficients of the Boser-Wooley modulator in Fig. 5.5.a were optimized through simulations to be $a_2=2.5a_1$. Assuming the same ratio between the corresponding coefficients of the modulator in Fig. 5.26.c results in

$$C_{24} = 2.5C_{13} \tag{5.90}$$

Rule 2: Considering the maximum output of the first integrator (i.e., $\Delta T_{OUT1,Max}$)

should be less than $T_{TL,SDU}$, $T_{OUT1,SIG-HIgh}$, and $T_{OUT1,SIG-Low}$, the upper limit for the normalized output of the first integrator in Fig. 5.26.c is

$$\left|\frac{\Delta T_{OUT1,Max}}{g(V_B)}\right| < min\left\{\frac{T_{OUT1,SIG-High}}{g(V_B)}, \frac{min\left(T_{OUT1,SIG-Low}\right)}{g(V_B)}, \frac{T_{TL,SDU}}{g(V_B)}\right\}. \tag{5.91}$$

Substituting Eqns. (5.73), (5.74), and (5.79) in Eqn. (5.91) results in

$$\left|\frac{\Delta T_{OUT1,Max}}{g(V_B)}\right| < min\left\{\frac{V_{REF}-V_{Th,inv}}{V_{DD}-V_{Th,inv}}C_{11}+C_{14}, C_{12}, C_{TL}\right\}. \tag{5.92}$$

Likewise, the upper limit for the normalized output of the second integrator in Fig. 5.26.c can be considered as

$$\left|\frac{\Delta T_{OUT2,Max}}{g(V_B)}\right| < min\left\{\frac{T_{OUT2,SIG-High}}{g(V_B)}, \frac{min\left(T_{OUT2,SIG-Low}\right)}{g(V_B)}\right\}. \tag{5.93}$$

Adopting Eqns. (5.80) and (5.81), this equation will be simplified as

$$\left|\frac{\Delta T_{OUT2,Max}}{g(V_B)}\right| < min\{C_{21}+C_{23}, C_{22}\}. \tag{5.94}$$

Rule 3: As expected from a delta-sigma modulator, the input signal should be smaller than the feedback amplitude; so that, the feedback can change the polarity of the signal at the input of the integrator. This condition results in

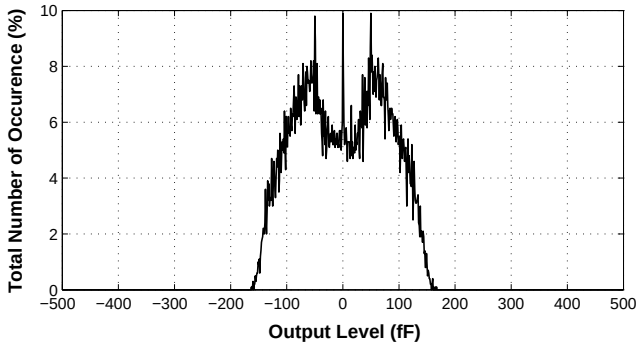
$$v_{IN} < (V_{DD}-V_{Th})\frac{C_{13}}{C_{11}} \tag{5.95}$$

as the upper limit for the input voltage.

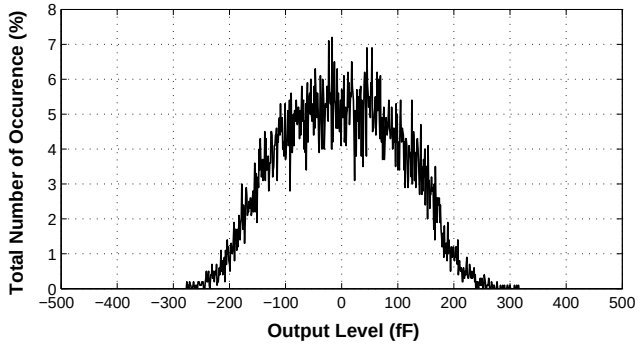
These three rules together with Eqns. (5.87) and (5.89) can be used to develop a capacitor selection algorithm. The objective of this algorithm is to find a series of capacitors that satisfy the above-mentioned rules and conditions. To explain the design procedure, a sample set of capacitors will be extracted in the next subsection.

5.4.4. Design algorithm for a sample 2nd order TMDS modulator

As the first step, we start with ***Rule 1*** by assigning a practical value to the capacitors C_{13} and C_{24} as $C_{24}=2.5C_{13}$=125 fF. To proceed with the design, we consider $C_{11}=C_{13}$=50 fF; however, the value for C_{11} can be modified later to tune



(a)



(b)

Fig. 5.27. The signal distribution at the out of (a) the first and (b) the second integrator

for different ranges of the input voltage. The block diagram shown in Fig. 5.26.c is simulated at the desired f_{IN} and f_s ($1/T_1$). During simulations, the input amplitude is set at the value that results in the maximum output SNR. The output of the first and the second integrator are investigated to find the range for the signal variation. As explained earlier, the time-mode signals of the simulated modulator are of capacitance type and fF will be used as the measurement unit.

As shown in Fig. 5.27.a, the simulated signal amplitude at the output of the first integrator changes from -170 fF up to +170 fF. Thus, according to ***Rule 2,*** it can be written

$$min\left\{\frac{v_{IN}}{V_{DD}-V_{Th}}C_{11}+C_{14},C_{12},C_{TL}\right\}>170\,fF \tag{5.96}$$

Also, as shown in Fig. 5.27.b, the range of the signal at the output of the second integrator is from -280 fF up to +310 fF which results in

$$min\{C_{21}+C_{23},C_{22}\}>310\,fF\,. \tag{5.97}$$

Any set of capacitors that satisfy Eqns. (5.96), (5.97), and (5.89) will be a potential answer. However, we can assume more applicable conditions to have a more controlled design flow. For example, by assuming equal low-to-high and high-to-low pulse widths,

$$T_{OUT,SIG-Low}=T_{OUT,SIG-High}\,, \tag{5.98}$$

for the oscillating signals at the output of each oscillator, a more limited set of capacitors will be achieved. Eqn. (5.98) for the first integrator results in

$$\frac{v_{IN}}{V_{DD}-V_{Th}}C_{11}+C_{14}=C_{12} \tag{5.99}$$

and alternatively for the second integrator

$$C_{21}+C_{23}=C_{22} \tag{5.100}$$

will be concluded. By selecting C_{TL}=250 fF to satisfy Eqn. (5.96), C_{21}=200 fF, C_{22}=350 fF and C_{23}=150 fF based on Eqns. (5.99) and (5.100), and ignoring C_{11} term in Eqn. (5.99) compared to C_{14}, the values for C_{12} and C_{14} should satisfy the following equation

$$C_{12}+C_{14}\geq 1400\,fF\,, \tag{5.101}$$

Table 5.1. List of the selected values for each capacitor in the proposed second-order TMDS modulator

C_{11}	C_{12}	C_{13}	C_{14}	C_{21}	C_{22}	C_{23}	C_{24}	C_{TL}
50 *fF*	700 *fF*	50 *fF*	700 *fF*	200 *fF*	350 *fF*	150 *fF*	125 *fF*	250 *fF*

which in turn is concluded from Eqns. (5.87) and (5.89). The final values selected for these capacitors are set as C_{12}=C_{14}=700 fF.

In Table 5.1, the selected value for each capacitor is listed. Based on the values selected for C_{13} and C_{24}, all the capacitor values may change and the designer is free to select one set of available values based on any other design criteria. After setting the values for each individual capacitor, the bias voltage V_B can be used to set the frequency of the modulator by modifying the $g(V_B)$

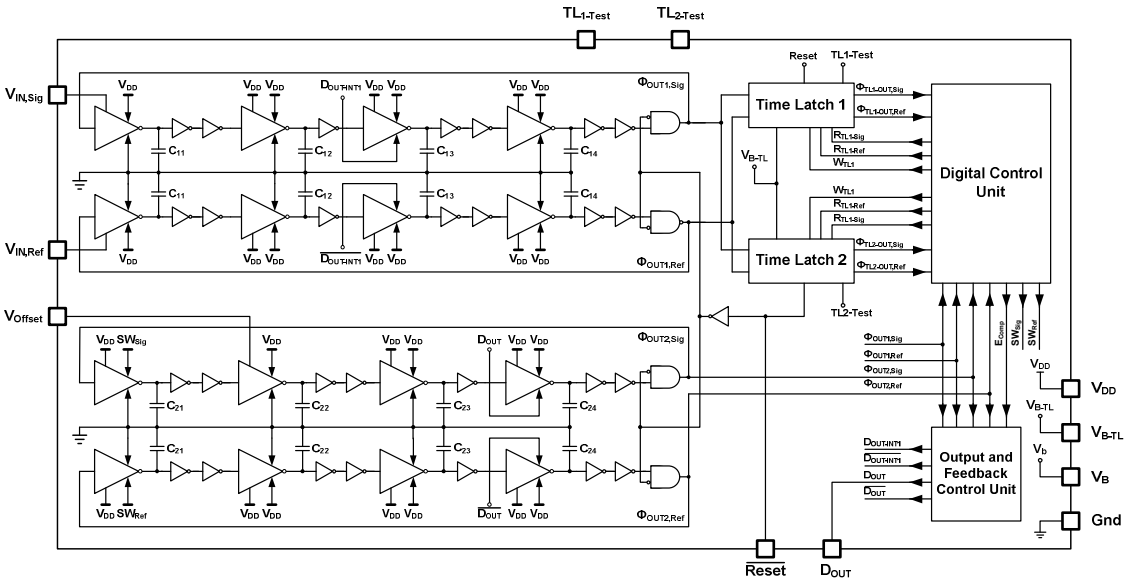


Fig. 5.28. The block diagram of the second-order time-mode delta-sigma modulator implemented in a 0.13-um IBM CMOS technology

constant of the circuit, as will be shown through the simulations.

5.5. Simulation Results

The proposed TMDS modulator was designed and implemented in 0.13-μm IBM CMOS process. The whole diagram of the implemented design is shown in Fig. 5.28. The ring-oscillators in this figure are the ones shown in Figs. 5.24 and 5.25 plus one additional AND gate in each loop. The AND gates are used to cease the oscillation of each oscillator when the input $\overline{Reset}$ signal is activated and to start the oscillation of each two corresponding oscillators in phase when the input $\overline{Reset}$ is deactivated. The capacitors included in the ring-oscillators are set according to Table 5.1. The Digital Control Logic and Time Latches have the same specs as reported for the time-to-time integrator in the previous chapter. Finally, the Output and Feedback Control Unit includes the logic presented in Figs. 5.7 and 5.8 to implement the feedback signals. Transistor dimensions for all circuits are revealed in Appendix A.

The circuit was biased at 1.2 V power supply and the bias voltage, V_B, for all the delay blocks of the modulator was set to 0 V that resulted in the maximum oscillating frequency for each ring-oscillator. The input voltage-to-phase

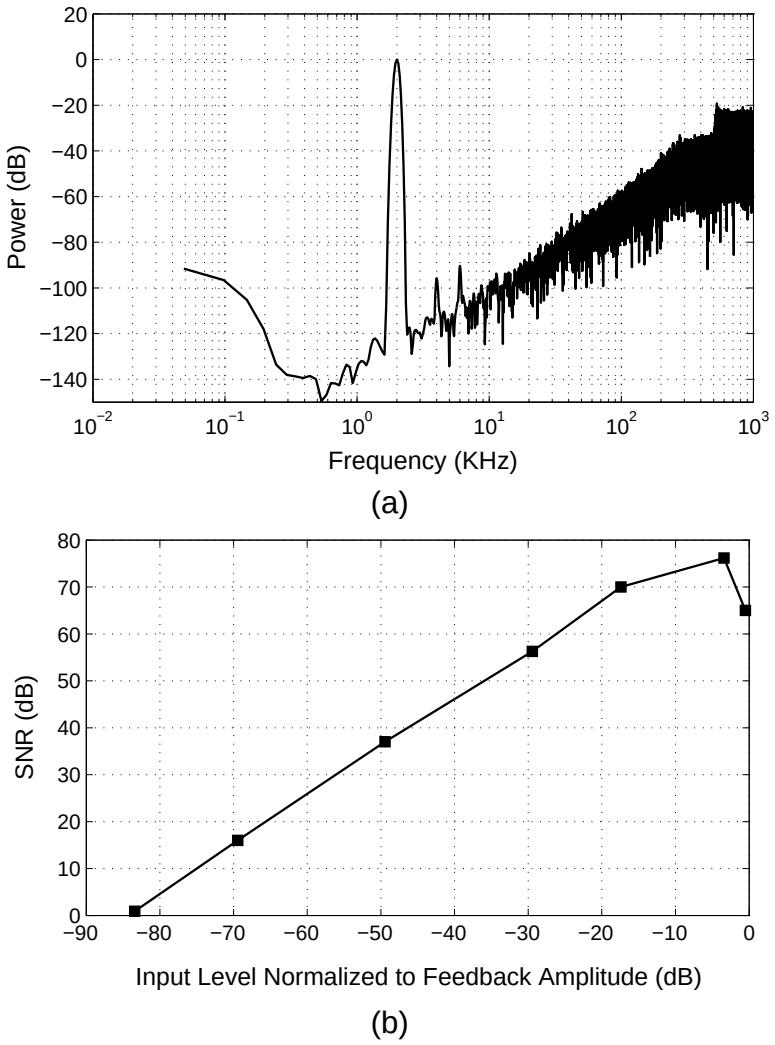


Fig. 5.29. (a) Output PSD spectrum of the proposed TMDS modulator simulated in Spectre for f_{IN}=2 KHz, (b) Dynamic range

conversion coefficient was set to -26 ns/V; also, T_{FB1} and T_{FB2} applied as the feedback to each oscillator in the first and the second integrator were set to 16 ns and 40 ns, respectively.

Based on simulations, average $V_{Th,inv}$ of the inverters included in the VCDUs or SDUs was measured equal to 0.575 V that is the maximum value for the input voltage applied to the input of the modulator (according to Fig. 5.10). This, in turn, results in a maximum peak-to-peak value of 1.15 V for the allowable differential voltage applied to the $V_{IN,Sig}$ and $V_{IN,Ref}$ inputs of the simulated modulator. The CM level for each one of these two signals was set to 0.9 V.

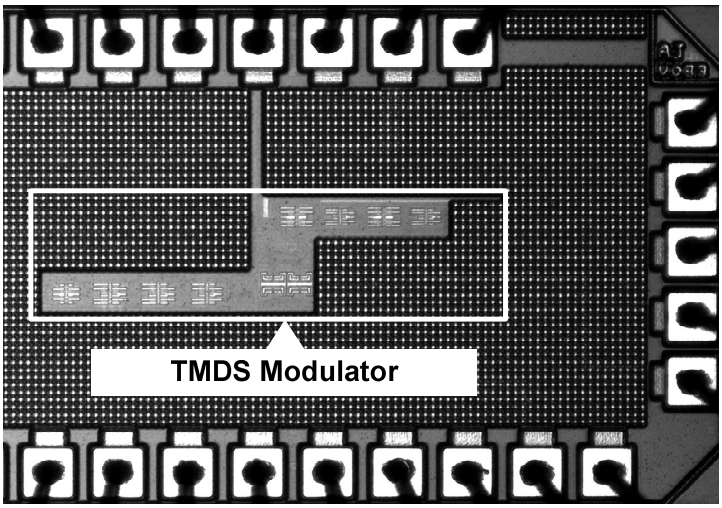


Fig. 5.30. The die photo of the prototype of the TMDS modulator developed in 0.13 um IBM CMOS Technology

The transistor design of Fig. 5.28 was post-layout simulated with Spectre and an example PSD results is presented in Fig. 5.29.a. It can be seen from the PSD plot that the noise increases with frequency at a 40 dB/dec rate, as expected for a second-order delta-sigma modulator. The oscillators were oscillating at an average frequency of 3.215 MHz. The Input frequency was set to 2 kHz with differential amplitude of 0.4 V. The SNDR extracted within a 16 kHz bandwidth (for audio applications) was 76.11 dB. As expected, harmonic distortion due to non-uniform sampling was seen at the output spectrum; however, the second-order harmonic was well attenuated. The input dynamic range, shown in Fig. 5.29.b, was determined to be 80 dB by calculating the SNR of the Spectre simulations for various input levels.

Spectre simulations confirm that the proposed TMDS modulator implements a second-order noise shaping. The differential input configuration, removes the second harmonic distortion induced by non-uniform sampling. The harmonic cancellation that improves the output SFDR with a few orders of magnitude, however, is achievable at the expense of a perfect matching between the ring-oscillators of the first integrator. At the presence of any source of uncompensated mismatch, a factor of the second harmonic will be forwarded to the output that may spoil the output SNDR. Consequently, the effect of non-

uniform sampling on the performance of the modulator is a function of the matching quality as well. For the implementation of the modulator in a low-cost design, where matching techniques are not affordable, using a separate sample-and-hold at the input of the circuit might be necessary to handle high-frequency input signals.

Finally, it should be mentioned that the operation of the modulator is more sensitive to the implementation quality of the first integrator compared to the second one. Any non-ideality associated with the first integrator will be forwarded to the output after a first-order noise shaping where the non-idealities of the second integrator will be attenuated by a second-order noise shaping. One design consideration is to separate the power supplies to each integrator and ensure the power supply to the first stage has an acceptable noise level.

All the above-mentioned simulation results and design analysis prove that the proposed techniques for addition, subtraction, and integration of time-mode variables can be adopted to implement higher orders of delta-sigma modulators. Compared to the semi time-mode delta-sigma modulators reviewed in section 5.2, the presented time-mode second-order delta-sigma modulator does not include any conventional analog block. In addition, despite the design presented in [53], the technique developed in this chapter does not imply only to a specific structure of delta-sigma modulators. Its principles of operations can be extended to modulators of higher orders. It should be reminded that the target of the research conducted in this chapter was not to improve the specs of a second-order delta-sigma modulator. The knowledge of delta-sigma design has been matured during the past decades and many different circuits have been reported. All well-distinguished circuits adopt analog design techniques such as gm-C, switched-cap or continuous integration. In this chapter, it was intended to show that by developing a more advanced series of TMSP techniques, some of the most commonly used analog applications such as a delta-sigma modulator can be implemented in a digital environment adopting digital building blocks. Further evaluation and extension of the proposed TMDS modulation technique is the subject of future research.

5.6. Experimental Results

The microphotograph of the prototype of the proposed second-order time-mode delta-sigma modulator implemented in a 1.2V 0.13-μm IBM CMOS process is shown in Fig. 5.30 while part of the circuit in the figure is covered by a passivation layer. The integrator occupies an area of 700μm×210μm including the output buffers. The same test board and test setup as shown in Fig. 4.23 was used to test the performance of the circuit.

The implemented prototype failed to operate. It is strongly believed that the failure happened because the input transistors were damaged due to the lack of proper ESD protection at the I/O pads[‡]. The ARM ESD PCells included in the IBM design Kit were not available to non-Canadian citizens; also, due to time shortage prior to tape-out it was not possible to design proper ESD circuits. Assuming special attention will be paid during the test, the design was submitted for fabrication. The fabricated prototypes were delivered in original package with un-cut pins. It is believed that a number of the chips had been damaged due to ESD problems during the cutting of the pins since professional equipments were not available. During the test, a major number of the prototypes showed live and meaningful signals; however, due to high number of input pins all connected to some CMOS gates it was not possible to test the performance of the chip. As the design of the modulator was based on the post-calibration of the chip, any interaction with the chip through the input pins was subject to ESD damages. The other probable scenario was the antenna effect. Long metal wires were used to connect the input I/O to the corresponding gates. Due to the lack of ESD diodes, the accumulated charge over some of these tracks may have burnt the corresponding gates. Since the chip was covered by a passivation layer, it was not possible to investigate the die after the signals had been discontinued; however, these two possible scenarios were mostly confirmed where the input

[‡] After the testing phase was over, it was figured out that National Instrument™ had a group of data acquisition modules that could be used in such a situation. For example, NI USB-6210 is a bus-powered multifunction data acquisition module that is optimized for superior accuracy at fast sampling rates. This module could be used as an easy-to-use interface to forward the proper analog and digital inputs into the sensor interface circuit; in that situation, all the pins connected to the inputs of the test chip were associated with proper ESD protection circuits.

resistance of some input pins were decreased from open circuit to a few kilo or hundreds of ohm after the live signals were discontinued.

5.7. Summary

This chapter explored the design of a second-order time-mode delta-sigma modulator utilizing the TMSP components described in the previous chapters. The feasibility of implementation and proof of concept for the proposed modulator was justified by transistor level simulations. The simulation results demonstrated a second-order noise shaping with a maximum output SNR of 76 dB. Harmonic distortion was observed in the output spectrum that was explained by the non-uniform sampling at the input of the modulator. While the differential structure of the design can reduce the even-order harmonic distortion, a sample-and-hold circuit could be included to remove the distortion in presence of mismatches. The methodology proposed in this chapter offers a potential avenue for the digital implementation of delta-sigma modulators. By utilizing digital blocks alongside voltage-controlled delay units, the limitations introduced to the analog design in deep sub-micron technologies can be tackled. While a CMOS implementation in a 1.2 V 0.13 um process from IBM was fabricated, the test of the chip failed due to ESD damages encountered to the input stage of the prototype.

Chapter 6: Time-Mode Readout Circuitry for Capacitive Sensors

6.0. Introduction

In previous chapters, practical techniques were proposed to implement the storage, addition, subtraction and integration of time-mode variables. The feasibility of these functions extends the application of TMSP to the implementation of well-known topologies like delta-sigma modulators and filters. These techniques, as one of the most fundamental blocks in any signal processing methodology, open the door for digital processing of analog information. To take more advantage of TMSP, the concept of voltage to time conversion can be extended into other domains. So that, by converting real world variables into time, we can sense, measure and control our environment in a digital domain.

In this chapter, the application of capacitance to time conversion is adopted to implement very affordable interface circuits to readout the output capacitance of capacitive sensors for lab on chip applications. It will be shown that digital building blocks can be used to develop generic interface circuits without any concerns about matching or component trimming.

6.1. Interfacing Capacitive Sensors

Capacitive sensing is used extensively in a wide range of micro-electromechanical sensors (MEMS). It offers low-power operation, high

sensitivity, low temperature variation, simple structure and the option of applying electrostatic actuation for closed-loop control [63,64].

Due to the high impedance nature of a capacitor at low frequencies, capacitive sensing is susceptible to parasitic components and noise at the interface between the readout circuit and the capacitor [65]. The design of the readout circuit cannot be initiated until the specification of the sensor is finalized and the range of the capacitance subject to measurement is determined. One approach that attempts to circumvent the need to know the specifications in advance of fabrication is to integrate alongside the sensor a bank of capacitors that can be digitally adjusted to compensate for processing errors associated with MEMS sensor. In [66] the reference capacitor is implemented through a gyrator, which can be tuned by changing the resistors associated with the gyrator; however, resistors themselves are not easily adjustable over a continuous range of resistor values, especially in fully monolithic form.

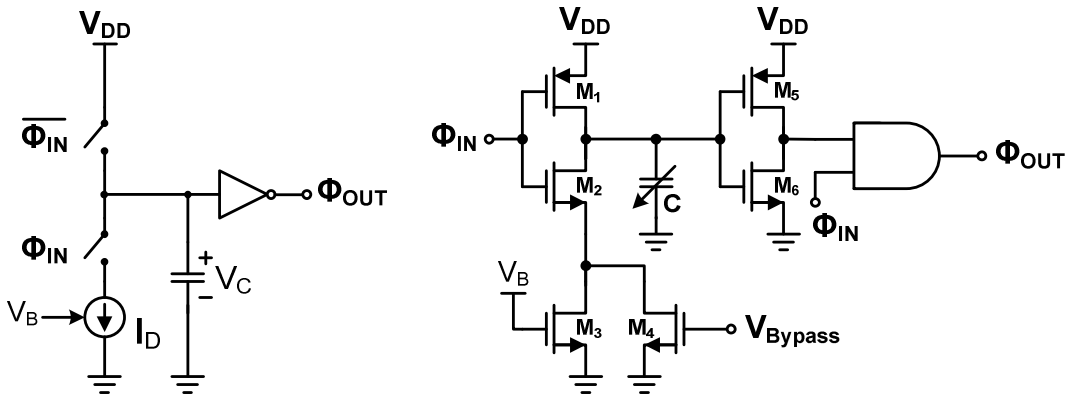
Manufacturing technologies used to construct practical sensors generally do not include the electronics for the readout circuitry and they are developed on separate dies and assembled together in multi-chip packages. In such cases, interconnection parasitic capacitances may evoke sensor repeatability errors and offsets that may mask the useful signal information. In [64, 67, and 68], some advanced switched-capacitor (SC) circuits have been reported, whereby the resolution of the readout circuit has been as low as 10 aF with compensation for interconnect parasitic capacitance. However, such SC circuits usually employ a significant amount of operational amplifiers and switches synchronized by multiphase clock-signals that prevent them from being used in applications where die-size and power-budget constitute critical requirements [69]. On the other hand in cases where sensor is manufactured alongside its readout circuit on the same die, the silicon-substrates suffer from poor uniformity, forcing transistor parameter-variation to rise [70, 71]. This fact sets another requirement for the readout circuit that has minimum sensitivity to process variations. In [72], although the authors have claimed a digital readout technique, the input front-end of the design consists of SC circuits and operational amplifiers. In [73], a digital-

compatible technique is presented that it mostly takes advantage of low-sensitivity components; however, the method is just applicable for differential capacitive sensors. Moreover, to achieve finer resolution, high frequency clocks are required thereby increasing the power consumption even further.

Application of an AC bridge with voltage amplification [74] and trans-impedance amplification [75] are two other techniques previously reported. These circuits are capable of measuring a capacitance change of less than 1 fF. To achieve such a low resolution, however, additional blocks and techniques are included to control or cancel charge injection and component mismatching effects; thus, the increased measuring resolution comes at a dramatic increase in power consumption and design complexity. Finally, the charge-based capacitance-measurement approach (CBCM) [76] eliminates the need for a reference capacitor; however, this method relies on an accurate current measurement whose precision is highly dependent on the complexity of the on-chip circuitry.

An increasing number of medical, entertainment and sports applications are making use of sensor systems in and around the body. These sensors should work as distributed small units that can collect data over a long period and consume ultra-low power [77]. Many of the sensor interfaces previously reported are fixed designs, tailored towards one specific application. The development of sensor interface circuits that are suited for a wider range of applications would help to reduce the cost of such circuits and speed their time-to-market. In some ways, a more generic topology for a sensor interface circuit is required.

This chapter presents the design and experimental results of a proof-of-concept prototype implementation for a novel low-power, low-cost semi-digital generic delta-sigma sensor interface circuit. The circuit is developed by adopting time-mode signal processing. It uses two capacitance-controlled ring-oscillators to perform a capacitance-to-time conversion. The output time difference is quantized to a serial stream of output bits through a configurable delta-sigma structure. By adopting delay units, the circuit can be tuned for different capacitance ranges from a single reference capacitor; also, the resolution or



(a) (b)

Fig. 6.1. (a) The symbolic block diagram for a voltage controlled delay unit, (b) circuit diagram for a capacitance-controlled delay unit (CCDU)

sensitivity to resolve coarse/fine input capacitance variations can be externally adjusted. Due to the digital nature of the circuit, digital routines can be used to control the linear operation and to implement the calibration procedure to correct for process variations.

6.2. Delta-Sigma Interface for Capacitive Sensors

6.2.1. General Operation

As explained in Chapter 3, the delay between the rising edges at the input and output of a voltage-controlled delay unit, shown in Fig. 6.1.a, is denoted as T_{Delay} and it is well defined using the following equation

$$T_{Delay} = \frac{C \times (V_{DD} - V_{Th,inv})}{I_D} \tag{6.1}$$

where I_D is the discharge current and $V_{Th,inv}$ represents the threshold voltage for the output inverter. By changing the capacitor, C, the slope of the discharge procedure changes linearly. Correspondingly, we can relate the delay to the

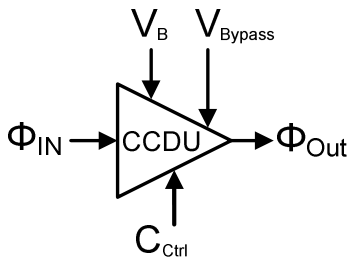


Fig. 6.2. The circuit symbol for a CCDU

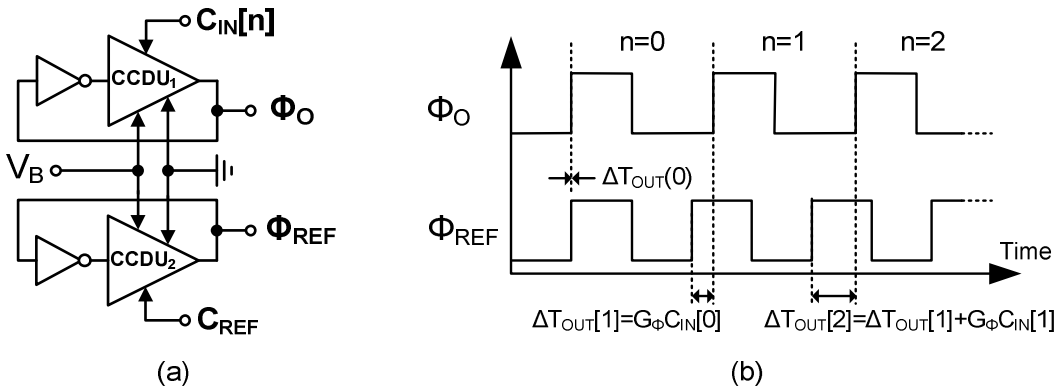


Fig. 6.3. (a) capacitance-to-time integrator, (b) timing diagram for the integrator

capacitance variable according to the following equation

$$T_{Delay} = F_{\phi} C \tag{6.2}$$

F_{Φ} denotes the proportionality coefficient that relates the two quantities as described by Eqn. (6.2), i.e.

$$F_{\phi} = \frac{V_{DD} - V_{Th,inv}}{I_D}. \tag{6.3}$$

It is evident from Eqn. (6.1) that the delay of the circuit shown in Fig. 6.1.a is linear in terms of the capacitor value *C*. This block may be called a Capacitance-Controlled Delay Unit (CCDU). In Fig. 6.1.b, the CMOS schematic for the CCDU is presented. It is the same as the diagram for a VCDU where an additional AND gate is used to ensure that the input falling edge at Φ_{IN} is propagated to the output without being influenced by the control capacitance, *C*. Also, transistor M_4 is included to discharge the control capacitor quickly and to bypass the capacitance-controlled delay of the block, where applicable. Fig. 6.2 shows the circuit symbol for the developed CCDU.

Capacitance-to-time integration may be implemented by connecting the CCDU outputs to their respective inputs through an inverter. This circuit is equivalent to two capacitance-controlled ring oscillators and is depicted in Fig. 6.3.a. Considering C_{IN} equal to C_{REF}, the delay induced by these two blocks will be the same. Ignoring the mismatches between the gates in the two ring oscillators, the oscillation period for both oscillator outputs, Φ_O and Φ_{REF}, will be the same. Writing the time of the output rising edge in terms of the arrival time for

the input edge into each CCDU as a function of the sampling instance, *n*, we can write

$$t_O[n] = t_I[n-1] + F_\phi C_{IN}[n-1] \tag{6.4}$$

and

$$t_{REF}[n] = t'_I[n-1] + F_\phi C_{REF} \tag{6.5}$$

where, t_I (and t'_I) and t_O (and t_{REF}) represent the time for the rising edges at the inputs and outputs of $CCDU_1$ (and $CCDU_2$) respectively. Furthermore, the feedback path established by the inverter allows us to state

$$t_I[n-1] = t_O[n-1] + \tau_{CCDU} + 2\tau_{inv} \tag{6.6}$$

and

$$t'_I[n-1] = t_{REF}[n-1] + \tau_{CCDU} + 2\tau_{inv} \tag{6.7}$$

where, $\tau_{CCDU}+2\tau_{inv}$ is the total propagation delay of a low-to-high transition at the CCDU output back to its input as a low-to-high transition. Apparently, this delay is independent of the CCDU control capacitance. Combining Eqns. (6.4)-(6.7), we can write

$$t_O[n] = t_O[n-1] + F_\phi C_{IN}[n-1] + \tau_{CCDU} + 2\tau_{inv} \tag{6.8}$$

and

$$t_{REF}[n] = t_{REF}[n-1] + F_\phi C_{REF} + \tau_{CCDU} + 2\tau_{inv}\,. \tag{6.9}$$

Finally, by subtracting Eqn. (6.9) from Eqn. (6.8), we obtain

$$\Delta T_{OUT}[n] = t_O[n] - t_{REF}[n] = \Delta T_{OUT}[n-1] + F_\phi\left(C_{IN}[n-1] - C_{REF}\right) \tag{6.10}$$

Here, $\Delta T_{OUT}[n]$ represents the time difference between the signals at the outputs of the two oscillators. A timing diagram demonstrating three samples of the integrator operation is presented in Fig. 6.3.b. The initial integrator output time-difference $\Delta T_{OUT}[0]$ is assumed equal to zero. The next time-difference $\Delta T_{OUT}[1]$ is shown proportional to the input capacitance at time instance $n=0$. The proceeding output $\Delta T_{OUT}[2]$ is the sum of $\Delta T_{OUT}[1]$ and the input capacitance $C_{IN}[1]$ scaled by F_Φ.

The developed capacitance-to-time integrator of Fig. 6.3.a can be extended to a delta-sigma modulator based on the error-feedback structure for a

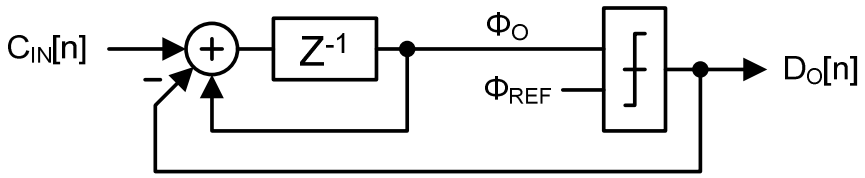


Fig. 6.4. Block diagram for a first-order delta-sigma modulator

first-order delta-sigma modulator presented in Fig. 6.4. The output quantizer is a single-bit comparator (DFF) to check for the sign of the output phase difference. To implement the DAC operation included in Fig. 6.4, the output bit should be applied directly to the bypass input of one of the CCDUs in the ring oscillators shown in Fig. 6.3.a. This will cause the delay of the corresponding CCDU to be excluded from the loop delay when the DFF output D_O is "1", as well force the instantaneous oscillation period of the corresponding oscillator to decrease. Conversely, when the DFF output is "0", the delay induced by the CCDU will be accumulated into the overall loop delay.

The complete system of the delta-sigma-based interface is presented in Fig. 6.5 and it consists of two ring-oscillator loops forming a capacitance-to-time integrator and one DFF. For ease of reference, the top oscillator will be referred to as the signal oscillator and the bottom oscillator will be referred to as the reference oscillator. All CCDUs are biased at the fixed voltage of V_B and the

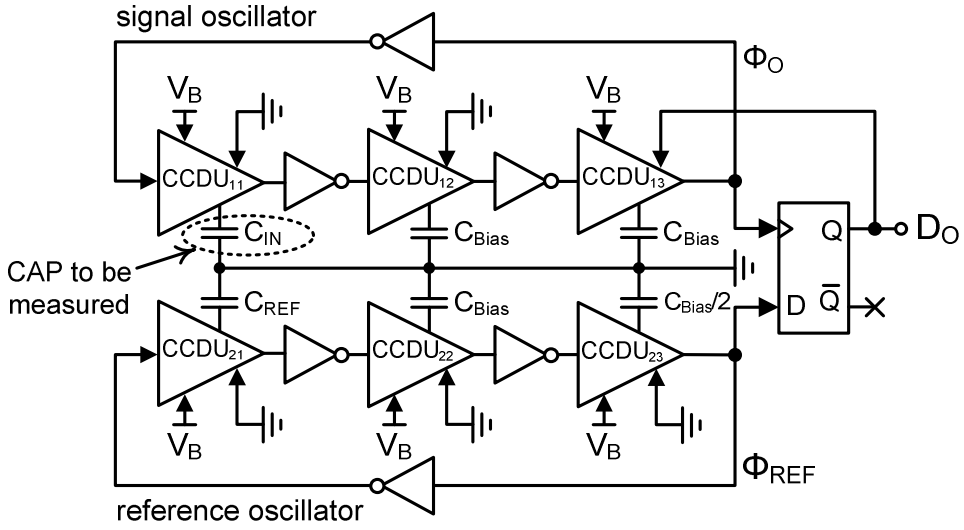


Fig. 6.5. The circuit schematic for the proposed first-order delta-sigma sensor interface circuit

control capacitors for $CCDU_{12}$, $CCDU_{13}$, and $CCDU_{22}$ are fixed to C_{Bias}. For feedback purposes, the bias control capacitor of $CCDU_{23}$ is set to $C_{Bias}/2$. The bypass input to $CCDU_{13}$ is connected to the output of the DFF whereas all other CCDU bypass inputs are connected to ground.

As previously explained, the delay behavior of a CCDU block while its bypass input is connected to ground is governed by Eqn. (6.1). However, as the discharge current I_D is controlled by V_B, this equation can be rewritten in general terms as a function of the bias voltage, i.e.

$$T_{CCDU} = C \times f(V_B). \tag{6.11}$$

Now returning to the circuit of Fig. 6.5, the period of each oscillator can be derived by considering the delay around each loop to invert any step change in the output levels for Φ_O and Φ_{REF}. In the case of a high-to-low step change at the output of the reference oscillator, the propagation delay around the loop to invert it back to a low-to-high step can be written as

$$T_{REF,Low} = 3\tau_{inv} + C_{REF} \times f_{21}(V_B) + \tau_{CCDU\ 22} + \frac{C_{Bias}}{2} \times f_{23}(V_B), \tag{6.12}$$

where, we make use of the delay-bias voltage functional notation for each CCDU in the loop. Likewise, the low-to-high step change at the output of the reference oscillator lasts as long as the time given by

$$T_{REF,High} = 3\tau_{inv} + \tau_{CCDU21} + C_{bias} \times f_{22}(V_B) + \tau_{CCDU23}. \tag{6.13}$$

Consequently, the total period of any single oscillation at the output of the reference oscillator can be written as

$$T_{REF} = T_{REF,Low} + T_{REF,High}. \tag{6.14}$$

Similar equations might be extracted for the signal oscillator as well. The falling edge at the output of the signal oscillator will be inverted through the loop after a time described by

$$T_{O,Low} = 3\tau_{inv} + C_{IN} \times f_{11}(V_B) + \tau_{CCDU12} + (1 - D_O) \times C_{Bias} \times f_{13}(V_B). \tag{6.15}$$

Finally, the propagation delay for the rising edge is equal to

$$T_{O,High} = 3\tau_{inv} + \tau_{CCDU11} + C_{Bias} \times f_{12}(V_B) + \tau_{CCDU13} \tag{6.16}$$

And the total period for any single oscillation at the output of the single oscillator

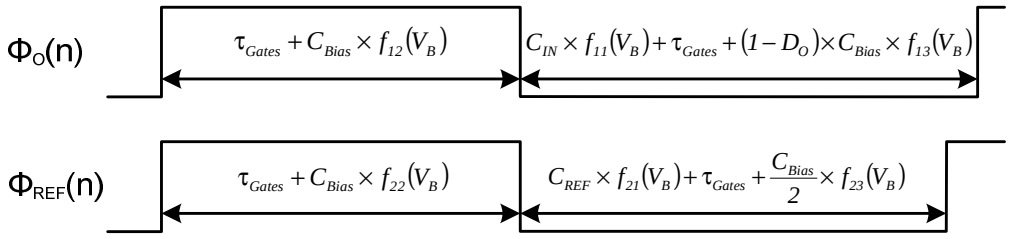


Fig. 6.6. The duration of a single period of the SIG and REF oscillators

is given by

$$T_O = T_{O,Low} + T_{O,High}. \tag{6.17}$$

The reference oscillator in Fig. 6.5, provides the clock reference for the output comparator. Fig. 6.6 shows the timing signals for each oscillator output, Φ_O and Φ_{REF}, based on the results derived above. As is evident from the timing diagram, the reference oscillation period is independent of the input capacitance C_{IN} and DFF state, D_O. It is essentially constant throughout the operation of the sensor interface. However, the time width for the low-level state of the signal oscillator is a function of both C_{IN} and D_O; thus, making the period of this oscillator a function of the capacitance subject to measurement. As the DFF quantizes the accumulated time difference between the instantaneous periods of the two oscillator outputs, Φ_O and Φ_{REF}, we can write this quantity as

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + T_O[n] - T_{REF} \tag{6.18}$$

Using Eqns. (6.12) - (6.17), Eqn. (6.18) leads to a recursive expression for the instantaneous output time-difference $\Delta T_{OUT}[n]$. The resulting expression is rather complicated. Instead, let us consider $CCDU_{11}$, $CCDU_{12}$, and $CCDU_{13}$ identical to $CCDU_{21}$, $CCDU_{22}$, and $CCDU_{23}$ respectively; also, the $f(V_B)$ function representing them will be $f_1(V_B)$, $f_2(V_B)$, and $f_3(V_B)$ as well. The resulting expression becomes

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + (C_{IN}[n-1] - C_{REF}) \times f_1(V_B) + C_{bias} \times f_3(V_B) \times \left\{ \frac{1}{2} - D_O[n-1] \right\} \tag{6.19}$$

Assuming $D_O[n]$ is a digital signal toggling between “0” and “1”, the error signal $\Delta T_\varepsilon[n]$ induced by the DFF comparison may be expressed as the difference between the instantaneous output time difference and the size of the delay

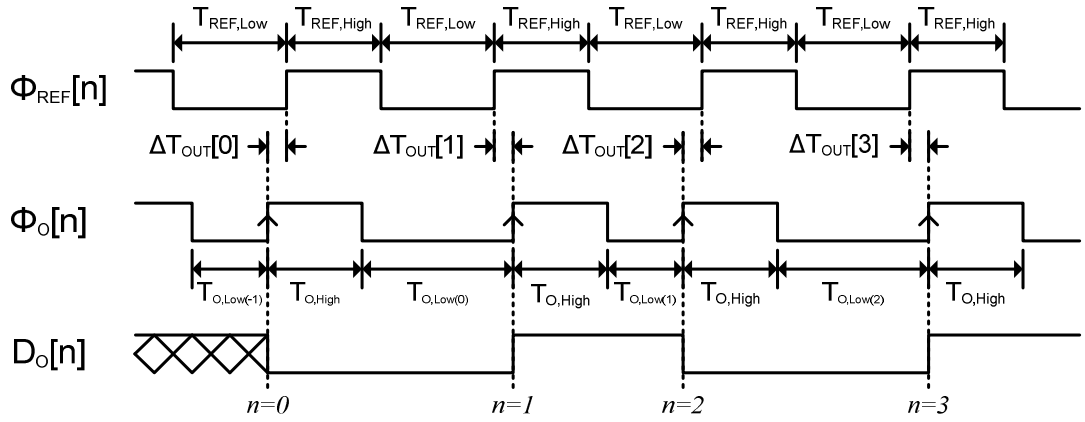


Fig. 6.7. Timing diagram of a short sequence of the delta-sigma operation

injected back into the loop, i.e.,

$$\Delta T_{\varepsilon}[n] = \Delta T_{OUT}[n] - C_{Bias} \times f_3(V_B) \times \left\{ D_O[n] - \frac{1}{2} \right\}. \tag{6.20}$$

Substituting Eqn. (6.20) into (6.19) reveals the first-order ΔΣ modulator difference equation as

$$D_O[n] = \frac{f_1(V_B)}{C_{Bias} \times f_3(V_B)} \{C_{IN}[n-1] - C_{REF}\} - \frac{1}{C_{Bias} \times f_3(V_B)} \{\Delta T_{\varepsilon}[n] - \Delta T_{\varepsilon}[n-1]\} + \frac{1}{2}. \tag{6.21}$$

Fig. 6.7 presents an example illustrating the timing of four periods of the modulator's operation with input condition C_{IN}=C_{REF}. The period of oscillation for Φ_{REF} is fixed; also, the duration of the high level corresponding to Φ_O is fixed at $T_{O,High}$. Here, the reader can see that how the duration of the logic low signal oscillator output toggles with constant input capacitance and DFF output.

6.2.2. Linear Range of Operation

C_{REF} is the reference value for the input capacitance C_{IN} and the system is designed to measure any capacitance variation compared to it. It means the input capacitance can be re-written as

$$C_{IN}[n] = C_{REF} + \Delta C_{IN}[n] \tag{6.22}$$

By substituting Eqn. (6.22) into (6.19), one can write an expression for the modulator output as:

$$\Delta T_{OUT}[n] = \Delta T_{OUT}[n-1] + \Delta C_{IN}[n-1] \times f_1(V_B) + C_{Bias} \times f_3(V_B) \times \left\{ \frac{1}{2} - D_O[n-1] \right\} \tag{6.23}$$

For stable modulator operation, the latter two terms associated with Eqn. (6.23) must undergo a full sign change. When D_O= “0”, we should have

$$\Delta C_{IN} \times f_1(V_B) + C_{Bias} \times \frac{f_3(V_B)}{2} > 0 . \tag{6.24}$$

Similarly, when D_O= “1”, we should have

$$\Delta C_{IN} \times f_1(V_B) - C_{Bias} \times \frac{f_3(V_B)}{2} < 0 , \tag{6.25}$$

which leads to the following condition on the input capacitance for linear operation

$$-\frac{C_{Bias}}{2} \times \frac{f_3(V_B)}{f_1(V_B)} < \Delta C_{IN} < \frac{C_{Bias}}{2} \times \frac{f_3(V_B)}{f_1(V_B)} . \tag{6.26}$$

Another condition for linear operation depends on the duration of the signal oscillator when its output, Φ_O, is logically low. As this duration is a function of the input capacitance, CCDU delay, and state of DFF, it can take on a large range of values. If this duration is longer than a period of the reference oscillator, as depicted in Fig. 6.8, then it is possible to lose one full cycle of the reference oscillator, e.g., create a cycle slip. To avoid such a condition, the timing for both oscillator outputs should satisfy the following relation,

$$T_{High} + T_{O,Low}\big|_{D_O=0} \le 2T_{High} + T_{REF,Low} , \tag{6.27}$$

where we assume that the logic high duration for each oscillator output are the same, i.e., T_{High}=$T_{REF,High}$=$T_{O,High}$. Eqn. (6.27) can be further simplified to

$$T_{High} \ge T_{O,Low}\big|_{D_O=0} - T_{REF,Low} . \tag{6.28}$$

Substituting corresponding expressions for each variable in (6.28) results in

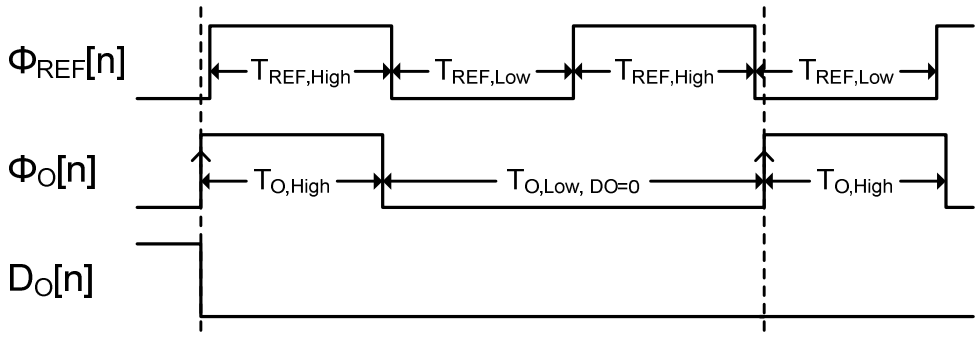


Fig. 6.8. The feedback pushing the circuit out of linear operation

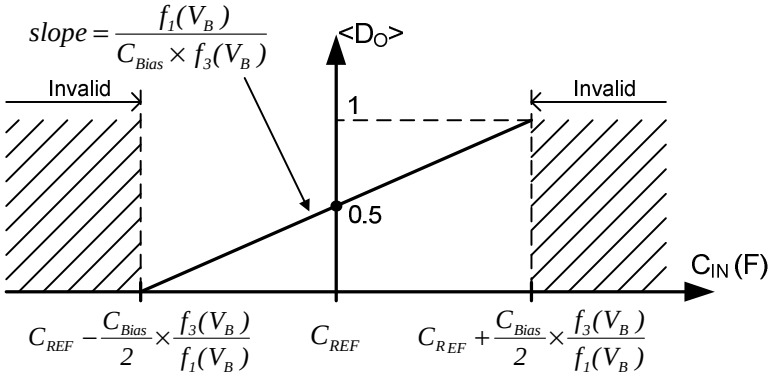


Fig. 6.9. Transfer characteristic of the sensor interface circuit

$$T_{High} \geq \Delta C_{IN} \times f_1(V_B) + \frac{C_{Bias}}{2} \times f_3(V_B). \tag{6.29}$$

The inequality shown in Eqn. (6.29) should be satisfied even for the largest value of the input capacitance specified by (6.26); ignoring the minor values for gate delays, Eqn. (6.29) can be reduced to

$$f_2(V_B) \geq f_3(V_B). \tag{6.30}$$

This expression indicates that for the same control capacitor, C_{Bias}, the delay induced by $CCDU_{12}$ and $CCDU_{22}$ should be equal or greater than the delay induced by $CCDU_{13}$ and $CCDU_{23}$ to guarantee the linear operation of the circuit when the input differential capacitance is within the linear range.

Satisfying inequality Eqn. (6.26) and Eqn. (6.30), the sensor interface operates in its linear mode and the error term ΔT_ε in Eqn. (6.21) will be removed through noise-shaping and averaging. As a result, the average value of the digital output will be equal to

$$\langle D_O \rangle = \frac{f_1(V_B)}{C_{Bias} \times f_3(V_B)} \Delta C_{IN} + \frac{1}{2} \tag{6.31}$$

where $\langle\ \rangle$ denotes the average value. In Fig. 6.9, the transfer characteristic of the sensor interface circuit is shown. Here the limits of the input differential capacitance are provided in terms of the C_{Bias} and the bias voltages. Also shown is the dependency of the slope (or gain) of the linear region in terms of these same two quantities. Outside of the linear region, the average value of digital output will be uncorrelated to the input capacitance and its value is invalid.

6.2.3. Noise Behavior

To characterize the effect of noise on the overall performance of the sensor interface circuit, two independent noise sources $v_{n,b}$ and $v_{n,d}$ are considered accompanied with the voltages V_B and V_{DD} in Fig. 6.1.b. Since transistor M_3, on the same figure, operates in the saturation region, the formula governing the discharge current can be written as

$$I_{D3} = \beta(V_B + v_{n,b} - V_{Th3})^2 \tag{6.32}$$

Expanding Eqn. (6.32) as a power series,

$$I_{D3} = \beta(V_B - V_{Th3})^2 + 2\beta(V_B - V_{Th3})V_{n,b} + \beta V_{n,b}{}^2 . \tag{6.33}$$

where, V_{Th3} represents the threshold voltage of transistor M_3. With condition $v_{n,b} << V_B - V_{Th3}$, we can ignore the last term and write the discharge current as

$$I_{D3} = I_D + K_n v_{n,b} . \tag{6.34}$$

Here I_D is the original discharge current without taking noise into account and $K_n = \beta(V_B - V_{Th3})$. Clearly, the noise $v_{n,b}$ associated with V_B is directly added to the discharge current. Substituting Eqn. (6.34) in Eqn. (6.1) and considering the noise source $v_{n,d}$ associated with V_{DD}, the delay formula influenced by noise will be

$$T_{CCDU,noise} = \frac{C \times (V_{DD} + v_{n,d} - V_{Th,inv})}{I_D + K_n v_{n,b}} . \tag{6.35}$$

Again provided $K_n v_{n,b} < I_D$, Eqn. (6.35) can be expanded using a binomial expansion leading to

$$T_{CCDU,noise} = \frac{C \times (V_{DD} - V_{Th,inv} + v_{n,d})}{I_D}\left(1 - \frac{K_n v_{n,b}}{I_D} + \frac{K_n^2 v_{n,b}^2}{I_D^2} \ldots\right). \tag{6.36}$$

Considering Eqn. (6.1) and ignoring the second and higher order components in (6.36), the formula for delay of a CCDU block can be written as the sum of a noise-free term and a noise component, i.e.

$$T_{CCDU,noise} = T_{CCDU} + \tau_{Noise} ; \tag{6.37}$$

where τ_{Noise} is given by

$$\tau_{Noise} = \frac{C}{I_D} v_{n,d} - \frac{T_{CCDU} K_n}{I_D} v_{n,b} - \frac{K_n C}{I_D^2} v_{n,b} v_{n,d} \tag{6.38}$$

Assuming that $v_{n,b}$ and $v_{n,d}$ are two noise sources that are uncorrelated with zero mean value, the expected value of the jitter will be equal to zero and the mean square value of the jitter will be

$$\sigma_{\tau}^{2} = \frac{C^{2}}{I_{D}^{2}}\sigma_{v_{n,d}}^{2} + \frac{T_{Delay}^{2}K_{n}^{2}}{I_{D}^{2}}\sigma_{v_{n,b}}^{2} \tag{6.39}$$

So, if the noise sources are Gaussian with zero mean value, the jitter will also be Gaussian with zero mean value and a variance equal to Eqn. (6.39).

The delay around each loop is the summation of the delays of the CCDUs in that loop; so, each oscillating signal undergoes the same type of jitter as a single CCDU block, albeit with some scaling coefficient between 1 and 3. Hence, Eqn. (6.39) provides the key noise behavior of each oscillator.

6.2.4. Impact of Transistor Mismatches

The architecture of the proposed circuit is differential and the reference and signal oscillator are supposed to be identical but have different control capacitors. However, mismatches are unavoidable in any CMOS process and it is impossible to have the two ring oscillators completely matched.

As shown in Fig. 6.5, the proposed circuit is composed of a series of inverters and CCDUs. Each component contributes to the overall performance by the propagation delay of the signal passing through that component. Mismatches between the corresponding elements in two oscillators will show up as the difference between the loop delays. As a result, any phase difference between the two oscillators might be modeled as a $v_{Mismatch}$ voltage connected to one of the CCDUs in the reference oscillator in series with the bias voltage of that CCDU or it can be modeled as a $c_{Mismatch}$ capacitor connected across the reference capacitor. As will be explained next, the effect of mismatches between the oscillators will be eliminated through the calibration procedure on start-up.

6.3. Tuning and Controlling the Sensor Interface Circuit

6.3.1. Changing the C_{REF} and the Range/Sensitivity of the Circuit

As previously explained, the six CCDUs adopted in the sensor interface circuit were presented by three different functions $f_1(V_B)$, $f_2(V_B)$, and $f_3(V_B)$. By controlling each individual CCDU, more control over the range of operation and

sensitivity of the circuit will be possible. For the rest of this paper, $CCDU_{11}$ and $CCDU_{21}$ will be represented by individual functions $f_{11}(V_B)$ and $f_{21}(V_B)$, respectively, and considering Eqn. (6.22), Eqns. (6.26) and (6.31) will change accordingly as

$$-\frac{C_{Bias}}{2}\times\frac{f_3(V_B)}{f_{11}(V_B)}<\Delta C_{IN}<\frac{C_{Bias}}{2}\times\frac{f_3(V_B)}{f_{11}(V_B)} \tag{6.40}$$

and

$$\langle D_O\rangle=\frac{f_{11}(V_B)}{C_{Bias}\times f_3(V_B)}(C_{IN}-C_{REF})+\frac{1}{2}. \tag{6.41}$$

As explained in the previous sections, each control capacitor contributes to the circuit by influencing the partial delays around each loop, as formulated by Eqn. (6.11). By changing C_{REF} in the modulator shown in Fig. 6.5 to $n\times C_{REF}$, the delay induced by $CCDU_{21}$ will be equal to

$$T_{CCDU\,21}=n\times C_{REF}\times f_{21}(V_B), \tag{6.42}$$

which can be rewritten as

$$T_{CCDU\,21}=C_{REF}\times f_{21}(V'_B), \tag{6.43}$$

when the following condition is assumed

$$f_{21}(V'_B)=n\times f_{21}(V_B). \tag{6.44}$$

Eqns. (6.42) and (6.43) indicates that there are two ways in which to achieve the same delay. One is to use a capacitance of $n\times C_{REF}$ and a bias voltage of V_B and the other is to use a physical reference capacitance of C_{REF} and a different bias voltage of V'_B. In other words, the effect of any change in the reference capacitor can be simulated by the change of the bias voltage. By increasing the bias voltage V_B, the magnitude of $f(V_B)$ decreases; by considering a fixed value for C_{REF}, the reference capacitance level in the circuit decreases. So, the bias voltage applied to $CCDU_{21}$ can be used to change the reference capacitance level of the sensor interface circuit while the range of operation and the sensitivity of the sensor interface circuit do not change. To proceed with this idea, the new concept of equivalent capacitance reference level, $C_{REF,EQV}$, can be defined as

$$C_{REF,EQV}=C_{REF}\times n_{21}(V'_B), \tag{6.45}$$

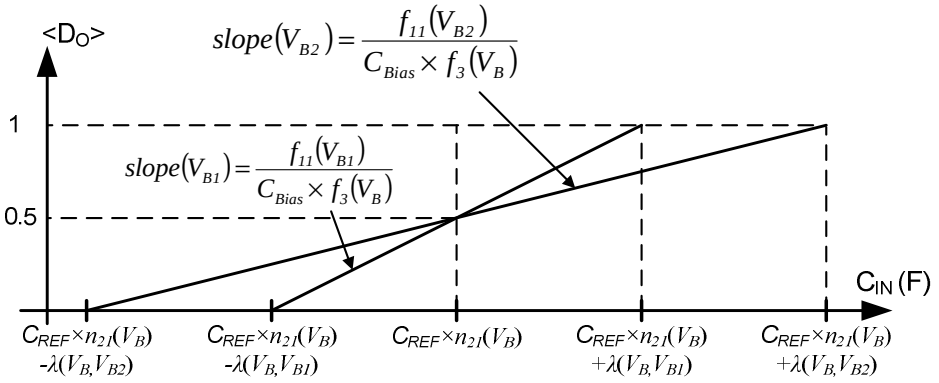


Fig. 6.10. Transfer characteristic of the sensor interface circuit for two different bias conditions on $CCDU_{11}$

where $n_{21}(V'_B)$ represents the scaling factor controlled by the bias voltage connected to $CCDU_{21}$. By changing this bias voltage, the capacitance reference level of the sensor interface circuit will change.

The same process might be implemented to modify the sensitivity of the sensor interface circuit. With respect to Eqn. (6.41), for the same output range, scaling the numerator term $f_{11}(V_B)$ by some factor, say α, the input differential capacitance C_{IN}-$C_{REF,EQV}$ can be scaled by the factor $1/\alpha$. This situation is depicted in Fig. 6.10 for two different bias conditions V_{B1} and V_{B2} when $V_{B1} < V_{B2}$. Here we make use of the functional representation

$$\lambda(V_B, V_{BN}) = \frac{C_{Bias}}{2} \frac{f_3(V_B)}{f_{11}(V_{BN})} \tag{6.46}$$

In effect, changing the bias voltage of $CCDU_{21}$ changes the equivalent reference capacitance and changing the bias of $CCDU_{11}$ changes the sensitivity of the circuit. Collectively, these two control variables enable the circuit to operate over a wide range of input capacitance conditions.

6.3.2. Detection of Non-Linear Operation

If the sensor interface behaves linearly, where the input capacitance C_{IN} is within the range specified by Eqn. (6.40), for each cycle of the signal oscillator there should be a corresponding cycle from the reference oscillator. If one of the rising edges is missing, it is good evidence that the input capacitance is out of range, as will be explained shortly. By observing the output of each oscillator, together with the state of the DFF, a digital code can be devised that keeps track

of the sequence of events occurring within the circuit. One component of the digital code consists of the order in which the rising edges appear at the output of each oscillator. For example, if the rising edge for the reference oscillator appears after the one for the signal oscillator and we denote the reference oscillator rising edge with symbol *"⌋⌈"* and signal oscillator rising edge with symbol *"A"*, then one part of the output code would be written as *"A⌋⌈"*. If this sequence continues then the output code would appear as *"A⌋⌈A⌋⌈…"*. The other component of this code consists of the state of the output DFF at the rising edge of the signal oscillator. We combine these two code components by substituting symbol *"A"* by the corresponding state of the DFF. For instance, if the state of the DFF follows the sequence *"110"*, then the combined code would be *"1⌋⌈1⌋⌈0⌋⌈…"*.

When C_{IN} is less than the minimum value allowed, the period of the signal oscillator will be shorter than the period of the reference oscillator and even the feedback signal cannot change this condition. Similarly, if C_{IN} is greater than its maximum allowed value, the signal oscillator period will be longer than the period of the reference oscillator and the feedback signal cannot correct this situation either. These two situations result in a set of error codes that indicate nonlinear

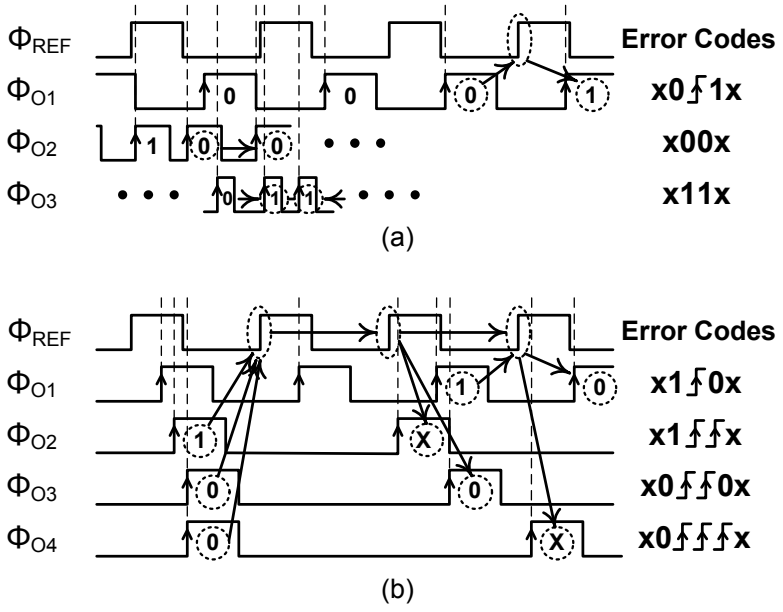


Fig. 6.11. Error codes to detect $C_{IN}<C_{IN,Min}$ situation, (b) error codes to detect a $C_{IN}>C_{IN,Max}$ situation

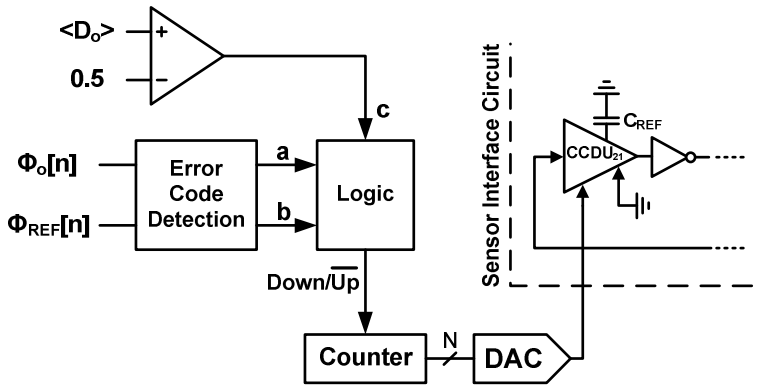
operation.

In Fig. 6.11.a three situations are shown where the signal oscillator period is less than the reference oscillator period. Considering the first situation involving Φ_{REF} and Φ_{O1}, the maximum period of Φ_{O1} is slightly shorter than the period of Φ_{REF}; after a few cycles, two rising edges for Φ_{O1} happens within one cycle of Φ_{REF}. This situation results in the code sequence of *"0_↑1"* representing the missing rising edge for Φ_{REF}. The correct sequence should have been *"0_↑_↑1"*. Another situation depicted by Φ_{O2} and Φ_{O3} captures the situation where the period of signal oscillator is much shorter and two successive rising edges of the signal oscillator may sample one identical digital level of Φ_{REF}. As a result, the sequence of *"11"* or *"00"* will be produced within the output code as specified in Fig. 6.11.a. The appearance of each one of these three error codes confirms that the input C_{IN} is less than the allowed minimum value.

Similarly, Fig. 6.11.b shows four situations when C_{IN} exceeds its maximum allowable value. Considering the first situation involving reference signal Φ_{REF} and signal oscillator Φ_{O1}, even after applying the feedback $D_O=1$, the period of signal oscillator is slightly greater than the period for reference oscillator. After a few cycles, one complete cycle of the reference oscillator will be missed and an error sequence of "*1_↑0*" appears where the correct sequence is *"10"*. Other situations depicted in Fig. 6.11.b corresponding to C_{IN} being much greater than the upper bond is captured by signals Φ_{O2}, Φ_{O3}, and Φ_{O4}. As the period of the signal oscillator increases compared to the period of the reference oscillator, the number of missed cycles of the reference oscillator increases as well. In much the same way as described for the previous code, error codes *"1_↑_↑"*, *"0_↑_↑0"*, and *"0_↑_↑_↑"* can be used to identify the nonlinear situations corresponding to Φ_{O2}, Φ_{O3}, and Φ_{O4}. It can be concluded that the input capacitance, C_{IN}, is out of range as soon as any one of these codes is detected.

6.3.3. The Algorithm to Tune for the Proper $C_{REF,EQV}$

The initial capacitance reference level for different sensors might be different; also, the phase difference between the two ring oscillators can change due to either transistor mismatches or aging over time. To avoid a trimming



(a)

a	b	c	Down/$\overline{Up}$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
~~1~~	~~1~~	~~0~~	**Undefined**
~~1~~	~~1~~	~~1~~	**Undefined**

(b)

Fig. 6.12. (a) The circuit to implement the tuning algorithm, (b) the truth table for the logic block in part (a)

procedure after fabrication and to take full advantage of a cheap digital CMOS process, the control code developed in the previous section can be adopted to tune the bias voltage for $CCDU_{21}$ (delay cell connected to the physical reference capacitor C_{REF}). This tuning process will be used to establish the appropriate equivalent reference capacitance level $C_{REF,EQV}$ for an unknown sensor element and to enable process and mismatch errors to be compensated for.

As the output, $\langle D_O \rangle$, ranges from 0 to 1 in some fractional value, it is appropriate to select the mid-range value of 0.5 to correspond to the desired reference level to maximize the dynamic range of circuit. On start-up, if the output is less than 0.5, the bias voltage of $CCDU_{21}$ should be increased to decrease the magnitude of $f_{21}(V_B)$ in Eqns. (6.43) – (6.45) and this in turn causes a decrease in $C_{REF,EQV}$. On the other hand if the output is greater than 0.5, the bias voltage for $CCDU_{21}$ should be decreased to increase $C_{REF,EQV}$. During the comparison, the

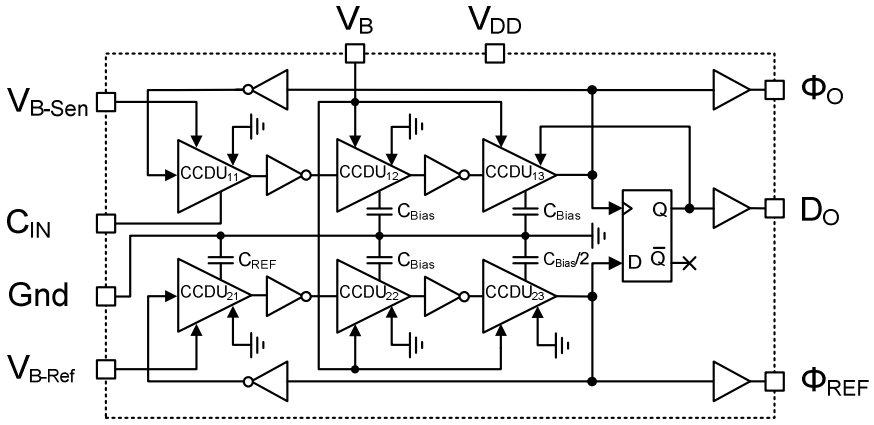


Fig. 6.13. The complete diagram of the time-mode delta-sigma interface

error codes described in the previous section are observed in real-time. If any one of the seven error codes of Fig. 6.11 is detected, depending on which errors are detected, the bias voltage for $CCDU_{21}$ is altered in the appropriate direction such that the output of the sensor interface circuit is set to 0.5. During normal sensing operation, the error codes are constantly monitored to see if the data remains valid.

In Fig. 6.12.a a block diagram capturing the essence of the tuning algorithm is shown. The error code detection block checks the oscillator outputs to see if an error has occurred (see Fig. 6.11). If any of the errors listed in Fig. 6.11.a or 6.11.b occur, the output bit flag *a* or *b* will be set to “1”. These two flag bits and the output of the comparator *c* are forwarded to a logic block whose truth table is listed in Fig. 6.12.b. Due to the nature of the output error codes, the situation when both *a* and *b* are set to “1” is undefined and should never happen. The output of the logic block is then used to set the proceeding counter to count up or down, depending on the action required, which directly alters the bias voltage of $CCDU_{21}$ through the DAC thereby establishing desired reference capacitance level.

6.4. Experimental Results

The final interface circuit, as illustrated in Fig. 6.13, is designed and implemented in 1-V, 90-nm ST CMOS technology. Transistor dimensions for all circuits are revealed in Appendix B. To satisfy Eqn. (6.30), an identical bias

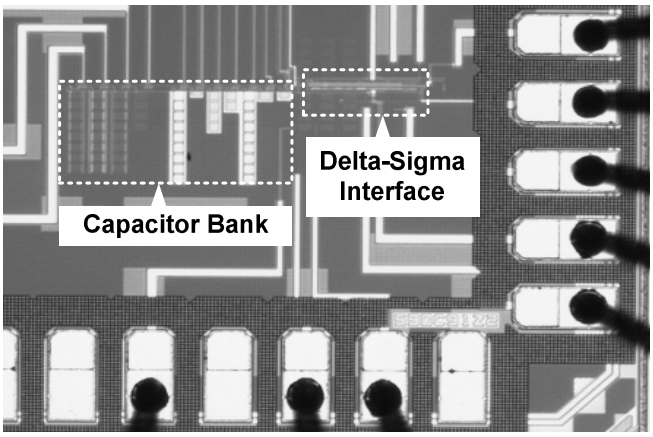
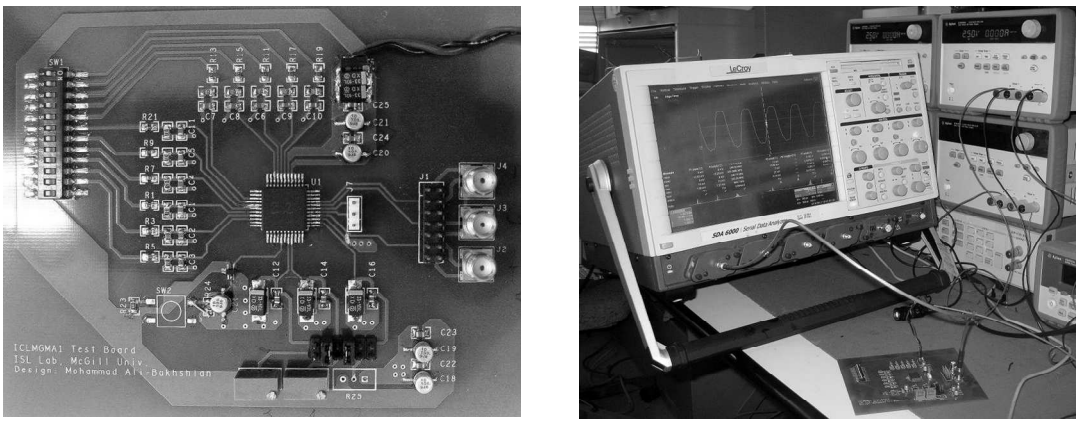


Fig. 6.14. The microphotograph of the implemented delta-sigma interface

voltage is used to bias $CCDU_{12}$, $CCDU_{22}$, $CCDU_{13}$, and $CCDU_{23}$. Voltage $V_{B\text{-}Sen}$ is used to control $CCDU_{11}$ in order to adjust the sensitivity of the circuit. $CCDU_{21}$ is controlled by $V_{B\text{-}Ref}$, the voltage responsible to establish the equivalent reference capacitance as explained earlier. To implement the control routines, Φ_O and Φ_{REF} are taken out of the chip through buffers. As explained earlier, these outputs will be used to detect error codes declaring the non-linear performance of the circuit.

C_{REF} and C_{Bias} capacitors have been implemented using 0.5 pF fringe-capacitors; also, a bank of capacitors has been implemented on-chip consisting of 12.5 fF, 25 fF, 50 fF, 100 fF, 200 fF, 400 fF, 800 fF, 1 pF, 2 pF, 4 pF, and 7 pF fringe-capacitors. Depending on the test, a combination of these capacitors will be applied to the input pin C_{IN}. Generally, the test conditions will consist of one



(a) (b)

Fig. 6.15. (a) The board designed to test the prototype, (b) the test setup

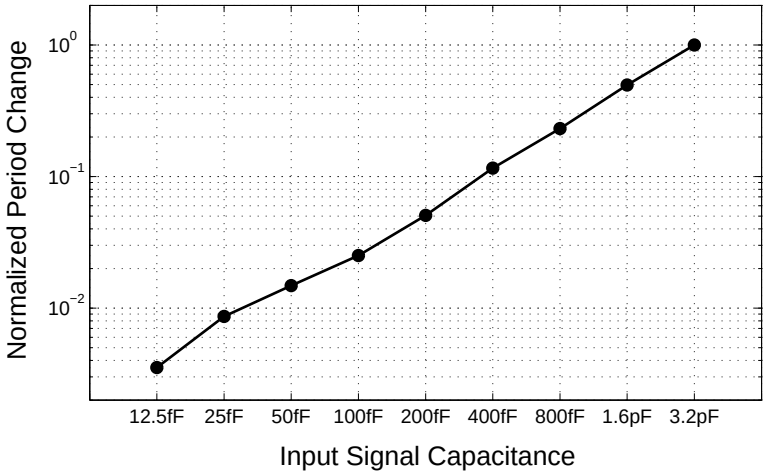


Fig. 6.16. The capacitor profile of the implemented capacitor bank.

input bias capacitor of values 0 pF, 1 pF, 2 pF, 4 pF or 7 pF together with some combination of the remaining capacitors called the signal capacitors. The signal capacitor components alter the input capacitance with respect to the input bias capacitance level (i.e. the signal with respect to a bias level). The sensor interface circuit should adapt $C_{REF,EQV}$ such it equals the input bias capacitance level. A microphotograph of the die is shown in Fig. 6.14 and it occupies an area of 120 µm x 20 µm including the output buffers.

The fabricated prototype was mounted on a customized test board as shown in Fig. 6.15.a. Each capacitor in the capacitor bank was individually characterized with respect to the open circuit situation whereby no capacitance was connected to the input pin C_{IN}. This was conducted by measuring the period of the signal oscillator. According to Eqns. (6.12)-(6.17), the change in the oscillation period is a linear function of the input capacitance C_{IN}. Using a *Le Croy* digital scope (model *SDA-6000*), shown in Fig. 6.15.b, the oscillation period for 10,000 cycles of Φ_O was measured and averaged to extract a measure for the assessment of the actual capacitance values realized on-chip. By normalizing the results, the plot in Fig. 6.16 was derived. Lines have been drawn between each data point for ease of illustration. In addition, the x-axis represents the nominal capacitor values or bins drawn on a nonlinear axis for ease of reference. This graph will be considered as the capacitor profile to be measured. Also in Fig. 6.17

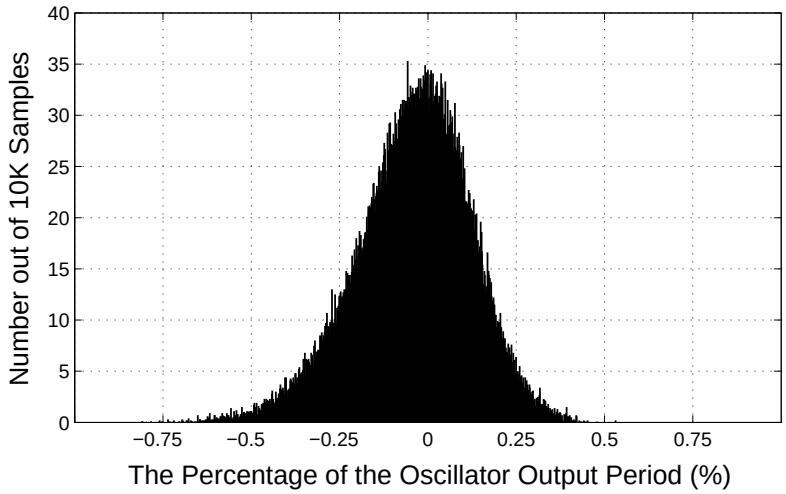


Fig. 6.17. The jitter noise associated with the circuit

and extracted out of 10,000 samples, the distribution percentage for the jitter associated with each oscillating signal relative to the period of oscillation is shown. The distribution pattern is very much Gaussian with a zero mean and a standard deviation of 0.14% of the oscillation period.

To measure the integrated capacitor bank, this time the proposed sensor interface circuit was used. The circuit configuration for test is shown in Fig. 6.18. The voltage at pin V_B is connected to a middle level voltage and the voltage at pins $V_{B\text{-}Sen}$ and $V_{B\text{-}Ref}$ are set using two different DACs. For any input capacitance, the output Φ_O and Φ_{REF} are being forwarded to the control unit to make sure that the interface is working in its linear mode. After assigning a voltage to $V_{b\text{-}Sen}$ through DAC1 and using the tuning algorithm described earlier,

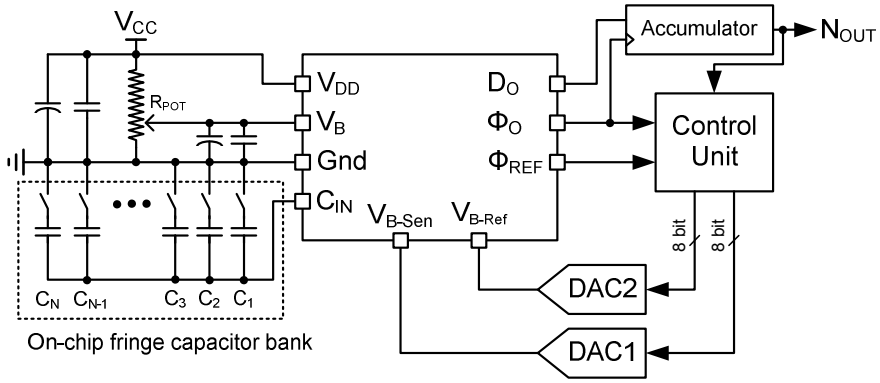


Fig. 6.18. The diagram scheme for the test circuit

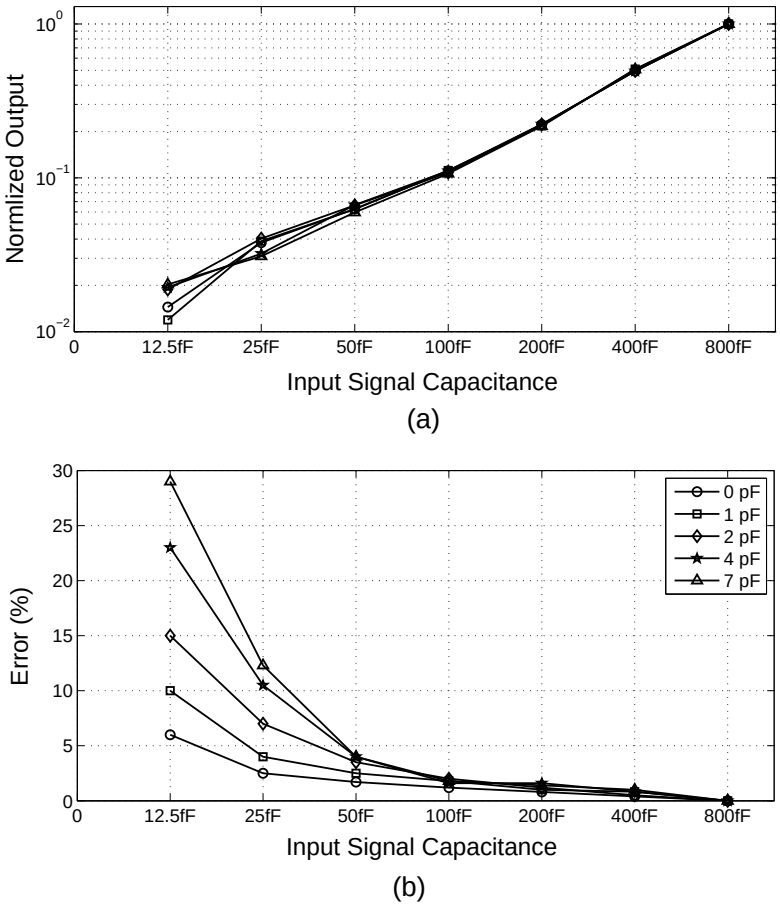


Fig. 6.19. (a) The characterized input C_{IN} between zero and 800 fF with different input bias capacitance, (b) absolute error associated with measurements in part (a).

the control unit modifies the input to DAC2 to set the proper $C_{REF,EQV}$ such that it equals the input bias capacitance level. During this process, any mismatches between the two oscillators will be corrected for, as well. The sensitivity of the sensor interface circuit is modified using DAC1 such that the gain is maximized over some desired capacitance range. In our specific case, an external known signal capacitor is connected in parallel with some input bias capacitance and the output of the sensor interface is monitored such that the slope of the output versus input signal capacitance reaches a desired level. Any modification in the sensitivity of the circuit should be followed by a tuning algorithm.

The data captured by the sensor interface circuit is shown in Fig. 6.19.a in a normalized format. The input bias capacitance was varied between 0 pF, 1 pF, 2 pF, 4 pF and 7 pF while the input signal capacitance was varied from 0 pf to

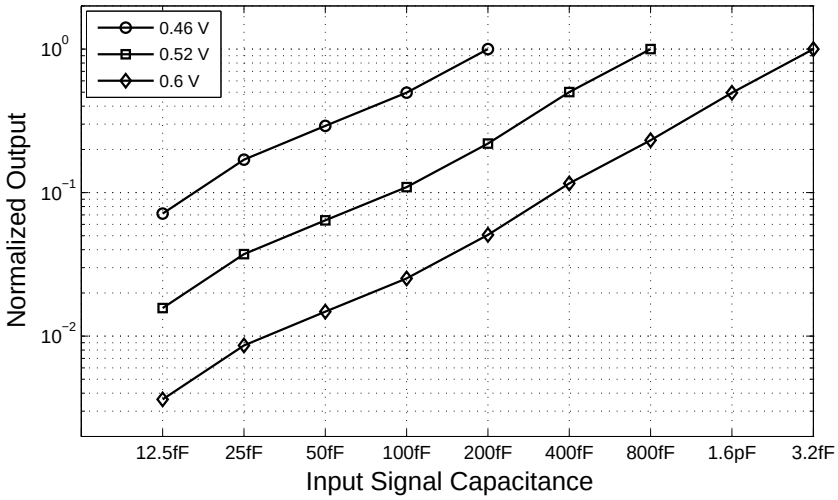


Fig. 6.20. Different ranges for input capacitance measurements for different values of $V_{b\text{-}Sen}$

800 fF. As is evident, the data is very similar for each bias condition, again indicating very good linearity. The relative absolute error in percent was computed with respect to the curve derived earlier through the oscilloscope measurements associated with the oscillation period (Fig. 6.16) and the results are shown in Fig. 6.19.b. Here, the data is identified according to the input bias capacitance level.

For small values of input signal capacitance, the relative error is greatest. It is also evident that the relative error is the largest when the input bias capacitance is at its maximum input value of 7 pF. These results appear to be consistent over several separate sets of measurements. This indicates that the jitter noise strongly affects the lower range of the measurements. This is not too surprising, as the variance of the jitter associated with each oscillator output is directly proportional to the input bias capacitance level as seen in Eqn. (6.39). This implies the accuracy of the sensor interface is better at smaller input bias capacitance levels than larger ones.

To illustrate the ability of the circuit to adjust its input range, the input to DAC2 was changed to modify the sensitivity of the sensor interface circuit. Three specific examples are shown in Fig. 6.20 for different values of $V_{b\text{-}Sen}$. In all cases, the input bias capacitance was fixed to 0 fF and the input signal capacitance was incrementally increased to a maximum value of 3.2 pF. Here it

is evident how the upper bound on the input signal capacitance range was adjusted from 200 fF to 3.2 pF. When these three curves are compared the capacitor profile extracted in Fig. 6.16, some error is evident. Specifically, at very small signal capacitance levels of 12.5 fF, the relative error varies from 2% to 67% as the sensitivity of the sensor interface circuit decreases (i.e., signal range increases).

Like any digital circuit, the static power consumption is a function of its operation frequency. By fixing the sampling frequency at 1 MHz, the power consumption was 110 μWatt. By scaling down the frequency to 300 kHz, the power consumption decreased to 34 μWatt. The fact that the operating frequency is externally tunable by adjusting the bias voltage V_B in Fig. 6.18 enables the power consumption of the sensor interface circuit to be adjustable as well. This, along with the very small silicon footprint, is an important contribution of this sensor interface circuit.

Table 6.1. Summary of features and extracted data for the proposed TM first-order delta-sigma interface circuit

Technology	90-nm ST-CMOS
Power Supply	1 V
Frequency	Up to 8 MHz
Static Power Dissipation	110 μW @ 1MHz
	34 μW @ 300 kHz
CMOS footprint (with buffers)	120 μm × 20 μm
Range	Variable from 0 to 8 pF
Smallest Test Cap. Measured On-Chip	12.5 fF

To make a fair comparison between different designs, all the designs should have been classified under the same category and the design specs for all circuits (such as input range, input frequency and measurement resolution) should be within the same range. Considering the fact that the author has tried to propose a generic tunable interface circuit, to the best of his knowledge, no other tunable designs have been previously reported. Since a conventional tunable circuit needs a large die area and incorporates a high level of complexity, all the

reported designs aim to have a wide input range instead of taking advantage of a tunable structure. However, by comparing the operation principles of some designs reviewed in sections 6.1 (such as the ones reported in [68, 70, 74, and 77]) with those of the time-mode design, some valuable information will be revealed.

The readout circuit of the design reported in [68] is capable of measuring the output of a capacitive sensor with a wide dynamic range as high as 74 dB. It takes a die area as large as 2.8 x 2.3 mm^2 and consumes a power of 10 mWatt. This design is mainly composed of analog blocks and it is not possible to integrate it with a typical sensor on the same wafer. In [70], the authors have dramatically decreased the power consumption, however, the design still includes analog blocks and the area of the implemented prototype is the main disadvantage of the design. These drawbacks are repeated for the generic readout circuit of [77] plus the fact that its SC circuit is quite sensitive to process variations and digital noise. It will be quite a tough job to integrate it with the sensor on the same die. The design reported in [74] is the only design with digital structure. Similar to the proposed time-mode circuit, this circuit takes advantage of capacitance-to-time conversion. To measure the capacitance-controlled output pulse, however, a 10-bit counter and a voltage comparator are incorporated into the design; these additions increase the silicon footprint. In addition, the design operates only on differential input capacitances that limit the application of the circuit to a special class of sensors. Finally, it does not include any calibration routine.

Compared to all the above-mentioned designs and the other ones reviewed in section 6.1, the proposed time-mode interface shows a great advantage over the die area while its power consumption is still one of the lowest reported by now. Furthermore, the digital structure of the time-mode interface is its other advantage that makes it feasible to implement the design on a low-quality silicon wafer alongside the sensor. The resolution of the time-mode interface, however, will be classified within a coarse or mediocre category compared to some of the reviewed design, such as [68]. The preference of the

proposed time-mode design over anyone of the designs of sections 6.1 totally depends on the applications and the fact that what range of input capacitance and output resolution are needed.

It should be noted that the time-mode interface circuit proposed in this chapter is a proof-of-concept for a general time-mode approach. Capacitance-to-time conversion, being tunable, low-power consumption and delta-sigma time-to-digital conversion distinguish this digital structure from other reviewed sensor interfaces. The advantages and abilities of this approach are beyond what presented in this chapter and the design can still be improved in many of its aspects and features.

6.5. Summary

This chapter explores the design and implementation of a semi-digital interface circuit for capacitive sensors. The application is best suited for lab-on-chip applications where a DC or low frequency output capacitance of a sensor is subject to measurement. The design utilizes standard digital cells in association with capacitive-controlled delay units which are synthesizable, portable across different technologies, reconfigurable on-the-fly and easy to calibrate, thereby maximizing time-to-market opportunities. The main advantage of the proposed circuit is its extremely low power consumption, as low as 34 μW, while occupying a very small footprint of 0.0024 mm^2. Due to the digital nature of the design, it can be implemented in a cheap CMOS digital process without the need for component trimming. Process-related mismatches would be corrected using the proposed digital tuning algorithm. Moreover, this design is believed to be capable of being integrated directly on a MEMS wafer thereby providing a fully monolithic digital-output capacitive sensor.

Chapter 7: Conclusion

7.0. Thesis Summary

This thesis investigated the concept of time-mode signal processing (TMSP) as a comprehensive methodology to implement analog signal processing adopting digital building blocks. Various TMSP techniques and circuit components were presented to enhance the processing of time-mode variables, as samples of analog information, in a full digital environment. It was shown by adopting the proposed techniques and components, time-mode variables can be latched, added together or subtracted from each other. All these can be done without any time to voltage/current conversion. By the introduction of an asynchronous approach, the direct integration of a sequence of time-mode inputs was implemented again in a digital environment. This achievement opens the doors for the implementation of processing systems of higher orders than one as it was used to design and implement a second-order digital delta-sigma modulator. Finally, it was shown that the application of TMSP could be extended further to implement a very affordable interface for capacitive sensors for lab-on-chip applications. The extra low power and compact area of the design proves the advantages of TMSP over conventional analog techniques.

A voltage-to-time converter with improved dynamic range, a dual-path time-to-time integrator and a tunable low-power interface for capacitive sensors were designed, fabricated, and tested successfully. A second-order digital delta-

sigma modulator was designed and fabricated as well; however, it failed to operate due to ESD problems.

Digital techniques to implement the addition and subtraction of instantaneous time-mode variables were proposed adopting the new concept of delay interruption. By introducing a new component called switched-voltage-controlled delay unit (SVCDU), the propagation delay of the rising edge at the input of this delay block was controlled by a digital bit; so that, this delay could be either the nominal delay value of the block or infinity. By using two SVCDUs in parallel together with some additional logic, a new component called TLatch was proposed. Adopting the TLatch and applying different propagation delays to each one of the input pair of rising edges, it was possible to latch the time-difference between the input pair of rising edges or combine it with another time-mode variable to perform addition or subtraction between them. Simulation results show the proof of concept for the proposed techniques and components. Also the simulations show that because of digital construction, the design was robust to power supply noise; in addition, the mismatch between the corresponding components in the two paths resulted in a signal independent DC offset at the output.

An Asynchronous approach for direct processing of time-mode variables was introduced. By defining the time-mode variable as the phase difference between the rising edges at the corresponding points of two parallel paths, the TM variable under processing could be manipulated using the SVCDU in each path. Adopting the asynchronous approach, a digital dual-path time-to-time integrator was designed, fabricated and tested in 1.2 V 0.13-um IBM CMOS process. Due to the digital construction, the compensation for the mismatches between the two parallel paths was accomplished easily by tuning the frequencies of two internal ring oscillators. The experimental results confirmed the operation of the proposed SVCDUs, TLatches and the integrator, where the integrator performed with a peak error of 1.5% over full-scale. This circuit is expected to be the basis for other time-mode signal processing circuits like high-order delta-sigma modulators and frequency-selective filter circuits.

The above-mentioned time-to-time integrator was used to implement a digital second-order delta-sigma modulator. By modifying the structure for a previously reported voltage-controlled delay unit, the input dynamic range of the modulator was improved. Experimental results show that for linearity better than ±0.1%, the input dynamic range increased from 22% of the power supply up to 42%. The structure for the digital modulator consists of identical digital unit and for fine-tuning of the design specs, the value specification for different capacitors across the modulator were considered as the design target. Post layout simulation results show that at the average clock frequency of 3.215 MHZ, the maximum output SNDR over a 16 KHz bandwidth was equal to 76.11 dB. The modulator was fabricated in 1.2V 0.13-um IBM CMOS process; however, it was not possible to test the chip due to ESD problems.

A tunable interface circuit for capacitive sensors was designed, fabricated and tested in 1V 90-nm ST CMOS process. Adopting capacitance-to-time conversion it was possible to linearly convert the input capacitance subject to measurement into the phase difference between two rising edges. Adopting TMSP, the converted time-mode variable was quantized through a first-order delta-sigma modulator. The design was done for lab-on-chip application and it was possible to tune it for different range of input capacitance, different sensitivity and power consumption. The main advantage of the proposed circuit is its extremely low power consumption, as low as 34 μW, while occupying a very small footprint of 0.0024 mm^2. Moreover, this design is believed to be capable of being integrated directly on a MEMS wafer thereby providing a fully monolithic digital-output capacitive sensor.

In this thesis, all the designs are constructed from digital circuitry. Hence, these circuits occupy small areas, consume low power and are portable across different technologies. Due to the digital nature of the design, it can be implemented in a cheap CMOS digital process without the need for component trimming. Process-related mismatches would be corrected using the proposed digital tuning algorithms. All the developments are made in search for an alternative to the conventional analog design techniques were the design

constraints for sub-micron CMOS technologies increases as time advances. Similar to any other technique, TMSP is associated with some drawbacks as well; for example, the transient nature of the variable to be processed, i.e. time, can complicates the design of such circuits; also, there is an inherent trade-off between the dynamic range and speed of a TMSP circuit. However, TMSP is a topic and it needs more time to be matured. As time passes, the discovery of more advantages and disadvantages of this technique can help us to make a fair judgment about its applications.

7.1. Future Works

The concept of time-mode signal processing is still new and at this stage of its development, the possibilities seem endless. The work presented in this dissertation offers a foundation for the development of TMSP as a general signal-processing tool, and exemplifies some mixed-signal circuits built from this foundation. Other possibilities to advance and extend this work are:

1- The input to a TMSP circuit is a form of analog information such as voltage, current, capacitance, etc. It is important to be able to process a wide range of input information. To increase the dynamic range for the voltage inputs, the idea proposed in this thesis might be used to extend the input dynamic range. By adopting a complementary input stage, the input dynamic range might be increased to the full range of power supply. Therefore, there is an open avenue for further linearization of the VCDU.

2- Although there are some very good analog designs to implement time amplifiers, the idea presented in this thesis to implement a switched-voltage-controlled delay unit might be used to design a time amplifier with a digital construction. By latching the input time-mode variable at one discharge rate and reading the residual charge across the capacitors inside the TLatch at another discharge rate, shrinkage or expansion of the time-difference between two input digital rising edges can be investigated.

3- Although the test of the fabricated prototype for the second-order delta-sigma modulator failed due to ESD problems, the post-layout simulation results

make a strong motivation to re-fabricate the design together with proper ESD protection.

4- It would be interesting to investigate and formulate the upper limit for the speed of the proposed second-order delta-sigma modulator.

5- Perhaps the greatest contribution of this work is the techniques proposed for the addition and subtraction of time-mode variables. The second-order delta-sigma modulator was a direct result of this contribution. There would be a great research opportunities to conduct a research thesis on the development of modulators of higher orders like cascade 2-1 or 2-2 delta-sigma modulators.

6- The test and verification of a digital design is a mature knowledge that has been dramatically developed during the last years. Considering that all the critical signals in a TMSP circuit are digital rising edges, it might be possible to take advantage of digital test techniques to improve the manufacturing test routines applied to analog designs.

7- A final proposal for future work is to investigate the possibility for the design of a multi-purpose floor plan that consists of a series of identical building blocks such as TLatches, SVCDUs, logic gates, etc. the purpose to design such a floor plane is to investigate the how the connection between these blocks can be re-arranged for different applications. One valuable research avenue is to exhaust the search for a synthesizable approach for the implementation of TMSP circuits.

References

[1] A. J. Annema, B. Nauta, R. Van Langevelde, and H. Tuinhout, “Analog Circuits in Ultra-Deep-Submicron CMOS,” IEEE Journal of Solid-State Circuits, Vol. 40, No. 1, pp.: 132-143, Jan. 2005

[2] P. Basedau, Q. Huang, O. Paul, and H. Baltes, “Isolating Analog Circuits from Digital Interferences,” International Conference on Solid-State and Integrated Circuit Technology, pp.: 656 – 658, Oct. 1995

[3] C. Taillefer; “Analog-to-Digital Conversion via Time-Mode Signal Processing,” Ph.D. Thesis, McGill University, Aug. 2007

[4] G. Kim, M. K. Kim, B. S. Chang, and W. Kim; “A Low-Voltage, Low-Power CMOS Delay Element,” IEEE Journal of Solid-State Circuits, Vol. 31, Issue: 7, pp.: 966-971, July 1996

[5] J. G. Maneatis; “Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques,” IEEE Transactions on Solid-State Circuits, Vol. 31, Issue: 11, Nov. 1996

[6] W. Rhee; “A Low Power, Wide Linear-Range CMOS Voltage-Controlled Oscillator,” IEEE International Symposium on Circuits and Systems, Vol. 2, pp. 85-88, Jun. 1998

[7] N. R. Mahapatra, S. V. Garimella, A. Tareen; “An Empirical and Analytical Comparison of Delay Elements and a New Delay Element Design,” Proceeding of the IEEE Computer Society Workshop on VLSI, pp. 81-86, Apr. 2000

[8] D. A. Badillo, S. Kiaei; “Comparison of Contemporary Ring Oscillators,” IEEE Radio Frequency Integrated Circuits Symposium, pp. 281-284, Jun 2004

[9] M. El-Hage, F. Yuan; “An Overview of Low-Voltage VCO Delay Cells and a Worst-Case Analysis of Supply Noise Sensitivity,” Canadian Conference on Electrical and Computer Engineering, Vol. 3, pp 1785-1788, May 2004

[10] H. Pekau, A. Yousif, J. W. Haslett; “A CMOS Integrated Linear Voltage-to-Pulse-Delay-Time Converter for Time Based Analog-to-Digital Converters,” IEEE International Symposium on Circuits and Systems, pp. 2373-2376, May 2006

[11] C. Taillefer, G. W. Roberts; “Delta–Sigma A/D Conversion Via Time-Mode Signal Processing,” IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 56, Issue: 9, pp.:1908 – 1920, Sep. 2009

[12] A. M. Abas, A. Bystrov, D. J. Kinniment, O. V. Maevsky, G. Russell, and A. V. Yakovlev; “Time Difference Amplifier,” Electronics Letters, Vol. 38, Issue: 23, pp.: 1437-1438, Nov. 2002

[13] M. Oulmane, G. W. Roberts; “Digital domain time amplification in CMOS process,” International Conference on Solid-State and Integrated Circuits Technology, Vol. 2, pp.:1416 – 1420, Oct. 2004

[14] G. C. Temes, R. Schreier, S. R. Norsworthy; “Understanding Delta-Sigma Data Converters”, Wiley-IEEE press, Oct. 1996

[15] H. Berndt, R. Richter, H. J. Jentschel; “A 100 Ms/sec, 8th-order Quadrature Sigma-Delta ADC for Complex-If Signal Digitization in a Wideband-IF Sampling Receiver,” International Conference on ASIC, Vol. 1, pp. 669 – 672, Oct. 2003

[16] Y. Geerts, M. S. J. Steyaert, W. Sansen; “A High-Performance Multibit ΔΣ CMOS ADC,” IEEE Journal of Solid-State Circuits, Vol. 35, Issue: 12, pp. 1829 – 1840, Dec. 2000

[17] M. Hovin, A. Olsen, T. S. Lande; Toumazou, C.; “Delta-sigma modulators using frequency-modulated intermediate values,” IEEE Journal of Solid-State Circuits, Vol. 32, Issue:1, pp.: 13 – 22, Jan 1997

[18] U. Wismar, D. Wisland, P. Andreani; “A 0.2V 0.44 uW 20 kHz Analog to Digital Sigma-Delta Modulator with 57 fJ/conversion FoM,” Proceedings of the 32nd European Solid-State Circuits Conference, ESSCIRC, pp.: 187 – 190, Sep. 2006

[19] J. Kim; T. K. Jang; Y. G. Yoon; “Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter,” IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 57, Issue: 1, pp.: 18-30, Jan 2010

[20] M. Z. Straayer, M. H. Perrott; “A 10-bit 20 MHz 950 MHz CT ΔΣ ADCwith a 5-bit noise-shaping VCO-based quantizer and DEM circuitin 0.13 u CMOS,” in Proc. IEEE Int. Conf. VLSI Des, pp.: 246–247, Jan. 2007

[21] M. Z. Straayer, M. H. Perrott; “A 12-bit, 10 MHz bandwidth, continuous-time ΔΣ ADC with a 5-bit, 950 MS/s VCO-based quantizer,” IEEE J. Solid-State Circuits, Vol. 43, Issue: 4, pp. 805–814, Apr. 2008

[22] K. H. Cheng, Y. L. Lo; “A Fast-Lock Wide-Range Delay-Locked Loop Using Frequency-Range Selector for Multiphase Clock Generator,” IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 54, Issue: 7, pp.:561-565, July. 2007

[23] M. J. E. Lee, W. J. Dally, T. Greer, Hiok-Tiaq Ng, R. Farjad-Rad, J. Poulton, R. Senthinathan; “Jitter transfer characteristics of delay-locked loops - theories and design techniques,” IEEE Journal of Solid-State Circuits, Vol. 38, Issue 4, pp.:614–621, Apr. 2003

[24] J. G. Maneatis; “Low-jitter process-independent DLL and PLL based on self-biased techniques,” IEEE Journal of Solid-State Circuits, Vol. 31, Issue 11, pp.:1723–1732, Nov. 1996

[25] J. G. Kenney, D. Dalton, E. Evans, M. H. Eskiyerli, B. Hilton, D. Hitchcox, T. Kwok, D. Mulcahy, C. McQuilkin, V. Reddy, S. Selvanayagam, P. Shepherd, W. S. Titus, L. DeVito; "A 9.95-11.3-Gb/s XFP Transceiver in 0.13-um CMOS," IEEE Journal of Solid-State Circuits, Vol. 41, Issue 12, pp.: 2901–1910, Dec. 2006

[26] H. H. Chang, R. J. Yang, S. I. Liu; "Low jitter and multirrate clock and data recovery circuit using a MSADLL for chip-to-chip interconnection," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 51, Issue: 12, pp.: 2356-2364, Dec. 2004

[27] L. Rodoni, G. Von Buren, A. Huber, M. Schmatz, H. Jacke; "A 5.75 to 44 Gb/s quarter rate CDR with data rate selection in 90 nm bulk CMOS," IEEE Journal of Solid-State Circuits, Vol. 44, Issue: 7, pp.: 1927-1941, July 2009

[28] B. Razavi; "Design of Analog CMOS Integrated Circuits", McGraw Hill Press, Oct 2000

[29] A. E. Stevens, R. P. Van Berg, J. Van Der Spiegel, and H. H. Williams; "A time-to-voltage converter and analog memory for colliding beam detectors," IEEE Journal of Solid-State Circuits, Vol. 24, Issue: 6, pp. 1748-1752, Dec. 1989

[30] E. Raisanen-Ruotsalainen, T. Rahkonen, and J. Kostamovaara; "A time digitizer based on time-to-voltage conversion," in Proc. 40th Midwest Symposium on Circuits and Systems, pp. 197-200, Aug. 1997

[31] R. L. Sumner; "Apparatus and method for measuring time intervals with very high resolution," U.S. Patent 6 137 749, Oct. 24, 2000

[32] D. M. Santos, S. F. Dow, M. E. Levi; "A CMOS delay locked loop and sub-nanosecond time-to-digital converter chip," IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, pp.: 289–291, Oct. 1995

[33] F. Baronti, L. Fanucci, D. Lunardini, R. Roncella, R. Saletti, R.; “A high-resolution DLL-based digital-to-timeconverter for DDS applications,” IEEE International Frequency Control Symposium and PDA Exhibition, pp.: 649–653, 2002

[34] C. T. Gray, W. Liu, W. A. M. Van Noije, T. A. Hughes, Jr., R. K. Cavin; “A sampling technique and its CMOS implementation with 1 Gb/s bandwidth and 25 ps resolution," IEEE Journal of Solid-State Circuits, Vol. 29, Issue: 3, pp.: 340-349, Mar. 1994

[35] P. Dudek, S. Szczepanski, J. V. Hatfield; “A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line,” IEEE Journal of Solid-State Circuits, Vol. 35, Issue 2, pp.: 240–247, Feb. 2000

[36] Y. Jianjun, F. F. Dai, R. C. Jaeger; “A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13-um CMOS Technology,” IEEE Journal of Solid-States Circuits, Vol. 45 , Issue: 4, pp.: 830 – 842, Apr. 2010

[37] A. H. Chan, G. W. Roberts; “A jitter characterization system using a component-invariant Vernier delay line,” IEEE Transactions on Very Large Scale Integration(VLSI) Systems, Vol. 12, Issue: 1, pp.: 79-95, Jan. 2004

[38] P. Chen, C. Chen, J. C. Zheng, Y.S. Shen; “A PVT Insensitive Vernier-Based Time-to-Digital Converter With External Input Range and High Accuracy,” IEEE Transactions on Nuclear Science, Vol. 54, Issue: 2, pp.: 294-302, Apr. 2007

[39] L. Yue, U. Vollenbruch, C. Yangjian, C. Wicpalek, L. Maurer, Z. Boos, R. Weigel; “Multi-stage pulse shrinking time-to-digital converter for time interval measurements,” European Microwave Integrated Circuit Conference, pp.: 267–270, Oct. 2007

[40] F. M. Gardner; "Charge-pump phase-locked loops," IEEE Trans. on Communications, Vol. COMM-28, pp.: 1849-1858, Nov. 1980

[41] R. B. Staszewski, C. M. Hung, D. Leipold, P. T. Balsara; "A first multigigahertz digitally controlled oscillator for wireless applications," IEEE

Trans. on Microwave Theory and Techniques, Vol. 51, Issue: 11, pp.: 2154-2164, Nov. 2003

[42] C. M. Hung, R. B. Staszewski, N. Barton, M.-C. Lee, D. Leipold; "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," IEEE Journal of Solid-State Circuits, Vol. 41, Issue: 5, pp.: 1160-1170, May 2006

[43] R. B. Staszewski, D. Leipold, K Muhammad, P. T. Balsara; "Digitally controlled oscillator (DCO)-based architecture for RF frequency synthesis in a deep-submicrometer CMOS process," IEEE Trans. on Circuits and Systems II, Vol. 50, Issue: 11, pp.: 815-828, Nov. 2003

[44] R. B. Staszewski, K. Muhammad, D. Leipold, et al.; "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 39, Issue: 12, pp.: 2278-2291, Dec. 2004

[45] R. B. Staszewski, J. Wallberg, S. Rezeq, C.-M. Hung, 0. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, D. Leipold; "All-digital PLL and transmitter for mobile phones," IEEE Journal of Solid-State Circuits, Vol. 40, issue: 12, pp.: 2469-2482, Dec. 2005

[46] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, P. T. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," IEEE Trans. on Circuits and Systems II, Vol. 53, Issue: 3, pp.: 220-224, Mar. 2006

[47] R. B. Staszewski, K. Waheed, S. Vemulapalli, F. Dulger, J. Wallberg, C. M. Hung, O. Eliezer; “Spur-free all-digital PLL in 65 nm for mobile phones," IEEE International Solid-State Circuits Conference, pp.: 52-54, Feb. 2011

[48] C.-M. Hsu et al.; “A low-noise, wide-BW 3.6GHz digital ΔΣ fract.-N frequency synthesizer with a noise-shaping TDC and quantization noise cancellation,” ISSCC Dig. Tech. Papers, pp.: 340-341, Feb. 2008

[49] H.-H. Chang et al.; “A fractional spur-free ADPLL with loop-gain calibration and phase-noise cancellation for GSM/GPRS/EDGE,” IEEE International Solid-State Circuits Conference, pp.: 200-201, Feb. 2008

[50] C. Weltin-Wu et al.; “A 3GHz fractional-N all-digital PLL with precise time-todigital converter calibration and mismatch correction,” IEEE International Solid-State Circuits Conference, pp. 344-345, Feb. 2008

[51] C. Weltin-Wu et al.; “A 3.5GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation,” IEEE International Solid-State Circuits Conference, pp.: 468-469, Feb. 2010

[52] V. Ravinuthula, J.G. Harris; “Time-Based Arithmetic using Step Functions,” IEEE International Symposium on Circuits and Systems, pp.: 305-308, May 2004

[53] C. Ying, P. Leroux, W. De Cock, M. Steyaert; “A 1.7mW 11b 1–1–1 MASH ΔΣ time-to-digital converter,” IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp.: 480–482, Feb. 2011

[54] K. Martin; “Digital Integrated Circuit Design” Oxford University Press, Sep. 1999

[55] B.K. Swann, B.J. Blalock, L.G. Clonts, D.M. Binkley, J.M. Rochelle, E. Breeding, K.M. Baldwin; “100-ps time-resolution CMOS time-to-digital converter for positron emission tomography imaging applications,” IEEE Journal of Solid-State Circuits, Vol. 39, Issue: 11, pp.: 1839–1852, Nov. 2004

[56] J.A. Tierno, A.V. Rylyakov, D.J. Friedman; “A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI,” IEEE Journal of Solid-State Circuits, Vol. 43, Issue: 1, pp.: 42–51, Jan. 2008

[57] G.W. Roberts, M. Ali-Bakhshian; “A Brief Introduction to Time-to-Digital and Digital-to-Time Converters,” IEEE Transaction on Circuits and Systems II: Express Briefs, Vol. 57, Issue: 3, Mar 2010

[58] L. Hernández, E. Prefasi; “Continuous time ΣΔ modulator based on digital delay loop and time quantization,” Electronics Letters, Vol. 46, Issue: 25, pp.: 1655–1656, Dec 2010

[59] K., Papathanasiou; A., Hamilton; "Pulse based signal processing: VLSI implementation of a Palmo filter," IEEE International Symposium on Circuits and Systems, 1996., Vol.1, pp.: 270-273, May 1996

[60] L., Hernandez; J., Fernandez; E., Prefasi; S., Paton; "A time encoded decimation filter for noise shaped power DACs", Proceedings of 2010 IEEE International Symposium on Circuits and Systems, pp.: 289-292, May 2010

[61] M. M., Guttman; G. W., Roberts; “Sampled-data IIR filtering using time-mode signal processing circuits,” IEEE International Symposium on Circuits and Systems, ISCAS 2009, pp.: 2285–2288, May 2009

[62] F. Marvasti; “Non-Uniform Sampling (Theory and Practice),” Kluwer Academics/Plenum Publishers, 2001

[63] L. K. Baxter; “Capacitive Sensors—Design and Applications,” New York: IEEE Press, 1997

[64] H. Kulah, J. Chae, N. Yazdi, K. Najafi; “Noise analysis and characterization of a sigma-delta capacitive microaccelerometer,” IEEE Journal of Solid-State Circuits, Vol. 41 , Issue: 2, Feb 2006

[65] N. Yazdi, H. Kulah, K. Najafi; “Precision readout circuits for capacitive microaccelerometers,” IEEE Sensors Proc., Vol. 2, pp.: 28-31, Oct. 2004

[66] D. M. G. Preethichandra, K. Shida; “A simple interface circuit to measure very small capacitance changes in capacitive sensors,” IEEE Transactions on Instrumentation and Measurement, Vol. 50, Issue: 6, pp.: 1583-1586, Dec. 2001

[67] J. O'Dowd, A. Callanan, G. Banarie; E. Company-Bosch; “Capacitive sensor interfacing using sigma-delta techniques,” IEEE Sensors Proc., Nov. 2005

[68] W. F. Lee, P. K. Chan; “A Capacitive-Based Accelerometer IC Using Injection-Nulling Switch Technique,” IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 55, Issue 4, pp.: 980-989, May 2007

[69] K. Takahata, A. DeHennis, K. D. Wise, Y. B. Gianchandani; “A wireless microsensor for monitoring flow and pressure in a blood vessel utilizing a dual-inductor antenna stent and two pressure sensors,” 17th IEEE International Conference on Micro Electro Mechanical Systems (MEMS), pp.: 216-219, 2004

[70] P. D. Dimitropoulos, D. P. Karampatzakis, G. D. Panagopoulos, G. I. Stamoulis; “A low-power/low-noise readout circuit for integrated capacitive sensors,” IEEE Sensors Journal, Vol. 6, Issue: 3, pp.: 755-769, Jun. 2006

[71] M .Ylimaula, M. Aberg, J. Kiihamaki, H. Ronkainen; “Monolithic SOI-MEMS capacitive pressure sensor with standard bulk CMOS readout circuit,” Proceedings of the 29th European Solid-State Circuits Conference (ESSCIRC), pp.: 611-614, Sept. 2003

[72] Xiaojing Shi; H. Matsumoto, K. Murao; “A high-accuracy digital readout technique for humidity sensor,” IEEE Transactions on Instrumentation and Measuremen, Vol. 50, Issue: 5 , pp.:1277-1282, Oct. 2001

[73] W. Jiangfeng, G. K. Fedder, L. R. Carley; “A low-noise low-offset capacitive sensing amplifier for a 50-µg/√Hz monolithic CMOS MEMS accelerometer”, IEE Journal of Solid-State Circuits, Vol. 39, pp.: 722-730, May 2004

[74] T. G. Constandinou, J. Georgiou, C. Toumazou; “Micropower front-end interface for differential-capacitive sensor systems,” Electronics Letters, Vol. 44, Issue: 7, pp.: 470-472, Mar 2008

[75] J. A. Geen, S. J. Sherman, J. F. Chang, S. R. Lewis; “Single-chip surface micromachined integrated gyroscope with 50°/h Allan deviation,” IEEE Journal of Solid-State Circuits, Vol. 37, Issue: 12, pp.: 1860-1866, Dec. 2002

[76] T. Sutory, Z. Kolka; “C-V Characterization of Nonlinear Capacitors using CBCM Method,” 14th International Conference on Mixed Design of Integrated Circuits and Systems, pp.: 501-505, Jun 2007

[77] W. Bracke, P. Merken, R. Puers, C. Van Hoof; “Ultra-Low-Power Interface Chip for Autonomous Capacitive Sensor Systems,” IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 54, Issue: 1, pp.: 130-140, Jan 2007

[78] M. Ali-Bakhshian, G.W. Roberts; “Digital Storage, Addition and Subtraction of Time-Mode Variables,” Electronics Letters, Vol.:47, Issue:16, pp.:910-911, Aug 2011

[79] M. Ali-Bakhshian, G.W. Roberts; “A Digital Implementation of a Dual-Path Time-to-Time Integrator,” IEEE Transaction on Circuits and Systems I: Regular Papers, Apr 2012

[80] M. Ali-Bakhshian, G. W. Roberts; “A Semi-Digital Interface for Capacitive Sensors,” IEEE International Symposium on Circuits and Systems, ISCAS, Taipei, Taiwan, May 2009

Appendix A

Appendix A offers all the circuit diagrams and the transistor dimensions required to reproduce the design presented for the implementation of the digital second order delta-sigma modulator. As explained in Chapter 5, this design includes all the sub-blocks needed for the implementation of the time-to-time integrator presented in Chapter 4.

Circuit Diagrams and Block Connections

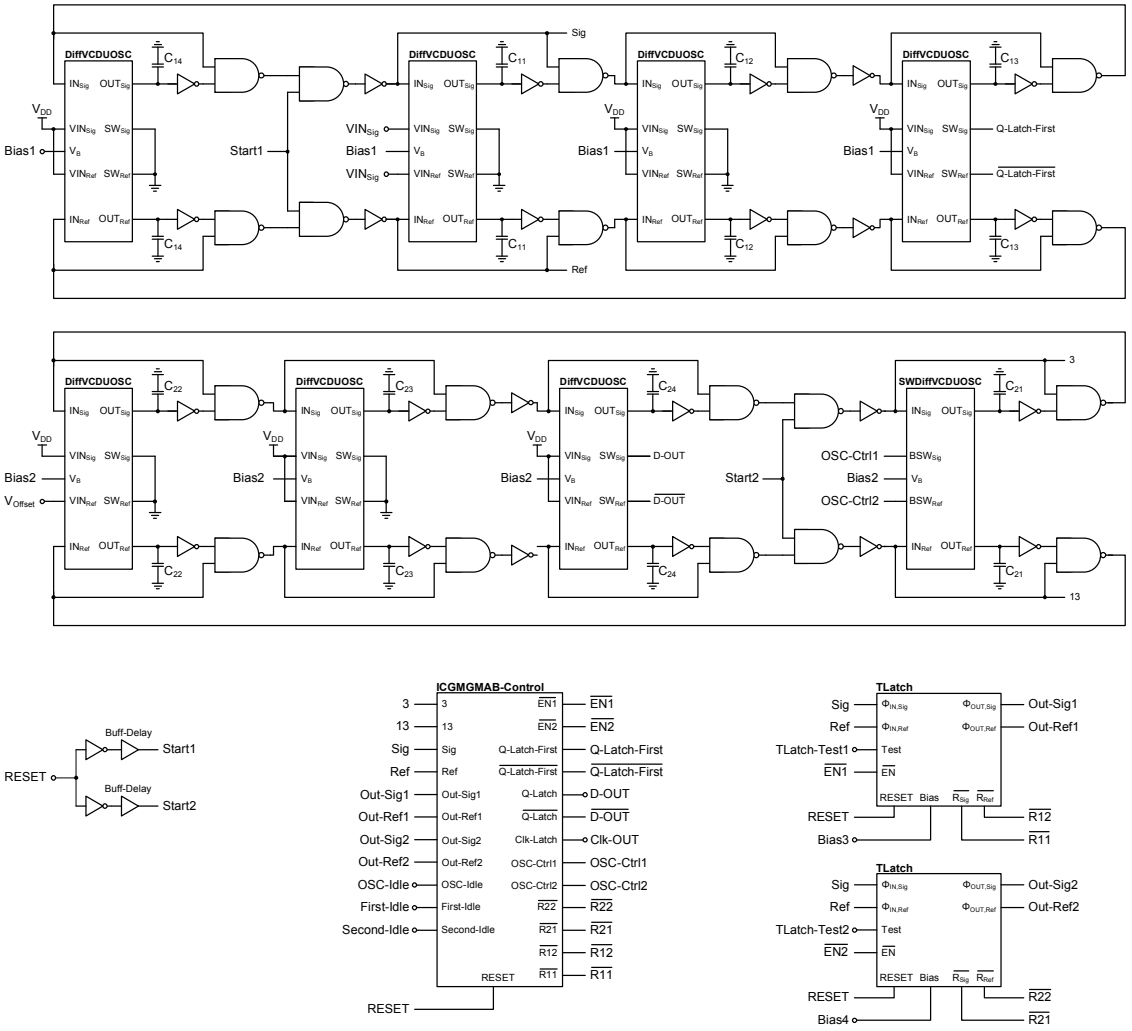


Fig. A.1. Top-level schematic of the digital second order delta-sigma modulator

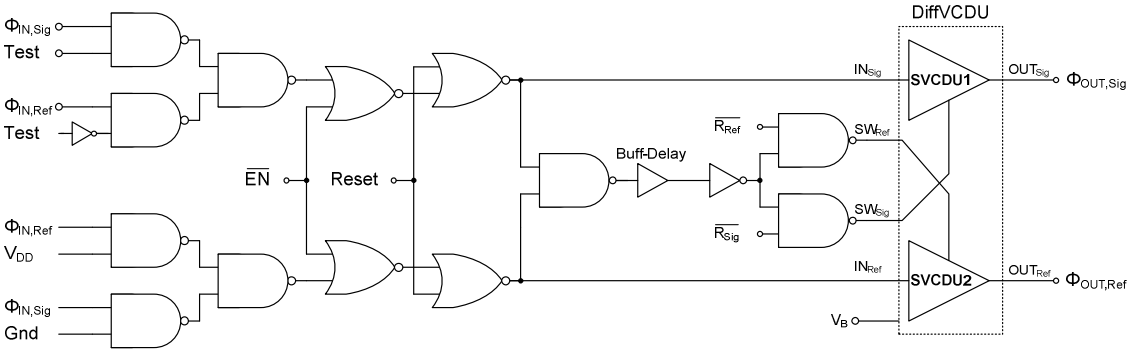


Fig. A.2. The circuit diagram for the block “TLatch” shown in Fig. A.1

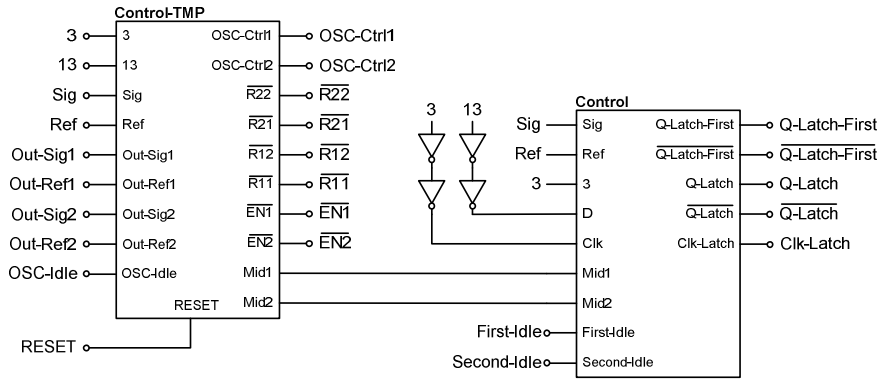


Fig. A.3. The circuit diagram for the block “ICGMGMAB-Control” shown in Fig. A.1

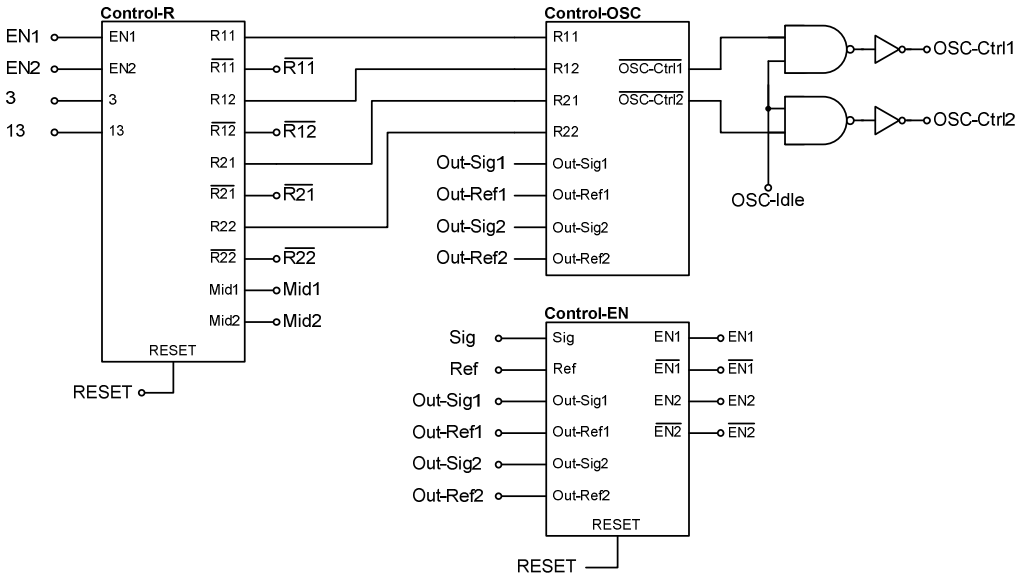


Fig. A.4. The circuit diagram for the block “Control-TMP” shown in Fig. A.3

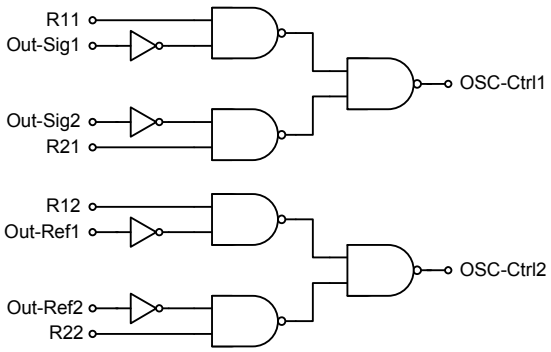


Fig. A.5. The circuit diagram for the block “Control-OSC” shown in Fig. A.4

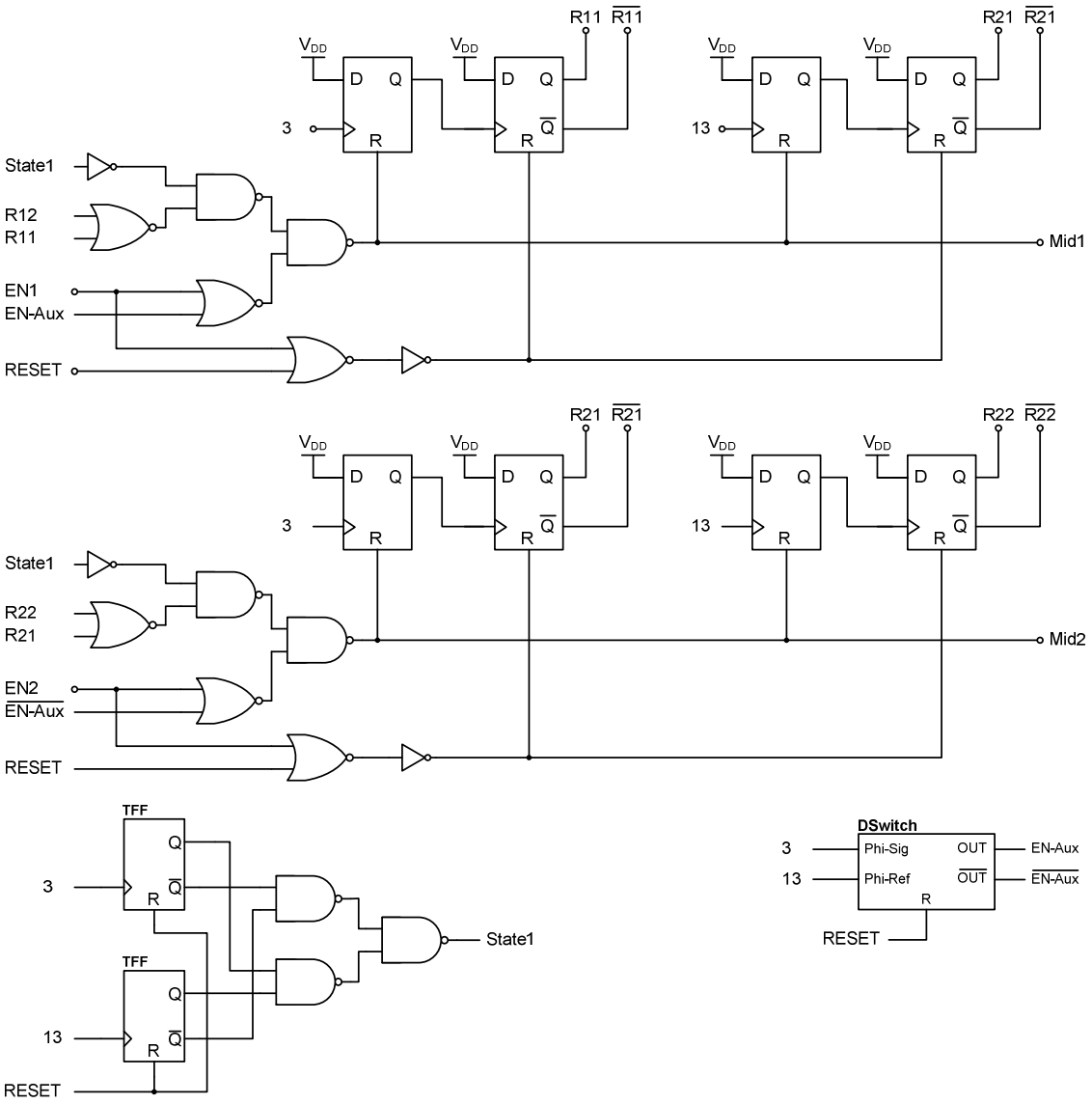


Fig. A.6. The circuit diagram for the block “Control-R” shown in Fig. A.4

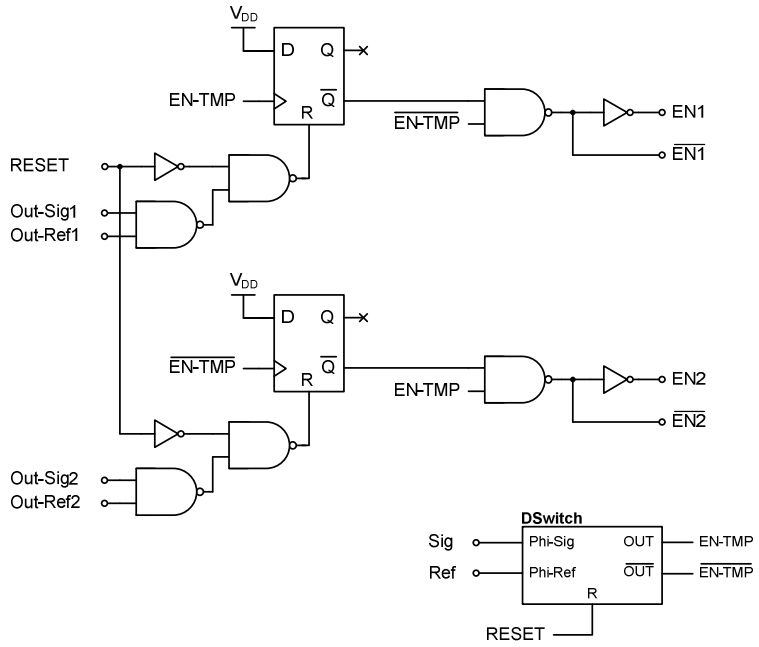


Fig. A.7. The circuit diagram for the block “Control-EN” shown in Fig. A.4

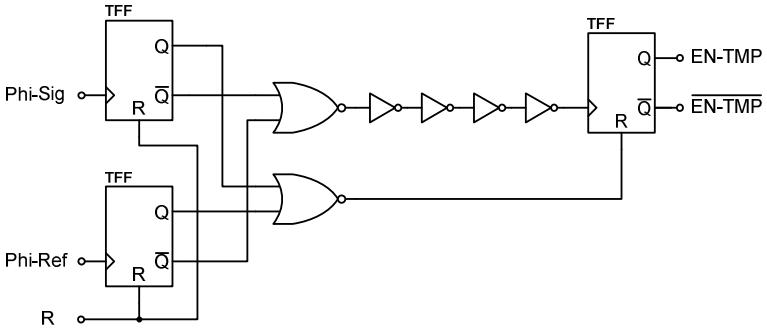


Fig. A.8. The circuit diagram for the block “DSwitch” shown in Fig. A.6 and Fig. A.7

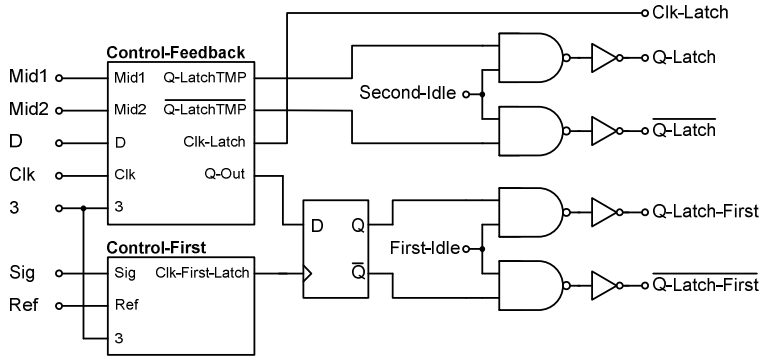


Fig. A.9. The circuit diagram for the block “Control” shown in Fig. A.3

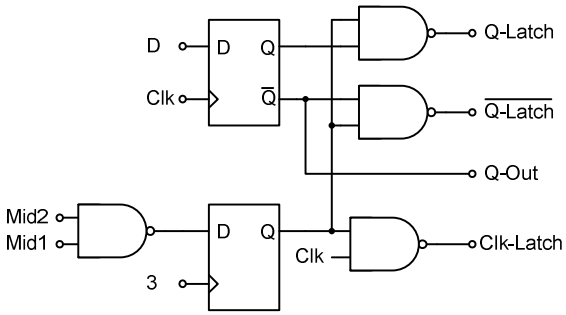


Fig. A.10. The circuit diagram for the block “Control-Feedback” shown in Fig. A.9

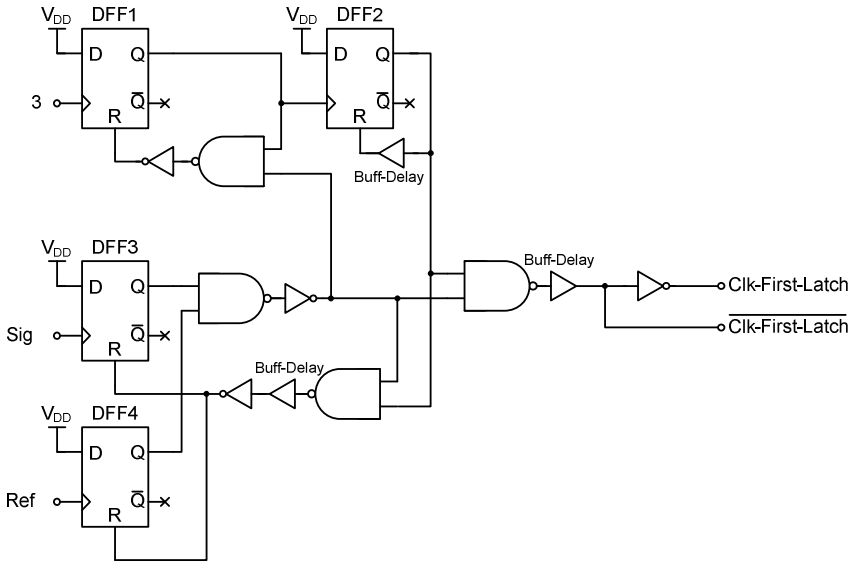


Fig. A.11. The circuit diagram for the block “Control-First” shown in Fig. A.9

Transistor Dimensions

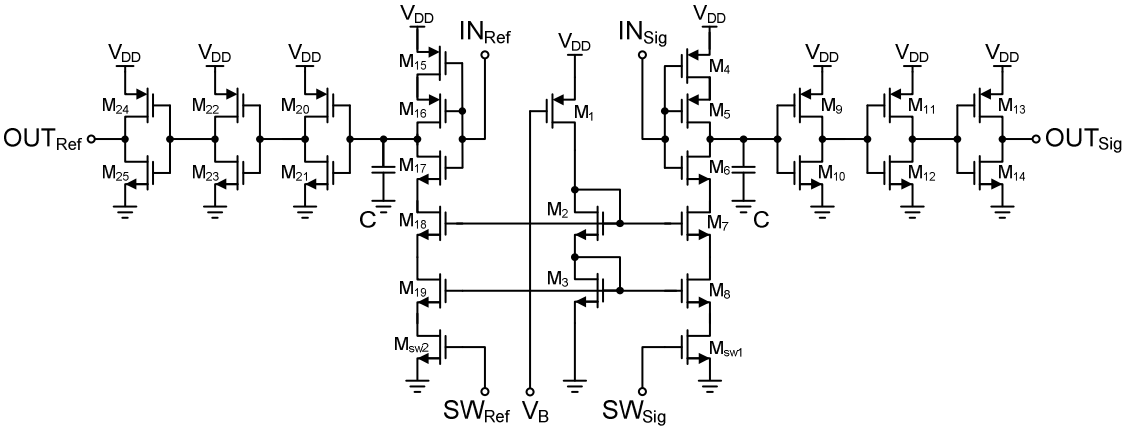


Fig. A.12. The transistor schematic for the block “DiffVCDU” in Fig. A.2

M_1	0.6um/8um
M_2, M_7, M_{18}	1um/0.4um
M_3, M_8, M_{19}	2um/0.4um
M_4, M_{15}	1um/0.2um
M_5, M_{16}	0.4um/0.3um
M_6, M_{17}	0.5um/0.12um
M_9, M_{12}, M_{14}, M_{20}, M_{23}, M_{25}	1um/0.12um
M_{10}, M_{21}	0.5um/0.12um
M_{11},M_{13}, M_{22}, M_{24}, M_{SW1}, M_{SW2}	2um/0.12um

Table A.1. The dimensions (W/L) of the transistors in the schematic of Fig. A.12

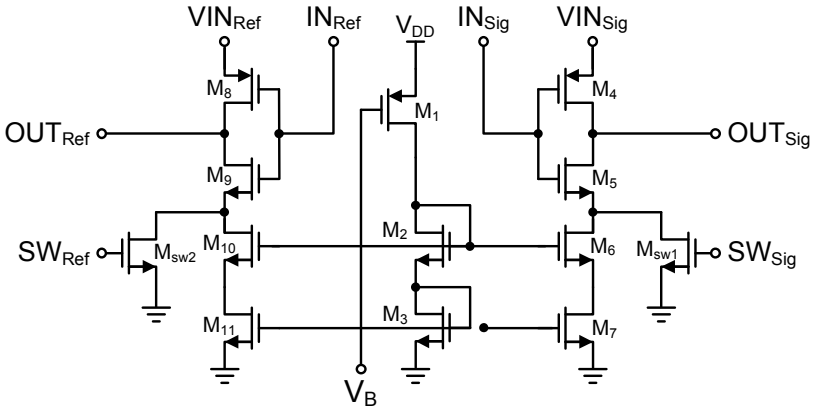


Fig. A.13. The transistor schematic for the block “DiffVCDUOSC” in Fig. A.1

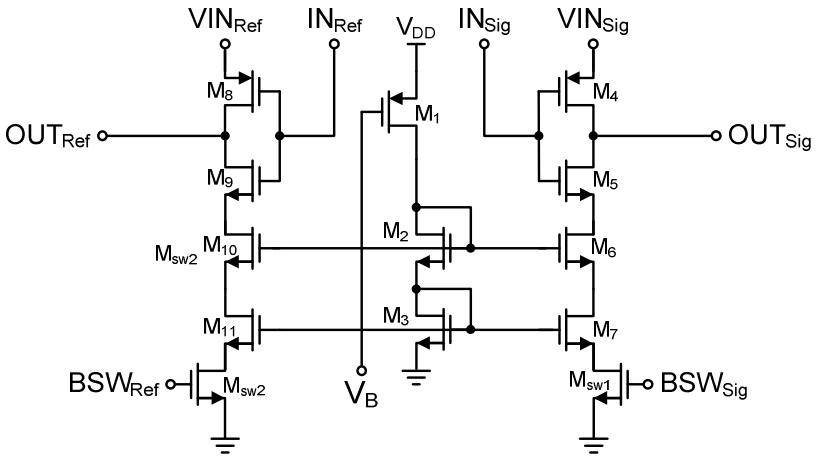


Fig. A.14. The transistor schematic for the block “SWDiffVCDUOSC” in Fig. A.1

M_1	0.6um/8um
M_2, M_6, M_{10}	1um/0.4um
M_3, M_7, M_{11}	2um/0.4um
M_4, M_8	3um/0.12um
M_5, M_9	0.5um/0.12um
M_{sw1}, M_{sw2}	2um/0.12u

Table A.2. The dimensions (W/L) of the transistors in the schematics of Fig. A.13 and Fig. A.14

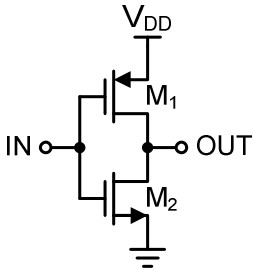


Fig. A. 15. The transistor schematic for the digital “INVERTER” block

M_1	2um/0.12um
M_2	1um/0.12um

Table A.3. The dimensions (W/L) of the transistors in the schematic of Fig. A.15

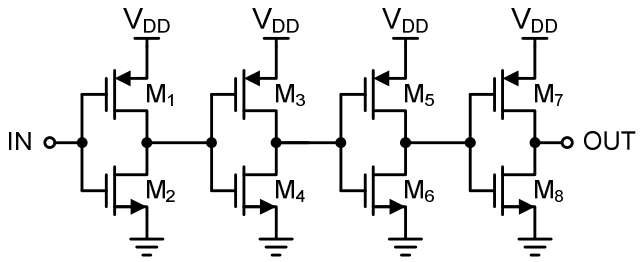


Fig. A.16. The transistor schematic for the digital buffer “Buff-Delay” block

M_1, M_3, M_5	1um/1um
M_2, M_4, M_6	0.5um/1um
M_7	2um/0.12um
M_8	1um/0.12um

Table A.4. The dimensions (W/L) of the transistors in the schematic of Fig. A.16

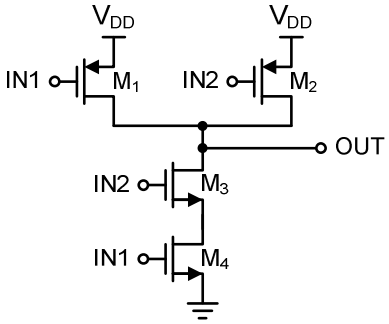


Fig. A.17. The transistor schematic for the digital “NAND” block

M_1, M_2	2um/0.12um
M_3, M_4	1um/0.12um

Table A.5. The dimensions (W/L) of the transistors in the schematic of Fig. A.17

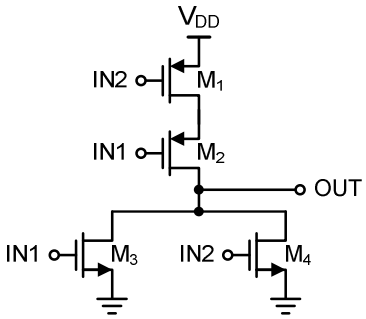


Fig. A.18. The transistor schematic for the digital “NOR” block

M_1, M_2	2um/0.12um
M_3, M_4	1um/0.12um

Table A.6. The dimensions (W/L) of the transistors in the schematic of Fig. A.18

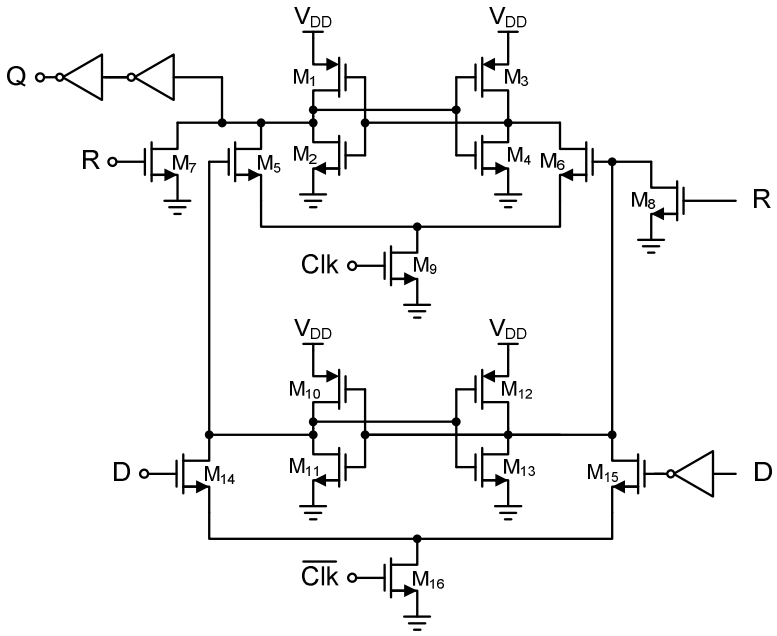


Fig. A.19. The transistor schematic for the digital “D-Flip-Flop” block

M_1, M_3 ,M_7, M_8, M_{10}, M_{12}	2um/0.12um
M_2, M_4, M_{11}, M_{13}	1um/0.12um
M_5, M_6, M_9, M_{14}, M_{15}, M_{16}	3um/0.12um

Table A.7. The dimensions (W/L) of the transistors in the schematic of Fig. A.19

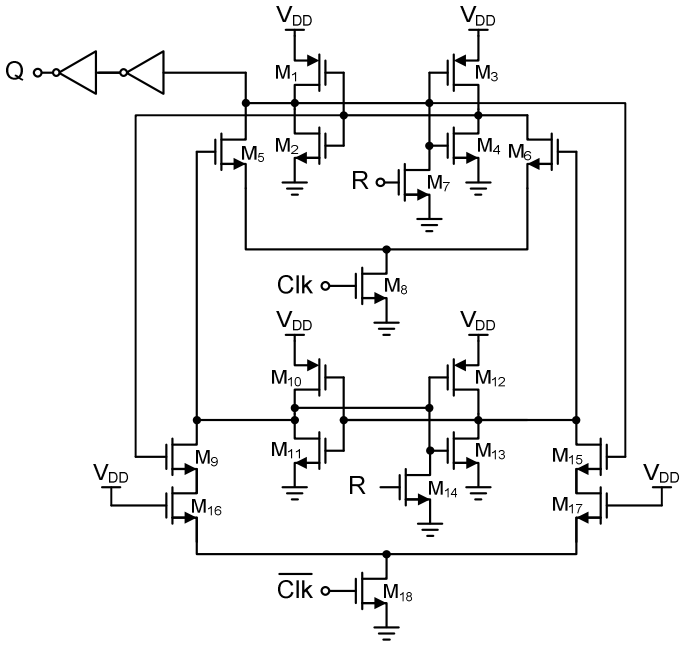


Fig. A.20. The transistor schematic for the digital “T-Flip-Flop” block (TFF) with the T-input internally connected to V_{DD}

M_1, M_3 ,M_7, M_{10}, M_{12}, M_{14}	2um/0.12um
M_2, M_4, M_{11}, M_{13}	1um/0.12um
M_5, M_6, M_8, M_9, M_{15}, M_{16}, M_{17}, M_{18}	3um/0.12um

Table A.8. The dimensions (W/L) of the transistors in the schematic of Fig. A.20

Appendix B

Appendix B offers the circuit diagram and all the transistor dimensions required to reproduce the design presented in Chapter 6 for the implementation of the time-mode interface for capacitive sensors.

Circuit Diagrams and Block Connection

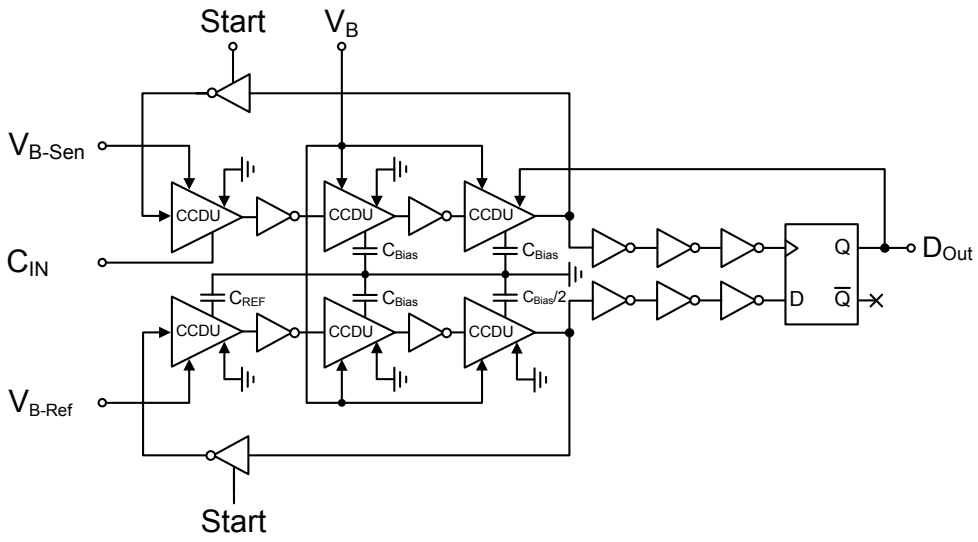


Fig. B.21. Top-level schematic of the time-mode interface for capacitive sensors

Transistor Dimensions

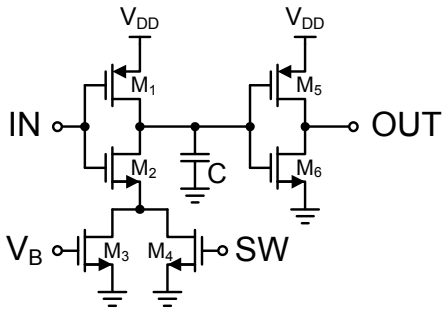


Fig. B.22. The transistor schematic for the “CCDU” block in Fig. B.1

M_1, M_2, M_5	1um/0.1um
M_3	0.5um/3um
M_4	2um/0.1um
M_6	0.5um/0.1um

Table B.9. The dimensions (W/L) of the transistors in the schematic of Fig. B.1

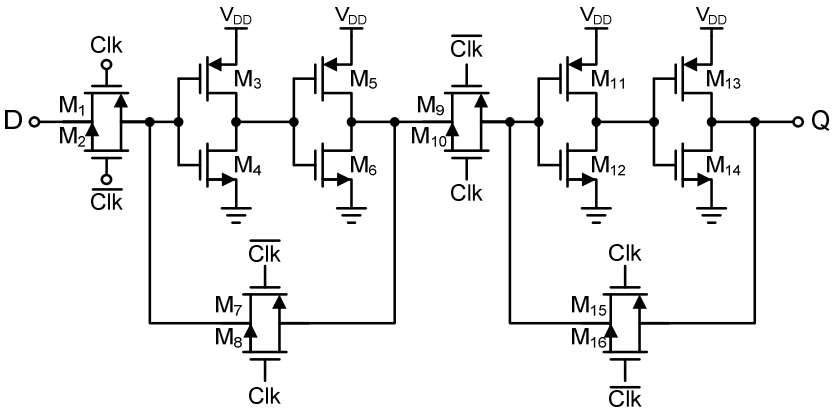
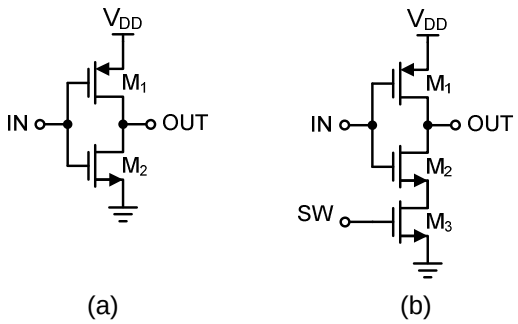


Fig. B.23. The transistor schematic for the digital “D-Flip-Flop” blockTFF) of Fig. B.1

M_1, M_5 ,M_8, M_{13}	2um/0.1um
M_2	4um/0.1um
M_3	3um/0.1um
M_4, M_6, M_7, M_9, M_{11}, M_{14}, M_{15}	1um/0.1um
M_{10}, M_{12}, M_{16}	0.5um/0.1um

Table B.10. The dimensions (W/L) of the transistors in the schematic of Fig. B.3



(a) (b)

Fig. B.24. The transistor schematic for the (a) typical inverter (b) inverter with three inputs of Fig. B.1

M_1, M_3	2um/0.1um
M_2	1um/0.1um

Table B.11. The dimensions (W/L) of the transistors in the schematic of Fig. B.4