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HIGH MVA FACTS CONTROLLERS BASED ON DIODE-CLAMPED MULTILEVEL CONVERTER

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A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for the degree of
Doctor of Philosophy

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July 1997

Dedicated to my parents,

my wife, my sister and brothers

ABSTRACT

Several multilevel converter topologies have stimulated widespread interests amongst researchers because they have the capabilities of: (i) reaching high voltage ratings without magnetics and transformers and (ii) attaining low Total Harmonic Distortions (THD), using the low switching frequencies of gate-turn-off thyristors (GTOs). This thesis focuses on the diode-clamped multilevel converter topology as the basic module for realizing the high kV voltage rating and the high MVA rating in controllers for the Flexible AC Transmission Systems (FACTS).

The thesis has extended the topology configurations to include: (i) multiple modules of multilevel converters and (ii) multimodules of multilevel converters in a back-to-back rectifier/inverter link. These configurations form the backbones for the following multilevel FACTS controllers: (a) the Shunt STAT(ic)COM(pensator), (b) the Series STATCOM, (c) the Unified Power Flow Controller (UPFC) and (d) the Asynchronous Link.

A number of key technical innovations have been assembled together to make the new multilevel FACTS controllers possible. On the sides of the ac lines, the Fundamental Frequency Switching strategy has been extended so that it succeeds in simultaneously (a) lowering the Total Harmonic Distortions in the voltage and current waveforms, (b) controlling directly the ac voltage magnitudes, and (c) sharing the current loading in the parallel modules. On the side of the dc links of the STATCOMs, feedback controls have succeeded in: (a) regulating the total dc link voltages and (b) equalizing the dc capacitor voltages in all the levels. The voltage equalization by feedbacks cannot be accomplished in the case of the Unified Power Flow Controller (UPFC) and the Asynchronous Link. A system of locally controlled class-B choppers which transfer the charges from dc capacitors with the higher voltages to their contiguous neighbours with the lower voltages succeeds in equalizing the dc capacitor voltages.

The proofs of performance of the multilevel FACTS controllers are substantiated by digital simulations. The equalization of the multilevel rectifier/inverter using the system of class-B choppers has been proven experimentally.

RÉSUMÉ

Plusieurs convertisseurs à topologies multi-niveaux suscitent présentement un grand intérêt chez les chercheurs, grâce à leurs propriétés fort attrayantes: (i) ils atteignent des niveaux de tension élevés sans faire appel à des transformateurs ou autres appareils magnétiques, et (ii) ils contribuent peu d'harmoniques, tirant profit des faibles fréquences de commutation des transistors GTO. Dans cette thèse, le convertisseur multi-niveaux à diode de clampage servira comme module principal dans la réalisation de contrôleurs pour des systèmes flexibles d e transport à courant alternatif (FACTS, de l'anglais) à haute tension et à grande puissance.

Nous étudions plusieurs variantes tributaires d'une configuration de base, pour inclure (i) de multiples modules de convertisseurs multi-niveaux et (ii) des ensembles multi-modulaires de convertisseurs multi-niveaux formant des liens redresseur/onduleur. Ces configurations sont au coeur des contrôleurs FACTS suivants: (a) le compensateur statique shunt, (b) le compensateur statique série, (c) le contrôleur unifié (UPFC), et (d) le lien asynchrone.

Les contrôleurs proposés recèlent plusieurs innovations techniques importantes. Du côté alternatif, le choix de la stratégie de commutation à la fréquence fondamentale offre les advantages majeurs suivants. Elle permet (a) de réduire la distorsion harmonique des signaux de tension et de courant, (b) de contrôler directement l'amplitude de la tension alternative, et (c) de dicter le partage des courants chez les modules en parallèle. Chez les compensateurs statiques, la présence de contre-réaction du côté continu permet (a) de régulariser la tension continue du lien, et (b) d'égaliser les tensions des condensateurs à tous les niveaux. Par contre, utilisant cette dernière stratégie de contre-réaction, nous n'avons pas pu reproduire les résultats favorables pour le UPFC ou pour le lien asynchrone. Dans une stratégie de rechange, l'égalisation des tensions des condensateurs est assurée par un système de hacheurs de classe B, contrôlés localement, qui transfèrent des charges à partir des condensateurs à haute tension vers leurs voisins à tensions plus faibles.

Des essais numériques ont prouvé le bien-fondé des conceptions proposées pour les contrôleurs FACTS multi-niveaux. Au laboratoire, un lien redresseur/onduleur multi-niveaux à système de hacheurs a été construit et a franchi ses essais avec succès.

ACKNOWLEDGMENTS

First of all, I would particularly like to thank Professor Dr. B.T.Ooi, my supervisor, who has not only provided me with a research assistantship to pursue my Ph.D program, but has also given me extremely helpful guidance, encouragement, inspiration and discussions.

I am grateful to Professor Dr. H.C.Lee, Professor Dr. N.Hori, my Ph.D committee members, for their exceptional advice and suggestions.

I want to give my hearty thanks to Professor Dr. F.D.Galiana for his support , friendship and for letting me have full access to the computer facilities for simulation, hardware design and the preparation of papers.

I want to express my special gratitude to Dr. Z.Wolanski and Mr. B.Mwinyiwiwa for their pioneering role in setting up the DSP real-time control system and their laboratory assistance throughout the course of research.

I also want to thank my lab colleagues, especially Dr. M.Kazerani, Dr. L.Lopes, Mr. J.Cheng, Ms. Z.Li, Ms. X.Huang, Mr. B.Lu, Ms. X.Nie, Mr. Jia, Mr. Mark, Ms. Elene for their friendship.

My special gratitude goes to Mr.C.Jorgensen, Mr.J.Mui, Mr.J.Walker, Ms.N.de Verteuil, Mrs. T.Hyland, Ms.C.Bethelmy and Mrs.R.Pinzarrone for their kindness and significant help in dealing with my many technical and financial problems. The same gratitude also goes to other supporting staffs of the Electrical Engineering Department, especially, Mr.T.Levasseur, Mr.S.Henry, Mrs.P.Jorgensen, Mrs.V.Soltani, Miss.C.Greco, Ms.H.Mayer and Mrs.Menon.

I would like to extend my thanks to Dr.M.Huneault for putting his precious time in making the translation of the abstract of this thesis.

Finally, I must give my special thanks to my wife, Dongxian, for her everlasting love and support. My special thanks also go to my parents for their constant encouragement and support.

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LIST OF MAIN SYMBOLS

C	Capacitor
f_c	Carrier Frequency
f_m	Modulation Frequency
φ	Power factor angle
I	AC Current
L	Inductance
X	Reactance
R	Resistance
δ	AC voltage phase angle
V,v	AC voltage
V_{dc}	DC voltage
V_{cj}	Voltage of the *j*th dc capacitor
V_m	Modulation signal
V_{REF}	Reference voltage
α_{im}	The *i*th Switching degree of freedom in the *m*th module of the *N*-level converter, using the extended Fundamental Frequency Switching strategy.

LIST OF ACRONYMS

AC, ac	Alternating current
A/D	Analog to Digital
BJT	Bipolar Junction Transistor
D/A	Digital to Analog
DC, dc	Direct current
DSP	Digital Signal Processor
FACTS	Flexible AC transmission System
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
GTO	Gate Turn-Off Thyristor
HVdc	High Voltage direct current
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
MCT	MOS-Controlled Thyristor
MVA	Mega Volt Ampere
NPC	Neutral Point Clamped
PI	Proportional and Integral
PLD	Programmable Logic Device
PLL	Phase Lock Loop
SITH	Static Induction Thyristor
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Compensator

SVC	Static VAR Compensator
TCRs	Thyristor Controlled Reactors
THD	Total Harmonic Distortion
TSCs	Thyristor Switched Capacitors
UPFC	Unified Power Flow Controller
VAr	Voltage Ampere reactive
VCO	Voltage Controlled Oscillator

CHAPTER ONE

INTRODUCTION

The research of this thesis forms a part of McGill University's continuing research program on Flexible AC Transmission Systems or FACTS. In the past years, the research has been devoted to the concepts, the topologies and the feedback controls of the following FACTS Controllers: the series STATCOMs, the UPFCs, the Asynchronous Links. This research phase is over.

The research of this thesis belongs to the second phase, which is to find the practical means of realizing the FACTS controllers so that they can withstand hundreds of kilovolts (kV) and handle hundreds of megavoltamperes (MVAs) of the electric utility environment. This thesis is focussed on using the diode-clamped, multilevel converter topology to realize the high kV and high MVA FACTS controllers.

This chapter introduces the reader firstly to conventional power controllers and

their limitations. The advances in high power electronics usher in the era of FACTS controllers. The literature review is brief because FACTS is a recent research subject. The research papers on the methods of increasing the kV and the MVA ratings of the FACTS controllers are scantier still. As the research subject is on multilevel converters, a close examination is made of the 3 promising multilevel topologies and justifications for devoting the entire research to the diode-clamped topology are given. The chapter ends with a guide to the chapters which constitute this thesis.

1.1 Flexible AC Transmission Systems (FACTS)

1.1.1 Conventional Power Controllers

The modern power system contains hundreds of transmission lines. Apart from the voltage and frequency regulators of the generators, the power system depends on numerous other power controllers to regulate the terminal voltages, to reduce the reactive power in the transmission lines and to maintain the power flow at an economical and secure level below their thermal limits with optimal margin. In theory, the rotating synchronous machine can undertake all these tasks. However, because of the long time constants in the field excitation control and the governor speed control, the operating margins have to be set conservatively.

In order to increase the capability of power transmission, most of the power controllers in use today are static ones, such as the Thyristor Switched Capacitors (TSCs)

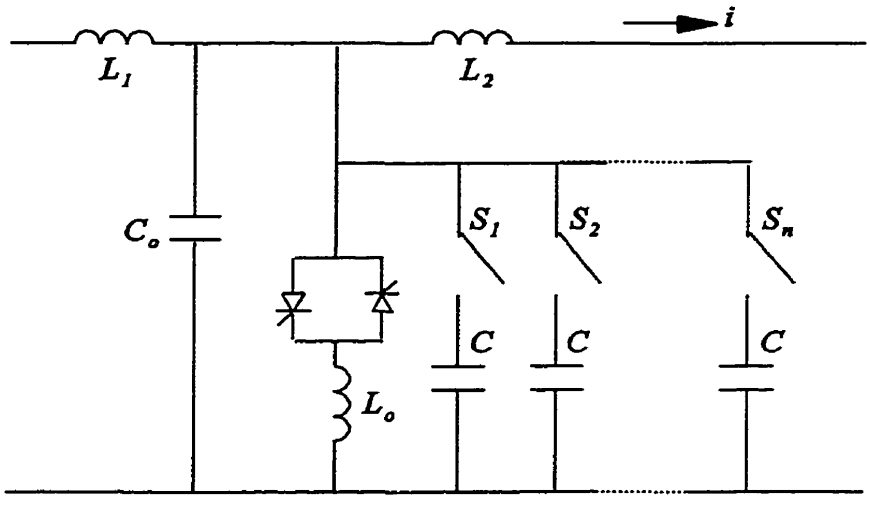

Fig.1-1 Static VAr compensator using thyristor controlled reactor with switched capacitors.

and the Thyristor Controlled Reactors (TCRs) [1] for VAr compensation, Phase Shifting Transformers [2,3] for phase angle control. The static VAr compensator [4] as shown in Fig.1-1, for example, contains banks of inductors and capacitors to change reactive power in steps and depends on the line-commutated thyristors to fine-tune the equivalent

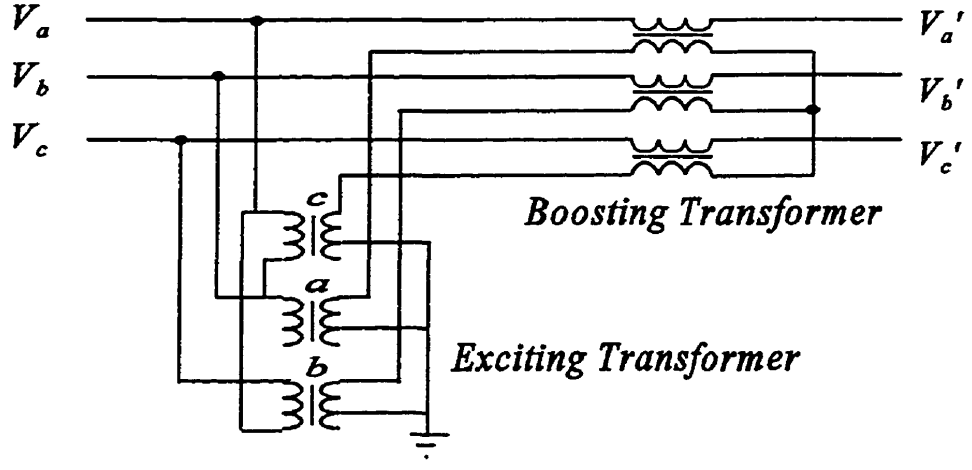

Fig.1-2 Phase-shifter using transformers.

reactance. Although it is fast with respect to the field excitation and the governor controls, it is still slow in dynamic response because the thyristor cannot be turned OFF through the gate and has to be line-commutated. The conventional phase-shifter, as shown in Fig.1-2, uses delta/wye transformers with boost transformers to inject quadrature voltages into power system. It is difficult to control the phase shift with mechanically driven tap-changers.

1.1.2 FACTS Power Controllers

Gate-turn-off thyristors (GTOs) at ratings of 6 kV and 3 kA are now available for the development of a new generation of flexible power controllers based on GTO technology. Unlike the thyristor, the GTO can be switched OFF at any specified instant by a gate signal. Therefore active switching strategies can be applied and new power controllers, similar to but with faster response than that of the synchronous machines, can be developed.

Foreseeing the advantages which high power electronics can bring to electric power utilities, the Electric Power Research Institute (EPRI) of USA initiated the Flexible AC Transmission Systems (FACTS) program in the late 1980s [5,6] to use solid-state power controllers to load the transmission lines to the levels nearer their thermal limits [7,8]. By increasing the transmissibility of power in existing lines, the need to build new lines can be postponed. As the rights-of-the-way to build new lines are increasingly difficult to secure, this postponement is very desirable.

The GTO-FACTS controllers have been conceived to interact with the power system in several ways to bring about the increase in power transmissibility. As a series capacitive reactance compensator (series STATCOM), the FACTS controller compensates the large inductive line reactance to lower the total line reactance. As a shunt capacitive reactance compensator (shunt STATCOM), it regulates the ac voltage at any point in the transmission line against voltage sags and overvoltages and increases the power transmissibility. One of the most powerful control attributes comes from the ability of the GTO-FACTS controller to function as a phase-shifter. With multiple control degrees of freedom, the FACTS controller, in the form of an Asynchronous Link or as a Unified Power Flow Controller (UPFC), can control independently the real power and the reactive powers of both ends of the radial transmission line. In general, the fast action of the GTO-FACTS controller enables the limit of the transient stability to be increased.

As a result of EPRI's initiatives, a small number of GTO-FACTS prototypes are now in existence. A ±100 MVAR Static Compensator (STATCOM) for voltage control of transmission systems [9,10] has been designed and installed in USA. The STATCOM makes use of 8 modules of 2-level converters, with each converter taking the circuit of Fig.1-3. {In this thesis, the symbol of the V inside the square box is used to denote a valve with gate-turn-ON and gate-turn-OFF capabilities. Besides GTOs, other possible valves are IGBTs (Insulated Gate Bipolar Transistors), MCTs (MOS-Controlled Thyristors), SITHs (Static Induction Thyristors,) etc.} Another example is the Unified Power Flow

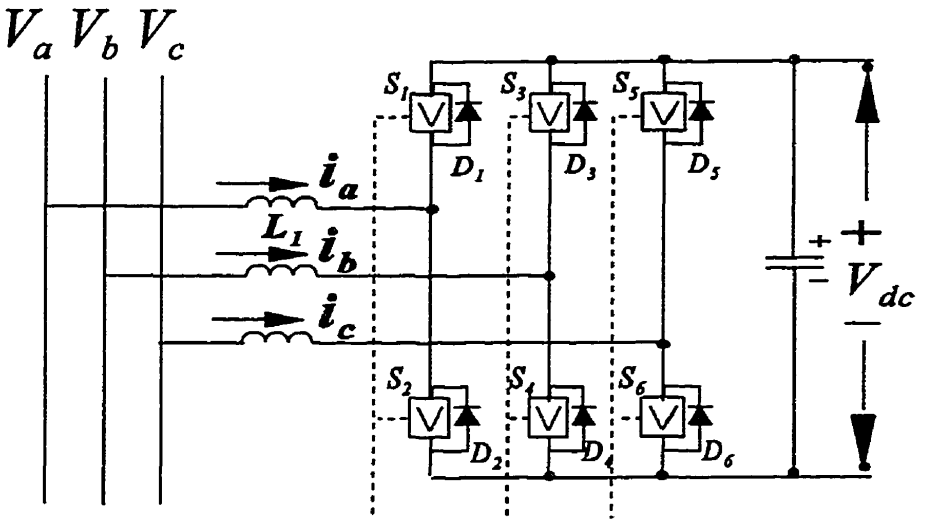

Fig.1-3 Shunt Static VAr compensator using GTO converter.

Controller (UPFC) [11-16] as shown in Fig.1-4 which has been invented to provide a universal solution to voltage regulation, series compensation, phase-shifter control and multi-function power flow control. It consists of two back-to-back voltage-source GTO converters, one in series and the other in parallel with the transmission line. The shunt-converter half of a prototype UPFC has been installed in the American Electric Power utility in Ohio which now operates as a shunt-STATCOM. The series-converter half is expected to be completed shortly.

Outside North America, the research has concentrated on High Voltage Direct Current (HVdc) Transmission using GTO technology. A 300MW self-commutated converter prototype [17] is being developed in Japan for research in future HVdc transmission and dc interconnections. In May 1997, ASEA Brown Boveri (ABB) invited

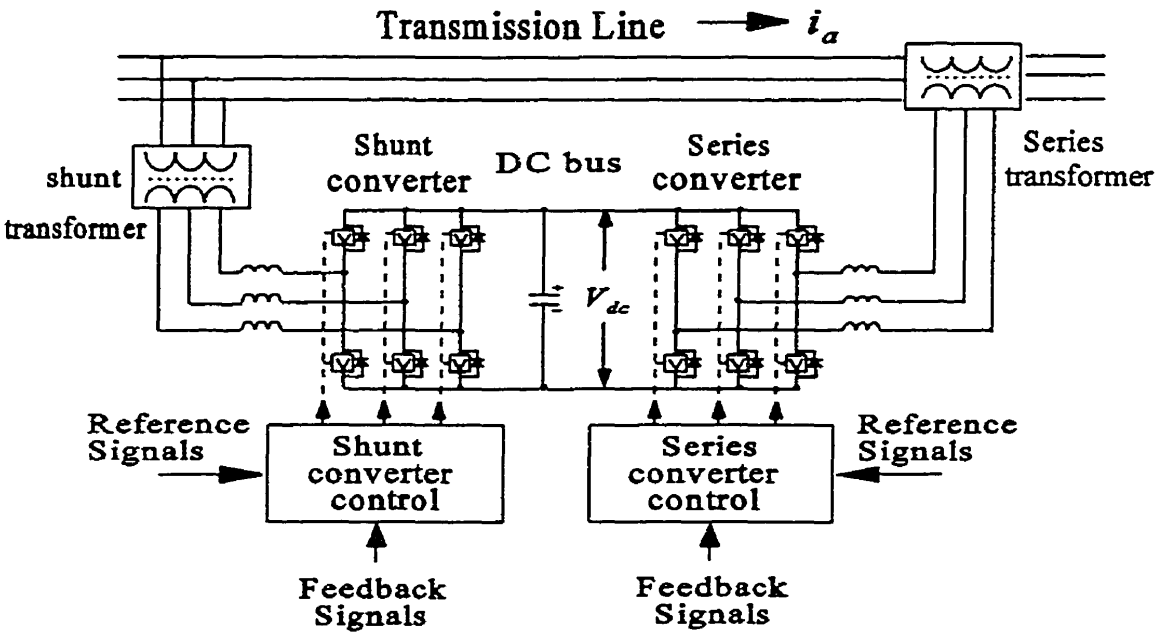

Fig.1-4 Unified Power Flow Controller using GTO converters.

the electric utility community to visit its prototype HVdc Light. ABB, however, has opted for IGBT technology instead of GTO technology. Solid-state Phase Shifters [18-21] have also been proposed to replace magnetic Phase Shifting Transformers.

1.2 Methods to Meet High kV and High MVA Rating Requirements

The family of FACTS controllers, which this thesis is concerned with, is based on the 3-phase, voltage-source bridge converters of Fig.1-3 In order to withstand the high voltage stresses and to carry the large currents of the electric utility environment, many valves must be connected in series and/or in parallel (with auxiliary circuits to ensure that the voltages and currents are shared equally). The connection of the valves in

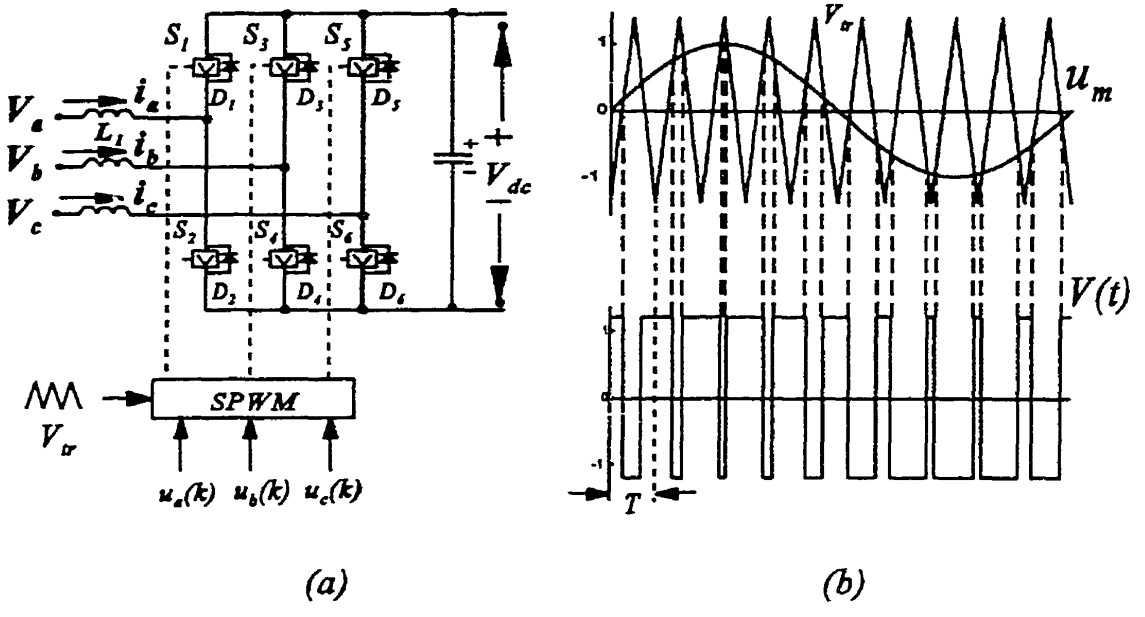

Fig.1-5(a) 2-level voltage source inverter, (b) output voltage waveform using SPWM switching strategy.

series/parallel can be accomplished in at least 3 ways: (1) as series/parallel strings of valves, (2) as multiple modules of 2-level voltage-source converters, and (3) as a multi-level converters.

1.2.1 Series/Parallel Strings of Valves

Fig.1-5(a) shows the 3-phase, two-level converter which is composed of 6 power switches and six anti-parallel diodes. The power switches are switched ON or OFF in a complementary mode. Each power switch has to sustain the voltage stress which is equal to the dc capacitor voltage. In order to withstand the high voltage and to carry the high current loading, each power switch must be made of a large number of series- and/or parallel-connected GTOs to sustain the high voltage and high current ratings. This entails

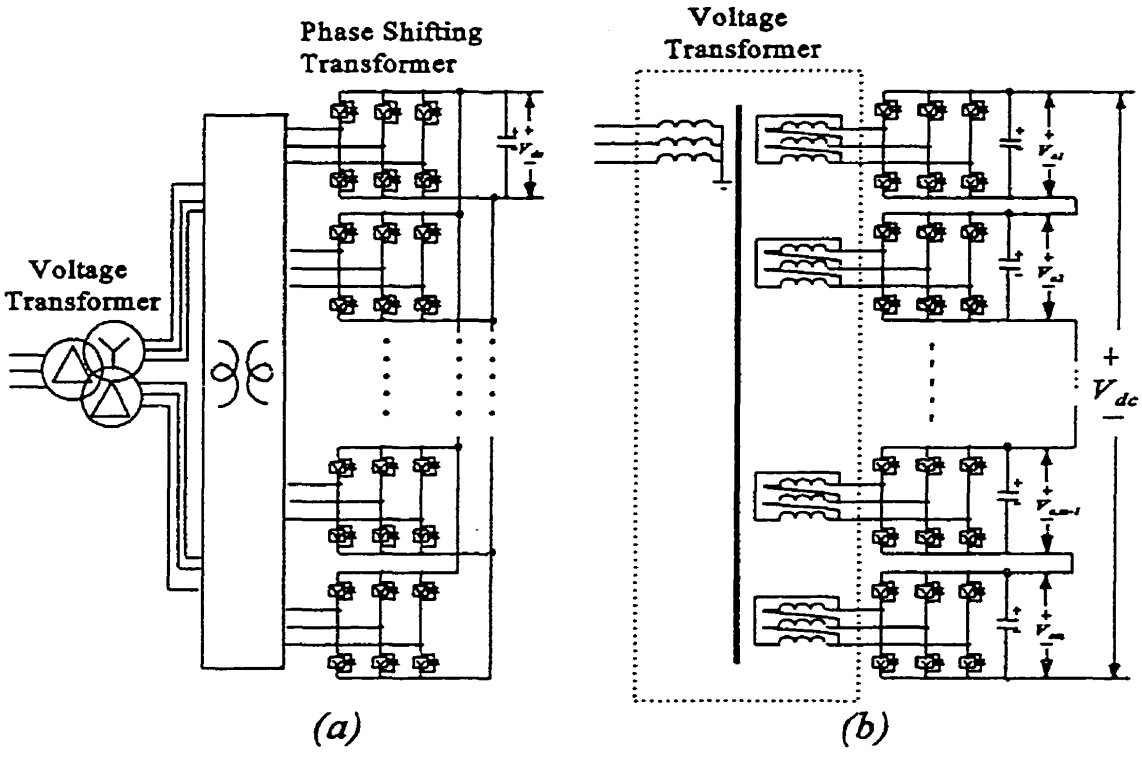

Fig.1-6 Multimodules of 2-level converters, (a)STATCOM, (b)HVdc.

the simultaneous switching ON and OFF of the individual GTOs in order to equalize the voltage and the current stresses across the GTO devices in steady-state and in transient. Recently, it has been reported that GTOs connected in series have successfully operated as a single power switch [17,23].

1.2.2 Multiple Modules of 2-level converter

The necessity to master the technology of simultaneous switching of the series- and parallel-connected GTO devices can be bypassed by connecting multiple modules of 2-level converters in parallel [9] and/or in series [25].

Fig.1-6(a) shows the schematic of the STATCOM [9] based on multiple modules of 2 level converters. The GTO in each converter is switched ON and OFF only once every cycle and the low harmonics of the output voltages are eliminated by using the gating signals of each converter to phase-shift the square voltage waveforms. Because the output voltages of the converters have the phase-shifts, the converter ac terminals cannot be parallelled without the penalty of a large circulating current. Phase-shifting transformers (phase shifts obtained for tertiary windings) are interposed between the converters to bring their voltages in time phase at their common terminals, thus allowing parallel connection without the large circulating current. At their common terminals, another transformer stage steps up the low voltages of the converters to the high voltages of the transmission lines.

Fig.1-6(b) shows the schematic of a HVdc terminal [25] which is based on multiple modules of 2-level converters. The modules are series-connected in the dc link to build up a high dc voltage. The phase-shifted triangle carrier technique applied to the well known Sinusoidal Pulse Width Modulation (SPWM) strategy has the very attractive property that the carrier frequency is effectively increased by a multiple equal to the number of modules in connection. This has the implication that the slow switches such as the GTOs can be used in controllers such as the HVdc terminal by using a large number of modules to compensate for the low triangle carrier frequency at which each module has to operate.

1.2.3 Multilevel Converter Structures

In their attempts to overcome harmonics distortion and to improve the efficiency of the motor drive system, Nabae invented the Neutral-Point-Clamped, 3-level inverter [26] in 1981. Bhagwat and Stefanovic then proposed the generalized structure of a multilevel inverter [27] in 1983. However, the research on this subject is sparse until the 1990s when the advance in GTO technology has re-triggered researchers' interests in multilevel converters because of their capability to reach a high voltage rating without the need of magnetic transformers. Its unique structure enables the GTOs to be connected in series to build up the voltage rating, without the necessity of perfecting the technology of triggering them ON and OFF simultaneously. The multilevel research [28-51] has been directed mostly to realizations of the STATCOM.

So far, three types of voltage source multilevel converters are recognized as potential candidates for FACTS Controllers: (1) the diode-clamped converter , (2) the flying-capacitors converter, and (3) the cascaded-inverters with separated dc sources. The thesis research is devoted entirely to the diode-clamped topology. However, brief descriptions are given in the next sections to all the 3 candidates and the evaluations which have been made show that the diode-clamped topology is the most promising one.

1.2.3.1 Diode clamped multilevel converter

Fig.1-7 shows the structure of the diode-clamped multilevel converter [28-32], which is actually an expanded version of Nabae's Neutral-Point, 3-level converter [26]. In the structure, (N-1) dc capacitors divide the total dc link voltage into N levels and each

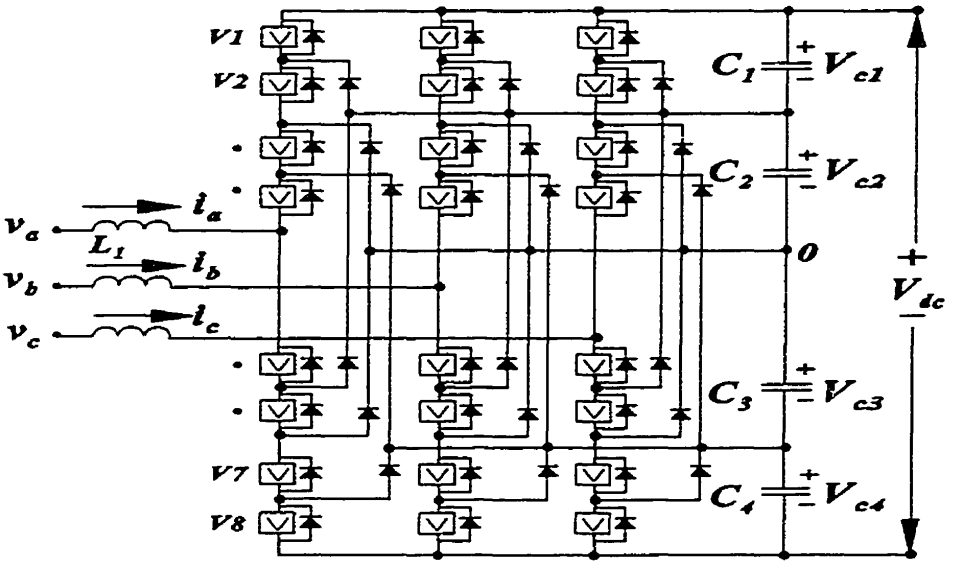

Fig.1-7 Diode clamped 5-level converter.

half-leg consists of (N-1) series-connected valves, with each valve being interconnected to the corresponding level of the dc capacitor via clamping diodes. The idea is to limit the voltage stress of the valves to the dc link capacitor voltage of the jth level (j=1,2 ... N-1) with the help of these clamping diodes. Thus the voltage ratings of the converter can be increased by adding the number of levels that are connected in series without increasing the individual GTO rating, provided the technology to ensure that the dc link voltages are equal at all the levels is perfected. However, the clamping diodes have to sustain the high voltage stress as the number of levels increases. The voltage withstand of the diodes can be increased by connecting several units in series. Unlike the GTOs, the turning ON and OFF of the diodes do not depend on gate-triggering so that passive circuits are sufficient to ensure equalization of the voltage stresses in steady-state and in transient.

1.2.3.2 Flying-capacitor multilevel converter

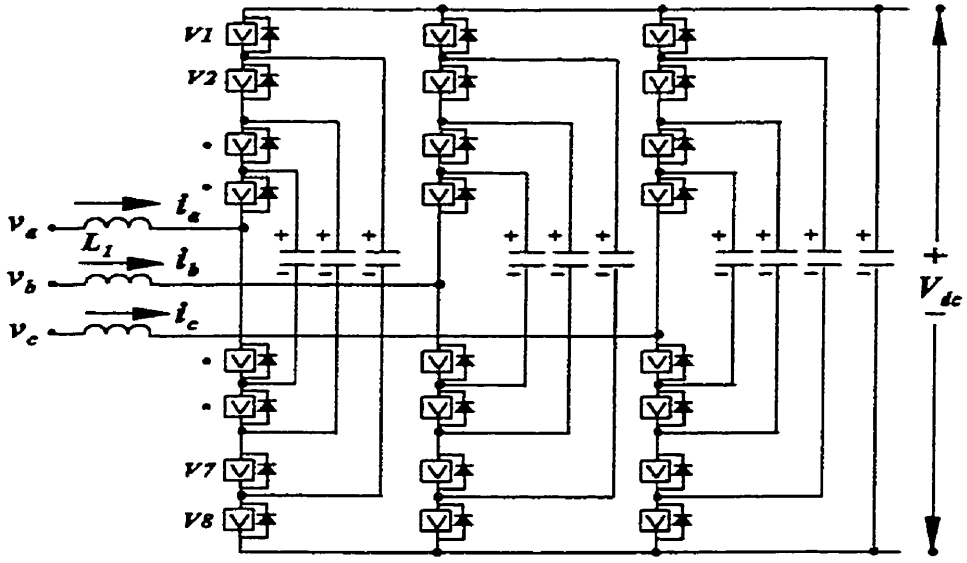

Fig.1-8 Flying capacitor 5-level converter.

Fig.1-8 shows the structure of the flying-capacitor multilevel converter [28]. In the structure, every pairing of the valves that are symmetrically located on the phase legs is spanned by a dc capacitor. The size of the voltage increment between any capacitor and the capacitor bracketing it on the outside determines the size of the forward voltage stress of the switching valves clamped by the two dc capacitors. For a N-level converter, it requires 6(N-1) switching valves and (3N-5) dc capacitors. The structure appears to be simple and symmetric. However, compared with diode-clamped converter, it requires a large number of capacitors, which normally entails the same number of complicated controllers or independent dc power suppliers to maintain their voltages at the specified levels.

1.2.3.3 Cascade multilevel converter

Fig.1-9 shows the structure of the cascade multilevel inverters [33,34], in which full

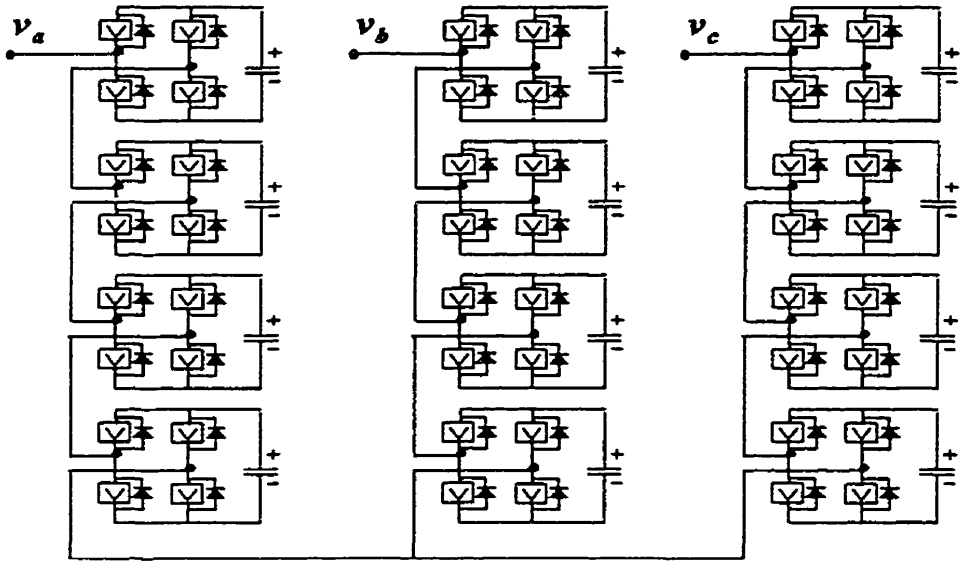

Fig.1-9 Cascade 9-level converter.

single phase H-bridge inverter modules are connected in series, with each module being fed by the voltage from a separate dc capacitance. The N-level cascaded-inverter uses 6(N-1) switching valves and 3(N-1)/2 dc capacitors . It has been proposed for application as a static VAr compensator (STATCOM).

1.3 FACTS Controllers Based on Multilevel Converters

1.3.1 Comparison of Different Multilevel Structures

In this section, the 3 multilevel structures will be evaluated for the purpose of determining which is the most promising structure to follow in the research of the thesis. In the comparison, formulas of the components count of the GTOs, the diodes, the capacitors etc. required for the 3 different structures to implement the *N*-level converter

Table 1-1 Formulas for counting components of multilevel converter

	Diode clamped inverter	Flying capacitor inverter	Cascade inverter
Switching valves	6(N-1)	6(N-1)	6(N-1)
dc capacitors	(N-1)	(N-1)*(N-2)*3/2+(N-1)	3(N-1)/2
Clamping diodes	(N-1)*(N-2)*3	0	0

STATCOM of a given MVA rating and kV rating are compiled in Table 1-1.

Table 1-2 lists the number of solid switches, dc capacitors and clamping diodes required to implement a 9-level converter. Obviously, the cascade structure and the flying-capacitance structure require more capacitors and the diode-clamped structure needs more clamping diodes. Table 1-3 lists their fields of application.

Table 1-2 Actual number of components required in 9-level converter

	Diode-clamped inverter	Flying capacitor inverter	Cascade inverter
Switching devices	48	48	48
dc capacitors	8	92	12
Clamping diodes	168	0	0

Table 1-3 Fields of application of multilevel converter

	Diode clamped	Flying capacitor	CASCADE
application	STATCOM, UPFC, ...	STATCOM	STATCOM

Compared with the diode-clamped structure, both the cascade structure and the flying-capacitor structure require many more dc capacitors and complex capacitor voltage controllers. In addition, both of them cannot be used for application in the back-to-back rectifier/inverter dc link, which is the core of the Unified Power Flow Controller (UPFC) and the Asynchronous Link. This is because the dc capacitors are specific to each of the three phases, so that on the dc-side, the three-phase ac real powers of the rectifier-side do not surrender their identities and merge into a single collective dc-power so as to enable the real power on the inverter-side to emerge as 3-phase ac complex power with a different phase angle.

Although the diode-clamped structure will need more clamping diodes, it incurs less cost and losses. Unlike the other two structures, the 3-phase legs of the diode-clamped structure share the common series-connected dc capacitors. Therefore, it can be used in almost all kinds of FACTS controllers, including those based on the aforesaid back-to-back, rectifier/inverter dc link.

Based on above comparisons, **the diode-clamped multilevel converter is chosen as the structure for research in this thesis.**

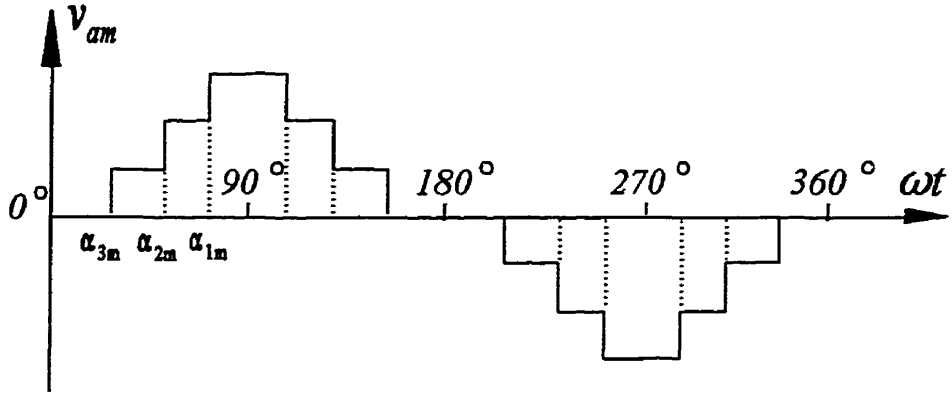

Fig.1-10 Output voltage waveform of 7-level converter under fundamental frequency switching strategy.

1.3.2 Switching Strategy

The literature search shows that only two switching strategies have been considered: (1) the Fundamental Frequency Switching (Selective Harmonics Elimination) strategy [29-32] and (2) the Sinusoidal Pulse-Width-Modulation (SPWM) strategy [29,30]. They differ in their ways to form the output voltage waveforms.

Fig.1-10 shows the staircase output voltage waveform of the Fundamental Frequency Switching strategy from a 7-level converter. For a N-level converter, there are (N-1)/2 degrees of freedom that can be employed for the purpose of control, most of which are currently employed to eliminate up to (N-1)/2 low order harmonics. The magnitude of the kth harmonic of the output voltage waveform of the mth module of N-level converter is:

$$H(k)=\frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(x)\sin(kx)dx$$
$$=\frac{4V_{dc}}{(N-1)\pi}[\cos(k\alpha_{1m})+\cos(k\alpha_{2m})+\ldots+\cos(k\alpha_{(N-1)/2,m})] \quad (1\text{-}1)$$

where k is odd integer and α_{1m}, α_{2m}, ... $\alpha_{(N-1)/2,m}$ are switching angles of the converter in Fig.1-10. The magnitude of its fundamental part is

$$V = H(1) = \frac{4V_{dc}}{(N-1)\pi}V_{dc}(\cos\alpha_{1m}+\cos\alpha_{2m}+\ldots+\cos\alpha_{(N-1)/2,m}) \quad (1\text{-}2)$$

Fig.1-11 shows how the Sinusoidal Pulse Width Modulation technique of Fig.1-5

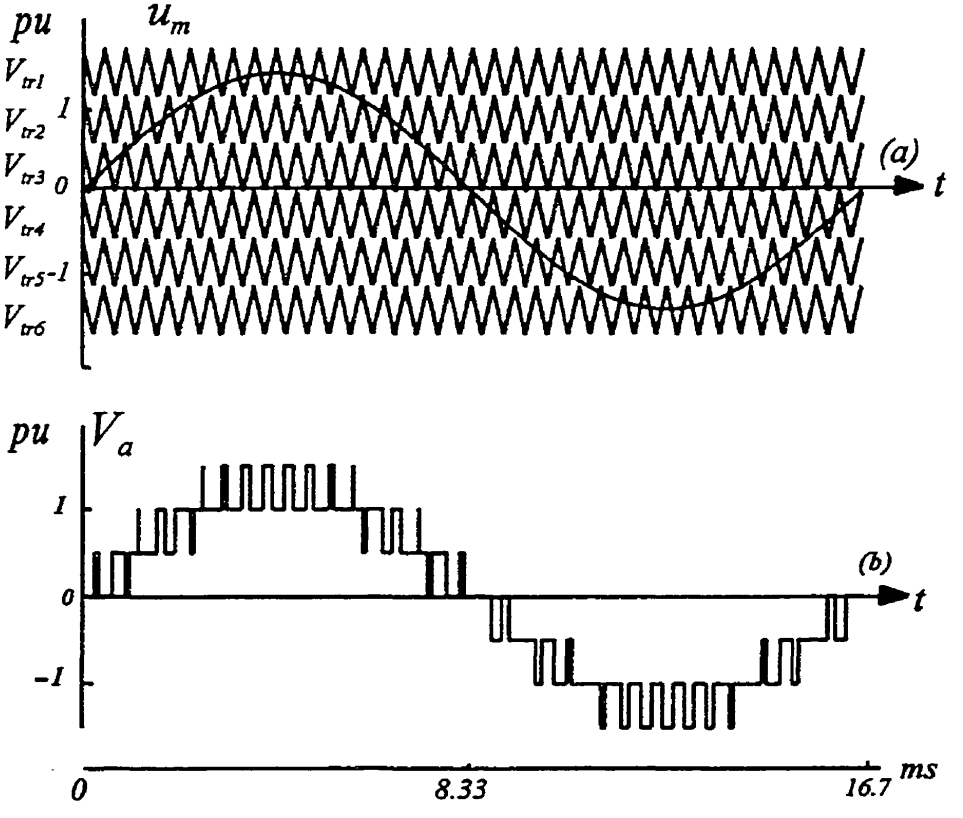

Fig.1-11 (a) Triangle carrier signals and sinusoidal modulation signal, (b) output voltage waveform.

(b) is modified for application to the diode-clamped, 7-level converter. The 7 levels divide the sinusoidal modulation waveform of Fig.1-11 (a) into 6 voltage bands, with the switching of the valves of Fig.1-7 producing the pulsed waveforms in the corresponding bands so that on summation they produce the output of Fig.1-11(b). As illustrated in Fig.1-11(a), each voltage band is provided with its triangle carrier signals. The intersections of the sinusoidal modulating signal and the carriers determine the turning ON and OFF of the values of Fig.1-7 of the corresponding voltage band. When the modulating signal exceeds the upper level or falls below the lower level of the voltage band, the switching logic interpretes the situation as "overmodulation." Thus there is no switching until the modulation signal falls into the voltage band to intersect with the triangle carrier signal of the voltage band. In its output voltage waveform, the local average value within each triangle cycle is proportional to that of the modulation signal and its fundamental component is a linearly amplified signal of the sinusoidal modulation signal [24].

1.4 Objectives of Thesis

This thesis focuses on the diode-clamped multilevel converter topology as the basic module for realizing the high kV voltage rating and the high MVA rating in FACTS controllers. It extends the topology configurations and proposes the extended Fundmental Frequency Switching strategy for realizing the following multilevel FACTS controllers: (a) the Shunt STAT(ic)COM(pensator), (b) the Series STATCOM, (c) the Unified Power

Flow Controller (UPFC) and (d) the Asynchronous Link.

The objectives of the research, reported in this thesis, are to provide the knowledge needed for the practical realization of the high MVA diode-clamped, multilevel STATCOM in the first instance, and later for the realizations of the more complex FACTS controllers such as the Unified Power Flow Controllers (UPFC), which require back-to-back rectifier/inverter dc links.

1.5 Organization of Thesis

The contents of the thesis are organized as follows:

Chapter 2:

Upper most in the mind for the practical realizations are the very large MVA ratings and the very high kV voltage ratings which the FACTS controllers must be able to handle with GTOs which are rated at only 6kV and 3kA. As transformers will be used to bring the transmission line voltages down to the lower voltage of the GTO multilevel converter, the converter-side currents become very large and this implies that many parallel-connected modules of the multilevel converters must be used. This raises the issue of ensuring that the rms currents are shared equally by the parallel modules. In the course of the research, it has been found that the necessity to use multiple modules can be turned into an advantage, as in applying the Fundamental Frequency Switching strategy, the degrees of freedom in designing the switching instants of the GTOs are increased by a

multiple equal to the number of modules. The increased degrees of freedom are exploited to achieve the multiple objectives of: (1) eliminating more low order harmonics so as to improve the Total Harmonic Distortion (THDs) indexes, (2) controlling directly the output ac voltage magnitudes (previous researchers have depended on the slower method of charging and discharging of the dc capacitor voltage), and (3) equalizing the rms ac currents in the different modules. The targetted FACTS controller in this chapter and in chapter 3 is the shunt STATCOM.

Chapter 3:

The requirement of equal sharing of currents in the parallel converter modules in the realization of the shunt STATCOM has the co-requisite of equal sharing of voltage stresses applied across the GTOs [33,36,46]. As the GTOs in the multilevel converter are bracketed between the dc buses of the many levels, this requirement implies the equalization of the voltages across the dc capacitors of each of the multilevels. In the beginning of this research, it was already common knowledge that a feedback loop can apply phase angle control to maintain the total dc voltage regulated [53]. However, this thesis is the first to point out that there is no self-voltage-equalization mechanism in the diode-clamped multilevel converter. For this reason, the dc capacitor voltages will naturally diverge. Since the total dc voltage is regulated, the voltage collapse in one level leads automatically to overvoltage, and in consequence, valve failures at another level.

As a matter of fact, one referee of the first submission of [46], rejected the manuscript because he insisted that the dc capacitors must be naturally equalized and the

authors were fussing over a non-problem. The objections were overcome upon a resubmission containing digital simulations pointing to dc voltage divergences, in the absence of equalization feedback control. This rejection caused a delay of several months, by which time the research group from Oak Ridge National Laboratory claimed a prior publication date. When laboratory multilevel facilities were available at a later date, the voltage divergence was proved experimentally.

The early recognition that the multilevel converter will malfunction, in the absence of self-voltage-equalization mechanism, has led to a major research effort in finding feedback schemes for the equalization of the dc capacitor voltages at the different levels. The voltage equalization is considered as a sine-qua-non of the diode clamped multilevel converter because: (1) it guards the GTOs against failures from overvoltages, and (2) it guarantees the low Total Harmonic Distortions because the equal DC capacitor voltages constitute the basic assumptions of the Fundamental Frequency Switching (Selective Harmonic Elimination) strategy.

In addition to finding relatively fast, and stable equalization feedbacks for the Fundamental Frequency Switching strategy, chapter 3 has also succeeded for the Sinusoidal Pulse Width Modulation strategy. This stage of the research has taken a long time, because the problem is highly nonlinear. In addition, inherent third harmonics ride on each of the dc capacitor voltages so that the feedback loops must face the difficult problem of discriminating of the dc signal from the unwanted third harmonic noise.

Chapter 4:

From the successes in safeguarding the multilevel shunt STATCOM with equalized currents and equalized voltages in chapters 2 and 3, the research in chapter 4 takes up the challenge of solving the problems in making the diode-clamped multilevel converters operate as a back-to-back rectifier/inverter pair in a dc link. From the experiences in the digital simulations, it was soon recognized that in using the Fundamental Frequency Switching strategy, the ac-side voltages of both the rectifier and the inverter must be equal in magnitude for the dc link voltages to be equalizable by feedback control, as in the case of the shunt STATCOM of chapter 3. This constrictive requirement has been proved mathematically in the chapter. The practical implication is that multilevel versions of the FACTS controllers such as the Unified Power Flow Controllers (UPFCs) and the Asynchronous Link, which are based on the back-to-back dc link, will have to operate with ac voltages whose magnitudes must form fixed ratios. This reduces the control degrees of freedom so that the vaunted ability to control independently the real power and the reactive power on both sides, is compromised.

Faced with this impasse, the research adopts a system of Class B choppers which equalizes the dc capacitor voltages by transferring the electric charges from the dc capacitors with higher voltages to their immediate neighbours with lower voltages, using local feedback control. The preliminary study results have shown that the current ratings of GTOs of the choppers are less than 0.1 p.u. and their switching rates are about one pulse per line frequency cycle, so that their cost is only around 10% of the rectifier (or

inverter) and their switching rates are comparable to the rectfier/inverter pair . The 10% increase in cost is considered to be justifiable for the regain of full flexibility in the UPFC and the Asynchronous Link.

In addition to proof of concept by digital simulation tests, the concept has been proven experimentally with laboratory choppers controlled by a software driven platform consisting of digital signal processors (DSPs) and field programmable gate arrays (FPGAs).

Chapter 5

Chapter 5 presents the results of a study of the integrated, Class B Chopper stabilized, diode-clamped, multi-module, multilevel Unified Power Flow Controller. The simulations show that fast, independent controls of the real power and the reactive powers on both sides of the UPFC are achievable. The simulation results of the multilevel Asynchronous Link are also shown in this chapter.

Chapter 6

Chapter 6 presents a summary of the results of the research, the conclusions of the thesis and suggestions for further work.

CHAPTER TWO

MULTIMODULES OF DIODE-CLAMPED MULTILEVEL CONVERTERS AND THEIR SWITCHING ALGORITHMS

2.1 Introduction

High MVA realizations of the FACTS controller using GTOs must circumvent the limited voltage and current ratings of GTOs available [9,52]. It has been recognized that the multilevel converter can reach higher voltage ratings by adding voltage levels. The GTO at each of the multilevels is stressed by the dc voltage across the dc link capacitor of the corresponding level. The GTOs are evenly stressed when all the dc link capacitors are charged equally to the same safe voltage.

The multilevel approach offers two other advantages. Firstly, as the GTOs at each level do not have to switch simultaneously, their switching instants can be designed so that selected low order harmonics can be eliminated. Secondly, after the unwanted low

frequency harmonics are cancelled as voltages in the serially connected multilevels, the residual high frequency harmonics currents can be diminished by relatively small (and cheap) filter inductances.

However, its application is still limited by the individual GTO current ratings. In order to overcome the limitation of the individual GTO current ratings, several modules of multilevel converters [47-50] can be connected in parallel to achieve higher current ratings without increasing the individual GTO current rating. This idea has evolved from the success of multiple modules of 2-level converter [9,25] in application where the voltage rating or the current rating exceeds the capability of a single module. The HVdc thyristor bipole station, consisting of 4 units of three-phase thyristor bridges connected in series to increase the voltage rating, is an example of the multimodular approach. The examples in the GTO era are found in the 100 MVA-size STATCOM prototypes in USA [9,10] and Japan [17] which consist of 8 units of 3-phase voltage-source, GTO bridges in parallel. In the first example, there are two transformer stages. One stage is for matching the low voltages of the converters to the high voltages of the transmission line. The second transformer stage is for the purposes of harmonic cancellations of switching harmonics and equalization of the currents in the parallel modules. This chapter shows that the second transformer stage is unnecessary as the multimodular multilevel FACTS controllers can perform both tasks. The first transformer stage is also not needed in low distribution ac voltages, around 15 kV.

This chapter will focus on the topology of the multimodules of the diode-clamped multilevel converters [47-50]. The research addresses the switching algorithms for harmonics elimination, ac voltage magnitude control and ac current equalization. The study will show how it is suited for application as FACTS controllers.

2.2 Multimodular Multi-level Converter

Fig.2-1(a) shows the example of a 7-level converter and Fig.2-2 illustrates the

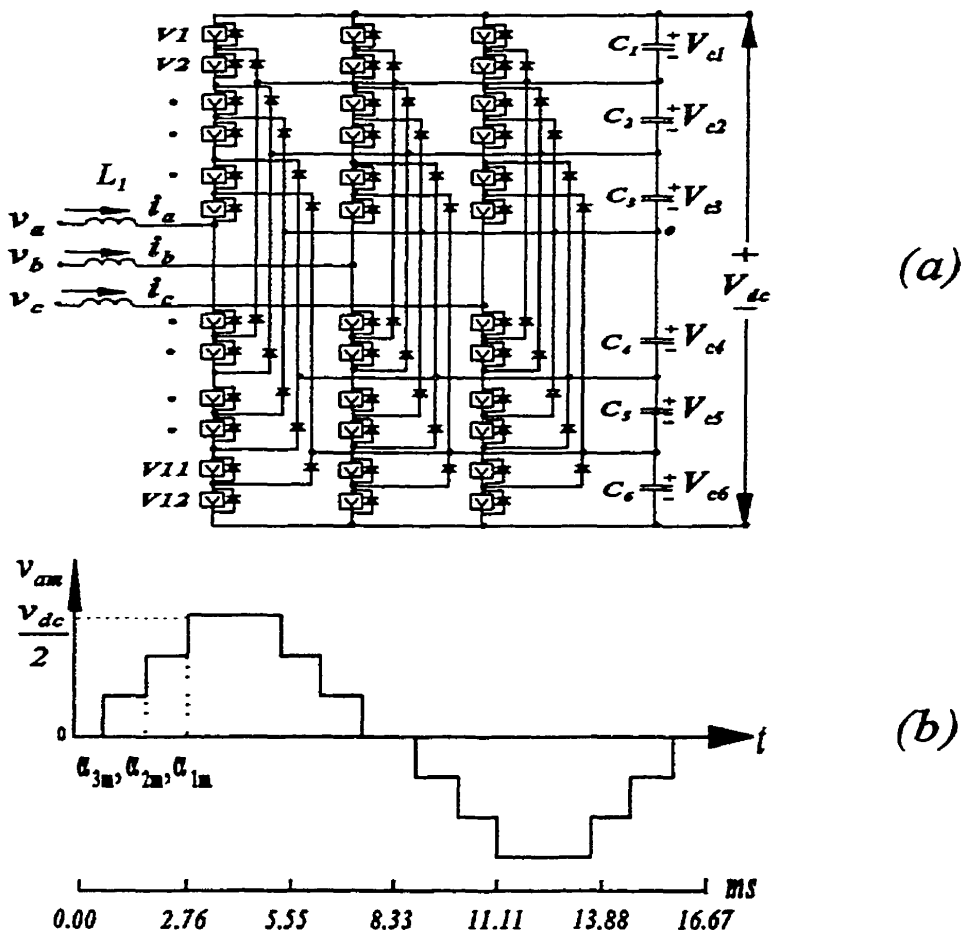

Fig.2-1 (a) Diode-clamped 7-level converter module, (b) voltage waveform of a-phase under fundamental frequency switching strategy.

specific case of 2-module configuration. From the conclusions of this case study, it should be possible to generalize the conclusion from the specific case-study to the M-modules, N-level converter station. The critical features as illustrated in Fig.2-2 are: (1) On the ac side, the three phases including the filter inductance L_1 of the individual modules are terminated at 3 nodes. The a-phase input current, for example, is branched into the two modules as i_{a1} and i_{a2}. The requirement that the GTOs of the a-phase of Fig.2-2 of module m=1 shares the same load as the module, m=2, implies that the rms values of i_{a1} and i_{a2} must be equal. (2) On the dc side, the 7 dc buses of each module are connected in parallel so as to share the dc link capacitors C_1, C_2 , ... ,C_6. The GTOs of both modules at the same level are bracketed between the terminals of the same capacitor C_j (j=1,2 ... 6) and their voltage stresses are determined by the capacitor voltage V_{cj}(j=1, 2 ... 6). Equalization of the voltage stress requires that V_{cj}=(V_{dc}/6) (j=1,2 ... 6). As will be discussed in chapter 3, active

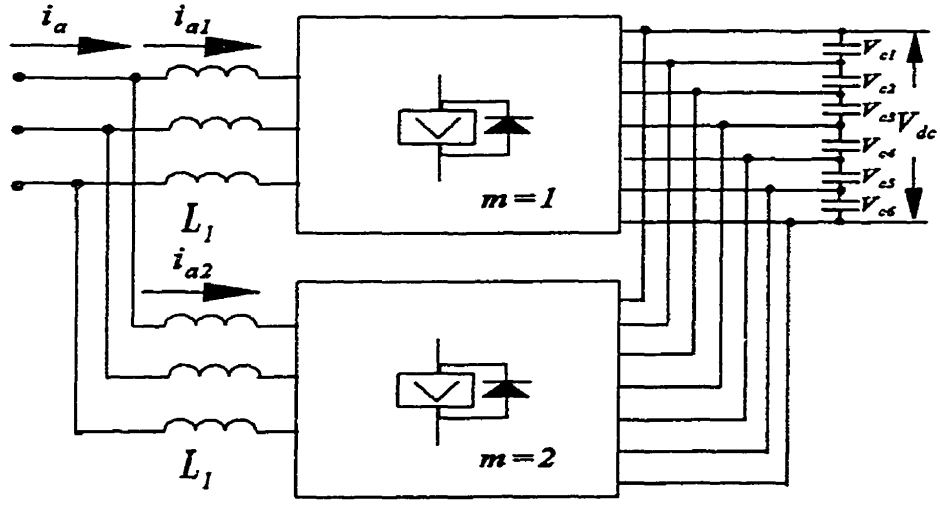

Fig.2-2 Multimodular Multilevel Converters - case study:M=2, N=7.

equalization by the control of the switching instants of the GTOs is more efficient than the passive equalization introduced in chapter 4 as it does not incur the additional losses through the resistances of the equalization circuits. However, under the assumption that the equal and regulated dc voltage sources are available, the switching algorithms described in this chapter are also required to meet other basic functions of the FACTS controller which are:

(i) achieving low total harmonic distortion (THD) factors in the ac voltages and the currents.

(ii) achieving a range of voltage amplitude control.

In the fundamental frequency switching strategy, the requirement of the quarter wave symmetry in the waveform as illustrated in Fig.2-1(b) allows only 3 switching degrees of freedom for the 7-level converter. In general, the odd number N-level offers $J=(N-1)/2$ switching degrees of freedom for control. Multiple modules could be used to increase the degrees of freedom. Thus the six switch angles α_{1m}, α_{2m}, α_{3m} (m=1,2) from 2 modules can be applied to eliminate unwanted low harmonics and to specify the magnitude of the fundamental component [34,48,49]. The elimination of selected harmonics contributes towards meeting THD standards. The ability to specify the fundamental component enables the reactive power (VAr) control for the STATCOM [34] and phase-shift control for the UPFC [49]. The fundamental voltage harmonic in each module can also be specified for the purpose of equalization of the ac currents.

2.3 Fundamental Frequency Switching Strategy Design

The Sinusoidal Pulse Width Modulation (SPWM) strategy has been widely used in the control of converters for medium-power industry application. For utilities application, however, the Fundamental Frequency Switching strategy [30-32] is preferred because it requires only one switching at each cycle of the utility standard frequency. In the literatures [30,36], the independent switching instants of multilevel converter are applied to eliminating harmonics. The output ac voltage magnitude has to be regulated by controlling the total dc capacitor voltage, which is usually slow in response. Furthermore, the control by dc capacitor voltage limits the application of the multilevel converter to STATCOMs only where there is no other converter connected to the dc link. For other applications which require a rectifier/inverter link [11-16], control by the dc capacitor voltage means that the ac magnitude of the rectifier must be at a fixed ratio to that of the inverter. For independent control over the two ac voltages, it is necessary to control ac magnitude by designing the switching instants.

In the 2-module example of Fig.2-2, there are 6 degrees of freedom in the design of the switching strategy which can be used to perform the following functions:

(1) controlling the magnitude of the fundamental harmonic of the ac output voltage,

(2) eliminating the 5th, 7th, 11th and 13th harmonics,

(3) balancing the rms currents in the two modules.

Using the Fourier Series Analysis of the waveform of Fig.2-1(b), the kth harmonic

of the mth module is

$$V_{km} = \frac{4V_{dc}}{3k\pi}[\cos k\alpha_{1m} + \cos k\alpha_{2m} + \cos k\alpha_{3m}] \quad (2\text{-}1)$$

for k=1,3,5,7 ... m=1,2.

2.3.1 AC Voltage Magnitude Control

In controlling the equivalent ac output magnitude V_1 of the converter station, the fundamental component (k=1) of module m=1 must be

$$V_{1,1} = \frac{4V_{dc}}{3\pi}[\cos \alpha_{11} + \cos\alpha_{21} + \cos\alpha_{31}] = V_1 \quad (2\text{-}2)$$

and of module m=2

$$V_{1,2} = \frac{4V_{dc}}{3\pi}[\cos \alpha_{12} + \cos\alpha_{22} + \cos\alpha_{32}] = V_1 \quad (2\text{-}3)$$

Equation (2-2) and (2-3) leave 4 remaining degrees of freedom for the design of the waveforms.

2.3.2 Elimination of 5th, 7th, 11th and 13th Harmonics

As even and triplen harmonics cannot exist, the 4 lowest harmonics are the 5th, 7th, 11th and 13th, which are eliminated by setting

$$V_{k1} + V_{k2} = 0 \quad (2\text{-}4)$$

substituting equation (2-1), one has

$$\sum_{m=1}^{2}(\cos k\alpha_{1m} + \cos k\alpha_{2m} + \cos k\alpha_{3m}) = 0 \qquad (2\text{-}5)$$

for k =5, 7, 11, 13.

2.3.3 Balancing Currents in Individual Modules

The rms values of the two modules are balanced when the summation of the squares of the harmonic voltages k=1, 5, 7, 11 and 13 of module m=1 is equal to the summation of the same harmonics in module m=2. Mathematically, this means that

$$I_{1,1}^2 + I_{5,1}^2 + I_{7,1}^2 + I_{11,1}^2 + I_{13,1}^2 = I_{1,2}^2 + I_{5,2}^2 + I_{7,2}^2 + I_{11,2}^2 + I_{13,2}^2 \qquad (2\text{-}6)$$

Neglecting resistance in the filter inductance, (2-6) implies:

$$V_{1,1}^2 + \frac{V_{5,1}^2}{5^2} + \frac{V_{7,1}^2}{7^2} + \frac{V_{11,1}^2}{11^2} + \frac{V_{13,1}^2}{13^2} = V_{1,2}^2 + \frac{V_{5,2}^2}{5^2} + \frac{V_{7,2}^2}{7^2} + \frac{V_{11,2}^2}{11^2} + \frac{V_{13,1}^2}{13^2} \qquad (2\text{-}7)$$

From (2-2) and (2-3), one sees that

$$V_{1,1}^2 = V_{1,2}^2 \qquad (2\text{-}8)$$

and from (2-4), since

$$V_{k,1}^2 = V_{k,2}^2 \qquad (2\text{-}9)$$

for k=5, 7, 11, 13.

from (2-7) to (2-9), one sees that (2-6) is already satisfied.

2.3.4 Residual Harmonic Currents

Since $/cosk\alpha_{im}/ < 1$ (i=1,2,3), it follows from (2-1) that the kth harmonic voltage of the mth module satisfies the inequality

$$V_{km} \leq 4\frac{V_{dc}}{k\pi} \tag{2-10}$$

As the filter reactance with respect to the kth harmonic is

$$X_k = jk\omega L_1 \tag{2-11}$$

the magnitude of the kth harmonic current is

$$/I_{km}/ < \frac{V_{km}}{/X_k/} < \frac{4V_{dc}}{k^2\omega L_1} \tag{2-12}$$

As $|I_{km}|$ in (2-12) varies inversely with k^2, the square of the harmonic number, the harmonic current diminishes rapidly with increasing k. Furthermore, as even and triplen harmonics do not exist, the lowest harmonics number not already considered in the equalization of the rms voltage is k=17. From (2-12), it is clear that the filter inductance L_1 can be quite economically sized without causing noticeable unbalance.

2.3.5 Solutions of Transcendental Equations

The 6 unknown switch angles α_{im} (i=1,2,3; m=1,2) in the 6 transcendental equations of (2-2), (2-3) and (2-5) are solved numerically using Matlab Software. The solutions are listed in Table 2-1 and Appendix B and plotted as a function of V_1 in

Table 2-1 Switching Angles

		Switching angles					
index	V_1(pu)	α_{31}	α_{21}	α_{11}	α_{32}	α_{22}	α_{12}
1	0.48	35.36°	72.84°	88.00°	47.03°	58.70°	90.00°
2	0.52	35.41°	70.10°	85.80°	45.95°	57.50°	90.00°
...	...	...	...	...	...	...	...
49	0.96	20.28°	27.04°	64.00°	9.28°	43.23°	57.00°
50	0.98	18.58°	25.13°	62.50°	8.77°	39.48°	56.20°

Fig.2-3(a). The look-up table of Table 2-1 is used for real-time control of the ac voltage magnitude.

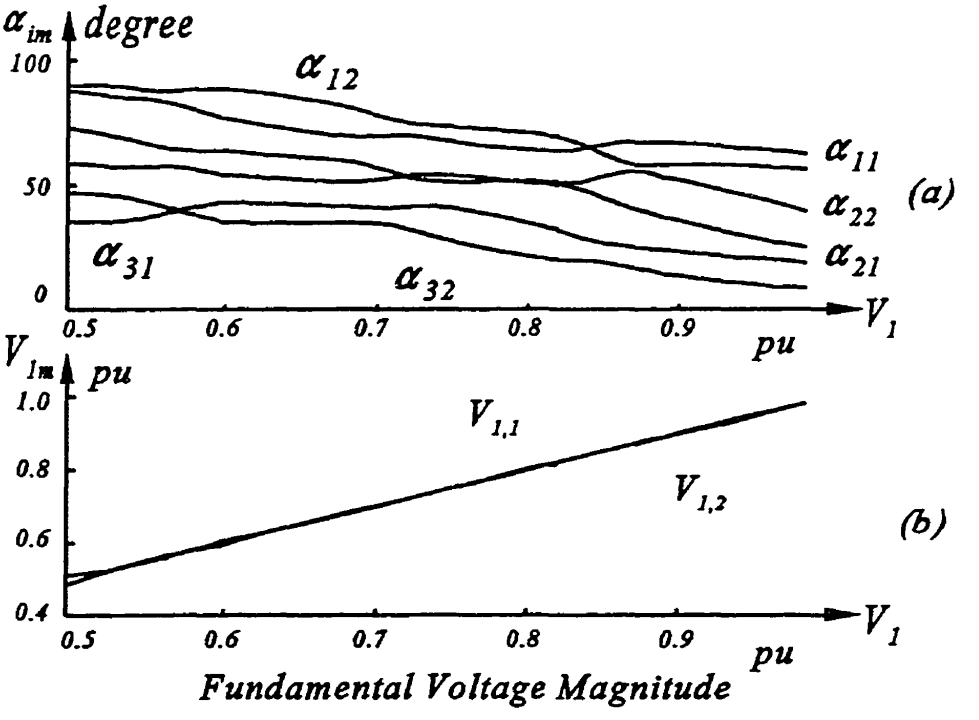

Fig.2-3 (a) Switching angles-vs-ac voltage magnitude, (b) fundamental voltage of individual module vs terminal voltage magnitude.

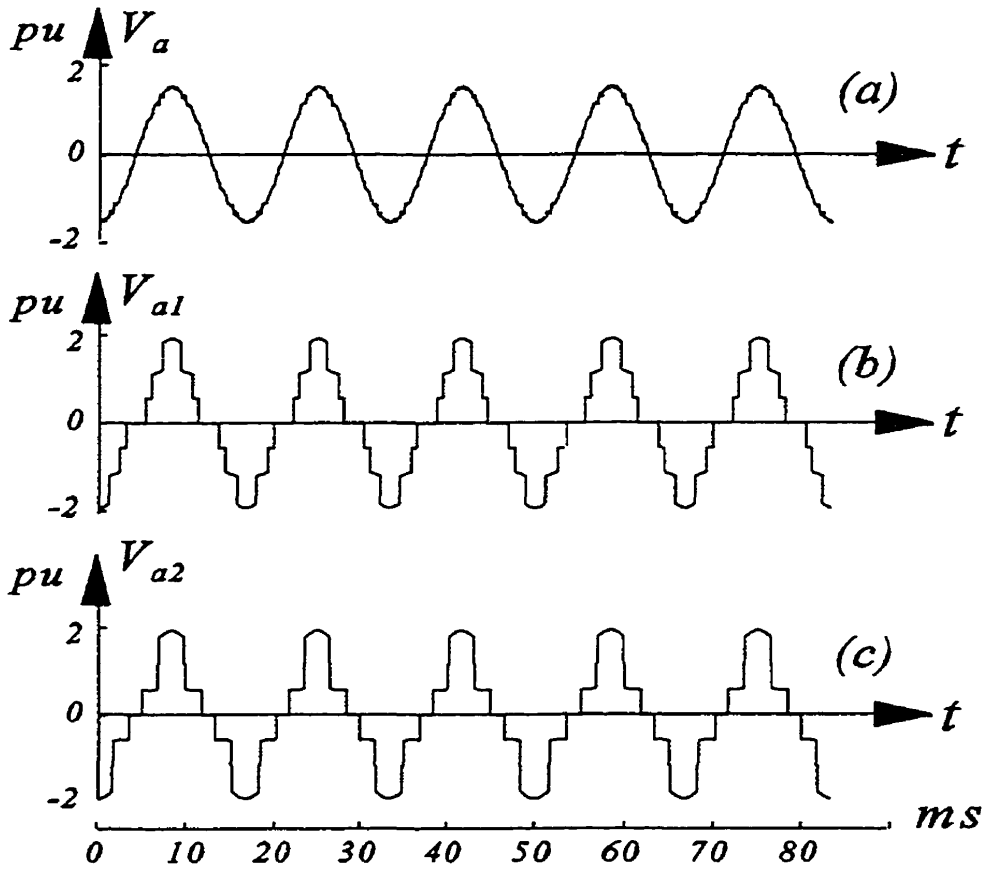

Fig.2-4 Steady-state voltage: (a) average, (b) module 1, (c) module 2.

Fig.2-3(b) displays $V_{1,1}$ and $V_{1,2}$, the fundamental Fourier component of the voltage from module m=1 and m=2, which are based on the solutions of α_{im} (i=1,2,3; m=1,2), in the range of $0.5 < V_1 < 1.0$ p.u. One sees $V_{1,1}$ and $V_{1,2}$ are almost equal so that (2-2) and (2-3) are satisfied, and thus the two modules share the load currents for the range of voltage magnitudes.

2.3.6 Voltage and Current Waveforms

Fig.2-4(a) shows the simulated line-to-neutral ac output of one phase V_a . The

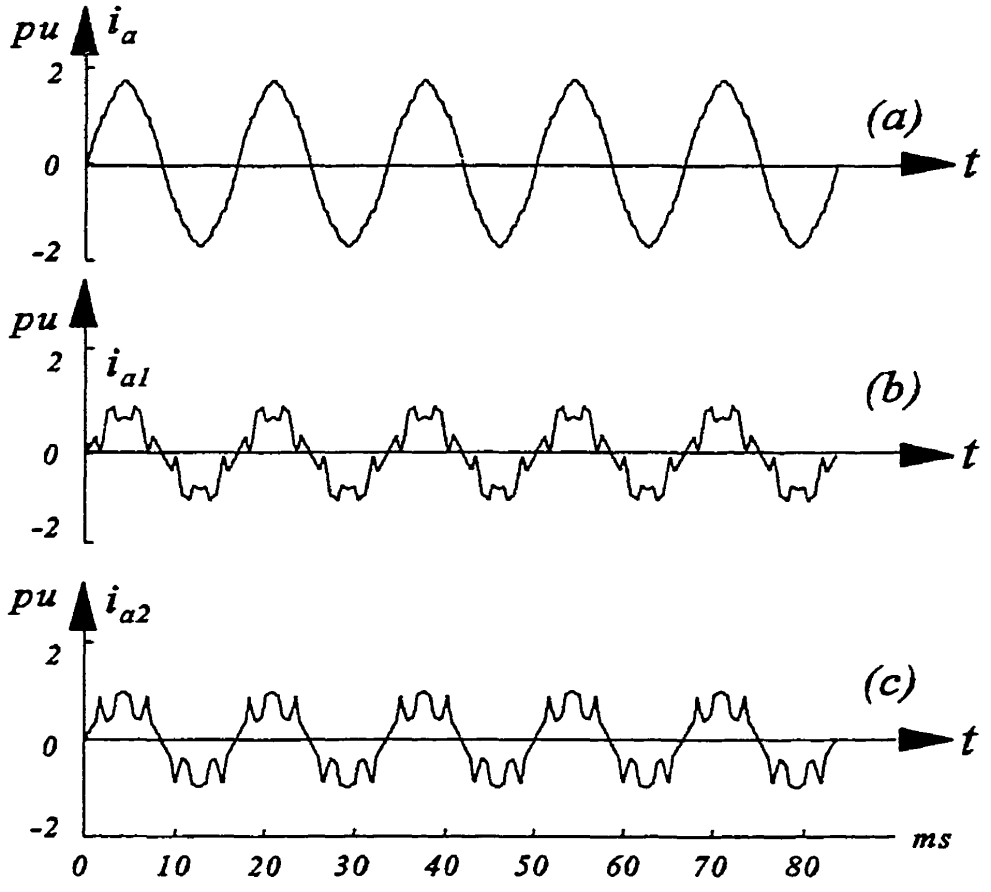

Fig.2-5 Steady-state current: (a) total, (b) module 1, (c) module 2.

voltage waveforms of the individual modules are shown in Fig.2-4(b) and (c) when the switching angles are determined by Fig.2-3(a) which contains the specification that the fundamental harmonic components of the voltage are equal. The total line current i_a is a high quality sinusoidal waveform as shown in Fig.2-5(a). The currents i_{a1} and i_{a2} in the two modules m=1 and m=2 are shown in Fig.2-5(b) and (c) for steady-state operating condition of capacitive rated current. The THD of V_a and i_a are 5.5% and 3.0% respectively. The current i_{a1}, i_{a2} in the individual modules contain large 5th, 7th, 11th and 13th harmonics

which are equal and opposite so that they eliminate each other in i_a. The fundamental harmonic currents are equal from the design specification.

2.3.7 Verification of Current Balancing

Fig.2-6 displays the rms value of the current i_{a1} and i_{a2}, obtained from simulation runs and plotted against the MVA of the converters operated as a shunt STATCOM. Positive MVA is for operation as a capacitive reactance. The small unbalance is due to the residual high harmonic currents. The condition of current equalization of (2-6) is satisfied.

2.4 Extension to *M* Modules of *N*-Level Converter

From the specific case of designing the switching angles of 2 modules of 7-level

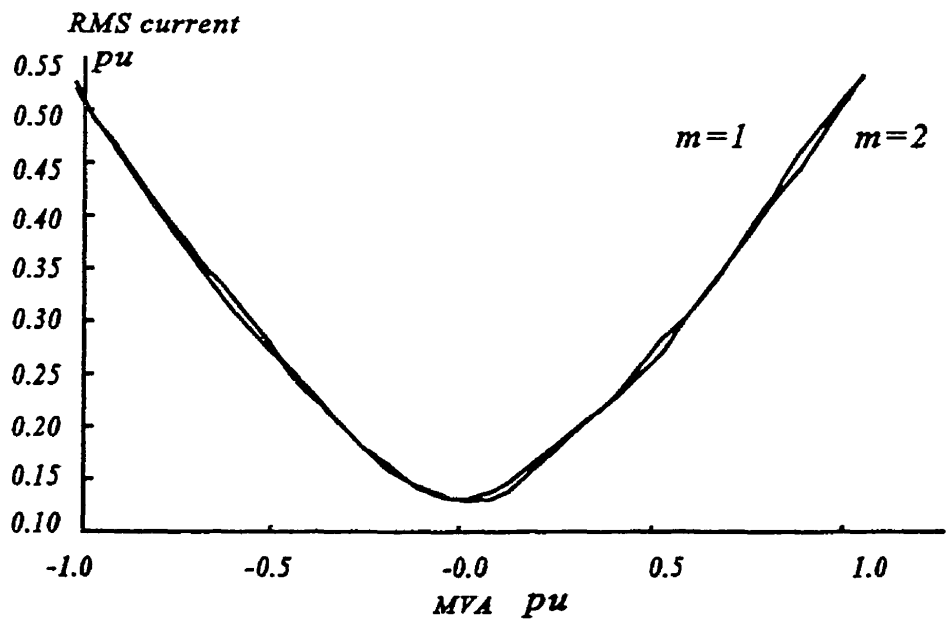

Fig.2-6 RMS currents in modules-vs-MVA.

converters, this section extends the method to cover the general case of M-module of N-level converter.

For M modules of N-level converter, there are ($M \times J$) independent switching angles α_{im} (i=1,2 ... J, m=1,2, ... M,) where $J=(N-1)/2$

For the mth module, the kth harmonic is:

$$V_{km} = \frac{4V_{dc}}{3k\pi}\sum_{i=1}^{J}\cos k\alpha_{im} \tag{2-13}$$

M equations are required to specify the variable magnitude V_1 of the fundamental harmonic as in (2-2) and (2-3). The M equations for this are

$$V_{1m} = V_1 \tag{2-14}$$

for m=1, 2 ... M, one equation for each module.

(M-1) equations are required to specify the balancing of the rms voltages in each module as in (2-6). The summation of the squares of the harmonic voltages up to $k=K$, (where K is the highest harmonic which will be eliminated) in the *mth* module is

$$T_m = I_{1,m}^2 + I_{5,m}^2 + I_{7,m}^2 + \ldots + I_{K,m}^2 \tag{2-15}$$

$$S_m = \omega^2 L_1^2 T_m = V_{1,m}^2 + \frac{V_{5,m}^2}{5^2} + \frac{V_{7,m}^2}{7^2} + \ldots \frac{V_{K,m}^2}{K^2} \tag{2-16}$$

As even and triplen harmonics are not present, the harmonics k in V_{km} which are to be eliminated are $k=6q-1$ and $k=6q+1$, where $q=1,2,3$ ...

Based on constraining S_m of (2-16) to be equal in all the M modules, (M-1)

equations are obtained:

$$\begin{aligned} S_2 &= S_1 \\ S_3 &= S_1 \\ &\vdots \\ S_M &= S_1 \end{aligned} \tag{2-17}$$

The number of equations which are already constrained by (2-14) and (2-17) are $(2M\text{-}1)$ of the original $(M\times J)$ degrees of freedom. This leaves $(J\text{-}2)M+1$ equations of the form

$$\sum_{m=1}^{M} V_{km} = 0 \tag{2-18}$$

to eliminate harmonics in the series k=5, 7, 11, 13 ... $6q$-1, $6q$+1, ...K, which are the odd, non-triplens.

Substituting (2-13) in (2-18), one has $(J\text{-}2)M+1$ equations of the form:

$$\sum_{i=1}^{J}\sum_{m=1}^{M} \cos k\alpha_{im} = 0 \tag{2-19}$$

The $(M \times J)$ angles α_{im} are solved from (2-14), (2-17) and (2-19) using a numerical routine in MATLAB. The results can be stored in a table like that of Table 2-1 for real-time control of the output ac voltage magnitude, meanwhile maintaining the elimination of $(J-2)M+1$ harmonics in the equivalent output voltage waveform and the equalization of current loads among individual modules.

2.5 Conclusions

This chapter begins from the special case of 2 modules of 7-level diode-clamped converter. The case study is simple enough to illustrate the design issues of control under fundamental frequency switching strategy. The number of voltage levels in each module and the number of modules can be selected to make its output voltage and current ratings meet high MVA requirements. It has been shown that multiple modules increase the degrees of freedom in the design of the GTO switching angles which can be exploited to accomplish 3 major tasks simultaneously: (1) to achieve low THDs in voltages and currents, (2) to achieve direct, fast control of output voltage magnitude, which does not depend on the charge and discharge of the dc capacitor, and (3) to achieve equalization of rms current in the separate modules. The 2-module, 7-level example has been extended to *M*-module, *N*-level. FACTS controllers based on multimodular diode-clamped multilevel converters can take advantage of the switching algorithm to implement the multiple control goals in the chapters to follow.

CHAPTER THREE

REGULATING AND EQUALIZING DC CAPACITOR VOLTAGES IN MULTILEVEL STATCOM

3.1 Introduction

Chapter 2 has shown how the switching angles α_{im} of Fig.2-1(b) in multi-level converter can be used to attain three objectives: (1) suppression of selected low harmonics so that the residual voltage waveforms contain dominant fundamental frequency component (low total harmonic distortion,) (2) direct control of the magnitude of the fundamental frequency components in designs involving multiple modules of multi-level converters, and (3) equalization of rms current in the separate modules. Chapter 2 has exhausted all the degrees of freedom in the choice of the switch angles α_{im} in the quarter symmetry of the fundamental frequency switching strategy. The switch angles α_{im} are "frozen" in the "look-up tables". The remaining flexibility consists of : (4) phase-shifting

the "frozen switch angles" with respect to the voltage angle of the electric utility system [53] and this is used in this chapter to regulate the total dc link voltage, (5) sliding the "frozen" switch angles of the different levels with respect to each other to charge or discharge the dc capacitors [33,36,46] differentially and this is used to equalize the dc capacitor voltages in the different levels.

The principles of dc capacitor voltage regulation and equalization are explained in full in the context of the Fundamental Frequency Switching strategy. This chapter also includes the simulation results from another strategy, namely the Sinusoidal Pulse Width Modulation (SPWM) strategy. To avoid another lengthy exposition, only the simulation results of the SPWM strategy are presented. As in chapter 2, the application example chosen is the shunt STATCOM. The GTO is envisaged as the valve chosen for this application.

This chapter addresses the methods to regulate and equalize the dc capacitor voltages so that the multilevel STATCOM can exist as a stand-alone entity. DC capacitor voltage equalization is necessary to share the voltage stresses of the GTOs evenly. It is useful to be reminded that the harmonic elimination strategy, the ac voltage magnitude control and the current equalization method described in chapter 2 assume ideal, equal, dc voltages so that the realizability of the assumptions affects the quality in the performance of the multilevel converter for application in FACTS controllers. The dc voltages have to be obtained by charging the dc link capacitors by power rectified from the ac system. Even when the total dc voltage is regulated, the cumulative effects of (1)

capacitor leakage currents, (2) unequal delays in GTO switchings and (3) asymmetrical charging of the capacitors during transients and disturbances, all contribute towards the divergence of the capacitor voltages, resulting in the voltage collapse of some and the overcharging of others.

The goal in this chapter is to demonstrate, through digital simulations of a 7-level diode clamped inverter (DCMLI) in section 3.4 and multimodular of 7-level converters in section 3.5, that the controls to the GTOs are adequate for the task of regulating and equalizing the dc capacitor voltages for STATCOM application. The task is complex because it involves control of multivariables. Furthermore, the functions of regulating and equalizing are not clearly decoupled. It should be mentioned that "voltage balancing circuits" have been proposed in [39]. They serve virtually as choppers to transfer the electric charges from the dc capacitors with high voltages to boost the capacitors with low voltages. The chopper-based equalization control will be explored in details in chapter 4 for the case of back-to-back dc link application of multilevel converter. The goal of this chapter is to find solutions based entirely on the control of the GTOs of the multilevel converter.

The 7-level converter has been chosen because it exemplifies a high degree of complexity without incurring the excessive computational costs of still higher levels. As there have already been results of studies reported on the diminution of component sizes with respect to meeting Total Harmonic Distortion Standards [30,31], the main thrust of this part of research is on the methods of regulating and equalizing the dc capacitor

voltages for two different schemes of controlling the multilevel STATCOM:

1. *Fundamental Frequency Switching* strategy, which is the method of the existing STATCOMs [52,54-56] as it requires the GTOs to switch at 1 pulse per line cycle, the switching loss is minimum.

2. *Sinusoidal Pulse Width Modulation (SPWM)* strategy, which requires a higher switching rate of at least 8 pulses per cycle of the line frequency. The switching loss is not acceptable for presently available GTOs and the flexibility and advantages, which come with SPWM, will have to wait for improved, faster GTOs.

3.2 Multilevel STATCOM

Fig.3-1 shows the detail schematic of the 3-phase, 7-level, diode-clamped

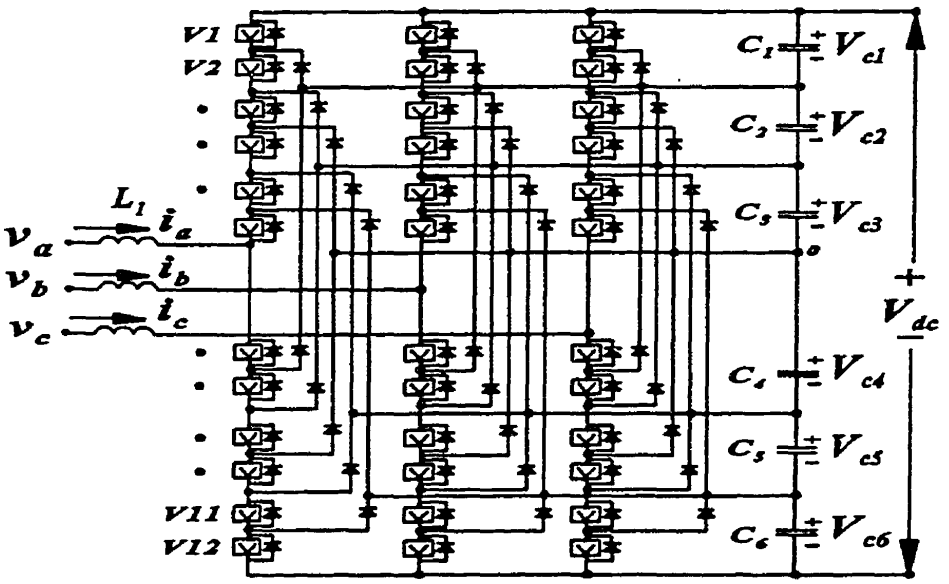

Fig.3-1 3-phase, 7-level diode-clamped converter.

converter. Its operating principles have already been described previously [28-30] with the assumption that the dc voltages $V_{c1}=V_{c2}=...=V_{c6}$ are available as ideal voltage sources. For stand-alone operation, the dc voltages must be derived from the real ac power taken from the ac terminal voltages, which after rectification, is directed to charging the dc capacitors at 6 levels: C_1, C_2, ... C_6. The real ac power must be just sufficient to charge the capacitor voltages and to replenish all dissipative losses in the GTOs, in the leads and in the capacitor leakages. The control is accomplished through a dc voltage regulation feedback loop and, in principle, this is not different from the method already in use in the existing STATCOMs [55,56] and in the PWM-SVCs [27,30]. In the multilevel converter, however, there is the additional requirement to equalize the voltages in all the dc

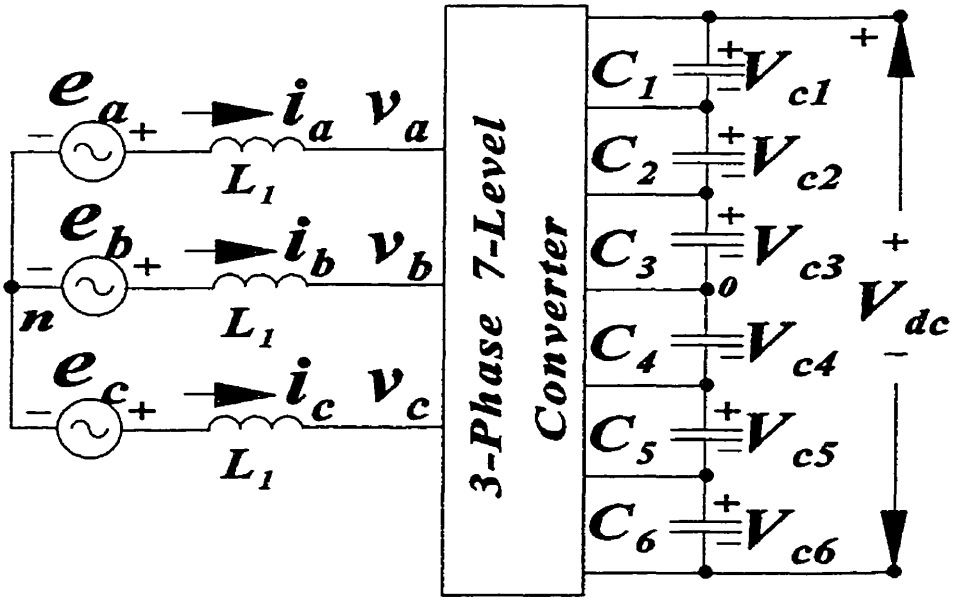

Fig.3-2 3-phase, 7-level converter connected to an ac system.

capacitors: $V_{c1}=V_{c2}=...=V_{c6}=V_{dc\_ref}/6$.

3.2.1 Single Module of Multilevel Converter

The detail schematic of Fig.3-1 is represented by a simplified block diagram shown in Fig.3-2. Fig.3-2 shows the external features: (1) on the ac side, the three phases are connected to the ac network of the electric utility which is represented by the Thevenin voltages e_a, e_b, e_c and Thevenin inductance L_1, (2) on the dc side, the 7 dc buses of each module are connected to the dc link capacitors C_1, C_2 , ... , C_6. The voltage stresses of

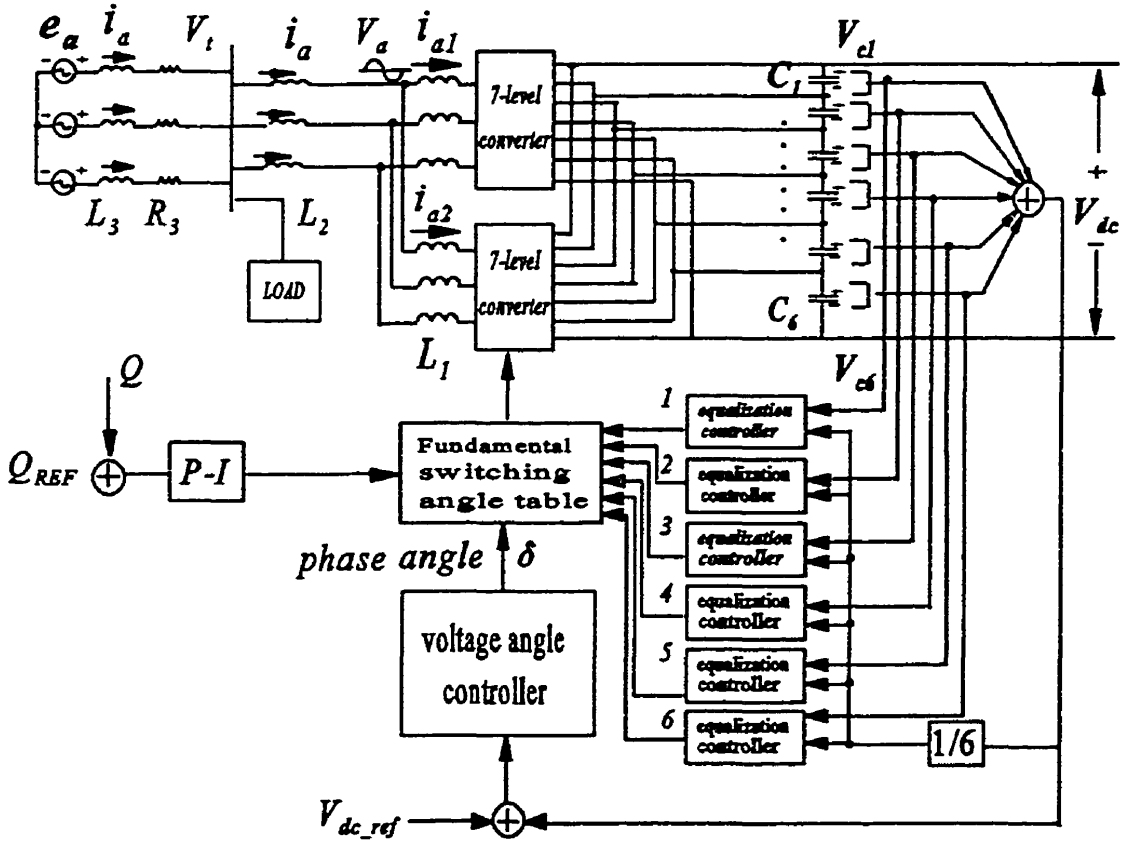

Fig.3-3 STATCOM based on 2 modules of 7-level converter with 3 regulation feedback control loops.

GTOs are determined by the capacitor voltage V_{cj}(j=1, 2 ... 6). Equalization of the voltage stress requires that $V_{cj}=(V_{dc}/6)$ (j=1,2 ... 6). Active equalization by the control of the switching instants of the GTOs is more efficient than passive equalization as it does not incur the additional losses through the resistances of the equalization circuits.

3.2.2 STATCOM Based on Multimodules of Multilevel Converter

Fig.3-3 displays the STATCOM based on 2 modules of 7-level converter with 3 regulation feedback control loops. As described in chapter 2, the six switch angles α_{1m}, α_{2m}, α_{3m} (m=1,2) from 2 modules are applied to eliminate unwanted low harmonics, to equalize the load current between the two modules and to specify the magnitude of the fundamental component. The elimination of selected harmonics contributes towards meeting low Total Harmonic Distortion standards. The ability to specify the fundamental component enables the reactive power (VAr) to be controlled. As shown in the block diagram of Fig.3-3, the reactive power Q is measured, compared with the reference Q_{REF} and the error after the passing through a proportion-integral block is used to vary V_1, the magnitude of the fundamental voltage harmonic. This is accomplished by accessing from the "look-up" table the switching angles α_{im} which correspond to the desired voltage magnitude.

Once the switch angles are fully specified, the remaining control freedom is the phase angle of the voltage waveform of Fig.2-1(b) with respect to the phase angles of the Thevenin voltages e_a, e_b and e_c. The phase angle control is employed to regulate the

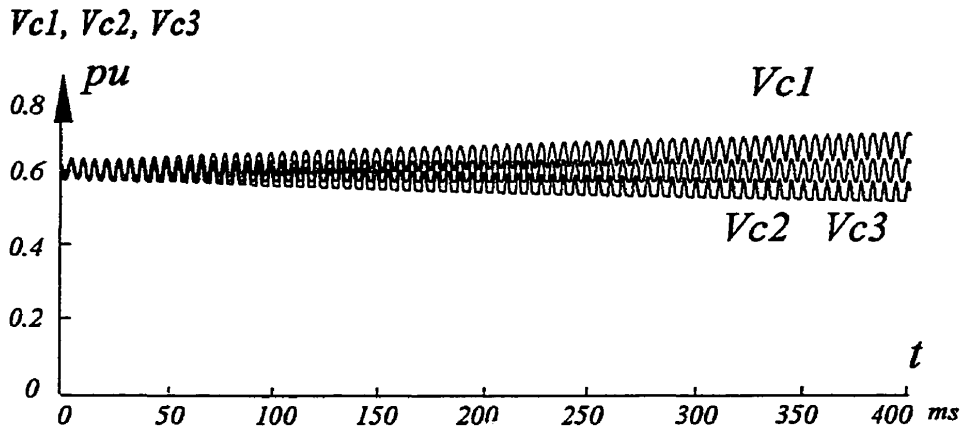

Fig.3-4 Test of dc capacitor voltages without equalization feedback control.

total dc voltage V_{dc}.

The outer feedback loop of Fig.3-3, however, exercises no control over the individual capacitor voltages, and normally the capacitor voltages diverge as the digital simulation of Fig.3-4 shows. This has been confirmed in laboratory experiments. As the total voltage V_{dc} is regulated, this has the implication that as some capacitor voltages collapse, others will increase beyond the safe voltage limits of the GTOs. For this reason, the switching instants of the GTOs in each of the capacitor level will be phase-shifted to equalize the individual dc capacitor voltages.

3.3 Control of Capacitor Voltages

3.3.1 DC Voltage Regulation by Voltage Angle Feedback Loop

Representing the fundamental Fourier Series component of the multilevel

converter voltage v_a by the phasor $\tilde{V}_a$, the Thevenin voltage e_a by the phasor $\tilde{E}_a$ and the phase current i_a by the phasor $\tilde{I}_a$, the general phasor diagram for the operation of Fig.3-2 is shown in Fig.3-5(a). The line current is

$$\tilde{I}_a = \frac{\tilde{E}_a - \tilde{V}_a}{jX_L} \tag{3-1}$$

and it makes an angle φ with respect to $\tilde{V}_a$. The ac power entering the converter is

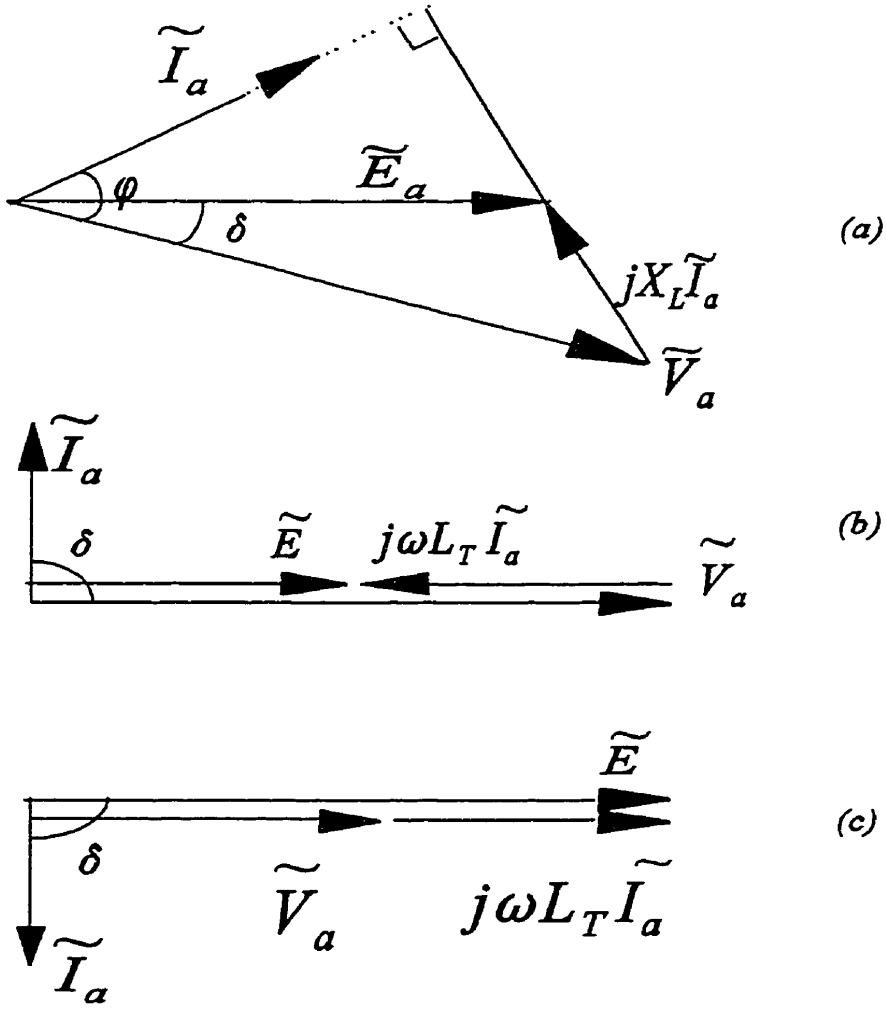

Fig.3-5 (a) General phase diagram of Fig.3-2, (b) STATCOM as inductive reactance, (c) STATCOM as capacitive reactance.

$$P_{ac}=\frac{3|\tilde{E}_a||\tilde{V}_a|\sin\delta}{X_L} \tag{3-2}$$

and after deducting for the losses in the GTOs, the diodes and the capacitor leakages, the remainder goes to charging the storage energy of the capacitors. Once the dc voltage V_{dc} has risen so that the error $\epsilon_{dc}=V_{dc\_ref}-V_{dc}$ with respect to the reference, V_{dc_ref}, is nulled, then the charging can be terminated. Since the losses are low, the error null situation implies that $cos\varphi\approx 0$ or $\varphi\approx+90°$ or $-90°$.

In the highly inductive electric utility environment, the voltage angle δ is the control lever of real power and by advancing the voltage angle of $\tilde{V}_a$, the phasor diagram of Fig.3-5(a) can be shifted to the form of Fig.3-5(b) or (c), which are the STATCOM operating conditions of $\varphi=90°$, with $\tilde{I}_a$ leading $\tilde{V}_a$ *or* $\varphi=-90°$, with $\tilde{I}_a$ lagging behind $\tilde{V}_a$.

Fig.3-6 shows the schematic of the dc voltage regulation feedback loop for STATCOM. The voltage controlled oscillator (*VCO*) provides its autonomous frequency

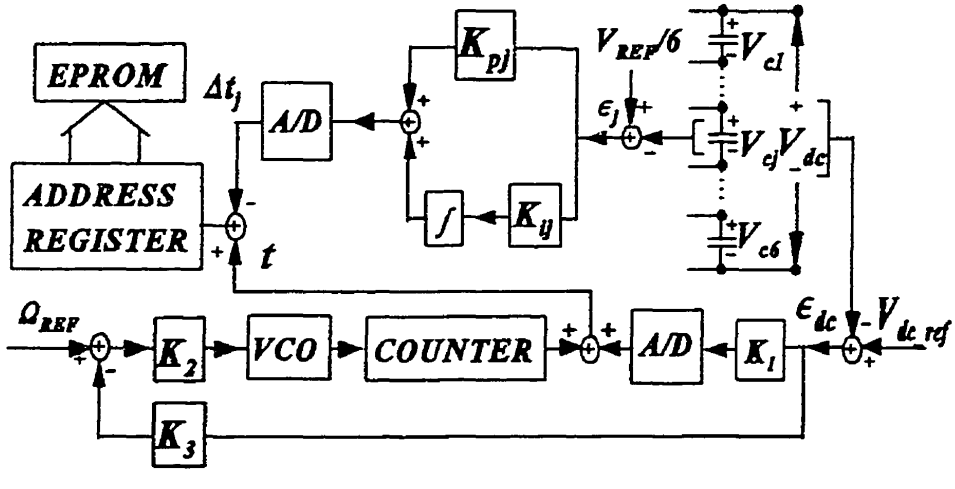

Fig.3-6 Block diagram of regulation and equalization feedback.

ω. The frequency adjustment Ω_{REF} is set at the nominal 60Hz standard, and the STATCOM must be phase-locked to the system frequency to allow for drifts in frequency. The integral and proportional feedback signals are added and stored in the address register which serves as a pointer of discretized time 't'. The 'modulo' implements the cycling periods $2\pi/\omega$.

There are 18 sets of memories (EPROM) which are addressed simultaneously by the address register. Each set contains the switching instructions to the GTOs for each of the 3 phases, in each of the 6 levels. As the *VCO* generates pulses at a rate determined by its input, the counter serves the function of digitizing the progression of time 't'. The switching instructions to the GTOs of a given phase produce a voltage waveform such as v_a in Fig.3-7(a). The error ϵ_{dc} advances or retards the time phase of the waveforms so that through δ in (3-2) the converter rectifies or inverts real power from the ac side to charge or discharge the capacitors C_1, C_2... C_6 until the error is nulled. The nulled error situation corresponds to the converter operation as an inductive or capacitive reactance since the rectified real power is a minuscule amount which replaces the losses in the GTOs and capacitor leakages.

3.3.2 Charging of DC Capacitors

In this research, the equalization of the dc capacitors of the STATCOM will be considered in: (a) the Fundamental Frequency Switching strategy and (b) the Sinusoidal Pulse Width Modulation strategy. As the charging of the dc capacitors have certain

features common to both methods, it is sufficient to examine the capacitor charging currents of the capacitors as shown in Fig.3-7 for the case of Fundamental Frequency Switching strategy. Fig.3-7(a) shows the ac phase current i_a leading the voltage V_a by 90° and Fig3-7(b),(c) and (d) show the portions of i_a which are admitted by the GTOs of the a-phase to form i_{c1}, i_{c2}, and i_{c3} to charge C_1, C_2 and C_3. The charging of C_4, C_5 and C_6 in the negative half cycles of the voltages is not shown. The other two traces of charging currents in the 60Hz cycle come from the phase current i_b and i_c. The contribution of the charging currents from the 3 phases account for the 3*rd* and triplen harmonics. The voltage of the *jth* dc capacitor is:

$$v_{cj}(t) = \frac{1}{C_j}\int_{-\infty}^{t} i_{cj}(\tau)d\tau \tag{3-3}$$

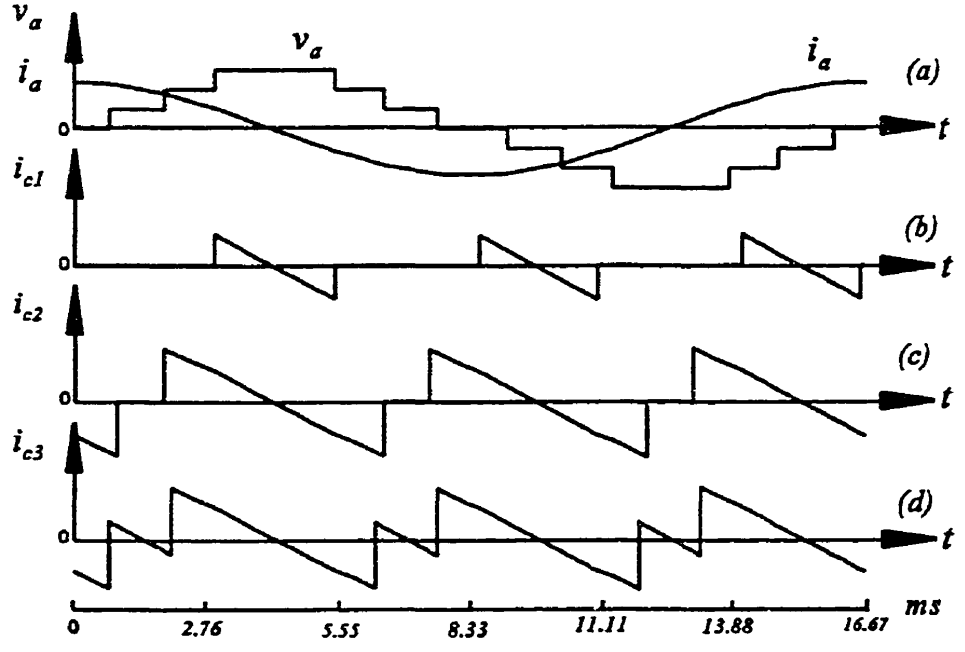

Fig.3-7 Fundamental Frequency Switching strategy: (a) phase current and voltage, (b),(c) and (d) capacitor currents.

Under the ideal odd symmetric condition of the current $i_{cj}(t)$ depicted in Fig.3-7, as much charge flows into the capacitor C_j as leaves it. As the b-phase and the c-phases repeat the capacitor charging and discharging sequence at *T/3* and *2T/3* time delays, there are 3rd and triplen harmonic ripple voltages riding on a constant dc average voltage. The size of the average dc voltage is determined from a previous transient charging period when the steady-state odd symmetric condition was temporarily overridden by the unsymmetric switchings of the GTOs. In the absence of equalization control, the average voltage would remain unchanged at the value determined by the transient charging.

3.3.3 Controlling Average Capacitor Voltages

Equalization presupposes that the average dc voltage is controllable. Choosing a time origin so that $i_a = -I\sin\omega t$ as illustrated in Fig.3-8(a), and triggering the GTOs to admit i_{cj} in the conduction window $[-t_{xj}+\Delta t_j,\ t_{xj}+\Delta t_j]$ as shown in Fig.3-8(b), the voltage of the capacitor C_j, according to (3-3) is

$$\begin{aligned} v_{cj}(t_{xj}+\Delta t_j) - v_{cj}(-t_{xj}+\Delta t_j) &= \frac{1}{C_j}\int_{-t_{xj}+\Delta t_j}^{t_{xj}+\Delta t_j} -I\sin\omega t\ dt \\ &= -\frac{2I}{\omega C_j}\sin\omega t_{xj}\ \sin(\omega t_j) \end{aligned} \tag{3-4}$$

For small Δt_j,

$$v_{cj}(t_{xj}+\Delta t_j) = v_{cj}(-t_{xj}+\Delta t_j) - \frac{2I}{\omega C_j}\sin\omega t_{xj}\ \Delta t_j \tag{3-5}$$

Fig.3-8(c) illustrates the voltages as a consequence of the shifting of the

conduction window for the 3 cases: (i)Δt_j>0-discharging, (ii)Δt_j=0-sustaining, (iii)Δt_j<0-charging. Fig.3-7 and 8 illustrate the case of STATCOM operating as a capacitor. In the inductance mode of operation, when v_a leads i_a, the control method must be reversed, (i) Δt_j>0 -charging, (ii) Δt_j=0 -sustaining, (iii) Δt_j<0-discharging.

3.3.4 Equalization of Average Capacitor Voltage

The time shift Δt_j, to decrease, sustain or increase the capacitor voltage, is added to t, the output of the dc voltage regulation feedback loop as shown in Fig.3-6, so that the address register points to EPROMs of time, $t+\Delta t_j$. The time t of the dc voltage regulation feedback loop is common to all the 6 address registers (j=1,2,...6) and the EPROMs of the

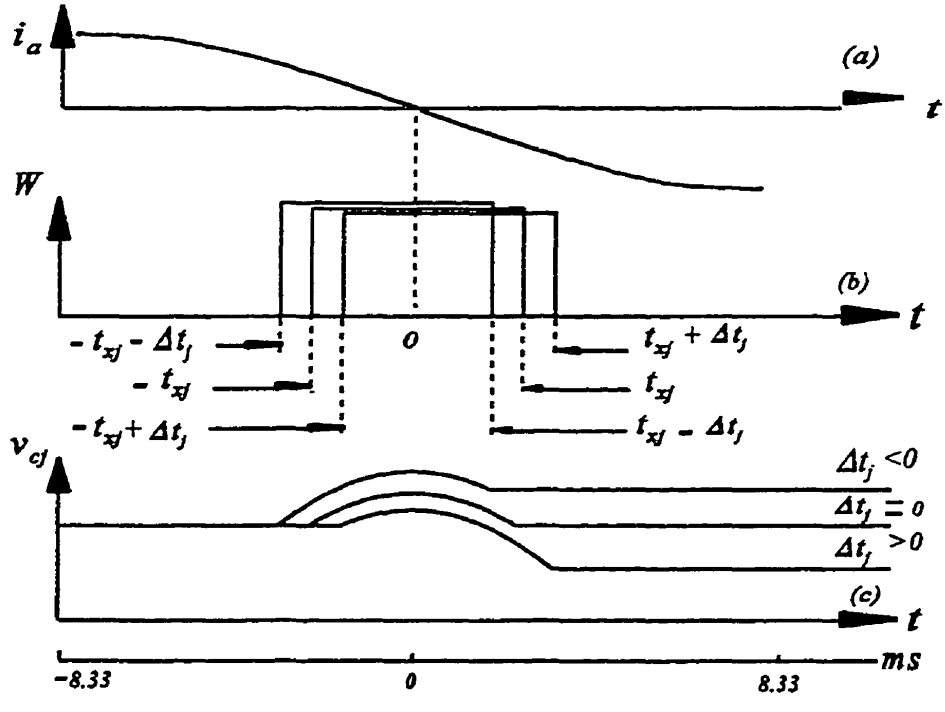

Fig.3-8 Controlling capacitor voltage by shifted conduction window: (a) i_a, (b) window, (c) v_{cj}

jth level contain GTO switching instructions so that the conduction period of i_{cj} spans $[-t_{xj}+\Delta t_j, t_{xj}+\Delta t_j]$. In negative feedback response to the flow of i_{cj}, the error $\epsilon_j=(V_{dc\_ref}/6)-V_{cj}$ is nulled.

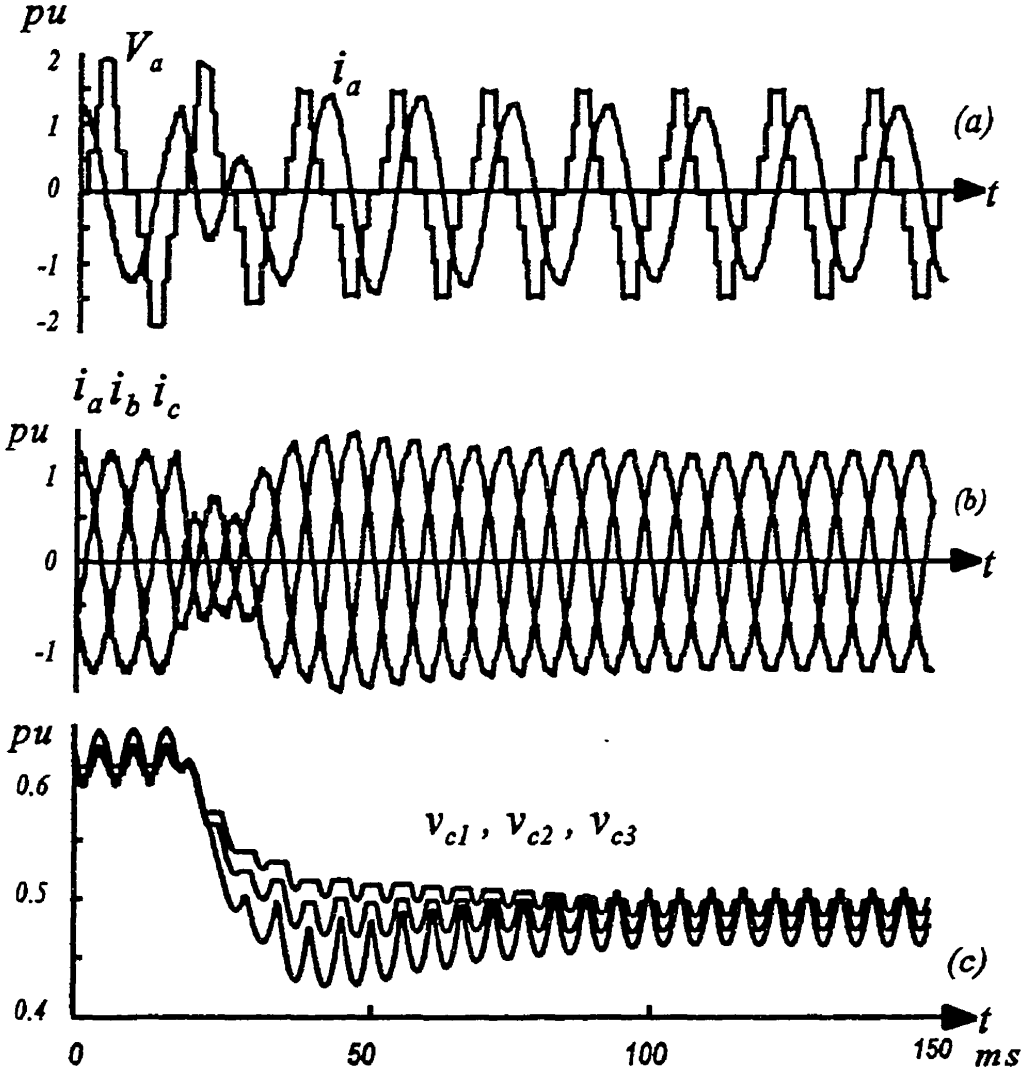

Fig.3-9 Response of regulation feedback under Fundamental Frequency Switching strategy : (a) ac voltage v_a and current i_a, (b) 3 phase current i_a ,i_b, i_c, (c) dc capacitor voltages v_{c1}, v_{c2}, v_{c3}.

3.4 Simulation Test for Single Module-Based STATCOM—Fundamental Frequency Switching Method

3.4.1 Step Response of Regulation and Equalization Feedbacks

Fig.3-9 shows the transient responses as the reference V_{dc_ref} is reduced in a step change so that the STATCOM changes from the capacitive to inductive mode of operation. Fig.3-9(b) and (c) show the 3-phase currents and the capacitor voltages V_{c1}, V_{c2}, V_{c3} during this transient which is completed within 1.5 cycle of the line frequency. This transient response time is a property of the dc voltage regulation loop and the gain constants K_1, K_2K_3 of Fig.3-6. The parameters of the simulations are listed in Appendix C. In Fig.3-9(c), one sees that the equalization feedbacks are at work in ensuring that the capacitor voltages are equalized throughout the step change.

3.4.2 Step Response without Equalization Feedback

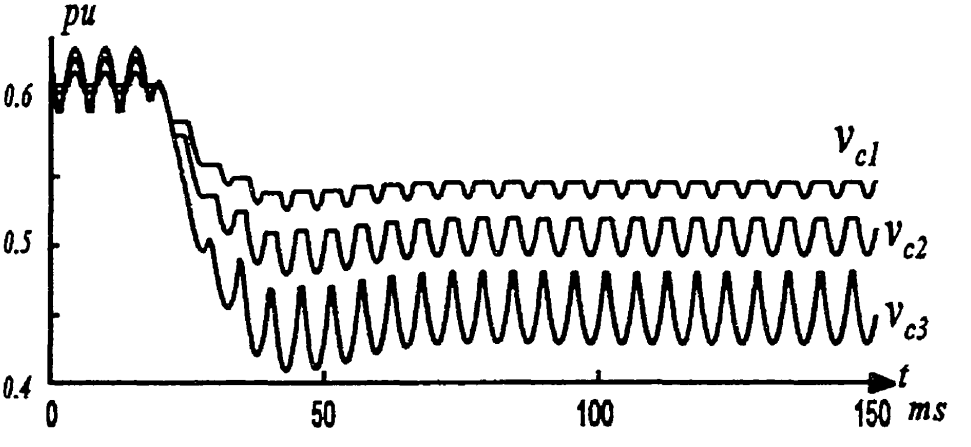

Fig.3-10 Step response without equalization feedback control.

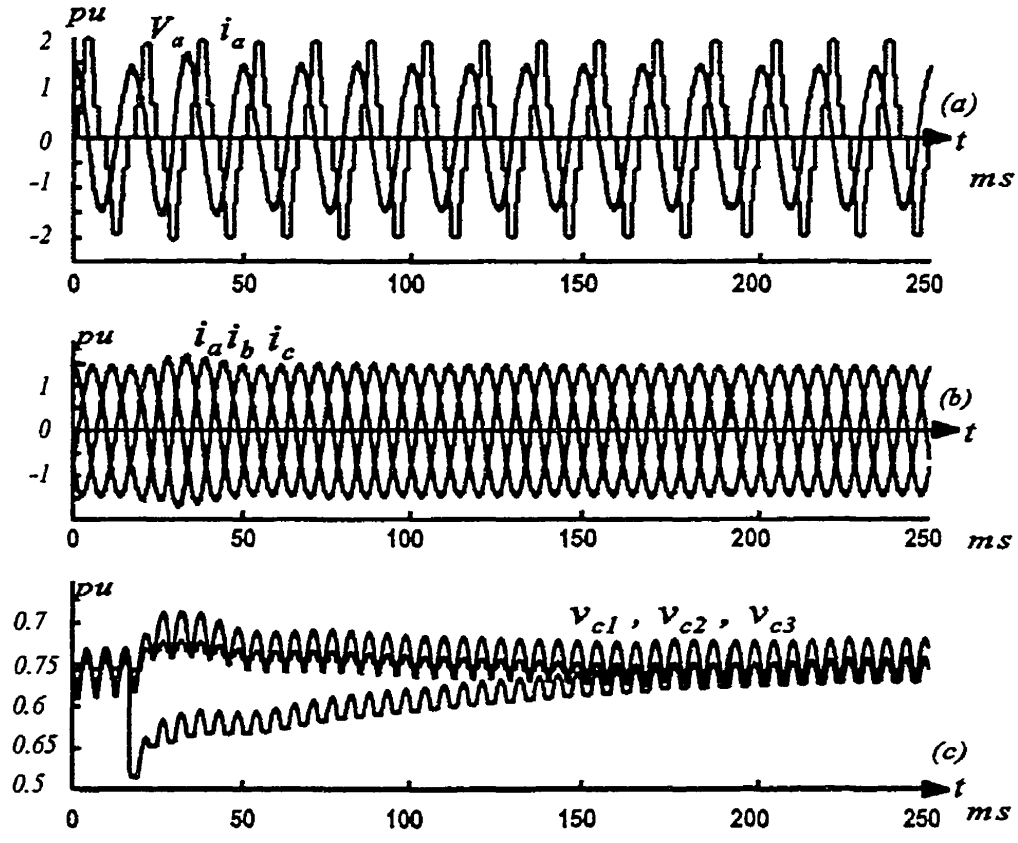

Fig.3-11 Response of equalization feedback under Fundamental Frequency Switching strategy: (a) ac voltage v_a and current i_a, (b) 3 phase current i_a ,i_b, i_c, (c) dc capacitor voltages v_{c1}, v_{c2}, v_{c3}.

When the same step change is repeated without the equalization feedbacks, the capacitor voltages, as shown in Fig.3-10, become unequal.

3.4.3 Response of Equalization Feedback

Fig.3-11 shows, on a different time scale, a transient introduced by a step change in V_{cj}, the voltage in only one capacitor. One sees that the equalizing feedback draws it back to $V_{dc\_ref}/6$ but in a longer time of about 8 cycles. This is because the equalizing feedback constants k_{pj} and k_{ij} are different from those of K_1 and K_2K_3.The feedback

constants have been chosen after extensive trial and error tests.

3.4.4 Comparison of Waveform Harmonics

Table 3-1 compares the harmonics (in % using fundamental waveform as base) of the waveforms of the steady-state ac voltage waveforms (phase-to-neutral of Fig.3-2) after the transient of Fig.3-9(a) and Fig.3-10. The level of dc voltage unbalance in Fig.3-10 is not large, so that the THD in voltage has deteriorated only marginally from 9.70% to 10.15% (The 5% specification [58] is for voltage at the load and not at the STATCOM). In the design using the Fundamental Frequency Switching strategy, the 5th, 7th and 11th harmonics have been chosen to be eliminated.

Table 3-1 Voltage Waveform Harmonics

	Equalization Capacitor Voltage, Fig.3-9(a)	Unequal Capacitor Voltage, Fig.3-10
Harmonic number	%	%
5	0.23	0.42
7	0.16	0.39
11	0.029	0.21
13	3.21	3.21
17	2.36	2.41
19	3.98	4.08
23	0.47	0.22
25	3.81	5.01
...	...	...
THD	9.7	10.15

3.5 Digital Simulation of Multimodular Multilevel Converter Using Multiple Regulation Feedback Control — Fundamental Frequency Switching Method

In chapter 2, the research has described **multiple** modules of the diode-clamped multilevel converter. Up to now, this chapter has focussed on the regulation and equalization of the dc link capacitor voltages for a **single**-module only. Since the multiple modules are connected in parallel to share the same dc link capacitors, it is expected that the regulation and equalization strategies which "work" for the single module should also "work" for multiple modules. Nevertheless, thoroughness requires a statement that digital simulations of the **2-module** example of chapter 2 yield results similar to Fig.3-9 and Fig.3-11, which have been obtained from a single-module. These results are not repeated here. Instead, more interesting results on the ac sides are presented in Fig.3-12. The waveforms show how the 2-module of the diode-clamped multilevel converters operate as a STATCOM while fulfilling the specifications of: (i) direct control of reactive power Q , (ii) low total harmonic distortions in current and voltage waveforms and (iii) equalization of the rms currents. It should be stressed that the dc voltage regulation and equalization feedbacks are essential to the successful operation of the STATCOM.

Fig.3-12 displays the simulation run for a step change in the Q_{ref} from -1.0 pu to +1.0 pu. The simulation of Q in Fig.3-12(a) shows the completion of the reversal from inductive to capacitive reactive power in about 3 cycles of the supply frequency.

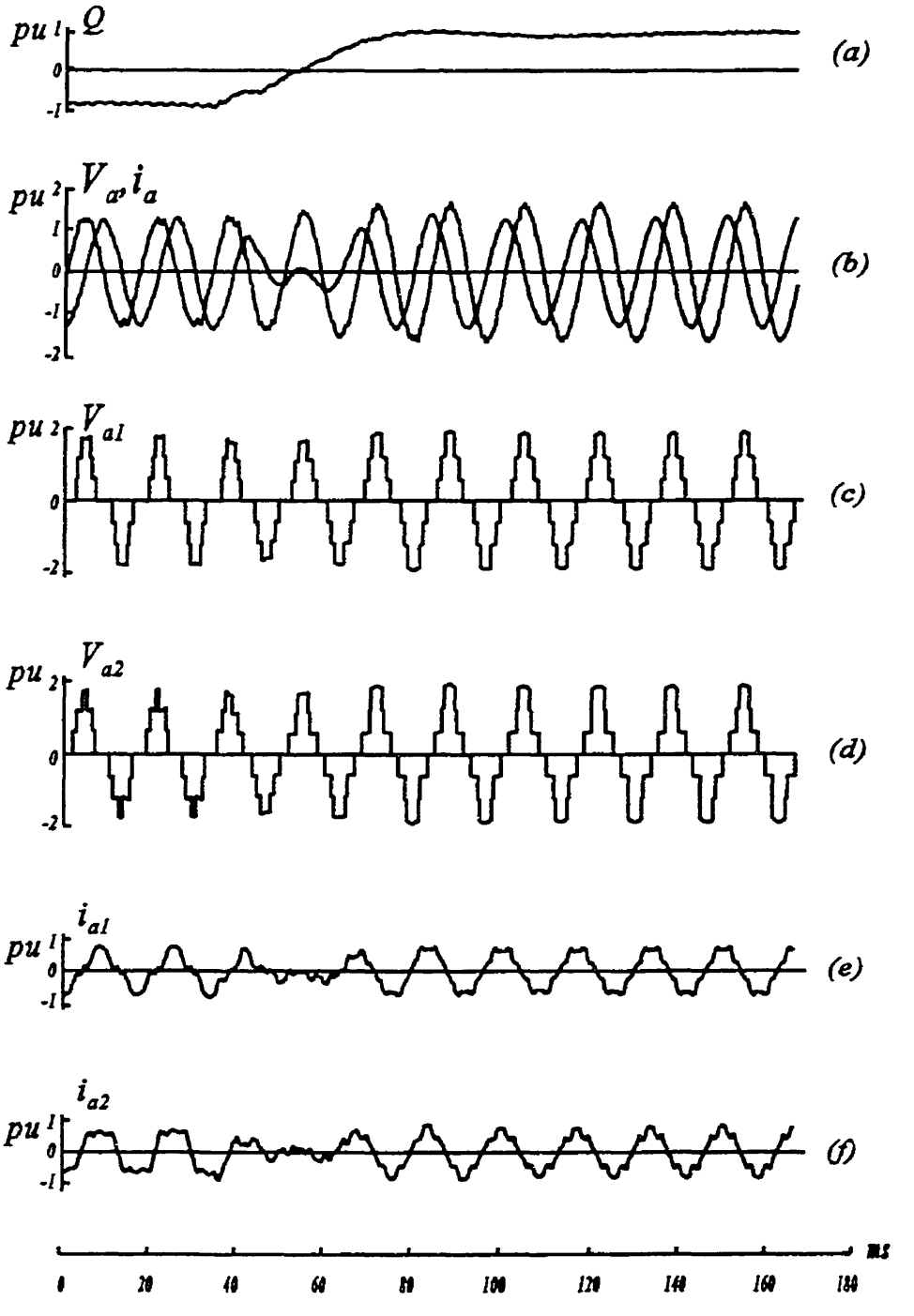

Fig.3-12 Digital simulation of step change in Q_{REF}: (a) reactive power, (b) STATCOM output voltage $v_a(t)$ and current $i_a(t)$, (c) phase-a output voltage of first module, (d) phase-a output voltage of second module, (e) phase-a output current of first module, (f) phase-a output current of second module.

Fig.3-12(b) shows the current initially lagging the voltage by 90° changing to 90° leading. The voltage magnitude changes from the under excitation value to the over excited voltage level. The THD of the voltages is 5.5% and the THD of the current is 3.0%.

Fig.3-12(c) and (d) display the voltage waveforms of Fig.2-1(b) of the 2 modules. Fig.3-12(e) and (f) display the currents of both modules.

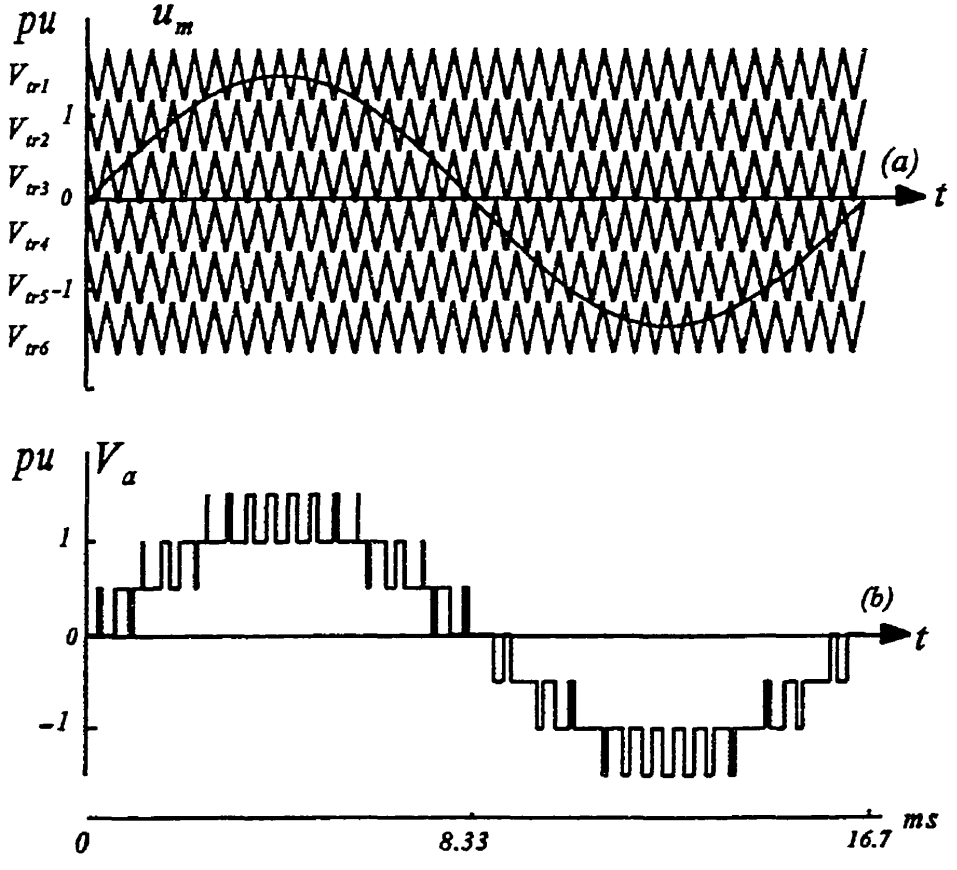

Fig.3-13 (a) Implementation of multilevel sinusoidal pulse width modulation technique f_c/f_m=36, (b) Output voltage waveform using SPWM.

3.6 Sinusoidal Pulse Width Modulation Method

Most research on the diode-clamped multilevel converter are based on the Fundamental Frequency Switching strategy which is suited to GTO technology because the GTOs are required to switch at the lowest rate of 1 pulse per period of the modulation frequency. This chapter extends the research to the Sinusoidal Pulse Width Modulation (SPWM) strategy as Insulated Gate Bipolar Transistors (IGBTs) are now possible competitors of GTOs in high power applications because they are available at 250A, 3KV, switching at 2KHz.

The research of the remaining chapter has been devoted to developing regulation and equalization feedbacks. The conclusion based on digital simulations is that for the low carrier-to-modulation frequency ratio, f_c/f_m=36, the equalization feedback is more difficult to stabilize.

Fig.3-13(a) illustrates the implementation of the sinusoidal pulse width modulation (SPWM) technique as applied to the 7-level converter. The triangle carriers are generated in the 6-levels associated with the capacitors C_j, j=1,2...6. The GTOs admitting the current i_{cj} to control C_j are turned-on and turned-off at the intersection points of the sinusoidal modulating waveform and the triangle waveform of the jth level.

It is found that in order to attain comparable total harmonic distortion (THD) in the current waveforms, which is comparable to the Fundamental Frequency Switching strategy, the carrier frequency to modulating frequency ratio (f_c/f_m) has to as high as 36.

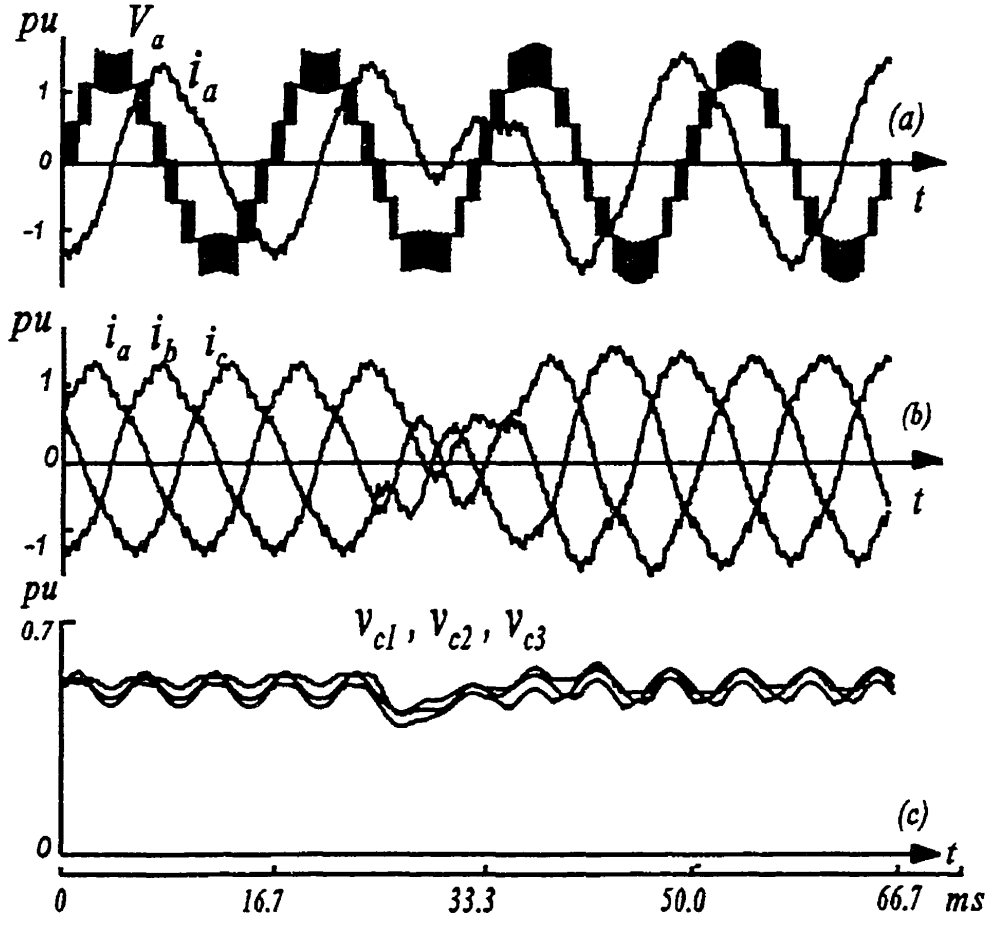

Fig.3-14 Response of regulation feedback under Sinusoidal Pulse Width Modulation strategy with f_c/f_m=36: (a) ac voltage v_a and current i_a, (b) 3 phase current i_a ,i_b, i_c, (c) dc capacitor voltages v_{c1}, v_{c2}, v_{c3}.

The charging and equalization of the capacitor voltages follow the principles and physical insights offered by the Fundamental Frequency Switching strategy, described in Section 3.3. The schematic of the feedback controls is the same as in Fig.3-6. The difference lies in that the modulating signal is programmed into EPROMS. As the EPROMs are addressed at each increment of the COUNTER, the modulating signal is read and compared with the triangle carriers and the intersection points cause the GTOs

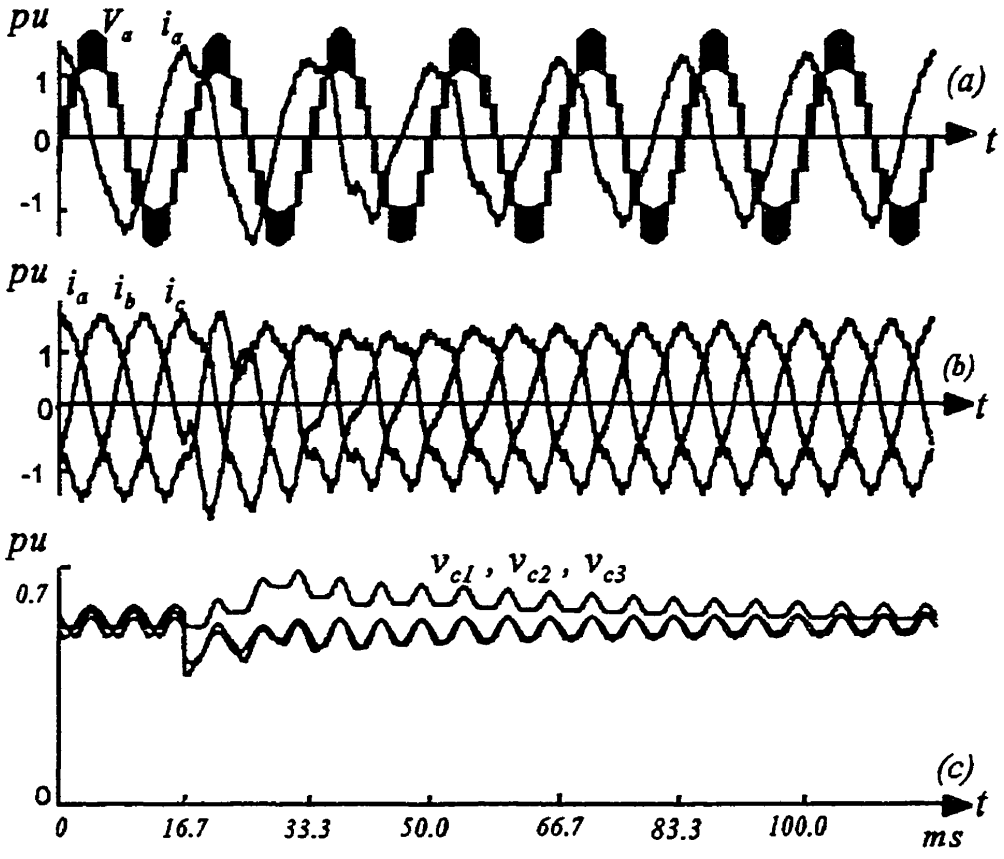

Fig.3-15 Response of equalization feedback under Sinusoidal Pulse Width Modulation strategy with f_c/f_m=36: (a) ac voltage v_a and current i_a, (b) 3 phase current i_a ,i_b, i_c, (c) dc capacitor voltages v_{c1}, v_{c2}, v_{c3}.

of the jth level to be activated. The dc voltage regulation by voltage angle feedback has been described in [53,57] and needs no further-elaboration.

The equalization control follows the principle of the shift of Δt_j as illustrated in Fig.3-8. In the SPWM method, this corresponds to shifting the modulating signal by Δt_j for each of the 6-levels.

Fig.3-14 shows respectively (a) v_a, i_a,(b) the 3-phase currents and (c) the capacitor voltage waveforms following a step-change in the input modulating signals which change

the STATCOM from capacitive to inductive operating mode of operation. The 3rd and triplen harmonic ripples are evident. Fig.3-15 shows again a slower response of the equalization feedback.

3.7 Conclusions

Because of the high MVA ratings, it would be expensive to provide independent, equal, regulated dc voltage sources to power the multilevel converters which are presently proposed for STATCOMs. DC voltage sources can be derived from the dc link capacitors which are charged by the rectified ac power. This chapter has addressed two control issues: (1) regulation of the dc capacitor voltages and (2) their equalization. Equalization is necessary (i) to ensure the even sharing of voltage stresses in the gate-turn-off thyristors (GTOs), and (ii) to prevent the degradation of total harmonic distortion (THD) factors, as all harmonic elimination strategies depend on equal voltages in their assumptions. The strategies considered are: (a) the Fundamental Frequency Switching strategy, (b) the Sinusoidal Pulse Width Modulation strategy. Digital Simulations are used to confirm the feasibility of the control methods in both the cases of single module and multimodule of multilevel converter. The research has shown conclusively that the dc voltage regulation feedback loop alone cannot equalize the dc capacitor voltages at the different levels of the multilevel STATCOM. The equalization feedback loop is necessary for this task. As equalization entails only an additional feedback loop, it is cost effective and no additional loss is incurred.

CHAPTER FOUR

CHOPPER-BASED DC CAPACITOR VOLTAGE EQUALIZATION OF MULTILEVEL RECTIFIER/INVERTER LINK

4.1 Introduction

It has been widely recognized, through digital simulations and reduced scale laboratory experiments, that the diode-clamped multilevel converter of Fig.2-1(a) is suitable for application as a STATCOM [28,30-32,40]. This chapter is a continuation of the research on the "diode-clamped" topology operating under fundamental frequency switching strategy [46]. Having successfully addressed the problem of dc capacitor voltage equalization in the STATCOM in chapter 3, this chapter investigates the feasibility of extending the multilevel concept to other GTO-FACTS controllers. The rectifier/inverter link plays a pivotal role in two FACTS controllers: (1) the Unified Power Flow Controller (UPFC) [17-22], and (2) the back-to-back Asynchronous Link [17,59]. The enquiry of this

chapter is directed again to the problems of equalizing the dc capacitor voltages. The initial disappointing finding is that the feedback method applied successfully in the STATCOM [33,36,46] is effective only when the ac voltage magnitudes of the rectifier and the inverter are equal [35]. The practical implication is that reactive power on both sides cannot be controlled independently and consequently the flexibility of the FACTS controllers is limited.

This chapter shows that the limitation can be surmounted by incorporating dc choppers [39,49] to transfer electric charges from capacitors with excessive voltages to capacitors with deficient voltages. The MVA rating of the chopper is around 0.1pu. The added cost of the chopper must be balanced against the revenues which come from the increased flexibility.

This chapter continues to use the concept of multiple modules of multilevel converters which has been introduced in chapter 2 to increase the MVA rating. As has been shown, multiple modules offer additional switching degrees of freedom in the fundamental frequency switching strategy to eliminate more unwanted harmonics and thus improving waveform quality. In the design example of this chapter, the rectifier and the inverter are each based on 2 modules of diode-clamped 7-level converters because they offer 6 degrees of freedom in design which are sufficient to provide magnitude (VAr) control, ac current equalization in the modules and the suppression of 4 harmonics (5th, 7th, 11th, 13th).

4.2 Rectifier/Inverter Link

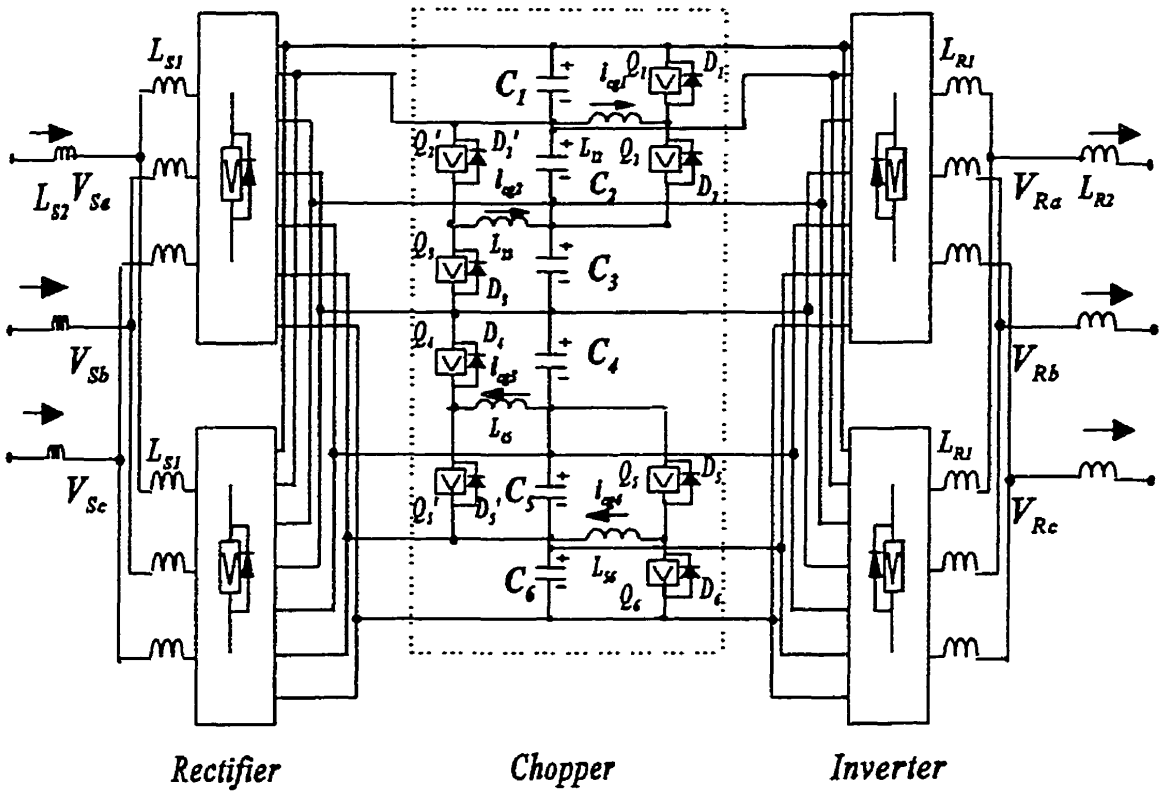

Fig.4-1 Schematic of multimodular multilevel converter with chopper.

Fig.4-1 shows the schematic of the rectifier/inverter link based on the 2 modules of 7-level converter of Fig.2-1(a) on each side of the dc link. The rectifier and the inverter are interconnected through the 7 dc buses and share the 6 dc capacitors. The chopper-based dc voltage equalization system [39,49] is shown in the dc link. A full description of it appears in section 4.3. The application of the rectifier/inverter link will be discussed in chapter 5.

4.3 DC Capacitor Voltage Unbalance

Equalization of the dc capacitor voltages is necessary to ensure that the voltage

stresses across the GTOs are equally shared. As the dc voltage regulator ensures that the total dc link voltage, V_{dc}. is maintained at V_{dc_ref}, undervoltage at one level automatically implies overvoltage at another level which may exceed the voltage rating of the GTOs. Furthermore, the fundamental frequency switching strategy assumes equal dc voltages and any departures imply that the harmonic cancellations will be imperfect.

4.3.1 Equalization of DC Capacitor Voltages in Multilevel STATCOM

In the multilevel STATCOM in chapter 3, it is possible to use a second set of feedback loops which control the switching angle α_{im} (of Fig.2-1(b)) to equalize the dc link voltages at the different levels of the converter [34,36,46]. As has been explained more fully in chapter 3, under steady-state operation, the conduction window of the GTOs at each level (illustrated in Fig.4-2 as $\alpha_i \le \omega t \le \pi - \alpha_i$, i=1, ..., (N-1)/2 for N-level converter) is symmetrically centered with respect to the zero cross-over point of the current . The dc

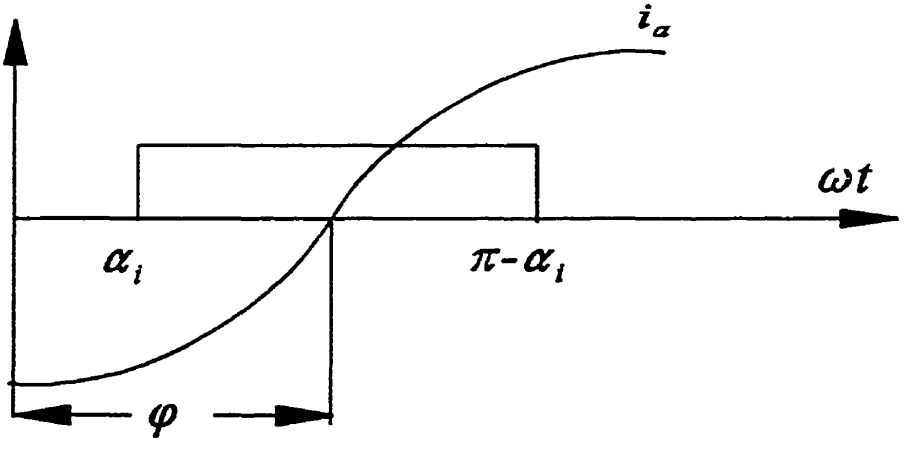

Fig.4-2 Line current and conduction window of jth level.

voltage of the jth level is based on the electric charge Δq deposited on the dc capacitor of that level which is equal to the area under the curve of the current i_a from $\omega t=\alpha_i$ to $\pi-\alpha_i$. In the illustration of Fig.4-2 in which the window is centered, the total area is zero so that the electric charge is not changed and the voltage remains constant. However, when the window is shifted by $\Delta\alpha_i$ so that the window limits are $\alpha_i+\Delta\alpha_i$ and $\pi-\alpha_i+\Delta\alpha_i$, the total area is positive causing the dc voltage to increase when $\Delta\alpha_i$ is positive and vice-versa. The equalization control is based on measuring the dc voltage of each level, comparing it with the reference and using the error in negative feedback to control $\Delta\alpha_i$. The equalization control by feedback in chapter 3 is possible because the conduction window is symmetrically centered in the STATCOM.

4.3.2 Equalization of DC Capacitor Voltages in Rectifier/Inverter Link

In order to reduce the complexity in the analysis of dc voltage unbalance, Fig.4-3 shows the back-to-back rectifier/inverter link using single module of 7-level converter. The conclusion of this simpler model can be extended to FACTS controllers using multimodules of multilevel converters of Fig.4-1. Fig.4-4 illustrates the a-phase currents i_{ha} (h=1 for rectifier and h=2 for inverter) and the conduction windows of a typical level of the rectifier and the inverter. In Fig.4-4, the time origins of the rectifier and the inverter have been chosen to that $i_{1a}=\sqrt{2}I_1\sin\omega_1 t_1$ and $i_{2a}=\sqrt{2}I_2\sin\omega_2 t_2$. It is useful to bear in mind that under steady-state, the centers of the conduction windows of all levels are aligned with the

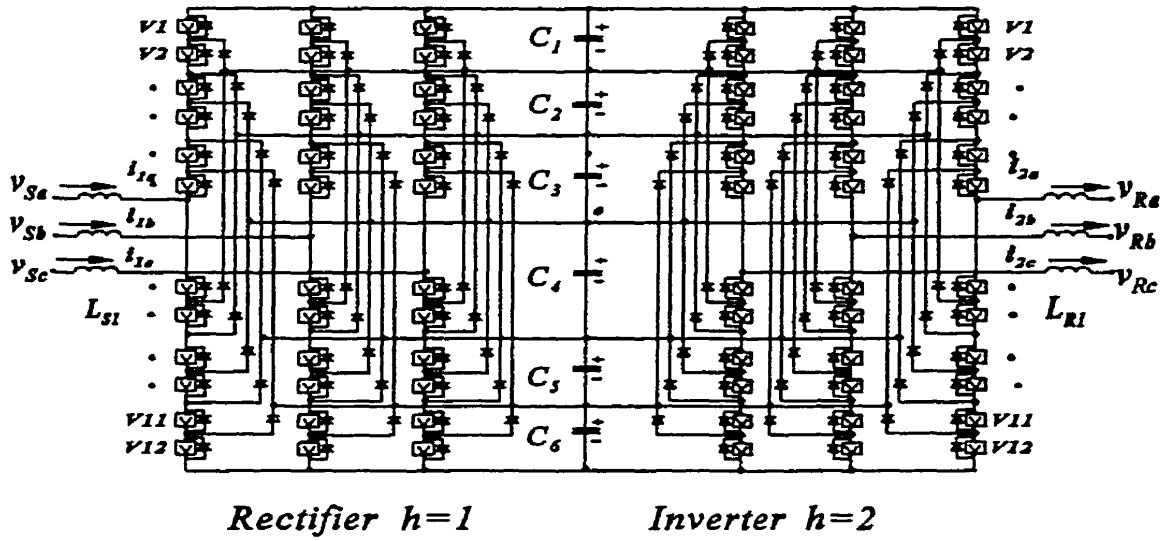

Fig.4-3 Schematic of rectifier/inverter link composed of single module of multilevel converters.

peak of the voltage waveforms. The voltage and current have a phase angle φ_h between them, and this angular constraint is described by $\xi_h=\frac{\pi}{2}-\varphi_h$. The conduction angles, α_{ih} (i=1, ..., *(N-1)/2* for *N*-level converter) which are solved from Fundamental Frequency Switching Strategy described in chapter 2, define the half-window width $\beta_{jh}=\frac{\pi}{2}-\alpha_{ih}$ (i=j, when $j\leq\frac{N-1}{2}$ and i=N-j when $\frac{N-1}{2}<j<N$.) Under steady-state, the electric charge admitted to the jth capacitor in each period is

$$\begin{aligned}\Delta q_j &= \int_{\xi_1-\beta_{j1}}^{\xi_1+\beta_{j1}} i_{1a}\, d(\omega_1 t_1) - \int_{\xi_2-\beta_{j2}}^{\xi_2+\beta_{j2}} i_{2a}\, d(\omega_2 t_2) \\ &= 2\sqrt{2}I_1 \sin\xi_1 \sin\beta_{j1} - 2\sqrt{2}I_2 \sin\xi_2 \sin\beta_{j2}\end{aligned} \tag{4-1}$$

In order to stabilize the capacitor voltage, $\Delta q_j=0$:

$$2\sqrt{2}I_1 \sin\xi_1 \sin\beta_{j1} - 2\sqrt{2}I_2 \sin\xi_2 \sin\beta_{j2} = 0 \tag{4-2}$$

Since $\varphi_h=(\frac{\pi}{2}-\xi_h)$, h=1,2, are the power factor angle of the rectifier and the inverter respectively, the above equation can be rewritten as

$$V_1 I_1 \cos\varphi_1 \sin\beta_{j1} = \frac{V_1}{V_2} V_2 I_2 \cos\varphi_2 \sin\beta_{j2} \tag{4-3}$$

or

$$P_1 \sin\beta_{j1} = \frac{V_1}{V_2} P_2 \sin\beta_{j2} \tag{4-4}$$

where P_1 and P_2 are the active powers, V_1 and V_2 are the rms values of voltages, I_1 and I_2 are the rms ac currents of the rectifier and inverter respectively. Obviously P_1 should be equal to P_2 and therefore we have

$$\frac{V_1}{V_2} = \frac{\sin\beta_{j1}}{\sin\beta_{j2}} \qquad (j=1,2 \ \ldots \ N-1) \tag{4-5}$$

In the 3-level converter, (4-5) is automatically satisfied. For levels higher than 3-level, it is necessary to operate with the same switching patterns at both the rectifier and inverter sides, that is $\beta_{j1}=\beta_{j2}$ and $V_1=V_2$, in order to satisfy (4-5). However, β_{j1}, β_{j2} (j=1,2

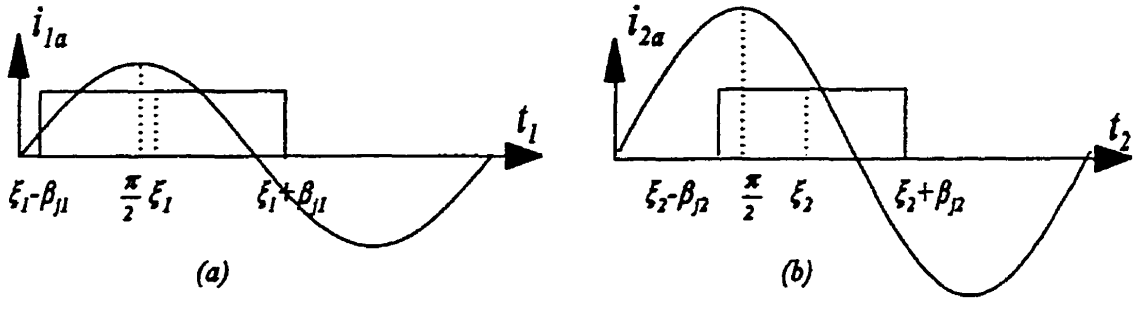

Fig.4-4 Conduction window of the (a) rectifier and (b) inverter.

..., *N-1*) are determined by harmonic elimination and other considerations. In order to achieve the capability of multi-function power flow control, the multilevel Asynchronous Link or the multilevel UPFC depends on changing the switching patterns to obtain the independent control of the ac voltage magnitudes at both the rectifier and inverter sides. Therefore, (4-5) is a serious constraint to the multilevel asynchronous link or the multilevel UPFC.

The analysis shows that for $V_1 \neq V_2$, in order to stabilize and equalize the dc capacitor voltages, the electric charges of capacitor must be transferred from one level to another level.

4.4 Auxiliary Chopper Circuits for Capacitor Voltage Equalization

As it is not possible to use feedback controls to equalize the dc voltages, the auxiliary chopper circuits of Fig.4-1 are incorporated into the design. This design presupposes that the flexibility which comes from the ability to vary the ac voltages independently is worth the additional cost, which is affordable when the ratings of the auxiliary GTOs, diodes and inductors are low.

4.4.1 DC Chopper Circuit

Fig.4-1 contains 4 class B dc chopper circuits. Comparing the GTOs Q_1, ... Q_6 and the antiparallel diodes D_1, ... D_6 of Fig.4-1 with the GTOs of the main converter in Fig.2-1(a), one sees that they must have the same voltage ratings. The chopper circuits are

economically feasible only when their current ratings are small.

To explain its operation by way of an examples, Q_1, D_1, Q_2, D_2 and L_{12} form the elements of one chopper circuit. If the voltage V_{c2} of capacitor C_2 is higher than V_{c1} of capacitor C_1 and it is desired to transfer some of the charge in capacitor C_2 to C_1, Q_2 is turned on briefly. The capacitor C_2 discharges through Q_2 transferring energy to the inductance L_{12}. As the current i_{cg1} increases from zero, the magnetic energy of L_{12} builds up. When Q_2 is turned off, i_{cg1} continues to flow through diode D_1 to charge the capacitor C_1. The opposing voltage V_{c1} causes i_{cg1} to decrease to zero, at which point the stored magnetic energy in L_{12} has been transferred entirely to C_1.

When the charge of C_1 is to be transferred to C_2, it is Q_1 which is turned on momentarily so that i_{cg1} reverses in direction. The capacitive energy of C_1 is converted as magnetic energy in L_{12} as i_{cg1} increases in the negative direction from zero. When Q_2 is turned off, i_{cg1} continues to flow through the diode D_2 to charge the capacitor C_2.

4.4.2 DSP Algorithm for Equalization

Fig.4-5 shows the flow chart of the control algorithm used in equalizing the voltages V_{c1} and V_{c2} across capacitors C_1 and C_2. The total dc voltage V_{dc} is measured and the mean equalized capacitor voltage for the 7-level converter is set at $V_o=V_{dc}/6$, with an upper threshold V_{max} and a lower threshold V_{min} of 1%. The GTOs Q_1 and Q_2 are triggered ON and OFF based on 4 logic decisions in the flow chart.

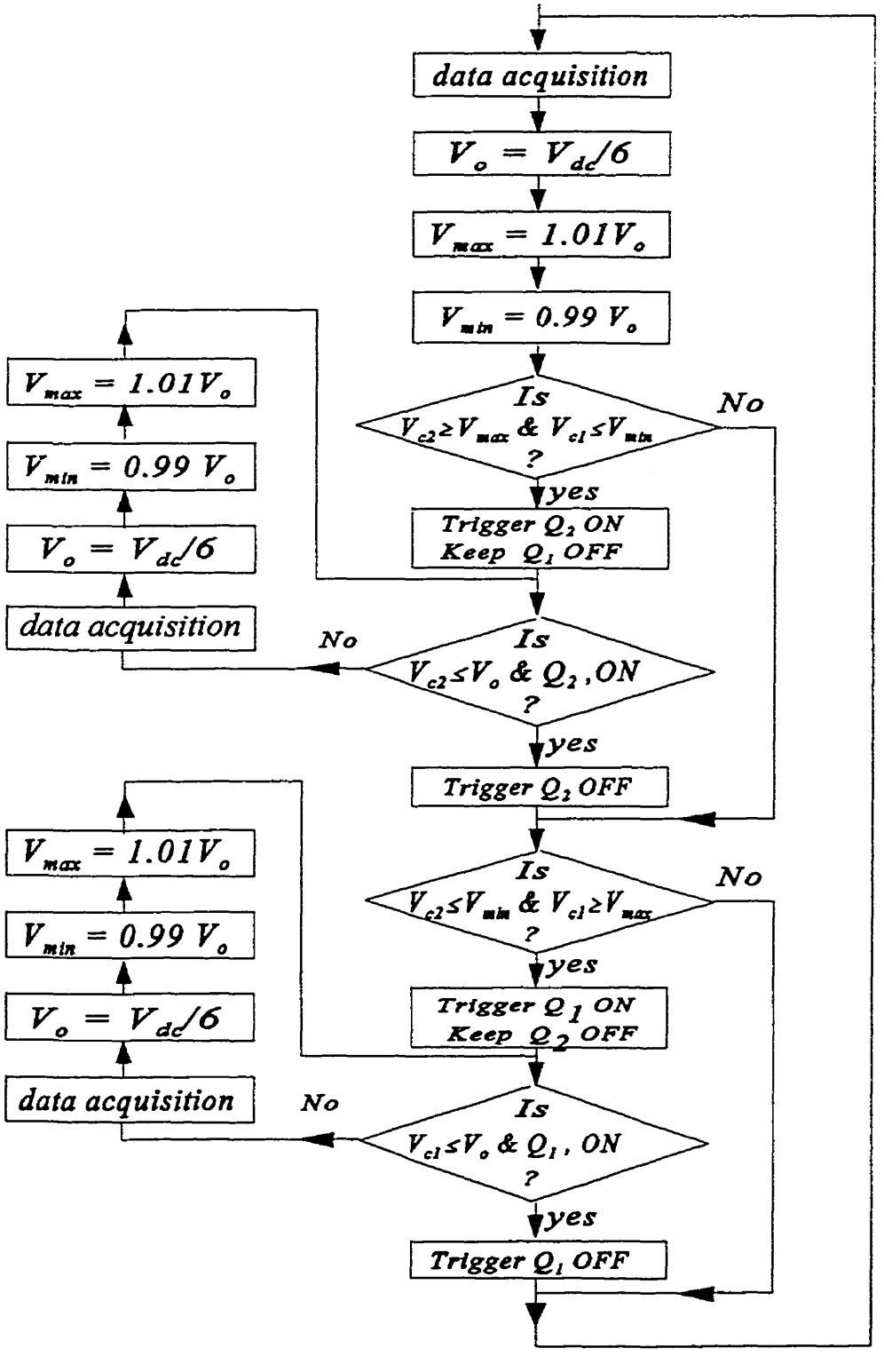

Fig.4-5 DSP control algorithm of the chopper control.

Fig.4-6 shows V_{c1}, V_{c2} and i_{cg1} which illustrate the operation of the control algorithm of Fig.4-5. Because of the unequal rectifier/inverter power transfer, V_{c1} is collapsing while V_{c2} is increasing. At time t_1, $V_{c2}=V_{max}$ and $V_{c1}<V_{min}$, so that Q_2 is turned ON and Q_1 is turned OFF. The flow of the current i_{cg1} drains the charge in C_2 so that V_{c2} drops. The voltage V_{c1} of capacitor C_1 continues to decrease. At time t_2, when $V_{c2}=V_o$, the GTO Q_2 is turned OFF. The magnetic energy stored in the inductance maintains the flow of i_{cg1} which takes a path through the diode D_1 to charge C_1. The voltage V_{c1} increases until t_3 when i_{cg1} drops to zero. Thereafter V_{c2} continues to increase and V_{c1}

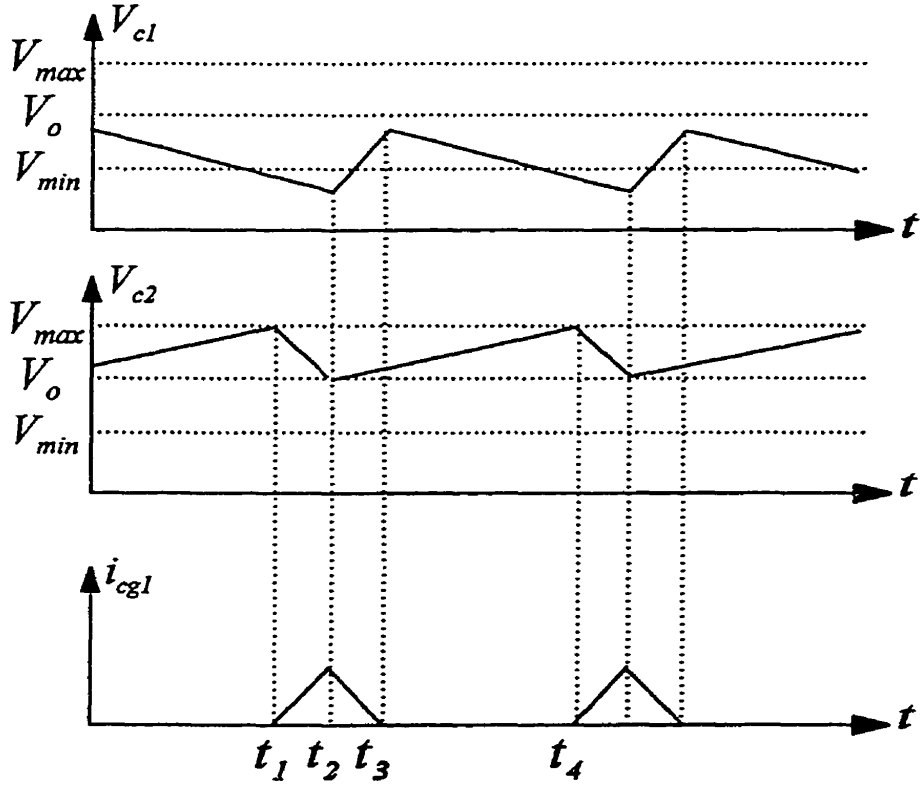

Fig.4-6 Illustration of voltage equalization control algorithm.

continues to decrease because of the inherent unbalance in the rectifier/inverter. The action of the equalization circuit is repeated at time t_4.

Fig.4-1 shows other chopper circuits: Q_2',Q_3 and L_{23} to equalize the voltage of C_2 and C_3, Q_4, Q_5' and L_{45} to equalize the voltage C_4 and C_5,Q_5, Q_6 and L_{56} to equalize the voltages of C_5 and C_6. Each chopper circuit is locally controlled by the algorithm of Fig.4-5.

4.5 Simulation Test of Auxiliary Circuits

Fig.4-7 shows the digital simulation of the unstable dc link capacitor voltages without the chopper circuits when the rectifier and the inverter have different magnitudes of the fundamental ac voltages so that the constraint of (4-5) for balance is not satisfied.

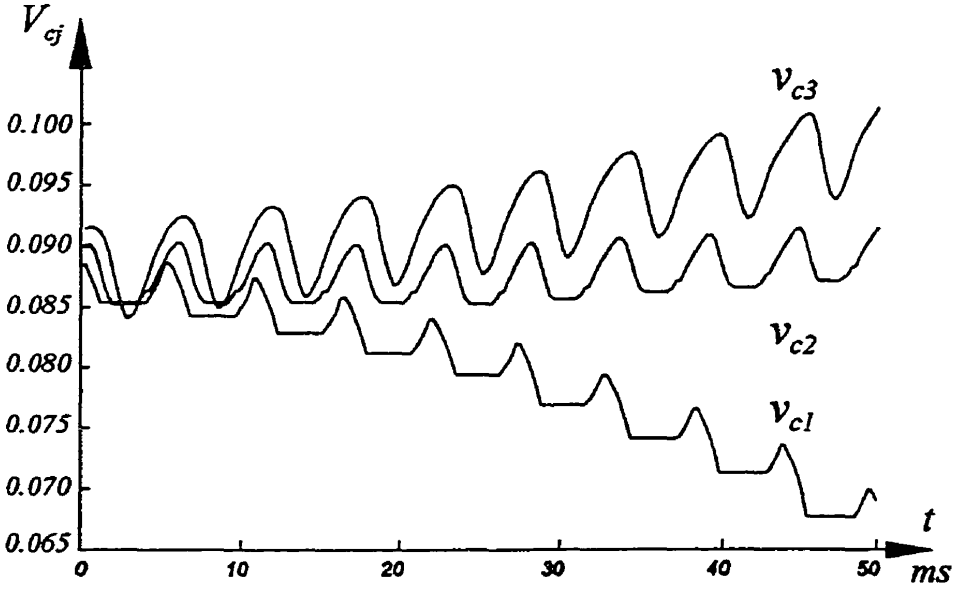

Fig.4-7 DC capacitor voltages without chopper controls.

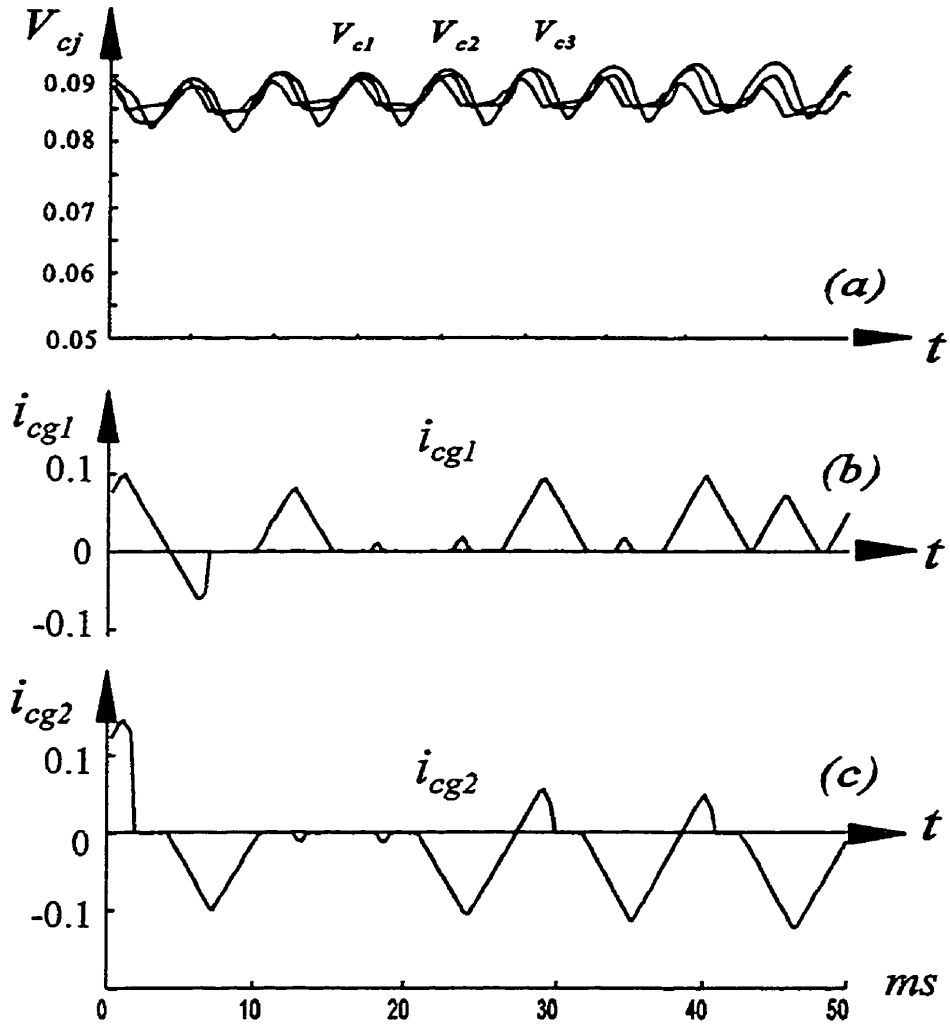

Fig.4-8 Waveforms of: (a)capacitor voltages with chopping circuits, (b) and (c) charging currents of chopping circuits.

Fig.4-8 shows the digital simulation of the stabilization by the chopper circuits so that the upper capacitor voltages v_{c1}, v_{c2} and v_{c3} converge towards a common average dc level. Fig.4-8(b) and (c) show the typical chopper currents, i_{cg1} and i_{cg2}.

In the simulation runs of Fig.4-8(b) and (c), it was found that the currents taken by the chopper do not exceed 10% of the rectifier/inverter. The switching frequency is also of

the order of 1 pulse per 60 Hz period so that switching loss is not prohibitive. Finally, the addition of the chopper has not caused the Total Harmonic Distortion Factor to be increased.

4.6 Experimental Tests

As the problem of using multilevel converters in the rectifier/inverter link is dc voltage instability, the program of experimental tests is focussed on proving that the system

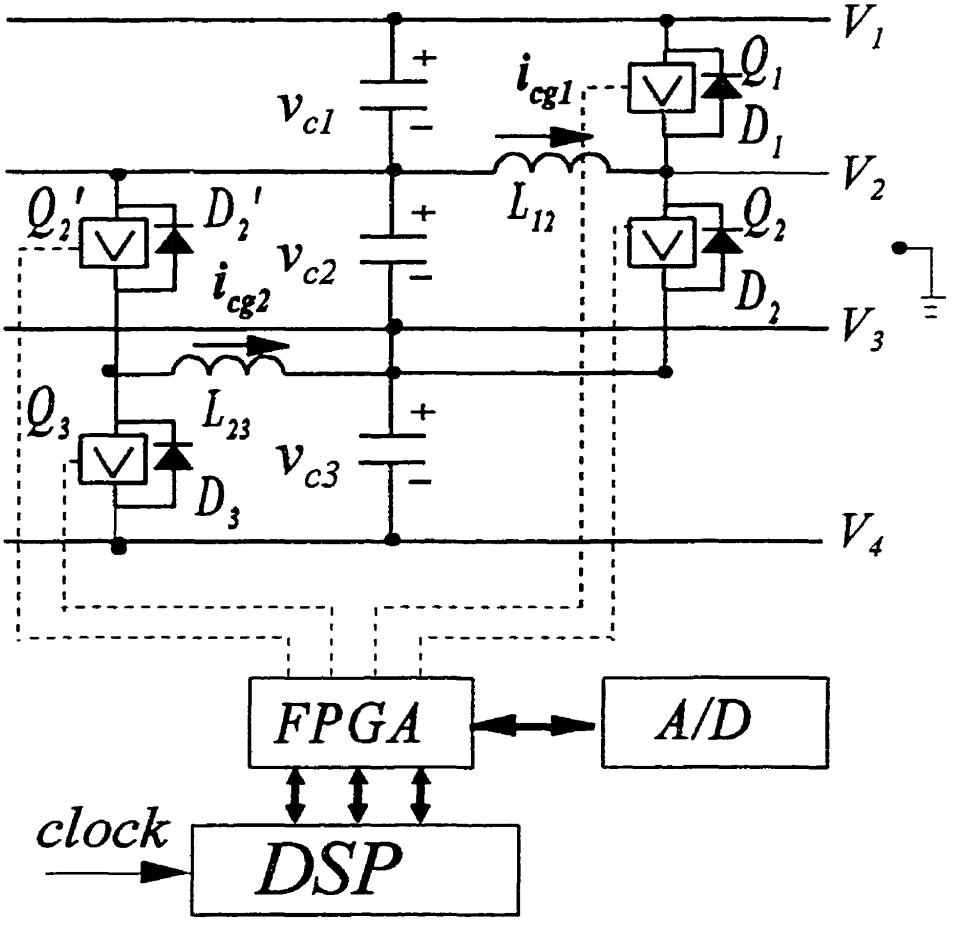

Fig.4-9 Laboratory Chopper System

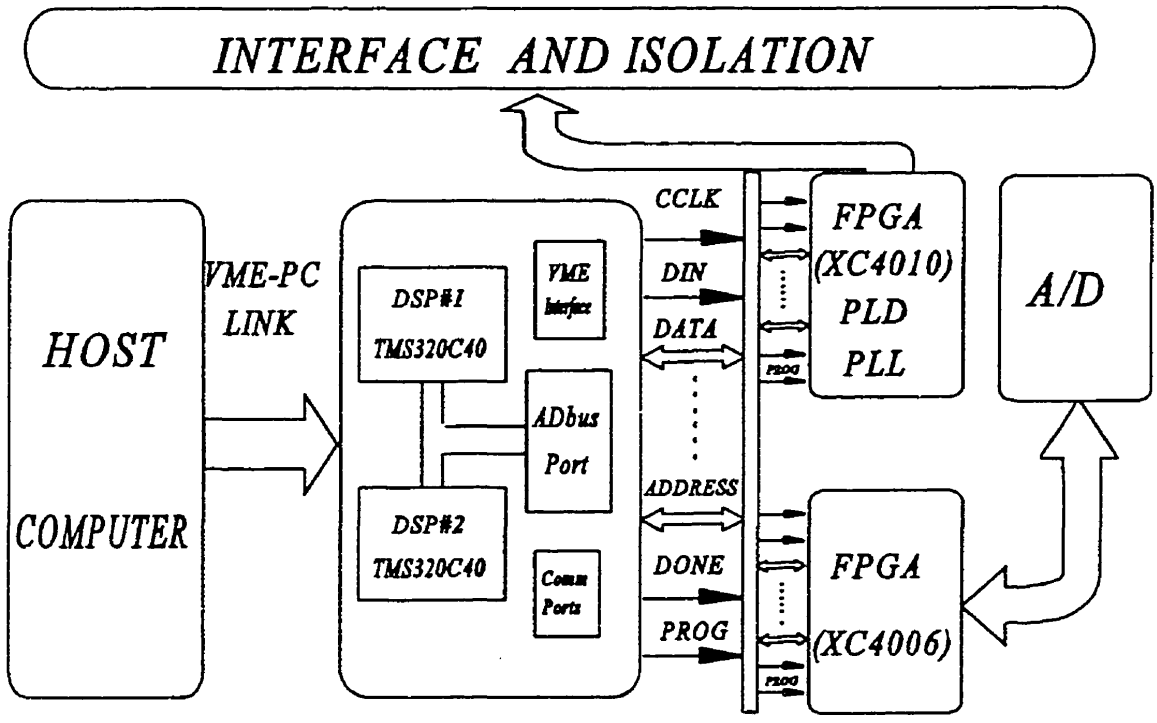

Fig.4-10 Real-time control system for chopper-based voltage equalizing in rectifier/inverter dc link based on 4-level converters.

of class B-choppers can stabilize the dc voltages by equalizing the capacitor voltages in the different levels.

4.6.1 Voltage Equalizing Chopper System

Fig.4-9 shows the Voltage Equalizing Chopper System which has been built in the laboratory for experiments with 4-level converters. The controls are local, that is the chopper of Q_1, Q_2 equalizes V_{c1}, V_{c2} and the chopper of Q_2', Q_3 equalizes V_{c2}, V_{c3}. The control strategies are based on using voltage thresholds of the V_{max} and V_{min} to turn the GTOs on and off as illustrated in Fig.4-6. The electronic implementation makes use of a

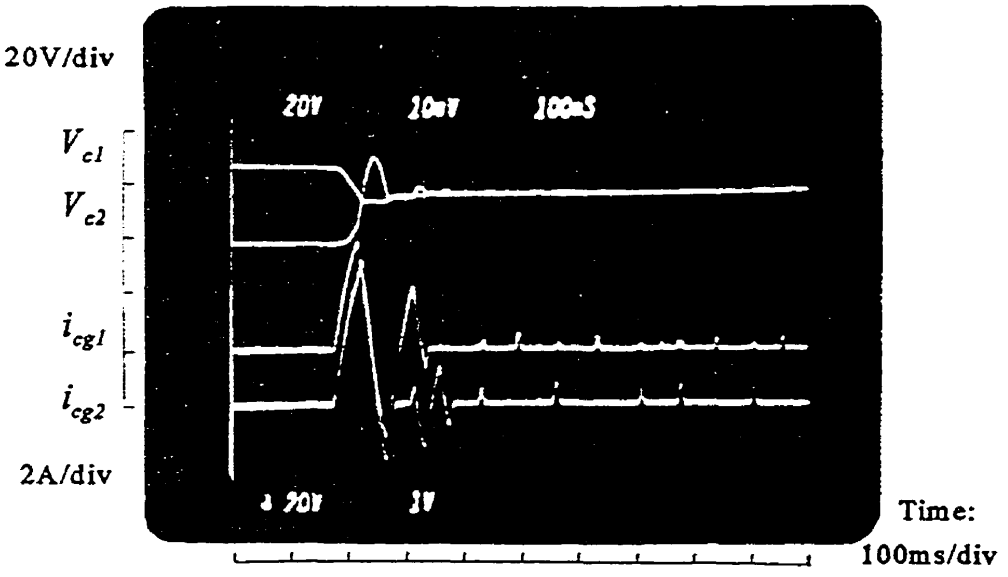

Fig.4-11 Test of capability of choppers to equalize capacitor voltages.

real-time system composed of TMS320C40 DSPs and Xilinx FPGAs as shown in Fig.4-10.

4.6.1.1 Equalization Tests

Fig.4-11 is the oscillogram of a passive test in which initially the capacitor voltages v_{c1} and v_{c2} had been charged unequally. The traces of i_{cg1} and i_{cg2} show that after the initial large charging currents required to equalize the capacitor voltages, small notches keep the voltages equalized in the face of small, unequal current drains in the supply circuit.

4.6.1.2 Suppression of Peak Currents in Chopper Circuits

Since the chopper systems in the simulation tests have been found to switch at a frequency of about once every ac supply cycle and the peak currents are sized at less than 10% of the ac current ratings, they are attractive for FACTS application. However, the test results of Fig.4-11 disclose that under transient conditions, there are large peaks of the charging currents which can exceed the ratings of the GTO devices of the chopper system.

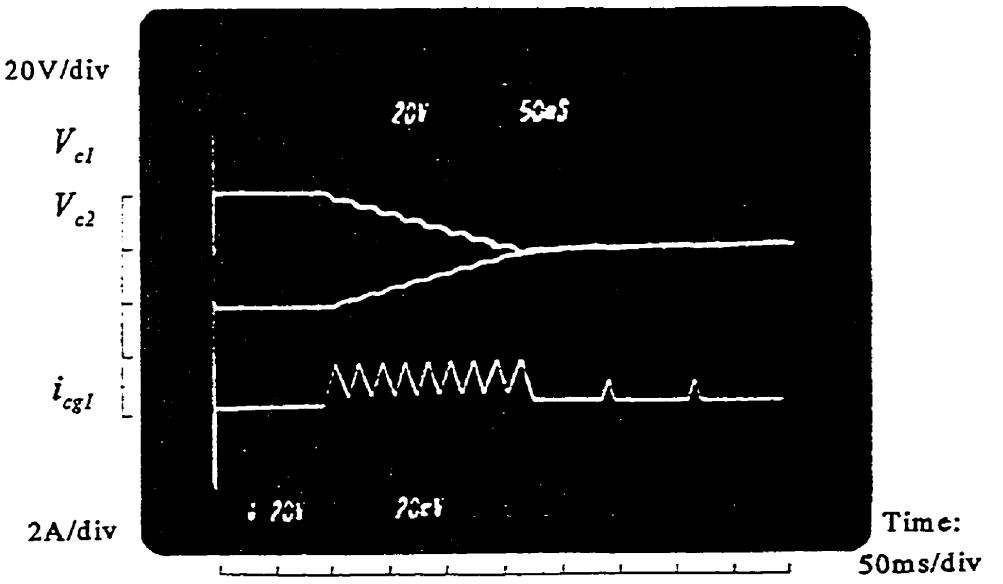

Fig.4-12 Test of overcurrent suppression of the chopper system

In order to suppress the overcurrent, a DSP algorithm for overcurrent suppression is designed and implemented to supplement the algorithm for equalization of Fig.4-5. As shown in the experiment test of Fig.4-12, when the capacitor, C_2 of Fig.4-1, for example, continues to discharge through inductance L_{12} and the charging current i_{cg1} reaches an upper limit, the gating signal for the corresponding GTO of Q_2 is blocked so that the discharging of C_1 is stopped and the charging current i_{c1} begins to decrease and charges C_1 through D_1. The blocking algorithm is deactivated when i_{cg1} has decreased to a safe value and V_{c2} is still 1% higher than V_{c1}.

4.6.2 Rectifier/Inverter DC Link Based on 4-level Converter

The 6 modules of 3-phase IGBT bridge converters available in the laboratory are connected as two 4-level converters in a back-to-back rectifier/inverter link. The 4-level

converter has only one degree of freedom in the design of the switching angle in the fundamental frequency switching strategy. The switching angle of the rectifier is used to eliminate the 5th harmonic, leaving it no magnitude control. However, the phase angle of the waveform is shifted by the error between the dc voltage reference and the measured total dc voltage. Thus this converter rectifies or inverts real ac power to null the error and in the process, tracks the real power of the inverter module. The switching angle of the inverter is used to control the magnitude of the ac voltage in the experiment. In consequence, the inverter currents have poorer ac waveforms than the rectifier.

4.6.3 Steady-State Test

Fig.4-13 shows the line-to-neutral, 4-level voltage waveforms of the rectifier and the inverter. The conduction angles of the switches of the rectifier are not proportional to

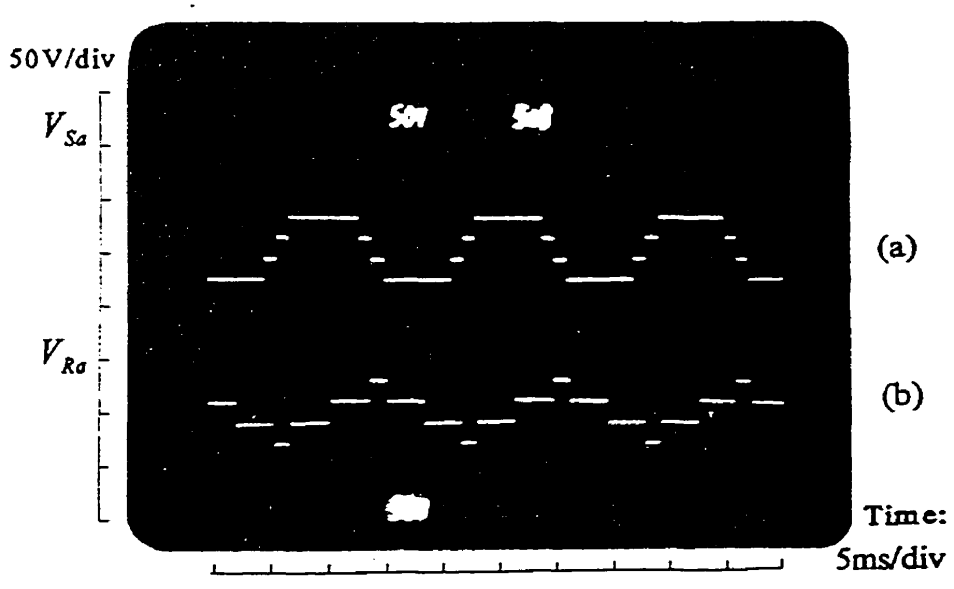

Fig.4-13 Line-to-neutral voltage waveforms: (a) rectifier, (b) inverter.

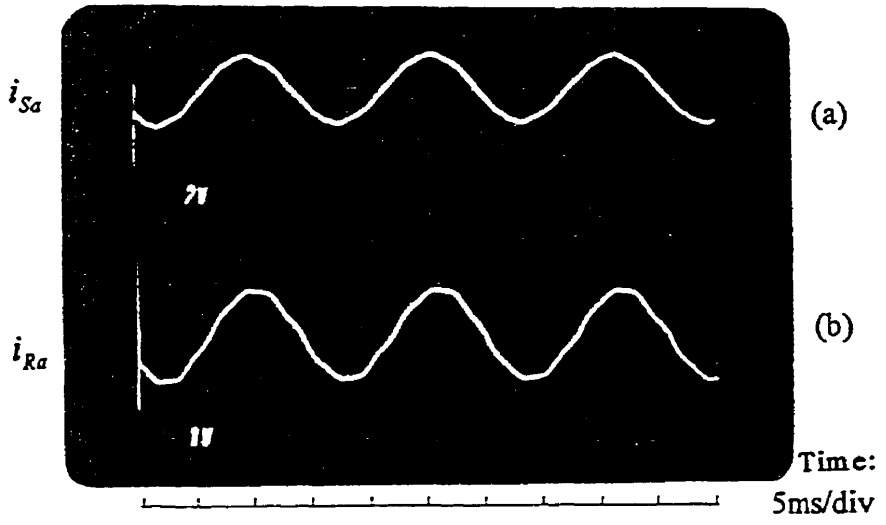

Fig.4-14 Line currents: (a) rectifier, (b) inverter.

those of the inverter, a condition which normally leads to voltage instability. Fig.4-14 shows the quality of their current waveforms in steady-state operation. The control which ensures that the ac power drawn by the rectifier equals that delivered by the inverter is the dc voltage regulating feedback loop of the rectifier. The dc chopper equalize the dc voltages in all the levels.

4.6.4 Transient Test

The transient test consists of introducing a step-change in the magnitude of the inverter ac voltages through the switching angle shown in Fig.4-15. In Fig.4-15, the trace of the inverter ac voltage, V_{Ra}, shows a sudden widening of the conduction angle of the top and bottom segments. The trace of the rectifier ac voltage remains unchanged. The ac voltage and current on the inverter side are captured in the oscillogram of Fig.4-16 (at a

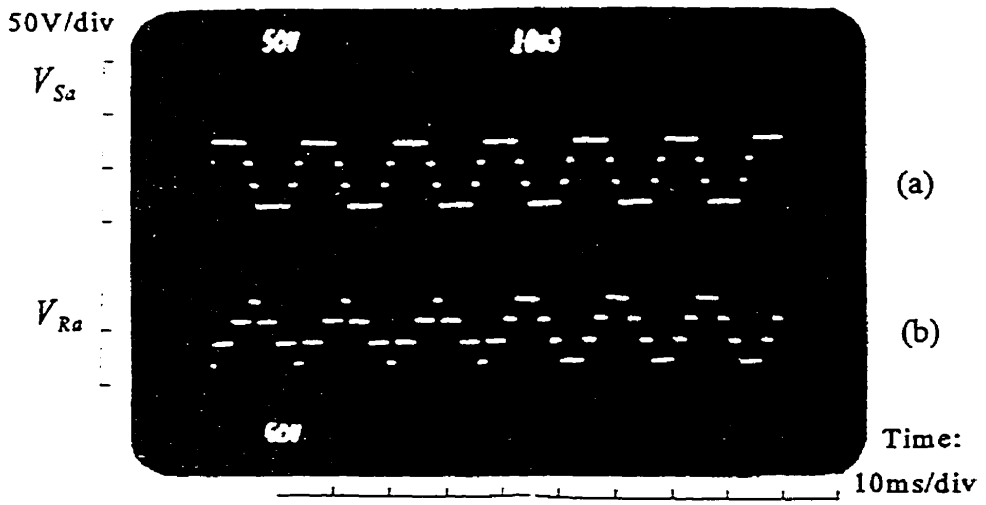

Fig.4-15 Line-to-neutral voltage waveforms showing step change in voltage introduced in inverter (b), while rectifier maintains constant voltage (a).

different time scale).

Fig.4-17 shows the voltages of the dc buses V_1, V_2, V_3 and V_4 with respect to the ground. Measurements show that the capacitor voltages $V_{c1}=V_1-V_2$, $V_{c2}=V_2-V_3$,

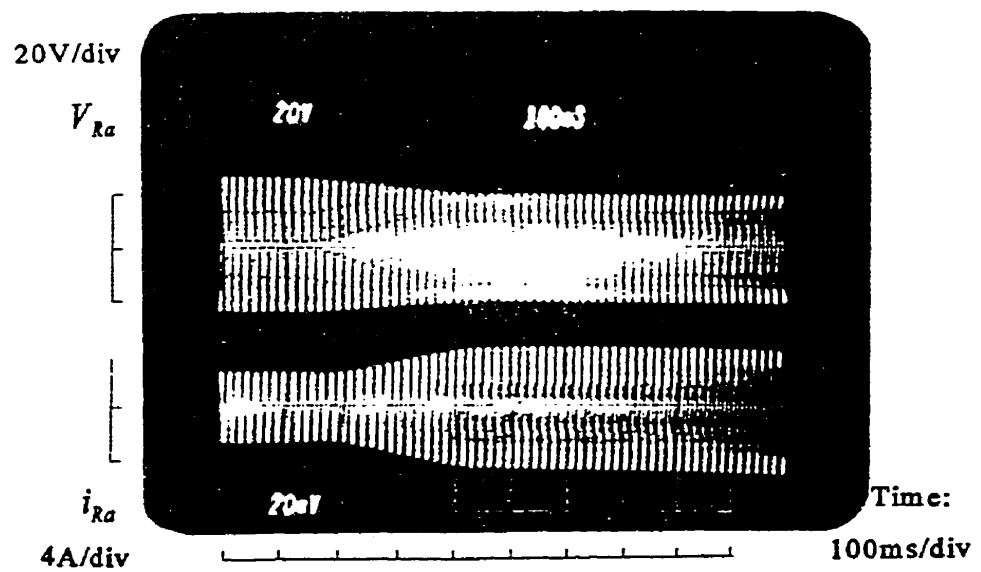

Fig.4-16 Inverter voltage and current in transient test.

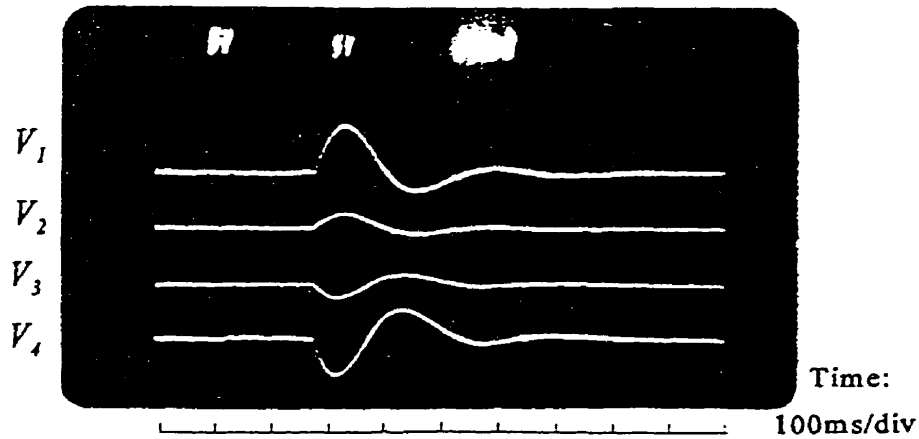

Fig.4-17 DC link voltages in transient test.

$V_{c3}=V_3-V_4$ are almost equal even during the transient, showing the fast action of the dc choppers. The initial increase of $V_{dc}=V_1-V_4$ is due to the fact inverter side has reduced the real power output. As the rectifier is slow in tracking this change, the real power intake causes the capacitor charges and the dc voltages to increase. The adjustment by the phase angle of the rectifier waveform in response to the error in the dc voltage regulator feedback loop causes the intake real power to be lowered as the rectifier power tracks the inverter power. Some hunting has taken place before the new steady-state reaches equilibrium.

4.7. Conclusions

This chapter has shown that by incorporating a dc chopper based dc capacitor voltage equalization system, the multimodular multilevel rectifier/inverter link can operate

with independent ac voltages. Thus independent reactive power control is possible. As the back-to-back Asynchronous Link [17,59] and the UPFC [11-16] depend on the rectifier/inverter link, the research opens up the feasibility of realizing them by multimodular, multilevel converters.

CHAPTER FIVE

BACK-TO-BACK ASYNCHRONOUS DC LINK AND UNIFIED POWER FLOW CONTROLLER BASED ON CHOPPER STABILIZED MULTILEVEL CONVERTER

5.1 Introduction

When the multilevel rectifier/inverter pair, as shown in Fig.5-1, is applied as a back-to-back Asynchronous Link [17,59] of Fig.5-2, or as the shunt and the series converters of the Unified Power Flow Controller (UPFC) [11-16] as shown in Fig.5-3, the dc voltage instability condition has the implication that the magnitudes of the ac voltages of the series and shunt converter must always operate at a fixed ratio determined by the transformer turns ratios chosen. This is a severe constraint and limits its range of operation and flexibility. Therefore, a system of feedback controlled class B-chopper [39,49] has been proposed in chapter 4 to surmount the impasse. As shown in Fig.5-1, each class B-chopper consists, for

example, of an inductor L_{12} and GTO's Q_1, Q_2 and their antiparallel diodes D_1, D_2. The capacitor with the voltage higher than the preset threshold has its excess electric charge transferred to the capacitor with the lower charge. Only local controls are employed. In the 7-level converters of Fig.5-1, there are altogether 4 class B choppers: Q_1, Q_2 to equalize V_{c1}, V_{c2}, Q_2', Q_3 to equalize V_{c2}, V_{c3}, Q_4, Q_5' to equalize V_{c4}, V_{c5} and Q_5, Q_6 to equalize V_{c5}, V_{c6}. The voltage V_{cj} is the voltage across capacitor C_j, j=1,2 ... 6.

The successful equalization of the dc voltages of the back-to-back connected multilevel converters, which has been substantiated by digital simulation and experimental tests in chapter 4, removes the constraint of (4-5) that the voltages of both converters must operate at a fixed ratio. This allows the back-to-back Asynchronous Link and UPFC

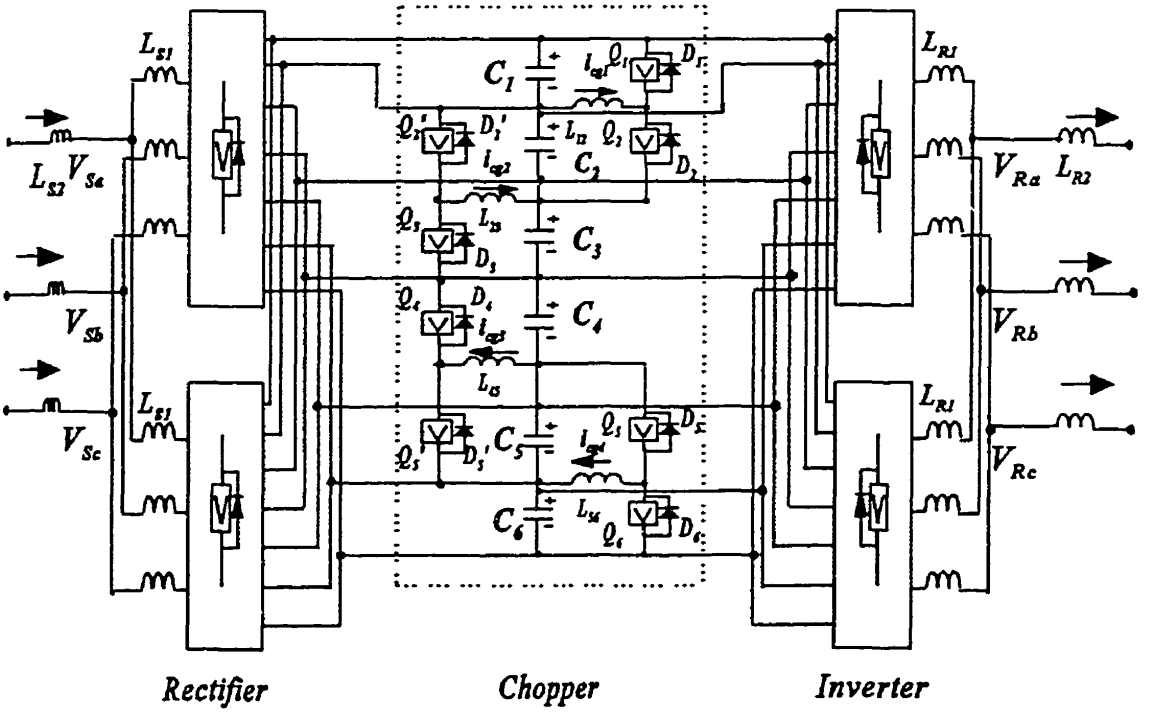

Fig.5-1 Schematic of multimodular multilevel converter with chopper.

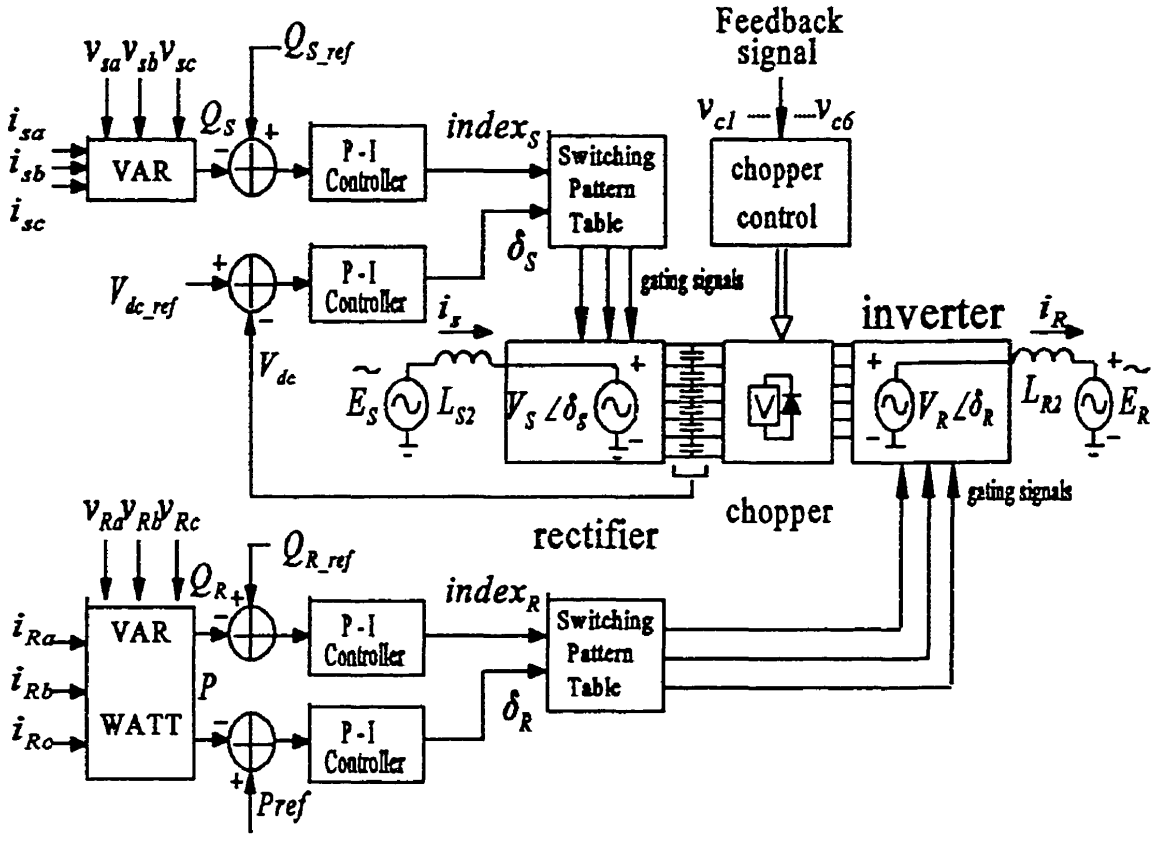

Fig.5-2 Co-ordination of real and reactive power control of the back-to-back asynchronous dc link.

to operate with independent controls over the real power and reactive powers on both sides.

This chapter will study the feasibility of the back-to-back Asynchronous Link and UPFC based on the chopper stabilized multilevel converter. The claims are confirmed by digital simulations.

In the event when the MVA ratings require multiple modules to fulfil the current ratings which cannot be met by a single GTO module, the modules can be connected directly in parallel. It has been shown in chapter 2 that the parallel modules share the load current evenly.

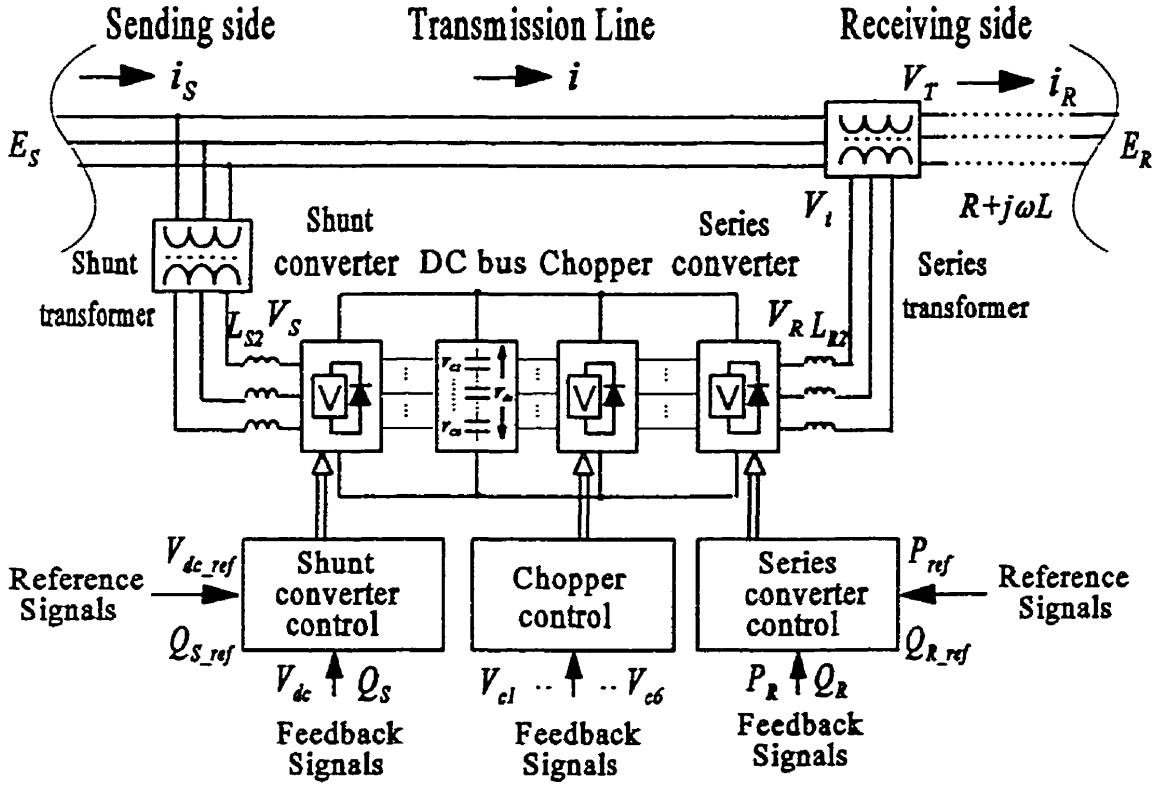

Fig.5-3 Schematic of a transmission line with UPFC in service.

5.2 Back-to-back Asynchronous DC Link with Independent Reactive Power Controls

Fig.5-1 shows the schematic of the rectifier/inverter link based on the 2 modules of 7-level converter of Fig.2-1(a) on each side of the dc link. The rectifier and the inverter interconnect through the 7 dc buses and share the 6 dc capacitors. The chopper-based dc voltage equalization system [39,49] is shown in the dc link. The full description of it has appeared in chapter 4. This section is devoted to the controls of the real and reactive power through the dc link, using the back-to-back Asynchronous Link of Fig.5-2. The conclusion can be extended to UPFC of Fig.5-3.

5.2.1 Co-ordination of Real Power Transfer

In the highly inductive electric power transmission environment, real power transfer is based on control of the voltage angle δ_{ij} in the equation:

$$P=\frac{V_i\ V_j\ \sin\delta_{ij}}{X_{ij}} \tag{5-1}$$

This is done by advancing or retarding δ_{ij}, the angle of the converter voltage waveform V_j of Fig.2-1(b) with respect to the Thevenin voltage V_i and the Thevenin reactance jX_{ij} of the ac system as seen at the ac terminals of the converter. In Fig.5-2, V_i, V_j are E_S, V_S and $\delta_{ij}=\delta_S$ on the rectifier side, and V_i, V_j are E_R, V_R and $\delta_{ij}=\delta_R$ on the inverter side.

The co-ordination of real power transfer through the rectifier/inverter system consists of using δ_{ij} as the control levers to null the errors in two local feedback regulated systems: (1) power dispatcher and (2) dc voltage regulator as shown in Fig.5-2 and described in [59].

5.2.2 Power Dispatcher

The inverter, for example, may be configured as a power dispatcher [59] with the specified power set as its regulator reference. The real power P through the rectifier is measured and compared with the reference P_{ref}. The error is applied in negative feedback through a proportional-integral transfer block to null the error by controlling δ_R of (5-1) on the inverter side.

5.2.3 DC Voltage Regulator

The rectifier needs only to ensure that the total dc link voltage V_{dc} is regulated at its set-point voltage V_{dc_ref}. This is done by using δ_S, the angle control lever of the rectifier to transfer real power so as to null the error between the measured total dc voltage and the reference voltage [59]. To maintain the dc voltage at its reference setting, the rectifier must replenish the dc power taken by the inverter. Thus the real power transfer of the rectifier/inverter pair is co-ordinated.

5.2.4 Independent Reactive Power Control on Either Side

Having committed δ_{ij} in co-ordinated control of the real-power through the rectifier/inverter, the voltage magnitudes of the rectifier and the inverter are available for independent reactive power control. Corresponding to the desired ac voltage magnitude, the switching angles α_{1m}, α_{2m}, α_{3m} (m=1,2) of Fig.2-1(b) are accessed from Switching Pattern Table to control the GTO switchings. As illustrated in Fig.5-2, the reactive power Q_S, Q_R of the rectifier/inverter terminals are measured, compared with the reference settings and their errors point to the indexes of the Switching Pattern Tables.

5.2.5 Digital Simulation Tests of Back-to-back Asynchronous DC Link

Digital simulation programs have been written in C language and the numerical integration is carried out using the Euler method.

Fig.5-4 and Fig.5-5 present the digital simulations of two tests. The design data are

listed in appendix E. In Fig.5-4, the regulated real power is set at P=0.5 pu. On the rectifier-side, Q_S = 0.0pu. On the inverter-side, the initial setting of the reactive power is Q_R=-0.9 pu. A step-change is introduced to reverse the inverter-side reactive power to Q_R = +0.9pu.

Fig.5-4(a) and (b) show that P and Q_S maintain their regulated values and Fig.5-4(c) shows the changeover of the inverter reactive power from Q_R = -0.9 to +0.9pu. Fig.5-4(f) is total inverter line current and (d) (e) are the currents from its two multilevel converter modules.

The chopper currents i_{cg1} and i_{cg2} are shown in Fig.5-4(g) and (h). Typical dc capacitor voltages V_{c1}, V_{c2} and V_{c3} are shown in Fig.5-4(i).

In the test of Fig.5-5, the reactive power settings of the both converter stations are maintained constant. A step-reversal in the real power transfer is introduced, that is the regulated power setting of P = +0.85pu is changed to P = -0.85pu. Fig.5-5(a) to (i) show the same quantities as in Fig.5-4.

The significant findings of the tests relate to sizing of the auxiliary chopper voltage equalization circuits. From the waveforms of i_{cg1} and i_{cg2} in (g) (h), one estimates that their ratings do not exceed 10% of the main converter ratings.

The tests show that the rms currents in (d) and (e) and the capacitor voltages in (i) are held equal during steady-state and transients.

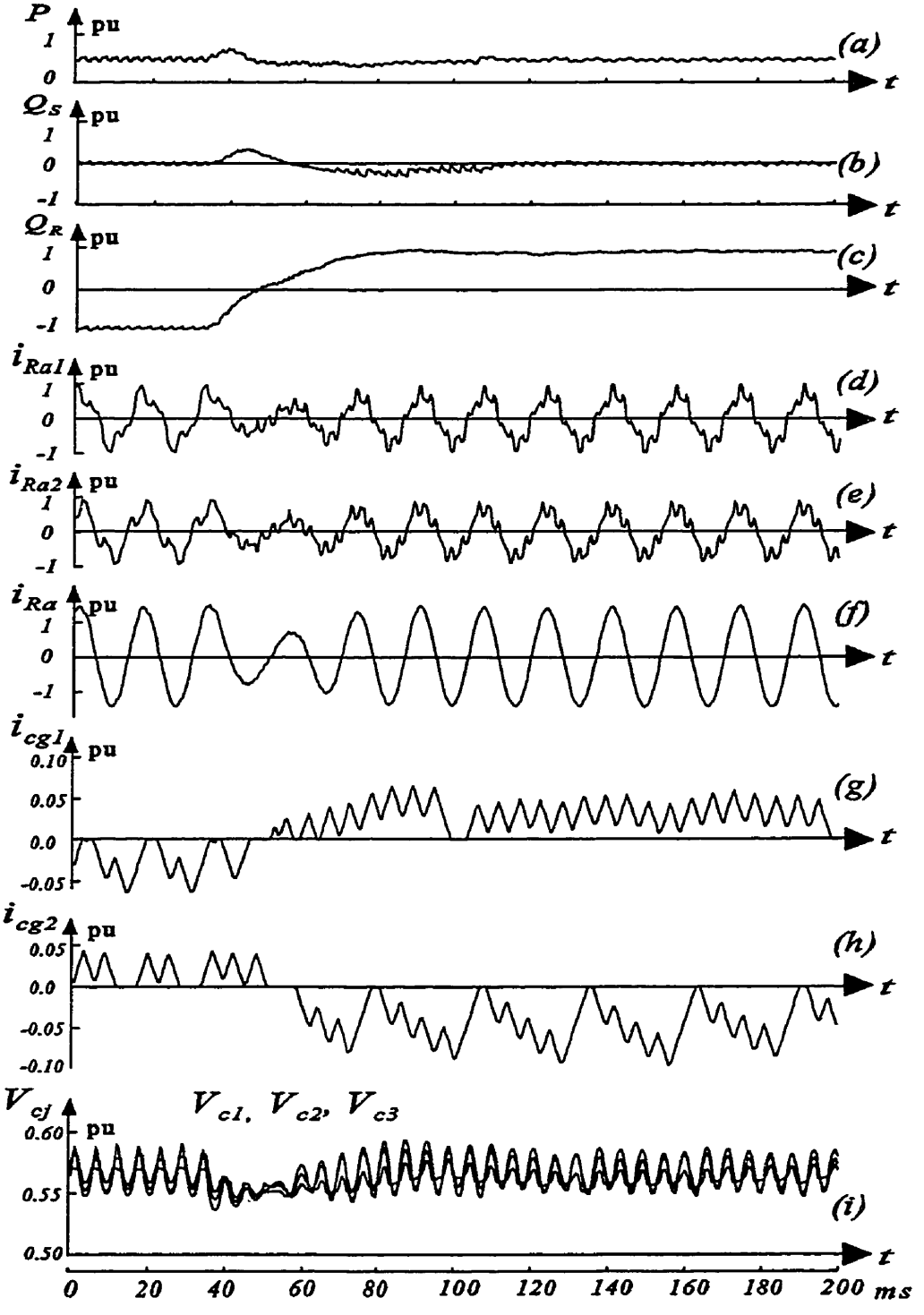

Fig.5-4 Digital Simulation of back-to-back asynchronous dc link: reversal of inverter reactive power.

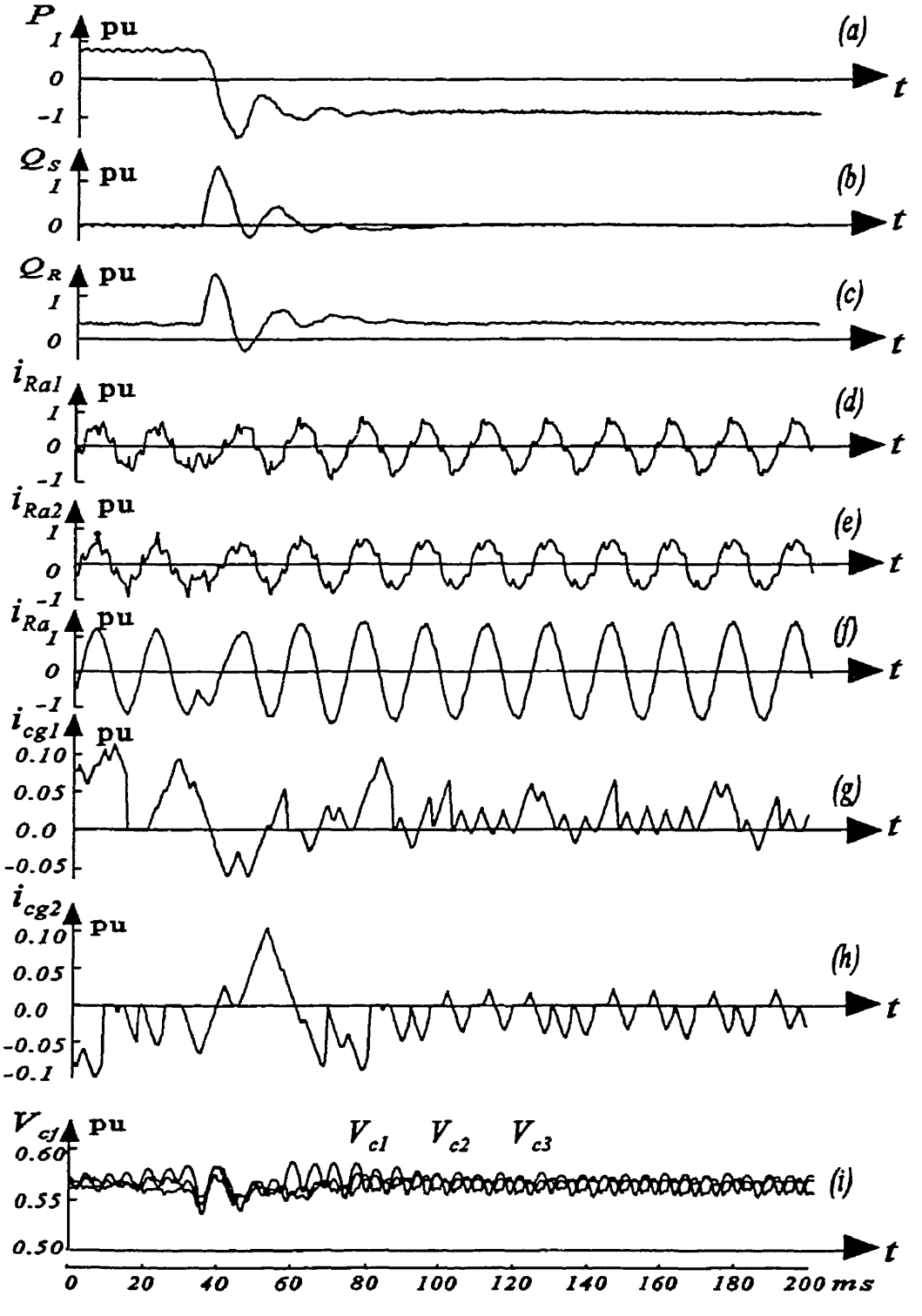

Fig.5-5 Digital simulation of back-to-back asynchronous dc link: real power reversal.

5.3 Unified Power Flow Controller Based on Chopper Stabilied Multilevel Converter

5.3.1 Rectifier/Inverter Link for UPFC

Fig.5-3 shows schematic of the proposed UPFC based on the chopper stabilized multilevel converters. The UPFC is situated at the sending-end of the transmission line which is represented by impedence $R+j\omega L$. The converter on the left side of the UPFC is connected in parallel with the source side of the transmission line. Its ac voltage phase angle and magnitude are independently regulated to control the real power transfer to or from the UPFC and the reactive power generated or absorbed by the converter. The converter on the right side of the UPFC is connected in series with the transmission line with its voltage phase angle and magnitude being applied to control the voltage phase angle and magnitude of V_T, and as a result, the amount of the real power and reactive power transmitted to the receiving end.

The voltage instability of the dc busses, resulting from the independent control of the ac voltage magnitudes using switching pattern control of both converters, are overcome by the class B dc choppers described in chapter 4.

5.3.2 Digital Simulation Tests of UPFC

Fig.5-6 shows the transient response when the voltage angle δ between the

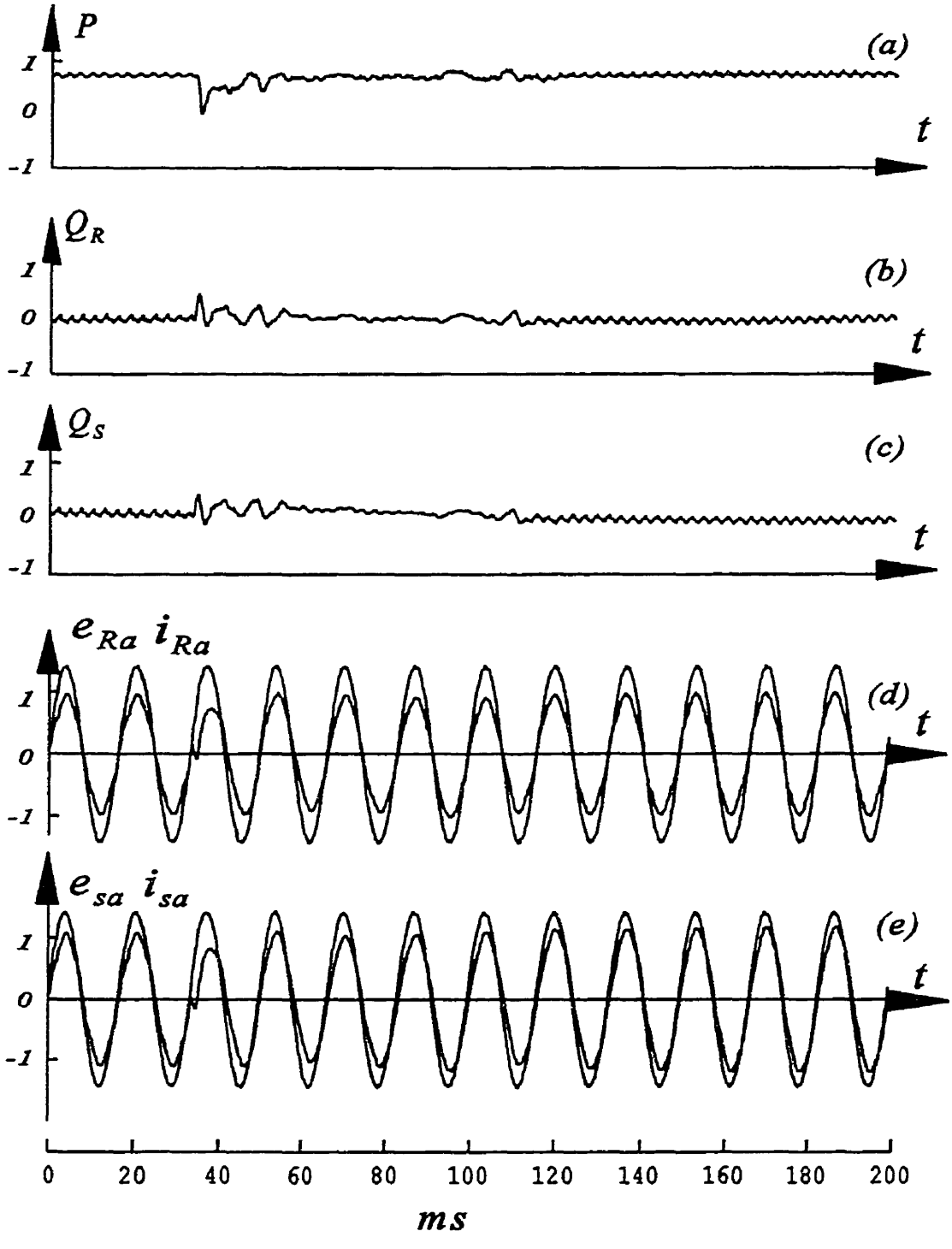

Fig.5-6 Transient response when voltage e_R is phase shifted.Waveform of: (a) P, (b) Q_R, (c) Q_S, (d) and (e) voltage and current at both sides.

sending-end voltage e_S and the receiving-end voltage e_R has a step increase by a small amount $\Delta\delta$. Fig.5-6(a)(b) and (c) show the real power P and the reactive powers Q_R and Q_S as measured on the transmission line. Fig.5-6(d) and (e) show the voltages and currents e_R, i_R and e_S, i_S. The feedback strategies have been designed to regulate the P, Q_s and Q_R and the results show that the transients are damped out within 5 cycles.

Fig.5-7 shows the same step increase in the voltage angle $\Delta\delta$ for the case when the UPFC is not present. One sees that P, Q_S and Q_R settle to new equilibrium values. In comparing Fig.5-6 and 5-7, one concludes that UPFC has acted as a phase-shifter to compensate for the voltage angle change $\Delta\delta$ introduced as a step in the digital simulation

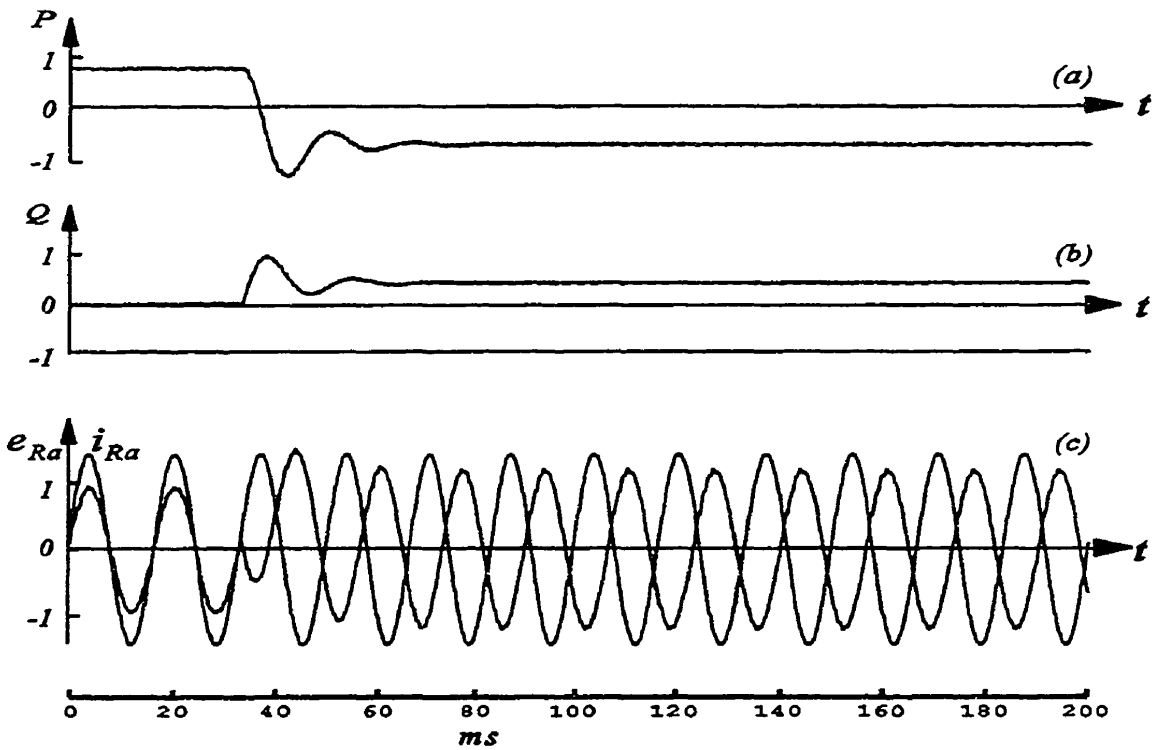

Fig.5-7 Transient response when E_R is Phase shifted and no UPFC is in service.

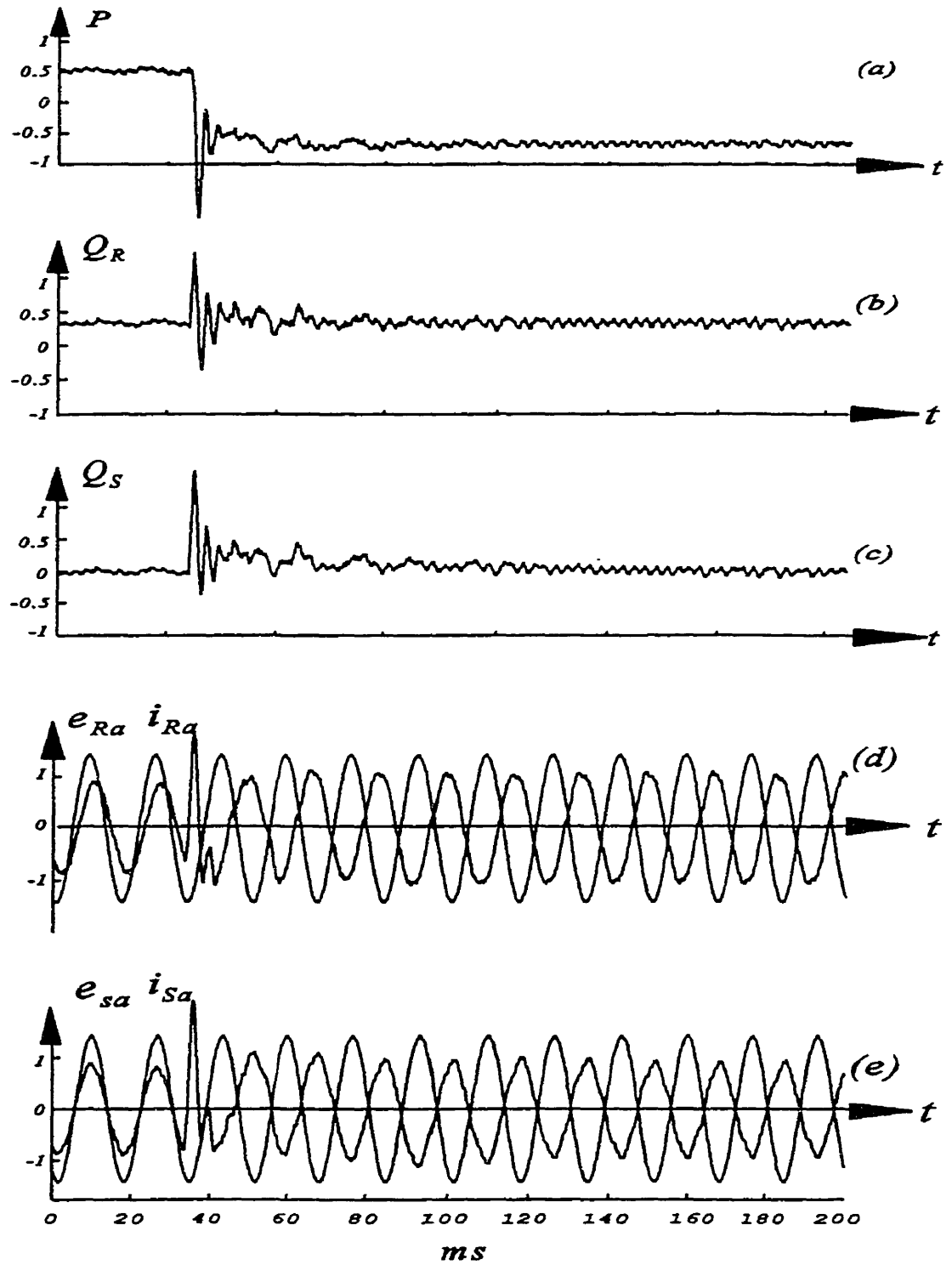

Fig.5-8 The transient response when the UPFC is used to control the real power reversal.

experiment.

In Fig.5-8, the sending-end and the receiving-end voltage magnitudes have initially been set at constant values. The experiment consists of making a step-change in the reference setting of the real power P_{ref} from a positive value to a negative value without changing the reactive power references Q_{R_ref} and Q_{S_ref}. In Fig.5-8(a), (b) and (c), one sees that unity power factors is kept in the sending-end side while constant positive reactive power is kept at the receiving-end side. Fig.8(d) and (e), one sees the 180° phase reversals of the current as a consequence of the power reversal.

The simulations of the multilevel converter based UPFC would not have been possible without the class B chopper systems to stabilize and equalize the dc link voltages thus allowing the magnitudes of the ac voltages of the series and shunt converter to vary Q_S and Q_R independently, so that the UPFC operates more effectively. The simulations have shown that a multilevel UPFC is feasible.

5.4 Conclusions

Digital simulations have established the feasibility of a back-to-back asynchronous dc link and a UPFC based on a rectifier/inverter pair, each being made up of 2 parallel connected modules of 7-level converters. The dc voltages at the different levels are equalized by dc choppers thus solving the problem of voltage instability inherent in multilevel converter when the ac voltage magnitudes are not equal.

In incorporating a dc chopper based dc capacitor voltage equalization system to free the back-to-back asynchronous dc link and the UPFC from the constraint that it must operate with equal ac voltage magnitudes, they enjoy the full flexibility of independent controls over the real power P and the reactive power Q_S and Q_R on either side.

CHAPTER SIX

CONCLUSIONS

Summary:

Three years ago when the research of this thesis began, there was a sudden surge of interests in multiconverters as controllers of reactive power, or STATCOMs, in Flexible AC Transmission Systems (FACTS). It dawned on researchers of FACTS controllers that the multiple-level allow the solid-state switch devices to be connected in series, thus building up a high voltage rating, without exceeding the safe voltage limit of the devices. The ability to switch the devices independently allows selective harmonic cancellations to be incorporated to lower the Total Harmonic Distortions (THDs) in the output waveforms. As both FACTS controllers and the multiconverter concept were recent arrivals to the scene, the field of research was unexplored territory.

In undertaking research in this field, the literature search and the preliminary

evaluations in chapter 1 have narrowed the focus to the diode-clamped topology as the most promising one. Chapters 2 to 5, after uncovering the characteristics of the diode-clamped topology, have found strategies which control the solid-state switches in the multi-level framework to operate as stand-alone, high-quality, high kV and high MVA FACTS controllers. In the beginning, the hope has been to perfect the multilevel STATCOM. As it has turned out, the research has been very fruitful because the number of FACTS controllers has been enlarged to include the multilevel UPFC and the multilevel back-to-back Asynchronous Link.

Contributions to Knowledge

To the best knowledge of the candidate, the research on the diode-clamped, multilevel converters as controllers of Flexible AC Transmission Systems in this thesis has made the following contributions:

(1) Extending its field of application, which up to this thesis has been limited to STATCOMs, to the Unified Power Flow Controller (UPFC) and the back-to-back Asynchronous Link.

(2) Extending the topology, which up to this thesis has been limited to the single multilevel converter, to multiple modules of multilevel converters.

(3) Extending the Fundamental Frequency Switching strategy, which up to this thesis has been restricted to selective harmonic elimination only, to include: (i) modulation index control and (ii) rms current equalization in the multiple modules.

(4) Developing methods of equalization of the DC capacitor voltages by negative feedback strategy.

(5) Developing a class B chopper-based scheme for the stabilization of voltage instability.

6.1 Extended Field of Application

Hitherto, the multilevel converter has been applied as a STATCOM only. The STATCOM functions as an electronically controllable shunt reactance or series reactance. The STATCOM is restricted to one control degree of freedom over the reactive power.

The Unified Power Flow Controller (UPFC) and the back-to-back Asynchronous Link offer three independent control degrees of freedom: the real power and the reactive powers on either side of the controller. The research of the thesis offers the conclusion that:

- The UPFC and the Asynchronous Link can be realized by the multilevel converters.

6.2 Extended Topology

In order to satisfy the hundreds of kV requirement of FACTS controllers with GTOs which are rated at 6kV, a step-down transformer stage is necessary to bridge the

transmission line voltage to the GTO-based multilevel converter voltage. As the cost of voltage insulation is high, it is preferred to keep the converter voltage low.

The high MVA requirement of the FACTS controller and the stepped-down voltage have the implication that the transformer secondary currents are much higher than can be carried by a single multilevel converter, as the GTOs are rated at 3 kA. One requisite is to ensure the equalization of the load current in the GTOs in the multiple modules. As passive equalization circuits usually incur additional losses in the auxiliary circuits, this thesis prefers active strategies based on the control over parallel connected multiple modules of multilevel converters.

The necessity to use multiple modules is made into a virtue in this thesis. Instead of switching the multiple modules in unison, each module is made to contribute actively in harmonic elimination. The degrees of freedom in the designing switching instants of the GTOs are increased by a factor equal to the number of modules.

6.3 Extended Fundamental Frequency Switching Strategy

As the early researchers in multilevel STATCOMs have limited the number of levels to N=7, the limited degrees of freedom in the Fundamental Frequency Switching strategy are used up in the selective elimination of low harmonics. The MVAR control of the STATCOM is left to the charging and discharging of the dc capacitors.

In forming an array of M modules of N-level converters, the degrees of freedom

in the Fundamental Frequency Switching strategy are increased by a multiple of *M*. Chapter 2 has shown that the increased degrees of freedom offer the following benefits:

- Direct control over the magnitude of the fundamental harmonic. The response time in the STATCOM is much faster than the indirect control of the dc link voltage, based on the charging and the discharging of the dc capacitors.
- The rms currents in the multiple modules are approximately equalized.
- The Total Harmonic Distortions (THDs) of the ac waveforms can be made as low as desired by the elimination of more and more harmonics.

6.4 DC Capacitor Voltage Equalization

The voltage across the GTOs in each level of the diode-clamped multilevel converter is circumscribed by the dc capacitor voltage across the dc buses of its level. The research into the process of charging the dc capacitor voltage in chapter 3 has yielded an important conclusion that:

- There is no inherent "mechanism" to equalize the dc capacitor voltages in the different levels.

For this reason, the equalization of the dc capacitor voltages must be "engineered"

into the FACTS controllers. The voltage equalization is, in fact, a sine qua non of FACTS controllers for two reasons. Firstly, the equal sharing of the voltage stress ensures that no excessive high voltage is applied across any GTO. Secondly, the Fundamental Frequency Switching strategy assumes equal dc voltages as the basis of selective harmonic elimination. For these reasons, chapter 3 has a significant conclusion that:

- The equalization of the dc capacitor voltages in the different levels in the diode-clamped multilevel converter can be achieved by negative feedback circuits.

It should be mentioned that the research teams of Oak Ridge National Laboratory, USA [33] and Electrical and Computer Engineering Department, University of Wisconsin-Madison [36] also discovered the same method of dc capacitor voltage equalization by negative feedback. The work of Oak Ridge National Laboratory was presented in the Industry Application Society Annual Meeting, October, 1995, Orlando, Florida. The candidate's paper appeared together with that of University of Wisconsin-Madison in Power Engineering Society 1996 Summer Meeting, July, Denver, which was late because the referees insisted on revisions. However, the editors of the *IEEE Transactions on Power Delivery* credited the paper submission date of the candidate's publication [46] as July 31, 1995. Thus, the candidate's claim to original contribution is justified.

6.5 Back-to-Back Multilevel Rectifier/Inverter Link

Research on the multilevel rectifier/inverter link is critical because it forms the core of the Unified Power Flow Controller and the back-to-back Asynchronous Link. In chapter 4, one is confronted with the conclusion (which is proven mathematically) that:

- The multilevel rectifier/inverter has voltage instability in the DC link unless their ac voltages are equal in magnitude.

The equal ac voltage magnitude constraint reduces the flexibility of control in the UPFC and the Asynchronous Link as it lowers the degrees of freedom in control from 3 to 2. Further research to overcome the potential shortcoming has yielded the conclusion:

- The voltage instability can be suppressed by a system of class B choppers which transfer the electric charge from the dc link capacitor with the higher voltage to the contiguous neighbour with the lower voltage.
- Local controls are sufficient in co-ordinating the electric charge transfers by the system class B choppers.

6.6 Suggestions for Further Work

In the research on the multilevel UPFC, the simulations have shown that the current levels of the GTOs in the Class B Choppers do not exceed 10% of the full load rating. Since the cost is critical, a more thorough study should be made covering the extreme ranges of reactive power on both sides.

The Fundamental Frequency Switching strategy has been the mainstay of the thesis because in the beginning of the research, the GTOs were considered to be the switches for FACTS controllers. At the time of the writing of the thesis, IGBTs are available at 3kV with switching frequencies at 2 kHz. At such high switching frequencies, the SPWM strategy can be used. Some preliminary research based on SPWM strategy showed that dc capacitor voltage equalization was not easy to achieve at low switching frequencies. For this reason, the thesis research did not pursue SPWM. However, the IGBTs have changed the operating constraints and there is room for future research based on the SPWM strategy

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APPENDIX A

REAL-TIME DIGITAL SYSTEM FOR EXPERIMENTAL TESTS

Two real-time digital systems have been successfully developed in Power Lab, McGill University, so that extensive experimental test of Fig.4-11 ~ Fig.4-17 for chopper-based dc capacitor voltage equalization of multilevel rectifier/inverter link can

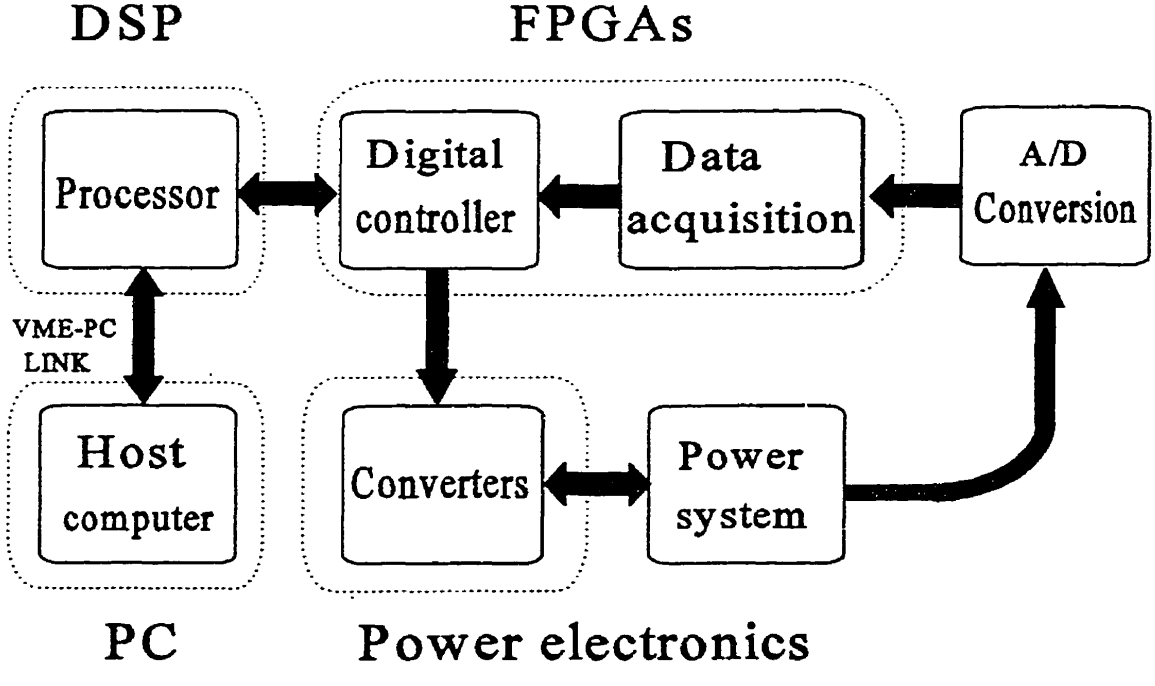


Fig.A-1 Block diagram of experimental set-up.

be performed with one digital system being used to control the multilevel rectifier/inverter link and the other to control the choppers.

A.1 Real-time Digital System

Fig.A-1 shows the block diagram of the experimental set-up and Fig.A-2 shows the overall view of the experimental facilities. The real-time data acquisition and control strategy are implemented in a digital system, which is an integration of hardware and software, including host-computer, VME-based multi-DSP [60-63] system, multiple FPGA [64] and PLD logic devices, VCO, A/D and D/A converters etc.

From Fig.4-10 and Fig.A-1, one can see that TMS320C40 DSPs and Xilinx FPGA

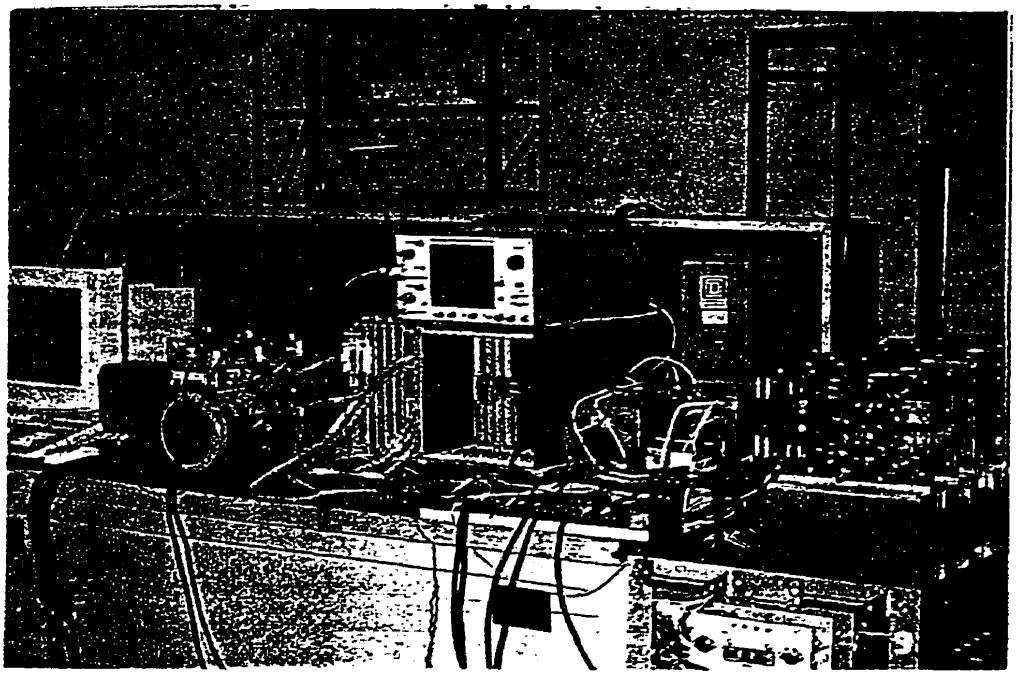


Fig.A-2 Overall view of the experimental facilities.

Table A-1 VMEbus J1/P1 Pin Assignments

Pin	(a) Signal	(b) Signal	(c) Signal
1	D00	BBSY	D08
2	D01	BCLR	D09
3	D02	ACFAIL	D10
4	D03	BG0IN	D11
5	D04	BG0OUR	D12
6	D05	BG1IN	D13
7	D06	BG1OUT	D14
8	D07	BG2IN	D15
9	GND	BG2OUT	GND
10	SYSCLK	BG3IN	SYSFAIL
11	GND	BG3OUT	BERR
12	DS1	BR0	SYSRESET
13	DS0	BR1	LWORD
14	WRITE	BR2	AM5
15	GND	BR3	A23
16	DTACK	AM0	A22
17	GND	AM1	A21
18	AS	AM2	A20
19	GND	AM3	A19
20	IACK	GND	A18
21	IACKIN	SERCLK (1)	A17
22	IACKOUT	SERDAT (1)	A16
23	AM4	GND	A15
24	A07	IRQ7	A14
25	A06	IRQ6	A13
26	A05	IRQ5	A12
27	A04	IRQ4	A11
28	A03	IRQ3	A10
29	A02	IRQ2	A09
30	A01	IRQ1	A08
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

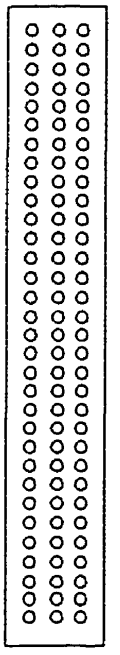
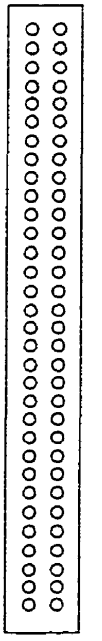


Table A-2 Ariel V-C40 Hydra ADbus pin-out

Pin	Signal	Pin	Signal
1	VCC	31	D22
2	VCC	32	D23
3	VCC	33	GND
4	GND	34	A0
5	D0	35	A1
6	D1	36	A2
7	D2	37	A3
8	D3	38	A4
9	D4	39	A5
10	GND	40	GND
11	D5	41	*STRB
12	D6	42	*RESET
13	D7	43	*RD
14	D8	44	*WR
15	D9	45	N.C.
16	GND	46	GND
17	D10	47	N.C.
18	D11	48	*INTA
19	D12	49	N.C.
20	D13	50	*INTB
21	D14	51	N.C.
22	GND	52	N.C.
23	D15	53	N.C.
24	D16	54	N.C.
25	D17	55	N.C.
26	D18	56	GND
27	D19	57	N.C.
28	GND	58	TIMER
29	D20	59	CLOCK
30	D21	60	GND



devices are the core of the digital system. To implement the phase-lock-loop, data acquisition and control logic in FPGAs, Mentor Graphics Software [65-67] and XACT development system [68] are used for schematic entry, simulation, automatic block placement and routing of the logic design and finally the creation of the configuration bit stream, and then the configuration data is loaded from DSP into the internal memory cells of the daisy-chained FPGA devices for customization. Since FPGA devices can be reprogrammed an unlimited number of times, they provide valuable flexibility for different experimental tests. The complicated mathematical manipulation and control algorithm can be performed by DSPs. DSPs also store some valuable data, such as switching patterns of Appendix B. DSPs are interfaced with FPGAs, so that DSPs can address

FPGAs and FPGAs can interrupt DSPs.

A.2 System Interfaces

Table A-1 [69] and Table A-2 [60] show the VMEbus J1/P1 and Ariel V-C40 Hydra ADbus pin assignments respectively. The PCBs for control and data acquisition must be compatible to VMEbus and ADbus pin assignments..

ADbus is a 24-bit parallel bus to provide signal I/O capabilities to the DSPs independent of the VME bus, so that the DSPs can address the FPGAs. Fig.A-3 and Fig.A-4 show the ADbus timing diagram of its read cycle and write cycle respectively.

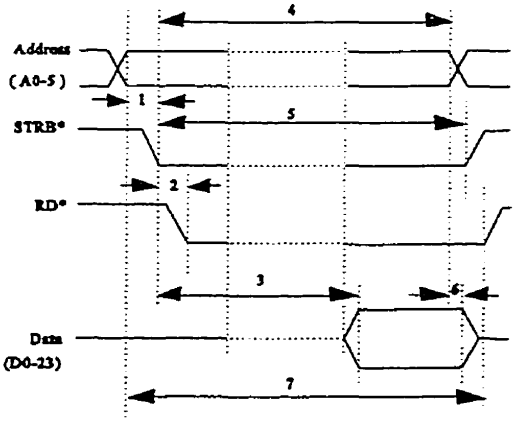


Fig.A-3 ADbus timing diagram: read cycle.

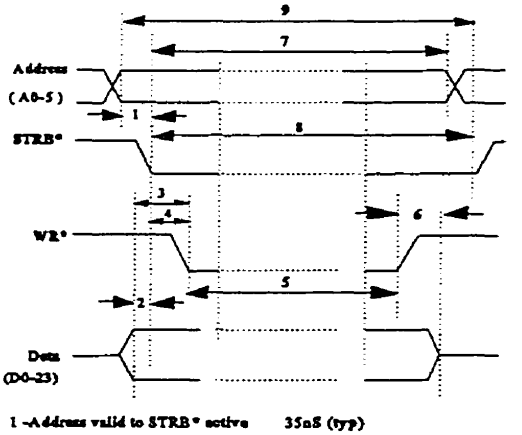


Fig.A-4 ADbus timing diagram: write cycle.

The clock frequency on pin 59 of the ADbus is 20MHz. *INTA and *INTB on pin 48 and 50 of the ADbus are buffered , logical Ored and connected to the IIOF3 pin of DSP#2. They provide the FPGAs devices and V-C40 internal TIMERs the capability to interrupt the DSPs. As an example, two interrupt routine are detailed in section A.3.

A.3 DSP Programs

DSP programs contain the interrupt routines to perform mathematical manipulation and control algorithms. They can address, write or read FPGAs.

To run a DSP program, it must be first compiled and linked using Texas Instrument's C compiler and linker for C40.

Fig.A-5 illustrates the TMS320C40 DSP development flow. The C compiler accepts C source code, fpga.c for example, and produces TMS320C40 assembly language source code, then the assembler translates assembly language source files into machine COFF (Common Object File Format) object file. The linker combines object files into a single executable object module. The object library, rts40.lib, contains standard runtime-support functions, compiler utility functions and math functions that can be called from C programs that have been compiled for TMS320C40. The typical command lines for compiling and linking are:

- cl30 -v40 fpga.c
- lnk30 fpga.lnk

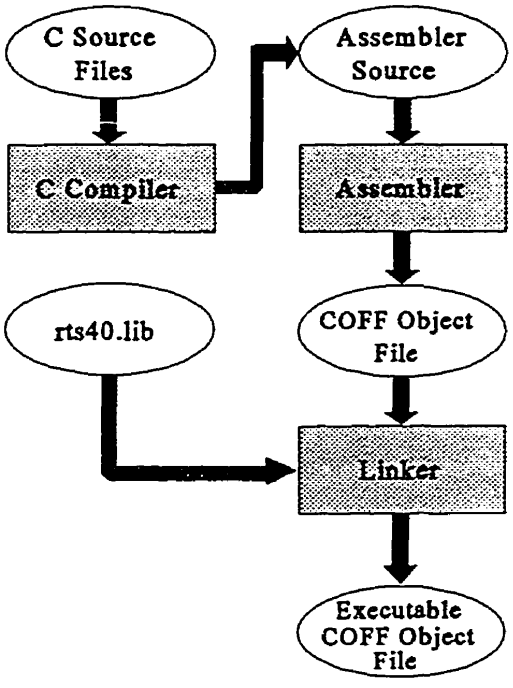


Fig.A-5 DSP program development flow.

The content of fpga.lnk is shown in Table A-3. Its MEMORY and SECTIONS directives describe a basic memory configuration of the target processor. As specified in fpga.lnk, the whole process creates an executable COFF object file named fpga.out.

Once the DSP program has been compiled and linked, the executable code exists in a COFF file and it can be loaded into a specified DSP. Then the DSP will automatically start running the program. The typical command line for loading a DSP program from the host computer into a specified DSP is:

- load -v 0xf100 a2 fpga.out

Table A-4 shows a DSP program written in C language for chopper-based dc capacitor voltage equalization of multilevel rectifier/inverter link to get the experimental

results of Fig.4-11 ~ 4-17. It includes 2 interrupt routines: (i) c_int1( ) to control the data acquisition and (ii) c_int2( ) to control the chopper. Fig.4-5 and Fig.4-6 explain the control algorithm of the interrupt routine c_int2( ). The DSP program also includes 4 head file: (i) address.h of Table A-5, (ii) bits.h with bitstreams obtained from Mentor Graphics Software and XACT Development System for FPGA design, (iii) math.h for function declarations and (ix) hydra.h for macros and utilities definition.

Table A-3 fpga.lnk for basic memory configuration of DSP

```
/* $Id: fpga.lnk,v 1.2 1996/04/09 16:14:47 tpa Exp $ */
fpga.obj
setivec.o40

-o fpga.out
-m fpga.map
-cr                /* LINK USING C CONVENTIONS    */
-stack 0x100       /* 1K STACK                    */
-heap  0x400       /* 1K HEAP                     */
-lrts40.lib        /* GET RUN-TIME SUPPORT        */

MEMORY
{
RAMBLK0:     o = 0002FF800h     l = 400h
RAMBLK1:     o = 0002FFC00h     l = 400h
L_ADBUS:     o = 000300000h     l = 10000h
INT_VECTS:   o = 040000E00h     l = 200h
L_SRAM:      o = 040001200h     l = 3400h
G_SRAM:      o = 0C0000000h     l = 4000h
G_JTAG:      o = 081040000h     l = 100h
}

SECTIONS
{
.text:  > L_SRAM        /* CODE                          */
.cinit: > L_SRAM        /* INITIALIZATION TABLES         */
.const: > L_SRAM        /* CONSTANTS                     */
.stack: > RAMBLK1       /* SYSTEM STACK                  */
.sysmem: > L_SRAM       /* DYNAMIC MEMORY (HEAP)         */
.bss:   > L_SRAM        /* VARIABLES                     */
}
```

Table A-4 DSP program for chopper-based dc capacitor voltage equalization

```
/*  Program: chop6.c, a DSP program for chopper system control */
        This program succeeds in putting three capacitors in series. Since the capacitors are parallelled with resistances of different size. Their dc voltages become unequal. When the chopper system is put into operation, the dc voltages are successfully equalized. It is important to put more than 150 difference in PWM registers so that there are enough switching delay to prevent shoot-through.
        I use some available facilities (either the FPGA design in 'bits3.h' or C programming) for chopper control. For example, the number of the triangle actually specifies the frequency of data_acquisition. When the triangle number is 57 every utilities cycle, the sampling period is: 16.7ms/(2*57)=150 us. It appares in "PWM_counter" as 20,000,000(Mhz)/(57*60*2) = 3000; These information is also useful when hardware interlock in PLD is not appliable and software interlock (in this program) is developed. The swiches of the chopper circuit requires 5-8 us to interlock.
    This program makes a modification so that the switches will be kept on when v_average <v_n<v_average*tolerence.

Note:Must run " *PWM_register_c2 = 0xFFFFFFFF; " to start the counter in every sampling period.

Orginization of the program:
    (1) "setivec.o40" must be available in the same subdirectory.
    (2) after running "cl30 -v40 chop6.c", chop6.obj is obtained.
    (3) in order to utilize the fpga.lnk. the chop6.obj is renamed as fpga.obj because that is the name of input obj file in the fpga.lnk file.
    (4) Then running lnk30 fpga.lnk. The fpga.out file is obtained which could be "load -v 0xf100 a2 fpga.out" and the chop6's function will be implemented successfully */

#include "address.h"
#include "math.h"
#include "hydra.h"
#include "bits.h"
#define TINT1 (0x2b)            /* Timer 1 internal interrupt */
#define LED 0x00200000          /* LED bit in MCR */
#define IIOF3 (0x6)
#define TableLen 8192
#define PI 3.1415926
#define System_Clock 20000000
#define Mod_Freq 60
#define Tri_Number 21

long cont,n_samp,set,val,val2,val3,current;
double v_dc, v_dc1, v_dc2, v_dc3, v_dc_upper,
       v_dc_lower;
int a1, b1;
/* int sinx[16384]; */
long sinx, current_a_phase, Im;
float ModIndexf, m_index=0.8;
int SHIFT, PWMcount, f_triangle,
f_sample,ModIndex;
long time;
void c_int01( void );   /* this is handler function */
void c_int02( void );

main()
{

int i,j,M,N;
char L1;
i=sizeof(bits)/sizeof(bits[0]);
n_samp=0;
GIE_ON()
for(j=0;j<=i;j++)
{
L1=bits[j];
for(N=0; N<32; N++)
 {
*load_or_start_sample=L1;
L1= L1 << 1;
 }
 }

for(i=0;i<2000;i++) { }

*PLL_VCO=0xC2FF0000;   /* for 60 hz */

for(j=0;j<100;j++)
{
for(i=0;i<20000;i++) { }  /* the PLL have not started working, must wait */
}                                   /* so long, otherwise, wrong data obtained for val */
```

```
/* for PWM */
f_triangle=Mod_Freq*Tri_Number; /* frequency of
triangle waveform */

f_sample=f_triangle*2;        /* sampling frequency
*/
PWMcount=System_Clock/f_sample;
*PWM_half_triangle_counter=PWMcount<<16;;
SHIFT=PWMcount/2;
ModIndexf=SHIFT*m_index;  /*  initialize  the
Modulation Index */
Im=14000; /* equivalent to 2.4 ampers */
for (j=0;j<TableLen;j++)
{
bits[j]=(int)(Im*sin(2*PI*j/TableLen));
bits[j]=bits[j]+Im+Im/2;      /* upper-shift to get
always  positive  value  to  compare  with
current_a_phase */
}

/                                                *
**************************************
**************************************
```

The following 5 instructions are necessary for setting and enabling either internal or external interrupt. The "iack" instruction acknowledge the external interrupt for initialization. Without "GIE_ON", "iack", or withour "setivec", it will not work".

```
**************************************
**************************************/

GIE_ON();                /* enable global interrupt
interrpts */
                         /* in hydra.h, GIE_ON() is
defined as  asm ("or 02000h, st"); */
asm(" push ar0");
asm(" ldhi 4000h,ar0");
asm(" iack *ar0");
asm(" pop ar0");

setivec(IIOF3,c_int01);
asm( " or 9000h,iif" );

set=0;

*PWM_register_c2=0xFFFFFFFF; /* starting the
counter */
*PWM_register_a1=0xFFFFFFFF;
*PWM_register_a2=4<<16;
for(i=0;i<10;i++) { }
*PWM_and_interrupt_enable=0x300;  /* 0x300 */
while (1)
 {
 }

}


/                                                *
**************************************
**************************************** */
/* The Interrupt Handler Routine to read the data
from FPGA.
   FPGA receives and stores in registers the 16-bit
digital number outputted in series by AD677, the
analog-to-digital converter. After the hardware
finishs the data acquisition, its "busy" bit edges down
and initiates the interrupt signal "IIOF3" of DSP2 of
HYDRA1 from AD_BUS, tells DSP that the data is
ready. This handler routine will read the data */
/                                                *
**************************************
**************************************** */

void c_int01( void )
{
asm(" push ar0");
asm(" ldhi 4000h,ar0");
asm(" iack *ar0");
asm(" pop ar0");

setivec(IIOF3,c_int02);
asm( " or 9000h,iif" );

*load_or_start_sample=0x0;
}

/* ************ Routine for the chopper control
******************** */

void c_int02( void )
{
val=*(read_data_channel_2);
val2=*(read_data_channel_3);
val3=*(read_data_channel_5);
v_dc1=(val>>8) & 0x0000FFFF; v_dc2=(val2>>8)
& 0x0000FFFF;
v_dc3=(val3>>8) & 0x0000FFFF;
v_dc2=v_dc2/0.915; v_dc3=v_dc3/0.9;

v_dc=(v_dc1+v_dc2+v_dc3)/3;
v_dc_upper=v_dc*1.016; v_dc_lower=v_dc/1.016;
```

```
if(v_dc1>v_dc_upper ) a1=1;
else if( v_dc2>v_dc_upper & v_dc1<v_dc_lower )
a1=-1;

/* when a1 or b1 =1, they will charge middle
capacitance */

if( v_dc3>v_dc_upper ) b1=1;
else if( v_dc2>v_dc_upper & v_dc3<v_dc_lower )
b1=-1;

if( a1==1 )
  {
      if      (      v_dc1<v_dc      )      {
*PWM_register_a1=0xFFFFFFFF;

*PWM_register_a2=4<<16; a1=0;
                    }
    else {    *PWM_register_b1=0xFFFFFFFF;
*PWM_register_b2=4<<16;
                  *PWM_register_a1=270<<16;
*PWM_register_a2=0xFFFFFFFF; }
  }
  else if( a1==-1 )
  {
             if     (     v_dc2<v_dc     )     {
*PWM_register_b1=0xFFFFFFFF;

*PWM_register_b2=4<<16; a1=0; }
      else  {  *PWM_register_a1=0xFFFFFFFF;
*PWM_register_a2=4<<16;
                   *PWM_register_b1=270<<16;
*PWM_register_b2=0xFFFFFFFF; }

  }

 if( b1==1 )
  {

if      (      v_dc3<v_dc      )      {
*PWM_register_d1=0xFFFFFFFF;

*PWM_register_d2=4<<16; b1=0;
/* also start counter */
 *PWM_register_c1=0xFFFFFFFF;

*PWM_register_c2=4<<16;
                        }
  else { *PWM_register_d1=270<<16;
 *PWM_register_d2=0xFFFFFFFF;
  *PWM_register_c1=0xFFFFFFFF;
 *PWM_register_c2=4<<16; }
  }
 else if( b1==-1 )
  {
  if( v_dc2<v_dc ) {
 *PWM_register_c1=0xFFFFFFFF;

*PWM_register_c2=4<<16; b1=0; }
 else { *PWM_register_d1=0xFFFFFFFF;
 *PWM_register_d2=4<<16;
 *PWM_register_c1=270<<16;
 *PWM_register_c2=0xFFFFFFFF; }
  }
else            *PWM_register_c1=0xFFFFFFFF;
*PWM_register_c2=4<<16;

/* *PWM_register_c2=0xxxxx  also starting the
counter */
/* don't forget to start the counter in any situation */

/                                                    *
*****************************************
******************** */

/* if( (val2>>8 & 0x0000FFFF) >10000)

if(n_samp<4000)
{

n_samp=n_samp+1;
if(n_samp>=2000)
{
current=*(read_data_channel_4);
global_mem1=global_mem1+1;
 *global_mem1=current<<8;

}
}                 */
/* ***************** */

*MCR^=LED;

asm(" push ar0");
asm(" ldhi 4000h,ar0");
asm(" iack *ar0");
asm(" pop ar0");

setivec(IIOF3,c_int01);
asm( " or 9000h,iif" );
}
```

Table A-5 Head file of the DSP program for ADbus address definition: Address.h

```
/* November 2, 1996
        This head file contains the Hydra I address for data acquisition, phase-lock-loop and Pulse-width-modulation control in FPGAs. The A5 of ADbus is connected to the "RD" of the data acquisition (without change of the design for HYDRA II). While A4 (effective at low) will enable the addressing of the data acquisition design. When A5=0 and A4=0, the write or read cycle will start the sampling. When A5=1 and A4=0, the read cycle will read the data from the one of the 15 registers (received from AD converter) specified by address lines A0-A3. Since A4 (active at low) replace "RD" line, so the write and RD signal line of AD_bus is not connected to the data_acquisition board , therefore, 0x30000x (*load_or_start_sample) of AD_bus to be addressed by DSP 2 is reserved only for start-sampling and 0x30002x is reserved for reading the data acquisition results. (x=1-A, or 1st-15th channel). All other addressing should avoid these addresses. Please note that there is only six address line (a0-a5).

(1)*PWM_register_a1 is for upper
**************************************
so, only 0x30001x or 0x30003x are available for application other than data-acquisition.
**************************************
*/

long *timer1_glb = (long *)0x00100030;
 /* address of timer 1 global register */
long *timer1_prd = (long *)0x00100038;
/* address of timer 1 period register */
long *MCR = (long *)0xbf7fc008;
 /* address of the MCR */

/* Addressing the data acquisition board */

long *load_or_start_sample = (long *)0x00300000;
long *read_data_channel_1 = (long *)0x00300021;
long *read_data_channel_2 = (long *)0x00300022;
long *read_data_channel_3 = (long *)0x00300023;
long *read_data_channel_4 = (long *)0x00300024;
long *read_data_channel_5 = (long *)0x00300025;
long *read_data_channel_6 = (long *)0x00300026;
long *read_data_channel_7 = (long *)0x00300027;
long *read_data_channel_8 = (long *)0x00300028;
long *read_data_channel_9 = (long *)0x00300029;
long *read_data_channel_10 = (long *)0x0030002a;
long *read_data_channel_11 = (long *)0x0030002b;
long *read_data_channel_12 = (long *)0x0030002c;
long *read_data_channel_13 = (long *)0x0030002d;
long *read_data_channel_14 = (long *)0x0030002e;
long *read_data_channel_15 = (long *)0x0030002f;
long *global_mem = (long *)0x8d0ff7d0;
/* base address of the global memory */
long *global_mem1 = (long *)0x8d0ff7da;
/* start of the data block */

/* addressing the PWM part */
long *PWM_register_a1=(long *)0x00300030;
long *PWM_register_a2=(long *)0x00300031;
long *PWM_register_b1=(long *)0x00300032;
long *PWM_register_b2=(long *)0x00300033;
long *PWM_register_c1=(long *)0x00300034;
long *PWM_register_c2=(long *)0x00300035;
long *PWM_register_d1=(long *)0x0030003d;
/* for chopper test */
long *PWM_register_d2=(long *)0x0030003e;
 /* for chopper test */
long *PWM_half_triangle_counter=(long *)0x00300036;
long *read_PLL_VCO=(long *)0x00300037;
long *read_time_axis=(long *)0x00300038;
/* from MicroP_out of pll_b1 design the data from *read_time_axis from lowed VCO frequency output will address 4096 numbers (of one cycle sin waveform) in DSP program table as the modulation signal of PWM strategy */
long *PLL_VCO=(long *)0x00300039;
/* for 60 hz */
long *PWM_and_interrupt_enable=(long *)0x0030003a;
```

APPENDIX B

SWITCHING ANGLE TABLE OF 2 MODULES OF 7-LEVEL CONVERTERS

Chapter 2 describes the way to design the switching angles of multiple modules of multilevel converters to achieve multiple control targets. This appendix lists the switching angles of 2 modules of 7-level converter solved numerically from equations of (2-2), (2-3) and (2-5) by Matlab Software. The solutions are also plotted as a function of the equivalent voltage magnitude of V_1 in Fig. 2-3(a) and utilized in the research which are described in chapter 3 ~ chapter 5. The switching angles for M modules of N-level converters can be obtained from solving equations of (2-14), (2-17) and (2-19) and the similar solutions can be achieved.

Table B-1 Switching Angles of 2-module of 7-level converter

V_1(pu)	α_{31}	α_{21}	α_{11}	α_{32}	α_{22}	α_{12}
0.48	35.36	72.84	88.00	47.03	58.70	90.00
0.52	35.40	70.09	85.80	45.95	57.50	90.00
0.53	35.74	68.75	85.10	45.18	57.22	89.50
0.54	36.58	67.19	84.90	43.86	57.29	88.40
0.55	38.08	65.48	84.00	42.09	57.53	87.70
0.56	39.20	64.76	83.19	40.80	57.58	87.69
0.56	39.20	64.58	82.52	40.70	57.42	87.94
0.57	39.90	64.34	81.98	39.90	57.30	88.03
0.57	40.30	64.19	81.42	39.30	57.12	88.16
0.59	41.20	64.00	80.38	38.50	56.65	88.36
0.59	42.70	63.75	77.59	36.15	54.87	88.59
0.62	43.30	63.91	77.05	35.40	54.32	88.75
0.62	43.00	62.88	75.21	35.15	53.52	87.72
0.67	42.80	62.24	73.97	35.00	52.97	86.85
0.68	41.80	35.00	60.24	51.37	70.19	82.73
0.70	41.25	58.78	69.36	35.00	51.19	80.14
0.70	40.71	55.39	34.23	69.87	52.59	76.50
0.72	41.43	52.74	69.70	32.04	53.86	74.70
0.73	41.57	52.40	69.50	31.42	53.89	74.40
0.74	41.60	51.49	68.60	29.56	54.03	73.80
0.74	41.52	51.29	68.30	29.07	54.06	73.70
0.75	41.31	51.30	68.00	28.48	53.88	73.50
0.76	40.69	51.18	67.20	27.20	53.68	73.20
0.77	39.27	51.22	66.00	25.28	53.18	72.70
0.76	37.34	51.89	65.00	23.38	51.89	71.90
0.78	36.73	51.72	64.90	22.96	51.72	71.60
0.80	33.99	51.51	63.80	20.95	50.62	70.50
0.81	32.99	50.90	63.70	20.46	50.67	69.90
0.81	32.44	51.30	63.60	20.21	49.97	69.60
0.82	31.67	50.34	63.70	19.99	50.52	69.00
0.83	29.93	49.09	64.00	19.67	50.90	67.50
0.83	28.80	48.22	64.60	19.62	51.28	66.10
0.84	27.49	46.39	65.50	19.43	52.48	64.00
0.85	26.66	44.60	66.30	18.89	53.69	62.00
0.85	26.29	43.64	66.60	18.48	54.29	61.00
0.86	25.97	42.28	67.10	17.67	55.08	59.50
0.86	25.69	41.67	67.10	17.37	55.32	59.00
0.86	25.41	41.03	67.10	17.03	55.50	58.50
0.87	25.16	40.41	67.10	16.67	55.56	58.10
0.87	24.94	40.06	67.00	16.52	55.50	58.00
0.87	24.83	39.79	67.00	16.35	55.43	57.90
0.88	24.36	38.66	66.90	15.68	54.82	57.80
0.88	24.16	37.14	67.30	14.25	53.00	58.30
0.89	23.63	36.26	67.00	13.85	52.42	58.20
0.90	22.83	34.81	66.50	13.15	51.18	58.10
0.91	22.55	34.00	66.50	12.55	50.32	58.00
0.92	21.93	32.60	66.00	11.88	48.97	58.00
0.93	21.47	31.47	65.50	11.41	47.89	58.00
0.94	21.12	30.50	65.00	11.01	46.91	58.00
0.96	20.28	27.04	64.00	9.28	43.23	57.00
0.98	18.58	25.13	62.50	8.77	39.48	56.20

APPENDIX C

PARAMETERS OF FIG.3-2 AND FIG.3-6

C.1 Fundamental Frequency Switching Strategy

(K_p = rad/pu.volt, K_i = rad/(s · pu.volt))

$1/\omega C_1 = 1/\omega C_6 = 0.100$pu,	$K_{p1} = K_{p6} = 0.40$,	$K_{i1} = K_{i6} = 0.30$;
$1/\omega C_2 = 1/\omega C_5 = 0.100$pu,	$K_{p2} = K_{p5} = 0.35$,	$K_{i2} = K_{i5} = 0.25$;
$1/\omega C_3 = 1/\omega C_4 = 0.100$pu,	$K_{p3} = K_{p4} = 0.35$,	$K_{i3} = K_{i4} = 0.20$;
$K_1 = 0.1$,	$K_2 K_3 = 3.5$;	
$X_{L1} = 0.08$pu ,	$R_1 = 0.02$pu;	

C.2 Sinusoidal Pulse Width Switching Stragegy

(K_p = rad/p.u.volt, K_i = rad/(s · pu.volt))

$1/\omega C_1 = 1/\omega C_6 = 0.240$pu,	$K_{p1} = K_{p6} = 0.15$,	$K_{i1} = K_{i6} = 0.12$;
$1/\omega C_2 = 1/\omega C_5 = 0.125$pu,	$K_{p2} = K_{p5} = 0.08$,	$K_{i2} = K_{i5} = 0.10$;
$1/\omega C_3 = 1/\omega C_4 = 0.125$pu,	$K_{p3} = K_{p4} = 0.08$,	$K_{i3} = K_{i4} = 0.10$;
$K_1 = 0.1$,	$K_2 K_3 = 5.0$;	
$X_{L1} = 0.08$pu,	$R_1 = 0.02$pu;	

APPENDIX D

PARAMETERS OF FIG.4-9 AND FIG.4-6

D.1 Chopper of Fig.4-9

$C_1 = 6000$ MFD, $C_2 = 6000$ MFD, $C_3 = 6000$ MFD;

$L_{12} = 6.67$ mH, $L_{23} = 6.67$ mH;

D.2 DSP Control of Fig.4-9 Using the Algorithm of Fig.4-6

As shown in interrupt routine c_int02( ) of Table A-4, $V_{max} = 1.016\ V_o$ and $V_{min} = V_o/1.016$.

APPENDIX E

PARAMETERS OF FIG.5-1 AND FIG.5-2

E.1 Rectifier/inverter Link

$\omega_o = 377$ rad/s, $\omega_o L_{S1} = 0.1$ pu, $\omega_o L_{S2} = 0.01$ pu, $\omega_o L_{R1} = 0.1$ pu, $\omega_o L_{R2} = 0.01$ pu;

$1/(\omega_o C_j) = 0.12$ pu (j=1,2 ... 6).

E.2 Chopper

$\omega_o L_{12} = 12$ pu, $\omega_o L_{23} = 12$ pu, $\omega_o L_{45} = 12$ pu, $\omega_o L_{56} = 12$ pu.

APPENDIX F

PARAMETERS OF FIG.5-3

F.1 Rectifier/inverter Link

$\omega_o = 377$ rad/s, $\omega_o L_{S1} = 0.1$ pu, $\omega_o L_{S2} = 0.01$ pu, $\omega_o L_{R1} = 0.1$ pu, $\omega_o L_{R2} = 0.01$ pu;

$1/(\omega_o C_j) = 0.12$ pu (j=1,2 ... 6).

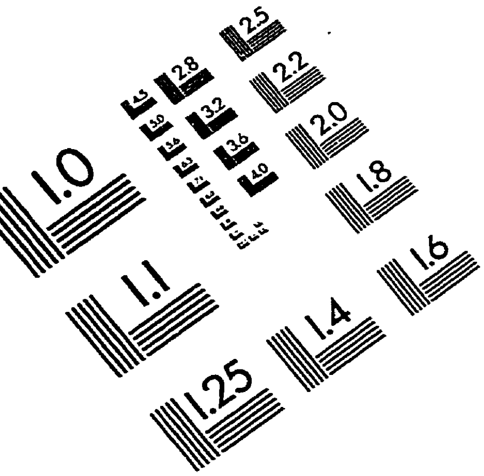
F.2 Chopper

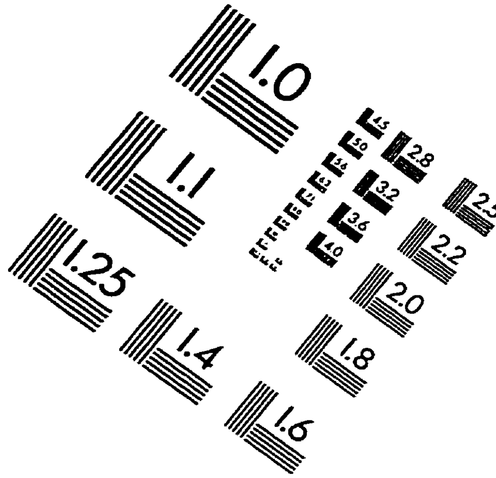
$\omega_o L_{12} = 1$ pu, $\omega_o L_{23} = 1$ pu, $\omega_o L_{45} = 1$ pu, $\omega_o L_{56} = 1$ pu.

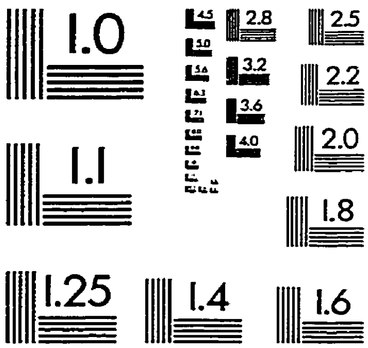
F.3 Transmission Line

$\omega_o L = 0.035$ pu, $R = 0.01$pu;

IMAGE EVALUATION TEST TARGET (QA-3)

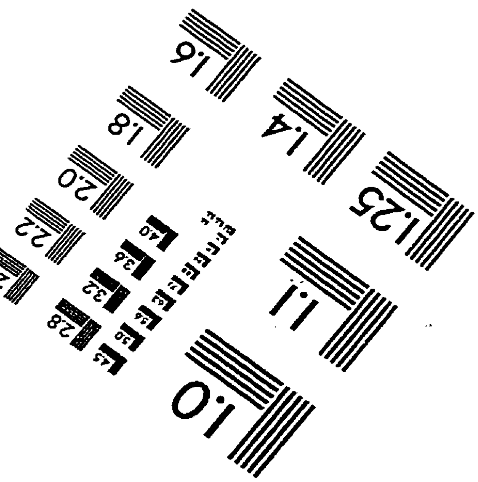


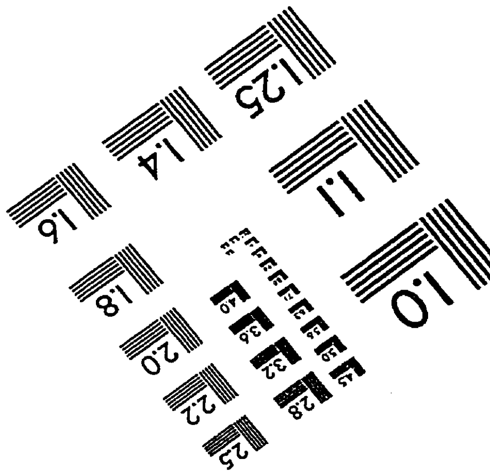




150mm

6″





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