Computationally efficient and fabrication error tolerant inverse-designed mode converters and mode-division (de)multiplexers

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Abstract

The explosion in data processing, storage, and communication of present time demands for consistent growth of cloud services and supporting hardware technologies. Silicon photonics (SiPh) offers higher data transmission and processing speed at low latency and low thermal dissipation. One of the current research drives in SiPh is to achieve dense integration of photonic interconnects. Computational inverse design techniques have shown potential to become reliable means for designing compact nanophotonic devices. Much effort has been made to obtain final designs that are robust to fabrication imperfections. In this work, we experimentally demonstrate optical mode converters (MCs) on the silicon-on-insulator platform designed using the computationally efficient shape optimization method. The mode conversion is performed between different transverse electric (TE) mode pairs among TE0, TE1, TE2, and TE3 modes. These MCs have mode conversion efficiencies above 95%, and the insertion loss ranging from 0.3 dB to 1 dB over a wavelength span of 80 nm ranging from 1.5 μm to 1.58 μm. Maximum modal crosstalk found experimentally in the C-band is -19 dB. The conversion efficiency drops at most by 2.2% at 1.55 μm for 10 nm over/under etch, implying good robustness to dimensional variations. To characterize their performance in the time domain, a 28 Gbps on-off keying (OOK) and a 20 GBaud pulse amplitude modulation (PAM-4) payload transmissions were performed, which supports their utility for high throughput data communications. The open eye diagrams exhibit Q-factors of 8 dB. Additionally, the mode conversion mechanisms of these MCs are investigated by studying the simulated electromagnetic field patterns and validated by supportive data. This interpretation of the working principles leads to formulating the optimization such that more efficient designs are obtained without requiring larger design area. It also guides to a two-step design approach for dealing with relatively more complex design problems.

Inverse design usually deals with many design parameters, and the optimized designs are eventually the local optima in the non-convex design parameter space. But a local optimum may not turn out to be a good design with acceptable performance. A collection of good designs is very useful, since one design may turn out to be superior to the rest for an application-specific performance attribute. An exhaustive search for all the good designs in a given parameter space is computationally burdensome. To reduce the computation cost involved with the 3D optimization

of any type of optical interconnect which can be designed in the shape optimization method, a machine learning-based regression model has been proposed and implemented to the TE0-TE1 mode converter design for a demonstration. It shows a reduction of the computation load by 35% in the 3D optimization step, which is the most computationally expensive part.

Finally, using the density topology optimization technique, several three-channel mode-division (de)multiplexers (MDMs) are designed with a design footprint of 4.5×4.5 μm^2. Experimental results show maximum insertion loss of 1.2 dB and channel crosstalk below -18 dB in the C-band (1.53 – 1.565 μm). A physics-guided approach is adopted for faster convergence to the optimum designs. An aware selection of the initial design parameters shows some advantage over the random selection of the starting conditions. However, the optimized designs are sensitive to fabrication imperfections. The channel crosstalk increases by several folds after fabrication (~6 dB on average).

Abrégé

L'explosion actuelle du traitement, stockage et la communication de données exige une croissance constante des services informatiques. La photonique en silicium (SiPh) offre une vitesse de transmission et de traitement des données plus élevée avec une faible latence et une faible dissipation thermique. L'un des axes de recherche actuels en SiPh consiste à réaliser une intégration dense des interconnexions photoniques. Les techniques numériques de conception inverse ont montré qu'elles pouvaient devenir des moyens fiables pour concevoir des dispositifs nanophotoniques compacts. De nombreux efforts ont été déployés pour obtenir des conceptions robustes aux imperfections de fabrication. Dans ce travail, nous démontrons expérimentalement des convertisseurs de mode optiques sur la plate-forme de silicium sur isolant qui ont étés conçus en utilisant la méthode d'optimisation numérique de conception inverse. La conversion de mode est effectuée entre différentes paires de modes transverses électriques (TE), parmi lesquelles figurent TE0, TE1, TE2 et TE3. Ces convertisseurs de mode présentent des efficacités de conversion supérieures à 95 %, et des pertes d'insertion allant de 0.3 dB à 1 dB pour des longueur d'onde allant de 1.5 µm à 1.58 µm. La diaphonie modale maximale trouvée expérimentalement dans la bande C est de -19 dB. Le rendement de conversion chute jusqu'à 2.2% à 1.55 µm pour une sur-/sous-gravure de 10 nm, ce qui implique une bonne robustesse aux variations dimensionnelles. Pour caractériser les performances dans le domaine temporel et valider l'utilité pour les communications de données à haut débit, des tests OOK (on-off keying) à 28 Gbps et PAM-4 (modulation d'amplitude) à 20 GBauds ont été réalisées. Les diagrammes à œil ouverts présentent des facteurs de qualité de 8 dB. De plus, les mécanismes de conversion de mode de sont étudiés en simulant les champ électromagnétiques et validés par des données de référence. Ceci permet d'obtenir des conceptions plus efficaces à taille égale, et mène vers une approche de conception en deux étapes pour traiter des problèmes de conception plus complexes.

La conception inverse optimise de nombreux paramètres à la fois, et les résultats sont idéalement les optima locaux dans l'espace non convexe de paramètres. Mais un optimum local peut ne pas s'avérer être une conception avec performances acceptables. Avoir une sélection de bonnes conceptions est très utile, car une conception peut s'avérer supérieure aux autres pour un attribut de performance spécifique à une application. Une recherche exhaustive de tous les bons

modèles dans un espace de paramètres donné est très coûteuse en termes de calcul. Afin de réduire le coût de calcul lié à l'optimisation 3D de tout type d'interconnexion optique pouvant être conçue par la méthode d'optimisation de forme, un modèle de régression basé sur l'apprentissage automatique a été proposé et mis en œuvre pour la conception du convertisseur de mode TE0-TE1 à titre de démonstration. Il montre une réduction de la charge de calcul de 35% dans l'étape d'optimisation 3D, qui est la partie la plus coûteuse en calcul.

Enfin, en utilisant la technique d'optimisation de la topologie de densité, plusieurs (dé)multiplexeurs de mode à trois canaux sont conçus avec une empreinte de 4.5×4.5 μm^2. Les résultats expérimentaux montrent une perte d'insertion maximale de 1.2 dB et une diaphonie de canal inférieure à -18 dB dans la bande C (1.53 – 1.565 µm). Une approche guidée par la physique est adoptée pour une convergence plus rapide vers le résultat optimale. Une sélection consciente des paramètres de conception initiaux présente un certain avantage par rapport à la sélection aléatoire des conditions de départ. Cependant, les conceptions optimisées sont sensibles aux imperfections de fabrication. La diaphonie du canal augmente considérablement après fabrication (~6 dB en moyenne).

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List of Acronyms

ASE	Asynchronous Source Noise
ASIC	Application Specific Integrated Circuit
CE	Conversion Efficiency
CW	Continuous Wave
CMOS	Complementary Metal Oxide Semiconductor
DCA	Digital Communication Analyzer
DUT	Device Under Test
EDFA	Erbium Doped Fiber Amplifier
FPGA	Field Programable Gate Array
GC	Grating Coupler
IL	Insertion Loss
MC	Mode Converter
MDM	Mode Division Multiplexer
MMI	Multimode Interference
MZI	Mach-Zehnder Interferometer
OOK	On-Off Keying
PAM	Pulse Amplitude Modulation
PC	Polarization Controller
PDK	Process Design Kit
PDM	Polarization-Division Multiplexing
PIC	Photonic Integrated Circuit
PPG	Programmable Pattern Generator

PRBS	Pseudo Random Bit Sequence
SiPh	Silicon Photonic
SNR	Signal to Noise Ratio
SOI	Silicon on Insulator
TE	Transverse Electric
TM	Transverse Magnetic
Tx	Transmission
XT	Crosstalk
VCSEL	Vertical Cavity Surface Emitting Laser
VOA	Variable Optical Attenuator
WDM	Wavelength-Division Multiplexing

Chapter 1

Introduction

Increasing diversity in electronic devices and their applications in our daily lives have led to creating, storing, and communicating enormous amount of digital information. This explosion in data processing, storage, and communication demands for consistent growth of cloud services and supporting hardware technologies. Besides preserving the useful shared and stored data, to meet the demand of the tremendous amount of information being generated, the large-scale restructuring the datacenters is one of the most dynamic transformations happening in the information technology. Emerging technologies, such as autonomous vehicles, demand for instantaneous responsiveness among machines, which requires ultrafast cloud computing, cognitive computing, data transmission to ensure timely response. Since light can carry considerably more information than electrical signals, light has traditionally been utilized for long-haul data transmission, which is facilitated by optical fibers and satellites, covering wide bandwidth and causing low thermal dissipation. Further progress in optics and photonics brought photonic devices closer to the die. Presently, electro-optic devices and photonic interconnects are directly designed on chip to build application specific integrated circuits (ASICs), field programmable gate array (FPGA), and even processors for machine learning computations.

1.1 Silicon photonic interconnects

Digital electronics is facing the limit of Moore's law, and Dennard Scaling (energy density of shrinking transistors) has reached its end, which demands for a new technology that offers higher data transmission and information processing speed, low latency, and most importantly low energy dissipation. Recent progress in integrated photonics and fiber optic systems has largely eliminated several bottlenecks of the electronic systems and provided viable solutions for large-scale datacenters, high-speed telecommunication, and digital information processing. Until late 1990s no reasonable solution for the precise measurement of optical frequencies existed. Later, optical clocks for atomic timekeeping and electro-optic sampling systems led to frequency synthesizers that allowed the synthesis of both optical and microwave frequencies [1]. Nowadays, a single optical source can provide tens to thousands of optical frequency lines for massive parallelization in wavelength-division multiplexed (WDM) systems [2] and thus address the rapid growth of data traffic on the internet and in data centres. Combined with WDM, polarization-division multiplexing (PDM) [3] and mode-division multiplexing (MDM) [4] have further facilitated incorporating additional data channels using the same wavelength.

Usually, a typical datacenter server generation lasts 3-5 years while the infrastructure undergoes reconstruction every 3-5 generations. Thus, the choice of technology adopted today becomes the legacy infrastructure over the next 10-25 years. To meet the increasing demand of superior and more environment-friendly technology than the existing, silicon photonics presents a viable solution for re-architecture of datacenters by enabling more efficient switches, transceivers, various (de)multiplexing systems. Fig. 1.1(a) shows one of the Facebook datacenter networks, and Fig. 1.1(b) shows a schematic of a typical datacenter fabric topology containing various types of photonic interconnects. It shows the importance of compact and power-efficient photonic interconnects to build such massive infrastructures.

The advent of vertical cavity surface emitting lasers (VCSELs) enabled co-packaging optical source with photonic integrated circuits (PICs), which led to rapid incorporation of short-reach interconnects and multimode fiber for faster communication [6, 7]. In early times, the surface roughness of the waveguides in PICs used to cause high waveguide loss (> 1 dB/cm) [8] which was the major impediment in designing efficient photonic circuit blocks. The improvement of the fabrication quality over the time and the advent of new processes, such as photonic damascene process [9], reflow process [10], etc., made it possible to fabricate high quality photonic waveguides exhibiting significantly low losses (< 0.5 dB/m). Several material platforms are available for designing PICs, such as GaAs, InP, Si_3N_4, silicon-on-insulator (SOI), polymer, etc.

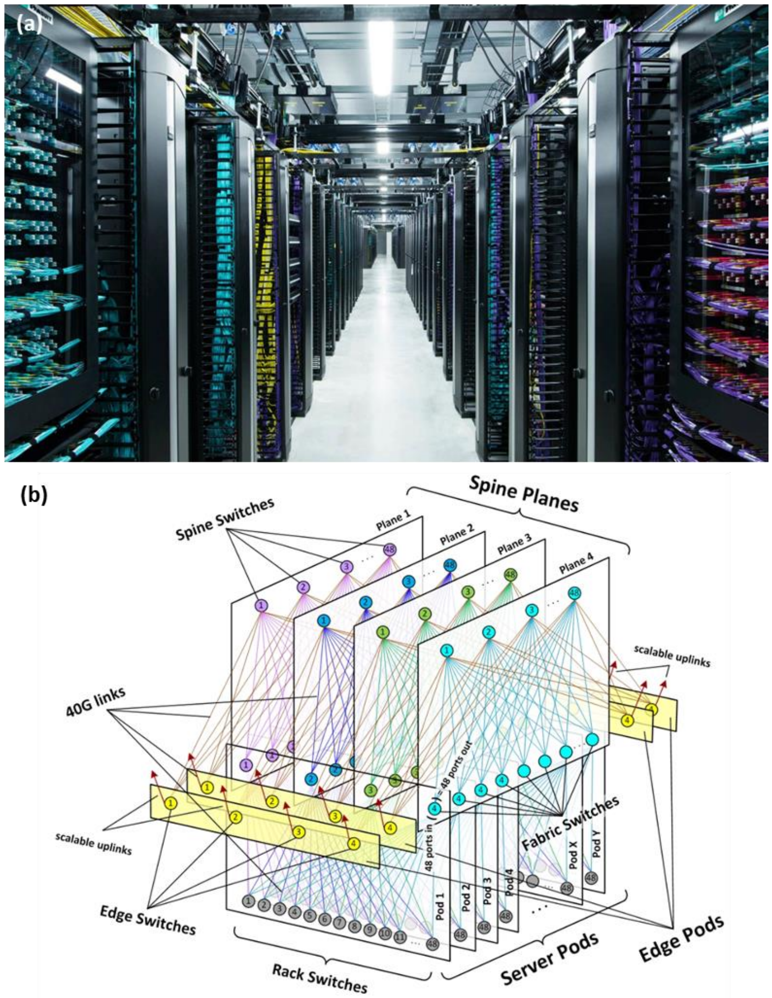


Fig. 1.1 (a) Facebook datacenter network, (b) schematic of Facebook datacenter fabric network topology; reproduced from [5].

Among these materials, SOI is the most intensively studied platform because of its compatibility with monolithic integration with already matured complementary metal oxide semiconductor (CMOS) technology, suitable for low-cost commercial manufacturing and power efficient applications. The original band or O-band (1.26-1.36 μm) is incorporated in datacenters for short-reach data transmission within the range of 100 m to 2 km [11] because of the minimum dispersion in the operating bandwidth, while for long-haul data transmission, signal power attenuation is more significant concern and C-band (1.53-1.565 μm) is deployed. Ciena's 100G-400G transceivers [12], Intel's 400 GHz CWDM transmitter [13], 400 Gbps Ethernet traffic, 800 Gbps products sampling [14], etc. are some of the state-of-the art commercial products realized by silicon photonics.

1.2 Utilizing orthogonal optical modes

Depending on the dimensions and the refractive index contrast between the waveguide core and the cladding, optical waveguides can support multiple modes with electromagnetic field distribution being orthogonal among themselves. This has enabled space-division multiplexing of optical signal, also known as mode-division multiplexing. To overcome the capacity limitation of the single-mode fiber infrastructure, data transmission utilizing mode division multiplexing in the few-mode fiber has been extensively studied [15]. With a mature technology, few-mode optical fibers have recently been commercially available to accommodate several signals at the same wavelength in the fiber with one single core [16]. In upcoming years, it is expected to be adopted in large scale in datacenters and long-haul transmission systems. Compared to optical fibers, chip-level solutions for PICs are relatively young and are going through essential developments. Until recently, in PICs sidewall roughness of the waveguides due to the fabrication imperfections posed a limitation on utilizing different modes for carrying different channel information, since scattering caused by the roughness would contribute to high modal crosstalk. Therefore, unlike multimode fibers, on-chip MDM for multimode operations is still in the engineering phase and will take some time to be commercialized. Recent improvements in electron beam lithography, photolithography, and plasma etching process made way for using different waveguide modes separately for carrying optical signals, leading to an increase of data transmission and processing capacity by several folds [17]. A single multimode waveguide is used to carry information from multiple channels embedded in multiple guided modes, resulting in reduced chip space. This is simultaneously energy and cost-effective approach as one monochromatic laser source can be used for several data channels [4, 17]. Therefore, despite the challenge of modal crosstalk reduction and design complexity, multimode operations in integrated photonics have received much attention. Among the basic building blocks of multimode SiPh systems, like multimode reconfigurable optical switches, are the mode converters and the MDMs.

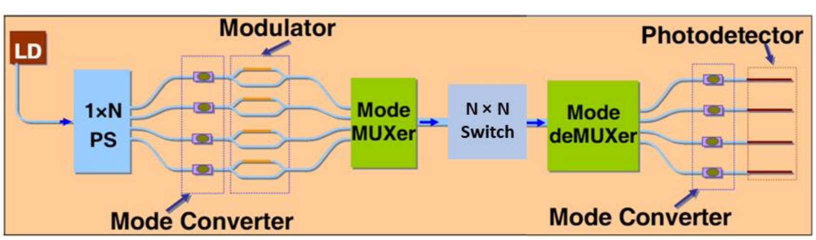


Fig. 1.2 Schematic of a SiPh MDM link (adopted from [17]). LD: laser diode, PS: power splitter, N: number of data channels.

Fig. 1.2 shows a schematic diagram of a typical SiPh MDM link for switching purpose, which consists of a continuous wave (CW) light source, power splitter, mode converters, optical modulators, MDMs, switch circuit and photodetectors.

The CW optical power is split into several channels using the power splitter. The optical power in each channel undergoes a mode conversion before being modulated by the corresponding message signal. The modulated signals are multiplexed into a multimode waveguide by the MDM and enters the switch followed by a mode demultiplexer (deMUX) to be routed to the desired receiver channels. Finally, at the receiving end, higher order modes are converted back to the fundamental mode, and optical signals are converted to electrical signals by the photodetectors. In this work, compact footprint mode converters and mode-division (de)multiplexers are designed.

1.3 Motivation

Although photonic systems are far more efficient than electronic counterparts in terms of data transmission rate, bandwidth, and thermal dissipation, they are far behind the electronic systems, which are usually composed of transistors, when it comes to device footprint. The main building blocks of an electronic system are usually different types of transistors which are usually less than 100 nm long. Moreover, electrical conductors can be very thin and bend at any angle without much affecting the signal and current propagation. Such flexible wiring allows an electronic system to be highly compact. However, photonic components and waveguides do not have such flexibility in size and bending angles. Unlike electrical current, optical signal must be confined inside the waveguide by means of total internal reflection, posing serious limitations on the waveguide dimensions and bending angles. Additionally, two adjacent electrical conductors can be isolated by a significantly thin layer of insulator, whereas depending on the material platform two waveguides need to be separated by more than 0.5 μm to ensure optical isolation, preventing evanescent coupling of the optical fields [17]. Because of such fundamental limitations, traditional optical interconnects encompass very large footprints, starting from a few microns (ring resonators), tens of microns (grating couplers, photodetectors, etc.) to several hundreds of microns (directional couplers, Mach Zehnder interferometer-based modulators, etc.). Thus, reducing the size of the standard optical devices has been a drive since the beginning of integrated photonics to enable dense integration of the PICs.

In this work, compact footprint (only a few microns long) mode converters for first four transverse electric (TE) modes, and three-channel mode-division (de)multiplexers have been designed and experimentally characterized. Two inverse design techniques, shape optimization and density topology optimization, are adopted to design these devices, since inverse design has emerged as a reliable means for designing compact devices by tuning a large number of design parameters. Despite limiting their length below 8 μm, no compromise was made with the operating bandwidth, insertion loss, transmission efficiency, and crosstalk, which are comparable with those of the conventional designs having large footprints (tens to hundreds of microns). Such reduction in the device sizes will facilitate denser integration of photonic components. The performance of the typical photonic interconnects is vulnerable to regular fabrication errors, such as sidewall roughness, nonuniform silicon layer thickness, under/over etch errors including waveguide width variations, smoothing of the sharp features/corners, to name a few. It is very common to have device performance degraded severely after fabrication, especially the crosstalk increases by several folds (6-10 dB) compared to the predicted crosstalk in simulation of the optimized designs. Thus, one objective of the design of MCs in this work is to achieve robustness to dimensional variations, under/over etch errors leading to waveguide width variations to be specific.

Next, inverse design techniques usually take a lot of computations in its iterative optimization process. Depending on the size of the design area, it even may take more than 24 hours for a typical four-core processor to complete one optimization and converge to a local optimum in the nonconvex design parameter space, which may eventually turn out to have unsatisfactory performance. Then, another optimization run needs to be initiated with different starting parameters values, and the process may go on until a good design is obtained. Sometimes, the objective function may contain more than one terms for optimizing multiple performance attributes simultaneously. In such cases, often finding the right weight coefficients leading to a good balance of the design objectives needs a lot of experimentations. Thus, much effort is invested in developing computationally efficient inverse design methods. Here, a machine learning-based regression model has been developed to reduce the computation cost involved with burdensome 3D optimization of MCs. This method is applicable for shape optimization of any linear photonic devices.

Finally, the working principles of the shape optimized MCs are investigated. In recent years, many inverse designed photonic devices have been reported. Such designs usually include very complex structures, which makes their working mechanisms very difficult to interpret for the humans. Consequently, the discussion on the working principles of the inverse designed devise are found in only a limited number of articles [19, 20]. In this work, the shape optimization leads to relatively less complicated design structures for the MCs. By studying the simulated electromagnetic field patterns in these MCs, their mode conversion mechanisms have been figured out and validated with supportive experimental data. Such interpretation of the device functionality has led to formulating the design problem such that more efficient designs are obtained later by changing some initial conditions, more favorable for the device functionality. On top of that, following the insights obtained in the investigation of the working mechanism, a two-step design approach has been proposed which is deployed to design some MCs, which would otherwise be difficult to design in the standard single-step approach.

1.4 Research contributions

The research works presented in this thesis are conducted by the candidate, Md Mahadi Masnad, under the supervision of Prof. Odile Liboiron-Ladouceur along with a collaboration with the National Research Council (NRC) Canada. These research projects are done under the AI4Design program of the Digital Technologies Research Center and the High-throughput Secure Networks program of Advanced Electronics and Photonics Research Center. The concepts are presented, and design optimization and experimental validations are performed by the candidate. The progresses of the work have been regularly reported to the program's principal investigator, Prof. Liboiron-Ladouceur, and the collaborators from NRC, Drs. Y. Grinberg and D.-X. Xu. Their feedback and technical support made it possible to materialize the design ideas and demonstrate the concepts. The contributions of this thesis are summarized below following the order of the contents presented here.

- Four types of mode converters are designed for various pairs of first four quasi-transverse electric (TE) modes using computationally efficient shape optimization method. The designs are fabricated and experimentally characterized. The device lengths vary from 3 μm to 7.8 μm. Despite the compact sizes, the MCs show good tolerance (the mode conversion efficiency remains above 90% at 1.55 μm operating wavelength) to ±10 nm etch errors, corresponding to ±20 nm waveguide width variations. A detailed discussion on the mode conversion mechanisms is presented. This interpretation of the working principle leads to the formulation of the design problems for more efficient designs and computation cost-effective design approaches. For time-domain characterization, on-off keying (OOK) and four-level pulse amplitude modulation (PAM-4) payload transmissions experiment are performed, which shows their utility in high-speed data transmission. PhD student Guowu Zhang helped with the experimental setup and collection of the measurement data. The simulation results are presented at two conferences in 2021: the IEEE International Photonics Conference (IPC) and the OSA Photonics in Switching and Computing (PSC). The design of a TE1-TE3 MC and its performance have been presented at the Optical Fiber Conference (OFC) 2022. A detailed report including the experimental results is published in the peer-reviewed journal, Optics Express in 2022 (volume 30, issue 14).

Related publications

1. **Md Mahadi Masnad**, Yuri Grinberg, Dan-Xia Xu, and Odile Liboiron-Ladouceur, **"**Physics-guided Inverse Design for SiPh Mode Manipulation**,"** *Photonics in Switching and Computing*, 2021.
2. **Md Mahadi Masnad**, Dan-Xia Xu, Yuri Grinberg, and Odile Liboiron-Ladouceur, "Computationally efficient and fabrication error tolerant inverse designed mode converters," *IEEE Photonics Conference,* 2021.
3. **Md Mahadi Masnad**, Guowu Zhang, Dan-Xia Xu, Yuri Grinberg, and Odile Liboiron-Ladouceur, "Dimensional variation tolerant inverse designed broadband mode converter," *Optical Fiber Communication Conference*, 2022.
4. **Md Mahadi Masnad**, Guowu Zhang, Dan-Xia Xu, Yuri Grinberg, Odile Liboiron-Ladouceur, "Fabrication error tolerant broadband mode converters and their working principles," *Optics Express,* vol. 30, No. 14, pp. 25817-25829 (2022).

- Shape optimization is a gradient descent-based inverse design method. Finding the local optima in the highly nonconvex design parameter space requires intensive computation loads. The computation cost increases exponentially with the design region dimensions. Thus, novel approaches need to be implemented to reduce the time and computations needed for the design optimization. A machine learning-based regression model is proposed, which has been demonstrated to reduce the computation load involved with 3D optimization of the TE0-TE1 MC. This method is applicable for any photonic component design using the shape optimization method. An undergraduate student, Nishat Salsabil, from Bangladesh University of Engineering and Technology helped building the dataset for this project by performing the simulations required for the design optimization, while NRC researcher Dr. Yuri Grinberg guided the project steps. A manuscript is now under preparation for publication in a peer-reviewed journal.

- Compact footprint three-channel MDMs are designed using topology optimization and experimentally characterized. The design approach is scalable to include additional channels and higher order modes. This project has been combined with another project conducted by a post doctoral fellow, Dusan Gostimirovic, who has developed a deep neural network (DNN) model to predict the design structures after fabrication. Since topology optimized designs usually contain very complex structures having sharp bends and small features, many of them are difficult to fabricate properly. The DNN model can predict the structure after fabrication, which can be used to predict the fabricated device performance beforehand. Bad designs can be discarded, saving the time for experimental measurements involved with identifying the bad designs. To demonstrate the practical application of the prediction model, the topology optimized three-channel MDMs are adopted for the implementation of the prediction algorithm. A summary of this work is going to be presented at the European Conference on Optical Communication (ECOC) and the IEEE Photonics Conference 2022 (IPC). Experimental characterization of several MDM building blocks is going on, which will eventually be published in a peer-reviewed journal.

Related publications

1. Dusan Gostimirovic, **Md Mahadi Masnad**, Dan-Xia Xu, Yuri Grinberg, and Odile Liboiron-Ladouceur, "Pre-Fabrication Performance Verification of a Topologically Optimized Mode Demultiplexer Using Deep Neural Networks." to be presented at *European Conference on Optical Communication (ECOC)*, 2022.
2. **Md Mahadi Masnad**, Dusan Gostimirovic, Dan-Xia Xu, Yuri Grinberg, and Odile Liboiron-Ladouceur, "Feature Correction of a Topologically Optimized Mode Demultiplexer using Deep Neural Networks," to be presented at *IEEE Photonics Conference (IPC)*, 2022.

1.5 Thesis organization

In this thesis, three projects have been conducted—designing broadband mode converters robust to dimensional variations using shape optimization method, developing a machine learning-based design approach which incurs less computation cost, and designing three-channel mode-division (de)multiplexers using topology optimization. Design and optimization are performed in Ansys Lumerical finite-difference time-domain (FDTD) and variational FDTD or varFDTD suites [21]. Optimized designs are transferred to the gds file in KLayout [22], an open-source package for optical interconnects design layout. The design layouts are sent for fabrication at Applied Nano Tools Inc. [23] and fabricated using electron-beam lithography. The fabricated chips are measured and characterized in the laboratory facility at McGill University.

In chapter 1, a brief introduction to SiPh interconnects and their prospects in information technology, along with some associated challenges and shortcomings, have been presented. Then the motivation behind this thesis has been discussed, where three concerns are addressed—compact design footprint, device robustness to fabrication imperfections, and reduction of the computation cost. The research contributions of the candidate, Md Mahadi Masnad, are mentioned.

In chapter 2, a theoretical background of the optical modes in the waveguide is presented. A brief literature review on MCs and MDMs is provided. The shortcomings of the conventional designs, and how to avoid those in inverse design are discussed. The current status of the MC and MDM technologies and their applications are surveyed.

In chapter 3, a detailed report on the mode converter design steps and shape optimization approach is provided. In the results and performance analysis section, the simulation results of the optimized designs and the experimental results of the fabricated MCs are presented. Their performance, such as mode conversion efficiency, insertion loss, and crosstalk, variations due to the waveguide width variations caused by under/over etches are analyzed and compared with previously reported works. The mode conversion mechanisms studying the simulated electromagnetic field patterns are presented. Finally, a two-step design approach is proposed.

In chapter 4, a machine learning-based regression model assisted shape optimization method has been proposed which can significantly reduce the computation cost involved with 3D optimization of SiPh interconnects. The quasi-TE0 to quasi-TE1 mode converter is selected to demonstrate the idea, and 35% computation cost reduction has been achieved. This method is applicable for designing any other photonic device which can be optimized in the shape optimization technique.

In chapter 5, the design approach for three-channel MDMs in topology optimization method is presented. The simulation results of the optimized MDMs, along with the experimental results of the fabricated devices, are presented.

In chapter 6, a conclusion of the thesis is presented. The chapters are summarized highlighting the key findings. The scope of the future endeavors and issues to be addressed are also discussed briefly.

Chapter 2

Background

2.1 Guided modes in the rectangular waveguide

The relationship between the electric field $\bar{E}$ and the magnetic field $\bar{H}$ of an electromagnetic wave can be expressed by the following Maxwell's equations.

$$\nabla \times \bar{E} = -\mu \frac{\partial \bar{H}}{\partial t} \tag{1}$$

$$\nabla \times \bar{H} = \epsilon \frac{\partial \bar{E}}{\partial t} \tag{2}$$

Where ϵ and μ are the material permittivity and permeability, respectively. The wave equation is as follows.

$$\nabla^2 \bar{E} - \epsilon\mu \frac{\partial^2 \bar{E}}{\partial t^2} = 0 \tag{3}$$

For the wave propagating along the z-axis, the general solution of Eqn. 3 is

$$\bar{E} = \bar{E}(x, y) e^{j(\omega t - \beta z)} \tag{4}$$

where ω is the angular frequency, and β is the propagation constant. For the TE mode propagating along the z-axis inside a planner slab waveguide with thickness of d, like shown in Fig. 2.1, Eqn. 3 reduces to

$$E_x = E_z = 0, \qquad \frac{d^2E_y}{dx^2} - (k_0^2 n1^2 - \beta^2)E_y = 0 \tag{5}$$

where $k_0 = \frac{\omega}{c_0} = \frac{2\pi}{\lambda}$ is the free space wavenumber. For some discrete values of β, corresponding to different order guided TE modes, this equation is satisfied.

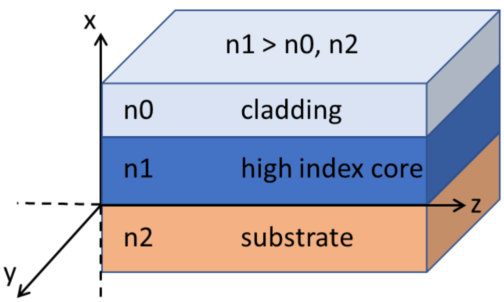


Fig. 2.1 A schematic of a planner slab waveguide with refractive index of n1, flanked by a substrate and a cladding with refractive indices of n2 and n0, respectively. The slab waveguide is confined along the x-axis while continuous along the other two directions.

For the guided modes, the propagation constant must remain within the limit $k_0 n1 \leq \beta \leq k_0 n2$, assuming that $n2 \geq n0$. After applying all the boundary conditions, an eigenvalue equation is obtained which is known as the TE mode dispersion relation.

$$\tan(kd - \mathrm{m}\pi) = \frac{k\mathrm{d}(\delta d + \gamma d)}{k^2 d^2 - \delta\gamma d} \tag{6}$$

where $\delta^2 = \beta^2 - k_0^2 n0^2$, $k^2 = k_0^2 n1^2 - \beta^2$, $\gamma^2 = \beta^2 - k_0^2 n2^2$. Here, m is an integer representing the mode order number. In a one-dimensional rectangular waveguide, the guided modes cannot be purely transverse electric (TE) or transverse magnetic (TM); these modes are called quasi-TE and quasi-TM, respectively. Because of the dimensional confinement in two directions and change of medium at the interface, spatial partial derivatives of the magnetic field are nonzero, resulting in small electric field component along the x- and z-directions in quasi-TE modes, and vice versa in quasi-TM modes. The optical interconnects in this work are designed for quasi-TE modes in the rectangular waveguides.

In Fig. 2.2 the electric field amplitude distribution along with electric field y-component (E_y) distributions are presented for the first four quasi-TE modes in a 220 nm thick and 1.75 µm wide rectangular silicon waveguide with silicon dioxide cladding.

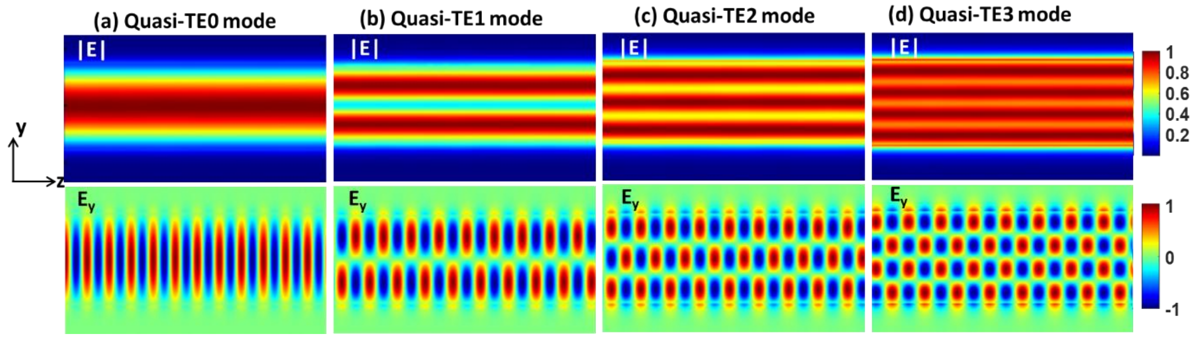


Fig. 2.2. Electric field distributions for first four quasi-TE modes in a 1.75 μm wide and 0.22 μm thick silicon waveguide with silicon dioxide cladding. |E| field distributions (top row) and E_y field distributions (bottom row) for (a) quasi-TE0 mode, (b) quasi-TE1 mode, (c) quasi-TE2 mode, (d) quasi-TE3 mode.

2.2 Silicon photonic mode converters

Since the fundamental mode is usually coupled most efficiently to the waveguide from the fiber than higher order modes, on-chip mode conversion of the fundamental mode to higher order modes requires mode converters (MCs) [24, 25]. MCs also have important applications in coupling between various types of waveguides [26] as different waveguides are suitable for different functionalities, such as photonic crystal waveguides for slow light applications [25, 27] and metal-insulator waveguides for surface plasmon resonance [28, 29], to name a few. Several methods have been demonstrated to convert the optical modes in the PIC waveguides, such as phase matching [17, 30-37], beam shaping [38-41], and coherent scattering [42-44]. Phase matching can be performed in various means. Utilizing the evanescent coupling between two adjacent waveguides, asymmetric directional coupler has been a popular choice for mode conversion and MDM applications [30-33]. The effective index of a guided mode increases with the cross-sectional area of the waveguide. When two adjacent waveguides having different dimensions carry optical signals and if the propagation constant of the lower order mode in the narrower waveguide matches with the propagation constant of a higher order mode in the wider waveguide, it can excite the higher order mode in the wider waveguide, and vice versa. If the coupling length is designed properly, the entire optical signal from one waveguide can transfer to the adjacent one into a different guided mode. Similar mode conversion has also been demonstrated using grating structures between two waveguides [34]. Grating-assisted MCs are also reported which do not use the evanescent coupling, rather introduce some imbalance on the wavefront to match the phase of the target mode [35, 36]. MCs designed using asymmetric directional coupler, Y junctions, and Bragg grating usually have large footprints, from tens to several hundreds of microns. Beam shaping method for mode conversion either splits the beam and recombines them with desired phase conditions [37, 38], or makes different portions of the wavefront travel different optical paths for the optical field rearrangement before reaching the output [20, 40]. These MCs still are tens of microns long.

MCs designed using micro-ring resonators encompass small footprint but suffer from narrow bandwidth [37]. For high performance and compact designs, various inverse design methods demonstrate significant advantages over the traditional approaches by tuning a large number of design parameters [42-48], and usually utilizes coherent scattering or beam shaping for mode conversion. Consequently, computational inverse design of nanophotonic devices received much attention recently in improving the performance of various photonic integrated circuits [49-53]. Mode converters designed using topology optimization, a versatile inverse design method, are compact and have high conversion efficiencies [26, 46]. But the disadvantages are possible tiny features in the design area and an additional computation cost for boundary optimization carried out in the binarization step [54]. Moreover, discrete features, typical of topological inverse design methodology, make the device performance sensitive to common fabrication errors such as under and over etches, that result from shorter and longer time exposures, respectively, of the die to the etching chemicals. Longer exposure causes unwanted lateral etching under the photoresist, resulting in narrower waveguides while shorter exposure does the opposite. To mitigate these issues, a novel method called topology optimization with energy constraint has been proposed by our group [49]. It results in devices comparatively more tolerant to fabrication errors by limiting the optical field overlap within the design structure sidewalls. For simple functionalities such as mode conversion, power splitting, etc., this approach remains computationally demanding. Another method known as direct binary search, in which the minimum pixel dimension is kept larger than the allowed minimum feature size, is often used to design photonic devices to perform various mode manipulation operations in silicon photonics [50, 51]. But design optimization in this method incurs a significant computation cost as well. Also experimentally, these devices suffer from lower transmission (in the order of -1 dB to -2.2 dB) and higher crosstalk (as high as -8.5 dB). Mode converters are also designed implementing inverse design methods on photonic crystal waveguides. However, such MCs often have either lower conversion efficiency and higher crosstalk [45] or narrower bandwidth [43].

2.3 Silicon Photonic mode-division (de)multiplexers

Compared to WDM and PDM, MDM is relatively new multiplexing system and being investigated intensively lately. In 1996, on-chip MDM is first proposed by Luthold *et al.* [55, 56]. Multi-mode interference (MMI) coupler derived from converter-combiner MMIs was used to separate anti-symmetric mode from symmetric mode. This MMI and passive phase shifters were used to demonstrate mode multiplexing of the first two TE modes. Later, different version of the MMI-based MDM systems emerged with improved bandwidth, reduced footprints, and flexibility in power splitting ratio [57, 58]. MDMs are also designed using single and cascaded asymmetric Y-junctions [59, 60]. These MDMs show very good performance in terms of low insertion loss (~1.5 dB) and low crosstalk (-30 dB), but the device lengths are as long as 1.2 mm, which is not suitable for dense integration.

Often various combinations of two different photonics components result in significant improvement in a target performance attribute. For instance, MCs and MDMs realized by combining the Y-junction with MMI couplers show low-loss mode conversion and multiplexing in compact footprint [61]. Typically, the Y-junction is wavelength sensitive, Y-junction-based MDMs suffer from low bandwidth. But adopting asymmetric adiabatic couplers with Y-junction led to broadband MDMs [62, 63]. However, most of the MDMs reported above are not reconfigurable, *i.e.*, each input fundamental mode is converted to one specific high-order mode. It limits the application of the MDMs in the increasingly complex multiplexing networks. The drive for designing reconfigurable MDMs for more flexible applications made way for newer versions, such as mode-selective switches and add-drop multiplexers. Such devices are demonstrated using microring resonators, MZIs, and micro-electromechanical systems [64-66]. Mode conversion was demonstrated using three-waveguide coupling [67], which is adopted for scalable and reconfigurable mode (de)multiplexing functionality [68].

MDMs having lengths below 10 μm have been demonstrated implementing several inverse design techniques. By adopting subwavelength structures in a wide divergence angle asymmetric Y-junction, two- and three-channel MDMs have been reported with design footprints of 2.4×3 μm^2

and 3.6×4.8 μm^2, respectively [69]. Despite such compact sizes, the ILs are below 1 dB and modal crosstalks are below -24 dB over an operating bandwidth of 1.53-1.59 μm. Among various inverse design techniques, density topology optimization is one of the most versatile design methods and is utilized to achieve a wide range of functionalities. Recently, a simulated 12-channel MDM design, routing the first 12-order TE modes to 12 output channels, has been reported having a footprint of 18×18 μm^2 only [70]. However, it is typical of topology optimized designs to have complex geometries with isolated structures and tiny features. Often, it is usually difficult to fabricate the resulting optimized designs at commercial foundries because of the limitations on minimum feature size and maximum curvature. If the optimized design is not identically fabricated, its performance is adversely affected, especially the channel crosstalk which increases by several folds. Therefore, special measures need to be adopted in design steps to make the devices suitable for mass manufacturing in the commercial silicon photonic process. In the design optimization algorithm, restrictions are imposed on the minimum feature size as well as the maximum curvature of the structure contours to obtain designs that are readily fabricable. Lately, Piggott *et al.* reported four types of SiPh devices, including a two-channel MDM, which are suitable for commercial foundries [71]. It is also worth investigating the effect of the isolated structures in the design region on the device performance. Often, very little optical field couples to some regions in the design area, and the device performance is not strongly dependent on such discrete or isolated structures. Frellsen *et al.* presented such an investigation on a topology optimized two-channel MDM [72]. The apparently inactive region, named as “appendix”, was removed and simulation results showed slight degradation in crosstalk and transmission of the device.

2.4 Summary

In this chapter, a brief introduction of the optical modes in the slab waveguide is presented. The electromagnetic field patterns of different orders of the modes show that the optical modes are orthogonal in their field distributions and, therefore, do not interfere with each other ideally. Thus, the modes can be utilized to carry data information from different channels through the same physical path (waveguide), giving rise to the concept of mode-division multiplexing. The mode converter is one of the basic elements of mode-based multiplexing and switching systems. Different strategies of on-chip mode conversion and various approaches for designing MCs are discussed along with their respective advantages and disadvantages in terms of performance, device footprint, and design complexity.

A brief survey on MDM design methods and the evolution of compact footprint MDMs are presented. The large design footprints of the photonic components designed in traditional approaches limit achieving dense integration of photonic interconnects. Computational design techniques have led to significant progress in reducing the device size as well as diversifying application-specific component designs. But such design techniques often require significant computation load and time. Moreover, small footprint designs tend to be sensitive to fabrication process variations. In this thesis, these issues are addressed in the design of MC and MDM design blocks

Chapter 3

Mode converters

In this chapter, we report compact broadband mode converters designed using a shape optimization method. A small set of structure boundary points are parameterized, and a gradient-based algorithm changes the shape of the material block in the design area to maximize a defined figure of merit (FOM). This approach does not require any binarization step since the structure is binarized right from the beginning. On the SOI platform, a binary design refers to the design which consists of silicon structures with silicon dioxide cladding, *i.e.*, any given point in the design area has material permittivity of either silicon or silicon dioxide. Consisting of a single silicon block, the optimized designs are readily manufacturable and robust to dimensional variations such as 10 nm under/over etch, which corresponds to ±20 nm waveguide width variation. To demonstrate the scalability, MCs were designed for mutual conversion of different combinations of mode pairs among the first four quasi-transverse electrical (TE) modes (*e.g.*, fundamental TE mode, TE0, to 3rd order mode, TE3). The simulation and experimental results of two MCs, *i.e.*, TE0↔TE1 and TE1↔TE3, are highlighted here. The measured insertion losses (IL) are below 1 dB over a wavelength span of 80 nm ranging from 1.5 μm to 1.58 μm, and the modal crosstalks (XT) are below -19 dB in the C-band (1.53 μm to 1.565 μm). We present the mode conversion mechanism of these MCs by studying the simulated electromagnetic field patterns and validate with supportive data. Payload transmissions (28 Gbps On-Off-Keying, OOK, and 20 GBaud 4-level pulse amplitude modulation, PAM-4) have been carried out for time domain characterization, and open eye diagrams are obtained.

3.1 Design approach

The mode converters are designed for their implementation on a commercial silicon-on-insulator (SOI) platform with a silicon layer thickness of 220 nm and a 2 μm thick buried oxide layer. The top cladding consists of 2.2 μm deposited silicon dioxide (SiO_2). Thus, any point in the design area assumes either of the two material permittivities, $\boldsymbol{\epsilon_{Si}} = 12.11$ and $\boldsymbol{\epsilon_{SiO_2}} = 2.085$ [73]. As a common practice in shape optimization, a device geometry from either an initial guess or a random initialization is needed as the starting structure to begin the optimization. Deciding the dimensions and the aspect ratio of the design area is one of the most important contributing factors to the final device performance. While the widths of the input and output (I/O) waveguides depend mostly on the application and the device interface with the rest of the circuit, their positions and spacing directly determine the local and global optima in the design parameter space. Particularly in this work, the mode conversion requires relative phase shifts on the traveling wavefront, which in turn requires a sufficiently long optical path to traverse the design area. For a TE0-TE1 MC, for instance, reducing the device length shorter than 3 μm results in lower conversion efficiency (CE) between the two modes (at a length of 2.5 μm, CE is approximately 92%) as well as XT worse than -18 dB. Increasing the device length beyond 3.5 μm does not significantly improve the CE, while the XT performance improves by a few decibels. Below is a table summarizing average mode conversion efficiencies and worst crosstalk of TE0-TE1 MCs having different lengths in simulation.

Table 3.1. Effect of the device length on its performance

Length	Bandwidth, Center wavelength 1.55 μm	Average CE across the bandwidth	Maximum XT across the bandwidth
2.5 μm	100 nm	92.1%	-14.6 dB
2.8 μm	100 nm	95.1%	-17.7 dB
3.0 μm	100 nm	96.6%	-19.0 dB
3.2 μm	100 nm	97.3%	-18.6 dB
3.4 μm	100 nm	97.6%	-19.9 dB
3.6 μm	100 nm	97.7%	-20.7 dB
4.0 μm	100 nm	97.8%	-21.8 dB

Without designer intervention or manual tuning, inverse design techniques can generally find local optima in the design parameter space with respectable performance [46]. However, utilizing physical intuition in deciding the starting geometry space for the optimization lead to computational cost reduction and devices with better performance [74].

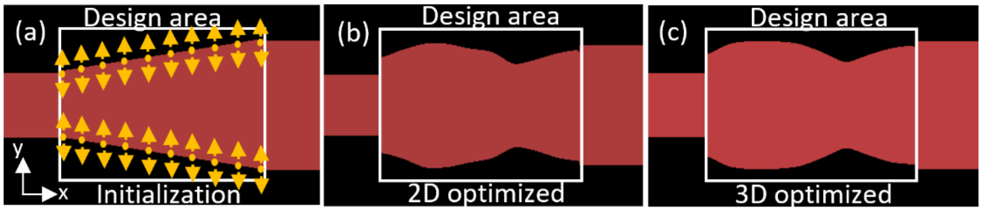


Fig. 3.1 (a) Initialization of the optimization in 2D simulation, the boundary points on the sidewalls are parameterized, (b) 2D optimized design, which is the starting point for initiating optimization in 3D simulation, (c) 3D optimized design, ready for fabrication.

As shown in Fig. 3.1 (a), 20 points on the structure boundary are taken as the design parameters. The limited-memory Broyden-Fletcher-Goldfarb-Shano bound-constrained (L-BFGS-B) [75], a quasi-Newton algorithm, is employed to optimize a figure of merit (FOM). The design parameters, *i.e.*, the vertical positions of the boundary points, are updated according to the gradient information from the current iteration and the estimated second-order derivative information of the FOM from the previous iterations. A line search, performed in each iteration, determines the step length. The optimization terminates when the gradient amplitude is smaller than 10^{-5}. In every iteration, a forward and an adjoint simulations are performed to evaluate the field profile and calculate the gradient of the FOM with respect to the permittivity at every pixel in the design area. This gradient is multiplied to the partial derivatives of the permittivity with respect to the design parameters to calculate the gradient of the FOM with respect to the design parameters. The FOM is defined as the average mode conversion efficiency at 11 equally spaced wavelength points across the bandwidth from the input mode to the desired output mode for broadband performance. The conversion efficiency (CE) is defined here as the ratio of the power transmitted into the specified mode in the output waveguide ($P_{out,T}$) and the power in the input mode ($P_{in,S}$).

$$CE = P_{out,T}/P_{in,S} \tag{1}$$

$$FOM = \frac{1}{n}\sum_{i=-(n-1)/2}^{(n-1)/2} CE\left(\lambda_0 + i\frac{\Delta\lambda}{n-1}\right), \tag{2}$$

where $n = 11$, $\lambda_0 = 1.5$ µm, and $\Delta\lambda = 100$ nm. Here the modal crosstalk is defined as the optical power coupling to any other guided mode except for the target mode. To quantify the XT, the ratio of the optical power in the undesired mode ($P_{out,U}$) and the total input power is calculated in dB unit.

$$XT = 10log_{10}(P_{out,U}/P_{in,S}) \quad (3)$$

As the algorithm maximizes the mode conversion efficiency, the optical energy left for contributing to the crosstalk is inherently minimized. Moreover, adding a new penalty term to the objective function comes at the cost of some amount of trial-and-error to find the right magnitude for the penalty. Since maximizing the conversion efficiency alone results in low crosstalk MCs, the modal crosstalk was not adopted in the FOM in this work to keep the optimization process simple. The designs are optimized through 2D simulations first. If the FOM exceeds 90%, the 2D optimized design is used as the starting structure for the 3D optimization. This is a time efficient approach since a computer with a processor having four cores (Core™ i7-3770 CPU @ 3.40 GHz) takes around 24 minutes to perform one iteration in 3D optimization whereas 18 iterations in 2D can be executed in the same amount of time. Most MCs in this work converge to the final designs within 50 iterations through 2D simulations and then around 29 iterations on average in 3D optimization. In the 2D optimization, the effective index method is used where a refractive index of 2.85 is used for quasi-transverse electrical (quasi-TE) modes. The simulations are performed using Ansys Lumerical Mode and FDTD solvers [21], and the optimizations are done using an open-source package, LumOpt, along with the scipy package [76], an open-source Python library used for scientific and technical computing. The design approach is similar to the one reported by Lalau-Keraly *et. al.* in [19]. The code provided in the "Lumerical support" [77] is used as a template, which can be directly used to design symmetric devices with symmetric electromagnetic field distributions with respect to the propagation axis. The code is modified to move all the parameter points up and down independently to incorporate asymmetry in the design structure. Additionally, the "cubic"-type interpolation used in the template often results in self-intersecting polygon boundaries, which is a problem because the resulting structures are not realistic designs. In this work, this part is replaced with a Gaussian smoothing filter which is convolved with linearly interpolated boundary points defining the design structure. The mesh size for the simulations is set to 20 nm along all axes providing sufficiently fine resolution to obtain reliable results. All the optical modes in this work are quasi-TE modes in the waveguides confined in two dimensions, but for ease of discussion in the upcoming sections, the prefix “quasi” before TE modes is often dropped.

The same approach is applicable to design mode converters for TM polarization. To do so, the designer needs to “Calculate Modes” in the “FDTD Mode Source”-panel for the given waveguide dimension and permittivity values and carefully select the mode order corresponding to TM modes in the design algorithm. MCs for TM polarization have not been designed, but a 3 dB power splitter was designed for the TM polarization utilizing the shape-optimization method. No issue showed up in the optimization method, and TE mode structures are reported mainly since the long-term goal of the research group is to develop various building blocks for an MDM-based integrated system.

It is important to note that the conversion from the TE mode into TM mode cannot be achieved by a design structure having uniform thickness (*i.e.*, single vertical etch). Such rotation of the polarization requires asymmetry in the effective index along the vertical axis. Hence a shallow etch along with a full etch are needed for conversion between the two polarizations. In fact, TE to TM mode conversion has been demonstrated using multilevel shape optimization [78].

3.2 Result and performance analysis

3.2.1 TE0-TE1 mode converters

To convert the fundamental TE mode into TE1 mode with different I/O waveguide dimensions but aligned with respect to each other (*i.e.*, on the same horizontal axis), out of 97 initializations, 16 TE0-TE1 mode converters are obtained with conversion efficiencies above 95% at 1.55 μm in 3D FDTD simulation. The device lengths vary from 3 μm to 3.6 μm. Three designs were selected for fabrication. To characterize the mode converter under study, two mode-division (de)multiplexers (MDM) are inserted to interface with single mode input and output waveguides. The MDM is designed using asymmetric directional couplers (DC) [79] to excite TE1 mode from the TE0 mode and also to separate them (demultiplex). This MDM was further optimized and characterized by our research group [80]. The measurement error (or performance variation) of this mode multiplexer is approximately 0.5 dB according to our previous investigation [81]. Fig. 3.2 shows the schematic of the circuit block used for device characterization and how different optical modes are routed. In forward propagation, TE0 mode is sent through the multimode waveguide. The MC converts it to TE1 mode which propagates through the multimode waveguide on the right along with the unconverted optical power remaining in TE0 mode as the crosstalk. The directional coupler separates TE1 mode from the crosstalk utilizing evanescent coupling. The widths of the two arms of the DC are tuned such that effective index of TE1 mode in the wider waveguide matches with that of TE0 mode in the narrower waveguide. Thus, TE1 mode couples to TE0 mode in the single mode waveguide in the upper arm. Similarly, in the reverse propagation, input TE0 mode excites TE1 mode in the multimode waveguide. The MC converts it to TE0 mode and the unconverted optical power in TE1 mode is separated by the DC on the left. By increasing the width of the multimode waveguide, higher order TE modes are excited and also separated by the DCs, used for the characterization of TE1-TE3 MC reported in section 3.3.2.

Fig. 3.2 Schematic of the circuit block for device characterization, showing the forward (in green) and reverse (in red) propagation through the TE0-TE1 mode converter.

Fig. 3.3 (a) shows an optical microscope image of the circuit block for device characterization. Two grating couplers (GCs), numbered 1 and 6, connected by a 0.5 μm wide single-mode waveguide are used to align a 12-channel optical fiber array with the grating couplers connected to the MDM circuit. The MC is placed at the position marked by the blue rectangle. The scanning electron microscope (SEM) image of one MC and its footprint are shown in Fig. 3.3 (b). The mode conversion efficiencies for both directions, calculated in 3D FDTD simulations, are plotted in Fig. 3.3 (d). Simulation predicts mode conversion efficiencies in both directions above 95% across a wavelength span of 100 nm from 1.5 μm to 1.6 μm. The spatial electric field amplitude profile of the mode conversion is shown in the inset of Fig. 3.3 (d).

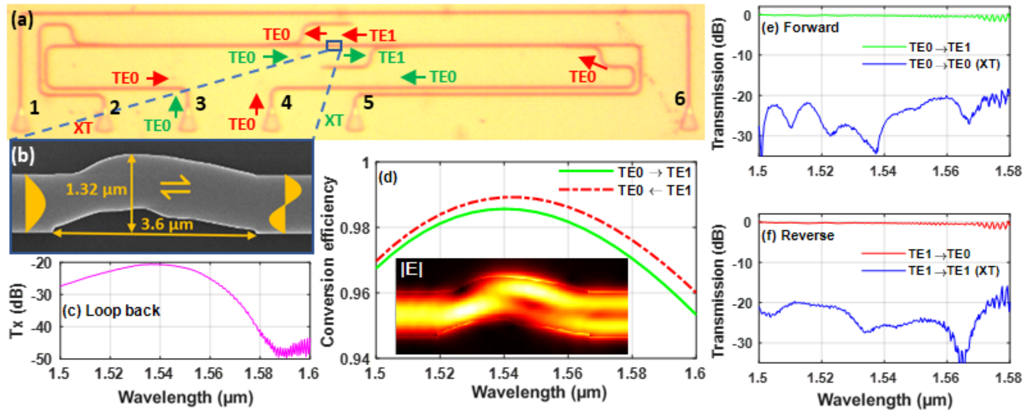


Fig. 3.3 (a) Optical circuit block used to measure the transmission and crosstalk of TE0-TE1 MCs, also showing the forward (green) and reverse (red) propagation with arrows, (b) SEM image of the TE0-TE1 mode converter, (c) transmission spectrum of the loop-back structure, showing undesired fluctuations at wavelengths longer than 1580 nm with 19.4 dB insertion loss at 1.54 μm, (d) mode conversion efficiencies, calculated in 3D FDTD simulations, for the forward propagation (TE0 → TE1) and the reverse propagation (TE1 → TE0); inset: spatial electric field amplitude profile, (e) transmission into desired TE1 mode and the modal crosstalk into TE0 mode, (f) transmission into desired TE0 mode and the modal crosstalk into TE1 mode for propagation in the reverse direction.

To measure the transmission spectra, a tunable laser and a optical power meter with sensitivity of -78 dBm at 1550 nm are used to collect transmission data at a wavelength interval of 0.2 nm between 1.5 μm and 1.6 μm. The laser output is 10 dBm and the combined insertion loss of the polarization controller and connectors is approximately 1 dB. All continuous wave (CW) measurements are normalized to the loopback structure. To account for any excess loss coming from the asymmetric directional coupler-based MDM, a circuit block like the one shown in Fig. 3.3 (a) is used but without any mode converter. The optical signal is sent through GC-2 and collected from GC-4 for the transmission, while optical modal crosstalk is measured through GC-5, which is below -30 dB across the wavelength range from 1.5 μm to 1.58 μm. Fig. 3.3 (c) shows a back-to-back GC insertion loss of 19.4 dB, implying the coupling loss of the grating coupler being 9.7 dB. The corresponding measurement error (or performance variation) for IL of the grating coupler at 1550 nm is approximately 1.2 dB according to the previous publication [82]. The fluctuations in the transmission spectrum, which come from the large back reflection of the GCs, makes the experimental data less reliable at longer wavelengths. Therefore, the experimental data beyond 1.58 μm is not reported, although the MCs are optimized to operate across the bandwidth of 1.5- 1.6 μm. The normalized transmission spectra in Fig. 3.3 (e) and (f) show an insertion loss of the mode converter below 0.5 dB and a modal crosstalk at most -18 dB for mode conversion in both directions across the wavelength range from 1.5 μm to 1.58 μm.

3.2.2 TE1-TE3 mode converters

The next set of MCs designed are for TE1-TE3 mode conversion. The input and the output waveguides are chosen to be 1 μm and 2 μm wide, respectively, placed along the same horizontal axis (*i.e.*, aligned horizontally). The spacing between them was varied from 3.2 μm to 4.2 μm to find an optimum length of the design area. With several random initializations, three final designs are obtained with conversion efficiencies above 97% at 1.55 μm and similar crosstalk performances. The SEM image and performance of one MC are reported in Fig. 3.4. The optical microscope image of a segment of the tapered directional coupler-based MDM array is shown in Fig. 3.4 (a), which separates (or demultiplexes) four TE modes into four channels for transmission and crosstalk measurement. The TE1-TE3 mode converter is placed at the left end of the cascaded MDMs. Using a tapered directional coupler, the TE1 mode is excited from the fundamental TE mode in the 1 μm wide waveguide on the left of the mode converter. The MC transforms the input mode into TE3 mode, while a small fraction of light couples to lower order modes as crosstalk. The width of the multimode- waveguide is changed at three successive directional couplers such that TE3, TE2, and TE1 modes are separated one by one by the DCs leaving behind TE0 mode as light travels forward. The design structure, shown in Fig. 3.4 (b), encompasses a footprint of 4×2 μm^2. The device boundary evolved to be symmetric with respect to the propagation axis, while the field profile is antisymmetric. Similar to the previous device, this MC is also bidirectional; if the TE1 mode is sent through the narrower waveguide, the device converts it to the TE3 mode which propagates in the wider waveguide, and vice versa. The mode conversion efficiency in both directions is above 95% across a 100 nm wavelength span between 1.5 μm and 1.6 μm. Fig. 3.4 (d) and (e) show the measured transmission spectra for the forward and reverse propagation. In both directions, the insertion losses are below 1 dB over the full reported bandwidth, and modal crosstalks below -20 dB in the C-band.

It is worth noticing that the final optimized design makes abrupt connections (unmatched waveguide widths) with the I/O waveguides. Following the gradient in the design parameter space, the algorithm changes the shape of the device to maximize the transmission into the specified mode in the output channel, impervious to making any smooth connections with the two ends of the I/O waveguides. Thus, in every type of the mode converters, we ended up having final designs with abrupt width mismatches at the junctions between the design and the I/O waveguides. The change in the device performance is studied by forcing the design to make smooth connections with the input and the output waveguides. Restrictions are imposed on the four corner points of the design, marked in red in Fig. 3.4 (f), to be held fixed with the two edges of the I/O waveguides, while the algorithm was allowed to move the remaining points on the boundary to maximize the FOM. Without any exception, the optimized smooth designs yield lower conversion efficiencies, represented by the black dashed curve in Fig. 3.4 (c). The transmission and crosstalk of the smooth TE1-TE3 mode converter are shown in Fig. 3.4 (g). Its lower mode conversion efficiency is responsible for increased modal crosstalk compared to the performance of the mode converter designed without such restriction.

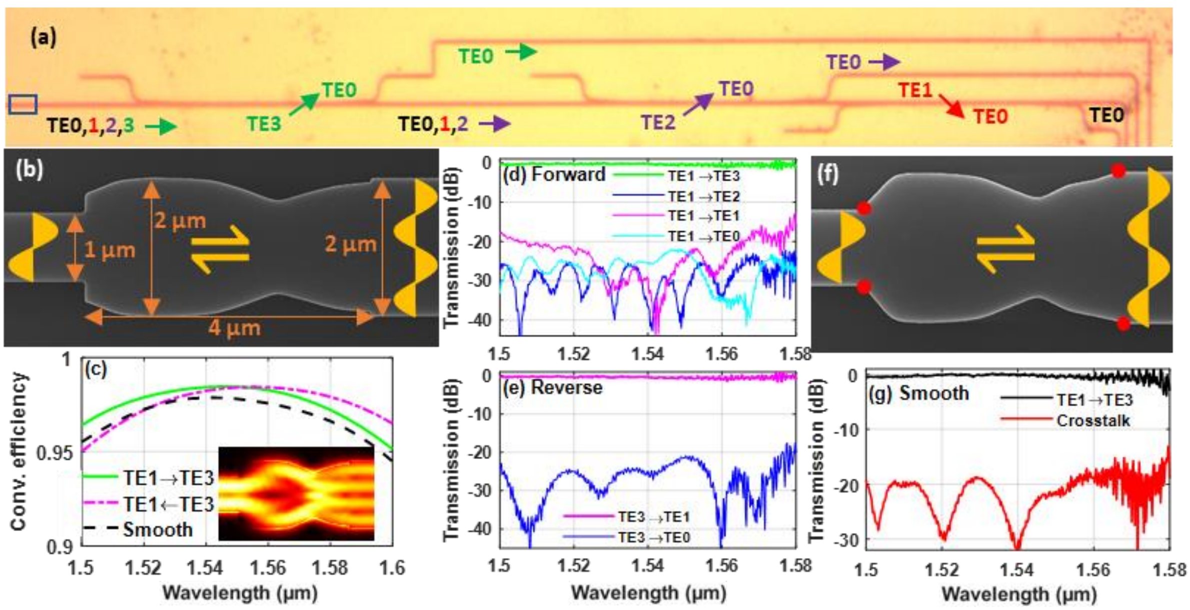


Fig. 3.4 (a) A segment of the tapered directional coupler-based MDM array to separate four TE modes and excite higher order modes from the fundamental TE mode, (b) the SEM image of a TE1-TE3 mode converter and its dimensions, (c) mode conversion efficiencies above 95% across the bandwidth, calculated using 3D FDTD simulation in both mode conversion directions; inset: spatial electric field amplitude profile, (d) transmission into desired TE3 mode and the modal crosstalk in lower order TE modes; crosstalk is below -20 dB in C-band, (e) transmission into desired TE1 mode and the modal crosstalk into TE0 mode for propagation in the reverse direction, (f) SEM image of the TE1-TE3 mode converter making smooth ends with the I/O waveguides, (g) transmission and crosstalk in the smooth design; lower mode conversion efficiency results in increased modal crosstalk.

3.2.3 Robustness to dimensional variations

To investigate the effects of dimensional variations in fabricated devices, each of the side walls of the mode converter layout (including the I/O waveguides) is intentionally extended (and shrunk) by 10 nm to mimic the effect of under (and over) etch. Along with the nominal designs, these variants with intentional extended and shrunk boundaries were also included for fabrication. Fig. 3.5 (a) illustrates the design layouts after introducing ±10 nm etch errors; +10 nm refers to extension of each sidewall by 10 nm, resulting in waveguide width expansion of 20 nm to emulate the under etch error, and -10 nm refers to the opposite. Fig. 3.5 (b) and (c) show how the CE is affected for extended and shrunk boundaries for TE0-TE1 and TE1-TE3 mode converters, respectively, in 3D FDTD simulations. At 1.55 μm wavelength for the TE0-TE1 mode converter, CE drops by approximately 2.2%, and the CE peaks shift in opposite directions. But for the TE1-TE3 converter, the conversion efficiency drops only by 0.6%. Similarly, its CE peaks move away from the central wavelength in opposite directions. The shifts of CE peak wavelength and efficiency drop for the same ±10 nm change for TE1-TE3 mode converter are smaller than those observed for TE0-TE1 mode converters. This can be explained by the relative size of the devices.

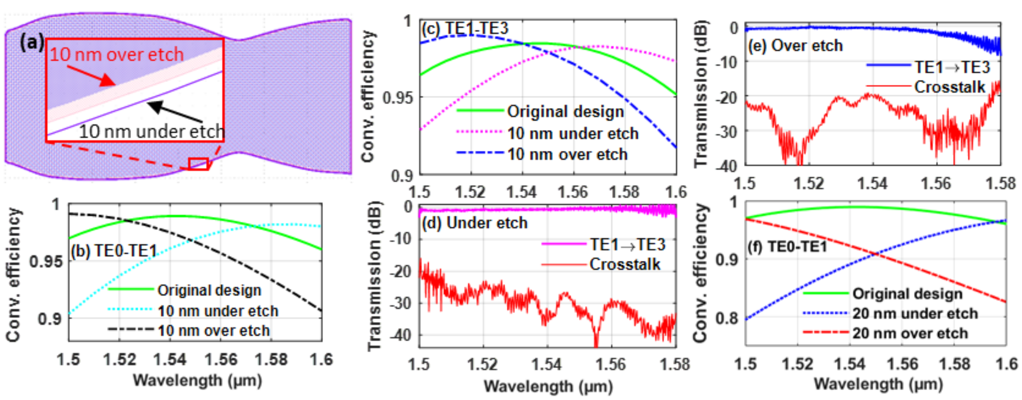


Fig. 3.5 (a) Layouts of the TE1-TE3 mode converter and its ±10 nm etch variants, overlayed on top of each other, (b) effects of 10 nm under and over etches on the conversion efficiency of TE0-TE1 mode converter in simulation, (c) effects of 10 nm under and over etches on the conversion efficiency of TE1-TE3 mode converter in simulation. Transmission and crosstalk spectra of (d)10 nm under etched and (e) 10 nm over etched TE1-TE3 mode converter, (f) effects of 20 nm under and over etches on the conversion efficiency of TE0-TE1 mode converter in simulation.

Compared to the TE0-TE1 mode converter, the TE1-TE3 mode converter has a larger footprint. The same amount of variation of the boundary of the TE0-TE1 MC leads to relatively higher changes; thus, larger shifts of CE peak. The experimental results confirm that under-etched MCs are more efficient at longer wavelengths while over-etched MCs at shorter wavelengths, which is predicted in simulation. The transmission and crosstalk spectra for 10 nm under and over etched TE1-TE3 mode converter are plotted in Fig. 3.5 (d) and (e). Apparently, under etched TE1-TE3 MC performs better at longer wavelengths, manifested by low insertion loss (0.1 dB at 1.56 μm) and lower crosstalk. On the other hand, over etched MC performs better at shorter wavelengths; transmission drops significantly at longer wavelengths. Across the C-band, all three variants of the MC have transmissions above -0.5 dB and crosstalk below -19.5 dB, indicating its robustness to ±10 nm etch errors. To compare with the mode conversion efficiencies of inverse-designed TE0-TE1 mode exchanger for ±20 nm etch errors reported in [50], additional simulations were run on the TE0-TE1 mode converter incorporating equal amount of under and over etches. The MC in our work shows approximately 10% higher mode conversion efficiency than that reported in [50]. The mode conversion efficiencies for ±20 nm etch errors are plotted in Fig. 3.5 (f). Despite 20 nm dimensional variations, the conversion efficiencies remain above 90% at 1.55 μm. Apart from these devices, TE0-TE2 (6.7 μm long) and TE1-TE2 (7.8 μm long) MCs have also been optimized [74] and experimentally characterized. Table 3.2 presents a summary of the key performance parameters of the four mode converters in this work along with the MCs reported by other research groups.

Table 3.2. Performance summary of the MCs in this work and previously reported MCs

Ref.	Mode conversion pair	Footprint (μm^2)	Average CE in simulati-on	Decrease in CE at 1.55 μm for ±20 nm width variations	Reported Bandwidth	Maximum IL across the reported bandwidth	Maximum XT measured across the bandwidth
[20,41]	TE0-TE1	18.6 × 2.65	98.6%	Not reported	100 nm	0.4 dB	-21.0 dB
[20,41]	TE2-TE0	19.3 × 4.68	98.8%	Not reported	100 nm	0.5 dB	-18.0 dB
[45]	TE0-TE1	6.3 × 3.6	82.0%	Not reported	43 nm	2.0 dB	-12.0 dB
[46]	TE0-TE1	2.4 × 1.6	86.4%	Not reported	Not reported	Not reported	Not reported
This work	TE0-TE1	3.6 × 1.32	97.7%	0.6%	80 nm	1.0 dB	-18.0 dB
This work	TE1-TE3	4 × 2	97.6%	2.2%	80 nm	0.8 dB	-17.0 dB
This work	TE2-TE0	6.7 × 2.4	95.1%	1.6%	80 nm	1.2 dB	-13.0 dB
This work	TE1-TE2	7.8 × 2.25	98.0%	1.3%	80 nm	0.8 dB	-18.2 dB

3.2.4 Data transmission experiment

To characterize the time domain performance of the mode converters, 28 Gbps on-off keying (OOK) and 20 GBaud 4-level pulse amplitude modulation (PAM-4) data transmission measurements were carried out. The experimental setup is shown in Fig. 3.6. Continuous-wave optical power at 1.54 μm from the tunable laser is injected into the $LiNbO_3$ modulator through a polarization controller. 28 Gbps OOK and 20 GBaud PAM-4 electrical signals from a programmable pattern generator (PPG) were used to modulate the optical signal. A pseudo-random bit sequence (PRBS) of 2^7-1 was used. The modulated optical signal is coupled in and out of the chip using a 12-channel single mode optical fiber array. The modulator output power is 0 dBm, and the polarization controller after that introduces an attenuation of approximately 0.7 dB. Because of the poor coupling efficiency to the grating coupler array, the input power to the EDFA with a noise figure below 5 dB (Thorlabs EDFA100S, single mode) is approximately -20 dBm. The EDFA is used to provide a gain of 18 dB. The tunable optical filter is used to suppress the out of band amplified spontaneous emission (ASE) noise of the EDFA. Then the optical signal is sent to a digital communication analyzer to observe the eye diagram.

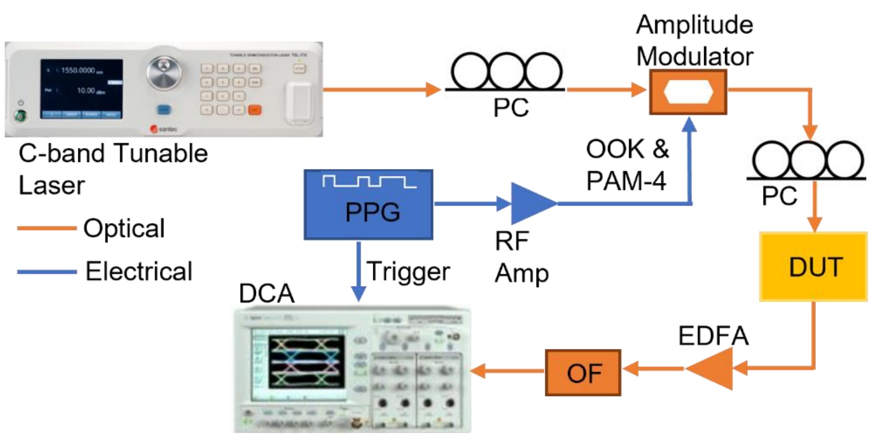


Fig. 3.6 Experimental setup for 28 Gbps on-off keying (OOK) and 20 Gbaud PAM-4 data transmission. PC: polarization controller, DC: bias voltage supply, PPG: programmable pattern generator, RF Amp: RF amplifier, DUT: device under test, EDFA: erbium-doped fiber amplifier, OF: optical filter, DCA: digital communication analyzer.

Fig. 3.7 (a) shows an open and clear eye diagram of the electrical signal directly coming from the PPG. The eye diagram of the modulator output for PAM-4 signal is open (Fig. 3.7 (b)); the degradation is mainly caused by the RF amplifier. Because of the high system insertion loss around

20 dB at 1.54 μm, the eye quality degrades as the modulated signal travels through the chip, the EDFA, and finally the optical filter.

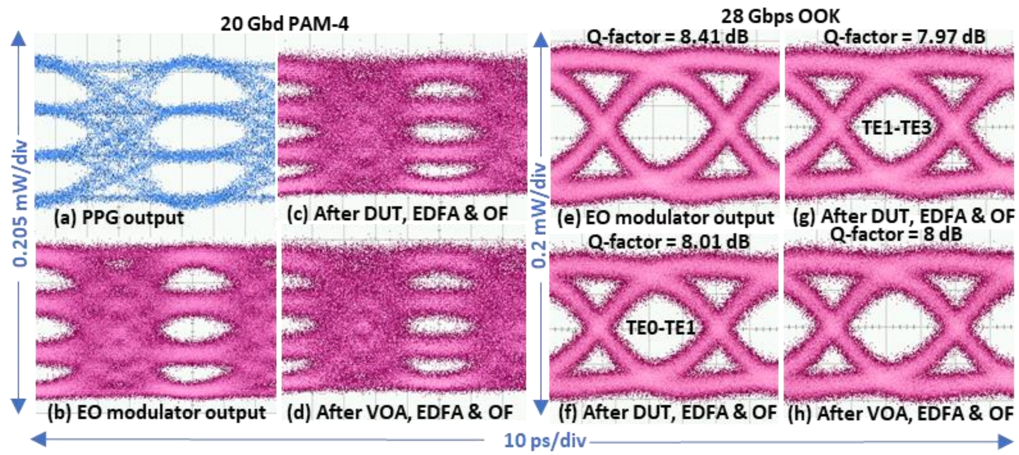


Fig. 3.7 (a) Eye diagrams of the 20 GBaud PAM-4 electrical signal coming from the programmable pattern generator; eye diagram of the optical signal (b) at the optical modulator output, (c) after going through the chip and being amplified 18 dB by the EDFA and filtered by an optical filter, (d) when the chip was replaced by a loss representing the die using a variable optical attenuator (VOA); eye diagrams for 28 Gbps OOK signal transmission (e) at the optical modulator output, (f) after going through the TE0-TE1 mode converter, EDFA, and optical filter, (h) when the chip was replaced by the VOA with a corresponding loss.

To identify the noise contributing source. Data transmission is performed afterwards replacing the chip with a variable optical attenuator (VOA) introducing 20 dB attenuation to mimic the insertion loss of the grating couplers. For OOK signal, the Q-factor of the modulator output signal is 8.41 dB, while for TE0-TE1 and TE1-TE3 MCs, we observe open eye diagrams with a Q-factor of 8.01 dB and 7.97 dB, respectively. Replacing the chip with the VOA also results in OOK transmission with a Q-factor of 8 dB, implying that the SNR degradation is due to the ASE noise of the EDFA.

3.3 Working mechanism

The working mechanisms of various inverse-designed nanophotonic devices were deemed nonintuitive/sophisticated in some published works [19, 46], while such discussion is absent in most of the reports on inverse design [45, 49-53]. The mode conversion mechanism is explained here by analyzing the simulated field patterns and validate our theory with supportive evidence found in the simulation and experimental data. For the fundamental TE mode with symmetric E_y field profile, the light rays on the wavefront have the same phase, with the peak field amplitude at the center of the lobe. On the other hand, TE1 mode has two antisymmetric lobes with a field null at the center; two peaks are shifted toward the opposite boundaries, having a phase difference of π. Therefore, to convert a TE0 mode into a TE1 mode, besides the spatial field amplitude rearrangement, the phase of half of the wavefront in the TE0 mode needs to be altered by π with respect to the remaining half wavefront. Additionally, the wavevector (k=2π/λ) projection along the propagation axis, in other words the propagation constant (β), needs to be matched with that of the TE1 mode in the output waveguide. The phase shift can be achieved by introducing a delay to one portion of the wavefront by making it travel a longer optical path. An asymmetric design geometry can introduce this optical path difference to different portions of the TE0 mode wavefront and transform it into two antisymmetric lobes, like we observe in this work. A similar pattern is observed in the inverse-designed mode exchanger device using topology optimization reported in [80], where the optimization algorithm incorporates a narrow trench in the design area to split the TE0 mode wavefront into two parts and introduces a relative phase shift by making them travel in two imbalanced channels with different effective indices. Also, the field pattern in Fig. 8 in [26] shows the rays in the lower half wavefront of the TE0 mode travel faster than the rays in the upper half wavefront through fictitious materials having intermediate permittivities (between those of Si and SiO_2 before the binarization step). Thus, the upper half wavefront lags in phase by π relative to the lower half wavefront by the time they reach the output waveguide.

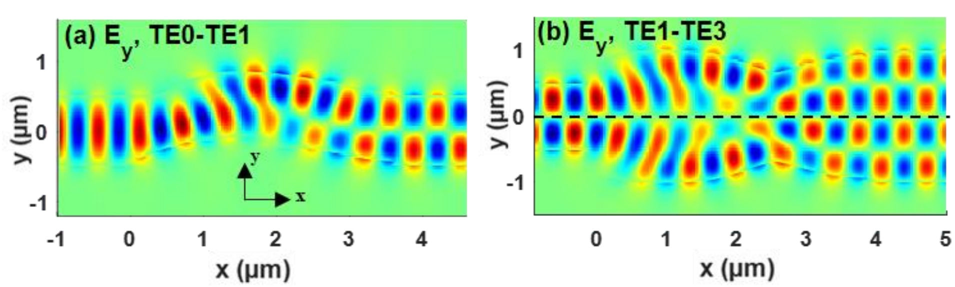


Fig. 3.8 The y-component of the electric field distribution in (a) TE0-TE1 mode converter and (b) TE1-TE3 mode converter.

For the TE0-TE1 mode converter in this work, Fig. 3.8 (a) suggests that the upper portion of the TE0 mode wavefront travels a longer optical path than the lower portion. This way the upper portion accumulates gradual shifts in the phase and the spatial field amplitude before reaching the output waveguide. Thus, across the design area, the fundamental TE mode transforms into TE1 mode with the wavefront having two antisymmetric lobes. This very mechanism is observed in the field profiles of other TE0-TE1 mode converters we optimized. With the same dimensions of the input/output (I/O) waveguides, the effective index of TE1 mode is smaller than the effective index of TE0 mode. Therefore, to convert TE0 mode into TE1 mode, the propagation constant needs to be reduced in the design area. To accomplish this change in the propagation constant, the algorithm chooses the shape of the design such that, in addition to the phase and the spatial amplitude shifts, the optical rays deviate from its initial propagation axis, adjusting the k-vector projection to match that of the TE1 mode in the output waveguide. Similarly, if the conversion of TE1 mode to TE0 mode is considered, Fig. 3.3 (d) and Fig. 3.8 (a) show that the two antisymmetric lobes of TE1 mode are combined into one lobe, which is guided by the oblique design boundary in such a way that the wavevectors make smaller angle with the horizontal axis of the left waveguide. Thus, the k-vector projection along the propagation axis is increased to match the propagation constant of the TE0 mode. For the mode converter devices with I/O waveguides having different dimensions, similar maneuver of optical rays takes place in the design area to match the propagation constant of the specified mode in the output waveguide. This explanation also applies to the mode conversion of TE1-TE3. The field pattern in Fig. 3.8 (b) shows both TE1 and TE3 have antisymmetric field (E_y) profile with respect to the horizontal axis (black dashed line). To convert the TE1 mode into TE3 mode, two antisymmetric lobes are formed from each of the lobes of TE1 mode. The different portions of the wavefront of TE1 mode travel different optical paths, and a π-phase shift is accumulated on half of each of the TE1 mode lobes. In fact, the field pattern on either side of the horizontal dashed line has strong resemblance with the field pattern observed in Fig. 3.8 (a), implying both TE1 lobes went through identical change in phase and amplitude rearrangements which justifies the symmetry in the design geometry.

The effects of under/over etch on the conversion efficiency in these mode converters provide supportive evidence to the conversion mechanism described above. The CE peak shifts toward shorter wavelength for over etch fabrication error, where the device boundary shrinks by 10 nm on both sides. The opposite effect is noticed on the CE peak for under etched devices. This shift in the CE peak substantiates the concept of optical rays on the wavefront traveling different optical path lengths. As the device boundary shrinks, it favors the optical signal with shorter wavelengths to achieve the peak conversion efficiency, since it requires relatively smaller optical path mismatch (with respect to the central wavelength of 1.55 μm) to accumulate a π-phase shift. A similar argument is applicable to CE peak shift towards longer wavelengths in the under etched devices.

Additionally, the CE peaks at shorter wavelengths are higher than those at longer wavelengths. This trend is explained by the fact that optical modes at shorter wavelengths are more confined in the silicon waveguide than the modes at longer wavelength. More confined modes have smaller evanescent field spread in the cladding and experience less scattering loss caused by waveguide sidewall roughness. Hence, higher conversion efficiency is obtained at shorter wavelengths. It has been demonstrated in [49] that reduced field overlap with the boundary makes the designs more tolerant to fabrication imperfections.

3.4 Symmetry and asymmetry of the design geometry

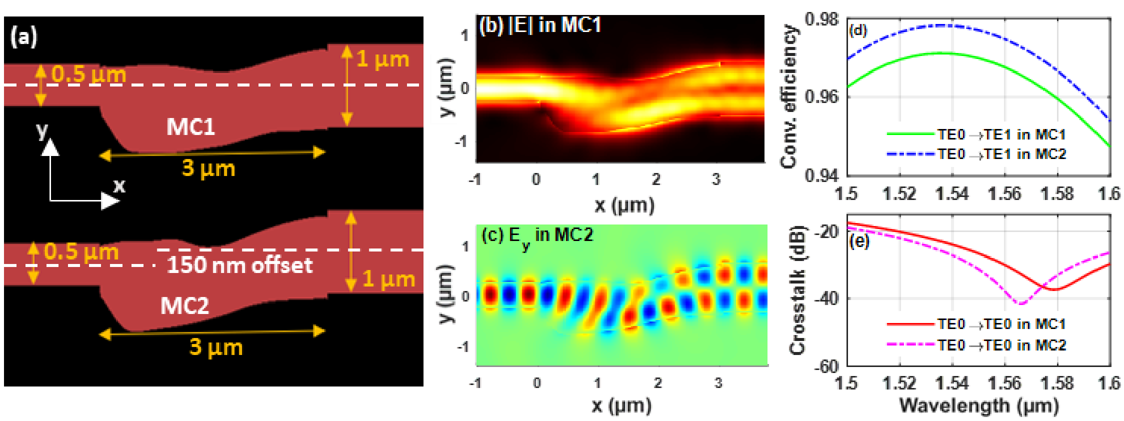


Fig. 3.9 (a) TE0-TE1 mode converters with I/O waveguides lying on the same horizontal axis (MC1) and with an offset of 150 nm between the waveguide axes (MC2), (b) electric field amplitude distribution in MC1, clearly showing formation of two lobes of TE1 mode as TE0 mode enters from left, (c) E_y distribution in MC2, showing the conversion of symmetric TE0 mode to into antisymmetric TE1 mode, (d) conversion efficiencies of MC1 and MC2, consistently higher mode conversion efficiency across the bandwidth, (e) modal crosstalks calculated in 3D FDTD simulations using the mode expansion monitor.

It is worth noticing that TE0-TE1 mode converter is asymmetric, while TE1-TE3 mode converter is symmetric. To convert a symmetric mode, in terms of E_y field distribution with respect to the propagation axis, such as TE0 into an antisymmetric mode such as TE1, a phase shift of π needs to be introduced to the half of the wavefront. This operation requires imbalanced optical paths for different parts of the wavefront. Therefore, an asymmetric design geometry is needed to perform the operation. On the other hand, the conversion between a symmetric mode pair, such as TE0-TE2, or an antisymmetric mode pair, such as TE1-TE3, requires symmetric design geometry as long as the I/O waveguides lie on the same horizontal axis since the mode conversion operation is symmetric with respect to the propagation axis like it is discussed in the previous section. This appreciation of (a)symmetry in the device structure and its operation leads to formulation of the design problem such that more efficient final designs are obtained in the same design area and with the same parameter initialization [74]. It has been shown that for mode conversion between a symmetric mode and an antisymmetric mode, introducing a lateral offset between the I/O waveguides results in more efficient designs than the designs with I/O waveguides lying on the same horizontal axis. The offset facilitates the asymmetry needed by the mode conversion operation.

To demonstrate the concept, a set of TE0-TE1 mode converters are optimized with lateral offsets between the I/O waveguides' axes and compare their performance with the initial designs with no offset. Without any exception, for all 16 TE0-TE1 mode converters mentioned earlier, higher FOMs are obtained by placing one waveguide vertically off the axis. In this section, we report MCs having different waveguide widths—0.5 μm for TE0 mode and 1 μm for TE1 mode. The spacing between the waveguides is 3 μm. Fig. 3.9 (a) shows the final optimized designs without any lateral offset (MC1) and with a lateral offset of 150 nm (MC2). These designs have not been fabricated, and we report the simulation results only. The mode conversion efficiencies are plotted in Fig. 3.9 (d). The mode conversion efficiency increases by 0.7% on average, as the lateral offset is introduced, across the wavelength range from 1.5 μm to 1.6 μm. This is not a significant improvement. However, we also need to consider that the CE peak of MC1 is 97%; there is not enough room left to make significant improvement in CE. In this regard, 0.7% higher efficiency is appreciable. Fig. 3.9 (e) shows both MCs have similar crosstalk performance.

3.5 Designing in two steps

Unlike the earlier two types of mode converters, designing efficient TE0-TE2 and TE1-TE2 mode converters seemed to be challenging in shape optimization method in a single step — deciding the design area dimensions, parameterizing the boundary points of a guess structure, and optimizing it first in 2D and then reoptimizing in 3D simulations. In the non-convex design parameter space, random starting points lead the gradient-based optimization to different local optima, with no guarantee of reaching the global optimum. Since the design parameters can assume any values within the bounds, there are infinite number of possible starting shapes, some of which lead to very efficient designs. Therefore, smart initializations based on the designer's insight about the device functionality and/or the underlying physics can significantly speed up the optimization process, avoiding the time-consuming process of trying out many random initializations. Additionally, guided by our interpretation of the mode conversion mechanism, efficient TE0-TE2 and TE1-TE2 mode converters are eventually designed in a two-step process- first, designing two components separately to perform different operations on the wavefront, and then, optimizing the final design consisting of the two components cascaded. In our repeated attempts to design these mode converters, it is seen that the conversion of a higher order mode to a lower order mode in the forward simulation and the opposite in the adjoint simulation takes lower number of iterations to converge. In the following section, the problems encountered while designing TE0-TE2 mode converters are discussed and how our interpretation of the field pattern led us to develop a two-step design process with smart initialization.

3.5.1 TE0-TE2 mode converters

In the single-step approach, within 4.2 μm I/O waveguide spacing, among more than 26 different initializations, only four led to final designs having conversion efficiencies above 74%. Fig. 3.10 (a) shows the optimized design of the best TE2-TE0 mode converter, with a CE of 78.6% at 1.55 μm. The mode conversion mechanism begins with having the side lobes travel longer optical paths to bring them in the same phase as that of the central lobe. Meanwhile, the structure suddenly becomes narrow in an attempt to converge the wavefront into one lobe of a TE0 mode. The optimized design suffers from significant loss of optical power in the mode conversion process. The reason is investigated for the consistent poor performance. In the simulation region, four frequency-domain field and power monitors are placed at different positions, as indicated by the vertical dashed lines denoted as m1, m2, m3, and m4. Transmissions through these monitors are plotted in Fig. 3.10 (b). A large difference between the transmissions through m1 and m2 indicates a significant amount of power loss in that region. It turns out when the side lobes of TE2 mode hit the design boundary portions denoted as ab and a'b' in Fig. 3.10 (c), some power escapes into the cladding, and some power is reflected back. The reflected power can be seen in the dashed rectangular box on the left (Fig. 3.10 (c)). As this region of the input waveguide is located behind the optical mode source, only the reflected optical power is captured by that monitor. The input waveguide is 3 μm wide since narrower input waveguide consistently resulted in poorer performance. Transmission decreases further in the region between m2 and m4. The lowest two curves in Fig. 3.10 (b) are the final transmission and conversion efficiency recorded by a monitor placed at 20 μm from the end of the design area.

The abrupt change in the waveguide width in the region between m1 and m2 is responsible for the high optical loss. However, a notable difference in the transmissions through m2 and the monitor placed at far led us to examine the convergence of the wavefront into one lobe more closely. By examining Fig. 3.10 (d) and (e), it is seen that after having the three lobes in the same phase, the wavefront splits into two symmetric lobes first before converging into one lobe. The E_y field distribution inside the dashed rectangle in Fig. 3.10 (d) vaguely hints at this, while E_x field profile in Fig. 3.10 (e) clearly shows the formation of two lobes before converging into one, which propagates as the fundamental mode through the output waveguide. Note that in a TE0 mode propagating along the x-axis, E_x components have antisymmetric distribution along the y-axis. The additional optical power loss because the two symmetric lobes do not get sufficient space to efficiently converge into the fundamental TE mode. Rather, a small fraction of light is coupled into radiative modes which decay into the cladding leaving out the TE0 mode in the output waveguide.

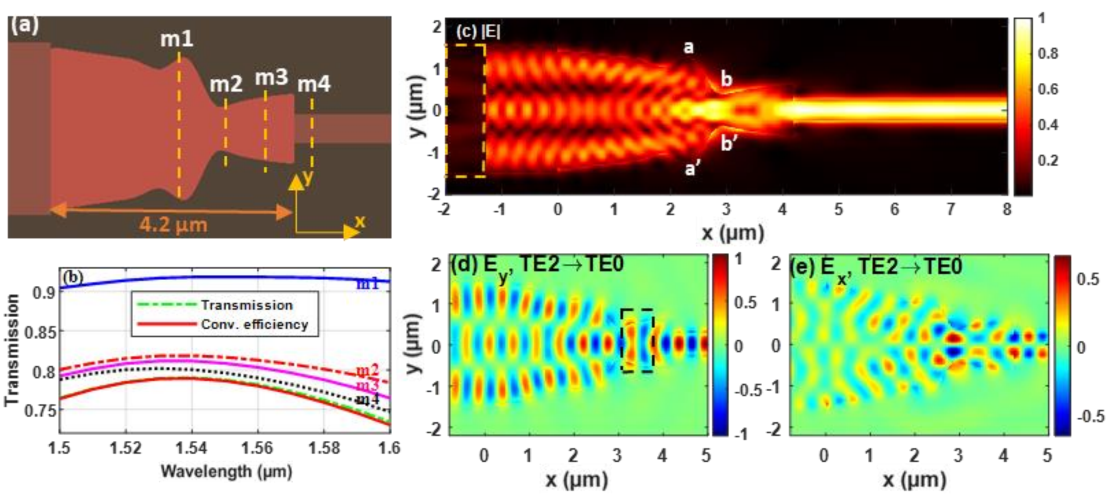


Fig. 3.10 (a) 4.2 μm long TE0-TE2 mode converter layout optimized in a single step with dashed lines indicating the positions of the monitor to calculate the transmission, (b) transmissions through the four monitors (m1, m2, m3, m4) and final transmission into TE0 mode, (c) electric field amplitude distribution, (d) electric field y-component distribution, (e) electric field x-component distribution showing the formation of two lobes with the same phase before merging into one.

The presence of electric field in the x-component (E_x) in TE modes may seem unusual. E_x exists for two reasons. First, for a propagating TE mode even in a straight waveguide, wavevectors of the optical rays are not exactly parallel to the waveguide axis (*i.e.*, the x-axis in the reference frame adopted in this work) as the optical rays proceed through successive total internal reflections. Therefore, the electric field is not exactly entirely parallel to the y-axis. Second, following Maxwell's equations, the electric field is calculated using the curl operation on the magnetic field vector. In a waveguide with finite width and height, the magnetic field distribution is nonuniform over the cross-sectional plane resulting in nonzero partial derivatives along all axes giving rise to E_x component in addition to E_y and a very small E_z component along the side walls.

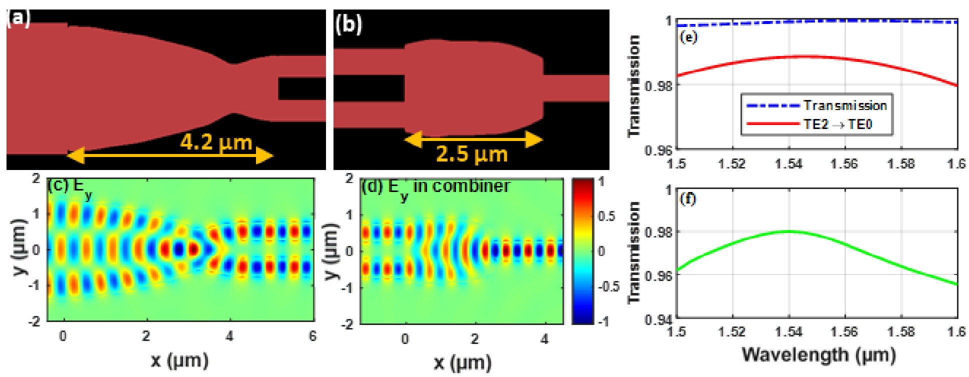


Fig. 3.11 (a) Design geometry of the TE2-TE0 mode converter which first splits the optical power into two output waveguides (TE0 modes), (b) design geometry of the TE0 combiner (a flipped 3 dB splitter), (c) E_y field distribution showing the mode conversion from TE2 to TE0, and the 3 dB splitting of the optical power into two lobes with same phase, (d) E_y field distribution of the combiner, (e) total transmission (blue curve) captured by the monitor and the combined transmission from the two output waveguides into TE0 mode (red curve); the difference between those two curves represent the scattering into other modes (modal crosstalk) and radiative modes, (f) transmission obtained in the power combiner output.

To make room for the split lobes to merge, it would be a time-consuming search for a good final design if we increased the design area length by step and tried out different initial parameters. Rather, based on our observation of the wavefront splitting into two symmetric lobes, we design two components to design a TE2-TE0 mode converter with two outputs and a combiner. The first component takes TE2 mode as the input and splits the optical power at the two output waveguides as TE0 mode. The device topology is shown in Fig. 3.11 (a) and E_y field distribution is shown in Fig. 3.11 (c). The input waveguide and the design area dimensions are kept the same as before, but the single output is replaced by two output waveguides separated by 0.5 µm. The optimized design smoothly brings the three lobes of the input TE2 mode in the same phase and splits the power into two symmetric lobes. With no abrupt change in its width, like in the previous one, the unwanted back reflection and scattering loss in the cladding decrease remarkably. The total transmission and combined transmission through the two output waveguides into the fundamental mode are plotted in Fig. 3.11 (e). We then design a combiner, which is simply a flipped 3 dB optical power splitter. The final combiner design is shown in Fig. 3.11 (b). It takes two inputs and combines them into a single lobe of the fundamental TE mode in the waveguide on right. Fig. 3.11(d) shows the E_y field distribution, and the transmission is plotted in Fig. 3.11 (f).

In the second step of our TE2-TE0 mode converter design, these two components are cascade and 17 points on one of the side boundaries are taken as the design parameters for the final optimization. Note that the symmetry in the design geometry does not require optimizing parameters on both side boundaries. The cascaded structure is re-optimized changing the input waveguide width from 3 μm to 2 μm. The final design, its field profile, and performance are shown in Fig. 3.12. The mode conversion efficiency (CE) at 1.55 μm is 96.4%, which is higher than the CE that would be obtained if the above two components were cascaded without further optimization. The mode conversion efficiency drops by approximately 2% at the central wavelength 1.55 μm when introducing a ±10 nm dimensional variations (see Fig. 3.12 (d)).

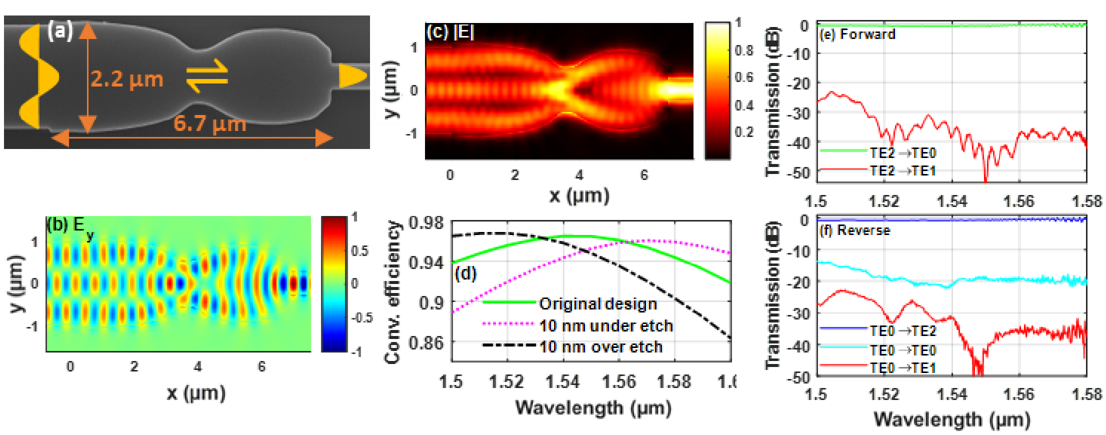


Fig. 3.12 (a) SEM image of the TE0-TE2 mode converter and its footprint, (b) E_y field distribution showing the mode conversion, (c) electric field amplitude distribution, (d) mode conversion efficiencies of the original design with 10 nm under and over etched devices showing an efficiency dropping by appr. 2% at 1.55 μm, (e) forward transmission spectrum of TE2 converted into TE0 with modal crosstalk into TE1 mode, (f) reverse transmission spectrum from converting TE0 into TE2 mode with modal crosstalk into TE0 and TE1 modes.

This MC has the lowest crosstalk across the entire optical bandwidth. Since the 0.5 μm wide output waveguide can support only TE0 mode and TE1 mode with lower confinement, but it does not support TE2 mode. Thus, transmission into TE2 mode is eliminated. The field profile of TE1 mode is antisymmetric with respect to the propagation axis, thus, with a symmetric TE2 mode as the input and symmetric device geometry, very small amount of light is coupled to the TE1 mode. Fig. 3.12 (e) shows modal crosstalk below -23.5 dB while it is below -30 dB in the C-band. For both forward and reverse propagation, the device insertion loss is below 1.2 dB across the wavelength span of 80 nm from 1.5 μm to 1.58 μm. In Fig. 3.12 (f), we observe that the crosstalk performance degrades in the wider waveguide when the signal travels in the opposite direction and TE0 mode is converted into the TE2 mode. In the reverse propagation, the dominant crosstalk is the optical power remaining in the TE0 mode, while very small amount of power is coupled into the TE1 mode.

3.5.2 TE1-TE2 mode converters

Similar to the previous one, TE1-TE2 mode converters designed in direct parameterization and optimization in a single step kept resulting in low conversion efficiencies. But once an efficient TE0-TE2 mode converter was designed in two steps, the approach to designing an efficient TE1-TE2 converter became obvious. To cascade with the first (left) component, instead of a combiner (a flipped 3 dB splitter), a component is designed that takes the fundamental TE mode through two input waveguides, introduces a π-phase shift onto one input wavefront with respect to the other, and transforms those into two antisymmetric lobes of a TE1 mode in the output waveguide. Like discussed before, introducing a phase shift requires the two input TE0 mode wavefronts to travel unequal optical paths. A design with symmetric boundaries cannot do the job. A 1 μm wide waveguide is chosen on the right of the design area as the output channel. Previously, it was demonstrated that introducing an offset between the input and output waveguides for TE0-TE1 mode conversion resulted in higher mode conversion efficiency because of the asymmetry in the structure [74]. For each of the 16 TE0-TE1 mode converter designs, an offset between the I/O waveguides consistently gave better mode conversion efficiency than the base design with I/O waveguides lying on the same axis. Following this idea, after running a few sweeps, the narrower waveguide is moved upward by 0.35 μm, shown by the dashed lines in Fig. 3.13 (a). This lateral offset facilitates the optimization of the second component having an asymmetric geometry. As the second step of this design approach, this new component is cascaded with the earlier design which splits the optical power of the TE2 mode into two output channels in TE0 mode. Then the cascaded structure is reoptimized to obtain the final design of the TE1-TE2 mode converter. Lengths of the individual components are 4.2 μm and 3.6 μm, respectively, making the final design footprint 7.8×2.25 μm^2. The mode converters with lateral offsets between the I/O waveguides were not sent for fabrication. Therefore, the simulation result is only reported for now. Fig. 3.13 (b) shows mode conversion efficiencies for both mode conversion directions above 95% across the wavelength range from 1.5 μm to 1.6 μm. Electric field distributions are shown in Fig. 3.13 (c) and (d). According to the FDTD simulation, modal crosstalk is below -19 dB over the 100 nm bandwidth. As shown in Fig. 3.13 (f), the conversion efficiency stays above 90% despite introducing ±10 nm dimensional variations.

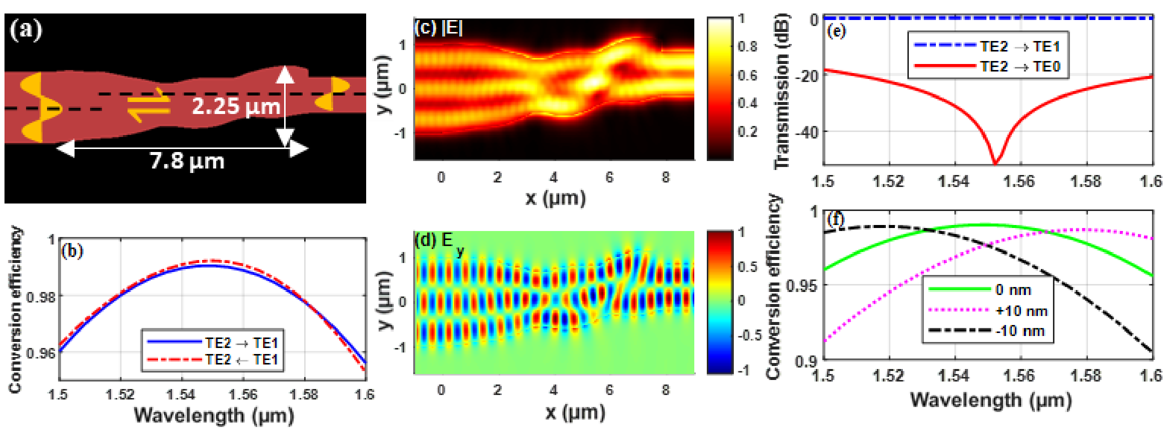


Fig. 3.13 (a) Final optimized design of the TE1-TE2 mode converter and its footprint, (b) mode conversion efficiencies for forward and reverse propagation with peak efficiency of 99.2% at 1.55 μm, (c) electric field amplitude distribution, (d) E_y distribution showing the mode conversion between antisymmetric TE1 mode and symmetric TE2 mode, (e) transmission spectra of the TE2-TE1 mode conversion with crosstalk into TE0 mode, (f) effects of 10 nm under and over etches on the mode conversion efficiency with mode conversion efficiency dropping by appr. 1.5% at 1.55 μm for 10 nm dimensional variations.

3.6 Summary

In this chapter, inverse designed broadband SOI mode converters for TE polarization are designed using an adjoint shape optimization. Note that the same method can be used to design mode converters for TM polarization by carefully selecting the mode order in the optimization algorithm. The footprints of the MCs in this work range from 3 μm to 7.8 μm in length. Based on 3D FDTD simulations, the mode conversion efficiencies are predicted to be above 95% across 100 nm wavelength span centered at 1.55 μm. Experimental data shows the maximum insertion loss is 1.2 dB across the wavelength range from 1.5 μm to 1.58 μm, while modal crosstalk remains below -19 dB in the C-band. Due to the optical bandwidth limitation of the grating couplers used for interfacing with off-chip fibers, the measured results beyond 1.58 μm are unreliable and, therefore, are not reported. The design approach is formulated in such a way that the device structure consists of a single silicon block between the I/O waveguides, ensuring high confinement of the optical fields in the Silicon core, which makes the designs robust to fabrication imperfections. Despite introducing ±20 nm waveguide width variations, the mode conversion efficiency remains above 90% across the entire bandwidth of 100 nm. The working mechanism of the MCs are also investigated and validated by simulation and experimental data. Open eye diagrams are obtained for 28 Gbps OOK transmission with a Q-factors of 8 dB and a 20 GBaud PAM-4 payload transmission, demonstrating the utility of these devices in high-capacity optical communication systems.

Chapter 4

Computation cost reduction in shape optimization

While designing a photonic device, besides the primary functionality, other performance attributes may turn out to have crucial importance depending on the specific application. Often trade-offs are made among various performance attributes, such as broadband grating couplers often come at a cost of reduced peak coupling efficiency [83], topology optimized wavelength multiplexer more tolerant to fabrication imperfections comes at a cost of reduced channel transmission [49], to name a few. For high-speed data transmission, reduction of the crosstalk at the operating wavelength is of serious importance. Thus, it is useful to have a comprehensive collection of optimized designs with different design samples being superior to the others for different performance attributes. In traditional design approaches, often the design parameters can be directly correlated with specific performance attributes, for instance, longer photodetectors tend to have higher responsivity [84], longer directional couplers tend to be broadband [79], etc. Thus, in traditional design approaches, the effects of a handful of design parameters can often be easily mapped to the performance attributes of the photonic device. As the functionality span of the photonic devices expands [85-87], and more complicated geometries are optimized in limited footprints [88], advanced optimization methods such as particle swarm optimization [89], genetic algorithm [90], topology optimization [91] and shape optimization [92] in inverse design are deployed. These methods optimize the device performance by tuning many design parameters such that the direct correlation between a specific design parameter and a performance attribute is usually nonintuitive. Even though in gradient descent-based optimization, the objective function can be defined such that it optimizes several performance attributes simultaneously, it can take a lot of experimentation to specify the right objective function that provides the best trade-off among all the requirements. Thus, an exhaustive search of the local optima is needed.

Recently, some investigations have been conducted to establish a computational mapping between the design parameters and the performance attributes, where principal component analysis was implemented to form lower dimensional design subspaces where good designs reside [83, 93-95]. To conduct such studies on a comprehensive collection of possible good designs in a given design parameter space (corresponding to local optima), finding good designs through many random initializations is a time-consuming process in addition to incurring a huge computation cost. Even though 2D optimization is fast, not all the 2D optimized designs retain their good performances after being re-optimized in 3D FDTD simulation. This is manifested by the statistics collected in this work — only 59 designs out of 85 2D optimized designs eventually retain an average mode conversion efficiency above 90% after being re-optimized in 3D simulations. Thus, before selecting the good designs for fabrication, it is important to characterize their performance in 3D simulation. But 3D optimization is significantly more computation expensive. In this work, a regression model has been utilized to predict the final design parameters, which, when used as the starting point of the 3D optimization, take 35% less time to converge to the final designs.

4.1 Methodology

A machine learning based regression model is adopted to demonstrate computation cost reduction on 3D optimization. The regression model is used to predict the final design parameters after 3D optimization. It takes the design parameters of the 2D optimized design as the input and calculates their probable 3D optimized values. Assume that the design is defined by n design parameters. Let p_{2D_i} denote the i-th parameter of a 2D optimized design, while p_{3D_i} denotes the i-th parameter of the 3D optimized design. We define $\boldsymbol{W}$ as the $n \times n$ weight matrix and $\boldsymbol{w}_0$ as a $n \times 1$ column vector such that,

$$\begin{bmatrix} w_{11} & \cdots & w_{1n} \\ \vdots & \ddots & \vdots \\ w_{n1} & \cdots & w_{nn} \end{bmatrix} \begin{bmatrix} p_{2D\_1} \\ \vdots \\ p_{2D\_n} \end{bmatrix} + \begin{bmatrix} w_{10} \\ \vdots \\ w_{n0} \end{bmatrix} = \begin{bmatrix} p_{3D\_1} \\ \vdots \\ p_{3D\_n} \end{bmatrix} \tag{3.1}$$

In the compact form, it can be written as $\boldsymbol{W}\boldsymbol{p}_{2D} + \boldsymbol{w}_0 = \boldsymbol{p}_{3D}$, where $\boldsymbol{p}_{2D} = [p_{2D\_1}\ p_{2D\_2}\ \ldots\ p_{2D\_n}]'$ and $\boldsymbol{p}_{3D} = [p_{3D\_1}\ p_{3D\_2}\ \ldots\ p_{3D\_n}]'$. To conduct the study, a dataset containing all optimized designs is split into a training set and a test set. Then the pairs of 2D and 3D optimized designs in the training set are used to train the regression model to obtain deterministic values of the weight terms w_{ij} and the bias terms w_{i0}. After that, this regression model is used to predict the 3D optimized parameters of the 2D optimized designs in the test set. Let p_{reg_i} denote the i-th predicted parameter by the regression model, then the predicted parameters are obtained by

$$\begin{bmatrix} p_{reg\_1} \\ \vdots \\ p_{reg\_n} \end{bmatrix} = \begin{bmatrix} w_{11} & \cdots & w_{1n} \\ \vdots & \ddots & \vdots \\ w_{n1} & \cdots & w_{nn} \end{bmatrix} \begin{bmatrix} p_{2D\_1} \\ \vdots \\ p_{2D\_n} \end{bmatrix} + \begin{bmatrix} w_{10} \\ \vdots \\ w_{n0} \end{bmatrix} \tag{3.2}$$

In the compact form, it becomes $\boldsymbol{p}_{reg} = \boldsymbol{W}\boldsymbol{p}_{2D} + \boldsymbol{w}_0$, where $\boldsymbol{p}_{reg} = [p_{reg\_1}\ p_{reg\_2}\ \ldots\ p_{reg\_n}]'$. To validate the effectiveness of the approach, the predicted designs (composed of the predicted design parameters) are reoptimized in 3D simulations. Then, the time needed to converge to the final design is compared with the time needed for the 2D optimized design to converge to the final design.

4.2 Device chosen for demonstration and how the dataset is built

To conduct this study, a type of device is needed such that for given I/O waveguide dimensions and the spacing between them, many good designs are obtainable in the design parameter space. For the diversity of the design geometry, the devices with asymmetric geometry are more favorable than the devices with symmetric geometry since a structure can be asymmetric in many ways. On the other hand, symmetry imposes limitations on availability of various design structure geometries that can perform the operation in question. Here, the TE0-TE1 mode converter is chosen for a conceptual demonstration. The MCs are designed for the SOI platform with a silicon layer thickness of 220 nm. A 0.45 μm wide single-mode waveguide is used to carry the fundamental TE mode, while the waveguide width is set to 0.85 μm for TE1 mode to avoid higher order modes, eliminating the chance of contributing to crosstalk into modes other than the TE0 mode. The spacing between the I/O waveguides is chosen to be 3.6 μm, which is expected to be large enough to accommodate a variety of good base designs with the I/O waveguides aligned on the same axis.

It has been demonstrated that, for mode conversion between an even- and an odd-order TE modes, designs with asymmetric structure are favored by introducing a vertical offset between the I/O waveguides axes [73]. As shown in Fig. 4.1, 14 boundary points of the design structure, along with a vertical offset between the I/O waveguides, are taken as the design parameters for optimization using the gradient-descent based algorithm, LBFGS-B.

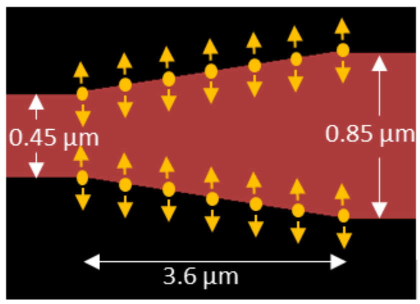


Fig. 4.1 Initialization of 2D optimization of the TE0-TE1 mode converter with arbitrary initial structure. The gradient-descent based algorithm moves around the boundary points in the design area to come up with a shape of the structure which maximizes the FOM.

Initially in 2D optimization, the I/O waveguides are positioned on the same horizontal axis, and out of 64 random initializations (excluding identical final designs), 12 designs turned out to have a figure of merit (FOM) above 90% which is the average mode conversion efficiency over 11 equally spaced wavelength points between the wavelengths 1.5 μm and 1.6 μm. Additional random initializations keep resulting in 2D optimized designs which are already found. Therefore, these 64 designs may be considered almost as an exhaustive set of designs (local optima) in the given parameter space. The average mode conversion efficiencies (FOM) and the average modal crosstalks across the optical bandwidth of 1.5- 1.6 μm of these 2D optimized MCs are plotted in Fig. 4.2. As expected, MCs with high mode conversion efficiency have better crosstalk performance since less optical energy is left to contribute to the crosstalk mode.

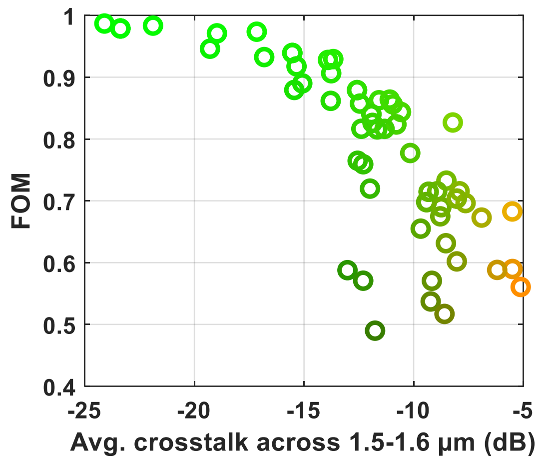


Fig. 4.2 Average mode conversion efficiency and average modal crosstalk of the 2D optimized devices.

For the next step of the study, 12 good designs are kept, while remaining designs having FOM below 90% are discarded. However, standard regression methods require more data points than the number of parameters. For MCs with and offset between the I/O waveguides, starting from scratch, i.e., random initializations for 2D optimization, would be a time-consuming task. Thus, instead of random initializations, additional copies of these 12 base designs (with I/O waveguides lying on the same horizontal axis) are optimized by introducing vertical offsets, both upward and downward, between the I/O waveguide axes ranging from 50 nm to 200 nm. These additional copies can be regarded as “variants” of the 12 base designs. This way, 85 2D optimized designs are obtained with FOM above 90%, each defined by 15 parameters (14 boundary points and a vertical offset).

The 85 2D optimized designs are re-optimized in 3D FDTD to construct the dataset. In 3D simulations, 59 designs turn out to have FOMs above 90%. Fig. 4.3(a) shows two 3D optimized designs, one base design without the vertical offset and the other with a 150 nm offset (the wider waveguide is moved upward by 150 nm with respect to the narrow waveguide). The mode conversion efficiencies of these two designs across the 100 nm bandwidth from 1.5 μm to 1.6 μm are plotted in Fig. 4.3 (b). Also, the average CE of all the variants (with different vertical offsets) of these two designs (denoted by circles and squares) are plotted in Fig. 4.3 (b). Though their mode conversion efficiencies are very close, resulting in similar transmission performances, some of the variants have appreciably lower modal crosstalk than the base design at different operating wavelengths, as depicted in Fig. 4.3 (c) and (d).

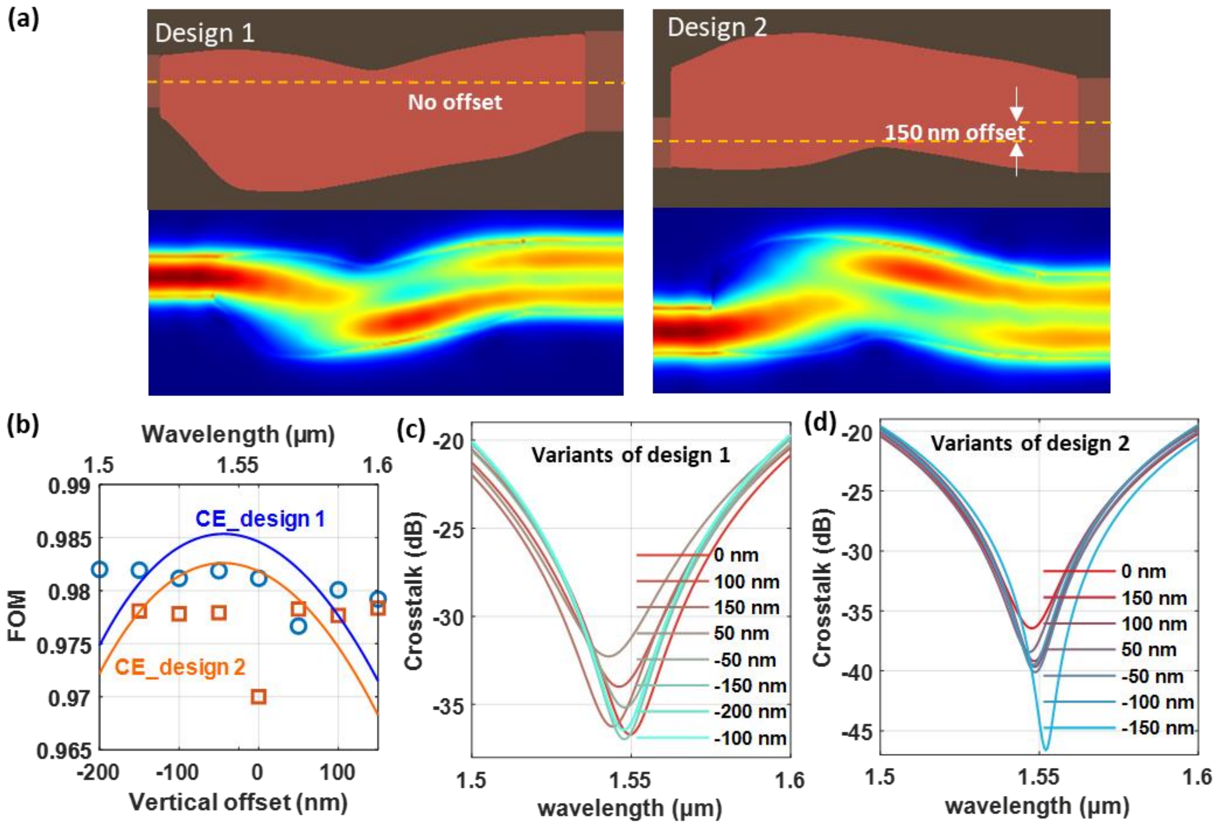


Fig. 4.3 (a) Two 3D optimized mode converters, one base design with no vertical offset (left) and the other design with 150 nm vertical offset (right) between the I/O waveguides, along with the electric field distributions showing the mode conversion; (b) mode conversion efficiency of design 1 and design 2 as a function of optical wavelength (top horizontal axis) and average mode conversion efficiencies (FOM) with respect to vertical offsets (bottom horizontal axis) of all the variants of the two 3D optimized designs; modal crosstalk of all variants of (c) design 1 and (d) design 2.

For the next step of this study, we keep the 59 3D optimized designs with FOMs above 90% and build a dataset consisting of the 15 design parameters and four performance attributes: 1) average mode conversion efficiency (FOM), 2) average crosstalk, changes in 3) FOM, and 4) crosstalk at 1.55 µm for ±20 nm width variations. Fig. 4.4 shows the average mode conversion efficiency and the average modal crosstalk of the selected 59 designs. The general trend follows the expectation — higher mode conversion efficiency implies lower modal crosstalk, except for a group of designs with FOMs around 96% having the lowest modal crosstalk. In the applications where modal crosstalk is a very important performance parameter, this group of MCs can be adopted with a small cost on the CE.

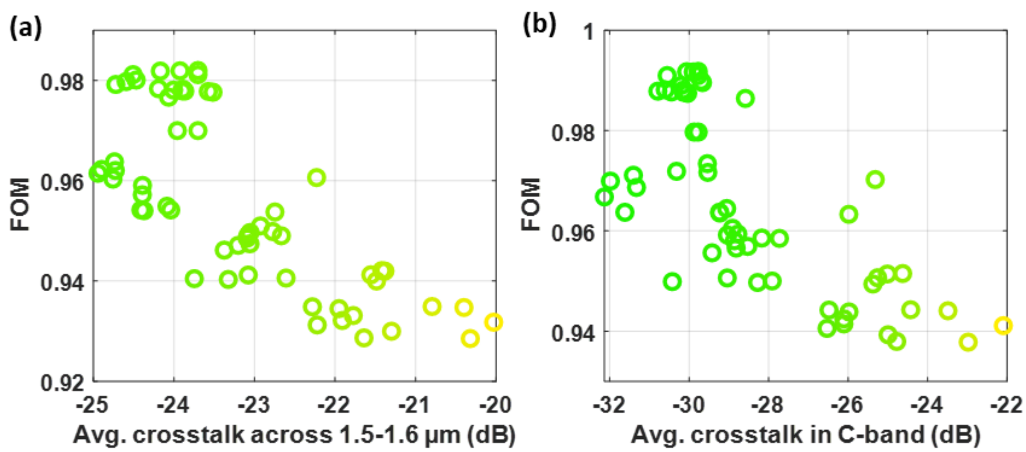


Fig. 4.4 Average mode conversion efficiency and the average modal crosstalk of the selected 59 3D optimized MCs (a) across the bandwidth of 1.5-1.6 μm and (b) in the C-band (1.530-1.565 μm).

Another important performance attribute of the photonic devices is the robustness to fabrication process variations. Since inverse designed devices have small features and are small in size, regular fabrication errors such as under etch and over etch cause notable impact on the device performance. Shape optimized MCs have been demonstrated to be tolerant to dimensional variations such as 10 nm under/over etches [96, 97]. This dataset contains 11 base designs with 11 different design geometries. It is likely that some of their performances are less affected by under/over etch fabrication errors compared. To quantify the effect of under/over etch on their CE and XT performances, additional copies with expanded and shrunk boundaries of the 11 base designs are simulated (to mimic the effect of under and over etch respectively). In Fig. 4.5 the effects of under and over etch on the mode conversion efficiency of these MCs are presented. The average CEs across the 1.5- 1.6 μm wavelength range of the nominal designs, under-etched, and over-etched designs are plotted in Fig. 4.5 (a) using ‘o’, ‘+’, and ‘x’, respectively, following the left vertical axis. The difference between the CE of the nominal design and the under-etched design is denoted as δ+, and the difference between the nominal design and the over-etched design is denoted as δ-. The average differences are also plotted in the same figure following the vertical axis on the right. For comparing the CE, the average value is a good representation since the minimum and maximum values of CE across the bandwidth of 1.5-1.6 μm are within ± 2% of the average value (Fig. 4.3 (a)). For a fixed operating wavelength of 1.55 μm, the corresponding CE and the differences are plotted in Fig. 4.5 (b). In both plots, design 1 seems to be the most robust while design 8 tends to be the most sensitive to the dimensional variations.

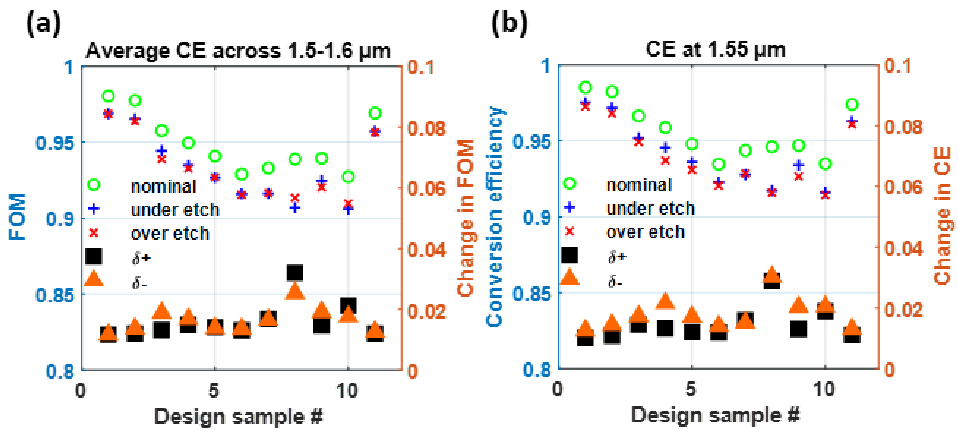


Fig. 4.5 (a) Average mode conversion efficiency (FOM) of the nominal, under etched, over etched designs plotted with respect to the left vertical axis; the changes in the FOM for 10 nm under etch (δ+) and 10 nm over etch (δ-) plotted for right vertical axis, (b) the mode conversion efficiency at 1.55 μm of the nominal, under etched, over etched designs plotted for left vertical axis; the changes in the CE for 10 nm under etch (δ+) and 10 nm over etch (δ-) plotted for right vertical axis.

Similarly, the effects of under and over etches on the crosstalk of these MCs are examined. The average crosstalk (normalized in linear scale) across the bandwidth of 1.5-1.6 μm calculated in logarithmic scale of the nominal designs, under-etched, and over-etched designs are plotted in Fig. 4.6 (a) using ‘o’, ‘+’, and ‘x’, respectively. Their differences are also plotted in the same figure with respect to the positive vertical axis.

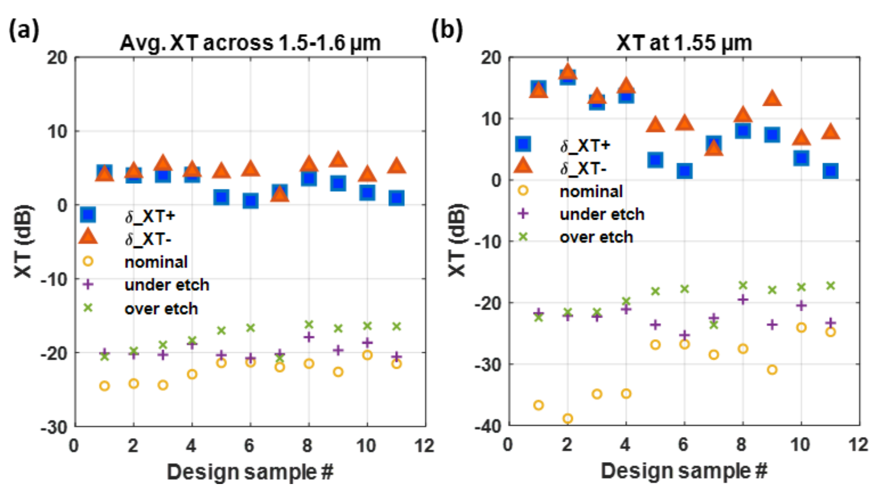


Fig. 4.6 (a) Average XT across the bandwidth of 1.5-1.6 μm of the nominal, under etched, and over etched designs, and their differences are plotted with respect to the positive vertical axis. δ_XT+ denotes the difference between the XTs of nominal and under etched designs, while δ_XT- denotes the the difference between the XTs of nominal and over etched designs. (b) the XT at 1.55 μm of the nominal, under etched, over etched, and their differences.

The difference between the average crosstalk of the nominal design and the under etched design is denoted as δ_XT+, while the difference between the average crosstalk of the nominal design and the over etched design is denoted as δ_XT-. However, unlike the mode conversion efficiency, the modal crosstalk varies widely across the bandwidth as shown in Fig. 4.3 (b) and (c). Thus, the average value across the bandwidth is not a very good representative of the device's robustness of crosstalk performance to the dimensional variations. Therefore, it would be more practical to choose an operating wavelength and compare the changes in the XT for under/over etch. Fig. 4.6 (b) presents the effect on the XT performance of these 11 design samples at a fixed operating wavelength of 1.55 μm. Design samples 6, 7, and 10 tend to be more robust to 10 nm under and over etches when XT is considered.

However, one may carefully notice that each of the design samples 6, 7, and 10 has relatively higher XT to begin with (more than 3 dB compared to design samples 1,2, and3). Measuring the change in XT in logarithmic scale may falsely guide the designer since 3 dB increase from an arbitrary -x dB accounts for twice the optical power corresponding to 3 dB increase from -(x+3) dB. Thus, measuring the XT in linear scale would make more sense for this kind of comparison.

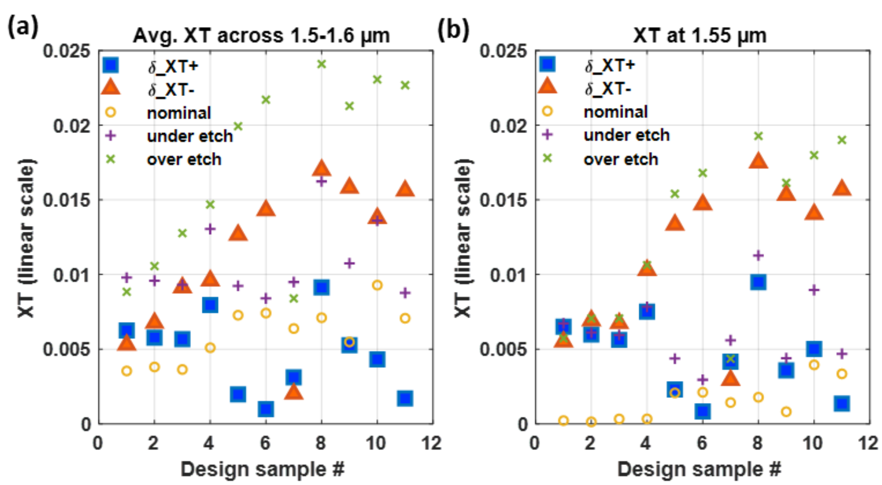


Fig. 4.7 (a) Average XT in linear scale across the bandwidth of 1.5-1.6 μm for the nominal, under etched, over etched designs, and their differences. δ_XT+ denotes the difference between the XTs of nominal and under etched designs, while δ_XT- denotes the the difference between the XTs of nominal and over etched designs. (b) the XT at 1.55 μm of the nominal, under etched, over etched, and their differences.

Therefore, Fig. 4.6 is regenerated with the XTs expressed in linear scale as shown in Fig. 4.7 where the vertical axis shows the fraction of optical power contributing to the XT. On the linear scale, design sample 7 stands out to be the most robust design with respect to under etch and over etch, while design samples 1-3 show lowest nominal XT as well as improved robustness compared to other samples.

4.3 Reduction of the computation cost

For a given performance attribute, some designs turn out to be better than thers. Therefore, depending on the application requirements different designs can be chosen as the most suitable ones. For example, if the operating wavelength is 1.55 µm and the crosstalk is the most important concern for a particular application, design 2 with -150 nm vertical offset between the I/O waveguide would be preferable over any of the variants of design 1, even though design 1 has ~2% higher average CE than design 2. To make the best choice among the available options, it is necessary to have a collection of good designs characterized for their performance attributes. But an exhaustive search of good designs in a given design parameter space is a time-consuming process incurring a prohibitive computation cost.

In this section, a machine learning based regression model is utilized to demonstrate 35% computation cost reduction on 3D optimization. The regression model is used to predict the final design parameters after 3D optimization. It takes the design parameters of the 2D optimized design as the input and calculates their probable 3D optimized values. To conduct the study, the dataset containing 59 optimized designs is split into a training set containing 24 randomly picked designs and a test set containing the remaining 35 designs. Then the 24 pairs of 2D and 3D optimized designs in the training set are used to train the regression model to obtain deterministic values of the weight terms w_{ij} and the bias terms w_{i0}. After that, this regression model is used to predict the 3D optimized parameters of the 2D optimized designs in the test set. p_{reg_i} denotes the i-th predicted parameter by the regression model, then the predicted parameters are obtained by

$$\begin{bmatrix} p_{reg\_1} \\ \vdots \\ p_{reg\_15} \end{bmatrix} = \begin{bmatrix} w_{11} & \cdots & w_{115} \\ \vdots & \ddots & \vdots \\ w_{151} & \cdots & w_{1515} \end{bmatrix} \begin{bmatrix} p_{2D\_1} \\ \vdots \\ p_{2D\_15} \end{bmatrix} + \begin{bmatrix} w_{10} \\ \vdots \\ w_{150} \end{bmatrix} \tag{3.3}$$

This way the predicted parameters are calculated for all 35 samples in the test set. Next, the Euclidean distances of the 3D optimized parameters from the 2D optimized parameters ($|p_{2D\_i} - p_{3D\_i}|$) and from the predicted parameters ($|p_{3D\_i} - p_{reg\_i}|$) are compared for the 35 samples in the test set. Fig. 4.8 shows the box plots of these Euclidean distances with their percentiles and some outlier points. The average difference between the 2D and 3D optimized parameters (all parameters combined) is approximately 86 nm with a standard deviation of about 87 nm and a standard error of the mean of 14.7 nm.

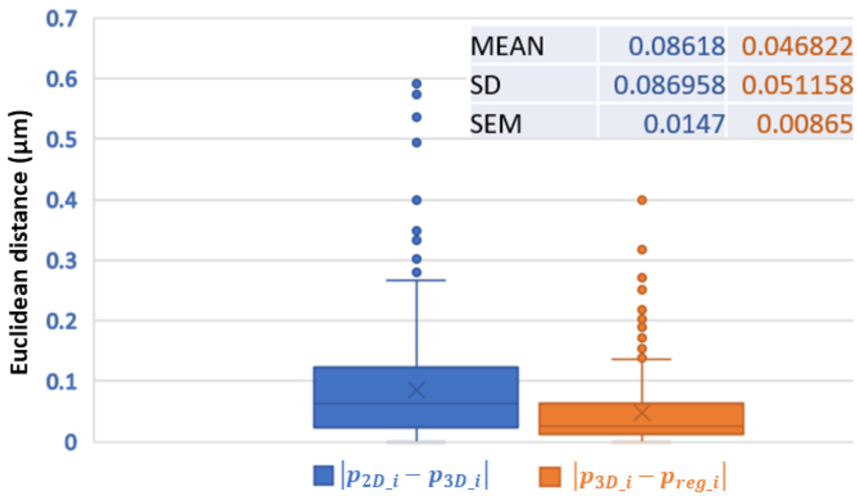


Fig. 4.8 The box plots showing the distributions of $|p_{2D\_i} - p_{3D\_i}|$ (blue) and $|p_{3D\_i} - p_{reg\_i}|$ (orange).

On the other hand, the average difference between the 3D optimized parameters and the predicted parameters is approximately 46.8 nm with a standard deviation of approximately 51.2 nm and a standard error of the mean of 8.7 nm. Evidently, the regression model is beneficial since the predicted structure (formed by the predicted parameters) is closer to the final 3D optimized structure than the 2D optimized design.

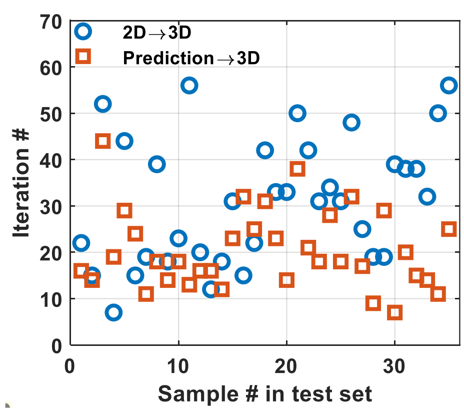


Fig. 4.9 Number of iterations needed by the samples in the test set to converge to the final 3D optimized designs starting from 2D optimized designs (blue circles) and predicted designs (orange rectangles).

Thus, it is expected that using the predicted structure as the starting point for the 3D optimization will effectively reduce the computation cost by reducing the number of iterations needed for the convergence of the optimization. To validate this hypothesis, all 35 predicted designs are optimized in 3D FDTD simulations. Fig. 4.9 shows the number of iterations needed, per sample, in the test set to converge to the final 3D optimized designs starting from the 2D optimized designs (blue circles) and the predicted designs (orange rectangles). Evidently, the predicted designs take less iterations to converge to the final designs except for 5 designs for which the predicted designs took more iterations for convergence than 2D optimized designs.

Table 4.1 summarizes some statistical data of the two approaches of optimization. The average number of iterations needed until convergence starting from the 3D predicted designs is around 20 while for the 2D optimized design starting points it is 31, implying around 35% computation cost reduction. Additionally, the predicted structures show an average mode conversion efficiency (FOM) of 76.2% in 3D FDTD simulation before optimization begins, while it is only 59% for the 2D optimized parameters. Within 5 iterations, the predicted structures reach an average FOM of 93.5% which is only 2.3% behind the final average FOM (95.7%). Thus, by predicting the design structures utilizing the regression model before the 3D optimization commences shows significant leverage over the traditional approach of performing 3D optimization starting from 2D optimized designs. This regression-based design prediction model can further leverage the computation cost reduction in dimensionality reduction-based design approach reported in [83, 93-95] since regression can help collect the initial set of optimized designs faster.

Table. 4.1 Statistical comparison between the optimization from 2D designs and the optimization from the predicted designs

	2D → 3D	Prediction → 3D
Number of samples	35	35
Average number of iterations to converge to the final design	31.1	20.4
Standard deviation of the average number of iterations	13.52	8.44
Standard error of the mean (of iteration #)	2.29	1.43
Average FOM at the 0^{th} iteration	0.5882	0.7618
Standard deviation of the FOM at the 0^{th} iteration	0.1860	0.2204
Average FOM at the 5^{th} iteration	0.9041	0.9350
Standard deviation of the FOM at the 5^{th} iteration	0.0579	0.0546

4.4 Summary

In this chapter, a machine learning-based regression model has been proposed to predict the final design parameters in the shape optimization method. The design parameter space is usually nonconvex and contains multiple local optima, and each optimum corresponds to a final design. Depending on the significance of a particular performance attribute, an individual or a group of designs may turn out to be more suitable than the rest. Thus, a collection of all the possible good designs is useful for various applications. It can also be used to build a process design kit (PDK) library containing multiple designs customized for different applications. This regression-based prediction model can be implemented to significantly reduce the computation involved with the time-consuming 3D optimization step for the exhaustive search. For a case analysis, the TE0-TE1 MC is chosen. With 3.6 μm spacing between the I/O waveguides and vertical offsets ranging from -200 nm to 200 nm, 59 3D optimized designs are obtained with average CE above 90%. 24 designs are used to train the regression model. Then it was used to predict the final design parameters of the 35 samples in the test set. It shows 35% save in the computation cost involved in the 3D optimization step. This model can be adopted for any other photonic interconnect design suing the shape optimization technique.

Chapter 5

Mode-division (de)multiplexers

To enhance the data transmission rate and on-chip data processing capacity, in densely integrated photonic circuits, mode-division multiplexing systems with compact footprint and excellent performance is of great importance. Mode multiplexers designed using asymmetric directional couplers exhibit low insertion loss and low modal crosstalk, but they typically encompass hundreds of μm^2 chip area [50-52]. Other conventional design approaches include utilization of multi-mode interferometer (MMI) [53, 54] and asymmetric Y-junction [55, 56]. These MDMs exhibit good crosstalk performance, often below -30 dB, but have large footprints ranging from tens to hundreds of μm^2. Increasing the number of modes in these multiplexer systems increases the device size substantially. Ring resonator based MDMs are small in footprint, but they suffer from narrow bandwidth [57].

In this regard, inverse design has enabled compact footprint mode multiplexers with low insertion loss, wide operating bandwidth, and good crosstalk performance [58, 59]. For complex functionalities like mode multiplexing, shape optimization would be a naive approach and not suitable for design optimization. Therefore, topology optimization is adopted in this work to design 3-channel MDMs.

5.1 Mode demultiplexer design approach

The insights obtained in the optimization of mode converters are implemented in designing mode division (de)multiplexers using topology optimization technique. In this section the design approach of three-channel MDMs is discussed. The objective of the topology optimization is to obtain a design which separates three input modes, TE0, TE1, and TE2, sent through the 1.5 μm wide multimode waveguide, into the three 0.5 μm wide output channels in their fundamental TE modes. Fig. 5.1 (a) shows the design footprint is set to 4.5×4.5 μm^2. 1.5 μm wide multimode waveguide is placed on the left of the design area and three 0.5 μm wide waveguides are placed on right side at 1 μm vertical spacing to carry the demultiplexed signals. The design area is divided into 50625 grid cells, each with an area of 20 × 20 nm^2. Material permittivities of these grid cells are the design parameters to optimize for the desired mode routing. The gradient calculations are performed using the adjoint method [46]; regardless of the number of design parameters in the optimization region, one backward FDTD simulation per objection function is sufficient to determine the gradient of the figure of merit (FOM) with respect to the design variables [47]. The optimization is performed in two phases — grayscale phase and binarization phase. Initially, each grid cell may assume any permittivity value in the range from 2.85 (SiO_2) to 12.05 (Si). Thus, the gird cells in the design area assume to be fictitious materials to guide the modes to the assigned channels.

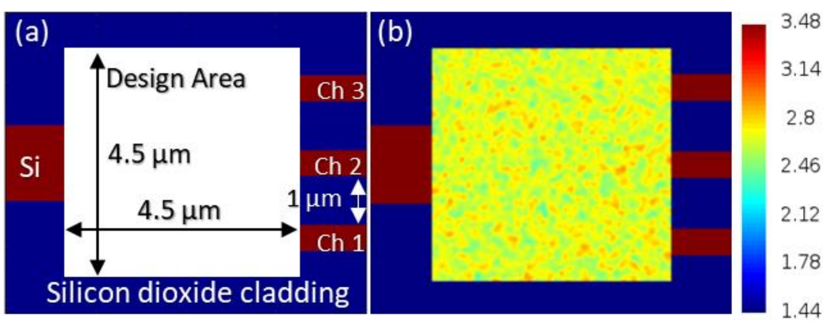


Fig. 5.1 Initialization of the topology optimization. (a) A 4.5×4.5 μm^2 design area with a 1.5 μm wide multimode waveguide on the left and three 0.5 μm wide single mode waveguide channels on right, equally spaced vertically at 1 μm interval, (b) initialization of the topology optimization with arbitrary permittivity value to each of the pixels in the design area; the colorbar shows the material index ranging from 1.44 to 3.48.

To initiate the optimization, random material index values are assigned to the grid cells in the design area as shown in Fig. 5.1 (b), with upper and lower limits of 3.48 and 1.44, respectively, corresponding to the material indices of silicon and silicon dioxide. In each iteration three pairs of forward and adjoint simulations are carried out for three input modes, and design parameters are altered following the gradient of the FOM, defined as the average modal overlap with the TE0 mode in the output waveguides. This requires the TE1 and TE2 modes to be converted into TE0 mode before entering in their respective channels.

Fig. 5.2 (a) shows that within 200 iterations, the FOM reaches 99%. The binarization step is introduced after 140 iterations. The effect of the binarization phase is depicted in Fig. 5.2 (b) which is the zoomed in plot of the apparently flat curved in Fig. 5.2 (a). As the beta factor in the sigmoid function increases, the sudden change in the design parameters causes sudden drop in the device performance, manifested by the kinks in the plot. The algorithm keeps reoptimizing the FOM until the design structure is more than 99% binarized.

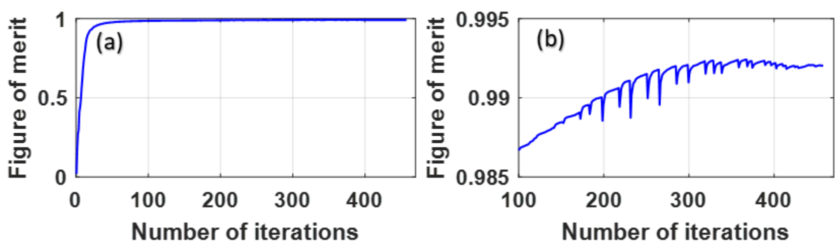


Fig. 5.2 (a) Convergence of the topology optimization of the MDM, (b) the zoomed in plot of the FOM after 100 iterations, showing the effect of the change in the beta factor manifested by the kinks in the graph. As the beta factor is increased, sudden change in the design parameters results in sudden drop in the FOM.

Fig. 5.3 shows the gradual evolution of a topology optimized mode demultiplexer. Initially, the pixels in the design area assume any permittivity values within the range to maximize the FOM.

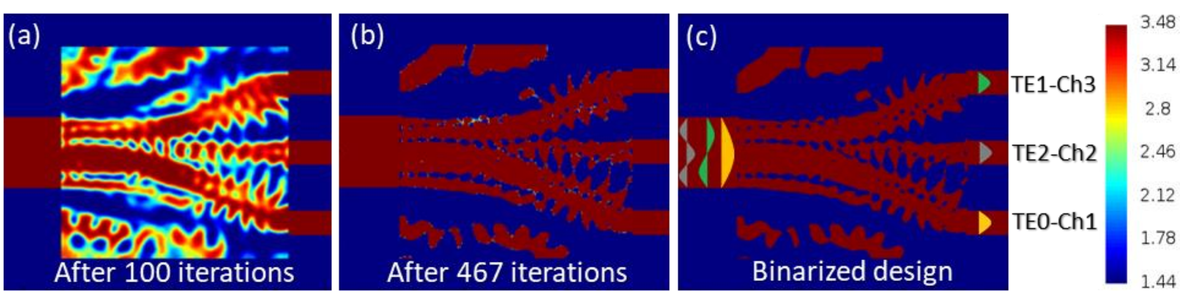


Fig. 5.3 Evolution of the topology optimized MDM design. (a) after 100 iterations, many grid cells in the design area have intermediate permittivity values, depicted by the yellowish regions, (b) the optimization converges to the final design after 431 iterations, and the design structure is almost binarized, (c) final design layout ready for fabrication, completely binarized as transferred to the gds file.

Thus, many grid cells end up having intermediate permittivity values, exhibited by the yellowish regions in Fig. 5.3 (a). After 140 iterations, as the binarization phase kicks in, the intermediate permittivity values are slowly pushed towards the upper and lower limits by increasing the beta factor of the sigmoid function at successive binarization steps, each consisting of 20 iterations. The topology optimization converges to a final design after 467 iterations, when less than 1% grid cells are not completely binarized, visible by the tiny regions in Fig. 5.3 (b). This final design is transferred to design layout where the entire structure consists of silicon and silicon dioxide only, shown in Fig. 5.3 (c). The assignment of the input modes to the output channels are also shown here. The reason behind choosing this channel order for different input modes will be discusses later.

5.2 Result and performance analysis

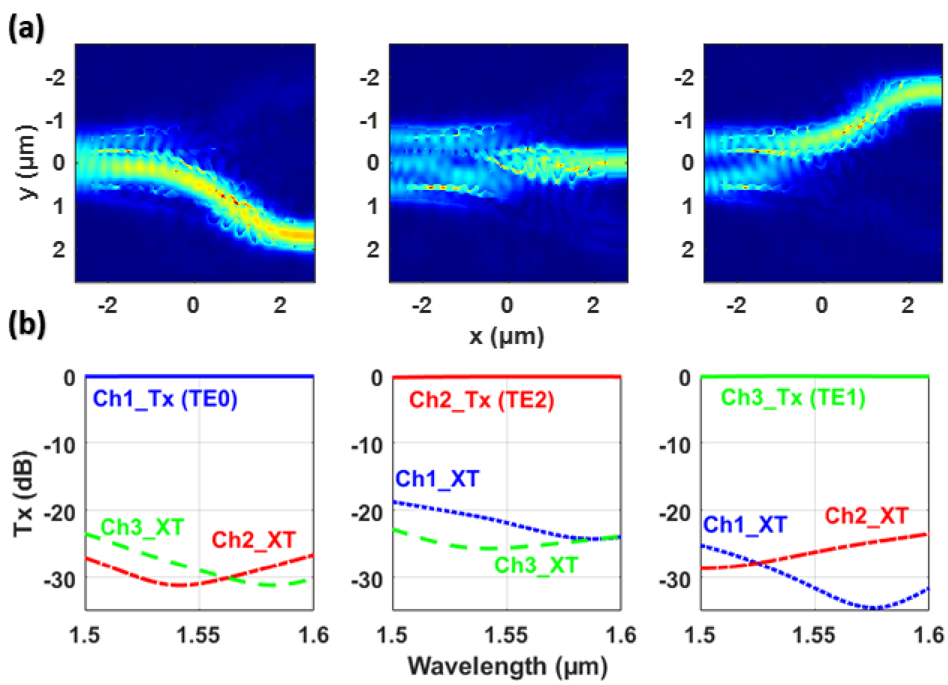


Fig. 5.4 (a) Simulated electric field patterns showing how three input modes are routed—TE0, TE1, and TE2 are routed to channel 1 (bottom), channel 3 (top), channel 2 (middle) respectively, (b) the signal transmission into the target channel in solid curves, and channel crosstalks in dotted and dashed curves, while the colors are output channel specific.

The simulated electric field patterns for three input modes are shown in Fig. 5.4 (a). TE0 mode is routed to bottom channel, and it does not go through any mode conversion. TE1 mode is routed to the top channel, while TE2 mode is routed to the middle channel, and these modes are converted to TE0 modes in their respective output waveguides. Fig. 5.4 (b) shows the expected performance, respective channel transmission and crosstalks into other channels, of this MDM. The signal transmission through every output channel, plotted in solid curves, is greater than 96% across the 100 nm wavelength span centered at 1.55 μm. The MDM shows good crosstalk performance as well, for every input mode, the XTs into other two channels are below -23 dB except for the XT of TE2 signal into channel 1, plotted in dotted and dashed curves. The FDTD simulation shows very optimistic performance of the optimized design.

In the optimized design in Fig. 5.3 (c), there are some discrete structures along the top and bottom edges away from the main silicon block at the center. In the simulated field patterns in Fig. 5.4 (a), very little optical field density is located in these discrete structures, which can be referred to as appendices. To quantify the contribution of these appendices to the overall performance of the MDM, additional simulations are performed removing these appendices. The MDM design without the appendices and its channel transmission and crosstalks are shown in Fig. 5.5. Since the discrete structures are located far from the main silicon block and very little optical field couples to them, removing the appendices makes a little difference to the MDM performance. To compare with the performance of the actual design, the crosstalk curves are plotted in the same figure in thin black curves. Overall, removing the appendices causes slightly higher XT in the bottom channel. Therefore, the discrete structures are retained when the layout was sent for fabrication.

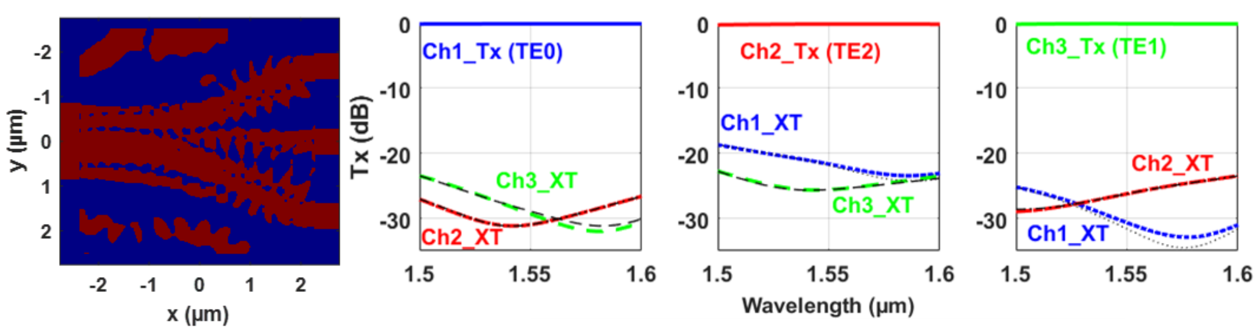


Fig. 5.5 The MDM design without the appendices and its cannel transmission and crosstalk performance. The black dotted and dashed curves are the crosstalks of the actual design.

Since the final design layout sent for fabrication contains small and sharp features, the electron beam lithography cannot realize identical structure. Sharp features are smoothed out, and the resulting structure deviates from the actual design, resulting in degradation of the performance. The SEM image of the fabricated MDM and its simulated performance are shown in Fig. 5.6. The average channel transmission decreases from 97.2% to 92% across the bandwidth of 1.5-1.6 μm. This change is not obvious in the transmission curves in Fig. 5.6 since they are calculated in the logarithmic scale. However, the change in the crosstalk performance is evident. Across the bandwidth, the average XT increases by 6 dB. The reduction in the channel transmission is responsible for this increased XT since more signal power leaked into the undesired channels.

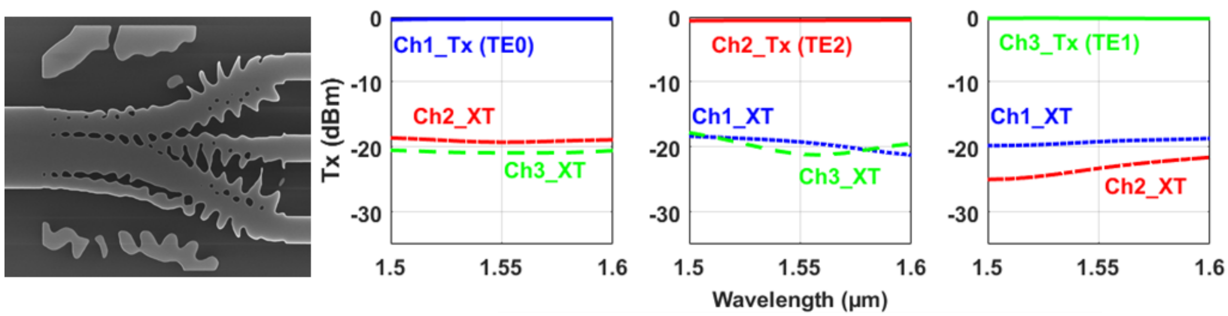


Fig. 5.6 The SEM image of the fabricated MDM on left. The FDTD simulation results of this SEM image are presented for three input modes. Transmission plots across the bandwidth of 1.5-1.6 μm and the channel crosstalks; the fabricated device exhibits ~6 dB increased average crosstalk than the actual design.

For the experimental characterization of the MDM, two MDMs are cascaded, one MDM flipped horizontally and connected by a common multimode waveguide. The design layout is fabricated at Applied NanoTools Inc (ANT). Below the experimental results are reported for the wavelength range of 1.5-1.58 μm. Similar to the mode converters reported in earlier chapters, the MDMs are optimized to operate in a wavelength range of 1.5-1.6 μm, but the fluctuations in the grating coupler transmission curve make the experimental data unreliable at the longer wavelength, beyond 1.58 μm to be specific. Therefore, the experimental data beyond 1.58 μm is not reported here. The experimental results show good agreement with the simulation results of the SEM image. The insertion loss varies between 0.1 dB and 1.5 dB, which is consistent with the measurement uncertainty (1.2 dB) of the grating coupler [31]. For the channel crosstalk, the experimental data shows some dips in the XT transmission curves which are caused by the interference effects due to back reflections in the grating couplers. The MDM experiences high channel XTs at the two ends of the reported bandwidth, but it has reasonably good performance in the C-band (1.53-1.565 μm) with worst crosstalk of -18 dB.

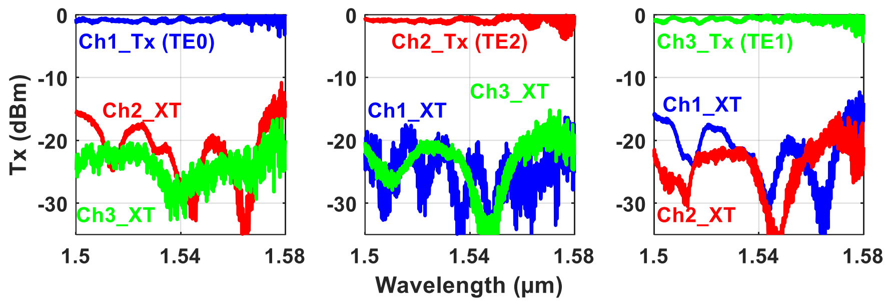


Fig. 5.7 Experimental characterization of the MDM. The insertion loss varies between 0.1 dB and 1.5 dB while the worst channels crosstalk is -14 dB.

5.3. Physics guided design approach

Previously, it was demonstrated that the mode conversion between a symmetric mode and an asymmetric mode is favored by incorporating a vertical offset between the I/O waveguides which facilitates the asymmetry in the design structure. Following that idea, when it came to designing the MDM, the output channel assignment to the input mode is not an arbitrary choice. For MDM1, reported in the previous section, the output assignment follows insight gained through the MCs, which suggests that TE1 to TE0 conversion is easier to achieve by routing it to either the top or bottom channel. Routing TE2 to the middle channel would be favorable, which lies on the same axis as the input waveguide. TE0 can be routed to any output channel since no mode conversion occurs to it. Specifically, the outputs are assigned in the following order: TE1, TE2, and TE0 from top to bottom. In the highly nonconvex design parameter space, the locations and magnitudes of the optima are determined by factors such as design area, I/O waveguides dimension and position, and channel assignment. It is expected that such intentional choice of output channels for the input modes would be favorable for obtaining good designs as well as efficient optimization of those.

To demonstrate this hypothesis, additional copies of 3-channel MDM are optimized. Here, a detailed discussion on another MDM (MDM2) is presented, which is optimized from the same initialization as that of MDM1 except for the output channel assignments. For MDM2 shown in Fig. 5.8 (d), the output channels are assigned in a sequential order, TE0 to TE2 from bottom to top. Despite the same initial parameters at the beginning of the optimization, the design structure of MDM2 turns out to be a very different from that of MDM1 simply because of the different channel assignment. Moreover, it took more iterations for MDM2 to converge to the final design, whereas the FOM of MDM1 reaches 98% within 100 iterations. Fig. 5.8 (a) shows MDM2 always lags behind MDM1, with a FOM of 90.6% at 100th iteration. Fig. 5.8 (b), (c), and (d) show the evolution of MDM2 design at 100th iteration, final optimized design at 516th iteration, and binarized design layout, respectively.

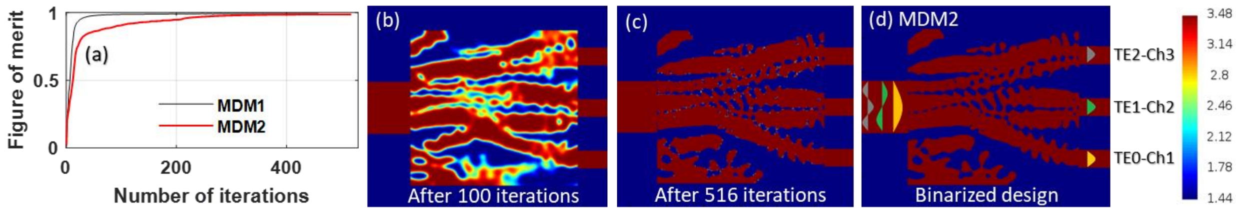


Fig. 5.8 (a) Figure of merit vs. number of iterations for MDM2 (red); for comparison, Fig. 5.2 (a) for MDM1 is regenerated with narrow black curve. It shows the optimization of MDM1 is way more efficient than that of MDM2. (b) The topology of MDM2 at 100th iteration, (c) final optimized design with less than 1% regions having intermediate permittivities, (d) binarized MDM2 design layout sent for fabrication.

The simulated electric filed distributions in MDM2 for different input modes are shown in Fig. 5.9 (a). The FDTD simulation results of the MDM2 binarized structure are plotted in Fig. 5.9 (b). Despite having good transmissions through each of the channels, channel 1 and channel 3 experience higher crosstalks from input optical signals in TE2 and TE1 modes, respectively. It is expected that after fabrication, the crosstalk performance would worsen.

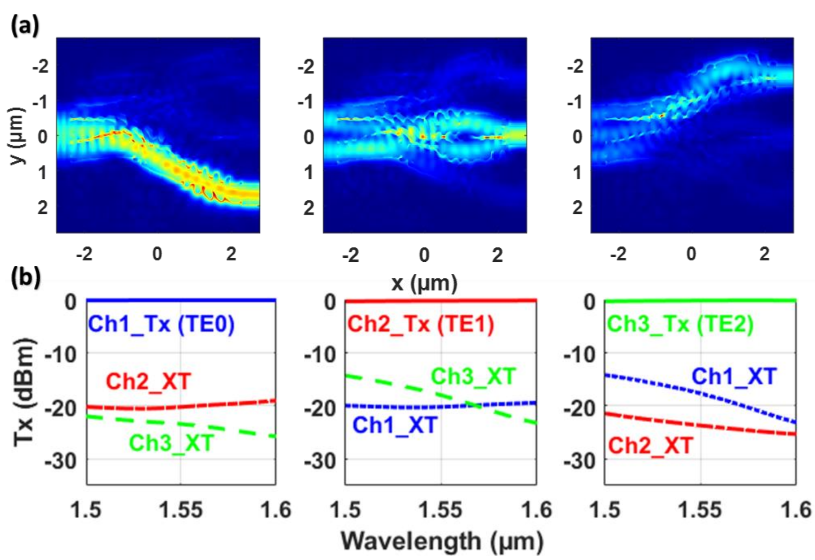


Fig. 5.9 (a) The simulated electric field pattern in MDM2 showing how different input modes are routed to different output channels, (b) FDTD simulation results of the binarized MDM2 design layout. Input

optical signals in TE1 and TE2 modes contribute to XTs in channel 3 and channel 1, respectively, as high as -14.2 dB at 1.5 µm wavelength.

Fig. 5.10 (a) shows the SEM image of the fabricated MDM2. The FDTD simulation results of the SEM image are plotted in Fig. 5.10 (b). It clearly shows increase in the insertion losses and significant degradation in the crosstalk performance. Across the bandwidth, the average channel transmission decreases by 11.6%, resulting in an increase in the average insertion loss from 0.2 dB to 0.74 dB, while average channel crosstalk increases by 4.1 dB. The experimental results are plotted in Fig. 5.10 (c), which shows good agreement with the simulation results of the SEM image taking the measurement uncertainty of the grating coupler into account.

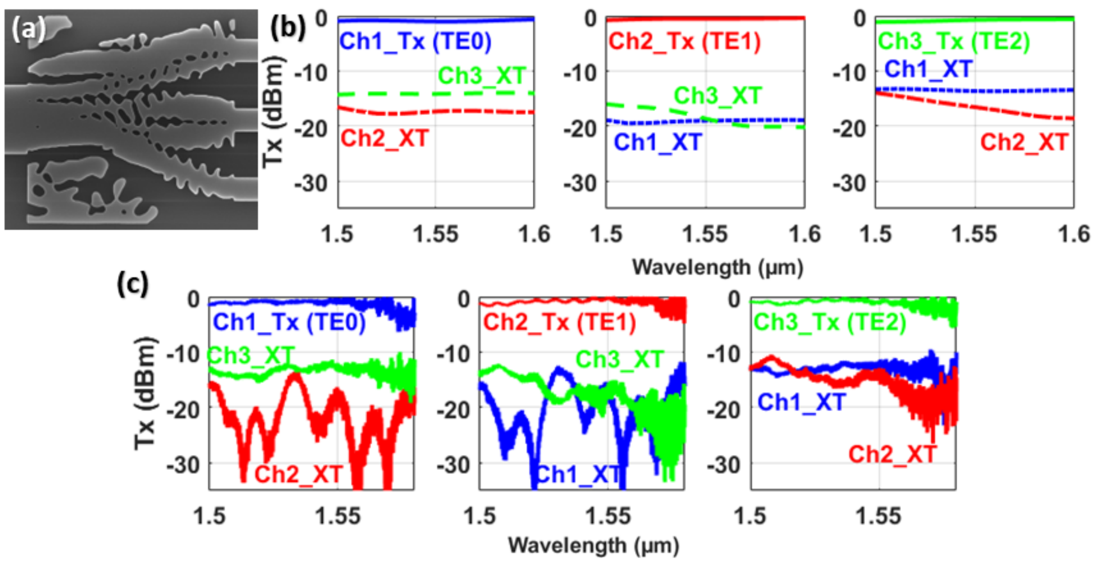
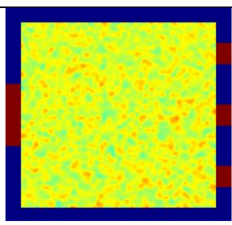
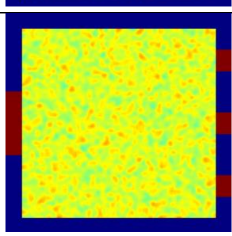
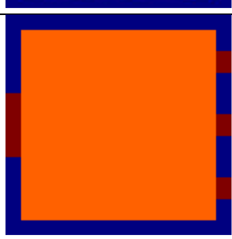


Fig. 5.10 (a) SEM image of MDM2, (b) the simulation results of the SEM image showing channel transmission and crosstalks, average transmission drops by 11.6% and average XT increases by 4.1 dB, (c) experimental data showing good agreement with the simulation results of the SEM image.

One pair of MDMs with identical initializations, except for the output channel assignment, are not sufficient to conclude the advantage of such physics guided design approach. To establish the idea, two additional pairs of 3-channel MDMs are optimized using 3D FDTD simulations, with the same design area dimension but different initial parameter values. The summary of their optimization convergence and important performance parameters are presented in table 5.1 which shows that the physics guided output channel assignment to the input modes indeed benefits from faster convergence to the final design, requiring fewer number of iterations than their counterparts, except for the last pair. Additionally, by comparing the average channel ILs and maximum XTs across the bandwidth of 1.5- 1.6 μm of the MDMs in each pair, physics guided designs offer better performance. However, it is important to acknowledge that to establish the hypothesis, an exhaustive search of all the good designs in the given design area needs to be performed. Additionally, the process needs to be repeated for smaller design footprint. The advantage of such intentional setup for the initialization of the optimization is expected to be more eminent for smaller design footprints, since increasing the design footprint always favors better performance.

Table. 5.1 Pairs of 3-channel MDMs optimized from the same initial parameters except for different output channel assignments. Their average channel insertion losses, maximum crosstalks, and number of iterations for convergence.

Initial parameters	Channel assignment 1[a]	Channel assignment 2[b]	Number of iterations to converge		Average IL (1.5-1.6 μm)	Maximum XT (1.5- 1.6 μm)
	✓		467	Ch1	0.11 dB	-18.8 dB
				Ch2	0.21 dB	-23.5 dB
				Ch3	0.14 dB	-22.8 dB
		✓	521	Ch1	0.15 dB	-14.2 dB
				Ch2	0.31 dB	-19.2 dB
				Ch3	0.30 dB	-14.3 dB
	✓		464	Ch1	0.19 dB	-21.6 dB
				Ch2	0.26 dB	-20.7 dB
				Ch3	0.23 dB	-18.9 dB
		✓	516	Ch1	0.22 dB	-18.4 dB
				Ch2	0.47 dB	-19.5 dB
				Ch3	0.27 dB	-17.1 dB
	✓		486	Ch1	0.28 dB	-22.4 dB
				Ch2	0.33 dB	-21.0 dB
				Ch3	0.18 dB	-18.3 dB
		✓	478	Ch1	0.21 dB	-19.6 dB
				Ch2	0.39 dB	-22.0 dB
				Ch3	0.26 dB	-19.5 dB

[a] Channel assignment 1: Ch1 (bottom) → TE0, Ch2 (middle) → TE2, Ch3 (top) → TE1
[b] Channel assignment 2: Ch1 (bottom) → TE0, Ch2 (middle) → TE1, Ch3 (top) → TE2

Chapter 6

Conclusion

In this thesis, three related projects have been conducted and reported:1) the design of mode converters in shape optimization method, 2) the development of a machine learning-based design parameter prediction model to reduce the computation cost involved in 3D optimization, and 3) the design of three-channel mode-division multiplexers.

MCs designed in conventional methods adopting asymmetric directional couplers, asymmetric Y-junctions, Bragg gratings, etc. usually have large footprints, few tens to several hundred microns. Therefore, these MCs are not suitable for dense integration of PICs. Micro ring resonator-based MCs are small in size but suffer from limited bandwidth and also sensitive to fabrication imperfections. Good designs of MC based on coherent scattering are obtainable in compact footprints. Conventional methods using tapered waveguides still results in few tens of microns long MCs. In this regard, computational optimization techniques such as genetic algorithm and inverse design has enabled device lengths below 10 μm. Since methods like direct binary search, genetic algorithm, topology optimization, are computationally expensive, a relatively simpler method, shape optimization, is employed in this work to design various MCs for TE modes. The same method can be used to design mode converters for TM polarization by carefully selecting the mode order in the optimization algorithm. The footprints of the MCs in this work range from 3 μm to 7.8 μm in length. The mode conversion efficiencies of the optimized designs are above 95% across 100 nm wavelength span centered at 1.55 μm based on 3D FDTD simulations. Experimental results show the maximum insertion loss is 1.2 dB across the wavelength range from 1.5 μm to 1.58 μm, while their modal crosstalks are below -19 dB in the

C-band. Due to the bandwidth limitation of the grating couplers used for interfacing with fibers, the measured results beyond 1.58 μm are deemed unreliable and, therefore, not reported. The design approach is formulated in such a way that the device structure consists of a single silicon block between the I/O waveguides, ensuring high confinement of the optical fields in Si core, which makes the designs robust to standard dimensional variations caused by the fabrication process. Despite introducing ±20 nm waveguide width variations, the mode conversion efficiency remains above 90% across the entire bandwidth of 1.5-1.6 μm. Over etching results in shrunk design structures, while under etching produces expanded structures. In simulations, the shrunk designs favor optical signals at shorter wavelengths, manifested by the peak mode conversion efficiency occurring at the shorter wavelength and increased crosstalk at longer wavelengths. Expanded designs just have the opposite effects. Experimentally, these observations are confirmed by the increased insertion loss and crosstalk at the longer wavelengths for the over-etched designs, and the opposite effects for the under-etched ones. Additionally, 28 Gbps OOK and 20 GBaud PAM-4 payload transmissions are performed for the time-domain characterization of the MCs. Open eye diagrams with a Q-factor around 8 dB are obtained, demonstrating the utility of these devices in high-speed optical communication systems.

The working mechanisms of the MCs are thoroughly investigated by studying the simulated electromagnetic field patterns in the design area and validated by simulation and experimental data. The insight into how the devices work turns out to be useful for formulating the design approach such that the performance can be enhanced without requiring additional design space. Moreover, it guides the designer to make smart choices for setting up the initial conditions of the optimization which are favorable for faster convergence as well as improved device performance. For the mode conversion between an anti-symmetric and symmetric modes, the asymmetry in the field scattering process requires asymmetric design geometry. By introducing a vertical offset between the I/O waveguide axes, more efficient designs are achieved. Similarly, the advantage of the intentional output channel assignment in the MDMs is not completely established yet because sufficient design samples could not be obtained due to time limitations. But, according to the small collection of MDMs, favorable results are found and reported.

Finally, the computation cost involved with most of the gradient-based optimization techniques is tremendous. When more than one performance parameters are optimized simultaneously, finding the right weight-coefficients of the objective terms often takes a lot of experimentation and tuning. Since gradient descent-based optimization techniques does not guarantee finding the global optimum (the best design obtainable), an exhaustive search for all the possible good designs is needed. Thus, it is highly desirable to find means to reduce the computation load for more efficient optimizations. Here, machine learning-based regression model is proposed which can predict the design parameters of the final 3D optimized designs. The structure formed by the predicted parameters is closer to the final design than the 2D optimized designs are. Using the predicted design parameters as the initialization of the 3D optimization, the number of iterations needed to converge to the final design is reduced, saving significant amount of time and computation. To demonstrate the idea, the TE0-TE1 MC is chosen because of its structural asymmetry and possibility of having many good solutions in the given design footprint (3.6 μm long). A dataset containing 59 MCs with an average CE above 90% across the bandwidth of 1.5-1.6 μm is built to conduct the study. 24 randomly picked designs are used to train a regression model to predict 15 design parameters defining the device structure. Then, the remaining 35 designs are used to test the regression model. Using the 2D optimized parameters of these 35 designs the regression-model predicts the 3D optimized parameters. Later, the predicted parameters are reoptimized to obtain the final designs, which takes 35% fewer number of iterations to reach the optima.

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