Noise-Shaping Enhancement in Continuous-Time Delta-Sigma Modulators

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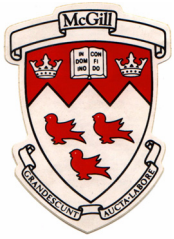

A thesis submitted to McGill University in partial fulfilment of the requirements of the degree of Master of Engineering

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ABSTRACT

A technique is presented for designing high-order continuous-time (CT) ΔΣ modulators with noise-transfer-function (NTF) enhancement. This enhancement is achieved by injecting the quantization noise into the forward path of the CT ΔΣ modulator, through a passive CT filter. This passive filter introduces a real pole-zero pair into the NTF. Thus, the order of the NTF is increased, without affecting the signal transfer function (STF). The proposed NTF-enhancement technique is applied to a CT ΔΣ modulator with a capacitive-feedforward architecture, where all feedforward paths are summed within the last integrator of the ΔΣ loop filter. This eliminates the need for an analog summation amplifier at the output of the ΔΣ loop filter. Behavioral and circuit-level simulation results confirm that the proposed feedforward CT ΔΣ modulator with NTF enhancement has improved noise-shaping and stability characteristics, as compared to classical CT ΔΣ modulators.

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RÉSUMÉ

Une technique est présentée pour la conception du modulateur ΔΣ en temps continu (CT) ordre-haut avec amélioration de la fonction de transfert du bruit (NTF). Cette amélioration est obtenue par injection du bruit de quantification dans la chemin feedforward du modulateur ΔΣ CT, via un filtre passif CT. Ce filtre passif introduit une paire de pôle-zéro réel dans la NTF. Donc, l'ordre de la NTF est augmenté, sans affecter la fonction de transfert du signal (STF). La technique proposé pour l'amélioration de la NTF est appliquée à un modulateur ΔΣ CT avec une architecture feedforward-capacitive, où tous les chemins feedforward sont ajoutée dans le dernier intégrateur du filtre de boucle ΔΣ. Ceci élimine la nécessité d'un amplificateur de sommation analogique à la sortie du filtre de boucle ΔΣ. Les résultats de simulation du comportement et niveau circuit confirment que la proposition du modulateur ΔΣ CT feedforward avec amélioration de la NTF a permis d'améliorer le bruit-façonnement et les caractéristiques de stabilité, par rapport aux modulateurs ΔΣ CT classiques.

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Chapter 1

Introduction

1.1 Overview

Continuous-time (CT) ΔΣ modulators (Fig. 1.1a) have recently gained popularity over their discrete-time (DT) counterparts, owing to their potential for low-power high-speed A/D conversion [Huang, ISSCC09] [Yang, ISSCC08] [Mitteregger, JSSC06], suppression of sampling errors, and implicit anti-aliasing filtering [Peev, ICECS08] [Keller, TCASI07]. However, their principal disadvantages are their high sensitivity to clock jitter [Chopp, TCASI09] [Reddy, TCASI07] and their need for tuning circuitry.

Noise-transfer-function (NTF) enhancement is a technique for improving the noise-shaping performance of a ΔΣ modulator, without using additional integrators in its ΔΣ loop filter and without affecting its signal transfer function (STF). This enhancement is achieved by injecting the quantization noise into the forward path of the ΔΣ modulator through an NTF-enhancement filter $G(s)$, as depicted in Fig. 1.1b. This filter introduces a real pole-zero pair into the NTF, such that the order of the NTF is increased (Chapter 2). The advantage of this technique is that the noise-shaping performance of a ΔΣ modulator can be enhanced, with: a) minimal increase in power dissipation due to an additional D/A converter (DAC), if the NTF-enhancement filter $G(s)$ and the sample-and-hold (S&H) in Fig. 1.1b can be implemented using only additional passive elements, as proposed in this thesis (Chapter 3); and b) the maximum stable input is maintained at its level before NTF enhancement (i.e., the modulator stability is not degraded by the NTF enhancement

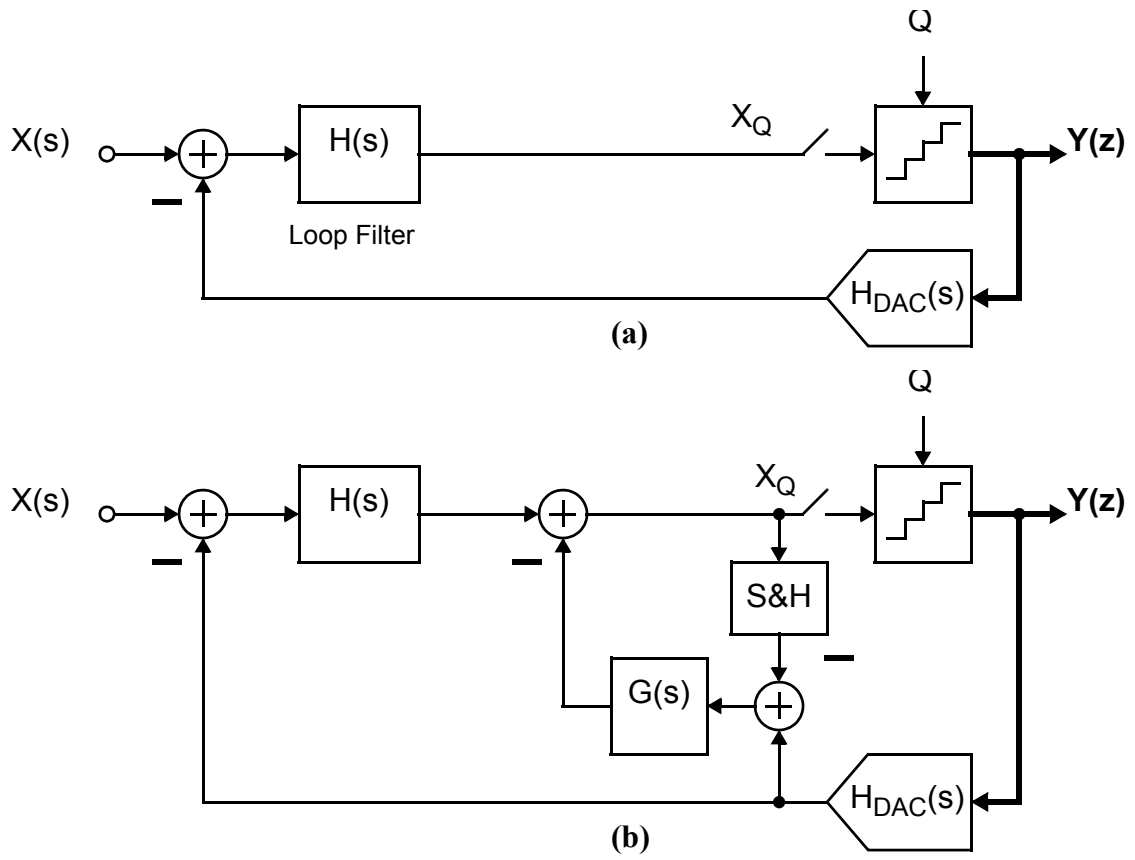

Figure 1.1 Block diagram of **(a)** a classical CT ΔΣ modulator; and **(b)** a CT ΔΣ modulator with NTF enhancement.

[Lee, ICECS06] [Lee, CICC08]). Furthermore, when applied to CT ΔΣ modulators, NTF enhancement can relax the requirements on the accuracy of the tuning circuitry (Chapter 3). In this thesis, the NTF-enhancement technique is developed for CT ΔΣ modulators using passive CT filters, thus increasing their potential for low-power A/D conversion.

The CT loop filter $H(s)$ in Fig. 1.1b can be implemented using a chain of integrators with feedback or feedforward compensation [Cherry 00]. Assuming an active-RC implementation, the feedback-compensation coefficients are realized using *RC* time constants in the feedback topology, while the feedforward-compensation coefficients are implemented as ratios of resistors or capacitors in the feedforward architecture. In standard digital CMOS technologies, capacitor and resistor ratios can be accurate to ±0.1%, while *RC* products can vary up to around ±30%

[Johns 97]. Thus, feedforward architectures enable more accurate control over the modulator coefficients. Furthermore, feedforward architectures reduce the signal component at the output of the loop-filter integrators, thus reducing the modulator sensitivity to integrator nonlinearities [Steensgaard, ICECS98]. However, to sum the feedforward paths in a ΔΣ modulator with feedforward architecture, an analog summation amplifier is required at the output of the ΔΣ loop filter.

This thesis develops a technique for NTF enhancement in CT ΔΣ modulators with a feedforward architecture, where all feedforward paths [Schimper, ESSCIRC04] and the excess-loop-compensation feedback path [Mitteregger, JSSC06] are summed within the last integrator of the ΔΣ loop filter, thereby eliminating the need for an analog summation amplifier at the output of the ΔΣ loop filter. This NTF enhancement is implemented using passive elements, sampling switches, and a DAC (realized using digital inverters). Thus, it requires minimal additional power dissipation.

1.2 Thesis Outline

This work is divided as follows:

Chapter 2: NTF-Enhancement in CT ΔΣ Modulators

This chapter explains the fundamental concepts of NTF-enhancement, which can be used to increase the noise-shaping performance of ΔΣ modulators. The technique for NTF-enhancement in DT ΔΣ Modulators is adapted for CT implementations. It describes how different types of NTFs (FIR and Butterworth NTFs) can be enhanced using the proposed technique. Furthermore, it discusses the implementation of NTF-enhancement using passive elements for low-power implementation.

Chapter 3: Realization of the NTF Enhancement in CT ΔΣ Modulators

This chapter describes an architecture for CT ΔΣ modulators that employs capacitive feedforward paths, which can yield low-power implementations and provides improved control over feedforward coefficients. The proposed CT ΔΣ modulator integrates NTF-enhancement within this feedforward architecture for improved noise-shaping performance. Circuit-level schematics are provided to map mathematical models onto an actual circuit implementation.

Chapter 4: Behavioral Simulation of CT ΔΣ Modulators with NTF Enhancement

System-level optimizations (e.g. dynamic-range scaling) and non-idealities such as thermal noise and clock jitter etc. are included into the design for more accurate modeling. SIMULINK models are provided for the opamps used to implement the CT integrators of the ΔΣ modulator as well as models for the proposed NTF-enhanced 2^{nd}-order CT ΔΣ modulator. Behavioral simulations are used to confirm the noise-shaping improvement and stability advantage and studies the effects of opamp non-idealities.

Chapter 5: NTF-Enhanced 2nd Order CT ΔΣ Modulator Implementation

This chapter provides a detailed description of the various circuit components needed to implement the proposed NTF-enhanced 2^{nd}-order CT ΔΣ modulator, such as opamps, comparators and current-steering DACs. SPICE simulation results confirm circuit functionality for the proposed CT ΔΣ modulator with capacitive feedforward architecture and NTF enhancement, designed for 12-bit SNDR resolution over 1.1-MHz bandwidth. The circuits are implemented in 1-V, 65-nm CMOS technology.

Chapter 6 Conclusion

This chapter summarizes the work presented in this thesis and highlights the research contribution.

Chapter 2

NTF Enhancement in CT ΔΣ Modulators

Noise-transfer-function (NTF) enhancement is a technique for increasing the noise-shaping performance of a ΔΣ modulator, without using additional integrators in its ΔΣ loop filter and without affecting its signal transfer function (STF). The advantage of this technique is that the noise-shaping performance of a ΔΣ modulator can be enhanced, with:

a) minimal increase in power dissipation, if the NTF-enhancement can be implemented using only passive elements and an additional D/A converter (DAC), as proposed in this thesis (Chapter 3);

b) the maximum stable input is maintained at its level before NTF enhancement (i.e., the modulator stability is not degraded by the NTF enhancement [Lee, ICECS06]); and

c) when applied to CT ΔΣ modulators, NTF enhancement can relax the requirements on the accuracy of the tuning circuitry (Chapter 3).

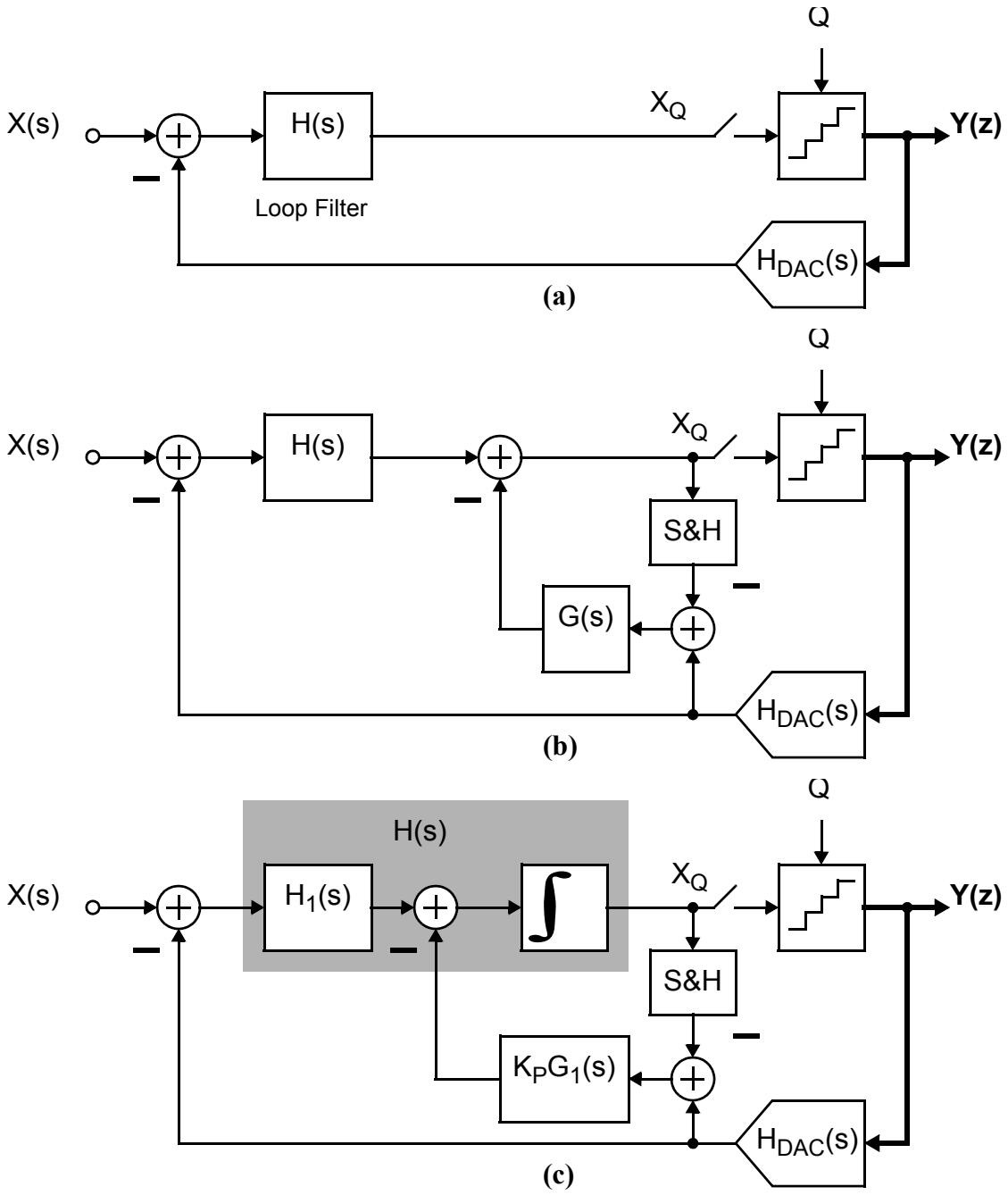

Figure 2.1 Block diagram of: **(a)** a classical CT ΔΣ modulator; **(b)** a CT ΔΣ modulator with NTF enhancement; and **(c)** the proposed simplified realization of the ΔΣ modulator in (b). Here, $\int \equiv 1/(sT_S)$.

2.1 NTF Enhancement

Consider the classical CT ΔΣ modulator modeled in Fig. 2.1a. Define an equivalent DT loop filter:

$$H_{eq}(z) \equiv IIT\{H(s)H_{DAC}(s)\} \equiv Z\left\{ L^{-1}\{H(s)H_{DAC}(s)\}\Big|_{t = nT_S} \right\} \tag{2.1}$$

where $IIT\{.\}$ denotes the impulse-invariant transform, while $Z\{.\}$ and $L\{.\}$ denote the Z transform and Laplace transform, respectively. Here, $T_S = 1/f_S$ is the sampling-clock period, and f_S is the sampling frequency. The output of the CT ΔΣ modulator (Fig. 2.1a) can then be expressed as:

$$Y(z) = [STF(s)X(s)]^* + NTF(z)Q(z) \tag{2.2}$$

where [.]* denotes the sampling operation, as defined in [De Mayer, TCASI07]. Here, the noise and signal transfer functions of the CT ΔΣ modulator (Fig. 2.1a) are, respectively, defined as:

$$NTF(z) \equiv \frac{Y(z)}{Q(z)}\Bigg|_{X(s) = 0} = \frac{1}{1 + H_{eq}(z)} \tag{2.3}$$

$$STF(s) \equiv \frac{Y(e^{sT_S})}{X(s)}\Bigg|_{Q(z) = 0} = \frac{H(s)}{1 + H_{eq}(e^{sT_S})} \tag{2.4}$$

To increase the NTF order without affecting the STF, the quantization noise $Q(z)$ can be injected into the forward path of the CT ΔΣ modulator, as in Fig. 2.1b. Thus, the output of the CT ΔΣ modulator with NTF enhancement (Fig. 2.1b) becomes:

$$Y(z) = [STF(s)X(s)]^* + G_{eq}(z)NTF(z)Q(z) \tag{2.5}$$

where

$$G_{eq}(z) \equiv IIT\{1 - G(s)H_{DAC}(s)\} \tag{2.6}$$

Here, to increase the order of the modulator's noise-shaping characteristics by 1, the NTF-enhancement factor $G_{eq}(z)$ can be designed such that it introduces an additional zero at dc ($z = 1$) and a real pole z_p into the NTF:

$$G_{eq}(z) \equiv IIT\{1 - G(s)H_{DAC}(s)\} = \frac{1 - z^{-1}}{1 - z_p z^{-1}} \tag{2.7}$$

Assume that the feedback digital-to-analog converter (DAC) is effectively a zero-order hold:

$$H_{DAC}(s) = \frac{e^{-s\alpha T_S} - e^{-s\beta T_S}}{s} \tag{2.8}$$

where, α and β are the normalized start and end times of the rectangular DAC pulses [Cherry 00]. Substituting (2.8) into (2.7) and taking a $z \to s$ impulse-invariant transform results in an equivalent CT NTF-enhancement filter:

$$G(s) = \frac{K_p}{sT_S - s_p} \tag{2.9}$$

where

$$s_p \equiv \ln(z_p) \quad \text{and} \quad K_p \equiv \frac{(1-z_p)\ln(z_p)}{(z_p^{\,1-\alpha} - z_p^{\,1-\beta})} \tag{2.10}$$

Accordingly, the required NTF-enhancement filter $G(s)$ is merely a CT low-pass filter.

2.1.1 Realizing the NTF Enhancement using Passive Filters

The realization of the NTF enhancement in Fig. 2.1b is complicated by the need for an additional summation amplifier at the output of the loop filter $H(s)$. For ease of implementation, the NTF-enhanced CT ΔΣ modulator in Fig. 2.1b can be re-designed as proposed in Fig. 2.1c, with the output of the NTF-enhancement filter added to the input of the last integrator (Integ. 1) in the loop filter $H(s)$. Then, the output of the CT ΔΣ modulator with NTF enhancement (Fig. 2.1c) can be expressed as:

$$Y(z) = [STF(s)X(s)]^* + G_{eq1}(z)NTF(z)Q(z) \tag{2.11}$$

where

$$G_{eq1}(z) \equiv IIT\left\{1 - \frac{K_p}{sT_S}G_1(s)H_{DAC}(s)\right\} \tag{2.12}$$

To increase the order of the modulator's noise-shaping characteristics by 1, the NTF-enhancement factor $G_{eq1}(z)$ in (2.12) can be designed equal to $G_{eq}(z)$ in (2.7):

$$G_{eq1}(z) \equiv IIT\left\{1 - \frac{K_p}{sT_S}G_1(s)H_{DAC}(s)\right\} = \frac{1-z^{-1}}{1-z_p\,z^{-1}} \tag{2.13}$$

Substituting (2.8) into (2.13) and taking a $z \to s$ impulse-invariant transform results in an equivalent CT NTF-enhancement filter:

$$G_1(s) = \frac{sT_S}{sT_S - s_p} \tag{2.14}$$

where s_p and K_p are as defined in (2.10).

Accordingly, $G_1(s)$ is a passive CT filter. As described in Chapter 3, its circuit implementation, together with the summation blocks at its input and output (Fig. 2.1c), can be incorporated into the last integrator of loop filter $H(s)$ and, hence, explicit summation amplifiers are not needed.

2.1.2 High Order NTF Enhancement

As proposed in this thesis, enhancing the order of an NTF by one (i.e., 1st-order NTF enhancement) is attractive, as it requires introducing one real pole-zero pair in the NTF. Therefore, it can be implemented using passive filters and, hence, with minimal additional power dissipation.

Enhancing the order of an NTF by more than one (i.e., high-order NTF enhancement) is also feasible. However, it requires introducing multiple pole-zero pairs in the NTF, which cannot be implemented using passive filters. Therefore, high-order NTF enhancement is not attractive, because its implementation requires additional active filters and, hence, can significantly increase the power dissipation.

2.2 Design of the NTF-Enhancement Filter

2.2.1 Enhancement of an FIR NTF

Consider an N^{th}-order finite-impulse-response (FIR) NTF with its zeros at dc ($z = 1$):

$$NTF_N(z) = (1 - z^{-1})^N \tag{2.15}$$

Note that, in this thesis, the subscript N in $NTF_N(z)$ is used to denote the order of the NTF. To increase the order of this FIR NTF by one, the NTF-enhancement factor in (2.12) must be selected as:

$$G_{eq1}(z) = 1 - z^{-1} \tag{2.16}$$

However, this requires setting pole z_p of $G_{eq1}(z)$ at $z = 0$ in (2.13), which implies setting pole $s_p f_S$ of $G_1(s)$ in (2.14) at, ideally, $s_p = \lim_{z_p \to 0} \ln(z_p) = -\infty$. Therefore, for a practical implementation of NTF-enhancement filter $G_1(s)$, a practical range for s_p must be determined.

The normalized[1] single-sided inband quantization-noise power at the output of the ΔΣ modulator with a classical NTF of $NTF(z)$ and an enhanced NTF of $G_{eq1}NTF(z)$ can be expressed, respectively, as:

$$P_Q = \int_0^{f_S/(2OSR)} \left|NTF(z)\right|^2_{|\, z = e^{j2\pi f/f_S}} df \qquad \text{Classical NTF} \tag{2.17}$$

and

$$P_Q = \int_0^{f_S/(2OSR)} \left|G_{eq1}(z)NTF(z)\right|^2_{|\, z = e^{j2\pi f/f_S}} df \qquad \text{Enhanced NTF} \tag{2.18}$$

where OSR is the oversampling ratio of the ΔΣ modulator and, based on (2.13) - (2.14), the NTF-enhancement factor is:

$$G_{eq1}(z) = \frac{1 - z^{-1}}{1 - z_p z^{-1}} \tag{2.19}$$

where

$$z_p = e^{s_p} \tag{2.20}$$

and $s_p f_S$ is the location of the pole of $G_1(s)$ in (2.14).

Figure 2.2a depicts the effect of the pole $s_p f_S$ on the inband quantization-noise power P_Q for a ΔΣ modulator with an *enhanced* 2nd-order FIR NTF $G_{eq1}(z)NTF_2(z)$ versus a ΔΣ modulator with a *classical* 3rd-order FIR NTF $NTF_3(z)$. Accordingly, for $s_p < -2.5$, the signal-to-quantization-noise ratio (SQNR) of the ΔΣ modulator with an enhanced 2nd-order FIR NTF will

[1] For comparison, the quantization error is assumed to have a normalized root-mean-square power: $Q_{rms}^{\ 2} = 1$.

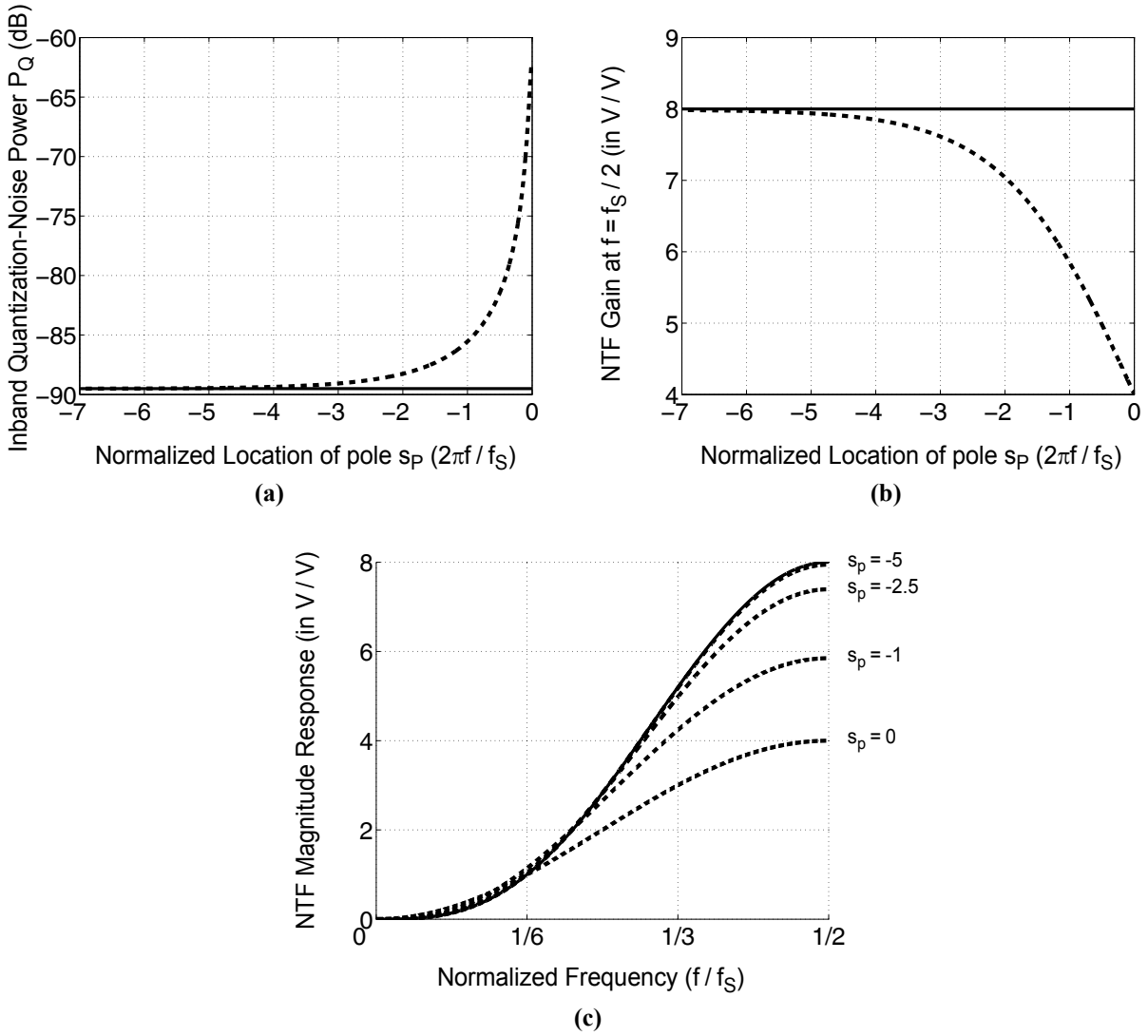

Figure 2.2 Effect of the location of pole $s_p f_S$ of the NTF-enhancement filter $G_1(s)$ on: **(a)** the inband quantization-noise power P_Q; **(b)** the NTF gain at $f = f_S/2$ (i.e., at $z = e^{j\pi}$); and **(c)** the magnitude response of the NTF for a ΔΣ modulator with an *enhanced* 2nd-order FIR NTF (**dashed lines - - -**) versus a ΔΣ modulator with an *classical* 3rd-order FIR NTF (**solid lines ——**). OSR = 8.

deviate by about only 1 dB from its ideal value (when $s_p \to -\infty$) or, equivalently, from the SQNR of the ΔΣ modulator with a classical 3rd-order FIR NTF. Therefore, the value of s_p does not have a significant effect on the achievable SQNR, provided that $s_p < -2.5$. As discussed in Chapter 3, the realizable value of s_p is limited by the unity-gain frequency f_T of the opamp in the last integrator of the ΔΣ loop filter.

Figure 2.2b depicts the effect of the pole $s_p f_S$ on the gain of the NTF at $f = f_S/2$ (i.e., at $z = e^{j\pi}$) for the enhanced 2nd-order FIR NTF (i.e., $\left|G_{eq1}(e^{j\pi})NTF_2(e^{j\pi})\right|$) and for the classical 3rd-order FIR NTF (i.e., $\left|NTF_3(e^{j\pi})\right|$). Accordingly, for $s_p < 0$, $\left|G_{eq1}(e^{j\pi})NTF_2(e^{j\pi})\right| \le \left|NTF_3(e^{j\pi})\right|$. Therefore, the location of the pole $s_p f_S$ will not cause the out-of-band gain of an enhanced N^{th}-order FIR NTF to exceed that of a classical $(N+1)^{\text{th}}$-order FIR NTF and, hence, will not cause any instability of the ΔΣ modulator with the enhanced NTF. Figure 2.2c plots the magnitude response of the enhanced 2nd-order FIR NTF and that of the classical 3rd-order FIR NTF for various s_p, thereby confirming that maximum quantization-noise suppression is achieved when $s_p < -2.5$, without destabilizing the NTF-enhanced ΔΣ modulator (assuming that the equivalent classical $(N+1)^{\text{th}}$-order ΔΣ modulator is stable).

2.2.2 Enhancement of a Butterworth NTF

A Butterworth NTF is defined as:

$$NTF_N(z) \equiv \frac{K_0(1-z^{-1})^N}{D(z)} \tag{2.21}$$

$$D(z) = \begin{cases} \displaystyle\prod_{k=1}^{N/2}(1-z_k z^{-1})(1-z_k^* z^{-1}) & , N = \text{even} \\ (1-z_0 z^{-1})\displaystyle\prod_{k=1}^{(N-1)/2}(1-z_k z^{-1})(1-z_k^* z^{-1}) & , N = \text{odd} \end{cases} \tag{2.22}$$

where the real pole z_0 and the complex-conjugate poles z_k and z_k^* are set using standard Butterworth functions, and the gain K_0 is a normalizing factor.

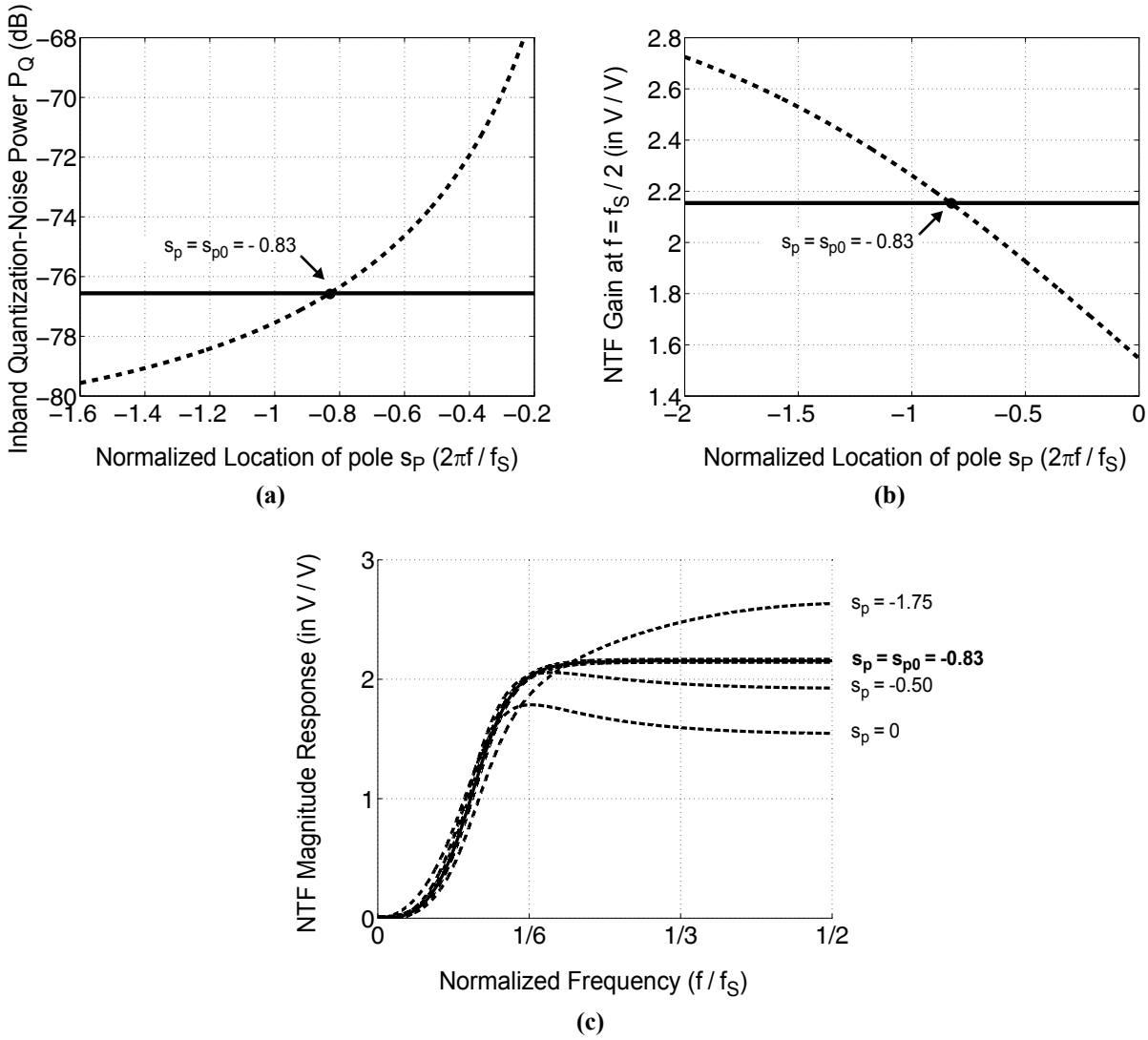

Figure 2.3 Effect of the location of pole $s_p f_S$ of the NTF-enhancement filter $G_1(s)$ on: **(a)** the inband quantization-noise power P_Q; **(b)** the NTF gain at $f = f_S/2$ (i.e., at $z = e^{j\pi}$); and **(c)** the magnitude response of the NTF for a ΔΣ modulator with an *enhanced* 2nd-order Butterworth NTF (**dashed lines - - -**) versus a ΔΣ modulator with an *classical* 3rd-order Butterworth NTF (**solid lines ——**). OSR = 8.

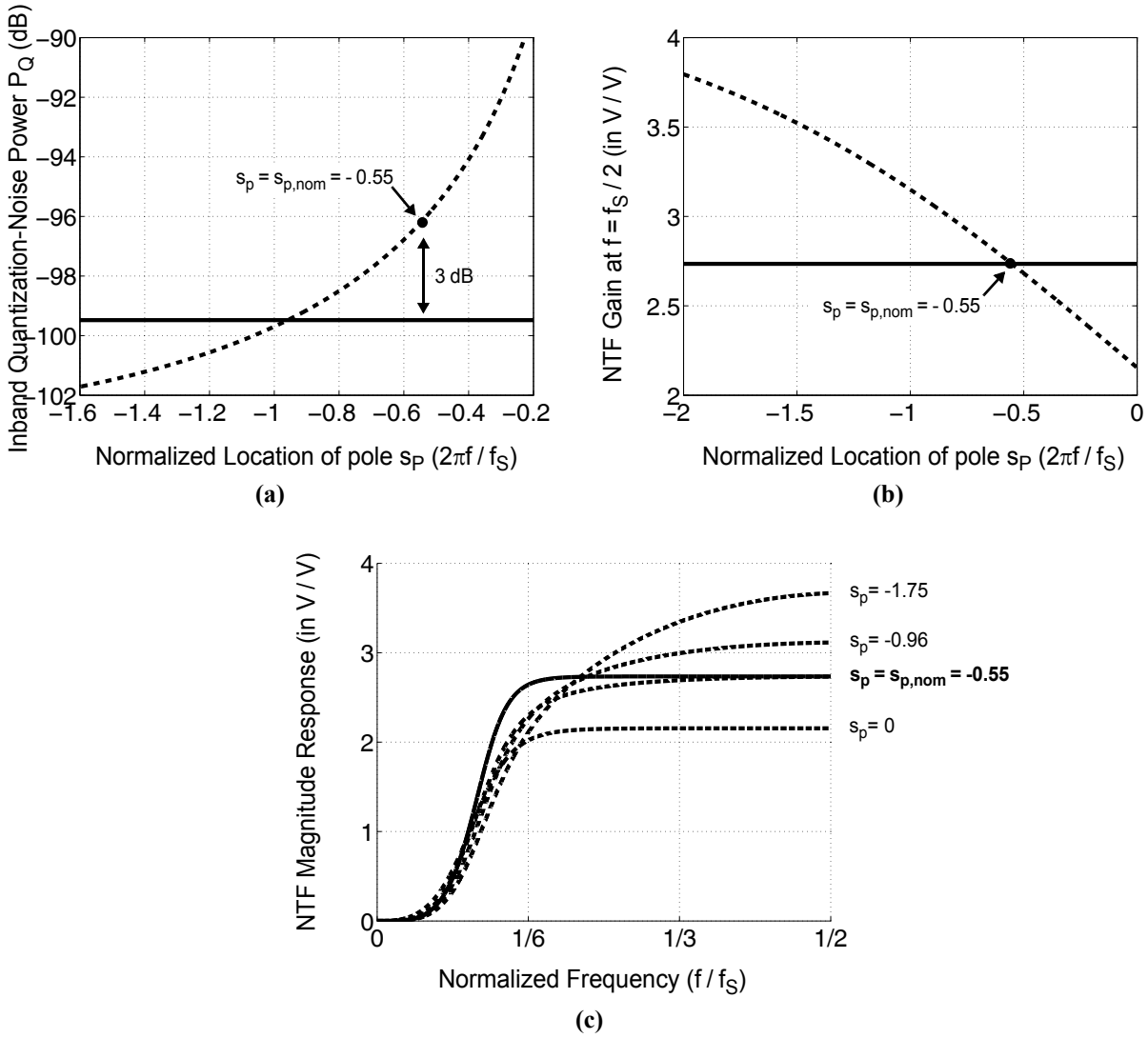

Figure 2.4 Effect of the location of pole $s_p f_S$ of the NTF-enhancement filter $G_1(s)$ on: **(a)** the inband quantization-noise power P_Q; **(b)** the NTF gain at $f = f_S/2$ (i.e., at $z = e^{j\pi}$); and **(c)** the magnitude response of the NTF for a ΔΣ modulator with an *enhanced* 3rd-order Butterworth NTF (**dashed lines - - -**) versus a ΔΣ modulator with an *classical* 4th-order Butterworth NTF (**solid lines ——**). OSR = 8.

The NTF-enhancement filter $G_1(s)$ in (2.14) can also be utilized to enhance the noise-shaping characteristics of a CT ΔΣ modulator with a Butterworth NTF. The procedure below is followed to enhance an N^{th}-order Butterworth NTF:

b) When N is even:

1. Start with an $(N+1)^{\text{th}}$-order Butterworth NTF in (2.21).
2. Remove the pole on the real axis z_0 and one of the zeros at dc from the NTF in step 1, in order to form an N^{th}-order NTF.
3. Design the proposed feedforward CT ΔΣ modulator in Fig. 2.1c, using N integrators in its loop filter $H(s)$ to implement the N^{th}-order NTF in step 2.
4. To enhance the N^{th}-order NTF of the ΔΣ modulator in step 3, set the pole of its NTF-enhancement filter $G_1(s)$ in (2.14) at $s_p f_S = s_{p0} f_S$, where $s_{p0} = \ln(z_0)$ and z_0 is the pole removed in step 2.

This is illustrated in Fig. 2.3 for an enhanced 2nd-order Butterworth NTF (OSR = 8). In Fig. 2.3a, the inband quantization-noise power P_Q is plotted versus s_p for the enhanced 2nd-order Butterworth NTF and for the classical 3rd-order Butterworth NTF. In Fig. 2.3b, the gain at $f = f_S/2$ of the enhanced 2nd-order Butterworth NTF (i.e., $\left|G_{eq1}(e^{j\pi})NTF_2(e^{j\pi})\right|$) and that of the classical 3rd-order Butterworth NTF (i.e., $\left|NTF_3(e^{j\pi})\right|$) are plotted versus s_p. Observe that the intersection of the curves in Fig. 2.3a and Fig. 2.3b (i.e., when the classical and the enhanced NTFs have the same P_Q and the same gain at $f_S/2$) corresponds to $s_p = s_{p0}$. Accordingly, for $N = 2$, $s_{p0} = -0.83$. Figure 2.3c, plots the magnitude response of the enhanced 2nd-order Butterworth NTF and that of the classical 3rd-order Butterworth NTF for various s_p, thereby confirming that the magnitude responses of both NTFs are identical at $s_p = s_{p0}$.

b) When N is odd:

1. Start with an N^{th}-order Butterworth NTF in (2.21).
2. Design the proposed feedforward CT ΔΣ modulator in Fig. 2.1c, using N integrators in its loop filter $H(s)$ to implement the N^{th}-order NTF in step 1.

3. To enhance the N^{th}-order NTF of the ΔΣ modulator in step 2, set the pole of its NTF-enhancement filter $G_1(s)$ in (2.14) at $s_p f_S = s_{p,\,nom} f_S$. Here, $s_{p,\,nom}$ is defined as the nominal value of s_p, that results in the enhanced N^{th}-order NTF (i.e., $\left|G_{eq1}(e^{j\pi})NTF_N(e^{j\pi})\right|$) having the same gain as its equivalent classical $(N+1)^{\text{th}}$-order NTF (i.e., $\left|NTF_{N+1}(e^{j\pi})\right|$) at $f = f_S/2$ (i.e., at $z = e^{j\pi}$):

$$s_{p,\,nom} \equiv s_p\Big|_{\left|G_{eq1}(e^{j\pi})NTF_N(e^{j\pi})\right| = \left|NTF_{N+1}(e^{j\pi})\right|} \tag{2.23}$$

Observe that, when N is even, $s_{p,\,nom}$ corresponds to s_{p0}. When N is odd, setting $s_p = s_{p,\,nom}$ ensures that the out-of-band gain of the enhanced N^{th}-order Butterworth NTF matches that of a classical $(N+1)^{\text{th}}$-order Butterworth NTF and, thus, maximum quantization-noise suppression is achieved without destabilizing the NTF-enhanced ΔΣ modulator (assuming that the equivalent classical $(N+1)^{\text{th}}$-order ΔΣ modulator is stable). However, contrary to the case when N is even, this will not result in an enhanced N^{th}-order NTF with a magnitude response that is identical to that of a classical $(N+1)^{\text{th}}$-order NTF. This is because the proposed NTF-enhancement technique in Section 2.1 can only introduce a real pole (namely, $s_p f_S$) into the NTF, whereas a complex-conjugate pole is needed to perfectly enhance an odd-order Butterworth NTF. Yet, using a real pole to enhance an odd-order Butterworth NTF (as proposed here) is sufficient to significantly improve the inband quantization-noise power P_Q of its ΔΣ modulator. This is illustrated in Fig. 2.4 for an enhanced 3rd-order Butterworth NTF (with OSR = 8). In Fig. 2.4a, the inband quantization-noise power P_Q is plotted versus s_p for the enhanced 3rd-order Butterworth NTF and for the classical 4th-order Butterworth NTF. In Fig. 2.4b, the gain at $f = f_S/2$ of the enhanced 3rd-order Butterworth NTF (i.e., $\left|G_{eq1}(e^{j\pi})NTF_3(e^{j\pi})\right|$) and that of the classical 4th-order Butterworth NTF (i.e., $\left|NTF_4(e^{j\pi})\right|$) are plotted versus s_p. Observe that the intersection of the curves in Fig. 2.4b (i.e., when the classical and the enhanced NTFs have the same gain at $f_S/2$) corresponds to $s_p = s_{p,\,nom}$. Accordingly, for $N = 3$, $s_{p,\,nom} = -0.55$. Observe that, although, at $s_p = s_{p,\,nom}$, the inband quantization-noise power P_Q of the enhanced 3rd-order Butterworth NTF is larger than that of the classical 4th-order Butterworth NTF (by 3dB in Fig. 2.4a), a 19 dB decrease in P_Q is still achieved through the proposed NTF-enhancement technique: P_Q = -77 dB for the classical 3rd-order Butterworth NTF in

Fig. 2.3a, while $P_Q = -96$ dB for the enhanced 3rd-order Butterworth NTF in Fig. 2.4a at $s_p = s_{p,nom}$. Figure 2.4c plots the magnitude response of the enhanced 3rd-order Butterworth NTF and that of the classical 4th-order Butterworth NTF for various s_p, thereby confirming that the magnitude responses of both NTFs have equal out-of-band gains at $s_p = s_{p,nom}$. In summary, when N is odd, although the inband quantization-noise power P_Q of an enhanced N^{th}-order Butterworth NTF is not as low as that of a classical $(N+1)^{th}$-order Butterworth NTF, it is still significantly lower than that of a classical N^{th}-order Butterworth NTF. Furthermore, the NTF-enhanced N^{th}-order $\Delta\Sigma$ modulator has the same stability characteristics as the classical N^{th}-order $\Delta\Sigma$ modulator.

Chapter 3

Realization of the NTF Enhancement in CT ΔΣ Modulators

This chapter presents the design of CT ΔΣ modulators with a feedforward architecture where all feedforward paths are summed within the last integrator, thereby eliminating the need for an analog summation amplifier at the quantizer input. Furthermore, noise-shaping enhancement and excess-loop-delay compensation are integrated into the proposed feedforward ΔΣ modulator architecture.

3.1 Architecture of the Proposed CT ΔΣ Modulator with NTF Enhancement

Consider the classical N^{th}-order feedforward CT ΔΣ modulator in Fig. 3.1a. Its loop filter can be expressed as:

$$H(s) = \frac{K_N(sT_S)^{N-1} + \ldots + K_2 sT_S + K_1}{(sT_S)^N} \tag{3.1}$$

The equivalent DT representation of $H(s)$ in (3.1) has the general form:

$$H_{eq}(z) = \frac{a_N z^{-N}}{(1-z^{-1})^N} + \ldots + \frac{a_2 z^{-2}}{(1-z^{-1})^2} + \frac{a_1 z^{-1}}{(1-z^{-1})} \tag{3.2}$$

Therefore, the feedforward CT ΔΣ modulator architecture in Fig. 3.1a can be utilized to implement an N^{th}-order NTF of the form:

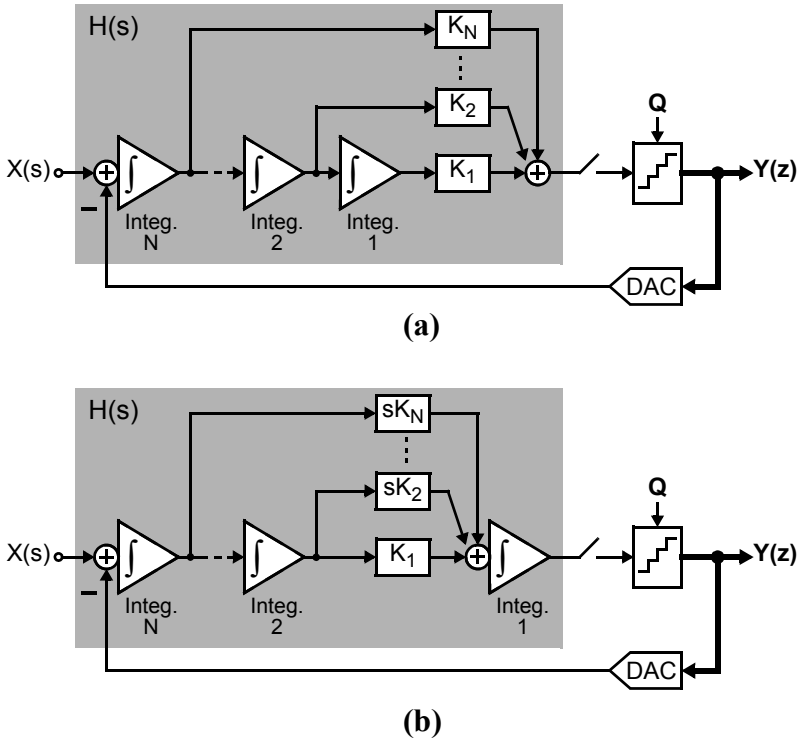

Figure 3.1 N^{th}-order feedforward CT ΔΣ modulator with: **(a)** classical feedforward compensation; **(b)** feedforward summation at the input of the last integrator. Here, $\int \equiv 1/(sT_S)$.

$$NTF_N(z) = \frac{(1-z^{-1})^N}{1 + c_1 z^{-1} + ... + c_{N-1} z^{-(N-1)} + c_N z^{-N}} \tag{3.3}$$

where the coefficients c_i are determined by the type of NTF (e.g., FIR or Butterworth). Note that, in this thesis, the subscript N in $NTF_N(z)$ is used to denote the order of this NTF.

A feedforward ΔΣ modulator architecture, where all the feedforward paths are summed within the last integrator stage of the loop filter (rather than at the input of the quantizer), is proposed in [Hamoui, TCASI04]. Thus, no summation amplifier is required at the input of the quantizer (the output of the ΔΣ loop filter), thereby reducing the circuit complexity and saving power. The concept in [Hamoui, TCASI04] was extended to CT ΔΣ modulators in [Schimper, ESSCIRC04] using capacitive feedforward paths, as modeled in Fig. 3.1b. Figure 3.2 depicts how the proposed NTF- enhancement technique can be applied to the CT feedforward ΔΣ modulator in

Fig. 3.1b. Observe that an additional feedback path K_H is used in Fig. 3.2 to compensate for excess loop delay [Ortmanns 06] [Keller, TCASI08]. To set the excess loop delay to exactly half a clock period, a half-delay block is inserted in the feedback path. To implement the required excess-loop-delay compensation, in Fig. 3.2, DAC2 must have a different pulse shape than DAC1. Since DAC1 generates a non-return-to-zero (NRZ) pulse, a return-to-zero (RZ) pulse is generated in DAC2 through a discrete-time differentiation, as proposed in [Mitteregger, JSSC06]. Note that an additional DAC (DAC3 in Fig. 3.2) and a sample-and-hold (S&H) are used to implement the NTF enhancement.

3.2 Circuit Implementation of the Proposed CT ΔΣ Modulator with NTF Enhancement

Figure 3.3 presents the circuit implementation of the last integrator in the proposed feedforward CT ΔΣ modulator with NTF enhancement and excess-loop-delay compensation in Fig. 3.2. Since the feedforward coefficients sK_i (i = 2, ... , N) in Fig. 3.2 can be implemented as ratios of capacitors in Fig. 3.3, their values are more accurately controlled than RC time constants. DAC2 in Fig. 3.3 consists of two replicas of DAC1 (DAC2a and DAC2b) and, hence, it has a simple implementation [Mitteregger, JSSC06]. The feedback coefficient K_H is implemented by scaling the feedback current level at the output of DAC2 [Kulchycki 07].

The passive NTF-enhancement filter $G_1(s)$ in Fig. 3.2 can be implemented using a simple RC network, which is connected to the input of the opamp used to implement the last integrator in loop filter $H(s)$, as shown in Fig. 3.3. Note that any opamp nonideality can affect the performance of this passive NTF-enhancement filter $G_1(s)$. Specifically, the opamp unity-gain frequency f_T limits the maximum realizable value of pole $s_p f_S$ of NTF-enhancement filter $G_1(s)$ in (2.14). The effect of the opamp nonidealities (finite nonlinear dc gain A_0 and finite unity-gain frequency f_T) on the performance of the proposed NTF-enhanced CT ΔΣ modulator are analyzed in Chapter 4.

The quantizer input X_Q is then fed back into the last integrator through a passive sample-and-hold (S&H) circuit, which is implemented using the double sampling technique shown in Fig 3.3.

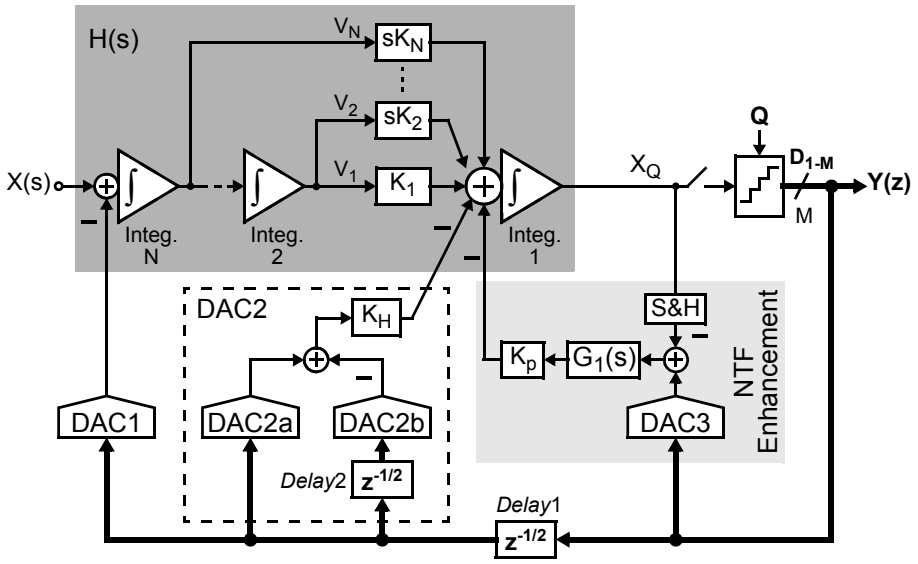

Figure 3.2 Proposed N^{th}-order feedforward CT ΔΣ modulator with NTF enhancement and excess-loop-delay compensation (using feedback path K_H through DAC2). Here, $\int \equiv 1/(sT_S)$.

Note that an accurate S&H (i.e., a S&H with an active implementation) is not used because errors in the voltage across the sampling capacitor C_S are suppressed at the input of the integrator in Fig. 3.3. This sample-and-hold is used to match the DAC transfer function $H_{DAC}(s)$ introduced by DAC3. This DAC3 can have a simple implementation, using only digital inverters. Furthermore, multibit operation can be achieved by splitting the passive circuit elements of $G_1(s)$ into multiple (M) unit elements, as shown in Fig. 3.3.

Due to the increased capacitive load on the last integrator of the ΔΣ loop filter in Fig. 3.1b, this integrator has higher power requirements (to drive the load), compared to the last integrator of the ΔΣ loop filter in a classical implementation (Fig. 3.1a) of an equivalent CT ΔΣ modulator. However, as explained in [Schimper, ESSCIRC04], the power saved by removing the summation amplifier at the output of the ΔΣ loop filter (at the input of the quantizer) in Fig. 3.1a more than compensates for the additional power consumed by the last integrator of the ΔΣ loop filter in

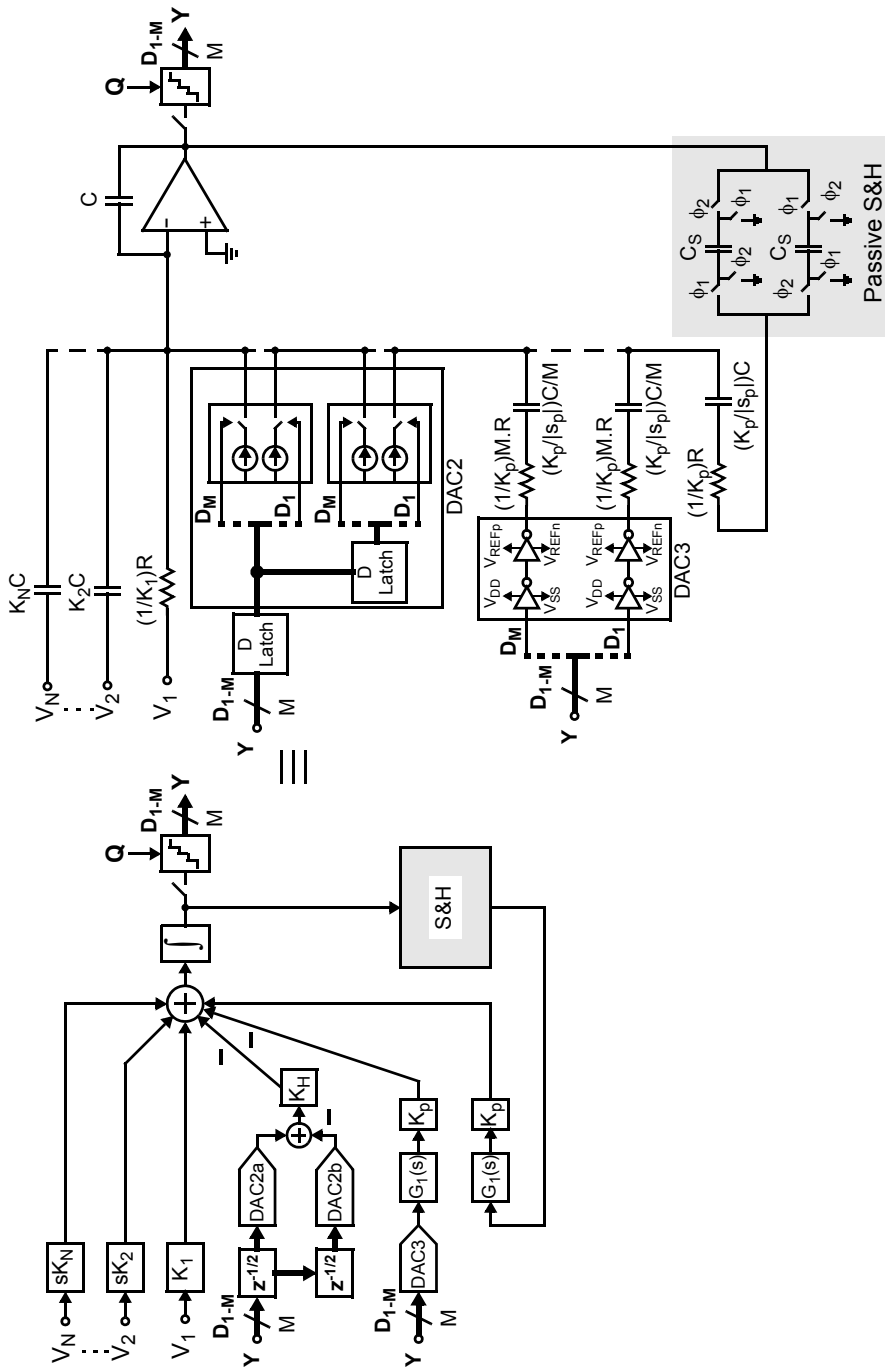

Figure 3.3 Single-ended circuit implementation of the last integrator (Integ. 1) in Fig. 3.2. Here, C and R are unit-size capacitors and resistors; C_S is the sampling capacitor; V_{REFp} and V_{REFn} are the positive and negative reference voltages of the quantizer; M is the number of output thermometer digits (input threshold levels) of the quantizer.

Fig. 3.1b. The inclusion of the passive S&H and the passive NTF-enhancement filter $G_1(s)$ in Fig. 3.2 and 3.3 further increases the capacitive load on the last integrator of the ΔΣ loop filter and, hence, further increases its power requirements. However, the relative increase in the loading effect due to the S&H and $G_1(s)$ is marginal, compared to the total loading effect of all the feedforward paths on the last integrator of the ΔΣ loop filter in Fig. 3.2 and 3.3. Therefore, the additional power requirements on this integrator, due to the inclusion of S&H and $G_1(s)$, are only minimal. This is further demonstrated through behavioral simulations in Chapter 4.

Chapter 4

Behavioral Simulation of CT ΔΣ Modulators with NTF Enhancement

4.1 System Level Non-idealities

In a ΔΣ modulator, the input node is not subject to any noise-shaping and hence needs to be designed carefully considering thermal noise, clock jitter and signal swing level. The following sections discusses how each of these three factors influences the ΔΣ modulator design.

4.1.1 Voltage-Level Scaling at the Output of the Last Integrator

As the rail voltages are getting smaller with advanced CMOS technologies, it is becoming increasingly important to limit the output signal swing to within the linear operating region of active circuits. The input-signal swing of the ΔΣ modulator needs to be maximized to avoid performance limitation due to thermal noise, however, larger signal swings would introduce distortion due to output saturation voltages of the opamps. Voltage-level scaling is used to scale down the signal levels at the output of the last opamp to within the range of linear operation.

Figure 4.1 shows how the coefficients of a classical CT ΔΣ modulators with feedforward architecture can be scaled to reduce the signal swing at the output of the last integrator of the loop filter. The scaling factor *g* needs to be carefully selected to optimize thermal noise level at the input and the settling and power requirement of the first opamp, as explained in [Hamoui 04]. Note that to reduce the signal swing at the output of the last integrator, the signal is scaled down by a factor of 2^a and then digitally scaled up to the original level. However, this will result in a loss of

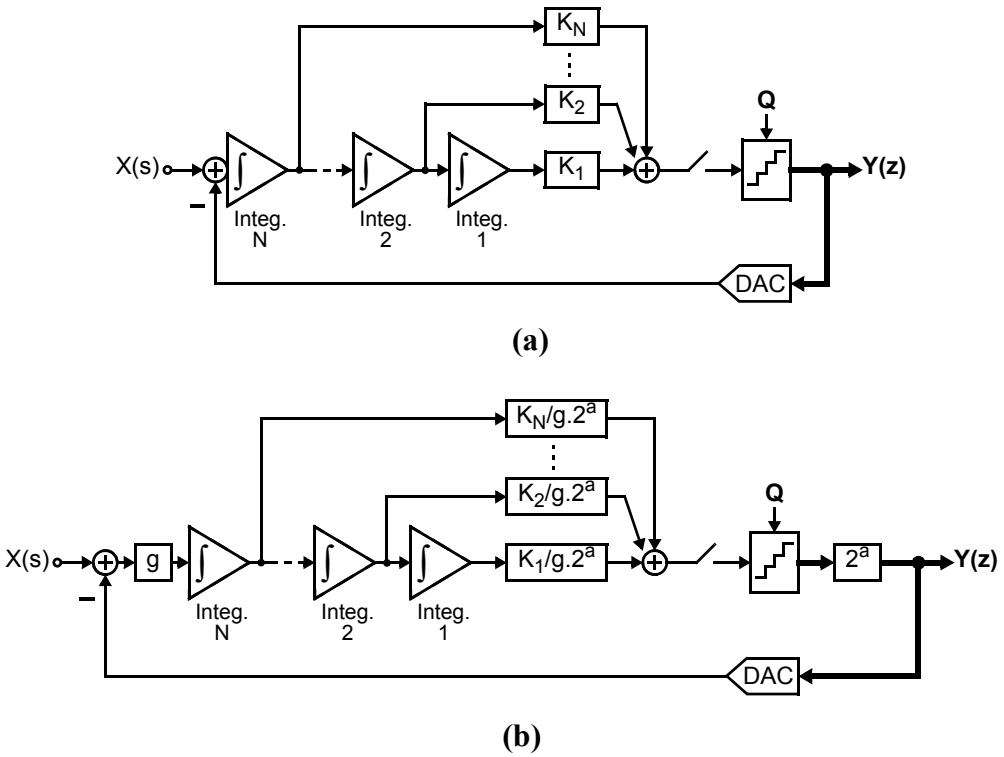

Figure 4.1 N^{th}-order feedforward CT ΔΣ modulator with: **(a)** classical architecture; **(b)** output voltage-level scaling. Here, $\int \equiv 1/(sT_S)$, g is a scaling coefficient and a is an integer.

quantizer resolution by a factor of 2^a and so, the amount of gain necessary from the quantizer needs to be carefully selected.

4.1.2 Thermal Noise

Circuit noise exists in all electric circuits due to the motion of electrons. This noise can have a white or frequency dependent spectrum. In CT ΔΣ modulators only the inband noise components influence the performance because the out-of-band noise is filtered out by the CT loop-filter and does not alias back inband, however, the location of the noise source is very important in determining its influence on performance. In ΔΣ modulators, the greatest amount of noise-shaping is available at the quantizer input and the least amount is available at the modulator input. Thus,

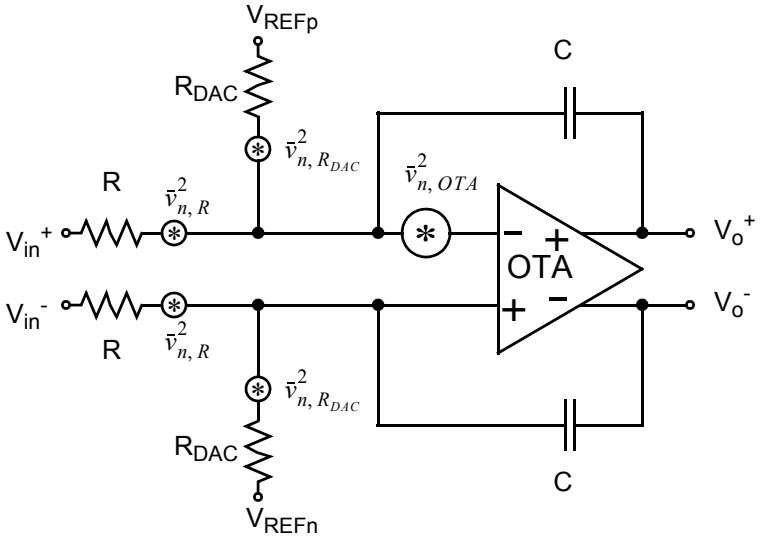

Figure 4.2 Schematic of a fully differential active RC-integrator with thermal noise sources.

the first integrator needs to satisfy the noise requirement of the entire ΔΣ modulator [Norsworthy 97].

Figure 4.2 shows the noise model of a fully differential active RC-integrator [Ortmanns 06]. For simplicity, the frequency dependent components are ignored. The total input-referred thermal-noise spectrum is:

$$\overline{v_{n,in}^2} = 2\left(\overline{v_{n,R}^2} + \overline{v_{n,R_{DAC}}^2}\frac{R^2}{R_{DAC}^2}\right) + \overline{v_{n,OTA}^2}\left(1+\frac{R}{R_{DAC}}\right)^2 \quad \frac{V^2}{Hz} \tag{4.1}$$

where, $\overline{v_{n,R}^2}$ and $\overline{v_{n,R_{DAC}}^2}$ is the thermal noise spectrum of the resistors R and R_{DAC} respectively, and $\overline{v_{n,OTA}^2}$ is the thermal noise spectrum of the OTA in Fig. 4.2.

Given that $\overline{v_{n,R}^2} = 4KTR$, $\overline{v_{n,R_{DAC}}^2} = 4KTR_{DAC}$ and $\overline{v_{n,OTA}^2} = 4KT\frac{\gamma}{g_{m_{OTA}}}$, then the total input-referred noise power is:

$$P_N = 8KTf_{BW}\left[R + R_{DAC}\frac{R^2}{R^2_{DAC}} + \frac{\gamma}{g_{m_{OTA}}}\left(\left(1+\frac{R}{R_{DAC}}\right)^2 + \frac{\pi^2}{3OSR^2}\right)\right] \tag{4.2}$$

where, γ is the transistor thermal noise factor, $g_{m_{OTA}}$ is the OTA transconductance and f_{BW} is the ΔΣ modulator bandwidth [Ortmanns 06].

4.1.3 Clock Jitter

CT ΔΣ modulators have been found to be particularly sensitive to clock-jitter errors that arise from two sources: (a) sampling errors in the forward path and (b) time-delay errors in the output pulses of the feedback DAC. Since maximum noise shaping is available at the quantizer input, the sampling errors are greatly suppressed and hence the dominant source of clock-jitter errors is the feedback DAC [Ortmanns 06]. Clock jitter can be represented as an additive timing error on the nominal edges α and β of the rectangular DAC pulses:

$$\widehat{\alpha}(n) \equiv \alpha + \Delta\alpha(n) \text{ and } \widehat{\beta}(n) \equiv \beta + \Delta\beta(n) \tag{4.3}$$

where $\widehat{\alpha}(n)$ and $\widehat{\beta}(n)$ represent the timing of the jittered edges of the rectangular DAC pulse, n represents the time index ($t = nT_S$) and the time-delay errors $\Delta\alpha$ and $\Delta\beta$ depend on the power spectrum of the clock jitter [Chopp, TCASI09].

Several techniques are available to alleviate the effects of clock jitter on CT ΔΣ modulators such as the use of multibit quantization as well as DAC pulse shaping (e.g. using non-return-to-zero rectangular pulses or exponentially sloping pulses) [Ortmanns 06]. Thus, CT ΔΣ modulators can be designed such that they are dominated by thermal and quantization noise and the effects of clock jitter can be marginalized.

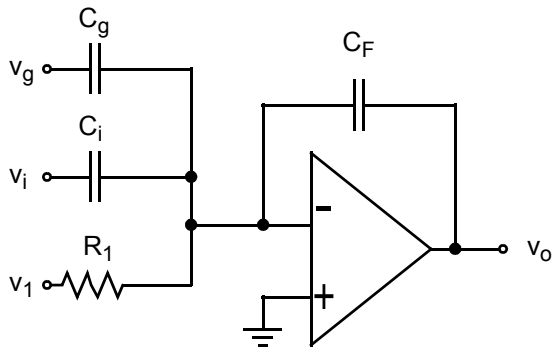

Figure 4.3 Schematic of a single-ended CT integrator (in Fig. 3.3) with an integration path (R_1), i feedforward summation paths (C_i) and an NTF-enhancement feedback path (C_g).

4.2 Behavioral Model of the CT Integrator

Consider the single-ended active RC-integrator in Fig. 4.3 with a resistive path (R_1) and i-capacitive feedforward paths (C_i). C_g is the total capacitive load from the NTF-enhancement filter $G_1(s)$ (in Fig. 3.3) seen at the input of the integrator and C_F is the integrator feedback capacitor. The resistive path implement the integration functionality and the capacitive paths implement a summation amplifier functionality. The opamp is defined using first order approximation:

$$A(s) = \frac{A_0}{1 + s/\omega_p} \tag{4.4}$$

where A_0 is the opamp dc gain, ω_p is the dominant pole and s is the Laplace operator [Johns 97]. It is assumed that the opamp has a 2-stage configuration such that the opamp gain A_0 and dominant pole ω_p remain unaffected by the load and that all other opamp poles are located at frequencies much higher than the opamp unity-gain frequency ω_t, and, hence, are ignored. The opamp's unity-gain frequency can be can be approximated as:

$$\omega_{ta} = A_0\omega_p \tag{4.5}$$

The resistive path R_1 in Fig. 4.3 is used to perform the CT integration. The ideal transfer function of the CT integrator is then:

$$I_{ideal}(s) = K_1 \frac{f_S}{s} \tag{4.6}$$

where f_S is the sampling frequency of the CT ΔΣ modulator and the integrator scaling coefficient K_1 is given by:

$$K_1 = \frac{1}{R_1 C_F f_S} \tag{4.7}$$

Accounting for the finite gain and bandwidth of the opamp, the transfer function of the CT integrator (resistive path R_1 in Fig. 4.3) can be expressed as:

$$I(s) = K_1 \frac{f_S}{s} GE(s) \tag{4.8}$$

where

$$GE(s) = \frac{\omega_{ta} s}{\left(1 + \frac{C_g}{C_F} + \sum_{i=2}^{N} K_i\right) s^2 + \left[\omega_{ta} + K_1 f_S + \omega_p \left(1 + \frac{C_g}{C_F} + \sum_{i=2}^{N} K_i\right)\right] s + (\omega_p K_1 f_S)} \tag{4.9}$$

Here, $GE(s)$ is the gain-error transfer function introduced due to the opamp's finite gain A_0 and finite bandwidth ω_p and K_i is the i^{th} capacitive coefficient defined as:

$$K_i = \frac{C_i}{C_F} \tag{4.10}$$

The capacitive paths C_i in Fig. 4.3 are used to perform the summation amplifier function. The ideal transfer function for the summation amplifier is:

$$v_{o,\,ideal} = \sum_{i=2}^{N} K_i v_i \tag{4.11}$$

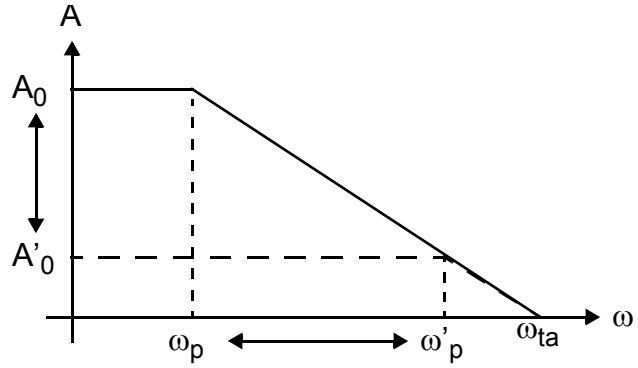

Figure 4.4 Effect of nonlinear variations in opamp dc gain on its frequency response.

However, due to the opamp's finite gain and finite bandwidth, a gain error is introduced in the summation amplifier function as follows:

$$v_o = \sum_{i=2}^{N} K_i v_i \; GE(s) \tag{4.12}$$

where $GE(s)$ is defined in (4.9).

In addition to the finite gain and finite bandwidth properties of the opamp, nonlinear dc gain is included into the CT integrator model. Nonlinear gain arises when the output signal swing is large and affects the MOSFET output resistance r_{DS}. The nonlinear variations in opamp dc gain A_0 can be modeled as the function of opamp output voltage v_o using:

$$A_0(v_o) = \begin{cases} A_{0\max}\left[1 - \left(\dfrac{v_o}{v_{o,\,sat}}\right)^2\right] & \text{for } v_o \le v_{o,\,sat} \\ 0 & \text{for } v_o > v_{o,\,sat} \end{cases} \tag{4.13}$$

where $A_{0\max}$ is the maximum dc gain and $v_{o,\,sat}$ is the opamp's output saturation voltage [Hamoui 04] [Hamoui 09]. The nonlinear variation in opamp dc gain is included into the model such that a change in dc gain A_0 affects the opamp's dominant pole ω_p, while keeping the unity-gain frequency ω_{ta} constant, as shown in Fig. 4.4. Although this model is not accurate, it provides a reasonable approximation for the purpose of system-level behavioral simulations.

4.3 Behavioral Simulation Results

4.3.1 Behavioral-Simulation Conditions and Models

Behavioral simulations were performed in SIMULINK to compare the performance of the proposed NTF-enhanced N^{th}-order CT ΔΣ modulator (Fig. 4.5b) versus a classical feedforward $(N+1)^{\text{th}}$-order CT ΔΣ modulator (Fig. 4.5a), for the cases of $N = 2$ and $N = 3$, under the following conditions:

- FIR NTFs, with the pole of the NTF-enhancement filter $G_1(s)$ (2.14) in Fig. 4.5b at $s_p f_S = -3f_S$.
- Ideal DACs, with NRZ rectangular pulses (for DAC1 in Fig. 4.5b) having $\alpha = 0$ and $\beta = 1$. Hence, as per (2.10), $K_p = -s_p$ in (2.14).
- Ideal midrise quantizer with 15-level (4-bit) output in the $N = 2$ case and 31-level (5-bit) output in the $N = 3$ case. The quantizer reference voltage is set to $V_{REF} = 1/\sqrt{2}$ V in both cases.
- The input-signal bandwidth is assumed to be $f_{BW} = 1.1$ MHz, and a sinusoidal input signal at $f_{in} = 330$ kHz is applied, so that the first 3 input-signal harmonics fall within the signal band.
- Opamp output saturation voltage is set to $v_{o,sat} = 1/\sqrt{2}$ V.

The behavioral models accounted for the finite dc gain A_0 and the finite unity-gain frequency f_T of the opamps in the CT integrators, as described in [Ortmanns 06]. Furthermore, the nonlinear variations in the opamp dc gain A_0 are modeled as a function of the opamp (integrator) output voltage v_o, as defined in (4.13).

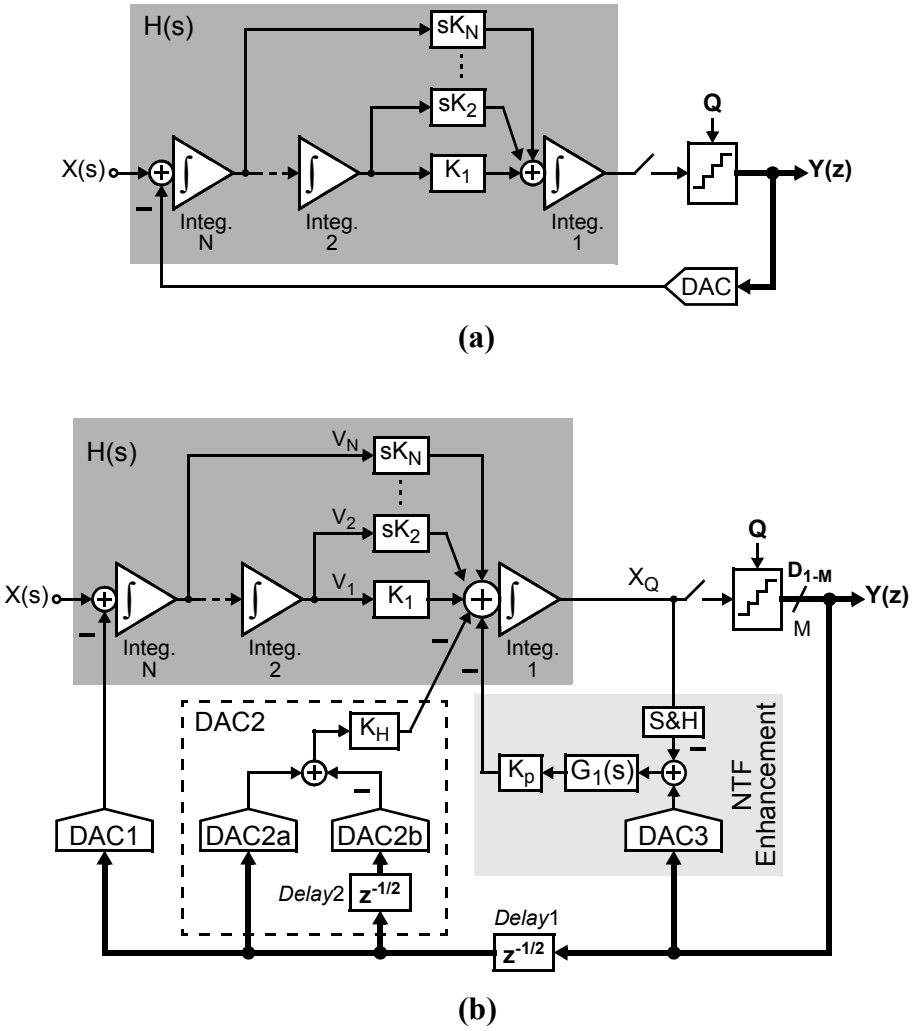

Figure 4.5 N^{th}-order feedforward CT ΔΣ modulator with: **(a)** classical feedforward architecture. **(b)** proposed architecture with NTF enhancement and excess-loop-delay compensation (using feedback path K_H through DAC2). Here, $\int \equiv 1/(sT_S)$.

Let τ_{RC} denote the RC time constant of the integrating path in the CT integrators. For example, τ_{RC} of the last integrator (Integ. 1) in the feedforward CT ΔΣ modulators of Fig. 4.5a and Fig. 4.5b can be expressed as:

$$\tau_{RC} = \frac{1}{K_1 f_S} \tag{4.14}$$

where f_S is the modulator's sampling frequency [Ortmanns 06]. Furthermore, define the gain-bandwidth excess factor of the opamps in the CT integrators of the ΔΣ modulators as:

$$K_{GBW} = \frac{f_T}{f_S} \tag{4.15}$$

where f_T is the opamp's unity-gain frequency.

In the following, behavioral simulation results are presented to compare the performance of NTF-enhanced (Fig. 4.5b) versus classical (Fig. 4.5a) feedforward CT ΔΣ modulators, in terms of their dynamic ranges, their tolerances to errors in τ_{RC}, and their requirements on K_{GBW} in their last integrator (Integ. 1).

4.3.2 Requirements on the Opamp Unity-Gain Frequency

Figure 4.6 plots the SNR versus K_{GBW} for the *last* integrator (Integ. 1) of the NTF-enhanced N^{th}-order (Fig. 4.5b) and classical N^{th}-order and $(N+1)^{\text{th}}$-order (Fig. 4.5a) feedforward CT ΔΣ modulators, for $N = 2$, OSR = 16 (Fig. 4.6a) and $N = 3$, OSR = 8 (Fig. 4.6b). A large $K_{GBW} = 5$ is assumed in the previous integrators, in order to decouple their effects on the overall performance. Furthermore, an $A_{0\max} = 45$ dB is assumed in the first integrators, while an $A_{0\max} = 50$ dB is assumed in the last integrator which does not have any resistive load and, hence, can have a larger dc gain. To focus this analysis on the effect of K_{GBW} on SNR, the dc gains A_0 of opamps are assumed to be constant (i.e. the nonlinear dc-gain variations are neglected) in these behavioral simulations. The input-signal amplitude is set to $V_{in} = -3.1$ dBFS for all cases. It is observed that the last integrator of the NTF-enhanced N^{th}-order CT ΔΣ modulator (Integ. 1 in Fig. 4.5b) has a larger K_{GBW} requirement when compared to a classical N^{th}-order CT ΔΣ modulator because the passive NTF-enhancement filter $G_1(s)$ in Fig. 4.5b introduces more

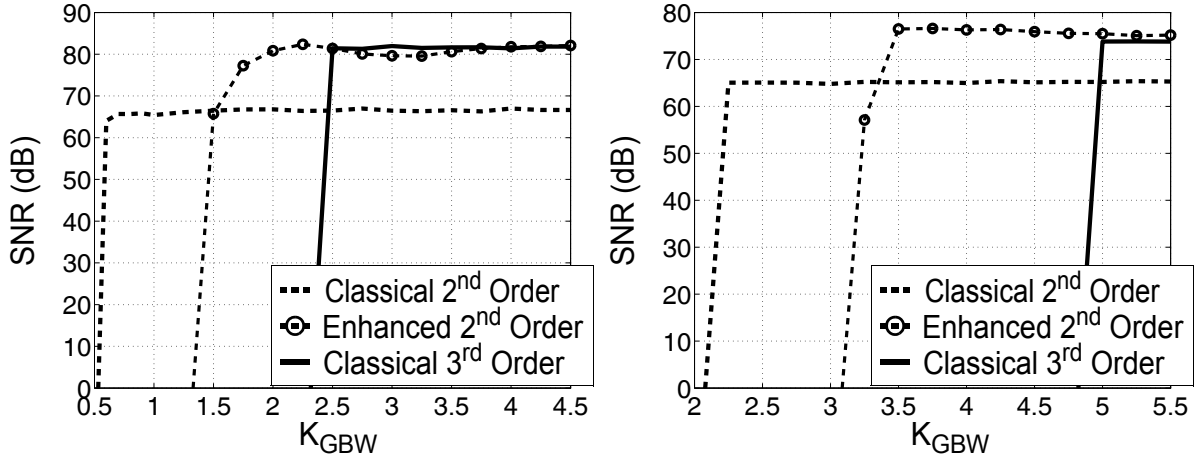

Figure 4.6 Effect of opamp gain-bandwidth excess factor K_{GBW} on SNR performance of the classical N^{th}-order, NTF-enhanced N^{th}-order and classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulators, for the last integrator (Integ. 1) in Fig. 4.5a and Fig. 4.5b with constant dc gain $A_0 = 50$ dB, for: **(a)** $N = 2$, OSR = 16; and **(b)** $N = 3$, OSR = 8. A large $K_{GBW} = 5$ with constant dc gain $A_0 = 45$ dB is set for all previous integrators. Input-signal amplitude is set to V_{in} = -3.1 dBFS for all cases.

capacitive load on Integ. 1. However, the K_{GBW} requirement for this integrator (Integ. 1 in Fig. 4.5b) is significantly lower when compared to the classical $(N+1)^{\text{th}}$-order CT ΔΣ modulator. This is because the classical $(N+1)^{\text{th}}$-order CT ΔΣ modulator has an additional capacitive feedforward path K_{N+1} that loads its last integrator. Furthermore, the feedforward coefficient values for the classical $(N+1)^{\text{th}}$-order CT ΔΣ modulator, K_i $(i = 2...N+1)$ are larger than the feedforward coefficient values for the NTF-enhanced N^{th}-order CT ΔΣ modulator. Accordingly, the last integrator (Integ. 1) of the classical $(N+1)^{\text{th}}$-order CT ΔΣ modulator has a significantly larger capacitive load when compared to the NTF-enhanced N^{th}-order CT ΔΣ modulator and, hence, it has a significantly larger K_{GBW} requirement. Thus, the proposed NTF-enhancement technique can be used to design CT ΔΣ modulators with lower power requirements.

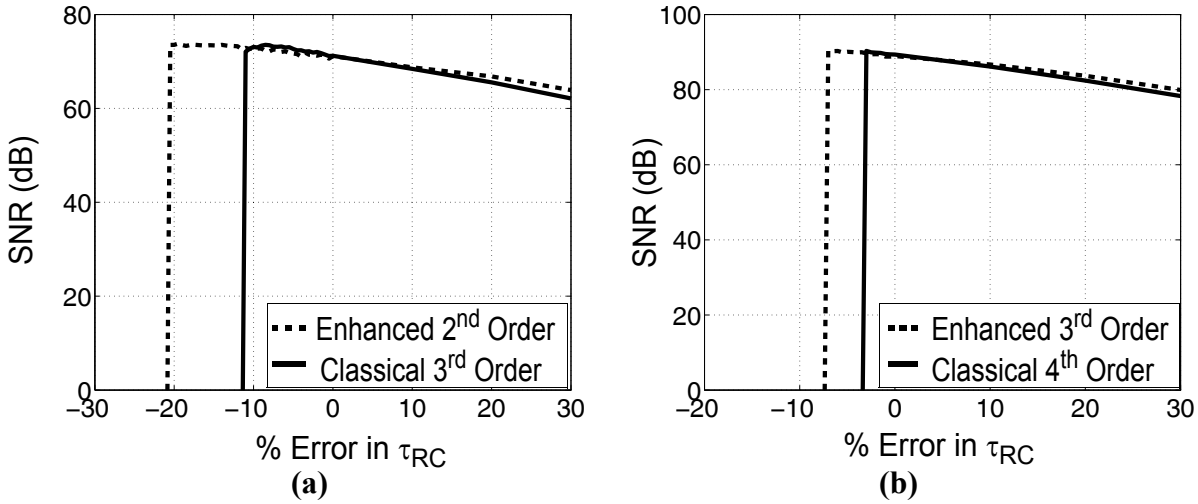

Figure 4.7 Effect of errors in integrator *RC* time constants (τ_{RC}) on SNR performance of the NTF-enhanced N^{th}-order and classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulators, for: **(a)** $N = 2$; and **(b)** $N = 3$. Here, OSR = 12, V_{in} = -6.2 dBFS and all integrators have a large $K_{GBW} = 5$. Integ. 1 has a constant dc gain $A_0 = 50$ dB and all previous integrators have a constant dc gain $A_0 = 45$ dB.

4.3.3 Tolerance to Integrator Gain Errors

Figure 4.7 compares the SNR versus error in τ_{RC} for the NTF-enhanced N^{th}-order and classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulators for $N = 2$ (Fig. 4.7a) and $N = 3$ (Fig. 4.7b). The input-signal amplitude $V_{in} = -6.2$ dBFS and OSR = 12. All integrators have a large $K_{GBW} = 5$ in order to decouple their effects on the overall performance. The last integrators (Integ. 1) have a constant dc gain $A_0 = 50$ dB and all previous integrators have a constant dc gain $A_0 = 45$ dB (i.e. the nonlinear dc-gain variations are neglected). Accordingly, for $N = 2$, while the classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulator is only stable up to 10% error in τ_{RC}, the NTF-enhanced N^{th}-order feedforward CT ΔΣ modulator is stable up to 20% error. Similarly, for $N = 3$, while the classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulator is only stable up to 3% error in τ_{RC}, the NTF-enhanced N^{th}-order feedforward CT ΔΣ modulator is stable up to 7%

error. This confirms that a significant improvement in the tolerance of the ΔΣ modulator to τ_{RC} error can be achieved by using the proposed NTF-enhancement technique. This improved stability performance is expected, as an NTF-enhanced N^{th}-order feedforward CT ΔΣ modulator has one less integrating-path coefficient than a classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulator, even though both modulators have the same FIR NTF. In the NTF-enhanced ΔΣ modulator, this coefficient is implemented using path K_p. Therefore, variations in this coefficient value do not increase the NTF's out-of-band gain in the NTF-enhanced ΔΣ modulator (Fig. 2.2b) and, hence, do not affect the modulator's stability. Accordingly, although coefficient-tuning techniques are still required to compensate for τ_{RC} errors in high-order NTF-enhanced CT ΔΣ modulators, the constraints on the accuracy of these techniques are significantly relaxed.

Note that, in Fig. 4.5b, the NTF enhancement is implemented in a ΔΣ modulator with a feedforward single-loop architecture and, hence, the coupled quantization noise is partially correlated to the quantization noise introduced by the quantizer. A further improvement in stability can be achieved if the coupled quantization noise and the noise introduced by the quantizer were uncorrelated. This can be accomplished by applying the NTF-enhancement technique to ΔΣ modulators with 'split' architecture [Lee, ICECS06] [Wang, CICC08]. In this case, the NTF-enhanced N^{th}-order feedforward CT ΔΣ modulator will maintain the stability of a classical N^{th}-order feedforward CT ΔΣ modulator (i.e., before NTF-enhancement).

4.3.4 Tolerance to Quantizer Overload

The SNDR performance versus input-signal amplitude V_{in} of the NTF-enhanced N^{th}-order and classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulators is shown in Fig. 4.8, for $N = 2$ (Fig. 4.8a) and $N = 3$ (Fig. 4.8b). When $N = 2$, Integ. 1 has a dc gain $A_{0\max} = 50$ dB and opamp gain-bandwidth excess factor $K_{GBW} = 3$ and when $N = 3$, Integ. 1 has $A_{0\max} = 50$ dB and $K_{GBW} = 5$. All previous integrators have $A_{0\max} = 45$ dB and $K_{GBW} = 1$. The over-sampling ratio is set to OSR = 12 for all cases. It is observed that, in each case ($N = 2, 3$), both ΔΣ modulators have equal (within 2 dB) peak-SNDR and dynamic-range (DR) performances. It is important to point out that in the NTF-enhanced N^{th}-order feedforward CT ΔΣ modulators, the

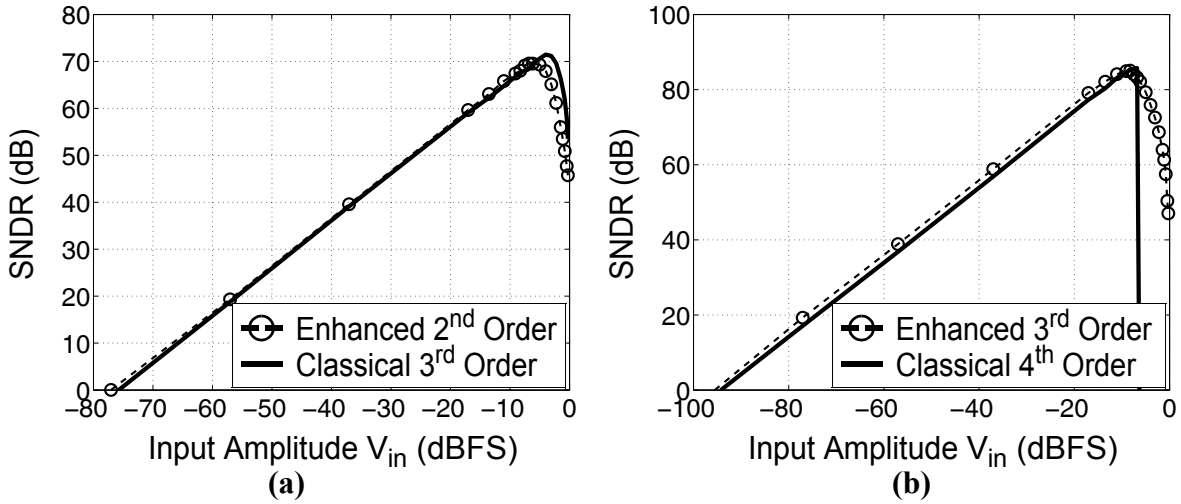

Figure 4.8 Effect of input-signal amplitude V_{in} on SNDR performance of the NTF-enhanced N^{th}-order and classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulators, for: **(a)** $N = 2$, Integ. 1 has $A_{0\max} = 50$ dB and $K_{GBW} = 3$; and **(b)** $N = 3$, Integ. 1 has $A_{0\max} = 50$ dB and $K_{GBW} = 5$. Here, OSR = 12 and all previous integrators have $A_{0\max} = 45$ dB and $K_{GBW} = 1$.

noise-shaping enhancement only affects the quantization noise and, therefore, any opamp distortion and sampling errors at the output of the last integrator are shaped by an N^{th}-order NTF only (i.e., without enhancement). Therefore, at low OSR, the drop in peak SNDR and DR of the NTF-enhanced N^{th}-order feedforward CT ΔΣ modulator compared to those of the classical $(N+1)^{\text{th}}$-order feedforward CT ΔΣ modulator becomes significantly larger than 2 dB, especially for low-order ΔΣ modulators.

Chapter 5

Design of an NTF-Enhanced 2nd-Order CT ΔΣ Modulator

5.1 Voltage-Level Scaling at the Output of the Last Integrator

The proposed NTF-enhancement technique is applied to a 2nd-order feedforward CT ΔΣ modulator, targeting a 12-bit SNDR over 1.1-MHz bandwidth. In order to meet the 12-bit SNDR requirement, this ΔΣ modulator is over designed at the system level, to have a 13-bit resolution. The NTF-enhanced CT ΔΣ modulator is modeled in SIMULINK as shown in Fig. 5.1. Behavioral simulations were performed to compare the performance of the ΔΣ modulator in Fig. 5.1 for the

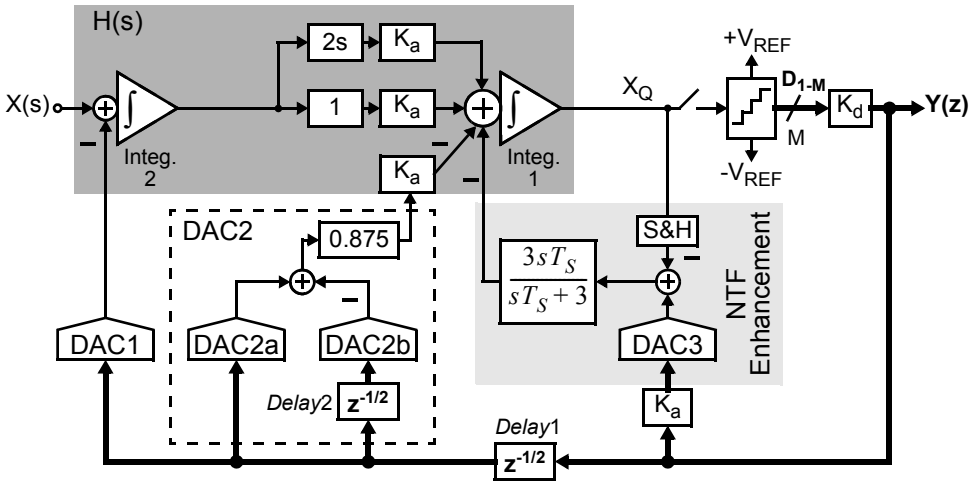

Figure 5.1 Behavioral model of the proposed NTF-enhanced 2nd-order CT ΔΣ modulator with capacitive feedforward architecture, including excess-loop-delay compensation and output-level scaling (K_a = 0.5, K_d = 2). Here, $\int \equiv 1/(sT_S)$, $V_{REF} = v_{o,\,sat}$ = 0.7 V, OSR = 20, V_{in} = -3.1 dBFS.

case of $K_a = 0.5$, $K_d = 2$ (i.e., output-voltage-level scaling is performed) versus the case of $K_a = 1$, $K_d = 1$ (i.e. output-voltage-level scaling is not used), under the following conditions

- FIR NTFs, with the pole s_p of the NTF-enhancement filter $G_1(s)$ (2.14) in Fig. 5.1 at $-3f_S$.
- Ideal DACs, with NRZ rectangular pulses (for DAC1 in Fig. 5.1) having $\alpha = 0$ and $\beta = 1$. Hence, as per (2.10), $K_p = -s_p$ in (2.14).
- Ideal midrise quantizer with 31-level (5-bit) output. The quantizer reference voltage is set to $V_{REF} = 1/\sqrt{2}$ V in both cases.
- The input-signal bandwidth is assumed to be $f_{BW} = 1.1$ MHz, and a sinusoidal input signal at $f_{in} = 330$ kHz is applied, so that the first 3 input-signal harmonics fall within the signal band.
- Opamp output saturation voltage is set to $v_{o,sat} = 1/\sqrt{2}$ V.
- The unity-gain frequency ω_{ta} for Integ. 1 and Integ. 2 in Fig. 5.1 is set to $6\pi f_S$ and $4\pi f_S$ respectively and dc gain for Integ. 1 and Integ. 2 was set to $A_{0\max} = 50$ dB and $A_{0\max} = 45$ dB respectively.
- The modulator over-sampling ratio is set to $OSR = 20$.
- Effects of clock jitter are not included for simplicity.
- Excess loop delay of half-clock period was introduced into the feedback path.

Figure 5.2 shows the variation in SNR performance as the total input-referred thermal noise $\overline{v_{n,in}^2}$ is increased. It is determined that, before output-level scaling is performed ($K_a = 1$, $K_d = 1$), the performance is severely limited due to input-referred thermal noise. When $\overline{v_{n,in}^2}$ is only about $1.5\times10^{-16} V^2/Hz$, the modulator performance falls below the 13-bit resolution target.

When output-level scaling is performed ($K_a = 0.5$, $K_d = 2$), as shown in Fig. 5.1, the input-signal amplitude can be set to $V_{in} = -3.1$ dBFS while still maintaining the signal swing within the opamp's output saturation voltage level $v_{o,sat} = 1/\sqrt{2}$. Additionally, the signal level at the quantizer input X_Q remains unchanged by the output-level scaling, as shown by the histograms in Fig. 5.3. This implies that, the number of comparators needed to implement the quantizer remain unchanged and, thus, the quantizer does not consume additional power.

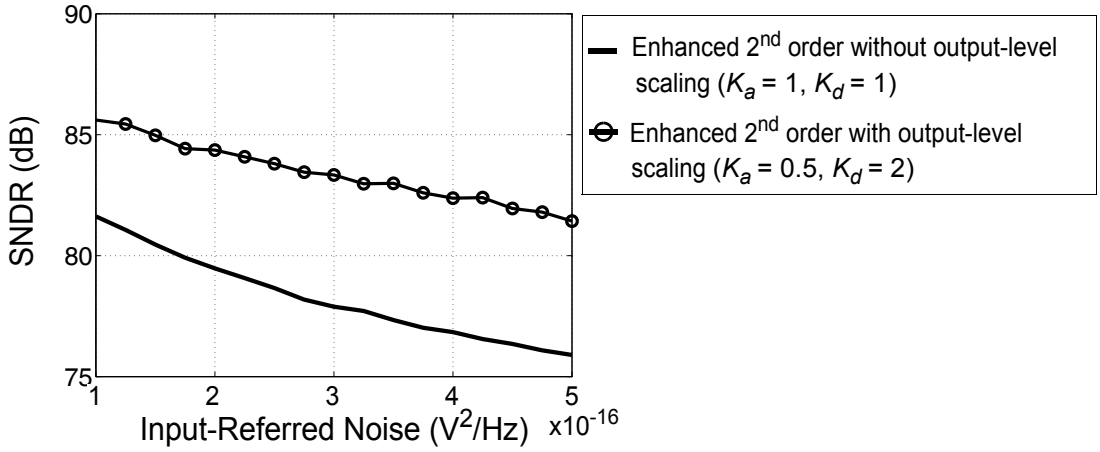

Figure 5.2 Effect of thermal noise on SNR performance of the NTF-enhanced 2nd-order CT ΔΣ modulator in Fig. 5.1. ($V_{REF} = v_{o,\,sat} = 0.7$ V, OSR = 20, V_{in} = -3.1 dBFS).

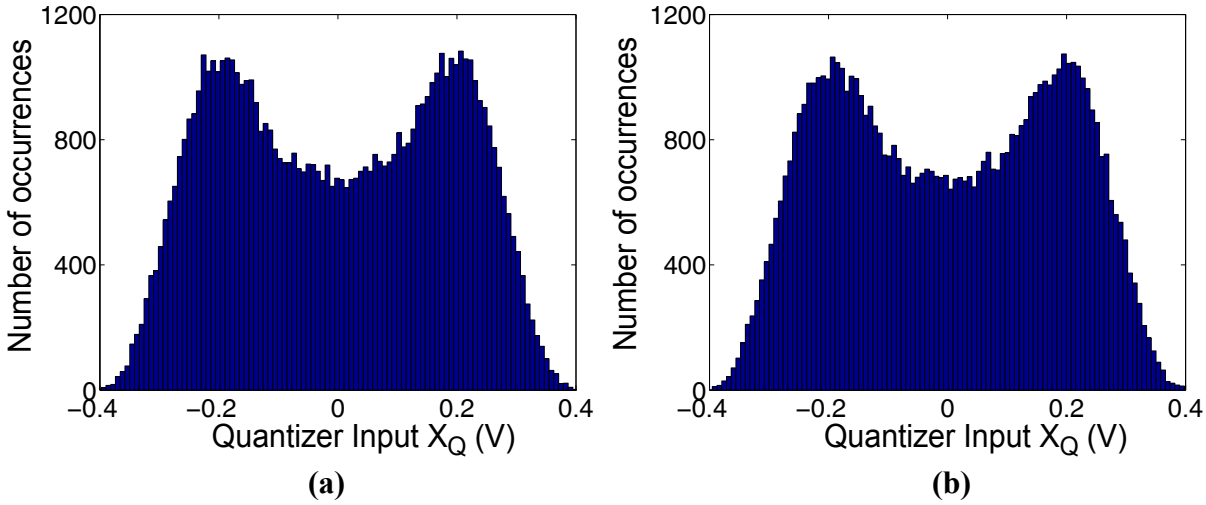

Figure 5.3 Histogram of the quantizer input signal level X_Q for the NTF-enhanced 2nd-order CT ΔΣ modulator in Fig. 5.1: **(a)** with output-level scaling ($K_a = 0.5$, $K_d = 2$); and **(b)** without output-level scaling ($K_a = 1$, $K_d = 1$). ($V_{REF} = v_{o,\,sat} = 0.7$ V, OSR = 20, V_{in} = -3.1 dBFS).

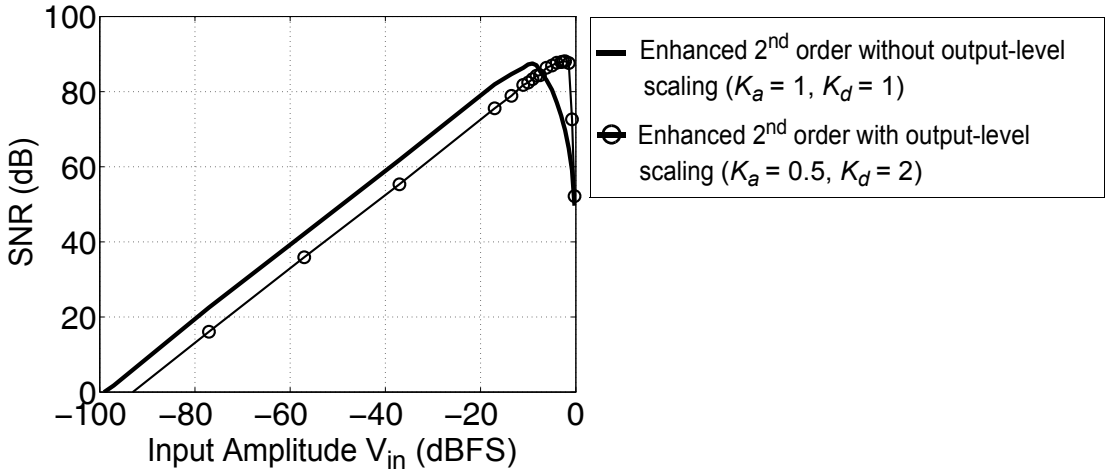

Figure 5.4 Effect of output-level scaling on SNR performance of the proposed NTF-enhanced 2nd-order CT ΔΣ modulator in Fig. 5.1 ($V_{REF} = v_{o,\,sat}$ = 0.7 V, OSR = 20, V_{in} = -3.1 dBFS, DR = 90dBFS).

Furthermore, the increased tolerance to thermal noise (up to about $4.5\times10^{-16}V^2/Hz$), implies that less power is needed to reduce thermal noise at the input node of the ΔΣ modulator and, hence, provides greater potential for low power design. As shown in Fig. 5.4, the effective dynamic range (DR) of the ΔΣ modulator remains unchanged at DR = 90 dBFS.

5.2 Noise Budget

The dominant noise component is the thermal noise from the input resistors of the integrator and the opamp used to implement the integrator, of which, the input resistor is set to be the larger noise source. Accordingly, the first opamp is designed to contribute $1.5\times10^{-16}V^2/Hz$ and the input resistor contributes $3\times10^{-16}V^2/Hz$ of noise. This implies that, the maximum value of the input resistor has to be less than 9kΩ. Table 5.1 lists the minimum specifications for the opamps used to implement the CT integrators in Fig. 5.1. The first opamp drives a resistive load, and so, its dc gain value is reduced due to the loading effect. The first stage of the first opamp (Integ. 1) is scaled down by a factor of 3 to reduce power consumption. This is possible because of the first-order noise shaping available at the input of Integ. 1 in Fig. 5.1. The second stage of this opamp is not scaled

down because it needs to drive a large capacitive load (quantizer and passive S&H). Table 5.2 lists the SNR performance of the NTF-enhanced 2nd-order feedforward CT ΔΣ modulator when different nonidealities are introduced into the system. Behavioral simulations in SIMULINK, under the conditions listed in Section 5.1, confirmed that the ΔΣ modulator in Fig. 5.1 meets the 13-bit resolution specification for a 1.1 MHz signal bandwidth.

Specification	Second Opamp (Integ. 2)	First Opamp (Integ. 1)
Total load capacitance	4.5 pF	5.5 pF
Total load resistance	30 kΩ	N/A
Differential output voltage swing amplitude	300 mV	700 mV
DC gain (with load), A_0	45 dB	50 dB
Unity-gain frequency, f_t	200 MHz	200 MHz
Phase margin	70^o	70^o
Input-referred thermal noise, $\overline{v_{n,OTA}^2}$	$1.5 \times 10^{-16}\, V^2/Hz$	$4.5 \times 10^{-16}\, V^2/Hz$

Table 5.1 Minimum opamp specifications for the integrators in Fig. 5.1.

Error Source	SNDR (dB)
Ideal Case (quantization noise only)	89
Additional Error Sources	
Opamp finite gain and finite bandwidth ($A_0 = 50dB$, $\omega_{ta} = 200MHz$)	88.9
Nonlinear opamp gain ($V_{in} = -3.1dBFS$)	88.3
Thermal noise ($\overline{v_n^2} = 4.5\times10^{-16}$ V^2/Hz)	82.5
Including all non-idealities	81.5

Table 5.2 Noise budget for the proposed NTF-enhanced CT ΔΣ modulator in Fig. 5.1 with output-level scaling. ($V_{REF} = 0.7$ V, $V_{in} = 0.7V_{REF}$, $OSR = 20$, $f_{BW} = 1.1$ MHz, $f_{in} = 0.3f_{BW}$, $f_S = 44$ MHz, $K_a = 0.5$, $K_d = 2$).

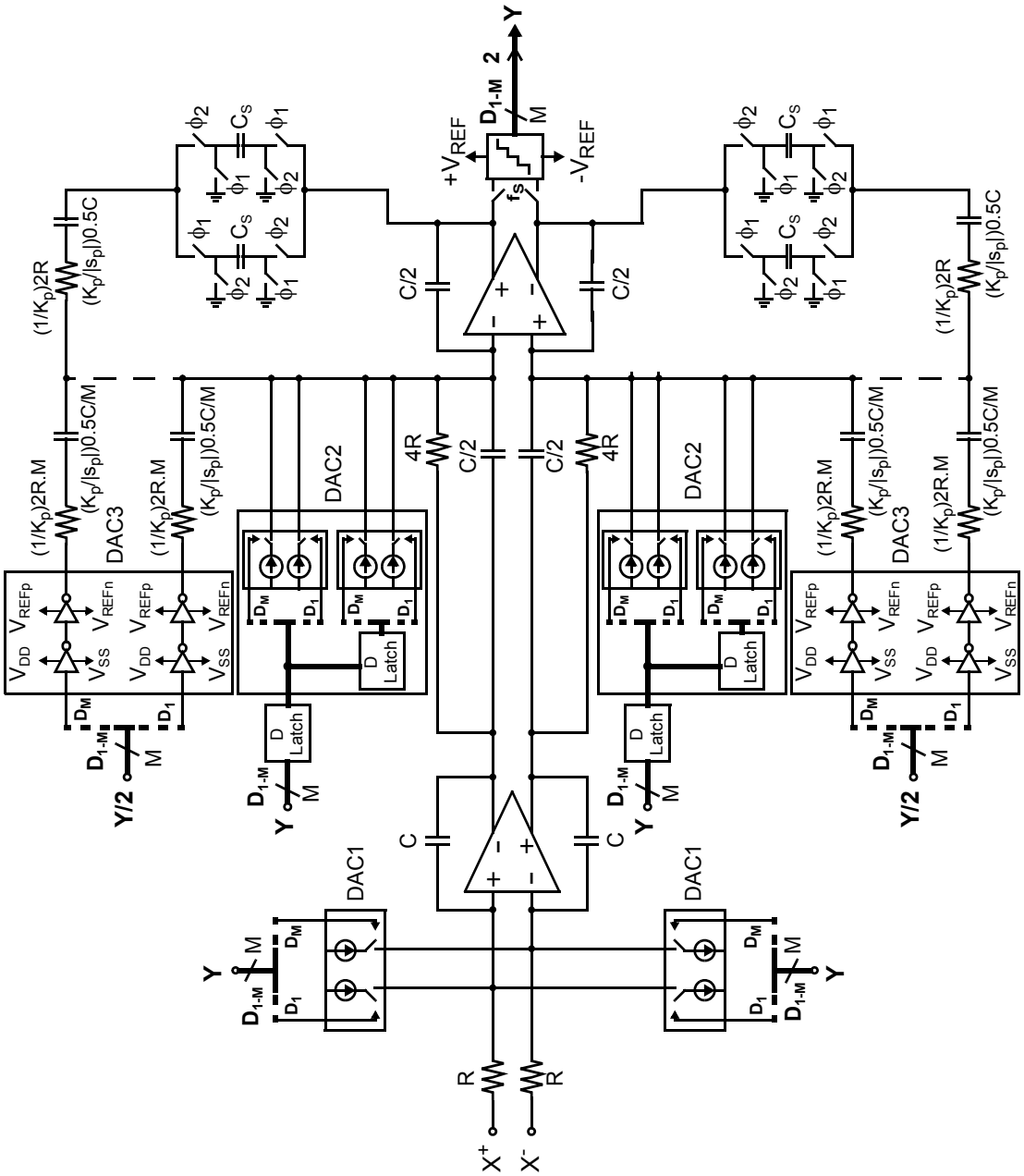

Figure 5.5 Fully-differential circuit-level implementation of the NTF-enhanced 2nd-order feedforward CT ΔΣ Modulator in Fig. 5.1 with output-level scaling ($K_a = 0.5$, $K_d = 2$). Here C and R are unit capacitors and unit resistors respectively such that $f_S = 1/RC$ and C_S is the sampling capacitor. V_{REFp} and V_{REFn} are the quantizer positive and negative reference voltages respectively and M is the number of quantizer levels.

5.3 Proposed NTF-Enhanced 2nd-Order CT ΔΣ Modulator

Figure 5.5 shows the entire fully-differential, circuit-level implementation of the proposed NTF-enhanced 2nd-order feedforward CT ΔΣ Modulator from Fig. 5.1. R is set to 7.6kΩ and C is set to 3pF in order to meet the noise budget for the ΔΣ Modulator as explained in the previous section. The NTF-enhancement filter pole s_p is set to $-3f_S$, $K_p = |s_p| = 3$ and $M = 31$.

5.4 Opamp Design

Fully-differential 2-stage opamps [Johns 97] are used to implement the integrators in the NTF-enhanced 2nd-order feedforward CT ΔΣ modulator shown in Fig. 5.5. The circuit-level implementation of the 2-stage opamp is shown in Fig. 5.6. This 2-stage opamp topology is advantageous for this application because the first stage provides moderate gain and the 2nd stage provides a wide-swing output and isolates the dominant opamp pole from the load. The opamps output swing (region of linear operation) needs to be maximized because of the small supply voltage (1V) and sensitivity of the NTF-enhanced 2nd-order feedforward CT ΔΣ modulator to opamp errors as described in the previous chapter.

The bulks for the input transistors M_1 and M_2 are slightly positively biased to reduce their threshold voltage V_{th}, to ensure they operate in the saturation region even with a low supply voltage. This low-voltage design technique is described in [Chatterjee, JSSC05].

The opamp's output common-mode voltage is controlled by the CMFB circuits described in [Chatterjee, JSSC05]. For the 2-stage opamp, two CMFB circuits are required, one of each stage as shown in Fig. 5.6. A current is driven through the resistors R_1 using the transistor M_{11}, in order to create a voltage difference across them. This is used to bias the gates of transistors M_3 and M_4 and coupling it with the output common-mode voltage of the first stage. This creates a negative feedback and hence sets the output common-mode voltage of the first stage.

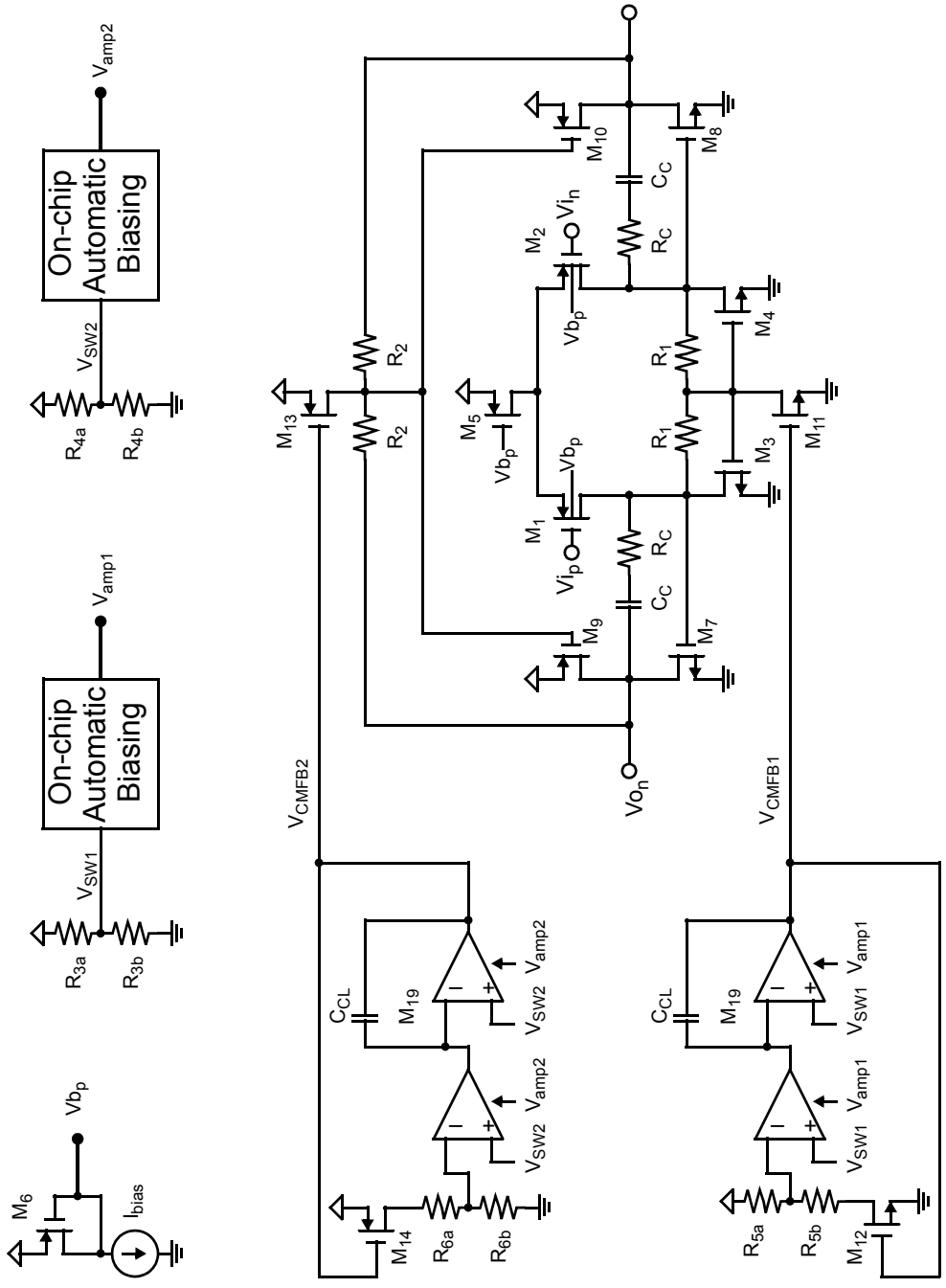

Figure 5.6 Fully-differential 2-stage Opamp with lead compensation [Johns 97]. The conceptual schematic for the CMFB circuit is shown here [Chatterjee, JSSC05].

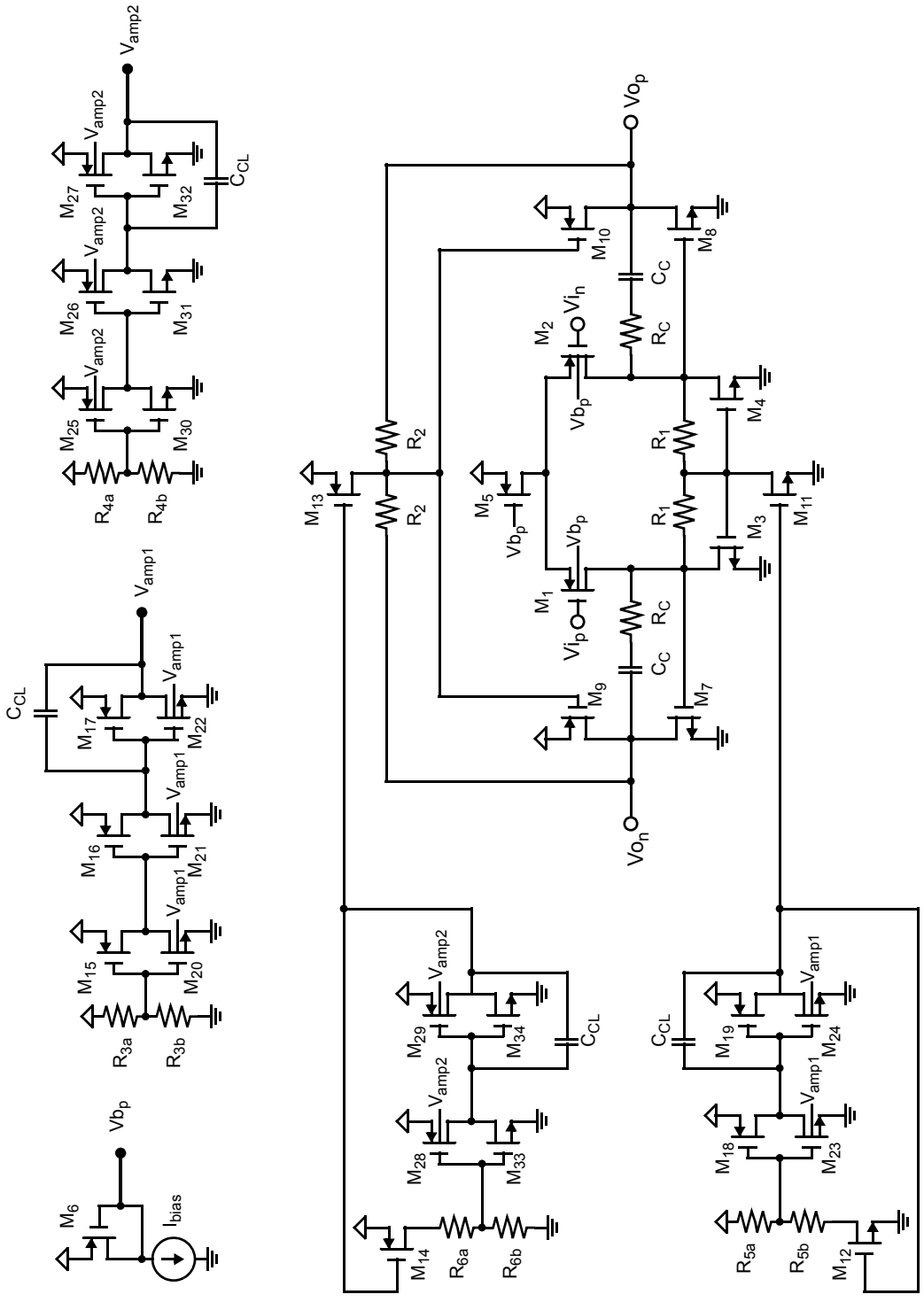

Figure 5.7 Complete circuit-level schematic for the fully-differential 2-stage Opamp with lead compensation [Johns 97] and CMFB [Chatterjee, JSSC05].

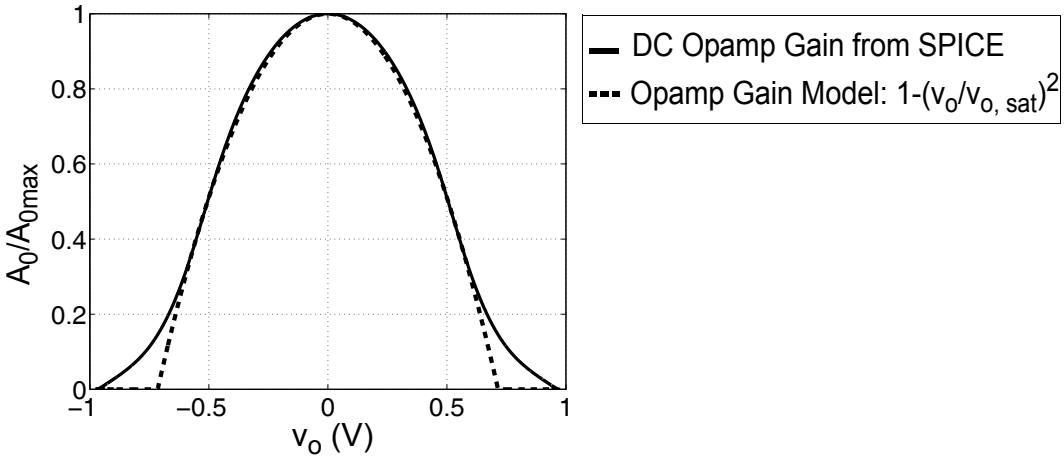

Figure 5.8 Opamp nonlinear dc gain determined from SPICE and from the gain model in (4.15). A_0 is the dc opamp gain, v_o is the output voltage and $v_{o,\,sat}$ is the opamp output saturation voltage. $v_{o,\,sat}$ = 0.7 V.

The bias voltage for the gate of transistor M_{11} is made independent of process and temperature variations by mirroring the drain current of M_{12} into M_{11}. The current through M_{12} is set using the feedback voltage V_{cmfb1} from the difference amplifiers, as shown in Fig. 5.6. These difference amplifiers are based on the inverter amplifier design. They compare their input to their internal switching threshold voltage V_{SW1} and amplify the difference at the output. The switching threshold is set by controlling their bulk biasing voltage, V_{amp1}. This bulk biasing voltage V_{amp1} is generated by using replicas of the difference amplifier in feedback, as shown in 5.6. The full circuit-level opamp schematic, including CMFB circuits, is shown in Fig. 5.7. The capacitors C_{CL} is used to stabilize the negative-feedback loop formed by the difference amplifiers. A similar set of circuits is used to control the output common-mode voltage of the second opamp stage. The advantage of this CMFB circuit is that, unlike traditional CMFB circuits [Johns 97], it does not limit the output swing of the opamps, which is essential for the design of the CT ΔΣ modulator in Fig. 5.1.

The opamp design in Fig. 5.7 is simulated in SPICE to confirm it meets the specifications outlined in Table 5.1. Figure 5.8 shows the nonlinear variation in the opamp's dc gain with respect

to its output voltage. The opamp output saturation voltage $v_{o,\,sat}$ is determined from (4.15) as follows:

Define the opamp output-swing voltage $v_{o,\,swing}$ as:

$$v_{o,\,swing} \equiv v_o\big|_{A\,=\,A_0/2} \tag{5.1}$$

Then, based on (4.15), $$A(v_{o,\,swing}) \;=\; A_0\left(1 - \frac{v_{o,\,swing}}{v_{o,\,sat}}\right)^2 \equiv \frac{A_0}{2} \tag{5.2}$$

$$\Rightarrow \quad v_{o,\,swing} \equiv v_o\big|_{A\,=\,A_0/2} \;=\; \pm\sqrt{2}\; v_{o,\,sat} \tag{5.3}$$

Solving (5.3), using data from SPICE simulations, yields $v_{o,\,sat} \;=\; \sqrt{2}/2$ V. Figure 5.8 plots the opamp gain A versus its output voltage v_o based on an accurate SPICE simulation and based on the model in (4.15). Accordingly, for $|v_o| < v_{o,\,swing}$, the model in (4.15) predicts the actual opamp gain to within $\pm 1.5\%$. Table 5.3 lists the opamp specifications achieved and Table 5.4 lists the transistor sizes, as well as circuit component values, used for each opamp in the $\Delta\Sigma$ loop filter. Process-corner SPICE simulations were performed to confirm proper operation of the opamps.

Specification	Second Opamp	First Opamp
Total load capacitance	4.5 pF	5.5 pF
Total load resistance	30.4 kΩ	N/A
Differential output voltage swing amplitude	700 mV	700 mV
Input and output common mode voltage	450 mV	450 mV
DC gain (with load), A_0	45.8 dB	49.0 dB
Unity-gain frequency, f_t	230 MHz	200 MHz
Phase margin	71.2°	70.3°
Input-referred thermal noise, $\overline{v_{n,\,OTA}^2}$	$1.5 \times 10^{-16}\, V^2/Hz$	$4.5 \times 10^{-16}\, V^2/Hz$
Power consumption (including CMFB)	700 μW	500 μW

Table 5.3 Specifications obtained from SPICE simulations for the opamp in Fig. 5.7.

Opamp 2 (including CMFB)

Transistor Sizes

	$M_{1,2}$	$M_{3,4}$	M_5	M_6	$M_{7,8}$	$M_{9,10}$	$M_{11\text{-}14}$	$M_{15\text{-}19}$
W(μm)	45	6	15	3	6	15	0.12	0.12
L(μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.12	0.06

	$M_{20\text{-}24}$	$M_{25\text{-}29}$	$M_{30\text{-}34}$
W(μm)	0.36	2.4	0.13
L(μm)	0.06	0.06	0.06

Resistor Values

	$R_{1,2}$	R_{3a}	R_{3b}	R_{4a}	R_{4b}	R_{5a}	R_{5b}	R_{6a}	R_{6b}
kΩ	100	11.6	8.4	12	28	20	10.4	4.45	35.4

Capacitor Values

	C_C	C_{CL}
fF	850	100

Opamp 1 (without CMBF)

Transistor Sizes

	$M_{1,2}$	$M_{3,4}$	M_5	M_6	$M_{7,8}$	$M_{9,10}$
W(μm)	15	2	5	1	6.6	16.5
L(μm)	0.18	0.18	0.18	0.18	0.18	0.18

C_C = 350fF

CMFB circuit for Opamp 2 is identical to the one used by Opamp 1

Table 5.4 Circuit component sizes and values used in the design of opamps from Fig. 5.7.

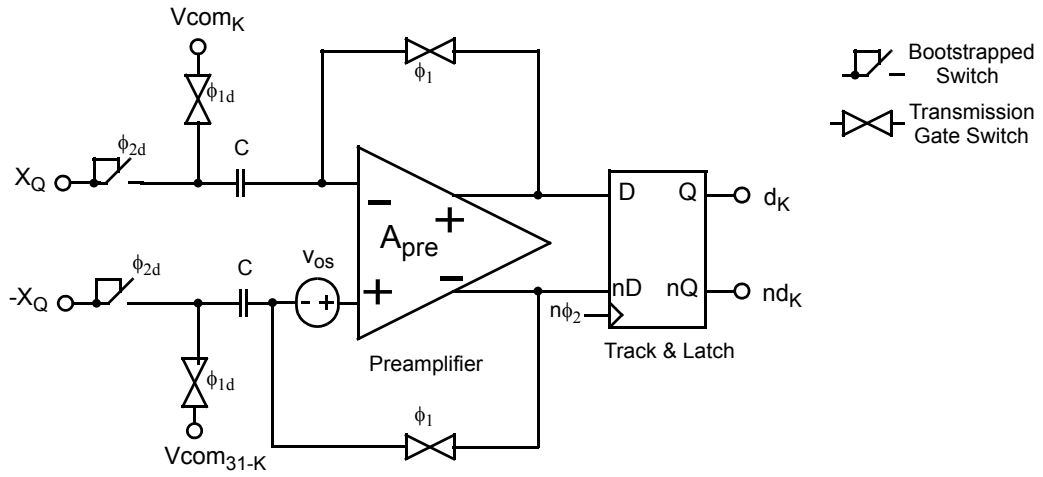

Figure 5.9 Comparator unit cell with input-offset storage, preamplifier and track-and-latch [Gregorian 99].

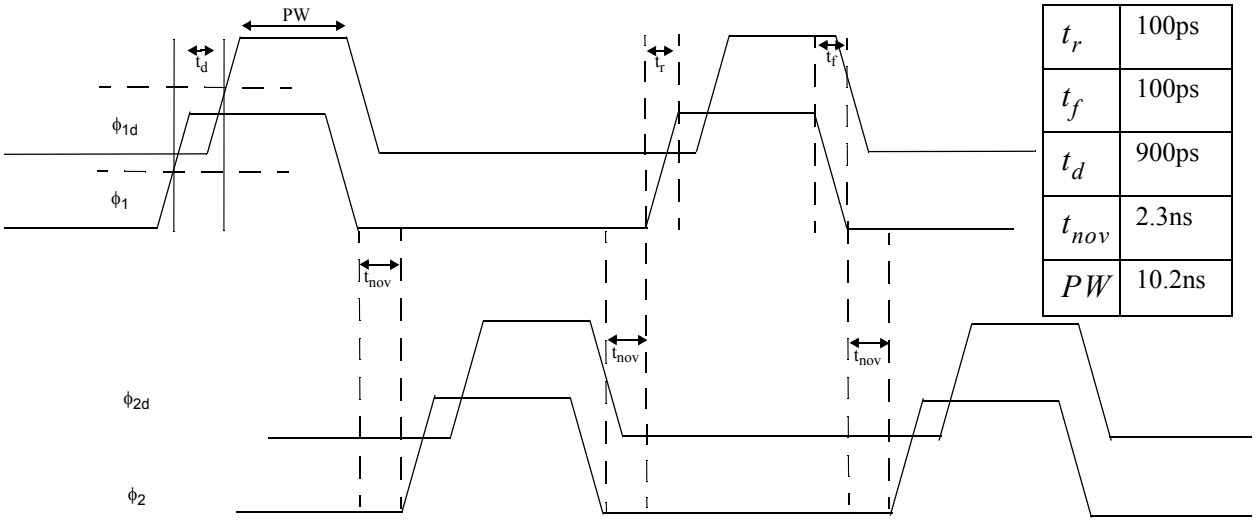

Figure 5.10 Four phase non-overlapping clocking scheme for comparator in Fig. 5.9.

5.5 Comparator Design

The comparator used in the design of the 5-bit quantizer in Fig. 5.1 is shown in Fig. 5.9. It utilizes the input-offset storage method to minimize the effects of the preamplifier offset voltage v_{os} [Razavi, JSSC92]. This offset arises due to transistor mismatches and process variations. The capacitor used to store the preamplifier offset voltage needs to be kept small to minimize the load on the preceding opamp. However, a small capacitor would introduce more kT/C noise and so its

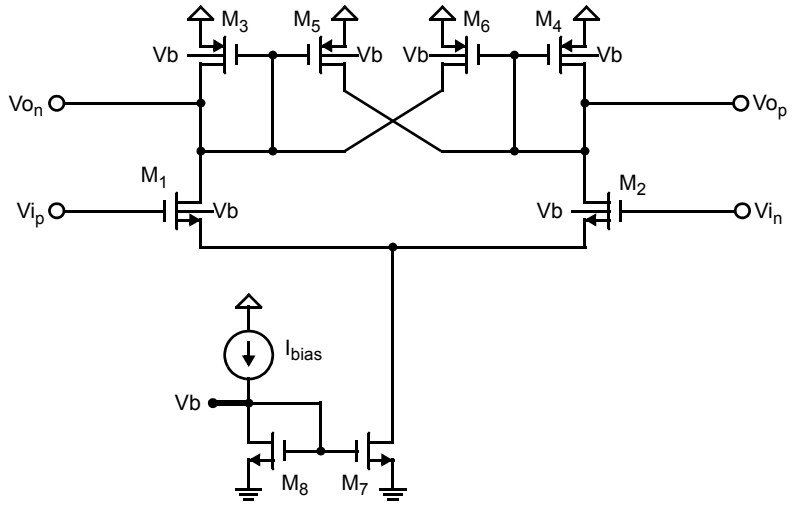

Figure 5.11 Preamplifier circuit for the comparator in Fig. 5.9 [Gregorian 99, Fig. 5.16].

size needs to be carefully determined. A 75fF capacitor is used in the comparator in Fig. 5.9. The sampling switches at the input of the comparator in Fig. 5.9 are bootstrapped [Dessouky, JSSC01] because they are in the signal path, and see a full-scale signal (500 mV). NMOS switches are not used here because they would introduce too much signal-dependent errors (due to nonlinear on resistance). Transmission gates offer constant on resistance in the region $V_{DD} - (V_{th,n} + V_{th,p})$, however, with a 1-V supply voltage, this region is less than 200mV and therefore cannot be used at the comparator input. However, transmission-gate switches are used in the paths that do not see the full signal swing, as shown in Fig. 5.9. The comparator utilizes a four-phase clocking scheme to minimize charge injection errors [Johns 97], shown in Fig. 5.10. The following subsections describe the design of the preamplifier, bootstrapped switch, transmission-gate switch and latch.

5.5.1 Preamplifier

The circuit-level implementation of the preamplifier used in the comparator of Fig. 5.9 is shown in Fig. 5.11 [Gregorian 99, Fig. 5.16]. It consists of an input differential pair ($M_{1,2}$) with a diode connected load ($M_{3,4}$). The transistors M_5 and M_6 are used to increase the amplifier gain by introducing a negative transconductance at the amplifier output. The bulks of the transistors M_1-M_6 are slightly forward biased to reduce their threshold voltage V_{th} to ensure that all transistors

operate within the saturation region [Chatterjee, JSSC05]. SPICE simulations were used to determine $v_{o,\,sat}$ for the preamplifier and was found to be 500mV. This was determined by plotting the preamplifier's dc gain A_{pre} versus its output voltage v_o, as shown in Fig 5.12. Curve fitting was used to estimate $v_{o,\,sat}$ using the opamp nonlinear dc gain model in (4.15) as described in Section 5.4. SPICE was also used to perform a monte-carlo analysis to determine the **input-referred RMS offset voltage** $\boldsymbol{v_{os,\,RMS}}$, introduced due to mismatch and process variations in the transistor widths as well as in their threshold voltages. As shown in Fig. 5.13, the input-referred RMS offset voltage is 50mV when using minimum sized transistors. Each data point $v_{os,\,RMS}$ in Fig. 5.13 is obtained by plotting several v_o versus v_{in} graphs in a SPICE monte-carlo simulation (for the preamplifier in Fig. 5.11) and then computing the RMS value of the points $v_{in}\big|_{v_o\,=\,0}$ for all the graphs. This offset voltage can be reduced by increasing the transistor sizes. However, to maintain transistor operation in the saturation region and to maintain a given transistor overdrive voltage ($v_{ov} = v_{GS} - v_{th}$), the preamplifier bias current, and, hence, power consumption needs to be increased.

As explained in [Razavi, JSSC92], the **effective input-referred offset voltage** $\boldsymbol{v'_{os}}$ for the comparator in Fig. 5.9 is $v'_{os} = v_{os}/A_{pre}$, where $\boldsymbol{v_{os}}$ is the **preamplifier input-referred offset**. To maintain the quantizer accuracy, this effective input-referred offset needs to be less then half the minimum quantizer step size Δ: i.e., $v'_{os} < \Delta/2$ [Doernberg, JSSC89] [Gregorian 99]. The quantizer reference voltage V_{REF} is set equal to the integrator output saturation voltage (700mV) and so quantizer step size $\Delta = (2V_{REF})/M = 45mV$.

When a worst-case effective input-referred offset $v'_{os,\,worst}$ is assumed to be $v'_{os,\,worst} = v_{os,\,RMS}$ (i.e., a 1-σ error is assumed), then $A_{pre} = 2.2$ V/V is sufficient to reduce v'_{os} to less than $\Delta/2$ and, hence, a single preamplifier stage is sufficient for proper comparator functionality. However, in order to amplify the minimum input signal $(X_Q - V_{com_k})\big|_{min} = \Delta/2$ up to the switching threshold of the track-and-latch, a gain of $A_{pre} = 3.6$ V/V is required (as determined by SPICE simulations). Thus, when a 1-σ error is assumed, the transistors can be set to minimum size to minimize power consumption. Table 5.5 lists the transistor sizes used to implement the preamplifier and Table 5.6 lists its specifications obtained from SPICE simulations.

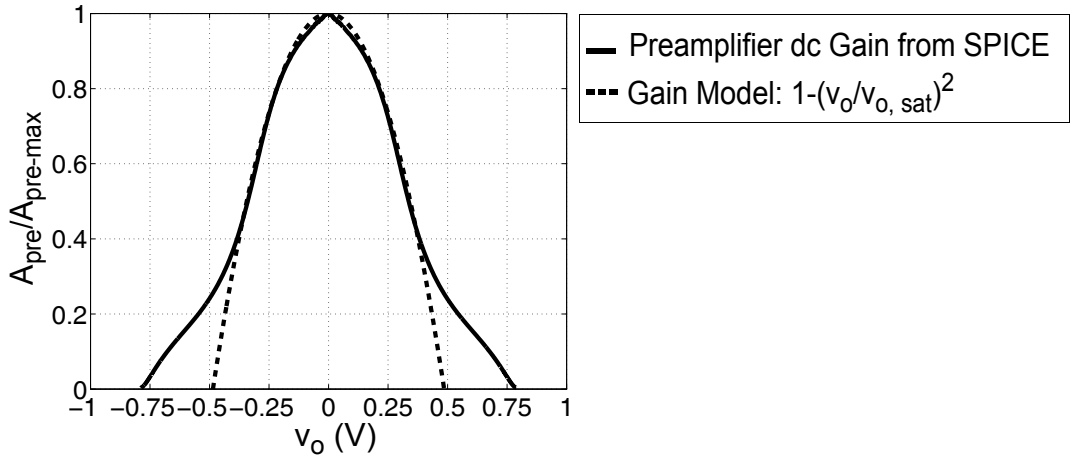

Figure 5.12 Nonlinear dc gain A_{pre} for the preamplifier in Fig. 5.11, determined from SPICE. v_o is the output voltage and $v_{o,\,sat}$ is the output saturation voltage.

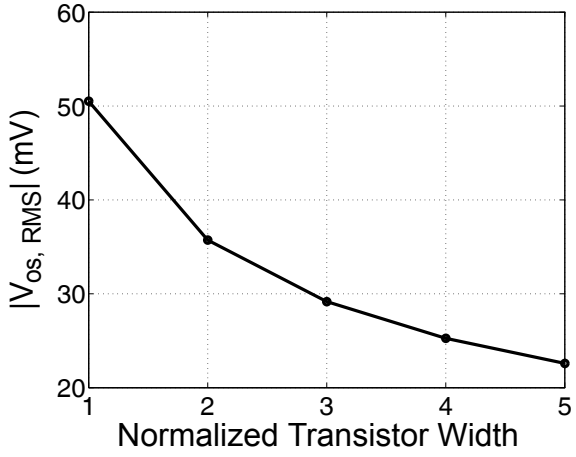

Figure 5.13 Absolute input-referred RMS offset voltage $v_{os,\,RMS}$ for the preamplifier in Fig. 5.11. A normalized transistor width of 1 corresponds to a min-sized transistor. The monte-carlo simulations performed in SPICE included mismatch and process variations in the transistor widths as well as their threshold voltages.

	$M_{1,2}$	$M_{3,4}$	$M_{5,6}$	M_7	M_8
W(μm)	0.12	0.16	0.12	0.24	0.12
L(μm)	0.06	0.18	0.18	0.06	0.06

Table 5.5 Transistor sizes used in the design of the preamplifier in Fig. 5.11.

Preamplifier Specification	Value
Differential output voltage swing amplitude	500 mV
Input and output common mode voltage	550 mV
Input-referred RMS offset voltage, $v_{os,\,RMS}$	50 mV
DC gain, A_{pre}	3.6 V/V
Power consumption	30 μW

Table 5.6 Specifications of the preamplifier in Fig. 5.11, obtained from SPICE simulations.

When a worst-case preamplifier input-referred offset is assumed to be $v'_{os,\,worst} = 3v_{os,\,RMS}$ (i.e., a 3-σ error is assumed), then an $A_{pre} = 6.7$ V/V is required. Alternatively, the widths of the transistors, used to implement the single-stage preamplifier in Fig. 5.11, can be increased by a factor of 4 (determined from Fig. 5.13) to reduce the preamplifier offset voltage. However, to maintain transistor operation in the saturation region and to maintain a given transistor overdrive voltage ($v_{ov} = v_{GS} - v_{th}$), the preamplifier bias current, and, hence, power consumption need to be increased by approximately a factor of 4 (to about 120μW).

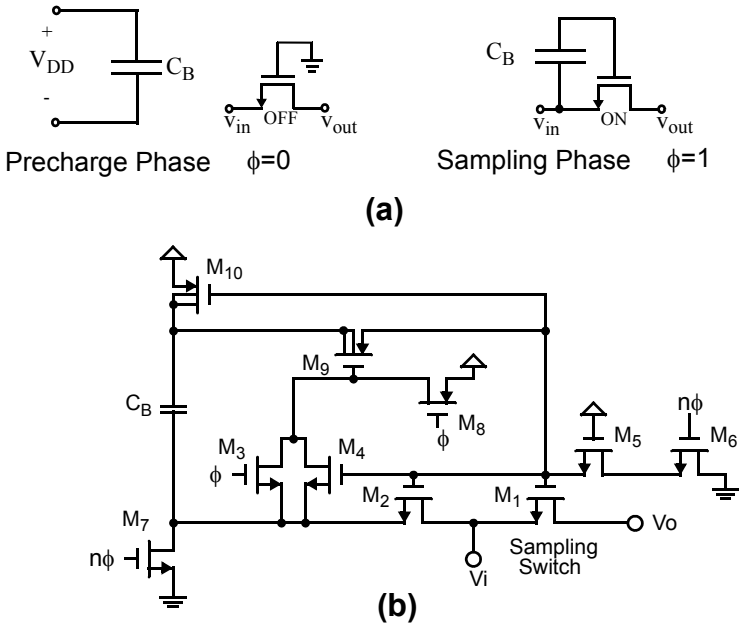

Figure 5.14 Bootstrapped switch design for the comparator in Fig. 5.9: **(a)** Conceptual diagram depicting its operation; **(b)** Circuit-level implementation [Dessouky, JSSCC01].

	M_1	$M_{2\text{-}7}$	$M_{8\text{-}10}$
W(μm)	0.24	0.12	0.12
L(μm)	0.06	0.06	0.06

C_B = 75 fF

Table 5.7 Transistor sizes used in the design of the bootstrapped switch in Fig. 5.14.

5.5.2 Bootstrapped Switch

A conceptual diagram of the operation of a bootstrapped switch is shown in Fig. 5.14a. During the precharge phase, the capacitor (C_B) is pre-charged to V_{DD}. During the sampling phase, this capacitor C_B is connected between the gate and source terminals of the sampling NMOS switch. Thus, during the sampling phase, the NMOS sampling switch has a constant gate-to-source voltage v_{GS} and hence, an approximately constant on resistance. The circuit implementation of the bootstrapped switch is shown in Fig. 5.14b [Dessouky, JSSCC01] and Table 5.7 lists the

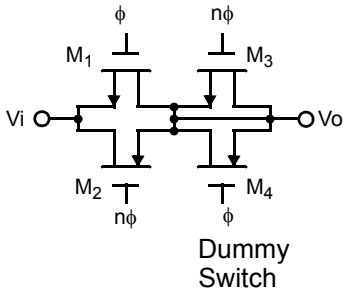

Figure 5.15 Transmission-gate switch for the comparator in Fig. 5.9, including dummy structure to reduce charge injection errors.

	M_1	M_2	M_3	M_4
W(μm)	0.24	0.32	0.12	0.16
L(μm)	0.06	0.06	0.06	0.06

Table 5.8 Transistor sizes used in the design of the transmission-gate switch in Fig. 5.15.

component sizes and values used. SPICE simulations were used to confirm that the switch introduced a total-harmonic distortion (THD) of *THD* = -85dB (up to the 7th harmonic) for a full-scale peak-to-peak input $V_{in,\ p\text{-}p}$ = 500mV at $f_{in} = f_{BW}/10$.

5.5.3 Transmission-gate Switch

The transmission-gate switch is shown in Fig. 5.15. Transistors M_1 and M_2 form the actual switch, while transistors M_3 and M_4 form a dummy structure to minimize the charge-injection and clock-feedthrough errors [Razavi 01]. When M_1 and M_2 turn off, they release excess charge that is absorbed by M_3 and M_4 when they turn on. Table 5.8 lists the transistor sizes used to implement the transmission-gate switches. SPICE simulations were used to confirm that the switch introduced a THD of *THD* = -80 dB (up to the 7th harmonic) for a peak-to-peak input $V_{in,\ p\text{-}p}$ = 250mV at $f_{in} = f_{BW}/10$.

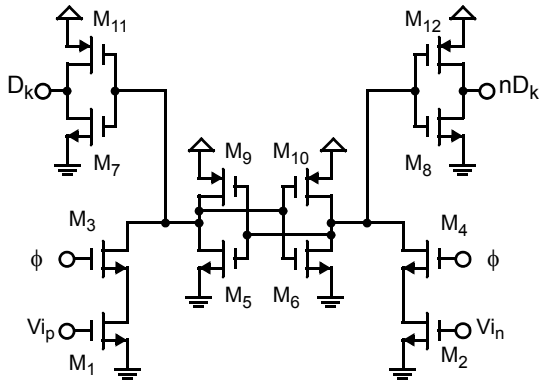

Figure 5.16 Ratioed CMOS Latch for the comparator in Fig. 5.9 [Rabaey 03, Fig. 7-21].

	$M_{1\text{-}4}$	$M_{5\text{-}8}$	$M_{9\text{-}12}$
W(μm)	0.36	0.12	0.16
L(μm)	0.06	0.06	0.06

Table 5.9 Transistor sizes used in the design of the ratioed CMOS latch in Fig. 5.16.

5.5.4 Track and Latch

The track-and-latch in Fig. 5.9 is used to amplify the output of the preamplifier up to the voltage rail, using cross-coupled inverters, as shown in Fig. 5.16 [Rabaey 03, Fig. 7-21]. The cross-coupled inverters ($M_{5,9}$ and $M_{6,10}$) are driven from one state into another using the pull-down network $M_{1\text{-}4}$. The size of the pull-down network needs to be large enough to drive the inverters into its proper state in less than half a sampling clock cycle: $\phi < f_S/2$. The inverters $M_{7,11}$ and $M_{8,12}$ are used to buffer the latch output. The transistor sizes used to implement the latch is listed in Table 5.9.

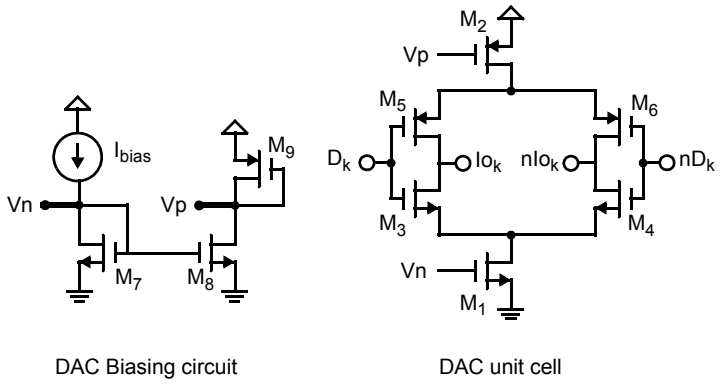

Figure 5.17 DAC unit cell and biasing circuit for NRZ current-mode feedback in Fig. 5.1.

	M_1	M_2	$M_{3\text{-}4}$	$M_{5\text{-}6}$	M_7	M_8	M_9
W(μm)	0.12	0.24	0.12	0.24	0.12	0.12	0.24
L(μm)	0.18	0.18	0.06	0.06	0.18	0.18	0.18

Table 5.10 Transistor sizes for DAC unit cell with biasing circuit in Fig. 5.17.

5.6 DAC Design

The fully-differential DACs in Fig. 5.5 output currents with non-return-to-zero pulse. They consist of current sources controlled by simple NMOS switches as shown in Fig. 5.17 [Breems, JSSC04]. Each DAC consists of 31 unit elements, corresponding to a 5-bit (31-level) quantizer. The DAC elements need to drive a current pulse with a magnitude:

$$I = (V_{in,\,max}/\mathrm{R})/M = (500\mathrm{mV}/7.6\mathrm{k}\Omega)/31 = 2.1\mu\mathrm{A}. \tag{5.4}$$

where $V_{in,\,max}$ is the maximum input-signal swing amplitude. The NMOS switches are sized such that the current source remains in saturation region when the switch is on. Table 5.10 lists the sizes for the transistors used to implement each DAC element. Data-weighted averaging (DWA) techniques can be used to reduce DAC errors [Hamoui, TCASI04].

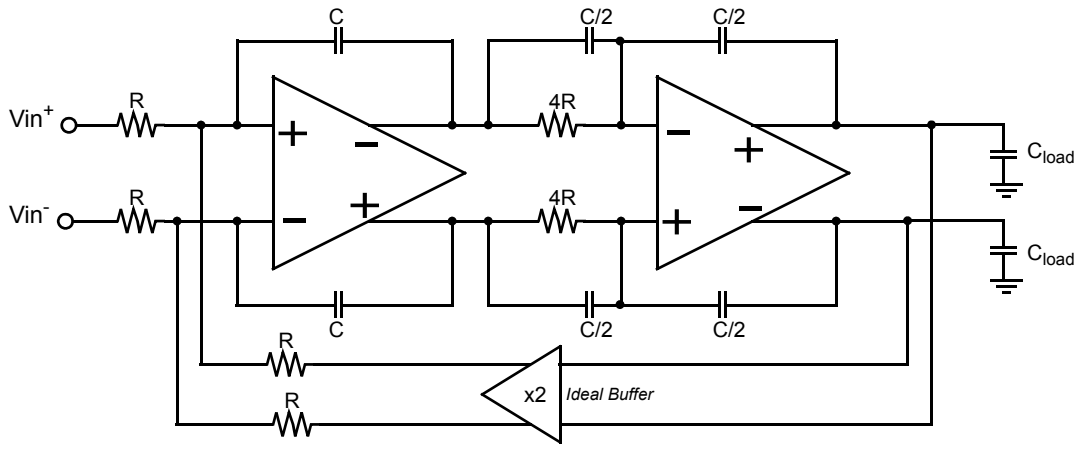

Figure 5.18 Loop filter $H(s)$ for the NTF-enhanced 2nd-order CT ΔΣ modulator in Fig. 5.1, including output-level scaling.

5.7 SPICE Simulation Results

5.7.1 Loop Filter *H*(*s*)

The loop filter $H(s)$ for the NTF-enhanced 2nd-order feedforward CT ΔΣ modulator in Fig. 5.1 is shown in Fig. 5.18. It is implemented using the designed opamps (Table 5.4) and is simulated in SPICE to confirm that it meets the linearity requirements for 12-bits of SNDR resolution. The over-sampling ratio (OSR) is set to 20, the pole s_p of the NTF-enhancement filter $G_1(s)$ was set to $s_p = -3f_S$. The unity-gain frequency ω_{ta} for Integ. 1 and Integ. 2 was $6\pi f_S$ and $4\pi f_S$ respectively, the dc gain for Integ. 1 and Integ. 2 was $A_{0\max} = 50$ dB and $A_{0\max} = 45$ dB respectively and the opamp output saturation voltage was $v_{o,\,sat} = 1/\sqrt{2}$. A sinusoidal input signal with amplitude $V_{in} = -3.1$ dBFS and frequency $f_{in} = 110$ kHz $(= f_{BW}/10)$ was applied at the input of the loop filter $H(s)$. The total-harmonic distortion (THD) (up to the 7th harmonic) is *THD* = -90dB.

5.7.2 NTF-Enhancement Filter $G_1(s)$

The NTF-enhancement filter $G_1(s)$ for the NTF-enhanced 2nd-order CT ΔΣ modulator in Fig. 5.1 is used to enhance the NTF for a 1st-order CT ΔΣ modulator with 1-bit quantizer as shown

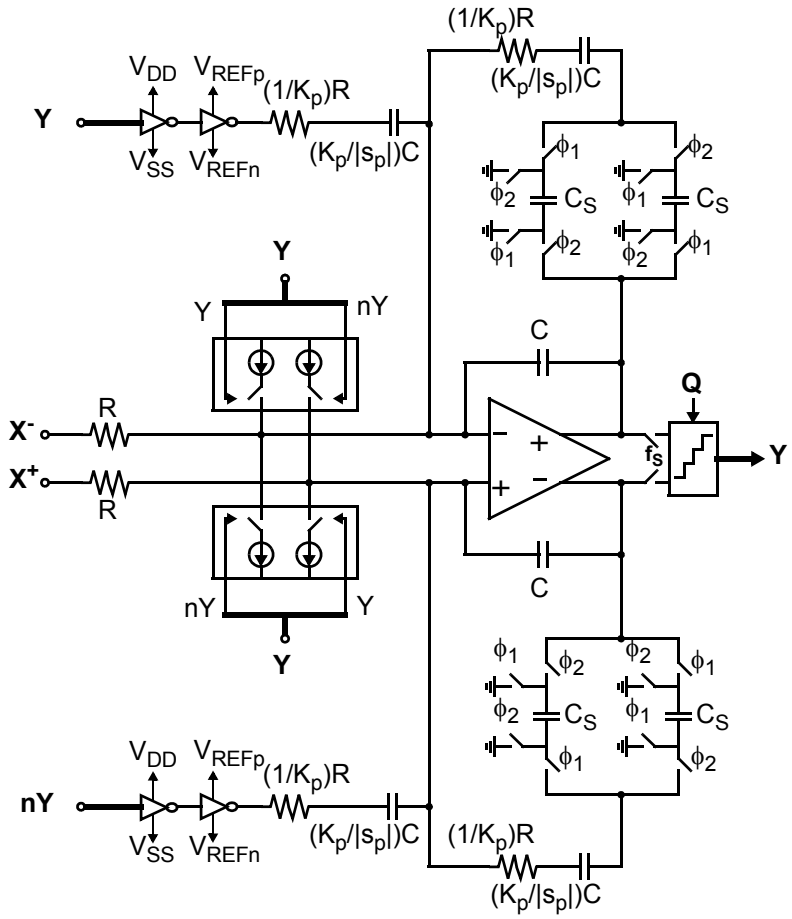

Figure 5.19 Circuit implementation of NTF-enhanced 1st-order CT ΔΣ modulator with 1-bit quantizer and passive S&H, used to verify the functionality of the NTF-enhancement filter $G_1(s)$ in Fig. 5.1. Here, excess-loop-delay is not included.

in Fig. 5.19. Excess-loop-delay compensation is not included for simplicity. The entire system in Fig. 5.5 is not simulated because of the intractable memory and time requirements. For the circuit in Fig. 5.19, the OSR was set to 20, pole s_p of the NTF-enhancement filter $G_1(s)$ was set to $s_p = -3f_S$. The unity-gain frequency for the integrator was $\omega_{ta} = 6\pi f_S$ and opamp dc gain was $A_0 = 50$ dB. A sinusoidal input signal with amplitude $X = -3.1$ dBFS and frequency $f_{in} = 110$ kHz ($=f_{BW}/10$) was applied at the input. The quantizer reference voltage is set equal to the opamp output saturation voltage $V_{REF} = v_{o,sat} = 1/\sqrt{2}$ V. Figure 5.20 shows the output power-spectral density (PSD) for the NTF-enhanced 1st-order CT ΔΣ modulator and Table 5.11

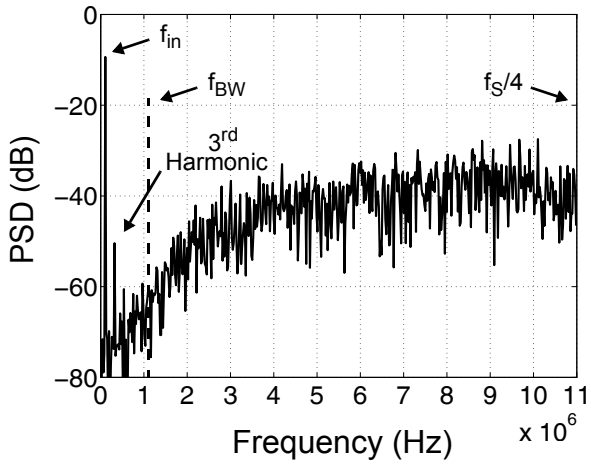

Figure 5.20 Output power spectral density (PSD) for the NTF-enhanced CT ΔΣ modulator in Fig. 5.19.

SNDR Performance	SIMULINK	SPICE
Without G(s)	35.3dB	35.0dB
With G(s)	42.3dB	41.3 dB

Table 5.11 SNDR performance comparison between SIMULINK and SPICE for the CT ΔΣ modulator in Fig. 5.19.

lists its SNDR performance compared to behavioral simulations in SIMULINK. Simulation results from SPICE show that, when the proposed NTF-enhancement technique is used to enhance the noise-shaping performance of the 1st-order CT ΔΣ modulator, an improvement of nearly 1 bit of SNDR resolution is observed, which closely matches the results predicted by SIMULINK behavioral simulations.

Chapter 6

Conclusion

Modern broadband digital communication applications demand high-speed, high-resolution and low-power ADCs built in standard digital CMOS processes for higher system integration and lower fabrication costs [Hamoui 04]. Continuous-time (CT) ΔΣ modulators are being used increasingly to meet these demands, owing to their potential for low-power high-speed A/D conversion [Huang, ISSCC09] [Yang, ISSCC08] [Mitteregger, JSSC06], suppression of sampling errors, and implicit anti-aliasing filtering [Peev, ICECS08] [Keller, TCASI07], in spite of their drawbacks, including high sensitivity to clock jitter [Chopp, TCASI09] [Reddy, TCASI07] and their need for tuning circuitry to maintain modulator stability.

This thesis developed a technique to design high-order feedforward CT ΔΣ modulators with noise-transfer-function (NTF) enhancement. This technique increases the noise-shaping order of an N^{th}-order CT ΔΣ modulator by one, thus matching the noise-shaping performance of a classical $(N+1)^{th}$-order CT ΔΣ modulator, while maintaining the stability characteristics of a classical N^{th}-order CT ΔΣ modulator. Hence, the proposed NTF-enhancement technique relaxes the accuracy requirements on the coefficient-tuning circuitry needed to maintain modulator stability. Furthermore, the NTF-enhanced ΔΣ modulator has greater potential for low-power design than its equivalent classical ΔΣ modulator, owing to the reduced gain-bandwidth requirements for the opamp used to implement the last integrator in the ΔΣ loop filter. Moreover, the proposed NTF-enhancement technique can be implemented using a passive filter, a passive sample-and-hold, and a DAC, thereby requiring minimal additional power.

The proposed NTF-enhancement technique is implemented in a capacitive-feedforward CT ΔΣ modulator, owing to the potential for low-power design and good control over the modulator coefficients of this architecture [Schimper, ESSCIRC04]. Behavioral models are developed in SIMULINK and behavioral simulation results show the increased noise-shaping and stability advantage achieved by using the proposed technique. Effects of non-idealities such as thermal noise and opamp distortion are also studied. Dynamic-range scaling is used to alleviate the performance limitations, imposed due to high input-referred thermal noise and low supply voltage.

An NTF-enhanced 2^{nd}-order feedforward CT ΔΣ modulator is designed in a 1-V, 65-nm digital CMOS technology. SPICE simulations confirm that this modulator can achieve a 12-bit SNDR over a 1.1-MHz bandwidth. Its main circuit blocks (opamps, comparators and current-steering DACs) are also simulated individually in SPICE to demonstrate that they meet the system specifications.

For operation at low-supply voltages, wide-swing CMBF circuits with automatic on-chip biasing are used to control the output common-mode voltages of the opamps. Furthermore, transistor bulk biasing is used to reduce the threshold voltages of the MOSFETs and ensure that they operate in the saturation region [Chatterjee, JSSC05].

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