Towards Design of Power-Efficient and Cost-Effective Optical Interconnect for Short-Reach Applications

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Abstract

The ever-growing demand for bandwidth in data centers and supercomputers has significantly increased the need for high-speed, low-cost, and energy-efficient short-range optical interconnects. This thesis presents several research outcomes towards designing energy-efficient and cost-effective short-reach optical interconnects. First, it studies existing hardware implementations of optical soft-decision forward error correction (SD-FEC) receivers in the literature. Then, it presents a novel methodology for analyzing the decoding performance of multi-branch configurations of SD-FEC receivers. The proposed methodology allows prediction of the impact of a receiver's configuration on its decoding performance.

Second, it explores vertical germanium photodetectors and short wavelength silicon photodetectors (Si-PDs) to develop power-efficient high-speed photodetectors. It details an innovative methodology for maximizing the responsivity of a high-speed vertical Ge-PD. The resulting Ge-PD provides a responsivity of 1.09 A/W at 1550 nm, a dark current of 3.5 μA, and bandwidth of 42.5 GHz at 2 V reverse-bias voltage. Further, it demonstrates the design, fabrication, and measurement results of four novel grating-assisted silicon photodetectors (Si-PD) for 850 nm applications fabricated in silicon-on-insulator (SOI) technology. The optimized design of the grating-assisted Si-PD has a responsivity of 0.3 A/W, an avalanche gain of 6, a dark current of 2 μA, and bandwidth of 16.4 GHz at 14 V reverse-bias voltage. It also shows an open eye diagram at 35 Gb/s data rate, which to the best of our knowledge, is the fastest operation speed reported for this type of detectors.

Third, this thesis presents the design and experimental results of a novel low-power and compact 25 Gb/s optical receiver in 65 nm TSMC technology. It is prototyped with the previously-proposed optimized design of a grating-assisted Si-PD. The proposed optical receiver has a transimpedance gain of 69.4 dBΩ, a bandwidth of 13.6 GHz, and an input-referred noise of 3.28 μA_{rms}. It occupies only 0.0056 mm^2 and consumes 30.8 mW at

1.1 V supply voltage. It has an energy efficiency of 1.23 pJ/bit at 25 Gb/s bit rate with an input sensitivity of 54 μA_{p-p} for bit error rate (BER) of 10^{-12}.

Sommaire

La demande toujours croissante pour de la bande passante dans les centres de données et les superordinateurs a considérablement augmenté la nécessité d'interconnexions optiques à courte portée, à grande vitesse, à faible coût et économes en énergie. Cette thèse présente plusieurs résultats de recherche visant à concevoir des interconnexions optiques à faible portée et rentables. Tout d'abord, les implémentations matérielles des récepteurs optiques de correction d'erreur directe (SD-FEC) disponibles dans la littérature sont étudiées. Ensuite, une nouvelle méthodologie pour analyser les performances de décodage des configurations multi-branches des récepteurs SD-FEC est présentée. La méthodologie proposée permet de prédire l'impact de la configuration d'un récepteur sur ses performances de décodage.

Deuxièmement, les photodétecteurs de germanium verticaux et les photodétecteurs en silicium à courte longueur d'onde (Si-PD) sont explorés pour développer des photodétecteurs à haute vitesse efficaces. En outre, une méthodologie novatrice pour maximiser la réceptivité d'un Ge-PD vertical à grande vitesse est détaillée. Le Ge-PD résultant offre une réactivité de 1.09 A/W à 1550 nm, un courant d'obscurité de 3.5 μA et une bande passante de 42.5 GHz à une tension de polarisation inverse de 2 V. De plus, les résultats de la conception, de la fabrication et de l'évaluation de quatre nouveaux photodétecteurs en silicium assistés par des réseaux (Si-PD) pour des applications à 850 nm et fabriqués par la technologie de silicium sur isolant (SOI) sont démontrés. La conception optimisée du Si-PD assisté par un réseau a une capacité de 0.3 A/W, un gain d'avalanche de 6, un courant d'obscurité de 2 μA et une bande passante de 16.4 GHz à une tension de polarisation inverse de 14 V. Un diagramme de l'œil ouvert à un débit de données de 35 Gb/s, qui, à notre connaissance, est la vitesse de fonctionnement la plus rapide rapportée pour ce type de détecteurs, est également démontré.

Troisièmement, cette thèse présente la conception et les résultats expérimentaux d'un nouveau récepteur optique à faible puissance et compact de 25 Gb/s dans la technologie TSMC à 65 nm. Il est prototypé avec la conception optimisée précédemment proposée du Si-PD assisté par un réseau. Le récepteur optique proposé a un gain de transimpédance de 69.4 dBΩ, une bande passante de 13.6 GHz et un bruit d'entrée de 3.28 μA_{rms}. Il occupe seulement 0.0056 mm2 et consomme 30.8 mW à une tension d'alimentation de 1.1 V. Il a une efficacité énergétique de 1.23 pJ/bit à un débit de 25 Gb/s avec une sensibilité d'entrée de 54 μA_{p-p} pour un taux d'erreur binaire (BER) de 10^{-12} .

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Contents

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List of Acronyms

ADC	analog-to-digital converters.
BER	bit error rate.
BPG	bit pattern generator.
CH	Cherry–Hooper.
CMOS	complementary metal-oxide-semiconductor.
DAC	digital-to-analog converters.
DSP	digital signal processing.
FEC	forward error correction.
FGC	focusing grating coupler.
FSR	free spectral range.
FWHM	full width at half max.
GC	grating coupler.
Ge-PD	germanium photodetector.
HPC	high-performance computing.
IM/DD	intensity modulated/direct detection.
ISI	inter-symbol interference.
LCA	lightwave component analyzer.

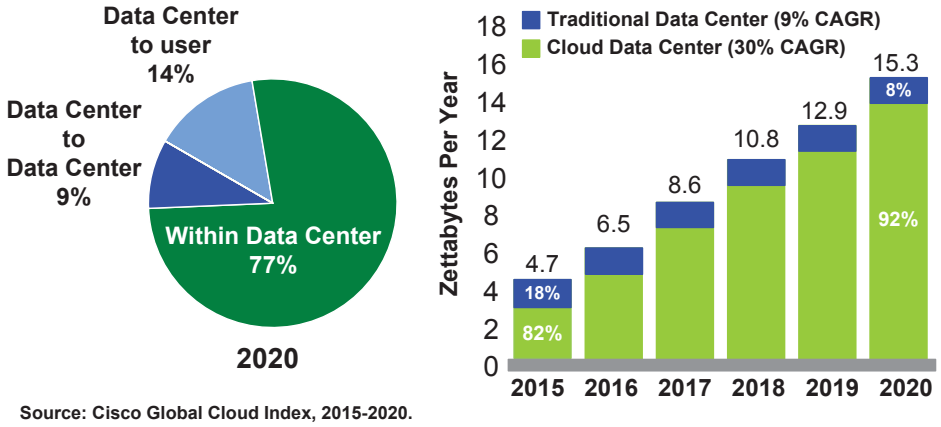
LDPC	low density parity check.
LLR	log-likelihood ratio.
MMF	multi mode fiber.
MOSFET	metal oxide semiconductor field effect transistor.
MPW	multi-project wafer.
NGC	net coding gain.
PA	post-amplifier.
PAM	pulse amplitude modulation.
PC	polarization controller.
PD	photodetector.
PDF	probability distribution function.
PP	power penalty.
PRBS	pseudo random bit sequence.
RGC	regulated cascode.
RIN	relative intensity noise.
RX	receiver.
SD-FEC	soft-decision forward error correction.
Si-PD	silicon photodetector.
SiP	silicon photonics.
SMF	single mode fiber.
SNR	signal-to-noise ratio.
SOI	silicon-on-insulator.
SPA	sum-product algorithm.

TCAD	technology computer-aided design.
TIA	transimpedance amplifier.
TX	transmitter.
VCSEL	vertical cavity surface-emitting laser.
WDM	wavelength division multiplexing.
XNOR	exclusive negative oR boolean logic.

Chapter 1

Introduction

Over the past few years, Internet traffic has been drastically augmented and is expected to increase by nearly three times over the next five years [1]. This growth is the result of expanding use of online high-definition video streaming, video conferences, online games, social networks, mobile Internet, cloud-based storage, and many other bandwidth-intense services. Moreover, the proliferation of new Internet-based services such as Internet of Things (IoT) will further intensify network traffic. According to the Cisco Global Cloud Index [2], by the year 2020, 15.3 zettabytes will be transferred per year. Interestingly, the most of this traffic, i.e., 77%, remains within the data center, while the traffic between data center to data center and data center to the user will be 9% and 14%, respectively (Fig. 1.1) [2]. Also, the growth of cloud computing requires larger and larger scale data centers with thousands of high-speed interconnect links. Optical interconnects have been predominated transmission links for long-distance data transmissions due to low loss and inherently large bandwidth density. With scaling data centers, optical interconnects become even more essential for short-range links inside the data centers [3–5]. Also, the rapid growth of bandwidth requirements in high-performance computing (HPC) systems pushes the need for high-speed optical interconnects for board-to-board and even chip-to-chip



CAGR: compound annual growth rate.

Fig. 1.1 Data center traffic growth and distribution [2].

connections [6–8]. To maintain a reasonable cost and power target for future HPC systems, the off-chip optical interconnect must operate at less than 1 pJ/bit and with costs below 10's of cents/Gbps [6, 7]. In addition, most of the data center applications are free of charge for the end users. Hence, to satisfy the need for rapid growth of bandwidth requirement in data centers and HPC systems, the short-reach interconnects not only require supporting high-speed data transmission but also must be energy-efficient and cost-effective [9]. While multi mode fiber (MMF) with 850 nm wavelength directly modulated vertical cavity surface-emitting lasers (VCSELs) currently dominates the technology used for short-reach optical data communications, single mode fiber (SMF) optical transmission becomes necessary for reach beyond 500 m due in part to modal dispersion, especially as data rates increase.

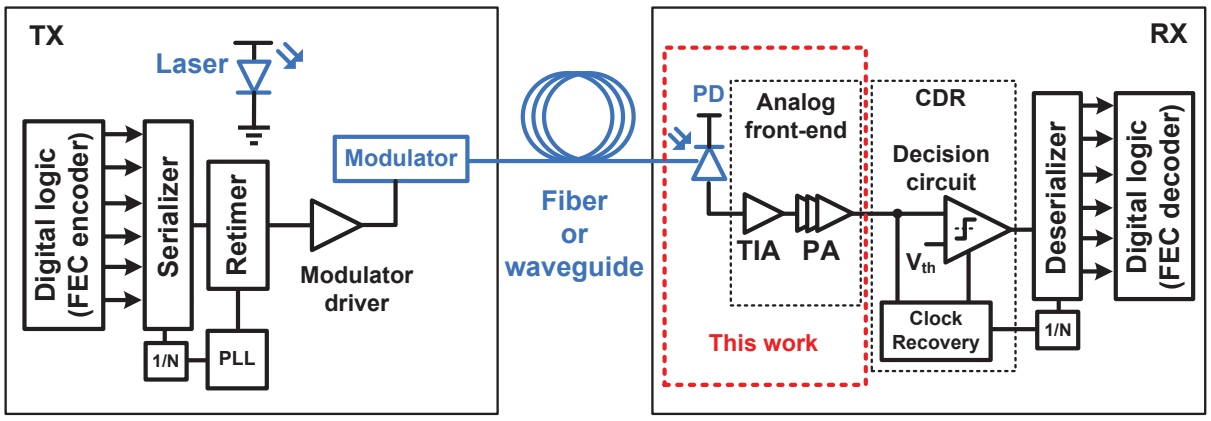
1.1 Motivation

Recent research efforts have focused on scaling current architectures with interconnections operating at 40–100 Gbps to 400–1000 Gbps for the next-generation of optical communication systems [10–14]. Advanced modulation formats such as quadrature phase shift

keying (QPS) and quadrature amplitude modulation (QA) in combination with coherent detection considerably improves the capacity-reach product in long-haul data transmission. The use of high-speed, high-resolution analog-to-digital converterss (ADCs) in coherent-based receivers enables performing powerful digital signal processing (DSP) to mitigate the effects of fiber impairments and improve the overall optical link performance in long-haul applications. Moreover, powerful forward error correction (FEC) codes in combination with soft-decision decoding considerably increase the error tolerance of the transmission link and enable faster and longer optical interconnects [15]. These improvements are achieved at the cost of significantly increasing the cost, complexity, power consumption, and transceiver chip area, which is acceptable for high-capacity long-haul applications.

On the other hand, short-reach optical interconnects must be low cost, power efficient, and compact. These requirements make the coherent detection the least feasible solution for such applications. An intensity modulated/direct detection (IM/DD)-based optical link is a promising low-cost solution for short-reach interconnects. Also, to satisfy the ever-growing bandwidth demands, short-reach optical interconnects are applying previous work done for long-haul links to push system limitations for high-speed data transmission. Employing a wavelength division multiplexing (WDM) scheme [11, 16], advanced modulation schemes with less complexity such as multilevel pulse amplitude modulation (PAM) and, specifically, a PAM-4 modulation scheme [17, 18], use of FEC codes with hard-decision decoding [19] or low-bit soft-decision decoding [20], and low complex digital signal processing [19] are examples of advanced techniques that have been proposed for the next generation of high-speed short-reach optical interconnects.

Figure 1.2 illustrates a simplified example of a short-reach optical link with FEC technique. In the transmitter (TX), a serializer multiplexes low-speed encoded parallel data streams into a high-speed serial data. This data stream drives an optical modulator to modulate the intensity of the continuous-wave light, which is provided by a laser. In the



TX: transmitter; **RX:** receiver circuits; **PLL:** phase lock loop; **FEC:** forward error correction; **TIA:** transimpedance amplifier; **PA:** post-amplifier

Fig. 1.2 Example of a short-reach optical link.

MMF-based optical links, the data stream is applied to a VCSEL through a laser driver and directly modulates the light intensity. The modulated light propagates through a fiber or a waveguide. The insertion loss of the modulator, connectors, and the fiber impairment degrade the received optical power. At the receiver (RX) side, a photodetector (PD) converts the weaken received modulated light into an electrical signal, which is amplified by an analog front end. Then, the decision circuit compares the amplified signal with the threshold level (V_{th}) and the clock and data recovery (CDR) circuits extract the data stream and clock from the received signal. The deserializer demultiplexes the high-speed serial data into parallel bit streams, and then a decoder reproduces the original data. The efficiency of a short-reach optical link can be improved by optimizing the performance of each optical and electrical sub-circuits and also by developing cost-effective and energy-efficient advanced techniques for high-speed data transmission.

This thesis presents a collection of work related to designing an efficient optical interconnect for short-reach applications. It discusses the design, optimization, and test results of sub-components of an optical interconnect such as photodetectors and receiver front

end (red dashed boxes in Fig. 1.2). Also, various hardware implementations of a low-bit soft-decision forward error correction (SD-FEC) optical front-end receiver are studied, and a new performance evaluation analysis is presented, which shows the effect of the front-end configuration on the decoding performance.

1.1.1 Silicon Photonics for High-Speed Short-Reach Interconnects

Over the last decade, silicon photonics (SiP) has attracted significant attention due to the possibility of monolithically integrated silicon-on-insulator (SOI) optical devices with microelectronic circuits using mature, standard, and cost-effective complementary metal-oxide-semiconductor (CMOS) fabrication techniques. The large difference between the refractive indices of the core silicon waveguide and the surrounded glass (SiO_2) enables the dense integration of thousands of optical devices in a single chip. Such integration makes SiP a unique technology solution for the rapid growth of bandwidth required in today's communication systems in data centers and supercomputers [21]. Figure 1.3 shows a cross-section of a typical silicon photonics platform to fabricate grating coupler (GC), waveguide germanium photodetector (Ge-PD), waveguides, optical modulators, and metal oxide semiconductor field effect transistors (MOSFETs) [22]. IBM's 90 nm CMOS photonic technology (CMOS9WG) is an example of a silicon photonics platform, which monolithically integrates optical devices with analog and mixed-signal circuits [23]. Other companies such as Intel, Luxtera, ST Microelectronics, Lightwire/Cisco, and many others have developed their own silicon photonics platforms. Some of these technologies focus on hybrid integrations of optical devices with electrical circuits instead of monolithic integrations.

Currently, commercial 100 Gb/s silicon photonics transceivers are available for 2–10 km using four parallel SMF, each at 25 Gb/s, or using 4×25 Gb/s coarse wavelength division multiplexing (CWDM) on a single SMF [24, 25]. However, to support higher speed, faster and more power-efficient optical interconnect are required [26].

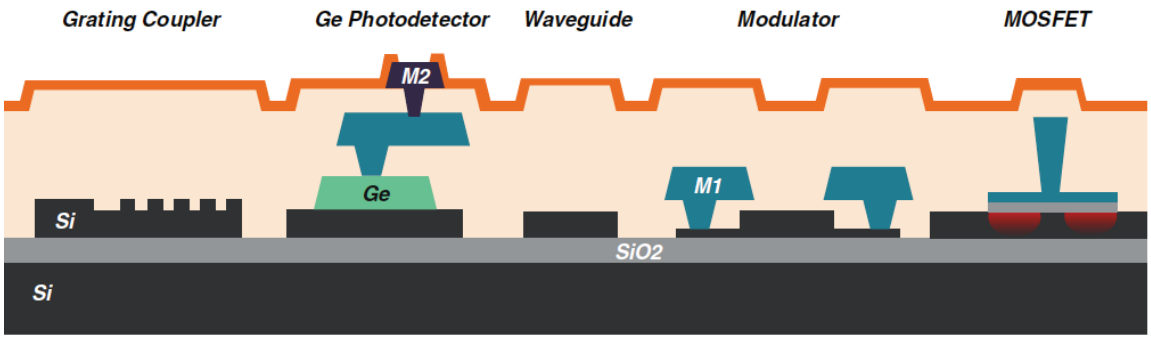


Fig. 1.3 Cross-section of a silicon photonics platform on a silicon-on-insulator wafer [22].

1.2 Thesis Objectives

The primary objective of this thesis is to design low power, cost-effective, and high-speed short-reach optical interconnects for modern data centers. To reach this goal, we have considered research in advance techniques such as FEC as well as performance optimization of optical and electrical sub-circuits in an optical link. We have studied the low-bit soft-decision forward error correction (SD-FEC) technique in an optical link and various hardware implementation of SD-FEC receivers. The novel double-branch 2-bit optical SD-FEC front-end proposed in [27] provides some advantages regarding linearity, bandwidth, optoelectronic integration, power consumption, and cost in comparison with existing SD-FEC front-end [28]. Since the evaluation methodology for SD-FEC decoding performance in the literature is focused on a single-branch configuration, a new evaluation method is required to evaluate the error performance of a multi-branch SD-FEC front end for short-reach applications. Also, silicon photonics (SiP) technology and photodetectors are studied to develop more efficient optical components. We investigated optimizing the performance of vertical waveguide germanium photodetectors (Ge-PDs) for 1550 nm wavelength and silicon photodetectors (Si-PDs) for 850 nm wavelength. For the electrical component level viewpoint, a power-efficient optical receiver front-end in CMOS technology is investigated.

The objectives of this thesis are summarized as follow:

- Study the possible ways of a hardware implementation of an SD-FEC receiver and develop a methodology to evaluate the error performance of multi-branch SD-FEC front-end configurations.
- Explore novel SiP devices for the next generation of high-speed short-link optical interconnects.
  - Optimize performance of vertical waveguide germanium photodetectors (Ge-PD).
  - Optimize performance of silicon photodetectors (Si-PD) for short wavelength applications.
- Investigate a fast and low power optical receiver in CMOS technology and develop an energy-efficient optical receiver for the next generation of high-speed short-link optical interconnects.

1.3 Claim of Originality

The contributions of this dissertation can be summarized in chronological order as follows:

- We present a novel methodology for evaluating the error performance of a multi-branch optical soft-decision forward error correction (SD-FEC) receivers. The noise behavior of three front-end schemes is investigated. A new concept of an inconsistent thermometer code is explained and studied in terms of decoding performance. The proposed methodology and performance comparison is presented for both short-reach optical interconnect and optically amplified long-haul applications. Furthermore, the proposed method is experimentally validated in a short-reach optical link [20, 27, 29].

- We present a complete study of the effect of design geometries of a vertical waveguide germanium photodetector (Ge-PD) and the size and location of the top metal contact on the Ge-PD's performance. A novel methodology is detailed in which to optimize the responsivity and bandwidth of a Ge-PD for a given data rate. Several Ge-PDs were designed and fabricated in commercial silicon photonics (SiP) technology to evaluate the optimization methodology [30].

- We demonstrate the design, fabrication, and experimental results of a novel grating-assisted silicon photodetector (Si-PD) for 850 nm wavelength applications fabricated in silicon-on-insulator (SOI) technology. The proposed grating coupler in the Si-PD enables the fabrication of a photodetector with reasonable responsivity and broad bandwidth. Also, three design variations of the proposed grating-assisted Si-PD for high-speed operation are presented. To the best of our knowledge, we demonstrate the first high-speed Si-PD that operates at 35 Gb/s data rate [31, 32].

- We present the design and measurement results of a novel inductor-less and power-efficient 25 Gb/s optical receiver in 65 nm TSMC technology. The proposed optical receiver is prototyped with the optimized design of the novel Si-PD. The receiver front end occupies only 0.0056 mm^2 and consumes 30.8 mW at 1.1 V supply voltage. For a bit error rate (BER) of 10^{-12}, the optical receiver with a wire-bonded Si-PD has a sensitivity of 46 μA_{p-p} and 54 μA_{p-p} at data rates of 20 and 25 Gb/s, respectively, at a reverse-bias voltage of 0.41 V. The energy efficiency of the all-silicon 850 nm optical receiver is 1.23 pJ/bit at 25 Gb/s data rate [33].

1.3.1 Publications and Contribution of the Author

The content of this dissertation is presented in several publications that include five journal articles, and two conference proceedings. In the following, a list of publications and

contributions of the author are presented. Two journal papers J4 and J5 and conference paper C2 are related to the first research objective, study possible ways of a hardware implementation of an SD-FEC receiver and develop a performance evaluation methodology. The second research objective, which is exploring novel SiP devices, resulted two journal papers and one conference proceeding. Journal paper J3 is related to the research objective of optimizing the performance of a Ge-PD. Journal paper J2 and conference paper C1 are related to the research objective of optimizing the performance of Si-PDs for 850 nm applications. The journal paper J1 is related to the third research objective, which is developing an energy-efficient high-speed optical receiver. Also, the author of this thesis has contributed as a co-author to two patents, one journal paper and four conference proceedings that are not directly related to the content of this thesis.

Patents not Directly Related to This Thesis

- O. Liboiron-Ladouceur, M.S. Hai, **M. Moayedi Pour Fard** (2016). Methods and devices for photonic M-ary pulse amplitude modulation, United States Patent, US20160103382, 18 Oct. 2016.

- O. Liboiron-Ladouceur, M.S. Hai, **M. Moayedi Pour Fard**, C. Zhang, M. Sakib (2015). Methods and systems for board level photonic bridges, United States Patent, US App. 14/955142, 1 Dec. 2015.

Peer-reviewed Journal Articles:

J1) **M. Moayedi Pour Fard**, O. Liboiron-Ladouceur, and G. Cowan, "1.23 pJ/bit 25 Gb/s inductor-less optical receiver with low-voltage silicon photodetector," *submitted to IEEE Journal of Solid State Circuits (JSSC).*

M. Moayedi Pour Fard: Proposed the idea, designed and drew the layout of the de-

vice, performed a complete measurement, and wrote the manuscript.

O. Liboiron-Ladouceur: Supervised the work, edited and reviewed the manuscript.

G. Cowan: Supervised the work, edited and reviewed the manuscript.

J2) **M. Moayedi Pour Fard**, C. Williams, G. Cowan, and O. Liboiron-Ladouceur, "High-speed grating-assisted all-silicon photodetector for 850 nm applications," *Optics Express*, vol. 25, no. 5, pp. 5107-5118, March 2017.

The initial idea of the proposed device was developed in a group meeting.

M. Moayedi Pour Fard: Proposed high-speed design variation of the device, designed the optical grating coupler for 850 nm, supervised the design of p-i-n diode, wrote a script that generates the layout of the photodetector for various design parameters, performed a complete measurement on the devices, and wrote the manuscript.

C. Williams: Designed the p-i-n diodes, drew the layout of the devices, and reviewed the manuscript.

G. Cowan: Supervised the work, edited and reviewed the manuscript.

O. Liboiron-Ladouceur: Supervised the work, edited and reviewed the manuscript.

J3) **M. Moayedi Pour Fard**, G. Cowan, and O. Liboiron-Ladouceur, "Responsivity optimization of a high-speed germanium-on-silicon photodetector," *Optics Express*, vol. 24, no. 24, pp. 27738-27752, November 2016.

M. Moayedi Pour Fard: Proposed the idea, designed and drew the layout of the devices, performed a complete measurement, and wrote the manuscript.

G. Cowan: Supervised the work, edited and reviewed the manuscript.

O. Liboiron-Ladouceur: Supervised the work, edited and reviewed the manuscript.

J4) **M. Moayedi Pour Fard**, G. Cowan, and O. Liboiron-Ladouceur, "Analysis of low bit soft-decision error correction in optical front-ends," *Journal of Optical Communications and Networking (JOCN)*, vol. 7, no. 9, pp. 885-897, September 2015.

M. Moayedi Pour Fard: Wrote a MATLAB code to analysis the front-ends, verified the analysis with measurements, and wrote the manuscript.

G. Cowan: Supervised the work, edited and reviewed the manuscript.

O. Liboiron-Ladouceur: Supervised the work, edited and reviewed the manuscript.

J5) M. N. Sakib, **M. Moayedi Pour Fard**, W. J. Gross, and O. Liboiron-Ladouceur, "A 45 Gb/s low complexity optical front-end for soft-decision LDPC decoders," *Optics Express*, vol. 20, no. 16, pp. 18336-18347, July 2012.

M. N. Sakib: Designed and tested the front-end and wrote the manuscript.

M. Moayedi Pour Fard: Helped M. N. Sakib with part of the MATLAB code to make the frame capturing more efficient, and reviewed the manuscript.

W. J. Gross: Supervised the work and reviewed the manuscript.

O. Liboiron-Ladouceur: Supervised the work, and edited and reviewed the manuscript.

Peer-reviewed Conference Papers:

C1) **M. Moayedi Pour Fard**, C. Williams, G. Cowan, and O. Liboiron-Ladouceur, "A 35 Gb/s silicon photodetector for 850 nm wavelength applications," *IEEE Photonics Conference (IPC)*, PD2 (post-deadline paper), September 2016.

M. Moayedi Pour Fard: Designed the optical grating coupler for 850 nm, supervised the design of p-i-n diode, wrote a script that generates the layout of the photodetector for various design parameter, performed a complete measurement on the device, wrote the manuscript and prepared the slides for the presentation.

C. Williams: Designed the p-i-n diodes, drew the layout of the devices, and reviewed the manuscript.

G. Cowan: Supervised the work, edited and reviewed the manuscript.

O. Liboiron-Ladouceur: Supervised the work, edited and reviewed the manuscript,

and presented the paper at the conference.

C2) M. N. Sakib, **M. Moayedi Pour Fard**, and O. Liboiron-Ladouceur "A 45 GS/s optical soft-decision front-end," *IEEE Photonics Conference (IPC)*, paper WM4, October 2012.

M. N. Sakib: Designed and tested the front-end, wrote the manuscript and presented the paper at the conference.

M. Moayedi Pour Fard: Helped M. N. Sakib with part of the MATLAB code to make the frame capturing more efficient, reviewed and edited the manuscript.

O. Liboiron-Ladouceur: Supervised the work, edited and reviewed the manuscript.

Peer-reviewed Journal Articles Not Directly Related to This Thesis:

1) M. S. Hai,* **M. Moayedi Pour Fard**,* O. Liboiron-Ladouceur, "A ring-based 25 Gb/s DAC-less PAM-4 modulator," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 22, no. 6, November 2016 (***equal contribution**).

Peer-reviewed Conference Articles Not Directly Related to This Thesis:

1) **M. Moayedi Pour Fard**, M. S. Hai, and O. Liboiron-Ladouceur, "A compact 25 Gb/s Mach-Zehnder assisted ring modulator," *Photonics North Conference (PN)*, May 2016.

2) M. S. Hai, **M. Moayedi Pour Fard**, D. An, F. Gambini, S. Faralli, G. Preve, G. W. Roberts, and O. Liboiron-Ladouceur, "Automated characterization of SiP MZI-based switches," *Optical Interconnects Conference (OI)*, pp.94-95, April 2015.

3) F. Lou, **M. Moayedi Pour Fard**, P. Liao, M. S. Hai, R. Priti, Y. Huangfu, C. Qiu, Q. Hao, Z. Wei, O. Liboiron-Ladouceur, "Towards a centralized controller for

silicon photonic MZI-based interconnects," *Optical Interconnects Conference (OI)*, pp.146-147, April 2015.

4) M. S. Hai, **M. Moayedi Pour Fard**, and O. Liboiron-Ladouceur, "A low-voltage PAM-4 SOI ring-based modulator," *IEEE Photonics Conference (IPC)*, October 2014.

1.4 Thesis Organization

This thesis is divided into three topics, which are closely related to the design of an efficient optical link for short-reach applications, and it is organized into eight chapters. In Chapter 2, some general background information used throughout this thesis is reviewed. This chapter, briefly explains the concept of forward error correction (FEC), hard-decision decoding, and soft-decision decoding. Then, an overview of the silicon photonics (SiP) platform and SiP photodetectors is presented. A brief discussion of the optical receiver front-end is also provided. Chapter 3 presents the novel methodology for analyzing the advantageous decoding performance of multi-branch configurations of low-bit optical soft-decision forward error correction (SD-FEC) receivers. Chapter 4 details a novel methodology to maximize the responsivity of a Ge-PD based on the bandwidth requirement for a given data rate application. Also, it presents complete comparative experimental results validating the proposed methodology. Chapter 5 demonstrates the design and measurement results of four novel high-speed silicon photodetectors (Si-PD) in silicon-on-insulator (SOI) technology. Chapter 6 presents the design and measurement results of a new compact and power-efficient 25 Gb/s optical receiver fabricated in 65 nm TSMC technology. Chapter 7 describes the design and measurement results of a novel 25 Gb/s ring-based PAM-4 modulator fabricated in the silicon photonics platform. This work is not directly related to the content of this thesis. We have presented the results to list our contribution in another project in parallel

with this research work. Finally, Chapter 8 presents the conclusions and summarizes the key achievements of this work. Further, it discusses several research directions to extend the work presented in this dissertation for future optical short-reach interconnects.

Chapter 2

Background

This chapter describes the essential background for the upcoming chapters, and it is organized into three sections. The first section overviews basic information about forward error correction (FEC) technique, hard-decision decoding, and soft-decision decoding. The critical information about the silicon photonics (SiP) platform and SiP photodetectors are discussed in section 2. Section 3 presents basic information about optical receiver front ends in CMOS technology.

2.1 Forward Error Correction (FEC)

Forward error correction (FEC) is a technique for controlling errors in transmitted information in a noisy channel. It is implemented by sending redundant data on the same channel as a message, thus providing a means that the receiver can recover information if the channel is corrupted. Therefore, data retransmission is avoided at the cost of extra bandwidth for transferring the redundant data and additional data processing for encoding and decoding the information. FEC is one of the cost-effective techniques for mitigating the effects of system impairments in an optical link and it improves the data rate

and the optical distance reach [15]. Conventional long-haul optical communication extensively employs classical FEC codes such as Reed-Solomon (RS), or Bose-Chaudhuri Hocquenghem (BCH) codes [34,35]. In the last decade, iteratively decodable codes such as Turbo codes and low density parity check (LDPC) codes have attracted significant research attention for expanding the speed and transmission distance of the next generation of optical links [10,14,15]. The presence of the high-resolution analog-to-digital converter (ADC) in the coherent based detection also provides enhanced link performance using soft-decision (SD) decoding [10,14,15]. For instance, by using soft-decision decoding, data transmission over a link up to 9000 km at 100 Gbps per wavelength channel was demonstrated [36].

On the other hand, in short-reach optical interconnects, the cost and power efficiency requirements preclude the consideration of either coherent detection or a high-resolution ADC [9, 11, 12]. Nevertheless, by using lower resolution with a 2- or 3-bit ADC, the net coding gain (NCG) of soft-decision decoding can still be improved by 1-2 dB compared to hard-decision (HD) decoding [28, 37]. While a high-speed high-resolution ADC can be designed for sub-watt power consumption [38], a low-resolution soft-decision receiver will dissipate less power and be more cost-effective than its high-resolution counterpart, at the expense of a slightly degraded NCG. For instance, by using a 2-bit ADC, the decoding performance degrades only by 0.4 dB compared to a high-resolution ADC [28]. Since the high-resolution requirement of ADCs in long-haul transmission stems from the post-processing performed by the DSP which are not favored in short-reach applications, low-bit ADCs become a prospective solution. In fact, it is increasingly important to investigate technologies that will enable the development of power-efficient SD-FEC decoders for scalable short-reach data communication.

In [27,39], our group introduced a low complexity and energy efficient optical front end for 2-bit SD-FEC decoders. In comparison with existing soft-decision front ends [28], the proposed optical front end provides a number of advantages in terms of linearity, bandwidth,

optoelectronic integration, power consumption and cost [27]. The decoding performance of the proposed front end was evaluated experimentally. The reported optical receiver was implemented using off-the-shelf components, where tapping the incoming optical signal before the photodetector provided an extra bit in a double-branch configuration of the receiver. The effect of the front end configuration was not considered in this work nor was an evaluation methodology discussed in the literature available. The literature focuses on a single-branch receiver [40] and not on multi-branch receiver proposed in [27,39]. Chapter 3 presents a novel methodology for evaluating the error performance of a multi-branch optical SD-FEC receiver before its hardware implementation.

2.1.1 Error Performance Evaluation in Optical Links

An appropriate noise analysis is required to evaluate the error performance of an optical link. Three major sources of noise are considered in an optical link: 1) transmitter noise; 2) channel noise; 3) receiver noise [41]. Depending on the characteristics of the optical link, each of them can be the dominant noise source. The transmitter noise consists of the relative intensity noise (RIN) of the semiconductor laser with a standard deviation σ_{RIN}. The channel noise originates from amplified spontaneous emission (ASE) in optically amplified long-haul links and is considered insignificant in the case of nonamplified short-reach links. Finally, the receiver noise consists of the shot noise of the photodetector, the thermal noise of the load resistance of the photodetector with standard deviations of σ_{sh}, σ_{th-RL}, respectively, and the input-referred noise of the electrical post-amplifier stages. The noise equations are discussed in detail in Appendix A. Noise source due to RIN, beating noise between the received signal and ASE, and shot noise are data dependent. These noise sources generate a signal distribution with different variances for each binary value.

In an optical link, the quality factor (Q-factor) of the received signal in dB is given by

$$Q = 20\log_{10}\left(\frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}\right), \tag{2.1}$$

where μ_0 and μ_1 are the mean values of the received binary 0 and 1, respectively, and σ_0 and σ_1 are the standard deviations of the received binary 0 and 1, respectively [41]. The mean values depend on the average received optical power (P_{av}) and the extinction ratio (ER) of the intensity modulation. As discussed in Appendix A, the total standard deviations σ_0 and σ_1 are the square root of the sum of the squares of the standard deviations of the noise sources in an optical link for a binary 0 and 1, respectively. Bit error rate (BER) is a metric that indicates the link reliability and, for uncoded data, is calculated by

$$BER = \frac{1}{2} erfc \frac{Q}{\sqrt{2}}, \tag{2.2}$$

where $erfc$ is the complementary error function [41]. The BER value calculated by eq. 2.2 is also known as pre-FEC BER. Using FEC technique considerably improves the BER values, required for reliable data transmission systems. The BER value of the decoded data known as post-FEC BER. Net coding gain (NGC) is a metric that evaluates the FEC code performance and defines as the difference between the required Q-factor levels between the uncoded system and coded system to reach the same BER level.

2.1.2 Hard-Decision Versus Soft-Decision Decoder

In the receiver side, two ways of decoding can be considered for iteratively decodable codes: hard-decision decoding and soft-decision decoding. In a hard-decision decoder, the receiver performs a single decision, comparing the input to a threshold to identify the binary value (0 or 1) of the received signal. In an N-bit soft-decision decoder, $2^N - 1$ decision

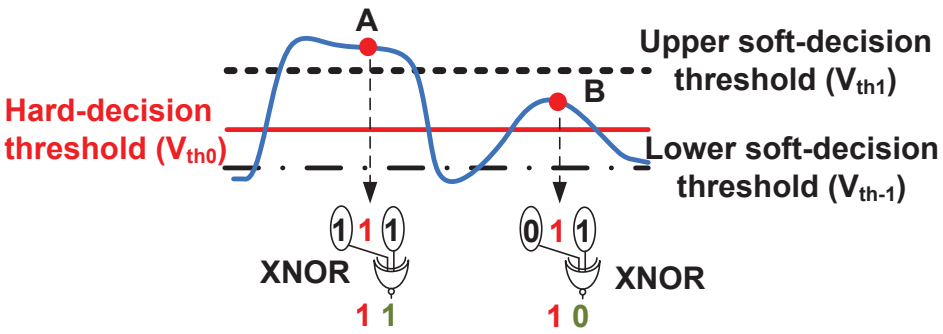


Fig. 2.1 Illustration of a 2-bit soft-decision threshold with the hard-decision bit (red) and the confidence bit (green).

thresholds exist in the receiver such that one threshold identifies the hard-decision bit (centered), while the other thresholds provide confidence decision bits that determine the probability of the hard-decision bit. Compared with hard-decision decoders, the confidence bits improve the decoding performance when making use of an iterative decoder [15,28,39]. In particular, the LDPC decoding algorithm decodes a block of bits using a graphical message-passing model called the sum-product algorithm (SPA) [42]. The SPA makes use of probabilistic information of the received signal such as log-likelihood ratio (LLR). The LLR is the logarithm of the likelihood of the transmitted signal level being a binary 1 over the likelihood of that same signal being a binary 0 [40, 43], as expressed by

$$LLR(y_i) = \ln\left(\frac{P(x_i = 1|y_i)}{P(x_i = 0|y_i)}\right), \tag{2.3}$$

where y_i is the received sample, and the conditional probability is given by

$$P(x_i|y_i) = \frac{P(y_i|x_i)P(x_i)}{P(y_i|x_i = 0)P(x_i = 0) + P(y_i|x_i = 1)P(x_i = 1)}, \tag{2.4}$$

where $P(x_i)$ is a *priori probability* of the transmitted data of x_i and $P(y_i|x_i)$ is the corresponding probability distribution function (PDF) of the received sample. Figure 2.1 illustrates a 2-bit soft decision. Two additional decision circuits with each a threshold

(V_{th1} and V_{th-1}) provide one single confidence-bit from an exclusive negative oR boolean logic (XNOR) of the binary decisions related to the two thresholds. In Fig. 2.1, the sampled data point examples, A and B, are both above the hard decision threshold (V_{th0}). However, there is more confidence in the decision for point A because it is above both soft-decision threshold levels. Thus, sampled data point A has a confidence-bit set to 1. The confidence-bit is 0 for the sampled signal that resides between the two soft-decision threshold levels. Indeed, the confidence level increases as the sampled data are farther away from the middle threshold, thus indicating the low probability that an error in the decision was made. Table 2.1 lists the truth table for the three bits resulting from the entire dynamic range of the receiver. The dynamic range of the received sample 'y' is digitized by increasing the number of 1s in the 3-bit thermometer code as the amplitude of the sampled data increases. This representation is referred to as thermometer coding. The 3-bit thermometer code $[D_1, D_0, D_{-1}]$ is converted to 2-bit soft data [H, C] corresponding to the hard-decision bit $[H = D_0]$ and the confidence-bit $[C = \overline{D_1 \oplus D_{-1}}]$.

Table 2.1 Conversion table 3-bit thermometer code to 2-bit soft data

	3-bit Thermometer code			2-bit soft data	
	D_1	D_0	D_{-1}	H	C
$y \leq V_{th-1}$	0	0	0	0	1
$V_{th-1} < y < V_{th0}$	0	0	1	0	0
$V_{th0} < y < V_{th1}$	0	1	1	1	0
$V_{th1} \leq y$	1	1	1	1	1

The PDF of the received sampled data is needed for calculating the LLR value of each sampled data. In a long-haul optically amplified link, the channel noise originating from amplified spontaneous emission (ASE) is the dominant noise source. The photodetector, a quadratic element, generates a non-central chi-squared PDF of the received sampled

data [40]. For numerical calculation, however, Gaussian PDFs with different standard deviation for each binary value are used [43]. For the case of nonamplified short-reach optical links where the receiver noise is the primary noise source, the received data consist of Gaussian PDFs with similar standard deviation for each logic level.

Figure 2.2 illustrates the general case of two Gaussian distributions with different standard deviations (σ_0, σ_1) for each binary value with their respective mean values (μ_0, μ_1) [40]. The corresponding unquantized LLR values (blue line in Fig. 2.2, bottom) are calculated

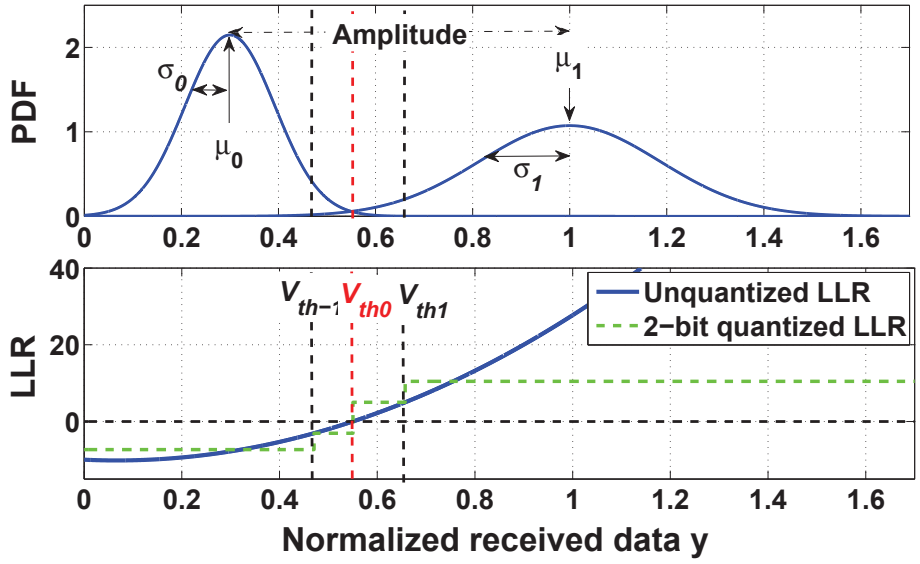


Fig. 2.2 (top) PDF with standard deviations (σ_0, σ_1) and mean values (μ_0, μ_1) corresponding to binary value 0 and 1, respectively, for normalized received data samples; (bottom) corresponding LLR with set threshold levels (V_{th-1}, V_{th0}, V_{th1}) for a 2-bit soft-decision decoder (green) and the corresponding unquantized LLR values (blue).

by

$$LLR(y) = \ln\left(\frac{\sigma_0}{\sigma_1}\right) + \frac{1}{2}\left(\frac{y^2(\sigma_1^2 - \sigma_0^2) - 2y(\mu_0\sigma_1^2 - \mu_1\sigma_0^2) + \mu_0^2\sigma_1^2 - \mu_1^2\sigma_0^2}{\sigma_0^2\sigma_1^2}\right), \tag{2.5}$$

The best decoding performance is achieved with unquantized LLR values (i.e., infinite

number of quantization levels). Therefore, more quantization levels lead to higher accuracy and improved decoding performance of iterative SPA decoding. For an N-bit soft-decision receiver, the initial LLR values provided to the SPA are quantized to 2^N levels intersecting the unquantized LLR curve obtained with equation 2.5. The green dashed line (Fig. 2.2, bottom) illustrates the 2-bit quantized LLR values for given threshold values. Selecting appropriate hard-decision and soft-decision threshold levels are explained in Appendix B.

2.2 Silicon Photonics Platform

This section briefly discusses the basic properties of the silicon photonics (SiP) platform used to fabricate the optical devices in this work. Then, it provides key information about silicon photonics photodetectors. The proposed optical components in this work are fabricated through multi-project wafer (MPW) runs by the Institute of Microelectronics IME-A*Star in Singapore. This MPW fabrication process only provides optical components and uses a silicon-on-insulator (SOI) wafer with 220 nm silicon (Si) thickness. In addition to the full etch of the Si layer (220 nm) to form the channel waveguides, there are two partial etches of 70 nm and 130 nm. The 70 nm etch of the Si layer forms a ridge waveguide with 150 nm slab waveguide, which mainly is used in the grating couplers as I/O interfaces. The 130 nm etch of the Si layer forms a ridge waveguide with 90 nm slab waveguide, which is used in modulators and other active devices such as optical switches. The process also provides six doping layers of p++, p+, p, n, n+, n++ for active devices, a thin-film germanium (Ge) deposition to make photodetectors and two metal layers. Figure 2.3 shows the process cross section [44].

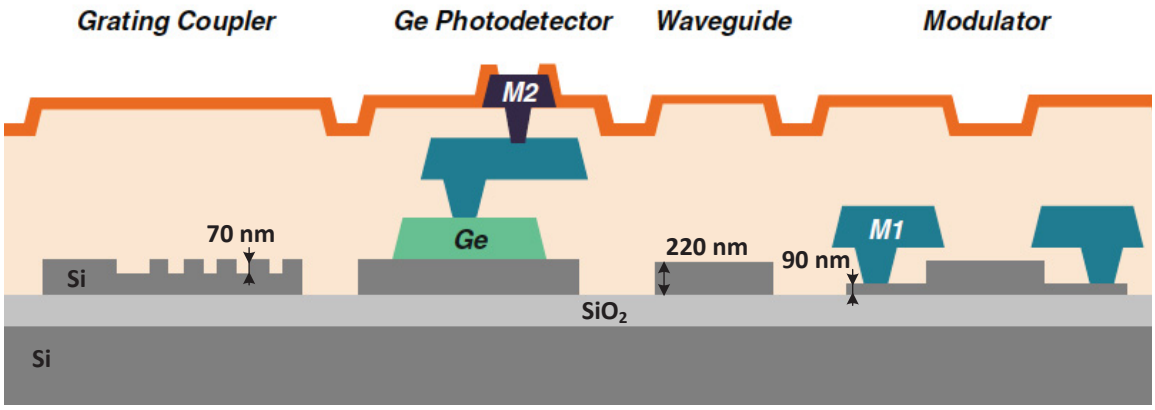


Fig. 2.3 Process cross-section [44].

2.2.1 Photodetectors (PDs)

A key building block in any optical link is a photodetector (PD), which acts as an optical-to-electrical (OE) converter. Reverse biased p-i-n diodes are the most common detectors that are used in high-speed optical links. The intrinsic region in a p-i-n diode absorbs photons with energy larger than the bandgap of the semiconductor. Figure 2.4 shows the absorption coefficient of silicon (Si) and germanium (Ge) for various wavelengths at room temperature [45]. Silicon has significant absorption coefficients at short wavelengths, and it is suitable for fabricating a PD for these wavelengths. However, it is transparent at standard communication wavelengths such as 1310 nm and 1550 nm. Hence, to build a PD for long wavelengths in the SOI technology, a thin-film of Ge is deposited on the silicon layer through a selective epitaxial growth [46, 47].

The performance of a photodetector is evaluated by three critical parameters namely responsivity (R), 3 dB bandwidth, and dark current (I_d). Responsivity is the ratio of the generated photocurrent to the incident optical power and usually, is presented with the unit of A/W and is given by

$$R = \eta \frac{q\lambda}{hc} \tag{2.6}$$

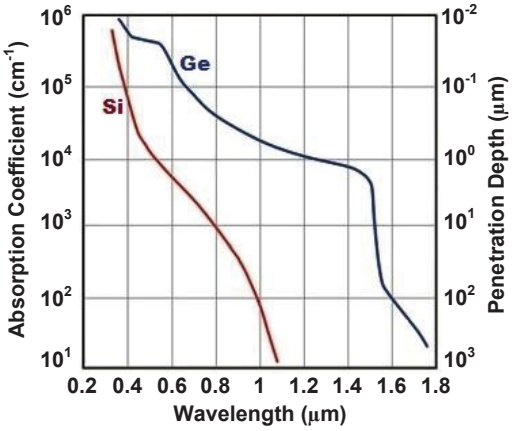


Fig. 2.4 Absorption coefficient of silicon and germanium [45].

where η is the quantum efficiency, q is the charge of an electron, h is Planck's constant, c is the speed of light, and λ is the wavelength of light. For a photodetector without any internal gain, the maximum quantum efficiency is 1. Therefore, the photodetector has a maximum responsivity of 1.25 A/W at 1550 nm, 1.06 A/W at 1310 nm, and 0.68 A/W at 850 nm [48].

The 3 dB bandwidth determines the speed of a detector, which depends on two factors: carrier transit time and RC time constant of the parasitics of the detector [48]. The transit time is the time that takes for photogenerated carriers to leave the active region of the detector and reach to the electrodes. In a p-i-n diode, the maximum transit time bandwidth is estimated by $f_{tr} = 0.38 \times \nu_s/t$, where ν_s is the carrier velocity-saturation and t is the thickness of the intrinsic region. The RC time constant is the electrical characteristic of the detector circuit as shown in Fig. 2.5 [48]. The current source I_{pd} models the photocurrent, C_{pd} and R_{pd} are the parasitic capacitor and resistor of the photodetector, respectively, and R_{load} is the load resistance of the detector. The bandwidth due to RC limitations is

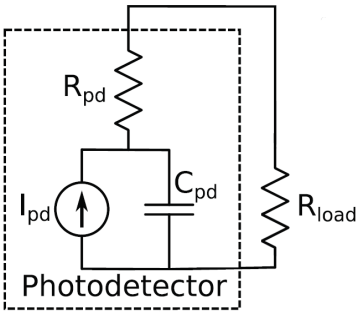


Fig. 2.5 Equivalent circuit model for a photodetector [48].

$f_{RC} = 1/[2\pi C_{pd}(R_{load} + R_{pd})]$. The total bandwidth of the photodetector is given by

$$f = \sqrt{(\frac{1}{f_{tr}^2} + \frac{1}{f_{RC}^2})^{-1}} \tag{2.7}$$

The dark current is a current from a photodetector without any incident light. It is caused by the random generation of carriers in the active area of the detector. The dark current increases with the reverse-bias voltage and temperature, and it contributes to the shot noise, as discussed in Appendix A.

Waveguide Germanium Photodetector (Ge-PD)

Figures 2.6(a) and 2.6(b) show the cross-section of waveguide germanium photodetectors with vertical n-i-p diode junction and lateral p-i-n diode junction, respectively [48]. As shown in Fig. 2.6(c), the light is incident on the photodetector through a taper silicon waveguide, and it evanescently couples from the silicon to the top Ge [46]. The dark current in a Ge-PD is caused by bulk leakage (J_{bulk}) and surface leakage (J_{surf}) [48]. The large difference between the lattice of silicon and germanium causes mid band-gap states. As a result, the bulk generation is dominated by the Shockley–Read–Hall process [49]. Surface leakage is resulted from surface defects such as dangling bonds [48]. The total dark

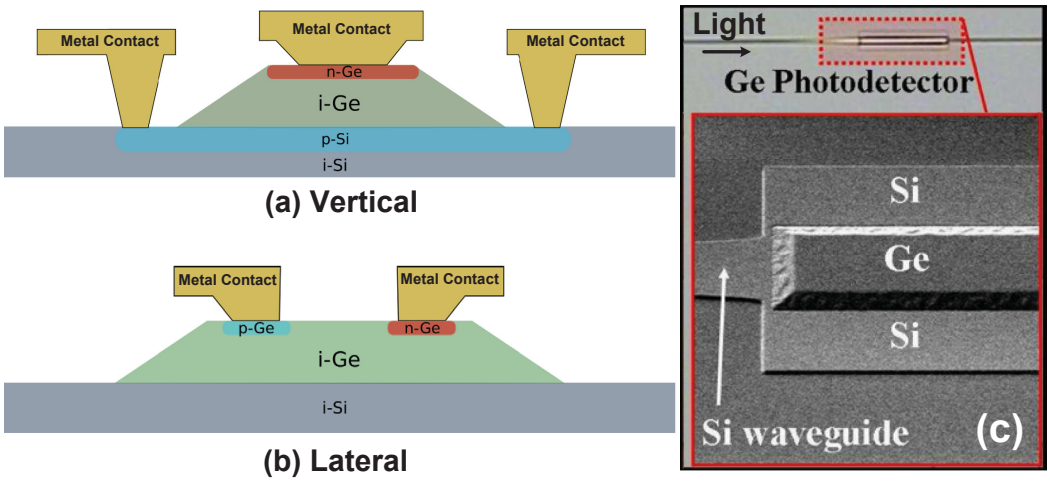


Fig. 2.6 Cross-sections of waveguide Ge photodetectors, (a) with lateral p-i-n diode junction, and (b) vertical n-i-p diode junction [48]. (c) Micrograph of the waveguide Ge-PD [46].

current of a Ge-PD with junction area of A is calculated by [50]:

$$I_{dark} = J_{bulk}A + J_{surf}\sqrt{4\pi A} \tag{2.8}$$

Significant effort has been made to improve the performance of Ge-PDs by optimizing the fabrication process to reduce the dark current and increase the PD's responsivity [46]. Recently, it has been shown that the responsivity of a Ge-PD improves considerably by reducing the optical loss caused by the metal contact directly above the Ge area. Three effective ways are proposed in the literature to reduce metal absorption loss: 1) removing the metal contact above the Ge area and changing the vertical p-i-n diode's structure to a lateral one [51–53] (Fig. 2.7(a)), 2) using a small size off-centered top contact above the Ge [54, 55] (Fig. 2.7(b)), and 3) using multi-finger connections instead of large contacts [56] (Fig. 2.7(c)). Some of these techniques may be limited by the design rules of a specific fabrication process, such as minimum feature size, exclusion and inclusion distances. For instance, to fabricate a PD without having the

metal contact above the Ge region, the width of the Ge would need to be as small as 0.5 μm to reduce the carrier transient time [52]. This is a feature size that is not provided in the fabrication run in which the Ge-PDs in this work were fabricated. Further, the required minimum feature size of a contact via and the minimum distance between two contacts challenges the use of multi-finger compared to an off-centered top contact. Consequently, an off-centered top contact remains a more practical solution to reduce metal absorption. The responsivity of a photodetector can be enhanced by increasing the photodetector's geometry at the cost of lower bandwidth from inherently larger junction capacitance.

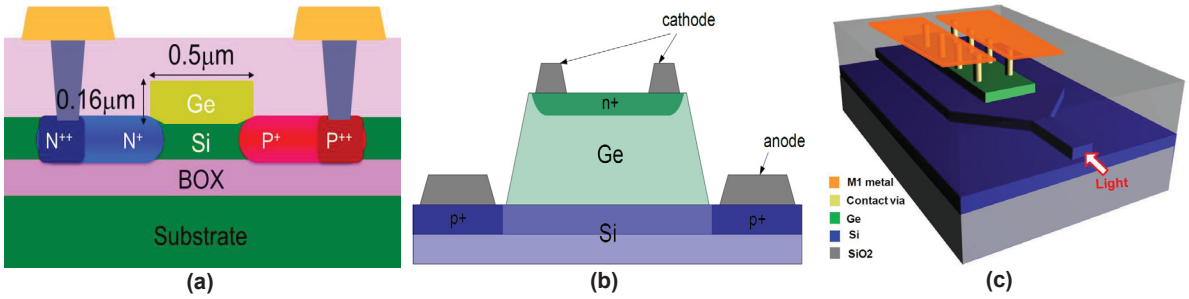


Fig. 2.7 (a) Cross-section of a Ge-PD without top metal contact [52]; (b) cross-section of a Ge-PD with two off-centered top metal contacts [55]; (c) the 3D view of the Ge-PD with multi-finger connections [56].

It has been shown that the bandwidth of a Ge-PD can be enhanced with integrated peaking inductor [57, 58] or by properly using wire-bond connections [59]. Figure 2.8(a) shows a simplified electrical model of a photodetector with serial inductor of L_p [57]. By using a serial inductor with an optimum value of $L_p = 0.5 \times C_{pd}(R_{load}+R_{pd})^2$, the 3 dB bandwidth of the detector improves by $\sqrt{2}$ [57]. Figure 2.8(b) shows the micrograph of a Ge-PD with 360 pH integrated inductor [58]. As shown in Figure 2.8(c), using a peaking inductor of 360 pH, the bandwidth of an unpeaked detector (in blue) is enhanced from 30 GHz to 60 GHz (in green) [58].

Chapter 4 presents a detailed discussion of the effect of the design geometries of a vertical germanium photodetector (Ge-PD) and the size and location of the top metal contact on

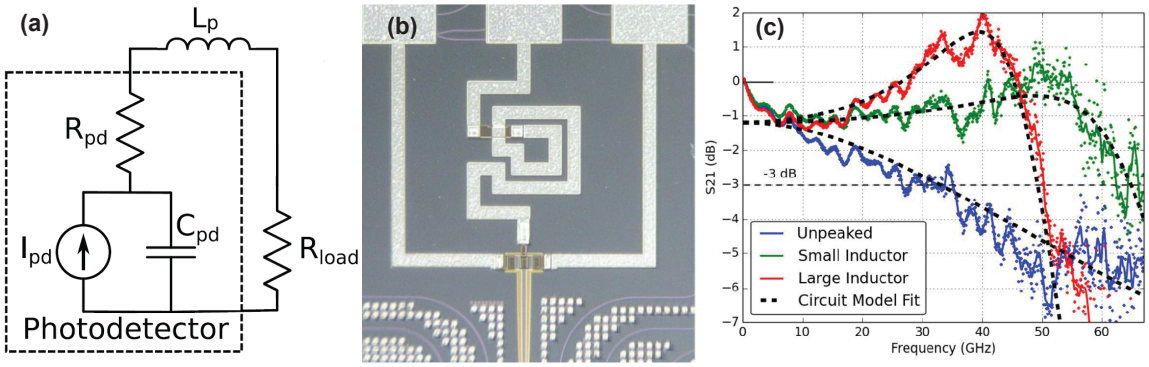


Fig. 2.8 (a) Simplified electrical model of a PD with a serial inductor [57]; (b) micrograph of the Ge-PD with 360 pH integrated inductor; (c) electro-optic S_{21} response at 2 V reverse bias of the unpeaked detector as well as two same size detectors with a small integrated inductor (360 pH) and a large integrated inductor (580 PH) [58].

its performance. Further, it presents a novel methodology to optimize the responsivity of a high-speed Ge-PD. The proposed optimization process investigates design geometry for larger responsivity of a PD and considers modifying the top metal contacts within the fabrication constraints while an integrated peaking inductor mitigates the bandwidth trade-off.

Silicon Photodetector (Si-PD)

Silicon with high absorption coefficient at 850 nm enables monolithic integration of an optical receiver with a photodetector. This integration reduces the cost and complexity of the packaging and provides a more reliable optical system [60–62].

Figure 2.9 shows an example of a p-n Si-PD in a bulk CMOS technology. Since the penetration depth of the 850 nm light in bulk silicon is larger than 10 μm (Fig. 2.4), most of the photons are absorbed outside the depletion region [63]. The slow diffusion current of carriers generated outside the depletion region limits the speed of the Si-PD to sub-GHz in bulk technology [63]. Several techniques have been demonstrated to reduce the slow carriers in Si-PDs at the cost of responsivity degradation [61–67]. Figures 2.10(a)

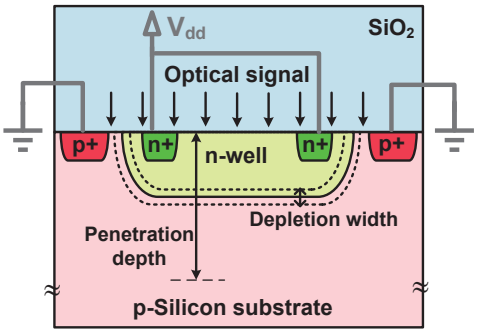


Fig. 2.9 Structure of a p-n Si-PD in a bulk CMOS technology.

and 2.10(b) show the two most common techniques to reduce the diffusion current. In the first technique known as double photodetector (DPD) (Fig. 2.10(a)), the p+/N-Well (NW) junction makes the photodetector, and the NW/p-substrate junction is the second diode that shields the input of the optical receiver from the slow carriers generated in the p-substrate. This technique decreases the diffusion current and consequently increases the speed of the photodiode, but degrades the device's reliability and responsivity [64]. The second technique is shown in Fig. 2.10(b) known as spatially modulated light (SML) consists of differential photodetectors. One of the PDs is shaded by floating metals while another one is illuminated [62, 66]. This technique eliminates the diffusion current by subtracting the illuminated signal from the shaded signal and improves the speed of the Si-PD. However, the responsivity of the photodetector is degraded due to the reflection of 50% of the received light, and also, it requires a differential optical receiver with high common-mode rejection ratio (CMRR). Most of the Si-PDs are designed for avalanche performance (avalanche photodetector (APD)) to increase the responsivity in the modified Si-PDs [64–67]. However, to the best of our knowledge, the maximum bandwidth reported of a Si-PD fabricated in a bulk CMOS technology is 12 GHz with a responsivity of 0.03 A/W, which is resulted from an avalanche gain of 10.6 at 9.7 V reverse-bias voltage [66].

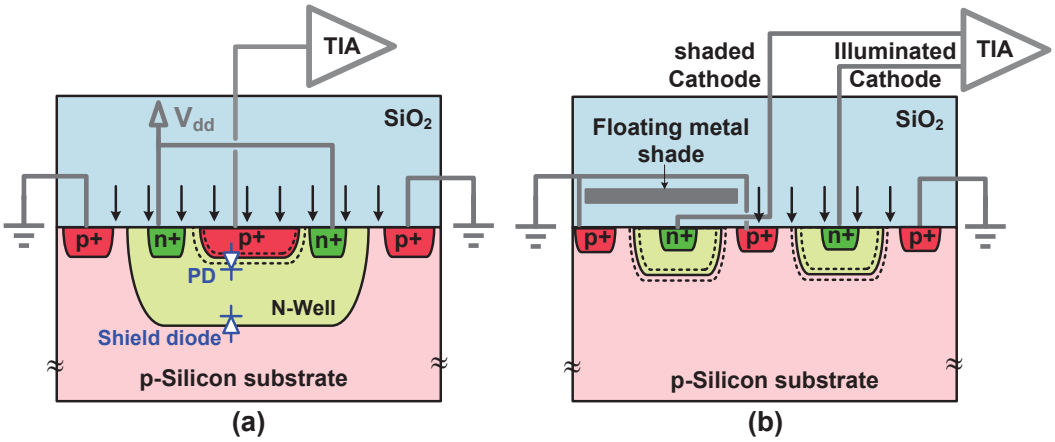


Fig. 2.10 (a) Structure of double photodetector (DPD); (b) structure of spatially modulated light (SML) Si-PD.

The bandwidth of the Si-PD can be improved further by fabricating the photodetector on a silicon-on-insulator (SOI) platform. The structure of a lateral p-i-n Si-PD in an SOI technology is shown in Fig. 2.11. Elimination of the diffusion current by using the insulator between the active area of the Si-PD and the substrate improves the bandwidth of the PD without any equalization techniques [68, 69]. However, the responsivity of this type of PD is limited by the thickness of the silicon on the insulator. For instance, in the case of a 210-nm silicon layer, more than 98% of the vertically incident light passes through the silicon and limits the responsivity of the Si-PD to 0.0075 A/W [69].

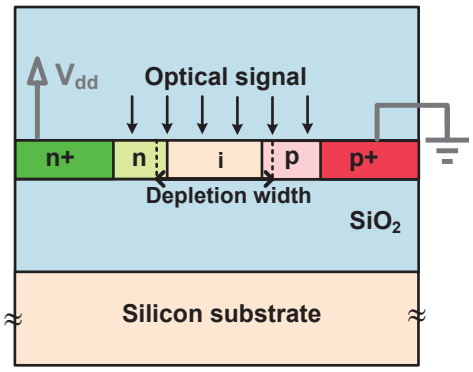


Fig. 2.11 Structure of a lateral p-i-n Si-PD in an SOI technology.

To increase the quantum efficiency and as a result improving the responsivity of an

SOI-based Si-PD, a waveguide-grating coupler (GC) is fabricated on top of the detector [70]. Figures 2.12(a) and 2.12(b) show cross-section of a SOI-based p-i-n diode with a waveguide-grating coupler on top of the diode and the micrograph of the fabricated device, respectively [70]. Measurement result shows that the designed grating coupler improves the quantum efficiency by a factor of four in comparison with a detector without GC. However, the large size of the grating coupler on top of the diode area limits the bandwidth of the detector to 4.1 GHz due to a large parasitic capacitance and resistance of the doped area under the GC [70]. Chapter 5 demonstrates the design and measurement results of novel SOI-based Si-PDs that use grating couplers to direct the incident light horizontally to the intrinsic area of the p-i-n diode for an efficient absorption while the structure of the p-i-n diode is optimized for high-speed operation.

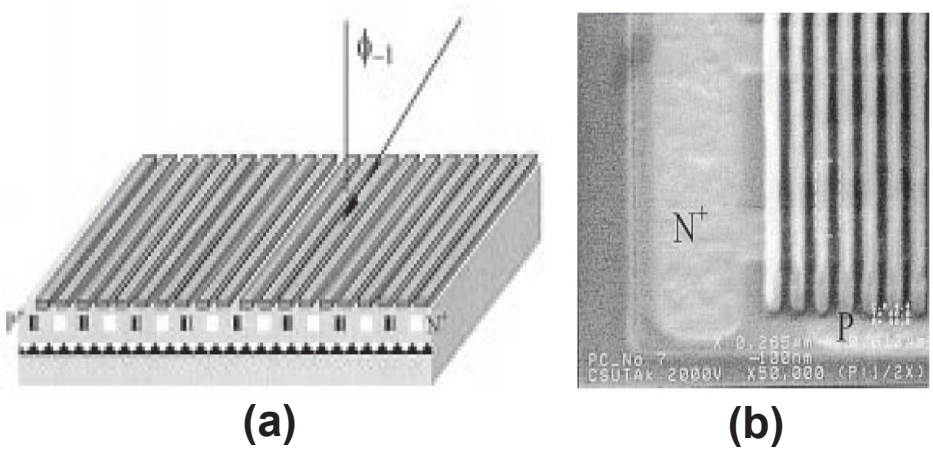


Fig. 2.12 (a) Cross-section of an SOI-based p-i-n diode with a waveguide-grating coupler on top of the diode; (b) the micrograph of the fabricated device [70].

Avalanche Photodetector (APD)

An avalanche photodetector (APD) is a p-n/p-i-n junction purposely made to work at high electric fields to achieve internal gain. A high electric field resulted from a large reverse-bias voltage increases the drift velocity and kinetic energy of carriers in the depletion

region. Hence, a carrier (electron or hole) has sufficient energy to break a bond and generates a new electron-hole pair. This process is known as impact ionization [71]. The original carrier and the generated carriers will be accelerated by the electric field and contribute to generating more carriers that gradually increases the photocurrent. Therefore, the avalanche multiplication process increases the responsivity of the photodetector. Note that amplification applies to photogenerated carriers as well as carriers generated by any other mechanism (e.g., thermally generated carriers). It also increases the noise of the photodetector. The excess noise factor F_A is given by

$$F_A(M) = k_A M + (1 - k_A)\left(1 - \frac{1}{M}\right) \tag{2.9}$$

where M is the multiplication factor also known as avalanche gain and k_A $(0 < k_A < 1)$ is the ratio of ionization coefficients of electrons (α_e) and holes (α_h). The variance of the shot noise (σ_{sh}^2) of an avalanche photodetector is given by

$$\sigma_{sh}^2(i) = 2qM^2F_A[R(P_{in}) + I_d)]B_e \tag{2.10}$$

where q is the charge of an electron, R is the responsivity of the photodetector, P_{in} is the received optical power, and B_e is the bandwidth of the optical receiver [41]. In an optical receiver with dominant thermal noise, using an avalanche photodetector increases the signal-to-noise ratio (SNR) by a factor of M^2, while when the shot noise is dominant, the SNR degrades by the excess noise factor (F_A) [41].

2.3 Optical Receiver Front End

Developing a compact, low-power, and highly sensitive optical receiver is essential for short-reach applications. As shown in Fig. 1.2, a receiver front-end typically consists of a

transimpedance amplifier (TIA) and some post-amplifier (PA) stages. A TIA converts the photocurrent to a voltage signal and amplifies it. For further amplification, there are post-amplifier stages that provide enough peak-to-peak amplitude at the input of the decision circuit. The total bandwidth of the TIA and PA stages needs to be large enough to avoid large inter-symbol interference (ISI). On the other hand, broad bandwidth of the front end increases the total noise power, which results in degradation of the receiver sensitivity. Also, providing large bandwidth results in a lower gain per stage, which increases noise due to the higher noise density and further degrades the receiver sensitivity. Due to the trade-off that exists between ISI and sensitivity, the total bandwidth of the front end is typically chosen around 0.5–0.7 times of the target data rate [72, 73].

2.3.1 Transimpedance Amplifier

The design of a transimpedance amplifier has the most impact on the trade-off among noise, bandwidth, gain, and power consumption of an optical receiver [73]. Usually, the large input capacitance (parasitic capacitance of the photodetector, packaging, and TIA) and the input impedance of the TIA determine the bandwidth. A high-performance TIA topology needs to have a low input impedance, high current-to-voltage gain, and a small input-referred current noise. The noise of the TIA is caused by the thermal noise of the resistors and transistors in the TIA topology. Figures 2.13(a) and 2.13(b) show the thermal noise model of a transistor and a resistor, respectively. In this figure, k is the Boltzmann constant, T is the temperature, g_m is the transconductance of the transistor, and γ is the excess noise coefficient.

Figure 2.14 shows the block diagram of three common single-ended TIAs in a CMOS technology. The common-gate (CG) amplifier shown in Fig. 2.14(a) has a low input impedance (R_{in}) of g_{m1}^{-1}, where g_{m1} is the transconductance of the transistor M_{n1}. The CG amplifier acts as a current buffer with almost a unity current gain, so the transimpedance

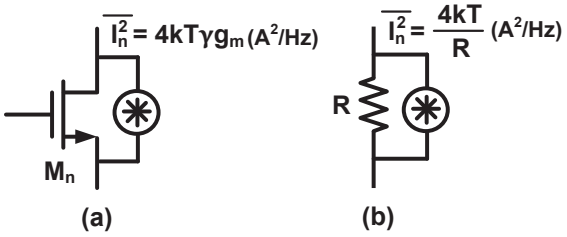


Fig. 2.13 (a) Thermal noise model of a NMOS transistor; (b) Thermal noise model of a resistor.

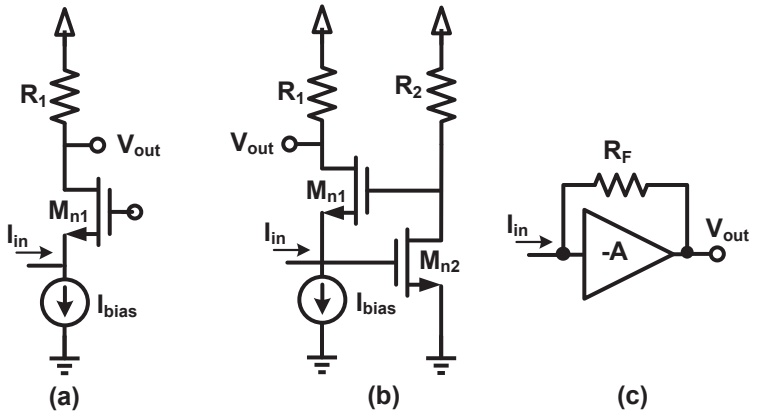


Fig. 2.14 (a) Schematic of a common-gate (CG) TIA; (b) regulated cascode; (c) shunt feedback TIA.

gain of the CG TIA is equal to R_1. The main drawback of this topology is that the noise of the bias current circuit adds to the input current (I_{in}) and degrades the signal-to-noise ratio (SNR). The current noise of a transistor directly increases with its g_{m1}; hence, there is a strong trade-off between bandwidth and noise in this structure. The regulated cascode (RGC) topology, as shown in Fig. 2.14(b), is essentially a CG structure with negative feedback (M_{n2}) [74]. The negative feedback decreases the input impedance to $[g_{m1}(1+g_{m2}R_2)]^{-1}$, while the g_{m1} of the transistor would be remained almost the same as the CG topology. Therefore, the RGC provides higher bandwidth in comparison to the CG TIA. The local feedback may cause instability due to the creation of a second pole and requires careful design. Figure 2.14(c) illustrates the block diagram of a shunt feedback TIA. Due to the Miller effect of the feedback resistor (R_F), the input impedance

at DC is decreased to $R_F/(1+A)$, while the DC transimpedance gain (R_T) is equal to $R_T=R_F/(1+A^{-1})$, which for $A \gg 1$ results in $R_T \approx R_F$. In this topology, the noise of the feedback resistor (R_F) is directly referred to the input, which is similar to the noise contribution of R_1 in CG TIA. The input-referred voltage noise of the amplifier in shunt feedback TIA is devided by R_F when it is referred to the TIA's input. Hence, for a large R_F value, the input-referred current noise of the amplifier can be much smaller that the noise contribution of the bias current source in CG topology. As a result, shunt feedback TIA provides a better noise performance in comparison to the two other topologies [73].

As shown in Figs. 2.15(a) and 2.15(b), a common-source (CS) amplifier and inverter-based amplifier are two typical single-ended topologies used to implement the feedback TIA circuit of Fig. 2.14(c). A simplified small-signal model is shown in Fig. 2.15(c), which is used to analyze the performance of a shunt feedback TIA. In this figure, C_{PD} is the

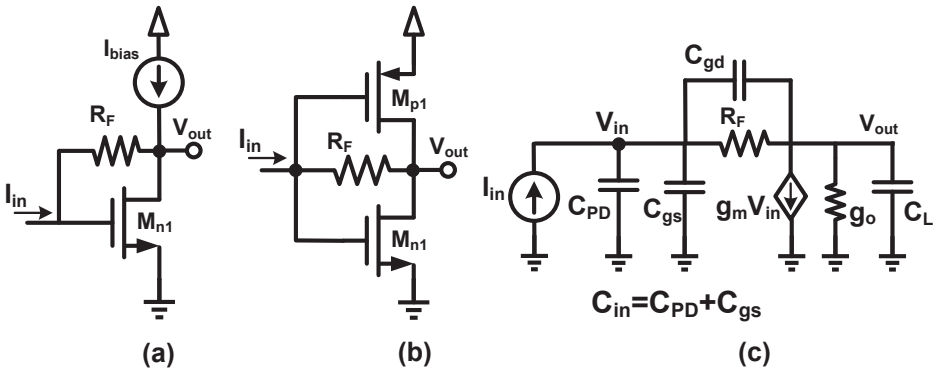


Fig. 2.15 (a) Schematic of a common-source (CS) feedback TIA; (b) an inverter-based feedback TIA; (c) simplified small-signal model.

parasitic capacitor of the photodetector and its packaging, C_{gs} is the gate-source parasitic capacitor of a transistor, and C_{gd} is the gate-drain parasitic capacitor of a transistor. In the inverter structure, C_{gs} represents the sum of the gate-source parasitic capacitors of PMOS and NMOS transistors. Also, C_{gd} represents the sum of the gate-drain parasitic capacitors of PMOS and NMOS transistors. The g_o is the effective output conductance

of the amplifier. For the CS amplifier, it is the sum of the output conductances of the NMOS transistor (g_{dsn}) and the bias circuit. While, for the inverter structure, g_o is the sum of the output conductances of PMOS (g_{dsp}) and NMOS (g_{dsn}) transistors. C_L is the parasitic load capacitor of the TIA, which includes the drain-source and drain-body parasitic capacitors of the TIA and the parasitic input capacitor of the following post-amplifier. The transimpedance transfer function of the feedback TIA is given by

$$\begin{aligned} Z_t(s) &= \frac{A(s)}{B(s)}, \\ A(s) &= 1 - g_m R_f + s R_f C_{gd}, \\ B(s) &= g_m + g_o + s[C_{in} + C_L + R_f(C_{gd} g_m + C_{gd} g_o + C_{in} g_o)] \\ &+ s^2 R_f [C_{in} C_{gd} + C_{in} C_L + C_L C_{gd}] \end{aligned} \tag{2.11}$$

The equation shows that increasing the g_m of the transistors improves the transimpedance gain, while the output conductance of g_o degrades it. Assuming that the two poles are far apart and C_{gd} is negligible, the bandwidth (BW) can be approximated by

$$BW \approx \frac{g_m + g_o}{2\pi[C_L + C_{in}(1 + R_F g_o)]} \tag{2.12}$$

The equation indicates that increasing the g_m directly improves the bandwidth. However, increasing the size of the transistor increases g_m, g_o, and the parasitics capacitor C_{gs}. Therefore, increasing the size of the transistors would eventually limit the bandwidth of the TIA by enlarging the capacitor of the amplifier and increasing g_o. The inverter-based feedback TIA has several advantages in comparison to the CS feedback TIA. First, the inverter-based feedback TIA has a larger effective transconductance (g_m=g_{mn}+g_{mp}) for a given bias current. However, this comes at the expense of larger input capacitance. Second, it is more suitable for small supply voltages and offers a large output swing [75].

The total input-referred noise of the receiver front end and the photodetector noise determine the sensitivity of the receiver. Usually, the noise of the TIA is the main contributor to the receiver noise because it gets amplified through the following post-amplifier stages. Therefore, designing a low noise TIA is essential to improve the sensitivity of an optical receiver. The TIA noise is mostly due to the thermal noise of the feedback resistor R_F and the noise of the amplifier. A detailed noise analysis of the feedback TIA can be found in [73].

2.3.2 Post-Amplifiers

Due to the gain-bandwidth trade-off in designing a TIA, it is difficult to achieve a desirable gain-bandwidth product in a single-stage amplifier. Hence, the TIA stage is followed by several post-amplifier stages to increase the gain of the receiver front-end. Cascading N uniform first-order amplifiers with a voltage gain of A_v and bandwidth of BW_0 increases the total gain of the amplifier chain to $A_{Total}=A_v^N$. While the overall bandwidth of the N-cascaded amplifiers is $BW_{Total}=BW_0\sqrt{\sqrt[N]{2}-1}$, which is less than the bandwidth of each stage. Therefore, for a certain total gain-bandwidth product, each stage requires the gain-bandwidth product of $GBW_0=\sqrt[N]{A_{Total}}\times BW_{Total}/\sqrt{\sqrt[N]{2}-1}$, which decreases considerably as the number of stages (N) increases and it has a minimum value for $N=2ln(A_{Total})$ [73]. The power consumption of the post-amplifier chain increases proportionally with the number of stages. Also, with a large number of low-gain stages, the noise contribution of post-amplifiers becomes significant. Consequently, a high-gain post-amplifier usually is designed with less than five stages [73]. The single ended or differential common-source (CS) amplifier and Cherry–Hooper (CH) amplifier are two typical topologies that have been used as post-amplifier stages. Note that a single-ended structure is more sensitive to the power supply noise, substrate noise, and package resonances. However, in comparison with a differential topology, it consumes less power, which is favorable for a low-power design.

Using an on-chip regulated power supply can reduce the supply noise in the single-ended topologies [76].

Figures 2.16(a) and 2.16(b) show a single-ended CS amplifier with a load resistance of R_L and a CS-based CH amplifier, respectively. There is a strong trade-off between the voltage gain and bandwidth of the CS amplifier. It has a pole at $W_{p(CS)}=(R_L C_L)^{-1}$ and the low-frequency voltage gain of $|A_{V(CS)}|=g_{ma}\times R_L$, where g_{ma} is the transconductance of the NMOS transistor. As shown in Fig. 2.16(b), the CH amplifier consists of two cascaded CS amplifiers with a feedback resistor (R_F) around the second section. Due to this feedback resistor, the small-signal resistance seen at the output nodes of both first and second sections of a CH amplifier is about g_{m2}^{-1} resulting in high-frequency poles of $W_{p1(CH)} \approx (g_{m2}/C_x)$ and $W_{p2(CH)} \approx (g_{m2}/C_L)$ [73]. The low-frequency gain of the CH amplifier is $|A_V \approx g_{m1}\times R_F - g_{m1}/g_{m2}$, where g_{mi} is the transconductance of transistor M_i (i=1,2). Assuming that $R_F \gg g_{m2}^{-1}|$, the gain of a CH amplifier is close to the gain of a CS amplifier with a load resistance of R_F while it has a larger bandwidth [73].

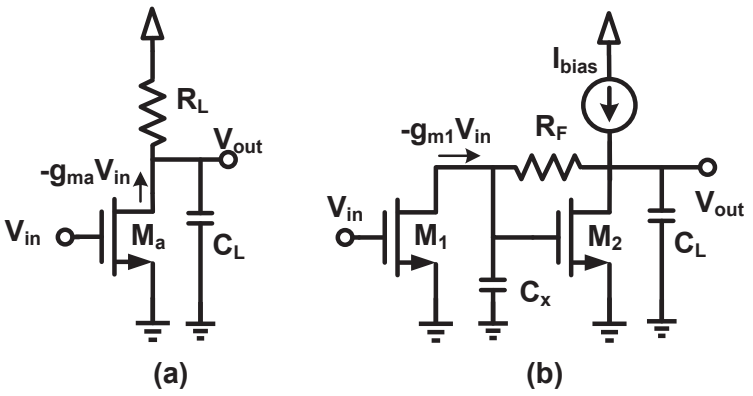


Fig. 2.16 (a) Schematic of a CS amplifier with a load capacitance; (b) a CS-based CH amplifier with node capacitances.

2.3.3 Bandwidth Enhancement Techniques

Designing a power-efficient optical receiver with a high gain-bandwidth product is more challenging in CMOS technology compared with SiGe, GaAs, and InP technologies, due to the lower transition frequency (f_T) of CMOS. When the technology is not fast enough to design a receiver with a high gain-bandwidth product, broadband techniques are employed. Inductive peaking is a common bandwidth enhancement technique at the cost of chip area [77–83]. For example, a 1 nH inductor in 65 nm CMOS technology may occupy an area of 300 μm$\times$300 μm. There are more compact bandwidth extension techniques such as active inductors [84], third-order interleaved active feedback [85], multi-peaking bandwidth extension [86], and local positive feedback [87,88]. In a single-ended DC-coupled multistage amplifier, optimizing the active inductors increases the design complexity of the biasing for each stage and the desing would be more sensitive to fabrication process [89]. The third-order interleaved active feedback and multi-peaking bandwidth extension techniques enhance the bandwidth of uniform multistage amplifiers by separating the poles. Here, we overview two techniques, third-order interleaved active feedback (IAFB), and positive feedback (PFB), that are used in the proposed optical receiver (Chapter 6).

Interleaved Active Feedback (IAFB)

Figures 2.17(a) and 2.17(b) show the block diagram and circuit schematic of a third-order active feedback amplifier, respectively. It consists of three gain stages of G_1, G_2, and G_3 and an active feedback cell of G_f [85]. To simplify the analysis, all of the resistive and capacitive loads and the transconductance of the gain stages are considered to be equal to R, C, and g_m, respectively. The transfer function of the gain stage and active feedback can

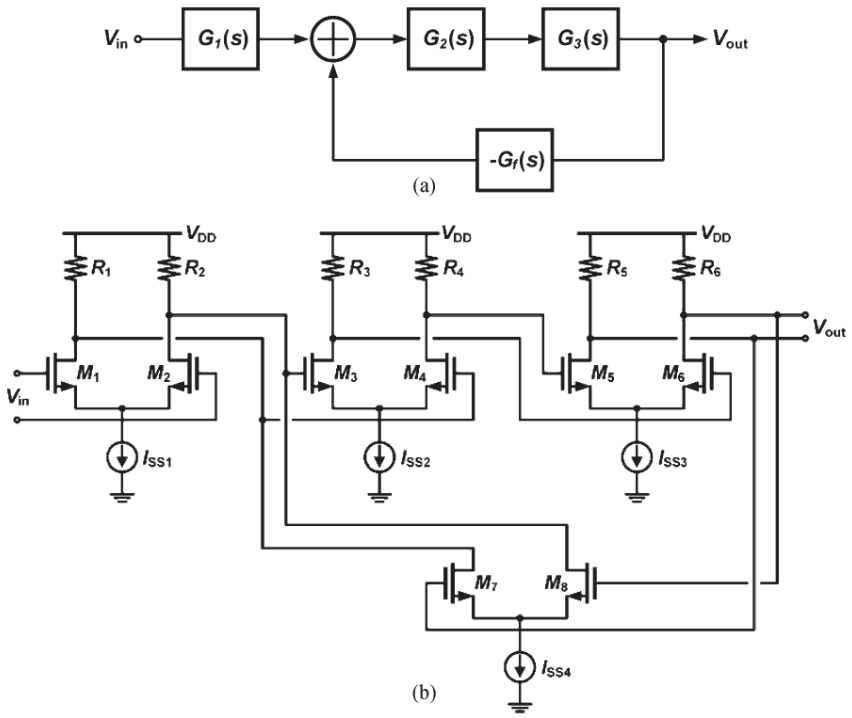


Fig. 2.17 (a) Block diagram and (b) circuit schematic of a third-order active feedback amplifier [85].

be approximated by a single-pole equation as

$$G_1(s) = G_2(s) = G_3(s) = G(s) = \frac{g_m R}{1 + sRC} \tag{2.13}$$

$$G_f(s) = \frac{g_{mf} R}{1 + sRC} \tag{2.14}$$

where g_{mf} is the transconductance of the active feedback stage. The overall transfer function of the three-stage amplifier without active feedback is $G^3(s)$, which has three repeated real poles of $W_{p1-3}=(RC)^{-1}$, while adding active feedback G_f results in an overall transfer function of $G^3(s)/(1+G^2(s)G_f(s))$ with one non-dominant real pole and two dominant complex conjugate poles [85]. Indeed, an active feedback shapes the placement of the poles of a uniform three-stage amplifier. Selecting an appropriate gain for the feedback stage ($\beta=g_{mf}R$) increases the overall bandwidth of the amplifier at the cost of degrading the to-

tal gain of the amplifier. Cascading the third-order active feedback amplifiers increases the gain of the amplifier. However, it may result in a large peaking at the frequency response and overshoot and ripple in the transient response of the amplifier [85]. Using interleaved active feedback further improves the overall bandwidth of the cascaded third-order active feedback amplifiers and suppresses the gain peaking [85]. Figures 2.18(a) and 2.18(b) show the block diagram of two cascaded third-order active feedback amplifiers without and with interleaved feedback, respectively. Figure 2.19(a) compares the simulated frequency re-

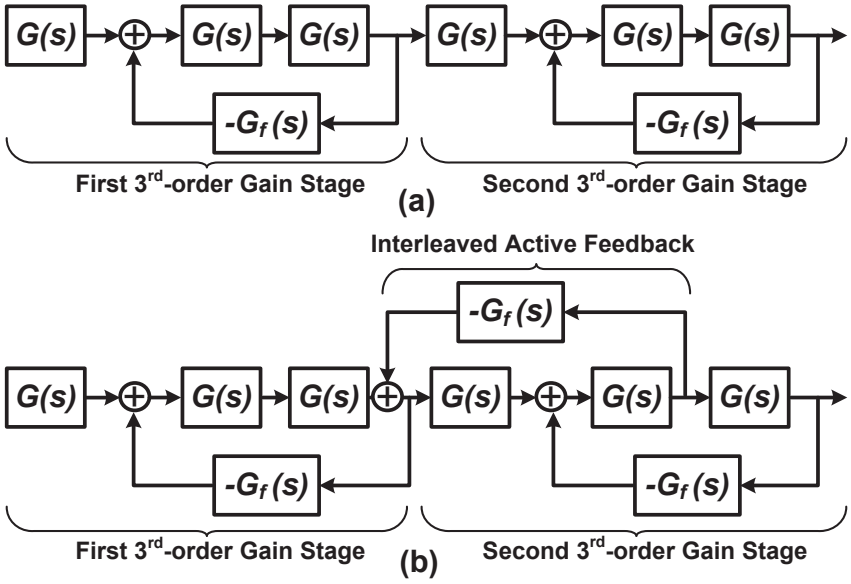


Fig. 2.18 (a) Block diagram of two cascaded third-order active feedback amplifiers; (b) block diagram of two cascaded third-order active feedback amplifiers with interleaved feedback [85].

sponse of a six-stage amplifier without active feedback, with active feedback (Fig. 2.18(a)) and with interleaved active feedback (Fig. 2.18(b)). In this simulation R, C, g_m, and g_{mf} are considered to be 100 Ω, 200 fF, 25 m℧, and 2 m℧ (results in feedback gain of β= 0.2), respectively. Simulation results show that the bandwidth of a six-stage amplifier increases by more than 3.3 times with active feedback at the cost of 14 dB gain degradation. Using interleaved active feedback increases the bandwidth by more than 3.8 times with a flat response at the cost of 16 dB gain reduction. Figure 2.19(b) shows their pole locations. The

radial and half circle dashed lines in Fig. 2.19(b) represent the damping factors and the natural frequencies, respectively. The six-stage amplifier without active feedback has six coincide real poles of $W_{p1-6}=(RC)^{-1}=$ 50 GHz (blue cross). The six-stage amplifier with active feedback also has six poles: two coincide real poles and two repeated sets of two complex conjugate poles (red crosses). The six-stage amplifier with interleaved active feedback has two real poles and four complex conjugate poles shown with black crosses. Indeed, the interleaved active feedback separates the repeated poles of two cascaded third-order active feedback amplifiers and shapes the frequency response.

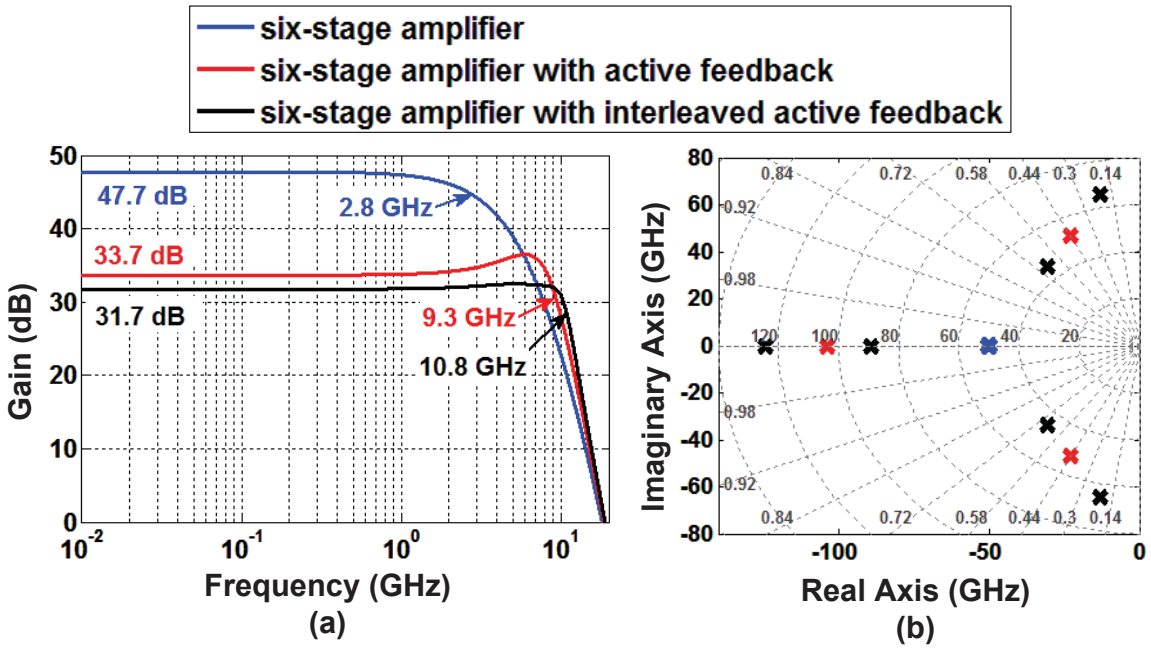


Fig. 2.19 (a) Frequency response of a six-stage amplifier without active feedback, with active feedback, and with interleaved active feedback; (b) their pole locations.

Positive Feedback (PFB)

Using a local positive feedback (PFB) to extend the bandwidth of an inverter-based TIA was briefly proposed in [87] and the analysis of the PFB technique was presented in [88]. Figure 2.20 shows the schematic of an inverter-based TIA with an inverter-based CH am-

plifier and a positive feedback around the first section of the inverter-based Cherry-Hooper (CH) amplifier. In this figure, R_{in} is the input resistance of the CH amplifier with positive

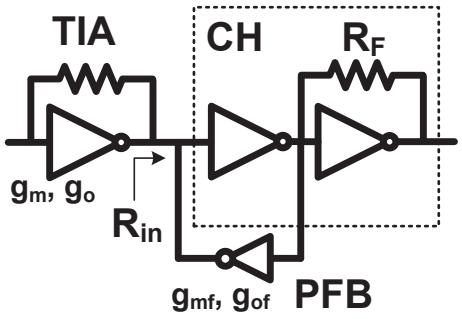


Fig. 2.20 Schematic of an inverter-based TIA and CH amplifier with positive feedback (PFB).

feedback, and each forward inverter has a total transconductance of g_m and total output conductance of g_o. The g_{mf} and g_{of} are the total transconductance and total output conductance of the positive feedback inverter, respectively. The input resistance of the inverter-based CH amplifier is loading the TIA and is given by [88]:

$$R_{in}^{-1} = G_{in} = g_{of} - \frac{g_{mf}g_m}{g_m + g_o} = (\frac{1}{A_v} - \frac{A_v}{1 + A_v})g_{mf} \tag{2.15}$$

where, A_v is the gain of an inverter, and it is equal to g_m/g_o [88]. The gain should be larger than 1 to amplify the input signal, thus, the G_{in} is negative. The negative resistance at the input of CH amplifier extends the bandwidth of the previous stage and also slightly increases the transimpedance gain of the TIA [88].

2.3.4 Power Penalty in Optical Receivers

Measuring the bit error rate (BER) as a function of received optical power is one of the main criteria to evaluate the performance of an optical receiver. As discussed in section 2.1.1, the BER of a transmission system initially is determined by the total noise

level at the input of the receiver. For example, if the total input-referred noise of a broadband optical receiver has a standard deviation of $\sigma_{input-referred}$, it requires an input current peak-to-peak of $14\times\sigma_{input-referred}$ for BER of 10^{-12} [73]. Note that the input current is proportional to the received optical power based on the responsivity of the photodetector. The required optical power to achieve a given BER known as sensitivity of the optical receiver. Impairments in the transmitter, fiber, and receiver increase the required optical power for a given BER. Power penalty (PP) is a useful tool to quantify the impairments and is defined as the additional transmitted optical power required to achieve the same BER as in a system without the impairment. Power penalties in dBs are using the conversion of 10log(PP) [90]. The limited bandwidth of an optical receiver, low cut-off frequency, offset of the decision threshold, an ambiguity of the decision threshold, and jitter of the sampling time are some of the main impairments in an optical receiver. The issues of limited bandwidth and low cut-off frequency are related to the receiver front end and are briefly discussed here.

Bandwidth

As mentioned in Appendix A, the smaller bandwidth of an optical receiver reduces the total input-referred noise. However, the limited bandwidth causes signal distortion known as inter-symbol interference (ISI). The limited bandwidth degrades the high-frequency components of the received data and causes finite rise time and fall times. Therefore, the magnitude level of each bit is affected by the magnitude of the previous bits. Figure 2.21 compares the eye diagram without ISI and with ISI [90]. In Fig. 2.21(a) the signal without ISI has the maximum eye opening of V_E. The ISI degrades the maximum eye opening to V'_E (Fig. 2.21(b)). Hence, as shown in Fig. 2.21(c), to achieve the same BER as for the eye diagram without ISI, a larger signal is required. As a result, the power penalty is $PP=V_E/V'_E$ [90]. Note that this power penalty estimation is based on the worst-case eye

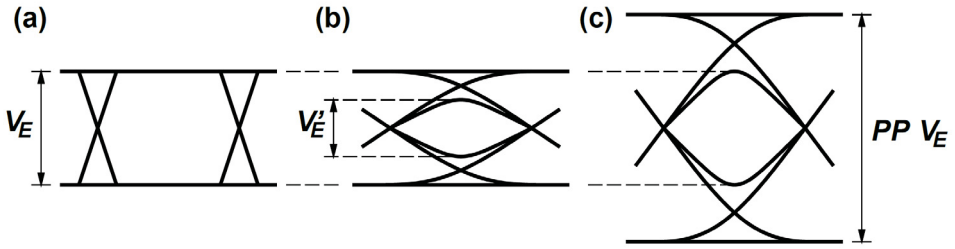


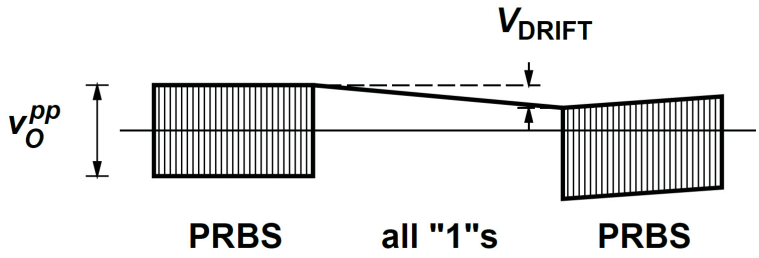
Fig. 2.21 Eye diagram (a) without ISI, (b) with ISI, (c) with ISI and increased signal amplitude to achieve the original BER [90].

opening. Therefore, the actual power penalty would be smaller than this estimation.

Low Cut-Off Frequency

Device mismatches in the fabricated receiver, low-frequency noises, and DC current from a DC-coupled photodetector generate an offset voltage that changes the bias point of the optical front end and may saturate the output swing. To avoid this issue, usually, an offset cancellation (OC) feedback is used that reduces the low-frequency gain and generates a low cut-off frequency (f_{LF}). In addition to suppressing the offset voltage, the offset cancellation feedback degrades the low-frequency components of the receiver data. Hence, the output level may degrade significantly during a long string of identical bits (also known as runs). As shown in Fig. 2.22 the output level drifts during a long run [90]. Also, the drift of the output signal, which is known as baseline wander, may generate data dependent jitter [90]. To minimize baseline wander effect, the time constant of $1/(2\pi f_{LF})$ should be sufficiently larger than the longest run of the data pattern. Assuming a linear system with a single-pole high-pass filter transfer function, the drift voltage after r consecutive zeros or ones is given by

$$V_{DRIFT} = \frac{V_O^{pp}}{2}\left[1 - exp(-2\pi f_{LF}\frac{r}{B})\right] \tag{2.16}$$
$$\frac{1}{2\pi f_{LF}} \gg \frac{r}{B} \Rightarrow V_{DRIFT} \approx \frac{V_O^{pp}}{2}\left(\frac{2\pi f_{LF}}{B}\right) r$$



PRBS: pseudo random bit sequence.

Fig. 2.22 The effect of low cut-off frequency; the output signal drifts during a long string of ones [90].

where B is the bit rate [90]. The power penalty caused by the drift voltage is given by PP=1+2V$_{DRIFT}$/V$_O^{pp}$ [90]. Assuming a value for the power penalty (PP), the highest allowable low cut-off frequency calculated by $f_{LF}<(PP-1)B/(2\pi r)$. For example, assuming a run-length of r=72 (in SONET system) and bit rate of B=10 Gb/s and for 0.2 dB power penalty, the f_{LF} should be lower than 1.04 MHz [90].

2.4 Summary

This chapter provided the background information about three topics that are discussed in the following chapters. For the first topic, we went over the basics of forward error correction techniques and hard-decision decoding and soft-decision decoding. The equations required for evaluating the error performance of an optical link were reviewed. For the second topic, the fundamentals in silicon photonics (SiP) platforms and SiP photodetectors were presented. Finally, a typical structure of an optical receiver front end was discussed, and different topologies of the transimpedance amplifier (TIA) and post-amplifier stage were presented. Also, a brief background on the feedback TIA, Cherry–Hooper (CH) post amplifier, interleave active feedback techniques, positive feedback, and power penalties in receiver front ends were provided.

Chapter 3

Analysis of Low-Bit SD-FEC Optical Front Ends

This chapter presents a novel methodology for evaluating the error performance of a multi-branch optical SD-FEC receiver before its hardware implementation. For the presented methodology, low density parity check (LDPC) codes are used which are powerful codes that perform close to Shannon's capacity limit [91]. They have been proposed for next generation high-speed optical communications [14, 36] and are now defined in standards for submarine optical communications [35] and wireless communications [92]. In this chapter, a long block length LDPC (32768, 26803) is used to compare the decoding performance of different front end configurations. A long block length code is more suitable for long-haul application and not necessary appropriate for certain applications related to short-reach optical interconnects where low latency, less complex and more power efficient encoder and decoder modules are required. In such applications, a shorter block length code is more practical and is used for the experimental validation of the methodology. The work presented in this chapter has been published in Journal of Optical Communications and Networking (JOCN) [29].

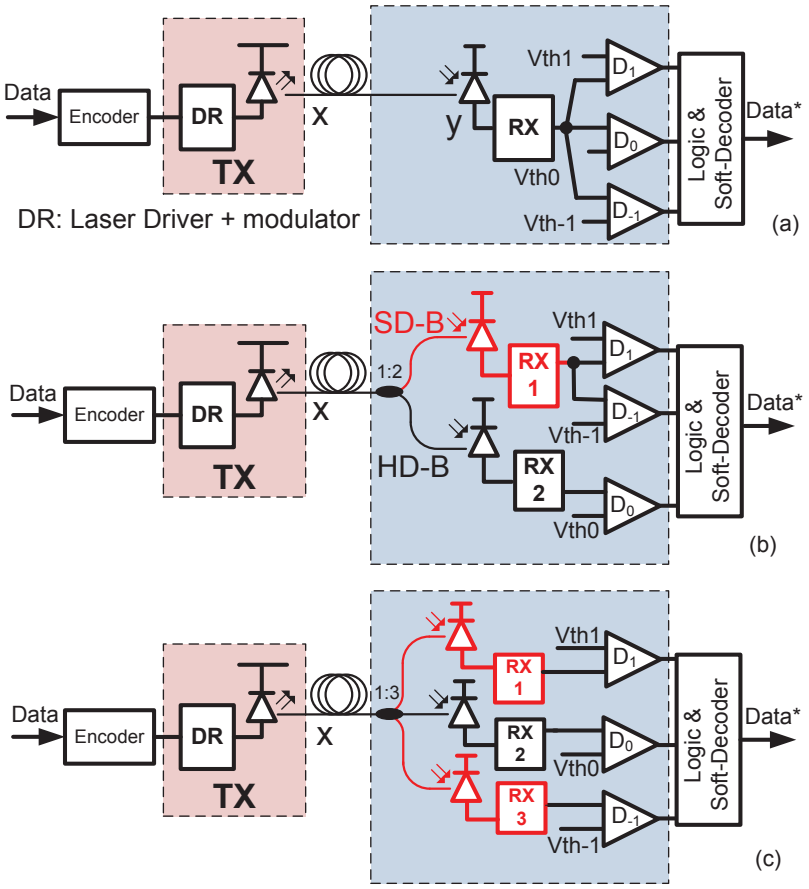
3.1 Soft-Decision Receiver Configurations

In this section, different front end configurations of an optical soft-decision receiver are presented and the properties of each configuration are discussed. Considering the possible hardware implementations of an optical SD-FEC receiver, we categorized the configurations in three major categories:

1. Electrical fan-out
2. Hybrid fan-out
3. Optical fan-out

Schematic diagrams of the three categories are illustrated in Fig. 3.1 for 2-bit soft-decision optical receivers for a fiber-based optical link. The first receiver front end configuration, the electrical fan-out in Fig. 3.1(a), is a conventional implementation of a soft-decision optical receiver [28]. The photodetector converts the received optical signal to an electrical signal that is amplified by the transimpedance amplifier (TIA) and the post-amplifier stages, shown here as an RX block. The amplified signal is fed to the 2-bit ADC that consists of three decision circuits (D_{-1}, D_0, D_1). In this configuration, the hard and soft information are extracted electrically by comparing the same signal with three different threshold levels. The hard-decision bit and confidence-bit are obtained from the hard-decision threshold V_{th0} and the soft-decision thresholds V_{th-1} and V_{th1}, respectively.

The second front end configuration was first proposed and implemented in [39], and consists of the soft information being separated optically from the hard-decision bit (Fig. 3.1(b)). The received optical data is coupled unequally to two branches. Two photodetectors convert the optical signal to electrical signals that are amplified by TIAs and post-amplifier stages (RX1 and RX2). The hard-decision bit and confidence-bit are extracted from two different branches called hard-decision branch (HD-B) and soft-decision branch (SD-B). This architecture is referred to as the hybrid fan-out, since the signal is



DR: Laser Driver and modulator, **TX:** Transmitter, **RX:** Receiver circuits, **Di:** Decision circuit, **SD-B:** Soft-Decision Branch, **HD-B:** Hard-Decision Branch.

Fig. 3.1 Optical link with three major configurations of 2-bit soft-decision receiver.

fanned-out optically to the hard-decision and soft-decision branches and that the signal is split electrically to the two decision circuits within the soft-decision path.

In the third configuration (Fig. 3.1(c)), referred as the optical fan-out, the signal is extracted optically to all three decision circuits. The coupler ratio can be completely balanced with a third of the optical power directed to each decision circuit, or unbalanced.

3.1.1 Uncorrelated Noise in Multi-Branch Receiver

In an electrical fan-out configuration, the three decision circuits compare the same signal but with different thresholds. The noise presented to the decision circuits is therefore correlated since it originates from the same source. In the hybrid and optical fan-out front ends, however, the received signal is detected by different photoreceivers, two in the case of the hybrid fan-out and three in the case of the optical fan-out. This give rises to uncorrelated sources of noise from the photodetector, the TIA and post-amplifiers. Consequently, the decision circuits are handling signals with different noise characteristics. In other words, the noise at the input of each decision circuit D_1, D_0, and D_{-1}, will have common noise sources prior to the optical coupler splitting the signal and uncorrelated noise sources after the optical coupler. Since the channel noise is the dominant source of noise in an optically amplified link, the common noise is larger than the uncorrelated noise. In nonamplified short-reach applications, receiver noise becomes the dominant source of noise leading to more uncorrelated noise at the decision circuit.

Interestingly, uncorrelated noise generates inconsistent encoding at the output of the decision circuits that may occur in either an amplified or nonamplified optical link. Inconsistency exists when the three decision circuits generates a 3-bit code that cannot be represented as a thermometer code. The phenomenon is illustrated in Fig. 3.2 with an example where a received signal is plotted as it would appear in the hard-decision branch and the soft-decision branch. While the two signals should be similar, the uncorrelated noise from the multiple branches (two branches in this example) leads to changes in the received data points "A" and "B" in the soft-decision branch. For data point "A", the hard-decision bit is 1 (in green) as the signal amplitude is above the threshold (V_{th0}) but the soft-decision branch generates 0 for both thresholds (V_{th1} and V_{th-1}) which leads to a high confident bit of 1 ($\overline{D_1 \oplus D_{-1}} = 1$). However, based on the sampled data "A" in

hard-decision branch, the confidence bit should be 0. Similarly, for data point "B", the confident bit is a 1 as the data is above both thresholds whereas the hard-decision branch sees a data point that should be a 0 with lower confidence, i.e., 0.

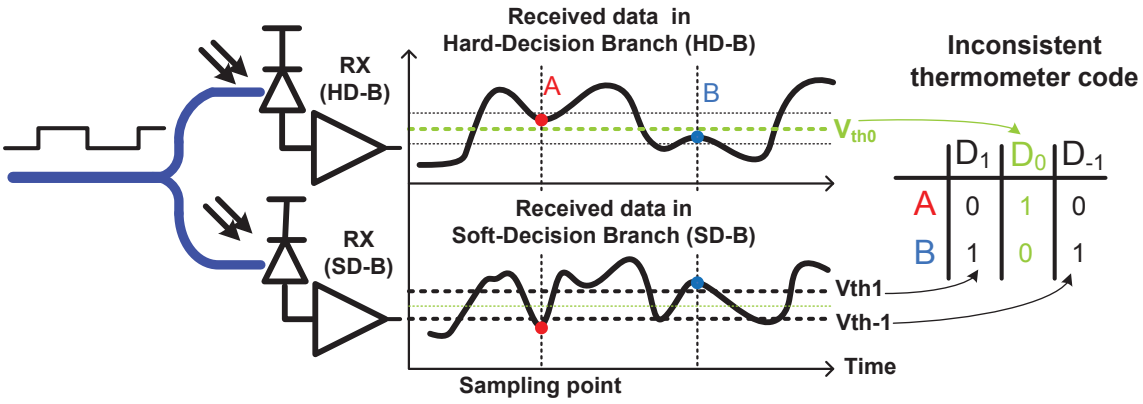


Fig. 3.2 An example of a received signal in the hard-decision (top) and soft-decision (bottom) branches of an hybrid fan-out configuration that leads to inconsistent thermometer codes for sample data point A and B. (Thin dashed lines corresponding to the threshold of the other branch shown for references only).

Inconsistency, it turns out, may arise for up to four possible cases which are listed in Table 3.1. In general, an m-bit thermometer code provides a digital representation of the outputs of m decision circuits, comparing the sampled data to m thresholds from the lowest to the highest in voltage. There are 0 to m sequential 1s in a thermometer code (i.e., [...0000], [...0001], [...0011], [...0111], [...1111]...). For an m-bit thermometer code, (m+1) codes are expected, referred to as *"consistent thermometer codes"*. Considering the 2^m possible binary representation, this means that there are 2^m-(m+1) binary codes that are not expected. These are the code referred to as *"inconsistent thermometer codes"*.

In an electrical fan-out configuration (Fig. 3.1(a)), the inconsistencies comes from offset noise in the threshold of the decision circuits and degrade the decoding performance and need to be filtered [37]. In multiple-branch front ends such as the hybrid and optical fan-out (Figs. 3.1(b) and 3.1(c)), inconsistent thermometer codes are generated even with ideal decision circuits without threshold offset fluctuation. More precisely, the source of

Table 3.1 Inconsistence cases for the 3-Bit binary data

D_1	D_0	D_{-1}	Thermometer code
0	0	0	Consistent
0	0	1	Consistent
0	1	0	Inconsistent
0	1	1	Consistent
1	0	0	Inconsistent
1	0	1	Inconsistent
1	1	0	Inconsistent
1	1	1	Consistent

inconsistency in hybrid and optical fan-out is the uncorrelation between the two branches rather than the nonideality of the decision circuit.

To study the inconsistent thermometer codes, a Monte-Carlo simulation is used with over 10^6 random binary bits. White Gaussian noise with a standard deviation σ_{common} is added to the received signal, and then divided between the branches based on the receiver configuration. In each path, another Gaussian noise with standard deviation σ_i is added to the signal where i is 1 and 2 for the hybrid fan-out configuration, and $i = 1, ..2^N - 1$ for the optical fan-out configuration. The signal in the hard-decision branch is compared with its hard-decision threshold. The signal in the soft-decision branches are compared with the corresponding soft-decision thresholds. The generated code is counted and reported as a logic table such as Table 3.2. In Table 3.2, the column $x = 0$ represents the number of times the specific thermometer code (in a row) was generated when the transmitted data was a logic 0. Likewise, column $x = 1$ represents the number of times the code was generated when the transmitted data was a logic 1. The conditional probabilities that a logic 1 or a logic 0 is transmitted are given in columns $P(x = 0|y)$ and $P(x = 1|y)$, respectively, calculated using equation (2.4). The logarithm of the likelihood of the received signal of

each thermometer code is then calculated using (2.3) is given in column LLR(y).

Table 3.2 shows an example for the hybrid fan-out front end (Fig. 3.1(b)) with a 50/50 optical coupler, splitting 50% of the optical power in each branch. No optical amplifiers are considered in short-reach optical link and the transmitter and channel noise are set to represent 10% of the total noise while the receiver noise in each branch is dominant and represent 90% of the total noise. The $Q-$factor in each branch is equal and is set to 4.8 dB. In total, 2^{20} uncoded bits were transmitted with half of the bits being 0s and half of the bits being 1s. Simulations can be done for various splitting ratios and with different percentage of noise contribution to represent both amplified links (i.e., long-haul links) and nonamplified links (i.e., short-reach links). The number of occurrences of each inconsistent thermometer code in a amplified link is lower than that of the short-reach application because the dominant effect of channel noise leads to more similar received signal in two branches. From the simulation results presented in Table 3.2, a received signal y leading to an inconsistent code of [101] has greater probability of originating from a binary 1 since the calculated LLR value is positive 0.50. This result is explained from the observation that the soft-decision branch has a soft-decision threshold V_{th1} above the hard-decision threshold while both branches have the same signal power for the case 50/50 (50% optical power in each branch). Therefore, the decision in the soft-decision branch is more reliable than the decision in the hard-decision branch since the sampled data is above the two soft-thresholds (V_{th-1} and V_{th1}). In the case that more of the optical power is in the hard-decision branch, the dominant decision will be based on the hard-decision bit.

Table 3.2 shows that by considering the inconsistent thermometer codes, six LLR values can be fed to the decoder instead of four LLR values. Therefore, it is expected that the two additional LLR values improve the decoding due to the more accurate estimation of initial LLR value of the received sample. The effect of inconsistent thermometer codes and additional LLR values on the decoding performance is investigated in section 3.2.

Table 3.2 Monte-Carlo simulation results example for short-reach link with hybrid fan-out 50/50 receiver

Thermometer code			$x=0$	$x=1$	$P(x=0\|y)$	$P(x=1\|y)$	LLR
D_1	D_0	D_{-1}					
0	0	0	468818	862	0.4471	0.0008	-6.30
0	0	1	21569	1372	0.0205	0.0013	-2.75
1	0	1	11899	19522	0.0113	0.0186	0.50
0	1	0	19848	11904	0.0189	0.0114	-0.51
0	1	1	1324	21942	0.0012	0.0209	2.81
1	1	1	830	468686	0.0008	0.4470	6.33

3.1.2 Methodology for Multi-Branch Soft-Decision Receivers

The methodology to assess the optimum soft-decoding error performance of each receiver front end is discussed in this section. The methodology uses Monte-Carlo simulation by considering the noise statistics related to the link properties and the optical front end configuration. The following 9 steps define the methodology:

Step 1. Specify the link properties: the relative intensity noise (RIN) of the laser, the extinction ratio (ER) of the modulator, the gain and noise figure of the EDFAs for amplified links, the rectangular equivalent optical bandwidth (B_{opt}) of the optical filter, the effective electrical bandwidth of the front end circuit (B_e), the responsivity (R) and dark current (I_d) of the photodetector, the resistance load of the photodetector, the noise coefficient NF of the receiver front end, and the required Q-factor.

Step 2. Generate a random data frame and encode it using the selected code.

Step 3. Calculate the standard deviation of common noise (σ_{common}) and uncorrelated noise (σ_i) based on the optical link properties and the receiver front end configuration, for each binary level. In the cases of the hybrid and optical fan-out configurations, the common noise is added to the encoded data before splitting and the uncorrelated noise is added to

the split optical signal.

Step 4. Determine soft- and hard-decision threshold. Selecting appropriate hard-decision and soft-decision thresholds is an important part that affects the decoding performance, as discussed in Appendix B. Based on the statistics of the received data in the hard-decision branch, an appropriate hard-decision threshold is selected. However, for selecting appropriate soft-decision thresholds, we need to sweep them and calculate the total post-FEC bit error rate (BER). Therefore, for each Q-factor, step 2 to step 9 are repeated for various soft-decision thresholds to find the optimum thresholds. Note that in multi-branch fan-out configuration, the calculation of hard-decision threshold setting is based on the statistics of the PDFs in the hard-decision branch and the calculation of soft-decision threshold setting is based on the statistics of the PDFs in the soft-decision branch.

Step 5. The noisy signal in each branch is compared with the corresponding thresholds to generate a thermometer-coded signal.

Step 6. The generated consistent and inconsistent thermometer codes are counted and a logic table such as Table 3.2 is formed. The calculated LLR values are fed to the SPA iterative decoder.

Step 7. Run the SPA iterative decoder. The decoder stops if it finds a valid code word or if the number of iteration reaches an iteration limit.

Step 8. Calculate the number of erroneous bits in the frame, and go to step 2 for the next frame until all the frames are decoded

Step 9. Calculate the total post-FEC bit error rate (BER) and frame error rate (FER).

3.1.3 Optical Coupler Ratio Versus Q–factor

The effect of optical power splitting in the hybrid and optical fan-out configurations on the Q-factor is studied in this subsection. It is assumed that all receiver configurations have received the same optical power before the optical splitter. The Q-factor for each branch

is calculated for two cases: 1) when the dominant noise source occurs before the splitter, i.e., from the transmitter and the optical channel, and 2) when the dominant noise source is after the splitter, i.e., from the receiver. Table 3.3 summarizes the Q-factor in (dB) in each branch for various configurations.

Table 3.3 Branch $Q-$factor comparison for the three configurations

2-bit SD topology	Dominant TX and channel noise		Dominant RX noise	
	HD-B Q-factor	SD-B Q-factor	HD-B Q-factor	SD-B Q-factor
E fan-out	8.00 dB	——	8.00 dB	——
H, 90/10	7.94 dB	0.41 dB	7.09 dB	-11.95 dB
H, 80/20	7.85 dB	4.50 dB	6.07 dB	-5.94 dB
H, 70/30	7.74 dB	6.09 dB	4.92 dB	-2.42 dB
H, 60/40	7.56 dB	6.87 dB	3.58 dB	0.07 dB
H, 50/50	7.30 dB	7.30 dB	2.00 dB	2.00 dB
O, 90/5/5	7.94 dB	-4.90 dB	7.09 dB	-17.97 dB
O, 80/10/10	7.85 dB	0.41 dB	6.07 dB	-11.95 dB
O, 70/15/15	7.74 dB	3.00 dB	4.92 dB	-8.43 dB
O, 60/20/20	7.56 dB	4.50 dB	3.58 dB	-5.94 dB
O, 50/25/25	7.30 dB	5.45 dB	2.00 dB	-4.00 dB
O, 33/33/33	6.41 dB	6.41 dB	-1.51 dB	-1.51 dB

HD-B: hard-decision branch; **SD-B**: soft-decision branch, **E**: electrical fan-out;
H, x/y: hybrid fan-out with "x" percent of optical power in hard-decision branch and "y" percent of optical power in soft-decision branch;
O, x/y/y: optical fan-out with "x" percent of optical power in hard-decision branch and "y" percent of optical power in soft-decision branches.

In an optical link where the transmitter and channel noise sources are dominant such as in an optically amplified long-haul links (in the simulated optical link, the common noise has 87% contribution to the total noise), the effect of optical power splitting on the received Q-factor for the hard-decision bit is small as long as the received signal is sufficiently large compared to the receiver noise level. For instance, in the particular simulated link, the

Q-factor in the hard-decision branch varies by only 0.64 dB and 1.53 dB for the hybrid and optical fan-out configurations, respectively. However, the soft-decision branch suffers significantly from the optical power splitting. For example in Table 3.3, the hybrid fan-out configuration with a 90/10 splitter (row H, 90/10), the Q-factor in the soft-decision branch exhibits a significant degradation since only 10% of the optical signal is in that branch such that receiver noise becomes comparable with the received signal. Compared to the hybrid fan-out configuration, the degradation in the soft-decision branch is considerably worst for the optical fan-out configuration, up to 5.31 dB when comparing for the same ratio of optical power in the hard-decision branch (e.g., O, 90/5/5 versus H, 90/10). On the other hand, when the receiver noise is the dominant noise source such as in unamplified short-reach links (in the simulated optical link, the receiver noise has 96% contribution to the total noise), the Q-factor in each branch degrades dramatically regardless of the branch. For instance, the Q-factor degrades by 0.91 dB compared to the electrical fan-out configuration even with 90% of the optical power in the hard-decision branch. This can easily be explained since the signal amplitude is degraded by 10% while the noise remains the same. The Q-factor degradation in each branch is approximately $\triangle Q \approx 20 \times \log_{10}(XC)$, where XC is the degradation ratio of optical power in the branch of the fan-out configuration. In the hybrid topology H, 50/50 where XC=0.5, the degradation of Q-factor is -6 dB. In some topologies, the Q-factor of the received signal in the soft-decision branch is negative such that the noise is larger than the signal.

Based on the calculated Q-factor shown in Table 3.3, in an optical link with dominant receiver noise, the soft-decision decoding with optical fan-out receiver is expected to have poor error performance compared to other configurations. Considering the dramatic degradation of the signal quality due to the optical power splitting, the electrical fan-out is the best way to implement a 2-bit SD-FEC receiver for an unamplified optical link for short-reach applications. To study the effect of uncorrelated noise on the decoding per-

formance and the quality of the signal required for the soft-decision branch, the proposed methodology is used and the results are discussed in the following section.

3.2 Error Performance Investigation

This section compares the error performance of the different soft-decision front ends and the impact of their respective configurations. In the first comparison, the received optical power is fixed for all receiver schemes to study the effect of the optical coupler ratio. A second comparison sets the Q-factor of the received signal to be the same in the hard-decision branch for all configurations to evaluate the impact of uncorrelated noise and inconsistent thermometer codes. Further, this latter comparison will determine the minimum signal-to-noise required for the soft-decision branch.

For the investigation, an LDPC (32768, 26803) code is used. The code has a 22.25% overhead with a code rate (CR) of 0.818 (CR=26803/32768). Hence, 0.87 dB of optical power is used for transmitting the overhead bits. To account for this overhead, a correcting factor of -10log(CR) is added to the Q value of the post-FEC BER curves [93]. For each simulated point of post-FEC BER in this section, approximately 6.5×10^7 encoded random bits are simulated.

Note that the optical fan-out configuration has similar performance limitations as the hybrid fan-out due to the optical couplers. Therefore, only the decoding performance of the hybrid fan-out and the electrical fan-out is presented. Since the optical fan-out has more degradation of the Q-factor in the soft-decision branches compared to the hybrid fan-out with the same ratio of optical power in the hard-decision branch, the decoding performance of optical fan-out is further degraded with respect to the hybrid fan-out.

3.2.1 Impact of Coupling Ratio

The decoding performance of the hybrid fan-out and the electrical fan-out configurations are presented as post-FEC BER versus pre-FEC Q-factor for both amplified and unamplified links. For all simulation results, the uncoded, hard-decision and unquantized BER curves are provided for reference.

Amplified Optical Link with Dominant Channel Noise

An optically amplified link with a hybrid fan-out front end receiver has first been studied experimentally in [39] with a block code LDPC (32000, 29759). However, the XNOR gate was used to generate the confidence-bit of the soft-decision branch from the two decision circuits D_{-1} and D_1. As such, the uncorrelated noise effect and possible inconsistent thermometer codes could not be observed since only the XNOR gate output information was available. Thus, the added information from the inconsistent codes was not used for better LLR estimation. Even worse, for the H, 50/50 configuration, the generated confidence-bit from the inconsistent codes is incorrect and degrades the decoding performance due to incorrect estimation of the LLR values of the received data. For example, the received thermometer code [101] was interpreted as [01] (or a strong-decision logic 0). Based on the Monte-Carlo simulation results in Table 3.2, code [101] should be considered as a weak-decision logic 1.

The amplified optical link is simulated with the channel and transmitter noise set to 87% of the total noise. Figure 3.3 shows post-FEC BER versus pre-FEC Q-factor for 2-bit electrical and hybrid fan-out while the confidence-bit is generated from ($\overline{D_1 \oplus D_{-1}} = 1$) and the initial LLR values are calculated based on 2-bit soft data. The simulation results show decoding performance similar to experimental results in [39]. The results show that the 2-bit electrical fan-out exhibits a 0.5 dB penalty over a hypothetical soft-decision configuration

with unquantized LLR but a 0.75 dB improvement over hard-decision. The results shown in Fig. 3.3 also show that for the hybrid fan-out configuration with optical ratios of 80/20 and 90/10, more optical power in the hard-decision branch leads to a better decoding performance than a pure hard-decision decoding. From optical ratios of 70/30, 60/40, and 50/50, the performance is worse than hard-decision since the signal-to-noise ratio of the hard-decision branch is degraded more and the LLR values are estimated incorrectly due to the use of XNOR in the soft-decision branch. The best performing hybrid configuration is 0.54 dB worse than the 2-bit electrical configuration.

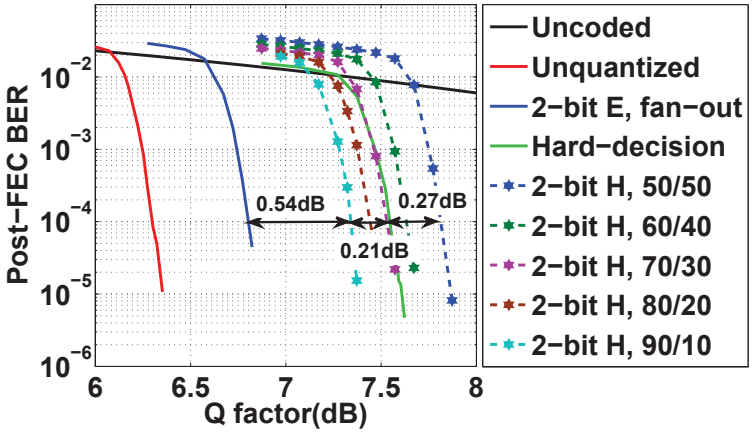


Fig. 3.3 Decoding performance of the 2-bit soft-decision front end receivers using LDPC (32768, 26803) in optically amplified optical link, using XNOR to extract the confidence-bit.

The post-FEC BER is now re-evaluated when the LLR quantization levels are calculated using the output of the decision circuits $[D_{-1}, D_0, D_1]$ rather the logical output of $(\overline{D_1 \oplus D_{-1}})$. As shown in Fig. 3.4, the hybrid fan-out configurations have 0.27 dB to 0.43 dB better decoding performance than the conventional hard decision. In addition, they have better decoding performance when compared with Fig. 3.3. For example, a 50/50 optical coupler ratio in the hybrid configuration leads to a 0.7 dB improvement when the benefit of uncorrelated noise is exploited. Indeed, the improvement comes from the strong

benefit of the inconsistent thermometer codes that adds additional LLR quantization levels for a better estimation. Despite the performance improvement, the best performing hybrid configuration remains 0.32 dB worse than the 2-bit electrical configuration.

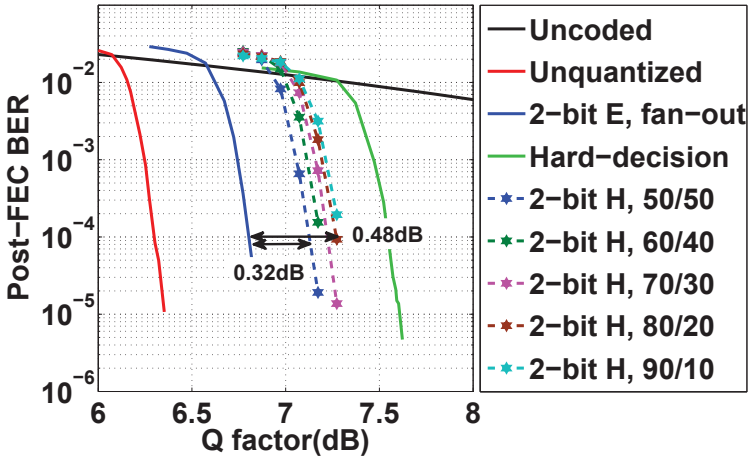


Fig. 3.4 Decoding performance of the 2-bit soft-decision front end receivers using LDPC (32768, 26803) in optically amplified optical link considering uncorrelated noise in the LLR quantization.

Unamplified Optical Link with Dominant Receiver Noise

An optical link without channel noise (e.g., ASE noise) leads to a link that has dominant receiver noise. In this investigation, the unamplified optical link is simulated with 96% of the total noise being the receiver noise. The error performance for the electrical and hybrid fan-out configurations is shown in Fig. 3.5. In this link, the received Q-factor is degraded severely by the optical coupler ratio. For the hybrid fan-out configuration with a 90/10 coupler, the simulated Q-factor results presented in Table 3.3 show a 0.91 dB degradation in the hard-decision branch over the electrical fan-out. However, the decoding performance of the given front end is 2.2 dB worse than the 2-bit soft-decision electrical fan-out. The additional degradation, 2.2-0.91=1.29 dB, is from the negative Q-factor in the soft-decision branch that leads to a wrong estimation of the LLR values. For the hybrid configura-

tion with a 50/50 coupler, the simulated Q-factor results presented in Table 3.3 shows a 6 dB degradation over the electrical fan-out while the decoding performance for a given optical link is degraded by only 4.52 dB over the electrical fan-out. Thus, the inconsistent thermometer codes improve the decoding performance by adding more LLR levels. Some improvement can be seen for the other optical coupler ratio configurations.

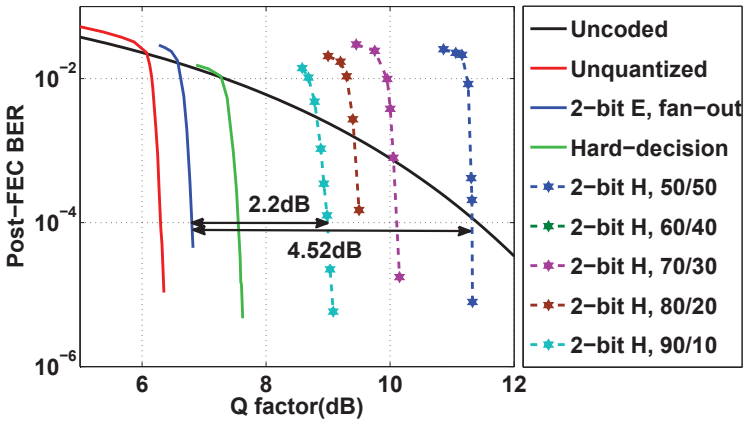


Fig. 3.5 Decoding performance of the 2-bit soft-decision front end receivers using LDPC (32768, 26803) in dominant receiver noise optical link.

3.2.2 Benefit of Uncorrelated Noise

To study the effect of uncorrelated noise in two branches, the Q-factor in the hard-decision branch is kept constant for all optical coupler splitting ratios to isolate the effect from Q-factor degradation in the hard-decision branch. Consequently, the received optical power prior to the coupler is larger in the hybrid fan-out configuration than the electrical fan-out configuration. Figure 3.6 shows the corresponding error performance for the 2-bit electrical and hybrid fan-out configuration. As discussed previously, the hybrid configuration with a 50/50 coupler (blue dashed-line) benefits greatly from the inconsistent codes, exhibiting a 1.47 dB improvement in decoding performance over 2-bit electrical fan-out. In other hybrid fan-out configurations with lower optical power in the soft-decision branch, the

improvement gained from uncorrelated noise is lessened due to degradation of the Q-factor in the soft-decision branch. For instance, the hybrid fan-out configuration with a 60/40 coupler (green dashed-line) shows only a 0.33 dB improvement over the electrical fan-out configuration while a 70/30 coupler has worse performance over the 2-bit electrical fan-out due to the noisy signal in the soft-decision branch.

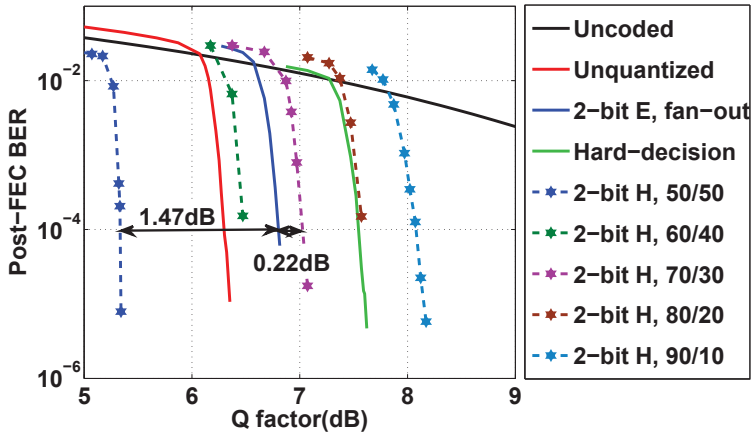


Fig. 3.6 Decoding performance of the 2-bit soft-decision receivers using LDPC (32768, 26803) with constant Q-factor in hard-decision branch.

3.3 Methodology Validation

The proposed methodology to investigate the effect of the configuration in soft-decision decoding is experimentally validated. The 2-bit soft decision receiver for amplified optical links has been studied experimentally in [27,39] and the decoding performance has a similar trend to the simulation result in subsection 3.2.1. Therefore, the methodology is validated in an unamplified short-reach link for electrical and hybrid fan-out configurations. The target short-reach application is related to the optical link with a length of 2 km to 10 km. A short block length LDPC (672, 588) code with a code rate of 0.875, which is adopted for ultra-wideband (UWB) wireless communication applications [92], is used for validation.

Figure 3.7 shows the test setup for validating the proposed methodology. The continuous wave (CW) optical signal from a distributed feedback (DFB) laser source emitting at a wavelength of 1310 nm is injected into a Mach-Zehnder modulator (MZM) with a V_π of 8 V driven by the baseband signal from the output of a programmable bit pattern generator (BPG). The MZM has an insertion loss of 13 dB at 1310 nm. The optical power launched into the fiber is -6 dBm.

Each LDPC block contains 672 bits and by adding 50 blocks of encoded data, a frame is created. Each frame is preceded by 60 unique preamble bits to identify each frame in the received sequence using cross-correlation. Four frames and their respective preambles form a super frame of about 134,640 bits. The super frame of the LDPC code is first loaded onto the BPG using a MATLAB interface.

The 10 Gb/s modulated NRZ-OOK optical signal is sent through 8.3 km of single mode fiber (SMF), with a fiber loss of α=0.38 dB/km and negligible chromatic dispersion at 1310 nm. Since the performance of the electrical or hybrid fan-out front-ends is evaluated based on the Q-factor of the received data, the comparison would be independent of the length of the fiber. Therefore, we used the available fiber with a length of 8.3 km (slightly lower than 10 km) in our setup. A variable optical attenuator (VOA) reduces the optical power to degrade the signal-to-noise ratio in the electrical or hybrid fan-out receiver configuration. For the electrical fan-out configuration, the received signal is fed to a p-i-n photoreceiver that has a 3-dB electrical bandwidth of 11 GHz and a conversion gain of 200 V/W at a wavelength of 1310 nm. The signal is then amplified by a broadband RF amplifier for proper electrical sampling. As for the validation of the methodology for the hybrid fan-out configuration, the received optical signal is fed to an optical directional coupler and both output branches are connected to two identical photoreceivers with a bandwidth of 10 GHz and sensitivity of -18 dBm. The optical receivers are linear for optical power lower than -8 dBm. The available directional couplers have a splitting ratio

of 81/19 and 53/47, respectively, at 1310 nm. A tunable delay line is used to compensate the delay mismatch between the hard-decision (HD) and soft-decision (SD) branches. The sampling oscilloscope is programmed to capture 4 samples per bit. Since only one p-i-n photoreceiver with a bandwidth of 11 GHz and a conversion gain of 200 V/W, which is used for the electrical fan-out configuration, is available in our labs, we used different photoreceivers for evaluating the hybrid fan-out configuration. Note that the performance of the front-ends is evaluated based on the Q-factor of the received data. Also, both types of the photoreceivers used for the electrical and hybrid fan-out configurations are linear and have a large bandwidth with a negligible ISI effect at 10 Gb/s data rate. Therefore, the post-FEC BER comparison is independent of the photoreceiver's type.

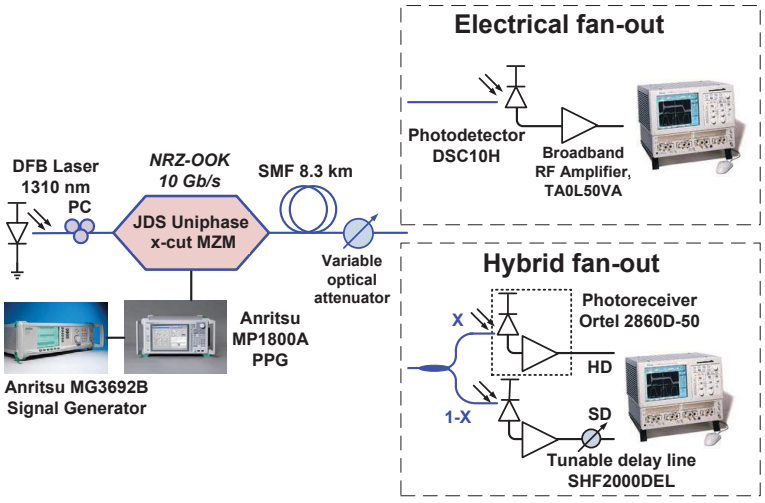


Fig. 3.7 Experimental setup used to validate the proposed methodology for unamplified links with an electrical or hybrid fan-out configuration as the soft-decision receiver.

The sampling oscilloscope has two channels with a 14-bit analog-to-digital converter (ADC) at the input of each channel that samples the received data. In each branch of the hybrid fan-out configuration, the noise of the sampled data has a common part from the noise sources prior to the optical splitter and an uncorrelated noise from the associated photoreceiver. For each measurement, around 1.3×10^6 bits are captured, and the decoding

is performed off-line in MATLAB. The frames are first synchronized using a cross correlation function on the received data with a predefined unique preamble. The signal is then down sampled to 1 sample per bit by selecting the optimum sample based on hard-decision error counting of received data. For the case of the hybrid fan-out configuration, the received signals in both branches down-sampled to 1 sample by selecting the optimum sample based on the hard-decision error counting of the received data in the HD branch. A DC offset added by the oscilloscope is removed. For the electrical fan-out configuration, the initial LLR values are calculated using 2.5 and the iterative SPA decoder is used for decoding the data [42]. For the hybrid fan-out configuration, the initial LLR is calculated considering the inconsistent thermometer codes from quantized data in the HD and SD branches. The optimum thresholds were selected following the method described in Appendix B. The Q-factor of the received signal before the optical splitting is used for comparison.

Due to the larger overlap of two PDFs in low Q-factor values, the calculated Q-factor of the captured sequence is considered to be a weak estimation. Hence, the pre-FEC BER is calculated first and the Q-factor corresponding to the uncoded BER is used as the received Q-factor, rather than calculating the Q-factor from the PDFs directly.

The experimental results are shown in Fig. 3.8. The results are in good agreement with the simulation results for both the electrical and hybrid fan-out configurations, and therefore validate the proposed methodology. The 2-bit electrical fan-out soft-decision decoding has a net coding gain (NGC) of 4.13 dB and 0.915 dB over the uncoded and hard-decision decoding, respectively, for the post-FEC bit error rate (BER) of 10^{-6} using LDPC (672, 588) code. In addition, compared with the 2-bit electrical fan-out configuration, the 2-bit hybrid fan-out configuration degrades the decoding performance by 2.2 dB for the 81/19 coupler. The performance is worse for the 53/47 coupler.

The agreement between the experimental result and the simulation results validate the noise modeling of the multi-branch front end used in the proposed methodology and the

occurrence of the inconsistent thermometer codes in unamplified optical link.

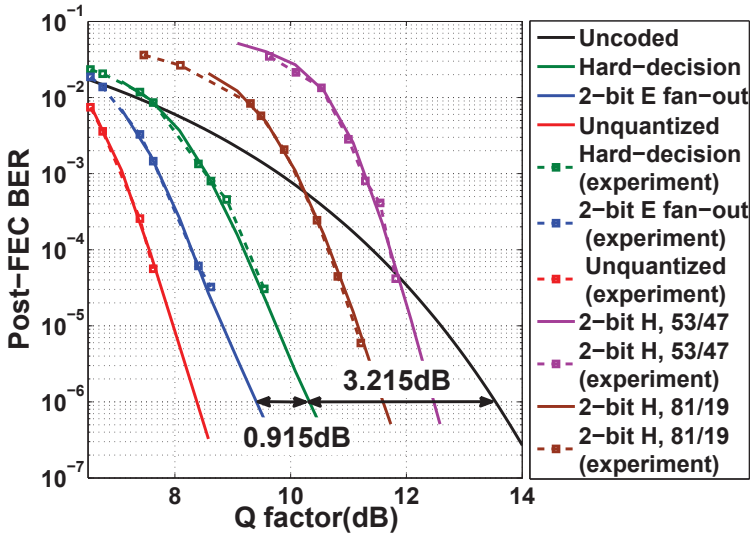


Fig. 3.8 Decoding performance of the 2-bit electrical and hybrid fan-out soft-decision receivers using LDPC (672, 588).

3.4 Summary

In this chapter, the error performance of various fan-out configurations of an optical front end for soft-decision decoder was thoroughly investigated using a novel methodology. The effect of the uncorrelated noise of the receivers in the hybrid and optical fan-out was further analyzed and a new concept of inconsistent thermometer codes and its beneficial effect on the decoding performance was presented. Based on the simulation results for the unamplified optical links, the optical coupler ratio degrades the overall decoding performance compared to conventional hard-decision receiver. Thus, the hybrid fan-out and optical fan-out configurations are not appropriate for unamplified links where the noise is dominant in the receiver.

In comparison with existing electrical fan-out soft-decision front ends [28], the hybrid fan-out configuration provides a number of advantages in terms of linearity, bandwidth,

and power consumption for optically amplified applications, where the channel noise is the dominant noise source [27]. The proposed methodology was experimentally validated and simulation results of the proposed methodology are in good agreement with the experimental results.

Chapter 4

Responsivity Optimization of Germanium Photodetectors

In a silicon photonics (SiP) platform, the waveguide germanium photodetector (Ge-PD) has been the subject of important research in the last decade [51–59]. In short-reach applications, the receiver noise is the dominant noise source. In this context, a detector with larger responsivity improves the receiver sensitivity and further reduces the required electrical gain of the downstream circuits. Consequently, more power-efficient optical interconnections are achieved. This chapter investigates the effect of a Ge-PD's design geometry and the size and location of the top metal contact on the PD's performance. Also, it details a novel methodology for optimizing the responsivity of a high-speed photodetector (PD). The work presented in this chapter has been published as a journal paper in Optics Express [30].

4.1 Vertical Waveguide Germanium Photodetector

This section demonstrates the numerical simulation results obtained using technology computer-aided design (TCAD) tools investigating the impact of top metal contact ge-

ometry and germanium-region dimension on the performance of an evanescently-coupled waveguide germanium-on-silicon PD with a vertical p-i-n diode. Figure 4.1 illustrates the side-view (left figures) and top-view (right figures) of the two approaches to the design of PDs discussed in this chapter. Figures 4.1(a) and 4.1(b) show respectively the side-view and top-view of a Ge-PD with a single centered electrode on top of the n-doped germanium area (dark green). Figures 4.1(c) and 4.1(d) show respectively the side-view and top-view of a Ge-PD with two electrodes on top of the n-doped germanium area. The length (L_{Ge}) and width (W_{Ge}) of the germanium area, the length ($L_{n-doped}$) and width ($W_{n-doped}$) of the n-doped germanium, and the length (L_{seg}) and width (W_{seg}) of the metal contacts are indicated in the figures. The two other contacts on top of the p++ doped silicon area (dark red) represent the anode connection and have only a trivial degradation effect on the bandwidth of the PD. The highly doped silicon (Si-p++) and germanium (Ge-n++) layers form low resistance contacts with the metal layer.

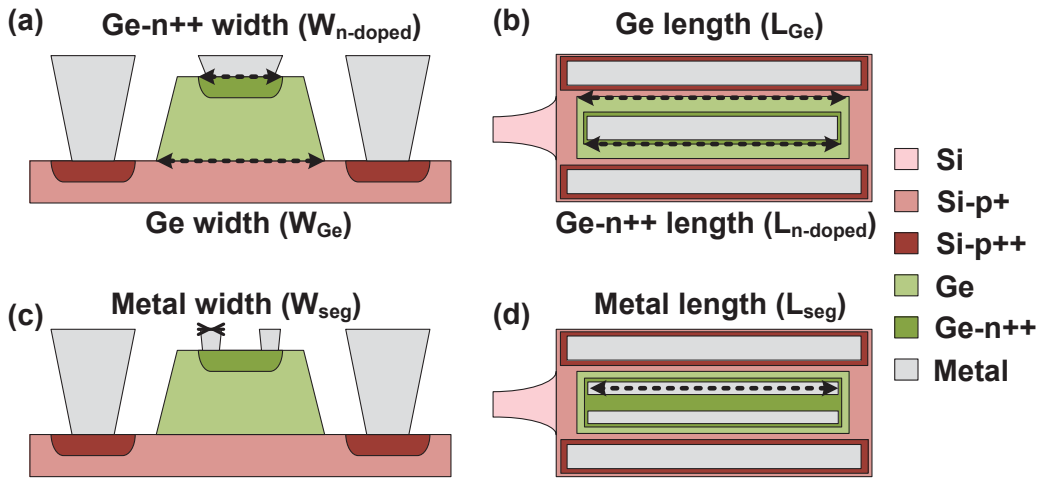


Fig. 4.1 (a) Side-view and (b) top-view of a Ge-PD with a single electrode on top of the n-doped germanium (Ge-n++ in dark green); (c) side-view and (d) top view of a Ge-PD with two electrodes on top of the n-doped germanium.

4.1.1 Impact of Top Metal Contact

Commercial software (Lumerical FDTD and Device [94]) is used to study the degrading effect of the top metal contact on the responsivity of the germanium-on-silicon PD. The three-dimensional (3D) FDTD simulation software is used to calculate the electric field of the light evanescently coupling from the silicon to the germanium, as well as the absorbed optical power per unit volume [48]. Figure 4.2 shows the simulated results for the electric field propagation in a PD with a Ge area of 8 μm$\times$25 μm (indicated by the white box). Figures 4.2(a), 4.2(c), and 4.2(e) show the top view of the electric field, 10 nm below the top interface of the Ge area for a PD without the top metal contact, with a 1 μm wide centered metal contact, and with two off-centered 1 μm wide metal contacts, respectively. Figures 4.2(b), 4.2(d), and 4.2(f) show the corresponding side-views. Note that the large size of the Ge leads to a multimode detector. Figure 4.2(a) shows that the electric field is stronger in the center of Ge area. A centered top metal contact leads to more optical power loss due to metal absorption. Thus, Figs. 4.2(e) and 4.2(f) using two off-centered contacts located where the electric field is weaker would lead to less optical power loss. Increasing the gap between the two metal contacts further decreases optical power loss with better responsivity. The required minimum feature size of a contact via and the minimum distance between two contacts in the fabrication process which is used in this work challenges the use of multi-finger off-centered top contacts (Fig 2.7(c)) compared to two off-centered top contacts (Fig 4.1(d)).

For the simulation, an absorption coefficient of 1800 cm^{-1} at a wavelength of 1550 nm is used for the thin film Ge at room temperature [95]. The results show that a top centered aluminum (Al) contact with a width of 3.6 μm reduces the responsivity by 19% due to metal absorption compared to the simulation result not considering the effect of metal loss. With two off-centered smaller size contacts with a gap distance of 2 μm, the responsivity

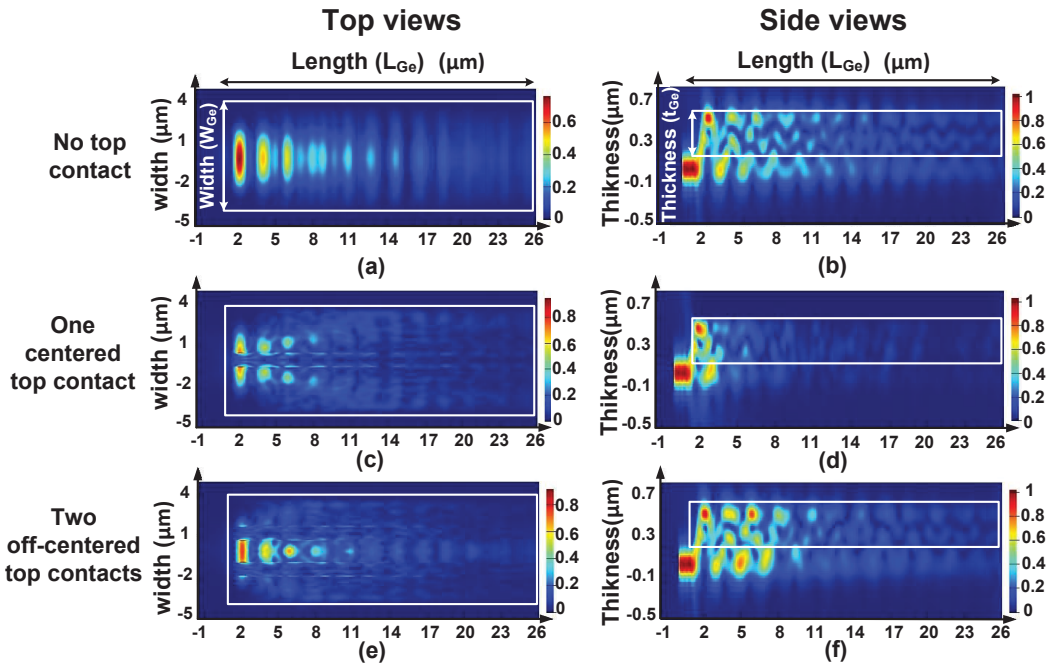


Fig. 4.2 The simulated electric field in a Ge-PD with a length of 25 μm, a width of 8 μm, and a thickness of 500 nm (linear scale). The Ge area is indicated by the white contour box. Left-side figures show the top view near the top interface of Ge (a) without top contact; (c) with one centered contact; (e) with two off-centered contacts. Right-side figures show the side view at the middle width of the Ge area for a PD (b) without top contact; (d) with one centered contact; (f) with two off-centered contacts.

degradation is only around 1%.

4.1.2 Impact of PD Dimension

To study the impact of a PD's dimensions, responsivity, dark current, and bandwidth are simulated for various widths and lengths of the Ge area. Figures 4.3(a) and 4.3(b) show the responsivity for various widths and lengths of the Ge area, respectively. In these simulations, the width of the n-doped Ge is half of the Ge width (W_{Ge}), and its length is the same as the length of the Ge area. The metal loss is ignored to reduce the simulation time. The simulations confirm that the responsivity depends more on the length of the PD than the width.

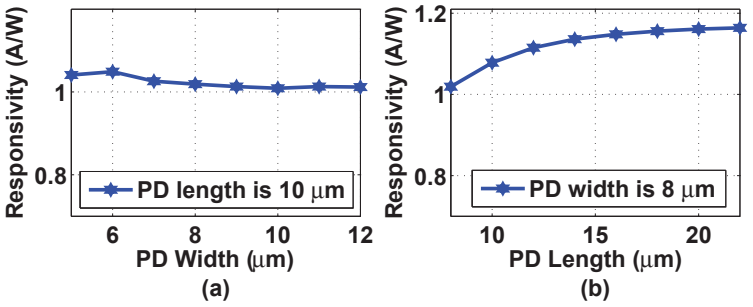


Fig. 4.3 Responsivity variation of the PD with various sizes of the Ge area. (a) For a PD with a constant length of 10 μm and various widths. (b) For a PD with a constant width of 8 μm and various lengths.

Figures 4.4(a) and 4.4(b) show the dark current for various widths and lengths of the doped Ge area, respectively, at 2 V reverse-bias voltage. As it is expected, the dark current increases linearly with Ge area [50]. Figures 4.4(c) and 4.4(d) show the RF bandwidth for various widths and lengths of the Ge area, respectively, at 2 V reverse-bias voltage. TCAD software models the impact of carrier transit time as well as the RC time constants in the bandwidth calculation. Although the junction capacitor of the p-i-n PD decreases with reduced size, the smaller width of the n doped Ge area leads to larger series resistance reducing the bandwidth of the PD. This can be observed in Fig. 4.4(c) for width less than 8 μm where the bandwidth does not improve. For width larger than 8 μm, the increased junction capacitor degrades the bandwidth of the PD. The tradeoffs lead to an optimum bandwidth for a width of 8 μm. A length increase of the PD increases the junction capacitor reducing the PD's bandwidth. In this type of photodetector, the Ge thickness is 500 nm. Therefore, the Ge intrinsic thickness (t) is smaller than the 500 nm due to the n++ doped Ge profile. Considering the carrier velocity-saturation (ν_s) in Ge of 0.6×10^7 cm/s, the calculated transit time bandwidth from $f_{tr} = 0.38 \times \nu_s/t$ is approximately 60 GHz [48]. Since the simulated bandwidth is area dependent, the photodetector bandwidth is mainly RC-limited.

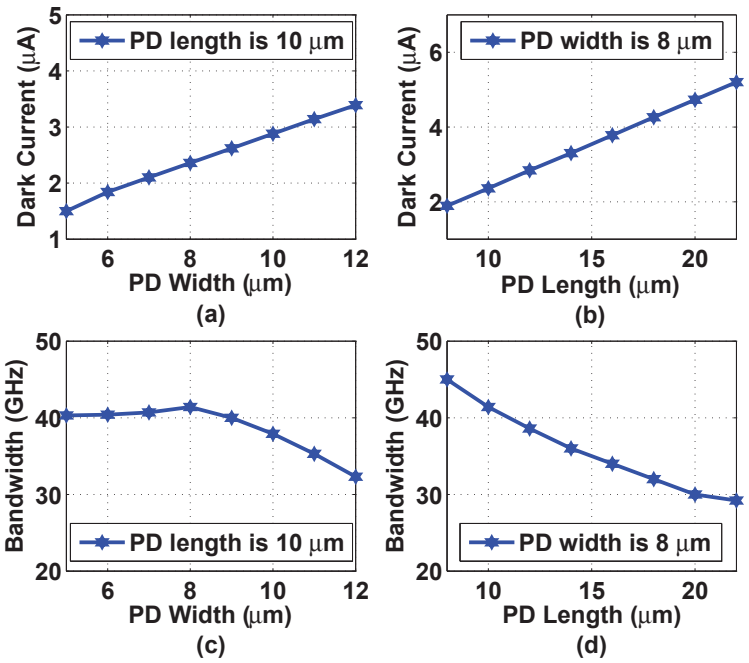


Fig. 4.4 Dark current and bandwidth of the PD for various size of the Ge area. (a) Dark current of a PD with a constant length of 10 μm for various widths. (b) Dark current of a PD with a constant width of 8 μm for various lengths. (c) Bandwidth of a PD with a constant length of 10 μm for various widths, and (d) bandwidth of a PD with a constant width of 8 μm for various lengths.

4.2 Optimization Methodology

In this section, the innovative methodology details the optimization process for the PD's responsivity based on the bandwidth requirement of a target application. It also discusses the design of an appropriate peaking inductor based on the small-signal model of a PD. The required bandwidth for a given data rate generally specifies the photodetector dimensions. Therefore in a photodetector with RC-limited bandwidth, the PD will usually be small at the expense of reduced responsivity. In the proposed methodology presented in Fig. 4.5, the photodetector is first designed for high responsivity and then an integrated peaking inductor enhances the bandwidth to reach the required bandwidth. The peaking inductor is designed for minimum settling time to provide maximum eye opening.

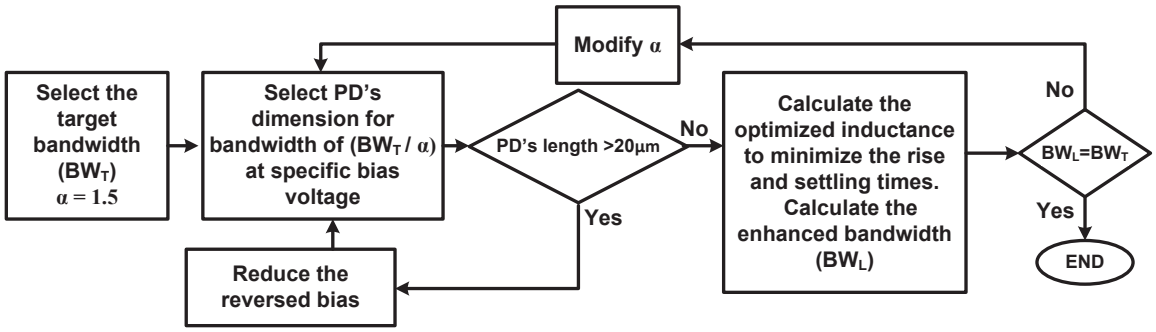


Fig. 4.5 Flowchart of the optimization methodology with target bandwidth BW_T, calculated bandwidth BW_L, and bandwidth peaking factor α.

As an initial step, the peaking inductor is assumed to enhance the bandwidth by α=1.5 times. The accuracy of the enhancement factor value α is based on the electrical model of the PD and the peaking inductor. The reduction in bandwidth (α^{-1}) provides design margin towards larger responsivity. The responsivity can be maximized through appropriate dimensions of the PD, and size and location of the metal contact. For PDs longer than 20 μm, the responsivity improvement becomes negligible while the linear increase in dark current degrades the sensitivity from increased shot noise. In such cases, instead of increasing the length of the PD, the optimization uses the peaking inductor to lower the required reverse-bias voltage thereby reducing the dark current. A photodetector with a Ge area of 8×8 μm^2 is selected as a reference PD with a bandwidth of 45 GHz for a 50 Gb/s application. As α=1.5, the bandwidth of the optimized PD without a peaking inductor is 1.5 times smaller than the reference PD. Consequently, the length of the optimized PD can be increased to 20 μm leading to better responsivity with a reduced bandwidth of 30.1 GHz (67% of 45.2 GHz). A more accurate optimized-length is calculated at a later stage based on the electrical model of the PD and the optimized peaking inductor.

4.2.1 Peaking Inductor Design

The design methodology for the integrated peaking inductor is now detailed. The green box in Fig. 4.6(a) shows the equivalent small-signal circuit of a photodetector. The current source I_{PD} models the photocurrent, and C_{jPD} is the PD junction capacitor. The PD resistance, R_{PD}, is the series combination of the contact resistances and the resistance of the n-doped Ge and the p-doped silicon of the p-i-n photodetector. The red box in Fig. 4.6(a) is the lumped model of a non-ideal integrated inductor [57]. L_{peak} models the peaking inductor in series with the small resistance of the spiral-shaped inductor ($R_{par-ind}$) and in parallel with the parasitic capacitance of the inductor $C_{par-ind}$. R_L in Fig. 4.6(a) is the load resistance seen by the PD such as the input resistance of the transimpedance amplifier (TIA) or the 50 Ω terminated test and measurement equipment. C_L is the combination of the parasitic capacitance of the pads and the parasitic capacitance of the circuit loading the PD. Designing a peaking inductor to minimize the rise and settling times requires determination of the small-signal circuit parameters. Cadence software is used to simulate the frequency and transient responses. The PD resistance (R_{PD}) is estimated based on the sheet resistance of the doped Si and doped Ge, and the contact resistance reported by the foundry. The effective dimension of the doped semiconductor is calculated based on the path that the generated photocurrent follows to reach the anode and cathode pads. The PD's capacitance is estimated from a reported measured capacitor per unit area ($f\mathrm{F}/\mu\mathrm{m}^2$) of a fabricated PD in the similar fabrication process presented in [58]. ANSYS HFSS software calculates the parameters of the inductor and the parasitic capacitor of the pads. Table 4.1 summarizes the simulation parameters. Figure 4.6(b) shows the frequency response of the reference 8×8 $\mu\mathrm{m}^2$ PD (red line), as well as a long 8×20 $\mu\mathrm{m}^2$ PD without peaking inductor (dashed blue line), with an optimized peaking inductor (360 pH, blue line), and with a peaking inductor larger than the optimum value (540 pH, green dashed

line). The optimized peaking inductor enhances the bandwidth by 1.503 times.

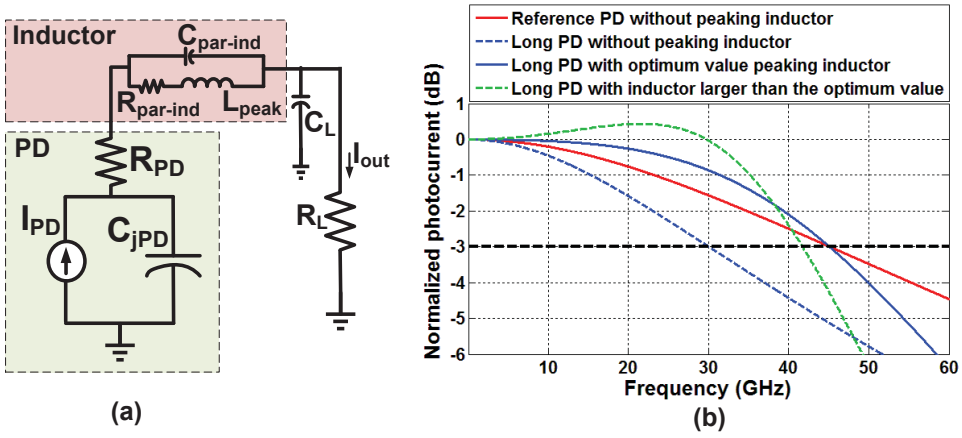


Fig. 4.6 (a) Equivalent small-signal circuit of PD with peaking inductor. (b) The simulated frequency response of an 8×8 μm^2 reference PD and a 8×20 μm^2 PD with and without peaking inductor.

Table 4.1 The parameters for the equivalent small-signal circuit of the reference PD and the longer PD with optimum peaking inductor and the longer PD with peaking inductor larger than optimum.

	R_{PD} Ω	C_{jPD} fF	L_{peak} pH	$C_{par-ind}$ fF	$R_{par-ind}$ Ω	C_{load} fF	R_{load} Ω
Reference PD	215	12.2	—	—	—	15.2	50
Long optimized PD	87	35.2	360/540	2/4	4/5	15.2	50

Figures 4.7(a) and 4.7(b) compare the simulated 50 Gb/s eye diagram of the reference PD (in red) to a long PD with optimum peaking inductor (in blue), and to a long PD with peaking inductor larger than the optimum value (in green), respectively. Interestingly, for a similar bandwidth of 45 GHz, the optimized PD with optimum peaking inductor (in blue) has slightly wider eye opening compared to the reference PD eye due to reduced inter-symbol interference (ISI). Although the optimum peaking inductor for the design is 360 pH, the fabricated inductor is 540 pH following an overestimation of the PD's junction capacitor reported in reference [96]. Using a peaking inductor larger than the optimum

value generates peaking in the frequency response and reduces the optimum bandwidth. It also generates larger overshoot and undershoot in the transient response. However, the eye diagram has an eye-opening similar to that of the reference eye diagram. It worth mentioning that the long PD has a larger responsivity than the reference design. Therefore, with equal optical input, the peak-to-peak of the electrical eye of the long PD (in green) will be bigger than the eye of the reference PD (in red).

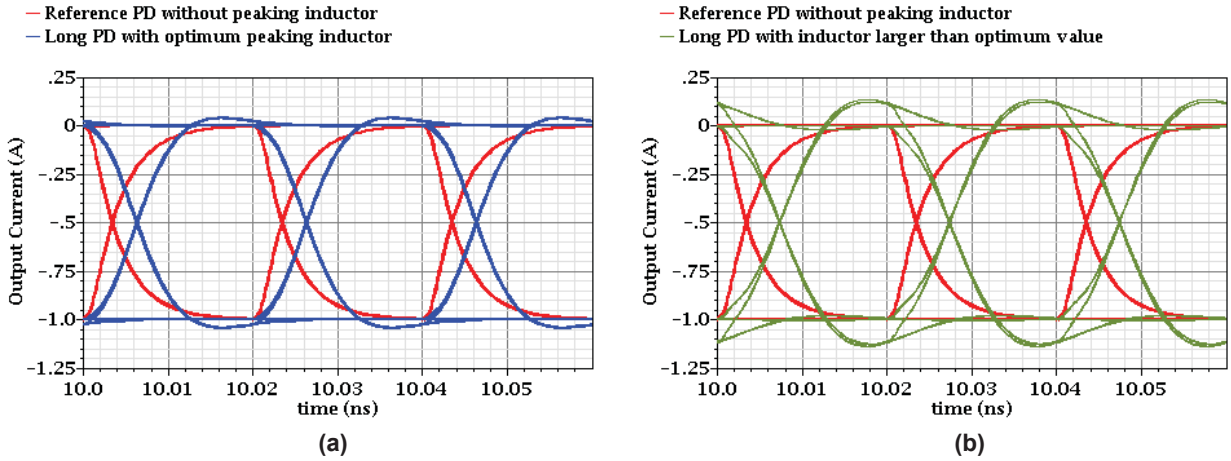


Fig. 4.7 Simulated 50 Gb/s eye diagram of the 8×8 μm^2 reference PD in comparison with the 8×20 μm^2 PD (a) with the optimum peaking inductor (350 pH), and (b) with peaking inductor larger than the optimum value (540 pH).

4.3 Fabrication and Experimental Results

This section presents the fabrication process used for the PDs. The experimental results of the reference PD and the optimized PD are compared to validate the proposed optimization methodology.

4.3.1 Fabrication Process

The photodetectors are fabricated through a process detailed in Fig. 4.8(b). To build a photodetector, a 500 nm thick Ge was deposited through a selective epitaxial growth

[46, 47]. Figure 4.8(a) shows the top view of the optimized PD with an integrated peaking inductor. The process provides two metal layers with a thickness of t_1=0.75 μm and t_2=2 μm separated by 1.5 μm of silicon dioxide (SiO_2) giving the opportunity to design an integrated inductor. The left half of Table 4.2 summarizes the design parameters of the fabricated PDs. PD-A is the reference PD with a centered top contact, and PD-D is the optimized PD with two off-centered top contacts and an integrated peaking inductor. Two additional PDs are designed to separate the effect of using two off-centered contacts from the effect of increased size PD with peaking inductor: 1) PD-B has the same size as the reference PD but with two off-centered contacts, 2) PD-C has the same size as the optimized PD (PD-D) but with a centered contact. Further, it has a peaking inductor to enhance its bandwidth.

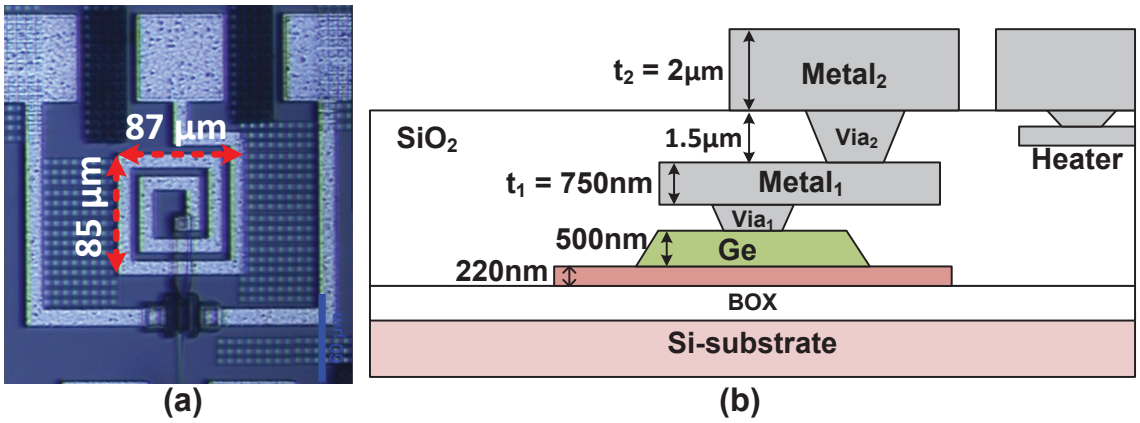


Fig. 4.8 (a) Fabricated photodetector with an integrated peaking spiral inductor; (b) fabrication process layers.

4.3.2 DC and Small-Signal Measurement Results

This subsection presents the measured dark current and responsivity of the PDs along with the small-signal measurement to determine the PD's bandwidth. Using two connected grating couplers (GCs) in proximity to each input GC of the photodetector, the GC loss

is measured to calculate responsivity. The dark current of the PDs for various reverse-bias voltages is first measured with a precise ammeter (Keithley, sensitivity: 0.1 pA). Then, the responsivity is calculated from the measured photocurrent for an injected continuous wave (CW) at 1550 nm. The optical-electrical (OE) bandwidths of PDs are calculated from S-parameter (S_{21}) measured by a 50 GHz lightwave component analyzer (LCA) (Agilent N4373C). The right half of Table 4.2 summarizes the experimental results of the fabricated PDs. Additional experimental results of various modified PDs are shown in section 4.4 which show the performance impact of different design modifications.

Table 4.2 Summary of the photodetector's dimensions and their measurement results.

PD	$W_{Ge}\times L_{Ge}$ (μm^2)	$W_{n-doped}$ $\times L_{n-doped}$ (μm^2)	Contact parameters		Dark current (μA)		Responsivity (A/W)	Bandwidth (GHz)	
			$Num(Gap)$ (μm)	$W_{seg}\times L_{seg}$ (μm^2)	$2V$	$4V$		$2V$	$4V$
A	8×8	4×5.6	1	3.6×5.2	1.05	**10**	0.66	35	**42**
B	8×8	4×5.6	2(1.6)	1×5.2	0.49	**4.9**	0.9	34.6	**41.4**
$C*$	8×20	4×17.6	1	3.6×17.2	**5.5**	54	0.86	**42.6**	45.2
$D*$	8×20	4×17.6	2(1.6)	1×17.2	**3.5**	35.8	1.09	**42.5**	45

Num: *number of contact on top of the germanium.*
******* *photodetector has an integrated peaking inductor.*

Note that for a similar bandwidth of 42 GHz, the reference photodetector (PD-A) requires 4 V reverse-bias voltage while the optimized PD with an integrated peaking inductor (PD-D) needs a lower reverse-biasing voltage of 2 V. The PD-D provides 65% larger responsivity at lower biasing voltage leading to smaller dark current compared to the reference PD (PD-A). Using one of the optimization methods, the responsivity improves by 36% and 30% in PD-B (same size as the reference PD but with two off-centered contacts) and in PD-C (same size as the optimized PD with peaking inductor but with a centered contact), respectively. Figure 4.9(a) shows the OE frequency response (S_{21}) of

the reference PD (PD-A) at 4 V reverse-bias voltage and the optimized PD (PD-D) at 2 V reverse-bias voltage, with their respective small-signal model simulation for parameters reported in Table 4.1. The measured S_{21} curves are normalized to the S_{21} value at 10 MHz. Figure 4.9(b) shows the corresponding reflection frequency response (S_{22}). Although the simulation results for S_{22} are in good agreement with the measurement results, the simulation results for S_{21} show differences. The measured S_{21} of the reference PD exhibits small peaking (<0.21 dB) below 1 GHz. The frequency response linearly decreases afterward (zoomed-in view in Fig. 4.9(a)). While the small-signal model (Fig. 4.6(a)) does not model this low-frequency roll-off behavior, it predicts the high-frequency behavior with the simulated 3-dB bandwidth of 45 GHz which is close to the measured value of 42 GHz for the reference PD. In Fig. 4.9(a) for frequencies larger than 10 GHz, the S_{21} simulated results of the reference PD have the same declining slope compared to the measurement results. On the other hand, by subtracting a DC offset (black arrow in zoomed-in view in Fig. 4.9(a)) from the simulated S_{21}, the effect of the low-frequency roll-off is removed, and the simulation agrees with the measurements for frequencies larger than 10 GHz. The low-frequency roll-off also affects the measured S_{21} of the optimized PD with its peaking inductor (PD-D). However, the simulated S_{21} is in good agreement with the measurement result at high frequencies. Disagreement between simulation and measurements also relates to the inaccurately estimated parameters. The doping of the Ge and Si areas are assumed to be constant with uniform doping depth independent to the PDs' dimensions. In fact, the fabrication process exhibits non-uniform doping density which impacts both parasitic resistance and capacitance. Further, the variation of the Ge thickness changes the parasitic capacitance. Finally, the larger difference for the PD with peaking inductor suggests that the inductor model needs to account for the parasitic capacitance between the integrated spiral inductor and the substrate [97].

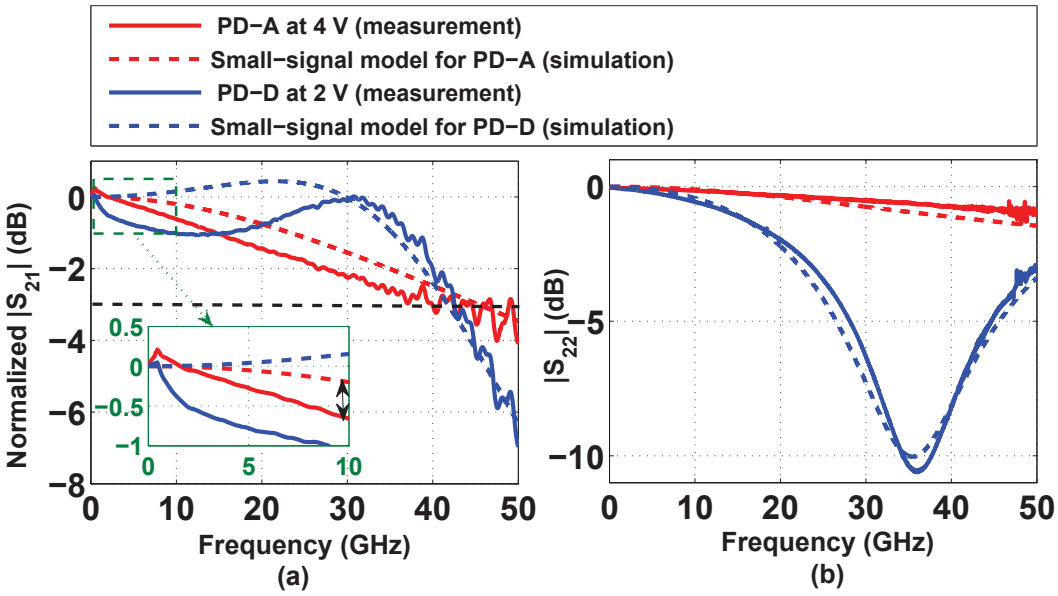


Fig. 4.9 (a) Measured S_{21} OE frequency response of the optimized PD (PD-D) with a reverse-bias voltage of 2 V and reference PD (PD-A) at 4 V reverse-bias voltage with their respective small-signal simulations; (b) measured S_{22} (reflection) of both PDs with their respective small-signal simulations.

4.3.3 Large-Signal Measurement Results

This subsection presents the BER measurements of the fabricated PDs and compares the measured BER and eye diagram of the optimized PD with the reference PD. Figure 4.10 illustrates the test bed for these measurements. The bit pattern generator (BPG) generates PRBS-31 data, and the error analyzer (EA) measures the error rate of the signal detected by the PD. The continuous wave (CW) generated by a DFB laser from EMCORE with 16 dBm optical power at 1550 nm is injected through a polarization controller (PC) with 0.5 dB insertion loss. A 40 Gb/s Mach-Zehnder modulator (MZM) with insertion loss of 8 dB at 1550 nm is driven by the baseband signal from the output of the BPG. The modulated optical carrier is injected into a variable optical attenuator (VOA) with an insertion loss of 2 dB. The VOA is used to reduce the received signal-to-noise ratio (SNR) in the BER measurement. Since the input grating coupler (GC) is polarization sensitive,

the modulated data is then injected to another PC. The optical power at the input GC of the device (point E in Figure 4.10) is 5 dBm. The modulated optical signal is launched to the GC, and the PD converts it to a photocurrent. The 50 Ω terminated measurement devices (EA or Sampling Scope) convert the photocurrent into voltage. The photodetector is biased through a 65 GHz bias tee. Although the bandwidth of the measured PDs is large enough to support 50 Gb/s data, the BER comparison is presented at 30 Gb/s. Beyond that data rate, the test bed exhibits a noise floor. A fair comparison to validate the proposed methodology is required where the difference in performance is not due to the test bed link budget.

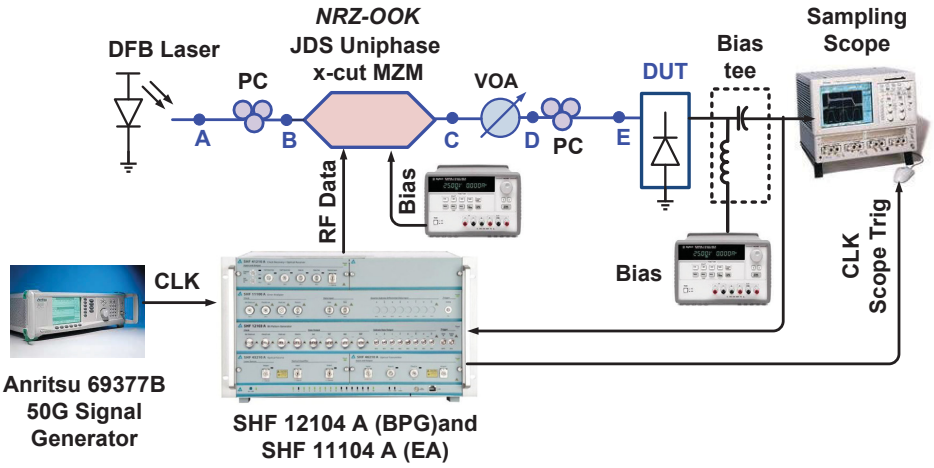


Fig. 4.10 Test bed for the eye diagram and BER measurement.

The measured BER at 30 Gb/s for the reference photodetector (PD-A) is shown in Fig. 4.11 along with BER for the same size PD with two off-centered contacts (PD-B), and 20 μm length PD with a centered contact and peaking inductor (PD-C). Those three PDs are compared to separate the effect of using two off-centered contacts from the effect of increased size PD with peaking inductor. The bias condition for each PD is selected to match the PDs bandwidth (4 V for PD-A (42 GHz bandwidth) and PD-B (41.4 GHz bandwidth), and 2 V for PD-C (42.6 GHz bandwidth)). By extrapolation to a BER of

10^{-12}, the sensitivity of the long PD with a centered contact and peaking inductor (PD-C) is 1.9 dB better than the reference PD while using two off-centered contacts exhibit similar improvement. Figure 4.11 also shows the measured BER for the optimized photodetector (PD-D) for various bias conditions. For matched bandwidth (2 V for optimized PD with a bandwidth of 42.5 GHz), the sensitivity of the optimized photodetector (PD-D) is 3.2 dB better than the reference photodetector (PD-A) at the extrapolated BER of 10^{-12}. Increasing the reverse-bias voltage of the optimized PD to 4 V increases its bandwidth from 42.5 GHz to 45 GHz which in turn improves the sensitivity by 0.6 dB.

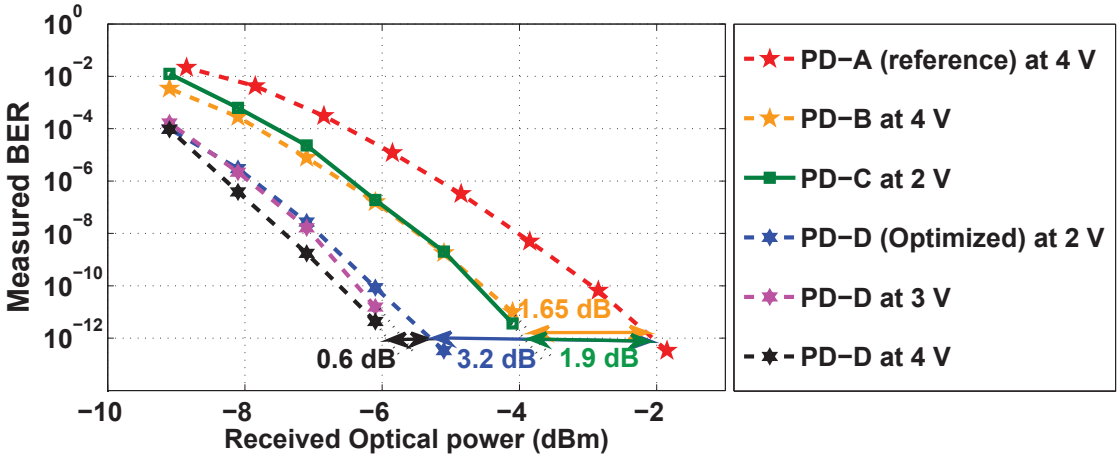


Fig. 4.11 (a) BER performance at 30 Gb/s for the reference PD (PD-A), the same size PD as the reference PD with two off-centered top contacts (PD-B), and 20 μm length PD with a centered top contact and peaking inductor (PD-C); (b) BER performance at 30 Gb/s for optimized PD (PD-D).

Figure 4.12 shows the output electrical eye diagrams of the reference PD (PD-A) with a bandwidth of 42 GHz at 4 V reverse-bias and the optimized PD (PD-D) with a bandwidth of 42.5 GHz at 2 V reverse-bias at various data rates. The optimized PD has larger eye opening amplitudes due to 65% larger responsivity. As expected from simulation results, the eye diagram of the optimized PD has less ISI than the reference PD.

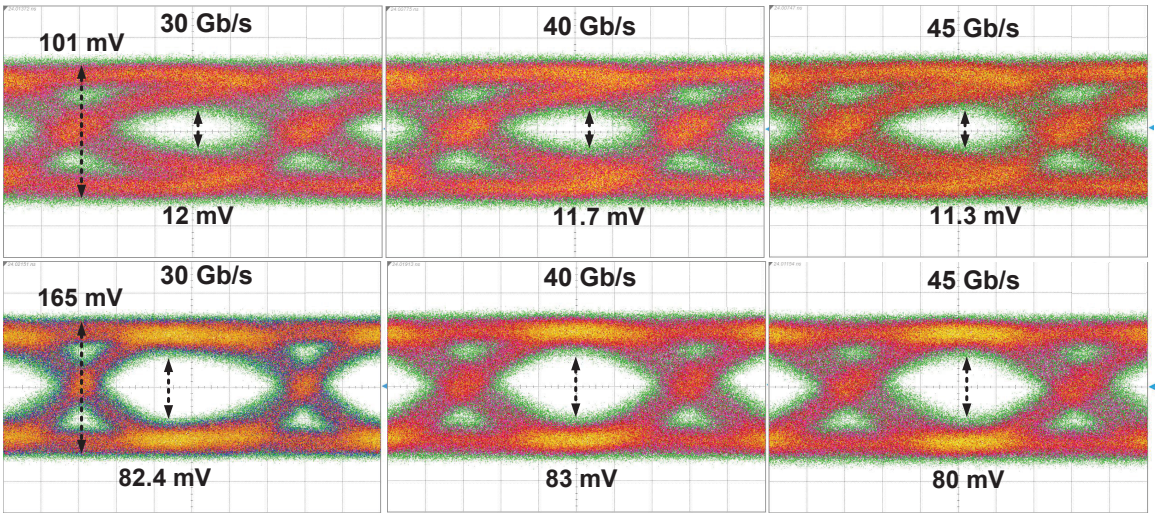


Fig. 4.12 (top) Output electrical eye diagrams of the reference PD (PD-A) at various data rates; (bottom) output electrical eye diagram of optimized PD (PD-D) at corresponding data rates.

4.4 Measurement Results of Other Photodetectors

This section presents the measurement results of several photodetectors with various design parameters to study the performance impact of different design modifications. Table 4.3 summarizes the design properties of the fabricated devices and their measurement results.

Figure 4.13(a) shows the responsivity for various lengths of the photodetector with one centered contact and two off-centered contacts. The measurements are compared to simulation results (Fig. 4.3). The responsivity of PDs with one centered electrode is consistently lower than 0.9 A/W due to the metal absorption of the contact on top of the Ge area (green line). Using two off-centered top contacts with 1.6 μm distance between them, the responsivity improves by $\sim$0.24 A/W (red line) for the same length of PD. The simulated responsivity without the effect of metal loss (blue line) is larger because the distance between the two contacts in two off-centered top contacts is 1.6 μm, and a small effect of the metal loss remains. For the PD with a length of 8 μm, increasing the gap distance to 2 μm in device no. 3 and 2.7 μm in a device no. 4 lead to a responsivity increase

Table 4.3 Summary of device dimensions of fabricated PDs and their measurement results.

No.	$W_{Ge}\times L_{Ge}$ (μm^2)	$W_{n-doped}$ $\times L_{n-doped}$ (μm^2)	Contact parameters		Dark current at 2V (μA)	Responsivity (A/W)	Bandwidth at 2V (GHz)	
			$Num(Gap)$ (μm)	$W_{seg}\times L_{seg}$ (μm^2)				With L
1	8×8	4×5.6	1	3.6×5.2	1.05	0.66	35	—
2	8×8	4×5.6	2(1.6)	1×5.2	0.49	0.9	34.6	> 50
3	8×8	5.4×5.6	2(2)	1.5×5.2	1.26	0.93	27.9	50
4	8.5×8	6.1×5.6	2(2.7)	1.5×5.2	2.08	0.98	34.7	46.9
5	8×10	5.4×7.6	2(2)	1.5×7.2	1.32	0.94	27.8	44.9
6	8×15	4×12.6	1	3.6×12.2	4.35	0.77	34.4	49.5
7	8×15	4×12.6	2(1.6)	1×12.2	2.36	1.03	32	—
8	8×20	4×17.6	1	3.6×17.2	5.5	0.86	32.2	42.6
9	8×20	4×17.6	2(1.6)	1×17.2	3.5	1.09	21.8	42.5
10	8×25	4×22.6	1	3.6×22.2	9.3	0.88	—	39.3

Num: *number of contact on top of the germanium.*
With L: *measured bandwidth of the photodetector with integrated peaking inductor (L).*

to 0.93 and 0.98 A/W, respectively, due to lower metal loss. Those results are in line with the simulation results of 1.01 A/W. Figure 4.13(b) shows the dark for various lengths of the photodetector with one centered contact and two off-centered contacts. The measurements are compared to simulation results (Fig. 4.4). The linear increase of the measured dark current (green line) with the length of the photodetector shows the dominance of the bulk current. The reasons for the differences between simulated dark current and measurement results are the following: 1) due to a limitation in the simulation, the Ge-Si, and Ge-metal interface models are not included in this simulation, 2) the electrical properties of the thin film Ge model are not accurate, and 3) the exact doping density levels of n-doped Ge remains unknown.

The OE frequency response (S_{21}) of various fabricated PDs is shown in Fig. 4.14. Each curve is normalized to its S_{21} value at 10 MHz frequency. The measured S_{21} of all

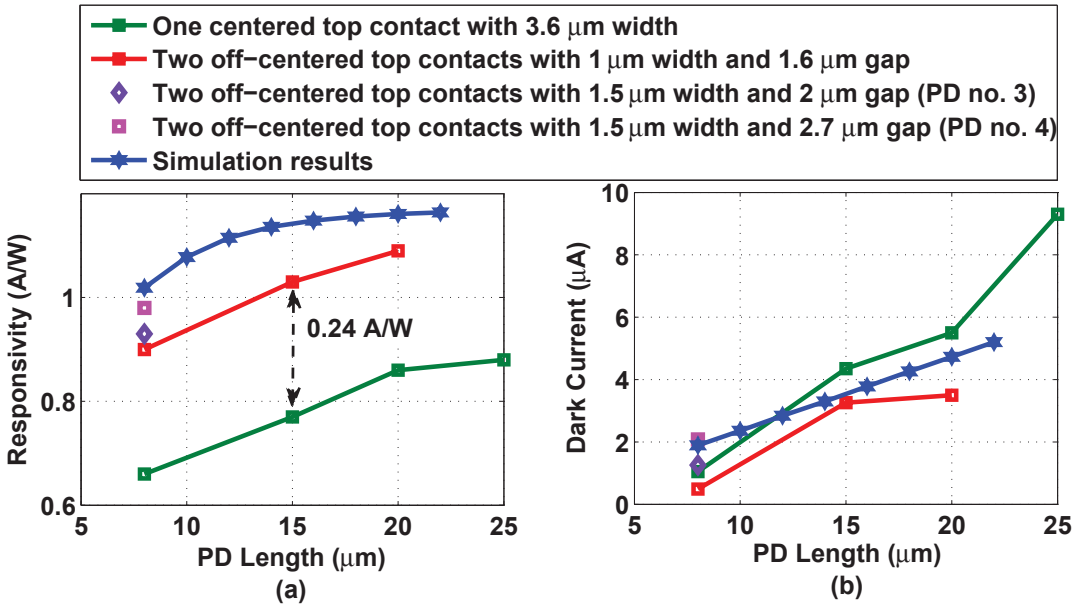


Fig. 4.13 (a) Measured and simulated responsivity; (b) measured and simulated dark current for various PD lengths with one centered top contact and with two off-centered top contacts. Results are compared to simulation results from Figs. 4.3 and 4.4.

PDs shows the low-frequency roll-off. All photodetectors with a peaking inductor have a bandwidth larger than 39 GHz at 2 V reverse-bias voltage. The largest bandwidth reached for photodetectors without a peaking inductor is 35 GHz (no. 1).

The BER performance of various other fabricated devices is shown in Fig. 4.15. All devices with larger responsivity compared to the reference PD (no. 1) have better sensitivity. For instance, PD no. 6 with a longer Ge (15 μm) has slightly lower bandwidth than the reference PD (no. 1) but exhibits an improved sensitivity by 0.7 dB at an extrapolated BER of 10^{-12}. Interestingly for PD no. 7 (Ge length of 15 μm with two top off-centered contacts) with lower bandwidth, the sensitivity improves by 2.8 dB at BER of 10^{-12} from the 56% increase in responsivity from the two off-centered contacts optimization and a longer Ge area.

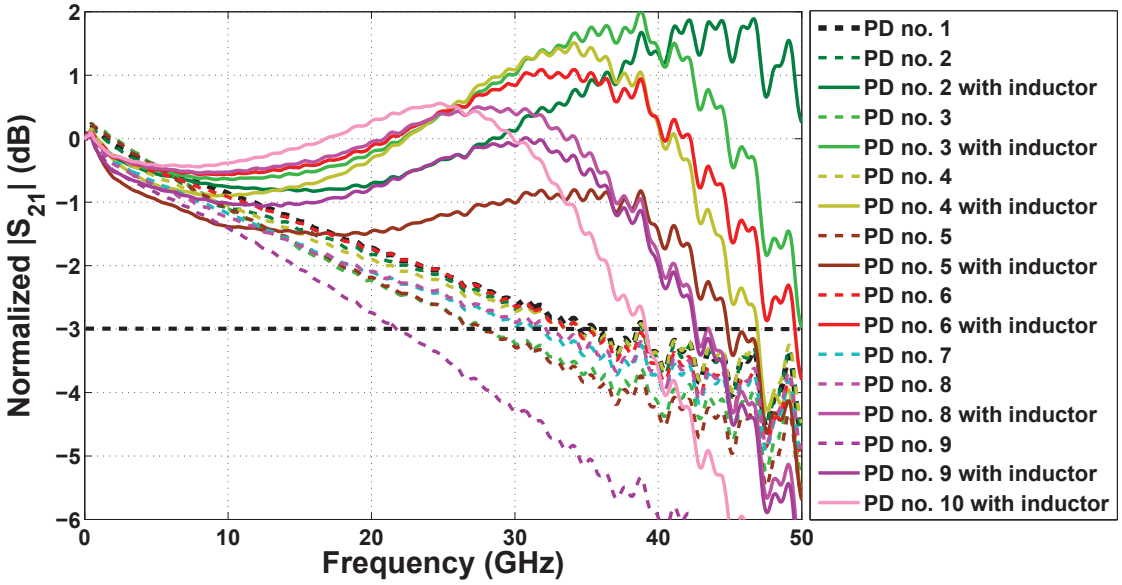


Fig. 4.14 Normalized OE frequency response (S_{21}) response of various PDs at 2 V.

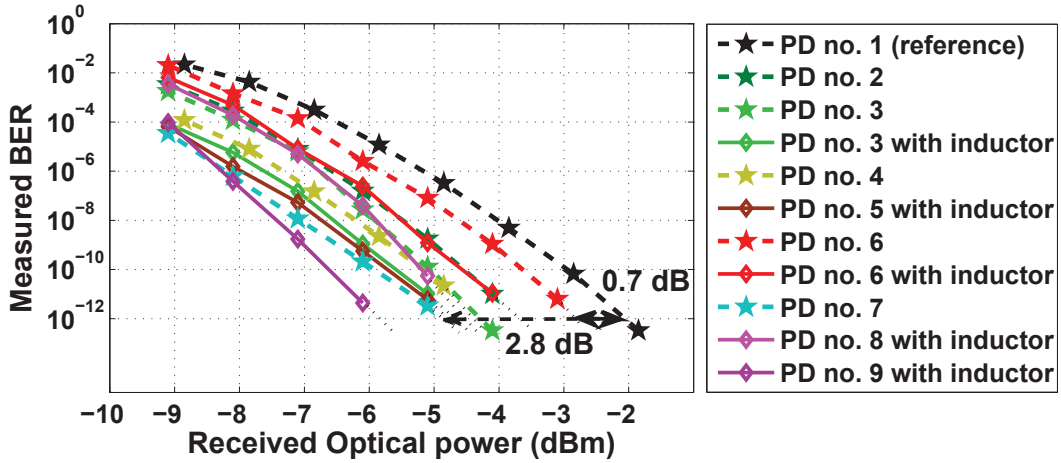


Fig. 4.15 Measured BER at 30 Gb/s of various devices at 4 V reverse-bias voltage.

4.5 Summary

This chapter presented an investigation into the impact of various design parameters of a germanium-on-silicon photodetector along with an optimization of the metal contact on the PD's performance. Using this investigation, it proposed a methodology to maximize

the responsivity of a PD based on the bandwidth requirement of a given application. In the proposed optimization process, increasing the PD's design geometry and using two off-centered small size contacts on top of the germanium enhances the responsivity of the PD. An integrated peaking inductor was designed to mitigate the bandwidth reduction trade-off of the responsivity optimization. To validate the optimization process, a reference design from a silicon photonic foundry process design kit (PDK) was selected. The small size photodetector with an 8×8 μm^2 germanium area was used as a reference. The optimized PD design with an integrated peaking inductor has an 8×20 μm^2 germanium area and two off-centered electrodes on top of the germanium. The optimized design provides a responsivity of 1.09 A/W at 1550 nm, a dark current of 3.5 μA and a bandwidth of 42.5 GHz at 2 V reverse-bias voltage. To the best of our knowledge, in this fabrication process, this is the largest responsivity reported for a Ge-PD with a bandwidth larger than 40 GHz. The reference PD has a similar bandwidth of 42 GHz at 4 V reverse-bias voltage with a responsivity of 0.66 A/W and an increased dark current of 10 μA at this bias voltage. The sensitivity of the optimized PD exhibits a 3.2 dB improvement compared to the small size PD for a bit error rate (BER) of 10^{-12} at 30 Gb/s data rate.

Chapter 5

Grating-Assisted All-Silicon Photodetectors

This chapter demonstrates the design, fabrication, and experimental results of four novel grating-assisted silicon photodetectors (Si-PD) for 850 nm wavelength applications fabricated in an SOI technology. The proposed Si-PDs use grating couplers to direct the incident light horizontally to the intrinsic area of the p-i-n diode for an efficient absorption. The work presented in this chapter has been presented in IEEE Photonics Conference 2016 (post-deadline paper) [31] and published as a journal paper in Optics Express [32].

5.1 Proposed SOI-Based Si-Photodetectors

5.1.1 Baseline Grating-Assisted Si-PD

An illustration of the proposed grating-assisted Si-PD is shown in Fig. 5.1. It consists of a lateral p-i-n structure similar to [68]. However, rather than directing light through the depletion region in the z-direction as in [68], to increase the absorption of light in the depletion region, a grating coupler directs light in the y-direction along the intrinsic region. Since the silicon waveguide is highly absorptive at 850 nm, the grating coupler must be

adjacent to or possibly overlapping the p-i-n diode. Figure 5.1(a) shows the 3-dimensional (3D) structure of the proposed baseline grating-assisted Si-PD (Si-PD no. 1). The top view and side view of the PD are shown in Fig. 5.1(b) and 5.1(c), respectively.

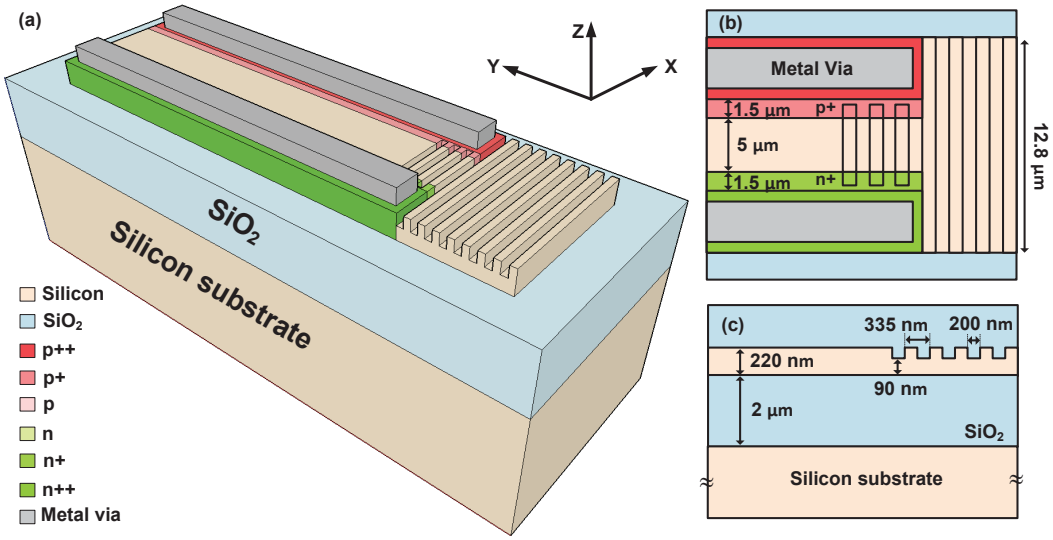


Fig. 5.1 Schematic of the baseline design of the SOI-based grating-assisted Si-PD (Si-PD no. 1) (a) 3D view; (b) top view; (c) side view.

The grating coupler is designed for 850 nm wavelength based on the analytic calculation of the Bragg condition [48]. It is further optimized through 2D and 3D FDTD simulations using commercially available technology computer-aided design (TCAD) tools from Lumerical [94]. The dimensions of the grating coupler are shown in Fig. 5.1(c). Figure 5.2(b) shows the side view of the electric field coupled to the silicon waveguide when the grating coupler is illuminated at 850 nm wavelength at an angle of 24 degrees from normal as shown in Fig. 5.2(a). In this simulation, the silicon is considered lossless for calculating the grating coupler efficiency. The software simulates the forward transmission, back transmission, top reflection, and pass through transmission as shown in Fig. 5.2(c). As the simulated forward transmission shows, the grating coupler larger than the fiber mode field diameter ($\sim$5 μm for a single-mode 850 nm fiber) has a coupling efficiency of 62% at 850 nm wavelength. The maximum responsivity (R) at 850 nm would therefore be 0.425 A/W [48]. Using a grating

coupler smaller than the fiber mode diameter degrades the coupling efficiency. Further, due to the silicon loss at this wavelength, part of the light will be absorbed before reaching the p-i-n region, reducing the responsivity. Considering an absorption coefficient of 1000 cm^{-1} at 850 nm for thin-film silicon [98], a 220 nm silicon layer without a grating coupler absorbs only 2% of vertically illuminated light leading to a maximum responsivity of 0.013 A/W.

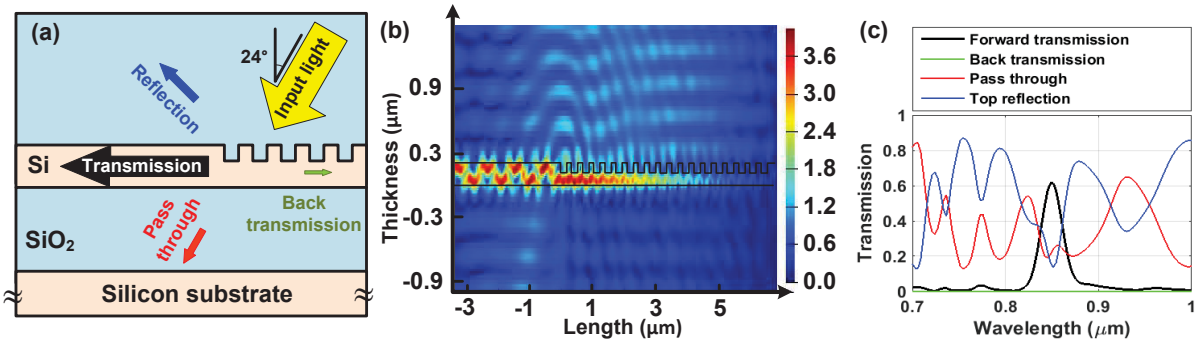


Fig. 5.2 (a) Direction of the incoming and coupled light; (b) side view of the electric field coupled to the silicon waveguide for 24 degrees angled light at a wavelength of 850 nm; (b) simulated transmission for the forward transmission, back transmission, pass-through, and top reflection.

The width of the intrinsic region and the size, location, and doping density of the p-doped and n-doped area determine the speed of the SOI grating-assisted Si-PD. Three doping levels are available for the p-doped and n-doped silicon in the fabrication process in which the proposed Si-PDs are fabricated. Doping densities were found using Sentaurus device simulation software for the specific doping dose and doping energy for each doping layer. The average doping densities for the p++, p+, p, n++, n+ and n layers were found to be 1.2×10^{20} cm^{-3}, 1.8×10^{18} cm^{-3}, 4×10^{17} cm^{-3}, 3.3×10^{20} cm^{-3}, 3×10^{18} cm^{-3}, and 3.2×10^{17} cm^{-3}, respectively. In the Si-PD no. 1 shown in Fig. 5.1, the doping levels of p++, p+, n+ and n++ were used. The length of the p-i-n diode is 60 μm, and the intrinsic width is 5 μm to maximize the responsivity. The parasitic capacitance (C_{PD}) and resistance

(R_{PD}) of the Si-PD are estimated to be 0.27 fF and 39 Ω, respectively. Considering the carrier velocity saturation in silicon to be 10^7 cm/s, the time constant related to the carrier transit time for the intrinsic width of 5 μm would be approximately 50 ps while the RC time constant is approximately 0.01 ps. Therefore, the speed of the photodetector is mainly limited by the carrier transit time.

5.1.2 Design Variations for High-Speed Applications

This subsection describes three design variants of the proposed grating-assisted Si-PD in an SOI technology. Shrinking the width of the intrinsic region in the p-i-n diode reduces the carrier transit time. As a result, the speed of the PD improves as long as the bandwidth is limited only by the carrier transit time. Two approaches are considered to shrink the intrinsic region. In the first approach, the grating coupler from the baseline Si-PD is overlapped with a p-i-n diode with its intrinsic width smaller than the incident mode diameter of the input fiber. Therefore, part of the coupled light would be absorbed outside the intrinsic region which may generate diffusion current and degrade the speed of the Si-PD. Further, in this approach, a grating coupler area smaller than the incident mode size is used which degrades the photodetector responsivity due to reduced coupling efficiency. In the second approach, the fiber mode is transferred into a small waveguide mode through a gradually tapered waveguide. The straight GC used in the Si-PD no. 1 requires a tapered waveguide longer than 100 μm to transfer the mode with low reflection [48]. Consequently, the coupled mode would be absorbed before reaching the p-i-n diode intrinsic region. To reduce the length of the tapered waveguide, a focusing grating coupler (FGC) is designed for 850 nm wavelength.

Figure 5.3(a) shows the top view of Si-PD no. 2 that uses the first approach of shrinking the intrinsic width. It has a similar design as Si-PD no. 1 shown in Fig. 5.1 but with an intrinsic width of 2 μm and p+ and n+ doping widths of 0.5 μm. In comparison with

Si-PD no. 1, the 2.5 times smaller intrinsic width in Si-PD no. 2 leads to a larger parasitic capacitance of 0.69 fF for the p-i-n diode length of 60 μm. However, the carrier transit time is 2.5 times smaller than Si-PD no. 1. The parasitic resistance is estimated to be 32 Ω. The proposed grating-assisted Si-PD no. 3 also uses the first approach for reducing the intrinsic width to 1 μm as shown in Fig. 5.3(b). Three small PDs are combined to improve the responsivity and only the p++ and n++ doping layers are used. The parasitic capacitance and resistance of this Si-PD are estimated to be 4.1 fF and 9.5 Ω, respectively, for the p-i-n diode length of 60 μm. Figure 5.3(c) shows the grating-assisted Si-PD no. 4 with an 850 nm focusing GC. The focusing GC couples the incident light into a 500 nm wide rib waveguide with 0.3 μm intrinsic width. The narrow intrinsic width reduces the carrier transit time enabling high-speed performance. Further, the narrow width enables an avalanche behavior at a reverse-bias voltage lower than 20 V. The p+ and n+ doping width is 0.9 μm and the length of the p-i-n diode is 30 μm. The responsivity of this photodetector at low reverse-bias voltage is lower than the other three proposed Si-PDs since only 17% of the coupled light reaches to the p-i-n diode. However, due to the avalanche behavior, the responsivity improves considerably at high reverse-bias voltage. The parasitic capacitance and resistance of this Si-PD are estimated to be 2.3 fF and 57 Ω, respectively. It is expected that this photodetector provides the largest bandwidth compared to the other three Si-PDs since the carrier transit time is approximately 3 ps. In addition to the four proposed Si-PDs, two extra Si-PDs similar to the grating-assisted Si-PDs no. 1 and no. 3 but without grating coupler are fabricated to study the coupling efficiency of the grating couplers.

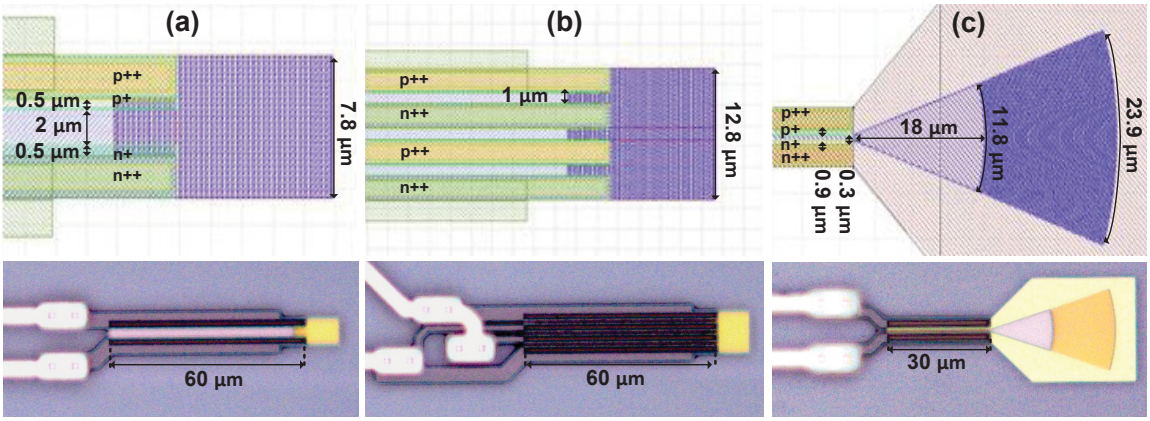


Fig. 5.3 Three designs of SOI-based grating-assisted Si-PD with lower responsivity, but larger bandwidth (top figures are the layout and bottom figures are the micrographs of fabricated devices); (a) grating coupler overlapped with a p-i-n diode with an intrinsic width smaller than the incident mode size (Si-PD no. 2); (b) grating coupler with three-finger PD (Si-PD no. 3); and (c) focusing grating coupler (Si-PD no. 4).

5.2 Experimental Results

This section presents the measurement results of the SOI-based grating-assisted Si-PDs and compares them with previously published Si-PDs. The dark current of the grating-assisted Si-PDs for various reverse-bias voltages is first measured with a precise ammeter (Keithley, sensitivity: 0.1 pA). Then, the responsivity is calculated from the measured photocurrent for an injected continuous wave (CW) at 848.2 nm wavelength generated by a VCSEL source from Thorlabs. Figure 5.4(a) is the measured dark current, and the photocurrent for 0 dBm illuminated CW light for various reverse-bias voltages. The responsivity of the grating-assisted Si-PDs with respect to reverse-bias voltage is shown in Fig. 5.4(b). Figure 5.4(c) plots the variation in photocurrent with respect to the received optical power at 8 V reverse-bias voltage.

The Si-PD no. 1 (baseline Si-PD) has the largest responsivity of 0.24 A/W at 0 V reverse-bias voltage compared to the other three designs. A Si-PD with the same structure as the grating-assisted Si-PD no. 1, but without the grating coupler has a responsivity

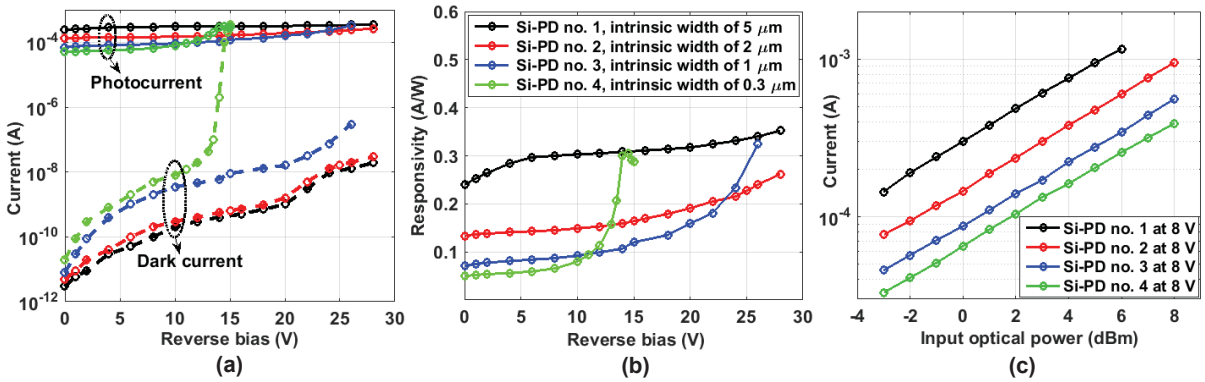


Fig. 5.4 DC measurement results of the Si-PDs; (a) dark current and photocurrent for 0 dBm illuminated CW light; (b) responsivity of the Si-PDs; (c) measured photocurrent of the Si-PDs for various received optical power at 8 V reverse-bias voltage.

of 0.006 A/W at 0 V reverse-bias voltage. As such, the grating coupler improves the responsivity by 40 times. By increasing the reverse-bias voltage of Si-PD no. 1, the responsivity increases to 0.3 A/W for voltages larger than 6 V. The responsivity remains almost flat up to 18 V and gradually increases for larger voltages. The measured dark current is lower than 1 nA for a reverse-bias voltage lower than 20 V. At high reverse-bias voltages, the responsivity increases due to impact ionization. Si-PD no. 2 with a smaller intrinsic width (2 μm) has a responsivity of 0.133 at 0 V reverse-bias voltage. The responsivity increases to 0.19 A/W at 20 V with a dark current lower than 2 nA at this bias voltage. Si-PD no. 3 with a 1 μm intrinsic width and three diode fingers has a responsivity of 0.071 A/W at 0 V reverse-bias voltage. A Si-PD with the same structure as Si-PD no. 3 but without the grating coupler has a responsivity of 0.0043 A/W at 0 V. Here, the grating coupler increases the responsivity by more than 16.5 times. Overlapping the p-i-n diodes with a small intrinsic width reduces the light coupling improvement by 59% in comparison to Si-PD no.1 due to the discontinuity of the grating in the overlapped area and the interference of the metal via on the light coupling. The responsivity of Si-PD no. 3 increases to 0.324 A/W at 26 V reverse-bias voltage with a dark current lower

than 0.3 μA. Increasing the reverse-bias voltage improves the responsivity by more than 4.5 times. Si-PD no. 4 with a focusing GC and 0.3 μm intrinsic width has the lowest responsivity of 0.05 A/W at 0 V reverse-bias voltage compared to the other three designs. However, the responsivity rapidly increases for a reverse-bias voltage larger than 10 V. Si-PD no. 4 has a responsivity of 0.3 A/W and dark current of 2 μA at 14 V reverse-bias voltage. By increasing the reverse-bias voltage to larger than 14.4 V, the photocurrent saturates and the responsivity degrades due to the space-charge effect that reduces the electric field in the center of the intrinsic area [71].

Next, the optical-electrical (OE) bandwidths of the grating-assisted Si-PDs are calculated from the S-parameters (S_{21}) measured by a 50 GHz microwave network analyzer (Agilent PNA-X N5245A). The test bed for the S-parameter measurements is illustrated in Fig. 5.5(a). The CW light generated by a VCSEL source from Thorlabs at 848.2 nm is injected through a polarization controller (PC) into a 40 GHz Mach-Zehnder modulator (MZM). The microwave network analyzer drives the MZM to modulate the CW light. Since the input grating coupler is polarization sensitive, the modulated data is then injected to another PC. The grating-assisted Si-PD detects the modulated data, converting it to a photocurrent, which is then injected into the second port of the microwave network analyzer through a 65 GHz bias tee that also provides the bias voltage for the photodetector. By increasing the reverse-bias voltage, the bandwidth of the Si-PDs increases and then saturates at high voltages. The reverse-bias voltage of each Si-PD is selected to be in the range where the bandwidth improvement is negligible. Figure 5.5(b) plots the measured S_{21} of the designed grating-assisted Si-PDs. To compare the 3-dB bandwidth of the Si-PDs, each curve is normalized to its S_{21} value at 100 MHz frequency.

The Si-PD no. 1 shows the lowest bandwidth of 4.7 GHz at 20 V reverse-bias voltage in comparison with the other proposed Si-PDs. Although Si-PD no. 3 has a smaller intrinsic width than Si-PD no. 2, it has lower OE bandwidth due to a larger diffusion current.

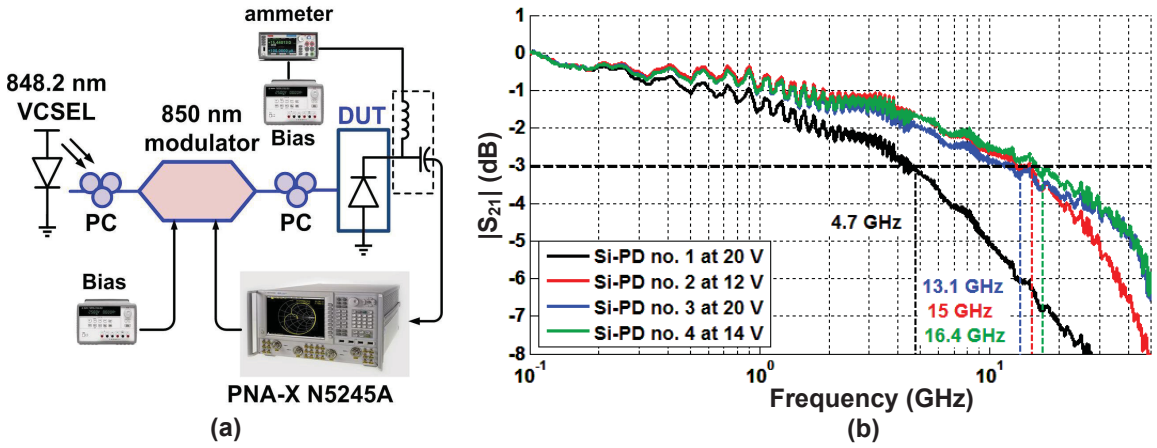


Fig. 5.5 (a) S-parameter measurement setup; (b) measured S_{21} OE frequency response of the grating-assisted Si-PDs.

The focusing grating-assisted Si-PD no. 4 has the largest bandwidth (16.4 GHz at 14 V reverse-bias voltage).

Following the DC and frequency response measurements, the eye diagrams are captured. Further, the bit error rate (BER) of two of the proposed Si-PDs is measured. Then, the performance of the proposed grating-assisted Si-PDs is compared with the performance of published high-speed Si-PDs. The test bed for the eye diagram and BER measurements is illustrated in Fig. 5.6. The bit pattern generator (BPG) generates PRBS-31 data, and the error analyzer (EA) measures the error rate of the signal detected by the PD. The CW generated by the VCSEL source with 11.8 dBm optical power at 848.2 nm is injected through a PC with 0.5 dB insertion loss. A 40 GHz MZM with insertion loss of 6.5 dB at 850 nm is driven by the baseband signal from the output of the BPG. The modulated data is then injected to another PC. The optical power at the input GC of the device is 3.5 dBm. The modulated optical signal is launched to the Si-PD and converted to a photocurrent. The 50 Ω termination of test equipment converts the photocurrent into a voltage. The photodetector is biased through a 65 GHz bias tee while its current is simultaneously measured with the precise ammeter. Since the amplitude of the detected signal is smaller

than the sensitivity of the EA, a 12 GHz low noise amplifier amplifies the detected signal for BER measurement. To change the signal-to-noise ratio (SNR) for BER measurement, the position of the input fiber is shifted. Shifting the fiber from the optimum position reduces the received optical power and as a result, it degrades the SNR. The corresponding average optical power is calculated based on the monitored photocurrent.

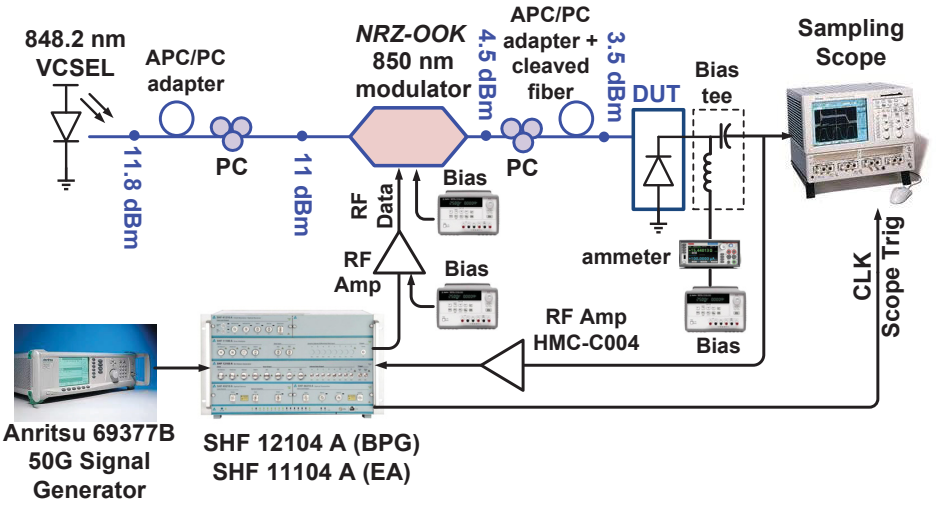


Fig. 5.6 Test bed for the eye diagram and BER measurement.

The measured eye diagram for Si-PD no. 1 with an intrinsic width of 5 μm at 20 V reverse-bias voltage for 8 Gb/s and 10 Gb/s PRBS-31 NRZ-OOK are shown in Fig. 5.7. Figure 5.8 plots the measured eye diagram for Si-PD no. 2 with an intrinsic width of 2 μm at 12 V reverse-bias voltage for 25 Gb/s, 30 Gb/s and 35 Gb/s PRBS-31 NRZ-OOK data. The eye diagrams for multi-finger Si-PD no. 3 with an intrinsic width of 1 μm at 20 V reverse-bias voltage for 25 Gb/s, 30 Gb/s and 35 Gb/s PRBS-31 NRZ-OOK data are shown in Fig. 5.9. Figure 5.10 illustrates the eye diagrams for Si-PD no. 4 with focusing grating coupler and an intrinsic width of 0.3 μm and at 14 V reverse-bias voltage for 25 Gb/s, 30 Gb/s and 35 Gb/s PRBS-31 NRZ-OOK data.

As it is expected from the frequency response measurement, Si-PD no. 1 can support a bit rate of 10 Gb/s. The other three Si-PDs show open eye diagrams at 35 Gb/s. The

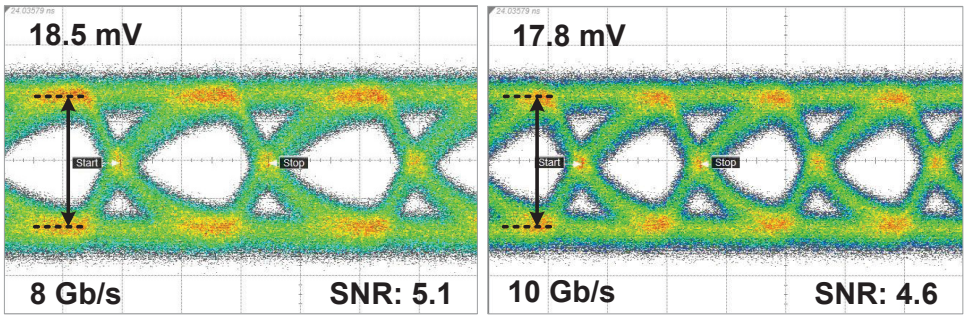


Fig. 5.7 Electrical eye diagrams of Si-PD no. 1 with 5 μm intrinsic width at reverse-bias voltage of 20 V.

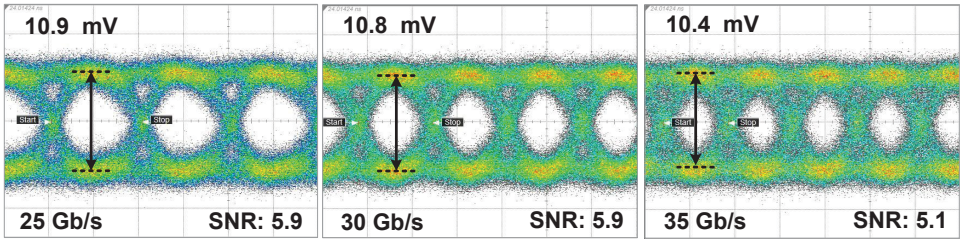


Fig. 5.8 Electrical eye diagrams of Si-PD no. 2 with 2 μm intrinsic width at reverse-bias voltage of 12 V.

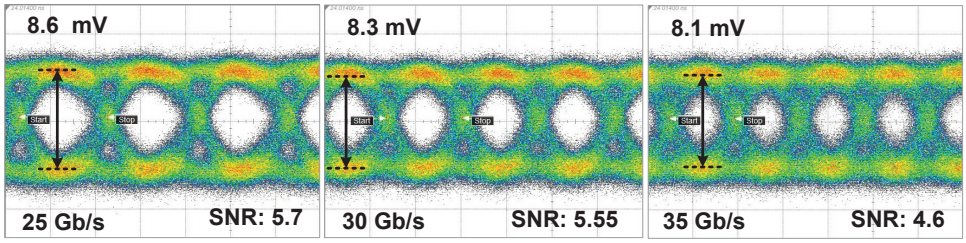


Fig. 5.9 Electrical eye diagrams of the Si-PD no. 3 with 1 μm intrinsic width and three-finger p-i-n diodes at 20 V reverse-bias voltage.

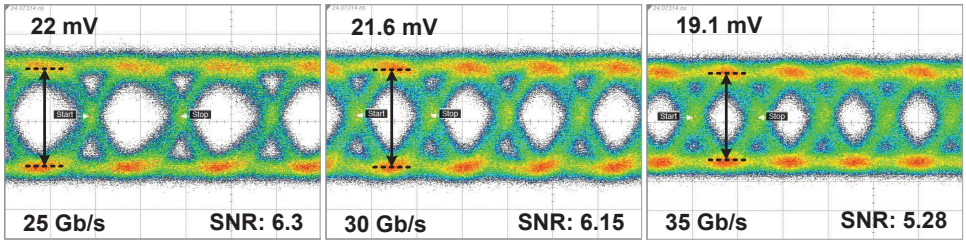


Fig. 5.10 Electrical eye diagrams of the Si-PD no. 4 with focusing grating coupler and an intrinsic width of 0.3 μm at 14 V reverse-bias voltage.

measured SNR of the eye diagram of Si-PD no. 4 is better than Si-PDs no. 2 and no. 3 due to the larger responsivity and larger 3-dB bandwidth.

The bit error rate (BER) for Si-PD no. 2 and Si-PD no. 3 are measured at 10 Gb/s. The instability of the measurement setup for testing the Si-PD no. 1 and Si-PD no. 4 prevented us from measuring the BER of these two Si-PDs. The off-the-shelf 12 GHz amplifier for BER measurement degrades the SNR of the amplified signal due to the 3 dB noise figure of the amplifier. Further, due to the limited power budget and noise floor of the optical link, the BER measurement is limited to 10 Gb/s PRBS-31 OOK-NRZ data (Fig. 5.11). The Si-PD no. 2 has a slightly better sensitivity (0.4 dB) for BER at 10^{-12} in comparison with Si-PD no. 3. The improvement is 1.3 dB at BER of 10^{-9}.

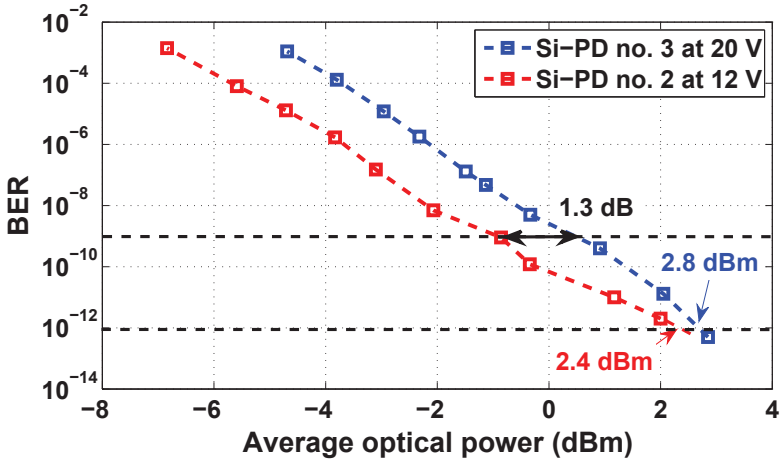


Fig. 5.11 BER measurement results for Si-PD no. 2 and no. 3 for 10 Gb/s PRBS-31 OOK-NRZ data.

Table 1 summarizes the performance of the proposed SOI-based grating-assisted Si-PDs and compares them with previously published high-speed Si-PDs. For comparison, a figure of merit (FoM) is defined as FoM=R (mA/W)×BW (GHz), using two important photodetector parameters, responsivity (R) and bandwidth (BW). Based on the FoM values, the proposed grating-assisted Si-PDs provide excellent performance. The optimized design (Si-PD no. 4) has the FoM value of 4920 GHz×mA/W by at least 35% larger than other

published Si-PDs. The grating coupler enables the fabrication of Si-PDs with reasonable responsivity and larger bandwidth without relying on equalization techniques. Further, the small parasitic capacitor of the proposed Si-PDs makes the design of a downstream transimpedance amplifier stage less challenging for high-speed applications.

Table 5.1 Summary of the proposed grating-assisted Si-PDs performance and comparison with fabricated Si-PDs.

	Technology	Type of PD		R (A/W)	Dark current	C_{PD} (fF)	BW (GHz)	Bias (V)	FoM GHz×mA/W
3'PTL [68]	0.13 μm SOI t=2 μm	Lateral p–i–n		0.08	∼1 nA	210	8	20	640
13'TED [65]	0.13 μm CMOS	APD p+/NW		0.48	—	35	7.6	10.25	3648
15'PTL [67]	0.25 μm CMOS	APD p+/NW		0.2	∼1 nA	—	5.6	12.2	1120
15'JAP [69]	0.18 μm SOI t=0.21 μm	Lateral p–i–n		0.0075	∼0.01 nA	∼65	13.6	10	102
16'PTL [66]	0.13 μm CMOS	SML-APD p+/NW		0.03	<0.1 nA	5 [a]	12	9.7	360
This work	0.12 μm SOI t=0.22 μm	Lateral p–i–n	1	0.32	1 nA	0.27 [b]	4.7	20	1504
			2	0.153	0.4 nA	0.69 [b]	15	12	2295
			3	0.155	16 nA	4.1 [b]	13.1	20	2030
			4	0.3	2 μA	2.3 [b]	16.4	14	4920

BW: 3-dB bandwidth; **t:** silicon thickness; **SML-APD:** spatially modulated light avalanche photodetector.
[a]: Capacitor is extracted from the equivalent small-signal model of the APD.
[b]: Capacitor is estimated based on the dimensions of the p-i-n diode in the Si-PD.

5.3 Summary

This chapter demonstrated the design, fabrication, and measurement results of four novel silicon photodetectors (Si-PD) for 850 nm applications fabricated in silicon-on-insulator (SOI) technology. The proposed photodetectors use grating couplers to couple the injected light to the silicon waveguide for an efficient absorption. The grating coupler in

the baseline design increases the responsivity by 40 times compared with the PD without a grating coupler. We experimentally showed the trade-off between speed and responsivity for various designs of the Si-PD. The proposed designs provide promising performance in terms of responsivity and bandwidth. The optimized design of the grating-assisted Si-PD has a responsivity of 0.3 A/W, an avalanche gain of 6, a dark current of 2 μA, and a 3-dB bandwidth of 16.4 GHz at 14 V reverse-bias voltage that leads to a FoM of 4920 GHz×mA/W for this photodetector. Further, it shows an open eye diagram for 35 Gb/s PRBS-31 NRZ-OOK data at this bias voltage.

Chapter 6

Compact and Power-Efficient Optical Receiver

Using a mature and reliable complementary metal-oxide-semiconductor (CMOS) technology provides a cost-effective solution for optical transceivers. However, the design of a power-efficient optical receiver with a high gain-bandwidth product is more challenging in CMOS technology compared with SiGe, GaAs, and InP technologies, due to the lower transition frequency (f_T) of CMOS.

As discussed in Chapter 2, third-order interleaved active feedback is a compact bandwidth extension technique and it has been implemented using cascaded first-order differential or single-ended common source (CS) amplifiers [85]. In this work, for the first time, the interleaved active feedback enhances the bandwidth of a cascade of second-order Cherry–Hooper (CH) post-amplifiers. In this structure, local positive feedback is also employed to increase the bandwidth of the transimpedance amplifier (TIA). This chapter demonstrates the design and experimental results of the proposed optical receiver front end fabricated in TSMC 65nm technology. Further, optical measurements are obtained by wire bonding the optimized design of the novel Si-PD (Section 5.1.2) to the proposed

optical receiver. The work presented in this chapter has been submitted to IEEE Journal of Solid State Circuits (JSSC) [33].

6.1 Optical Receiver Front End Design

In this section, the bandwidth enhancement of the cascaded second-order inverter-based CH amplifier with third-order interleaved active feedback is discussed. Also, the design of the proposed optical receiver and the trade-off among bandwidth, power dissipation, group delay variation, and noise is presented.

An inverter-based CH amplifier is a low-power design with a reasonable gain-bandwidth product, especially in low-voltage technologies [99]. It consists of two inverters with resistive feedback (R_f) around the second inverter. Based on our simulation results, for the same gain and power dissipation, an inverter-based CH amplifier can provide a larger bandwidth than two cascaded common-source (CS) amplifiers.

6.1.1 Bandwidth Enhancement of CH-Amplifier Chain with Active Feedback

Two forms of third-order active feedback (AFB) are considered in a chain of CH amplifiers. Figure 6.1(a) shows the cascade of two CH amplifiers when the active feedback connects to the input of the first section of the second CH (G_3). Figure 6.1(b) shows the feedback signal added to the input of the second section of the CH (G_4).

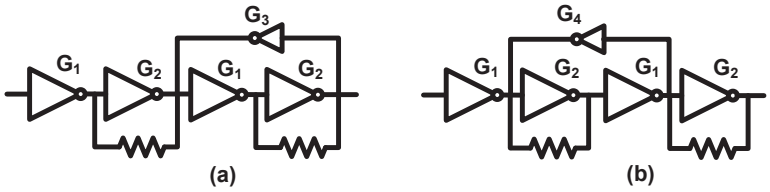


Fig. 6.1 Block diagram of two cascaded CH amplifiers with active feedback; (a) the feedback signal is added to the input of the first section of a CH; (b) the feedback signal is added to the input of the second section of a CH.

First, the transfer function of two cascaded CH amplifiers with active feedbacks G_3 and G_4 are calculated. For simplicity, it was assumed that the sizes of G_3 and G_4 are small and their loading on G_1 and G_2 are negligible. In practice, the size of the feedback inverter is lower than 0.1 times that of the CH's inverters. Also, all stages have the same capacitive load C_L (mainly caused by the gate-source capacitor of the following stage). The transfer function of each stage is calculated by

$$G_1(s) = \frac{-g_{m1}}{Y_{L1}}, Y_{L1}(s) = g_{ds1} + sC_L + \frac{g_{m2} + g_{ds2} + sC_L}{1 + g_{ds2}R_f + sC_LR_f} \tag{6.1}$$

$$G_2(s) = \frac{1 - g_{m2}R_f}{1 + g_{ds2}R_f + sC_LR_f} \tag{6.2}$$

$$G_3(s) = \frac{-g_{m3}}{Y_{L2}}, Y_{L2}(s) = g_{ds2} + sC_L + \frac{g_{m2} + g_{ds1} + sC_L}{1 + g_{ds1}R_f + sC_LR_f} \tag{6.3}$$

$$G_4(s) = \frac{-g_{m4}}{Y_{L1}} \tag{6.4}$$

where R_f is the feedback resistor, g_{mi} is the sum of the transconductances of the PMOS and the NMOS transistors in the inverter, and g_{dsi} is the sum of the output conductance of PMOS and NMOS transistors in the inverter. Note that $G_2(s)$ is the voltage-to-voltage gain of the stage consisting of the inverter G_2 and the feedback resistor. Assuming $g_m \gg g_{ds}$ and $1 \gg g_{ds2}R_f$, the transfer functions are simplified as follows

$$G_1(s) = \frac{-g_{m1}(1 + sC_LR_f)}{g_{m2} + 2sC_L + s^2C_L^2R_f}, A_1 = \frac{g_{m1}}{g_{m2}} \tag{6.5}$$

$$G_2(s) = \frac{1 - g_{m2}R_f}{1 + sC_LR_f}, A_2 = g_{m2}R_f - 1 \tag{6.6}$$

$$G_3(s) = \frac{-g_{m3}(1+sC_LR_f)}{g_{m2}+2sC_L+s^2C_L^2R_f}, \beta_a = \frac{g_{m3}}{g_{m2}} \tag{6.7}$$

$$G_4(s) = \frac{-g_{m4}(1+sC_LR_f)}{g_{m2}+2sC_L+s^2C_L^2R_f}, \beta_b = \frac{g_{m4}}{g_{m2}} \tag{6.8}$$

The transfer function of a CH amplifier is calculated by

$$H_{CH}(s) = G_1(s)G_2(s) = \frac{A_1A_2}{1+2s/\omega_g+s^2/(\omega_g\omega_r)} = \frac{A_{CH}}{D(s)} \tag{6.9}$$

where $\omega_r = 1/(C_LR_f)$ and $\omega_g = g_{m2}/C_L$. Assuming that $g_{m2}R_f \gg 1$, the CH amplifier has a pair of complex conjugate pole of $\omega_{p1,p2} = \omega_r(-1+j\sqrt{A_2})$. The transfer function of the two cascaded CH amplifiers with active feedback G_3 or G_4 is given by

$$H_{AFB}(s) = \frac{G_1^2G_2^2}{1-G_1G_2G_k}, k = 3, 4 \tag{6.10}$$

By substituting the G_i, i=1, 2, 3, and 4:

$$H_{AFB-a}(s) = \frac{A_{CH}^2}{D^2(s)+A_{CH}\beta_a(1+s/\omega_r)} \tag{6.11}$$

$$H_{AFB-b}(s) = \frac{A_{CH}^2}{D^2(s)+A_{CH}\beta_b(1+s/\omega_r)} \tag{6.12}$$

where H_{AFB-a} is the transfer function of the circuit in Fig. 6.1(a) and H_{AFB-b} is the transfer function of the circuit in Fig. 6.1(b). Using the same size feedback inverters G_3 and G_4 results in equal feedback gain ($\beta_a = \beta_b = \beta$). Therefore, $G_3 = G_4 = G_f$ and as a result, the transfer functions H_{AFB-a} and H_{AFB-b} are equal. The effect of the active feedback on the CH structure is presented through numerical simulations. The gain of the CH stage is set to 2.3, ω_r=80 rad/ns and ω_g=150 rad/ns. Figure 6.2 shows the variation

of the gain, gain peaking, and normalized bandwidth of two cascaded CH amplifiers with respect to various feedback gain (β). The normalized bandwidth is calculated by dividing the bandwidth of the amplifier with active feedback to the bandwidth of the amplifier without active feedback. Increasing the feedback gain reduces the gain of the amplifier and increases its bandwidth, and generates gain peaking for a feedback gain larger than 0.3. Figure 6.3 shows the pole locations for two cascade CH amplifiers for variation of the feedback gain β from 0 to 1. The arrows in the figure show the trend as the feedback gain increases. Without feedback, the system has two repeated pairs of complex conjugate poles (blue crosses in Fig. 6.3). The active feedback pushes one pole to high frequency, leaving one real pole and a pair of complex conjugate poles to shape the frequency response. Increasing the feedback gain moves the two dominant poles to lower damping factor which generates peaking in the magnitude frequency response. In the next section, the active feedbacks are combined to improve the bandwidth of a multistage CH amplifier.

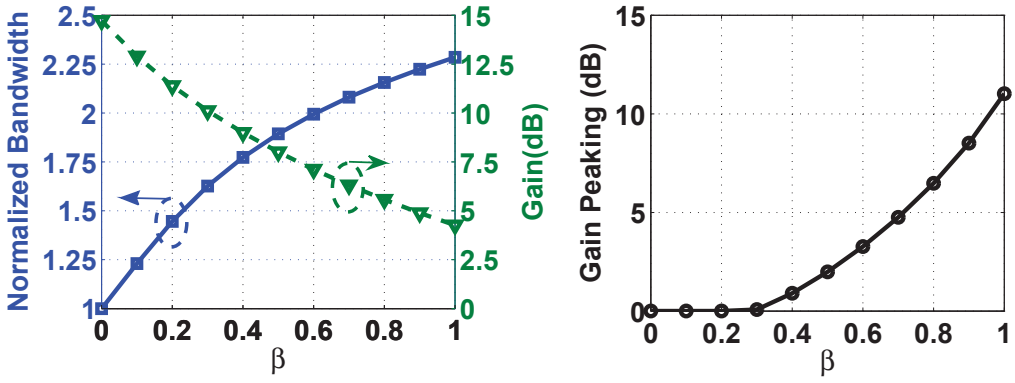


Fig. 6.2 Variation of the bandwidth and gain of two cascaded CH amplifiers for various feedback gain (β); (b) the associated gain peaking.

Figure 6.4(a) shows the block diagram of three cascaded CH amplifiers with interleaved active feedback (IAFB). The transfer function of the circuit is obtained by

$$H_{IAFB}(s) = \frac{G_1^3 G_2^3}{1 - 5G_1G_2G_f + 3G_1^2G_2^2G_f^2} = \frac{G_1^2G_2^2}{1 - 4.303G_1G_2G_f} \cdot \frac{G_1G_2}{1 - 0.607G_1G_2G_f} \qquad (6.13)$$

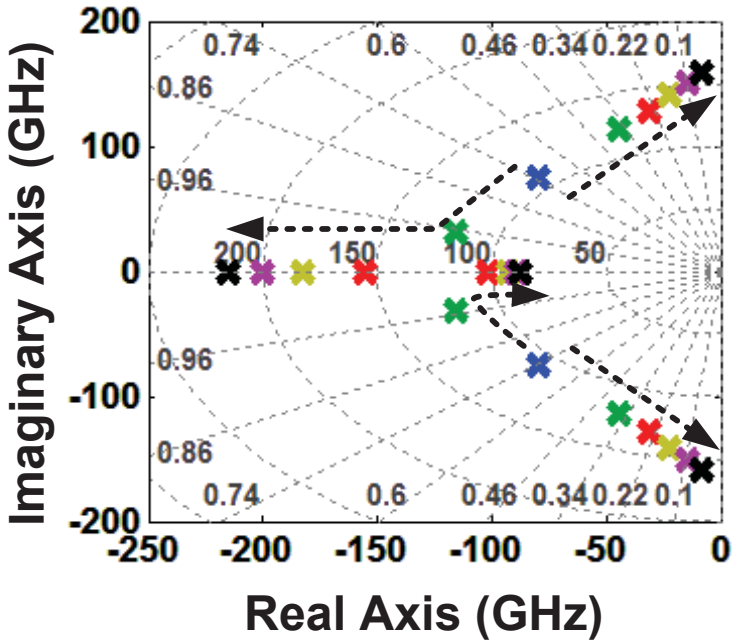


Fig. 6.3 The poles plot of two cascaded CH amplifiers for different gains of active feedback.

By substituting the expressions for G_1, G_2, and G_f in (6.13), the transfer function of the three cascaded CH amplifiers with interleaved active feedback is calculated by

$$H_{IAFB}(s) = \frac{A_{CH}^2}{D^2(s) + 4.303A_{CH}\beta(1 + s/\omega_r)} \cdot \frac{A_{CH}D(s)}{D^2(s) + 0.607A_{CH}\beta(1 + s/\omega_r)} \tag{6.14}$$

The first term in (6.14) has the same denominator as the transfer functions in (6.11) and (6.12) but with a feedback gain of $P_a \times \beta$, where P_a=4.303. Also, the second term has the same denominator as the two cascaded CH amplifiers with a feedback gain of $P_b \times \beta$ (P_b=0.607). Therefore, the three cascaded CH amplifiers with interleaved active feedback (IAFB) with the feedback gain of β have the same transfer function as the three cascaded CH amplifiers with two non-uniform active feedbacks. This observation is similar to that of [85]. Figure 6.4(b) shows the block diagram of the equivalent circuit with two non-uniform active feedbacks.

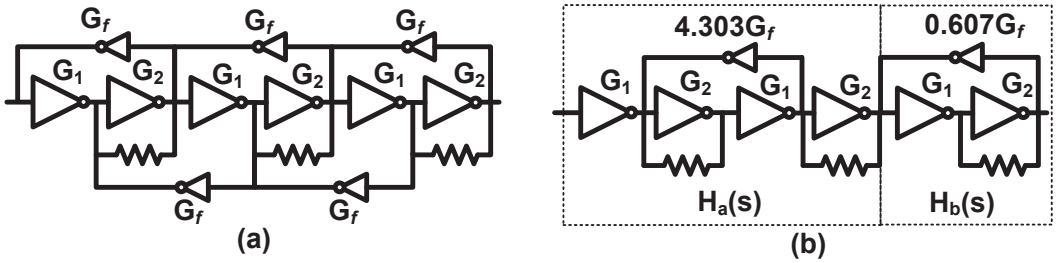


Fig. 6.4 (a) Block diagram of three cascaded CH amplifiers with interleaved active feedback (IAFB). (b) Its equivalent circuit with two non-uniform active feedbacks.

Replacing the two weighted feedbacks in Fig. 6.4(b) with two uniform feedbacks with a gain of β, which means $P_a = P_b = 1$, results in a transfer function with eight complex poles, occurring as two sets of repeated poles (red triangles in Fig. 6.5). By giving the amplifier non-uniform feedback, (i.e., P_a=4.303 and P_b=0.607) poles no longer occur in repeated pairs (shown in blue). The arrows in Fig. 6.5 show the effect of coefficients P_a and P_b on the poles' movement in comparison with two uniform feedbacks. Note that both transfer functions also have a pair of conjugated zeros.

Figure 6.6 compares the frequency response of three cascaded CH amplifies with two non-uniform active feedback and with two uniform active feedback for β=0.08. In comparison with an amplifier with two uniform active feedback, using interleaved active feedback increases the bandwidth by 32% at the cost of 3.7 dB gain reduction.

6.1.2 Proposed Optical Receiver

Figure 6.7 shows the block diagram of the proposed receiver front end. The post-amplifier chain is connected to the output of an inverter-based feedback TIA. A small positive feedback (PFB) is added in the first section of the first CH amplifier to extend the bandwidth of the TIA by creating a negative resistance at the output of the TIA [88]. The required transimpedance gain determines based on the input-referred noise of the optical receiver,

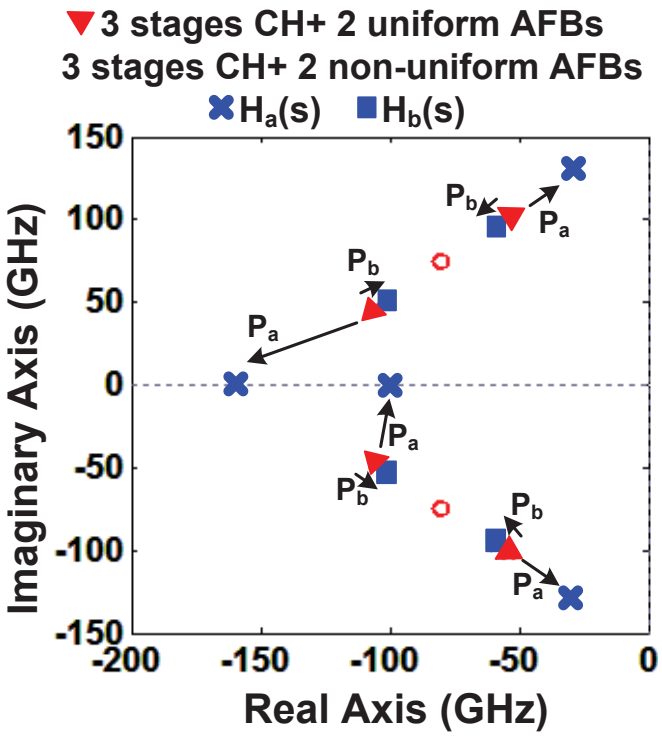


Fig. 6.5 Pole splitting behavior of three cascaded CH amplifier with uniform interleaved active feedback for feedback gain of β=0.08.

and the required peak-to-peak amplitude of the following circuits after the receiver front end such as the integrated decision circuit. The proposed optical receiver is designed for operating at 25-30 Gb/s and with transimpedance gain larger than 70 dBΩ. The DC gain of the proposed receiver front end including the TIA and PFB is given by

$$R_T = \frac{A_{tia}A_1^3A_2^3}{1 + 5\beta A_1A_2 - A_1\alpha + 3A_1^2A_2^2\beta^2 - 3A_1^2A_2\alpha\beta} \tag{6.15}$$

where $A_{tia} = (g_{mt}R_t - 1)/g_{mt}$, which is the gain of an inverter-based feedback TIA with the effective transconductance and the feedback resistor of g_{mt} and R_t, respectively. Also, $\alpha = g_{m-PFB}/g_{mt}$, where g_{m-PFB} is the effective transconductance of the PFB inverter. As it is expected, the active feedback reduces the DC gain and the positive feedback increases the DC gain. Appendix C indicates a discussion about the effect of feedback inverters on the

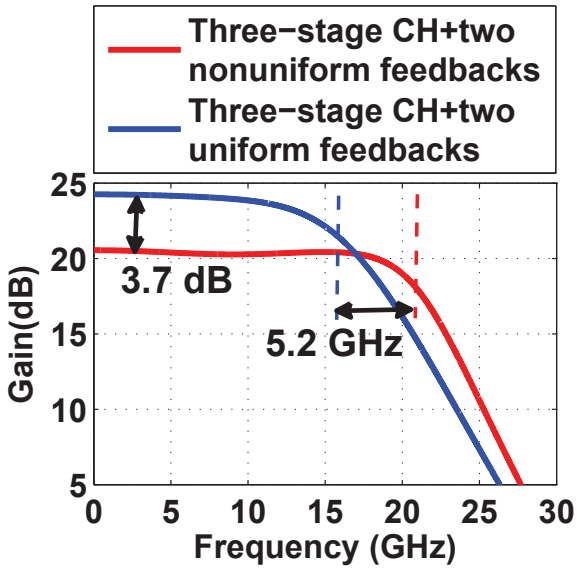


Fig. 6.6 Simulated frequency response for three cascaded CH amplifiers with two non-uniform active feedbacks (or uniform interleaved active feedback) and with two uniform active feedbacks.

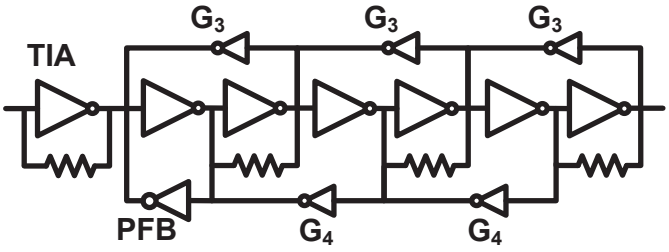


Fig. 6.7 Block diagram of the proposed receiver front end.

low frequency input-referred current noise of the receiver front end. Table 6.1 summarizes the design goals of the proposed optical receiver.

Table 6.1 Design goals of the proposed optical receiver.

Transimpedance gain	>70 dBΩ
Data rate	25–30 Gb/s
3 dB bandwidth	>15 GHz
Power dissipation	≤30 mW (for 1 pJ/bit)

In designing the receiver, the CH inverters are assumed to be the same size as the TIA inverter. In an inverter, selecting an equal size for the PMOS and NMOS transistors maximizes the total transconductance for a given input capacitance, which increases its gain-bandwidth product [100]. Also, the equal bias voltage of the inverters leads to the same current density in the TIA, CH amplifier, and feedback inverters. The width of the transistors in the TIA are swept to find an optimum gain-bandwidth product. Figure 6.8 shows the gain-bandwidth product of an inverter-based feedback TIA with respect to the transistor width. In this simulation, both input and output capacitors are 100 fF, and the feedback resistors (R_F) is 300 Ω. The simulation result shows that the TIA has an optimum gain-bandwidth product of 3310 GHzΩ for transistor width of 25 μm. Also, the size of the IAFB inverters and PFB inverter are swept for maximum bandwidth with a flat response. In simulations, capacitance was added to each transistor to model additional metal coupling capacitance not part of the intrinsic transistor model. The gate-source, gate-drain, and drain-source capacitors of 0.11×W fF/μm, 0.1×W fF/μm, and 0.08×W fF/μm obtained from layout extraction are added where W is the width of the transistor in μm.

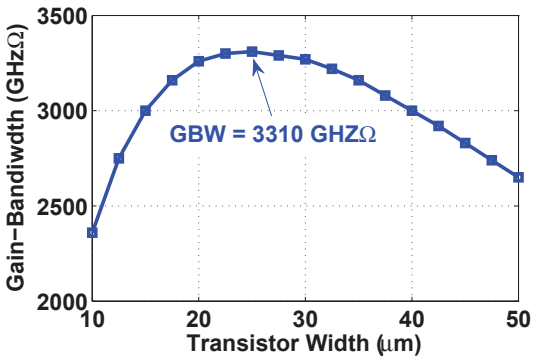


Fig. 6.8 Gain-bandwidth product with respect to the transistor width.

Table 6.2 summarizes the design parameters of the proposed optical receiver in the third column. Also, it presents the design parameters of an optical receiver consisting of an

inverter-based TIA and CH amplifiers without IAFB and PFB to study the performance trade-off in the proposed optical receiver. The load capacitor of the receiver front end is chosen based on the anticipated capacitive load of the following circuits such as the integrated decision circuit and an output buffer. Table 6.3 compares simulation results of the proposed optical receiver to an optical receiver consisting of an inverter-based TIA and CH amplifiers without IAFB and PFB.

Table 6.2 The simulation parameters for a three-stage CH amplifier.

	TIA and three-stage CH (reference)	TIA and three-stage CH with IAFB and PFB
TIA feedback resistor	300 Ω	300 Ω
CH feedback resistor	150 Ω	215.5 Ω
PFB ratio	—	0.16
IAFB ratio	—	0.064
Input Cap. (pads+PD)	100 fF	100 fF
Load Cap. (pads+PD)	100 fF	100 fF

With the same transimpedance gain, the proposed receiver front end has a 35% larger bandwidth, while the power consumption increases only by 6.2%. The proposed design also has a ±1.3 ps larger group delay variation in comparison with the reference design. The group delay variation of the proposed design is ±0.07 ps larger than ±10% of the 30Gb/s bit unit interval (UI), ±0.1×UI=±3.33 ps, which is the typical limit for group delay variation [90]. Figure 6.9 compares the output eye diagram of the reference receiver front end (top) and the proposed receiver front end (bottom) for 30 Gb/s 30 μA_{p-p} random data. The maximum eye opening of the proposed front end is 46 mV larger than the maximum eye opening of the reference design. It has slightly larger pattern-dependent jitter resulting from a slight increase in the group delay variation. Although the proposed receiver has a signal-to-noise ratio (SNR) slightly less than the SNR of the reference design, the larger

Table 6.3 Comparison of the simulation results.

	TIA and three-stage CH (reference)	TIA and three-stage CH with IAFB and PFB
Supply voltage	1.2 V	1.2 V
Bias current	22.7 mA	24.1 mA
Transimpedance gain	76.6 dBΩ	76.6 dBΩ
Bit rate	30 Gb/s	30 Gb/s
3 dB bandwidth	12.34 GHz	16.65 GHz
Total output noise	8.65 mV_{rms}	11.76 mV_{rms}
Group delay variation	±2.1 ps	±3.4 ps
Maximum eye opening for 30 μA_{p-p} input	135 mV_{p-p}	181.8 mV_{p-p}
Power dissipation	27.3 mW	29 mW

peak-to-peak eye of the proposed front end provides a better performance by relaxing the design requirement of the following circuits after the receiver front end such as integrated decision circuits.

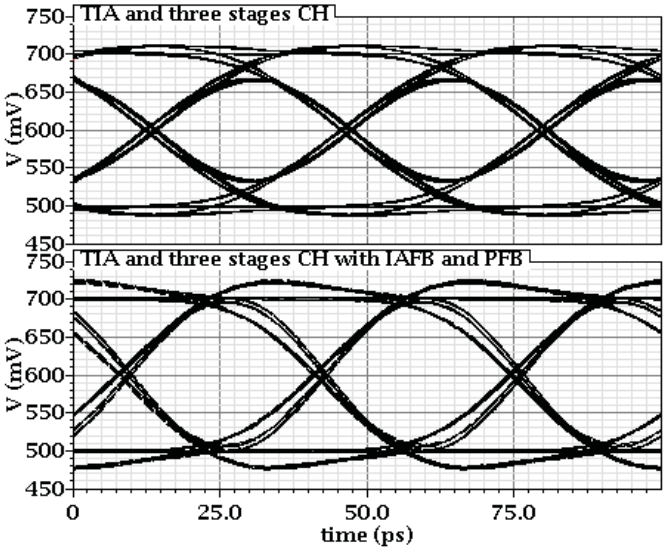


Fig. 6.9 Eye diagrams of the reference receiver front end and the proposed receiver front end for 30 Gb/s random data with 30 μA_{p-p} input.

The performance of the proposed receiver is studied for various fabrication process corners with ±10% supply variation and temperature variation (PVT). Based on the simulation results, the proposed receiver is stable across PVT. Except for the slow-slow (ss) corner that exhibits 0.4 dB peak in the magnitude of the frequency response and ±6.35 ps group delay variation. Else, the proposed circuit shows a flat response with group delay variation lower than ±4.3 ps across PVT. The design parameters of the fabricated optical receiver are modified based on post-layout simulation results for optimum performance for a targeted data rate of 25–30 Gb/s.

The block diagram of the fabricated optical receiver and the design parameters are shown in Fig. 6.10. It consists of an analog front end with a variable gain control (VGC) circuit and an offset cancellation feedback which, based on the simulation result, generates a 2.8 MHz low frequency cutoff. The PMOS and NMOS transistors in inverter-based feedback TIA and three CH amplifiers have a width of 25 μm and a minimum length of 60 nm. The feedback resistors in the TIA and CH amplifier are 300 Ω and 200 Ω, respectively. The PMOS and NMOS transistors in the inverter-based interleaved active feedback (IAFB) are 2.25 μm wide and 60 nm in length. The first stage of the CH amplifier has a fixed inverter-based positive feedback (PFB) with PMOS and NMOS transistors 4 μm wide and a 3 bit variable positive feedback with PMOS and NMOS transistors 0.5, 1, and 2 μm wide. The effective width of the PFB transistors can be adjusted from 4 μm for control bits of 000 to 7.5 μm for control bits of 111. There is also a variable resistor in the TIA and in the two stages of post-amplifier that controls the gain and bandwidth of the front end by applying a voltage through the $V_{Control}$ pin in Fig. 6.10. A 7 μm wide NMOS transistor in parallel with the fixed feedback resistor implements the variable resistor. Based on the simulation result, the minimum resistance of the NMOS variable resistor is approximately 60 Ω for $V_{Control}$ of 1.2 V. Therefore, the $V_{Control}$ of 1.2 V minimizes the gain of the receiver front end and maximizes its bandwidth. There is a PMOS CS amplifier with a resistive

load of 100 Ω to drive the AC-coupled 50 Ω termination of the measurement equipment. To reduce the power consumption only a small single stage output buffer is used. Post-layout simulation results show that the transimpedance gain of the front end before the output buffer is 7.8 dB larger than after the output buffer, and it has a slightly larger bandwidth. Note that by integrating the decision circuits with the optical front end, the output of the front end directly connects to the decision circuits. Therefore, the transimpedance gain is 7.8 dB larger than the measured transimpedance gain at the output buffer.

To compensate the offset voltage, an offset cancellation (OC) feedback is used that employs an active low-pass filter. As discussed in Chapter 2, the low cut-off frequency should be small enough to avoid a large power penalty due to the baseline wander problem for transmitting a long string of identical bits (also called runs). In the active low pass filter the effective time constant is $\tau = R_{oc}C_{oc}(1+g_m r_o)$, where R_{oc} and C_{oc} are the low pass filter resistor and capacitor, respectively (Fig. 6.10), g_m is the total transconductance of the inverter I_1, and r_o is the total resistance at the output of the inverter I_1. Based on the post-layout simulation results, the receiver front end has 2.8 MHz low cut-off frequency. There are on-chip shift-registers that enable/disable switches in the optical receiver for various receiver configurations to provide an optimized performance.

6.2 Receiver Front End Characterization

This section presents a complete characterization of the receiver front end with an electrical input signal. Figure 6.11 shows the micrograph of the optical receiver fabricated in TSMC 65 nm CMOS technology. The total size of the chip is 1.5 mm×0.5 mm, while the receiver occupies only 0.0056 mm^2 (70 μm×80 μm) of the area. The fabricated chip is packaged in a ceramic quad flat package CQFP80 and is partially wire bonded. The cavity size of the package is 7.6 mm×7.6 mm. The input and output pads of the front end (shown with

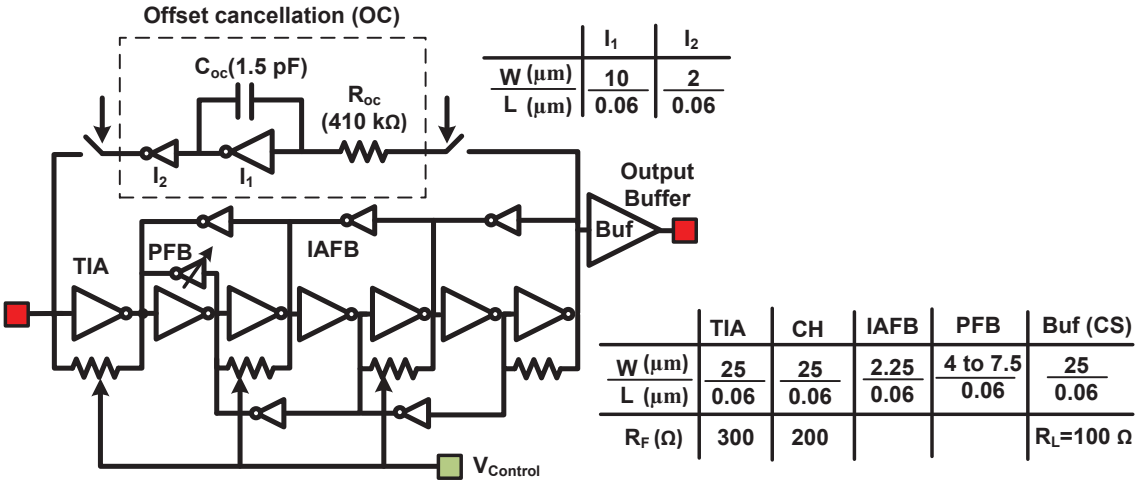


Fig. 6.10 Block diagram of the fabricated optical receiver.

red squares in Fig. 6.10) interface to two 40 GHz ground-signal-ground (GSG) probes in the electrical measurement and later the input pad is wire-bonded to a fabricated SOI-based all-silicon photodetector. Due to the large cavity size of the CQFP80, relatively long wire bonds for the supply voltage affect the receiver performance, which is an issue discussed later in this section. An ATmega328 microcontroller is programmed to generate the required bit stream for loading the on-chip shift registers that control the switches in the optical receiver. The receiver front end without the output buffer (4.4 mW) consumes 26.4 mW at 1.1 V supply voltage. In the following subsections, the experimental results of the frequency response and the transient response of the proposed receiver front end are discussed.

Frequency Response Measurement

The frequency response of the receiver front end is measured using a 50 GHz microwave network analyzer (Agilent PNA-X N5245A). Figure 6.12 compares the measured S-parameters of the receiver with the post-layout simulation results. In this measurement, the offset cancellation feedback is enabled, while the 3 bit positive feedback is set to 000, and the vari-

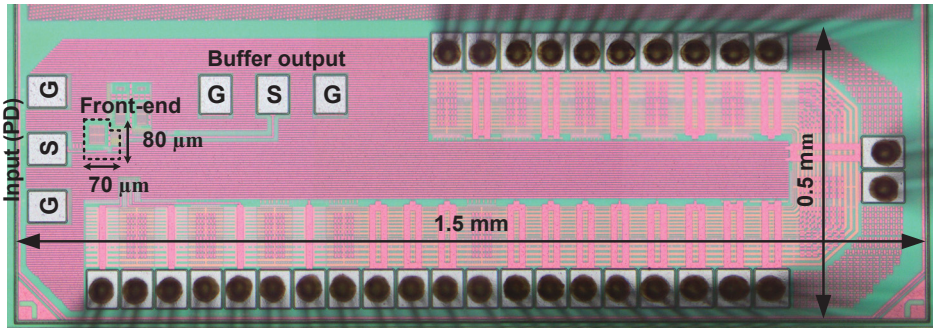


Fig. 6.11 Micrograph of the proposed optical receiver.

able gain control is disabled by applying 0 V to the $V_{Control}$, which results in a maximum gain for the front end. The effect of a long wire bond for the supply voltage is modeled as a 4 nH inductor. As expected from the simulation, there is a low-frequency notch caused by the resonance between the inductance of the supply voltage's long wire-bond and the on-chip decoupling capacitors. The magnitude of the measured S_{21} is approximately 2 dB larger than the simulation, while its bandwidth is approximately 1.4 GHz smaller. The S_{21} obtained in simulation also shows a low frequency cutoff of 1.9 MHz which is smaller than the low frequency cutoff 2.8 MHz in the transimpedance simulation. For frequencies larger than 10 GHz, the large difference between the measured and simulated S_{12} resulted from a signal coupling between the input and output pads.

The transimpedance gain (Z_T) of the front end is extracted from the measured S-parameters by

$$Z_T = Z_0 \frac{S_{21}}{1 - S_{11}} \tag{6.16}$$

where Z_0 is the characteristic impedance of 50 Ω. The simulated and measured transimpedance gain is compared in Fig. 6.13. The transimpedance gain is approximately 68.1 dBΩ (or 2541 Ω), which is 2.2 dB larger than the simulation result. It shows a 3 dB bandwidth of 13.2 GHz, which is 1.8 GHz smaller than the simulation result.

The increase in the transimpedance gain and the reduction in the bandwidth of the

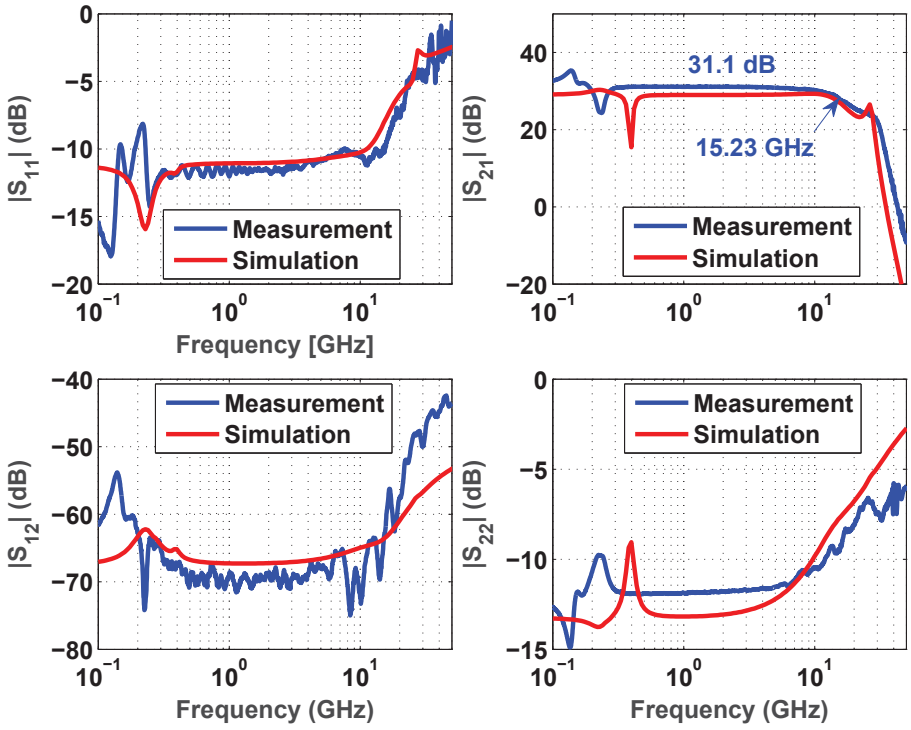


Fig. 6.12 Measured S-parameter in comparison with the simulated S-parameter.

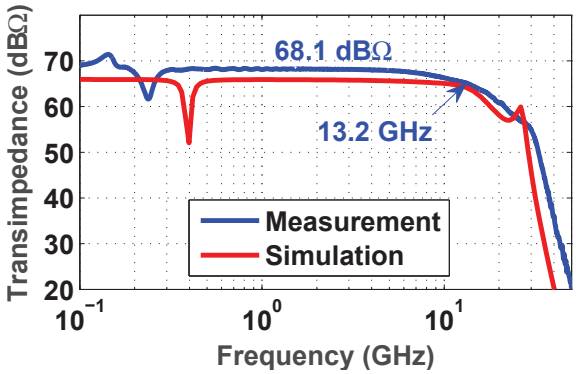


Fig. 6.13 Extracted transimpedance gain from measured S-parameter in comparison with the simulated transimpedance gain.

fabricated chip may be due to larger feedback resistors in the TIA and post-amplifier relative to the designed values due to process variation. The higher resistance value in the offset cancellation loop also reduces the low frequency cutoff of the receiver.

By setting the 3 bit positive feedback to 111 (3 bit PFB=111), the measured transimpedance gain increases by 1.3 dB to 69.4 dBΩ, while the bandwidth increases by 0.4 GHz to 13.6 GHz. Applying a voltage larger than 0.6 V to the $V_{Control}$ reduces the voltage gain and increases the bandwidth of the front end, as is shown in Fig. 6.14. The receiver shows a maximum gain-bandwidth product of 33.16 THzΩ for a $V_{Control}$ of 0.6 V for a bandwidth of 13.2 GHz and gain of 2512 Ω. Further, a minimum gain-bandwidth product of 5.74 THzΩ is obtained for a $V_{Control}$ of 0.9 V for a bandwidth of 19 GHz and gain of 302 Ω.

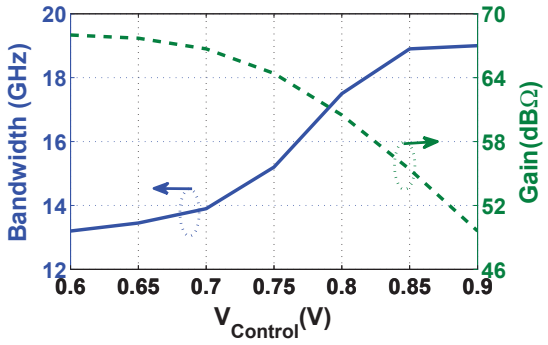


Fig. 6.14 Measured bandwidth and gain of the receiver front-end for various $V_{Control}$.

Noise Measurement

The noise standard deviation is measured at the front end output without applying any input signal to the receiver. The total standard deviation (σ_{Total}) is 4.11 mV_{rms}. The receiver noise is calculated from σ^2_{RX}=σ^2_{Total}-σ^2_{Scope}, where the noise standard deviation (σ_{Scope}) of a disconnected 30 GHz scope is measured to be 0.47 mV_{rms}. The noise standard deviation of the front end (σ_{RX}) is 4.08 mV_{rms} when the offset cancellation feedback is enabled, the 3 bit positive feedback is set to 000, and 0 V is applied to the $V_{Control}$. By enabling all positive feedback for control bits of 111 (3 bit PFB=111), the standard deviation of the receiver increases to 4.87 mV_{rms}. Applying 0.9 V to the $V_{Control}$ increases

the noise standard deviation of the receiver to 10.7 mV_{rms}. Table 6.4 summarized the performance of the receiver front end for various receiver configurations.

Table 6.4 Front end performance for various receiver configurations.

	3-bit PFB =000 $V_{Control}$ = 0 V	3-bit PFB =111 $V_{Control}$ = 0 V	3-bit PFB =000 $V_{Control}$ = 0.9 V
Transimpedance gain	68.1 dBΩ	69.4 dBΩ	49.6 dBΩ
Bandwidth	13.2 GHz	13.6 GHz	19 GHz
Output noise (σ_{RX})	4.08 mV_{rms}	4.87 mV_{rms}	10.7 mV_{rms}

Transient Measurement

For the transient measurements presented in this subsection, the offset cancellation feedback is enabled, the 3 bit positive feedback is set to 000, and the variable gain control is disabled by applying 0 V to the $V_{Control}$.

The test setup used for the bit error rate (BER) and eye diagram measurements is shown in Fig. 6.15. A 400 mV_{p-p} output of a bit pattern generator (BPG) is attenuated with an 18 GHz variable attenuator to reduce the amplitude of the input signal. The attenuator changes from 0 to 69 dB and with 1 dB attenuation step. Then, the signal is applied to the input pad of the receiver front end. The amplified output is detected by an error analyzer (EA) for BER measurement and by a 30 GHz scope for eye diagram measurement. The loss of the cables and connectors is ignored in the measurement results.

The BER measurement for NRZ-OOK pseudorandom binary sequence (PRBS) 2^7-1 data for different bit rates are plotted in Fig. 6.16(a). Figure 6.16(b) shows the sensitivity of the receiver front end for BER lower than 10^{-12} and different PRBS patterns. The sensitivity of the front end at a bit rate of 30 Gb/s increases from 7 mV_{p-p} for PRBS 2^7-1 (PRBS7) data to 11.25 mV_{p-p} for PRBS 2^{31}-1 (PRBS31) data, which corresponds to a

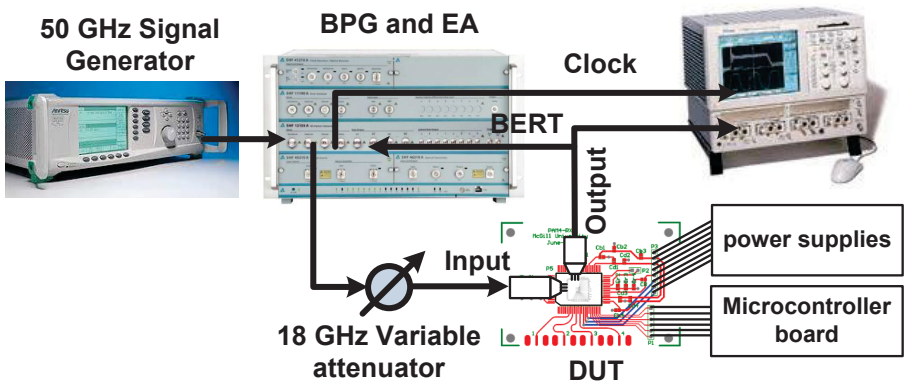


Fig. 6.15 Test setup for transient measurement with an electrical input signal.

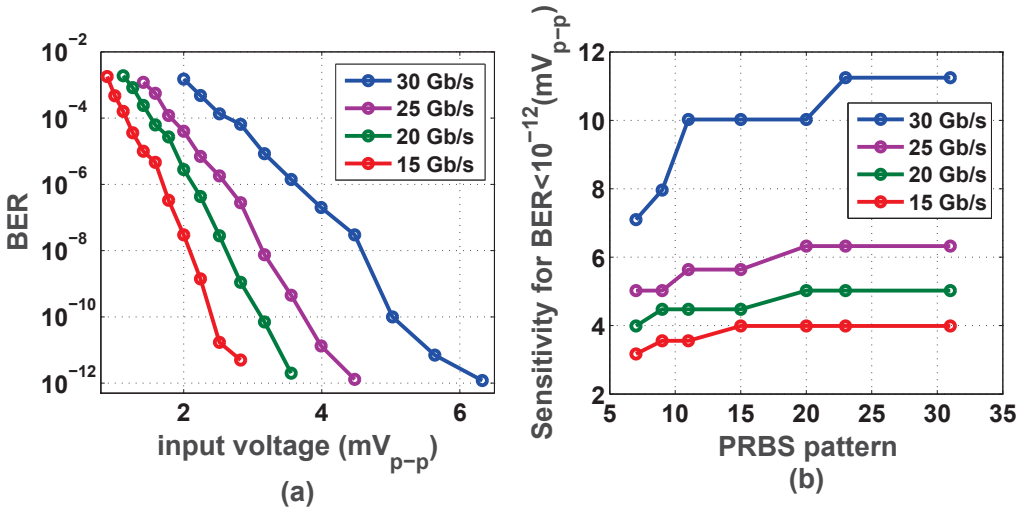


Fig. 6.16 (a) BER measurement for various bit rates with respect to the received peak-to-peak input voltage; (b) input sensitivity for BER lower than 10^{-12} with respect to the different lengths of PRBS data.

2 dB power penalty for 30 Gb/s bit rate; for the other measured bit rates, the power penalty is 1 dB. The power penalty for a longer length of PRBS data results from larger jitter and baseline wander due to the low cut-off frequency of the receiver front end [90]. To decrease the baseline wander effect on the long PRBS pattern, the low frequency cutoff of the receiver should be in the range of a few hundred kHz. This can be achieved by increasing the resistance and capacitance of the offset cancellation feedback by a factor of

three to four. A schematic simulation is performed to further confirm the effect of low cut-off frequency on different PRBS pattern lengths. In this simulation, the output buffer and offset cancellation feedback are added to the schematic shown in Fig. 6.7. Figure 6.17 compares the simulated output of the optical receiver for 30 Gb/s 30 μA_{p-p} PRBS7 (in blue) and PRBS15 (in red) input signals. The simulation results show a low frequency modulation for PRBS15 pattern that reduces the maximum eye opening from 84.6 mV_{p-p} to 79.1 mV_{p-p} and increases the jitter from 1.4 ps to 3 ps. The reduction of eye opening results in 0.3 dB power penalty.

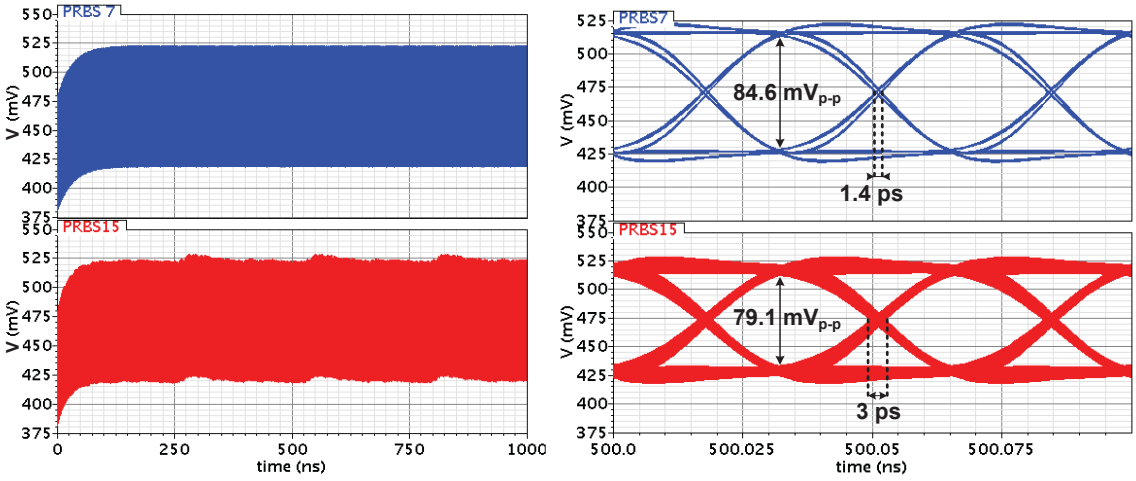


Fig. 6.17 Simulated output of the optical receiver for 30 Gb/s 30 μA_{p-p} PRBS7 (in blue) and PRBS15 (in red) input signal.

The step response of the receiver front end is measured to study the effect of the low-frequency notch in the time domain operation. Figure 6.18 shows the response of the receiver front end for a 20 MHz square-wave input. The step response shows overshoot and ringing with an approximate period of 4.4 ns or a frequency of 227 MHz, which is the frequency of the notch in the measured S_{21}. As shown in Fig. 6.18, the undershoot degrades the average peak-to-peak amplitude by 20%, which results in 0.98 dB power penalty [90].

Figure 6.19 shows the output eye diagram of the front end for various bit rates of NRZ-OOK PRBS 2^{31}-1 data for an 8 mV peak-to-peak input signal. The larger inter-symbol

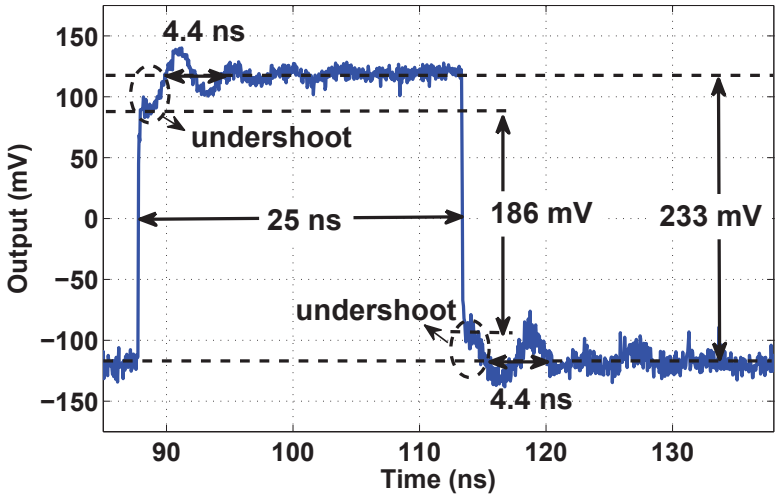


Fig. 6.18 Step response of the receiver front-end.

interference (ISI) at 30 Gb/s reduces the maximum eye opening by 55% in comparison with the maximum eye opening at 20 Gb/s.

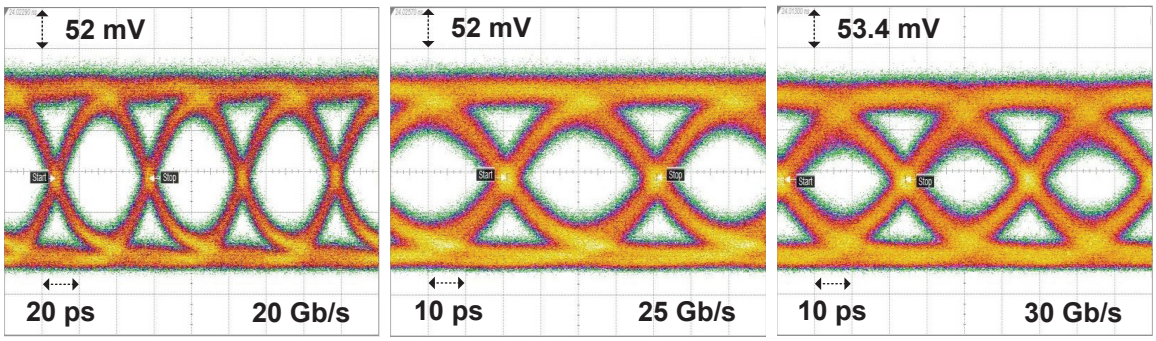


Fig. 6.19 Eye diagrams for 20 Gb/s, 25 Gb/s, and 30 Gb/s PRBS 2^{31}-1 NRZ-OOK data for 8 mV_{p-p} input signal.

The energy efficiency of the receiver was explored by measuring the BER across supply voltage at various data rates of PRBS 2^7-1 data pattern. Figure 6.20(a) shows the receiver sensitivity for BER lower than 10^{-12} for different power dissipation, while the related supply voltage is shown. At each data rate, the sensitivity improves before becoming constant as the supply voltage and hence power dissipation is increased. Figure 6.20(b) indicates the energy per bit with respect to the bit rate. The blue dashed line is calculated based on

the lowest power dissipation that provides the minimum peak-to-peak input sensitivity for each bit rate, while the red dashed line is calculated based on the lowest power dissipation for input signal sensitivity of 5 mV_{p-p} at bit rates of 25 Gb/s and lower.

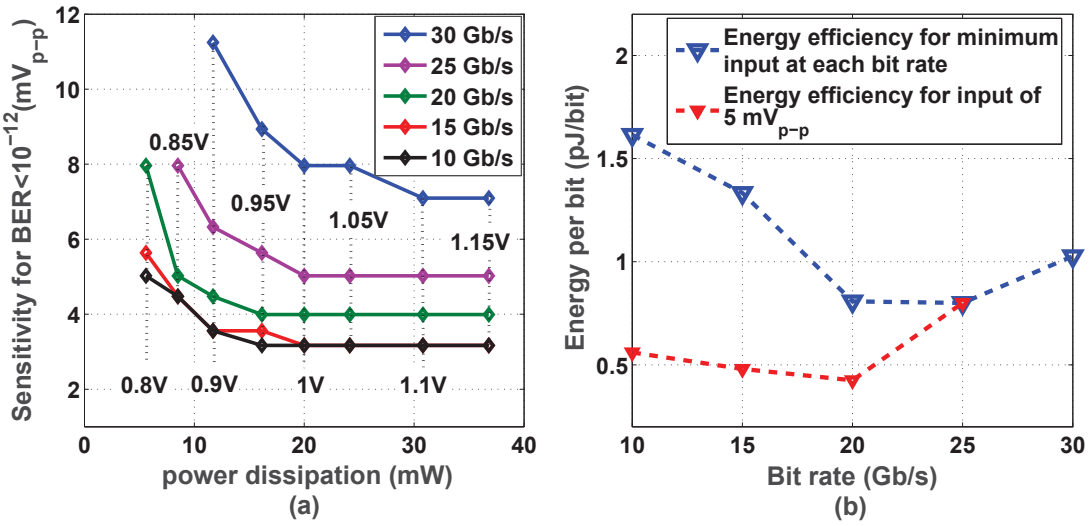


Fig. 6.20 (a) The input sensitivity of the front end for BER less than 10^{-12} for various power dissipation; (b) energy efficiency for different bit rates.

The proposed receiver front end has an energy efficiency of 1.03 pJ/bit at 30 Gb/s bit rate for an input sensitivity of 7 mV_{p-p} and supply voltage of 1.1 V. The receiver operates at minimum sensitivity with an energy efficiency of 0.8 pJ/bit for bit rates of 20 Gb/s and 25 Gb/s. For the input sensitivity of 5 mV_{p-p}, the front end shows the energy efficiencies of 0.425 pJ/bit at 20 Gb/s at a supply voltage of 0.85 V.

6.3 Receiver Measurements with Wire-Bonded Si-PD

The proposed receiver front end is packaged with the focusing grating-assisted silicon photodetector (Si-PD no. 4) discussed in subsection 5.1.2. The performance of the Si-PD at 14 V reverse-bias voltage is demonstrated in section 5.2, while in this chapter the Si-PD operates at a reverse-bias voltage lower than 0.5 V. The Si-PD has a responsivity of

0.05 A/W, a dark current of 20 pA, and a broad bandwidth of 12.6 GHz at 0 V reverse-bias voltage. High bandwidth at low reverse-bias voltage makes this photodetector a perfect candidate for low-voltage applications. Further, it eliminates the equalization techniques required to compensate the low bandwidth of other types of Si-PD fabricated in a bulk CMOS technology. In addition, the photodetector potentially can be implemented in an SOI-based CMOS technology for monolithic integration with an optical receiver.

Figure 6.21 shows the micrograph of the proposed optical receiver with the wire-bonded Si-PD. The total size of the photodetector chip is 350 μm×460 μm, while the Si-PD occupies only 30 μm×80 μm of the area.

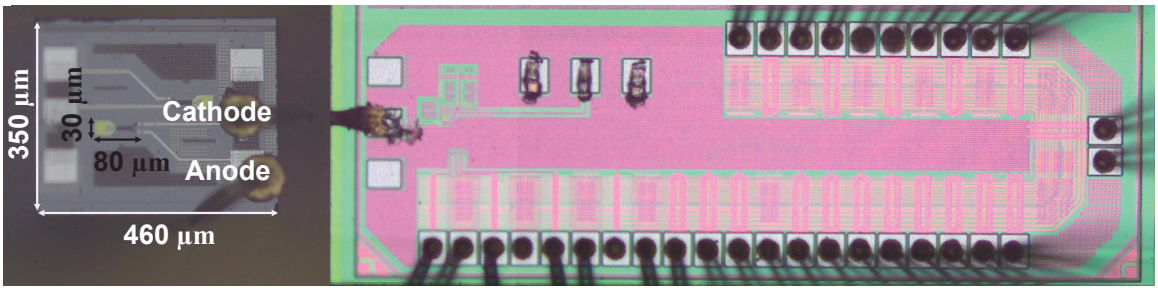


Fig. 6.21 The micrograph of the proposed optical receiver with the wire bonded all-silicon photodetector.

6.3.1 Optical Measurement Results

Figure 6.22 shows the test setup used for the eye diagram and BER measurements. The picture of the measurement test bed with landed fiber and probe is shown in Fig. 6.23. A continuous wave (CW) generated by a VCSEL source from Thorlabs with 11.8 dBm optical power at 848.2 nm is injected through a polarization controller (PC) with 0.5 dB insertion loss. A 40 GHz Mach–Zehnder modulator (MZM) with an extinction ratio of 14 dB and an insertion loss of 6.5 dB at 850 nm is driven by a baseband signal from the output of the BPG. For reducing the signal-to-noise ratio (SNR) in BER measurement, the modulated data are injected into a variable optical attenuator (VOA). A 99%–1%

directional coupler is used to monitor the average received optical power. Because the input grating coupler is polarization sensitive, the modulated data are then injected into another PC. The maximum optical power on the GC of the Si-PD is 2.5 dBm. The modulated optical signal is launched to the Si-PD and converted to a photocurrent. The optical front end converts the photocurrent into a voltage and amplifies it. The cathode of the Si-PD is wire-bonded to the input pad of the optical front end, which has a DC voltage of 0.41 V. To reduce the length of the wire bond of the photodetector, the anode of the Si-PD is wire-bonded to the bottom metal plate of the CQFP80 cavity, which is grounded. The optical front end has a 1.1 V supply voltage, and 0 V is applied to the $V_{Control}$ for maximum receiver gain while the 3 bit positive feedback is swept from 000 to 111 to find an optimum performance at each bit rate.

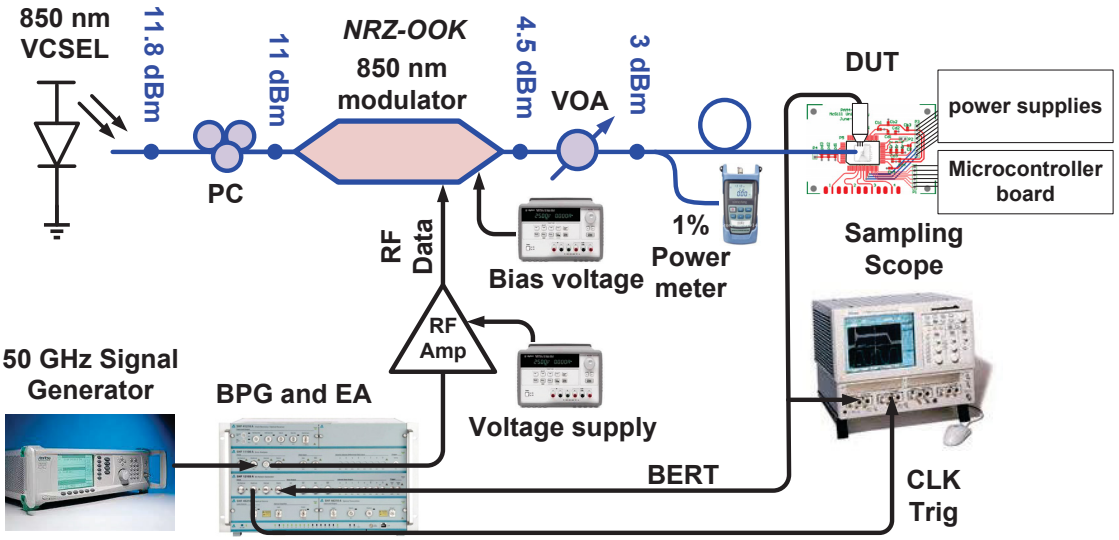


Fig. 6.22 Test setup for transient measurement with an optical input signal.

Figure 6.24 shows the output eye diagram for 20 Gb/s NRZ-OOK PRBS 2^{31}-1 data for an average optical power of 0 dBm. Eye diagrams are compared when the 3 bit positive feedback is set to 000 and 111. As expected, the front end has a larger gain that increases the peak-to-peak eye diagram. Further, the quality of the eye diagram is improved due to

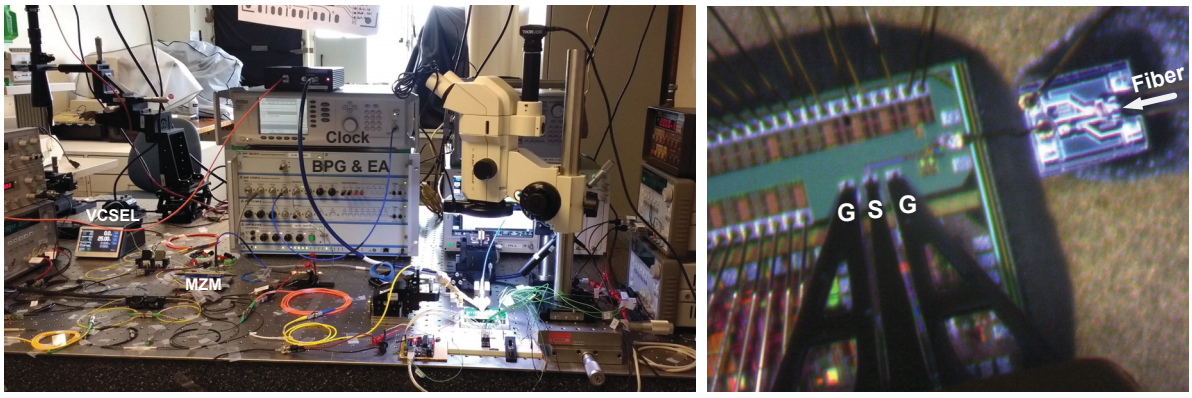


Fig. 6.23 Picture of the measurement test bed for transient measurement with an optical input signal.

the increased bandwidth. Figure 6.25 shows the output eye diagram of the front end for 25 and 30 Gb/s bit rates NRZ-OOK PRBS 2^{31}-1 data for the average optical power of 0 dBm. At 25 Gb/s bit rate, the 3 bit positive feedback is set to 111. At 30 Gb/s bit rate, the 3 bit positive feedback is set to 000 since the quality of the eye diagram is slightly better than the eye for control bit of 111.

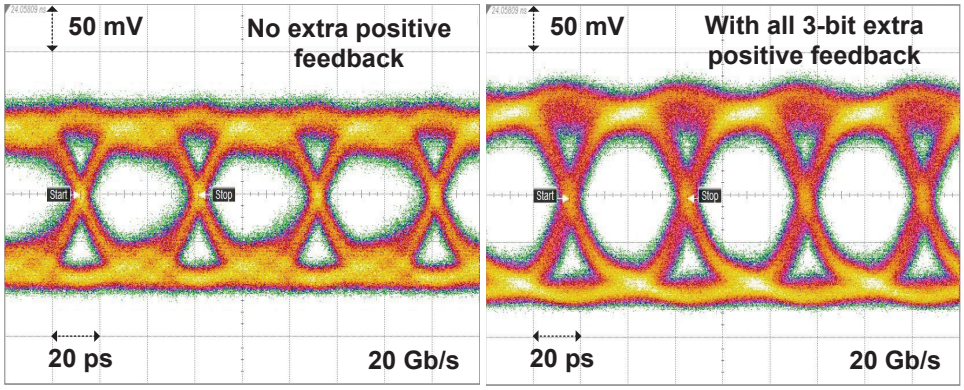


Fig. 6.24 Eye diagram for 20 Gb/s PRBS 2^{31}-1 NRZ-OOK data for 0 dBm average optical power.

Next, the BER is measured for the NRZ-OOK PRBS 2^{7}-1 data at different bit rates. Figure 6.26 shows the BER measurement with respect to the optical modulation amplitude (OMA). For bit rates of 20 Gb/s and 25 Gb/s, the 3 bit positive feedback is set to 111, while at 30 Gb/s is set to 000.

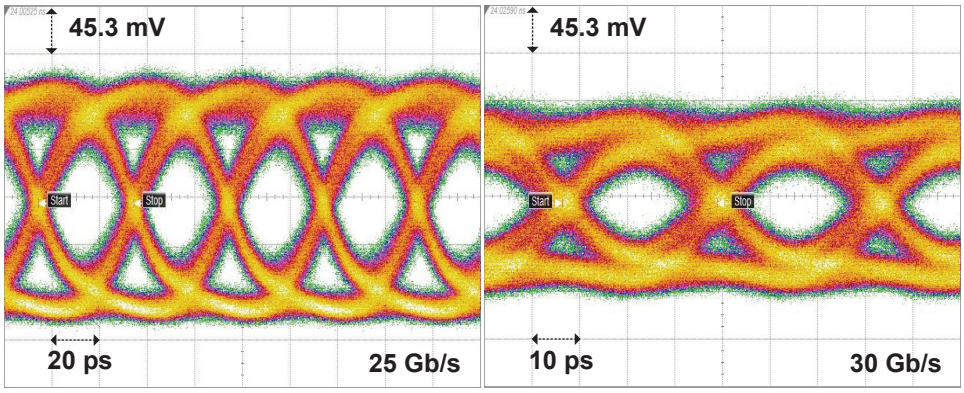


Fig. 6.25 Eye diagrams for 25 Gb/s, and 30 Gb/s PRBS 2^{31}-1 NRZ-OOK data for average optical power of 0 dBm.

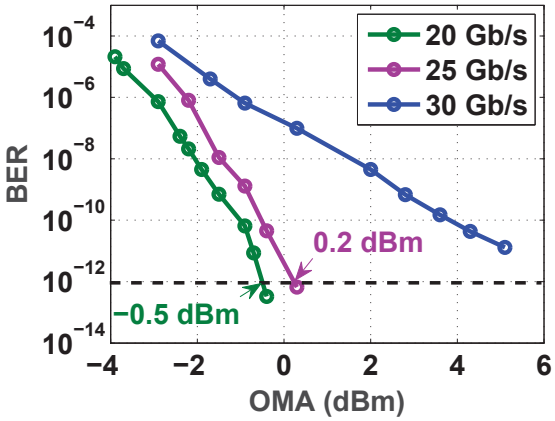


Fig. 6.26 BER measurement for NRZ-OOK PRBS 2^7-1 data.

The optical front end has input sensitivities of -0.5 dBm and 0.2 dBm OMA for BER of 10^{-12} at bit rates of 20 Gb/s and 25 Gb/s, respectively. The highest data rate of the receiver is limited by the low bandwidth (12.6 GHz) of the photodiode at a low reverse-bias voltage and the large group delay variation caused by the inductance of the Si-PD's wire bonds. Further, the BER is measured for the NRZ-OOK PRBS 2^{31}-1 data. The sensitivity of the optical receiver degrades by 0.3 dB and 4 dB for bit rates of 20 and 25 Gb/s, respectively.

The peak-to-peak current sensitivity is calculated from the OMA sensitivity and responsivity of the Si-PD. The input current sensitivity of the proposed optical front end is

46 μA_{p-p} at 20 Gb/s, which results in an input-referred current noise of 3.28 μA_{rms} [73].

Table IV summarizes the performance of the proposed optical receiver with wire-bonded Si-PD and compares it with previously published high-speed optical front ends for 850 nm applications. To evaluate the performance of the proposed optical receiver, a figure of merit (FoM) is introduced that is related to the process node, data rate (DR), energy per bit, chip area, and the peak-to-peak current sensitivity (I_{in}) of the receiver.

$$FoM = \frac{DR(Gb/s) \times Technology(nm)}{Energy(pJ/bit) \times I_{in}(\mu A_{p-p}) \times Area(mm^2)} \tag{6.17}$$

Overall, the proposed optical front end has at least 31% larger FoM in comparison with other optical receivers. The proposed optical front end also shows the lowest peak-to-peak current sensitivity of 54 μA_{p-p} at 25 Gb/s data rate while providing a reasonable energy efficiency of 1.23 pJ/bit. The low responsivity of 0.051 A/W at 0.4 V reverse-bias voltage of the Si-PD leads to a larger optical sensitivity in comparison with other optical front ends. Note that the responsivity of the proposed Si-PD increases to 0.3 A/W for 14 V reverse-bias voltage, which would improve the optical sensitivity to -7.45 dBm. However, the packaging arrangement in this work preventing us from measuring the performance of the receiver with a large reverse-bias voltage.

It is worth mentioning that the offset cancellation feedback capacitor of the proposed optical receiver occupies more than 45% of the area. Using another offset cancellation technique that doesn't require an on-chip capacitor reduces the chip area of the proposed receiver considerably. Although the conventional inverter-based optical receiver in [99] has been fabricated in 90 nm CMOS, it shows a smaller chip area in comparison with the proposed design due to the 30% smaller offset cancellation feedback capacitor.

The integrated avalanche Si-PD in [101] has a responsivity of 0.273 A/W and 3-dB bandwidth of 1.1 GHz at 12.3 V reverse-bias voltage. However, the proposed silicon pho-

todetector has a large bandwidth of 12.6 GHz at 0 V and can support high-speed operation without requiring any equalization techniques.

Table 6.5 Performance summary of the proposed front end compared with the recently published works.

	ISSCC'12 [99]	JSSC'15 [80]	JSSC'15 [81]	JSSC'16 [102]	JSTQE'16 [101]	CICC'17 [103]	This work
Technology	CMOS 90 nm	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm	CMOS 28 nm	CMOS 65 nm
Front-end topology	TIA+LA	TIA+LA	TIA+LA+CDR	TIA+IIR-DFE	TIA+LA+CTLE +On-chip Si-PD	TIA+ID	TIA+PA
Peaking inductor	No	Yes	Yes	No	Yes	No	No
Wavelength	850 nm	850 nm	N.A.	850 nm	850 nm	850 nm	850 nm
PD responsivity	0.55 A/W	0.47 A/W	N.A.	0.5 A/W	0.272 A/W at 12.3 V	0.5 A/W	0.051 A/W at 0.41 V
Data rate	22 Gb/s	25 Gb/s	25-26.5 Gb/s	20 Gb/s	18 Gb/s	20 Gb/s	25 Gb/s
Gain	76 dBΩ	72.5 dBΩ	71 dBΩ	—	102 dBΩ	—	69.4 dBΩ
Data pattern	PRBS 2^7-1	PRBS 2^7-1	PRBS 2^7-1	PRBS 2^7-1	PRBS 2^{15}-1	PRBS 2^7-1	PRBS 2^7-1
Sensitivity@ 10^{-12} current	138 μA_{p-p}	98 μA_{p-p}	106-184 μA_{p-p}	88.9 μA_{p-p}	88 μA_{p-p}	69 μA_{p-p}	54 μA_{p-p}
Sensitivity@ 10^{-12} OMA	-6 dBm	-6.8 dBm	N.A.	-7.5 dBm	-4.9 dBm	-8.6 dBm	0.2 dBm
Power efficiency	1.14 pJ/bit	2.72 pJ/bit	1.35 pJ/bit (front-end)	0.75 pJ/bit	2.7 pJ/bit	0.7 pJ/bit	1.23 pJ/bit
Total area	0.0038 mm^2	1.0725 mm^2*	0.32 mm^2**	0.027 mm^2	0.23 mm^2	0.005 mm^2	0.0056 mm^2
FoM $\frac{(Gb/s)(nm)}{(pJ/bit)(mm^2)(\mu A)}$	3312	22.7	21.67	722.1	21.4	2318.8	4368.8

LA:limiting amplifier;**EQ:** equalizer; **CDR:** clock and data recovery; **IIR-DFE:** infinite impulse response-decision feedback equalizer;
PA: post-amplifier; **CTLE:** continues-time linear equalizers; **ID:** integrate-and dump circuit.
***** There are 4 receivers in that area.
****** Total area of the optical receiver with CDR.

6.4 Summary

This chapter presents the design and experimental results of a novel low-power and compact 25 Gb/s optical receiver in 65 nm TSMC technology. It was prototyped with a novel low-voltage SOI-based all-silicon photodetector (Si-PD). The receiver front end consists of an inverter-based feedback TIA and three cascaded inverter-based CH amplifiers. To this structure, variable positive feedback and third-order interleaved active feedback are added to increase the total bandwidth of the optical front end. The proposed optical receiver has a transimpedance gain of 69.4 dBΩ, a bandwidth of 13.6 GHz, and an input-referred noise of 3.28 μA_{rms}. It occupies only 0.0056 mm^2 and consumes 30.8 mW at 1.1 V supply voltage. The photodetector used in this demonstration has a responsivity of 0.05 A/W, a dark current of 0.02 nA, and bandwidth of 12.6 GHz at 0 V bias voltage. The optical receiver with wire-bonded Si-PD has input sensitivities of -0.5 and 0.2 dBm, for bit error rate (BER) of 10^{-12} at data rates of 20 and 25 Gb/s, respectively, while the Si-PD has a reverse-bias voltage of 0.41 V. The energy efficiency of the optical front end is 1.23 pJ/bit at 25 Gb/s data rate. Additional electrical measurement results show that the receiver front end has input sensitivities of 3.6, 4.5, and 6.4 mV_{p-p} for BER of 10^{-12} at data rates of 20, 25, and 30 Gb/s, respectively. Further, the electrical measurement with supply voltage lower than 1.1 V shows that, for input sensitivity of 5 mV_{p-p}, it has energy efficiencies from 0.425 to 0.8 pJ/bit for data rates between 10 to 25 Gb/s and supply voltages from 0.8 to 1 V.

Chapter 7

Other Work

This chapter presents a research project that is not directly related to the content of this thesis and is performed in parallel with our research work. We have designed a novel 25 Gb/s ring-based DAC-less PAM-4 modulator. The following sections present the design and measurement results of this device. The work presented in this chapter has been presented at Photonics North Conference 2016 [104] and published in IEEE Journal of Selected Topics in Quantum Electronics (JSTQE) [105].

7.1 25 Gb/s DAC-Less Ring-Based PAM-4 Modulator

Modulators based on Mach-Zehnder interferometer (MZI) and ring resonator are the two main types of modulators demonstrated in an SOI technology for bit rates up to 50 Gb/s [106–108]. While the MZI modulator is more thermally stable and more robust to fabrication variation compared to the ring modulator, the latter shows a lower loss and excellent modulation efficiency at lower peak-to-peak voltage driving signal leading to a more energy efficient approach [109]. Also, the compact size of an SOI ring resonator relative to an MZI modulator makes it a cost-effective candidate for a WDM system that

requires high integration of electro-optical devices [16].

For increasing the throughput of a bandwidth-limited system, it is important to explore the functionality of these modulators in obtaining multilevel and complex modulation format. The pulse amplitude modulation (PAM) and particularly PAM-4 as the least complex form of a higher-order modulation has been the subject of intense research for high-speed short-reach optical interconnects. Recently, silicon photonics multi-segmented PAM-4 MZI modulators operating at data rates over 50 Gb/s are demonstrated [110, 111]. The multi-segmented electrode substantially replaces a linear electrical digital-to-analog converters (DAC), commonly used to achieve multilevel electrical driving signal, with an optical DAC. In this work, we explore designing a multi-segmented electrode ring-based PAM-4 modulator. We present the first experimental demonstration of a reverse biased MZI-assisted ring modulator, where two p-n diode segments are designed on the MZI arm for inter-coupling modulation. The phase of the two independent electrical driving signals is adjusted such that a 25 Gb/s (12.5 Gbaud/s) PAM-4 signal is achieved at the output.

7.2 Design and Fabrication of the Proposed PAM-4 Modulator

Figure 7.1 shows the proposed inter-coupling modulator with single drive diode segments. For generating the same amount of phase shift, the single drive inter-coupling modulator requires approximately twice the length of the diode segment in a dual drive push-pull mode inter-coupling modulator. However, the diode phase shifters and two optical waveguide arms do not require perfect symmetry, which relaxes the fabrication tolerance of this type of modulator. Further, the inter-coupling PAM-4 modulator can be driven with single ended electrical signals reducing the complexity of the voltage settings. In such configuration, the optical signal modulation is enabled by coupling modulation, change in the round-trip phase shift and slight variation of its loss. The modulator has two p-n diode segments in

the lower arm of the balanced MZI with lengths of L_{LSB} = 220 μm and L_{MSB} = 330 μm. There are also two thermal heaters, which is implemented by the top metal layer. The smallest p-n diode segment generates a phase shift $\Delta\phi_1$ with an RF signal V_1 representing the lowest significant bit (LSB). The largest p-n diode segment produces a phase shift $\Delta\phi_2$ with an RF signal V_2 representing the most significant bit (MSB). The top heater on the ring cavity (heater-1) enables a shift in the resonance wavelength. The top heater on the lower arm of the MZI (heater-2) generates the required initial phase θ to optimize the extinction ratio and exploit the linear optical transmission portion of the modulator. In this device, the ring cavity length (L_{ring}) and MZI coupling length (L_c) are determined mainly based on the total length of the two p-n diode segments to generate the required phase shift for modulation.

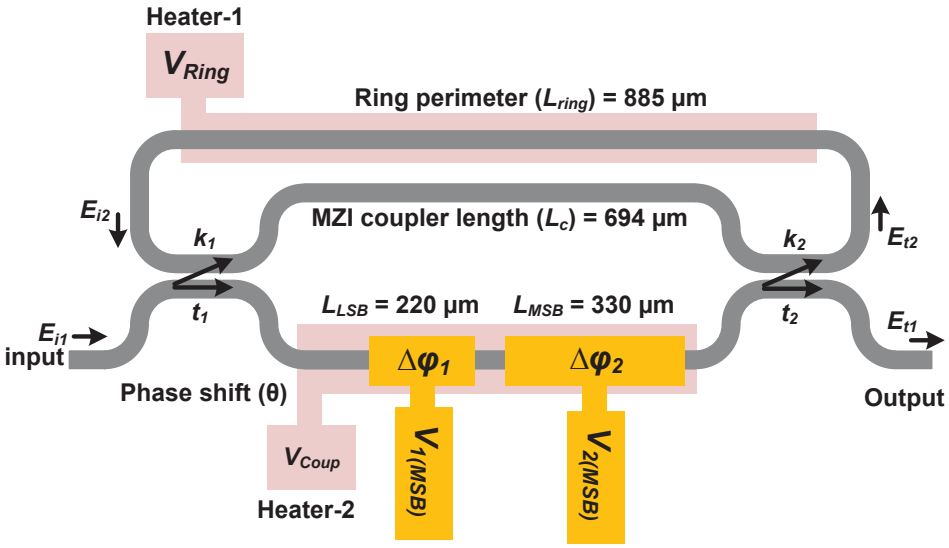


Fig. 7.1 Schematic of the proposed inter-coupling modulation based PAM-4 ring modulator.

7.2.1 Design Methodology

This part describes the simulation method used to determine the required length of the two p-n diode segments towards optimal extinction ratio at the targeted reverse bias voltage.

The transfer matrix and transfer function between the MZI input electric fields (E_{i1} and E_{i2}) and the MZI output electric fields (E_{t1} and E_{t2}) are given by

$$\begin{pmatrix} E_{t1} \\ E_{t2} \end{pmatrix} = \begin{pmatrix} T_1 & K_2 \\ K_1 & T_2 \end{pmatrix} \begin{pmatrix} E_{i1} \\ E_{i2} \end{pmatrix} \tag{7.1}$$

$$E_{i2} = \alpha_{ring} \exp(-j\delta) E_{t2} \tag{7.2}$$

where α_{ring} is the total loss, and δ is the phase due to the ring cavity length (L_{ring}) and the effect of heater-1. The matrix elements T_i and K_i representing the transmission from input port i of the MZI to the through-port and cross-port output, respectively (i = 1, 2). They are calculated using the following equations.

$$T_1 = t_1 t_2 \alpha_{arm1} \exp\left(-j(\phi + \Delta\phi_1 + \Delta\phi_2 + \theta)\right) + k_1 k_2 \alpha_{arm2} \exp(-j\phi) \tag{7.3}$$

$$T_2 = t_1 t_2 \alpha_{arm2} \exp(-j\phi) + k_1 k_2 \alpha_{arm1} \exp(-j(\phi + \Delta\phi_1 + \Delta\phi_2 + \theta)) \tag{7.4}$$

$$K_1 = k_1 t_2 \alpha_{arm2} \exp(-j\phi) + t_1 k_2 \alpha_{arm1} \exp(-j(\phi + \Delta\phi_1 + \Delta\phi_2 + \theta)) \tag{7.5}$$

$$K_2 = k_1 t_2 \alpha_{arm1} \exp(-j(\phi + \Delta\phi_1 + \Delta\phi_2 + \theta)) + t_1 k_2 \alpha_{arm2} \exp(-j\phi) \tag{7.6}$$

where t_1 and k_1 are the transfer functions of the electric field coupled to the through-port and cross-port of the first directional coupler, respectively; and t_2 and k_2 are the transfer functions of the electric field coupled to the through-port and cross-port of the second directional coupler, respectively. The variable ϕ_1 is the phase due to the MZI coupling length (L_c) and θ is the initial phase generated with thermal heater. For an ideal 50/50 compact directional coupler, t=$1/\sqrt{2}$ and k=$\exp(-j\pi/2)/\sqrt{2}$, at a specific wavelength. Due to fabrication process variation, however, the coupling coefficient of the directional couplers differs and considerably affect the performance of the device. The variables α_{arm1}

and α_{arm2} are the total losses in the lower and upper arms of the MZI, respectively. The electric field transfer function of the device is calculated by

$$\frac{E_{t1}}{E_{i1}} = \frac{T_1 - (T_1T_2 - K_1K_2)\alpha_{ring}\exp(-j\delta)}{1 - T_2\alpha_{ring}\exp(-j\delta)} \tag{7.7}$$

With the assumption of ideal 50/50 directional couplers and loss-less MZI, the solution to equation (7.7) leads to the following three equations.

$$T_1T_2 - K_1K_2 = \exp(-j(2\phi + \Delta\phi_1 + \Delta\phi_2 + \theta)) \tag{7.8}$$

$$T_1 = \sin((\Delta\phi_1 + \Delta\phi_2 + \theta)/2)\exp(-j(2\phi + \Delta\phi_1 + \Delta\phi_2 + \theta + \pi)/2) \tag{7.9}$$

$$T_2 = \sin((\Delta\phi_1 + \Delta\phi_2 + \theta)/2)\exp(-j(2\phi + \Delta\phi_1 + \Delta\phi_2 + \theta - \pi)/2) \tag{7.10}$$

Unlike the inter-coupling ring modulator with push-pull driving signals, where the resonance condition depends on the constant phases ($2\phi + \theta + \delta = 2\pi m$, m is integer), the resonance condition for a single ended driving signal ($2\phi + \Delta\phi_1 + \Delta\phi_2 + \theta + \delta = 2\pi m$, m is integer) depends on the variation of both phase shifts $\Delta\phi_1$ and $\Delta\phi_2$. Applying an electrical driving signal results in both a shift in the resonance wavelength as well as a change in the transmission amplitude.

The methodology presented in [48] is followed for simulating the general behavior of the device for various biasing conditions. First, the variation in the refractive index of the doped silicon in the presence of free carriers for various biasing voltages applied to the p-n diode is calculated. Then, by using the effective index method, the effective refractive index and the corresponding mode profile is computed. The voltage-dependent effective index and loss are calculated based on the mode profiles and charge carrier distributions [112]. Finally, based on the properties and geometry of the device and applied voltage, the electric field transfer function (7.7) is calculated for various wavelengths and bias voltages. The nor-

malized output transmission power is taken as the square of the absolute value obtained by eq. 7.7. Figure 7.2 shows the cross-section of the designed p-n diode segments with dimensions for each doping layer, which is used for the simulation. Doping densities were found using Sentaurus Device simulation software for the particular doping dose and doping energy for each doping layer. The average doping densities for the p++, p+, p, n++, n+ and n layers were found to be 1.2×10^{20} cm^{-3}, 1.8×10^{18} cm^{-3}, 4×10^{17} cm^{-3}, 3.3×10^{20} cm^{-3}, 3×10^{18} cm^{-3}, and 3.2×10^{17} cm^{-3}, respectively. The highly doped p++ and n++ layers were used to form the low resistance contact with the top metal layer. The intermediate doping layers (p+ and n+) were formed to reduce the series resistance [113]. The intermediate doping layers were 0.25 μm apart from the rib waveguide to minimize the optical propagation loss.

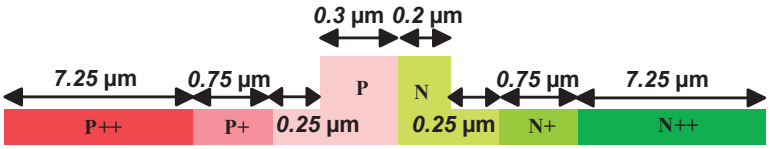


Fig. 7.2 Cross-section of the p-n diode segment with dimensions for each doping layer.

The total length of the p-n diode segments (220 μm and 330 μm) is determined based on the necessary phase shift for 0 to 1 modulation. In the inter-coupling ring modulator, the required phase shift ($\Delta\phi$) for 0 to 1 modulation is $\Delta\phi = \pi - 2(\sin(\alpha))^{-1}$, where α is the total round trip loss of the resonator cavity ($\alpha = \alpha_{ring} \times \alpha_{arm1} \times \alpha_{arm2}$) [114, 115]. With larger cavity loss (smaller α), more phase shift is required resulting in a larger total length of the p-n diode or larger applied voltage. For PAM-4 modulation, the length ratio of the longer and shorter p-n diode segments is designed to have four equidistant transmittivity levels for specific bias voltages of the LSB and MSB diode segments. The optimized design of the modulator has a cavity feedback length of L_{ring} = 885 μm and an MZI coupling length of L_c = 694 μm. The total design area of the modulator is 0.48 mm^2. Figure 7.3

shows the simulated spectral response of the designed PAM-4 modulator for four voltage conditions. The propagation loss of the undoped waveguide is considered to be 2 dB/cm. The simulation results show the inter-coupling effect where the resonance extinction ratio is changing for the applied voltages. The cavity phase shift effect on the resonance wavelength for various biasing voltages is also apparent. In this simulation, the initial phase of θ is set to 2.5 rad for optimum extinction ratio and linear performance. Based on the simulation results the free spectral range (FSR) of the design modulator is 0.39 nm.

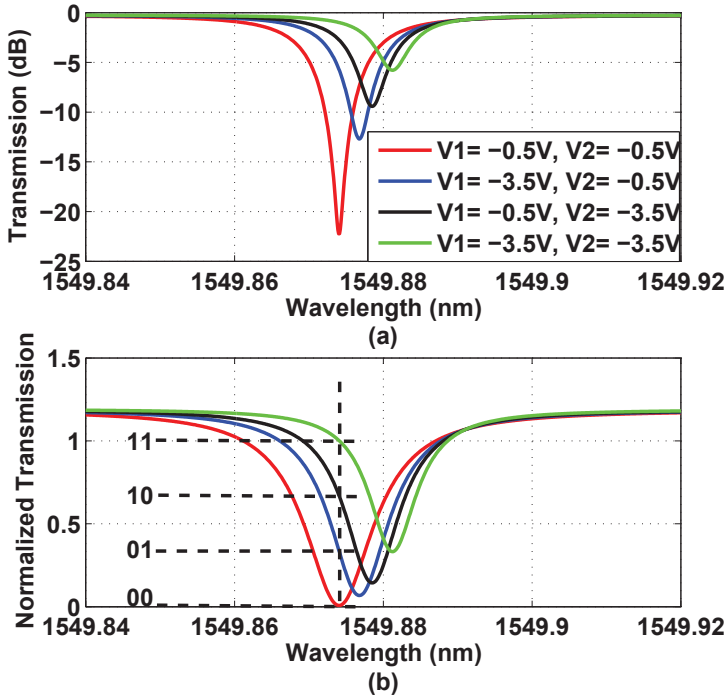


Fig. 7.3 The simulated spectral response of the modulator at for four input voltage conditions, (a) in logarithmic scale, (b) in linear scale.

7.3 Experimental Results

Figure 7.4(a) shows the characterization test setup of the fabricated modulator with the two DC and two GSGSG RF probes. The DC probes are used to apply DC voltages to the

heaters to optimize the ring modulator's extinction ratio (V_{Coup}) and to shift the resonance wavelength (V_{Ring}) to match the wavelength of the CW light source. Both the DC signals share common electrical ground (G) with the RF signals. Figure 7.4(b) shows a photograph of the external fiber array and electrical probe connections to the chip.

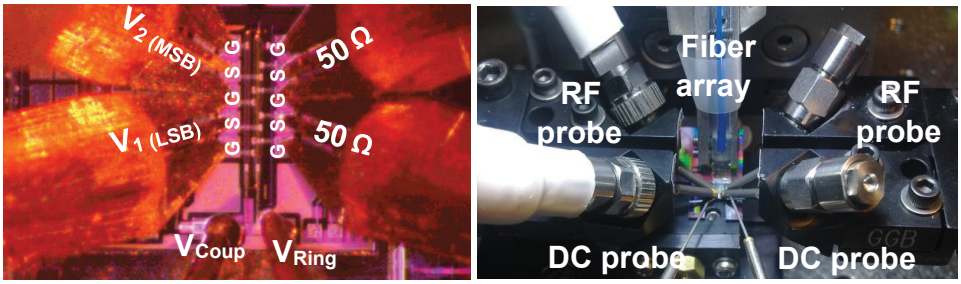


Fig. 7.4 (a) Image of the chip test setup with DC and RF probes. (b) Test setup photograph of the chip with fiber array and electrical probes.

7.3.1 DC Measurement

For determining the amplitude and DC bias of the electrical driving voltages and the resonance wavelength, a continuous wave (CW) laser source emitting an optical output power of 5 dBm is injected into the modulator. Its wavelength is swept from 1530 nm to 1565 nm. Figure 7.5(a) shows the spectral response of the modulator when the voltage at the thermal tuner/heater on top of the MZI arm is set to 1.2 V (current: 2 mA). The grating coupler (GC) pair transmission response shows around 2 dB insertion loss in the modulator. Figure 7.5(b) is a zoom on the spectral response of the modulator to measure the FSR of the modulator. The measured FSR is 0.38 nm, which is in line with the simulated results of 0.39 nm. Figure 7.5(b) also shows the full width at half max (FWHM) linewidth of 0.026 nm, at the resonance wavelength of $\lambda_0 = 1552.8$ nm, from the spectral response of the modulator.

Figure 7.6(a) shows the spectral response of the modulator recorded at 1552.8 nm for

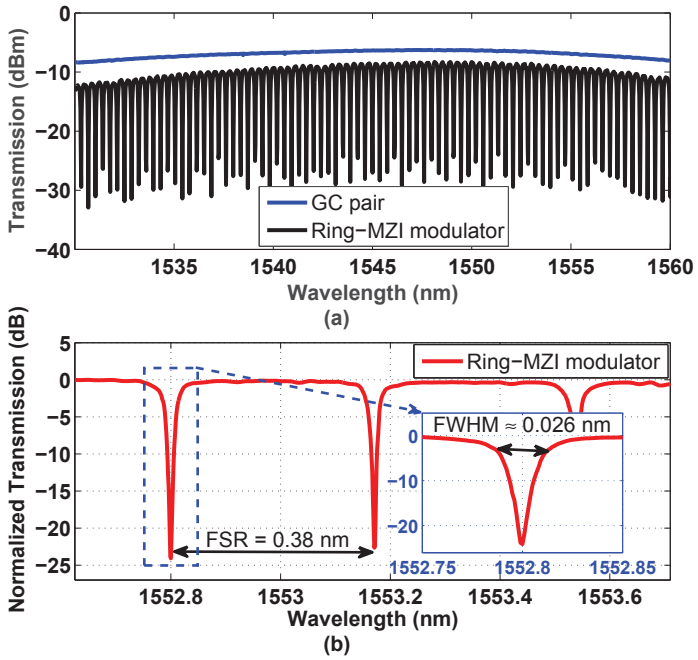


Fig. 7.5 (a) Spectral response of the GC pair and ring modulator; (b) Spectral response of the modulator (zoomed) to measure FSR with measured FWHM ≈ 0.026 measured from the spectral response of the ring modulator.

four input voltage conditions, which set the p-n electrode in the reverse-bias mode. For all circumstances, the fixed DC bias voltage to the thermal tuner/heater is maintained at 1.2 V (drawn current = 2 mA). As expected from the simulation results, while the resonance wavelength shifts, the extinction ratio also diminishes with changes in the applied voltage. The normalized optical power levels are 0 dB, -1.82 dB, -4.63 dB and -22.75 dB at 1552.8 nm wavelength. In the linear scale, Fig. 7.6(b), the four optical power levels correspond to the modulator transmittivity of 1, 0.65, 0.34 and 0.005, respectively. The four equidistant transmittivity values indicate that the ring modulator can properly generate a PAM-4 optical signal at the output when driven by two independent electrical signals.

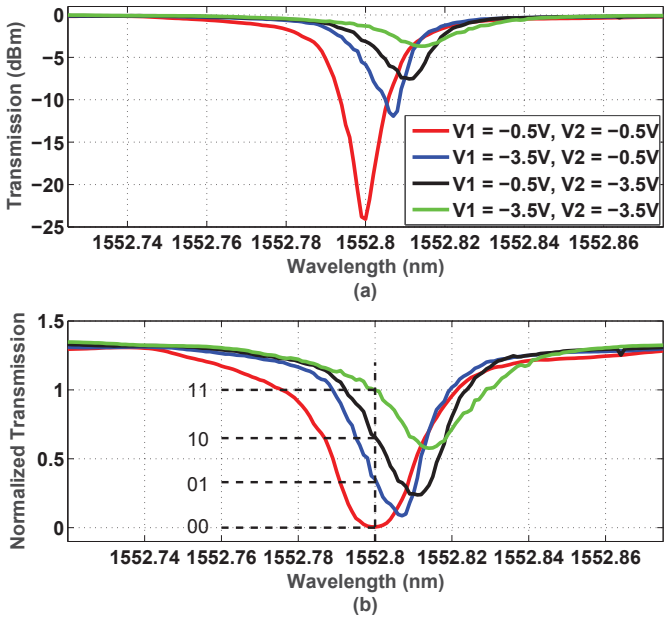


Fig. 7.6 Measured spectral response of the modulator at four input voltage conditions (a) in dB scale; (b) in linear scale.

7.3.2 Frequency Response Measurements

The frequency response of each LSB and MSB p-n diode segments are measured separately by a 50 GHz Agilent N5225A lightwave component analyzer and two 40 GHz GSG probes. One of the GSG probes is used to apply the electrical RF signal to the diode segment, while the second one is used to connect the off-chip 50 Ω termination. Figure 7.7 shows the S-parameter measurement (input reflection (S_{11}) in the top figures and electro-optic (EO) S_{21} response in the bottom figures) at 2 V reverse bias voltage of the short and long electrode segments with and without connecting a 50 Ω termination. A large reflection is expected without the 50 Ω termination in the S_{11} measurement (Fig. 7.7(a), top). The reflection drops after 12 GHz. With a 50 Ω termination, the reflection is reduced to below 20 dB up to 2 GHz and -10 dB at 12 GHz (Fig. 7.7(b), top). Although the smallest EO bandwidth measured from the S_{21} curves of the p-n diode without the 50 Ω termination is approximately 8.7 GHz, the high speed modulation is limited by the high reflection. At

2 V reverse bias voltage, both of the electrodes have OE bandwidth over 14 GHz with the 50 Ω termination.

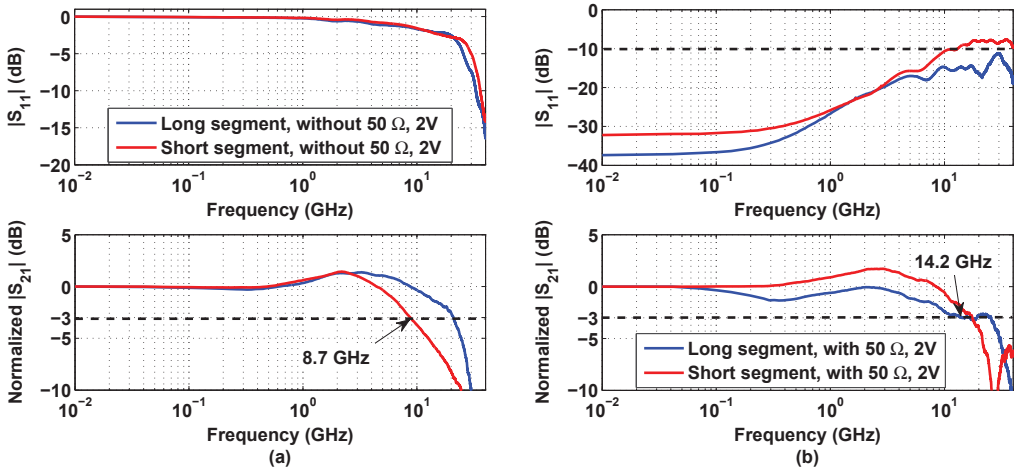


Fig. 7.7 S-parameter measurements: S_{11}-parameter and EO S_{21}-parameter of the long and short electrodes; (a) without 50 Ω termination; (b) with 50 Ω termination.

7.3.3 Transient Measurement

Figure 7.8 shows the experimental setup to generate an optical PAM-4 signal from the modulator. Two 12.5 Gb/s data rate Anritsu-MU181020A programmable pattern generator (PPG) cards are used in a synchronous mode to tune the phase of each of the electrical driving signal independently. As such, the rising and falling edges of the two input signals occur at the same time. Two independent 2^{31}–1 pseudo random bit sequence (PRBS) data from two PPGs are injected to two 20 GHz electrical amplifiers (model: Hittite HMC-C004) boosting the signal amplitude to 3 V_{p-p} and then be the input to two 6 GHz bias tees to add the desirable DC bias to the driving electrical signal. The two RF signals are injected to the LSB and MSB electrode segments of the inter-coupling ring modulator. The sub-figures on the left side of Fig. 7.9 shows the electrical eye diagrams of the 12.5 Gb/s driving signals for the MSB and LSB electrode segments, respectively. The bandwidth limitation of the two 6 GHz bias tees and noise injected by the electrical amplifier limits the signal to

noise ratio (SNR = 8) of the driving signal.

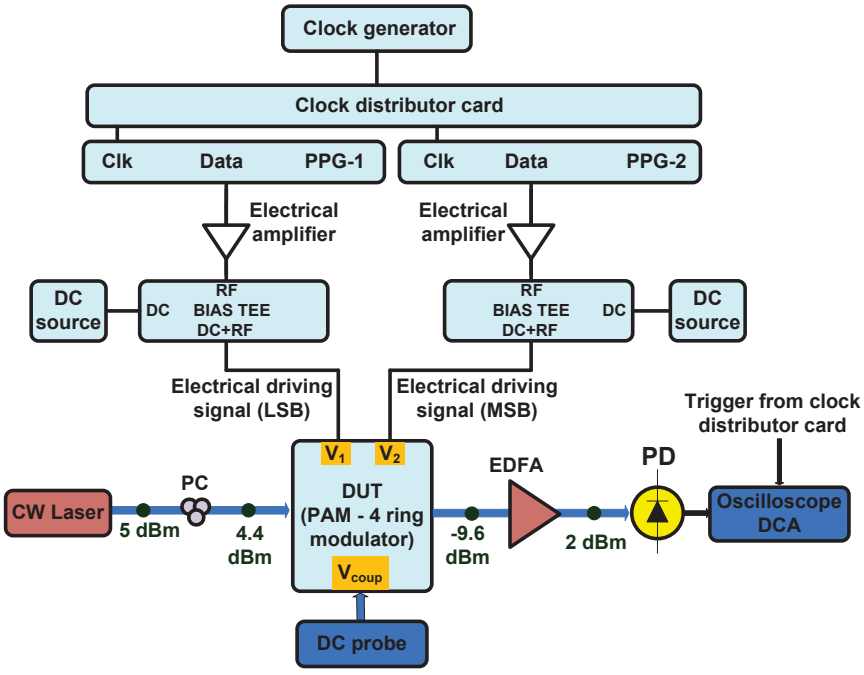


Fig. 7.8 Experimental setup to generate PAM-4 modulated signal.

A 5 dBm CW light at the wavelength of 1552.8 nm is launched through the polarization controller (PC) which optimizes the light coupled to the inter-coupling PAM-4 modulator. The average optical power at the output of the modulator is -9.6 dBm. The total optical loss from the laser to the modulator output consists of 0.6 dB insertion loss from the PC, 2 dB insertion loss from the modulator (DUT) and 6 dB loss per grating coupler. The optically modulated signal is amplified with an EDFA to increase the received optical signal to 2 dBm at the receiver. A commercial 45 GHz photodetector (PD) converts the optical PAM-4 signal. The electrical signal is finally captured with a sampling oscilloscope (DCA) with an RF bandwidth of 30 GHz. The right-side sub-figures on Fig. 7.9 show the photodetected electrical eye diagrams from the output of the ring modulator when it is driven by V_1 (LSB) and V_2 (MSB), one at a time. The peak-to-peak voltage amplitude of the modulated signal for the shorter p–n diode (V_1) is smaller (approximately half) than that

of the longer segment (V_2), as the LSB diode segment (or phase shifter) length is smaller than the MSB segment length.

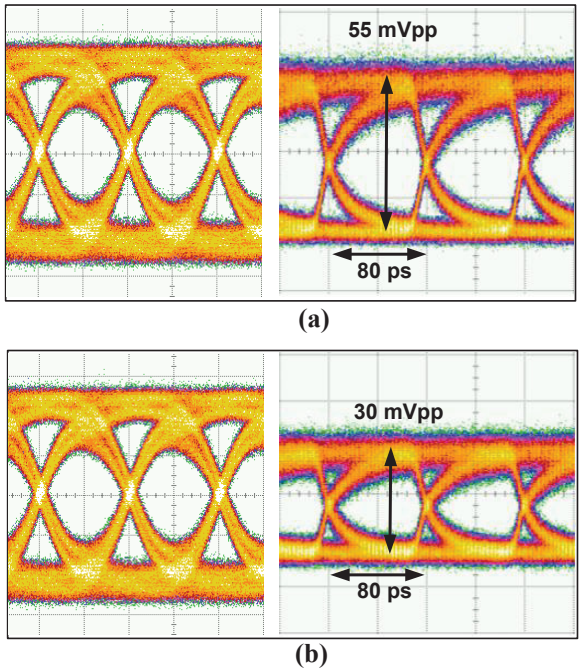


Fig. 7.9 Eye diagrams (12.5 Gb/s) at the output of the ring modulator when driven by (a) only V_2 (MSB), (b) only V_1 (LSB). The corresponding electrical eye diagrams are shown at the left.

Figure 7.10 shows the photodetected 25 Gb/s PAM-4 electrical eye diagram when the modulator is simultaneously driven by V_1 and V_2. The voltage difference between adjacent levels is approximately 27 mV leading to the symmetric four-level signal.

Table 7.1 summarized the recorded standard deviation (σ) of the '0' level and '1' level of the OOK eye diagram for both MSB and LSB segments and the standard deviation of each four level of the PAM-4 signal. The increase in the 'σ' of each of the four level indicates that there is some crosstalk between the two electrical driving signals.

For verifying that the original binary stream of the MSB and LSB OOK data can be properly recovered from the PAM-4 signal, a 2^7-1 PRBS data is captured by the sampling oscilloscope.

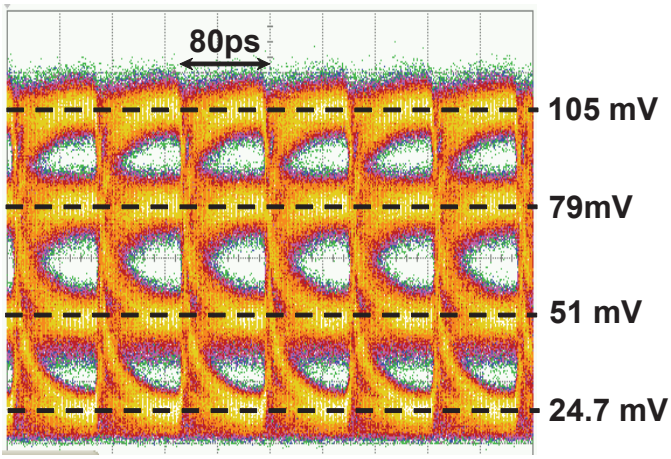


Fig. 7.10 PAM-4 eye diagram (12.5 GBaud/s) at the output of the ring modulator when simultaneously driven by V_1 (LSB) and V_2 (MSB) electrical driving signals.

Table 7.1 The standard deviation of the captured OOK and PAM-4 eye diagrams

	MSB (OOK)		LSB (OOK)		PAM-4			
Level	(0)	(1)	(0)	(1)	(00)	(01)	(10)	(11)
σ (mV)	3.5	4.8	2.5	3.3	4.3	5.2	5.1	5.2

Figure 7.11(a) shows the captured PAM-4 signal data stream which was then processed off-line in MATLAB to recover the two original MSB and LSB input data. Figure 7.11(b) shows the recovered MSB and LSB data. The regenerated data is compared against the original input MSB and LSB data, which shows no error in the modulated data.

The static and dynamic dissipated power are estimated separately for calculating the energy efficiency of the modulator is. The static power dissipated by the modulator is governed by the two 50 Ω termination loads ($P_{static1} = 2{\times}V_{DC}^2/50$), where V_{DC} = 2 V and the thermal heater ($P_{static2} = V_{th}{\times}I_{th}$), where V_{th} = 1.2 V, I_{th} = 2 mA. The total static power dissipation of the modulator is 6.5 pJ/bit. The dynamic power dissipation of the modulator is estimated by the switching energy ($E_s = CV_{p-p}^2$), where C is the parasitic capacitance of the diode segment and V_{p-p} is the peak-to-peak driving voltage [116]. Based

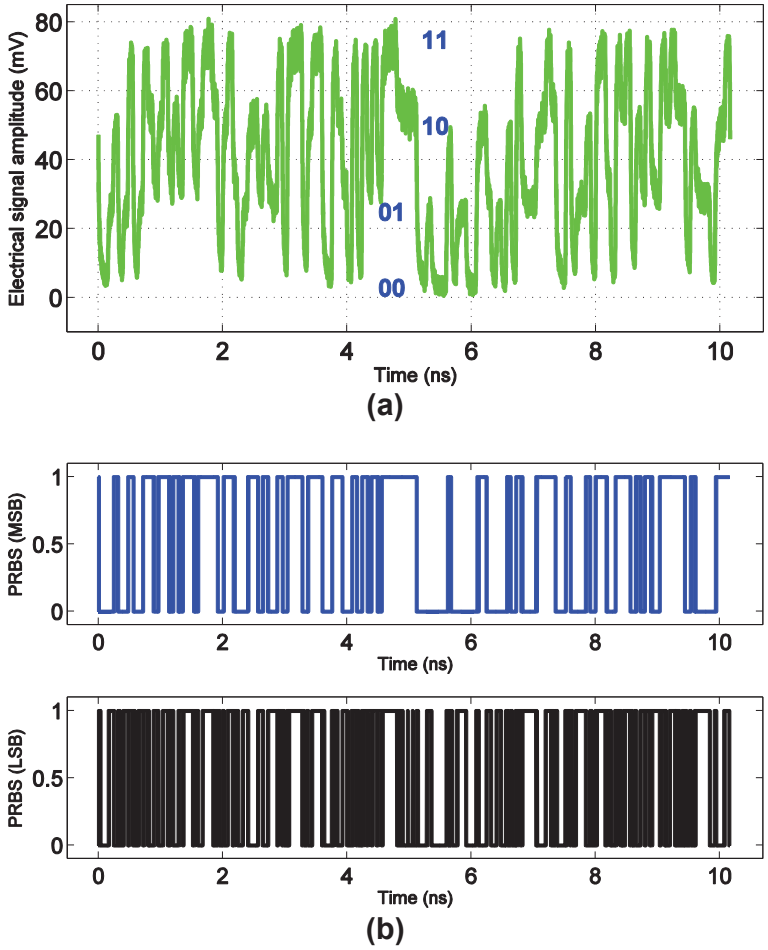


Fig. 7.11 (a) Pattern locked PAM-4 signal generated. (b) Recovered MSB and LSB patterns from the PAM-4 signal.

on the simulation results, the short diode segment has a parasitic capacitance of ∼34 fF, and the long diode segment has a parasitic capacitance of ∼51 fF. The estimated dynamic power consumption is 0.0765 pJ/bit and 0.144 pJ/bit for the short and long segment, respectively. Practically, the designed modulator can be wire-bonded or flip-chip to a driver. In such configuration, the 50 Ω termination is not required, because the driver can be designed for low reflection and optimum power transmission based on the load effect of the diode segments. Therefore, the static power consumption is limited to the power dissipates by the thermal heater on top of the MZI arm. In fact, using the 50 Ω termination

enables testing the modulator without the limiting effect of the high reflection.

7.4 Summary

This chapter presents the design and measurement results of a novel ring-based PAM-4 modulator. To the best of our knowledge, this is the first experimental demonstrations of silicon photonics (SiP) two-segment inter-coupling PAM-4 modulator with a single ended configuration. The 25 Gb/s (12.5 GBaud/s) PAM-4 eye diagram obtained with 3 V_{p-p} electrical driving signal shows promise towards the design of a power efficient optical modulator with a small footprint of 0.48 mm^2. It has an energy efficiency of 0.32 pJ/bit without considering the 6.4 pJ/bit static power, which is consumed by the 50 Ω termination. The design methodology of the proposed modulator was also presented. Driving the modulator with single ended electrical signal reduces the operational complexity of the modulator. The experimental values of the optical powers levels and free spectral range of the modulator closely agree with the simulation results presented in this work.

Chapter 8

Conclusions

In this thesis, three research directions have been explored, which are closely related to designing an efficient high-speed short-reach optical interconnect. In the first research direction, we have studied different hardware implementation of low-bit soft-decision forward error correction (SD-FEC) receivers and provided a complete analysis that predicts the decoding performance of multi-branch receiver configurations in short-reach applications. In the second direction, the silicon photonics (SiP) platform has been explored for developing more efficient optical devices such as germanium-on-silicon photodetectors (Ge-PD) and silicon photodetectors (Si-PD). Finally, in the third direction, a power-efficient and compact 25 Gb/s optical receiver in 65 nm CMOS technology has been developed.

8.1 Thesis Highlights

First, we provided a novel methodology for analyzing the advantageous decoding performance of multi-branch configurations of low-bit optical soft-decision forward error correction (SD-FEC) receivers. Three different hardware implementations of an SD-FEC receiver were investigated, and their decoding performance and noise behavior were evaluated and

compared. Arising from a multiple-branch configuration, the concept of inconsistency in the decoder (thermometer code) was presented and used to optimize the decoding performance. The proposed methodology was experimentally evaluated in a short-reach optical link. The evaluation method shows that, in an unamplified link such as a short-reach optical interconnect, using a multi-branch SD-FEC receiver configuration degrades the overall soft-decision decoding performance in comparison with the hard-decision decoding performance. Therefore, the conventional single-branch SD-FEC receiver is more appropriate for such applications. The hybrid fan-out configuration is a low-complex and power-efficient approach for optically amplified application with the dominant channel noise [27].

Second, we experimentally demonstrated a design optimization of an evanescently coupled waveguide germanium-on-silicon photodetector (Ge-PD) toward high-speed (>30 Gb/s) applications. The resulting PD provides a responsivity of 1.09 A/W at 1550 nm, a dark current of 3.5 μA, and bandwidth of 42.5 GHz at 2 V reverse-bias voltage. For optimizing the PD, the impact of various design parameters on performance was investigated. A novel optimization methodology for the PD's responsivity based on the required bandwidth was developed. The responsivity of the PD is enhanced by enlarging its geometry and using off-centered contacts on top of the germanium, while an integrated peaking inductor mitigates the inherent bandwidth reduction from the responsivity optimization. The performance of the optimized PD and the conventional, smaller size non-optimized PD was compared to validate the optimization methodology. The sensitivity of the optimized PD improves by 3.2 dB over a smaller size non-optimized PD. Further discussion on the impact of top metal contacts on the photodetector's performance was also presented through simulation and measurement.

Third, we demonstrated the design, fabrication, and measurement results of a novel lateral p-i-n silicon photodetector (Si-PD) in a silicon-on-insulator (SOI) platform for 850 nm wavelength. In the proposed photodetector, the incident light is directed hor-

izontally using a grating coupler, thus significantly increasing optical absorption in the depletion area thereby increasing the PD's responsivity. The measurement results show that the grating coupler increases the responsivity by 40 times compared with the Si-PD without a grating coupler. The grating-assisted Si-PD with 5 μm intrinsic width has a responsivity of 0.32 A/W and a dark current of 1 nA at 20 V reverse-bias voltage. Further, it shows an open-eye diagram for 10 Gb/s PRBS-31 non-return-to-zero on–off keying (NRZ-OOK) data and has a 3-dB bandwidth of 4.7 GHz at this bias voltage. Also, the design parameters of three variations of the novel grating-assisted Si-PD for high-speed applications (>25 Gb/s) were presented. The optimized grating-assisted Si-PD uses a focusing grating coupler, and its p-i-n diode has a 0.3 μm intrinsic width. It has a responsivity of 0.3 A/W, an avalanche gain of 6, a dark current of 2 μA, and a 3-dB bandwidth of 16.4 GHz at 14 V reverse-bias voltage. Further, it shows an open-eye diagram of 35 Gb/s PRBS-31 NRZ-OOK data that, to the best of our knowledge, is the fast data rate reported for a Si-PD.

Finally, we presented the design and measurement results of a novel inductor-less and power-efficient 25 Gb/s optical receiver in 65 nm TSMC technology. The proposed receiver front end consists of an inverter-based feedback transimpedance amplifier (TIA) and three stages of an inverter-based Cherry-–Hooper (CH) post-amplifier. To this structure, local positive feedback and third-order interleaved active feedback are added to increase the bandwidth of the front end. The receiver front end has a transimpedance gain of 69.4 dBΩ, a bandwidth of 13.6 GHz, and an input-referred current noise of 3.28 μA_{rms}. It occupies only 0.0056 mm^2 and consumes 30.8 mW at 1.1 V supply voltage. First, the bit error rate (BER) measurement was performed with an electrical input signal. The results show that the proposed front end has a sensitivity of 3.6, 4.5, and 6.4 mV_{p-p} for BER of 10^{-12} at data rates of 20, 25, and 30 Gb/s, respectively. The receiver front end also was measured with supply voltages lower than 1.1 V. The measurement results show that, for BER of

10^{-12} and an input sensitivity of 5 mV_{p-p}, the receiver front end has energy efficiencies of 0.425 and 0.8 pJ/bit at data rates of 20 and 25 Gb/s, for supply voltages of 0.85 and 1 V, respectively. Next, the optical receiver is prototyped with the optimized grating-assisted Si-PD. The receiver with a wire-bonded Si-PD has a sensitivity of 46 μA_{p-p} and 54 μA_{p-p} at data rates of 20 and 25 Gb/s, respectively, at a reverse-bias voltage of 0.41 V. The energy efficiency of the all-silicon 850 nm optical receiver is 1.23 pJ/bit at 25 Gb/s data rate.

8.2 Future Work

This section presents several future research directions to extend the work presented in this dissertation.

8.2.1 2-Bit Soft-Decision Forward Error Correction (SD-FEC) Receiver

The proposed methodology shows that in a short-reach optical link, splitting the optical power prior to the receiver degrades the decoding performance considerably. On the other hand, simulation result shows the benefit of the uncorrelated noise in the decoding. Therefore, the electrical fan-out after the TIA and prior to the post-amplifier stages may benefit from the uncorrelated noise of the post-amplifier stages.

Further, investigation on circuit implementation of a power-efficient 2-bit electrical fan-out SD-FEC receiver can be an interesting research direction on this topic. The proposed optical receiver front end presented in Chapter 6 can be used for implementing a 2-bit SD-FEC receiver. Figure 8.1 shows the block diagram of the proposed 2-bit SD-FEC receiver. The output of the receiver front end is connected to three sets of decision circuits that compare the amplified data with a hard-decision threshold level (V_{th0}) and two soft-decision threshold levels (V_{th-1} and V_{th1}). The decision circuits are working with four phases of a clock (CLK1, CLK2, CLK3, and CLK4) at the quarter rate of the received

data rate. Using multi-phase clock reduces the required speed of the decision circuits and relaxes the design requirement. A peak detector and a minimum detector determine the dynamic range of the amplified data. Six variable resistors use the peak and minimum values to generate three digitally tunable threshold levels. The peak value also is used to automatically control the gain of the front end for linear operation.

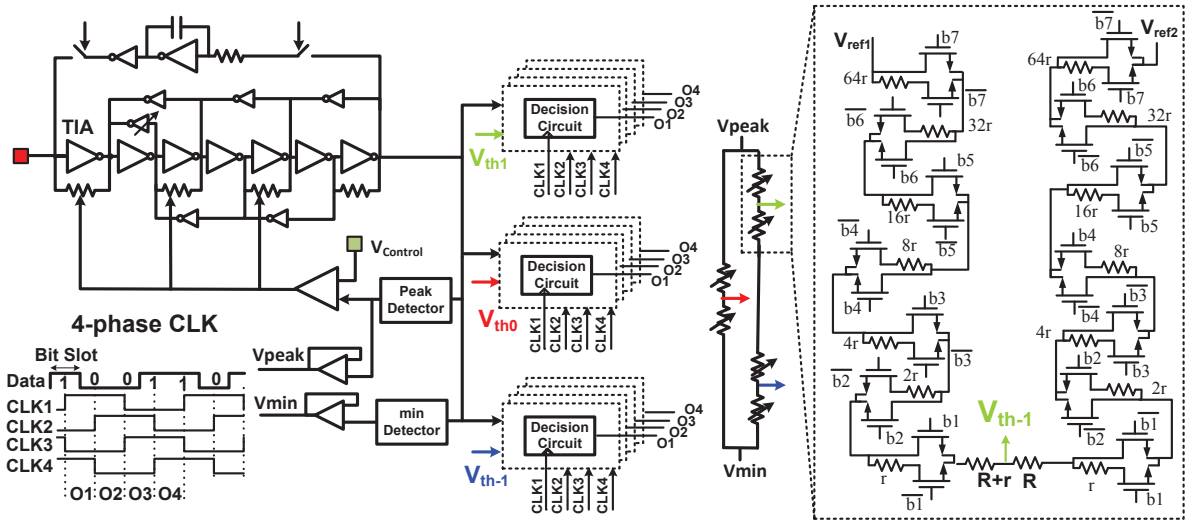


Fig. 8.1 An example of implementing a 2-bit SD-FEC receiver using the proposed optical front and digitally tunable threshold levels.

8.2.2 High Performance Ge-PD

The performance of the Ge-PD can be improved further with some modifications on the fabrication process. For example, if the Ge can grow properly on the 90 nm thick silicon instead of the 220 nm thick silicon, the light couples faster to the Ge and as a result the Ge-PD has larger responsivity for a shorter length detector. Further, the availability of a 0.5 μm minimum feature size of the Ge on the silicon maximizes the detector responsivity by omitting the top metal contact [51–53].

8.2.3 Grating-Assisted Si-PD

The single mode and polarization sensitive grating couplers in the proposed Si-PD results in an optimum responsivity for a single mode and single polarization application. The availability of multi mode grating coupler [117, 118] expands the application of this photodetector.

Another research direction is investigating the design of the proposed grating-assisted Si-PD on an SOI-based CMOS technology that enables monolithically integration of this photodetector with the proposed optical receiver [23, 119]. Monolithic integration improves the performance of the optical receiver by omitting the parasitic capacitors of the bonding pads and the parasitic inductance of the wire bond between the receiver and the photodetector.

8.2.4 Optical Receiver

The proposed inverter-based optical receiver with identical interleaved active feedback shows slightly larger group delay variation in comparison with the conventional inverter-based design. Non-identical interleaved active feedback can be used to minimize the group delay variation of the proposed design.

Further, the proposed optical receiver would be integrated with decision circuits and clock and data recovery circuit. The gain of the optical front-end can be adjusted based on the sensitivity of the integrated decision circuits for more power-efficient design. Also, the proposed optical receiver can be implemented in more advanced technology node such as 45 nm or 28 nm CMOS technology to support faster data rate.

Appendix A

Optical Link Noise Modeling

Here, the noise theory and definitions used in the optical link modeling are discussed. The theory and the models are then used to model the noise statistics (common noise and uncorrelated noise) of each branch of a multiple–branch receiver for various configurations. Three major sources of noise are considered: 1) channel noise, 2) transmitter noise and 3) receiver noise.

Channel noise: In optically amplified long-haul links, the amplified spontaneous emission (ASE) noise of optical amplifiers is the main channel noise. The power spectral density of the ASE noise is calculated by [41]:

$$S_{ASE} = NF_{EDFA}(G_{EDFA} - 1)\frac{hc_0}{2\lambda} \tag{A.1}$$

where NF_{EDFA} and G_{EDFA} are the noise figure and gain of the EDFA amplifier, respectively, h is Planck's constant, c_0 is the light speed in vacuum, and λ is the wavelength of the channel. The channel noise is modeled with two Gaussian distributions at the receiver front-end with standard deviations of $\sigma_{ASE-ASE}$ and $\sigma_{Signal-ASE}$ due to the beating of

ASE-noise with itself and the beating of the signal with ASE-noise, respectively [41].

$$\sigma^2_{ASE-ASE} = 2R^2 S^2_{ASE}[2B_{opt}B_e - B_e^2] \tag{A.2}$$

$$\sigma^2_{Signal-ASE}(i) = 4R^2 S_{ASE} P_{in}(i) B_e \tag{A.3}$$

The standard deviation of $\sigma_{Signal-ASE}(i)$ is data dependent, therefore it is different for received optical power corresponding to a logical zero and one, ($i = 0$ or 1). In equation (A.2) and (A.3), the B_{opt} and B_e are the equivalent rectangular bandwidths of the optical filter and electrical front-end respectively, R is the responsivity of the photodetector, and $P_{in}(i)$ is the received optical power for a logic zero or one ($i = 0$ or 1).

Transmitter noise: Relative intensity noise (RIN) of a semiconductor laser in the transmitter (TX) is the main transmitter noise source. The RIN noise is modeled in the receiver with a Gaussian distribution with a standard deviation σ_{RIN} [41].

$$\sigma^2_{RIN}(i) = RIN_{Hz}(R(P_{in}(i) + S_{ASE}B_{opt}) + I_d)^2 B_e \tag{A.4}$$

where RIN_{Hz} is the maximum value of the laser relative intensity noise (RIN) in dB/Hz and I_d is the dark current of the photodetector. Note that the standard deviation σ_{RIN} is data dependent. Therefore, it is different for received optical power corresponding to a logical zero and one.

Receiver noise: The receiver noise consists of shot noise of the photodetector and thermal noise of the load resistance of the photodetector with standard deviations of σ_{sh} and σ_{th-R_L}, respectively [41]:

$$\sigma^2_{sh}(i) = 2q[R(P_{in}(i) + S_{ASE}B_{opt}) + I_d)]B_e \tag{A.5}$$

$$\sigma^2_{th-R_L} = \frac{4kT}{R_L} B_e \tag{A.6}$$

where q is the electric charge, k is the Boltzmann constant, T is the temperature, R_L is the load resistance of the photodetector. The receiver noise also includes the input referred noise of the electrical post amplifier stages whose effect is calculated with a noise coefficient NF derived by:

$$NF = \frac{\overline{V^2_{n_{out-TIA}}} + \overline{V^2_{n_{input-referred-Amps}}}}{\sigma^2_{th-R_L} A^2_{TIA}} \tag{A.7}$$

where A_{TIA} and $\overline{V^2_{n_{out-TIA}}}$ are the gain and output noise power of the transimpedance amplifier, respectively, and $\overline{V^2_{n_{input-referred-Amps}}}$ is the input referred noise power of the amplifier stages. The coefficient NF is analogous to the noise figure of front-end electrical circuits. It has been modified here for the integrated-circuit implementation of an optical receiver. The standard deviations of the common noise $\sigma_{Common}(i)$, and uncorrelated noise $\sigma_i(i)$, are calculated using (A.8) and (A.9) respectively, for received optical power corresponding to a logical zero and one.

$$\sigma^2_{Common}(i) = \sigma^2_{Signal-ASE}(i) + \sigma^2_{ASE-ASE} + \sigma^2_{RIN}(i) \tag{A.8}$$

$$\sigma^2_i(i) = \sigma^2_{sh}(i) + NF\sigma^2_{th-R_L} \tag{A.9}$$

In a conventional optical receiver, the total noise variance for received optical power corresponding to a logical zero and one is calculated by

$$\sigma^2_I(i) = \sigma^2_{Signal-ASE}(i) + \sigma^2_{ASE-ASE} + \sigma^2_{RIN}(i) + \sigma^2_{sh}(i) + NF\sigma^2_{th-R_L} \tag{A.10}$$

Appendix B

Optimum Hard and Soft Decision Threshold Levels

Choosing the hard-decision threshold is based on a LLR value of zero (shown as the vertical red dashed-line in Fig. 2.2). Due to varying standard deviation of the Gaussian distribution of both the binary logic one and zero, the optimum hard-decision threshold varies with the Q-factor of the received signal. Figure B.1 illustrates the impact of the hard-decision threshold (value is normalized to the mean value of the received signal for logic one) on the pre-FEC BER at various Q-factors as similarly depicted in [120]. The ratio of the standard deviations (σ_1/σ_0) is set to two. The optimum hard-decision threshold changes from 0.453 to 0.414 by increasing the Q-factor of the received signal from 4 dB to 10 dB. A larger standard deviation ratio leads to a greater change in the optimum hard decision thresholds for different Q-factors. Therefore, the hard-decision threshold setting needs to be adjusted to obtain the optimum error performance.

To select the appropriate soft-decision thresholds, one of the soft-decision thresholds is swept while the other is calculated based on the mean and standard deviation of the PDFs assuming that both soft-decision thresholds have the same pre-FEC BER [121].

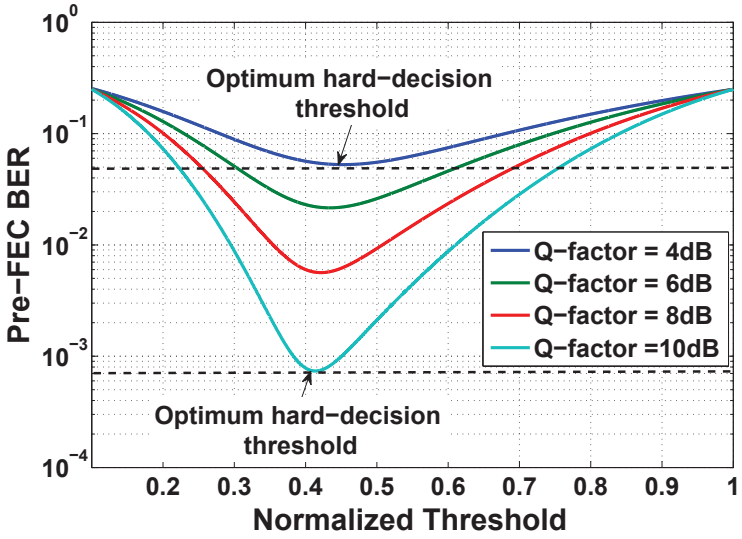


Fig. B.1 The pre-FEC BER for normalized hard-decision thresholds of the two Gaussian distributions for various Q-factors, while the ratio of standard deviation of the binary levels is fixed to $(\sigma_1/\sigma_0) = 2$.

Then, the post-FEC BER is calculated using the soft decoding algorithm. Note that the upper soft-decision threshold is farther in value from the hard-decision value than the lower soft-decision threshold because the variance of logic 1 (σ_1^2) is larger than the variance of logic 0 (σ_0^2). Therefore, the soft-threshold on the upper side should be farther from the hard-threshold to have the same pre-FEC BER compared to the lower soft-threshold [121]. Figure B.2 shows the post-FEC BER as a function of the threshold difference (or threshold distance) between the hard-decision and both soft-decision thresholds. The upper soft-decision threshold is calculated from the lower soft-decision threshold setting based on the statistics of the PDFs. The LDPC (32768, 26803) code and SPA decoding algorithm are used for this simulation, with approximately 6.5×10^7 encoded bits and a Q-factor of 6.7 dB.

To summarize, for each Q-factor, the optimum hard-decision threshold is calculated by eq. 2.5, where the LLR is zero. However, for calculating the optimum soft-decision thresholds, we need to sweep one of the soft-decision thresholds and calculate the post-

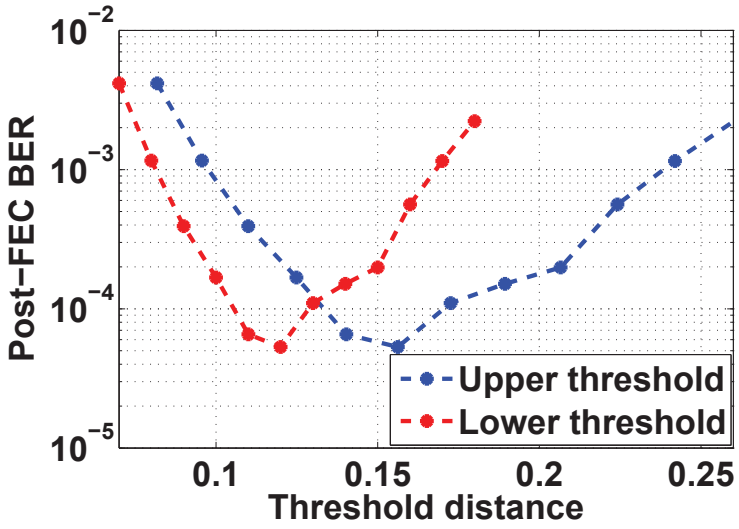


Fig. B.2 Post-FEC BER for various distances of lower soft-decision threshold (red dashed-line). The distance of the upper soft-decision threshold (blue dashed-line) is calculated based on the statistics of the PDFs. The simulation is for optically amplified link with electrical fan-out and Q-factor of 6.7 dB; and the ratio of standard deviation of binary levels is $(\sigma_1/\sigma_0)\approx 2$.

FEC BER. The post-FEC BER is sensitive to the variation of the soft-decision thresholds in the waterfall region of the code rather than in the low Q-factor area with high-BER. Therefore, the threshold sweep is required for Q-factor in the waterfall region.

Appendix C

Calculation of Input-Referred Current Noise

This section presents the calculation of the low frequency input-referred current noise of the proposed receiver (Fig. 6.7). First, we calculate the output noise of our proposed receiver coming from the TIA and three cascaded CH amplifiers. Then, the output noise caused by the interleaved active feedback (IAFB) and positive feedback (PFB) is calculated. A CH amplifier consists of a transconductance stage (G_1) and a transimpedance stage (G_2), which has a similar structure as the input TIA stage. For a transimpedance stage, its output noise is caused by the thermal noise of the feedback resistor (V_{nR}^2) and the thermal noise of the PMOS and NMOS transistors in the inverter (V_{ninv}^2). We used the model illustrated in Fig. C.1 to calculate the output noise of the transimpedance stage due to the feedback resistor and the inverter.

In this figure, Y_L is the output admittance of the transimpedance stage given by $Y_L = g_{ds}+sC_L$. Y_{in} is the input admittance of the transimpedance stage. For the input TIA, $Y_{in} = sC_{in}$, where C_{in} represents the input capacitor of the TIA. For the transimpedance stage in the CH amplifier, $Y_{in} = Y_L$, if all inverters have the same load capacitance and

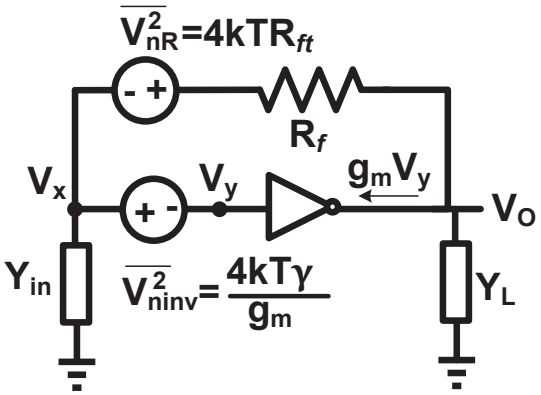


Fig. C.1 Block diagram for calculating the output noise of a transimpedance stage.

output conductance. The relation between the output noise of the transimpedance stage and the thermal noise of the feedback resistor along with the thermal noise of the inverter is calculated by

$$V_{no} = V_{nR}\frac{g_m + Y_{in}}{g_m + Y_{in} + Y_L + Y_{in}Y_L R_f} + V_{ninv}\frac{g_m(1 + Y_{in}R_f)}{g_m + Y_{in} + Y_L + Y_{in}Y_L R_f} \tag{C.1}$$

Assuming that $g_m \gg g_{ds}$ and $g_m \gg g_{ds}^2 R_f$, the low frequency noise at the output of the transimpedance stage is obtained by

$$\overline{V_{no}^2} = \overline{V_{nR}^2} + \overline{V_{ninv}^2} = \overline{V_{nR}^2} + \frac{\overline{I_{ninv}^2}}{g_m^2} \tag{C.2}$$

where $\overline{I_{ninv}^2}$=4kTγg_m. Note that at low frequency, the feedback resistors in the TIA and the transimpedance stage in the CH amplifier reduce both input and output resistances of the TIA to approximately $1/g_m$. Therefore, the output noise of the transconductance stage G_1 is given by

$$\overline{V_{no-G1}^2} = \frac{\overline{I_{ninv1}^2}}{g_{m2}^2} \tag{C.3}$$

The total output noise due to the TIA and three cascaded CH amplifiers in the proposed design shown in Fig. 6.7 is obtained by

$$\begin{aligned}\overline{V^2_{n-out(TIA+CH)}} &= \left(\frac{1}{1+5\beta A_1A_2 - A_1\alpha + 3A_1^2A_2^2\beta^2 - 3A_1^2A_2\alpha\beta}\right)^2 \\ &\times \left(\begin{array}{l}\left(\overline{V^2_{nRt}} + \frac{\overline{I^2_{ninv}}}{g^2_{mt}}\right)A_1^6A_2^6 \\ +\frac{\overline{I^2_{ninv1}}}{g^2_{m1}}\left(A_1^4A_2^6 + A_1^2A_2^4 + A_2^2\right) \\ +\left(\overline{V^2_{nR}} + \frac{\overline{I^2_{ninv2}}}{g^2_{m2}}\right)\left(A_1^4A_2^4 + A_1^2A_2^2 + 1\right)\end{array}\right)\end{aligned} \tag{C.4}$$

The low frequency input-referred current noise of the proposed receiver due to the TIA and three cascaded CH amplifiers is calculated by

$$\overline{I^2_{n-in(TIA+CH)}} = \frac{\overline{V^2_{n-out(TIA+CH)}}}{R_T^2} \tag{C.5}$$

Assuming that $g_{mt} = g_{m2} = g_{m1} = g_m$, which results in $A_1 = g_{m1}/g_{m2} = 1$, the input-referred current noise caused by the TIA and CH amplifier is given by

$$\begin{aligned}\overline{I^2_{n-in(TIA+CH)}} &= \frac{\overline{V^2_{nRt}}}{A^2_{tia}} + \frac{\overline{V^2_{nR}}}{A^2_{tia}}\left(\frac{1}{A_2^2} + \frac{1}{A_2^4} + \frac{1}{A_2^6}\right) \\ &+ \frac{\overline{I^2_{ninv}}}{A^2_{tia}g_m^2}\left(2 + \frac{2}{A_2^2} + \frac{2}{A_2^4} + \frac{1}{A_2^6}\right)\end{aligned} \tag{C.6}$$

From the equation (C.6), we see that the feedback inverters (G_f, G_{PFB}) do not affect the low frequency input-referred noise caused by the TIA and CH amplifiers. More precisely, the low frequency noise contribution of the TIA and CH stages to the input-referred noise of the receiver with IAFB and PFB is the same as the receiver without IAFB and PFB. If $g_{mt}R_t \gg 1$, the TIA gain $A_{tia} \approx R_t$, also if $A_2 \gg 1$ (in our design $A_2 \approx 3$) the equation can be

simplified to

$$\overline{I^2_{n-in(TIA+CH)}} = \frac{4kT}{R_t} + \frac{8kT\gamma}{R_t^2 g_m} \tag{C.7}$$

The first term in the above question is the current noise of the TIA's feedback resistor, which directly appears in the input-referred current noise and has the dominant effect. The second dominant part is related to the thermal noise of the inverters in the TIA and the transconductance stage of the first CH amplifier. Next, the noise contribution of several feedbacks to the input-referred current noise is calculated. The thermal noise current injected into the outputs of the IAFB and the PFB are given by

$$\begin{aligned} \overline{I^2_{n_I AFB}} &= 4kT\gamma g_{mf} \\ \overline{I^2_{n-PFB}} &= 4kT\gamma g_{m-PFB} \end{aligned} \tag{C.8}$$

Note that at low frequency, the feedback resistors in the TIA and the TIA portions of the CH amplifiers reduce both input and output resistances of the TIA to approximately $1/g_m$. Therefore, the output noise of the of feedback inverters G_f and the G_PFB inverter are given by

$$\begin{aligned} \overline{V^2_{no-Gf}} &= \frac{\overline{I^2_{n-IAFB}}}{g^2_{m2}} \\ \overline{V^2_{no-GPFB}} &= \frac{\overline{I^2_{n-PFB}}}{g^2_{mt}} \end{aligned} \tag{C.9}$$

The low frequency output noise of the receiver due to the IAFB and the PFB is obtained

by

$$\begin{aligned}\overline{V^2_{n-out(IAFB+PFB)}} &= \left(\frac{1}{1+5\beta A_1A_2 - A_1\alpha + 3A_1^2A_2^2\beta^2 - 3A_1^2A_2\alpha\beta}\right)^2 \\ &\times \left(\begin{array}{l}\left(\frac{\overline{I^2_{n-PFB}}}{g^2_{mt}} + \frac{\overline{I^2_{n-IAFB}}}{g^2_{mt}}\right)A_1^6A_2^6 \\ +\frac{\overline{I^2_{n-IAFB}}}{g^2_{m2}}\left(A_1^4A_2^6 + A_1^4A_2^4 + A_2^2A_2^4 + A_1^2A_2^2\right)\end{array}\right)\end{aligned} \tag{C.10}$$

The input-referred current noise PSD is calculated by dividing the output noise PSD by the square of the transimpedance gain. Assuming that $g_{mt} = g_{m2} = g_{m1} = g_m$, then $A_1 = g_{m1}/g_{m2} = 1$. The input-referred current noise caused by the IAFB and PFB is calculated by

$$\overline{I^2_{n-in(IAFB+PFB)}} = \frac{\overline{I^2_{n-PFB}}}{A^2_{tia}g^2_mA^6_2}A_2^6 + \frac{\overline{I^2_{n-IAFB}}}{A^2_{tia}g^2_mA^6_2}\left(A_2^6 + A_2^6 + A_2^4 + A_2^4 + A_2^2\right) \tag{C.11}$$

The three first terms in the above equation, which are related to PFB and the two left-most IAFB have the largest contribution to the input-referred noise of the receiver. By substituting β=g_{mf}/g_m and α=g_{m-PFB}/g_m, the equation can be simplified to:

$$\overline{I^2_{n-in(IAFB+PFB)}} = \frac{4kT\gamma}{A^2_{tia}g^2_m}\left(\alpha + \beta\left(2 + \frac{2}{A_2^2} + \frac{1}{A_2^4}\right)\right) \tag{C.12}$$

Assuming that γ=1, the ratio of the input referred-noise due to the IAFB and PFB over the input referred-noise due to the TIA and CH amplifiers is obtained by

$$\frac{\overline{I^2_{n-in(IAFB+PFB)}}}{\overline{I^2_{n-in(TIA+CH)}}} = \frac{\frac{1}{g_m}\left(\alpha + \beta\left(2 + \frac{2}{A_2^2} + \frac{1}{A_2^4}\right)\right)}{R_t + R_f\left(\frac{1}{A_2^2} + \frac{1}{A_2^4} + \frac{1}{A_2^6}\right) + \frac{1}{g_m}\left(2 + \frac{2}{A_2^2} + \frac{2}{A_2^4} + \frac{1}{A_2^4}\right)} \tag{C.13}$$

In our design α= 0.064, β= 0.16, g_m≈40 m℧, Rt=300 Ω, Rf=215.5 Ω, and A_2≈3, which results in a ratio of 0.0197. Assuming that $A_2 \gg 1$, the ratio is simplified to:

$$\frac{\overline{I^2_{n-in(IAFB+PFB)}}}{\overline{I^2_{n-in(TIA+CH)}}} = \frac{\alpha + 2\beta}{g_m R_t + 2} \tag{C.14}$$

Equations (C.13) and (C.14) show that the low-frequency noise density of the receiver is only slightly increased using the proposed combination of active feedback.

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