Dual Two-Level and Three-Level Inverter Topologies: Modulation and Control Strategies

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Abstract

As the proliferation of electric vehicles becomes more prevalent in the transportation sector, power electronic traction inverters used in these systems have been critically evaluated. With the thrust on improving inverter efficiency, reliability and reduced passive components, different variants of inverter topologies have been previously proposed and investigated. Amongst them, dual inverter topologies represent an emerging trend that has experienced growth. This thesis investigates the modulation and control strategies of dual inverter topologies using conventional two-level and three-level T-type voltage-source converters for traction applications.

The thesis includes an overview of firstly, the different variants of traction inverter topologies along with the advantages and disadvantages associated with them. The advantages and research potential of the dual inverter topology is considered. Secondly, an interleaved modulation strategy for the dual two-level inverter topology is discussed which improves the performance of the passive DC-link capacitor of the inverters. Thirdly, a dual three-level T-type inverter topology is proposed which reduces the DC-link capacitor voltage balancing problem associated with a conventional three-level inverter. Additionally, the topology decouples modulation strategies to reduce switching losses from voltage balancing strategies.

Moreover, three different modulation strategies for three-level inverters are proposed. Firstly, a discontinuous modulation strategy is presented which improves loss and thermal distribution of the three-level T-type inverter switching devices at lower modulation indices. The strategy entails the inverter to increase its current throughput around 30% or utilize up to 35% higher switching frequency. Secondly, a three-level generalized discontinuous modulation algorithm is proposed which enables around 50% switching loss reduction at all operating power factors. Thirdly, sub-fundamental cycle current ripple of a three-level inverter is analyzed and a variable switching frequency strategy is presented which helps in 10-20% inverter switching loss reduction.

Résumé

Avec l'augmentation du nombre de véhicules électriques dans le domaine de l'automobile, les onduleurs électroniques de traction utilisés doivent être évalués de façon critique, l'emphase étant mise sur l'augmentation de l'efficacité de l'onduleur, de sa fiabilité, et la réduction du volume du condensateur du bus continu. Différentes topologies d'onduleurs ont déjà été proposées et étudiées. Parmi ces variantes, les topologies à deux onduleurs branchés au même bus continu représentent une nouvelle tendance et leur utilisation est en croissance. Cette thèse étudie les stratégies de modulation et de contrôle des topologies à deux onduleurs utilisant des convertisseurs classiques à deux niveaux et à trois niveaux de type T dans des applications en traction électrique.

Cette thèse présente d'abord une vue d'ensemble des différentes variantes de topologies de l'onduleur de traction ainsi que leurs avantages et inconvénients. Les points forts et le potentiel de recherche des topologies avec deux onduleurs sont notamment discutés. Deuxièmement, une stratégie de modulation entrelacée pour la topologie à double onduleur à deux niveaux est décrite. Elle permet d'améliorer la performance du condensateur de bus continu. Troisièmement, une topologie à deux onduleurs à trois niveaux de type T est proposée. Elle réduit les exigences d'équilibrage de la tension des condensateurs du bus continu associé à un onduleur à trois niveaux classiques. De plus, cette topologie découple les stratégies de modulation afin de réduire les pertes de commutation liée à l'équilibrage de la tension des condensateurs du bus.

Trois différentes stratégies de modulation pour les onduleurs à trois niveaux sont également proposées. Premièrement, une stratégie de modulation discontinue est présentée, qui réduit les pertes et améliore la répartition de la perte et de la température de la jonction des interrupteurs de l'onduleur à trois niveaux de type T à des profondeurs de modulation faibles. Cette stratégie permet une augmentation d'environ 30 % de la puissance de sortie de l'onduleur, ou une augmentation jusqu'à 35 % de la fréquence de commutation. Deuxièmement, un algorithme généralisé de modulation discontinue est proposé, qui permet une diminution

d’environ 50 % des pertes de commutation à tous les facteurs de puissance. Troisièmement, le profil de l’ondulation du courant est analysé et une stratégie de fréquence de commutation variable est présentée, qui contribue à diminution de l’ordre de 10 à 20 % des pertes de commutation.

Acknowledgments

First and foremost, I would like to express my deepest gratitude to my supervisor Prof. Geza Joos for all his guidance, support and advice during my PhD studies. I have learned a lot from his critical thinking, technical knowledge, and precision, enabling me to handle and develop my capabilities as an individual. I am grateful for his expertise and insight without which this thesis could not be framed in the right direction and I wish to get his extended collaboration in my future endeavor.

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I would also like to express my gratitude for the members of TM4 Inc. including Jianhong Xu, Jean-Marc Cyr, Charles Obry, Mohammed Amar, Marco Bolduc, and Remi Raffin for all the assistances and fruitful discussions as part of the Automotive Partnership Canada project. I sincerely thank them to conduct few experiments at the premise of the company. The conducted experiments helped to improve the content of my proposition in the thesis. Additionally, during my PhD studies, TM4 Inc. accepted me as an intern under the MITACS Accelerate internship program which benefitted me to gain knowledge from an industry point of view.

I am extremely grateful to the Department of Electrical Engineering and the Graduate Office for the support, equipment and help I needed to produce and complete my thesis. It's my privilege to collaborate with McGill University for their standard of education, technology and facilities.

Finally, this thesis would not have been possible without the co-operation from my wife Poulami Chakraborty. Her continuous encouragement and support during this journey of good and stressful times kept my spirits high. I also owe sincere thanks to my parents Prabir Kumar Bhattacharyya, Mita Bhattacharyya and my brother Debojyoti Bhattacharjee for their encouragement, patience and faith throughout my life.

"विद्या ददाति विनयं विनयाद्याति पात्रताम् ।
पात्रत्वाद्धनमाप्नोति धनाद्धर्मं ततः सुखम् ॥ ५ ॥"

"Education gives Humility, Humility gives Character, from character one gets wealth, from wealth one gets righteousness, in righteousness there is joy."

Narayana Pandit, Mangalakaranam, Hitopadesa.

Preface

Thesis Format and Style

This thesis is presented in the manuscript based format according to the guidelines of the National Library of Canada. The work presented here is the original work of the candidate. It consists of a set of manuscripts on which the candidate is the lead author.

The thesis explores interleaving PWM techniques for dual two-level and dual three-level inverter topologies; and three improved PWM strategies for the three-level inverters. These contributions have been explored in Chapter 2-6 and connecting statements at the end of each chapter were used to provide links between them. Along with a brief literature survey relevant to the proposed contributions in each of the chapters, the general introduction in Chapter 1 provides the overall rationale and background information about the thesis, thereby creating a cohesive document.

Contributions of the co-authors

During the completion of this doctoral thesis at McGill University, the candidate has received invaluable advices and assistances from his thesis supervisor Prof. Geza Joos and other co-authors – Diego Mascarella (McGill University), Sourabh Kumar Sharma (McGill University), Jean-Marc Cyr (TM4 Inc.) and Jianhong Xu (TM4 Inc.). The co-authors have contributed to the progression of the thesis through technical suggestions, logistical supports, and editorial guidance on the articles. The candidate was, however, the primary contributor figuring out the problem statement, preparing the analytical and experimental results, and writing the thesis along with the corresponding articles.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

A-NPC	Active Neutral Point Clamped
CSF	Constant Switching Frequency
DPWM	Discontinuous Pulse Width Modulation
DPWM2	Discontinuous Pulse Width Modulation Type 2
DPWMA	Discontinuous Pulse Width Modulation A -type
DPWMO	Discontinuous Pulse Width Modulation O -type
DPWM0O	Discontinuous Pulse Width Modulation O -type and 0^{th} number
DPWM1O	Discontinuous Pulse Width Modulation O -type and 1^{st} number
DPWM2O	Discontinuous Pulse Width Modulation O -type and 2^{nd} number
DPWMPN	Discontinuous Pulse Width Modulation PN -type
DPWM0PN	Discontinuous Pulse Width Modulation PN -type and 0^{th} number
DPWM1PN	Discontinuous Pulse Width Modulation PN -type and 1^{st} number
DPWM2PN	Discontinuous Pulse Width Modulation PN -type and 2^{nd} number
DPWMLPFj	Discontinuous Pulse Width Modulation Low Power Factor type j
EIF	Efficiency Improvement Factor
EV	Electric Vehicle
ESR	Equivalent Series Resistance
GDPWMO	Generalized DPWMO
IM	Induction Motor
IPM	Interior Permanent Magnet Motor (also IPMSM)
IGBT	Insulated Gate Bipolar Transistor
LUT	Look Up Table
NPC	Neutral Point Clamped
NPP	Neutral Point Piloted
PWM	Pulse-Width Modulation
PMSM	Permanent Magnet Synchronous Motor
RMS	Root Mean Square
SynRM	Synchronous Reluctance Motor
SLF	Switching Loss Function
SPWM	Sine Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
SM-PMSM	Surface Mounted PMSM
T-NPC	T-type Neutral Point Clamped
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

List of Symbols

α	Clamping angle
β	Interleaving angle
Δi_{dqj}	d-q axis current error of j^{th} inverter
Δv_{dqE}	d-q axis equalizing voltage
ΔI_{max}	Maximum ripple at a modulation index
Δf_{sw-nom}	Nominal change in switching frequency
$\Delta f_{sw-coeff}$	Change in switching frequency coefficient
$f_i(\theta)$	Absolute current to be switched
f_{sw}	Switching frequency
$f_{sw-operating}$	Operating switching frequency
$f_{sw-base}$	Base switching frequency
i_{inv}	Inverter input current
i_{cap}	DC-link capacitor current
i_{bat}	Battery current
i_{line}	Line current (inverter output current)
i_{pos}	Current through positive DC bus
i_{neg}	Current through negative DC bus
$i_{neutral}$	Current through neutral DC bus
i_{dj}	d-axis inverter output current for j^{th} inverter
i_{dqref}	dq-axis reference current
i_{qj}	q-axis inverter output current for j^{th} inverter
I_{dc}	DC link current
$\overrightarrow{\Delta I}$	Current ripple
I_{nj}	Harmonic component associated with n^{th} harmonic of j^{th} inverter
I_{RMS}	RMS current
k	Switching frequency adjustment coefficient
k_{pj}	j^{th} proportional constant
k_{pE}	Proportional constant of equalizing block
k_{Ij}	j^{th} integral constant
k_{IE}	Integral constant of equalizing block
K_T	Torque constant
λ_f	Back-emf constant
L	Inductance
m	Modulation index
n	Number of harmonic
P_{av}	Average switching loss
Ω	Measured speed
Ω_{red}	Reference speed
ϕ	Flux

φ	Displacement Power factor angle
φ_v	Angle of space vector
pf	Power factor
R	Resistance
θ	Angle of duration of stay in one subsector
θ_{R2}	Duration of stay in sector in subsector 2 form<0.577
θ_{R3}	Duration of stay in sector in subsector 2 form>0.577
θ_e	Motor electrical position angle
T	Motor Torque
T_{sw}	Time period
V_{dc}	DC link voltage
V_{abc}	abc phase voltage
V_{ph}	Phase voltage
$\overrightarrow{\Delta V_{ref}}$	Reference space phasor
$\overrightarrow{\Delta V_1}$	Actual space phasor
V_{line}	Line-to-line voltage
V_{dqref}	d-q axis reference voltage

1 Introduction

The background and the research questions that are addressed in the thesis are presented in this section. A brief review of the early research is described and the technical contributions of the thesis are listed. Finally, the chapter outlines and major results are presented.

1.1 Background

Traction motors are high power electric motors that are an essential part of the Electric Vehicles (EVs) [1]. Since they must be fed with three-phase AC voltage that is not readily available in an EV, power converters consisting of power semiconductor devices, energy storage elements and control circuitry are needed to interface energy storage elements for instance batteries to power the traction motor. These power electronic converters and their individual functions define the overall EV system performance, in terms of power conversion efficiency, power density as well as the voltage and current waveform quality [2]. Active power semiconductor devices such as Insulated Gate Bipolar Transistors (IGBTs) implemented in power converters are made to operate as ON/OFF switches which are either fully ON or fully OFF other than during switching state transitions [3]. These switches along with passive elements such as diodes, inductors, capacitors can be implemented in various converter structure configurations commonly referred in literature as topologies.

Inverter topologies are used in applications where it is required to convert DC voltage from a power source (e.g. a battery) to an AC voltage that can be fed to a motor. They do so by using their switching devices to convert the DC input voltage into waveforms that consist of appropriately placed rectangular pulses of varying widths and of either polarity. The waveforms contain a fundamental AC component and other less dominant AC harmonics [4]. The topologies can be classified in terms of – (i) number of output AC line voltage levels they produce (e.g. two-level, three-level, multilevel inverter), and (ii) the DC-link configuration on the DC side of the inverter – voltage source when a DC voltage source or capacitor is placed across the inverter,

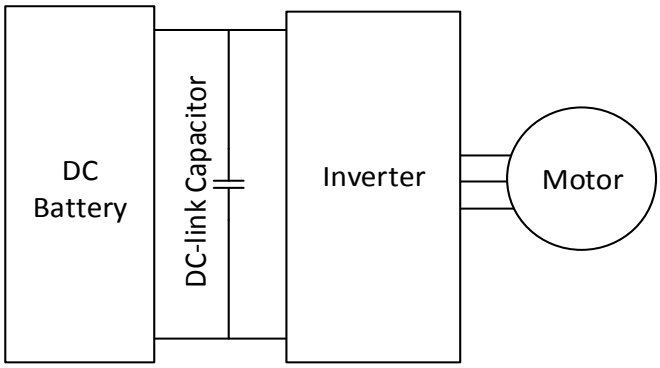


Figure 1-1: A generic diagram showing Inverter fed Motor drive from a DC battery

current-source if an inductor is placed across the inverter [5]. A generic diagram of the inverter-fed motor drive topology is shown in Fig. 1-1.

In EV traction drive applications, the inverters need to be controlled in accordance with the specific needs of the EV traction drive [6]. An automotive inverter typically operates with a wide output voltage range due to volatility in the drive cycle. They may also need to provide higher reactive power depending on the type of motors used. Moreover, they also have a space constraint which puts limits on the maximum cooling capability and size of passive components of inverters. The losses incurred by the inverters cause the system to curtail the theoretical power throughput of the drive, and the higher ripple current through the passive DC-link capacitor requires an oversized design. To avoid this, an automotive inverter should be controlled such that losses incurred by the switching devices reduce over its entire operating range, and the ripple current through its passive components reduce, hence enabling a smaller footprint.

Dual inverter fed dual motor topologies, schematically shown in Fig. 1-2, have been introduced [7] – [9]. The type of inverter used in these include both two-level and three-level inverters, and the dual motor topology includes various configurations of two sets of three-phase motor windings. Earlier works on applications of dual inverter topology in EV applications focused on increasing power throughput of the drive and fault tolerance strategies due to the presence of two drive systems. What makes these dual inverter topologies even more interesting is that the operation of one of the inverter impacts the other one due to their interaction through either of the common DC-link and motor topologies, or both. Hence, it allows a research into the issues of the individual inverter topologies and their solutions using the dual inverter topologies.

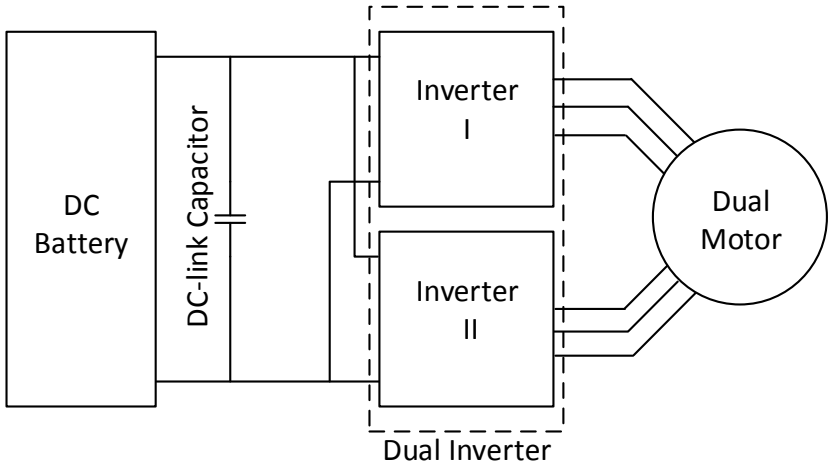


Figure 1-2: Dual Inverter Dual Motor topology

1.2 Thesis Rationale & Problem Statement

Due to the volatility of the drive cycles associated with the EV application, the switching devices of the inverters typically operate over a wide range of modulation index, defined as the ratio of the maximum output line voltage to the DC-link voltage. For example, for operation with Highway-Fuel-Economy-Test (HWFET) or Urban-Dynamometer-Driving-Schedule (UDDS) driving cycles, the inverter would operate over the entire modulation index range with the average modulation index magnitude around 0.3-0.5 [123]. Moreover, EV traction drives utilizing interior permanent magnet synchronous motors [125] and synchronous reluctance motors [127] would need to provide a larger amount of reactive power during steady state and transient conditions, thus operating with a lower power factor. Although the automotive inverters are designed for maximum speed/loading conditions, the control strategies of single and dual inverter topologies need to be readdressed appropriately for a wider operating modulation indices and power factors for optimum performance.

As discussed in the previous section, the dual inverter topology allows a research into the issues of the individual inverter topologies it uses, their behaviors as well as possible solutions using the dual inverter topology. This is addressed in this thesis with the objective of designing appropriate control strategies for dual two-level and dual three-level inverter topologies. The strategies look at the following issues – (i) the DC-link capacitor RMS ripple current of two as well as three-level inverters, and (ii) the unbalance in the split DC-link capacitor voltages of a three-

level inverter. The strategies then look at how we can reduce these metrics in comparison to the single two-level and three-level inverter topologies over a wide operating range.

Furthermore, in comparison to the more conventional two-level topologies, the three-level topologies provide more number of switching states which allows research into different control strategies. In addition, due to the higher number of switching devices and associated switching states- (i) the three-level inverters suffer from unequal loss distribution amongst its switching devices, and (ii) the output waveform ripple profile changes from a two-level topology. The specific problems that will be addressed in this thesis include: Which modulation and control strategies for a three-level inverter we can develop such that – (i) the device losses get redistributed more evenly amongst the devices, (ii) the switching losses reduce over the entire power factor range, and how the sub-fundamental output current ripple profile changes over the entire modulation index range as well as its associated application in deciding the operating switching frequency of a three-level inverter.

1.3 Literature Review

In this section, several inverter topologies were reviewed to assess the relative merits and demerits of the earlier work. While doing so, various inverter topologies working with single three-phase motors or dual motors have been looked at. Furthermore, the conventional inverter control strategies and their operational constraints are also studied.

The inverter topologies, which have been primarily investigated for EV traction drives, are shown in Fig. 1-3 and Fig. 1-4. The conventional two-level and different variants of three-level inverter topologies along with their modulation strategies have been reported. The use of these topologies in dual inverter topologies, shown in Fig. 1-7, has also been reviewed. The following sections describe both the merits and demerits of these topologies.

1.3.1 Two-Level Inverter

The two-level inverter topology, as shown in Fig. 1-3, is conventionally used in the EV traction drive system. The control strategies used by these inverters to convert DC voltage into 3-phase AC voltage are based on pulse-width modulation (PWM). With PWM, an inverter is

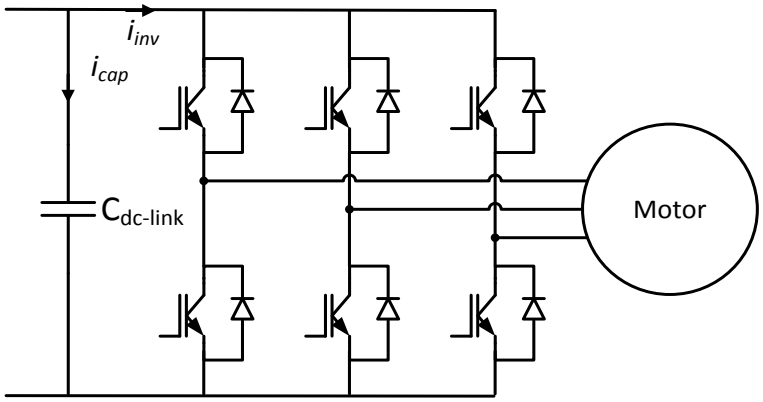


Figure 1-3. Conventional 2-level VSI and motor

controlled based on the width, time-instants and frequency of the ON/OFF signal pulses that are fed to the gates of the inverter's switching devices. This topology has six IGBT-diode pair, and has highest switch-utilization (defined as the ratio of maximum output power to the maximum installed capacity of the inverter) [4] and lowest conduction loss amongst all inverters.

Different PWM strategies of two-level inverters have been provided in [10]- [12]. These are: (i) Sine-PWM (SPWM) [10], (ii) Space Vector PWM (SVPWM) [11], and (iii) discontinuous PWM (DPWM) [12] strategies. Amongst them, the space vector PWM and its DPWM variants are mainly used because it provides maximum DC-link utilization of a two-level inverter. Moreover, the DPWM strategies help to reduce the switching losses of the inverter as it prohibits any switching instance for one-third of a fundamental cycle for each phase.

The two-level inverters have the following limitations [13]:

i. The inverter generates high frequency ripple currents at its dc-link input [14] due to device switching. This input ripple current amounts to approximately 30-60% of the rated load current. The DC-link capacitors handle this high frequency ripple current content, resulting in losses. At high operating temperatures, 50°-120° C, typical of an automotive system, the capacitor ripple current capability greatly reduces. This requires the traction drive to use an oversized capacitor, thus increasing the cost and weight of the drive [15].
ii. Two-level inverter fed traction drives do not have fault-tolerance capability. If there is any fault in the inverter, especially if an EV is in motion, then the result can be very serious [16].

Several variations of conventional PWM schemes and strategies have been proposed in [18]- [37] to reduce input DC current ripple and switching loss in two-level VSIs, including:

i. In [29] - [36], modified PWM strategies were presented that reduced DC-link capacitor ripple. However, these strategies also introduced additional output current ripple.

ii. In [18] - [29], several discontinuous PWM strategies have been discussed which reduces inverter switching losses. However, their uses on a dual inverter topology while reducing the DC-link capacitor ripple content has not been adequately addressed.

From all these previous works, it is understood that the two-level inverter fed EV-traction drives have room for improvement, thus encouraging to explore other inverter topologies which are more beneficial for the system. Subsequently, the three-level inverter topologies were investigated for EV traction drive systems. As shown in Fig. 1-4(i-iii), there are three variants that have been investigated extensively. These topologies have been assessed in the following section.

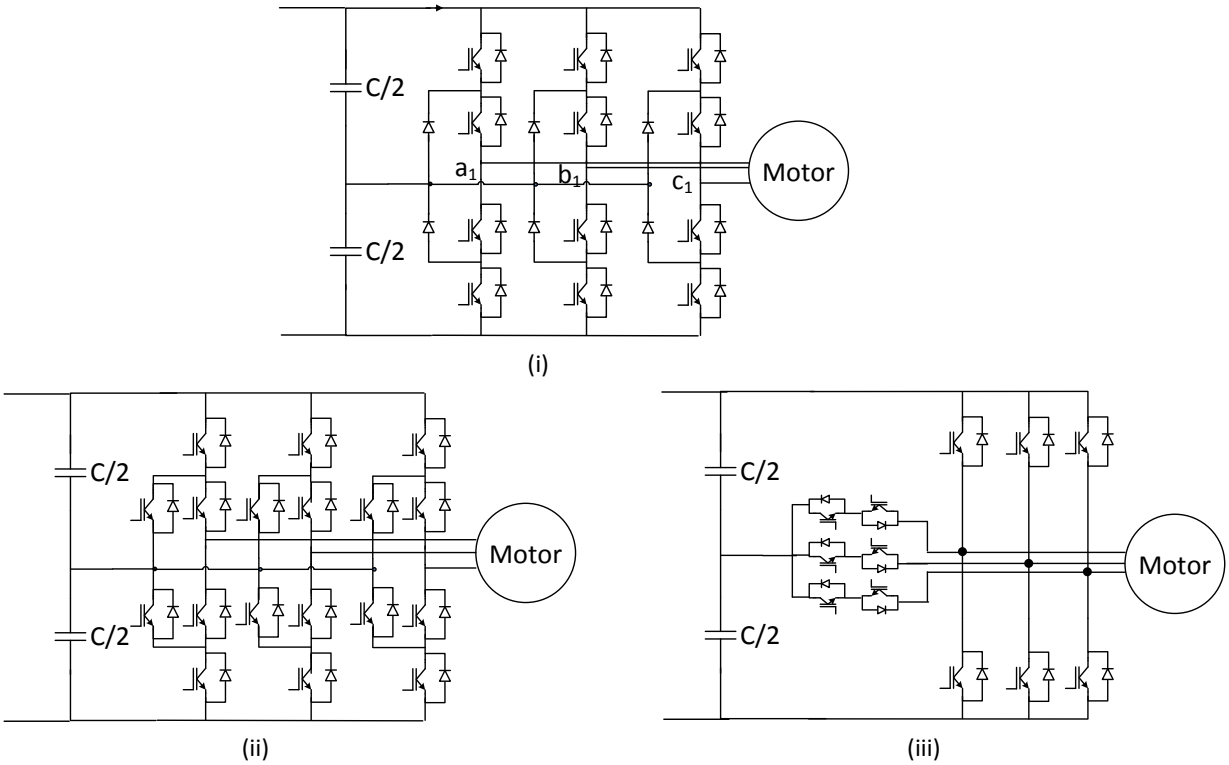


Figure 1-4: (i) NPC inverter (ii) A-NPC inverter (iii) T-NPC Inverter

1.3.2 Three-Level Inverter

The three-level inverters, as shown in Fig. 1-4(i-iii), use a split-capacitor arrangement at their DC-link [38]. Instead of being exposed to the full DC-link voltage as in a two-level VSI, a switch in a three-level inverter is exposed to half the DC-link voltage. So, it can be theoretically implemented with lower voltage rated switches. Alternatively, a higher power rated traction drive can be achieved using a three-level NPC converter by doubling the DC-link voltage of the system if the switches are operated with the same peak voltage stress as those in a two-level inverter.

It should be noted that the presence of the additional switches in these topologies allows for additional control options. Individual switches can be turned ON and OFF less frequently than those in a two-level VSI, so that they are less stressed (and can incur lower switching losses as it is also exposed to lower voltages [39]) while resulting comparable output AC voltage waveform. Alternatively, a better output current waveform can be achieved while using similar switching frequency as of a two level VSI.

The equivalent representation of a three-phase three-level inverter is shown in Fig. 1-5(i). A single three level inverter can produce three different possible voltages: $\frac{-V_{dc}}{2}, 0, \frac{V_{dc}}{2}$ at each phase. The switch positions of the three-level inverter are now described using the nomenclature $v_a, v_b, v_c \in \{N, O, P\}$. Each variable corresponds to one phase of the inverter, and the values N, O, P correspond to the phase potentials $\frac{-V_{dc}}{2}, 0, \frac{V_{dc}}{2}$ respectively [39].

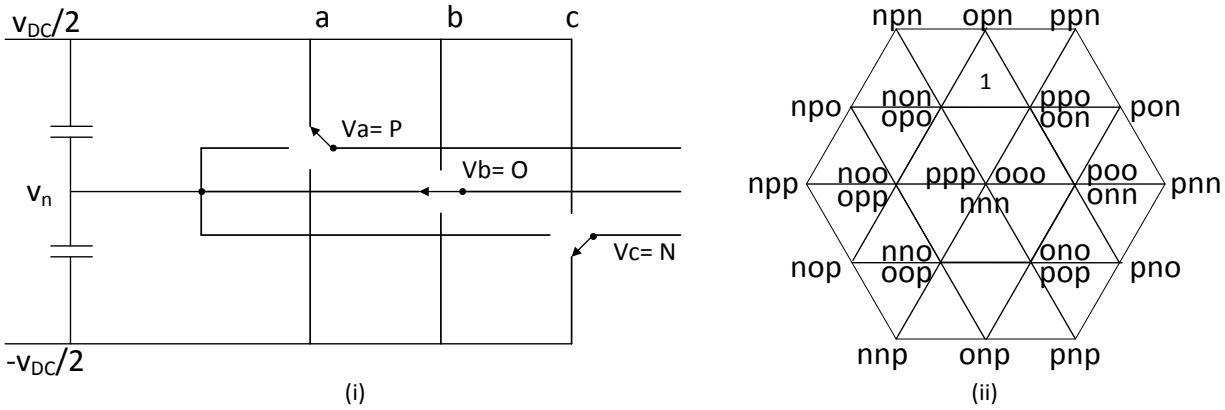


Figure 1-5: (i) Three-level Inverter operation, (ii) Three-level Inverter switching vectors

There exist 27 different vectors of the form $v_{abc} = [v_a\ v_b\ v_c]^T$. They are mapped onto an orthogonal plane as shown in Fig. 1-5 (ii). These voltage vectors can be divided in four groups: six long vectors forming the outer hexagon, six vectors of medium length, twelve short vectors spanning the inner hexagon and three zero vectors. The twelve short vectors form six pairs. The zero vectors correspond to the switch combinations (PPP), (NNN) and (OOO).

The primary variant of the three-level inverter topology is the Neutral point clamped topology. Other two topologies have been investigated to introduce several topological and operational changes to improve the performance of the primary variant.

1.3.2.1 Neutral Point Clamped (NPC) Inverter

The neutral point clamped inverter, as shown in Fig. 1-4(i), has four active switches along with four antiparallel diodes and two diodes which are connected to the neutral point of the DC-link, in one phase leg [38]- [40]. Thus, as discussed before, theoretically it can use lower voltage switches, which reduces switching losses substantially. Also, due to the use of four switches, the individual devices of the NPC inverter switches less frequently than a two-level inverter, while resulting comparable output AC voltage waveform. This characteristic also improves the efficiency of the inverter topology.

However, along with the advantages, it has been found that NPC inverters have several drawbacks, including the following [41] - [50]:

i. Sophisticated PWM methods are needed to balance the voltage across the DC-link capacitors. [41]- [42]. Appendix I provides an analysis of capacitor current which shall be used in this thesis.
ii. This introduces additional switching instances, increasing switching losses by 10-15% [43]-[44]. On the other hand, the use of sophisticated switching schemes to reduce switching losses effects capacitor balancing problem [48] - [50].
iii. There is an uneven loss distribution among the different inverter switches as – (i) in the lower modulation indices the uppermost and the lowermost switch in one leg operate less frequently than the two middle switches [40], [51], and (ii) at higher modulation indices the uppermost and the lowermost switch in one leg operate more frequently.

The other two three-level inverter variants also suffer from unbalanced DC-link capacitor voltages in a similar manner. The capacitor balancing schemes, which have been tried on NPC inverters, are equally applicable for the other two variants, more so for the T-type NPC inverters, due to similar voltage vectors, as shown in Fig. 1-5(ii). Nevertheless, the other two variants have their own traits, as following:

1.3.2.2 Active Neutral Point Clamped (A-NPC) Inverter

This topology was introduced to improve the unequal loss distribution of the NPC inverter. Comparing Fig. 1-4(i) with Fig. 1-4(ii), the single diodes of the NPC inverters have been replaced by active switches in the Active NPC inverter. This configuration provides the following advantages [51], [53] - [56]:

i. These extra switches provide additional paths for the current flowing in and out of the DC-link midpoint so that the current through each switch can be more similar. The difference in switching transitions can be seen from Fig. 1-6. It shows that, in NPC inverter,

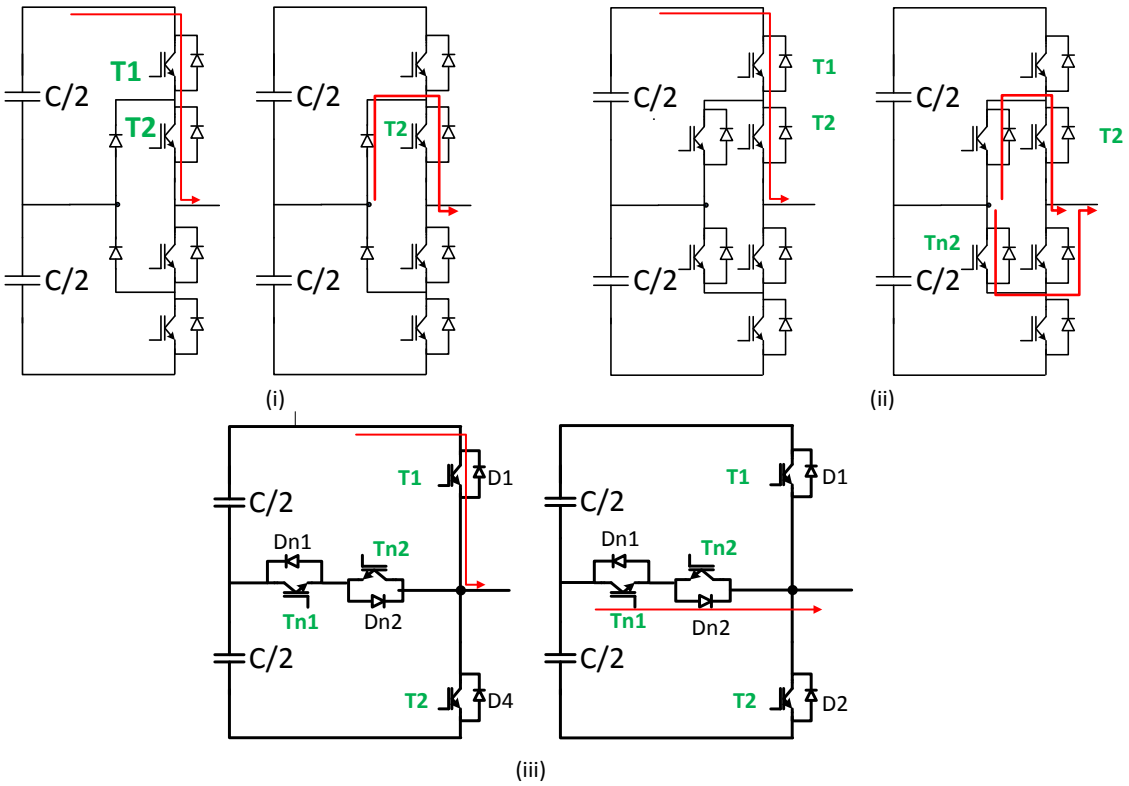


Figure 1-6: Inverter Switching Transitions (P to O) (i) NPC Inverter, (ii) A-NPC Inverter, (iii) T-NPC Inverter

the neutral point current, in one direction can only flow through the one diode; while in A-NPC inverter, the circuit provides two separate paths for the neutral current to flow.

ii. This helps in distributing the losses over the switches in an even manner.

iii. The extra switches provide more avenue towards fault-tolerant capability [55].

Although the converter losses are more equally distributed, the topology has the following limitations:

i. The overall inverter efficiency reduces [51] that of the NPC and T-NPC inverters due to use of more number of switches.

ii. It also suffers from DC-link capacitor balancing problem and associated control schemes and related increase in switching losses. Even though it has more number of possibilities to balance the neutral point voltage, more number of switches always introduces more losses in the system [54].

1.3.2.3 T-Type Neutral Point Clamped (T-NPC) Inverter

This inverter consists of a six-switch inverter and six lower voltage-rated switches that are connected to the neutral point of the DC-link (midpoint of the split capacitors in the DC-link) as shown in Fig. 1-4(iii). The topology has a T-structure, hence its name. In the literature, the T-type NPC inverter topology has been used to provide three-level waveform while maintaining the structure of a conventional two-level inverter [52], [56]- [67]. Research has also been conducted to look at new single switch which can replace two middle switches, thus improving performance of the inverter [56].

Compared to conventional two-level and NPC inverters, it has the following benefits:

i. This topology has lower conduction losses that the NPC and A-NPC inverters because of only one switch in the positive and negative conduction paths, as shown in Fig. 1-4 (iii) and Fig 1-6(iii).

ii. There are fewer switching losses compared to the conventional two-level VSI because each switch is exposed to [57] only half the DC-link voltage (which reduces switching losses in each switch to half those of a switch in a two-level VSI) and lower voltage-rated

switches with better switching characteristics can be used in the neutral point current path, that further reduces switching losses [56].

iii. Unlike NPC inverters, there is no requirement for higher voltage switches while connected to the neutral point for probable fault situations. Hence, it maintains the advantages associated with lower rated switches [52].

Comparing the efficiencies of these three variants, it has been seen [52], [56]- [57], [61], [65], [67] that the T-NPC inverter topology is effective for switching frequencies in the range of 4 kHz to 20 kHz, which are commonly used in traction drive applications.

Despite its advantages, the topology still suffers from the following concerns:

i. It also inherits the DC-link capacitor balancing problem along with the associated sophisticated control schemes and related increase in switching losses [52], [58]- [60].

ii. The loss distribution amongst different switching devices, though better than NPC inverter, remains uneven, as the middle switches carry more current than the upper and lower switches at modulation indices lower than 0.5 [52], [57].

In recent years, several discontinuous PWM (DPWM) schemes were proposed to reduce the switching losses of these three-level inverter topologies. However, following limitations are present with those PWM strategies:

i. The PWM strategies did not investigate at the loss distribution amongst various switching devices [40], [51] - [52] of the T-type inverter topology.

ii. As the reported three-level DPWM strategies are extensions of two-level switching loss reduction strategies, they do not provide any benefit for power factor lower than 0.866 [52].

iii. The current ripple of a three-level inverter varies within a fundamental operating cycle, due to discrete PWM strategies. Earlier works did not look at the impact of different PWM strategies on sub-fundamental cycle current ripple, and resulting variable frequency strategy to reduce inverter switching losses, like existing two-level inverter strategies [37].

1.3.3 Dual Inverter Dual Motor Topology

The single inverter topologies have been used as a part of several dual inverter-motor topologies, as discussed in [30], [68] - [76]. Different dual inverter topologies (also commonly known as parallel inverter topologies in grid-connected applications) exist which can be classified in terms of the motor topologies the dual inverter uses. These motor topologies are either dual motor topologies which consist of two sets of three-phase windings with relative phase-difference (the existing ones have 30°, 180° or 0°) or open-ended winding motors which uses two inverters on two sides of the motor winding.

In Fig. 1-7(i), a dual two or three-level fed dual motor topology has been shown, in which the dual motor had 30° phase difference between two winding sets, which warranted two separate DC-links to avoid circulating current [69-71]. In [72-76], dual two-level or three-level inverter topologies have been used with open-ended configuration, either using an open-ended motor [75-76], or using a three-phase transformer primary side for renewable applications, as shown in Fig. 1-7(ii). Either they used separate balancing circuit to balance capacitor voltages

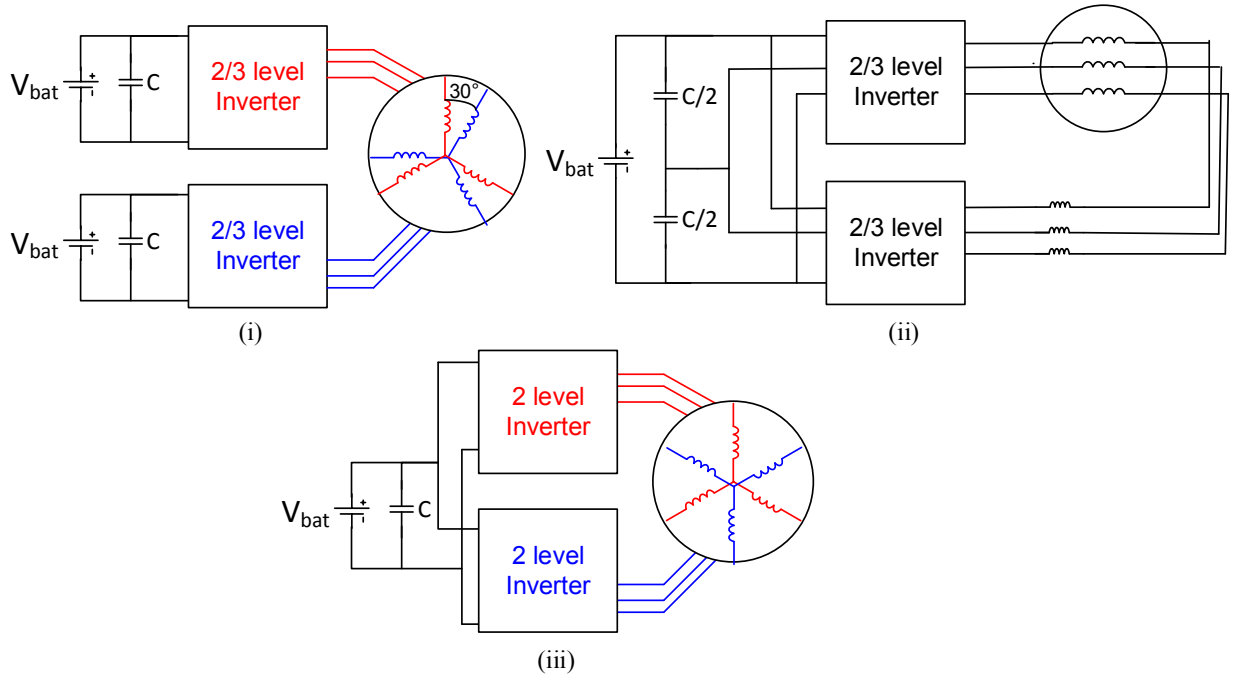


Figure 1-7: Dual Inverter topologies with (i) Dual PMSM (30° phase shifted) (ii) Open-winding motor (iii) Dual PMSM (180° phase shifted) motor

[73], or tried to eliminate circulating current [74] using additional inductors. These configurations, incurred more inverter and losses in additional passive elements due to circulating current flowing through two inverters.

However, the dual motor with 180° phase difference [44] between two sets of windings has been found to be advantageous as it provides two winding sets with negligible mutual coupling compared to the other variants. In [45-46], as shown in Fig. 1-7(iii), a drive topology consisting of two interleaved 2-level inverters feeding such a machine was shown to successfully reduce DC-link capacitor ripple. Thus, the two inverters can be independently controlled.

1.4 Methodology and Tools

The methodology can be outlined by the four main components: (i) Formulating and analyzing state-of-the-art control strategies, (ii) proposing modulation strategies to improve the performance of the inverter topologies, (iii) integration of the models into software tools to perform tests for a wide operating range of operation, and (iv) experimental validation of the proposed strategies. In the following sections, the methodologies are explained.

1.4.1 Formulating and Analyzing State-of-the-art Strategies

The initial approach involves – (i) Formulation of state-of the-art space-vector based PWM strategies for both two-level and three-level inverters. The strategies are designed such that the output voltages have quarter-wave and half-wave symmetry, and in result does not introduce even harmonics in the system. The impacts of these strategies on DC-link current and voltage ripple, device switching losses and output waveform distortion are analyzed. (ii) Formulation of the control structure of a single PMSM based on the conventional field oriented control.

1.4.2 Developing Modulation Strategies for Improvement in Performance

These developed models are used to create new modulation schemes and control structures. The additional factors considered are: (i) The p.u. magnitude and phase of the current waveform at which the device is being switched, (ii) The number of switching sequence needed to create an appropriate three-level voltage waveform, and (iii) The output current harmonic spectrum produced, due to such a sequence. Depending on that information, optimum patterns

of switching sequences are selected to reduce switching losses. The effective switching frequency of the operation is also varied to find the region where the proposed control strategy provides equivalent device junction temperature as the conventional strategy.

While modeling a dual PMSM motor, it is assumed that the mutual coupling between two sets of three-phase winding is negligible, which entails us independent control of each three-phase winding set by two three-level inverters. Therefore, the dual PMSM is modeled as two separate PMSM, driven with the same speed. The dynamic equations of the dual PMSM are formulated, considering the above-mentioned assumption of negligible coupling.

1.4.3 Simulation Implementation

The modulation schemes and control strategies will be implemented using several simulation tools, including the following: (i) PSIM® and Simulink SimPowerSystems® is applied to model the inverter topologies, with inverter loss measurements modeled using datasheet parameters, (ii) MATLAB®/Simulink® is used to implement the modulation schemes and control strategies, and (iii) Infolytica MotorSolve® is used to model the dual PMSM. Two separate PMSMs driven by same speed (Ω) will be considered instead of a dual PMSM.

1.4.4 Experimental Validation

The formulated modulation schemes and control strategies are tested and validated on a small-scale hardware prototype. The hardware setup consists of the following components: (i) a step-up transformer to step-up available three-phase 208 V AC source voltage; (ii) a variac (autotransformer) to manually adjust the step-up transformer output voltage; (iii) a diode rectifier to rectify the variac output voltage to provide the DC-link voltage, (iv) a split-capacitor bank with a neutral point; (v) two, three-level T-NPC inverters; (vi) two, two-level T-NPC inverters; (vii) sets of three-phase R-L load that will be used for testing PWM strategies, as open-loop control of the inverters has been deemed sufficient to compare impact of different PWM strategies on the fundamental operating characteristics of the inverter topologies. The efficacy of the PWM schemes is tested for different modulation indices (varying from 0 to 1) and power factors (by changing load impedances, keeping constant current); (viii) a real-time rapid control prototyping system (OPAL-RT®) which sends gating signals to dedicated gate drivers of inverter

IGBTs. Additionally, a dual three-phase PMSM has also been tested along with a dual three-level T-type topology. The dual PMSM was provided by TM4 Inc., an industrial partner of the Automotive Partnership Canada (APC) project.

1.5 Claims of Originality

The thesis builds on the well-established PWM techniques of the inverter topologies and proposed the following strategies which, to the best of the author's knowledge, are original and are not previously implemented:

1. Identifying the optimal interleaving angles for interleaved continuous and discontinuous pulse-width-modulation strategies for dual two-level inverters. This reduces DC-link capacitor current ripple over the entire modulation index range.
2. An interleaved modulation strategy for dual three-level inverter topology. This maintains DC-link capacitor voltages balanced over the entire operating range.
3. A series of three-level discontinuous PWM strategy which redistributes the device losses and resulting junction temperature more evenly amongst the switching devices of a T-NPC inverter at lower modulation indices.
4. A series of three-level discontinuous PWM strategy for lower power factors, and a space-vector based generalized discontinuous modulation strategy. The strategies decrease switching losses at lower power factors and are applicable for all three-level inverters operating at lower modulation indices.
5. The sub-fundamental cycle current ripple profile of a three-level inverter employing continuous and discontinuous pulse-width-modulation strategies. Based on the profile, the operating switching frequency is varied within a fundamental cycle, which reduces the inverter switching losses.

1.6 Thesis Outline

The work in this thesis is divided into the following parts:

Chapter 2: Interleaved PWM for Dual Two-level Inverter. This chapter studies the dual three-phase inverter configuration for an electric vehicle (EV) drive feeding a dual three-phase

permanent magnet synchronous machine (PMSM). Employing interleaved SVPWM and DPWM modulation techniques with optimum interleaving angles with the proposed configuration, the input capacitor ripple current has been substantially reduced by 40-80%.

Chapter 3I: Dual Three-level T-NPC Inverter. This chapter presents the working principle of the dual three-level, T-type, neutral-point clamped (T-NPC) inverter fed dual Permanent Magnet Synchronous Motor (PMSM) topology. The switching pulses of the T-NPC inverters are interleaved and controlled such that they produce equal and opposite three-phase currents at their output. This maintains balanced DC-link capacitor voltages in steady-state and transient conditions. Hence, the proposed configuration decouples the modulation strategy from the capacitor balancing control.

Chapter 4: DPWM Sequences for Device loss and thermal Redistribution. With conventional pulse-width modulation (PWM) strategies, the switching devices of a three-level inverter are not equally utilized. At modulation indices lower than 0.5, the inner switching devices incur more losses and higher junction temperatures, thus becoming the bottleneck in providing more output power. This chapter presents a series of space-vector based discontinuous PWM (DPWM) sequences which relocates the phase current from the inner to the outer switches of a three-level T-NPC inverter. In consequence, the sequences redistribute the device losses and junction temperatures more equally amongst the inner and outer switches.

Chapter 5: Generalized Discontinuous PWM for Three-Level Inverters Operating at Low Modulation Index. This chapter proposes a series of discontinuous Pulse-width Modulation (DPWM) sequences and a generalized DPWM strategy for a three-level T-NPC inverter operating with modulation indices lower than 0.5. The strategy aligns the no-switching durations of the pulse patterns with the respective phase-current peaks, at all operating power factors. With change in power-factor, the proposed strategy adapts the pulse sequences with minimum possible switchings during the transitions. Thus, the proposed strategy ensures that the switching

loss reduction does not depend on operating power factor and around 50% switching loss reduction can be achieved even at lower power factors.

Chapter 6: Sub-fundamental Cycle Switching Frequency Variation Strategy. This chapter investigates general principles of sub-fundamental cycle current ripple variation of a three-level voltage-source inverter. The investigation employs three-level space-vector based continuous and discontinuous pulse-width modulation strategies to analyze the current ripple variation over the entire operating modulation index, including the over-modulation index range. Based on the current ripple variation, a methodology is used to change the operating switching frequency within a fundamental cycle.

2 Interleaved PWM for Dual Two-Level Inverter

2.1 Overview

This chapter proposes specific interleaving angles for interleaving PWM employed on dual three-phase inverter configuration for an electric vehicle drive feeding a dual three-phase permanent magnet synchronous machine. Employing specific interleaving angles with SVPWM and DPWM modulation techniques, the input capacitor ripple current has been substantially reduced to 50-60 % compared to that of a conventional 2-level VSI. The optimal interleaving angles have been identified for DC-link capacitor RMS ripple current reduction considering the entire modulation indices pertaining to the traction motor's operating range.

2.2 Introduction

Several papers in the literature have analyzed the ripple content of the dc-link capacitor current and recommended modifications to modulation schemes such that it can be reduced. In [29] - [77], [78] - [79] analytical expressions for the capacitor RMS ripple current have been discussed for different modulation indexes and power factors. Use of the high-frequency film capacitor [31], corresponding losses and self-heating of the capacitors for different PWM techniques have been analyzed in [33]. In [15], the influence of the capacitor's ESR at different switching frequencies, modulation indexes and power factors have been analyzed. A space vector modulation (SVPWM) algorithm has been proposed in [34] to reduce the loss in the DC-link capacitors. A modification of the earlier strategy is also proposed in [80] to reduce the DC-link ripple, however, both studies increase the output current distortion significantly. In [81], a direct capacitor current control is proposed, however, any impact on inverter device switching losses have not been considered.

Moreover, these studies used the conventional 2-level VSI and a 3-phase PM motor. In last decade, studies have been conducted on dual three-phase inverter for open-end winding motors [82], six-phase motors [68]- [84], dual three-phase motors [76], [85]- [88], and segmented

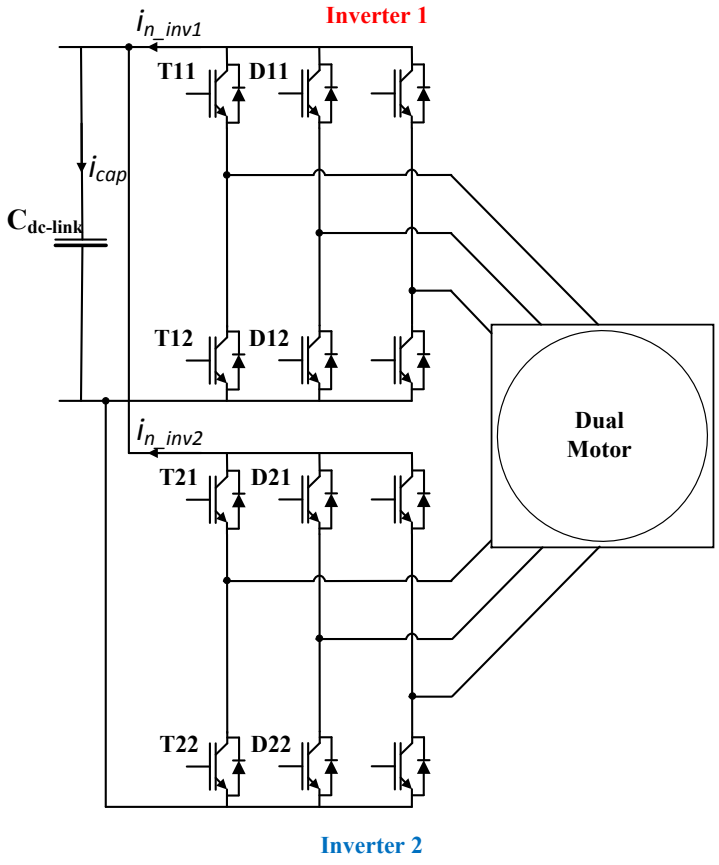


Figure 2-1. Dual 2-level inverter feeding a dual 3-phase PMSM (180° phase-shifted stator winding sets)

six- phase motors [30], [89]- [91]. Recently, different PWM strategies for these dual three-phase inverter topologies have also been introduced in [85] - [86], [30], [91] - [92] for motor drive applications, and in [29] for grid applications to reduce the DC-link ripple. For example, in [30] an interleaved sine-PWM (SPWM) is used with 180° phase shifted carrier waveforms, to reduce the capacitor ripple current for different modulation indexes and motor speeds. However, it did not look at impact of different interleaving for SVPWM and discontinuous PWM (DPWM) strategies over the entire modulation index range.

This study deals with interleaved SVPWM and DPWM strategies for a dual two-level inverter, shown in Fig. 2-1, and proposes specific interleaving angles to reduce the DC-link capacitor ripple over the entire modulation index range [85]. The investigation has been divided into three different parts. In Section II, the influence of using the PWM techniques on the harmonic contents of the capacitor current ripple have been analyzed for different operating

points. Based on the analysis, suitable interleaving angles have been identified for different operating points. The confirmatory simulation and experimental results are provided in section III and section IV.

2.3 DC-Link Input Capacitor Ripple Analysis

The two-level 3-phase inverter has an input current (i_{inv}) , shown in Fig. 1-3, which can be decomposed to a dc component and several harmonic components, at and around f_{sw} and its integer multiples (nf_{sw}), where f_{sw} is the operating switching frequency of the system and 'n' is the harmonic order. The current can be written as

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} I_{n,k}\sin\left[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}\right] \quad (2.1)$$

where $I_{n,k}$ and $\alpha_{n,k}$ represent respectively the amplitude and phase angle of the harmonic component identified by the integers, n and k. The switching frequency harmonic components present in the inverter's input current are handled by the dc capacitor whereas the dc component of the input current is supplied by the battery. The major components of the capacitor ripple current have frequencies of multiples of the switching frequency (nf_{sw}). The RMS value of the capacitor ripple current i_{cap} can be calculated by

$$i_{cap(rms)} = i_{o/p(rms)} * \sqrt{\frac{m}{4\pi}\left[2\sqrt{3} + 8\sqrt{3} - 4.5\pi m)cos^2\varphi\right]} \quad (2.2)$$

where m is the modulation index; φ the displacement power factor; and $i_{o/p(rms)}$ the RMS values of the fundamental motor phase current. The capacitor ripple current can reach over 60 % of the motor current.

2.3.1 Capacitor Harmonic Content for Single Inverter

Typically, the switching frequency current component handled by the dc-link capacitor of a single inverter is composed of fundamental switching frequency components (harmonics on or aroundf_{sw}), and first switching frequency harmonic components (harmonics on or around$2f_{sw}$). Fig. 2-2 shows the relative magnitude distribution of these two components over the entire modulation index range for SVPWM and DPWM2 strategies. The following can be noted:

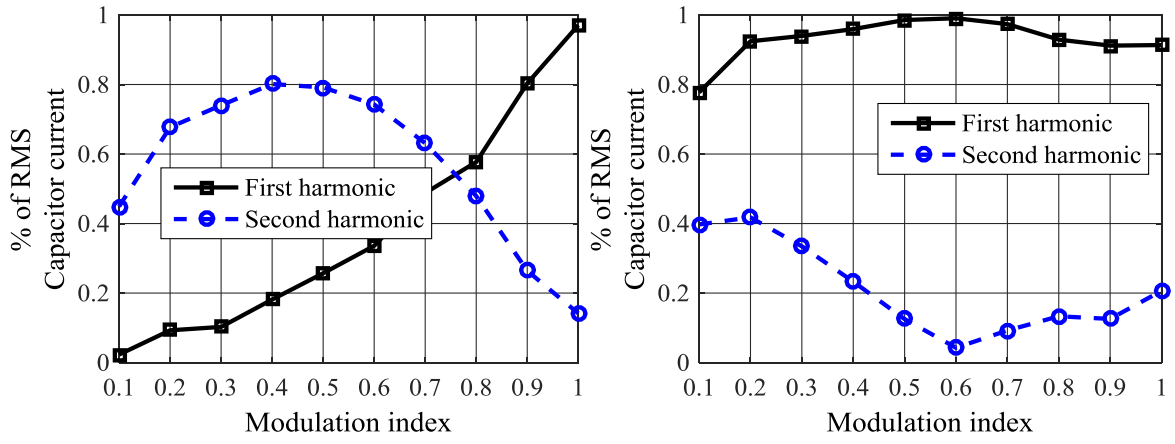


Figure 2-2. First and Second switching First and Second switching frequency harmonic components for (i) SVPWM, and (ii) DPWM2 strategies for single inverter frequency harmonic components for (i) SVPWM, and (ii) DPWM2 strategies for single inverter

- As shown in Fig. 2-2 (i), with SVPWM, the second harmonic (harmonics around on or around $2f_{sw}$) are substantially higher than the first harmonic (harmonics around on or around f_{sw}) components for modulation indices lower than 0.8. Above 0.8 modulation index, the magnitude of first harmonic component is higher than the second component. This phenomenon is since at modulation indices considerably lower than unity, the continuous modulation pattern of SVPWM creates two pulses per switching cycle in a line-line voltage waveform. As it approaches unity modulation index, the pulses become wider, thus increasing the first harmonic component.
- As shown in Fig. 2-2 (ii), with DPWM2, the second harmonic (harmonics around on or around $2f_{sw}$) are always substantially lower than the first harmonic (harmonics around on or around f_{sw}) components for the entire modulation index range. This can be attributed to the discontinuity is pulse patterns and resulting single pulse patterns in a switching cycle for the line-line voltage waveform.

2.3.2 Technique to Reduce Current Ripple for Dual Inverter

Referring to Fig. 2-1, in the dual-inverter configuration, each inverter supplies power to dedicated sets of three-phase load, while using a common DC bus. Compared to the single inverter topology, the dual inverter's input capacitor's current harmonic components consist of harmonic created by both inverters. This is illustrated in Fig. 2-1 whereby I_{n_inv1} and I_{n_inv1}

represent the harmonic component associated with the nth harmonic of two inverters (assuming $|I_n| = |I_{n\_inv1}| = |I_{n\_inv2}|$ in a similar system).

Now, referring to Fig. 2-3(i), if the carrier waveforms of both inverters are not interleaved (signifying $n\beta = 0$; where $n\beta$ is the angle difference between the nth harmonic component of each inverter input current due to an interleaving angle β), the total nth harmonic component would be $2I_n$. On the other hand, referring to Fig. 2-3(ii), if the carrier signals are interleaved (i.e. $n\beta \neq 0$), the total inverter input current can be written as

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty}\sqrt{\frac{1+\cos(n\beta)}{2}} * I_{n,k}\sin\left[2\pi(nf_{sw} \pm kf_m)t + \frac{\alpha_{n,k} + n\beta}{2}\right] \qquad (2.3)$$

Hence, the total nth harmonic component would be $2I_{n,k}\cos(n\beta/2)$. Moreover, the following can be noted:

- For 'n' taking the value of 1, the term $2I_n\cos(n\beta/2)$ equates to zero if the value of the interleaving angle β is 180°.
- For 'n' taking the value of 2, the term $2I_n\cos(n\beta/2)$ equates to zero if the value of the interleaving angle β is 90°.

Hence, if the dominant harmonics are around the first switching frequency harmonic, 180° interleaving angle needs to be used. On the other hand, if the dominant harmonics are around the second switching frequency harmonic, 90° interleaving angle needs to be used.

Hence, for SVPWM strategy, 90° interleaving angle needs to be used for modulation indices lower than 0.8 due to dominance of second harmonics. For higher modulation indices, due to dominance of first harmonics, 180° interleaving angle needs to be used. On the other hand, for DPWM2 strategy, due to dominance of first harmonics, 180° interleaving angle needs to be used for the entire modulation index range. Impact of these two different interleaving angles have been shown in Fig. 2-3 (iii). It can be seen that without any interleaving, the net DC bus current is higher than the cases when 180° and 90° interleaving angles are used. The relative reduction will be measured by looking at the harmonic spectrum of the current in later sections.

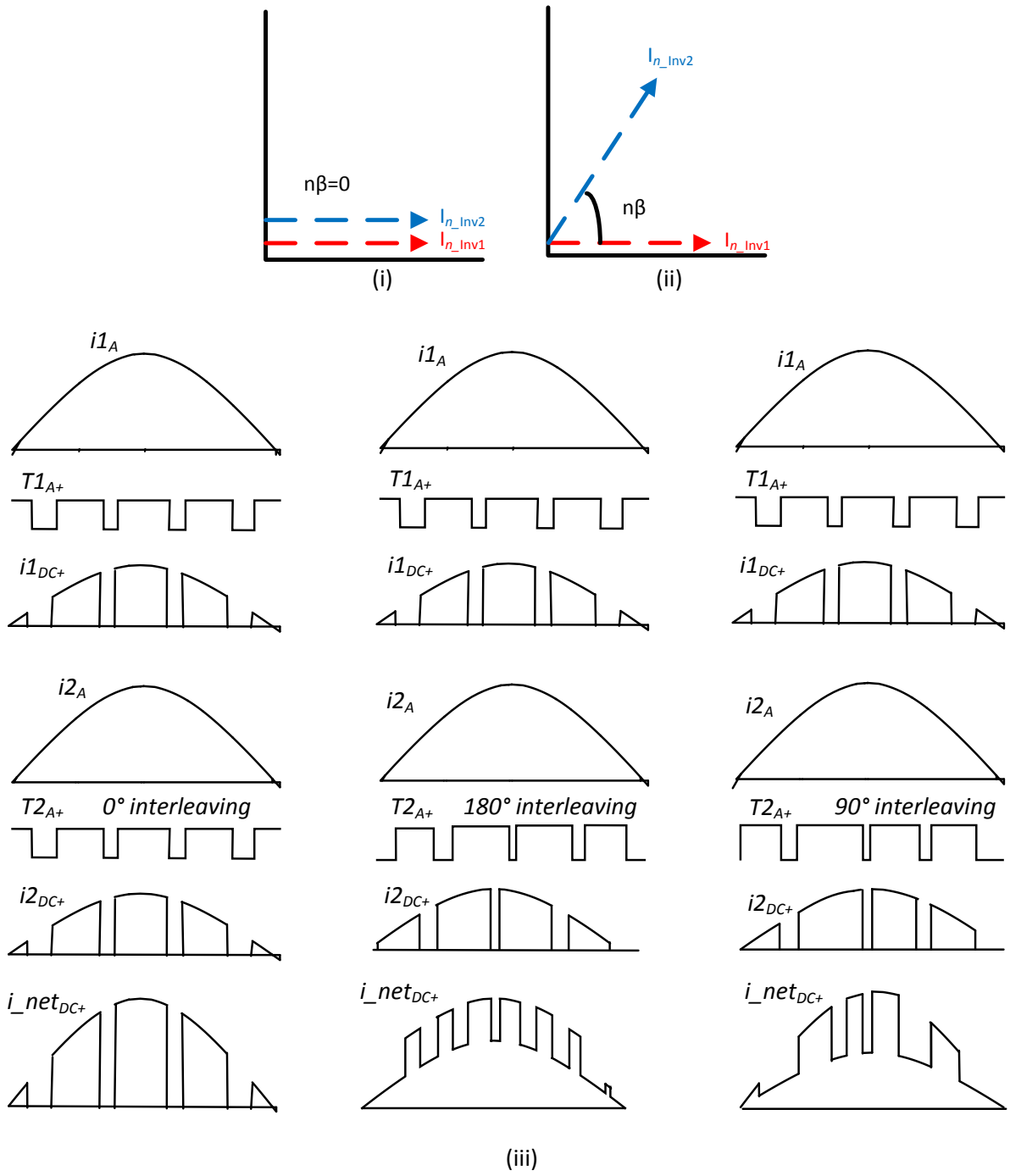


Figure 2-3. Capacitor nth harmonic contents (i) Interleaving angle 0°, (ii) Interleaving angle nβ, (iii) graphical waveform showing impact of interleaving on positive DC bus current ripple

It is worthwhile to mention that in an electric vehicle operation, although the EV drive is mostly in transients, the modulation index can easily be monitored based on its speed. As the proposed strategy depends only on modulation index value (not on the first and second switching

frequency harmonics magnitude), and the changeover between 90° and 180° only happens at modulation indices higher than 0.85, the system implementation complexity would not increase.

2.4 Simulation Results

The simulations have been conducted using – (i) A dual two-level inverter with no interleaving between the pulses of two inverters, fed from a 400 V battery with a 500 µF DC-link capacitor feeding a three-phase passive R-L load, and (ii) A dual two-level inverter with interleaving, fed from a 400 V battery with a 500 µF DC-link capacitor feeding a dual three-phase passive R-L load. The power factor of the load is 0.9. The tests had been conducted for the entire modulation index range. The modulation index has been calculated regarding the maximum dc-link voltage using SVPWM. The fundamental frequency is 100 Hz and the nominal switching frequency is 4.8 kHz.

In comparison to the interleaved SPWM studied in [1] in which two identical carrier waveforms (saw-tooth and triangular) have been phase-shifted by 180°, in this study, the interleaved SVPWM and DPWM2 is implemented by interleaving the duty-cycle calculation sequences. As for each switching cycle period ($T_{sw} = 1/f_{sw}$), each inverter uses different switching patterns and calculates the duty-cycle of the discrete switching states (100, 101, 001,..) to provide the reference voltage vector, interleaving is employed to change the duty cycle calculation, resulting in interleaved pulses.

2.4.1 Inverter Current Waveforms without Interleaving

In Fig. 2-4(i), the inverter's output line current, dc-link capacitor current (i_{cap}), its RMS component and the battery current (i_{bat}) have been. The modulation index is 0.5 and the SVPWM strategy is used. The modulation index is 0.5 and the SVPWM strategy is used. The capacitor RMS ripple current is 171 A and the battery current varies considerably between 40 A and 220 A.

2.4.2 Inverter Current Waveforms with Interleaving

In Fig. 2-4(ii), the dual inverter's output line currents, dc-link capacitor current(i_{cap}), its RMS component and the battery current (i_{bat}) have been plotted. The modulation index is 0.5

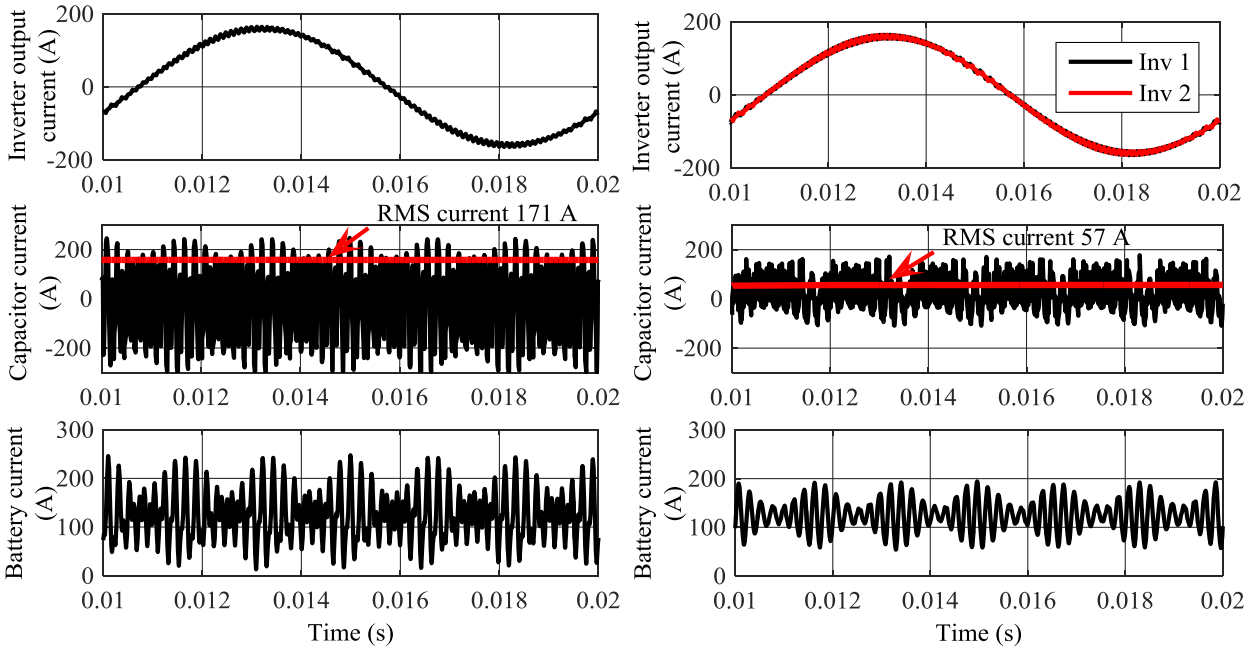


Figure 2-4. Line currents, DC-link capacitor currents, DC-link capacitor RMS current and battery current for (i) without interleaving and (ii) with interleaved SVPWM

an d the interleaved SVPWM strategy with 90° interleaving angle is used. The capacitor RMS ripple current reduces to 57 A, a 70% reduction compared to the single inverter topology. the battery ripple current reduced to 80-190 A, considerable reductions when compared to Fig. 2-4(i).

2.4.3 Harmonic Content of Ripple Current

To investigate and compare the capacitor ripple contents of both the single inverter and dual inverter configuration, two different operating points have been considered. These are: (i) modulation index: 0.5, and (ii) modulation index: 1. The switching frequency has been taken as 4.8 kHz. SVPWM and DPWM2 have been employed to study the capacitor ripple content.

Referring to Fig. 2-5(i-ii), the single inverter employing SVPWM generates dominant components around twice the switching frequency (n=2) for lower modulation indices and around the switching frequency (n=1) for higher modulation indices. This entails the use of two different interleaving angles when employing SVPWM for the full operating range of the traction motor. As seen from Fig. 2-5(i-ii), at lower modulation index, employing a 90° interleaving angle

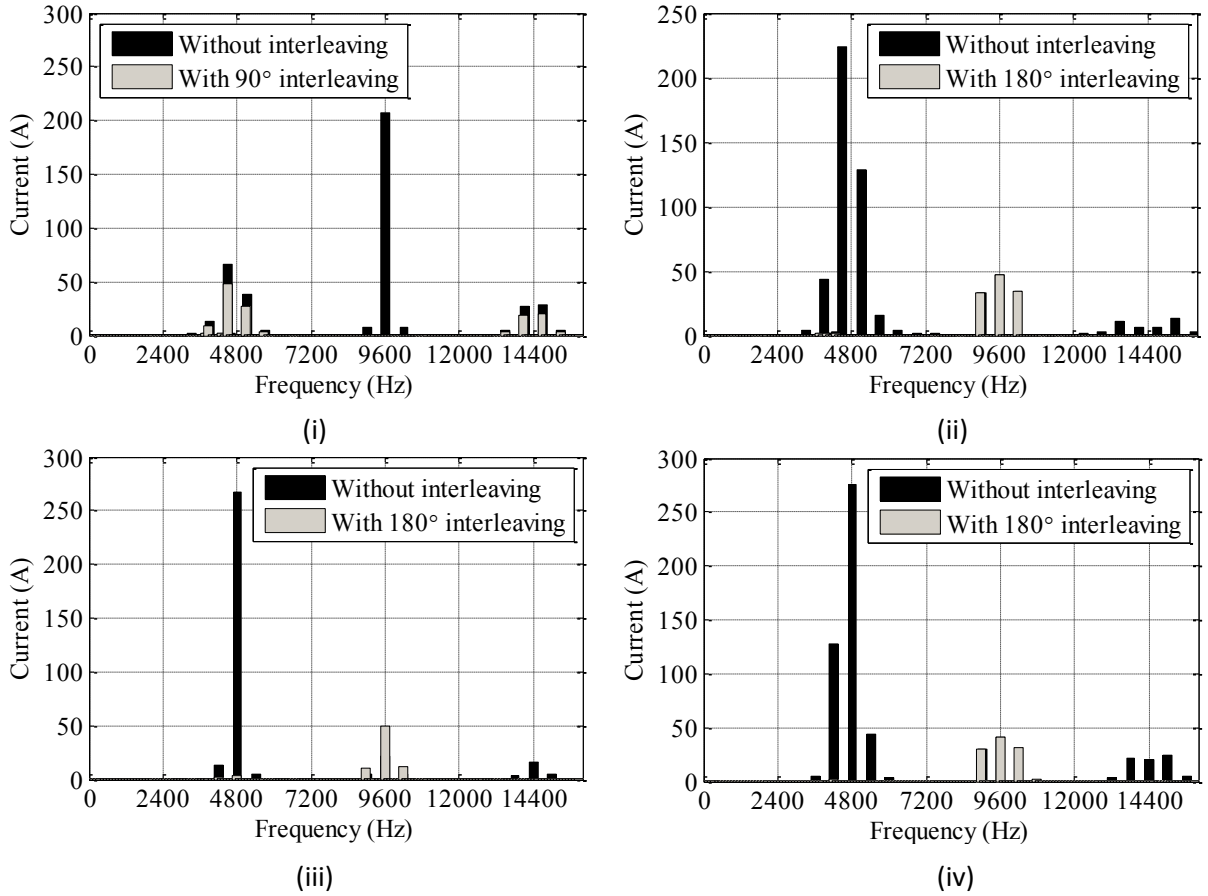


Figure 2-5. Capacitor harmonic spectrum for without and with interleaved PWM (i) m: 0.5 SVPWM with interleaving angle 90°; (ii) m: 1 SVPWM with interleaving angle 180°; (iii) m: 0.5 DPWM2 with interleaving angle 180°, and (iv) m: 1 DPWM2 with interleaving angle 180°

cancels the dominant harmonic components whereas at higher modulation index, use of a 180° interleaving angle cancels the dominant harmonic components. Employing interleaving, the ripple content has been reduced to 5-20% of the output fundamental RMS current compared to the 60-70% for the strategy without interleaving.

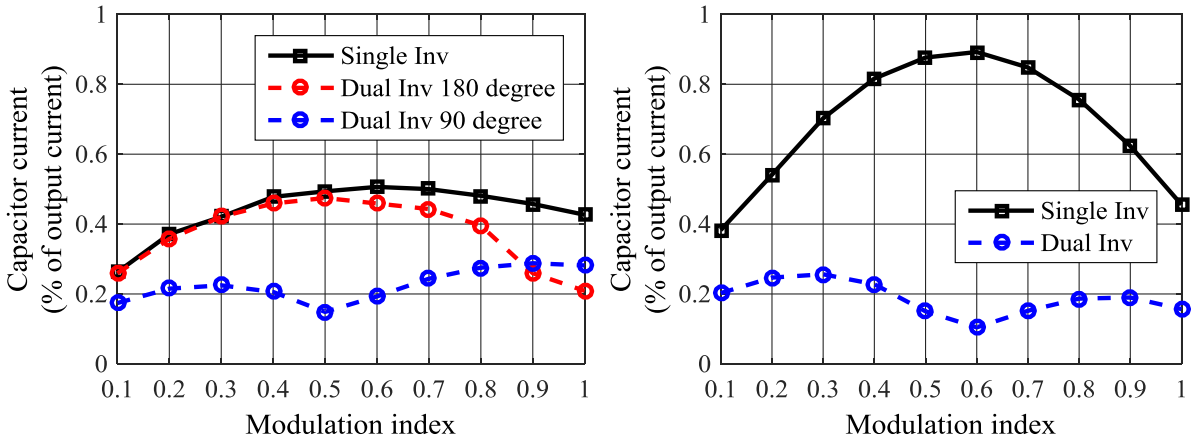
Moreover, DPWM2 strategy without interleaving is implemented and it can be noted that the capacitor RMS ripple current is 60-80% of the output fundamental RMS current. Moreover, the dominant capacitor harmonic components are at the switching frequency (4800 Hz; denoted as n=1). This implies using an 180° interleaving angle to cancel the dominant harmonics. As seen from Fig. 2-5 (iii-iv), using a 180° interleaving angle, the dominant harmonic component at 4.8 kHz (n=1) has been cancelled. With interleaving, the ripple content has been reduced to 15-20% of the output fundamental RMS current. The results have been summarized in Table 2-1.

TABLE 2-1: SUMMARY OF SIMULATION RESULTS

Case	Modulation index	1st switching frequency harmonic (A)	2nd switching frequency harmonic (A)
Without interleaving - SVPWM	0.5	70	210
	1	225	50
With 90° interleaving angle - SVPWM	0.5	70	0
	1	-	-
With 180° interleaving angle - SVPWM	0.5	-	-
	1	5	50
Without interleaving - DPWM	0.5	260	50
	1	260	40
With 180° interleaving angle - DPWM	0.5	5	50
	1	2	40

2.4.4 Impact on DC-link Capacitor RMS Current

Based on the previous analysis, the appropriate interleaving angles have been selected for capacitor ripple RMS current reduction for SVPWM and DPWM2 techniques as shown in Fig. 2-6(i-ii). For operation without interleaving, the RMS ripple current follows Equation 2.2. Below 0.9 modulation index, use of 90° interleaved angle for interleaved SVPWM strategy provides a considerable capacitor ripple reduction, around 50-70%. Whereas, above 0.9 modulation index, due to dominance of first harmonics, the interleaving angle is changed to 180°. This reduces DC-



(i) (ii)

Figure 2-6. DC-link capacitor current w.r.t. RMS output current for (i) SVPWM, and (ii) DPWM2 strategies

link capacitor RMS current component more than the value obtained with the use of 90° interleaving angle.

On the other hand, for DPWM2 strategy, due to dominance of first frequency harmonics over the entire modulation index range, 180° interleaving angle is only used, and it results in the around 50-90% RMS capacitor ripple current reduction.

2.5 Experimental Results

The proposed interleaved PWM strategy has been tested on a scaled down setup, shown in Fig. 2-7. The setup consists of a dual two-level inverter feeding two three-phase passive loads (22 Ω, 30 mH). The fundamental frequency is 100 Hz and the switching frequency is 4.8 kHz (resulting in 48 carrier ratio, typical of an EV application). A lower inductance (5 mH), if available, would have produced higher ripple for each of the above cases, however, the impact of different interleaving angle on harmonic current reduction would remain similar. The DC-link voltage of the setup is 200 V and the operating modulation index is varied to check the impact at different

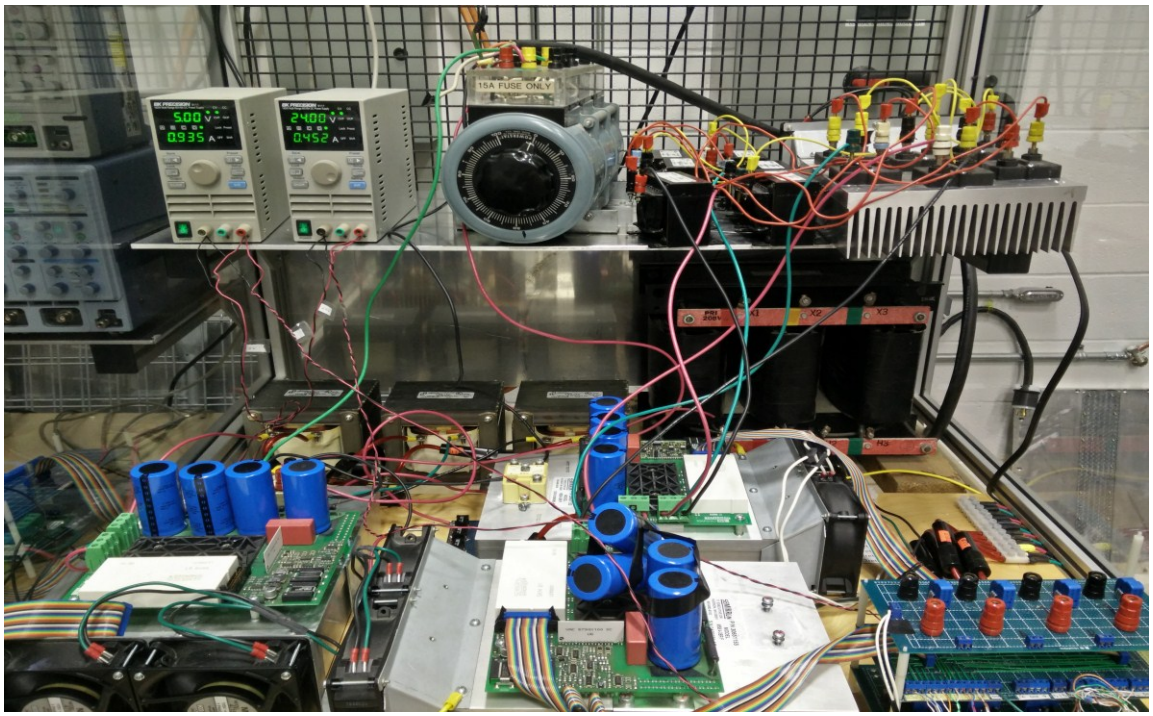


Figure 2-7. Experimental setup of Dual two-level inverter

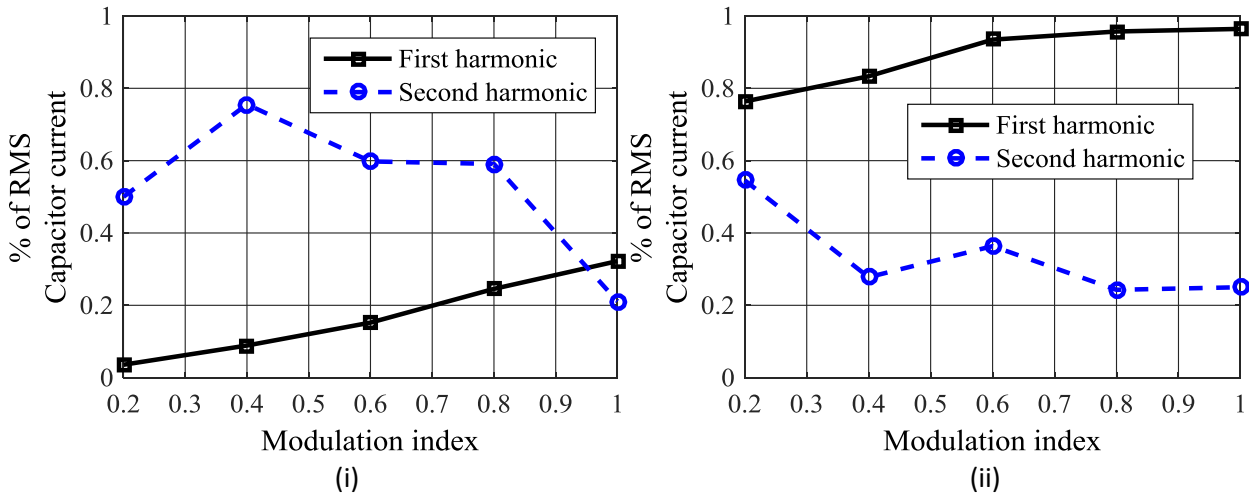


Figure 2-8. Experimental results - first and second switching frequency harmonic components for (i) SVPWM, and (ii) DPWM2 strategies for single inverter

operating points. The control is implemented on an OPAL-RT based real time prototyping tool with a 25 μs operational time step.

2.5.1 Capacitor Harmonic Content without Interleaving

Like simulation results, the first and second switching frequency harmonics are compared in Fig. 2-8, for SVPWM and DPWM2 strategies. For SVPWM, the first switching frequency component is lower than the second component till 0.9 modulation index, and increases afterwards. On the other hand, for DPWM2, the first switching frequency component of the ripple is always higher than the second switching frequency harmonic component.

2.5.2 Inverter Waveforms and Harmonic Spectrum Comparison

Fig. 2-9 shows the experimentally obtained phase voltage, phase differences between pulses of two inverters, line currents and DC-link capacitor currents for dual inverter using the following interleaving angle – (a) 0°, (b) 90°, and (c) 180°. Fig. 2-10 also shows the harmonic spectra of the DC-link capacitor current. The following can be noted:

- Referring to Fig. 2-9(i-ii), with 0° interleaving angle, there is no phase difference between the pulses of two inverters. With 0.5 and unity modulation indices, the capacitor RMS currents are 0.43 A and 0.9 A. Referring to Fig. 2-10(i-ii), for 0.5 modulation index, the dominant harmonics are around 9.6 kHz (second fsw harmonic), and around 4.8 kHz (first fsw harmonic) for unity modulation index.

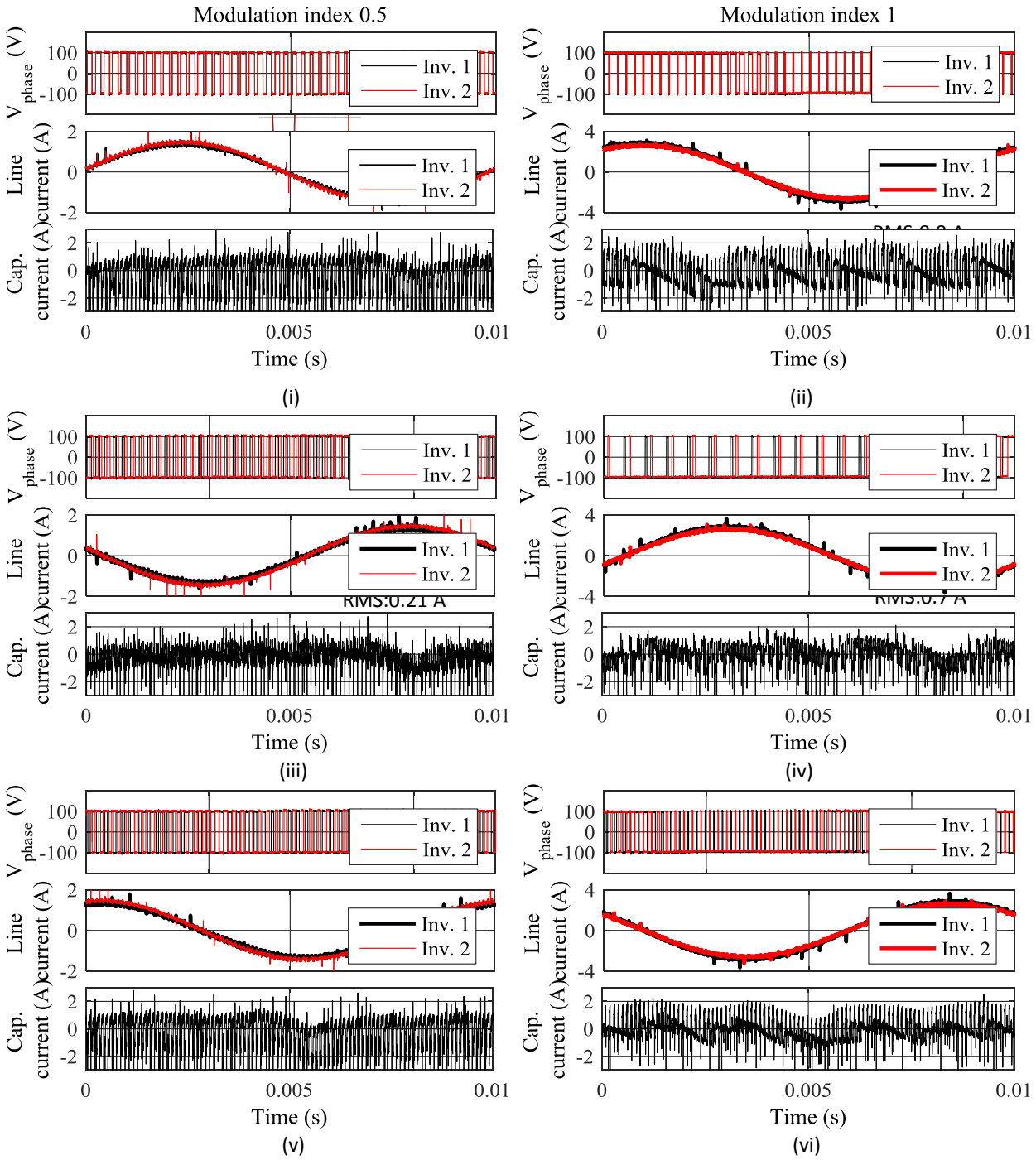


Figure 2-9. Experimental phase voltage (also showing phase difference between pulses of two inverters), Line currents and DC-link capacitor currents for SVPWM with 0° interleaving angle with modulation index (i) 0.5 and (ii) 1; SVPWM with 90° interleaving angle with modulation index (i) 0.5 and (ii) 1; SVPWM with 180° interleaving angle with modulation index (i) 0.5 and (ii) 1

- Referring to Fig. 2-9 (iii-iv), with 90° interleaving angle, there is phase difference between the pulses of two inverters. With 0.5 and unity modulation indices, the capacitor RMS current

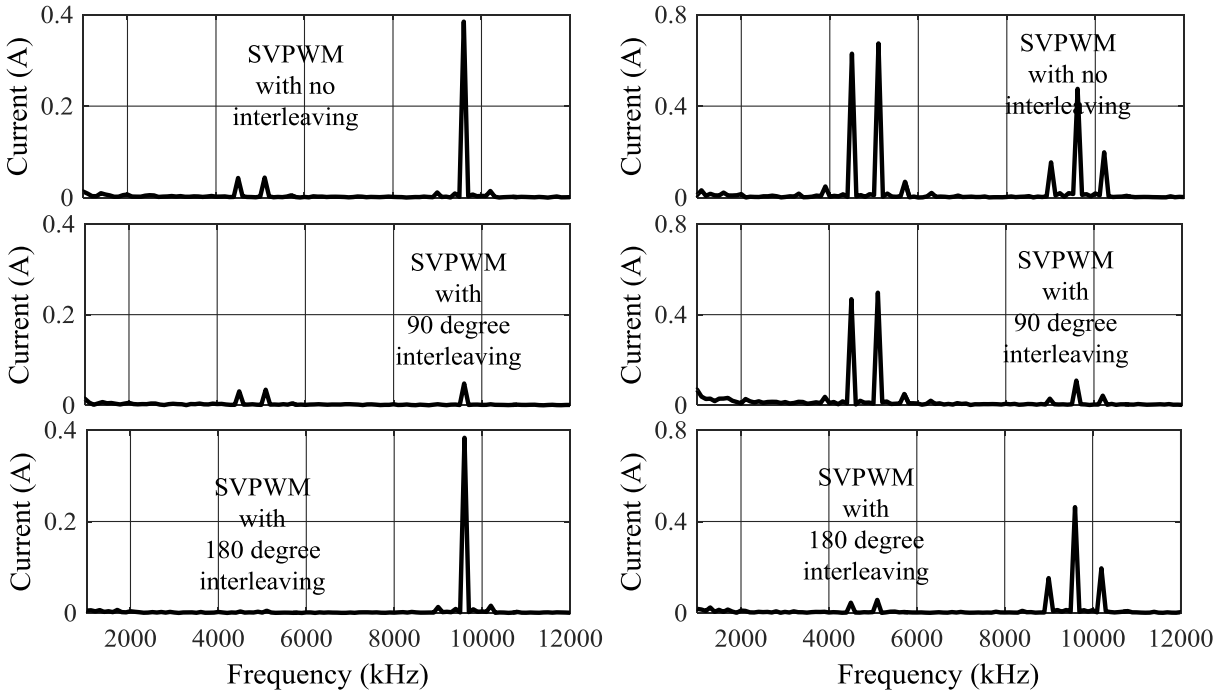


Figure 2-10. Experimental results - Capacitor harmonic spectrum for (i) m: 0.5 ,SVPWM with 0°, 90° and 180° interleaving angle (top to bottom) and (ii) m: 1 ,SVPWM with 0°, 90° and 180° interleaving angle (top to bottom)

reduces to 0.21 A and 0.7 A. Referring to Fig. 2-10 (i-ii), using 90° interleaving angle, the harmonics which are around 9.6 kHz (the second fsw harmonic) reduces appreciably.

- Referring to Fig. 2-9 (v-vi), with 180° interleaving angle, the pulses of two inverters are out of phase. With 0.5 and unity modulation indices, the RMS content of the capacitor current reduces to 0.4 A and 0.55 A. Referring to Fig. 2-10 (i-ii), using 180° interleaving angle, the harmonics around 4.8 kHz (the first fsw harmonic) reduces appreciably. These results have been summarized in Table 2-2.

2.5.3 Impact on RMS Current Ripple of Capacitor

The DC-link capacitor ripple RMS currents for the interleaved PWM techniques are shown in Fig. 2-11 (i-ii). For SVPWM, 90° and 180º interleaving angles are used for modulation indices lower and higher than 0.9, respectively. For DPWM2 strategy, over the entire modulation index range, 180° interleaving angle is only used. The results show that the strategy reduces around 40-80% RMS capacitor RMS ripple content over entire modulation index.

TABLE 2-2: SUMMARY OF EXPERIMENTAL RESULTS

Case	Modulation index	1st switching frequency harmonic (A)	2nd switching frequency harmonic (A)
Without interleaving - SVPWM	0.5	0.005	0.4
	1	0.7	0.5
With 90° interleaving angle - SVPWM	0.5	0.005	0.005
	1	0.5	0.1
With 180° interleaving angle - SVPWM	0.5	0	0.4
	1	0.005	0.5

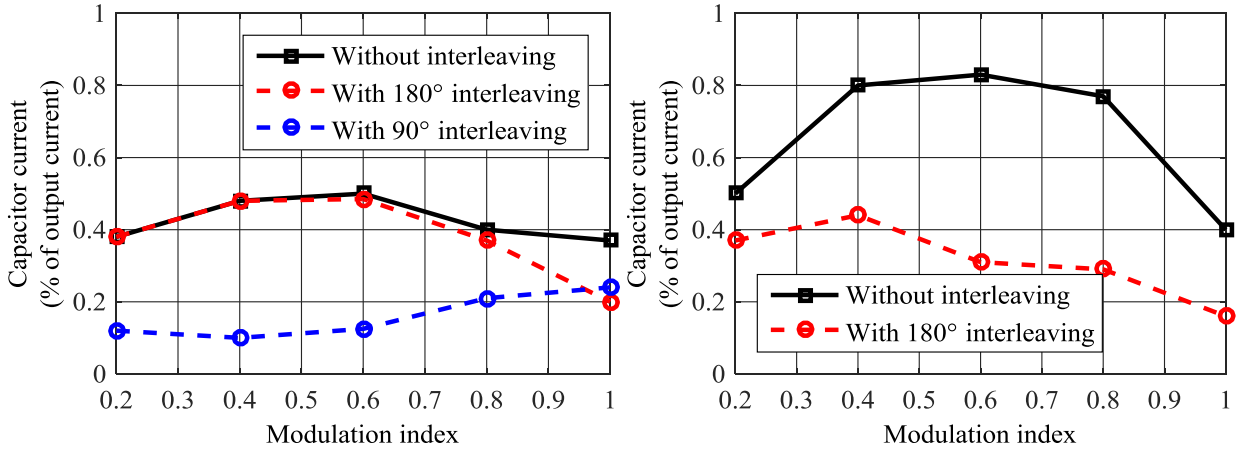


Figure 2-11. Experimental results - DC-link capacitor current w.r.t. RMS output current for (i) SVPWM, and (ii) DPWM2 strategies

2.6 Conclusion

In this work, the influence of the dual 3-ϕ inverter configuration, employing both interleaved SVPWM and DPWM modulation techniques on the capacitor ripple current has been studied. It was shown that for different operating points, only specific interleaving angles lead to a substantial reduction in the capacitor ripple currents. Implementation of this traction drive configuration and associated modulation techniques would lead to a capacitor ripple current reduction of 60 %, thus reducing the rating and cost of the input capacitor.

In the next chapter, a dual three-level three-phase T-NPC inverter is investigated similarly for reduction of its dc-link capacitor voltage ripple reduction using interleaved PWM technique.

3 Dual Three-level T-NPC Inverter

3.1 Overview

This chapter presents the working principle of the dual three-level T-NPC inverter fed dual PMSM topology. The switching pulses of the T-NPC inverters are interleaved and controlled such that they produce equal and opposite three-phase currents at their output. This maintains balanced DC-link voltages, thus decoupling the modulation strategy from the capacitor balancing control.

3.2 Introduction

Three-level inverter solutions such as three-level Neutral Point Clamped (NPC) [40], [93] – [94] and T-type NPC (T-NPC) inverters [52], [56]- [58] have been investigated for potential acceptance in the low-vo ltage, high-power automotive applications. Compared to the conventional two-level VSI, their capabilities include: 1) Lower switching losses; as the switches of the three-level inverters switch at half of the switching frequency and half of the DC-link voltage, 2) Lower output current distortion. Moreover, the T-NPC inverters incorporate the advantages [52] associated with the conventional two-level VSI, for instance, lower conduction loss when compared with the NPC inverter.

However, these three-level inverters have some drawbacks that limit their applications. These include: (i) To balance the voltage levels among split DC-link capacitors (explained with few equations in Appendix A, section A.5), passive DC-link capacitor voltage balancing schemes [42] - [45], [58] are typically used which introduce more switching instances, increasing switching losses by 10-15% [43]. Additionally, these strategies have limited impact on reducing capacitor voltage deviation and their effectiveness during transient conditions has not been reported. (ii) For better performance, active capacitor balancing schemes [95] have been developed, however, they incur more switching instances and require more sensors for operation. (iii) If the capacitor voltages are not balanced using the balancing techniques, the inverter output voltage becomes distorted. This degrades inverter output current. (iv) The DC-link capacitors of three-level inverters carry

the load current. This heats the DC-link capacitors which may be problematic when operating under high ambient temperatures [94]. (v) As the capacitor balancing schemes are coupled with inverter PWM strategies, they limit the use of advanced discontinuous PWM schemes, aimed to further reduce switching losses [52], [96].

In this chapter, a new approach of controlling a dual three-level T-NPC inverter fed dual PMSM topology [97], as shown in Fig. 3-1, is proposed for the low-voltage, high-power automotive applications. The proposed topology has the following features: (i) The dual three-level T-NPC topology employs two identical T-NPC inverters. These two inverters share a single DC-link with split DC-link capacitors and provide balanced three-phase output to two separate three-phase loads. Compared to a dual two-level topology as shown in chapter 2, it does not require any additional sensors. (ii) The inverters feed two sets of a dual PMSM topology which consists of two s eparate three-phase stator windings with a single exterior rotor. The respective

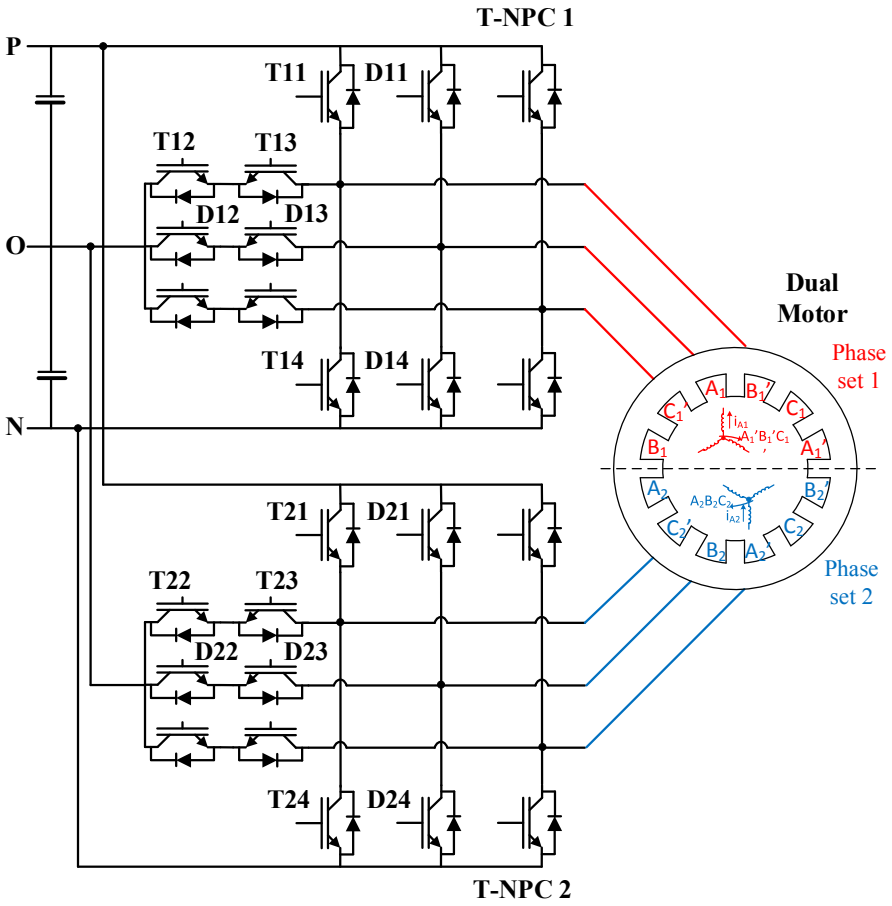


Figure 3-1. Dual T-NPC inverter fed dual PMSM topology

stator winding sets are housed in two separate parts of the stator for reduced mutual inductance. Both sets operate with the same fundamental frequency and similar current. (iii) The inverter topology and proposed control strategy balances DC-link capacitor voltages and decouples inverter PWM strategy from DC-link capacitor voltage balancing, thus avoiding additional switching instances compared to the single T-NPC inverter topology. (iv) The current through the DC-link capacitors (explained with few equations in Appendix A, section A.5) is reduced, which reduces associated capacitor heating and losses. (v) The topology is able to use three-level discontinuous PWM schemes, aimed to further reduce switching losses, without impacting capacitor voltage deviation, compared with the conventional three-level T-NPC topology.

3.3 System Configuration & Modulation Strategy

The schematic of the proposed inverter topology has been shown in Fig. 3-1. The topology has two T-NPC inverters, connected to the same DC-link. Each leg of a T-NPC inverter has four IGBTs and four anti-parallel diodes. The IGBT switches and diodes of i^{th} inverter (i=1, 2) is denoted as T_{ij} and D_{ij} where j denotes the number of a IGBT/diode among 12 IGBTs/diodes of one T-NPC inverter. Two of the IGBTs along with respective antiparallel diodes are connected to the neutral-point of the DC-link. The other two switches are placed like a conventional two-level

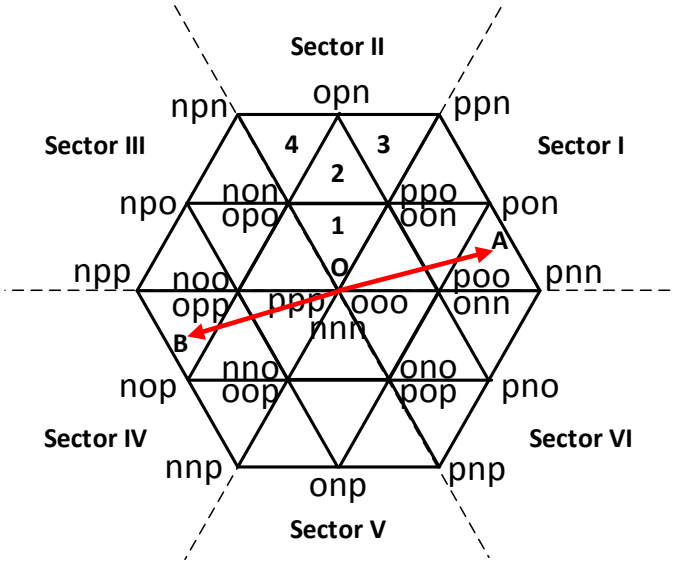


Figure 3-2. Dual T-NPC inverter fed dual PMSM topology

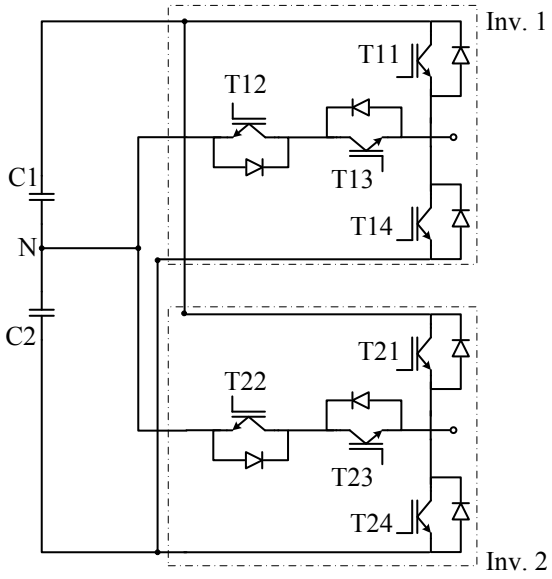


Figure 3-3. A single leg of T-NPC inverter

inverter. Each T-NPC inverter feeds to the respective three- phase stator winding sets (A1B1C1 and A2B2C2) of the dual PMSM.

Conventionally, the three-level space vector PWM (SVPWM) technique [98] provides the switching pulses to the T-NPC inverters. Fig. 3-2 shows the space vectors of a three-level inverter with 27 switching states. It has six sectors (I-VI) and each sector is divided into four sub-sectors (1-4).

Looking at the single legs of two T-NPC inverters in Fig. 3-3, consider that the PWM pattern that sets the gating signals of the inverters' switches are such that the uppermost IGBT of Inverter 1 (T11) has the similar gating signal pulse as the lowermost IGBT of Inverter 2 (T24), and switch T12 of Inverter 1 has the similar pulse as T23 of Inverter 2. Thus, the line-line voltages produced by two inverters will be 180° phase-shifted. For example, referring to Fig. 3-2, the reference voltage of inverter 1 is OA and in subsector 3 of sector I, the switching sequence to form OA is [(POO) – (PON) – (PNN) – (PON) – (POO)]. The corresponding switching sequence of inverter 2 is (NOO) – (NOP) – (NPP) – (NOP) – (NOO)]. Thus, the reference voltage of inverter 2 is OB and it is in subsector 3 of sector IV, 180° phase-shifted from OA. Consequently, over a

complete fundamental cycle, the resultant output currents of these two inverters will be 180° phase-shifted.

A du al three-phase Permanent Magnet Synchronous Motor (PMSM) topology is considered as the dual motor load of the proposed topology. The dual PMSM consists of two sets of three-phase stator windings (A1B1C1 and A2B2C2) with a common rotor. As reported in [99], in a dual three-phase motor, if the windings of A1B1C1 set do not share any slot with the windings of A2B2C2 set, the mutual inductance between two sets of three-phase windings can be neglected. For example, in [100]- [101], for dual three-phase interior permanent magnet (IPM) and surface-mounted permanent magnet (SPM) motors, authors have discussed a winding configuration which places two sets of three-phase windings in two separate halves of a single stator. A generic diagram of such a configuration is shown in Fig. 3-1. As reported in [100]- [102], with this configuration, the mutual coupling between two sets of three-phase windings is minimized and therefore can be neglected in comparison to the self-inductances of each phase-set. So, from the control point-of-view, those two sets of three-phase windings can be considered as two independent phase-sets [100] - [102].

As shown in Fig. 3-1, for the phase set 1, the neutral-point is formed using the A1', B1' and C1' winding terminals. On the other hand, for the phase set 2, the neutral-point is formed using the A2, B2 and C2 winding terminals. In this manner, the respective stator winding sets are also 180 electrical degrees apart.

If the phase currents through each of the three-phase winding sets are also 180° phase-shifted from each other, both currents corresponding to any phase (for instance for phase A: i_{A1}, i_{A2}) would be in the same direction, relative to the rotor reference frame. This is shown in Fig. 3-1. As they are in the same direction, torque produced by the dual PMSM will be the algebraic sum of the torques produced by each three-phase stator winding set on the common rotor. Considering only the fundamental components of the magnetic fields produced by each phase set, can be written as

$$T = k_T \varphi \left(i_{q1} + i_{q2} \right) \tag{3.1}$$

where k_T torque is constant, φ is rotor flux and $i_{q1,2}$ are the q-axis inverter output currents.

In a three-level inverter, the DC-link capacitors carry load currents, resulting in unbalanced capacitor voltages. In the proposed topology, as the output currents of each inverter are 180° phase-shifted from each other, the current through each capacitor due to both inverters are also opposite in direction. If these two sets of three-phase output currents are the same, the upward (or downward) capacitor current due to inverter 1 will be cancelled by the downward (or upward) capacitor current due to inverter 2. Thus, the capacitor voltage imbalance by first inverter is naturally cancelled by the second inverter. As the capacitor voltages are balanced due to the output load current interleaving, effect of different switching sequences will not have significant impact on the capacitor balancing.

In the next section, the control strategy of the dual T-NPC inverter supplying such a dual PMSM is discussed. The control strategy, proposed in this investigation, uses the interleaved modulation strategy mentioned above. Additionally, it tries to control the output currents of each inverter to be equal, if there is any mismatch between the three-phase motor loads.

3.4 Drive Control Strategy

The control structure of the dual T-NPC inverter and the dual motor has been shown in Fig. 3-4. The dynamics of the dual T-NPC inverter and dual motor are modelled and controlled in the dq reference frame [102] - [103]. The conventional field oriented control technique has been used to control each set of the stator windings using two T-NPC inverters. As the dual PMSM has two three-phase stator winding sets with negligible mutual coupling between them, it has been modelled as two separate three-phase PMSMs. Thus, the analysis and control of each of the three-phase PMSM has been modelled in the d-q subspace [102] - [104] only. Though the three-phase machine has two sets of windings fed by two inverters, the controller receives a single speed reference to operate under a given load torque. As shown, the speed controller, the flux-weakening controller and the torque controller regulates the speed of the system and generates the reference d/q-axis currents (i_{dqref}). Depending on the d/q-axis reference and measured

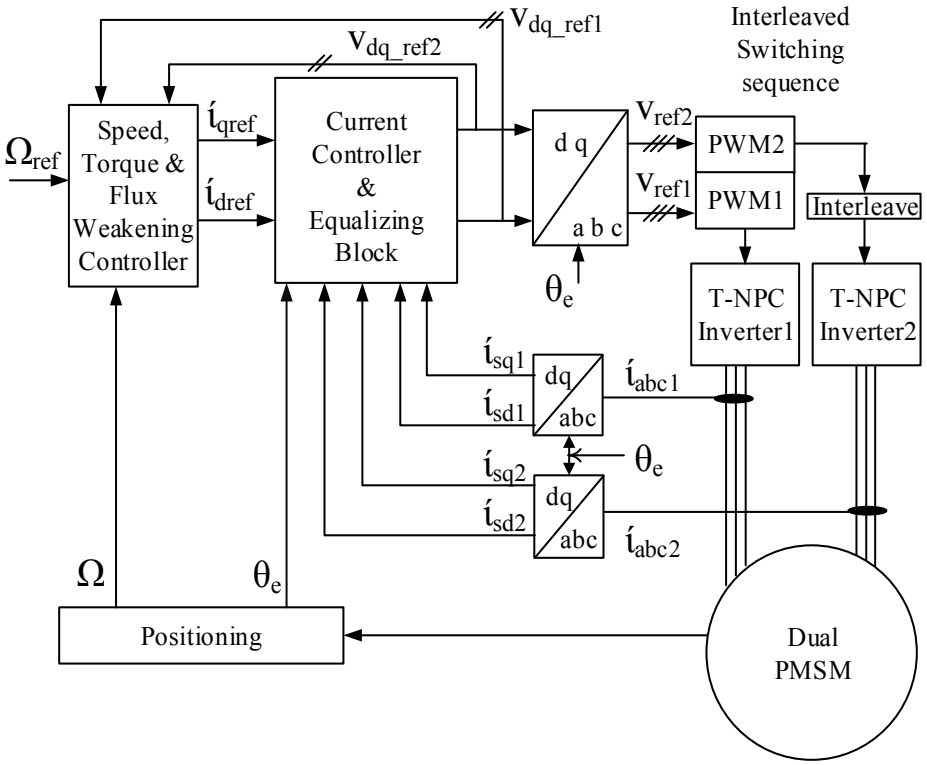


Figure 3-4. Overall control strategy of the dual inverter system

currents, the controller generates the reference voltage for both inverters. As discussed earlier, f or balanced DC-link voltages, each inverter should produce three-phase currents, equal in magnitude and 180° phase-shifted from each other. The currents produced by the two inverters may not be equal due to several reasons which include: 1) Inverter drift due to non-idealities (mismatch of pulse-patterns) and 2) dual motor non-idealities (mismatch of load magnitudes). To attain equalization of the output currents, an equalizing current control is proposed in this study.

Let us consider the following d-q current variables: $i_{d1}, i_{d2}, i_{q1}, i_{q2}$ which are the d-q axis currents of inverter 1 and inverter 2. Using scalar notation, the dq model of the PMSM in the synchronous rotor reference frame is

$$\begin{bmatrix} v_{di} \\ v_{qi} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{di} \\ i_{qi} \end{bmatrix} + R\begin{bmatrix} i_{di} \\ i_{qi} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_e L \\ \omega_e L & 0 \end{bmatrix}\begin{bmatrix} i_{di} \\ i_{qi} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_e \lambda_f \end{bmatrix} \tag{3.2}$$

for i = 1,2

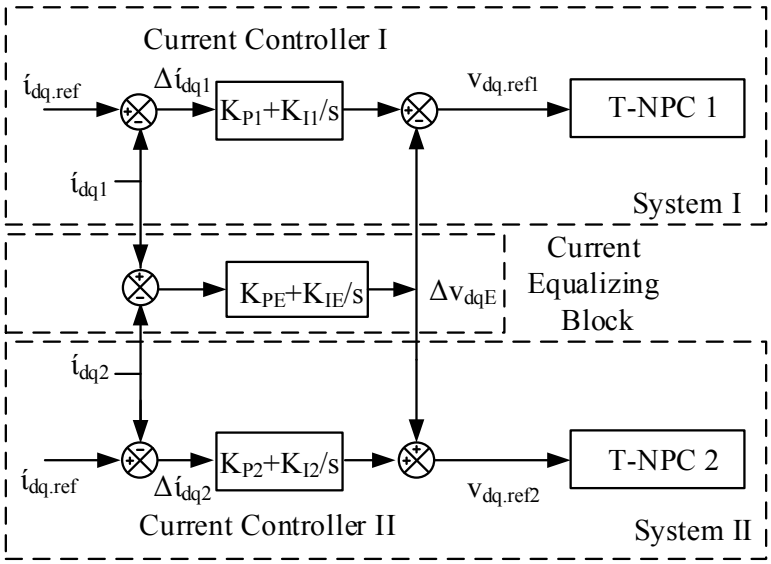


Figure 3-5. Control strategy for nullifying mismatch

where $v_{d1}, v_{d2}, v_{q1}, v_{q2}$ the d-q axis voltages are produced by the inverter 1 and inverter 2 respectively. $R, L, \omega_e, \lambda_f$ are the motor winding resistance, motor d/q-axis inductance, motor electrical speed and back-emf constant.

Fig. 3-5 presents the block diagram of the dual inverter PMSM current control. One single inverter with the corresponding set of three-phase stator windings has been considered as a system. Let us consider that the current produced by system 2 (i_{dq2}) gets deviated by an amount Δi_{dq} from the system 1 current (i_{dq1}). This relative error can be due to inverter or dual motor non-idealities. Due to this current deviation, the DC-link capacitors may become unbalanced. So, the input voltage of the second inverter (v_{dq2}) also gets deviated from the input voltage of the first inverter (v_{dq1}). This can be expressed as:

$$\begin{bmatrix} v_{d2} \\ v_{q2} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} + R\begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} + \begin{bmatrix} 0 & -\omega_e L \\ \omega_e L & 0 \end{bmatrix}\begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} + \begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix} \tag{3.3}$$

Hence, the output voltage deviation due to the output current deviation can be written as:

$$\Delta v_{dq} = L\frac{d\Delta i_{dq}}{dt} + R\Delta i_{dq} + j\omega_e L\Delta i_{dq} \tag{3.4}$$

As seen from (3.4), a deviation in the d-axis (or q-axis) current magnitude affects the d-axis and q-axis voltage references. If the inverters' input reference voltages are adjusted depending on the magnitude and polarity of the d/q-axis current deviation, the current through each inverter can be controlled to have the same magnitude.

As shown in Fig. 3-5, the proposed current equalizing block feeds the difference between measured d-axis and q-axis currents of two inverters to two proportional-integral (PI) controllers. The outputs of the PI controllers are added to the input reference voltages (v_{dqref}) of the inverters such that if the system 1 outputs more current than the system 2, the controller will lower first inverter's input reference voltage. Mathematically, the modified reference voltage of inverter 1 is

$$v_{dqref1} = K_{P1}\left(i_{dqref} - i_{dq1}\right) + K_{I1}\int\left(i_{dqref} - i_{dq1}\right)dt - K_{IE}\int\left(i_{dq2} - i_{dq1}\right)dt + j\omega_e\left(Li_{dq} + \lambda_f\right) \quad (3.5)$$

Thus, using this current equalizing block, each inverters' output current attains its reference current while regulating the relative error between them, if any.

After obtaining the d/q-axis reference voltages of two inverters, they are transformed into reference modulating voltages in ABC frame of reference. The modulating voltages are fed into the three-level modulation block to produce the gating pulses of the switching devices. As shown in Fig. 3-3, the gating pulses produced for inverter 1 are fed straight to each of the corresponding devices. On the other hand, the gating pulses produced for inverter 2 are fed to an interleave block which changes the switching sequence such that T24 and T23 receive gate pulse of T21 and T22, respectively. This interleaving creates a 180° shifted output current of inverter 2 compared to that of the inverter 1.

3.5 Simulation Results

The dual T-NPC inverter dual PMSM topology is simulated and controlled using the modulation and control strategies. An equivalent representation of the dual motor was modeled using two three-phase motors as the respective three-phase stator winding sets have negligible

mutual coupling between them. The simulation system has been modelled using the following software: 1) MATLAB/Simulink – used to implement the modulation and drive control strategies, 2) Infolytica/MotorSolve – used to model each three-phase PMSM having 10 poles, and 3) PSIM – used to simulate the T-NPC inverter and to provide inverter losses using its extensive device database. The motor and inverter models are co-simulated with Simulink using the following: 1) MotorSolve/Simulink plug-in, and 2) PSIM's Sim-coupler module.

The operation of the topology and control loop has been evaluated using three metrics, which are: 1) Capacitor voltage deviation, 2) Capacitor RMS current stress, and 3) Impact on drive efficiency. The parameters of the simulation model are as follows: - DC-link voltage is 700 V, switching frequency is 4 kHz, and the total DC-link capacitance is 220 µF. In steady state, the motors are running at a speed of 3000 RPM which for a 10-pole motor, results in 250 Hz output fundamental frequency. Comparisons have been done with a single T-NPC inverter feeding a single PMSM.

3.5.1 Capacitor Voltage Deviation

3.5.1.1 Steady-State Operation

Fig. 3-6 shows the comparison of steady state operation of four scenarios: 1) Scenario I: Single T-NPC inverter operating with SVPWM technique having additional switching instances employing redundant voltage vectors [98], 2) Scenario II: Single T-NPC inverter operating with DPWMA type three-level discontinuous PWM (DPWM) technique [105], 3) Scenario III: Dual T-NPC inverter operating with an SVPWM sequence without the additional switching instances of scenario I, and 4) Scenario IV: Dual T-NPC inverter operating with the DPWMA sequence.

For scenario I, as shown in Fig. 3-6 (i), a 50 V DC-link capacitor voltage deviation is observed with 9 switching pulses for T11 IGBT. Similarly, for scenario II, as shown in Fig. 3-6 (ii), around 80 V DC-link capacitor voltage deviation is observed with 6 switching pulses for T11 IGBT. On the other hand, for scenario III, as shown in Fig. 3-6 (iii), the output current of one inverter is 180° phase shifted from the output current of the second inverter, resulting in naturally balanced DC-link capacitor voltages (as explained in Appendix A, section A.5). Also, T11 IGBT incurs 8

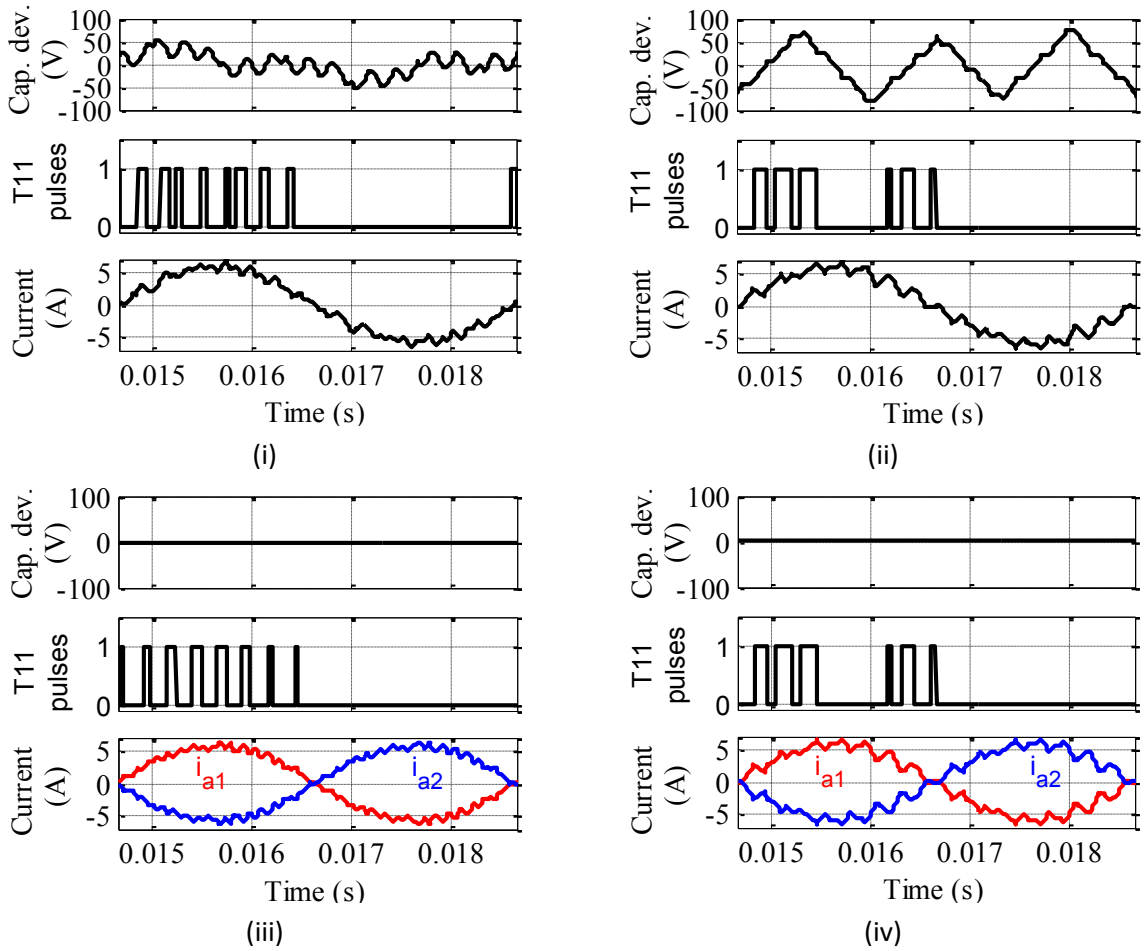


Figure 3-6. Capacitor voltage deviation, number of IGBT pulses and output line currents: (i) Single T-NPC with SVPWM employing passive capacitor voltage balancing, (ii) Single T-NPC with DPWM with no capacitor voltage balancing ability, (iii) Dual T-NPC with SVPWM having no additional switching instances, and (iv) Dual T-NPC with DPWM with no capacitor voltage balancing ability.

switching instances. Thus, it avoids 1 additional switching instance, a 12.5% reduction per IGBT. Similarly, for scenario IV, as shown in Fig. 3-6 (iv), the output current of one inverter is 180° phase shifted from the output current of the second inverter, resulting in naturally balanced DC-link capacitor voltages. T11 IGBT incurs 6 switching instances due to use of DPWM technique. Thus, the dual T-NPC inverter topology avoids additional switching instances and can also operate with discontinuous PWM strategies without impacting DC-link capacitor voltage balancing.

3.5.1.2 Transient Operation

Fig. 3-7 shows the transient waveforms for the machine speed, machine torque and the DC-link capacitor voltage difference as the dual PMSM goes from 4000 RPM to 8000 RPM speed

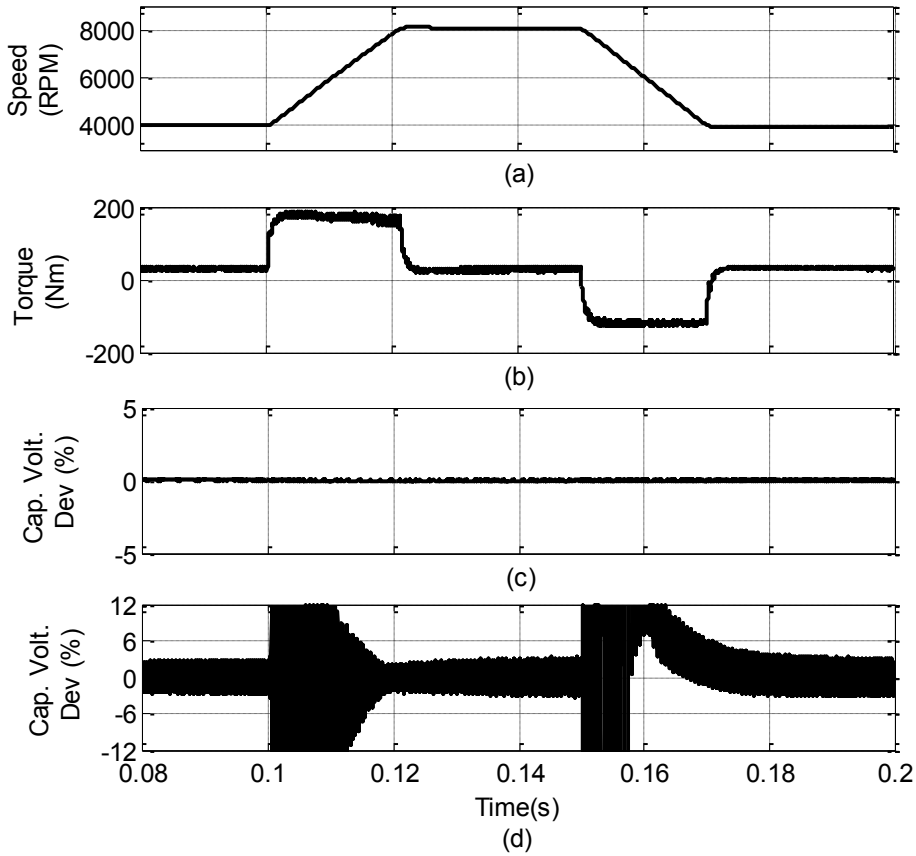


Figure 3-7. Transient Operation: (a) Speed Profile, (b) Torque profile, Capacitor voltage deviation with (c) dual T-NPC and (d) single T-NPC

and back to 4000 RPM speed. Even with such transient conditions; balanced DC-link capacitor voltages can be maintained. On the other hand, with a single T-NPC running with an SVPWM technique having capacitor voltage balancing ability, the DC-link capacitor voltages are not regulated within a tolerable band during transient operation.

3.5.1.3 Operation with Unbalance in Three-Phase Stator Windings

To validate the proposed control strategy in the presence of mismatches between two sets of stator windings in terms of stator winding flux linkages, the leakage inductance of one set of three-phase windings has been increased by 10%. An exaggerated increase has been considered to check the effect of the mismatch on different output variables of the system. In Fig. 3-7, Fig. 3-8, effect of impedance mismatches is shown. With the leakage inductance mismatch, the controller readjusts the output voltages such that the current produced by each

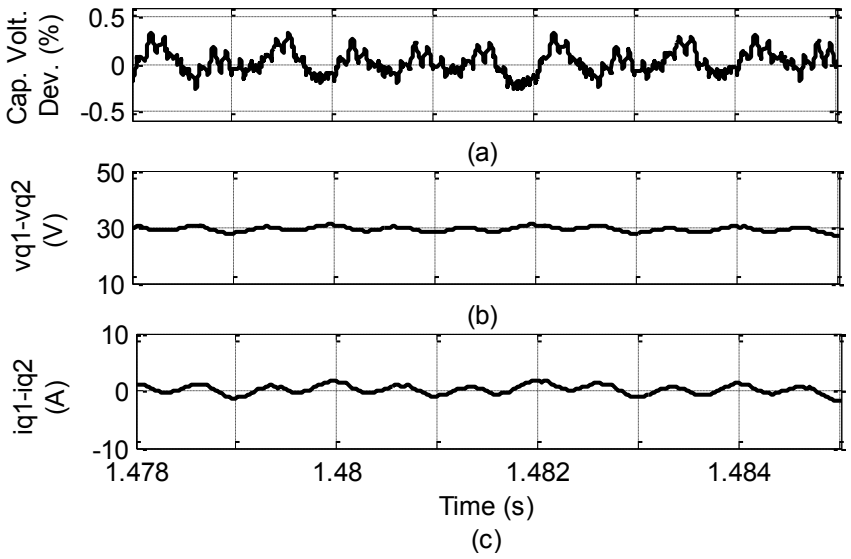


Figure 3-8. Operation with unbalance in winding impedance: (a) Capacitor voltage Difference, (b) q-axis voltage difference, (c) q-axis current difference

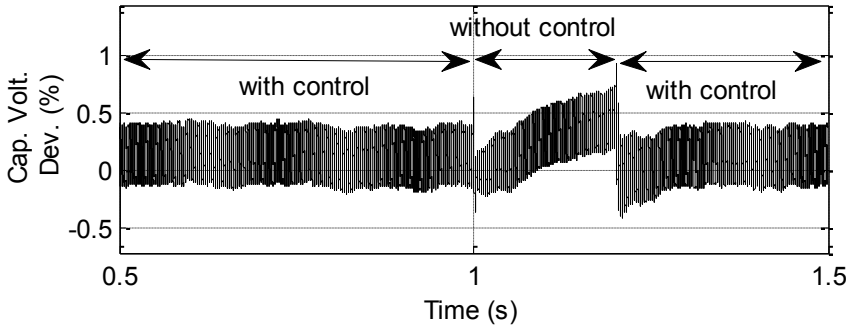


Figure 3-9. Effect of the controller in maintaining balancing

inverter is same, thus maintaining DC-link capacitors' voltages balanced. Even with a 10% impedance mismatch, the capacitor voltage deviation remains within a limit, whereas the difference between q-axis voltages of two inverters is increased to take care of the impedance mismatch. By changing the reference voltage magnitude, the output currents and the neutral point currents are maintained equal, resulting in reduction in combined ripple current through the DC-link neutral point and reduced capacitor voltage deviation.

3.5.2 Current Stress of DC-link Capacitors

In a three-level inverter, the DC-link capacitors carry the output load current when the neutral point is connected to a phase. This is shown in Fig. 3-10 (a) with the help of DC-link neutral current whose RMS magnitude is around 70-75% of the output load current. This is also explained

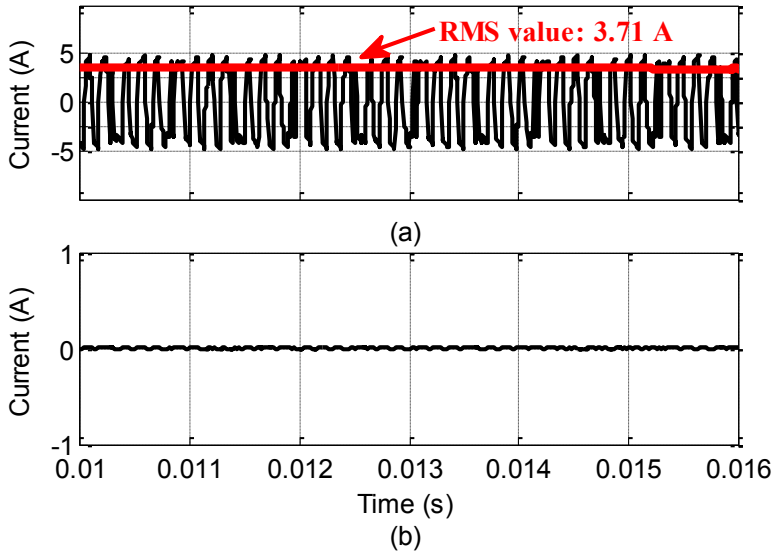


Figure 3-10. DC-link neutral current (a) Single T-NPC inverter fed PMSM (b) Dual T-NPC inverter fed dual PMSM

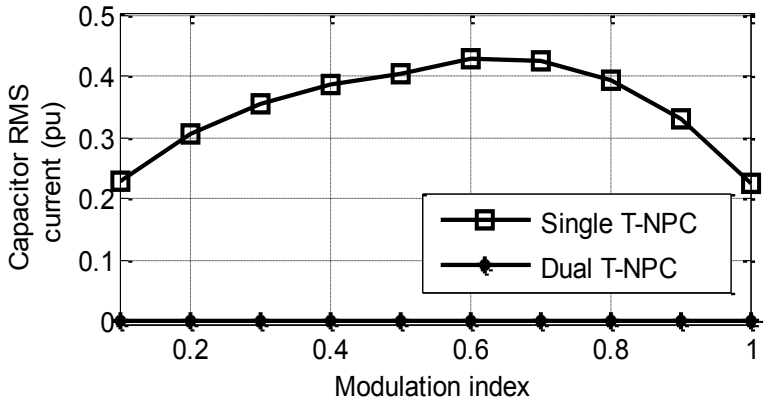


Figure 3-11. Difference in DC-link capacitor RMS current

with few equations in Appendix A, section A.5. So, each of the DC-link capacitors carries around 35% output RMS current [106]. However, as shown in Fig. 3-10 (b), in the proposed dual T-NPC inverter, the current through the DC-link neutral is negligible.

Fig. 3-11 shows the difference between current through DC-link capacitors of a single T-NPC inverter and the proposed dual T-NPC inverter, over a complete range of operating modulation index. It shows that the RMS current of the DC-link capacitors of a single T-NPC inverter is about 25-45% of the output load current. In contrast, the RMS current of the DC-link capacitors of the proposed topology is reduced by 95-97%.

3.5.3 Impact on Drive Efficiency

In the proposed topology, the DC-link capacitor voltages are naturally balanced using interleaved output load currents, whereas in the conventional three-level topology, additional switching transitions are needed to balance the capacitor voltages. Fig. 3-12 shows the impact of the proposed topology on the reduction of the switching losses and overall inverter loses in comparison to conventional three-level topology. The loss comparison has been conducted for unity modulation index, 600 Hz fundamental frequency and 7.2 kHz switching frequency. The inverter conduction and switching losses have been measured using PSIM. The loss models are discussed in Appendix A, section A.7. The proposed topology reduces the switching losses by 9% and overall losses by 4.5 %. This loss reduction is attributed to absence of additional switching instances to balance DC-link capacitor voltages.

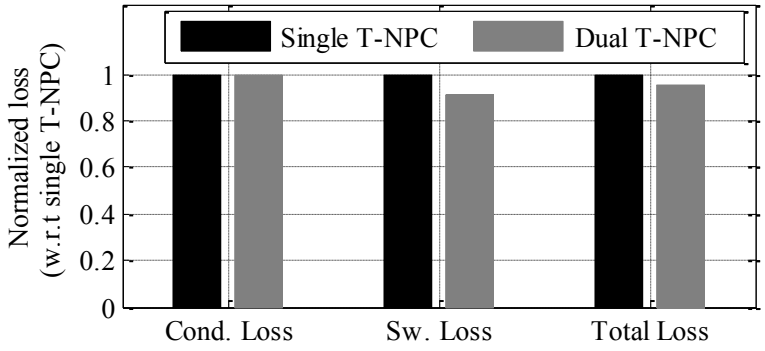


Figure 3-12. Loss reduction using Dual T-NPC topology operating with DPWM techniques

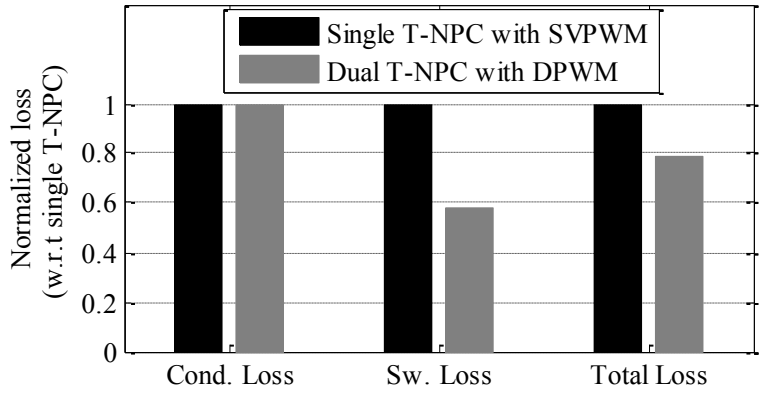


Figure 3-13. Loss reduction using Dual T-NPC topology due to absence of additional switching instances as in single T-NPC topology

This provides the topology an additional degree of freedom to use sophisticated modulation strategies such as discontinuous PWM schemes [105] to further reduce inverter losses. As these discontinuous PWM schemes do not have any ability to balance capacitor voltages, conventional three-level inverter topologies typically cannot use them without compromising a balanced DC-link [52], [58], [105]. Fig. 3-13 shows the impact of the switching scheme on the reduction of the switching losses and overall losses of the inverter topologies for similar operating conditions as before. The discontinuous PWM schemes used with the proposed dual T-NPC topology reduces overall converter loss by 20 % compared with a single T-NPC topology operating with SVPWM technique with passive capacitor voltage balancing capability.

The simulation results have been summarised in Table 3-2.

TABLE 3-1: SUMMARY OF SIMULATION RESULTS

Case	Number of pulses	Cap. Voltage deviation (V)	Cap. RMS current (A)
Single TNPC - SVPWM	9	50	3.71
Single T-NPC - DPWM	6	60	-
Dual TNPC - SVPWM	8	0	0
Dual T-NPC - DPWM	6	0	-

3.6 Experimental Setup and Results

The proposed dual T-NPC inverter fed dual PMSM topology and its modulation and control strategy are evaluated on a scaled-down experimental setup, shown in Fig. 3-14. The setup consists of two three-level T-NPC inverters feeding a dual three-phase PMSM. The motor parameter data are provided in Table 3-1.

The following capabilities of the proposed topology have been validated: 1) Balanced DC-link capacitors' voltages, 2) Reduced capacitor current stress, and 3) Inverter loss reduction. The

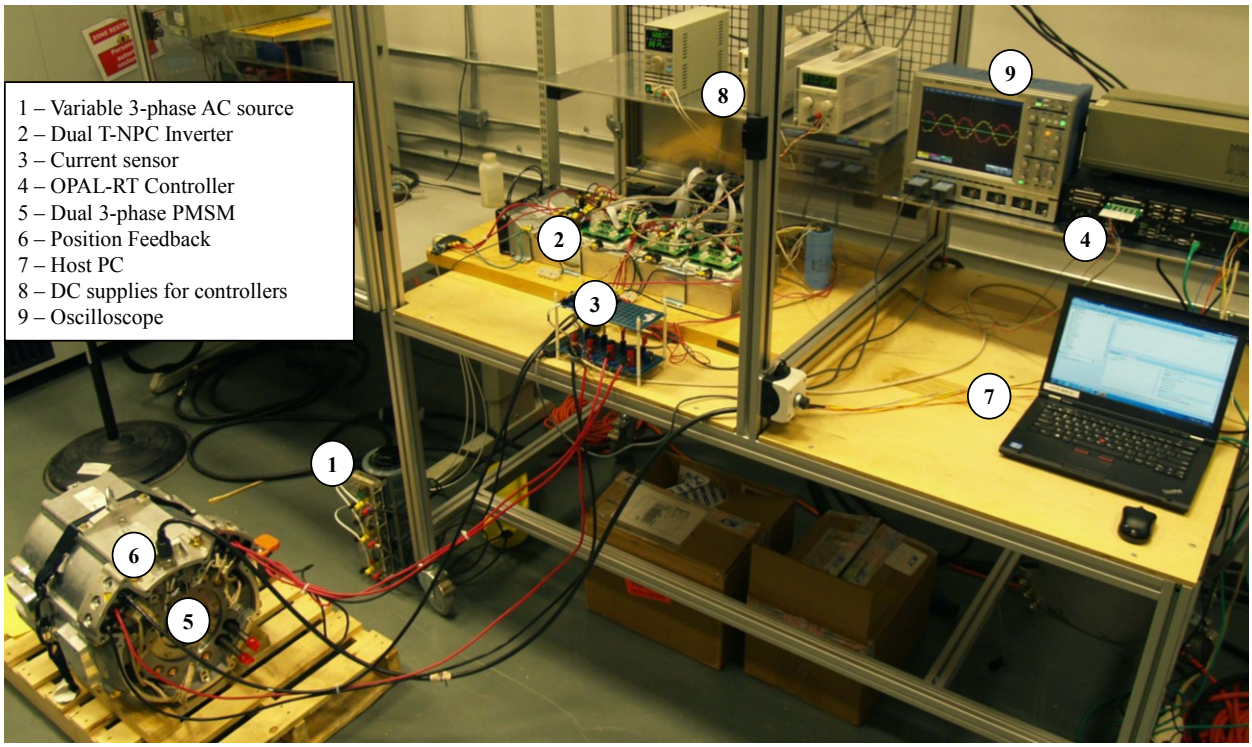


Figure 3-14. Experimental setup of the dual three-level T-NPC inverter fed dual PMSM topology

control strategies are implemented using OPAL-RT based real time prototyping tool. The operational time-step is 25 µs. The switching frequency of the inverters is 4 kHz, the dead time is 1 µs, the DC-link voltage is 200 V, the maximum output phase current is 5 A and the DC-link capacitance is 220 µF.

Figs. 3-15, 3-16 show the performance of the proposed inverter with a comparison of capacitor voltage deviation and output current for two cases: 1) A single T-NPC inverter running

TABLE 3-2: MACHINE PARAMETERS

Parameters	Values
Nominal motor voltage	450 V
Nominal motor power	150 kW
Base speed	2100 RPM
Number of poles	16
Self-inductance of each phase-set	0.4 p.u.
Mutual inductance between two sets of windings	Negligible

only one set of the dual three-phase PMSM, and 2) The dual T-NPC inverter running the dual three-phase PMSM. The following observations have been made:

- In the first case, as shown in Fig. 3-15, the single T-NPC inverter is supplying 5 A current to one set of the dual three-phase motor. Similar to the simulation results, the capacitor voltage deviation is around 50 V.
- In the second case, as shown in Fig. 3-16, the dual T-NPC inverters are supplying 5 A current to both sets of the dual three-phase motor. Similar to the simulation results, the corresponding output currents are interleaved (i.e. the output currents are 180° phase shifted

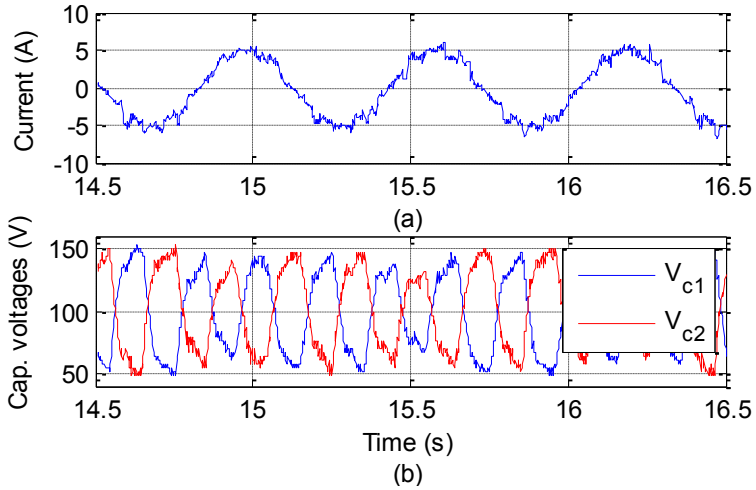


Figure 3-15. Experimental results of single T-NPC inverter fed PMSM (V_{dc}: 200 V, output current: 5A) - (a) line current (b) capacitor voltages

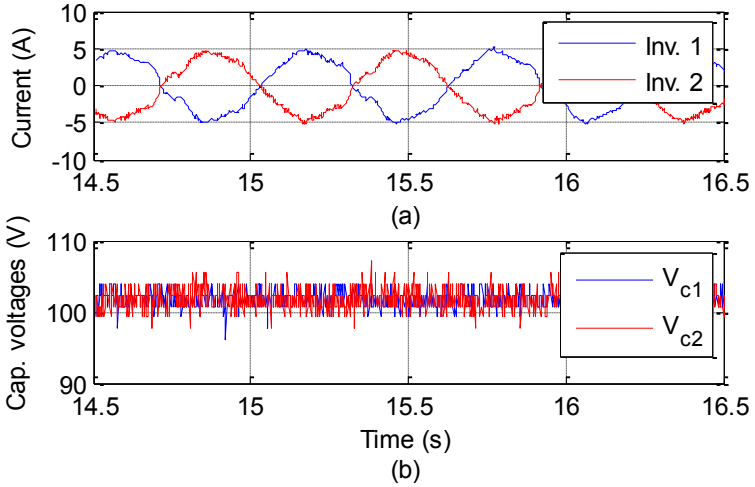


Figure 3-16. Experimental results of dual T-NPC inverter fed dual PMSM (V_{dc}: 200 V, o/p current: 5A) - (a) line currents (b) capacitor voltages

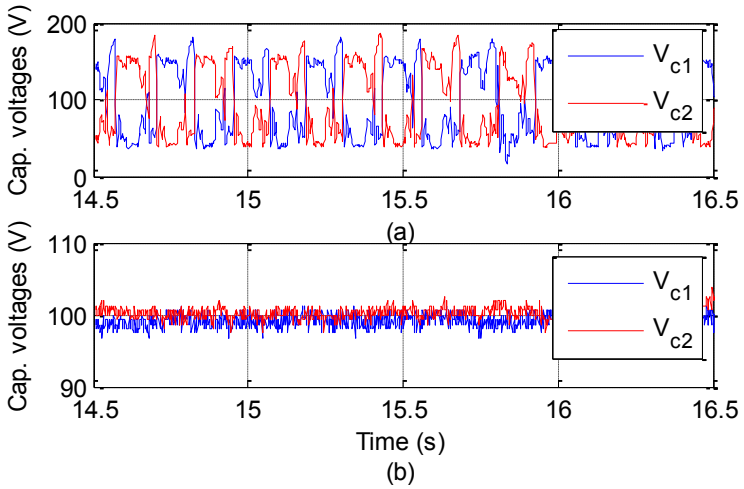


Figure 3-17. Experimental DC-link capacitor voltages with discontinuous PWM strategy (V_{dc}: 200 V, output current of a single inverter: 5A) - (a) Single T-NPC inverter fed PMSM (b) Dual T-NPC inverter fed dual PMSM

from each other) and the DC-link capacitor voltages are balanced around the nominal voltage, reducing capacitor voltage deviation by 90-95%.

The capacitor voltage deviation distorts the inverter output voltage waveforms and that results in increased output current distortion. It can be seen from Figs. 3-15, 3-16, that with a dual T-NPC topology maintaining nominal split capacitor voltages, the output currents' distortion reduces. It should be noted that, in the experimental setup, the DC voltage is directly provided from the output of a three-phase diode rectifier, instead of a battery. Thus, the harmonics generated due to the rectification have been propagated to the inverters' outputs, degrading current waveform quality. In an industrial setup of the proposed topology, a stiff DC-link voltage may be provided from a multi-pulse rectifier or a DC battery along with additional filters.

Fig. 3-17 shows the impact of three-level DPWM technique [105] on the capacitor voltage deviation for the two cases. Like the simulation results, for the single inverter fed PMSM, the capacitor voltage deviation is around 70-80 V, whereas, with the dual T-NPC inverter fed dual PMSM, the DC-link capacitor voltages remain balanced around the nominal voltage.

Figs. 3-18, 3-19 show the impact on the DC-link neutral current and DC-link positive bus current for the two cases. The following observations have been made:

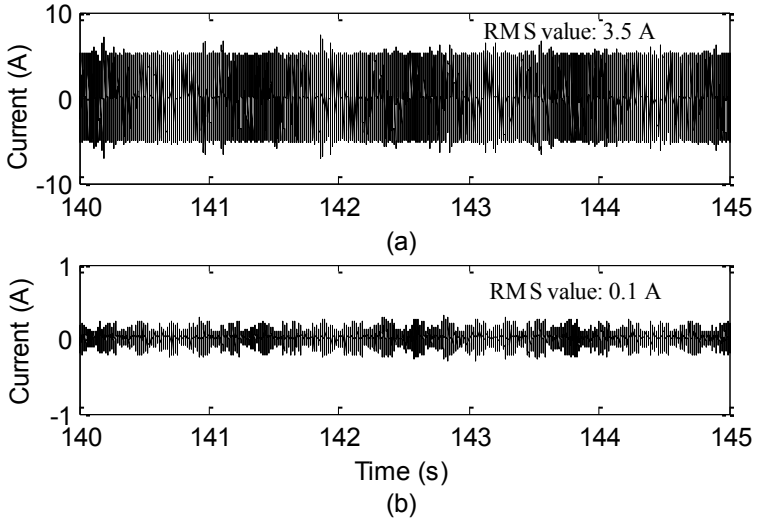


Figure 3-18. Experimental results of DC-link capacitor current dual T-NPC inverter fed dual PMSM (V_{dc}: 200 V, output current of each inverter: 5A) - (a) Single T-NPC inverter fed PMSM (b) Dual T-NPC inverter fed dual PMSM

- In the first case, as shown in Fig. 3-18(a), the RMS value of the DC-link neutral current is 3.5 A which is 70 % of the load current. Thus, the RMS DC-link capacitor current is around 35% of the load current [101], like the simulation results in section IV. On the other hand, with the dual T-NPC dual PMSM topology, as shown in Fig. 3-18(b), the RMS value of the DC-link neutral current is 0.1 A, a 97% reduction compared to the previous case, although the drive provides double the amount of power to the dual PMSM compared to the earlier case.

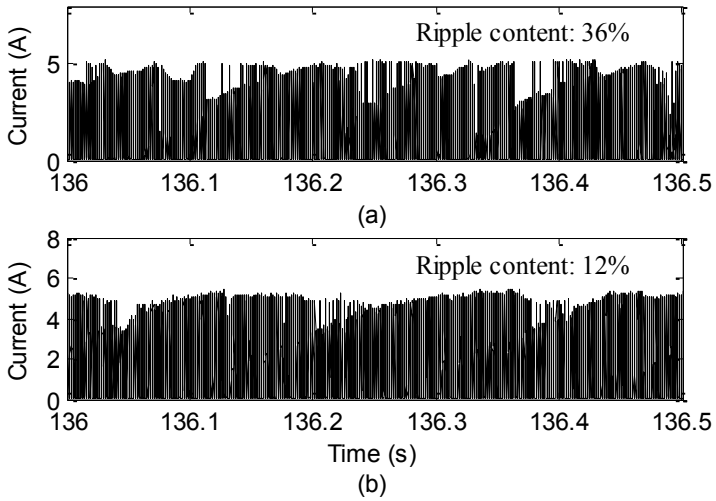


Figure 3-19. Experimental DC-bus current (output current of a single inverter : 5A) - (a) Single T-NPC inverter fed PMSM (b) Dual T-NPC inverter fed dual PMSM

- As shown in Fig. 3-19(a-b), for a single T-NPC inverter, the amount of DC-bus ripple content is 1.8 A, 36% of the load current. On the other hand, with the dual T-NPC dual PMSM topology, although the drive provides double the amount of power to the dual PMSM compared to the earlier case, the ripple current component is reduced to 1.2 A, 12% of the total load current of two inverters. Please note that in Fig. 3-19 (b), the ripple current is due to two inverters, whereas, in Fig. 3-19 (a), the ripple current is due to only one inverter.

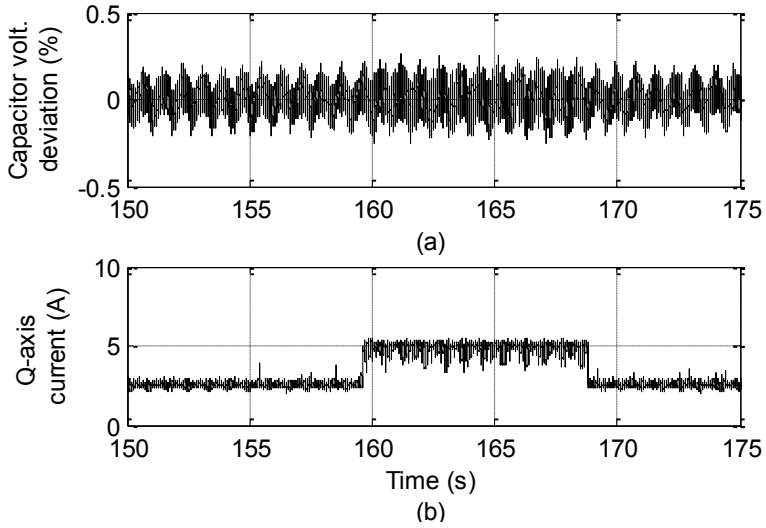


Figure 3-20. Experimental results of transient operation of dual T-NPC inverter fed dual PMSM (a) Capacitor voltage deviation (b) Change in dual motor current (from 2.5 A to 5 A)

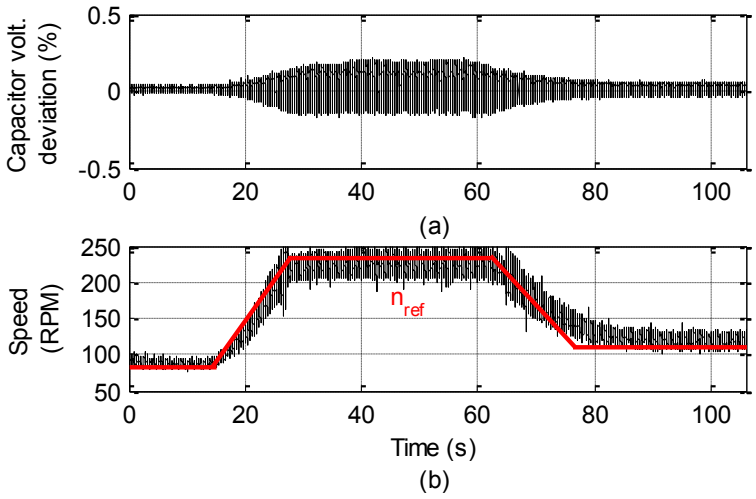


Figure 3-21. Experimental results of transient operation of dual T-NPC inverter fed dual PMSM (a) Change in speed (80 RPM→240 RPM→120 RPM) (b) Capacitor voltage deviation

Fig. 3-20, 3-21 show the performance of the proposed topology in transient conditions. Fig. 3-20 shows that during a change in the dual motor current from 2.5 A to 5 A, the DC-link capacitor voltages remain balanced. Similarly, as shown in Fig. 3-21, the reference speed of the dual motor is changed between 80 RPM, 240 RPM and 120 RPM. The dual motor attained the reference speeds and the DC-link capacitor voltages remain balanced, with around 0.2% deviation around the nominal value.

Table 3-3 summarizes the experimental results.

TABLE 3-3: SUMMARY OF EXPERIMENTAL RESULTS

Case	Cap. Voltage deviation (V)	Cap. RMS current (A)
Single TNPC - SVPWM	50	3.5
Single T-NPC - DPWM	60-65	-
Dual TNPC - SVPWM	2-3	0.1
Dual T-NPC - DPWM	2-3	-

Fig. 3-22 and Table 3-2 show the impact of the proposed topology and the control strategy on reducing inverter losses. The losses have been determined by subtracting the output AC power (calculated using inverter output line-line voltages and line currents) from the input DC power (calculated using DC input voltage and input current). The input and output power levels are shown in Table 3-2. The inverter loss reduction is in the range of – a) 3 % while operating with the SVPWM technique without additional switching instances to balance DC-link capacitor voltages and b) 16 % while operating with the DPWM technique.

3.7 Conclusion

This chapter proposes a dual three-level T-NPC inverter fed dual PMSM topology for low-voltage, high-power applications. Both simulation and experimental results show a significant improvement over the conventional single T-NPC inverter fed PMSM drive. The proposed

topology and its interleaved PWM control strategy decouple pulse-width modulation strategies of the inverters from DC-link capacitor voltage balancing and can maintain balanced DC-link capacitor voltages both during steady-state and transient conditions. Due to the interleaved control strategy, the currents through the DC-link capacitors are reduced by 90-97%. The reduced voltage deviation and current stress results in: 1) an opportunity to use a DC-link capacitor with lower current rating and 2) lower capacitor operating temperature and losses. The proposed topology reduces inverter losses by avoiding additional switching instances to balance DC-link capacitor voltages, and therefore, increases the overall efficiency of the proposed topology.

As the topology achieves balanced DC-link voltages without using conventional capacitor balancing algorithms, the topology can use different switching loss reduction schemes. Use of these schemes reduces system loss appreciably without interfering with DC-link voltages.

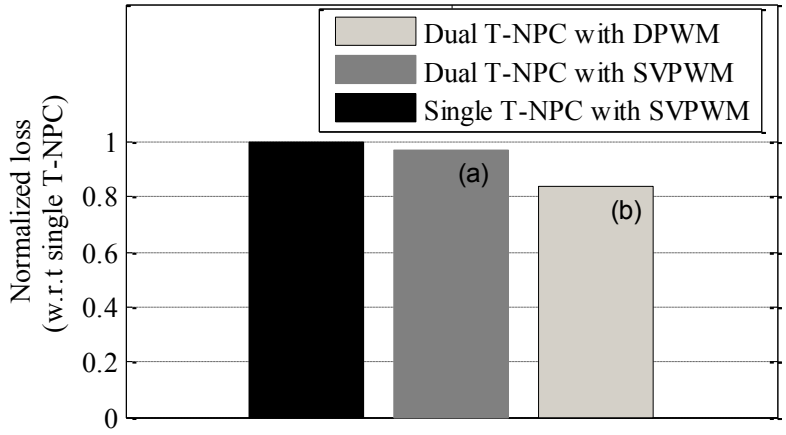


Figure 3-22. Experimental result showing inverter loss reduction using Dual T-NPC topology (output current of a single inverter: 5A, speed of the motor: 240 RPM) - (a) due to absence of additional switching instances of single T-NPC topology and (b) using DPWM technique

TABLE 3-4: EXPERIMENTALLY MEASURED INPUT AND OUTPUT POWER

System type	Input power (W)	Output power (W)	Loss (W)	Normalized loss
Single T-NPC with SVPWM	570	422	148	1
Dual T-NPC with SVPWM	1130	846	284	0.96
Dual T-NPC with DPWM	1086	846	240	0.81

Hence, in chapter 4-6, three modulation strategies have been proposed which improves the loss redistribution amongst different devices of a three-level inverter, reduces switching losses at lower power factors, and provides a variable switching frequency strategy for switching loss reduction.

4 DPWM Sequences for Device Loss and Thermal Redistribution

4.1 Overview

With conventional pulse-width modulation (PWM) strategies, the switching devices of a three-level inverter are not equally utilized. At modulation indices lower than 0.5, the inner switching devices incur more losses and higher junction temperatures, thus becoming the bottleneck in providing more output power. This chapter presents a series of space-vector based discontinuous PWM (DPWM) sequences which relocates the phase current from the inner to the outer switches of a three-level T-NPC inverter. In consequence, the sequences redistribute the device losses and junction temperatures more equally amongst the inner and outer switches.

4.2 Introduction

With conventional three-level modulation strategies [98], the inner (Tn1-Dn1 and Tn2-Dn2) and outer devices (T1-D1 and T2-D2) of a T-NPC inverter are not equally utilized [40], [107]. For example, at lower modulation indices, the inner devices carry 2-3 times higher RMS current compared to the outer devices. Moreover, referring to Fig. 4-1, there are two switches (e.g. Tn1 and Dn2) in the inner conduction path compared to only one switch (e.g. T1 or D2) in the outer conduction path. These cumulatively result in unequal loss and temperature distribution amongst the inner and outer switching devices, limiting the output current capability of the drive [108], [107] or requiring an oversized design of the inverter [109].

To overcome these – 1) A two-level SVPWM strategy has been introduced for the Neutral-Point-Clamped (NPC) inverters [107], however, it introduces additional switching losses due to alternating carrier band transitions, 2) Active- Neutral-Point-Clamped (A-NPC) topologies with additional active neutral-connected-switches [49] were introduced as a hardware solution, 3) The Neutral-Point-Piloted (NPP) topology was introduced [110] which only distributes switching losses at higher modulation indices over two outer devices and has no impact on current

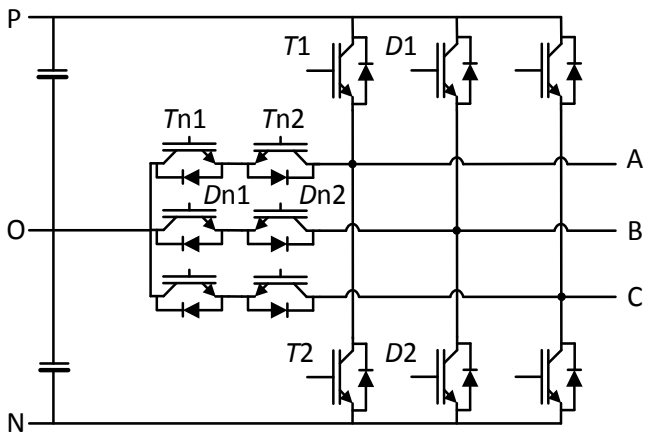


Figure 4-1. Three-level T-NPC inverter; showing the inner devices (*T*n1-*D*n1 and *T*n2-*D*n2) and outer devices (*T*1-*D*1 and *T*2-*D*2)

distribution amongst inner and outer devices at lower modulation indices as it uses conventional PWM strategies, and 4) Switching strategies to redistribute device losses of an NPC inverter were proposed in [111]- [112], being only beneficial during high reactive power operation. Moreover, these studies did not discuss any impact of different three-level discontinuous PWM (DPWM) strategies on individual devices of a three-level T-NPC inverter [52], [105].

This paper studies the distribution of losses (switching and conduction) along with junction temperatures amongst the devices of a T-NPC inverter operating with modulation indices lower than 0.5. The three-level SVPWM and DPWM templates [49]- [50], [98], [105], [113]- [117] are investigated along with their commutation and conduction profiles. A series of DPWM templates have been identified which redistribute the losses amongst the devices more equally than the other PWM strategies, and enable higher output power or higher operating switching frequency at the regions of a T-NPC inverter fed traction drive where higher inner device losses typically limit output current capability. Moreover, these improvements are obtained without requiring an oversized inverter design or compromising the waveform quality in comparison to other DPWM templates.

4.3 Conventional Three-Level Modulation Strategies

Fig. 4-2 shows the three-level space vector hexagon which is divided into six sectors (I-VI) and each sector has 4 subsectors (1-4). The subsector 1 is divided in two parts - 1a and 1b. The modulation index (m) is the ratio of the peak of the output line-line voltage to the DC-link voltage. As the focus of the paper is at modulation indices lower than 0.5, the sequences in subsector 1 of sector I-VI are only studied.

Typically, three-level inverters use the conventional continuous SVPWM sequences [98], [113], as shown in Table 4-1. The average A-phase modulation voltage [105] of the sequence is shown in Fig. 4-3(i). As this modulation pattern remains fixed for all operating conditions, impact on device losses vary with modulation indices and power factors [105].

To reduce switching losses of these inverters, DPWM strategies have been introduced in [107], [113] - [116], [49] which typically clamp each phase-leg to the neutral point of the DC-link (O) at modulation indices lower than 0.5 [107]. These sequences, named as DPWMO sequences in this study, have three variants – DPWM0O, DPWM1O and DPWM2O [116]. Referring to Fig. 4-2, their characteristics are: i) DPWM0O – A-phase clamping at sectors III, VI, ii) DPWM1O – A-phase clamping at subsectors 1b of sectors I, IV, subsectors 1a of sectors III, VI, and iii) DPWM2O

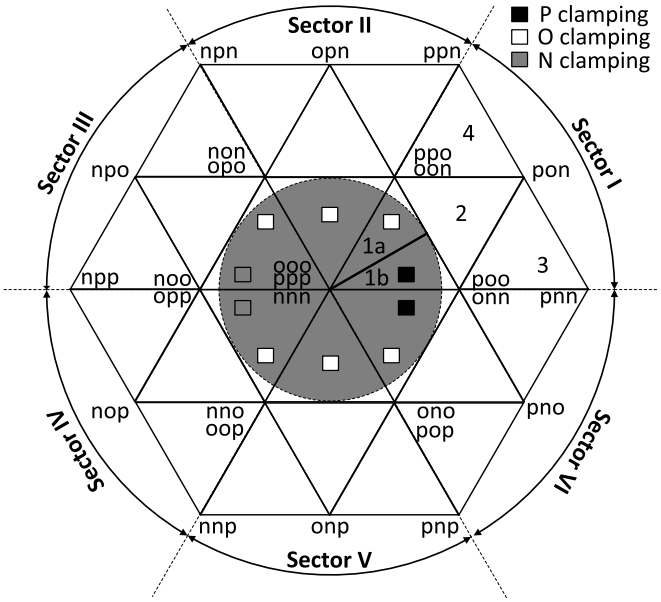


Figure 4-2. Three-level space-vector hexagon with A-phase clamping possibilities; shaded region is for modulation index ≤ 0.5

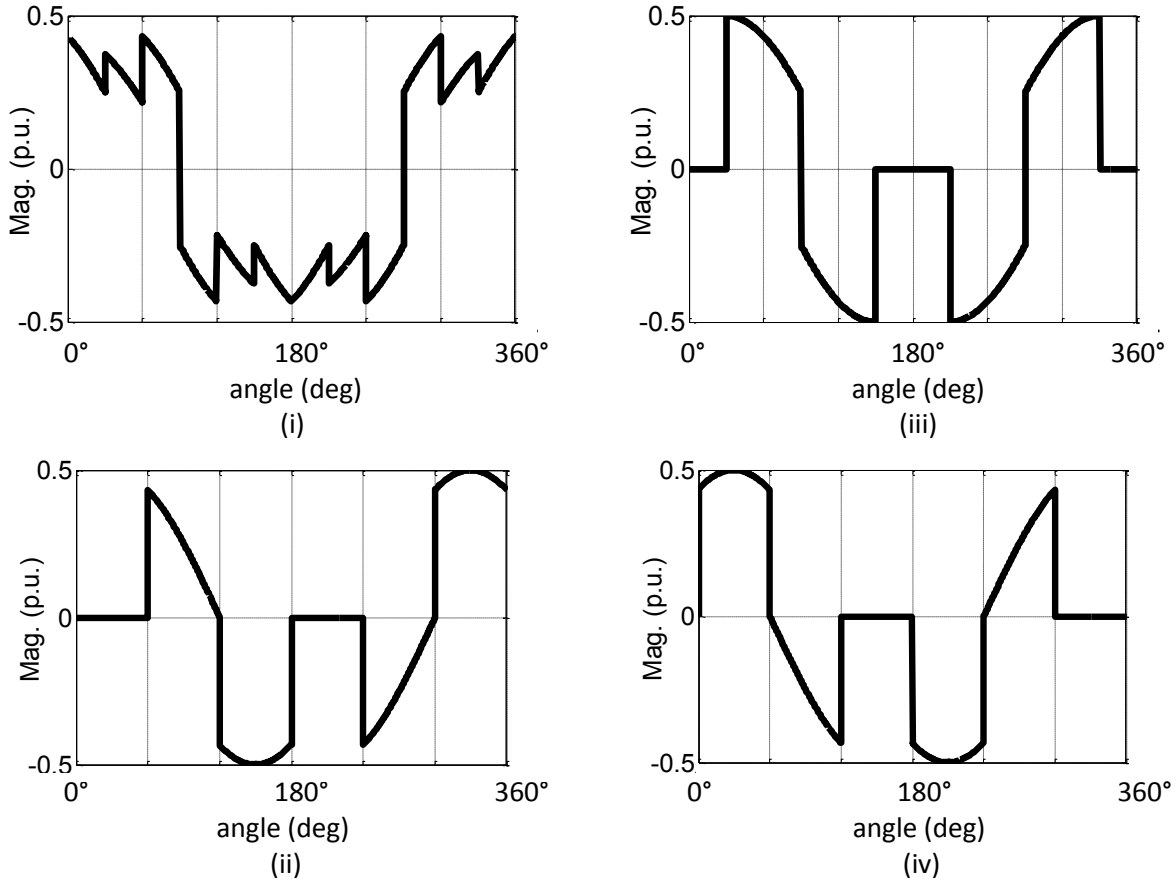


Figure 4-3. Average A-phase to DC-link neutral voltage waveforms for modulation index less than 0.5, normalized w.r.t DC-link voltage for conventional PWM templates - (i) SVPWM ; (ii) *DPWM2O*; (iii) *DPWM1O*; (iv) *DPWM0O* ; 0.5 signifies half DC-link voltage

– A-phase clamping at sectors I, IV. These DPWMO sequences have been shown in Table 4-1 and the average A-phase modulation voltage waveforms along with the clamping intervals are shown in Fig. 4-3(ii-iv).

However, as these three-level DPWMO strategies clamp each phase-leg to the neutral point of the DC-link, they increase the current through the inner devices during the clamping intervals. This increased current aggravates the unequal distribution of phase-current and device losses associated with the conventional SVPWM sequences.

4.4 Three-Level DPWMPN Strategies: Analysis

Referring to Fig. 4-2, the switching vectors for $m \leq 0.5$ shows that the phase A can be clamped to the positive DC-bus (P) in the subsector 1 of sector I and VI, and to the negative DC-

TABLE 4-1: CONVENTIONAL AND INVESTIGATED THREE-LEVEL SWITCHING TEMPLATES

Strategy		Optimum pf	Sector I		Sector II	
			Subsector 1a	Subsector 1b	Subsector 1a	Subsector 1b
SVPWM		-	(POO↔OOO ↔ OON↔ONN)	(OON↔OOO ↔ POO↔PPO)	(OON↔OOO ↔ OPO↔PPO)	(OPO↔OOO ↔ OON↔ONN)
DPWMO	*DPWM0O*	30° lead	(OOO↔POO ↔ PPO)	(OOO↔POO ↔ PPO)	(OOO↔OON ↔NON)	(OOO↔OON ↔ NON)
	DPWM1O	unity	(OOO↔OON ↔ ONN)	(OOO↔POO ↔ PPO)	(OOO↔OPO ↔PPO)	(OOO↔OON ↔ NON)
	DPWM2O	30° lag	(OOO↔OON ↔ ONN)	(OOO↔OON ↔ ONN)	(OOO↔OPO ↔PPO)	(OOO↔OPO ↔PPO)
DPWMPN	*DPWM0PN*	30° lead	(OON↔ONN ↔ NNN)	(OON↔ONN ↔ NNN)	(OPO↔PPO↔ PPP)	(OPO↔PPO↔ PPP)
	DPWM1PN	unity	(POO↔PPO↔ PPP)	(OON↔ONN ↔NNN)	(OON↔NON ↔ NNN)	(OPO↔PPO↔ PPP)
	DPWM2PN	30° lag	(POO↔PPO↔ PPP)	(POO↔PPO↔ PPP)	(OON↔NON ↔ NNN)	(OON↔NON ↔ NNN)

1. POO signifies that A-phase is connected to 'P', B phase is connected to 'O', and C phase is connected to 'O'
2. The double-sided arrow signifies that the switching sequence is only for half switching cycle and it follows the opposite direction in the other half. The complete sequence of (POO↔OOO↔OON↔ONN) is - (POO→OOO→OON→ONN→OON→OOO→POO)

bus (N) in the subsector 1 of sector III and IV [50]. Referring to Fig. 4-1, if the phases are clamped only to the positive/negative DC bus instead of the DC-link neutral point - 1) the current flows through a single switch (for example, T1 or D2) during the clamping interval, and 2) the conduction time of the devices connected to the neutral path reduces appreciably.

Switching sequences arising out of this possibility are named as DPWMPN sequence and like the DPWMO sequences, these can have three variants – i) DPWM0PN – A-phase PN clamping at sectors III, VI, ii) DPWM1PN – A-phase PN clamping at subsectors 1b of sectors I, IV, subsectors 1a of sectors III, VI, and iii) DPWM2PN – A-phase PN clamping at sectors I, IV. These sequences are listed in Table 4-1 and the average A-phase modulation voltage waveforms along with the clamping intervals are shown in Fig. 4-4(i-iii).

The investigated switching strategies are variants of three-level DPWM strategies, thus they are able to reduce switching losses of the devices. Moreover, they provide PN clamping,

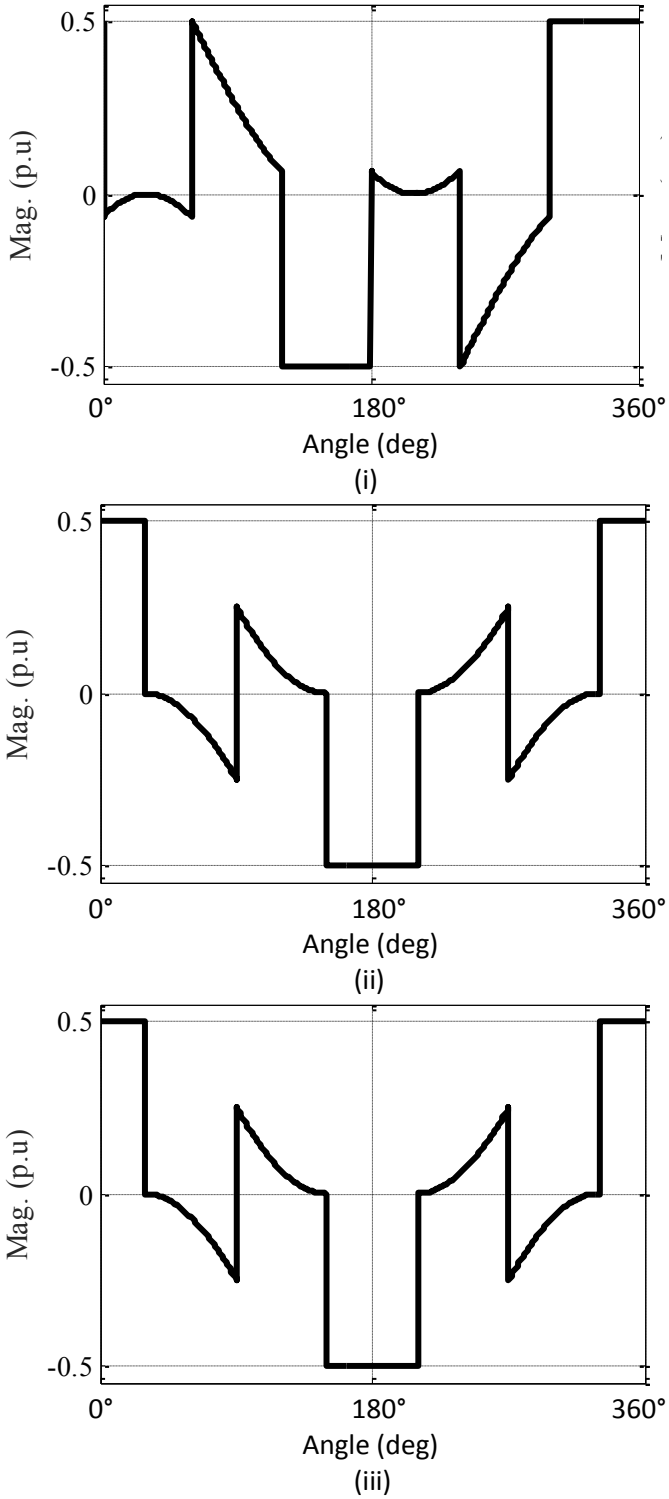


Figure 4-4. Average phase to DC-link neutral voltage waveforms for modulation index less than 0.5, normalized w.r.t DC-link voltage - (i) *DPWM0PN*; (vi) *DPWM1PN*; (vii) *DPWM2PN*

instead of O clamping, thus relocating the phase current and the resulting device conduction losses from the inner devices to the outer devices during clamping intervals.

It should be noted that in contrast to the T-NPC inverter, in a conventional NPC inverter, the inner IGBTs always conduct irrespective of the switching sequence [49]. Hence, in that topology, the DPWMPN templates will have no impact on current distribution between the inner and outer IGBT devices, and may only reduce the conduction losses of the neutral-point connected diodes at lower modulation indices; however, this is out-of-scope of this investigation.

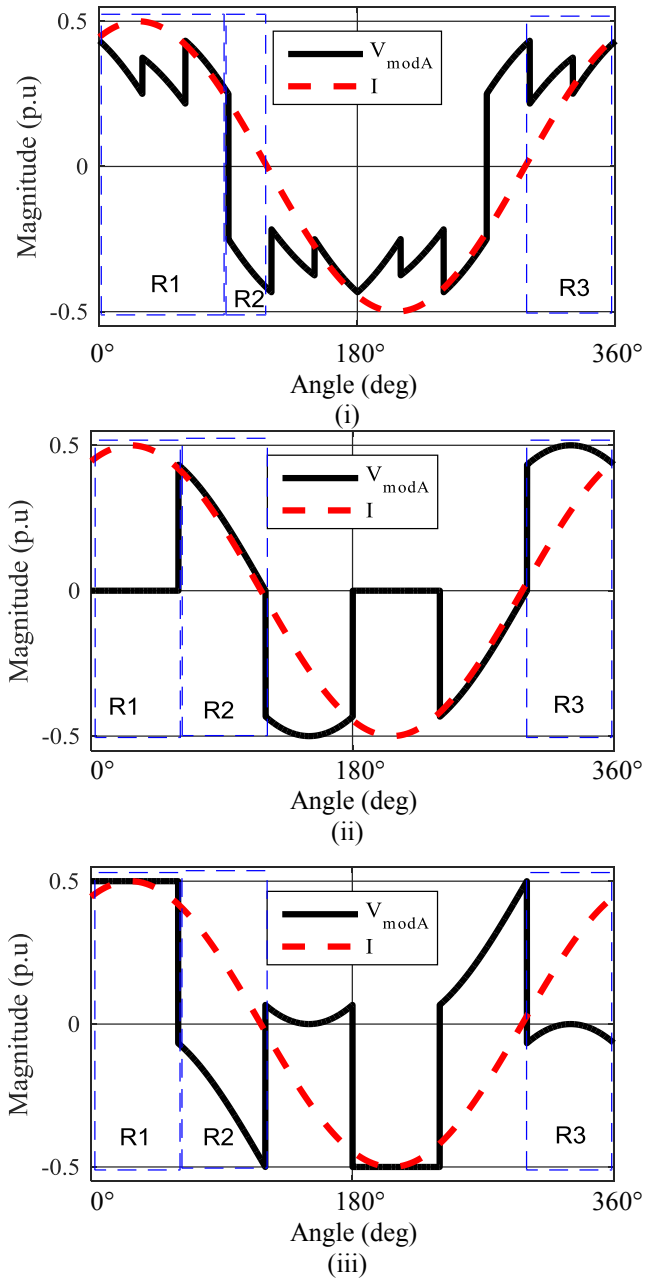


Figure 4-5. Average phase to DC-link neutral voltage waveforms and current waveforms for (i) SVPWM, (ii) DPWM2O, and (iii) DPWM2PN for 30° power factor angle. It shows the regions (R1, R2 and R3) in the positive half-cycle of the current. The regions siginify different possibilities of device conducting.

4.4.1 Operation: Conduction and Commutation Profile

Referring to Fig. 4-1, in each phase leg of a T-NPC inverter, there are four IGBT-diode pairs. In the positive fundamental cycle of the A-phase current, T1, Tn1, Dn2 and D2 only conduct. In Fig. 4-5 (i-iii), the average a-phase modulation voltage and a-phase current for the PWM strategies are shown. The observations are as following – (i) SVPWM – In the region 1 and 3 (R1 and R3), the modulating voltage and current is positive, thus T1, Tn1 and Dn2 conduct and commutate amongst them. However, the device Tn1 does not experience any switching loss as the modulating voltage is positive [52]. Hence, in these regions, T1 and Dn2 experience both conduction and switching losses whereas Tn1 only incurs conduction losses. In the region 2 (R2), the modulating voltage is negative and current is positive; thus Tn1, Dn2 and D2 conduct and commutate amongst them. The device Tn1 experiences switching loss as the modulating voltage is negative [52]. Hence, in this region, Tn1, Dn2 and D2 experience conduction and switching losses. (ii) DPWMO – In R1, due to clamping, no device experiences switching losses. Tn1 and Dn2 conduct the phase-current, thus experiencing conduction losses. In R2 and R3, based on similar arguments as with SVPWM, T1 and Dn2 experiences both conduction and switching losses whereas Tn1 only incurs conduction losses. (iii) DPWMPN – In R1, due to PN clamping, no device experiences switching losses, and only T1 incurs conduction losses due to conducting the clamped current. In R2 and R3, due to negative modulating voltage and positive current, Tn1, Dn2 and D2 experience conduction and switching losses [52]. Appendix A provides the method of calculating analytical switching and conduction losses from the modulation functions.

4.4.2 Switching Loss of Individual Devices

Fig. 4-6 shows a comparison of the devices' switching losses, based on assumptions provided in [18], for the PWM strategies. It shows the following: (i) with SVPWM, T1 and Dn2 incur maximum switching losses, and Tn1 and D2 incur negligible switching losses, (ii) with DPWMO, due to clamping, the switching losses incurred by T1 and Dn2 reduce by 50 %, and (iii) with DPWMPN, the switching losses of T1 is negligible, however, switching losses of Tn1 and D2 increases. Hence, use of the DPWMPN strategy results in switching loss redistribution amongst the switching devices.

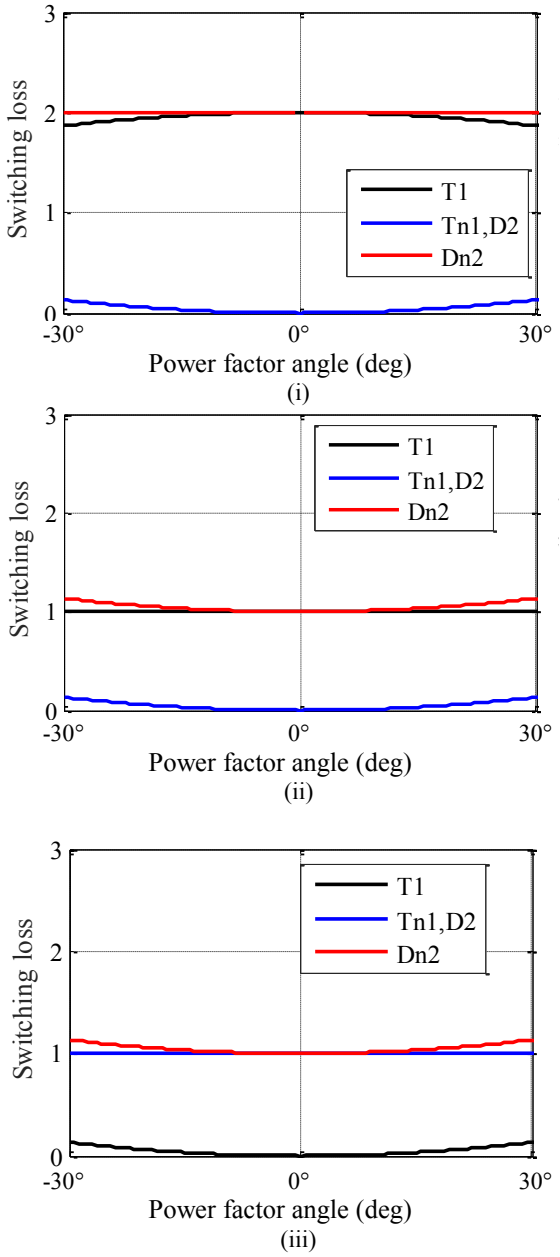


Figure 4-6. Device switching loss comparison between (i) SVPWM, (ii) DPWM2O, and (iii) DPWM2PN over change in power factor angle

4.4.3 Conduction Loss of Individual Devices

Referring to Fig. 4-5, the conduction losses of the devices are calculated and shown in Fig. 4-7. It shows the following: with SVPWM and DPWMO, the inner devices (Tn1, Dn2) incurs substantially higher conduction losses at lower modulation indices, in comparison to the outer devices (T1, D2). On the other hand, with DPWMPN, the conduction losses incurred by the

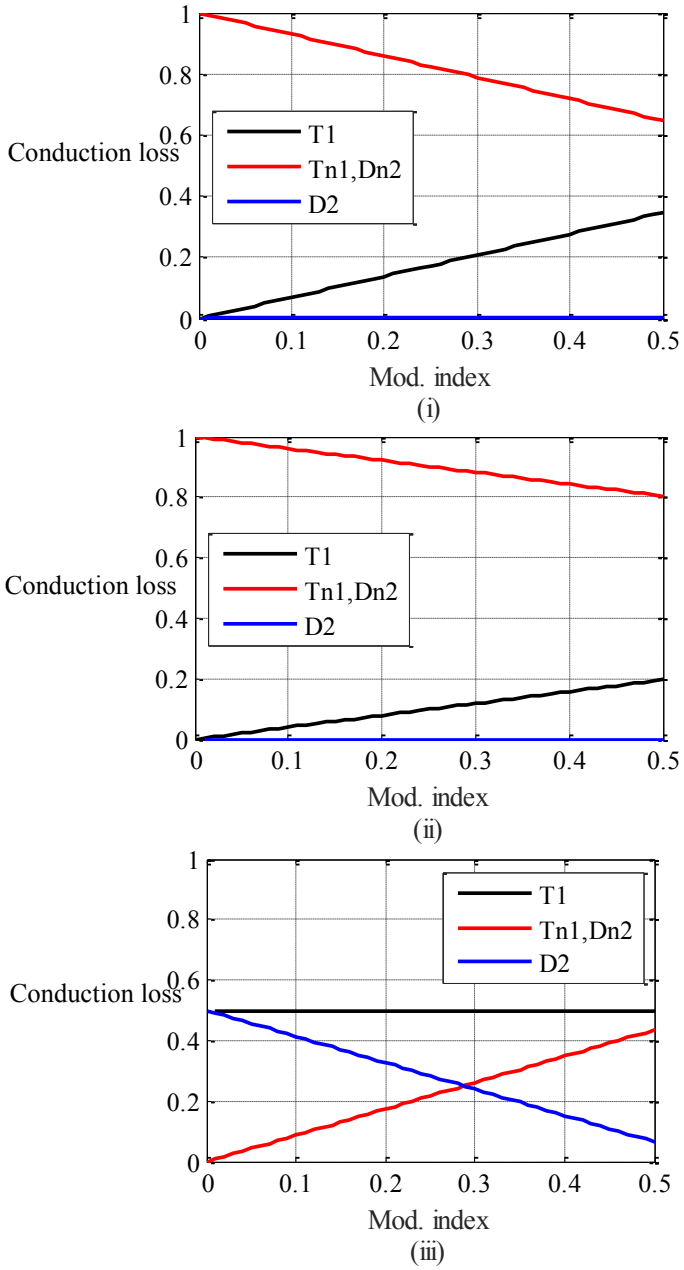


Figure 4-7. Device conduction loss comparison between (i) SVPWM, (ii) DPWM2O, and (iii) DPWM2PN over change in modulation index.

switching devices are more equally distributed. T1 and D2 have more conduction losses than DPWMO and SVPWM due to PN clamping, and these in turn reduce conduction losses of the inner Tn1 and Dn2 devices.

From Figs. 4-6 and 4-7 with SVPWM and DPWMO strategy, the switching losses of inner and outer devices do not have much difference, whereas, they show substantial unequal

conduction loss distribution amongst them. With DPWMPN, the switching losses of the outer devices are lower than the inner devices, whereas, the conduction losses are higher for the outer devices; hence the cumulative losses get distributed more equally.

4.4.4 Inverter Output Current Ripple

Each PWM strategy impact inverter output current ripple in a different manner due to variations in switching sequence. The impact of the switching strategies on output current ripple [18] is shown in Fig. 4-8 with the help of current ripple triangle. With SVPWM, the centroid of the ripple triangle (C1) is nearer to the origin (0, 0), in comparison to those of DPWMO and DPWMPN (C2 and C3). This is since SVPWM does not have any clamping interval, thus it can use redundant switching vectors. As the centroid of the ripple triangle is an indicator of the current distortion [18], ripple due to DPWMO and DPWMPN is higher than SVPWM, as knows from earlier studies.

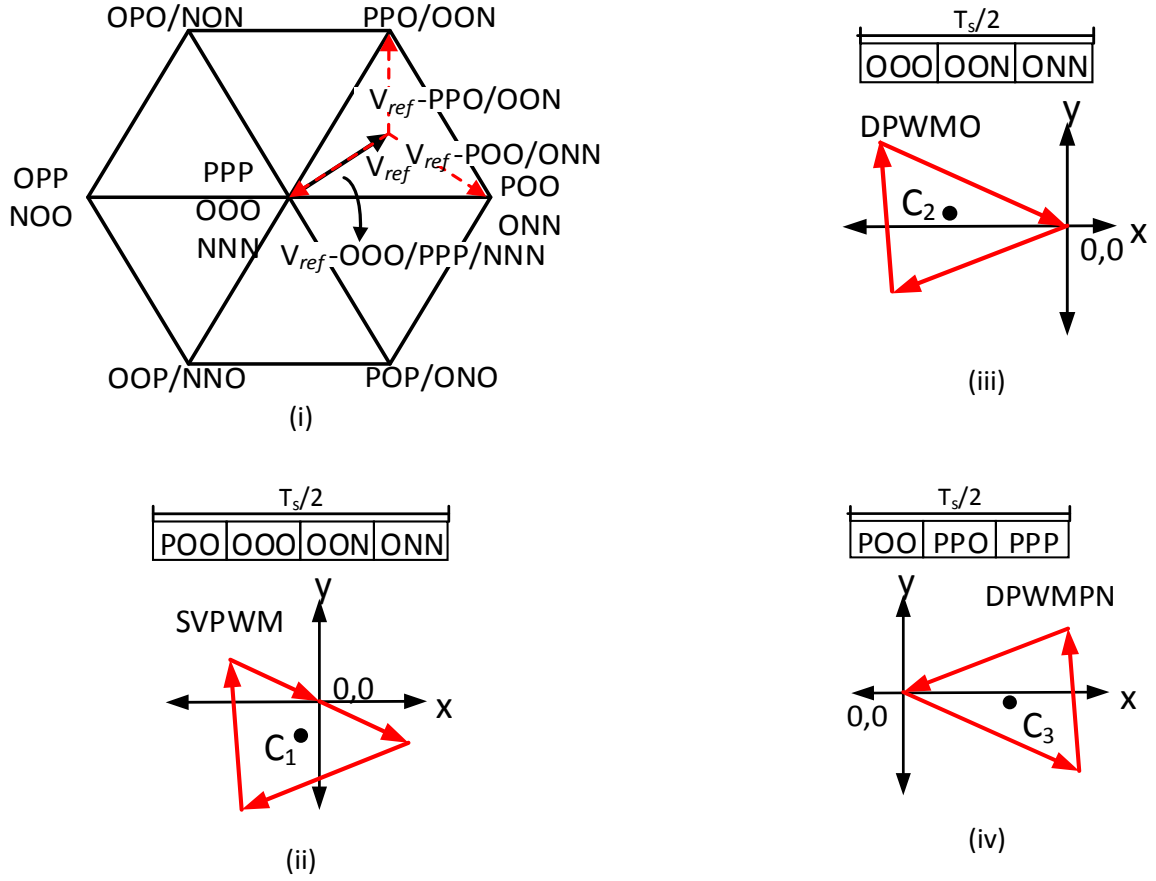


Figure 4-8. (i) Switching cycle voltage ripple, Switching cycle current ripple comparison between (ii) SVPWM, (iii) DPWM2O, and (iv) DPWM2PN

On the other hand, the centroid of the ripple triangles formed due to DPWMO and DPWMPN are identical in size and form, although they are situated at different sides of the y-axis. This indicates that the distortion due to these two DPWM techniques would be same, and the relative position of current ripple triangle is a mere indication of opposite current ripple direction at an instant.

4.5 Simulation Implementation & Results

The PWM sequences have been simulated on a T-NPC inverter with Vdc = 700 V, Irms = 70 A, modulation index = 0.4, and power factor = 0.866 lagging. The switching pulses were generated using MATLAB/Simulink and were fed to PSIM [118] to simulate the inverter under study [119] while providing the loss and junction temperature of each switch [120] - [121]. The model to calculate device losses and junction temperature is briefly discussed in Appendix A.

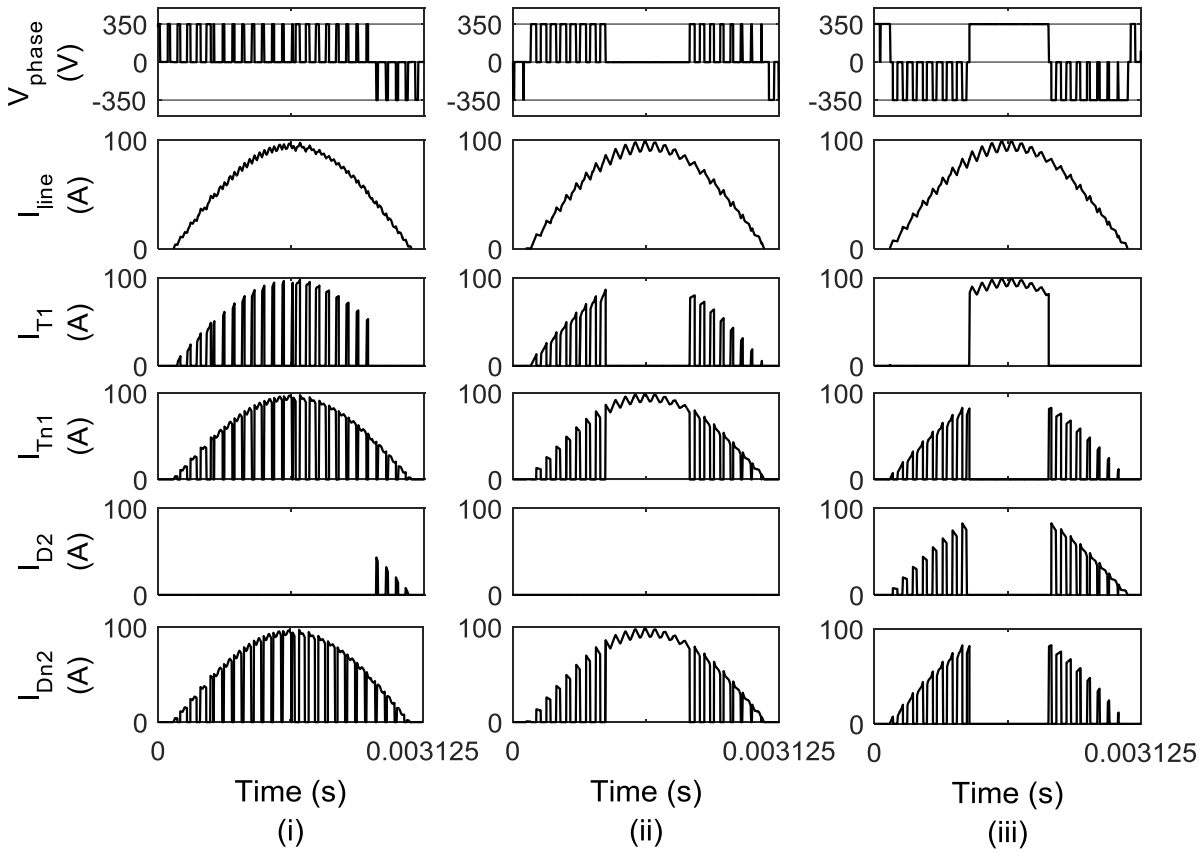


Figure 4-9. Simulation results showing phase to DC-link neutral voltage, line currents, *T*1 currents, *T*n1 currents, D2 currents and *Dn*1 currents at 0.4 modulation index, 0.866 power factor, 160 Hz fundamental frequency and 7.68 kHz switching frequency for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWM2PN*.

4.5.1 Comparison of Output Waveforms

Fig. 4-9 shows that with conventional SVPWM, there are 24 switching instances every half cycle. The positive half-cycle current is carried by either T1 or D2 or Tn1 and Dn2 together. With DPWM2O, the A-phase is clamped to neutral-point of the DC-link, and Tn1 (and Dn2) carry the current during clamping. There are 16 switching instances every half cycle. With DPWM2PN, the A-phase is clamped to the positive bus of the DC-link. This reduces the current through Tn1 and Dn2 devices compared with other two switching sequences. There are 17 switching instances every half cycle. Fig. 4-10 shows a comparison of current harmonics of the line currents using the PWM strategies. With SVPWM, it has 3% THD, whereas, with DPWM2O and DPWM2PN, the THD magnitude is around 4.5%. Thus, the DPWMPN strategy does not deteriorate output waveform more than conventional DPWM strategies.

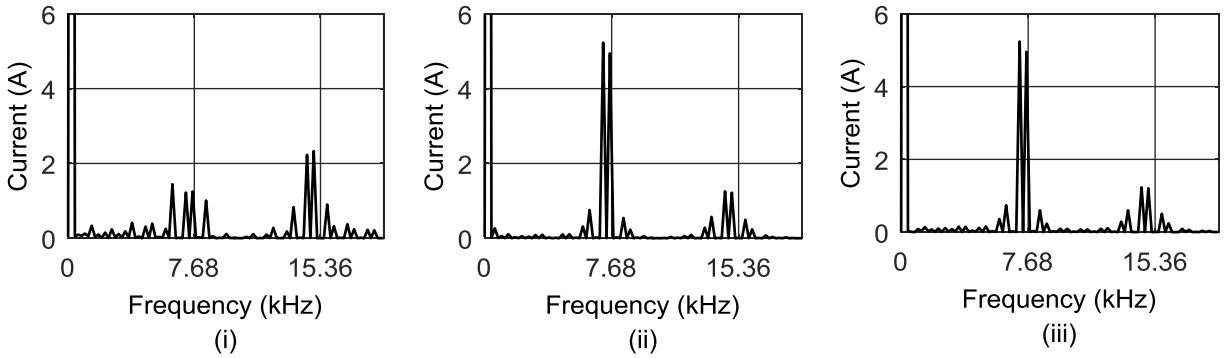


Figure 4-10. Simulation results showing current harmonics for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWM2PN*. Fundamental frequency component: 86 A

4.5.2 Comparison: Device Losses and Junction Temperature Rise

Figs. 4-11 and 4-12 show the switching and conduction losses of T1- D2 and Tn1-Dn2 switches. Referring to Fig. 4-11, with SVPWM and DPW2MO, T1 incurs maximum switching losses. With DPWM2PN, switching losses in T1 is substantially reduced, however, switching losses in Tn1 is increased due to use of more number of commutations due to 'O' - 'N' type switching.

Referring to Fig. 4-12, with SVPWM and DPWM2O, the inner devices – Tn1 and Dn2 incur 3-8 times more conduction losses compared to the outer switching devices - T1 and D2. With

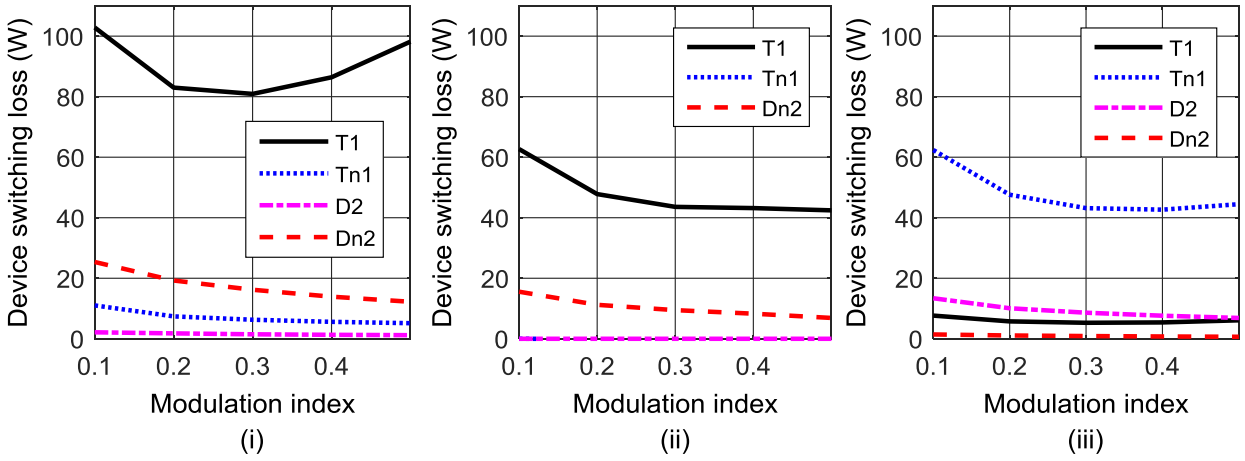


Figure 4-11. Simulation results showing switching loss distribution amongst different switching devices for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWM2PN*.

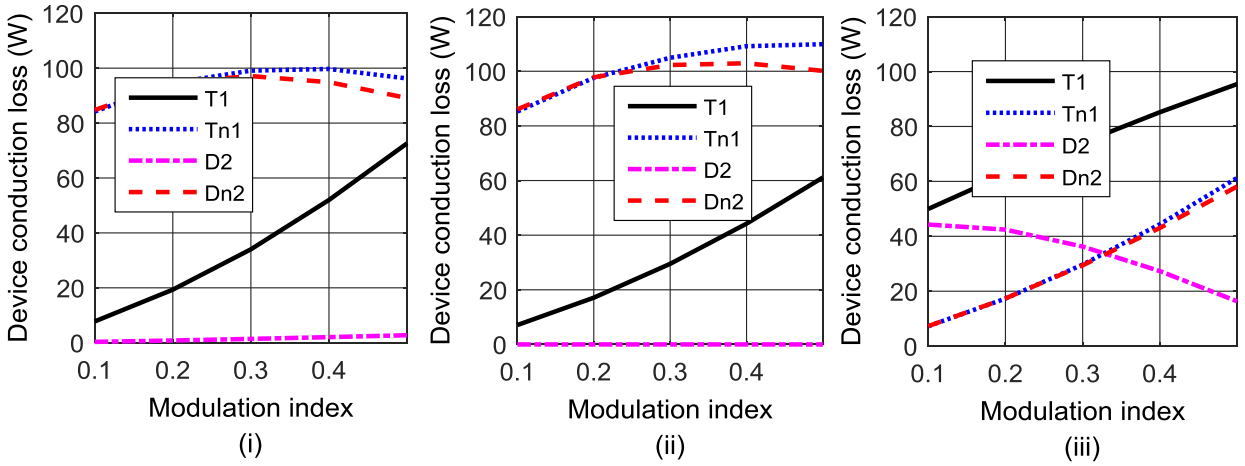


Figure 4-12. Simulation results showing conduction loss distribution amongst different switching devices for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWM2PN*.

DPWM2O, the discrepancy between device conduction losses increases more. However, with DPWM2PN, conduction loss in T1 increases while the conduction loss of Tn1 and Dn2 decreases appreciably. Hence, the simulated results follow the trend of the analysis done in Section III.

Fig. 4-13(i) shows the distribution of the cumulative losses of the devices. It shows that in comparison to SVPWM and DPWM2O, DPWM2PN re-distributed the device losses more equally amongst the devices due to the transfer of switching and conduction losses to D2 and reduction of conduction losses in Tn1 and Dn2. Also, the total losses with the DPWM2PN technique is lower than the other strategies.

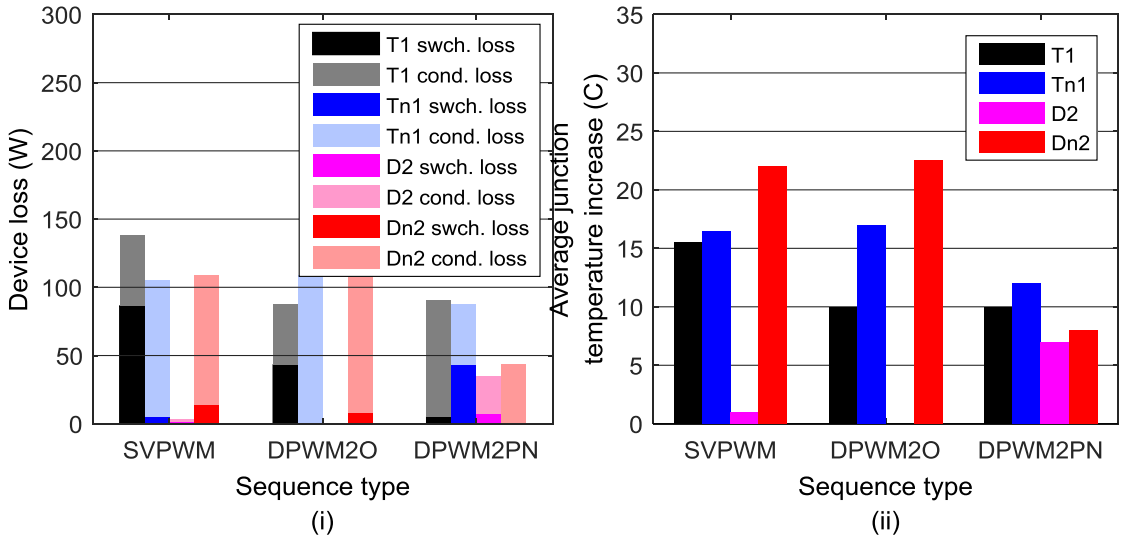


Figure 4-13. Simulation results showing (i) total inverter loss distribution amongst different switching devices, and (ii) device average temperature rise distribution for SVPWM, *DPWM2O*, and *DPWM2PN*.

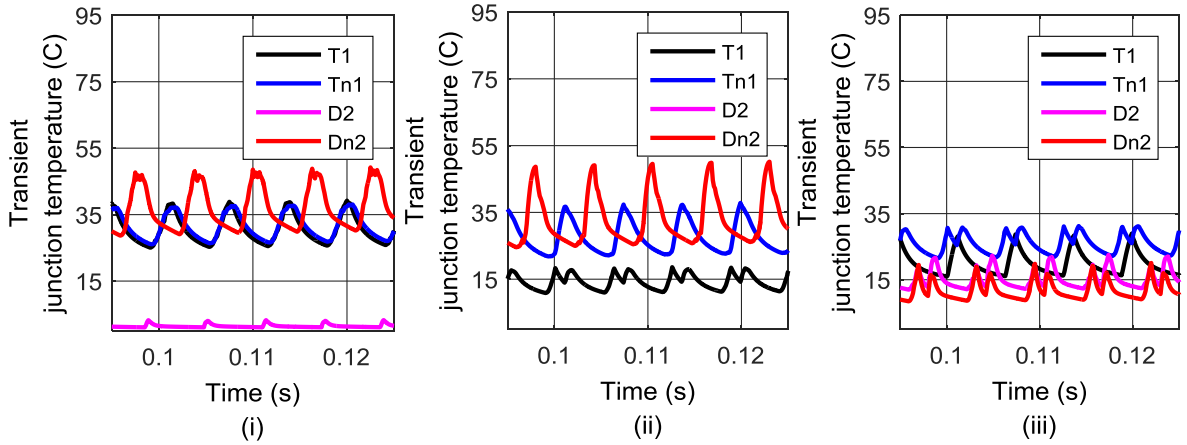


Figure 4-14. Simulation results showing transient junction temperature distribution amongst different switching devices for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWM2PN*.

Fig. 4-13(ii) shows the distribution of the increase of average junction temperature of the devices. Like the distribution of the device losses in Fig. 4-12(i), DPWM2PN produces a more equal temperature distribution amongst the devices.

Fig. 4-14 shows the distribution of the transient junction temperature increase of the devices. It shows that with SVPWM and DPWM2O, diode Dn2 incurs highest temperature increase, in the range of 45°-55° C. On the other hand, with DPWM2PN, the maximum peak temperature increase is attained by T1 and Tn1, in the range of 20°-30° C.

Fig. 4-15 shows the impact of the conventional SVPWM, DPWM2O and proposed DPWM2PN sequences on the analytical current ripple []. The current ripple forms are discussed in Chapter 6. It can be seen that – 1) Both DPWM techniques have higher current ripple compared to the conventional SVPWM technique, and 2) The proposed DPWM2PN sequence does not deteriorate the inverter output current waveform in comparison to the conventional DPWM2O sequence.

4.5.3 Capability of Higher Output Power or Switching Frequency

As seen from the above results, with DPWM2PN, the switches incur reduced junction temperature rise, thus they can withstand additional losses while remaining within the peak junction temperature attained for SVPWM and DPWM2O. Hence, there is an opportunity to

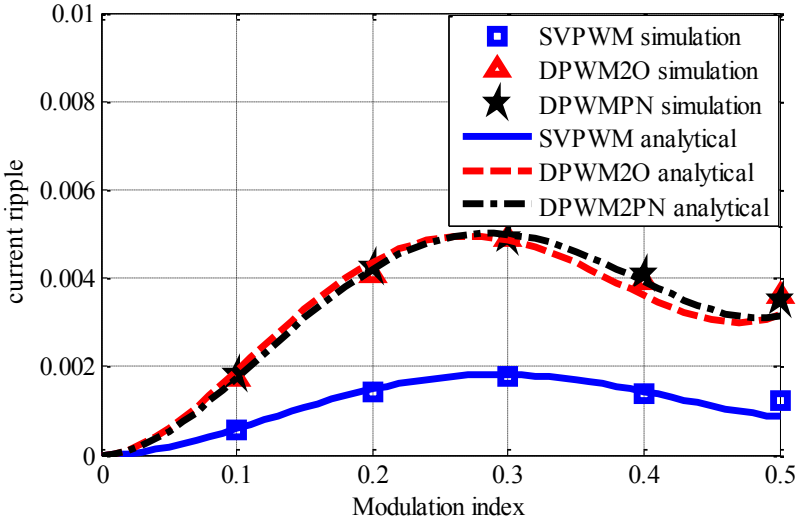


Figure 4-15. Simulated and analytical results of the dependency of the RMS value of output line current ripple on the modulation index

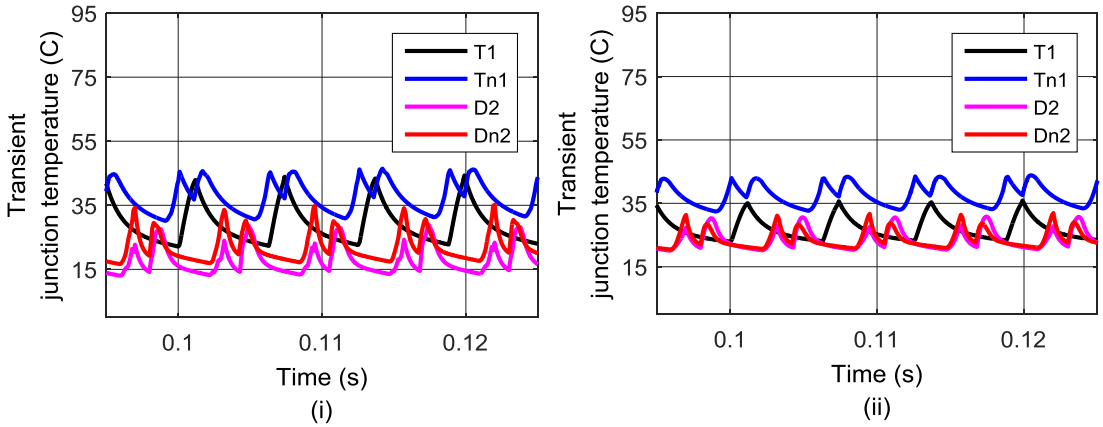


Figure 4-16. Simulation results showing transient junction temperature distribution for DPWM2PN using (i) 30% more current, and (ii) 37.5% higher switching frequency

increase either the output current or the device switching frequency. As shown in Fig. 4-16 (i), with a 30% increase in output current, the peak temperatures of the T1 and Tn1 devices, working with the DPWM2PN strategy, reach in the range of 45°-55° C. Fig. 4-16(ii) shows the temperature distribution when the operating switching frequency is increased from 7.68 kHz (carrier ratio: 48) to 10.56 kHz (carrier ratio: 66), a 37.5 % increment. It shows that even with this higher switching frequency, the peak temperatures of T1 and Tn1 remain around 45°-55° C. Thus, with the DPWM2PN strategy, a 30 % increase in output power or a 37.5 % increase in switching frequency is attainable while incurring similar junction temperature increase as the SVPWM and DPWM2O strategies.

The simulation results have been summarized in Table 4-2.

TABLE 4-2: SUMMARY OF SIMULATION RESULTS

Case	Number of pulses	THD (%)	Maximum junction temperature (°C)
SVPWM	24	3	45-55
DPWMO	16	4.5	45-55
DPWMPN	16	4.5	20-30

4.6 Experimental Results

The switching strategies have been implemented on a scaled down experimental setup [122] having a T-NPC inverter fed from a 200 V DC-link and supplying a three-phase passive R-L load (22 Ω, 5.1 mH). The setup is shown in Fig. 4-17. The switching frequency is 4.8 kHz, and the fundamental frequency is varied between 100-400 Hz to vary the operating power factor between 0.86-0.98. The inverter output waveforms are compared to validate the fundamental operational characteristics of the DPWMPN strategies.

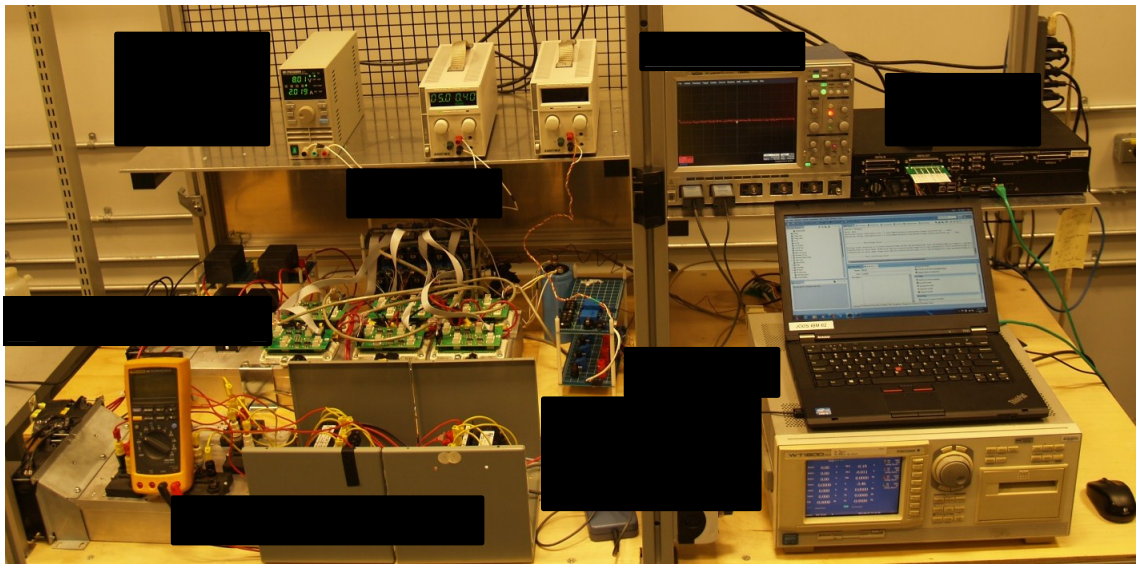


Figure 4-17. Experimental setup of three-level T-type inverter feeding resistive-inductive load

TABLE 4-3: EXPERIMENTAL SETUP PARAMETERS

Parameters	Values
Input DC voltage	200 V
DC-link capacitor	110 µF, Film Propylene
Output resistive load	22 Ω
Output inductive load	30 mH
Operating frequency	200 Hz
Operating power factor	0.5
Switching frequency	4.8 kHz

A comparison of the SVPWM, DPWM2O and DPWM2PN switching sequences for 0.866 pf, and a comparison of the SVPWM, DPWM1O and DPWM1PN switching sequences for 0.98 pf have been shown in Figs. 4-18 and 4-19. The following observations can be made:

- The SVPWM sequence has 7 switching instances per phase for DPWM2PN sequence and 23 switching instances for DPWM1PN. Higher number of switchings with DPWM1PN is due to use of higher carrier ratio. The current through the DC-link neutral point (designated as ineutral) is more than the current through the DC-link positive and negative bus currents designated as ipos and ineg).

- The DPWM2O sequence incurs 4 switching instances and the DPWM1O sequence incurs 15 switching instances. Due to the clamping at the DC-link neutral point, the current peak is carried by the inner devices, increasing conduction losses of the devices.

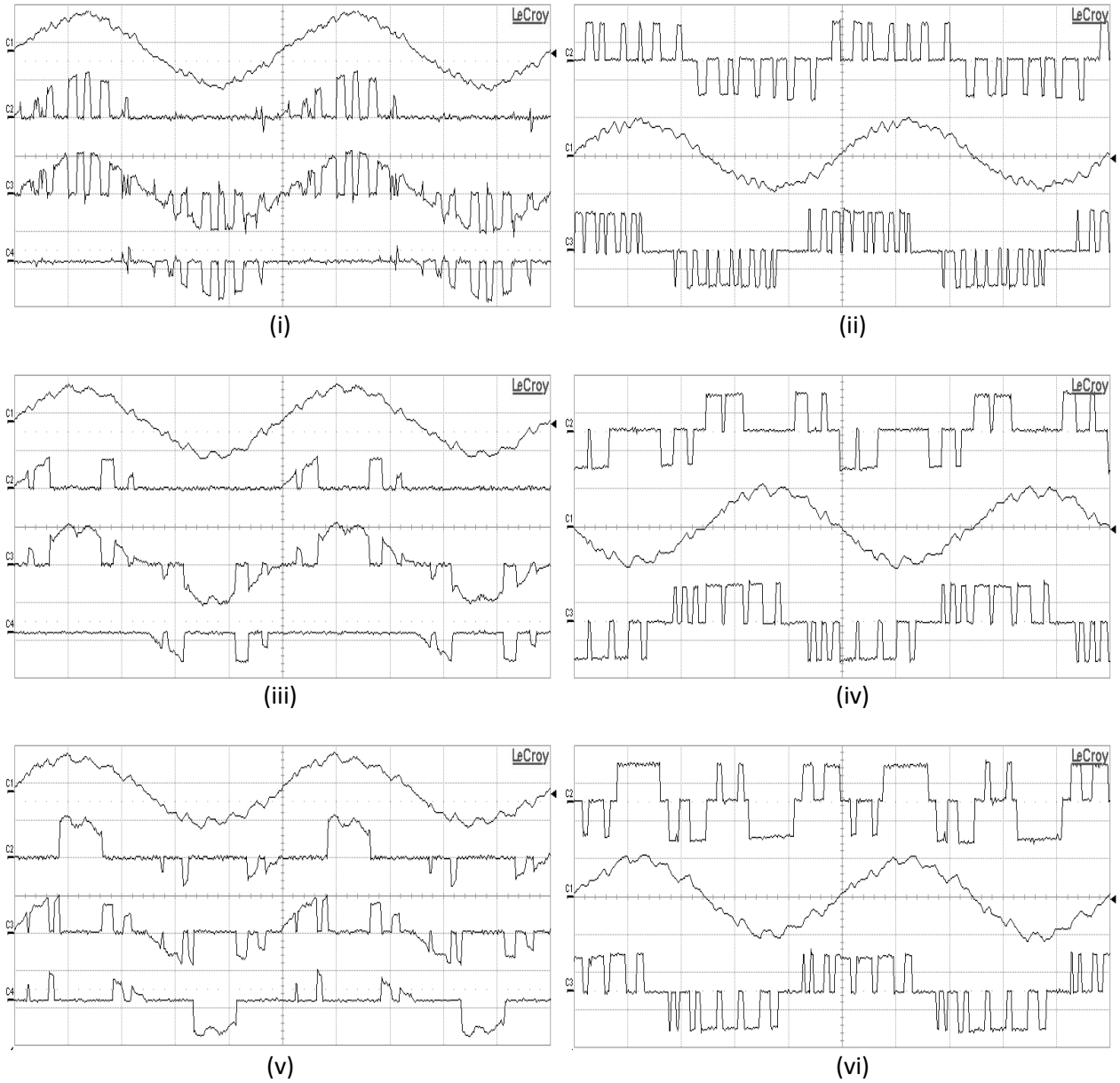


Figure 4-18. Experimental line currents, current through positive DC-bus, DC-link neutral point and negative DC-bus for (i) SVPWM, (iii) DPWM2O, and (v) *DPWM2PN* and experimental phase to DC-link neutral voltages, line currents and line-line voltages for (ii) SVPWM, (iv) DPWM2O, and (vi) *DPWM2PN*. Voltage scale: 100 V/div and current scale: 2 A/div, experimental conditions (dc-link voltage: 200 V, modulation index: 0.4, fundamental frequency: 400 Hz, switching frequency: 4800 Hz, power factor: 0.866, time step: 500 μs/div)

- The DPWM2PN switching sequence incurs 5 switching instances and the DPWM1PN sequence incurs 16 switching instances. As the clamping occurs with the positive and negative bus, the line current gets redistributed to the outer switches from the inner switches.

Fig. 4-20 shows the harmonic profile of the output current using the PWM strategies. With SVPWM, the dominant switching frequency harmonics are around twice the switching frequency

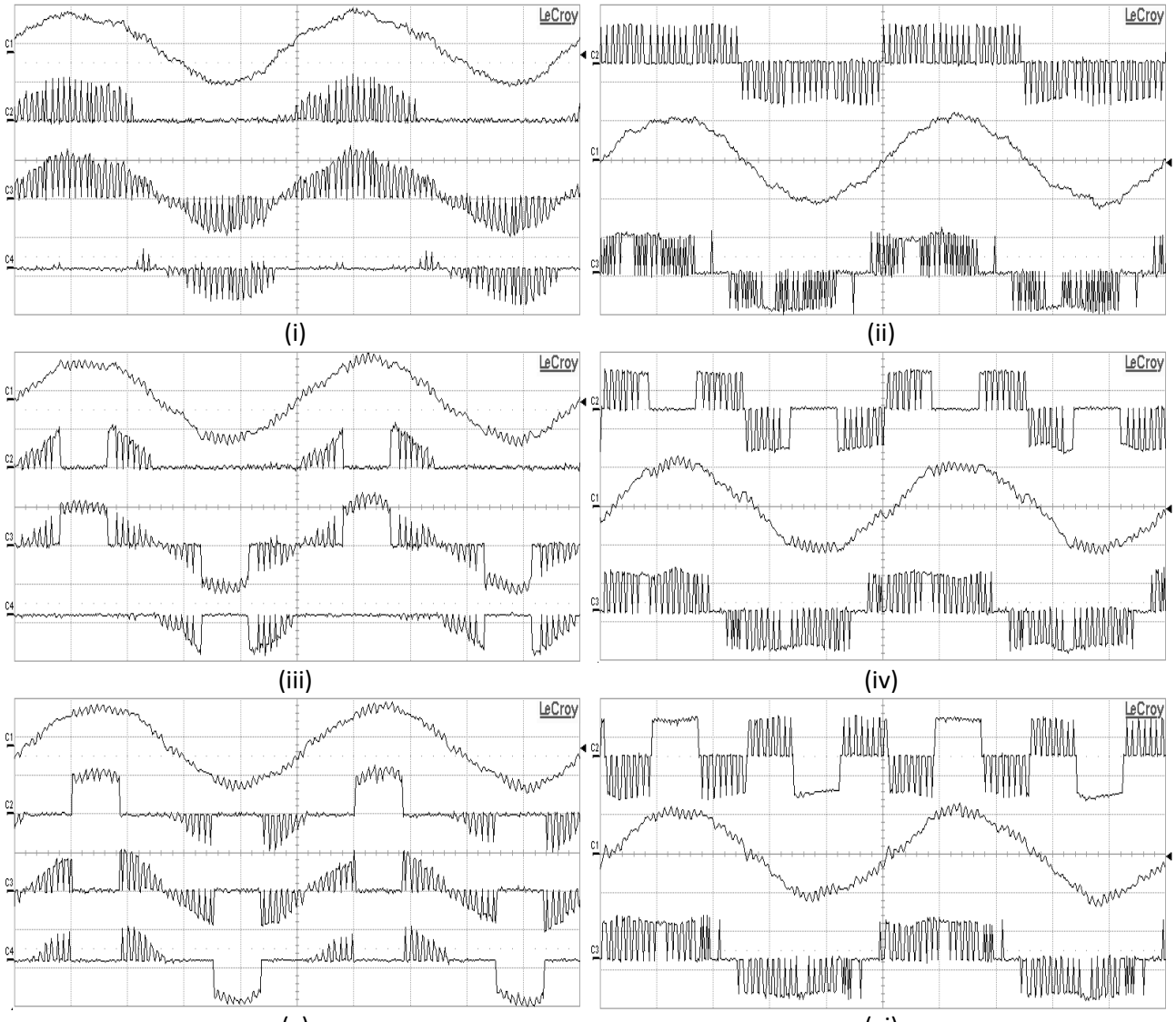


Figure 4-19. Experimental line currents, current through positive DC-bus, DC-link neutral point and negative DC-bus for (i) SVPWM, (iii) DPWM1O, and (v) *DPWM1PN* and experimental phase to DC-link neutral voltages, line currents and line-line voltages for (ii) SVPWM, (iv) DPWM1O, and (vi) *DPWM1PN*. Voltage scale: 100 V/div and current scale: 2 A/div, experimental conditions (dc-link voltage: 200 V, modulation index: 0.4, fundamental frequency: 100 Hz, switching frequency: 4800 Hz, power factor: 0.98, time step: 500 μs/div)

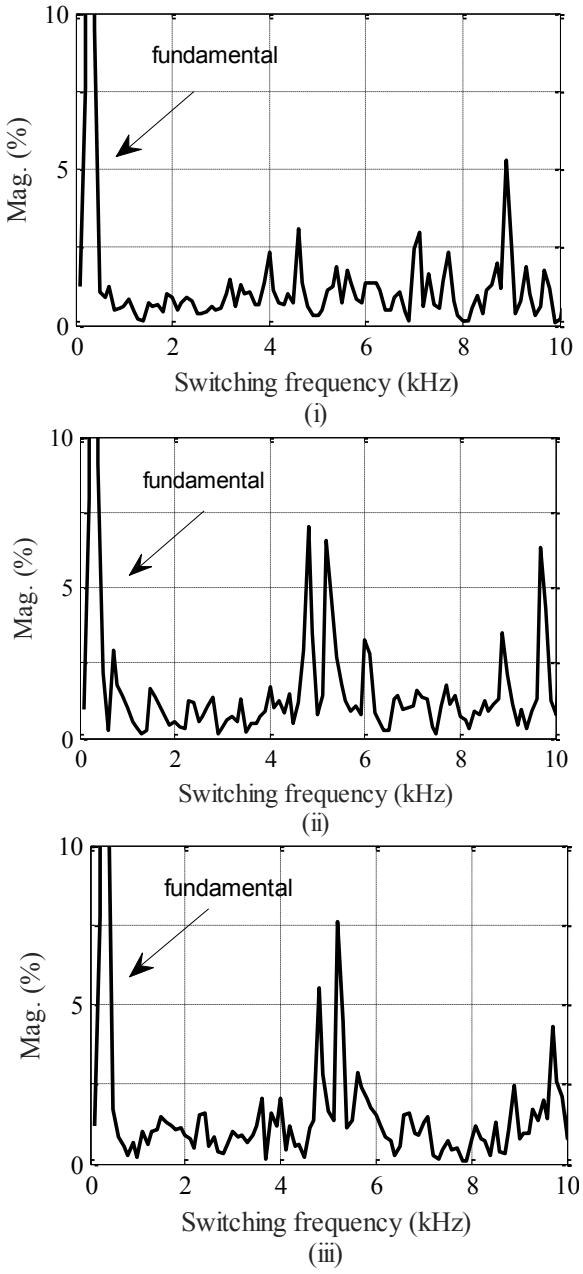


Figure 4-20. Experimental results showing current harmonics for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWM2PN*.

(9.6 kHz), whereas with the DPWMO and DPWMPN techniques they are around the switching frequency, like the simulation results. Thus, the proposed DPWMPN strategy does not deteriorate the output waveform more than conventional DPWM strategies.

The abovementioned experimental results have been summarized in Table 4-4.

TABLE 4-4: SUMMARY OF EXPERIMENTAL RESULTS

Case	Number of pulses	THD (%)	Comment
SVPWM – 0.98 pf	23	5	Higher current through neutral
DPWM1O – 0.98 pf	15	6.7	Higher current through neutral
DPWM1PN – 0.98 pf	16	6.6	Current redistributed
SVPWM – 0.866 pf	7	3.2	Higher current through neutral
DPWM2O – 0.866 pf	4	4.5	Higher current through neutral
DPWM2PN – 0.866 pf	5	4.6	Current redistributed

Impact of the PWM strategies on the inverter efficiency has been measured using the efficiency improvement factor (EIF) [117]. EIF of DPWMO and DPWMPN techniques have been measured in 0.2 and 0.4 modulation index for – (i) three different operating switching frequencies – 4.8, 6 and 7.2 kHz, and (ii) two operating power factors – 0.866 and 0.98. At 0.866 power factor, DPWM2O and DPWM2PN switching strategy is used. On the other hand, at 0.98 power factor, DPWM1O and DPWM1PN switching strategy is used. The results are shown in Fig. 4-21 and Table 4-5. The results show that with the DPWM1PN and DPWM2PN strategies, the EIF's are always higher than DPWM1O and DPWM2O strategies. For example, at 0.4 modulation index and 0.866 power factor, the average EIF of DPWMPN is 8 % whereas for DPWM2O, it is around 5.6%. Similarly, at 0.98 power factor, the average EIF of DPWMPN is 5.8 % whereas for DPWM2O, it is around 4.5%. These experimental results show that the DPWMPN strategies re-distribute the line currents from the inner switching devices to the outer switching devices and incur lower device losses, like the simulation results.

4.7 Conclusion

The three-level inverters are extensively used in medium voltage, high-power applications (e. g. industrial drives), and recently they have also been introduced in low-voltage, high-power

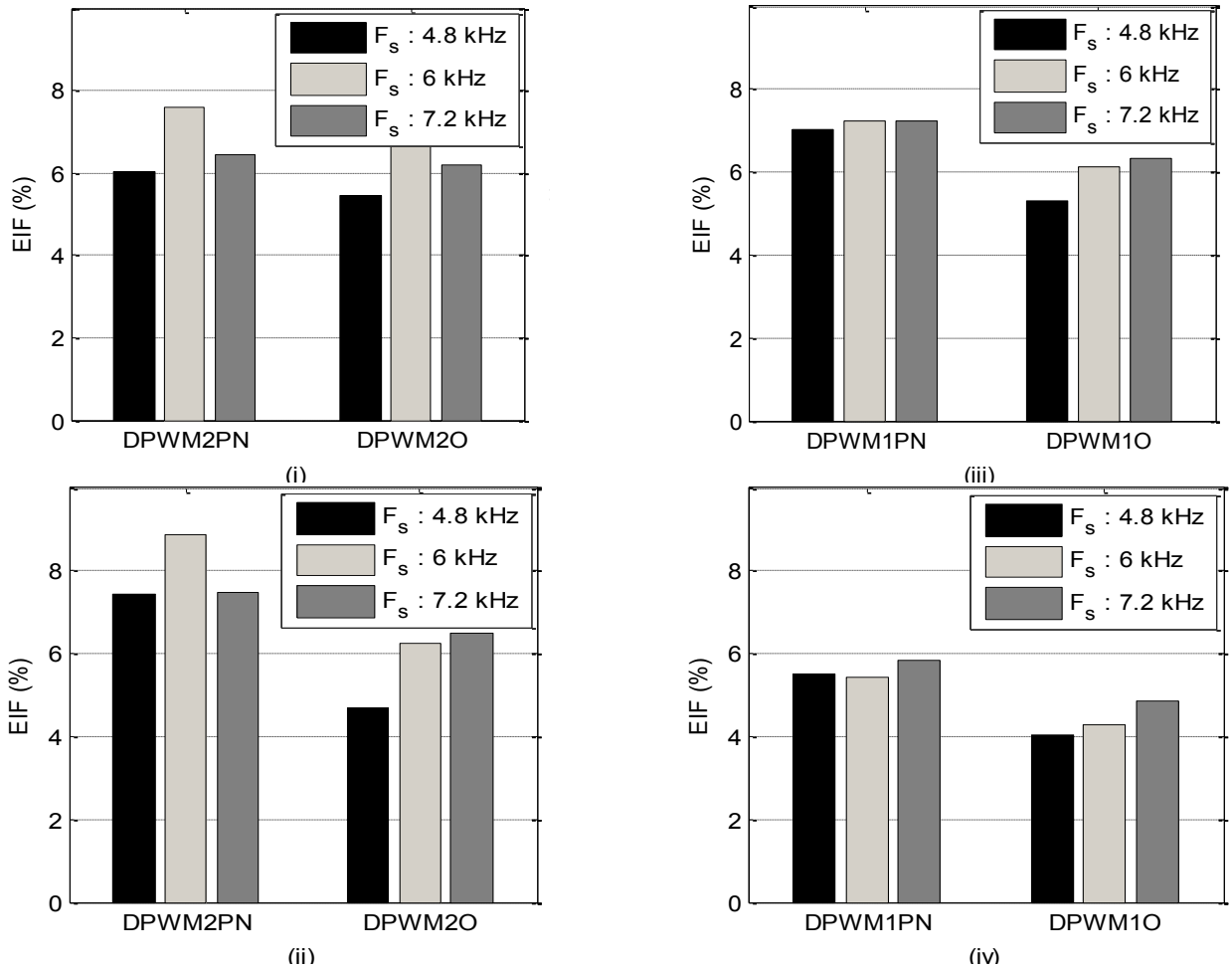


Figure 4-21. Experimental efficiency improvement factor (EIF) comparison between – (i) DPWM2PN and DPWM2O at 0.2 modulation index and 0.866 power factor, (ii) DPWM2PN and DPWM2O at 0.4 modulation index and 0.866 power factor, (iii) DPWM1PN and DPWM1O at 0.2 modulation index and 0.98 power factor, and (iv) DPWM1PN and DPWM1O at 0.4 modulation index and 0.98 power factor

traction applications. Amongst different variants of three-level inverter topologies, the T-type Neutral-Point-Clamped (T-NPC) inverter, is shown to be one of the most promising solutions. In these applications, the three-level inverters often need to operate with modulation indices lower than 0.5. Although the three-level inverters and the respective thermal design for these applications are designed for maximum speed/loading conditions; even at lower modulation indices (speed), the inverter may need to provide higher output current during acceleration or deceleration. Hence, they also need to be controlled appropriately at lower modulation indices for optimum performance. Also, at lower modulation indices, as the switches are not utilized in an equal manner, PWM strategies needs to be designed for redistribution of device losses.

TABLE 4-5: EXPERIMENTALLY MEASURED EFFICIENCY AND EIF

PWM type		Mod. index	Power factor	Efficiency (%)	EIF (%)
Switching Frequency: 4.8 kHz	SVPWM	0.2	0.98	70.48	-
		0.4		79.64	-
	DPWM1O	0.2	0.98	74.1	5.2
		0.4		81.25	4
	DPWM1PN	0.2	0.98	75.42	7
		0.4		81.84	5.6
	SVPWM	0.2	0.866	68.7	-
		0.4		77.8	-
	DPWM2O	0.2	0.866	71.9	4.7
		0.4		80.9	4
	DPWM2PN	0.2	0.866	72.8	6
		0.4		82.1	5.5
Switching Frequency: 6 kHz	SVPWM	0.2	0.98	68.5	-
		0.4		78.92	-
	DPWM1O	0.2	0.98	72.7	6.1
		0.4		82.23	4.2
	DPWM1PN	0.2	0.98	73.3	7.2
		0.4		83.26	5.5
	SVPWM	0.2	0.866	66.8	-
		0.4		77.1	-
	DPWM2O	0.2	0.866	70.94	6.2
		0.4		80.34	4.2
	DPWM2PN	0.2	0.866	71.94	7.7
		0.4		81.6	5.8
Switching Frequency: 7.2 kHz	SVPWM	0.2	0.98	67.9	-
		0.4		78.11	-
	DPWM1O	0.2	0.98	72.1	6.2
		0.4		81.85	4.8
	DPWM1PN	0.2	0.98	72.8	7.2
		0.4		82.64	5.8
	SVPWM	0.2	0.866	68	-
		0.4		77	-
	DPWM2O	0.2	0.866	72.3	6.3
		0.4		80.7	4.8
	DPWM2PN	0.2	0.866	72.97	7.3
		0.4		81.16	5.4

For the low modulation index range, a discontinuous modulation strategy has been

proposed for the three-level T-NPC inverter topology. The proposed DPWMPN switching sequences can relocate the phase currents to the outer switches, from the inner switches during clamping. Hence, with the proposed sequences, the distribution of losses and junction temperature is more equal amongst the switching devices. In consequence, the inverter – 1) can increase its current throughput by around 30% or 2) can utilize a 30-40% higher switching frequency to improve output waveform quality, while incurring similar increase of device junction temperatures as conventional PWM sequences. Moreover, these improvements have been obtained without deteriorating the waveform quality in comparison to conventional three-level DPWM techniques and without using any additional switches.

At lower modulation indices, the power factor of a motor can be lower than 0.866, if an interior permanent magnet motor or a synchronous reluctance motor is used. In that case, the existing PWM strategies need to be improved. The following chapter provides few PWM sequences and strategy which caters for lower power factor operation.

5 Generalized Discontinuous PWM for Three-Level Inverters Operating at Low Modulation Index

5.1 Overview

The chapter proposes three DPWM templates for lower power factors and a generalized three-level DPWM strategy that aligns the 60° no-switching durations with respective phase current peaks, for all power factor angles (90° leading to 90° lagging) for modulation indices lower than 0.5. Thus, without any switching instances around the current peaks, the maximum switching loss reduction capability gets extended to all operating power factors. Please be noted that the term 'power factor' only corresponds to displacement power factor, i.e. the phase difference between the fundamental voltage and current waveform. The paper also offers an in-depth analytical analysis of switching loss reduction of a T-NPC inverter for the conventional SVPWM and generalized DPWM strategies for comparison.

5.2 Introduction

At lower modulation indices, traction drives operating with induction motors (IMs), interior permanent magnet motors (IPMs) or synchronous reluctance motors (SynRMs) may need to provide higher reactive power, thus operating with a lower power factor [40], [112], [123]-[130]. For example, in [124], the power factor of IPMSMs at 0.2 modulation index is shown to be 0.52. The power factor of SynRMs also varies between 0.3-0.7 based on designed saliency [130]. Hence, the three-level inverters for these applications need to be controlled appropriately at lower modulation indices and lower power factors for optimum performance.

Three-level Discontinuous PWM (DPWM) strategies have been introduced in [48], [58] [96], [105], [107], [116] - [117], [131] as natural extensions of the DPWM strategies of two-level inverters [18] - [20] to reduce switching losses. In these strategies, each inverter phase is not switched for one-third of a fundamental cycle, known as the no-switching durations. By doing so,

a maximum 33% switching loss reduction is achievable [116]. Moreover, if the no-switching duration is divided into two 60° sectors and if they are aligned with respective current peaks, the inverter avoids switching at higher current magnitudes, thus reducing switching losses in the range of 50% [117].

However, the following can be noted of the reported three-level DPWM strategies:

- The 60° no-switching durations of the existing three-level DPWM templates are only capable to remain aligned with the phase-current peaks for power factor angles within the range of 30° lagging to 30° leading over the entire modulation index range. This is shown in Fig. 5-1 with the help of average a-phase modulation voltage waveform for DPWM2O and a-phase current for 0.5 power factor. As the clamping interval is not aligned with the current peak, there would be switching instances around current maxima, prohibiting maximum switching loss reduction. Thus, their impact on the switching loss reduction is restricted [3] at power factors lower than 0.866. Moreover, the studies did not look at any other possibilities at lower modulation indices.
- Existing works did not look at space-vector based three-level generalized DPWM strategy to adapt the no-switching duration and provide clamping at current peaks for all power factors. A similar procedure exists for two and three level inverters; however, they use carrier based

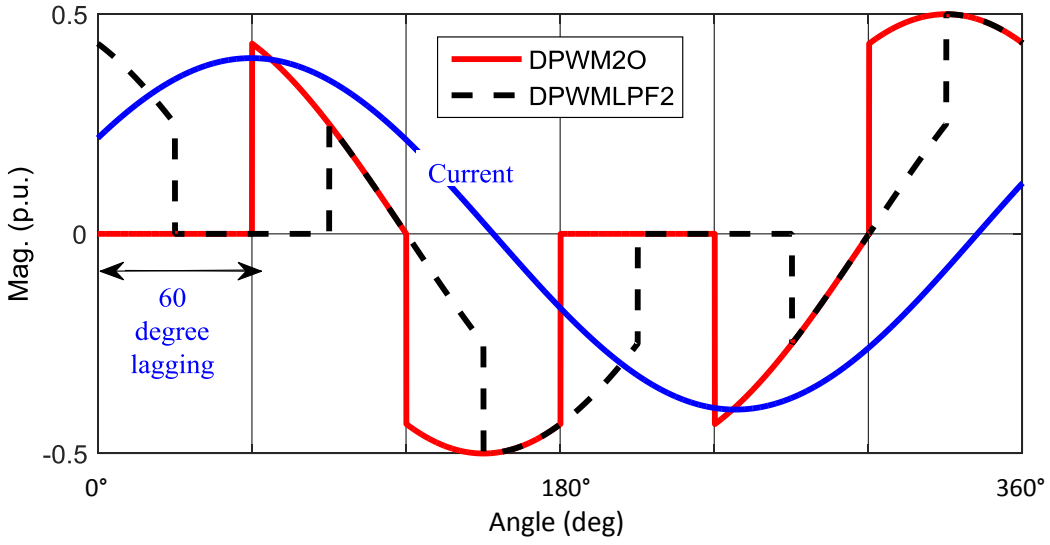


Figure 5-1. Phase difference between a-phase fundamental current (power factor 0.5) and average phase to DC-link neutral voltage waveforms for DPWM2O and DPWMLPF2

third harmonic injected sine-PWM strategy, and is only applicable for power factor angles inside the range of 30° lagging to 30° leading.

- Moreover, all the DPWM switching templates are designed for a specific power factor. Their impact on switching losses of a three-level inverter for different power factors has not been identified.

5.3 Proposed DPWM Sequences for Lower Power Factors

Referring to Fig. 4-2, a closer look at the available switching vectors for $m \leq 0.5$ shows that each of the three-legs (A, B and C) can be clamped to the neutral-point (O) of the DC-link for all the sectors (I-VI). For example, phase A can be clamped to O using (OOO↔OON↔ONN) sequence in sector I, (OON↔OOO↔OPO) sequence in sector II, (OOO↔ONO↔ONN) sequence in sector VI, and (OOP↔OOO↔ONO) sequence in sector V. Thus, two 60° no-switching durations can be designed in all the sectors (I-VI) and for different operating power factors, switching sequences can be designed such that each phase-leg would have two 60° 'no-switching' durations aligned with its current peaks.

In Table 5-1, the proposed three additional DPWM templates have been listed, and they are named as variants of DPWMLPF (DPWM Low Power Factor): i) DPWMLPF1 – a-phase

TABLE 5-1: DIFFERENT THREE-LEVEL SWITCHING SEQUENCES FOR LOWER POWER FACTOR

Strategy	Optimum pf	Sector I		Sector II		Sector III	
		Subsector 1a	Subsector 1b	Subsector 1a	Subsector 1b	Subsector 1a	Subsector 1b
DPWMLPF 1	90° lead and lag	(OON↔OOO↔NOO)	(OON↔OOO↔POO)	(OPO↔OOO↔OON)	(OPO↔OOO↔OON)	(NOO↔OOO↔OPO)	(NOO↔OOO↔OPO)
DPWMLPF 2	60° lag	(OON↔OOO↔POO)	(OOO↔OON↔ONN)	(OPO↔OOO↔OON)	(OOO↔OPO↔PPO)	(OPO↔OOO↔NOO)	(OOO↔NOO↔NON)
DPWMLPF 3	60° lead	(OOO↔POO↔PPO)	(OON↔OOO↔POO)	(OOO↔OON↔NON)	(OPO↔OOO↔OON)	(OOO↔OPO↔OPP)	(NOO↔OOO↔OPO)

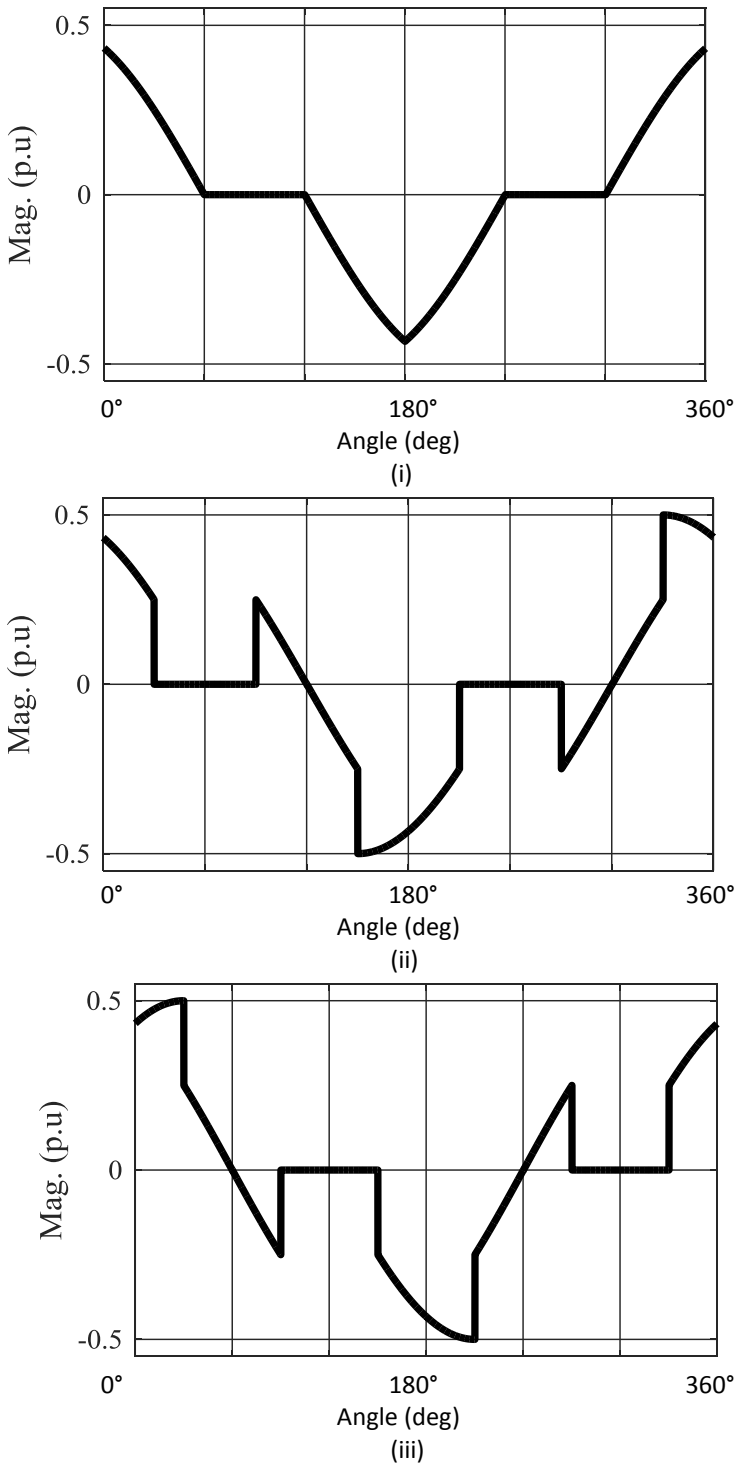


Figure 5-2. Average phase to DC-link neutral voltage [28] waveforms for modulation index less than 0.5, normalized w.r.t DC-link voltage for proposed DPWM templates - (i) *DPWMLPF1*; (ii) *DPWMLPF2*; (iii) *DPWMLPF3* ; 0.5 signifies half DC-link voltage

clamping at sectors II, V and designed for 90 degree lagging and leading pf, ii) DPWMLPF2 – a-

phase clamping at subsectors 1a of sectors I, IV, subsectors 1b of sectors II, V and designed for 0.5 lagging pf, and iii) DPWMLPF3 – a-phase clamping at subsectors 1b of sectors VI, III, subsectors 1a of sectors V, II and designed for 0.5 leading pf. The average a-phase modulation voltage waveforms [132] of these switching sequences along with the clamping intervals are shown in Fig. 5-2(i-iii). Fig. 5-1 also shows that in comparison to the DPWM2O sequence, the clamping intervals of the proposed DPWMLPF2 switching sequence (which is designed for 0.5 power factor) are aligned with the line current peaks for a lagging 60° power factor angle.

5.4 Proposed Generalized DPWMO Strategy

The conventional and proposed DPWM strategies shown in Tables 4-1 and 5-1 I have fixed templates and provides maximum switching loss reduction possibility only at that power factors

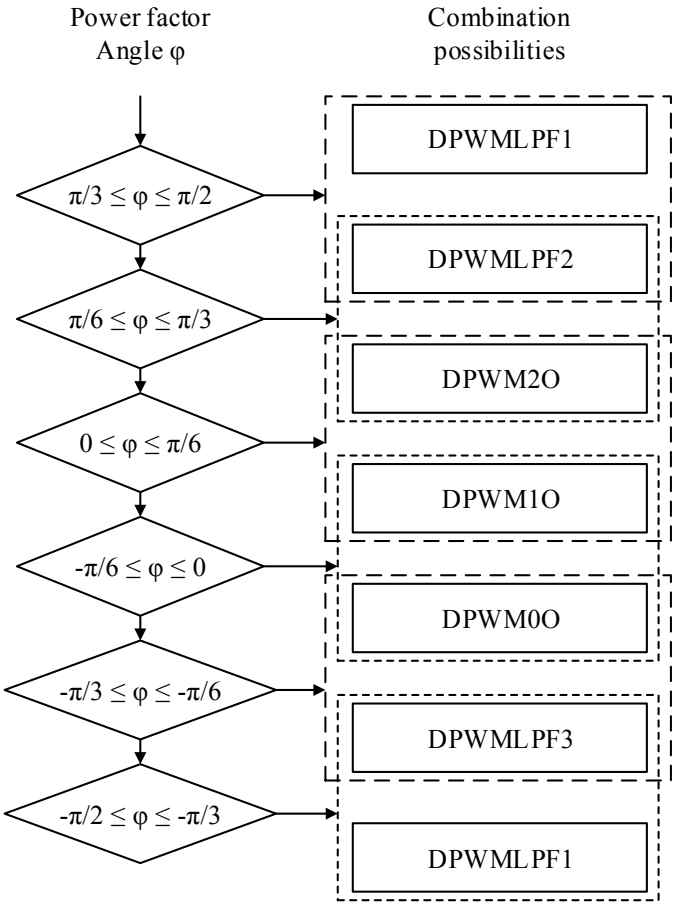


Figure 5-3. Combinations of the DPWMO sequences for generalized DPWMO (GDPWMO) based on operating power factor angle

TABLE 5-2: CLAMPING INTERVAL IN A QUARTER CYCLE FOR $30° \leq \varphi \leq 60°$

Strategy	Angle of operation
DPWMLPF2	$0 \leq \theta_v \leq \alpha - 30°$
DPWM2O	$\alpha - 30° \leq \theta_v \leq 30°$
DPWMLP2 or *DPWM2O*	$30° \leq \theta_v \leq 60°$
DPWMLPF2	$60° \leq \theta_v \leq 30° + \alpha$
DPWM2O	$30° + \alpha \leq \theta_v \leq 90°$

for which they are designed. During operation, the load power factor of a three-level inverter may vary and the clamping intervals need to be shifted so that they remain aligned with the phase current peaks. To achieve that, the following generalized DPWMO (GDPWMO) strategy is designed.

5.4.1 Operating Principle

In this strategy, portions of different DPWM templates are selected and combined within a fundamental cycle to provide clamping interval aligned with the phase-current peak. As depicted in Fig. 5-3, the DPWM templates to be combined, are selected based on the operating power factor (φ). For power factor angle between 90° and 60°, *DPWMLPF*1 and *DPWMLPF*2 templates are used. For power factor angle between 60° and 30°, *DPWMLPF*1 and DPWM2O templates are used. For power factor angle between 30° and 0°, DPWM1O and DPWM2O templates are used. Similar combinations exist for operating with leading power factor. An example of combination between two fixed DPWM templates (DPWM2O and *DPWMLPF*2) is described as follows:

- For an operating power factor angle $30°$, the a-phase current peaks in the middle of sector I, as shown in Fig. 5-4(i). So, the two 60° clamping intervals are in sector I and sector IV.

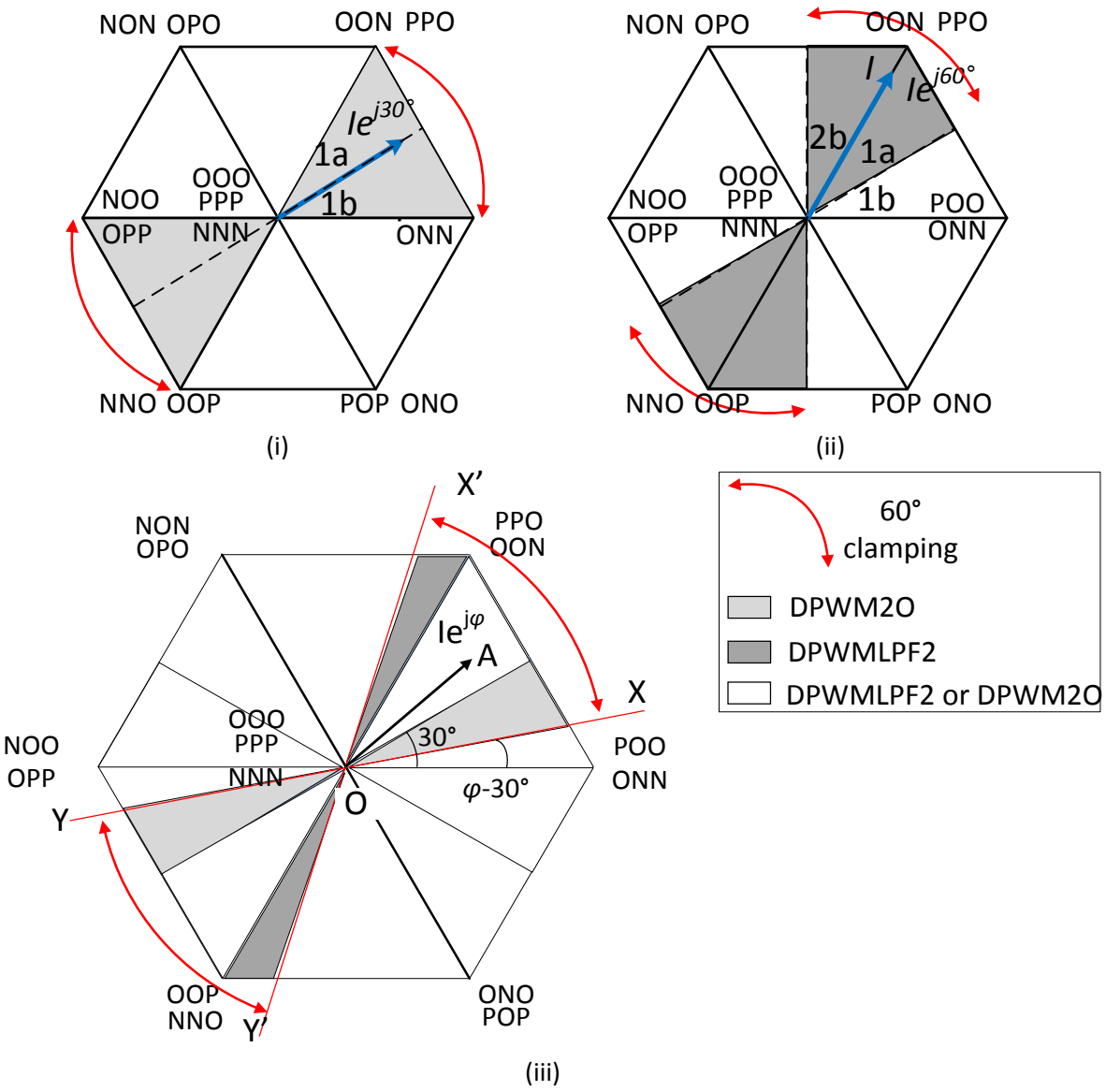


Figure 5-4. The position of the current vector and the clamping strategy with (i) conventional DPWM2O, operating with a 30° power factor angle load, (ii) proposed *DPWMLPF2*, operating with a 60° power factor angle load, and (iii) *GDPWMO,* operating with ϕ power factor angle (30°≤ϕ≤60°) load and combining between *DPWMLPF2* and DPWM2O. The intervals shown using the red colored arrows are the 60° clamping durations

- For an operating power factor angle 60°, the a-phase current peaks at the edge of sector I and sector II, as shown in Fig. 5-4(ii). So, the two 60° clamping intervals are in sector I-II and sector IV-V, comprising 30° intervals in each of those sectors.

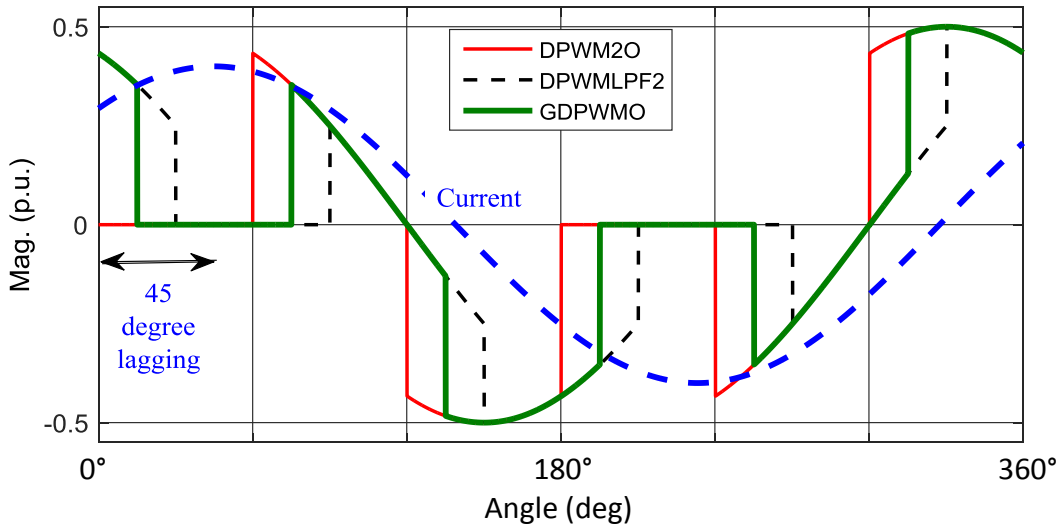


Figure 5-5. Phase difference between a-phase fundamental current (power factor 0.707) and average phase to DC-link neutral voltage waveforms for DPWM2O, *DPWMLPF2* and *GDPWMO*. The peaks of the line current are aligned with *GDPWMO*

- For an operating power factor angle φ $(30° \leq \varphi \leq 60°)$ assume that the a-phase current peaks along the line OA, as shown in Fig. 5-4(iii) with the help of current phasor $Ie^{j\varphi}$. Hence, two 60° clamping intervals need to be designed such that – (i) they are aligned with the line O, and (ii) within the part of the space-vector hexagon enclosed by XOY and X′OY′ lines, as shown in Fig. 5-4(iii). As the power factor angle is within $30°$ and $60°$, a combination of DPWM2O and DPWMLPF2 templates is used. Referring to Fig. 5-4(iii) and Fig. 5-5, the following combination provides the desired clamping intervals: (a) DPWM2O for $\varphi - 30° \leq \theta_v \leq 30°$, (b) DPWMLPF2 or DPWM2O for $30° \leq \theta_v \leq 60°$ as in this region, both sequences have similar templates (ref. Table 5-1), and (c) DPWMLPF2 for $60° \leq \theta_v \leq 30° + \varphi$. The light grey color signifies use of DPWM2O template, the dark grey color signifies use of DPWMLPF2, and the white color signifies that both DPWM2O and DPWMLPF2 templates can be used. Furthermore, from the clamping intervals shown above, it can be deduced that for a 30° power factor angle, DPWM2O is used solely. On the other hand, for 60° power factor angle, DPWMLPF2 is only utilized. For any power factor angle between 30° and 60°, both templates are used, thus, providing a generalized pattern.

5.4.2 Reducing Switching During Transition between Templates

Fig. 5-6 shows the implementation technique for the GDPWMO technique, taking the combination of DPWM2O and DPWMLPF2 as an example. Referring to Table 5-1, the switching sequences are implemented along with the individual timing durations of the switching vectors. In addition, the implementation is done such that the number of switching instances during transition between two DPWM templates within a fundamental cycle is minimized. To achieve that, space-vector pairs are formed taking one vector from each of the templates, as shown by the rectangles with red dashes. A switching changeover between two templates is only allowed within these pairs at the points of transition. For example, for a transition between DPWMLPF2 and DPWM2O, the strategy ensures a switching transition using only one of the following three possibilities: (i) POO to OOO, (ii) OOO to OON, and (iii) OON to ONN. Each possibility incurs only one switching instance, as shown in Fig. 5-6. Hence, this strategy ensures minimum switching instances during a transition between two DPWM templates. Other possibilities of transitions between the switching templates would create additional switching instances. Similar switching changeovers have been designed for transition between other templates. Moreover, as these switching transitions do not occur near the current peak (due to the clamping intervals), they do not degrade the loss reduction capability of the resulting PWM sequence.

As all these switching templates are specifically devised for a power factor, it is interesting to identify their impact on inverter switching losses with respect to the continuous SVPWM

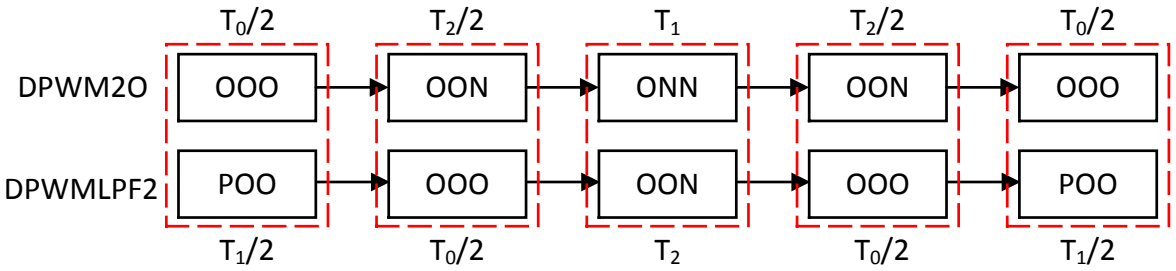


Figure 5-6. Implememtation technique of two DPWM strategies (DPWM2O and DPWMLPF2) in sector I, subsector 1b. It also contains the strategy of reduced switching during transition. The rectangles with red dashes show the only allowable transitittions between two templates. T_1 is the timing durations of POO or ONN, T_2 is the timing duration of OON, and T_0 is the timing duration of OOO.

sequence. Therefore, analytically calculated switching losses of a T-NPC inverter for different switching templates are presented in the following section.

5.4.3 Theoretical Switching Loss Calculation

The discontinuous switching strategies (DPWM0O-DPWM2O, DPWMLPF1-3 and GDPWMO) are designed for switching loss reduction of a three-level inverter at different fixed power factors, as seen from Tables 4-1 and 5-1. In real applications, operating power factor does not remain constant over the operating range of the inverter. As the switching losses are influenced by the switching sequence used and load power factor, it is important to analyze and compare the switching losses due to the three-level DPWM methods.

In [128], analytical switching loss calculation of a two-level inverter had been done if the switching loss is linearly proportional to the phase current switched by each switching device. Several authors have also assumed a squared proportionality relation between phase current and switching loss due to increase in device energy-loss with increase in current magnitude. However, as a comparison between different modulation strategies would remain similar for both assumptions, a linear relationship has been considered in this investigation.

As discussed in [17,105], the average value of switching loss (P_{av}) of a device over the fundamental cycle can be calculated as:

$$P_{av} = k \int_{0}^{2\pi} f_i(x)\, dx \tag{5.1}$$

Where $f_i(x)$ is the absolute current which the switching device accounts for during modulation and k is a constant value. As the absolute accounted current changes with load power f actor, P_{av} also changes with load power factor (φ). The calculation also assumes steady-state condition and neglect additional switching loss due to switching frequency ripple. The average switching losses due to each switching sequence is calculated and compared against the switching loss due to conventional SVPWM strategy. For comparison, a metric called switching

TABLE 5-3: AVERAGE SWITCHING LOSS EQUATIONS DUE TO GDPWMO STRATEGY

Strategy & Clamping angle (α)	Power factor Angle (φ)	Average Switching Loss
SVPWM	$-\frac{\pi}{2} \le \varphi \le \frac{\pi}{2}$	$2k\{2 + \sin^2(\varphi/2)\}$
GDPWMO $\frac{\pi}{2} \le \alpha \le -\frac{\pi}{6}$	$-\frac{\pi}{2} \le \varphi \le -\frac{\pi}{6}$	$2k\{2 - \cos(\varphi - \alpha)\}$
	$-\frac{\pi}{6} \le \varphi \le \frac{\pi}{6}$	$2k\left\{\sin(\frac{\alpha}{2} - \frac{\varphi}{2} - \frac{\pi}{3} + \frac{\lvert\pi/3 - \varphi + \alpha\rvert}{2}) + \sin(\alpha - \frac{\pi}{6} - \varphi) + \sin(\alpha - \frac{\pi}{3}) + \frac{5}{2}\right\}$
	$\frac{\pi}{6} \le \varphi \le \frac{\pi}{2}$	$2k\left\{\cos(\frac{\alpha}{2} - \frac{\varphi}{2} + \frac{\pi}{3} + \frac{\lvert 2\pi/3 - \varphi + \alpha\rvert}{2}) + \sin(\varphi) + \frac{\sqrt{3}}{2}\cos(\alpha)\right.$
GDPWMO $-\frac{\pi}{6} \le \alpha \le \frac{\pi}{6}$	$\alpha \le \varphi \le \frac{\pi}{3} + \alpha$	$2k\left\{\frac{5}{2} - \frac{3\sqrt{3}}{4}\cos(\varphi + \frac{\pi}{6} - \alpha) - \frac{3}{4}\sin(\varphi + \frac{\pi}{6} - \alpha)\right\}$
	$-\frac{\pi}{3} + \alpha \le \varphi \le \alpha$	$2k\left\{-2\sin(\varphi - \frac{\pi}{6} - \alpha) + \frac{\sqrt{3}}{2}\cos(\varphi - \frac{\pi}{6} - \alpha)\right\}$
	$-\frac{\pi}{2} \le \varphi \le -\frac{\pi}{3} + \alpha$ & $\frac{\pi}{3} + \alpha \le \varphi \le \frac{\pi}{2}$	$2k\left\{2\sin(\varphi - \frac{\pi}{6} - \alpha) + \frac{\sqrt{3}}{2}\cos(\varphi - \frac{\pi}{6} - \alpha)\right\}$
GDPWMO $\frac{\pi}{6} \le \alpha \le \frac{\pi}{2}$	$\frac{\pi}{6} \le \varphi \le \frac{\pi}{2}$	$2k\left\{\frac{5}{2} - \sin(\varphi + \frac{\pi}{6} - \alpha) - \frac{\sin(\varphi)}{4} - \frac{\sqrt{3}}{2}\cos(\varphi) - \cos(\varphi + \frac{1}{2}\right.$ $\left. - \alpha)\right\}$
	$-\frac{\pi}{6} \le \varphi \le \frac{\pi}{6}$	$2k\left\{\frac{5}{2} - \sin(\varphi + \frac{\pi}{6} - \alpha) + \frac{3\sin(\varphi)}{4} - \frac{\sqrt{3}}{4}\cos(\varphi) + \sin(\frac{\varphi}{2} - \right.$ $\left. - \frac{\pi}{3} + \frac{\lvert\pi/3 + \varphi - \alpha\rvert}{2})\right\}$
	$-\frac{\pi}{2} \le \varphi \le -\frac{\pi}{6}$	$2k\left\{\frac{\sqrt{3}}{2}\cos(\varphi) - \sin(\varphi) - \sin(\frac{\varphi}{2} - \frac{\alpha}{2} - \frac{\pi}{6} + \frac{\lvert 2\pi/3 + \varphi - \alpha\rvert}{2})\right.$

loss function (SLF) [17] is used which is be defined as ratio of average switching loss of DPWM strategy used and conventional SVPWM [98].

Referring to Fig. 4-1, in each phase leg of a T-NPC inverter, there four IGBT-diode pairs. In the positive fundamental cycle of the output current, IGBT T1, T2 and Diodes D3 and D4 carries

current. So, the cumulative switching loss of the inverter is calculated based on the switching losses of these four switching devices. Additionally, it has been observed [52] that the switching losses in T2 and D4 devices are zero when the phase switching sequence changes between 'P' (1100) and 'O' (0110), and are non-zero when the phase switching sequence changes between 'O' (0110) and 'N' (0011). In this investigation, switching losses of T2 and D4 devices have been considered similar. Appendix A provides the method of calculating analytical switching and conduction losses from the modulation functions.

The average switching loss of the inverter with the SVPWM and GDPWMO sequences are shown in Table 5-3. Unlike a two-level inverter [17], with a three-level inverter losses due to the SVPWM switching sequences depends on power factor. These equations have been plotted in Fig. 5-7 with the help of SLF function. The SLF of the SVPWM sequence is unity. Each DPWM sequence provides 50% switching loss reduction at the power factor they are designed for. For

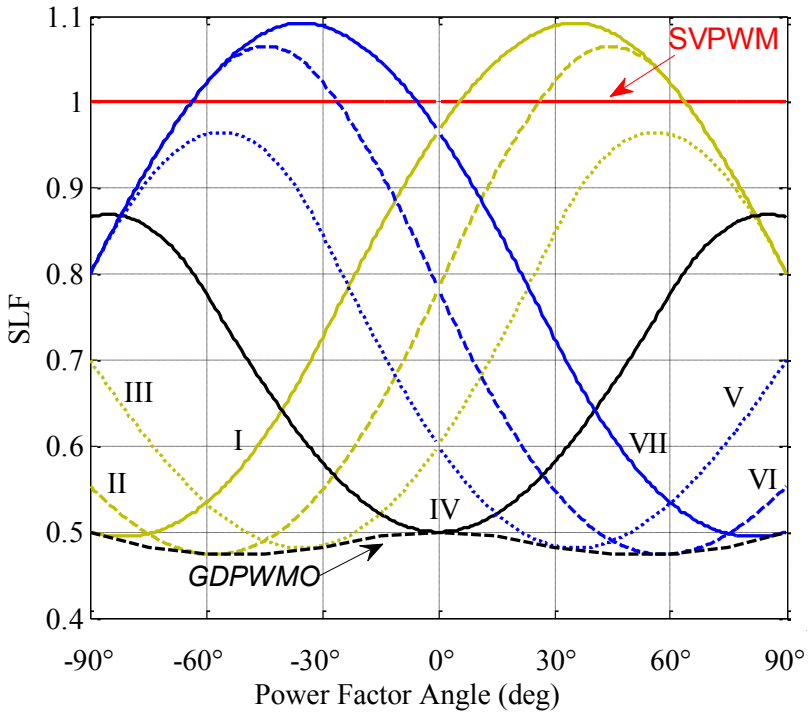


Figure 5-7. SLF characteristics of different PWM strategies with respect to power factor angle (ϕ) under fixed switching frequency –- I: *DPWMLPF1* ($\alpha = -90°$), II: *DPWMLPF3* ($\alpha = -60°$), III: DPWM0O ($\alpha = -30°$), IV: DPWM1O ($\alpha = 0°$), V: DPWM2O ($\alpha = 30°$), VI: *DPWMLPF2* ($\alpha = 60°$), and VII: *DPWMLPF1* ($\alpha = 90°$), in comparison to the conventional SVPWM strategies. Dotted line shows the SLF of *GDPWMO* strategy, and SLF of conventional SVPWM is unity.

example, DPWM2O provides maximum loss reduction at 30° power factor angle, whereas DPWMLPF2 provides maximum loss reduction at 60° power factor angle. The GDPWMO strategy uses part of each sequence to obtain maximum switching loss reduction at all operating power factor. Hence, its impact has been shown with the help of a dotted line, forming an envelope touching the maximum loss reduction points of all the DPWM strategies. It shows that in comparison to SVPWM technique, with GDPWMO, around 50% switching loss reduction can be achieved at all the power factors.

5.5 Simulation Implementation and Results

The PWM templates have been simulated on a three-level T-NPC inverter fed from a 700 V DC-link. The DC-link capacitance is 500 μF, the operating modulation index is 0.4, and the RMS output current is controlled at 70 A at different power factors. The switching pulses are generated using MATLAB/Simulink and fed to PSIM to simulate the inverter while providing the losses of the switching devices. The model to calculate device losses and junction temperature is briefly discussed in Appendix A.

Case I: *Power Factor Angle 60° (0.5 power factor), 200 Hz Fundamental Frequency and 4.8 kHz switching frequency*

In this case, three types of modulation strategies are compared - (i) conventional SVPWM, (ii) DPWM2O, and (iii) DPWMLPF2. The results of the phase-to-neutral voltages and line currents are shown in Fig. 5-8. The following can be noted:

- With the SVPWM sequence, there are 13 switching instances in every half period.
- With the DPWM2O sequence, there are 9 switching instances in every half period, a 33% reduction compared to the SVPWM sequence. However, the clamping interval is not aligned with the current peak, resulting in switching instances around the current peak.
- With the DPWMLPF2 sequence, there are 9 switching instances in every half period, a 33% reduction compared to the SVPWM sequence. Additionally, the clamping intervals are aligned with the current peaks, resulting in no switching instances around the current peak.

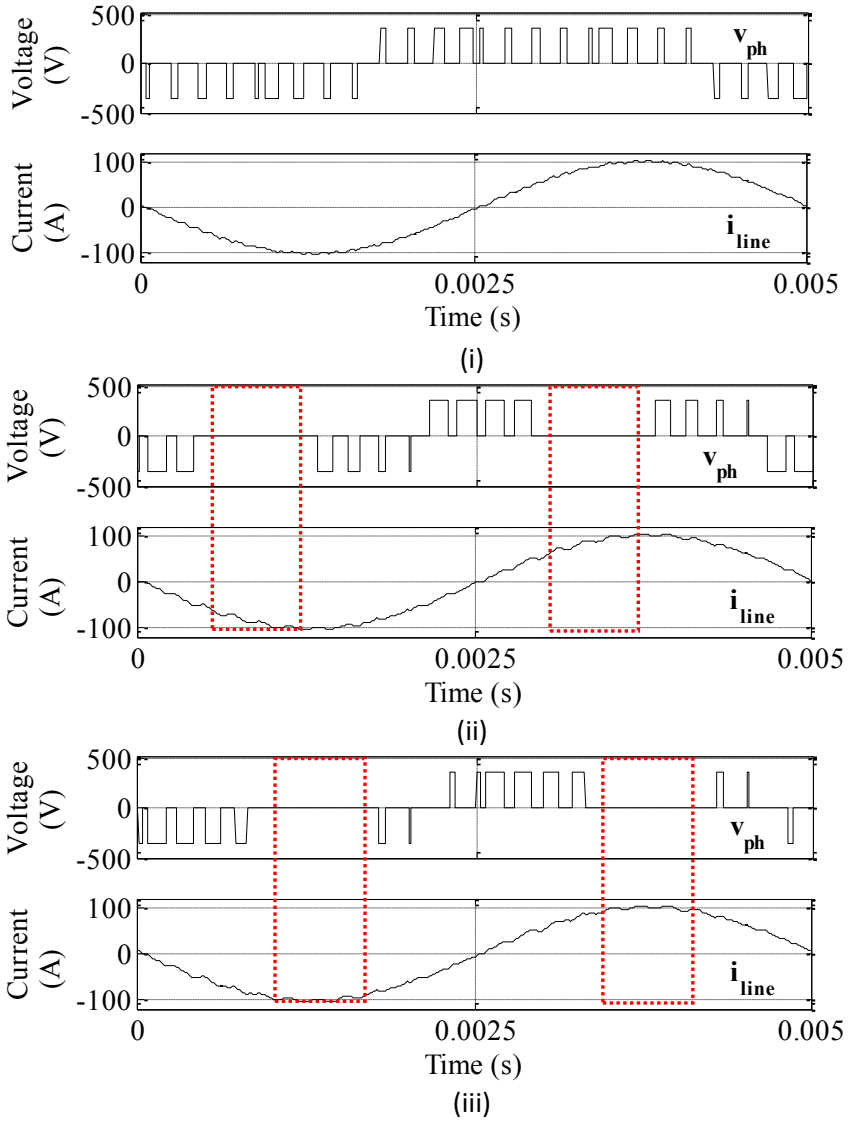


Figure 5-8. Simulation results showing phase to DC-link neutral voltage and line currents at 0.4 modulation index, 0.5 power factor, 200 Hz fundamental frequency and 4.8 kHz switching frequency for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWMLPF2*.

The harmonic spectra of the phase voltages and the line currents are also provided in Fig. 5-9. The following can be noted:

- With the SVPWM sequence, the weighted total harmonic distortion (WTHD) of the phase-to-neutral voltage waveform is 16%. The dominant harmonic of the line current is around twice the switching frequency and the THD of line current waveform is 2.84%.
- With the DPWM2O sequence, the WTHD of the phase-to-neutral voltage waveform is 27%. The dominant harmonic of the line current is around the switching frequency and the THD of line current is 4.6 %.

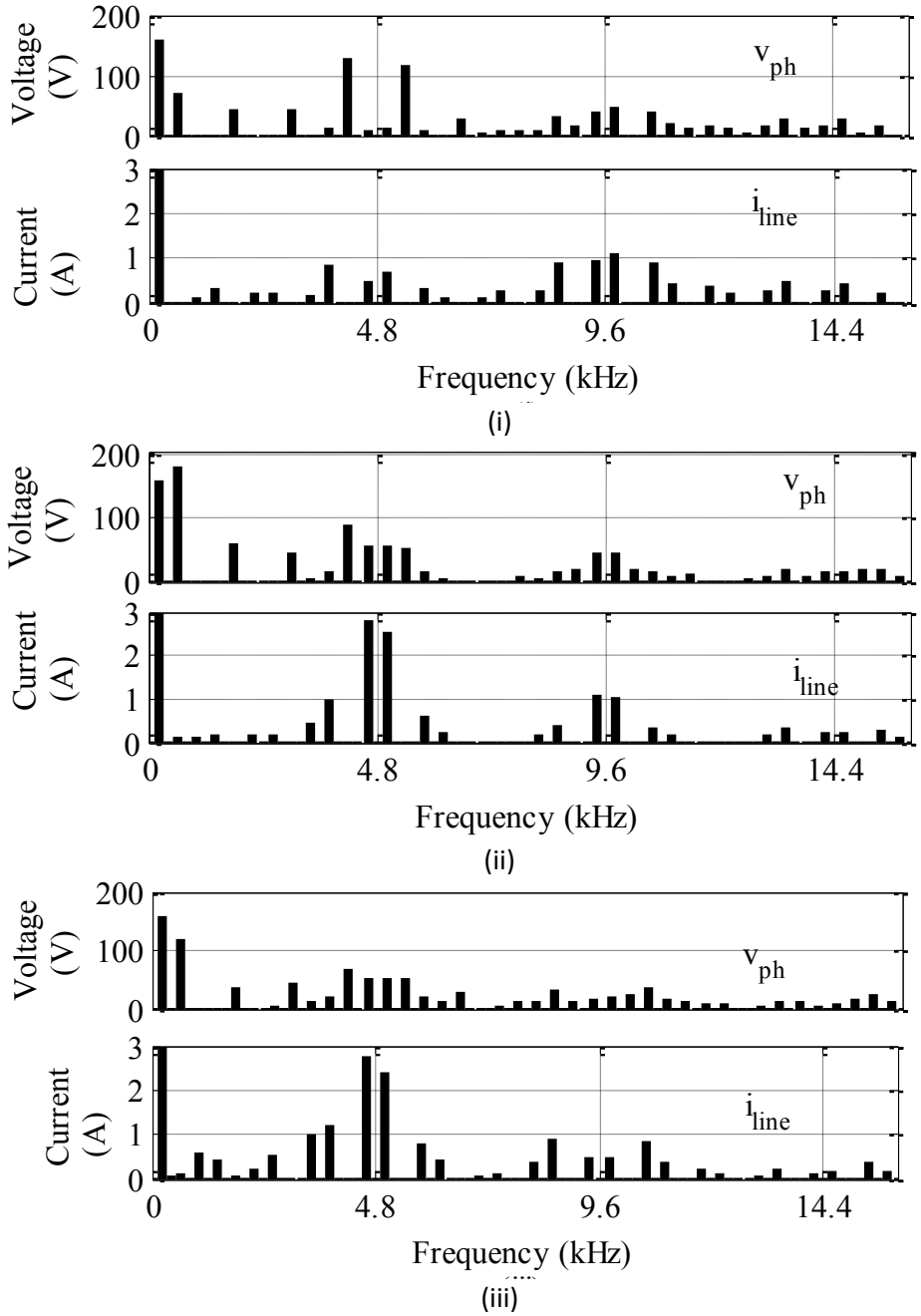


Figure 5-9. Simulation results showing harmonic spectra of phase to DC-link neutral voltage and line currents at 0.4 modulation index, 0.5 power factor, 200 Hz fundamental frequency and 4.8 kHz switching frequency for – (i) SVPWM, (ii) *DPWM2O*, and (iii) *DPWMLPF2*.

- With the DPWMLPF2 sequence, the WTHD of the phase-to-neutral voltage waveform is 25.2%. The dominant harmonic of the line current is around the switching frequency and the THD of line current is 4.6%, like DPWM20 sequence.

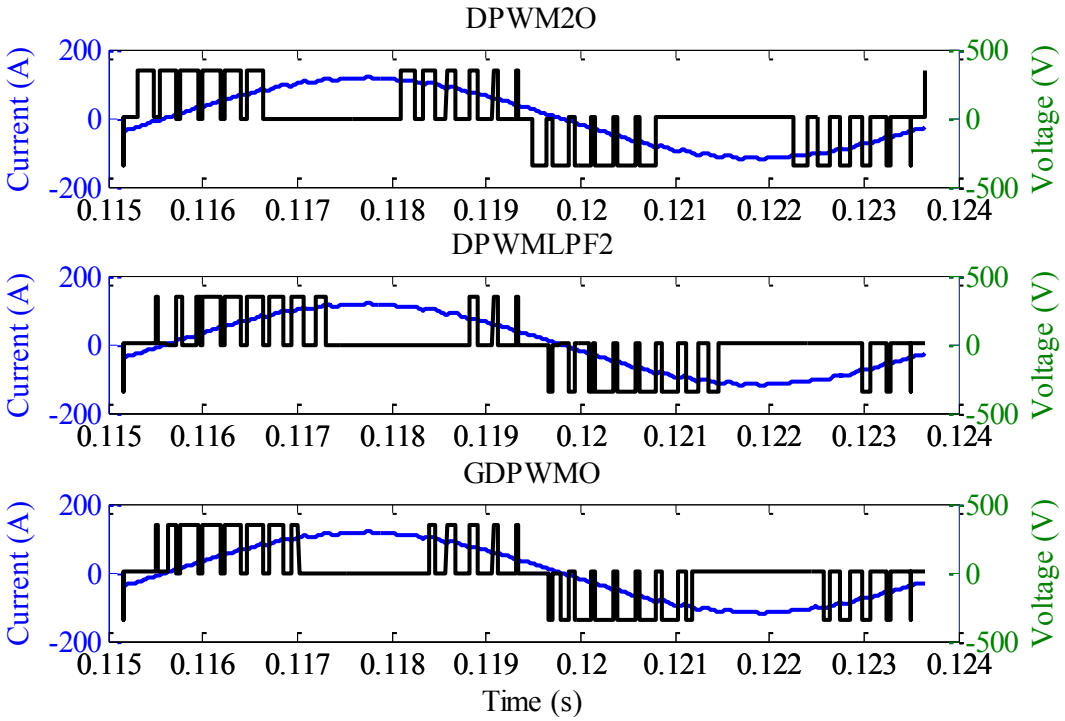


Figure 5-10. Simulation results showing phase to DC-link neutral voltage and line currents at 0.4 modulation index, 0.707 power factor, 120 Hz fundamental frequency and 4.32 kHz switching frequency for – (i) DPWM2O, (ii) *DPWMLPF2*, and (iii) *GDPWMO*.

Case II: *GDPWMO Power factor angle 45°, 120 Hz fundamental frequency and 4.32 kHz switching frequency*

Fig. 5-10 shows a comparison of DPWM2O, DPWMLPF2 and GDPWMO at 0.4 modulation index, and Fig. 5-11 shows the harmonic spectra of the line currents. The DPWM2O and DPWMLPF2 strategies produce 12 pulses in one half cycle, whereas the GDPWMO strategy has 13 pulses. However, the clamping interval of the GDPWMO strategy is aligned with the line current peaks, whereas the DPWM2O and DPWMLPF2 strategies incurs switching instances around the current peaks. Hence, as discussed earlier, the GDPWMO strategy will decrease the switching losses incurred by the three-level inverter.

The line current THD values are: - (i) DPWM2O - 2.21%, (ii) DPWMLPF2 – 2.23% and (iii) GDPWMO – 2.15%. Hence it can be concluded that they create similar output current distortion. However, from Fig. 5-11, GDPWMO spreads the spectrum compared to the DPWM2O and DPWMLPF2. This can be attributed to the use of two different DPWM templates within one fundamental cycle.

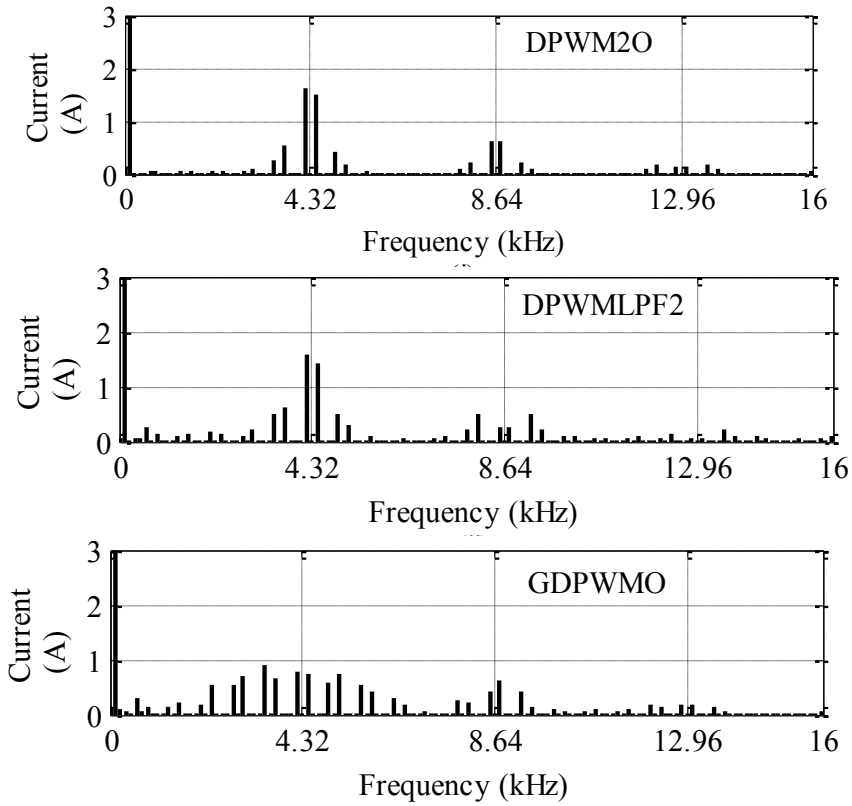


Figure 5-11. Simulation results showing harmonic spectra of line currents at 0.4 modulation index, 0.707 power factor, 120 Hz fundamental frequency and 4.32 kHz switching frequency for –DPWM2O, *DPWMLPF2*, and *GDPWMO*.

Simulated switching loss function (SLF) magnitudes

Fig. 5-12 shows the switching loss function using the DPWM2O, DPWMLPF2 and GDPWMO templates in comparison to the conventional SVPWM sequence for 30°-60° power

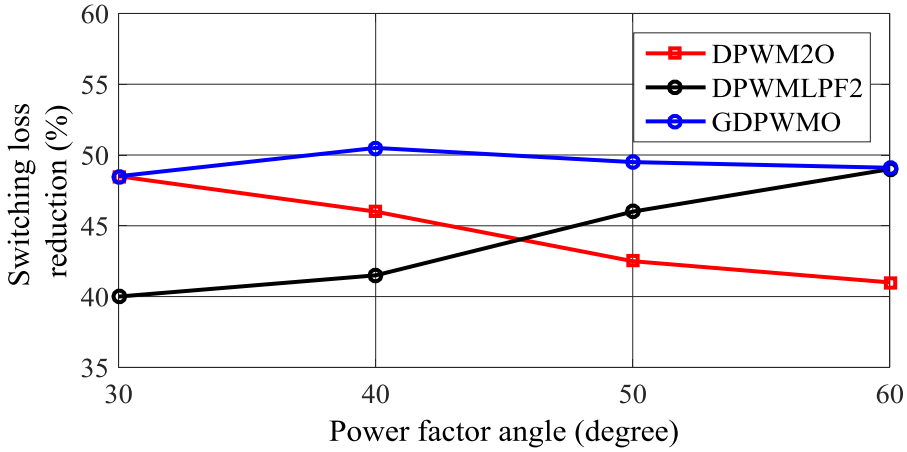


Figure 5-12. Comparisons of switching loss reduction using *DPWM2O*, *DPWMLPF2* and *GDPWMO* sequences for different operating power factor

TABLE 5-4: SUMMARY OF SIMULATION RESULTS

Case	Number of pulses	THD (%)	Switching loss reduction (%)
SVPWM – 0.5 pf	13	2.84	N/A
DPWM2O – 0.5 pf	9	4.6	40
DPWMLPF2 – 0.5 pf	9	4.6	50
DPWM2O– 0.707 pf	12	2.21	44
DPWMLPF2 – 0.707 pf	12	2.23	44
GDPWMO – 0.707 pf	13	2.15	50

factor angle range. Like the analytical results, the DPWM2O and DPWMLPF2 templates provide maximum switching loss reduction only at power factor angles 30° and 60°, respectively. In other power factor angles between 30° and 60°, their loss reduction capability reduces. On the other hand, the GDPWMO strategy reduces switching losses around 50% for all the power factor angles.

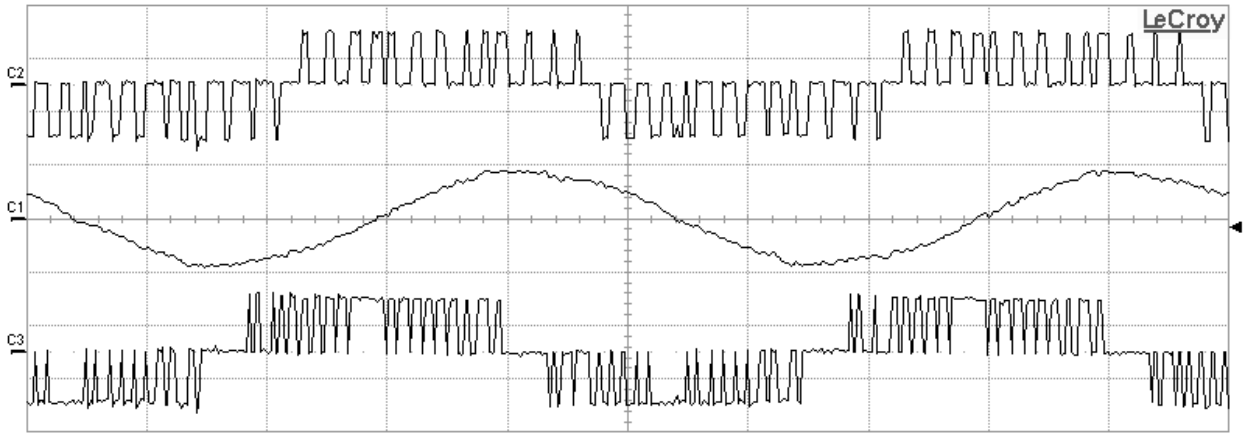
The simulation results have been summarized in Table 5-4.

5.6 Experimental Results

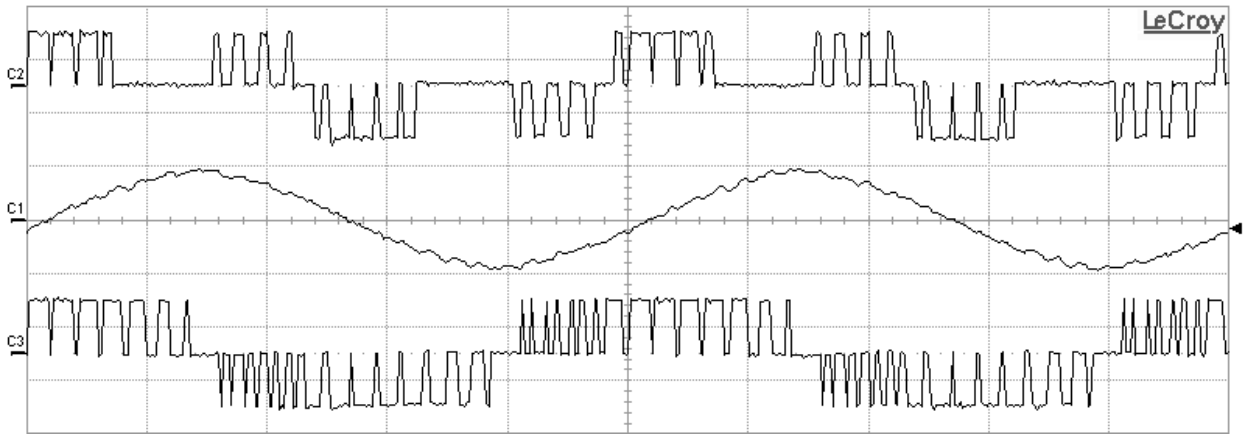
The switching strategies have been implemented on a scaled down three-level T-NPC hardware setup, as shown in Fig. 4-17. The results have been obtained with the three-level T-NPC inverter feeding a passive R-L load. The proposed control strategies are implemented using OPAL-RT based real time prototyping tool. The operational time-step is kept constant at 25 µs.

A comparison of the SVPWM, DPWM2O and DPWMLPF2 switching sequences for 0.5 power factor has been shown in Fig. 5-13. The SVPWM sequence creates 13 switching instances for every half fundamental cycle. On the other hand, both DPWM2O and DPWMLPF2 sequences create 9 switching instances, a 33% reduction compared to SVPWM. However, the clamping

intervals of the DPWM2O sequence are not aligned with the phase current peaks, whereas, with the DPWMLPF2 sequence, the clamping intervals are aligned with phase current peaks.



(i)



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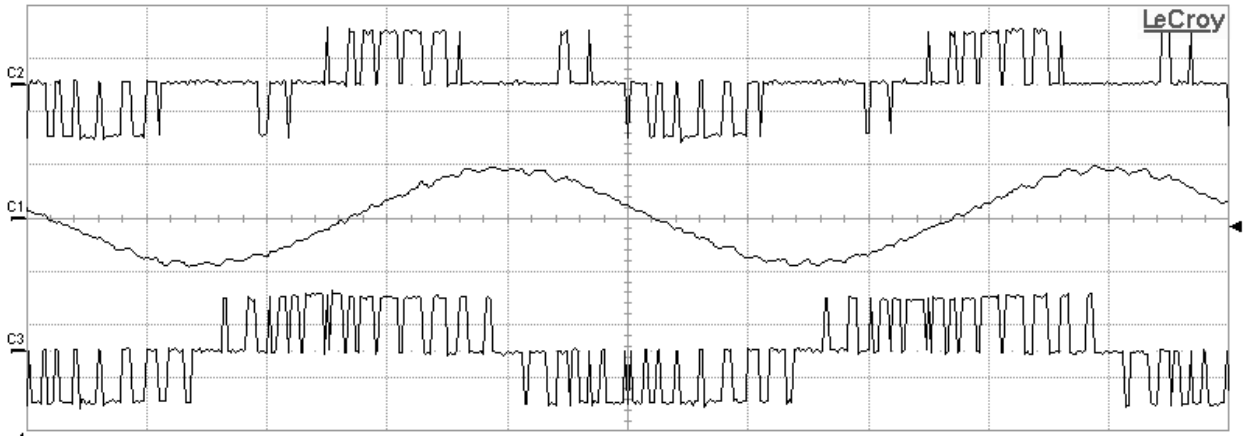


(iii)

Figure 5-13. Experimental phase-DC-link neutral voltages (V_{ph} : 100 V/div) and line currents (I_{line}:2 A/div) for (i) SVPWM, (ii) DPWM2O, and (iii) DPWMLPF - experimental conditions (modulation index: 0.4, fundamental frequency: 200 Hz, switching frequency: 4800 Hz, power factor: 0.5, time step: 1 ms/div).

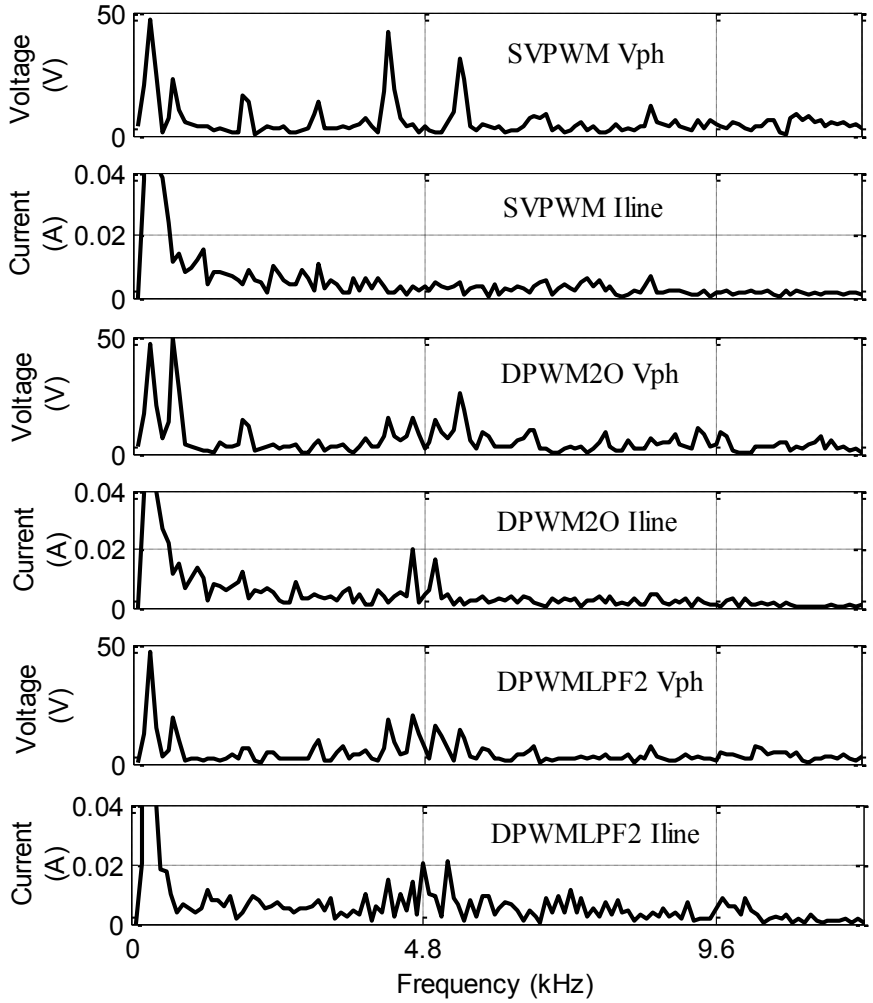


Figure 5-14. Experimental phase-DC-link neutral voltages' and line currents' harmonic spectra for SVPWM, DPWM2O, and *DPWMLPF2* - experimental conditions (modulation index: 0.4, fundamental frequency: 200 Hz, switching frequency: 4800 Hz, power factor: 0.5, time step: 1 ms/div). Red rectangles show current peaks

The harmonic spectra of Fig. 5-14 show similar characteristic as simulation results in Fig. 5-9. The line current THD values are: - (i) SVPWM – 3.4%, (ii) DPWM2O – 5.1% and (iii) DPWMLPF2 – 5.2%. Hence it can be concluded that the proposed DPWM templates do not deteriorate the waveform quality compared to conventional DPWM strategies.

EIF of DPWM2O and DPWMLPF2 techniques have been measured at 0.4 modulation index and 0.5 power factor for three different operating switching frequencies – 4.8, 6 and 7.2 kHz. The results are shown in Fig. 5-15 and Table 5-5. It shows that with the DPWMLPF2 strategy, the EIF's are always higher than DPWM2O strategies. The average EIF of DPWMLPF2 is 11 % whereas for

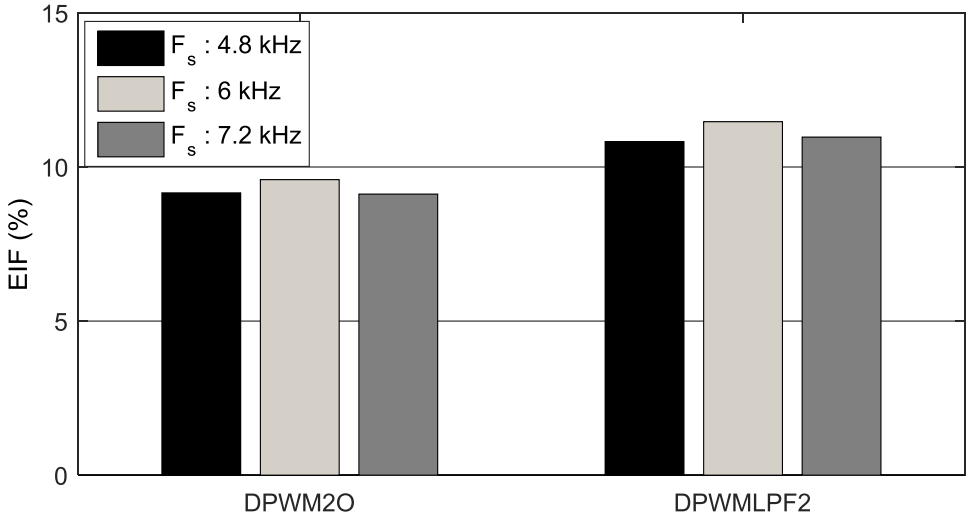
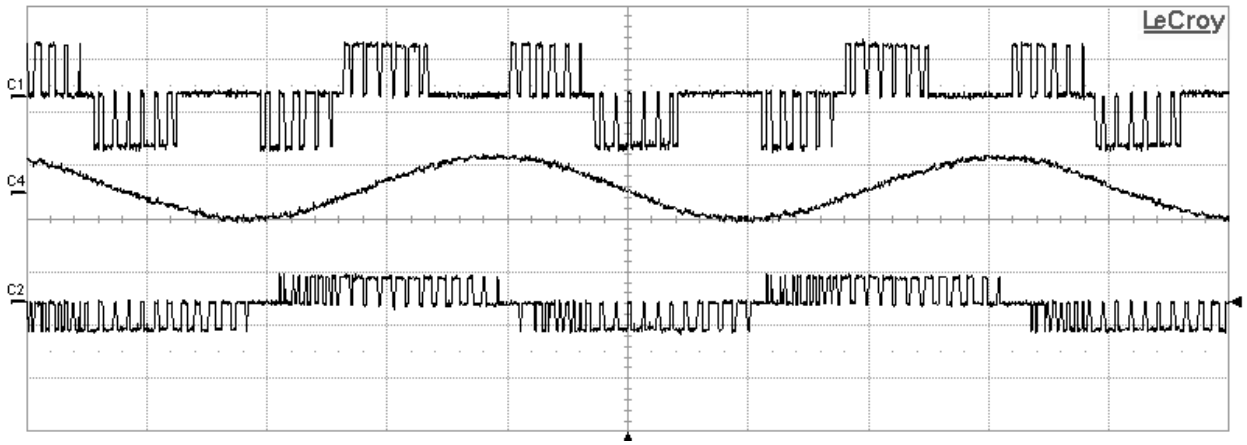


Figure 5-15. Experimental efficiency improvement factor (EIF) using DPWM2O and DPWMLPF2 in comparison to conventional SVPWM strategy at 0.4 modulation index and 0.5 power factor

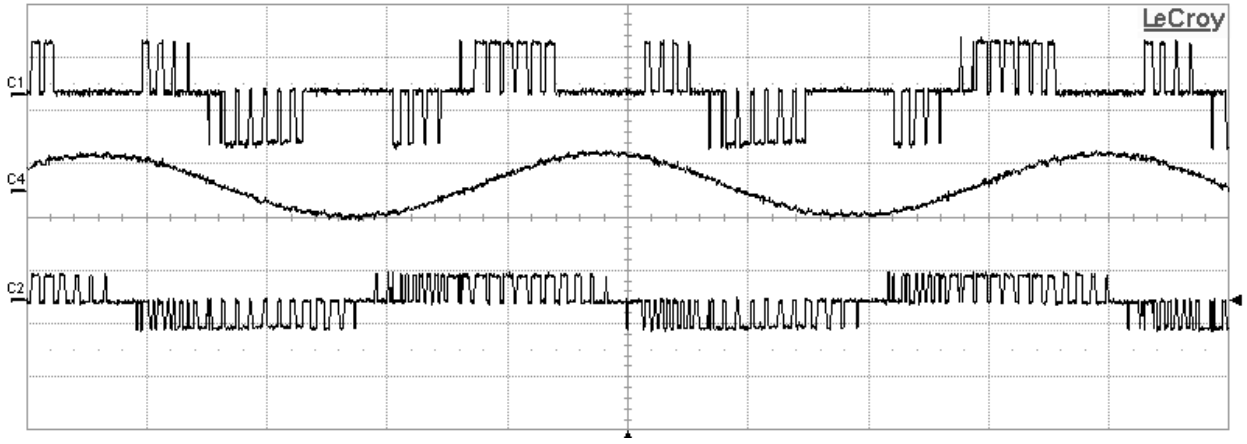
TABLE 5-5: EXPERIMENTALLY MEASURED EFFICIENCY AND EIF

PWM type		Mod. index	Efficiency (%)	EIF (%)
Switching Frequency: 4.8 kHz	SVPWM	0.2	68.6	-
		0.4	77.8	-
	DPWM2O	0.2	72.3	5.4
		0.4	84	8
	DPWMLPF2	0.2	72.7	6
		0.4	87	12
Switching Frequency: 6 kHz	SVPWM	0.2	66.6	-
		0.4	77.2	-
	DPWM2O	0.2	70.72	6.2
		0.4	84.1	9
	DPWMLPF2	0.2	71.7	7.6
		0.4	87.2	13
Switching Frequency: 7.2 kHz	SVPWM	0.2	66	-
		0.4	77	-
	DPWM2O	0.2	70.75	7.2
		0.4	83.16	8
	DPWMLPF2	0.2	71.15	7.8
		0.4	86	12

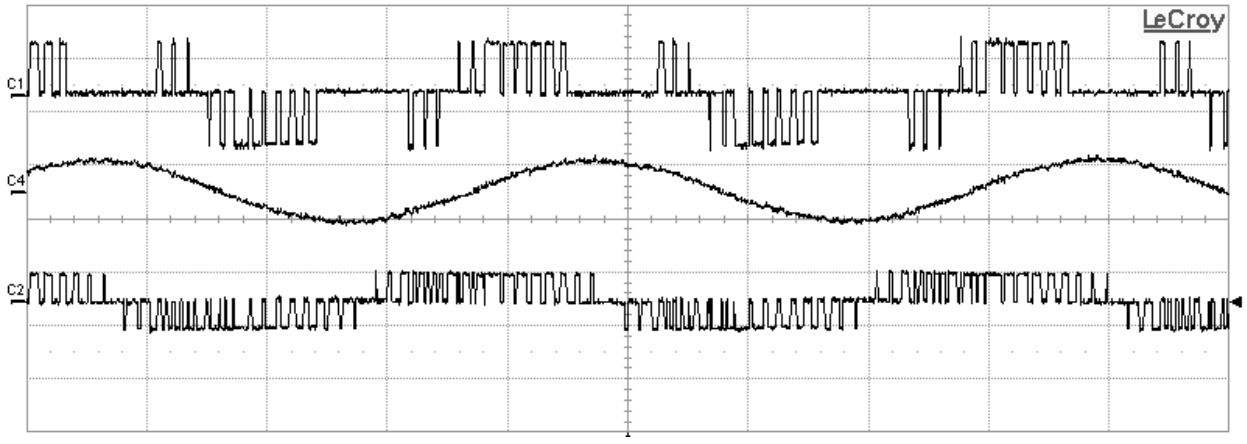
DPWM2O, it is around 8 %. Thus, like the analytical and simulation results, the experimental results show that the proposed sequences reduce the inverter losses more in comparison to



(i)



(ii)



(iii)

Figure 5-16. Experimental phase-DC-link neutral voltages (V_{ph} : 100 V/div) and line currents (I_{line}:2 A/div) for (i) SVPWM, (ii) DPWM2O, and (iii) DPWMLPF - experimental conditions (modulation index: 0.4, fundamental frequency: 200 Hz, switching frequency: 4800 Hz, power factor: 0.5, time step: 1 ms/div). conventional DPWM sequences.

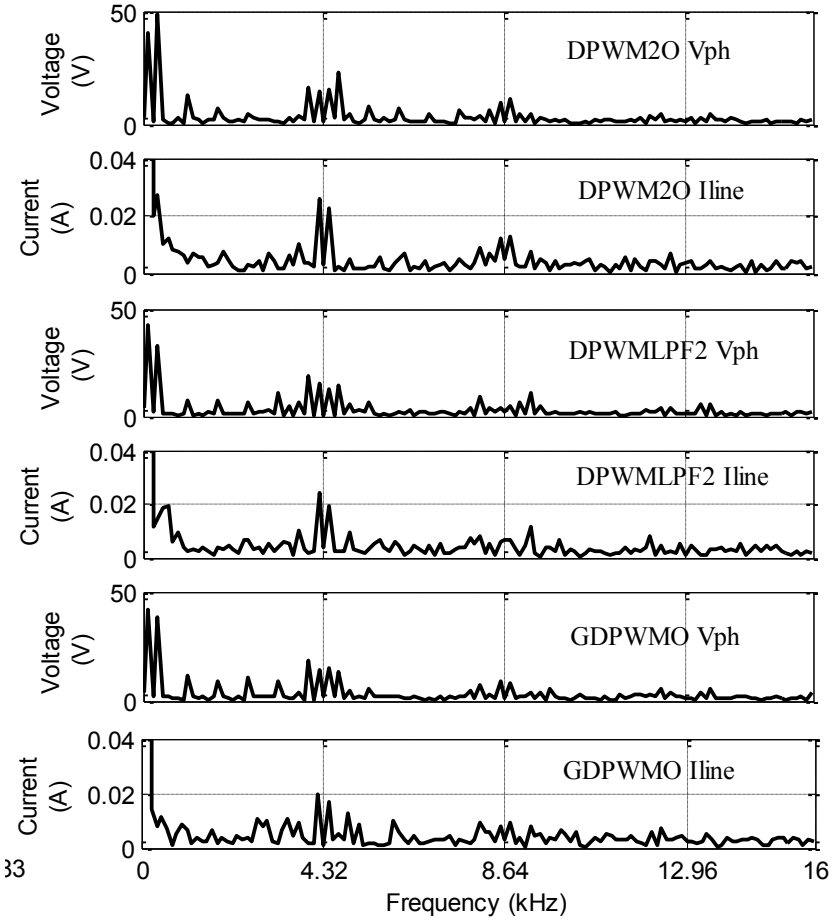


Figure 5-17. Experimental (i) phase-DC-link neutral voltages, line currents, and (ii) their harmonic spectra for DPWM2O, *DPWMLPF2* and *GDPWMO* - experimental conditions (modulation index: 0.4, fundamental frequency: 120 Hz, switching frequency: 4320 Hz, power factor: 0.707, time step: 1 ms/div). Red rectangles show current peaks

Fig. 5-16 shows a comparison of DPWM2O, DPWMLPF2 and GDPWMO at 0.4 modulation index. The inverter is operating with 120 Hz fundamental frequency and 4.32 kHz switching frequency. The output power factor angle is 45°. Each strategy produces 12-13 switching instances pulses in one half cycle. However, the clamping interval of the GDPWMO strategy is aligned with the line current peaks, whereas the DPWM2O and DPWMLPF2 strategies incurs some switchings around the current peaks, like simulation results shown before.

The line current THD values are: - (i) DPWM2O – 3.6%, (ii) DPWMLPF2 – 3.55% and (iii) GDPWMO – 3.2%. Hence it can be concluded that they create similar output current distortion, although like simulation results GDPWMO results in slightly reduced THD magnitude.

TABLE 5-6: SUMMARY OF EXPERIMENTAL RESULTS

Case	Number of pulses	THD (%)	Comment
SVPWM – 0.5 pf	13	3.4	5 Switchings around current peak
DPWM2O – 0.5 pf	9	5.1	2 Switchings around current peak
DPWMLPF2 – 0.5 pf	9	5.2	0 Switchings around current peak
DPWM2O– 0.707 pf	12	3.6	2 Switchings around current peak
DPWMLPF2 – 0.707 pf	12	3.55	2 Switchings around current peak
GDPWMO – 0.707 pf	13	3.22	0 Switchings around current peak

Additionally, from Fig. 5-17, GDPWMO spreads the current harmonic spectrum compared to the DPWM2O and DPWMLPF2. This can be attributed to the use of two different DPWM templates within one fundamental cycle.

The experimental results have been summarized in Table 5-6.

5.7 Conclusion

This chapter has proposed three space-vector based discontinuous PWM (DPWM) sequences for the three-level T-NPC inverter topology operating with power factors lower than 0.866 at modulation indices lower than 0.5. Further analysis of the proposed and conventional DPWM sequences have been done and a generalized three-level DPWM strategy has also been proposed. For all operating power factors, the proposed strategy can create PWM sequences combining the proposed and conventional DPWM sequences such that – (i) the combination

requires one switching transition only, and (ii) the no-switching durations of the created sequence is aligned with the respective current peaks. Analytical and implementation results demonstrate that the strategy ensures no switching instances around current peaks and consequently reduces inverter switching losses up to 50% at all operating power factors.

In the chapters 4 and 5, few improved PWM strategies are proposed, while the switching frequency over a fundamental cycle remain constant. In the following chapter, a variation of operating switching frequency within a fundamental cycle is proposed, and resulting inverter switching loss reduction is discussed.

6 Sub-fundamental Cycle Switching Frequency Variation Strategy

6.1 Overview

This chapter investigates general principles of sub-fundamental cycle current ripple variation of a three-level voltage-source inverter. The investigation employs three-level space-vector based continuous and discontinuous pulse-width modulation strategies to analyze the current ripple variation over one 60-degree sector and entire operating modulation index, including the over-modulation index range. Based on the current ripple variation, a methodology is used to change the operating switching frequency within a fundamental cycle. The results demonstrate that the proposed strategy reduces inverter switching instances and associated losses around 10-30%.

6.2 Introduction

Like a two-level inverter, the three-level inverter modulation and control strategies are aimed to reduce the device losses while maintaining the output current distortion within acceptable limits. These strategies include:

- *Different variants of PWM strategy:* Typically, three-level inverters employ conventional Space-vector PWM (SVPWM) sequence [98]. To reduce inverter switching losses in comparison to the SVPWM sequence, different variants of three-level discontinuous PWM (DPWM) strategies – DPWM0-2 [105,107] are also widely used. These PWM strategies impact the inverter switching losses and output waveform distortion in different ways, as reported in [77].
- *Variation in switching frequency:* A lower operating switching frequency reduces the switching losses, whereas, it increases the switching frequency ripple on the inverter output current waveform. Typically, in an inverter, the operating switching frequency is varied based on either current distortion at operating modulation indices (speed) or operating current

(torque) magnitude [133-135]. In these situations, the switching frequency is normally varied over a few fundamental cycles and remain constant within a fundamental operating cycle.

As discussed in [18], [11]- [19], the peak-peak output current ripple of a two-level inverter does not remain constant within a fundamental cycle, and varies based on the position of voltage vector and the operating modulation index. Similar analyses have also been conducted for dual two-level [136], multi-level [137], [138] and multi-phase inverters in [139]- [141]. In [137], an analysis for sub-fundamental cycle current ripple variation for a three-level inverter has been done, however, the authors did not look analyzing with respect to position of the voltage vector and modulation index. Also, the study did not look at the impact of different continuous and discontinuous three-level PWM strategies on sub-fundamental cycle current ripple in the linear and over-modulation regions.

Furthermore, several studies have been done to vary the switching frequency within a fundamental cycle based on output current ripple. Existing techniques are: (i) Variations based on the predicted current ripple envelope [37], [142]- [143], which needs computation of the switching frequency before every switching cycle, thus requiring a higher computational effort. (ii) Variations based on analytical equations which either do not follow any current ripple analysis [144], or do not provide a variation over modulation indices [145] and remain same for all PWM techniques, (iii) Variations due to use of several PWM strategies within one cycle [146], requiring a complicated implementation and (iv) Switching sequence optimization techniques [147], which only select the sequences by optimizing a cost function with multiple objectives before each switching instance, and do not explain the resulting switching frequency variation in the operating region.

6.3 Theoretical Sub-Cycle Current Ripple

In a three-level inverter, there are 27 switching states which are represented in the space vector diagram shown in Fig. 6-1 (i). In a three-level inverter, the available switching vectors are divided in four different kind of vectors which are: three zero vectors (Vzpon), twelve short vectors (Vs1-6pn), six long vectors (Vl1-6) and six medium vectors (Vm1-6). Similar to two-level space vector modulation strategy, the space-vector hexagon is divided in six sectors and each

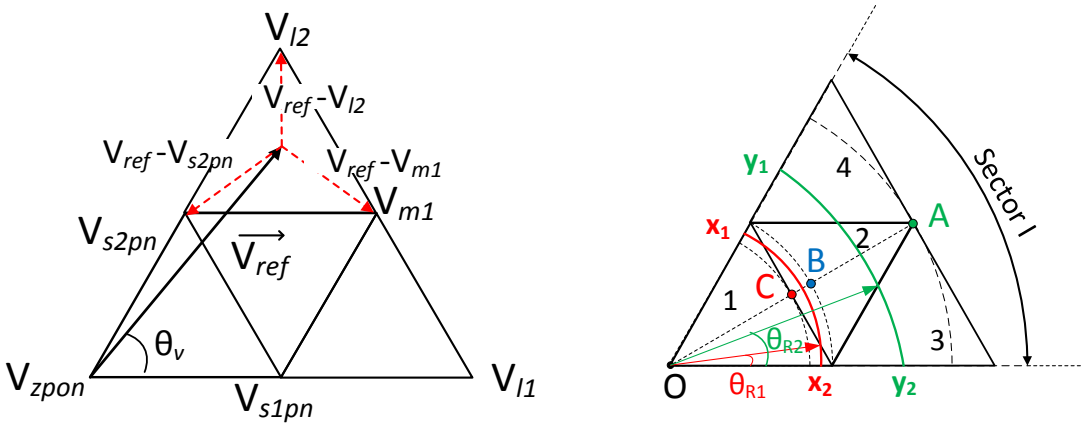


Figure 6-1. (i) Three-level space vector hexagon, switching vectors, sector I and subsector division. Also shows the deviation vectors generated because of discrete switching states of a PWM inverter, (ii) A 60-degree sector (sector I) showing subsectors, operating regions of the voltage vector and its duration of stay in different subsectors.

sector is divided in four subsectors. To synthesize a reference vector (Vref), nearest three-vectors are used to in different sequences such as continuous space-vector pulse-width modulation (CSVPWM), discontinuous PWM (DPWM). For example, as shown in Fig. 6-1(i), the reference voltage vector is inside the subsector 4 of sector 1. So, the reference voltage vector will be formed using different sequences of Vs2pn, Vl2 and Vm1 vectors.

6.3.1 Calculation of Duration of Stay in a Sub-Sector

As seen from Fig. 6-1 (ii), based on operating modulation index, the voltage vector can be within three different operating regions. These are: (i) Region I: Circle of radius OC - $0 \leq m \leq 0.5$, (ii) Region II: between Circle of radius OC and OB - $0.5 \leq m \leq 0.577$, and (iii) Region III: between Circle of radius OB and OA - $0.577 \leq m \leq 1$. So, the current ripple and possible switching frequency variations are calculated for all three- regions. It is also important to notice that – (i) in region I, the voltage vector stays within subsector 1, (ii) in region II, the voltage vector rotates within subsector 1 and subsector 2, and (iii) in region III, the voltage vector rotates within subsector 2, 3 and 4. With change in modulation index, their duration of stay within a sector also changes.

TABLE 6-1: DURATION OF STAY IN SUB-SECTORS

Region	Sub-sector	Duration of stay	Angle Information
II	1	$0 \le \theta \le \theta_{R2}$	$\theta_{R2} = \sin^{-1}\left(\frac{1-\sqrt{12m^2-3}}{4m}\right)$
	2	$\theta_{R2} \le \theta \le {}^{\pi}/_{3} - \theta_{R2}$	
	1	${}^{\pi}/_{3} - \theta_{R2} \le \theta \le {}^{\pi}/_{3}$	
III	3	$0 \le \theta \le \theta_{R3}$	$\theta_{R3} = \sin^{-1}\left(\frac{\sqrt{12m^2-3}-1}{4m}\right)$
	2	$\theta_{R3} \le \theta \le {}^{\pi}/_{3} - \theta_{R3}$	
	4	${}^{\pi}/_{3} - \theta_{R3} \le \theta \le {}^{\pi}/_{3}$	

Referring to Fig. 6-1(ii), consider in region II, the reference voltage vector is following the arc x1x2 at a modulation index m. The position of the reference voltage vector is shown in Table 6-1. It shows that, depending on modulation index value, the duration of stay within subsector 1 and subsector 2 changes. Similarly, consider in region III, the reference voltage vector is following the arc y1y2 at a modulation index. The position of the reference voltage vector is shown in Table 6-1 and it shows that depending on the modulation index value, the duration of stay within subsector 2, 3 and 4 changes.

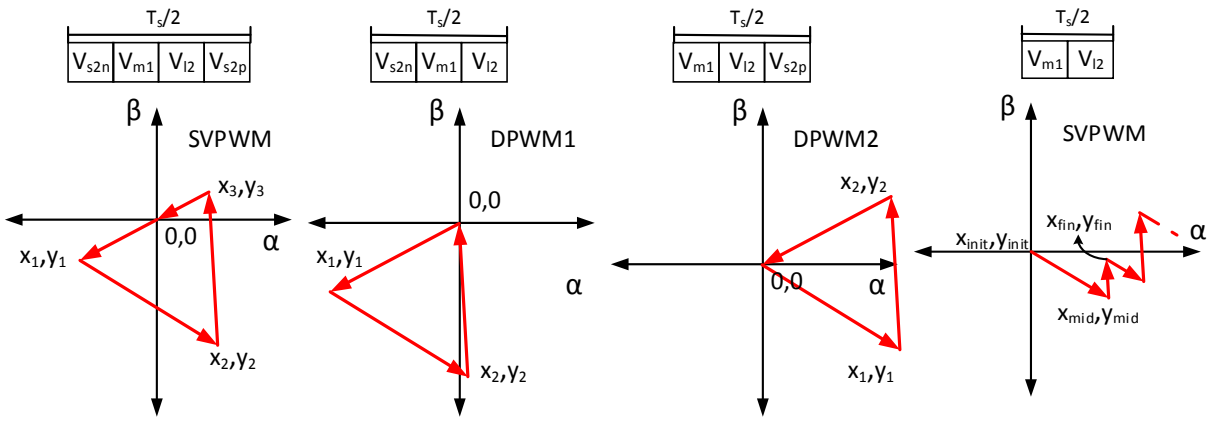
6.3.2 Calculation of Current Ripple

As the reference voltage vector is formed using discrete switching vectors, the operating voltage vector does not follow the reference trajectory [11]. The deviations between applied switching vector and reference voltage vector results in the ripple in the output current waveform. For any switching instance, the instantaneous current ripple due to application of i^{th} switching vector (i.e. application corresponding voltage vector Vi) can be written as

$$\frac{\mathrm{d}\overrightarrow{\Delta \mathrm{I}}}{\mathrm{dt}} = \frac{1}{\mathrm{L}}\left[\vec{V_i} - \overrightarrow{V_{ref}}\right] \tag{6.1}$$

Thus, the trajectory of current ripple, ΔI in the half-switching cycle is given by

$$\overrightarrow{\Delta \mathrm{I}} = \int_{t=0}^{t=\frac{Tsw}{2}} \frac{1}{\mathrm{L}}\left[\vec{V_i} - \overrightarrow{V_{ref}}\right] dt \tag{6.2}$$



(i) (ii) (iii) (iv)

Figure 6-2. Current ripple trajectory in a PWM technique in subsector 4, sector I for - (i) Continuous SVPWM, (ii) Discontinuous PWM1, (iii) Discontinuous PWM2 and (iv) over-modulation region for SVPWM and DPWM strategies where short vectors are not used. Ts corresponds to one switching period

This ΔI comprises of current ripple contribution from all the three phases [2, 8]

If the vertices of the current ripple trajectory are known, shown in Fig. 6-2 (i-iii) for SVPWM, DPWM1 and DPWM2 respectively, then the above equation can be numerically approximated using the following equation [148]- [149].

$$\left|\overrightarrow{\Delta I}\right|^2 = \sum_i t_i[{x_i}^2 + {x_{i+1}}^2 + {y_i}^2 + {y_{i+1}}^2 + x_i x_{i+1} + y_i y_{i+1}] \tag{6.3}$$

where (xi, yi) are the points corresponding to the vertices of the current ripple trajectory. As SVPWM and DPWM techniques use different switching sequences, the current ripple trajectories of them are also different. In this section, the trajectories of SVPWM, DPWM1 and DPWM2 sequences are analyzed. An analysis for operation in over-modulation region is also provided.

Space-Vector PWM Current Ripple Analysis

The trajectory of the current ripple for SVPWM in subsector 3, sector 1 is shown in Fig. 6-2 (i). The current ripple equations for SVPWM is:

$$\overrightarrow{\Delta I} = \frac{1}{L}\left[\overrightarrow{V_{s2n}} - \overrightarrow{V_{ref}}\right]\frac{t_{s2n}}{4} + \frac{1}{L}\left[\overrightarrow{V_{m1}} - \overrightarrow{V_{ref}}\right]\frac{t_{m1}}{2} + \frac{1}{L}\left[\overrightarrow{V_{l2}} - \overrightarrow{V_{ref}}\right]\frac{t_{l2}}{2} + \frac{1}{L}\left[\overrightarrow{V_{s2p}} - \overrightarrow{V_{ref}}\right]\frac{t_{s2p}}{4} \quad (6.4)$$

Referring to Fig. 6-2(i), in one half-cycle, due to use of four voltage vectors, the trajectory of the current ripple vector creates four corner points, one of them is (0,0). Other corner points (x1-3 and y1-3) have been provided in Table 6-2. Based on these four corner points and using Eqn. 6.3, the current ripple variation for SVPWM technique in subsector 4 of sector 1 is obtained. Similar operation is followed to obtain current ripple variation in other subsectors. The variation is shown in Fig. 6-3 (i) for one sector.

The current ripple in a sector is low at low modulation indices. In comparison to two-level inverter [11], at low modulation index, current ripple does vary over position of voltage vector. At higher modulation index, current ripple is lowest near those regions where maximum possible use of short vectors and medium vectors is achievable.

Discontinuous PWM1 Current Ripple Analysis

The trajectory of the current ripple for DPWM1 in sector 1 is shown in Fig. 6-2 (ii). The respective current ripple equations for DPWM2 are as follows:

$$\overrightarrow{\Delta \mathrm{I}} = \frac{1}{L}\left[\overrightarrow{V_{s2n}} - \overrightarrow{V_{ref}}\right]\frac{t_{s2n}}{4} + \frac{1}{L}\left[\overrightarrow{V_{m1}} - \overrightarrow{V_{ref}}\right]\frac{t_{m1}}{2} + \frac{1}{L}\left[\overrightarrow{V_{l2}} - \overrightarrow{V_{ref}}\right]\frac{t_{l2}}{2} \quad (6.5)$$

Referring to Fig. 6-2(ii), in one half-cycle, due to use of three voltage vectors, the trajectory of the current ripple vector creates three corner points, one of them is (0,0). Other corner points (x1-2 and y1-2) have been provided in Table 6-2. Based on these three corner points and using Eqn. 6.3, the current ripple variation in subsector 4 of sector 1 is obtained. The variation with respect to modulation index and position of voltage vector is shown in Fig. 6-3 (ii).

Discontinuous PWM2 Current Ripple Analysis

The trajectory of the current ripple for DPWM2 in sector 1 is shown in Fig. 6-2 (iii). The respective current ripple equations for DPWM2 are as follows:

$$\overrightarrow{\Delta \mathrm{I}} = \frac{1}{L}\left[\overrightarrow{V_{m1}} - \overrightarrow{V_{ref}}\right]\frac{t_{m1}}{2} + \frac{1}{L}\left[\overrightarrow{V_{l2}} - \overrightarrow{V_{ref}}\right]\frac{t_{l2}}{2} + \frac{1}{L}\left[\overrightarrow{V_{s2p}} - \overrightarrow{V_{ref}}\right]\frac{t_{s2p}}{4} \quad (6.6)$$

Referring to Fig. 6-2(iii), in one half-cycle, due to use of three voltage vectors, the trajectory of the current ripple vector creates three corner points, one of them is (0,0). Other corner points (x1-2 and y1-2) have been provided in Table 6-2. Based on these three corner points and using Eqn. 6.3, the current ripple variation in subsector 4 of sector 1 is obtained. Similar operation is followed to obtain current ripple variation in other subsectors of sector 1. The variation with respect to modulation index and position of voltage vector is shown in Fig. 6-3 (iii).

Hence, for DPWM1 and DPWM2 strategies, the current ripple variations in a fundamental cycle are low at low modulation indices and does not vary much over position of the voltage vector. Above 0.5 modulation index, current ripple variation trajectory is like SVPWM.

Over-Modulation Region Current Ripple Analysis

In the over-modulation region (m≥1), for a certain time [150], the switching strategies select three-nearest active vectors to synthesize the reference voltage vector when the reference voltage vector trajectory is within the space vector hexagon. When the circular trajectory is outside, the switching strategy only switches between the active vectors. Hence, the resulting current ripple will have a different shape in that region, and will be same for SVPWM and DPWM techniques.

As shown in Fig. 6-2(iv), as the zero vector is not used in that region, the resulting current ripple vector does not form a current ripple triangle as before. Thus, the ripple magnitude increases. This can be written as:

$$\overrightarrow{\Delta \mathrm{I}_{new}} = \overrightarrow{\Delta \mathrm{I}_{old}} + \frac{1}{\mathrm{L}}\left[\overrightarrow{\mathrm{V_{m1}}} - \overrightarrow{\mathrm{V_{ref}}}\right]\frac{\mathrm{t_{m1}}}{2} + \frac{1}{\mathrm{L}}\left[\overrightarrow{\mathrm{V_{l2}}} - \overrightarrow{\mathrm{V_{ref}}}\right]\frac{\mathrm{t_{l2}}}{2} \quad (6.7)$$

Referring to Fig. 6-2(iv), in one half-cycle, due to use of three voltage vectors, the trajectory of the current ripple vector creates three corner points, one of them is (0,0) at the first switching cycle and in the next cycles is (xinit and yinit). Other corner points (xmid ,ymid and xfin ,yfin) have been provided in Table 6-2. Based on these three corner points and using Eqn. 6.34,

TABLE 6-2: CORNER POINTS FOR PWM STRATEGIES AT SUBSECTOR 4, SECTOR I

Technique	Corner points **(x_i, y_i)**
SVPWM	$x_1 = 0.25t_{s2n}\left(\frac{1}{2\sqrt{3}} - m\cos\theta_v\right)$, $y_1 = 0.25t_{s2n}\left(\frac{1}{2} - m\sin\theta_v\right)$ $x_2 = x_1 + 0.5t_{m1}\left(\frac{\sqrt{3}}{2} - m\cos\theta_v\right)$, $y_2 = y_1 + 0.5t_{m1}\left(\frac{1}{2} - m\sin\theta_v\right)$ $x_3 = -x_1$, $y_3 = -y_1$
DPWM1	$x_1 = 0.5t_{s2n}\left(\frac{1}{2\sqrt{3}} - m\cos\theta_v\right)$, $y_1 = 0.5t_{s2n}\left(\frac{1}{2} - m\sin\theta_v\right)$ $x_2 = x_1 + 0.5t_{m1}\left(\frac{\sqrt{3}}{2} - m\cos\theta_v\right)$, $y_2 = y_1 + 0.5t_{m1}\left(\frac{1}{2} - m\sin\theta_v\right)$
DPWM2	$x_1 = 0.5t_{m1}\left(\frac{\sqrt{3}}{2} - m\cos\theta_v\right)$, $y_1 = 0.5t_{m1}\left(\frac{1}{2} - m\sin\theta_v\right)$ $x_2 = -0.5t_{s2p}\left(\frac{1}{2\sqrt{3}} - m\cos\theta_v\right)$, $y_2 = -0.5t_{s2p}\left(\frac{1}{2} - m\sin\theta_v\right)$
Over-modulation	$x_{init} = x_{fin\_old}$, $y_{init} = y_{fin\_old}$ $x_{mid} = x_{init} + 0.5t_{m1}\left(\frac{\sqrt{3}}{2} - m\cos\theta_v\right)$, $y_{mid} = y_{init} + 0.5t_{m1}\left(\frac{1}{2} - m\sin\theta_v\right)$; $x_{fin} = x_{mid} + 0.5t_{l2}\left(\frac{1}{\sqrt{3}} - m\cos\theta_v\right)$, $y_{fin} = y_{mid} + 0.5t_{l2}(1 - m\sin\theta_v)$

the current ripple variation in subsector 4 of sector 1 is obtained. The variation with respect to modulation index and position of voltage vector is shown in Fig. 6-4. It shows that in the over-modulation range, there is more variation of current ripple due to use of only active vectors. Beyond 1.05 modulation index, current ripple variation exists only for those regions where switching between active vectors exists. In other regions, the voltage vector remains fixed to one of the active voltage vector as the operation continues towards a square-wave operation [150].

6.4 Switching Frequency Variation Methodology

Figs. 6-3 and 6-4 show the current ripple variation within a sector over the entire modulation index range for SVPWM, DPWM1 and DPWM2 techniques. They show that at a modulation index, the current ripple is high only at certain regions of the sector. Thus, at a modulation index, the operating switching frequency can be reduced in the low current ripple regions of a sector while maintaining the resulting increment in the current ripple at those

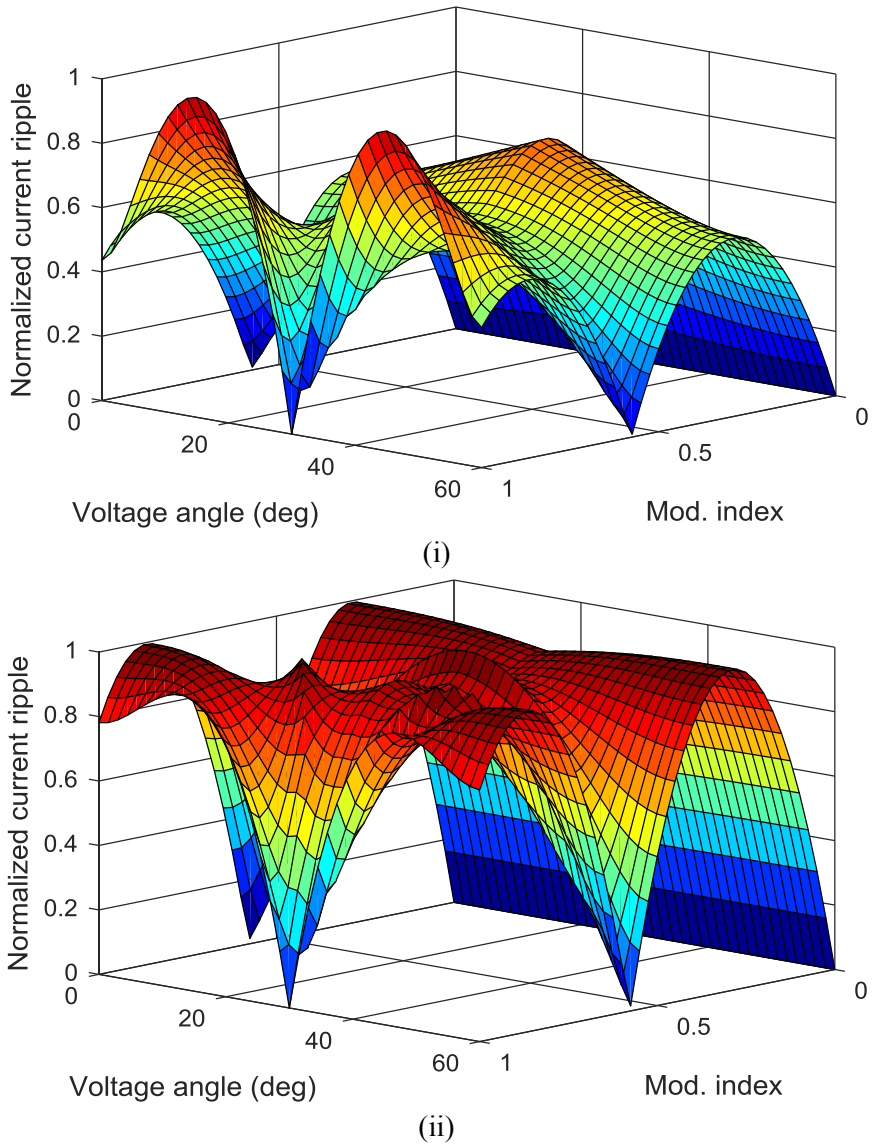
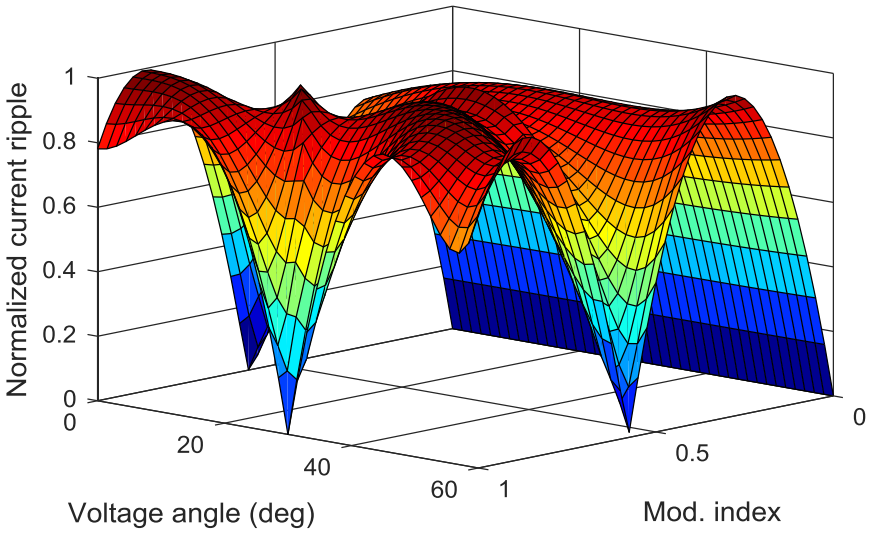


Figure 6-3. Normalized current ripple variation with respect to modulation index and position of space vector (θ_v) in sector 1 for (i) SVPWM, (ii) DPWM1

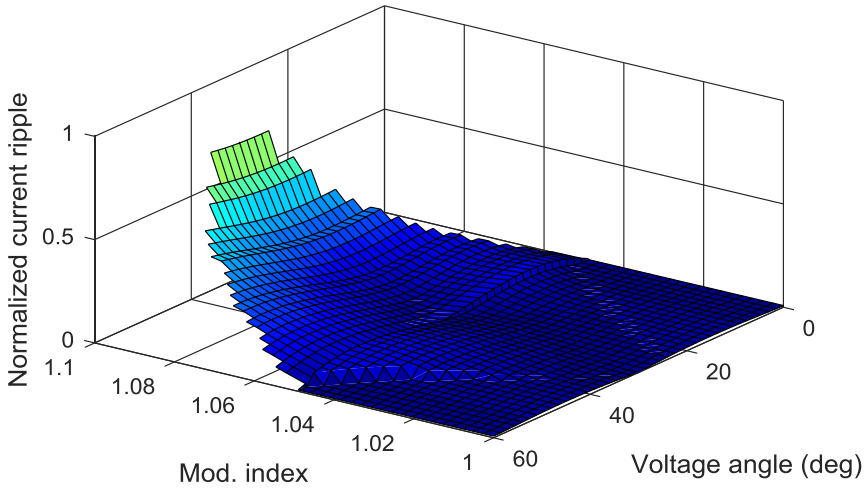
regions within the maximum ripple magnitude. In this chapter, this reduction of switching frequency within a fundamental cycle is termed as switching-cycle switching frequency variation.

To obtain a coefficient to vary the base switching frequency ($f_{sw-Base}$) based on the current ripple variation, the procedure shown in Fig. 6-5 is used. At first, the maximum current ripple of a modulation index (ΔIm), defined as

$$\Delta I_{max,m=m_1} = \max \{\Delta I(m,\theta v) \mid m = m_1\} \quad (6.8)$$



(i)



(ii)

Figure 6-4. Normalized current ripple variation and normalized switching frequency variation with respect to modulation index and position of space vector (θ_v) in sector 1 for (i) DPWM2, (ii) Over-modulation region

is obtained. In the next step, the current ripple variation matrix is divided by the maximum current ripple which provides a profile of the coefficients of switching frequency variation for each modulation index over a sector, named as Δf_{sw-nom}. This can be written as

$$\Delta f_{sw-nom}(m, \theta v) = \frac{\Delta I(m, \theta v)}{\Delta I_{max}} \tag{6.9}$$

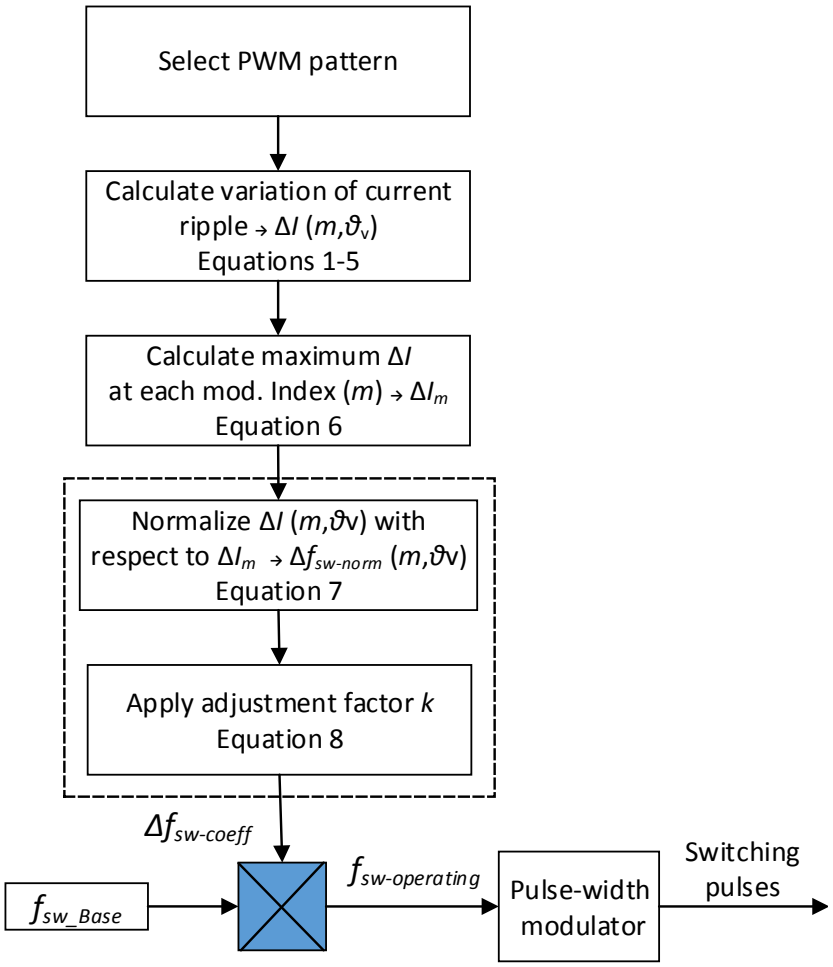


Figure 6-5. Variable switching frequency PWM strategy

The switching frequency variation plots are shown in Figs. 6-6 and 6-7 for SVPWM, DPWM1 and DPWM2 techniques. In these plots, a unity coefficient corresponds to that regions of the sector where current ripple is maximum and switching frequency cannot be reduced. At lower modulation indices, the switching frequency coefficients are around unity which can be attributed to insignificant current ripple variation over a sector. On the other hand, at higher modulation indices, the current ripple varies over a sector significantly. Thus, operating switching frequency can be reduced within a sector. For example, at 0.6 modulation index, the switching frequency coefficients vary between 0.4 to unity over a sector.

Following the sub-cycle switching frequency coefficients are calculated and stored in a look-up table (LUT) for implementation. During the operation of the inverter, based on operating

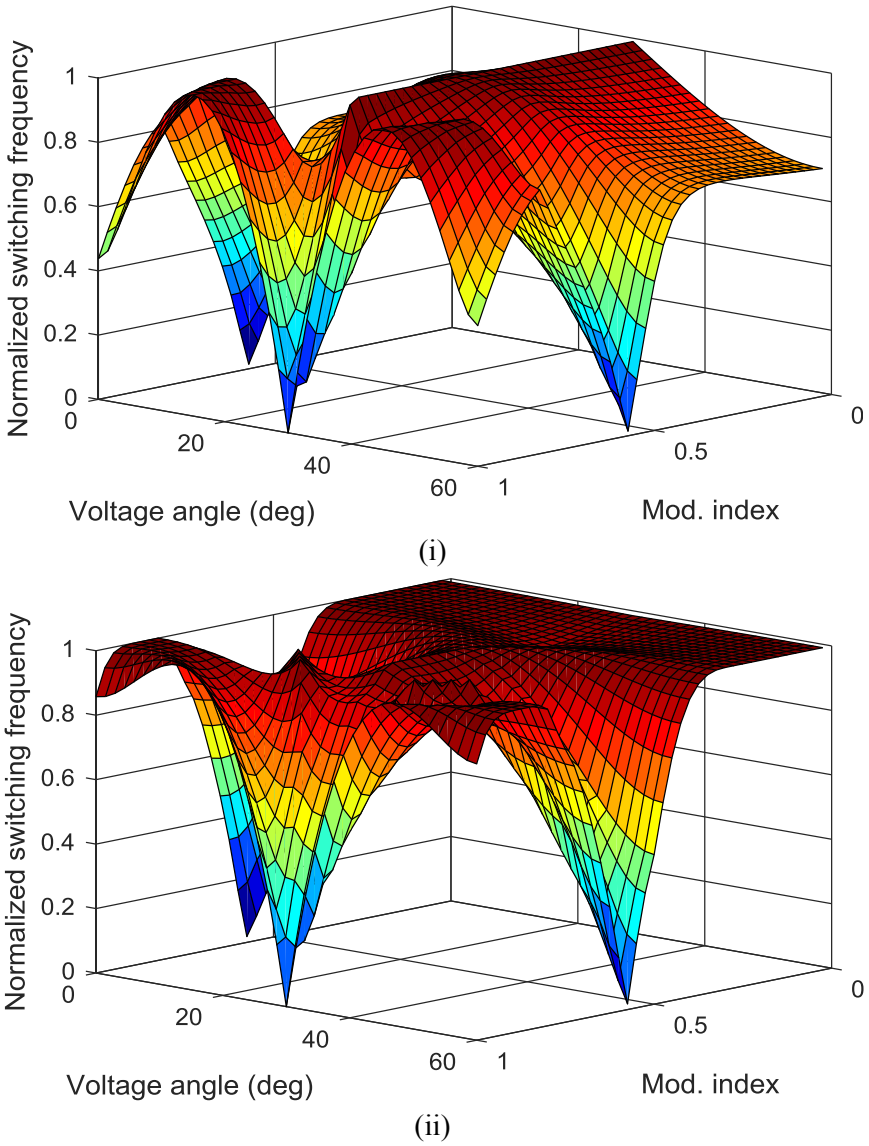
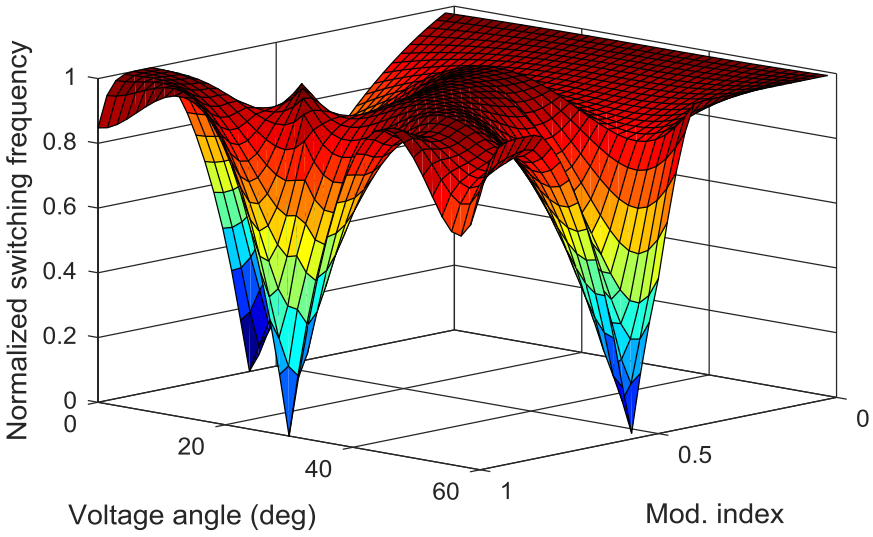


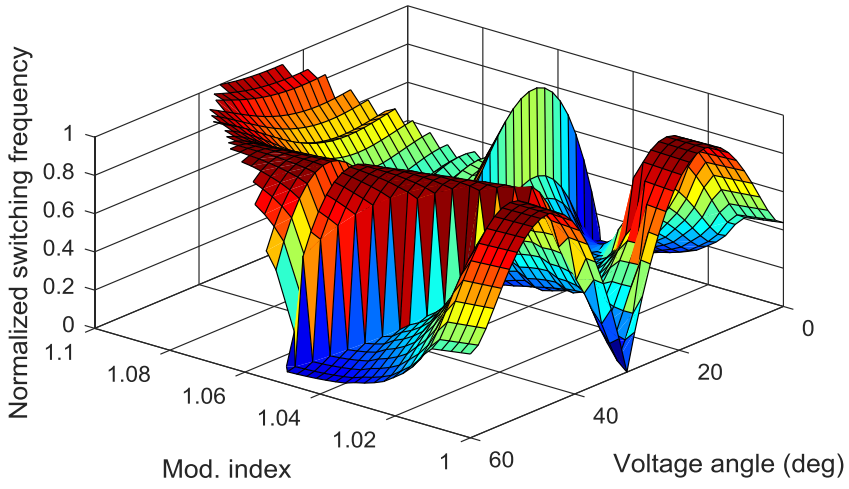
Figure 6-6. Normalized switching frequency variation with respect to modulation index and position of space vector (θ_v) in sector 1 for (i) SVPWM, (ii) DPWM1

modulation index and voltage vector angle, the LUT generates the switching frequency coefficients. An adjustment factor is applied to change the coefficients. This is needed as the theoretically calculated switching frequency variation assumes very high carrier ratio [148] which cannot be used in a practical scenario. With the adjustment factor (k) the switching frequency coefficients are:

$$\Delta f_{sw-coeff}(m, \theta v) = 1 - \left(1 - \Delta f_{sw-nom}(m, \theta v)\right) * k \quad (6.10)$$



(i)



(ii)

Figure 6-7. Normalized switching frequency variation with respect to modulation index and position of space vector (θ_v) in sector 1 for (i) DPWM2, (ii) Over-modulation region

The coefficient adjustment factor can have unity value at lower modulation index due to use of higher carrier ratio. At higher modulation index, its value can decrease up to 0.5.

The coefficients are multiplied with the base switching frequency to provide the operating switching frequency of the inverter, as shown in Fig. 6-5. It should be noted that the base

switching frequency magnitude does not depend on the sub-cycle current ripple variation and is typically adjusted based on operating current, speed and temperature of the traction drive [102].

6.5 Implementation Results

The impact of the proposed strategies on current ripple has been simulated on a three-level T-NPC inverter simulation setup for the entire modulation index and power factor range. Fig. 6-8 shows a comparison of the normalized current ripple at 0.5 and unity modulation index for SVPWM and DPWM2. It shows that it follows a profile like the theoretical results obtained in section 6.4. The current ripple does not touch zero at the middle of a sector as the operating carrier ratio is finite, unlike a very large value assumed in the theoretical analysis.

The Figs. 6-9, 6-10 show a comparative result of system operating with SVPWM and DPWM2 strategies with constant switching frequency and variable switching frequency strategy at 0.8 modulation index. The proposed approach shows that the current ripple before and after the application of switching frequency variation is within the maximum allowable limits for both

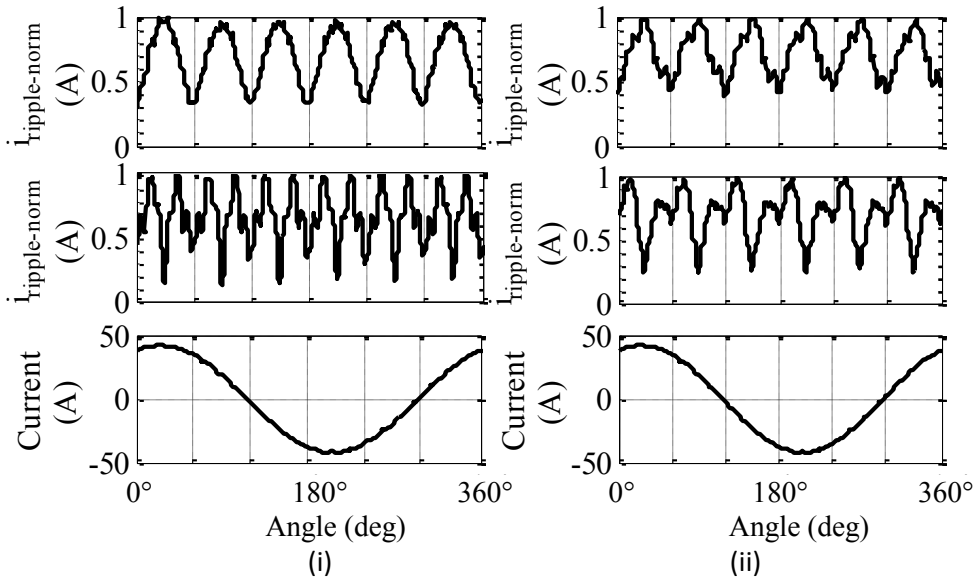


Figure 6-8. Current ripple variation comaparison of (i) SVPWM, and (ii) DPWM2

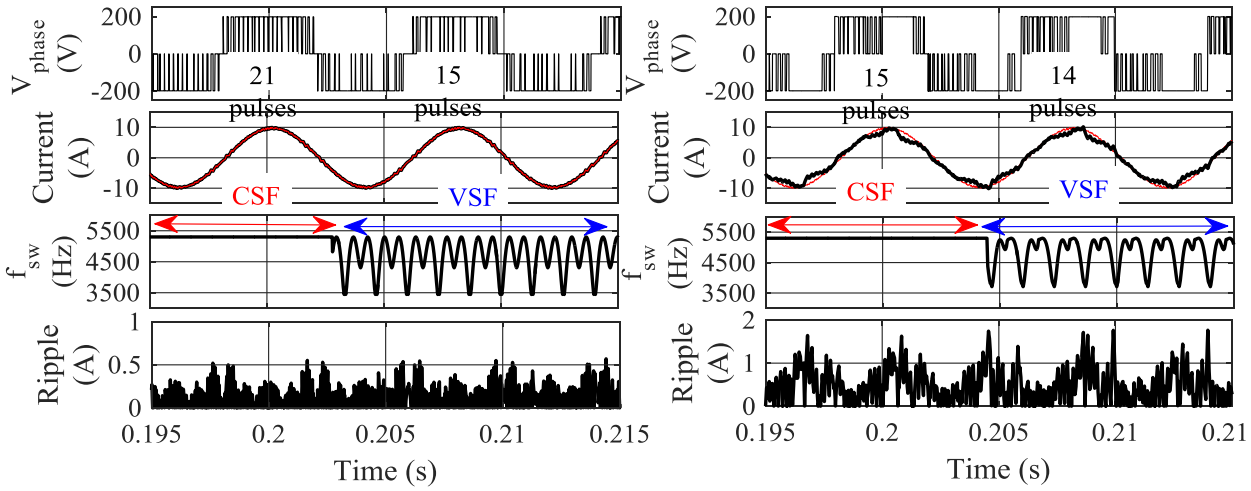


Figure 6-9. Comparison of phase A current, number of switching, current ripple and switching frequency variation for (i) SVPWM, and (ii) DPWM2 at constant and variable switching frequency

the SVPWM and DPWM2. The variation in SVPWM is higher than DPWM2 because of a higher current ripple variation in a sector for SVPWM, compared to DPWM2.

Fig. 6-9 also compares the switching instances for the PWM strategies. The application of VSFPWM has reduced 7 instances (18 %) for SVPWM and 3 instances (10.7%) for DPWM2, which shows that it can reduce switching losses.

Fig. 6-10 shows impact of SVPWM, DPWM1 and DPWM2 techniques employing variable switching frequency strategy in reducing switching losses over entire operating modulation

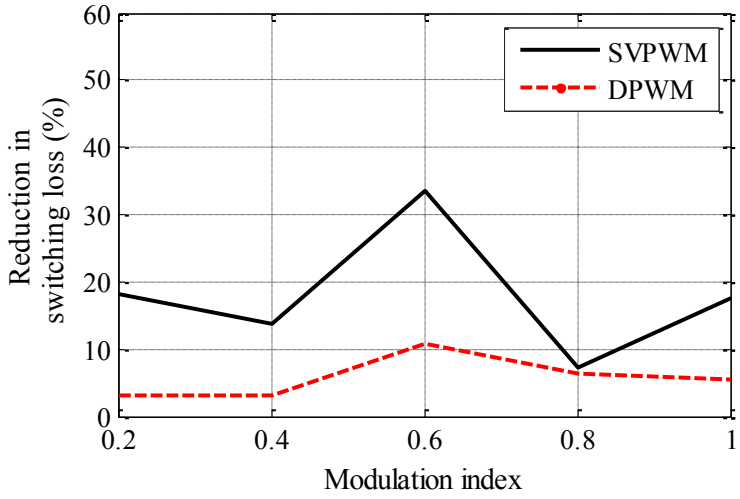


Figure 6-10. Comparison of reduction in switching losses with SVPWM, and DPWM2 operating with variable switching frequency. For DPWM1 and DPWM2 techniques, the values signify switching loss reduction due to variable switching frequency only

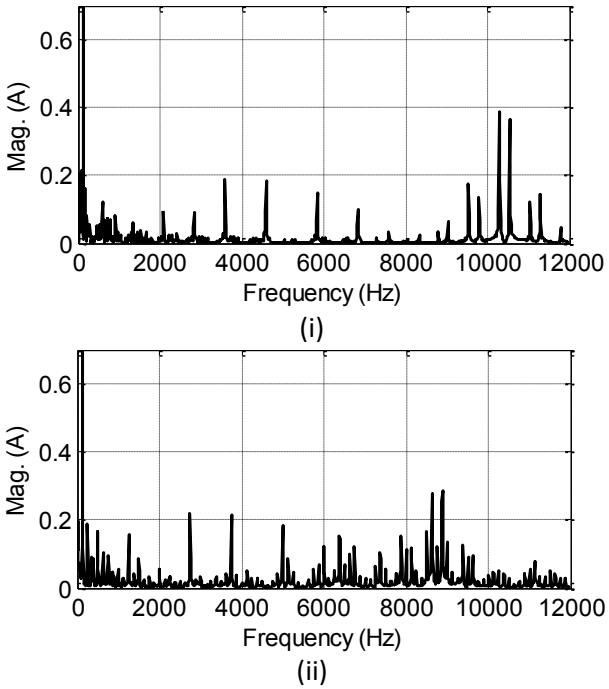


Figure 6-11. Output Current harmonic spectrum (i) without and (ii) with variable switching frequency PWM

index. With SVPWM, 10-30% switching loss reduction is achieved. With DPWM1 and DPWM2, switching loss reduction is around 5-10%. It should be noted that, with DPWM techniques, the cumulative switching loss reduction is more than VSFSVPWM technique. The values shown in Fig. 6-10 only signify the additional switching loss reduction achievable using the sub-cycle variable switching frequency strategy.

TABLE 6-3: SUMMARY OF SIMULATION RESULTS

Case	Number of pulses	THD (%)	Switching loss reduction
CSF - SVPWM	21	3.2	N/A
VSF - SVPWM	15	5.8	10%
CSF - DPWM	15	4.6	N/A
VSF - DPWM	14	6.1	10%

Fig. 6-11 shows the harmonic profile of output current with and without the use of variable switching frequency PWM strategy. It shows that with the variable switching frequency, the harmonic spectrum spreads out, in comparison to a peaky harmonic spectrum with fixed switching frequency modulation. Hence, the total harmonic distortion of the output waveform increases; with fixed switching frequency strategy, the THD is 3.2%. On the other hand, with variable switching frequency strategy, the THD is 5.8%. Hence, the proposed strategy increases output current THD. The simulation results have been summarized in Table 6-3.

6.6 Experimental Results

The proposed variable switching frequency strategy has been tested on a scaled down experimental setup, shown in Fig. 6-12. The setup consists of a three-level T-NPC inverter [122] feeding a surface mounted permanent magnet synchronous motor (SM-PMSM). The test motor is mechanically coupled to a load motor, controlled by a two-level inverter. The experimental setup parameters are provided in Table 6-4. The control is implemented on an OPAL-RT based real time prototyping tool with a 20 μs operational time step.

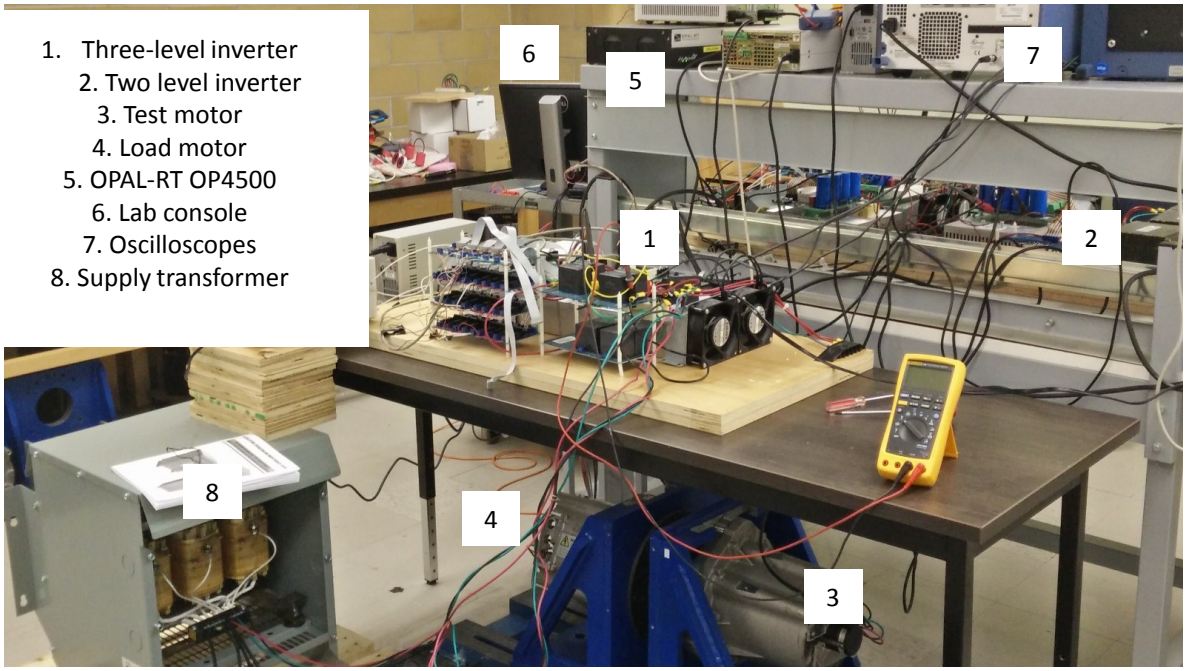


Figure 6-12. Experimental setup of three-level T-type inverter feeding a motor load

TABLE 6-4: EXPERIMENTAL SETUP PARAMETERS

Technique	Values
DC-link voltage	180 V
Motor base speed	1500 RPM
Inverter dead time	1 μs
Maximum RMS phase current	7 A
Switching frequency adjustment factor (k)	0.5
Base switching frequency	5.25 *k*Hz

Fig. 6-13 shows the sub-fundamental cycle current ripple at 0.37 and 0.95 modulation indices (600 and 1500 RPM speeds) for CSF-SVPWM. The variation is like the analytical and simulated results presented in Section III and IV.

Figs. 6-14, 6-15 show the current waveform, current ripple, switching frequency variation and the pulse counts for the SVPWM and DPWM2 techniques with CSF and VSF. The speed of the

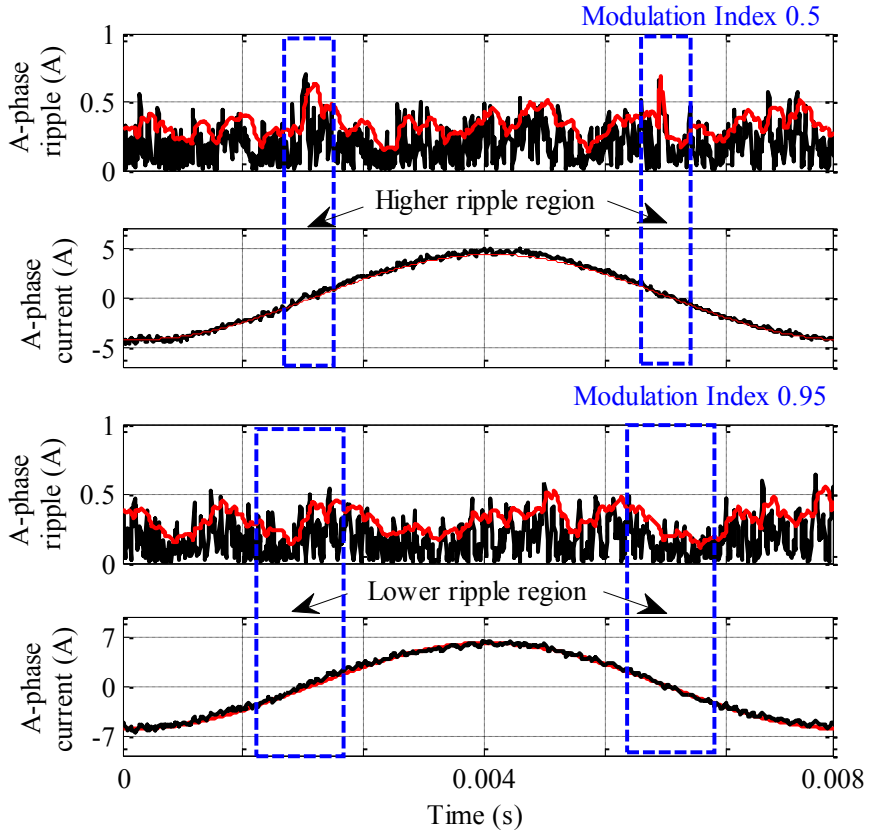


Figure 6-13. Experimental ripple variation of SVPWM at 0.5 and 0.95 modulation index

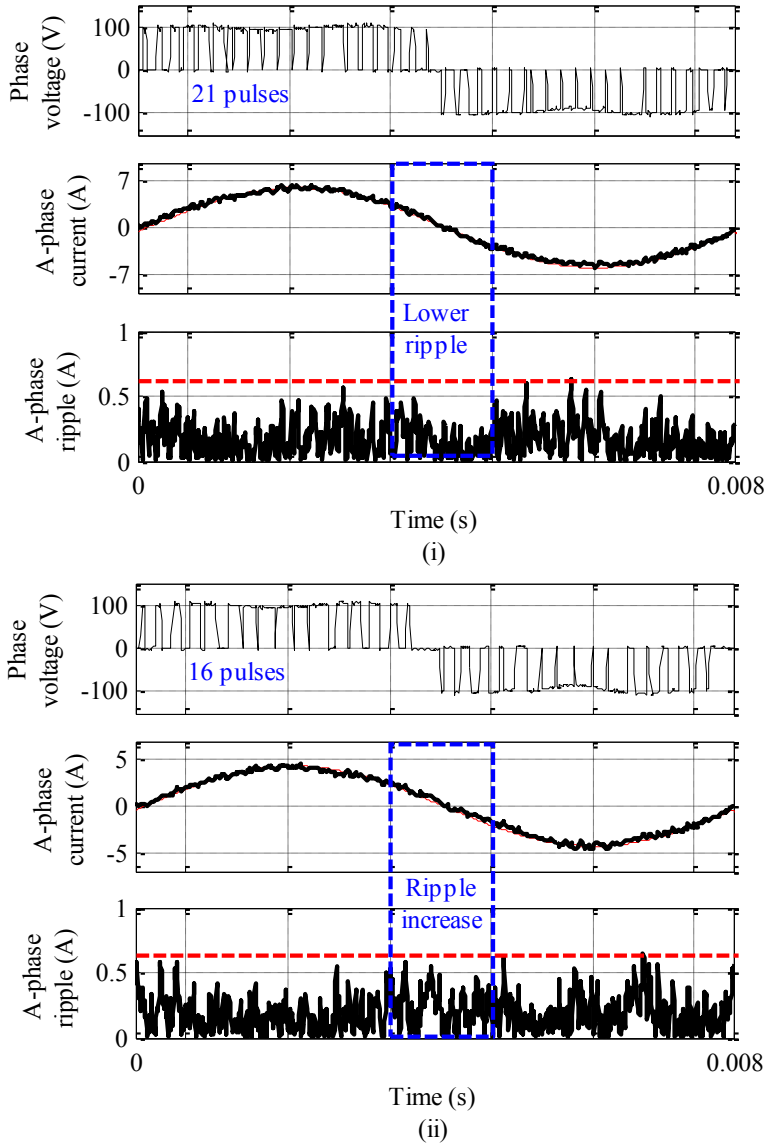


Figure 6-14. Comparison of experimental phase voltage, number of switching, current, and current ripple for SVPWM with (i) constant and (ii) variable switching frequency, Operating modulation index=0.95

motor is maintained at 1500 RPM and the inverter output RPMS current is 7 A. The following can be noted:

- For CSF-SVPWM, the current ripple within a fundamental cycle is not constant. It is higher in some parts of the fundamental cycle while lower for the rest. The switching frequency is maintained at 5.25 kHz, resulting in 21 pulses per fundamental cycle. With VSF-SVPWM, the switching frequency is varied within a fundamental cycle below 5.25 kHz base switching frequency. The resulting output current ripple shape changes, yet remains within 0.6 A, the

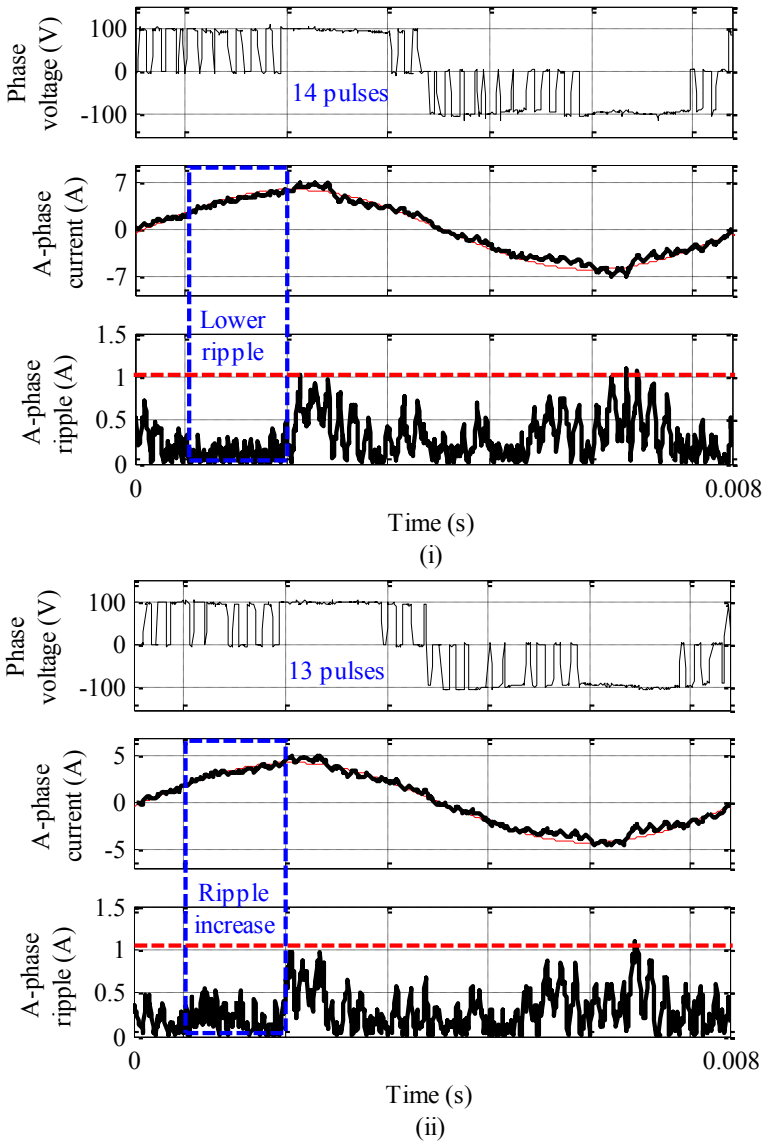


Figure 6-15. Comparison of experimental phase voltage, number of switching, current, and current ripple for DPWM with (i) constant and (ii) variable switching frequency, Operating modulation index=0.95

maximum ripple magnitude with CSFSVPWM. The number of pulses reduce to 16, a 25 % reduction.

- For CSF-DPWM2 strategy, the switching frequency remains fixed at 5.25 kHz, and the current ripple varies within a fundamental cycle with a peak amplitude of 1.1 A. There are 14 switching instances per fundamental cycle. With VSF-DPWM2 technique, the switching frequency varies below its value, although with a slightly different shape compared to the

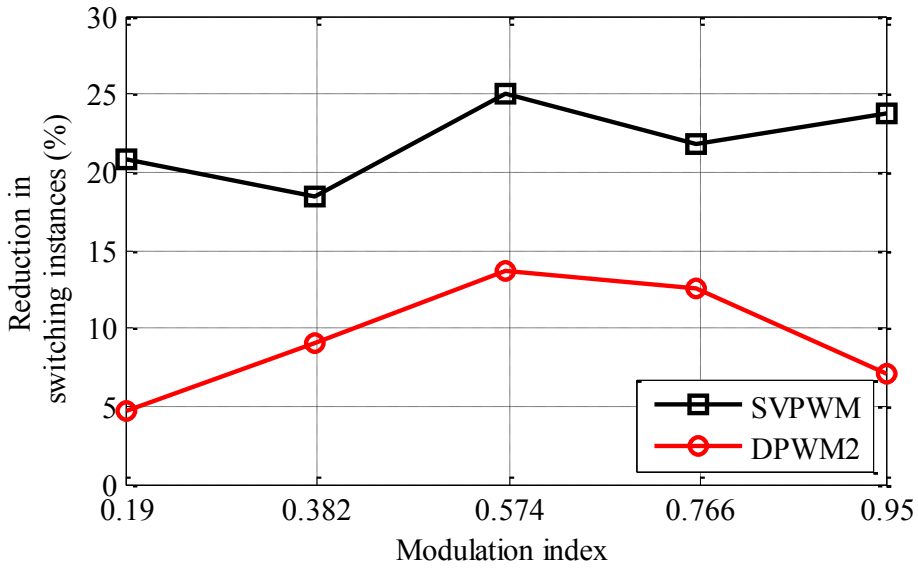


Figure 6-16. Comparison of reduction in switching losses with SVPWM, and DPWM2 operating with variable switching frequency. For DPWM1 and DPWM2 techniques, the values signify switching loss reduction due to variable switching frequency only

VSF-SVPWM strategy. The resulting current ripple is contained within 1.1 A, and the number of pulses reduce to 13, a 7.14% reduction.

Fig. 6-16 shows the impact of the proposed strategy on reducing the number of switching instances compared to fixed switching frequency techniques, while maintaining the peak-peak current ripple, at different operating speeds. Like the simulation results, with SVPWM, VSF strategy reduces number of switching instances by 20-25%. With DPWM2, switching instance

TABLE 6-5: SUMMARY OF EXPERIMENTAL RESULTS

Case	Number of pulses	THD (%)	Switching instance reduction
CSF - SVPWM	21	4%	N/A
VSF - SVPWM	16	5.8%	23.8%
CSF - DPWM	14	5.6%	N/A
VSF - DPWM	13	6.4%	7.14%

reduction is around 5-15%. Hence, the results show that the proposed VSF strategy has the capability to reduce switching losses of a three-level inverter over the entire operating modulation index range.

Table 6-5 summarizes the results obtained using experimental setup.

6.7 Discussion

As discussed earlier, the variable switching frequency strategy increases output waveform THD; and his increased current distortion would introduce additional motor or magnet heating in steady state. However, the time constant of a motor or magnet material is considerably higher than the time-constant of the inverter IGBTs. For example, the time constant of a motor is in tens of seconds, whereas the largest junction-case time constant of the switching devices is under one second. In a transient over-torque region of a traction drive, the inverter momentarily needs to be higher current, and typically, during this short time, any impact on motor or magnet is neglected. Hence, if the proposed variable switching frequency strategy is utilized in the transient over-torque regions of a traction drive the result would be twofold – (i) it would enable the inverter incurring lower switching losses than the conventional fixed switching frequency techniques at higher output current, and (ii) there would not be any appreciable rise in the motor/magnet temperature due to its higher time constant and usage of the strategy for a shorter time-period. Hence, the proposed strategy is appropriate to use at the transient over-current region of a two-level inverter fed traction drive.

Moreover, the variable switching frequency strategy uses the correction factor ‘k’ to take care of the variation in carrier ratio. As carrier ratio decreases at higher modulation indices, ‘k’ value needs to be reduced from unity, which reduces the variation in switching frequency. However, as at higher modulation indices, the theoretical switching frequency variation is around 80%; a lower value of ‘k’ will not impede a reduction in switching instances and switching losses.

6.8 Conclusion

The chapter provides an in-depth analysis of sub-cycle current ripple variation of a three-level inverter over operating modulation index and position of voltage vector. The analysis

considers three-level space-vector based continuous and discontinuous PWM sequences and the entire operating range of a three-level inverter, including the over-modulation region. The analysis shows that within a fundamental cycle, the current ripple variation increases at higher modulation indices due to use of more number of voltage vectors. When the voltage vector is nearer to the space-vectors to be used, up to 60% variation in current ripple is observed. Based on the analysis, the chapter also presents a methodology to vary the operating switching frequency within a fundamental cycle. Unlike conventional strategies, the proposed technique utilizes pre-computed switching frequency variation factors without relying on prediction or optimization techniques since the peak-peak current ripple follows a definite trajectory within a fundamental cycle. The sub-fundamental cycle switching frequency variation strategy maintains the current ripple within a predefined band, and can reduce switching losses up to 30% and 10% with continuous SVPWM and DPWM switching sequences, respectively.

7 Summary & Conclusions

Electric vehicles (EVs) require traction drive systems to interface three-phase electrical motors and DC voltage batteries. These traction drive systems consist of power electronic inverters that convert the DC voltage of batteries to three-phase AC that can be used to operate electric motors. Both, the inverters and the motors can be implemented in various ways.

The main objective of the thesis was to develop modulation and control strategies for dual two-level and three-level inverter topologies with special focus on DC-link capacitor current and voltage ripple, as well as the efficiency and output waveform distortion of the three-level inverters. The proposed strategies were implemented along with an experimental prototype that has been built, and tested.

7.1 Thesis Summary

This thesis explores the various conventional inverter implementations for automotive applications, and modulation methods to improve their performances in Chapter 1. After a review of the basic inverter topologies, further considerations have been concentrated on dual two-level and three-level inverter topologies. Amongst different three-level inverter topologies, the T-type three-level inverter topology has been chosen for further approach as it incurs lower losses than the other three-level topologies. As discussed in Chapter 1, the inverter input DC-link ripple, inverter switching losses and loss distribution are the common concerns associated with automotive inverters. Hence, the thesis focuses on modulation strategies of dual two-level and dual-three-level T-NPC inverters, and proposes several modulation strategies in the later chapters to address the issues.

In Chapter 2, the dual two-level inverter topology is investigated to reduce the DC-link capacitor RMS current ripple. Firstly, a single two-level inverter is simulated to investigate the harmonic spectra of the DC-link capacitor current, and the dominant harmonics are identified for the entire modulation index. Secondly, impact of interleaving the switching pulses of two such inverters on the dominant harmonics is investigated, and the optimum interleaving angles are identified. The strategy is implemented in MATLAB/Simulink, and tested on an experimental

setup containing 2 two-level inverters connected to the same DC-link and feeding two sets of three-phase loads.

The dual three-level T-type inverter topology is investigated in chapter 3. The topology is considered supplying power to a dual three-phase motor which has two separate three-phase winding sets without appreciable mutual inductance between them. Hence, the system is modelled as two three-level T-type inverter feeding two separate three-phase motors. The DC-link capacitor voltage balancing issue is studied, and an interleaved modulation strategy is proposed to reduce it. The method is implemented on a simulation system where the inverter is simulated in MATLAB/Simulink, and the motors are simulated in Infolytica/MotorSolve environment. The strategies are tested on an experimental setup which was built along with the dual motor provided by TM4 Inc., the industrial partner of the project.

In Chapter 4-5, several discontinuous modulation strategies are proposed for the three-level T-type inverter topology. More specifically, the clamping possibilities at modulation indices lower than 0.5 are investigated. In chapter 4, the distribution of losses and device junction temperatures amongst the switches of a T-type topology for the conventional continuous and discontinuous modulation strategies are examined. Based on the analysis, a modulation strategy is proposed to improve the distribution profile. In chapter 5, impact of conventional discontinuous modulation strategies on switching losses at lower power factors is researched. Several discontinuous PWM sequences and a generalized modulation strategy is proposed. Initially, the losses are analyzed based on the analytical equations and average modulation voltage waveforms. Furthermore, the T-type inverter is simulated in MATLAB/Simulink, and the losses and the junction temperatures are obtained using PSIM tool. Finally, the strategies are tested on an experimental set-up containing a three-level T-type inverter feeding a passive three-phase load. Since the experimental setup operates on a small-scale power level, the loss calculation, and separation of losses between conduction and switching losses proved difficult. Hence, impact of the strategies on inverter losses is measured in terms of the number of switching instances, along with the number of switchings around the current peak.

As the inverter switching devices are switched discretely, the output voltage and current waveforms are not purely sinusoidal, and exhibits distortion. In Chapter 6, the current ripple

profile of a three-level inverter within a fundamental cycle is investigated for the entire modulation index range. To do this, the cumulative current ripple on the current phasor is considered, and the conventional continuous and discontinuous PWM strategies are considered. The current ripple profile is saved as a look-up table, and used to reduce the operating switching frequency within a fundamental cycle. The strategies are implemented on a MATLAB/Simulink environment, and experimentally validated on the three-level T-type set-up. Like previous chapters, as the experimental setup is operating on a small-scale power level, the loss calculation, and separation of losses between conduction and switching losses proved difficult. Hence, impact of the strategies on inverter losses is only measured in terms of the number of switching instances.

7.2 Conclusions

The principal conclusions and original contributions of this thesis are listed here (in order of appearance in the thesis):

i. The interleaved modulation strategy for the dual two-level inverter topology reduces input DC-link capacitor current ripple around 50-60%. It was shown that for different operating points, only specific interleaving angles lead to a substantial reduction in the capacitor ripple currents. For example, with continuous SVPWM strategy, at lower modulation index, the interleaving angle is 90°, whereas at higher modulation index, 180° interleaving angle must be chosen. The discontinuous SVPWM strategy uses 180° interleaving angle over the entire modulation index.

ii. The dual three-level T-NPC inverter fed dual PMSM and its interleaved PWM control decouple pulse-width modulation strategies of the inverters from DC-link capacitor voltage balancing and maintains balanced DC-link capacitor voltages during steady-state as well as in transient conditions. In addition, due to the interleaved control strategy, the currents through the DC-link capacitors are reduced by 90-97%. The strategy also provides the dual three-level inverter topology the ability to use sophisticated modulation strategies without considering capacitor voltage balancing issues.

iii. The proposed DPWMPN discontinuous modulation strategy for the three-level T-NPC inverter topology can relocate the phase currents to the outer switches, from the inner switches during clamping. Hence, with the proposed sequences, the distribution of losses and junction temperature is more equal amongst the switching devices. In consequence, the inverter – 1) can increase its current throughput by around 30% or 2) can utilize a 30-40% higher switching frequency to improve output waveform quality, while incurring a similar increase of device junction temperatures as conventional PWM sequences.

iv. The proposed generalized discontinuous PWM strategy can create PWM sequences such that the no-switching durations of the created sequence are aligned with the respective current peaks at all power factors. Analytical and implementation results demonstrate that the strategy ensures no switching instances around current peaks and consequently reduces inverter switching losses up to 50% at all operating power factors.

v. The sub-fundamental current ripple analysis shows that within a fundamental cycle, when the reference voltage vector approaches one of the space-vectors of the switching hexagon, up to 60% variation in current ripple is observed. The sub-fundamental cycle switching frequency variation strategy, based on the current ripple profile, maintains the current ripple within a predefined band, and can reduce switching losses up to 20% for a three-level inverter.

7.3 Recommendations for Further Work

Some aspects of three-level and dual inverter topologies for EV traction drive applications have been considered in this thesis work. Nevertheless, the work can be extended to the further research studies. Some of them are listed here:

i. Investigation of different dual three-phase motor topologies, such as open-ended motors and topologies with three-phase winding sets having 30° phase difference between them. These topologies would impact the inverter DC-link current ripple, inverter losses and loss distribution profiles differently.

ii. Research on modulation strategies which further reduces conduction losses of the inner switching devices of a three-level inverter over the entire modulation index range. It can

be performed by using the inner devices only during switching from devices connected to positive DC-link to negative DC-link, like traditional soft-switching techniques.

iii. Implementation of a predictive current control technique of three-level and dual inverter topologies which would feature the advantages associated with the modulation strategies introduced in this thesis, namely:
    a. Interleaving capability
    b. Improved loss distribution.

    As this strategy would maintain the current ripple within a limit, a comparison with the variable switching frequency strategy can also be investigated.

iv. Several fault tolerant strategies of the dual three-level topologies can be studied. The fault tolerant locations can be different, such as:
    a. Fault in the motor windings, which would require a change in the inverter control technique to provide limp-home capability.
    b. Fault in the switching devices, which would require a curtailment in the operating modulation index range, and associated changes in inverter modulation strategies.
    c. Fault in the current sensors, which could be taken care of if a suitable current reconstruction technique is designed based on the measured DC-link current.

v. A variable pulse strategy for the three-level inverters can be designed which will increase the pulse count of each legs at an appropriate position of a fundamental cycle to reduce the current ripple, and improve output waveform quality. This would also utilize the current ripple profile presented in this thesis.

vi. The three-level inverter discontinuous modulation strategies have been implemented using space vector technique. The techniques can be implemented using the sine-PWM techniques which would require extensive analysis of zero sequence injection techniques.

Appendix A: Definitions & Software Implementations

This appendix defines some of the terms that are used in the thesis and explains the MATLAB/Simulink implementations of different variants of the Space-Vector PWM strategy for three-level inverters. The definitions are not a contribution of the author. The references for the definitions are provided.

A.1. Modulation Index

As discussed in [4], in an inverter, each of semiconductor devices are controlled using switching pulses, generated using different variants of pulse-width-modulation (PWM) strategy.

The sinusoidal PWM (SPWM) strategy is the simplest PWM strategy, and it is often used to modulate the semiconductor devices. In this strategy, a low-frequency sinusoidal signal is compared to a high-frequency triangular signal train. The sinusoidal signal has a fundamental frequency equal to the desired fundamental frequency of the output waveform and a peak magnitude lower than or equal to unity. The triangular waveform has a frequency commonly known as switching frequency and has a unity peak magnitude. In the SPWM strategy, if the instantaneous magnitude of the sinusoidal signal is greater than the triangular signal, the upper switch of one-leg of a two-level inverter gets ON. Thus, depending on the peak magnitude of the sine signal, the duty cycle of the switches can be controlled. In the SPWM strategy, the modulation index (m) is defined as

$$\mathrm{m} = \frac{\text{peak amplitude of the controllable sinusoidal signal}}{\text{peak amplitude of the triangular signal}} \tag{7.1}$$

As discussed in [4], with this PWM strategy, the maximum attainable peak-peak output line voltage is

$$\mathrm{V_{l-lpeak\_SPWM}} = \frac{\sqrt{3}}{2}\mathrm{V_{DC}} \tag{7.2}$$

Thus, in the SPWM strategy, the modulation index can also be defined as

$$m = \frac{\text{peak amplitude of fundamental component of the line} - \text{line voltage}}{\frac{\sqrt{3}}{2}V_{DC}} \quad (7.3)$$

As discussed in [10] - [12], the maximum magnitude of output voltage can be increased if the above operation is done using a signal which is formed as follows:

$$\text{Controllable sinusoidal signal} = 1.15 * m * \left(\sin\omega t + \frac{1}{6}\sin 3\omega t\right) \quad (7.4)$$

Due to the injection of third harmonic component, the maximum attainable peak-peak output line voltage becomes

$$V_{l-lpeak\_THI\_SPWM} = V_{DC} \quad (7.5)$$

In this thesis, space-vector PWM strategy is used for both two-level and three-level inverters. With this SVPWM strategy, the maximum attainable peak-peak line voltage is equal to the Third-harmonic injected SPWM (THI-SPWM) technique [10]- [12]. Moreover, the radius of the largest inscribed circle, touching the arms of the space-vector hexagon defines the maximum modulation index.

Thus, with the SVPWM and THISPWM techniques, the modulation index cannot be defined anymore using the equation 7.1, and can only be defined as

$$m = \frac{\text{peak amplitude of fundamental component of the line} - \text{line voltage}}{V_{DC}} \quad (7.6)$$

A.2. Continuous Modulation

In continuous modulation strategy, each semiconductor device of an inverter is subjected to switching over a complete fundamental cycle. Examples of such modulation strategies are:

i. Sinusoidal PWM (SPWM) [4]
ii. Third-harmonic injected sine PWM (THI-SPWM) [10]- [12]
iii. Continuous SVPWM (CSVPWM) [10]- [12]

A.3. Discontinuous Modulation

In discontinuous modulation strategy, one-phase of an inverter is subjected to switching over two-third of a complete fundamental cycle. For the rest of the fundamental cycle, the devices are not switched, and remains connected to different points of the DC-link. Examples of such modulation strategies are:

iv. Different variants of Third-harmonic injected sine PWM (THI-SPWM) [10]- [12]

v. Discontinuous SVPWM (DSVPWM) [10]- [12]

A.4. Software Implementation of Three-Level SVPWM

Referring to Fig. 1-5 (ii), in a three-level space-vector hexagon, based on magnitude, the voltage vectors can be divided into four groups: Zero vector (Vo), Small vector (VS), Medium vector (VM), and Large vectors (VL). All zero vectors have zero magnitude, small vectors have a magnitude of Vdc/3, medium vectors have magnitude of Vdc/3 and large vectors have magnitude of 2Vdc/3. Each small vector has two switching states, one containing P and other containing N, and therefore can be further classified into a P-type or N-type vector. Taking all the three phases in account, the inverter has a total of 27 possible combinations of switching states. Fig. 1-5 (ii) shows the space vector diagram of total 27 switching states corresponding to 19 voltage vectors for three-level inverter.

Initially, the space-vector modulation for 3-level NPC has been discussed without any associated neutral point balancing technique for understanding of the system. The input to a space-vector modulation block is the reference voltage (V_{ref}) and the phase angle θ. From the phase angle, the sector at which the reference vector is and the angle it makes with the shifted reference line can be determined as:

$$S_i = int\left(\frac{\theta}{60}\right) + 1; \quad \theta_i = rem\left(\frac{\theta}{60}\right) \tag{7.7}$$

Now, the reference vector can be divided along the two sides of the triangle as:

$$m_1 = \sqrt{3}m_a\left(\cos\theta - \frac{\sin\theta}{\sqrt{3}}\right); m_2 = 2\sqrt{3}m_a\left(\frac{\sin\theta}{\sqrt{3}}\right); \; where \; m_a = \sqrt{3}\frac{V_{ref}}{V_d} \tag{7.8}$$

Now, depending on the values of m_1 and m_2, the region of the sector can be selected and V_{ref} can then be obtained by the volt-second balance of the surrounded three vectors. The dwelling times of these three vectors are tabulated in Table AP_A-1. This is also shown in Fig. Ap_A-1.

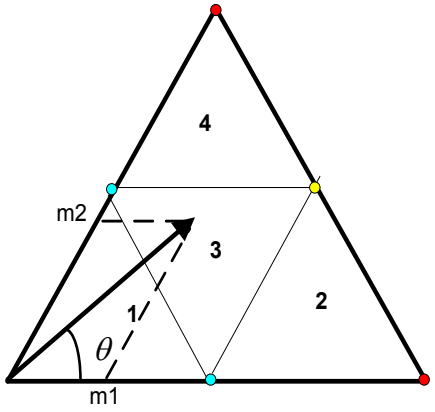


Figure Ap_A-1: A single sector with four region

TABLE AP_A-1 : DWELLING TIMES OF DIFFERENT SPACE VECTORS

Region	Dwelling Times	Criteria for region selection
I	$T_{s1} = T_s\left[2m_a \sin\left(\frac{\pi}{3} - \theta\right)\right]$ $T_o = T_s\left[1 - 2m_a \sin\left(\frac{\pi}{3} + \theta\right)\right]$ $T_{s2} = T_s[2m_a \sin(\theta)]$	$m_1 \leq 1, m_2 \leq 1, m_1 + m_2 \leq 1$
II	$T_{s1} = T_s\left[2 - 2m_a \sin\left(\frac{\pi}{3} + \theta\right)\right]$ $T_m = T_s[2m_a \sin(\theta)]$ $T_{L1} = T_s\left[2m_a \sin\left(\frac{\pi}{3} - \theta\right) - 1\right]$	$m_1 > 1$
III	$T_{s1} = T_s[1 - 2m_a \sin(\theta)]$ $T_m = T_s\left[2m_a \sin\left(\frac{\pi}{3} + \theta\right) - 1\right]$ $T_{s2} = T_s\left[1 - 2m_a \sin\left(\frac{\pi}{3} - \theta\right)\right]$	$m_1 \leq 1, m_2 \leq 1, m_1 + m_2 > 1$
IV	$T_{L2} = T_s[2m_a \sin(\theta) - 1]$ $T_m = T_s\left[2m_a \sin\left(\frac{\pi}{3} - \theta\right)\right]$ $T_{s2} = T_s\left[2 - 2m_a \sin\left(\frac{\pi}{3} + \theta\right)\right]$	$m_2 > 1$

The region at which the vector is can be found in Table AP_A-1. To select switching sequences, seven segment switching are used and care is taken over of one switching transition i.e. only one device gets on or off. This is most widely used conventional 7-segment SVM [15, 22]. Seven-segment SVPWM divides the dwell time of only one small vector in P-type and N-type out of two small sectors available in region 1 and 3.

Using earlier discussion and equations, three-level Space Vector Modulation has been implemented. As depicted in Fig. Ap_A-2, the reference voltages have been used to (Block 1) calculate the reference voltage needed for SVM, the sector at which the vector is and the angle the reference voltage vector is making with the lagging long-type vector in a sector. The calculated reference voltage and angle have been used to calculate (Block 2) the sub-sector in which the reference voltage is. In this block, the reference voltage is normalized using the proper DC-link voltage. This information is then used to calculate the dwelling times in the sub-sectors over a switching period. The dwelling times are then rotated with the help of information about the sector in which the vector is and the angle it makes.

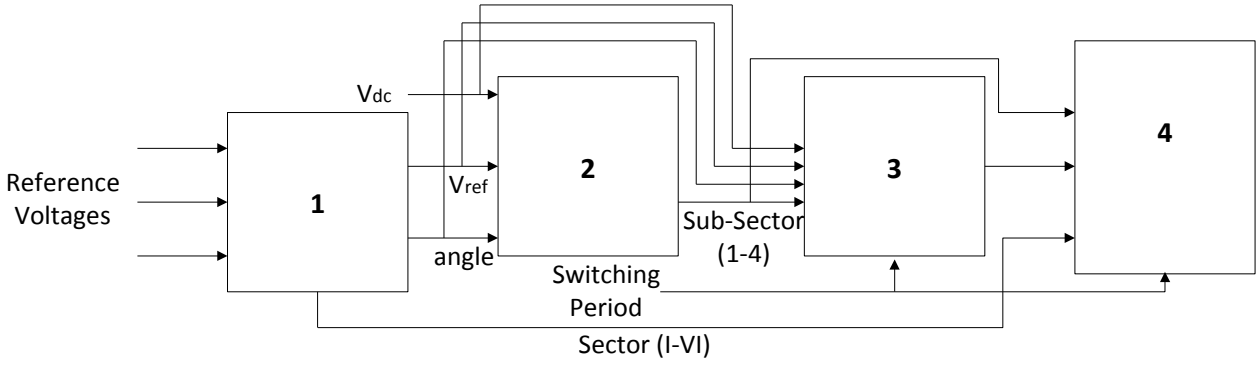


Figure Ap_A-2: Three-level SVM implementation

A.5. DC-link Capacitor Voltage Deviation and DC-link Current Ripple in Three-level Inverters

As seen in Fig. Ap_A-3 , the source DC-link current gets divided into three sets of current which are current flowing through positive DC rail, negative DC rail and neutral point connection. In doing so, the current flows through two capacitors. This has been analyzed as follows:

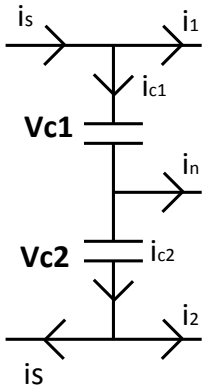


Figure Ap_A-3: Three-level dc-link capacitor current and voltages

The current flowing through two capacitors ($i_{c1}$and i_{c2}) can be written as

$$\begin{bmatrix} i_{c1} \\ i_{c2} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_2 \\ i_n \end{bmatrix} \tag{7.9}$$

Now, the voltages of those two capacitors can be written as

$$\begin{bmatrix} V_{c1} \\ V_{c2} \end{bmatrix} = \frac{1}{C} \int \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_2 \\ i_n \end{bmatrix} . dt \tag{7.10}$$

$$\Delta V_c = V_{c1} - V_{c2} = \frac{1}{C} \int i_n \, dt \tag{7.11}$$

So, load current from middle of the dc-link controls the neutral point potential difference. So, over a time-period, average neutral current must be zero. Using the dual three-level inverter topology, the neutral point current consists of two currents due to two three-level inverters. As those two currents (i_{n1} & i_{n2}) are 180° phase-shifted, the resultant neutral-point current is controlled to zero, resulting in negligible capacitor voltage deviation.

As shown in [106], the capacitor RMS current of a single three-level inverter can be written as (for modulation indices lower and higher than 0.5)

$$i_{Cap\_RMS\_m\_less\_0.5} = I_m \sqrt{-m(0.75m \cos^2 \varphi - 0.64 \cos^2 \varphi - 0.16} \tag{7.12}$$

$$i_{Cap\_RMS\_m\_more\_0.5}$$

$$= \frac{I_m}{m}\left(m^4\left(\sin^{-1}\left(\frac{0.5}{m}\right)^2 * (-0.227 + 0.227\cos^2\varphi) + \sin^{-1}\left(\frac{0.5}{m}\right)\right.\right.$$

$$\left.* (-0.42\sin 2\varphi) - 0.75\cos^2\varphi\right) + m^3\left((0.159 - 0.275\sin 2\varphi) + 0.64\cos^2\varphi\right)$$

$$+ m^2\left(\sqrt{4m^2-1}\right.$$

$$* \left(0.113 * \cos^2\varphi * \sin^{-1}\left(\frac{0.5}{m}\right) - 0.113 * \sin^{-1}\left(\frac{0.5}{m}\right) + 0.034\sin 2\varphi\right.$$

$$\left.\left.+ \sin^{-1}\left(\frac{0.5}{m}\right) * (-0.2\cos^2\varphi + 0.2) + 0.056\cos^2\varphi - 0.056 + 0.537\sin 2\varphi\right)\right)$$

$$+ \sqrt{4m^2-1} * (-0.04 * \cos^2\varphi + 0.049 - 0.034\sin 2\varphi) + 0.028 * \cos^2\varphi$$

$$\left.- 0.059\sin 2\varphi - 0.028\right)^{0.5} \quad (7.13)$$

In [106], it has been shown that the capacitor current can reach 40-50% of the load current.

A.6. Analytical Conduction and Switching Loss Calculation

The inverter switching and conduction loss calculation procedure of a three-level inverter for the proposed GDPWMO strategy involving DPWM2O, DPWM1O and DPWM0O PWM templates (for power factor angle (ϕ) between -30° and 30°; and for clamping angle (α) between -30° and 30°) are discussed here. Similar procedure is implemented for the proposed DPWMPN strategy with the help of modulation voltage and current waveforms of Fig. 4-5.

In Fig. Ap_A-4(i)-(iii) DPWM2O template with current having power factor angles 0°, 30° and -30° are shown. In Fig. Ap_A-4 (i)-(iii), in R1 region, no switching occurs. In Fig. Ap_A-4 (i), in R2 and R4 region, T1, Tn1 and Dn2 conduct; however, only T1 and Dn2 have switching losses. In the R3 region, as the modulation voltage is negative, commutations occur in Tn1, Dn2 and D2. In

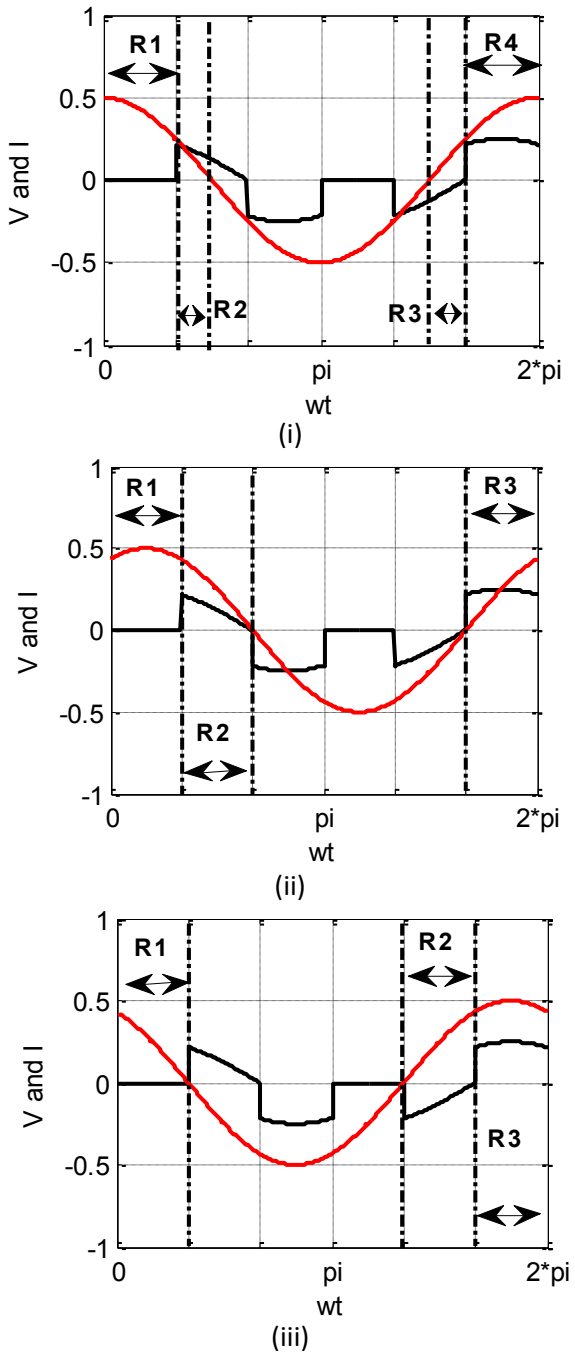


Figure Ap_A-4: Modulation voltage waveform and current waveform for DPWM2O with (i) 0º, (ii) 30º and (iii) -30º power factor angle

Fig. Ap_A-4 (ii), in R2 and R3 regions, T1 and Dn 2 have switching losses. In Fig. Ap_A-4 (iii), in R3 region, T1 and Dn2 have switchings, and in R2 region, Tn1, Dn2 and D2 have switchings. Hence, due to switching at different duration creates asymmetrical switching for different switching

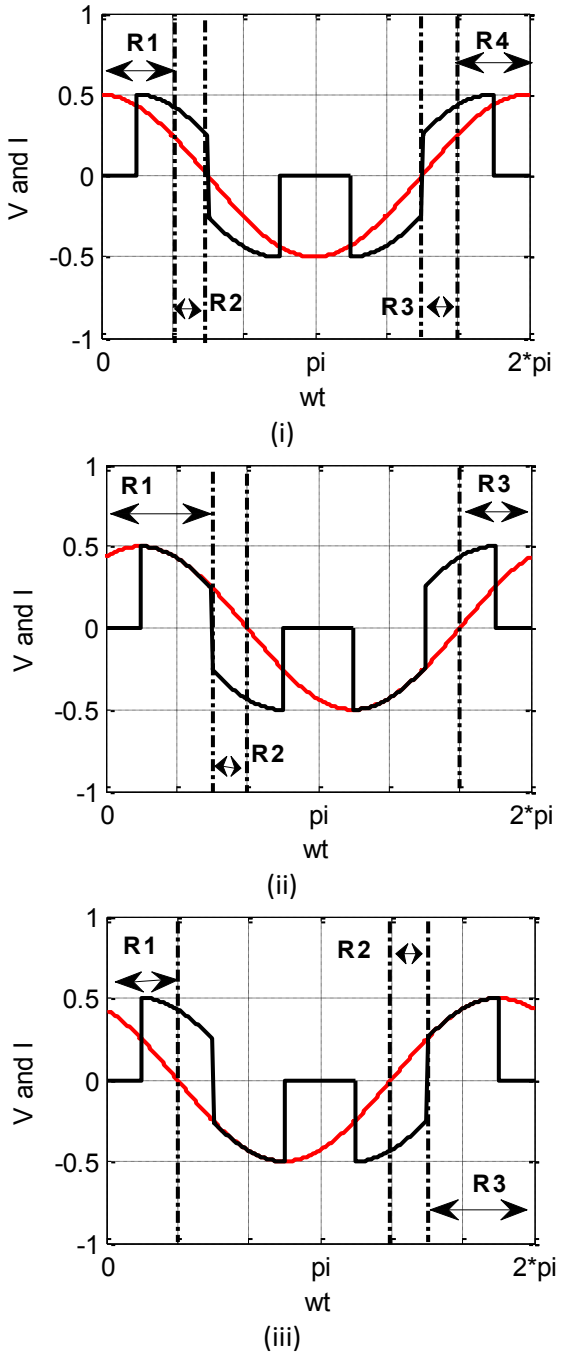


Figure Ap_A-5: Modulation voltage waveform and current waveform for DPWM1O with (i) 0º, (ii) 30º and (iii) -30º power factor angle

devices. Similar analysis can be done for DPWM1O (Fig. Ap_A-4 (iv-vi)) and DPWM0O (Fig. Ap_A-4 (vii-ix)) templates. From the above analysis, Table Ap_A-2 is created which has the angle durations in which different switches commutate. Only the positive half cycle is considered. From

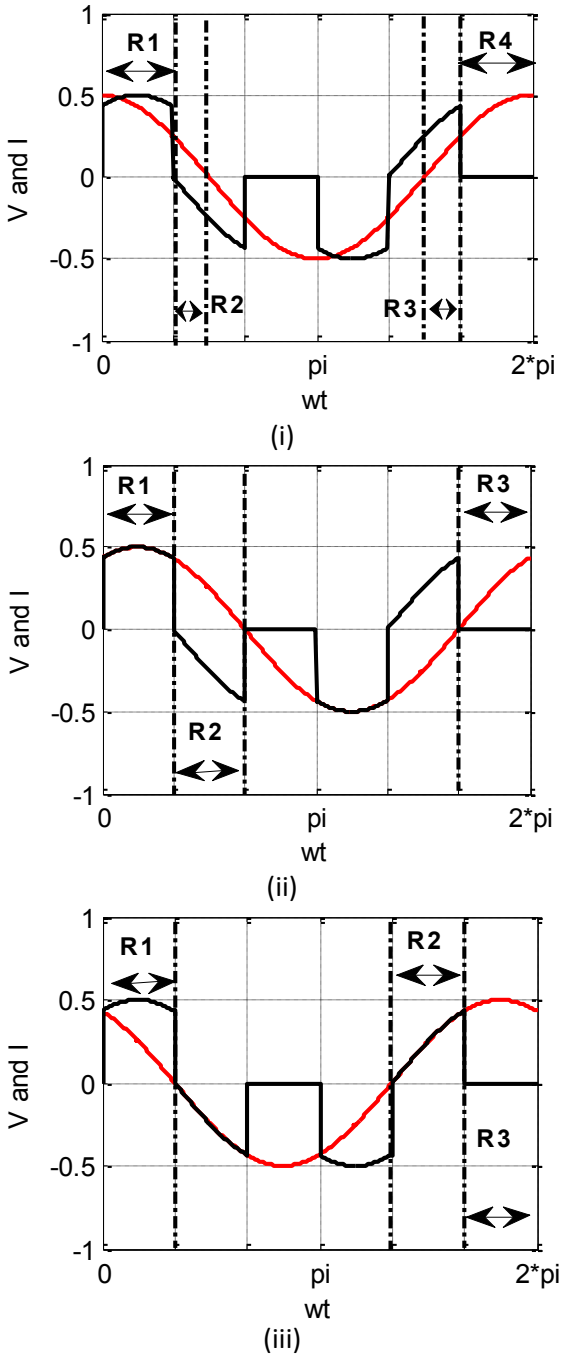


Figure Ap_A-6: Modulation voltage waveform and current waveform for DPWM0O with (i) 0º, (ii) 30º and (iii) -30º power factor angle,

the information of Table Ap_A-2, in Table Ap_A-3, generalized angle durations are listed which are functions of the clamping angle (α), and the power factor angle (ϕ).

TABLE AP_A-2 : DEVICE SWITCHING DURATIONS FOR DPWM0O-DPWM2O STRATEGIES

Device witching	DPWM2O with unity pf	DPWM2O with 30 degree pf angle	DPWM2O with -30 degree pf angle	DPWM1O with unity pf	DPWM1O with 30 degree pf angle	DPWM1O with -30 degree pf angle	DPWM0O with unity pf	DPWM0O with 30 degree pf angle	DPWM0(with -30 degree pf angle
T1	60°→90°, (-60°) →0°	(-30°) →30°	(-30°) →30°	30°→90°, (-90°) → (-30°)	0°→60°, (-90°) → (-60°)	60°→90°, (-60°) →0°	0°→60°, (-90°) → (-60°)	(-30°) →30°	30°→90° (-90°) → (-30°)
Tn1	(-90°) → (-60°)	-	(-90°) → (-30°)	-	60°→90°	(-90°) → (-60°)	60°→90°	30°→90°	-
Dn2	60°→90°, (-90°) →0°	30°→90°, (-90°) → (-30°)	(-90°) →30°	30°→90°, (-90°) → (-30°)	0°→90°, (-90°) → (-60°)	60°→90°, (-90°) →0°	0°→90°, (-90°) → (-60°)	(-30°) →90°	30°→90° (-90°) → (-30°)
D2	(-90°) → (-60°)	-	(-90°) → (-30°)	-	60°→90°	(-90°) → (-60°)	60°→90°	30°→90°	-

TABLE AP_A-3 : DEVICE SWITCHING DURATIONS FOR GDPWMO STRATEGY

Device switching	T1	Dn2	Tn1 & D2
Generalized Switching timings	$\pi/6 - \varphi + \alpha$ → $\left(\pi/2 - \frac{\lvert\alpha-\varphi\rvert}{2} + \frac{\alpha-\varphi}{2}\right)$ $\left(-\pi/2 + \frac{\lvert\alpha-\varphi\rvert}{2} + \frac{\alpha-\varphi}{2}\right)$ → $-\pi/6 - \varphi + \alpha$	$\pi/6 - \varphi + \alpha$ → $\left(\pi/2 - \frac{\lvert\alpha-\varphi\rvert}{2} + \frac{\alpha-\varphi}{2}\right)$ $\left(-\pi/2 - \frac{\lvert\alpha-\varphi\rvert}{2} + \frac{\alpha-\varphi}{2}\right)$ → $(-\pi/6 - \varphi + \alpha)$	$\left(-\pi/2 - \frac{\lvert\alpha-\varphi\rvert}{2} + \frac{\alpha-\varphi}{2}\right)$ → $\left(-\pi/2 + \frac{\lvert\alpha-\varphi\rvert}{2} + \frac{\alpha-\varphi}{2}\right)$

The switching loss of a device is found as:

$$P_{sw} = \sum k \int_{\theta 1}^{\theta 2} |I|(\theta)\, d\theta \tag{7.14}$$

Where θ1 and θ2 signifies the angle durations during the switch conducts and commutates.

The conduction loss of a device is found as:

$$P_{cond} = \sum k1 \int_{\theta 1'}^{\theta 2'} |I|^2(\theta)\, d\theta + \sum k2 \int_{\theta 1'}^{\theta 2'} |I|(\theta)\, d\theta \quad (7.15)$$

Where θ1' and θ2' signifies the angle durations during the switch conducts; K1 is the device on-state resistance and k2 is the device on-state voltage drop.

The summation signifies integrations for different angle durations, as shown in Table Ap_A-3. Using the information of Table Ap_A-3, the closed form equations of Table 5-3 and the analytical switching and conduction losses in Fig. 4-6, Fig. 4-7 and Fig. 5-7 are found. As the comparisons were only made between two PWM templates, the device characteristics remain same and the only the modulating functions change. It can be seen that the equations (i.e. resulting losses) are dependent on power factor angle φ and clamping angle α. In addition, the modulation functions also change based on operating modulation index, as discussed in [105], [132]. Hence, the losses also change with the operating modulation index.

A.7. Simulation Loss and Junction Temperature Estimation

As indicated in Chapter 3-6, the inverter loss and junction temperature is calculated in PSIM and MATLAB environment. The following discussion provides a brief overview of the procedure.

PSIM provides the most updated database of various power switches on the market. Besides, the SimCoupler module in PSIM provides the link between PSIM and MATLAB/Simulink for co-simulation [118]. Unfortunately, PSIM's existing thermal Module does not feature the three-level TNPC module used in this investigation (Infineon's 1 leg 3L F3L400R12PT4_B26 module), and only the two-level 6-pack exists in PSIM device manager. The three-level topology was assembled and modeled with discrete components. With the PSIM Thermal Module, users can

easily add devices of any manufacturers into a database. The device characteristic curves were imported from the datasheet of the device [119]. Inside PSIM, the device losses are calculated based on standard loss equation, as seen in [151]. The characteristics were directly extrapolated from the manufacturer's datasheets. Of course, the loss calculation is only an approximation, and the accuracy of the results depends on the accuracy of the device data as well as the proper scaling of the results from the device test condition to the actual circuit operating conditions. The loss calculation formulas are shown below:

$$Diode\ conduction\ losses = v_D * I_{D_{av}} + r_D . {I_{D_{RMS}}}^2 \tag{7.16}$$

$$IGBT\ conduction\ losses = v_C * I_{C_{av}} + r_C . {I_{C_{RMS}}}^2 \tag{7.17}$$

$$Diode\ switching\ losses = \frac{1}{4} Q_{rr} v_{drr} f_{sw} \tag{7.18}$$

$$IGBT\ switching\ losses = (E_{ON} + E_{OFF}) f_{sw} \tag{7.19}$$

where v_D is the diode on-state voltage drop, $I_{D_{av}}$ is the diode average current, r_D is the diode on-state resistance, $I_{D_{RMS}}$ is the IGBT RMS current, v_C is the IGBT on-state voltage drop, $I_{C_{av}}$ is the IGBT average current, r_C is the diode on-state resistance, $I_{C_{RMS}}$ is the IGBT RMS current, Q_{rr} is the reverse recovery charge of the diode,

Based on the calculated device losses, a thermal model, as shown in [152] is used in Simulink to obtain the device junction temperature. A mathematical electro-thermal (Foster) model was implemented in Simulink with the transient thermal impedance parameters provided in the datasheet of F3L400R12PT4_B26. There are 4 different time constants for the thermal model (for IGBT and diode), and the resulting temperature rise is calculated as

$$Temp = P(t) \times \left[R_{thQ1}(1 - e^{-t\tau_{Q1}}) + R_{thQ1}(1 - e^{-t\tau_{Q1}}) + R_{thQ1}(1 - e^{-t\tau_{Q1}}) + R_{thQ1}(1 - e^{-t\tau_{Q1}})\right] \quad (7.18)$$

$P(t)$ is the device loss calculated in PSIM. For instantaneous junction temperature estimation, the device losses were calculated over a shorter period (over a switching cycle), whereas, for steady-state junction temperature, device losses were calculated over a longer period (over a complete fundamental cycle). R_{thQi} is the ith thermal resistance of the IGBT/diode and τ_{Qi} is the ith thermal time constant of the IGBT/diode.

Appendix B: Components of Hardware Setup

The diagrams below show the different parts of the experimental setup. It consists of the following: Two three-level T-NPC inverters, DC-link capacitors, DC-link discharge resistors, Three-phase diode rectifier, Gate-drive power supply and gate-drive logic supply. OPAL-RT based hardware prototyping control is used in the setup. The experimental prototype is shown in Fig. Ap_B-1 and Ap_B-5.

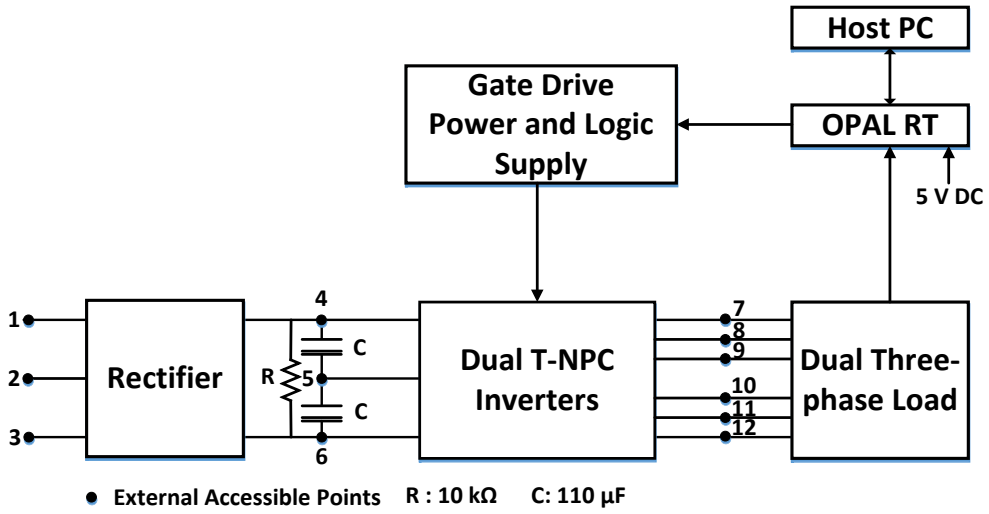


Figure Ap_B-1: Experimental Setup schematics

The schematics of the gate-drive power supply are shown in Fig. Ap_B-2- Ap_B-3. The schematics of the gate-drive logic supply to provide the pulses to the semiconductor devices is shown in Fig. Ap_B-4.

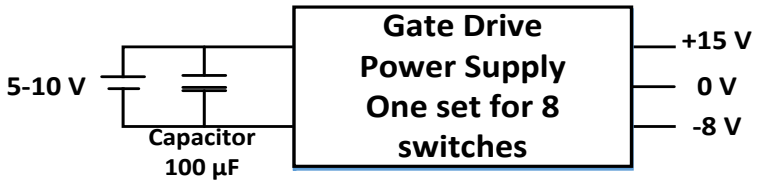


Figure Ap_B-2: Gate drive Power supply block diagram for 8 switches with DC power supply and bypass capacitor; three such sets in the setup

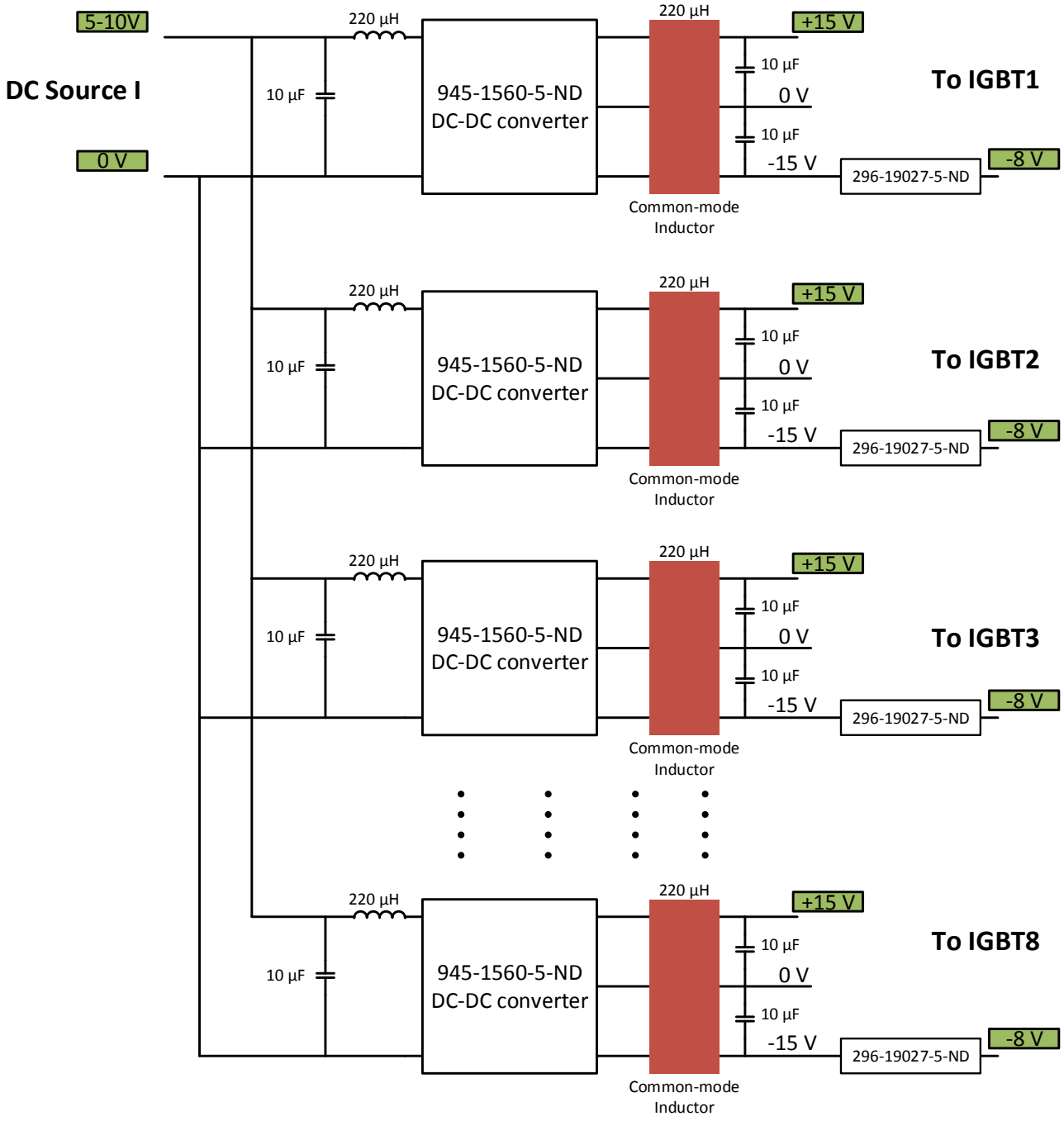


Figure Ap_B-3: Circuit diagram and components of Gate drive power supply (for 8 switches)

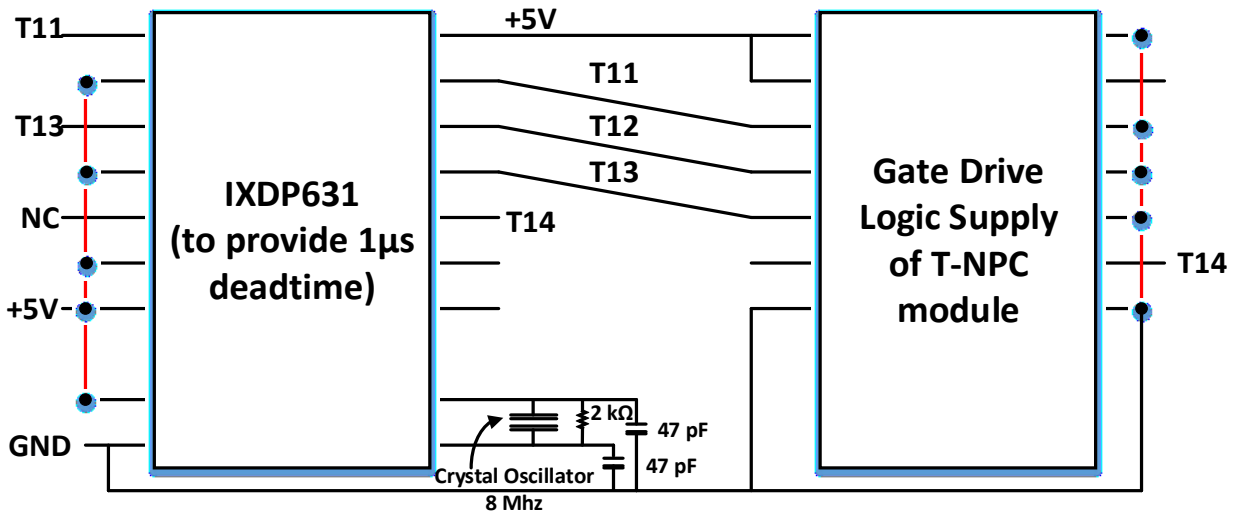


Figure Ap_B-4: Circuit diagram and components of Gate drive logic supply (for 4 switches in one leg)

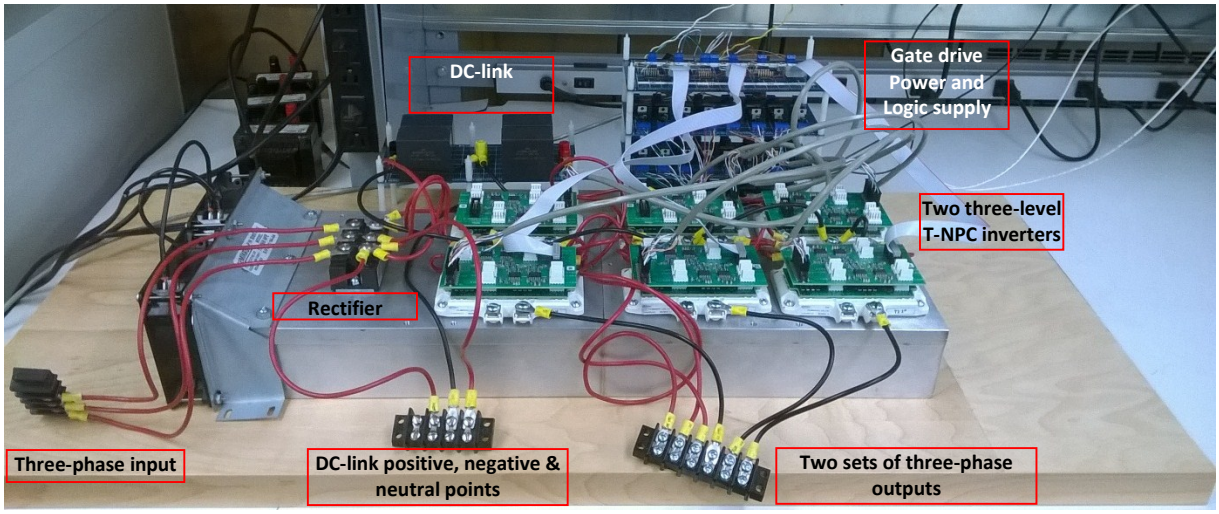


Figure Ap_B-5: The experimental setup of dual T-type inverters

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