CONSTRUCTION AND TEST OF A SPWM CURRENT SOURCE CONVERTER

by

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ABSTRACT

The thesis describes a stand-alone, unity power factor, current-regulated SPWM rectifier. The topology is based on the series connection of 3 single-phase, 4-valve rectifier bridges, which allows 2-state logic SPWM strategy to be used without interphase interference. The issues and problems of LdI_{dc}/dt voltage and low harmonic waveform distortion are identified. Solutions are found by using a dc snubber circuit and a simple local notch filter feedback circuit which performs the dual function of stabilizing and active filtering. From the clarification given by this more expensive but less constrained topology, the stage is set for the next step in incorporating the lessons learnt here to the more economical topology based on the 6-valve, 3-phase parallel bridge, which requires a tri-state logic for PWM control when operating in the current-source configuration.

RÉSUMÉ

Cette thèse décrit un redresseur autonome avec facteur de puissance unitaire, à l'impulsion de largeur variable sinusoïdale régulé par le courant. La topologie est basée sur la connection en série de 3 ponts de redresseurs monophasés à 4 valves, qui permet l'utilisation de la stratégie d'impulsion de largeur variable sinusoidale avec logique à 2 états sans interférence d'interphase. Les questions et problèmes du voltage LdI_{cc}/dt et de distortion de forme d'onde à basses harmoniques sont identifiés. Des solutions sont trouvés dans l'utilisation d'un circuit amortisseur à courant-continu et d'un simple circuit localisé bouclé à l'élimination de bande qui en même temps stabilisent et filtrent activement. Les leçons apprises de cette topologie plus coûteuse mais moins contrainte peuvent être incorporées à la topologie plus économique basée sur le pont parallèle triphasé à 6 valves, qui requiert une logique à 3 états pour le contrôle à l'impulsion de largeur variable lors de son opération dans la configuration source de courant.

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TABLE OF CONTENTS

NOMENCLATURE

V_a, V_b, V_c	Three phase ac current source converter input voltages
V_{sa}, V_{sb}, V_{sc}	Three phase ac voltage source converter input voltages
V_{ca}, V_{cb}, V_{cc}	Three phase ac capacitor voltage
V_c	Voltage source converter capacitor voltage
V_{1a}, V_{1b}, V_{1c}	Output voltage across each phase of the current source converter
V_2	DC link voltage
Vc1	Voltage across snubber capacitor
i_a, i_b, i_c	Three phase ac current source converter input currents
i_{ca}, i_{cb}, i_{cc}	Three phase ac capacitor current
i_{3a}, i_{3b}, i_{3c}	Three phase modulating current
I_{dc}	DC link current
I_{REF}	DC link reference current
I_R	Raise edge signal
I_L	Lower edge signal
L_T	AC side equivalent inductance
L_{dc}	DC link inductance
R_T	AC side equivalent resistance
R	Snubber resistance
C	AC capacitance
C1	Snubber Capacitance
D1	Snubber diode

PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
f_c	Switching frequency
f_m	Modulation frequency
m_f	Frequency modulation ratio
X_m	Modulating signal amplitude
X_T	Triangular Carrier signal amplitude
MI	Modulation index
T1	Positive half cycle transistor group
T2	Negative half cycle transistor group
ϵ	Error signal
k_p	Outer feedback gain
k_f	Inner feedback gain
GTO	Gate turn off thyristor
ω	Angular frequency
Q1	Logic signal to transistor group T1
Q2	Logic signal to transistor group T2
r.m.s	Root mean square
BD	Base drive unit
BDL	Base drive logic
β	The angle between ac input voltage and ac control current
$\delta T1$	Snubber capacitor charging period
$\delta T2$	Snubber capacitor discharging period
f	Frequency
f_n	Notched frequency

CHAPTER I

INTRODUCTION

1.1 INTRODUCTION

The development of power electronic industry started with the thyratrons and mercury arc rectifiers, and then, the thyristors. In recent years the industry has been enjoying the use of power semiconductor devices like: Bipolar Junction Transistor (BJT), Gate Turn Off thyristor (GTO), and power MOSFET. Now, at the turn of this century there have emerged modern power semiconductor devices which are: Insulated gate bipolar transistor (IGBT), Static induction transistor (SIT), Static induction thyristor (SITH) and MOS-controlled thyristor (MCT).

The invention of these power semiconductor devices has been simplifying and advancing the capabilities of power electronics in its applications.

The advances of semiconductor research over the past decades have resulted in the following benefits: (a) the improved voltage and current rating of power semiconductor devices, (b) their increased switching speed, (c) the simplified means of controlling power semiconductor devices, and (d) the reduced cost of these modern power semiconductors devices.

For the above reasons many new converter topologies have been developed. But, until recently diode and thyristor

rectifiers have remained dominant in the AC to DC converters despite that the harmonics of their line currents are relatively high and their power factor decreases with increasing firing angle. The bidirectional properties of both rectifying and generating capabilities have also attracted many researchers to the forced commutated converters. This research has been mainly of two kinds: (a) the current source converter, (b) the voltage source converter.

The research on the two topologies is still in their early stages. The winning topology is yet to be known. However, the current source inverter has until now demonstrated high reliability and excellence in its application with variable speed drives.

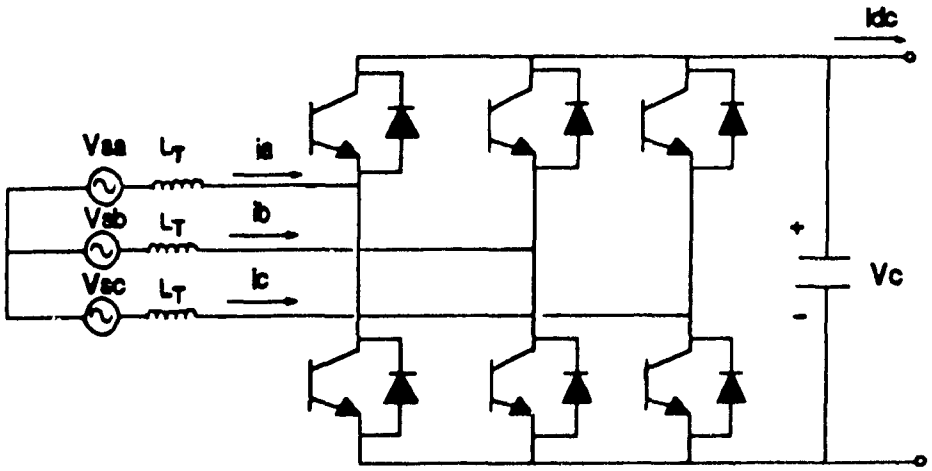


Fig. 1.1(a) Schematic of 3-phase Voltage Source Converter

In a 3-phase voltage source converter of Fig.1.1(a), only six valves are connected in parallel across the dc link. This parallel connection finds its dual in the series connection as shown in Fig.1.1(b). However, twelve switches are needed now, four in each phase forming the single phase bridge converter. The parallel current source converter though economical, has many problems which have to be resolved. For instance, the ac capacitor voltages in the three phase bridge are not equal and cannot in principle be connected in parallel, unless two of the three valves in the upper half of the bridge and two in the lower half are blocking.

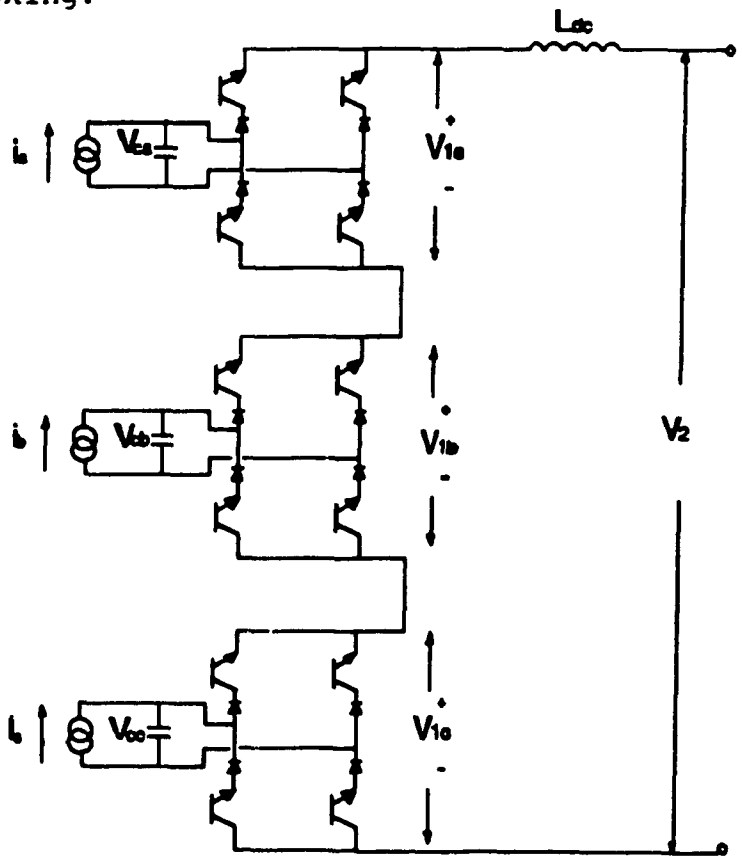


Fig. 1. 1(b) Schematic of 3-phase Current Source Converter

The aim of many researchers, whether developing current or voltage source converters, has been to produce converters capable of delivering sinusoidal current waveform at the input with high power factor. They have been concerned also on the possibility of varying the voltage and frequency.

Various PWM techniques have been used. For the purpose of this thesis only the Sinusoidal PWM technique is described.

1.2 SINUSOIDAL PWM

In the sinusoidal PWM strategy, a sinusoidal control signal is made to intersect with a triangular carrier waveform, as shown in fig.1.2(a).

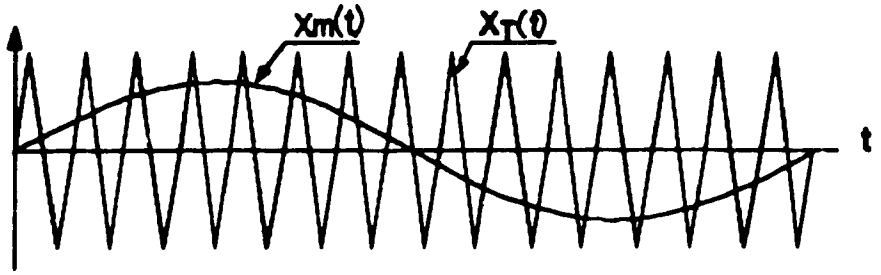


Fig. 1.2(a) Intersection of Modulating and Triangular Carrier Signal

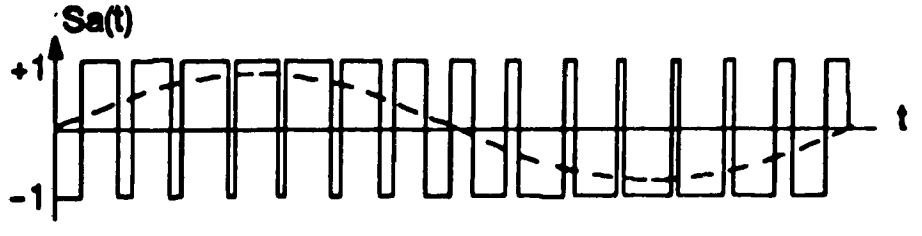


Fig. 1.2(b) SPWM Signal with its Fundamental

The converter switching frequency is determined by the triangular carrier frequency, f_c. This frequency together with its amplitude X_r are normally kept constant. The control signal, $X_m(t)$ with a frequency, f_m is used to modulate the switch duty ratio.

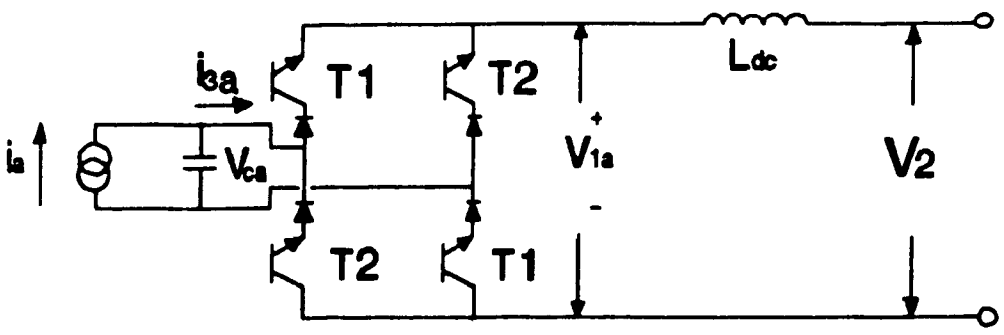


Fig. 1.3 Schematic of Single Phase Current Source Converter

To explain how the SPWM signal is obtained, consider the a-phase of the current source converter of fig.1.3. The switching states of the power electronic valves T1 and T2 are described by the switch function Sa(t) which assumes the value of:

Sa(t) = +1 when T1 conduct and T2 block

Sa(t) = -1 when T2 conduct and T1 block

The ON and OFF of the switches T1 and T2 depend on the magnitude of $X_m(t)$ and $X_T(t)$. The following output results will be obtained:

$X_m(t) > X_T(t)$, T1 is on, Sa(t) = +1

$X_T(t) > X_m(t)$ T2 is on, Sa(t) = -1

The switching states Sa will be alternating between -1 and +1. The SPWM signal and its fundamental frequency component are shown in fig.1.2(b).

In fig. 1.2(a), $X_m(t)$ and $X_T(t)$ are time functions of two general variables. Up to the present, most SPWM schemes are applied to voltage systems. In this thesis, it is the current which is modulated. Thus, when the dc link current is I_{dc}, then

$$i_{3a} = Sa(t) \cdot I_{dc} \qquad (1\text{-}1)$$

where the switching function Sa(t) of fig.1.2(b) is based on the intersections of $X_m(t)$ and $X_T(t)$ of fig.1.2(a).

1.3 THE SPWM CURRENT SOURCE CONVERTER

The objective of the research reported in this thesis is to produce a stand-alone, current-source rectifier which meets the following specifications:

(1) near sinusoidal current waveform at unity power factor on the ac side

(2) regulated dc link current

Such a rectifier can be applied as: (a) a high quality dc source to the current-source inverters in variable speed ac

drives, (b) a high quality rectifier in variable speed dc drives without the need of a chopper intermediate controller.

The Sinusoidal PWM (SPWM) strategy is considered here because its switching harmonics are predictable. A high quality current waveform is obtainable at low switching frequencies.

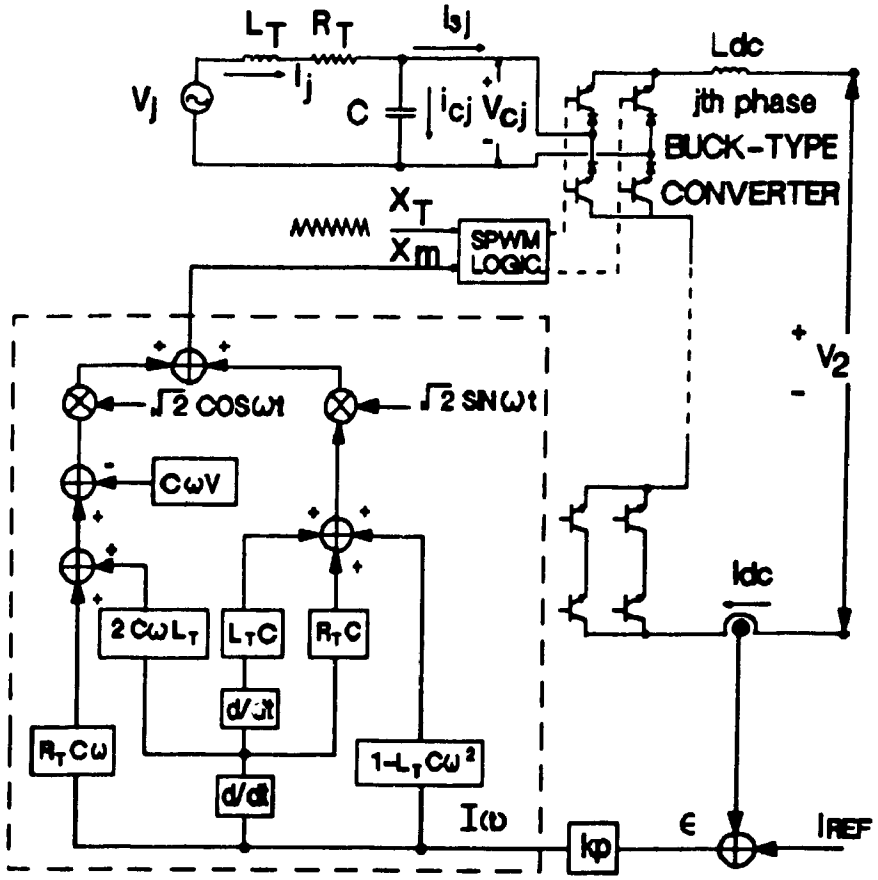


Fig. 1.4 Schematic of SPWM Current Source Converter Control

There are many problems which have to be solved before the specifications can be met. The list of problems begins with the circuit topology. Recently, it has been recognised that the current source 3-phase bridge topology allows at most only one upper valve and only one lower valve to conduct at any time instant. In applying the pulse width modulation technique, a strategy for tri-state logic has to be developed and through the tri-static logic, recent workers [3,4,5,6] have finally succeeded in producing sharply defined near sinusoidal current waveforms which meet the specifications under steady state. These tri-state logic schemes have been designed for static situations and while they may also function for dynamic situations, further research will be required to confirm their capabilities to convey dynamic transient information through the tri-logic pulse widths.

The research leading to this thesis examines the current-source topology based on the series connection of 3 single-phase full bridge as shown in fig.1.4.

As fig.1.4 requires 12 valves and 3 transformers, it is not economical compared to the 6-valve 3-phase bridge configuration used in Ref [3,4,5,6]. The purpose of fig.1.4 is that it serves as a research tool by which the attributes of the current source topology can be studied apart from the dynamically unproven tri-state PWM strategies. The delta modulation [2] or the SPWM strategies can be applied directly to each of the 3 single-phase bridges using the

familiar two-state switching logic without fear of inter-phase interference of the switching of the valves. Both the delta modulation and the SPWM strategies cannot be faulted in dynamic situations because the pulse widths are known to represent faithfully the value of the modulating signal at the sampled period. For this reason, the more expensive topology of fig.1.4 allows the researchers to investigate what feedback configuration is necessary to ensure that the current regulation is stable. In Ref [2], one finds that when the delta modulation strategy is used, the feedback signal must include one d/dt operator on the error signal. As will be shown in this thesis, the SPWM strategy requires a d^2/dt^2 operation on the error signal.

The topology of fig.1.4 also allows another problem to be identified and solved. The problem is recognized as low harmonic ac current waveform distortion which persists even though the valves implement the SPWM strategy without a fault. The origins of the low harmonic distortion may be: (a) ac circuit L_T-C resonance, (b) ac side harmonic pollution arising from the magnetic circuit saturation, (c) harmonics carried by the feedback channels. In order to meet the specification of near sinusoidal fundamental waveform, it is clear that the rectifier must also be an active filter to clean up the harmonic distortion.

A second contribution of this thesis is that an inner feedback loop using a twin-tee notch filter enables the two problems to be overcome:

(1) active filtering to remove the low order harmonic pollution on the ac side

(2) securing an extensive stable domain without the need of implementing the second differentiation, d^2/dt^2.

As the author does not have a background in control theory, the stability analysis has been done by Professor S.Z.Dai. The thesis does not cover the research in stabilization.

The thesis reports on the problems associated with the destructive $L_{dc}dI_{dc}/dt$ voltage when the 4-valve bridge has a non-conduction period. The thesis discusses the reasons for the occurrence of the non-conduction period. It also analyses the requirements of the dc snubber circuit for efficient protection.

With an understanding of the requirements for stabilization and active filtering in the circuit of fig.1.4, the next step of research consists of translating the solution to the economical 6- valve 3-phase bridge.

This research in SPWM control follows previous work in delta-modulation control [2]. The SPWM control has the advantage of yielding comparable waveform quality at a lower, more regular switching frequency. Furthermore, it is in the main stream and is preferred by many workers.

1.4 PRINCIPLES OF SPWM CONTROL IN CURRENT SOURCE TYPE RECTIFIER

Irrespective of the topology, whether it is the 6-valve 3-phase bridge or the circuit as shown in fig. 1.4, the stability problem which is identified here is inherent in SPWM control. This is because it arises from the capacitor C which must be connected in shunt across the ac terminals of the converter to serve as a buffer between the equivalent inductance L_T on the ac circuit and the dc link inductance L_{dc}.

Fig.1.4 shows the series connection of the three single-phase full bridge converters. On the dc link side, the inductance L_{dc} must be sufficiently large to ensure a reasonably smooth dc current $I_{dc}(t)$. For dc current regulation, the measured value of $I_{dc}(t)$ is compared with a reference I_{REF} and the error ϵ is used in the negative feedback loop to request the rectification of sufficient ac power to maintain the stored magnetic energy $0.5L_{dc}I_{dc}(t)^2$ in the face of dc power demand, $V_2(t)I_{dc}(t)$, of the rectifier output.

The output of the feedback block enclosed by broken lines consists of the modulating signal $X_m(t)$, which is inputted in the SPWM LOGIC block together with the triangular wave carrier signal $X_T(t)$. The 4 valves as controlled by the SPWM LOGIC block admit positive and negative pulses of I_{dc} of varying widths into the ac side. Designating the fundamental harmonic of this train of pulses

as the modulating current $i_{3_j}(t)$, the single-phase full bridge converter may be thought of as a linear amplifier because $i_{3_j}(t)$ is proportional to the modulating signal $X_m(t)$. The analysis in chapter III describes how this linear amplifier can be integrated with the block enclosed by broken lines to ensure unity power factor operation.

1.5 THESIS COVERAGE

The main aim of this thesis is to construct and test a laboratory size SPWM current source converter. The converter has been tested in a rectifier mode only.

In order to be able to compare with other control techniques, this rectifier has to be able to generate 3-phase sinusoidal current at unity power factor with dc current regulation.

1.6 ORGANISATION OF THE CHAPTERS

Chapter II describes the power circuit which consists of bipolar power transistor, the ac snubber circuit and the base drive unit.

Chapter III gives the mathematical formulation of the modulation signal and its practical implementation. The generation of the triangular carrier waveform is also discussed in this chapter.

Chapter IV discusses the current snubber circuit in the dc side capable of protecting the converter, during the interruptions of the dc link current flow during the turning

off of the switches.

Chapter V describes the local notch filter feedback that is used to overcome the harmonic distortion in the control signal.

Chapter VI presents the digital simulation results, together with the experimental results before and after the inner feedback loop.

Chapter VII presents the conclusion of this work and the scope for further research in this area.

CHAPTER II.

THE POWER CIRCUIT.

2.1 INTRODUCTION

The power circuit consists of:

(1) A series connection of 3 galvanically isolated single-phase bipolar transistor full bridge

(2) The ac snubber circuits

(3) The base drive (BD) circuits

(4) The dc snubber circuits

The detailed design of the series connection of 3 galvanically isolated single-phase full bridge, the ac snubber circuits and the base drive units can be found in [8]. Details on the dc snubber circuit will be presented in chapter IV.

The ac snubber circuit and the base drive units have been made on printed circuit boards. This is because no much changes are expected in these circuits which have been used previously in Ref.[7,8] and which have proved to be working perfectly. Some minor changes have been made on the ac snubber circuits.

2.2 THE CURRENT SOURCE PWM BRIDGE CONVERTER

Fig 2.1 shows the complete circuit diagram of the current source PWM bridge converter excluding the ac snubber circuit. Each transistor receives signal from its respective

base drive unit (BD). Since the upper transistors of each phase are common emitter connected, their base drives [e.g BD1 and BD2 for phase a] share a common power supply. Each of the lower base drive units has its own independent dc power supply.

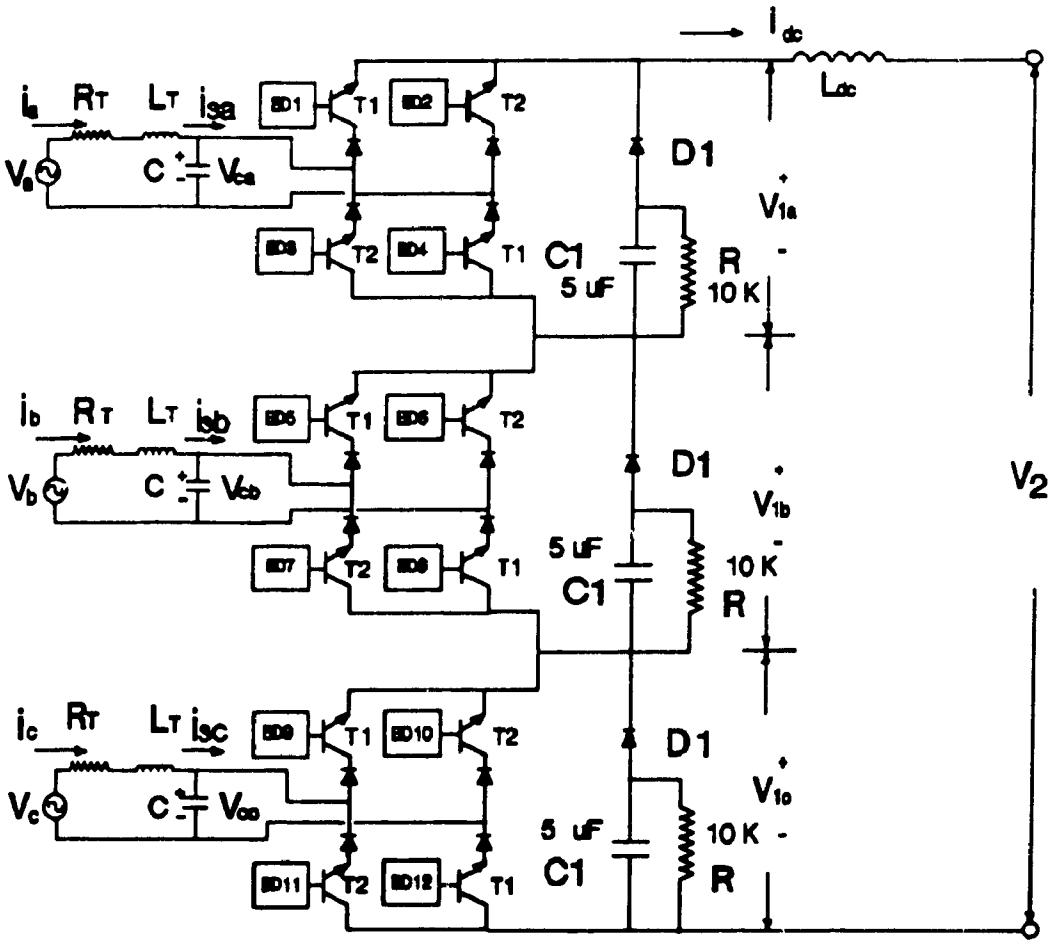


Fig. 2. 1 Series Connection of Three Single-Phase Full Transistor Bridge

The ac voltages V_a, V_b and V_c represent the outputs of transformer secondaries. The elements R_T and L_T include the resistance and leakage inductance of the transformer together with inductance added for filtering purpose. The capacitance C is required for the proper switching of the transistor because a shunt current path is necessary between L_T on the ac side and the inductance L_{dc} on the dc side.

Each of the 3-ac phases has its 4 transistor single-phase bridge converter. As the transformer secondaries "float", the dc side voltages of each bridge V_{1a}, V_{1b} and V_{1c} can be added serially:

$$V_1(t) = V_{1a}(t) + V_{1b}(t) + V_{1c}(t) \qquad (2\text{-}1)$$

The output voltage is defined by V_2.
The dc link current $I_{dc}(t)$ is solved from the equation:

$$L_{dc}dI_{dc}(t)/dt = V_1(t) - V_2(t) \qquad (2\text{-}2$$

In the current source (buck-type) converter, $I_{dc}(t)$ is the dominant variable. It is assumed that L_{dc} is sufficiently large so that $I_{dc}(t)$ is virtually a constant current, in the time intervals between the switchings of the transistors.

The current I_{dc} cannot be interrupted abruptly because the $L_{dc}dI_{dc}(t)/dt$ voltage would cause overvoltages which would cause component failures. For this reason the capacitor C1 with the diode D1 provide an alternate path

when the transistors happen to block simultaneously. The resistance R allows the voltage built up across the capacitor C1 to discharge.

The dc snubber circuit consisting of D1, C1 and R will be discussed in greater detail in chapter IV.

The principle of operation of the converter taking phase a as an example is as follows: When transistor group T1 is turned ON by receiving the appropriate gate signal from the base drive, the capacitor C assumed to have polarity as shown in fig 2.1, has the current I_{dc} flowing through the negative terminal of the ac capacitor, thus decreasing the voltage, V_{ca} across it. When transistor group T2 is ON, and transistor group T1 is OFF, current flows from the positive terminal to the negative terminal of capacitor C thus increasing the capacitor voltage, V_{ca}. Fig 2.2 shows a photograph of the capacitor voltage V_{ca}, taken from the oscillogram, showing alternate charging and the discharging of the capacitor. By controlling the widths of the charging and discharging current pulses, it is possible to control the overall waveform of the capacitor voltage.

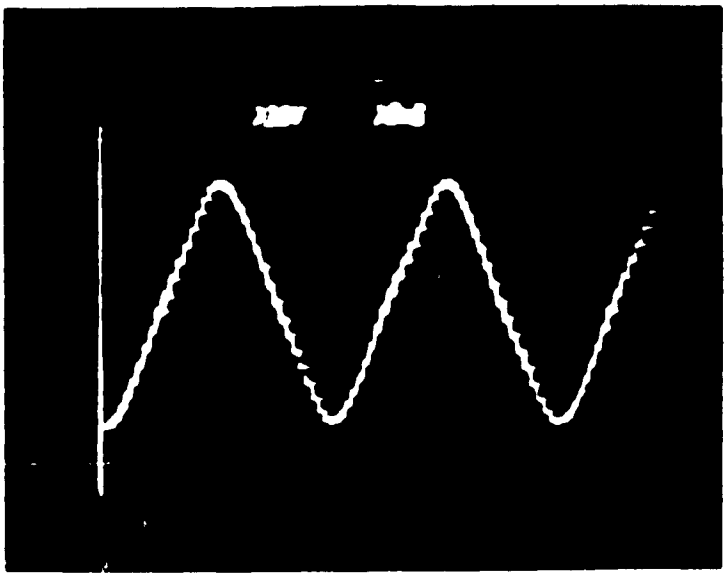


Fig 2.2 The ac capacitor voltage.

2.3 BASE DRIVE CIRCUIT.

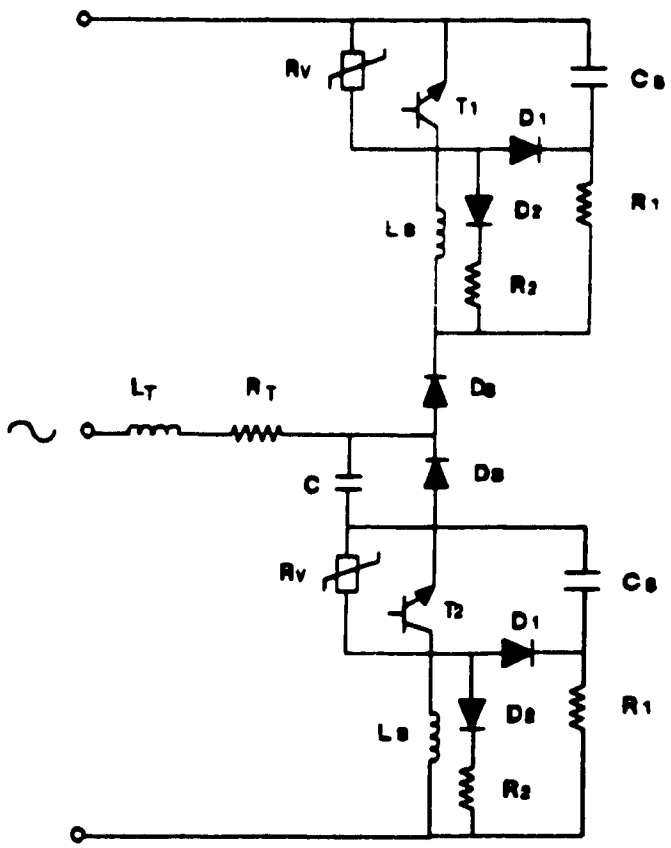
The base drive circuit that has been used can be found in [7,8]. The SPWM signal from the logic of the control circuit is fed directly to the optocoupler of the base drive circuit, to provide isolation between the control and the power circuitry. Since details on design, circuit diagrams and the operation of this circuit can be found in [7,8], readers interested in this work are requested to refer to these references.

2.4 THE POWER BIPOLAR TRANSISTOR.

The bipolar transistor was not an automatic choice. Thyristors, MOSFET's and GTO's were given due consideration. Because of the previous experiences in successfully operating PWM converters, the bipolar transistors continue to be used in this research. The objective of the research is to study the SPWM technique applied to the current source (buck-type) topology. The principles which are established experimentally in this work, have the same validity in GTO's, MOSFETS etc. provided the scaling laws are applicable and provided the switching frequencies are comparable. The bipolar power transistor operates at high switching frequencies and moderately high voltage and current rating. It is inexpensive and familiar. On these bases it was decided to use the Darlington Bipolar power transistor. The data sheets for this device are given in Appendix C.

2.5 THE AC SNUBBER CIRCUIT.

Fig 2.3 shows the snubber circuit that is used to protect the power transistors T1 and T2 against the rate of change of voltage and current (dv/dt and di/dt). Two such snubbers are used for each phase of the transistor bridge. Varistors rated in the range of 350V are used. These varistors clips voltage higher than 350V to protect the bipolar power transistor. More details are described in Ref [7,8].



T1,T2 MJ10015 Bipolar Transistor
Rv 350 V Varistor
D1,D2 MR854 Diodes
D3 40HFL60SO2 Diodes
Cs 0.047uF Capacitors
Ls T60-40, 7t Inductor
R1 68 ohms, 2W Resistor
R2 3.3 ohms, 4W Resistor

Fig.2.3 The ac Snubber Circuit

2.6 SUMMARY.

All the circuits making the power circuit (except the dc snubber circuit) have been discussed. These circuits have been made on printed circuit boards. Their photographs are shown in appendix B. References have been given for readers who would like to go in the detailed design of these circuits. The next chapter describes the mathematical

formulation and the practical implementation of the SPWM signal for switching the transistors.

CHAPTER III

PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This chapter describes the generation of the control signal using the traditional sinusoidal PWM strategy. In the SPWM strategy the switching instants are obtained by intersecting a pure sinusoidal waveform (modulating signal) and a triangular waveform (carrier signal) using a comparison circuit. The bipolar power transistors of the converters are alternatively turned ON and OFF between these switching instants. The generation of both signals is discussed.

It is worth mentioning at this stage, the following important features, which when adhered to, will yield good results:

(1) High frequency of the triangular waveform will result in a good quality of ac current waveform. An added advantage would be the lower cost and size of the harmonic filters. However, excessive switching frequency will cause too much switching losses and may even overload the switching devices. In this respect, compromise must be reached where the advantages should overweigh the disadvantages. From the laboratory experience, a switching frequency of 2160 Hz was observed to give good results.

(2) The modulation index, $MI=X_m/X_t$, where X_m=the

amplitude of the sinusoidal modulating signal and X_T=the amplitude of triangular carrier signal. The size of the SPWM signal is changed by varying the amplitude of the modulating signal, keeping the triangular carrier frequency constant in order to keep the desired average switching frequency substantially constant. The Fourier Series fundamental component of the switching signals is proportional to the modulation signal.

3.2 REVIEW OF SINUSOIDAL PULSE WIDTH MODULATION PRINCIPLE

For convenience fig.1.2(a) and 1.2(b) are repeated here as fig.3.1(a) and (b).

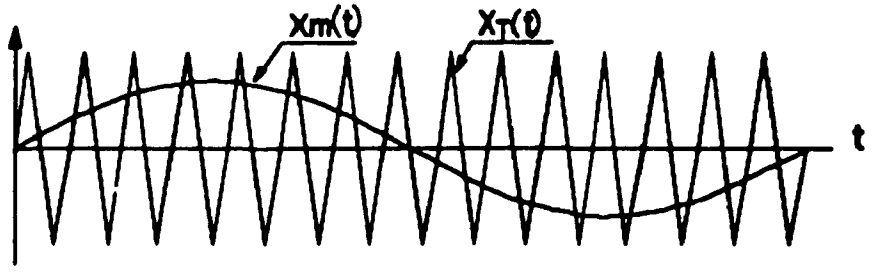


Fig.3.1(a) Intersection of Modulating and Triangular Carrier Signal

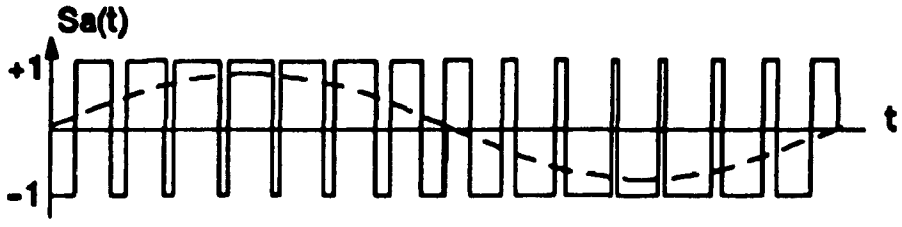


Fig.3.1(b) SPWM Signal with its Fundamental

The goal is to produce a modulating signal which when compared with the carrier signal as shown in fig 3.1(a) will produce SPWM signal with its fundamental shown in fig 3.1(b). The Fourier Series fundamental, as it is well known, is in phase and proportional with the modulating signal.

3.3 PRINCIPLES OF INDIRECT CONTROL

Considering the schematic diagram of a-phase single phase current source converter of Fig 3.2,

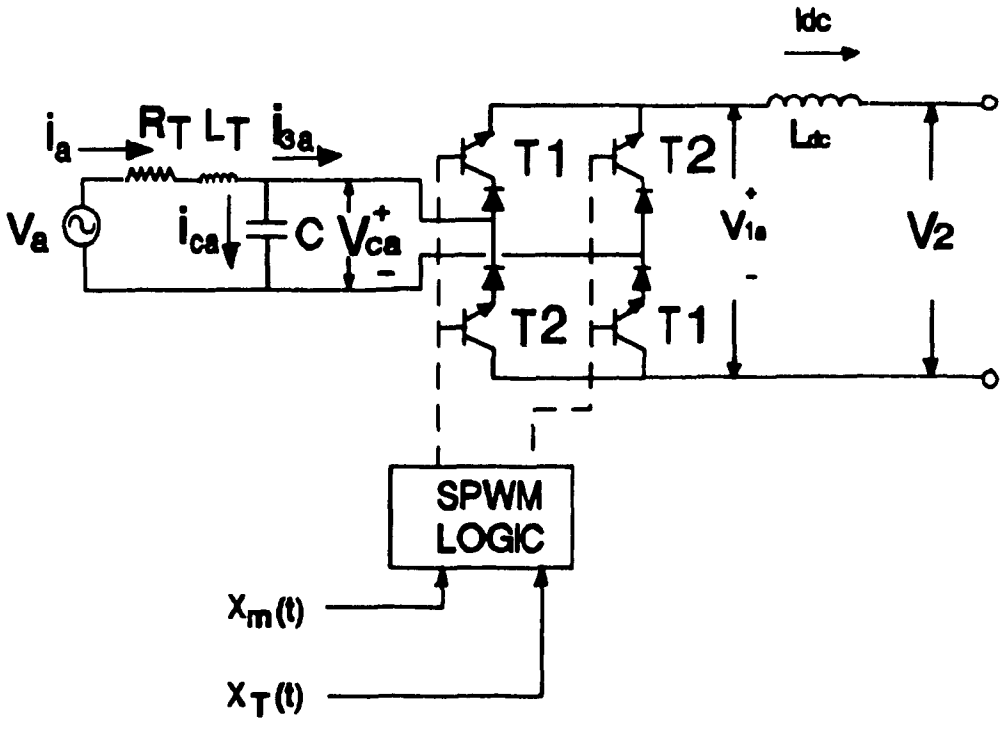


Fig. 3.2 Single Phase Current Source Converter

the ac source voltage,

$$V_a = \sqrt{2} \cdot V \cdot \sin\omega t \qquad (3\text{-}1)$$

where V= the r.m.s phase voltage supplied by the transformer.

The transformer impedance and other inductance added to the ac line for filtering purposes is represented by R_T and L_T.

The objective is to produce an ac current whose Fourier Series fundamental component is in phase with the voltage and whose r.m.s magnitude is I. This fundamental ac current is:

$$i_a = \sqrt{2} \cdot I \cdot \sin\omega t \qquad (3\text{-}2)$$

Since R_T and L_T are known, one can obtain the current i_a of eq.(3-2), provided the capacitor voltage V_{ca} can be controlled precisely.

The b and c phases are identical to Fig.3.2 except for the phase shifts of 120 degrees and 240 degrees respectively. The three phases are connected in series at their dc links.

Kirchhoff's Voltage Law gives the voltage across the capacitor, as

$$V_{ca} = V_a - R_T i_a - L_T di_a/dt \qquad (3\text{-}3)$$

The capacitor voltage in turn is controlled by the injection of the current i_{3a} from the single-phase converter.

By the application of Kirchhoff's Current Law the current i_{3a} is:

$$i_{3a} = i_a - CdV_{ca}/dt \qquad (3\text{-}4)$$

where CdV_{ca}/dt = the current through the ac capacitor
At this stage, only the fundamental Fourier Series component is considered. By substitution of (3-3) into (3-4) gives:

$$i_{3a} = \sqrt{2}\cdot I\cdot \sin\omega t - C\cdot dV_a/dt + R_T\cdot C\cdot di_a/dt + L_T\cdot C\cdot d^2i_a/dt^2 \qquad (3\text{-}5)$$

and further substitution of (3-1) into (3-5) results in:

$$i_{3a} = \sqrt{2}\{[I + R_T\cdot C\cdot dI/dt + L_T\cdot C(d^2I/dt^2 - I\omega^2)]\sin\omega t + [R_T\cdot C\cdot I\cdot\omega - C\cdot\omega\cdot V + 2\cdot C\cdot\omega\cdot L_T\cdot dI/dt]\cos\omega t\} \qquad (3\text{-}6)$$

This is the fundamental of the current that should be produced by the switching of the power transistors. The requirement is therefore, to generate a modulating signal, that would take the shape of eq.(3-6). As mentioned in section 3.2, advantage is to be taken of the fact that, with a modulating signal in the shape of eq.(3-6) properly intersected with a triangular signal, the switched current

intersected with a triangular signal, the switched current waveform based on triggering at the instants at the intersection points would give a SPWM signal whose fundamental Fourier component is also in the form of eq.(3-6).

Referring to fig 3.1(a), the modulating signal can be shown to be in the form of [1] :

$$x_m(t) = \sqrt{2}X_m[\cos\beta\sin\omega t - \sin\beta\cos\omega t] \qquad (3\text{-}7)$$

where X_m = the magnitude of the modulated current and ß is the angular phase shift.

With the switching states alternating between -1 and 1 as in fig 3.1(b), the switching signal can be expressed in the Fourier Series as:

$$Sa(t) = \sqrt{2}(X_m/2X_{Tpeak})\ [\cos\beta\sin\omega t - \sin\beta\cos\omega t] + \sum_{k=2}^{\infty} A_k\sin\omega kt + B_k\cos k\omega t \qquad (3\text{-}8)$$

where, A_k, B_k are the Fourier Coefficients and
X_T = the magnitude of the carrier signal.
In general A_k, B_k are negligible except for selected k near the integral multiples of the carrier frequency. These non-negligible Fourier coefficients are Bessel functions.

In order that the fundamental component of eq.(3-8) will have the form of eq.(3-6), one first put eq.(3-6) in the form:

$$i_{3a} = \sqrt{2} \cdot (a \sin\omega t + b \cos\omega t) \qquad (3\text{-}9)$$

where

$$a = [I + R_T \cdot C \cdot dI/dt + L_T \cdot C \cdot (d^2I/dt^2 - I \cdot \omega^2)] \qquad (3\text{-}10)$$

and

$$b = [R_T \cdot C \cdot I\ \omega - C \cdot \omega \cdot V + 2 \cdot C \cdot \omega \cdot L_T dI/dt] \qquad (3\text{-}11)$$

Eq.(3-7) is now compared with (3-9).
This requires that

$$X_m = \sqrt{(a^2+b^2)}$$

and

$$\beta = \tan^{-1} -b/a.$$

Fig 3.3 is the phasor diagram summarizing the requirements which I_{3a} must fulfil in order that the ac phase current is at unity power factor.

Fig.3.3 shows that for the current I_a to be in phase with supply voltage V_a, the capacitor voltage must be

created so that V_{ca} has the magnitude and the phase angle such that the voltage drop $I_a R_T$ and $j\omega L_T I_a$ must be compensated for. The question is: How can the voltage V_{ca} be created? The answer is: One injects the correct amount of current i_{3a} from the dc link side. This injected current consists of positive and negative pulses of the dc link current whose magnitude is I_{dc}. One varies the pulse widths using the SPWM strategy as illustrated in fig.3.1. The fundamental harmonic of i_{3a} is the phasor I_{3a} in fig.3.3.

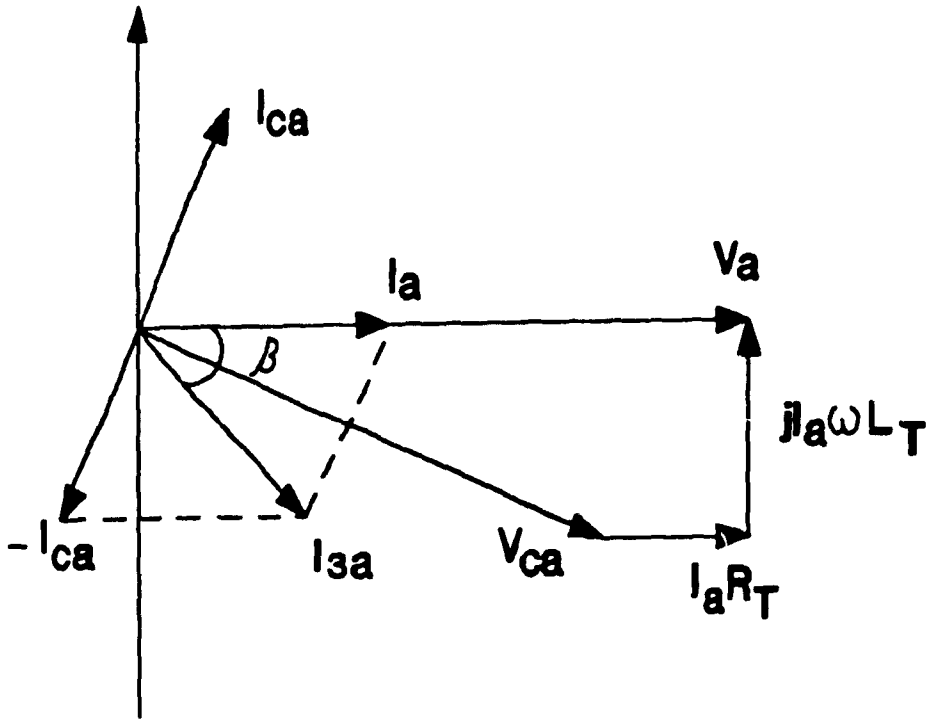


Fig.3.3 Phasor Diagram of a Single Phase Current Source Converter

Based on Kirchhoff's Current Law at the capacitor node in fig.3.2,

$$I_{3a} = I_a - I_{ca} \qquad (3\text{-}12)$$

where I_{ca} is the fundamental harmonic of the capacitor current. Since V_{ca} has been determined and $1/j\omega C$ is known, I_{ca} is also a known result.

The phasor diagram of fig.3.3 is correct only for the steady-state operating condition only. Under transient condition, the capacitive current has two additional terms giving rise to di_a/dt and di_a^2/dt^2 as shown in eq.(3.5) and (3.6).

These two terms must be included so that the stability region is not compromised. Thus in the block diagram of fig.3.4, there are two d/dt blocks in sequence to designate how, in principle eq.(3.5) and (3.6) should be implemented in the feedback.

It is well known that the differentiation operation magnifies high frequency noise. The high frequency noise can be eliminated by a low pass filter. As long as the bandwidth of the signal (which in this case is in the low frequency range) is well separated from the bandwidth of the SPWM switching signal noise (which begins at the frequency around triangular carrier frequency), a single stage differentiation has been implemented successfully [7,8].

It is anticipated that the second differentiation may

not be practical because of the following reason: The feedback channel is based on measuring the dc link current $I_{dc}(t)$, which is compared with the reference current setting I_{REF}, as shown in fig.3.4. The command of the ac current magnitude I(t) is determined by the proportional negative feedback strategy:

$$I(t) = k_p(I_{REF} - I_{dc}(t)) \qquad (3\text{-}13)$$

The noise of I(t) has their origin from $I_{dc}(t)$. By connecting the 3 single-phase converters in series, the second harmonic frequency is eliminated. In practice, it is found that a 6th harmonic is perceptible, after the switching noise has been filtered.

It is barely possible to design the filter for so close a signal-noise separation for the 1st stage differentiation. This is because the filter involves integration which nullifies the action of the differentiator unless the filter cut-off frequency is separated from the signal.

The 2nd stage differentiation is considered to be difficult to achieve. The scope of this thesis is limited to implementing the 1st stage differentiation. The consequence of this limitation is that a larger dc inductance would be needed to operate the system in the stable region.

Future research will be directed towards overcoming the restriction.

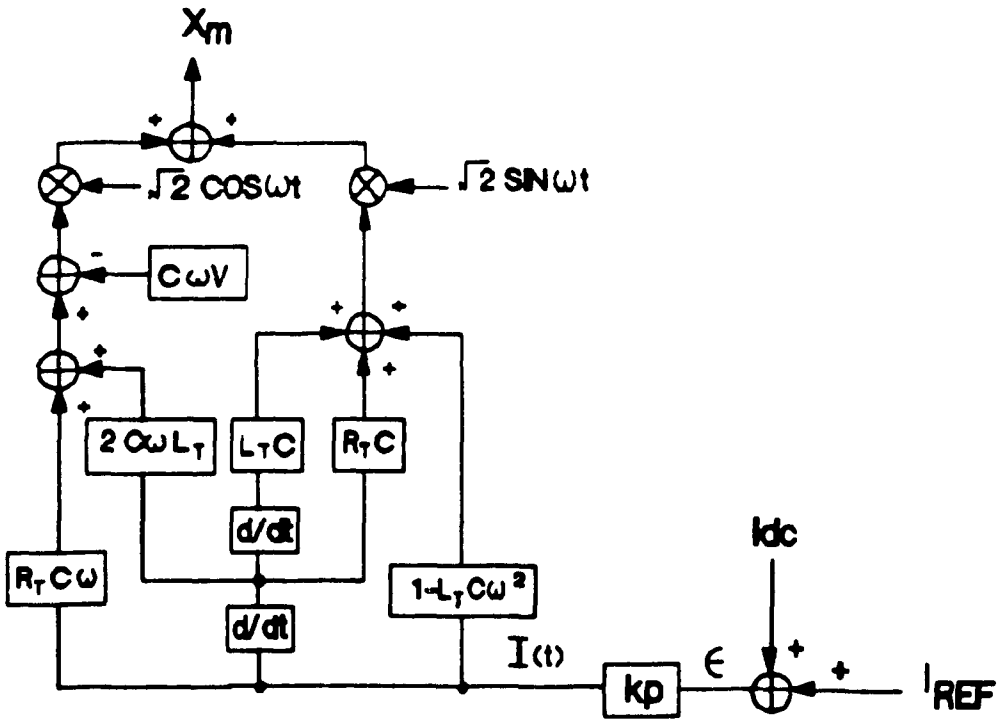


Fig.3.4 Generation of Modulating Signal (Block Diagram)

3.4 PRACTICAL IMPLEMENTATION.

Fig 3.4 shows the block diagram used to generate the modulating signal $X_a(t)$ of a typical phase of the three phases.

This block diagram is derived from eq.(3.6). The input of the control block of fig 3.4 is controlled by the current error, ϵ, which is obtained by comparing the dc link current

and the current reference I_{REF}. Using this outer feedback loop the magnitude of the current can be controlled through a proportional controller k_p.

3.5 CIRCUIT DIAGRAMS OF DETAIL IMPLEMENTATION.

The circuit diagrams to implement the block diagram of fig 3.4 are shown in fig 3.5 and 3.6.

Fig.3.5 shows how the $\sqrt{2}\sin\omega t$ and $\sqrt{2}\cos\omega t$ of the 3 phases are obtained.

Fig.3.6 shows the OP-AMP'S (Operational amplifiers), multipliers and adders which implement Fig.3.4 from I(t) to $X_m(t)$.

Fig.3.7 shows the implementation of the triangular carrier waveform generator.

Fig.3.8 shows the comparator circuit implementing the SPWM logic and the output signal which is fed to the base drive logic.

Fig.3.9 shows the Base Drive Logic circuit, the output signal of this circuit and the transistor switching logical signals.

Fig.3.10 provides an overall view of the integration of the components parts.

3.6 SINUSOIDAL WAVEFORM GENERATOR

The sinusoidal waveforms and their phase angle references are taken from the line voltages as shown in fig.3.5, using step down transformers. Third and fifth

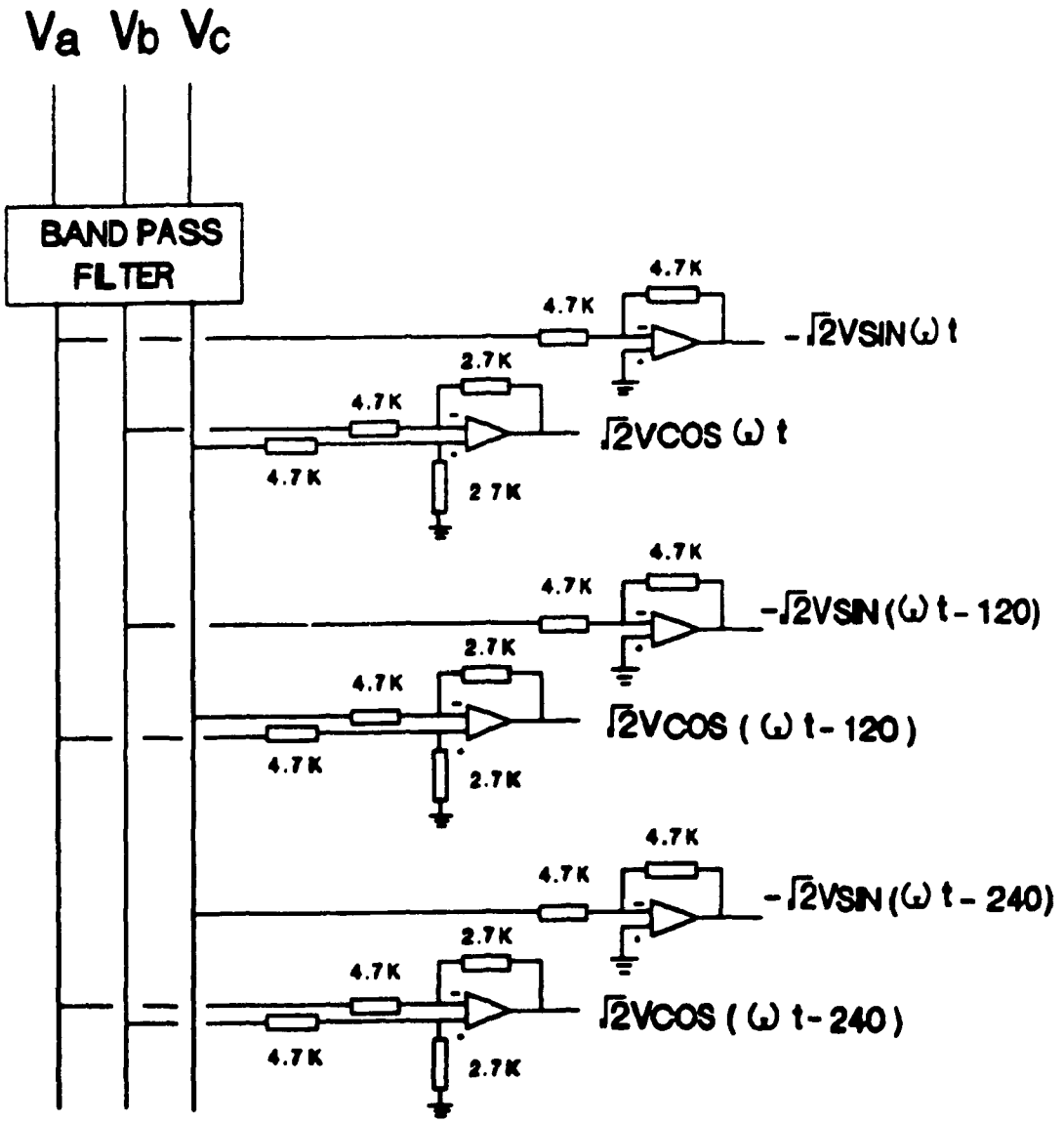


Fig. 3.5 Sinusoidal Waveform Generator

harmonic band pass filters are required to clean the waveforms of the nonlinear distortion coming from the transformer iron. Each of the three phases has its own $\sqrt{2}\sin\omega t$ and $\sqrt{2}\cos\omega t$ waveform references which are multiplied to the circuit of Fig.3.6.

3.7 IMPLEMENTATION OF UNITY POWER FACTOR CONTROL CIRCUIT

Fig.3.6 shows the analogue circuit implementation of the blocks of fig.3.4. The input is the signal I(t) and the output is $X_m(t)$. The components consists of resistors, capacitors, OP-Amps, adders and multipliers. The component values are chosen to match the measured values of C, L_T and R_T of the laboratory experimental model.

3.8 GENERATION OF THE TRIANGULAR CARRIER SIGNAL

Fig. 3.7 is the circuit used to generate the triangular carrier signal. The amplitude of this signal is given by:

$$V_T = \frac{R_2 \cdot V_z \cdot R_4}{(R_1 + R_2) \cdot R_3} \qquad (3\text{-}14)$$

where V_z is the voltage across the zener diode.
The required magnitude of V_T can be achieved by varying the potentiometer R_4. The period of the triangular waveform is obtained from:

$$T = \frac{R_2 \cdot C \cdot R}{R_1} \qquad (3\text{-}15)$$

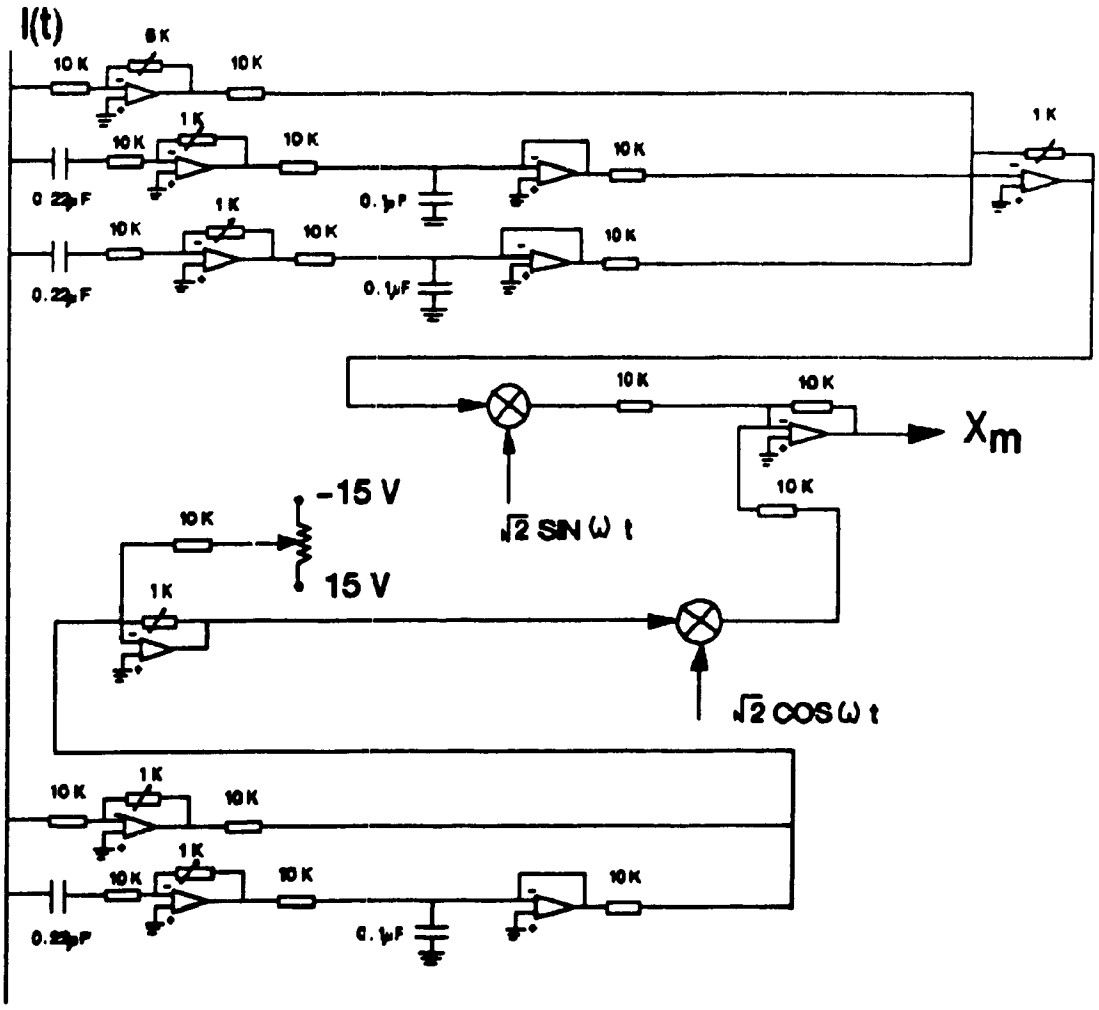
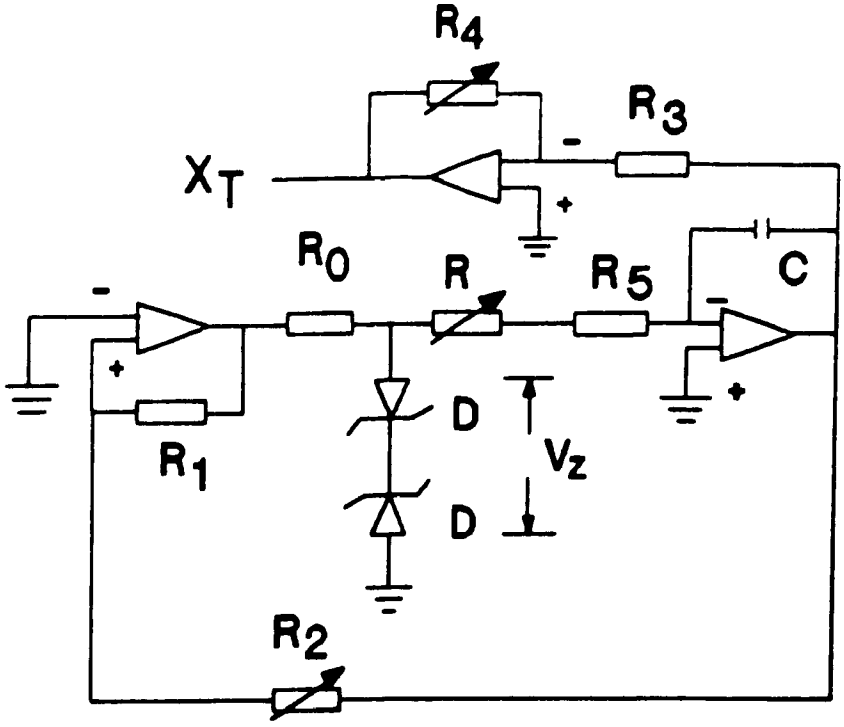


Fig. 3.6 Implementation of Unity Power Factor Control



R	20K Potentiometer
R_0	270 Resistor
R_1	10K Resistor
R_2	10K Potentiometer
R_3	10K Resistor
R_4	20K Potentiometer
R_5	1K Resistor
C	1μF Capacitor
D	Zener Diode IN 756

Fig. 3.7 Generation of Triangular carrier Waveform

the appropriate value is achieved by the variation of R.

3.9 THE COMPARATOR CIRCUIT.

Fig.3.8 (a) shows the comparator circuit. The input to this circuit is the modulating signal $X_m(t)$ and the triangular carrier signal $X_T(t)$.

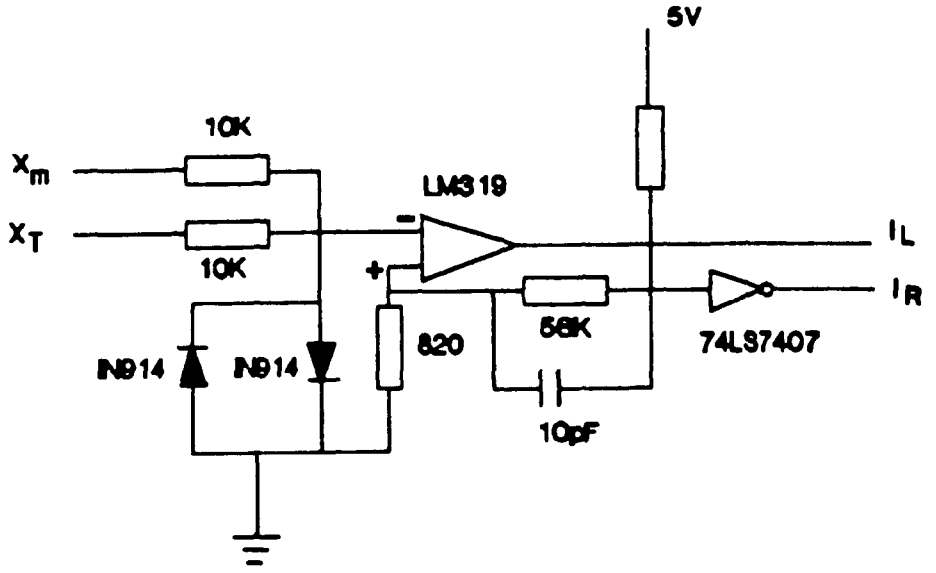


Fig.3.8(a) The Comparator Circuit

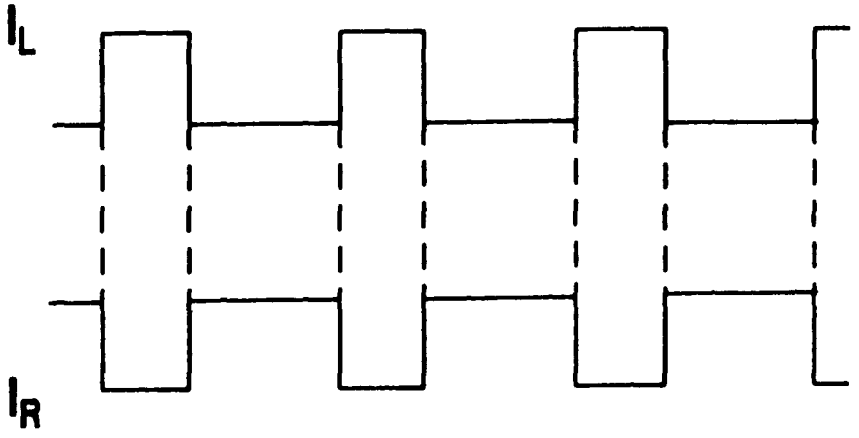


Fig.3.8(b) Output Waveform of the Comparator Circuit

The output signals (I_R) and (I_L) are fed to the base drive logic for switching the power transistors appropriately. The output signal is required to be as fast as possible with minimum uncertainty.

The circuit has been constructed using analogue devices for two reasons: (1) to reduce the delay times in the feedback loop, (2) to keep the cost of the converter to the minimum.

The diodes shown in fig.3.8(a) protects the comparator from over voltages. The cathode of one diode is connected to the anode of the other diode to make the input capacitor as small as possible. This enables the converter to switch at high speed.

Fig.3.8(b) shows the output waveform of the comparator circuit. This output is based on the intersection of the modulating signal, X_m and the triangular carrier signal, X_T. The two output signals are named raise edge signal (I_R) and lower edge signal (I_L) corresponding to the raising and lowering of the current signal, i_{3j} (see fig.3.2) respectively.

3.10 THE BASE DRIVE LOGICAL CIRCUIT.

The base drive logical circuit shown in fig 3.9(a) receives signal from the comparator. The switching instants of the transistors is controlled in this circuit. The original design [7,8] suffered a non uniform delay time between its output and the signal received from the

comparator circuit. This resulted to unstable ac input current and capacitor voltage waveforms. In the new design, stable waveforms have been obtained by using Retriggerable Monostable Multivibrators to obtain constant delay time.

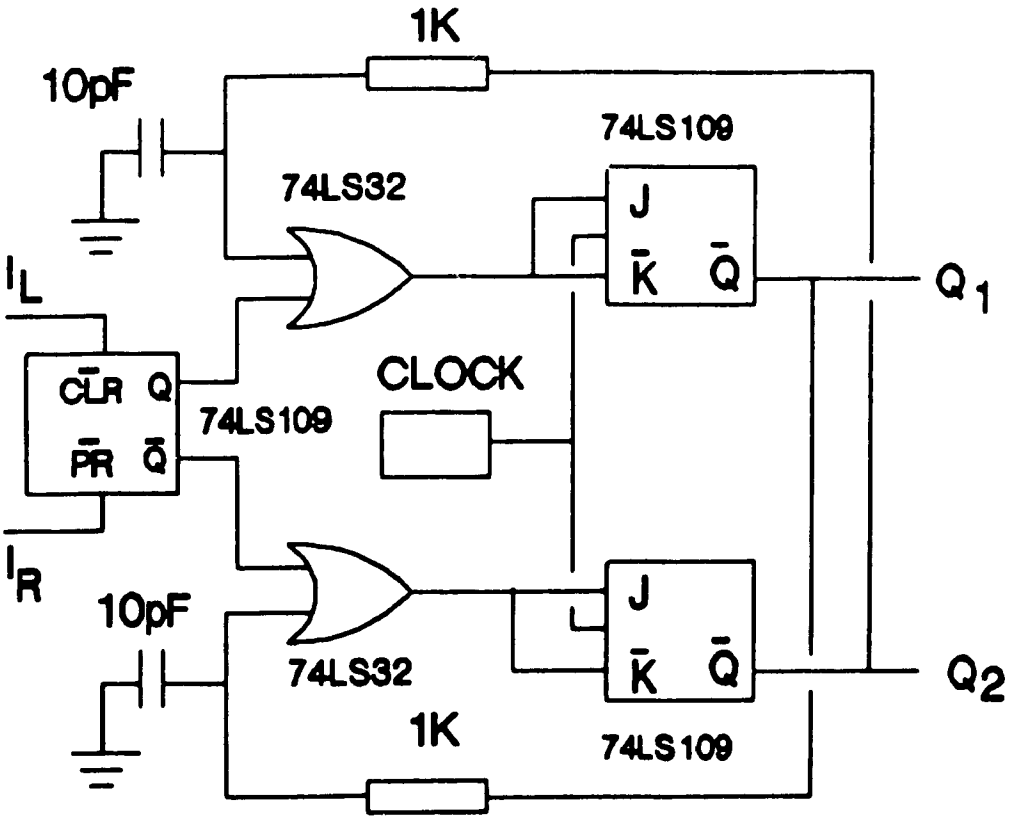


Fig. 3.9(a) The Base Drive Logic Circuit

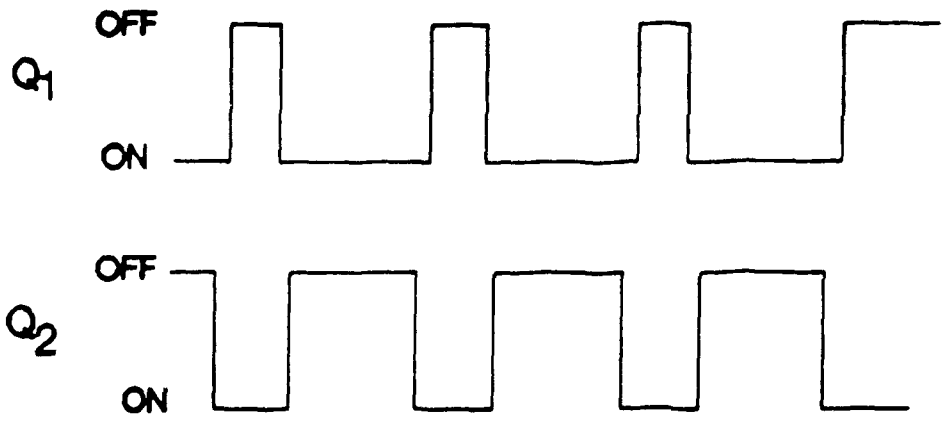


Fig. 3.9(b) Output Signal of the Base Drive Logic

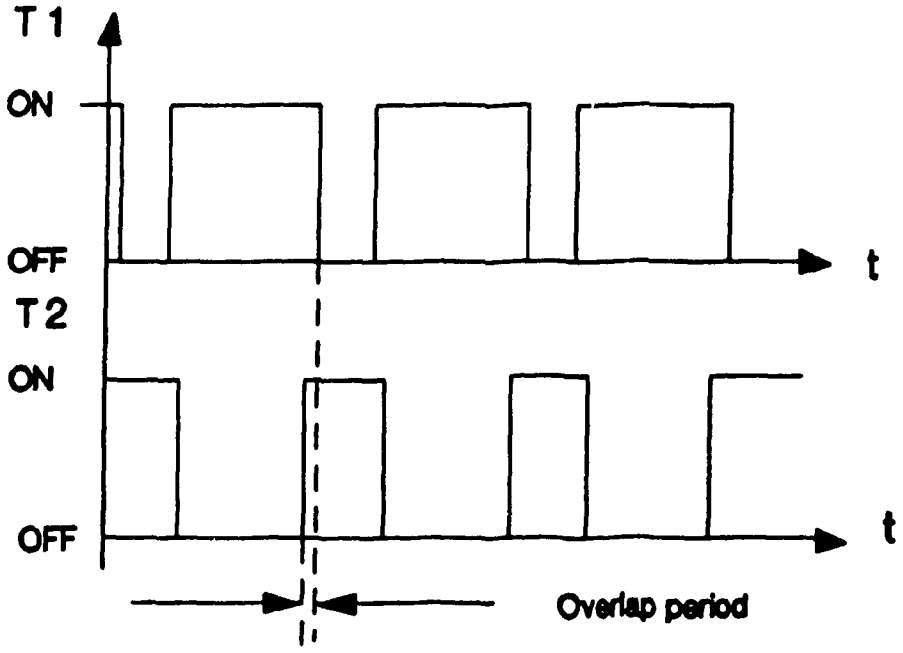


Fig. 3.9(c) Transistor Switching Signals

Fig 3.9(b) shows the output current signal of the base drive logic Q_1 and Q_2. Note that there is an overlap period in each half cycle of each signal, where both transistor

group (T1 and T2) receives gating signal. During this time one transistor group experiences reverse voltage and it cannot turn ON.

Fig 3.9(c) shows the transistor switching logical signals (transistor group T1 and T2) in relation to the intersections of the modulating and carrier signals.

3.11 OVERALL VIEW OF THE CONTROL CIRCUIT

Fig 3.10 shows the complete block diagram of the control circuitry. The block diagram shows the integration of all component parts that form the control circuit. The local feedback notch filter also included in this diagram is discussed in detail in chapter V. All other components parts have been discussed in this chapter.

3.12 SUMMARY.

This chapter described the generation of the control signal using the SPWM technique. The generation of both the modulating and the triangular carrier signal have been presented. Their block and circuit diagrams have been described. The SPWM control logic which consists the comparison circuit and the base drive logic have been discussed. The comparison and the base drive logic circuits were constructed on the printed circuit boards. The circuits for generating the modulating and the triangular signals were made on the bread boards in order to be able to make quick re-arrangement when necessary.

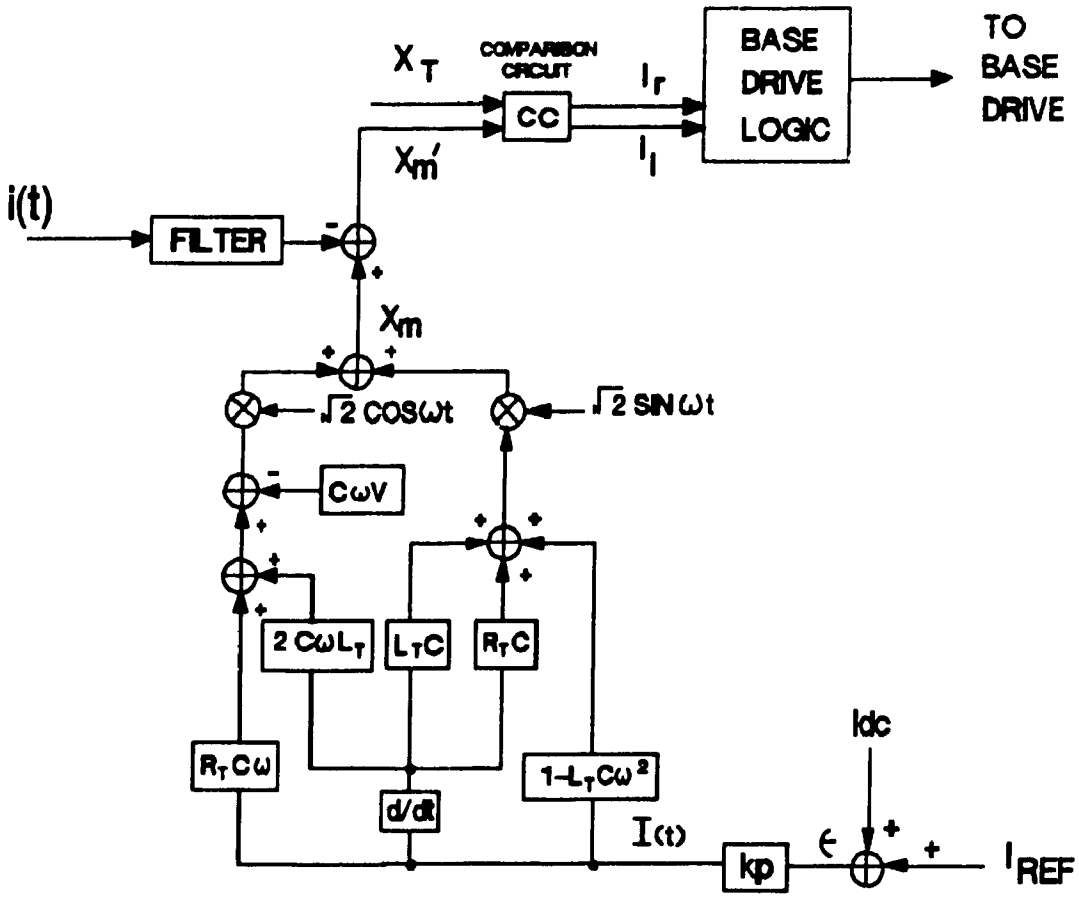


Fig. 3. 10 Overall Control Block diagram

The photographs showing the implementation of these circuits are presented in Appendix B.

Little has been mentioned in chapter II, on the operation of the dc snubber circuit. The next chapter discusses at length this circuit which is responsible for protecting the power circuit against the interruptions of the dc link current flow during turning off the switches.

CHAPTER IV

DC SNUBBER CIRCUIT

4.1 INTRODUCTION

A dc snubber circuit is specifically required in the current source converter for two main reasons:

(1) To protect the circuit against the voltage LdI_{dc}/dt, during the very short periods when none of the transistors in the bridge is conducting.

(2) To enable inverter mode of operation.

As it has been explained in chapter I, this converter is intended to operate in both rectifier and inverter mode. When operated as a rectifier only, the dc voltage output is always positive. In protecting this operation, one requires only a freewheeling diode across each phase of the dc link as shown in fig 4.1. However the inverter operation requires a negative voltage in order to have negative power, since the dc current does not change direction. With just a freewheeling diode in the circuit the inverter operation is impossible since no transistor will turn ON because the freewheeling diode becomes forward biased and the current will just circulate through it and to the load.

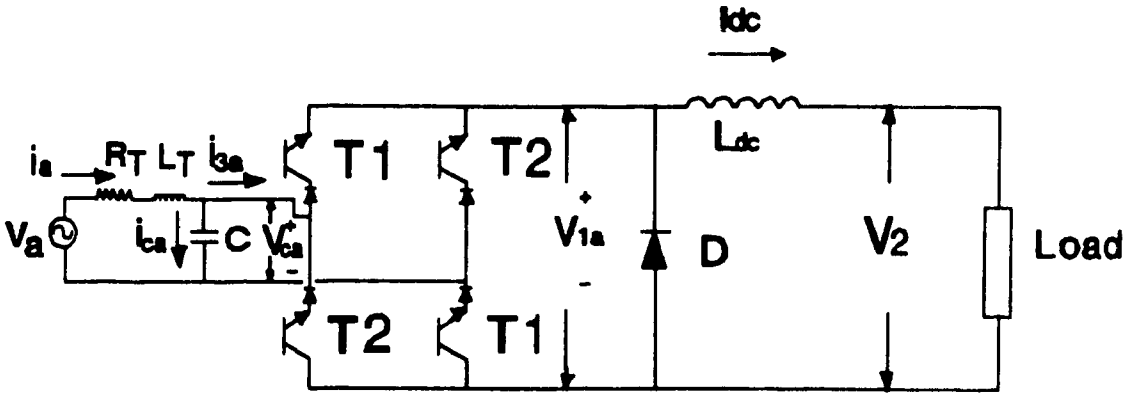


Fig. 4.1 Single Phase Converter with a Freewheeling Diode

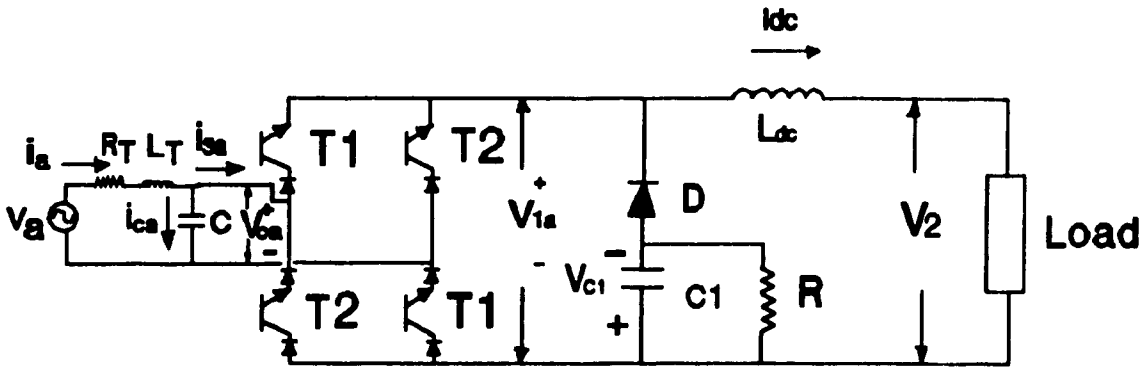


Fig. 4.2 Single Phase Converter with a complete snubber circuit

4.2 DC SNUBBER CIRCUIT

The operation of the circuit of Fig.4.1 as an inverter would be impossible since once the dc voltage is reversed, the freewheeling diode will be turned ON. The remedy to this at first will be to connect a capacitor C1 in series with the freewheeling diode as shown in Fig.4.2. It is required

that this capacitor be charged to a voltage higher than the ac capacitor voltage, so that the transistors T1, T2 are positively biased so that they can be turned ON when they receive the ON gate signals. A resistor should be connected across it to facilitate the discharging of this capacitor. Since the diode conducts current only in one sense, the capacitor voltage will build up indefinitely unless the charge is removed, in this case by resistive dissipation.

The voltage V_{c1} across the capacitor C1 will be increasing and decreasing depending on the action of the converter at that particular time. When any transistor group is ON, the voltage across capacitor C1 will be decreasing, because the capacitor C1 is discharging through resistor R. The capacitor current, i_c will be circulating in the loop containing the resistor R and the capacitor C1.

The charging of the capacitor will take place when no transistor is conducting. This occurs briefly when the gating signal is removed from one transistor group, and fed to the other transistor group, which may not turn ON instantaneously.

4.2.1 NON CONDUCTION IN TRANSISTOR BRIDGE

This brief "blocking" occurs at alternate switchings of the transistor group. The protection ensures that the gating signals will be ON for an overlap time before they are turned OFF. The overlap time is intended to ensure that the transistors which are being turned ON (from their previous

OFF states) will be ON until the other pair are turned OFF. This protection is supposed to provide a current path through the transistors at all times. Unfortunately, the protection is effective only half the time. To appreciate this, first consider the successful half of the time.

4.2.1.1 SUCCESSFUL PROTECTION

This occurs when the transistor T2 of fig.4.2 are initially conducting. With the polarity of the voltage V_{ce} across the ac capacitor C as shown, the OFF transistors T1 are forward biased. Thus when the gate signals are reversed, T1 can turn ON even though T2 are ON.

4.2.1.2 UNSUCCESSFUL PROTECTION

The difficulty occurs in the next stage signal reversal. When T1 are ON, the capacitor voltage V_{ce} reverse biases the transistor T2. As a result , although T2 receive the turn ON gate signals, they cannot turn ON until T1 are fully turned OFF so that the capacitor voltage is effectively disconnected across the collector-emitter terminals of T2. Thus, there always exists a brief period of non conduction to the flow of the dc current in the bridge and the function of the snubber is to provide the alternate path.

4.2.2 ANALYSIS OF SNUBBER CIRCUIT

Fig 4.3 shows the expanded time scale of the voltage

across the snubber capacitor of one phase. In the analysis, the snubber circuit is considered to consists of the ideal diode D1, the capacitor C1 and the resistor R. The analysis is intended to enable C1 and R to be chosen. For economy, C1 should be small. For efficient operation R should be large. The capacitor voltage must not exceed the permissible voltages across the transistors.

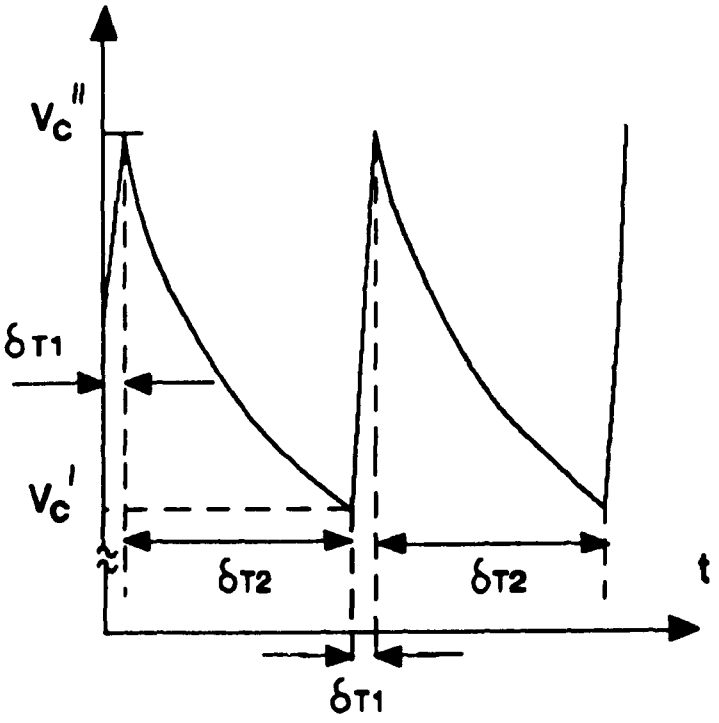


Fig. 4.3 Expanded Time Scale of the Capacitor Voltage

δT1 is the very short period when capacitor C1 is charging (transition time between the turning OFF of one transistor group and the turning ON of the other transistor group). δT2 is the period when capacitor C1 is discharging, this is the time when either of the transistor group is ON.

4.2.2.1 CHARGING CAPACITOR.

When the transistors in the bridge are all blocking in the period $\delta T1$, the capacitor C1 is being charged. Assuming that the resistor R is very large, the dc link current will be circulating in the load and snubber circuit and will be given by:

$$C1 \cdot dV_{c1}/dt = I_{dc} \qquad (4\text{-}1)$$

Integrating eq. (4-1)

$$V_{c1}'' - V_{c1}' = \frac{I_{dc} \cdot \delta T1}{C1} \qquad (4\text{-}2)$$

where: V_{c1}'' = Final charge capacitor voltage

V_{c1}' = Initial capacitor voltage

In general, $\delta T1$ is not exactly known as it is a property of the transistor turn-on and turn-off times. However, it may be estimated from information from the manufacturer's data sheets. The initial capacitor voltage V_{c1}' is here treated as an algebraic unknown to be solved subsequently.

4.2.2.2 DISCHARGING CAPACITOR

The discharging of the capacitor occurs when transistors are conducting, the discharging current circulates in the RC1 circuit. This current can be written as:

$$i_c = C1 \cdot dV_{c1}/dt = -V_{c1}/R \qquad (4\text{-}3)$$

This can in turn be written as:

$$R \cdot C1 \cdot dV_{c1}/dt = - V_{c1}$$

the solution for this equation is:

$$V_{c1} = V_{c1}'' \exp -t/(RC1) \qquad (4\text{-}4)$$

where V_{c1}'' is the initial capacitor voltage.

From Eq.(4-2),

$$V_{c1}'' = V_{c1}' + \frac{I_{dc} \cdot \delta T1}{C1} \qquad (4\text{-}5)$$

At $t = \delta T2$

$$V_{c1}' = V_{c1}'' \exp -\delta T2/(RC1) \qquad (4\text{-}6)$$

At $\delta T2$ it is assumed that V_{c1} has discharged to its initial value.

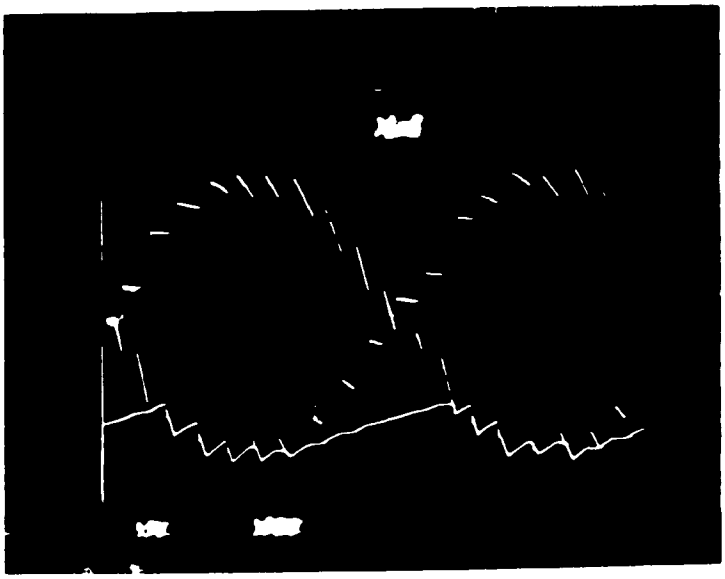
Using Eq.(4-5) and (4-6) to eliminate V_{c1}'', the solution for V_{c1}' is

$$V_{c1}' = \frac{I_{dc} \cdot \delta T1}{C1 \ [\exp \delta T2/(RC1) \ -1]} \qquad (4\text{-}7)$$

$$V_{c1}'' = \frac{I_{dc} \cdot \delta T1}{C1} + V_{c1}' \qquad (4\text{-}8)$$

In using SPWM, $\delta T2$ is not a constant value. It can be estimated as the period of the triangular carrier signal frequency.

For the power bipolar transistor (MJ 10015) it is estimated that $\delta T1$ is in the range of 2-3 microseconds



(a)

(b)

Fig.4.4 (a) The voltage, V_{1a} (b) The voltage, $-V_{c1}$

In the design, V_{c1}' should exceed the amplitude of V_{ca} (the capacitor voltage) so as to assist in turning on the transistors T1 and T2. At the same time, $0.5V_{c1}''$ should

always be less than the permissible collector to emitter voltage of the transistor.

Fig.4.4 shows (from top to bottom) V_{1a}, the voltage across one phase of the converter on the dc side (before the inductor) and the voltage $-V_{c1}$ across the capacitor C1 as taken from the oscillogram.

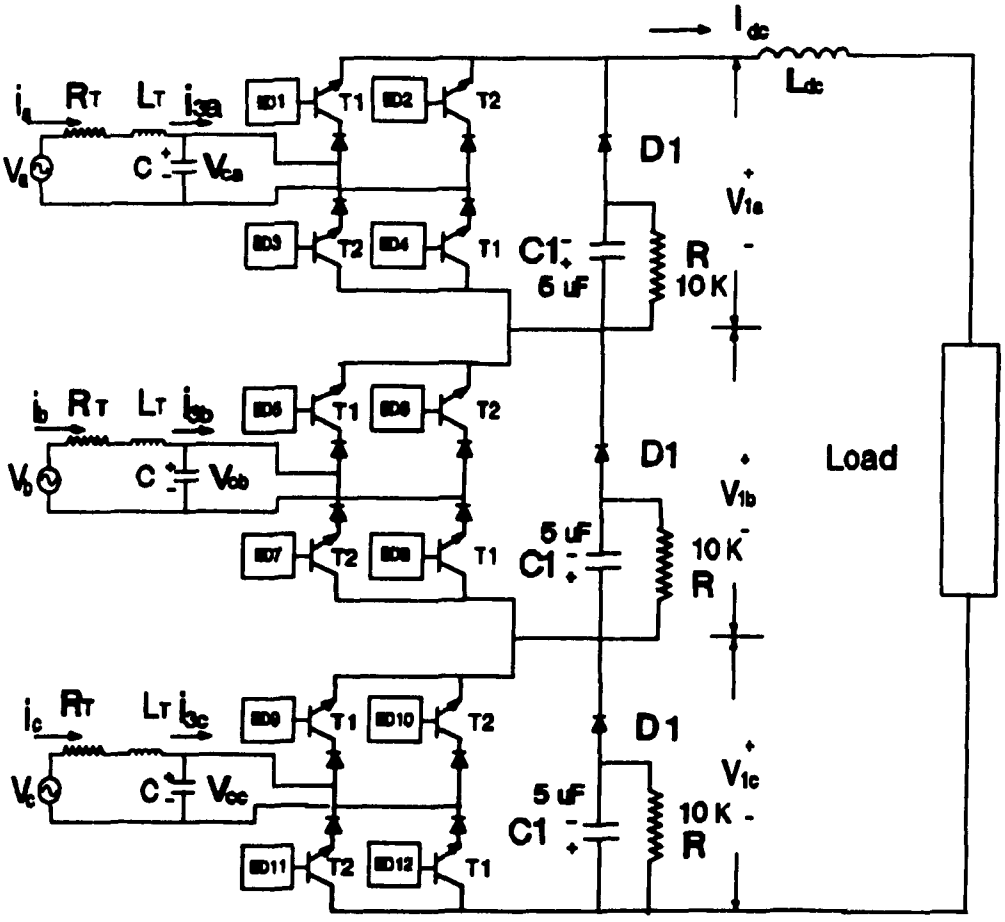


Fig.4.5 A Complete Three Phase Converter with the Snubber Circuit

Fig.4.5 gives a complete three phase circuit diagram of the converter showing the snubber circuit in each phase of the converter.

4.3 SUMMARY

This chapter has presented the dc snubber circuit for protecting the converter against the LdI_{dc}/dt voltage. Analysis of this circuit has been done and its role has been explained. It has also been shown that the choice of the components in this circuit is based on the derived equations and estimation.

The next chapter describes the inner feedback loop, which is used to compensate for the harmonics generated in the resonating ac input circuit. The output of this circuit is also processed in the SPWM logic.

CHAPTER V

THE INNER FEEDBACK LOOP

5.1 INTRODUCTION

The necessity of using an inner feedback loop was recognised after testing the converter. As can be seen in fig.6.2(e) the current waveforms were distorted, and it was noticed that the third and fifth harmonics were present in significant proportions. The sources of these harmonics are believed to originate from: (a) the ac supply voltages, (b) the switching ripples on the dc link current which are transmitted through the outer current regulator feedback loop. The inductance L_f and the capacitance C form a resonating high Q circuit and when the resonating frequency is close to the frequency of the harmonic sources, magnified harmonic currents will flow.

The method that is used to overcome this problem is to use an inner feedback loop which rejects harmonics in the line current. The inner feedback loop measures the line current using a Hall Effect Current Sensor and the SPWM bridge converter is used effectively as a high gain feedback amplifier to null all harmonics except the 60-Hz component. A 60-Hz notch filter in the feedback loop allows the fundamental frequency current to flow without being cancelled.

5.2 LOW HARMONIC DISTORTION

In the stable region of a 1 kw size laboratory model whose parameters are listed in appendix A, the ac current waveform is found to have serious distortions.

In order to understand the sources of this distortions, the ac side of the rectifier is mathematically modelled as shown in fig.5.1, where the transfer functions $W_1(s)$ and $W_2(s)$ are:

$$W_1(s) = \frac{Cs}{L_T Cs^2 + R_T Cs + 1} \qquad (5\text{-}1)$$

$$W_2(s) = \frac{1}{L_T Cs^2 + R_T Cs + 1} \qquad (5\text{-}2)$$

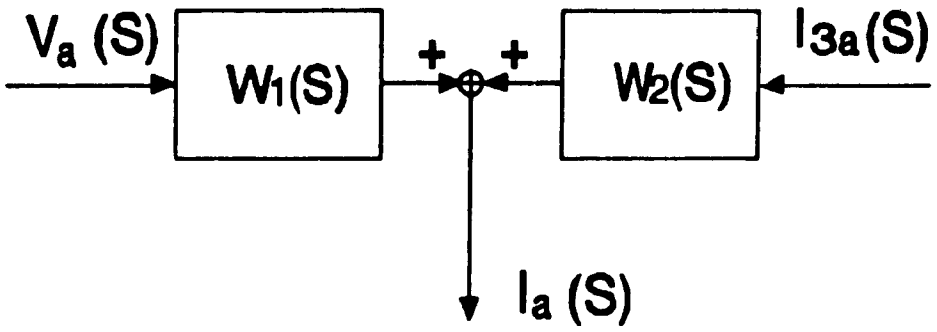


Fig. 5. 1 Block Diagram Showing the a-phase Current $I_a(s)$ in Relation to its Sources V_a (s) and $I_{3a}(s)$

These transfer functions relate the line current $I_j(s)$ to the excitation sources through the equation:

$$I_j(s) = W_1(s)V_j(s) + W_2(s)I_{3j}(s) \qquad (5\text{-}3)$$

where $V_j(s)$ and $I_{3j}(s)$ are the Laplace's Transforms of the ac voltage sources and the rectifier modulated current respectively.

Typically , $V_j(s)$ contains the 3^{rd} and 5^{th} harmonic of the supply frequency arising from the nonlinear characteristics of the transformer iron.

The sources of $I_{3j}(s)$ is traceable from fig.1.4 to $X_m(s)$ and ultimately to $I_{dc}(s)$. The dc current has a perceptible 6^{th} harmonic. The measurement of $I_{dc}(t)$ is by a sample-and-hold, with a sampling rate of twice the triangular carrier frequency. The d/dt in fig.1.4 is performed by digital differentiation on the sample-and-hold signals. Although this mode of data acquisition is free of the switching noise, the 6^{th} harmonic noise becomes magnified by the digital differentiator. When the 6^{th} harmonic components becomes multiplied by $\sqrt{2}\cos\omega t$ and $\sqrt{2}\sin\omega t$, $X_m(s)$ contains significant 5^{th} and 7^{th} harmonics.

Fig.5.2 shows the Bode diagram of $W_1(s)$ as an example, using the system parameters of Appendix A.

The conclusion is that the low harmonic distortion has appeared because the resonant frequency in the L_T - C circuit is too near the 3^{rd} and the 5^{th} harmonic of the

supply and is amplified through eq.(5-1). One remedy is to choose a C whose L_1 - C resonance frequency is remotely located from source frequencies of $V_1(s)$ and $I_{31}(s)$. However, the elements L_1 and C cannot be too small because they must contribute towards filtering the switching harmonics which are near integral multiples of the triangular carrier frequency.

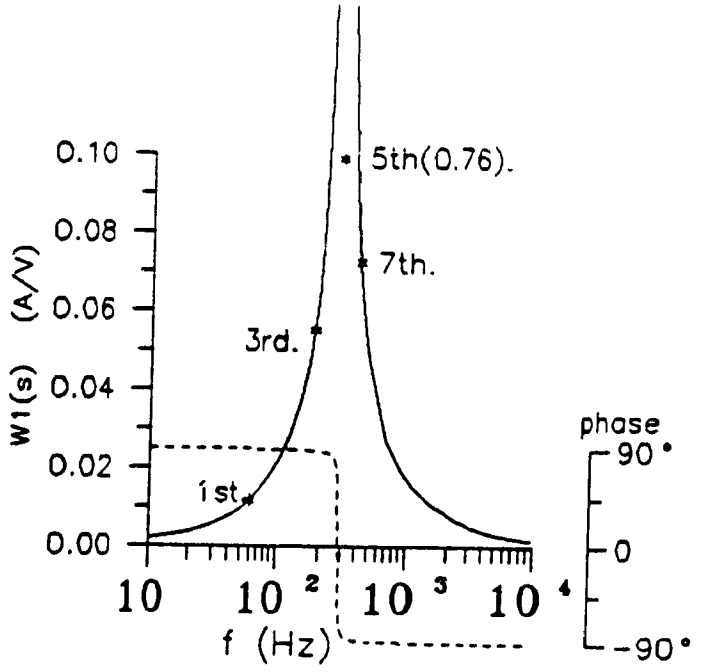


Fig.5.2 Bode Diagram of $W_1(s)$

5.3 LOCAL NOTCH FILTER FEEDBACK

Fig.5.3 shows the local feedback loop which, when introduced into the circuit in fig.1.4, results in the low harmonic distortion being suppressed by active filtering.

There are two elements in the feedback: the feedback gain k_f and the notch filter whose transfer function is $W_f(s)$. This circuit incurs the increased cost of 3 broad band accurate current transducers which are necessary to measure the line current.

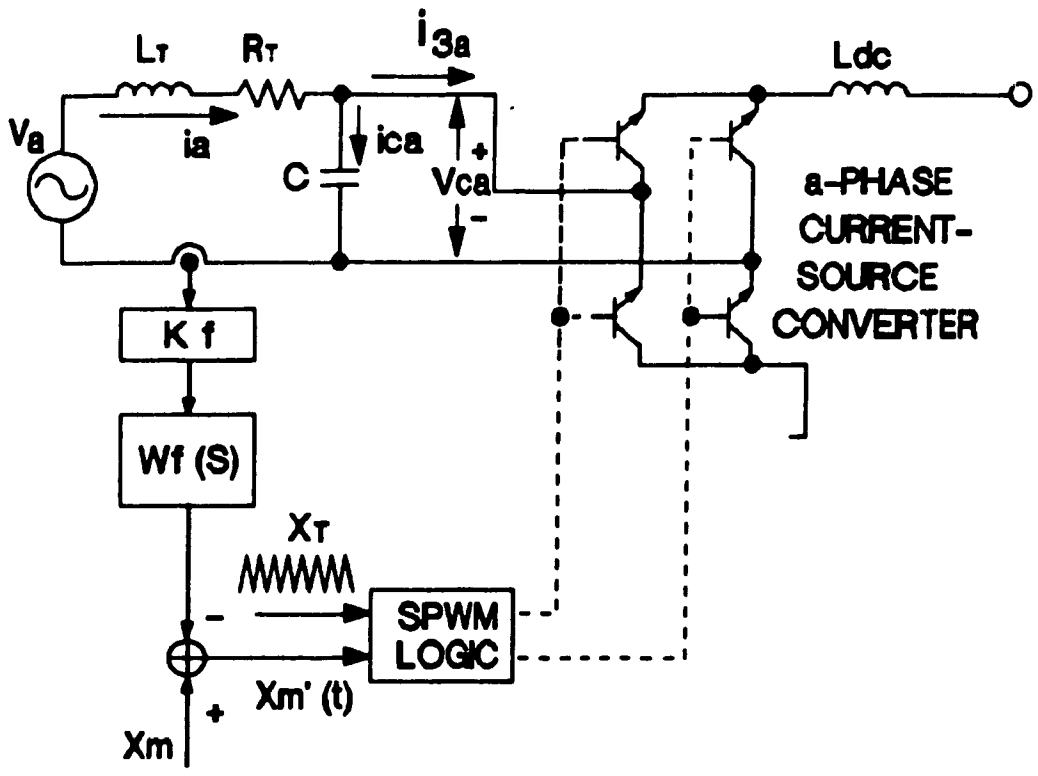


Fig. 5.3 Notch Filter Feedback on One Phase of the Converter

5.4 ACTIVE FILTERING

In incorporating the local feedback, the transfer function of fig.5.1 is modified to those shown in fig.5.4. In order to grasp the essence of the local feedback loop , it is assumed first that the transfer function of the notch filter is unity, i.e.

$$W_f(s) = 1 \qquad (5-4)$$

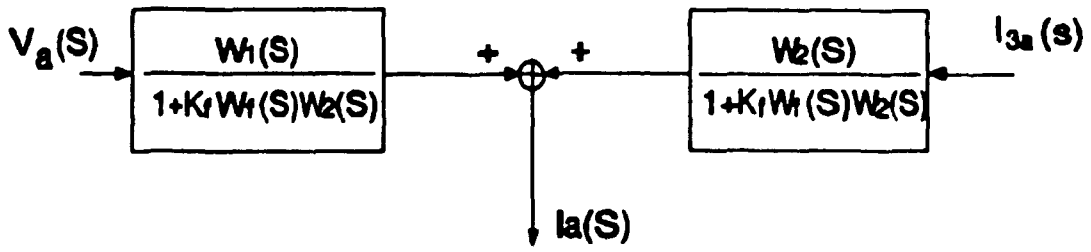


Fig. 5.4 Block Diagram with Transfer Function in Local Notch Filter feedback Loop

In this case, the transfer function $W_1(s)$ say, of eq.(5-1) and fig.5.1, has changed to

$$W_1''(s) = \frac{Cs}{(L_T Cs^2 + 1 + k_f) + R_T Cs} \qquad (5\text{-}5)$$

The resonant frequency has changed from

$$\omega_r = (1/L_T C)^{0.5} \qquad (5\text{-}6)$$

to

$$\omega_r'' = [(1 + k_f)/L_T C]^{0.5} \qquad (5\text{-}7)$$

Thus by using the feedback gain k_f, one can shift the resonant frequency away from those of known harmonic sources without having to tamper with the values of L_T and C.

In the low frequency range,

$$W_1(s) \approx Cs \qquad (5\text{-}8)$$

whereas

$$W_1''(s) \approx \frac{Cs}{1 + k_f} \qquad (5\text{-}9)$$

Thus one conclude that by setting large values of k_f, one reduces the lower order harmonics by a factor of $1/(1 + k_f)$. Unfortunately the attenuation by this local feedback loop would affect the fundamental frequency signal and the design

in fig.1.4 to meet the requirement of unity power factor operation and dc current regulation.

5.5 TWIN-TEE NOTCH FILTER

The objectives in mind are that the characteristics of eq.(5-5), (5-7) and (5-9) are all desirable except that one likes an exemption to be made at the fundamental frequency. At the fundamental frequency, the local feedback should not be there. This wish is incorporated through the use of the twin-tee notch filter [9] whose transfer function is:

$$W_f(s) = \frac{1 + T^2s^2}{1 + 4Ts + T^2s^2} \qquad (5\text{-}10)$$

By choosing T such that the numerator of eq.(5-10) is zero at the supply frequency, then the local feedback loop is virtually disconnected vis-a-vis the supply frequency.

Fig.5.5 shows the Bode diagram of eq.(5-10). The gain in general is unity except in the region of the notch where the gain drops to zero at the notched frequency $f_n = 1/2\pi T$. In general there is no phase shift, except again in the region of the notch where it lags for $f < f_n$ and leads for $f > f_n$. The phase shift does not exceed 90 degrees.

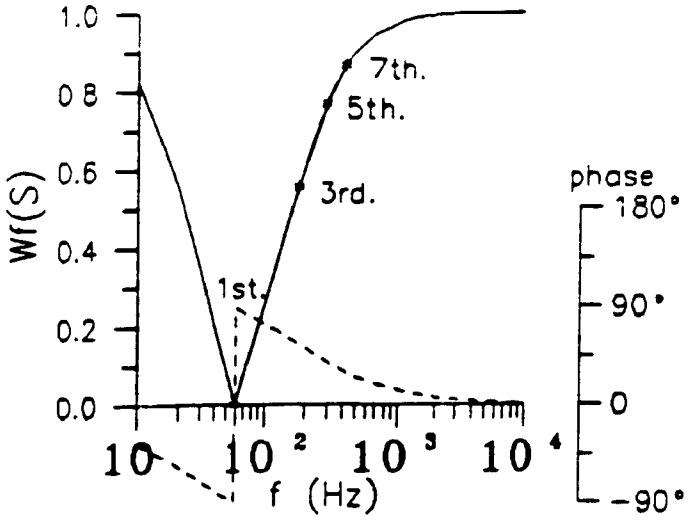


Fig.5.5 Bode Diagram of Twin-Tee Notch Filter

Fig.5.6 shows the Bode Diagram of the transfer function

$$W_1'(s) = \frac{W_1(s)}{1 + k_f W_f(s) W_2(s)} \qquad (5\text{-}11)$$

In fig.5.2 the transfer gains for the 3rd and 5th harmonic are 4.7 and 64.5 A/volt respectively and in fig.5.6

these have been lowered by almost a factor of 10. The feedback gain for fig.5.6 is $k_f = 10$.

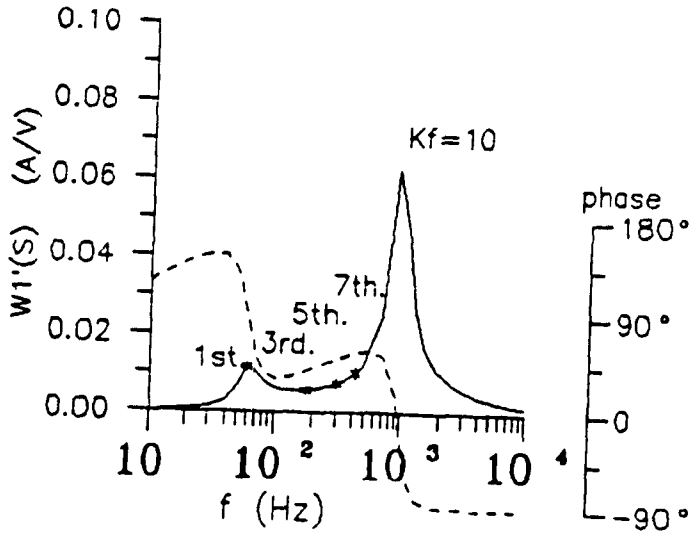


Fig.5.6 Bode Diagram of $W_1'(s)$

Fig.5.7 shows an analog circuit realization of the Twin-tee Notch filter.

5.6 LOCAL FEEDBACK STABILITY

The local feedback with the twin-tee notch filter is always stable. This is evident from the denominator terms (1 + $k_f W_f(s) W_2(s)$) in the transfer function of Fig.5.4. Applying

the Nyquist criterion, the open loop transfer gain $k_f W_f(s) W_2(s)$ never encircles the -1.0 point in the s-plane. This is because the phase shifts of $W_2(s)$ in eq.(5-2) and $W_f(s)$ in eq.(5-10) (see Fig.5.5) never exceed 90 degrees so that their combined phase shift cannot exceed 180 degrees. Without exceeding 180 degrees in phase shift, there is no possibility of encirclement of the -1.0 point. Thus stability is assured by the Nyquist criterion.

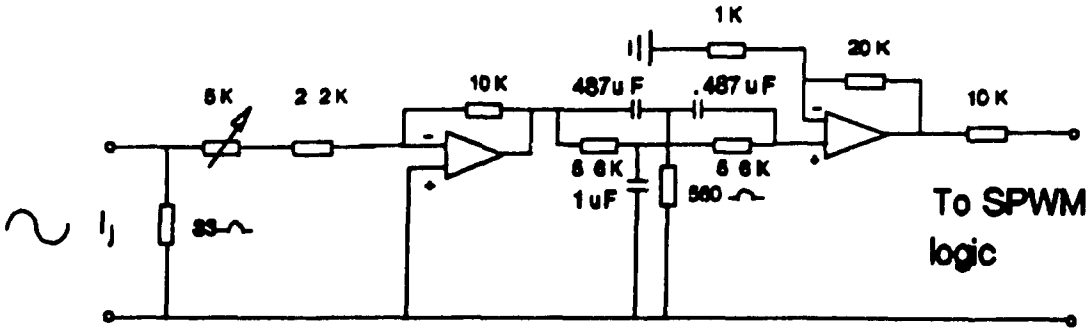


Fig.5.7 The Notch Filter

5.7 SUMMARY

In this chapter sources for low harmonic ac current waveform distortion have been identified. A solution is found by using a simple local notch filter which perform the

job of active filtering to clean up the low order harmonic distortion on the ac side. The photograph of this circuit is shown in appendix B.

The next chapter presents the simulation results of the system with the inner feedback loop. Experimental results with and without the inner feedback loop are also presented.

CHAPTER VI

RESULTS

6.1 INTRODUCTION

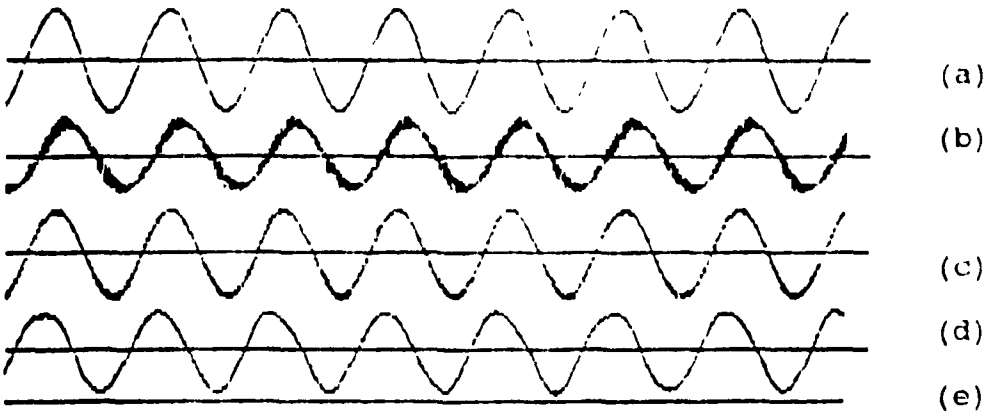
Chapter II described the power circuit of the converter. Chapter III discussed the principles of SPWM technique and the generation of the control signal. Chapter IV described the dc snubber circuit and chapter V presented the inner feedback loop.

This chapter presents computer simulation and experimental results. Experimental test results will cover the operation of the system without and with the inner feedback loop, while the computer simulation results will only consider the system with the inner feedback loop.

6.2 SIMULATION RESULTS

Fig 6.1 shows the simulated waveforms of the system operated at an output voltage V_2 of 100 V_{dc}. The waveforms from top to bottom are: (a) the ac input supply voltage V_j, (b) the modulating signal $X_m(t)$, (c) the ac capacitor voltage V_{cj}, (d) the ac supply current i_j and (e) the dc link current I_{dc}.

The ac supply current is near sinusoidal and almost in phase with the ac input supply voltage.

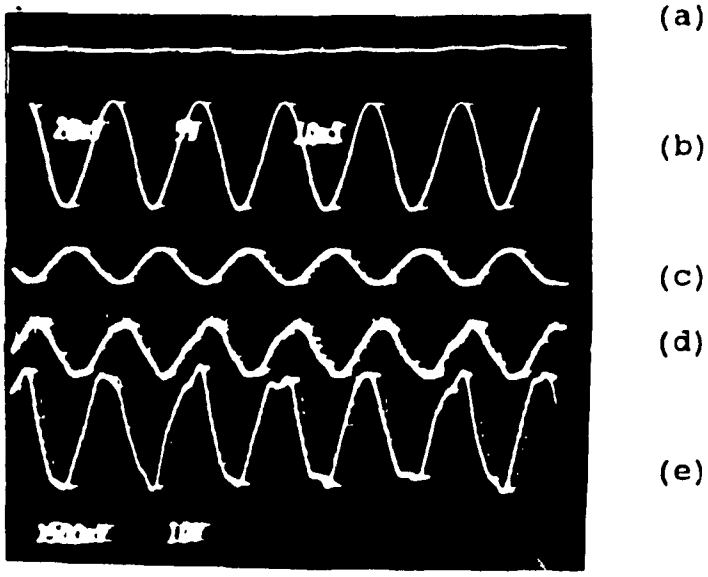


V_j=90V, V_2=100V, I_{dc}=2A, L_{dc}=50mH, C=30μF, I_{REF}=12

Fig.6.1 Simulation results with the inner feedback loop

6.3 EXPERIMENTAL RESULTS

6.3.1 WITHOUT INNER FEEDBACK LOOP



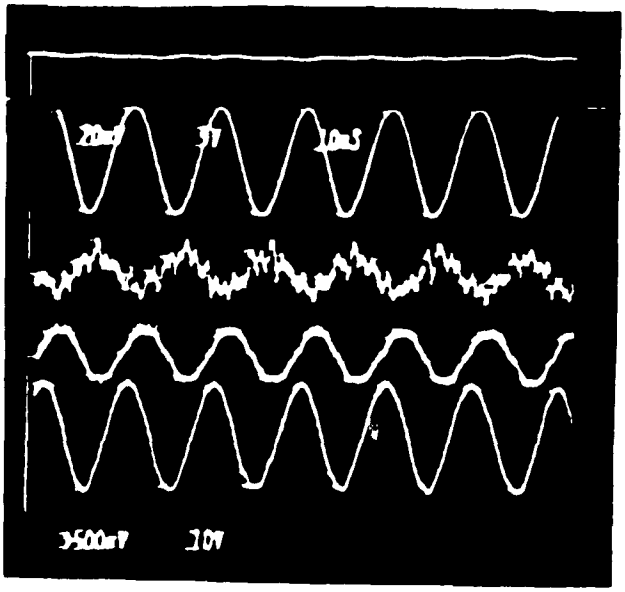
I_{dc}=2A, V_j=50V, V_{cj}=50V, i_j=0.7A, time scale: 10ms/div.

Fig.6.2 Experimental results without the inner feedback loop

Fig 6.2 shows experimental results obtained when the converter is operated without the inner feedback loop. The waveforms (from top to bottom) are: (a) the dc link current I_{dc}, (b) the ac input supply voltage V_j, (c) the modulating signal X_m, (d) the ac capacitor voltage V_{cj} and (e) the input supply current i_j.

It is clearly seen that the waveform of the input supply current is distorted as a result of magnification of the third and fifth harmonics. It is because of these harmonics that an inner feedback loop is included in the system.

6.3.2 WITH INNER FEEDBACK LOOP



(a)

(b)

(c)

(d)

(e)

I_{dc}=2A, V_j=50V, V_{cj}=50V, i_j=0.7A, time scale: 10ms/div

Fig 6.3 Experimental results with the inner feedback loop

Test results with the inner feedback loop are shown in fig 6.3. From top to bottom the waveforms are: (a)the dc link current I_{dc}, (b) the ac input supply voltage V_{ij}, (c) the modulating signal X_m, (d) the ac capacitor voltage V_{cj} and (e) the input supply current i_j.

The input current waveform is near sinusoidal. In both experimental tests the input supply current is in phase with the input supply voltage.

6.4 DISCUSSION OF THE RESULTS

Experimental results have shown that this converter can operate at unity power factor. The converter has also demonstrated the ability to provide near sinusoidal input current waveform. The tests have been done with a resistance load in the circuit. It has been possible to obtain a dc power output close to 1kW with a load resistance of 10 ohms.

An input capacitance of 30 microfarads and a dc inductance of 50 mH have been used in all experimental tests. The input current waveform may still be improved by having larger values of the ac input capacitance, C and dc inductance, L_{dc}. However, this increases the overall cost of the converter. Compromise has to be reached between the cost and the quality of the performance.

6.5 SUMMARY

In this chapter simulation and experimental results have been presented. To some extent the two results agree

with each other. The next chapter presents the conclusion of this thesis and suggestions for further work to be done on this converter.

CHAPTER VII

CONCLUSIONS

7.1 CONCLUSIONS

The objective of the research leading to this thesis has been to construct and test the SPWM current source converter. This research is the continuation of the research program which began with the research on the delta-modulated buck type converter [8]. The evaluation of the converter topology can be found in reference [2,8]. This research is therefore, directed to the evaluation of the SPWM technique in controlling the current source converter and not the evaluation of the topology.

The design of the dc snubber circuit presented in chapter IV has given assurance that there is always a continuous dc current path through all the three single phase bridges. Moreover, this circuit is now successfully and efficiently protecting the switches against the excessive $L_{dc}dI_{dc}/dt$ voltage which occurs during disruption of the flow of this current.

The comparison between the SPWM strategy and other strategies of current source converter control forms part of the research program. Because of the time limit set by the Germany Academic Exchange Scholarship Committee to pursue M.Eng degree, the performance of the SPWM current source converter has not been exhaustively evaluated. There is a

need for more experimental testing to evaluate the reliability of this converter.

The following conclusions can be made so far from the experimental tests which have been done with the SPWM current source converter:

(1) The converter draws near sinusoidal ac input current when the inner feedback loop is included in the control circuit.

(2) The converter is capable of operating at unity power factor.

These attractive features suggest that the system merits a complete evaluation and comparison with other control techniques. However, the need of a broad band current sensor in each phase of this system continue making this type of converter much more expensive.

7.2 SUGGESTIONS FOR FURTHER WORK

A further investigation has to be carried out before the final decision on merits and deficiencies is made. The following work is suggested :

(1) Research in the operation of the system as an inverter. This was one of the goals at the beginning of this research, but due to the time limit it has not been possible to test this converter in four quadrant mode. However, the inclusion of the dc snubber circuit presented in chapter IV will make this operation possible.

(2) Translating the need for active filtering in this

type of converter to the more economical 6 valve 3-phase parallel bridge.

APPENDICES

APPENDIX A:

CONVERTER PARAMETERS

	real values	p.u. values
V_T	90V	1.0
R_T	0.6Ω	0.025
ωL_T	3.7Ω	0.152
$1/\omega C$	88.4Ω	10.9
L_{dc}	50mH	0.775
R_{dc}	0.5Ω	0.02

V_{BASE} = 90 V P_{BASE} = 1000 W Z_{BASE} = 24.3 Ω

C = 10 microfarad

APPENDIX B:

PHYSICAL CONSTRUCTION OF THE CONVERTER

Fig.B.1 shows the photograph of the circuit implementing the modulating signal $X_m(t)$. This circuit was constructed on the bread board.

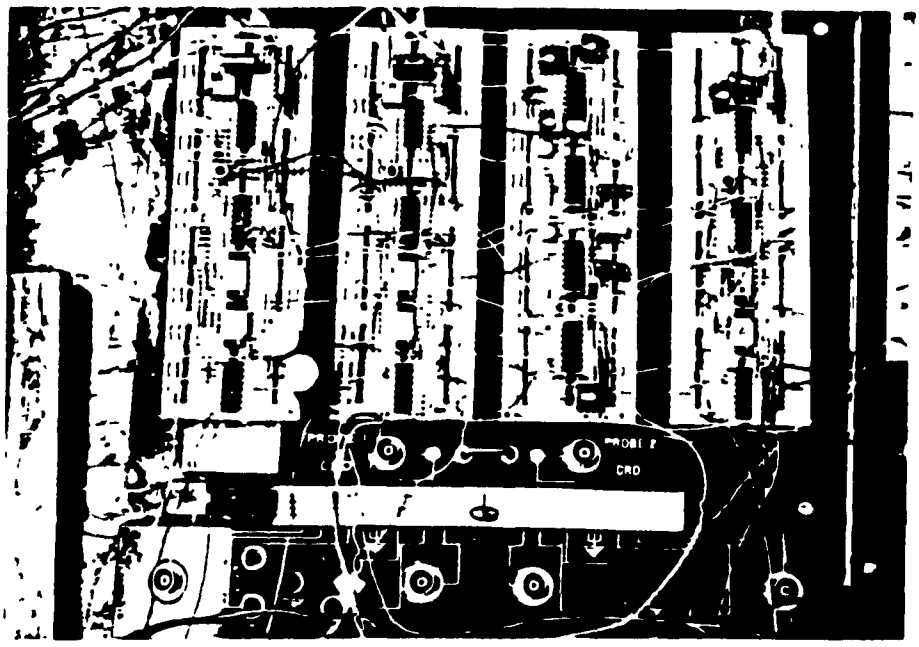


Fig.B.1 Implementation of the Modulating Signal

Fig.B.2 is the photograph of the Local Notch Feedback Filter together with the circuit implementing the Carrier Signal. These circuits were also made on the bread board.

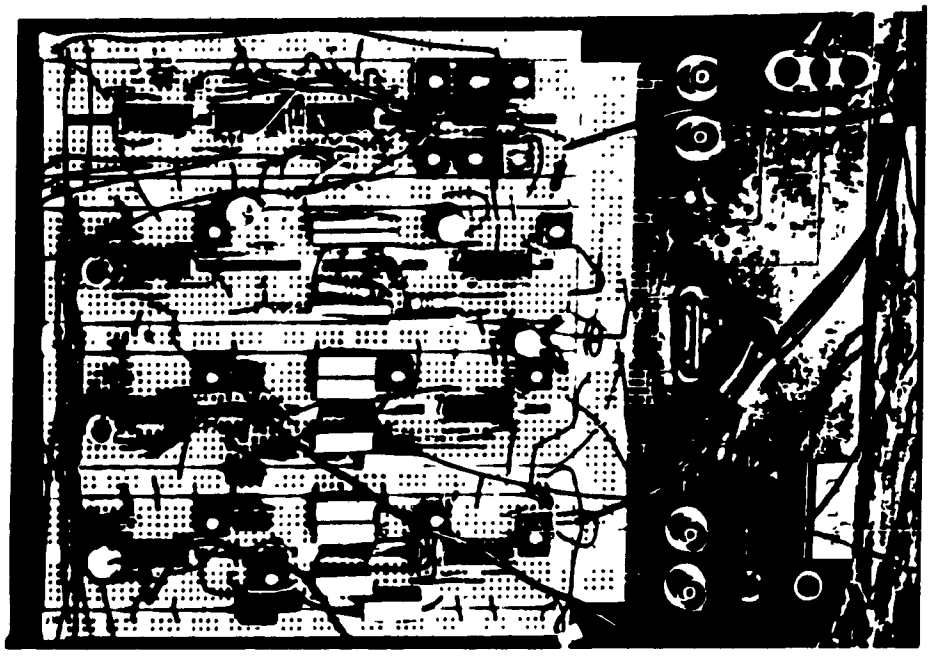


Fig.B.2 Implementation of the Local Notch Filter and the Carrier Signal

The rest of the circuits have been constructed on printed circuit boards. Fig.B.3, B.4 and B.5 shows the view of one phase of the converter from different directions.

In Fig.B.3 the two Power Bipolar Transistor are seen mounted on the heat sink on one leg of the single phase converter. The power connections are also seen in this photograph.

Fig.B.4 is also one leg of the single phase converter showing the snubber circuit and the base drive unit.

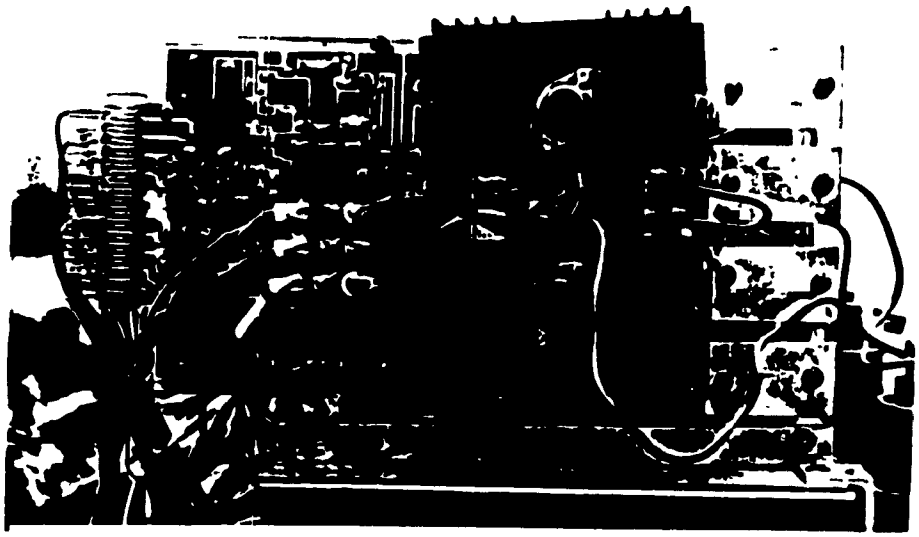


Fig.B.3 One Leg of the Single Phase Converter Showing the Power Bipolar Transistor and the Power Connections

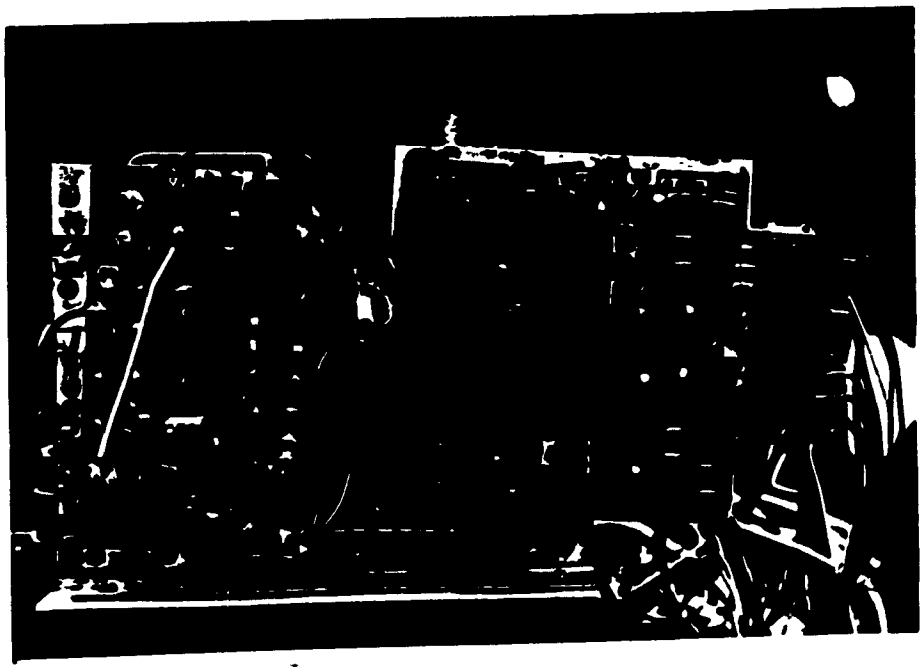


Fig.B.4 One Leg of the Single Phase Converter Showing the Snubber Circuit and the Base Drive Unit

Fig.B.5 is the complete single phase converter. A high frequency snubber capacitor is seen mounted on one leg of the single phase converter.

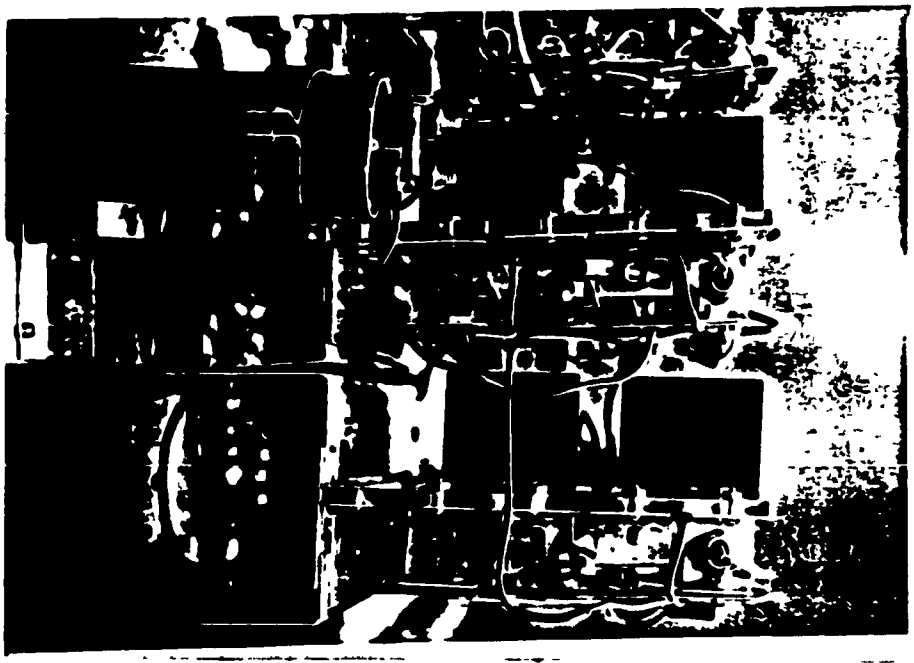


Fig.B.5 The Arrangement of One Phase of the Current Source Converter

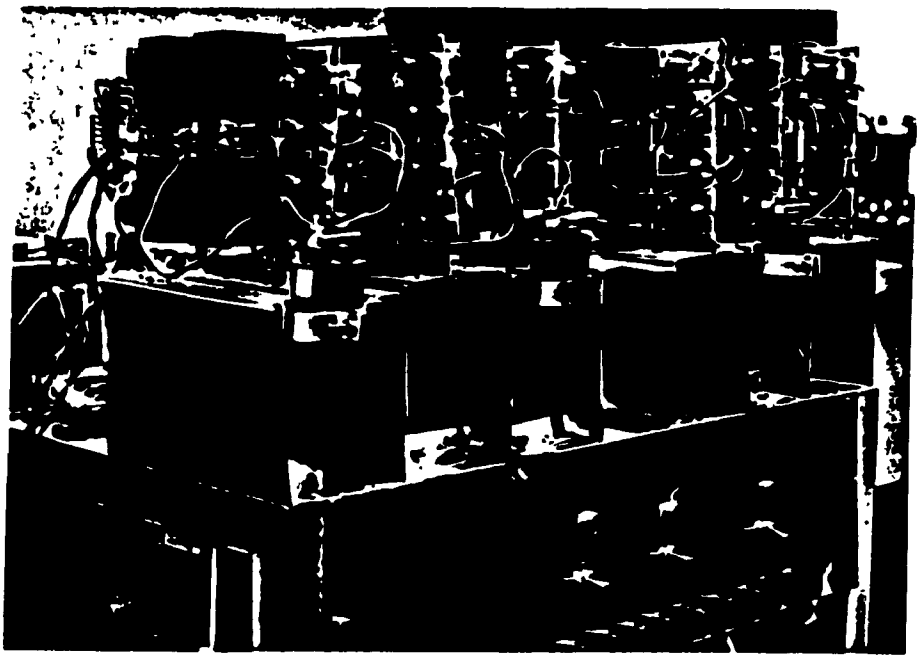


Fig.B.6 The Complete SPWM Current Source Converter

APPENDIX C:

POWER BIPOLAR TRANSISTOR DATA SHEET

MJ10015
MJ10016

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE EMITTER SPEEDUP DIODE

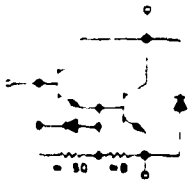
The MJ10015 and MJ10016 Darlington transistors are designed for high voltage, high speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

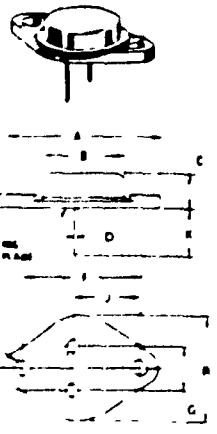
- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 1.0 µs (max) Inductive Crossover Time – 20 Amps
  - 2.5 µs (max) Inductive Storage Time – 20 Amps
- Operating Temperature Range – 65 to +200°C
- Performance Specified for
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

50 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

400 and 500 VOLTS
250 WATTS





STYLE 1
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	8.26	9.14	0.325	0.360
D	1.65	1.90	0.065	0.075
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	3.21	3.77	0.126	0.148
J	17.64	17.91	0.695	0.705
K	11.18	12.19	0.440	0.480
R	3.84	4.09	0.151	0.161
S	26.39	26.67	1.039	1.050

CASE 197-01
MODIFIED TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector Emitter Voltage	$V_{CEO(sus)}$	400	500	Vdc
Collector Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	50 75		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10015 MJ10016	$V_{CEO(sus)}$	 400 500	 – –	 – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)		I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{s/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 8			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc) (I_C = 40 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 25 10	 – –	 – –	–
Collector Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	 – –	 – –	 2.2 5.0	Vdc
Base Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)		V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	–	–	750	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs, Duty Cycle ≤ 2%)	t_d	–	0.14	0.3	μs
Rise Time		t_r	–	0.3	1.0	μs
Storage Time		t_s	–	0.8	2.5	μs
Fall Time		t_f	–	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

(2) The internal Collector to Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

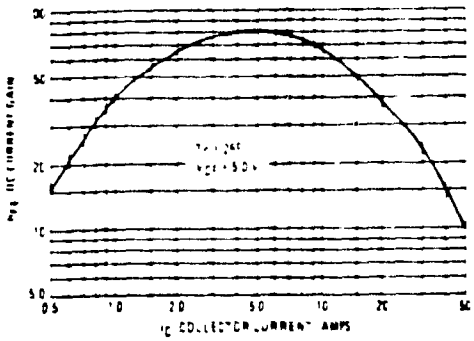


FIGURE 2 – COLLECTOR EMITTER SATURATION VOLTAGE

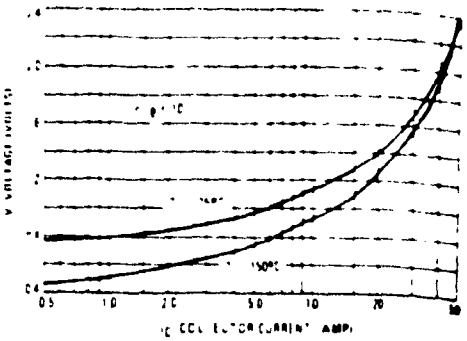


FIGURE 3 – BASE EMITTER SATURATION VOLTAGE

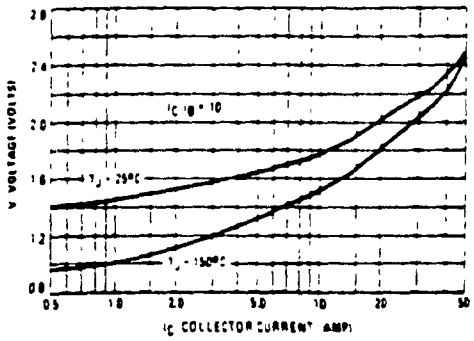


FIGURE 4 – COLLECTOR CUTOFF REGION

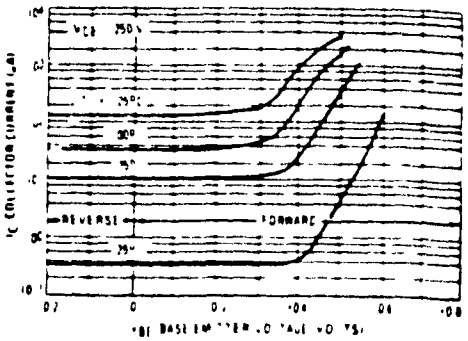


FIGURE 5 – OUTPUT CAPACITANCE

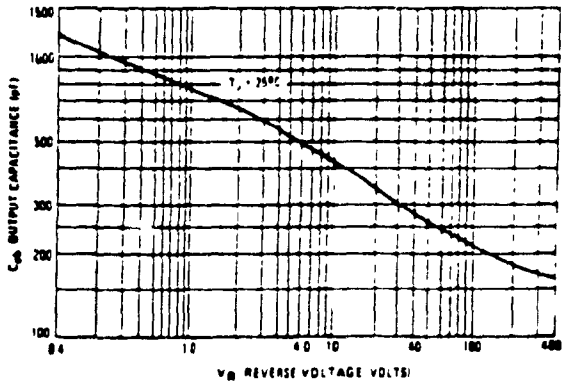
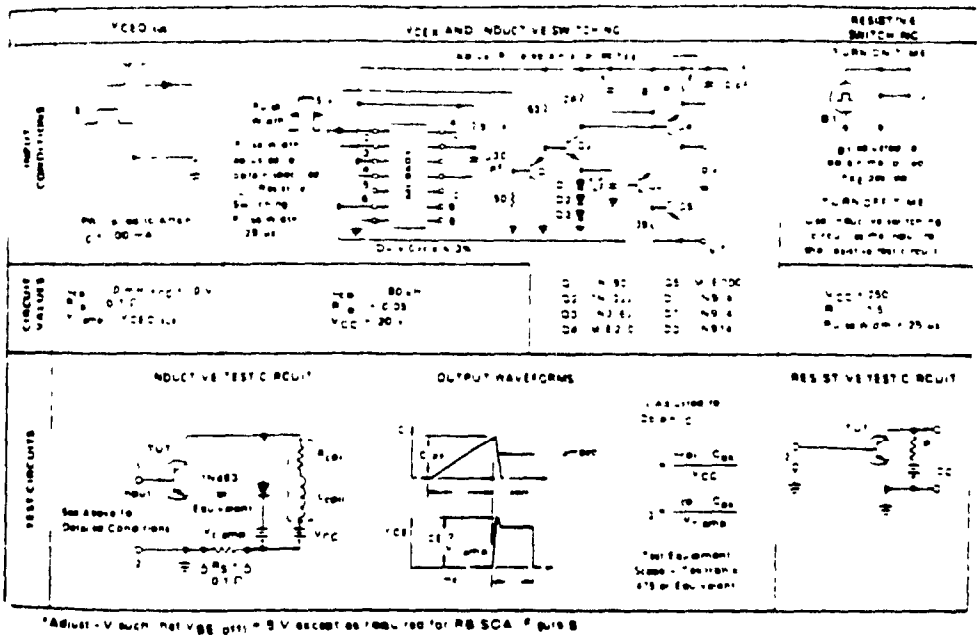
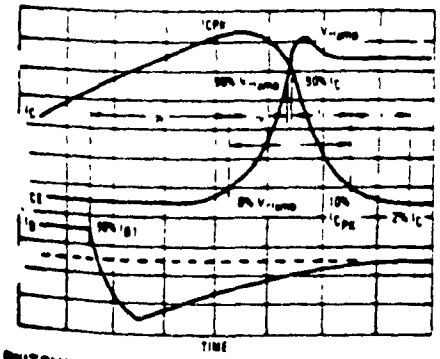


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust – V such that $V_{BE(off)}$ = 9 V except as required for RBSOA. Figure 8

FIGURE 6 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits rise, fall and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10 – 90% V_{clamp}
t_{fi} = Current Fall Time, 90 – 10% I_C
t_{ti} = Current Tail, 10 – 2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN 222.

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a SWITCHMODE transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figure 7 and 8 are specified ratings for these devices under the test conditions shown.

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

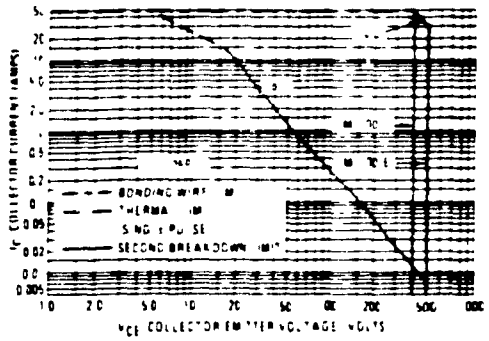
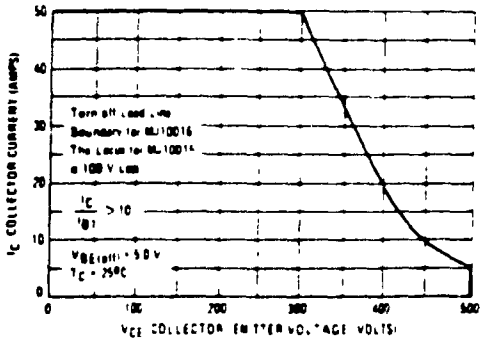


FIGURE 8 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

FIGURE 9 – POWER DERATING

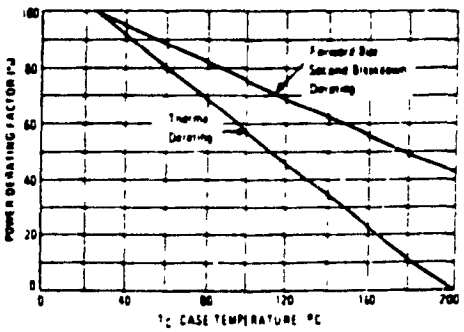
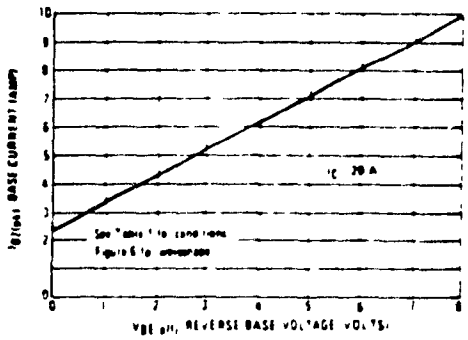


FIGURE 10 – TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



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