On route to infinite gain CMOS Operational Transconductance Amplifiers and its impact on speed and capacitive load drivability of closed-loop analog applications

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بسم الله الرحمن الرحيم

In the Name of Allah the Most Gracious, the Most Merciful

(نَرْفَعُ دَرَجَٰتٍ مَّن نَّشَآءُ، وَفَوْقَ كُلِّ ذِى عِلْمٍ عَلِيمٌ)

[القرآن الكريم، سورة يوسف، آية:76]

"We elevate in rank whoever We will. But above those ranking in knowledge is the One All-Knowing"

Translation of the meaning of the Noble Quran by Dr. Mustafa Khattab, `The Clear Quran`

[Surat Yusuf – Chapter 12, Verse 76]

Dedication

To the memory of my father Dr. Abdullah Al-Totonchi (May Allah have mercy on him)

To my mother, the one and the only, Nada Hamudat

To my brothers Omar, Ali, Mohammed, and Ibrahim

To my wife Dr. Alyaa Habeeb

To my son Hamzah

To my nephews & nieces: Abdullah, Abdulrahman, Sara, Leen, Sali, and Ali

Acknowledgments

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List of Acronyms

ADC	Analog-to-Digital Converters
$A_{DC,N}$	Overall DC Gain
AC	Alternating Current
Anti-PSA	Anti-Pole Splitting Approach
APC	Active Parallel Compensation
CAD	Computer Aided-Design
C_L	Load Capacitor
CMFB	Common Mode Feedback
CMOS	Complementary-Metal-Oxide-Semiconductor
CS	Common Source
DC	Direct Current
dB	Decibels
FCTs	Frequency Compensation Techniques

FOM	Figure-of-Merit
HF	High Frequency
GBW	Gain-Bandwidth Product
IC	Integrated Circuits
IM	Improvement Metric
LCD	Liquid Crystal Display
LDO	Low-Dropout
LF	Low Frequency
LHP	Left Half-Plane
MC	Monte Carlo
MEMS	Micro-Electromechanical Systems
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMC	Nested-Miller compensation
OTAs	Operational Transconductance Amplifiers
PCB	Printed Circuit Board
PID	Proportional Integral Derivative
PM	Phase Margin
PSA	Pole-Splitting Approach
P-Z	Pole-Zero
P-ZC	Pole-Zero Cancellation Approach

PVT	Process, Voltage, and Temperature
RHP	Right Half-Plane
SR	Slew-Rate
TF	Transfer Function
T_S	Settling Time
TSMC	Taiwan Semiconductor Manufacturing Company
V_{DD}	Supply Voltages
V_{in}	Input Voltage
V_{OUT}	Output Voltage

Abstract

This thesis introduces a many-stage CMOS Operational Transconductance Amplifiers (OTAs) design technique that allows cascading identical gain stages (for arbitrarily scalable ultra-high DC gain) while driving an ultra-wide range of capacitive loads (C_Ls). At the heart of the proposed design technique, is a new generalized theory on the relationship between frequency response and settling time of CMOS OTAs in the presence of Pole-Zero (*P-Z*) pairs (or doublets). Interestingly, the presence of *P-Z* pairs/doublets in the open-loop frequency response of CMOS OTAs has always been considered detrimental to the closed-loop operation of CMOS OTAs. However, the new proposed theory is showing how to reduce the impact of such *P-Z* pairs on the closed-loop operation of CMOS OTAs - using low-frequency zeros and cascaded-gain stages – consequently revealing untapped opportunities for many-stage CMOS OTA design. The proposed scalable design of the many-stage CMOS OTA ensures stability, when configured in closed loop, by means of a new frequency compensation technique that relies on low-frequency left-half-plane zeros to allow the proposed OTA to operate for a desired closed-loop behavior.

The proposed design realizes a CMOS OTA with scalable-gain that increases in 25 dB increments per stage, achieving a total gain from 50 dB to 200 dB for a 2-stage to an 8-stage

configuration, respectively. The design is verified through extensive simulations based on a standard TSMC 65 nm CMOS process. Also, as a proof-of-concept, the design has been validated by fabricating 2-, 3-, and 4-stage CMOS OTAs, and the measurement results show that the 2-stage OTA is achieving a DC gain of 50 dB with a C_L-drivability ratio of 10,000x, the 3-stage OTA is achieving a DC gain of 70 dB with a C_L-drivability of 1,000,000x, and the 4-stage OTA is achieving a DC gain of 90 dB with a C_L-drivability of 1,000,000x. This is a 10-to-1000-time improvement in the state-of-the-art.

Résumé

Cette thèse présente une technique de conception d'amplificateurs à transconductance opérationnelle (OTA) CMOS à plusieurs étages qui permet de mettre en cascade des étages de gain identiques (pour un gain en courant continu (CC) ultra-élevé arbitrairement évolutif) tout en pilotant une gamme ultra-large de charges capacitives (C_L). Au cœur de la technique de conception proposée, se trouve une nouvelle théorie généralisée sur la relation entre la réponse en fréquence et le temps d'établissement des OTA CMOS en présence de paires (ou doublets) Pôle-Zéro (P-Z). Fait intéressant, la présence de paires/doublets P-Z dans la réponse en fréquence en boucle ouverte des OTA CMOS a toujours été considérée comme préjudiciable au fonctionnement en boucle fermée des OTA CMOS. Cependant, la nouvelle théorie proposée montre comment réduire l'impact de ces paires P-Z sur le fonctionnement en boucle fermée des OTA CMOS - en utilisant des zéros basse fréquence et des étages de gain en cascade - révélant ainsi des opportunités inexploitées pour le design des OTA CMOS à plusieurs étages. La conception évolutive proposée de l'OTA CMOS à plusieurs étages assure la stabilité, lorsqu'il est configuré en boucle fermée, au moyen d'une nouvelle technique de compensation de fréquence qui repose sur des zéros du demi-plan gauche basse fréquence pour permettre à l'OTA proposé de fonctionner en boucle fermée comme souhaitée.

La conception proposée réalise un OTA CMOS avec un gain évolutif qui augmente par incréments de 25 dB par étage, atteignant un gain total allant de 50 dB à 200 dB pour une configuration allant de 2 étages à 8 étages, respectivement. La conception est vérifiée par des simulations approfondies basées sur le processus CMOS 65 nm standard de TSMC. De plus, en tant que preuve de concept, la conception a été validée en fabriquant des OTA CMOS à 2, 3 et 4 étages, et les résultats des mesures montrent que l'OTA à 2 étages atteint un gain CC de 50 dB avec un rapport de maniabilité C_L de 10 000x, l'OTA à 3 étages atteint un gain CC de 70 dB avec une maniabilité C_L de 1 000 000x, et l'OTA à 4 étages atteint un gain CC de 90 dB avec une maniabilité C_L de 1 000 000x. Il s'agit d'une amélioration de 10 à 1000 fois dans l'état de l'art.

CHAPTER 1

INTRODUCTION

Complementary-Metal-Oxide-Semiconductor (CMOS) Operational Transconductance Amplifiers (OTAs) are at the core of analog and mixed-signal circuits. Since the 1960's, enormous works in literature have been devoted to discussing their applications, requirements, limitations and design techniques. This thesis adds to these works by revealing untapped opportunities to cascade many-gain stages, and realizing a scalable ultra-high DC gain CMOS OTAs with ultra-wide capacitive-load drivability. This proposed OTA design is suitable for a wide-range of closed-loop analog applications. At the heart of this thesis, a new fundamental theory on the impact of left-half-plane low-frequency zeros on the closed-loop step response of CMOS OTAs is introduced for the first time.

This chapter gives a background regarding the design of multi-stage CMOS OTAs. It also highlights the motivation behind the work presented in this thesis. A number of research objectives are set and defined, and an overview of the thesis is presented. Finally, a summary of the main contributions along with a list of derived publications from this thesis are presented.

1.1. Background

Over the past decades, the CMOS technology nodes have been reduced dramatically and beyond expectations. This dramatic reduction in the technology nodes raised some real challenges in the design of analog microelectronics circuits. These challenges are directly related to the reduction in supply voltages (V_{DD}) and transistor dimensions in advanced nanometer scale CMOS technology nodes. Since CMOS OTAs are at the core of analog and mixed-signal circuits, and despite all efforts in designing them, OTAs are still facing challenges when it comes to meeting the design requirements of modern analog and mixed-signal applications, such as achieving high DC gain.

Accordingly, recent design efforts have been focused on proposing different techniques and topologies to overcome the limitations of scaled-down CMOS technologies on OTA design. These proposed designs in literature can be categorized as belonging to one of the two deep-rooted fundamental approaches [1]: (1) cascoding or stacking of transistors on the top of each other, and (2) cascading multiple stages of OTAs in series.

The cascoding approach is limited by headroom issues related to the maximum allowable supply voltage in the modern scaled-down technologies. Consequently, cascading gain stages is the preferred method to achieve sufficient DC gain in modern CMOS technology processes operating with low voltage supply levels. Fig. 1.1(a) shows the cascading scheme of N gain-stages, where in such scheme, the overall DC gain ($A_{DC,N}$) is the gain multiplication of each individual stage, i.e.,

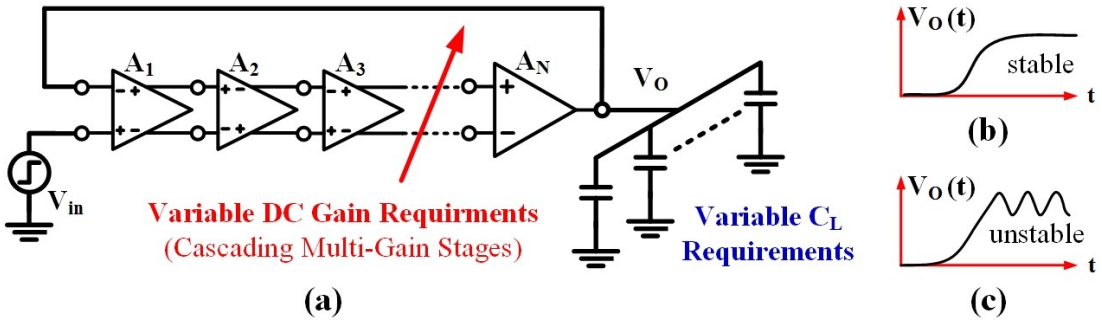

Fig. 1.1: (a) The proposed topology of cascading many-stage CMOS amplifiers while driving a wide range of C_Ls in closed-loop configuration, (b) stable closed-loop time response, and (c) unstable closed-loop time response.

$$A_{DC,N} = \prod_{i=1}^{N}(A_i) \quad , \tag{1.1}$$

where *Ai* is the gain provided by the i^{th} gain stage and *N* is the number of stages. Interestingly, the DC gain requirements are not only varying between different applications, but they are also varying for the same application. For example, in Analog-to-Digital Converters (ADCs), the OTA is required to provide a DC gain of 50 dB for a 6-bit resolution [2], while a DC gain of 150 dB is required to achieve a 32-bit resolution [3]. Therefore, cascading different numbers of gain stages is required to achieve these variable DC gain requirements.

Ultimately, such OTAs are configured in a closed-loop negative-feedback as seen in Fig. 1.1(a), where the output voltage (V_O) must remain bounded within specific values while achieving the desired closed-loop behavior (i.e., V_O(t) must exhibit a stable response as seen in Fig. 1.1(b)). However, such an intuitive systematic approach of cascading gain stages has greatly been limited by stability issues that arise when implementing multi-stages OTAs in closed-loop

feedback configurations [4]. In other words, once cascading many gain stages, $V_O(t)$ becomes a subject to oscillation in closed-loop configuration (i.e., exhibits unstable response as seen in Fig. 1.1(c)).

According to control systems, the source of instability in unity-gain closed-loop negative-feedback systems is the significant increase in phase shift that might occur around the loop such that it becomes a positive feedback system [5]. This significant increase in phase shift can be controlled by proper positioning of the system`s poles and zeros in open loop. Therefore, to ensure stability, different Frequency Compensation Techniques (FCTs) have been proposed in the literature. The main goal of these FCTs is to position the OTA`s poles and zeros according to a specific pattern (as will be discussed in chapter 2) to prevent the oscillation once the OTA is configured in a closed loop.

In addition to adequate DC gain and stable response requirements, modern analog applications have a set of different requirements that the CMOS OTAs must also satisfy. Driving a wide range of Capacitive Loads (C_L) (i.e., in the range of pF-to-μF) is one of these well-known requirements, and it is referred to by C_L-drivability ratio, which can be written as

$$C_{L-drivability} = \frac{C_{L,max}}{C_{L,min}} \quad , \tag{1.2}$$

where $C_{L,max}$ and $C_{L,min}$ are the maximum and minimum C_L, respectively, that the OTA can handle without having stability issues. For example, in parallel Integrated Circuits' (ICs) testing (i.e., Burn-in IC testing [6]), OTAs are required to drive different C_Ls based on the number of devices under testing, which can vary from pF- to μF-range. In some other applications, OTAs

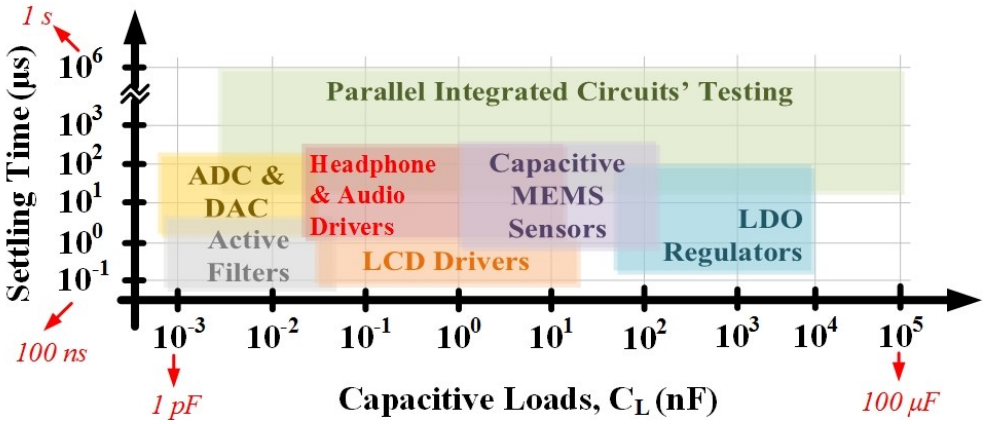

Fig. 1.2: Applications' examples where a wide-range of C_Ls are being driven by CMOS amplifiers and the approximated range of settling time requirements for these applications as a function of C_L.

are required to drive a C_L in the range of pF as in data converters [2, 7] and active filters [8], a C_L up to 22 nF as in headphone and Audio drivers [9]-[11], a C_L of 1.2 nF as in (Liquid Crystal Display) LCD drivers [12], a C_L up to 10 nF as in capacitive Micro-Electromechanical Systems (MEMS) sensors and DNA sensing [13, 14], a C_L up to 10 µF as in Low-Dropout (LDO) regulators [15]-[17], etc.

Moreover, the OTAs are required to achieve a desired speed (i.e., settling time) while driving such C_L in these different applications. To illustrate this, the approximated settling time requirements (i.e., speed) vs. C_L of the previously mentioned applications [2, 6-17] can be seen in the shaded areas of Fig. 1.2. Other important parameters are also required, such as OTA's power consumption, silicon area, input-referred noise, slew rate, etc. Interestingly, all these parameters are affected by the DC gain requirements and designers' choices for the FCTs.

1.2. Motivation

Clearly, cascading gain-stages to design CMOS OTAs is the preferable method to achieve adequate DC gain values in modern analog applications. However, looking at the advancements that have been made in designing multi-stage CMOS OTAs, one can observe the following:

1. Apart from a single exception of a 5-stage OTA in [18], the maximum number of cascaded OTA stages found in the literature has been limited to 4-stages [19]-[24]. Nonetheless, the design in [18] consumes high power (~10 mW) and introduces unusual levels of overshoot in the transient response of the system, while the designs in [19]-[24] are only customized for large capacitive loads (i.e., nF-range), making their FCTs unsuitable to be systematically expanded to higher stages or for driving small loads.
2. Other conventional FCTs in the literature are only suitable for single, 2-, and 3-stage OTAs (as will be discussed in chapter 2) and they are all based on limiting the frequency range of operation to ensure stability when configured in closed loop. Interestingly, limiting the frequency range of operation (to ensure stability) means wasting the extra frequency range that is being offered once using the modern scaled-down CMOS technologies. In other words, although we have a reduction in V_{DD} and transistors' dimensions in modern scaled-down technologies, the frequency range of operation is increasing due to the reduction in the parasitic capacitance. This means that the parasitic poles are allocated at higher frequencies and the value of unity-gain bandwidth (ω_t) can be increased.

3. Despite the need for an OTA to handle pF-to-uF range C_Ls (as depicted from Fig. 1.2), the maximum C_L-drivability ratio that has been reported to date (with the available FCTs) is 1000× [25].

Consequently, the available FCTs seem to have serious challenges when it comes to ensuring the stability of such cascading techniques while driving a wide range of capacitive loads. In the light of these previously mentioned challenges to meet the different requirements of modern analog applications, there remains to be a pressing need for an OTA design that maintains stability in closed-loop applications while enabling the cascade of many OTA gain-stages. Also, such OTA design is required to drive a wide range of capacitive loads to be suitable for a wide range of applications. This work addresses such a need through proposing a new fundamental theory that reveals untapped opportunities to cascade many-gain stages and significantly increase their C_L-driveability ratio.

1.3. Research Objectives and Thesis Scope

This thesis addresses the following research question:

- *Ideally, can we cascade infinite gain-stages to design CMOS OTAs with infinite DC gain?*

Since the main challenge in cascading gain-stages is stability, and since infinite DC gain OTAs have no practical application in analog design, the above research question can be narrowed down to:

- *Is there an FCT that can ensure stability of CMOS OTAs' closed-loop step-response regardless of the number of gain stages?*

As mentioned earlier, the main goal of FCTs is to position the OTA's poles and zeros such that the OTA is exhibiting a stable closed-loop step-response, hence, a prerequisite to finding a solution is to answer the following two questions:

1- *Is there an arrangement of the OTA's poles and zeros that will prevent the OTA closed-loop response from entering the instability region regardless of the number of gain stages?*
2- *What is the impact of such an arrangement on the speed and C_L-drivability of CMOS OTAs?*

Therefore, the objective of this thesis is to answer these questions by, first, investigating the available arrangements of poles and zeros and their impact on the closed-loop step response of CMOS OTAs. Once defining the proper positioning of poles and zeros such that stability is almost unconditionally ensured, a new FCT will be introduced. Accordingly, cascading many-stage CMOS OTAs can become a reality. Also, this thesis will investigate the impact of this new arrangement of poles and zeros on the C_L-driveability and the speed of the proposed CMOS OTAs.

1.4. Thesis Overview and Structure

This thesis is organized as follows:

- Chapter 2 gives a brief background on the concept of cascading multi-stages CMOS OTAs. Also, it discusses the previously-reported works on the design of multi-stage CMOS OTAs. To easily discuss these previously-reported works, this chapter will be divided based on the number of cascaded-gain stages (i.e., 2-stage, 3-stage, and 4-stage). For each number of stages, the available FCTs will be briefly discussed and the maximum C_L-drivability will be reported. This chapter will highlight the different arrangements of poles and zeros in these previously-reported FCTs. On doing so, a certain arrangement of poles and zeros will be pointed-out as a potential candidate to allow cascading many-stage CMOS OTAs. This arrangement is called: the Pole-Zero (*P-Z*) Pair or the *P-Z* Doublet. Interestingly, the presence of an open-loop *P-Z* pair (or doublet) has always been considered detrimental to the settling time of CMOS OTAs. Nevertheless, it will be a subject of investigation in Chapter 3.
- Chapter 3 starts by revisiting the well-established analysis on the relationship between frequency response and settling time of CMOS OTAs having one pole-zero pair (or doublet). Then this relationship, having one *P-Z* pair, will be studied to overcome the limitations of the previously-reported analyses, paving the way towards a generalized relationship having (N-1) *P-Z* pairs, hence establishing relevance to many-stage design. This new fundamental theory will be revealing that the impact of the *P-Z* pairs on the settling time of CMOS OTAs can be minimized by positioning the open-loop zeros at low frequencies provided that there is sufficient DC gain.
- Chapter 4 builds on the discussion in Chapter 3 to introduce a new FCT that depends on low-frequency zeros, through which a scalable many-stage CMOS OTAs with an ultra-

wide C_L-drivability will be realized. This chapter starts by introducing the overall idea, then discussing the choice of gain-stages and the details regarding the transistor-level implementation. Afterwards, the proposed FCT will be implemented in two steps; the first step involves designing the OTA's compensation circuit to position the 2-stage CMOS OTA's pole-zero pair, then scale this design for higher stages (i.e., 3-, 4-, …, 8-stage). This 1st step will be done having a small capacitive load. Once finalizing the design of many-stage CMOS OTAs having a small C_L, the second step of implementing the proposed FCT will be introduced. This 2nd step involves increasing C_L-drivability of the CMOS OTA for a desired settling time.

- Chapter 5 verifies and validates the proposed fundamental theory (i.e., generalized relationship between frequency response and settling time of CMOS OTAs) of chapter 3 by exploiting the design technique of Chapter 4. The verification and validation in Chapter 5 will be done through simulations (schematic and post-layout) as well as some measurement results. This chapter concludes with a performance summary of the proposed OTAs and a comparison with the most recent designs.
- Chapter 6 verifies and validates the proposed FCT and the proposed many-stage CMOS OTA of chapter 4 through simulations and measurements results. Also, this chapter discusses the experimental setup, which includes the measurements' equipment, the PCB, and the on-chip and off-chip components. This chapter concludes with a performance summary of the proposed OTAs and a comparison with state-of-the-art designs.
- Chapter 7 concludes the work presented in this thesis and the future advancements are discussed.

1.5. Claim of Originality

In this section, a summary of the original contributions made in this thesis is presented in point-form. The contributions are as follows:

- A new fundamental theory is presented in this thesis showing the generalized relationship between frequency response and settling time of CMOS OTAs in the presence of P-Z pairs/doublets. This theory shows how to reduce the impact of *P-Z* pairs/doublets on the settling time of CMOS OTAs - using low-frequency zeros and cascaded-gain stages - consequently revealing untapped opportunities for many-stage CMOS OTA design. This theory has been validated through simulations (schematic and post-layout) as well as some measurement results. This original contribution is discussed in chapter 3 and the verification and validation are discussed in chapter 5.
- Based on the proposed theory, a new FCT is proposed in this thesis. This new FCT relies on low-frequency left-half-plane zeros to allow the proposed many-stage CMOS OTAs to exhibit a stable response and operate for a desired closed-loop behavior while driving an ultra-wide range of capacitive loads. Unlike conventional FCTs, the proposed FCT is applicable regardless of how many gain stages are being cascaded, and it is not constrained by any specific circuit topology. Also, this FCT depends on intuitive technique to position the OTA's poles and zeros. To easily implement the proposed FCT, the well-known Miller R-C compensation circuit will be used to position the poles and zeros according to the proposed theory. This original contribution is discussed in chapter 4 and the verification and validation are discussed in chapter 5 and Chapter 6.

- A new study on the impact of low-frequency zeros on C_L-driveability and settling time requirements of CMOS OTAs is also presented as a part of the proposed FCT. This study shows how the Phase Margin (PM) is changing with the increase in C_L based on different scenarios of positioning the OTA's poles and zeros in the proposed FCT. Accordingly, it indicates the behavior of the closed-loop step response, hence, defining the OTA's speed. This original contribution is discussed in chapter 4 and the verification and validation are discussed in chapter 6.

- Based on the proposed theory and the proposed FCT, a new scalable CMOS OTA design that systematically enables cascading many identical gain stages - in a closed loop configuration - is presented in this thesis. The proposed scalable CMOS OTA uses classical gain-stages (i.e., differential pair and common source transistors) to design fully-differential 2-, 3-, 4-, 5-, 6-, 7-, and 8-stage CMOS OTAs. The presented design realizes a CMOS OTA with scalable-gain that increases in 25 dB increments per stage, achieving a total gain from 50 dB to 200 dB for a 2-stage to an 8-stage configuration, respectively. The presented design is verified through extensive simulations based on a TSMC 65 nm CMOS process. Also, as a proof-of-concept, the design has been validated by fabricating 2-, 3-, and 4-stage CMOS OTAs in the standard TSMC 65 nm CMOS process, and the measurement results show that the 2-stage OTA is achieving a DC gain of 50 dB with a C_L-drivability ratio of 10,000×, the 3-stage OTA is achieving a DC gain of 70 dB with a C_L-drivability of 1,000,000x, and the 4-stage OTA is achieving a DC gain of 90 dB with a C_L-drivability of 1,000,000x. This is a 10-to-1000-time

improvement in the state-of-the-art. This original contribution is discussed in chapter 4 and the verification and validation are discussed in chapter 5 and Chapter 6.

1.6. Derived Publications

This section lists the publications that were derived from this thesis. In all of these publications the author of this thesis was the main, first and corresponding author. Professor Gordon W. Roberts has supervised the work, and reviewed these publications. These publications are as follows:

Peer-reviewed journal papers:

1- M. A. Mohammed and G. W. Roberts, "Generalized Relationship Between Frequency Response and Settling Time of CMOT OTAs: Toward Many-Stage Design", *IEEE Transaction on Circuits and Systems-I, Regular Papers*, vol. 68, no.12, pp. 4993-5006, December 2021.

2- M. A. Mohammed and G. W. Roberts, "Scalable Multi-Stage CMOS OTAs with a Wide C_L-Drivability Range Using Low-Frequency Zeros", *IEEE Transaction on Circuits and Systems-I, Regular Papers*, (Under review).

US Patents:

3- M. A. Mohammed and G. W. Roberts, "Enhance Gain of Operational Amplifiers through Low-Frequency Zero Positioning" *US Provisional Patent. No. 63/190,961; Y/R: 2021-075; O/R: 05001770-919USPR,* filed: May 20, 2021 (PENDING).

4- M. A. Mohammed and G. W. Roberts, "Design of High-Order OTA/Op-Amps with Single-Time-Constant Response" *US Provisional Patent No. 62/874563 For ROI 2019-066,* filed: July 16, 2019. (PENDING).

Peer-reviewed conference papers:

5- M.A. Mohammed and G. W. Roberts, "A Scalable Many-Stage CMOS OTA for closed-loop Operation" *in Proc. IEEE International Symposium on Circuits and Systems (ISCAS 2021)*, May 2021, Daegu, South Korea.

6- M.A. Mohammed and G. W. Roberts, "Conventional CMOS OTAs Driving nF-Range Capacitive Loads" *in Proc. IEEE International Symposium on Circuits and Systems (ISCAS 2021)*, May 2021, Daegu, South Korea.

7- M. Mohammed and G. W. Roberts, "The Impact of the Scaled Down CMOS Technologies on the Step Response Degradation Caused by the Pole-Zero Doublets in the OTAs", *in Proc. of the 11th IEEE Latin American Symposium on Circuits and Systems (LASCAS 2020)*, February 25 - 28, 2020, San José, Costa Rica.

8- M. Mohammed and G. W. Roberts, "Investigating the Developments on the Frequency Compensation Techniques of the Two-Stage OTAs - A Brief Guide and Updated Review -" *in Proc. of the IEEE 31st International Conference on Microelectronics (IEEE-ICM 2019)*, December 15 – 18, 2019, Cairo, Egypt.

CHAPTER 2

LITERATURE REVIEW

Since enormous works have been reported in the literature on the design of multi-stage CMOS OTAs, one can present these works from different perspectives, such as:

1. The number of gain stages, as single-, two-, three-, four, and five-stage CMOS OTAs have been reported in the literature.
2. The circuit topology which has been used to design the gain stages. Interestingly, many topologies have been reported such as: the classical differential pair followed by common-source transistors [4], inverter-based gain cells [26], fully balanced linear amplifiers [27], digital-based OTA [28], etc.
3. The FCT that has been used to ensure the OTA's stability. Based on these FCTs different arrangements of OTAs poles and zeros have been discussed.
4. The OTAs' capacitive load drivability, where different C_L values have been reported in the literature (i.e., small loads in the pF-range, large loads in the nF- range, a wide range of loads, etc.).

5. The performance metrics such as: the DC gain, speed, power consumption, silicon area, etc.
6. The applications where the previously reported design can be used in. For instance, one can study the CMOS OTAs which have been used in active filters, in ADCs, etc.

However, as mentioned in chapter 1, the 1st objective of this thesis is to investigate the possible *P-Z* arrangements of CMOS OTAs in search for a potential arrangement that can ensure stability while cascading many-gain stages. Therefore, this chapter will present the previously reported works based on their FCTs to highlight different *P-Z* arrangements.

Knowing that the previously reported FCTs are varying based on the number of gain stages and/or the circuit topologies, this chapter will simplify the discussion by categorizing these FCTs in accordance with the number of gain stages. Then, a separate section will be dedicated to comment on these FCTs and evaluate the advancements that have been made on C_L-drivability. Finally, this chapter will highlight a certain arrangement of poles and zeros to be investigated in chapter 3 as a potential candidate to cascade many-gain stages.

2.1. The Choice for the Block Diagram and the Transfer Function

Before proceeding with these previously reported FCTs, a reference block diagram and a general transfer function that can represent the cascading schemes are required. Fig. 2.1 shows the block diagram of *N*-stage CMOS OTAs, which will be used as the analysis and design vehicle throughout this work. As seen in the block diagram of Fig. 2.1, building multi-stage CMOS

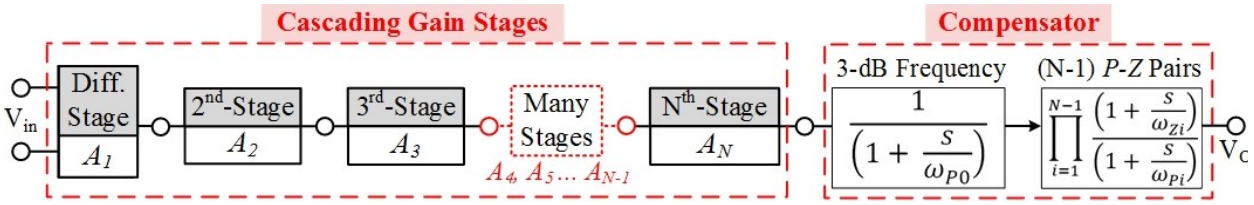

Fig. 2.1: block diagram having *N*-cascaded gain-stages and a compensator.

OTAs requires cascaded-gain stages (to achieve the required gain) and a compensator (to ensure stability and achieve frequency requirements). Since this is a CMOS-based OTA, poles and zeros will be part of the OTA's realization. To appropriately control these poles and zeros, a compensator, similar to the one seen in Fig. 2.1, will be used. Usually, in such OTAs, in addition to the 3-dB frequency, each gain stage will produce a *P-Z* Pair. Therefore, the open-loop transfer function takes a bilinear-cascade form; and it can be written as

$$A(s) = \frac{A_{DC,N}}{\left(1+\frac{s}{\omega_{P0}}\right)} \times \prod_{i=1}^{N-1} \frac{\left(1+\frac{s}{\omega_{Zi}}\right)}{\left(1+\frac{s}{\omega_{Pi}}\right)} \times \prod_{i=1}^{N-1} \frac{1}{\left(1+\frac{s}{\omega_{Ppar,i}}\right)}, \qquad (2.1)$$

where $A_{DC,N}$ is the overall DC gain (i.e., given by Eqn. (1.1)), ω_{P0} is the 3-dB frequency, ω_{Pi} and ω_{Zi} are the open-loop *P-Z* pairs which are produced by the compensation circuit of each stage, and $\omega_{Ppar,i}$ are the parasitic poles, which are produced by the parasitic capacitances associated with the various gain stages. Usually there is no design control over $\omega_{Ppar,i}$, therefore, they have not been included in the compensator of Fig. 2.1. Also, these parasitic poles are usually ignored in the previously reported analysis as they are assumed to be at frequencies much higher than the unity-gain frequency (ω_t). However, they have an important design value in the proposed theory of chapter 3 and the proposed many stage CMOS OTA design in chapter 4, hence, they need to be considered here.

2.2. The Frequency Compensation Techniques of Two-Stage CMOS OTAs

The FCTs of two-stage CMOS OTAs are considered the most critical where the FCTs of the higher order stages are developed based on their core ideas. Many works managed to evaluate and discuss all of these FCTs in one work such as [1, 29-31]; however, they rarely trace the origin of these works and the gradual development that took place over the years. In this section, a brief, yet updated, review of the works on FCTs for the two-stage OTAs will be given, as the last full comprehensive literature review was published in 2001 [30].

The FCTs of the systems with one pole and a *P-Z* pair (i.e., $N = 2$ in Eqn. (2.1)) can be categorized as usually belonging to one of the two commonly used approaches:

(1) Pole-Splitting Approach (PSA), and

(2) Pole-Zero Cancellation approach (P-ZC).

Also, a third compensation technique has been discussed as a result of the P-Z cancellation and considered impractical for the closed- loop applications, which is:

(3) The Pole-Zero Doublet (PZD).

The previous three FCTs are associated with real poles and zeros; however, a fourth FCT has been introduced to deal with complex poles. This FCT is called:

(4) Anti-Pole Splitting approach (Anti-PSA).

The flow chart of Fig. 2.2 shows the revolution in the major FCTs of 2-stage CMOS OTAs since the 1960's for these four FCTs. A brief discussion on these FCTs is presented in the following subsections.

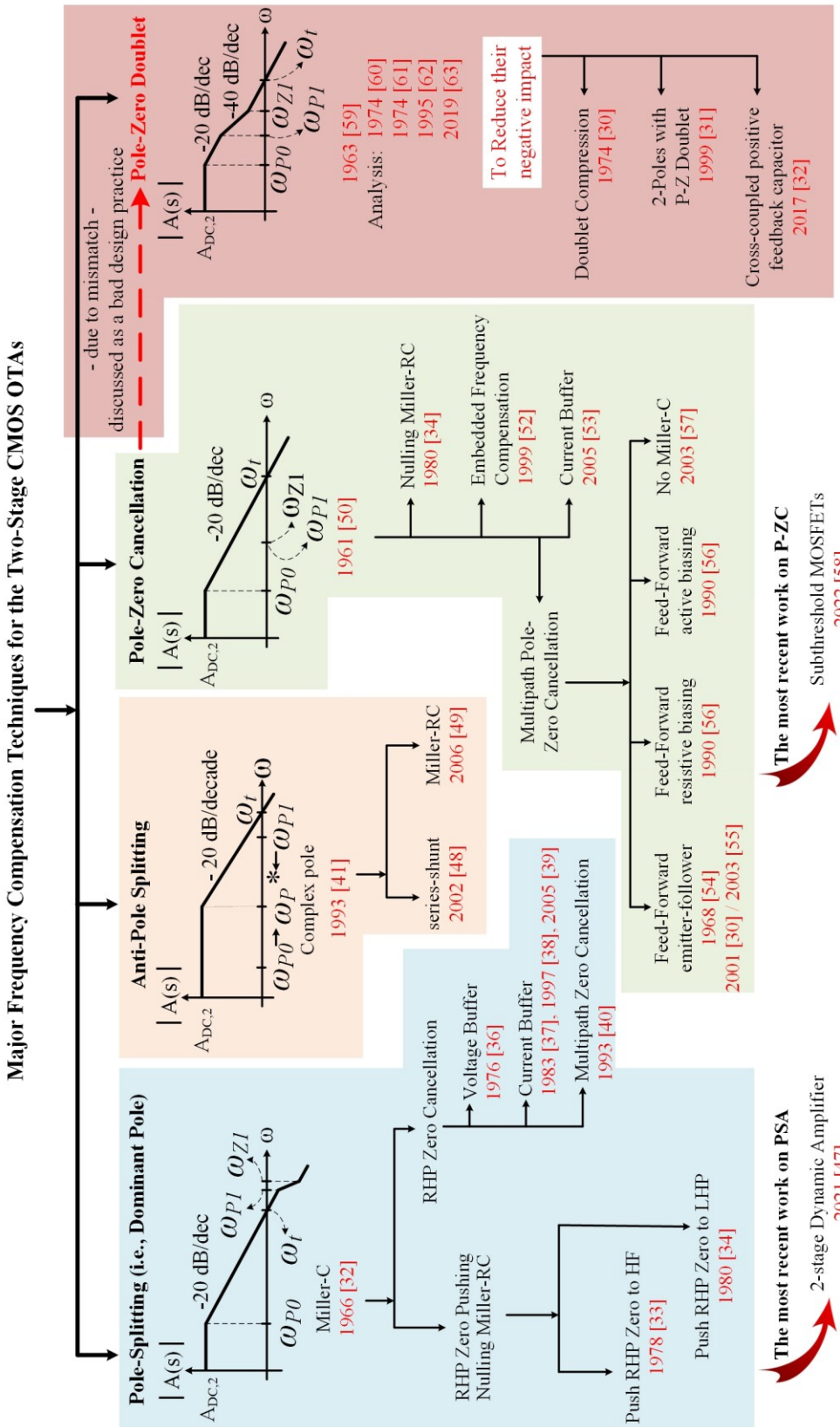

Fig. 2.2: Flow chart of main frequency compensation techniques for two-stage CMOS OTAs.

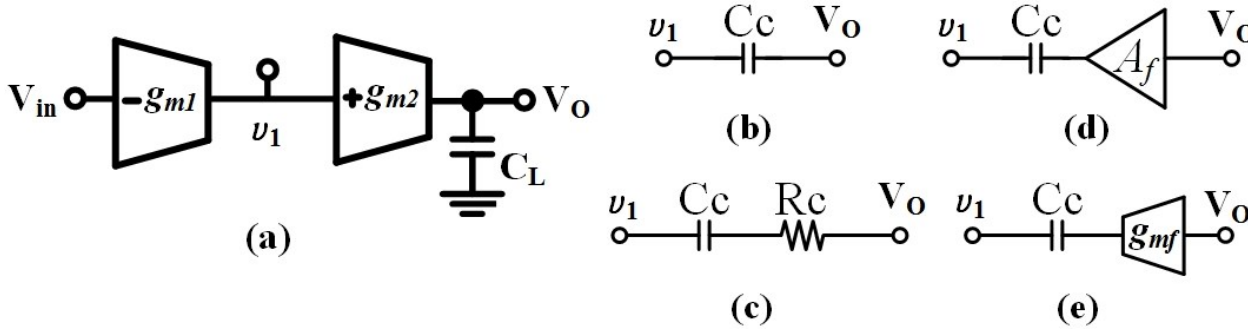

Fig. 2.3: Common compensation circuits (i.e., compensator) used in Fig. 2.1, (a) the block diagram of 2-stage CMOs OTAs, (b) Miller-C, (c) Miller R-C, (d) voltage buffer, and (e) current buffer.

Fig. 2.3(a) shows the block diagram of 2-stage CMOS OTAs, while the common compensation circuits used to stabilize 2-stage OTAs are shown in Fig. 2.3(b) - (e). The developments of the FCTs of Fig. 2.2 are described as follows.

2.2.1. Pole-Splitting Approach (PSA)

The PSA is considered the most well-known FCT. It is commonly referred to as the dominant pole approach, and it was presented in 1966 [32]. The design technique using this approach is to position the pole at frequency ω_{P0}, of Eqn. (2.1), below ω_t and push the *P-Z* pair designated by frequencies ω_{PI} and ω_{ZI} to frequencies above ω_t by appropriately designing the OTA circuit using Miller capacitor of Fig. 2.3(b). On doing so, the open-loop transfer function can be approximated over frequencies less than ω_t by a first-order response described as

$$A(s) = \frac{A_{DC,2}}{\left(1 + \frac{s}{\omega_{P0}}\right)} \quad . \tag{2.2}$$

The AC magnitude response (i.e., $|A(s)|$ vs. ω) of the OTA compensated with the PSA can be seen in the plot at the upper left-side of Fig. 2.2.

To achieve the above mentioned arrangements of the poles and the zero, the position of ω_{Z1} is the critical one, as it will follow the position of the compensated pole (ω_{P1}) to eliminate its effect, or at least reduce it. But, if ω_{P1} has no effect on the response, ω_{Z1} becomes undesired. For this purpose, the following major ideas and techniques have been introduced to control the zero.

2.2.1.1. Right Half-Plane (RHP) Zero Pushing

In this technique the zero is controlled through a proper design of Miller-RC components shown in Fig. 2.3(c) [33]. Here, the undesired zero is located at a very high frequency in the RHP. An alternative technique is to push the RHP zero to the LHP as in [34], where it will give the opposite effects to ω_{P1}. This will ensure that the overall behavior will follow the transfer function given by Eqn. (2.2).

2.2.1.2. RHP Zero Cancellation

The zero is created when a feedforward path is created from input to output [35]. Therefore, some works have blocked this path using different techniques such as:

1. Voltage Buffer:

   In [36] a source follower is placed in the feedforward path. This path has been created by the compensation capacitor and the voltage buffer (i.e., A_f) which are seen in Fig. 2.3(d). This voltage buffer eliminates the RHP zero.

2. Current Buffer:

   The idea here is to create a path for the current to pass through instead of flowing through the feedforward path as seen in Fig. 2.3(e). This will eliminate the zero from being created in the response. The idea has been presented in [37] and then enhanced in [38] and [39].

3. Multi-path Zero Cancellation:

   This technique depends on creating a parallel path to the compensation path. This will allow the current to counteract the current in the feedforward path. This technique has been introduced for the first time in [40].

The PSA has the advantage of a stable response because only one pole is below ω_t. Unfortunately, this technique provides limited Gain-Bandwidth Product (GBW) because it requires positioning ω_{P1} and ω_{Z1} at frequencies above ωt [41]. Also, the possible improvements on the PSA are limited, especially for the two-stage OTA, as the choices for the poles and the zero positions are limited. Nevertheless, many works have been proposed to enhance the operation of two-stage CMOS OTAs under the PSA as in [42-46], with the most recent work in 2021 [47].

2.2.2. Anti-Pole Splitting Approach (Anti-PSA)

As seen in Fig. 2.2, this approach was presented in 1993 [41]. Unlike the PSA, in this approach the two poles are pushed towards each other to create a complex pole, where the zero is assumed to be at a very high frequency. This is achieved by adding a capacitive feedback path other than

the compensation path. This approach has been enhanced in [48] and [49]. In [48] a resistor has been added to give an extra degree of freedom to control the position of the poles and the zero. However, in [41] and [48], BJTs have been used to build the OTA; while in [49] MOSFETs have been used to design the OTA. In [49] the capacitive feedback has been cross connected to the outputs of first and second stages, combined with the classic Miller RC compensation network. This contributed to a better Phase Margin (PM).

This approach has an advantage of higher GBW compared to the PSA. However, this approach requires a tight control over the values of the components used to control the positions of the poles. Also, this approach is sensitive to the components mismatch. Even though, this approach requires more enhancement and only few works have considered deploying it.

2.2.3. Pole-Zero Cancellation Approach (P-ZC)

The P-ZC, which was presented in 1961 [50], is another approach to design 2-stage CMOS OTA for stable closed-loop operation. By positioning the zero and the pole at the same frequency, i.e., $\omega_{P1} = \omega_{Z1}$, the open-loop response takes on a 1st-order response described by Eqn. (2.2). The magnitude response of this pole-zero arrangement is illustrated in Fig. 2.2. Different techniques have been introduced to achieve P-Z cancellation. These techniques are:

2.2.3.1. Nulling Miller-RC

This technique has been presented in [34], where the Miller-RC compensation circuit is used. The difference between the technique here and the technique in the PSA approach is that instead

of positioning the zero at high frequencies, the zero is placed on the top of the compensated pole in the LHP to totally cancel its effects. This requires a tight control over the value of the RC network. This technique has been enhanced in many works, like in [51], where an additional Miller RC network has been cross connected to the outputs of first and second stages, combined with the original Miller RC compensation network.

2.2.3.2. Embedded Frequency Compensation

In [52] the proposed technique depends on the inter-stage coupling capacitors in between the stages to create the poles and the zeros to cancel each other. For the two-stage OTA, the second-stage LHP pole is inherently and exactly canceled by a first-stage LHP zero.

2.2.3.3. Current Buffer

Similar to the current buffer in PSA, the idea here is to add a current buffer (e.g. common-gate MOSFET) in the compensation network. However, the principle here is not to create a different path for the current, but rather to have a control over the zero location and place it on the top of the compensation pole as in [53].

2.2.3.4. Multi-path Pole-Zero Cancellation

The idea of the multi-path P-ZC is to create more than one path from input to output. But the condition here is that each path must counteract the effects of the other path. Many circuit techniques have been presented to create these different paths, such as:

1. Feed-Forward “emitter-follower”:

   The idea of the feed-forward has been presented for the first time in [54]. The idea has been realized here by adding an emitter-follower coupling between the first and the second stages. This technique has also been enhanced in [30] and [55].

2. Feed-Forward “resistive biasing”:

   This technique has been introduced in [56]. It is similar to feedforward with emitter-follower, except that a resistor is being added to the feedforward path. This resistor will give more controllability to position the pole-zero pair to achieve a full pole-zero cancellation.

3. Feed-Forward “active biasing”:

   Similar to the previous technique, this technique has been introduced in [56]. The only difference is that this technique deploys a transistor instead of the resistor in biasing the feedforward path.

4. No Miller-C:

   In [57] a new technique to achieve full P-Z cancellation has been introduced. The technique used in this paper employs a feedforward path to create LHP zero. However, no Miller capacitors have been used. Therefore, the dominant pole is not pushed to lower frequencies, resulting in a higher GBW.

The P-ZC approach has the advantage of high bandwidth response, therefore, the advancement on this approach is undergoing with the most recent work in 2022 [58]. However, a critical drawback in this method is that the P-ZC does not take place completely due to components mismatch resulting in a P-Z pair [59]. This results in an open-loop TF described by

$$A(s) = \frac{A_{DC,2}}{\left(1 + \frac{s}{\omega_{P0}}\right)} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad . \tag{2.3}$$

2.2.4. Pole-Zero Doublet (P-Z Doublet)

The presence of the *P-Z* pair in the open loop response was first discussed in 1963 [59] as a result of the concern towards the effect of mismatch in the P-ZC approach. The presence of *P-Z* pair in open-loop will create a *P-Z* doublet in closed-loop. The open-loop response with the presence of a *P-Z* pair is described by Eqn. (2.3) whose magnitude frequency response is shown in Fig. 2.2. A detailed analysis on the impact of *P-Z* doublet on the time response of closed-loop OTAs was performed in [60 - 63]. It was shown that the *P-Z* doublet deteriorates the settling time and the slew rate of two-stage CMOS OTAs. Consequently, few works have suggested some solutions to deal the time response degradation caused by the *P-Z* doublet, such as:

1. Doublet Compression:

   The degradation in the time response caused by the *P-Z* doublet has been fixed by adding a level shifter with a feed-forward path in [64]. This technique ensures a full P-ZC.

2. Two-pole Op-Amp with a *P-Z* doublet:

   In [65] a system consisting of two poles denoted P_1 and P_2 and a problematic *P-Z* pair has been compensated by adjusting the position of P_2 to maximize the phase margin (PM) of the open-loop response. It is important to note that the positions of the *P-Z* pair are left unchanged by the designer.

3. Cross-coupled positive feedback capacitor:

A gain boosted telescopic OTA has been frequency compensated with cross-coupled positive feedback capacitor with auxiliary op-amp in [66]. Here the settling time has been improved by properly sizing the feedback capacitor.

Almost all related-works in the literature have considered this technique as a bad design practice; therefore, it has been ignored in analog design. Surprisingly, the *P-Z* pair (or doublet) is at the heart of this thesis. The reason behind considering this arrangement of poles and zeros as a potential candidate to cascade many-stage CMOS OTAs will be discussed in the last section of this chapter (i.e., section 2.6) and in Chapter 3.

2.3. The Frequency Compensation Techniques of Three-Stage CMOS OTAs

Once adding a 3rd gain-stage (i.e., $N = 3$), the degree of complexity increases compared to the 2-stage CMOS OTAs, as a new *P-Z* pair is added to the TF of Eqn. (2.1). Therefore, a system of three poles with two zeros will result, and getting the exact expressions of these poles and zeros to accurately positioning them becomes a challenge due to the coupling between stages and the sources of uncertainty, such as variable C_L values, devices' sizes, non-linear effects, etc [67].

Despite these challenges, 3-stage CMOS OTAs seems to be the preferable topology in the literature as it can easily achieve adequate DC gain values in modern CMOS technology nodes. Interestingly, enormous works on the design of 3-stage CMOS OTAs have been reported in the literature, which includes at least 12 published papers [30, 67-77] to review these designs and compare between them in accordance to their FCTs, loads, performance metrics, ect.

However, according to the 1st objective in this thesis, our goal in this chapter is still to investigate the pole-zero arrangements in the previously reported FCTs. Fig. 2.4 illustrates the flow-chart of well-known FCTs for 3-stage CMOS OTAs, with the Miller compensation being at the core of all these FCTs. Interestingly, one can easily see that most proposed FCTs on the design of 3-stage CMOS OTAs follow the lead of 2-stage CMOS OTAs. In other words, almost all proposed FCTs on the design of 3-stage OTAs are arranging the poles and zeros according to the PSA and the P-ZC approach, with no discussion on the presence of pole-zero doublets. A brief discussion on these FCTs is presented in the following subsections.

2.3.1. Pole-Splitting Approach (PSA)

Nested-Miller compensation (NMC) is known as one of the most classical pole splitting techniques for 3-stage OTAs frequency compensation [78]. The basic idea of NMC scheme was firstly presented in 1985 [79] where nested-capacitors were added across several pairs of gain stages to achieve pole-splitting. Fig. 2.5 shows a compensated 3-stage OTA using NMC method, where three gain-stages, including: two inverting OTAs (i.e., g_{m1} and g_{m3}), and one non-inverting OTA (i.e., g_{m2}) have been used. Also, two Miller compensation capacitors (i.e., C_{M1} and C_{M2}) are used between gain stages in the NMC compensation. However, this technique has the disadvantage of having a low GBW and a large silicon area due to the use of Miller capacitors, hence; different techniques have been proposed to overcome these drawbacks. The central idea of these enhancements is to modify the compensation capacitors by adding extra feedforward or feedback paths, replacing one of the capacitors with a feedback or feedforward active

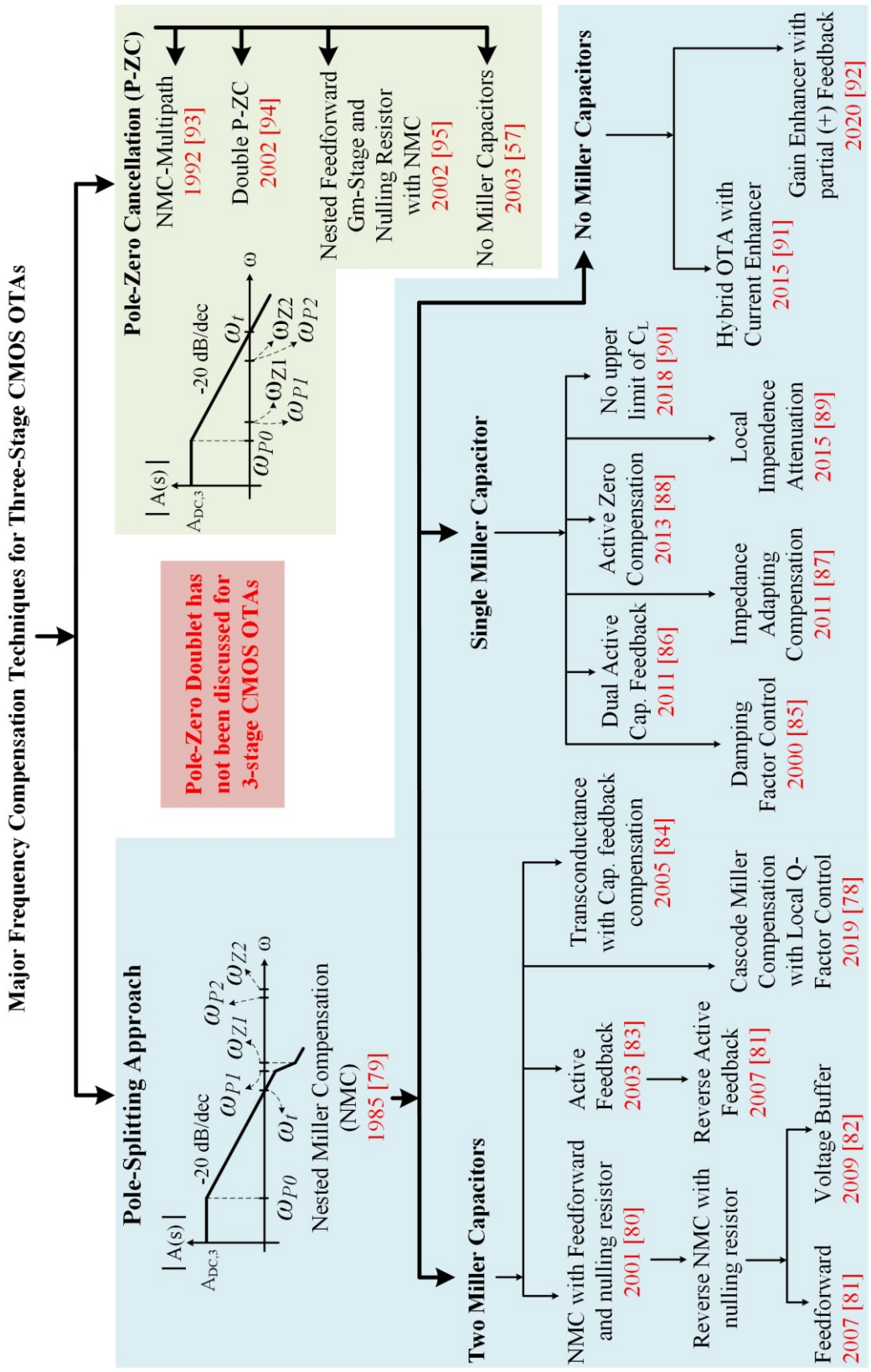

Fig. 2.4: Flow chart of main frequency compensation techniques for three-stage CMOS OTAs.

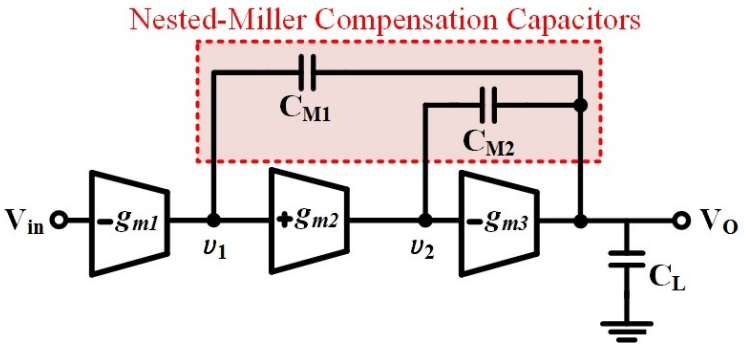

Fig. 2.5: Three-stage CMOS OTA with NMC.

component(s), or by proposing capacitor free compensation techniques. To easily discuss these works, one can divide them based on their use of the Miller capacitors to (1) compensation with two Miller capacitor as in [78, 80-84], (2) compensation with single Miller capacitor as in [85-90], and (3) compensation with no Miller capacitors as in [57, 91-92]. These three compensation techniques will be discussed in the following three subsections.

2.3.1.1. Compensation Using Two Miller Capacitors

To enhance the NMC of Fig. 2.5, some reported works in the literature have kept the two Miller capacitors but they have added auxiliary circuits to enhance this well-known technique, such as:

1. The NMC with Feedforward and nulling resistor

   In [80], a resistor (R_C) has been added to the compensation path to address the RHP zero in the open-loop response of NMC as seen in Fig. 2.6(a). Also, a feedforward transconductance stage (g_{mf}) has been included to enhance the GBW of NMC.

   To increase C_L-drivability of the NMC with nulling resistor, a reverse structure seen in Fig. 2.6(b) was proposed in [81]. Then, in [82] a voltage buffer (i.e., A_f) and two

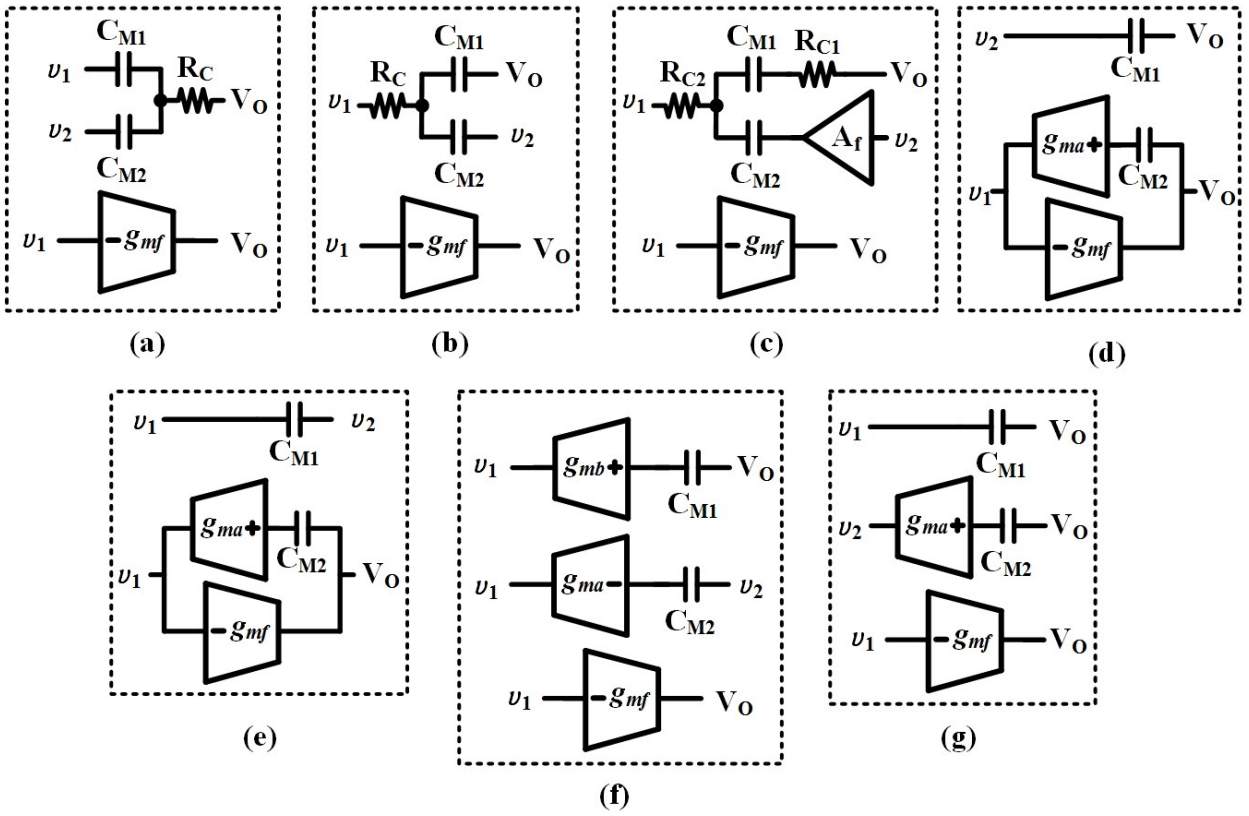

Fig. 2.6: Frequency compensation structures for the 3-stage CMOS OTAs of Fig. 2.5 with two Miller capacitors: (a) The NMC with feedforward and nulling resistor, (b) reverse NMC with feedforward and nulling resistor, (c) reverse NMC with voltage buffer and nulling resistor, (d) active feedback, (e) reverse active feedback, (f) cascode Miller compensation with local Q-factor control, (g) transconductance with capacitor feedback compensation.

nulling resistors (i.e., R_{C1} and R_{C2}), along with a feedforward stage, have been added, as seen in Fig. 2.6(c), to the compensation network to improve slewing and settling performance of NMC with feedback and nulling resistors technique.

2. Active Feedback

In [83], a high-speed block separates the low-frequency high-gain path and high-frequency signal path such that high gain and wide bandwidth can be achieved simultaneously. Fig. 2.6(d) shows the high-speed block in between v_1 and V_O, while low-

frequency high-gain path includes C_{M1}. To increase C_L-drivability of Active Feedback method, a reverse structure seen in Fig. 2.6(e) was proposed in [81], where C_{M1} is connected between v_1 and v_2 instead of v_2 and V_O.

3. Cascode Miller Compensation with local Q-factor control

   Fig. 2.6(f) shows the compensation scheme of this technique [78] where it consists of cascode Miller compensation block (i.e., $+g_{mb}$ and C_{M1}) to eliminate the feed-forward signal path (which may cause the RHP zero) that exists in simple Miller compensation, and create a LHP zero. A feed-forward path (g_{mf}) is added to form a push-pull output stage to improve the transient performance. Also, a feedback path (i.e., $-g_{ma}$ and C_{M2}) is added to enhance the Q-factor in order to ensure stability.

4. Transconductance with capacitor feedback compensation

   Fig. 2.6(g) shows the compensation circuit in this technique, which was proposed in [84]. In this technique a transconductance stage and capacitive feedback (i.e., $+g_{ma}$ and C_{M2}) are used for compensation to improve GBW, stability, and reduce sensitivity of the system. Also, a transconductance stage ($-g_{mf}$) is added to improve the slew-rate.

2.3.1.2. Compensation Using Single Miller Capacitor

In some proposed works in the literature, the NMC technique of Fig. 2.5 has been enhanced by eliminating one of the Miller capacitors to reduce the occupied silicon area. However, similar to the FCTs with two Miller capacitors, auxiliary circuits are being used in the single Miller capacitor techniques to boost the GBW or to increase the OTA's C_L-drivability. Some examples of these previously reported works on single Miller capacitor are as follows:

1. Damping factor control

   This technique was presented in [85]. As seen in Fig. 2.7(a), a damping-factor-control block (i.e., g_{ma} and C_f) is added to control the damping factor and make the amplifier stable. The main advantage of this technique is to drive large capacitive loads.

2. Dual active capacitive feedback

   In [86], dual high-speed active-capacitive-feedback paths (i.e., $g_{ma,1}$, $g_{ma,2}$, and C_{M1} of Fig. 2.7(b)) enable the non-dominant complex poles of the amplifier to be located at high frequencies for bandwidth extension. Also, the use of the small compensation capacitance and the presence of push-pull second and output stages (i.e., $g_{mf,1}$ and $g_{mf,2}$) has helped enhance the time response of the proposed amplifier.

3. Impedance adapting compensation

   As seen in Fig. 2.7(c), this technique has a normal Miller capacitor (C_{M1}), which is still needed to provide an internal negative feedback loop. However, serial RC impedance has been used as a load to the intermediate stage (i.e., C_f and R_f) to improve performance parameters such as stability, gain-bandwidth product and power dissipation. This technique was proposed in [87].

4. Active Zero Compensation

   Fig. 2.6(d) shows the FCT in [88], where the 3-stage OTA has been optimized via combining current-buffer Miller compensation (i.e., g_{ma}, g_{mf}, and C_{M1}) and parasitic-pole cancellation via an active left-half-plane zero circuit (i.e., g_{mb}, C_f, and R_f) to extend the OTA's C_L-drivability and achieve a low power consumption and occupies a small silicon area.

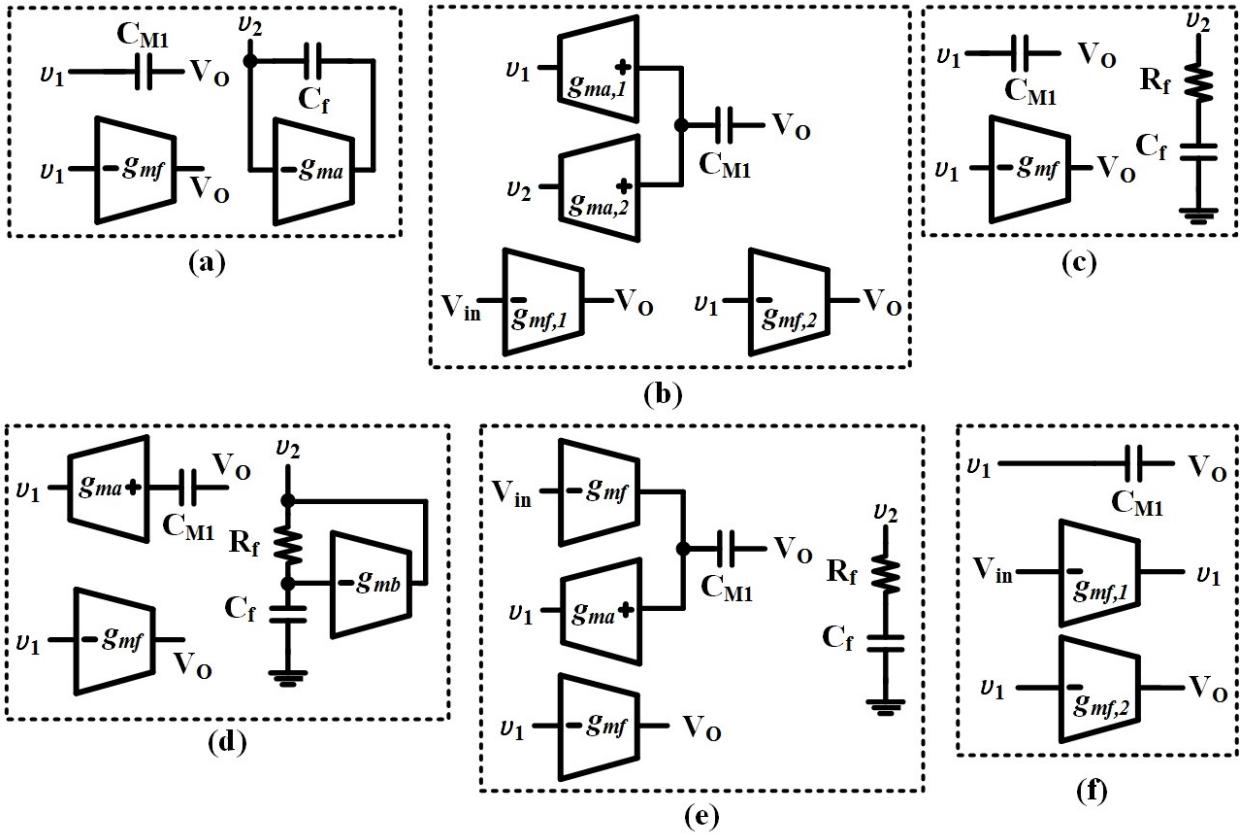

Fig. 2.7: Frequency compensation structures for the 3-stage CMOS OTAs of Fig. 2.5 with single Miller capacitor: (a) damping factor control, (b) dual active capacitive feedback, (c) impedance adapting compensation, (d) active zero compensation, (e) local impedance attenuation, and (f) no upper limit of C_L.

5. Local impedance attenuation

   This technique has been presented in [89] as an enhancement on the dual active capacitive feedback technique of [86]. As seen in Fig. 2.7(e), a local impedance attenuation block (i.e., C_f and R_f) has been added to control the complex poles. This block attenuates the high-frequency resistance at the second-stage output and achieves an optimized trade-off between the frequency and the Q-factor of the complex poles.

6. No upper limit of C_L

   In [90], a single Miller capacitor and an inverting current buffer embedded in the input stage (i.e., $g_{mf,1}$ and C_{M1}) are exploited to implement the frequency compensation network. An additional feed-forward path (i.e., $g_{mf,2}$) and a slew rate enhancer are also utilized to improve the large-signal transient response. This FCT starts to operate properly for $C_L > 5$ nF.

2.3.1.3. Compensation with no Miller Capacitors.

The third structure to enhance the NMC technique of Fig. 2.5 is by eliminating the Miller compensation capacitors. This technique has been proposed in the following works:

1. Hybrid OTA with current enhancer

   This technique was presented in [91], where a cascade structure of six proposed signal-current enhancers (i.e., g_{mf} of Fig. 2.8(a)) is applied to a standard operational transconductance amplifier (OTA) to improve its gain-bandwidth (GBW) product, slew rate (SR), and voltage gain through significant enhancements of the small-signal and transient output currents.

2. Gain enhancer with partial positive feedback

   In [92] a state feedback compensation strategy with gain enhancement using partial positive feedback is proposed. Here, the 3-stage OTA can be made output-compensated, thereby requiring no Miller capacitance while being able to drive a wide range of load capacitances. As seen in Fig. 2.8(b) three transconductance blocks (i.e., g_{mf}, $g_{ma,1}$ and

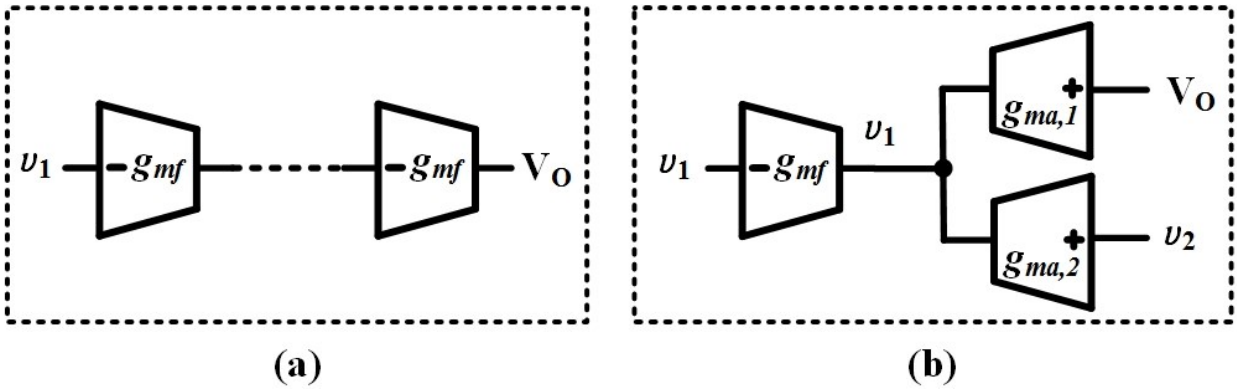

Fig. 2.8: Frequency compensation structures for the 3-stage CMOS OTAs of Fig. 2.5 with no Miller capacitors: (a) Hybrid OTA with current enhancer, and (b) Gain enhancer with partial positive feedback.

$g_{ma,2}$) are used. The output impedance of the first stage is reduced due to the local loop by g_{mf} , which allows the non-dominant poles to be pushed to higher frequencies. Similar observations can be made about the gain of the second stage and $g_{ma,1}$. This feedback is also seen as the cause of gain degradation and hence the need for the restorative effect of $g_{ma,2}$.

2.3.2. Pole-Zero Cancellation Approach (P-ZC)

According to Eqn. (2.1), for $N = 3$, one can get a full P-ZC by positioning ω_{P1} and ω_{P2} at the exact frequencies of ω_{Z1} and ω_{Z2}. However, getting such full P-ZC is difficult due to components mismatch. Nonetheless, some works in the literature have proposed different techniques to get such P-ZC. These techniques are based on the idea of NMC, such as:

1. NMC-Multipath

   In [93], one of the RHP zeros has been moved to the LHP to achieve pole-zero cancellation. In order to get such P-ZC, a transconductance stage (i.e., g_{mf}) is added to the

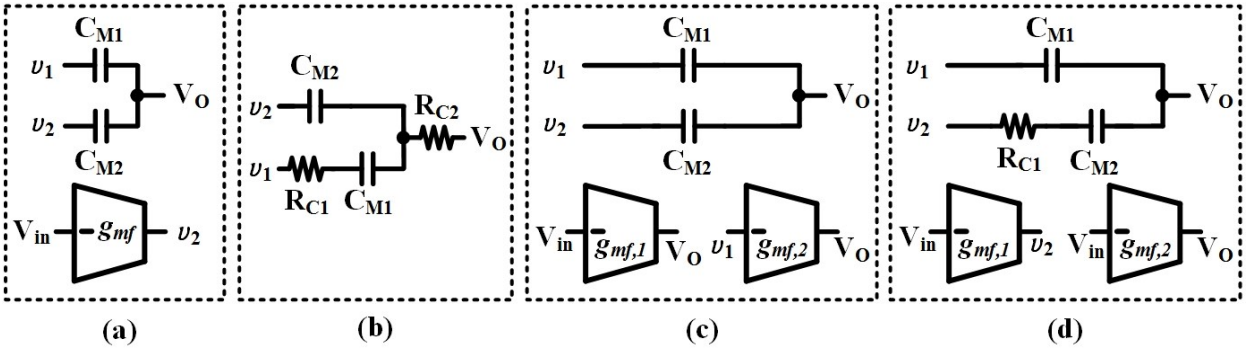

Fig. 2.9: Frequency compensation structures for the 3-stage CMOS OTAs of Fig. 2.5 to achieve P-ZC: (a) NMC-Multipath, (b) Double P-ZC, (c) Nested G_m-Capacitor Compensation, and (d) Nested feedforward G_m-stage and nulling resistor with NMC.

structure of NMC of Fig. 2.5. This results in the compensation structure seen in Fig. 2.9(a). However, this technique allows achieving P-ZC in one *P-Z* pair only.

2. Double P-ZC

   In [94], two Miller capacitors (i.e., C_{M1} and C_{M2}) and two Miller resistors (i.e., R_{C1} and R_{C2}) were used to control the OTA's poles and zeros to get a full P-ZC. This technique is applicable under large C_L conditions. Fig. 2.9(b) illustrates the compensation network in the double P-ZC technique.

3. Nested feedforward G_m-stage and nulling resistor with NMC

   In the NMC-Multipath structure, one of the RHP zeros has been canceled by adding a transconductance stage. Therefore, both RHP zeros can be compensated by adding two transconductance stages as has been done in [19]. These two transconductance (i.e., $g_{mf,1}$ and $g_{mf,2}$) can be seen in Fig. 2.9(c). However, the work in [19] has been done for 4-stage CMOS OTAs; therefore, in [95] this technique has been adapted with a slight modification to make it suitable for 3-stage CMOS OTAs. This modification can be seen

in Fig. 2.9(d), where a nulling resistor has been added to better control the zeros positions and the transconductance blocks are slightly modified to get a better GBW.

4. No Miller capacitors

   In [57], a feedforward path is used to create a LHP zero, where Miller capacitors have not been used. Therefore, the dominant pole is not pushed to lower frequencies, resulting in a higher GBW. This technique has also been used for 2-stage CMOS OTAs. Interestingly, a full P-ZC has not been achieved in this work, thus, a P-Z doublet has been created in the closed-loop response. Surprisingly, this impact of *P-Z* doublets was not apparent in [57] and the settling time degradation was barely noticeable.

2.4. The Frequency Compensation Techniques of Four-Stage CMOS OTAs

Four-stage CMOS OTAs can provide higher DC gains than 3-stage and 2-stage CMOS OTAs, but once they are configured in closed-loop, they are a challenge to stabilize. Therefore, only a few works have proposed four-stage designs in the literature such as [19]-[24]. Fig. 2.10(a) shows the cascading of 4 gain-stages which will be used in this section. Unlike 2- and 3-stage CMOS OTAs, it is easier to discuss the previously reported FCTs for the 4-stage CMOS OTAs individually rather than dividing them based on their pole-zero arrangements.

- In [19], the 4-stage OTA has been compensated using Nested G_m-Capacitor Compensation. This technique adds feedforward paths to the nested structure to eliminate the right-half-plane (RHP) zeros associated with the Miller capacitors. The 4-stage implementation of this strategy is shown in Fig. 2.10(b). This technique improves on the

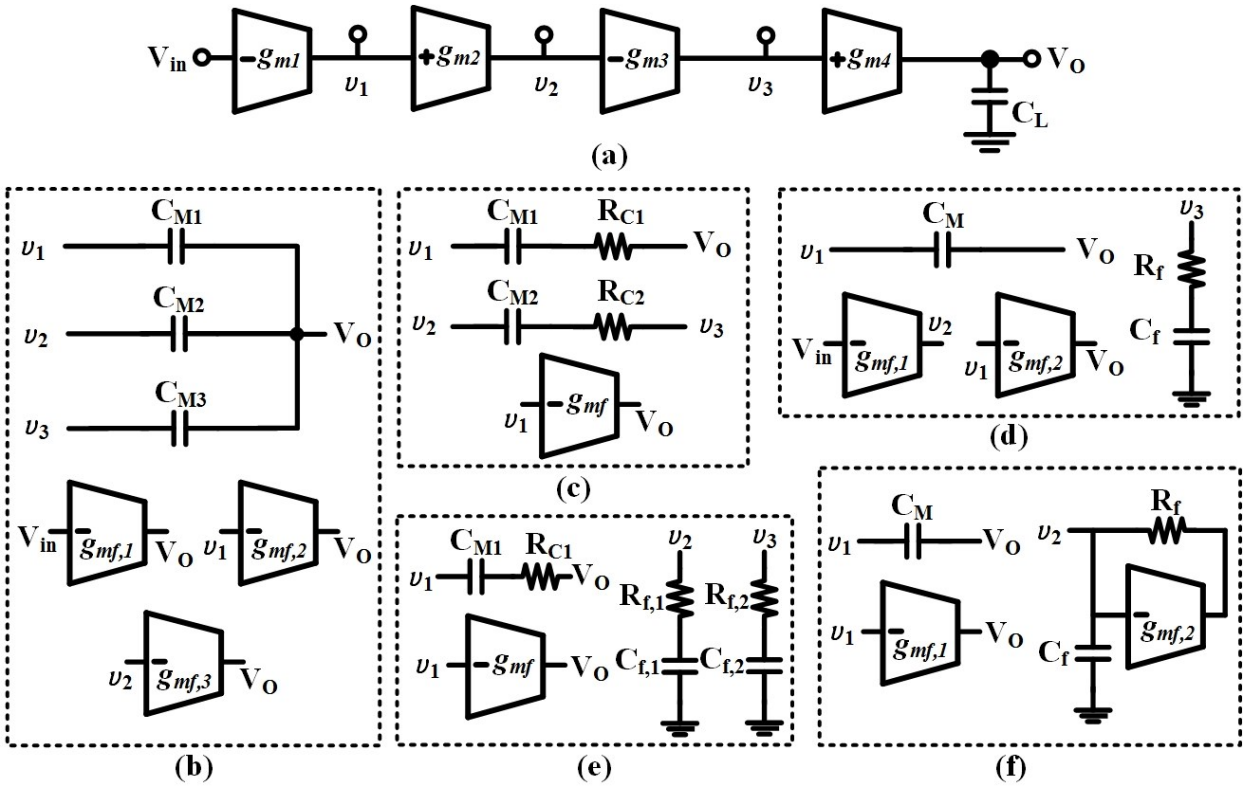

Fig. 2.10: Frequency compensation structures for the 4-stage CMOS OTAs: (a) block diagram of cascading 4-stage OTA, (b) FCT in [19], (c) FCT in [20], (d) FCT in [21], (e) FCT in [22], and [23], and (f) FCT in [24].

performance of NMC due to the elimination of the RHP zeros but its power consumption and required compensation capacitors remain comparatively large.

- In [20], one feedforward stage and two separate Miller compensation signal paths are constructed. The block diagram of the proposed compensation technique is shown in Fig. 2.10(c). In this technique, all the zeros and poles are on the left-half plane without having full P-ZC. Therefore, this technique follows the PSA.
- In [21], a shunt circuit is added at the output of the third stage. Also, two feedforward transconductance elements are used as shown in Fig. 2.10(d) to enhance stability and large signal performance. It should be noted that this technique places a strict accuracy

constraint on R_f to get a full P-ZC and avoid pole-zero doublet as this will deteriorate the transient performance of the amplifier.

- In [22], a shunt circuit (i.e., $R_{f,2}$ and $C_{f,2}$ of Fig. 2.10(e)) is added at the output of the third stage and a Miller compensation with a nulling resistor are also used as shown in Fig. 2.10(e). This technique partially follows PSA as one of the P-Z pairs is canceled. Also, under perfect P-ZC, extension of either the GBW or the capacitive load drive can be achieved.
- In [23], this technique is based on the work in [22], except that it uses two shunt circuits; one at the second stage output and one at the third stage output as shown in Fig. 2.10(e). Two zeros were created from the two shunt circuits and were used for P-ZC. Here, the resistors are required to be accurate to avoid pole-zero doublets.
- In [24], a PSA has been adapted. The main feature of this architecture is the use of single active parallel compensation (APC) structure (i.e., $g_{m,f2}$, $R_{f,2}$ and $C_{f,2}$ of Fig. 2.10(f)). The stability of the proposed OTA is ensured through the Miller capacitor C_m and the APC structure. The Miller capacitor creates a dominant pole and achieves single-pole roll-off at gain crossover. The APC structure produces a zero and two poles to maintain a certain PM values.

2.5. Comments and Observations on the Previously Reported Works

Based on the previous discussion regarding 2-, 3-, and 4-stage CMOS OTAs, one can summarize this discussion with the following points:

1. *The proposed FCTs:*

   Apart from [18], [57], and [96] where the design of *N*-stage CMOS OTAs has been discussed, the previously reported works are proposing FCTs which are suitable for OTAs with specific number of stages and/or circuit topologies. Nevertheless, the work in [57] and [96] have demonstrated the design of 2- and 3-stage CMOS OTAs only, while the work in [18] has demonstrated the design of 2- to 5-stage CMOS OTAs, but it consumes high power (~10 mW) and introduces unusual levels of overshoot in the transient response of the system. Also, almost all previously reported FCTs are arranging the poles and zeros based on the PSA and the P-ZC. This indicates the pressing need to propose and demonstrate an FCT that is not constrained by the number of gain-stages nor the circuit topology. Clearly, using the same approaches to arrange the OTA's poles and zeros (i.e., PSA and P-ZC) seems to be inappropriate to propose such an FCT.

2. *The advancement on C_L-drivability of CMOS OTAs:*

   Due to the importance of C_L-drivability from the analog applications' perspective, many previously reported works focused on C_L as they were presenting the FCTs. However, few of these reported works discussed the OTA's capability to drive a wide range of capacitive loads, as most of these previously reported works have focused on a specific load, regardless of being small (i.e., in the pF-range) or large (i.e., in the nF-range). To easily discuss the advancement on C_L-drivability of previously reported works, one can categorize them based on the number of gain stages placed in cascade and evaluate their C_L-drivability ratio (i.e., $C_{L,max}/C_{L,min}$) as follows:

- Many works have managed to demonstrate single- and two-stage CMOS OTAs with wide C_Ls [25, 44, 45, 97-99]. However, they all make use of additional circuit techniques to achieve adequate DC gain while handling such C_L. In the case of single-stage OTAs, the maximum-reported C_L-drivability ratio is 150× [99]. In the case of two -stage OTAs, the maximum C_L-drivability ratio is 1000× [25].
- To achieve both the load driving capability and the DC gain requirement, most works found in the literature deploy 3-stage OTAs [86-92, 100 and 101]. However, the maximum C_L-drivability ratio that has been reported in literature with 3-stage OTAs is 555.5× [92].
- As for 4-stage CMOS OTAs, only a few works have proposed 4-stage designs to drive a wide range of C_Ls, such as [19 and 24]. However, the maximum C_L-drivability ratio was limited to 30× [24].

2.6. Conclusion: a Potential *P-Z* Arrangement for Cascading Many-Stage CMOS OTAs

Since the 1st objective of this thesis is to investigate the possible *P-Z* arrangements of CMOS OTAs in search for a potential arrangement that can ensure stability while cascading many-gain stages, one can easily observe that the *P-Z* pair (or doublet) arrangement has been ignored in the literature due to the analysis in [59-63]. As mentioned in subsection 2.2.4, the analyses in [60-63] showed that the closed-loop *P-Z* doublet deteriorates the OTA's settling time. Surprisingly, the *P-Z* doublet was seen in some designs in the literature, such as in [57], but their impact was

not apparent and the settling time degradation was barely noticeable. Moreover, this arrangement of poles and zeros (i.e. the P-Z doublet) is a very well-known and commonly-employed compensation technique in switching and linear power regulators (in power electronics). This idea is used to compensate standard buck converters and is typically referred to as PID control or type-III compensation [102].

These observations open the door to revisit these analyses and take a closer look at [60-63]. On doing so, the initial investigation on [60-63] reveals the following:

1. The analyses of the relationship between frequency response and settling time were restricted to the case of having a single open-loop *P-Z* pair only, making them most relevant for 2-stage OTAs.
2. The analyses were based on CMOS technologies that range from line widths greater than 1 micron [60] down to only 0.35 μm [63], without considering more advanced nanometer scale technology nodes.
3. Cascading gain-stages was not a design goal in these works, especially that such older technology nodes allowed supply voltages greater than 3 V, relaxing the need for a multi-stage design.

Based on the above, Chapter 3 will be proposing a new generalized relationship between frequency response and settling time to extend the discussion while having many *P-Z* pairs (or doublets), hence establishing relevance to many-stage design. This will be done by revisiting and building upon earlier efforts and analyses. Also, Chapter 3 is extending the analysis – and its implementation - to more advanced nanometer scale technology nodes.

CHAPTER 3

GENERALIZED RELATIONSHIP BETWEEN FREQUENCY RESPONSE AND SETTLING TIME OF CMOS OTAS

The closed-loop step response defines some of the most important metrics that measures the performance of OTAs. Settling Time (T_S), which is the time taken for the output of OTAs to settle within 0.1 % or 0.01 % after the application of an input step [60], is an example of such metrics [1]. Many works in the literature have discussed different sources that might degrade the step response of the OTAs. One of these sources is the existence of the Pole-Zero (*P-Z*) Doublets in the closed-loop operation of OTAs [60-63].

As mentioned earlier in chapter 2, the presence of an open-loop *P-Z* pair below ω_t creates a *P-Z* doublet in closed-loop, and such a phenomenon is well-known in the literature and was first discussed in 1963 [59]. However, the presence of closed-loop *P-Z* doublets at that time was discussed as an effect that arises due to an inevitable mismatch between the pole and the zero when trying to achieve *P-Z* cancellation. The leading and the detailed analysis on the effects of having a *P-Z* pair on the settling time of a closed-loop amplifier was first discussed in [60] and

[61]. Then, the same discussion and conclusion was also stated in [62] and [63]. All these previously reported analyses have discussed this issue while having one *P-Z* pair only.

Based on the observations which have been stated in chapter 2 (i.e., section 2.6) regarding the analyses in [60-63], this chapter attempts at generalizing the relationship between frequency response and settling time, by revisiting and building upon earlier efforts, with the following in mind: (1) the possibility of having many *P-Z* pairs (or doublets), hence establishing relevance to many-stage design, (2) extending the analysis – and its implementation - to more advanced nanometer scale technology nodes. In order to achieve this, the analysis will begin by identifying the independent parameters that control the relationship, eventually leading up to its generalization based on these parameters. Such a generalization will reveal how to reduce the impact of *P-Z* doublets on settling time - through positioning the OTA zeros at Low Frequencies (*LF*) and increasing their gain - consequently revealing untapped opportunities for many-stage CMOS OTA design.

For clarity purposes, from this point and onwards, we shall distinguish between two terms: '*P-Z* pair' and '*P-Z* doublet', where 'pair' will be used for open-loop configurations and 'doublet' will be used for closed-loop configurations.

This chapter starts by revisiting the previously reported analysis on the relationship between frequency response and settling time having one *P-Z* pair in Section 3.1. Then this relationship, having one *P-Z* pair, will be studied to overcome the limitations of the previously reported works in Section 3.2, paving the way toward Section 3.3, in which the relationship will be generalized for *N*-stage OTAs, having (*N*-1) *P-Z* pairs. Finally, Section 3.4 summarizes this chapter.

3.1. Previously Reported Analysis on the *P-Z* Pair Impact on Settling Time

To realize an open-loop transfer function with a one *P-Z* pair (i.e., ω_{P1} and ω_{Z1}) and a finite pole (i.e., ω_{P0}), a two-stage OTA can be used (i.e., $N = 2$). Thus, the *TF* of Eqn. (2.1) can be written as

$$A(s) = \frac{A_{DC,2}}{\left(1 + \frac{s}{\omega_{P0}}\right)} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \times \frac{1}{\left(1 + \frac{s}{\omega_{Ppar,1}}\right)} \ . \tag{3.1}$$

The analyses in [60-63] have ignored the parasitic pole ($\omega_{Ppar,1}$), and they depend mainly on the open-loop *P-Z* pair separation distance (δ_{OL}), which can be expressed as

$$\delta_{OL} = \ \omega_{P1} - \omega_{Z1} \tag{3.2}$$

or as a ratio given by

$$\delta_R = \frac{\omega_{P1}}{\omega_{Z1}} . \tag{3.3}$$

Based on Eqn. (3.1) one can show that the *TF* for the unity-gain closed-loop configuration has the following general form (ignoring the parasitic pole $\omega_{Ppar,1}$):

$$G(s) = \frac{A(s)}{1 + \ A(s)} = \frac{A_{DC,2}}{\left(1 + \frac{s}{\omega_{CL,a}}\right)} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{CL,b}}\right)} \tag{3.4}$$

where $\omega_{CL,a}$ is the frequency of the first pole and $\omega_{CL,b}$ is the frequency of the second pole in the closed-loop response. Fig. 3.1(a) shows the open-loop *P-Z* pair (i.e. ω_{P1} and ω_{Z1}) of 2-stage CMOS OTA that is responsible for creating the closed-loop *P-Z* doublet (i.e. $\omega_{CL,a}$ and ω_{Z1}) of Fig. 3.1(b).

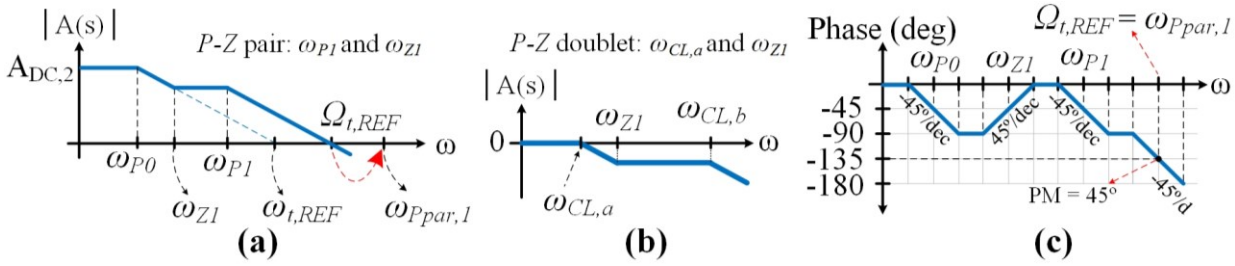

Fig. 3.1: The AC response of 2-stage OTA: (a) the open-loop magnitude response with a *P-Z* pair, (b) the unity-gain closed-loop magnitude response with a *P-Z* doublet, and (c) the open-loop phase response with a *P-Z* pair.

The closed-loop poles of Eqn. (3.4) have been shown [60] to be expressible in terms of the open-loop OTA parameters as:

$$\omega_{CL,a} \approx \omega_{t,REF} \tag{3.5}$$

and

$$\omega_{CL,b} = \omega_{Z1}\left[1 - \frac{\left(1 - \frac{\omega_{P1}}{\omega_{Z1}}\right)}{\left(\frac{\omega_{t,REF}}{\omega_{Z1}} - 1\right)}\right] \approx \omega_{Z1} \tag{3.6}$$

where they have assumed that the unity-gain frequency is equal to GBW, i.e.,

$$\omega_{t,REF} = A_{DC,2} \times \omega_{P0} \tag{3.7}$$

Correspondingly, the closed-loop step response to an input step of magnitude V_{in} can be written as follows [60]

$$V_{OUT}(t) = V_{in}\left[1 - k_1 e^{-t\,\omega_{t,REF}} + k_2 e^{-t\,\omega_{Z1}}\right] \tag{3.8}$$

where

$$k_1 = 1 + \frac{\delta_{OL}}{\omega_{t,REF}} \quad , \tag{3.9}$$

and

$$k_2 = 1 - k_1 = -\frac{\delta_{OL}}{\omega_{t,REF}} \quad . \tag{3.10}$$

From Eqn. (3.8) we see that the step response consists of two time-dependent parts: one involving $\omega_{t,REF}$ and the other ω_{Z1}. Each term is weighted by separate coefficients k_1 and k_2 that are also dependent on δ_{OL}.

Although the *TF* of Eqn. (3.1) has two finite poles, the settling time will be affected by the distance between ω_{P1} and ω_{Z1} only, while the distance between ω_{P0} and ω_{Z1} has no impact. The reason is that once the OTA is constructed in unity-gain closed-loop configuration, ω_{P1} will move towards ω_{Z1}, and ω_{P0} will move towards *the unity-gain frequency*. Consequently, the OTA step response will not be affected by the ratio ω_{Z1}/ω_{P0}. Appendix A gives more clarifications on this idea.

As seen in Eqn. (3.8) and (3.10), the slow settling component residual (i.e., V_{in} k_2) depends on the critical ratio [(V_{in} δ_{OL})/$\omega_{t,REF}$]. This ratio can be made small if the numerator is small or the denominator is large, or both simultaneously. Under such conditions, k_1 is very close to unity and k_2 is very close to zero. In the past, [60] suggested that a small frequency difference between the *P-Z* pair is necessary to achieve a small value for k_2 as it relates to the slow settling component. As this requires tight control over the *P-Z* pair position, it is generally considered impractical. Also, it was concluded that positioning the *P-Z* pair at low frequencies will produce a slower time response with smaller amplitude compared to positioning the *P-Z* pair at high frequencies. Thus, the closed-loop *P-Z* doublet deteriorates the OTA's settling time [60-63].

However, the previous open-loop *P-Z* pair-based analysis is associated with some limitations, which can be discussed in the following two subsections.

3.1.1. The Limitations of the Previously Reported Analysis on the *P-Z* Pair Impact on Settling Time

While deriving the closed-loop poles (i.e., $\omega_{CL,a}$ and $\omega_{CL,b}$), it has been assumed that $\omega_{t,REF} = (A_{DC,2} \times \omega_{P0})$ as seen in Eqn.(3.7). This is not accurate, where the open-loop *P-Z* pair is below the unity-gain frequency, thus, the exact unity-gain frequency ($\Omega_{t,REF}$) can be deduced from the geometry depicted in the bode plot shown in Fig. 3(a), and should be expressed as

$$\Omega_{t,REF} = A_{DC,2} \times \omega_{P0} \times \frac{\omega_{P1}}{\omega_{Z1}} = \omega_{t,REF} \times \delta_R \tag{3.11}$$

Considering the unity-gain frequency to be $\omega_{t,REF}$ in [60] has hidden the fact that increasing δ_R, by increasing δ_{OL}, will increase the unity-gain frequency, which in turn will reduce the slow settling component residual of Eqn. (3.10). This can be clearly seen if k_2 in Eqn. (3.10) is re-written with its exact form (after replacing $\omega_{t,REF}$ by $\Omega_{t,REF}$) as

$$k_2 = -\frac{\delta_{OL}}{\Omega_{t,REF}} = -\frac{\delta_{OL}}{\omega_{t,REF} \times \delta_R} \tag{3.12}$$

While the exact k_1 of Eqn. (3.9) can be rewritten as

$$k_1 = 1 + \frac{\delta_{OL}}{\Omega_{t,REF}} = 1 + \frac{\delta_{OL}}{\omega_{t,REF} \times \delta_R} \quad . \tag{3.13}$$

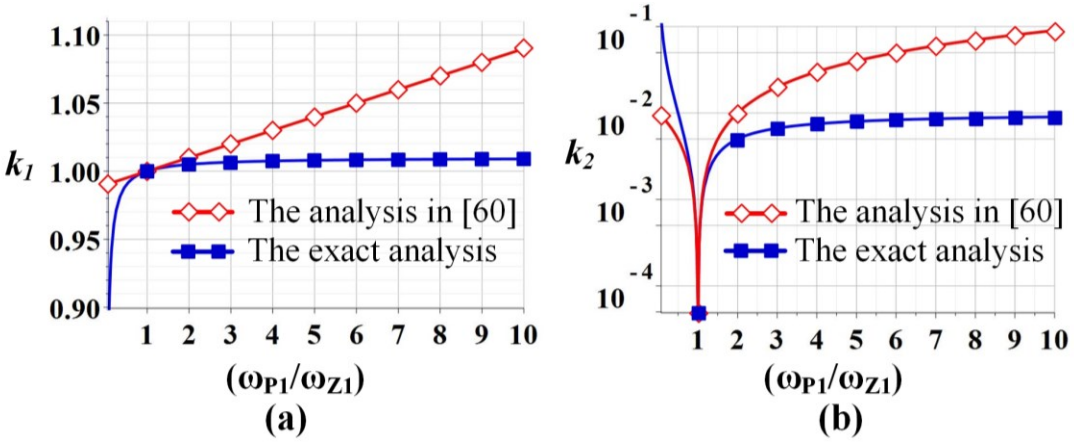

Fig. 3.2: The difference between the previously reported analysis and the proposed exact analysis for step response coefficients: (a) k_1, and (b) k_2.

By simulating Eqs. (3.9), (3.10), (3.12) and (3.13), Fig. 3.2(a) and (b) show the hidden behavior of k_2 and k_1, respectively. As depicted form Fig. 3.2(a) and (b), the results of k_1 and k_2, which have been reported in [60], are accurate only around $\omega_{P1}/\omega_{Z1} = 1$ (i.e., $\delta_R = 1$). Once δ_R goes beyond 2, the slow settling component residuals saturates, as seen in the exact analysis of Fig. 3.2(b), and no more degradation can be introduced even if δ_{OL} is increased.

In addition to the above-mentioned issue of conducting the analysis while having the open-loop dependent parameter $\omega_{t,REF}$, the analysis in [60] has only considered the case where $\omega_{Z1} \geq \omega_{P1}$, while the case of having ω_{Z1} at low frequencies (below ω_{P1}) has not been investigated.

3.1.2. The Impact of the Scaled-Down CMOS Technology Nodes on the Previously Reported Analysis

The conclusion made in [60] on positioning the *P-Z* pair at low or high frequencies is actually relative to $\Omega_{t,REF}$ (i.e., $\omega_{t,REF}$ before correction). Also, the terms fast or slow responses are relative to the actual speed of the response (i.e., $e^{-t\,\Omega_{t,REF}}$); which depends directly on $\Omega_{t,REF}$ (after

replacing ($e^{-t\,\omega_{t,REF}}$) by ($e^{-t\,\Omega_{t,REF}}$) in Eqn. (3.8)). This shows that $\Omega_{t,REF}$ is a critical term, thus, in the following subsection, the relationship between $\Omega_{t,REF}$ and the CMOS technology node will be examined.

3.1.2.1. The Relationship Between the Upper Value of $\Omega_{t,REF}$ and the CMOS Technology Node

Equation (3.8), (3.12) and (3.13) indicate that, if δ_{OL} (or δ_R) is fixed, the higher the value of $\Omega_{t,REF}$, the lower the impact of the *P-Z* pair on the step response of the OTA. However, designing the OTA with the highest possible $\Omega_{t,REF}$ is limited by some factors. One of these factors is the impact of the parasitic pole (i.e., $\omega_{Ppar,1}$) on the frequency response. As seen in Fig. 3.1(a), ideally, the highest value of $\omega_{t,REF}$ (i.e., $\Omega_{t,REF}$ after correction) is $\omega_{Ppar,1}$ to keep the Phase Margin (PM) no less than a desired value (i.e. 45º as seen in Fig. 3.1(c)).

Interestingly, $\omega_{Ppar,1}$ has an inversely-proportional relationship with the parasitic capacitance (C_{par}) of CMOS OTAs (as will be discussed in details in chapter 4). On the other hand C_{par} has a proportional relationship with the CMOS technology node, that is; the smaller the technology node, the smaller C_{par} is [103]. The rate of change in the value of C_{par} with respect to the technology node is $(1/S)$, where S is a dimensionless factor that reflects the scaling in the critical parameters of the transistors devices due to technology scaling [103]. This means that by using scaled-down CMOS technologies, the value of C_{par} will be reduced, thus, $\omega_{Ppar,1}$ will be located at higher frequencies. Consequently, the value of $\Omega_{t,REF}$ can be increased, which allows reducing the negative impact of the *P-Z* pair on the settling time according to Eqn. (3.12) and (3.13).

3.1.2.2. The Predicted Step Response for Different Technology Nodes with the Presence of the P-Z Pair

To examine the exact impact of CMOS technology nodes on the settling time degradation that is caused by the presence of the P-Z pair, a 2-stage CMOS OTA should be designed using different CMOS technology nodes. However, for simplicity one can directly simulate Eqn. (3.8) using predicted models of these different CMOS technology nodes, based on the scale factor (S). In other words, since we have the values of Ω_t, ω_{ZI} and ω_{PI} which were reported in [60], one can simulate Eqn. (3.8) using 0.5 µm, 0.35 µm, and 65 nm CMOS technologies by defining the S factor as

$$S = \frac{2\ \mu m}{x\ \mu m} \qquad , x = [0.5, 0.35, and\ 0.065] \tag{3.14}$$

Accordingly, once using 0.5 µm, 0.35 µm, and 65 nm CMOS technology nodes, the predicted increase in Ω_t can be given as

$$\Omega_{t,x\mu m}(predicted) = S \times \Omega_{t,2\mu m} \quad , x = [0.5, 0.35, and\ 0.065] \tag{3.15}$$

The predicted values of the OTA parameters are shown in Table 3.1. For the Low-Frequency (LF) and High-Frequency (HF) positions of the open-loop *P-Z* pair, the value of Ω_t has been scaled by (1/500) and (1/10), respectively. However, the selection of the LF and HF locations of the open-loop *P-Z* pair is considered for two different cases: (1) $\omega_{ZI} > \omega_{PI}$ and (2) $\omega_{ZI} < \omega_{PI}$. The ratio in distance between the open-loop *P-Z* pair (i.e. ω_{PI}/ω_{ZI}) has been selected to represent the worst case scenario; which is 30% [60]. This gives four different scenarios to the frequency locations of the open-loop *P-Z* pair, which are: (1) LF ($\omega_{ZI} > \omega_{PI}$), (2) LF ($\omega_{ZI} < \omega_{PI}$), (3) HF ($\omega_{ZI} > \omega_{PI}$) and (4) HF ($\omega_{ZI} < \omega_{PI}$).

TABLE 3.1
THE PREDICTED VALUES OF THE DIFFERENT OTA PARAMETERS FOR DIFFERENT CMOS TECHNOLOGY NODES

CMOS Technology node	**Max. V_{in_step} (V)**	**Open-loop P-Z pair (ω_{P1} and ω_{Z1}*)**		**Max. predicted Ω_t**
		ω_{P1} @ Low Frequency (LF)	**ω_{P1} @ High Frequency (HF)**	
2 µm	5	20 kHz	1 MHz	10 MHz
0.5 µm	3.3	80 kHz	4 MHz	40 MHz
0.35 µm	2	120 kHz	6 MHz	60 MHz
65 nm	1	600 kHz	30 MHz	300 MHz

*The value of ω_{Z1} has two different cases for each value of ω_{P1}:
(1) For $\omega_{Z1} > \omega_{P1}$ → [$\omega_{Z1} = \omega_{P1}$ + 30% ω_{P1}], and
(2) For $\omega_{Z1} < \omega_{P1}$ → [$\omega_{Z1} = \omega_{P1}$ - 30% ω_{P1}].

Fig. 3.3 shows the step response of all possible scenarios for the different technology nodes using Eqn. (3.8). These simulations are based on the predicted values of Table 3.1 and they are simulated using *Maple* ©.

To easily investigate the impact of the different CMOS technology nodes on the settling time in the OTA step response when having a *P-Z* pair, a measure parameter is required. Knowing that the settling time degradation can be mostly seen when a settling time at 0.01% of the steady-state value of V_{OUT} is of interest; one can define a parameter called, the degradation in T_S, to represent the time difference between the T_S at 0.01% and the T_S at 1% of the V_{OUT} as follows:

$$T_{S\_degredation} = T_{S\_0.01\%} - T_{S\_1\%} \tag{3.16}$$

As seen in Fig. 3.3(a)-(d), two windows for T_S at 0.01% (yellow solid line) and at 1% (yellow dashed line) have been defined. To be able to explicitly see how the settling time is improving as we move to the scaled-down technologies; Fig. 3.4 shows the $T_{S\_degradation}$, given by Eqn. (3.16), with respect to the CMOS technology nodes. For different cases of the positions of the P-Z pair, and for different technology nodes, the results are consistent with the claim that the

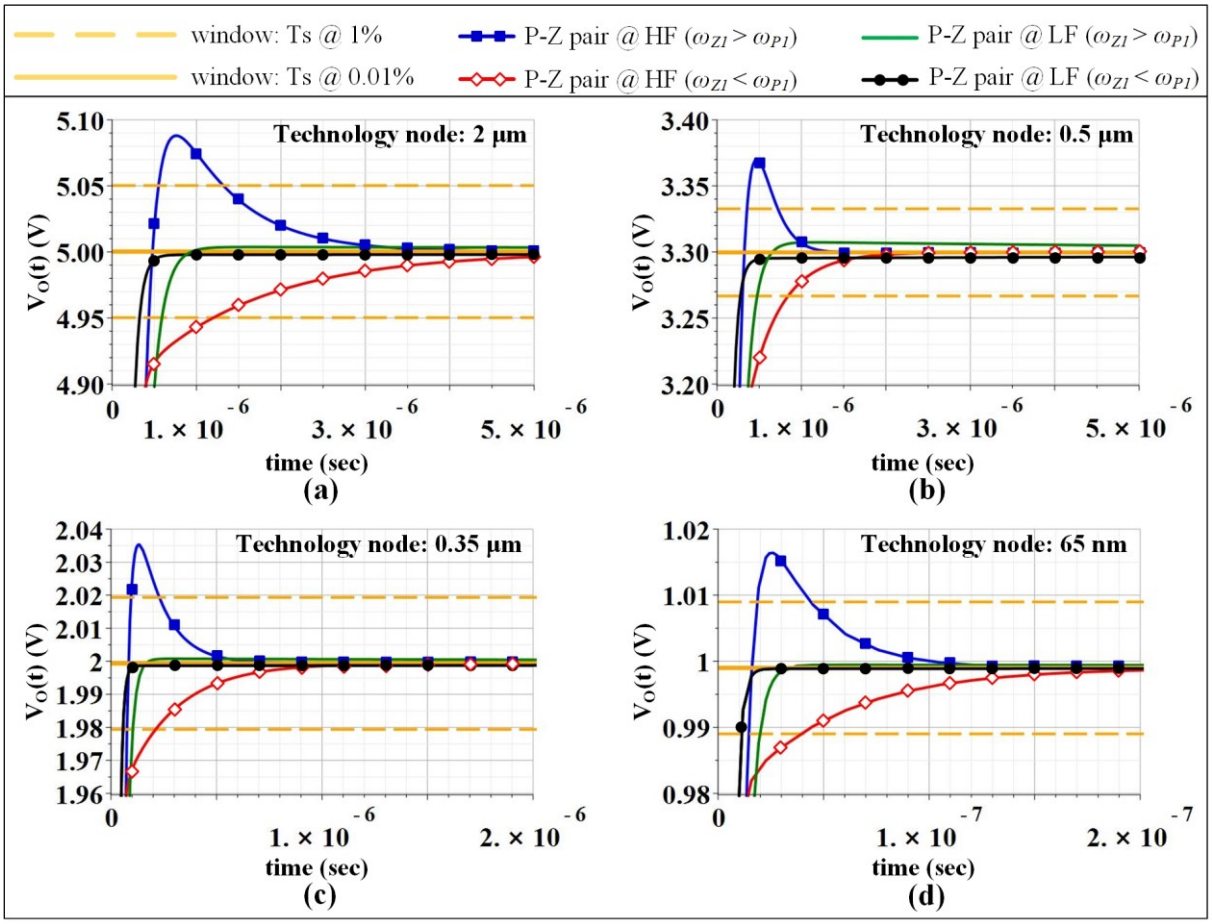

Fig. 3.3: The closed-loop simulation results of the unity-gain step responses for the 4 different cases of the P-Z pair frequency positions for the four CMOS technology nodes: (a) 2 µm, (b) 0.5 µm, (c) 0.35 µm, and (d) 65 nm.

degradation in the settling time is insignificant in the scaled-down CMOS technologies. According to Fig. 3.4, the maximum improvement in the $T_{S\_degradation}$ is for the case of having the *P-Z* pair at LF ($\omega_{Z1} < \omega_{P1}$); where using the 65 nm technology gives a $T_{S\_degradation}$ that is about 300 times less than the $T_{S\_degradation}$ of using the 2 µm technology. Also, as depicted from Fig. 3.4, the minimum improvement in the $T_{S\_degradation}$ is for the case of having the *P-Z* pair at HF ($\omega_{Z1} > \omega_{P1}$); where using the 65 nm technology gives a $T_{S\_degradation}$ that is about 130 times less than the $T_{S\_degradation}$ of using the 2 µm technology.

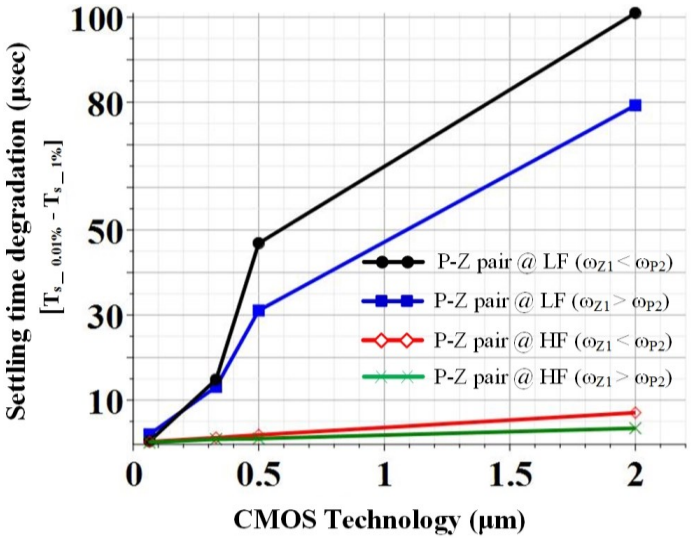

Fig. 3.4: The settling time degradation in the step response vs. the CMOS technology node for the 4 different cases of the open-loop P-Z pair frequency positions.

In the light of these issues which have been discussed in subsection 3.1.1 and 3.1.2, there remains to be a timely need for a generalized analysis using all open-loop independent parameters to examine the actual impact of having a *P-Z* pair below the unity-gain frequency.

3.2. Demystifying the Relationship Between Frequency Response and Settling Time Having One Pole-Zero Pair

The proposed analysis in this section will include all open-loop independent parameters of Eqn. (3.1). However, OTAs are usually required to operate over a large range of frequency conditions. Rather than design a new *TF* for each case, a better approach is to normalize the *TF* to reduce the degree of complexity as discussed in Appendix B.

Based on the results found in Appendix B, the open loop *TF* of Eqn. (3.1) can be written using the normalized approach (where the "*s*" Laplace variable will be replaced with the "*p*" Laplace variable) as

$$A(p) = \frac{A_Z}{p} * \frac{(1 + p)}{\left(1 + \frac{p}{\omega_P}\right)} \tag{3.17}$$

where A_Z is the gain at the new position of ω_{Z1} after normalization (i.e., after setting the compensation zero ω_{Z1} at 1 rad/s), and ω_P is the new position of the compensation pole ω_{P1} after this normalization, and it is unitless. Also, the frequency-normalized unity-gain frequency (Ω_t) can be written in terms of the open-loop parameters for all values of ω_P as

$$\Omega_t = A_Z \,.\, \omega_P \tag{3.18}$$

Ultimately, the OTA will be used in a closed-loop configuration where the impact of the open-loop frequency-response parameters will be revealed. Once applying an input step while having the OTA in closed-loop unity configuration, the OTA's settling time can be examined. Therefore, in the next subsections, the close-loop response will be discussed to precisely identify how to control the closed-loop parameters based on the open-loop response. Then, the generalized relationship between frequency response and settling time will be derived after investigating the 2-stage OTA's unity step response having the *P-Z* pair below Ω_t.

3.2.1. Analyzing the Closed-Loop Frequency-Response in the Presence of *P-Z* Doublets

If the open-loop *TF* includes a *P-Z* pair as described by Eqn. (3.17), then the unity-gain closed-loop *TF*, *T(p)*, (i.e., having unity-feedback factor) would appear as

$$T(p) = \frac{(1 + p)}{\left(1 + \frac{p}{\omega_{CL,1}}\right)\left(1 + \frac{p}{\omega_{CL,2}}\right)} \tag{3.19}$$

where $\omega_{CL,1}$ and $\omega_{CL,2}$ are the poles of the closed-loop configuration after normalization. As $A_Z >> \omega_P$, $\omega_{CL,1}$ and $\omega_{CL,2}$ will be widely spaced apart. Further, using the quadratic formula for a 2nd-order polynomial, as clarified in Appendix C, one can find that:

$$\omega_{CL,1} = A_Z\, \omega_P \;\approx\; \Omega_t \tag{3.20}$$

and

$$\omega_{CL,2} \;\approx \frac{A_Z}{1 + A_Z} + \frac{1}{A_Z \omega_P} \qquad . \tag{3.21}$$

Here one of the poles of the closed-loop system will be located at $A_Z\, \omega_P$ (i.e., Ω_t) and the other one is located very close to 1 rad/s (i.e., the normalized frequency location of ω_{Z1}). The residual *LF* closed-loop pole ($\omega_{CL,2}$) depends on A_Z, when A_Z is large, and on $1/(A_Z\omega_P)$, when ω_P is very small (i.e., $\omega_P < 1$).

Going forward, the frequency difference between the *P-Z* doublet (i.e., the *LF* closed-loop pole ($\omega_{CL,2}$) and the zero at 1 rad/s) will be denoted with the term δ_{CL}. Assuming the compensation pole can take on values either larger than unity or less than unity, the *closed-loop pole-zero doublet separation distance (δ_{CL})* can be written as

$$\delta_{CL} = \; \omega_{CL,2} - 1 \qquad . \tag{3.22}$$

By substituting the expression of $\omega_{CL,2}$, seen in Eqn. (3.21), into Eqn. (3.22), δ_{CL} can be re-written as

$$\delta_{CL} \approx \; \frac{1}{A_Z \omega_P} - \frac{1}{A_Z} = \; \frac{1 - \; \omega_P}{A_Z \omega_P} \qquad . \tag{3.23}$$

For many situations, the compensation pole ω_P is either much greater than unity or much less than unity. As such, the closed loop *P-Z* doublet separation distance can be approximated as

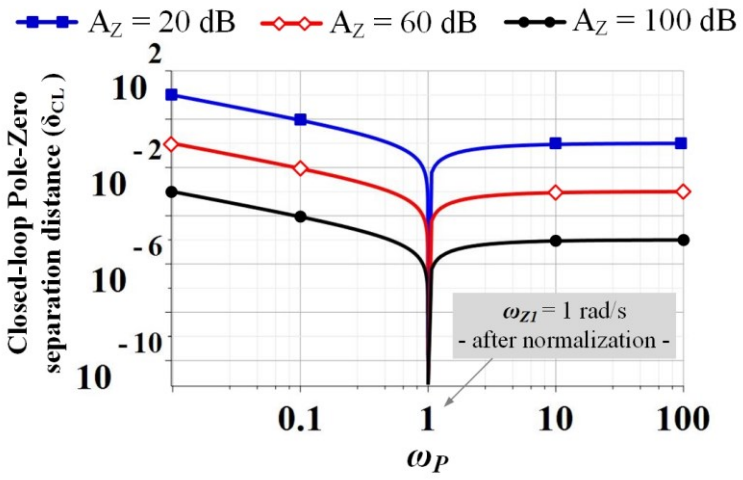

Fig. 3.5: The closed-loop P-Z separation distance (δ_{CL}) as a function of ω_P for different values of A_Z.

$$\delta_{CL} = \begin{cases} \dfrac{1}{A_Z\,\omega_P}, & \omega_P \ll 1 \\ -\dfrac{1}{A_Z}, & \omega_P \gg 1 \end{cases} . \qquad (3.24)$$

Fig. 3.5 plots the behavior of δ_{CL} (according to Eqn. (3.23) and (3.24)) for a sweep of ω_P between 0.01 and 100, for different values of A_Z. As depicted form Fig. 3.5, controlling δ_{CL} can be done through two independent parameters: A_Z and ω_P. To reduce δ_{CL} one can target higher A_Z regardless of the value of ω_P. However, the minimum possible value of δ_{CL}, when controlling its value through ω_P, can be achieved when ω_P = 1 rad/s, which is the position of ω_{ZI} after normalization. Nevertheless, the optimum value of δ_{CL} will be determined by the design requirements as will be discussed in chapter 4. This shows that the open-loop *P-Z* pair separation ratio (i.e., ω_{PI}/ω_{ZI} before normalization and $\omega_P/1$ after normalization) is a parameter that affects δ_{CL} as previously reported in other works [60-63]. But what has not been reported previously (due to technology limitations) is that increasing ω_P (i.e., ω_{PI}/ω_{ZI}) beyond certain values (i.e., $\omega_P \geq 10$), will have no effect on δ_{CL}, as seen in Fig. 3.5. Also, the zero gain (A_Z) plays a critical role

in controlling the value of δ_{CL}. In the next subsection, these relationships will show how to reduce the effects of having the *P-Z* doublets on the settling time of two-stage OTAs (i.e., when having one *P-Z* pair).

3.2.2. The Relationship between Settling Time and Open-Loop Frequency-Response Parameters

Based on the results found in Eqs. (3.20), (3.21) and (3.24), and as derived in Appendix D, the unit step response can be simplified as

$$y(t) = 1 - \left(1 + \frac{1 - \omega_P}{A_Z\,\omega_P}\right) e^{-A_Z\omega_P\,t} + \left(\frac{1 - \omega_P}{A_Z\,\omega_P}\right) e^{-\left(1+\frac{1-\omega_P}{A_Z\omega_P}\right)t} \tag{3.25}$$

This expression will hold over a wide range of ω_P and A_Z, regardless of their values. However, Eqn. (3.25) can be written for different cases of ω_P as follows:

$$y(t) = \begin{cases} 1 - \left(1 - \dfrac{1}{A_Z}\right) e^{-A_Z\omega_P\,t} - \left(\dfrac{1}{A_Z}\right) e^{-\left(1-\frac{1}{A_Z}\right)t}, & \omega_P \gg 1 \\ 1 - e^{-A_Z\,t}, & \omega_P = 1 \\ 1 - \left(1 + \dfrac{1}{A_Z\omega_P}\right) e^{-A_Z\omega_P\,t} + \left(\dfrac{1}{A_Z\omega_P}\right) e^{-\left(1+\frac{1}{A_Z\omega_P}\right)t}, & \omega_P \ll 1 \end{cases} \tag{3.26}$$

Showing such wide range impact of ω_P and A_Z has not been discussed in the previously reported analyses, hence, Eqn. (3.26) represents the generalized relationship between frequency response and time response having one *P-Z* doublet. It also shows all independent parameters through which one can reduce the impact of the *P-Z* doublet on the step response.

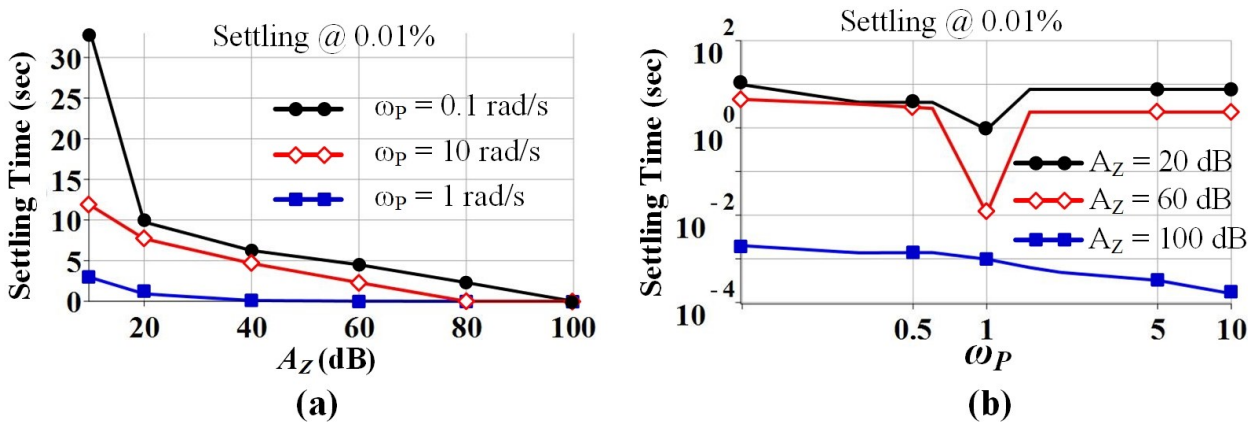

Fig. 3.6: The proposed theory results having one *P-Z* pair: (a) settling time as a function of A_Z for different ω_P when the steps settles @ 0.01% of the final value, based on the step-response result of Eqn. (3.26), and (b) settling time as a function of ω_P for different A_Z when the steps settles @ 0.01% of the final value, based on the step-response result of Eqn. (3.25).

Based on Eqn. (3.26), Fig. 3.6(a) shows the settling time as a function of A_Z for different values of ω_P. This figure reports the settling time at 0.01% of the final value, as it is usually the minimum required settling time different applications [60]. As seen in Fig. 3.6(a), the settling time, when $\omega_P >> 1$ (i.e., red line), is lower than the settling time when $\omega_P << 1$ (i.e., black line). Also, as A_Z reaches 80 dB, the settling time, when $\omega_P >> 1$, will have almost similar values of having ω_P at 1 (i.e., full *P-Z* cancellation). This impact of high A_Z (i.e., having a *LF* zero) on enhancing the OTA's settling time has not been reported in previous works.

Similarly, and unlike the previously reported works, Fig. 3.6(b) shows the settling time but this time as a function of ω_P for different values of A_Z. When A_Z = 100 dB, the settling time is no longer affected by the open-loop *P-Z* pair separation (i.e., $\omega_P/1$), which suggests that at high A_Z, the response settles to its final value before the impact of *P-Z* doublets starts. Interestingly, for A_Z = 100 dB, when increasing ω_P, the response will exhibit faster settling times.

Clearly, some values of A_Z might be hard to achieve practically when cascading 2 or 3 gain-stages. Therefore, one can position ω_P at values near 1 to reduce δ_{CL}, which in return, will reduce the impact of the closed-loop *P-Z* doublet. However, when using many gain-stages ($N \geq 4$), A_{DC} will be larger, and these values for A_Z are easy to achieve if the zero is positioned at *LF*, where A_{DC} is proportional to A_Z.

To conclude this section and clarify the new proposed observations, it is readily apparent from Eqs. (3.24) and (3.26) that a higher A_Z forces two things to occur: (1) The coefficient in front of the *LF* term of the unit-step response will reduce in magnitude, and (2) the separation distance between the closed-loop *P-Z* doublet will also reduce in magnitude. These two things will help reducing the delay caused by the presence of the *P-Z* doublets.

3.3. Generalized Relationship between Frequency Response and Settling Time Having *N*-1 Pole-Zero Pairs

For *N*-Stage CMOS OTAs the analysis's degree of complexity will increase, where each stage will add a *P-Z* pair. For example, when $N = 3$, the OTA will have two *P-Z* pairs (i.e., ω_{P1}, ω_{Z1}, ω_{P2}, and ω_{Z2}). There are 24 different cases to position and arrange the two *P-Z* pairs. Therefore, to simplify the analysis, one can start with the bilinear *TF* of the normalized N^{th}-order integrator-based OTAs with zero-only compensator. This *TF* is derived in a manner similar to that used with Eqn. (3.17) in Appendix B, and can be written as

$$A(p) = \frac{A_Z}{p^N} \times (1 + p)^{N-1} \quad . \tag{3.27}$$

Thus, in the following subsections, the closed-loop analysis and the step response will be discussed based on Eqn. (3.27). Then, the results will be expanded while having pole-zeros compensator instead of having zeros-only compensator. To the best of the author's knowledge, these proposed analyses with $N > 2$ have not been discussed in literature before.

3.3.1. Closed-Loop Analysis Having a Zeros-Only Compensator

Based on Eqn. (3.27), the unity-gain closed-loop *TF* can be written as

$$T(p) = \frac{A_Z\,(1+\,p)^{N-1}}{p^N + A_Z\,(1+\,p)^{N-1}} \quad . \tag{3.28}$$

Using the binomial theorem, the above N^{th}-order *TF* can be rewritten in general form as follows

$$T(p) = \frac{A_Z\left[\binom{N-1}{N-1}p^{N-1} + \binom{N-1}{N-2}p^{N-2} + \binom{N-1}{N-3}p^{N-3} + \cdots + \binom{N-1}{1}p^1 + \binom{N-1}{0}\right]}{p^N + A_Z\left[\binom{N-1}{N-1}p^{N-1} + \binom{N-1}{N-2}p^{N-2} + \binom{N-1}{N-3}p^{N-3} + \cdots + \binom{N-1}{1}p^1 + \binom{N-1}{0}\right]} \tag{3.29}$$

Owing to the nature of the *LHP* zeros located at frequencies of 1 rad/s, all but one of the N closed-loop poles will move towards these zeros with individual separation distances of $\delta_{CL,i}$ for $i = 1$ to $N\text{-}1$. The N^{th} pole will be positioned essentially at Ω_t.

To illustrate this, consider the closed-loop poles distributions in Table 3.2 for the particular case of A_Z = 80 dB across orders ranging from N = 3 to 5. The pole-zero separation distance ($\delta_{CL,i}$) is computed by taking the exact differences between the zero (i.e., zeros frequencies = -1 rad/s) and the pole positions in the p-plane.

TABLE 3.2
CLOSED-LOOP POLES DISTRIBUTION AND THE POLE-ZERO SEPARATION DISTANCE ($\delta_{CL,i}$) VERSUS NUMBER OF STAGES (N) FOR ZEROS-ONLY COMPENSATOR WITH A_Z = 80 dB (i.e., Ω_t = 10^4 rad/s)

N	**closed-loop poles' frequencies (rad/s)**					**Pole-Zero separation distance ($\delta_{CL,i}$)**			
	$\omega_{CL,1}$	$\omega_{CL,2}$	$\omega_{CL,3}$	$\omega_{CL,4}$	$\omega_{CL,5}$	$\delta_{CL,1}$	$\delta_{CL,2}$	$\delta_{CL,3}$	$\delta_{CL,4}$
3	- 1.0101	-0.99014	- 9997.9	-	-	0.0101	- 0.00986	-	-
4	- 1.0495	- 0.97554 + j0.03772	- 0.9755 - j0.0377	- 9996.9	-	0.04950	- 0.0244 +j0.0377	- 0.0244 -j0.0377	-
5	- 1.1145	- 0.91099	- 0.9877 +j0.0987	- 0.9877- j0.0987	- 9995.9	0.1145	-0.0890	- 0.0122 + j0.098	- 0.0122 +j0.098

It is interesting that some entries in Table 3.2 have complex coefficients and pole locations. The presence of these complex terms or poles is discussed in Appendix E.

Owing to the presence of the *N-1* coincident zeros in the open-loop response, the *N-1* poles of the closed-loop system will move very close to the same frequency locations as these zeros but will not overlap. In a manner similar to the previous two-stage case (i.e., having one *P-Z* pair), we shall denote the small separation distance between the i^{th}-pole and the i^{th}-zero of the closed-loop system by $\delta_{CL,i}$. The remaining closed-loop pole will appear at frequency Ω_t (where $\Omega_t = A_Z$). Consequently, the closed-loop *TF* can be approximated as

$$T(p) = \frac{(1+p)^{N-1}}{\left(1+\frac{p}{A_Z}\right)\prod_{i=1}^{N-1}\left[1+\frac{p}{(1+\delta_{CL,i})}\right]} \quad . \quad (3.30)$$

3.3.2. Unit Step-Response Having a Zeros-Only Compensator

With the denominator polynomial of the *TF* of Eqn. (3.30) described in factor form, the step-response can easily be found by converting the *TF* to partial fraction form, then taking the inverse Laplace transform, resulting in

TABLE 3.3
APPROXIMATE EXPRESSIONS OF STEP RESPONSE COEFFICIENTS FOR DIFFERENT NUMBER OF STAGES *(N)* WITH ZEROS-ONLY COMPENSATOR HAVING $A_Z = 80$ dB (i.e. $\Omega_t = 10^4$ rad/s)

N	3	4	5
k_1	$-\delta_{CL,1}^2 \frac{(1+\delta_{CL,2})}{(\delta_{CL,1}-\delta_{CL,2})}$	$-\delta_{CL,1}^3 \frac{(1+\delta_{CL,2})(1+\delta_{CL,3})}{(\delta_{CL,1}-\delta_{CL,2})(\delta_{CL,1}-\delta_{CL,3})}$	$-\delta_{CL,1}^4 \frac{(1+\delta_{CL,2})(1+\delta_{CL,3})(1+\delta_{CL,4})}{(\delta_{CL,1}-\delta_{CL,2})(\delta_{CL,1}-\delta_{CL,3})(\delta_{CL,1}-\delta_{CL,4})}$
k_2	$-\delta_{CL,2}^2 \frac{(1+\delta_{CL,1})}{(\delta_{CL,2}-\delta_{CL,1})}$	$-\delta_{CL,2}^3 \frac{(1+\delta_{CL,1})(1+\delta_{CL,3})}{(\delta_{CL,2}-\delta_{CL,1})(\delta_{CL,2}-\delta_{CL,3})}$	$-\delta_{CL,2}^4 \frac{(1+\delta_{CL,1})(1+\delta_{CL,3})(1+\delta_{CL,4})}{(\delta_{CL,2}-\delta_{CL,1})(\delta_{CL,2}-\delta_{CL,3})(\delta_{CL,2}-\delta_{CL,4})}$
k_3	-	$-\delta_{CL,3}^3 \frac{(1+\delta_{CL,1})(1+\delta_{CL,2})}{(\delta_{CL,3}-\delta_{CL,1})(\delta_{CL,3}-\delta_{CL,2})}$	$-\delta_{CL,3}^4 \frac{(1+\delta_{CL,1})(1+\delta_{CL,2})(1+\delta_{CL,4})}{(\delta_{CL,3}-\delta_{CL,1})(\delta_{CL,3}-\delta_{CL,2})(\delta_{CL,3}-\delta_{CL,4})}$
k_4	-	-	$-\delta_{CL,4}^4 \frac{(1+\delta_{CL,1})(1+\delta_{CL,2})(1+\delta_{CL,3})}{(\delta_{CL,4}-\delta_{CL,1})(\delta_{CL,4}-\delta_{CL,2})(\delta_{CL,4}-\delta_{CL,3})}$

$$y(t) \approx 1 - \prod_{i}^{N-1}\left(1+\delta_{CL,i}\right) e^{-A_Z t} + \sum_{i}^{N-1} k_i \; e^{-(1+\delta_{CL,i})t} \quad , \tag{3.31}$$

where the k_i-coefficients are the *LF* frequency exponential term coefficients, and can be approximated as follows:

$$k_i \approx {\delta_{CL,i}}^{N-1} \times \frac{\prod_{m=1,m\neq i}^{N-1}\left(1+\delta_{CL,m}\right)}{\prod_{m=1,m\neq i}^{N-1}\left(\delta_{CL,i} - \delta_{CL,m}\right)} \quad . \tag{3.32}$$

Table 3.3 provides a summary of the approximate values of the step-response k_i-coefficients for stages ranging from 3 to 5 with A_Z = 80 dB. In all cases, the need for values for $\delta_{CL,i}$ is readily apparent. While no simple expression of the individual pole-zero separation distances $\delta_{CL,i}$ have yet been found, empirical evidence suggests the following general relationship:

$$\delta_{CL,i} \approx \frac{1}{\sqrt[N-1]{A_Z}}, \quad i = 1 \ldots N-1 \quad . \tag{3.33}$$

While it was shown previously that a single closed-loop *P-Z* separation distance was inversely proportional to A_Z, the above statement suggests that this gain must be spread equally across all

P-Z combinations. To illustrate this statement, for A_Z = 80 dB, $\delta_{CL,1}$ = 0.010 at N = 3, $\delta_{CL,1}$ = 0.0464 at N = 4, and $\delta_{CL,1}$ = 0.1000 at N = 5. Scanning the $\delta_{CL,1}$ of Table 3.2 that lists the *P-Z* separation distances as a function of *TF* order, one can see that the above results correlate quite well with the theory captured by Eqn. (3.33).

Using the above principle of $\delta_{CL,i}$ suggested by Eqn. (3.33), the unit-step response of the N^{th}-order closed-loop *TF* can be approximated with the following expression:

$$y(t) \approx 1 - \left(1 + \frac{1}{\sqrt[N-1]{A_Z}}\right) e^{-A_Z t} + \sum_{i=1}^{N-1} \frac{1}{\sqrt[N-1]{A_Z}} \; e^{-\left(\frac{\sqrt[N-1]{A_Z}+1}{\sqrt[N-1]{A_Z}}\right)t}. \tag{3.34}$$

Table 3.4 illustrates how the unit step response behavior changes with increasing A_Z for a 3-stage OTA as found by an exact analysis. Fig. 3.7 provides a plot of the exponential terms in the unit step response for orders ranging from N = 3 to 5. As is evident from all three plots, all coefficients decrease in magnitude with increasing A_Z (or alternatively, increasing gain at 1 rad/s). Depending on the order of the TF, the contribution of each *LF* exponential term will vary. The lower the order, the smaller its overall contribution. To see this more clearly, pick one A_Z value from Fig. 3.7, say 100 dB and observe the worst-case coefficient values across all three orders. From Fig. 3.7, these would be approximately (3-stage, $2\text{x}10^{-3}$), (4-stage, $8\text{x}10^{-3}$) and (5-stage, $1\text{x}10^{-2}$) – clearly increasing in value with increasing order in accordance with the relationship suggested by Eqn. (3.33).

Fig. 3.8 shows the impact of increasing A_Z on settling time for different number of *P-Z* pairs (i.e., N = 2 to 8) based on Eqn. (3.34). As seen in Fig. 3.8(a) and (b), settling time is decreasing as A_Z increases for different percentages of settling time. Again, this implies that the impact of

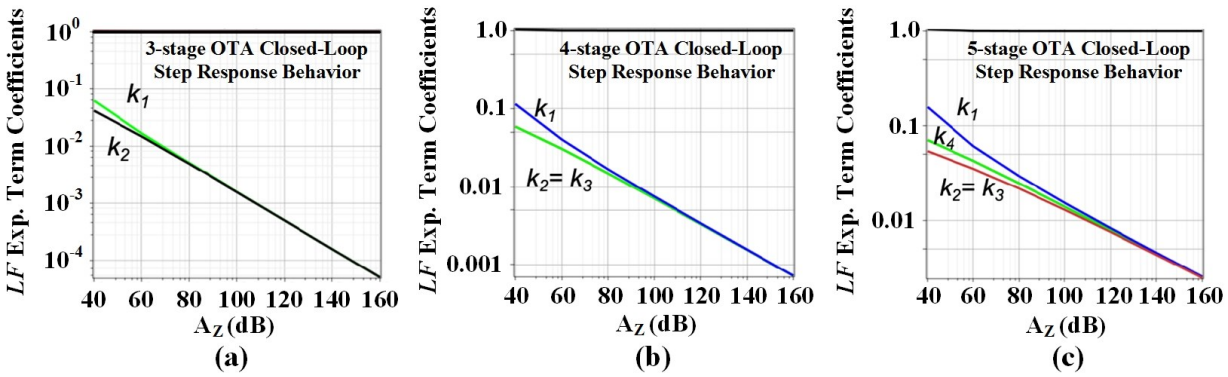

Fig. 3.7: Coefficient weights (k_i) of *LF* exponential terms of unit-step response of closed-loop system involving an OTA with Zeros-Only Compensator for number of stages ranging from 3 to 5: (a) 3-stages, (b) 4-stages and (c) 5-stages.

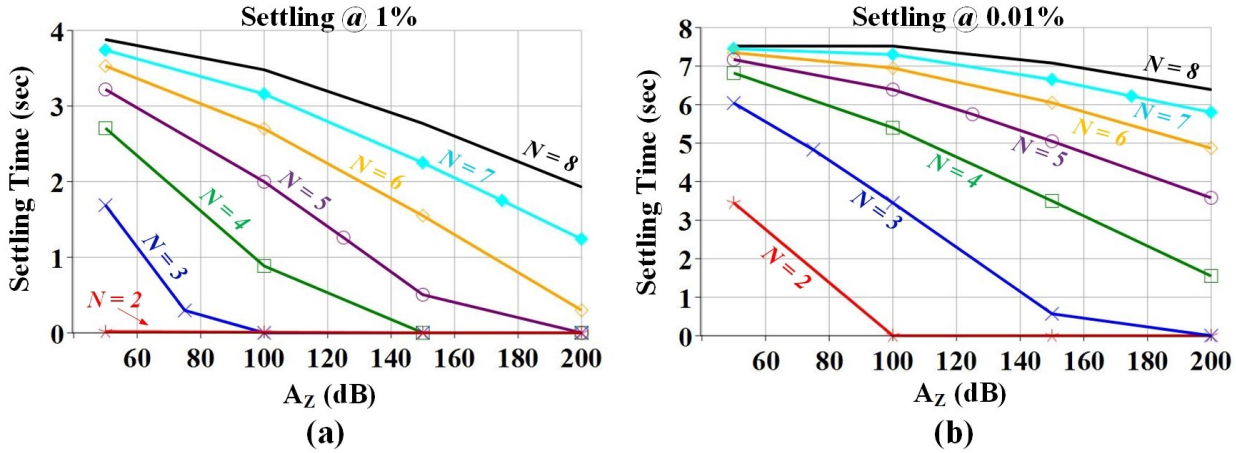

Fig. 3.8: The relationship between settling time and A_Z for different numbers of P-Z pairs: (a) settling at 1% of final value, and (b) settling at 0.01% of final value.

TABLE 3.4
UNIT STEP RESPONSE BEHAVIOR FOR 3-STAGE OTA WITH ZEROS-ONLY COMPENSATOR FOR INCREASING A_Z

Az (dB)	Step Response
40	$1.000000 - 1.021060\, e^{-97.968956\, t} + 0.062842\, e^{-1.118252\, t} - 0.041782\, e^{-0.912792\, t}$
60	$1.000000 - 1.002010\, e^{-997.996990\, t} + 0.016886\, e^{-1.033211\, t} - 0.014876\, e^{-0.969799\, t}$
80	$1.000000 - 1.000200\, e^{-9997.999700\, t} + 0.005102\, e^{-1.010153\, t} - 0.004902\, e^{-0.990147\, t}$
100	$1.000000 - 1.000020\, e^{-99997.999970\, t} + 0.001591\, e^{-1.003177\, t} - 0.001571\, e^{-0.996853\, t}$

closed-loop *P-Z* separation distances can be highly reduced with higher gain, regardless of how many *P-Z* pairs the OTA might have or what is the exact separation distance between them.

Also, to measure the improvement, one can compare the settling time at 0.01% of the final value to the settling time at 1% for each stage, where this was the main issue of having *P-Z* doublets as stated in [60]. But, in [60], the impact of the *P-Z* doublets has been discussed having only one *P-Z* pair. However, by adding more *P-Z* pairs (when increasing the number of stages) it is important to consider the impact of these extra *P-Z* pairs compared to having one *P-Z* pair. Consequently, the Improvement Metric (*IM*) can be given by

$$IM = \frac{Settling\ time\ @\ 0.01\ \%}{Settling\ time\ @\ 1\ \%} \times \frac{1}{N-1} \quad , \tag{3.35}$$

where (*N*-1) represents the number of *P-Z* pairs/doublets the OTA will have in its frequency range of operation. Table 3.5 shows the settling time results which are obtained based on Eqn. (3.34) and Fig. 3.8. Based on these results, Fig. 3.9 shows how the impact of the *P-Z* pairs (i.e., *IM* of Eqn. (3.35)) is decreasing when increasing A_Z.

In conclusion, through the appropriate selection of the A_Z parameter in the OTA open-loop response as described by Eqn. (3.27), *the zeros of the compensator can be placed at low frequency to enhance the performance attributes of the closed-loop system provided that the open-loop gain at a normalized frequency of 1 rad/s is high enough for the given application.*

3.3.3. Analysis Having Pole-Zeros' Compensator

The analysis steps of the previous subsections will be followed here again, but with the assumption that an OTA's *N*-stage open-loop *TF* is described as follows:

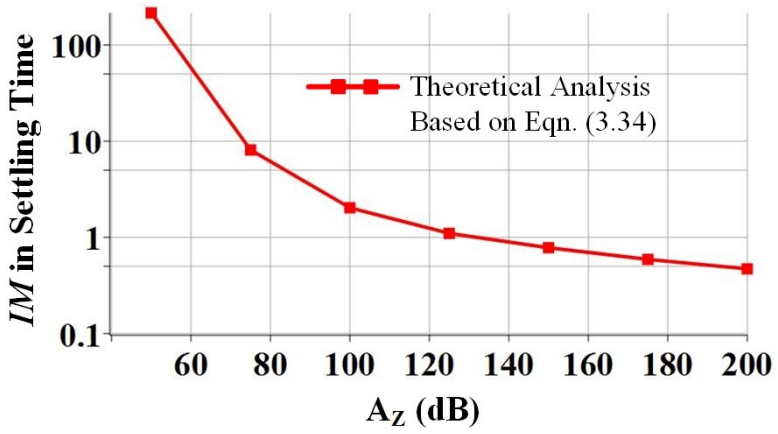

Fig. 3.9: The Improvement Metric (*IM*) in settling time when increasing the gain based on Eqn. (3.34).

TABLE 3.5
THE IMPACT OF GAIN AND NUMBER OF *P-Z* PAIRS ON SETTLING TIME WHICH IS EXPRESSED BY *IM*

Metric	**N = 2**	**N = 3**	**N = 4**	**N = 5**	**N = 6**	**N = 7**	**N = 8**
Gain: AZ (dB)	**50**	**75**	**100**	**125**	**150**	**175**	**200**
Settling time @ 1% (sec)	0.016	0.297	0.885	1.26	1.55	1.75	1.93
Settling time @ 0.01% (sec)	3.45	4.83	5.4	5.75	6.05	6.22	6.39
***IM in settling time* (theory)**	**215.6**	**8.1**	**2.03**	**1.1**	**0.78**	**0.59**	**0.47**

$$A(p) = \frac{A_Z}{p^{N-1}} \times \frac{(1+p)^{N-1}}{\left(1+\frac{p}{\omega_P}\right)} \quad , \tag{3.36}$$

where there are *N-1* poles at DC and one at a frequency of ω_P. Here it is assumed that ω_P is greater than but not equal to 1. Subsequently, the unity-gain closed-loop *TF* can be written in no particular form as

$$T(p) = \frac{A_Z\,(1+p)^{N-1}}{p^{N-1}\left(1+\frac{p}{\omega_P}\right) + A_Z\,(1+p)^{N-1}} \quad . \tag{3.37}$$

Owing to the presence of the *LHP* zeros at 1 rad/s, Eqn. (3.37) can be approximated with a pole at $A_Z \times \omega_P$ (unity-gain frequency for the integrator cascade with zeros-pole compensator) and *N-1* poles located very close to 1 rad/s, as follows

$$T(p) = \frac{(1+p)^{N-1}}{\left(1+\frac{p}{A_Z\omega_P}\right)\prod_{i=1}^{N-1}\left[1+\frac{p}{(1+\delta_{CL,i})}\right]} \quad . \tag{3.38}$$

Once again, the poles located near 1 rad/s are represented by an error term representing the distance the closed-loop pole is from the zeros at 1 rad/s. In a manner very similar to the discussion for the zero-only compensator of the previous section, the separation distances $\delta_{CL,i}$ can be expressed in terms of the gain of the open-loop TF at 1 rad/s as in Eqn. (3.33). While the expression for the $\delta_{CL,i}$ is the same as the zeros-only compensator, the gain of the open-loop *TF* at 1 rad/s is different in general.

On the other hand, the unit step response takes on the exact same form as the Nth-order integrator with zeros-only compensator except that the *HF* time constant is a product of A_Z and ω_P instead of A_Z, i.e.,

$$y(t) \approx 1 - \prod_{i}^{N-1}\left(1+\delta_{CL,i}\right)e^{-(A_Z\omega_P)\,t} + \sum_{i}^{N-1} k_i\, e^{-(1+\delta_{CL,i})t} \quad , \tag{3.39}$$

where the k_i-coefficients are approximated as in Eqn. (3.32). Table 3.3 also provides a summary of the approximate values of the step-response k_i-coefficients for orders ranging from N = 3 to 5 when A_Z = 80 dB. The magnitude of the *LF* exponential terms over a frequency range of A_Z

TABLE 3.6
UNIT STEP RESPONSE BEHAVIOR FOR 3-STAGE OTA WITH POLE-ZEROS COMPENSATOR (WITH ω_P = 10) FOR INCREASING A_Z

A_Z(dB)	Step Response
40	$1-(0.004-j0.047)e^{(-0.992-j0.094)t}-(0.004+j0.047)e^{(-0.992+j0.094)t}-0.992e^{-1008.017t}$
60	$1-(0.000-j0.015)e^{(-0.999-j0.03)t}-(0.000+j0.015)e^{(-0.999+j0.03)t}-0.999e^{-10008.002t}$
80	$1-(0.000-j0.005)e^{(-1.00-j0.009)t}-(0.000+j0.005)e^{(-1.000+j0.009)t}-1.000e^{-100008.00t}$
100	$1-(4.0\times10^{-6}-j0.001)e^{(-1.0-j0.003)t}-(4.0\times10^{-6}+j0.001)e^{(-1.0+j0.003)t}-1.0e^{-1.0\times10^{6}t}$

ranging from 20 dB to 160 dB (with ω_P set to 10) exhibits similar behavior of the one shown in Fig. 3.7. In other words, the *LF* exponential terms has a monotonically decreasing behavior with increasing A_Z.

A more effective method is to work with the exact *TF* under specific parametrization and perform an inverse-Laplace transform on it and collect the unit step response. The sequence of operations was performed with the open-loop *TF* described by Eqn. (3.36) for N = 2 in Section 3.2. But, for N = 3, ω_P = 10 and by sweeping A_Z from 40 dB to 100 dB, the results are summarized in Table 3.6. It is interesting to note that the location of the compensation pole has little effect on the magnitude of coefficients of the *LF* exponential terms. Some small change is evident but nothing significant. However, the compensation pole does affect the High-Frequency (*HF*) time constant, as it adds directly with the A_Z parameter of the integrator section.

Using the above principle of pole-zero separation distances suggested by Eqn. (3.33), the unit-step response of the N^{th}-order closed-loop *TF* (Pole-Zeros compensation) can be approximated with the following expression:

$$y(t) = \begin{cases} 1 - \left(1 - \frac{1}{\sqrt[N-1]{A_Z}}\right) e^{-A_Z \omega_P t} - \sum_{i=1}^{N-1} \frac{1}{\sqrt[N-1]{A_Z}} \; e^{-\left(\frac{\sqrt[N-1]{A_Z}+1}{\sqrt[N-1]{A_Z}}\right)t} & , \omega_P \gg 1 \\ 1 - \left(1 + \frac{1}{\sqrt[N-1]{A_Z}}\right) e^{-A_Z \omega_P t} + \sum_{i=1}^{N-1} \frac{1}{\sqrt[N-1]{A_Z}} \; e^{-\left(\frac{\sqrt[N-1]{A_Z}+1}{\sqrt[N-1]{A_Z}}\right)t} & , \omega_P \ll 1 \end{cases} \quad (3.40)$$

The same conclusion can be stated here; even if the poles are not at DC, once the zeros are positioned at *LF*s with higher DC gains, the impact of $\delta_{CL,i}$ will become insignificant and the step response will follow the same behavior of Eqn. (3.40).

3.4. Summary

By revisiting the previously reported analysis on the impact on *P-Z* pair on the settling time of CMOS OTAs, one can conclude that there remains to be a timely need for a generalized analysis using all open-loop independent parameters to examine the actual impact of having a *P-Z* pair below the unity-gain frequency.

On doing so, it was readily apparent from Eqs. (3.24) and (3.26) that the low-frequency zero gain (A_Z) has a critical role in reducing the impact of *P-Z* doublets on the closed-loop response of OTAs. In other words, a higher A_Z forces two things to occur: (1) The coefficient in front of the *LF* term of the unit-step response will reduce in magnitude, and (2) the separation distance between the closed-loop *P-Z* doublet will also reduce in magnitude. These two things will help reducing the delay caused by the presence of the *P-Z* doublets. **Fig. 3.5 and Fig. 3.6 captured this impact of A_Z on settling time.**

Then, by expanding the analysis having *N*-1 *P-Z* pairs, it was shown that through the appropriate selection of the A_Z parameter in the OTA open-loop response as described by Eqn. (3.27) and (3.36), the zeros of the compensator can be placed at low frequency to enhance the performance attributes of the closed-loop system provided that the open-loop gain at a normalized frequency of 1 rad/s is high enough for the given application. In other words, once the zeros are positioned at *LF*s with higher DC gains, the impact of $\delta_{CL,i}$ (given by Eqn. (3.33)) will become insignificant and the step response will follow the behavior of Eqn. (3.40). **Fig. 3.9 captured the improvement in settling time once positioning the zeros at low frequencies to achieve higher A_Z values.**

In conclusion, the proposed theory suggests that once increasing A_Z (by increasing A_{DC} and/or positioning the zeros at low frequencies) the open-loop *P-Z* pairs' impact on settling time will be reduced, regardless of open-loop *P-Z* pairs' numbers or their separation distances (i.e., ω_{P1}/ω_{Z1}). Thus, to verify the proposed theory, one should design an OTA which can provide a wide range of DC gains. At the same time, this OTA should have the capability to create a specific number of *P-Z* pairs and offers the capability to control their positions. This will be the central discussion in Chapter 4 and Chapter 5, as the proposed theory will be validated and verified through a design example that also demonstrates how the generalized theory unveils opportunities for many-stage OTA design.

CHAPTER 4

A SCALABLE MANY-STAGE CMOS OTA WITH A WIDE C_L-DRIVABILITY RANGE

Based on the proposed theory in Chapter 3, this Chapter introduces a many-stage CMOS OTA design technique that allows cascading identical gain stages (for arbitrarily scalable high DC gain) while driving an ultra-wide range of capacitive loads. At the heart of the proposed design is a new frequency compensation technique that relies on low-frequency left-half-plane zeros to allow the proposed OTA to operate for a desired closed-loop behavior. Stability of the many-stage OTA is ensured by re-positioning the poles and zeros of all gain stages in a systematic scalable pattern whenever a new gain-stage is added.

This chapter starts by introducing the overall proposed idea in Section 4.1. In Section 4.2, the design choice for the gain-stages is introduced. In Section 4.3 and 4.4, the detailed implementation of the proposed FCT is discussed. Finally, Section 4.5 concludes the work presented in this chapter.

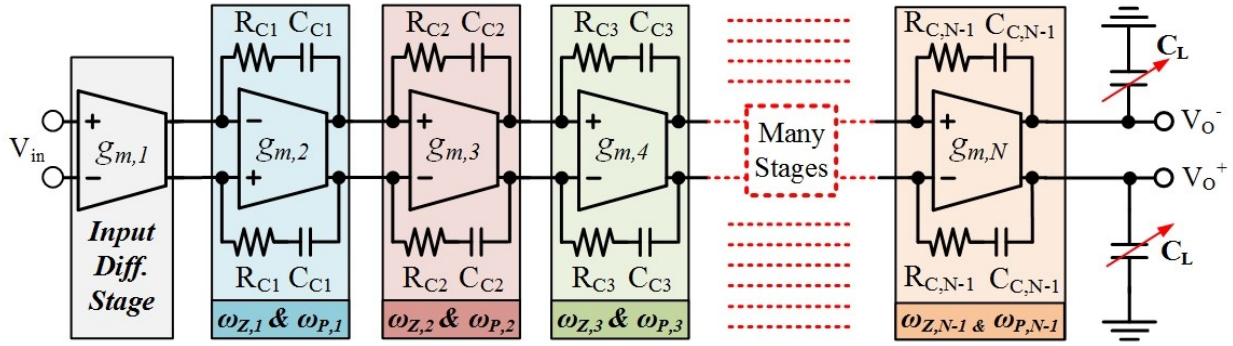

Fig. 4.1: The circuit level realization of the proposed differential-ended *N*-stage CMOS OTA driving a wide range of capacitive loads.

4.1. Cascading Many-Stage CMOS OTAs and Increasing their C_L-Drivability: the Overall Proposed Idea

The diagram of Fig. 2.1(a) and its bilinear *TF* of Eqn. (2.1) can be realized by using the differential-ended circuit level implementation of Fig. 4.1. The *gm*-blocks will be responsible for achieving the required DC gain, while the R-C compensation networks (which are connected across each stage) will properly place the open-loop *P-Z* pairs at the required frequencies.

The purpose of the proposed architecture is to provide a uniform scalable DC gain while driving a wide-range of capacitive loads. Therefore, all gain-stage will be designed to achieve the same *Ai*. However, for such cascading of multi gain-stages to be stable and to allow the OTA to drive a wide range of C_Ls (regardless of the number of gain stages) a new FCT is proposed in this work. This new FCT exploits the fundamental theory of chapter 3, hence, it will rely on positioning the *P-Z* pairs (i.e., ω_{P1}, ω_{Z1} … $\omega_{P,N-1}$, and $\omega_{Z,N-1}$, seen at the bottom of each gain stage in Fig. 4.1) below ω_t. In addition, the reliance on positioning the zeros at low frequencies will be at the heart of the proposed FCT. This will also be done while allowing the OTA to drive

an ultra-wide range of C_L and operate for a desired closed-loop behaviour. A brief discussion regarding the proposed FCT is introduced in the following subsection.

4.1.1. The Proposed Frequency Compensation Technique

The objective of the proposed FCT is to identify the placement of the proposed scalable multi-stage OTA's poles and zeros, so that the load-drive capability and unity-gain bandwidth are maximized (while the OTA is exhibiting a stable closed-loop response). This is further constrained by requiring the settling time of a unity-gain closed-loop configuration be bounded by some desired value denoted by T_S^D. This can be mathematically expressed as follows:

$$\begin{array}{lll} \textit{maximize:} & & \textit{subject to:} \\ \{\omega_t \text{ and } C_L\} & \rightarrow & \{T_S < T_S^D\}. \end{array} \tag{4.1}$$

Solving this problem will lead to an OTA with a higher GBW and greater C_L driving capability. It is important to note that this problem includes both small and large-signal effects. Eqn. (4.1) contains a two-dimensional objective function involving ω_t and C_L, which are inversely inter-dependent. That is, if C_L increases, ω_t decreases. This makes it difficult to identify the maximum. Instead, this optimization problem is performed in two steps using the following sequential, non-iterative procedure. The first step is to solve the problem expressed as

$$\begin{array}{lll} \textit{maximize:} & & \textit{subject to:} \\ \{\omega_t\} & \rightarrow & \{C_{L,min} = 0.5 \text{ pF}\}. \end{array} \tag{4.2}$$

This can be performed using a small-signal AC analysis, so it takes very little time to perform with a transistor-level simulation. This step places the poles and zero at desired frequency

locations for maximum unity-gain frequency while having the minimum required capacitive load, $C_{L,min}$, (say 0.5 pF). Next, a transient analysis is performed on the OTA in a closed-loop configuration subject to an input step V_{in} with different load conditions, i.e.

$$\begin{array}{ll} \textit{maximize:} & \textit{subject to:} \\ \{C_L\} & \rightarrow \{T_S < T_S^D \text{ for input step} = V_{in}\} \end{array} \quad (4.3)$$

While this approach can be executed in a sequential, non-iterative manner, the result may not be optimal but orders of magnitude simpler to implement with excellent results.

The ideal positioning of the *P-Z* pairs should follow the *TF* of Eqn. (3.35). Howerver, apart from the 2-stage OTA, controlling the exact positions of poles and zeros (using the R-C compensation circuit of Fig. 4.1) is limited due to the coupling between stages and the correlation between the poles and zeros' positions. Therefore, the exact positioning of the *P-Z* pairs cannot be achieved according to Eqn. (3.35).

Fortunately, the proposed theory suggests that increasing A_Z will reduce the impact of the *P-Z* pairs regardless of their exact numbers or the positions/distances between them. Thus, if one can position the poles and zeros below ω_t, with no specific order, the improvement of having higher gain (i.e., higher number of stages) on settling time can still be seen. The reason is that once the OTA is configurated in closed-loop, the *N*-1 poles will move towards the *N*-1 zeros, and one pole will move towards the unity-gain frequency, ω_t. Appendix F discusses this issue in more details.

Consequently, to satisfy Eqn. (4.2) and (4.3), and avoid the complexity of using the exact poles and zeros' equations, the proposed FCT positions the open-loop *P-Z* pairs of Eqn. (2.1) at

frequencies below ω_t and above ω_{P0}, without being excluded or canceled (i.e., unlike conventional FCTs), such that

$$\omega_{P0} < \omega_{z1} < \omega_{P1} < \cdots < \omega_{zi} < \omega_{Pi} < \omega_t \quad . \tag{4.4}$$

where this arrangement reduces the coupling between stages and allows positioning the *P-Z* pairs apart from each other.

Based on the *P-Z* pair arrangement in Eqn. (4.4), the unity-gain frequency is no longer equal to the Gain-Bandwidth Product (GBW) (as it is usually the case in conventional FCTs) but it is now given by

$$\omega_t = A_{DC,N} \times \omega_{P0} \times \prod_{i=1}^{N-1} \left(\frac{\omega_{Pi}}{\omega_{Zi}}\right) \quad . \tag{4.5}$$

According to Eqn. (4.5), the lower the zeros' frequencies the higher ω_t is; hence the higher C_L is for a desired settling time.

Since the objective of the proposed FCT is to identify the positions of the OTA's poles and zeros according to Eqn. (4.4), it is required to identify what governs these poles and zeros from the circuit level realization's perspective. Once these relationships are identified, the detailed steps of implementing the proposed FCT can be easily revealed.

4.1.2. The Small Signal Model of the Proposed OTA

Figure 4.2 shows the ideal single-ended small-signal model of the circuit level realization seen in Fig. 4.1. From circuit theory, one can identify that the small-signal low-frequency gain of each stage is ($g_m \cdot R_O$). Therefore, the overall DC gain, $A_{DC,N}$, can be expressed as

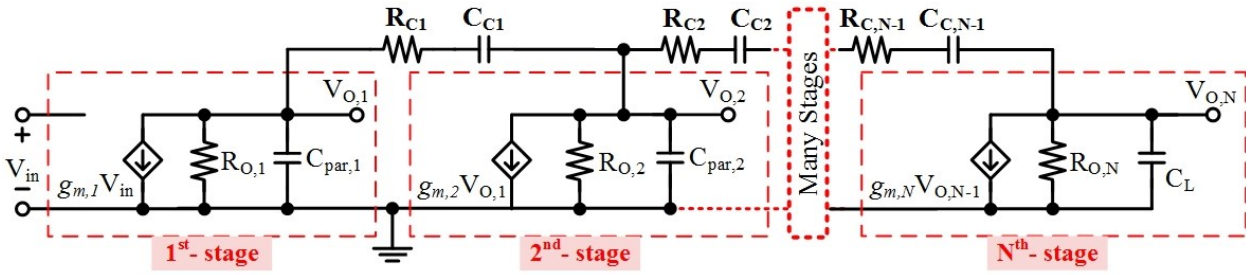

Fig. 4.2: The single-ended small-signal model of the proposed CMOS OTA.

$$A_{DC,N} = \prod_{i=1}^{N} (g_{m,i} R_{O,i}) \tag{4.6}$$

where $g_{m,i}$ is the transconductance of each stage, $R_{O,i}$ is the output resistance of each stage.

The first step in the proposed design technique involves setting the voltage gain of the OTA to some desired value. This will pin-down the required sizes of all transistors to meet power consumptions and overdrive voltage requirements. Also, this step will define the values of the small-signal parameters (i.e., $g_{m,i}$ and $R_{O,i}$) of all stages.

Once $g_{m,i}$ and $R_{O,i}$ are defined, the multi-Miller R-C compensation circuits will control the positions of the open-loop *P-Z* pairs. According to the *TF* of Eqn. (2.1), the OTA will have a different number of poles and zeros based on the designer's choice for *N*.

For example, if $N = 2$, one can identify that the 2-stage OTA has three poles and one zero. Typically, only two-poles of this circuit are of concern, as the third is assumed to be at a frequency much higher than ω_t. As a result, the frequency locations of the two-poles and the zero are approximated based on some assumptions as follows [4 and 104]:

$$\omega_{P0} \approx \frac{g_{m,2}C_{C1}}{C_{par,1}C_L + C_C\left(C_{par,1} + C_L\right)} \approx \frac{g_{m,2}}{C_L} \tag{4.7}$$

$$\omega_{P1} \approx \frac{1}{g_{m,2}R_{O,1}R_{O,2}C_{C1}} \tag{4.8}$$

$$\omega_{Z1} \approx -\left(\frac{g_{m,2}}{C_{C1}}\right)\frac{1}{\left(1 - g_{m,2}R_{C,1}\right)} \tag{4.9}$$

The third pole $\omega_{Ppar,1}$ - typically ignored in the analysis - has an important design value in the proposed theory and needs to be considered here. It can be approximated by [104]:

$$\omega_{Ppar,1} \approx \frac{1}{R_{C1}C_{par,1}} \tag{4.10}$$

where $C_{par,1}$ represents the total shunt capacitance to ground on the output node of the first stage of the OTA and it consists of numerous parasitic elements.

Since the R-C compensation circuits are creating paths between the inputs and outputs of all gain-stages, coupling between stages and correlation between the poles and zeros' positions will occur. Therefore, apart from the two-stage OTA, identifying the exact positions of poles and zeros and/or deriving their exact expressions (using the R-C compensation circuit of Fig. 4.1) is limited. Also, due to the existence of the parasitic capacitances (i.e., $C_{par,1}$, $C_{par,2}$, …, and $C_{par,N-1}$), parasitics poles will also exist and they will also correlate with the open-loop *P-Z* pairs. In addition, relying on the exact equations of poles and zeros will require re-defining them whenever a new stage is added, hence re-designing the R-C compensation circuit with the addition of each new gain-stage. This will highly complicate the design process.

Consequently, to avoid the complexity of using the exact poles and zeros' equations, a scalable FCT is proposed in this work. The proposed FCT starts by designing the compensation circuit of the 2-stage OTA first to satisfy Eqn. (4.2). This is achieved by adjusting $R_{C1,(2\text{-stage.})}$ and $C_{C1,(2\text{-stage.})}$ such that ω_{Z1} is positioned at low frequency so that ω_t is increased, provided it meets certain conditions (to be described later). Then, the proposed FCT will scale the R-C compensation circuit for higher stages while maintaining sufficient values for ω_t. Finally, the proposed FCT follows Eqn. (4.3) to increase C_L-drivability of the proposed OTAs for a desired settling time. Before clarifying these steps of implementing the proposed FCT in Section 4.3 and Section 4.4, the following section will discussed the choice of gain stages as it is the first step in the design process to achieve the required DC gain.

4.2. The Design Choice of the Gain Stages

The proposed design of the scalable many-stage CMOS OTA, shown in Fig. 4.1, consists of a differential input-stage, cascaded by many identical gain-stages. Fig. 4.3 shows the transistor level implementation of the differential stage, which serves as the first stage (i.e. M_1 – M_5), followed by identical common-source (CS) gain-stages (the second stage consists of $M_{6,2}$ and $M_{7,2}$ while subsequent stages consist of transistors identical to them, i.e., $M_{6,3}$ and $M_{7,3}$, …, $M_{6,N}$ and $M_{7,N}$).

Having a differential pair followed by CS transistors is a conventional way to configure OTAs. However, when N = 2, this particular OTA has long been assumed to be limited to applications with pF-range loads [4]. Here, through employing the proposed FCT on this circuit,

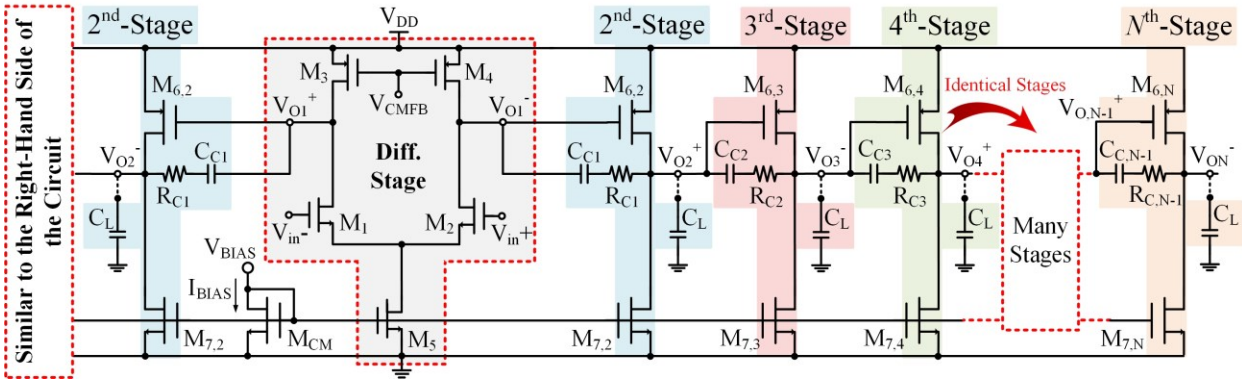

Fig. 4.3: Transistor level implementation of the scalable *N*-stage CMOS OTAs. The circuit uses a differential-ended configuration, the right-hand side is shown here only, and an identical left-hand side has been omitted for simplicity.

it will be shown that it can increase its C_L-drivability up to the nF-range. Also, when $N = 3$, similar architectures have been described in the literature having a Nested-Miller Capacitor (NMC), as in [86], to help stabilize the OTA. Interestingly, this NMC is of no use in the proposed design technique, and this will contribute to having an area-efficient OTA design. Moreover, using this conventional architecture will show that the proposed FCT is unconstrained by a specific OTA circuit topology.

The purpose of the proposed architecture is to provide a uniform scalable DC gain, where each gain-stage will produce the same DC gain of 25 dB (including the differential input-stage). This pins-down the required sizes of all transistors to meet power consumption and overdrive voltage requirements. Also, this defines the values of the small-signal parameters (i.e., g_m and r_O) of all transistors. To achieve this, all gain stages will be biased at the same voltage, and all transistors' sizes of the CS gain stages will be identical.

Consequently, to obtain an A_{DC} of 50 dB, a designer would select $N = 2$, or in other words, use the 2-stage OTA topology. Likewise, the 3-, 4-, 5-, 6-, 7-, and 8-stage OTA configurations

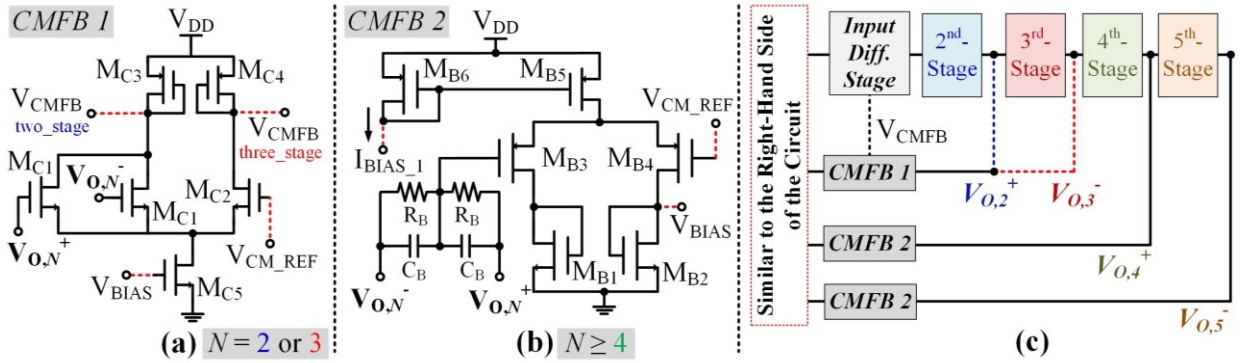

Fig. 4.4: Common Mode Feedback circuits: (a) The CMFB circuit used for $N = 2$ or 3, (b) an extra CMFB circuit used for $N \geq 4$ (i.e., one per stage), and (c) block diagram showing the CMFB circuits connections to the proposed N-stage CMOS OTAs.

would achieve gains of 75 dB, 100 dB, 125 dB, 150 dB, 175 dB, and 200 dB, respectively, and so on.

These gain stages are biased with the current mirror transistors M_{CM}, M_5 and $M_{7,i}$. However, to ensure proper biasing of the output voltages, the Common-Mode Feedback (CMFB) circuits of Fig. 4.4 have been included in the design. These CMFB circuits are based on standard techniques as described in [5] and [104]. If the 2-stage OTA is to be designed, then the CMFB circuit of Fig. 4.4(a) is to be used, and the CMFB voltage (V_{CMFB}) is to be created at the drain of M_{C1}. But if N = 3 (i.e., the 3-stage OTA is to be designed), V_{CMFB} is created at the drain of M_{C2} (in Fig. 4.4(a)). Once more than three gain-stages are needed, the DC gain will significantly increase, thus, the CMFB circuit of Fig. 4.4(a) will not be able to hold the biasing voltages at the output of all gain-stages. Therefore, an extra CMFB circuit will be used to keep the biasing voltages of these additional gain-stages within the required values. Fig. 4.4(b) shows the extra CMFB circuit that will be included when $N \geq 4$. In this case, the CMFB circuit of Fig. 4.4(a) will be connected at the differential output of the 3rd gain-stage, while the CMFB circuit of Fig. 4.4(b) will be connected at the differential output of each new gain-stage (i.e., $N \geq 4$). Fig. 4.4(c) summraizes

the CMFB circuit connections for *N*-Stage CMOS OTAs (i.e., up to 5-stage has been shwon in Fig. 4.4(c) for simplicity).

4.3. Implementation of the Proposed FCT - STEP (1): Increase ω_t Under Small C_L Using Low-Frequency Zeros

Conventional FCTs are usually applicable for specific number of stages and/or specific OTAs' circuit topologies. However, the proposed FCT has the advantage of being applicable to *N*-stage CMOS OTAs, as well it is not constrained by any specific circuit topology, and it is technology independent. Therefore, the key idea here is to accurately perform the proposed FCT which is described by Eqn. (4.2) and Eqn. (4.3). In this section we shall start by following the technique described by Eqn. (4.2) to design the 2-stage OTA of Fig. 4.3, then scale it for higher stages.

4.3.1. Implementation of the Proposed FCT Having $N = 2$

The starting point in implementing the proposed FCT is to begin with a two-stage OTA, thus, Eqs. (4.7) - (4.10) will govern the positions of ω_{P0}, ω_{P1}, ω_{Z1}, and $\omega_{Ppar,1}$, respectively.

As discussed in Chapter 2, in conventional 2-stage OTAs, where Miller R-C compensation networks are used, stability is ensured by positioning ω_{P1} at low frequencies (by increasing the value of C_{C1}) and placing ω_{P0} and ω_{Z1} at frequencies above ω_t or by positioning them at the exact same frequency to achieve a pole-zero cancellation. Thus, ω_t in such conventional designs is the GBW, and will be referred to (here) as: $\omega_{t,ref}$. Fig. 4.5(a) shows the magnitude response (i.e., black-dashed line) of such conventional designs, where $\omega_{t,ref}$ is given by

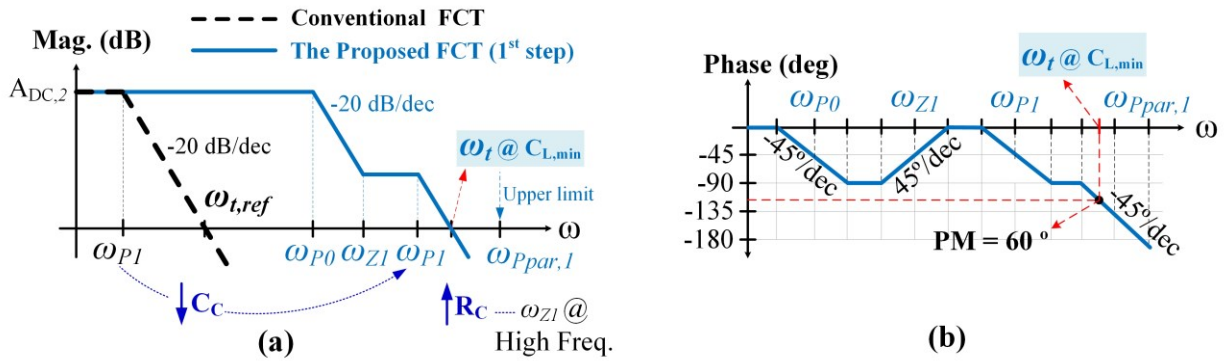

Fig. 4.5: The ideal AC open-loop response of conventional FCT and the proposed FCT for N = 2: (a) the ideal magnitude response showing the impact of the proposed FCT on the value of ω_t according to Step (1), (b) the ideal phase response showing the possible location of ω_t to achieve a PM of 60º.

$$\omega_{t,ref} = A_{DC,2} \times \omega_{P1} \quad . \tag{4.11}$$

However, relying on large values of C_{C1} to compensate for the 2-stage OTA will slow down the OTA's response, increase the silicon area, and most importantly; prevent the R-C compensation circuit from being scaled for higher stages as will be discussed in the next subsection.

Consequently, the proposed FCT adapts a different arrangement of poles and zeros to enhance ω_t while having a small C_L ($C_{L,min}$) (i.e., say 0.5 pF); hence, Eqn. (4.11) will be extended to accurately express the new proposed arrangement of the poles and zeros. Then, the additional increase in ω_t can be traded off for higher C_L.

According to Eqn. (4.11), it should be obvious that the value of $\omega_{t,ref}$ can be increased by increasing $A_{DC,2}$ and/or ω_{P1}. However, $A_{DC,2}$ has already been pre-defined, consequently, increasing $\omega_{t,ref}$ is simply achieved by increasing ω_{P1}, or in other words; by reducing the value of C_{C1} according to Eqn. (4.8). The new position of ω_{P1} after reducing C_{C1} is shown (in blue) in Fig.

4.5(a). Interestingly, pushing ω_{P1} to higher frequencies, by reducing C_{C1} will allow ω_{P0} to become the 3-dB frequency of the OTA instead of ω_{P1} (i.e., ω_{P0} mainly depends on $g_{m,2}$ and C_L). This will become useful when increasing the C_L-drivability in the next section. However, reducing the value of C_{C1} alone is a bad design practice because it will alter the stability of the OTA as ω_{P1} will move towards ω_{P0}, and at the same time, ω_{Z1} will be shifted to higher frequencies (i.e., as depicted by Eqn. (4.9)). Therefore, the gain roll-off will drop to values around -40 dB/dec, and thus, the phase margin will also drop. But, if one can properly re-position ω_{Z1} (after reducing C_{C1}) according to Eqn. (4.4), the zero will counteract the effect of the two poles on the gain-roll off and the phase margin. As a result, the stability issue can be controlled and the new general expression of ω_t can be written as in Eqn. (4.5).

To re-position ω_{Z1} according to Eqn. (4.4) and shift it from higher to lower frequencies as seen in Fig. 4.5(a), one can use a large R_C (i.e., ~ kΩ). As a result, the impact of the proposed FCT in this 1st step, compared to the conventional design, is shown in the AC response of Fig. 4.5(a).

Since $A_{DC,2}$ is pre-defined, and ω_{P0} is almost independent of the R-C network, Eqn. (4.5) indicates that the maximum value of ω_t (i.e., near-optimum) can be achieved, ideally, by increasing ω_{P1} while decreasing ω_{Z1}. However, the limitation of the upper value of ω_t is $\omega_{P_{par,1}}$, seen in Eqn. (4.10) and Fig. 4.5(a); as there is no full-design control over this parasitic pole. Also, increasing ω_{P1} while decreasing ω_{Z1} should be done such that the phase margin is greater than some desired value. For example, to obtain a PM of 60°, one can arrange the poles and zeros as shown in the AC phase response of Fig. 4.5(b). Here, the PM is

$$PM = 180 - \sum_{i=1}^{N-1} \theta_{P,i} + \sum_{i=1}^{N-1} \theta_{Z,i} \quad , \tag{4.12}$$

where $\theta_{P,i}$ is the phase of the i^{th}-pole and $\theta_{Z,i}$ is the phase of the i^{th}-zero.

To achieve this at the circuit level, one can start with the minimum possible value of C_{C1} given by a certain CMOS technology (i.e., slightly higher than $C_{par,1}$). Then, R_C (~ kΩ) is increased in value to achieve the required PM so that ($\omega_t \leq \omega_{P_{par,1}}$), or until the value of R_C becomes impractical in the given CMOS technology. This will allow the R-C circuit to occupy a small-silicon area. Accordingly, with this, the 1st step of the design process, described by Eqn. (4.2), would have now been completed for $N = 2$.

4.3.2. Scaling the 2-Stage R-C Compensation Circuit for $N \geq 3$ under $C_{L,min}$

To design the 3-stage OTA, a new gain-stage is added to the 2-stage OTA as depicted in Fig. 2 and Fig. 3. Also, to design a 4-stage OTA, two gain-stages are added to the 2-stage OTA, and so on. Each new gain-stage comes with its own compensation circuit. Consequently, a new *P-Z* pair will be added to the *TF* with each new stage as described in Eqn. (2). Also, according to Eqn. (7), ω_t will significantly increase, as $A_{DC,N}$ will also increase. However, this new value of ω_t will most likely exceed the previously defined upper limit of ω_t. Therefore, it would be necessary to re-adjust the value of ω_t by re-positioning the poles and the zeros, according to Eqn. (6), whenever a new stage is added. This can be done by re-sizing the R-C circuit with the addition of each new stage.

Instead of deriving new equations for the poles and zeros for each stage separately, and by knowing that the *P-Z* pairs have an inverse relationship with R_C and C_C, the values which were found for the 2-stage OTA can be scaled to size the compensation circuits of higher OTA stages. Interestingly, since the poles and zeros are positioned according to Eqn. (36) and since the maximum ω_t is defined, the sizes of the R-C compensation circuit components follow a certain pattern in order to position the *P-Z* pairs when a new gain-stage is added. This scalable pattern can be seen in Table III and can be described as follows: whenever a new stage is added, the compensation capacitors of the previous stages are increased in size to decrease the frequency of the poles of the new OTA stage, and hence help in reducing ω_t to its defined upper limit (i.e., lower than the parasitic pole). Since no exact positioning of the *P-Z* pairs is required, the amount of increment in C_Cs of the previous stage is being decided by observing the poles' positions – to make sure that they are at frequencies less than ω_t. Therefore, quantitative patterns are found (by simulations) to increase C_Cs for different stages uniformly. These uniform quantitative patterns of increasing C_Cs can be described by:

$$C_{C(i-1),(N-stage)} = C_{C(i-2),[(N-1)-stage]} \quad , 3 \leq i \leq N \tag{4.13}$$

and

$$C_{Ci,(N-stage)} > C_{Ci,[(N-1)-stage]} \quad , 1 \leq i \leq N-1 \, . \tag{4.14}$$

Thus, the new compensation capacitor ($C_{C(i-1),(N\text{-stage})}$) is sized to the minimum capacitance value, which was found for the 2-stage OTA (i.e., $C_{C(i-1),(N\text{-stage})} = C_{C1,(2\text{-stage})}$). This highlights the difference between the proposed technique and the conventional methods that rely on large C_{C1} values to design the 2-stage CMOS OTAs.

Sizing C_Cs according to these patterns will change the poles and zeros positioning (i.e., reducing them) simultaneously, hence, according to Eqn. (4.5), ω_t might not be increased to frequencies higher than ω_{Ppar}. Also, sizing C_Cs only might not satisfy the *P-Z* arrangement of Eqn. (4.4). Therefore, to make sure that $\omega_t \leq \omega_{Ppar}$, and to satisfy the arrangement of the poles and zeros according to Eqn. (4.4), the compensation resistors will be sized according to an opposite pattern of sizing C_Cs; that is: whenever a new stage is added, the compensation resistors of the previous stage are reduced to increase the frequency of the zero of the new OTA stage, and hence reduce ω_t to its defined upper limit (i.e., lower than the parasitic pole). The amount of change in R_Cs of the previous stage is being decided by observing the OTA stability via simulations. In a similar fashion of sizing C_Cs, quantitative patterns are being used to initially size the R_Cs. Therefore, once adding a new stage, the reduction in R_Cs can be described as

$$R_{Ci,(N-stage)} \leq R_{Ci,[(N-1)-stage]} \ ,1 \leq i \leq N-1 \tag{4.15}$$

while the new compensation resistor (i.e., $R_{C(N-1),(N-stage)}$) is initially sized according to the following condition

$$R_{C(N-1),(N-stage)} \leq R_{C(N-2),(N-stage)} \tag{4.16}$$

Since the constraint equations in (4.13)-to-(4.16) show an intuitive technique of sizing the R-C compensation circuits for $N \geq 3$, and since there is no need for exact positioning of the poles and zeros, one can slightly tweak these patterns to enhance the open-loop and closed-loop responses if necessary. For example, such tweaking can be done if an exact PM of 60º is required under $C_{L,min}$ of 0.5 pF.

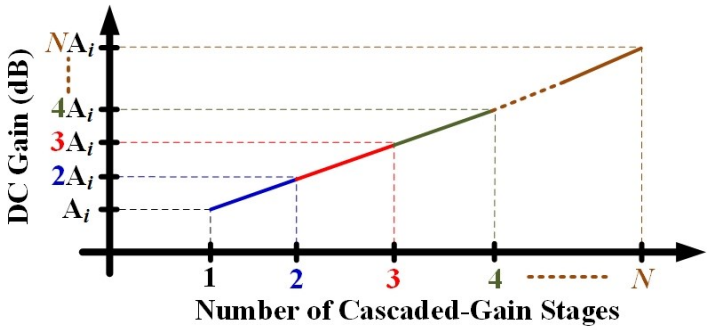

Fig. 4.6: The increase in DC gain with the increase in number of stages at $C_{L,min}$.

At this point the proposed scalable *N*-stage CMOS OTA is compensated to drive $C_{L,min}$ under the required PM. Also, as seen in Fig. 4.6, the overall DC gain (in dBs) is increasing linearly with the addition of gain stages since all gain stage are providing the same DC gain of A*i*.

4.4. Implementation of the Proposed FCT - STEP (2): Maximize C_L for a Desired Settling Time

Since the design achieved through Step (1) is transferring the dependency of the dominant pole to ω_{P0} (i.e., $C_{L,min}$), one should distinguish between compensating the OTAs with C_L only and the proposed FCT. Interestingly, one can remove the R-C compensation circuit and rely only on C_L to position ω_{P0} below ω_t while leaving the *P-Z* pairs (i.e., ω_{P1}, ω_{Z1}, ω_{P2}, ω_{Z2} ... ω_{Pi} and ω_{Zi}) without being controlled. On doing so, the stability can be achieved once $C_{L,min}$ is increased such that ω_t is shifted to frequencies much lower than the *P-Z* pairs (i.e., PSA). However, this technique is associated with some critical drawbacks. First, this technique is technology dependent, in other words; leaving the *P-Z* pairs without being controlled, will allow the parasitic

capacitances (which are technology dependent) to decide their frequency positions. Second, this technique will work, if and only if, a large $C_{L,min}$ is required (i.e., in the range of tens of nano-Farads). Also, this large $C_{L,min}$ is increasing with the addition of extra gain stages, due to the increase in $A_{DC,N}$ (i.e., ω_t). For these reasons and others, this dependency of the dominant pole on C_L has been claimed to be a bad design practice in [105]. Nevertheless, this will not be an issue in the proposed FCT, since the *P-Z* pairs have already been positioned at the required frequencies. Consequently, one can define the range of C_L that prevents the *P-Z* pairs from alternating the OTA's stability. To easily capture the shortage of relying on C_L only to compensate the OTA, and to clearly discuss the advantages of the proposed FCT in increasing C_L-drivability of the proposed OTA, Fig. 4.7 introduces the relationship between the PM and C_L.

The PM is an open-loop parameter that can indicate the closed-loop step response behavior. Fig. 4.7 shows how the PM is changing with the increase in C_L based on different scenarios of positioning the OTA's poles and zeros in the proposed FCT. Accordingly, it indicates the behavior of the closed-loop step response.

Since the design achieved through step (1) was still loaded with a very small C_L (i.e., $C_{L,min}$ = 0.5 pF) and achieved a sufficient PM (say 60º), one can carry on from this point and investigate the impact of increasing C_L on the PM. According to Eqn. (4.7), increasing $C_{L,min}$ will result in shifting ω_{P0} to lower frequencies, thus, shifting ω_t to lower frequencies as well. As can be seen in Fig. 4.7, this will create three different regions based on the new positions of ω_t with respect to the *P-Z* pairs. In each region the impact of increasing C_L on the PM will depend on the position of ω_{Zi} with-respect-to ω_{Pi}, thus, three cases will be created in each region. To clarify

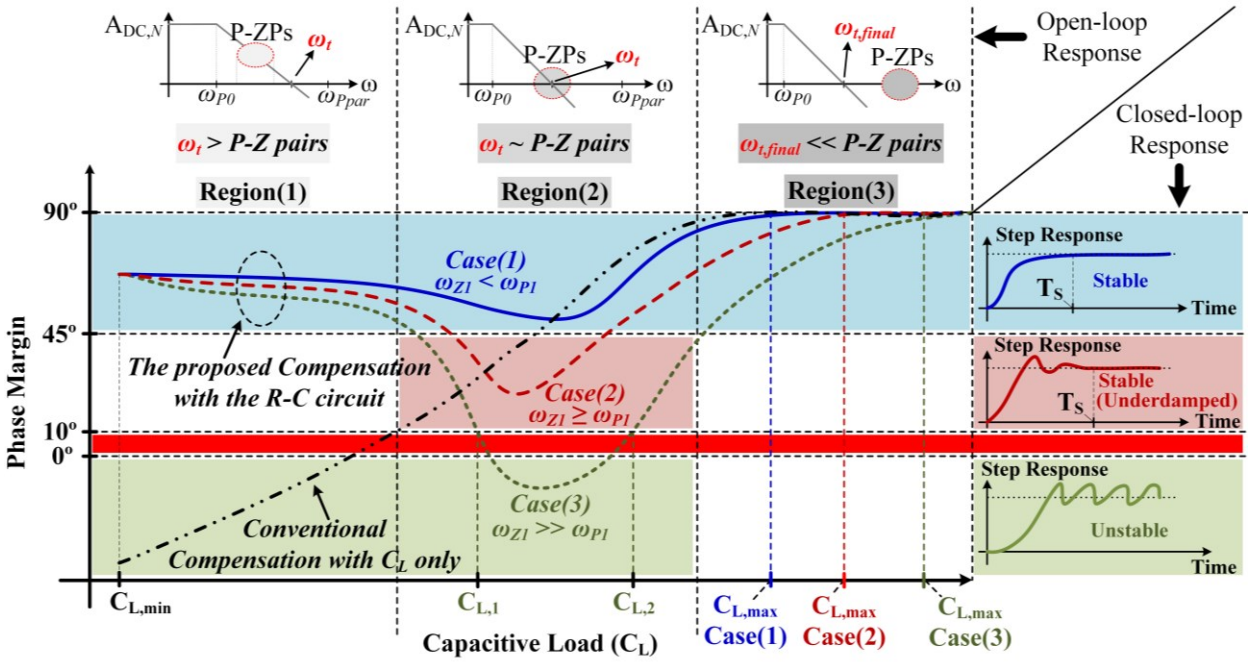

Fig. 4.7: Phase margin vs. C_L showing the impact of positioning the open-loop *P-Z* pair on the closed-loop step response of the proposed OTAs.

this, let's consider the cases when $N = 2$, and discuss the PM behavior in these three regions based on the position of ω_{Z1} and ω_{P1}.

A. Region (1): ω_t > P-Z pairs

This region starts at $C_{L,min}$, where the OTA exhibits a stable response (as discussed in Step (1) of the proposed FCT) and the *P-Z* pair are positioned below ω_t. As C_L increases, ω_t moves towards the *P-Z* pair and a slight drop in the PM will occur. However, this will not affect the closed-loop response as the PM ≥ 45º. Therefore, the impact of positioning ω_{Z1} with-respect-to ω_{P1} will not impact the OTA's stability in this region. Nonetheless, it is recommended to achieve sufficient values for PM in Step (1) (i.e., PM ≥ 60º) to expand this region as much as possible. This can be done by positioning ω_{Z1} at low frequencies.

In this region, one can clearly distinguish between the proposed FCT and the conventional techniques that depend on C_L only (i.e., the dashed-dotted black line in Fig. 4.7), where stability cannot be ensured at small values of C_L.

B. Region (2): ω_t ~ P-Z pairs

Once increasing C_L to higher values, such that ω_t will be located slightly above, in between, or slightly below the *P-Z* pair, the impact of positioning ω_{ZI} with-respect-to ω_{PI} will become significant. In other words, according to Eqn. (4.12), if ω_{ZI} is positioned at low frequency (i.e., Case (1): $\omega_{ZI} < \omega_{PI}$), it will compensate the PM drop that will be caused by ω_{PI}, and the PM will be kept above 45º (i.e., the solid-blue line in Fig. 4.7 is always within the blue shaded area). However, ω_{ZI} will have less impact on the PM if it is positioned slightly above ω_{PI} (i.e., Case (2): $\omega_{ZI} \geq \omega_{PI}$). Consequently, the PM might drop to values below 45º and above 10º (i.e., the dashed-red line is entering the light-red shaded area in Fig. 4.7). Nonetheless, the step response will exhibit a stable underdamped behavior, which will be seen as an increase in settling time. However, if $\omega_{ZI} >> \omega_{PI}$ (i.e., Case (3)), the PM drop (with the increase in C_L) might reach values below 10º, hence, the step response will become unstable within a specific range of C_L (i.e., the dotted-green line will enter the green-shaded area between $C_{L,1}$ and $C_{L,2}$ in Fig. 4.7).

Although the step response might exhibit a stable response for $0º \leq PM \leq 10º$, it has been assumed unrecommended in Fig. 4.7 (i.e., the dark-red shaded area) as it will be associated with excessive ringing. Interestingly, further increase in C_L, within *Region (2)*, will allow ω_t to be at frequencies lower than the *P-Z* pair, thus, the PM will start increasing toward 90º.

C. Region (3): ω_t << P-Z pairs

Once the PM reaches 90º, the proposed FCT reaches its definition for the maximum capacitive load ($C_{L,max}$), because at PM = 90º, the R-C compensation circuits will have no more impact on the design, and C_L will compensate the OTA. Accordingly, one can define C_L-drivability ration as

$$C_{L-drivability} = \begin{cases} \frac{C_{L,max}}{C_{L,min}}, & for\ Case\ (1)\ and\ (2) \\ \\ \frac{C_{L,max}}{C_{L,min}} \times \frac{C_{L,1}}{C_{L,2}}, & for\ Case\ (3) \end{cases} . \quad (4.17)$$

Since the *P-Z* pairs will have no impact on ω_t in this region, the unity-gain frequency will be referred to as $\omega_{t,final}$ (seen in Fig. 4.7) and it can be written as:

$$\omega_{t,final} = A_{DC,N} \times \omega_{P0} \quad . \quad (4.18)$$

Also, the step response will follow a single time constant behavior, and it can be written as

$$V_{O,N}(t) = V_{in}\,[1 - e^{-t\,\omega_{t,final}}] \quad . \quad (4.19)$$

Apparently, the proposed OTA will exhibit a stable response once increasing C_L beyond $C_{L,max}$, where the PM will always be 90º, but it will not be included in the discussion to avoid confusing the proposed FCT with conventional ones.

4.4.1. Settling time requirements

According to Eqn. (4.3), the objective of this section is to define the range of C_L that corresponds to a desired settling time. Since the design achieved through Step (1) was still loaded with a very

small capacitance (i.e., $C_{L,min}$ = 0.5 pF), the settling time ($T_{S,initial}$) of the closed-loop amplifier would be very short. Indeed, it is assumed to be much shorter than the desired settling time T_S^D, and hence an increase in settling time can be traded-off for a higher C_L. Knowing that T_S^D is widely varying based on the required application, as seen in Fig. 1.2, one can define a range of C_L's that corresponds to a range of different settling time values by searching on the step response of the closed-loop amplifier beginning with $C_{L,min}$. This can be simply done by increasing C_L, starting from $C_{L,min}$, until the desired settling time is reached, as long as $C_L \leq C_{L,max}$. At this point, the desired C_L ($C_{L,desired}$) can be identified. Here, V_{in} can be driven with a step input whose magnitude can be in the small or large-signal range. There are no constraints on the input condition.

Increasing C_L, starting from $C_{L,min}$, will result in different closed-loop responses based on the P-Z pair's positions, as can be seen on the right hand side of Fig. 4.7. Therefore, Fig. 4.8 builds on these different cases on positioning the P-Z pairs and indicates the relationship between settling time and C_L. Here one sees the three curves that will be created as C_L is increasing according to the P-Z pairs' positions.

For all scenarios of positioning the P-Z pairs, settling time is increasing with the increase in C_L, however, when $\omega_{ZI} < \omega_{PI}$ the OTA will exhibits faster closed-loop response as the region of underdamping behavior will not be entered (this is was shown in the solid-blue line in Fig. 4.7 and now can be seen in the solid-blue line of Fig. 4.8). As for $\omega_{ZI} \geq \omega_{PI}$ and $\omega_{ZI} >> \omega_{PI}$, the closed-loop response will be partially experiencing stable-underdamped response (as seen in Fig. 4.7); which will result in slower settling times. Consequently, for the same T_S^D the case of positioning ω_{ZI} at low frequencies will achieve higher C_L-drivability, as $C_{L,desired}$ will be larger

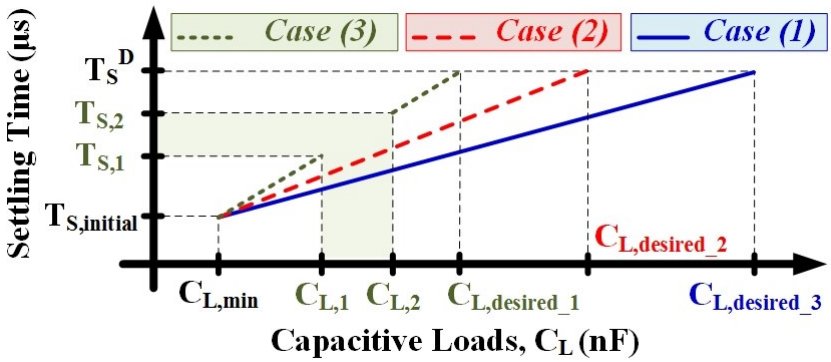

Fig. 4.8: The relationship between settling time and C_L, showing the different cases that will be created based on the proposed FCT.

(i.e., $C_{L,desired,3} > C_{L,desired,2} > C_{L,desired,1}$ in Fig. 4.8). But, for the case when $\omega_{Z1} >> \omega_{P1}$ (i.e., green-dotted line of Fig. 4.8) the OTA will not be stable between $C_{L,2}$ and $C_{L,1}$ as the PM might drop to values below 10º (the green-shaded area of Fig. 4.7).

If the C_L range between $C_{L,min}$ and $C_{L,max}$ does not meet the requirements on T_S^D, one can re-adjust the reference design of the OTA by optimizing the biasing voltages and the transistors' aspect ratios. If this still does not allow the proposed technique to meet the requirements on T_S^D, then the proposed OTA is not suited for the given application.

4.5. Summary

By exploiting the theory which was introduced in Chapter 3, a new frequency compensation technique that allows cascading many-stage CMOS OTAs (to achieve an ultra-high DC gain) and driving a very wide range of C_L was introduced. The proposed technique involves positioning the OTA's zeros at low frequencies to increase ω_t of the OTA. The additional increase in ω_t can be traded off for higher C_L by transferring the dependency of the dominant

pole to C_L. To achieve this, the OTA was designed using multi-Miller R-C compensation circuits across the OTA's gain-stages. Also, the proposed technique was shown to be unconstrained by the OTA's circuit topology. Hence, conventional gain-stages (i.e., differential pair and common source transistors) were used to design fully-differential *N*-stage CMOS OTAs. Also, a study on the impact of low-frequency zeros on the C_L- drivability of CMOS OTAs was introduced in this chapter. This study shows that the lower the zeros' frequencies, the wider the C_L- drivability is.

The main contribution of this chapter is captured in three figures as follows:

1. **Fig. 4.6, where the increment in the number of cascaded gain-stages is allowing the realization of a scalable-gain CMOS OTAs (without having stability issues).**
2. **Fig, 4.7, where the impact of LF zeros on the PM (as C_L is increasing) is revealed.**
3. **Fig. 4.8, where the technique to achieve a desired settling time for a desired C_L is shown.**

Finally, the proposed design technique needs to be verified and validated with schematic, post layout, and measurement results. Therefore, Chapter 5 and Chapter 6 are discussing the implementation of an actual many-stage CMOS OTA. **Through this implementation, the main contribution of this chapter, which can be seen in Fig. 4.6, 4.7 and 4.8, will be verified and validated.**

CHAPTER 5

VERIFICATION & VALIDATION OF THE PROPOSED RELATIONSHIP BETWEEN FREQUENCY RESPONSE & SETTLING TIME

The proposed theory in Chapter 3 has introduced a generalized relationship between frequency response and settling time of CMOS OTAs in the presence of *P-Z* pairs. As mentioned in the summary of Chapter 3, the main contribution of this theory has been captured in Fig. 3.5, Fig. 3.6, and Fig. 3.9. Accordingly, this chapter will verify and validate the proposed theory on transistor level implementation, with the focus on reproducing Fig. 3.5, Fig. 3.6, and Fig. 3.9 through simulations (schematic and post-layout) as well as some measurement results. In order to design an OTA for the purpose of verification and validation, the proposed design technique of Chapter 4 will be followed, hence; the OTA of Fig. 4.3 will be used as the analysis and design vehicle throughout this chapter. Interestingly, the proposed theory will be validated and verified through a design example that also demonstrates how the generalized theory unveils opportunities for many-stage OTA design. Extensive simulations were conducted (using Cadence), as well as some measurements, based on the standard 65 nm TSMC CMOS, addressing all possible operation modes of the OTA.

This chapter starts with the verification and validation of the proposed theory while having one *P-Z* pair in Section 5.1. Since one *P-Z* pair is required in this section, a 2-stage OTA will be used to verify and validate Fig. 3.5 and Fig. 3.6 of Chapter 3 in two different subsections (i.e., 5.1.1 and 5.1.2, respectively). In each subsection, the 2-stage OTA design setup, the results, and the design robustness will be discussed. Then, the verification and validation of the proposed theory while having *N*-1 *P-Z* pairs will be introduced in Section 5.2. In this section, 2- to 8-stage CMOS OTAs will be introduced to verify the results of Fig. 3.9.

5.1. Verification and Validation of the Proposed Theory Having One Pole-Zero Pair

Figure 3.5 and Fig. 3.6 of Chapter 3 summarize the proposed theory having one *P-Z* pair. Therefore, the following subsections are verifying and validating the results of Fig. 3.5 and Fig. 3.6 by designing the two-stage CMOS OTA (i.e., $N = 2$) of Fig. 4.3.

5.1.1. The P-Z Doublet Separation Distance (δ_{CL}) vs. the *P-Z* Pair Separation Ratio (ω_{P1}/ω_{Z1})

Since the theoretical analysis of Fig. 3.5 suggested that changing ω_{P1} and A_Z is the way to control δ_{CL}, the conventional 2-stage OTA of Fig. 4.3 has been designed to verify and validate this.

5.1.1.1. The OTA Design Setup

The initial design has been done without optimization and without the CMFB circuit of Fig. 4.4 to keep the values flexible as a wide range of values for ω_{P1} is required. Therefore, the initial

TABLE 5.1
DEVICES' SIZES OF THE TWO-STAGE OTA OF FIG. 4.3 FOR THE PURPOSE OF VERIFYING δ_{CL} WITH I_{BIAS} = 6 µA

Device	Aspect Ratio/Size	Device	Aspect Ratio/Size		
$M_1 = M_2$	(2 µm / 390 nm)	**$M_{6,2}$**	(23 µm / 120 nm)		
$M_3 = M_4$	(1.2 µm / 325 nm)	**$M_{7,2}$**	(15 µm / 240 nm)		
M_5	(4 µm / 520 nm)	**C_{C1}**	10 pF	R_{C1}	35 kΩ

design has been done by fixing ω_{P0} and ω_{Z1} at 5 kHz and 460 kHz, respectively, (by fixing the values of C_{C1}, R_{C1} and $g_{M6,2}$ (i.e., aspect ratio of $M_{6,2}$) as seen in Table 5.1). Consequently, the performance will be controlled by sweeping ω_{P1}. For A_{DC} of 56.4 dB at V_{DD} = 1 V, ω_{P1} has been swept to sweep the ratio of (ω_{P1}/ω_{Z1}) between 0.2 to 28, by sweeping the value of C_L between (20 pF and 10 nF).

5.1.1.2. Simulation Results

Fig. 5.1(a) shows the two-stage OTA's open loop AC response for the case of A_{DC} = 56.4 dB, and different ratios of (ω_{P1}/ω_{Z1}). Here, the sweeps in ω_{P1} are expressed in terms of the open-loop *P-Z* pair ratio (ω_{P1}/ω_{Z1}). However, for simplicity, the ratio of (ω_{P1}/ω_{Z1}) has been plotted for three scenarios only: the maximum of 28, the minimum of around 0.2 and the near pole-zero cancellation of 1.

Fig. 5.1(b) shows δ_{CL} as a function of (ω_{P1}/ω_{Z1}). The results in Fig. 5.1(b) clearly satisfy the claim in Eqn. (3.23) along with the results seen in Fig. 3.5. Although some values of δ_{CL} are off when (ω_{P1}/ω_{Z1}) < 1, due to the coupling between ω_{P0} and ω_{P1}, the overall behavior verifies the proposed analysis in Chapter 3 regarding δ_{CL}.

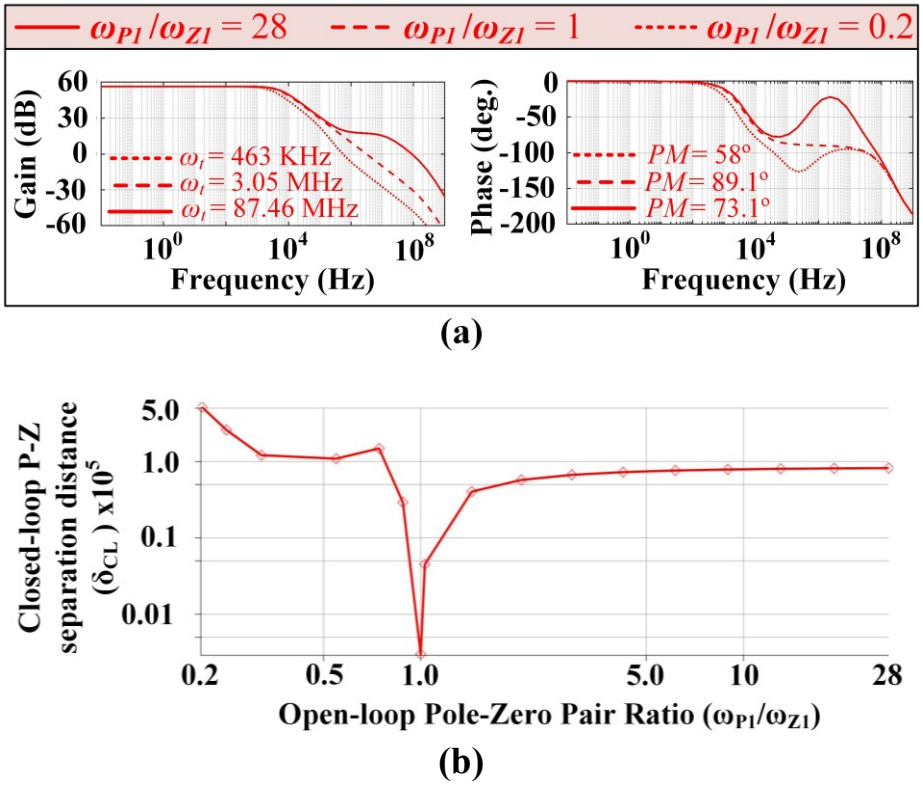

Fig. 5.1: (a) The Open-loop AC response of the tow-stage OTA of Fig. 4.3 having different scenarios for open-loop P-Z pair (ω_{PI}/ω_{ZI}) with a DC gain of 56.4 dB, and (b) the closed-loop pole-zero separation distance (δ_{CL}) as a function of (ω_{PI}/ω_{ZI}) to verify part of the theory which is reported in Eqn. (3.23) and Fig. 3.5.

5.1.2. Settling Time vs. LF Zero Gain (A_Z) Having One *P-Z* Pair

Figure 3.6(a) and (b) of Chapter 3 show the settling time as function of A_Z and ω_P (i.e., ω_{PI}/ω_{ZI}), respectively. To validate these relationships, the two-stage OTA of Fig. 4.3 has been fabricated using standard TSMC 65 nm CMOS process.

5.1.2.1. The OTA Design Setup

Figure 5.2(a) shows the microphotograph of the fabricated chip. The design parameters of the fabricated chip are shown in Table 5.2.

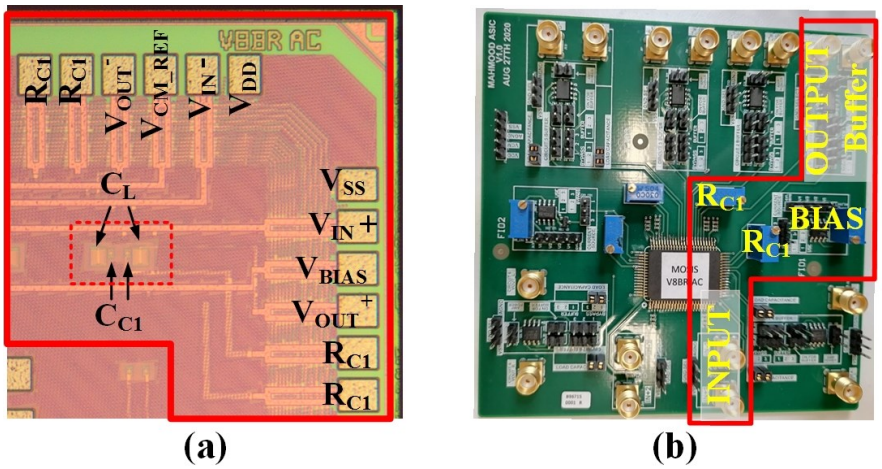

Fig. 5.2: The fabricated differential-ended two-stage CMOS OTA of Fig. 4.3: (a) the chip's microphotograph, and (b) the PCB showing off-chip R_{C1} for controlling purposes.

TABLE 5.2
DEVICES' SIZES AND RESULTS SUMMARY OF FABRICATED TWO-STAGE CMOS OTA OF FIG. 4.3 AND FIG. 4.4(a)

Device	Aspect Ratio/Size			Metric	Value
$M_1 = M_2 = M_{C2}$	2 × (1 µm / 390 nm)			Process	65 nm
$M_3 = M_4 = M_{C3} = M_{C4}$	8 × (0.75 µm / 325 nm)			V_{DD}	1.2 V
$M_5 = M_{C5}$	4 × (1.1 µm / 520 nm)			Gain	50.5 dB
$M_{6,2}$	8 × (0.55 µm / 130 nm)			BW	29.8 kHz
$M_{7,2}$	10 × (0.66 µm / 260 nm)			Area	(95 µm × 35 µm)
M_{C1}	1 × (1 µm / 390 nm)			Power	108 µW
C_{C1}	50 fF	C_L	1 pF	V_{CM_REF}	0.53 V

Here a wide range of values for A_Z and (ω_{P1}/ω_{Z1}) are required. But, once the circuit is being fabricated, changing circuit parameters becomes challenging. Therefore, controlling the values of A_Z and (ω_{P1}/ω_{Z1}) are limited. Nevertheless, in this experiment setup, we were able to sweep A_Z by sweeping the values of ω_{Z1}. This has been achieved by having an off-chip R_{C1}, as seen in the PCB of Fig. 5.2(b), to control the position of ω_{Z1}.

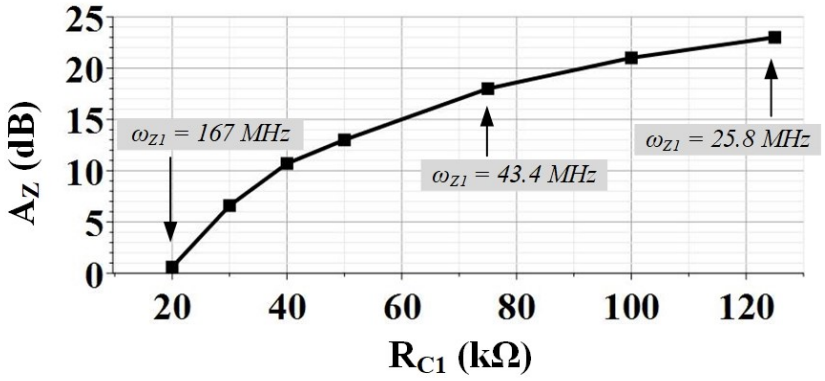

Fig. 5.3: The low-frequency zero gain (A_Z) as a function of R_{C1}.

5.1.2.2. Simulations and Measurements Results

Simulation result of Fig. 5.3 shows that by sweeping R_{C1} from 20 kΩ to 125 kΩ, A_Z is swept from 0.6 dB to 23 dB, where ω_{Z1} is decreasing form 167 MHz to 25.8 MHz. Once R_{C1} is increased beyond 125 kΩ, the parasitic poles will start to appear next to ω_t. Appendix G shows the full details of producing Fig. 5.3.

Since increasing R_{C1} will increase A_Z, then if one increases R_{C1} and observe the settling time, the relationship between A_Z and settling time when having one *P-Z* pair can be revealed. Fig. 5.4 shows the closed-loop unity-gain step response for schematic and post-layout simulations in Fig. 5.4(a), and the measurement results in Fig. 5.4(b) (based on the fabricated chip of Fig. 5.2) for the minimum and the maximum values of R_{C1}. It is clear from Fig. 5.4(b) that the step response settles faster when R_{C1} = 128 kΩ.

Interestingly, as ω_{Z1} is decreasing by increasing R_{C1}, the ratio of (ω_{P1}/ω_{Z1}) is increasing as reported in Table 5.3. Nevertheless, the settling time is decreasing due to the increase in A_Z, which once again emphasis the impact of A_Z, regardless of (ω_{P1}/ω_{Z1}) value.

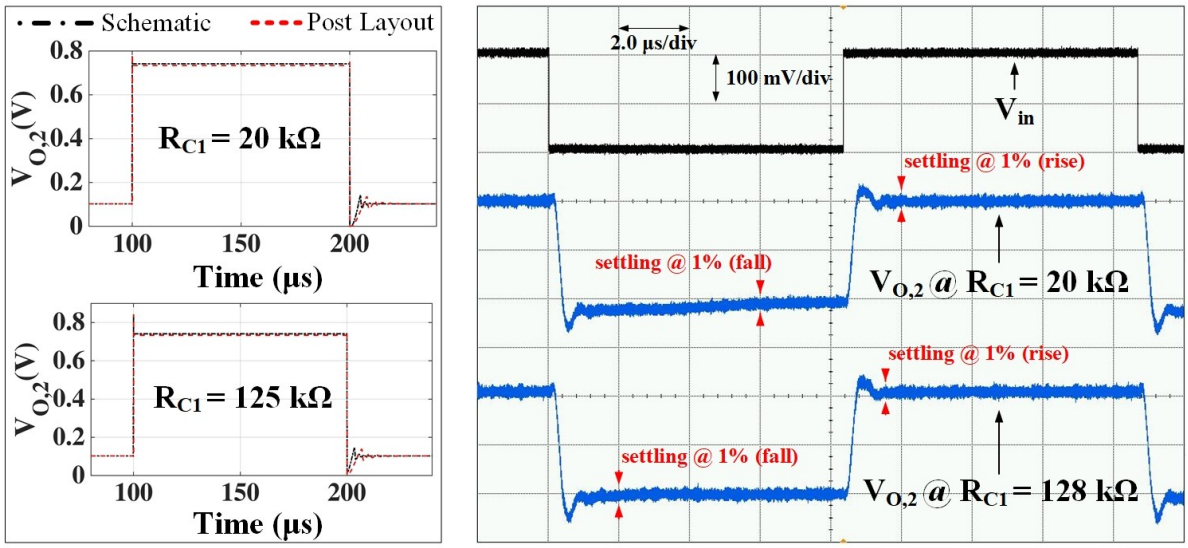

Fig. 5.4: The closed-loop unity-gain step response results: (a) schematic and post-layout simulations for R_{C1} = 20 kΩ (upper part) and R_{C1} = 128 kΩ (lower part), and (b) measured step response when applying a step input of 200 mV for R_{C1} = 20 kΩ and R_{C1} = 128 kΩ.

TABLE 5.3
THE IMPACT OF SWEEPING R_{C1} ON THE OPEN-LOOP P-Z PAIR RATIO (ω_{P1}/ω_{Z1})

R_{C1} (kΩ)	20	40	60	80	100	125
ω_{P1}/ω_{Z1}	0.89	1.87	2.85	3.8	4.81	5.81

Fig. 5.5 summarizes the relationship between R_{C1} (i.e., the increase in A_Z according to Fig. 5.4) and the settling time. This figure clearly validates the theory in Fig. 3.6(a), and it is true for schematic, post layout, and measured results. Also, it is true when the response settles to 1% and 0.01% of the final value.

5.1.2.3. Robustness Tests

Fig. 5.6(a) shows the design robustness against PVT variations for open-loop (upper part) and closed-loop (lower-part) responses for R_{C1} = 20 kΩ. Based on these PVT simulations, the maximum ω_t was obtained at the Fast-Slow (FS) corner with a value of 191 MHz and a PM of

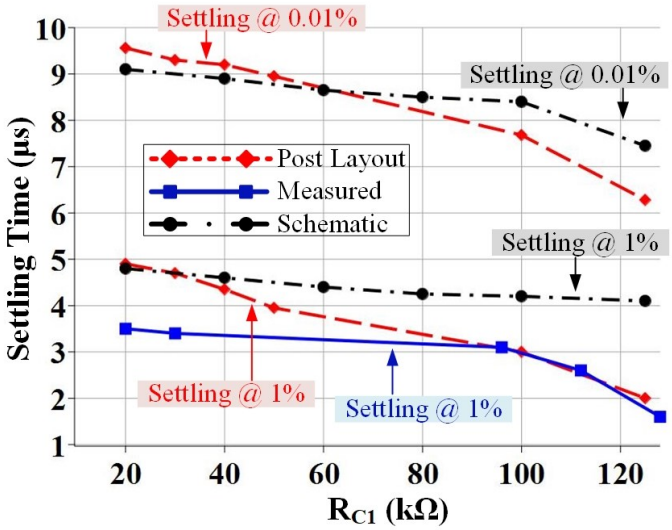

Fig. 5.5: Settling time behavior when sweeping R_{C1} from 20 kΩ to 125 kΩ (i.e., sweeping A_Z form 0.6 dB to 23 dB) for the case of having one *P-Z* pair. This Figure validates Fig. 3.6(a).

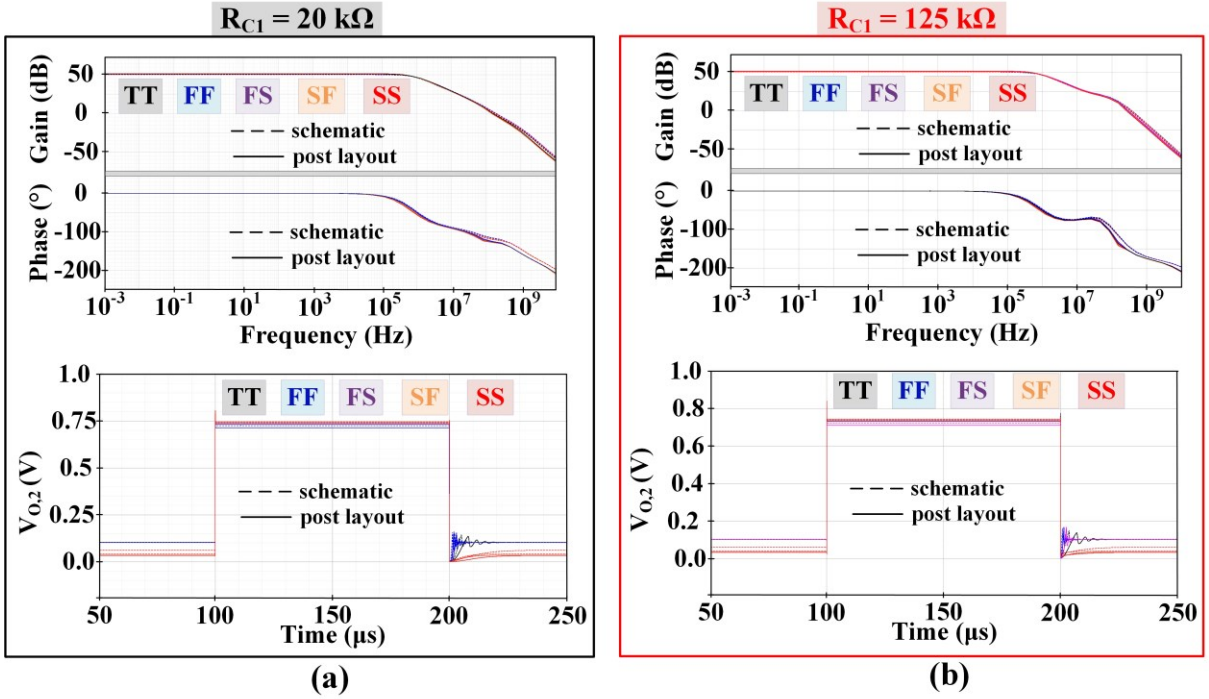

Fig. 5.6: Robustness and Stability tests: (a) the open-loop (upper part) and the closed-loop (lower part) responses under different process corners to show the design robustness against PVT variations for both schematic and post-layout simulations for R_{C1} = 20 kΩ, and (b) The open-loop (upper part) and the closed-loop (lower part) responses under different process corners to show the design robustness against PVT variations for both schematic and post-layout simulations for R_{C1} = 125 kΩ.

62°, while the minimum ω_t was obtained at Slow-Slow (SS) corner with a value of 140 MHz and a PM of 52.4°. The same can be concluded for the case of R_{C1} = 125 kΩ in Fig. 5.6(b).

5.2. Verification of the Proposed Theory Having *N*-1 Pole-Zero Pairs

The proposed theory in Chapter 3 suggests that once increasing A_Z, the open-loop *P-Z* pairs' impact on settling time will be reduced, regardless of open-loop *P-Z* pairs' numbers or their separation distances (i.e., ω_{PI}/ω_{ZI}).

To verify the proposed theory, one should design an OTA which can provide a wide range of DC gains. At the same time, this OTA should have the capability to create a specific number of *P-Z* pairs and offers the capability to accurately control their positions and the distances between them.

5.2.1. The OTA Design Setup

The circuit of Fig. 4.3 shows the design of *N*-stage CMOS OTAs. If one can follow the proposed technique of Chapter 4 to design each gain stage to achieve a specific DC gain, this circuit can provide a wide and a scalable DC gain. Also, the circuit of Fig. 4.3 can create a *P-Z* pair whenever a gain stage and its R-C compensation circuit are added. Therefore, the proposed theory can be verified by following the technique which has been described in Chapter 4 (with C_L = 1 pF) to design 2- to 8-stage CMOS OTAs. This design example will also demonstrate how the generalized theory unveils opportunities for many-stage CMOS OTA design.

TABLE 5.4
DEVICES' SIZES OF 2- TO 8-STAGE CMOS OTA OF FIG. 4.3 AND FIG. 4.4(a)

Device	Aspect Ratio/Size	Device	Aspect Ratio/Size
$M_1 = M_2 = M_{C2}$	2 µm / 1 µm	$M_{6,i}$*	4.8 µm / 455 nm
$M_3 = M_4 = M_{C3} = M_{C4}$	0.6 µm / 130 nm	$M_{7,i}$*	5 µm / 130 nm
$M_5 = M_{C5}$	2 µm / 620 nm	M_{C1}	1 µm / 1 µm

* i = 2 to 8

TABLE 5.5
COMPONENT VALUES USED IN THE COMPENSATION CIRCUITS FOR THE REALIZATION OF DIFFERENT OTA STAGES

Component / OTA stage	Compensation Capacitors (pF)							Compensation Resistors (kΩ)						
	C_{C1}	C_{C2}	C_{C3}	C_{C4}	C_{C5}	C_{C6}	C_{C7}	R_{C1}	R_{C2}	R_{C3}	R_{C4}	R_{C5}	R_{C6}	R_{C7}
2-stage OTA	0.05	-	-	-	-	-	-	180	-	-	-	-	-	-
3-stage OTA	0.25	0.05	-	-	-	-	-	100	60	-	-	-	-	-
4-stage OTA	0.5	0.25	0.05	-	-	-	-	80	60	50	-	-	-	-
5-Stage OTA	2	0.5	0.25	0.05	-	-	-	60	40	40	60	-	-	-
6-stage OTA	4	2	0.5	0.25	0.05	-	-	40	40	40	40	40	-	-
7-stage OTA	8	4	2	0.5	0.25	0.05	-	40	40	30	30	30	50	-
8-stage OTA	12	8	4	2	0.5	0.25	0.05	40	40	35	35	30	25	20

The purpose of designing 2- to 8-stage CMOS OTAs is to provide a scalable DC gain in the range of 50 dB to 200 dB to obtain the same range that has been used in the theory as seen in the X-axis of Fig. 3.9. Therefore, each stage has been designed to achieve an A_{DC} of 25 dB (including the differential input-stage). This pins-down the required sizes of all transistors to meet power consumption and overdrive voltage requirements. Also, this defines the values of the small-signal parameters (i.e., g_m and r_O) of all transistors. The transistor sizes used in this design can be seen in Table 5.4.

Also, by following the proposed frequency compensation technique, which has been proposed in Section 4.3, the poles and zeros are positioned according to Eqn. (4.4). The values of these R-C compensation circuits are listed in Table 5.5. Apart from $R_{C4,(5\text{-stage})}$ and $R_{C6,(7\text{-stage})}$,

TABLE 5.6
THE OPEN-LOOP *P-Z* PAIRS' POSITIONS OF 7-STAGE AND 8-STAGE CMOS OTAS
[For 7-Stage OTA: $\omega_{P0,7\text{-}stage}$ = 1.76 kHz, and $\omega_{t,7\text{-}stage}$ = 215.5 MHz]
[For 8-Stage OTA: $\omega_{P0,8\text{-}stage}$ = 1.4 kHz, and $\omega_{t,8\text{-}stage}$ = 331.3 MHz]

		1st pair	**2nd pair**	**3rd pair**	**4th pair**	**5th pair**	**6th pair**	**7th pair**
7-stage	**poles (Hz)**	-2.288 x10^4	-1.236 x10^6	-1.208 x10^7	-3.211 x10^7	-3.739 x10^7	-7.557x10^7 ± j 1.023 x10^8	-
	zeros (Hz)	-2.288 x10^4	-1.236 x10^6	-1.236 x10^7	-2.473 x10^7	-3.723 x10^7	-1.241 x10^8	-
8-stage	**poles (Hz)**	-2.109 x10^4	-2.587 x10^6	-1.224 x10^7	-3.232 x10^7	-3.516 x10^7	-3.484x10^7 ± j 2.098 x10^8	-3.083x10^8 ± j 2.735 x10^7
	zeros (Hz)	-2.1 x10^4	-2.587 x10^6	-1.236 x10^7	-3.069 x10^7	-3.235 x10^7	-2.03 x10^8	-3.389x10^8 ± j 1.367 x10^7

which are increased for better PM, all sizes follow from Eqn. (4.15). Also, apart from $R_{C3,(8\text{-}stage)}$ and $R_{C4,(8\text{-}stage)}$, which are increased for better PM, all sizes follow from Eqn. (4.16).

5.2.2. Simulation Results

Based on the transistors` sizes in Table 5.4, and the R-C compensation circuits in Table 5.5, the distribution of the *P-Z* pairs in the 7- and 8-stage OTAs are shown in Table 5.6 as an example. Since the exact positioning of these *P-Z* pairs is not required, nor their exact numbers, and since the positioning is being done in a relatively small frequency range, getting *P-Z* cancellations in some entries of Table 5.6 is expected, and it is one of the design limitations. Nevertheless, having *P-Z* cancellation in some *P-Z* pairs will not impact the overall OTA's response.

Before discussing the verification of the proposed theory, Fig. 5.7(a) shows the open-loop *AC* response of the 2- to 8-stage CMOS OTAs. Since the proposed OTA is meant for closed-loop operations, a test of its stability under large and small input-signals is shown in Fig. 5.7(b). These simulations have been conducted for all stages, but, for simplicity, part of these transient

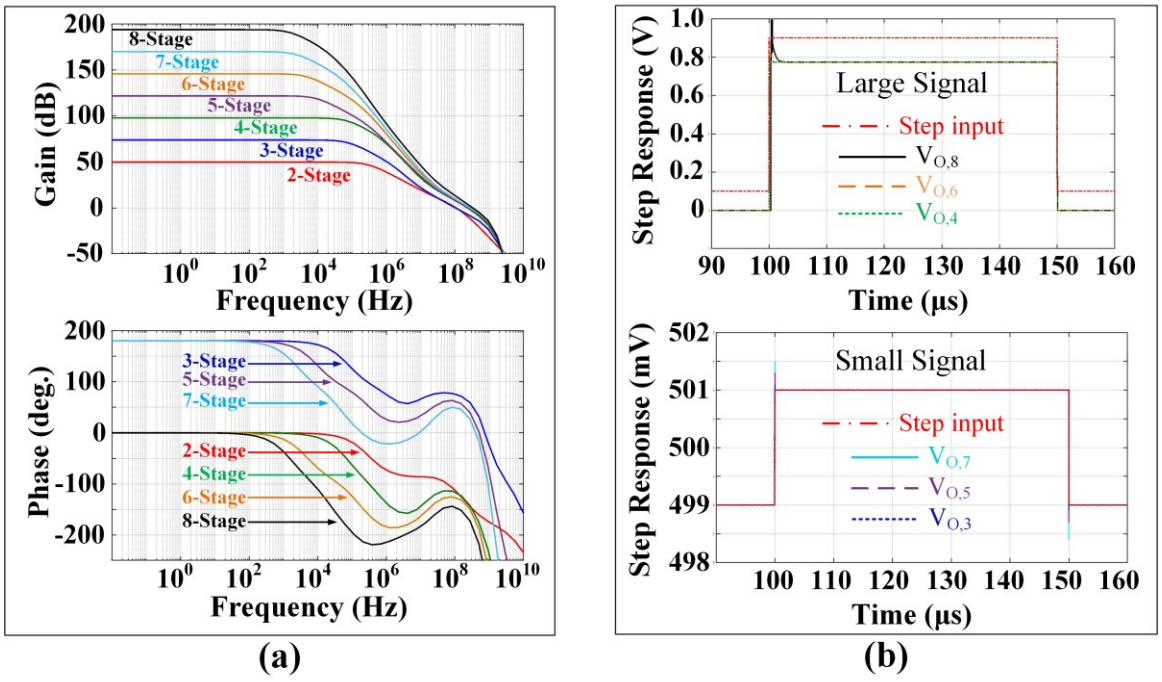

Fig. 5.7: Simulation results of the proposed OTA design of Fig. 4.3: (a) the open-loop *AC* response of the 2- to 8-stage OTAs, (b) stability tests, using the closed-loop unity-gain step response of the proposed 4-, 6-, and 8-stage OTAs subject to a large signal of 800 mV (upper part) and stability test for 3-, 5-, and 7-stage OTAs subject to a small signal of 2 mV (lower part).

responses is being shown here and the rest are reported in Appendix H. Apart from the overshoot that can be seen in the step response, the closed-loop operation is stable. A summary of these results will be discussed in subsection 5.2.4.

Clearly, the circuit of Fig. 4.3 increases the gain and adds *P-Z* pairs whenever a new stage is added. Thus, sweeping the gain for a specific number of *P-Z* pairs to verify the theory in Fig. 3.8 is practically challenging. Nevertheless, one can still measure the improvement in settling time by comparing the settling time at 0.01% of the final value to the settling time at 1% for each stage using *IM* of Eqn. (3.35).

TABLE 5.7
COMPARING THE IMPACT OF GAIN AND NUMBER OF *P-Z* PAIRS ON SETTLING TIME BETWEEN THEORY AND CIRCUIT SIMULATIONS

	Metric	N = 2	N = 3	N = 4	N = 5	N = 6	N = 7	N = 8
Theory -Based on Eqn. (3.34)- (The same results are reported in Table 3.5)	**Gain: A_Z (dB)**	**50**	**75**	**100**	**125**	**150**	**175**	**200**
	Settling time @ 1% (sec)	0.016	0.297	0.885	1.26	1.55	1.75	1.93
	Settling time @ 0.01% (sec)	3.45	4.83	5.4	5.75	6.05	6.22	6.39
	***IM in settling time* (theory)**	**215.6**	**8.1**	**2.03**	**1.1**	**0.78**	**0.59**	**0.47**
Circuit Realization -Based on the simulation results of Fig. 5.7-	**Gain: A_{DC} (dB)**	**50**	**73.7**	**97.75**	**121.7**	**145.7**	**168**	**193.6**
	Settling time @ 1% (μs)	0.031	0.173	0.069	1.25	0.295	6.84	0.885
	Settling time @ 0.01% (μs)	0.08	0.316	0.16	2.08	0.655	10.45	1.89
	***IM* in settling time (circuit)**	**2.58**	**0.91**	**0.77**	**0.42**	**0.44**	**0.25**	**0.3**

Table 5.7 compares the settling time results which are obtained based on the circuit level simulations with the results which are obtained by the theory in Section 3.3 (i.e., Eqn. (34) and Fig. 3.8). The results are obtained here for the same conditions in both cases: theory and circuit level realization. This means that the gain (i.e., the number of stages *N*) is almost equal for both cases. Also, the same *P-Z* pairs' numbers are ensured while obtaining the settling time for these two cases. The only difference between both cases is that the theory is showing normalized values of settling time, while the circuit level realization is not. For this reason, one can see a large difference between settling time of both cases.

Fig. 5.8 shows how *IM* is decreasing when increasing the gain. This is true for both theory and circuit realization; thus, it verifies the proposed theory in Fig. 3.9.

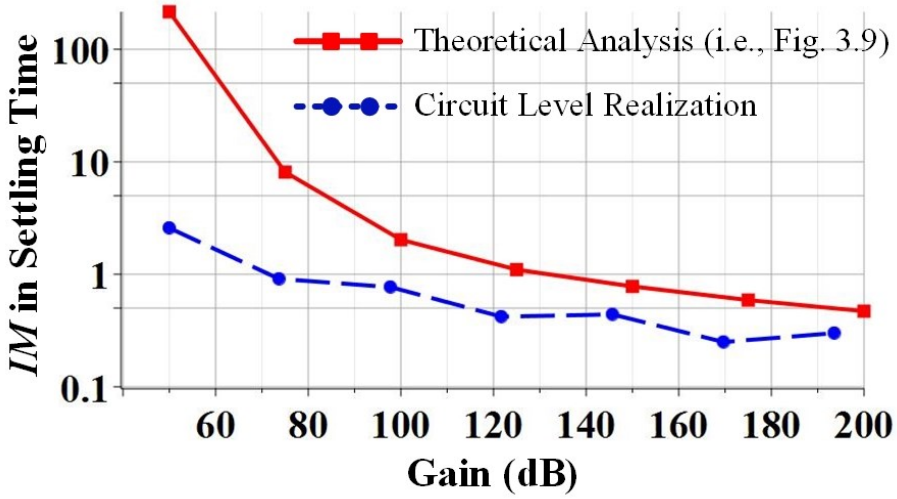

Fig. 5.8: The Improvement Metric (*IM*) in settling time when increasing the gain for both theory and circuit level realization.

However, the decreasing in *IM* for the circuit level realization is not uniform compared to the theoretical behavior. The reason is that the distance between all open-loop *P-Z* pairs in theory is 1 rad/s, whereas the distance between the open-loop *P-Z* pairs in the circuit realization of Fig. 4.3 is not uniform. To illustrate this, Table 5.6 shows the exact *P-Z* pair's positions of the 8-stage OTAs as an example. It is clear that most zeros are positioned at *LF*s (compared to ω_t); however, the ratios between the *P-Z* pairs are different. This applies to the *P-Z* pairs of each stage and the *P-Z* pairs between different stages, and it is true for $N = 2$ to 8.

Also, it is expected to have the lowest *IM* when $N = 8$, but *IM* for $N = 7$ is slightly lower in the circuit level realization. The reason is the *P-Z* cancellation of the 1st and 2nd *P-Z* pairs in the 7-stage OTA, where $\omega_{P1,7}$ and $\omega_{Z1,7}$ are allocated at -2.288 x10^4, while $\omega_{P2,7}$ and $\omega_{Z2,7}$ are allocated at -1.236 x10^6. Thus, two *P-Z* pairs are with almost no impact in the closed-loop operation of the 7-stage OTA.

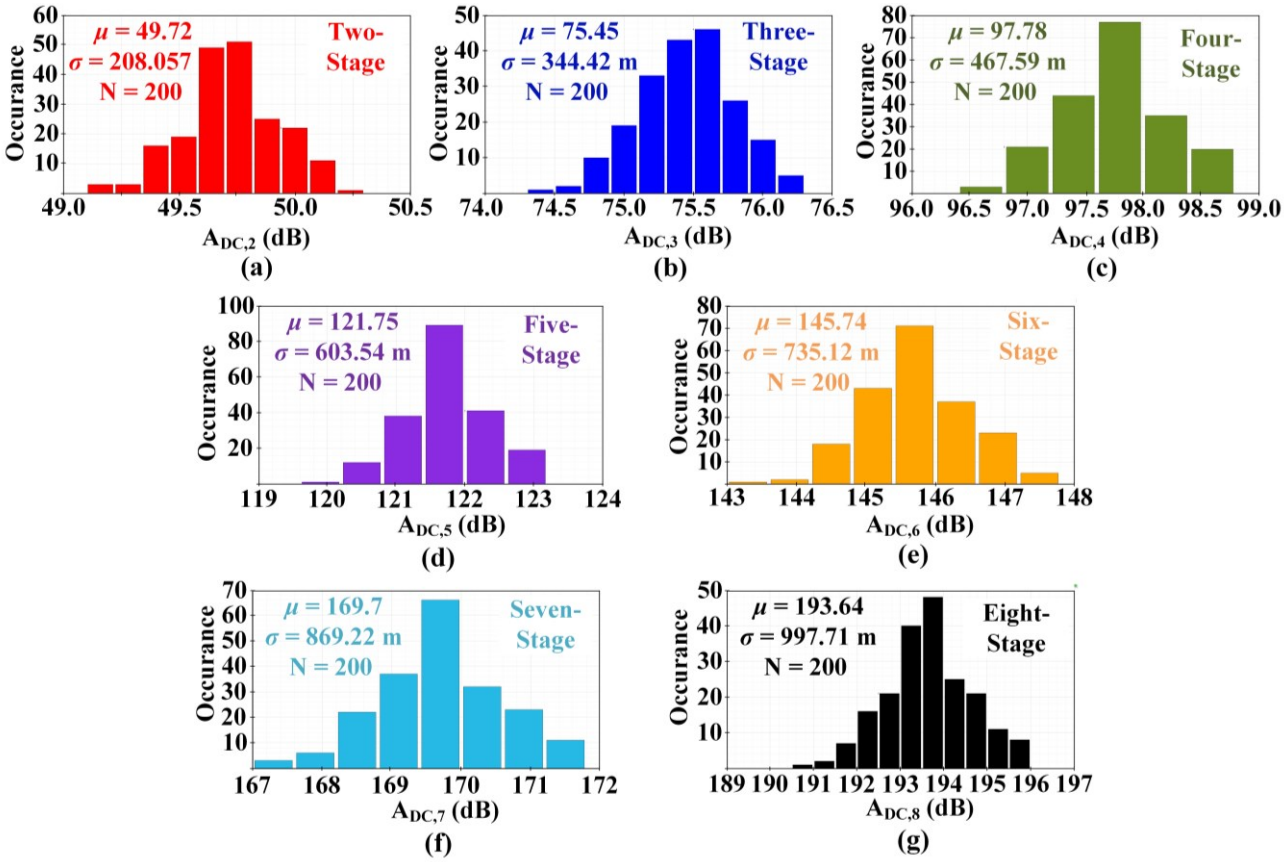

Fig. 5.9: The open-loop DC gain Monte Carlo Simulations for the (a) 2-stage OTA, (b) 3-stage OTA, (c) 4-stage OTA, (d) 5-stage OTA, (e) 6-stgae OTA, (f) 7-stages OTA, and (g) 8-stage OTA.

5.2.3. Robustness Tests

The tests for design robustness using A_{DC} Monte-Carlo (MC) simulations for the 2- to 8-stage CMOS OTA are provided in Fig. 5.8, where the relative percent errors of less than 1.5% were obtained. Also, to ensure the robustness of the proposed design against PVT variations, the 6-stage OTA was used as an example. The PVT varations are considered for all circuit compnents. Table 5.8 shows that the proposed design is robust under different process corners. The same conclusion can be made for all other satges of the proposed design of Fig. 4.3.

TABLE 5.8
ROBUSTNESS TESTS: PVT VARIATIONS FOR THE 6-STAGE CMOS OTA OF FIG. 4.3.

Metric \ Process Corner	SS	SF	TT	FS	FF
DC gain (dB)	148.5	145.8	**145.7**	145.3	144.4
BW (kHz)	3.69	4.3	**4.4**	4.56	5.2
ω_t (MHz)	234.1	251.9	**276.3**	298.3	336.8
PM (deg.)	35	32.6	**30.1**	25.7	18.6
T_S at 0.01% (ns)	653	465.6	**655**	800	806
Avg. SR (V/µs)	24.65	35.35	**37.95**	32.4	28.67

5.2.4. Comparison

In order to appreciate the advantages of the presented many-stage OTA design, it is important to compare the results presented here with other recent works that report different designs of multi-stage OTAs. Table 5.9 shows a summary of these results. In order to facilitate this comparisson, a small signal figure-of-merit (FOM_S) and a large signal figure-of-merit ($SIFOM_L$) are defined as [18]:

$$\mathrm{FOM_S} = \frac{\mathrm{GBP} \cdot \mathrm{C_L}}{\mathrm{Power}} \ , \tag{5.1}$$

and

$$\mathrm{SIFOM_L} = \frac{\mathrm{GBP} \cdot \mathrm{C_L}}{T_S \,.\, \mathrm{Power}} \ . \tag{5.2}$$

It is evident from Table 5.9 that the proposed design compares well to recent 2- and 3-stage designs, while outperforming those with 4- and 5-stage. Notably, 6-, 7-, and 8-stage OTAs have not been reported in litreature before. Clearly, the 6-, 7-, and 8-stage OTA significantly outperfoms all other stages.

TABLE 5.9
SUMMARY OF RESULTS AND PERFORMANCE COMPARISON WITH MOST RECENT PUBLISHED WORKS

Ref. / Metric	[106] 2019	This Work	[107] 2020	[92] 2020	This work	[23] 2015	[24] 2020	This work	[18] 2016	This work	This work	This work	This work
# of Stages	Two-stages		Three-Stages			Four-Stages			Five-Stages		Six	Seven	Eight
CMOS process	180nm	65nm	180nm	130nm	65nm	350nm	130nm	65 nm	130nm	65 nm	65 nm	65 nm	65 nm
V_{DD} (V)	1.8	1	0.3	1	1	3	1.2	1	1.2	1	1	1	1
DC gain (dB)	84	50	98.1	72.4	73.7	173	107	97.75	150	121.7	145.7	168	193.6
GBP (MHz)	91	87.7	0.0031	4.23	363.1	2.9	2.75	2807.7	885437	10945.6	84811	442092	6253570
Power (µW)	3100	38.8	0.013	95	66.9	156	175.2	94.9	10200	123	150.9	178.9	206.9
C_L (pF)	100	1	30	90	1	1000	400	1	1	1	1	1	1
ω_t (MHz)	91	128.6	0.0031	4.23	103.7	2.9	2.75	231.8	20	248.1	276.3	215.5	331.3
T_S at 1% (µs)	-	0.031	-	0.2	0.173	0.46	0.33	0.069	1.27	1.25	0.295	6.84	0.885
T_S at 0.01%(µs)	-	0.08	-	-	0.316	-	-	0.16	-	2.08	0.655	10.45	1.89
FOM_S	2.93	2.26	7.1	4	5.4	18.5	6.2	29.5	86.8	88.98	565.4	2471.1	30225.08
$SIFOM_L$	-	72.9	-	20	31	40.2	18.7	427.5	68.3	71.1	1916.6	361.2	34152.6

5.3. Summary

This chapter has verified and validated the proposed theory of Chapter 3 through a design example of a 2- to 8-stage CMOS OTAs, where the standard 65 nm TSMC CMOS process was used for the design of the OTA. Since the main contribution of Chapter 3 has been captured in Fig. 3.5, Fig. 3.6, and Fig. 3.9, this chapter has reproduced these figures through simulations (schematic and post-layout) as well as some measurement results. **Consequently:**

1. **Fig. 3.5 has been verified in Fig. 5.1,**
2. **Fig. 3.6(a) has been verified in Fig. 5.5, and**
3. **Fig. 3.9 has been verified in Fig. 5.8.**

CHAPTER 6

VERIFICATION & VALIDATION OF THE PROPOSED SCALABLE MANY-STAGE CMOS OTA

The proposed theory in Chapter 4 has introduced the design of a scalable many-stage CMOS OTAs with an ultra-wide range C_L. As mentioned in the summary of Chapter 4, the main contribution of this scalable many-stage OTA design has been captured in Fig. 4.6, Fig. 4.7, and Fig. 4.8. Accordingly, this chapter will verify and validate the proposed design technique through extensive simulations (schematic and post-layout) and measurement results. By following the steps in Eqs. (4.3) and (4.4), and the detailed procedure of Section 4.2, 4.3, and 4.4, the OTA of Fig. 4.3 has been designed to achieve a scalable DC gain while driving a wide range of C_Ls. The standard TSMC 65 nm CMOS process has been used to design this OTA with a supply voltage (V_{DD}) of 1 V. Also, Cadence CAD tools have been used for simulation purposes. Despite being applicable to *N*-stage OTAs, the proposed FCT will be verified by discussing the design of 2-, 3-, and 4-stage OTAs for simplicity and as a proof-of-concept.

This chapter starts by discussing the design choice for the gain stages in Section 6.1 to pin-down the transistors sizes and the small signal parameters. Then, the detailed verification of Step

(1) and Step (2) of the proposed FCT are discussed in Section 6.2 and 6.3, respectively. These discussions are based on schematic and post-layout simulations. Section 6.4 shows the experimental results, while Section 6.5 shows robustness of the proposed FCT. In Section 6.6, the proposed 2-, 3-, and 4-stage CMOS OTAs are compared with the state-of-the-art works. Finally, Section 6.7 summarizes the work presented in this chapter.

6.1. Designing the OTA Gain Stages

First, each gain stage has been designed to achieve a DC gain of about 25 dB, thus, the 2-, 3-, and 4-stage OTAs of Fig. 4.3 are providing a post-layout A_{DC} of 51.18 dB, 77.2 dB, and 92 dB, respectively. To achieve this, the gain stages have been biased with gate voltages at about 0.5 V (i.e, $V_{DD}/2$) and the CS transistors are designed to be identical with the sizes shown in Table 6.1. Also, the current source transistors (i.e., M_5 and $M_{7,i}$) are biased at I_{BIAS} = 6 µA. Consequently, the small signal parameters are shown in Table 6.2.

For the 2- and 3-stage OTA, the CMFB circuit of Fig. 4.4(a) has been used, while the CMFB circuit of Fig. 4.4(b) has also been added for the 4-stage OTA with I_{BIAS_1} = 3 µA. Due to the loading effect of the CMFB circuit of Fig. 4.4(b), the 4-stage OTA has achieved an $A_{DC,4}$ of 92 dB instead of values around 100 dB.

Once designing the OTA for the required DC gain, the practical focus will be verifying the proposed FCT by designing the compensation circuits according to Step (1) and (2) (i.e., Eqn. (4.2) and (4.3)), so that ω_t is enhanced to a near-optimum value to allow the OTA to drive a wide C_L range. These steps will be discussed in the following sections.

TABLE 6.1
DEVICES' SIZES OF THE PROPOSED SCALABLE *N*-STAGE CMOS OTA OF FIG. 4.3 AND THE CMFB CIRCUITS OF FIG. 4.4

Device	Size
$M_1 = M_2 = M_{C2} = M_{B1} = M_{B2}$	2 × (1 µm / 390 nm)
$M_3 = M_4 = M_{B3} = M_{B4}$	8 × (0.75 µm / 325 nm)
$M_5 = M_{C5} = M_{B5}$	4 × (1.1 µm / 520 nm)
$M_{6,i}^* = M_{B6}$	8 × (0.55 µm / 130 nm)
$M_{7,i}^*$	10 × (0.66 µm / 260 nm)
M_{C1}	1 × (1 µm / 390 nm)
M_{CM}	2 × (0.6 µm / 260 nm)
R_B	44 kΩ
C_B	0.5 pF

* $i \leq N$.

TABLE 6.2
THE VALUES OF THE SMALL-SIGNAL PARAMETERS OF THE DIFFERENTIAL PAIR STAGE AND THE CS-STAGES

Parameter	Size	Parameter	Size
$g_{m,M2}$	112.2 µA/V	$g_{m,M6,i}^*$	540.9 µA/V
$r_{O,M2}$	70.23 kΩ	$r_{O,M6,i}^*$	11.96 kΩ
$g_{m,M4}$	113.6 µA/V	$g_{m,M7,i}^*$	695.7 µA/V
$r_{O,M4}$	68.4 kΩ	$r_{O,M7,i}^*$	12 kΩ

* $i \leq N$.

6.2. Verification of Step (1) in the Proposed FCT: Increase ωt under $C_L = 0.5$ pF

The proposed FCT starts by designing the 2-stage OTA's R-C compensation circuit (according to Step (1)) having $C_{L,min}$ = 0.5 pF. Therefore, the value of $C_{C1,(2\text{-stage})}$ has been selected to be

TABLE 6.3
THE OPEN-LOOP PARAMETERS AND THE *P-Z* PAIRS' POSITIONS OF THE PROPOSED 2-, 3-, AND 4-STAGE CMOS OTAS OF FIG. 4.3 UNDER C_L = 0.5 PF

OTA Stage	Band-Width	1st P-Z pair		2nd P-Z pair		3rd P-Z pair		f_t (MHz)	f_{par} (GHz)	*PM* (º)
	f_{P_3dB} (kHz)	f_{P1} (MHz)	f_{Z1} (MHz)	f_{P2} (MHz)	f_{Z2} (MHz)	f_{P3} (MHz)	f_{Z3} (MHz)			
Two-Stage	**846.6**	180.5	166.3	-	-	-	-	**293.2**	**0.787**	**70.9**
Three-Stage	**191.1**	10.06	15.03	167	165.4	-	-	**548.2**	**1.527**	**57**
Four-Stage	**89.51**	1.8	14.58	12.4	29.1	59.4	32.1	**288.4**	**1.192**	**67.1**

almost 5 times the value of the parasitic capacitance given by the technology (i.e. C_{C1} = 50 fF). For $R_{C1,(2\text{-stage})}$, the value has been swept starting from 1 kΩ, and kept increasing till $R_{C1,(2\text{-stage})}$ reached a value of 21 kΩ. Thus, ω_t has become 293.2 MHz. This value of ω_t is near optimum as PM = 70.9 º, which is a reasonable value to indicate stability.

The frequency positions of the poles and the zero after designing the 2-stage OTA's R-C circuit according to Step (1) are shown in Table 6.3. Clearly, these values are satisfying Eqn. (4.4) and the parasitic pole is twice the value of ω_t.

Following the scalable technique given by Eqs. (4.13)-to-(4.16), the R-C compensation circuits of the 3- and 4-stage OTAs are designed as shown in Table 6.4. Based on these values, Table 6.3 shows all open-loop frequency parameters. Even though Eqn. (4.4) has not been fully satisfied for 3- and 4-stages, where some *P-Z* pairs are having ω_{Pi} at frequencies less than ω_{Zi}, the PM has reached values around 60º. Also, ω_t is at high frequencies and the parasitic poles are still higher than ω_t.

TABLE 6.4
COMPONENT VALUES USED IN THE COMPENSATION CIRCUITS FOR THE REALIZATION OF DIFFERENT OTA STAGES

Components / OTA Stage	Compensation Caps. (pF)			Compensation Resistor (kΩ)		
	C_{C1}	C_{C2}	C_{C3}	R_{C1}	R_{C2}	R_{C3}
Two-Stage	0.05	-	-	21	-	-
Three-Stage	0.25	0.05	-	44*	21	-
Four-Stage	0.5	0.25	0.25*	12.6	44	21

* These values are not exactly following the scalable pattern of Eqs. (4.14) and (4.16) as they have been tweaked to achieve PM values of around 60º.

Fig. 6.1 summarizes all schematic and post-layout results for open-loop and closed-loop configurations after implementing Step (1) of the proposed FCT under C_L = 0.5 pF.

Due to the inverse relationship between Slew Rate (SR) and the capacitors: $C_{C,Eq}$ and C_L, (where $C_{C,Eq}$ is the equivalent capacitance that the compensation capacitors will create in series when N > 2), and since the value of C_L is higher than $C_{C,Eq}$, the SR will be determined by the current flowing in the CS transistor of the last gain stage (i.e., $M_{6,N}$) ($I_{M6,N}$) and C_L. Thus, the SR can be approximated as

$$SR \approx \frac{I_{M6,N}}{C_{C,Eq} + C_L} \quad . \tag{6.1}$$

If a very large C_L is required, one can increase the value of $I_{M6,N}$ to keep the SR within sufficient values. However, by designing the OTA to have a high $I_{M6,N}$, the power consumption will increase. This will become a trade-off between C_L, SR, and power consumption. The post-layout power consumption in the proposed designs is 106 µW, 180.1 µW, and 243.5 µW for the 2-, 3-, and 4-stage OTAs, respectively. Also, one should consider that this value is for a fully differential-ended topology.

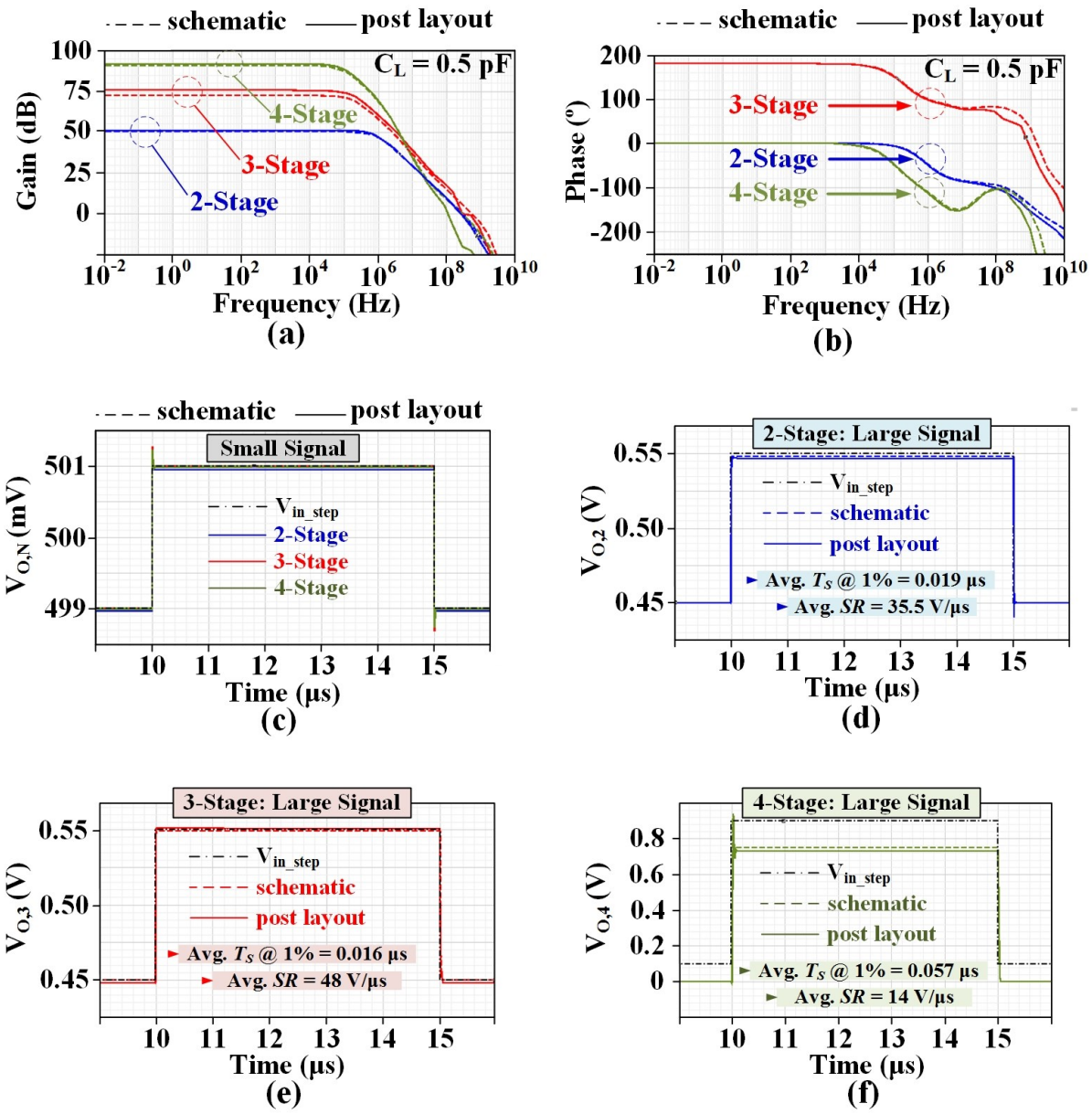

Fig. 6.1: Schematic and post-layout simulations of the open-loop and unity-gain closed-loop configurations of the differential-ended 2-, 3-, and 4-stage CMOS OTAs of Fig. 4.3 after implementing the proposed FCT under C_L = 0.5 pF, (a) the AC magnitude response, (b) the AC phase response, (c) the 2, 3-, and 4-stage step responses subject to a small-signal of 2 mV step input, (d) the 2-stage step response subject to a large-signal of 100 mV step input, (e) the 3-stage step response subject to a large-signal of 100 mV step input, (e) the 4-stage step response subject to a large-signal of 800 mV step input.

Even though many resistors are being used in the proposed OTAs, the noise has not been affected that much, because the resistors mainly affect the noise of the output stage, while the 1st stage noise is the dominant noise. Therefore, the post-layout input referred noise at 10 kHz is 82.2 nV/$\sqrt{\text{Hz}}$ for the 2- and 3-stage OTAs and 78.1 nV/$\sqrt{\text{Hz}}$, for the 4-stage OTA.

6.3. Verification of Step (2) in the Proposed FCT: Maximize C_L for a Desired Settling Time

After designing the proposed OTAs to properly drive $C_{L,min}$ of 0.5 pF, the goal now is to define the range of C_L under which the 2-, 3-, and 4-stage OTAs' closed-loop responses are stable, and to find the corresponding settling time for this range of C_L. Therefore, similar steps of creating Fig. 4.7 and Fig. 4.8 (i.e., investigating the PM and the settling time variations vs. the increase in C_L) are being followed here.

Consequently, Fig. 6.2 shows the simulation results of PM vs. C_L. Apparently, the proposed 2-stage OTA (solid-blue line with circles) is stable with PM ≥ 45º, for all values of C_L, except between 10 pF to 100 pF where it goes slightly below 45º. Therefore, it mainly follows *Case (1)* of Fig. 4.7, which is the expected response since $\omega_{ZI} < \omega_{PI}$ (as reported in Table 6.3). To define $C_{L,max}$, one can observe the C_L value of Fig. 6.2 at which the PM becomes 90º. Clearly, $C_{L,max}$ is 10 nF; thus, C_L-drivability ratio according to Eqn. (4.17) is 20,000.

As for the proposed 3-stage OTA, the closed-loop response is always stable as the PM doesn't reach the instability region (i.e., green-shaded area of Fig. 6.2) with the increase in C_L. Clearly, the PM follows *Case (2)* of Fig. 4.7, which is an expected response since $\omega_{ZI} > \omega_{PI}$ of

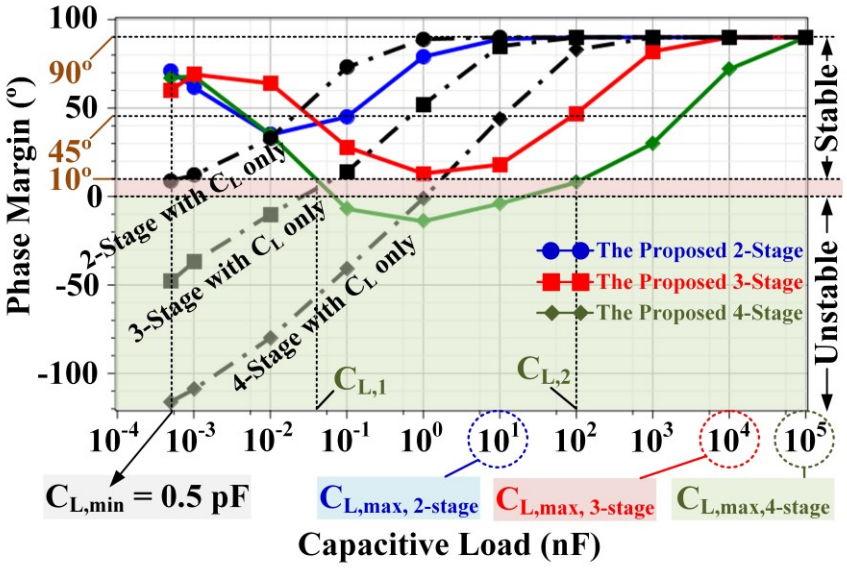

Fig. 6.2: The relationship between PM and C_L as described in Fig. 4.7.

the 1st *P-Z* pair in Table 6.3. Interestingly, with $C_{L,max}$ of 10 µF, C_L-drivability ratio of the proposed 3-stage OTA is 20,000,000.

As for the proposed 4-stage OTA, the PM behavior follows *Case (3)* of Fig. 4.7, where it goes below 10º in between $C_{L,1}$ = 40 pF and $C_{L,2}$ = 100 nF. Again, this is an expected behavior due to the 1st and 2nd *P-Z* pairs' arrangement which can be seen in Table 6.3 (i.e., $\omega_{ZI} >> \omega_{PI}$). Nonetheless, the proposed 4-stage OTA is operating properly under all other values and exhibiting a C_L-drivability ratio of 80,000.

To clearly measure the improvement that has been done by the proposed FCT on C_L-drivability of CMOS OTAs, one can compensate the proposed OTAs with the conventional FCT (i.e., which relies on C_L only to compensate the OTA) and compare the results. Fig. 6.2 shows the PM behavior once conventional techniques are used to compensate for the proposed 2-, 3-,

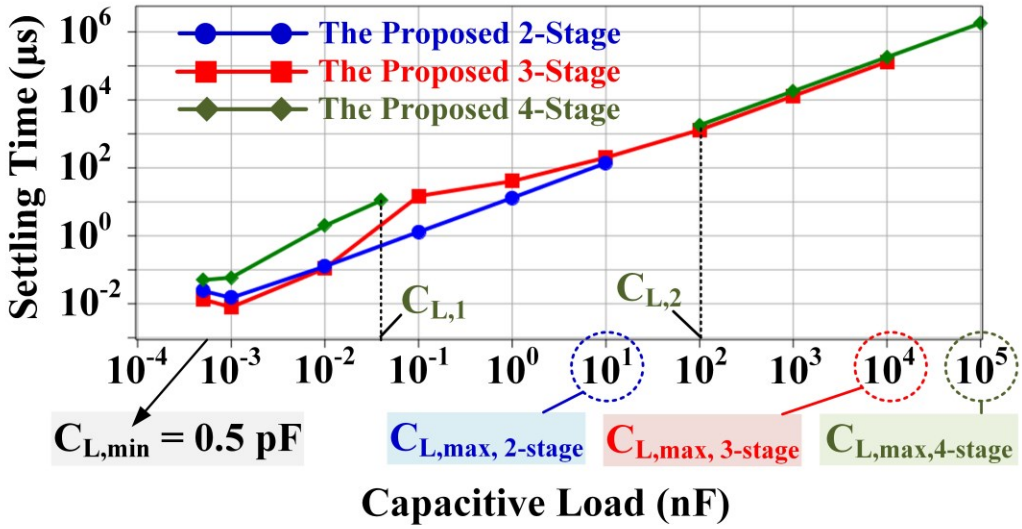

Fig. 6.3: The relationship between settling time and C_L as described in Fig. 4.8.

and 4-stage OTAs (i.e., the dashed-dotted black lines in Fig. 6.2). Clearly, the conventional technique might only work for 2-stage OTA, but it cannot be scaled for higher number of stages (i.e., it is not suitable for scaled-down CMOS technologies) unless large C_Ls are only required, which is not the case in most applications.

The results in Fig. 6.2 pave the way to verify the unity-gain closed-loop step-response of the proposed OTAs to find the relationship between settling time and C_L. Since the settling time is expected to vary based on the different cases of positioning the open-loop *P-Z* pairs as stated in Fig. 4.8, the 2-stage OTA is expected to have the fastest response as it mostly follows *Case (1)*. Fig. 6.3 verifies this for all C_L values above 100 pF. However, although the 3-stage OTA is following *Case (2)*, it exhibits faster response for C_L values below 100 pF. The reason for this can be indicated from Fig. 6.2, where the 3-stage OTA is having higher PM values than the 2-stage OTA in between 1 pF to 100 pF.

All other open-loop and closed-loop simulation-based parameters are being considered as the value of C_L is increasing; but for simplicity, these simulations are shown in Appendix I. Also, all these parameters will be shown as the proposed OTAs are being validated with measurement results in the following section.

6.4. Experimental Results

The standard TSMC 65 nm CMOS process is used to fabricate the differential-ended 2-, 3- and 4-stage CMOS OTAs of Fig. 4.3 with the devices' sizes shown in Table 6.1. Fig. 6.4 shows the fabricated chip's microphotograph. Since a wide range of C_L is required, each proposed OTA has been fabricated twice (i.e., with C_L on-chip for a small C_L = 1 pF and C_L off-chip for higher values). To illustrate the area and the elements in fabricating the proposed differential-ended 2-, 3-, and 4-stage CMOS OTAs, the layout drawing of the 2-stage OTA is embedded and enlarged in Fig. 6.4, where the overall dimensions is 53.9 μm × 39.7 μm, resulting in an area of 0.0021 mm^2. As seen in the layout drawing, R_{C1} dominates the chip's size and occupies almost half the chip's silicon area. But, as C_{C1} is set just above the parasitic level, the overall silicon area remains quite small (total area = 0.0021 mm^2). As seen in the layout drawing, R_{C1} dominates the chip's size and occupies almost half the chip's silicon area. But, as C_{C1} is set just above the parasitic level, the overall silicon area remains quite small (total area = 0.0021 mm^2). The R_C used here is the standard N-well resistor with sheet resistance 316 Ω/square. As for the C_{C1}, a mimcap with the same length and width of 4.8 μm is used for a C_{C1} value of 50 fF. The same can be said for the 3- and 4-stage OTAs, except more silicon area is required as seen in the area-list below the chip's microphotograph in Fig. 6.4. Appendix J gives more details and clarifications

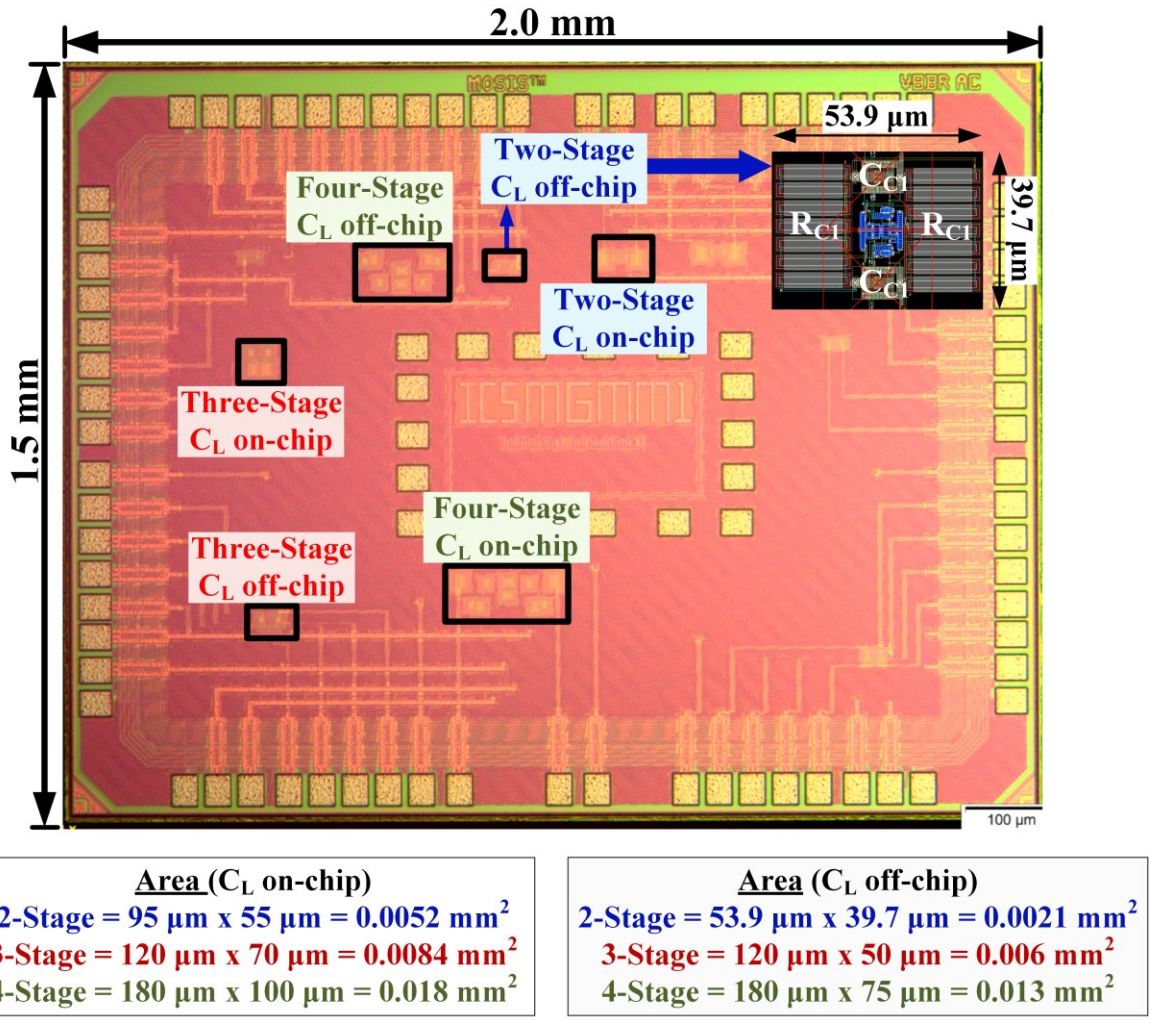

Fig. 6.4: The chip's microphotograph showing the proposed differential-ended 2-, 3- and 4-stage CMOS OTAs with C_L on- and off-chip for each OTA along with the occupied silicon area.

on the layout drawings of the proposed 2-, 3-, and 4-stage CMOS OTAs for the case of having C_L on-chip.

Figure 6.5 shows the measurement setup used to evaluate the 2- , 3-, and 4-stage OTAs' operation. The test equipment is shown in Fig. 6.5(a) along with the PCB's main components. The off-chip biasing circuit and the output buffers are shown in Fig. 6.5(b), (c), and (d),

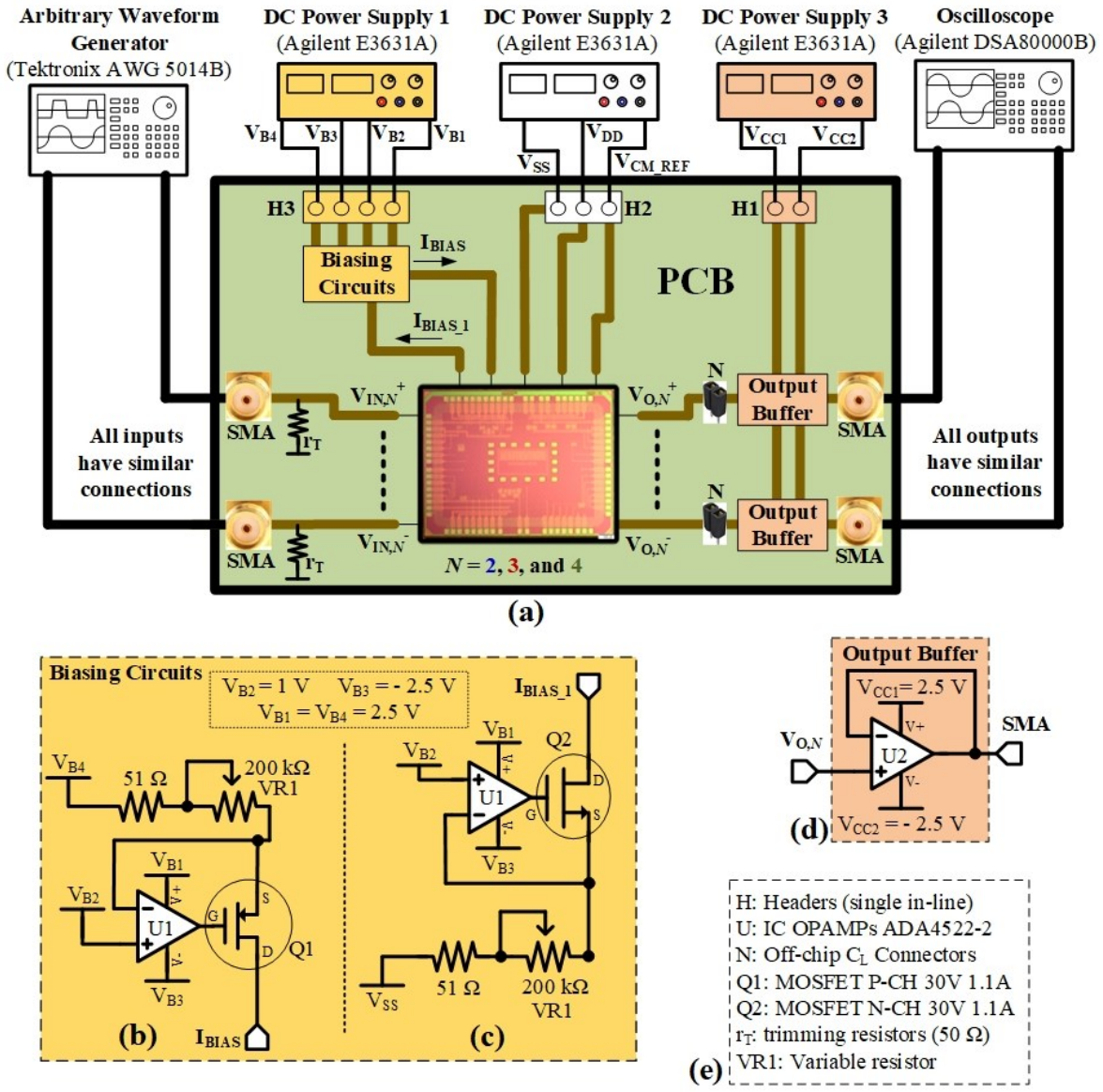

Fig. 6.5: Measurement's setup: (a) the testing equipment and the PCB, (b) the biasing circuit to create I_{BIAS}, (b) the biasing circuit to create I_{BIAS_1}, (d) the output buffer, and (e) the off-chip components which are used to fabricate the PCB for testing purposes.

respectively. In order to power all different components on the PCB, three separate power supplies have been used with the values shown in Fig. 6.5(b) and (c). Also, the off-chip PCB components are listed in Fig. 6.5(e).

TABLE 6.5
THE MEASUREMENTS' BIASING VOLTAGES AND CURRENTS

Biasing Parameters	Two-Stage	Three-Stage	Four-Stage
V_{CM_REF} (V)	0.43	0.47	0.5
V_{IN_BIAS} (V)	0.43	0.49	0.43
I_{BIAS} (µA) & I_{BIAS_1} (µA)	27.2 & N/A	27.2 & N/A	27.2 & 13.6

This chip has been tested in a unity-gain closed-loop configuration to obtain the closed-loop and open-loop performance metrics of each OTA. Table 6.5 lists the critical OTA biasing parameters from a step response test involving a 100 mV step input. Subsequently, Fig. 6.6 show the output step response of the 2-, 3-, and 4-stage OTAs under different values of C_L (i.e., starting from $C_{L,min}$ up to $C_{L,max}$) as captured by an Agilent DSA80000B oscilloscope. The closed-loop performance metrics (i.e. settling time and SR), for different values of C_L, are included on each time plot shown in Fig. 6.6.

By comparing these measurement results with the schematic and post-layout simulation results we found during the verification, one can conclude that these results are in general agreement with one another. Thus, the proposed FCT is being applied properly. It should be noted, however, that the 4-stage OTA has a $C_{L,1}$ and $C_{L,2}$ values that is slightly different than what was predicted by simulation, i.e., 40 pF versus 100 pF for $C_{L,1}$, and 100 nF versus 10 nF for $C_{L,2}$.

As for the open-loop performance metrics (i.e., $A_{DC,N}$ and f_t), one can also use the closed-loop unit-gain step-response to obtain them, where $A_{DC,N}$ can be evaluated according to

$$A_{DC,N} = 20\log_{10}\left[\left(\frac{1}{\varepsilon}\right) - 1\right] \quad , \tag{6.2}$$

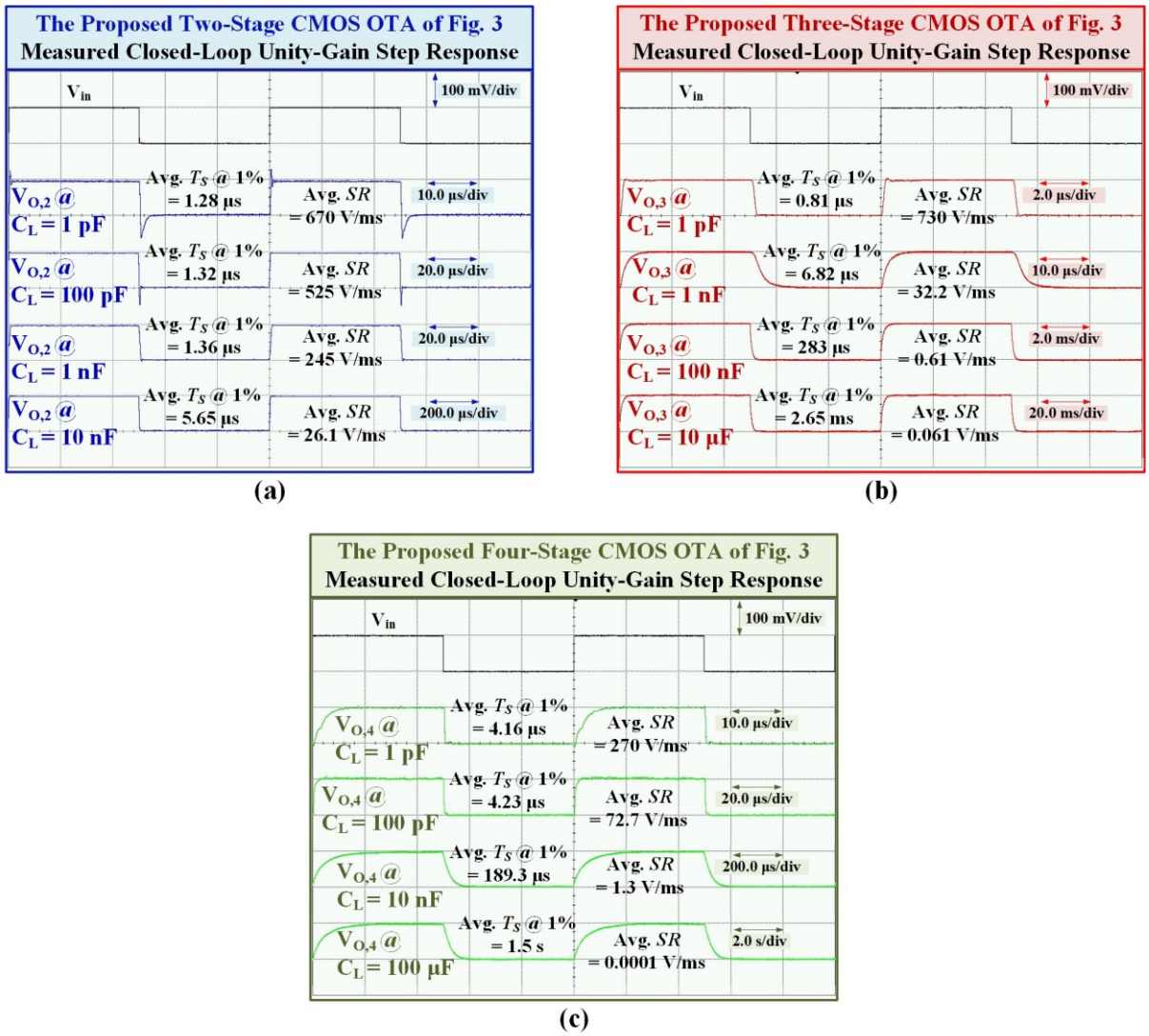

Fig. 6.6: Measurement's results of the unity-gain closed-loop step response under different capacitive load values (a) the proposed two–stage CMOS OTA of Fig. 4.3, (b) the proposed three–stage CMOS OTA of Fig. 4.3, and (c) the proposed four–stage CMOS OTA of Fig. 4.3.

where ε is the final steady-state error of the step response. Although the measured value of ε has no exact value, one can still find the minimum and maximum values of ε in the step response and estimate the value of A_{DC}. For the two-stage OTA, the minimum measured value of ε is 2 mV, which corresponds to an $A_{DC,2}$ of 53.69 dB. Whereas the maximum value of ε is 4 mV, which corresponds to an $A_{DC,2}$ of 47.9 dB. This indicates that $A_{DC,2}$ is about 50.8 dB. The same can be

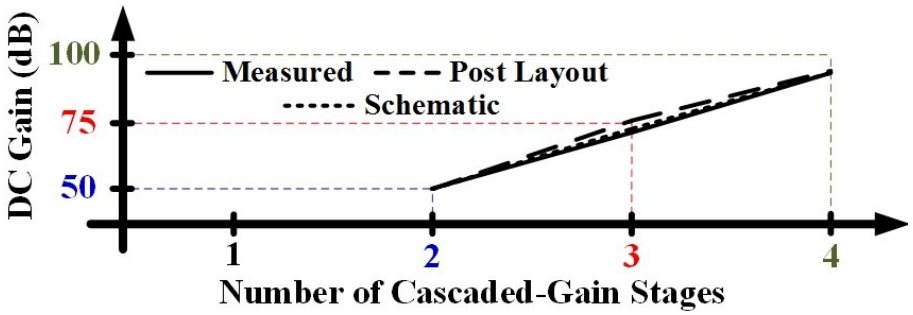

Fig. 6.7: DC gain vs. number of gain stages as described in Fig. 4.6.

TABLE 6.6
MEASUREMENTS' RESULTS OF THE OPEN-LOOP PERFORMANCE METRICS

Metric	**Two-Stage**		**Three-Stage**		**Four-Stage**	
Power (µW)	126.8 @ 1V		227.9 @ 1V		353.1 @ 1V	
C_L	1 pF	10 nF	1 pF	10 µF	1 pF	100 µF
$f_{t,final}$ (MHz)	6.17	0.06	7.75	0.0011	0.47	0.000002

said for the three-, and four-stage OTA, and the approximated value of $A_{DC,3}$ is about 70 dB and 90 db, respectively.

For $f_{t,final}$, and since the proposed OTAs' step responses are following a single-time constant behavior, one can find the time constant (τ) at 67% of the step-response final value and evaluate $f_{t,final}$ using the following expression:

$$f_{t,final} = \frac{1}{2\pi\tau} \quad . \tag{6.3}$$

Accordingly, Fig. 6.7 shows the DC gain of the proposed OTA, and a summary of the open-loop measurements' results is shown in Table 6.6, for the proposed 2-, 3-, and 4-stage CMOS OTAs under $C_{L,min}$ and $C_{L,max}$ for each OTA. Clearly the results in Fig. 6.7 validates the results in Fig. 4.6.

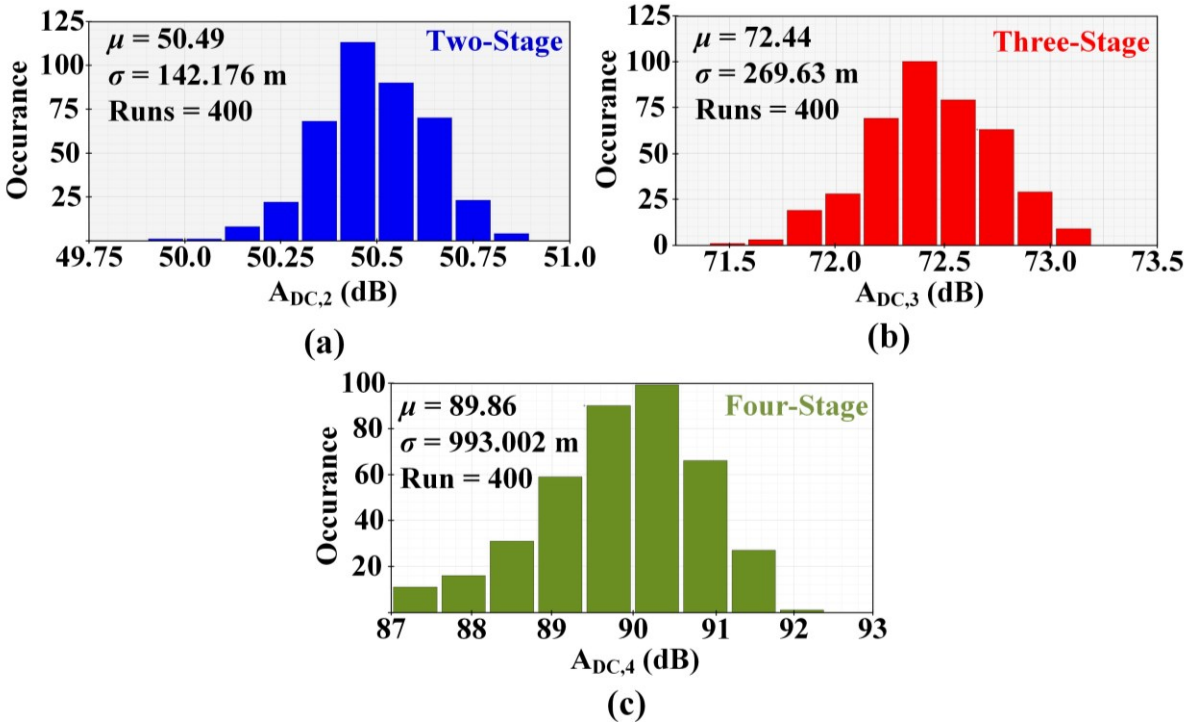

Fig. 6.8: The schematic-based Monte-Carlo simulations of A_{DC} for proposed scalable OTA: (a) the 2-stage OTA, (b) the 3-stage OTA, and (c) the 4-stage OTA.

6.5. Robustness Tests

To ensure the robustness of the proposed design, excessive process corners and Monte-Carlo (MC) simulations have been conducted for different OTAs' parameters, under different C_L's, in open-loop and closed-loop configurations. This was conducted for both schematic-based and post-layout-based designs. Fig. 6.8 shows a test for the design robustness using the schematic-based open-loop A_{DC} MC simulations for the 2-, 3-, and 4-stage CMOS OTAs. Here, a relative percent error of less than 1.5% is obtained. The same can be said for all other performance metrics.

Moreover, to test the proposed OTAs robustness under PVT variations, the post layout-based process corners of the proposed 2-, 3-, and 4-stage OTAs under C_L of 1 pF and 1 nF are

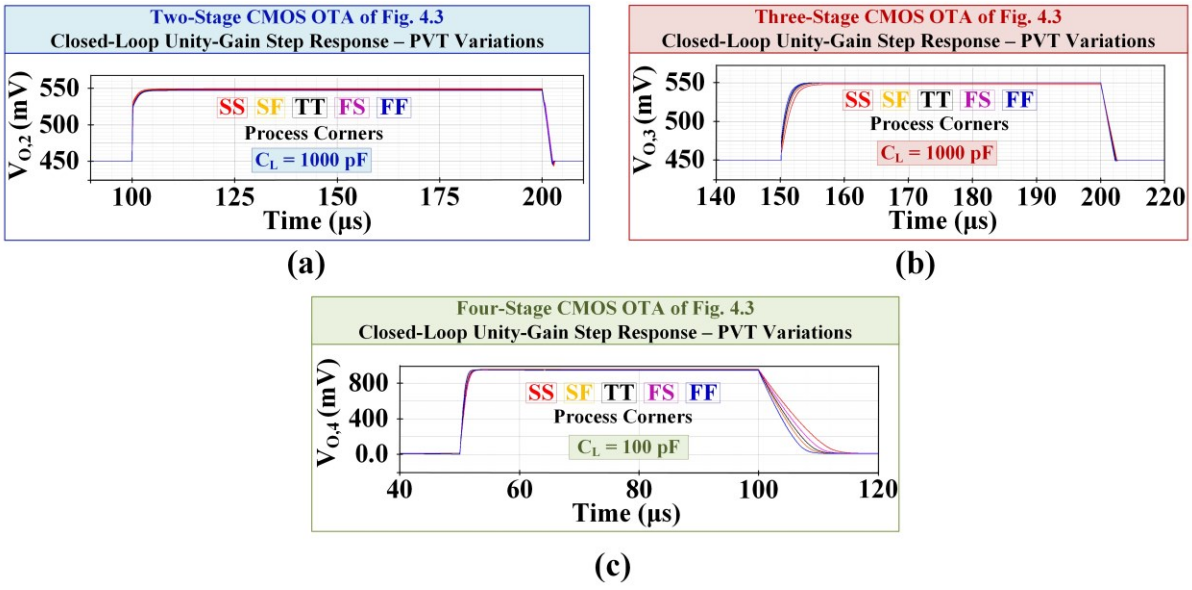

Fig. 6.9: The closed-loop unity-gain step response subject to a large-signal step input under process corners: (a) the 2-stage OTA with C_L = 1 nF, (b) the 3-stage OTA with C_L = 1 nF, and (c) the 4-stage OTA with C_L = 100 pF.

TABLE 6.7

ROBUSTNESS TESTS USING POST-LAYOUT SIMULATION-BASED PROCESS CORNERS, AT T = 25°C, FOR DIFFERENT PERFORMANCE PARAMETERS FOR THE PROPOSED TWO-, THREE-, AND FOUR-STAGE CMOS OTAS OF FIG. 4.3 UNDER (C_L = 1 PF).

	Corners	A_{DC} (dB)	*Power* (µW) @ V_{DD} = 1 V	$\omega_{t,final}$ (MHz)	*PM* (°)	*Avg. T_S* @ 1% (ns)	*Avg. SR* (V/µs)	*In-Referred Noise* (nV/$\sqrt{\text{Hz}}$) @ 10 kHz
TWO-STAGE	**SS**	51.58	98.2 @ 1V	143.2	54.1	0.056	22.15	84.8
	SF	51.26	101.2 @ 1V	151.3	54	0.042	16.2	82
	TT	**51.18**	**106** @ 1V	**157.7**	**53.8**	**0.025**	**18.07**	**82.2**
	FS	50.89	110.6 @ 1V	163	54.2	0.015	18.97	82.2
	FF	50.76	113.4 @ 1V	175	55	0.018	28.3	78.9
THREE-STAGE	**SS**	76.8	172.4 @ 1V	218	50	0.017	19.8	117.5
	SF	75.7	179.8 @ 1V	235	53.5	0.02	6.3	113.4
	TT	**77.2**	**180.1** @ 1V	**242.8**	**53.1**	**0.009**	**29.55**	**109.6**
	FS	75.6	193.8 @ 1V	248	53.1	0.015	6.25	106.2
	FF	74.6	201.9@ 1V	261	54.3	0.013	8.1	106.5
FOUR-STAGE	**SS**	93.2	262.1 @ 1V	63.9	63	0.046	59.1	1589
	SF	91.5	307.8 @ 1V	69.4	67	0.024	51.1	1518.7
	TT	**92**	**243.5** @ 1V	**73.5**	**66.7**	**0.077**	**23.88**	**1849.1**
	FS	91.9	292.9 @ 1V	78	66	0.032	43.9	2119.5
	FF	88.3	328.2 @ 1V	85.4	67	0.033	28.7	1794.2

conducted. Table 6.7 reports the results of different performance metrics' behavior under these process corners for C_L = 1 pF, while Fig. 6.9 shows the closed-loop step response under process corners for C_L = 1 nF. As can be seen in Table 6.7 and Fig. 6.9, all process corners, for all metrics, indicates no unforeseen sensitivity issues. Consequently, using the results shown in Fig. 6.8, Table 6.7, and Fig. 6.9, one can conclude that the proposed OTA designs are robust under PVT variations.

6.6. Comparison

To clearly highlight the achieved advancements of this work, the proposed 2-, 3-, and 4-stage OTA designs have been compared with 20 previously reported different OTA designs. Measurement-based works, where CMOS OTAs can drive a wide range of C_Ls (i.e., not only a single C_L driving capability), have been reported in Table 6.8, except for [21] and [25], where simulation-based works have been reported. This comparison has been done regardless of the stages' number, however, for clarity purposes, these works are organized in Table 6.8 based on the number of stages.

Referring back to Fig. 1.2 in Chapter 1, where the settling time requirements vs. C_L for different applications are shown, one can appreciate the need for an OTA with a wide-ranging drivability features, even if the OTA settles in seconds. Fig. 6.10 superimposes a load-drivability summary of the OTA results of this work with the best results found in the literature [99, 25, 92 and 42], as it compares with the applications reported in Fig. 1.2. As is clearly evident*, the proposed OTAs cover more applications than any other reported work.*Also, Fig. 6.10 verifies the results found in Fig. 4.8.

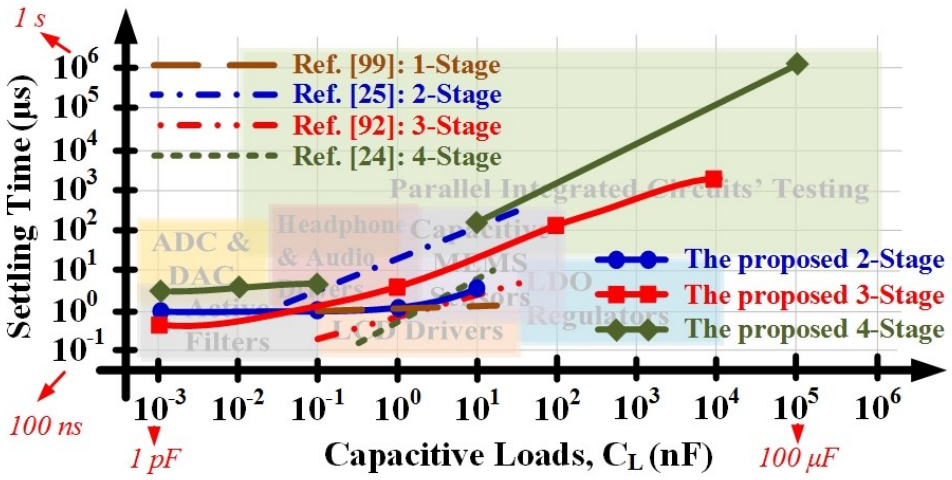

Fig. 6.10: Comparing the proposed OTA designs with the previously reported works in terms of C_L-drivability from the applications' perspective.

In addition to the simplicity of the proposed design which uses conventional gain stages with multi-Miller R-C compensation circuits across gain stages, the proposed FCT is applicable to 2-, 3-, and 4-stage OTAs. This is a feature that is not available in any of the previously published works. This offers wider design choices for DC gain and power consumption for different applications.

To set the comparison in a conventional way, the following well-established figures of merit (FOMs) have been used [92]:

$$FOM_S = \frac{\text{GBW} \,.\, C_L}{\text{Power} \,.\, \text{Area}} \times C_{L-drivability} \tag{6.4}$$

$$SIFOM_L = \frac{\text{GBW} \,.\, C_L}{\text{Power} \,.\, \text{Area}} \times \frac{C_{L-drivability}}{T_S} \tag{6.5}$$

Table 6.8 shows that the proposed OTAs outperform all other reported works in FOM_S, where the highest values is reported for the proposed 3-stage OTA, followed by the proposed 4-

stage OTA and then comes the proposed 2-stage OTA. Also, the proposed OTAs outperform all other reported works in $SIFOM_L$, where the highest values is reported for the proposed 4-stage OTA (at C_L = 100 pF), followed by the proposed 3-stage OTA and then comes the proposed 2-stage OTA. However, the proposed 4-stage OTA has a low $SIFOM_L$ at $C_{L,max}$ = 100 µF due to the long settling time of such large C_L. Also, looking at the OTAs' metrics individually, one can see that the proposed 4-stage OTA has the highest $C_{L,max}$ of 100 µF. Moreover, the proposed 4- and 3-stage OTA have the maximum C_L drivability of 1,000,000x, followed by the proposed 2-stage OTA with a C_L-drivability of 10,000x. Finally, apart from the single-ended single-stage OTA in [98], the proposed differential-ended 2-stage OTA occupies the smallest silicon area of 0.0021 mm^2.

6.7. Summary

This chapter has verified and validated the proposed scalable many-stage CMOS OTAs with an ultra-wide C_L-drivability range of Chapter 4 through a design example of a 2- to 4-stage CMOS OTAs. The standard 65 nm TSMC CMOS process was used to fabricate the proposed OTA. Since the main contribution of Chapter 4 has been captured in Fig. 4.6, Fig. 4.7, and Fig. 4.8, this chapter has reproduced these figures through simulations (schematic and post-layout) and extensive measurement results. **Consequently:**

1- **Fig. 4.6 has been verified in Fig. 6.7,**

2- **Fig. 4.7 has been verified in Fig. 6.2, and**

3- **Fig. 4.8 has been verified in Fig. 6.3 and Fig. 6.10.**

TABLE 6.8
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART WORKS THAT DRIVE A WIDE RANGE OF C_LS

# of Stages	Ref.	Circuit/ Compensa. Topology	CMOS process (nm)	DC gain (dB)	Power (µW) @V_{DD}(v)	Chip Area (mm^2)	C_L (nF)	C_L-drivability	GBW (MHz)	T_S @1% (µs)	FOM_S	SI-FOM_L
Single-Stage	[97] '14 TCAS-I	Current Booster	180	>100	36.5 @ 1.8	0.007	4.4	4.3x	1.08	2.5	79.64	31.68
							19		0.289		91.2	11.4
	[98] '15 JSSC	Nested-Cur. Mirror	180	72	**3.6 @ 1.2**	**0.0013**	0.15	100x	0.283	20.8	907	43.6
							15		0.0027	2149	865.3	0.39
	[91] '15 JSSC	Signal-Cur. Enhancer	130	100	16.8 @ 0.7	0.0027	10	3x	1.99	0.974	1316	1351
							30		0.77	2.61	1527	585
	[99] '16 TCAS-I	Pseudo amplifier	180	100	7.4 @ 1.1	0.0021	0.1	150x	1.66	1.2	1602.3	1335.2
							15		0.01	2.4	1447.5	603
Two-Stage	[25]*'11 CAS Mag.	Capacitor Multiplier	350	82	56.7 @ 1.5	-	0.05	1000x	1.15	1.1	1.01**	0.92**
							50		0.02	621	17.5**	284x10^{-4}
	[44] '15 TCAS-II	Capacitor Multiplier	180	82	32.4 @ 1.2	0.0045	0.02	750x	3.06	0.36	314.8	874.4
							15		0.22	11	16,974	1,542
	[45] '16 TVLSI	12Cross-Co. gain stages	130	100	14 @ 0.7	0.0056	9.5	2x	1.17	1	283.48	283.48
							18.9		0.856	1.9	412.5	215.4
	This Work	Multi-Miller R-C	65	~50	126.8 @ 1	**0.0021**	0.001	10,000x	6.17	1.28	231.7	181
							10		0.06	5.65	22,532	3,988
Three-Stage	[86] '11 JSSC	Dual Acti. C-FB	350	>100	260 @ 2	0.014	0.5	1.6x	4	0.6	0.87	1.45
							0.8		3.6	0.7	1.26	1.8
	[88] '13 JSSC	Current Buff Miller	350	>100	144 @ 2	0.016	1	15x	1.37	1.28	8.9	6.9
							15		0.95	4.49	92.7	19.5
	[100] '16 TCAS-I	Single Miller Capacitor	350	136*	49.8 @ 2	0.003	5	3x	2.85	0.63	286	454
							15		2.8	0.93	843	906
	[90] '18 TCAS-II	Single Miller Capacitor	350	113	8.9 @ 1.4	0.0025	10	10x	1.7	2	7640	3820
							100		0.43	7.7	19320	2500
	[91] '15 JSSC	Current Enhancer	130	~100	16.8 @ 0.7	0.0027	10	3x	1.99	0.97	1316	1356
							30		0.77	2.61	1527	585
	[92] '20 TCAS-I	Cap. Free	130	~72	185 @ 1 95 @ 1	0.006	0.09	555.5x	4.23	0.2	194.5	972.8
							50		0.46	4.62	22,410	4850
	[89] '15 JSSC	Cascode Miller	130	>100	12.7 @ 1.2	0.0032 0.0054	0.33	45.4x	4.21	0.7	1552	2217.1
							15		0.84	19	8340	438.9
	[101] '17 JSSC	Acti. Zero Miller	180	>100	69.6 @ 1.2	0.013	1.5	12x	3.46	0.57	68.7	120.7
							18		1.18	4.1	280.8	68.4
	[87] '11 JSSC	Damping Factor Ctrl	800	>100	420 @ 2	0.11 0.14	0.1	10x	2.6	1.16	0.0562	0.0485
							1		1.0	3.54	0.17	0.048
	This Work	Multi-Miller R-C	65	~70	227.9 @ 1	0.0084	0.001	**1,000,000x**	7.75	0.81	4048.3	4997.9
							10000		0.0011	2650	**5,746,045**	2100
Four-Stage	[21]*'14 IJCTA	2FF/ Miller C & R-C	90	92.1	54.9 @ 0.9	-	0.5	2x	18	0.541	0.16**	0.59**
							1		15.1	0.65	0.27**	0.83**
	[24] '20 TVLSI	Active ParallelAmp.	130	107	175.2 @ 1.2	0.007	0.4	30x	2.75	0.33	67.2	203.8
							12		1.18	9.75	28.8	2.96
	This Work	Multi-Miller R-C	65	~ 90	353.1 @ 1	0.013	0.001	**1,000,000x**	0.47	4.16	102.3	24.5
							0.1		1	4.23	21,785	**5150.1**
							10		0.018	189.3	39,213	207.1
							100,000		0.000002	1.5x10^6	43,570	0.025

* Simulation-based. ** FOM calculations have been done without (Area).

CHAPTER 7

CONCLUSION

A new generalized relationship between frequency response and settling time was presented in this thesis addressing the impact of *P-Z* pairs/doublets on CMOS OTAs. The proposed theory showed that using low frequency zeros and cascaded-gain stages reduces the impact of *P-Z* pairs on the settling time of CMOS OTAs. Interestingly, it was shown that increasing the number of gain-stages reduces the impact of *P-Z* pairs, while having such *P-Z* pairs helps stabilize the OTA. By exploiting this new theory, this thesis has introduced a many-stage CMOS OTA design technique that allows cascading identical gain stages (for arbitrarily scalable high DC gain) while driving an ultra-wide range of capacitive loads (C_Ls). At the heart of the proposed design is a new frequency compensation technique that relies on low-frequency left-half-plane zeros to allow the proposed OTA to operate for a desired closed-loop behavior. This chapter summarizes the findings presented throughout this thesis and recommends a number of future work suggestions by briefly discussing a number of potential opportunities and advantages that the proposed CMOS OTAs may offer in the future, which could potentially advance the future analog and mixed-signal applications.

7.1. Summary of Findings

To easily summarize the findings in this thesis, one can refer back to the research objectives of ***Chapter 1*** (i.e., Section 1.3) and present these findings accordingly. Since the central research question was: "*Ideally, can we cascade infinite gain-stages to design CMOS OTAs with infinite DC gain?"*, a follow up research question regarding the availability of *an FCT that can ensure stability of CMOS OTAs' in closed-loop operation regardless of the number of gain stages* was raised. Accordingly, two other research questions were set as follows:

1- *Is there an arrangement of the OTA's poles and zeros that will prevent the OTA closed-loop response from entering the instability region regardless of the number of gain stages?*
2- *What is the impact of such an arrangement on the speed and C_L-drivability of CMOS OTAs?*

Based on these questions, this thesis started by investigating the available arrangements of poles and zeros in ***Chapter 2***, and the following was found:

- Despite being ignored in the literature and considered detrimental to the settling time of CMOS OTAs, the *P-Z* pair (or doublet) arrangement is a potential candidate to be revisited as the early observations indicated that the available analyses regarding the presence of *P-Z* pairs (or doublets) are associated with some limitations. Interestingly, the available analyses on the impact of *P-Z* pair on the settling time of CMOS OTAs were restricted to the case of having a single open-loop P-Z pair only, making them most

relevant for 2-stage OTAs, (2) the analyses were based on CMOS technologies that range from line widths greater than 1 micron [16] down to only 0.35 μm [19], without considering more advanced nano-meter scale technology nodes, (3) cascading gain-stages was not a design goal in these works, especially that such older technology nodes allowed supply voltages greater than 3 V, relaxing the need for a multi-stage design.

Therefore, ***Chapter 3*** took the initiative to elaborate more on these limitations of the well-established analysis on the relationship between frequency response and settling time of CMOS OTAs having one *P-Z* pair (or doublet). Accordingly, a new generalized relationship between frequency response and settling time of CMOS OTAs was introduced, and the following were found:

- For the case of having one *P-Z* pair, it was shown that the low-frequency zero gain (A_Z) has a critical role in reducing the impact of *P-Z* doublets on the closed-loop response of OTAs.
- By expanding the analysis having *N*-1 *P-Z* pairs, it was shown that through the appropriate selection of the A_Z parameter in the OTA open-loop response, the zeros of the compensator can be placed at low frequency to enhance the performance attributes of the closed-loop system provided that the open-loop DC gain is high enough for the given application.

Based on these findings, ***Chapter 4*** introduced a many-stage CMOS OTA design technique that allowed cascading identical gain stages (for arbitrarily scalable high DC gain) while driving an ultra-wide range of capacitive loads. At the heart of the proposed design is a new frequency

compensation technique that relies on low-frequency left-half-plane zeros to allow the proposed OTA to operate for a desired closed-loop behavior. Stability of the many-stage OTA was ensured by re-positioning the poles and zeros of all gain stages in a systematic scalable pattern whenever a new gain-stage is added.

In addition to achieving an ultra-high DC gain, the ability to cascade many gain stages (as presented in ***Chapter 4***) provide the following advantages:

1. In the case of single stage amplifier with low gain, (e.g., A_{DC} = 10 dB), numerous stages can be used to achieve an overall DC gain that is useful (i.e., 7-stages can be cascaded to achieve a DC gain of about 60 dB to 70 dB). This would be the case for ultra-small size CMOS technology nodes (i.e., less than 10 nm technologies).
2. In the case of single stage amplifiers with a DC gain of around 20 dB, numerous gain stages can be used to achieve an overall DC gain that exceeds 100 dB. This will result in improving the CMRR, PSRR, offset, etc. over and above a 2- or 3-stage amplifier. For instance, Texas Instruments (TI) sells OPA 277 high-precision OPAMP that has a DC gain of 134 dB together with CMRR of 140 dB and PSRR of 130 dB. According to their data sheet, these ultra-high gain amplifiers are being marketed for use in Transducer amplifier, precision integrators, battery power instruments, etc.

Based on these findings of ***Chapter 3*** *and* ***Chapter 4****, the previously-mentioned research questions and objectives were answered. However, verifications and validations were required to solidify these findings; therefore,* ***Chapter 5*** *and* ***Chapter 6*** *were introduced for this purpose.*

In ***Chapters 5 and 6***, classical gain-stages (i.e., differential pair and common source transistors) were used to design fully-differential 2-, 3-, 4-, 5-, 6-, 7-, and 8-stage CMOS OTAs. The presented design realizes a CMOS OTA with scalable-gain that increases in 25 dB increments per stage, achieving a total gain from 50 dB to 200 dB for a 2-stage to an 8-stage configuration, respectively. Furthermore, the proposed FCT used a multi-Miller R-C compensation circuit across the gain stages to position the *P-Z* Pair created by the R-C compensation networks below ω_t of the compensated OTAs whenever a new gain stage is added. The presented design is verified through extensive simulations based on a TSMC 65 nm CMOS process. Also, as a proof-of-concept, the design has been validated by fabricating 2-, 3-, and 4-stage CMOS OTAs in the standard TSMC 65 nm CMOS process, and the measurement results show that the 2-stage OTA is achieving a DC gain of 50 dB with a C_L-drivability ratio of 10,000×, the 3-stage OTA is achieving a DC gain of 70 dB with a C_L-drivability of 1,000,000x, and the 4-stage OTA is achieving a DC gain of 90 dB with a C_L-drivability of 1,000,000x. This is a 10-to-1000-time improvement in the state-of-the-art.

7.2. Future Directions

As this thesis pushes the boundaries on the maximum number of gain-stages that one can cascade in pursuit to design ultra-high DC gain CMOS OTAs with a wide C_L-drivability range, many recommendations can be made to further expand this work in future. These recommendations are presented in point-form for each individual chapter.

Chapter 2:

This chapter presented the previously reported works on the design of CMOS OTAs based on their number of stages and the FCTs they have used. The purpose of this type of presentation was to highlight the different possible arrangements of *P-Z* pairs. However, one can also expand this chapter by:

- Presenting the previously reported works from different perspectives as mentioned at the beginning of ***Chapter 2***. This will open doors to set clear parameters for comparison purposes and show the trade-offs between all these works across different perspectives; hence, offering a design guidance for the design engineers in the industry as well as the universities teaching graduate level advanced electronics.

Chapter 3:

This chapter introduced a mathematical-based relationship between frequency response and settling time of CMSO OTAs. This chapter can be expanded by

- Giving the physical explanation on how the current is flowing in the compensation circuit to clearly define the actual impact of *P-Z* pairs on the step response of CMOS OTAs. Accordingly, a possible circuit technique might be developed to prevent the impact of *P-Z* pairs.

Chapter 4:

This chapter introduced the design of a scalable many-stage CMOS OTA with an ultra-wide range of C_Ls using classical differential pair followed by common-source transistors (to design

the gain stages) and Miller R-C circuits (to design the compensation network). Consequently, this chapter can be expanded in future by:

- Using a different circuit topology to design the gain-stages, such as: the inverter-based gain cells, the fully balanced linear amplifiers, digital-based OTAs, etc.
- Using a different compensation circuit to position the poles and zeros according to the proposed FCT.
- Optimizing the FCT by deriving exact equations to position the poles and zeros instead of the intuitive proposed technique.
- Optimizing the OTAs for power, area, noise, etc.
- Using the proposed OTA in a real-world application and making use of the scalable DC gain feature. For example, programmable analog-to-digital converters can benefit from the scalability feature to design an ADC with a set of different resolutions. Also, the capability to drive a wide range of C_Ls makes the proposed OTA suitable for a wide range of analog applications as reported in Fig. 1.2.
- Automating the OTA design, as one of the interesting features in the proposed OTAs is the use of identical gain-stages. In other words, if one can design a gain cell with a specific DC gain, and include it to the analog library, the analog designers can replicate (i.e., cascade) this gain cell to achieve the required overall DC gain without the need to design a new OTA whenever a new value of A_{DC} is required. This is also applicable to the Miller R-C compensation circuit, where the proposed FCT depends on replicating the R-C compensation circuit to reposition the poles and zeros whenever a new stage is added.

Chapters 5 and 6:

These chapters introduced the verification and validation of the proposed theory in ***Chapter 3*** and the proposed OTA design ***in Chapter 4***. These chapters (i.e., 5 and 6) can be expanded by:

- Fabricating more ICs for a higher number of stages.
- Using different technology nodes to build the proposed OTAs.

REFERENCES

[1] P. R. Gray and R. G. Meyer, “MOS operational amplifier design—A tutorial overview,” IEEE J. Solid-State Circuits, vol. SSC-13, no. 3, pp. 285–294, 1978.

[2] M. A. Mohammed, S. Kawar, and K. Abugharbieh, “Methodology for designing and verifying switched-capacitor sample and hold circuits used in data converters”, *IET Circuits, Devices and Systems*, vol. (8), no. (4), pp. 252 – 262, July, 2014.

[3] Analog Devices, “32-Bit Oversampling ADC with Configurable Digital Filter,” LTC2508-32 datasheet, 2016.

[4] A. Sedra, and K. Smith, ‘Microelectronic Circuits’. 7th ed., New York: Oxford University Press, 2015, pp.871-883, and 996-1006.

[5] B. Razavi: ‘Design of Analog CMOS Integrated Circuits’, (McGraw-Hill Publisher, New York, 2001), p.p. 345-348, 314-324.

[6] N. Aghaee, Z. Peng, and P. Eles, “Temperature-Gradient-Based Burn-In and Test Scheduling for 3-D Stacked ICs,” *IEEE Trans. on VLSI*, vol. 23, no. 12, pp. 2992-3005, December 2015.

[7] A. S. Emara, D. Romanov, G. W. Roberts, S. Aouini, S. Ziabakhsh, M. Parvizi, and N. Ben-Hamida, “An Area-Efficient High-Resolution Segmented ΣΔ-DAC for Built-In Self-Test Applications” *IEEE Trans. on VLSI,* vol. 29, no. 11, pp. 1861-1874, August 2021.

[8] Active Filters for Video, reference design 3172, Maxim Integrated, San Jose, CA USA, July 2004.

[9] V. Dhanasekaran, J. Silva-Martinez, and E. Sanchez-Sinencio, “Design of three-stage class-AB 16 Ω headphone driver capable of handling wide range of load capacitance,” *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1734–1744, June 2009.

[10] F. Xiao, P.K. Chan, “A Performance-Aware Low-Quiescent Headphone Amplifier in 65 nm CMOS” *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 505–516, February 2017.

[11] C. Mohan and P. M. Furth, “A 16-Ω_audio amplifier with 93.8-mW peak load power and 1.43-mW quiescent power consumption,” *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 59, no. 3, pp. 133–137, Mar. 2012.

[12] W.-J Huang, S. Nagayasu, and S.I-. Liu, “A rail-to-rail class-B buffer with DC level-shifting current mirror and distributed Miller compensation for LCD column drivers” *IEEE Trans.on Circuits Syst. I, Reg. Papers,* vol. 58, no. 8, pp. 1761–1772, August, 2011.

[13] B. Li, W. Wang, J. Liu, W.-J. Liu, Q. Yang, and W.-B. Ye, " A 1 pF-to-10 nF Generic Capacitance-to-Digital Converter Using Zero-Crossing Δ-Σ Modulation", *IEEE Trans.on Circuits Syst. I, Reg. Papers*, vol. 65, no.7, pp. 2169-2182, July 2018.

[14] C. Stagni *et al.*, “CMOS DNA sensor array with integrated A/D conversion based on label-free capacitance measurement,” *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2956–2964, December. 2006.

[15] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003. M. A.

[16] A. Fahim, "Low-leakage current, low-area voltage regulator for system-on-a-chip processors," *Electron. Lett.*, vol. 41, no. 19, pp. 1054–1055, Sep. 2005.

[17] W. Oh and B. Bakkaloglu "A CMOS Low-Dropout RegulatorWith Current-Mode Feedback Buffer Amplifier" *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, no. 10, pp. 922–926, October 2007.

[18] M. Yang and G. W. Roberts, "Synthesis of High Gain Operational Transconductance Amplifiers for Closed-Loop Operation Using a Generalized Controller-Based Compensation Method" *IEEE Trans. On Circui. and Sys.–I*, vol. 63, no. 11, November 2016, pp. 1794 – 1806.

[19] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested G_M-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.

[20] W. Yan, R. Kolm, and H. Zimmermann, "Efficient four-stage frequency compensation for low-voltage amplifiers," *in Proc. IEEE Int. Symp. Circuits Syst.,* May 2008, pp. 2278–2281.

[21] M. Mojarad and M. Yavari, "A low-power four-stage amplifier for driving large capacitive loads," *Int. J. Circuit Theory Appl*., vol. 42, no. 9, pp. 978–988, Sep. 2014.

[22] A. D. Grasso, G. Palumbo, S. Pennisi, and G. Di Cataldo, “High performance frequency compensation topology for four-stage OTAs,” *in Proc. 21st IEEE Int. Conf. Electron., Circuits Syst. (ICECS),* Dec. 2014, pp. 211–214.

[23] A. D. Grasso, G. Palumbo, and S. Pennisi, “High-performance four-stage CMOS OTA suitable for large capacitive loads,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2476–2484, Oct. 2015.

[24] S. A. Fordjour, J. Riad, and E. Sánchez-Sinencio, “A 175.2-mW 4-Stage OTA With Wide Load Range (400 pF–12 nF) Using Active Parallel Compensation,” *IEEE Trans. on VLSI*, vol. 28, no. 7, pp. 1621-1629, July 2020.

[25] Z. Yan, P. Mak and R. P. Martins, "Two Stage Operational Amplifiers: Power and Area Efficient Frequency Compensation for Driving a Wide Range of Capacitive Load," in *IEEE Circuits and Systems Magazine*, vol. 11, no. 1, pp. 26-42, First Quarter 2011.

[26] B. Nauta, “A CMOS Transconductance-C Filter Technique for Very High Frequencies” *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142-153, Feb. 1992.

[27] F. Krummenacher and N. Joehl, “A 4-MHz CMOS continuous-time filter with on-chip automatic tuning,” *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 750–758, Jun. 1988.

[28] P. Toledo, P. Crovetti, H. Klimach, S. Bampi, O. Aiello, and M. Alioto, “A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier” *IEEE Trans. Circuits Syst. II, Exp. Briefs,*vol. 68, no. 9, pp. 3073-3077, September 2021.

[29] R.G. Eschauzier and J. H. Huijsing, “Frequency Compensation Techniques for Low-Power Operational Amplifiers” 1st edition, Springer Science and Business Media, 1995.

[30] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-Frequency Compensation," *IEEE Trans. Circuits Syst. I*, vol. 48, no. 9, pp. 1041–1056, Sep. 2001.

[31] A.D. Grasso, G. Palumbo and S. Pennisi, "Comparison of the Frequency Compensation Techniques for CMOS Two-Stage Miller OTAs" *IEEE Trans. on Circuits and Systems-II*, vol. 55, no. 11, pp. 1099-1103, November 2008.

[32] J. E. Solomon and G. R, Wilson "A Highly Desensitized, Wide-Band Monolithic Amplifier" *IEEE Journal of Solid State circuits*, vol. sc-1, no.1, pp. 19-28. Septemper 1966.

[33] D. Senderowicz, D. Hodges and P. Gray, "High-performance NMOS Operational Amplifier," *IEEE Journal of Solid-state Circuits*, vol. sc-13, no.6, pp. 760-766, December 1978.

[34] W. C. Black, Jr., D. J. Allstot and R. A. Reed, "A High Performance Low Power CMOS Channel Filter" *IEEE Journal of Solid-state Circuits*, vol. sc-15, no.6, pp. 929-938, December 1980.

[35] Y. P. Burns, "Nonuniform pulse code modulation encoding using integrated circuit techniques", PhD dissertation, University of California Berkely, 1976.

[36] Y. Tsividis and P. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation," *IEEE Journal of Solid-Stare Circuits*, vol. sc-11, no. 6, pp. 748-753, December 1976.

[37] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers*," IEEE Journal Solid-State Circuits*, vol. SC-18, no. 6, pp. 629–633, Dec. 1983.

[38] G. Palmisano and G. Palumbo, “A Compensation Strategy for Two-Stage CMOS Opamps Based on Current Buffer” *IEEE Journal Solide-Stage Circuit,* vol. 44, no. 3, pp. 257-262, March 1997.

[39] J. Mahattanakul, “Design Procedure for Two-Stage CMOS Operational Amplifier Employing Current Buffer” *IEEE Trans. on Circuits and Systems-II*, vol. 52, no. 11, pp. 766-770, November 2005.

[40] R. G.H. Eschauzier and J. H. Huijsing, “An Operational Amplifier with multipath Miller Zero Cancellation for RHP Zero Removal” *in Proc. IEEE Nineteenth European Solid-State Circuits Conference*, Sep. 1993, pp. 122-125.

[41] M. Vadipour, “Capacitive Feedback Technique for Wide-Band Amplifiers”, *IEEE Journal Solid-State Circuits*, vol. 28, no. 1, pp. 90 - 92, January 1993.

[42] P. J. Hurst, S. H. Lewis, J. P. Keane, F. Aram, and K. C. Dyer, “Miller Compensation Using Current Buffers in Fully Differential CMOS Two-Stage Operational Amplifiers” *IEEE Trans. Circuits Syst. I*, vol. 51, no. 2, pp. 275–285, Feb. 2004.

[43] J. Ramírez-Angulo, R. G. Carvajal, J. A. Galán, and A. López-Martín, “A Free But Efficient Low-Voltage Class-AB Two-Stage Operational Amplifier” *IEEE Trans. on Circuits and Systems-II*, vol. 53, no. 7, pp. 568-571, July 2006.

[44] Z. Yan, P. Mak and R. P. Martins, “A 0.0045-mm^2 32.4-µW Two-Stage Amplifier for pF-to-nF Load Using CM Frequency Compensation” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 62, no. 3, pp. 246–250, March 2015.

[45] M. Ho, J. P. Guo, T. W. Mui, K. H. Mak, W. L. Goh, H. C. Poon, S. Bu, M. W. Lau and K. N. Leung, "A two-stage large-capacitive-load amplifier with multiple cross-coupled

small-gain stages", *IEEE Transactions on VLSI Systems*, vol. 24, no.7, pp. 2580-2592, July 2016.

[46] Y. Xin, X. Zhao, B. Wen, L. Dong, and X. Lv, "A High Current Efficiency Two-Stage Amplifier With Inner Feedforward Path Compensation Technique", *IEEE Access*, vol. 8, pp. 22664 – 22671, Feb. 2020.

[47] Y. Kwon, T. Kim, N. Sun, and Y. Chae, "A 348-µW 68.8-dB SNDR 20-MS/s Pipelined SAR ADC With a Closed-Loop Two-Stage Dynamic Amplifier" *IEEE Solid-State Circuits Letters*, vol. 4, pp. 166 - 169, Sep. 2021.

[48] F. Centurelli, R. Luzzi, M. Olivieri and A. Trifiletti "A Bootstrap Technique for Wideband Amplifiers" *IEEE Trans. on Circuits and Systems-I*, vol. 49, no. 10, pp.1474-1480, October 2002.

[49] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos and Y. Papananos, "A Lowe-Power Wideband Reconfigurable Integrated Active-RC Filter With 73 dB SFDR", *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 1997 - 2008, September 2006.

[50] M. S. Ghausit and D. Pedersons, "A New Design Approach for Feedback Amplifiers" *IRE Transaction on Circuit Theory*,vol. 8, no. 3, pp. 274 – 284, September 1961.

[51] M. Abdulaziz, M. Törmänen and H. Sjöland, "A Compensation Technique for Two-Stage Differential OTAs," *IEEE Trans. on Circuits and Systems -II: Express Briefs*, vol.61, no.8, pp.594-598, Aug. 2014.

[52] H. Ng, R. M. Ziazadeh and D. J. Allstot, "A Multistage Amplifier Technique with Embedded Frequency Compensation", *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 339 - 347, Mar. 1999.

[53] J. Mahattanakul and J. Chutichatuporn, “Design Procedure for Two-stage CMOS Opamp With Flexible Noise-Power Balancing Scheme” *IEEE Trans. on Circuits and Systems*, vol. 52, no. 8, pp. 1508-1514, August 2005.

[54] T. J. Van Kessel, “An Integrated Operational Amplifier with Novel HF Behaviour”, *IEEE J. Solid-State Circuits*, vol. SC-3, no. 4, pp. 348 - 352, Dec. 1968.

[55] P.K. Chan and Y. C. Chen, “Gain-Enhanced Feedforward Path Compensation Technique for Pole-Zero Cancellation at Heavy Capacitive Loads” *IEEE Trans. on Circuits and Systems -II: Express Briefs*, vol.50, no.12, pp.933-941, December 2003.

[56] W. Sansen and Z. Y. Chang, “Feed forward Compensation Techniques for High Frequency CMOS Amplifiers”, *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1590 - 1595, December 1990.

[57] B. Kumar Thandri and J. Silva-Martínez, “A Robust Feedforward Compensation Scheme for Multistage Operational Transconductance Amplifiers With No Miller Capacitors”, *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237 - 243, Feb. 2003.

[58] J. Beloso-Legarra, A.D. Grasso, A.J. Lopez-Martin, G. Palumbo, and S. Pennisi, “Two-Stage OTA with all Subthreshold MOSFETs and Optimum GBW to DC-Current Ratio” *IEEE Trans. on Circuits and Systems -II: Express Briefs*, early access, DOI 10.1109/TCSII.2022.3156401, 2022.

[59] F. D. Waldhauer, “Analog integrated circuits of large bandwidth”, *in 1963 IEEE Conv. Rec.*, Part 2, pp. 200-207.

[60] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship Between Frequency Response and Settling Time of Operational Amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, pp. 347–352, Dec. 1974.

[61] P. R. Gray and R. G. Meyer, "Recent Advances in Monolithic Operational Amplifier Design" *IEEE Tran. On Circuits and Systems*, vol. CAS-21, no. 3, pp. 317-327, May 1974.

[62] R. G. Eschauzier and Johan H. Huijsing, "Frequency Compensation Techniques for Low-power Operational Amplifiers" 1st ed., Dordrecht, Springer Science + Business Media, 1995, p.p. 153-157.

[63] G. Giustolisi and G. Palumbo, "In-Depth Analysis of Pole-Zero Compensations in CMOS Operational Transconductance Amplifiers" *IEEE Trans. On Circui. and Sys.–I*, vol. 66, no. 12, December 2019, pp. 4557 – 4570.

[64] R. J. Apfel and P. Gray, "A Fast-Settling Monolithiic Operational Amplifer Using Doublet Compression Technique", *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, pp. 332 - 340, Dec. 1974.

[65] G. Palmisano and G. Palumbo, "Analysis and Compensation of Two pole Amplifiers with a Pole-Zero Doublet," *IEEE Trans. Circuits Syst- I*, vol. 46, no. 7, pp. 864–868, Jul. 1999.

[66] A. Joshi, H. Shrimali and S. K. Sharma, "Systematic Design Approach for a Gain Boosted Telescopic OTA with Cross-Coupled Capacitor", *IET Circuit, Devices and Systems,* vol. 11, Iss. 3, pp. 225-231, April 2017.

[67] E. Ranjbar, M. Danaie, "Frequency Compensation of Three-Stage Operational Amplifiers: Sensitivity and Robustness Analysis" *Microelectronics Journal*, vol. 66, pp. 155–166, July 2017.

[68] S. Cannizzaro, G. Palumbo, and S. Pennisi "Distortion Analysis of Miller-Compensated Three-Stage Amplifiers" *IEEE Trans. Circuits Syst- I*, vol. 53, no. 5, pp. 961-976, May 2006.

[69] S. Cannizzaro, A. D. Grasso, R. Mita, G. Palumbo, and S. Pennisi "Design Procedures for Three-Stage CMOS OTAs with Nested-Miller Compensation" *IEEE Trans. Circuits Syst-I*, vol. 54, no. 5, pp. 933-940, May 2007.

[70] A. D. Grasso, R. Mita, G. Palumbo, and S. Pennisi "Analytical Comparison of Frequency Compensation Techniques in Three-Stage Amplifiers." *Int. Journal of Circuit Theory and Applications*, vol. 36, no.1, pp. 53-80, February 2008.

[71] D. Marano, G. Palumbo, and S. Pennisi. "Step-Response Optimization Techniques for Low-Power Three-Stage Operational Amplifiers for Large Capacitive Load Applications" *In Proc. of the 2009 IEEE International Symposium on Circuits and Systems (ISCAS 2009)*, Taipei, Taiwan, pp. 1949–1952, May 2009.

[72] A. Pugliese, F. Amoroso, G. Cappuccino, G. Cocorullo, "Settling Time Optimization for Three-Stage CMOS Amplifier Topologies" *IEEE Trans. Circuits Syst- I*, vol. 56, no. 12, pp. 2569–2582, December 2009.

[73] D. Marano, G. Palumbo, and S. Pennisi. "Step-Response Optimisation Techniques for Low-Power, High-Load, Three-Stage Operational Amplifiers Driving Large Capacitive Loads" *IET Circuits, Devices and Systems*, vol. (4), no. (2), pp. 87-98, March, 2010.

[74] R. Nguyen and B. Murmann, "The Design of Fast-Settling Three-Stage Amplifiers Using the Open-Loop Damping Factor As a Design Parameter" *IEEE Trans. Circuits Syst- I*, vol. 57, no. 6, pp. 244–1254, June 2010.

[75] S, Seth and B. Murmann, "Settling Time and Noise Optimization of a Three-Stage Operational Transconductance Amplifier" *IEEE Trans. Circuits Syst- I*, vol. 60, no. 5, pp. 1168–1174, May 2013.

[76] A. D. Grasso, G. Palumbo, S. Pennisi, and W. Sansen "The Noise Performance of CMOS Miller Operational Transconductance Amplifiers with Embedded Current-Buffer Frequency Compensation" *Int. Journal of Circuit Theory and Applications*, vol. 45, no.4, pp. 457-465, September 2016.

[77] J. Riad, J. J. Estrada-López, and E. Sánchez-Sinencio, "Classification and Design Space Exploration of Low-Power Three-Stage Operational Transconductance Amplifier Architectures for Wide Load Ranges" *Electronics*, vol. 8, no. 11, pp. 1268-1300, November 2019.

[78] Q. Cheng, W. Li, X. Tang, and J. Guo "Design and Analysis of Three-Stage Amplifier for Driving pF-to-nF Capacitive Load Based on Local Q-Factor Control and Cascode Miller Compensation Techniques" *Electronics*, vol. 8, no. 5, pp. 572-590, May 2019.

[79] J. Huijsing, D. Linebarger, "Low-Voltage Operational Amplifier with Rail-To-Rail Input and Output Ranges" *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1144–1150, Dec. 1985.

[80] K. N. Leung, and P. Mok, ”Nested Miller Compensation in Low-Power CMOS Design” *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 48, no. 4, pp. 388–394, April 2001.

[81] A. Grasso, G. Palumbo, and S. Pennisi, “Advances in Reversed Nested Miller Compensation” *IEEE Trans. Circuits Syst. I Regul. Pap*., vol. 54, no. 7, pp. 1459–1470, July 2007.

[82] D. Marano, G. Palumbo, S. Pennisi, “An Efficient RNM Compensation Topology with Voltage Buffer and Nulling Resistors for Large-Capacitive-Load Three-Stage OTAs” *In Proc. IEEE 16th International Conference on Electronics, Circuits and Systems—(ICECS 2009)*, Yasmine Hammamet, Tunisia, 13–16 December 2009.

[83] H. Lee, and P. Mok, “Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers” *IEEE J. Solid-State Circuits* vol. 38, no. 3, pp. 511–520, March 2003.

[84] X. Peng, and W. Sansen, “Transconductance with Capacitances Feedback Compensation for Multistage Amplifiers” *IEEE J. Solid-State Circuits*, vol. 40, no, 7, pp. 1514–1520, July 2005.

[85] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, “Three-stage large capacitive load amplifier with damping-factor-control frequency compensation,” *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb. 2000.

[86] S. Guo, H. Lee, “Dual Active-Capacitive-Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers” *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 452–464, February 2011.

[87] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, Feb. 2011.

[88] Z. Yan, P. I. Mak, M. K. Law, R. P. Martins, "A 0.016-mm^2 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load with >0.95-MHz GBW" *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 527–540, February 2013.

[89] M. Tan and W.-H. Ki, "A cascode Miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 440–449, Feb. 2015.

[90] A. D. Grasso, D. Marano, G. Palumbo, S. Pennisi, "High-Performance Three-Stage Single-Miller CMOS OTA with No Upper Limit of C_L" *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 11, pp. 1529–1533, November 2018.

[91] K. H. Mak, M.W. Lau, J. Guo, T.W. Mui, M. Ho, W. L. Goh, K. N. Leung, "A 0.7 V 24 μA Hybrid OTA Driving 15 nF Capacitive Load with 1.46 MHz GBW" *IEEE J. Solid-State Circuits,* vol. 50, no. 11, pp. 2750–2757, November 2015.

[92] J. Riad, J. J. Estrada-Lopez, I. Padill-Cantoya, and E. Sanchez-Sinencio, "Power-Scaling Output-Compensated Three-Stage OTAs for Wide Load Range Applications" *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 67, no. 7, pp. 2180-2192, July, 2020.

[93] R. G. H. Eschauzier, L. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath Nested Miller compensation structure," *Solid-State Circuits, IEEE J.*, vol. 27, no. 12, pp. 1709–1717, 1992.

[94] G. Palumbo, S. Pennisi, "Design Methodology and Advances in Nested-Miller Compensation". *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 49, no. 7, pp. 893–903, July, 2002.

[95] X. Peng, and W. Sansen,"Nested Feed-Forward G_m-Stage and Nulling Resistor Plus Nested-Miller Compensation for Multistage Amplifiers" *In Proc. IEEE 2002 Custom Integrated Circuits Conference*, Orlando, FL, USA, 15 May 2002, pp. 329–332.

[96] Biabanifard, S.; Hosseini, S.M.; Biabanifard, M.; Asadi, S.; Yagoub, M.C. Multi Stage OTA Design: From Matrix Description To Circuit Realization" *Microelectronics Journal*, vol. 77, pp. 49–65, May 2018.

[97] K. H. Mak and K. N. Leung, "A signal- and transient-current boosting amplifier for large capacitive load applications," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 10, pp. 2777–2785, Oct. 2014.

[98] Z. Yan, P. I. Mak, M. K. Law, R. Martins, and F. Maloberti, "Nested-current-mirror rail-to-rail-output single-stage amplifier with the enhancements of dc gain, GBW and slew rate," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2353–2366, Oct. 2015.

[99] S. W. Hong G. H. Cho, "A Pseudo Single-Stage Amplifier with an Adaptively Varied Medium Impedance Node for Ultra-High Slew Rate and Wide-Range Capacitive-Load Drivability," *IEEE Trans. Circ. Syst.I*, vol. 63, no. 10, pp. 1567–1578, Oct. 2016.

[100] D. Marano, A. D. Grasso, G. Palumbo, and S. Pennisi, "Optimized active single-miller capacitor compensation with inner half-feedforward stage for very high-load three-stage OTAs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1349–1359, Sep. 2016.

[101] W. Qu, S. Singh, Y. Lee, Y.-S. Son, and G.-H. Cho, "Design-oriented analysis for Miller compensation and its application to multistage amplifier design," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 517–527, Feb. 2017.

[102] R. W. Erickson, and D. Maksimovic, "Fundementals of Power Electronics" 2nd ed., Kluwer Academic Publishers, New York, 2004, pp. 348-354.

[103] N. weste and D. Harris, "CMOS VLSI Design", 4th ed., Pearson Education, Inc. 2011, pp. 256 - 257.

[104] D. A. Johns, and K. Martin, "Analog Integrated Circuit Design". United States: John Wiley & sons, 1997., pp. 290.

[105] R.J. Reay, G. Kovacs, "An unconditionally stable two-stage CMOS amplifier", *IEEE J. Solid-State Circ*., vol. 30, pp. 591-594, May 1995.

[106] S. Mahmoud Anisheh, H. Abbasizadeh, H. Shamsi1 , C. Dadkhah, and K.-Y Lee, "84 dB DC-gain two-stage class-AB OTA", *IET Circuits Devices Syst.*, 2019, Vol. 13 Iss. 5, pp. 614-621.

[107] T. Kulej and F. Khateb, "A 0.3-V 98-dB Rail-to-Rail OTA in 0.18 m CMOS", *IEEE Access*, 2020, Vol. 8, pp. 27459 – 27467.

APPENDICES

APPENDIX A

THE RELATIONSHIP BETWEEN THE 3-dB FREQUENCY (ω_{P0}) AND THE LF-ZERO (ω_{Z1})

This appendix provides more details on why the OTA step response will not be affected by the ratio ω_{Z1}/ω_{P0} that was mentioned in ***Section 3.1***.

To clarify the relationship between ω_{P0} and ω_{Z1}, we shall use the transfer function of Eqn. (3.1) (ignoring the parasitic pole), which is:

$$A(s) = \frac{A_{DC,2}}{\left(1+\frac{s}{\omega_{P0}}\right)} \times \frac{\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)}. \qquad (A.1)$$

Now, let us consider and compare all possible scenarios between ω_{Z1} and ω_{P0}, which are: $\omega_{Z1} < \omega_{P0}$, $\omega_{Z1} = \omega_{P0}$, and our proposed scenario $\omega_{Z1} > \omega_{P0}$. For this analysis, we shall keep the distance between ω_{Z1} and ω_{P1} fixed to only investigate the distance between ω_{Z1} and ω_{P0}.

Fig. A. 1(a) shows the open-loop AC response of these different scenarios. *Once the OTA is constructed in unity-gain closed-loop configuration, ω_{P1} will move towards ω_{Z1}, and ω_{P0} will*

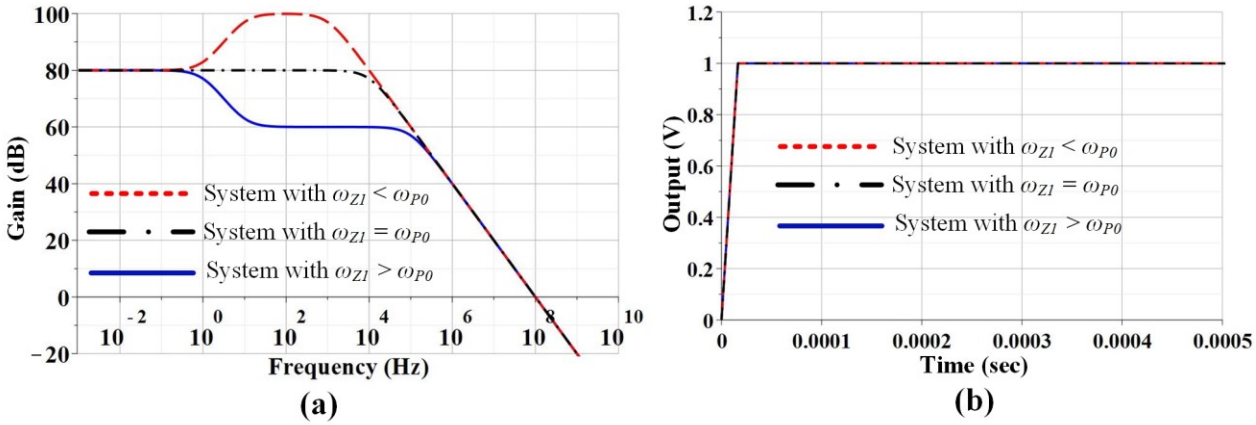

Fig. A.1: Comparison between the different scenarios of ω_{Z1} and ω_{P0} arrangements: (a) The open-loop AC magnitude response, and (b) the closed-loop unity-gain step response.

move towards ω_t. Consequently, the system will have almost the same step response as seen in Fig. A. 1(b) regardless of the distance between ω_{Z1} and ω_{P0}. Thus, the distance between ω_{Z1} and ω_{P0} will have no impact on the step response. The range of the time scale of Fig. A. 1(b) is purposely made large so that the effects of any step response residual can be seen.

APPENDIX B

REDUCING THE TRANSFER FUNCTION COMPLEXITY HAVING ONE *P-Z* PAIR

The proposed analysis in ***Section 3.2*** deals with an OTA that is usually required to operate over a large range of frequency conditions. Rather than design a new *TF* for each case, a better approach is to normalize the *TF* to reduce the degree of complexity as will be discussed in this Appendix.

Frequency scaling is a mathematical technique of shifting the poles and zeros of a *TF* to a new location in the complex s-plane, while maintaining the same functional behavior albeit over a different frequency range, i.e.

$$A(p) = A(s)|_{s=p/a} \qquad (B.1)$$

In this work, frequency normalization is used to reduce the number of coefficients in the *TF* of Eqn. (3.1) (ignoring the parasitic pole), as this serves to simplify the presentation. However, before performing the normalization on Eqn. (3.1), and since integrators are ideally at the core of

all OTA implementations, lets us consider having a DC pole and a finite pole instead of 2 finite poles. Therefore, the *TF* of Eqn. (3.1) is now described as an integrator function in the Laplace domain with a DC gain, $A_{DC} = A_1A_2$, and a *P-Z* pair as follows

$$A(s) \approx \frac{A_{DC}}{s} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \qquad (B.2)$$

This assumption will have some practical implications at frequencies < ω_{P0}. However, the proposed theory deals with the *P-Z* pair which are allocated at frequencies > ω_{P0}, thus, these practical implications will be of no significance.

The magnitude response of an undamped integrator is shown in Fig. B.1(a) and can be written with a scale factor A_{DC} as: $[A(s) = A_{DC}/s]$. Here A_{DC} represents the magnitude of the *TF* at 1 rad/s. However, as an alternative perspective, A_{DC} can also be viewed as the frequency at which the magnitude of the *TF* is unity (which will be referred to as $\omega_{t,REF}$) as depicted by Fig. B.1(a). Thus, the frequency and magnitude axes intercept points form an isosceles right-angled triangle. By introducing the *P-Z* pair, the *TF* will be written as Eqn. (B.2).

For the case, 1 rad/s ≤ ω_{Z1} < ω_{P1}, the magnitude of the TF will appear as that shown in Fig. B.1(b). The net effect of this *P-Z* arrangement is that $\omega_{t,REF}$ of the compensated OTA increases to Ω_t. Inspecting the plot in Fig. B.1(b), one can deduce that

$$\Omega_t = \frac{\omega_{P1}}{\omega_{Z1}} . \omega_{t,REF} = \frac{\omega_{P1}}{\omega_{Z1}} . A_{DC} \qquad (B.3)$$

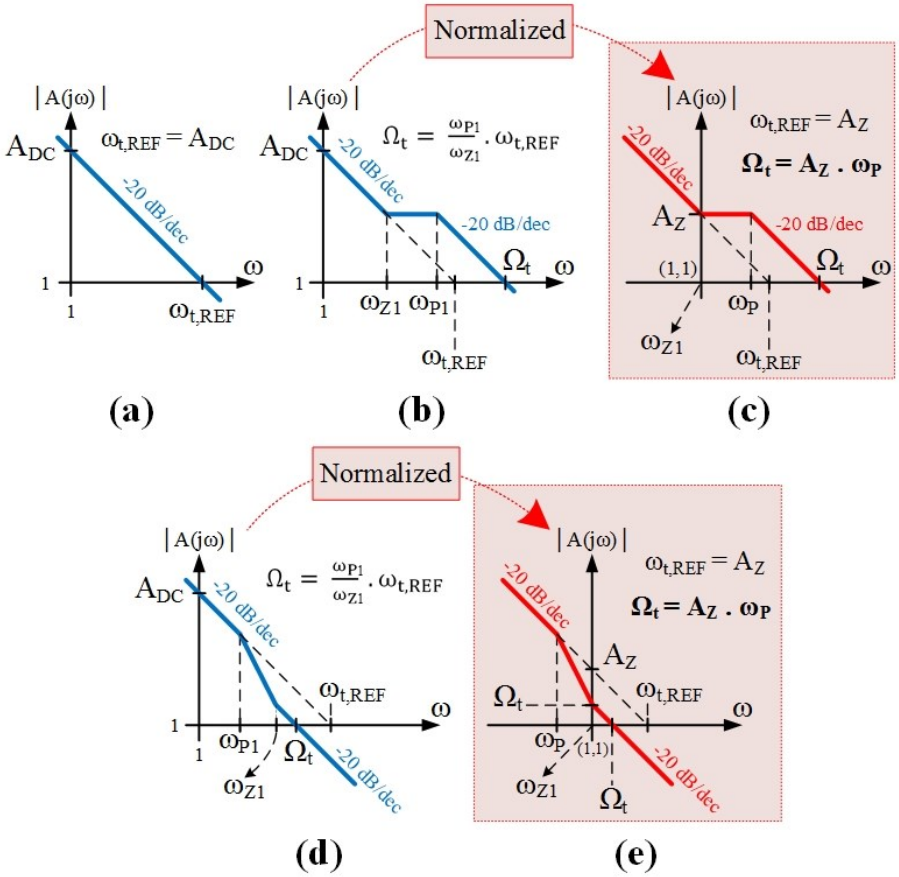

Fig. B.1: Integrator-based OTA magnitude response: (a) response with no *P-Z* compensator, (b) response with *P-Z* compensator ($\omega_{Z1} < \omega_{P1}$), (c) frequency normalized response of (b), (d) response with P-Z compensator ($\omega_{P1} < \omega_{Z1}$), and (e) frequency normalized response of (d).

Clearly, the greater the frequency distance between the *P-Z* pair, the higher the unity-gain frequency achievable.

For the case when 1 rad/s $\leq \omega_{P1} < \omega_{Z1}$), then a different magnitude response appears as shown in Fig. B.1(d). In this case Ω_t is less than $\omega_{t,REF}$. Even though $\omega_{P1} < \omega_{Z1}$ the expression for Ω_t is the same as that listed in Eqn. (B.3).

OTAs are required to operate over a large range of frequency conditions. Rather than design a new TF for each case, a better approach is to normalize the *TF* with respect to 1 rad/s and then translate the *TF* such that the zeros are shifted to a new location. On doing so, the poles of the *TF* are shifted as well. In this work, the frequency normalization was performed by setting ω_{ZI} to 1 rad/s, such as that shown in Fig. B.1(c) and (e). Also superimposed on this figure is the frequency-normalized unity-gain frequency Ω_t in terms of the open-loop parameters, where it can be written as in Eqn. (3.18).

To rewrite the open loop *TF* of Eqn. (B.2) using the normalized approach, the "*s*" Laplace variable will be replaced with the "*p*" Laplace variable (i.e., $p = s/\omega_{ZI}$). On doing so, Eqn. (B.2) would be written as in Eqn. (3.17), where ω_{ZI} is always assumed to be at 1 rad/s and the value A_Z is always the gain of the integrator at $\omega_{ZI} = 1$ rad/s, regardless of the relation between ω_{PI} and ω_{ZI}. The same concept can be generalized for *N*-stages to derive Eqn. (3.27) and (3.36).

APPENDIX C

DERIVATION OF THE CLOSED-LOOP POLES HAVING ONE *P-Z* PAIR

This Appendix gives more detail on the analysis in ***Section 3.2.1*** to find the expressions for the closed-loop poles.

If the open-loop transfer function includes a *P-Z* pair as described in Eqn. (3.17), then the closed-loop transfer function, T(p), would appear as

$$T(p) = \frac{A_Z\ \omega_P\ (p+\ 1)}{p^2 + p\ (1 + A_Z)\ \omega_P + \ A_Z\ \omega_P} \qquad (C.1)$$

Factoring the denominator, the closed-loop TF can be written as in Eqn. (3.19). As $A_Z >> \omega_P$ (i.e. or $\omega_{t,REF} >> \omega_P$), the two closed-loop poles will be widely spaced apart. Further, using the quadratic formula for a second-order polynomial, specifically the denominator of Eqn. (C.1), combined with the series relationship $\sqrt{1-x}\ \approx 1 - \frac{1}{2}\ x - \frac{1}{8}\ x^2$, one can find the two closed-loop pole frequencies as in Eqn. (3.20) and (3.21).

APPENDIX D

DERIVATION OF THE UNITY-GAIN STEP-RESPONSE HAVING ONE *P-Z* PAIR

This Appendix gives more detail on the analysis in ***Section 3.2.2*** to derive and simplify the unit-step response of Eqn. (3.25).

Based on the results found in Eqns. (3.20), (3.21) and (3.24), the closed loop TF of Eqn. (3.19) can be approximated as

$$T(p) = \frac{(p+\ 1)}{\left(1 + \frac{p}{A_Z \omega_P}\right)\left(1 + \frac{p}{(1+\ \delta_{CL})}\right)} \qquad (D.1)$$

Then the unit step response y(t) can be written as

$$y(t) = 1 - \left(\frac{A_Z\ \omega_P}{A_Z\ \omega_P - 1 -\ \delta_{CL}}\right)(1 + \delta_{CL})\ e^{-\ A_Z \omega_P\ t} + \left(\frac{A_Z \omega_P}{A_Z \omega_P - 1 -\ \delta_{CL}}\right)\delta_{CL}\ e^{-\ (1+\delta_{CL})t} \qquad (D.2)$$

According to Eqn. (3.18), and as ($A_Z \times \omega_P$) is much greater than unity, the step response expression can be reduced to

$$y(t) \approx 1 - (1 + \delta_{CL})\, e^{-A_Z\, \omega_P\, t} + \delta_{CL}\, e^{-(1+\delta_{CL})t} \qquad (D.3)$$

where δ_{CL} is given by Eqn. (3.23). It is interesting to note that exponential term with a *LF* time constant has a multiplicative term that depends directly on δ_{CL}. From Eqn. (3.23), this separation distance depends on two parameters from the open loop response, A_Z and ω_P.

The unit step response can be simplified by substituting Eqn. (3.23) into (D.3) and write

$$y(t) = 1 - \left(1 + \frac{1 - \omega_P}{A_Z\, \omega_P}\right) e^{-A_Z \omega_P\, t} + \left(\frac{1 - \omega_P}{A_Z\, \omega_P}\right) e^{-\left(1+\frac{1-\omega_P}{A_Z \omega_P}\right)t} \qquad (D.4)$$

This expression will hold over a wide range of ω_P and A_Z, regardless of value. However, y(t) in Eqn. (D.4) can be written for different cases of ω_P as in Eqn. (3.26).

APPENDIX E

DEALING WITH THE COMPLEX POLES, ZEROS, AND COEFFICIENTS

This Appendix explains the impact of the complex poles which were found in ***Section 3.3.1***.

The presence of complex terms or poles in Table 3.2 offers no conceptual difficulties if one considers that any one complex term always appears with a second complex conjugate term that forms a pair having the following general form:

$$(A + jB)\, e^{(C+jD)t} + (A - jB)\, e^{(C-jD)t} \quad . \qquad (E.1)$$

Rearranging the above expression, one can show that

$$(A + jB)\, e^{(C+jD)t} + (A - jB)\, e^{(C-jD)t} = 2\sqrt{A^2 + B^2}\cos(D.t + \emptyset)\, e^{-Ct} \quad , \qquad (E.2)$$

where

$$\emptyset = \tan^{-1}\left(\frac{B}{A}\right) \quad . \qquad (E.3)$$

Putting aside the cosine term as its value is bounded between – 1 and 1, the effective exponential coefficient term is essentially twice the magnitude of the leading complex term $A+jB$ of one term of the complex conjugate pair.

APPENDIX F

THE JUSTIFICATION FOR ARRANGING THE POLE-ZERO PAIRS ACCORDING TO EQN. (4.4)

This Appendix gives more justifications of using Eqn. (4.4) as mentioned in ***Section 4.1.1***.

Equation (3.27) and Eqn. (3.36) in the proposed theory represent the ideal normalized case of positioning the poles and zeros. However, once the transfer function is realized using circuit level components, coupling between stages, correlation between *P*-*Z* positions and parasitic poles will limit our flexibility to satisfy the desired transfer function. Therefore, we had to arrange the *P*-*Z* pairs according to Eqn. (4.4) to ensure stability and avoid the complexity of describing the exact positions of the poles and zeros. Fortunately, this new practical arrangement (i.e., according to Eqn. (4.4)) will not affect our verification of the proposed theory, which suggests that increasing A_Z will reduce the impact of the *P*-*Z* pairs regardless of their exact numbers or the positions/distances between them. The reason is that once the OTA is configurated in closed-loop, the *N*-1 poles will move towards the *N*-1 zeros, and one pole will move towards the unity-gain frequency, ω_t.

To clarify this issue in more details, let's start by assuming an OTA with an N^{th}-order transfer function with N-1 zeros, such as that defined by Eqn. (3.1), i.e.,

$$A(s) = \frac{A_{DC}}{\left(1 + \frac{s}{\omega_{P\_3dB}}\right)} \times \prod_{i=1}^{N-1} \frac{\left(1 + \frac{s}{\omega_{Zi}}\right)}{\left(1 + \frac{s}{\omega_{Pi}}\right)} \qquad (F.1)$$

the N-1 poles of the unity-gain closed-loop system will converge towards the zeros of the open-loop transfer function for large A_{DC}. Mathematically, this can be expressed as

$$\omega_{P,i} \rightarrow \omega_{Zi} \;\; \forall \, i = 1..N-1 \qquad (F.2)$$

The remaining pole will move upward in frequency to a high-frequency value given by

$$\omega_{P,HF} = A_{DC} \times \omega_{P0} \times \prod_{i=1}^{N-1} \frac{\omega_{Pi}}{\omega_{Zi}} \qquad (F.3)$$

This is true regardless of the positions of the parasitic poles and zeros, $\omega_{P,i}$ and $\omega_{Z,i}$. Consider an OTA with a second transfer function such as

$$A(s) = \frac{A_{DC}}{\left(1 + \frac{s}{\omega_{P0}}\right)} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \qquad (F.4)$$

The transfer function of a unity-gain configuration involving this OTA would have a closed-loop transfer function given by

$$T(s) = \frac{A_{DC} \times \omega_{P0}(s + \omega_{Z1})\omega_{P1}}{\omega_{Z1}s^2 + (A_{DC}\omega_{P0}\omega_{P1} + \omega_{P1}\omega_{Z1} + \omega_{P0}\omega_{Z1})s + A_{DC}\omega_{P0}\omega_{P1}\omega_{Z1} + \omega_{P0}\omega_{P1}\omega_{Z1}} \qquad (F.5)$$

Factoring the roots of the denominator, leads to

$$\omega_{P,CL,1} = \frac{A_{DC}\omega_{P0}\omega_{P,1}\omega_{Z,1} + \omega_{P0}\omega_{P,1}\omega_{Z,1}}{A_{DC}\omega_{P0}\omega_{P,1} + \omega_{P0}\omega_{Z,1} + \omega_{P,1}\omega_{Z,1}} \qquad (F.6)$$

and

$$\omega_{P,CL,2} = \frac{A_{DC}\omega_{P0}\omega_{P,1} + \omega_{P0}\omega_{Z,1} + \omega_{P,1}\omega_{Z,1}}{\omega_{Z,1}} \qquad (F.7)$$

For large A_{DC}, the roots can be approximated as

$$\omega_{P,CL,1} \approx \omega_{Z,1} \qquad (F.8)$$

and

$$\omega_{P,CL,2} \approx A_{DC} \times \omega_{P0} \times \frac{\omega_{P,1}}{\omega_{Z,1}} \qquad (F.9)$$

For higher-order amplifier transfer functions, similar results can be seen to occur. Unfortunately, finding symbolic formulae for the closed-loop poles is no easy task. This is the reason for the attempting to work the theory from the perspective of co-incident poles and zeros, together with frequency normalization.

To give more clarifications and proof that the theory is indeed sound, lets' consider a 3rd order numerical example. Let the OTA open-loop transfer function be described by

$$A(s) = \frac{1000}{\left(1 + \frac{s}{100}\right)} \times \frac{\left(1 + \frac{s}{200}\right)}{\left(1 + \frac{s}{300}\right)} \frac{\left(1 + \frac{s}{400}\right)}{\left(1 + \frac{s}{500}\right)} \qquad (F.10)$$

where the parasitic poles and zeros are located above the 3-dB frequency of 100 rad/s. The unity-gain closed-loop transfer function becomes

$$T(s) = \frac{A(s)}{1 + A(s)} = \frac{15 \times 10^9 \times \left(1 + \frac{s}{200}\right)\left(1 + \frac{s}{400}\right)}{s^3 + 1884 \times 10^2 s^2 + 11273 \times 10^4 s + 15015 \times 10^6} \qquad (F.11)$$

The poles of closed-loop system are therefore (-1.878x10^5, -199.92, -399.91). According to the above expressions, the magnitude of the closed-loop poles would be

$$\omega_{P,CL,1} \approx \omega_{Z,1} = 200 \qquad (F.12)$$

$$\omega_{P,CL,2} \approx \omega_{Z,2} = 400 \qquad (F.13)$$

$$\omega_{P,HF} \approx A_{DC} \times \omega_{P,3dB} \times \frac{\omega_{P,1}}{\omega_{Z,1}} \times \frac{\omega_{P,2}}{\omega_{Z,2}} = 1000 \times 100 \times \frac{300}{200} \times \frac{500}{400} = 1.875 \times 10^5 \qquad (F.14)$$

Thus, agreeing with the above theory.

For a DC gain of 10,000, the closed-loop poles are (-1.8753x10^6, -199.992, -399.991) and the closed-loop poles predicted by theory are

$$\omega_{P,CL,1} \approx \omega_{Z,1} = 200 \qquad (F.15)$$

$$\omega_{P,CL,2} \approx \omega_{Z,2} = 400 \qquad (F.16)$$

$$\omega_{P,HF} \approx A_{DC} \times \omega_{P,3dB} \times \frac{\omega_{P,1}}{\omega_{Z,1}} \times \frac{\omega_{P,2}}{\omega_{Z,2}} = 10000 \times 100 \times \frac{300}{200} \times \frac{500}{400} = 1.875 \times 10^6 \qquad (F.17)$$

Thus, closed-loop poles predicted by theory is in very good agreement with those found by factoring the characteristic polynomial of the closed-loop transfer function.

Next, let us consider different pole and zero positions, as described by the following open-loop transfer function:

$$A(s) = \frac{1000}{\left(1+\frac{s}{100}\right)} \times \frac{\left(1+\frac{s}{10}\right)}{\left(1+\frac{s}{300}\right)} \frac{\left(1+\frac{s}{200}\right)}{\left(1+\frac{s}{500}\right)} \qquad (F.18)$$

Here one zero is placed below the lowest pole at 100 rad/s to emphasize the fact that location of the poles relative to the zeros does not change the above-described facts. Consequently, the closed-loop transfer function becomes

$$T(s) = \frac{A(s)}{1+A(s)} = \frac{15 \times 10^9 \times \left(1+\frac{s}{10}\right)\left(1+\frac{s}{200}\right)}{s^3 + 75009 \times 10^2 s^2 + 157523 \times 10^4 s + 15015 \times 10^6} \qquad (F.19)$$

and the roots of the denominator are (-7.50068x10^6, -200.002, -10.0089). The magnitude of the poles predicted by theory are

$$\omega_{P,CL,1} \approx \omega_{Z,1} = 10 \qquad (F.20)$$

$$\omega_{P,CL,2} \approx \omega_{Z,2} = 200 \qquad (F.21)$$

$$\omega_{P,HF} \approx A_{DC} \times \omega_{P,3dB} \times \frac{\omega_{P,1}}{\omega_{Z,1}} \times \frac{\omega_{P,2}}{\omega_{Z,2}} = 1000 \times 100 \times \frac{300}{10} \times \frac{500}{200} = 7.5 \times 10^6 \qquad (F.22)$$

Thus, closed-loop poles under the above three different conditions follow the proposed theory very closely.

APPENDIX G

THE DETAILS OF PRODUCING FIGURE 5.3

This Appendix provides the full details about the steps being followed to produce Fig. 5.3 in ***Section 5.1.2.2.***

The simulations on the two-stage OTA of Fig. 4.3 to produce Fig. 5.3 have been done by fixing all circuit parameters and sweeping R_{C1} from 20 kΩ to 125 kΩ to observe the value of (ω_{P1}/ω_{Z1}), and to make sure that ($\omega_t \leq \omega_{Ppar}$) for all this range of R_{C1}.

Fig. G.1 shows the open-loop AC response of the 2-stage CMOS OTA of Fig. 4.3 for different values of R_{C1}. As can be clearly seen in Fig. G.1, ω_{Z1} is moving to lower frequencies by increasing R_{C1}, while ω_{P1} is almost fixed at around 150 MHz. Based on these simulations Table G.1 shows how the ratio (ω_{P1}/ω_{Z1}) is increasing by increasing R_{C1}. This ratio has been reported in Table 5.3. Also, ω_{Ppar} impact can be seen increasing as R_{C1} is increasing, which indicates that ω_{Ppar} is moving to lower frequencies, but ω_{Ppar} is always higher than ω_t. To clarify these relationships, Table G.1 summarizes these simulation results.

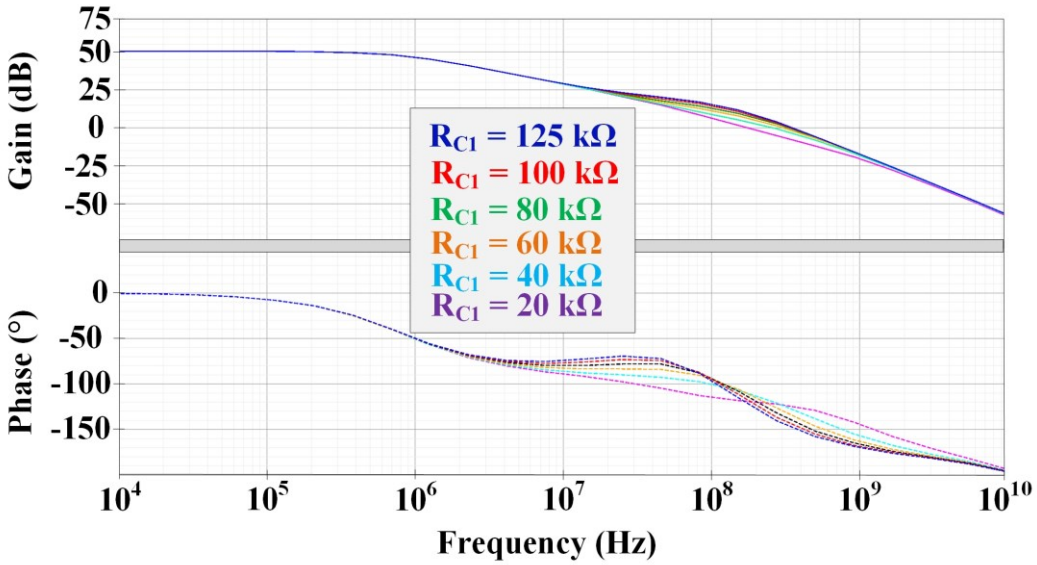

Fig. G.1: The open-loop AC response of the 2-stage OTA (i.e., Fig. 4.3) for different values of R_{C1}.

TABLE G.1
SIMULATION RESULTS SHOWING THE IMPACT OF INCREASING R_{C1} ON OPEN-LOOP PARAMETERS OF THE 2-STAGE CMOS OTA OF FIG. 4.3

	R_{C1} (kΩ)					
	20	**40**	**60**	**80**	**100**	**125**
ω_{P1} (MHz)	150	150	150	150	150	150
ω_{Z1} (MHz)	167	80.2	52.6	39.4	31.25	25.8
(ω_{P1}/ω_{Z1})	0.89	1.87	2.85	3.8	4.81	5.81
ω_t (MHz)	175	255	307	331	343	354
PM (°)	62	60.8	50	42	36.5	33
ω_{Ppar} (MHz)	800	511	487	406	403	400

Looking at the maximum value of R_{C1} (i.e., 125 kΩ) in Table G.1, one can see that ω_{Ppar} is still at frequencies higher than ω_t, but its impact on the PM is increasing. However, this impact on PM has not affected the OTA's stability, and to investigate this, the output step response of all process corners under PVT variations were conducted at R_{C1} = 20 kΩ and R_{C1} = 125 kΩ in Fig. 5.6 of Section 5.1.2.3. It is clear form Fig. 5.6 that the OTA is stable:

1. For schematic and post-layout,

2. Under all process corners
3. At the minimum value of R_{C1} (i.e., 20 kΩ) and at the maximum value of R_{C1} (i.e., 125 kΩ).

This indicates that the theory is applicable, and the parasitic poles are being observed according to the proposed design technique, and their impact is under control. Also, this indicates that the proposed theory regarding the impact of A_Z on settling time is true, where the increment in A_Z (i.e., positioning the zero at low frequencies) will highly reduce the impact of (ω_{P1}/ω_{Z1}).

APPENDIX H

SIMULATION RESULTS OF THE TRANSIENT UNITY-GAIN CLOSED-LOOP STEP-RESPONSE OF THE 2- TO 8-STAGE CMOS OTAS

This Appendix shows the simulation results that have been omitted from ***Section 5.2.2*** for simplicity.

Since the proposed OTA is meant for closed-loop operations, a test of its stability under large input-signals as well as small-input signals is shown in the closed-loop unity-gain step responses of Figs. 5.7(b). However, for simplicity, part of these transient responses is being shown in Fig. 5.7(b), and the rest are being reported in Fig. H.1.

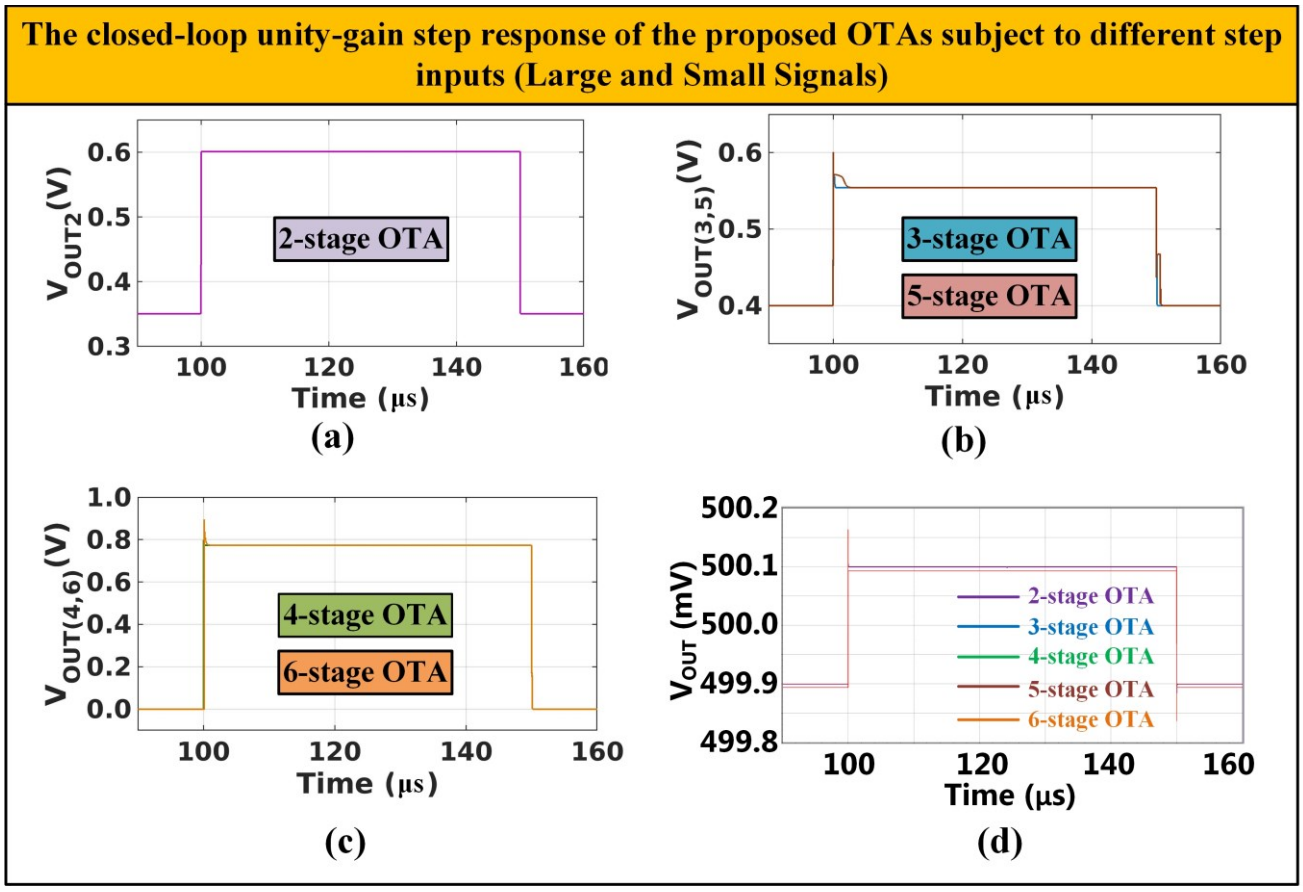

Fig. H.1: Stability tests, using the closed-loop unity-gain step response, of the proposed OTAs of Fig. 4.3 subject to a range of different large signals (to show the OTAs' capability to operate under different step values). (a) 2-stage OTA subject to a large signal of 300 mV, (b) 3-stage and 5-stage OTAs subject to a large signal of 200 mV, (c) 4-stage and 6-stage OTAs subject to a large signal of 800 mV, and (d) the closed-loop unity-gain step response, of the proposed 2-, 3-, 4-, 5- and 6-stage OTAs subject to a small signal of 0.2 mV. All OTA-stage responses from 2 to 5 are matched.

APPENDIX I

OPEN-LOOP & CLOSED-LOOP SIMULATIONS OF THE PROPOSED OTAS UNDER DIFFERENT C_LS

In this Appendix, the open-loop and closed-loop simulations that have been omitted from ***Section 6.3*** for simplicity, are shown here.

The open-loop and closed-loop simulations (i.e., schematic and post-layout) are shown for the 2-, 3-, and 4-stage CMOS OTAs in Fig. I.1, I.2, and I.3, respectively. These simulations have been done for different values of C_L. Based on these simulations; all OTA metrics have been extracted to create Fig. 6.2 and Fig. 6.3 in attempt to verify the proposed scalable many-stage CMOS OTA design results of Fig. 4.7 and 4.8.

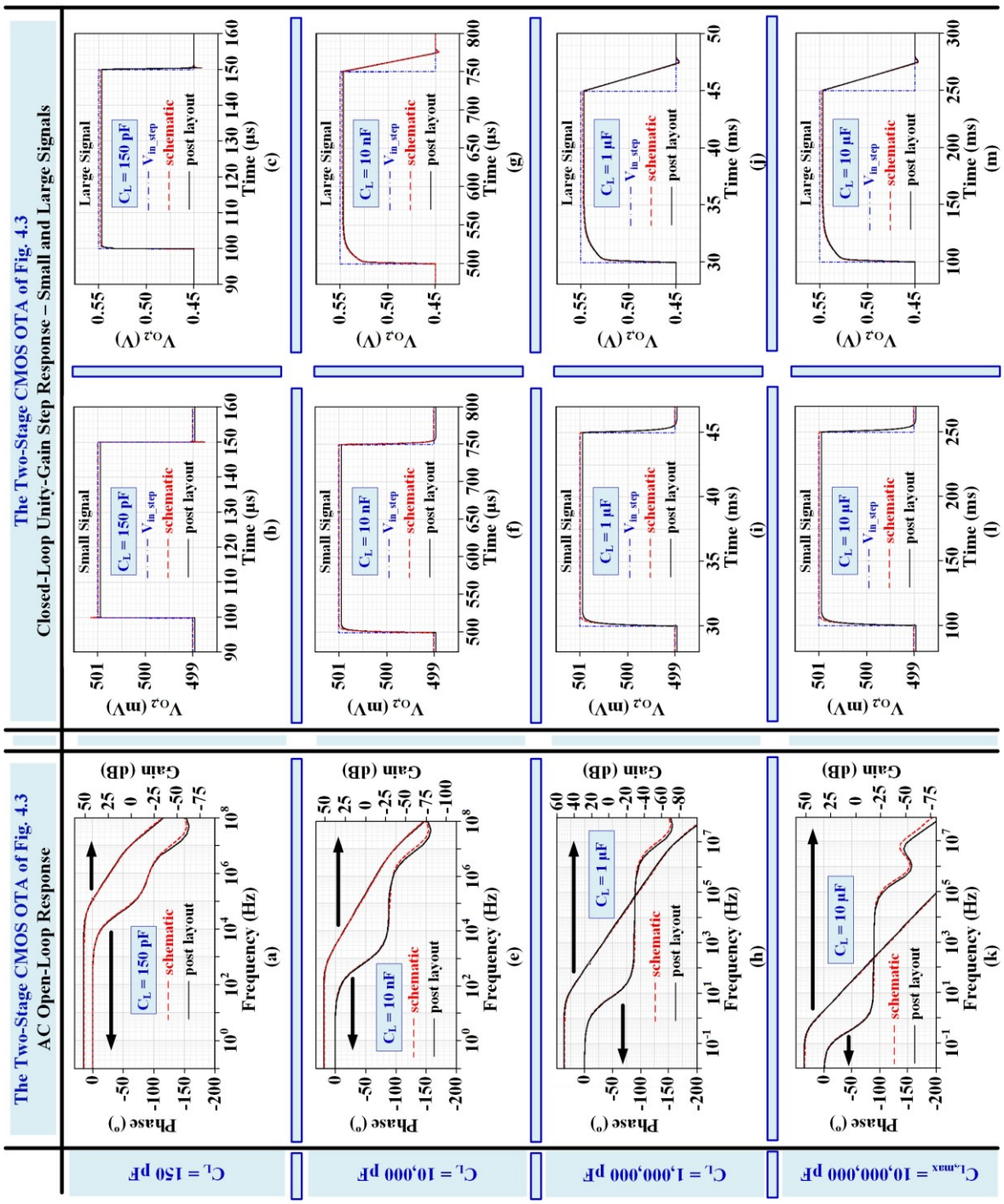

Fig. I.1: Open-loop & closed-loop schematic and post-layout simulations of the differential-ended two-stage CMOS OTA of Fig. 4.3 after implementing the proposed FCT under different values of C_L

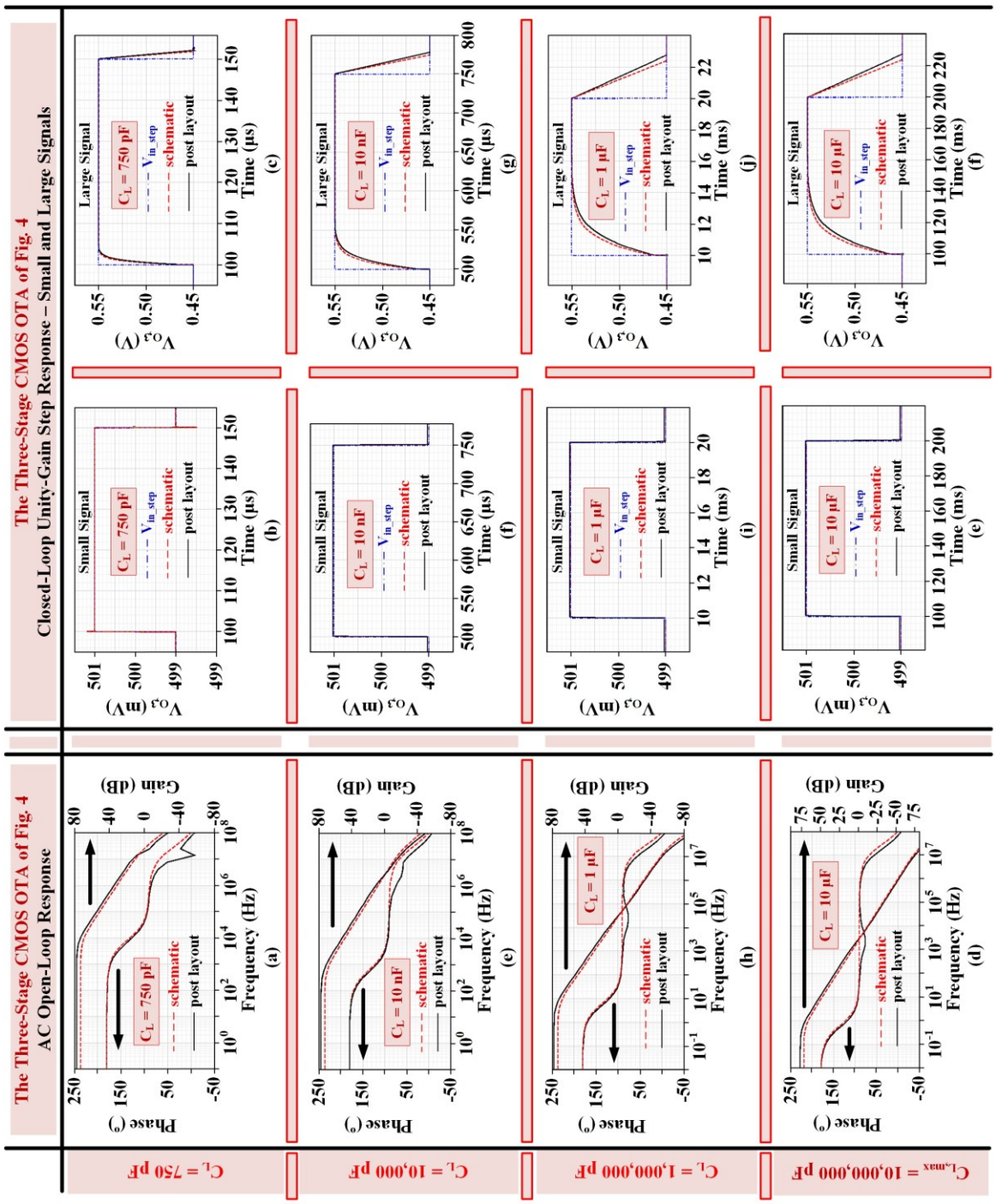

Fig. I.2: Open-loop & closed-loop schematic and post-layout simulations of the differential-ended three-stage CMOS OTA of Fig. 4.3 after implementing the proposed FCT under different values of C_L

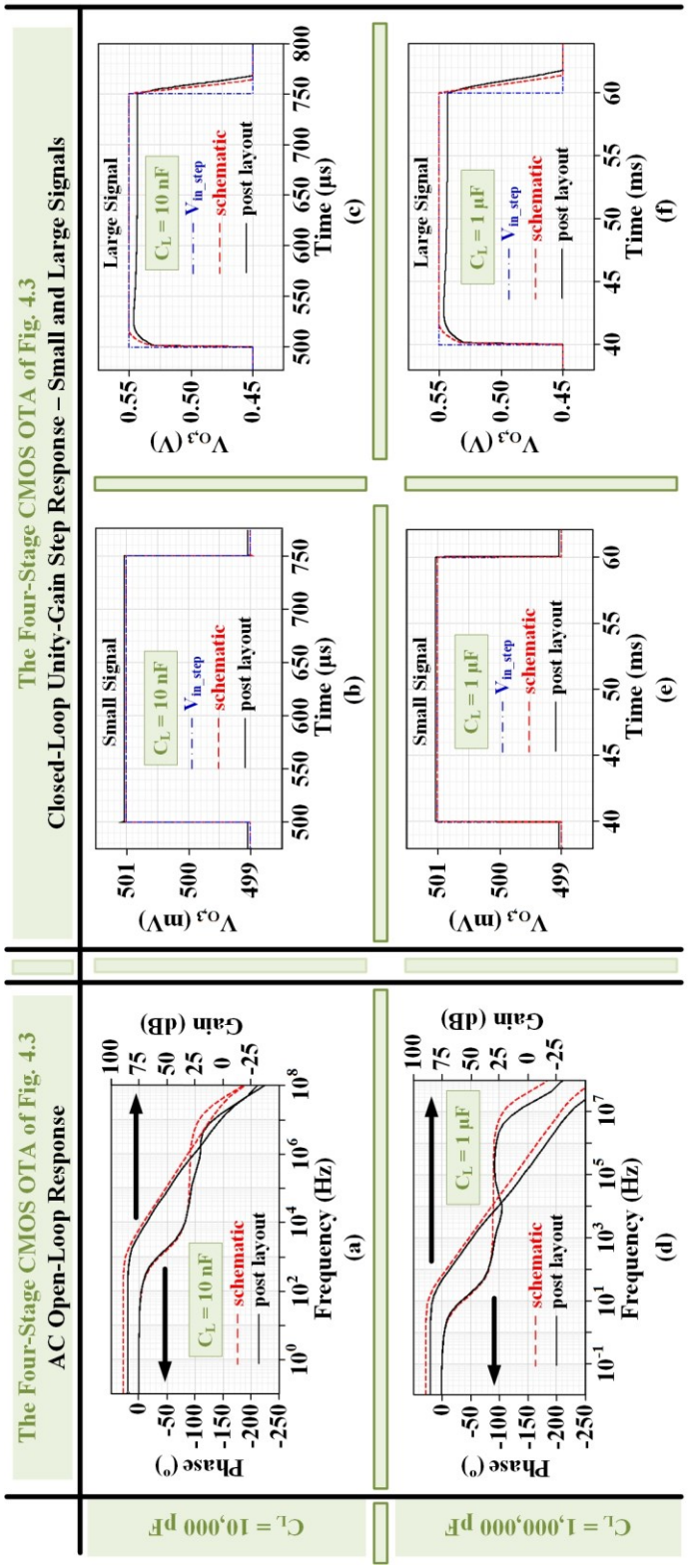

Fig. I.3: Open-loop & closed-loop schematic and post-layout simulations of the differential-ended Four-stage CMOS OTA of Fig. 4.3 after implementing the proposed FCT under different values of C_L

APPENDIX J

THE LAYOUT DRAWINGS OF THE PROPOSED OTAS

This Appendix illustrates the layout drawings of the fabricated chip of Fig. 6.4 (i.e., in ***Section 6.4***). Therefore, Fig. J.1 shows the layout drawings for the differential-ended 2-, 3-, and 4-stage CMOS OTAs for the case of having C_L on-chip. The dimensions and the occupied silicon area of these OTAs are shown in Fig. 6.4. As for the design with C_L off-chip, the same drawings are used, except that C_L has been removed from these drawings. To illustrate this, one can compare between the two-stage OTA layouts of Fig. 6.4 and J.1, where in Fig. 6.4 the layout is for the case of having C_L off-chip, while Fig. J.1 shows the layout drawing having C_L on-chip.

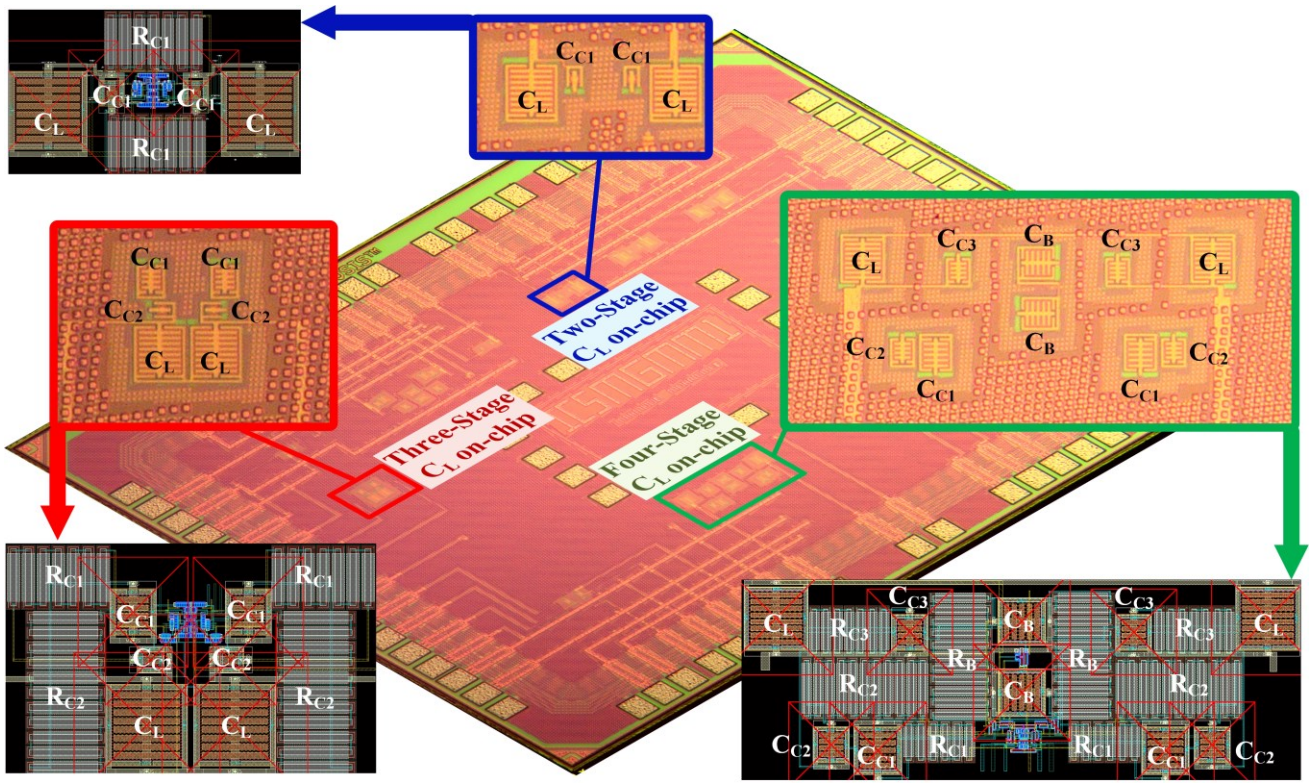

Fig. J.1: The chip's microphotograph showing the proposed differential-ended 2-, 3- and 4-stage CMOS OTAs with C_L on-chip along with the layout drawing for each OTA.

Our closing prayer will be, “All praise is for Allah—Lord of all worlds!”