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DEVELOPMENT OF HIGH-EFFICIENCY SOLAR CELLS ON $CuInSe_2$ SINGLE CRYSTALS

by

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A thesis submitted to the Faculty of Graduate Studies and Research

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

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February, 1996

ISBN 0-612-12515-7

ABSTRACT

Photovoltaic cells with a ZnO/CdS/$CuInSe_2$ structure have been fabricated on bulk $CuInSe_2$ substrates. Conversion efficiencies of more than or near 10 % were routinely obtained on cells with an active area of up to 8 mm^2 and without the use of an antireflection coating. The highest conversion efficiency of 11.5 % was obtained on a cell with an active area of 4 mm^2. This cell is comparable in conversion efficiency to the highest value of 12 % [1] reported in the literature for monocrystalline $CuInSe_2$ cells but has an active area of more than five times larger.

The $CuInSe_2$ single crystals were grown by a horizontal Bridgman method. Adhesion of the $CuInSe_2$ ingot to the inner wall of the quartz ampoule was observed in earlier experiments. This problem was later overcome by the inclusion of a getter, such as a thick layer of carbon or a piece of solid graphite, into the ampoule. Using this method, uniform p-type $CuInSe_2$ single crystals of up to 2 cm on a side were obtained. A thin layer of high-resistivity CdS was deposited onto the mechanical-polished $CuInSe_2$ substrate as the buffer layer. The CdS layer was deposited by a chemical-bath method and was about 300 to 500 Å thick. A low-resistivity ZnO window layer of about 1 μm thick was then deposited on top of the CdS by r.f. magnetron sputtering.

An annealing of the $CuInSe_2$ substrate before the CdS deposition was found to be essential in obtaining high photovoltaic performance. The optimal annealing condition was 350 °C in argon for 2 hours. The annealing was able to reduce the large density of defect states on the mechanical-polished $CuInSe_2$ surface and led to a substantial decrease of the dark junction current. Both the open-circuit voltage and fill factor were significantly improved by the substrate annealing. Temperature-dependent I-V measurements showed that the current transport of the

$ZnO/CdS/CuInSe_2$ cells was governed by a tunneling/recombination mechanism. Capacitance-voltage measurements showed the presence of interface states and deep levels. The buried homojunction observed in some $CdS/CuInSe_2$ cells [2] was not detected by electron-beam-induced-current (EBIC) measurements in the $ZnO/CdS/CuInSe_2$ cells. The diffusion lengths of the $CuInSe_2$ substrates were also determined by EBIC and were estimated to be about 4 to 6 μm. A deep level at about 0.23 eV from the valence band edge was identified in most of the $CuInSe_2$ crystals by deep-level transient spectroscopy. The density of this deep level was about 10^{13} to 10^{14} cm^{-3}. A shallower deep level was also observed in some of the samples.

[1] J.L. Shay, S. Wagner and H.M. Kasper, *Appl. Phys. Lett.* **27**, 89 (1975).

[2] R.J. Matson, R. Noufi, R.K. Ahrenkiel and R.C. Powell, *Solar Cells* **16**, 495 (1986).

RÉSUMÉ

Des cellules photovoltaïques de structure ZnO/CdS/$CuInSe_2$ ont été fabriquées sur substrats de $CuInSe_2$. Une efficacité de conversion de plus ou de près de 10 % a régulièrement été obtenue sur des cellules dont la surface active allait jusqu'à 8 mm^2, sans l'utilisation d'une couche antireflet. L'efficacité de conversion maximale de 11.5 % a été obtenue sur une cellule ayant une surface active de 4 mm^2. Cette cellule est comparable, en termes d'efficacité de conversion, à la valeur maximale de 12 % [1] publiée au sujet des cellules monocristallines de $CuInSe_2$, mais possède une surface active cinq fois plus grande.

La croissance de monocristaux uniformes de $CuInSe_2$ de type p a été obtenue par la méthode de Bridgman horizontale. Une adhésion du lingot de $CuInSe_2$ sur les parois intérieures de l'ampoule de quartz a été observée lors d'essais précédents. Ce problème a été résolu par l'ajout d'un anti-adhésif, tel une épaisse couche de carbone ou une pièce de graphite solide, dans l'ampoule. Grâce à cette méthode, des monocristaux de $CuInSe_2$ ayant des dimensions latérales jusqu'à 2 cm ont été obtenus. Une mince couche de CdS à haute résistivité a été déposée sur le substrat mécaniquement poli de $CuInSe_2$ à titre de couche tampon. La couche de CdS, d'une épaisseur de 300 à 500 Å, a été déposée par méthode de bain chimique. Une couche fenêtre de ZnO à basse résistivité d'environ 1 µm d'épaisseur a ensuite été déposée sur le CdS par pulvérisation cathodique r.f.

Une recuite du substrat de $CuInSe_2$ avant la déposition du CdS s'est avérée essentielle afin d'obtenir de hautes performances photovoltaïques. Les conditions de recuite optimales étaient de 350 °C dans l'argon pour 2 heures. La recuite a permis de réduire la haute densité d'état de

défauts sur la surface de $CuInSe_2$ mécaniquement polie et a conduit à une baisse substantielle du courant de la jonction non illuminée. La tension en circuit ouvert et le facteur de charge ont tous deux été significativement améliorés par la recuite du substrat. Des mesures I-V selon la température ont démontré que le transport du courant dans les cellules de $ZnO/CdS/CuInSe_2$ était réglé par un mécanisme d'effet tunnel et de réassociation. Des mesures de capacité-tension ont démontré la présence d'états d'interface et de niveaux profonds. L'homojonction enfouie, observée dans quelques cellules de $CdS/CuInSe_2$ [2], n'a pas été détectée par les mesures de courant induit par faisceaux d'électrons (EIBC) effectuées sur les cellules de $ZnO/CdS/CuInSe_2$. La longueur de diffusion des substrats de $CuInSe_2$ a également été déterminée par EBIC à environ 4 à 6 μm. Un niveau profond à près de 0.23 eV du bord de la bande de valence a été identifié, dans la plupart des cristaux de $CuInSe_2$, par spectroscopie transitoire à niveaux profonds. La densité de ce niveau profond était d'environ 10^{13} à 10^{14} cm^{-3}. Un niveau plus superficiel a également été observé dans quelques-uns des échantillons.

[1] J.L. Shay, S. Wagner and H.M. Kasper, *Appl. Phys. Let.* **27**, 89 (1975).

[2] R.J. Matson, R. Noufi, R.K. Ahrenkiel and R.C. Powell, *Solar Cells* **16**, 495 (1986).

ACKNOWLEDGMENTS

The author wishes to express his sincere gratitude to his supervisor, Dr. I. Shih, for his guidance and assistance throughout this study. Special thanks are extended to Dr. C. H. Champness for his helpful suggestions and discussions on the present work and also for reading the manuscript.

The author is also indebted to Dr. C. X. Qiu for her assistance on the initial work of ZnO deposition, Mr. W.W Lam for his assistance on the Hall-effect measurements, and Ms. Christine Alain for translating the abstract into French. Thanks are also due to the staff in the electrical and mechanical workshops in the department for their technical assistance.

Acknowledgments are also due to The Natural Sciences and Engineering Research Council of Canada for the financial support.

The author would like to express his gratitude to his parents, brothers and sisters for their love, encouragement and support throughout his life.

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CHAPTER 1

INTRODUCTION

As world energy consumption increases steadily, concerns of the prospect of exhaustion of convention energy resources, such as fossil fuels, are also growing. Combined with the environmental issues of fossil fuels, such as air pollution, acid rain and global warming, alternative resources of energy production are earnestly considered. Nuclear energy has been used in some countries and contributes significantly to their total energy production. However, radioactive waste disposal, safety concerns of the nuclear facilities and the possibility of misuse of the nuclear materials not only raise environmental but also political issues. The widespread use of nuclear energy is still controversial.

With minimum environmental pollution and unlimited resource, renewable energy has great potential to become the major supply of energy in the future. Photovoltaic energy conversion is one of the promising renewable energy sources. Although it is still too expensive to become a major energy source, photovoltaic energy conversion excels in several areas, such as space applications, consumer electronics and remote area power generation. With the continuous decrease of cost and increase of conversion efficiency, the use of photovoltaic systems for large-scale terrestrial energy production may be within reach in the near future.

Copper indium diselenide ($CuInSe_2$) is one of the four thin-film materials from which solar cells with conversion efficiencies greater than 10 % have been demonstrated. The other three materials are amorphous silicon, cadmium telluride and cuprous sulfide. Actually, thin-film $CuInSe_2$ cells are approaching commercial applications with Siemens Solar Industries

demonstrating $CuInSe_2$ alloy-based large-area modules with an area of 0.37 m^2 and a conversion efficiency of 11.4 % [1.1]. Thin-film photovoltaic cells are desirable for large-scale terrestrial applications because the manufacturing cost can be minimized by the small material cost of thin films and the use of low-cost deposition techniques. Therefore, most of the studies on $CuInSe_2$ have been carried out with thin polycrystalline films of this material. However, single-crystal $CuInSe_2$ has been proved to be valuable for providing fundamental understanding of this semiconductor. Furthermore, single-crystal $CuInSe_2$ cells, although not feasible for practical use because of cost considerations, may help to explore the potentials and limitations of this material for photovoltaic applications that may eventually lead to improvements in thin-film $CuInSe_2$ cells.

Copper indium diselenide is a ternary compound semiconductor with a chalcopyrite structure and an direct energy gap of about 1 eV. It has the highest optical absorption coefficient ($> 10^5$ cm^{-1}) reported for any semiconductor. Solar cells based on this material are also well known for their lifetime stability. Copper indium diselenide was first investigated in the 1950's as a member of the Cu-III-VI_2 family [1.2], which showed a potential in a variety of opto-electronic applications. However, the extraordinary absorption coefficients make $CuInSe_2$ an ideal absorber for solar cells, especially for thin-film applications. Shay, Wagner and Kasper [1.3] were the first to demonstrate its potential with a small-area 12 % CdS/$CuInSe_2$ photovoltaic cell in 1975 based on a single-crystal $CuInSe_2$ substrate. Later developments showed an extensive research activities on thin-film $CuInSe_2$-based solar cells and a steady increase of conversion efficiency for thin-film cells. However, there were limited research activities on single-crystal $CuInSe_2$ cells and the 12 % efficiency has remained the highest for single-crystal cells for the past two decades, probably due to the difficulties in growing high-quality $CuInSe_2$ single crystals and preparing the $CuInSe_2$ surfaces for device fabrication. The main objectives of the present work are to grow large and

good-quality $CuInSe_2$ single crystals and to fabricate solar cells based on these $CuInSe_2$ single crystals with high conversion efficiency.

In the pioneering work of $CuInSe_2$-based solar cells, Shay et al. [1.3] fabricated a cell with a conversion efficiency of 12 % by depositing a 5-10 μm thick CdS onto the cleaved "B" (selenium) (112) face of $CuInSe_2$ platelets. The CdS window layer was deposited by a coaxial isothermal double source method [1.4]. Au was used as the ohmic contact to the p-$CuInSe_2$ substrate. The open-circuit voltage (V_{oc}) , short-circuit current density (J_{sc}), fill factor (FF) and conversion efficiency (η) measured under a solar illumination of about 92 mW/cm^2 were 0.5 V, 38 mA/cm^2, 0.60 and 12%, respectively. It should be noted that an anti-reflection coating of SiO was applied on the cell for these measurements and the uncoated cell had a conversion efficiency of 10.6%. The high efficiency was measured in a small active area of 0.79 mm^2 in order to avoid microcracks, which severely limited the performance of the solar cell, on the $CuInSe_2$ substrate. An earlier CdS/$CuInSe_2$ cell fabricated by the same workers [1.4] as a broad-band visible and near-infrared detector showed a solar conversion efficiency ot about 5 %. The single-crystal $CuInSe_2$ substrate, however, was mechanically polished and etched in aqua regia before the CdS deposition.

An indium-tin-oxide (ITO)/$CuInSe_2$ heterojunction cell was fabricated by Kazmerski et al. [1.5]. The ITO provided a wide-bandgap window layer (3.7 eV) for the monocrystalline $CuInSe_2$ absorber. The ITO films were grown by electron beam deposition. An elevated substrate temperature of 180 °C had to be used in order to get improved device performance. No information was provided for the $CuInSe_2$ surface preparation or crystal orientation. The $CuInSe_2$ surface was ion-etched in situ before the ITO deposition and this procedure was essential in obtaining high V_{oc} and FF. Au was used as the back contact metal to the $CuInSe_2$ substrate. The

V_{oc}, J_{sc}, FF and η were 0.50 V, 30.77 mA/cm^2, 0.55 and 8.5 %, respectively, under AM1 illumination. The active area of the cell was 0.13 cm^2.

Arya et al. [1.6] also reported a CdS/$CuInSe_2$ cell fabricated on a $CuInSe_2$ polycrystal grown by the Bridgman method. Thin pellets of about 1 mm thick were cut from a large-grained $CuInSe_2$ boule, mechanically polished on both sides, and then etched in a 2 % solution of bromine+methanol. A layer of CdS with a thickness of 2.4 μm was evaporated onto the $CuInSe_2$ pellet. Au was also used as the ohmic contact to the p-$CuInSe_2$. The V_{oc}, J_{sc}, FF and η measured under a simulated solar illumination of about 100 mW/cm^2 were 0.42 V, 33.3 mA/cm^2, 0.42 and 5.9%, respectively, for a cell with an area of 4.5 mm^2. Small area cells (0.8 mm^2) were then defined by masking with microstop wax and etching away the excess area with hydrochloric acid in order to avoid microcracks and other inhomogeneities. This resulted in dramatic improvements in the photovoltaic performance. Under the same illumination, V_{oc}, J_{sc}, FF and η were improved to 0.45 V, 40.0 mA/cm^2, 0.59 and 10.6%, respectively. It appears that no anti-reflection coating was applied to the cells in these experiments, making the cell performance comparable to the one reported by Shay et al. [1.3] for the uncoated cell.

Although most of the cells based on monocrystalline $CuInSe_2$ were fabricated on bulk crystals, cells based on epitaxial $CuInSe_2$ films were also reported by Grindle et al. [1.7]. In these experiments, epitaxial layer of $CuInSe_2$ was deposited by molecular beam epitaxy (MBE) onto a single-crystal CdS (0001B) substrate at 300 °C. In the MBE system, the three elements Cu, In and Se were contained in three separate graphite crucibles, which were heated to the desired temperatures during the experiments. The elemental beams were directed to the CdS substrates for the deposition. The composition and the resistivity of the $CuInSe_2$ epitaxial layers were strongly dependent on the ratio of the Cu/In arrival rate. Cells fabricated from the low-resistivity

p-type $CuInSe_2$ showed an ohmic I-V characteristic due to the Cd diffusion into these films. Cells fabricated from high-resistivity layers gave a poor photovoltaic response until the cells were annealed at 300-400 °C in argon. Under a simulated solar illumination of 100 mW/cm^2, the V_{oc}, J_{sc}, FF and η of such a cell were 0.34 V, 31 mA/cm^2, 0.44 and 4.7%, respectively.

Homojunctions of $CuInSe_2$ were also reported by several workers [1.8-1.10]. Yu et al. [1.8] reported the formation of a $CuInSe_2$ p-n homojunction by the diffusion of cadmium into p-type $CuInSe_2$. The $CuInSe_2$ single crystals were prepared by a melt-grown method. P-type single crystals with flat as-grown (112) surfaces were chosen for substrates. Substrates were etched with a hot solution of $HCl:HNO_3$ (1:1) before the Cd diffusion. The diffusion was carried out with the substrate placed at one end of an evacuated quartz ampoule and Cd metal shots placed at the other end. The quartz ampoule was then heated to 400 °C for 6-8 minutes. The substrate was then made into a mesa structure by etching the substrate in a hot solution of $HCl:HNO_3$ (1:1) with the n layer protected by wax. Au was sputtered onto the p side and In-Sn to the n sides as ohmic contacts. A quantum efficiency of 35-40 % in the wavelength region 0.9-1.2 μm was obtained in these cells. Only the quantum efficiency was reported in this paper. A similar solar cell was also reported [1.9] by the same group with ion implantation replacing diffusion to form the junction. A quantum efficiency of 60-70 % in the wavelength region 0.7-1.1 μm was reported.

Tell et al. [1.10] reported the formation of p-n homojunctions by annealing Zn-, Cd- and Cu-plated p-type $CuInSe_2$ samples at temperatures from 200-450 °C. A zone-melting technique was used to grow the $CuInSe_2$ single crystals. Some of the as-grown slices were annealed in saturated Se vapour before the junction formation. This procedure resulted in more uniform junction depth after diffusion. P-type slices up to 1 mm thick were etched in $HCl:HNO_3$ (1:1) solution. Junctions were formed by plating the etched surfaces with Zn or Cd from cyanide

solutions or Cu from a Cu_2SO_4+HNO_3 solution and then by annealing and quenching to room temperatures in evacuated quartz ampoules. A series of junctions was formed with various combinations of annealing times and temperatures. The ohmic contact to the p-$CuInSe_2$ was provided by plated Au; while the plated Zn, Cd or Cu provided the ohmic contact to the n diffused region. A large V_{oc} of 0.45 V was obtained in a cell with Cd diffusion.

More recently, Abou-Elfotouh et al. [1.11] reported the fabrication of a (Cd,Zn)S/$CuInSe_2$ cell on mechanically-polished $CuInSe_2$ single-crystal substrates for the studies of defect levels. Photovoltaic performance of the cells were limited to below 4 % in conversion efficiency and 0.25 V in open-circuit voltage. To the author's knowledge, these were about all the single-crystal $CuInSe_2$ photovoltaic cells reported for the last two decades although other works on the studies of the properties of single-crystal $CuInSe_2$ or $CuInSe_2$ crystal growth have also been reported.

Although single-crystal $CuInSe_2$ cells have seen little progress for the last two decades, the same cannot be said to thin-film $CuInSe_2$ cells. Constant progress has been made for thin-film $CuInSe_2$ cells and the conversion efficiency has increased from just 3~4 % in 1976 [1.12] to more than 15 % [1.13] in 1993. Various methods such as three-source evaporation [1.14-1.16], sputtering [1.17-1.19], selenization of metal precursors [1.20-1.22], electro-deposition [1.23-1.25], spray-pyrolysis [1.26-1.27] have been used to deposit thin-film $CuInSe_2$ with a various degrees of success. Arising from the studies of $CuInSe_2$ thin-film cells, $CuInSe_2$-based alloys have also been investigated and shown great promise. Recently, a ZnO/CdS/Cu(In,Ga)Se_2 cell with a total-area conversion efficiency of 16.8 %, which is the highest reported for cells on $CuInSe_2$-based compounds, was demonstrated [1.28].

The present work was set out to develop a fabrication process for a high-efficiency single-crystal $CuInSe_2$ photovoltaic cell. A ZnO/CdS/$CuInSe_2$ hetero-structure was employed for the

cell. The ZnO acted as a window material to provide the necessary electric field by forming a heterojunction with the monocrystalline $CuInSe_2$ substrate for the collection of light-generated carriers. The CdS was very thin and mainly acted as a buffer layer. This structure has also been widely used for thin-film $CuInSe_2$-based cells so that a comparison of the two types of cells can be conveniently made. The $CuInSe_2$ single crystals were grown by a horizontal Bridgman method while the CdS was deposited by a chemical bath method and the ZnO by sputtering. Results of the characterization of the materials and the analyses of the heterojunction are reported in this thesis.

The structure of this thesis is the following. In chapter two, the theory of solar cells is briefly reviewed. The crystal growth of $CuInSe_2$ and the characterization of the crystals are presented in chapter three. The experimental details of the heterojunction fabrication are then described in chapter four. Chapter five presents the electrical and photovoltaic characterizations of the heterojunctions. Results on electron-beam-induced current analysis of the heterojunctions are shown in chapter six, which is followed by the studies of deep-level-transient spectroscopy in chapter seven. Finally, conclusions are given in chapter eight.

CHAPTER 2

THEORY OF SOLAR CELLS

2.1 Introduction

Solar or photovoltaic cells are devices that convert sunlight directly into electricity by means of special semiconductor materials and device structures. This electricity can be utilized when an external electric load is connected to the solar cell. The basic mechanism of this photovoltaic effect involves the release of electric charges, i.e. electrons and holes in semiconductors, by the incident light followed by the separation of these charges by an internal electric field, usually provided by a p-n junction, in the solar cell. These separated charges are then collected by metal electrodes and flow through an external load.

Fig. 2.1 shows the photovoltaic effect in a p-n junction in which the incident photons create electron-hole pairs that are eventually separated by the electric field in the space charge or depletion region. The electric field distribution of the p-n junction is also shown in the figure. Electron-hole pairs are created in the space charge region and also in the neutral regions. The charge carriers created inside the neutral region have to reach the depletion region by diffusion in order to be collected. Depending on the semiconductors used and the device structure, charge carriers created outside the space charge region can contribute significantly to the collected current for some devices, especially for those semiconductors with a small absorption coefficient; while for some devices, electron-hole pairs created inside the space charge region are more significant.

Only photons with energy larger than the bandgap energy of the semiconductor are absorbed by valence electrons, which will jump to the conduction band and leave behind holes in the valence band to form electron-hole pairs. However, the photons are not absorbed immediately at the incident surface, some will travel deep into the semiconductor before being absorbed. The absorption coefficient, which is different for each wavelength, of the semiconductor determines, on average, how far a photon can travel in the semiconductor before being absorbed. Charge carriers created too far, with a distance greater than one diffusion length of the minority carriers, from the space charge region usually do not contribute to the output current. They would recombine before they could reach the electric field and be collected. Therefore, in order to maximize the collection efficiency of the light-generated charge carriers, a cell structure which allows most of the light to be absorbed near the space charge region should be used. For example, in a p-n homojunction solar cell, this is achieved by using a very thin top layer to allow a significant portion of the incident light to reach and be absorbed in the depletion region and the bottom layer. The photocurrent contribution from the thin top layer is, thus, small and is usually further reduced by surface recombination and short diffusion length.

In the case of $CuInSe_2$, a heterojunction is commonly used. In the heterojunction, the top layer is usually a large bandgap semiconductor, called a window layer, which allows most of the spectrum of sunlight to pass without significant absorption. Most of the incident light will then be absorbed in the $CuInSe_2$, which is aptly called an absorber, inside or near the depletion region due to the large absorption coefficients of $CuInSe_2$, therefore, relaxing the requirement for long diffusion length. Other factors, such as shunt and series resistances, also affect the performance of a solar cell. In the following sections, the important parameters of a solar cell will be discussed in more details.

2.2 Absorption Coefficient

An incident photon flux in a semiconductor decreases exponentially into the semiconductor with the distance from the incident surface, due to absorption, and can be expressed as

$$F(x) = F(0)e^{-\alpha x}, \qquad (2.1)$$

where F(x) is the photon flux, measured in number of photons per square centimeter per second per photon energy, at a distance x, F(0) is the incident photon flux at the semiconductor surface and α is the absorption coefficient at a particular photon energy. The generation rate of electron-hole pairs, which is equal to the photon absorption rate per unit volume, can then be expressed as

$$G(x) = -\frac{dF(x)}{dx} = \alpha F(0)e^{-\alpha x}. \qquad (2.2)$$

It can be seen that the generation rate of the free carriers is a strong function of the absorption coefficient. The absorption coefficient as a function of photon energy is shown in Fig. 2.2 for several commonly used semiconductors for solar cell applications. Photons with energies smaller than the energy bandgap of a semiconductor are generally not absorbed, as can be seen from the essentially zero absorption coefficients for such photons. However, the transition of α is abrupt for direct-bandgap materials, such as $CuInSe_2$ and CdTe, but more gradual for indirect-bandgap materials, such as monocrystalline Si. Furthermore, the absorption coefficients of direct-bandgap materials are usually significantly larger than indirect-bandgap materials. In the case of single-crystal Si photovoltaic cells, most of the low energy photons will travel deep into the semiconductor and, hence, a thick layer of silicon (some tens of microns) is required to absorb

the whole solar spectrum. Charge carriers generated deep in the Si base region have to diffuse to the space charge region to be collected. Therefore, the longer the diffusion length in the base layer is, the better the collection efficiency will be.

For a direct-gap semiconductor suitable for solar cell applications, the absorption coefficients are relative high and constant compared to indirect-gap material for all the photons with energy larger than the bandgap. Hence, only a thin layer of material is needed to absorb all the photons. They are, therefore, more suitable for thin-film solar cell applications. $CuInSe_2$ has the highest absorption coefficient reported for any semiconductor, exceeding 10^5 /cm for photons with energies larger than the bandgap energy, so that a $CuInSe_2$ layer of less than 1 μm thick is sufficient to absorb most of the solar radiation. If a homojunction is used for such a semiconductor, most of the photons will be absorbed near the incident surface of the top layer. Most of the free carriers will have to diffuse across the top layer to the junction to be collected; unless a very thin top layer is used, loss of charge carriers through recombination can be large. Furthermore, a large density of recombination centres are usually present at the top surface and recombination loss at these centres can be significant. Therefore, a p-n heterojunction is usually used for $CuInSe_2$ and other semiconductors with high absorption coefficients.

In a heterojunction, the n- and p-type semiconductors forming the junction are two different semiconductors. Usually the pair of semiconductors should have a good lattice match in order to minimize the interface states, which can also act as recombination centres. A semiconductor with a large α is generally used as an absorber. A matching large bandgap semiconductor is used as the window layer. The energy band diagram of such a p-n heterojunction is shown in Fig. 2.3. In the figure, E_{g1} is the energy gap of the window layer and

E_{g2} is the energy gap of the absorber. As explained before only photons with energies lying between E_{g1} and E_{g2} will be absorbed by the absorber and contribute to the photocurrent.

It is obvious that the larger the energy band gap of the window layer material, the more photons can be absorbed by the absorber. However, it does not have to be exceedingly large because the solar spectrum has only a small number of high energy photons as can be seen in Fig. 2.4. Other properties such as lattice constants as mentioned before, thermal expansion coefficient and conductivity and other design considerations are also important factors that have to be taken into account for choosing an appropriate window layer material. CdS was a very common window layer material for $CuInSe_2$ because the (0001) plane of CdS has a very good lattice matching with the (112) plane of $CuInSe_2$ and has a modestly large bandgap of 2.4 eV. However, ZnO has replaced CdS as the more popular window layer for $CuInSe_2$ because of its large bandgap (3.3 eV) and good electrical and antireflection properties. Furthermore, it can minimize the use of the toxic cadmium although CdS is still commonly used as a thin buffer layer for $CuInSe_2$ based cells because of the excellent lattice matching.

2.3 Spectral Response

The number of light-generated charge carriers collected relative to the number of incident photons at a particular wavelength is the spectral response of a solar cell. The spectral response of a solar cell is sometimes called quantum efficiency. It can be represented by the following equation,

$$SR(\lambda) = \frac{I_p(\lambda) + I_n(\lambda) + I_{dr}(\lambda)}{qAF(\lambda)} = \frac{I_L(\lambda)}{qAF(\lambda)}, \qquad (2.3)$$

where λ is the wavelength of the photons, $I_p(\lambda)$, $I_n(\lambda)$ and $I_{dr}(\lambda)$ are the photocurrent collected at this wavelength in the p, n and depletion regions, respectively, q is the electron charge, A is the area of the solar cell, $F(\lambda)$ is the incident photon flux and $I_L(\lambda)$ is the total photocurrent collected. This is the external spectral response of the solar cell.

An internal spectral response is also defined by considering only the photons entering the cell, i.e. by subtracting the reflection at the top surface, in order to measure only the internal absorption and loss mechanism. The spectral response depends on the absorption coefficients, diffusion lengths and the doping concentrations of the window and absorber layers, and also depends on the design structure of the solar cell.

Some useful information can be learnt from the spectral response. For example, by looking at the spectral response, a cell designer may learn that absorption at some wavelengths needs improvement, which may be achieved by tuning the properties of the semiconductor and/or modifying the cell structure. The internal spectral response of a typical Si p-n homojunction solar cell is shown in Fig. 2.5. The ideal response curve corresponds to the ideal case in which every photon above the bandgap energy is absorbed and contributes to the photocurrent without any loss. It can be seen that the base region mainly absorbs low energy photon while the front region mainly absorbs high energy photons and the contribution to the total photocurrent from the depletion region is small in this cell. Of course, the spectral response curve of a solar cell with different semiconductors and cell structure could be quite different from the one shown in Fig. 2.5.

2.4 Open-circuit Voltage, Short-circuit Current, Fill Factor and Conversion Efficiency

The equivalent circuit of a p-n junction, either a homojunction or heterojunction, solar cell is shown in Fig. 2.6. It is basically considered as a p-n junction diode in parallel with a light-generated current source, which is opposite in direction to the forward-biased current of the diode. The shunt resistance R_{sh} of the diode can be caused by leakage along the edges of the cell or other defects such as crystal defects, grain boundaries or microcracks. The series resistance R_s accounts for the bulk resistance of the p- and n-type semiconductors and the resistance of the front and back contacts. R_L represents the resistance of the load to which the solar cell is connected and delivers power. When it is not illuminated, the solar cell can be considered just as a p-n junction diode and has the following current-voltage (I-V) characteristic,

$$I_D = I_o[e^{\frac{q(V-R_S I_D)}{nkT}} - 1] + \frac{V - R_S I_D}{R_{sh}}, \qquad (2.4)$$

where I_D is the diode current, I_o is the diode saturation current, n is the diode ideality factor, k is the Boltzmann's constant, T is the temperature, R_S is the series resistance and R_{sh} is the shunt resistance. The value of the diode ideality factor, n, depends on the current mechanism across the p-n junction. It has a value of one when the current mechanism is thermal injection of the charge carriers across the p-n junction energy barrier, but has a value of two when the current mechanism is due to carrier recombinations in the space charge region.

In a practical device, the n value may lie between one and two because either due to a combination of the two current mechanisms or a modification of the detail of the current mechanisms under certain conditions [2.4]. However, the dark current-voltage characteristics of heterojunctions are sometimes dominated by tunneling [2.5]; in such a case the term q/nkT of the

exponential in Eq. (2.4) has to be replaced by a constant which is temperature independent but the basic form of the equation is the same. Although the diode ideality factor is no longer applicable for tunneling current, it can lead to an apparent n value from smaller than two [2.5] to larger than two [2.6, 2.7]. Therefore, a tunneling current may sometimes be mistakenly interpreted as a recombination current and/or an injection current.

The equivalent circuit of an illuminated solar cell has an I-V characteristic that can be represented by the following equation,

$$I = I_D - I_{ph} = I_o[e^{\frac{q(V-R_sI)}{nkT}} - 1] + \frac{V - R_S I}{R_{sh}} - I_{ph}, \qquad (2.5)$$

where I_{ph} is the photocurrent. Fig. 2.7 shows the I-V characteristics of a Si homojunction solar cell. The intercept of the I-V curve to the current axis corresponds to the short-circuit condition, when V = 0. From Eq. (2.5),

$$I_{sc} = I_o[e^{\frac{-qR_sI_{sc}}{nkT}} - 1] - \frac{R_S I_{sc}}{R_{sh}} - I_{ph}. \qquad (2.6)$$

Under normal illumination, the effect of the series resistance is negligible at the short-circuit condition for a good solar cell and the short-circuit current can be considered as equal in magnitude to the photocurrent, i.e. $I_{sc} = -I_{ph}$. Similarly, the shunt-resistance effect is usually negligible at the open-circuit condition, when I = 0. The open-circuit voltage can be expressed as,

$$V_{oc} = \frac{nkT}{q} \ln(\frac{I_{ph} + I_o}{I_o}). \qquad (2.7)$$

The short-circuit and open-circuit conditions can be represented by the equivalent circuit when $R_L = 0$ and $R_L = \infty$, respectively.

When the load resistance is between 0 and ∞, the power delivered to the load is equal to the product of I and V, i.e. $P_{out} = IV$. In real application, a particular load resistance value is usually used to maximize the power output,

$$P_{out}(\max) = I_m V_m, \tag{2.8}$$

where I_m is the current and V_m is the voltage at the maximum output power. The fill factor, FF, is defined as,

$$FF = \frac{P_{out}(\max)}{I_{sc}V_{oc}} = \frac{I_m V_m}{I_{sc}V_{oc}}. \tag{2.9}$$

The fill factor is affected strongly by the series and shunt resistances and depends also on the current mechanism, which determines the shape of the I-V curve and, in turn, the maximum power point.

The conversion efficiency is the most important parameter of a solar cell and it is a measure of the power-deliverance capacity of the solar cell to an external load under optimum condition. It is given by

$$\eta = \frac{P_{out}(\max)}{P_{in}} = \frac{I_m V_m}{P_{in}} = \frac{FF \cdot I_{sc} \cdot V_{oc}}{P_{in}}, \tag{2.10}$$

where P_{in} is the incident solar power. The three parameters, FF, I_{sc} and V_{oc} determine the conversion efficiency of the solar cell.

2.5 Effects of Series and Shunt Resistances

A large series and/or a small shunt resistances can have a detrimental effect on the performance of a solar cell. The open-circuit voltage is not changed but the fill factor is seriously reduced by a large series resistance as can be seen in Fig. 2.8 (a). The short-circuit current is also

reduced by the series resistance, but for a good solar cell with a small series resistance, the reduction should be negligible. However, the reduction of the fill factor may not be negligible even for a small series resistance. The shunt-resistance effect is shown in Fig. 2.8 (b). The short-circuit current is not affected but the fill factor is again reduced by a small shunt-resistance. The open-circuit voltage is also reduced in this case. In a practical device, the shunt-resistance is usually large enough to be neglected at 1 solar intensity or above. At low illumination intensities and low temperatures, the effect of shunt resistance becomes more and more important. On the contrary, the series resistance affects the solar cell performance at higher intensities and temperatures.

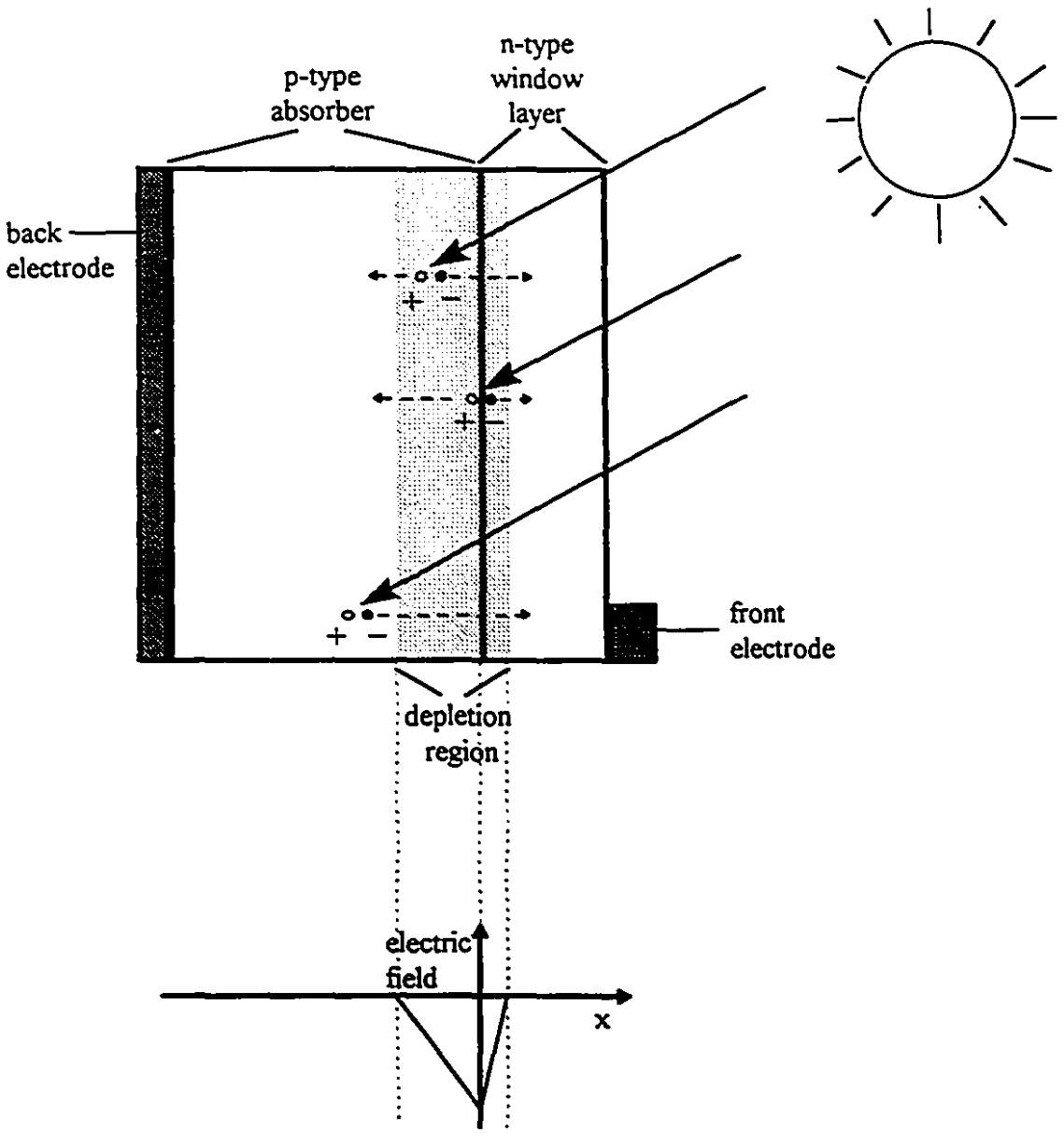


Fig. 2.1 Photovoltaic effect in a p-n junction. Electron-hole pairs are created inside and near the depletion region and separated by the electric field.

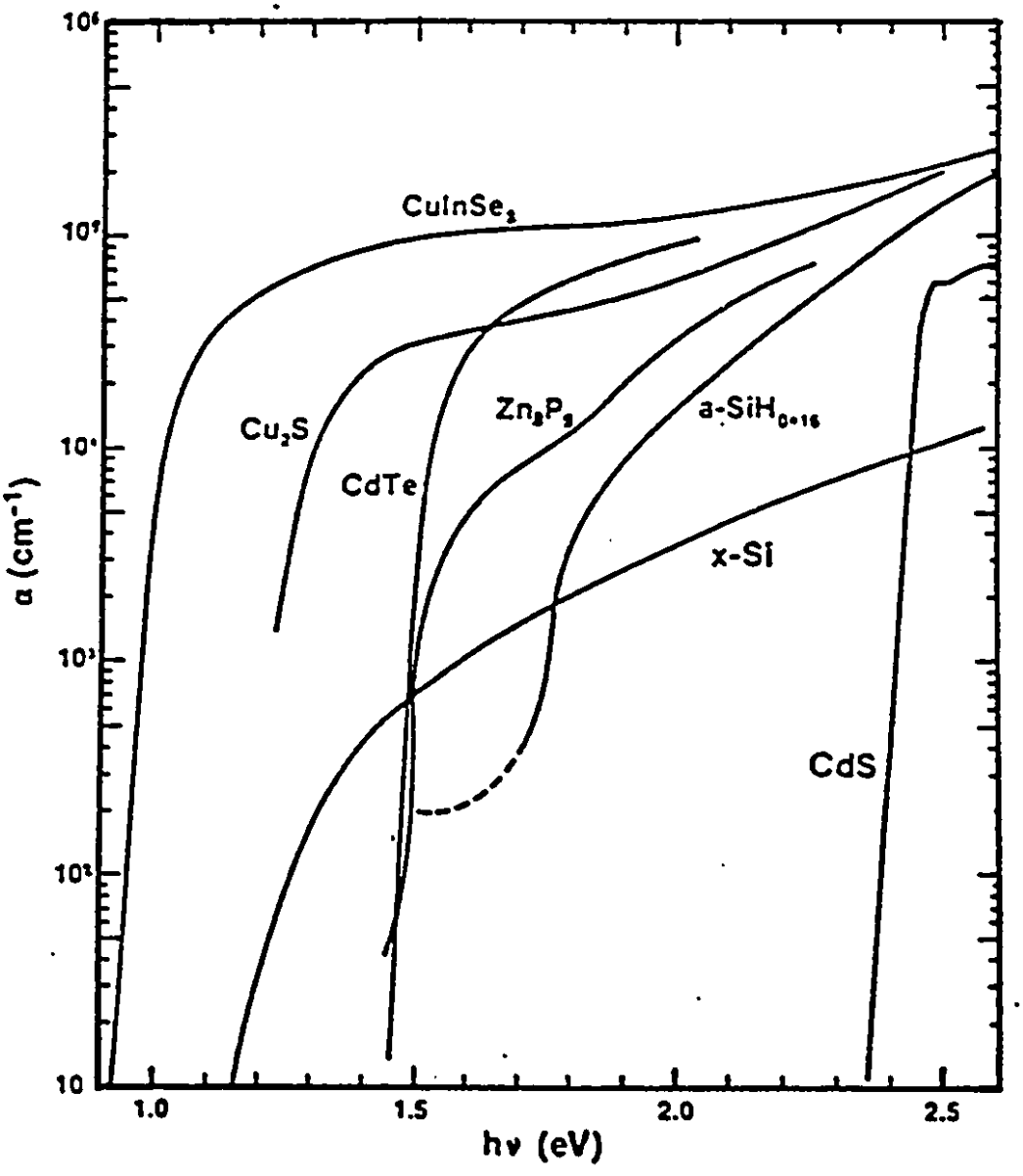


Fig. 2.2 Absorption coefficients of some semiconductors commonly used for solar cell applications. [2.1]

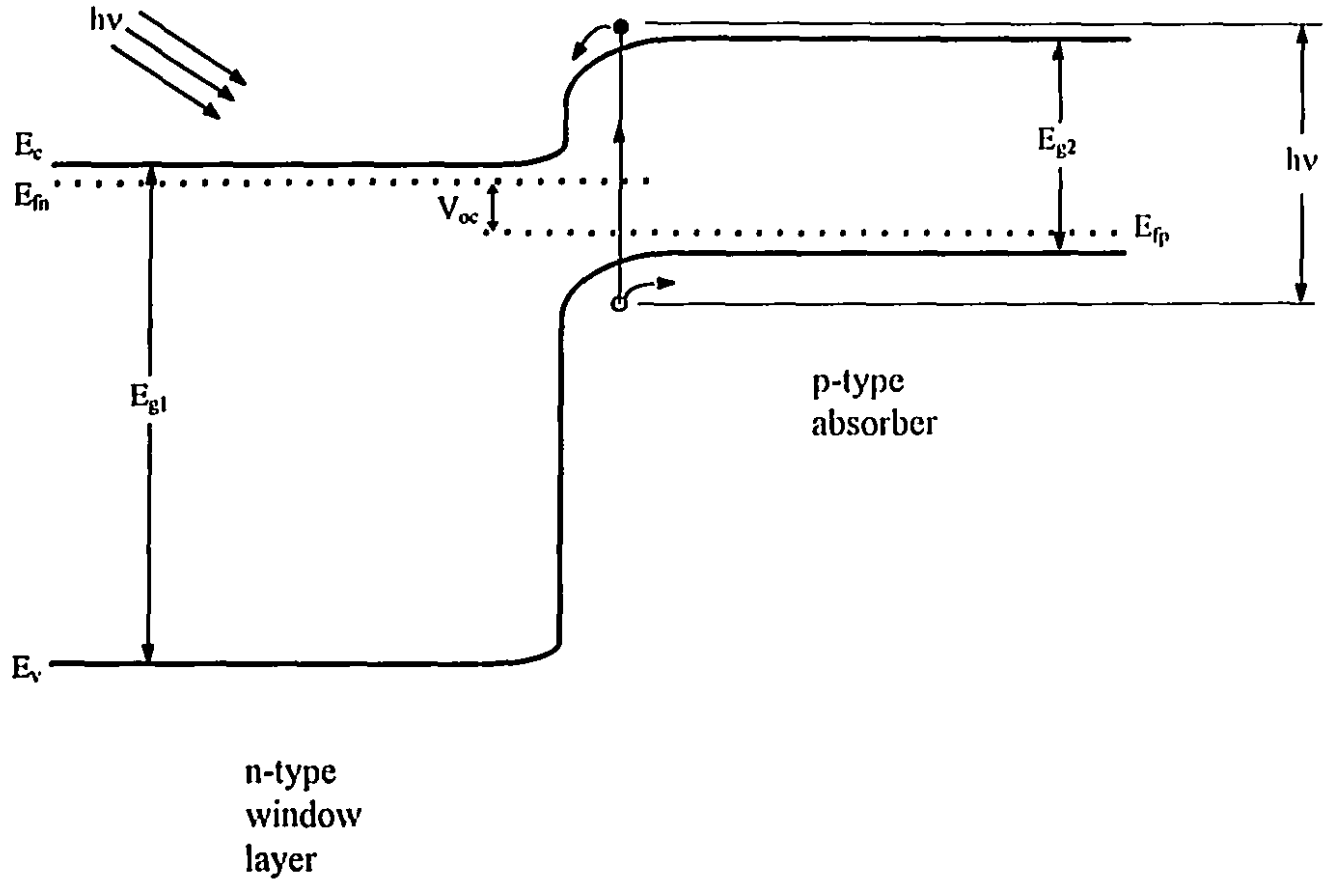


Fig. 2.3 The band diagram of a heterojunction solar cell.

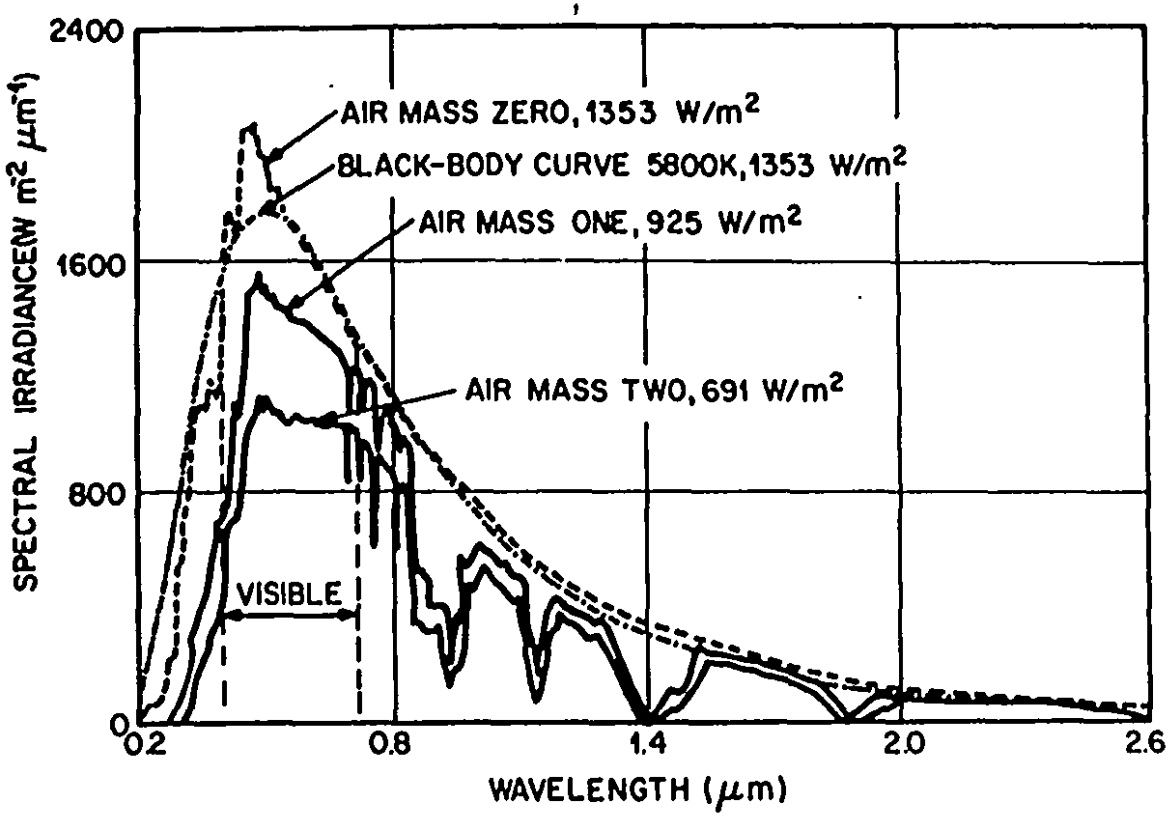


Fig. 2.4 Solar spectral irradiance measured at different air masses. [2.2]

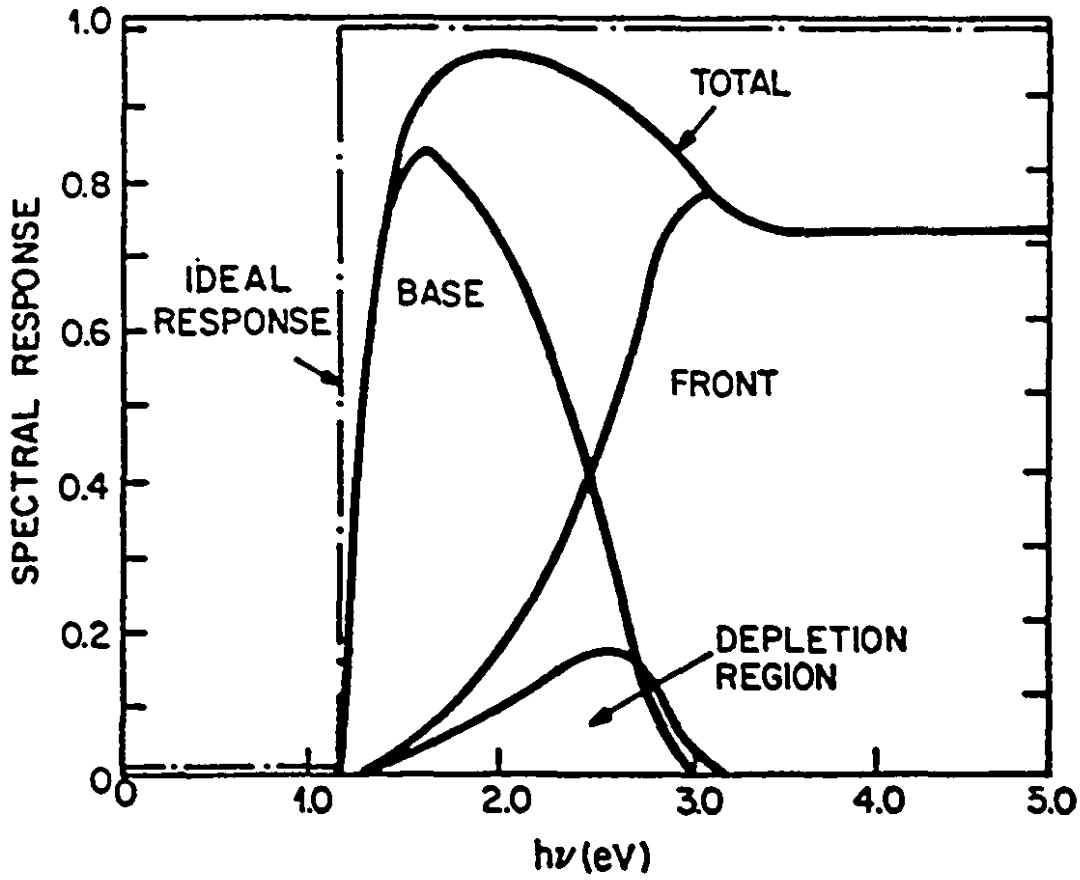


Fig. 2.5 The internal spectral response of a typical Si p-n homojunction solar cell. [2.3]

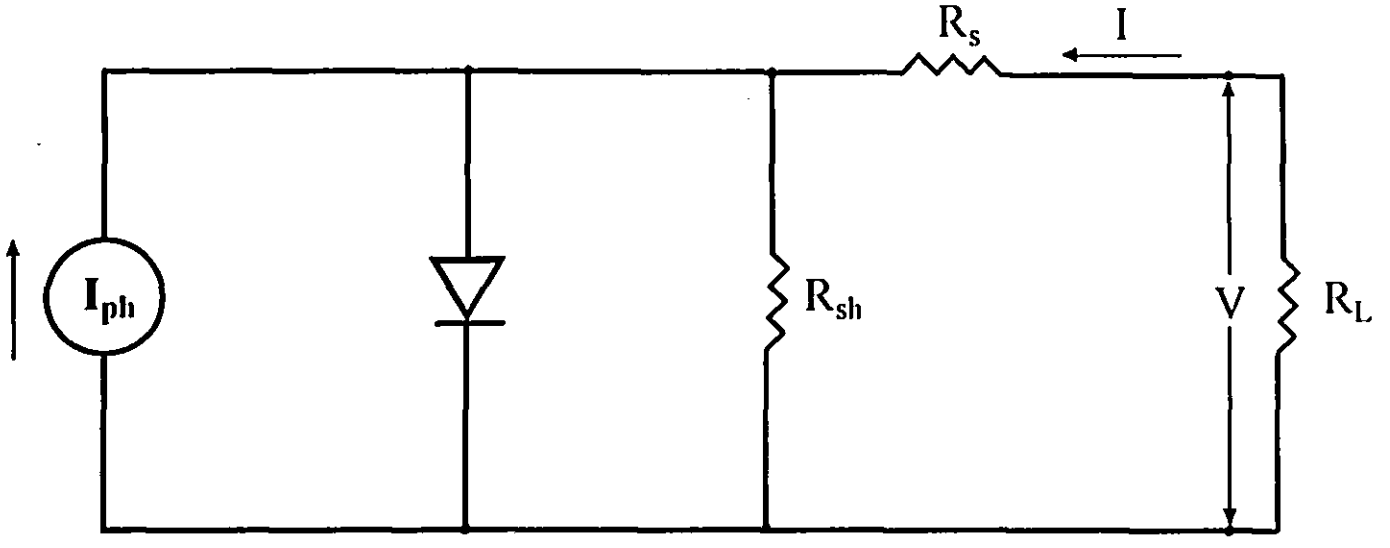


Fig. 2.6 Equivalent circuit of a p-n junction solar cell.

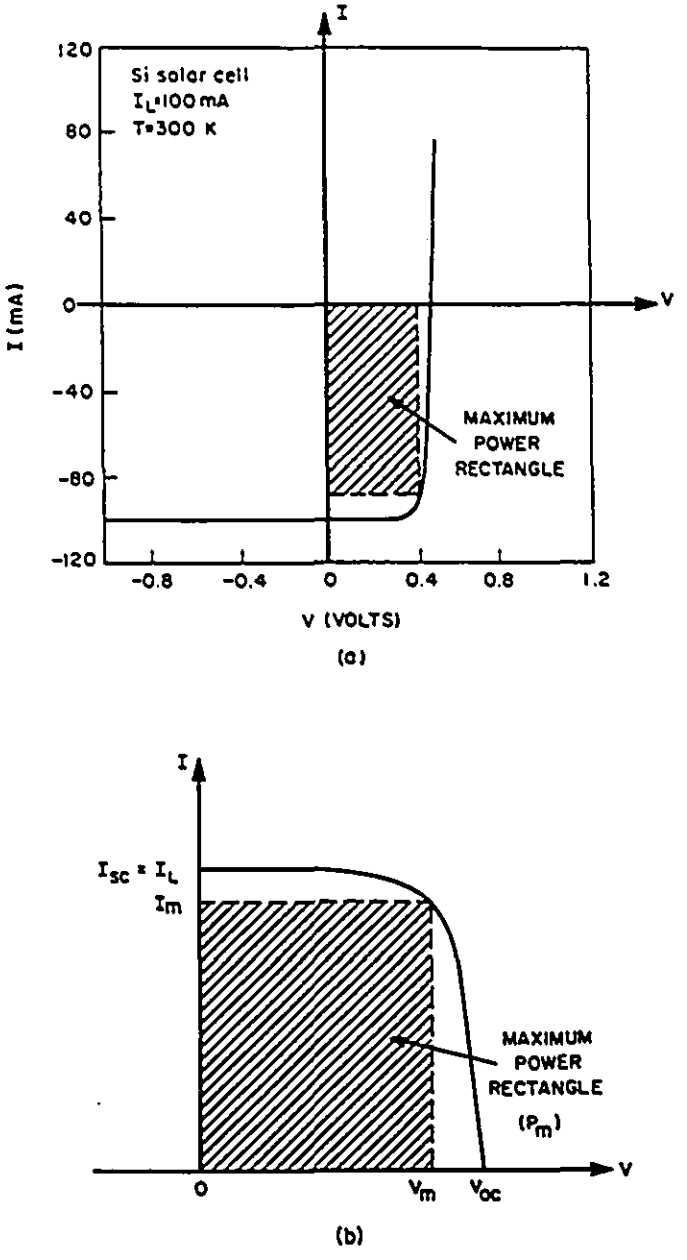
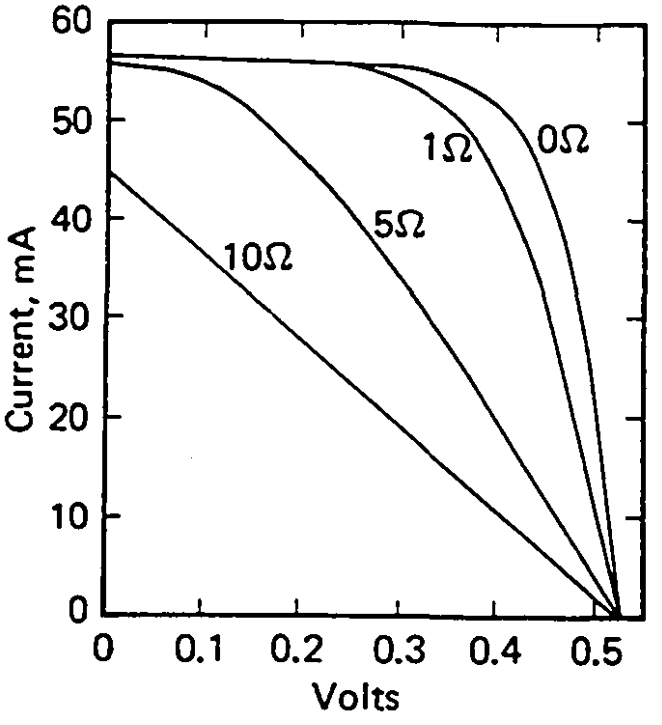


Fig. 2.7 (a) Current-voltage characteristics of a Si homojunction solar cell under illumination. (b) Inversion of (a) about the voltage axis. [2.8]

(a)



(b)

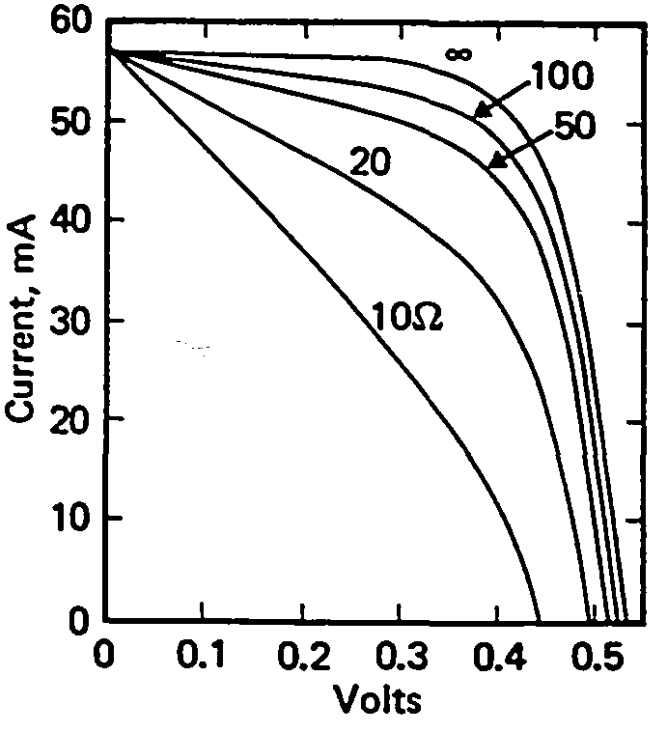


Fig. 2.8 (a) Effect of series resistance on the I-V characteristics of a solar cell. (b) Effect of shunt resistance. [2.9]

CHAPTER 3

GROWTH AND CHARACTERIZATION OF $CuInSe_2$ SINGLE CRYSTALS

3.1 Introduction

Large and good-quality single-crystal $CuInSe_2$ substrates are required for the fabrication of the ZnO/CdS/$CuInSe_2$(bulk) solar cells. A variety of methods have been reported for the growth of $CuInSe_2$ single crystals, but the Bridgman method [3.1-3.6], directional-freezing [3.7-3.11] and zone-melting [3.12,3.13] have been more commonly used. Growth experiments using the iodine-transport method [3.14], hydrothermal method [3.15] and open-crucible liquid-encapsulated Czochralski method [3.16] were also reported.

In the present work, a horizontal Bridgman method has been used for the growth of $CuInSe_2$ single crystals, although a vertical Bridgman system was also employed in the early stage of this work [3.4, 3.17-3.18]. The $CuInSe_2$ substrates used for cell fabrication were all grown by the horizontal Bridgman method. A one-ampoule process has been employed for the synthesis and growth of the compound. Ingots grown with this process were generally uniform in conductivity type and composition. Haupt and Hess [3.1] and Parkes et al. [3.12] reported the use of a two-ampoule methods, in which the synthesis and growth of $CuInSe_2$ were carried out in separate ampoules, resulting in ingots that were non-uniform in composition and conductivity type. The non-uniformity was probably caused by the loss of selenium from using a second ampoule for the growth because some selenium might have left behind in the first ampoule.

One of the greatest problems of the Bridgman growth of $CuInSe_2$ has been the adhesion of the ingot to the inner wall of the quartz ampoule after the growth. The adhesion not only induces cracks in the ingots and limits the size of the crystals but also creates other defects in the crystal structure. Several methods have been suggested to minimize this problem. These methods include degassing of the ampoule at a high temperature (about 1000 °C) in vacuum [3.19], roughening of the inner wall of the ampoule with alumina powder [3.3] and baking of the starting materials at a low temperature (about 100 °C) just prior to sealing the ampoule [3.20]. However, none of these methods was found to be very effective in avoiding the adhesion in the present work. A method has then been developed in this laboratory by introducing into the quartz ampoule a thick layer of carbon coating or a piece of solid graphite as a gettering agent and it was found to be very effective in avoiding the adhesion [3.21].

In this chapter, the crystal growth system and process, the adhesion problem and the characterizations of the crystals are described.

3.2 Horizontal Bridgman Growth of $CuInSe_2$

In the Bridgman method, the material to be grown is usually contained in an ampoule or a crucible. The ampoule is then passed through a stable temperature gradient, from temperatures above to temperatures below the melting point of the material. The starting materials for the growth are either polycrystals of the material to be grown or, in the case of a compound, constituents of the compound. If the starting materials are the constituent elements, they are allowed to react to form the compound before the crystal growth. The growth starts by bringing the ampoule to the high temperature zone of the furnace to let the starting materials melt and mix

for a certain period of time. The ampoule is then moved along the temperature gradient. The melt starts to solidify when it is passed through the melting point. With the right conditions, the melt crystallizes and single crystals can be obtained. In some cases, closed ampoules are required, especially for the growth of a material which is volatile or contains volatile components. Since selenium is highly volatile at elevated temperatures, closed ampoules are required for the growth of $CuInSe_2$.

3.2.1 Crystal Growth System

To provide the stable and appropriate conditions for the $CuInSe_2$ crystal growth experiments, a reliable horizontal crystal growth system had been assembled for the present work. A schematic diagram of this system is shown in Fig. 3.1. A Thermco MB-80 horizontal resistive furnace was used to provide the necessary temperature gradient for the growth experiments. It was a three-zone furnace with the central zone adjustable from 400 to 1400 °C and the end zones adjustable to ± 50 °C of the central-zone temperature. The furnace temperature could remain stable within ±1/4 °C. The growth chamber was a ceramic tube heated by the heating elements of the furnace and had an inner diameter of about 6 inches. During the growth, refractory materials and quartz wool were placed at the ends of the ceramic tube for insulation. The temperature profile of the furnace for the growth is shown in Fig. 3.2. The central zone was set at about 1100 °C for the growth.

In addition to a furnace, a pulling mechanism is required for passing the ampoule through the temperature gradient inside the furnace. In the present work, it was a home-made mechanism consisting of several parts as shown in Fig. 3.1. A dc motor and a gear system controlled the

horizontal movement of a platform on which an ac motor for rotation was seated. The ac motor was connected to a chuck into which the quartz rod joining the ampoule was clamped as in the diagram. In other words, the dc motor provided the horizontal movement of the ampoule for the growth process and the ac motor provided the rotational motion for mixing. The horizontal speed of the ampoule was adjustable from 1 mm/hr to more than 2 cm/hr by changing the voltage input to the dc motor. The rotational speed was fixed at about 15 rpm.

It should be noted that most experimental results reported in this thesis were obtained with $CuInSe_2$ samples grown by the horizontal Bridgman system, including all the results for the solar cell fabrication. Only the results of a few vertically-grown samples were reported for the etching experiments in section 3.4.4. Therefore, the vertical system will not be elaborated here, interested readers might refer to the references [3.4, 3.17-3.18] for details. However, similar crystal growth processes were used for the two systems.

3.2.2 Ampoule Preparation

In the crystal-growth experiments, a special step-shaped quartz ampoule was used, as shown in Fig. 3.3. Quartz tubes with an inner diameter of 12 mm and an outer diameter of 16 mm were used for the preparation of ampoules. First of all, one end of a quartz tube was closed and tapered into a conical shape using a H_2/O_2 torch. The purpose of the tapered end was to facilitate nucleation of the $CuInSe_2$ at the beginning of the crystal growth. The quartz tube was then bent into the desirable shape, usually a step-like shape. Following this, the quartz tube was cleaned thoroughly with soap, trichloroethylene and acetone to remove organic impurities and then soaked with aqua regia for 24 hours to remove any metallic impurities. It was next rinsed with

hot and cold de-ionized water for many times. After drying, the upper part, section B, of the ampoule was coated with a layer of carbon, as shown in Fig. 3.3, by the pyrolysis of acetone. Carbon coating was used because it was found to be effective in avoiding the adhesion of the $CuInSe_2$ ingot to the quartz ampoule after the crystal growth [3.21]. The carbon mainly acted as a gettering agent of some species, probably O_2 or H_2O, that could cause the adhesion. A more elaborated discussion of the adhesion problem will be presented in the next section.

The carbon coating was deposited in the following way. Small amount of acetone, CH_3COCH_3, was first introduced into the ampoule. The highly volatile acetone quickly vaporized and filled up the ampoule. By heating a localized region in the upper part of the ampoule with a torch, the acetone vapour decomposed by the action of heat into carbon and water vapour and a layer of carbon was formed and deposited locally at the region. The carbon-coating process was continued by applying heat to different regions of the upper part of the ampoule until the desired area was all covered with a layer of carbon. The ampoule was then carefully rinsed with acetone again to remove any loose carbon particles inside the ampoule. After the carbon coating, the ampoule, with the open end connected to a vacuum pump, was then baked at 1050 °C for 4 to 5 hours for outgassing. It was then ready to be charged with the starting materials.

The starting materials for the growth experiments were copper (6 9's), indium (5 9's) and selenium (5 9's) elements. The Cu was etched with diluted HNO_3 and the In with diluted HCl to remove the thin oxide layers covering the metal pellets. They were then rinsed with DI water followed by alcohol. The Se was used either as-received or rinsed with DI water and alcohol. After this, the lower part of the ampoule, section A in Fig. 3.3, was quickly charged with the starting materials weighed in stoichiometric proportions (Cu:In:Se=1:1:2). The total weight of the Cu, In and Se elements used was from 16 to 32 g. The ampoule was then pumped down to a

pressure of about 10^{-5} to 10^{-6} torr and sealed off with the H_2/O_2 torch. The newly sealed end of the ampoule was then connected to a quartz rod which, in turn, was fixed onto the horizontal pulling mechanism of the growth system for the growth experiment.

3.2.3 Crystal Growth

A one-ampoule method was used in the present work for the growth of $CuInSe_2$ crystal; whereas a two-ampoule method was used by other workers [3.1, 3.5, 3.12]. In the one-ampoule method, synthesis of the $CuInSe_2$ from the starting elements Cu, In and Se and crystal growth of the compound are carried out sequentially in the same ampoule. For the two-ampoule method, the synthesis of $CuInSe_2$ and the crystal growth take place in two separate ampoules. There are advantages of the one-ampoule method over the two-ampoule method. No breakage of vacuum and transfer of the compound to a second ampoule is required, reducing contamination and loss of materials.

A growth experiment started by pushing the ampoule into the furnace slowly from one end to the central zone of the furnace by the pulling mechanism. The temperature of the central zone of the furnace was set to 400 °C, which was the minimum adjustable temperature. However, it was observed that the reaction of the elements started slowly at about the melting point of In (156 °C) and turned vigorous at the melting point (217 °C) of Se, which has a very high vapour pressure beyond its melting point. In order to avoid ampoule cracking or even explosion, which occurred occasionally when the temperature of the ampoule was increased too rapidly [3.17] during the synthesis or reaction stage, the ampoule was placed at the end zone of the furnace where the temperature was below 150 °C. The ampoule was then pushed into the furnace slowly

at about 2 cm/h, giving a temperature increasing rate of the ampoule not more than 20 °C/h. Using such a procedure, cracking or explosion of the ampoule has not been observed.

After the ampoule reached the central region of the furnace, most of the starting materials had reacted to form the $CuInSe_2$ compound and the temperature of the furnace was raised quickly at a rate of about 100 °C/h to 1100 °C. The melting point of $CuInSe_2$ is 986 °C. The $CuInSe_2$ melt was then mixed either by rotating the ampoule for several hours using the rotation motor or by agitating the ampoule manually to prevent the melt to come into contact with the carbon coating. After the mixing, the growth was started by withdrawing the ampoule at a rate of 1 to 10 mm/h. Most of the samples were grown with a rate of 10 mm/h because a slower rate had not been found to yield crystals with higher quality. After the ampoule was pulled to the region with a temperature below the low-phase-transition temperature (665 °C)* [3.22], the temperature of the furnace was decreased at 50 °C/h to the minimum adjustable temperature of the furnace and then the furnace was turned off. Fig. 3.4 shows a photograph of an ingot inside an ampoule after the growth experiment. Using this procedure, ingots containing large $CuInSe_2$ grains from several millimeters to up to 2 centimeters a side were routinely obtained.

3.3 Adhesion Problem

One of the main difficulties encountered in growing $CuInSe_2$ crystals is the adhesion of the ingot to the quartz ampoule after the growth. To tackle this problem, carbon coating was first investigated in the present work as a barrier layer between the quartz ampoule and the $CuInSe_2$ by depositing the coating onto the inner wall of the whole ampoule. The idea behind this was to

* This phase transition was not observed by other workers. However, another confirmed phase transition is at 810 °C [3.22].

prevent the $CuInSe_2$ melt from making contact with the ampoule because it was speculated that the $CuInSe_2$ melt reacted with the quartz ampoule during the crystal growth. It was found that a thick layer of carbon deposited by pyrolysis of acetone was indeed capable of avoiding the adhesion, but a thin layer was ineffective. However, parts of the carbon coating were occasionally detached from the ampoule wall after the growth and the carbon would sometimes incorporate into the $CuInSe_2$ ingots. In the runs with mixing by rotating the ampoule, the peeling off of the coating was even more severe. An ingot contaminated by carbon is shown in Fig. 3.5 (a). It should be noted that the carbon contamination appeared only on the free surface of the ingot because those detached carbon particles floated on the $CuInSe_2$ melt during the growth and locked into the ingots after the $CuInSe_2$ melt had solidified. Although the elimination of the adhesion resulted in improvements of the quality of the $CuInSe_2$ ingots with less cracks and defects and generally larger $CuInSe_2$ grain size, severe carbon contamination could limit the grain size.

Another observation was that after the peeling off of the carbon coating, the $CuInSe_2$ was in direct contact with the quartz ampoule and yet there was no adhesion. This indicates that $CuInSe_2$ itself may not react with quartz. It is possible that the presence of carbon eliminated some substances, probably at high temperatures, that were causing the adhesion. In order to prove this, several experiments were carried out. Some ampoules were made with the carbon coating only covering the upper part, section B, of the ampoule, as shown earlier in Fig. 3.3. The $CuInSe_2$, in section A, had no contact with the carbon coating, but in direct contact with the quartz ampoule wall throughout the experiment. The mechanical mixing was replaced by a high temperature soaking, i.e. the ampoule was maintained at the same temperature for the same period of time but without the rotational mixing, to avoid any contact of the melt with the carbon

coating. Using such an arrangement the adhesion was also absent in such ampoules; whereas, under the same conditions but without the carbon, adhesion was always present. An experiment with an extended period (48 hr) of high temperature soaking was also carried out, using a partially coated ampoule, and no adhesion was found. These results present strong evidence that $CuInSe_2$ itself does not react with quartz because the material was in direct contact with the quartz ampoule throughout the experiment, yet no adhesion was found. Some substances that could be absorbed by carbon, however, might be the culprit of the adhesion problem.

Since oxygen or water vapour are the most common contaminants in such experiments, it is speculated that some oxygen-related compounds caused the sticking. Furthermore, carbon is a very effective agent for reducing oxygen, metal oxides or water vapour at high temperatures, it is likely that the adhesion was eliminated by the gettering action of carbon on the oxygen or oxides inside the ampoule. Therefore, even when the carbon was not forming a barrier between the $CuInSe_2$ and the ampoule, the ingot did not react and stick to the ampoule. Oxygen was also suspected by Yasuda et al. [3.23] for causing the adhesion problem of CdTe.

Several materials are also well known for reducing oxygen and oxides effectively, molybdenum and titanium being two of them. Two growth runs were also carried out using molybdenum and titanium as the gettering agents of oxygen. Care was taken in both cases to avoid any contact between the melt and the molybdenum or titanium during the experiments. The other experimental conditions were kept the same as before. It was found that the ampoule with a piece of titanium wire was free of adhesion, although some reaction had apparently taken place on the titanium surface. The ampoule with a piece of molybdenum sheet showed a little amount of sticking, but to ã much smaller extent than without any gettering agent. Reaction on the molybdenum was much stronger than on the titanium. It is apparent that these two materials are

not suitable gettering agents in the present case because of their reactions with and possibly contamination to the $CuInSe_2$. These results, however, provide stronger evidence that oxygen or some oxides could be the culprit causing the adhesion problem.

Solid graphite was also found to be a suitable gettering agent and a piece of solid graphite as small as 0.1 g was able to avoid ampoule adhesion. There are other advantages of using solid graphite as the gettering agent. First of all, it is much easier to prepare than carbon coating, just by cutting and cleaning. Secondly, the $CuInSe_2$ melt can be mixed by rotating the ampoule but with minimum carbon contamination. Although the $CuInSe_2$ melt comes into contact during the mixing, carbon particles detached from the solid graphite are minimal and do not seem to affect the crystal quality. For partially carbon-coated ampoule, the $CuInSe_2$ melt can only be mixed by agitating the ampoule manually to avoid the carbon coating from detaching by mechanical mixing. Therefore, solid graphite was used for most of the later growth experiments. An ingot grown with a partially coated ampoule is shown in Fig. 3.5 (b). No sticking or carbon contamination was observed for this ingot. A layer of boron nitride was also reported to be effective in avoiding adhesion of $CuInSe_2$ ingots to the quartz ampoules [3.24].

Another set of experiments was carried out [3.25] to determine the source of this contaminant or sticking agent, presumed to be oxygen or some oxides. In these experiments, specially made vacuum-sealed ampoules consisting of three sections A, B and C as shown in Fig. 3.6 were used. In this ampoule, section C was charged with the Cu, In and Se pellets, section B was coated with a thick layer of carbon internally, and section A was left empty. During the experiment, section B and section A were inserted into a furnace with temperature set at 1100 °C and heated for three days, while section C was immersed in a water bath to minimize the heating of the pellets inside. After this high temperature baking, the pellets in section C were poured into

section A and section A was sealed off and separated from sections B and C. The ampoule, now still under vacuum and consisting of section A and the Cu, In and Se pellets but without any carbon inside, was put through the same crystal growth process. Ingots grown in these experiments were always found to stick to the ampoules firmly. These results showed that the sticking agent was not from the quartz ampoule; otherwise, the sticking agent would have been reduced by the carbon before section A was separated from sections B and C.

The experiment was repeated with a two-section ampoule as shown in Fig. 3.3. With the pellet charge and the carbon coating in the same ampoule but different sections of it, the ampoule was heated slowly to 1100 °C and maintained at this temperature for two hours. It was then quickly withdrawn from the furnace and the charged section, section A, was then sealed off and separated from the carbon coated section B. The ampoule, now consisting of section A and the reacted charge but without any carbon inside, was then put through the crystal growth process. Ingots grown in these experiments were found to be free of any adhesion to the ampoule wall, indicating the sticking agent was present on the starting materials and was removed at high temperatures by the carbon in section B before section A was separated from it. In other words, the gettering action was on the charge rather than on the on the quartz ampoule. Recently, Shukri and Champness [3.26] reported the sticking agent, identified as oxygen, originated from the copper pellets and the use of oxygen-free copper might eliminate the need of a gettering agent for the growth of adhesion-free $CuInSe_2$ ingots.

3.4 Characterization of $CuInSe_2$ Single Crystals

3.4.1 Hot-point Probe and Hall-effect Measurements

The conductivity type of the samples was examined by hot-point probe. Almost all of the $CuInSe_2$ ingots grown in the present work using the one-ampoule method were uniformly p-type with an exception of a few ingots which also showed a small region of n-type conductivity. This uniformity in conductivity was in agreement with the result obtained in earlier work in this laboratory [3.3, 3.4]. However, the as-grown ingots prepared by several workers using the two-ampoule method were reported to be partially n-type [3.1, 3.12], probably the result of the loss of some selenium using the two-ampoule method. $CuInSe_2$ crystals with a deficiency of Se was reported to be n-type [3.27].

Hall-effect measurements were also carried out to obtain the mobility, resistivity and carrier concentration of the crystals, and the results of the measurements are summarized for five samples in Table 3.1. The results were similar to the ones obtained with the vertical Bridgman system [3.17]. The van der Pauw method was employed for the Hall-effect measurements to facilitate the measurements of irregular-shaped samples. The mobility values of the samples were found to be a little bit larger than the values reported in the literature [3.1,3.10,3.28-3.29]. Results of the measurements also confirms the p-type conductivity of the crystals.

3.4.2 Powder X-ray Diffraction

It is well known that a crystal behaves as a three-dimensional diffraction grating for X-rays. The diffraction can be considered as the scattering of X-rays by the lattice points in the

crystal as shown in Fig. 3.7 (a). The monochromatic X-rays scattered off adjacent lattice planes (Fig. 3.7 (b)) are in phase if their path difference is an integral number of the X-ray wavelengths, as described by the Bragg's law,

$$2d\sin\Theta = n\lambda, \qquad (3.1)$$

where d is the spacing of the lattice planes, θ is the incident angle of the X-rays, n is an integer and λ is the wavelength of the monochromatic X-rays. When the Bragg's law is satisfied, the intensity of the diffracted X-rays reaches a maximum due to constructive interference. It should be noted that the X-ray beam is deflected through an angle 2θ by the diffraction as shown in Fig. 3.7 (b). The diffracted X-ray beam should then be measured at this angle as shown in Fig. 3.8. In the powder X-ray diffraction method, the sample is in the form of many tiny crystalline grains with random orientation. For a given set of lattice planes, there are bound to be some crystalline grains oriented with this set of planes parallel to the incident plane (Fig. 3.8) and making an angle θ with the incident X-ray beam. A diffraction maximum will be recorded by the detector if the angle θ is the Bragg angle for this set of planes. By changing the angle θ, diffraction maxima for different sets of lattice planes will be recorded at different values of θ. These values and the corresponding lattice spacings are characteristic for a material with a particular crystal structure and are usually documented in the *American Society for the Testing and Materials* (ASTM) data. By comparing the powder diffraction pattern of a sample with the ASTM data, the crystal structure of the sample can be identified. The powder X-ray diffraction method can, of course, also be used to determine the lattice spacings of novel materials and the preferred orientation of thin-film samples.

Samples were selected randomly from several $CuInSe_2$ ingots and then ground to fine powder to be examined by powder X-ray diffraction method. The experiments were carried out in a Siemens model D500 diffractometer system with a Cu Kα radiation (wavelength 1.54 Å).

Earlier work by this author showed that a large excess of Cu in the starting materials resulted in extra phases, such as Cu_4In, in the ingot and these extra phases were detectable by powder X-ray detection and Electron Probe Microanalysis (EPMA) [3.30]. However, such extra phases are not expected to be present in the present case with a stoichiometric starting proportions of the elements. A typical powder diffraction pattern of one of the samples is shown in Fig. 3.9. Every peak or diffraction maximum in the pattern can be identified with a plane given in the ASTM data for $CuInSe_2$ with the chalcopyrite structure. It is safe to say that the samples prepared in the present work were crystals of $CuInSe_2$ with the stable chalcopyrite phase.

3.4.3 Electron Probe Microanalysis

Several ingots were examined by wavelength-dispersive electron probe microanalysis (EPMA) for the determination of composition. The sample to be examined was loaded into a vacuum chamber pumped down to about 10^{-6} torr. The sample was then bombarded by an electron beam (current 10 nA and accelerating voltage 15 kV) and the corresponding X-ray emission was analyzed by a CAMECA Analyzer. In principle, the emitted X-rays should have wavelengths characteristic of the elements composing the sample, leading to elemental identification. Furthermore, the intensities of these characteristic X-rays can be compared to the intensities of known standard samples (Cu, In and Se standards in this case) to obtain the amount of each element in the sample.

Table 3.2 shows the results of the analyses for 5 ingots. The measured composition was an average over 10 points on an ingot. The compositions of different ingots were generally not the same, although they were grown under the same conditions. However, the difference was not big and usually within 2 atomic percent . It is speculated that small variations in temperature,

growth speed and position of ampoule inside the furnace were a few of the factors affecting the final composition of the ingot. Composition was then measured along and across several uniformly p-type ingots. The results of one of the ingots, LS-13, are shown in Fig. 3.10. It can be seen that the composition is quite uniform along and across the ingot. The compositional uniformity should lead to uniform properties of the crystals in the same ingot. Similar results were found in other ingots. In other words, although composition might vary from ingot to ingot, the composition inside an ingot were generally quite uniform.

Two of the ingots, LS-7 and LS-12, with an n region were also examined by EPMA. It was found that the composition within each of the n or p region was uniform but the compositions of the two regions were different as can be seen in the Table 3.2. The n region had a smaller Cu/In ratio than the p region which seems to agree, at least in the same ingot, with the common belief that Cu-deficient $CuInSe_2$ is usually n-type. However, by simply looking at the Cu/In ratio, one cannot predict the conductivity type of the sample because the Se content is also playing a role in determining the conductivity type. Crystal growth of $CuInSe_2$ with nonstoichiometric starting proportions of the elements were also carried out earlier by this author [3.30, 3.31] using a vertical Bridgman system. It was reported that despite the large variation of starting proportions, the final compositions of the ingots determined by EPMA tended to converge into a certain compositional range. Within this range, only a small region gave rise to n-type $CuInSe_2$. The samples in the present work seem to agree with those results although two points fall very close to the margin of the compositional range.

3.4.4 Chemical Etching

Etching experiments were carried out to determine a suitable etch for $CuInSe_2$ single crystals. Several etches were reported for $CuInSe_2$. Wagner et al. [1.4] were the first to report the use of aqua regia, $HCl+HNO_3$ (3:1 by vol.), for the $CuInSe_2$ single-crystal substrates in their photovoltaic detectors. A similar etch, $HCl+HNO_3$ (1:1 by vol.), was also used in several other single-crystal $CuInSe_2$ devices [1.8-1.10,3.11]. This etch was found, in the present case, to be too strong and resulted in stained surfaces even in very diluted form. Yakusev et al. [3.32] also reported this etch would give Cu and In deficiencies for $CuInSe_2$ surfaces. Therefore, $HCl+HNO_3$-based etches have seldom been used for more recent single-crystal $CuInSe_2$ studies.

A mixture consisting of $K_2Cr_2O_7$ and H_2SO_4 (1:9 by weight) at room temperature was also used by several workers [3.32-3.34]. Little or no change in the near-surface composition was reported for periods up to 45 minutes using this etch [3.32], although stronger solutions could lead to compositional changes at the surface. Etching experiments were carried out on cleaved and mechanically-polished $CuInSe_2$ surfaces using this solution. Etching on mechanically-polished might reveal features that are not intrinsic to the surface because of the defects created by polishing. However, the etching results on mechanically-polished surfaces were important because polishing was required for device fabrication in the present work.

Ingots were cleaved and orientation of the cleaved planes were determined by both Laue X-ray diffraction and X-ray diffractometry. Although it was reported that $CuInSe_2$ cleaved easily along the (110) plane [3.35], most of the ingots grown in the present work with the horizontal furnace cleaved on the (101) plane and occasionally on the (112) plane but seldom on the (110) plane. It should be noted that the (101) orientation is not equivalent to the (110) plane because

$CuInSe_2$ has a chalcopyrite structure in which the lattice constant c is almost twice the value of the lattice constant a. However, it is interesting to find that several samples grown with the vertical Bridgman system cleaved on the (110) plane [3.36]. Some of these (112), (101) and (110) surfaces were mechanically polished for the investigation of polishing effect on the $CuInSe_2$ surfaces.

Etching on the polished (112) plane revealed a rough surface with tiny irregular-shaped etch pits even after only a short period time (less than one minute). Large triangular etch pits also started to appear after less than one minute of etching. A photograph of such a surface after a five-minute etching is shown in Fig. 3.11. Etching on cleaved (112) plane remained smooth for couple of minutes and triangular etch pits started to appear by further etching. The surface was smoother with much less tiny etch pits than the mechanically-polished surface. The number of the large triangular etch pits continued to increase with etching time with no sign of saturation until the whole surface was covered with them, indicating that they were not resulted from crystal defects. It is evident that the large triangular etch pits were intrinsic to the (112) and probably the results of preferential etching by the $K_2Cr_2O_7+H_2SO_4$ solution for this particular orientation. The tiny etch pits should be the results of surface defects created by polishing. These defects were etched away much faster than the rest of the surface because it is known that many etches attack "weak" points such as defects more easily. Experiments on (110) surfaces showed similar results except that preferential etching created sector-shapes etch pits as shown in Fig. 3.12. Etching experiments on cleaved (101) planes revealed no etch pits even after two hours of etching although material could be seen to have been etched away on the surface, indicating the lack of preferential etching on this orientation. Therefore, it seems that the $K_2Cr_2O_7+H_2SO_4$ solution can be used for chemical polishing on the (101) planes because it etches the crystal homogeneously.

However, the preferential etching of this solution in certain crystal orientations make it not very suitable for the surface preparation of $CuInSe_2$ for device fabrication.

Another commonly-used etch for single-crystal $CuInSe_2$ is a bromine+methanol (brome-methanol) solution. It has been used for ohmic-contact studies [3.37, 3.38], surface studies [1.11, 3.39] and device fabrication [1.6]. Moons et al. [3.37] reported the capability of this etch to remove the mechanical damage after polishing. However, solutions with a high concentration of bromine (> 2% by vol.) were reported to deplete the surface from copper [1.6, 3.37]. On the contrary, solutions with a low concentration of Br (< 1% by vol.) did not show any change in surface composition [3.32, 3.38]. Experimental results in the present work showed that this solution etched relatively faster than the $K_2Cr_2O_7$+H_2SO_4 solution, although etching rates were not obtained quantitatively.

A solution with a Br concentration larger than 2 % would sometimes result in stained surfaces after only a short period of etching time. Using a solution with a low Br concentration (< 1% by vol.), polished surfaces usually remained smooth for more than two minutes of etching, although tiny irregular-shaped etch pits as observed on polished surface etched with the $K_2Cr_2O_7$+H_2SO_4 solution started to appear by further etching. Another observation was that no preferential etching occurred, i.e. no large regular-shaped etch pits was observed, in all orientation even after prolonged etching. Considering the faster etch rate of the brome-methanol solution and the later appearance of the defect-related etch pits, it seems that this etch does not attack the surface defects much faster than the rest of the surface as in the case for the $K_2Cr_2O_7$+H_2SO_4 solution.

Taken into the account also the non-preferential etching by the brome-methanol solution, it is clear that this solution is a more suitable etch for $CuInSe_2$ surface preparation for device fabrication. This solution seems to be able to etch a mechanically-polished surface more homogeneously than any other etches. Therefore, this etch, usually with a 0.5 % Br concentration, was used exclusively for $CuInSe_2$ solar-cell fabrication in the present work. It is apparent than even the brome-methanol solution cannot remove completely all the surface defects on a polished $CuInSe_2$ surface, but it is, for the time, the only etch that can remove the largest thickness of the damage layer without revealing etch pits that might degrade the solar-cell performance.

Cleaved surfaces remained smooth for more than 30 minutes of etching with the brome-methanol solution without showing any of the tiny etch pits as on polished surfaces, further confirming that the tiny etch pits were locations of defects created by mechanical polishing. Again, preferential etch pits were not observed on any orientation.

3.5 Conclusions

Ingots of $CuInSe_2$ have been grown by a horizontal Bridgman method with a stoichiometric starting proportions of the elements. Using a gettering agent such as carbon coating or solid graphite in specially made ampoule, adhesion of the ingots to the quartz ampoule and carbon contamination were avoided. Void-free and microcrack-free single-crystal $CuInSe_2$ grains of several millimeters to up to two centimeters on a side have obtained. Almost all the ingots were found to be uniformly p-type with a carrier concentration of about 10^{17} cm^{-3}. Powder X-ray diffraction showed that the $CuInSe_2$ sample had a stable chalcopyrite structure.

Composition was found to be uniform along and across an ingot. A $K_2Cr_2O_7+H_2SO_4$ (1:9) solution was capable of revealing defect-related etch pits in additional to preferential etch pits in (112) and (110) crystal orientation. However, a brome-methanol solution was found to be more suitable for etching the $CuInSe_2$ surface for device fabrication. It is because this solution can etch the $CuInSe_2$ surfaces more homogeneously and remove mechanically-damaged layer more effectively than any other etches.

Table 3.1 Results of Hall-effect Measurements

Sample No.	Conductivity Type	Mobility (cm^2/V-s)	Carrier Conc. (cm^{-3})	Resistivity (Ω-cm)
LS-43	p	35	$8.9x10^{16}$	2.0
LS-51	p	30	$2.7x10^{17}$	0.77
LS-52	p	75	$1.9x10^{17}$	0.44
LS-53	p	41	$1.2x10^{17}$	1.27
LS-54	n	56	$1.5x10^{17}$	0.75

Table 3.2 Measured compositions of some $CuInSe_2$ samples by EPMA

Sample no.	Conductivity type	Measured Composition (at. %) Cu	In	Se	Cu/In ratio
LS-7	p	27.3	25.0	47.7	1.09
LS-9	p	26.1	25.4	48.5	1.03
LS-12	p	27.5	24.9	47.6	1.10
LS-13	p	27.5	24.9	47.6	1.10
LS-16	p	25.7	25.7	48.6	1.00
LS-7	n	25.5	25.7	48.8	0.99
LS-12	n	26.5	25.2	48.3	1.05

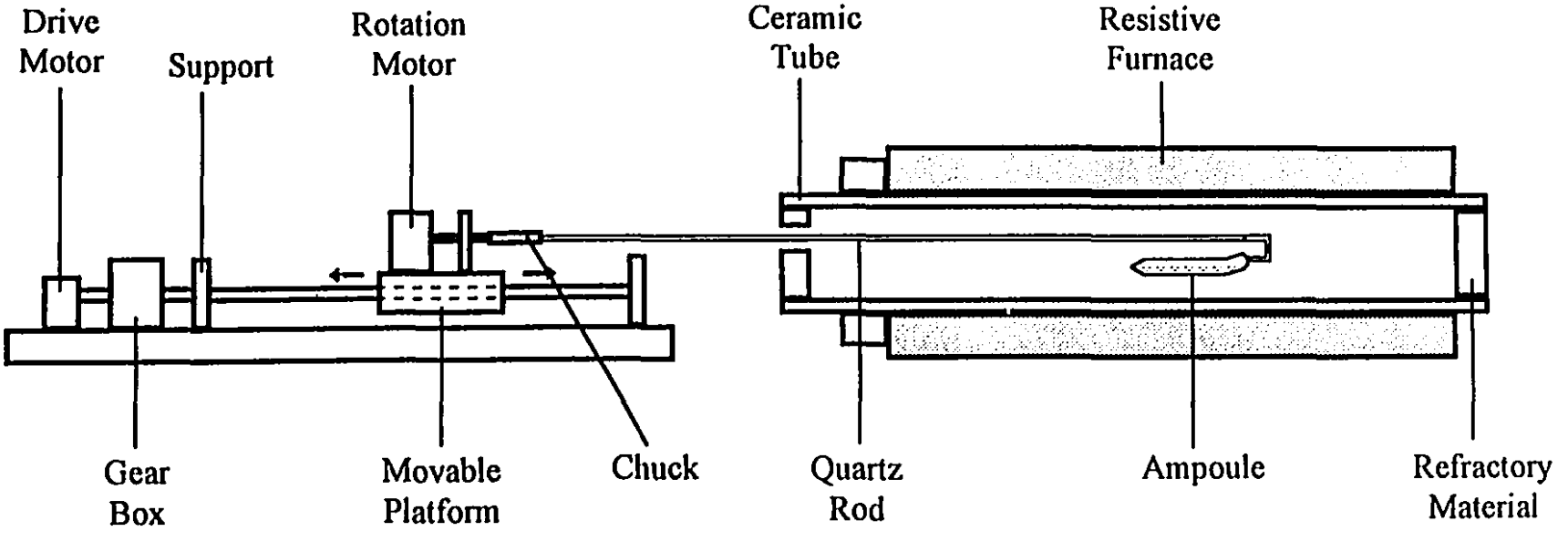


Fig. 3.1 Schematic of the horizontal Bridgman system for $CuInSe_2$ crystal growth.

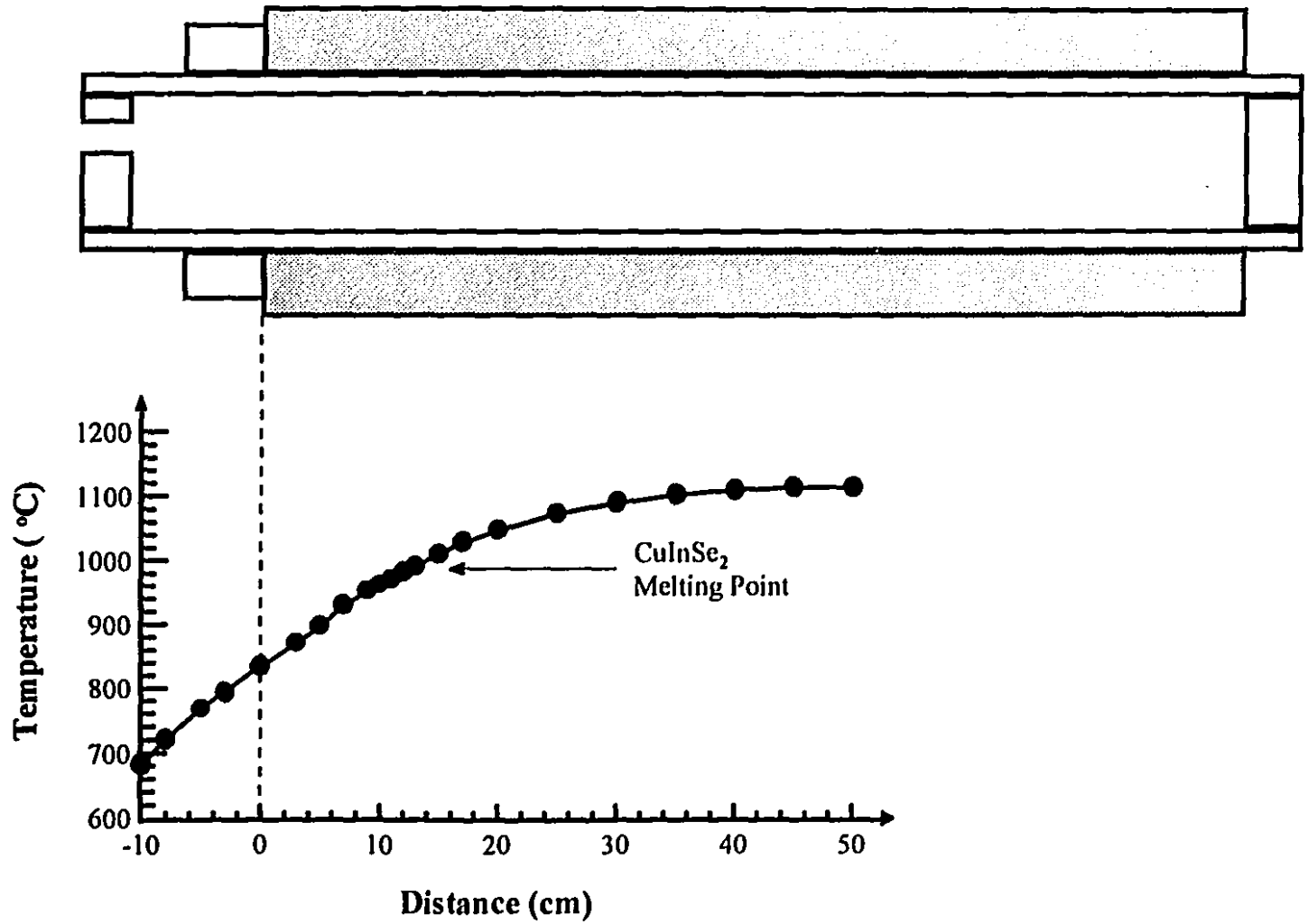


Fig. 3.2 Temperature profile of the furnace.

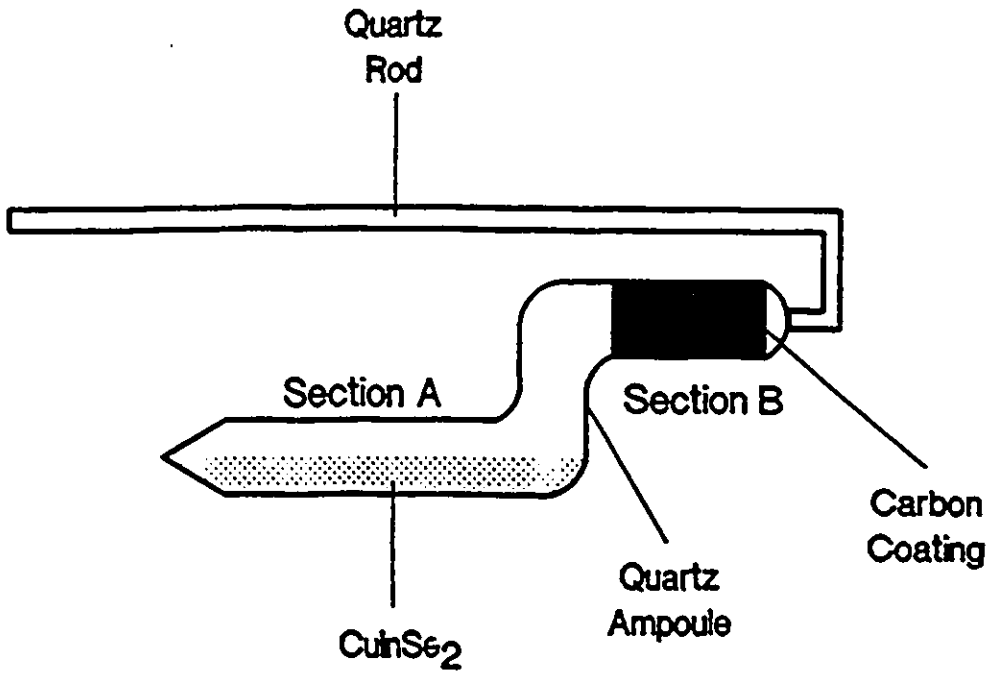


Fig. 3.3 Step-shaped quartz ampoule used in $CuInSe_2$ crystal-growth experiment.

Fig. 3.4 A $CuInSe_2$ ingot inside the quartz ampoule after the growth experiment.

(a)

(b)

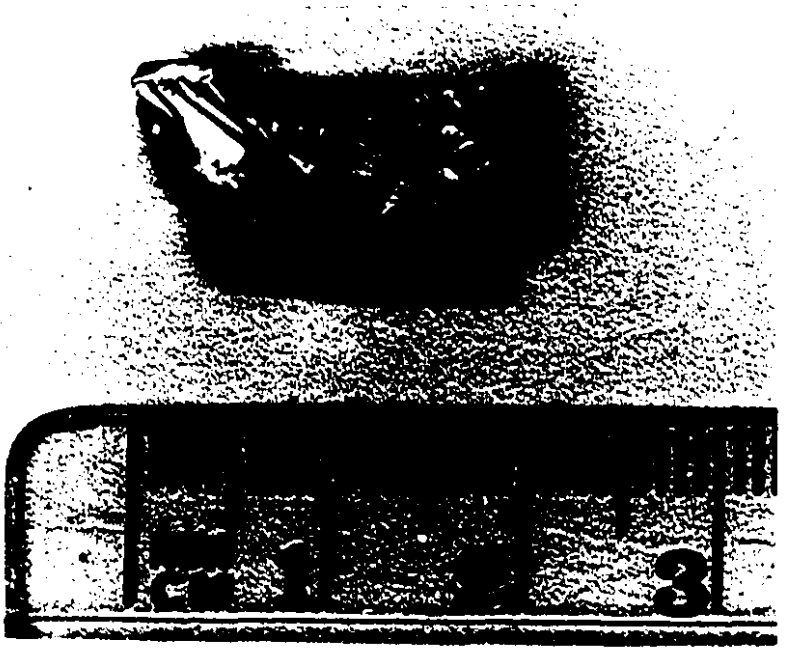


Fig. 3.5 (a) An ingot of $CuInSe_2$ contaminated by carbon detached from inner ampoule wall. (b) A monocrystal of $CuInSe_2$ grown with a partially carbon-coated ampoule.

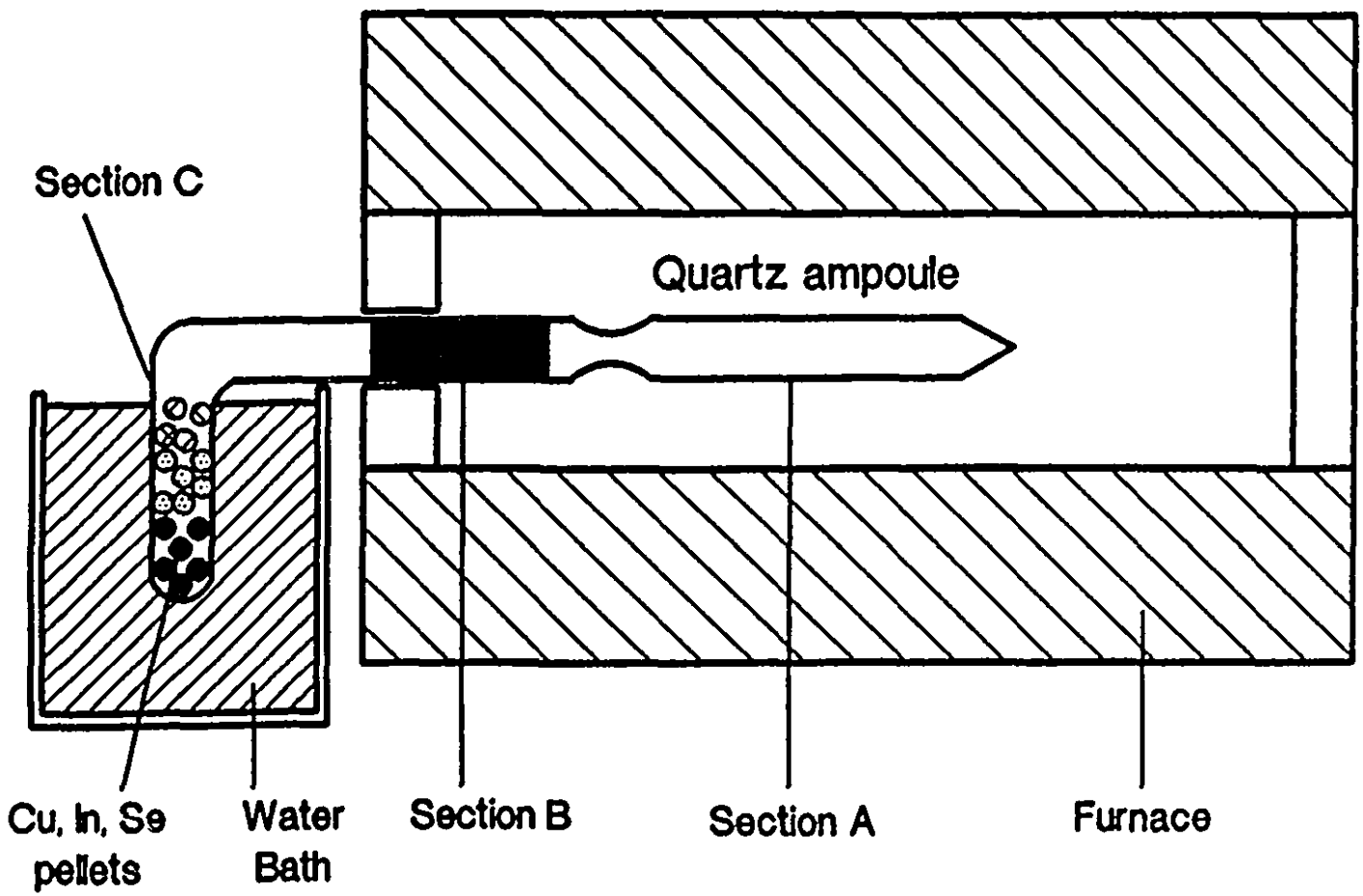
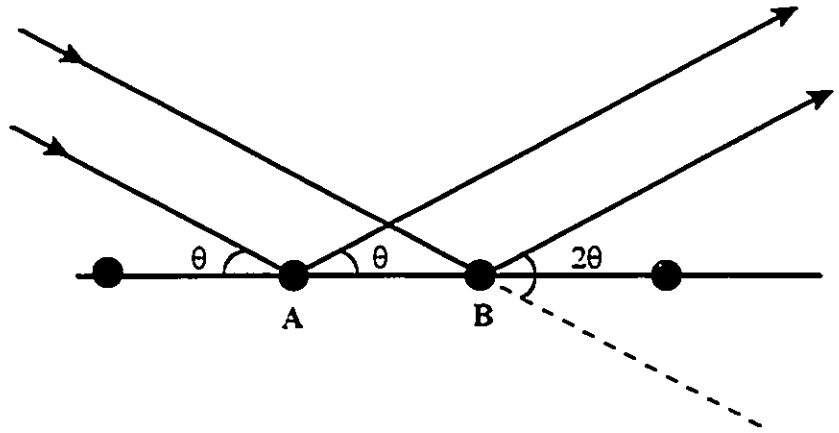
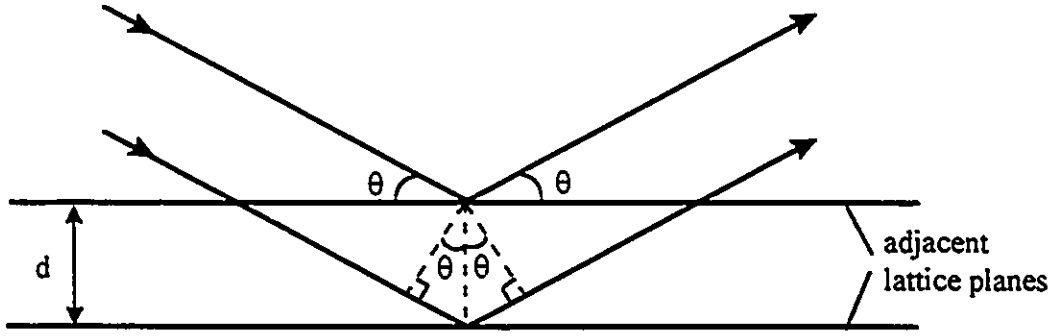


Fig. 3.6 High temperature bake of a three-section ampoule in the experiment to determine the source of the sticking agent.



(a)



(b)

Fig. 3.7 (a) Scattering of X-rays from the adjacent lattice points A and B in a lattice plane. (b) Scattering of X-rays off adjacent lattice planes. The path difference is $2d\sin\theta$.

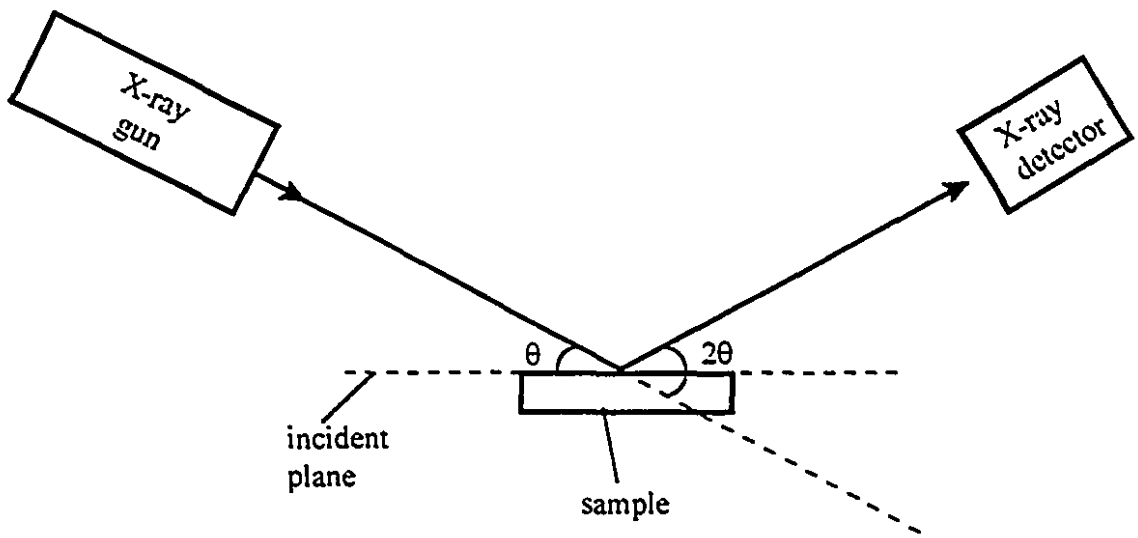


Fig. 3.8 A schematic diagram of the X-ray diffraction set up.

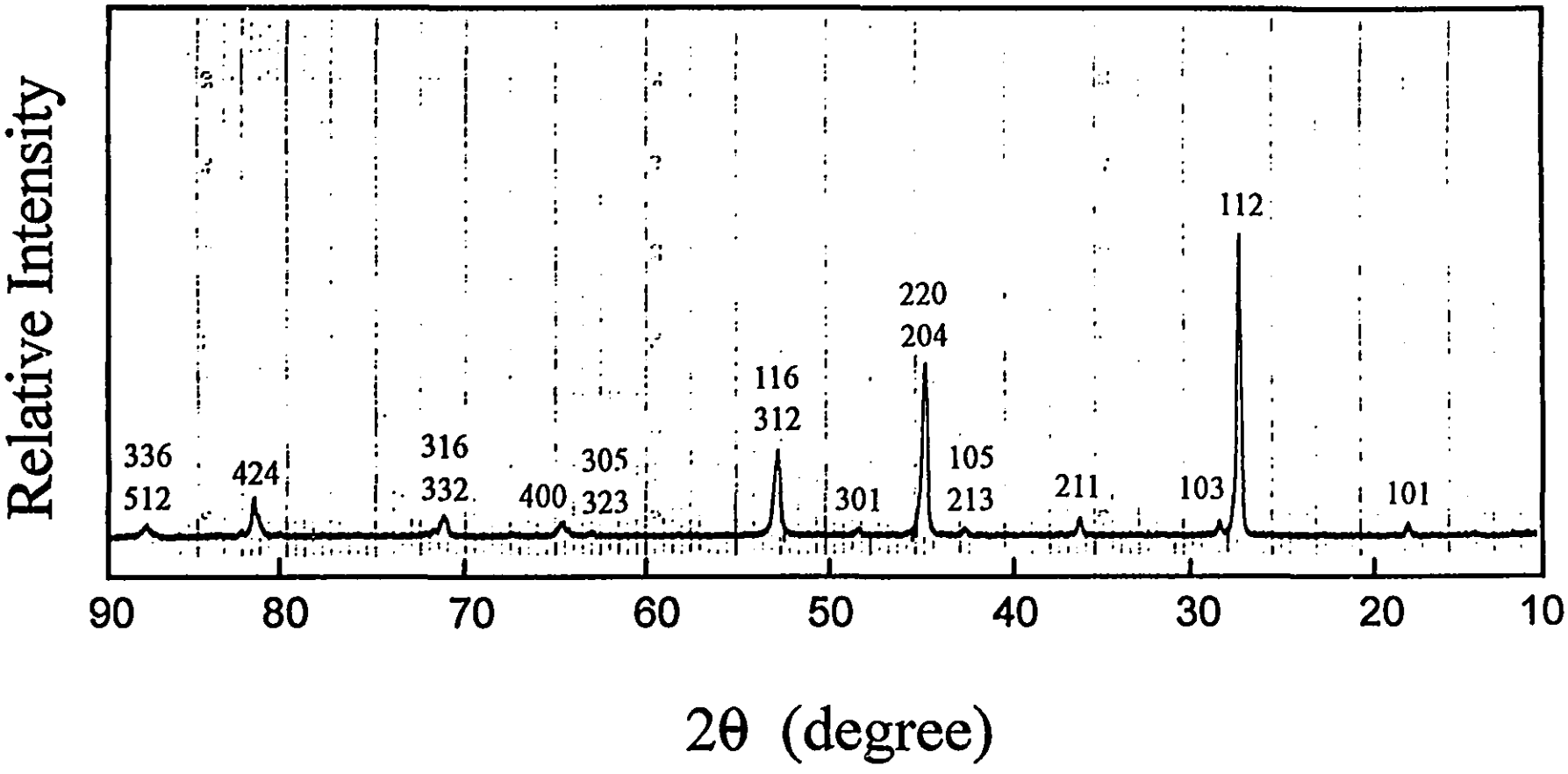


Fig 3.9 X-ray powder diffraction pattern of a $CuInSe_2$ sample.

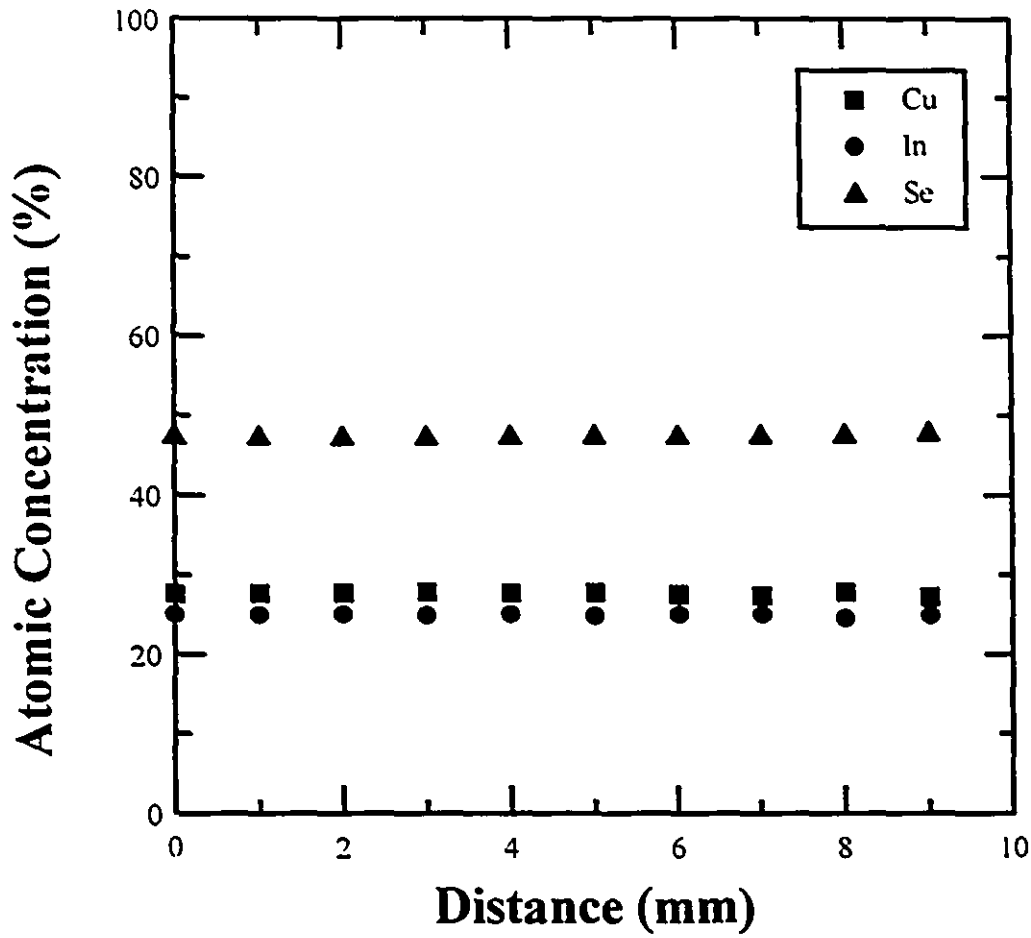


Fig. 3.10 (a) Measured composition as a function of distance across the growth plane of the ingot LS-13.

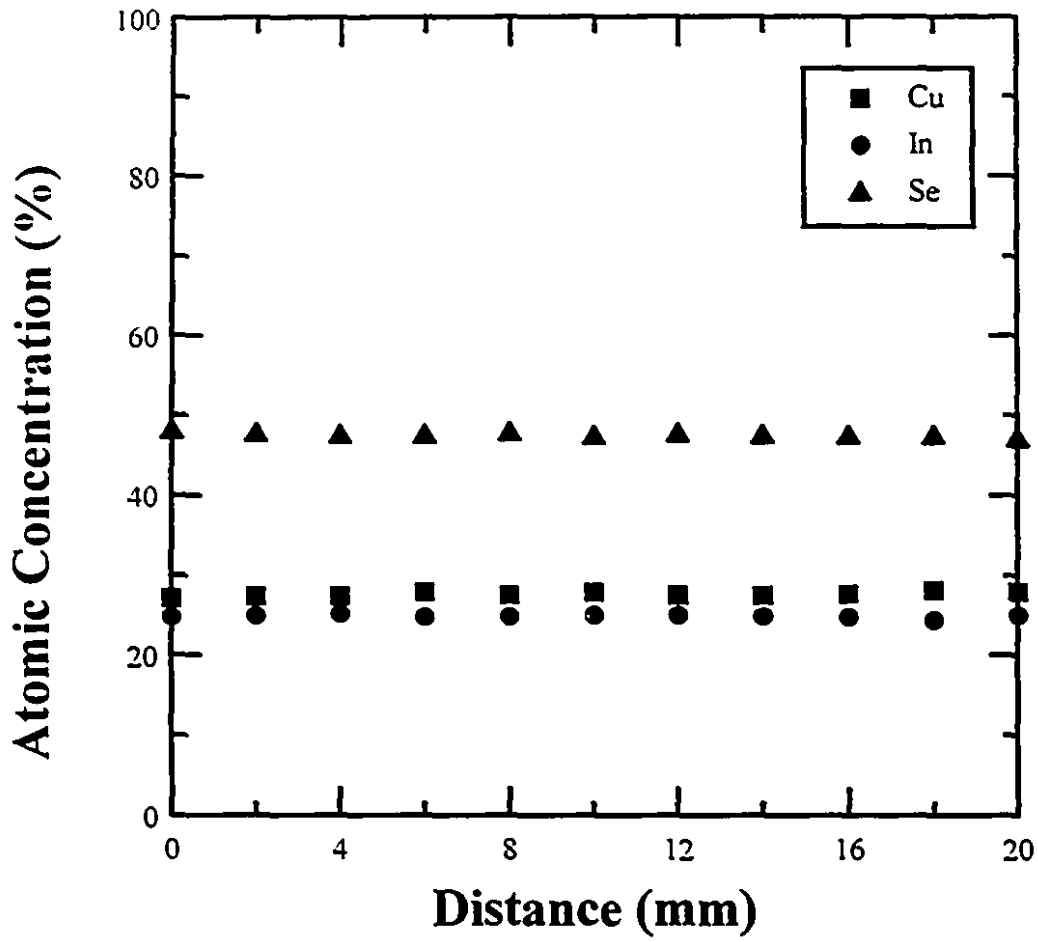


Fig. 3.10 (b) Measured composition as a function of distance along the growth direction of the ingot LS-13.

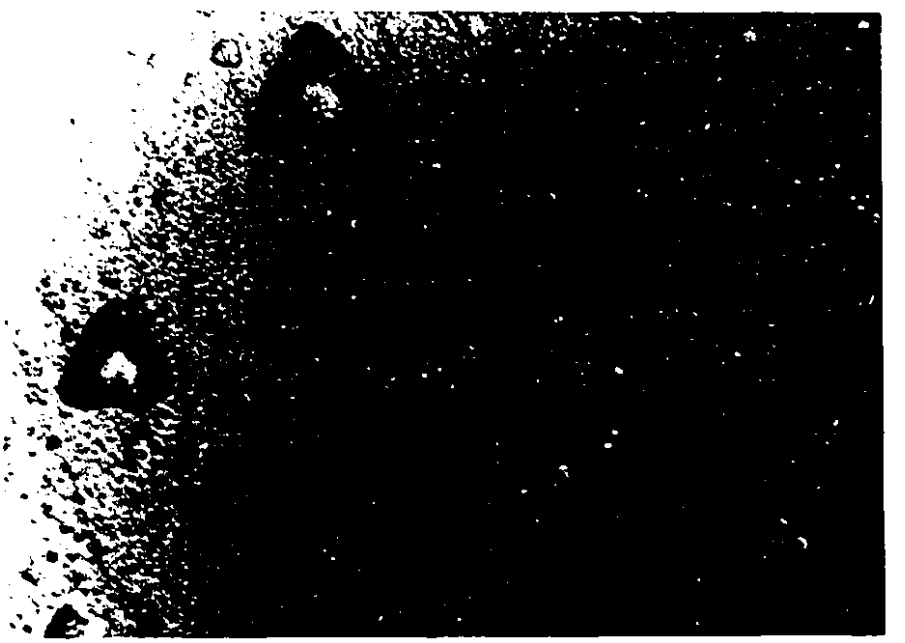


Fig. 3.11 Triangular etch pits on a polished (112) $CuInSe_2$ surface revealed after etching for 5 minutes with $K_2Cr_2O_7 + H_2SO_4$ (1:9 by weight).

Fig. 3.12 Sector-shaped etch pits on a cleaved (110) $CuInSe_2$ plane revealed after etching with $K_2Cr_2O_7 + H_2SO_4$ (1:9 by weight).

CHAPTER 4

FABRICATION OF ZnO/CdS/$CuInSe_2$ SOLAR CELLS

4.1 Introduction

Zinc oxide has become the most popular window material for $CuInSe_2$-based solar cells, mainly because of its large energy bandgap and the good electrical and antireflection properties. Furthermore, the nonuse of the toxic Cd is an additional advantage of ZnO over CdS, which was earlier the dominant window material for $CuInSe_2$. Potter et al. [4.1] were the first to use ZnO as the window layer on thin-film $CuInSe_2$ cells and demonstrated a 25 % improvement in photocurrent over cells with a CdS window layer. A very thin CdS buffer layer (< 500 Å) was still employed in the cells to provide a better junction quality with the $CuInSe_2$. Since then, the ZnO/CdS/$CuInSe_2$ structure has been widely used in thin-film $CuInSe_2$ cells. Such a structure has also been studied in our laboratory for electro-deposited $CuInSe_2$ cells [4.2]. A similar cell structure was used for the fabrication of single-crystal $CuInSe_2$ cells in the present work and they were the first single-crystal cells reported using this structure [4.3]. Sputtering has been commonly employed for ZnO deposition [1.13, 1.28, 4.4-4.5], although other methods were also reported [4.6-4.8]. A r.f.-magnetron sputtering method was used in the present work. The CdS buffer layer was deposited by a chemical-bath method, which has also been widely used by other workers [1.13, 1.28, 4.9-4.10]. The single-crystal $CuInSe_2$ substrates were carefully prepared by abrasive polishing, chemical etching and annealing in order to minimize the damage to the surfaces.

In this chapter, the deposition methods of ZnO and CdS and the surface preparation of the $CuInSe_2$ single crystals are described.

4.2 Surface Preparation of $CuInSe_2$ Substrates

Copper indium diselenide wafers were selectively cut from the ingots grown by the horizontal Bridgman method as the substrates for the CdS/ZnO/$CuInSe_2$ cells. Slices of $CuInSe_2$ with a thickness of 1 to 2 mm were sawed using a diamond-bonded wheel. The wafers were usually monocrystalline but occasionally contained multiple grains, and were generally with no specific orientation. However, several wafers were cut in the (112) orientation. After this, the wafer was lapped on both sides with a 600-grit silicon carbide paper mounted on a rotating polishing wheel to remove the damage layer resulted from the sawing. One surface was then mechanically polished with 6 μm and followed by 1 μm diamond abrasive, each for about 30 minutes, on a felt polishing cloth and then with 0.05 μm alumina powder for another 30 minutes on a Lecloth polishing cloth. Kerosene was used as lubricant for diamond abrasive and water was used for alumina. After polishing, the surface was highly specular with no visible scratches. However, scratches could be observed under microscopes.

The polished surface was then etched with a brome-methanol solution with 0.5 % bromine by volume in methanol for a period of up to one minute. Prolonged etching was avoided to prevent the appearance of etch pits as described in the previous chapter. The microscopic scratches resulted from the abrasive polishing were still visible under microscope after etching.

The sample was then annealed at 350 °C for 2 hours in argon. This was the optimal annealing condition developed from different combinations of annealing gases, temperatures and times. The purpose of the annealing was to reduce the surface defects created by mechanical polishing. The substrate annealing was found to be essential in obtaining high-performance cells.

The experimental set-up for the annealing is shown in Fig. 4.1. It was found that the presence of oxygen at elevated temperatures was detrimental to cell performance; therefore, the annealing chamber was first evacuated and then flushed with Ar for 10 minutes before raising the temperature. A SCR temperature controller was used to control the temperature to within a few degrees to the set temperature, 350 °C for most of the cases. After annealing, the samples were allowed to cool to room temperature inside the chamber with a continuous flow of argon. It was found that the annealing was very crucial in improving solar-cell performance although the extent of the effect varied with different samples.

4.3 Deposition of CdS Buffer Layer

After the surface preparation, a thin layer of high-resistivity CdS about 300-500 Å thick was deposited onto the $CuInSe_2$ substrate by a chemical-bath deposition (CBD) method. ZnO is a good window layer material for solar cells because it has a large energy bandgap and can be heavily doped into n-type conductivity. However, it has a large lattice mismatch with $CuInSe_2$ so that a high density of interface states, which could hamper the performance of the solar cell, is expected at a ZnO/$CuInSe_2$ heterojunction. In order to improve the interface properties, an intermediate layer of CdS, which has a very good lattice matching with $CuInSe_2$, is commonly used in order to minimize the interface states. The CdS is usually very thin to minimize light absorption by the buffer layer. It should be noted that only the (112) plane of $CuInSe_2$ matches well with the (0001) plane of CdS, which usually has a wurtzite structure. Since (112) is usually the preferred orientation of $CuInSe_2$ thin films and (0001) is the preferred orientation of CdS, the

lattice mismatch for thin-films cells are usually small. However, for $CuInSe_2$ substrates with orientation other than (112), the lattice mismatch might be large.

The CdS deposition was carried out by first preparing a solution of $CdCl_2$ + NH_4Cl + $(NH_2)_2CS$ + NH_4OH in a beaker. The beaker was then placed into a water bath maintained at a temperature of 60 °C. After ten minutes, the $CuInSe_2$ substrates were immersed into the solution for 10-20 minutes. It was found that a deposition time shorter than 10 minutes, i.e. CdS thinner than about 300 Å, would generally yield cells with a large leakage current. As long as it is larger than 300 Å, the CdS thickness did not seem to affect significantly the device performance. The purpose of the initial wait of ten minutes was to allow the CdS deposition to reach a steady state before dipping the substrates into the solution. Furthermore, it was also to avoid excessive etching of the $CuInSe_2$ surfaces at the initial state when the deposition rate was small. Kessler et al. [4.11] reported the etching of $CuInSe_2$ by NH_4OH during the dipping process. The experimental set-up was very simple and is shown in Fig. 4.2. The resistivity of the CdS films was about 10^5 Ω-cm. The thickness of the films was determined by the capacitance of a metal-CdS-metal structure and was also confirmed with a scanning electron microscope.

The CdS generally adhered very well onto the $CuInSe_2$ surfaces and peeled off only occasionally. However, it was observed that with an improved chemical-mechanical substrate polishing, in which a cotton wad soaked with the brome-methanol solution was used to repeatedly wipe the $CuInSe_2$ surface, the surface was too smooth for the CdS to adhere. No microscopic scratches were observed on those surfaces even under microscope in contrast with the surfaces simply etched by dipping into the brome-methanol solution. All CdS films deposited on such improved surfaces eventually peeled off during the subsequent processing. Fig. 4.3 shows a photograph of a $CuInSe_2$ surface with the peeled-off CdS. Careful cleaning and examination

ruled out the possibility of surface contamination. It appears that the bonding of the CdS film to the $CuInSe_2$ surface was not purely chemical, it involved also mechanical bonding because the CdS required a little roughness on the $CuInSe_2$ substrate to hold on to. The CdS, however, should stick very well on thin-film $CuInSe_2$ because of the roughness of the surface. The extra smoothness of the $CuInSe_2$ surfaces should be beneficial to cell performance; however, the problem of CdS detaching has not been solved. Therefore, the $CuInSe_2$ surfaces of all the devices reported in the present work were etched just by immersion into the brome-methanol solution. From these results, it is speculated that further improvement on the CdS deposition method might be required to improve the bonding of the CdS films to the $CuInSe_2$ substrates and, thus, the performance of the ZnO/CdS/$CuInSe_2$ solar cells.

4.4 Deposition of ZnO Window Layer

After the CdS deposition, low-resistivity n-type ZnO film was deposited by r.f. magnetron sputtering on top of the CdS as the window layer. The deposition was carried out in a vacuum system equipped with a turbo pump and a r.f. magnetron sputtering gun. The schematic diagram of the sputtering system is shown in Fig. 4.4. Powder of 99.9999 % pure ZnO doped with 2 wt. % of Al_2O_3 or In_2O_3 was pressed into a metal holder to form the target. The target was then fixed tightly onto the water-cooled target support. The $CuInSe_2$ substrates, now coated with a thin CdS layer, were fixed onto the aluminum substrate holder which was placed about 4 cm over the target. A glass slide was also fixed onto the substrate holder to obtain the ZnO film for characterization. The substrate holder was water cooled to minimize substrate heating during the sputtering.

The vacuum chamber was first evacuated to a pressure of about 10^{-6} torr and then refilled with pure argon, which acted as the sputtering gas, to a pressure of about 200 mtorr. The r.f. power supply was then turned on and set at 80 watts to start the sputtering. Once the plasma was formed, the argon pressure was reduced to 60 mtorr by reducing the flow rate of the argon and maintained at this pressure for the rest of the experiment. The sputtering process usually took about 8 hours to obtain a ZnO film of about 1 μm thick, giving a deposition rate of about 20 Å/min. The thickness of the ZnO film was determined by scanning electron microscope. The properties of the ZnO film were obtained by examining the film deposited on the glass slide. The resistivities of the ZnO films were about 10^{-3} to 10^{-2} Ω-cm as determined by four-point probe. Using the mobility values obtained for the same ZnO films [4.12], the electron concentrations were calculated to be in the order of 10^{20} cm^{-3}. The transmission of the ZnO films was measured over a range of wavelengths as shown in Fig. 4.5 for two samples. The transmission was over 90% for most of the photons with energy smaller than the bandgap of ZnO, indicating the high quality of the films.

After the ZnO deposition, a circular area of ZnO and CdS was defined by photolithography. Dilute HCl was used to remove the unwanted ZnO and CdS. The area of the ZnO was usually either 5.5 or 9.5 mm^2 although several larger cells were made.

4.5 Metal Front and Back Contacts

An aluminum dot was thermally evaporated onto the ZnO as the ohmic contact. The area of the aluminum dot was 1.5 mm^2, giving an active area of the solar cell (area of ZnO minus area of aluminum contact) to be 4 or 8 mm^2. Aluminum grid, instead of a dot, was used on several

cells in order to increase the collection efficiency of the photocurrent and reduce the series resistance of the cells. However, no significant improvement was observed for these cells probably because of the small cell area. Therefore, aluminum dot was deposited on most of cells as the front contact. A layer of gold was then deposited by thermal evaporation onto the backside of the $CuInSe_2$ substrates as the back contact. Most of the cells showed only a small series resistance, indicating the front and back contacts were more or less ohmic. Fig. 4.6 shows a schematic diagram of the complete cell structure.

4.6 Conclusions

ZnO/CdS/$CuInSe_2$ solar cells have been fabricated using single-crystal $CuInSe_2$ substrates. $CuInSe_2$ slices were cut from the Bridgman-grown ingots and abrasively polished using various grits of diamond and alumina abrasives. The highly specular surfaces were then etched by a brome-methanol solution. CdS films were then deposited by a chemical-bath method and had a resistivity of 10^5 Ω-cm and a thickness of 300-500 Å. The bonding of the CdS film to the $CuInSe_2$ surface was believed to be not purely chemical but also involved mechanical bonding. The ZnO was deposited by r.f. magnetron sputtering on top of the CdS and had a resistivity of 10^{-3} to 10^{-2} Ω-cm, carrier concentration of about 10^{20} cm^{-3} and thickness of about 1 μm. The transmission of the ZnO films was over 90 %. Photolithography was used to define the ZnO area and an aluminum dot was evaporated onto the ZnO as the front contact, giving an active area of 4 or 8 mm^2. Au was used to provide the back ohmic contact to the $CuInSe_2$.

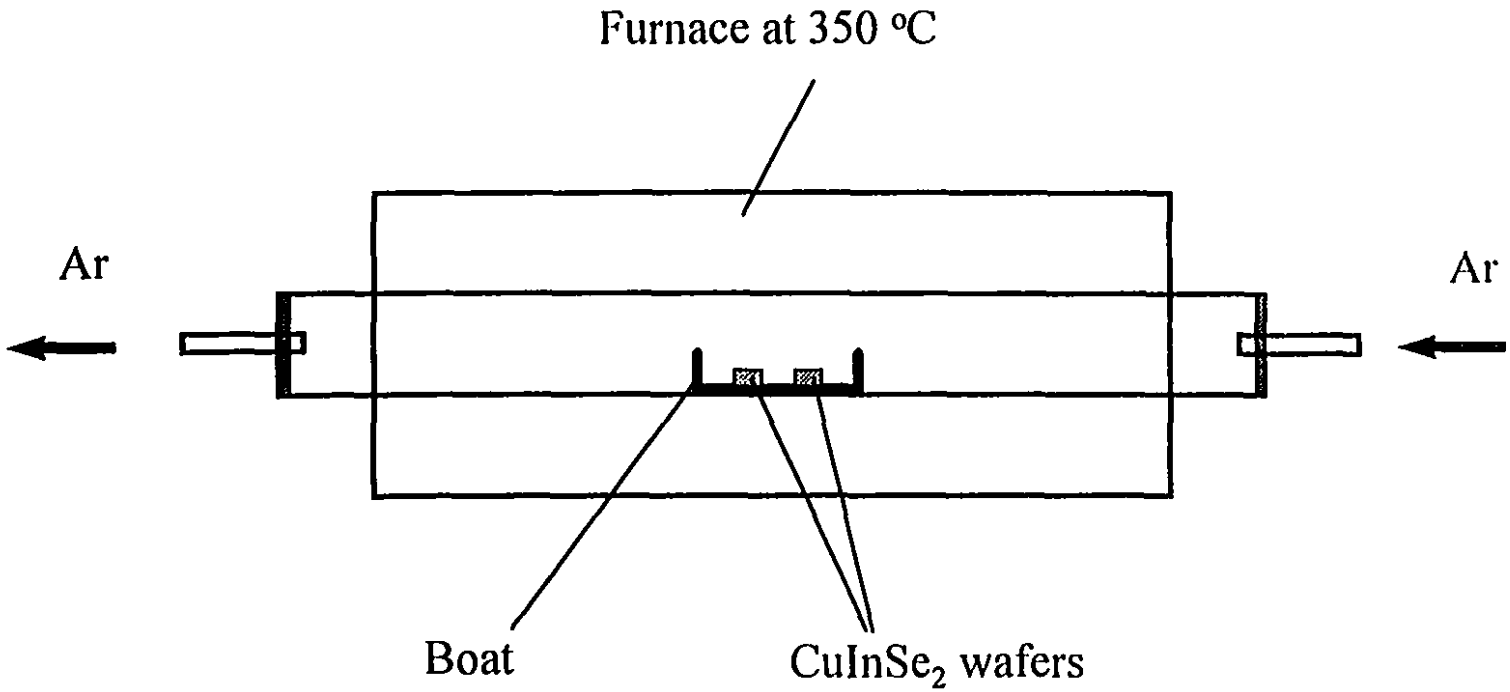


Fig. 4.1 Experimental set-up for $CuInSe_2$ substrate annealing.

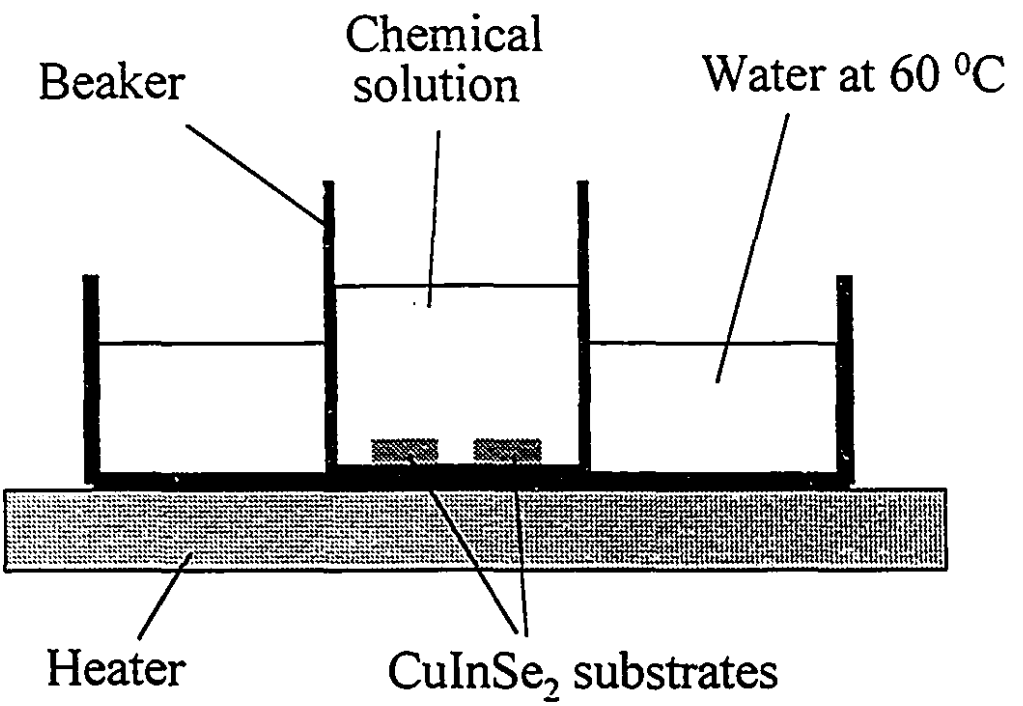


Fig. 4.2 Chemical-bath deposition of CdS onto $CuInSe_2$ substrates.

Fig. 4.3 Top view of a cracked CdS film on top of the $CuInSe_2$ substrate.

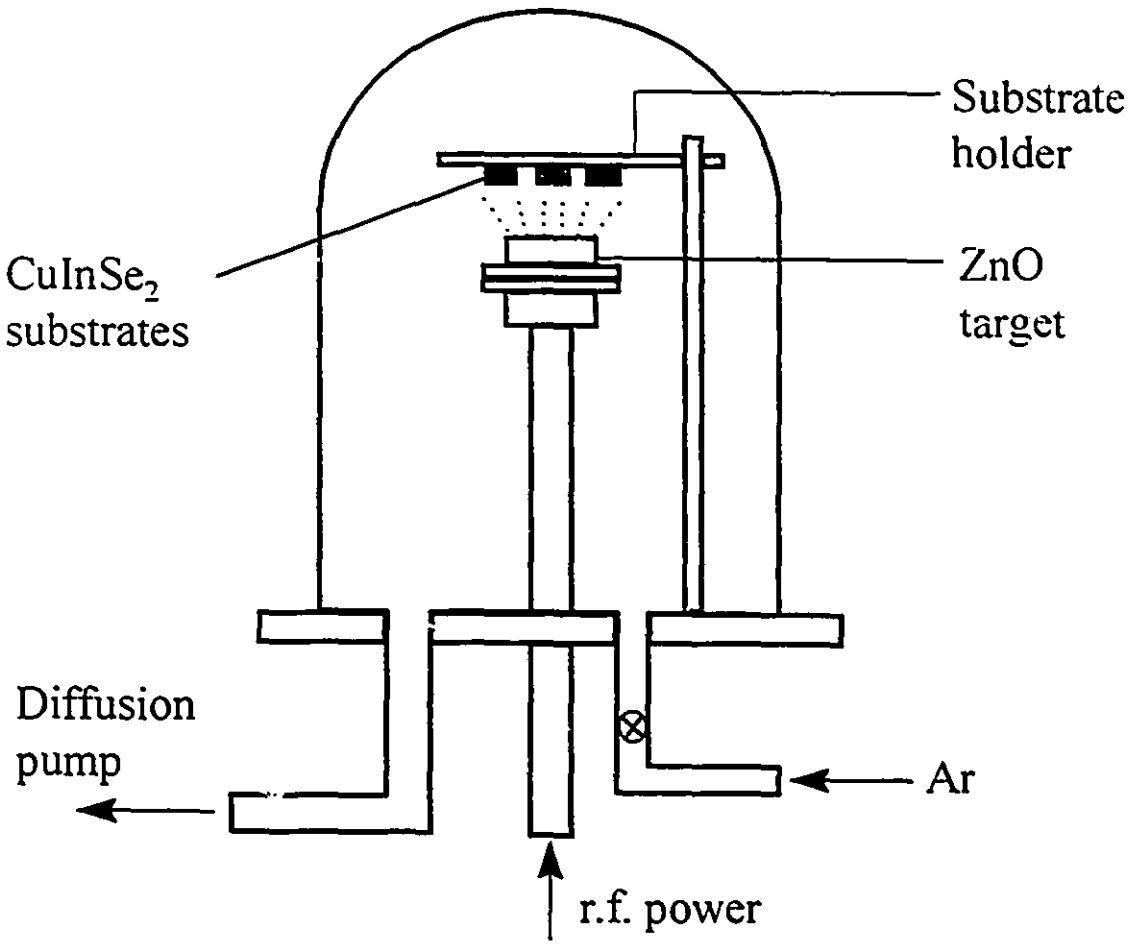


Fig. 4.4 ZnO sputtering system.

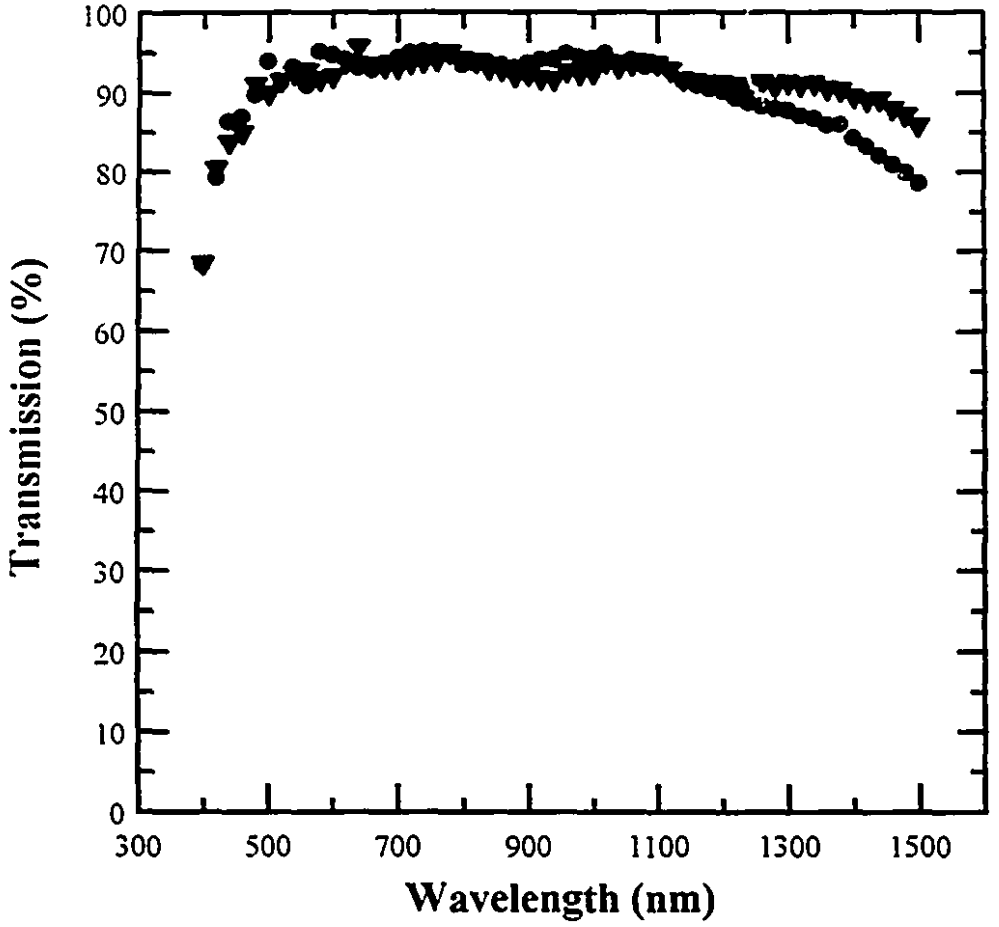


Fig. 4.5 Transmission of two ZnO films.

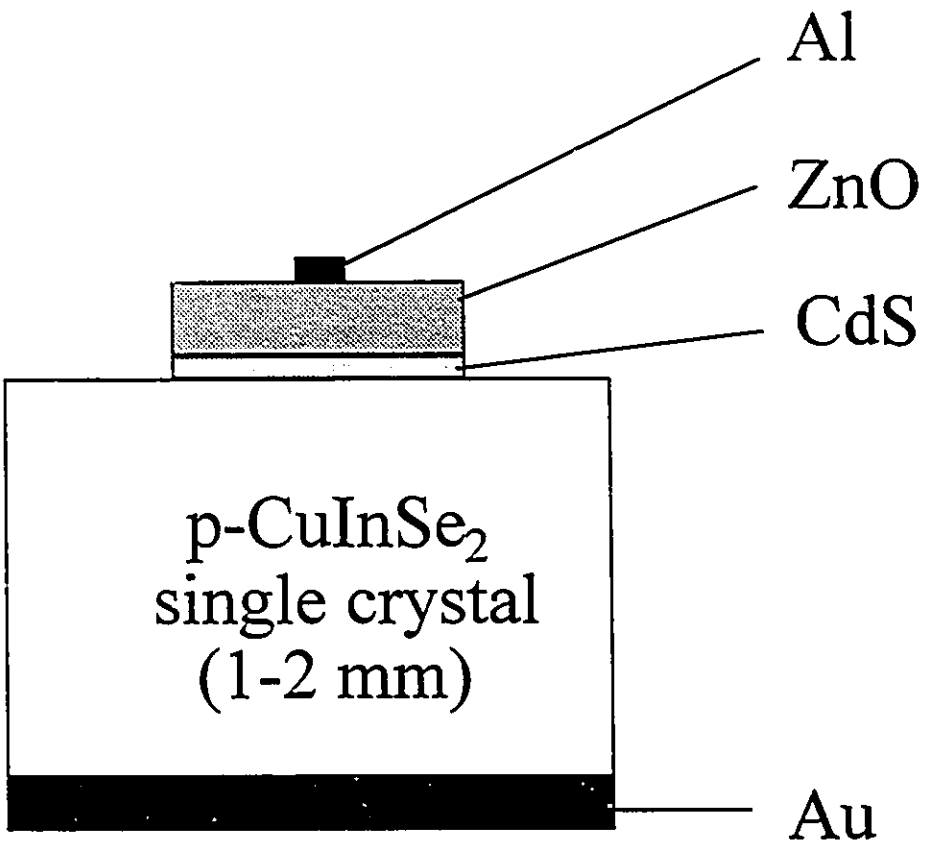


Fig. 4.6 The structure of the ZnO/CdS/$CuInSe_2$ cell.

CHAPTER 5

CHARACTERIZATION OF ZnO/CdS/$CuInSe_2$ SOLAR CELLS

5.1 Introduction

The pioneering single-crystal CdS/$CuInSe_2$ solar cell with 12 % conversion efficiency was fabricated on a cleaved $CuInSe_2$ surface and had a small active area of 0.79 mm^2 [1.3]. Ensuing works [1.5-1.11] did not show any improvement on the photovoltaic performance of single-crystal $CuInSe_2$ cells and the 12 % conversion efficiency has remained as the record. However, using a cleaved surface might limit the size of the device and reproducibility of the experimental results because cleaved $CuInSe_2$ surfaces usually have a small area and are not smooth. On the contrary, mechanical polishing should provide large and smooth surfaces for device fabrication, but photovoltaic cells fabricated on such mechanically-polished surfaces generally had poor performance [1.4-1.6, 1.11], probably due to the surface defects created by mechanical polishing.

In the present work, efforts have been made to improve the photovoltaic performance of the ZnO/CdS/$CuInSe_2$ cells fabricated on mechanically-polished $CuInSe_2$ substrates. A pre-cell-fabrication substrate annealing in argon was found to be one of the most important steps if not the most important step for obtaining high photovoltaic performance. Although annealing of bulk $CuInSe_2$ crystals in O_2 has been reported [5.1] for the studies of oxygen doping, the argon annealing in the present work was the first annealing process developed to minimize the surface defects on mechanically-polished $CuInSe_2$ surfaces. Experimental results on substrate annealing

and the electrical characterizations of the ZnO/CdS/$CuInSe_2$ solar cells are presented in this chapter.

5.2 Photovoltaic Measurements

Photovoltaic measurements were performed on the ZnO/CdS/$CuInSe_2$ cells by illuminating the cells with a tungsten light source, which was adjusted to a light intensity of global AM 1.5 (100 mW/cm^2) using an Si cell. Some cells were also measured under the sun to obtain the solar to electrical conversion efficiency. The current-voltage characteristics under illumination were recorded using an HP 4145A model Semiconductor Parameter Analyzer. Measurements were carried out immediately after the application of light to prevent heating of the cells.

5.2.1 Effects of Substrate Annealing

A series of experiments was carried out to develop an optimal annealing conditions for the $CuInSe_2$ substrates and it was found that an annealing at 350 °C in argon for 2 hours would give the best cell performance. Fig. 5.1 shows the effect of the substrate annealing on the photovoltaic performance for two cells (D-101 and D-106). The two cells were fabricated in the same run and all the fabrication procedures were the same except the $CuInSe_2$ substrate of the cell D-101 was annealed with the optimal conditions and the substrate of D-106 was not annealed at all. Both substrates were cut from the same ingot. It can be seen that the open-circuit voltage, fill factor and short-circuit current density all increased drastically by the annealing. The conversion efficiency increased more than four fold from 1.9 % to 8.3 % by substrate annealing. Not every

cell showed such a dramatic improvement, but substrate annealing was always beneficial to cell performance.

Fig. 5.2 shows a more modest improvement by substrate annealing. The open-circuit voltage increased more than 10 % from 0.42 V for the non-annealed cell (D-38) to 0.47 V for the annealed cell (D-39). The fill factor and short-circuit current density, however, showed smaller improvements. The conversion efficiency, in this case, increased from 8.0 % to 10.3 %. Table 5.1 summarizes the results obtained from Fig. 5.1 and 5.2. There were always improvements on the open-circuit voltage and fill factor by substrate annealing, but the short-circuit current density sometimes showed no significant improvement. It was found that cells with very poor performance benefited the most from substrate annealing. Most the cells fabricated with substrate annealing showed a conversion efficiency better than 8 %. However, the performance of the cells seemed to be also dependent on the quality of the $CuInSe_2$ substrates because cells with substrates cut from the same ingot generally showed very similar performance.

Although preliminary experiments showed that the optimum substrate annealing condition was about 350 °C in pure argon for about 2 hours, controlled experiments using substrates cut from the same region of an ingot and at the same orientation were later carried out to confirm the results. Different annealing temperatures, times and gases were tried by varying one variable at a time. The set of $CuInSe_2$ substrates was then processed with subsequent fabrication steps at the same time. It was found that the open-circuit voltage and the fill factor were strongly dependent on the annealing parameters. Fig. 5.3 and 5.4 show the variation of V_{oc} and F.F. with annealing temperature. It can be clearly seen that the temperature for the largest V_{oc} was about 350 °C while the fill factors were about the same for temperatures from 250 °C to 400 °C. The annealing

time had a similar effect as the annealing temperature to the device parameters. The F.F. saturated after about an hour of annealing as can be seen from Fig. 5.5 while the V_{oc} peaked at about 2 hours as in Fig. 5.6. It can also be seen that even an annealing for just ten minutes or at low temperatures showed a big improvement over non-annealed samples, indicating the importance of substrate annealing. However, the short-circuit current density did not seem to vary systematically with the annealing time and temperature in these experiments, non-annealed sample sometimes showed comparable or even larger current density than the annealed samples, confirming the results obtained from other cells.

Fig. 5.7 shows the illuminated I-V characteristics of four cells with substrates heat-treated in different gaseous environments. The samples treated in argon and hydrogen showed the best and comparable results. Considering the potential danger of H_2 gas, Ar was preferred as the annealing gas. Annealing in oxygen or air was always detrimental to cell performance; while annealing in vacuum was found to improve slightly the cell performance but not as effectively as Ar or H_2. From these results, the optimal condition for substrate annealing was confirmed to be about 350 °C in argon for two hours.

5.2.2 Spectral Response

Spectral responses of the ZnO/CdS/$CuInSe_2$ cells were measured in the wavelength (λ) range of 400 to 1300 nm. A monochromatic light source (Beckman model 2400) with a slit width of 1 mm was used. The light intensity was determined by a Si detector (United Detector model PIN 6DP) for the range of 400 to 1000 nm and by a liquid nitrogen-cooled Judson Infrared InSb

detector for wavelengths above 1000 nm. The photocurrent or short-circuit current was then measured for each wavelength to give the spectral response of a cell.

Fig. 5.8 shows the spectral response of two similar cells, one with (D-39) and one without (D-38) substrate annealing. The two cells had similar spectral responses although D-38 showed a few percent smaller quantum efficiencies than D-39 over the whole spectrum. This explains the smaller short-circuit density of D-38 as shown in Table 5.1. However, the similar shapes of the spectral responses indicate that substrate annealing did not alter significantly the nature of the collection mechanism. The quantum efficiencies were nearly constant in the range of 500 to 1000 nm for the annealed cell but declined slightly toward larger wavelengths for the non-annealed cell. Although this can account for the few percent smaller short-circuit current density for the non-annealed cell in the present case, this slight decline of quantum efficiency was also observed in some other annealed cells, showing that this was not unique to non-annealed cells. Furthermore, there were non-annealed cells showing larger short-circuit density than similar annealed cells as well, indicating that the difference of short-circuit densities of annealed and non-annealed cells was more likely to be due to other factors such as variations of ZnO and CdS transmissions or properties of $CuInSe_2$ substrates.

The quantum efficiencies of both cells decreased linearly with wavelengths beyond 1000 nm; while other thin-film cells [4.1] showed constant quantum efficiencies up to 1200 nm. Such a linear decrease of quantum efficiency could be due to the small depletion width of the cells because long-wavelength photons might penetrate beyond the thin depletion region and create charge carriers in the neutral $CuInSe_2$ region. Due to the high net acceptor concentration of the $CuInSe_2$ substrates ($\sim 10^{17}$ cm^{-3}), the depletion width must be thin. Therefore, in order to increase the quantum efficiencies of low energy photons, a smaller net acceptor concentration is required.

Another observation was that the optical absorption of the CdS buffer layer might not be negligible, as illustrated by the reduced quantum efficiencies of wavelengths between 390 and 520 nm. It is clear that the quality of the CdS films has to be further improved in order to obtain larger short circuit current density. It can also be seen that the quantum efficiencies for most of the wavelengths were smaller than 60 %, which is relatively low compared to more than 80 % for thin-film cells [1.13, 4.1, 4.4]. The small quantum efficiencies might result in the relatively small short-circuit current densities of the cells, about 30 mA/cm^2, compared to more than 40 mA/cm^2 for some thin-film cells [1.13]. Due to the specular nature of the $CuInSe_2$ surfaces and the fact that anti-reflection coating was not used in the present case, the reflection of the incident light could be very large. This might account for the low quantum efficiencies of the cells. With the use of an effective anti-reflection coating, the quantum efficiencies and, thus, the short-circuit current density might increase.

5.2.3 Photovoltaic Characteristics

All cells were measured with a simulated global AM 1.5 illumination (100 mW/cm^2) and some cells were also measured under the sun to confirm the measurements. The results of some cells are shown in Table 5.2. Most of the cells fabricated with substrate annealing showed a conversion efficiency over 8 %, an open-circuit voltage over 0.4 V, a short-circuit current density over 25 mA/cm^2, and a fill factor over 0.65. The illuminated and dark I-V characteristics of two of the best cells, D-39 and D-102, are shown in Fig. 5.9 and 5.10. The parameters of these two cells and the best single-crystal and thin-film cells reported in the literature are summarized in Table 5.3 for comparison. It can be seen that the fill factors of D39 and D102 exceed the best single-crystal cell and are comparable to the best thin-film cell. The open-circuit voltages are a

little bit smaller than the other two cells. However, the short-circuit current densities of D-39 and D-102 are considerably smaller. This might be due to the lack of an antireflection coating as explained before. Using an effective layer of antireflection coating should be able to increase considerably the short-circuit current density of these cells and also slightly the open-circuit voltage.

The 11.5 % and 10.3 % conversion efficiencies of D-102 and D-39 are comparable to the 12 % efficiency of the best single-crystal cell. In fact, 11.5 % has been the highest efficiency reported for a single-crystal $CuInSe_2$ cell for the last two decades since the 12 % cell. It should also be noted that the 12 % efficiency was obtained with the use of an anti-reflection coating and the same cell showed only a 10.6 % conversion efficiency without anti-reflection coating [1.3]. In other words, the 11.5 % conversion efficiency obtained in this work has been the highest efficiency reported for a single-crystal $CuInSe_2$ cell without antireflection coating. Furthermore, the active area of D-102 is five times larger and D-39 is about an order of magnitude larger than the 12-% cell. To summarize, this is the first report of a fabrication process that can routinely produce relatively large-area single-crystal $CuInSe_2$ cells with efficiencies close to or exceeding 10 %.

5.3 Dark Current-Voltage Measurements

The dark current-voltage (I-V) characteristics were measured using an HP model 4145A Semiconductor Parameter Analyzer. By analyzing the I-V characteristics, the current mechanism of the cells can be identified. Understanding the current mechanism might lead to further improvements of cell performance.

5.3.1 Dark Current-Voltage Characteristics

Fig. 5.11 and 5.12 show the logarithmic plot of the dark current against voltage (log I vs. V) of the devices D-102 and D-39. The forward currents consisted of three main sections. The curved section at voltages greater than about 0.5 volt was undoubtedly caused by series resistance. Examination of this section showed a linear I-V relationship, indicating a resistive behaviour of the cells at voltages greater than about 0.5 V. The series resistance were determined to be about 0.58 Ω-cm^2 for D-39 and 0.72 Ω-cm^2 for D-102 from the slope of linear I-V plots at large voltages. The series resistances of most of the cells were smaller than 1 Ω-cm^2 and should not cause a big problem in cell performance in the operating voltage range.

In the voltage range of about 0.3 to 0.5 V, which is about the operating voltage range of the cells, the current was exponentially dependent on the voltage and appeared to be straight in the log I vs. V plot. The n factor values were calculated to be 1.54 and 1.87 for D-102 and D-39, respectively. There did not seem to be a relationship between the performance of the devices and the n factor values, despite the fact that a smaller n factor is closer to the ideal case of pure injection current. In fact, there were several devices with an n factor as low as 1.37 showing much poorer performance than those with larger n factor values.

Values of n close to one are always considered to be due to injection current and values close to two are usually attributed to current due to recombination of charge carriers in the depletion region; while an n factor lying between 1 and 2 is generally believed to be due to a combination or a modification of the two current mechanisms. Most Si and GaAs p-n homojunction solar cells contained both of these two current mechanisms [5.2]. However,

tunneling has been reported to be the dominant current mechanism in many heterojunction devices such as Ge/GaAs [5.3], Ge/Si [5.4] and ITO/Si [5.5] heterojunctions and Cu_2S/CdS solar cells [5.6-5.8]. Tunneling currents are sometimes mistaken for the injection and/or recombination current because of its exponential dependence on voltage and an apparent n factor of smaller than two in some cases. Temperature-dependent measurements of the I-V characteristics are required to distinguish tunneling currents from thermal ones such as injection and recombination currents because tunneling currents are generally insensitive to temperature as opposed to thermal currents. Temperature-dependent I-V measurements were carrier out in the present study in order to determine the actual current mechanism in our ZnO/CdS/$CuInSe_2$ cells and the results will be presented in the next section.

It can also be seen in the figures that at voltages in the range of about 0.1 to 0.3 V, the slope of the log I-V curves changed to a smaller value. The smaller slope gave rise to an n factor usually greater than two and sometimes three for most of the devices. The large n factor cannot be explained by the thermal injection or recombination model but can be due to modifications of the recombination model in which the distribution of recombination centres are not uniform [5.9-5.12], to tunneling [5.8] or to shunt resistance [5.13]. With an exception of a few devices, most of the devices showed such a bulge at small voltages.

It was also observed that the bulge occurred when the forward current was sufficiently small and comparable in magnitude to the reverse current at the same voltage magnitude (Fig 5.11). It seems that it was a sum of the reverse current and the extrapolation of the forward current from higher voltages. This means that the current mechanism in the reverse bias might also be playing a role in the small forward bias region. Therefore, it is necessary to identify the current mechanism in the reverse bias.

The reverse currents of all the devices were carefully examined and it was found that they all showed a near linear I-V relationship, i.e. ohmic behaviour. The reverse current of four devices are shown in Fig. 5.13. The linear reverse current-voltage relationship can be clearly seen and such a linear relationship can only be explained by a shunt resistance across the p-n junction. Therefore, it can be concluded that the reverse current was dominated by shunt current. The shunt resistance can be calculated from the slope of a reverse I-V curve. The shunt resistances were calculated to be about 25.5 and 11.6 $k\Omega$-cm^2 for D39 and D102, respectively. By looking at the equivalent circuit of the cells in Fig. 2.6, it is apparent that the shunt current was present at both the reverse and forward bias and the forward shunt current could be dominant at low forward voltages when the diode or junction current was small. However, the shunt current could be neglected at higher voltages because the forward diode current increased exponentially with voltage. In the voltage range of operation of the solar cells, the shunt resistance could be neglected.

To obtain the junction current in the forward bias at low voltages, it is necessary to subtract the shunt current from the total forward current. It is apparent that at the same voltage magnitude, the reverse and forward shunt current should be the same in magnitude. Therefore, the correction for the shunt resistance was done by subtracting the reverse current from the forward current at the same voltage magnitude. This method of shunt-resistance correction has a benefit of taking into account of any nonlinearity of the shunt resistance that cannot be done by using a discrete shunt-resistance value. However, this method can only be applied when the reverse current is dominated by shunt current. After the correction for shunt resistance, some devices showed only a single slope as in Fig. 5.14. However, some devices still showed a second slope or a bulge at low voltages (0.1 to 0.3 V) in the log I-V plots (Fig. 5.15), indicating the

possibility of a second current component. In order to determine whether there is a second current component and its mechanism, temperature-dependent I-V measurements are required.

5.3.2 Temperature-dependent Current-Voltage Measurements

The I-V characteristics were measured in the temperature range of 100 K to 300 K. The dark forward I-V characteristics of two typical cells, D-100 and D-101, measured at different temperatures are shown in Fig. 5.16 and 5.17. Both cells were fabricated using the optimum method and had a conversion efficiency of about 8%. The currents were corrected for shunt resistance at each temperature as described in the previous section. In order to see whether the shunt current was still dominant at different temperatures, the reverse current was plotted against the reverse voltage for many devices. A linear reverse I-V relationship was observed at all temperatures as shown in Fig. 5.18 for D-100, justifying the shunt-resistance correction method.

Both cells showed similar temperature-dependent log I-V characteristics. The curved section at large voltages was due to series resistance as explained before. At smaller voltages, two straight-line sections can be clearly seen, especially at low temperatures (Fig. 5.16). Since the curves were corrected for shunt-resistance effect, it is likely that the corrected current represented the real junction current. The two straight-line sections can then be explained by two current components having an exponential dependent on voltage. One component was dominant at high temperatures and large voltages and the second component was dominant at low temperatures and small voltages. Thus, the I-V characteristics of the devices can then be described by two current components,

$$I(V,T) = I_{o1}(T)e^{B_1 V} \qquad \text{(for low voltages)}$$

$$= I_{o2}(T)e^{B_2 V} \qquad \text{(for high voltages)} \ , \qquad (5.1)$$

where B_1 and B_2 are the slopes of the two straight-line sections in the log I-V curves and are almost independent of temperature as can be seen from the constant slope at different temperatures in the graphs. The I_{o1} and I_{o2} terms accounts for the temperature dependence of the currents. The values of B_1 and B_2 were then determined from the slope of each section and I_{o1} and I_{o2} from the intercepts of the interpolation of each section to the current axis. The slopes of D101 were 14.8 for the low-voltage section and 24.8 for the high-voltage section. For D-100, these values were 11.2 and 25.2.

Another observation is that at some regions, e.g. the low voltage region of D-100 at 260 K and 220 K in Fig. 5.16, the slope of the logarithmic curve lay between B_1 and B_2; this might be due to the presence of both current components. It can be seen that at 300 K, only the current component having the slope of 25.2 was dominant at all voltages (0.1 to 0.5 V) for D-100. However, as the temperature was reduced, the second component with a slope of 11.2 began to appear at low voltages, became more and more significant as the temperature was further decreased, and became dominant at temperatures below 180 K, causing the slope to change from 25.2 to 11.2. At the temperatures which neither current components were dominant, i.e. between 300 K and 180 K, a slope between 11.2 and 25.2 was obtained. Similar explanation can be applied to D101 in Fig. 5.17, except the low-voltage current component was present even at 300 K and was dominant at all voltages at temperatures below 175 K. All the ZnO/CdS/$CuInSe_2$ cells, including the best cells, prepared in the present work showed similar temperature-dependent I-V characteristics.

The temperature-independent slope of the logarithmic curves is a characteristic of only tunneling current. All the other current mechanisms have a temperature-dependent slope in a log I-V plot. For these thermal currents, the slope should have reduced by a factor of three when the temperature is decreased from 300 K to 100 K. Since tunneling has also been reported to be quite common in heterojunctions [5.3-5.9], it is very likely that tunneling is the current mechanism of the ZnO/CdS/$CuInSe_2$ solar cells prepared in the present work.

There are several models each having a different tunneling mechanism. It is, therefore, necessary to examine each model carefully to determine the appropriate one for the present case. The first one was proposed by Esaki [5.14] to explain the behaviour of tunneling diodes. It involves the interband tunneling through a very thin depletion layer from the conduction band of a degenerated n-type semiconductor to the valance band of a degenerated p-type semiconductor. However, this model is not applicable in this case because the $CuInSe_2$ was not degenerated although the ZnO could be considered degenerated. Furthermore, the negative differential resistance and the current peak and valley that are typical of a tunnel diode were not observed experimentally in our devices.

The second model is the tunneling through the energy spike in the conduction or valence band which arises from the differences of the electron affinities and energy band gaps of the two materials in a heterojunction [5.3]. This model is similar to the one proposed by Padovani and Stratton [5.15] for thermionic-field emission tunneling in Schottky barriers in which the potential barrier or "energy spike" arises from the differences between the work function of the metal and the electron affinity of the semiconductor. However, the thermionic-field emission tunneling model is not applicable because it also gives a temperature-dependent slope of the exponential curve.

The third model was proposed by Riben and Feucht [5.3] for a Ge-GaAs heterojunction. The model was similar to the one proposed by Chynoweth et al. [5.16] to explain the excess current in tunneling diodes. In this model, the charge carriers tunnel across the junction through interface states or/and deep levels which lie in the forbidden gaps of the semiconductors. Depending on the distribution and the densities of these states in the energy gaps, several tunneling paths are possible. This tunneling model is illustrated in Fig. 5.19 for a n Ge-p GaAs heterojunction [5.3]. Three tunneling paths are shown in the figure. In path A, electrons drop to the interface states from the conduction band of Ge and tunnel to the top of the valence band of GaAs. In path B, electrons tunnel into the available bandgap state or deep level inside GaAs and then fall into the valence band. In path C, electrons tunnel through multiple levels of available bandgap states at the surface of GaAs and then fall into the valence band. All three paths should lead to similar functional dependence of current on voltage [5.3]. This model leads to a log I-V slope independent of temperature and has been found to be satisfactory, at least qualitatively, in explaining the I-V characteristics of Ge/Si [5.4], ITO/Si [5.5] and Cu_2S/CdS heterojunctions [5.6-5.8] as well. Therefore, it is speculated that this model is applicable to the present ZnO/CdS/$CuInSe_2$ cells as well. The tunneling current in this model can be expressed as [5.16],

$$I_{tunnel} = AN_t P_{tunnel} \propto N_t e^{BV}, \qquad (5.2)$$

where A is a constant, N_t is the density of available bandgap states and P_{tunnel} the tunneling probability, which is a function of the energy of the tunneling barrier and the electric field. The double slopes of the log I-V curves in the present case can then be explained by two different tunneling paths, each having a region of domination dependent on the density of the corresponding bandgap states and the tunneling probability of each path. Claassen [5.17] also

reported such a double-slope tunneling current through two distinct bandgap levels for the excess current in their Esaki diodes.

In order to help the understanding of the tunneling mechanism, the temperature-dependent I-V measurements were also carried out for the cells without substrate annealing because it was found that the I-V characteristics were strongly dependent on the surface preparation of the $CuInSe_2$ substrates Fig. 5.20 shows the temperature-dependent I-V characteristics of one of the non-annealed cells. It can be seen that the cell did not exhibit a straight line portion of the log I-V plot but showed an almost parallel shift of the curve with temperature. Almost all of the non-annealed samples showed such a curved log I-V plot. Furthermore, the dark current magnitude of a non-annealed cell was always greater than that of an annealed cell. The large forward current in non-annealed cells could be due to a small shunt resistance, which could result in a large shunt current. Examination of the reverse currents of the non-annealed cells showed that they were dominated by shunt current. However, the shunt current was small compared to the large forward current even at low voltages and was usually negligible. The large forward current was then likely to be the result of junction current and could be due to tunneling through multiple or continuous levels of bandgap states [5.17], which might be created by mechanical polishing and located at the $CuInSe_2$ surface. This is illustrated in the band diagram shown in Fig. 5.21. The large density of electrons in the ZnO conduction band can easily tunnel through the thin CdS where the electric field is large, into the defect states at the $CuInSe_2$ surface and then into the valence band of $CuInSe_2$. Deep level states intrinsic to the $CuInSe_2$ crystal are omitted in the diagram for clarity. The large density of defect states at the surface of non-annealed samples were further confirmed by DLTS measurements and the results will be presented in chapter 7.

The tunneling mechanism of a cell with substrate annealing should be different. It is believed that substrate annealing reduced significantly the amount of surface defects so that they were not playing an important role in the current mechanism of annealed samples. Each straight-line portion of the log I-V plot of an annealed cell corresponded to a single-path tunneling. Two scenarios are possible as illustrated in Fig. 5.22. In Fig. 5.22 (a), electrons drop to the interface states caused by lattice mismatch and tunneling directly into the valence band of $CuInSe_2$. Two tunneling paths are shown to account for the double slopes and each tunneling path dominates at certain voltage and temperature ranges.

Another scenario is tunneling assisted by deep levels in the $CuInSe_2$ as shown in Fig. 5.22 (b). In this case, electrons drop to the interface states, tunnel to the deep levels, and then fall to or recombine with holes in the valence band of $CuInSe_2$. The actual tunneling paths are, of course, not necessary to be exactly as shown in the figure, the important point is that the tunneling is assisted by deep levels. Two tunneling paths are possible because there are two deep levels. Since deep levels are very common in semiconductors, this tunneling mechanism is quite possible. Indeed, it is easier to visualize the two tunneling paths are caused by two deep levels than by direct tunneling because direct tunneling usually only occurs at the energy level where the energy barrier is thin enough for tunneling. Anyway, the two scenarios should lead to similar functional dependence of current on voltage.

The other important parameters that needed to be examined are the I_{o1} and I_{o2} terms in Eq. 5.1. Newman [5.18] reported an exponential dependence of the I_o term on temperature for various heterojunctions. The I-V characteristics of these devices obeyed the following empirical equation,

$$I = I_o e^{BV} = I_{oo} e^{\frac{T}{T_o}} e^{BV}, \qquad (5.3)$$

where, I_{oo}, T_o and B are constants and B, as explained before, is the slope of the log I-V curve. This temperature variation of the curves was suggested by Sites [5.5] and Riben and Feucht [5.3] to be due to a change in diffusion potential. However, it was found that the temperature variation of the devices in the present work showed a T^{-1} dependence of I_o similar to some published calculations [5.18], and the current can be expressed as

$$I = I_o e^{BV} = I_{oo} e^{-\frac{T_o}{T}} e^{BV} = I_{oo} e^{-\frac{E_A}{kT}} e^{BV}, \qquad (5.4)$$

where E_A is the activation energy of a thermally associated process and k is the Boltzmann's constant. Lindquist and Bube [5.8] had found activation energies of 0.26 and 0.45 eV for their Cu_2S/CdS p^+-n devices with Cd-face and S-face CdS monocrystalline substrates, respectively. They suggested that the electrons had to be activated to a certain level in the conduction band of CdS such that the barrier is thin enough for appreciable tunneling through interface states to occur, similar to the direct tunneling model shown in Fig. 5.22 (a). Since the log I-V plots of these devices showed only a single slope at all temperatures, only one tunneling path existed.

The activation energy of each tunneling current component can be obtained by plotting ln I_o against T^{-1}. As explained before, each value of I_o was obtained from the intercept of the current axis with the interpolation of each straight-line section in the log I-V plot at the corresponding temperature. It should be noted that in the cases where the slope lies between the two values, curve fitting was carried out to determine the magnitude of each current component. Fig. 5.23 shows the ln I_o-T plots for the two current components of the sample D-101. For this sample, the activation energies of the two current components were found to be about 0.09 eV for the low-voltage slope (14.8) and 0.29 eV for the high-voltage slope (24.8). Similar values of activation

energy, 0.11 eV and 0.30 eV, were obtained for D-100. The T^{-1} temperature variation of the current can be explained by the need of activating the holes in the $CuInSe_2$ valence band to a certain energy level before they can recombine with the tunneling electrons as shown in Fig. 5.22 (b). To put it in another way, the tunneling electrons fall from the deep level into the $CuInSe_2$ valence band inside the depletion region where there is band bending. The band bendings are E_{A1} and E_{A2}, measured from the top of the valence band in the neutral $CuInSe_2$ region, as shown in Fig. 5.22 (b). Considering path *a* in the figure, the density of holes available for recombination is

$$p_{E_{A1}} = p_o e^{-\frac{E_{A1}}{kT}}, \tag{5.5}$$

where p_o is the hole concentration in the neutral $CuInSe_2$ region. In Eq. (5.2) for the tunneling current, the electrons are assumed to tunnel to the top of the valence band in the neutral region where there is no band bending. The hole density p_o is high in this location so that it is not a limiting factor for the tunneling current. However, for the case in Fig. 5.22 (b), the hole density available for recombination is much smaller (Eq. (5.5)) and becomes a limiting factor for the tunneling current. Therefore, Eq. (5.2) has to be modified by Eq. (5.5) and becomes

$$I_{tunnel} = AN_t p_o e^{-\frac{E_A}{kT}} P_{tunnel} \propto N_t e^{-\frac{E_A}{kT}} e^{BV}. \tag{5.6}$$

This equation can account for both the temperature-independent slope and the T^{-1} dependence of the current observed experimentally. The decrease of activation energy of the current component with slope of 14.8 at very low temperatures in Fig. 5.23 can be considered as a change of recombination location where sufficient holes are available for recombination.

5.4 Analysis of Photovoltaic Performance

As described in section 5.2.1, it was found experimentally that substrate annealing could significantly improve the open-circuit voltage and fill factor, but did not show a strong effect on the short-circuit current density. Furthermore, it has been shown in the last section that the dark I-V characteristics changed significantly with substrate annealing. It is quite possible that these two phenomena are related and, therefore, they are further examined here.

The equivalent circuit of a solar cell shown in Fig. 2.6 is repeated in Fig. 5.24 for the short-circuit and open-circuit conditions. Shunt and series resistances are omitted in the figure to facilitate explanation but they should not significantly affect the arguments. It can be seen that under the short-circuit condition (Fig. 5.24 (a)), the photocurrent flows directly to the external circuit as the short-circuit current and is not significant affected by the I-V characteristics of the p-n junction. This can explain why the short-circuit current density is not significantly affected by substrate annealing as long as the substrate annealing changes only the dark I-V characteristics of the ZnO/CdS/$CuInSe_2$ junction but not the collection efficiency of the photocurrent. It has been shown to be the case that the spectral responses were not significantly changed by substrate annealing and should result in similar collection efficiencies.

Under the open-circuit condition (Fig. 5.24 (b)), all the photocurrent "flows" into the p-n junction. To put it in another way, all the photocurrent is negated by the dark junction current. The open-circuit voltage is the voltage across the p-n junction that can produce a dark junction current equal in magnitude to the photocurrent. Therefore, it is clear that the open-circuit voltage is highly dependent on the dark I-V characteristics of the junction. It has been demonstrated that substrate annealing changed the current mechanism and, thus, the dark I-V characteristics of a

cell, and a non-annealed cell always showed a larger dark current density than a similarly prepared cell with substrate annealing. The larger dark current density in an non-annealed cell can be explained by the multiple tunneling of charge carriers.

Fig. 5.25 shows the dark I-V characteristics of the two cells shown in Fig. 5.2. It can be seen that the annealed cell (D-39) had smaller current densities at the operation voltage range of the solar cell than the non-annealed cell (D-38). Suppose both cells had the same photocurrent of 30 mA/cm^2, D-39 would have a larger open-circuit voltage (about 0.48 V) than D-38 (about 0.44). Those values are not too far off to those obtained experimentally in Fig. 5.2. This can account for the larger open-circuit voltages of annealed cells than non-annealed cells observed experimentally. In other words, the photocurrent can "leak" more readily through the larger dark current of an non-annealed cell so that a smaller open-circuit voltage is obtained than in an annealed cell. This explanation is valid only when the illumination does not change the junction I-V characteristics drastically and this was usually the case for the cells prepared in the present work as can be seen from Fig. 5.9 for D-39. In this figure, the illuminated I-V curve is almost a direct translation of the dark I-V curve along the current axis with no change in the shape. Similar behaviour was observed for the non-annealed cell, D-38, as shown in Fig. 5.26.

The increase of fill factor was due to the change of the current mechanism. The exponential dependence of the current in annealed samples usually led to a more squared I-V curve than the multiple tunneling current in non-annealed samples and, hence, a larger fill factor.

5.5 Capacitance-Voltage Measurements

In order to examine further the properties of the heterojunction, differential capacitance-voltage (C-V) measurements were made. Information such as the doping uniformity, doping concentration, diffusion potential, and interface-state and deep-level effects may be deduced from these measurements. The capacitance of a p-n heterojunction is given by

$$C = \left[\frac{qA^2 \varepsilon_A \varepsilon_D N_A N_D}{2(\varepsilon_A N_A + \varepsilon_D N_D)} \frac{1}{(V_{bi} - V)} \right]^{\frac{1}{2}}, \tag{5.7}$$

where A is the area of the device, ε_A and ε_D are the dielectric constants of the two materials, N_A and N_D are the doping concentrations, V_{bi} is the diffusion or built-in potential and V is the applied voltage. This equation is derived for the ideal case without interface-states, deep-levels or other interface effects. C-V measurements are generally used to obtain the doping profiles of the semiconductors near the interface, from the slope of a $1/C^2$ vs V plot, especially for a Schottky junction or a one-sided p-n junction. The built-in potential can also be obtained from the voltage intercept of the plot. For a one-sided n^+-p heterojunction, Eq. (5.7) can be further simplified by letting $N_D >> N_A$, and the net acceptor concentration of the p side can be obtained from the slope of a $1/C^2$-V plot as expressed by the following equation,

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_r \varepsilon_A A^2 N_A} (V_{bi} - V) . \tag{5.8}$$

The net acceptor concentration of the $CuInSe_2$ substrates in the present case can be determined by this method.

An HP model 4247A LCR meter was used to measure the differential capacitance-voltage characteristics of the cells at the frequency range of 1 kHz to 100 kHz. The dc bias applied to the cells by the LCR meter was measured with a HP3468A multimeter. A Booton model 72B

capacitance meter was used to measure the capacitance at 1 MHz. Fig. 5.27 and 5.28 show the $1/C^2$ vs. voltage plots of two cells (D-102 and D-32) measured at three different frequencies. Both cells were fabricated with substrate annealing. The plots appear to be quite linear at high voltages but at voltages near zero bias, the slopes increase and become curved. A curved C-V plot may result from a concentration gradient, deep levels in the $CuInSe_2$ or interface states at the $CdS/CuInSe_2$ interface [5.19].

It is apparent that the three possibilities may also be applicable in the present case. Tavakolian et al. [5.20] also suggested that such a distinct kink near zero bias might be due to a more lightly doped layer near the $CuInSe_2$ surface. Since the $CuInSe_2$ substrates were annealed at 350 °C in the present case, it is possible that there was out- or in-diffusion of some elements that caused the concentration gradient. In order to confirm this, the non-annealed samples were also measured. Fig. 5.29 shows the $1/C^2$-V plot of one of the non-annealed samples. It can be seen that the curves did not show any straight-line portion and the curvature increased near zero bias as well. All the non-annealed samples showed similar behaviour. Therefore, it is clear that the curved $1/C^2$-V plots were not necessarily caused by substrate annealing. Since all the other fabrication steps were not high-temperature processes, it is unlikely that concentration gradient due to diffusion was the cause of the nonlinear behaviour of the $1/C^2$-V plots.

In order to find out whether this is due to surface states or deep levels, some cells were measured at a higher frequency and larger reverse biases. Higher frequency was used because it is well known that interface states and deep levels are not responsive to the small-signal voltage in C-V measurements when the frequency is sufficiently high. The use of larger reverse biases can probe deeper into the $CuInSe_2$ so that surface effect and bulk effect can be distinguished.

Fig. 5.30 and 5.31 show the $1/C^2$-V plots of two samples, one with substrate annealing (D-100) and one without the annealing (D-111). It can be seen that at 1 MHz, the $1/C^2$-V plots of both samples were completely straight up to small forward biases. The missing kinks indicate that they were frequency-dependent and further confirmed that they were not caused by concentration gradient. At lower frequencies, the curves were straight at large reverse biases, indicating that the curve bending was probably a surface or interface effect. If it was a bulk effect, the whole curves would be bent. Since deep levels are intrinsic to semiconductors and should exist in the bulk, the curve bending should not be caused by deep levels. Therefore, it is likely that it was caused by interface or surface states. It can be seen that the curve bending was more severe for the non-annealed samples (Fig. 5.30), especially at low frequencies, probably due to the much higher densities of surface defect states. According to Sah et al. [5.21], a charge-trapping bandgap energy level has a time constant of

$$\tau_t = \frac{1}{c_n n}. \qquad (5.9)$$

Here, only the electron capturing is considered and C_n is the electron capturing rate of the bandgap and n is the electron density. With large reverse bias, the electron density at the interface is very small and the time constants of the bandgap states (surface states in this case) are large so that they cannot follow the small-signal voltage, especially at high frequencies, for the C-V measurements. However, with the depletion region shrinking toward the interface with smaller reverse biases, more electrons will be available for the surface states and their time constants will decrease. The surface states can then start to follow the small signal and contribute to the capacitance measurements, causing an increase in capacitance.

Besides the curve bending, a near parallel shift of the $1/C^2$-V plots can also be seen. This frequency dispersion of the C-V curves was quite common in $CuInSe_2$ devices [5.19,5.22-5.24] and was believed to be due to the presence of deep levels. Sah et al. [5.21] proved that such a frequency dispersion of the C-V curves was caused by discreet levels of bandgap states or deep levels in the bulk of the semiconductor. Deep-level transient spectroscopy was used to identify and characterize these levels in the $CuInSe_2$ substrates and the results will be shown in chapter 7.

Net acceptor concentrations of the $CuInSe_2$ substrates were calculated from the slope of the $1/C^2$-V plots using Eq. (5.8). High-frequency curves (1 MHz or 100 kHz) were used for the calculation because they were less affected by surface states. The straight $1/C^2$-V curve indicated that the net acceptor concentration is quite uniform for both the annealed and non-annealed cells. The concentrations obtained were in the order of 10^{17} cm^{-3}, which agree quite well to the values obtained from Hall-effect measurements. Although deep levels did not alter the slope of the $1/C^2$-V curves, the frequency dispersion makes it impossible to determine the built-in potential.

5.6 Conclusions

ZnO/CdS/$CuInSe_2$(bulk) solar cells with conversion efficiencies close to or more than 10 % have been routinely fabricated in the present work. The best cell showed an open-circuit voltage of 0.48 V, a short-circuit current density of 33.8 mA/cm^2, a fill factor of 0.71 and a conversion efficiency of 11.5 % under global AM 1.5 illumination. The best cells prepared in the present work are comparable in performance to, but with an area of up to an order of magnitude larger than, the highest-efficiency cell reported in the literature.

It has been demonstrated that a $CuInSe_2$ substrate annealing following the abrasive polishing and etching was instrumental in obtaining the high-efficiency ZnO/CdS/$CuInSe_2$ photovoltaic cells. The optimal annealing condition was determined to be 350 °C in Ar for two hours. The improvements by substrate annealing were mainly in V_{oc} and fill factor, while no apparent gain was observed in J_{sc}. The improvements of V_{oc} and fill factor were probably due to the change of current mechanism from multiple tunneling through surface defect states in non-annealed samples to discrete deep-level assisted tunneling in annealed samples. Spectral response measurements showed the need of an improvement in the quality of CdS films and an antireflection coating to improve the short-circuit current density. Furthermore, a smaller net acceptor concentration of the $CuInSe_2$ substrates should also improve the device performance. Capacitance measurements indicated the strong effect of interface or surface states, especially for the non-annealed samples. High frequency was required to reduce such surface effect. Net acceptor concentration was observed to be quite uniform at the $CuInSe_2$ surface for both the non-annealed and annealed cells.

Table 5.1 Experimental results showing the effect of substrate annealing.

Sample no.	Ingot no.	Substrate annealing*	V_{oc} (V)	J_{sc} (mA/cm^2)	F.F.	Efficiency (%)
D-106	LS-42	no	0.23	19.2	0.42	1.85
D-101	LS-42	yes	0.44	28.0	0.67	8.25
D-38	LS-51	no	0.42	30.5	0.63	8.0
D-39	LS-51	yes	0.47	32.8	0.67	10.3

* 350 °C in Ar for 2 hours

Table 5.2 Photovoltaic characteristics of ZnO/CdS/$CuInSe_2$ solar cells.

Sample No.	Active Area (mm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	F.F.	Efficiency (%)
D-102	4	0.48	33.8	0.71	11.5
D-105#	4	0.48	32.4	0.69	10.7
D-39*	8	0.47	32.8	0.67	10.3
D-44	4	0.45	32.1	0.69	10.0
D-37*	8	0.45	31.3	0.68	9.6
D-32	8	0.43	31.9	0.65	8.9
D-29*	8	0.45	29.8	0.65	8.7
D-94	4	0.42	30.5	0.67	8.6
D-101	4	0.44	28.0	0.67	8.3
D-100	3.8	0.43	27.3	0.68	8.0

All $CuInSe_2$ substrates were annealed at 350 °C in Ar for 2 hrs except D-105, which was annealed in H_2.
* Cell performances measured under the sun at noon.

Table 5.3 Comparison of two cells fabricated in the present work with the best single-crystal and thin-film cells reported in the literature.

Sample No.	Active Area (mm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	F.F.	Efficiency (%)
D-102[&]	4	0.48	33.8	0.71	11.5
D-39[&]	8	0.47	32.8	0.67	10.3
SC-cell[*]	0.79	0.5	~38.0	0.6	12[†]
TF-cell[#]	-	0.515	41.2	0.726	15.4

& No antireflection coating was used for these two cells.

* Best single-crystal $CuInSe_2$ cell reported by Shay et al. [1.3]. Fabricated on a cleaved (112) $CuInSe_2$ surface. Antireflection coating was used.

† The efficiency of the same cell without antireflection coating was 10.6 %.

Best thin-film $CuInSe_2$ cell reported by Hedstrom et al. [1.13]. Antireflection coating was used.

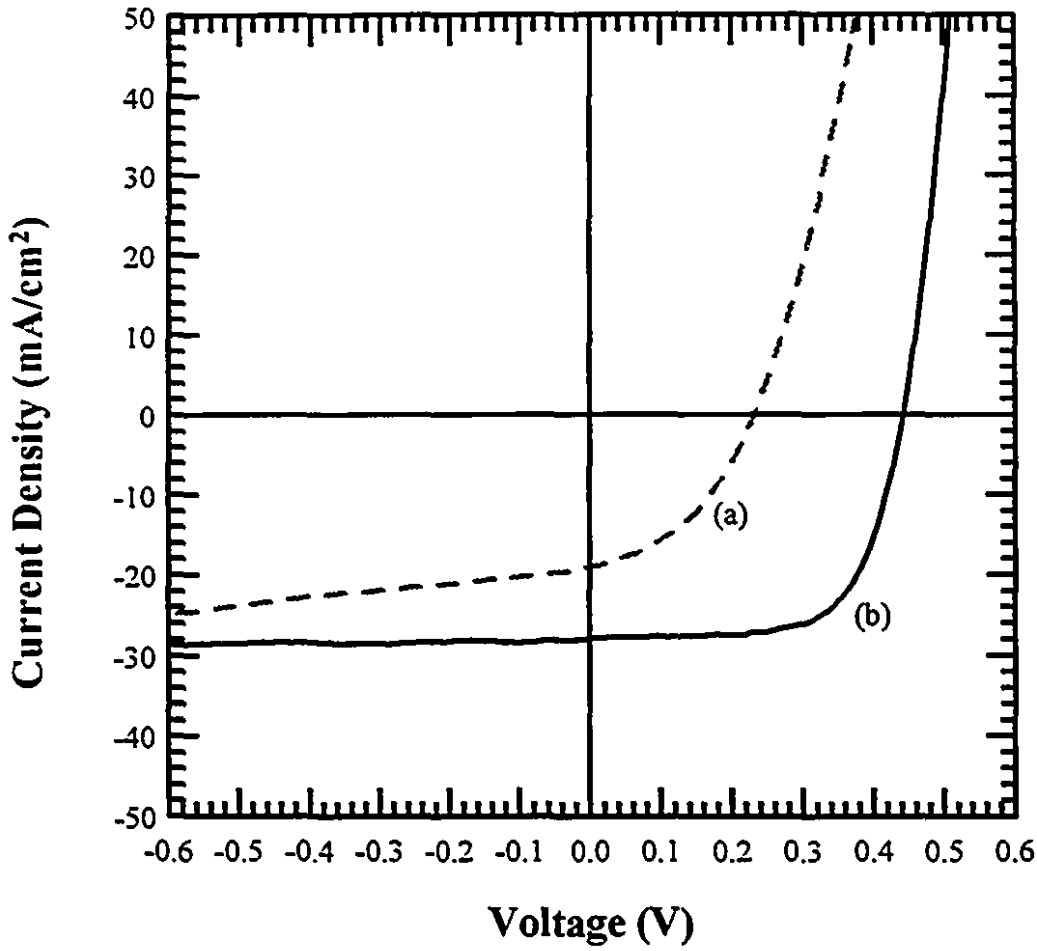


Fig. 5.1 Illuminated I-V characteristics of two ZnO/CdS/$CuInSe_2$ cells. (a) This cell, D-106, was fabricated without any substrate annealing. (b) The substrate of this cell, D-101, was annealed at 350 °C in Ar for 2 hours.

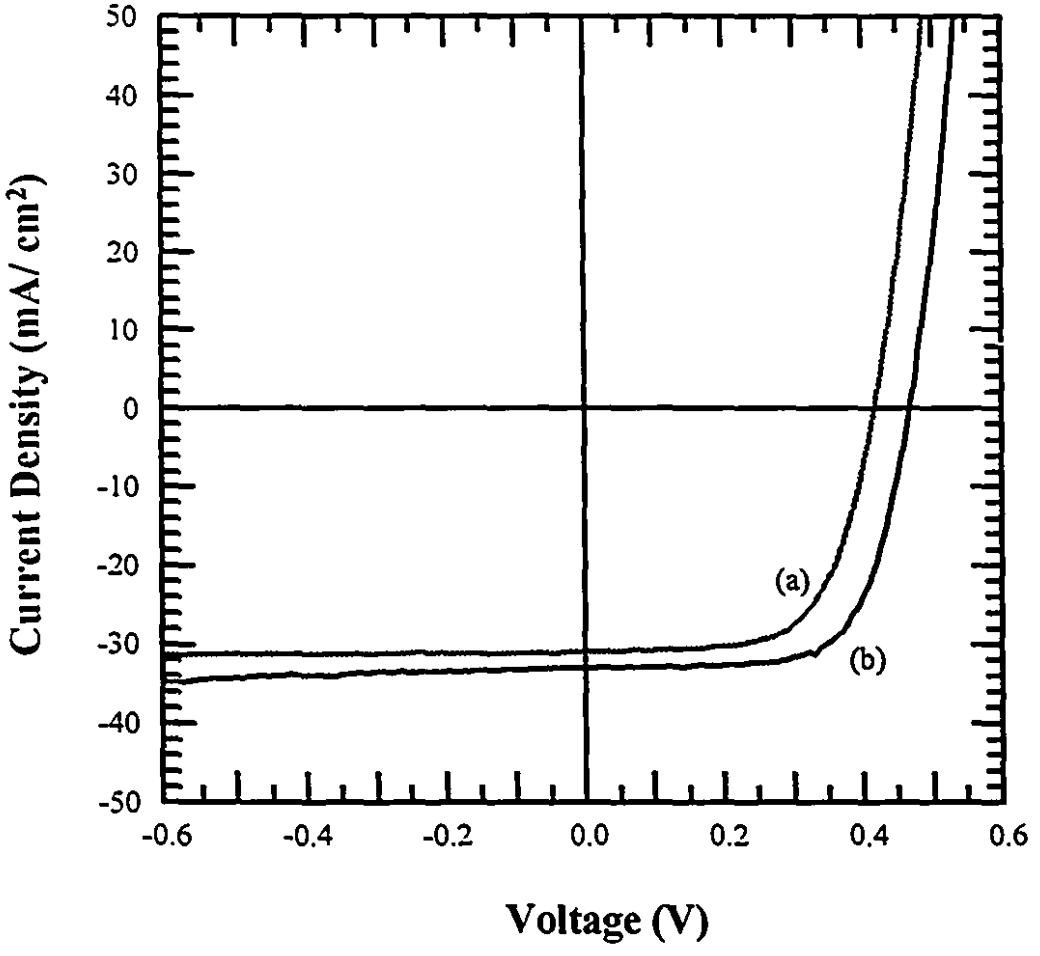


Fig 5.2 Another plot showing the effect of substrate annealing on photovoltaic performance. (a) Cell D-38 was fabricated without substrate annealing. (b) Cell D-39 was fabricated with substrate annealing at 350 °C in Ar for 2 hours.

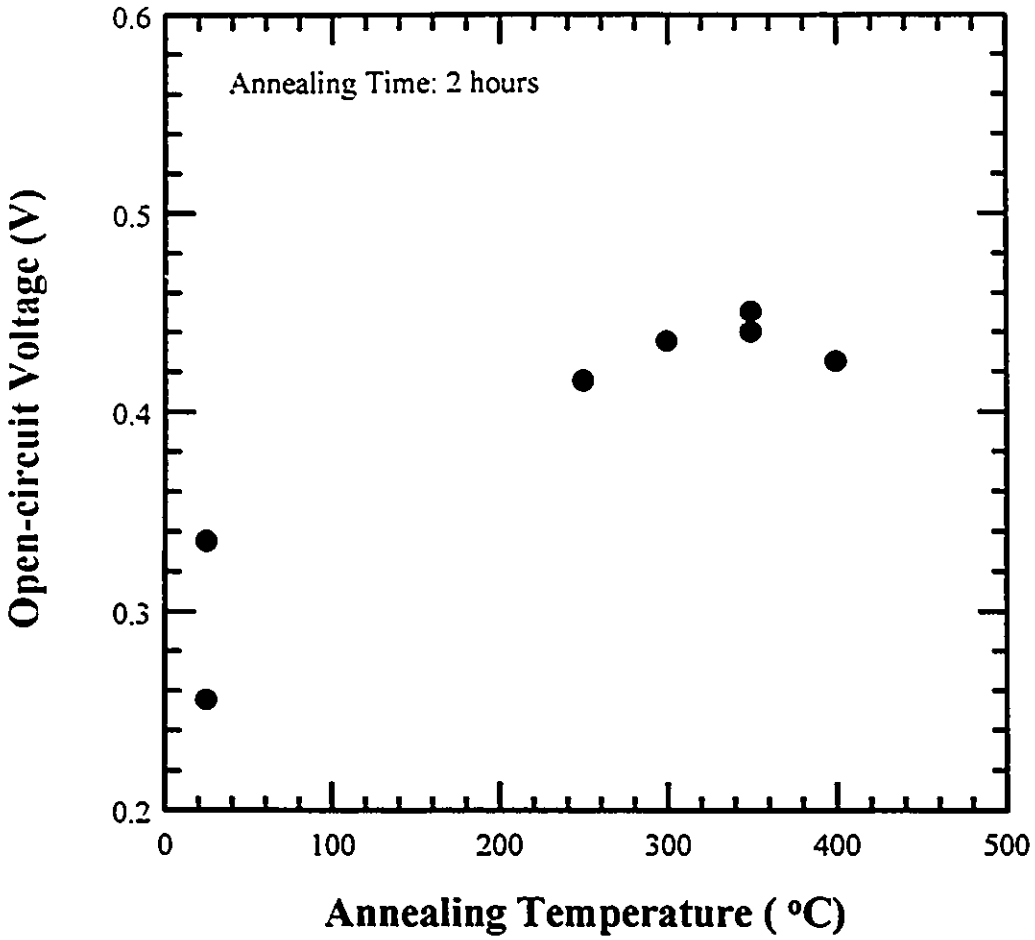


Fig. 5.3 Effect of substrate annealing temperature on open-circuit voltage.

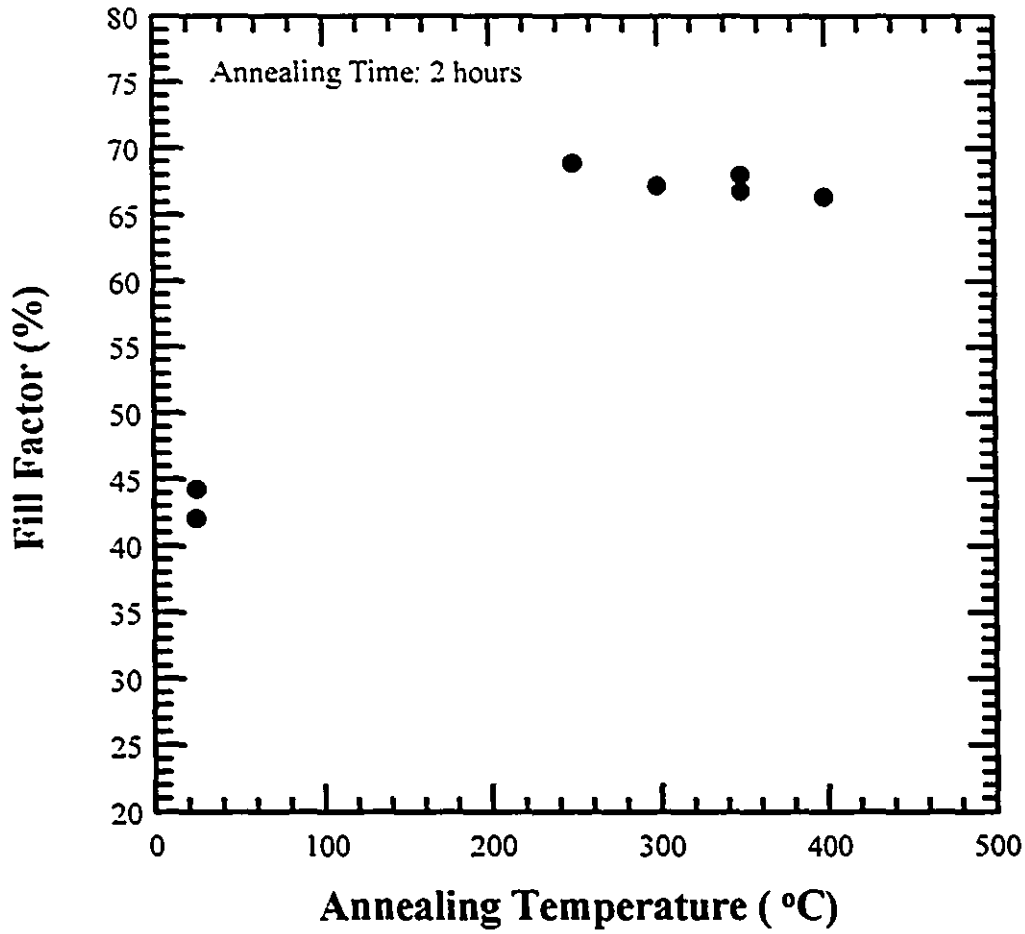


Fig. 5.4 Effect of substrate annealing temperature on fill factor.

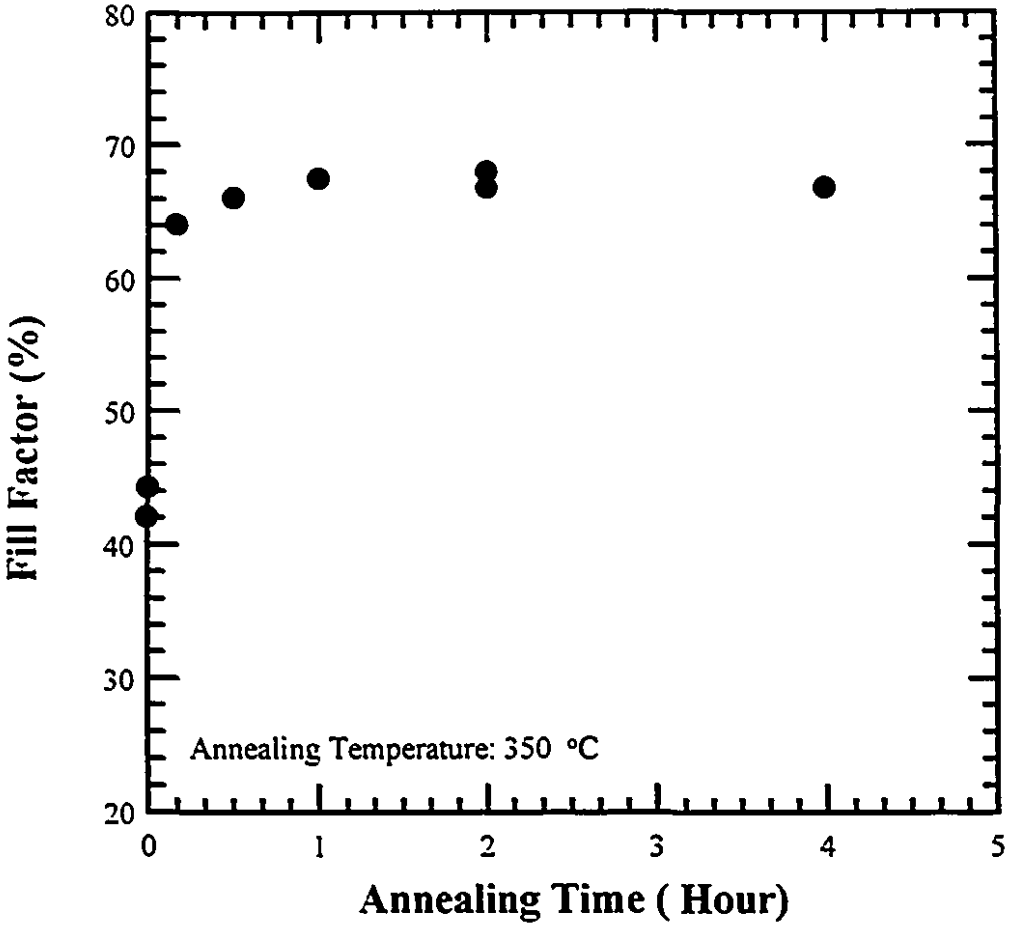


Fig. 5.5 Effect of substrate annealing time on fill factor.

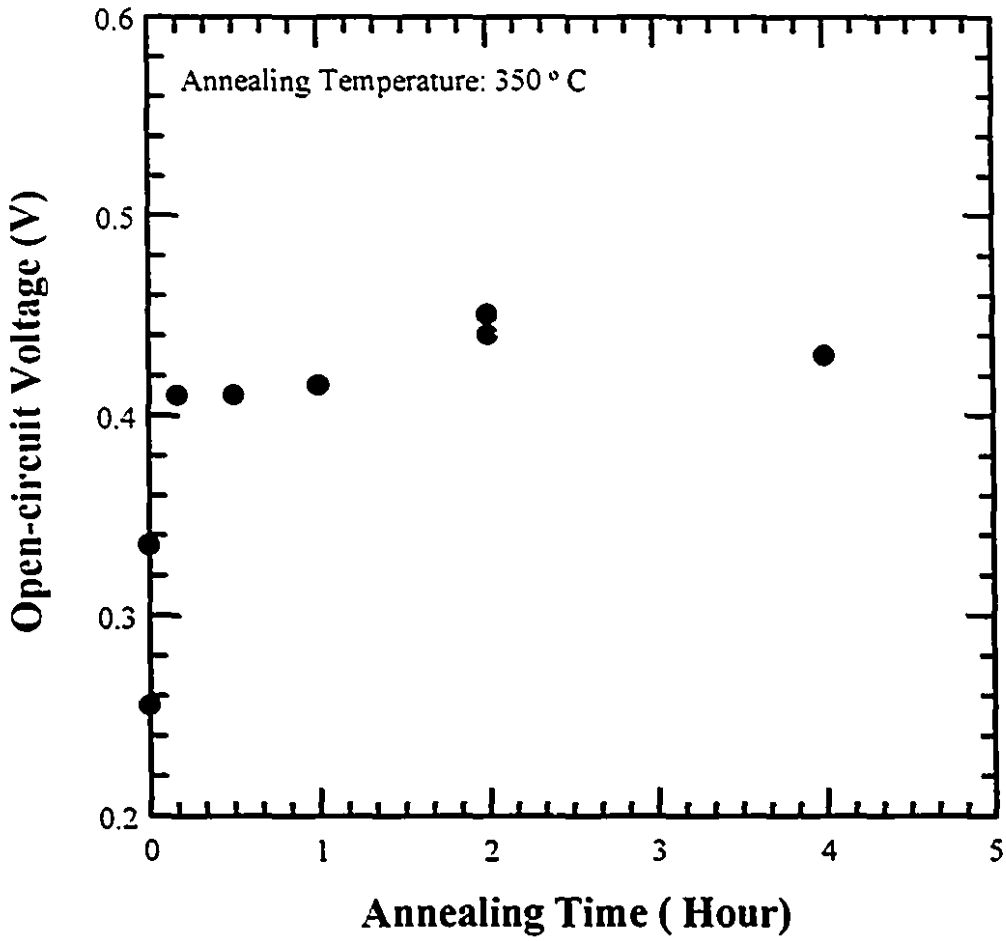


Fig. 5.6 Effect of substrate annealing time on open-circuit voltage.

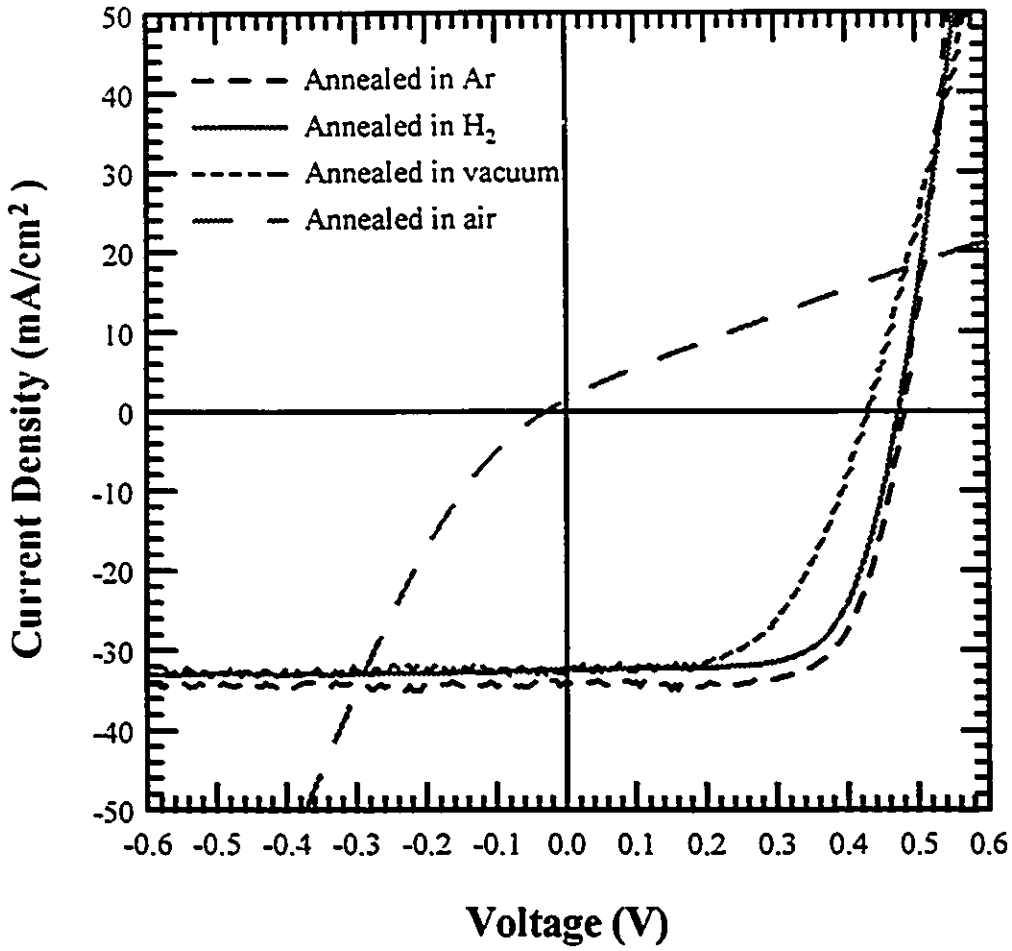


Fig. 5.7 Illuminated I-V characteristics of four cells with substrates annealed in different gaseous environments.

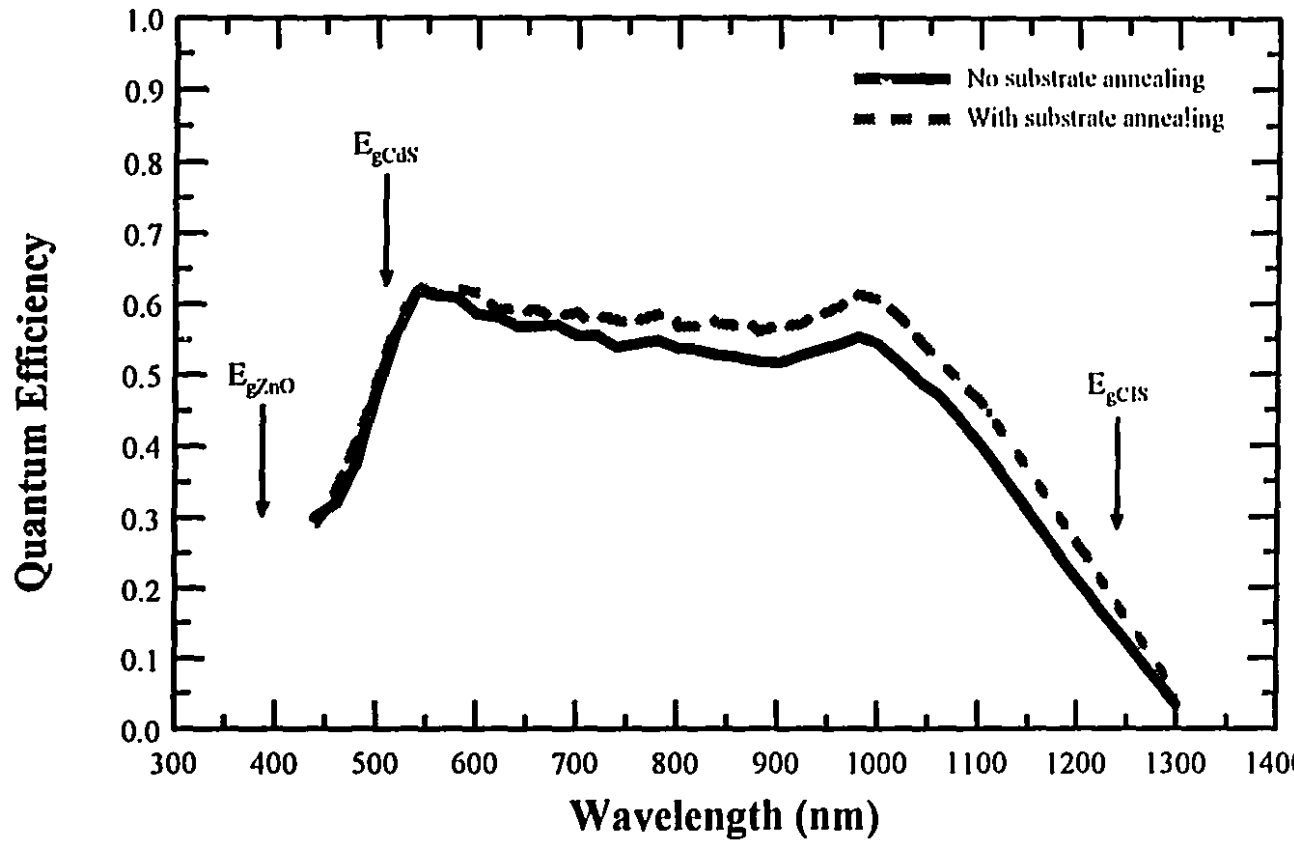


Fig. 5.8 Spectral responses of two cells, one with substrate annealing and one without.

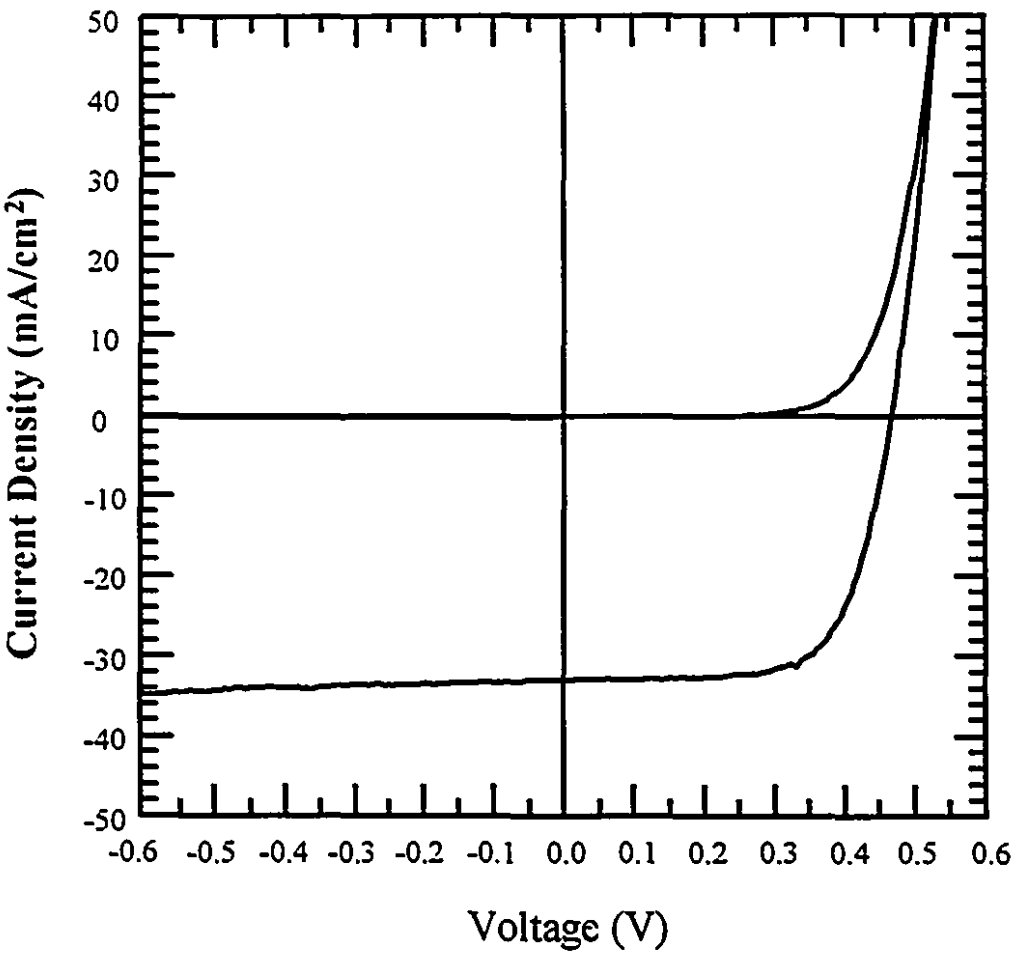


Fig. 5.9 Illuminated and dark I-V characteristics of cell D-39.

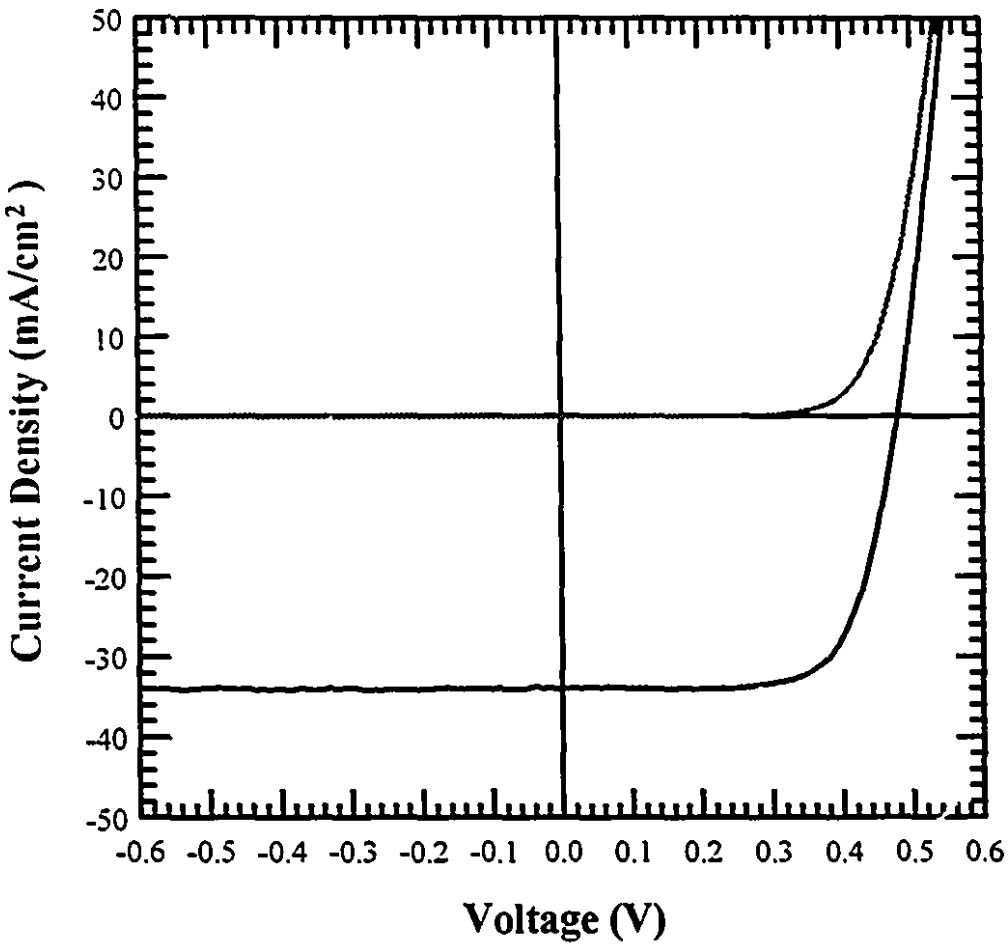


Fig. 5.10 Illuminated and dark I-V characteristics of cell D-102.

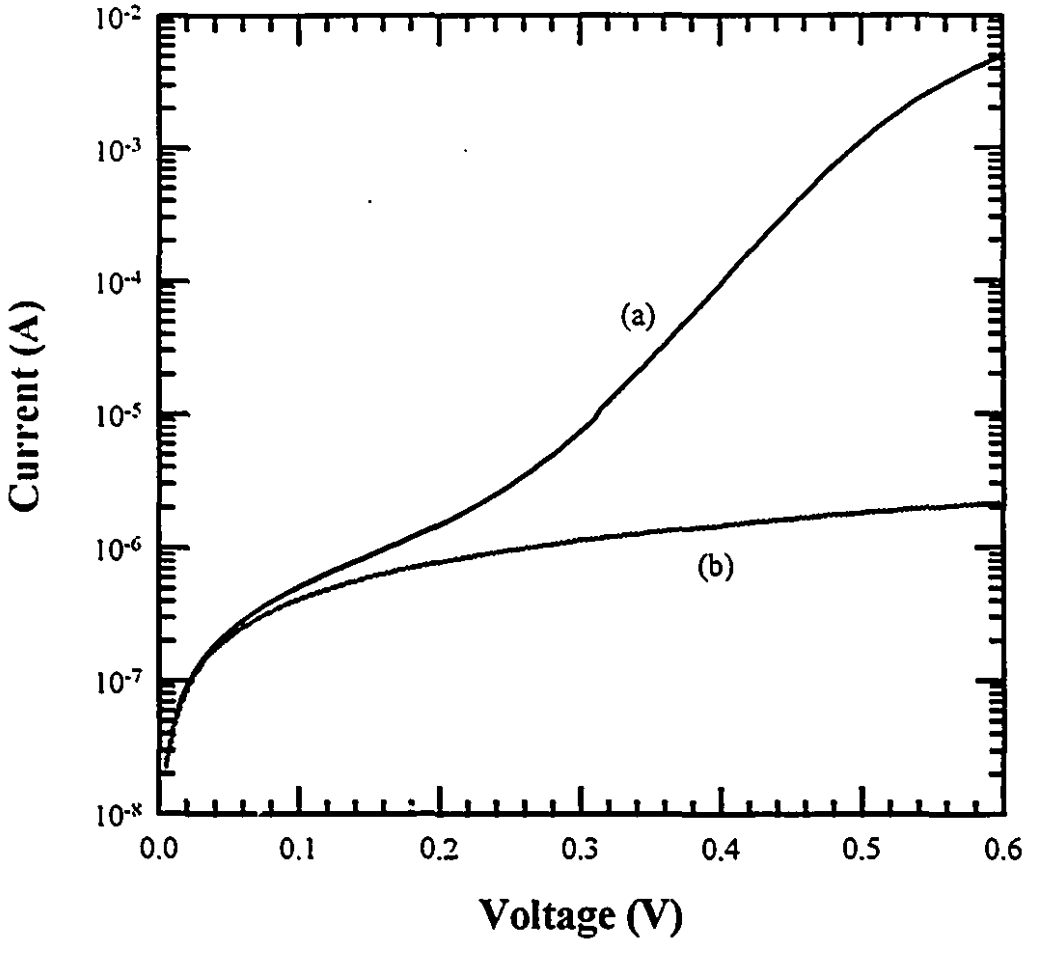


Fig. 5.11 Log I-V plot of cell D-102. Both the forward, (a), and reverse, (b), currents are shown.

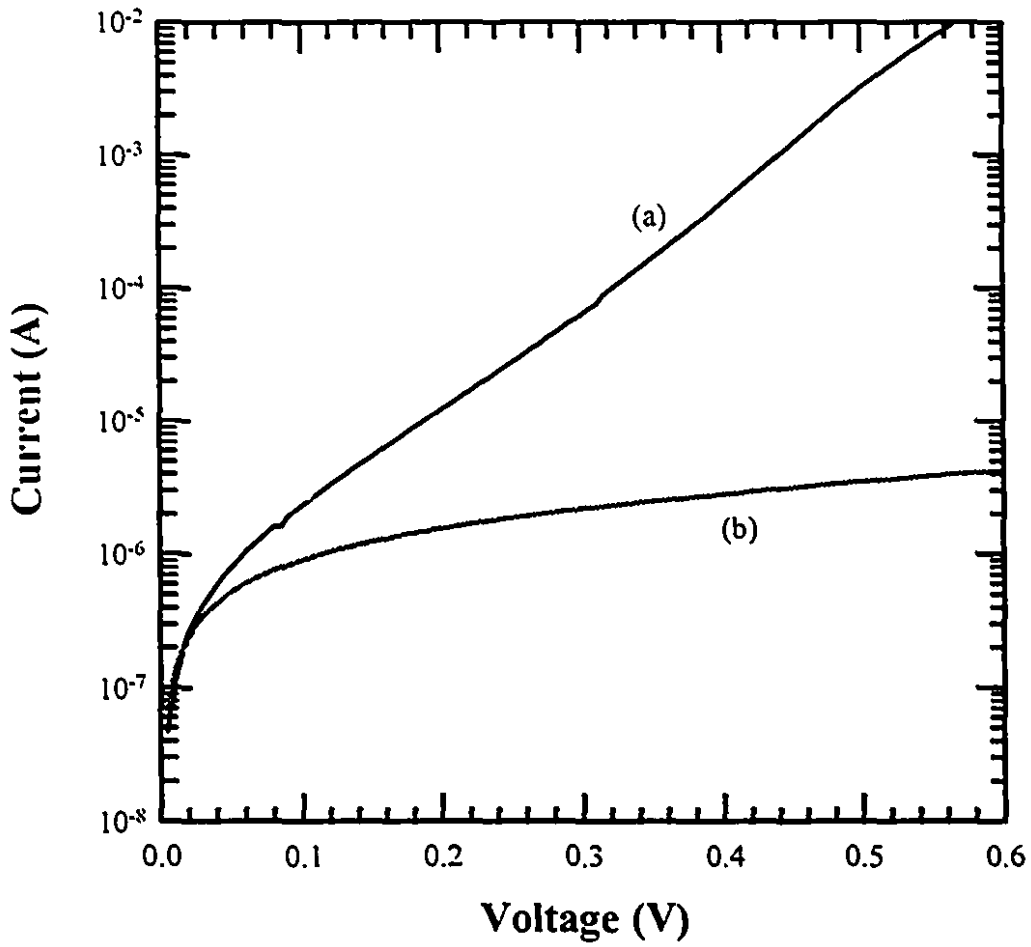


Fig. 5.12 Log I-V plot of cell D-39. Both the forward, (a), and reverse, (b), currents are shown.

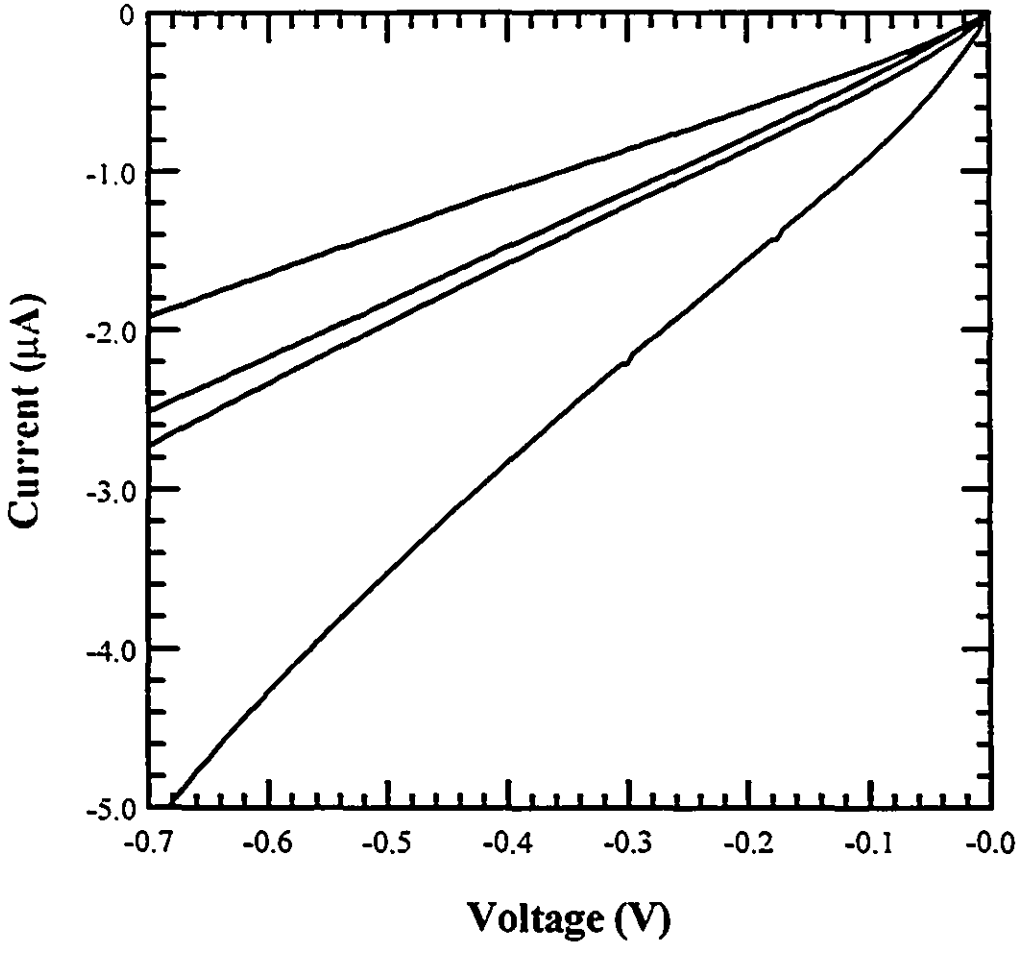


Fig. 5.13 Reverse currents of four cells showing a near linear relationship with reverse voltages.

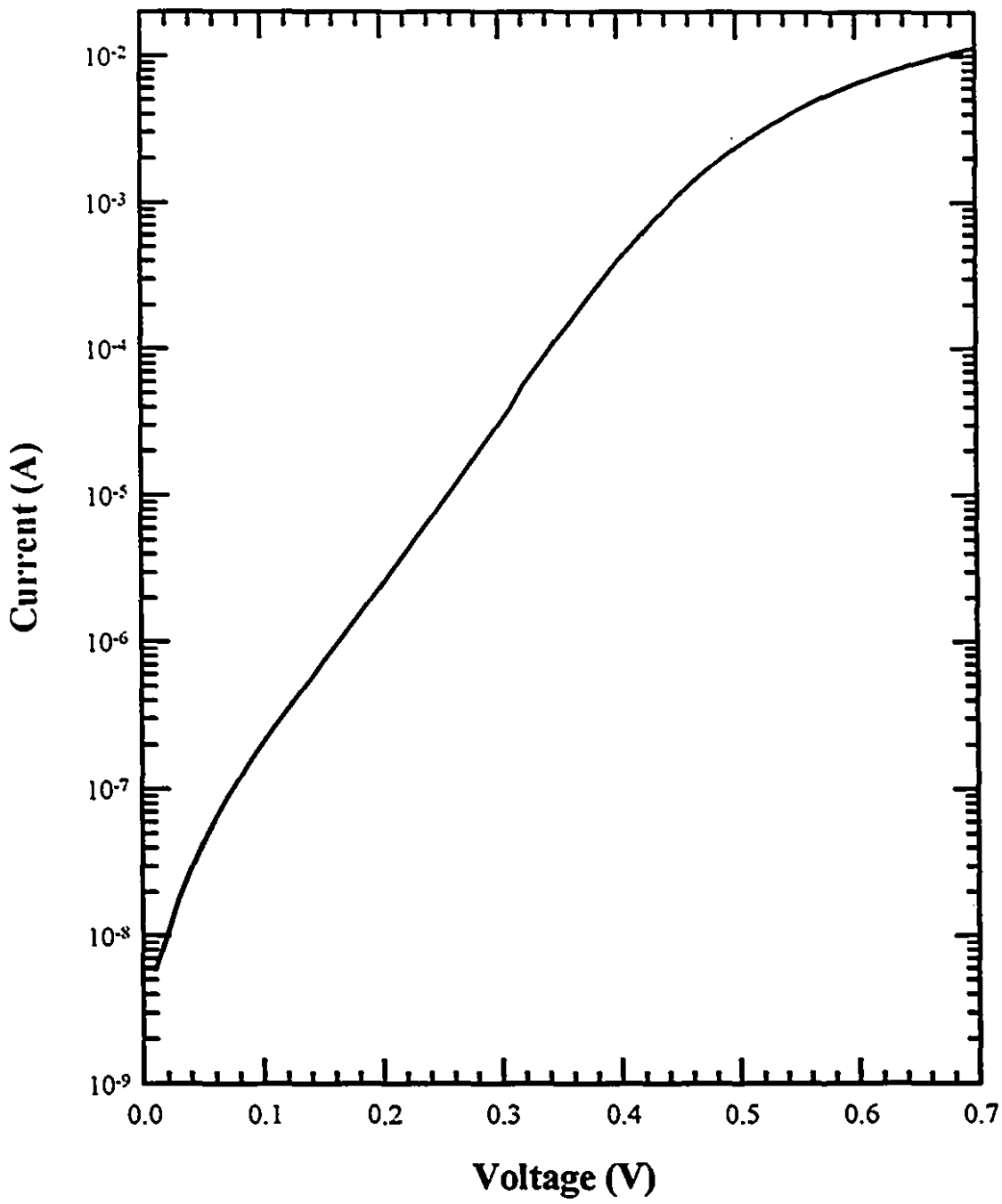


Fig. 5.14 An exponential plot of the forward current against forward voltage for the cell D-100. The forward current was corrected for shunt resistance and showed only a single slope from 0.1 to 0.45 V.

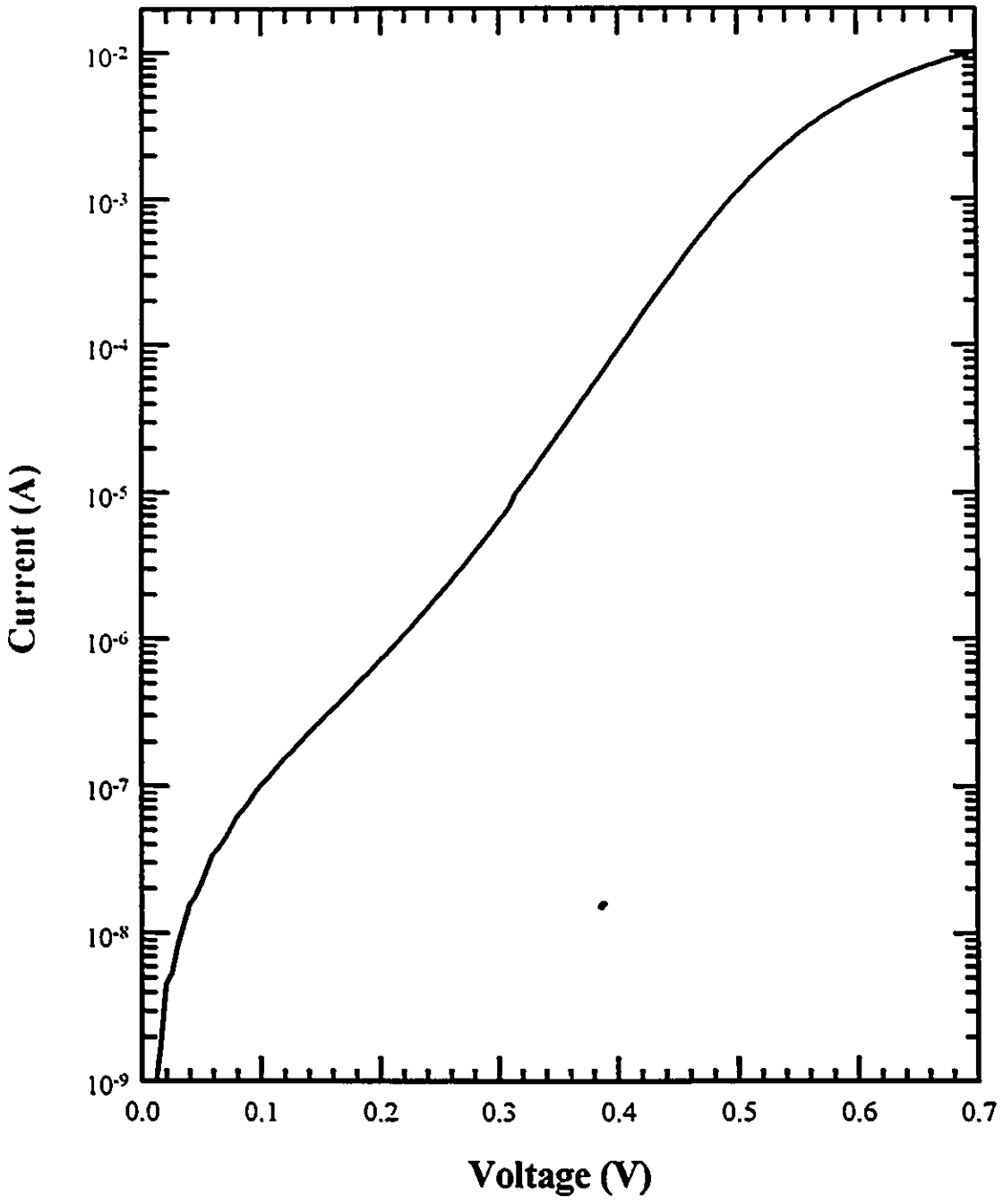


Fig. 5.15 An exponential plot of the forward current against forward voltage for the cell D-102. The forward current was corrected for shunt resistance but a second slope at low voltages (0.1 to 0.3 V) can be seen.

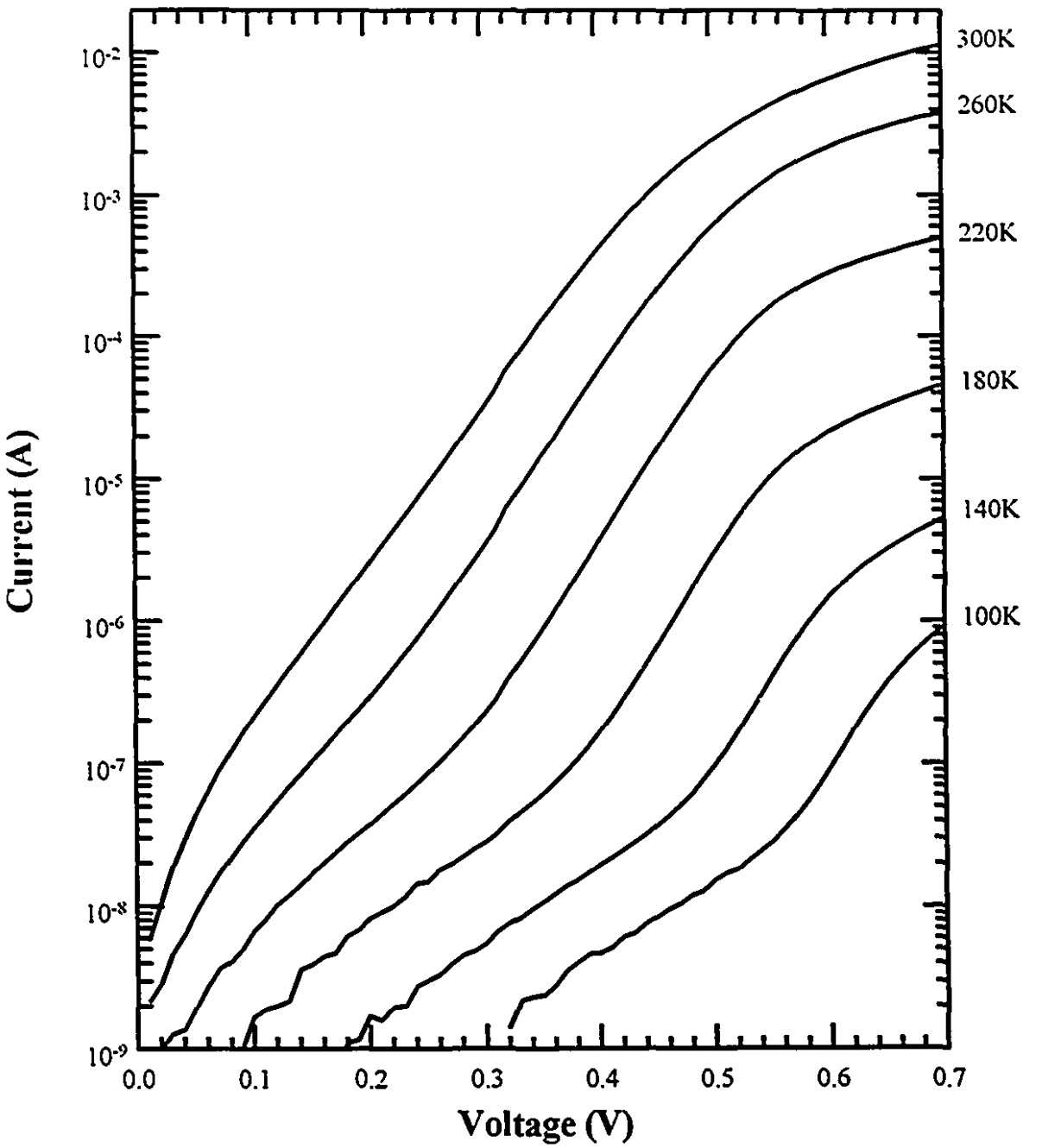


Fig. 5.16 Temperature-dependent I-V characteristics of cell D-100.

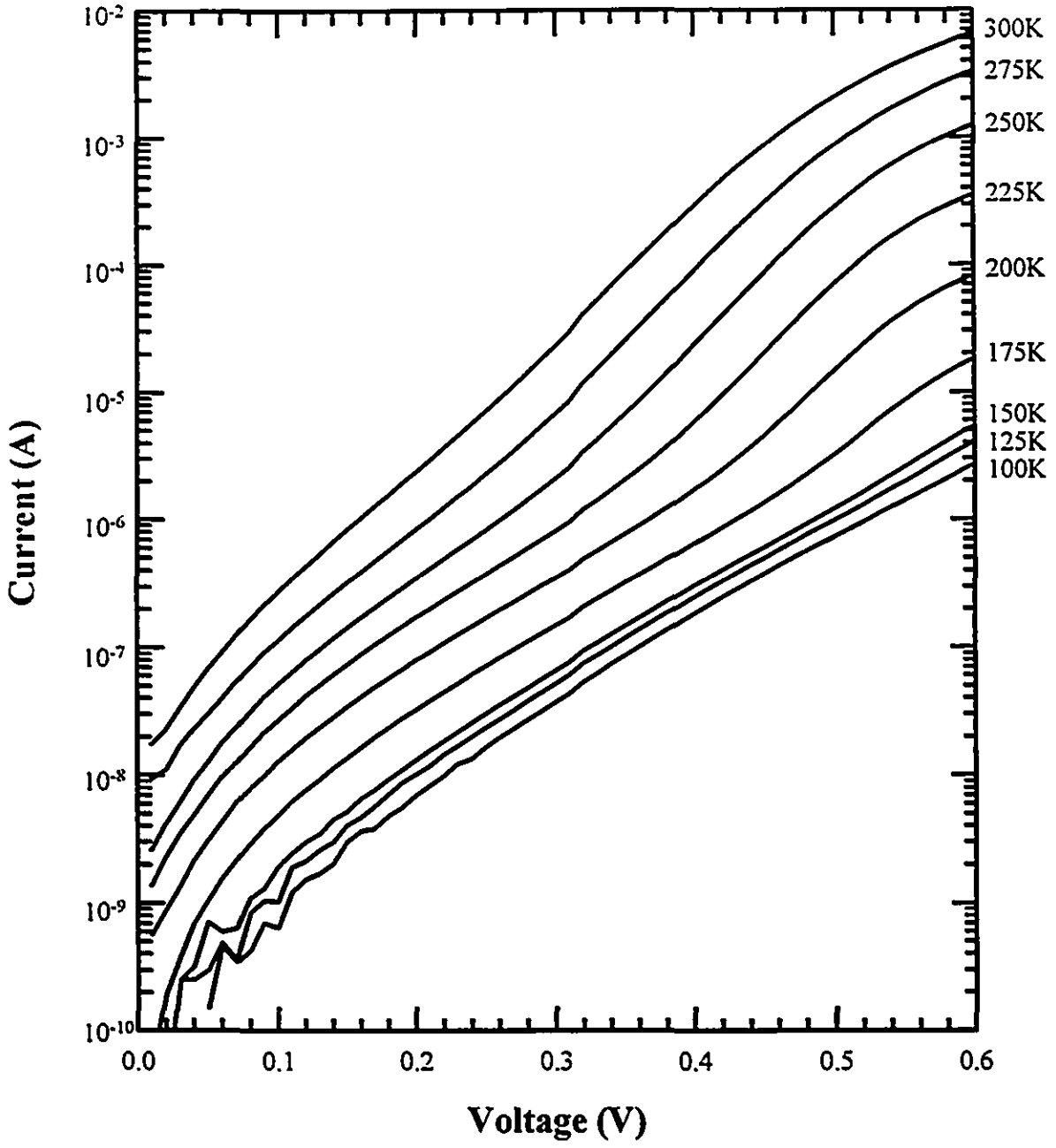


Fig. 5.17 Temperature-dependent I-V characteristics of cell D-101.

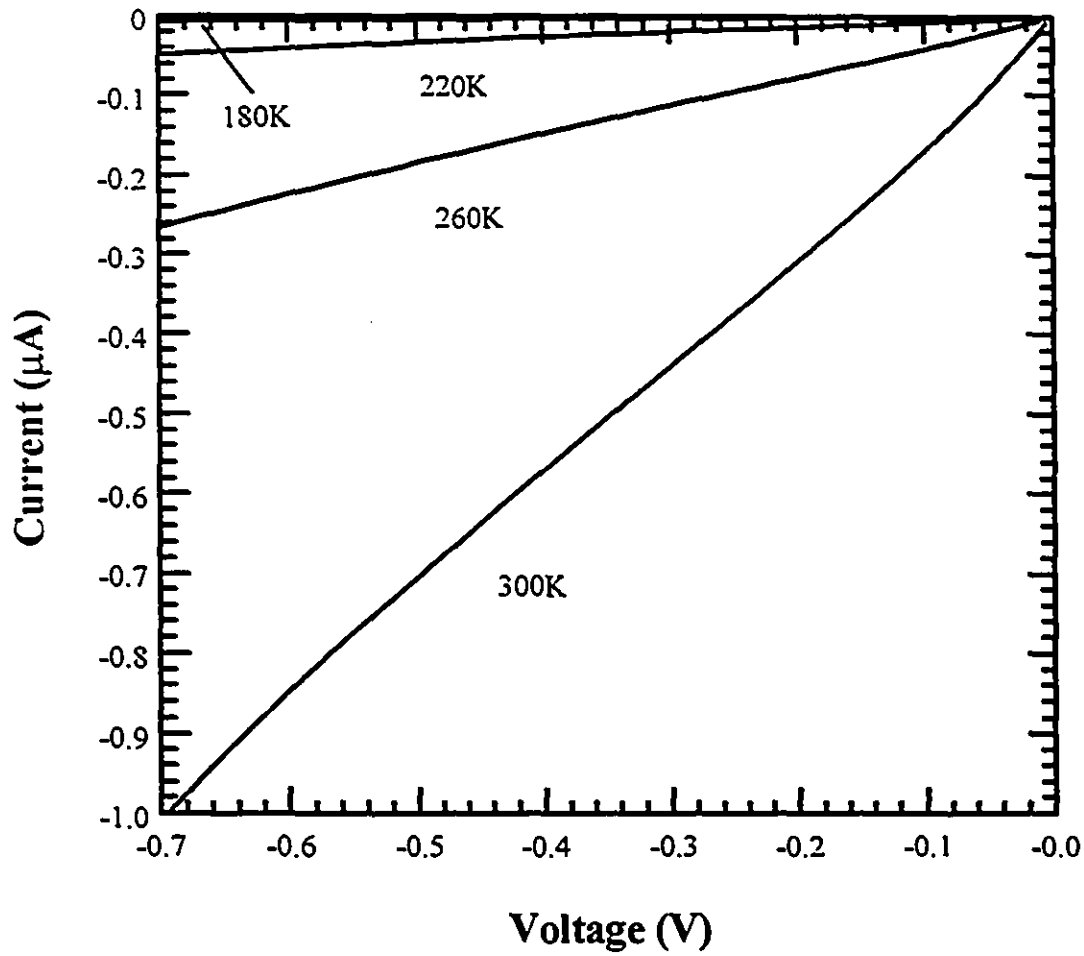


Fig. 5.18 Reverse I-V characteristics of the cell D-100 measured at different temperatures.

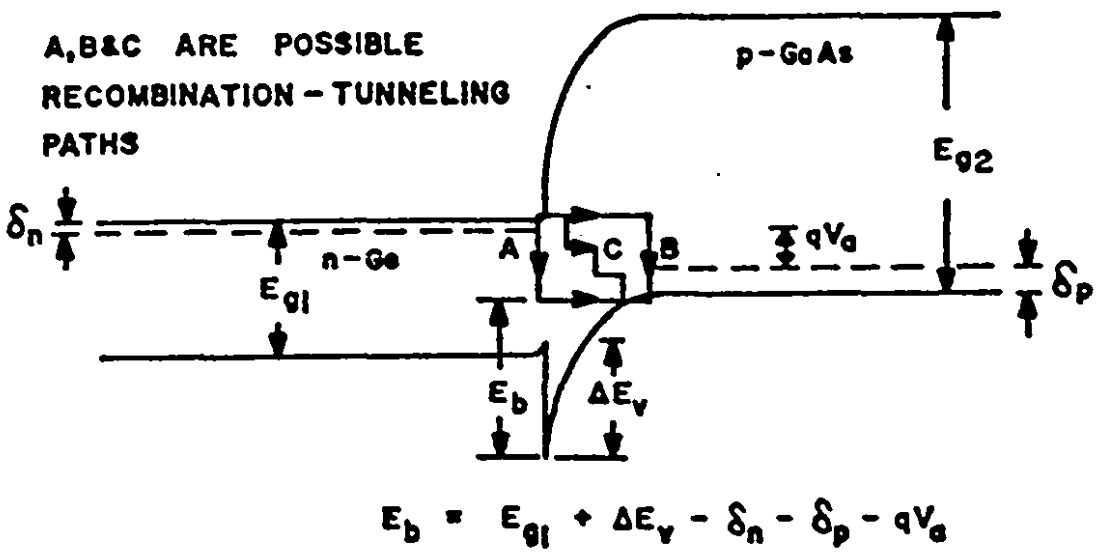


Fig. 5.19 Tunneling model proposed by Riben and Feucht [5.3] for a n Ge-p GaAs heterojunction. V_a is the applied forward bias and E_b is the tunneling barrier height.

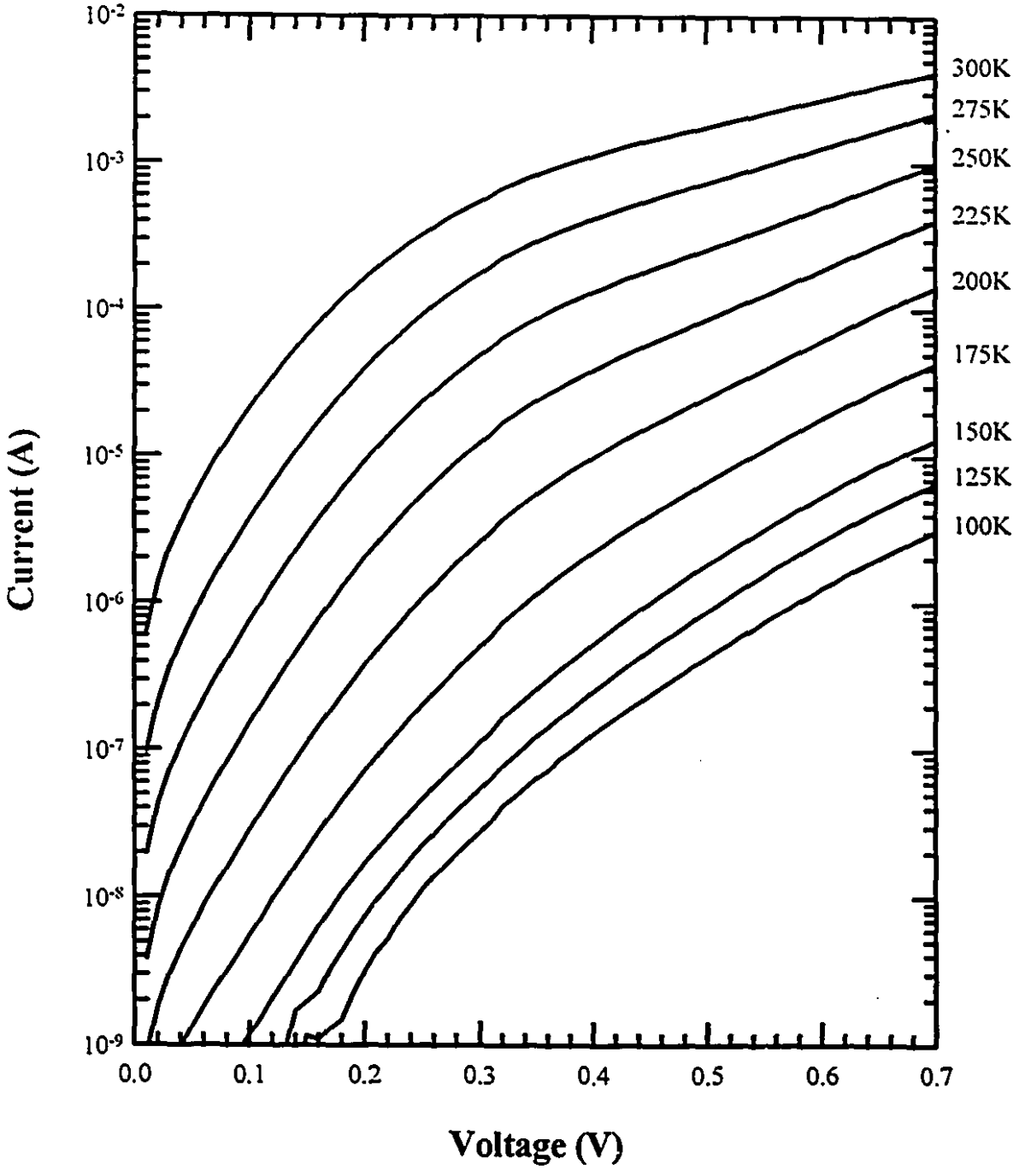


Fig. 5.20 Temperature-dependent I-V characteristics of a non-annealed cell (D-106).

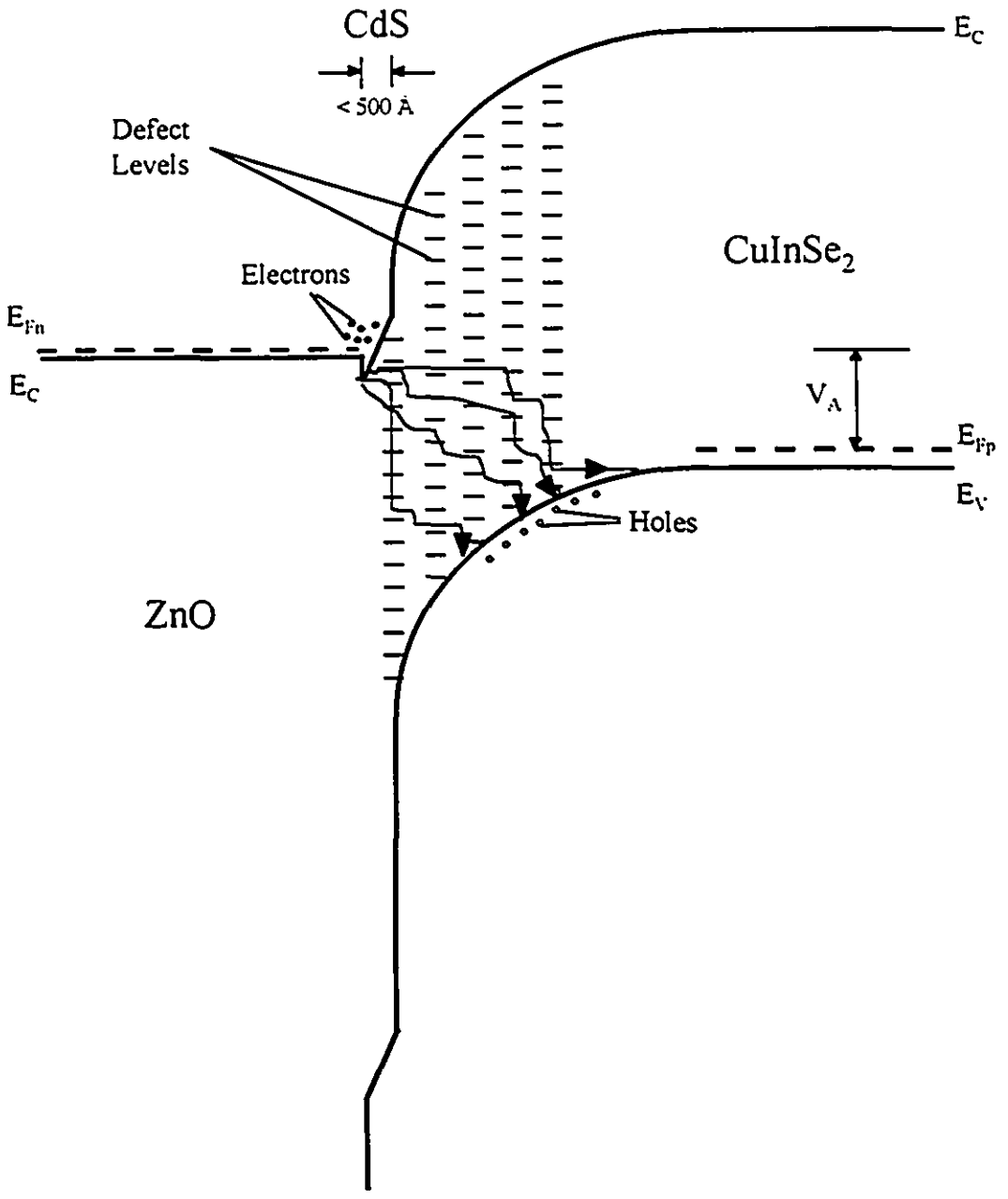


Fig. 5.21 A current mechanism model of multiple tunneling through surface states in $CuInSe_2$ for non-annealed samples.

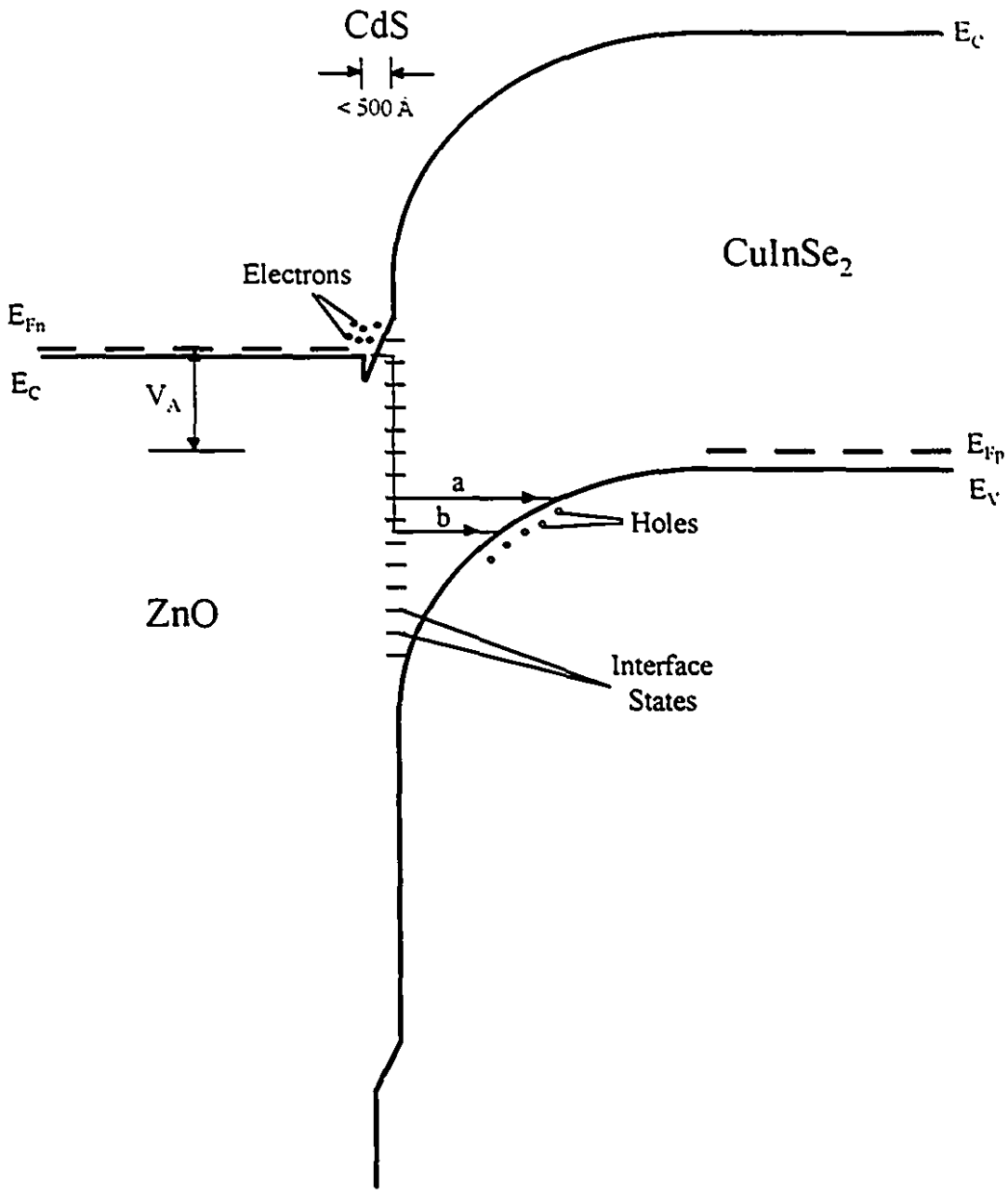


Fig. 5.22 (a) A current mechanism model of tunneling through interface states for annealed samples.

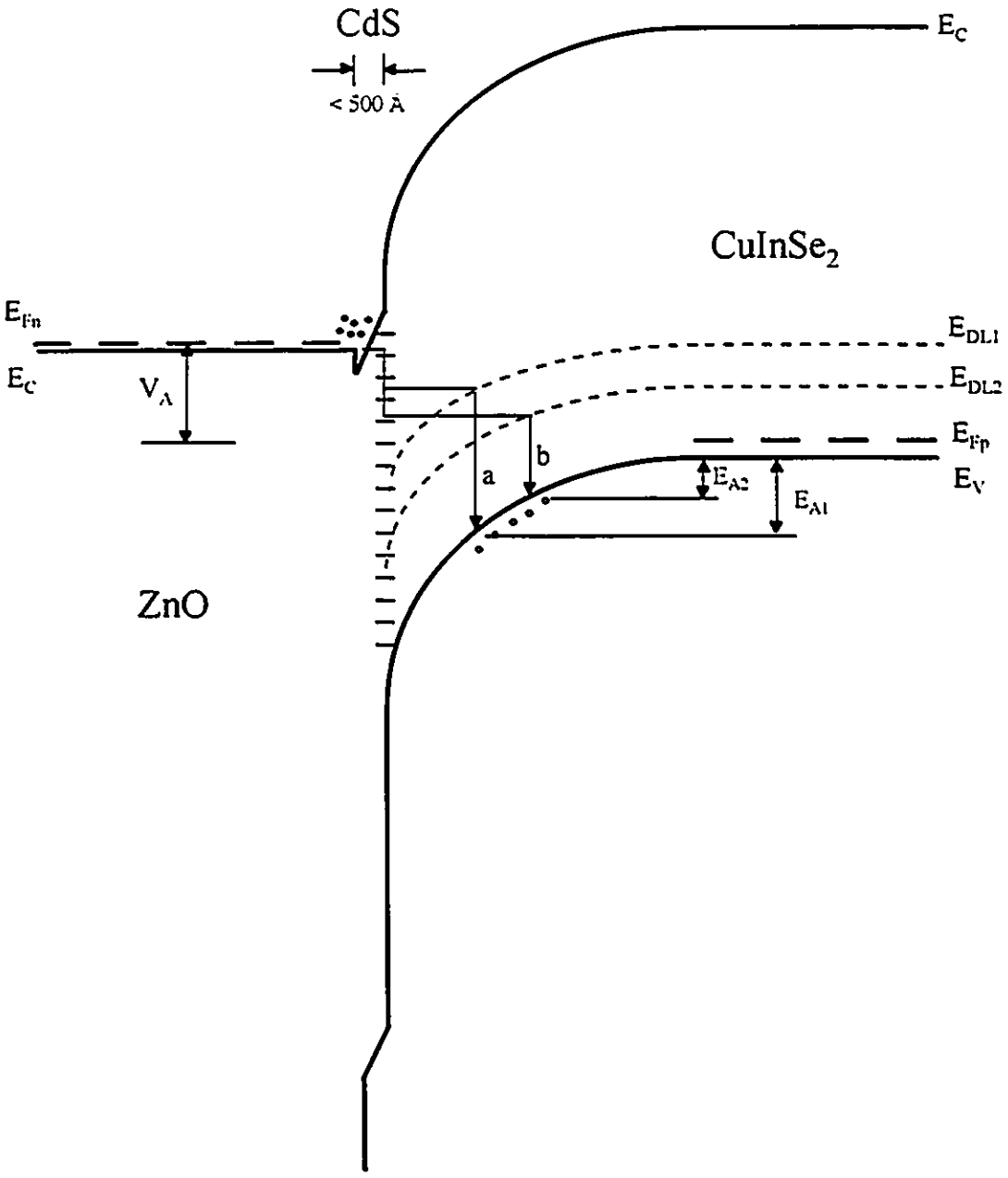


Fig. 5.22 (b) A current mechanism model of tunneling through deep-level states for annealed samples. E_{DL1} and E_{DL2} are the energy of the deep levels.

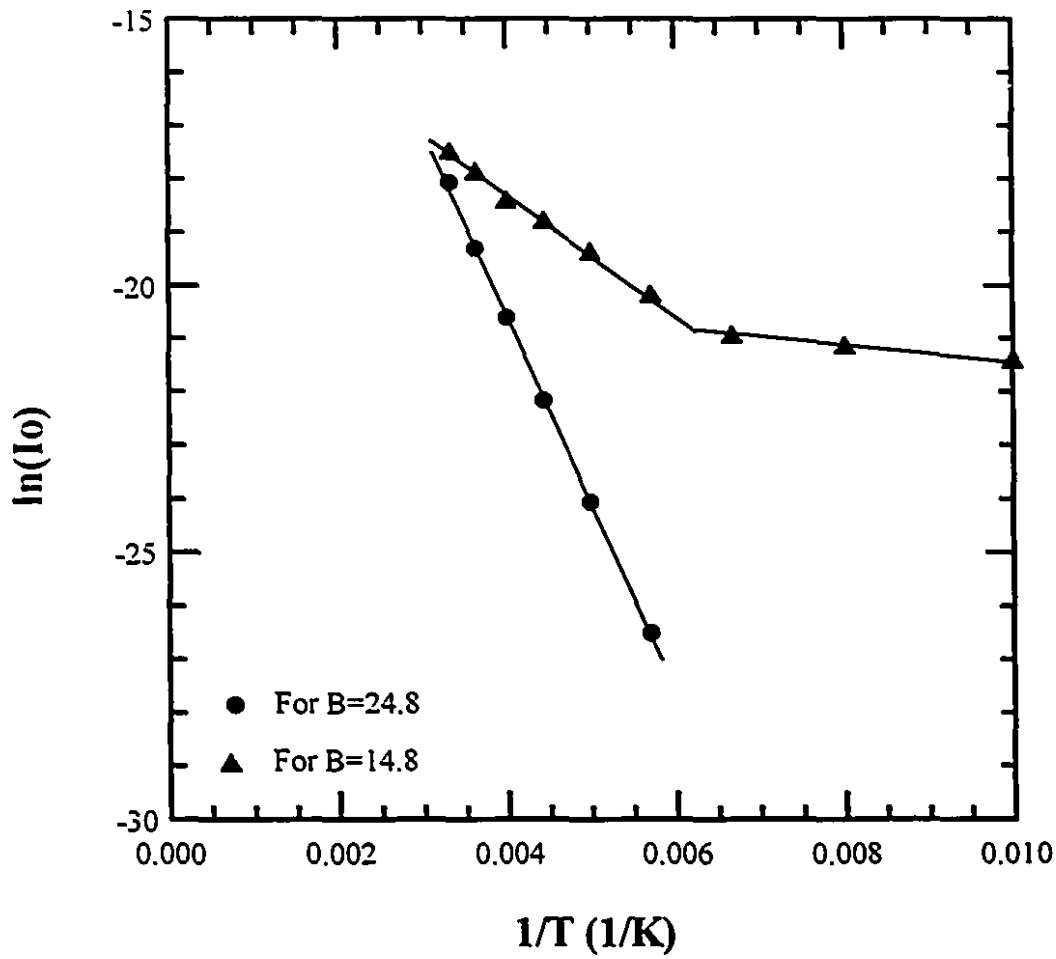
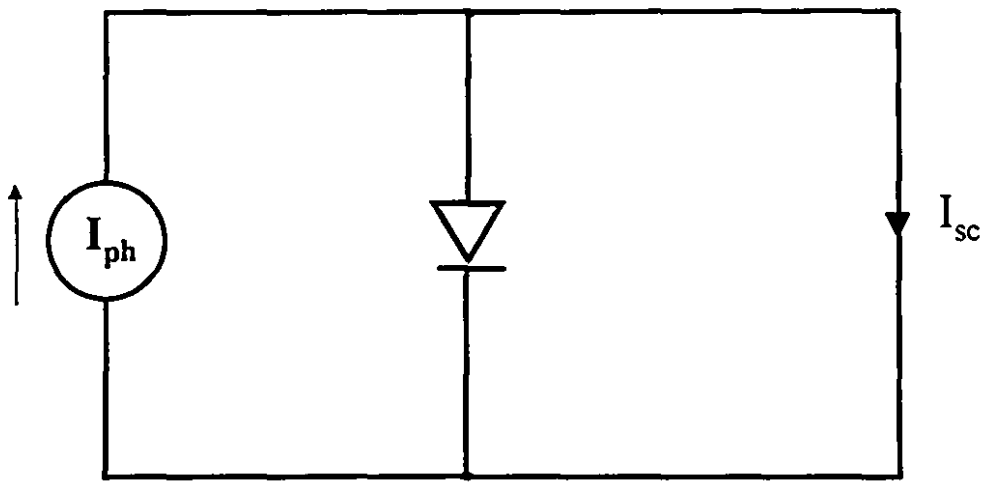
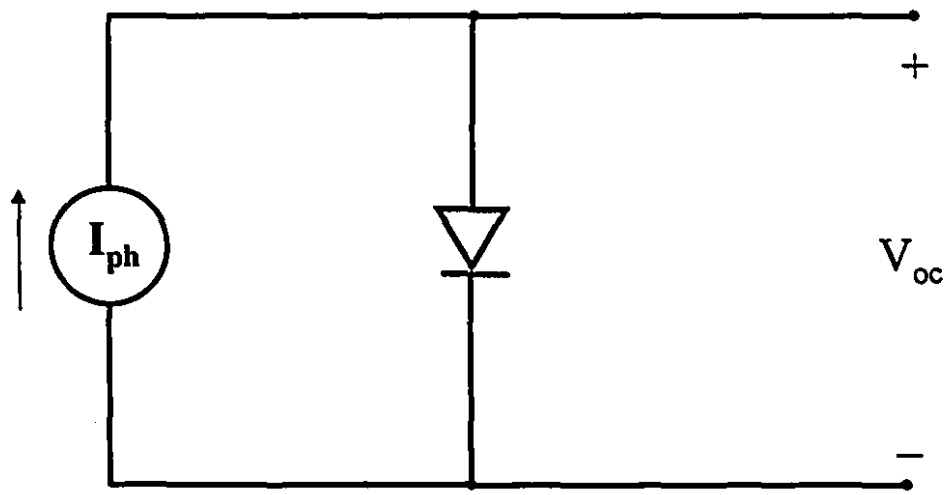


Fig. 5.23 A plot of the $\ln(I_o)$ vs 1/T for the cell D-101.



(a)



(b)

Fig. 5.24 Equivalent circuits for the (a) short-circuit and (b) open-circuit conditions. Shunt and series resistances are omitted.

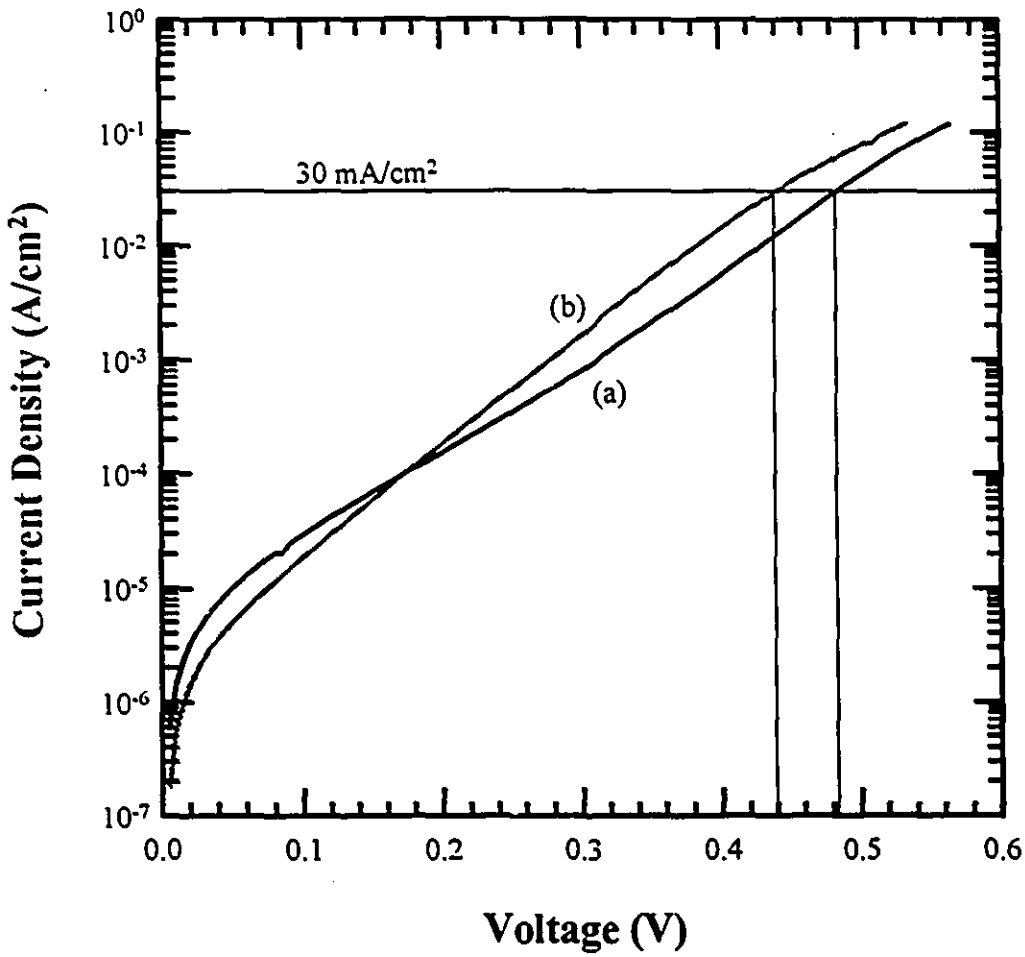


Fig. 5.25 A comparison of the dark I-V characteristics of two similar cells, one with substrate annealing (a) and one without (b). A hypothetical photocurrent of 30 mA/cm^2 would yield an open-circuit voltage of 0.48 V for cell (a) and 0.44 V for cell (b).

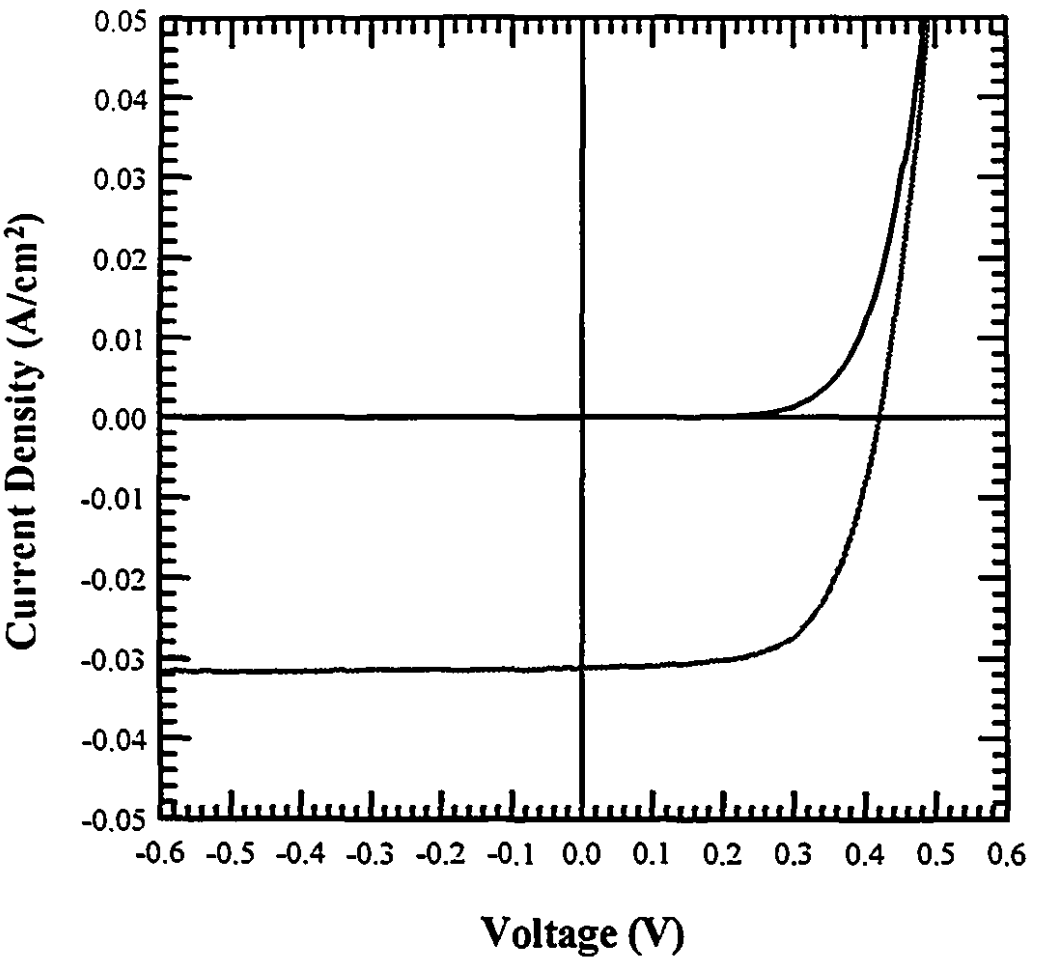


Fig. 5.26 Dark and illuminated I-V characteristics of a non-annealed cell (D-38).

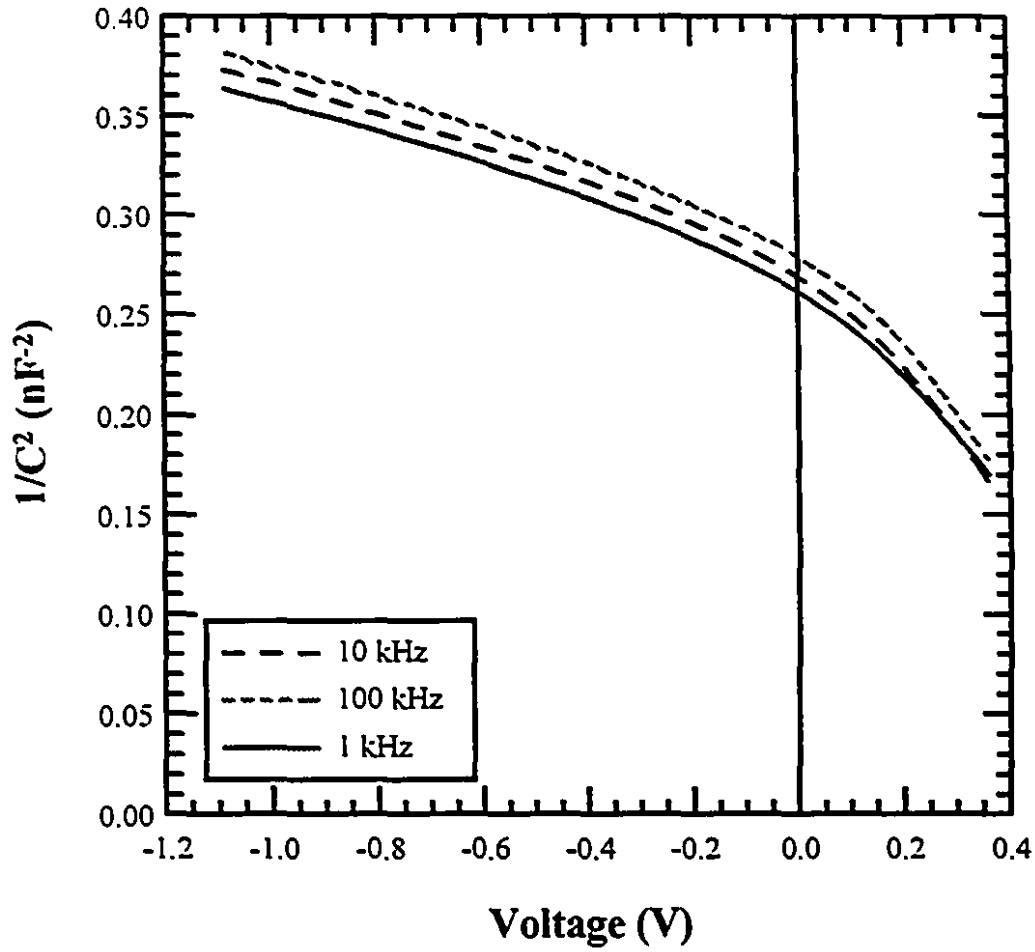


Fig. 5.27 A plot of $1/C^2$ vs voltage for the cell D-102 at three different frequencies.

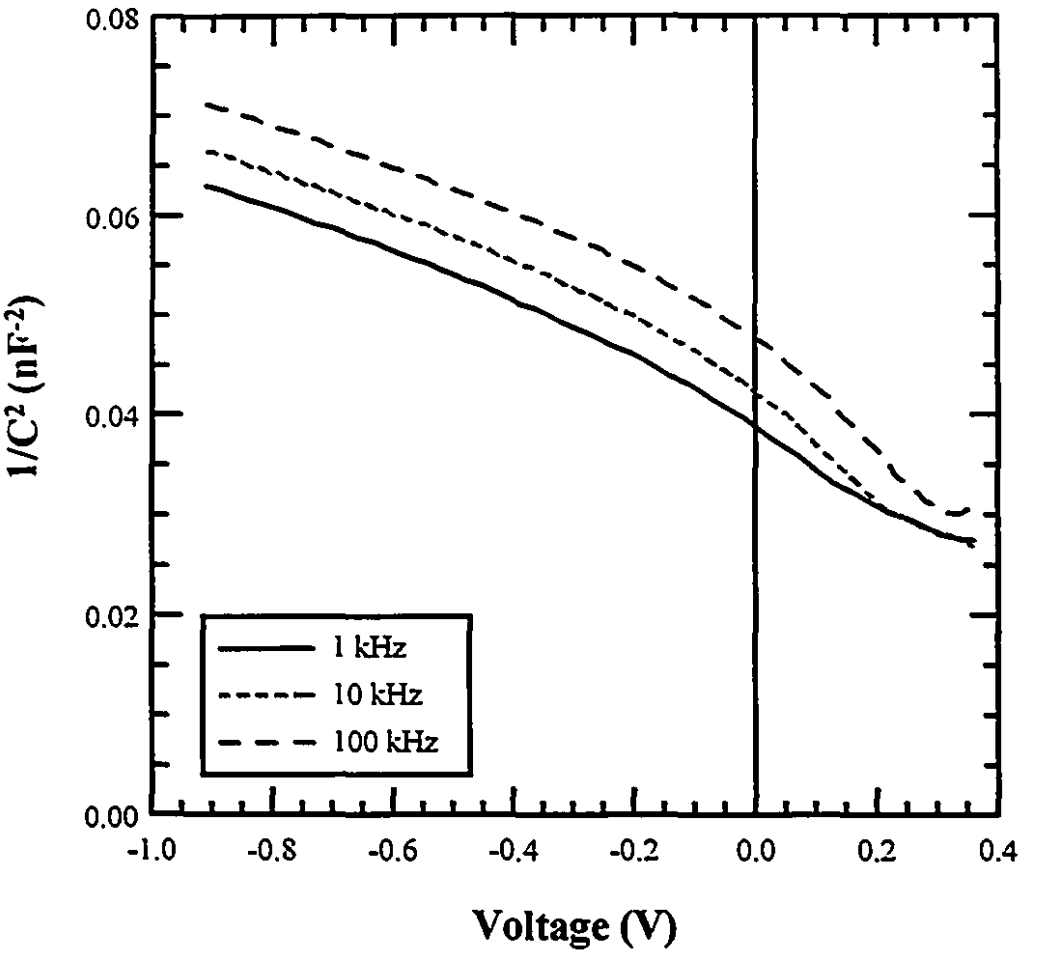


Fig. 5.28 A plot of $1/C^2$ vs voltage for the cell D-32 at three different frequencies.

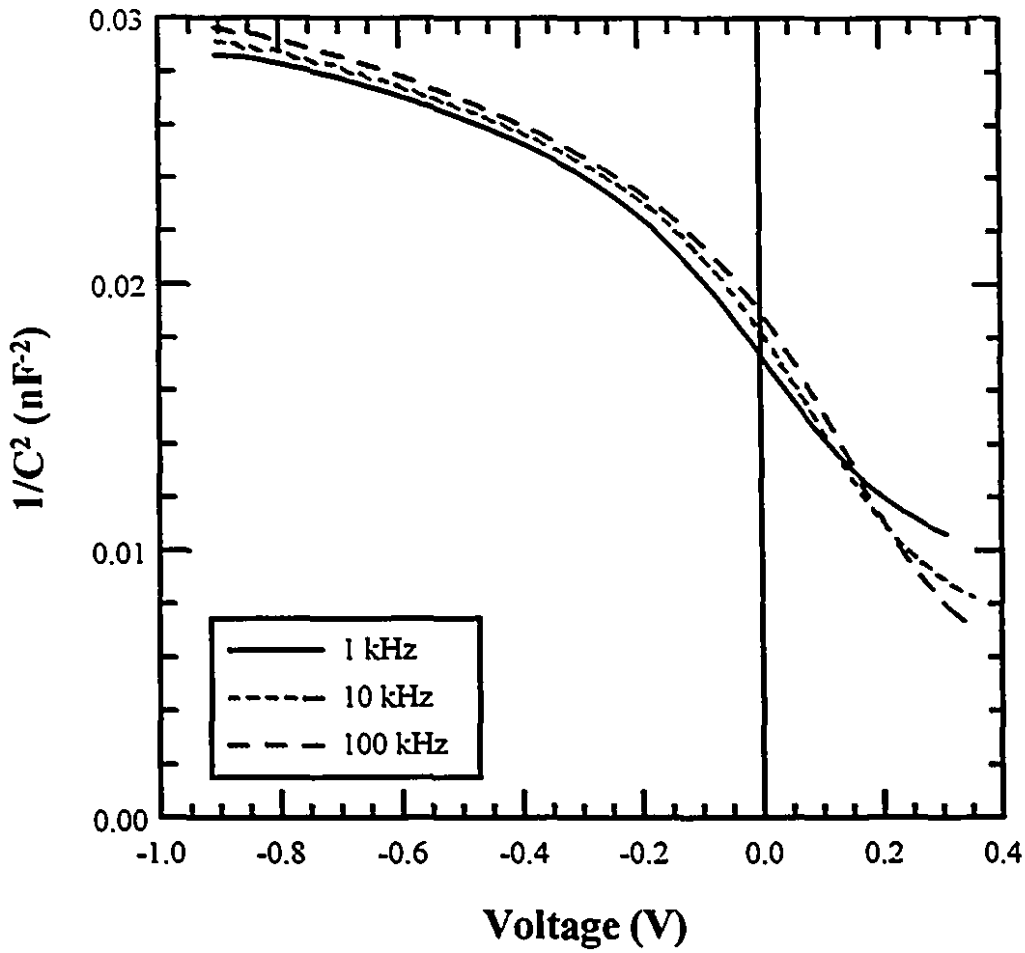


Fig. 5.29 A plot of $1/C^2$ vs voltage for a non-annealed cell (D-38) at three different frequencies.

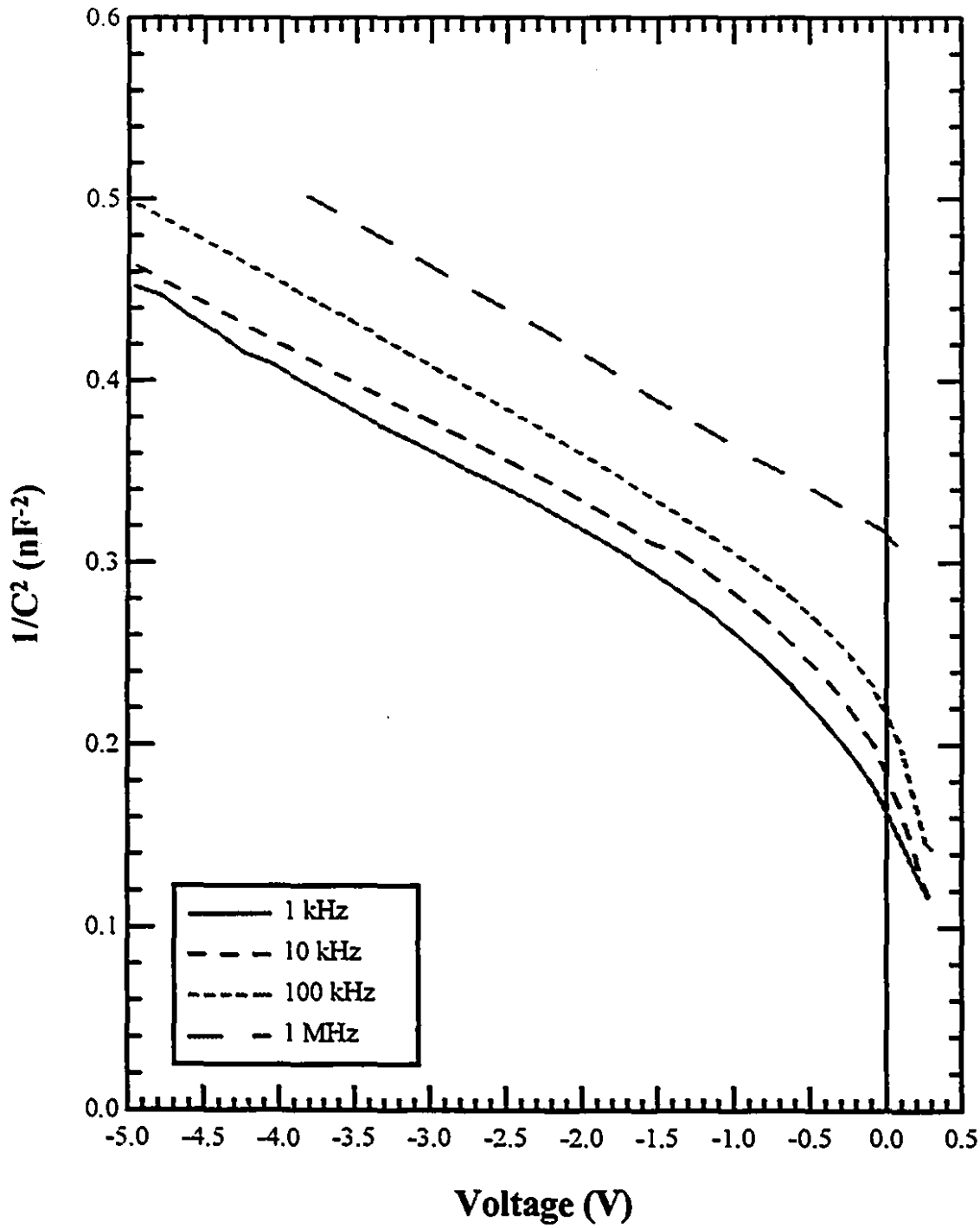


Fig. 5.30 A plot of $1/C^2$ vs voltage for the cell D-100. Capacitance was measured at large reverse voltages and up to 1 MHz.

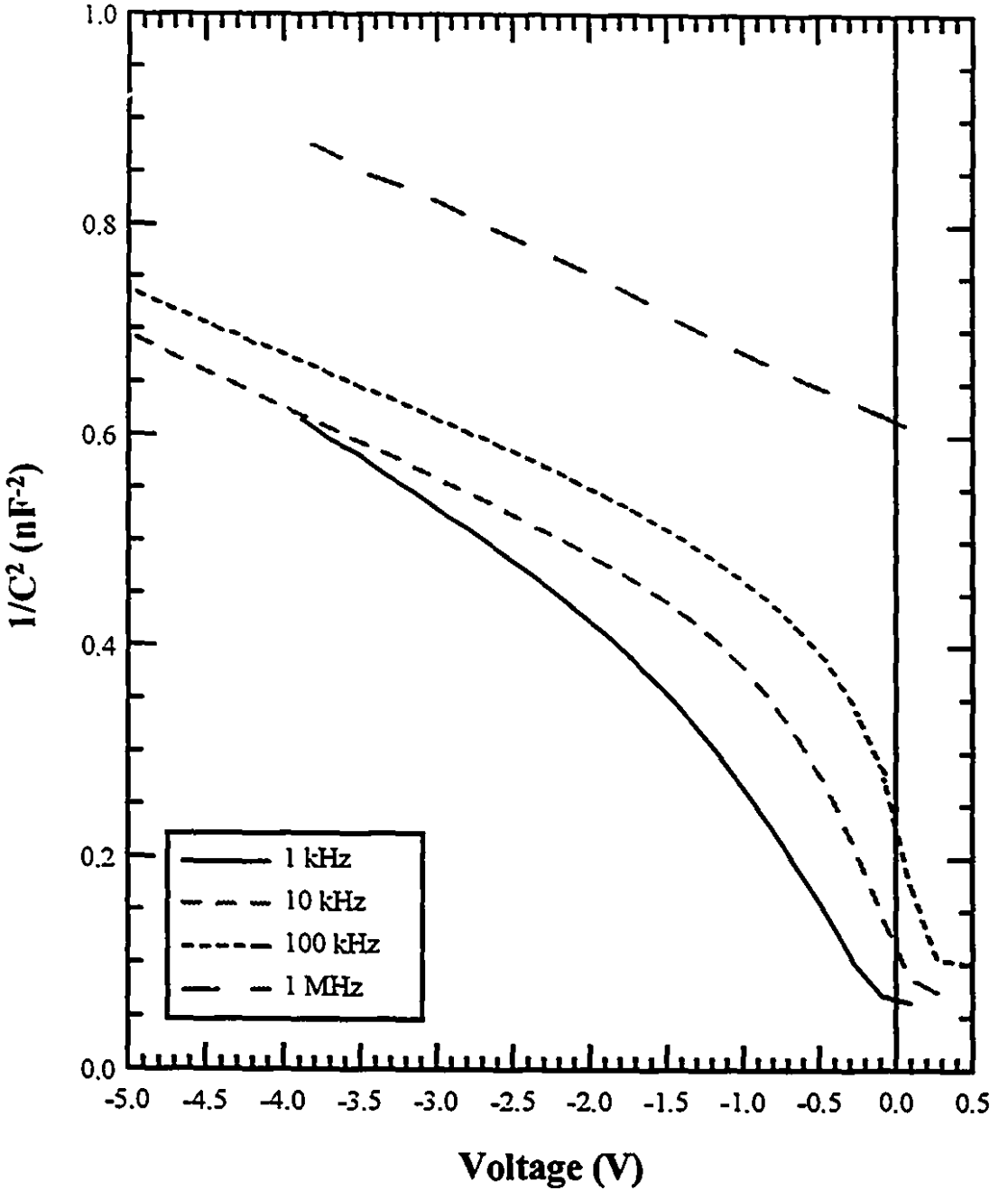


Fig. 5.31 A plot of $1/C^2$ vs voltage for a non-annealed cell (D-111). Capacitance was measured at large reverse voltages and up to 1 MHz.

CHAPTER 6

ELECTRON-BEAM-INDUCED-CURRENT MEASUREMENTS

6.1 Introduction

Before ZnO was established as a better window material for $CuInSe_2$ solar cells, CdS had been widely used. The CdS films were prepared by thermal evaporation. However, an active buried $CuInSe_2$ homojunction was observed by electron-beam-induced-current (EBIC) measurements in some CdS/$CuInSe_2$ cells fabricated on single-crystal or thin-film $CuInSe_2$ substrates [6.1-6.3]. The depth of the homojunction formed in a single-crystal substrate ranged from 1μm for an acceptor concentration of $1.8x10^{18}$ cm^{-3} to 9 μm for $2.6x10^{16}$ cm^{-3}, but the homojunction in a thin-film cell was usually much shallower.

The type conversion of the top layer of the p-type single-crystal $CuInSe_2$ substrate was believed to be due to either the in-diffusion Cd from the CdS film and/or the out-diffusion of Se or Cu during the CdS deposition at about 200 °C substrate temperature. However, the type-conversion mechanism in thin-film cells was less clear because of the fact that oxygen was believed to be commonly incorporated in $CuInSe_2$ films and also the fact that an oxidation, i.e. baking in O_2, was able to reverse the type conversion. The homojunction, therefore, could have been formed during the CdS deposition or EBIC measurements by reducing the oxygen content in the top layer of the $CuInSe_2$ film. However, atomic/defect diffusion should and could not be ruled out as the type-conversion mechanism in thin-film cells as well.

There has always been a concern of the possibility of the presence of such a homojunction in the now more commonly-used ZnO/CdS/$CuInSe_2$ structure, especially because CdS is used as

the buffer layer. Therefore, EBIC measurements were performed in the present work to check the existence of such a homojunction. The diffusion lengths of the $CuInSe_2$ substrates were also measured using the EBIC method. In this chapter, the principle of EBIC is first briefly explained and the results of the EBIC studies on the ZnO/CdS/$CuInSe_2$ cells are presented.

6.2 Principles of the EBIC Method

During the EBIC measurements, an electron beam is usually scanned across the cross section of a cleaved device with a charge-collecting junction as shown in Fig. 6.1 (a) for a CdS/$CuInSe_2$ junction. The electron beam will generate electron-hole pairs in a volume surrounding the electron beam inside the semiconductor and if these electron-hole pairs are generated close enough or inside the depletion region of a p-n junction, the electron-hole pairs will be separated by the electric field and contribute to an external short-circuited current. This current is then measured and recorded for the particular position of the electron beam. By scanning the electron beam across the junction and plotting the measured current against the electron beam position, the EBIC scan of the junction can be obtained. The energy band diagram, electric field distribution and the corresponding EBIC scan are also shown in Fig. 6.1. Ideally, as shown in Fig. 6.1 (d), the EBIC signal should peak at the position with the maximum electric field, i.e. at the metallurgical junction in the case of a p-n junction. Therefore, the position of the EBIC peak is a good indicator of the position of the p-n junction.

6.3 Characterization of ZnO/CdS/$CuInSe_2$ and CdS/$CuInSe_2$ Junctions

Several ZnO/CdS/$CuInSe_2$ cells with conversion efficiencies greater than 8 % were selected for the EBIC studies. A sample was fractured or cleaved to expose the p-n junction before being loaded into a JEOL model 6100 SEM system. The sample was made certain to be securely fixed into position because any small shift of the sample position might cause a misinterpretation of the position of the junction. The system was allowed to be stabilized prior to any measurements. It was also found that repeated scanning of the electron beam at the same position on the sample could gradually change the position and magnitude of the EBIC peak; therefore, all the results presented in this section were obtained from the first two EBIC scans.

An EBIC scan of one of the ZnO/CdS/$CuInSe_2$ cells (sample D-45) is shown in 6.2 (a). The picture is a SEM photograph superimposed with the EBIC signal. The EBIC scan was taken first on a Polaroid film and then the SEM image was taken on same film to combine the two images. It should be pointed out that the CdS is too thin to be observed in the SEM picture; only the ZnO and the $CuInSe_2$ are visible in the picture. It can be seen that the EBIC signal peaked at a position of about 0.2 μm from the metallurgical junction in the $CuInSe_2$ side. The apparent small shift of the peak could imply the existence of a very shallow homojunction as suggested by Matson et al. [6.1], although their homojunction was much deeper, up to 9 μm in one case. However, the shift could also be caused by the presence of interface states at the junction or other interface effects [6.1].

In order to find out the true cause of the shift, a CdS/Si junction was tested for comparison purpose. The CdS/Si cell was fabricated by evaporating a layer of CdS onto a (100)-oriented Si wafer. It also showed a very small shift, about 0.1-0.2 μm, of the EBIC peak away from the metallurgical junction. The existence of a homojunction in the CdS/Si cell is very

unlikely because of the usually high temperature (>1000 °C) required for diffusion in Si, while the CdS evaporation was carried out with a substrate temperature of only 180 °C. It is more likely the EBIC shift was due to interface states or other interface effects than of a homojunction in the CdS/Si junction. Of course, this does not prove anything for the case of the ZnO/CdS/$CuInSe_2$ junction, but just to show that EBIC shift occurs in other junctions due to interface effects as well.

A strong evidence of the absence of a homojunction in the ZnO/CdS/$CuInSe_2$ junction is shown in Fig. 6.2 (b) for another EBIC scan of the same sample as in Fig. 6.2 (a) but of different location. The SEM image shows that the ZnO/CdS layer of the area under examination was lifted off from the $CuInSe_2$ substrate during the fracturing of the cell. An EBIC scan of this area revealed no EBIC signal as in Fig. 6.2 (b), indicating no electric field in the $CuInSe_2$ substrate, although EBIC signals were still observed in other areas, including the edge of the lift-off region, where the ZnO/CdS was still in contact with the $CuInSe_2$ substrate.

It should be noted that the EBIC scan shown in Fig. 6.2 (b) was taken near a region where the ZnO/CdS layer was still attached to the $CuInSe_2$ substrate. If there was a homojunction in the $CuInSe_2$ substrate, the region with the ZnO/CdS layer would provide the electrical contact to the homojunction. The absence of an EBIC signal in an area without ZnO/CdS indicates that there was no buried homojunction in the ZnO/CdS/$CuInSe_2$ cells; otherwise, the electron-beam generated electron-hole pairs would have been separated by the homojunction, collected by the region with ZnO/CdS, and given rise to an EBIC signal. The need of the ZnO/CdS layer being attached to the $CuInSe_2$ substrate in order to obtain an EBIC signal indicates that the active junction was a heterojunction.

Although Matson et al. [6.1] showed that the homojunction was detectable by EBIC even when the top window layer was selectively removed at the scan area in their CdS/$CuInSe_2$ cells, it

is helpful to repeat this experiment to assure that such a buried homojunction can be detected by the EBIC system in our laboratory. Therefore, efforts were made to reproduce the CdS/$CuInSe_2$ heterojunction cell with a buried homojunction [6.1], using similar fabrication steps. The CdS was deposited by thermal evaporation in a vacuum system with a pressure of 10^{-6} torr. A CdS source containing 2 at. % In was used to obtain the CdS films with a resistivity of about 10^{-3} to 10^{-2} Ω-cm. The $CuInSe_2$ substrates were maintained at 180 °C during the evaporation. A thickness of about 2 μm was obtained with a deposition time of 10 minutes, excluding the heating and cooling of the substrate. The substrate was cooled after the deposition by passing water through the substrate holder. The conversion efficiency of the cell was less than 3 % although the $CuInSe_2$ substrate was also annealed with the optimal conditions.

An EBIC scan of the sample (D-83) is shown in Fig. 6.3 (a). It can be seen that the EBIC signal peaked at about 2.4 μm from the physical junction in the $CuInSe_2$ substrate, suggesting the presence of a homojunction. The CdS/$CuInSe_2$ heterojunction was almost inactive as indicated by the absence of a strong electric field compared to the homojunction. After the first EBIC scan, the CdS layer was removed from selective areas by protecting certain areas with wax and dipping the sample into dilute HCl solution. The exposed CdS was etched away and the EBIC measurements repeated. Fig. 6.3 (b) shows an EBIC scan of D-83 in the region where the CdS was removed. The shape and position of the EBIC peak were almost the same as that before the CdS removal. It is clear that the existence of a homojunction could be detected by EBIC even without the top window layer at the location of scan, as long as the top layer was present in other areas to provide the electrical contact to the homojunction.

It should also be noted that the homojunction EBIC peak was observable anywhere in the region where the CdS was removed, and was not necessary to be near the regions with CdS.

Therefore, the existence of a homojunction should be easily detected by EBIC. From these results, it is safe to conclude that there was no homojunction present in the ZnO/CdS/$CuInSe_2$ cells prepared in this laboratory.

6.4 Diffusion Length Measurements

Minority carrier diffusion length is an important parameter for solar cells because the longer the diffusion length usually means the larger the collection efficiency. However, the large absorption coefficient of $CuInSe_2$ relaxes the requirements for diffusion length because only a few tenths of a micrometer of $CuInSe_2$ is sufficient to absorb almost all the incident light, while the diffusion length of $CuInSe_2$, especially for single crystals, is usually larger than that. Nevertheless, diffusion length is still a good indicator of the quality of the $CuInSe_2$ absorber. Mora and Romea [6.4] reported a minority-carrier diffusion length of 0.5 μm determined by photo-electromagnetic effect for p-$CuInSe_2$ single crystals; while using EBIC, Matson et al. [6.1] estimated the diffusion length to be at least 2.4 μm and Piekoszewski et al. [6.5] obtained a value of 2.5 μm for p-$CuInSe_2$ single crystals. Bouazzi et al. [6.6] also reported the measurements of diffusion length by EBIC for thin-film $CuInSe_2$ and obtained a value of about 0.6 μm.

The electron-beam-induced current has long been known to be proportional to the exponential of the distance of the electron beam from the junction plane [6.7-6.9], as expressed by the equation

$$I_{sc}(x) = I_{max} e^{-\frac{x}{L^*}}, \qquad (6.1)$$

where I_{max} is value of I_{sc} at the junction plane, x is the distance of the electron beam from the junction plane as shown in Fig. 6.1, and L^* is the effective diffusion length of the minority carriers.

The EBIC are plotted against the distance from the junction plane in the $CuInSe_2$ side for one of the $ZnO/CdS/CuInSe_2$ cells (D-24) for 5 different accelerating voltages in Fig. 6.4. The EBIC scans were taken at five different locations, each slightly apart from each other but far enough to be not affected by previous scans. It can be seen that the EBIC peak was wider for a larger accelerating voltage, indicating a larger effective diffusion length.

A logarithmic plot of the currents is required to determine the effective diffusion length from the slope, $-1/L^*$, of the plot. Such a plot is shown in Fig. 6.5. From the plot, the effective diffusion lengths for the five accelerating voltages were determined and shown in Table 6.1. The effective diffusion length was found to increase with the accelerating voltage. This behaviour was reported to be due to the effect of the surface recombination at the incident plane [6.5,6.10]. The larger the accelerating voltage, the deeper the electron beam will penetrate and the larger portion of carriers will be generated deeper inside the material so that surface recombination will have less of an effect on L^*. If the surface recombination is small, the effective diffusion lengths at different accelerating voltages will be about the same and equal to the bulk diffusion length, L_B. If surface recombination is significant, as in the present case, L^* will increase and approach L_B asymptotically as the accelerating voltage increases [6.5, 6.10].

The effective diffusion length is plotted against the accelerating voltage in Fig. 6.6. It is clear that in Fig. 6.6 L^* was not approaching its asymptote, even at the largest accelerating voltage of 30 kV used in the experiments. However, L_B was at least equal to 1.56 μm, the value of L^* obtained at 30 kV. Jastrzebski et al. [6.10] proposed a model in which the surface recombination effect was taken into consideration. In this model L^* can be expressed as

$$L^{*2} = L_B^2\left(1 - \frac{s^*}{s^*+1}e^{\frac{-z}{L_B}}\right), \qquad (6.2)$$

where L_B is the bulk minority-carrier diffusion length, ξ is the penetration depth of the electron beam, and s^* is the "reduced" surface recombination velocity given by the relation, $s^*=s\tau_B/L_B$. Here s is the surface recombination velocity and τ_B is the minority-carrier lifetime which can be calculated from the relation, $\tau_B=(\mu_B kT/q)/L_B^2$, where μ_B is the minority-carrier mobility. In the model, the generation of electron-hole pairs by the electron beam is approximated by a point source located at ξ [6.5], which is given by

$$\xi = bR_B \propto V^{\alpha}, \tag{6.3}$$

where b is a constant, R_B is the mean range of the primary electron beam, V is the accelerating voltage of the electron beam and α has a value of 1.62 as suggested by Piekoszewski et al. [6.5]. Using this value for α, these authors calculated the values of R_B to be 0.9 μm for 10 kV, 2.9 μm for 20 kV and 5.6 μm for 30 kV for $CuInSe_2$ [6.5]. This set of R_B values was also used by Bouazzi et al. [6.6] for their thin-film $CuInSe_2$ cells and will be used in the present case as well. Slightly different values of α were also suggested by different authors [6.11-6.13]. Experimentally, α was found to have values in the range of 1.44 to 1.6 for materials with atomic number larger than 30 [6.13]. Substituting Eq. (6.3) into Eq. (6.2) will give

$$L^{*2} = L_B^2\left(1-\frac{s^*}{s^*+1}e^{\frac{-bR_B}{L_B}}\right). \tag{6.4}$$

The value of the constant b was taken as 0.085 by Bouazzi et al. [6.6] and Oakes et al. [6.14], although a value of 0.06 for b was obtained by Piekoszewski et al. [6.5]. With L^* and R_B known for each accelerating voltage, the two unknowns, L_B and s^*, in Eq. (6.4) can be solved using any two pairs of values of L^* and R_B. Using this method, the average value of the bulk diffusion length, L_B, was calculated to be 2.5 μm for a b value of 0.085 and 2.9 μm for a b value of 0.06.

However, the error of this method can be significant due to the uncertainties in the values of R_R and b. The diffusion length obtained in this case can then serve only as a rough estimate.

EBIC scans were also taken from the top of the cells as shown in Fig. 6.7. It is interesting to find that the measured effective diffusion length was relatively insensitive to the accelerating voltage of the electron beam as shown in Table 6.2. There are two possibilities of this behaviour. First of all, this could be due to a small depletion width compared to a large penetration depth of the electrons as shown in Fig. 6.7 so that only a small portion of the charge carriers generated near the surface would be collected by the junction. However, this does not seem to be the case. The depletion width was calculated to be about 0.2 μm from C-V measurements while the penetration depth was calculated to be about 0.08 μm for 10 kV, 0.25 μm for 20 kV and 0.48 μm for 30 kV. It is apparent that most of the electron-beam induced charge carriers could be collected by the depletion region if the electron beam was located within one diffusion length from the edge of the junction.

A more likely explanation for this independence on the accelerating voltage is that the surface recombination of the top $CuInSe_2$ surface, which was polished and annealed, was small enough to not significantly affect the diffusion length measurements. In other words, no significant amount of the generated charge carriers would be lost by surface recombination. The measured diffusion length would then be near to the bulk diffusion length. Fig. 6.8 shows the EBIC signal of such a top-surface or planar scan on the same sample shown in Fig. 6.4. The accelerating voltage was 30 kV. The diffusion length calculated from this figure was about 4 μm, which was larger than the 2.5 μm or 2.9 μm values obtained previously for the same sample by the method with the surface-recombination correction. However, it is believed that 4 μm is a more accurate measurement of the bulk diffusion length because no surface-recombination

correction was used. The diffusion length obtained from most of the other planar measurements generally lay in the range of 4 to 6 μm. These values are comparable to the diffusion length values obtained by a photocurrent-capacitance method on similar $CuInSe_2$ crystals [6.15].

6.5 Conclusions

It has been demonstrated by EBIC measurements that there was no buried homojunction in the cells prepared in the present work, indicating that the heterojunction was active and responsible for the high photovoltaic performance. However, a $CdS/CuInSe_2$ cell was found to have a buried homojunction and showed a conversion efficiency of less than 3 %. The diffusion length of the $CuInSe_2$ substrates has also been obtained by EBIC measurements. Diffusion length measurements on a fractured plane of the $ZnO/CdS/CuInSe_2$ junction were greatly affected by surface recombination. After surface-recombination correction, a bulk diffusion length of about 2.5 or 2.9 μm was obtained. A more accurate value of about 4 μm was obtained on the top surface for the same sample. Using the planar EBIC measurements, the diffusion length measured for most of the samples had a value of 4 to 6 μm.

Table 6.1 Effective diffusion lengths of $CuInSe_2$ measured at different electron-beam accelerating voltages from EBIC measurements for cell D-24. The measurements were performed on a fractured surface.

	Accelerating Voltage (kV)				
	10	15	20	25	30
L^* (μm)	0.45	0.73	1.0	1.25	1.56

Table 6.2 Effective diffusion lengths of $CuInSe_2$ measured at different electron-beam accelerating voltages for cell D-24. The measurements were performed on the polished top surface.

	Accelerating Voltage (kV)			
	15	20	25	30
L^* (μm)	3.85	3.79	3.91	4.0

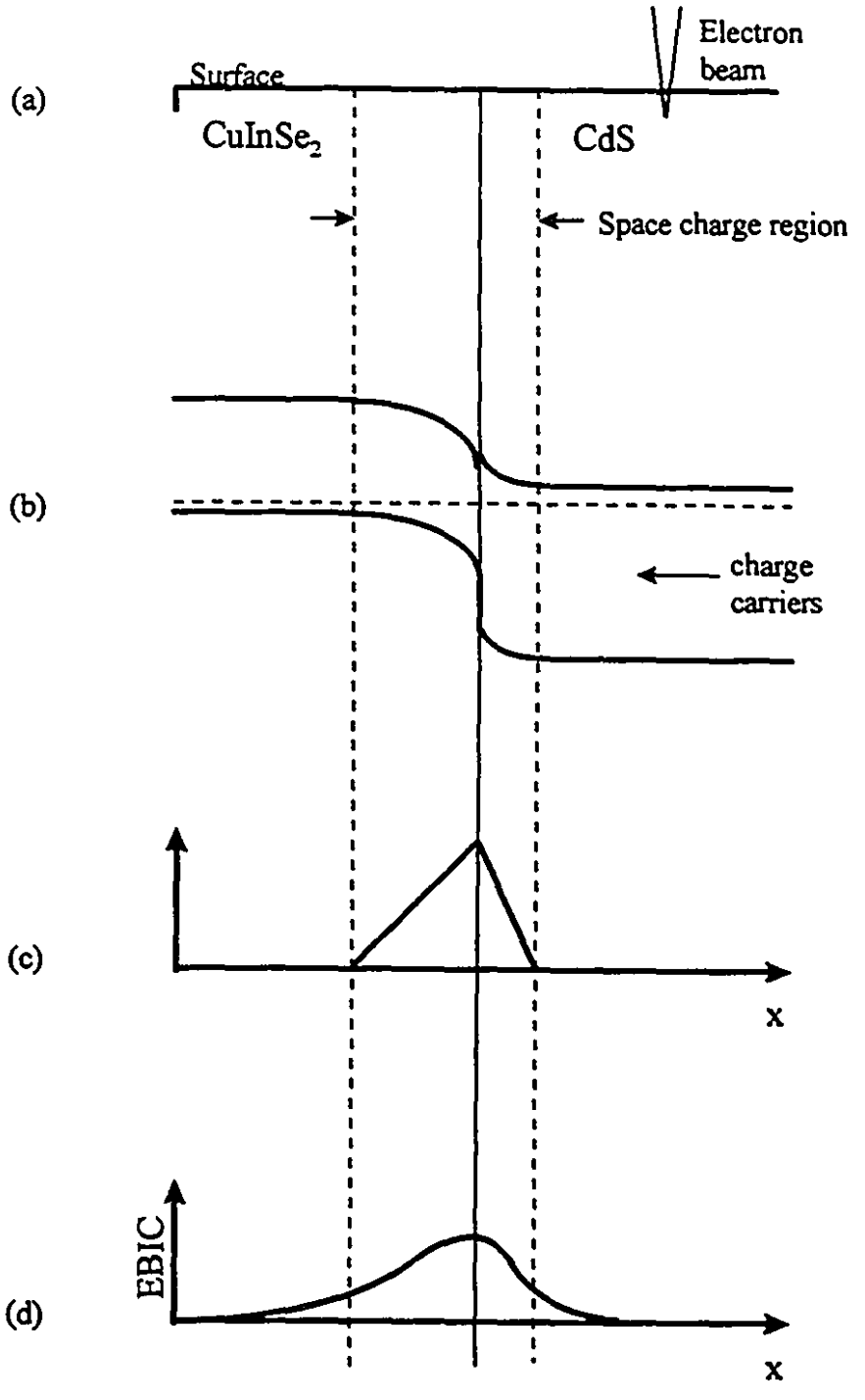
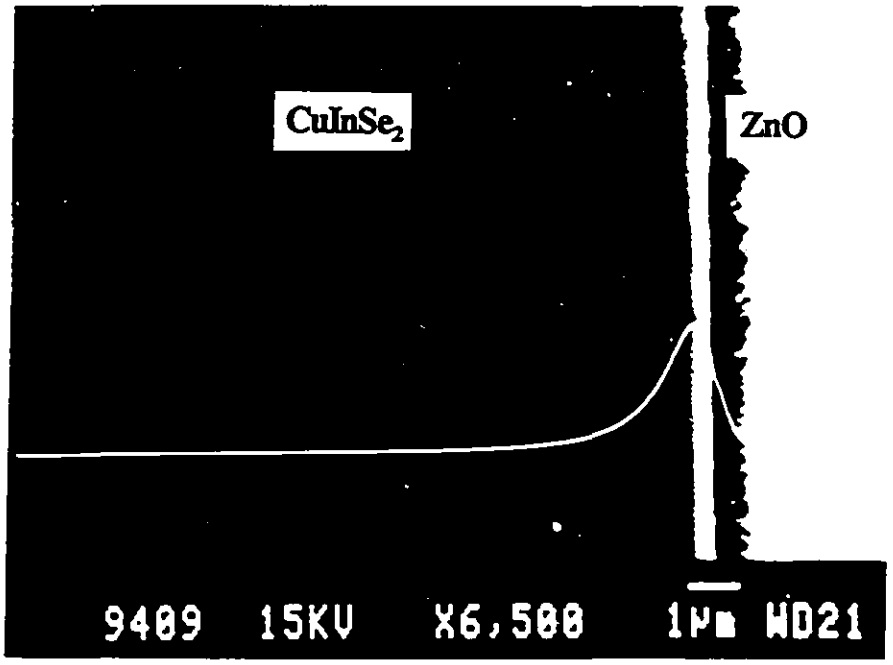


Fig. 6.1 (a) Electron beam scanning across a CdS/$CuInSe_2$ heterojunction. (b) Energy band diagram of the junction. (c) Electric field distribution across the junction. (d) Resulting EBIC signal. [6.1]

(a)



(b)

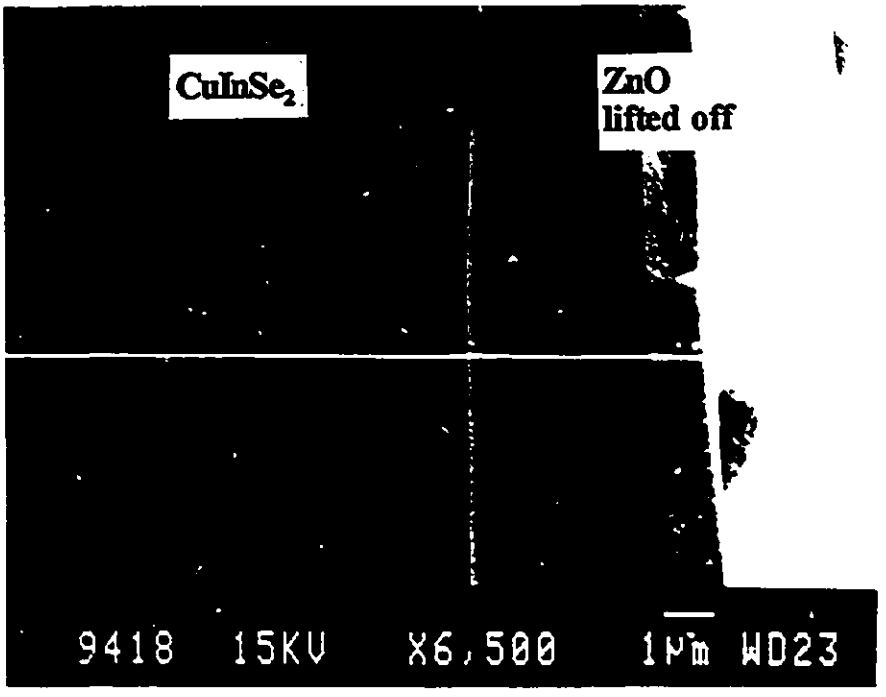
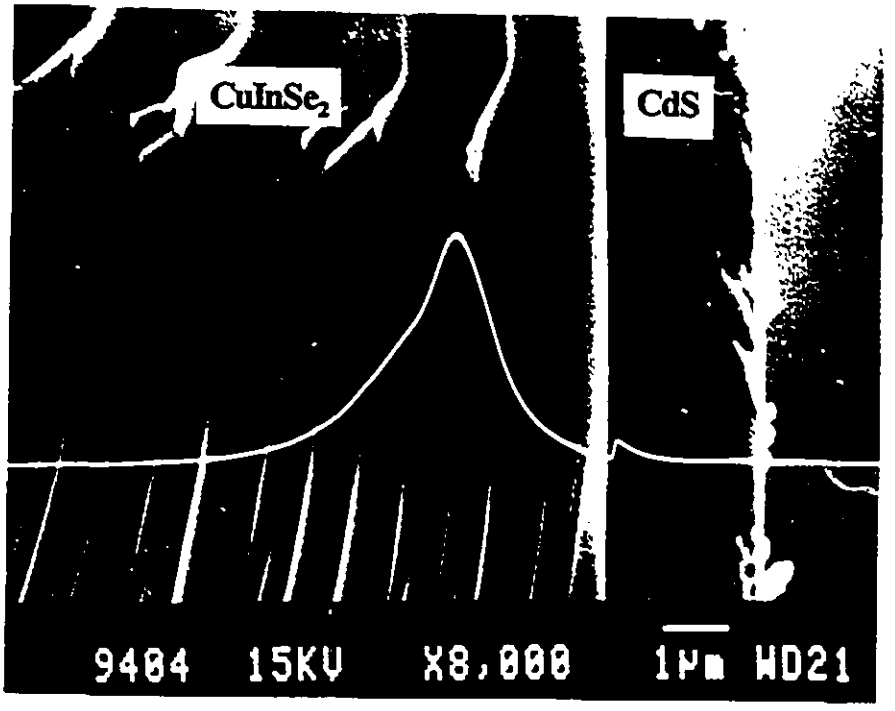


Fig. 6.2 (a) EBIC scan of a ZnO/CdS/$CuInSe_2$ cell (D-45). Note that the CdS is too thin to be visible. (b) EBIC scan of the same sample at a region where the ZnO layer was lifted off.

(a)



(b)

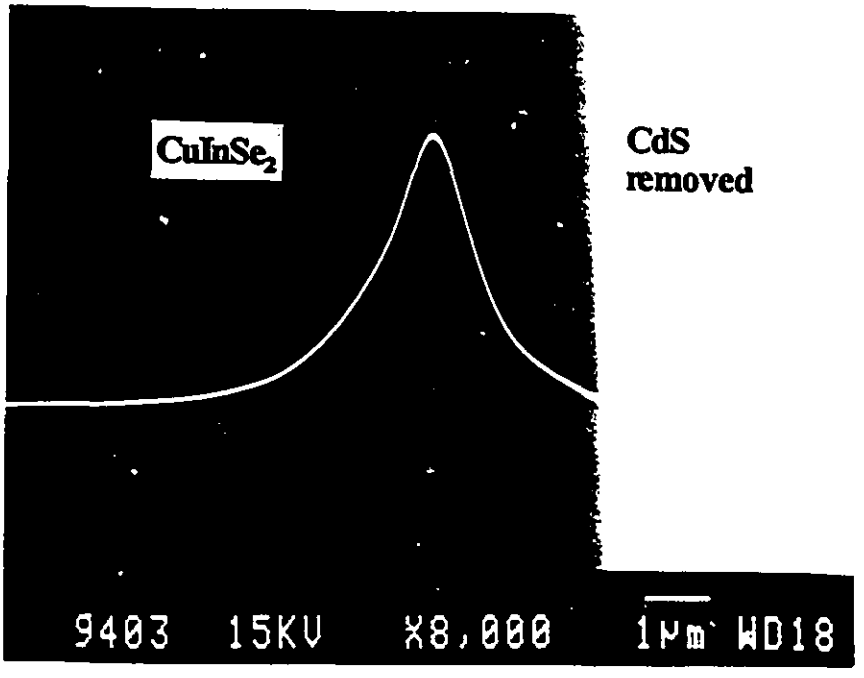


Fig. 6.3 (a) EBIC scan of a CdS/$CuInSe_2$ cell. (b) EBIC scan of the same sample at a region where the CdS was removed.

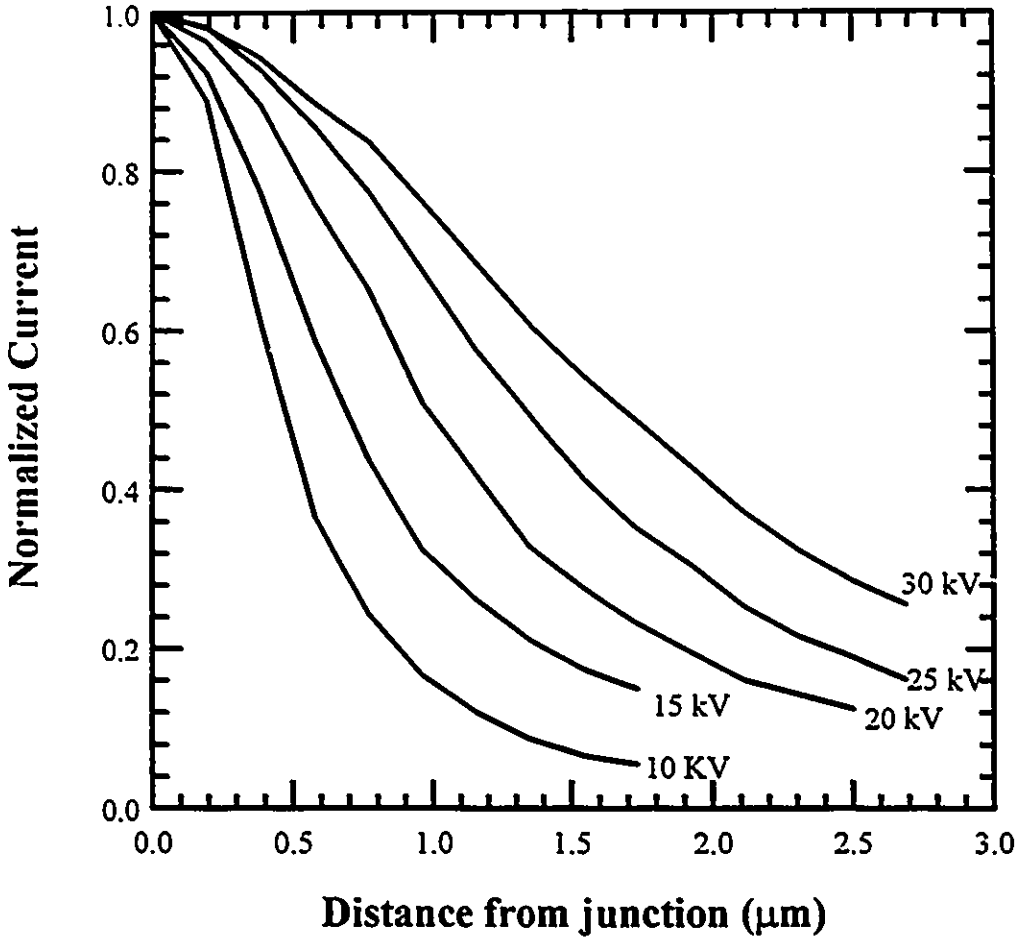


Fig. 6.4 EBIC scan at five different accelerating voltages for the cell D-24.

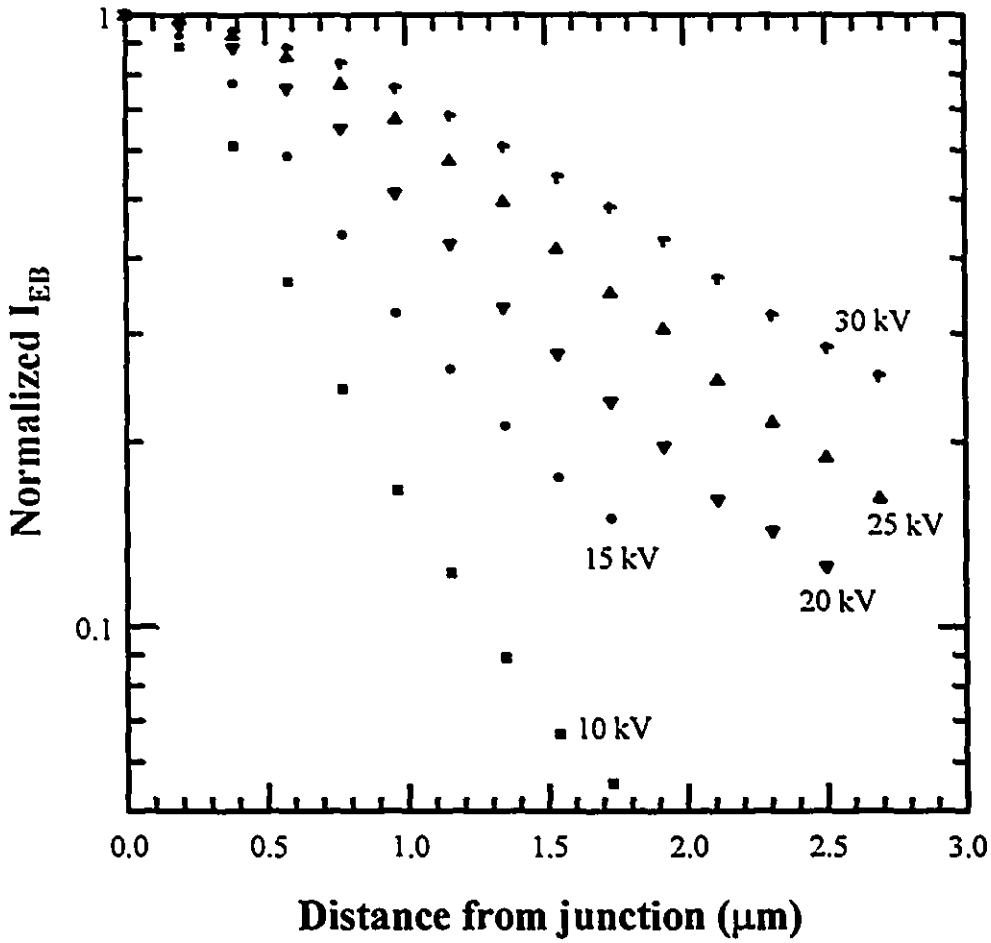


Fig. 6.5 Logarithmic plot of the EBIC signals for Fig. 6.4.

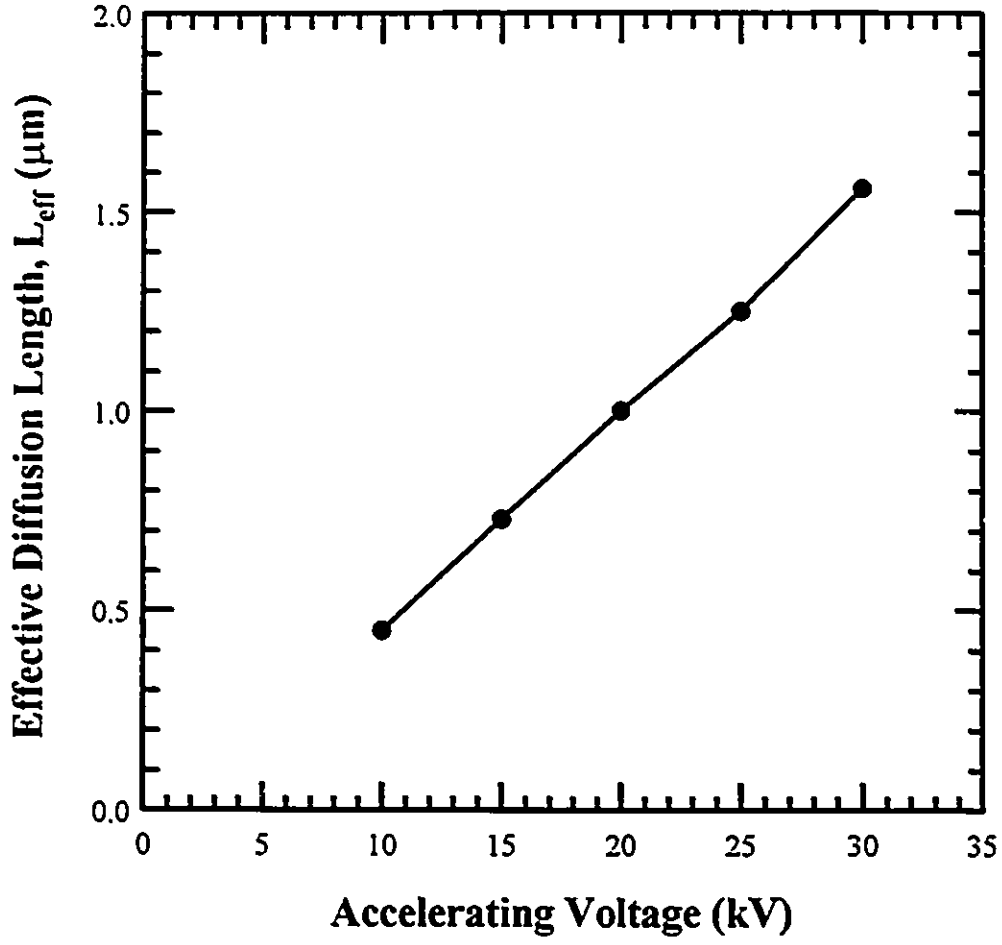


Fig. 6.6 A plot of effective diffusion length against the accelerating voltage for the cell D-24.

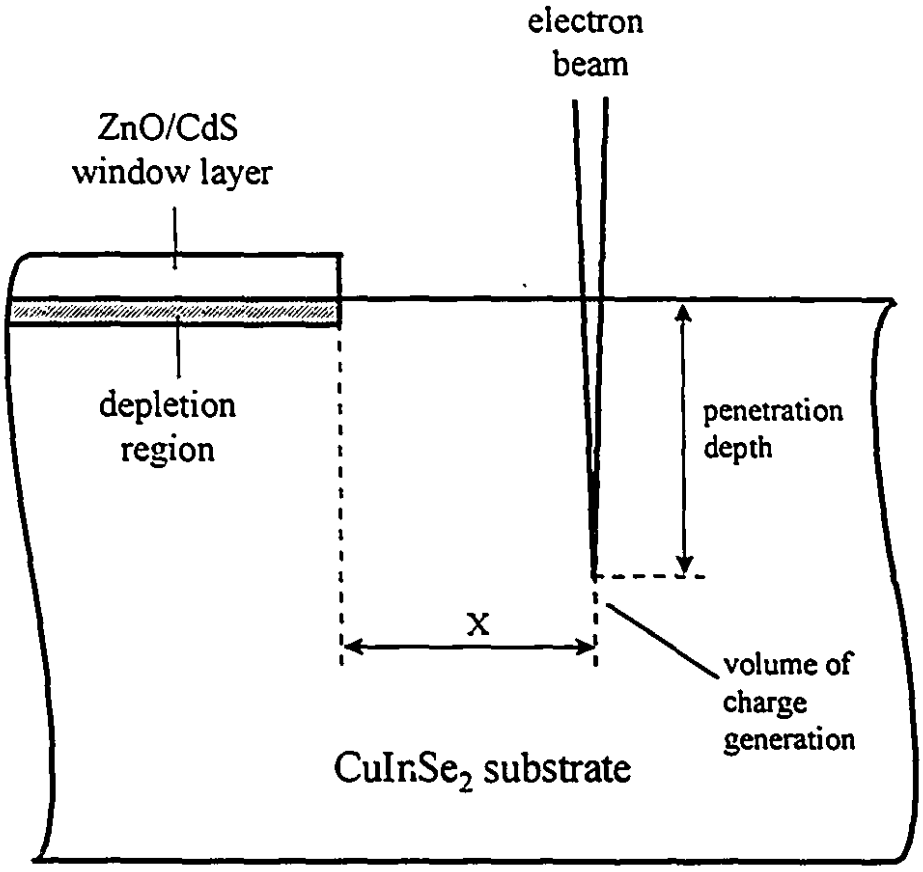


Fig. 6.7 A planar EBIC scan.

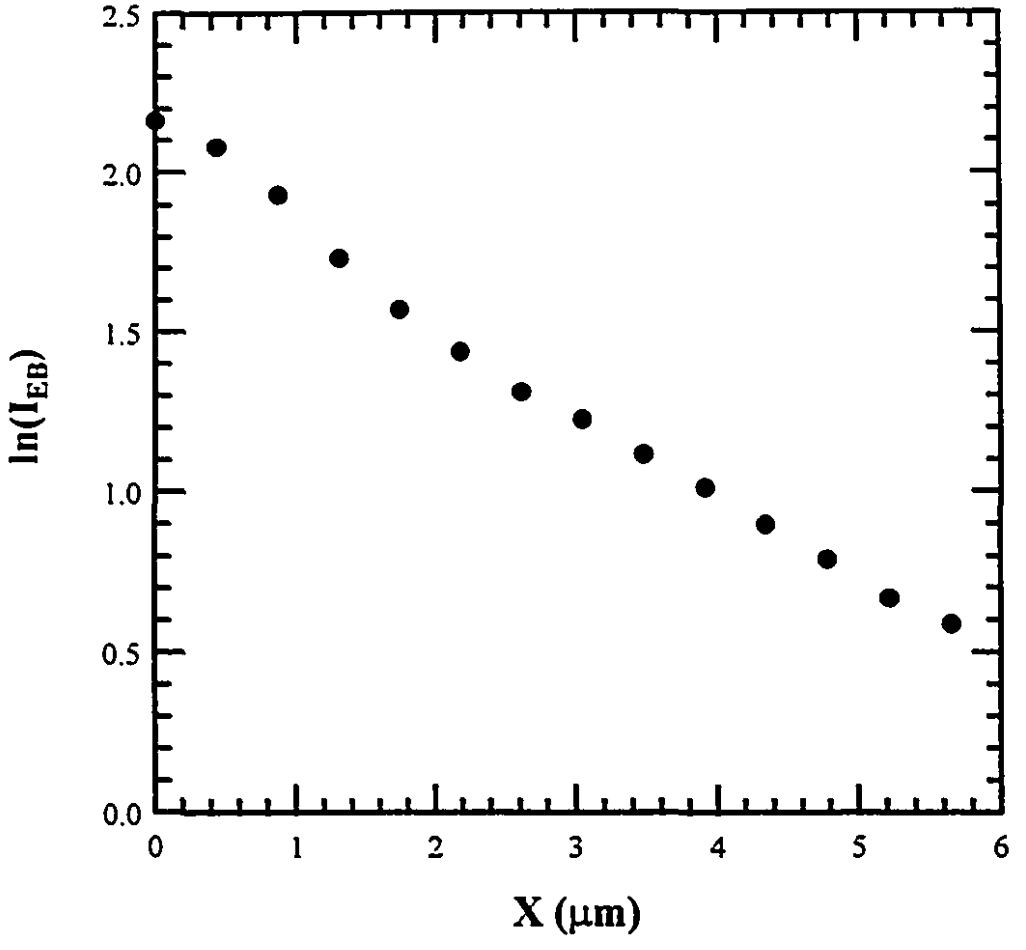


Fig. 6.8 A logarithmic plot of the EBIC signal against the distance from the edge of the junction for a planar EBIC scan of sample D-24.

CHAPTER 7

DEEP-LEVEL TRANSIENT SPECTROSCOPY MEASUREMENTS

7.1 Introduction

Deep-level-transient-spectroscopy (DLTS) is a powerful tool for the study of deep-level defect states in a semiconductor, since both the energy levels of these defect states and their densities can be determined. Such deep levels, which are very common in semiconductors, may be associated with the crystal growth or the device fabrication process. It is important to identify these defect levels because they may play an important role in the electrical properties of a p-n junction and, thus, the performance of a p-n junction solar cell. The results of the DLTS measurements on ZnO/CdS/$CuInSe_2$ are reported in this chapter.

7.2 Principles of Deep-Level Transient Spectroscopy

Deep levels are associated with impurities having energy levels located inside the forbidden gap of a semiconductor. Unlike the shallow-level impurities, which are usually introduced intentionally into semiconductors as dopants, deep levels lie deep in the forbidden gap, i.e. they are relatively far from the conduction band and valence band edges. Although deep levels are sometimes introduced into a semiconductor intentionally, usually by introducing foreign impurities, as recombination centres to reduce charge carrier lifetime, they are usually incorporated into the semiconductor unintentionally. Foreign impurity atoms exist substitutionally or interstitially and crystallographic defects such as vacancies, interstitials, dislocations and

stacking faults can all contribute to deep-level defect states in the forbidden gap. Each deep level is characterized by its energy, concentration, and capture and emission coefficients of charge carriers. In principle, a deep level is able to capture and emit charge carriers in both the conduction band and valence band, as can be seen by the following steady-state equation [7.1],

$$n_T = \frac{e_p + c_n n}{e_n + c_n n + e_p + c_p p} N_T, \tag{7.1}$$

where n_T is the concentration of the deep-level states occupied by electrons, N_T is the total concentration of the deep level states, n the concentration of free electrons in the conduction band, p is the concentration of free holes in the valence band, and e_p, e_n, c_p and c_n are the emission and capture coefficients of holes and electrons. Furthermore, the time constant τ of the deep level can be defined as

$$\tau = \frac{1}{e_n + c_n n + e_p + c_p p}. \tag{7.2}$$

It can be seen that the steady-state occupancy of the deep level is determined by the electron and hole concentrations and the emission and capture rates. The emission and capture coefficients are strongly dependent on the energy of the deep level. Those levels lying near the middle of the band gap can act, but not necessarily, as recombination centres because the capture and emission coefficients are comparable for electron and holes. Electrons from the conduction band will recombine with holes in the valence band through the recombination centres. Deep levels closer to one band edge usually act as trapping centres. Unlike recombination centres, such trapping centres usually only capture and emit charge carriers in either only the conduction band or only the valence band.

Deep levels closer to the conduction band, i.e. in the upper half of the energy gap, are dominant with electron emission/capturing and have large electron emission and capture coefficients. They are considered as electron traps. Therefore, Eq. (7.1) and (7.2) can be simplified by omitting the terms for hole emission and capturing. Similarly, the deep levels closer to the valence band, i.e. in the lower half of the energy gap, are generally hole traps. When a deep-level state becomes positively charged after emitting an electron, it is called a deep donor level regardless which half of the forbidden gap it is in. However, when a deep level becomes negatively charged after capturing an electron, it is called a deep acceptor level. These trapping levels are usually undesirable and could limit device performance [1.11, 5.22]. Therefore, it is necessary to identify and characterize such deep levels in order to have more understanding of the device characteristics.

Deep-level transient spectroscopy (DLTS) is a quick and easy way to characterize deep levels in semiconductors. Its major advantage over other techniques is the spectroscopic nature of the method, i.e. it gives a unique peak for each deep level detected. Using this method, the concentration and energy of each deep level can be obtained. A Schottky junction or p-n junction is required in the DLTS measurements. During the measurements, a voltage pulse is applied to the junction and the capacitance transient is measured and carefully analyzed at different temperatures. Fig. 7.1 shows the energy-band diagrams of a p^+-n junction, assuming it has only one deep-level acceptor in the upper half of the energy gap in the n side, under different conditions during DLTS measurements. As explained earlier, such a deep level is an electron trap, i.e. a majority carrier trap in this case, and holes can be neglected. For DLTS measurements, the junction is first zero biased (Fig. 7.1 (a)) or slightly forward biased for a certain period of time. Most of the deep level states are below the Fermi-level and will be occupied by electrons

provided that this period is long compared with the characteristic time constant of the deep level. After this filling period, the junction is reverse biased as in Fig. 7.1 (b). The depletion region now extends deep into the n region uncovering the electron-occupied deep levels. The electron-filled deep-level states with energy above the electron quasi-Fermi level, E_{Fn}, in the depletion region are bound to emit the trapped electrons; however, the response time or time constant of the deep level is very sensitive to temperature. The trapped electrons will be emitted slowly until the steady state is reached (Fig. 7.1 (c)), when all the deep level states above E_{qF} are empty. The time-dependent concentration of the trapped electrons following the reverse bias pulse can be described by

$$n_T(t) = N_T e^{-\frac{t}{\tau_e}} = N_T e^{-e_n t}. \tag{7.3}$$

The time constant τ_e of the electron emission is equal to the reciprocal of the emission coefficient as can be seen from Eq. (7.2) for the case when electron emission is dominating. As the electrons are emitted to the conduction band, they leave behind a net positive charge. i.e. the deep-level acceptor states change from negatively charged to neutral. This change of space charge density is reflected in the depletion capacitance, although the change is small. Using Eq. (5.7), by letting $N_A >> N_D$ and including the deep-level transient effect, the capacitance can be described as

$$C(t) = \left\{ \frac{qA^2\varepsilon_D}{2(V_{bi}+V_R)} [N_D - n_T(t)] \right\}^{\frac{1}{2}} = C_o \left[1 - \frac{n_T(t)}{N_D} \right]^{\frac{1}{2}}, \tag{7.4}$$

where N_D-$n_T(t)$ is the total space charge density in the depletion region and C_o is the capacitance without any deep levels at reverse bias $-V_R$. Generally, the deep level concentration is much smaller than the donor concentration, i.e. $N_D >> N_T$, and Eq. (7.4) becomes

$$C(t) = C_o\left[1 - \frac{n_T(t)}{2N_D}\right] = C_o\left[1 - \frac{N_T}{2N_D}e^{-e_n t}\right], \qquad (7.5)$$

by also substituting Eq. (7.3) for $n_T(t)$. It is this capacitance transient that the DLTS measurements are based on. The capacitance transient is shown in Fig. 7.2 with the biasing pulse. It can be seen that the capacitance increases from t=0 to a constant value as described by Eq. (7.5). It should be noted that as long as the deep level is a majority carrier trap, i.e. electron trap in n-type semiconductor and hole trap in p-type semiconductor, the capacitance always increases with time as in Fig. 7.2 . The time constant $1/e_n$ depends strongly on the energy of the deep level E_T and the temperature as described by the following equation,

$$e_n = A_o T^2 e^{-\frac{E_T}{kT}}, \qquad (7.6)$$

where A_o is a constant and T is the temperature. If the values of e_n are known at different temperatures, E_T can be determined from the slope of a $\ln(e_n/T^2)$ vs T plot (Arrhenius plot). It is clear that e_n can be determined from the capacitance transient using Eq. (7.5) and the method used in the present experiments is called Boxcar DLTS.

In this method, the capacitance transient is sampled at two points in time, let say t_1 and t_2 as shown in Fig. 7.2, for each temperature. The difference of the capacitance δC at the two sampling points at a particular temperature can be derived from Eq. (7.5) as

$$\delta C = C(t_2) - C(t_1) = \frac{C_o N_T}{2N_D}\left(e^{-e_n t_1} - e^{-e_n t_2}\right). \qquad (7.7)$$

δC is then recorded and plotted against the temperature. δC will go through a maximum at temperature T_{max} as in Fig. 7.3 for the chosen set of sampling points or rate window. A different rate window exhibits a maximum at a different temperature. T_{max} can be determined experimentally by carrying out a temperature sweep and observing the temperature of the

maximum of δC. Differentiating Eq. (7.7) with respect to e_n and setting the result to zero will give $e_{n,max}$ at T_{max} as

$$e_{n,\max} = \frac{\ln(t_2 / t_1)}{t_2 - t_1}. \tag{7.8}$$

It is clear that $e_{n,max}$ is determined by the selected values of t_1 and t_2. Therefore, the emission rate is known for one particular temperature, i.e. one data point is obtained for the $\ln(e_n/T^2)$ vs T plot. The experiment is then repeated for other sets of t_1 and t_2 to generate more data points for the $\ln(e_n/T^2)$ vs T plot. The deep level concentration can also determined from Eq. (7.7) by letting $t_1=0$ and $t_2=\infty$,

$$\delta C_{Total} = C(\infty) - C(0) = -\frac{C_o N_T}{2N_D}, \tag{7.9}$$

where δC_{Total} is the total capacitance change and C_o is the quiescent capacitance, and both quantities can be determined from a capacitance transient curve. N_D is determined from a plot of $1/C^2$ vs V as described in chapter 5. Rearranging Eq. (7.9), N_T can be calculated as

$$N_T = -\frac{2N_D \delta C_{Total}}{C_o}. \tag{7.10}$$

A sample DLTS plot (δC vs T) [7.3] is shown in Fig. 7.4 for a device with two deep levels, which yield two distinct sets of peaks in the plot. Another note about the DLTS measurements is that minority carrier trapping by deep levels may also occur at forward bias in a p-n junction. When a large forward bias is applied to a p-n junction, the concentration of injected minority carriers is high and capturing of the minority carriers by deep levels may be significant. The same set of equations can be used to describe the minority carrier traps. However, the capacitance transient due to a minority carrier trap will be the reverse of a majority carrier trap, i.e. the capacitance decreases instead of increases with time. The method for determining the parameters of a

minority carrier trap is the same as for a majority carrier trap as explained above except that a large forward bias is used during the fill pulse instead of zero bias. It should be noted that using a large forward-bias fill pulse, the majority carrier trap will also be filled. However, the resulting DLTS spectrum should be a summation of the negative minority carrier peaks and the positive majority carrier peaks.

It should be noted that all the arguments described above are equally applicable to a n^+-p junction as in the case for the present experiments. The use of a p^+-n junction for explanation is due to the fact that it is easier to visualize and understand with electrons than holes.

7.3 Experimental

The experiments were carried out with a Polaron model S4600 DLTS system. The block diagram of the system is shown in Fig. 7.5. The Boonton model 72B capacitance meter measured the differential capacitance of the sample at 1 MHz and had a fast response time to allow an accurate measurement of the capacitance transient. The device capacitance was usually offset so that the capacitance transient could be measured more precisely using a smaller capacitance scale. The biasing sequence required for the DLTS as shown in Fig. 7.2 was generated by the pulse excitation unit and applied to the sample. The length of the fill pulse could be selected but the length of the reverse pulse, or the sampling pulse, was fixed for each of the selected sets of rate windows. The signal output of the capacitance meter, a voltage proportional to the measured capacitance, was connected to the signal processing unit through an interface unit.

The signal processing unit sampled the capacitance at three different points in time, t_1, t_2 and t_3, for each measurement so that two rate windows, t_3-t_1 and t_2-t_1, were implemented for each

temperature scan. The capacitance difference for each rate window at a particular temperature corresponded to a data point in a δC vs T curve (Fig. 7.4). δC was positive for majority carrier trap and negative for minority carrier trap. In a DLTS spectrum generated by this system, positive peaks (majority carrier trap) appeared in solid line and negative peaks (minority carrier trap) appeared in dotted line. Therefore, it is very easy to distinguish the type of the trap. The temperature of the sample, which was mounted on a copper platform in an evacuated chamber, was controlled by the a temperature controller. The temperature controller controlled the heating and the flow of liquid nitrogen to the copper platform to attain the desirable temperature. All the units were coordinated by a Hewlett Packard model HP9816 computer through an IEEE-488 bus. The computer also collected the data of the measurements and recorded them in a floppy disk.

Many ZnO/CdS/$CuInSe_2$ cells were studied with DLTS, five of the better cells were studied in detail. One of the DLTS plots is shown in Fig. 7.6. The plot was obtained using a majority carrier fill pulse. There were six curves in each graph and each curve corresponded to one rate window as indicated on the graph. The rate windows were indicated on the graph as the reciprocal of the time difference, i.e. $1/(t_1-t_2)$. The symmetry of the peaks in Fig. 7.6 (D-39) indicates that they were caused by a single deep level. The lack of other local maxima in the DLTS spectrum revealed that no other majority carrier trap existed or, if they did exist, they had a density much lower that the observed one. The observed deep level had an energy of 0.24 eV from the valence band as shown in the Arrhenius plot in Fig. 7.7. The density of the deep level was calculated to be about 7.7×10^{13} cm^{-3}. Another one of the five samples (D-60) also showed almost exactly the same DLTS spectrum with a deep level energy of 0.24 eV and a density of 1.2×10^{14} cm^{-3}, although the $CuInSe_2$ substrates of the two samples were cut from two different ingots. Abou-Elfotouh et al. [1.11] also reported a similar deep level at 0.234 eV with a density

of $1.2x10^{14}$ in their (Cd,Zn)S/$CuInSe_2$ single crystal cell. However, they also observed another deep level at 0.481 eV, which is near the midgap energy, measured at the same temperature range using DLTS as in the present case. Such a mid-gap deep level could be an effective recombination centre that could reduce significantly the device performance. The highest efficiency and open-circuit voltage values obtained for their cells were about 4% and 0.25 V, respectively.

A single crystal $CuInSe_2$ homojunction fabricated in our laboratory [7.4] also showed a majority carrier trap at 0.25 eV, although two minority carrier traps at about 0.18 and 0.34 eV from the conduction band were observed in the homojunction as well, indicating that the minority carrier traps might be created during the homojunction fabrication. From all these results, it seems that this particular majority carrier trap at about 0.24 eV is quite common in single crystal $CuInSe_2$ cells. Giving the different device fabrication procedures for all these different cells, it is plausible to assume that this deep level is an intrinsic level, i.e. it is formed during the crystal growth process rather than from the device fabrication process. However, minority carrier traps were not observed in any of the present samples, even using a fill pulse with forward bias as large as 2.5 V which corresponded to a current density of more than 500 mA/cm^2.

Fig. 7.8 shows another DLTS spectrum (D-100). The broad and non-symmetrical curves of this spectrum indicated the presence of more than one deep level. It is clear that each curve can best be described by the summation of two peaks of comparable magnitude but with energies close to each other. Effort was made to try to estimate the maxima of the two closely-spaced peaks and subsequent Arrhenius plot was made as shown in Fig. 7.9. The maxima that could not be clearly identify were omitted in the Arrhenius plot. The energies of the two deep levels were about 0.198 eV (density $2.8x10^{13}$ cm^{-3}) and 0.135 eV (density $2.5x10^{13}$ cm^{-3}). Another sample

also showed similar DLTS spectrum and with deep level energies of 0.229 eV (density 1.8×10^{13} cm^{-3}) and 0.202 eV (density 1.6×10^{13} cm^{-3}). It is quite possible that the 0.198 eV and 0.229 eV traps were the same one described in the last paragraph, because they appeared at about the same temperature range and with energies close to 0.24 eV. However, the second deep level in the two samples was not reported elsewhere.

DLTS measurements were also carried out on the cell with the highest conversion efficiency (D-102). Surprisingly, no DLTS peaks were observed in this device. For a deep level to be undetectable by the current system, its density has to be much smaller than 10^{13} cm^{-3}. However, it is unlikely that no deep level was present in the sample, and it is more likely the density of deep level was low. Ahrenkiel [5.22] reported that the smaller the density of the deep level, the higher the conversion efficiency. Although it is tempting to conclude similarly that the low density of deep level is one of the reasons of the high performance, more work has to be done to confirm this because only this cell showed the absence of DLTS peaks. Another high-performance cell (D-39, conversion efficiency 10.3 %) also showed the presence of deep levels. However, if deep-level assisted tunneling is really the current mechanism as proposed in chapter 5, smaller deep level density should result in smaller dark current density and, thus, larger V_{oc} and fill factor.

Several non-annealed samples were also characterized with DLTS in order to study the effect of substrate annealing on the deep levels. However, it was found that the DLTS spectrum was dominated by a capacitance transient that did not change with temperature as can be seen in Fig. 7.10 for the sample D-111. The horizontal lines, which appeared below about 270 K, in the δC vs T plot indicated that δC was constant over that temperature range. Furthermore, the dotted line indicated that it was a minority carrier transient, i.e. the capacitance transient was

caused by the emission of minority carriers. The capacitance transient was also monitored during the DLTS measurements. It was found that both a majority carrier transient (solid line in Fig. 7.10) and a minority carrier transient (dotted line in Fig. 7.10) existed at temperatures above approximately 270 K. However, when the temperature reached below 270 K the minority carrier transient became dominant and completely masked off the majority carrier transient. The majority carrier transient was caused by a deep level and changed with temperature as predicted, but the temperature-insensitive minority carrier transient should not be caused by deep level because, otherwise, it would be strongly temperature dependent. This temperature-insensitive capacitance transient was observed in all samples without substrate annealing.

Santamaria et al. [7.5] observed a similar temperature-insensitive capacitance relaxation in some of their CdS/$CuInSe_2$ devices. They attributed this behaviour to the deionization, probably by tunneling, of the high density of interface states which interacted with the Fermi level, thus justifying the lack of temperature dependence of the relaxation. It is speculated that the same mechanism is applicable to the present case, considering the temperature-insensitivity of the capacitance transient and the fact that tunneling was also considered as the conduction mechanism for these devices. It is quite possible that the large density of surface states created by mechanical polishing dominated the capacitance transient. However, the annealed samples generally did not show such a temperature-independent transient, indicating the absence or low density of surface states. It was also found that for several non-annealed samples, after many runs of DLTS, the temperature-independent transient appeared at higher and higher temperature, meaning the magnitude of this transient was getting larger. This is probably caused by a further increase of the density of interface states to the already surface states-ridden interface because it is well known

that thermal stress can cause the increase of interface states. It is believed that the poor-quality interfaces were especially susceptible to effect the thermal stress.

7.4 Conclusions

Deep-level transient spectroscopy has shown the existence of one or two deep levels in the annealed $CuInSe_2$ substrates of the ZnO/CdS/$CuInSe_2$ solar cells. A majority carrier trap at about 0.24 eV was observed in most of the samples. The density of the deep levels generally lay in the range of 10^{13} to 10^{14} cm^{-3}. The absence of DLTS peaks in the cell with the highest conversion efficiency may suggest the photovoltaic performance is related to the density of deep levels, although further work is required to confirm this. A large temperature-insensitive capacitance transient was observed in non-annealed samples and is believed to be due to electron emission from a large density of surface states. Such surface states were not observed in annealed samples.

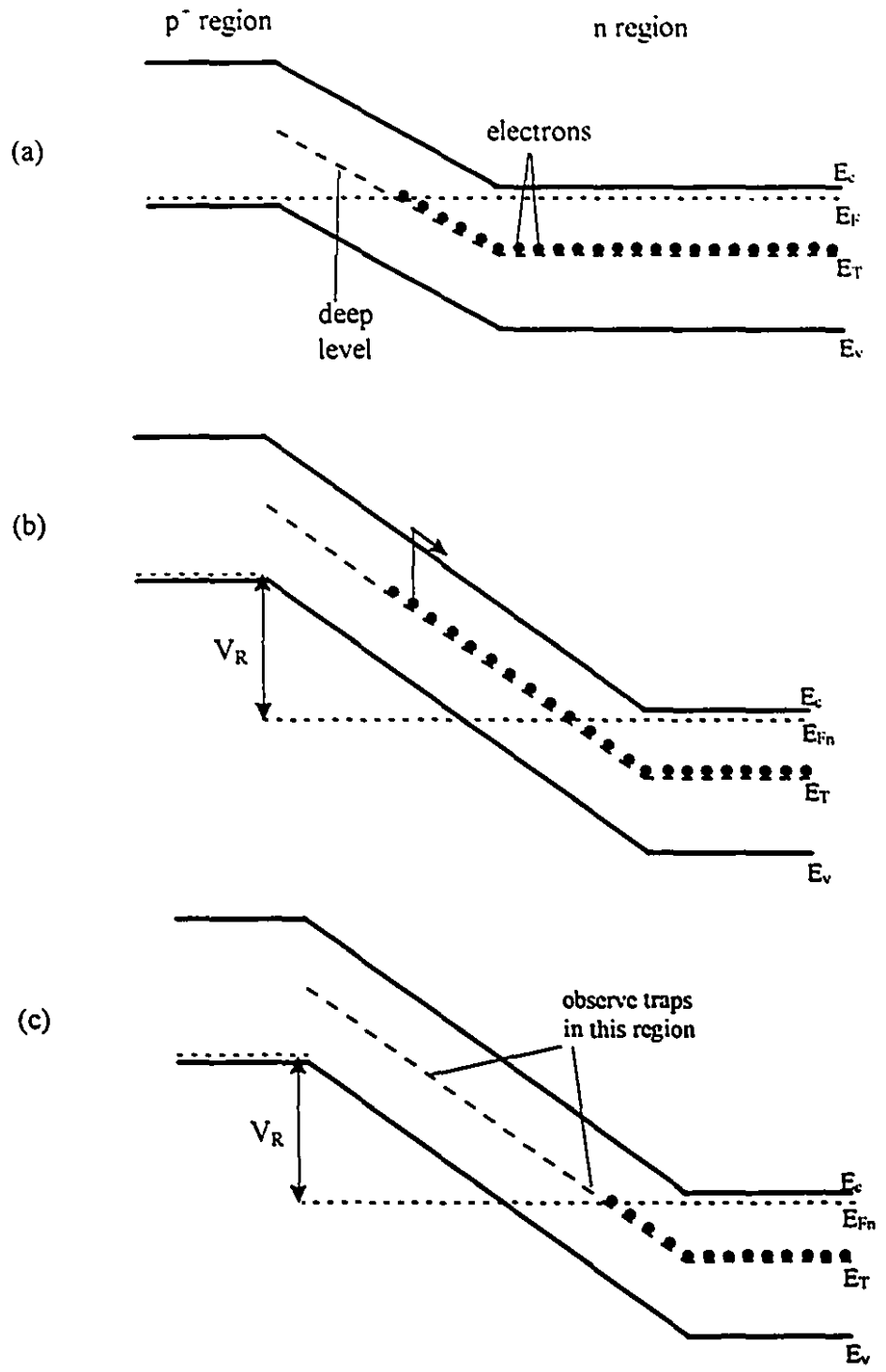


Fig. 7.1 A p⁻-n junction (a) at zero bias, (b) reverse bias, $-V_R$, at t=0, (c) reverse bias as $t \rightarrow \infty$.

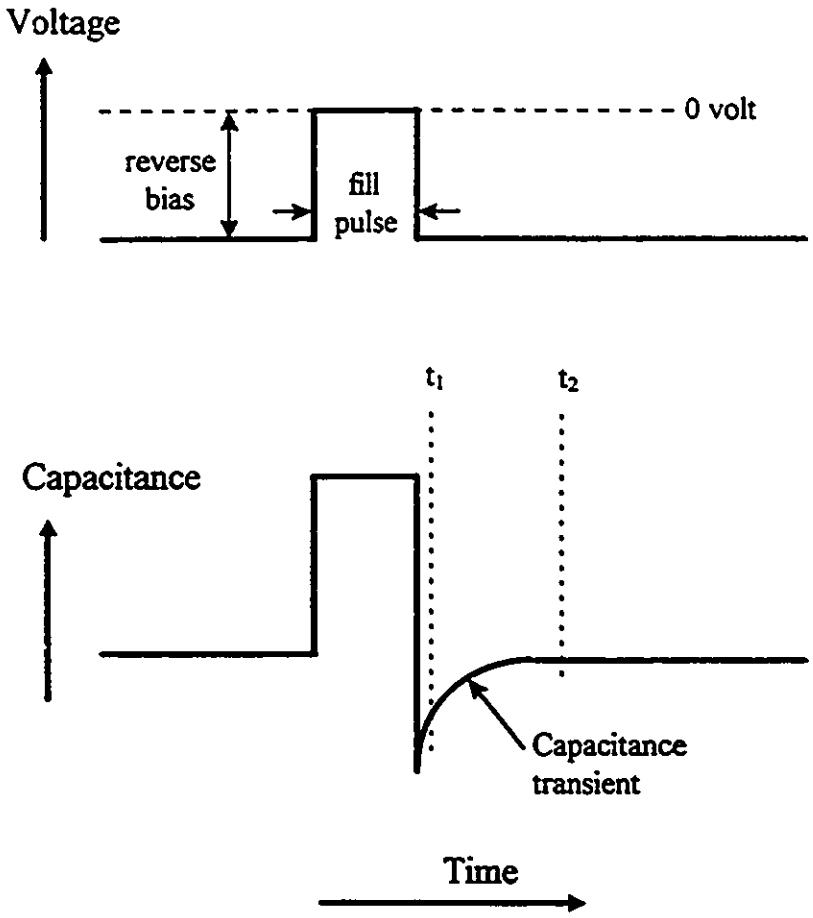


Fig. 7.2 The applied voltage waveform and the corresponding capacitance transient. t_1 and t_2 are the sampling points for DLTS measurements.

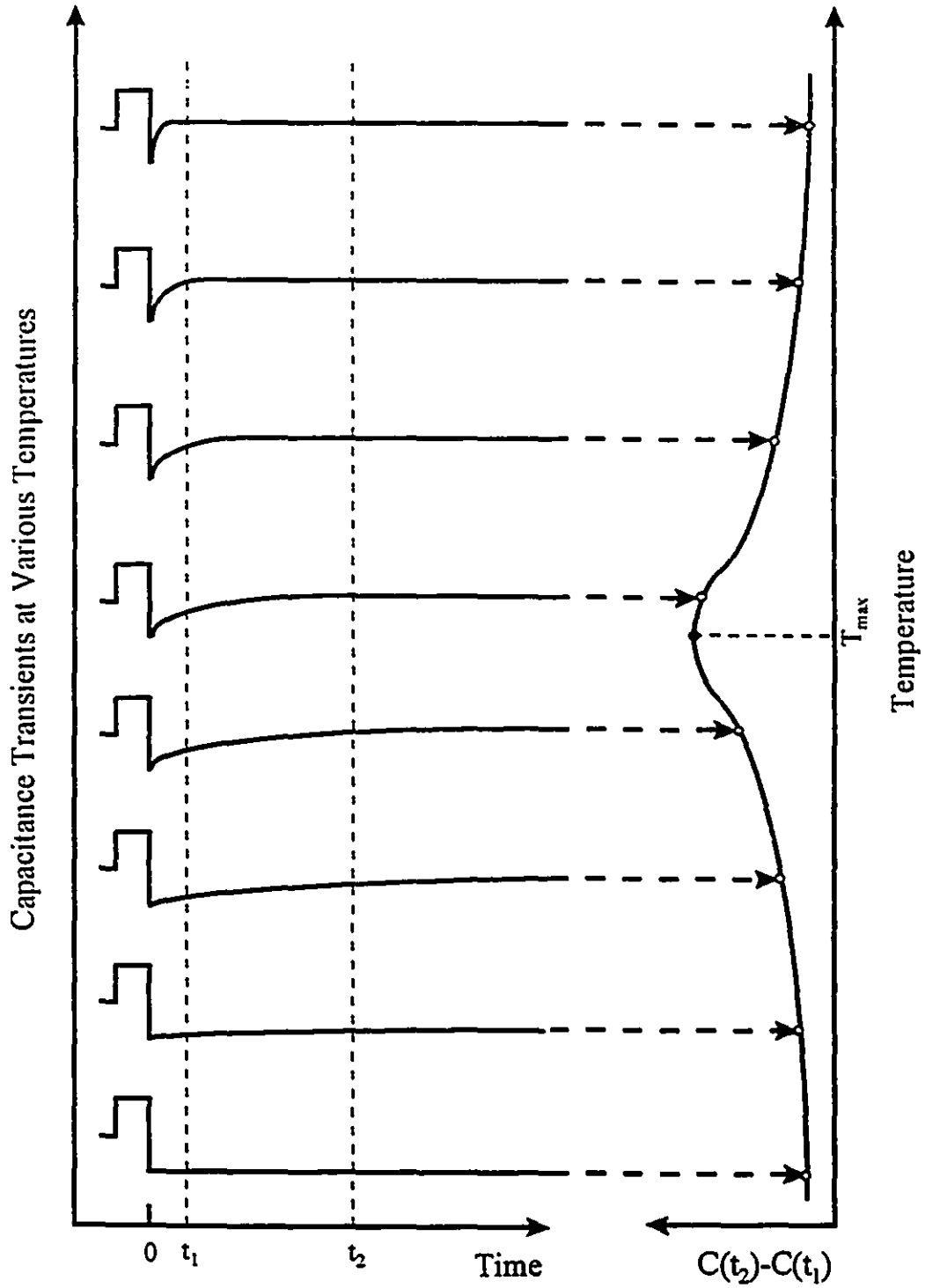


Fig. 7.3 Implementation of a rate window for DLTS measurements. The output is the average difference of the capacitance amplitudes at the sampling times t_1 and t_2. [7.2]

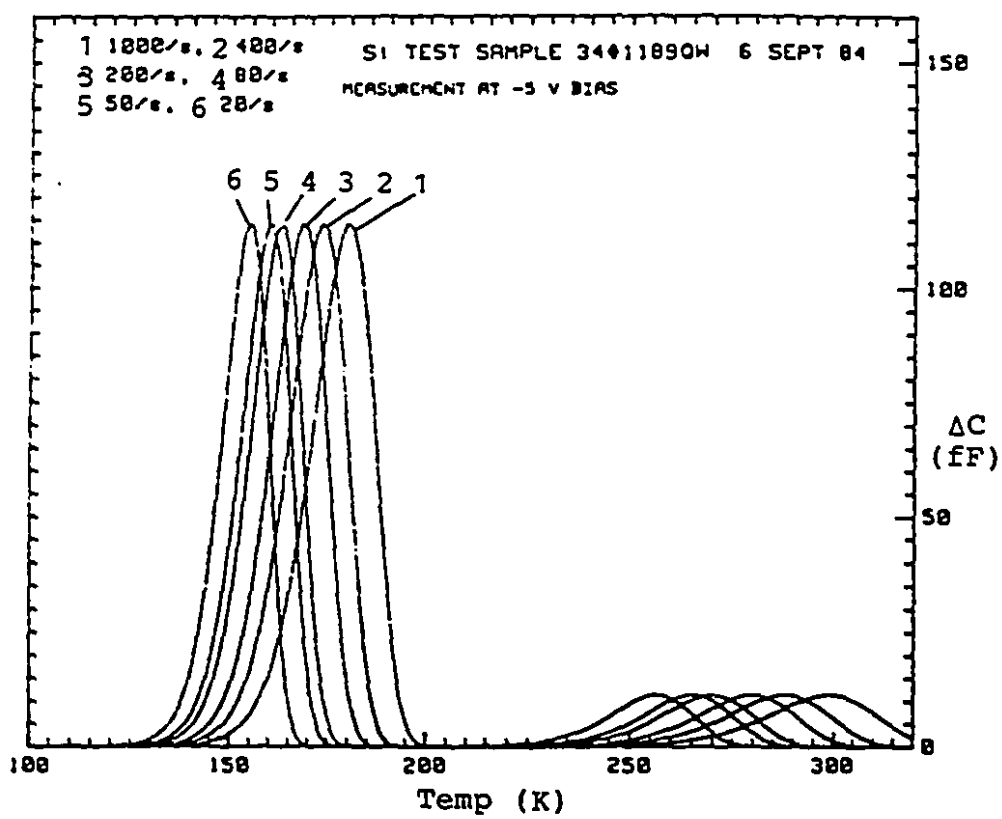


Fig. 7.4 A sample DLTS plot. [7.3]

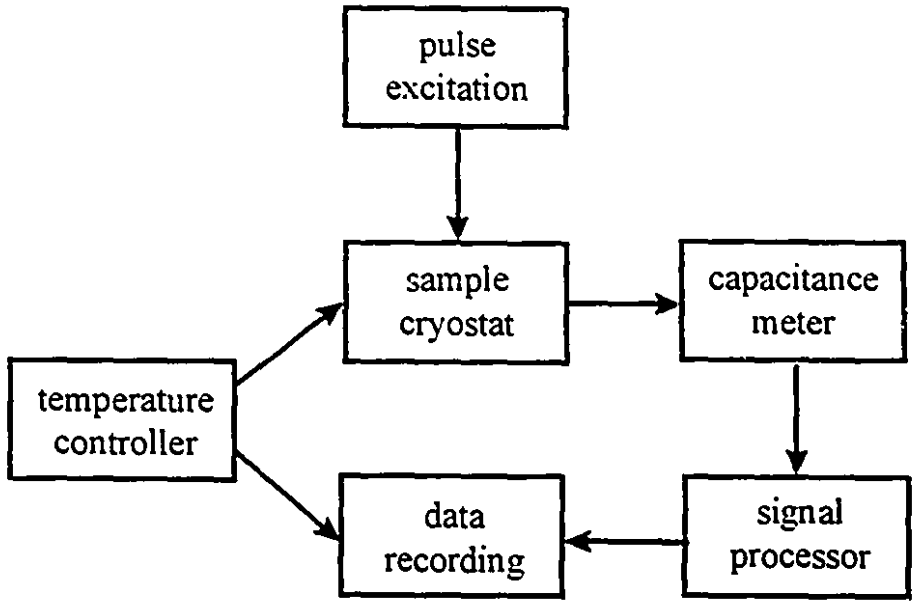


Fig. 7.5 Block diagram of DLTS system.

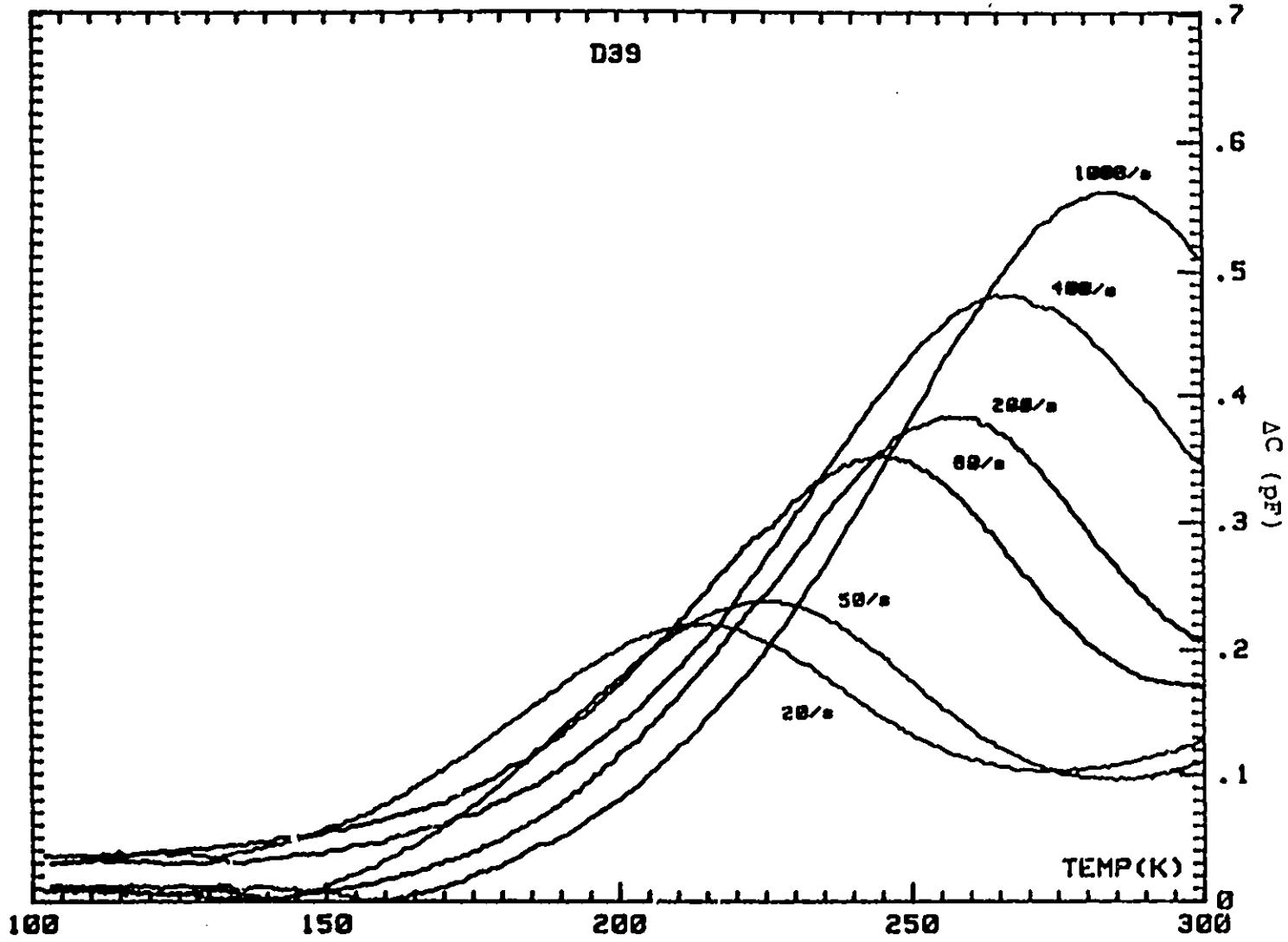


Fig. 7.6 DLTS spectrum of the sample D-39.

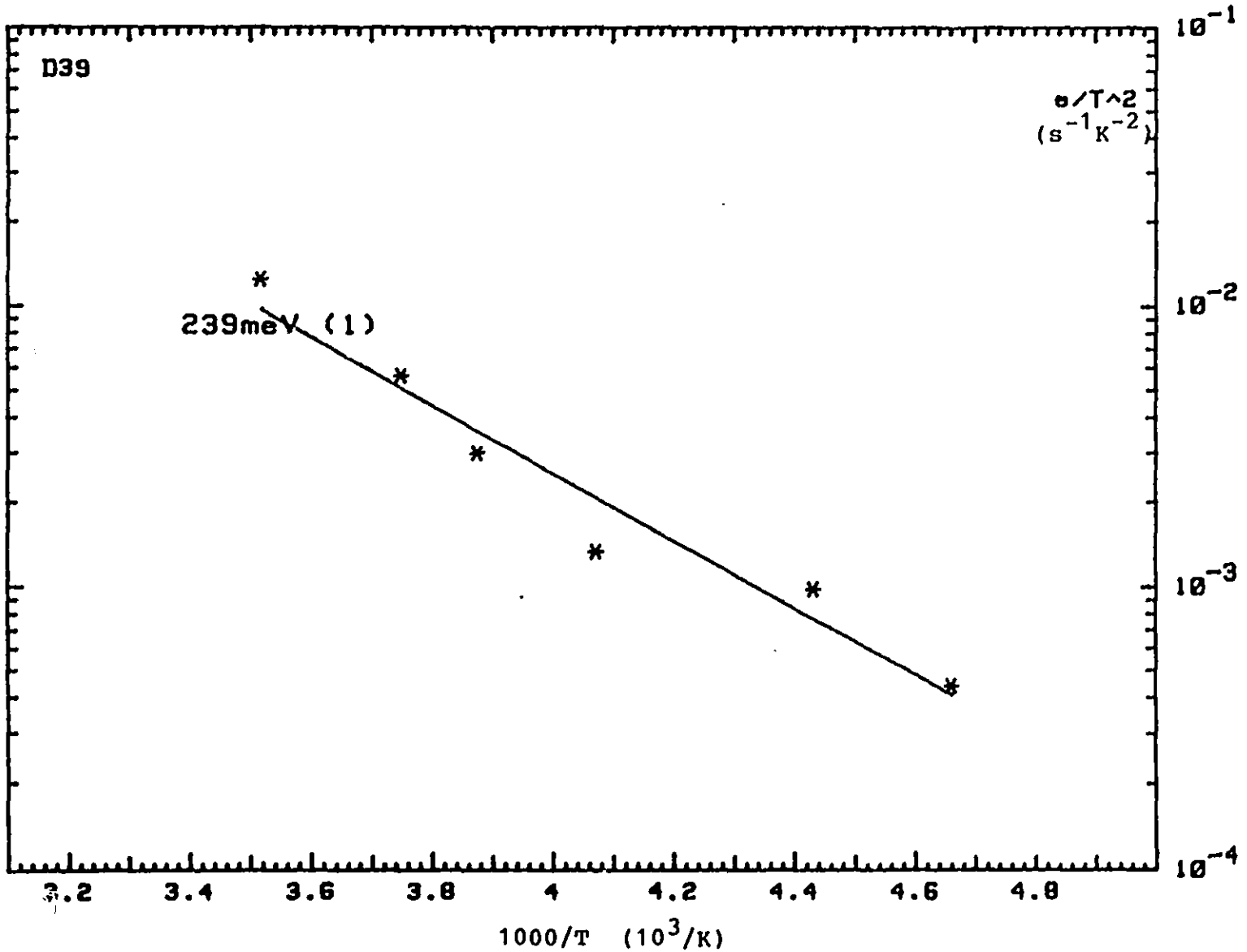


Fig. 7.7 Arrhenius plot of the sample D-39.

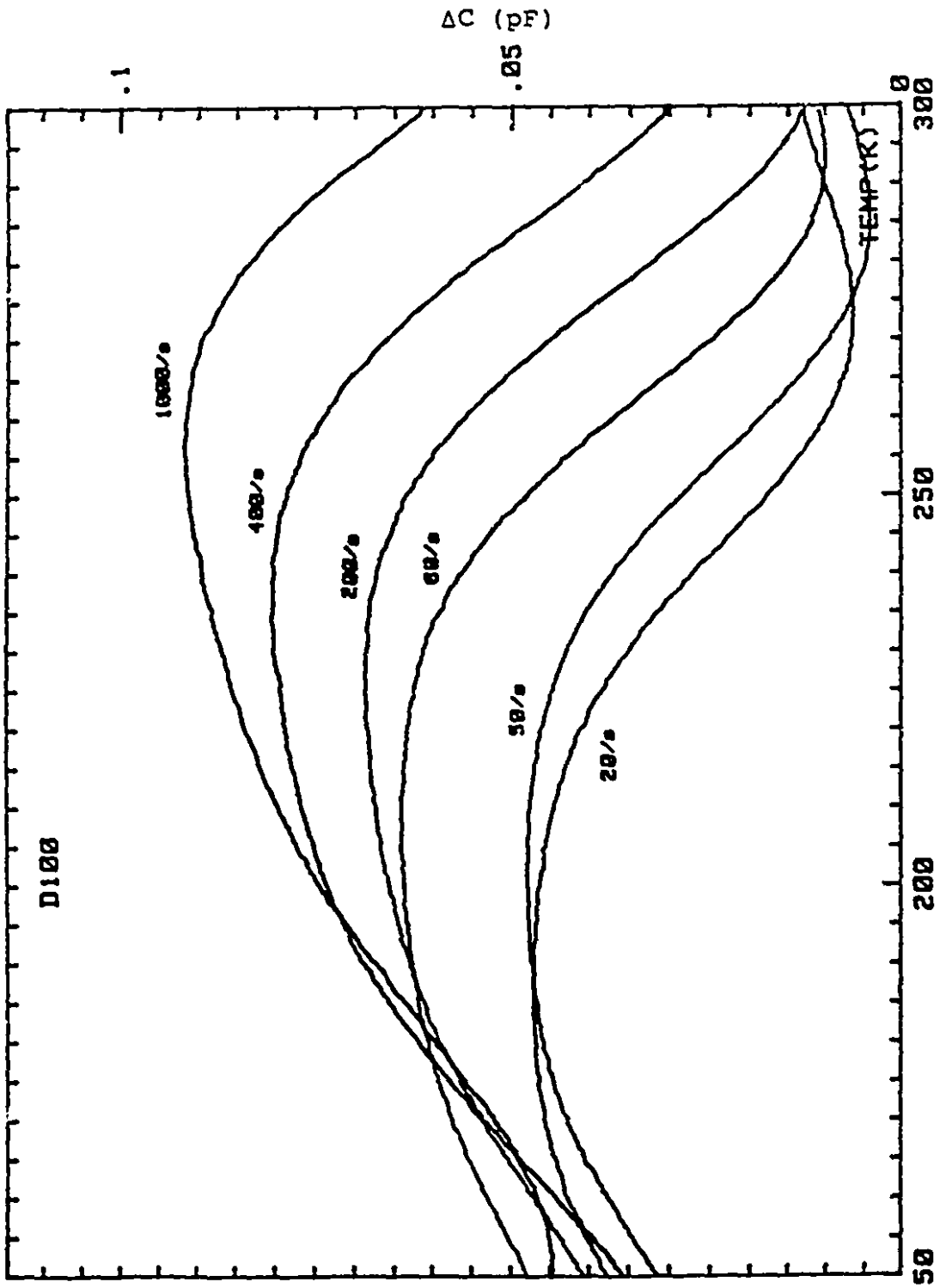


Fig. 7.8 DLTS spectrum of the sample D-100.

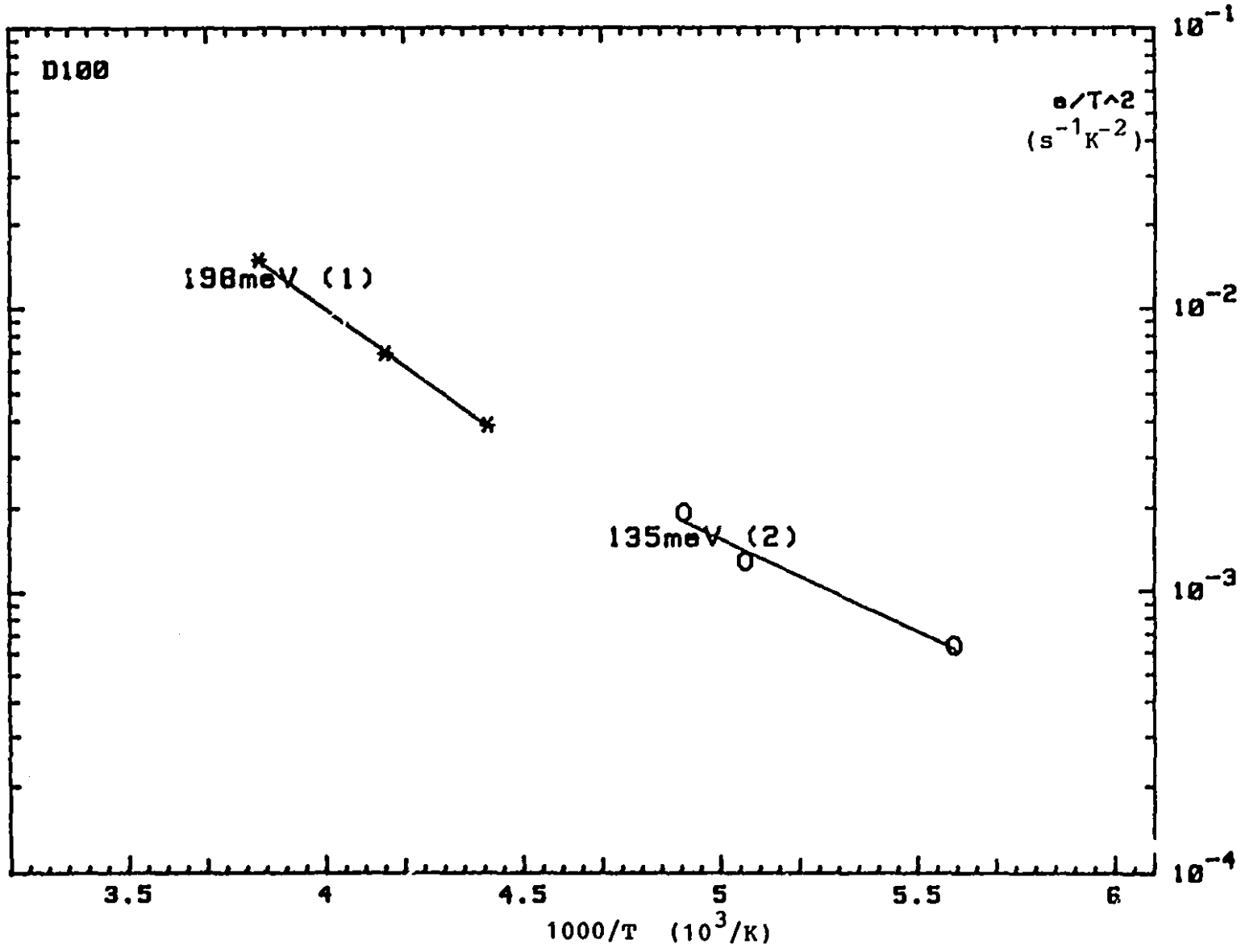


Fig. 7.9 Arrhenius plot of the sample D-100.

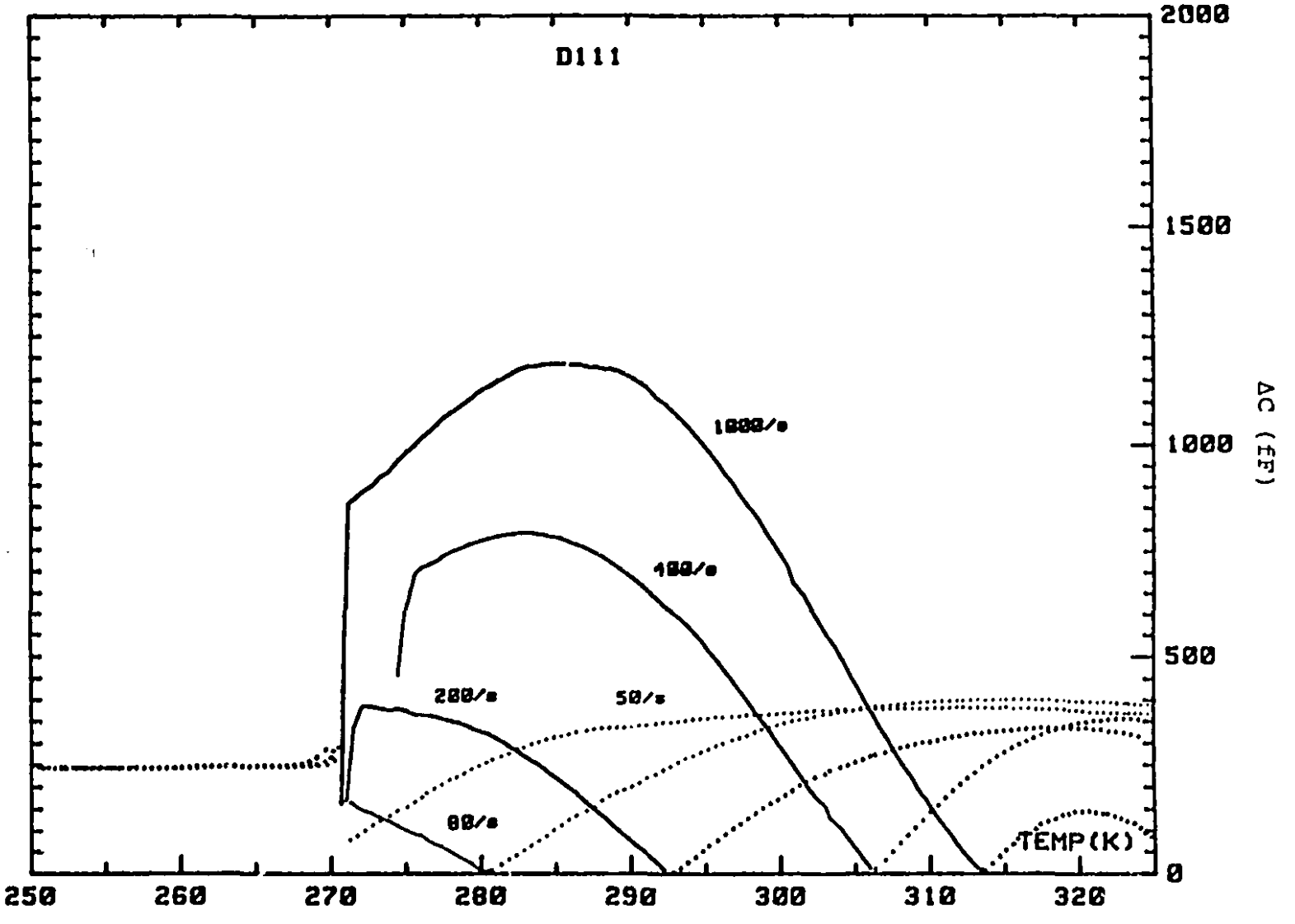


Fig. 7.10 DLTS spectrum for a non-annealed sample (D-111). Dotted lines represent minority carrier transients and solid lines represent majority carrier transients.

CHAPTER 8

CONCLUSIONS

High-efficiency photovoltaic cells in the form of ZnO/CdS/$CuInSe_2$ have been fabricated on monocrystalline $CuInSe_2$ substrates in the present work. Energy conversion efficiencies of more than 10 % have been achieved. The $CuInSe_2$ single crystals were grown by a horizontal Bridgman method; while the CdS buffer layer and the ZnO window layer were deposited by a chemical-bath deposition method and r.f. magnetron sputtering, respectively. The best cell prepared in the present work had a conversion efficiency of 11.5 % and an active area of 4 mm^2. This cell is comparable in conversion efficiency to the highest value of 12 % [1.3] reported in the literature for single-crystal $CuInSe_2$ cells but has an active area about five times larger than the 12 % cell. A 10.3 % conversion efficiency was also achieved on another cell with an active area of 8 mm^2. By contrast to the 12 % cell, antireflection coating was not used in the present cells.

Crystal growth experiments were carried out with a horizontal Bridgman system to produce the $CuInSe_2$ substrates. One of the main difficulties in earlier crystal growth experiments was the adhesion of the $CuInSe_2$ ingot to the inner wall of the quartz ampoule after the growth. A technique was developed to overcome this problem. This was done by the inclusion of a layer of carbon coating or a piece of solid graphite as a gettering agent into the sealed ampoule. The gettering agent was found to be effective in removing the sticking agent, probably O_2, from the starting materials. Specially made ampoules were used to separate the gettering agent from the $CuInSe_2$ melt to minimize contamination. Using this method, large void-free and microcrack-free $CuInSe_2$ single crystals of up to 2 cm on a side were obtained. Ingots grown by this method

were usually uniformly p-type with a hole concentration of about 10^{17} cm^{-3}. The composition inside each $CuInSe_2$ ingot was also found to be uniform.

Slices were cut from the $CuInSe_2$ ingots as the substrates for the photovoltaic cells. The $CuInSe_2$ surfaces were then prepared by mechanical polishing, etching with a 0.5 % brome-methanol solution and annealing in Ar at 350 °C for 2 hours. Good polishing was found to be important in obtaining high-performance cells. However, one of the most important fabrication steps in achieving high efficiency was the substrate annealing. Cells prepared with substrate annealing almost always showed a conversion efficiency of more than 8 %. The open-circuit voltage and fill factor were found to be improved with substrate annealing; while no apparent gain was observed for the short-circuit current density. The performance of the cells was also dependent on the quality of the $CuInSe_2$ crystals.

Spectral response measurements showed that the charge carriers generated by low-energy photons were not effectively collected, probably due to the small depletion width in the $CuInSe_2$ substrates. The reduced spectral responses for photons with energies larger than the energy band gap of CdS but smaller than the band gap of ZnO indicated that the light absorption by the CdS buffer layer might not be negligible. Furthermore, the overall spectral responses were relatively low compared to other $CuInSe_2$ cells, indicating the possibility of a large reflection of incident light.

The current mechanism of a non-annealed cell was believed to be multiple tunneling assisted by a large density of defect states on the $CuInSe_2$ surface. The multiple tunneling led to a large dark junction current that reduced the open-circuit voltage and fill factor of the cells. Such surface defect states were probably caused by the mechanical polishing and their existence was confirmed by DLTS measurements. Substrate annealing was found to be able to remove these

surface states and to improve substantially the photovoltaic performance. The current mechanism of the annealed samples was believed to be a combination of deep-level assisted tunneling and recombination in the $CuInSe_2$ depletion region. Two tunneling components dominating at different voltage and temperature ranges were found in most of the cells. Capacitance-voltage measurements of the ZnO/CdS/$CuInSe_2$ cells suggested the existence of interface states and deep levels. The interface-state effect could be minimized at high frequencies. Carrier concentration of the $CuInSe_2$ substrates was determined from high-frequency C-V measurements and found to be quite uniform even for the samples with annealing.

Electron-beam-induced-current measurements showed that the buried homojunction found in CdS/$CuInSe_2$ junctions did not exist in the present ZnO/CdS/$CuInSe_2$ cells. A large electric field was observed at the metallurgical junction, indicating the heterojunction was active and responsible for the high photovoltaic performance. The diffusion lengths of the $CuInSe_2$ substrates were also determined by EBIC measurements and were found to be in the range of 4 to 6 μm. Deep-level transient spectroscopy revealed a deep level with an energy of about 0.24 eV from the valence band edge in most of the $CuInSe_2$ crystals. A second deep level was also observed in some samples. The deep level concentrations were about 10^{13} to 10^{14} cm^{-3}. The capacitance transient of non-annealed samples was always masked by a temperature-insensitive component, which can be attributed to a large density of defect states on the $CuInSe_2$ surfaces.

Several suggestions are given here for possible further improvements in photovoltaic performance of the ZnO/CdS/$CuInSe_2$ cells. First of all, the carrier concentration of the $CuInSe_2$ substrates may be reduced to increase the depletion width for better collection of charge carriers generated by low-energy photons. This can be achieved by changing the conditions or starting composition for crystal growth or by annealing the $CuInSe_2$ substrates in appropriate conditions.

Secondly, the quality of the CdS buffer layer may be improved to reduce the absorption of high energy photons and to increase the bonding to the $CuInSe_2$ substrates. This can be achieved by changing the deposition conditions or the composition of the chemical solution. Thirdly, an improved $CuInSe_2$ surface preparation method such as a chemical-mechanical polishing and the use of (112) $CuInSe_2$ surfaces may further improve the quality of the heterojunction. Fourthly, an effective antireflection coating may be required to reduce the reflection of incident light and, thus, increase the short-circuit current density. Fifthly, a more detailed study of deep levels related to substrate annealing and device performance may lead to improved fabrication procedures because deep levels seem to be playing an important role in the electrical properties of the heterojunction.

Finally, the main contributions of the present work are summarized in the following list. From the research, the author:

1. developed a technique to eliminate the commonly encountered adhesion problem in $CuInSe_2$ crystal growth experiments;
2. grew large and high-quality $CuInSe_2$ crystals suitable for solar cell fabrication;
3. developed an annealing process and established the conditions that can substantially increase the surface quality of the $CuInSe_2$ substrates;
4. developed a fabrication process that can routinely produce single-crystal $CuInSe_2$ solar cells with conversion efficiency near or more than 10 % and with relatively large active area;
5. fabricated a relatively large-area cell with conversion efficiency of 11.5 %, which is close to the two-decade-old record of 12 % for monocrystalline $CuInSe_2$ cells;
6. investigated the substrate annealing effect on photovoltaic performance;
7. investigated the current transport mechanism in ZnO/CdS/$CuInSe_2$ cells;

8. proved the non-existence of buried homojunction in the ZnO/CdS/$CuInSe_2$ structure, at least for cells fabricated on single-crystal $CuInSe_2$ substrates;
9. studied the deep levels in $CuInSe_2$ crystals; and
10. proved the existence of a large density of surface defect states on mechanically polished $CuInSe_2$ surfaces.

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