

Substrate Coupling Analysis and Noise Reduction Methods

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Abstract

The trend of system-on-a-chip carries on the end of the VLSI era to fulfill the ever-rising demands of electronics industry. As system complexity increases, interconnect becomes the dominant factor over transistor sizes in determining the overall performance. Theoretically, systems-on-a-chip implementations eliminate most packaging interfaces to improve the system-level performance. Manufacturing cost is also reduced by integrating both analog and digital circuits using monolithic CMOS technologies. Unfortunately, substrate coupling is found to be a major obstacle for the advancement of system-on-a-chip. Accurate predictions of substrate coupling in large-scale systems demand a modeling algorithm with high speed and high resolution, which are difficult to achieve simultaneously. This thesis provides a comprehensive approach towards predicting and preventing substrate noise coupling issues in large systems efficiently. We are primarily interested in modeling the epitaxial-type heavily-doped bulk substrate, that is commonly used in system-on-a-chip designs. An efficient substrate parasitics extraction algorithm based on Delaunay triangulation is proposed. It is optimized for large-scale design applications. Active noise suppression circuits that improve guard band noise insulation efficiency are also developed. SPICE simulation results of circuit layouts comprising the proposed substrate model are compared against those with substrate models generated from Cadence Assura[®] Substrate Coupling Analysis tool. Various experiments are performed to obtain fabrication-related substrate parameters, measure the circuit performance and validate the modeling results.

Résumé

La tendance des systèmes-sur-une-puce transporte le domaine de la VLSI vers les exigences croissantes de l'industrie de l'électronique. Avec l'augmentation de la complexité des systèmes, les fils de connection prennent la place du transistor comme le facteur dominant de la performance. En théorie, les systèmes-sur-puce éliminent la plupart des interfaces de l'emballage pour améliorer la performance au niveau système. Le coût de fabrication est également réduit en intégrant les circuits analogiques et numériques sur une même puce monolithique CMOS. Malheureusement, le couplage au niveau du substrat se trouve à être un obstacle considérable au développement des systèmes-sur-puce. La prévision précise du couplage au niveau du substrat dans les systèmes à grande échelle exige un algorithme de modélisation possédant à la fois une grande vitesse et une grande résolution, ce qui est difficile à atteindre. Ce mémoire de maîtrise propose une méthodologie complète avec pour but la prévision et l'empêchement efficaces des phénomènes de couplage du substrat dans des systèmes à grande échelle. Nous sommes principalement intéressés à modéliser le substrat épitaxial de fort dopage. Nous proposons un algorithme efficace d'extraction des parasites du substrat basé sur la méthode de triangulation Delaunay. Il est optimisé pour des applications de conception à grande échelle. Des circuits d'élimination de bruit qui améliorent les propriétés isolatrices des 'guard ring' sont également développées. Des résultats de simulations SPICE effectuées sur des layouts comprenant le modèle proposé sont comparées à celles avec des modèles générés à partir de l'outil 'Cadence Assura® Substrate Coupling Analysis'. Plusieurs expériences sont effectuées pour obtenir des paramètres liés à la fabrication, mesurer la performance du circuit, et valider les résultats du modèle.

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I thank Micronet for their financial support that enabled me to complete my research. Also, the Canadian Microelectronics Corporation (CMC) provided me with the unparalleled experience of fabricating custom chips through access to Taiwan Semiconductor Manufacturing Corporation's (TSMC) CMOS processes, free of charge. They also supplied a large share of the test equipment used for this work.

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Contribution of Authors

The core of the original work on the development of the substrate parasitic extraction algorithm (GEOMEXT) and active noise suppression (ANS) circuits are located in Chapter 3 and 4 respectively. An experimental Managed Clock System-on-a-Chip (MCSoc) is used to test GEOMEXT. The development of the MCSoc project is a collaboration of four students: Ian Brynjolfson, Boris Polianskikh, Yanai Danan and the author of this thesis, Henry H. Y. Chan.

Chapter 3 presents the efficient GEOMEXT algorithm and the related experiments in modeling substrate coupling in the mixed-signal environment. Detailed description of the substrate models generated by the algorithm is given. This simplified method of substrate extraction scheme was not previously employed. The use of Voronoi Tessellation algorithm is based, in part, on the relatively complex scheme developed by Wemple et al. in [14], as discussed in Section 3.2. The ideas are also outlined in [1], coauthored with Prof. Zeljko Zilic. Also, the layout extraction rules was adapted by the author of this thesis for the requirements of both GEOMEXT and Cadence[®] Substrate Coupling Analysis (SCA) algorithms.

Chapter 4 presents ANS circuits. The implementation using digital inverters is original, while the translinear amplifier design was inspired by amplifier designs described in [20]. The ANS circuits are also discussed in [2], coauthored with Prof. Zeljko Zilic. The novelty of the inverter-based ANS circuits comes from the use of compact and configuration-free digital inverters to enhance the shielding efficiency of guardbands. ANS can be used extensively, thus results in significant savings on silicon area.

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Chapter 1 - Introduction

The perpetual goal in microelectronics is to achieve higher performance systems with lower cost. This goal has been achieved through miniaturization of integrated circuit (IC) feature sizes and packaging geometries. Traditionally, due to the generous noise margin of CMOS digital logic gates, predominant design constraints focus on high speed, low power operations and minimal area consumption. The silicon substrate and interconnect conductivities are considered to be practically infinite and neighboring nodes are assumed to be ideally shielded. Crosstalk and substrate noise problems were resolved using thoroughly tested legacy design topologies and techniques. However, today's industry prompts for even faster prototyping and system-level integration to achieve higher performance and lower cost. Digital logic circuits and analog circuits are being fabricated on a single silicon die to reduce interconnect parasitics and packaging costs, hence results in a mixed analog-digital system supported by a common substrate. Because of this fundamental shift in the operating environment, the reliance on legacy design techniques in resolving substrate noise problems becomes inadequate. Therefore, an efficient substrate modeling algorithm is urgently needed.

1.1 - Motivation

As single chip solutions often offer the best performance in terms of cost, area, speed and power, large-scale mixed signal systems and system-on-a-chips (SoCs) begin to dominate in today's high performance system implementations. While the new paradigm of SoC

design environment allows rapid prototyping of complex systems and mixed-signal system-level integrations, verification and testing strategies must be extended to cope with the emerging substrate noise problems. The goal of integrating multi-million-gates SoCs further raises the importance of substrate coupling, besides issues of power consumption, packing density and long-term reliability. In state-of-art high-speed deep-submicron ICs, even pure CMOS logic designs are limited by the effect of switching-induced power supply noise. Clearly, integrating any analog circuits successfully near digital circuitry requires some kind of robust noise reduction scheme to shield against heavy dosages of substrate coupling interference.

In order to achieve an effective and area-efficient shielding scheme, an accurate substrate modeling algorithm becomes crucial. Moreover, to be able to apply it on large systems, the modeling algorithm should not only be accurate, but fast in execution. The demand of a robust noise reduction scheme for large systems creates new challenges in devising accurate, yet efficient substrate modeling algorithms. While an overly simple model does not reflect realistic substrate coupling effects, simulating an excessively complex substrate model can easily lead to a bottleneck in the entire design flow. Thus, the problem of modeling substrate coupling in large systems must be resolved before SoC systems can offer the promised performance advantages.

1.2 - Substrate Modeling

Efficient modeling of substrate coupling is essential for high-performance mixed-signal design. Unlike $1/f$, thermal and shot noise, which originate in circuit devices internally due to the discrete nature of the charge carriers, substrate coupling takes place externally. It is the non-ideal interference among different components via the common substrate. $1/f$, thermal and shot noise are modeled by adding random signal sources within integrated circuit device models, while substrate coupling is modeled by including the conduction paths for the substrate. In other words, substrate coupling process can be simulated in conventional circuit simulators simply by including the associated parasitic devices to the netlist during extraction. However, since the parasitic devices depend strongly on the

layout geometry of the circuit, the time required to generate the substrate model grows with the size and complexity of the circuit. A typical substrate model is often large, as it includes parasitics information for all the possible coupling paths. Moreover, the model is complicated by the 3-dimensional nature of the substrate. Since a large model may be needed even for moderately large mixed-signal designs, the execution time for SoC substrate noise analysis can easily become prohibitively long.

In this thesis, we investigate an efficient substrate extraction algorithm to yield accurate substrate models. The primary objective of our extraction algorithms is to optimize the extraction and simulation speeds of substrate models for monolithic CMOS process, the technology of choice for mixed-signal integrated circuits. Due to the large amount of possible conduction paths needed to be considered, spatial discretization is the major overhead of the entire modeling process. It is a vital step to transform the problem of solving the continuous current densities into a netlist simulation problem, suitable for fast computer processing. Since spatial discretization directly affects the model complexity and thus the simulation process, the overall execution time can essentially be shortened by improving the discretization algorithm.

1.3 - Substrate Discretization Algorithm

Relative to circuit simulation optimization, the field of substrate parasitics extraction is relatively new. In contrast to rectangular mesh network, our substrate models are triangular-based, using the *Delaunay Triangulation* algorithm. This algorithm is capable to form moderate-size substrate models, which preserve only the critical substrate conduction paths. The rectangular- and triangular-based substrate discretization methods are examined in Chapter 2, followed by our approach to generate reduced models by using a triangular grid extraction scheme in Chapter 3. With the substrate parasitic components included in the circuit netlist, accurate spatial and temporal solution of substrate potentials and coupling effects can be obtained through circuit simulations. We also developed two compact active circuits that help reducing substrate noise. They will be discussed in Chapter 4. As a result, mixed-signal designers are able to place the active noise

suppression circuits and the passive shielding strategically around sensitive circuitry to block substrate noise interference.

It is demanding to formulate an accurate, yet compact substrate model, as any inefficiency in its formulation can impose excessive resource requirements for extraction and simulation. Existing tools in extracting substrate parasitic components are intended for radio-frequency circuit design applications. They can only practically handle small-scale circuits on the order of a hundred transistors [35].

1.4 - Thesis Outline

A brief description of the mixed-signal environment and its issues are given in Chapter 2. It includes a discussion of mixed-signal systems, substrate profile, and the fabrication technology of choice. Substrate coupling problems confronted by the mixed-signal system designers are also discussed, including a brief introduction to the Voronoi tessellation algorithm. Our substrate parasitic extraction algorithm, GEOMEXT, is explained in Chapter 3. Its implementation into the Cadence Design Environment is explained in detail, followed by circuit simulations of substrate coupling in the light of the GEOMEXT substrate models. The use of active circuits to enhance passive guard rings in reducing substrate noise is explored in Chapter 4. The proposed substrate coupling reduction methodologies are applied to the MCSoc project, a joint research project for next-generation system-on-a-chip designs. MCSoc is a comprehensive experimental platform for prototyping novel technologies for System-on-a-Chip (SoCs). Lastly, our conclusion is given in Chapter 5.

Chapter 2 - Mixed Signal Environment and Substrate Coupling

Integrated circuits (ICs) are interconnections of conducting and semi-conducting materials. These materials, which constitute the devices and interconnects of the circuits, are grown on an electrically inert substrate for mechanical support. Insulating materials are used to electrically isolate interconnect layers. The dielectric improves the electrical insulation against spurious electro-magnetic interference among distinct electrical nodes. However, maintaining adequate isolation is becoming more difficult to achieve, due to the miniaturization of fabrication technologies and design area limitations. Consequently, substrate coupling and crosstalk problems begins to reappear.

Mixed analog-digital systems have potentials to provide robust and economical solutions for high-performance applications. The widespread interest in high-performance wireless and portable devices has driven the trends in integrating the entire complex system on a single chip. Integrating analog and digital circuits on the same substrate can significantly reduce the manufacturing cost, propagation delays, area and power consumptions. However, the electrical isolation offered by the substrate is compromised. This conduction through the substrate due to its non-ideal insulation is known as *substrate coupling*. The spurious signal as a result of substrate coupling is known as *substrate noise*. Substrate noise can be generated by analog circuits, such as high-current analog power drivers, or by

digital networks, such as CMOS logic gate transitions in combinational logic networks. On the other hand, substrate coupling interferes with both digital and analog circuits through the body contacts of MOS transistors connected to the substrate.

2.1 - Mixed-Signal Systems

In high-performance electronics, high-resolution analog components and high-speed digital circuits are often required. Advances in VLSI fabrication technologies make integrating both of these components onto a single die possible. By reducing interconnect and package inductances, tightly coupled high-speed digital and precision analog circuits improve the overall power and speed performance while aggravate substrate coupling.

Analog power drivers and digital logic gates inject current into the substrate as they charge and discharge their loads. This type of noise is caused by the sudden discharge of electrons or holes during a transistion. It is often known as *switching noise*. When high-current transitions or simultaneous switching of a large number of transistors occur, transient peaks of the substrate potentials in the order of 0.1V can often be observed. Depending on the substrate doping profile and the layout geometry, the noise propagating in the substrate can either be absorbed by substrate contacts or coupled to other devices. Owing to the intrinsic regenerative mechanisms, signal integrity in all-digital designs is usually maintained by the high noise margins despite the noisy environment. Nevertheless, potential soft logic errors can result. Jitter performance of timing circuits also deteriorate. On the other hand, analog circuits are generally more susceptible to noise. For instance, amplifier gains can experience transient fluctuations, and resolutions of analog-to-digital or digital-to-analog converters are reduced. Some form of shielding is needed in the mixed-signal environment to insulate them against switching noise interference.

Traditionally, designers apply various *ad hoc* noise rejection schemes, such as placing guard rings around sensitive components and power supply isolations to reduce substrate-coupled interference. Guarding structures provide low-impedance absorption paths for the substrate or well to prevent the noise from further propagation. Nonetheless, the intensity of substrate coupled interference is determined by the specific substrate profile and local

layout geometry. Any successful design tools and verification methodologies for SoCs must include the effect of substrate coupling as an important design constraint. Clear understanding of the substrate profile in use and substrate coupling processes are vital to develop area-efficient shielding schemes for SoCs. The substrate profile and methods for suppressing substrate noise are described in Section 2.2 and 2.5 below, respectively.

2.2 - Substrate Profile

Two commonly used substrate profiles are the uniformly-doped (*bulk*) and heavily-doped epitaxial (*epi*) processes, as shown in Figure 2.1. The bulk process with uniform resistivities (Figure 2.1(i)) is commonly used in RF and analog designs. On the other hand, digital and SoC designs favor the heavily-doped epitaxial process (Figure 2.1(ii)). A third, less common type of substrate profile is the lightly-doped bulk epitaxial process. It is similar to the heavily-doped epitaxial process, except that the epitaxial layer is highly conductive and the bulk is highly resistive. From now on, we shall refer the *epi* process as the heavily-doped epitaxial process, unless otherwise specified.

The thin epitaxial layer of the *epi* process provides good near-range substrate noise attenuation. The heavily-doped bulk layer underneath reduces the far-range substrate parasitic resistance for better latch-up prevention and ensures uniform substrate voltage across the silicon die. A p-type substrate n-well *epi* process will be assumed from this point on.

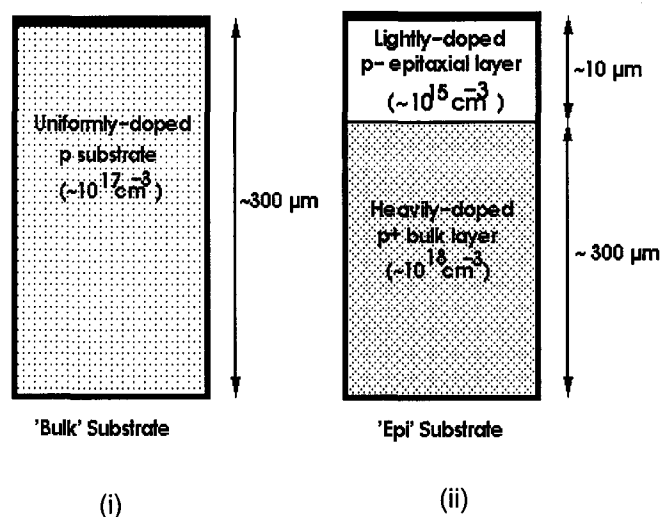


Figure 2.1: Typical substrate doping profiles: (i) 'Bulk' substrate with uniform resistivity and (ii) 'Epi' substrate with low resistivity bulk

2.3 - Choice of Technology

Mixed-mode analog and digital systems can be accomplished by various fabrication technologies. Monolithic Complementary MOS (CMOS) and Bipolar CMOS (BiCMOS) are among the most popular candidates. CMOS technology offers advantages such as high input and low output impedances, high and symmetrical noise margin, high packing density and low power dissipation [3]. The major disadvantage of CMOS is the relatively low current-driving capability, resulting in lower gain and bandwidth than bipolar transistors as the fanout or capacitive load increases. During its initial years of introduction about a decade ago, the BiCMOS approach brought about new opportunities for mixed-signal systems. It combined the advantages of the high-density integration of CMOS logic, high current-driving capability of BiCMOS buffer and high transconductance *npn* bipolar transistors. Since *npn* transistors were individually isolated by *n*-wells in BiCMOS processes, substrate coupling problems were also less severe.

However, due to the present trends in technology, the performance of CMOS devices has been rapidly catching up the BiCMOS counterparts. To strive for improved performance, not only does the amount of integration of analog and digital circuits on a single chip increase, but we also witness the growth in overall size of the integrated system. The

advantages gained by integrating bipolar devices have diminished. Integrating the entire ten-million-gates system on a single silicon die revives the previously ignored issues of power consumption and substrate coupling. For instance, in order to limit excessively large electric fields across junctions and other adverse effects, supply voltage has to be scaled accordingly when feature size shrinks. Since the built-in junction voltages of bipolar transistors do not scale [3,4], the performance of BiCMOS technology suffers substantial degradation as the supply voltage decreases. As high device packing density, reduced power consumption and fabrication cost are vital for large-scale systems, monolithic CMOS process remains the choice of implementation technology for most mixed-signal designs and virtually all SoCs.

2.4 - Substrate Coupling Mechanisms

In mixed-signal SoC designs, monolithic CMOS process remains the choice of implementation technology for its superior device packing density and reduced fabrication cost. CMOS logic gates inject current into the substrate as they charge and discharge their loads. A drawback of this strategy is that the injected digital switching noise can be easily coupled to the analog circuits through parasitic resistance and capacitance of the substrate. Noise coupling through the substrate can be analyzed in 3 steps: injection, propagation and reception. These processes will be briefly introduced in the following subsections. Strategies to minimize substrate noise injection are discussed in details in Section 2.5 as well as Chapter 4. They include developing efficient guarding schemes by using accurate substrate models, separate clean supply for substrate biasing and active noise suppression circuits.

2.4.1 - Substrate Noise Injection

Various types of devices, both passive and active, are grown on the silicon substrate. IC devices inject spurious currents to various points of the substrate. These can be pn-junctions of MOS, bipolar transistors and ohmic contacts of resistors, capacitors and substrate bias contacts. Generally, substrate noise is injected to the substrate through ohmic or capacitive coupling, depending on whether the region possess majority or

minority carrier diffusions. The intensity of the coupling depends on the frequency spectrum of the noise, as well as the substrate profile.

2.4.2 - Substrate Noise Propagation

The propagation of substrate noise depends on the substrate doping profile, parasitic inductance of the substrate backplane bias bond wire, and the noise frequency spectrum. From the distributed Ohm's Law,

$$J = (\sigma + j\omega\epsilon)E$$

where J , σ , ω , ϵ , and E are the current density, conductivity, signal frequency, permittivity and electrical field of the conductor respectively; the substrate current is contributed principally by its conductive and capacitive components, in which the conductive component dominates the process. For the epi process at typical silicon doping levels, the values σ and ϵ of the heavily-doped bulk layer are on the order of 100S/m and 0.1 nFm^{-1} respectively. For frequency of 1GHz, the product $\omega\epsilon = 2 \times 10^{-11}$, which is about 0.6% of the magnitude of the conductance. The capacitive component rises to about 6% at frequency of 10GHz. The parasitic capacitance can practically be neglected in the noise propagation process, and the substrate can be modeled as purely resistive.

In the bulk process, the substrate consists of a single uniformly-doped layer (See Figure 2.1(i)). The doping levels varies from low to high. High-resistivity substrate provides better device isolation against substrate noise. However, it is more susceptible to MOS *latch-up* problems. At high frequency, noise current conducts near the surface. On the other hand, low-resistivity substrate suppresses CMOS latch-up but facilitates substrate coupling. Noise current flows through the bulk and low inductance backplane contact is needed to achieve good device isolation against substrate noise.

The *epi* process attempts to combine the advantages of high- and low-resistivity bulk substrates (See Figure 2.1(ii)). In the epi process, the substrate consists of two uniformly-doped layers of different resistivity stacked together. A thin and resistive ($\rho = 10\Omega\text{cm}$) epitaxial layer on the substrate surface, and a highly conductive ($\rho = 0.001\Omega\text{cm}$) heavily-doped bulk layer lies underneath. The thin epitaxial layer at the surface increases the

lateral substrate resistance for better isolation, while the bulk layer maintains low conductive paths for latch-up prevention. For longer-range coupling, the heavily-doped bulk layer underneath dominates even at high frequencies, as the epitaxial layer is much thinner than the skin depths of most signals under 100GHz.

2.4.3 - Substrate Noise Reception

Due to the high σ of the heavily-doped bulk layer, the coupled substrate noise can reach die locations far away from the aggressors. Substrate coupling is thus a global effect for heavily-doped bulk substrate. Surface components such as resistors, capacitors, first layer interconnects and bipolar transistors can couple substrate noise through ohmic contacts and across capacitive junctions. Additionally, substrate noise can directly affect the operation of MOS transistors through the body contacts. Propagation delays of digital gates, gains or quiescent currents of analog transistors can have transient fluctuations due to substrate voltage variations.

2.5 - Substrate Coupling Detection and Suppression

As substrate coupling will quickly become the limiting factor [34] in large-scale mixed-signal systems, several strategies have emerged to help controlling substrate noise interference. Special fabrication and packaging processes such as *Silicon-on-Insulator* (SOI), diffusion trenches and *Multi-Chip Module* (MCM) attempt to contain substrate noise interference from dispersal by fully or partially disconnecting local portions of the substrate from others. Nonetheless, SOI and MCM processes increase the manufacturing cost significantly. To be consistent with the primary goal of mixed-signal integration for improved performance and reduced cost, the most desirable substrate noise reduction scheme should rely on physical layout separation strategies and passive barriers as much as possible.

To protect the noise-sensitive components against substrate-coupled interference in ordinary monolithic CMOS processes, designers apply some forms of noise protection.

Placing noise shielding structures, such as guard rings, around sensitive components is largely preferred for its simplicity and low cost. Efficiency of guard ring structures strongly depends on the local substrate current contours [13], the specific substrate profile, layout geometry and the impedance of the interconnect, bonding wires and pins used to ground the guard ring. The conventional strategy to account for the effect of all these factors is by *ad hoc* allocation of overly designed guard rings. In the midst of area-efficient designs and rapidly changing IC design environment, this is no longer acceptable.

For high performance systems, an accurate model representing the substrate parasitics is needed, so that the residue substrate noise penetrated through the guard rings can be quantitatively determined by extracted circuit simulations. Substrate coupling effects are then simulated using conventional circuit simulators simply by including parasitic devices that give rise to substrate coupling to the netlist during extraction. These are the parasitic capacitors at the drain, source and well junctions, and a resistive mesh for the substrate bulk. However, due to the size of the substrate, special tradeoff evaluations between accuracy and complexity must be made, such that the netlist is sufficiently accurate, yet does not incur resources that exceed what the simulator can handle. In practice, design tools and verification methodologies for SoCs must compromise the effectiveness of substrate noise shielding among other important design constraints. Our substrate parasitics extraction scheme is explained in detail in Chapter 3.

2.6 - Generalized Crosstalk Predictions

The common use of heavily-doped bulk process in SoCs and higher interconnect aspect ratios with process shrinks also contribute to the problem. To keep pace with the emergence of large-scale SoC architecture, which on average constitutes over 5 million transistors, a more efficient tool that envisions verification and testing for crosstalk due to substrate coupling and fabrication process variation is necessary.

The conventional notion of *crosstalk* is the coupling between interconnects, while *substrate coupling* is the coupling between substrate nodes, or between interconnects and substrate nodes. Other than their different physical origins, crosstalk and substrate

coupling are indistinguishable at the circuit level. Hence their analysis methods are practically identical. Techniques used for crosstalk fault diagnosis can easily be extended to cover substrate coupling faults by including the proper substrate models.

2.7 - Substrate Discretization

Spatial discretization procedure is the most important part of the substrate modeling scheme, because it directly affects the model complexity and thus the simulation process. However, due to the large amount of possible connections it needs to consider, it is also the major overhead of the entire substrate parasitics extraction scheme.

2.7.1 - Rectangular Grid Substrate Discretization

In the rectangular grid substrate model, the points discretizing the substrate are derived by intersecting the sets of rectilinear grid lines, as illustrated in Figure 2.2. The grid points should be positioned at the critical locations on the substrate. However, critical features of circuit layouts are typically very localized. When an increased precision is sought for, auxiliary grid lines are added. There is a trade-off between the grid uniformity and complexity of the generated network. Some local refinements can be added [13], but they inevitably increase the algorithmic complexity in rectangular grid-based discretization models. Nevertheless, even with this strategy, there is still a limited control over the exact individual grid point locations.

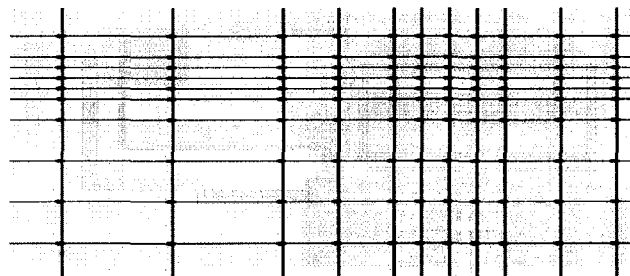


Figure 2.2: Rectangular grid with local refinements

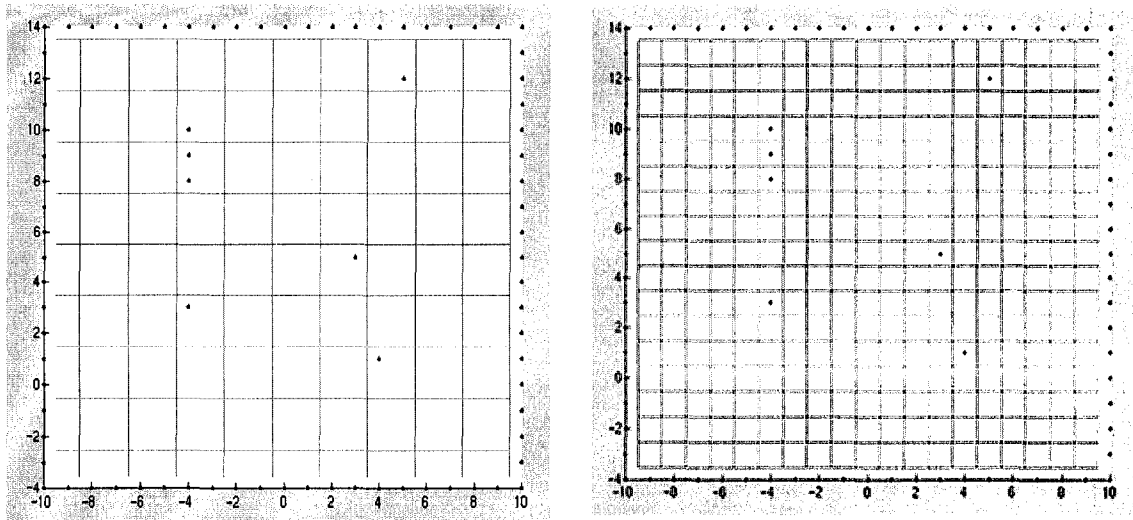


Figure 2.3: A large number of meshes are needed to achieve adequate refinement with rectangular mesh discretization scheme

Because of high non-linearity, small deviations in grid point locations can have a large impact on the accuracy of the subsequent model. In particular, at p-n junctions and semiconductor interfaces, carrier concentrations can vary over twenty orders of magnitude within a few tenths of a micron [12]. Such variations cannot be well-modeled by low-order approximations of interpolating nodes that are relatively far apart. Therefore, conventional substrate mesh generated by uniform grid partitions leads to inherently inefficient simulations. For most designs, an almost uniform grid size is usually required. Thus, a large number of grid points are generated to achieve adequate refinement (Figure 2.3). As a result, much computation effort is wasted to solve equations for regions of little importance. Hence, with the rectangular mesh structure, the simulation time and memory requirements pose a major bottleneck when extracting a large substrate accurately.

2.7.2 - Triangular Substrate Discretization

Naturally, the optimal discretization scheme should place the grid point locations at points where accuracy is the most crucial, while avoiding unnecessary points. The discretization should be driven by *critical locations* identified from the layout geometry. These critical

locations are points on the substrate that require the most accurate substrate potential computations, and they are usually where the circuit nodes are connected.

An algorithm based on *Voronoi tessellation* [15] partitions a substrate tile around each substrate port derived from the circuit layout. The computed graph is called a *Voronoi diagram*. By assigning the ports to locations of interest, the substrate is discretized with adaptive fineness. Computational effort can be concentrated on locations with high feature density, while broader slices are formed in regions of low complexity. Note that two critical locations can be arbitrarily close to each other. Also, unlike rectangular-grid algorithms, auxiliary substrate modeling points (Voronoi sites) at arbitrary locations can be added for further refinement without increasing the complexity of the algorithm. Consequently, the extracted model will provide more accurate information compared to the rectangular-grid models with the same number of substrate ports. Furthermore, in highly non-linear regions, the precision of low order interpolation approximations can be improved by inserting additional Voronoi sites or moving the sites closer to each other, without affect other regions of the model. A comprehensive substrate extraction algorithm that generates the dual of a Voronoi diagram (the *Delaunay diagram*) will be introduced in Chapter 3.

Chapter 3 - Substrate Modeling

The integration of analog and digital circuits reduces propagation delays, area and power consumption at the expense of increased coupling of digital switching noise to the analog circuits through parasitics of the common substrate. The objective of a substrate extraction algorithm is to yield a model describing the substrate parasitics, such that an accurate spatial and temporal solution of substrate potentials and coupling effects can be obtained through circuit simulations. Next generation design tools and methodologies must regard accurate rendering of substrate coupling effects as a critical criterion. The inefficiencies in the resulting model can impose unrealistic resource requirements for extraction and simulation.

Relative to circuit simulation optimization, the study of substrate parasitics extraction is relatively new. Traditionally, the substrate is treated as a single electrical node on the simulation netlist. Substrate coupling simulations were ignored except in very high frequencies applications, such as in radio-frequency (RF) designs. To reflect the effects of local and global substrate noise, we need to distinguish the potential differences among local regions of the substrate. Rather than solving for a continuous 3-dimensional potential function for the substrate, we approximate the solution with discrete potentials, using the finite difference approach. This discretization step is necessary to transform the problem of solving for the continuous current densities into a circuit analysis problem. This step renders it possible to apply efficient numerical algorithms.

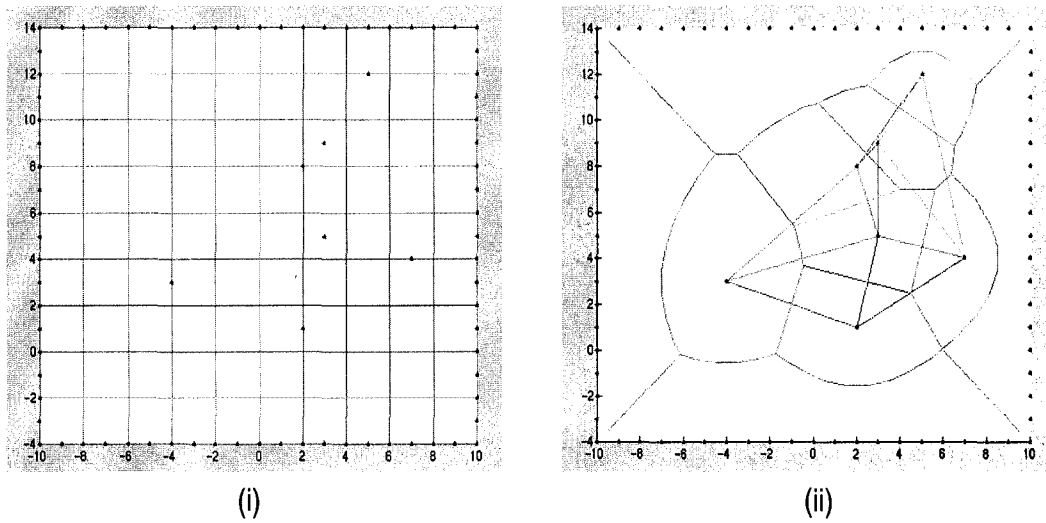


Figure 3.1: Substrate Discretization using (i) Rectangular grid method, and (ii) Triangular grid method.

To model the substrate with discrete potentials, first we have to decide how it should be discretized spatially. In this simplification process, the substrate is partitioned into numerous tiles each will then carries a discrete potential at any specific time point. Any two points lying within each tile are assumed to be equipotential. The tiles can be of uniform or irregular shapes. The conventional rectangular-grid and the triangular-grid discretization methods are illustrated in Figure 3.1. Details for these two methods has been covered previously in Section 2.7. Each has its own advantages over the other. However, almost all existing substrate modeling tools are based upon the rectangular-grid method. Several minor variations of the schemes exist among the tools. Our approach to using the alternative Delaunay triangulation algorithm is discussed in Section 3.2. In the following section, we shall first introduce an important computational geometry algorithm for *Delaunay Triangulation*, which will be used in our modeling algorithm.

3.1 - Delaunay Triangulation and Voronoi Diagram

The *Voronoi diagram* is a versatile and well-known geometric structure. For instance, it is widely used in computer graphics applications to generate a simplified geometric surface

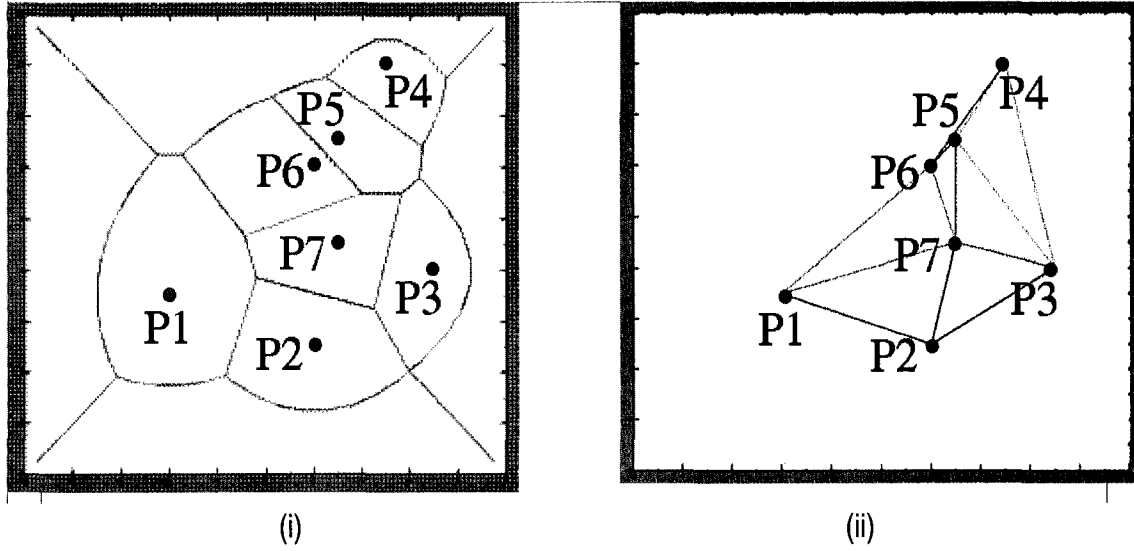


Figure 3.2: (i) Voronoi Tessellation, and (ii) Delaunay Triangulation for a set of points denoting the critical locations.

from an irregular and complex relief. In terms of computational geometry, given a finite set of *critical points* $P=\{p_1, \dots, p_n\}$ on a plane, the plane is partitioned into sites $S=\{s_1, \dots, s_n\}$ such that every point $q \in s_i$ is closer to point p_i than to p_j , where $j \neq i$. This site assignment is called the *Voronoi assignment model* [15]. The resultant partition is called the *Voronoi tessellation diagram* or simply *Voronoi diagram*. Detailed construction of a Voronoi diagram is widely available in computational geometry literatures, such as [15] and [16]. The most commonly used algorithm is known as the *Fortune's algorithm*, which computes the Voronoi diagram in $O(n \log n)$ time [15].

Each Voronoi diagram has a dual structure called *Delaunay triangulation diagram*, which is a set of line segments joining pairs of *closest* neighboring points P . A Voronoi diagram is shown in Figure 3.2(i), and its dual Delaunay diagram is shown in Figure 3.2(ii). Because of the one-to-one correspondence between the Voronoi and Delaunay diagrams, a Voronoi diagram can either be computed directly or indirectly from Delaunay triangulation. Since the structure and complexity of a Voronoi diagram is determined by the set of critical points, site locations and densities are adjustable.

In the context of substrate modeling, points in the region occupied by each polygonal tile (*Voronoi tile*) in the Voronoi diagram has the same voltage. The Delaunay diagram represents the netlist of the substrate parasitics, treating each Voronoi tile as a distinct electrical node. As the mesh refinement flexibility is critical to maintain a compact substrate model, the Voronoi and Delaunay diagrams are particularly efficient in discretizing the substrate.

3.2 - Delaunay algorithm for Epitaxial Substrate

Based on the experimental results and observations from literature [9,10,13,14], our model simplifies the Voronoi algorithm established in [14], in which Voronoi *nodeplanes* are stacked vertically to generate a 3-dimensional model for uniformly-doped substrate. Our algorithm employs a single Voronoi nodeplane to model the epitaxial layer, and a single node to represent the low-resistivity bulk layer (Figure 3.3) [1]. Hence its complexity is equivalent to that of a 2-dimensional Voronoi model.

In practice, the substrate model is expressed as a netlist of parasitics to represent a graph of interconnected Voronoi sites. This graph is called the *Delaunay diagram* in computational geometry, and it is the dual of the corresponding Voronoi diagram. The components of the netlist are thus obtained directly using the dual algorithm, *Delaunay triangulation* [15]. Figure 3.4 shows a section of the Delaunay triangulation applied to a

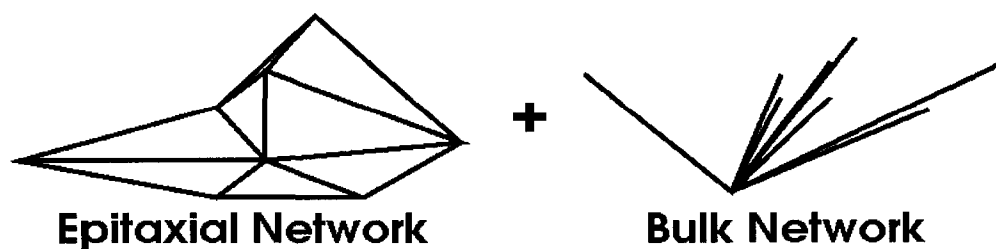


Figure 3.3: The epitaxial network and bulk network

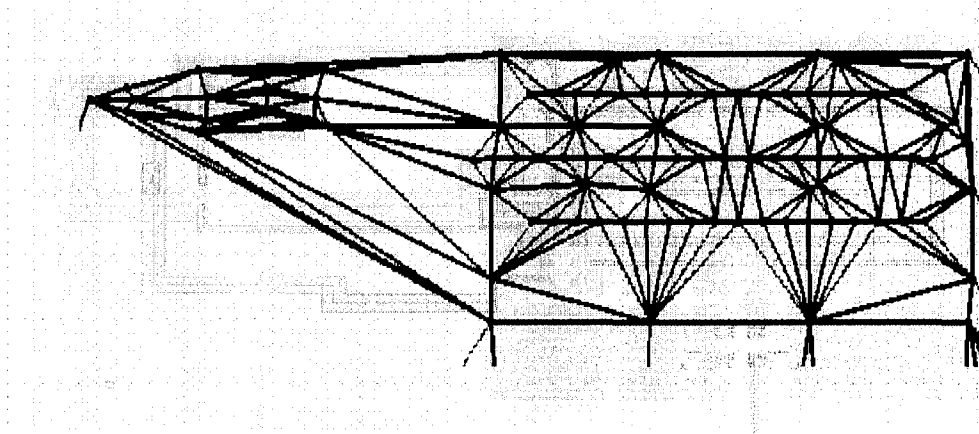


Figure 3.4: Triangular grid conforms with layout geometry

circuit layout. Each vertex in the graph represents a Voronoi site, interconnected by minimum length edges. From this graph, substrate parasitic components can be computed based on the geometric distances of the line segments. We present in this thesis further network reduction schemes to simplify the network before it is released for simulations.

3.3 - A Substrate Parasitics Extraction Algorithm

The goal of substrate modeling is to produce parasitic resistances and capacitances representing the coupling mechanisms. By attaching the substrate model to the circuit, the substrate coupling effects can be obtained by circuit simulations. A p^- -epi/ p^+ -bulk substrate is modeled by an RC network, tracing the current conduction paths through the epitaxial, n-well and the bulk layers.

A schematic of the proposed model configuration is shown in Figure 3.5. Referring to this figure, the laterally oriented capacitors $\{C_{well}\}$ model the pn -junctions at the substrate and well interface. Resistors running laterally $\{R_{epi_n}, R_{epi_p}\}$ in the figure stand for the purely resistive nodeplane models for the substrate and n-well. The low-resistivity bulk is connected to the epitaxial and n-well nodeplane via the vertically placed components $\{R_{psub}, R_{nwell}, C_{well}\}$. The bulk layer is electrically represented by a single node. The

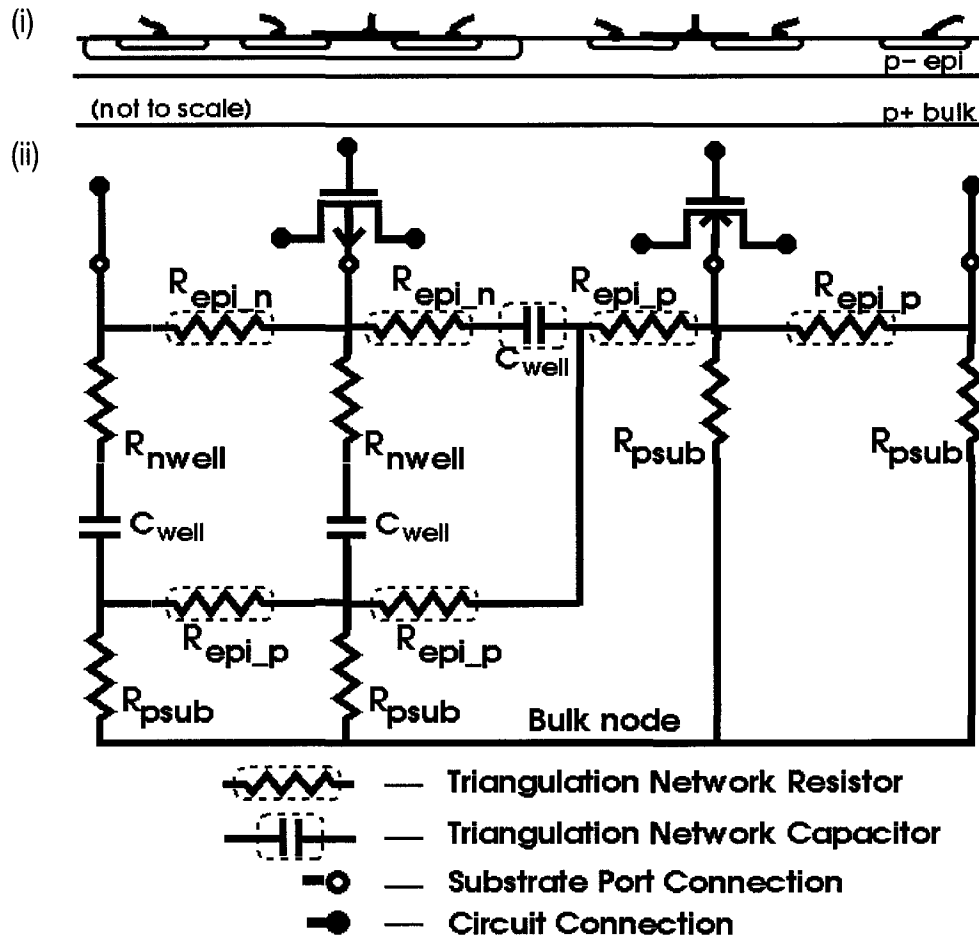


Figure 3.5: Substrate model general configuration (i) Substrate diffusion geometry, and (ii) Substrate circuit model

actual topology of the nodeplane and component values are determined by physical parameters and the layout data. We now describe in detail each of the steps involved.

3.3.1 - Overview

The substrate model generation procedure consists of the extraction step, followed by several netlist reduction steps. The following pseudocode in Figure 3.6 summarizes our

substrate parasitic extraction routine, `GEOMEXT()`, that generates the substrate netlist from a given layout geometry:

```

1  GEOMEXT(layout)
2  begin
3      identify_data_within_selection_window()
4      extract_and_import_substrate_ports()

5      collect_psub_substrate_ports()
6      collect_nwell_edge_points()
7      extract_critical_points()
8      generate_psub_bulk_connections()
9      generate_psub_epi_connections()
10     simplify_psub_epi_connections()
11     eval_RC()
12     save_netlist()

13     foreach nwell(i),
14         collect_nwell_substrate_ports()
15         collect_nwell_edge_points()
16         extract_critical_points()
17         generate_nwell_bulk_connections()
18         generate_nwell_epi_connections()
19         simplify_nwell_epi_connections()
20         eval_RC()
21         save_netlist()
22     end

23     combine_substrate_netlist()
24     simplify_substrate_netlist()
25     export_substrate_netlist()
26 end

```

Figure 3.6: GEOMEXT pseudocode to generate critical points for substrate ports and n-wells. Only top-level functions are shown. GEOMEXT algorithm is implemented in Matlab®.

In line 3, GEOMEXT first gathers the layout information within a user-defined selection window. It then extracts the substrate ports in line 4, from which the critical points for computation are determined. Second, the Delaunay triangulation algorithm is employed to generate a graph which optimally connects pairs of critical points. One triangulation algorithm is applied to the *p*-substrate (line 5-12), followed by the repeated extractions for

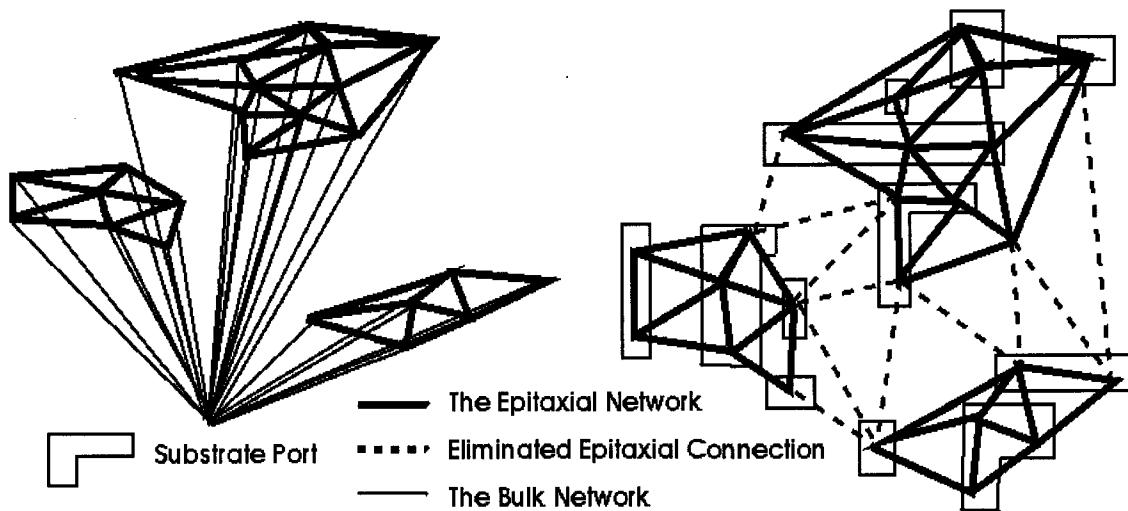


Figure 3.7: Clusters of epitaxial network connected to bulk node

each n -well (line 13-22). All triangulation graphs are then combined to form the skeleton of the epitaxial layer model (line 23). Each edge of the triangulation graphs represents a parasitic element between the corresponding substrate ports. Additional connections are created to model the p^+ bulk layer. Parasitic resistors and capacitors are then affixed to the substrate ports connection. Finally, based on their separation distances, the netlist is iteratively simplified (Figure 3.7) and exported in line 25-26.

3.3.2 - Substrate Ports

To determine the appropriate connections and the values of the substrate parasitic components, the layout geometry data must be collected. A layer drawings recognition routine first gathers information from the layout, assigns a global circuit netlist to individual circuit nodes, and then generates data layers carrying the geometric and netlist information of interest. In CMOS processes, geometric data for five types of structures (*layers*) are sufficient to determine the substrate model. These are the locations of the nMOS, pMOS, n -well, ohmic and capacitive connections of the p -substrate and n -well

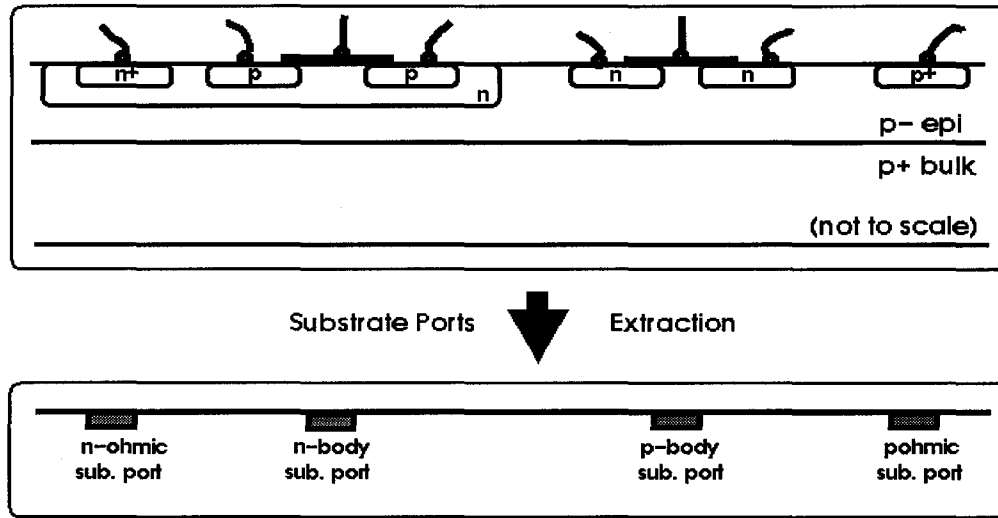


Figure 3.8: Types of substrate ports extracted from layout

(Figure 3.8). These layers represent the interface between the circuit and substrate networks, and are collectively known as the *substrate ports connection layer* P . Each of the n substrate ports forming the substrate is given by its r vertices,

$$\{a_{(i,1)}, a_{(i,2)}, \dots, a_{(i,r)}\} = P, \quad i = 1, \dots, n$$

where substrate port $P_i \in P$ is a *simple polygon* with r vertices. A simple polygon is a two-dimensional region enclosed by a closed polygonal chain that does not intersect itself [15]. Examples of simple polygons are illustrated in Figure 3.9.

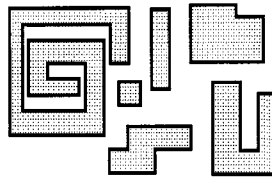


Figure 3.9: Substrate ports as simple polygons

3.3.3 - Critical Points Assignment

Critical points V specify the location of the substrate network nodes. As they directly affect the network complexity, they should be assigned to substrate port locations only when the substrate details are required. Generally, all n -wells and substrate ports are identified by simple polygon shapes P_i . For modeling reasons, substrate ports and n -wells have to be treated separately. Efficient algorithms can be obtained by processing a set of representative points, instead of polygons. Their two-dimensional shapes P_i will be converted to auxiliary sets of points V_i for computation convenience. A mapping M is applied to substrate port shapes

$$P_i \xrightarrow{M} \{V_{i1}, v_{i2}, \dots, v_{ik}\} \text{ , for each } i.$$

The mapping is chosen such that the set of critical points $V=\{V_i\}$ that is used to represent each substrate port i , is able to convey the position, size and shape of P_i . A logical choice for M is the centroid, i.e. the averaging position of P_i . To make the V_i further sensitive to the size and shape variation of P_i , each polygon is first sliced into sufficiently small rectangles, p_{ij} , where

$$\{p_{i1}, p_{i2}, \dots, p_{ik}\} = P_i \text{ ,}$$

where the centroids of them are taken as the critical points, thus

$$v_{ij} = \text{centroid}(p_{ij})$$

and

$$\{v_{i1}, v_{i2}, \dots, v_{ik}\} = V_i \text{ .}$$

Contrary to this, the critical points $V_{wi}=\{v_{wi1}, v_{wi2}, \dots, v_{wih}\}$ for the i^{th} n -well are generated along its edges, because this is where there are large potential differences across the

reverse-biased junction capacitance. All critical points belonging to the p -substrate and each n -well are then grouped together,

$$V = \{V_{psub}, V_{nwell_1}, V_{nwell_2}, \dots, V_{nwell_n}\}$$

where V_{psub} contains all vertices V_i obtained from P_i in the p -substrate, and V_{nwell_j} contains V_{wj} , and all V_i such that P_i is in the j^{th} n -well. Additional user-defined critical points $\tilde{V}_{psub}$ and $\tilde{V}_{nwell_j}$ can also be inserted into the p -substrate and n -well database, respectively, to further refine the netlist. The above critical points generation are performed by functions:

```

4      extract_and_import_substrate_ports()
5      collect_psub_substrate_ports()
6      collect_nwell_edge_points()
7      extract_critical_points()

14     collect_nwell_substrate_ports()
15     collect_nwell_edge_points()
16     extract_critical_points()
```

in the GEOMEXT() algorithm from Figure 3.6. Figure 3.10 illustrates the corresponding critical point locations on a generic CMOS process layout.

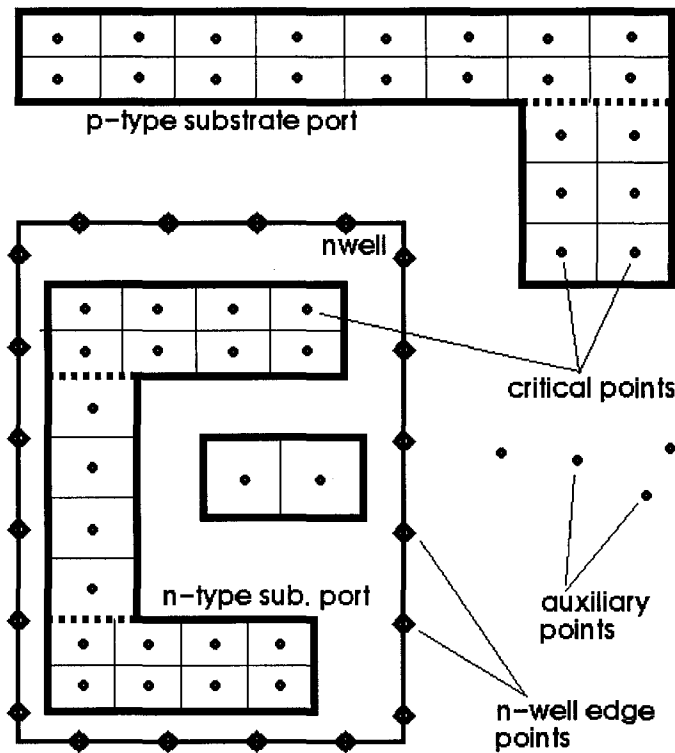


Figure 3.10: Critical points derived from substrate ports and n-wells

3.3.4 - Extracting the Substrate Network

The rectangular-grid extraction and the current density function approach usually require parasitic resistance to be attached three-dimensionally between every pair of substrate ports [11]. The large number of connections lead to large networks and dense matrices, making extraction and simulation tasks impractical for even small circuits. Analog simulation engines, such as SPICE, are designed to solve sparse matrices and therefore are not efficient in solving dense matrices [11]. Therefore, the reductions in the model size must accompany SoC design verifications.

The commonly used SoC process has a substrate profile of a lightly-doped epitaxial layer over a heavily-doped bulk substrate. The epitaxial layer is relatively thin and resistive ($\sim 10\Omega\text{cm}$), while the bulk layer has a low resistivity of $0.05\Omega\text{cm}$. The set of all substrate port connections is called the *substrate network edges* E . It consists of two parts: the

epitaxial network edges E_{epi} and the bulk network edges E_{bulk} , $E = \{E_{epi}, E_{bulk}\}$, where all sets of edges are obtained by the extraction process.

3.3.4.1 The Epitaxial Network

Due to the low resistivity of the bulk layer, and the thickness of epitaxial layer, the epitaxial current flow can be considered to be planar. The epitaxial layer can then be modeled by a planar resistor network E_{epi} . Delaunay triangulation algorithm is a particularly suitable algorithm for modeling this layer. It produces the optimum triangulation, connecting only the substrate port pairs that are closest to each others (Figure 3.11). Moreover, the generated planar lateral resistor mesh is particularly valid, based on the fact that the p^- epitaxial layer has negligible subsurface lateral conduction, and tends to attenuate long-range substrate conduction. The planar epi network in terms of the set of connections E_{epi} also implies sparse nodal matrices, which is advantageous for most simulation engines. E_{epi} consists of p -substrate and n -well epitaxial ports connections,

$$E_{epi} = \{E_{psub}, E_{nwell_1}, \dots, E_{nwell_2}\}$$

such that

$$E_{psub} = \text{delaunay}(V_{psub}, \{V_{w1}, \dots, V_{wj}\})$$

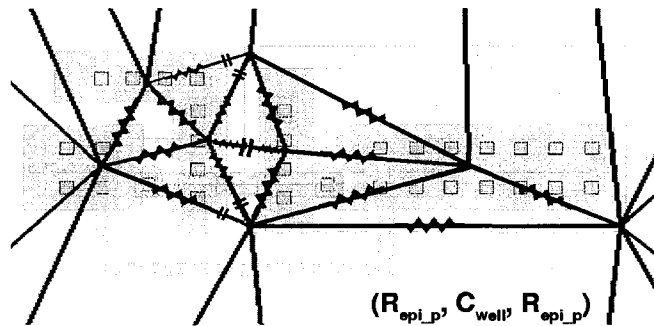


Figure 3.11: Triangulation grid p^- epitaxial layer substrate model (E_{epi})

and

$$E_{nwell_i} = \text{delaunay}(V_{nwell_i}), i = 1, \dots, j$$

where j is the total number of isolated n-wells. The generated E_{epi} will be reduced subsequently, when the parasitic values for the connections are evaluated.

3.3.4.2 The Bulk Network

Because of its low resistivity, the bulk layer can be represented electrically by a single node. The bulk network E_{bulk} consists of connections between the bulk node and every P_i of the nodeplane, as well as the backplane contact, if it exists. A general connection scheme for the bulk layer is illustrated in Figure 3.12.

3.3.5 - Inserting Substrate Parasitic Components

Parasitic components and their values are assigned to the connections as follows. After the substrate network E is formed, parasitic values $W(E)$ along each connection $E_i \in E$ are computed. Table 1 illustrates the types of parasitic components to be attached according to the type of the critical points pair. With W being a function of critical points separation distances, the resistive and capacitive parasitic components across points p_1 and p_2 are

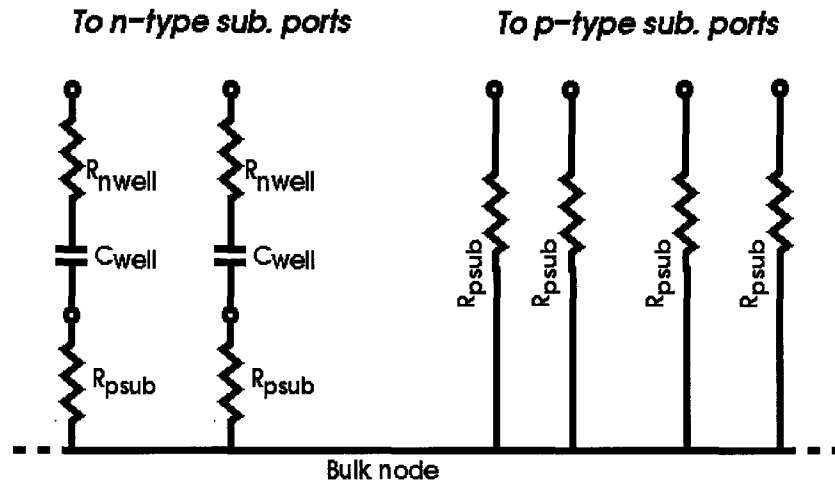


Figure 3.12: The bulk network (cross-section view)

evaluated as follows:

$$R_{p_1 p_2} = \rho \cdot \frac{\|p_1, p_2\|}{A(p_1, p_2)}, \text{ and}$$

$$C_{p_1 p_2} = \varepsilon \cdot \frac{A'(p_1, p_2)}{\|p_1, p_2\|},$$

where ρ and ε are the substrate resistivity and permittivity respectively, and $A()$, and $A'()$ are the effective cross-sectional area functions.

The components are then associated with the connected ports, forming the preliminary netlist. Figure 3.11 and 3.12 illustrate the parasitic devices added to the epitaxial network E_{epi} and bulk network E_{bulk} respectively.

The substrate model can be described as a weighted graph (network) G with critical points V' as vertices, the set of simplified substrate ports connections E as edges, and the substrate parasitic device parameters W as weights, $G(P)=(V',E,W)$, where $W(P_{V_{Ei1}}, P_{V_{Ei2}})$ is the resistive and/or capacitive impedance along edge $E_i \in E$ between two connected critical points. For accuracy reasons, the separation distance between the

Table 1: Types of parasitic components for various types of critical points

	nwell edge	psub port	nwell port	bulk node
nwell edge	NC	RC	R	NC
psub port	RC	R	NC	R
nwell port	R	NC	R	RC
bulk node	NC	R	RC	0

Legend:

NC -- No Connection

0 -- Direct Connection (short circuit)

R -- Resistive Connection

RC -- serial Resistive and Capacitive Connection

two corresponding polygons $P_{V_{Ei1}}, P_{V_{Ei2}}$ is evaluated, instead of that between the critical points V_{Ei1}, V_{Ei2} .

With the substrate parasitic model added to the circuit netlist, the effect of substrate coupling can be obtained through simulations. Critical points are now the nodes in the combined circuit. Hence, their voltages and the inter-node currents can be obtained from the simulation results. Values of other substrate locations can also be obtained by applying interpolation functions to the neighborhood of the critical points.

3.3.6 - Network Reduction

The formatted partial netlist (E, W) describing the substrate can be simplified. This is performed by function `simplify_substrate_netlist()` from Figure 3.6:

```
24    simplify_substrate_netlist()
```

It is described in following Figure 3.13:

```
1  simplify_substrate_netlist(raw_netlist)
2      while(change)
3          eliminate()
4          recombine()
5          integrity_check()
6      end while
7  end
```

Figure 3.13: Simplifying the substrate model

The redundant or insignificant connections in the network can be discarded before being combined with the circuit netlist. Two steps are employed to reduce the vertices V and edges E of the graph G . We also apply the criteria for verifying integrity of the netlist. These operations are described in details in the following subsections.

3.3.6.1 Reducing E : *Eliminate()*

This procedure eliminates selected edges E_i from the graph G . All connections across pairs of critical points which belong to the same node in the netlist can be removed, as

these nodes are at the same potential. Furthermore, taking the fact that the p^- epitaxial layer suppresses long-range conduction, an epitaxial resistive connection is eliminated (disconnected) if its resistances and/or the separation distance exceeds a certain threshold. If the neighboring components become open circuit as a result, they are also removed.

From experimental results and device simulations, the majority of substrate current flows in the *epi*-layer only when the lateral conduction path has conductance considerably smaller than the conduction path through the bulk layer. This occurs when the separation distance between the substrate ports is less than 4 times the *epi*-layer thickness apart [12]. Otherwise, most current conducts through the bulk layer. The threshold value is usually specified as a ratio of the thickness of the epitaxial layer, and can be refined to adjust the accuracy-complexity trade-offs of the obtained model. Distinct threshold values can also be assigned to different areas or types of connections.

3.3.6.2 *Reducing V: Recombine()*

This procedure removes nodes from graph G . Removable nodes include auxiliary nodes and n -well edge points. When an auxiliary node is found to have only two resistive connections, R_1 and R_2 , the resistors connected in series are combined $R = R_1 + R_2$ and the intermediate node is eliminated. Care has to be taken such that no substrate ports are deleted in this process. Since it is possible that the combined resistance R exceeds the threshold for elimination, more edges can be removed. These two steps are applied iteratively until the network remains unchanged.

The reduction techniques simplifies significantly the substrate network, especially when the layout has localized regions of dense substrate ports separated by substrate regions with few features. The resultant substrate consists of localized clusters of lateral resistor meshes, all interconnected together by the bulk node, as depicted previously in Figure 3.7.

3.4 - Test Setup and Simulation Results

An efficient substrate extraction algorithm based on Delaunay triangulation, GEOMEXT, has been proposed. Recall from the previous chapter that this algorithm discretizes the

substrate with adaptive fineness. Since its computational complexity does not depend on the physical values of the substrate parasitics, our primary focus of formulating GEOMEXT is on the substrate parasitics network structure. Resistivity and capacitance values are kept empirical and refitted with experimental measurements subsequently to accomodate various fabrication conditions and process variations.

Despite our temporary exclusion from the discussion, the specific values of the substrate parasitics will become important in evaluating the model's accuracy. These impedance parameters are necessary to verify the convergence between substrate coupling simulations using GEOMEXT and the experimental results. To complete the model, physical parameters measured on the fabricated chips must be used. This is because the nominal substrate parasitic values given by the fabrication technology providers are not accurate enough for our purposes, since substrate coupling attenuation is a strong function of substrate resistivity.

It is a consensus that accurate representations of substrate coupling effects are crucial for successful mixed-signal designs. Design tools such as Cadence Assura Substrate Coupling Analysis (SCA)¹ for modeling substrate effects in RF circuit simulations, are often assumed to be accurate, but are rarely experimentally verified. In investigating the improved performance of our substrate modeling tool, we decide to compare GEOMEXT with the SCA tool. Instead of assuming that SCA substrate models are completely accurate, we devise a series of experiments to confirm the accuracy of the Cadence Assura SCA tool. Four sets of experiments are performed to generate experimental data for the empirical GEOMEXT substrate model and modeling parameters retrieval. The measurement data obtained in this experiment is re-used later to verify the effects and simulation results of the Active Noise Suppression (ANS) circuit to be introduced in the next chapter.

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1. Additional layout extraction rules needed. The modified extraction rule deck and necessary procedures to setup the Cadence SCA tool has recently been contributed by the writer to Canadian Microelectronics Corporation (CMC) for public distributions.

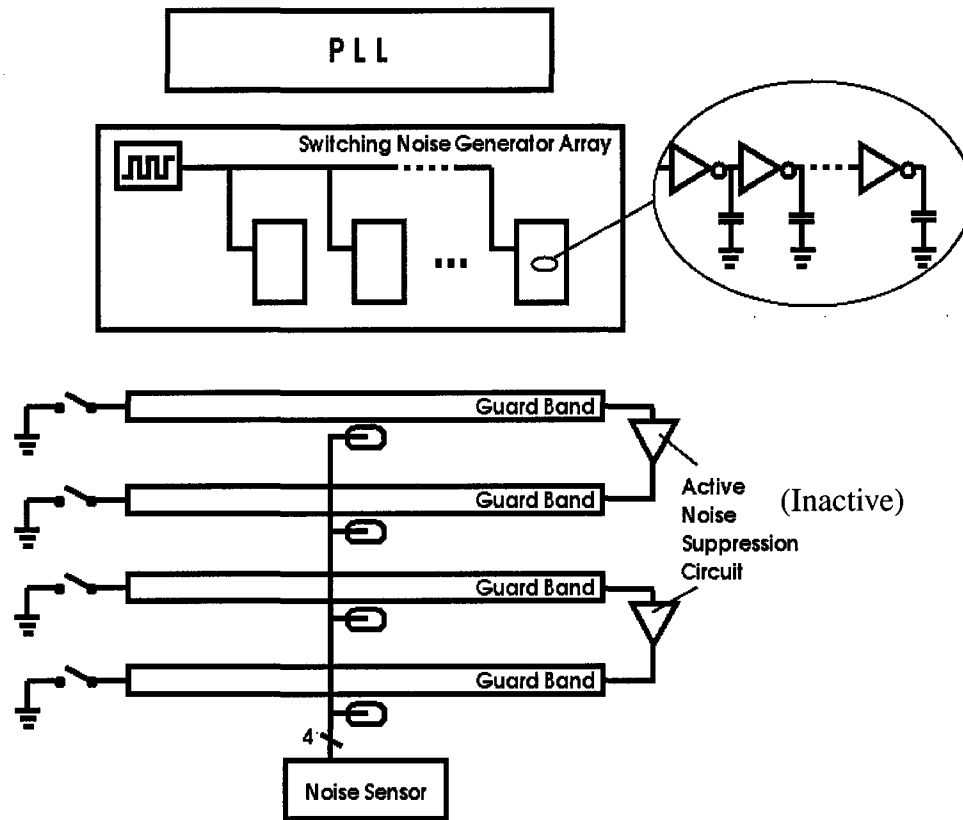
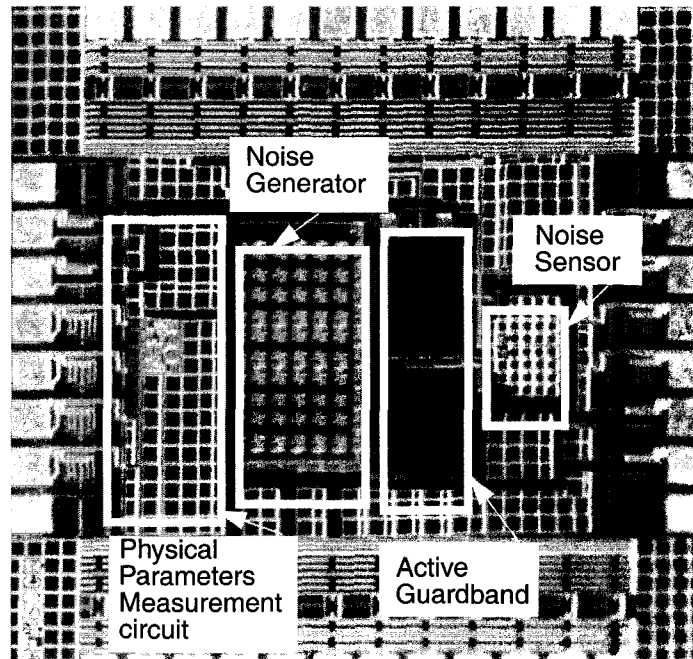


Figure 3.15: Active noise suppression and guard band insulation experimental setup

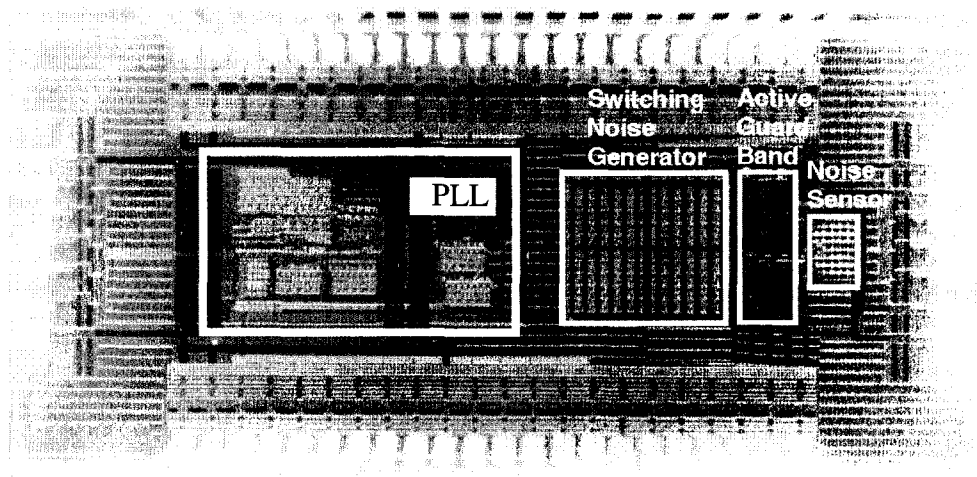
3.4.1 - Substrate-Coupled Switching Noise Experiment

The major goal of this experiment is to obtain vital measurements for a newly developed substrate modeling algorithm. The experimental setup is shared with another substrate noise suppression experiment to be described in the next chapter. The active suppression circuits connected to the guard bands are disabled in this experiment. The microphotographs of the circuits for this experiment are shown in Figure 3.14. The system consists of a programmable inverter-based substrate noise generator, 4 guardbands connected to the substrate, and 2 ANS circuits connected to the programmable guardbands that are able to partially neutralize the incident substrate noise. There is also a circuit that facilitates physical substrate parameters retrieval in the design shown in Figure 3.14(a). In Figure 3.14(b), the effect of substrate coupling near a PLL is evaluated. Figure 3.15 illustrates the schematic of this experiment. The printed circuit board (PCB) manufactured

for the design shown in Figure 3.14(b) to facilitate accesses to the packaging is depicted in Figure 3.16.



(a)



(b)

Figure 3.14: Substrate coupling experiments microphotographs. (a) Substrate coupling measurement circuits and physical parameter measurement circuit. (b) Substrate coupling and PLL jitter measurements.

The measurements obtained from this experiment are crucial to fine tune the technology parameters and verify the results predicted by the newly developed GEOMEXT substrate modeling algorithm. The results enable us to evaluate and improve the accuracies of GEOMEXT, as well as the Cadence Assura SCA tool for addressing the substrate coupling effects. Four programmable guardbands are placed next to an extensive array of switching noise generators at constant distances. Each of them can either be grounded to bias the substrate or keep floating to provide access for substrate potential measurements. Additionally, the 4 individually configurable guardbands can be used to compare several popular guardband biasing configurations for shielding substrate noise. The noise generator is programmable to produce a varying degree of noise intensity.

Four sample circuit layouts of different sizes, circuits A, B, C, D, are used to test the GEOMEXT and SCA algorithms. The GEOMEXT algorithm is triangle-based, while SCA is rectangular-based. Their extraction performances are summarized later in Table 2. Generally, GEOMEXT is capable to generate a smaller model with less number of distinct nodes. It also takes less time to execute, especially when the circuit area becomes large. This is due to the differences in executing the code in different platforms. The SCA is

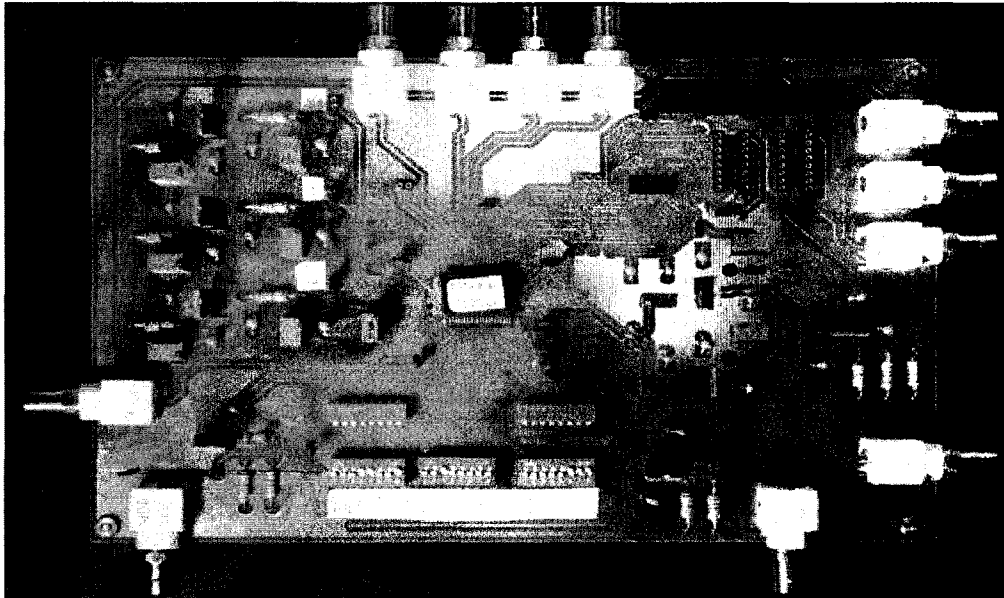


Figure 3.16: PCB for substrate coupling experiments

executed using several LISP-like SKILL scripts in the Cadence Command Interpreter Window, while GEOMEXT is implemented in Matlab software. The use of an optimal $O(n \log n)$ Fortune's algorithm in generating the Delaunay connections in Matlab also contributes to the performance differences. Due to the simplifications in GEOMEXT to ignore long-range epitaxial substrate conductions, the number of non-zero elements in the resultant Z-matrix from GEOMEXT is much smaller than that generated by the SCA algorithm.

3.4.2 - Transient Substrate Noise Simulations and Measurements

Since transient substrate noise measurement requires a low noise measurement circuit, and temporal and voltage resolutions in the pico-second and milli-volt ranges respectively, conventional noise measurement techniques are inadequate. On-chip low noise measurement circuits are not viable because when fabrication in available monolithic technologies, they are as vulnerable to the same substrate coupling effects as the circuits to be measured. Consequently, we attempted to design and fabricate an inverter-based, multi-phase cross-coupled amplifier to facilitate the measurements. However, due to limited resources, the fabricated circuit did not achieve the required precision to ensure the qualities of the measurement results using this method. Nonetheless, we gained a great deal of knowledge and experience in the development of these prototype circuits which will promise subsequent innovations in future test circuit designs. Meanwhile, we verify the accuracies of GEOMEXT against simulation results obtained using the substrate models generated by the SCA algorithm.

From comparisons between the GEOMEXT and SCA simulations, valuable insights for designing an efficient substrate modeling algorithm are gained. First, the impact of different extraction algorithms on simulation time is illustrated in Table 2. In this

comparision, the SpectreS circuit simulator is used. The results indicate that our extractions are performed in one fifth of the time required for the SCA extraction on average, while the resulting simulations are performed in roughly half of the time.

The accuracies of the substrate coupling simulations using GEOMEXT and SCA models are then compared. The transient simulations of short- and long-range substrate coupling are compared. As shown in Figure 3.17, the short range substrate simulations agree to each other within approximations, despite the smaller number of nodes in GEOMEXT models. However, some discrepancies exist between the simulations using GEOMEXT and SCA models, when long-range substrate measurements are considered (Figure 3.18). Nevertheless, both simulations exhibit similar trends in the DC voltage fluctuations. Assuming that the SCA models are accurate, these observations indicate that GEOMEXT has an accurate model for short-range substrate conductions, but it has over-simplified the substrate parasitics connecting distant substrate nodes. The absence of long-range substrate parasitic conduction paths should not be a surprise, since in the formulation of GEOMEXT, we have neglected the long-range epitaxial conduction paths, which are dominated by the conduction paths through the bulk in the *epi* process.

Table 2: Impact of extraction algorithms on simulation time

Algorithm	SCA	GEOMEXT	SCA	GEOMEXT	SCA	GEOMEXT	SCA	GEOMEXT
Circuit	A	A	B	B	C	C	D	D
# of nets	10	10	68	68	102	102	1589	1589
Extraction Time	34.92s	15.03s	12538s	87.60s	21389s	116.58s	>100000s	12357s
Z matrix density ²	32.96%	25.56%	96.73%	22.34%	88.04%	11.02%	-	0.15%

² The substrate impedance matrix density is the percentage of the number of non-zero elements among the total number of elements in the matrix.

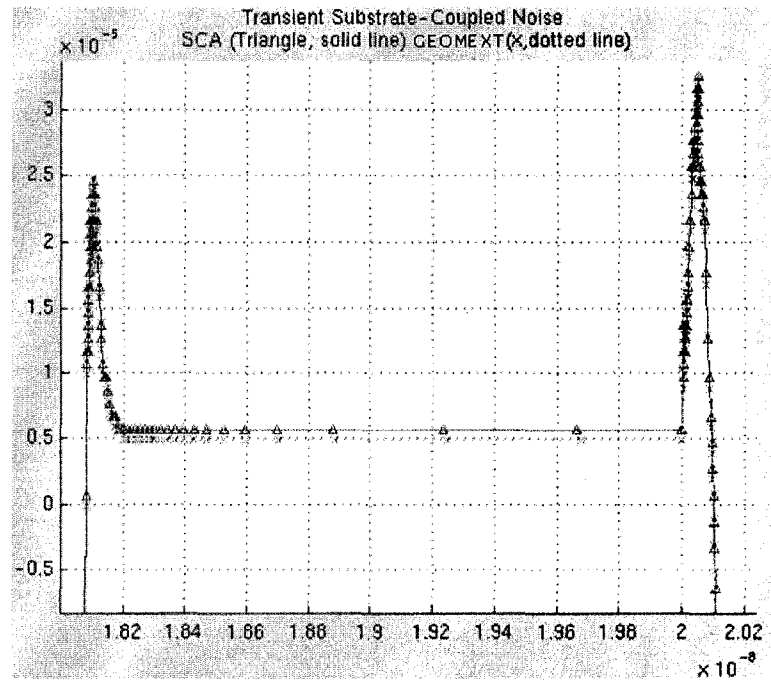


Figure 3.17: Short-range substrate transient potentials comparisons

3.4.3 - Substrate Parameters Measurement Experiment

This experiment is meant to retrieve physical substrate parameters for the developed substrate modeling algorithm GEOMEXT. The experimental setup consists of two 4 by 4 arrays of ohmic contacts to the *p*-substrate and *n*-well. The contacts distribution is illustrated in Figure 3.19. The contacts are uniform $1\mu\text{m}$ by $1\mu\text{m}$ squares. Each array of substrate contacts is organized into 4 rows and placed at different distances from neighboring contacts of the same row. Substrate parasitic resistance and capacitance measurements can be made between any two contacts within the same row. A multiplexer circuit selects one particular row of contacts to be active at any given time (see Table 3). There is also a calibration setting (not shown in the figure and table) that short-circuits two measurement bonding pads, thus the parasitics of the packaging, bonding wires, bonding pads and pass gates can be measured and subtracted from the substrate parasitics measurements.

A *wheatstone bridge* setup with a reference resistor was originally planned to give more accurate measurement results than direct measurements. However, due to power supply connection errors occurred in some parts of the PLL design, this experiment was not conducted.

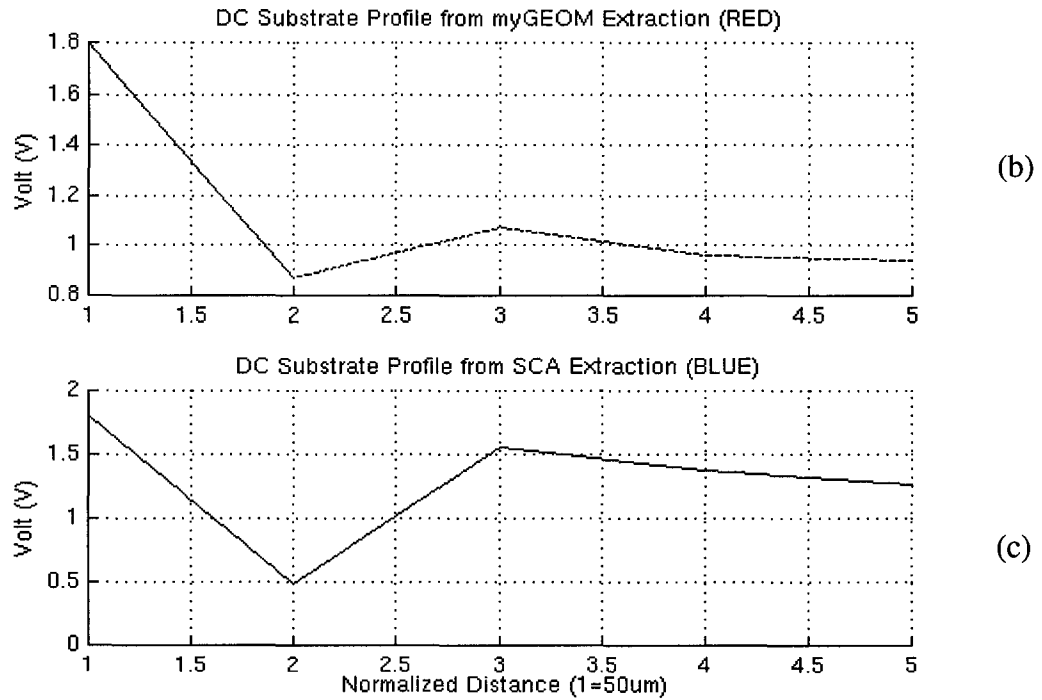
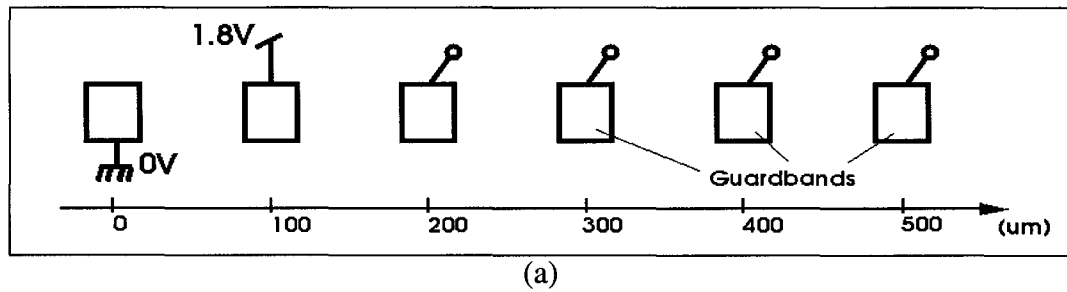


Figure 3.18: Short-range substrate transient potentials comparisons. (a) Guardbands at location 0um is biased to 0V (not shown), and at 100um is biased to 1.8V. DC voltages of 4 guardbands at locations 200, 300, 400 and 500um are measured. (b) Long-range substrate DC potentials using GEOMEXT model. (c) Long-range substrate DC potentials using SCA model.

3.4.4 - Phase Locked Loop Jitter Measurement

The objective of this experiment is to evaluate the performance of a PLL under the influence of substrate-coupled switching noise. Among other measurements, the extent of the PLL output clock jitter increases due to substrate noise interference is particularly interesting. This is because it demonstrates how substrate coupling, a physical-level effect, can transverse the abstraction hierachy and affect system-level performance.

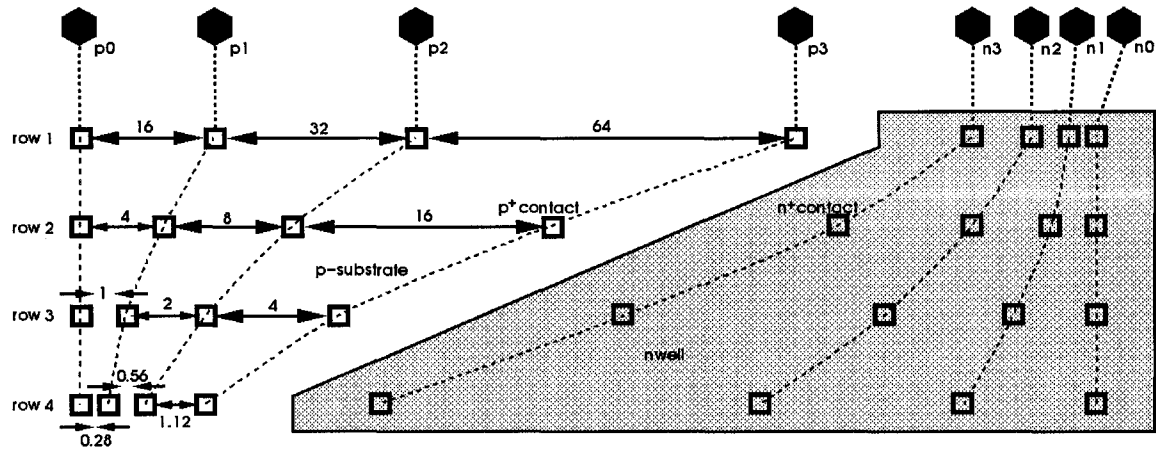


Figure 3.19: Substrate coupling parameters measurement circuit (Distances are in μm)

Table 3: Configurations for the substrate parameter measurement circuit

Control Inputs			Row Enabled
$\overline{\text{psub}}/\text{nwell}$	probe_sel1	probe_sel0	p[0..3]
0	1	1	<i>p</i> -substrate row 1
0	1	0	<i>p</i> -substrate row 2
0	0	1	<i>p</i> -substrate row 3
0	0	0	<i>p</i> -substrate row 4
1	1	1	<i>n</i> -well row 1
1	1	0	<i>n</i> -well row 2
1	0	1	<i>n</i> -well row 3
1	0	0	<i>n</i> -well row 4

The fabricated chip microphotograph is shown in Figure 3.20. Figure 3.21 shows one half of the layout block diagram. The actual layout comprises of two identical copies of the setups depicted, except one possesses an exposed voltage-controlled oscillator (VCO) circuit, while the other VCO is protected by guard rings. Referring to Figure 3.21, two

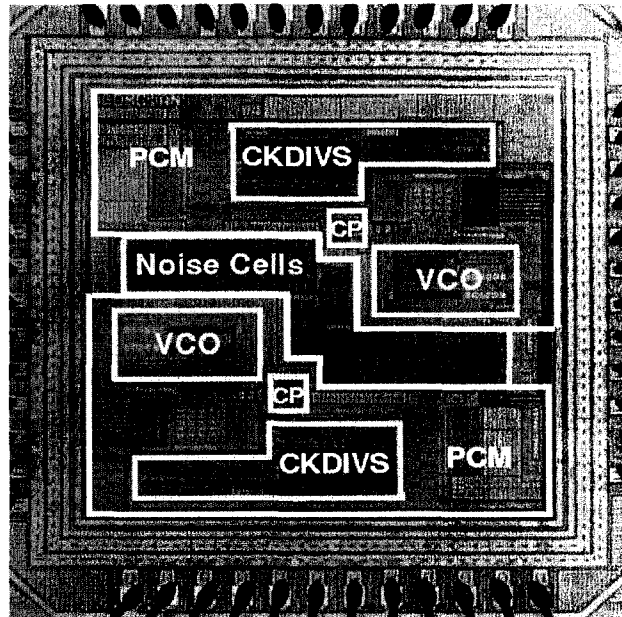


Figure 3.20: Microphotograph for PLL Jitter Measurement Experiment

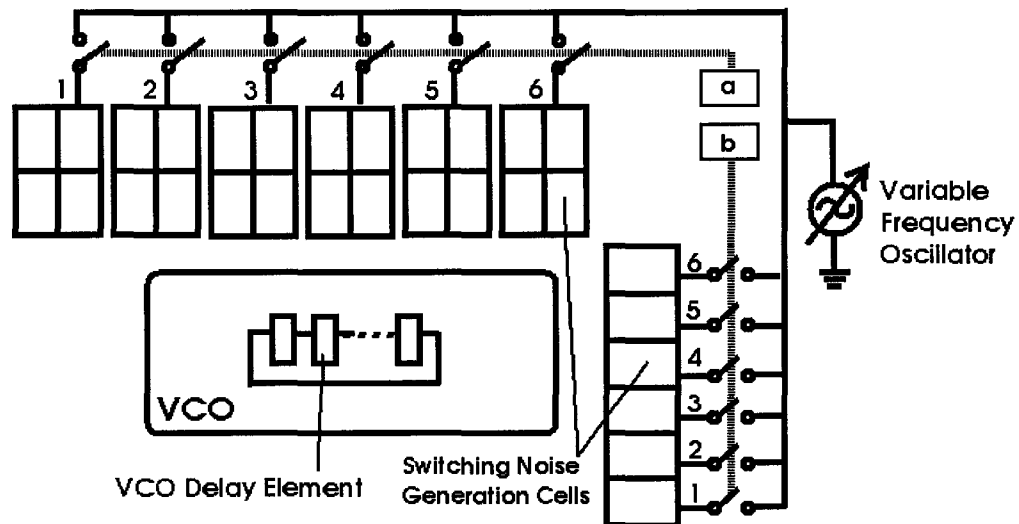


Figure 3.21: Experimental Setup for Phase Locked Loop Jitter Measurement. Controllers a and b specify the noise generations cells to be enabled.

groups of switching noise generation cells (noise cells) are placed orthogonally lining two sides of the Voltage-Controlled Oscillator (VCO) of the PLL. The noise cells can be independently set to source noise at different switching frequencies. This experimental setup is designed to resemble the typical environment for a monolithic PLL commonly found in SoCs. These PLLs share the same substrate with the rest of the circuits on the chip.

The PLL is operating besides a large group of CMOS digital logic gates, which are switching at a multiple of the PLL output clock frequency. The digital switching noise will be coupled to various parts of the PLL through the substrate, causing jitter at its output. The measured jitter under various coupling directions and switching rates are given in the following subsections.

3.4.4.1 PLL Jitter Against Locations of Coupling Sources

In this experiment, the locations of the substrate noise sources are varied. depicted the measured results of the root mean square (RMS) PLL jitter.

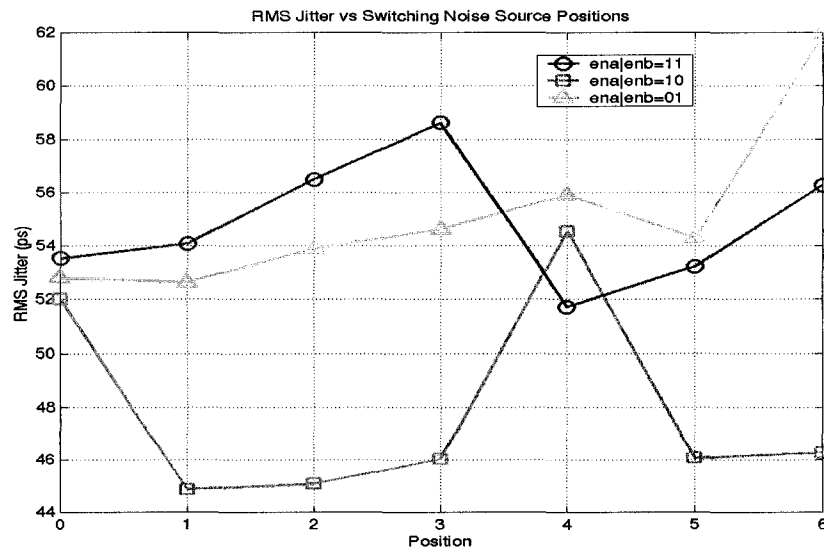


Figure 3.22: RMS PLL jitter measurement results. ena=1 or enb=1 enables the noise cells at the corresponding positions under controller a or b respectively.

3.4.4.2 PLL Jitter Against Switching Frequency

In this experiment, the PLL jitter is observed while varying the switching frequencies of the substrate noise sources. shows the measured results.

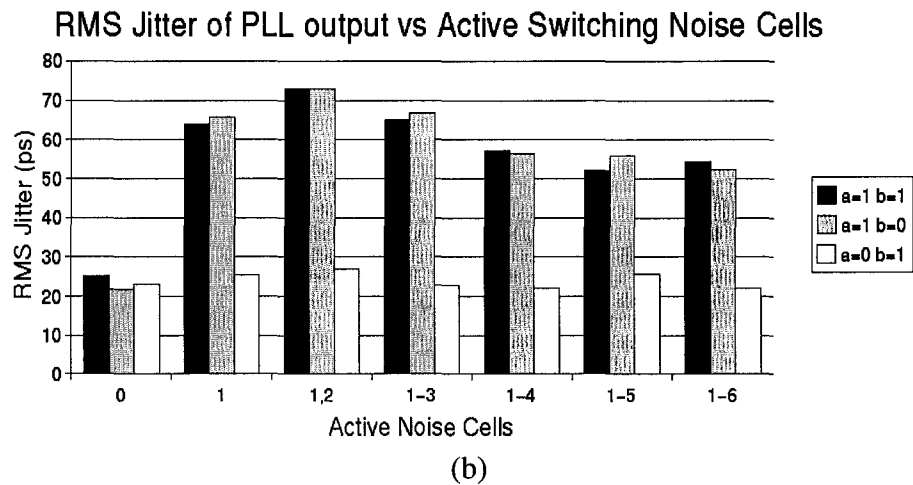
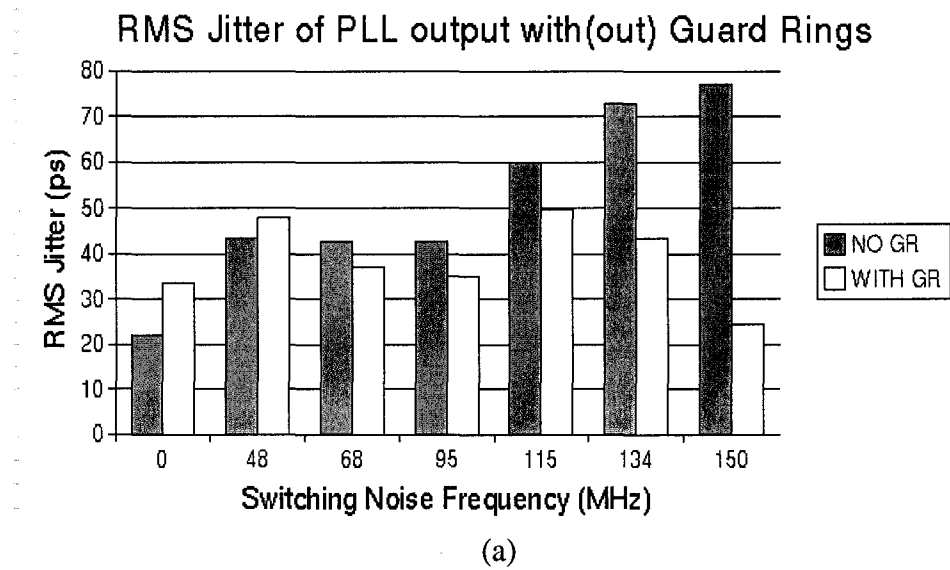


Figure 3.23: RMS PLL jitter measurements (a) The effect of guard rings on PLL jitter at different operating frequencies. (b) The effect of noise sources on PLL jitter from different directions. a=1 or b=1 enables the noise cells at the corresponding positions under controller a or b respectively.

Chapter 4 - Active Noise Reduction Methodologies

Traditional substrate noise reduction schemes rely on a combination of passive substrate noise barriers such as guard rings and a set of physical separation rules. Apart from using passive barriers, there are alternative ways to reduce noise, such as noise compensation strategies using *active* elements. The concept of noise cancellation using active elements presents a promising option for substrate noise reduction. Generally, in the active noise cancellation process, the transient substrate noise is sensed and then coupled to an inversion element. A phase-inverted copy of the noise is then capacitively coupled back to the substrate through another ohmic connection, and hence annihilates the substrate-coupled noise. This is illustrated in Figure 4.1. If the complementary signal is applied through a guard band, the result is an active guard band that responds actively to reduce the incoming noise. The key to successful active noise suppression lies in the design of the noise cancellation circuitry.

The frequency spectrum of switching noise is technology-dependent [35] and centres at the 1-10 GHz range, hence it is critical for the bandwidth of the noise suppression circuits to achieve this range to perform effectively. We propose two novel active suppression circuits in standard CMOS process with bandwidths achieving the GHz range. The suppression circuits are robust and compact, and can thus be applied extensively

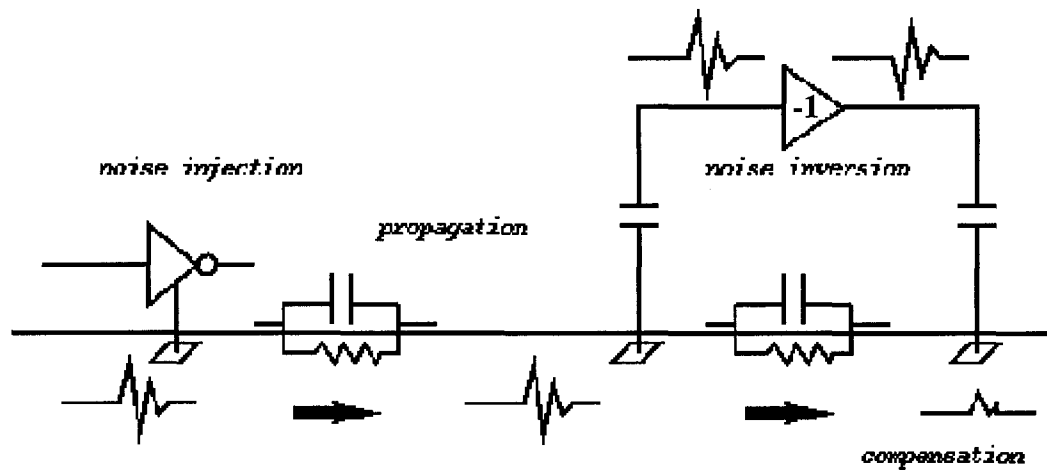


Figure 4.1: Active noise compensation circuit reduces noise by a phase-reversal unity-gain amplifier.

throughout the die to reduce substrate noise in monolithic SoC designs [2]. Noise reduction of over 80% is observed from simulation results. There are 2 different types of active noise reduction schemes. The first type is called *load balancing*, and the second type is called *active suppression*. Load balancing is discussed in Section 4.1. In Section 4.2, the basis of active noise suppression is discussed. Two novel active suppression guard bands are described in Section 4.3 and 4.4. In Section 4.5, our noise suppression circuits are simulated and tested.

4.1 - Load Balancing

The concept of load balancing is to create an image circuit with respect to the noisy circuit in order to minimize the overall switching noise. Authors in [20] investigated the use of dummy devices which produce counter-phase switching with respect to the aggressors, such that when the aggressors and dummy devices are switched simultaneously, the switching noise generated is canceled out. However, it has been concluded that the demands for proper synchronization are hard to achieve. The highly variable disturbance paths and rich high-frequency content involved could easily result in timing mismatch between the noise and the compensation waveforms, leading to increase in the overall RMS noise level. As typical switching noise pulses are in the GHz range, skews of a few

hundred pico-seconds can result in the increase of noise [20]. It is the practical difficulties in estimating the precise skew, which depends on numerous electrical characteristics of the aggressors, that deemed this technique unattractive.

4.2 - Active Noise Suppression

The shielding ability of guard rings can be improved by active suppression methods that create a compensation signal canceling the intercepting noise. Although the technique is appealing, its practical viability is hindered by bandwidth limitations and device non-idealities [20]. Since substrate coupled switching noise consists of short duration pulses concentrated in the 0.8-3GHz frequency range, GHz solutions must be used for any active suppression methodologies to be effective. Several articles [7,20,21,22] reported implementations of active circuits for substrate noise reduction for different purposes using CMOS, bipolar amplifiers and commercial OpAmps. However, all methods cannot attain bandwidth required to process switching-induced substrate noise. Liu et al. [21] and Fukuda [22] used OpAmps to suppress sub-100MHz substrate noise. *SiGe* bipolar technology is used in [7] to boost the bandwidth to the order of 100MHz. Unfortunately, the HBT amplifier cannot be integrated into CMOS SoC designs.

In this chapter, we introduce two high-bandwidth active suppression circuits that are robust and compact. They are suitable for applications of substrate noise reduction schemes in monolithic SoC designs. Several authors proposed to implement the inversion element by custom-designed and off-the-shelf analog operational amplifiers (OpAmps). The effective suppression range using commercial OpAmps are usually limited to a few tens of MHz. In [7], a high bandwidth *SiGe* HBT amplifier was designed to improve the bandwidth to 400MHz. The major drawback of the design in [7] is the costly heterojunction bipolar technologies, precluding its use for monolithic SoC applications. All of the circuits suffer from the aforementioned skew problems due to the lack of bandwidths, and thus inadequate for eliminating switching noise interference.

There are two common topologies for active noise reduction methods, based on feedback [21] and feed-forward [7,20,22] systems. Block diagrams for both types are depicted in

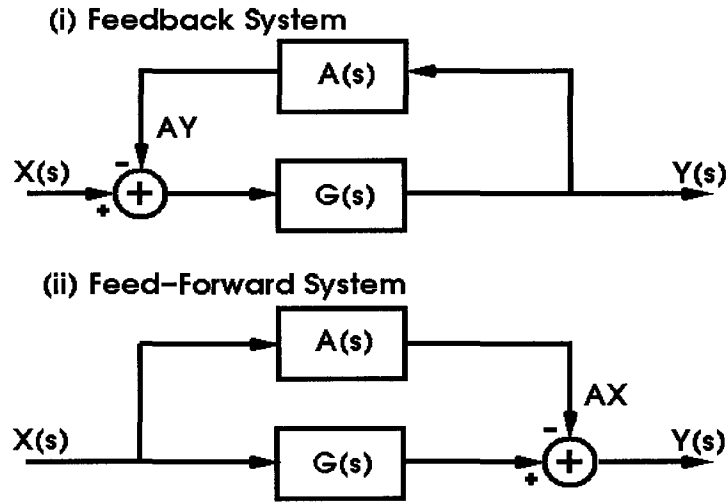


Figure 4.2: (i) Negative Feedback and (ii) Negative Feed-Forward systems

Figure 4.2. In both diagrams, $G(s)$ denotes the substrate coupling transfer function and $A(s)$ is the frequency response of the active suppression circuit. $X(s)$ is the injected substrate noise, and $Y(s)$ is the coupled substrate noise after applying active suppression. We use $H(s)=Y(s)/X(s)$ to represent the overall system transfer function. Note that substrate coupling is an attenuation process, therefore $|G(s)| < 1$ for all s .

In feedback systems, Figure 4.2(i), the output coupling noise is inverted and amplified by the active suppression circuit through the feedback loop. The resultant signal AY is then used to compensate the incoming substrate noise. The principle of negative feedback active suppression method derives from traditional feedback loop theory, which often involves a high gain element $G(s)$. In our case, however, $|G(s)|$ is less than unity for typical thin epi process, and thus a relatively high gain active suppression amplifier $A(s)$ is required to generate an effective compensation signal AY for the incoming noise X . Consequently, the bandwidth of $A(s)$ becomes inadequate to respond to high-frequency switching noise. The high gain A is also more sensitive to process variations, rendering it difficult to achieve the required precision consistently. Contrarily, with the feed-forward configuration, as in Figure 4.2(ii), a high gain active suppression circuit is not needed, because compensation takes place after the attenuation of X . Only a gain $|A(s)| < 1$ is required to produce the active suppression signal AX to compensate the attenuated

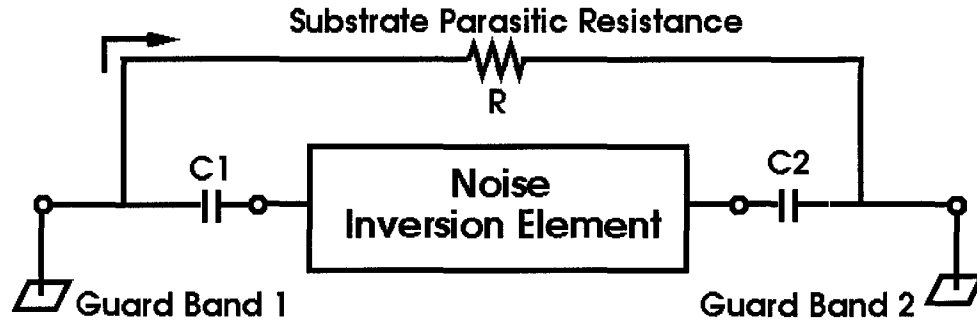


Figure 4.3: Active noise suppression circuit in feed-forward configuration

coupled noise GX . Feed-forward based active suppression systems thus permit the noise inversion element to maximize its bandwidth under existing gain-bandwidth constraints. Its response delay is also less than that of the feedback systems.

Based on the requirements for SoC substrate noise reduction applications, we developed two compact and high-bandwidth unity-gain active suppression circuits using the feed-forward configuration. They both share a common schematic illustrated in Figure 4.3, using different implementations of the noise inversion element. $C1$ and $C2$ are DC decoupling capacitors and R denotes the effective substrate parasitic resistance between guard bands 1 ($GB1$) and 2 ($GB2$). Substrate noise is capacitively coupled from $GB1$, and the compensation signal (noise) is capacitively coupled to $GB2$. $GB2$ should be placed close to the victim circuits it intends to protect, while the placement of $GB1$ can be strategically used to realize some particular R . The first circuit is a high-speed amplifier based on traditional modified translinear circuit principle [12]. Circuit simulations and experimental measurement show that its effect is satisfactory. The second circuit attains even better performance by using a CMOS digital inverter as the noise inversion element. Due to the improved bandwidth, it is responsive to high frequency noise spikes caused by CMOS gates transitions, the dominant noise source in SoCs.

4.3 - A Translinear Amplifier

The first proposed circuit is shown in Figure 4.4. It is a CMOS high-speed amplifier based on traditional modified translinear circuit principle, similar to the topology found in [7]. The circuit is aimed to compensate the noise partially, while maximizing the response bandwidth. Referring to Figure 4.4, V_{in} couples substrate noise from the outer guard band and returns a duplicated copy of the noise with inverted polarities at V_{out} , which is then coupled to the inner guard band to facilitate noise cancellations. Note that the compensation signal in [7] is applied to a uni-directional guard ring completely surrounding the victim circuit. A compensation signal is applied to all directions of the receptive circuit whenever a noise impulse is coming from any direction. Since switching noise is highly directional [7,20,23], an increase in the total noise level may result. Guard band is more appropriate for this application.

Assuming ideal supply and ground connections and matched current sources, the drain current of M_1 (input current I_1) and the drain current of M_2 (output current I_2) are complementary:

$$K_1\sqrt{I_1} + K_2\sqrt{I_2} = V_{DD} - 2V_T, \text{ with } K_i \equiv \sqrt{\frac{2}{k_i' \left(\frac{W}{L}\right)_i}}.$$

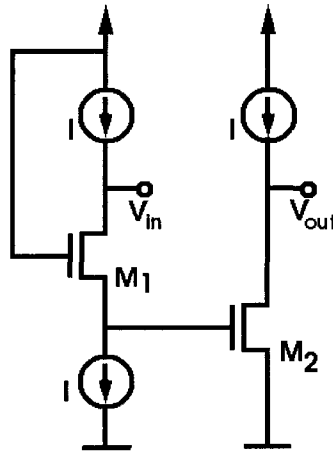


Figure 4.4: Phase-reversal amplifier using Translinear Circuit Principle

From this relation, it follows that the output current response, I_2 is inverted relative to the input current I_1 , while all other quantities are kept constant.

4.4 - CMOS Inverters Configuration

The second proposed circuit is shown in Figure 4.5(i). CMOS digital inverter is a bistable circuit. It has two stable states; in which the input port is HIGH and the output port LOW, and vice versa. There is also an unstable equilibrium (metastable) point V_m near $V_{DD}/2$. The CMOS digital inverter also exhibits its maximum slew rate at V_m of its voltage transfer characteristics trajectory Figure 4.5(ii). We utilize the transition region of the CMOS digital inverter to realize a high-bandwidth unity-gain inversion element. The circuit consists of 3 digital inverters, two small DC decoupling capacitors and a pair of guard bands. Neither precise bias currents nor stringent transistors size matching is required. On the other hand, its voltage gain is tunable to accommodate various substrate doping concentrations and geometric shapes of guard bands it attaches to. Because only small capacitors and near-minimum sized digital gates are used, the extra area consumed by an active suppression-enabled guard band is minimal. Figure 4.6 shows the gain of an inverter in various sizes biased at the maximum slew rate point. Both inverters $N1$ and $N3$

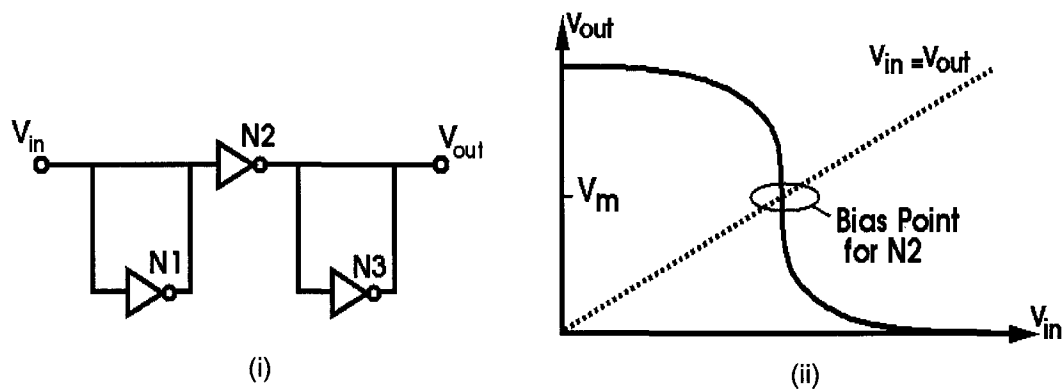


Figure 4.5: A digital inverter as phase-reversal element
(i) Schematics (ii) Bias Point of N2 on the inverter VTC

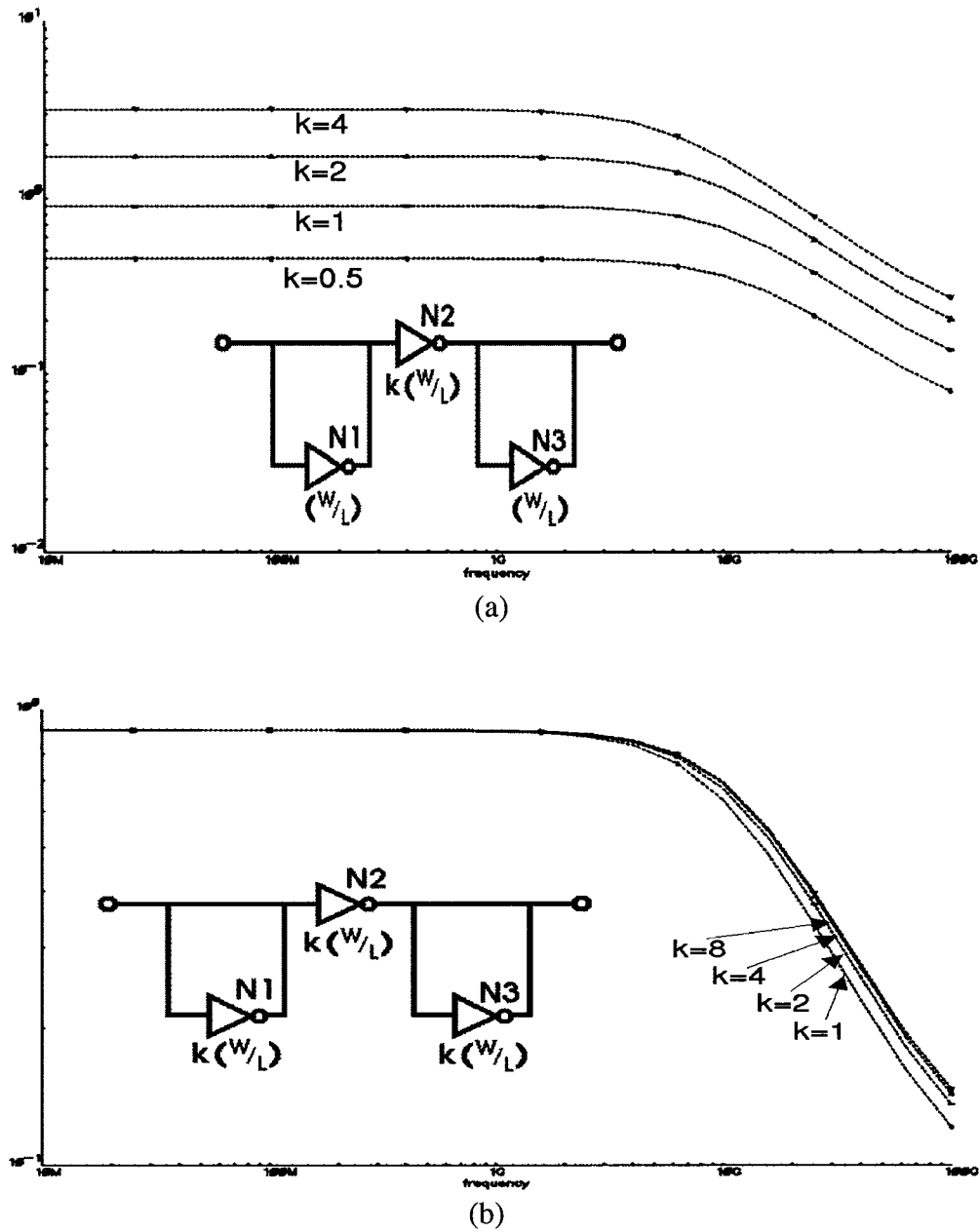


Figure 4.6: Frequency response of open-loop noise inverter: (a) depends on the size of $N2$ and $N1$ (or $N3$); (b) insensitive on their absolute sizes.

are self-coupled. Their input/output ports are forced to settle at their metastable states. It is critical to minimize the parasitic resistance and inductance between their input and output ports to preclude oscillations. Inverter $N2$ is responsible for phase-inversion. It is also biased at the metastable point by inverters $N1$ and $N3$ connected to its input and output

ports. However, unlike $N1$ and $N3$, the input and output ports of $N2$ are decoupled and thus independent, which eliminates feedback that otherwise hampers performance. Figure 4.6 also shows that the voltage gain A of the inverter depends on k , the size ratio of $N2$ and $N3$, but not on their absolute sizes. A is thus insensitive to process variations.

From Figure 4.2(ii), incorporating the minus sign at the adder into $A(s)$, the appropriate gain for

$$H(s) \equiv Y(s)/X(s) = A(s) + G(s) = 0 \text{ for all } s \text{ is } A(s) = -G(s) = |G(s)|e^{-j\pi}.$$

Ideally, the desired A equals the magnitude of signal attenuation function through substrate conduction between the two guard bands, with a π phase shift. In practice, A is chosen such that overall close-loop frequency response of the active suppression system is less than unity for all frequencies while maximizing the attenuation of the stop band. Figure 4.7 illustrates the closed loop transfer function $H(s)$ with various active suppression gains $A(s)$ with varying inverter size ratio k . The optimum gain is found at $k=3$. The $-3dB$ frequency is 1.65GHz. A too high gain A can cause prolonged oscillations

and therefore increase the noise level, while a low A does not provide adequate noise rejection. The whole procedure can easily be automated. With known substrate profile and guard band dimensions, $H(s)$ and A are pre-computed using substrate parasitic extractor, yielding the effective substrate parasitic resistance R between the guard bands. With a given R , an instance of active suppression circuit with optimized $N1$, $N2$ and $N3$ is added to a cell library. The appropriate active suppression circuit can then be selected by either the designers or tools, corresponding to the value of the substrate resistance R of the guard band pair used.

4.5 - Test Setup and Simulation Results

To evaluate the effectiveness of our active suppressions, the circuits are verified with simulations and experimental measurements. As transient substrate noise measurements are difficult to retrieve, we developed and incorporated an efficient substrate parasitics extraction algorithm into the Cadence design flow. The standard Cadence Assura layout extraction rules have been extended to identify substrate noise injection sources and

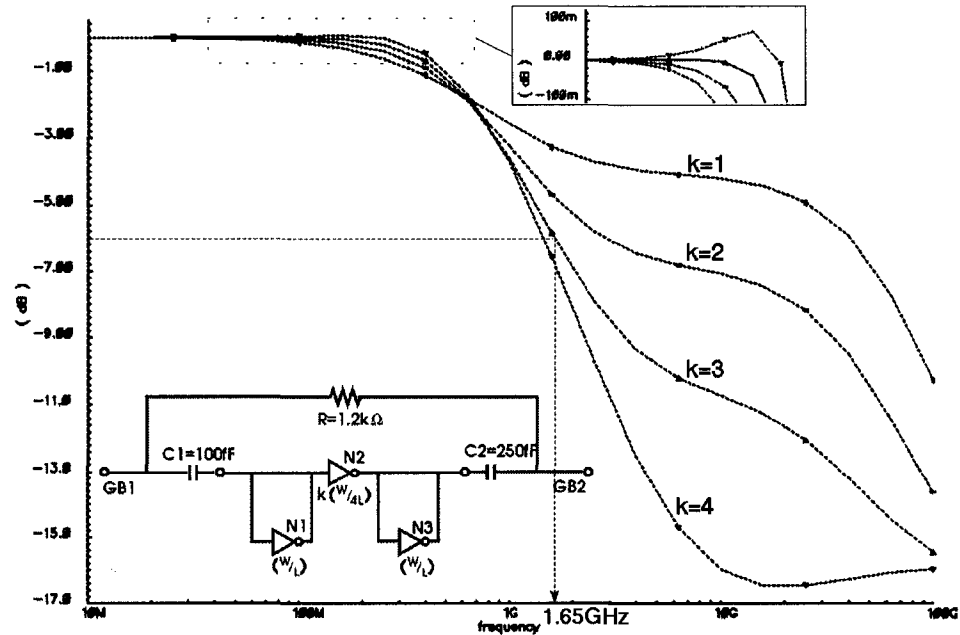


Figure 4.7: Closed loop frequency response of CMOS inverter active suppression circuit

reception sites, such as MOS transistors, wells, substrate and well contacts. The geometric data is analyzed and the substrate parasitic RC elements among the recognized sites are evaluated. A substrate parasitics mesh is generated and passed to SPICE circuit simulator. For comparison purposes, the Cadence SCA tool is also used.

4.5.1 - Active Guard Band Experiments

The objective of this experiment is to prove the effectiveness and viability of the active noise suppression concept, as illustrated in Figure 4.1. The active noise suppression circuits enhance the conventional passive guard bands in shielding substrate noise. In this experiment, the noise suppression circuit is implemented based on modified translinear principle to provide high bandwidth small-signal phase inversions. Figure 3.15 shows the block diagram of the layout. The microphotograph of the experiment fabricated 0.18 μm technology is shown previously in Figure 3.14. Figure 4.8 provides a close-up view of the noise generator, the active guard bands and the noise sensor.

The experiment setup is shared with the substrate coupling experiment described in the previous chapter. It consists of a bank of high-speed inverters to generate digital switching noise. Each noise generator comprises of 4 parallel chains of 16 digital inverters. Each

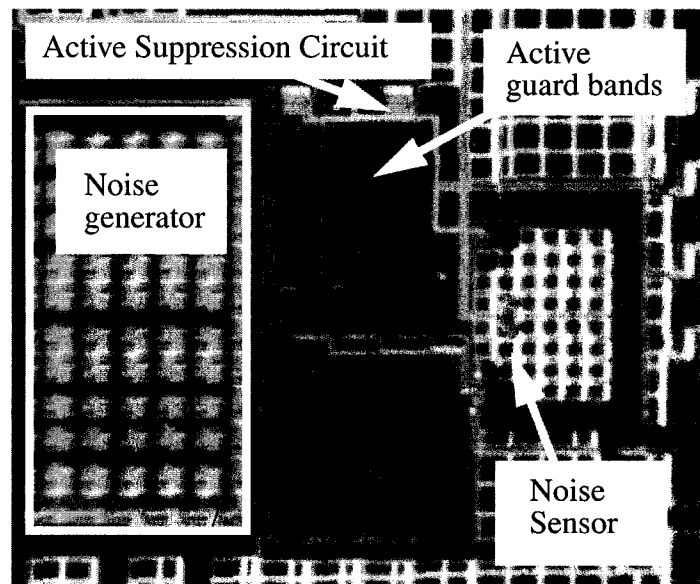


Figure 4.8: Active noise suppression experiments microphotograph

inverter has a 100fF load. The digital switching noise generators are driven by either an external clock or the output of the PLL. From Figure 4.9, an array of 144 switching noise generators is placed near a row of 4 guard bands. A PLL is placed on the other side of the noise generator to accommodate separate experiments described in Chapter 3. The 4 guard bands are placed at different distances from the noise sources. They can connect or disconnect the heavily-doped bulk substrate to the ground supply bias, remains floating. In this experiment, the ground bias are disconnected, and the active suppression circuits are activated. We are primarily interested in heavily-doped bulk epitaxial substrate, which is commonly used in system-on-a-chip designs. The extracted substrate models are both simulated using SPICE simulator. The substrate noise measurement is conducted using a cross-coupled inverter comparator. SPICE simulation results from GEOMEXT and SCA models are compared. Macromodels of active noise suppression guard band that enhances noise insulation efficiency is also incorporated in our GEOMEXT algorithm.

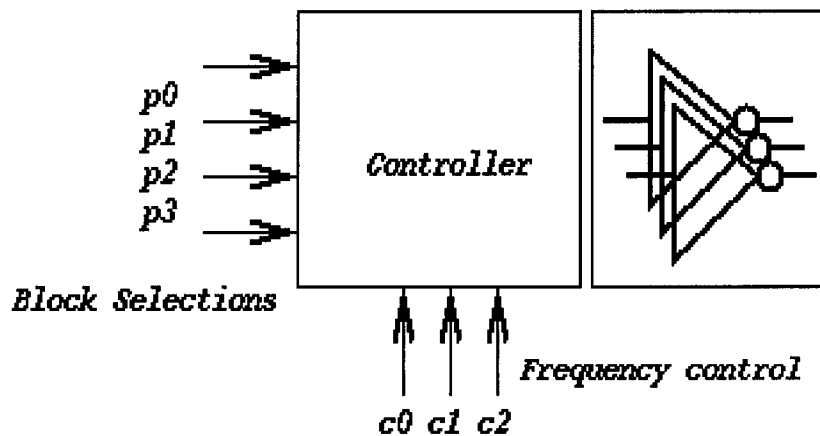


Figure 4.9: Switching noise generator with variable strength and switching frequencies

Figure 4.10 shows the simulated effects of the digital inverter noise suppression circuit in the time domain. Substrate coupled switching noise is injected by CMOS digital gates. Notice that the noise impulses are of duration on the order of 0.1ns. A π -phase shifted suppression signal is generated and is added to the attenuated substrate noise. With active noise suppression operating, the observed switching noise peaks are reduced by 65% nominally, and up to 80% in some cases.

The circuit based on modified translinear principle consumes 4.3mA of current from a 1.8V supply. The total static power consumption is 7.74mW. The total simulated quiescent current for the second active suppression circuit is 84uA. The total static power consumption of the CMOS inverter suppression circuit is 152uW. The translinear amplifier active suppression circuit has been fabricated using CMOS n-well 0.18um technology. A noise sensor using cross-coupled inverters is implemented to facilitate on-chip transient substrate noise measurements. Further circuits implementing the CMOS inverter-based active suppression circuit, that are even more promising, are under way.

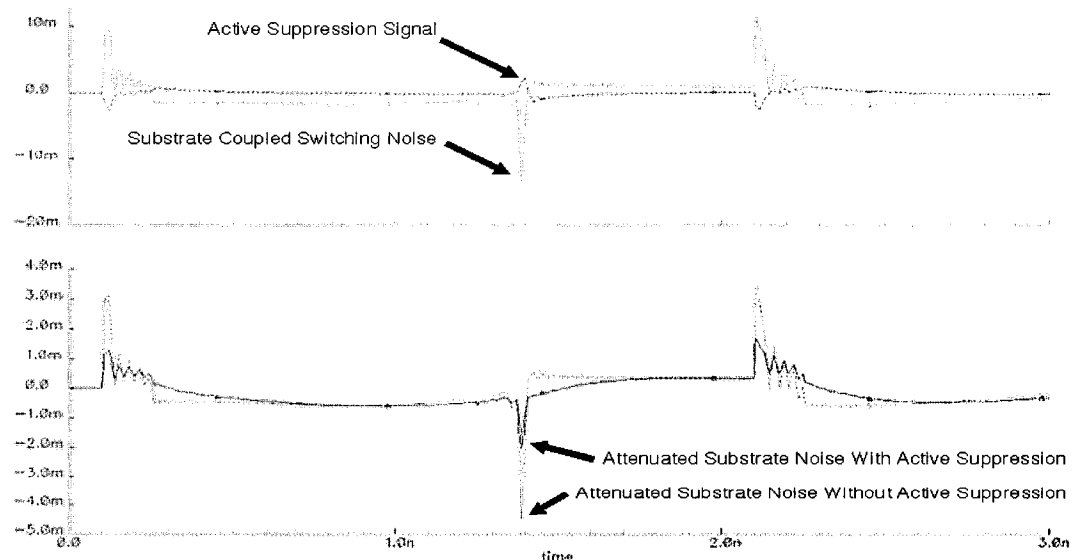


Figure 4.10: Simulated transient effects of active suppression circuit

Chapter 5 - Conclusion

To be able to deliver the promised performance increase with large-scale monolithic mixed-signal systems and SoCs, cost-effective noise shielding schemes must be efficiently applied. This thesis investigated the critical issues involved in determining the optimum means of noise shielding to be applied. To reduce cost, substrate coupling effects must be realized early during the design and signal integrity verification stages. We presented the GEOMEXT substrate parasitic modeling algorithm for large-scale systems as an additional pre-simulation step to enable substrate coupling hazard detections. As the substrate models are expressed in the form of circuit netlists, GEOMEXT is readily usable in any existing design environment. Alternatively, the algorithm can be incorporated into other signal integrity verification tools, such as those used for detecting crosstalk hazards, to extend their abilities in accounting for substrate coupling effects.

We have performed a series of experiments to observe and analyze substrate coupling effects. They are designed to recreate situations in the mixed-signal environment which coupling problems frequently occur. Through the measurements of the substrate potential fluctuations and PLL jitter in the presence of substrate noise, the physical-level and system-level impacts of substrate coupling were noted.

GEOMEXT was designed with practicability in mind and could determine the substrate parasitic models efficiently. Hence it is readily usable with large circuits. It generates a 3-dimensional RC network with a triangular-based construction that is capable of

accommodating local refinements without any increase in its structural complexity. GEOMEXT was applied to our MCSoc design project designs to predict spatially the potential amount of substrate coupling hazards pertained. Its extraction performance and accuracy were compared to Cadence SCA and is found to be superior. The simulation results were similar (after parameter matchings), but the size of the GEOMEXT substrate model is much smaller. Due to the inevitable variations induced by the IC fabrication processes, experiments were conducted to determine the physical parameters for the silicon substrate. Subsequently, these parameters were refitted into the extraction algorithms.

On the other hand, Active Noise Suppression (ANS) circuits were designed to partially equalize the transient substrate noise. Reduction schemes using both passive and active elements to reduce substrate coupling have been suggested. ANS circuits, when mixed with conventional guard ring techniques, can enhance the guard rings' effectiveness. Thus the actual area required by these guard rings is reduced for the same shielding ability, thus saving precious silicon area for additional design functionalities.

The substrate coupling reduction schemes described were applied to the Managed Clock System-on-a-Chip (MCSoc) project. The effectiveness of these schemes were evaluated. Due to the slow IC fabrication turn-over rate, not all experimental measurements were carried out as planned however, observations from substrate model simulations indicate very promising results under some conditions. The work described in this thesis has nevertheless paved the way for further investigations into the problem¹. It has developed the infrastructure needed to solve substrate noise issues in large-scale mixed-signal designs. The resultant substrate noise analysis suite will undoubtedly become a crucial part of future SoC design and verification tools. With the algorithm presented in this thesis, the next step in substrate coupling research is to develop a set of user configurable options to facilitate substrate model generation in different levels of accuracy that better suit the needs in designing systems of various sizes and substrate types.

1. Author of this thesis continues to pursue related research topics in his Ph.D. studies.

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