Fabrication of Indium Nitride Nanowire Hybrid Devices

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DEDICATION

This thesis is dedicated to my dear parents and my beloved Yue.

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Two years ago, when I decided to accept the offer from the Department of Physics at McGill University, I did not expect to learn so much. During the two years, I was exposed to micro-fabrication, nano-electronics and low-temperature physics, and acquired practical knowledge about experimental research. The most valuable things I gained from my lab members and my supervisors are the enthusiasm to explore new and unknown things, and a scientific way of thinking and solving problems – I am sure I will benefit from them throughout my life. Indeed, this work could not have been done without the help of many people.

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ABSTRACT

Semiconductor nanowires, known for their high quality, large surface-to-volume ratio and coaxial quantum confinement, are a promising material for the next generation nano-electronics and nano-photonics devices. Intensive research on this material has been done over the past decade. In particular, the single nanowire electrical device, which can be fabricated using cleanroom technology and is compatible with the well-developed integrated-circuit processing technique, has significant practical applications. In this work, the complete process of fabricating a single nanowire device, from mask design to pre-patterned chip making, from nanowire transfer to nanowire device fabrication, from substrate preparation and cleaning to dicing, from spin-coating and exposure to developing, from metal deposition and lift-off to packaging, was carefully investigated. In addition, basic measurements and preliminary results such as resistance - temperature (R-T) behavior, resistance - magnetic field (R-B) behavior and current - voltage (I-V) curve, are shown. This thesis thus provides detailed information about compatibility of single semiconductor nanowires with the standard integrated-circuit technique and can serve as a manual for single nanowire electrical device fabrication.

ABRÉGÉ

Les nanofils semiconducteurs, connus pour leur haute qualité, leur large rapport surface/volume et leur confinement quantique coaxial, sont des matériaux prometteurs pour la prochaine génération de technologies nanoélectroniques et nanophotoniques. Une recherche intensive sur ces matériaux a été effectuée au cours de la dernière décennie. En particulier, les nanofils, qui peuvent être fabriqués en salle blanche, sont compatibles avec la technique maîtrisée du traitement en circuit intégré et ils ont des applications pratiques significatives. Dans ce travail, le processus complet de fabrication d'un dispositif à nanofil simple, de la conception du masque à la fabrication de puces, du transfert du nanofil à la fabrication de dispositifs à nanofil, de la préparation et nettoyage du substrat au découpage en dés, du dépôt par centrifugation et de l'exposition au développement, de la déposition et décollage du métal à l'emballage, a été examiné soigneusement. En outre, des mesures de base et des résultats préliminaires sont également présentés. Cette thèse fournit donc des informations détaillées sur la compatibilité des nanofils semiconducteurs avec la technique standard de circuit intégré et peut servir de manuel pour la fabrication de dispositifs à base de nanofils simples.

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CHAPTER 1
Introduction

1.1 Aims and motivations

This thesis is part of an ongoing collaborative research project focused on finding Majorana fermions in a one-dimensional nanowire system so as to realise topological quantum computation (TQC)[1] . Majorana fermions, quasiparticles that have a spin of $-\frac{1}{2}$ and are their own anti-particles, were proposed by Ettore Majorana in his seminal paper in 1937[2] . Over the past decade, Majorana fermions have been intensively studied as a potential candidate to realize topological quantum computation[1,3–7] .

TQC requires a non-Abelian statistical system and holds a potentially promising solution for the draw-back of quantum computation due to its potential error-tolerant properties. Many exotic properties in condensed matter systems, such as Pfaffian states in fractional quantum Hall (FQH) systems[8–11] , chiral p-wave superconductors[12–14] , surface states of a topological insulator (TI) in which s-wave superconductivity is induced by proximity effect[15–17] , as well as the Majorana fermions[18–20] , have been proposed as platforms to support quasiparticles with non-Abelian statistics. Among these systems, Majorana fermions stand out as it is believed they can be "engineered" in a very simple approach: it is proposed that the Majorana modes can be detected by scanning tunnelling microscopy (STM) at the end of a nanowire with a strong spin-orbit coupling such as InAs[21–23] and InSb[24,25] , and is located in proximity of s-wave superconductors[26–29] . The proposed structure is basically a nanowire-based Josephson junction. To support Majorana modes, such devices must be clean and robust against perturbations

and impurity-based offsets. In this sense, making robust nanowire devices is an important step towards realizing TQC platforms.

The primary goal of this work is to establish a micro-fabrication method to make robust nanowire hybrid devices (with and without superconductors for comparison purposes) that can be used in experiments whose goal is to study Majorana modes in a condensed matter system. A variety of micro-fabrication processes were developed to make good contacts on the nanowires throughout the course of this work.

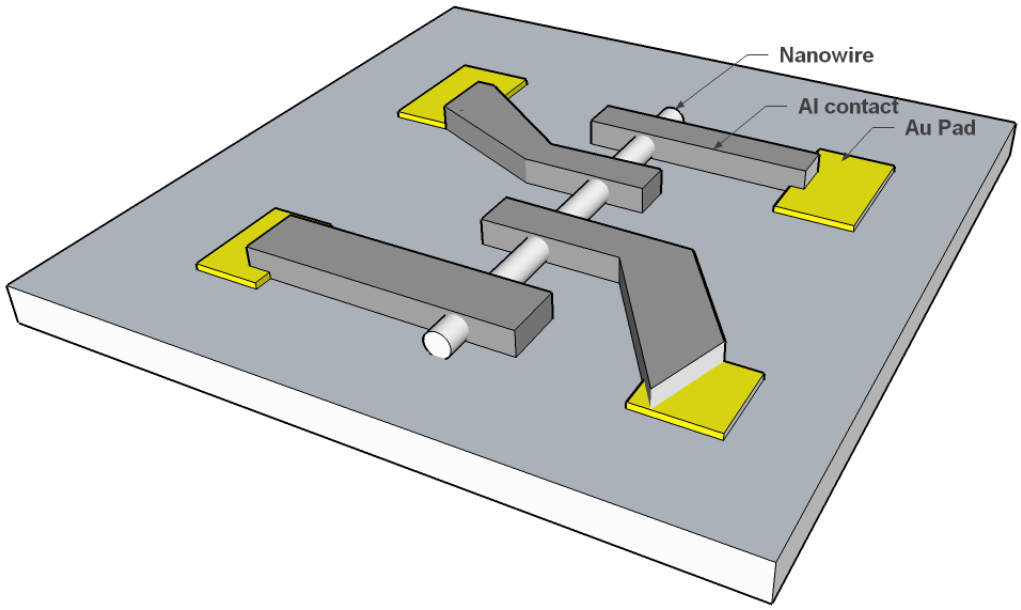

Figure 1–1: **Sketch of a four-terminal nanowire device.**

1.2 Device introduction

The device is essentially a nanowire (*Sec.1.2.3*) with at least two contacts (Fig.1-1). When the contacts are made from superconductors, the junction fabricated forms a Josephson junction (*Sec.1.2.2*). Standard clean-room technology (*Sec.1.2.1*) is used in fabricating such devices.

1.2.1 Cleanroom technology

The success of integrated-circuit processing techniques makes cleanrooms an important component of modern technology. The core of the cleanroom technology is, of course, micro-fabrication. Generally, a micro-fabrication process includes depositing resist on a substrate, patterning the substrate with the desired micro- or nano- features, removing (or etching) unwanted parts of the resist, and depositing metals onto the substrate to keep the features. Many important devices are now micro-fabricated with cleanroom technology: integrated circuits, micro-electro-mechanical systems (MEMS), micro-fluidic devices, light-emitting diodes (LEDs), solar cells, sensors (bio-sensors, micro-sensors and nano-sensors), etc. It is thus not surprising that quantum computers, the next generation computers, will likely be developed with cleanroom technology.

1.2.2 Josephson junctions

A Josephson junction is generally known as two superconductors connected by a non-conducting material with an energy barrier, usually an insulator[30] . A notable application of the Josephson junction is superconducting quantum interference devices (SQUIDs), which can be used as a component of a quantum computer[31] . The system is attractive due to the low energy dissipation of superconductors. Furthermore, the compatibility with cleanroom technology makes fabrication of complex circuits straightforward, given the continuous success of integrated-circuit processing with cleanroom technology.

Recently, it has been argued that semiconductors may also be used to build Josephson junctions.

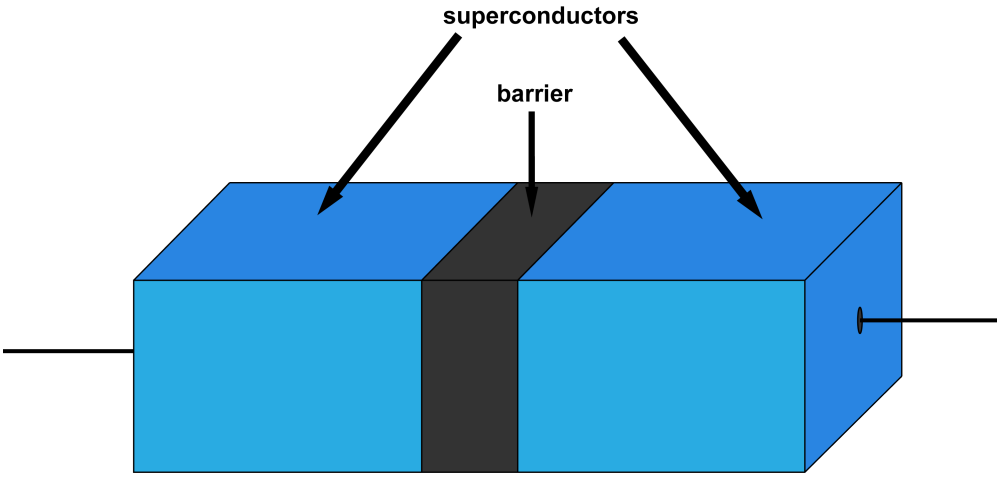

Figure 1–2: **Schematic drawing of a Josephson Junction.**

1.2.3 Proximity effect

The superconducting proximity effect occurs when a superconductor is put in contact with a non-superconductor. Below the critical temperature of the superconductor, Cooper pairs from the superconductor will diffuse into the non-superconductor within the coherence length. As a result, the non-superconductor will have weak superconductivity. Since Josephson junctions naturally have such structure, proximity effect is expected to be observed in semiconductors[32] .

1.2.4 Semiconductor nanowires

A nanowire is a wire with the diameter on the order of nanometers. Semiconductor nanowires are a very attractive candidate to be the building blocks of next generation nano-electonics and have been under intensive investigation for the past decade. A variety of nanowire-based electronic devices have been realized, including field-effect transistors[33] , logic circuits[34] , decoders[35] , etc.

From the point of view of fundamental physics, semiconductor nanowires are also of special interest. Lateral quantum confinement of the nanowire forces electrons to occupy discrete energy levels that are different from continuum levels of bulk structures. In addition to quantum confinement, the feasibility of synthesizing high quality semiconductor nanowires makes them an ideal platform to probe properties that may be inaccessible with large-scale structures. For example, intensive research has been done with nanowires on Luttinger liquid physics, which requires a one-dimensional clean material[36] .

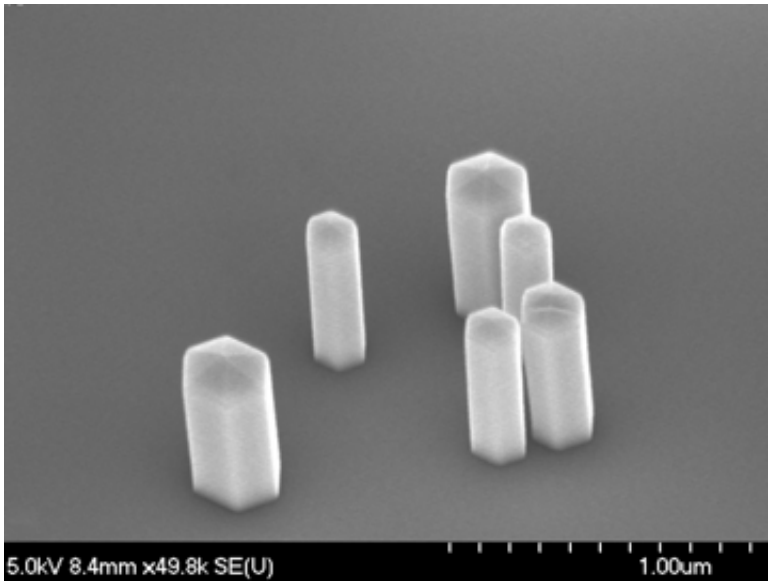

Figure 1–3: **Nanowires used in this work.**

Since we did not have nanowires made with strong spin-orbit coupling materials such as InAs and InSb, the nanowires used in this work are mostly intrinsic InN nanowires grown by Mi's Group at McGill. They are typically 200 nm to 300 nm in diameter and $1.5\ \mu$m to $2\ \mu$m in length. Even though InN does not have strong spin-orbit coupling compared to InAs and InSb, and so is unsuitable for the final goal of this project, these nanowires are of

impressively high quality[37] , and are a good starting point for investigating the physics of superconducting proximity effect in semiconductors.

1.3 Outline

A brief description of the chapters of this thesis will now be given. First and foremost, the fabrication method used in this work is discussed. As fabrication is the major part of the work, a detailed process flow will be introduced. Then, some important results from the electrical measurement, such as temperature and magnetic field dependences of resistance and current as a function of voltage, will be shown and discussed.

CHAPTER 2
Device Fabrication

2.1 Pre-patterned chip fabrication: photolithography

Nanowire devices, due to their small feature sizes (~ 100 nm), are first connected to the metal patterns (~ 100 μm) and then encapsulated with metal wires of ~ 40 μm. As the feature size of these metal patterns is relatively large, standard photolithography can be used. Photolithography is one of the most widely used methods in making thin film patterns. It shares some principles with photography, as patterns in the film (photo-resist) are created by exposing to it light (ultraviolet light) and developed by soaking it in a special solution. In this work, the iteration of photolithography has several steps: substrate-preparation, pre-baking, photo-resist coating, soft-baking, exposure, development, metal-deposition and lift-off. As a standard practice, grid-like metal patterns are made on oxide-coated wafers in order to divide them, identify the regions and make packaging devices more efficient.

2.1.1 Mask Design

A glass mask was used in the photolithography process to generate desired patterns repeatedly. In the mask, patterns are written on one side with chromium, which is opaque to UV light. This mask is either designed for positive resists with patterns left blank and the rest coated with chromium, or for negative resists with patterns coated with chromium and the rest blank. As is well known, positive photo-resists are generally more precise

than negative resists, and owing to the high resolution demand of this work, masks used here were all designed for positive photo-resists.

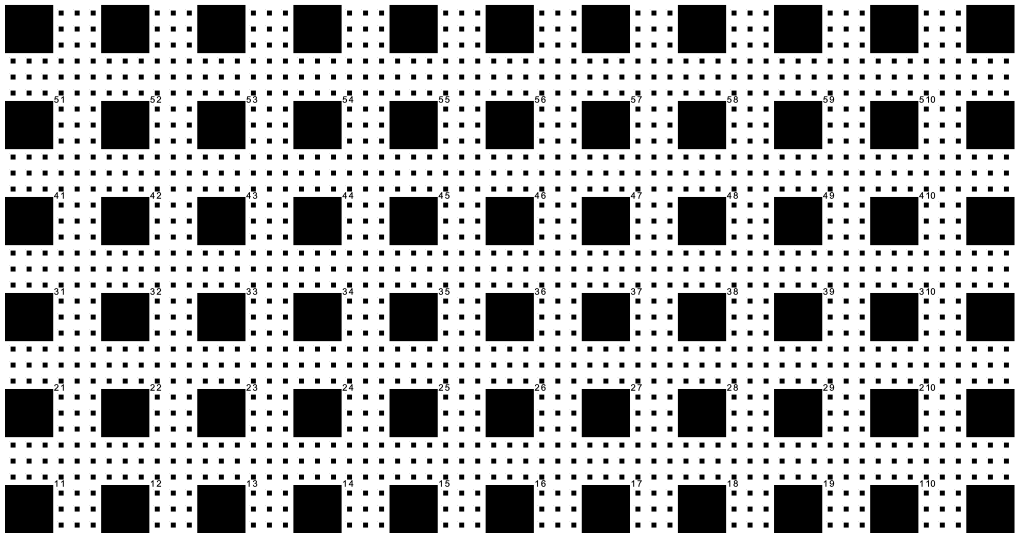

Figure 2–1: **Design of the "pads-array" mask (part of one unit).** The overall size of one pattern unit is 9.3 mm $\times$ 3.3 mm. Large pads are 300 μm $\times$ 300 μm and auxiliary pads are 30 μm $\times$ 30 μm. Spacing is 300 μm between two large pads, 70 μm between two auxiliary pads, and 35 μm between large and adjacent auxiliary pads.

In this work, two kinds of three-inch masks were designed and used. The earlier version is called "pads-array". As shown in Fig.2-1, the mask mainly contains three parts: the numbers, the large pads and the auxiliary pads. The numbers are used to indicate the location of large pads under scanning electron microscope (SEM), with the first digit identifying rows and the latter one or two digits identifying columns; the large pads are designed for wire-bonding to 8-pin or 16-pin side-brazed dual in-line ceramic packages (DIPs); the small auxiliary pads are added to help connect nanowire devices to large pads. Eventually, by connecting through small pads and large pads, nanowire devices will be bonded to the DIPs.

The whole pattern unit is then repeated to make an entire mask. After photolithography, patterns are transferred from the mask to the substrate and kept on the substrate permanently by metal deposition and lift-off (see *Sec.2.1.6*). The substrate is divided into several small chips via dicing (*Sec.2.1.6*).

A "pads-array" chip usually has 4-5 rows and 5-6 columns of large pads (2.7 mm by 4.6 mm on average), and is capable of making 12-15 two-terminal and 8-10 four-terminal devices (see *Sec.2.3.2* for two- and four-terminal device design). However, owing to a lack of uniformity of the resist coated (see *Sec.2.1.3* for resist-coating), pads on the edge can not be used. So, in practice, only 6-8 two-terminal and 5-8 four-terminal devices can be made.

Being the starting point of the work, this design has an advantage of being simple. In addition, the design takes care of several important issues in the processing. First, large pattern size makes photolithography easier and less rigorous. Second, large spacing (300 μm) between pads makes it easier to avoid patterns getting cut through when dicing a whole wafer/substrate. Third, having large-sized pads allows more space for wire-bonding. Fourth, using little metal leaves space for nanowires to lay and also provides benefits for the lift-off process later.

However, practical use of this design revealed that the numbers were a bit of a flaw, in that the non-uniformity of digits (two digits become three digits when the column goes over nine, see Fig.2-1) caused problems in identifying the locations of some large pads under SEM, as the photolithography is not always perfect (e.g. it can be confusing if the number "110" has a defect and misses a "0"). Besides, identical design of small auxiliary pads makes it hard to know the position of each pad. Frequent usage also showed that large pads are too large since they unnecessarily take up too

much space and the middle ones, being too far from the edge, are difficult to bond. With large pads being too close to where nanowire devices are fabricated, the devices were occasionally broken by the sonication created by the wire-bonder. In addition, the long design (9.3 mm) makes spin-coating difficult. Even when the chips are cut in half, which sacrifices some usable space, resist on the edges is still thicker after spinning due to the chips' rectangular shape, making the usable area relatively small (1/3 of the chip on average). Moreover, the long design does not fit the 8-pin DIPs very well, which are preferred due to their flexibility.

In order to solve the above problems found during practical use, and also to incorporate the feature of atomic force microscope (AFM) compatibility, with which only an area of around 10 μm by 10 μm can be identified, a second mask was designed (Fig.2-2).

This "AFM-friendly" mask contains mainly four parts: the numbers, the large pads, the side pads, and the small dot array areas. The numbers are set to be uniformly two digits, with the first one identifying the rows and second, the columns. The large pads, 100 μm by 200 μm, are now only used for connecting out nanowire devices. They are then linked to the side pads designed for wire-bonding. The small dot array area, 20 μm by 20 μm and upgraded from the previous small auxiliary pads, is constructed by a binary dot array (dots) and a encapsulation frame. The binary array is unique for each small dot area: it can give the coordinates of its center with a customized program so as to identify its location.

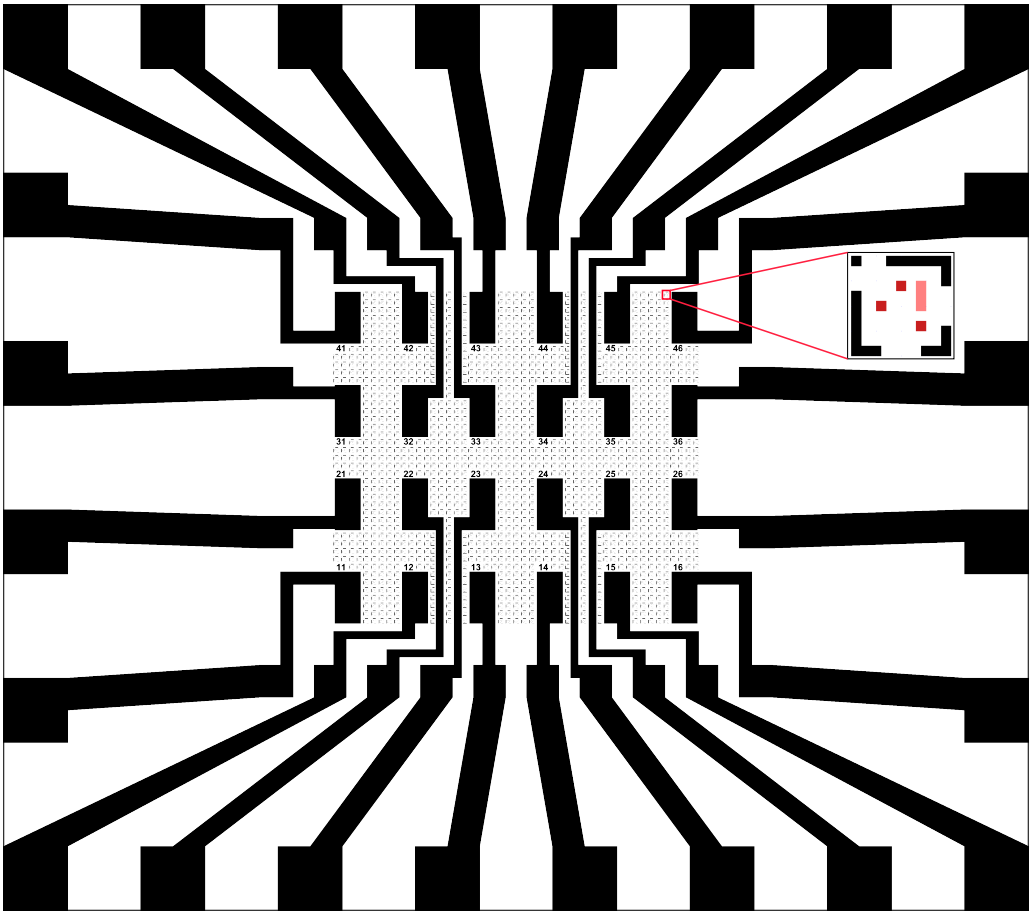

Figure 2–2: **Design of the "AFM-friendly" mask (one unit).** The overall size is 3.95 mm $\times$ 3.5 mm. Side pads are 200 μm $\times$ 200 μm, large pads are 100 μm $\times$ 200 μm and binary dot arrays (with frame) are 20 μm $\times$ 20 μm in which each dot (including the dot in the frame) is 2 μm $\times$ 2 μm and the frame is 2 μm in width and breaks on each side. Spacing is 280 μm laterally and 400 μm vertically between two side pads, 160 μm both laterally and vertically between two large pads, 10 μm between two binary dot arrays (with frame), and 5 μm between large pads and adjacent binary dot arrays. **Inset:** An example of the dot array. The binary dot arrays are all unique.

The encapsulation frame is added for several reasons: first and foremost, the frame can separate dot arrays from one another to clarify the area

of each one, making it more convenient to identify every dot array with an AFM; second, the frame will also be used for four-window alignment in electron beam lithography (see *Sec. 2.3.2*). In addition, the frame is designed to be intermittent so that nanowires inside the area can still be connected out without being shorted by the frame itself, and the dot on the upper-left corner of the frame is designed to indicate the upright direction.

Compared to the previous design, this mask has four advantages. First, with large pads much closer (160 μm now compared to 300 μm in the "pads-array" mask), connecting nanowire devices to the pads becomes more efficient, especially when making a four-terminal device. Second, wire-bonding becomes more efficient since only side pads need to be bonded while in previous design pads in the middle also need to be bonded, and more space is saved compared to previous large pads. Third, with side pads being far from the nanowire devices (between two large pads), wire-bonding never breaks the devices. Fourth, the unique binary dots makes it easier to find the current position under a scanning probe so that locating nanowires and making devices are far more efficient.

One major flaw it brings, however, is the difficulty in a later lift-off process for electron-beam lithography, since the many binary dots, which eventually become metal dots on the substrate, tend to hold new metal deposited onto the substrate. Besides, these metal dots also shrink the space for the nanowire devices.

The two designs differ from common masks in that they do not have alignment marks. Generally, a complete fabrication process will contain multiple photolithography processes during which several masks are used sequentially, with alignment marks on each mask to align the pattern at desired

positions. However, since there is only one single step of photolithography in this work, the alignment marks are not necessary.

2.1.2 Substrate preparation and cleaning

For measurement purposes, it is preferable that the nanowire devices can be back-gated and thus, located on an insulator. This is conventionally achieved with the metal and the insulator being silicon dioxide on top of the silicon substrate, forming a metal-oxide-semiconductor field-effect transistor (MOSFET) structure. Therefore, rather than bare silicon wafers, silicon dioxide (SiO_2) coated wafers were used.

In this work, we used two kinds of silicon dioxide coated wafers. The first kind is a 2-inch n-type wafer with home-coated SiO_2 layer. SiO_2 was grown using thermal oxidation via low-pressure chemical vapor deposition (LPCVD). The thickness of this SiO_2 layer is 200 nm. Possibly due to the oxide layer being too thin, this kind of wafer was unable to be gated and therefore a new type of wafer was used. The new type is a commercial, n-type, four-inch standard wafer. It has a 300 nm high quality oxide layer and can be gated at low-temperature.

After thermal oxidation, SiO_2 will form on both the front (polished) and back (unpolished) sides of the wafer. To incorporate a back-gate, the oxide layer on the back needs to be removed first. Diluted hydrofluoric acid (HF), a 10:1 mixture of deionized water and HF (49% stock concentration), is used to remove oxide from the wafers. Since HF will etch out the oxide layer isotropically, the front side should be protected by coating it with a thin layer of some resist (usually Shipley 1800 series, see *Sec. 2.1.3*). Then the wafer is soaked in the HF solution. The etching rate of the diluted HF is 23.5 nm to

25 nm per minute at room temperature, so 5 to 10 min is enough. Nevertheless, the etching duration can be judged visually as the oxide layer (namely glass) has a different reflection coefficient than bare silicon substrate; thus the back side will change from a shiny, smooth surface to a grey, coarse one (this can later be verified by ellipsometry). After this, the wafer is rinsed in deionized water for 1 to 2 min to wash out HF and dried with nitrogen gas so as to prevent dust particles from attaching to the surface. The resist can be washed away using acetone afterwards (see *cleaning process II* below).

As a result of this previous step, an oxide-coated wafer will have organic residues as well as metal ions on it. Therefore, it is always necessary to clean the wafer before using it. This will require at least two cleaning steps (cleaning process I). The piranha solution is first used to remove possible organic residue from the wafer. This solution is a mixture made from three parts concentrated sulfuric acid (H_2SO_4, 98% stock concentration) and one part hydrogen peroxide (H_2O_2, 30% stock concentration). When making the solution, only glass containers can be used as H_2SO_4 can carbonize organic containers, and H_2O_2 must be added to the H_2SO_4 to avoid splash. The solution should be used right after it is made. By soaking the wafer in the solution for 10 min, most organic residues, such as residues of photo-resist and/or acetone, will be removed. The cleaned wafer then needs to be put in a deionized water bath, for a rinse of three-cycle (around 2 min each cycle). Secondly, the "famous" RCA-2 clean process[38] is used to remove metal ions from the wafers. This solution is made from six parts deionized water, one part hydrochloric acid (HCl, 37% stock concentration) and one part 30% H_2O_2. When making the solution, deionized water is first put into the container followed by HCl, and the solution should be heated up to 70 - 80 ℃ using a hotplate. 30% H_2O_2 should also be added once the temperature is

reached. Metal ions are removed by soaking the wafer in this solution for 10 to 15 min. After this, the wafer can be rinsed in a water bath for 3 min and dried in nitrogen air-flow. In addition, since three-inch masks are used, the substrates need to be no larger than three inches to avoid wasting. Thus, the four-inch wafer must be first cut by a diamond (usually into quarters) before cleaning.

As the wafer mainly deals with resist after the initial cleaning, there will be mostly organic residues. A simpler cleaning process can be used to get rid of them fast (cleaning process II). First, resist residues or resists (Note *cleaning process I* should not be used to clean the resists themselves) can be washed away by soaking the wafer in acetone for roughly 30 s, and the result can be judged visually. Then the wafer should be put in isopropanol (IPA) for another 30 s, to get rid of acetone residue and finally in deionized water for 30 s to clean IPA residue. In the end, the wafer is always dried with nitrogen gas.

2.1.3 Spin-coating and soft-bake

Spin-coating is the most important process towards a successful lithography: by spraying resist on the substrate while attached to a spinner, and spinning the substrate at a relatively high speed, a thin layer of resist is formed on top of the substrate (see Fig.2-3). Adhesion, uniformity and thickness of the resists are three critical criteria for the quality of the spin-coating.

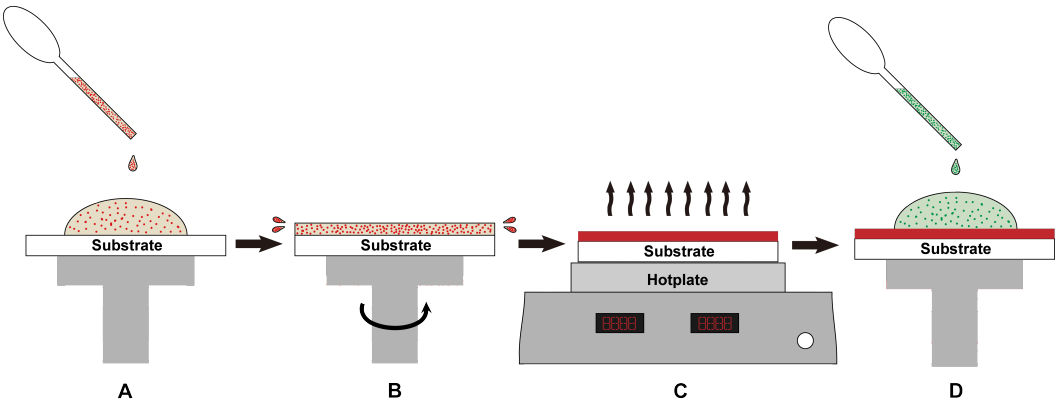

Figure 2–3: **Complete process of spin-coating.** A complete spin-coating process includes: **A.** Applying sufficient resist solution to cover most of the substrate, which is attached to a spin-coater. **B.** Rotating/spinning the substrate at a proper speed with the spin-coater. **C.** Baking the sample at a certain temperature with a hotplate or an oven (soft-bake). **D.** After soft-baking, continuing to coat a second layer of resist if necessary.

While adhesion can affect the quality of the development, uniformity of the resist determines the conformity of the patterns after development and thickness is an important factor concerning resolution, dose and developing time. A clean substrate is the prerequisite of uniformity. Therefore before coating, it is always necessary to clean the substrate – at least the *cleaning process II* introduced in *Sec.2.1.2* should be used. After cleaning, there may be moisture left on the substrate. It may be baked (at ~ 115 ℃) for some time (~ 5 min) to have better adhesion ("pre-baking"). Then the substrate can proceed to resist-coating.

For most photo-resists, a spinning speed of 3950 rpm with a sufficient acceleration (usually $1350\ \mathrm{rad/s^2}$) and a spinning duration of 45 s are usually sufficient to get a uniform thin film of resist. In addition to proper spinning speed and duration, it is best that the substrate be round or square, with

its center aligned to that of the spinner, so as to make the resist evenly distributed. However, even with round substrates, resist at the edge can be thicker, and can affect the distance between the mask and the substrate, and thus the quality of the lithography. This can be compensated for by wiping off the resist on the edge carefully using acetone.

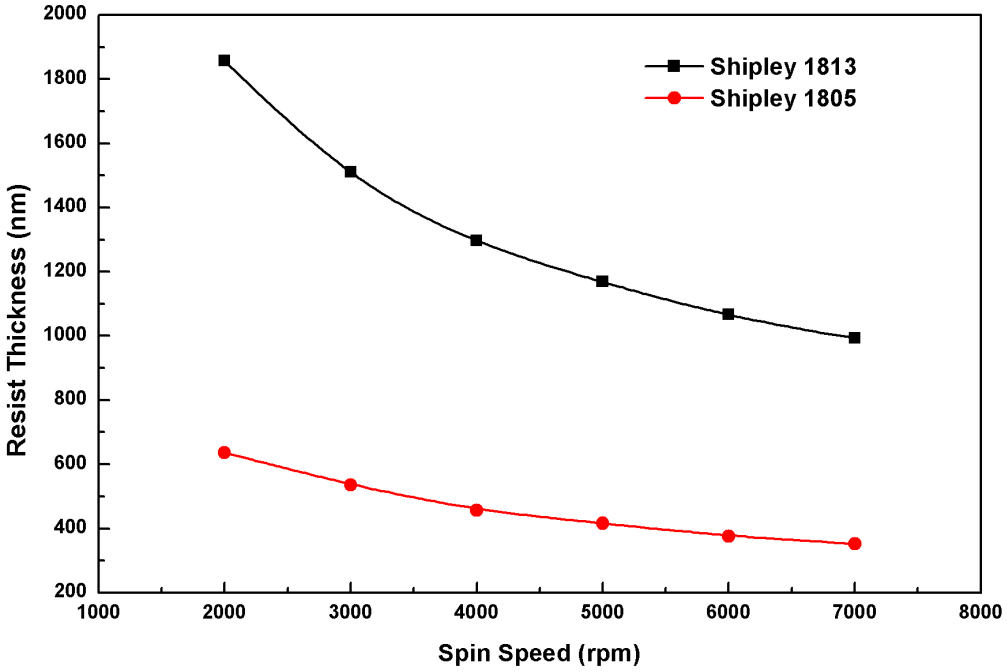

Figure 2–4: **Film thicknesses versus spin speed for Shipley® 1800 series.** Note that the actual thickness may vary with resist condition. For example, if the resist is close to expiration, it will become thicker as evaporation of the solvent leads to a higher viscosity. Figure reproduced from brochure of MICROPOSIT® S1800® series photo resists.

The final thickness of the resist is also determined by the spinning speed (Fig.2-4). Within a certain range, a higher spinning speed will result in a thinner resist film, but this effect saturates at a certain point above which the resist will no longer be thinner.

Table 2–1: **Spin-coating parameters used and corresponding resolution†.**

Resist type	Spin speed & duration	Bake temp. & duration	Final thickness	Resolution
Shipley® 1813	3950 rpm, 45s	115℃, 60s	$\sim 1.4\ \mu$m	$5 - 5.5\ \mu$m
Shipley® 1813	5000 rpm, 30s	115℃, 60s	$\sim 1.2\ \mu$m	$5 - 5.5\ \mu$m
Shipley® 1805	3950 rpm, 45s	115℃, 60s	$\sim 0.5\ \mu$m	$2 - 2.3\ \mu$m

† Note the acceleration is $1350\ \mathrm{rad/s^2}$ and the temperature may fluctuate a little (from 95℃ to 120℃); however, the final thickness and resolution are not affected significantly.

Once coated with resist, the substrate is heated (~ 100℃) to drive away solvent from the resist. This improves the adhesion of the resist to the substrate and it anneals the stress introduced during spinning. This is known as "soft-bake" (Fig.2-3C). For Shipley photo-resists, the soft-baking temperature ranges from 95℃ to 115℃ and baking duration can range from 60 s to several minutes, depending on the type of resist used. Sometimes another hard-baking process is used to anneal and strengthen the developed resist, with a baking temperature higher than that of the soft-bake (usually 150℃ - 180℃). Hard-bake is not good for the lift-off process since it makes the resist harder to be stripped, so it is not used in this work. In addition, if working with negative resist such as SU-8, a post-bake basically at the same temperature as soft-bake, must be done before development to denature the resist and reveal the pattern.

In this work, different positive resists were used to achieve the wanted resolution (see Table 2-1). For the "pads-array" mask, the common Shipley 1813 is used. At a spinning speed of 3950 rpm for 45 s followed by a soft-bake at 115℃ for 60 s, this type of resist usually has a thickness of $1.4\ \mu$m,

which is good enough to achieve a resolution of $\sim 5\ \mu$m (Tab.2-1). For the "AFM-friendly" mask which requires a better resolution, Shipley 1805 was used. By using different exposure and developing parameters, Shipley 1813 is able to achieve the higher resolution required by the "AFM-friendly" mask, however the conditions are more rigorous and sometimes many lithography defects such as incomplete patterns on the substrate are created. Being more dilute than Shipley 1813, Shipley 1805 reaches a thickness of 600 nm at 3950 rpm for 45 s followed by a soft-bake at 115℃ for 60 s, which can easily achieve a resolution of $\sim 2\ \mu$m or less.

2.1.4 Exposure

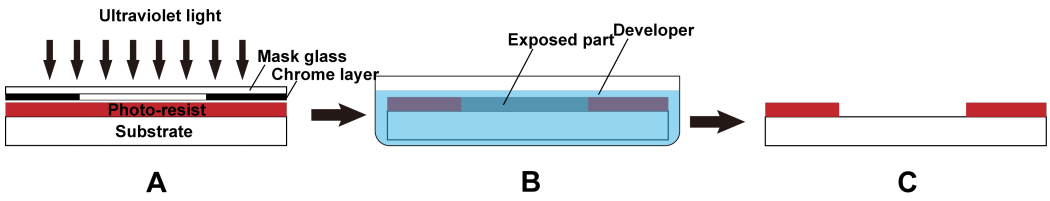

Figure 2–5: **Exposure and development. A.** The resist-coated substrate is exposed under UV light with a glass mask with the chrome-coated side facing the substrate. **B.** After exposure, part of the resist (exposed to UV light) will change properties. The substrate is then soaked in the developer. **C.** Denatured parts of the resist are stripped during development and patterns are revealed.

Exposure is the core process of lithography. This is done with an ultraviolet (UV) mask aligner. By putting a mask above the substrate and exposing it under UV light of certain strength for certain amount of time ("dose"), the pattern can be transferred from the mask to the resist (Fig.2-5A). Its name aligner comes from the fact that normally multiple masks are used successively, and must be aligned with alignment marks from patterns previously

made on the substrate to fabricate devices. However, here only one step photolithography is done, so it is not necessary to align the mask prior to the exposure.

There are mainly three exposure methods: contact, proximity and projection. In the contact method, the mask is put in direct contact with the resist-coated substrate and exposed to the UV light, while in the proximity method, a small gap is kept between mask and the substrate. Projection method is used by very-large-scale integration (VLSI). It projects only part of the mask to the substrate each time to achieve high resolution and completes exposing the whole mask by projecting many times. Among the three, the contact method is the simplest and can achieve high resolution although it may risk breaking the substrate or may even pollute it.

In this work, the contact method is used as it achieves both simplicity and high resolution. Within the contact method there are also two modes: the hard contact mode and the soft contact mode. Soft contact mode is similar to the proximity method, in which the mask is not put in tight contact with the substrate. It can avoid the mask being polluted but as the mask is still away from the substrate, the patterns will cast shadows on the substrate which lower the resolution. On the other hand, the hard contact mode reduces the shadow effect and can reach a higher resolution, but is liable to damage the substrate and pollute the mask. In reality, in the hard contact mode there is still a tiny gap between the mask and the substrate ($\sim 80\ \mu$m). Nonetheless, the hard contact mode is used to achieve good resolution in this work. As a result, the masks need to be checked and cleaned before using. The cleaning process for the mask is the same as *cleaning process II* introduced in *Sec.2.1.2*: first spray acetone to the surface to dissolve photo-resist and/or other organic residues – a soft clean tissue can be used to wipe away these

residues effectively – then use IPA to wash away acetone and water to clean IPA and finally dry the mask with nitrogen gas.

Table 2–2: **Exposure and developing parameters used‡.**

Resist type	Mask type	Dose	Developing time	Resolution achieved
Shipley® 1813	pads-array	60 $\mathrm{mJ/cm^2}$	15 s	5.0 μm
Shipley® 1805	AFM-friendly	30 $\mathrm{mJ/cm^2}$	10 s	2.2 μm

‡ Note the dose and developing time may vary with conditions of the resists.

For exposure, the most important parameter to tweak is the exposure dose. Similar to taking a photograph, the resist could be overexposed or underexposed, and thus an appropriate dose (usually from 20 $\mathrm{mJ/cm^2}$ to 200 $\mathrm{mJ/cm^2}$) is usually necessary. The dose can be different for different resists. Normally, a thinner resist of the same type will require a smaller dose than a thicker one (see Tab.2-2 for details).

2.1.5 Development

Just as in photography, patterns are not revealed unless they are developed in specific solvents (Fig.2-5B, C). Different solvents, known as developers, are used to reveal patterns for different resists. The developing process is in fact a wet etching process - the developers are only more sensitive to places directly exposed under UV light. This means by putting the exposed substrate in a developer for a sufficiently long time, the unexposed parts can also be etched away. Therefore, a good developing time will depend on type and thickness of the resist. Typical developing time ranges

from several seconds to several minutes. As photo-resists have high viscosity, the etched resist tends to stay where it is and may skew judgement of the developing time. The substrate can be gently swayed during developing and a sufficient large container for the developer is usually necessary. The substrate must then be rinsed in deionized water right away, as the remaining developer will continue developing the resist. When rinsing the substrate, developer residue on its back side must also be washed away in case they flow to the front side. The substrate must be dried by nitrogen gas afterwards.

It can be found from the literature that both dose and developing time depend on resist type and thickness[39,40] . They are also not independent of one another: a larger dose will require a shorter developing time and vice versa. In this sense, overexposure can sometimes be compensated for by a shorter developing time, and underexposure, by a longer developing time. To have better control over the developing quality and enough tolerance of variations in the developing duration, a slightly longer developing time is always preferred. However, there is always an optimal point at which the best developing result can be achieved given proper resist thickness, dose and developing time.

Developer MF-319 is a developer specially designed for the Shipley 1800 series resists. Normally, soaking the exposed substrate in MF-319 solvent for 45 s to 60 s gives a clearly defined pattern (in hard contact mode with dose around $60\ \mathrm{mJ/cm^2}$, bare wafer without oxide). In this work, the Shipley 1813 is developed in MF-319 for 15-20 s, and Shipley 1805 developed for 10-15 s (Fig.2-6). Sometimes, the resist can be developed very quickly, in two to three seconds, for example. This might be because of a very large

dose, or a bad resist-substrate adhesion. In such cases, pre-baking the substrate before coating is necessary.

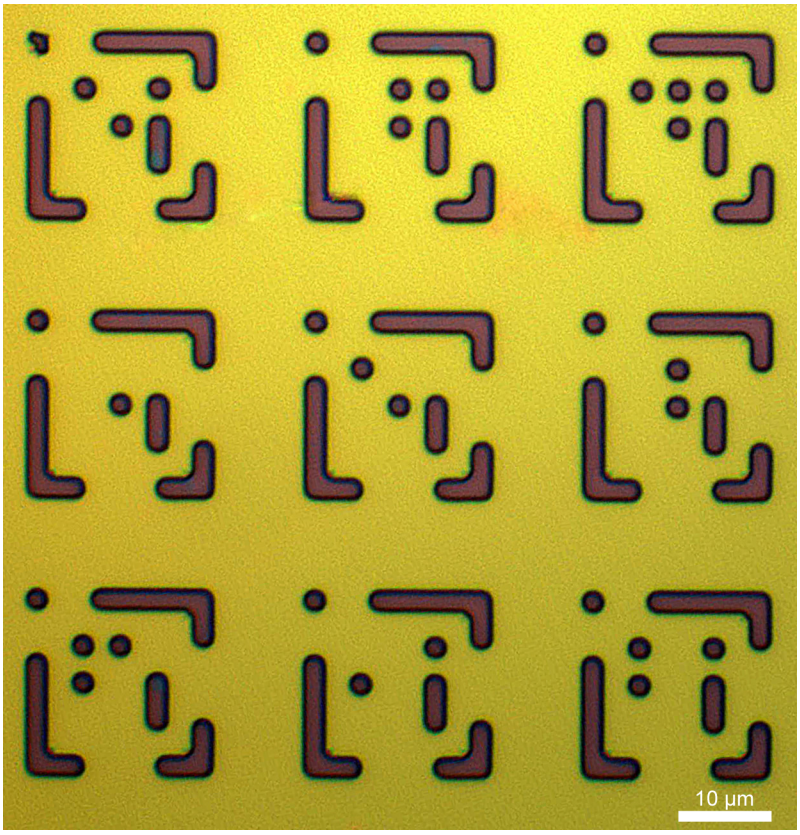

Figure 2–6: **Patterns after development ("AFM-friendly" mask, part).** The golden part is the remaining S1805 resist while the magenta part is the substrate. The resolution is $\sim 2.2\ \mu$m. The dots and edges of the patterns are round due to diffraction of the UV light. Note the frame point on the left top is a typical lithography defect.

2.1.6 Metal deposition and lift-off

After development, a metal-deposition process is done using the e-beam evaporator in order to generate patterns (Fig.2-7A, B). The e-beam evaporator has the advantage of depositing metal with small grain size and high

purity owing to its high vacuum ($\leq 10^{-6}$ torr). Furthermore, the deposition is not conformal compared to sputtering. To achieve good ohmic contacts and to avoid oxidation, gold is often the best choice for the metal pads. However, since gold has adhesive problems with silicon and silicon dioxide, a very thin layer of titanium (5 nm to 20 nm) is deposited first to attach gold to the substrate. The whole substrate is covered with metal after deposition: places where resist is developed will have metal directly on the substrate whereas other places (unwanted part) will have a resist layer between the metal and substrate.

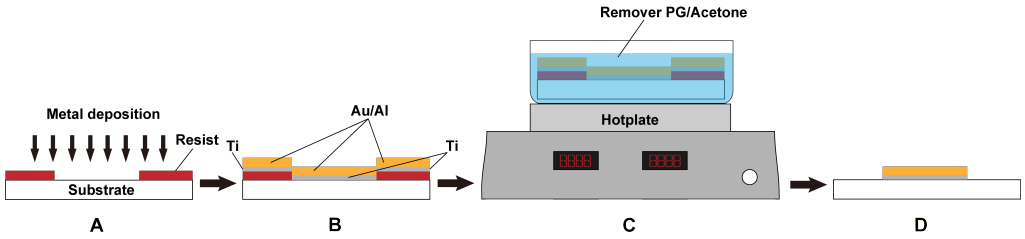

Figure 2–7: **Metal deposition and lift-off. A.** Metals are directly deposited on the developed substrate. **B.** Normally, at least two layers of metal are deposited: the first (usually titanium or nickel) is very thin (5 nm to 20 nm) and is used for metal-substrate adhesion, while the second is desired metal layer. **C.** The substrate is then soaked in Remover PG or acetone to lift-off. They can also be heated directly with a hotplate or in a hot water-bath. **D.** After several minutes up to four hours, the metal with resist underneath, namely the unwanted part, will be stripped, leaving only desired metal patterns.

Using a lift-off process, the unwanted part will be removed (Fig.2-7C, D). Lift-off can be done by soaking the substrate in Remover PG or acetone, in a water bath. Heating the solution can help to lift the metal off. Compared to acetone, Remover PG is more delicate and can work at relatively high temperature (higher than 60℃ whereas acetone boils at around 56℃), thus

it can be more efficient. However, for the lift-off process of Shipley series resists, heating is not necessary and acetone is good enough: in places with remaining photo-resist, the thin metal film will get wrinkled once the substrate is soaked in acetone. A pipette can be used to create bubbles to help lift the metals off. In addition, sonication can also be used. With a gentle power, it can help to get rid of unwanted metal quickly. However, using sonication may also destroy delicate parts of the patterns, and may also cause metals to redeposit on the substrate.

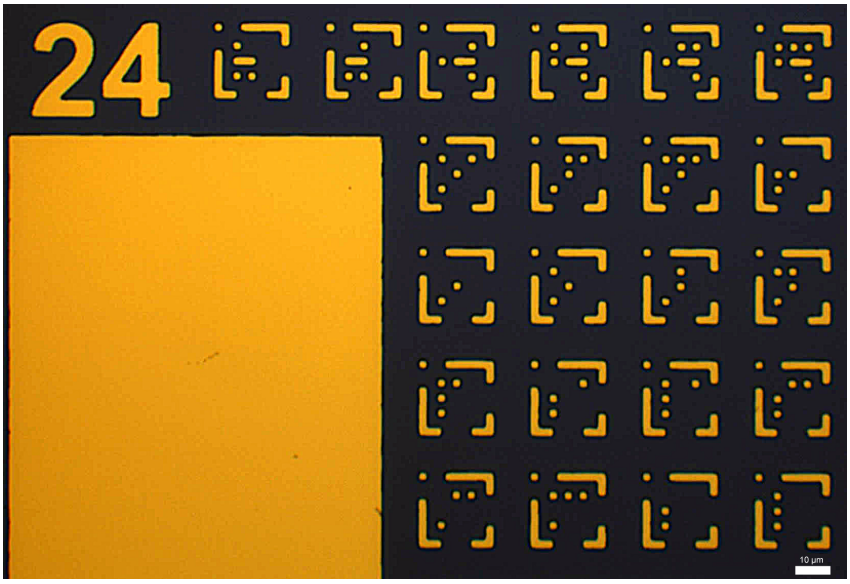

Figure 2–8: **Patterns after lift-off ("AFM-friendly" mask, part).** The golden part is the metal pattern while the dark part is the substrate. The resolution is $\sim 2.0\ \mu$m, slightly smaller than after the development. Scale bar is $10\ \mu$m.

Two problems often happen during lift-off process. First, sometimes there may be unwanted parts that do not lift during the process, and some may even remain during strong sonication ("retention"). A major reason for this is that the resist does not dissolve properly. In such cases, a bilayer resist setup (see *Sec.2.3.3*) may help, but its benefit is limited – if the metal

is way too thick or if the metal has adhered very well, it would still prevent lift-off. Therefore, for a resist of a given thickness, there may also be a limit for the thickness of metal that can be successfully lifted-off. Second, lifted metal can be reattached to the substrate ("redeposition"). This can be reduced by circulating and filtering the solvent during lift-off.

After lift-off, a standard cleaning process is always necessary. The substrate is soaked in acetone and IPA for at least 30 s respectively, then rinsed in deionized water and dried with nitrogen gas.

2.1.7 Dicing

The substrate then proceeds to dicing. Before dicing, coating the substrate with a thin layer of resist on the front side is preferred in order to protect the patterns and the substrate from silicon dust created by the dicing saw. Blades of the dicing saw usually have various thicknesses for different needs. As the blade has a thickness, cutting through a substrate will consume part of the substrate – this needs to be taken into consideration when designing the mask. To consume the least silicon of the substrate, the blade should be reasonably thin (a blade too thin might break during cutting). Here a blade with the thickness of $100\ \mu$m is used, making the cutting trace $\sim 250\ \mu$m.

After installing the proper blade, the substrate is attached to some tape which will hold the substrate tightly during dicing and prevent any relative movement that can damage the substrate or the blade. It is then placed at the center of the chuck and held in place by vacuum. Next, the space between two pattern units (left specially for dicing) on the substrate should be aligned with the blade, with the help of a charge-coupled device (CCD). After alignment, it is necessary to walk through the substrate and check with

a CCD to ensure that the blade will cut straight lines as wanted. Various parameters must be set before cutting, of which an important one is the chuck-to-blade distance. Note that cutting too deep may immediately separate the substrate and disarrange the alignment made before, while cutting too shallow will make it hard to divide the substrate afterwards. Therefore, a good blade-to-chuck distance must be chosen in order to prevent the blade cutting too deep or too shallow. In this work, the blade-to-chuck thickness is set to be 200 nm but it may also depend on wafer types. After dicing the substrate, it is then possible to divide the substrate into uniform chips.

After dicing, the diced chips must also be cleaned using *cleaning process II* introduced in *Sec.2.1.2*, to get rid of the previous coated resist and possible silicon dusts introduced while dicing. In addition to this, the chips must be cleaned using the same process before usage (e.g. before nanowire transfer introduced below), to wash away dust that falls on them during storage.

2.2 Nanowire transfer

Usually nanowires are grown vertically on substrates, in the morphology of a forest or grass. To make good use of these nanowires, transferring them to another substrate or chip (e.g. previously made pre-patterned chips) is necessary. Nanowire transfer can determine the position of nanowires and the amount that can be used. Mainly, there are two kinds of method to do this: the scratch method and the sonication method.

2.2.1 Scratch method

The scratch method is a dry, brute-force way to transfer nanowires. By putting the pre-patterned chip and nanowire-grown substrate in proximity

and scratching the pre-patterned chip through the nanowire substrate gently, a large amount of nanowires can be transferred to the chip (Fig.2-9). By checking under optical microscope, the amount of nanowires can be roughly estimated. The same process can be repeated until the desirable amount is reached. It is necessary to keep scratching the substrate in the same direction, so that nanowires have the same orientation and don't overlap with each other. A cotton-tip can also be used to scratch the nanowire substrate first and then transfer nanowires to a pre-patterned chip, however it may bring fibres and dust which is bad for later processing.

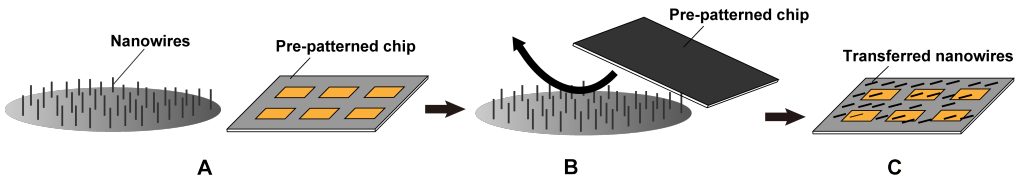

Figure 2–9: **Scratch method. A.** Preparing a nanowire-grown substrate and a clean pre-patterned chip. **B.** Scratching the chip on a desired region of the substrate gently. **C.** The nanowires are transferred to the chip with the same orientation.

The nanowire density is difficult to control with the scratch method since it requires experience and a proper applied force on the chip. Besides, sometimes nanowires are not grown uniformly on the substrate, and so having to choose a good part to scratch makes this method tricky. In addition to this, scratching the surface of the substrate can damage the patterns on the chip which may create difficulties for subsequent processes.

2.2.2 Sonication method

Compared to the scratch method, the sonication method is more gentle. The desired parts from the nanowire-grown substrate are first cut off and put into a centrifuge-tube filled with solvent. The tube is then put in a sonication bath and the nanowires are transferred into solution so that they become a "nanowire solution". By using a single-channel micro-pipette (measurement range: $2\ \mu\text{L} \sim 20\ \mu\text{L}$), the nanowire solution can be transferred from the centrifuge tube to pre-patterned chips. A hot-plate (with a temperature set at around 80℃- 90℃) can be used to accelerate the solvent evaporation.

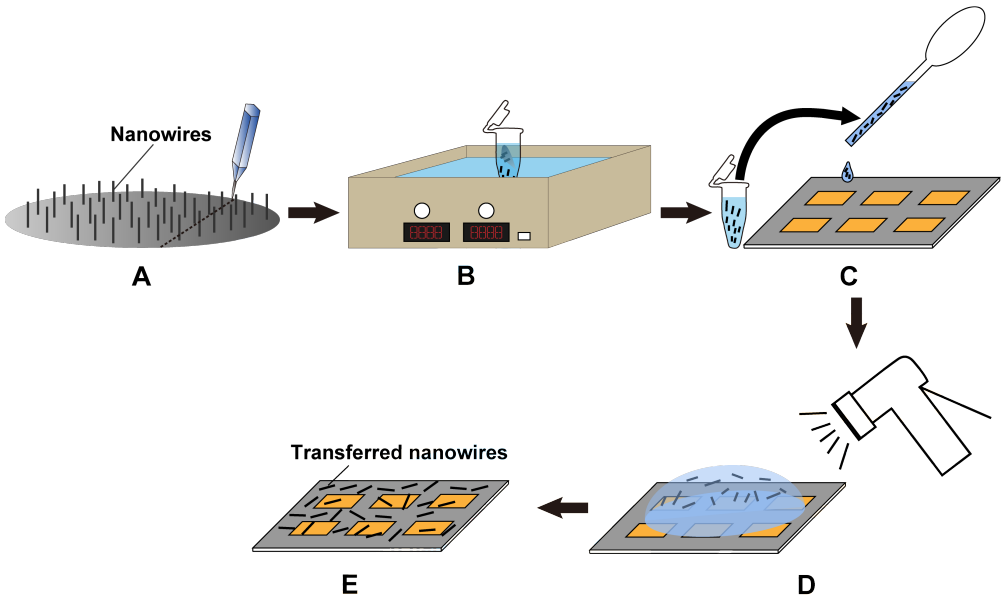

Figure 2–10: **Sonication method. A.** Cut "desired" part off from the nanowire-grown substrate. **B.** The cut substrate is placed into a centrifuge-tube and sonication is used to dissolve nanowires. **C.** The "nanowire solution" is deposited on a pre-patterned chip with a pipette. **D.** The chip is dried with nitrogen gas gently to ensure that nanowires are distributed evenly and will not form too many clusters. A hotplate can also be used to accelerate the evaporation. **E.** The nanowires are transferred to the chip with different orientations.

When the liquid is almost gone, a nitrogen gun is used to blow away the incoming dust from the air and prevents the nanowires from forming rings as the liquid dries.

Regarding the solvents, deionized water and IPA were used: deionized water evaporates slowly and usually leaves many clusters, whereas IPA evaporates faster but is not as pure as deionized water. Nevertheless, both solvents leave residue after evaporation sometimes.

The method has three major advantages. First, it does not cause damage to the patterns on the chip since it will not need to scratch the surface of the chip. Second, the nanowire density can be well-controlled by repeating the same process. Although the scratch method can also be repeated, the damage to the surface it may cause makes repeating the process difficult. Third, the quality of transferred nanowires can be well controlled by selecting only good parts on the nanowire-grown substrate. This can be done in two ways: cutting the good parts off using a diamond, or scraping the nanowires off with a clean razor and putting them into a centrifuge-tube. The latter technique, however, may break the wires and should not be used.

In spite of the advantages it has, this method has a major drawback in that clusters form during the drying process very often. Therefore, area close to clusters can not be used, as clusters make resist thickness non-uniform, and development and lift-off difficult. Moreover, the method leaves solvent residue which is not desired. Since nanowires are "dust-like", solvent residue is inevitable, but using purer solvent can reduce the amount of residue.

2.3 Nanowire device fabrication: electron-beam lithography

Once the nanowires are transferred to the pre-patterned chips, electron-beam lithography (EBL) is used to fabricate the nanowire devices. EBL is one of the possible ways of overcoming the diffraction limit of light and can reach an ultimate resolution of tens of nanometers. Thus, it is one of the most powerful method to fabricate devices at the nano-scale.

2.3.1 Nanowire locating

Even by cutting only the good part on the nanowire-grown substrate, the quality may still vary from wire to wire. Therefore, after transfer, it is necessary to choose nanowires with good quality and good location visually and take pictures of them to record their locations. This is done with the SEM to ensure good precision.

The criteria for good quality of the nanowires mainly include two aspects: the diameter and the length. Uniformity of the diameter along the wire is the most straightforward way of judging the quality of the nanowire. Usually, good nanowires are uniform in diameter because they have less defects at the surface and less stacking faults. The tapered ones, on the other hand, will have more stains introduced during growth so the quality is not good and the residual electron density is always high. Also, as it is hard to make a device with a very short nanowire, the nanowire must have a length of at least $\sim 700\text{nm}$.

For location of the nanowires, there are also two criteria. First, the nanowire must not lie on the pre-patterned pads completely (otherwise it will short the nanowire). Second, the nanowires should not lie above other nanowires or too close to a cluster of nanowires.

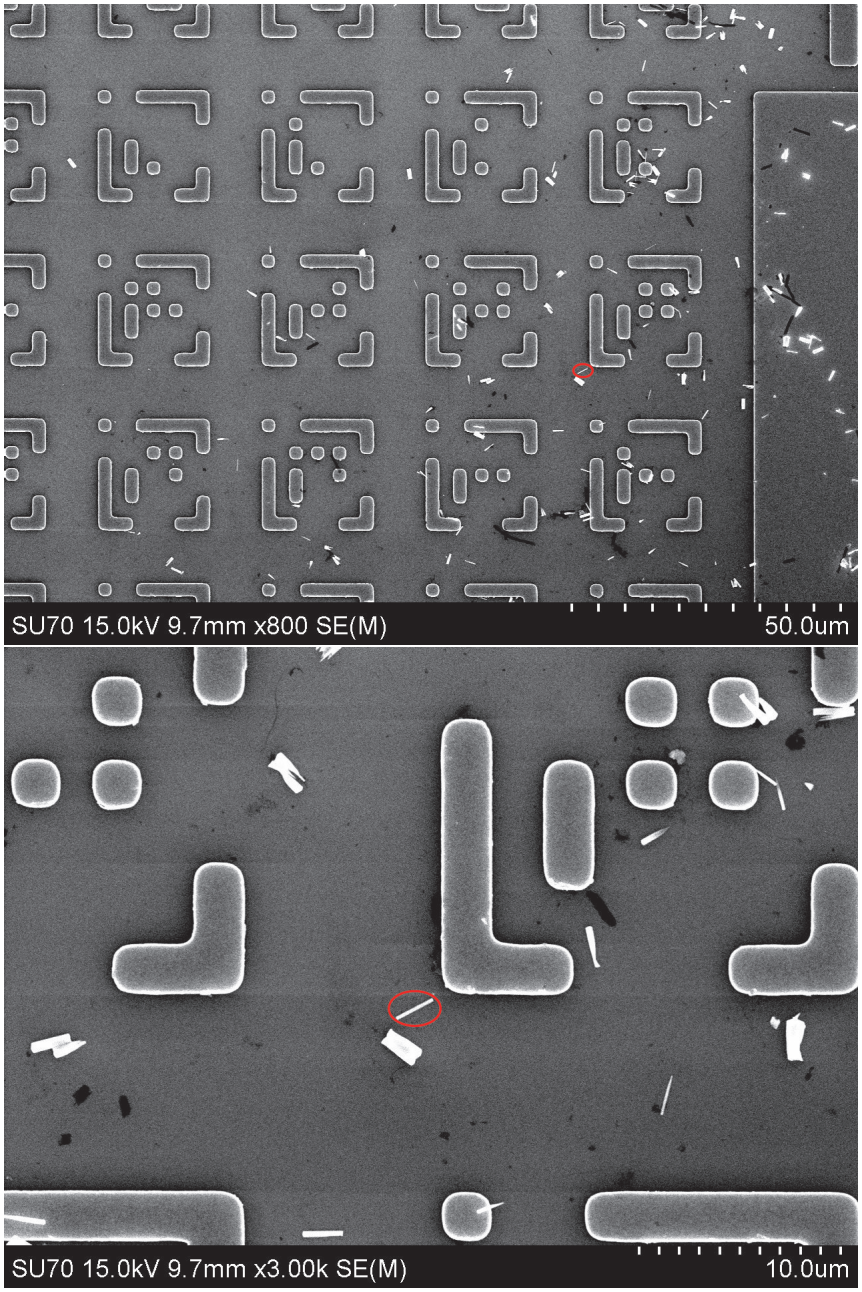

Figure 2–11: **Nanowire pictures. Upper.** Picture-1. The picture shows selected nanowire (circled) and 3×3 complete binary dot arrays with frames, for the purpose of the four-window alignment. Connecting leads to the large pads can be calculated according to the mask. **Lower.** Picture-2. Zoom-in of the selected nanowire (circled) region. Sonication method is used to transfer the nanowires.

In addition to this, for substrates made with the "AFM-friendly" mask, nanowires lying within binary dot frames are sometimes not good since connecting them out could lead to a short. Moreover, for four window alignment method (see *Sec.2.3.4*), the nanowire chosen must sit within the area enclosed by the selected four alignment marks.

When making a nanowire device, only one nanowire should be connected between two large pads since connecting more than one nanowire between two large pads will introduce a parallel circuit. Therefore, even if more than one nanowire is eligible for use when taking the picture, only one of the candidates should be used.

Generally, three different kinds of pictures need to be taken to make one nanowire device. Picture-1 (Fig.2-11 Upper) shows one containing the nanowire and other necessary parts such as the large pads to be connected and alignment marks. This picture shows what the nanowire pattern design is based on and is taken at the same magnification as that of the exposure to ensure precision. If this picture has a relatively low magnification it would become hard to identify the selected nanowire at a later stage. A second picture is also required. Picture-2 (Fig.2-11 Lower) of the nanowire shows a larger magnification and is taken to help identify the nanowire later. Picture-3 (not shown) is the reference point and is optional. Furthermore, as any place seen in the SEM will get exposed when doing EBL, it is always a good habit to first find a reference point relatively far (at least $10\ \mu$m) from the exposure spot, then shut the beam off and move to the spot to expose. This picture should be taken at a relatively large magnification (> 8k) since only a small area will be shown during EBL (in order to not expose too much area during the EBL process).

2.3.2 Pattern design

While EBL does not need a real "mask", it still requires a CAD pattern that works just like a "mask".

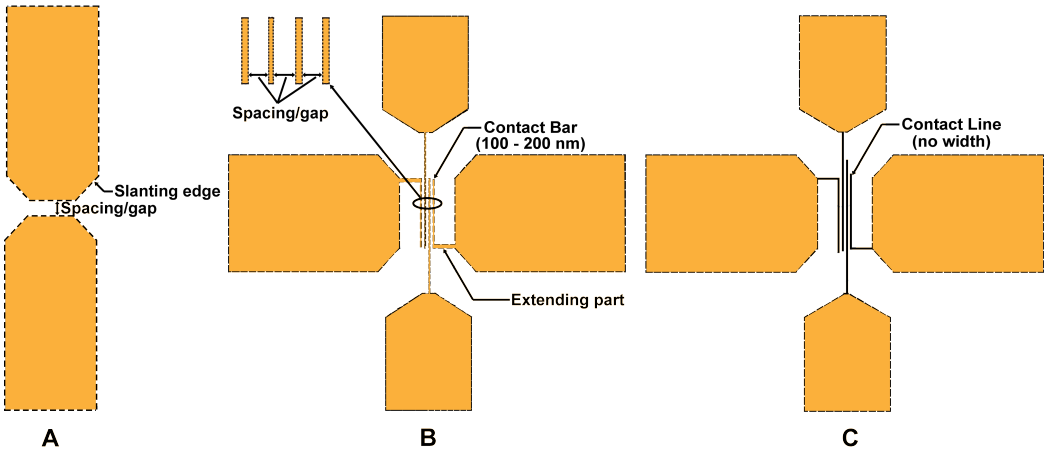

Figure 2–12: **Designed nanowire patterns.** All patterns are enclosed by dashed lines which means the whole area (golden area, hollow in real files) enclosed will be exposed. **A.** Two-terminal nanowire pattern. The spacing/gap used ranges from 200 nm to 1200 nm. **B.** Four-terminal nanowire pattern, initial design. The extending part is designed to reduce the e-beam proximity effect. It has a length of 1 μm, which prevents nanowire (usually 2 μm long at most) from being shorted by contact bars and horizontal pads. The contact bars have uniform widths, from 100 nm to 200 nm and the spacing/gap ranges from 250 nm to 350 nm between each two bars. **C.** Four-terminal nanowire pattern, second design. The contact bars in B are replaced with lines who have no width at all.

In this work, two kinds of nanowire patterns were designed and used. The first one is the two-terminal pads (Fig.2-12A) which turns the nanowire into a two-terminal electronic device. The spacing/gap between two pads ranges from 200 nm to 1200 nm. Note that since two close metal pads essentially form a capacitor when charged, a slanting edge is used in order

to reduce the capacitance. This design is simple and easy to realize, but to get the real resistance of the nanowire, a four-terminal measurement is required. Thus, a four-terminal design was made.

The design of the four-terminal went through two phases. In the beginning, a four-terminal pattern with two narrow bars, which served as the top gate (Fig.2-12B), was used. As these bars are still too thick at the nanoscale, developing the patterns is difficult. This is because they often tend to merge into one another. To overcome this, two straight-lines were eventually used in place of the bars (Fig.2-12C). With proper dose, the two lines can be developed well and reach a final width of around 50 nm to 70 nm.

Once the nanowire locating is achieved, the pictures will be used together with the nanowire pattern to make the whole EBL pattern for each nanowire. A complete EBL pattern includes the nanowire pattern introduced above and customized patterns for each device (since nanowires do not always lie in the same orientation or the same position (Fig.2-13)). When drawing the pattern for one nanowire, Picture-1 is imported first to serve as a template and scaled to the same size as the scale bar indicates. The nanowire chosen can be found with the help of Picture-2. Next, the nanowire pattern needs to be rotated to fit the orientation of the selected nanowire and put at its position in the picture. Then the nanowire pattern is connected to large pads on the picture with customized patterns drawn by CAD. These patterns can be put in same or different layers, depending on exposure needs. After the patterns are well-designed, the template picture is deleted as everything in the final pattern file will be exposed. Then patterns are divided and saved to different files.

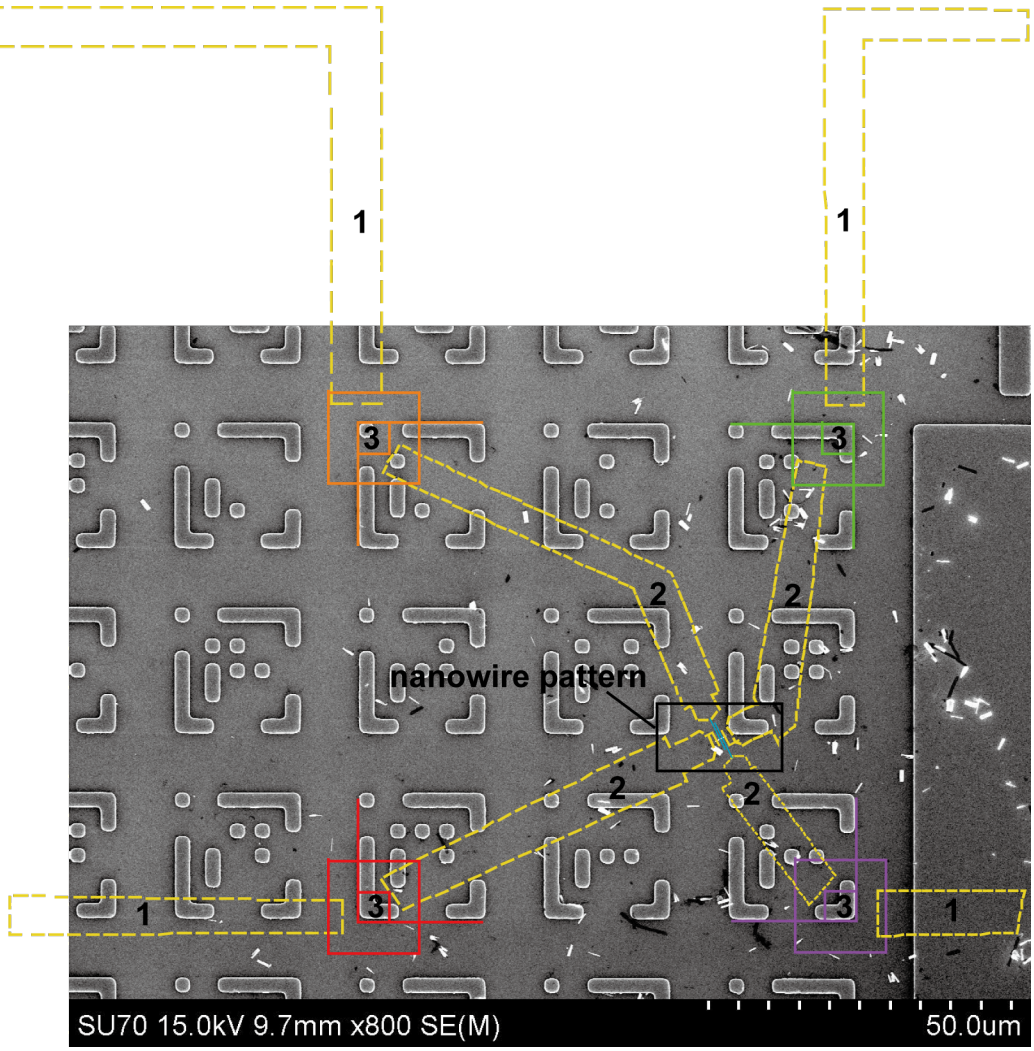

Figure 2–13: **Complete EBL pattern with four window alignment (without Picture-1).** Picture-1 is scaled according to its scale bar (50 μm in the fig.). Four windows (squares and L-shape lines) are aligned with the photolithography patterns (corners of four frames). Customized patterns include patterns both inside and outside the window area. Those within the window area are merged with nanowire pattern to reduce local exposure. Those beyond the window area are drawn with the help of the mask. All area enclosed by dashed lines will be exposed. When saving the pattern files, Picture-1 is deleted and the complete EBL pattern is divided into three files: patterns outside the window area (patterns denoted "1" in the fig.), patterns inside the window area ("2") and alignment windows ("3"). The actual design may vary slightly from this illustration.

For different photo-mask patterns, the design of a complete EBL pattern is different. For the "pads-array" mask, two different pattern files are prepared. One contains the nanowire pattern that makes two or four contacts directly on the nanowire, while the other contains other customized patterns that connects the nanowire patterns to two or four large pads close by.

The two kinds of patterns are drawn in the same CAD file and then save separately, as they need a mutual origin which is usually the center of the nanowire pattern.

For the "AFM-friendly" mask, an extra alignment pattern file is needed, as the four-window alignment technique is used (see *Appendix*). The four-window alignment exposes four square alignment windows before pattern exposure and enables users to use fine alignment lines to align with the alignment marks on the pre-patterned substrates (patterns denoted "3" in Fig.2-13). This alignment corrects all alignment/stage errors and is capable of exposing the whole area enclosed by these four windows accurately, with an accuracy of $\sim 50\text{nm}$. In this work, the alignment marks on the pre-patterned substrates are the edges of the binary-dot frames. The alignment windows and the fine alignment lines are also drawn with CAD. Similarly, Picture-1 is imported and scaled. Then the four alignment windows together with the fine alignment lines are placed at four corners to match the alignment marks in the picture; with the help of Picture-2, the selected nanowire is located, and the nanowire patterns are placed. Connecting the nanowire pattern to large pads are different here – the nanowire pattern is first connected to two or four of the windows, since the whole area within these windows can be exposed together, and then the windows are connected to the large pads. As a result, three different pattern files are generated: the

alignment file, patterns within the window area, and patterns beyond the window area.

2.3.3 Resist coating: single layer vs. double layer

Similar to photo-resists, there are many kinds of EBL resists. The most common ones are the 950PMMA A series and MMA Copolymer resists. Since chips used are very small (usually 4 mm by 5 mm), a larger spinning speed is needed to get a uniform distribution of the resist. Normally, a speed of 4000 rpm to 5000 rpm for 45 s is sufficient (see Fig. 2-12). For soft-baking, a temperature from 150℃ to 180℃ is suitable, and the baking time ranges from 60 s to 90 s.

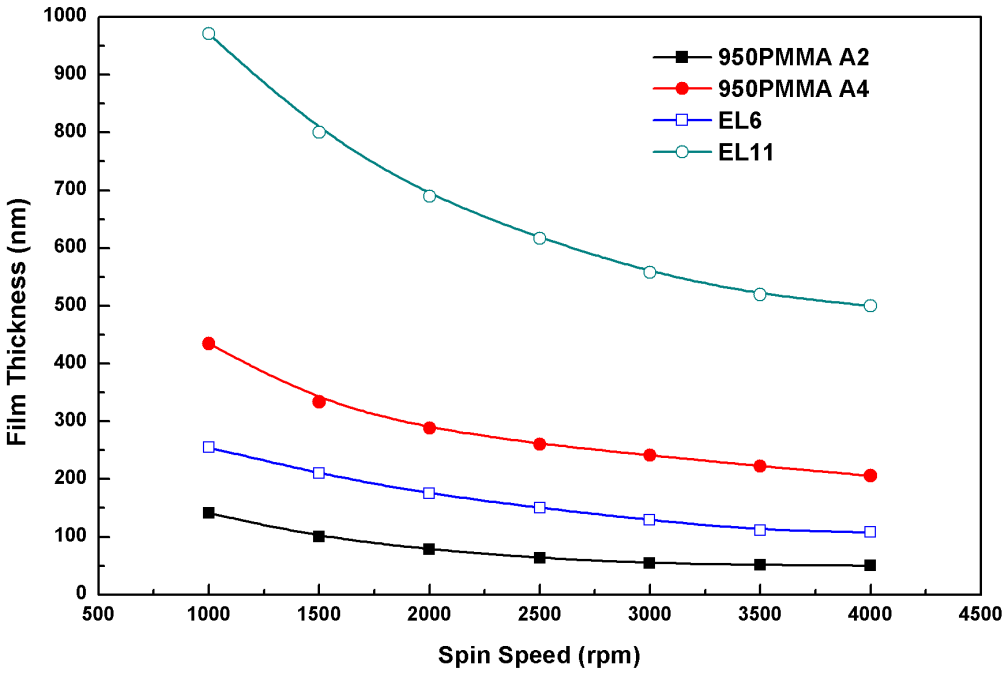

Figure 2–14: **Film thicknesses versus spin speed for 950PMMA A and MMA Copolymer resists.** Note the actual thickness may vary with resist and/or substrate condition. Figure reproduced from brochure of MICROCHEM® PMMA Data Sheet.

For PMMA A4, spinning the resist at 4000 rpm for 45 s and baking at 150℃ for 60 s gives a thickness of around 250 nm, while for PMMA A2, the same conditions give $\sim$ 60nm and for MMA EL 11, they give $\sim$ 500 nm.

It is generally believed that, to improve the lift-off process, a bilayer resist structure (i.e., two layers of resists) should be used. This is since after development, there may be a so-called undercut in the bottom layer of the bilayer setup (Fig.2-15). The undercut helps lift-off because during metal-deposition, metals will not be able to fill the undercut (Fig.2-15D), and thus the etchant will be able to penetrate into the space and etch out the resist easily. However, it has been found in this work that under certain conditions, a single layer of resist is already good enough to provide very successful lift-off and can even be better than the bilayer setup.

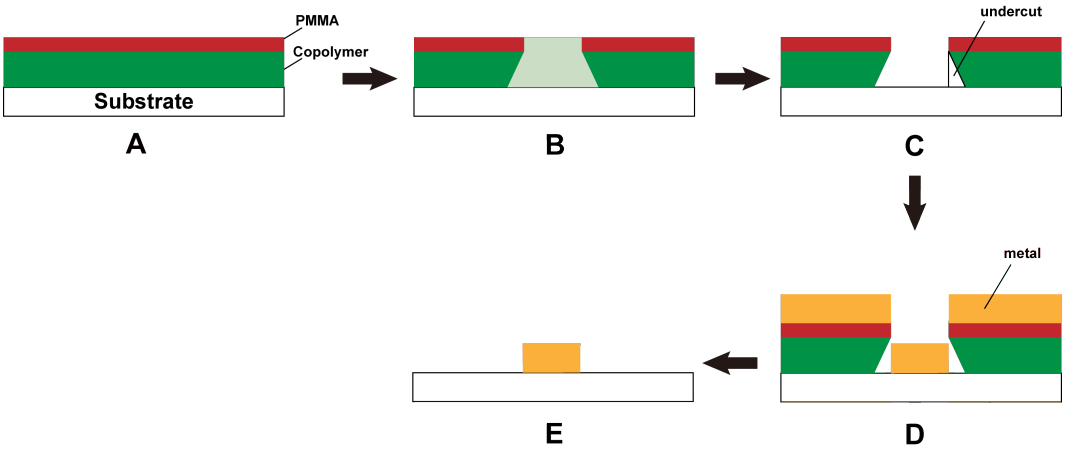

Figure 2–15: **Lift-off of bilayer resist. A.** A copolymer resist is coated before PMMA. **B.** As copolymer is more sensitive to electron beam, a larger portion will be exposed. **C.** After development, an undercut will form. **D.** When depositing the metal, there will be space left between the metal stack and the bottom copolymer. **E.** The metal should be lifted nicely.

The quality of the later lift-off process indeed depends on the surface of the substrate and the thickness of the metal stack (Tab.2-3). If the surface of the substrate is clean and has fewer patterns tending to keep the metals, single layer PMMA A4 is better than the bilayer setup since it is easier to handle and more stable. With the "pads-array" mask, PMMA A4 is able to reach a resolution of around 80 nm and can have a successful lift-off process with a thickness of 400 nm of metal. However, it does not work well with "AFM-friendly" mask, since there are too many metal dots that tend to hold the resist and metal, and only 120 nm of metal can be successfully lifted under the same conditions.

Table 2–3: **Coating parameters used and successful lift-off metal thicknesses reached in this work.**

No.	Resist type	Mask type	Spin speed & duration	Bake temp. & duration	Metal lifted
1	PMMA A4	pads-array	3000 rpm, 45s	180℃, 60s	255 nm
2	PMMA A4	pads-array	3000 rpm, 45s	150℃, 60s	480 nm
3	PMMA A4	AFM-friendly	3000 rpm, 45s	150℃, 60s	120 nm
4	EL6 & PMMA A2	AFM-friendly	4000 rpm, 45s (both)	150℃, 60s (both)	150 nm
5	EL11 & PMMA A2	AFM-friendly	4000 rpm, 45s (both)	150℃, 60s (both)	250 nm

On the other hand, by using a bilayer setup with the bottom layer more sensitive than the top one, an undercut shows up after development which makes the lift-off process easier. Normally, MMA EL series, which is more sensitive than PMMA A series, serves as the bottom layer and a dilute PMMA such as A2 serves as the top layer. The reason to use A2 as a

top layer is that A2 can have finer definition of lines under exposure and can give an overall resolution of around 60 nm, roughly the same as PMMA A4 single layer. Spinning MMA EL11 and PMMA A2 successively at 4000 rpm for 45 s and baking at 150℃ for 60 s gives a total thickness of 560 nm or so. A main drawback of this bilayer setup is that it is more difficult to control all parameters to obtain the desired resist thickness and surface flatness. Besides, it is hard to see the features needed for EBL clearly under SEM since the bilayer setup is thicker and the two resists have different diffraction coefficient. Tests with bilayer setup showed that the lift-off is not always clean in that the edges of the EBL pattern are sometimes not sharp whereas for PMMA A4 the edges are always very good for successful lift-off processes. An alternative for PMMA A4 single layer is the MMA EL6 with PMMA A2 bilayer setup whose thickness is comparable to A4 when spun at 4000 rpm for 45 s. Such a setup can do lift-off with a metal stack slightly thicker than that for A4 (~ 150 nm) but the edges are not always sharp either.

Both single layer and bilayer resists have retention and redeposition problems. However, in the case of a bilayer setup, the retention problem is less severe and the lift-off is definitely easier compared to that for a single layer setup with the same parameters.

2.3.4 Run-file edit and exposure

Prior to doing exposure, a run file that specifies EBL operations and exposure parameters is prepared. The operations mainly involve stage movement, magnification switch, and exposure. Stage movement dictates how much to move along the horizontal and/or vertical axes of the stage. It can move to a desired spot if the stage correction is done (introduced below).

The magnification switch can tell the SEM to switch to a specified magnification automatically. The exposure is composed of alignment, exposure parameters (dose type, line-to-line spacing, etc.) and the exposure method (whole pattern, fracture of the pattern, or array of the pattern).

The exposure is done with the EBL system. The EBL system used is converted from a SEM, so most of its operations are similar to the SEM with some slight differences. A higher acceleration voltage than for usual SEM imaging is required for EBL ranging from 20 kV to 30 kV. The larger the acceleration voltage, the higher the energy carried by the electrons and the smaller the beam. So in principle, a higher acceleration voltage gives a better resolution. For a resolution of around 80 nm, the desired resolution for this work, an acceleration voltage of 20 kV is sufficient. Prior to doing the exposure, several other operations are done. First, astigmatism adjustment and alignment adjustment of the SEM must be performed. A single nanowire is usually chosen as the object for astigmatism and alignment. The chosen nanowire should be located far (at least $10\ \mu\mathrm{m}$) from the exposure field where the nanowire device will be made, so as to avoid exposing the nanowire device, and should not be in the nanowire clusters where nanowires overlap each other to avoid having a wrong focus. The nanowires can still be clearly identified when covered by a single layer PMMA, whereas they can be difficult to observe clearly when covered by a bilayer EBL resist. Thus, adjusting the astigmatism and alignment with bilayer resist can be tricky. In this case, one can choose a binary dot which is larger and thus easier to see, as a starting point.

Second, a stage correction must be performed. When loading a sample, the axis on the sample can be different from that of the SEM system in both angles and units. The two axes are matched by doing an image rotation

and then the stage-axis is fixed to the sample axis by correcting the stage-rotation and stage-movement. In addition, focus on the chip may vary from place to place since the thickness of the resist and the substrate usually varies slightly, so a focus correction is sometimes necessary. There are two ways to achieve this. The first one is to correct stage-movement and focus once by calculating the rotation matrix and correcting the focus manually. But since this method takes control of the stage directly while it has a systematic movement error that cannot be avoided, it is not highly precise. If carefully done, this can limit the stage-movement error to 300 nm, which is still large compared to the average nanowire lengths of $1\ \mu$m. It is nevertheless simple: prior to doing the exposure, we can control the stage directly and align the stage-axes with three points on the substrate (usually three edges of the large pad) that form two perpendicular axes, and so the system will then be able to calculate a rotation matrix that corrects the stage-axes. When doing the exposure, the stage is first moved to the reference spot and after aligning to the reference spot, the stage can be moved to the target nanowire and the exposure is done. The second method is based on the first one, but in addition to calculating the rotation matrix, a more accurate stage-movement correction is done with the four-window alignment. Compared to the first one, the four-window alignment has the advantage that the correction is done *in situ* so the stage does not move after alignment and its systematic error can be avoided. By opening four windows, aligning to the alignment marks and calculating the correction, the stage-movement error can be reduced to the level of tens of nm.

For the exposure parameters, three parameters are critical: dose, center-to-center distance and line spacing. There are two kinds of dose: area dose and line dose. Area dose is used when a whole area is exposed while line

dose is used mostly for lines. The center-to-center distance is the distance of adjacent exposure points while line spacing indicates the distance of adjacent beam passed. Area dose is affected by both center-to-center distance and line spacing while line dose is only affected by center-to-center distance. Normally, the center-to-center distance and line spacing should be set $\frac{1}{4}$ to $\frac{1}{2}$ of the desired line-width of the pattern. Then the dose can be acquired by performing a dose test in which multiple doses are tested to obtain the optimal one.

Table 2–4: **Exposure, development parameters used and resolution achieved in this work*.**

No.	Resist type	Dose	Beam current	Development duration	Resolution
1	PMMA A4	1.60 nC/cm	140 pA	70 s - 90 s	250 nm
2	PMMA A4	240 nC/cm^2	140 pA	90 s - 100 s	800 nm
3	PMMA A4	300 nC/cm^2	135 pA	50 s - 55 s	200 nm
4	EL6 & PMMA A2	1.7 nC/cm, 140 nC/cm^2	16 pA	30 s - 40 s	80 nm
5	EL11 & PMMA A2	1.9 nC/cm, 140 nC/cm^2	17 pA	60 s - 70 s	80 nm

$*$ No. of the recipe corresponds to those of Table 2-3. The developing duration as well as resolution vary slightly from case to case. All parameters will depend on wafer type, mask type and condition of the EBL system (e.g. beam current listed above).

Doses vary for PMMA A2, PMMA A4 single layer and bilayer resist. For PMMA A4 spun at 4000 rpm for 45 s and baked at 150℃, the line dose is around 1.7 nC/cm and area dose around 120 nC/cm^2. For the EL11 and PMMA A2 setup, if both spun at 4000 rpm for 45 s, the line dose is around 1.9 nC/cm and the area dose around 140 nC/cm^2, while for the EL6 and

PMMA A2 setup the values are smaller (see Tab.2-4). This will also depend on the feature spacing, since e-beam proximity effect might occur if the feature spacing is too small, in which case, reducing the proper dose may be necessary.

2.3.5 Development

The EBL resists are developed by a mixture of one part MIBK and three parts IPA. For PMMA A4, normally a developing time of 60 s to 90 s is enough depending on the spinning speed and time. For the bilayer setup of PMMA A2 with EL6, a developing time of 40 s is usually good, whereas for the bilayer of PMMA A2 with EL11, 60 s is also enough (see Tab.2-4). Since spin-coating and baking vary slightly from time to time, it is always necessary to use an average developing time first, check the developing result with an optical microscope, and then continue developing with a non-aggressive time step (such as 5 s) if the sample is under-developed.

Another type of developer for the EBL resist is the IPA-water mixture with nine parts IPA and one part DI water. It is believed to be more delicate, but it is also very slow. Normally, a sample which can be fully developed in MIBK-IPA for 30 s needs 2 min to be fully developed in IPA-water. As it is not used in this work, the author will not discuss further this method.

2.3.6 Oxide removal

On the surface of InN, a thin layer of indium oxide may grow, preventing the metals and InN from forming an ohmic contact. So it is very important to remove the oxide before metal deposition.

Prior to the oxide removal, one optional step, the so-called descumming, can be done to remove resist residue in the developed patterns that should be gone after development. By using oxygen plasma at a power of 60 W for

10 to 15 s, the residue is removed. Since oxygen plasma basically burns resist into ash isotropically, the whole resist layer will get thinner and some delicate patterns may also get destroyed. Thus, it should be done with accurate time control and great care.

There are two ways of removing the indium oxide. A simple way is to use diluted 3% HCl. By soaking the developed InN nanowires in HCl for 15 s to 20 s, the oxide can be removed. The sample can then be rinsed in DI water for another 30 s to 60 s and dried in nitrogen gas. Note that since a mixture of IPA and water can develop the resist, IPA should never be used during this process. As the chip will be exposed to air after the treatment, the nanowires will continue to get oxidized. So it is important that the chip be put into the evaporation chamber (and so under vacuum) as quickly as possible.

A more sophisticated way is to use customized ammonium polysulfide ($(NH_4)_2S_x$). This solution has the advantage in that it not only removes the oxide layer, but also passivates the surface such that the treated surface will not get oxidized very fast. To make this solution, the commercial ammonium sulfide (usually 40%, stock concentration) is first diluted to 20%. Then 4.5 M of sulfur powder is added to the solution. The solution should then be stirred and heated at 40℃ for around 20 min until most of the sulfur powder is dissolved. The final stock concentration of the $(NH_4)_2S_x$ is 0.5% - 1%. Soaking the developed InN nanowires in the solution for 30 min will remove the oxide and form a passivated surface. However, the passivation has a limited effect, so if the sample is exposed in the air for a relatively long time, the nanowires will still get oxidized. As a result, the chip should be put into the evaporation chamber right after this treatment. In addition, it is noted

that $(NH_4)_2S_x$ can also etch the resist, so the sample should not be put in the solution for more than 30 minutes.

2.3.7 Lift-off

After oxide removal, the sample is put in the evaporation chamber for metal deposition. To make a Josephson junction, aluminium, which goes to a superconducting state at $\sim$ 1.1 K, is deposited with titanium deposited first as an adhesive layer. Normal metals such as gold are also used for comparison purposes. The thickness of the metal stack is approximately the same thickness as the diameter of the nanowire.

After metal deposition, the chips are taken to do the lift-off. Remover PG is used and heated at 70℃ without sonication, as sonication can break the thin metal layer covering the nanowire or at least loosen the binding between metal and nanowire, resulting in bad electrical contacts. Normally, a lift-off time of half an hour is enough, but it can be longer depending on the thickness of the metal deposited and the thickness of the resist: a thicker metal stack might sometimes require longer time to strip the unwanted part off, whereas a thicker resist makes lift-off easier and so it requires less time.

For bilayer resist, lift-off is usually easier, but it is within a certain range. If the thickness of the metal stack exceeds a certain limit, it will also be difficult to have a good lift-off. For example, for the EL6 and PMMA A2 bilayer setup with a total thickness of around 250 nm made on "AFM friendly" chips (both spun at 4000 rpm for 45 s and baked at 150℃ for 60 s), a metal thickness of 210 nm would make lift-off difficult.

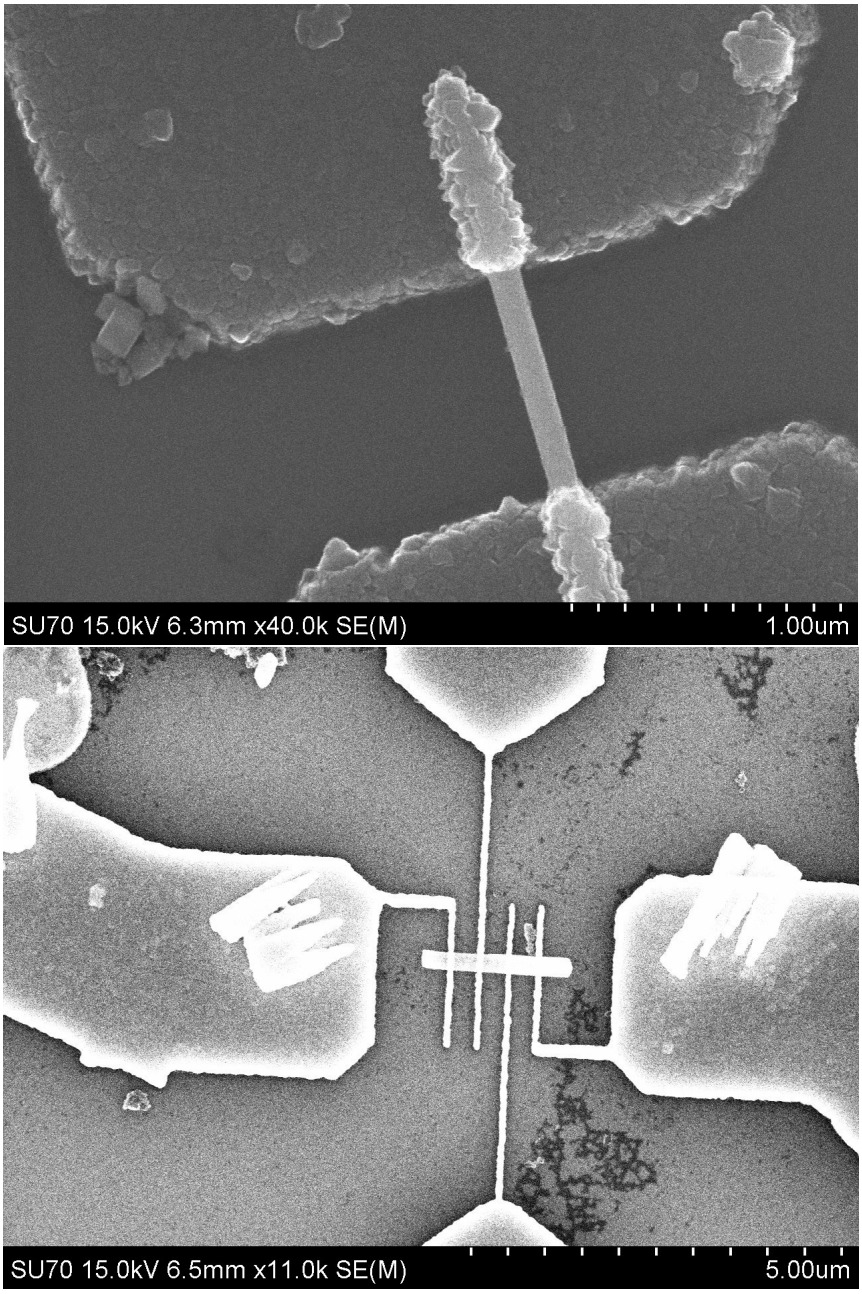

Figure 2–16: **Fabricated devices after lift-off. Upper.** Two-terminal device with a spacing/gap of 800 nm. Metal thickness is 210 nm. **Lower.** Four-terminal device using contact-line design (see Fig. 2-12C). The spacing/gap is 400 nm while the thickness of the line is 80 nm. The metal thickness is 210 nm.

As the chips are very small and sonication cannot be used, a disposable pipette can be used to create bubbles which help lift the metals. One concern is that these bubbles might also damage the sample, so alternatively, one can always scratch at the edge of a chip to help the solvent dissolve the resist, put the chip into a Remover PG filled beaker and create a gentle liquid flow using a magnetic stir bar. In this case, by controlling the stirring speed, one can lift the metals off gently, albeit occasionally still with retention or redeposition problems.

2.3.8 Packaging

After lift-off, the fabrication process is over (Fig.2-16). The devices can then be packaged. The packaging process has two steps.

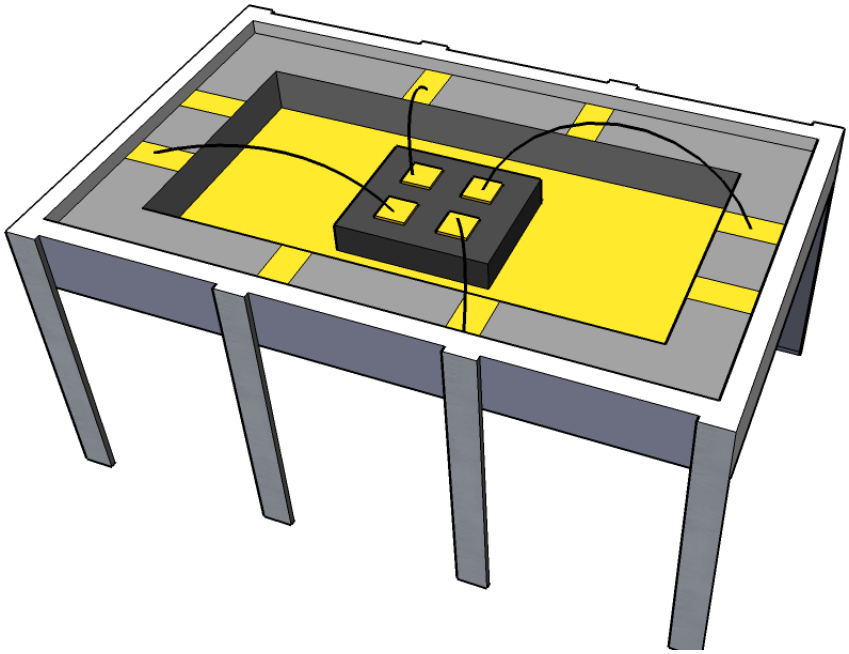

Figure 2–17: **Wire-bonding.** The wire-bonder bonds contact pads from the chips with metal pads along sides of DIPs which are connected to the pins.

First, the chips are attached to the DIP socket with epoxy. If a back-gate is needed, the conductive silver epoxy can be used; otherwise black epoxy can be used. The epoxy can usually be cured at 80℃ for 2 hours. Second, devices on the chip are connected to the metal pads of the DIP by a wire-bonder. The wire-bonder works in a way similar to a soldering iron except that it uses sonication, pressure and heat to make a weld. Wires used are either aluminium wires or gold wires, with the diameter of $40\ \mu$m. With this done, a complete InN hybrid nanowire device package is made.

2.3.9 Annealing

After the initial measurement, the robustness of a nanowire device can be roughly judged from its resistance. If the resistance is too high, a possible reason is that the metal attachment is not good enough. In this case, an annealing process can be done: the chip is first placed on a home-made metal stage and put into a test-tube carefully. Then the test-tube is pumped until the pressure is less than 1e-6 torr. Finally the test-tube is put in an oven and heated at 250℃ for 15 min to 30 min. After taking it out, the sample must be kept in the test-tube until it has cooled down to protect devices from active reaction with oxygen.

Annealing of the sample has limited effect on a very bad contact. This is because in this case, very likely indium oxide is present, thus preventing the metal and InN nanowire from forming an ohmic contact (this cannot be solved by annealing).

CHAPTER 3
Measurements

3.1 Introduction

The measurements are made with the packaged devices: after packaging, the chip is mounted to a female DIP, which is attached to an insert that can be dipped in a dewar and is compatible with the helium-3 system as well as with a dilution refrigerator. Each pin of the female DIP can be further connected to one BNC connector on a break-out box, and electrical measurements can be performed with the wanted pins.

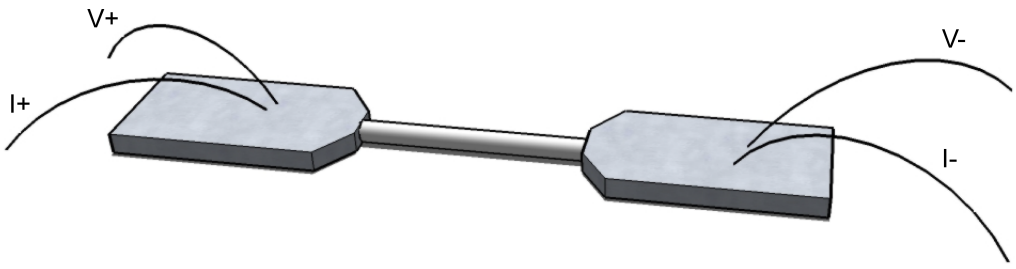

Figure 3–1: **Pseudo four-terminal method.** Two wires are connected out from each of the two-terminal pads, serving as V+, V-, I+ and I-. Both wires and pads are made of aluminium, which goes to superconducting at approximately 1 K.

The measurements include resistance as a function of temperature (R-T behavior), resistance as a function of magnetic field (R-B behavior), and current as a function of voltage (I-V curve). The sample used is a two-terminal device, but measured in a pseudo four-terminal method in which

two leads are attached to each contact of the device and the four leads served as current in/out and voltage in/out (Fig.3-1).

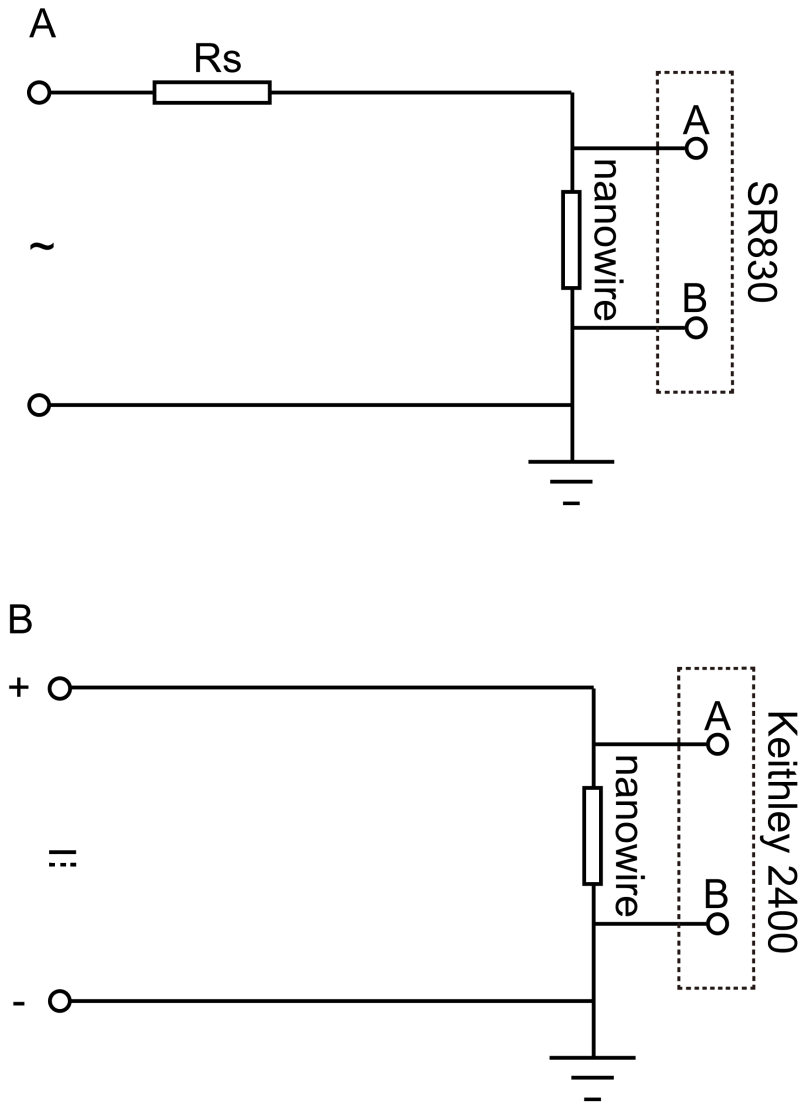

Figure 3–2: **Diagram of measurement. A.** Electrical diagram of AC measurement set-up. **B.** Electrical diagram of DC measurement set-up.

Two types of measuring methods were used. The first one is an alternating current (AC) method (Fig.3-2 A). A lock-in (model: SR830) is used to

generate a small AC signal and measure the resistance of the device. A resistor (Rs) with very large resistance (~ 1 MΩ) is used to ensure a small current such that the nanowire device does not get destroyed by noise and/or Joule heating. The second one is the direct current (DC) method (Fig.3-2 B). A source-meter is applied to give a DC signal and measure the DC resistance.

3.2 R-T behavior

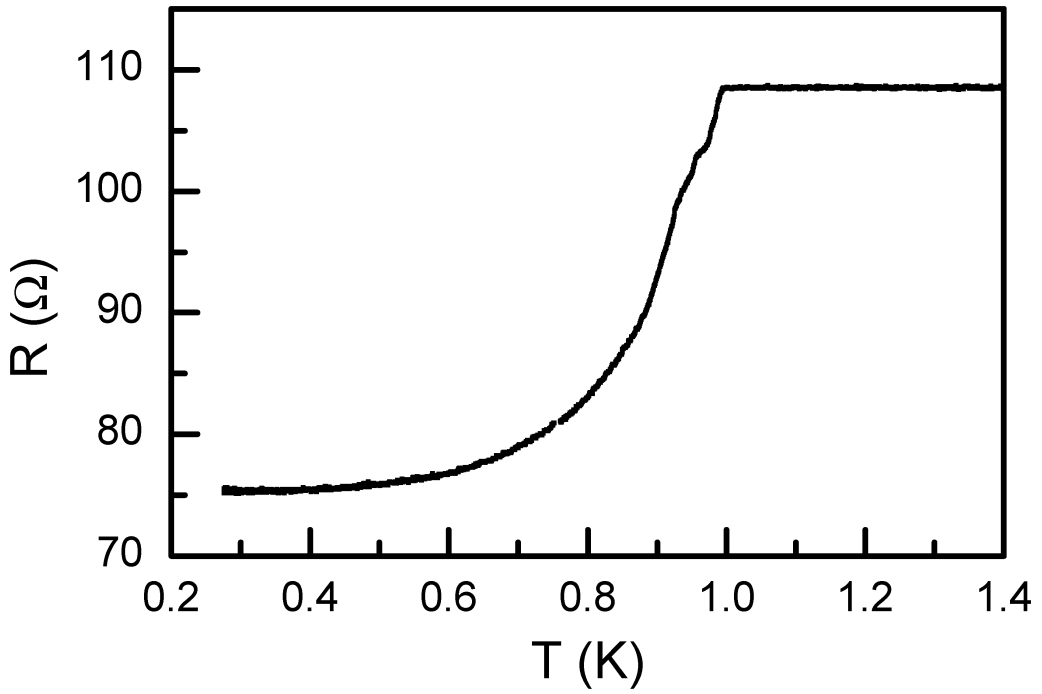

Figure 3–3: **Resistance as a function of temperature.** Superconductor (aluminium) critical temperature is Tc = 1 K. The measurement is performed using a pseudo four-terminal method.

Figure 3-3 shows the R-T behavior of the sample. It can be seen that resistance of the sample went through a phase transition at 1 K, which is very

close to the known superconducting critical temperature of bulk aluminium (1.1 K). Above 1 K, the resistance is almost flat (due to the small temperature range). At the lowest temperatures, T $\approx$ 0.3K, the zero-bias resistance of the sample is $\sim$ 75 Ω. This is roughly one order smaller than that measured by Frielinghaus *et al*[41] . On the other hand, below 1 K, aluminium leads (both aluminium wires and deposited aluminium) go to superconducting states and their resistance is almost zero. Under these conditions, the resistance which decreases as the temperature decreases can only be from that of the nanowire.

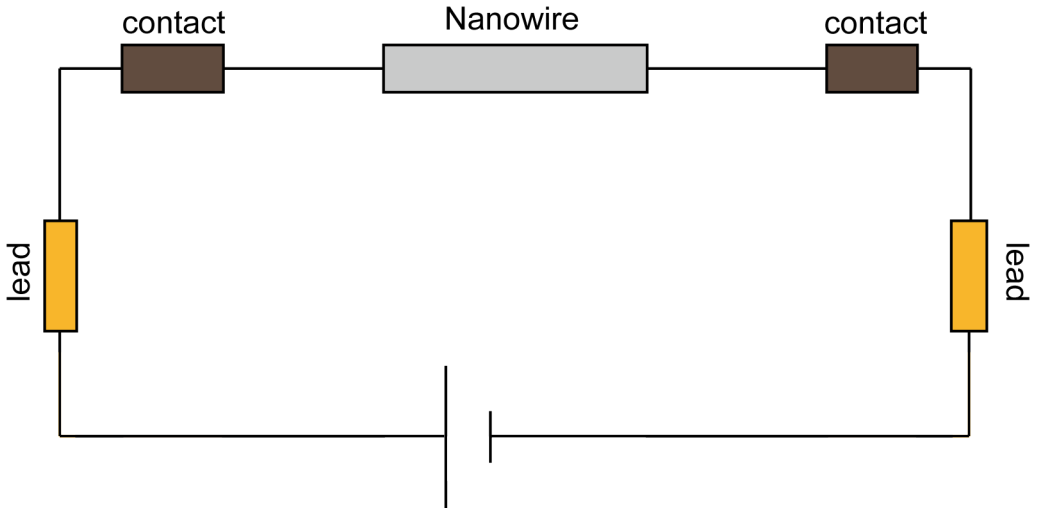

Figure 3–4: **Electrical diagram of a two-terminal nanowire device.** Total resistance includes that of the nanowire, as well as those from the leads and contacts. Resistance of the aluminium leads goes to zero below 1 K whereas that of the contacts cannot be eliminated.

The resistance of the nanowire, according to the superconducting proximity effect, should go to zero as the nanowire also goes to weak superconducting states. However, here it decays gradually as temperature decreases and does not reach zero when the resistance saturates. This can

be understood in two aspects. First, a likely reason why it does not reach zero is that there is some remnant contact resistance (Fig.3-4) in series with the nanowire. Second, the resistance of the nanowire may not reach a value below $\sim 75\ \Omega$ owing to impurities, and/or the length of the junction ($\sim 250\text{nm}$).

A large contrasting difference from a normal intrinsic nanowire whose resistance becomes larger as the temperature decreases, is that our device shows a metallic behavior. This might be because of the surface accumulation layer of InN. With the formation of the shell-like accumulation layer, the electrons are actually going through in a very thin shell which is like a two-dimensional electron gas (2DEG). Thus a metallic behavior is expected. This may also explain why the overall resistance of our device is so small compared to those previously reported in the literature[41,42] .

3.3 R-B behavior

The device resistance as a function of magnetic field was measured at various temperatures (Fig.3-5A). It is observed that below the denoted critical field ("Hc"), there is an evident drop in resistance. This is because at this magnetic field the Cooper pairs are broken. The temperature dependence of the critical field was also investigated (Fig.3-5B). For Type I superconductors such as aluminium, the Meissner effect states that as part of the nature of these superconductors, the magnetic field will be excluded if it does not exceed the critical value.

According to BCS theory, the magnetic field, as an order parameter, shares a similar result with that of the superconducting gap near critical temperature, which is

$$\frac{\Delta(T)}{\Delta(0)} \approx 1.74(1-\frac{T}{Tc})^{\frac{1}{2}},\ T \approx Tc. \tag{3.1}$$

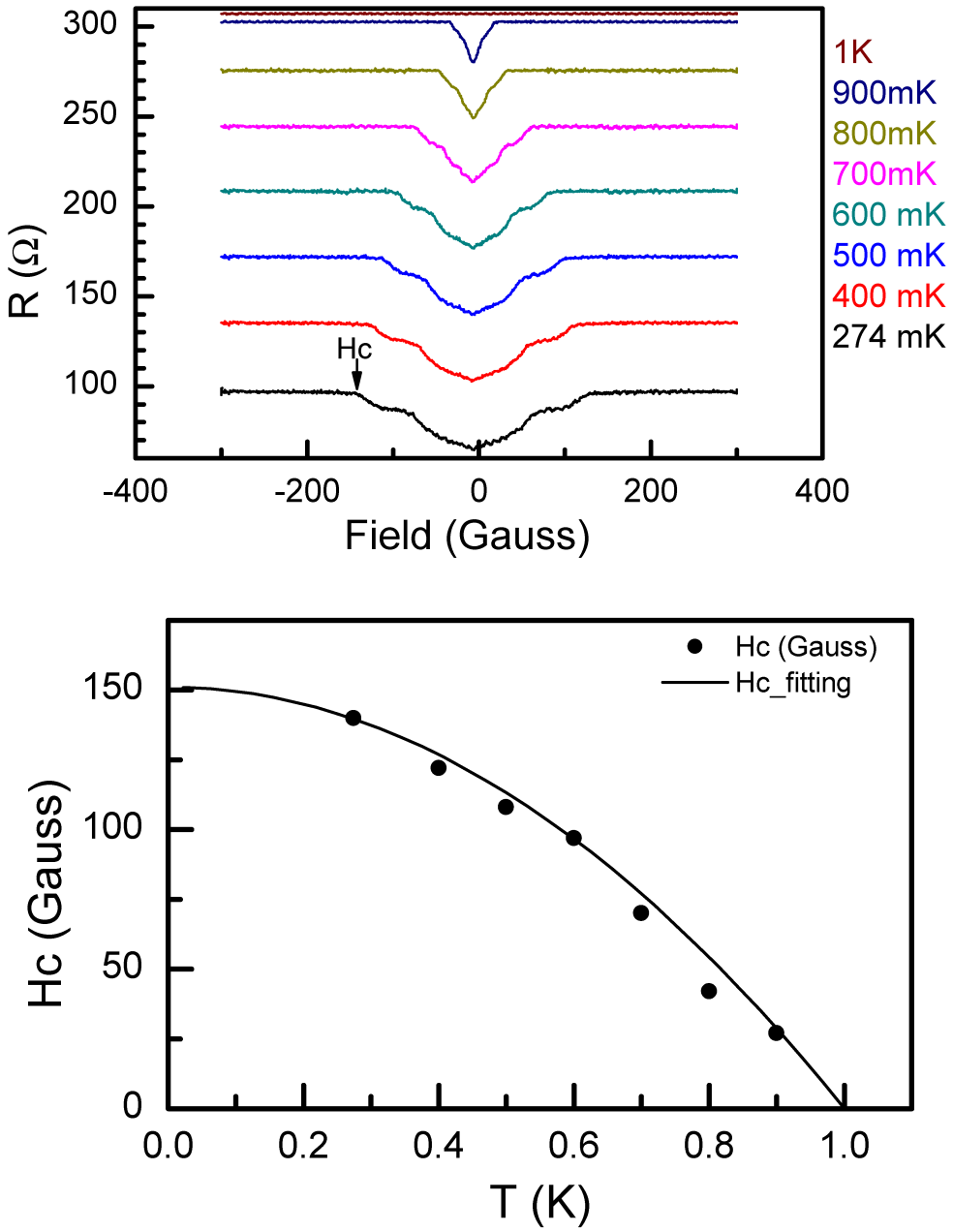

Figure 3–5: **Temperature dependent R-B behavior. A.** Resistance versus magnetic field as a function of temperature. An offset was set for each curve for easy-viewing purposes. Note that the dip of the curve does not sit at zero field, owing to a slight hysteresis in the magnet. **B.** Critical field as a function of temperature. The data are extracted from A. The data are fitted using Eq.3.2.

The critical field at temperature below the critical temperature, by a simple correction[43] and approximation of Eq.3.1, is given by the following formula,

$$\frac{Hc(T)}{Hc(0)} = 1 - (\frac{T}{Tc})^2. \tag{3.2}$$

With this formula, we can fit the data well and we obtain the zero temperature critical field $Hc(0) \equiv Hc(T = 0\ K) = \pm 151$ Gauss.

3.4 I-V curve

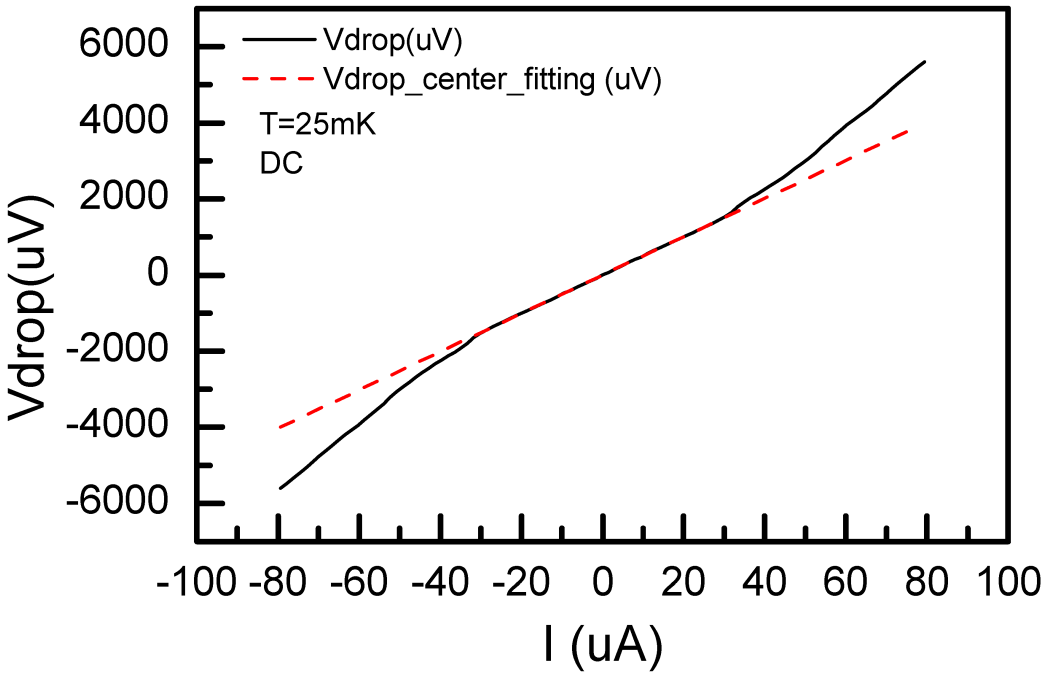

Figure 3–6: **Current as a function of voltage drop.** The measurement is performed at 25 mK using a DC technique. The fit of the curve in the central region at zero bias is indicative of a supercurrent.

To obtain the I-V characteristic of our InN device, a DC current was flowed through the device and measured as a function of voltage drop at 25 mK. A typical ohmic behavior is observed, demonstrating the successful fabrication of ohmic contacts in this device.

Nevertheless, the I-V curve also shows a kink at $\pm 32\ \mu$A (Fig.3-6). We interpret these features as critical supercurrent on the order of $\sim 32\ \mu$A. The central region of the I-V curve (in the superconducting state) is however, not flat owing to the contact resistance which is not superconducting. A further calculation of the slope of the center line fit shows a background resistance of approximately $75\ \Omega$, fully consistent with the previous R-T measurement.

Compared to the literature[41,42] , our supercurrent is two times larger even when dimensions of the nanowire are taken into account. We tentatively propose that this may due to the indium or indium oxide that may go superconducting. These have superconducting gaps reported to be larger than that of aluminium[44–47] . As the supercurrent is related to the superconducting gap, one might therefore expect that a combination of these gaps will lead to a larger supercurrent, as observed in this work.

CHAPTER 4
Conclusion

In this work, various cleanroom techniques were used to fabricate single nanowire hybrid devices. First, two kinds of mask designs were used and compared. The earlier version, a "pads-array" mask, is simple, easy for lift-off, but has several problems such as confusing digit and auxiliary pads design, lack of uniformity in spin-coating, and non-compatibility with AFM. The second version, an "AFM-friendly" mask is more complicated but solves the previous issues by its improved digit and pads design that are better suited for spin-coating. It is also fully compatible with AFM measurements at low temperature.

Second, important aspects of photolithography were investigated in the fabrication of pre-patterned chips. Two different cleaning processes were used to clean substrates according to different needs. Parameters of spin-coating, soft-bake, exposure, development, metal deposition, lift-off and dicing were explored and tweaked, so as to achieve ideal photolithography results.

Third, two kinds of nanowire transfer methods were explored and compared. The scratch method is simple and dry, but can damage patterns on the chips. The resulting nanowire distribution and density is also difficult to control. On the other hand, the sonication method will not damage patterns and can have good control over nanowire distribution and density, but it is wet and creates clusters.

Fourth, the method of fabricating single nanowire devices with EBL was studied. Nanowires were first carefully located and recorded before fabrication. Patterns were designed and customized with the pictures taken. For resist-coating, both single layer and bilayer resists were tried and compared. It was found that single layer resist worked well with "pads-array" whereas bilayer resists can achieve better results, but with limited improvement. All parameters including those of spin-coating, exposure, development, oxide removal, lift-off and annealing were also explored and optimized.

Finally, basic measurements were carried out and preliminary results show that this device has an extraordinarily low resistance (one order lower) compared to those from the previous literature. The device is also becoming a superconductor below 1 K, which is a clear signature of the proximity effect. We have also measured a critical supercurrent larger than what is expected from a Al-InN-Al junction. We speculate that this may be caused by some spurious superconductivity occurring in the InN itself.

Appendix A: Detailed recipe and manual for device fabrication

I. Fabrication of pre-patterned chips

- *1. Back oxide removal and wafer cleaning*
- Before spin-coating, turn on the hotplate and tune to the desired temperature as it will need some time to heat up. For the temperature, usually 115℃ is appropriate for Shipley series.
- Pre-bake the wafer at 115℃ for 3-5 min.
- Attach the substrate to the spin-coater and drip sufficient photo-resist (Shipley 1813 or any photo-resist) onto the substrate with a disposable pipette. When dripping the resist, it is important to spread it so that an even distribution is achieved after spinning. Spin the front side of the wafer at 4000 rpm for 45 s; a pre-spin with a speed of 500 rpm for 15 s is helpful for spreading the resist.
- Soft-bake the wafer at 115℃ for 1 min.
- (Optional) It is safer to attach a blue-tape (which can be dissolved in acetone) to the front side and clean the resist residue carefully on the backside (if any) by using a cotton tip soaked in acetone.
- Put the wafer into HF solution (buffered oxide etchant recommended, or simply the water diluted HF) for 5-10 min until the backside turns grey. This may vary from wafer to wafer, but the removal of oxide can be visually judged, as the silicon oxide is shiny.
- Rinse the wafer in water bath first and then clean the wafer with acetone, IPA and water for roughly 60 s, respectively (see *cleaning process II, sec. 2.1.2*). Dry the wafer with nitrogen gas.

- Normally, the organic residue can be removed using the piranha solution, and the metal ions, using the RCA-2 process (see *cleaning process I, sec. 2.1.2*). Dry the wafer with nitrogen gas.
- (Optional) The four-inch or larger wafer can be cut into quarters first, to make full use of it (since the mask is 3-inch in this case).
- *2. Spin-coating and soft-bake*
- Pre-bake the wafer at 115℃ for 3-5 min.
- Coat the wafer with Shipley 1805 (or Shipley 1813, depending on the desired resolution), at a spinning speed of 4000 rpm for 45 s (The spinning speed can actually vary from 1000 rpm to 5000 rpm, depending on desired thickness, but usually 4000 rpm is a good starting point.).
- Soft-bake the wafer at 115℃ for 1 min. Cautions are the same as for previous spin-coating.
- (Optional) Wipe out the resist on the edge with acetone.
- *3. Exposure and development*
- Before exposure, specify the recipe: resist thickness, substrate thickness and mask thickness should be measured. Dose is often around $60\ \mathrm{mJ/cm^2}$ for Shipley 1813 and $30\ \mathrm{mJ/cm^2}$ for Shipley 1805. Put the mask holder and the mask itself in position and expose the wafer following the instructions.
- After exposure, develop the substrate with MF-319. Both MF-319 and DI water should be prepared in dishes with larger diameter than the substrate for easy-handling purposes. Developing time is shorter for substrates that are not pre-baked (around 5 s to 10 s). Typically, developing time is 20 s for Shipley 1813 and 15 s for Shipley 1805, but it will depend on resist conditions. When developing, sway the container or the substrate in order to have the developer etch the resist uniformly.

The result can be judged visually: a well developed pattern will have a fine edge and show a color close to that of the substrate or much shallower than that of the resist.

- Rinse the wafer in DI water immediately. Note that the developer residue will continue etching the resist. It is necessary to take this duration into account during the developing process and gently sway the wafer in enough water to wash away the developer evenly. The rinsing duration is typically 30 s. The substrate is then dried with nitrogen gas. The backside of the wafer should also be dried.
- *4. Metal deposition and lift-off*
- For lift-off purposes, e-beam evaporation should be used. Before deposition, it is advised to make sure there is enough metal in the crucible and the crucible is at right position. Attach the substrate to the stage, close the evaporation chamber and pump it to near-vacuum. The lower the pressure, the purer the material, but normally 4 e-6 to 5 e-6 torr is sufficient. When doing the evaporation, it is necessary to ensure that the stage is rotating and the electron beam hits the center of the crucible.
- Put the substrate in acetone or Remover PG for lift-off. Acetone is fast but rough while PG Remover is slow but delicate. Heating the solution helps lift-off, but acetone cannot be heated higher than 57℃. Normally, half an hour should be enough for the lift-off. When stripping the unwanted metal, a pipette can be used to create bubbles. Mild sonication can also be used and is much faster than the pipette but has problem of redeposition and may damage fine patterns. After lift-off, *cleaning process II* should be used.
- *5. Dicing*

- Before doing dicing, spin a thin layer of photo-resist on the front side of the substrate, to protect the patterns from silicon dust. Soft-bake must also be done.
- Change the dicing blade to a silicon blade with the desired thickness (100 μm for this work).
- Size of a single pattern unit in the design should be measured, such that the moving distance of the blade can be specified. Chuck-to-blade thickness should be set according to the type of the substrate, 200 μm is a typical value. Other parameters can be kept at default values (dice blade rpm, feed rate, etc.).
- Attach a blue-tape (which can be dissolved in acetone) to the chuck and put the chuck under vacuum. Attach the substrate tightly to the tape (the substrate should not move on the tape) and align with the blade with the help of the CCD. It is very important to go through all the cutting lines before actual cutting, and adjust the blade so that it cuts straight through the space between patterns.
- After dicing, detach the blue-tape using acetone. Chips can be separated and then cleaned using *cleaning process II*.

II. Nanowire transfer: sonication method

- Select a good part of the nanowires grown on the substrate. Normally nanowires in dark regions have small diameters and are short while those in grey regions and colorful region have large diameters and are long. Therefore, the grey regions between dark and colorful regions are chosen. Cut this part off with a diamond.
- Put it in a centrifuge-tube filled with DI water, seal the tube and place it in a small beaker (25 mL) with some water so that it can be put in the

sonication machine. Apply mild sonication to detach nanowires from the substrate and mix them evenly with the solvent.

- Turn on the hotplate and heat it up to 80℃. The hotplate can help DI water evaporate and prevent nanowire clusters.
- Clean the chip first and put it on the hotplate.
- Use a micro-pipette to deposit a drop of nanowire solution around 15 μL in size, which should just cover the chip nicely.
- When the solution is almost dry, apply gentle nitrogen gas to prevent the drop of nanowires from forming nanowire clusters at the boundary of the drop.
- The result can be judged from the microscope, by checking nanowire distribution (typically small black lines, like bacteria seen from the optical microscope). If the distribution is not ideal, it can be improved by repeating the previous two steps, until a satisfying distribution is reached.

III. Nanowire device fabrication

- Locate usable nanowires: take SEM pictures to record the positions and orientations of the nanowire(s). Take Picture-1 under the magnification of 800 which includes an area containing four alignment marks (usually 3×3 binary dot arrays) and the selected nanowire(s) for patterning. Take Picture-2, an enlarged picture of the selected nanowire(s), usually under magnifications between 2.5k to 4k. Take Picture-3 (optional), an enlarged picture of the reference point, usually under magnifications between 4k and 18k. In addition, the selected nanowire must be uniform in diameter and have a length of at least 700 nm.

- Draw a customized pattern for patterning the selected nanowire. First, scale Picture-1 to fit its scale bar. Then put the nanowire pattern on the selected nanowire, rotate and move it so that the gap is parallel to the nanowire and in the centre of the nanowire. Third, connect the nanowire pattern to the big pads by customized area patterns. Fourth, divide the finished pattern file into three files, one containing the alignment windows, one containing the small patterns within the area of the windows (mostly nanowire pattern and some customized area patterns), the remainder of the pattern (for fracture pattern mode).
- Next, edit the run-file. First, stage-movement should be measured and specified in the move-only entity. Then for the alignment entity, alignment window should be selected and the pattern file containing the alignment windows should be chosen as a reference. The two other previously divided pattern files are then specified to be exposed in sequence. First, the small patterns are exposed, as a pattern entity, and then the large patterns, as a fracture entity (because the file can exceed the maximum exposure field). For the dose, use $\sim 1.9\ \mathrm{nC/cm}$ for line dose and $\sim 270\ \mathrm{nC/cm^2}$ for area dose. Accurate dose must be acquired through a dose-test.
- When doing the exposure, it is recommended that a rough adjustment of the microscope be first done before ramping up the voltage to 20 kV. After ramping up the voltage, do the astigmatism and alignment adjustment. The image should be very clear after all adjustments. After this, measure the beam current and specify it in the run-file. Then, the direct stage control, which corrects the stage-movement roughly, should be done.

- Move the stage to the reference point and run the run-file. Follow the instructions from the screen and wait till the exposure is fully done.
- After exposure, develop the sample in either 3:1 mixture of IPA and MIBK or 9:1 mixture of IPA and water. For IPA - MIBK mixture, the developing time is roughly 45 s to 90 s. Accurate developing duration must also be acquired from real test and can vary slightly from sample to sample. Then dry the sample with nitrogen gas (gently).
- Prior to metal deposition, the oxide on the nanowire must be etched away. Vent the chamber of the evaporator to 1 atm and keep flowing nitrogen so that the sample will be protected from oxygen after etching.
- (Optional) Perform a descumming by putting the sample in oxygen plasma at a power of 60 W for 10 s.
- Put the sample in the diluted HCl (3%) for 15 s to 20 s to get rid of the oxide. Then wash the sample with DI water and dry it with nitrogen gas (use the nitrogen gun gently).
- Attach the sample to the stage of the evaporator and pump down the chamber. Deposit first titanium and then aluminium. The thickness for titanium is usually 10 nm while that for aluminium may depend on the diameter of the nanowire (roughly the same as the diameter of the nanowire). Cautions are the same as for previous metal-deposition.
- Put the sample into a beaker filled with PG remover, seal the beaker and heat the solution at 60 - 70℃ for 30 min. Use a disposable pipette to create bubbles to lift-off the unwanted metal part.
- Clean the sample using *clean process II* and dry with nitrogen gas.

Appendix B: Four-window alignment method

- First, when drawing the EBL pattern, a four-window alignment layer must be drawn. A single window of these four windows contains a dashed square indicating the whole area which will be exposed, and a solid fold line (having a 90 degree angle) which is used to align with the selected alignment marks of the photolithography patterns (usually corners of the frames of the binary dot arrays). The four windows must be drawn in four different layers and the origin of the whole pattern must set as the center of these alignment windows.
- Second, after the pattern file is drawn, the run-file is specified. Before the actual exposure, an alignment entity is required in the run-file. The alignment entity is preceded by a move-only entity. Any movement must be done before the alignment or after the exposure. In the alignment entity, manual alignment mode is selected and once the alignment pattern file is specified, the software will recognize each alignment window according to their layers. Exposure magnifications of the four windows is typically 800, which is the same as that for the whole pattern, while center-to-center distance and line spacing can be large (usually 50 nm each). An important option in the alignment entity is the counts. It must be at least 20.
- Next, when doing the exposure, the stage is first aligned with the reference point and moved to the exposure spot with the beam shut off. Then the four-window alignment is executed as specified in the run-file. Four window areas will be scanned and shown on the screen. If the direct stage control has been properly done, these areas should be

almost identical as the areas covered by the four windows in the pattern file. It is good practice to switch the scan mode to single scan by pressing "S". At the beginning only one window is shown and the displayed pattern might not be clear. This can be resolved by pressing "a" to do the contrast average of all four windows. Once the four corners are clearly seen, the fine alignment lines can be adjusted to match them in each window area. Then by pressing "Space", the alignment matrix can be recalculated and the stage alignment will be modified to match the four corners. Usually, this adjustment is done three times to reach a really good alignment. If the direct stage control is not done well, patterns shown in the four-window area might be offset. If the alignment marks lie outside the windows, the fine alignment lines can be first moved towards the direction of alignment marks within each window area, and then the scanning window area can be moved by a recalculation.

- Finally, if the alignment is properly done, the alignment can terminated by pressing "Enter" and the alignment matrix can be saved by pressing "y". The exposure will start immediately afterwards.

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