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Low-Voltage Integrated RF CMOS Modules and Frontends for 5GHz RF Applications

by

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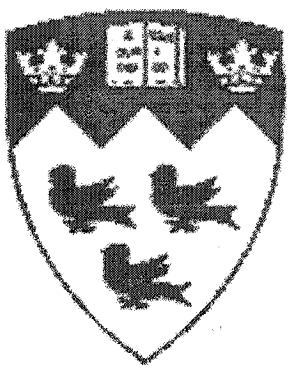

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Abstract

As the demand for wireless communications increases, high speed and low cost electronics are desired. Traditionally, RF circuits are implemented using high performance technologies such as GaAs or SiGe in order to minimize noise and achieve high gain. However, those high performance processes are incompatible with mainstream digital circuitry, which are usually implemented in CMOS technologies.

In this thesis, an RF receiver frontend which consists of a differential low noise amplifier, active mixers, passive mixers, and a quadrature voltage-controlled oscillator, for 5 GHz applications are designed and manufactured in a digital CMOS process, in order to demonstrate the RF potential of CMOS processes. We explore the use of simple circuit topologies and common packaging to build CMOS receivers that can operate from 1V supplies and lower, while providing reasonable image rejection without the use of any special image rejection filters. In addition, a high image rejection receiver is explored after designing it based on good and simple frequency planning.

Apart from inductors and capacitors, transformers are very useful passive components in RF applications. For example, transformers can act as on-chip single-ended to differential converters. In this thesis, a comprehensive study of transformer modeling is presented and discussed. A modeling program has been developed, and its accuracy verified through measurements of several transformer prototypes fabricated in a variety of state-of-the-art CMOS technologies. The program allows the generation of compact lumped transformer models to be used in circuit simulation.

Résumé

A cause de l'augumentation de la demande pour la communication sans fil, électronique de vitesse haute et de coût bas sont désirés. Traditionnellement, RF circuits sont réalisés en utilisant des technologies de haut performance telle que GaAs ou SiGe dans le but de reduire le bruit et obtenir le gain haut. Cependant, ces procédés de haut performance sont incompatibles avec le circuitry courant dominant numérique, qui sont habituellementdans réalisés dans technologies CMOS.

Dans cette thèse, un récepteur RF frontend, qui consiste en un amplificateur différentiel de bruit bas, des mixeurs actifs, des mixeurs passifs, et un quadrature voltage -contrôlé oscillateur, pour 5GHz applications sont conçus et sont fabriqués dans un procédé CMOS numériques. Nous explorons l'emploi de circuit simple topologies de circuit simple et emballage commun à bâtir récepteurs CMOS qui peuvent opérer 1V de ravitaillements ou moins, en même temps en fournissant le rejet raisonnable d'image sans l'emploi aucuns filtres spéciaux de rejet d'image. En outre, un récepteur de rejet d'image haut est exploré basé sur une planfication de fréquence qui est bien et simple.

A part des inducteurs et des capaciteurs, les transformateurs sont des composants passifs très utiles dans les applications RF. Par exemple, transformateurs peuvent agir comme sur-puce seul-terminait aux convertisseurs différentiels. Dans cette thèse, une étude compréhensive du modéle de transformateur est présentée et discutée. Un modéle de programme a été développé et son exactitude est vérifié par des mesures de plusieurs

prototypes de transformateur fabriqués dans une variété d'état technologies CMOS. Le programme permet la génération de modèles de transformateur compacte à être employés dans la simulation de circuit.

Acknowledgments

This thesis is dedicated to my grandmother who taught me multiplication table when I was three years old, and also to my grandfather who always reminds me that I should always strive to excel. Without them, the door to my scientific mind would have not be opened and I shall treasure everything that they gave me for the rest of my life.

I need to thank my supervisor, Prof. El-Gamal, for giving me the opportunity to study RF at McGill, and his guidance during this research. I also need to thank Ahmed and Ramez for their help. Without them, my life in McGill would have been a lot harder.

I wish to acknowledge the Canadian Microelectronics Corporation (CMC) for technology and equipment access, and Quebec's Government FCAR award for financial support.

I also need to thank my girlfriend, Sandy, for helping me to rediscover the lovely world outside the lab. Last but not least, my deepest appreciation to my parents and my sister, Kit Yue. No matter what happens to me, they are always my perfect fans.

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Chapter 1: Introduction

1.1 Introduction

With the explosion of the demand for wireless communications such as cellular phones, wireless local area networks etc., new frequency bands are needed in order to accommodate an increasing number of users and transmission speeds. In Europe, the standards for the HIPERLAN (High Performance Radio LAN) system, which operates in the 5.15-5.35/5.47-5.725 GHz frequency range, have been defined. Similar standards have also been defined in the United Staes.

Traditionally, radio-frequency (RF) transceiver frontends were implemented using Gallium Arsenide or bipolar technologies, since they had higher unity-gain frequencies and better transconductances than other technologies such as CMOS. On the other hand, CMOS processes are the choice for implementing the baseband sections of transceivers, since they offer low cost and low power consumption. As a result, it is highly desirable to be able to integrate both the frontend circuitry and the baseband sections onto a single chip.

As the feature sizes of CMOS technologies shrink, the unity-gain frequencies of CMOS transistors is improving. For example, in a 0.1 μm technology, the unity-gain

frequency of a MOS device can reach up to 100GHz under a 1V supply [1]. However, CMOS processes still suffer from the limitation of low transconductance values when compared to other processes. The primary objective of this work is to demonstrate the feasibility of using a CMOS process in realizing modern RF receiver frontends.

1.2 Motivation

A typical integrated RF receiver frontend consists of three main building blocks (Fig. 1.1 - 1.3), independent of the architecture:

1. A low-noise amplifier (LNA): It amplifies the incoming RF signal.
2. Mixers: Downconvert the high frequency RF signal to a lower frequency band.
3. A voltage-controlled oscillator (VCO): It provides a reference signal for the downconversion process.The output of the VCO needs to be tunable by an external voltage source.

Depending on the architecture chosen, surface acoustic wave (SAW) filters may be needed as off-chip components.

1.2.1 State-of-the-art RF receiver frontends

Table 1.1 summarizes the specifications of recently reported RF transceiver frontends operating in the 5-GHz range [2]-[9]. The table shows a trend in shifting from traditional technologies, such as SiGe and BiCMOS, to CMOS technologies for higher integration. Besides, all the transceivers operate from supply voltages at or above 1.8V. In order to have a single voltage supply for the entire transceiver chip, it is highly desirable for the

	[2] ISSCC'02	[3] JSSC '01	[4] ISSCC '01	[5] JSSC '00	[6] JSSC '00	[7] TMT '00	[8] JSSC '99	[9] CICC '99
Technology	CMOS 0.25 µm	CMOS 0.25 µm	CMOS 0.24 µm	CMOS 0.25 µm	Bipolar	SiGe HBT	BiCMOS	SiGe
Center Frequency	5.2 GHz	5.2 GHz	5 GHz	5.25 GHz	5-6 GHz	5 GHz	5 GHz	5.2 GHz
Noise Figure	8 dB	6.4 dB	7.2 dB	3 dB	5.1 dB	5.9 dB	7 dB	7.5 dB
Forward Gain	36 dB (with baseband ampl.)	43 dB (with baseband ampl.)	26 dB (with baseband ampl.)	8.7 dB	17 dB	19 dB	18 dB	11.7 dB
Output Third-Order Intercept	-	-15 dBm	-7 dBm	-11.3 dBm	-4.5 dBm	-	-17dBm	-11 dBm
Voltage Supply	2.5 V	2.5 V	1.8 V	3 V	2.34 V	3.5 V	3 V	3.3 V
Power Dissipation	250 mW	29 mW	58.8 mW	114 mW	55 mW	45 mW	55.5 mW	122 mW
Packaging	64-pin LPCC	-	32-pin ceramic flat pack	On-wafer probing	32-pin ceramic flat pack	On-wafer probing	On-wafer probing	On-wafer probing

Table 1.1: Comparison of recent RF transceiver frontends.

RF section to operate from the same voltage supply as the baseband circuitry. The latter has its voltage supply constantly dropping. For example, most recent digital circuits implemented in CMOS 0.1 µm technologies operate from 1V supplies.

There exists three main RF receiver architectures:

1. **The superheterodyne receiver (Fig. 1.1)**: Many of the RF transceivers manufactured

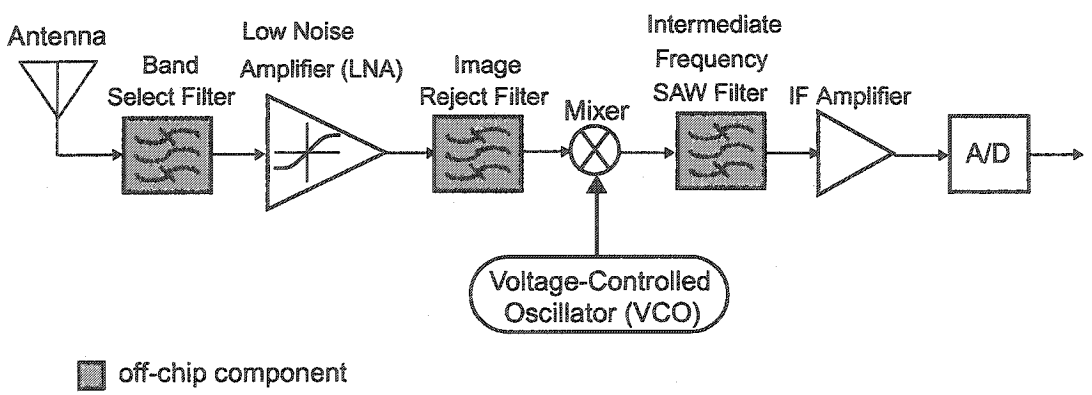


Fig. 1.1: Simplified conventional superheterodyne receiver frontend.

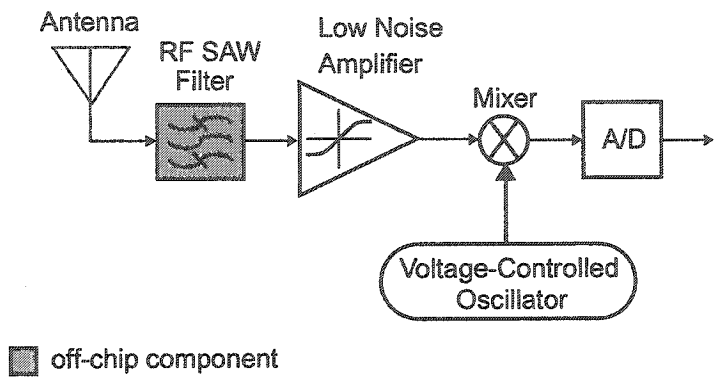


Fig. 1.2: Simplified direct conversion receiver frontend.

to date employ the superheterodyne architecture. This approach offers high selectivity and better image rejection. However, it requires off-chip high quality SAW filters for filtering the image of the RF signal. As a result, this architecture is not suitable for high levels of integration.

2. **The direct conversion receiver (Fig. 1.2)**: It is a well-known architecture that does not require off-chip high quality filters, since the output is directly converted to base-band using a single mixer stage. As a result, this approach has the potential for higher levels of integration. However, this architecture suffers from DC offsets. The LO signal is at the same frequency as the RF carrier, and any LO leakage to the mixer's RF inputs or to the antenna will result in self-mixing, producing a time-varying DC offset at the mixer output, which is difficult to separate from the baseband signal.
3. **The two-IF receiver (Fig. 1.3)**: It is a relatively new topology, which is similar to the superheterodyne architecture. It consists of downconverting the RF signal to an intermediate frequency (IF). The IF signal is then translated directly to baseband via a second mixer stage. Because of the non-zero IF after the first mixer stage, the image

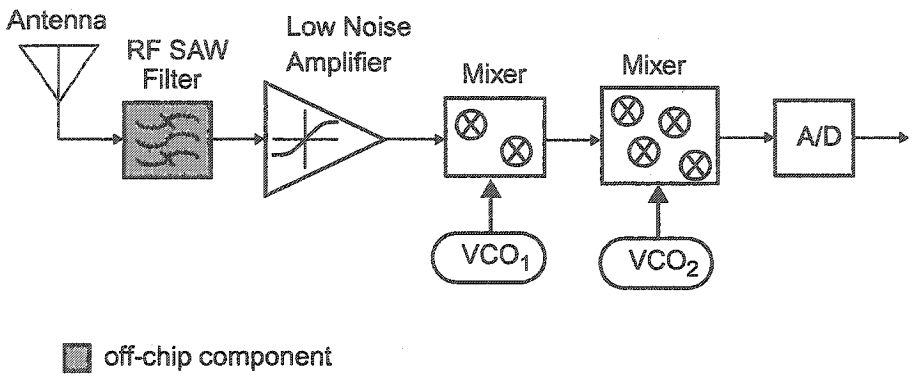


Fig. 1.3: Simplified two-IF architecture receiver frontend.

problem is introduced. Instead of using an off-chip filter as in the case of a superheterodyne architecture, the image problem is mitigated by using a second mixer stage to implement image-rejection through a special structure such as the Weaver structure [18], in order to allow high integration. However, the amount of image rejection is very sensitive to any mismatches in the signal paths.

One of the objectives of this thesis is to demonstrate the feasibility of using a CMOS process to implement a fully packaged integrated very low voltage RF receiver frontend at 5 GHz, and to explore alternate receiver architectures, such as the two-IF approach. A detailed analysis of the two architectures will be covered in Chapter 2. Simulation and measurement results of two receiver prototypes will be presented in chapter 3.

1.2.2 Integrated transformers

Passive devices, such as inductors and capacitors, are widely used in RF circuits. On the other hand, transformers, which can be used for differential to single-ended signal conversion [27], etc., are not as widely used. Unlike inductors, for which serveral robust modeling tools such as ASITIC from Berkeley [11], and the McGill Inductor Modeler

Program	Speed	Comments
Maxwell [10]	Very Slow	• EM simulation • Any topology
ASITIC [11]	Fast	• Pseudo-EM simulation • Many topologies
Gemcap [12]	Fast	• Transmission-line modeling • Basic interface • Few topologies
SISP[13]	Fast	• Transmission-line modeling • Many topologies
MIND [14]	Fast	• Transmission-line modeling • Basic structures only

Table 1.2: Comparison of transformer modeling programs.

(MIND) [14] exist, there are not many non-computational intensive and affordable tools available for transformers modeling. Before we can take advantage of using transformers in RF circuits, we need to fully understand their characteristics and be able to accurately model them when integrated on-chip.

Many of the available commercial transformer modeling programs (Table 1.2) employ electro-magnetic (EM) modeling techniques, based on Maxwell's equations. Although this method can provide very accurate results, it requires lenghty simulations. Since the structures of common transformers are pre-defined to a large extent, the generality of the EM technique is not needed. Transmission-line modeling, where each microstrip is modeled by an equivalent RLC circuit, trades-off generality for speed. The second objective of this thesis was to augment the in-house transmission-lines based inductor modeling tool, MIND, to be able to model transformers from measurements and to synthesize transformers from a given set of design specifications. This is discussed in

details in chapter 4.

1.3 Thesis contributions

Following is a summary of the contributions of this thesis:

1. Demonstrated that using folded cascode topologies, CMOS technologies can be used to implement 5GHz RF frontends which can operate from a very low-voltage supplies. This work was reported in:

   A. **Koon Hung Lee and Mourad N. El-Gamal, "A Very Low-Voltage (0.8V) CMOS Receiver Frontend for 5 GHz RF Applications," Proc. IEEE International Symposium on Circuits and Systems (ISCAS'02), pp. 125-128, May 2002.**

   B. **Mourad N. El-Gamal, Koon Hung Lee, and Tommy Tsang, " CMOS Receiver Frontend for 5GHz RF Applications," IEE Proceedings on Circuits, Devices and Systems, pp. 355-362, October 2002.**

2. Designed and tested a 5-6GHz two-IF downconversion architecture receiver, with high image rejection and wide frequency tuning capacbility:

   A. **Koon Hung Lee and Mourad N. El-Gamal, "A 6-7GHz CMOS Receiver Frontend with wide tunning range," submitted for publication, 4 pages, 2003.**

3. Designed and characterized on-chip inductors and transformers for RF applications, and augumented the in-house modelling tool to include transformers modelling. The work on inductor modelling was reported in:

   A. **Ahmed H. Mostafa, Koon Hung Lee, and Mourad N. El-Gamal, "Character-**

ization of CMOSP18 Inductors," Technical Report, Canadian Microelectronics Corporation, January 2001.

Chapter 2: Wireless Receivers Architectures

Over the past decades, thanks to the advances in digital signal processors (DSP) used for signal demodulation, the focus for RF receivers has shifted from high sensitivity to high integration. Complex demodulation schemes can now be implemented in DSP, resulting in an increase in the overall signal quality and bit error rate. As a result, architectures that favor high levels of integration, such as the direct conversion and two-IF architectures, are gaining popularity over the traditional superheterodyne approach which requires off-chip components, namely filters.

This chapter presents the most common receiver performance metrics, and a qualitative study of the direct conversion and the two-IF receiver architectures.

2.1 Receiver performance metrics

2.1.1 Noise figure

The noise figure (NF) is one of the most important parameters in measuring a receiver performance. It represents the amount of signal-to-noise ratio (SNR) degradation as the signal passes through a system. In a typical RF receiver, the main source of noise is the thermal noise, which is a white noise generated by resistors, the channel resistances of MOS transistors, etc. As a result, the use of resistors in the RF paths is always avoided in

order to minimize thermal noise. The ***noise factor*** is defined by:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}}, \tag{2.1}$$

and the ***noise figure*** is given by:

$$NF = 10\log_{10} F, \tag{2.2}$$

where S and N are the signal power and the noise power respectively, and F is known as the noise factor.

In order to evaluate the NF for a receiver, it is important to accurately evaluate the noise contribution from each stage. The overall noise factor from a cascaded system is given by:

$$F = F_1 + \frac{F_2 - 1}{A_1^2} + \frac{F_3 - 1}{A_1^2 A_2^2} + \ldots, \tag{2.3}$$

where A_i and F_i are the gain and noise factor for stage i. From Eq. (2.3), it can be seen that it is very important for the first stage in a receiver chain, usually an LNA, to have a high gain and low noise figure, in order to minimize the overall noise figure of the system. The noise figures of the subsequent stages will have secondary effects on the total noise figure, as long as the first stage has a high gain.

2.1.2 Distortion

Ideally, an RF receiver is modelled as a linear system. However, due to the practical nonlinearity effects resulting from characteristics such as the square-law i-v relationship

in MOS transistors, nonlinear models are needed to predict a more realistic circuit response. Let us assume that the system has the following transfer function:

$$y_{out}(t) = \alpha_1 x_{in}(t) + \alpha_2 x_{in}^2(t) + \alpha_3 x_{in}^3(t) \ , \tag{2.4}$$

and if $x_{in}(t) = A_1 \cdot cos(\omega_1 t) + A_2 \cdot cos(\omega_2 t)$, then the fundamental output components are:

$$\left[\alpha_1 A_1 + \frac{3}{4}\alpha_3 {A_1}^3 + \frac{3}{2}\alpha_3 A_1 {A_2}^2\right] cos(\omega_1 t) + \left[\alpha_1 A_2 + \frac{3}{4}\alpha_3 {A_2}^3 + \frac{3}{2}\alpha_3 A_2 {A_1}^2\right] cos(\omega_2 t) \ , \tag{2.5}$$

while the third-order intermodulation (IM) products for $(2\omega_1 \pm \omega_2)$ are:

$$\frac{3\alpha_3 {A_1}^2 A_2}{4} cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 {A_1}^2 A_2}{4} cos(2\omega_1 - \omega_2)t \ , \tag{2.6}$$

and for $(2\omega_2 \pm \omega_1)$ the IM products are:

$$\frac{3\alpha_3 {A_2}^2 A_1}{4} cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 {A_2}^2 A_1}{4} cos(2\omega_2 - \omega_1)t \ . \tag{2.7}$$

It is clear from the above expressions that, when a signal passes through a nonlinear system, the fundamental term, that is cos (ωt), generates many other higher-order harmonic terms. In the following sub-sections, we briefly discuss the two most important distortion metrics used to describe the nonlinear effects in systems.

A. 1-dB gain compression point

In a linear system, as the input signal increases, the output will increase proportionally. However, in reality, the output will increase up to a certain point within the transfer function. As shown from Eq. (2.5), when the input is relatively small, $\alpha_1 A_1$

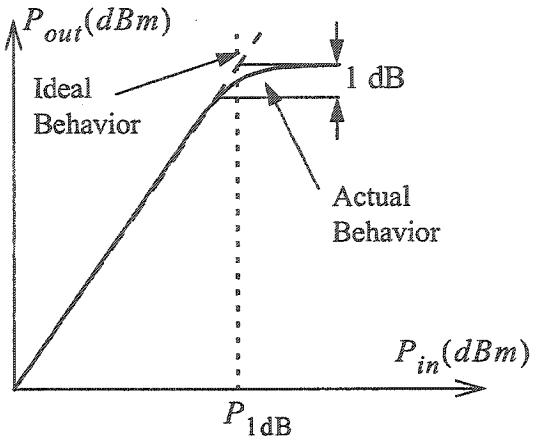


Fig. 2.1: 1 dB compression point.

will be the dominant term for the fundamental output signal. As the signal increases, the contribution from $\frac{3}{4}\alpha_3 A_1^3$ will increase. If $\alpha_3 < 0$, then the gain will start decreasing as the input signal, A_1, increases. As shown in Fig. 2.1, the 1-dB compression point describes the point where the actual and ideal response differ by 1 dB.

B. Third-order intercept point

If two adjacent tones, ω_1 and ω_2, are applied at the input of a non-linear system, the output described by Eq. (2.6) and Eq. (2.7) will be corrupted by nearby third-order

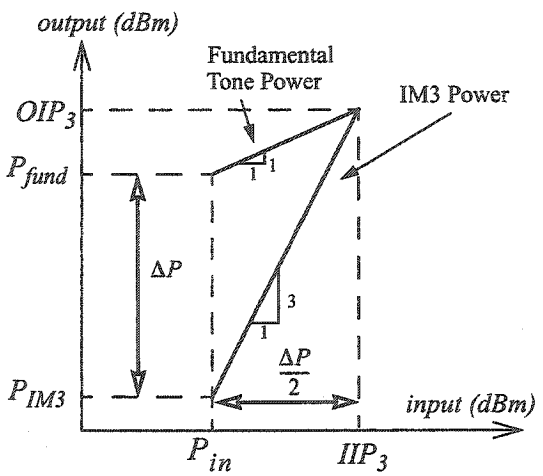


Fig. 2.2: Concept of the third-order intercept.

intermodulation products, i.e. at $(2\omega_1 \pm \omega_2)$ and $(2\omega_2 \pm \omega_1)$. The third-order intercept point (IP3) is used to characterize this behavior. To measure the IP3, a two-tone test is performed with sufficiently small inputs in order to avoid gain compression. As the input signals increase, the output fundamental signals increase proportionally, while the third-order intermodulation products increase at three times the rate of the fundamentals (on a logarithmic scale). The third-order intercept point is defined as the intersection between these two lines, as shown in Fig. 2.2. The x and y-coordinates for the IP3 are called the input and output intercept points (IIP3/OIP3) respectively.

Similar to the noise analysis, the overall IIP3 of cascaded systems can be expressed in terms of the IIP3 of each stage:

$$\frac{1}{IIP3} \approx \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \ldots \quad , \tag{2.8}$$

where $IIP3_i$ and G_i are the IIP3 and power gain for stage *i*. As proposed by the above expression, as long as the later stages in the chain have good IIP3 figures, a reasonable overall IIP3 can be achieved, even though the first stage, usually an LNA, may have a low IIP3 figure. This agrees with intuition since the LNA usually receives small signals, while the subsequent stages normally operate on amplified signals from the LNA and the following stages.

2.1.3 Image-rejection ratio

The image-rejection ratio (IRR) measures the amount of image suppression with respect to the wanted signal. For example, if the input signal is at 5 GHz and it is

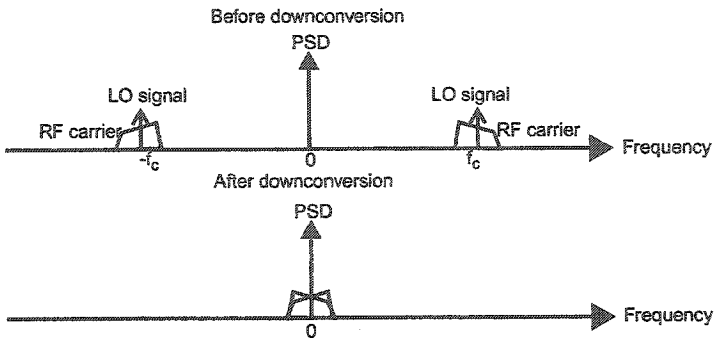


Fig. 2.3: Power density spectrum for a simple direct conversion architecture.

downconverted to 1 GHz, any signal at the image band, that is at 3 GHz, will also be downconverted to 1 GHz and will appear at the output. The IRR can be expressed as:

$$IRR = 10\log_{10}\left(\frac{P_{out-\text{image}}}{P_{out-signal}}\right) - 10\log_{10}\left(\frac{P_{in-\text{image}}}{P_{in-signal}}\right), \tag{2.9}$$

where $P_{i\text{-}i}$ is the power for the wanted signal and the image for both input and output.

2.2 High integration receivers architectures

2.2.1 Direct conversion (Homodyne)

Figure 1.2 shows the basic structure of a direct conversion receiver. Although this approach eliminates the use of off-chip components, it suffers from the following limitations:

1. Although direct conversion does not suffer from the same kind of image problem that the superheterodyne architecture suffers from [23], it has its own image limitations. Figure 2.3 shows the power density spectrum (PSD) of an intended signal and its counterpart from the mirror frequency, with the lower and upper sidebands overlap-

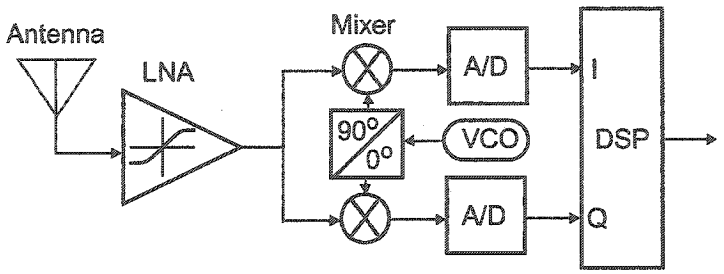


Fig. 2.4: Direct conversion receiver frontend with I/Q paths.

ping at baseband. As a result, the two signals can not be separated. The problem can be easily solved by performing the downconversion with two different local oscillator (LO) signals which are at 90° phase shift with respect to each other, as shown in Fig. 2.4 [16]. However, with the introduction of the I/Q quadrature structure, the image suppression for direct conversion architectures becomes very sensitive to phase and amplitude mismatches in the I and Q signal paths.

2. Since the RF carrier is downconverted to baseband, a direct conversion receiver requires the frequency for the LO signal to be the same as that of the RF input. As a result, a high frequency and low phase noise VCO is needed.
3. Since the isolation between the LO port to the RF port of the mixer is finite, any signal leakage between the two ports will contribute to DC offsets, resulting from self-mixing. This problem is amplified if the amount of DC offset is time varying as discussed in Chapter 1. The subsequent baseband sections may be saturated by this DC offset.

2.2.2 The two-IF receiver topology

Although the direct conversion architecture eliminates the use of off-chip filters, other drawbacks, such as DC offsets, greatly reduce the practical performance of those receivers. As a result, a non-zero intermediate IF stage is often used before downconverting the signal to baseband. Although the mixer in the second stage would have a finite LO feedthrough as well, the resulting DC offset is not as problematic as in direct conversion. This is because the frequency is lower and the potential for the LO signal of the second stage to rebound back from surrounding objects, after being transmitted through the antenna, is low. As a result, the main DC offset in this case is not time-varying, and can be removed using the methods proposed in [16]. Besides, with two downconversion stages, no LO signal needs to operate at the same frequency as the RF input, thus the VCO requirement is relaxed.

However, with the use of a non-zero IF, the image problem that superheterodyne architectures suffer from is reintroduced. Since there are two frequency downconversions that take part in cascade, on-chip image rejection schemes can be used, instead of off-chip filters. In the following, two image-rejection approaches will be explored.

A. Low-IF image-rejection architecture

This architecture is similar to the Weaver structure (Fig. 2.5) [18]. The RF carrier is first downconverted to IF by a pair of quadrature LO signals. With a special arrangement, the IF signals are translated to baseband by another set of quadrature LO signals. By exploiting the phase relationships, both the I and Q channels can be obtained. Figure 2.6

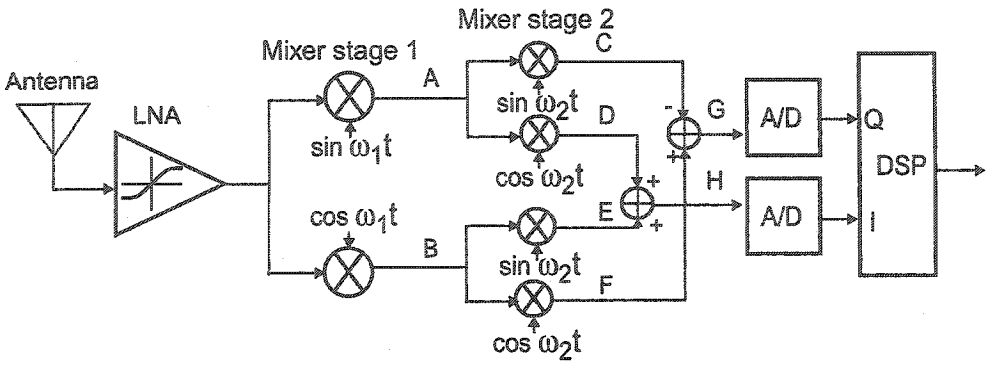


Fig. 2.5: Low-IF image-rejection architecture.

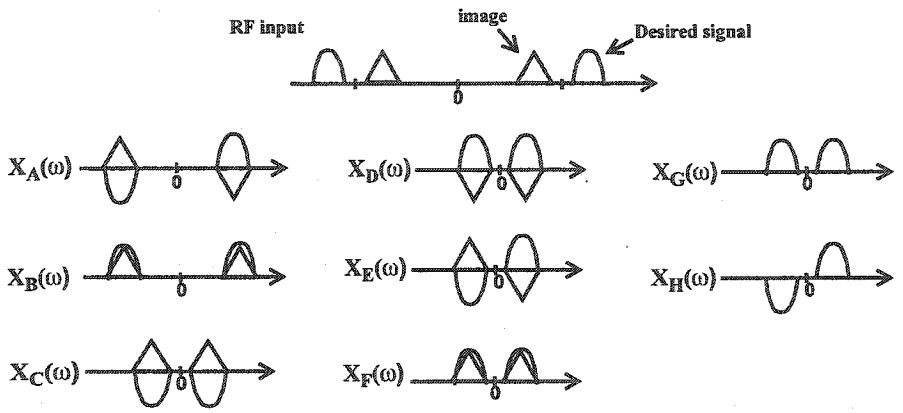


Fig. 2.6: Frequency domain representation for the image-rejection architecture in Fig. 2.5.

shows the frequency domain representation for the signals of the architecture in Fig. 2.5 at various nodes as indicated.

Although this architecture allows high level of integration, the amount of image rejection again depends heavily on the phase matching between the I/Q paths. In order to illustrate this, HP's Advance Design Systems (ADS) is used to perform a high level receiver simulation. Figure 2.5 is implemented in ADS except for the digital section. The outputs from the combiners are taken to calculate the IRR using Eq. (2.9). Table 2.1

	LNA	Mixer (stage 1)	Mixer (stage 2)
Forward Gain	10 dB	10 dB	-5 dB
Noise Figure	4 dB	15 dB	10 dB
IIP3	-10 dB	-1 dB	5 dB
S_{11}	-10 dB	-	-
LO-IF Feedthough	-	-40 dBm	-40 dBm

Table 2.1: Receiver components parameters used in HP ADS simulation.

LO Phase Mis-match	IRR
0^o	95 dB
1^o	40 dB
2^o	35 dB
3^o	32 dB

Table 2.2: IRR with respect to LO mismatch.

shows the performance parameters of the receiver components that were used in the simulation. Note that active mixers were used for the first stage, and passive mixers for the second stage. Table 2.2 shows the resulting IRR with different degrees of phase mismatch. As shown, the IRR is very sensitive to the phase mismatch in this type of architecture: It decreases from 95 dB to 32 dB as a result of a few degrees of mismatch!

B. Half-RF image rejection architecture

The second image-rejection architecture considered performs downconversion twice, using the same LO signal for the two stages (Fig. 2.7) [3]. In order to translate the RF signal to baseband, the frequency of the LO signal is set to be half that of the RF carrier. Unlike the previous image-rejection architecture that had additional circuitry for image rejection, this approach performs image rejection by selecting a specific LO signal. For

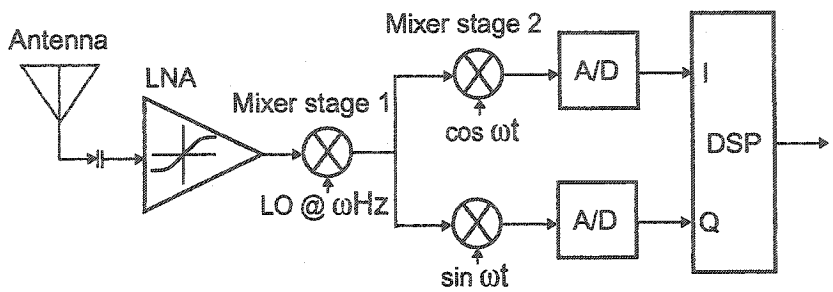


Fig. 2.7: Half-RF image-rejection architecture.

the first stage, since the LO signal is half that of the RF carrier, the image lies at DC. By using a DC blocking capacitor at the input, or using an on-chip high pass filter, which is feasible since the wanted signal and the image are widely separated, the image is eliminated. As a result, this architecture is considerably less sensitive to the mismatches in the signal paths compared to the previous topology.

Nevertheless, this architecture has its own limitations. First, the flicker noise of the LNA, which lies around the zero frequency, may upconvert to the IF signal and then subsequently downconvert to baseband. By using relatively large transistors for the LNA, the flicker noise corner frequency can be reduced. Second, if the LO-IF feedthrough for the first mixer stage is large, it may corrupt the IF signal, since both the IF and the LO signals are at the same frequency.

2.3 Conclusion

From the above discussion we conclude that the half-RF image rejection architecture is more immune to phase mismatch between the I and Q paths, and requires less components than the low-IF architecture. In order to demonstrate that a CMOS

technology can be used to implement such an architecture for 5 GHz applications, and to investigate the effect of the MOS transistor flicker noise on the system, detailed simulation and measurement results for a half-RF architecture implementation are presented and discussed in the following chapter.

Chapter 3: 5 GHz CMOS Receivers

3.1 Introduction

Two RF CMOS receiver frontends were designed and fabricated using TSMC's digital 0.18 μm CMOS technology available to the author. The objectives of each one of the two receivers are:

1. To demonstrate the feasibility of using a CMOS process to implement very low-voltage (0.8-1V) RF circuitry.
2. To explore the performance of the half IF image-reject receiver architecture discussed in the previous chapter.

3.2 A very low-voltage receiver frontend

Figure 3.1 shows the complete architecture of the first receiver prototype. An external microstrip balun is used to convert a single-ended signal to differential. The chip consists of a differential low noise amplifier (LNA) connected to a set of I/Q mixers, which are driven by a voltage-controlled oscillator (VCO) with quadrature outputs. The outputs of the I/Q mixers can subsequently be connected to another downconversion stage to translate the IF signal to baseband, and thus implementing a Weaver image reject

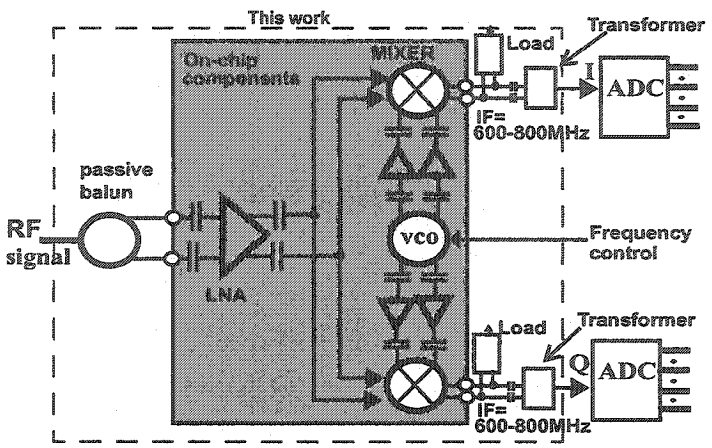


Fig. 3.1: Receiver architecture.

architecture (e.g. [18]). Another alternative is to directly process the IF signal, after being converted to single-ended by a transformer, using a high-speed ADC [7] followed by a digital signal processor, as suggested in Fig. 3.1. DC blocking capacitors are used between stages in order to be able to bias each sub-circuit independently. Buffers are used between the mixers and the VCO to increase isolation. Off-chip transformers are used to convert the differential outputs to single-ended for measurement purposes. All of these components are assembled together on a custom built PCB for testing.

3.2.1 Circuit description

A. Signal generation

Since the receiver requires a differential input, a balun (unbalanced-to-balanced transmission converter) is used to convert the single-ended signal from the signal generator to a differential signal. There are generally three methods to perform this conversion:

1. An on-chip transformer can be used, since it is hard to find a discrete off-chip trans-

	On-chip transformer	Active balun	Off-chip balun
Advantages	• easy to use • no power consumption • fully integrated solution	• can provide signal gain • consumes less space than an on-chip transformer	• phase and amplitude are well matched for the differential outputs • no power consumption
Limitations	• no accurate models available for the designer • depending on the structure and process, signal loss after conversion can be as high as 10 dB	• phase and amplitude outputs are very sensitive to parasitic effects at high frequency (>3 GHz) • consumes power	• needs a relatively large off-chip space to implement • about 3 dB signal loss

Table 3.1: Comparison of different methods for balun implementation.

former which can operate at 5 GHz.

2. An on-chip active balun, which is basically a differential amplifier with one of its input terminals grounded.
3. An off-chip microstrip balun on the PCB.

Table 3.1 shows the advantages and limitations for the different possible balun implementations. Ideally, the on-chip balun would be the best choice, since both the amplitude and the phases of the outputs can be better controlled and predicted, compared to the active balun. Also, it would provide a fully integrated solution. However, since there were no accurate transformer models available to the designer during the early design phases, it was decided that, from a research point of view, the off chip balun provides the most reliable solution. It's performance can be easily tested in a stand-alone setup. As a result, an off-chip balun is used to generate the differential signals, and transformer modeling was investigated at a later stage (Chapter 4) so that accurate modelling is made available for future use.

Figure 3.2 shows the structure of the off-chip balun, also known as a ring hybrid. Port 'A' is the input while the outputs at port 'B' and 'C' are 180^{o} out of phase with respect to

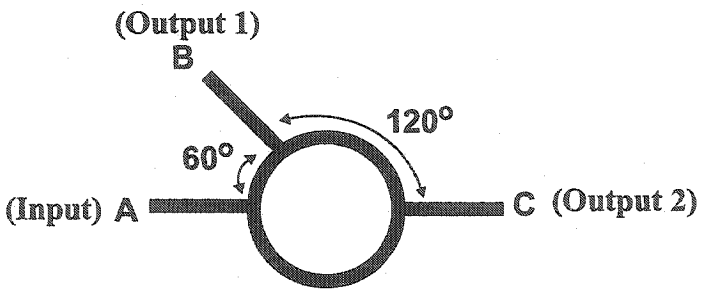


Fig. 3.2: Off-chip microstrip balun.

each other. The circumference of the balun is $3*\lambda_g/2$, where $\lambda_g = \frac{\lambda_o}{\sqrt{\varepsilon_{eff}}}$, and λ_o is the wavelength of the signal in free space, that is 1/5.2GHz in our case, and ε_{eff} is the effective permittivity of the microstrip material. An additional advantage of using the ring hybrid balun is the fact that if port A sees an impedance Z_o, then the same impedance appears at both output ports.

As for the outputs of the receiver, since they are at frequencies lower than 1 GHz, transformers from MiniCircuits are used to combine the differential signals to single-ended for measurement.

B. Inductors modelling

The performance of the receiver depends heavily on the quality factors of the on-chip inductors. In order to obtain accurate inductor models for simulation, ASITIC - an inductor modeling tool from Berkeley [11], and MIND (MIND: McGill INDuctor modeler), an in-house modeling tool [14], were used to produce and cross-check the π-models generated (Fig. 3.3).

C. Low noise amplifier

Figure 3.4 shows the simplified schematic of the LNA, including all on-chip

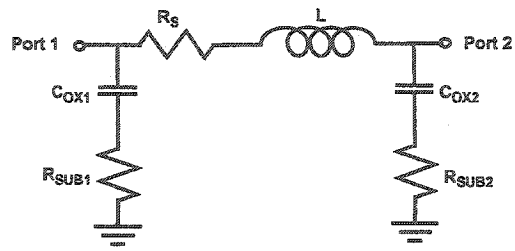


Fig. 3.3: Example of a π-model for an on-chip inductor [11][14].

components. In order to be able to operate from a very low voltage supply, a folded cascode structure is used, since it eliminates one level of transistor stacking [19]. In this configuration, transistors M1 and M4 act as common-source amplifiers, and transistors M2 and M5 are used as common-gate current buffers, with load inductors L7 and L9. As a result of this circuit topology, more voltage headroom can be used in biasing the transistors in saturation, leading to an improved linearity. An important added advantage of this topology is its improved reverse isolation.

The LC tanks, which resonate at the RF frequency, formed by inductors L1 and L2 and capacitors C1 and C2, behave as DC current sources. The advantage of using such an approach is to provide the necessary DC bias current without requiring extra voltage headroom, while presenting a high impedance to the RF signals at 5.2GHz. Besides, current sources implemented using transistors provide a wideband high impedance

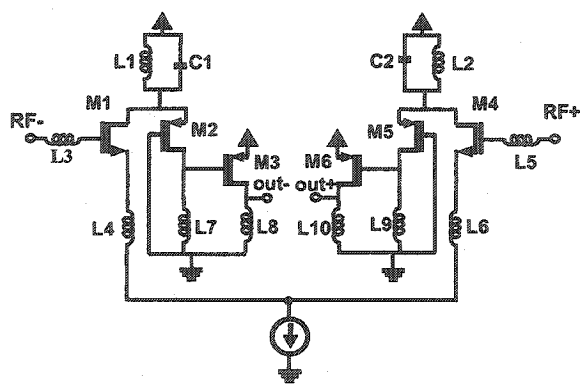


Fig. 3.4: Schematic of the LNA.

response, while an LC tank provides a low impedance to other frequency bands, including the image signal, resulting in better image rejection. The other advantage of using an LC tank as such is to nullify the effect of the parasitic capacitances of the transistors, resulting in an improvement of the noise figure (NF) [20].

In order to achieve minimum noise, the widths of transistors M1 and M4 need to be set to their optimum values, W_{opt}. According to [21]

$$W_{opt} = \frac{1}{3\omega L R_s C_{ox}} \quad , \tag{3.1}$$

where ω is the operating frequency of the circuit in radian, L is the minimum feature size of the fabrication process (0.18 μm in this work), C_{ox} is the gate capacitance per unit area, and R_S is the input resistance (50Ω in this case).

Inductors L3 and L4 are used for matching the input resistance, Z_{in}, to 50Ω, and to simultaneously resonate at the operating frequency of 5.2GHz. It can be shown that

$$Z_{in} = s(L3 + L4) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs} + C_{gd}}\right) L3 \,. \tag{3.2}$$

At the operating frequency, the first two terms in Eq. (3.2) should cancel each other by adjusting the value of L4. This leaves $\left(\frac{g_m}{C_{gs} + C_{gd}}\right) L3$ to set the value of the real part of the input impedance, by selecting an appropriate value for L3. Buffers formed by transistors M3 and M6 are used to provide extra gain, and to increase isolation between the LNA and the mixer.

D. Mixer

The mixer (Fig. 3.5), which is based on a double-balanced Gilbert active structure in order to reject any LO-to-RF feedthrough, downconverts the differential RF signal from 5.2 GHz to a 600 - 800 MHz IF. It consists of a pair of transconductors (M5 - M6) and four transistors (M1-M4) which act as switches.

Although passive mixers generate less noise than active mixers, they require a larger LO signal and have no conversion gain, resulting in a severe noise figure deterioration. On the other hand, while active mixers can provide signal gain, they suffer from the noise generated by the transconductor and the switching transistors. To minimize the noise from the latter, which appears directly in the output signal path, extra current sources I_o are used as shown in Fig. 3.5. This decreases the DC biasing currents of M1 - M4, thus reducing their shot noise, while maintaining the high bias of transistors M5-M6 necessary to ensure a high RF gain [23]. Apart from lowering the shot noise, the use of sources I_o also enables higher conversion gain by allowing the use of larger resistive loads, since the drain currents through the switching transistors are lowered. Besides the shot noise, the switching transistors M1 to M4 also contribute thermal noise to the output. At the zero-crossing of the LO signal, all the switching transistors will be on injecting thermal noise to the output. Therefore, a large LO is desired to minimize the transition time.

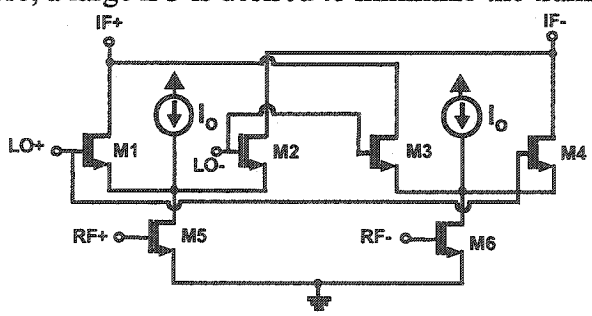


Fig. 3.5: Schematic of the I/Q mixer.

To improve the mixer linearity, the transconductor pair is realized as a grounded-source differential pair, rather than a differential pair with constant current source biasing. A current source biasing would introduce third-order intermodulation products and lower the overall linearity of the mixer [24], since the output drain current depends on the square of the input voltage. On the other hand, with the grounded-source pair (Fig. 3.6), the differential output current, I_{out}, can be expressed as:

$$I_{out} = \frac{1}{2}\mu_o C_{ox}\frac{W}{L}[(V_{gs1}-V_{th})^2-(V_{gs2}-V_{th})^2] = \frac{1}{2}\mu_o C_{ox}\frac{W}{L}(V_{gs1}-V_{gs2})(V_{gs1}+V_{gs2}-2V_{th})$$

$$I_{out} = \mu_o C_{ox}\frac{W}{L}V_{in}(V_{gs}-V_{th}) \,. \qquad (3.3)$$

As a result, the output current, I_{out}, only depends linearly on the input voltage, V_{in}. This topology also helps reducing the voltage headroom requirements, as it eliminates any additional transistor stacking, such that needed for a tail biasing current source.

Since the mixer is to operate from a 0.8-V supply, transistors with relatively large widths are used, in order to lower the threshold voltage required to bias the transistors in the saturation region. In addition, the gates of transistors M1-M4 are biased near threshold, in order to minimize their switching times, thus reducing the output noise. The RF signals from the LNA are AC coupled to the inputs of the mixers, in order to allow the latter to be set to different DC biasing points. As for the loads at the IF outputs, they can

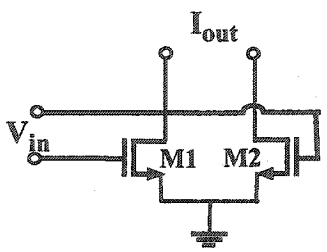


Fig. 3.6: Grounded-source differential pair.

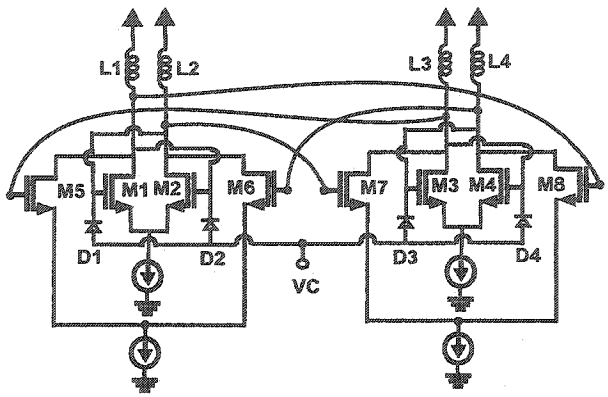


Fig. 3.7: Schematic of the quadrature VCO.

be either resistive or reactive (e.g. an LC tank).

E. Voltage-controlled oscillator

The core structure of the VCO (Fig. 3.7) is a differential topology, which consists of two pairs of cross-coupled LC oscillators formed by transistors M1-M2 and M3-M4, using on-chip load inductors L1-L4. The two transistor pairs are coupled through transistors M5-M8 in order to provide quadrature outputs for both the I and Q paths [25]. The two cross-coupled transistor pairs can only co-exist in quadrature phase. If the two pairs are in-phase or in anti-phase, then the negative resistance will be absorbed by one of the pairs, turning off the other pair and pulling up both of its drain nodes to V_{DD}. As a result, it will also shut off the remaining pair through the cross-coupled transistors, since both of the gates of the transistor pair cannot be connected to V_{DD} at the same time in order for oscillation to occur. In summary, oscillation cannot be maintained if the two pairs are in-phase or in anti-phase. Inductors L1-L4 resonate with the parasitic capacitors of the transistors to set the oscillation frequency, while the transistors provide the negative resistances necessary to overcome the inductors losses.

In order to ensure oscillation, the oscillator must provide sufficient transconductance

to overcome the losses in the LC tanks. Figure 3.8 shows the input resistance, R_{in}, seen by the LC tanks; it equals $2/g_m$, where g_m is the transconductance of one transistor. Assuming a biasing current of 3mA for each one of transistors M1 to M4, and the Q factor and series resistance of the inductor being 5 and 5Ω respectively, and $\mu_o C_{ox}$ is $429\mu A/V^2$ for the CMOS technology used, the minimum width of the transistor core is found using the following equation,

$$R_{in} = \frac{2}{g_m} = Q^2 \times R_s \tag{3.4}$$

where

$$g_m = \sqrt{2 I_D \mu_o C_{ox} \frac{W}{L}} \,. \tag{3.5}$$

From Eq. (3.4) and Eq. (3.5), g_m is 0.016S, and thus W/L needs to equal 100.

However, in order to guarantee that the VCO starts up, a safety factor of 3 was used. As a result, the transconductance value was tripled, and from Eq. (3.5):

$$g_m = \sqrt{2 I_D \mu_o C_{ox} \frac{W}{L}} = 0.016 \times 3 \,,$$

and the corresponding W/L is 900. To minimize the parasitics due to the drain capacitances of the transistors, minimum channel lengths were used, i.e., L=0.18 μm,

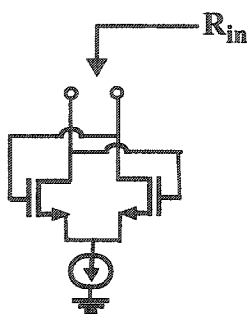


Fig. 3.8: Input resistance of the VCO core pair.

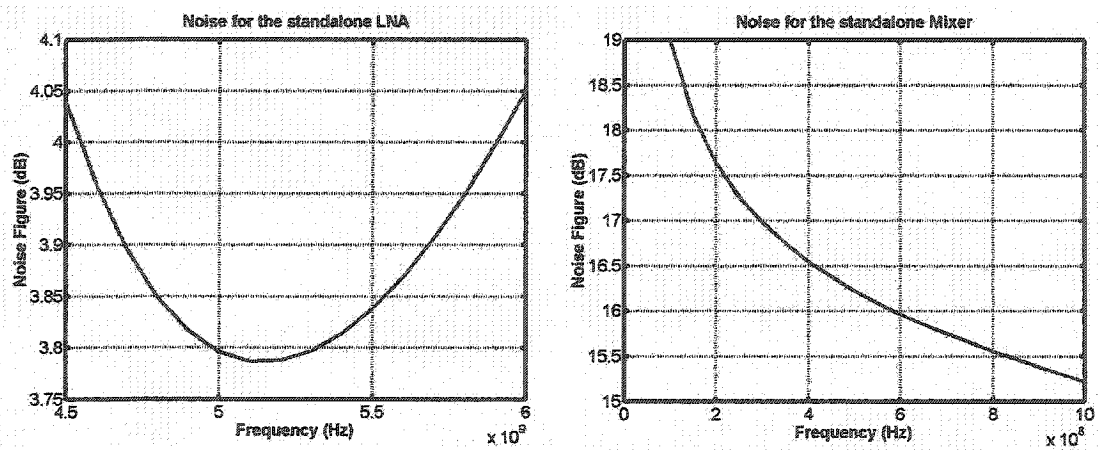
resulting in the widths of transistors M1 to M4 to be 150μm.

The output phase noise at an offset Δf from f_o can be approximated by the following relationship [26]

$$L\{\Delta f\} = kT(1+A)\,Z_o \frac{1}{Q_{tank}} \left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{V^2_{rms}}, \tag{3.6}$$

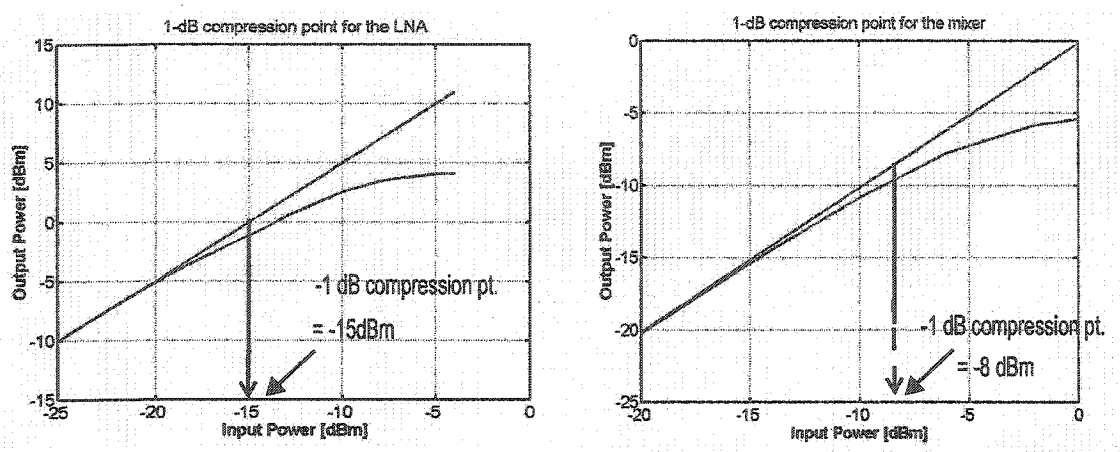
where kT is the product of the Boltzman constant by the absolute temperature, A is the noise factor safety margin necessary to ensure oscillation start-up, V_{rms} is the root mean square voltage at the oscillation nodes, and $Z_o = \sqrt{(L/C_{tank})}$ and Q_{tank} are the tank characteristic impedance and quality factor, respectively.

In order to provide tuning capabilities, accumulation mode varactors D1 - D4, which are implemented as NMOS transistors over N-wells [26], are used and are controlled with an external DC voltage source, V_c, in order to provide the desired capacitance. As a result, the tuning range of the VCO is from 4.4GHz to 4.6GHz. Common-source buffers with inductive loads are used to increase isolation to the mixer, and to provide a much desirable amplification for the VCO signals driving the mixers.



(a) (b)

Fig. 3.9: (a) Simulated LNA noise figure, and (b) mixer noise figure.



(a) (b)

Fig. 3.10: Simulated 1-dB compression point for (a) LNA (b) mixer.

3.2.2 Simulation results

HSPICE and SpectreRF were used to simulate the different receiver components, as well as the overall performance of the receiver from the extracted layout with parasitics. Figure 3.9 shows that the expected noise figure of the LNA is 3.8 dB at 5.2GHz, while the mixer has an expected noise figure of about 16.5dB. Figure 3.10 shows the 1-dB compression point of the LNA and of the mixer to be -15dBm and -8dBm respectively. The simulated phase noise of the VCO is about -104dBc/Hz at a 500kHz offset as shown

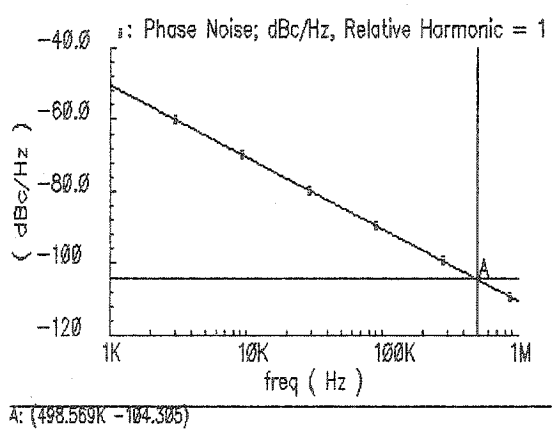


Fig. 3.11: Simulated VCO phase noise.

LNA	
Operating freq.	5.2GHz
Power consumption	24mW
Noise figure	3.8dB
S_{11}	-15 dB
1dB compression	-15dB
Voltage gain	15 dB

Mixer	
Power consumption	16mW
SSB noise figure	16.5dB
1dB compression	-8dB
Conversion gain with (inductive/ resistive) load	10dB/0dB

VCO	
Operating Freq.	4.5GHz
Power consumption	30mW
Phase noise @ 500kHz offset	–104 dBc/ Hz

Table 3.2: First receiver components simulation results.

in Fig. 3.11. Table 3.2 summarizes the simulation results for each individual component of the first prototype, with a 0.8V supply. The overall gain for the receiver is 15dB and the image rejection ratio is 20.5dB with an image signal at 3.8GHz.

A. Receiver overall performance

In order to verify the overall performance of the receiver, HP ADS was used to evaluate the system noise figure and 1-dB compression point. Figure 3.12 shows the ADS schematic that was used to perform the simulation. All the receiver components are taken from the ADS standard libraries, and the parameters for each component were set based

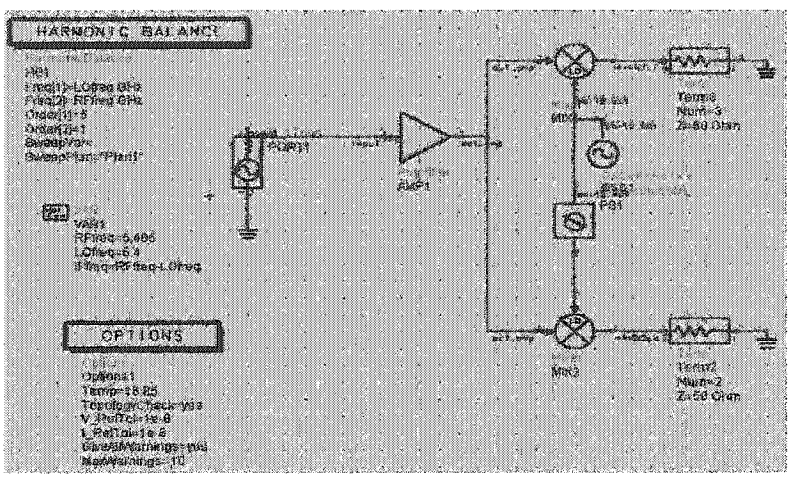


Fig. 3.12: ADS schematic.

on the simulated performances shown in Table 3.2. In order to generate the quadrature VCO signal in ADS, a 90° phase shifter was added, since a quadrature VCO component was not available in ADS. The simulated noise figure and 1-dB compression point for the receiver were found to be NF = 6.5 dB and -15 dBm respectively.

3.2.3 Measurement results

The low-voltage receiver frontend was fabricated in a standard 0.18 μm CMOS technology from TSMC. Figure 3.13 shows the micrograph of the chip with an area of 3.2mm x 1.7mm. As shown in the micrograph, the LNA and the VCO are placed as far as

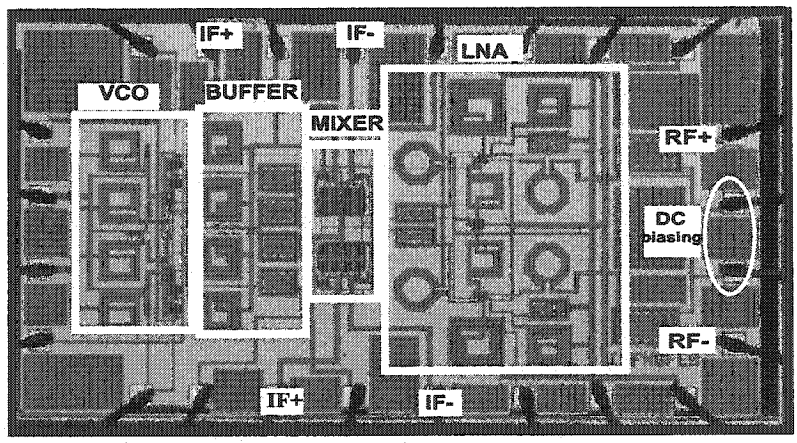


Fig. 3.13: Receiver chip

possible from each other to minimize interference. The differential RF inputs are separated by DC biasing pins in order to minimize the cross-coupling effects between them. A standalone LNA, which was designed to operate at 5.8GHz and was packaged in the same package (CFP24) as the receiver, and a standalone VCO, were also built in order to verify their performance. The only difference between the integrated components and the standalone versions is that the standalone versions had additional buffers with resistive loads in order to drive the 50Ω impedances of the measurement equipment,

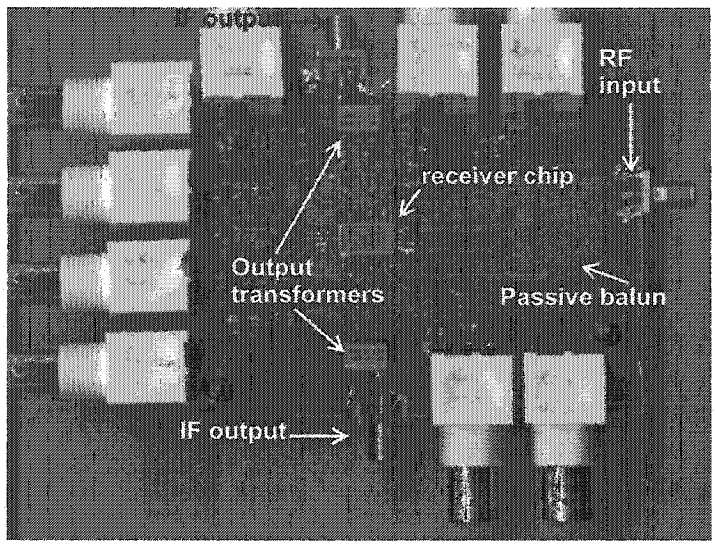


Fig. 3.14: Test fixture for the receiver.

instead of inductive loads.

A. Calibrating for the package and the test fixture losses

Since the CFP24 package (the best option that was available to the designer at the time) is optimized for operation up to 2GHz frequency, extra losses at 5GHz were expected, but could not be predicted during design/simulation.

To account for the package losses, the exact same test fixture (Fig. 3.14) that was used

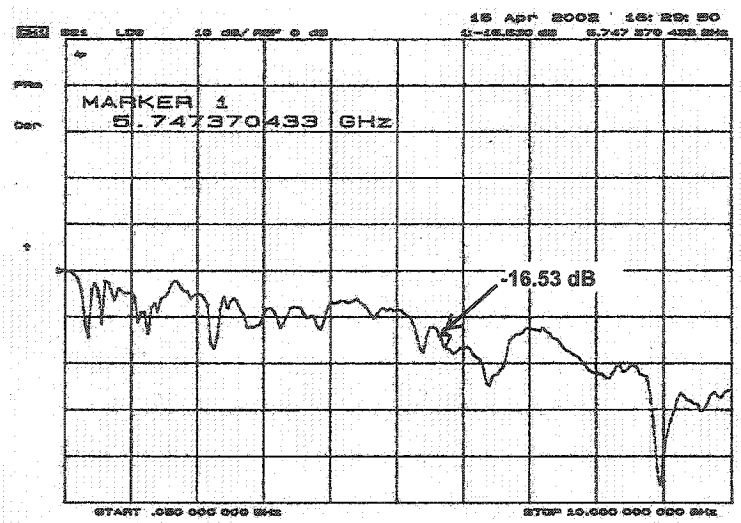


Fig. 3.15: Loss of the test fixture with package replaced by a short.

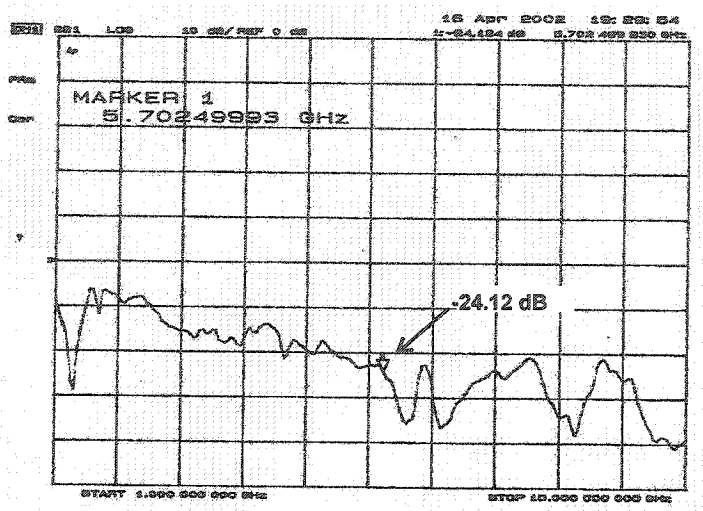


Fig. 3.16: Loss of the test fixture with an empty package shorted internally.

in measuring the performance of the receiver, was used with an empty CFP24 package having the two input and output pins of the receiver connected by a metal wire internally. This was done in order to measure the losses due to the package. The losses due to the test setup were measured separately: A metal wire was used to short two pins of the package on the PCB while the package was removed. Fig. 3.15 shows a -16dB loss for the test setup alone at 5.7GHz. With the empty package, as shown in Fig. 3.16, the loss at 5.7GHz is -24dB. As a result, it is estimated that each pin of the package has (24-16)/2 = 4dB loss at 5.7GHz.

Apart from accounting for the losses in the package, the losses due to the PCB and to the connection wires will also decrease the measured overall gain of the receiver.

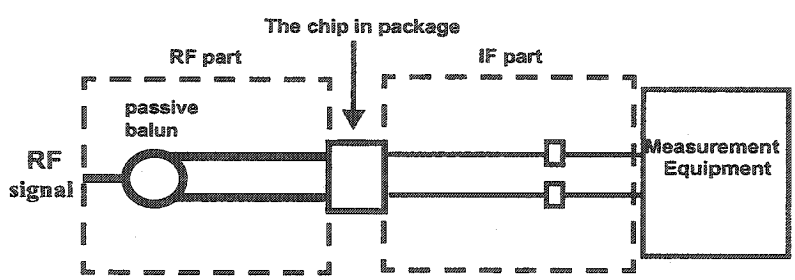


Fig. 3.17: Testing PCB setup.

Each pin of the CFP24 package @ 5GHz	-4dB
RF part of the PCB in the 5GHz range	-6.5dB
IF transformer @300MHz	-3dB
Connection cables and connectors @5GHz	-3dB
Total	-16.5dB

Table 3.3: Losses due to the test fixture.

Depicted in Fig. 3.17 is the testing PCB setup: The circuit consists of two sections, an RF part and an IF part. The RF part includes the passive balun and all the PCB traces that carry the input 5GHz signals, while the IF part includes the IF transformers. All the signals after the chip are in the few mega-hertz frequency range. The PCB in Fig. C.2 in Appendix C was used to measure the losses due to the RF part at 5GHz. Figure 3.18 shows a -6.2dB loss at 5.7GHz. Finally, it was found through measurements that the cables and connectors between the measurement equipment and the PCB contribute about 3dB of loss in the 5GHz range. Since the IF portion of the setup operates at a lower frequency, it does not contribute with significant losses, apart from the 3dB loss associated with the IF transformer. Table 3.3 summarizes all the estimated losses due to

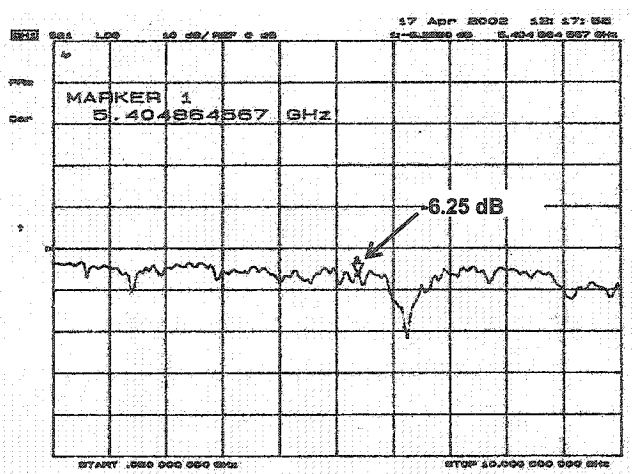


Fig. 3.18: Loss of the RF part of test fixture.

the test setup, with a total of -16.5dB.

B. Standalone LNA

A custom PCB was built to test the standalone LNA (Fig. 3.19). As described in section 3.2.1, a ring hyrid is used to generate the differential input signal. The same structure is used to combine the differential output signal to single-ended for measurement. To calibrate out the losses due to the baluns and to the PCB, a special test structure was built and used. The calibration procedure is detailed in Appendix B.

Although the LNA was designed to match a 50Ω input resistance, the parasitics from the PCB traces, connectors, cables, and the package do affect the input resistance. As a result, a simple off-chip matching network was used (Fig. 3.19). It consists of a pair of transmission lines that connect the balun to the LNA input, and a sliding capacitor. Together they form a differential π-matching network. By sliding the capacitor along the transmission lines, an input reflection coefficient S_{11} = -18.4 dB is obtained for the LNA, as shown in Fig. 3.20.

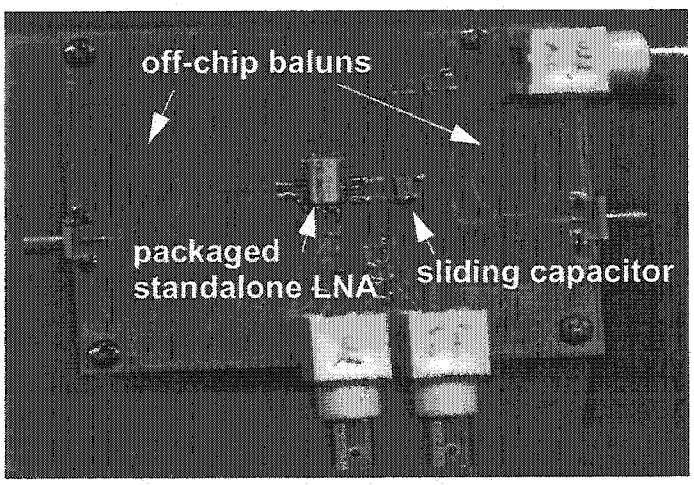


Fig. 3.19: PCB for testing the standalone LNA.

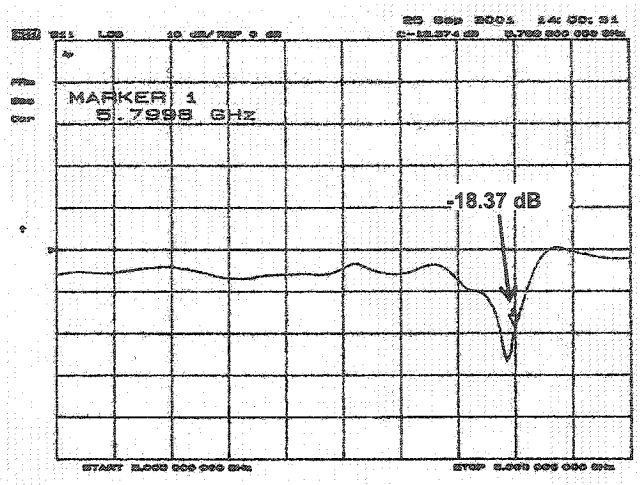


Fig. 3.20: Measured S_{11} of the standalone LNA.

As for the gain of the LNA, Fig. 3.21 shows a 5.7dB gain at 5.8 GHz. Taking into account the losses due to the package (section 3.2.3A), the gain of the standalone LNA is estimated to actually be (5.7 + 4 + 4) = 13.7dB, which is fairly close to the gain predicted by simulation (15 dB). The lower measured value is attributed to the fact that, at resonance, slightly lower than expected quality factors of the on-chip inductors and capacitors were achieved. As a result, a portion of the RF signal could be lost to the LC tank [5].

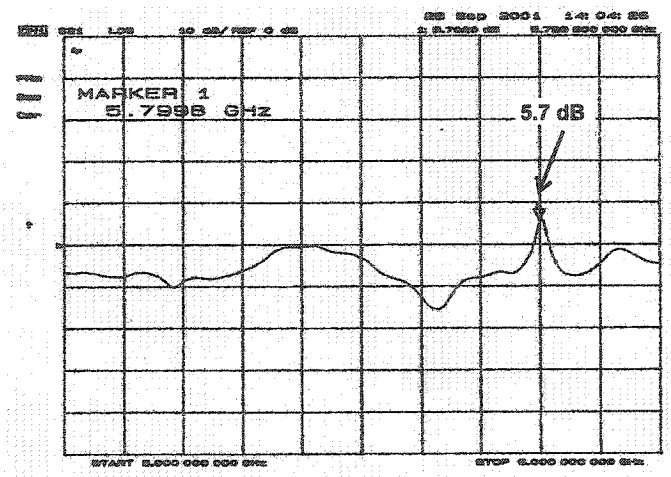


Fig. 3.21: Measured S_{21} of the standalone LNA.

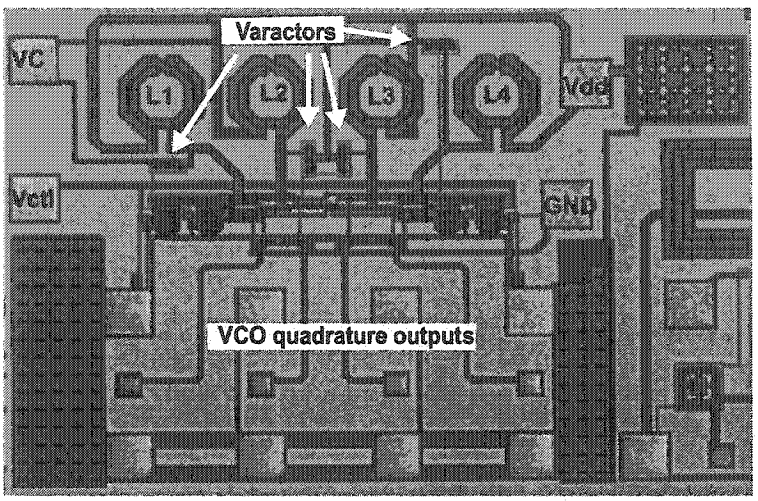


Fig. 3.22: Micrograph of the standalone VCO.

C. Standalone VCO

On-chip probing was used to test the performance of the standalone VCO (Fig. 3.22). The VCO generates quadrature signals at 4.5GHz. It has a tuning range from 4.4GHz to 4.6GHz, which agrees well with simulation (Table 3.2).

D. Overall

Since the performance of both the standalone versions of the LNA and of the VCO used in the receiver were verified, the next step is to test the receiver as a whole. Similar to the testing procedure for the standalone LNA, a custom test fixture which employs the hybrid balun to generate the differential RF input signals for the receiver is used. As was mentioned earlier, off-chip transformers from MiniCircuits were used to combine the output 700MHz IF signals. Figure 3.14 shows the PCB used in performing all the receiver measurements.

To verify that the on-chip VCO is functional and find its frequency, LO leakage was measured while turning off the supply voltage of the LNA. As shown in Fig. 3.23, an LO

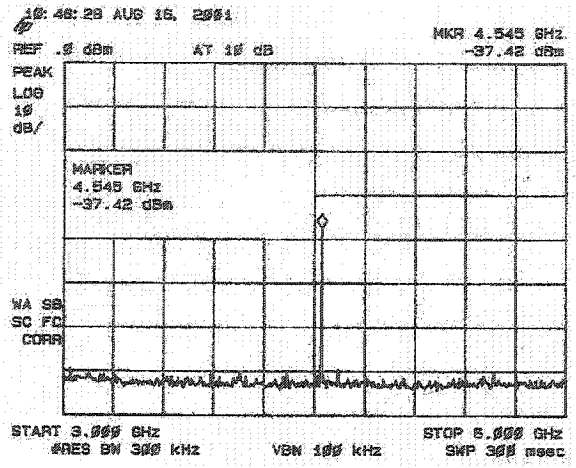


Fig. 3.23: LO leakage in the receiver.

leakage signal of -37.4 dBm is observed at 4.5GHz, which shows that the VCO is functional.

The next step in testing the receiver is to power up the entire chip from a 0.8V power supply. A sweep of the RF input frequency reveals that the LNA operates at 5.2 GHz, which was the desired operating frequency. With the VCO centered at 4.5 GHz, the IF signal is at 700 MHz. Resistive loads (50Ω) are used at the mixer outputs. Figure 3.24 shows a plot of the input reflection coefficient S_{11} (-20dB @ 5.2GHz) of the receiver, obtained with the help of a sliding capacitor as discussed earlier.

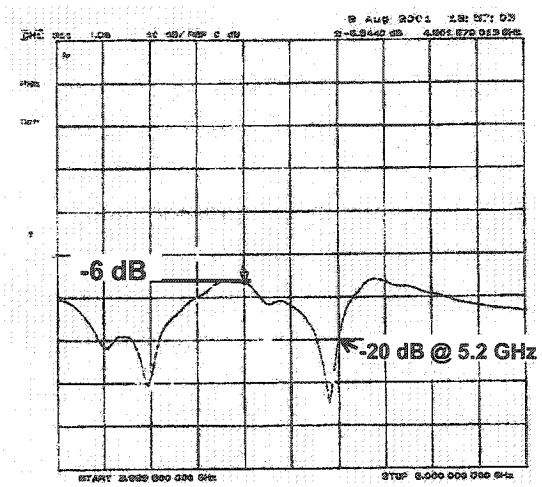
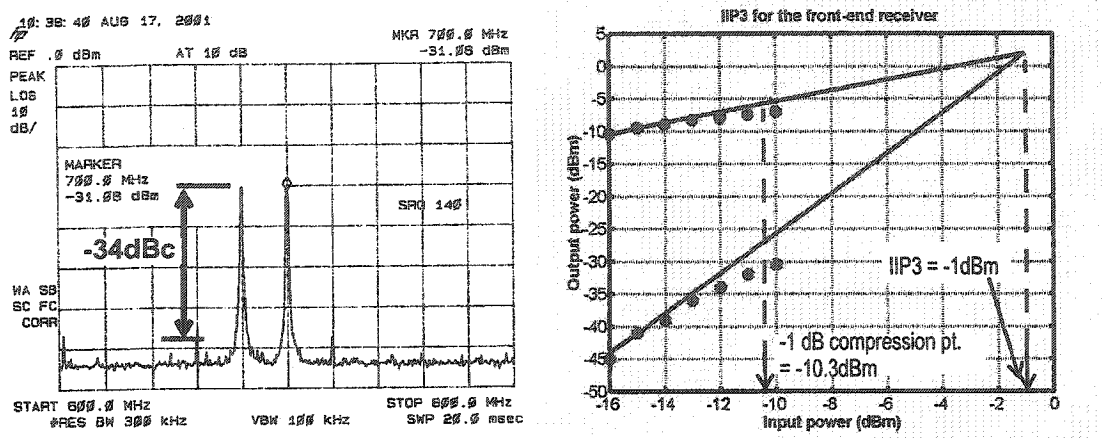


Fig. 3.24: Input reflection S_{11} of the receiver.



(a) (b)

Fig. 3.25: (a) frequency response of the two-tone test (b) Measured third-order intercept plot.

Figure 3.25a shows the measured output spectrum for a two-tone test input at 5.2GHz and 5.22GHz, with -20dBm of power. The fundamental signals appear at 680MHz and 700MHz, while the third-order intermodulation outputs, which are located at 660MHz and 720MHz, are -34dBc below the fundamentals. The same setup was used to obtain the overall 1-dB compression point and the IIP3 of the receiver, by sweeping the power of the two-tone input. Figure 3.25b depicts the third-order intercept plot, with the 1-dB compression point clearly denoted at -10.3dBm.

As can be deduced from Fig. 3.25a, the gain of the receiver without any calibration is about -11 dBm. As discussed in section 3.2.3A, the losses in the package and in the test fixture should be accounted for (Table 3.3). Doing so, the actual gain of the receiver is estimated to be about 6dB. However, the receiver overall gain was expected to be 13.5dB, knowing that the standalone LNA has a 13.5dB gain and that resistive loads are used at the mixer outputs, resulting in an expected mixer conversion gain of 0dB. A newly developed in-house tool was used to estimate and model the parasitic inductances of the

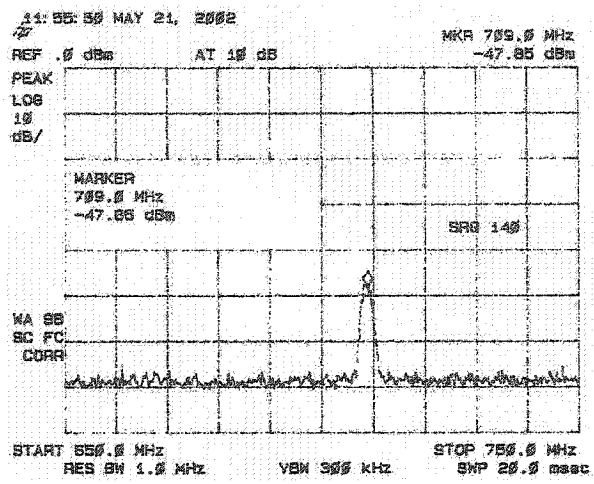


Fig. 3.26: Frequency response of the image signal.

metal strips connecting the LNA to the mixer on chip, and an extra loss of 6dB was observed. This accounts for a major portion of the observed loss in gain.

Figure 3.26 shows the IF output in the presence of a 3.8GHz signal at -15dBm, which falls in the image frequency range. After calibration, the power of the image signal is estimated to be -32dBm. Using Eq. (2.9), the image rejection ratio is therefore 22dBm, which is fairly close to the value expected from simulation. Table 3.4 summarizes the measured receiver performance.

Overall gain (50Ω system)	6dB
Overall noise figure	7dB
Input S_{11} @ 5.2 GHz	-20dB
IIP3	-1dBm
Input 1-dB compression	-10.3dBm
Image rejection ratio (IRR)	22dBm
Power dissipation @ 0.8V	56mW
Die size (0.18 μm CMOS process)	5.44mm^2

Table 3.4: Measured receiver performance.

3.2.4 Conclusion

In this section, we demonstrated that a 0.18 μm state-of-the-art CMOS technology is capable of operating in the 5 GHz range, from a very low-voltage supply, by using folded cascode structures, and with careful biasing and transistor sizing. Our prototype also demonstrated that, with a high IF architecture, combined with the passband characteristics of the LC tanks used in the folded cascode LNA, a receiver with reasonable image rejection can be realized, even without any additional filtering or special image rejection schemes.

3.3 Image-reject receiver front-end

The objective of this receiver prototype is to explore the performance of a CMOS half RF image-reject receiver architecture. A 1.8V supply is used. Figure 3.27 shows the overall architecture of the receiver. An external hybrid balun is used at the input. A differential low-noise amplifier is used as the first stage, followed by two mixers stages. For the first downconversion stage, as described in Chapter 2, the LO signal is half of the RF signal, resulting in the image lying at DC. By using a DC blocking capacitor at the input of the LNA, the image signal is minimized. Capacitors are inserted between the LNA and the mixer in order to remove the flicker noise generated by the LNA, which lies in the baseband region. The actual amount of image rejection obtained by this architecture will depend heavily on substrate leakage, since the image signal can always leak into the substrate and appear at the output. The second stage of mixing has limitations similar to those of a direct conversion architecture, resulting from the self-mixing of the leakage LO signal from the first mixer. Since the DC offset voltage resulting from LO leakage is constant, it can be removed by subsequent baseband stages. Buffers with resistive loads are used at the output in order to drive the 50Ω load of the

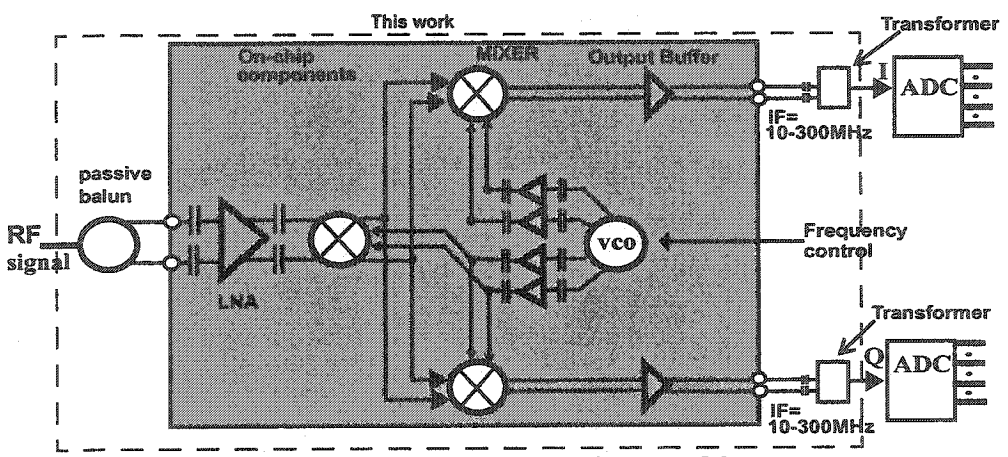


Fig. 3.27: Image-reject receiver architecture.

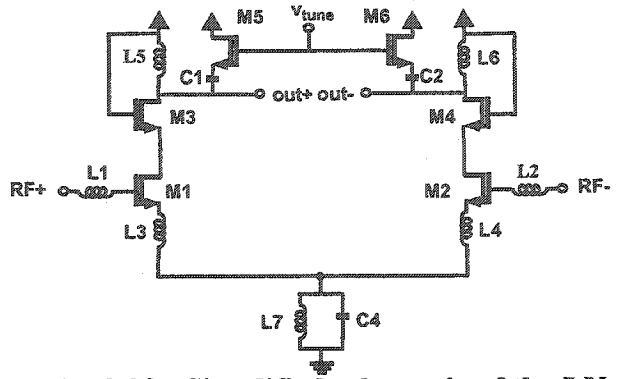


Fig. 3.28: Simplified schematic of the LNA.

measurement equipment.

3.3.1 Circuit description

A. Differential low-noise amplifier

Since the supply voltage is 1.8V, a cascode structure with inductive degeneration is used (Fig. 3.28), instead of a folded-cascode structure, in order to lower the DC biasing current. A cascode structure will provide a higher output resistance and better isolation between the input and output, compared to a single transistor LNA, at the expense of a slightly higher voltage requirement. Similar to the LNA in the previous section, equations (3.1) and (3.2) were used when designing the LNA in Fig. 3.28, in order to ensure input matching with resonance at 5.8GHz. Since the IEEE 802.11a standard is defined for both the 5.15-5.35GHz and the 5.725-5.825GHz ranges, switching capacitors formed by transistors M5 & M6 and capacitors C1 & C2 are used to allow the LNA to operate at 5.2GHz as well. By setting the external control voltage, v_{tune}, to high, transistors M5 and M6 are turned on. As a result, the capacitors in series with the transistors are connected to signal ground, instead of being floating, thus lowering the operating frequency of the

LNA from 5.8GHz to 5.2GHz.

The LC tank, formed by inductor L7 and capacitor C4, behaves as a DC current source. The advantage of using such an approach is to provide the necessary DC bias current, without requiring a voltage headroom, while presenting a high impedance to the RF signal, and presenting a lower impedance to the out of band signals resulting in suppressing them.

B. Active mixer

An active mixer similar to the one described in Section 3.2 is used to implement the first down conversion stage. For the LC loads of the mixer, on-chip components are used and tuned to resonate at 2.75GHz.

C. Passive mixer

Since the active mixer provides additional gain after the LNA, the magnitude of the output after the first stage of downconversion is relatively large. Thus, the second stage mixer needs to be of higher linearity compared to that of the first stage. As described in Section 3.2.1D, although passive mixers have no gain and may even introduce loss, they are more linear than active mixers. The other advantage of using a passive mixer is that it does not consume any DC power. Thus, a passive mixer is used for the second

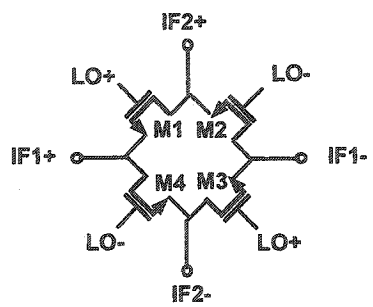


Fig. 3.29: Schematic of the passive mixer.

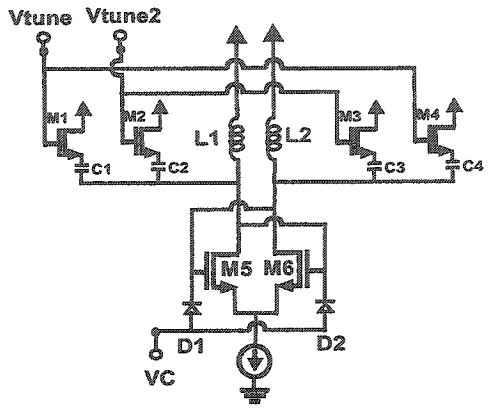


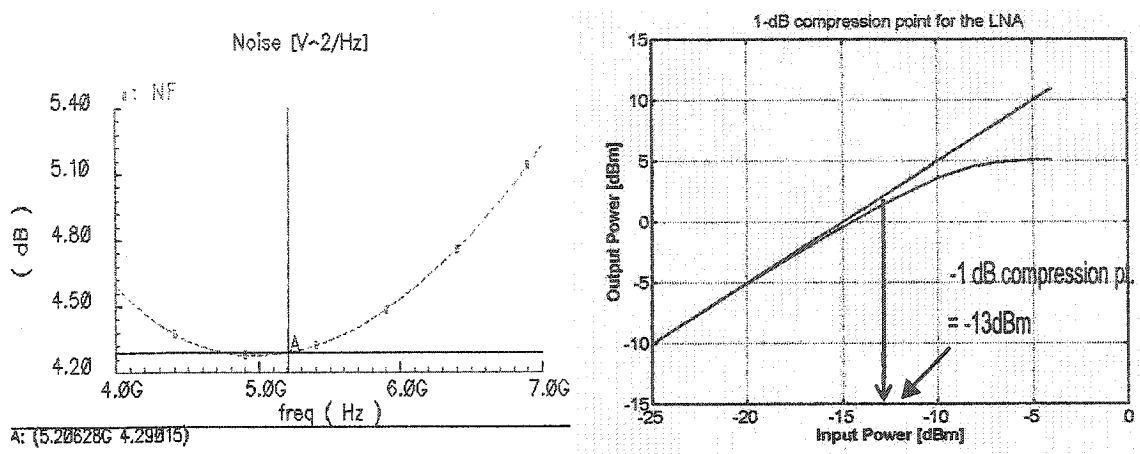
Fig. 3.30: Schematic of the core LC oscillator.

downconversion stage (Fig. 3.29).

The main task in designing a passive mixer is to determine the sizes of the four transistors M1 to M4, since the noise figure, linearity, and the conversion gain all depend on the widths of these transistors. Qualitatively, as the widths of the transistors increase, linearity improves due to the decrease of the series resistances of the transistors. However, the noise figure increases because of the increase in the parasitic capacitances. Finally, the conversion gain decreases as the series resistances decrease. As a result, the design of the widths of the transistors is a trade-off between noise, linearity and conversion gain. Apart from the widths of the transistors, the performance of a passive mixer also depends on the biasing conditions of the transistors and the amplitude of the LO signal.

D. Voltage-controlled oscillator

Two pairs of cross-coupled LC oscillators similar to those in Fig. 3.7 are used. Since from the measurement results of the first receiver prototype, varactors were found to only provide 5% of tuning, two switching capacitors are included in this design, in order to



(a) (b)

Fig. 3.31: Simulated LNA (a) noise figure (b) 1-dB compression point.

increase the tuning range to 10%, i.e. from 2.5GHz to 3GHz. Figure 3.30 shows the modified core LC oscillator circuitry.

In order to oscillate both at 2.6GHz and 2.9GHz, one set of capacitors (C2 and C3) is double the size of the other set (C1 and C4), providing different frequency tuning steps. The capacitors are implemented as to maintain a constant quality factor: the widths of the switching transistors in series with the capacitors are appropriately sized. For example, transistors M2 and M3 are double the size of M1 and M4, resulting in smaller series resistances.

3.3.2 Simulation results

HSPICE and SpectreRF were used to simulate the performance for each individual component of the receiver. Figure 3.31 shows that the noise figure and 1-dB compression point for the LNA are 4.2dB and -13dBm, respectively. As for the passive mixer, the noise figure and 1-dB compression point are 13dB and 0dBm, as shown in Figure 3.32. For the active mixer and the quadrature VCO, they have similar performance as those

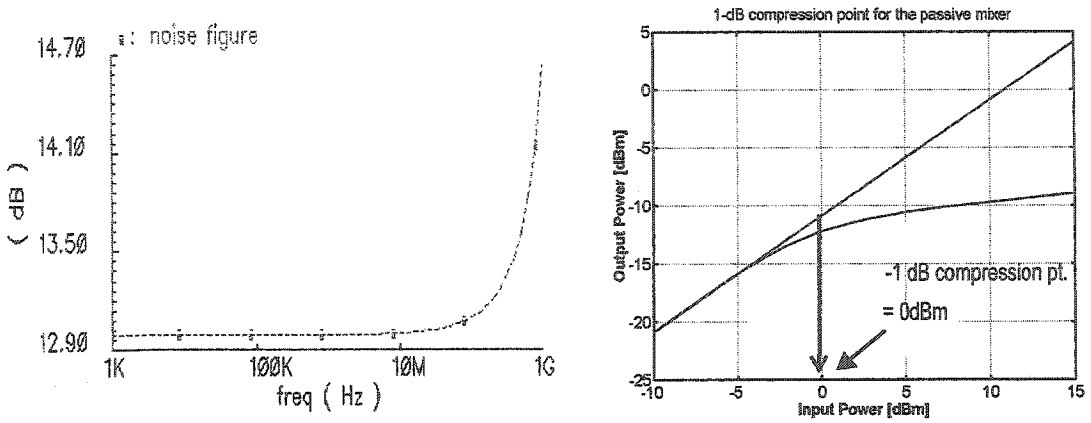


Fig. 3.32: Simulated passive mixer (a) noise figure (b) 1-dB compression point.

reported for the first receiver prototype, except that the conversion gain of the active mixer is 0 dB instead of 10dB, since low quality factor on-chip components are used here, as opposed to the off-chip LC tank in the previous receiver. Table 3.5 summarizes the LNA and mixers simulation results for the image-reject receiver.

To verify the overall performance of the receiver, HP ADS is used. A setup similar to that shown in Fig. 3.12 was used. It predicted an overall noise figure and a 1-dB compression point of 7.5dB and -16.5dBm, respectively.

LNA		
Operating Freq.	5.2GHz	5.8GHz
Power consumption	15mW	15mW
Noise figure	4.2dB	4.4dB
S_{11}	-13 dB	-13 dB
1dB compression	-12dB	-12dB
Voltage gain	10 dB	15 dB

Active Mixer	
Power consumption	20mW
SSB noise figure	16dB
1dB compression	-8dB
Conversion gain with load	0dB

Passive Mixer	
Power consumption	0 W
SSB noise figure	13dB
1dB compression	0dB
Conversion gain with load	-5dB

Table 3.5: Receiver components simulation results.

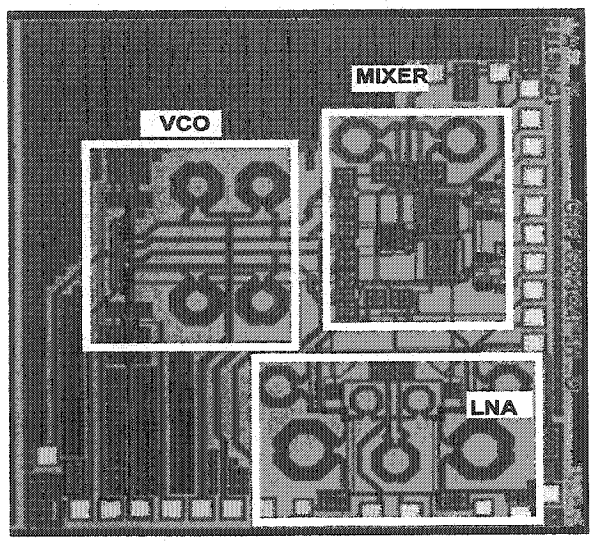


Fig. 3.33: Image-reject receiver chip.

3.3.3 Measurement results

The image-reject receiver frontend was fabricated in a standard 0.18 μm CMOS technology from TSMC, and packaged in a CFP80 package provided by the Canadian Microelectronics Corporation (CMC). Figure 3.33 shows the micrograph of the chip, with an area of 2.2mm x 2.3mm.

Similar to the procedure for the previous receiver, a custom printed circuit board (Fig.

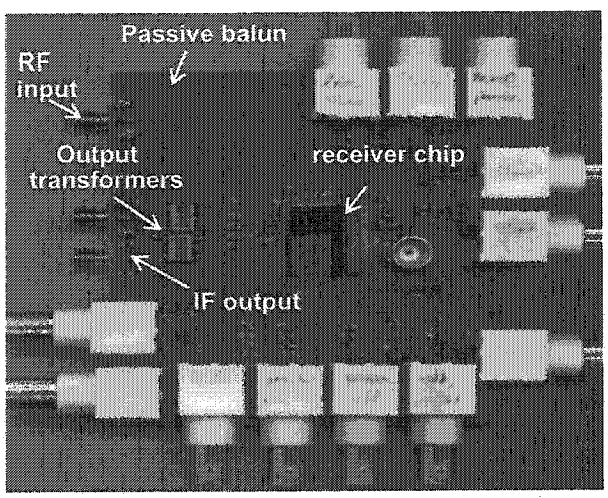


Fig. 3.34: Text fixture for the image-reject receiver.

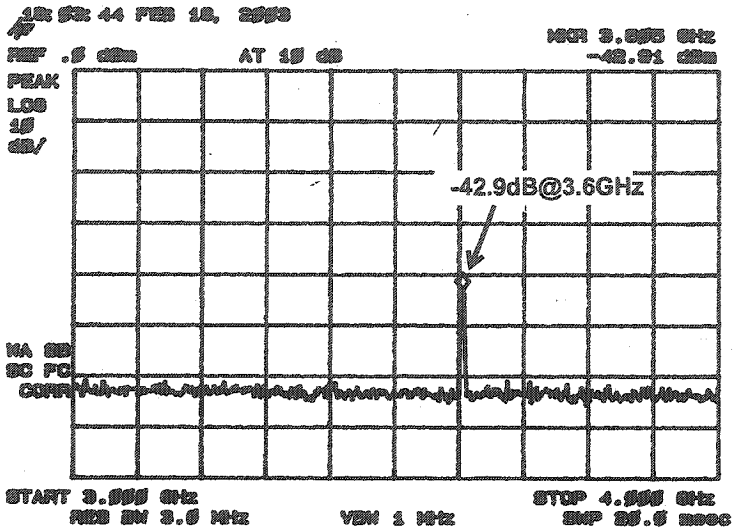


Fig. 3.35: Measured LO leakage for the receiver at 3.6GHz, with all switching capacitors turned off.

3.34), with a hybrid balun to generate the differential RF inputs, was built to test the chip. The VCO leakage is measured first in order to verify that the VCO is functional. Figure 3.35 shows that the VCO oscillates at 3.6GHz under a 1.8V supply, without turning on any of the switching capacitors. With the help of the switching capacitors and the varactors, the VCO can be tuned down to 3GHz (Fig. 3.36).

The next step is to test the whole receiver. A frequency sweep of the input reveals that the LNA operates in the range from 6.2GHz to 6.8GHz. In order to accurately determine the gain of the receiver, the new test fixture has to be calibrated, following the same steps described in section 3.2.3. Table 3.6 summarizes the losses due to the entire test fixture.

Each pin of the CFP80 package @ 6.5GHz	-4.5dB
RF part of the PCB in the 6.5GHz range	-8dB
IF transformer @30MHz	-1dB
Connection cables and connectors @6.5GHz	-3.5dB
Total	-17dB

Table 3.6: Losses due to the test fixture for the second receiver.

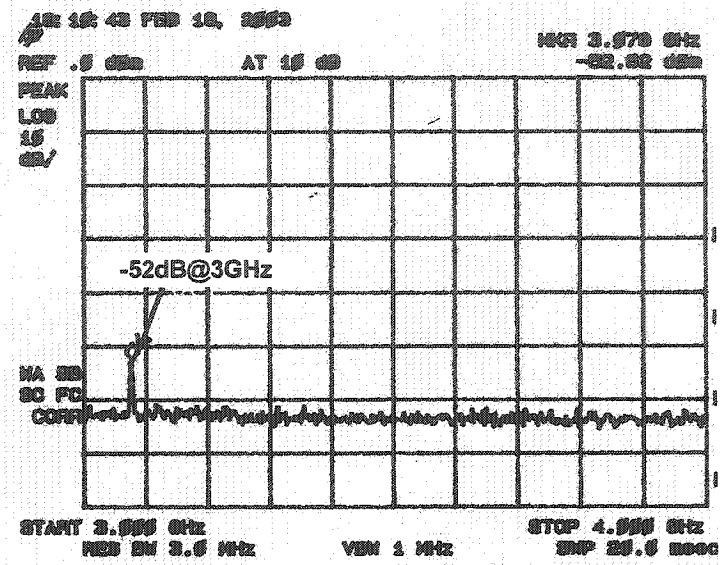


Fig. 3.36: Measured LO leakage for the receiver at 3GHz, with all the switching capacitors turned on, and the varactors at maximum setting.

Figure 3.37 shows the second IF output of the receiver at 20MHz, with a -15dBm input RF signal at 6.8GHz, and the VCO tuned to around 6.8GHz. Taking into account the losses of the test setup (17dB), and the losses due to the passive mixer (5dB), the overall gain of the receiver is estimated to be 12.88 dB. With the switching transistor of

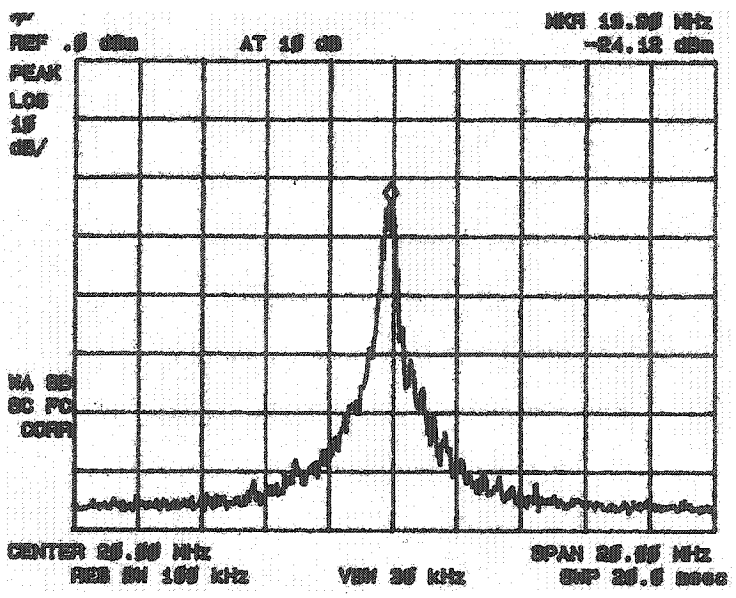


Fig. 3.37: Measured second IF output for a 6.8GHz input RF signal.

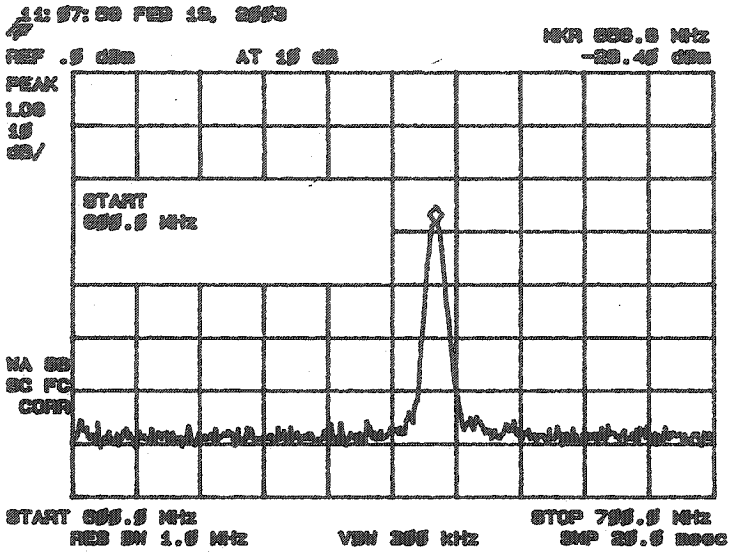


Fig. 3.38: Measured second IF output for a 6.2GHz input RF signal.

the LNA turned on, Fig. 3.38 shows the frequency response of the receiver with a 6.2GHz RF input and the VCO at 6.8GHz, maintaining the same LO drive input for the mixers. The second IF signal drops by about 4dB, when compared to Fig. 3.37. This is attributed to the switching capacitors: when included into the LC tank of the LNA, they introduce extra parasitics and lower the overall quality factor of the tank.

A sliding capacitor is used for input matching, as described in Section 3.2.3.

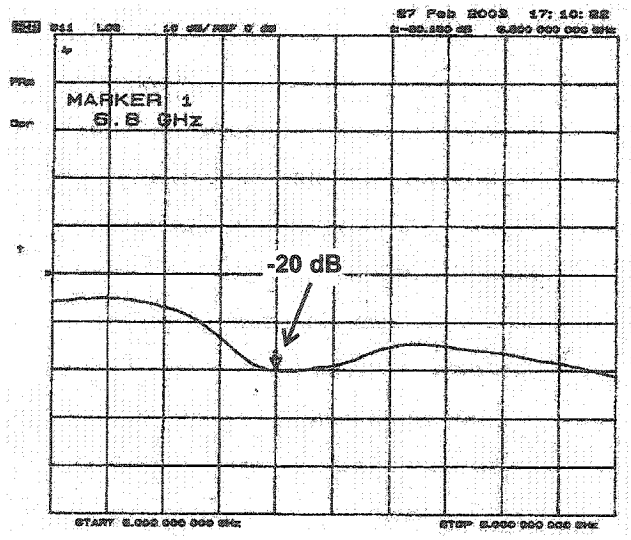


Fig. 3.39: Measured input reflection of the receiver.

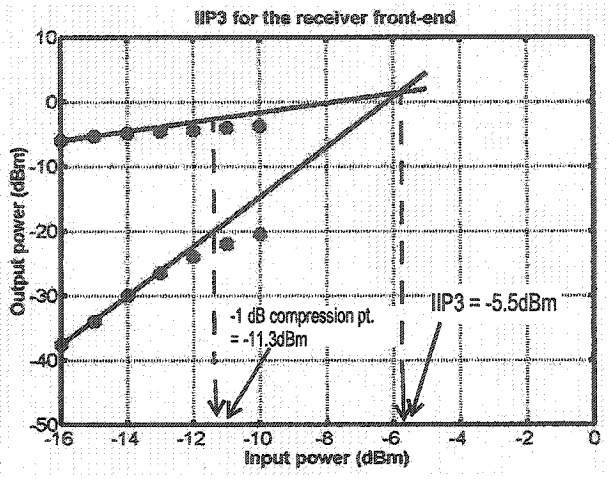


Fig. 3.40: Measured third-order intercept plot for the image-reject receiver.

Figure 3.39 shows that the measured input reflection coefficient, S_{11}, of the receiver at 6.8GHz is -20dB. As for the third-order intercept point and 1-dB compression point of the receiver frontend, they are -5.5dBm and -11.3dB respectively, as shown in Fig. 3.40.

As mentioned earlier, the amount of image rejection is mainly limited by the substrate feedthrough. Figure 3.41 shows an output power of -46dBm for an image signal at 125MHz. Taking into account the losses due to the test setup, the image rejection ratio of the receiver is estimated to be 45dB. Table 3.7 summarizes the measured performance of

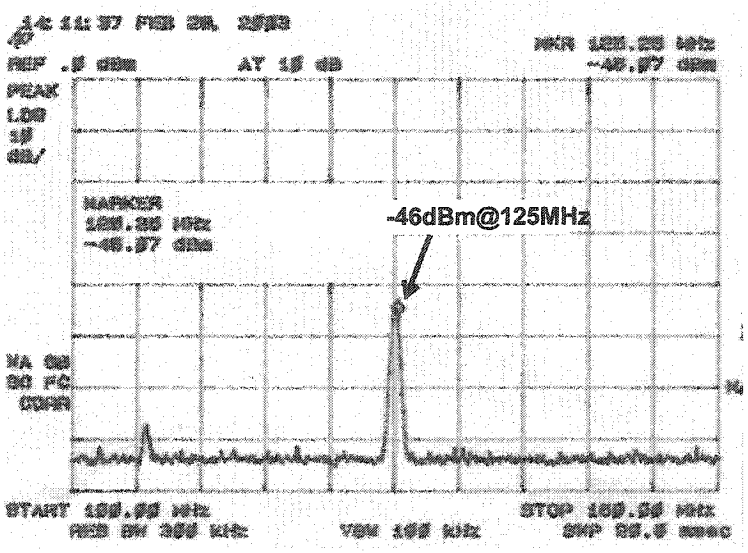


Fig. 3.41: Measured frequency response for an image signal.

Overall gain including the passive mixer (50Ω system)	8 dB
Image Rejection Ratio (IIR)	45 dB
Overall noise figure (simulation)	7.5dB
Input S_{11} @ 6.8 GHz	-20dB
IIP3	-5.5dBm
Input 1-dB compression	-11.3dBm
VCO tuning range (%)	15%
Power dissipation @ 1.8V	85mW
Die size (0.18 μm CMOS process)	5.06mm^2

Table 3.7: Summary of measured receiver performance.

the receiver.

There is a discrepancy between the operating frequencies obtained from simulation and the measurements. This is attributed to an unfortunate mistake that was made when designing all the inductors used in this receiver. The smaller inductors that was used in the design resulted in higher operating frequencies. With the correct inductors values, the prototype would have operated at the originally desired 5-6 GHz frequency range instead of 6-7GHz. Nevertheless, since the sizes of all inductors were over-estimated by the same percentage, all responses were shifted upwards by the same ratio, resulting in a fully functional CMOS receiver frontend.

3.3.4 Conclusion

In this section, we have designed and tested an image-reject receiver with tuning capability for both the LNA and the VCO. It operates in the 5-6GHz range. With careful frequency planning, it was possible to provide a high image-rejection ratio (45dB), while

using less components compared to other image-rejection architectures, such as the Weaver architecture or the superheterodyne architecture.

Chapter 4: Integrated Transformers

4.1 Introduction

Recently, monolithic transformers have been used in various RF systems, implemented on bipolar or GaAs substrates, for single-ended-to-differential conversion (e.g. [27]). As the operating frequencies of circuits increase, integrated transformers will find more and more applications, such as impedance transformation [27], replacement of inductors for higher quality factors [28], signal coupling [29], etc. With the increasing popularity of using CMOS technology for RF circuitry, the performance of the integrated transformers must be thoroughly understood, in order to make intelligent use of these passive device.

As shown in subsequent sections in this chapter, integrated transformers share similarity to inductors, since both are made up of a set of microstrips. Because our in-house inductor modeling tool, MIND [14], is based on transmission-line models, that is each strip of the inductor is modelled by an RLC π-model, it was straight forward to expand MIND to be able to model integrated transformers.

This chapter presents a qualitative study of silicon integrated transformers, and then describes the expansion of MIND. We conclude with a comparison between

measurements from several prototypes and the modeling done by the extended MIND engine. The transformers were fabricated using 0.18 μm and 0.25 μm CMOS technologies from the Taiwan Semiconductor Manufacturing Company, TSMC.

4.2 Characteristic of silicon transformers

4.2.1 Transformers fundamentals

An integrated transformer can be viewed/implemented as two intertwined inductors, as shown in Fig. 4.1. There are three important parameters that determine the performance of a transformer:

1. The self-inductance of the primary inductor, L_1.
2. The self-inductance of the secondary inductor, L_2.
3. The mutual inductance between the primary and the secondary inductor, M.

The performance of a transformer is usually evaluated by the strength of the magnetic

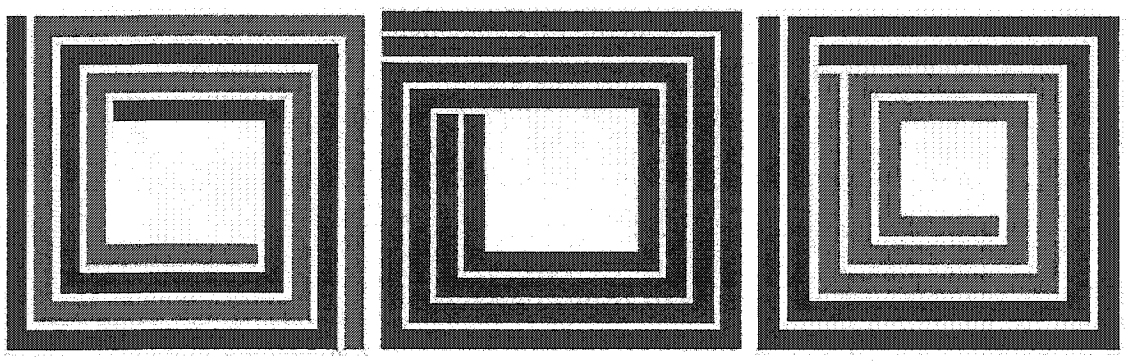


Fig. 4.1: Common transformer configurations (a) interleaved (b) parallel winding (c) concentric.

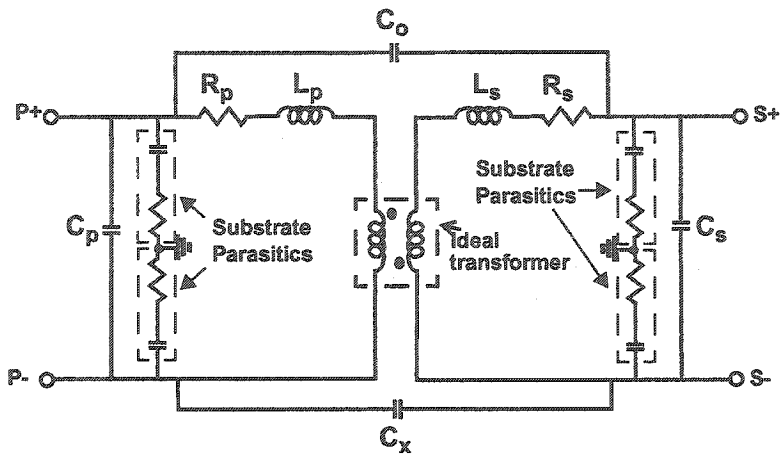


Fig. 4.2: Transformer model.

coupling between the primary and secondary inductors, as indicated by the k-factor:

$$k = \frac{M}{\sqrt{L_1 L_2}} . \tag{4.1}$$

A typical value for the k-factor for on-chip transformers is between 0.3 to 0.9. It depends on the transformer topology (Section 4.2.3), and the material used in implementing the transformer. The material determines the magnetic properties of the technology. For a transformer with perfect coupling, the k-factor is 1 (unity). For two inductors with no coupling, the k-factor is zero.

Figure 4.2 shows a lumped-element model for on-chip transformers [12]. At the core of the model is an ideal transformer, while the other components represent parasitics and leakage effects. L_p and L_s account for the leakage of the magnetic flux between the two windings, while C_p, C_s, C_o, and C_x model the different interwindings capacitances. R_p, and R_s represent the ohmic losses in the windings.

4.2.2 Performance description

Unlike inductors, which are described by their quality factors and inductances, transformers are often described/characterized by their S-parameters. S_{11} determines the amount of signal reflection, while S_{21} represents the amount of signal coupled from the primary to the secondary windings. Depending on the application, a high coupling transformer is desired in single-ended to differential converters, while peaking coils for high-performance broadband amplifiers require a low coupling factors transformers [30].

4.2.3 Common transformer topologies

Similar to inductors, integrated transformers are constructed using conducting strips intertwined in the same plane, or overlaid as stacked metal. Many of the methods used to improve the performance of integrated inductors can be used for transformers; for example, the addition of a patterned ground shield to minimize substrate losses resulting from electromagnetic energy coupling to the substrate.

Figure 4.1 shows three common topologies for silicon transformers. While both the parallel winding (Fig. 4.1b) and interleaved transformers (Fig. 4.1a) have similar properties, the latter provides a symmetric geometry, and thus the electrical parameters of the primary and secondary windings would be the same, if the same number of turns is used on both ends. When compared with the concentric transformer (Fig. 4.1c), the interleaved design allows more mutual coupling between the two windings, and thus its k-factor is higher. The focus in this thesis is on the interleaved transformer, but the modeling techniques adopted can be used for modeling other transformer structures.

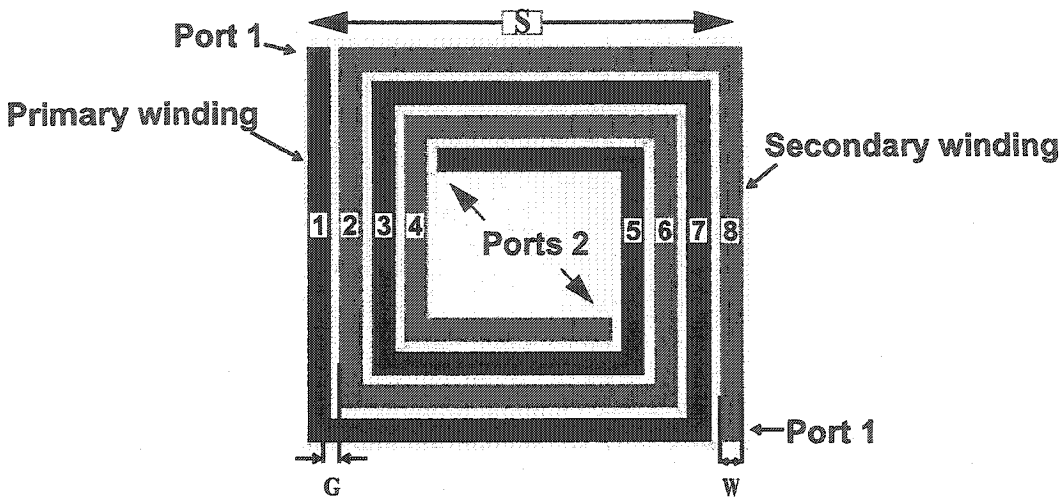


Fig. 4.3: Transformer parameters.

4.2.4 Physical parameters

As for inductors, transformers can be described by four main layout parameters (Fig. 4.3):

1. The number of turns *N* for each winding, which can be a decimal number when partial turns are used. In Fig. 4.3, *N* is equal to 2.
2. The width *W*, expressed in μm, of the microstrips.
3. The gap *G*, expressed in μm, between adjacent strips.
4. The outside length of the inductor *S*, expressed in μm.

4.3 Transformer modeling approach

Since an integrated transformer can be viewed as consisting of two inductors, the modeling is implemented using the lumped π-models generated by MIND, when estimating the self-inductances of the primary and secondary windings. Since the π-

model generated by MIND also accounts for the substrate parasitics, the remaining task is to include the mutual inductances and leakage inductances between the two windings.

There are two steps in modeling a transformer: 1) synthesis, and 2) model fitting. Based on the transformer physical parameters, that is N, W, G, and S, a netlist that emulates the S-parameters of the transformer is produced. Next, by fitting the S-parameters from simulation or from measurements, a model like the one shown in Fig. 4.2, can be generated for later use in circuits simulations.

4.3.1 Netlist extraction

In this sub-section, the steps involved in constructing a netlist from the physical dimensions of the transformer are discussed.

1. The self-inductances of both the primary and secondary windings are obtained from the MIND engine, which also include the oxide capacitances, as well as the substrate resistances and capacitances.
2. The equations that are used in calculating the mutual inductance, between two windings are similar to those used in the original MIND program for finding the mutual inductance between the inductor's strips. There are two types of mutual inductances: positive and negative mutual inductances. As shown in Fig. 4.3, strips 2 to 4 will generate positive mutual inductances to strip 1, since the currents flowing through those strips are all in the same direction. On the other hand, strips 5 to 8 will induce negative mutual inductances to strip 1, since their currents flow is the opposite direction. The mutual inductance effect is modeled by a voltage-dependent current source.
3. All the above effects are modeled by a circuit netlist. After AC simulation, the S-

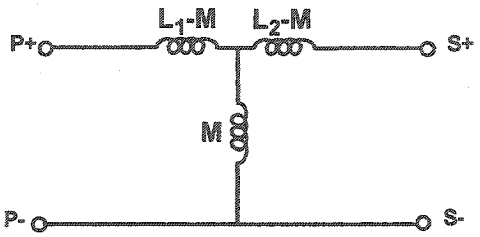


Fig. 4.4: T-section model for an ideal transformer.

parameters of the circuit are obtained (Section 4.3.2). Similar to the method of finding the equivalent inductor model used by the MIND engine, the results are then imported in MATLAB to be fitted to a chosen transformer model as described in the following section.

4.3.2 Compact model generation

The compactness and reasonable accuracy of the transformer model (Fig. 4.2) provide for an efficient means to take into account the practical behavior of transformers in circuit simulation. In modeling the ideal transformer in Fig. 4.2, the T-section of Fig. 4.4 is used to account for the mutual coupling between the windings [12]. L_1, L_2, and M are the self-inductances of the primary and secondary windings, and the mutual coupling inductance, respectively. As a result, this model is only valid for AC signals and not for DC, since there is no isolation between the DC currents in the primary and secondary windings. A compact model for a transformer can be created either from simulation or from actual measured data. In both cases, S-parameters describing the transformer as a two-port network (Fig. 4.5) are fitted to the model in Fig. 4.2, using a mathematical tool such as MATLAB. When no measured data are available, the complex netlist obtained as described in the previous section is used to generate the estimated S-parameters of the

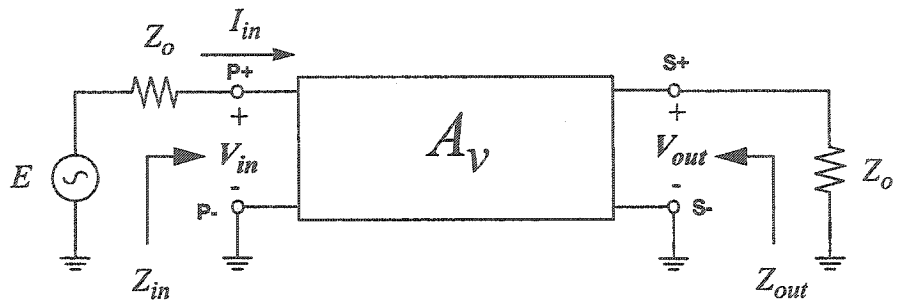


Fig. 4.5: Equivalent circuit for S-parameter evaluation.

transformers. Referring to Fig. 4.5, the following equations are used to obtain the S-parameters from AC simulation:

1. From its standard resistor-based definition, the reflection coefficient, S_{11}, may be expressed as:

$$S_{11} = 2 \cdot \frac{V_{in}}{E} - 1, \tag{4.2}$$

where E and V_{in} are the signals from the generator and the signal after Z_o respectively (Fig. 4.5).

2. The transmission coefficient S_{21} definition is given by:

$$|S_{21}| = \frac{2|V_{out}|}{|E|}, \tag{4.3}$$

where V_{out} is the voltage at the output (Fig. 4.5).

Using equations (4.2) and (4.3), the S-parameters of the lumped-element model can be derived symbolically, assuming that ports P- and S- in Fig. 4.5 are connected to ground (Fig. 4.6), as described in Appendix B.

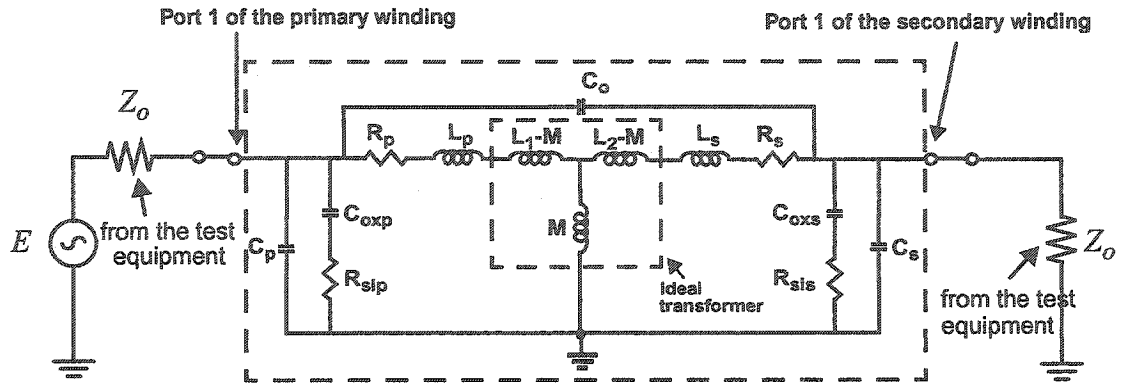
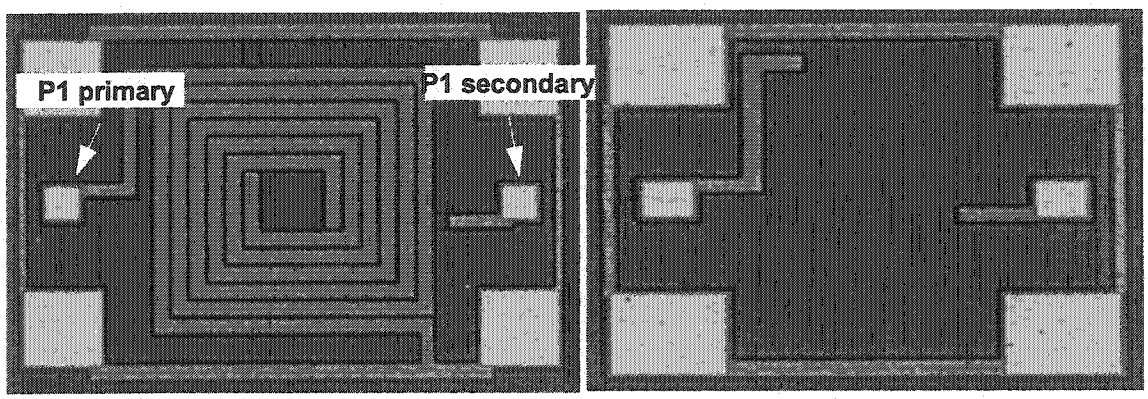


Fig. 4.6: The complete lumped-element model for a transformer.

4.4 Simulation and measurement results

In order to verify the accuracy of the transformer modeling developed, several transformers were implemented and characterized in 0.18 μm and 0.25 μm CMOS technologies. All the transformers use the top metals in the technology, that is metal 6 for the 0.18 μm technology and metal 5 for the 0.25 μm technology, in order to minimize losses to the substrate. Since a transformer is a 4-port device, port 2 from each winding was grounded in the fabricated prototypes, in order to facilitate the measurements. The



(a) (b)

Fig. 4.7: Micrograph of a transformer prototype (a) sample transformer test structure (b) calibration structure.

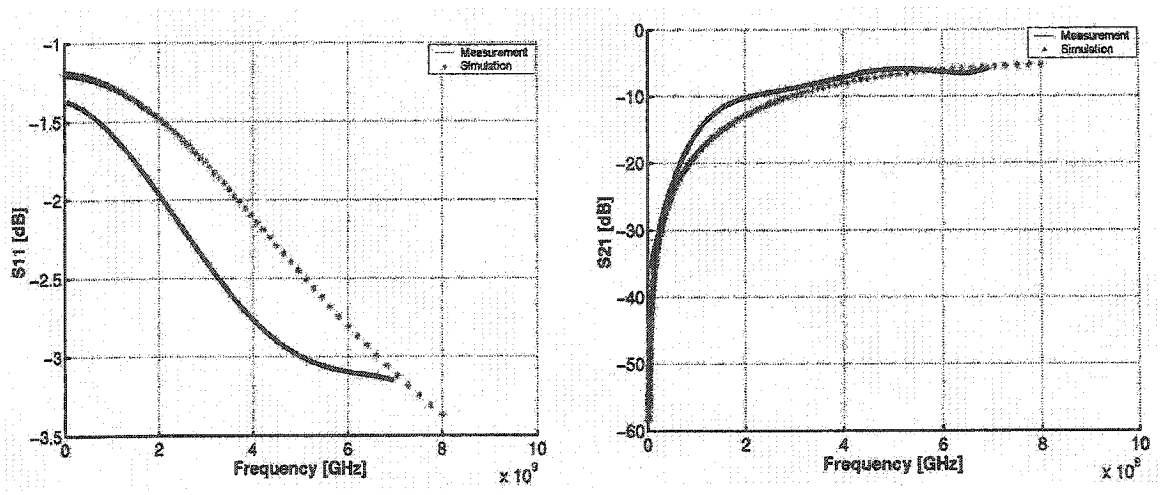
lumped-element model in Fig. 4.2 is thus simplified to that in Fig. 4.6, with the T-model accounting for the ideal transformer. Port 1 of each winding is connected to a pad, as shown in Fig. 4.7a.

4.4.1 Measurement procedure

The transformer measurements were done using a Vector Network Analyzer via on-chip probing. A Short-Open-Through-Load (SOLT) calibration technique was used. The measured S-parameters were deembedded by measuring the frequency response of an empty test setup (Fig. 4.7b).

4.4.2 Comparing MIND modeling to measurements

In the following, different transformer parameters are varied, and the measurement results are compared to the expected performance obtained from MIND. Comparison is done using the S_{11} and S_{21} parameters versus frequency. In addition, transformer models



(a) (b)

Fig. 4.8: Transformer response in a 0.25μm CMOS technology, N=2, W=15μm, G=0.8μm, S=210μm (a) S_{11} (b) S_{21}.

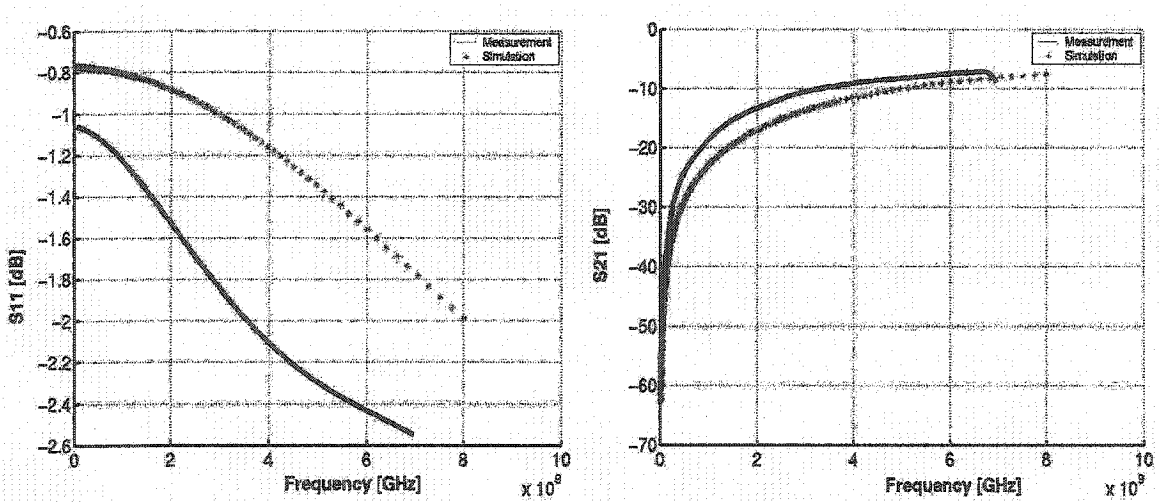
(Fig. 4.6) are generated from the measured data in order to investigate the effect of different transformer parameters on the k-factor coupling coefficient.

A. Standard transformer

Figure 4.8 shows the simulated and measured S_{11} and S_{21} of a specific transformer (with standard layout parameters). It can be seen that the S_{11} has around 0.5 dB to 1 dB discrepancy, while S_{21} has around 1 dB to 4 dB difference, from 0.5 GHz to 7 GHz. The discrepancy is the least between 5 GHz and 7 GHz. This is because the lumped model used are "narrow-band", and thus only valid for a specific range of frequencies. Our routines were optimized for this range of frequency, which is of interest nowadays to us ([26], [33],[34]) and to other researchers ([2]-[9]).

B. Transformers with wider metal

Increasing the widths of the metal strips of a transformer, result in decreasing the S_{21}. Compare S_{21} of Fig. 4.8b and Fig. 4.9b. As the width increases, the magnetic flux



(a) (b)

Fig. 4.9: Wide metals transformer characteristics in a 0.25μm CMOS technology, N=2, W=20μm, G=0.8μm, S=210μm (a) S_{11} (b) S_{21}.

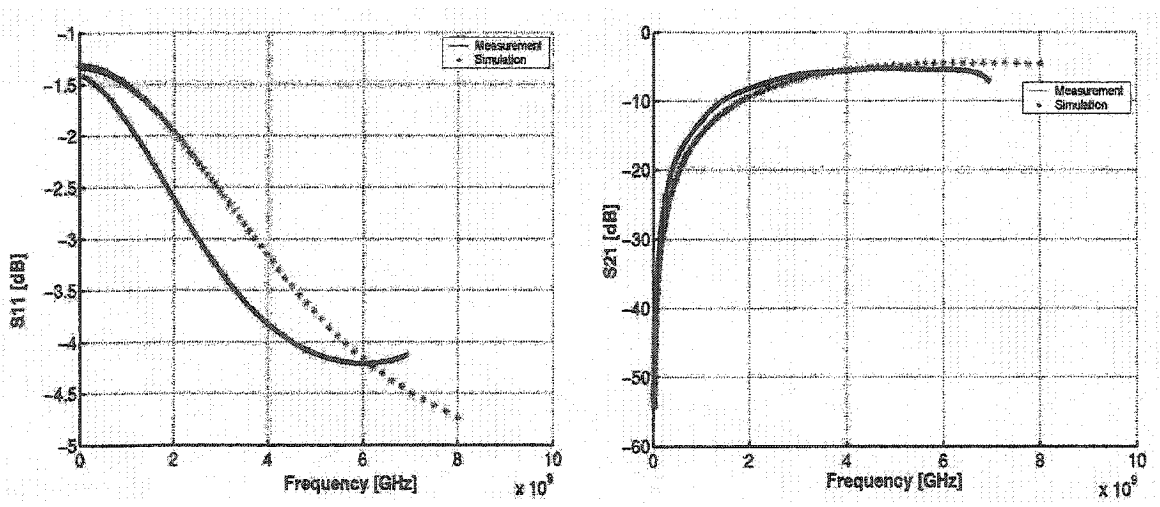
between the windings decreases. Similar to the previous case, the discrepancy in S_{11} is around 0.5 dB to 1 dB, and S_{21} has around 1 dB to 4 dB difference from 0.5 GHz to 7 GHz.

C. Large transformers

As the external dimensions of the transformer increase from 210 μm to 300 μm, the S_{21} increases, as shown in Fig. 4.10, for both measurement and simulation. In this case, there is more area to couple the energy from the primary to secondary windings.

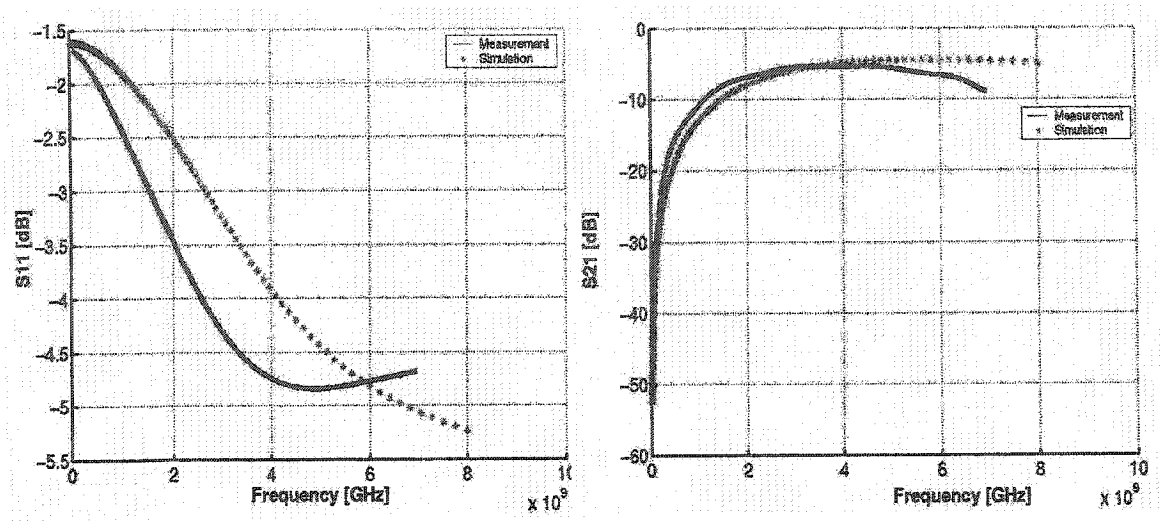
D. Many turns transformers

As the number of turns increases from 2 to 3, the S_{21} also increases (Fig. 4.11). Again, because the area for energy coupling increases.



(a) (b)

Fig. 4.10: Large transformer characteristic in a 0.25μm CMOS technology, N=2, W=20μm, G=0.8μm, S=300μm (a) S_{11} (b) S_{21}.



(a) (b)

Fig. 4.11: Many turns transformer characteristic in a 0.25μm CMOS technology, N=3, W=20μm, G=0.8μm, S=300μm (a) S_{11} (b) S_{21}.

E. Effects on k-factor

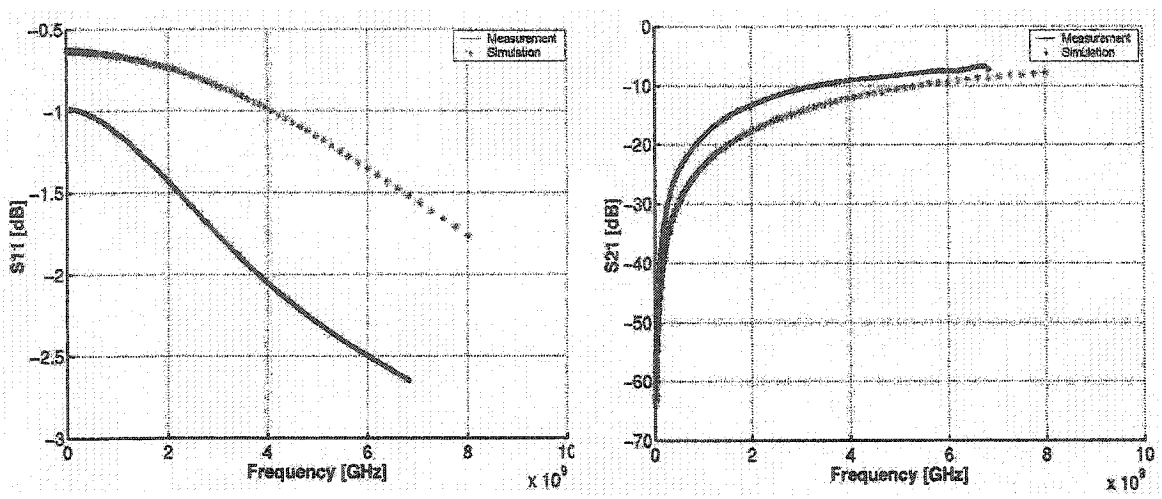
Table 4.1 shows the components values for the lumped-element model (Fig. 4.6) for the transformer in Fig. 4.8. Table 4.2 shows the effect of changing different transformer parameters on the k-factor. As the area and the number of turns of a transformer increase, more energy is coupled from the primary to the secondary winding, which corresponds to

Transformer	L_1	M	L_p	C_{oxp}	R_{sip}	C_p	C_s	C_o
Fig. 4.8	1.35 nH	0.81 nH	0.05 nH	10 pF	73 Ω	10 pF	10 pF	81 pF

Table 4.1: Components values for the transformer in Fig. 4.8.

Transformer	primary winding self-inductance	mutual coupling inductance	k-factor
Fig. 4.8	1.35 nH	0.81 nH	0.59
Fig. 4.9	1.05 nH	0.53 nH	0.50
Fig. 4.10	1.80 nH	1.14 nH	0.63
Fig. 4.11	2.26 nH	1.5 nH	0.66

Table 4.2: Different transformers k-factors.



(a) (b)

Fig. 4.12: Transformer characteristic in a 0.18μm CMOS technology, N=2, W=20μm, G=0.8μm, S=210μm (a) S_{11} (b) S_{21}.

a higher k-factor.

F. A transformer in a 0.18 μm CMOS technology

Figure 4.12 shows the S-parameters response for a transformer implemented in a 0.18μm CMOS technology. The transformer has the same layout parameters as the transformer in Fig. 4.9 which was implemented in the 0.25μm CMOS technology. Both transformers have similar S_{11} and S_{21} responses.

Chapter 5: Conclusion

This thesis has demonstrated that CMOS technologies constitute potential alternatives for high frequency RF applications over traditional RF processes, such as bipolar and GaAs. By using CMOS technologies in RF designs, higher level of integration with the baseband circuitry is made possible, resulting in lower cost and simplified packaging.

One of the objectives of this thesis was to explore the feasibility of using CMOS technologies to implement RF circuitry at 5 GHz. In Chapter 1, an overview of state-of-the-art RF receivers frontends at 5GHz, and a review of current transformer modeling programs, were presented. The motivation and contributions of this thesis were also discussed.

In Chapter 2, the performance parameters for evaluating a receiver frontend were presented, followed by a discussion of common receiver architectures. The two-IF downconversion architecture was discussed, showing that it can have superior performance compared to other architectures.

In Chapter 3, two RF receiver frontends operating in the 5GHz range were presented. With folded cascode structures, CMOS circuitry was operated at 0.8V supply, and a decent image rejection ratio was obtained, without the use of any special image reject filters. Through a second prototype and careful frequency planning, a two-IF

downconversion architecture using DC blocking capacitors was demonstrated to achieve very high image rejection (45dB).

Apart from exploring RF active circuitry, Chapter 4 discussed the modeling of on-chip transformers operating at multi-GHz frequencies. The in-house inductor modeling program, MIND, has been enhanced to include transformer modeling. It has been verified through measurements. Lumped element models can now be generated from the program in order to enable circuit simulation with transformers.

Appendices

Appendix A: S-Parameters for Narrowband RLC Modeling

The following set of equations describe the S-parameters of port 1 of the narrowband model of a transformer, as a function of its RLC components.

Using the setup of Fig. A.1, with port 2 of both windings connected to ground, the following equations were derived from Eq. (4.2) and Eq. (4.3):

$$S_{11} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o}, \tag{B.1}$$

$$|S_{21}| = \frac{2Z_3 Z_{in}}{(Z_{in} + Z_o)Z_A}\left(\frac{Z_2 A + Z_4 A + Z_4}{Z_2 + Z_3 + Z_4}\right), \tag{B.2}$$

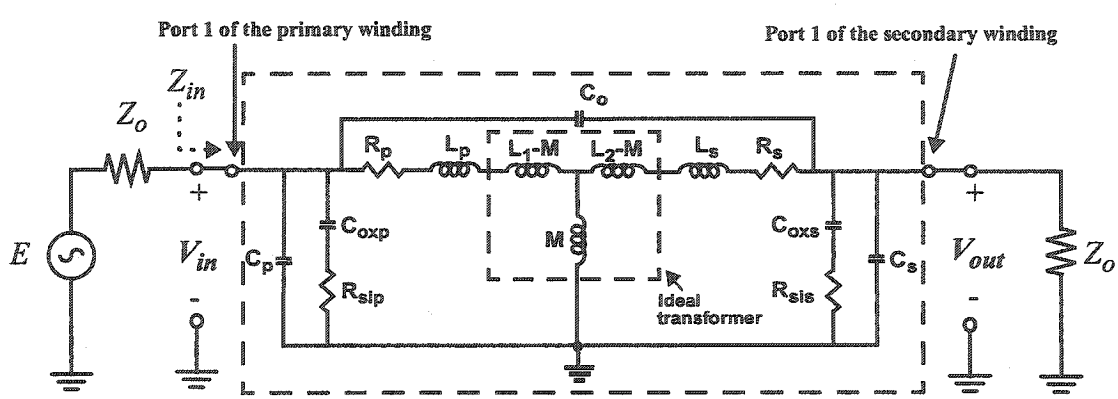


Fig. A.1: Narrowband model S-parameters extraction setup.

where $Z_{in} = \dfrac{1}{\dfrac{1}{Z_A} + \dfrac{1}{\dfrac{1}{sC_{oxp}} + R_{sip}} + sC_p}$,

$$Z_A = (2Z_1 + Z_4)A + Z_4\left(\frac{Z_2A - Z_4A + Z_4}{Z_2 + Z_3 + Z_4}\right) - (Z_1 + Z_4),$$

$$A = \frac{\left(\dfrac{Z_2Z_4}{Z_2 + Z_3 + Z_4}\right) - Z_1}{Z_5 - 2Z_1 + Z_2 - Z_2\left(\dfrac{Z_2 - Z_4}{Z_2 + Z_3 + Z_4}\right)}, \qquad Z_3 = \frac{1}{\dfrac{1}{Z_o} + \dfrac{1}{\dfrac{1}{sC_{oxs}} + R_{sis}} + sC_s},$$

$$Z_1 = s(L_P + L_1 - M) + R_P,\ Z_2 = s(L_S + L_2 - M) + R_S,\ Z_4 = sM,\ Z_5 = \frac{1}{sC_o}$$

Appendix B: Calibration Setup for the Standalone LNA

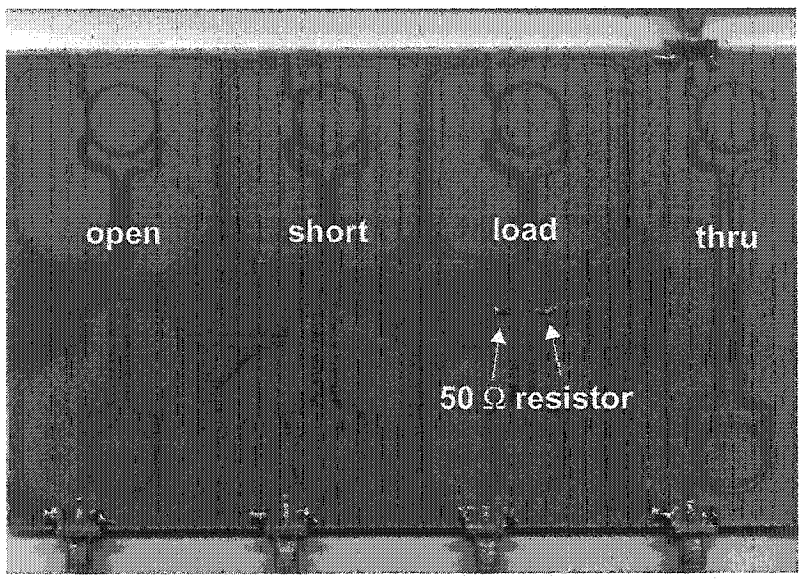


Fig. B.1: SOLT calibration fixture.

Before measuring the frequency response for the standalone LNA, calibration is performed in order to account for the effects of the test setup. Using the Vector Network Analyzer's FULL 2-port calibration functionality, a Short-Open-Load-Thru (SOLT) calibration fixture [31] was built. As shown in Fig. B.1, the calibration fixture consists of 4 structures; all the structures resemble the fixture that is actually used in measuring the device under test, except that the chip is not soldered to the PCB:

1. Short: Connected to the ground.
2. Open: An unterminated trace.
3. Load: Connect to a 50Ω resistor.
4. Thru: Both the input and the output traces are connected together.

Appendix C: Noise Measurement

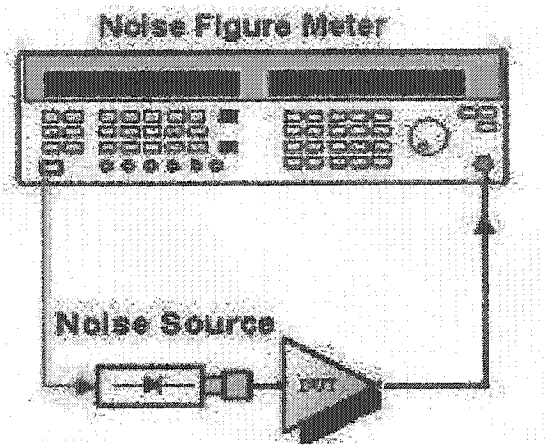


Fig. C.1: Noise measurement setup.

Figure C.1 shows the setup used for measuring the noise figure [32]. Before performing the noise measurement, the setup is first calibrated without the DUT at the frequencies of interest, to be tested in order to calibrate out any noise from the setup. Since an off-chip balun is needed to test the receiver, Fig. C.2 shows the fixture that is put after the noise source to account for the noise due to the passive balun. As shown in Figure C.2, one of the output ports of the balun is connected to a 50 Ω load, while the other one is connected to the noise figure meter in order to maintain the phase

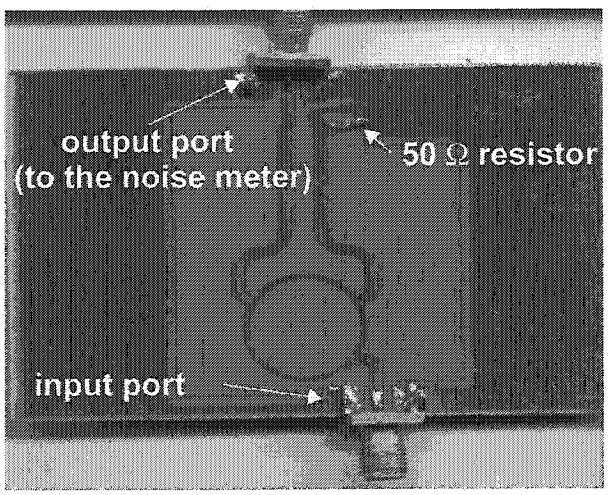


Fig. C.2: Noise measurement setup.

relationship between the two output ports.

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