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New Architectures for High-Order Bandpass Sigma-Delta Modulation in Digital-To-Analog Converters

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Abstract

Through exhaustive simulations and experimental work, this thesis investigates and develops practical solutions to efficiently perform bandpass digital-to-analog conversion using sigma-delta ($\Sigma\Delta$) techniques. Due to the robust VLSI CMOS technology, these techniques are widely used nowadays to realize high quality data converters. In particular, a novel and modular structure is proposed to implement high-order bandpass digital $\Sigma\Delta$ modulators with variable bandwidth and arbitrary resolution. Using this structure, near-optimum noise suppression is achieved even after coefficient quantization errors are introduced. In addition, high speed operation is now attained independent of the modulator order. A synthesis method is also provided which is straightforward and easy to automate. As such, the new $\Sigma\Delta$ modulator was entered into the Delta-Sigma Modulator and Oscillator Design program called DSMOD.

Because of the use of $\Sigma\Delta$ modulation, the signal band is surrounded by noise which requires post-filtering. In the second part of this thesis, a high frequency filtering approach using active inductors is examined as a potential solution to extracting the encoded information from the $\Sigma\Delta$ output bitstream. A novel floating active inductor was created. To illustrate the operation of this floating inductor, a sixth-order bandpass LC reconstruction filter was designed, built and tested on the bench.

All designs in this thesis were implemented with programmable gate arrays and/or custom -layout integrated circuits (IC) in a 0.8 μm BiCMOS process. Experimental results and measurements of these ICs will be provided.

Résumé

A l'aide de simulations et de travail expérimental, cette thèse présente une étude et développe une solution pratique pour effectuer la conversion numérique analogique à bande passante utilisant des techniques Sigma Delta ($\Sigma\Delta$). Grâce à la technologie CMOS VLSI, ces techniques sont très répandues a l'heure actuelle pour réaliser des convertisseurs de données de haute qualité. En particulier, une nouvelle structure modulaire est proposée afin de réaliser des convertisseurs a bande passante d'ordres élevés avec une largeur de bande variable et une précision arbitraire. En utilisant cette structure, une suppression quasi-optimale du bruit est obtenue même après l'introduction des erreurs dues à la quantification des coefficients. En plus, une haute fréquence d'opération est obtenue indépendamment de l'ordre du modulateur.

Du à la modulation $\Sigma\Delta$, la bande d'intérêt est entourée de bruit qu'il faut filtrer. Dans la seconde partie de cette thèse, une technique de filtrage à haute fréquence employant des inducteurs actifs est examinée comme solution potentielle pour extraire l'information encodée à la sortie du modulateur $\Sigma\Delta$. Un nouvel inducteur actif a été créé. Afin de vérifier l'opération de ce nouvel inducteur, un filtre à bande passante LC de sixième ordre a été conçu, fabriqué et testé.

Tous les désigns inclus dans cette thèse ont été réalisé à l'aide de logique programmable et/ou sur circuits intégrés dans un procédé BiCMOS 0.8 µm. Les résultats expérimentaux de ces circuits intégrés sont aussi inclus.

To my dearest parents: Mr. M. P. Leong & Mdm. K. H. Moey.

Acknowledgements

The completion of this thesis would not have been possible without the contributions of a number of selfless figures. I would like to take this opportunity to acknowledge their efforts and participation.

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Equally important were the discussions among my colleagues and the technical as well as mental support they have provided me during my "wonder years" in the MACS lab. Mr. Benoit Dufort, Loai Louis, John Abcarious, Mourad El Gamal, Vincent Leung, Ara Hajjar, Benoit Veillette, Arman Hematy, Xavier Haurie, Albert Au, Eric Mason, Victor Zia, Nilanjan Mukherjee and many more are among those who have influenced my way of scientific thinking in particular and life in general. It was with their help, advice and company that I was able to grow technically and handle any potential stress.

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Also I am very much obliged for the funding and contributions of NSERC and MICRONET. Without the fabrication service provided by CMC, the design cycle of this thesis would not have been completed.

Last but not least, I would like to dedicate this thesis to my parents, who have contributed immensely to my growth and education.

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Chapter 1 : Introduction

This chapter presents an overview of this thesis, detailing the issues behind the motivation of this work and introduces, at a high level, the bandpass digital-to-analog conversion system. Individual components and signal characteristics from the digital to the analog domains are each examined at the system level.

1.1 Motivation

With the growing importance of analog circuitry in commercial mixed-signal ICs and systems, fueled by a constant demand for lower manufacturing costs, the lack of economical, reliable and efficient analog testing methods has raised considerable interests [1] - [4] in this field of research. As an organized attempt to overcome this dilemma, a mixed-analog-digital built-in-self-test scheme was proposed in [5]. The success of this scheme relies on an on-chip analog test stimulus generator that is capable of synthesizing high quality analog signals with controllable characteristics. To simultaneously fulfil these requirements, a new category of analog oscillator using mostly digital hardware, called the ΣΔ oscillator, was proposed in [6]. Fig. 1.1 shows the proposed ΣΔ oscillator in block diagram form. This oscillator consists of two main components: an LDI resonator and a digital ΣΔ modulator. The resonator is made up of two lossless discrete integrators (LDIs), which have two registers R1, R2, and two adders. During the test phase, a ΣΔ oscillator is formed by inserting the modulator in the loop of the LDI resonator. By encoding an n-bit input signal to a one-bit output, this modulator replaces the use of an n-by-n multiplier by a 1-by-n multiplexer while performing digital-to-analog data conversion. The amplitude and phase of oscillation are digitally controlled by the initial conditions in registers R1 and R2. The coefficient k_f, on the other hand, independently sets the frequency of oscillation.

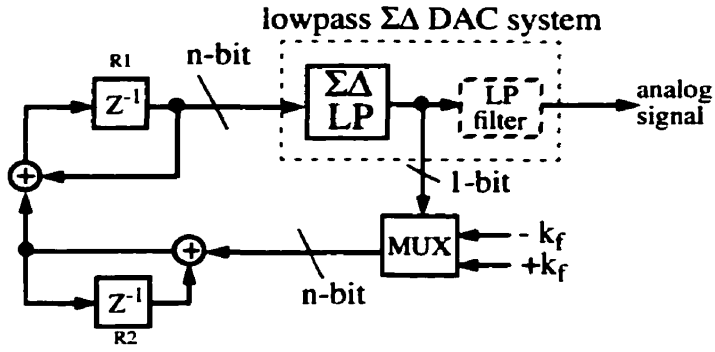


Figure 1.1: A lowpass delta-sigma oscillator in [6].

Being mostly digital in implementation, this signal generator can be verified first using more mature digital testing techniques, e.g. stuck-at-fault models, before it proceeds to excite an analog circuit-under-test (CUT). Indeed, this realization is highly desirable for analog testing application because it is insensitive to process variation, allows programmability and requires no trimming after fabrication. As an added attraction, this oscillator may involve the reuse of on-chip components, e.g. the delays and the modulator, which will further save on hardware overhead. Regardless of these advantages, this oscillator was restricted to lowpass applications due to stability limitation.

This oscillator structure was later improved in [7] in terms of speed and flexibility. Maintaining all the features mentioned previously, Fig. 1.2 shows the second generation of a ΣΔ oscillator whose functionality is now extended to cover bandpass applications. The amplitude, phase and frequency of oscillation are still controlled as before by the initial conditions and k_f. In addition, an extra coefficient, K_c, is introduced to select the frequency band

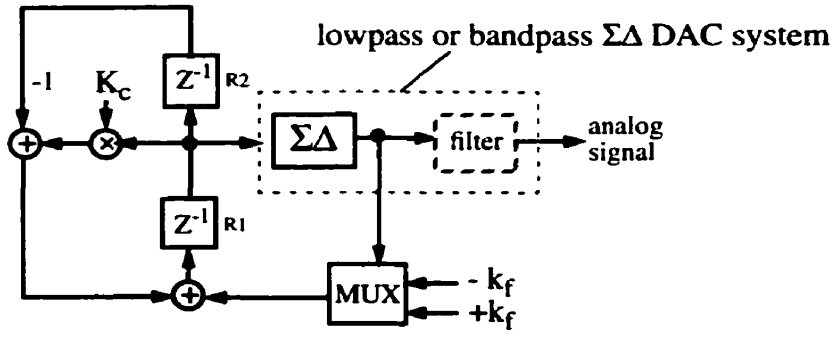


Figure 1.2: A lowpass or bandpass delta-sigma oscillator in [7].

of interest. Equivalent to the first generation, setting K_c to two results in a band centered at DC but the speed performance of this topology is enhanced. Referring to Fig. 1.1, instead of having a critical path of a cascade of two adders, the multiplexer and the modulator, the topology now has reduced the number of adders to only one. For the case when K_c is zero, the band center is shifted to a quarter of the clock frequency. Thus, a bandpass ΣΔ DAC system is required in this case.

In both [6] and [7], it is clear that the design of such a signal generator can be essentially reduced to the design of a ΣΔ D/A converter and research has since focused on finding efficient implementations of the ΣΔ modulator, in particular for high-order realizations [8]. A high-order modulator is attractive because it offers better control over the trade-off between resolution and bandwidth. Alternatively, a lower oversampling rate can be used to achieve the same resolution for a given signal bandwidth. In this case, the speed requirements on the analog hardware is relaxed [9]. It is also discovered through experiments in [7] that a stable bandpass ΣΔ oscillator requires the use of a high-order bandpass modulator so that the quantization error is not distinctly colored [10].

High-order modulators developed in [8] for lowpass and bandpass applications allow arbitrary specifications of bandwidth and resolution but fall short in high-speed operations. In those structures, the delay in the critical path increases with the modulator order. Although this shortcoming may be negligible in lowpass modulators, it is especially limiting in bandpass application requiring high speed operation since the clock frequency depends on the signal band center frequency as well as the *OSR*.

As part of this on-going research process, this thesis extends yet another effort of developing high-order ΣΔ modulator to the bandpass case, targeted at testing bandpass type devices such as those used in personal communication systems. In these applications, the need for both high-speed and high-resolution operations is readily apparent, e.g. frequency synthesizer for IF and RF applications, as well as area-efficient silicon implementations. Based on experience accumulated in previous works, Chapter 2 presents the complete process of developing a novel modular structure for efficient implementation of high-order bandpass

ΣΔ modulators. The drawbacks of using a high-order modulator, such as hardware complexity and modulator stability, are among the issues addressed in this work.

Due to the modulation scheme, the signal band is surrounded by noise. Depending on the intended signal resolution, this noise level rises rapidly beyond the signal band, up to 60+ dB above the in-band noise floor. For systems or CUTs that cannot properly handle this out-of-band noise, a post-processing step is necessary to suppress the noise before feeding the test stimuli to the CUTs. Traditionally, a passive LC ladder circuit is one of the popular methods to perform filtering due to its outstanding passband sensitivity property and its ability to handle large signal without saturation. Building on the existing LC ladder structure, a high frequency filtering approach using active inductors is examined in Chapter 3. Commonly known as a component simulation technique, this approach has made high-Q filter realizable [11] in monolithic form and serve as a potential solution to extracting the encoded information from the ΣΔ output bitstream. In Chapter 3, a novel floating active inductor was created and the complete filter was fabricated in a 0.8 μm BiCMOS process. To illustrate the application of this floating inductor, the sixth-order bandpass LC reconstruction filter was built to operate in the range of UHF, where the research value of this approach lies.

1.2 A Top Level Perspective of the DAC System

The operation of this DAC system is briefly discussed in this section. Fig. 1.3 shows the block diagram of a single-bit bandpass ΣΔ DAC system [8]. It consists of a bandpass ΣΔ modulator, a one-bit DAC and an analog reconstruction bandpass filter. The input and output time domain waveforms of each block are displayed on the left of the signal flow graph while their corresponding power spectral density plots on the right. The signal flow graph begins at the multibit (n-bit) digital input of a bandpass ΣΔ modulator. In the time domain, this input signal is oversampled in discrete time and its amplitude is quantized to 2^n levels as illustrated in Fig. 1.3(a). This oversampling can be achieved by a preceding interpolator [12] but in this application, this component is not needed since the whole oscillator is operating at the oversampling rate. This oversampled input contains a narrowband signal with

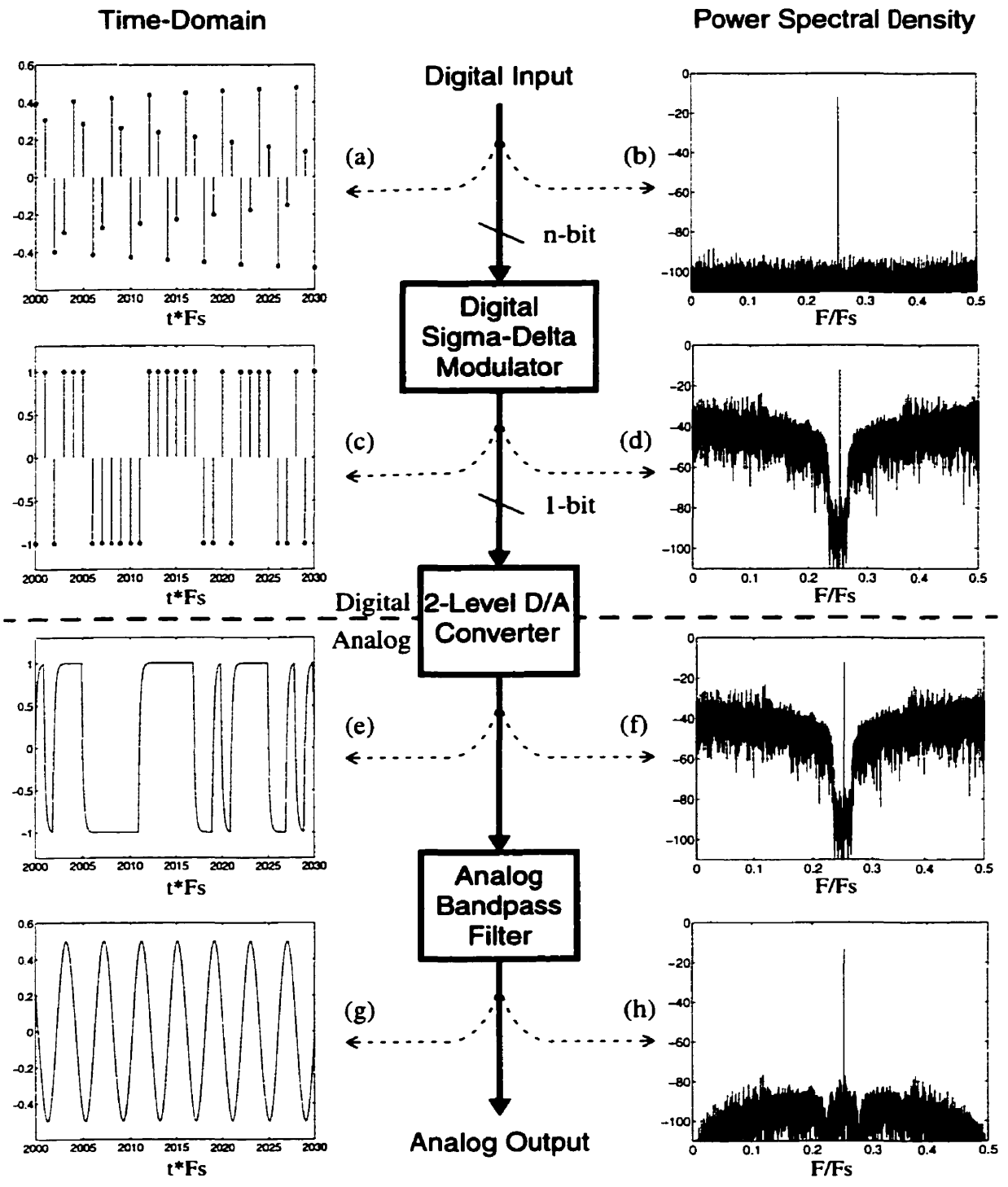


Figure 1.3: A Bandpass ΣΔ oversampling digital-to-analog converter. Time-domain signals are shown on the left. On the right are the same signals represented in the frequency domain.

a flat noise floor, as shown in Fig. 1.3(b). Using the ΣΔ modulation technique, this multibit signal is quantized to a single-bit representation while preserving the in-band signal integrity. As captured in Fig. 1.3(c), the modulator output is now one-bit wide but is still sampled data. In the frequency domain, it can be observed in Fig. 1.3(d) that the quantization noise generated in the modulation process is shaped out of the signal band. Due to this action, the in-band noise floor remains low and the signal resolution is preserved. This one-bit signal feeds a two-level DAC which converts it to continuous-time without altering its frequency content, as shown in Fig. 1.3(f). In time, we can see in Fig. 1.3(e) that this signal is represented by a train of finite-duration analog pulses, taking on only +Vref or -Vref analog levels. As a final step, the bandpass filter reconstructs the information in analog format by removing the out-of-band quantization noise.

1.3 Thesis Overview

It is the goal of this thesis to migrate the complexity of a mixed-mode system to its digital side so that the analog components involved are minimal. Thus, the design of a high-order digital modulator will first be explored and the use of an analog filter that is as simple and as low-order as possible will be investigated next.

As the first part of this thesis, Chapter 2 and 3 present an efficient implementation of a bandpass ΣΔ oversampling modulator for high speed D/A applications. Chapter 2 begins with an introduction to previous works and published literatures. In Section 2.1, the design process will be described starting with an intuitive understanding of the concepts followed by a noise transfer function (*NTF*) design. By an appropriate choice of the overall topology, the design of the modulator can be reduced to finding a digital filter structure such that the realized *NTF* fulfils the requirements of effective noise shaping while maintaining stable operation. Based on this topology, Chapter 3 proposes a new modular structure that is capable of implementing high-order bandpass modulators of variable bandwidths. FPGA and fixed-point simulations are used to characterize the stability of various orders as well as their noise shaping mechanism. The implementation results of orders from six to twelve are documented in terms of stability, pole-zero plots and Fast Fourier Transform of the output

waveforms. To speed up the highly iterative design process, design automation of this structure is incorporated into an in-house software for quick prototyping in the future.

The second part of this thesis deals with a high frequency filtering technique that has good potential in performing the reconstruction task. As will be shown in Chapter 4, the design of a passive LC ladder-based filter can be narrowed down to the design of various types of active inductors (i.e. grounded or floating). The realization of a grounded inductor is first considered using only silicon bipolar junction transistors. This single-ended version is then extended to a fully symmetrical floating architecture, biased using only CMOS current mirrors. Simulation is used to characterize this novel floating inductor in terms of its lossiness (i.e. the inductor Q factor) and the range of realizable inductance. This active inductor circuit is applied to an elliptic LC bandpass filter to demonstrate its ability to reconstruct analog signals from a $\Sigma\Delta$ modulator output bitstream. Experimental results are provided to illustrate its small signal frequency response and its intermodulation distortion behavior.

Finally, conclusions are drawn in Chapter 5 where the original ideas are identified and critical improvements highlighted. Based on the findings of this work, future directions are described to achieve further improvements in terms of the modulator's stability, the active inductor design, etc. VHDL codes are attached in the appendix for future reference.

Chapter 2 : Design of Digital Bandpass ΣΔ Modulators

Besides introducing the nomenclature used in this work, Chapter 2 highlights the fundamentals involved in developing high-order bandpass sigma-delta modulators. The important contributions to the field of sigma-delta modulation will be examined. To prepare the readers for the treatment of the proposed structure, this chapter also develops a design strategy and considers various digital implementation issues.

2.1 Introduction

With robust VLSI methods, ΣΔ modulation techniques have revolutionized data conversion as to achieve better resolution than that which was capable from conventional converters, such as successive approximation, subranging and flash types [13]-[14]. Similar to these converters, these modulation techniques involve trade-offs among signal bandwidth, output data resolution and the complexity of the analog and digital circuitry. An understanding of these trade-offs, together with its theory, is crucial to the design of ΣΔ modulator. These concepts will be developed and discussed with an emphasis on a digital bandpass modulator.

Although sigma-delta (ΣΔ) concepts have existed since the middle of the century [15], only in the last two decades have we seen extensive applications involving these techniques, as found in the collection of papers [14]. An obvious reason for this trend is the advances in VLSI technology, allowing high-speed high-density digital circuit integration. With such large amounts of integration, significant signal processing capability is available for processing the bitstream. A comprehensive overview of sigma-delta converters was done in [13] which covers a wide variety of techniques and design issues. The trend of using high-

order sigma-delta modulator started when a high-order topology was introduced for lowpass A/D applications [16]. On the D/A side, [17] provides the first complete treatment of the lowpass DAC system using a second-order noise shaper while an eighth-order modulator in a similar treatment was documented in [9]. Also in [9], comprehensive consideration was given to the one-bit DAC design, taking pulse shape, jitter and other nonideal effects into account. Since a sigma-delta converter is a nonlinear feedback system that can be unstable, a thorough empirical study was done in [19] to predict the maximum achievable SNRs for various orders and their corresponding stability limits. We find this work useful for selecting the appropriate ΣΔ modulator for the specifications at hand.

Instead of a one-bit DAC, recent developments have adopted the use of a multibit DAC which offers better trade-offs in terms of stability, SNR and circuit complexity. Even though relatively fewer bits than a typical Nyquist rate converter are used, this multibit DAC must provide linearity as high as the resolution of the modulator. To achieve such a linearity, algorithms were introduced to whiten the in-band noise such as [18] and [20] or even shape it out of the signal band [21][22][23][24]. However, these DACs involve extra circuitry for nonlinearity processing and their analog parts are not minimal in size. Thus in analog testing applications, the use of a multibit DAC might have to be avoided.

Both the A/D and D/A modulators share the same theory and concepts but differ significantly in terms of their hardware realizations. Since our primary objective is analog signal generation, this work will focus solely on the D/A application. The chosen topology for high-order modulator implementations and its corresponding transfer functions are identified in Section 2.2 which will facilitate the design of the noise transfer function in Section 2.3. Digital design issues are then considered in Section 2.4 to prepare for the treatment of the proposed structure in the next chapter.

2.1.1 The Basic Operation

The oversampled ΣΔ modulation technique essentially combines the advantage of oversampling and the effect of noise shaping to allow high resolution data conversion of signals with relatively low and medium bandwidth. In digital-to-analog (D/A) conversion applica-

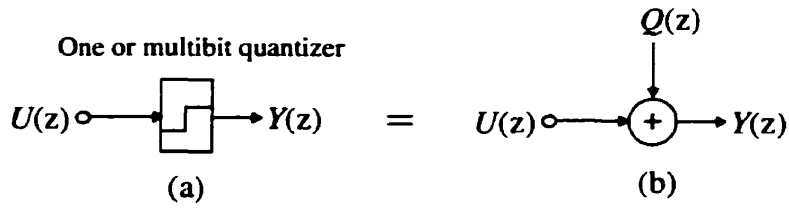


Figure 2.1: (a) The symbol and (b) the linear model of a quantizer.

tions, an n-bit signal is encoded by a digital modulator into a one-bit or relatively-few-bit output before it is converted into analog form. This mapping process, involving the quantization of the n-bit signal, generates quantization noise or error in a non-linear fashion which is difficult, if not impossible, to analyze by hand. To make the analysis of this quantizer tractable, the quantizer is often linearized and modeled as an additive white noise source with z-transform, $Q(z)$, summed with its input signal, to produce the quantized output signal $Y(z)$, as follows,

$$Y(z) = U(z) + Q(z). \tag{2.1}$$

The symbol and the model of the quantizer is shown in Fig. 2.1. This model is considered reasonable under certain conditions such as when the input bus size is large, the quantizer is not overloaded and the successive signal values are not excessively correlated. It should be pointed out that these conditions are not totally independent of each other. For example, an overloaded quantizer will yield a highly correlated output sequence which is also feeding back to the input of the modulator. In many cases, however, simulations and experiments have shown that a modulator's behavior can be closely predicted using this quantizer model.

With this model, the quantization error can be described as a random white noise process, with variance σ_q^2. When sampled at the Nyquist rate (f_s), this noise power will yield a noise floor or power spectral density of σ_q^2/f_s. In Fig. 2.2(a), a single-tone sine wave is shown with its noise floor on a power spectral density (PSD) versus frequency plot. However, as the sampling clock is increased in Fig. 2.2(b), the error power remains constant but spreads over a wider range of frequencies. Therefore, with higher sampling clock ($f_{os}>f_s$), the output noise floor of a modulator is lowered to σ_q^2/f_{os} as a result of the distribution of the

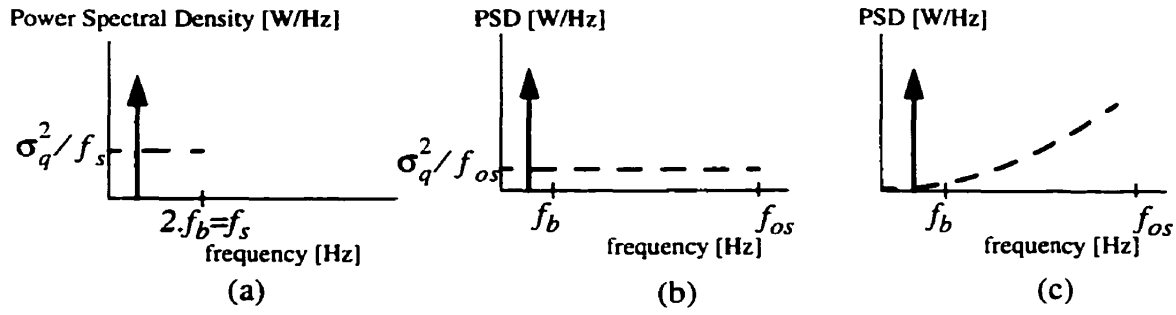


Figure 2.2: Frequency operations: (a) Nyquist conversion. (b) Oversampling conversion only (c) Oversampling plus noise shaping.

noise power outside the Nyquist band. The ratio of the oversampling clock (f_{os}) to twice the signal bandwidth (f_b) is known as the oversampling ratio or *OSR*, given by

$$OSR = \frac{f_{os}}{2 \cdot f_b} = \frac{f_{os}}{f_s}. \tag{2.2}$$

In addition to oversampling, the signal resolution is further improved by shaping the noise so that its amplitude is attenuated in the signal band. The amount of in-band attenuation is dependent on the shape and the order of the filter function. As illustrated in Fig. 2.2(c), this mechanism, appropriately termed noise shaping, is the essence of the ΣΔ modulation technique.

2.1.2 Digital-to-Analog Converter (DAC)

The encoding of an n-bit input to fewer bits enables the use of a relatively simple DAC to convert this digital signal into analog form. As an alternative to fine amplitude quantization, the digital output can be quantized to only one bit. This allows the DAC to take on its simplest form which reduces the amplitude of the analog pulses to only two. Being mainly digital hardware, this DAC system has a highly desirable property if it is to be used as part of a signal generator for mixed signal IC on-chip testing. That is, most of the generator can be confirmed defect-free with a mature digital testing scheme prior to an analog test. In addition, since there are only two output analog levels, this one-bit DAC is inherently linear and no calibration is required. Its inherent accuracy is derived from a precision, low-jitter clock source, eliminating the need for precision level reconstruction as long as the two lev-

els are consistent in time. In the following sections, the design steps for the modulator will be presented assuming a one-bit DAC is used, although a multi-bit DAC is also possible upon slight hardware modification [25].

One of the drawbacks of using a one bit output is the generation of large quantization error that may destabilize the modulator and corrupt the signal if it is not properly handled. Thus, ensuring the stability of a modulator is as important as maximizing its noise shaping performance or improving its resolution and bandwidth quality. Since there is still no complete mathematical expression that governs the stability of a ΣΔ modulator, we will rely on lengthy simulations and experimental prototypes as well as an ad-hoc criterion to predict its behavior. Details on the criterion and these simulations will be described in Section 2.3 and subsection 3.4.3.

2.1.3 Issues in ΣΔ Modulator Implementation

Based on the experience developed in [26], there are certain aspects and direction in ΣΔ modulator design that this thesis will adopt as its guidelines. In order to exploit the advantage of the transfer function's symmetry about the jω axis and hardware saving due to this symmetry, the oversampling clock of all the designs described in this work will be fixed at four times the carrier frequency. This will also correspond to the center of the signal band. This will require the band to appear near $\pm j$ on the z-plane. Due to this restriction, we will not rely on increasing the clock to enhance the signal dynamic range. In fact, increasing the oversampling clock imposes a stricter speed requirement on the analog hardware [9]. Further, relying on increasing the oversampling clock to improve the signal quality requires a flexible digital hardware implementation which may not be the most optimal in terms of area and speed. Instead, we will investigate the possibility of increasing the order of the modulator to improve signal quality. Higher-order modulators also have the flexibility of allocating wider than needed signal bandwidth so that the reconstructing filter's shape does not need to be very sharp (i.e. the filter's Q or order can be lower). Another approach to achieve this improvement will be to use a multi-bit instead of a single-bit DAC. With reduced internal feedback quantization error, the multi-bit DAC also enhances the stability of the modulator. However, this alternative may introduce more complications in mixed-

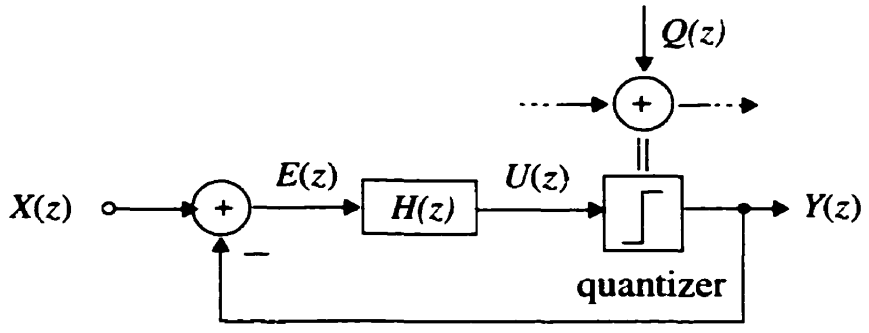


Figure 2.3: Standard overall structure for high-order ΣΔM.

signal testing applications as a more sophisticated analog component is now involved in the signal generator's self-testing process.

2.2 Topology and Transfer Function Considerations

Fig. 2.3 shows a general topology of a typical digital ΣΔM. It consists of an adder, a quantizer and a digital circuit that implements a transfer function $H(z)$. By using the linear model of the quantizer presented before, the overall modulator structure can be characterized by two transfer functions, referred to as the Signal Transfer Function (*STF*) and the Noise Transfer Function (*NTF*). Mathematically, these two transfer functions relate the output of the modulator to its two inputs, $X(z)$ and $Q(z)$, according to the following,

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot Q(z), \tag{2.3}$$

where

$$NTF(z) = \frac{1}{1 + H(z)} \tag{2.4}$$

and

$$STF(z) = 1 - NTF(z) = \frac{H(z)}{1 + H(z)}. \tag{2.5}$$

The basic idea of a ΣΔ modulator design is to find a circuit with transfer function $H(z)$ that serves to pass the input signal through without any change in its signal characteristics, albeit from an n-bit format to a one-bit format, and to minimize the effect of the quantizer noise on this signal at the modulator's output. These two conditions require a unique type

of circuit that can simultaneously implement the *STF* and *NTF*. This indeed can be done if the *STF* is a bandpass function and the *NTF* is a corresponding bandstop function. A linear phase bandpass *STF* not only can preserve the signal integrity during the encoding process, but will also performs out of band filtering of the input noise (not the quantization noise) during the ΣΔ modulation. Regrettably, a single transfer function of *H(z)* cannot be optimized to perform both noise shaping (i.e. the *NTF*) and effective filtering. Very often, due to the restriction of the *NTF*, the bandpass function is not sharp enough (i.e. low *Q*) and will most certainly introduce some in-band gain variation to the signal. Further, to include a ΣΔ modulator in a digital ΣΔ oscillator, which is the main application of this work, the *STF* is restricted to either unity or z^{-1}. Therefore, one should not rely on the modulator's *STF* to perform bandpass system filtering. Instead, the signal is just passed through the modulator without alteration. This can be easily achieved by re-arranging the topology [8] of the ΣΔM to that shown in Fig. 2.4. Straightforward analysis shows that it has a *STF* of unity for all frequencies, independent of *H(z)*. Also, the *NTF* of this topology is identical to that described by Eq. (2.4), which can be further represented by its numerator and denominator polynomials, as in the following,

$$NTF(z) = \frac{NTFnum(z)}{NTFden(z)} = \frac{den(z)}{num(z) + den(z)}, \tag{2.6}$$

where

$$H(z) = \frac{num(z)}{den(z)}. \tag{2.7}$$

Observe from Eq. (2.6) and Eq. (2.7) that the poles of *H(z)* become the *NTF* zeros. Also note that both the pole and zero polynomials of *H(z)* combine to form the pole polynomial

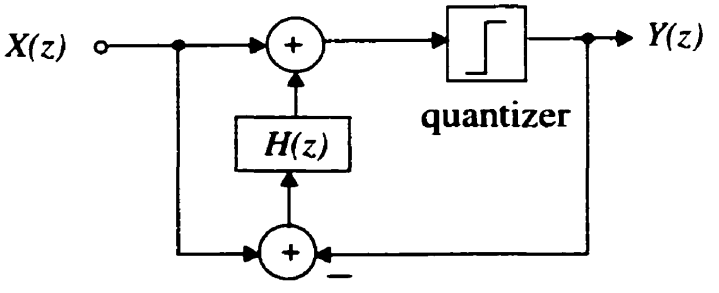


Figure 2.4: ΣΔM configuration that yields *STF*=1.

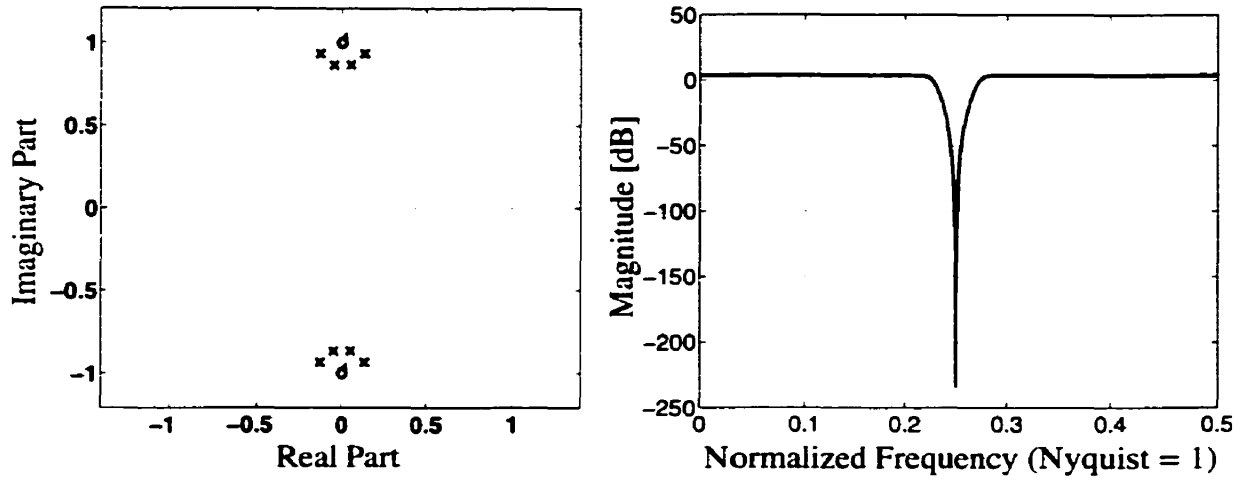


Figure 2.5: An eighth-order *NTF* design with coincidental zero

of the *NTF*. Thus, the design of this ΣΔM reduces to finding a filter structure with transfer function *H(z)* such that the realized *NTF* fulfils the requirements of effective noise shaping while maintaining stable operation.

2.3 *NTF* Design

There are two approaches in the design of *NTF* for a bandpass modulator: (i) by pole-zero placement, or (ii) mapping of a low-pass prototype to bandpass form. Being more intuitive, direct and allowing better control over the transfer function, the pole-zero placement method is adopted in this thesis. In this approach, the design of the bandpass ΣΔ modulator begins with the pole-zero placement of a *NTF*. The poles and zeros of the transfer function are placed independently on the z-plane to form a bandstop function. The zero placement will be done in such a manner that in the band of interest, the quantization noise is attenuated as much as possible by the *NTF* zeros while the out-of-band error is shaped for ease of post-filtering. To achieve stable operation, the poles will be placed inside the unit circle and at the same time limiting the *NTF's* out-of-band magnitude gain to 6 dB or below at all physical frequencies, complying with an ad-hoc stability criterion proposed in [27] and confirmed in [28]. Since the transfer function will be implemented with digital hardware, delay-free paths or non-causal loops must be avoided. This can be ensured if the *NTF* nu-

merator and denominator polynomials are of the same order and have identical leading coefficients, for which,

$$NTF(z)\big|_{z=\infty} = 1. \tag{2.8}$$

Thus, the ΣΔM design problem becomes a filter design problem with specific transfer function requirements. Such transfer functions can be easily synthesized using DSMOD, the MATLAB-based software for designing ΣΔM and oscillators [29].

Fixing the oversampling clock at four times the signal-band center frequency, the *NTF*'s poles can be placed on the unit circle according to the description above and illustrated in Fig. 2.5 for an eighth-order bandpass modulator. Specifically, the *NTF*'s zeros are all located at the band center and surrounded by poles on the inside of the unit circle. These poles have the same radius to the band center, i.e. to the point $(0, \pm j)$. We shall refer to this as Butterworth configuration for its similarity to the pole placement in a lowpass prototype. Due to this feature, the *NTF* has a maximally flat pass band. This flatness enables a simple check for the conditional stability criterion to be performed in the design software. This coincidental zero placement strategy, however, is not optimal and the resulting bandwidth is not adjustable. Experience has shown that maximum noise suppression can be achieved by distributing the zeros of the *NTF* throughout the frequency region occupied by the input signal [19], [27]. The effective bandwidth also can be controlled by this distribution, trading off signal dynamic range for wider bandwidth for a given modulator's order. This strat-

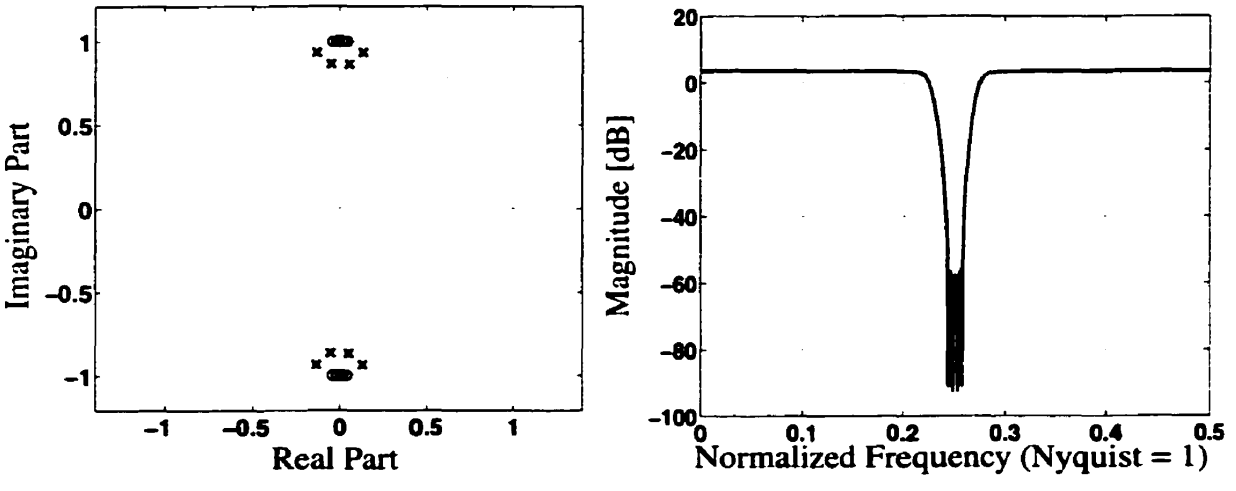


Figure 2.6: An eighth-order *NTF* design with optimally spaced zeros.

egy, called Butterworth-poles-and-optimally-placed-zeros in DSMOD [29], is shown in Fig. 2.6 for an eighth-order *NTF*.

There is a price to be paid for this improvement in terms of hardware complexity. Many structure coefficients are needed to optimally control the *NTF* zeros across the signal band and at the same time fix them on the unit circle. Potentially, the introduction of these coefficients can reduce the operating speed and increase the hardware involved by several orders of magnitude. In the next section, the requirements and limitations for the structure that realizes these pole-zero locations will be specified and examined before the design phase commences in the next chapter.

2.4 Digital Design Issues

The theory for both the lowpass and bandpass modulators are basically the same except that the shape of the filter function in bandpass applications effectively doubles the order of the modulator. In terms of digital hardware, the number of registers (or delays) and adders will also be doubled. However, the adders' size may increase at a much faster rate with increasing clock rate, especially for bandpass applications in which the speed can be much higher than the lowpass case. This increase of the adders' size is due primarily to the use of carry-look-ahead architectures in the synthesis process. Such architectures are necessary to help meet the timing constraint imposed by the fast clock. Therefore, in the search of an efficient implementation for bandpass applications, short combinational-logic paths throughout a structure is a must if the stringent speed requirements are to be met without severe hardware penalties.

With the switched-capacitor technique, an analog-to-digital $\Sigma\Delta$ modulator can be implemented using transconductance amplifiers as basic building blocks. Popular $\Sigma\Delta$ modulator structures, such as cascade-of-integrators or cascade-of-resonators [30], are well established and optimized for analog design considerations which include integrator's settling time and loading, noise injection, etc. Although these structures can be realized with digital hardware, they are not optimized for speed, coefficient quantization and other digital im-

plementation issues. Hence, there is a need to find a digital structure that can efficiently realize the *NTF* with a reasonable amount of hardware and power consumption. In particular, we would like to de-sensitize the effect of coefficient truncations on the structure's transfer function while maximizing its operating speed. Prior to this work, these two requirements could not be simultaneously met with existing digital ΣΔ modulator implementations.

To minimize the overall hardware requirements, it becomes clear rather quickly that multipliers should be avoided at all cost. This is because they consume large amounts of silicon area and, moreover, they are too slow. Hence, to get around the use of multipliers, we must be capable of realizing the desired transfer function *H(z)* using power-of-two coefficients. In this way, simple hard-wired shifts can be used to implement the necessary coefficients with no speed penalties. Obtaining exactly the desired transfer function, however, is not always possible, due to the coefficient quantization. Therefore, we adopted the approach suggested in [26].

Specifically, we have devised a circuit structure whose pole and zero positions are relatively insensitive to coefficient quantization. Furthermore, the *NTF* zero locations are constrained to always remain on the unit circle and, for stable operation, the poles are required to stay within the unit circle. In this way, even if the desired transfer function *H(z)* is not achieved exactly, we will have realized a very good approximation. Structures derived from LC ladder prototypes utilizing lossless discrete integrators (LDIs) possess these properties [26]. Unfortunately, as the order of the modulator increases, more adders are placed in series along the critical path, reducing the frequency range of the ΣΔ modulator. More details on this topic will be documented in subsection 3.2.2 of the next chapter. For bandpass applications involving wide bandwidth high carrier frequency (above 10 MHz and 10 bits) D/A conversion, the LDI prototype was not able to meet the specifications without serious hardware penalty in a 0.8 μm BiCMOS technology. Thus, a new structure was necessary to be created and one that will be described in the next section. Knowing the desired pole-zero locations/movements, our strategy is to find a structure that will naturally mimic this behavior of the *NTF*, starting with a second-order module as will be illustrated in the next chapter of this thesis.

2.5 Conclusions

This chapter carries an introduction to the technique of $\Sigma\Delta$ modulation. The key contributions to the advancement of this field were examined. In addition, high level design issues and digital implementation considerations were also provided. Having discussed these topics, the hardware design strategy which will be crucial to the development of the proposed structure in the next chapter was then investigated.

Chapter 3 : High-Order Bandpass ΣΔ Modulators for High Speed D/A Applications

A multiplier-free structure for implementing high-order bandpass digital ΣΔ modulators is provided in this chapter. Near-optimum noise suppression in the passband region of the modulator is achieved by constraining the Noise Transfer Function (*NTF*) zeros to lie on the unit circle, even after coefficient quantization. High-speed operation is obtained by using a highly modular structure with minimum critical path delays which are independent of the modulator order. Results from various simulations and experimental prototypes are given to illustrate both the stability of the designs and the flexibility of the overall structure. Design automation for modulators of order four to sixteen are incorporated into an in-house MATLAB based software called DSMOD.

3.1 Introduction

There are several digital structures capable of implementing high-order bandpass modulators, e.g. integrator-cascade, LDI ladder, etc. However, these structures are not optimal for high speed operation in bandpass implementations. In this chapter, we will examine a new architecture that can potentially replace all existing designs as an optimal solution in digital bandpass applications.

Building on top of the design issues considered in the previous chapter, the internal architecture of the proposed structure is examined in Section 3.2. Once the structure is presented, its speed performance is investigated and compared to other structures to illustrate the performance improvement. Using this architecture, an algorithm for automating the design of arbitrary-order ΣΔ modulator is presented in Section 3.3. Several implementation examples

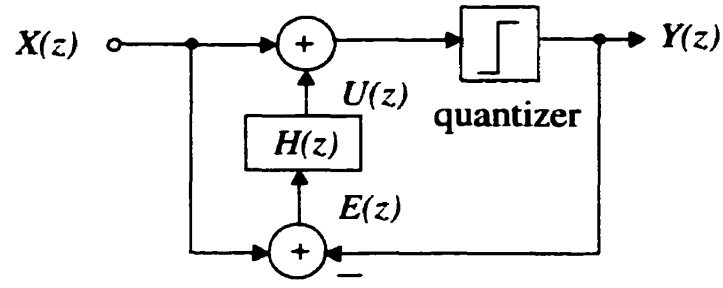


Figure 3.1: ΣΔM configuration that yields *STF*=1.

are demonstrated in the following section. Finally, simulation and experimental results are also provided to illustrate the validity of the proposed structure.

3.2 Internal structure of the New ΣΔ Modulator

Based on the background theory of ΣΔ modulators, a new structure to realize high-order bandpass digital modulators will be developed here in a top-down manner. Fig. 3.1 shows a specific topology of a digital ΣΔ modulator with a 1-bit quantizer [26] where *E(z)* and *U(z)* are the input and output of the internal block *H(z)*, respectively. Based on our understanding developed in the previous sections, the block *H(z)* can be realized using the second-order resonator as a basic building block as shown in Fig. 3.2(a). Straightforward analysis reveals that it has two poles at $e^{\pm j(\pi/2)}$ on the *z*-plane. Cascading two of these stages will result in four poles at $e^{\pm j(\pi/2)}$. As the poles of the *H(z)* are the zeros of the *NTF*, noise can be more effectively shaped [19] by varying the angles of these poles away from

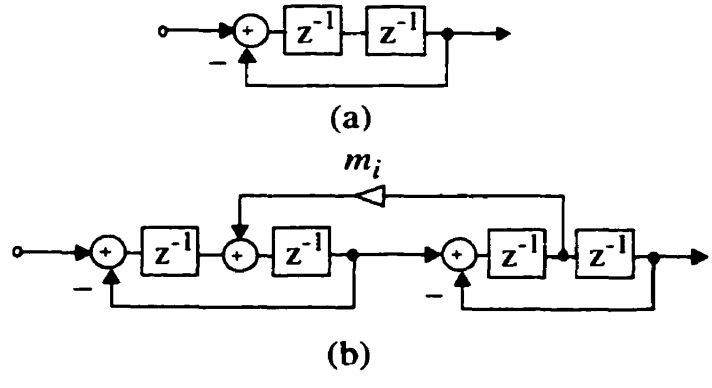


Figure 3.2: Digital resonator sections: (a) 2nd-order (b) 4th-order.

$\pm\pi/2$, while keeping their radii equal to one, as described in section 2.3. With hardware, this can be achieved by introducing an additional feedback path, labeled m_i, between two resonator sections as illustrated in Fig. 3.2(b). We shall refer to this as a fourth-order resonator. The characteristic equation of this structure is given by,

$$1 + (2 - m_i) \cdot z^{-2} + z^{-4} . \tag{3.1}$$

On the z-plane, this fourth-order resonator's pole configuration is drawn in Fig. 3.3. Mathematically, each root location can be described in the following form,

$$z - \left(r \cdot e^{j \cdot \left(\frac{k \cdot \pi}{2} \pm \phi \right)} \right), \tag{3.2}$$

where r is the radius of the root from the origin, k is either 1 or 3 and ϕ can be either positive or negative depending on which quadrant it is located in. Multiplying the four terms yields:

$$\left(z - r \cdot e^{j \cdot \left(\frac{\pi}{2} + \phi \right)} \right) \cdot \left(z - r \cdot e^{j \cdot \left(\frac{\pi}{2} - \phi \right)} \right) \cdot \left(z - r \cdot e^{j \cdot \left(\frac{3\pi}{2} + \phi \right)} \right) \cdot \left(z - r \cdot e^{j \cdot \left(\frac{3\pi}{2} - \phi \right)} \right) \tag{3.3}$$

$$= (z^2 - (\alpha 1 \cdot z) + r^2 \cdot e^{j \cdot \pi}) \cdot (z^2 - (\alpha 2 \cdot z) + r^2 \cdot e^{j \cdot \pi}) \tag{3.4}$$

$$= z^4 - ((\alpha 1 + \alpha 2) \cdot z^3) - ((2 - (\alpha 1 \cdot \alpha 2)) \cdot z^2) + ((\alpha 1 + \alpha 2) \cdot z)) + r^2 . \tag{3.5}$$

where

$$\alpha 1 = r \cdot e^{j \cdot \left(\frac{\pi}{2} - \phi \right)} + r \cdot e^{j \cdot \left(\frac{\pi}{2} + \phi \right)} , \tag{3.6}$$

$$\alpha 2 = r \cdot e^{j \cdot \left(\frac{3\pi}{2} - \phi \right)} + r \cdot e^{j \cdot \left(\frac{3\pi}{2} + \phi \right)} . \tag{3.7}$$

While requiring r to be unity, the pole-zero placement strategy in section 2.3 reduces the ($\alpha 1$+$\alpha 2$) coefficients of Eq. (3.5) to zero due to the symmetry of the root positions. Indirectly, this strategy has simplified the requirements on the implementation because less co-

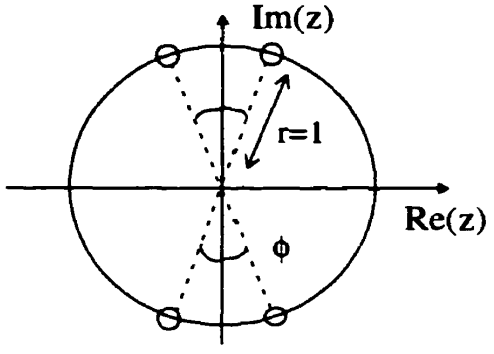


Figure 3.3: *NTF* zeros (poles of *H(z)*) in the *z*-plane.

efficients will be needed to realize a modulator of the same order, i.e. smaller hardware. With these simplifications, this pole configuration of Fig. 3.3 can be expressed in terms of ϕ only as follows

$$(1 + (4 \cdot \cos^2\phi - 2) \cdot z^{-2} + z^{-4}). \tag{3.8}$$

By comparing Eq. (3.8) with (3.1), we can assign,

$$m_i = 4 \cdot (1 - \cos^2\phi) = 4 \cdot \sin^2\phi. \tag{3.9}$$

Thus, interpreting the pole locations as being positioned on the unit circle with an angular distance $\pm\phi$ radians from the $j\omega$ axis with mirror symmetry as shown in Fig. 3.3. Variations in m_i due to coefficient quantization will not move the *NTF* zeros off the unit circle, only alter their passband positions. Thus, deep notches are always present in the *NTF* magnitude plot.

The *NTF* poles, effectively controlled by the zeros of *H(z)*, are formed by injecting a weighted-version of the unit-delayed error signal *E(z)* into each second-order resonator section of the modulator. This is shown in Fig. 3.4(a) for a 10^{th}-order example consisting of a cascade of two fourth-order resonator sections and one second-order section. Distributing *E(z)* throughout the resonator structure has two beneficial effects: (1) it allows arbitrary *NTF* pole placement, and (2) it minimizes the number of adders in the critical path of the overall modulator structure independent of the modulator order (two, if a_i and m_i are rep-

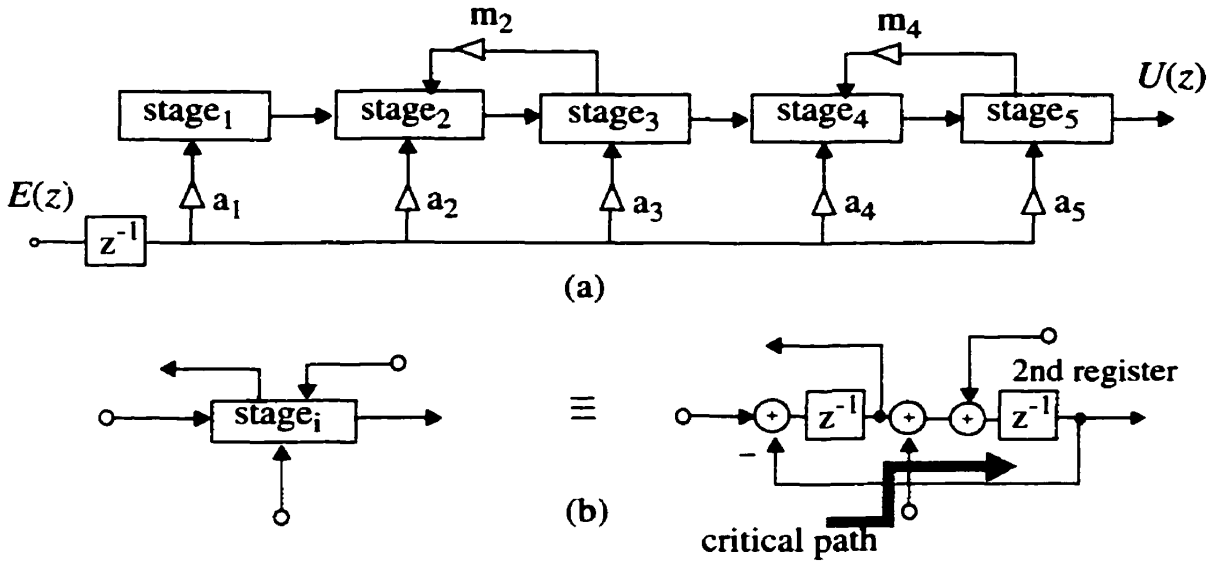


Figure 3.4: (a) The *H(z)* block for a 10^{th}-order BPΣΔM,
(b) symbol for second-order resonator section.

resented by a power-of-two coefficient). The latter point is particularly important for high-speed operation and is the main contribution of this structure.

Modulators of other orders are a straightforward variation of this 10^{th}-order example. In particular, an N^{th}-order structure will require N+1 registers and, assuming single-valued quantized coefficients, at least N+3 adders.

3.2.1 Critical Path Considerations of the New Structures

The critical path of a digital structure is the combinational-logic path between two registers that has the largest delay. This delay will dictate the maximum clock frequency of the structure. Taking a closer examination of Fig. 3.4(b), this path is identified as the route taken to travel through the a_i coefficients and the two adders before reaching the second register in each stage. Since this path begins and ends within a stage, the speed performance of this structure is order-independent.

Due to the chosen topology for high-order modulator implementation, another possible critical path, which is again order-independent, might exist as identified in Fig. 3.5. It stretches across two adders and the quantizer. However, some of these components can be

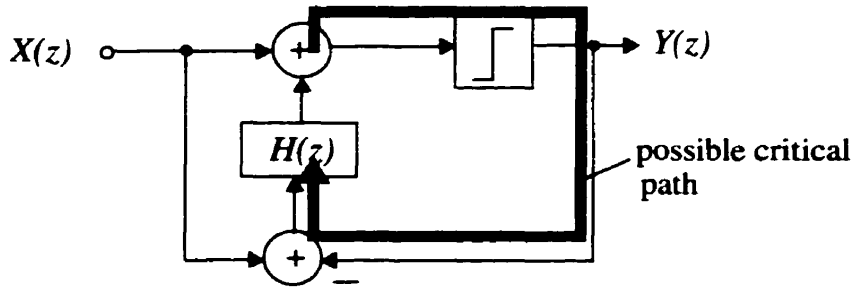


Figure 3.5: An illustration of one possible critical path in the ΣΔ modulator.

greatly simplified due the use of two's complement mathematics and the one-bit feedback. The quantizer is realized by the sign bit of the first adder's output. And since the feedback is only a one (00100....) or a negative one (11100...), the full adder after the quantizer can be reduced to a three-bit adder regardless of the internal bus size. Therefore, this path is no longer on the critical route. Subsection 3.4.4 provides further details of this implementation and interested readers may jump ahead.

The delay introduced by an adder is dependent on the design architectures (e.g. carry-look-ahead, ripple, etc.), the bus size and the process technology. To get an idea of the speed performance of the structure, consider a modulator with a fourteen-bit input bus implemented in a 0.8 μm BiCMOS technology. The critical path, consisting of two CMOS 17-bit ripple adders, introduces a delay of 21 nsec, resulting in an estimated maximum clock frequency of 45 MHz.

3.2.2 A Comparison on the Length of Critical Paths in Other Existing Structures

To draw a comparison in terms of speed performance, we will examine four eighth-order bandpass structures with unity *STF* that were developed in [26], namely the two integrator-cascade variants, the resonator-cascade and the LDI-ladder structures. The works on integrator-cascade structures in [26] were based on the contributions of Risbo [9] and Chao [16].

After the lowpass-to-bandpass mapping process, all these architectures involve the use of biquads mapped from delayed or nondelayed integrators. These two building blocks and

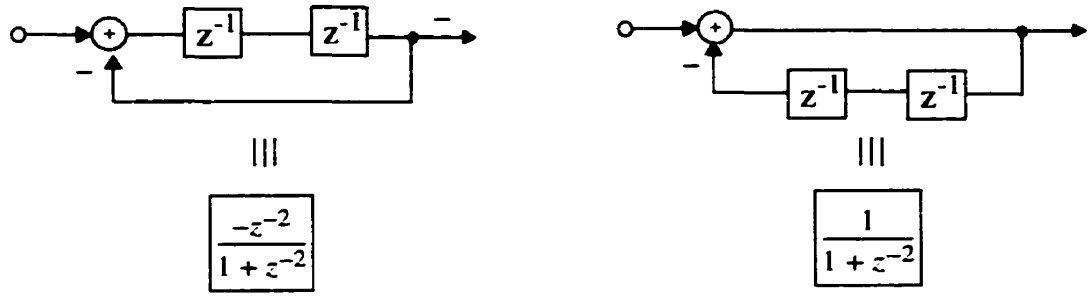


Figure 3.6: Two basic building blocks for the integrator-cascade, resonator cascade and LDI ladder structures.

their symbols are shown in Fig. 3.6. Assuming a band center frequency at $\pi/2$, each of them can be simplified to consist of only two registers and an adder. When the critical path is being considered, one should keep in mind that there is an adder in each of these blocks.

Fig. 3.7 contains the realization of the one of the integrator-cascade structures. As indicated on the figure, a critical path of seven adders is found in the eighth-order modulator. Another integrator-cascade topology shown in Fig. 3.8 can be operated at a slightly higher speed since there are five adders in series instead of seven.

The third structure considered is the resonator-cascade as depicted in Fig. 3.9. Since there is no register in the forward path of the $\frac{1}{1+z^{-2}}$ block, this structure has eight adders in its critical path. Suffering from the same problem is the modulator based on the lossless discrete integrator (LDI) ladder. As illustrated in Fig. 3.10, this structure also has eight adders in cascade in its critical path.

Similar analysis was also performed for the above structures of order four and six. Compared to the new structure which has two adders in its critical path, all four existing topologies are significantly slower. Moreover, as the modulator's order changes, so does the critical path delay for all four of the above structures. This is in contrast with the proposed structure, whose critical path delay is order independent. Table 3.1 provides a summary of

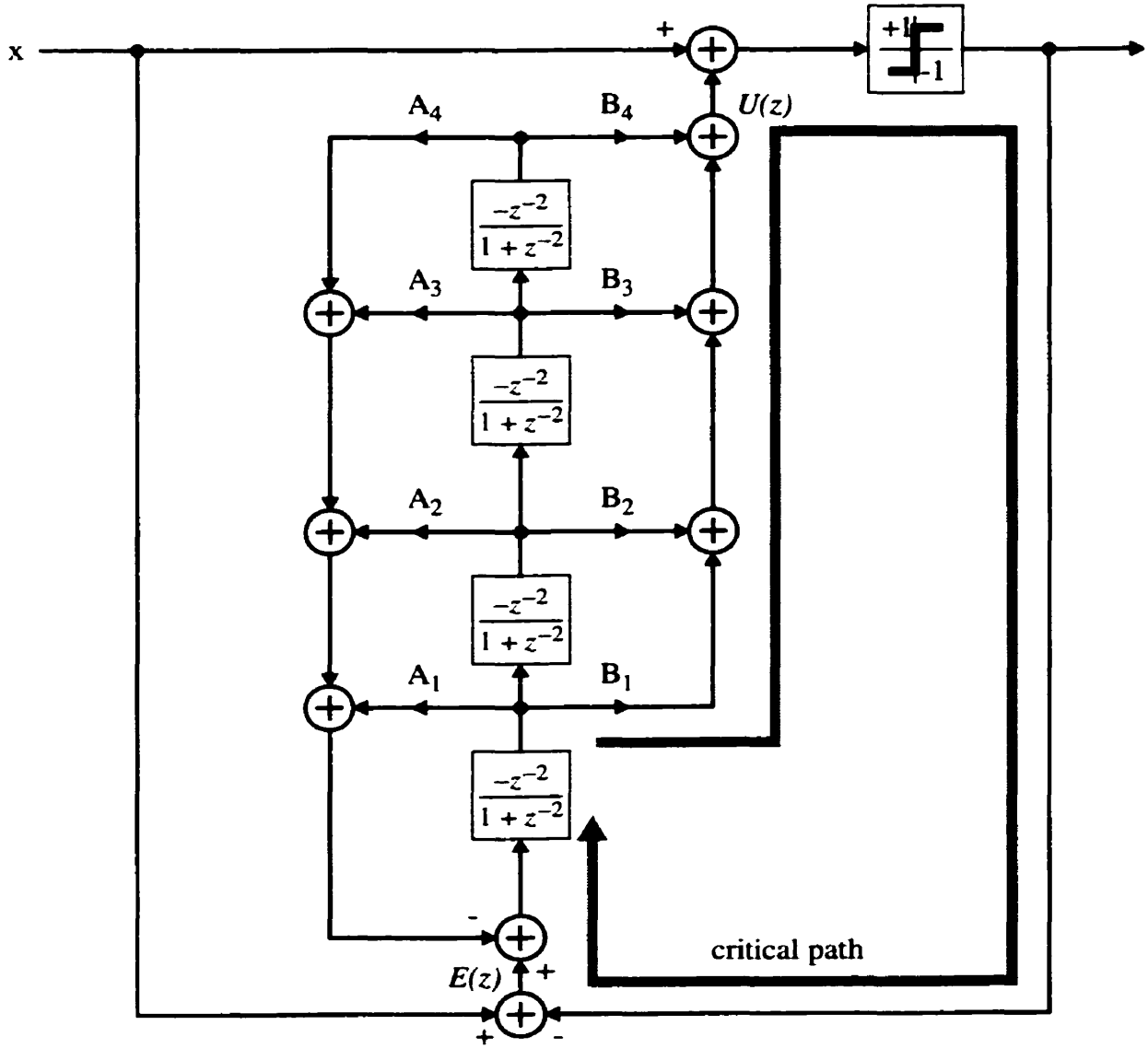


Figure 3.7: Realization of an 8[th]-order delta-sigma modulator based on Chao's multiloop-feedback integrator structure.

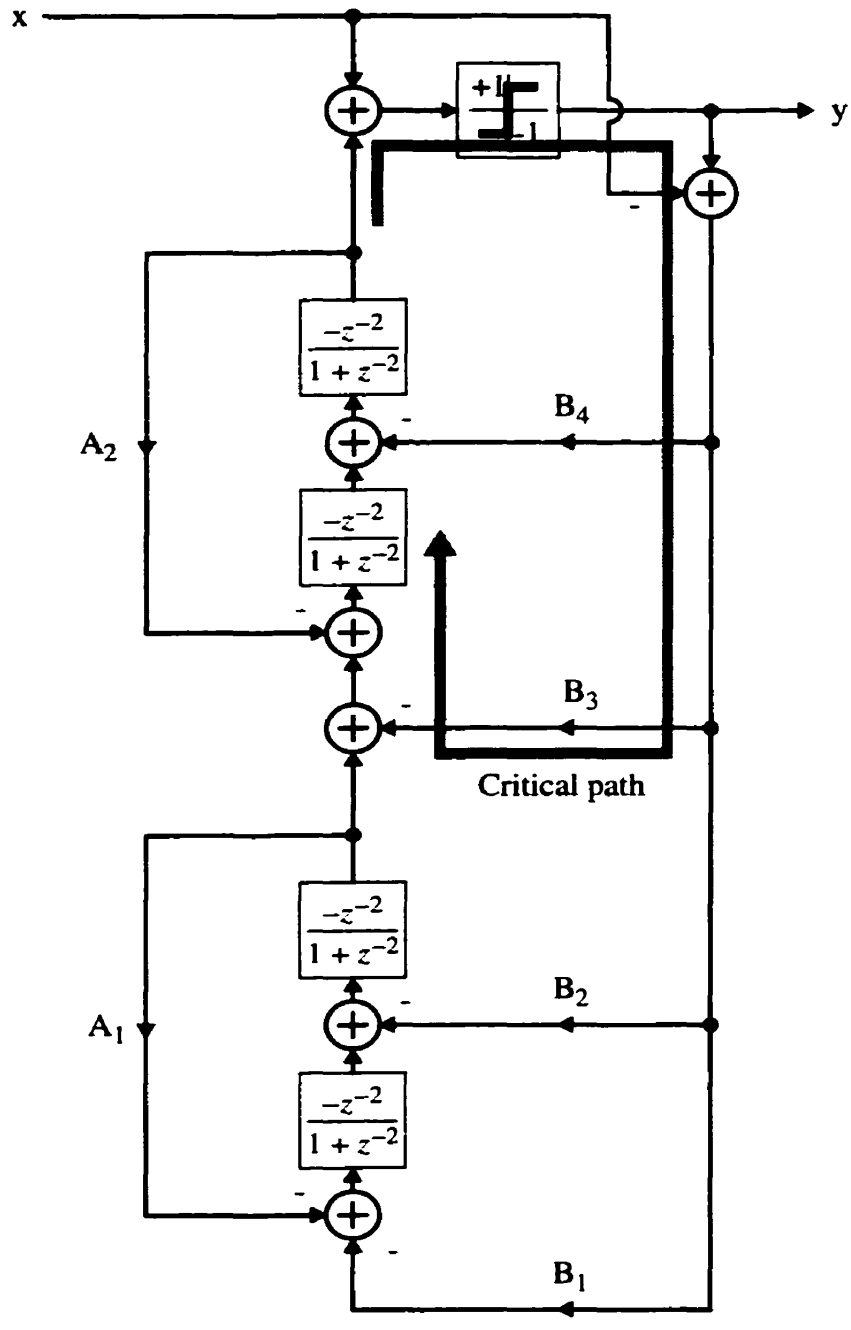


Figure 3.8: Realization of an 8[th]-order delta-sigma modulator based on [9] but modified to have unity STF.

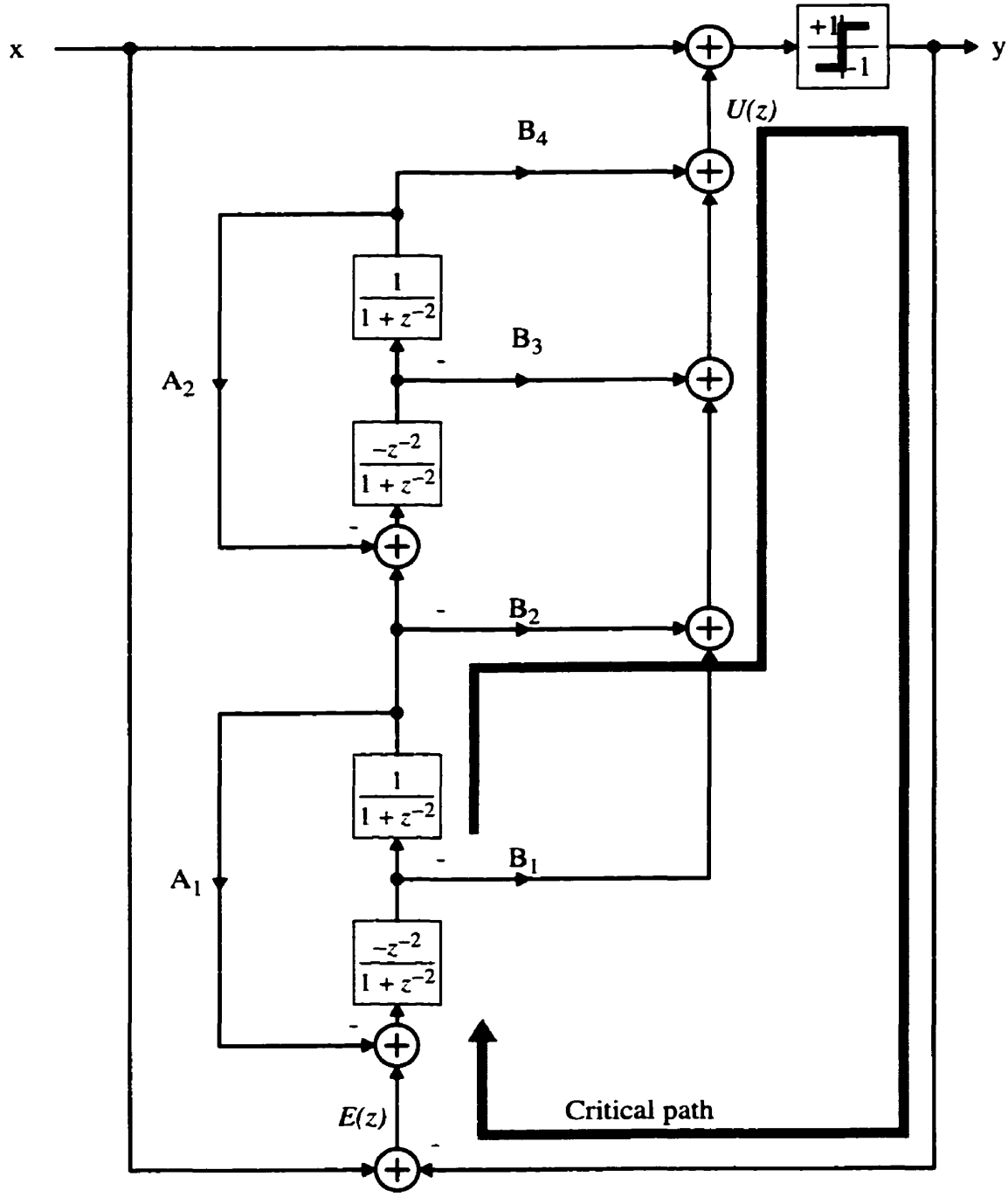


Figure 3.9: Realization of an 8[th]-order modulator based on a resonator-cascade with unity STF.

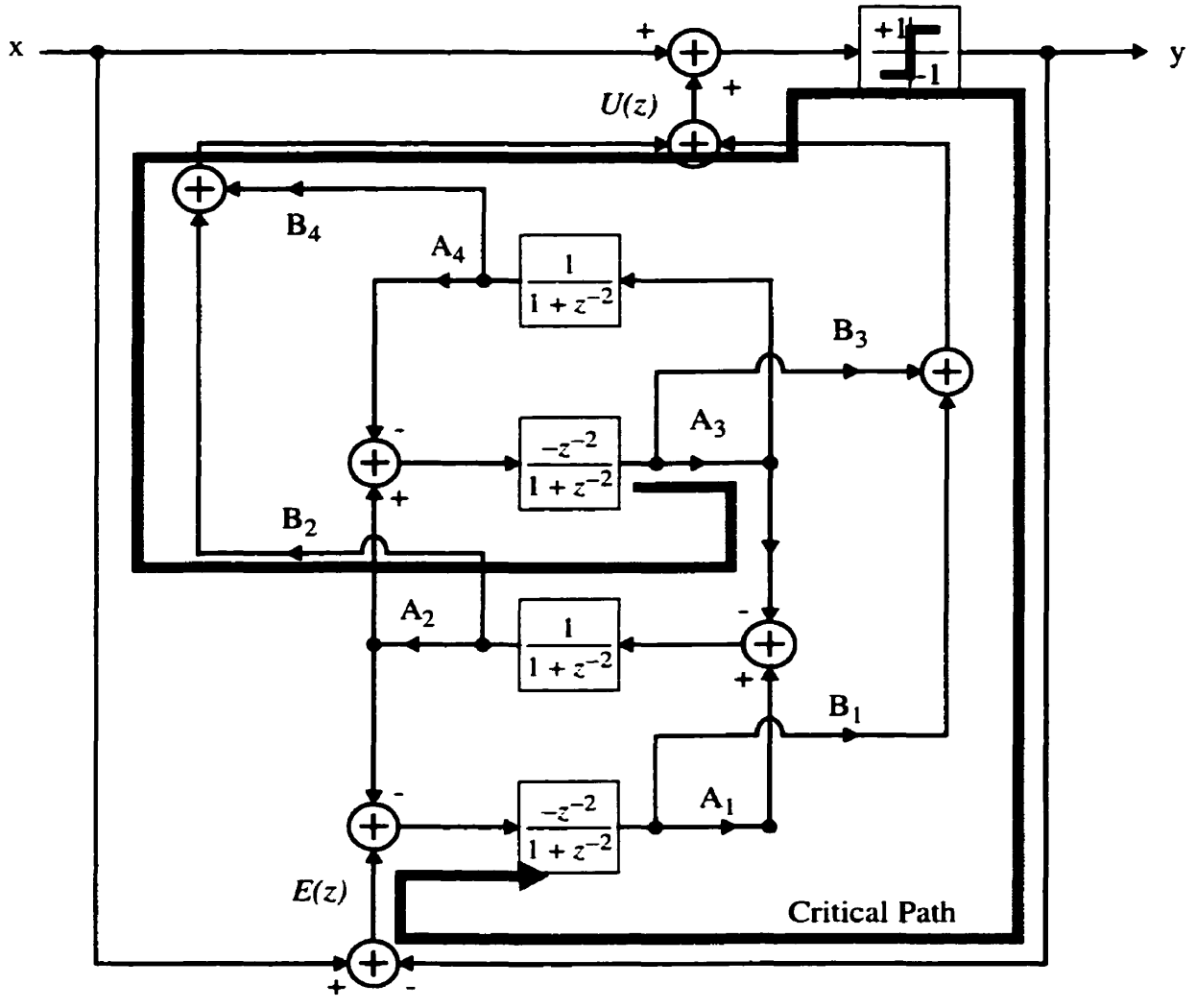


Figure 3.10: Realization of an 8[th]-order modulator based on the Lossless Discrete Integrator (LDI) ladder with an overall structure yielding a signal transfer function equal to unity.

Bandpass ΣΔ modulator structures	Critical Path (number of adders) for Various Orders		
	4^{th}	6^{th}	8^{th}
Chao's multiloop-feedback integrator-cascade	5	6	7
Integrator-cascade based on [9]	4	4	5
Resonator-cascade	6	7	8
LDI ladder	6	7	8
The proposed structure	2	2	2

Table 3.1: A comparison in speed performance for modulators of order four to eight implemented with different structures.

the comparison for all five structures, highlighting the speed-advantage of the proposed structure.

3.3 Design Automation

This new structure, aptly named coupled bandpass resonator, was incorporated into our design tool, DSMOD, an abbreviation for Delta Sigma Modulator and Oscillator Designer [29]. One of the goals of this tool is to speed up the computation-intensive and highly iterative design process of ΣΔ modulators. According to the design flow shown in Fig. 3.11, the *NTF* will be first selected through either a one-step calculation process in the "*NTF* Design" box or an optimizing routine in the "Optimal *NTF* Design" box. Both processes will base their computation on the specified *OSR*, the modulator's order, |*NTF*| stability bound and its passband type (which is bandpass in this case). The outcome, which is the *NTF*'s transfer function, is then mapped to the coefficients of the coupled bandpass resonator structure using Eq. (2.6), Eq. (3.9) and the topology shown in Fig. 3.1. Specifically, the m coefficients can be uniquely solved via Eq. (3.9) once the desired width of the passband is known. This unique solution enables the polynomial-to-coefficient mapping process to be performed sequentially, without iteration nor optimization. Unlike other structures that we are aware of, the calculation involved is less convolved and thus is much faster. With the

m coefficients solved, the a coefficients (as labelled in Fig. 3.4) can be obtained starting with the rearrangement of Eq. (2.6), as follows,

$$H(z) = \frac{NTFden(z) - NTFnum(z)}{NTFnum(z)}, \tag{3.10}$$

where

$$NTF(z) = \frac{NTFnum(z)}{NTFden(z)}.$$

Below, the process of solving for the a coefficients is done using a sixth-order $H(z)$ block as an example. The NTF is attained from the pole-zero placement procedure. According to Eq. (3.10), the $H(z)$ can be derived from this NTF, which we denote as $H_{ideal}(z)$, and is given by

$$H_{ideal}(z) = \frac{n_1 \cdot z^{-2} + n_2 \cdot z^{-4} + n_3 \cdot z^{-6}}{1 + (3 - m_1) \cdot z^{-2} + (3 - m_1) \cdot z^{-4} + z^{-6}}.$$

On the other hand, the transfer function of the proposed structure can be extracted to have the following form,

$$H_{structure}(z) = \frac{a_3 \cdot z^{-2} + ((2 - m_1) \cdot a_3 + a_2) \cdot z^{-4} + ((1 - m_1) \cdot a_3 + a_2 + a_1) \cdot z^{-6}}{1 + (3 - m_1) \cdot z^{-2} + (3 - m_1) \cdot z^{-4} + z^{-6}}.$$

Since the structure is to realize the ideal transfer function, i.e. $H_{ideal}(z) = H_{structure}(z)$, the a coefficients will be directly solvable through sequential term-by-term mapping. For the above example, we can write

$$n_1 = a_3 \tag{3.11}$$

$$n_2 = (2 - m_1) \cdot a_3 + a_2 \tag{3.12}$$

and

$$n_3 = (1 - m_1) \cdot a_3 + a_2 + a_1. \tag{3.13}$$

To systematically automate this mapping process, Eqs. (3.11) to (3.13) can be rearranged and grouped into matrix form as below,

$$\begin{bmatrix} n_3 \\ n_2 \\ n_1 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1-m_1 \\ 0 & 1 & 2-m_1 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}, \tag{3.14}$$

from which the a terms can then be found as follows,

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1-m_1 \\ 0 & 1 & 2-m_1 \\ 0 & 0 & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} n_3 \\ n_2 \\ n_1 \end{bmatrix}. \tag{3.15}$$

Therefore, the structure coefficients of the sixth-order modulator are completely solved sequentially in three steps. Regardless of the modulator's order, the design process is identi-

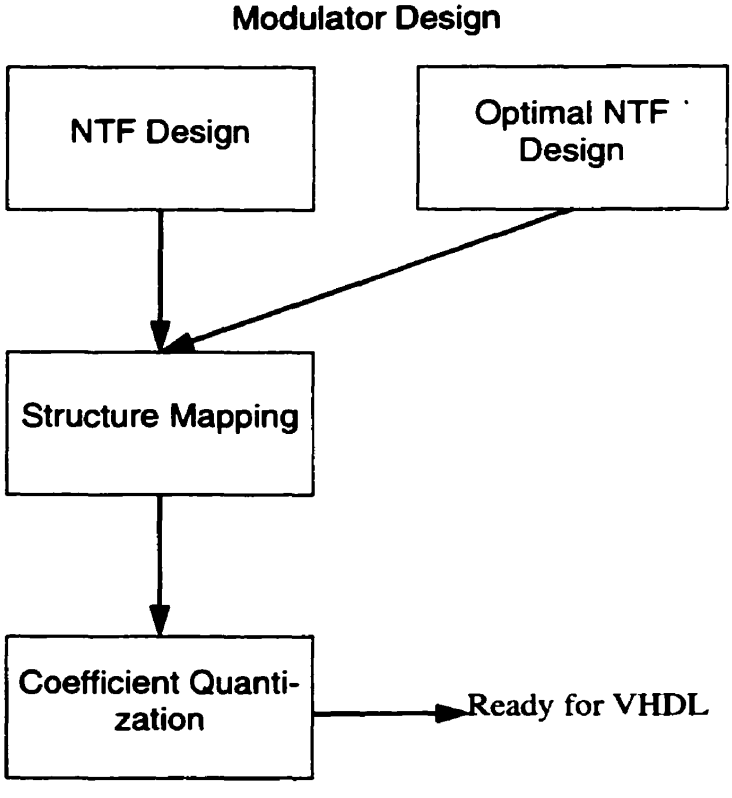


Figure 3.11: A partial DSMOD's design flow for modulators.

cal to this sixth-order case and only the dimensions of the procedure changes. As a result, we can rewrite Eq. (3.14) in the following manner

$$N = Hpar \cdot A \tag{3.16}$$

where

$$N = \begin{bmatrix} n_N \\ \cdots \\ \cdots \\ n_2 \\ n_1 \end{bmatrix}, A = \begin{bmatrix} a_1 \\ a_2 \\ \cdots \\ \cdots \\ a_N \end{bmatrix} \text{ and } \boldsymbol{Hpar} = \begin{bmatrix} 1 & c_{12} & c_{13} & \cdots & \cdots & c_{1\frac{N}{2}} \\ 0 & 1 & c_{23} & \cdots & \cdots & c_{2\frac{N}{2}} \\ 0 & 0 & 1 & \cdots & \cdots & c_{3\frac{N}{2}} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & c_{\frac{N-1}{2}\langle\frac{N}{2}\rangle} \\ 0 & 0 & 0 & \cdots & 0 & 1 \end{bmatrix}.$$

Here, ***Hpar*** is a N/2 x N/2 upper triangular matrix for an N^{th}-order $H(z)$ numerator polynomial where c_{ij} is a function of the m coefficients only for all $i < j$, c_{ij} is unity for all $i = j$ and zero for all $i > j$. Hence, to solve for the A vector in Eq. (3.16), one simply computes the inverse of ***Hpar*** and multiplies it by the N vector.

After the structure coefficients are mapped, they will be quantized to a pre-specified number of power-of-two terms for digital implementation. This quantization process is identical for all structures and will not be discussed here. Similar procedures and equations describing the coupled bandpass resonator structure, for orders four to sixteen, are programmed into DSMOD. For a complete description of this design tool, please refer to [8].

3.4 Examples

In order to illustrate the real-time behavior of this new BP ΣΔM structure, we designed four modulators of 6^{th}, 8^{th}, 10^{th} and 12^{th}-order. These modulators were designed to have a bandwidth of at least 200 kHz, centered at 10.7 MHz when clocked at 42.8 MHz. This corresponds to an oversampling ratio (OSR) of no greater than 107. All modulators were expected to provide an in-band *SNR* of at least 56 dB (corresponding to approximately 9 bit conversion). Using DSMOD, the initial *NTF*s were all selected and then mapped into the

appropriate structure. Table 3.2 lists the coefficients, OSR, and several other design parameters pertaining to the hardware implementation. In high-order low *OSR* designs, the signal band occupies a wide frequency range relative to the oversampling clock and are more likely to become unstable because there is less room on the frequency axis for noise displacement. Thus, the actual *NTF* magnitude gain can exceed the designed stable boundary. In order to effectively examine the stability issue of this structure, various designs of different orders were synthesized with relatively low *OSR*s to see if they would be unstable in real time. Arbitrary resolution and various bandwidth can be met by this modular structure in practice.

Except for coefficient a_2 of the 12^{th}-order modulator, all the coefficients were single powers-of-two number. Additional precision was assigned to this coefficient without increasing the critical delay path because coefficient m_2 was zero. These coefficients were all realized by single hard-wired shifts which impose neither speed penalty nor hardware overhead.

Order	6	8	10	12
a_1	-2^{-4}	2^{-6}	-2^{-9}	2^{-15}
a_2	2^{-1}	-2^{-3}	2^{-7}	$-2^{-10}-2^{-12}-2^{-14}$
a_3	-2^{0}	2^{-1}	-2^{-3}	2^{-6}
a_4	NA	-2^{0}	2^{-1}	-2^{-3}
a_5	NA	NA	-2^{0}	2^{-1}
a_6	NA	NA	NA	-2^{0}
m_1	0	2^{-6}	0	2^{-7}
m_2	2^{-10}	0	2^{-5}	0
m_3	NA	2^{-9}	-2^{-8}	2^{-8}
m_4	NA	NA	2^{-7}	0
m_5	NA	NA	NA	2^{-11}
OSR	100	23	18	31
Input Bus Size	20	17	19	24
Critical path (# adders)	2	2	2	2
# of registers	7	9	11	13

Table 3.2: Implementation details of various orders.

3.4.1 Addressing the Issue of Dynamic Range Scaling

Unlike analog or discrete-time implementations which require dynamic range scaling, signal handling capability of this structure can be optimized by simply altering the size of the digital bus throughout the modulator to accommodate the wide ranging signal levels.

For the pole-zero locations described in section 2.3, it is found that the *a* coefficients follow the trend of $1 > |a_{i+1}| > |a_i|$ for all modulator orders. The magnitude of $a_{N/2}$, the *a* coefficient closest to the output, is usually found to be quite close to unity. Due to this distribution of coefficient magnitudes throughout the structure, signal amplitude in the first stage is always the smallest, followed by the second stage, and gets increasingly larger as it moves to the final stage. As a result, the bus between each stage can be resized such that under maximum input conditions, each bus handles signals just below the overflow limit (i.e. an L_∞ norm). Altering the size of the data path throughout the structure results in a smaller hardware overhead. To get an idea how much hardware saving can be achieved, consider an 8^{th}-order modulator with an n-bit input. If the normalized input amplitude is restricted to a maximum of 0.5 (with the quantizer's feedback being unity), the first stage datapath can be reduced to (n-3) bits, the second stage remained at n bits, the third stage increased to only (n+2) bits and the final stage to (n+3) bits. Compared to the conventional way of implementing the whole modulator using (n+3) bit datapath throughout, this saving has significantly reduced the hardware of the design. The stability of the modulator and its signal integrity was not compromised by this operation. This was confirmed by stimulating the realized ΣΔM with a white noise source and, later, a frequency modulated (FM) input signal.

Due to the above data path assignment, the *m* coefficients should be rearranged to accommodate the smaller bus sizes found in the first few stages of the modulator. To do so, the highest-indexed *m* coefficient (say for the eighth-order example, m_3) is assigned to be the smallest so that the effect of each *m* coefficients are almost equally pronounced at the output (recall that the *m* coefficients place the *NTF* zeros and thus suppress the in-band noise).

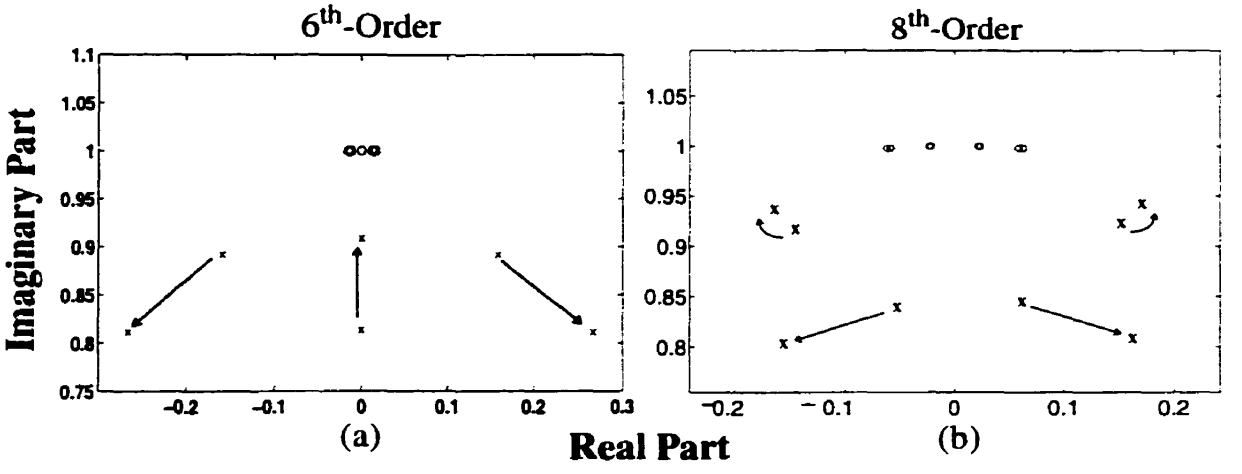


Figure 3.12: Effects of coefficient quantization on pole-zero locations: (a) 6^{th} and (b) 8^{th}-order.

3.4.2 Pole-Zero Plots

Figures 3.12 and 3.13 illustrate the pole-zero plots for the 6^{th}, 8^{th}, 10^{th} and 12^{th} -order *NTFs* before and after coefficient quantization. Arrows superimposed on each plot indicate the direction and magnitude of the pole movements. Clearly, large movements occurred in every case. Such movements suggest that lengthy simulations and/or real-time implementations are necessary to verify the stability of these modulators as the original theory used to select the design no longer applies. In spite of these large movements, all poles stay well within the unit-circle. This observation offers a good level of confidence in the stability and

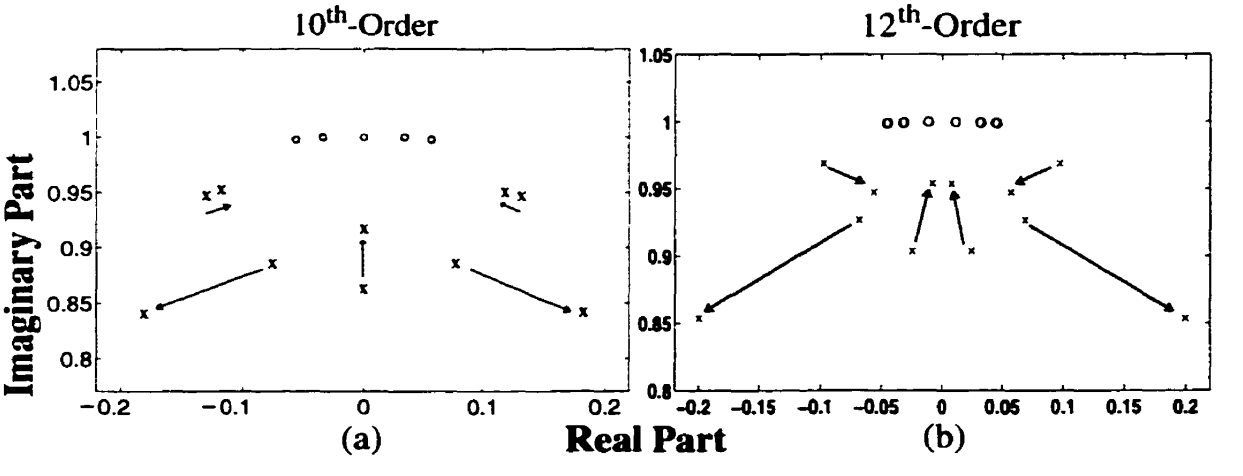


Figure 3.13: Effects of coefficient quantization on pole-zero locations: (a) 10^{th} and (b) 12^{th}-order.

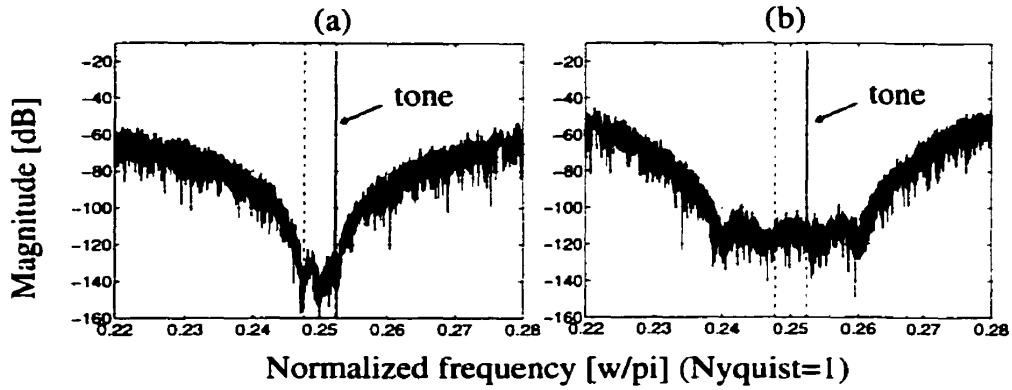


Figure 3.14: Experimental Results: (a) 6^{th} and (b) 8^{th}-order.

signal quality of the modulator. Although not very visible, the zeros have moved little from their intended positions and remain on the unit circle. This is indeed a highly desirable feature as it provides maximum noise suppression and some predictability in the expected SNR of the modulator after quantization.

3.4.3 Simulation and Experimental Results

Both the 6^{th} and 8^{th}-order modulators previously described were implemented using a Xilinx FPGA. As a particular reference, the 8^{th}-order modulator occupied about 55% of the CLBs on the Xilinx XC4010, with a compilation constraint of maximum 350 CLBs. The 10^{th} and 12^{th}-order designs were only simulated using MATLAB's Fixed Point Block Set (FPBS) simulator as they were too big for the XC4010.

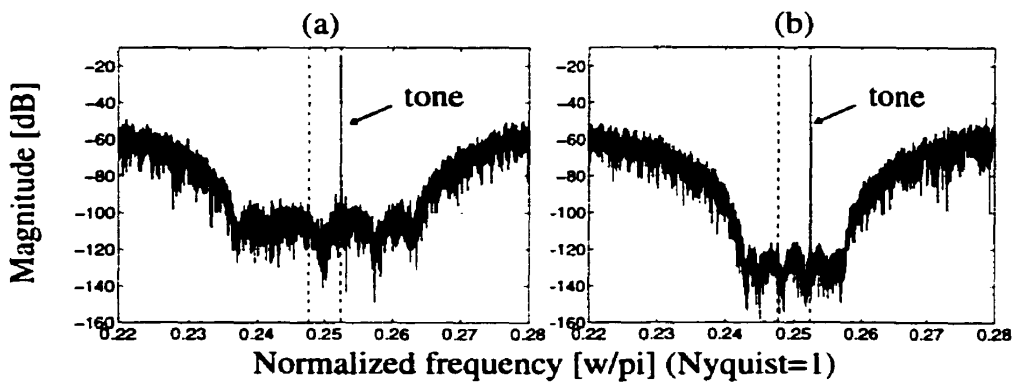


Figure 3.15: Simulation Results: (a) 10^{th} and (b) 12^{th}-order.

Figures 3.14 and 3.15 show the experimental and simulation results. From the 66,000 output bits collected, an FFT using a raised-cosine window was performed on the last 32,768 bits. As seen in both figures, a sinusoidal tone is placed in-band on frequency bin # 8273 (out of the 32768 points) with a normalized amplitude of 0.4. The noise shaping mechanism is clearly visible with deep notches in the passband region. The two dashed lines in each plot indicate the normalized frequency band of interest corresponding to 200 kHz when clocked at 42.8 MHz. FPGA implementations prove in real time that the proposed structure is capable of realizing stable modulators. All four cases easily meet both the bandwidth and SNR requirements. Moreover, the 8^{th}, 10^{th} and 12^{th}-order structures do so with plenty of extra bandwidth to spare. Hence, one can trade-off digital hardware complexity for lower-Q analog recovery filters.

3.4.4 BiCMOS Implementation

Since the operation and stability of the design have been confirmed with FPGA implementations, the goal of migrating the design to BiCMOS is to investigate the speed enhancement offered by the technology.

Fig. 3.16 illustrates the circuit schematic of this implementation. As explained in subsection 3.4.1, the modulator can be partitioned into stages and different bus sizes can be assigned to each stage. For this particular example, the number of bits are indicated in brackets on the figure. Also, as mentioned in subsection 3.2.1, the critical path of this modulator is the combinational-logic path between the two registers in stage 4, owing to the largest data path assigned and hence the two largest adders.

Shown in Fig. 3.17 is the microphotograph of a CODEC integrated circuit (IC): a bandpass $\Sigma\Delta$ A/D and D/A system that is equipped with built-in-self-test circuitry. The entire IC measures (5 x 5.5) mm^2 and the 8^{th}-order modulator for the D/A converter was implemented in a small part in the sea of digital gates. The design occupied an area of 2.1 mm^2, compiled for a clock of 42.8 MHz. Please refer to [49] for documentation on the analog-to-digital converter and [51] on the RAM usage. Unfortunately, the input and control data were found to be corrupted before the modulator could be tested. This is possibly due to

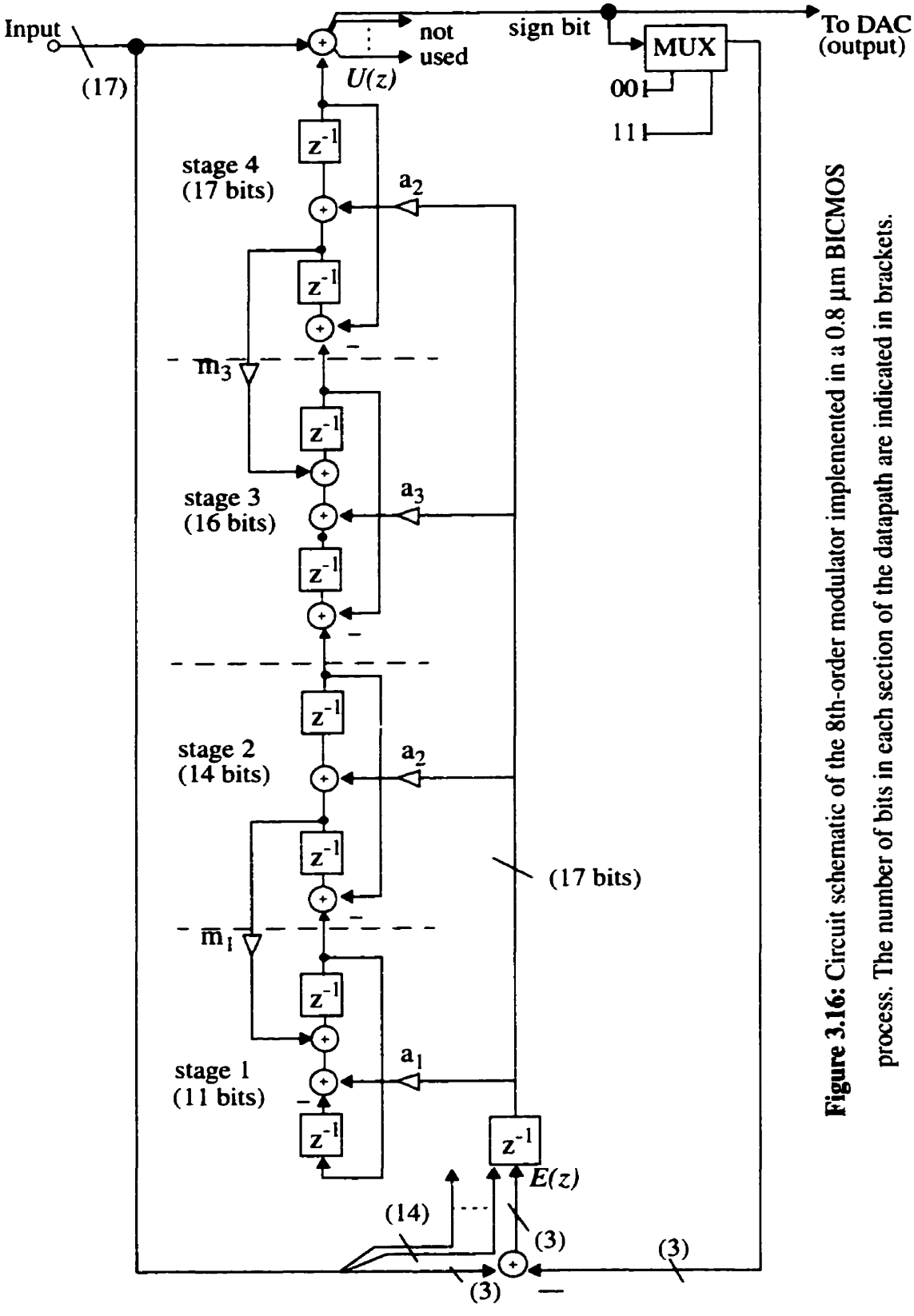


Figure 3.16: Circuit schematic of the 8th-order modulator implemented in a 0.8 µm BICMOS process. The number of bits in each section of the datapath are indicated in brackets.

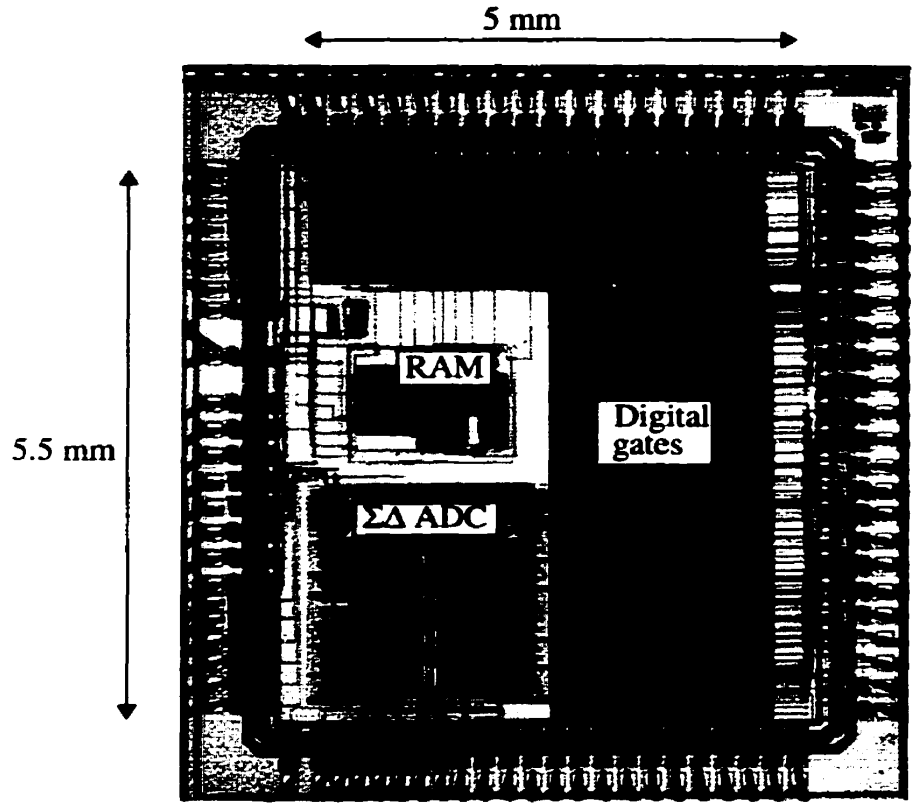


Figure 3.17: A CODEC microphotograph

software or place-and-route errors undetected during the design phase. Thus, no results are available to establish the speed comparison between the FPGA and BiCMOS implementations.

3.5 Conclusions

The proposed structure has been shown capable of implementing variable-bandwidth high-order bandpass digital sigma-delta modulators without multipliers. High speed operation is made possible as only two adders appear in the critical delay path regardless of the modulator order. Zero locations are fixed on the unit circle providing near-optimum noise suppression. Simulation and experimental results prove that this was achievable for 6^{th}, 8^{th}, 10^{th} and 12^{th}-order modulators.

Chapter 4 : A Bandpass Filter For Analog Reconstruction

Using the proposed structure described in the previous chapter, an efficient implementation is now available to realize high-order ΣΔ modulators in bandpass digital-to-analog converters. Depending on the applications, a post-processing step is usually necessary to suppress the shaped quantization noise for signal decoding. In the second part of this thesis, a high frequency filtering approach using active inductors is examined as a fully integrated solution for recovering the analog information from a bandpass ΣΔ bitstream.

Specifically, a 6^{th}-order elliptic LC bandpass filter centered at 300 MHz with 50 MHz bandwidth will be constructed to handle this post-processing task. In order to avoid spiral inductors, a novel design of a silicon all-NPN floating active inductor is created. Thus, with this component simulation approach, the filter design problem reduces to the design of an active inductor circuit. Using a 0.8 μm BiCMOS technology with the NPN f_T's at 11GHz, inductance values in the range of 10 - 70 nH can be realized on-chip for filter applications. These inductance values have a corresponding Q factor ranging from 6 to 23 in the UHF range. Simulation and experimental results are provided to illustrate the operation of this 6^{th}-order filter using the novel floating active inductor circuit.

In exploring this filtering method, approaching the speed limit of the technology is desired to enhance the research values of this work. This will be attempted assuming the bandpass ΣΔ bitstream can be provided at such frequencies. The work of the previous chapter was limited to less than 50 MHz, however, another technique using periodic ΣΔ modulated streams [31] can be employed for this high frequency signal generation.

4.1 Introduction

Among the three basic passive components, i.e. R, L and C, the inductor remains the most difficult component to integrate on a silicon chip. Today we are seeing numerous applications involving spiral inductors in the UHF (300 MHz - 1 GHz) and greater range. However, spiral inductors suffer from high series resistance, undesirable resonance due to parasitic capacitance and large area occupation. To circumvent these shortcomings, this work is concerned with the creation of a fully monolithic active inductor (**AI**) for similar applications. The idea of an AI can be traced back to the work of Tellegen in 1948 where he introduced the idea of a gyrator and subsequently, the active inductor [32]. This component was first used in the sixties to realize active filters for UHF and even higher frequencies [33]. In fact, AIs have made high-Q tunable LC filter structures realizable in monolithic form, e.g. [11], and its size independent of the inductance value.

Filters using AIs have good potential to operate at high frequency near the active device f_T since the device parasitic is used in its operation. Recent demonstration of a MESFET AI design by ATR in Japan [34] has created considerable interest in this approach for microwave monolithic integrated circuit (MMIC) applications. However, the high output conductance of a MESFET, denoted g_{ds}, was shown in [35] to degrade the gyrator performance by increasing its **equivalent series resistance, Rs,eq**. This drawback favors the use of bipolar junction transistors (BJTs) instead which have much higher output resistance, r_o. It was claimed in [35] that comparable performance can be achieved with a much slower and cheaper BJT process since the high f_T of a MESFET has only a few benefits in these applications. Further, the finite *Beta* of a BJT (~100) has almost no effect on the performance of the AI circuit. With respect to comparable MESFET transconductance, BJTs lower operating current and lower $V_{ce,\,sat}$ are welcome features for low voltage or low-power applications.

The drawback documented for using BJTs is the base-spreading resistance which can be partly eliminated by using an appropriate transistor structure with multiple base contacts and a long stripe-shaped emitter region [36]. A typical layout of this structure and its cross-

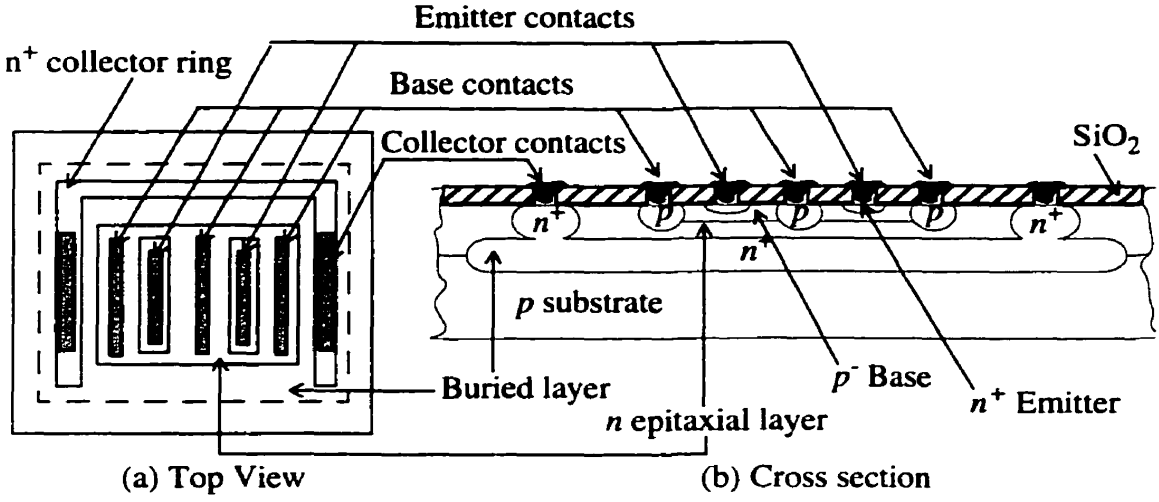


Figure 4.1: (a) Layout and (b) cross-sectional view of a high-frequency BJT.

sectional view is illustrated in Fig. 4.1. In fact, the base spreading resistance becomes the only resistive part of the input impedance at high frequency when r_π is ignored. Thus, a reduction in this resistance will enable the transistor to operate at higher frequency. In this work, NPN transistors used along the signal path will have layout features similar to this structure.

In this chapter, an LC ladder, with its passive inductors replaced by AI circuits, is built to perform bandpass filtering. Section 4.2 discusses the synthesis of LC ladders and AIs at a topological level. A novel floating AI, consisting of only transistors, is then presented in Section 4.3. In Section 4.4, the impedance characteristics of this AI are computed using HSPICE simulations. A 6^{th}-order elliptic band pass filter (**BPF**) using this floating AI is documented in Section 4.5. The layout of this filter was performed in a 0.8 μm BiCMOS process. Small-signal frequency analysis and transient responses of the extracted layout are provided. Frequency response and a two-tone test result of the fabricated chip will be documented at the end of the same section.

4.2 Background Theory

A passive LC-ladder network, using inductors and capacitors, is one of the oldest technique for filter realizations. A doubly terminated LC ladder is commonly formed by series/paral-

Table 4.1: The normalized LC-ladder component values.

R_S	1 Ω	R_L	1 Ω
C1	20.26 F	L1	0.05278 H
C2	6.126 F	L2	0.2639 H
C3	3.157 F	L3	0.2073 H
C4	20.26 F	L4	0.05278 H

lel combinations of inductors and capacitors, operated from a resistive source and terminated into a resistive load. Since the combinations of inductors and capacitors in between are lossless, maximum source power can be delivered to the load at passband frequencies. It can be shown that the sensitivity for the filter gain due to component variations is zero at the attenuation zeros [38] and remains relatively low at other frequencies in the passband. This property of LC ladders is highly desirable for monolithic realizations in which component variations are unavoidable.

In LC-ladder design, the component values are usually obtained for various filter specifications using computer programs [39] or tabulated data [40]. Shown in Table 4.1 are the normalized LC values given in [40] for a sixth-order elliptic bandpass filter depicted in Fig. 4.2. Its LC-network consists of only series/parallel combinations of LC-tank circuits. In Section 4.5, this ladder will be frequency and impedance scaled to the desired ranges in order to work with practical component values and operate at the appropriate frequencies. To perform impedance scaling, all inductance and resistance values are multiplied by a constant while all capacitance values are divided by the same constant. Since only the impedance level is scaled, this operation will not result in a change in the quality factor or frequency of the ladder. The passband center frequency can be shifted without altering the

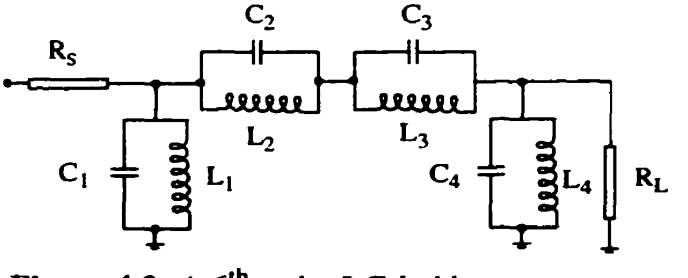


Figure 4.2: A 6^{th}-order LC-ladder prototype.

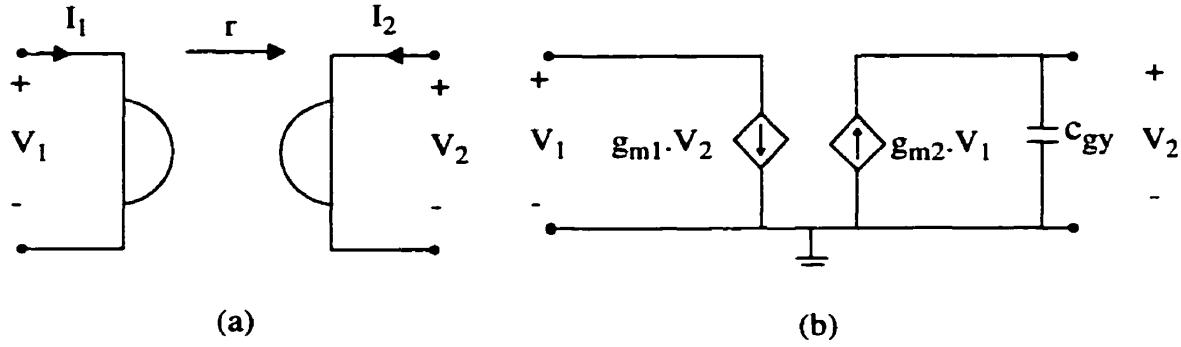


Figure 4.3: (a) A gyrator network symbol and (b) A realization of a grounded active inductor using two VCCSs.

filter shape using frequency scaling. This is achieved by dividing all inductance and capacitance values by a constant. Since a resistor is not a frequency dependent component, it will be left untouched in this denormalization process.

Due to the difficulty of integrating high quality passive inductors on a silicon chip, it seems advantageous to simulate the passive LC-ladder filters in active forms to exploit the low sensitivity property of the network. One of such active realizations is called the component simulation approach where the inductor's behavior is simulated in time and frequency. This can be achieved using a capacitively loaded gyrator [41]. Thus, in this active realization, the gyrator design becomes the main task and this topic will be discussed next.

4.2.1 Gyrator Design

An ideal gyrator is a passive, non-reciprocal two port network as shown in Fig. 4.3(a). It can be characterized by its gyration resistance, r, and its orientation as described by the following z-parameter matrix [32]

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & -r \\ r & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{4.1}$$

With two voltage-controlled current sources (VCCSs), the above relationship can in turn be used to realize a grounded AI [37] by terminating port 2 with a capacitor, c_{gy}, as illustrated in Fig. 4.3(b). Mathematically, this implementation can be described by Eq. (4.1) when r is replaced by $1/g_m$ and it can be shown that the realized inductance is given by

$$L = \frac{C_{gy}}{g_{m1} \cdot g_{m2}}.$$

Based on this concept, there have been numerous designs which realized single-ended active inductors using active elements such as operational amplifiers [42] or operational transconductance amplifiers (OTAs) [43] - [45]. Using transconductors, the block realization is illustrated in Fig. 4.4(a) for a grounded gyrator. As labeled in Fig. 4.4(a), the voltage-current relationship is identical as the two VCCS realization introduced earlier. The grounded active inductor, consisting of an inverting and a non-inverting transconductor, is terminated with a linear capacitor. A floating gyrator is required for the simulation of a floating inductor. As demonstrated in Fig. 4.4(b), the grounded gyrator can be extended to a floating design [46] using two grounded gyrators connected back-to-back. This floating active inductor is made up of four transconductors loaded with a grounded capacitor.

Alternatively as proposed in [34], the VCCSs in Fig. 4.3(b) can be realized using transistors instead of OTAs and the linear capacitor replaced by the device's parasitic capacitance. Due to the use of these parasitic capacitances, this design approach has good potential to operate at high frequencies. Thus, to explore the speed limitation, this approach will be adopted in the design of active inductors in the next section. This realization will be demonstrated using real transistors in various high frequency amplifier configurations, for example, as a common-base stage. AC-coupling capacitors, a common component for biasing, will be excluded from the biasing scheme, as they usually consume large silicon area, limit the lowest usable frequency and increase **Rs,eq**.

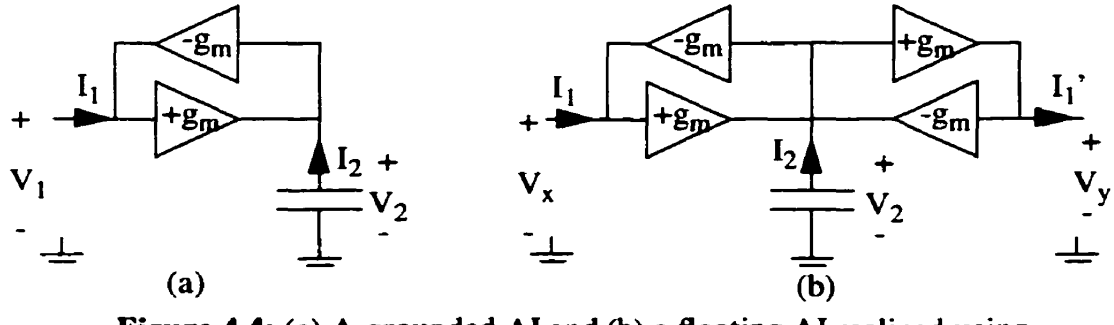


Figure 4.4: (a) A grounded AI and (b) a floating AI realized using transconductors.

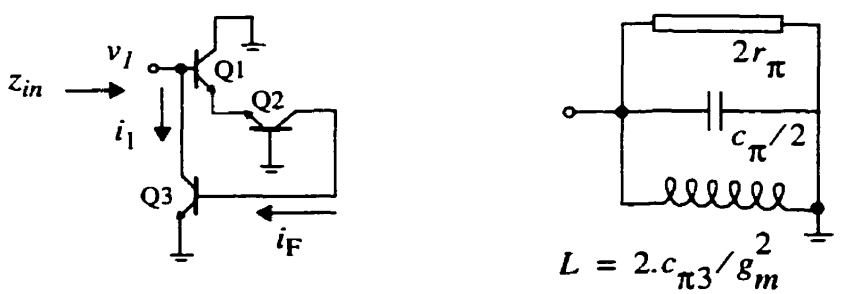
4.3 Active Inductor Design

As described in the previous section, a floating AI circuit design commences with the development of a grounded AI. Without the biasing circuitry shown, Fig. 4.5(a) illustrates how this can be done with three BJTs. By combining a common-collector common-base configuration (Q1, Q2) with a common-emitter stage (Q3), the input impedance seen looking into the base of Q1 is inductive.

For a brief description of the circuit operation, only two small signal parameters, g_m and c_π of a BJT will be considered and they are assumed to be identical among the three BJTs. By applying a test voltage v_1 at the input port in Fig. 4.5(a) a feedback current $i_F = g_m \cdot v_1/2$ is generated which charges up $c_{\pi 3}$. This in turn creates an input current, $i_1 = v_1 \cdot g_m^2/(s \cdot 2 \cdot c_{\pi 3})$. From this expression of i_1, we can calculate

$$z_{in} \equiv \frac{v_1}{i_1} \equiv s \cdot 2 \cdot c_{\pi 3}/g_m^2, \tag{4.2}$$

where we see that the idealized input impedance is purely inductive with a value of $(2 \cdot c_{\pi 3})/g_m^2$. This inductance value can be adjusted by changing the collector current of each BJT, which in turn alters g_m, thereby making tuning possible after circuit fabrication. This simplified small signal equivalent circuit closely matches the VCCS realization of the gyrator in Fig. 4.3(b) with $c_{gy}=c_{\pi 3}$. Referring to Fig. 4.5(a) again, it is observed, after converting the circuit to its hybrid-Π model, that the input terminal is connected to ground



(a) (b)

Figure 4.5: (a) A single-ended AI design and (b) its equivalent passive counterpart.

through two main paths. The first consists of the base-emitter circuits of Q1 and Q2, i.e. the two r_π // c_π series connection. Since Q3 generates the inductive current, looking into the collector of Q3 an inductor is seen connected to ground. Based on the previous descriptions, this grounded inductor can be represented by its passive counterpart as shown in Fig. 4.5(b). Using this model, more detailed analysis reveals that

$$z_{in} = \frac{s \cdot 2 \cdot c_{\pi 3}}{s \cdot c_{\pi 3}/r_\pi + s^2 \cdot 2 \cdot c_\pi \cdot c_{\pi 3} + g_m^2}, \tag{4.3}$$

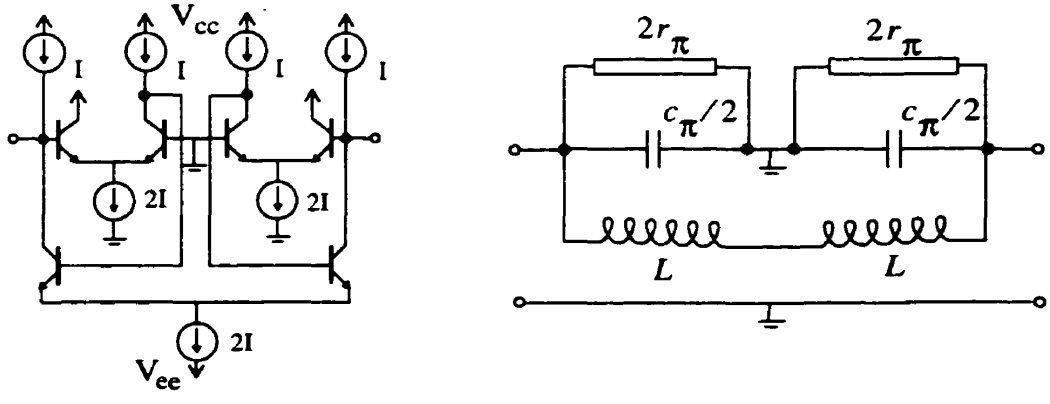
where:

r_π, c_π = base input impedance of Q1 or Q2,

$c_{\pi 3}$ = emitter-base capacitance of Q3, and

$g_m = g_{m2} = g_{m3}$ = transconductance of Q2 or Q3.

Besides inductance, the effects of the undesirable components are also captured by Eq. (4.3). The first term beginning from the left-hand side of the denominator contributes to **Rs,eq** and the second term indicates a very high frequency self resonance. Nevertheless, since a transistor is a distributed-parameter network, especially at high frequency, the analytical computations performed here based on a lumped-component circuit model are not



(a) (b)

Figure 4.6: (a) A floating active inductor and (b) its equivalent passive counterpart.

expected to be very accurate and we will rely on simulations to provide us with a more refined model of the circuit behavior instead (albeit, also a lumped-component simulation).

In **BPF** applications, floating AIs are usually required if the LC ladder is mapped from a lowpass prototype. A technique to float inductors that exhibits fully symmetrical two-port characteristics was proposed in [47]. Using a similar configuration as the floating AI in Fig. 4.4(b), this technique involves duplicating the single-ended half circuit to develop a differentially paired configuration. The final design of the AI used in this work was created with this approach leading to the circuit shown in Fig. 4.6(a) with complete biasing details shown. This scheme avoids the use of DC decoupling capacitors and potentially allows the circuit to operate at lower voltage supply. The simplified equivalent passive circuit of this floating inductor, derived in the same manner as the single-ended case, is illustrated in Fig. 4.6(b).

4.4 Inductance Realization

According to Eqn. (4.2), different inductance values can be realized by varying c_π/g^2_m (i.e. different NPN sizes) while maintaining roughly the same level of current biasing. This is desirable because current magnitudes of the same order can be generated by the same type of current source and allow g_m to be tuned easily. For the floating inductor of Fig. 4.5(a),

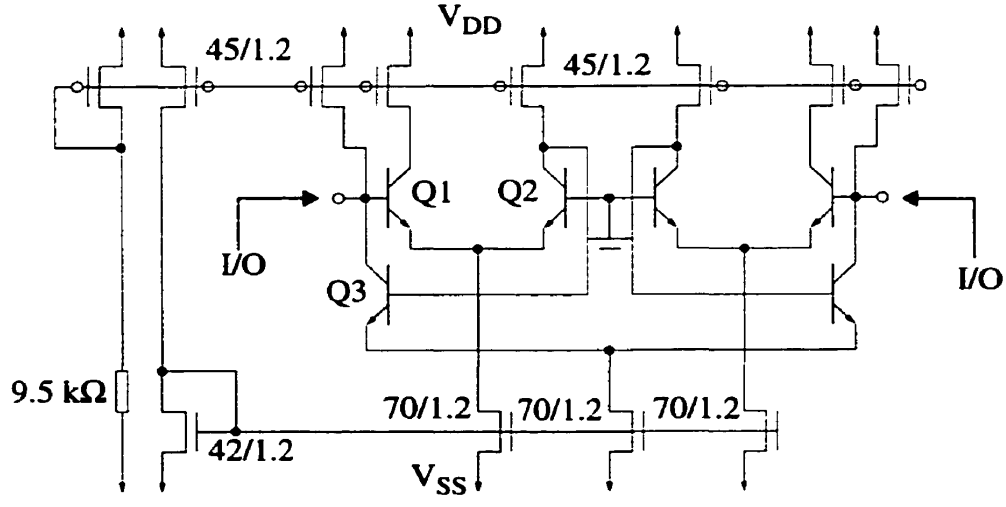


Figure 4.7: The schematic of a 14 nH active inductor.

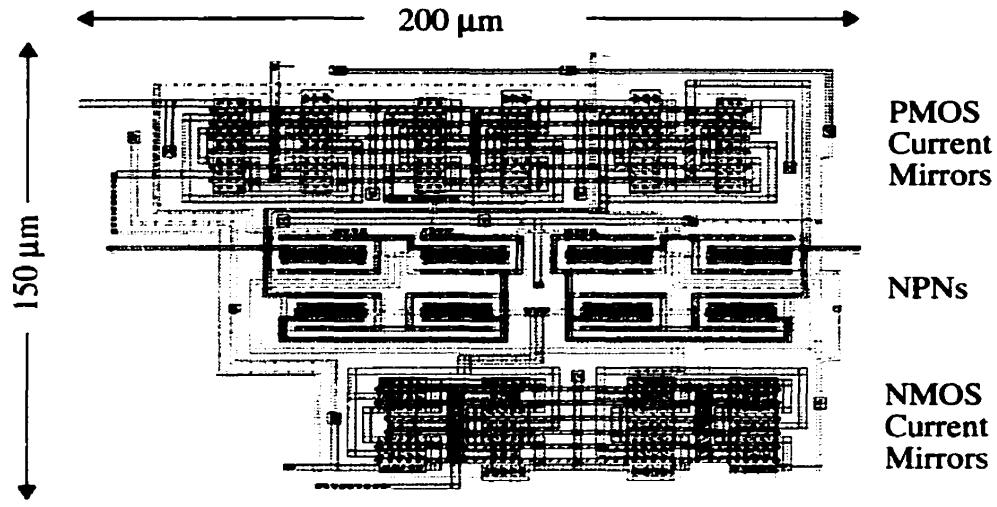


Figure 4.8: The layout of a 14 nH active inductor.

it was found that inductance values ranging between 10 nH and 70 nH were best achieved with different sizes of high speed NPN structures available in this 0.8µm BiCMOS technology. Fig. 4.7 depicts the schematic of a 14 nH AI. Q1 and Q2 are NPN type NN52F12X while Q3 is NN52F24X. The simple current sources were implemented using only MOS mirrors. Their W/L ratios are shown on the figure in brackets. The two input/output terminals are indicated as I/O in the figure. The 9.5 kΩ biasing resistor was left off-chip for ease of tuning. The corresponding layout of this AI is shown in Fig. 4.8. The actual cell is biased at a current level of 500 µA. The cell occupies an area of 0.2 x 0.15 mm^2 with the high speed NPNs sandwiched between the PMOS and NMOS simple current mirrors. Similarly, another cell was created with a nominal inductance of 65 nH having very similar feature sizes but biased at 100 µA.

Both AIs were extracted from layout, including the parasitics, and simulated with HSPICE. Fig. 4.9(a) illustrates the inductance values as a function of frequency and part (b) magnifies the details in the 0.1 to 1 GHz range of interest. Simulation reveals relatively constant inductances up to 1 GHz with the circuit's parasitic effect surfacing at higher frequency (above 1 GHz). The 14 nH inductor demonstrates a constant inductance value in the UHF range before its inductance turns negative. Over the same frequency range, the 65 nH inductor, on the other hand, is less constant but is acceptable for narrow band applications.

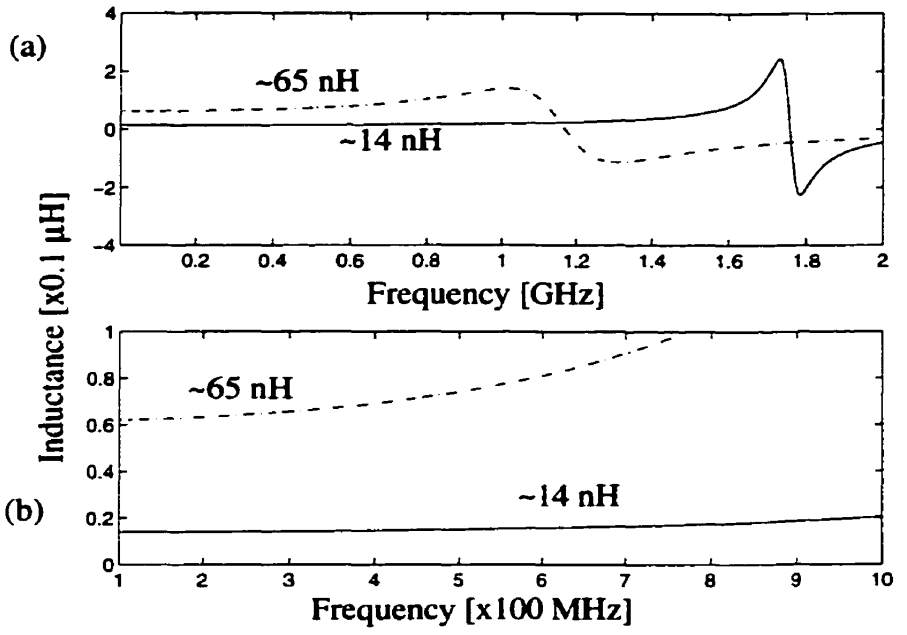


Figure 4.9: The realized inductance values: (a) up to 2 GHz and (b) a zoom into the range of 0.1 - 1 GHz.

With an identical frequency axis, Fig. 4.10 shows the simulated equivalent series resistance, $R_{s,eq}$, for the corresponding inductors. Needless to say, this resistance should be min-

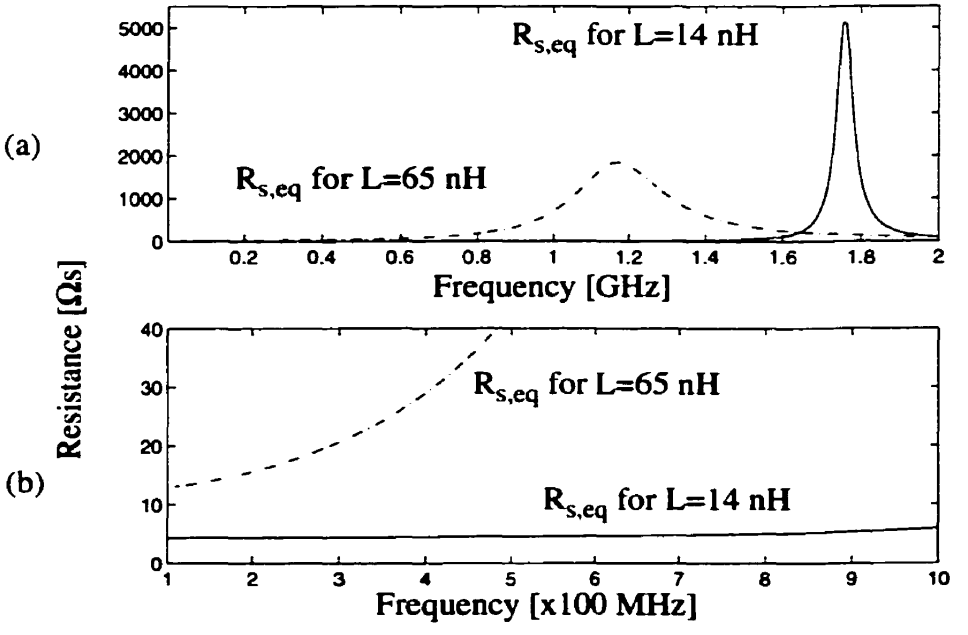


Figure 4.10: The corresponding equivalent series resistance:(a) up to 2 GHz and (b) a zoom into the range of 0.1 - 1 GHz.

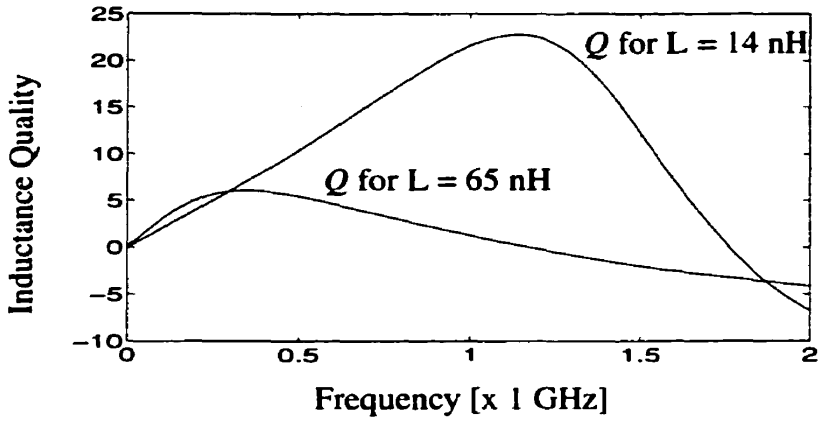


Figure 4.11: The inductor quality factor versus frequency.

imized in order to maintain the desired filter behavior. However, pushing this quantity to very low values, under process variations, may result in instability due to excessive positive feedback. Hence, it is important to reduce Rs,eq especially in the frequency band of interest while keeping it at a reasonable positive value. For the 300 MHz center-frequency filter of this work, this resistance was held in the range of 3 to 25 ohms, resulting in rather low Q's. As displayed in Fig. 4.11, the quality factor ranges between 5 to 9 around the signal band. The quality factor of the 14 nH inductor peaks with a value of 23 at 1 GHz because its series resistance is close to zero at those frequencies. As will be shown in subsection 4.5.2, this range of Rs,eq does not significantly influence the filter shape and its out-of-band noise suppression.

4.5 A Sixth-Order LC-Ladder Example

In order to investigate the performance of the novel floating AIs, an LC 6^{th}-order elliptic BPF shown in Fig. 4.12(a) was synthesized. Obtained from a filter design table [40] as first discussed in Section 4.2, this ladder was frequency level scaled to have a 3 dB passband ripple over a bandwidth of 50 MHz, centered at 300 MHz. The proposed filter was realized with double-poly capacitors and its inductors replaced by the tunable AIs. Thus, with this technique, a BPF synthesis was reduced to the AI design demonstrated in the previous two sections.

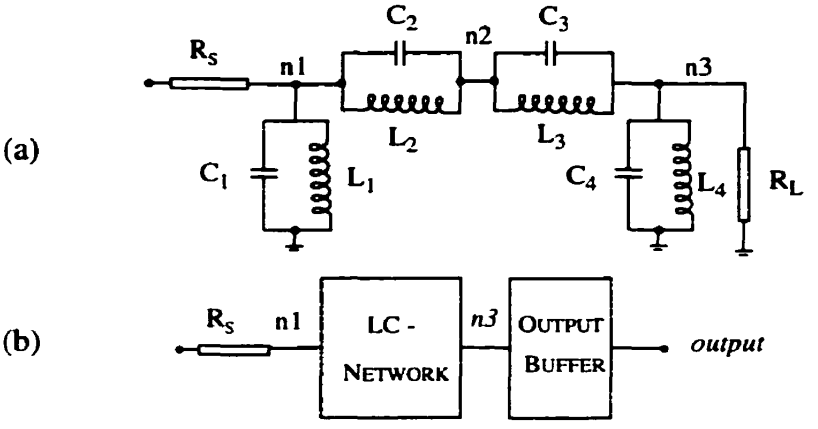


Figure 4.12: A 6th-order LC-ladder prototype.

Table 4.2 lists the components values of this ladder. Note that the ladder impedance level was scaled to 500 Ω so that all inductance values fell in the realizable range of the AIs. In synthesizing this ladder, the spread of the inductance values was closely monitored and intentionally minimized because large spread would require the active inductor circuit to implement a wider range of inductance values. To simplify the tuning process, both L2 and L3 were designed to be the same at 65 nH. On chip, all four inductors can be tuned to give better selectivity and balance in shape. However, as we discover in Section 4.5.5, tuning the filter for the desired passband response with four degrees of adjustment freedom does create some tuning problems. For modularity in layout, only floating AIs were used to implement the inductors in the filter, even though L1 and L4 could be realized with grounded inductors.

Table 4.2: The LC-ladder component values at 300 MHz

R_S	500 Ohms	R_L	500 Ohms
C1	20 pF	L1	14 nH
C2	6.75 pF	L2	70 nH
C3	3 pF	L3	55 nH
C4	20 pF	L4	14 nH

4.5.1 Impedance Matching Output Buffer

Since the ladder's load was 500 Ω and the characteristic impedance of the transmission line was 50 Ω, a buffer was required to match the impedances between node *n3* and the output, as shown in Fig. 4.12(b). This buffer was realized by a single-ended wideband amplifier without feedback and its current sources by simple MOS mirrors. As depicted in Fig. 4.13, the first stage consisted of a common-collector transistor Q1 followed by a common-base stage Q2. The output of the amplifier was then buffered and level-shifted twice by two cascaded common-collector stages, consisting of transistors Q3 and Q4. Besides buffering, the stage consisting of transistor Q4 also provided an output resistance, R_{out}, matched to the load for maximum power transfer (i.e. $R_{out}=R_{LINE}$). Small-signal analysis reveals,

$$R_{out} \cong r_{e4} + \frac{r_{e3}}{\beta} + \frac{R_c}{\beta^2} \tag{4.4}$$

and for $\beta = 100$, Eq. (4.4) can be simplified to,

$$R_{out} \cong r_{e4} = \frac{V_T}{I_3} = 50\Omega . \tag{4.5}$$

Here I_3 was set to 500 μA and the thermal voltage V_T was assumed to be 25 mV. The coupling capacitor C_c was selected to be 100 pF so that its voltage drop was insignificant over the desired frequency band.

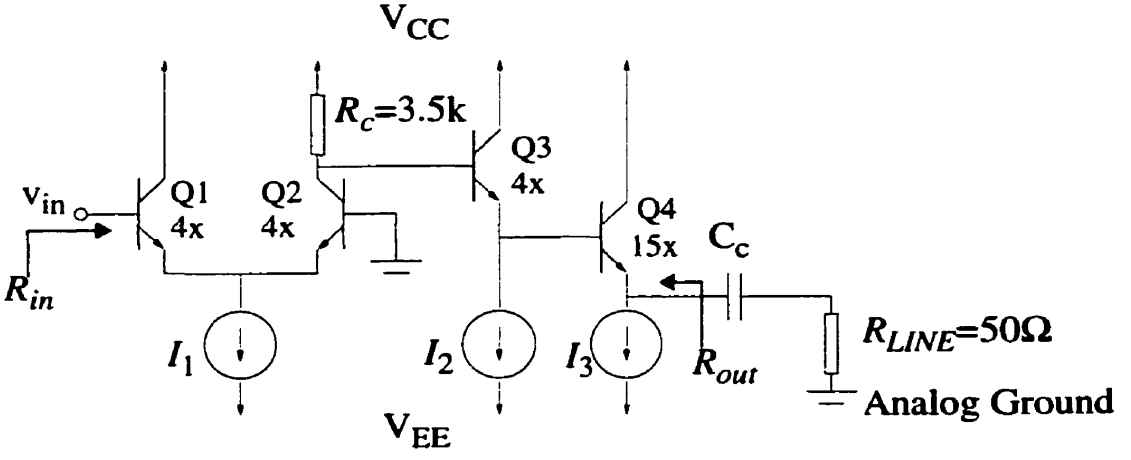


Figure 4.13: The schematic of the output buffer.

With the introduction of this buffer between the ladder and the transmission line, the input impedance of this output buffer, R_{in}, or the load of the ladder, R_L, had to be adjusted so that

$$R_{in} \parallel R_L = 500\Omega. \tag{4.6}$$

For $\beta = 100$, $I_1 = 500\ \mu A$,

$$R_{in} = 2 \cdot r_\pi = 4 \cdot (\beta + 1) \cdot \frac{V_T}{I_1} = 20,200\Omega. \tag{4.7}$$

Thus, R_L was modified to 513 Ω to satisfy Eq. (4.6).

Besides impedance matching, this output buffer was also designed to supply a 20+ dB of signal gain. Detailed analysis shows that the voltage gain of the buffer is governed by the following equation,

$$A_v = A_{v3} \cdot A_{v4} \cdot \frac{1}{2} \cdot g_m \cdot R_c, \tag{4.8}$$

where A_{v3} and A_{v4} are close to unity due to the common-collector configuration of Q3 and Q4. For $R_c = 3.5$ kΩ and $g_m = 10$ mA/V, Eq. (4.8) gives $A_v \sim 25$ dB (17 V/V). This gain, measured before the coupling capacitor C_c, is reflected in the low frequency region ($< 5 \times 10^8$ Hz) in Fig. 4.14(a). At 300 MHz when measured after the coupling capacitor, this gain

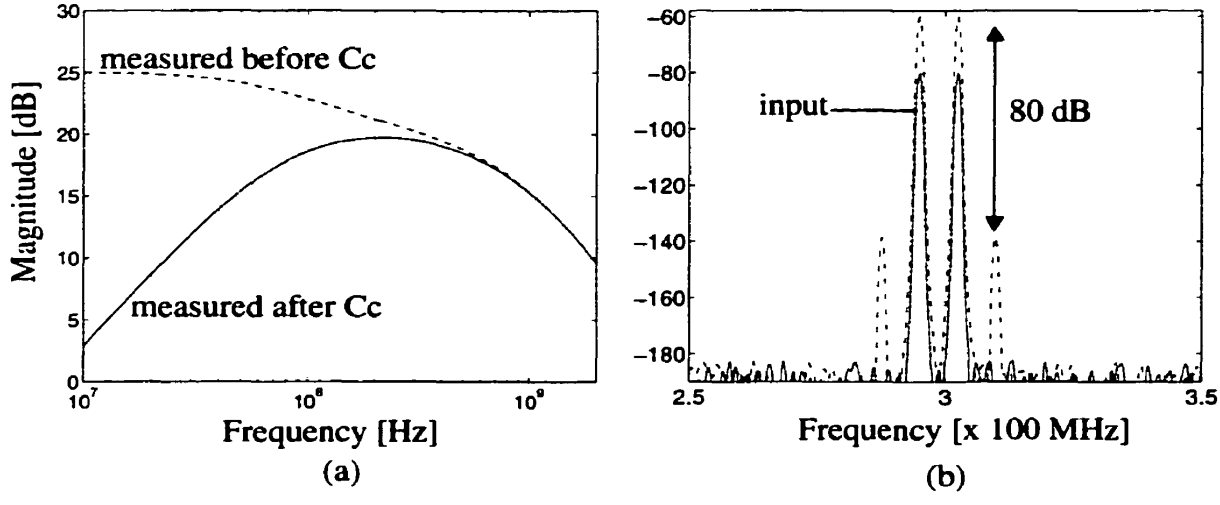


Figure 4.14: Two simulated results associated with the output buffer: (a) frequency response before and after the decoupling capacitor C_c, (b) a two-tone distortion test.

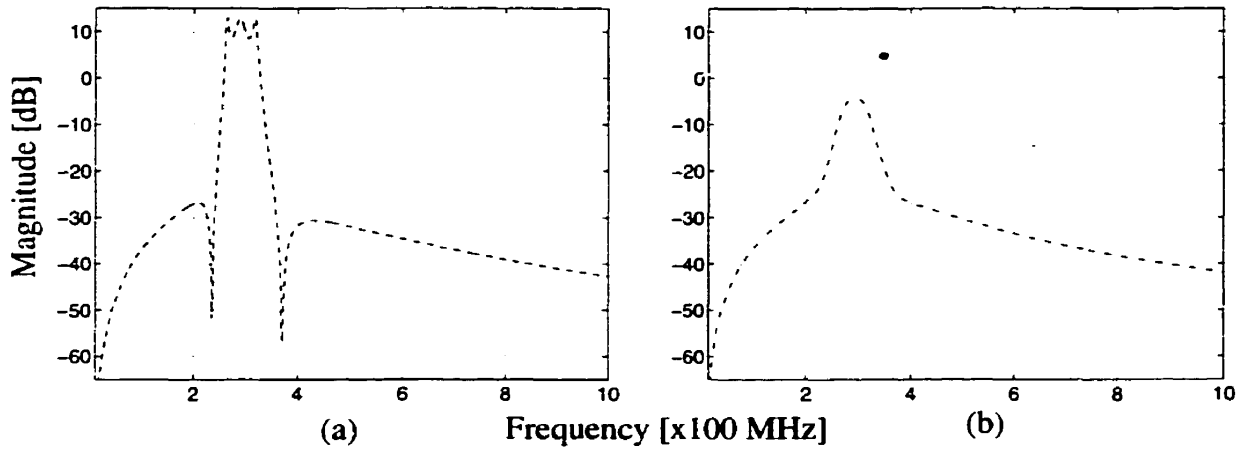


Figure 4.15: The small-signal frequency analysis results: (a) ideal ladder with passive inductor, (b) ideal ladder with lossy passive inductors.

drops to ~20 dB (11 V/V). In the low frequency region, we see that the gain is attenuated by this capacitor. Since this buffer will be placed in cascade with the LC ladder, it was important to ensure that it was at least as linear as the LC ladder. To investigate its linearity, a two-tone test was performed where the amplitude of each tone of the stimulus was set to 0.2 $mV_{p\text{-}p}$. The results are shown in Fig. 4.14(b). Here we see that about 80 dB SFDR (spurious-free dynamic range) was achieved. Through simulation, we shall see in subsection 4.5.3 that the linearity of the entire filter was indeed limited by the LC ladder, i.e. the active inductor circuits.

4.5.2 Small -Signal Frequency Analysis

Returning to the simulated 6^{th}-order LC ladder realization, Fig. 4.15 and 4.16 illustrate the small-signal frequency responses as computed by an HSPICE AC analysis. Fig. 4.15 contains the filter's magnitude responses when the inductors were modeled either as (a) ideal or (b) lossy ($R_{s,\,eq}$~ 3 or 20 Ωs depending on the corresponding inductance values of 14 or 65 nH). The lossy case was necessary to verify the AI operation later on in this section. In Fig. 4.15(a), the ideal ladder's response has a 3 dB passband ripple and approximately 40 dB out-of-band suppression. When modeled with lossy inductors, the passband ripple and the transmission zeros are lost while the passband gain drops by 15 dB as captured in Fig. 4.15(b). Examining the frequency response of the active circuit extracted layout in Fig.

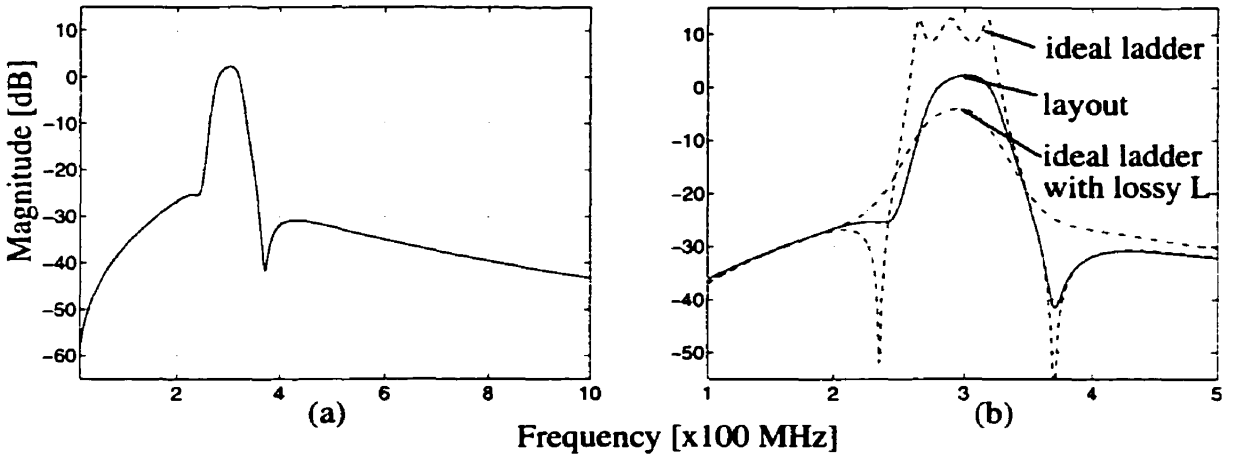


Figure 4.16: The small-signal frequency analysis results: (a) extracted layout, (b) a comparison among (a), the ideal ladder and the ideal ladder with lossy inductors.

4.16(a), we see that the passband gain drops by about 8 dB from the ideal case and the effects of the transmission zeros are less obvious. For precise comparison, these three plots are superimposed in Fig. 4.16(b). The similarity in shape and center frequency shared by the extracted layout and the ideal ladder with lossy inductors shows that the simulated and ideal inductance values are very close. Hence, the AIs are in fact unaffected by the loading of the ladder. With similar ladder component values, this comparison shows that the layout response deviates from the ideal case in terms of passband gain but not the out-of-band suppression. As will be illustrated in the next subsection, this unchanged out-of-band

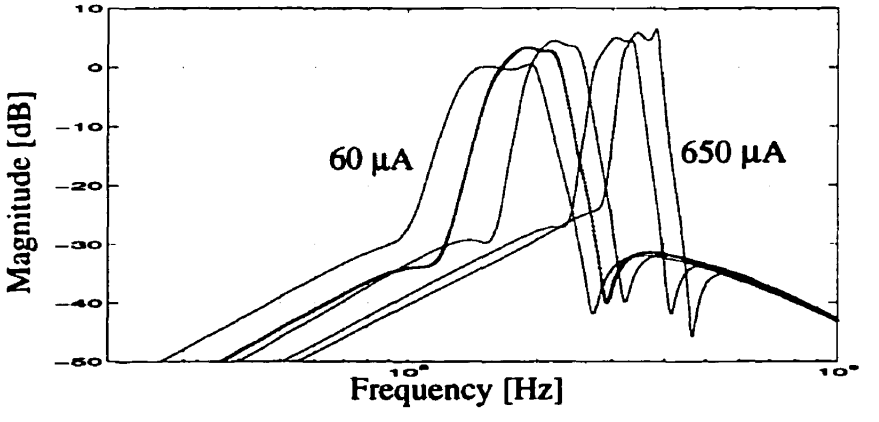


Figure 4.17: An illustration of the effects of tuning by altering the bias current from 60 µA - 650 µA.

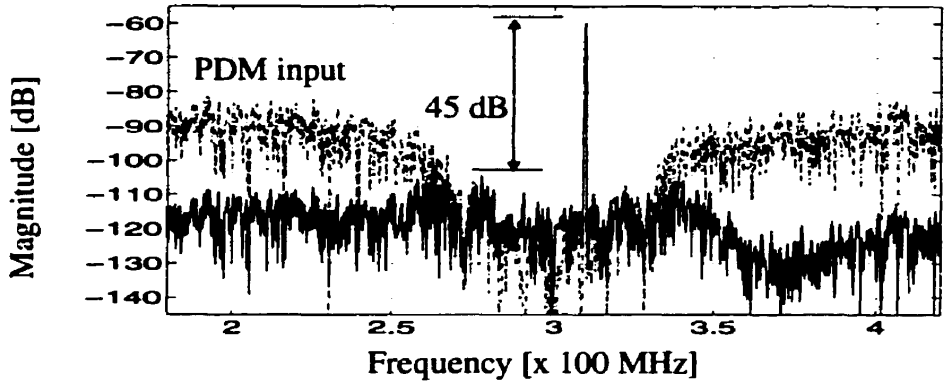


Figure 4.18: The frequency response of the filter to a PDM input.

suppression is crucial in the application of ΣΔ bitstream filtering while the passband loss, even though undesired, can be compensated by the buffer gain.

To demonstrate the frequency tunability of this filter, the bias current of each AI was varied over the range of 60 - 650 μA to realize different inductance values. According to Eq. (4.2), higher current level would yield lower inductance which would in turn shift the signal band to higher frequency. The results of this tuning are illustrated in Fig. 4.17 where the center of the signal band was varied in a range of 180 to 380 MHz. Since decreasing the bias current has the effects of increasing both the inductance value and its $R_{s,\,eq}$, independent inductance tuning was not possible without changing the quality factor of the AIs. Due to this condition, it could be observed that the filter passband gain was decreasing as the filter was tuned towards low frequencies.

4.5.3 Transient Analysis

Armed with an idea of the filter's frequency response, transient analysis was then carried out. As mentioned in the beginning of the chapter, the main application of this LC ladder is to filter out the shaped quantization noise contained in a bandpass ΣΔ bitstream. In order to investigate how this particular wide-band noise distribution was handled by the filter, an 8 mVp-p sigma-delta pulse-density modulated (PDM) square wave containing a 310 MHz sinusoid was applied to its input. This simulation was carried out for 7 μs with a time step of 0.1 ns. The output of the filter was then analyzed for its frequency content using an *FFT*. The result is shown in Fig. 4.18 where it can be seen that the filter effectively removes the

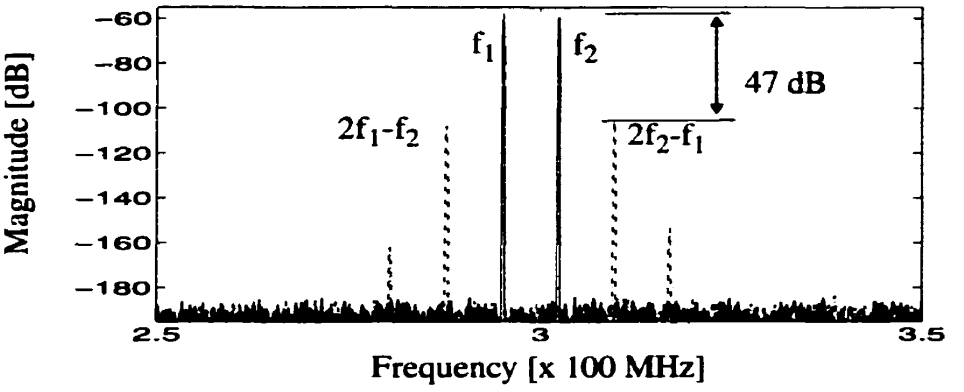


Figure 4.19: The response of the filter to a two-tone input.

out-of-band noise surrounding the main sinusoidal signal at 310 MHz. This shows that the filter is suitable as a reconstruction filter for a ΣΔ bitstream albeit with its considerable passband gain loss. This result also confirms the small-signal stability of the filter subject to an input rich in harmonics.

Due to the use of transistors and parasitic capacitances in the AI, it is also necessary to examine the linearity of the filter. To do so, a two-tone test was performed using two 2 mVp-p sinusoidal signals. Fig. 4.19 shows the result where the input tones were placed at 295 MHz and 302 MHz, respectively. The third-order intermodulation distortion (IMD) products were found to be at least 47 dB lower than the main tones, resulting in an extrapolated third order input intercept point (IIP_3) of -16 dBm.

To simulate the circuit at high frequency a small time step is required. To accomplish this, the HSPICE options [48] listed in Table 4.3 are crucial for accurate output data acquisition. In addition, it was found that the time-step specified in the transient analysis statement has to be a short integer, e.g. 2 μsec, instead of a real number with many digits, e.g. 2.033 μsec.

HSPICE OPTIONS	LVLTIM	DVDT	RELVAR	ABSVAR	Ft	Fs
values	2	2	0.2	0.2	0.2	0.2

Table 4.3: HSPICE options for accurate high frequency simulations

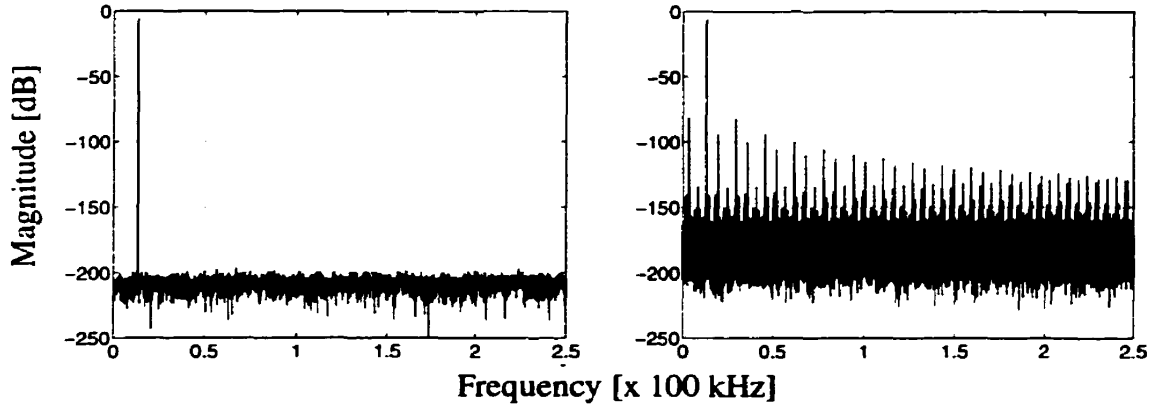


Figure 4.20: The effects of two different transient analysis request statements

Using the quoted numbers, simulations were carried out to capture a sinusoidal wave. Fig. 4.20(a) shows that a 'clean' *FFT* was produced using the following stimulus and transient statement,

Vs1 1 0 sin (0 1V 13.24462891e3 0 0 0)

.tran 2e-6 2e-2 0 1e-6

However, as shown in Fig. 4.20(b), excessive noise and distortion resulted when the above statements were replaced by,

Vs1 1 0 sin (0 1V 13.02963985e3 0 0 0)

.tran 2.033e-6 2e-2 0 1e-6

In both cases, the sinusoidal tones were placed on the same frequency bin, i.e. bin # 217, in their 8192 point *FFT*. This phenomenon was reproduced in a SPICE deck containing only an ideal sine wave generator connected to a resistor and the output data was recorded using maximum number of digits (HSPICE option: NUMDGT=8). To still meet the coherent sampling requirements with the above restriction, the input stimuli has to be specified to a high precision using many digits.

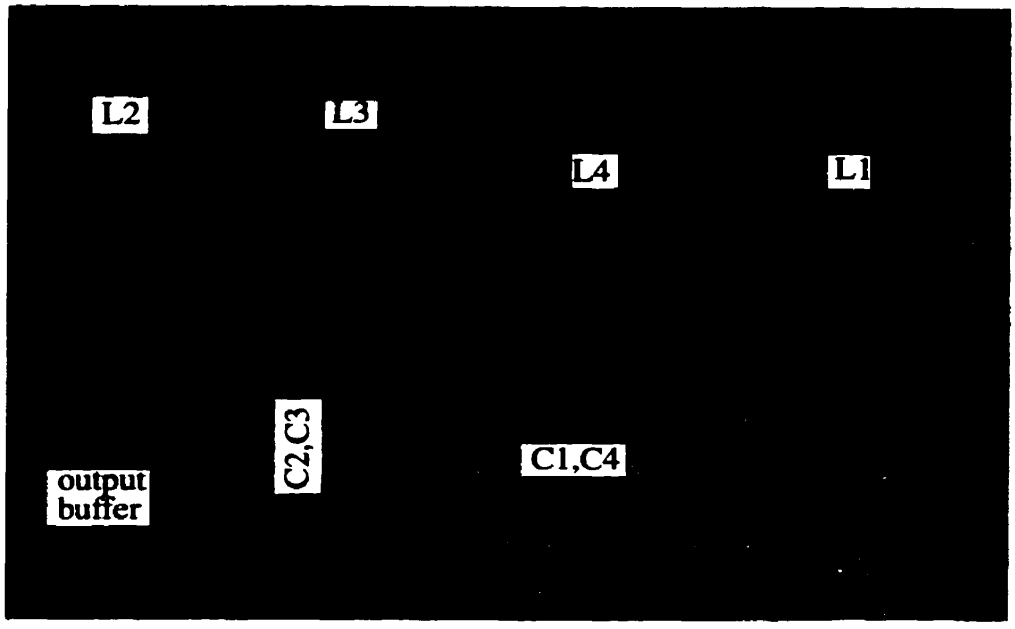


Figure 4.21: The BICMOS chip micrograph of the 6th-order BPF.

4.5.4 Layout of the Complete Design

Fig. 4.21 shows a micrograph of the chip where all four AIs are visible at the top of the chip. The capacitors and output buffer are seen in the remaining portion of the picture. The layout occupied a silicon area of less than 0.9 x 1.0 mm^2. Comparatively, the AI each occupied approximately 0.2 x 0.15 mm^2 as quoted in Section 4.4, leaving the majority of the silicon area for input and output AC coupling capacitors and the ladder's capacitors. These capacitors were all implemented with double-poly capacitor arrays using unit-sized elements.

Capacitor Layout Issues

Specific steps have to be taken in laying out capacitors to minimize the effects due to etching and process variation. Fig. 4.22(a) shows a layout of a 1 pF unit-sized capacitor. Its bottom plate is formed by the MOS gate polysilicon material while the top plate is an extra polysilicon layer. The connections to the top and bottom plates are made by metal 1 and metal 2, respectively. The capacitor arrays are placed on an Nwell platform biased by VCC to sink any stray charge or noise that will otherwise propagate into the signal path.

Etching imperfection will vary the perimeter of the capacitor and thus the capacitance. To minimize the etching effect, it is a common practice to maximize the area to perimeter (A/P) ratio and this can be achieved by using a square capacitor instead of a rectangular one. In addition, the edges of the top plate in Fig. 4.22(a) are trimmed to reduce the frindging electric field that will result in unpredictable capacitance variation. Based on these measures and requirements, a matlab program was written in [49] to calculate and fine tune the dimensions of a unit capacitor while maximizing the A/P ratio using the following equation:

$$C = C_{OA} \cdot Area + C_{OP} \cdot Perimeter, \tag{4.9}$$

where C is the total synthesized capacitance, C_{OA} is the capacitance per unit area, and C_{OP} is the capacitance per unit perimeter of the technology.

Fabrication inaccuracies introduce a gradient of oxide thickness that will cause capacitance mismatches. Fig. 4.22(b) illustrates a layout technique which will cancel the first order effects of the gradient by arranging the unit elements with a common centroid symmetry [50]. This figure presents the layout of two equal capacitors which are each formed by eight unit elements interlaced and connected in parallel. The symbol of the two capacitors is shown

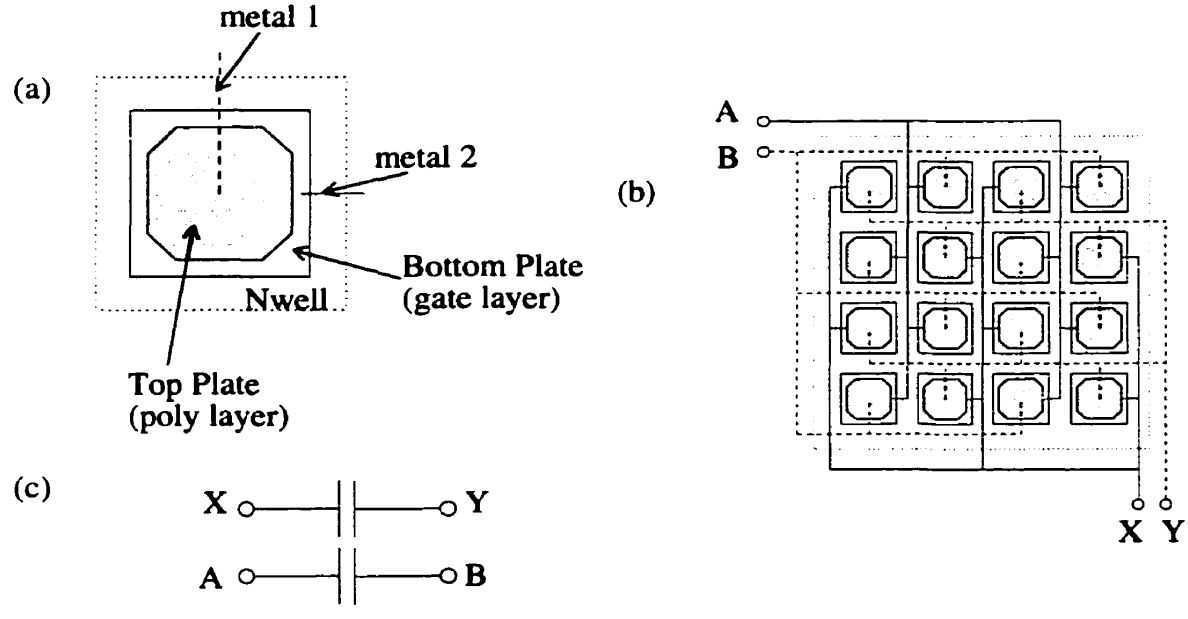


Figure 4.22: Capacitor layout.

in Fig. 4.22(c) where their terminals in (b) are identified. This layout technique was applied to match C2 to C3 and C1 to C4 in the LC ladder. Due to process variation, their absolute values will change but their ratios can be kept to within 0.5% by the above described layout technique. Thus, a shift in the signal band might occur after fabrication but, with the help of the tunable AIs, the filter shape would have been roughly preserved due to the constant ratios of the capacitors. However, the band center might also shift due to causes other than process variation, such as inaccuracies in the simulation models.

To preserve uniform boundary conditions, dummy capacitors were placed around the capacitor array as shown in the layout in Fig. 4.21.

4.5.5 Experimental Results

Fig. 4.23 captures the set-up of the equipments used in the experiment. A DC biasing board was built to provide power supply filtering and DC voltage tuning. This board was linked to a CMC supplied high-frequency four-layer board with soldered connections. The input and the output ports of the filter were interfaced with a network analyzer (HP 8753D) by

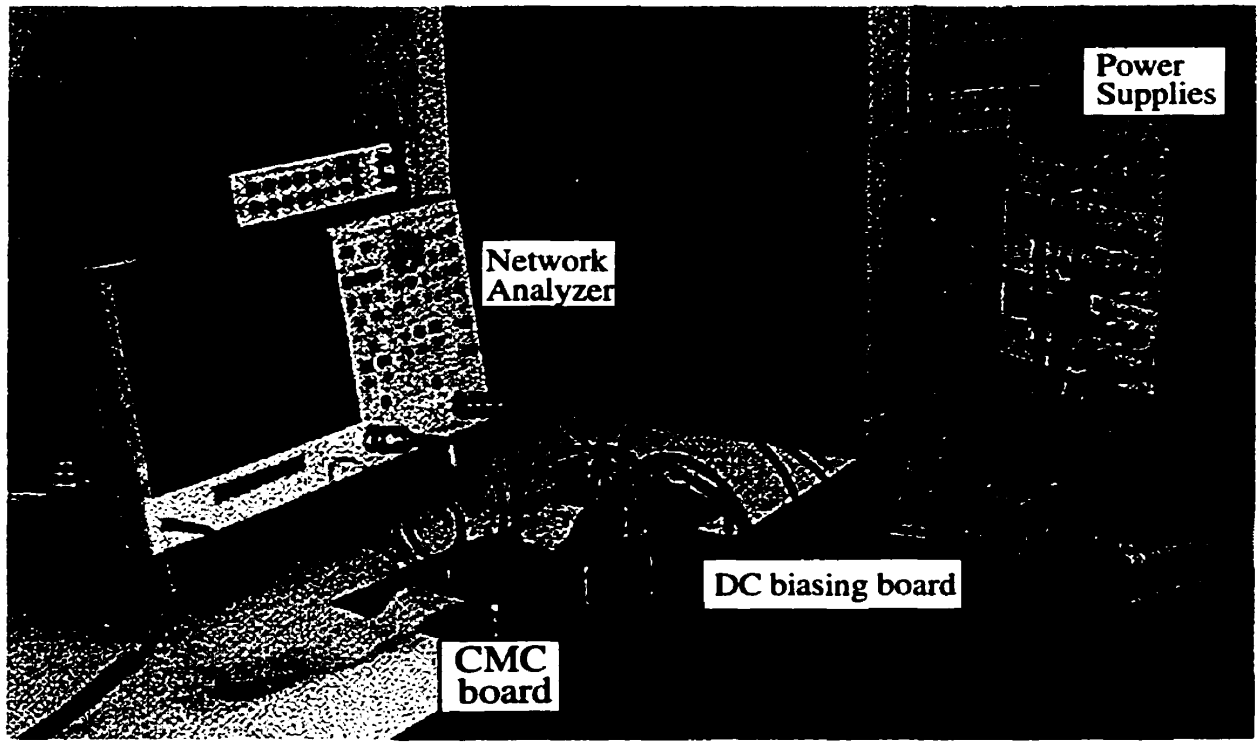


Figure 4.23: the experimental setup.

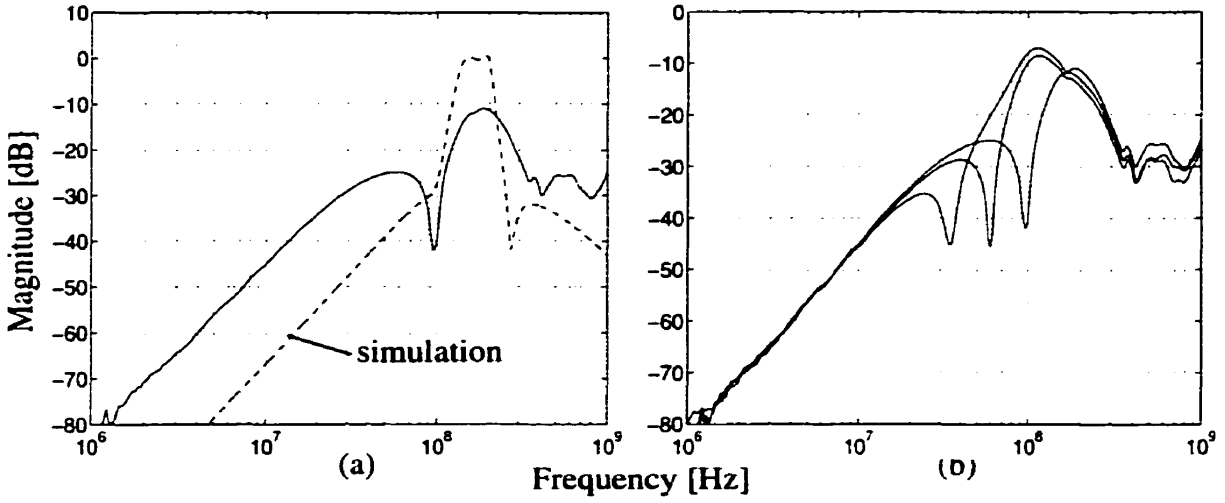


Figure 4.24: The experimental frequency response: (a) a comparison between the experimental and simulated behaviors, (b) the tuning of a transmission zero.

two SMA connectors. Both boards were placed on top of a common ground plane to reduce the effect of environmental noise on the circuit. The power supplies and tuning voltage supplies are shown on the right side of the picture. With this experimental set-up, the chip was then powered up to obtain the filter response.

Due to some problems associated with the on-chip test circuitry, the PDM input was unavailable as a stimulus to the filter. PDM signals can be generated off-chip but its clock frequency was limited to only 40 MHz in our lab.

Using a -34 dBm swept signal source from the network analyzer, Fig. 4.24(a) shows the measured frequency response. At frequencies below 30 MHz, a rising slope of 40 dB/decade is observed. This behavior at low frequencies is caused by two AC coupling capacitors at the input and the output of the filter. At frequency above 100 MHz, a transmission zero appears, with a notch depth of only -30 dB below the passband level. Moreover, the filter is centered at around 180 MHz with a 3 dB bandwidth of about 90 MHz. This is in contrast with the desired 300 MHz center frequency and 50 MHz bandwidth. This could be due to the effects of process variations on the ladder's capacitors and could not be significantly altered by tuning the AIs only. In order to draw an effective comparison, the simulated response was also tuned to 180 MHz. At frequencies higher than 400 MHz, several parasitic

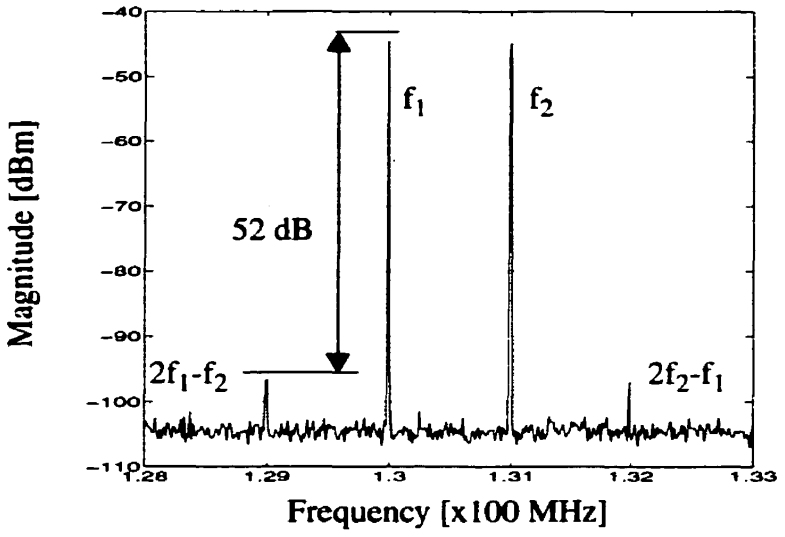


Figure 4.25: Measured results from a two-tone test.

poles introduced a non-tunable side lobe which limits the maximum out of band attenuation to about the -30 dB level. Fig. 4.24(b) illustrates an attempt to vary the frequency of a transmission zero from 35 MHz up to 100 MHz. This zero and its tunability clearly demonstrate the operation of the AI in the lower stopband LC-tank circuit. Movement of the upper stopband transmission zero was barely noticeable, as it seems to be masked by the parasitic poles above 400 MHz.

Fig. 4.25 is a power spectrum plot of a two tone test for a filter band ranging from 90 MHz - 160 MHz, when the in-band gain is set at its maximum. The two tones are placed at 130 MHz and 131 MHz, resulting in the IMD products to appear at 129 MHz [$2F_1$-F_2] and 132 MHz [$2F_2$-F_1]. Resolution bandwidth of the spectrum analyzer used for the measurement was 150 Hz (or equivalently sweep time = 111.21 sec). The input tones are at -34 dBm (6.3 mVp-p each) (3 dB loss of RF combiner included) and the output at -44 dBm (3.7 mVp-p each). With the IMD products at -96 dBm, an SFDR of 52 dB was achieved, resulting in an IIP_3 of -8 dBm. Compared to the simulation result in Fig. 4.18(b), the experimental measurement is better by a few decibels. This is most probably because of the higher on-chip $R_{s,\,eq}$ and thus the lower corresponding quality of the AIs, compared to the simulation. Higher $R_{s,\,eq}$ signifies a lower internal current gain in the AI and a gain decrease would potentially generate less distortion. This investigation provides an idea about the linearity of this technique. For BJTs, this finding is important because c_π, the parasitic capacitor in-

volved in this technique, is composed of two junction capacitance c_{je} and c_{de}, which are nonlinear and highly dependent on the value of V_{BE} and the DC biasing current [37].

Overall, noticeable discrepancy was observed between the simulated and the experimental frequency responses. Several reasons could be found to account for this discrepancy. The first two explanations provided are inherent problems to analog VLSI circuit design. The first reason being the inaccuracy of simulation models used, since only a level 3 model for the MOS and a Gummel-Poon model for the BJT were available. Also, even though appropriate layout steps had been performed, the effects of process variations could still be conspicuous as only the AIs were tunable and this tunability has a limited counter-influence on the change in capacitor values. Hence, with a different set of capacitances after fabrication, it might be impossible to preserve the filter shape and its center frequency. The third potential cause is closely related to the filtering technique involved. As we discovered during experimental measurements, the four degrees of tuning freedom did create difficulties in terms of tuning the shape of the filter. It could be a combination of these reasons that results in the observed discrepancy.

4.6 Conclusions

Due to the modularity of the active inductor approach, the implementation of an analog reconstruction filter has become relatively straightforward. The behaviors of this sixth-order LC filter, including distortion and insertion loss, were carefully characterized in simulation. During this characterization process, the post-processing of $\Sigma\Delta$ bitstream was shown feasible using transient analysis, thus illustrated the potential of this technique in performing the analog reconstruction task. Despite the use of transistors and parasitic capacitances, the linearity of this filter was found to be acceptable at high frequencies. Experimental measurements confirmed the basic operation of the active inductor design although further refinement of the tuning process is necessary to improve the overall filter response.

Chapter 5 : Conclusions

This chapter summarizes the features, efforts and contributions of this thesis in the area of bandpass digital-to-analog converters using oversampled sigma-delta modulation techniques. Specifically, a new structure has been proposed to efficiently implement the digital modulator and a novel floating inductor was created to be used in the analog reconstruction filter. As a result of the loose ends of this work, possible future directions will also be described.

5.1 Summary

The main objectives of this thesis are to improve signal conversion quality for a given bandwidth and to ensure stability in all bandpass D/A converters. Building on top of these objectives is the effort to migrate the design complexity of the converter to the digital side and to simplify the analog components as much as possible. This effort is necessary in mixed-signal testing applications so that the analog components used can be minimized and thus simplifying the self-testing process of the signal generator. To accomplish these goals, two components of bandpass ΣΔ digital-to-analog converters were designed and investigated at the IC level. Many practical implementation issues were examined with programmable and/or custom-layout ICs.

As a big part of this effort, a digital filter structure was developed in Chapter 3 to realize high-order modulators. These modulators allowed high resolution signal conversion with an OSR as low as 16. This bandwidth and signal resolution trade-off was easily adjusted by a specific set of coefficients in the structure. Using this structure, near-optimum noise suppression was achieved even after rounding all the coefficients to powers-of-two. In addition, high speed operation was attained independent of the modulator order. This speed performance is a few folds better compared to those of the integrator-cascade, resonator-

cascade or the LDI ladder structures. Design automation of the modulators for order 4 to 16 was incorporated into a CAD software called DSMOD. FPGA and fixed-point simulations were used to characterize the stability of various orders as well as their noise shaping mechanism. This work was published in [53] and [54] in 1997.

For post-processing of the ΣΔ output in order to recover the analog information, a high frequency filtering approach using active inductors was investigated. Using a component simulation approach, a floating active inductor was created to substitute spiral inductor in a passive LC ladder-based filter. The idea of using the parasitic capacitance of a BJT to perform signal processing was explored in the design of this floating inductor. The implementation of a sixth-order bandpass filter at high frequencies illustrated the modularity of the active inductor approach and demonstrated a proof of concept. Drawbacks such as distortion, high insertion loss were explained and quantified by simulations. Experimental measurements confirmed the basic operation of the active inductor design although further refinement of the tuning process is necessary to improve the overall filter response. This new inductor design was documented in [55].

5.2 Future Directions

Although the proposed digital structure has been shown capable of implementing stable high-order bandpass modulators for high speed digital-to-analog conversion, an effort to improve the NTF pole location control is certainly welcome since these locations are still sensitive to coefficient quantization. However, to make this improvement still attractive, it must be introduced without incurring more speed penalty to the existing structure. To further explore the modularity of this design, the same approach may be extended to yield lowpass modulators with similar features, i.e. they are insensitive to coefficient quantization and allow high speed operation independent of the modulator order. High speed operation is beneficial in lowpass applications as well since the trade-off between bandwidth and resolution of the modulator can be relaxed.

Even though the validity of the active inductor design has been confirmed experimentally, certain improvements in the design process are still needed to help justify its broad application in high frequency analog signal processing.

If the active inductor circuit is to be redesigned, in order to avoid more distortion in the signal path and to simplify tuning, the number of BJTs used in a single-ended AI should be limited to less than three if possible. As an improvement, these BJTs can be arranged in such a way that the DC biasing condition always forces them to operate in the active mode. The biasing scheme of the current design favors such mode of operation but is not able to guarantee this condition throughout the whole g_m tuning range.

To achieve independent frequency and Q tuning of the filter, independent resistance and inductance tunings need to be introduced to the new AI design. This can probably be done with a circuit that generates variable negative resistance (provides variable current gain) independent of inductance tuning.

By configuring the AI in a simple *RLC* bandpass resonator, this design can be first tested alone on chip to determine its characteristics and tunability. After ensuring the successful operation of an individual AI, a more sophisticated filter design can then be planned. However, this step-by-step design process may require a few fabrication runs and most probably a fast turn-around time, which is currently not possible in our lab.

Since they require twice as many transistors, the number of floating inductors should be minimized as their usage leads to a higher power consumption and a greater circuit complexity. Their use can be entirely avoided if a cascade-of-resonator topology [52] is used instead as this topology employs only grounded inductors and their values can be made the same (no spread). As a narrow-band approximation, this topology consists of grounded LC tanks connected in parallel by floating capacitors. Structures mapped from low pass prototype, such as the one used in this work, will most certainly require at least one floating inductor. However, when dealing with this topology, one should realize that it only works best in bandpass high-Q narrow-band applications.

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Appendix

```
------------------------------------------------------------
-- A Synopsys VHDL Code for
--  An 8th. Order Bandpass Delta-Sigma Modulator
------------------------------------------------------------
use work.bv_arithmetic.all;

entity bp8_dsm is

 generic( size : natural );
 port   ( clock, not_reset : bit;
          input : bit_vector(size-1 downto 0);
          output, ovf : out bit );
 -- pragma template
end bp8_dsm;

architecture struct of bp8_dsm is

 component reg
  generic( size : natural );
  port( clock, not_reset : bit;
        input : bit_vector(size-1 downto 0);
        output : out bit_vector(size-1 downto 0) );
 end component;

 component interbusUP
  generic( insize, outsize : natural );
  port   ( input : bit_vector(insize-1 downto 0);
           output : out bit_vector(outsize-1 downto 0) );
```

```
end component;

component interbusDOWN
  generic( insize, outsize : natural );
  port   ( input : bit_vector(insize-1 downto 0);
           output : out bit_vector(outsize-1 downto 0) );
end component;

component right_shift
  generic( size, shift : natural );
  port   ( input : bit_vector(size-1 downto 0);
           output : out bit_vector(size-1 downto 0) );
end component;

component mux2_1
  generic( size : natural );
  port   ( input0, input1 : bit_vector(size-1 downto 0);
         sel : bit;
         output : out bit_vector(size-1 downto 0) );
end component;

component ovf_adder
  generic( size : natural );
  port   ( in0, in1 : in  bit_vector(size-1 downto 0);
         output : out bit_vector(size-1 downto 0);
           ovf : out bit );
end component;

signal n3,n4,n6,n7,n9,n10:bit_vector(size-3-1 downto 0);
signal n5,n11,n12,n13,n14,n15,n16:bit_vector(size-1 downto 0);
signal n17,n18,n19,n20,n22,n23,n25,n26:bit_vector(size+2-1 downto 0);
signal n1,n2,n8,n24,n31,n33:bit_vector(size+3-1 downto 0);
signal n21,n27,n28,n29,n30,n32,n34:bit_vector(size+3-1 downto 0);
signal plus_one,minus_one,n35:bit_vector(2 downto 0);
```

```
begin

 plus_one(2 downto 0)  <= "001";

 minus_one(2 downto 0) <= "111";
 BUSi: interbusUP
        generic map( size, size+3)
        port map(input, n33);

 n1(size+3-1 downto size) <= n33(size+3-1 downto size) - n35;
 n1(size-1 downto 0) <= n33(size-1 downto 0);

 DEL1: reg
        generic map( size+3 )
        port map( clock, not_reset, n1, n2 );

 DEL2: reg
        generic map( size-3 )
        port map( clock, not_reset, n3, n4);

 RSH1: right_shift
        generic map( size, 9 )
        port map( n14, n5 );

 BUSa: interbusDOWN
        generic map( size, size-3)
        port map( n5, n6);

 n7 <= n6 - n4;

 RSH2: right_shift
        generic map( size+3, 6 )
        port map( n2, n8 );
```

```
BUSb: interbusDOWN
        generic map( size+3, size-3)
        port map(n8, n9);

n10 <= n7 + n9;

DEL3: reg
        generic map( size-3 )
        port map( clock, not_reset, n10, n3 );

BUSc: interbusUP
        generic map( size-3, size)
        port map(n3, n11);

n13 <= n11 - n12;

DEL4: reg
        generic map( size )
        port map( clock, not_reset, n13, n14 );

RSH3: right_shift
        generic map( size+3, 3 )
        port map( n2, n31 );

BUSh: interbusDOWN
        generic map( size+3, size)
        port map(n31 ,n15);

n16 <= n14 - n15;

DEL5: reg
        generic map( size )
        port map( clock, not_reset, n16, n12 );
```

```
BUSd: interbusUP
        generic map( size, size+2)
        port map(n12, n17);

n19 <= n17 - n18;

DEL6: reg
        generic map( size+2 )
        port map( clock, not_reset, n19, n20 );

RSH4: right_shift
        generic map( size+3, 6 )
        port map( n30, n21 );

BUSe: interbusDOWN
        generic map( size+3, size+2)
        port map(n21, n22);

n23 <= n20 + n22;

RSH5: right_shift
        generic map( size+3, 1 )
        port map( n2, n24 );

BUSf: interbusDOWN
        generic map( size+3, size+2)
        port map(n24, n25);
n26 <= n23 + n25;

DEL7: reg
        generic map( size+2 )
        port map( clock, not_reset, n26, n18);
```

```
BUSg: interbusUP
        generic map( size+2, size+3)
        port map(n18, n27);

OVF_CHK: ovf_adder
                generic map(size+3)
                port map(n27,n28,n29,ovf);

DEL8: reg
        generic map( size+3 )
        port map( clock, not_reset, n29, n30);

n32 <= n2 - n30;

DEL9: reg
       generic map( size+3 )
        port map( clock, not_reset, n32, n28 );
 n34 <= n33 - n28;

MUX1: mux2_1
        generic map( 3 )
        port map( plus_one, minus_one, n34(size+3-1), n35 );
 output <= n34(size+3-1);
end struct;
-------------------------------------------------
-- Component library starts here
-------------------------------------------------
--  An interface between different size buses
-------------------------------------------------

use work.bv_arithmetic.all;
-- input has a smaller bus size:
entity interbusUP is
 generic( insize, outsize : natural );
```

```
  port   ( input : bit_vector(insize-1 downto 0);
           output : out bit_vector(outsize-1 downto 0) );
  -- pragma template
end interbusUP;

architecture struct of interbusUP is
  signal sign_bit : bit_vector(0 downto 0);
begin

  sign_bit(0) <= input(insize-1);
  output(outsize-1 downto insize) <= sxt( sign_bit, outsize-insize );
  output(insize-1 downto 0) <= input(insize-1 downto 0);

end struct;

use work.bv_arithmetic.all;
-- output has a smaller bus size, use with cautions!:
entity interbusDOWN is
  generic( insize, outsize : natural );
  port   ( input : bit_vector(insize-1 downto 0);
           output : out bit_vector(outsize-1 downto 0) );
  -- pragma template
end interbusDOWN;

architecture struct of interbusDOWN is
  signal sign_bit : bit_vector(0 downto 0);
begin

  output <= input(outsize-1 downto 0);

end struct;

--------------------------------------------
-- Overflow Checking Adder
```

```
-----------------------------------------

use work.bv_arithmetic.all;

entity ovf_adder is
  generic( size : natural );
  port   ( in0, in1 : in bit_vector(size-1 downto 0);
           output : out bit_vector(size-1 downto 0);
           ovf : out bit );
  -- pragma template
end ovf_adder;

architecture struct of ovf_adder is

  signal y: bit_vector(size-1 downto 0);
  signal ow1, ow2: bit;
begin
  y <= (in0 + in1);
  output <= y;
  ow1 <= in0(size-1) and in1(size-1) and (not y(size-1));
  ow2 <= (not in0(size-1)) and (not in1(size-1)) and y(size-1);
  ovf <= ow1 or ow2;

end struct;
```