# The Design of Low-Voltage High Frequency CMOS Low Noise Amplifiers for Future Wireless Applications

*by*
*Tommy Tsang, B.Eng. 2000*

Department of Electrical & Computer Engineering
McGill University, Montreal, Canada.


March, 2002

---

A Thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Master of Engineering

# Abstract

Increasing demand for bandwidth, for both voice and data communications, has motivated the need for high speed electronics. Particularly, in the wireless domain, new standards are constantly evolving towards higher operating frequencies and higher level of integration, with strong emphasis on low voltage, low power, and low cost.

RFIC's are traditionally implemented in III - V compounded semiconductors or in bipolar technologies, due to their superior RF performances (e.g. low noise) when compared to CMOS technologies. As technology advances, modern sub-micron CMOS technologies, which used to be delicated for digital circuits operating at lower frequencies, are now becoming more performant and more suitable for radio frequency circuit designs. The challenges are not only to design RF transceivers in standard CMOS processes, but also to establish design methodologies and optimization techniques for their building blocks.

This thesis is concerned with one of the key building blocks, namely the Low Noise Amplifier (*LNA*). Several low-voltage LNA's were successfully implemented in a standard 0.18 μm CMOS technology, operating in the 5-9 GHz frequency band, targeted for future wireless applications. A new and very simple gain control mechanism is suggested for the first time, which does not affect the optimum noise and impedance matching. The 8-9 GHz prototypes are the highest LNA frequencies reported to-date in

CMOS. All prototypes exhibit gain tuning ranges of over 10 dB, and can operate from a supply voltage as low as 0.7 V.

Designing circuits at RF imposes many uncertainties and challenges, owing to the poor modeling of integrated passives and/or active devices. A design strategy for optimizing RF passive components (e.g. inductors, capacitors, and varactors) beyond 5 GHz is presented. Trade-offs between different design issues are discussed. The effectiveness of these techniques has been demonstrated through measurement results of several LNA's.

An attempt is made to explore the possibility of using Micro-Electro Mechanical Systems (*MEMS*) in the RF arena. Several successful tunable capacitor implementations, targeted to RF applications, are demonstrated through measurement results, and a detailed discussion of design equations is presented. Challenges and limitations of MEMS for future RF applications are addressed.

# Résumé

Dû à une demande accrue pour la bande passante des systèmes de la voix et des données, des circuits électroniques opérant à de grandes vitesses sont maintenant rendu nécessaire. Cet énoncé s'applique particulièrement au domaine du sans fil, les nouveaux standards ne cessent d'évoluer vers des fréquences de plus en plus élevées. Ces même circuits doivent dorénavant opérer à des fréquences élevées et être très intégrés, tout en consommant moins de puissance et ayant de faible coûts de production.

La technologie bipolaire ou composée III - V, dû à leurs performances supérieures pour les applications RF (ex. bruit, linéarité et gain) lorsque comparée à la technologie CMOS, est normalement utilisée dans la construction des circuits intégrés RF. Avec les récentes avancées technologiques, la technologie CMOS, principalement utilisée dans des circuits digitaux de fréquences plus basses, est maintenant convenable pour la conception des circuits de fréquence radio. En plus de concevoir de circuits RF robustes utilisant la technologie CMOS conventionnelle, les défis se portent aussi vers la méthodologie ainsi que les techniques d'optimization de ces même circuits.

Ce mémoire se penche sur une des composantes importantes de tel circuit: les amplificateurs à faible bruit (*AFB*). Différents AFB opérants à de bas potentiels ont été réalisés avec succès dans une technologie CMOS de 0.18 μm. Ces AFB opèrent dans une bande pour les futures applications sans fil: 5-9 GHz. Pour la première fois, un circuit

simple controllant le gain en affectant ni le bruit optimal ni l'impédance d'entrée du circuit est présenté. Les prototypes opérants dans la bande de 8-9 GHz sont les AFB les plus rapides à avoir été rapportés à ce jour. Opérant jusqu'à une tension de 0.7 V, tous les prototypes montrent un ajustement de gain de plus de 10 dB.

La conception de circuit RF est difficile dûe aux incertitudes liées à la modélisation incomplète des composantes actives et passives. Une stratégie de conception pour l'optimisation des composantes passives (ex. inductances, condensateurs et varators), opérant à plus de 5 GHz, est ici présentée. L'efficacité de ces techniques est démontrée à l'aide de mesures concluantes prises sur plusieurs AFB.

Une tentative a été faite pour explorer la possibilité d'utiliser des Micro-Electro Mechanical Systems (*MEMS*) dans le domaine du RF. Plusieurs condensateurs variables convenables aux applications RF sont présentés ainsi qu'une discussion détaillée des équations utilisées pour la conception. De plus, une discussion sur les défis et les limitations des MEMS pour de future application RF est faite.

# Acknowledgments

I would like to acknowledge many people, who have helped and supported me throughout the course of the research and writing of this thesis. In Him, I am grateful that I have grown up and learned so much. 'My heart trusts in Him, and I am helped.' - Psalm 28:7.

First and foremost, I would like to thank my supervisor, Prof. Mourad El-Gamal, for giving me the opportunity to pursue a master degree at the Microelectronics and Computer Systems (MACS) laboratory. His valuable guidance and insightful advises have been the key success of this work.

I would like to thank all the members of the MACS lab. for such a friendly and pleasant working environment. Special thanks goes to Ramez, Ahmed, Clarence, Nazmy, Geoffrey, Francis, Rola, Koon, Antonio and Tang, for actively participating in countless 'mind-stimulating' Q&A's. I am very thankful to my friends outside the lab. for their constant encouragement and enlightenment. Sincere thanks to Yan Yan, Lam Lam, Hoi Ying, Miranda, Ting, Pui Sang, Angie, and members of the Enoch fellowship. I would like to give my deepest thanks to Vanessa Lai who had sacrificed her time to take care of me during the period of my knee surgery.

I also wish to acknowledge the Canadian Microelectronics Corporation (CMC) for technology and equipment accesses, and MICRONET for partial funding of this work.

This thesis is delicated to my wonderful parents, Pak On and Lai Lin, for their never ending support and love. To them, I will always be grateful and proud.

# Table of Contents

# List of Figures

# List of Tables

# Chapter 1 - Introduction

Wireless technology came to existence when Guglielmo Marconi successfully demonstrated a radio signal transmission across the Atlantic Ocean in 1901. In later years, the invention of the transistor, the development of Shannon's information theory, and the concept of cellular systems - all developed by the bright minds at Bell Laboratories, had a big impact towards the evolution of modern mobile communications in the field of radio engineering.

Historically, radio frequency (*RF*) designs were thought to be incompatible with integrated circuit (*IC*) technology, because they rely heavily on tuned circuits and discrete filters, which are costly and bulky in nature. As a result, not much immediate development effort had been conducted in industry. As mobile telephony became popular in the 1990's, it was evident that there was a need to develop complex wireless transceivers to cope with the explosive growth in the number of mobile subscriber and base station infrastructure. Furthermore, the hardware had to be small in physical dimensions and to consume as little power as possible at minimal cost in order to remain competitive. These constraints revolutionized the research focus in radio architectures and analog circuit designs (e.g. [1] - [6]).

Nowadays, driven by an insatiable commercial demand for lower cost and higher bandwidth with enhanced digital functionality in RF transceivers, RF designs are moving towards high integration, low power, and low cost, while operating at higher frequencies (i.e. *in the GHz range*). A technology which can maintain a balance among all of these

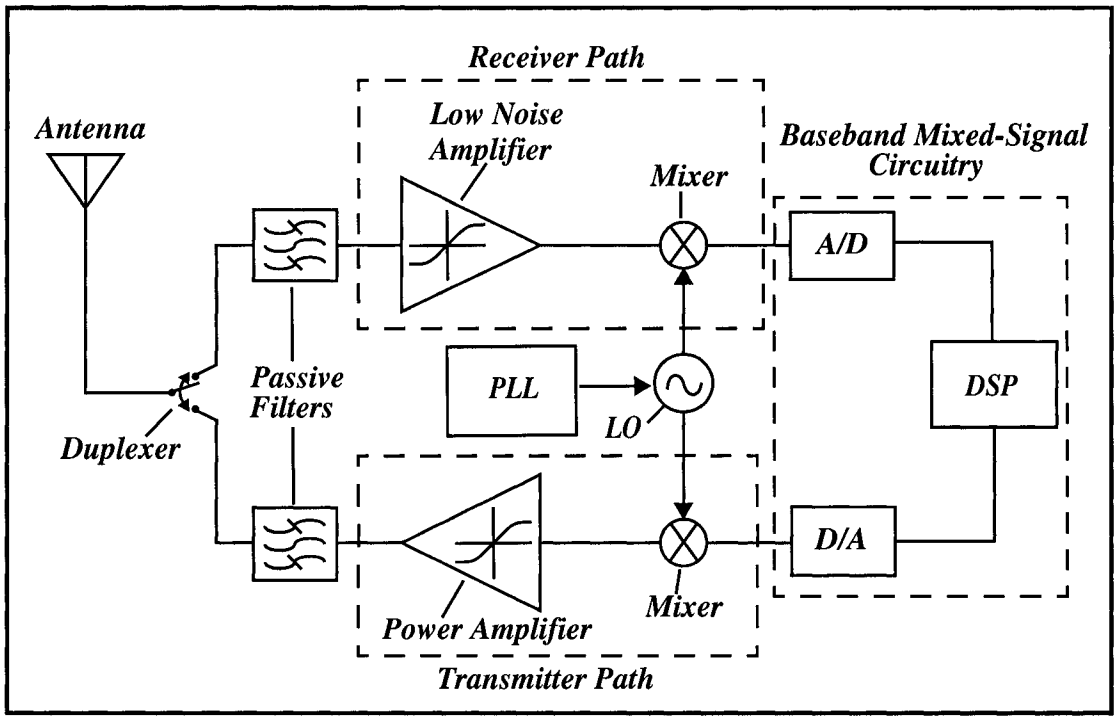


**Figure 1.1 The conceptual block diagram of a typical RF transceiver.**

factors will become the dominant technology choice for future wireless applications.

# 1.1 - Technology Choices in RF Designs

Portable RF communications devices are a fast growing market segment. Currently, the majority of RF transceivers are implemented as multi-chip modules (*MCM*), based on multiple technologies. A conceptual block diagram of a typical RF transceiver is shown in Fig. 1.1. Baseband and mixed-signal components (e.g. *D/A, A/D and DSP*) are predominantly implemented in Complementary Metal-Oxide Semiconductor (*CMOS*) technologies. The Low Noise Amplifier (*LNA*), mixer, and Power Amplifier (*PA*) are typically implemented in III - V compounded semiconductors, such as Gallium Arsenide (*GaAs*) and Indium Phosphide (*InP*). The Phase-Locked Loop (*PLL*) and Voltage-Controlled Oscillator (*VCO*) are usually implemented in Silicon (*Si*) and Silicon Germanium (*SiGe*) bipolar technologies. Passive filters and resonant tanks are realized as discrete passive components.

There are several limitations to this classical implementation, which include large size,

high weight and integration cost. Besides, interconnections between sub-systems introduce parasitics, which can deteriorate the overall RF performance of a transceiver. Due to the lack of a single technology which can support a commercially viable single-chip RF transceiver with adequate performance, the MCM approach remains the optimum one. As technology advances and matures, the level of integration of RF transceiver blocks is steadily rising, especially in the 1-6 GHz frequency range, where consumer-class wireless electronics dominate.

Substantial research efforts have been invested to explore the advantages and disadvantages of different competing technologies, mainly in terms of their noise, power efficiency, and linearity performances (e.g. [7], [8]). The RF performances and process issues in various existing technologies are summarized in Table 1.1.

It is evident that III - V compounds (e.g. *GaAs and InP*) dominate in all areas for wireless applications except for cost and integrability. Their intrinsic superior noise performance and higher speed over other technologies (e.g. *Si BJT and CMOS*) are mainly due to their improved electron mobilities (i.e. *use of majority carriers*) and saturated drift velocities. The use of low resistive metal gate structures, as opposed to polysilicon gates in CMOS, enhances their noise performance. Furthermore, the high resistivity nature of the substrate enables the realization of high quality monolithic

| Technology | GaAs PHEMT [9] | SiGe HBT [10] | Si BJT [10] | Si CMOS [11] | SOI CMOS [12] |
|---|---|---|---|---|---|
| $f_T$ (GHz) | 225 | 76 | 100 | 70 | > 100 |
| $f_{max}$ (GHz) | > 200 | 180 | 101 | 150 | 135 |
| NF | Good (100 GHz) | Fair (20 GHz) | Good | Fair (1 GHz) | Fair |
| Integration | Fair | Fair | Fair | Excellent | Good |
| Passives | Good | Fair | Fair | Poor | Excellent |
| Reliability | Good | Fair | Very good | Excellent | Good |
| Availability | Fair (expensive) | Fair (expensive) | Very good | Excellent | Very good |

**Table 1.1 - RF performances and process issues of various technologies.**

passive devices.

Among the III - V compounds, the High Electron Mobility Transistors (*HEMT's*) have the best overall performance. However, they are more useful in the microwave and millimeter wave frequency ranges, rather than in the 1-6 GHz which is targeted for low cost commercial telecommunication applications. The main reason is that in microwave and millimeter wave applications, device performance is the dominant factor rather than the production cost of each unit. The use of HEMT in these applications, mainly where high performance is required, such as for satellite transceivers, are not directly intended for the consumer market, but rather to niche market segments. In many cases, even a few tenths of a decibel improvement in noise figure is significant for specific wireless applications, especially in a base station or satellite receiver, because it translates directly into reductions in the transmit power requirements.

Despite the excellent RF performances of III - V compounds (e.g. *GaAs*), the incapability of integrating multiple functionalities on a single substrate (e.g. *RF and digital*) is one of the biggest drawbacks, especially when compared to other technologies with higher level of integration capability and with improved RF performances, such as Silicon-on-Insulator (*SOI*) CMOS and SiGe Heterojunction Bipolar Transistors (*HBT's*). Furthermore, higher processing costs, smaller wafer sizes, and moderate process reliability are additional shortcomings of III - V compounds, which prevent them from spreading to logic and mixed-signal circuitries.

Silicon BJT's are mainly used for implementing signal generation blocks (e.g *VCO's*) and mixing stages in a transceiver, due to their superior *1/f* noise performance. Performances of BJT's have been improved by the advent of SiGe HBT's, which emerge as a competitive candidate for wireless applications. Its performance is very comparable to III - V compounds, with inherent advantages in terms of low production cost, good manufacturing volumes, and good reliability of bulk silicon. Successful implementations of integrated RF building blocks, operating at the 5 GHz frequency band, in SiGe HBT's have been demonstrated [13], [14]. Despite its great promises in the RF arena, the lack of complementary devices in SiGe HBT's is one of its biggest limitations, making it difficult to integrate digital circuitries onto the same substrate.

Driven by increasing demand on digital functionalities at a reduced cost for wireless transceivers, CMOS and Bipolar-CMOS (*BiCMOS*) are becoming the popular choices of technologies for consumer electronics. BiCMOS technology has been viewed for a long time as a suitable compromise between RF and digital baseband circuitries, operating at 1-3 GHz [15], [16]. However, this comes at a higher technology cost, as well with a loss of performance in the digital components, since the minimum feature size of MOS transistors in a BiCMOS process is always larger than that of a delicated state-of-the-art CMOS process.

As the minimum feature size of CMOS devices decreases, the RF performances (e.g. $f_T$) continue to improve to the point where they become comparable to those of GaAs and SiGe processes. Deep sub-micron CMOS devices with $f_T$'s exceeding 100 GHz and minimum noise figures less that 0.5 dB at 2 GHz have been realized in [17]. Rapid technology advances, coupled with the overwhelming dominance of CMOS in the digital arena, is making Si CMOS the best candidate for a single-chip solution for modern RF transceivers. Although the RF performances of CMOS will probably never match those of GaAs or SiGe, its integration potential, combined with cost advantages and good process maturity, provide a strong driving force for its adoption over other technologies.

## 1.2 - Motivation

While the low cost and low power advantages of the CMOS technology are the dominant driving forces in the digital sector, the analog front-ends become the bottle necks in today's RF transceiver designs. Mainstream CMOS technologies are optimized for digital applications. The use of these CMOS technologies to implement high performance analog front-ends is highly desirable and beneficial, since higher integration with digital components results in significant space, cost, and power reductions. As a result, serious attention and research efforts, both from industry and from university research groups, have investigated the possibilities of single-chip CMOS RF transceiver solutions for future wireless applications [18] - [21].

Apart from the increasing acceptance of CMOS RFIC's in the wireless domain, there is always a need for efficient networks at high data rates. Motivated by the insatiable

demand for larger bandwidth, wireless standards are constantly evolving towards higher carrier frequencies, and at the same time driving the research focus of CMOS RFIC's into the GHz range [22], [24]. Over the last few years, wireless applications were developed for the 900 MHz and 1.8 GHz bands, followed by the current 2.4 GHz Bluetooth applications, then the 5-6 GHz bands for wireless LAN systems (e.g. IEEE 802.11a and HIPERLAN). Future technological advances and demand anticipate the use of CMOS technologies, operating at higher frequency bands (e.g. 5-10 GHz), for next-generation wireless communications applications.

The intense deployment of CMOS technologies for consumer wireless products has lead to the reduction in supply voltage standards for integrated circuits, mainly attributed to the continuous device scaling. This trend has motivated the evolution of low-voltage (e.g. < 1 V) RFIC design topologies [25], [26].

The Low Noise Amplifier (*LNA*) is a critical building block in communications systems. It is usually the first active circuitry in the signal path in a receiver, which is supposed to amplify the weak RF signals received, while introducing as little noise as possible. The performance of the LNA affects the overall performance of a receiver, such as its sensitivity.

The increased demand for single-chip CMOS RFIC's solutions, as well as technological advances in CMOS processes, have recently attracted substantial research focuses of CMOS LNA's. Although the CMOS technology is a promising cost effective choice, it represents several limitations and challenges in implementing monolithic CMOS LNA's. One dominant shortcoming is the inherently low quality factors of passive components, mainly the integrated inductors. The qualities of integrated inductors play an important role in the performance of an LNA. There are many factors that contribute to losses in integrated inductors and degradation in quality, which make them very hard to model, especially at GHz frequencies. Furthermore, the lack of general and systematic design guidelines for integrated inductors, and RF layout techniques in general, has increased the level of difficulties and uncertainties in designing CMOS LNA's. As a result, a typical successful CMOS LNA implementation usually requires a minimum of two design runs. The results from the first design cycle are used to fine tune

the design (e.g. center frequency) for the second run. This is highly inefficient and costly, especially in nowadays' competitive market with short turn-around time.

In this thesis, several successful implementations of high frequency low-voltage integrated CMOS LNA's are presented, demonstrating their performance and proving the feasibility of using standard CMOS technologies for the current, as well as for the future, low cost wireless telecommunication applications. Systematic design guidelines for optimizing integrated passive devices and RF layout techniques are also presented, in order to minimize design uncertainties in CMOS LNA's. The effectiveness of this design methodology has been supported by good measurement results of three successful LNA implementations.

## 1.3 - State-of-the-Art in LNA Designs

The Low Noise Amplifier (*LNA*) is an essential building block in a transceiver, which dictates the overall performance of the system. CMOS LNA design has become an interesting research topic, both in industry and in academia. In this section, some examples of LNA's, both commercially available and in academic research, are presented. Recently reported state-of-the-art CMOS LNA's in the literature are summarized and compared. The frequency range of the presented examples is limited to 1-12 GHz, since this is the frequency of interest for current and future portable and consumer products.

High performance LNA's are often implemented in various technologies other than CMOS, typically in III - V compounds. The main reason is their superior noise performance and high frequency behaviour when compared to CMOS technologies. As a result, almost all available commercial LNA's are implemented in technologies such as HEMT, MESFET, and HBT. Table 1.2 summarizes some existing high performance LNA's, both in industry [27], [28] and in academia [29], [30]. Note that all of the LNA designs exhibit excellent noise figures of less than 1.5 dB at a wide frequency range, especially when considering the commercial LNA's (e.g. [27], [28]), where all the package parasitics are taken into account. Typical reported noise figures are 1-2 dB lower

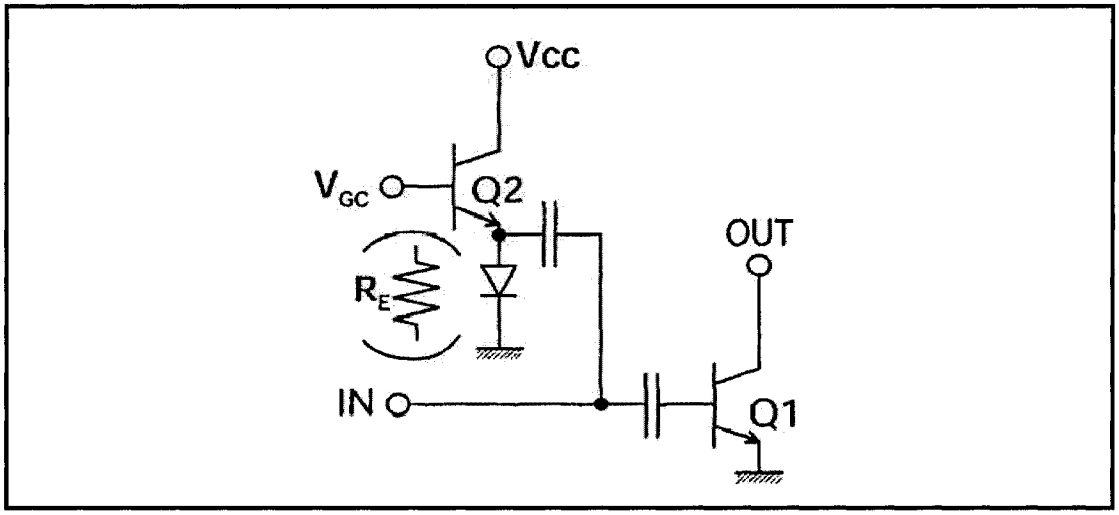


**Figure 1.2 Simplified schematic of the proposed gain controlled LNA [30].**

than the CMOS implementations, at similar frequencies.

One special feature of the proposed design in [30] is its gain controlability. Typical LNA's are designed for a fixed gain at a specific frequency with as low noise figure as possible. In this design, a wide gain control range (i.e -25 dB to 15 dB) was achieved without degrading the overall noise performance. This gain controlability is a desirable

| | [27] | [28] | [29] | [30] |
|---|---|---|---|---|
| **Technology** | **PHEMT** | **MESFET** | **PHEMT** | **HBT** |
| **Center Frequency, $f_o$** | **9-12 GHz** | **5.4-5.9 GHz** | **5.4 GHz** | **2 GHz** |
| **Power Gain, $S_{21}$** | **22 dB** | **12 dB** | **16 dB** | **15 dB** |
| **Noise Figure, NF** | **1.3 dB** | **1.0 dB** | **0.76 dB** | **1.4 dB** |
| **1-dB Compression Point (input), $P_{1\text{-}dB}$** | **-12 dBm** | **-17 dBm** | **-** | **-6.6 dBm** |
| **Voltage Supply, $V_{dd}$** | **3 V** | **15 V** | **3 V** | **3 V** |
| **Power Consumption** | **105 mW** | **900 mW** | **-** | **36 mW** |
| **Others** | **i) Fully integrated and packaged.** | **i) Fully integrated and packaged.** | **i) On-chip matching.** | **i) -40 dB gain control. ii) Off-chip matching.** |

**Table 1.2 - Examples of high performance LNA's.**

function in today's wireless applications since it can help enhancing the linearity of the system, especially the input third order intercept point ($IIP_3$), by decreasing the gain at a high input power level. The simplified schematic of the variable gain LNA is shown in Fig. 1.2. The basic idea behind this design is as follows: When the gain control voltage ($V_{GC}$) of transistor Q2 increases, the output impedance of the diode-loaded emitter follower decreases. The input RF signal is thus shorted to ground through this impedance, hence the overall gain of the LNA decreases.

One common drawback of all presented examples above is the need for a relatively high supply voltage (i.e. a minimum of 3 V) with high power consumption (36-900 mW), which goes against the current low-voltage and low-power trends. Furthermore, high production cost is another limiting factor. The unit cost of a typical high performance LNA (e.g. [27], [28]) is around $USD 1000 - 1500, whereas a CMOS implementation costs less than $USD 10. Such big cost difference has driven the industry to move towards CMOS RF implementations for consumer wireless products, while expensive high performance LNA's are only used for satellite applications at microwave

| | [31] | [32] | [33] | [34] |
|---|---|---|---|---|
| **Technology** | CMOS 0.6 μm | CMOS 0.25 μm | CMOS 0.25 μm | CMOS 0.25 μm |
| **Center Frequency, $f_o$** | 1.5 GHz | 5.2 GHz | 1.2 GHz | 7 GHz |
| **Power Gain, $S_{21}$** | 22 dB | 16 dB | 20 dB | 6.2 dB |
| **Noise Figure, NF** | 3.5 dB | 2.5 dB | 0.8 dB | 3.3 dB |
| **1-dB Compression Point (input), $P_{1\text{-dB}}$** | -19.3 dBm | -11.7 dBm | -24 dBm | -1.6 dBm |
| **Voltage Supply, $V_{dd}$** | 1.5 V | 3 V | 1.5 V | 2 V |
| **Power Consumption** | 30 mW | 48 mW | 9 mW | 13.8 mW |
| **Others** | i) Off-chip matching. | i) On-chip matching. ii) Thick top metal. | i) Bondwire matching. ii) ESD protection. | i) On-chip matching. ii) Special layout techniques. |

**Table 1.3 - State-of-the-Art CMOS LNA's in the literature.**

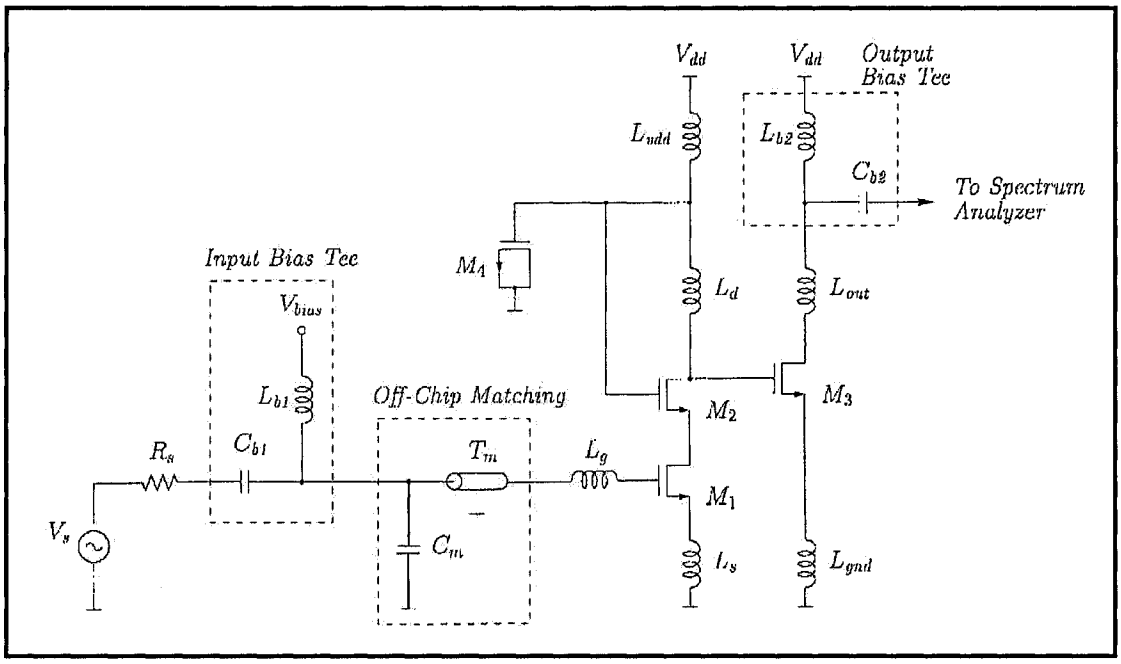


**Figure 1.3 Complete schematic of the LNA in [31], including off-chip elements.**

frequencies, where a stringent noise performance is required.

As the main focus of this thesis is on CMOS Low Noise Amplifiers, a summary of state-of-the-art CMOS LNA's in the literature is provided in Table 1.3. The work presented in [31] is considered to be a classic. It was the first successful implementation with detailed analysis of CMOS LNA's operating at GHz range. The proposed design was based on a conventional cascode topology with source inductive degeneration, as shown in Fig. 1.3. Off-chip high quality passive components were used for impedance matching. It was also shown that this architecture offers the possibility of achieving the best noise performance over any other architecture. The contribution of that work was significant, as most of the later CMOS LNA implementations (e.g. [22], [32] - [34], [47]) were based on this structure. In [32], the design targeted the 5 GHz band utilizing a conventional cascode structure with on-chip impedance matching. A thick top metal layer was available for high quality on-chip inductors, hence an overall low noise figure was achieved. A relatively large power consumption with the use of high supply voltage was the main drawback of that work. In [33], an excellent noise figure of less than 1 dB was achieved at low GHz frequency (i.e. 1.2 GHz), with the additive feature of ESD protection. Bonding wires were used for impedance matching. Finally, in an attempt to

push the frequency limit, a CMOS LNA operating at 7 GHz has recently been demonstrated [34]. Special layout techniques of transistors were employed in the design to enhance the RF performance. Unfortunately, the low power gain of 6.9 dB has put the effectiveness of these layout techniques in question.

The main focus of this thesis is to use a standard commercial CMOS technology to implement low-voltage fully integrated LNA's, operating in the 5-10 GHz frequency range, for next-generation wireless applications. Systematic performance enhancement techniques are also presented.

## 1.4 - Thesis Outline

The thesis began with an overview on the current technology choices in RF applications, with a focus on LNA designs. Application examples and performance summaries of state-of-the-art LNA designs were presented. The challenges and the need for integrated CMOS LNA's operating in the 5-10 GHz frequency band, with a strong emphasis on low-voltage design topologies, were motivated.

In Chapter 2, basic theory and important parameters such as noise and distortion in RF designs are reviewed. Design equations and constraints on CMOS LNA's are then discussed in details. Different LNA topologies, which are suitable for low-voltage sub-1 V applications, are presented. Trade-offs, in terms of gain, linearity, and noise performances, in each architecture are addressed. Finally, a modified architecture, based on a well-known folded cascode topology, is proposed to be the choice in today's low-voltage designs with good performances in all aspects, when compared to other architectures. Gain tunability is suggested for the first time for this architecture.

In Chapter 3, a systematic design strategy for optimizing RF passive elements (e.g. inductors and capacitors) beyond 5 GHz is presented. Trade-offs between different design issues are addressed. In inductor designs, the conductor width ($W$), the number of turns ($N$), the conductor spacing ($S$), and the number of conductor layers ($L$), are the key design parameters. An approach to optimize the quality factors of the inductors at 5-10 GHz, while extending their self-resonant frequencies ($f_{RES}$), is addressed. For capacitor and varactor designs, the tuning ranges and the methods to reduce parasitic resistances are the

key design issues which needed to be optimized.

Apart from a discussion of the mainstream RF passive devices, an attempt is made to explore the possibility of using Micro-Electro Mechanical Systems (*MEMS*) in the RF arena. Several successful tunable capacitor implementations, which are suitable for current RF applications, are demonstrated by measurement results, along with a detailed discussion of design equations. Challenges and limitations of MEMS for future RF applications are addressed.

In Chapter 4, three successful CMOS LNA implementations are demonstrated and verified by measurement results. Guidelines for RF layout techniques towards successful LNA implementations are presented. The first LNA is operating at the 5-6 GHz frequency range with gain and frequency tunability, targeted for applications of wireless LAN in the US (IEEE 802.11a standard for the FCC unlicensed national information infrastructure, the U-NII band), and the European High Performance Radio LAN (HIPERLAN). In an attempt to push the frequency limit in CMOS RF technologies, the second and third LNA's are designed to operate at a much higher carrier frequency of 8 GHz and 9 GHz. Different inductor structures are used in these two designs. Both LNA's have the advantage of tunability in gain over any other popular LNA implementation (e.g. conventional cascode amplifier structures). All three LNA implementations are designed with a low supply voltage of 1 V and are still functional at a much lower supply voltage of 0.7 V. Finally, a summary of all three implementations, together with a comparison to other designs from the literature, is presented.

In Chapter 5, the thesis concludes with a summary of the work done and with the results obtained, ending up with suggestions for future work.

## 1.5 - Thesis Contributions

The following is a summary of the contributions of this thesis:

1. Provided a summary of some existing topologies which are suitable for low-voltage sub-1 V LNA applications. Demonstrated the validility of these topologies to operate beyond 5 GHz, by implementing several chips both in modern bipolar and CMOS technologies. More specifically, the following work was the result of this thesis:

    a) A successful chip implementation of a fully integrated 5.8 GHz bipolar LNA using the LC-coupled topology. It was the *first to demonstrate* a 5.8 GHz LNA running from a 1 V supply with a low power consumption of 6.6 mW in a 0.5 μm bipolar technology. This was published as [35]:

    1- **T. K. K. Tsang and M. N. El-Gamal, "A Fully Integrated 1 V 5.8 GHz Bipolar LNA", *2001 IEEE International Symposium on Circuits and Systems (ISCAS 01)*, vol. 2, pp. 843-845, May 2001.**

    b) A chip implementation of an integrated 1 V conventional cascode LNA in a 0.18 μm CMOS technology. Due to some fatal layout errors, a resonant frequency of 7.6 GHz was measured, which was different from the designed value of 5.8 GHz. Nonetheless, the measurements have shown the usability of the cascode topology with a 1 V power supply, operating beyond the 5 GHz band.

    c) Based on the well-known folded cascode topology with some modifications, three successful chip designs were fabricated in a 0.18 μm CMOS technology. *Gain tunability of this modified structure was suggested for the first time.* The first prototype was targeted at the 5.8 GHz band, while the other two prototypes were the *first successful demonstrations* for sub-micron CMOS LNA's operating at 8-9 GHz to be reported in the literature. The results were published in [36], [37]:

2- **T. K. K. Tsang and M. N. El-Gamal, "Gain and Frequency Controllable Sub-1 V 5.8 GHz CMOS LNA", *2002 IEEE International Symposium on Circuits and Systems (ISCAS 02)*, accepted May 2002.**

3- **T. K. K. Tsang and M. N. El-Gamal, "Gain Controllable Very Low Voltage (< 1 V) 8-9 GHz Integrated CMOS LNA", *2002 Radio Frequency Integrated Circuits (RFIC) Symposium*, accepted June 2002.**

2. Provided a design methodology, which is strongly supported by excellent measurement results, on designing CMOS LNA's beyond 5 GHz. Detailed design guidelines for optimizing RF passive devices, and essential layout techniques to enhance the LNA performance are presented. This provides a valuable input for CMOS RF designers to avoid the "trials-and-errors" design approach.

3. An attempt to implement RF passive devices in MEMS, particularly in a low cost and commercially available Multi-User MEMS Process (MUMPs). Several variable capacitor structures were implemented, with one newly proposed structure which has an infinite tuning range in theory. Preliminary measurement results have shown that the devices are suitable for up to 4 GHz RF applications.

# Chapter 2 - CMOS LNA Basics and Circuit Topologies

The first active circuitry of a receiver is usually a Low Noise Amplifier (*LNA*), whose main function is to provide adequate gain to suppress the additive noise of subsequent stages (e.g. mixer and image rejection filter). The noise characteristics of the LNA limits the sensitivity of the entire receiver. Apart from providing enough gain while adding as little noise as possible, an LNA with low distortion is highly desirable.

In this chapter, some basic parameters such as noise and distortion in RF circuits are addressed. This is then followed by a detailed derivation of design equations and constraints on CMOS LNA's. Different LNA topologies, which are suitable for low-voltage (i.e. < 1 V) applications, are presented and their advantages and limitations are discussed. Finally, this chapter concludes with the presentation of a detailed design methodology for the chosen low-voltage LNA topology.

## 2.1 - Noise

### 2.1.1 - Thermal Noise

Thermal noise is caused by the thermal agitation of charge carriers in a conductor, which results in a random fluctuation in current and gives rise to a random voltage in a load. The available noise power ($P_{NA}$) is given by:

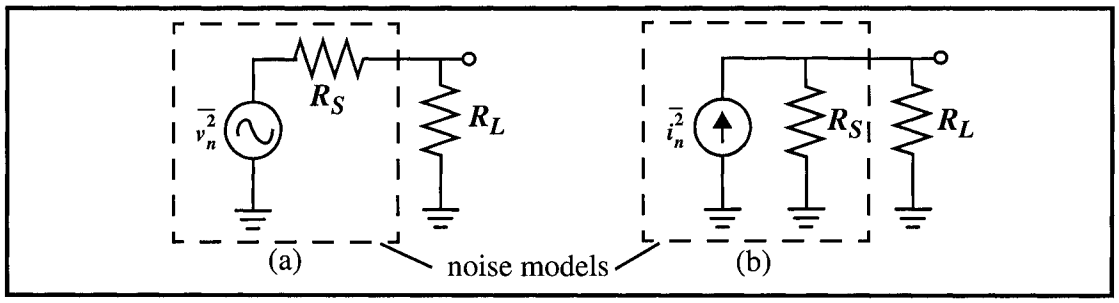


**Figure 2.1 (a) Noise voltage model and (b) noise current model for computing the thermal noise of a resistor.**

$$P_{NA} = kT\Delta f, \tag{2.1}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzman's constant, $T$ is the absolute temperature, and $\Delta f$ is the noise bandwidth. For a noise bandwidth of 1 Hz at room temperature (i.e. 298 °K), the available noise power is about -174 dBm, which is often referred to the 'noise floor' of the system.

The available thermal noise power of a resistor is defined as the power delivered by a noisy source resistor ($R_S$) to a noiseless and matched load resistor ($R_L$). The noisy resistor can be modeled in two ways [38]: i) A noisy voltage source in series with a noiseless resistor, or ii) a noisy current source in parallel with a noiseless resistor. Both resistor thermal noise models, which are used to compute the thermal noise power, are shown in Fig. 2.1.

From the noise voltage model shown in Fig. 2.1(a), the power delivered by the source resistor to a load resistor of equal value (i.e. $R_S = R_L = R$) is by definition the available noise power:

$$P_{NA} = kT\Delta f = \overline{v_n^2} \cdot \frac{R_L}{(R_S + R_L)^2} = \frac{\overline{v_n^2}}{4R}, \tag{2.2}$$

and

$$\overline{v_n^2} = 4kTR\Delta f, \tag{2.3}$$

where $\overline{v_n^2}$ is the root-mean-square (*rms*) noise voltage generated by the resistor R over a

bandwidth of $\Delta f$ at a given temperature.

Similarly, the rms noise current can be derived from the noise current model shown in Fig. 2.1(b), and is equal to:

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} = 4kTG\Delta f. \tag{2.4}$$

From the above equations, it can be seen that an approach to reduce the thermal noise of a given resistance is either to keep the temperature as low as possible or to limit the noise bandwidth to the minimum useful value.

### 2.1.2 - Shot Noise

Shot noise occurs due to the direct flow of current in diodes and transistors. It is due to the random drifting of charge carriers across the PN-junction, which results in current fluctuation (i.e. shot noise) around the average current value. The shot noise current is expressed as:

$$\overline{i_{sn}^2} = 2qI_D\Delta f, \tag{2.5}$$

where $\overline{i_{sn}^2}$ is the rms noise current, $q = 1.602 \times 10^{-19}$ C is the electron charge, $I_D$ is the average DC current, and $\Delta f$ is the noise bandwidth.

From equation 2.5, the additive shot noise can be reduced by minimizing the bias current of an active device.

### 2.1.3 - Flicker Noise (1/f Noise)

Flicker noise is due to random trapping of charge carriers associated with contaminations and defects in crystal lattices, which gives rise to a noise power dominated at low frequencies.

Similar to shot noise, flicker noise $\overline{i_{fn}^2}$ occurs in the presence of direct current flow, and is given by:

$$\overline{i_{fn}^2} = K\frac{I^a}{f^b}\Delta f, \tag{2.6}$$

where $K$ is a device-specific empirical parameter, $I$ is the average DC current, $\Delta f$ is again the noise bandwidth, $a$ is a constant ranging from 0.5 to 2, and $b$ is another constant of about unity.

In LNA applications, RF signals are amplified in a narrowband fashion with a typical bandwidth of few hundreds of MHz around the center frequency. Hence, flicker noise does not play an important role in LNA applications, because it only dominates at low frequencies. However, it becomes an important noise source when considering a complete transceiver where frequency translation is performed. On the receiver side, excessive flicker noise will corrupt the downconverted RF signals at baseband. On the transmitter side, flicker noise can be upconverted to the RF band where it interferes with the desired RF signals. Nonetheless, flicker noise is a bigger concern in oscillator designs, for example, compared to the main focus of this work.

### 2.1.4 - Noise Sources in MOSFET's

There are two dominant noise sources in MOS transistors at RF: Namely, the intrinsic channel thermal noise, and the geometry related gate resistance noise.

**(a) Channel thermal noise** - The inversion layer joining the source and drain regions is modulated by the gate-source voltage and is resistive in nature, hence it exhibits thermal noise. It can be shown that this noise source can be modeled by an rms noise current source:

$$\overline{i_{ch}^2} = 4kT\gamma g_{d0}\Delta f, \tag{2.7}$$

where $g_{d0}$ is the zero-bias drain conductance of the transistor, and $\gamma$ is a bias and layout dependent parameter, found to be in the range of $\frac{2}{3} < \gamma < 1$ for long channel devices. For short channel devices, measurements have shown that $\gamma$ can be as high as two to three, depending on the bias conditions [39]. This excess noise may be attributed to the presence of hot electrons in the channel, where the high electric fields in sub-micron

MOS devices cause the electron temperature to exceed the lattice temperature.

**(b) Gate resistance noise** - The additive thermal noise to the gate due to the distributed gate resistance. It can be modeled by an rms noise voltage source in series with a resistance at the gate. The amount of additive gate resistance noise is layout-dependent. By interdigitating the device, the contribution of this noise source can be significantly reduced. The distributed gate resistance is given by [40]:

$$R_g = \frac{R_{sh}W}{3n^2L}, \tag{2.8}$$

where $R_{sh}$ is the sheet resistance of the polysilicon, $W$ is the total gate width of the device, $L$ is the gate length, and $n$ is the number of gate fingers used. The factor 1/3 arises from the distributed analysis of the gate resistance and is assumed that only one side of each gate finger is connected together. By connecting both ends, this factor reduces to 1/12. Nonetheless, by doing a careful layout with multiple fingers, $R_g$ can be minimized and rendered insignificant.

### 2.1.5 - Noise Figure

A useful measure of the noise performance of a system is the noise factor ($F$), which is defined as the degradation of the signal-to-noise ratio ($SNR$) due to the device under test ($DUT$) and is given by:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}}, \tag{2.9}$$

where $S_{in}$ and $N_{in}$ are the signal and noise power at the input of the $DUT$, respectively, while $S_{out}$ and $N_{out}$ are the output signal and noise power, respectively.

Consider a $DUT$ having a power gain $G_p$, the input-output relationship can be expressed as (Fig. 2.2):

$$S_{out} = G_p \cdot S_{in}, \tag{2.10}$$

and

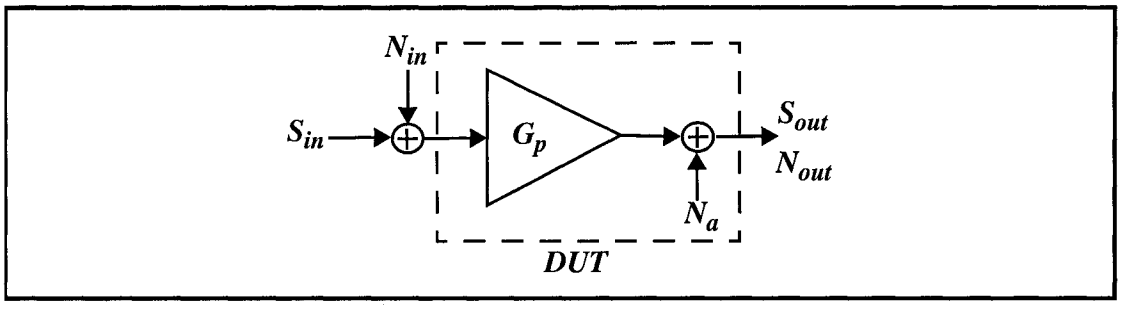


**Figure 2.2 Noise equivalent block diagram of a system.**

$$N_{out} = G_p \cdot N_{in} + N_a, \tag{2.11}$$

where $N_a$ is the induced available noise power of the *DUT* to the subsequent stage. Equation 2.9 can then be rewritten as:

$$F = \frac{S_{in}/N_{in}}{(G_p \cdot S_{in})/(G_p \cdot N_{in} + N_a)} = \frac{G_p N_{in} + N_a}{G_p N_{in}} = 1 + \frac{N_a}{G_p N_{in}}. \tag{2.12}$$

Thus, the noise factor can be viewed as the ratio of the total output noise to the part of the output noise which is due to the input source:

$$F = \frac{total\ output\ noise}{output\ noise\ due\ to\ input\ source}, \tag{2.13}$$

or alternatively,

$$F = 1 + \frac{output\ noise\ due\ to\ injected\ noise}{output\ noise\ due\ to\ input\ source}. \tag{2.14}$$

In RF designs, it is common to express the noise performance in terms of the noise figure (*NF*), which is merely the noise factor *F* expressed in dB:

$$NF = 10\log_{10} F = SNR_{in}(dB) - SNR_{out}(dB). \tag{2.15}$$

In an ideal case, where the system is noiseless, this results in $F = 1$ and $NF = 0$ dB, which never occurs in real life.

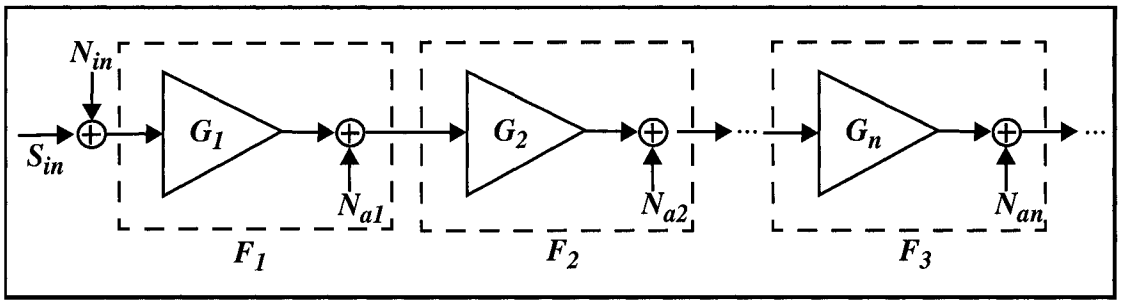


**Figure 2.3 Cascaded noisy stages.**

## 2.1.6 - Noise Temperature

In addition to the noise figure, another figure of merit used to determine the noise performance of a system is the noise temperature. The noise temperature ($T_N$) is defined as the increase in the required temperature of the source resistance for it to account for all of the output noise at the reference temperature $T_{ref}$ (i.e. 290 K). It is related to the noise factor as follows:

$$F = 1 + \frac{T_N}{T_{ref}} \Rightarrow T_N = T_{ref} \cdot (F - 1). \tag{2.16}$$

The noise temperature is particularly useful for systems with a noise factor quite close to unity, since it offers a higher resolution on noise performance compared to the noise figure metric.

## 2.1.7 - Cascade of Noise Figures

Considering a cascade of $n$ matched noisy stages with power gains $G_k$ and noise factors $F_k$ as shown in Fig. 2.3, the equivalent total injected noise contribution of $k$ stages relative to the input of the system can be expressed as:

$$F = \frac{N_{in} + \sum_{k=1}^{n} N_{ai,k}}{N_{in}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_n}. \tag{2.17}$$

The above equation is called the Friis equation [41]. It expresses the overall noise

figure in terms of the noise figure of each stage. It also indicates that the noise contributed by each stage decreases as the gain of the preceding stage increases, implying that the first stage in a cascade system is critical. In fact, the first stage, usually a low noise amplifier, has the most pronounced effect on the noise performance. Hence, it is highly desirable to have a low noise figure and a high gain in an LNA in order to minimize the overall noise figure of the system.

## 2.2 - Distortion

### 2.2.1 - Non-linearity

The behaviour of many analog and RF circuits can be approximated by a linear model represented in the form of a small signal response. As the input signal power increases to a level beyond the small signal approximation, non-linear effects become prominent. In circuits, these non-linearities are mainly due to the characteristics of the transistors.

To account for the non-linear effects, consider a practical system with a transfer function:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots, \tag{2.18}$$

where $\alpha_1$ is the linear gain factor of the system and $\alpha_n > 1$, for $n > 1$, are the non-linear gain factors.

By applying a sinusoid at input $x(t) = G\cos\omega t$ to a non-linear system, the output generally exhibits frequency components that are integer multiples of the input frequency and is given by [42]:

$$y(t) = \alpha_1 G\cos\omega t + \alpha_2 G^2 \cos^2 \omega t + \alpha_3 G^3 \cos^3 \omega t + \ldots \tag{2.19}$$

$$= \alpha_1 G\cos\omega t + \frac{\alpha_2 G^2}{2}(1 + \cos 2\omega t) + \frac{\alpha_3 G^3}{4}(3\cos\omega t + \cos 3\omega t) + \ldots \tag{2.20}$$

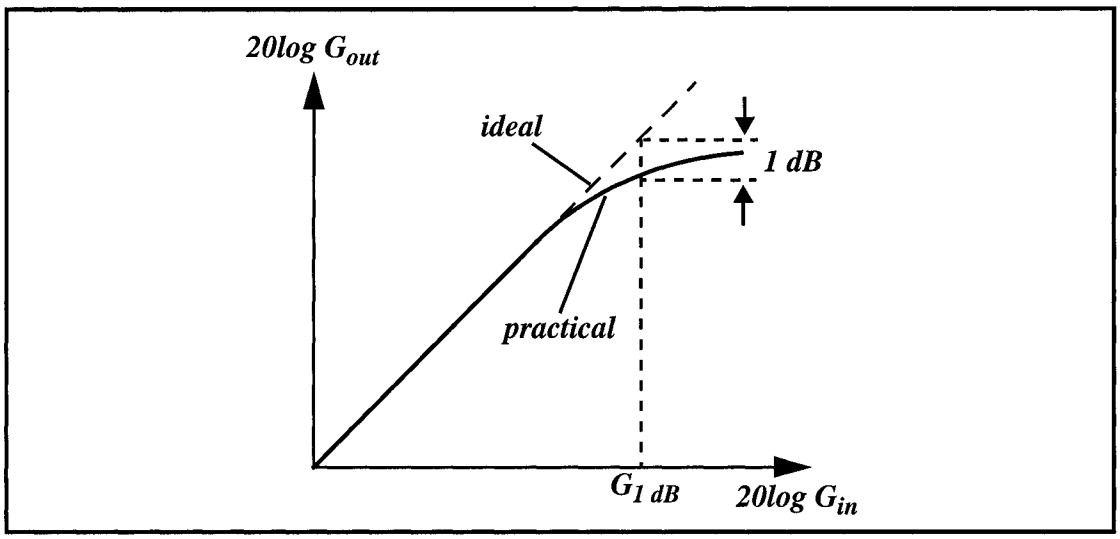


**Figure 2.4 Graphical explanation of 1 dB compression point.**

$$= \frac{\alpha_2 G^2}{2} + \left(\alpha_1 G + \frac{3\alpha_3 G^3}{4}\right)\cos\omega t + \frac{\alpha_2 G^2}{2}\cos 2\omega t + \frac{\alpha_3 G^3}{4}\cos 3\omega t + \ldots . \quad (2.21)$$

It can be easily seen from equation 2.21 that the $n$ th harmonic is approximately proportional to $G^n$, and that the even-order harmonics resulting from $\alpha_j$, for even $j$, will vanish for systems with symmetry (i.e. fully differential). In reality, finite accuracy in matching will corrupt the symmetry, hence yielding weak even order harmonics.

## 2.2.2 - Gain Compression

The small signal gain of a circuit is usually obtained with the assumption that the harmonics are negligible. In other words, from equation 2.21, it is assumed that $\alpha_1 G$ is much larger than all other terms. However, as the input signal amplitude increases beyond the linear range, the output begins to saturate. This effect is often quantified by the 1 dB compression point, which is defined as the input signal power that causes the small signal gain to drop by 1 dB from its nominal value, as shown in Fig. 2.4.

The 1 dB compression point is calculated as the difference between the practical gain, $G_{practical} = \left(\alpha_1 G + \frac{3}{4}\alpha_3 G^3\right)$, and the ideal gain, $G_{ideal} = \alpha_1$, being 1 dB and is expressed as:

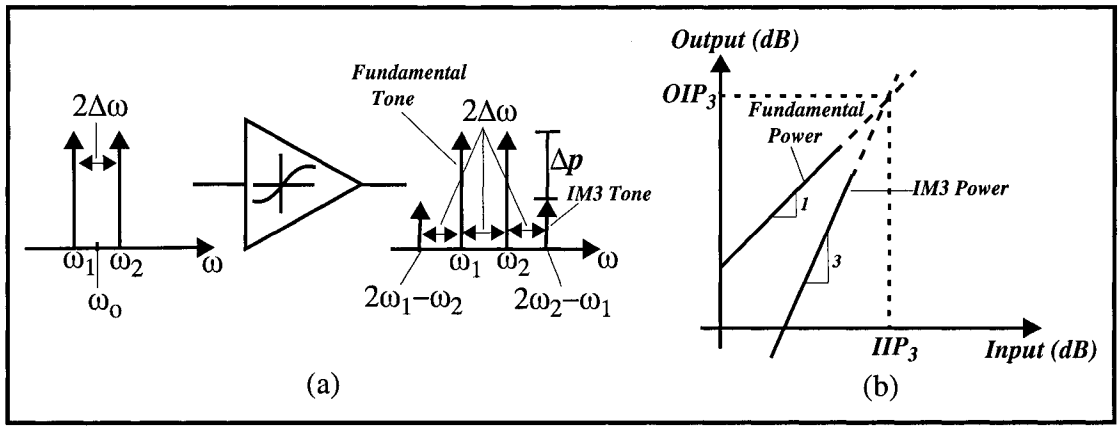


**Figure 2.5 (a) Intermodulation in a non-linear system. (b) Third-order intercept.**

$$20\log_{10}\left|\alpha_1 G + \frac{3}{4}\alpha_3 G^3\right| = 20\log_{10}|\alpha_1| - 1dB, \tag{2.22}$$

resulting in:

$$G_{1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \quad (dB) \quad , \tag{2.23}$$

alternatively in dBm:

$$G_{1dB} = 0.36 + 10\log\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right| \quad (dBm) \quad . \tag{2.24}$$

## 2.2.3 - Intermodulation Distortion

Another performance metric used to evaluate the distortion of a system is to measure how "multiplicative" the distortion is, by applying an input with multiple-tones and measuring the system response. A common measure used is the intermodulation distortion in a "two-tone" test, and is quantified by the input and output third-order intercepts, $IIP_3$ and $OIP_3$, respectively.

When two adjacent tones, separated by a frequency of $2\Delta\omega$, are applied to the input of a non-linear system, the output generally exhibits some frequency components that are not direct harmonics of the input frequencies, called intermodulation (*IM*) products,

which are due to the mixing of the two input tones as shown in Fig. 2.5(a).

Consider the input signal $x(t) = G\cos\omega_1 t + G\cos\omega_2 t$, where $\omega_1 = \omega_o - \Delta\omega$, and $\omega_2 = \omega_o + \Delta\omega$, and $\omega_o$ is the center frequency. The output spectrum, as given by equation 2.18, becomes:

$$y(t) = \alpha_1(G\cos\omega_1 t + G\cos\omega_2 t) + \alpha_2(G\cos\omega_1 t + G\cos\omega_2 t)^2 + \alpha_3(G\cos\omega_1 t + G\cos\omega_2 t)^3 + \ldots. \tag{2.25}$$

By expanding equation 2.25, the third order *IM* products (*IM3*) can be obtained as:

$$\omega = 2\omega_1 - \omega_2;\ y_{IM3} = \frac{3\alpha_3 G^3}{4}\cos(2\omega_1 - \omega_2)t = \frac{3\alpha_3 G^3}{4}\cos(\omega_o - 3\Delta\omega)t, \tag{2.26}$$

$$\omega = 2\omega_2 - \omega_1;\ y_{IM3} = \frac{3\alpha_3 G^3}{4}\cos(2\omega_2 - \omega_1)t = \frac{3\alpha_3 G^3}{4}\cos(\omega_o + 3\Delta\omega)t. \tag{2.27}$$

From equations 2.26 and 2.27, it can be easily seen that the third order *IM* products increase in proportion to $G^3$, whereas the fundamental tone increases linearly with $G$. On a logarithmic scale, the magnitude of the *IM* products grows at three times the rate at which the main tone increases. The $IIP_3$ and $OIP_3$ are defined as the point where the powers of the fundamental tones (i.e. $\alpha_1 G$) equal the powers of the third order intermodulation products (i.e. $\frac{3\alpha_3 G^3}{4}$), as shown in Fig. 2.5(b). Mathematically, it can be expressed as:

$$\alpha_1 IIP_3 = \frac{3\alpha_3 (IIP_3)^3}{4}\ . \tag{2.28}$$

Hence,

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}\ \ (dB)\ , \tag{2.29}$$

and alternatively, the $IIP_3$ can be expressed in dBm and is given by:

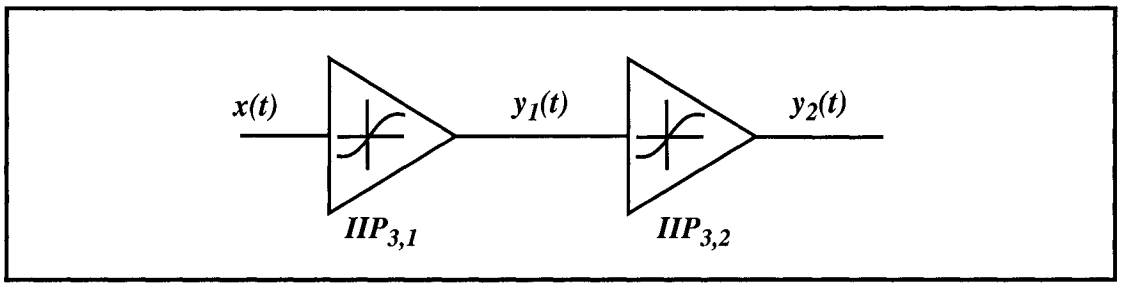


**Figure 2.6 Cascade of two non-linear stages.**

$$IIP_3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm}, \tag{2.30}$$

where $P_{in}$ is the input power level in dBm, and $\Delta P$ is the difference in the power level in dB between the fundamental and the *IM3* tones, as shown in Fig. 2.5(a).

## 2.2.4 - Cascaded Non-Linearities

Consider two non-linear stages in cascade as shown in Fig. 2.6, with input-output characteristics expressed as:

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t), \tag{2.31}$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^2(t) + \beta_3 y_1^3(t). \tag{2.32}$$

Then, by only considering the first and third order terms, it can be easily shown that the overall transfer function of a cascade system is given by:

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3)x^3(t) + \ldots. \tag{2.33}$$

Thus, similar to equation 2.29, the overall $IIP_3$ of two non-linear stages in cascade is:

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3}\right|} \quad (dB) \ . \tag{2.34}$$

Alternatively, by manipulating equation 2.34, we can write:

$$\frac{1}{IIP_3^2} = \frac{3}{4} \cdot \frac{|\alpha_3\beta_1| + |2\alpha_1\alpha_2\beta_2| + |\alpha_1^3\beta_3|}{|\alpha_1\beta_1|} \tag{2.35}$$

$$= \frac{1}{IIP_{3,1}^2} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1^2}{IIP_{3,2}^2}, \tag{2.36}$$

where $IIP_{3,1}$ and $IIP_{3,2}$ are the input $IP_3$ of the first and second stages, respectively.

For $n$ cascaded non-linear stages, the overall $IIP_3$ of the system can be derived by generalizing equation 2.36 and is expressed as:

$$\frac{1}{IIP_3^2} \approx \frac{1}{IIP_{3,1}^2} + \frac{\alpha_1^2}{IIP_{3,2}^2} + \frac{\alpha_1^2\beta_1^2}{IIP_{3,3}^2} + \ldots + constant. \tag{2.37}$$

As can be seen from equation 2.36, the non-linearity of the latter stages have a bigger impact on the overall non-linearity of the system, since the $IP_3$ of each stage is effectively degraded by the total gain preceding that stage.

## 2.3 - CMOS LNA Fundamentals

Apart from the low noise characteristics targeted in LNA designs, input matching and power gain are also two important performance metrics. Input impedance matching is essential in an LNA design because the device has to provide a 50 Ω termination for the transmission line delivering the RF signal from off-chip. It should be noted that often the performance of the preceding filter (e.g. band selection filter) depends heavily on the quality of the terminating impedance. The power gain of an LNA is also critical, since higher gain translates into an improvement in the overall receiver noise figure, at the expense of higher non-linearity for the subsequent stages, as evident from equations 2.17 and 2.37.

In this section, a detailed derivation of design equations and constraints on the input matching and the gain of CMOS LNA's are presented.

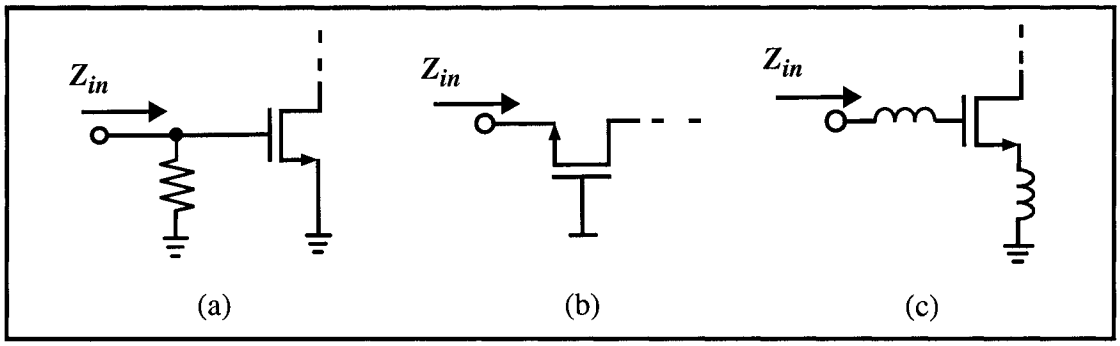


**Figure 2.7 LNA input matching topologies: (a) resistive terminations, (b) $1/g_m$ terminations, and (c) inductive degeneration.**

## 2.3.1 - Input Impedance Matching

There exists several input impedance matching approaches in LNA designs, as shown in Fig. 2.7. Each of these matching techniques can be applied in either a single-ended (as shown) or in a differential form. Note that a balun is required to transform a single-ended RF signal from the antenna to the differential form. Practical baluns introduce losses to the signal path, which directly add to the overall noise figure of the system.

The first topology, shown is Fig. 2.7(a), uses resistive termination at the input port in order to provide a 50 Ω impedance matching. There are several disadvantages in using this technique: The extra resistor contributes its own thermal noise to the output, which equals the noise contribution of the source resistance. This means that there would be an immediate 3 dB increase in the noise figure. Furthermore, the input signal is attenuated by the resistor termination before reaching the active device, which translates into a reduction in gain and a further degradation in the overall noise performance. The large noise penalty due to the use of a resistive termination makes this architecture undesirable.

The second topology, shown in Fig. 2.7(b), uses the source of a common gate stage as the input termination. Appropriate transistor sizing and biasing is chosen such that the impedance looking into the source of the transistor (i.e. $1/g_m$) equals the characteristic impedance of 50 Ω. It can be shown that the lower bounds on the noise factor of this topology in a CMOS technology is given by:

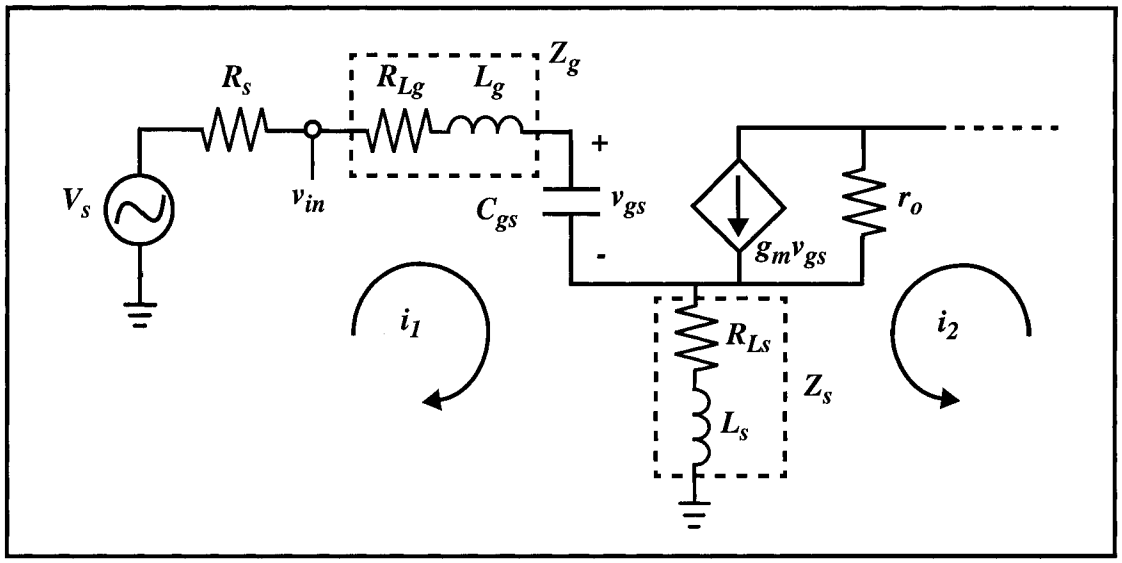


**Figure 2.8 Small signal equivalent circuit at the input of the LNA.**

$$F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} \Rightarrow NF = 2.2\,dB, \tag{2.38}$$

and

$$\alpha \equiv \frac{g_m}{g_{d0}}, \tag{2.39}$$

where $\gamma$ is a bias-dependent factor of the channel thermal noise, $g_m$ is the device transconductance, and $g_{d0}$ is the zero-bias drain conductance. The computed minimum noise figure of 2.2 dB in equation 2.38 is based on the assumption of long channel devices with parameters $\gamma$ = 2/3 and $\alpha$ = 1. In today's deep sub-micron CMOS devices, $\gamma$ can be as high as two-to-three, which is due to the hot electrons effect, and $\alpha$ can be less than one. The theoretical minimum achievable noise figure for short channel devices in this topology is around 3 dB, which doesn't satisfy today's low noise requirements.

The third topology is popular due to its inherent good noise performance: It employs inductive source degeneration, as shown in Fig. 2.7(c), to present a real impedance at the input terminal. This architecture has been adopted in our designs and is discussed in details.

Consider the small signal equivalent circuit at the input of the LNA, as shown in

Fig. 2.8. We can write down the following KVL equation:

$$v_{in} = i_1 Z_g + v_{gs} + (i_1 + i_2) Z_s, \tag{2.40}$$

where

$$v_{gs} = \frac{i_1}{j\omega C_{gs}}. \tag{2.41}$$

By ignoring the effect of channel length modulation, modeled by $r_o$, the loop current $i_2$ becomes $g_m v_{gs}$. This assumption is valid in the case of the cascode configuration, since the impedance looking into the following stage equals to $1/g_{m2}$, which is much smaller than $r_o$.

By manipulating equation 2.40, the input impedance ($Z_{in}$) can be expressed as:

$$Z_{in} \equiv \frac{v_{in}}{i_1} = Z_g + Z_s + \frac{1}{j\omega C_{gs}} + \frac{g_m}{j\omega C_{gs}} Z_s. \tag{2.42}$$

From equation 2.42, one can see that a real term can be obtained by making $Z_s$ to be inductive. Furthermore, $Z_g$ can also be made inductive and, combined with $Z_s$, it can be made to resonate with $C_{gs}$ at the required center frequency $\omega_o$. Hence, equation 2.42 becomes:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}. \tag{2.43}$$

At the resonant frequency (i.e. $\omega = \omega_o$), the above equation becomes:

$$\omega_o^2 = \frac{1}{(L_g + L_s) C_{gs}}, \tag{2.44}$$

$$Z_{in}(\omega = \omega_o) = \frac{g_m L_s}{C_{gs}} = \omega_T L_s. \tag{2.45}$$

By choosing appropriate sizing for the transistor and inductors, source degeneration inductor ($L_g$) is used to match the real part of the input impedance to the characteristic

impedance of 50 Ω, while the combination of the source and gate inductors are used to cancel out the reactance due to the parasitic capacitance ($C_{gs}$) of the input transistor at the resonant frequency.

In reality, integrated inductors are lossy with finite parasitic series resistances as shown in Fig. 2.8. This affects the quality of the input impedance matching and equation 2.43 becomes:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}}(1 + g_m R_{L_s}) + \frac{g_m L_s}{C_{gs}} + R_{L_s} + R_{L_g}. \qquad (2.46)$$

Note that, with the presence of the inductor series resistance, the matching conditions become more complex to satisfy, as the inductance values and resistances are correlated and layout dependent parameters. Furthermore, the absence of accurate inductor modeling programs at RF increases the difficulty in obtaining the optimum matching. Nonetheless, initial inductance values can be obtained from equations 2.44 and 2.45.

### 2.3.2 - LNA Gain

Reconsider the equivalent circuit of the input of the LNA at resonance, as shown in Fig. 2.8, with the input impedance matched to the source impedance (i.e. 50 Ω). The gate-to-source voltage, from equation 2.41, can be expressed as:

$$v_{gs} = \frac{i_1}{j\omega C_{gs}} = v_s \cdot \frac{1/(j\omega_o C_{gs})}{2Z_{in}}. \qquad (2.47)$$

Hence:

$$\left|\frac{v_{gs}}{v_s}\right| = \frac{1/\left|(j\omega_o C_{gs})\right|}{2Z_{in}} = \frac{Q_{in}}{2}, \qquad (2.48)$$

and

$$\left|\frac{i_2}{v_s}\right| = \left|\frac{g_m v_{gs}}{v_s}\right| = g_m \frac{Q_{in}}{2}, \qquad (2.49)$$

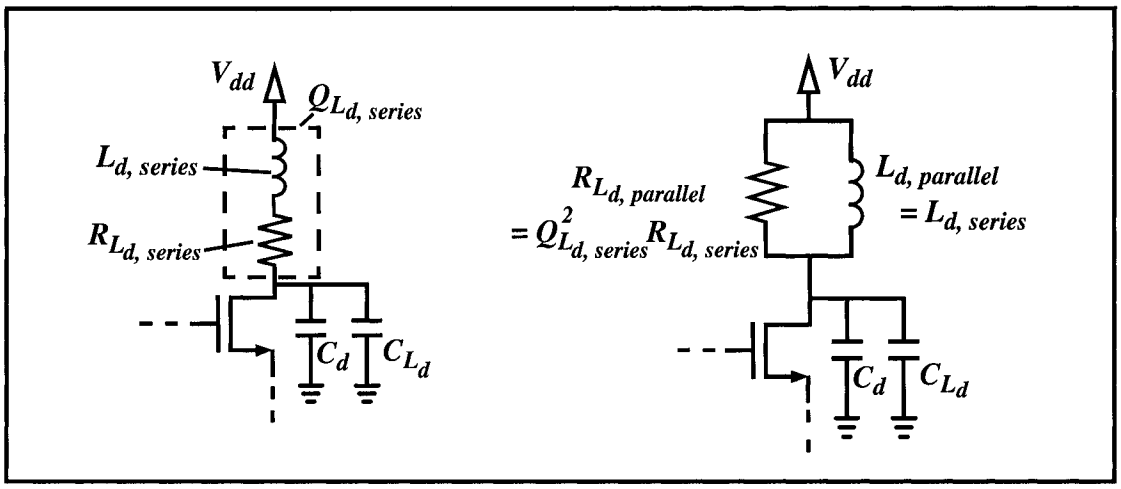


**Figure 2.9 Series-shunt transformation of the resonant tank.**

where $Q_{in}$ is the quality factor of the input series RLC resonant tank.

Thus, the voltage gain can be expressed as:

$$A_v = g_m \frac{Q_{in}}{2} Z_d, \tag{2.50}$$

where $Z_d$ is the drain impedance.

Note that a high voltage gain can be obtained by increasing $Q_{in}$ and $Z_d$. The quality factor of the input tank can be maximized by reducing the gate-to-source capacitance ($C_{gs}$), as shown from equation 2.48. Decreasing $C_{gs}$ means that $L_s$ and $L_g$ have to increase in order to maintain the same resonant frequency, as can be seen from equation 2.44. In reality, blindly increasing these inductance values has a negative impact on $Q_{in}$, since the added parasitic series resistances would degrade the overall quality factor of the input tank. Hence, there is a trade-off when choosing the inductance values. This trade-off often varies between different technologies, as well as different design methodologies.

Maximizing the drain impedance can also increase the overall voltage gain of the LNA. Consider a drain inductor ($L_{d,series}$) with a series resistance ($R_{L_{d,\,series}}$). It can be shown that by applying the series-shunt transformation at the resonant tank, as described in Fig. 2.9, the impedance looking into the tank becomes:

$$L_{d,\,parallel} = \frac{Q_{L_{d,\,series}}^2 + 1}{Q_{L_{d,\,series}}^2} L_{d,\,series} \approx L_{d,\,series}, \tag{2.51}$$

and

$$R_{L_{d,\,parallel}} = \left(Q_{L_{d,\,series}}^2 + 1\right) R_{L_{d,\,series}} \approx Q_{L_{d,\,series}}^2 R_{L_{d,\,series}} = Z_d. \tag{2.52}$$

From equation 2.52, it is quite misleading to think that the drain impedance can be simply maximized by both increasing the drain inductor quality factor and the series resistance! In fact, this is not the case, since the quality factor and the series resistance are two counter-balancing parameters and are related as follows:

$$Q_{L_{d,\,series}} = \frac{\omega_o L_{d,\,series}}{R_{L_{d,\,series}}}. \tag{2.53}$$

Hence, the drain impedance at resonance can be expressed as:

$$Z_d(\omega = \omega_o) = \frac{\omega_o^2 L_{d,\,series}^2}{R_{L_{d,\,series}}}, \tag{2.54}$$

and

$$\omega_o^2 = \frac{1}{L_{d,\,series}(C_d + C_{L_d})}, \tag{2.55}$$

where $C_d$ is the capacitance at the drain, and $C_{L_d}$ is the parasitic capacitance of the drain inductor. Note that the drain impedance can be maximized, hence the overall voltage gain can be increased, by choosing an inductor that can achieve the maximum $L^2/R$ ratio, rather than just simply optimizing for its quality factor alone, as evident from equation 2.54.

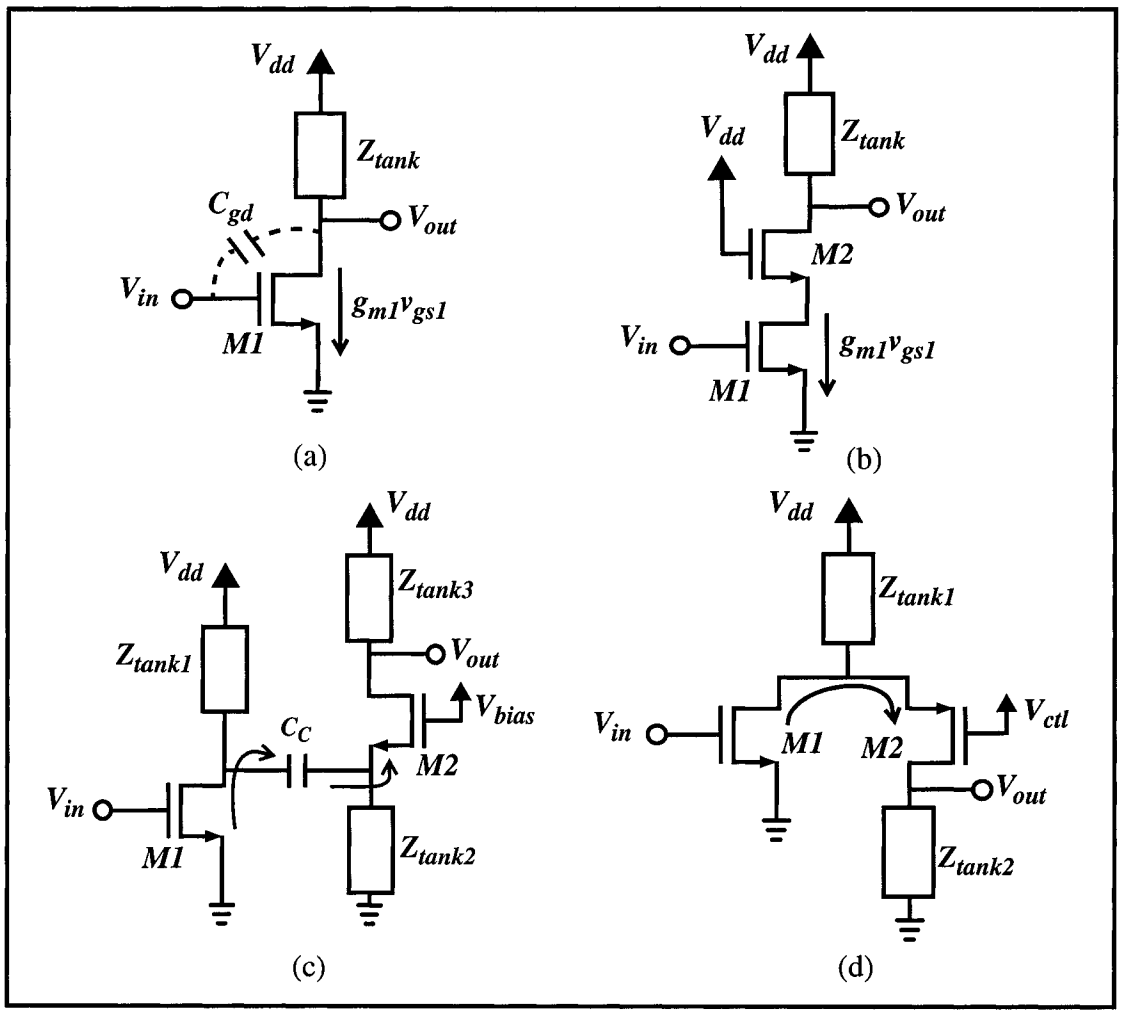


**Figure 2.10 LNA topologies: (a) Single transistor. (b) Conventional cascode. (c) LC-coupled. (d) Modified folded cascode [44].**

## 2.4 - Low Voltage LNA Topologies

The development of wireless portable electronics is moving towards smaller and lighter devices with longer operating time, which requires compact low-voltage and low-power design topologies [43], [44]. Furthermore, the general trend of semiconductor device scaling has lead to reduced voltage requirements in order to avoid breakdown effects. For example, by migrating from a 0.35 μm to a 0.18 μm CMOS process, the typical turn-on voltage of an NMOS transistor is decreased from 0.7 V to 0.5 V, while the core supply voltage is reduced from 3.5 V to 1.8 V. These trends dictate that future RF

frond-ends will have to operate with low supply voltages (i.e. < 1 V). Under the reduced voltage supply, many common circuit topologies in RF designs, such as the conventional cascode structure and the Gilbert-cell structure, can no longer be employed because of the stacking constraints of transistors between the supply rails.

With the targeted voltage supply down to 1 V there are limited numbers of suitable LNA topologies. Some amplifier implementations which can operate at sub-1 V, along with the conventional cascode amplifier, are shown in Fig. 2.10. Due to the superior noise performance of the common-source configuration with inductive degeneration in LNA designs, as discussed in section 2.3.1, all the topologies presented in this thesis are based on this configuration. Furthermore, inductors are used as resonant tanks instead of resistive loads in order to minimize the loss of voltage headroom. Although the discussions here are focused in the context of CMOS LNA's, these low-voltage topologies can be generalized to other technologies such as silicon bipolar, which was demonstrated in [35], [45].

### 2.4.1 - Single Transistor LNA Topology

Consider the single transistor amplifier shown in Fig. 2.10(a). The minimum voltage headroom for this topology equals the voltage required to set the transistor into saturation (i.e. $V_{ds-sat}$). Since only a single voltage supply is used in an actual implementation, the absolute minimum voltage equals the threshold voltage of the transistor (i.e. $V_{th}$), which is typically greater than $V_{ds-sat}$. Despite meeting the sub-1 V design requirement, there remains many challenges with using this topology, which make it not desirable as the choice for a low-voltage RF architecture. The main disadvantage of this topology is that it is very susceptible to instability problems as the frequency of operation increases. This is mainly due to the gate-to-drain parasitic capacitance ($C_{gd}$) which provides a low impedance feedback signal path at RF. Furthermore, following Miller transformation [46], the equivalent input capacitance ($C_{in}$) of the transistor becomes:

$$C_{in} = C_{gs} + (1 - A_v)C_{gd}, \tag{2.56}$$

where $A_v$ is the voltage gain across the gate-to-drain capacitance of the common-source

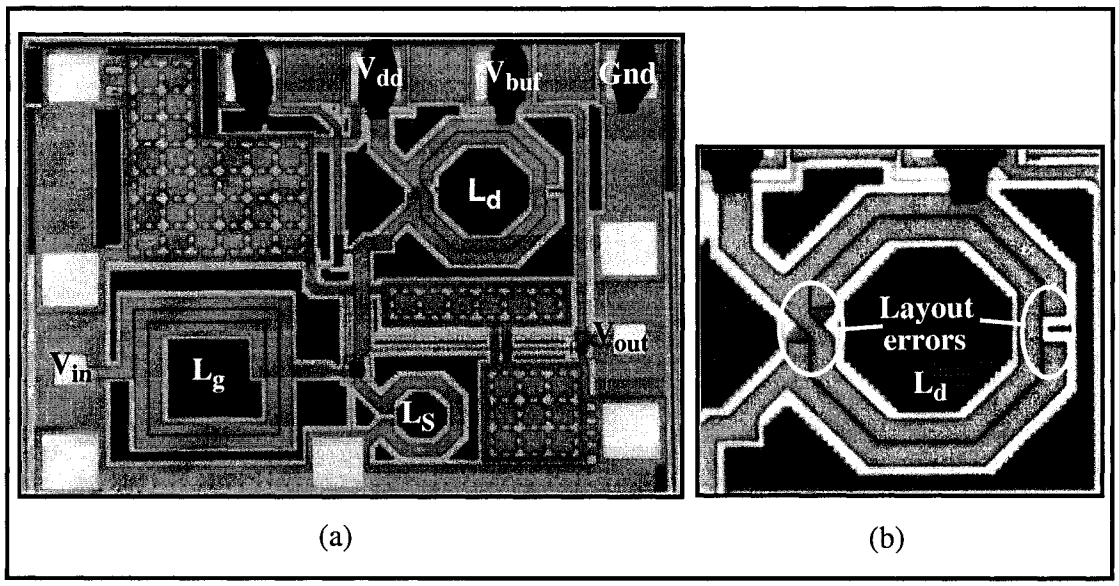


**Figure 2.11 (a) Microphotograph of the 1 V 5.8 GHz cascode CMOS LNA. (b) A zoom-in view of the tank inductor [47].**

transistor. This setup further complicates the input impedance and noise matching, since the input reactance becomes not only dictated by $C_{gs}$, as can be seen in equation 2.43, but is also a function of $A_v$ and $C_{gd}$. Hence, it is rare to see implementations using this topology in modern ***fully integrated*** high frequency RF designs.

## 2.4.2 - Conventional Cascode LNA Topology

In order to alleviate the potential instability problems in a single transistor amplifier, a common approach is to use the cascode configuration shown in Fig. 2.10(b). This topology, together with the common-source configuration, has proven to be popular with excellent gain and noise performance in LNA designs. Substantial research (e.g. [22], [31]) have been invested in LNA designs based on this topology. One of the main drawbacks of this structure is the need for a relatively high supply voltage headroom, since it involves a minimum of two transistor stacking, which is not quite suitable for sub-1 V applications. However, as the minimum feature size of transistors decreases, the threshold voltage ($V_{th}$) and the drain-to-source voltage ($V_{ds}$) are further reduced. It becomes possible to implement a low-voltage (i.e. < 1V) cascode LNA in deep sub-micron technologies, but at the price of a degradation in linearity. The reason behind the

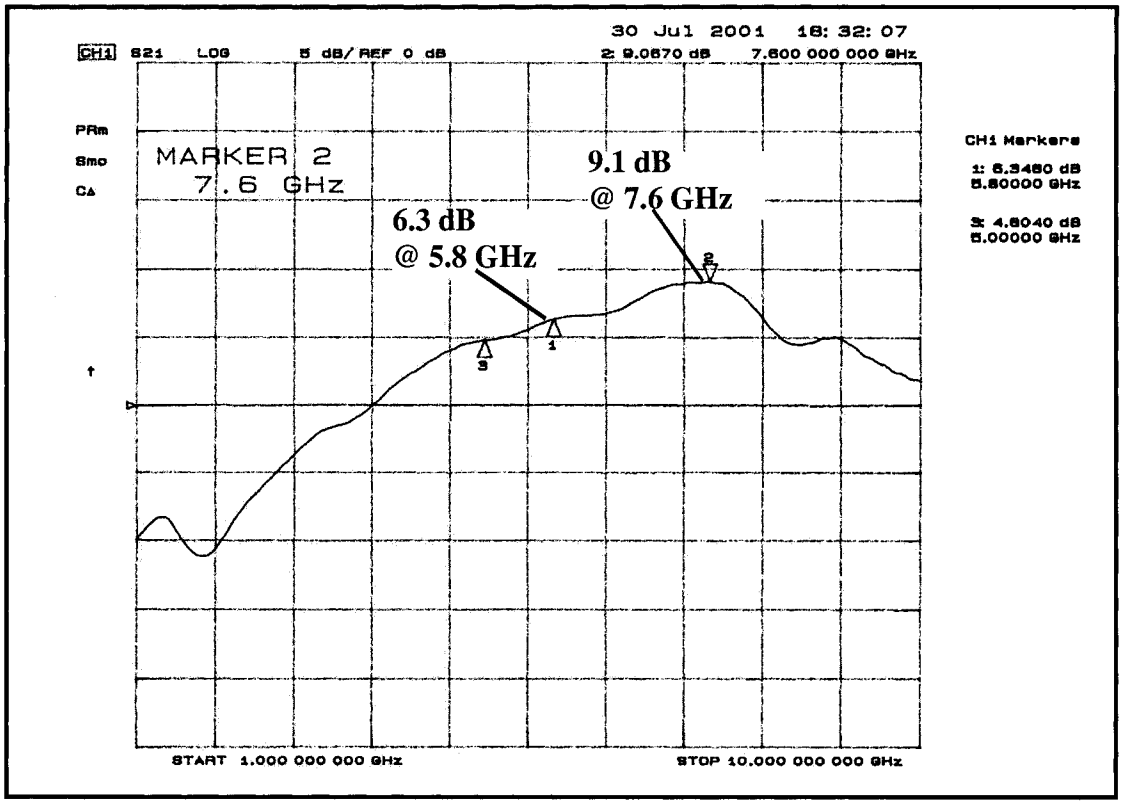


**Figure 2.12 Measured power gain of the 1 V cascode CMOS LNA [47].**

linearity degradation is that the transistors are forced to operate close to the triode region (i.e. close to $V_{ds-sat}$) as the supply voltage decreases.

A prototype has been implemented to evaluate the performance of the conventional cascode structure under low-voltage operation [47]. The design was implemented in a 0.18 μm digital CMOS process, targeting a center frequency of 5.8 GHz with a supply voltage of 1 V. The expected power gain and noise figure were 17 dB and 1.7 dB respectively. The microphotograph of the CMOS LNA is shown in Fig. 2.11(a). The measured forward transmission ($S_{21}$) of the LNA is shown in Fig. 2.12. The expected, as well as the measured, LNA performances are shown in Table 2.1. Note the discrepancy between the expected and measured performances. In particular, the center frequency shifted from 5.8 GHz to 7.6 GHz, and the gain was reduced by more than 7 dB. After a detailed investigation, it was found that this large discrepancy was mainly due to a fatal layout error. This mistake was caused by the shortening of the resonant tank inductor loop, as can be seen in Fig. 2.11(b). This resulted in a decrease in the inductance as well

as the tank impedance (equation 2.54), and hence the tank resonates at a higher frequency with a lower gain. Accurate overall noise figure and linearity can not be expected in this case since the resulting resonant frequency is off from the targeted operating frequency of 5.8 GHz. Nevertheless, this work has demonstrated the feasibility of using the conventional cascode structure to realize LNA designs operating at 1 V. With further device scaling, we anticipate the use of this topology at lower supply voltages.

### 2.4.3 - LC-Coupled LNA Topology

The need to increase the linearity of the conventional cascode structure, when operated from a very low supply voltage, has motivated the development of the LC-coupled LNA topology shown in Fig. 2.10(c). The main idea behind this low-voltage topology is the ability to decouple the AC and DC currents between the two transistors, hence allowing the reduction of the voltage supply to less than 1 V, and avoiding pushing the transistors close to the triode region (i.e. $V_{ds} > V_{ds-sat}$). This architecture can be viewed as the low-voltage version of a cascode amplifier when certain constraints are satisfied.

To ensure that the circuit operates as a cascode amplifier, two conditions must be met simultaneously. First, in order to minimize the Miller effect, the magnitude of the signal

| | Simulated | Measured |
|---|---|---|
| Technology | CMOS 0.18 μm | CMOS 0.18 μm |
| Voltage Supply, $V_{dd}$ | 1 V | 1 V |
| Center Frequency, $f_o$ | 5.8 GHz | 7.6 GHz |
| Power Gain, $S_{21}$ | 17 dB | 9.1 dB @ 7.6 GHz |
| Noise Figure, NF | 1.7 dB | - |
| Input Reflection, $S_{11}$ | -10.7 dB | -5.9 dB @ 5.8 GHz |
| Output Reflection, $S_{22}$ | -10.9 dB | -6.1 dB @ 5.8 GHz |
| Power Consumption | 9.9 mW | 10.2 mW |

**Table 2.1 - Performance summary of the 1 V cascode CMOS LNA [47].**

gain at the drain of M1, relative to the input RF signal, should be near unity. Second, the entire RF signal current ($g_{m1}v_{gs1}$) generated by M1 should be fed into the source of M2 (i.e. driving $1/g_{m2}$). This is done by setting the LC tanks 1 and 2 to resonate (i.e. have high impedances) at the frequency of interest. However, due to the finite Q's of the integrated inductors, the impedances of the LC tanks at resonance are also finite and are given as follows:

$$Z_{\tan k1} = (Q_{\tan k1}^2 + 1)R_{L1}, \tag{2.57}$$

$$Z_{\tan k2} = (Q_{\tan k2}^2 + 1)R_{L2}, \tag{2.58}$$

where $Z_{tank}$ and $Q_{tank}$ are the impedance and the quality factor of the LC tank at resonance, and $R_L$ is the series resistance of the inductor in the resonant tank. In order to avoid signal losses along the signal path, two factors must be taken into account: The LC tank impedance ($Z_{tank1}$) must be much larger than the impedance looking into the coupling capacitor ($C_C$), in order to minimize signal divider losses. Similarly, the LC tank impedance ($Z_{tank2}$) must be larger than the impedance looking into the source of M2, in order to avoid signal losses to ground. The above constraints are summarized as follows:

$$Z_{\tan k1} \gg \frac{1}{j\omega C_C} + Z_{\tan k2} \| \frac{1}{g_{m2}}, \tag{2.59}$$

$$Z_{\tan k2} \gg \frac{1}{g_{m2}}. \tag{2.60}$$

A silicon bipolar LNA based on this topology has been demonstrated in [35]. It has shown the ability to use this topology to operate at above the 5 GHz band, with a low supply voltage of 1 V. The performance summary of this 5.8 GHz LC-coupled bipolar LNA is shown in Table 2.2

A comparative study in [45] has shown that the linearity performance (in terms of IP3's) of the 1 V LC-coupled structure is similar to the conventional cascode structure with twice the voltage headroom (i.e. 2 V) at 1.9 GHz. This LC-coupled architecture is a

promising low-voltage topology but it imposes certain challenges. The performance of this structure is heavily dependent on the quality of the two coupled LC resonant tanks which act as AC blockers. Furthermore, it is critical to match the two LC tanks to resonate at the frequency of interest. All of these stringent requirements are rooted to the fundamental question of how good are the performances of the integrated inductors in a particular process. Both of the two implementations reported are implemented in a silicon bipolar technology, where slightly higher qualities and more accurate modeling of inductors were available. CMOS implementations of this topology has not been successfully demonstrated, owing to the low qualities of inductors operating at frequencies beyond 5 GHz. Future advances in the development of high performance integrated inductors (e.g in SOI CMOS technologies) with accurate modeling will increase the popularity of this topology.

| | **Measured Results** |
|---|---|
| **Technology** | **Silicon Bipolar $f_T$=25 GHz** |
| **Voltage Supply, $V_{dd}$** | **1 V** |
| **Center Frequency, $f_o$** | **5.8 GHz** |
| **Power Gain, $S_{21}$** | **11.5 dB** |
| **Noise Figure, NF** | **4.0 dB** |
| **Input Reflection, $S_{11}$** | **-9.0 dB** |
| **Output Reflection, $S_{22}$** | **-13.7 dB** |
| **Power Consumption** | **6.6 mW** |
| **1-dB Compression Point, $P_{1\text{-}dB}$** | **-19 dBm** |

**Table 2.2 - Performance summary of the 1 V LC-coupled bipolar LNA [35].**

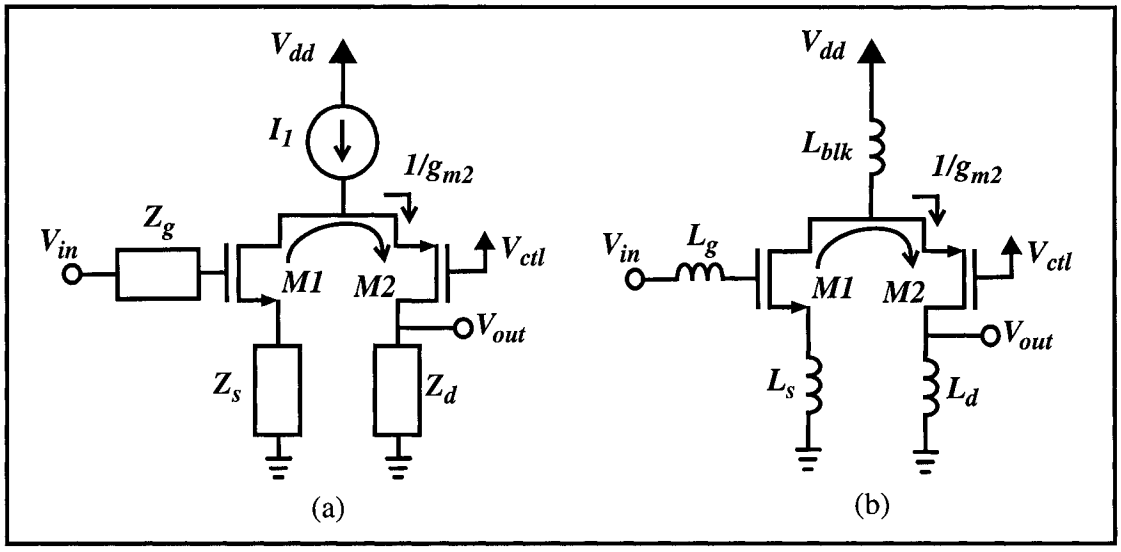


**Figure 2.13 Folded cascode topologies: (a) Wideband conventional. (b) Narrowband modified.**

## 2.4.4 - Folded Cascode LNA Topology

Motivated by the need to relax the requirements on integrated inductors, a new low-voltage LNA topology has been developed as shown in Fig. 2.10(d). Historically, PMOS devices were not favorable in LNA designs because of their poor RF performances (e.g. $f_T$). As CMOS technologies scaled down to 0.18 μm, the $f_T$ of PMOS devices became in the order of 20 GHz, making them good candidates for low-voltage high performance LNA designs. The proposed low-voltage design is based on a folded cascode topology with modifications, which make it suitable for sub-1 V LNA applications.

The conventional folded cascode topology, shown in Fig. 2.13(a), is a popular structure in op-amp designs used to reduce the supply voltage requirement. In this topology, NMOS transistor M1 is used for amplifying the input signal, while the PMOS transistor M2 acts as a current buffer. The signal current (i.e. $g_{m1}v_{gs1}$) generated by M1 is forced into the source of M2 (i.e. driving $1/g_{m2}$), since the current source ($I_1$) exhibits a wideband (*from DC to* $f_T$) small signal high impedance. The main idea behind the modified folded cascode structure, shown in Fig. 2.13(b), is similar to the conventional folded cascode amplifier.

Since LNA's are usually used for narrowband applications to amplify the signals of

interest in a desired band of several MHz, the wideband current source ($I_1$) could be replaced by a narrowband equivalent circuit. One simple candidate is to replace the current source by an LC resonant tank circuit which makes use of an integrated inductor to resonate with the parasitic capacitances at the center frequency. Similar to the LC-coupled topology, the performance of this structure is limited by using an on-chip LC resonant tank with low quality factor. In a typical CMOS process, the quality factor of integrated spiral inductors, operating over the 5 GHz band, is in the order of 5 - 6. This low quality factor translates into a low tank impedance $Z_{tank}$ for signal blocking (equation 2.54), which is comparable to the impedance looking into the source of M2 (i.e. $1/g_{m2}$). Hence, the overall gain obtained by using this technique is reduced due to the signal division between the tank and the signal path.

One of the remedies to mitigate this problem is to use high quality off-chip components for the resonant tank circuit. One might object to the use of this approach since it goes against the trend of full integration. However, when examining the topology carefully, it is not difficult to notice that the DC voltage supply connected to the LC resonant tank is essentially coming from an off-chip power supply (e.g. from a battery in a wireless receiver system). Hence, in an actual chip implementation, the LC resonant tank can be implemented by a combination of bonding wires, package leads, and inductive traces on a printed circuit board. The estimated inductance of the "combined" inductor ($L_{blk}$) is greater than 5 nH at frequencies beyond 5 GHz. Thus, the blocking impedance ($Z_{blk}$) is much larger than the fully integrated counterpart and results in better signal blocking. The blocking condition is summarized as follows:

$$Z_{blk} \approx j\omega_o L_{blk} \gg \frac{1}{g_{m2}}. \tag{2.61}$$

One inherent advantage of this topology over the other architectures is its potential to allow gain controlability, which can result in overall linearity improvement. The gain variation is achieved by controlling the gate voltage ($V_{ctl}$) of the PMOS transistor M2, hence adjusting the overall gain of the LNA by varying the impedance looking into the source of transistor M2 (i.e.$1/g_{m2}$). Gain control is done ***without affecting the input noise and impedance matching*** which are set by the input NMOS transistor M1 only. A

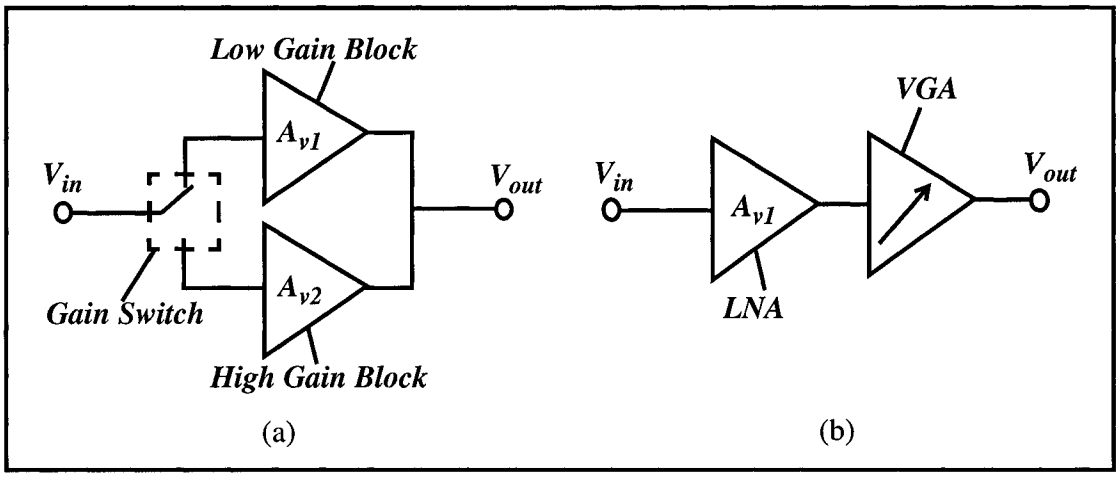


**Figure 2.14 Conceptual view of the variable gain amplifiers: (a) Switch-control type. (b) Two-stage LNA-VGA type.**

reasonably low noise figure can be achieved with gain controllability using this topology. Conventional cascode amplifiers do not have this flexibility in gain-control, since the overall gain of the LNA is governed by the input transistor M1 while the cascode transistor M2 only acts as a current buffer. Gain control could only be achieved by altering the biasing current through M1, and consequently affecting the whole input noise and impedance matching, which is definitely not desirable.

The simplicity of incorporating gain-control in this topology is really one of its biggest advantages. Existing variable gain amplifier (*VGA*) solutions (e.g. [48], [49]), are shown in Fig. 2.14. They include i) a switch-control type, which provides gain control by switching on/off active gain components, and ii) the two-stage LNA-VGA type, which achieves gain control through the use of a VGA as a second stage. This additive gain-control functionality comes at the price of higher circuit complexity, which also results in an increase in power consumption and noise degradation. Contrarily, the only increase in the LNA circuit complexity in the narrowband folded cascode topology suggested in this work is an extra gain-control signal ($V_{ctl}$), as shown in Fig. 2.13(b). The performance of the folded cascode topology is presented as experimental results in Chapter 4.

With a strong drive towards low-voltage design topologies, several LNA architectures which are suitable for sub-1 V applications have emerged. The conventional folded cascode structure is a popular low-voltage approach in low frequency op-amp designs. The modified folded cascode LNA topology is based on this conventional architecture,

with slight modifications making it suitable for narrowband RF applications. It is a promising low-voltage structure, well-balanced in terms of stability, noise, and gain performances, with an inherent advantage of gain controlability over other architectures. In this work, all the designs are based on the modified folded cascode topology, with a strong focus on pushing the operating frequency limit beyond 5 GHz, in commercial CMOS processes for future wireless communications.

One of the common limitations in all topologies is that the performances of the LNA's are heavily dependent on the qualities of on-chip passive components (e.g. inductors and capacitors), which are low in integrated CMOS technologies. In the next chapter, we focus on design guidelines of integrated passive devices.

# Chapter 3 - Design of RF Passive Components

Passive components such as inductors and capacitors play an integral part in the performances of circuit building blocks in a transceiver, especially at high frequencies. In particular, passive devices are used for impedance and noise matching, as well as in LC-tuned loads in LNA designs, which are the main focus of this thesis.

In this chapter, systematic design and optimization of passive devices beyond 5 GHz is presented. Various loss mechanisms which limit the performances of passives at RF, in silicon CMOS processes are examined. The possibility of using emerging technologies such as MEMS for implementing passive devices are investigated. Design equations and measurement results of RF MEMS passive devices are summarized.

## 3.1 - Passive Devices in Si CMOS Technologies

### 3.1.1 - The Quality of Passive Devices

An important parameter to consider when discussing passive devices is the quality factor ($Q$). The quality factor is generally defined as:

$$Q = 2\pi \frac{E_{store}}{E_{diss}}, \tag{3.1}$$

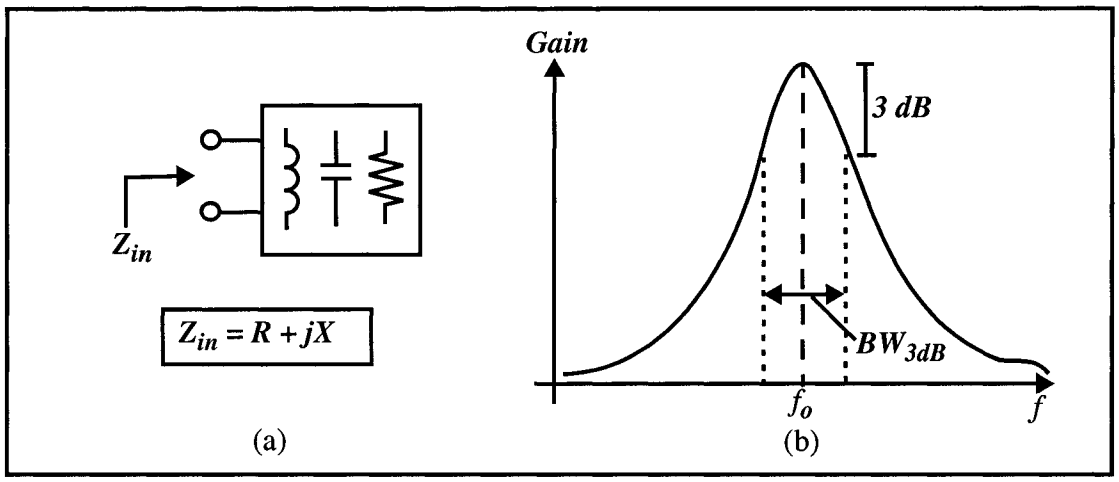


**Figure 3.1 (a) Input impedance of a practical passive device. (b) Quality factor of an LC resonant tank.**

where $E_{store}$ is the energy stored per cycle, and $E_{diss}$ is the energy dissipated per cycle in a device.

The higher the Q factor, the lower the loss of a passive device. This definition is the most relevant when discussing inductors and capacitors, as such devices are meant to store energy, while dissipating little to no energy in the process. Thus, ideal inductors and capacitors having zero energy loss would have infinite Q's, whereas practical devices normally have finite Q's.

Based on the definition in equation 3.1, the quality factor of a practical inductor can be expressed as:

$$Q = \frac{X_{ind}}{R_{ind}} = \frac{\omega L}{R} = \frac{2\pi f L}{R}, \tag{3.2}$$

and the quality factor of a practical capacitor can be expressed as:

$$Q = \frac{X_{cap}}{R_{cap}} = \frac{1}{\omega C R} = \frac{1}{2\pi f C R}, \tag{3.3}$$

where $X$ is the reactive component of a passive device storing energy, and $R$ is the resistive component of a passive device dissipating energy (Fig. 3.1(a)).

Apart from measuring the performance of a passive device, the quality factor can also measure the selectivity of a resonant circuit. Due to the bandpass nature of a resonant

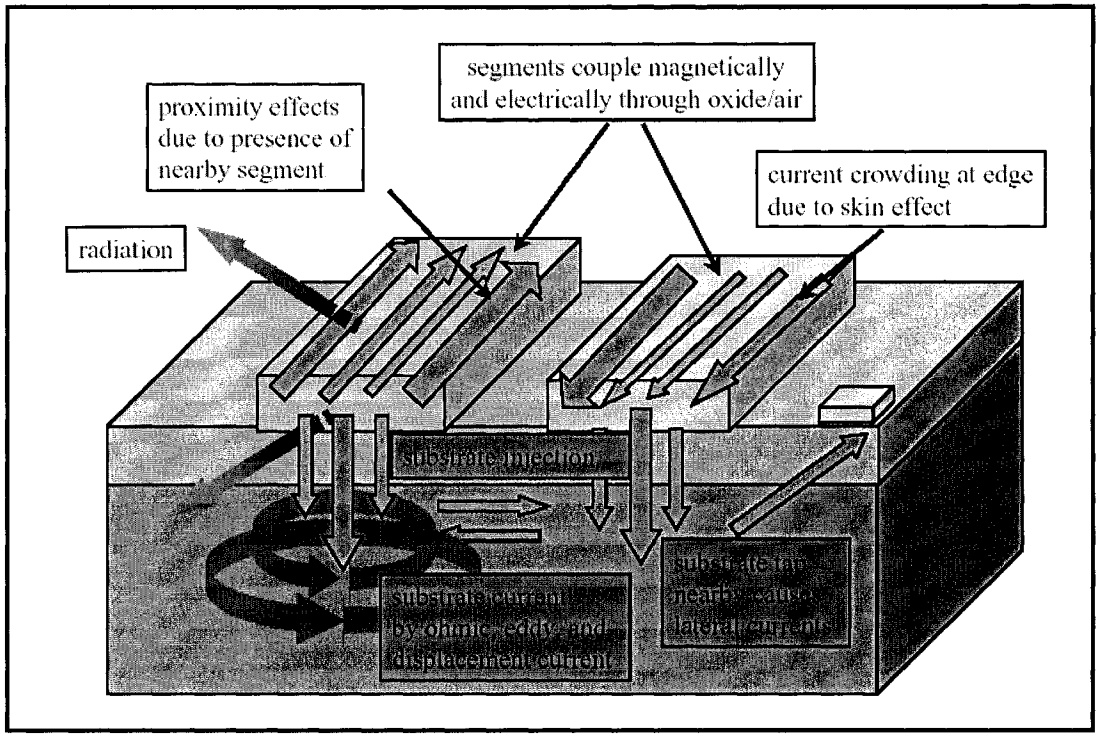


**Figure 3.2 Various loss mechanisms in an IC process [50].**

tank, the quality factor of an LC-tank can be expressed as follows (among several other possible definitions):

$$Q = \frac{f_o}{BW_{3dB}}, \tag{3.4}$$

where $f_o$ is the resonant frequency and $BW_{3dB}$ is the 3 dB bandwidth of the response, as shown in Fig. 3.1(b).

## 3.1.2 - Loss Mechanisms

The quality factors of integrated passive devices are largely dependent on the material used in the IC fabrication processes. Particularly, the semiconductor substrate and the metal layers used to construct the devices play the most important roles. Various loss mechanisms at RF for a simple example consisting of two parallel conductors carrying currents in opposite directions are summarized in Fig. 3.2 [50]. Some dominant losses at RF include metal losses and substrate induced losses.

**(a) Metal Losses** - Passive devices such as inductors and capacitors are constructed from layers of metal, typically aluminum and polysilicon layers. Their conductivities essentially dictate the quality factors of the passive devices at frequencies below 1 GHz. Due to the finite conductivities of the metal layers, practical passive devices exhibit ohmic losses, which results in finite Q factors. The ohmic losses are dissipated as heat in the volume of the conductors. In an electric model, these losses can be represented by resistors in series with the passive devices.

As the frequency increases, the current distribution in the metal layers changes due to the Eddy currents in the conductors, which results in the skin and proximity effects. The skin-effect arises when AC currents tend to accumulate at the outer layer, or skin, of the conductors, resulting from the fact that the magnetic fields of the device penetrate the conductors and produce opposing electric fields within its volume. The reduction of the effective cross-sectional area of the conductors increases the current density of the device at increasing frequencies. This results in an increase in the "effective" AC resistance, and is typically a function of $\sqrt{f}$ . The skin-effect is more pronounced at high frequencies when the thickness of the conductor is comparable to the depth of penetration of the current or the skin depth ($\delta$), which is defined as:

$$\delta = \sqrt{\frac{2}{2\pi f \mu \sigma}}, \tag{3.5}$$

where $\mu = \mu_o$ is the permeability of free space for a good conductor, and $\sigma$ is the conductivity of the conductor.

Another loss mechanism is the proximity effect. It arises when the magnetic fields of a particular conductor are affected by the neighboring magnetic fields, which results in varying the effective AC resistance of the conductor. In the case of a spiral inductor, conductors enhance the magnetic fields in nearby conductors, hence increase their AC resistance. On the other hand, in the case of a transformer, the magnetic fields oppose those of nearby conductors, resulting in a decrease of the AC resistance.

**(b) Substrate Induced Losses** - Planar integrated passive devices are fabricated on conductive Si substrates. The conductive nature of the Si substrates, in particular for a CMOS substrate which has a fairly low resistivity, leads to various forms of losses,

namely the conversion of the electromagnetic energy into heat through the substrate. First, the electric energy is coupled to the substrate through displacement currents. These displacement currents flow through the substrate to nearby grounds. The flow direction is perpendicular to the spiral segments. Second, substrate currents (i.e. Eddy currents) are induced due to the time-varying solenoidal electric fields which are generated by the magnetic fields penetrating the substrate. These Eddy currents flow in parallel directions to the device segments.

Finally, all other loss mechanisms can be lumped into radiation where part of the signal power is transformed into electromagnetic waves. Electromagnetically induced losses occur at frequencies where the physical dimensions of the devices are comparable to the wavelengths of the RF signals. In this work, with the targeted operating frequency range of 5-10 GHz, the equivalent wavelengths are in the order of several centimeters, which are much larger than the conductor sizes (e.g. 20 μm). Hence, radiation losses can be safely ignored at this point.

## 3.2 - Integrated Inductor Design Guidelines

Proper modeling of integrated inductors at radio frequencies is a challenging and crucial task in RFIC designs. Standard CMOS integrated inductors have inherently low quality factors (i.e. $Q < 5$) since they exhibit serious substrate and dielectric losses, which become dominant at GHz frequencies. This is mainly due to the high conductivity of the CMOS substrate. Substantial research efforts was invested into this topic recently, attempting to improve the accuracy of inductor modeling and the quality factors of inductors in a CMOS technology. The main objective of this section is to provide qualitative practical guidelines, and to point out the trade-offs in inductors design in CMOS for RF.

### 3.2.1 - Existing Work on Integrated Inductor Design

As mentioned in section 3.1.2, various losses limit the qualities of integrated inductors. In order to reduce the metal and substrate induced losses, many research efforts have been aimed at modifying the devices structures and/or the fabrication processes.

Using thick and more conductive metallizations to minimize low frequency ohmic losses, and increasing the substrate resistivities with light doping profiles, have been proposed. Also, eliminating the substrate through etching is another possible approach.

For example, to minimize metal losses, Ashby et al. [51] used a special process with highly conductive thick gold metallizations, realizing a Q of 12 at 3.3 GHz for a 2.5 nH inductor with a self-resonant frequency ($f_{RES}$) beyond 10 GHz. Burghartz and Souyer et al. [52] proposed using multi-level metallizations to realize shunt-connected spirals in order to emulate thicker conductors. They achieved a 2 nH inductor with a Q of 9.3 at 4 GHz. To minimize the effects of the substrate, Chang and Abidi [53] demonstrated the feasibility of realizing high inductances and quality factors by selectively etching out the silicon substrate under the inductors. They realized a 100 nH inductor with a self-resonant frequency of 3 GHz.

Removing the Si substrate seems to be the best technique to eliminate substrate induced losses, but it requires costly post-processing etching steps, which are not compatible with conventional CMOS processes. The work in [54] suggested a CMOS compatible method to reduce substrate losses, by utilizing patterned polysilicon or metal layers under the inductors. The patterned ground shields are used to minimize Eddy current losses in the substrate. Unfortunately, the added ground shields have a negative impact on the self-resonant frequencies due to the resulting higher capacitive coupling between the devices and the ground plane.

Apart from the mainstream optimization approaches, novel techniques using emerging technologies have also been proposed. Micromachined solenoid-type coils were demonstrated in [55], [56]. A 2.5 nH inductor with a quality factor of 19 at 5.5 GHz was illustrated.

In summary, building RF passive devices on Si substrates imposes several challenges, which need to be overcome by either process modifications or novel shielding techniques. Recent standard digital CMOS processes are equipped with RF options, where a thick top metal interconnect with high conductivity is available for implementing high quality passive elements. The focus of the following sections is to discuss the implementation of high quality passive elements in a standard CMOS process, without

any post-processing steps, for future wireless applications.

### 3.2.2 - Integrated Inductors Design Strategy Beyond 5 GHz

Much of the work described in the previous section is dealing with inductors design in the 1-5 GHz frequency range. Increasing demand on bandwidth have pushed RFIC's towards a higher span of the GHz spectrum, particularly in the 5-10 GHz domain. Most existing CMOS inductor designs in the literature, operating beyond 5 GHz, generally exhibit low quality factors. Little work has been reported in the literature on the feasibility of implementing high quality (i.e. $Q > 5$) inductors beyond 5 GHz in standard CMOS processes. In this section, a design strategy of high performance integrated inductors beyond 5 GHz is presented. It can be viewed as an extension of the optimization techniques used in the low GHz (i.e. 1-5 GHz) range.

Based on earlier work from the literature for inductors design (e.g. [51] - [58]), there is a number of approaches to implement integrated inductors. Apart from the key geometrical parameters such as conductor width ($W$), number of turns ($N$), and inductor shape, the use of patterned ground shields (*PSG's*) and multi-layer structures are other inductors design techniques. Since the targeted operating frequencies in this thesis are above 5 GHz, the prime objective is to design inductors with high quality factors (i.e. $Q > 5$) at those frequencies, while simultaneously maximizing their self-resonant frequencies ($f_{RES}$).

Designing inductors for RF applications is a multi-dimensional problem, which involves many inter-related factors. The first thing that should be considered is the frequency range of interest. As the frequency of operation increases, the required inductance for matching and resonant tanks decreases. For instance, at 100 MHz, a typical tank inductance value would be in the order of 100 nH, whereas the required tank inductance would be around 1 nH at 10 GHz. In an extreme case where the operating frequency is in the millimeter range (e.g. 50 GHz), the required inductance would be so small that a conventional lumped inductor model would no longer be valid. Transmission lines are used instead. As the targeted frequency range in this work is 5-10 GHz, the required inductance is in the order of 0.8 to 1.5 nH, which can be easily implemented

with a simple planar structure. Hence, the multi-layer series structure often used to increase the effective inductance (e.g. [58]) is not necessary.

Circular spiral structures should be used whenever possible, as they are known to yield higher quality factors than other planar structures such as squares and polygons. However, typical IC processes do not support non-manhattan-type structures. An octagonal structure, which is considered to be a fair approximation of a circular spiral, is used to maximize the quality factor. Furthermore, symmetric structures are preferred since they provide better magnetic coupling (i.e. higher inductance for a given area) than an asymmetric spiral [50]. In addition, they provide higher quality factors when excited differentially. Although differential circuits have not been employed in this thesis, future work anticipates an increasing need of this structure.

In order to achieve high Q's through reducing the series resistances, the number of turns ($N$) should be minimized while the conductor width ($W$) should be made large. However, increasing W can have a negative effect on the self-resonant frequency, since wider metal traces translates into larger parasitic capacitances to substrate. There exists an optimum value for W in each inductor design. Both simulation and measurement data were used to select the optimum conductor width. A pseudo-electromagnetic simulator, ASITIC [50], was used for simulations. It has the capability of modeling many topologies such as symmetric polygons and transformers. Measurements were made on-chip using microwave probes, followed by deembedding of the pad parasitics. Deembedding is critical when characterizing inductors. Failing to remove the effects of the test setup would result in an underestimation of the inductances and quality factors [59]. Several structures, with metal widths ranging from 15 μm to 25 μm, were implemented and examined. From past experience, inductors with widths of less than 15 μm yielded poor performances with quality factors of around 2 to 3 at 2 GHz. Furthermore, their self-resonant frequencies were much lower than the intended operating frequencies of this work. Hence, these structures (i.e. $W < 15$ μm) are not considered. The upper limit of 25 μm is constrained by the maximum allowable width in particular fabrication

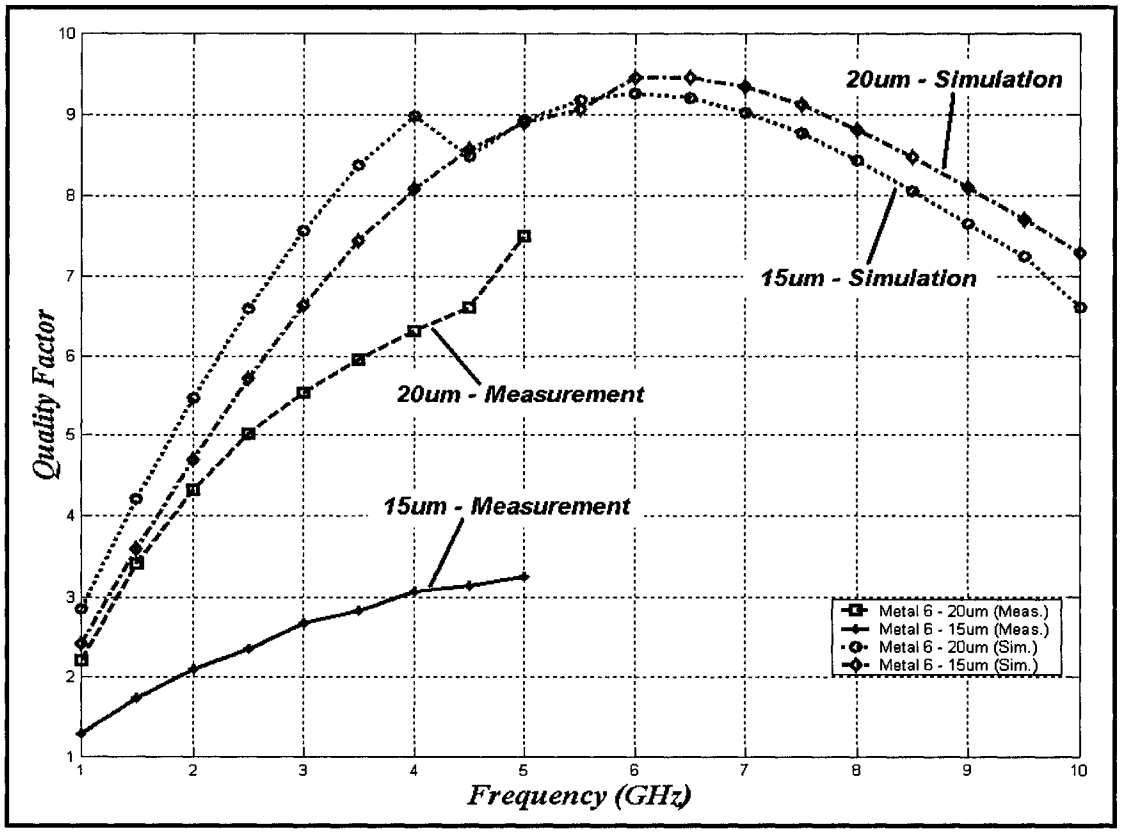


**Figure 3.3 A comparison of the quality factor of the two inductor structures with different conductor widths.**

processes. A comparison between two different conductor widths is shown in Fig. 3.3. From simulation, both structures (15 μm and 20 μm) have high quality factors of greater than 6 at 5-10 GHz, with slightly better performance for the wider conductor. From measurements, a poor performance of the 15 μm structure has been observed, which deviated considerably from the expected value. This difference is mainly due to the under-estimation of the inductor series resistance by the simulator. On the other hand, a reasonable performance has been obtained for the 20 μm structure, even though there still are substantial discrepancies between the simulated and measured data. These discrepancies are mainly attributed to the limitations of the simulator.

Apart from choosing the optimum width for an inductor, increasing the thickness of the conductor can also reduce the metal losses, as well as the skin-effect at high frequencies. Without process modifications, a thicker conductor can be implemented by stacking multiple metal layers in parallel. However, more metal stacking, using lower

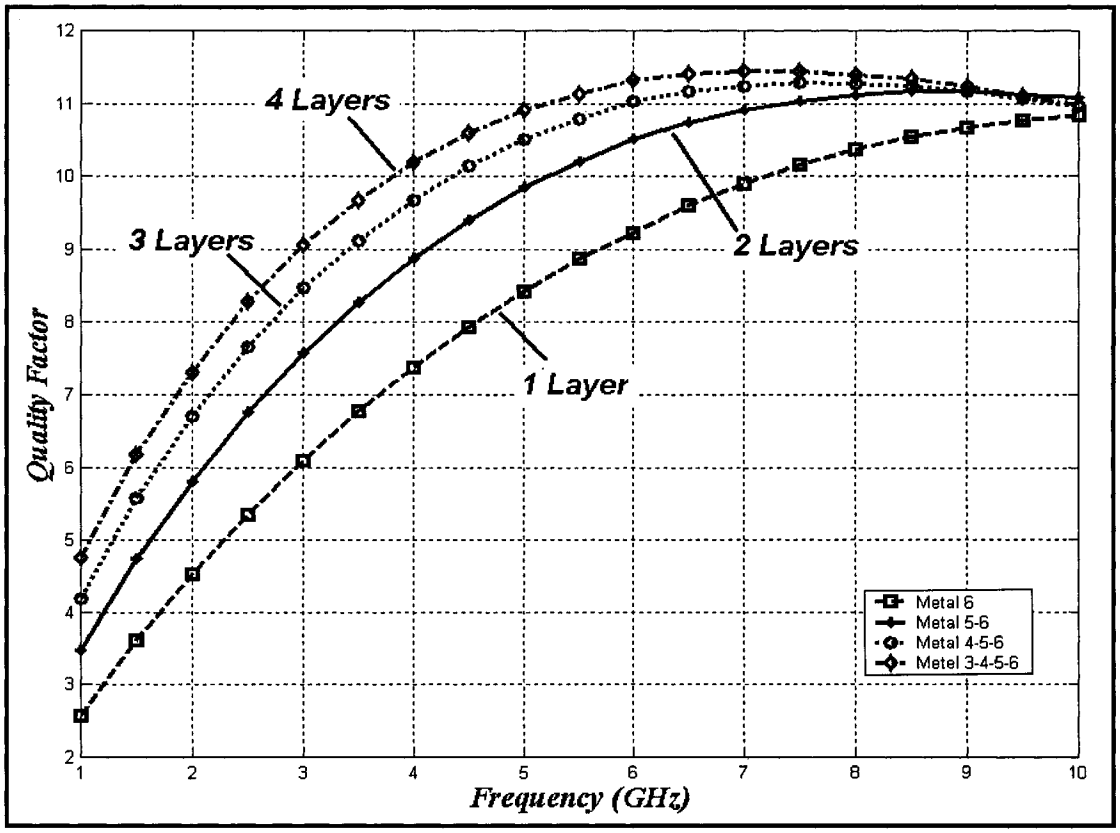


**Figure 3.4 Simulation plot of the quality factor of the multi-layer stacking inductor structures.**

metal layers (e.g. Metal-5 and Metal-4), will induce more capacitive coupling and losses to the substrate. In order to evaluate the effectiveness of multiple stacking, simulations were performed for multi-layer stacking inductor structures, as shown in Fig. 3.4. Due to the limitations of the simulator, only square inductors were simulated. The main purpose of this simulation was to determine the optimum number of metal stacking for performance enhancement. From Fig. 3.4, it can be seen that there are significant improvements in quality factor by stacking the top two metal layers compared to a single metal layer. Further increase in stacking (i.e. 3 and 4 layers) enhances the quality factor but at a reduced margin. Note that all structures have similar quality factors as the frequency is approaching 10 GHz. This is mainly due to more serious capacitive losses to the substrate as the frequency increases. Due to the uncertainties on the accuracy of the simulator, a more conservative approach was used when designing inductors. Hence, only the 2-layer and 3-layer structures were used in this work.

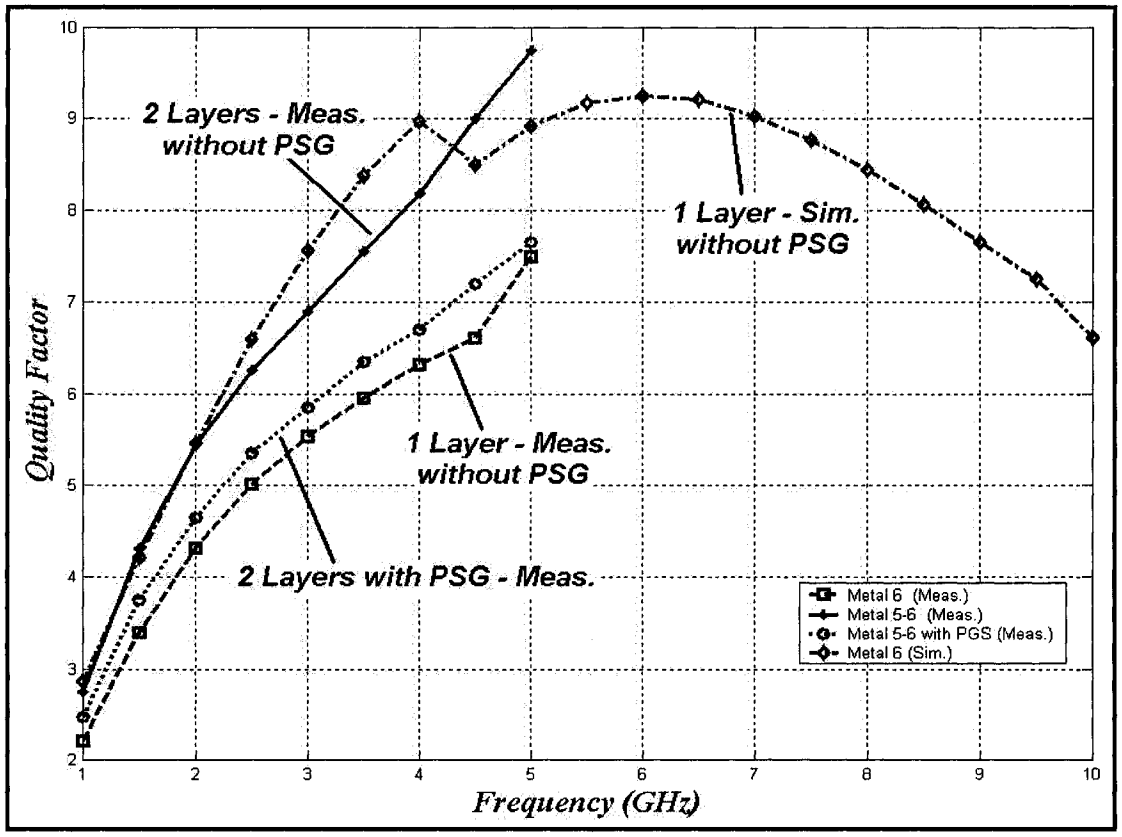


**Figure 3.5 A comparison on the quality factor of the inductors with or without patterned ground shield.**

Ideally, the use of patterned ground shields (*PSG's*) would reduce the Eddy current losses, and improve the quality factor. However, they could significantly reduce the self-resonant frequencies of the inductors due to the additional capacitive parasitics they introduced. By attempting to push the frequency limit in this work, inductors are operating much closer to their self-resonant frequencies. Hence, patterned ground shields were not inserted between the spiral inductor and the silicon substrate in order to avoid self-resonance degradation. A comparison plot showing the impact of the patterned ground shields on the quality factors of inductors is illustrated in Fig. 3.5. The measured data support the idea of not using patterned ground shields, since performance degradation has been observed for the 2-layer structures when PSG's were used. Once again, such large discrepancies are attributed to the inability to properly model the effects of the PSG's by the simulator.

The impacts of different parameters on the quality factors, the inductances, and the

self-resonant frequencies of integrated inductors are summarized in Table 3.1. Note that the first four parameters (e.g. thickness and resistivity) are governed by the fabrication process, hence the designer does not have much control over them, considering our main goal of implementing RFIC's in standard CMOS processes without any modifications. Other parameters in Table 3.1 are controllable. As shown, with the main objective of maximizing the quality factor while pushing the self-resonant frequencies as high as possible, inductors are designed considering many various trade-offs.

| Parameter | Conditions | $Q_{max}$ | L | $f_{RES}$ |
|---|---|---|---|---|
| Conductor Thickness | ↑ | ↑ | — | — |
| Conductor Sheet Resistance | ↑ | ↓ | — | — |
| Substrate Resistivity | ↑ | ↑ | — | ↑ |
| Insulator Thickness | ↑ | ↑ | — | ↑ |
| Number of Turns | ↑ | ↓ | ↑ | ↓ |
| Conductor Width | ↑ | ↑ | ↓ | ↓ |
| Multi-Layer in Series | ↑ | ↓ | ↑ | ↓ |
| Multi-Layer in Shunt | ↑ | ↑ | — | ↓ |
| Patterned Ground Shields | Yes | Varies | — | ↓ |

↑: Increase; ↓: Decrease; —: Almost constant;

**Table 3.1 - Integrated inductor performance trends.**

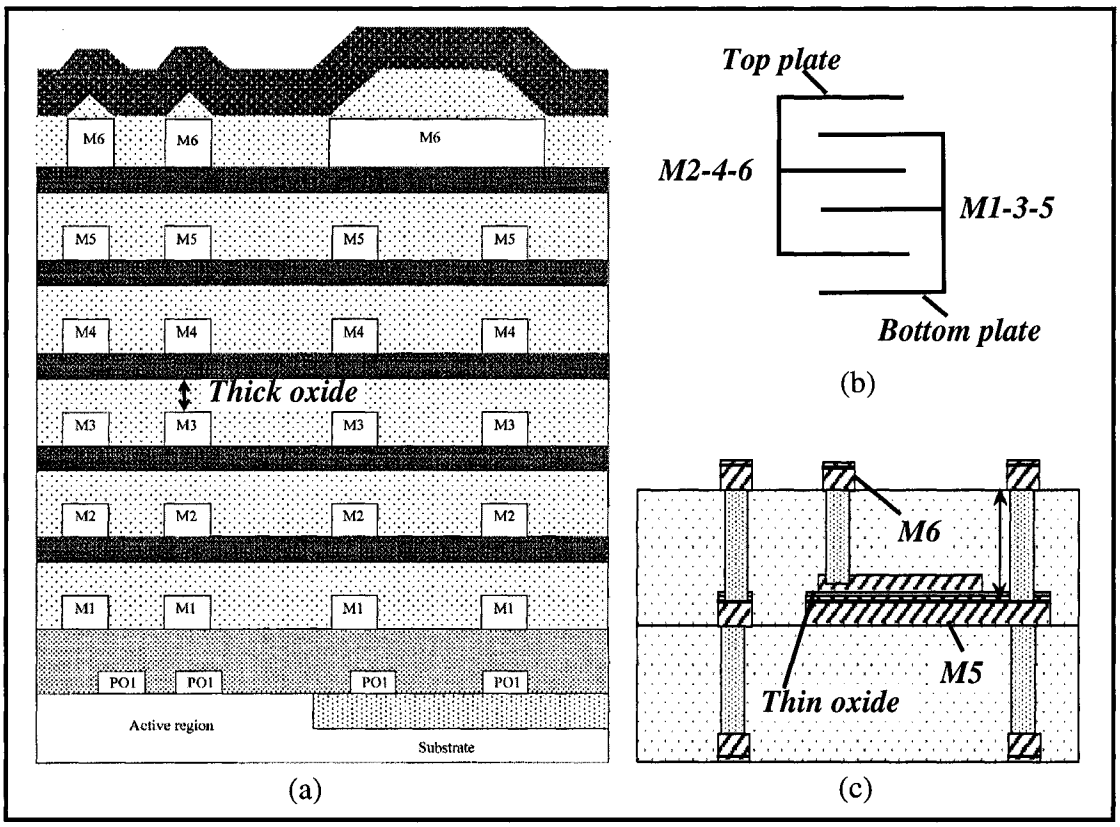


**Figure 3.6 (a) The cross section of a typical CMOS process. (b) Multi-layer capacitor structure. (c) The cross section of a special MIM structure.**

## 3.2.3 - Integrated Capacitors Design

In general, low voltage coefficients, good capacitor matching, precision capacitance control, and small parasitic capacitances, along with high reliability and low defect densities are essential requirements for high performance RF circuits. Integrated capacitors are realized as either MOS capacitors, poly-poly capacitors, poly-diffusion capacitors, or metal-insulator-metal (*MIM*) capacitors. For RF applications, MIM capacitors are clearly the preferred choice, since they result in the lowest losses at high frequencies. Although standard metal interconnects can be used to implement MIM capacitors, they have several limitations. The large process variation in the oxide thickness across the wafer results in a big uncertainty in the capacitance. Furthermore, the thick oxide separating the metal layers results in a low capacitance density per unit area (e.g. 0.05 fF/$\mu m^2$). The cross section of a typical CMOS process is shown in Fig. 3.6(a).

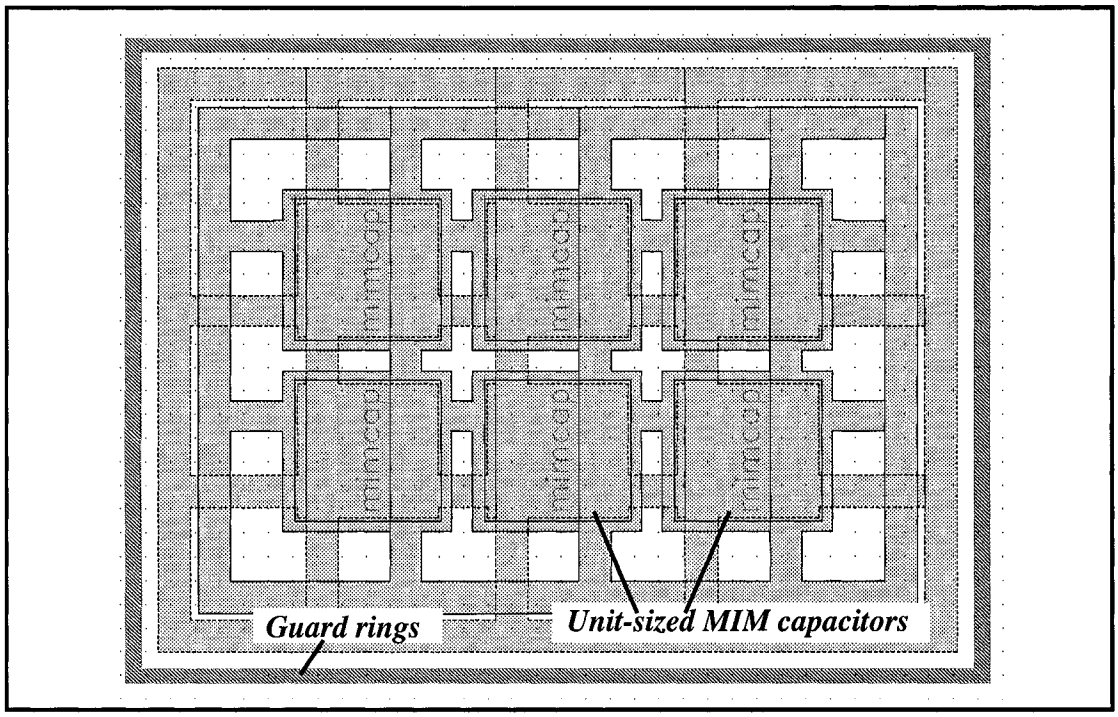


**Figure 3.7 Example layout of a MIM capacitor.**

In order to increase the capacitance density, several metal layers can be connected in parallel, as illustrated in Fig. 3.6(b). For instance, metal 2-4-6 would form one capacitor plate, whereas metal 1-3-5 would form the other plate. In order to avoid serious substrate coupling and losses, only the metal layers which are far from the substrate should be used. In other words, metal-1 and metal-2 should not be used for the multi-layer capacitor structures since they reside close to the substrate.

A special MIM capacitor which is implemented with a well-controlled thin oxide is preferred and is commonly available in a standard CMOS process with RF options. This structure can have high capacitance density per unit area due to the thin dielectric between the metal layers. For instance, in a 0.18 μm CMOS process, it can have a density of 1 fF/μm$^2$, which is at least five times higher than the standard multi-layer structure. The cross section of this MIM capacitor structure is shown in Fig. 3.6(c).

Although MIM capacitors exhibit low losses, careful layout is required to ensure their high quality performance at RF. A large capacitor is constructed by combining unit-sized capacitors in parallel in order to improve matching accuracy. Furthermore, metal interconnects between each capacitor cell are made short and wide to avoid Q

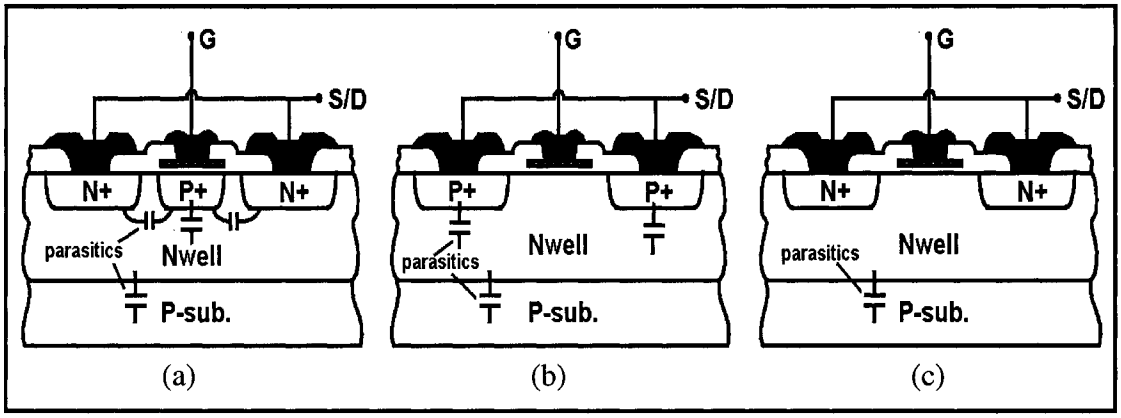


**Figure 3.8 The cross-sectional views of (a) PN-junction, (b) PMOS, and (c) NMOS over Nwell varactors.**

degradation and resistive losses. Guard rings are used to protect the capacitor structure from coupling through the substrate of nearby signals. An example layout of a MIM capacitor is shown in Fig. 3.7.

### 3.2.4 - Integrated Varactors Design

Varactors, or variable capacitors, are commonly used in integrated voltage-controlled oscillator (*VCO*) designs (e.g. [23], [60]) for tuning the center frequencies of the LC resonant tanks. In this thesis, varactors are also used in one of the LNA designs to achieve frequency tuning capability.

PN-junctions, PMOS capacitors, NMOS over Nwell varactor structures, etc. are the common ways to implement a varactor. The cross sections of these structures are illustrated in Fig. 3.8. The simplest varactor structure is constructed as a PN junction, as shown in Fig. 3.8(a). It consists of a P+ and an N+ region residing in an Nwell. The depletion region is formed between the P+ region and the Nwell. The typical tuning range of a PN-junction is around ±10 %, and it varies with the doping profile. This small tuning range is limited by the parasitic capacitances across the PN junction. The PMOS varactor, shown in Fig. 3.8(b), utilities the gate capacitance of a PMOS transistor. It has a wider tuning range than the PN-junction varactor due to the reduced parasitics. However, the tuning range is now limited by the drain and source parasitic capacitances. The NMOS over Nwell structure, commonly known as the accumulation-mode varactor, replaces the drain and the source of a PMOS varactor with N+ contacts. Due to the removal of the

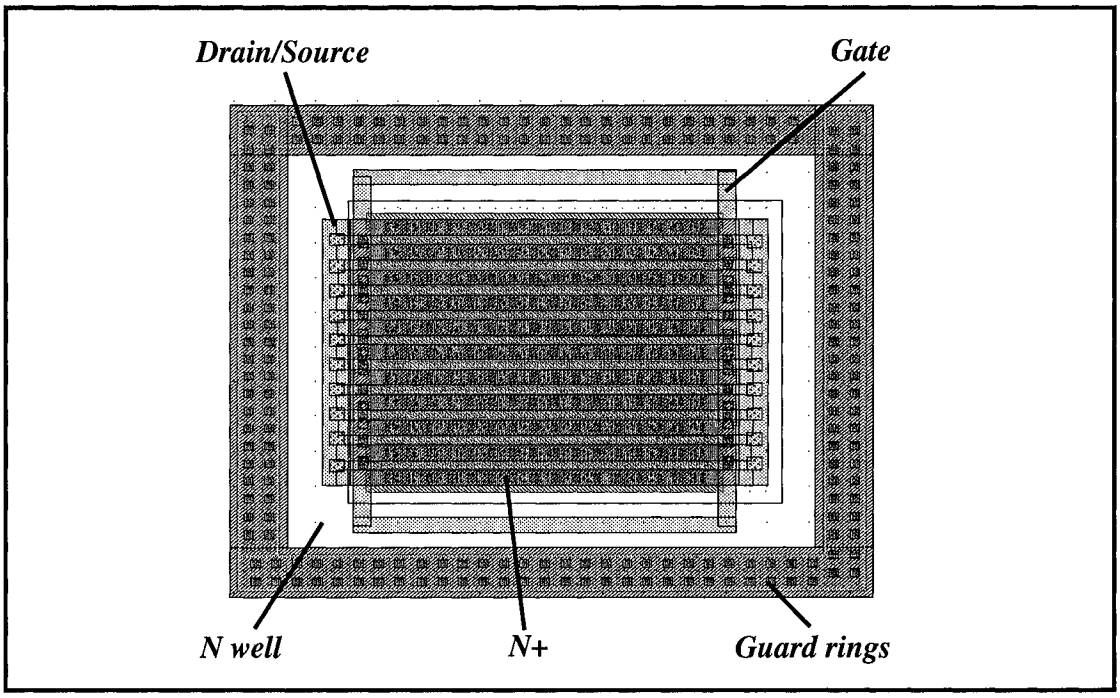


**Figure 3.9 The layout of the accumulation-mode varactor.**

parasitic drain and source capacitances, this structure is capable of achieving a tuning range of ±30 %. The accumulation-mode varactors have been reported (e.g. [61], [62]) to provide wider tuning ranges and better quality factors in comparison to the two other varactor structures, while providing the same order of magnitude of capacitance. Hence, the accumulation-mode varactors are used for implementing frequency tuning in this thesis.

To achieve frequency tuning, varactors are usually connected to the LC resonant tank of the circuit. In order to avoid Q degradation of the tank, the quality factor of the varactor should be as high as possible. This can be done by layout optimization. The layout of the accumulation-mode varactor is shown in Fig. 3.9. Minimum channel length is used to reduce the parasitic series resistances of the varactor. To minimize the effect of the gate resistance noise, both ends of the gate fingers are connected together, as described in section 2.1.4. Furthermore, guard rings are used to improve the isolation of signals and to reduce noise coupling. In order to ensure a wide tuning range, layout dependent overlap capacitances should be minimized.

## 3.3 - MEMS for RF Applications

Low loss and wide tuning range varactors are often required to ensure adequate frequency tunings in LNA and VCO designs, in order to compensate for process and temperature induced variations in the passives, as well as to tune for different center frequency bands. Even though a wealth of research efforts have been invested on improving the quality factors of integrated passives, their performances are often inadequate for today's modern wireless applications. The need for high quality passive components for RFIC's has motivated many research groups to seek other implementation methods such as using Micro-Electro Mechanical Systems (*MEMS*).

Recent developments in micromachining suggest that hybrid technologies, where micromachined passive devices and integrated electronics reside on a single chip, will be widely adopted in the future. Commercial products such as pressure sensors in air-bag systems, which are based on a BiCMOS technology integrated with a surface polysilicon process, are readily available nowadays [63]. Such a technology can realize not only integrated mechanical resonant devices, but also integrated electrical resonant passives which are tunable by electro-mechanical means.

Passive devices have been realized in various MEMS technologies (e.g [64] - [66]), exhibiting high quality factors (i.e. $Q > 10$) up to 2 GHz. In particular, MEMS-based switches and variable capacitors seem to be the most promising structures among the RF passive devices. Some of the advantages include a wide tuning range for the varactors, and low harmonic distortion for both varactors and switches. In the following section, the design and characterization of several MEMS-based varactor structures in a Multi-User MEMS Process (MUMPs) technology, together with measurement results, are presented.

### 3.3.1 - The Multi-User MEMS Processes (MUMPs)

As one of the main purposes of this work is to use cost effective and commercially available standard processes to design RF circuits, a widely adopted polysilicon surface micromachining process, known as MUMPs, is used in this thesis. Despite the superior electrical properties of aluminum-based processes (e.g. [66]), polysilicon is often chosen as the structural material for MEMS-based RF passives, due to its good mechanical

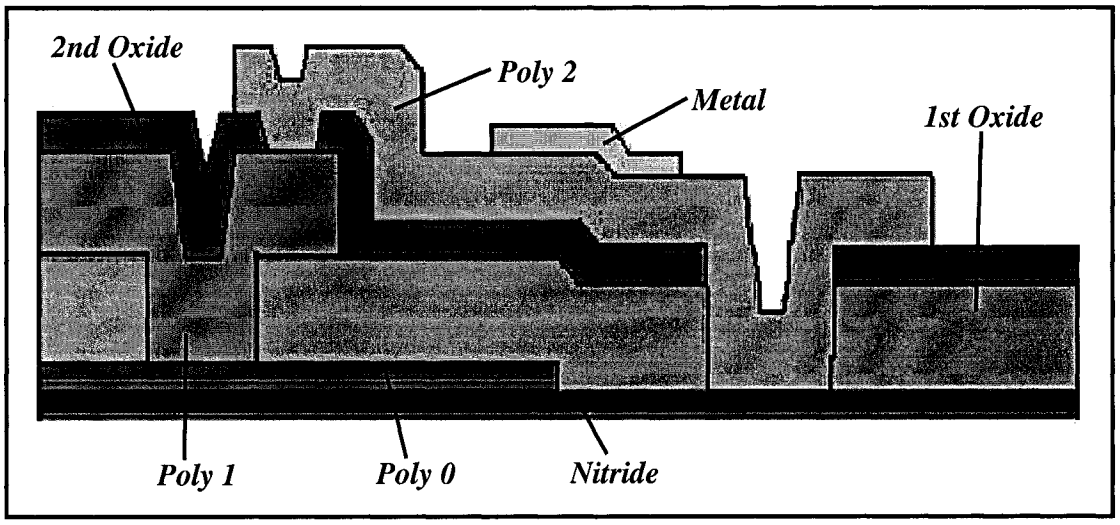


**Figure 3.10 The cross-sectional view of the 7-layers MUMPs process [68].**

properties [67].

The MUMPs process [68] has the general features of a standard surface micromachining process. Polysilicon is used as the structural layer, deposited oxide is used as the sacrificial layer, and silicon nitride is used as electrical isolation between the polysilicon and the substrate. The cross section of the MUMPs process used is shown in Fig. 3.10. The process features three layers of polysilicon (poly 0, poly 1, and poly 2) and one layer of gold, where gold can only be deposited on the top polysilicon layer (i.e. poly 2). The thicknesses and sheet resistances of the polysilicon and gold layers, as well as of the oxide layers, are summarized in Table 3.2. The MUMPs devices, constructed

| | Thickness | Sheet Resistance |
|---|---|---|
| Poly 0 | 0.5 μm | 30 Ω/sq |
| 1st Oxide | 2.0 μm | - |
| Poly 1 | 2.0 μm | 10 Ω/sq |
| 2nd Oxide | 0.75 μm | - |
| Poly 2 | 1.5 μm | 20 Ω/sq |
| Metal (Gold) | 0.5 μm | 0.06 Ω/sq |

**Table 3.2 - Summary of the MUMPs process parameters.**

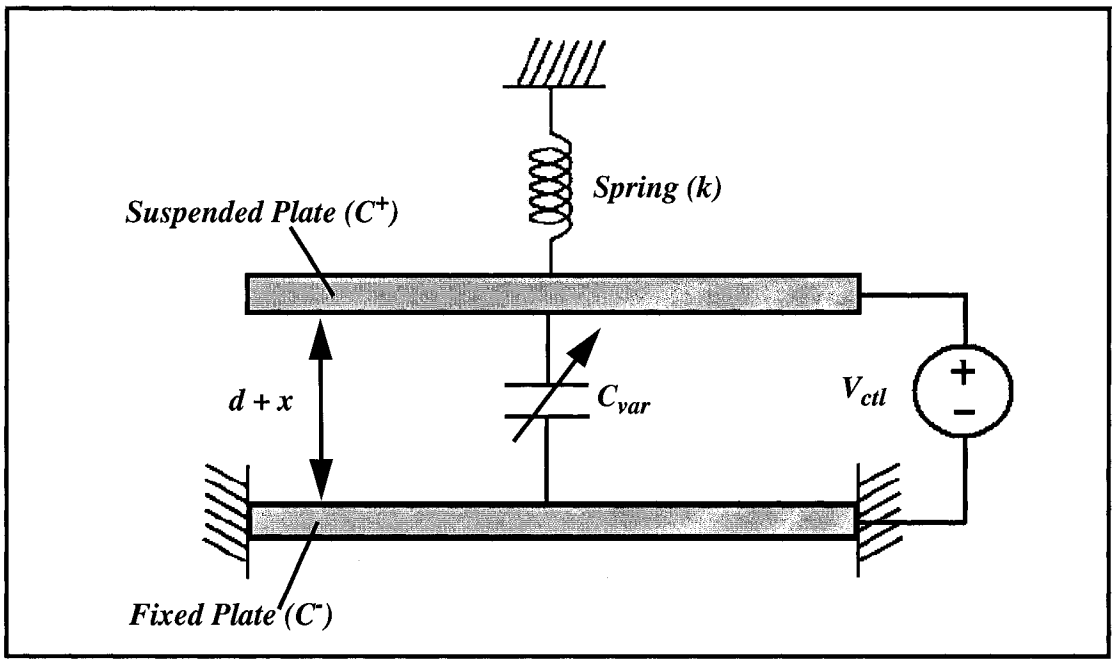


**Figure 3.11 The conceptual model of a MEMS-based tunable parallel plate capacitor.**

using the polysilicon layers, are released by using a hydrogen fluoride (*HF*) sacrificial oxide layer etch and a supercritical carbon dioxide ($CO_2$) drying process. The supercritical drying process is used to ensure satisfactory device yield.

## 3.3.2 - MEMS-Based Variable Capacitors

**(a) Basic Principle of Operation** - The capacitance of a typical integrated varactor in an IC process is changed by varying its depletion region, as described in section 3.2.4. MEMS-based variable capacitors operate in a totally different fashion. The conceptual model of a MEMS-based tunable capacitor is shown in Fig. 3.11. The electro-mechanical variable capacitor consists of two parallel plates. The top plate ($C^+$) of the capacitor is suspended by a spring with a spring constant ($k$), whereas the bottom plate ($C^-$) of the capacitor is mechanically fixed. When a control voltage ($V_{ctl}$) is applied across the two capacitor plates, the suspended plate (i.e. $C^+$) is attracted towards the fixed plate (i.e. $C^-$) due to the resultant electrostatic force. The suspended plate continues to move towards to the fixed plate until an equilibrium between the electrostatic force and the spring force is reached. The equilibrium between the forces can be expressed as follows:

$$kx = \frac{1}{2}\frac{dC_{var}}{dx}V_{ctl}^2 = -\frac{1}{2}\frac{\varepsilon_d A V_{ctl}^2}{(d+x)^2}, \tag{3.6}$$

where $C_{var}$ is the variable capacitance, $\varepsilon_d = \varepsilon_{air}\varepsilon_o$ is the dielectric constant of air, $A$ is the area of the capacitor plates, $d$ is the distance of separation between the two capacitor plates when the spring is in its relaxed state, and $x$ is the vertical displacement at a certain control voltage ($V_{ctl}$) condition.

By solving equation 3.6, it can be shown that the desired capacitance is a function of the control voltage and can be expressed as follows [65]:

$$C_{var}(V_{ctl}) = \frac{\varepsilon_d A}{d + x(V_{ctl})}, \tag{3.7}$$

where,

$$x(V_{ctl}) = (p(V_{ctl}) + q(V_{ctl})) - \frac{2d}{3}, \tag{3.8}$$

$$p(V_{ctl}) = \left\{ w(V_{ctl}) + \sqrt{u^3 + w^2(V_{ctl})} \right\}^{1/3}, \tag{3.9}$$

$$q(V_{ctl}) = \left\{ w(V_{ctl}) - \sqrt{u^3 + w^2(V_{ctl})} \right\}^{1/3}, \tag{3.10}$$

$$u = \frac{d^2}{9}, \tag{3.11}$$

$$w(V_{ctl}) = \frac{d^3}{27} - \frac{\varepsilon_d A V_{ctl}}{4k}. \tag{3.12}$$

It should be noticed that an equilibrium between the electrostatic and the spring forces only exists for the vertical displacements of $0 \geq x \geq -d/3$. The electrostatic force is greater than the spring force when $x < -d/3$, which results in contact between the

suspended and fixed plates. The limitation to reduce the spacing beyond 1/3 of the initial separation ($d$) of the two capacitor plates is known as the pull-in effect. This phenomenon has set a theoretical limit of 50% on the tuning range with a maximum capacitance of $3C_{var}/2$, since the suspended plate ($C^+$) acts simultaneously as the capacitance and the actuation electrode.

**(b) Variable Capacitor Design** - The pull-in effect imposes a theoretical limit of 50% on the tuning range of a simple parallel-plate capacitor. This is due to the equilibrium of the spring and electrostatic forces between the two capacitor plates. In order to exceed this theoretical limit, it is required to isolate the mechanisms of capacitance tuning and of actuation. This can be done by separating the capacitance and actuation electrodes. Furthermore, higher tuning range can be achieved by having different spacings between the capacitance tuning and actuation electrodes.

In the MUMPs process used, three polysilicon layers (poly 0 - poly 2) are employed for the structural material of the capacitor plates. A layer of gold can be deposited onto the top polysilicon layer in order to reduce the overall series resistance of the structure. Since the spacings (i.e. after HF release) between each polysilicon layer are different as shown in Table 3.2, different capacitance tuning characteristics can be achieved.

Fig. 3.12 shows a simplified cross-sectional, top, and SEM views of a conventional tunable capacitor structure (Type-1). Note that the suspended plate acts as both the capacitance tuning and actuation electrode. Hence, the tuning range of this structure is limited by the pull-in effect. Furthermore, in practice, the tuning range would be smaller than the theoretical limit since a parasitic capacitance ($C_{fix}$) exists between the fixed plate ($C^-$) and the substrate. In order to minimize $C_{fix}$, poly 1 is used as the fixed plate instead of poly 0, since poly 1 is further away from the substrate (i.e has less parasitics).

By assuming the area ($A$) of the suspended plate being equal to the fixed plate with spacings of $d_1 = 0.75\ \mu m$ and $d_2 = 2.0\ \mu m$, the parasitic capacitance of the fixed plate ($C_{fix}$) is estimated as follows:

$$C_{fix} = \frac{\varepsilon_d A}{d_2} = \frac{3}{8} \cdot \frac{\varepsilon_d A}{d_1} = \frac{3}{8} C_{var}. \qquad (3.13)$$

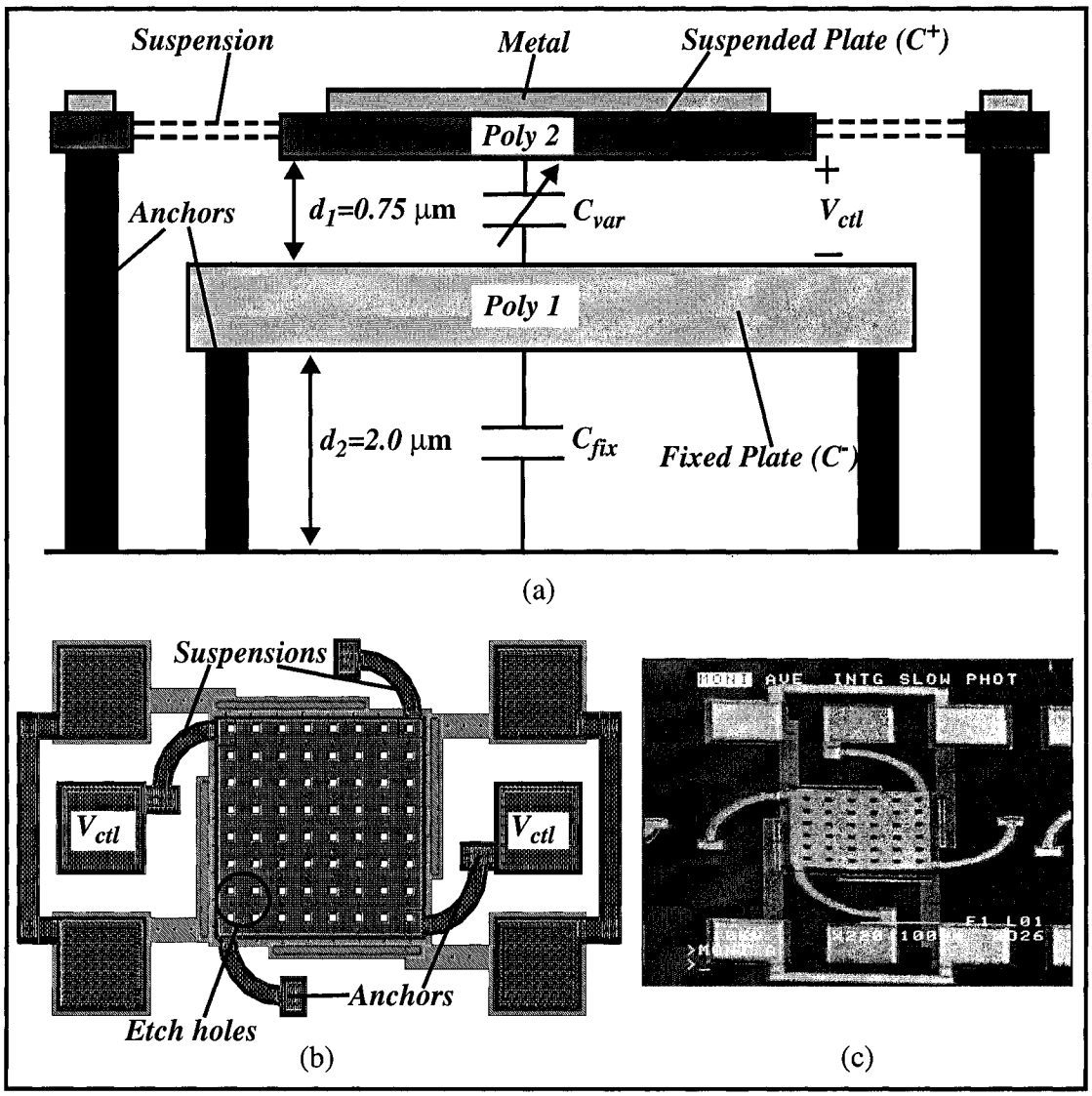


**Figure 3.12 The (a) cross-sectional, (b) top, and (c) SEM views of a tunable capacitor (Type 1).**

The tuning range of this type of capacitors is defined as:

$$Tuning\ range = \frac{Maximum\ capacitance}{Steady\ state\ capacitance\ under\ zero\ bias}. \quad (3.14)$$

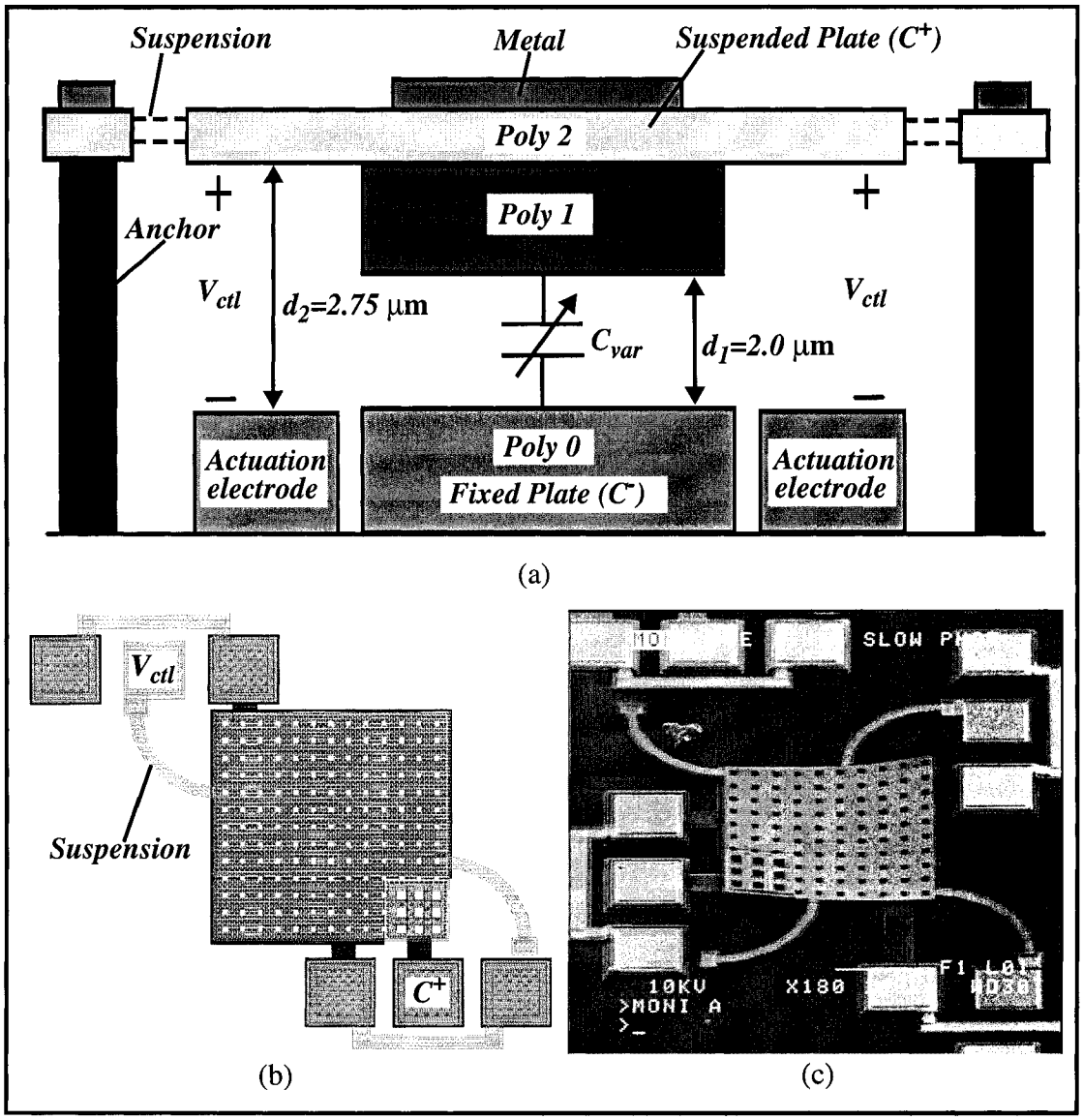


**Figure 3.13 The (a) cross-sectional, (b) top, and (c) SEM views of a tunable capacitor (Type 2).**

When incorporating the expression for the parasitics (i.e. equation 3.13), the tuning range becomes:

$$Tuning\ range = \frac{C_{fix} + \frac{3}{2}C_{var}}{C_{fix} + C_{var}} = \frac{\frac{3}{8}C_{var} + \frac{3}{2}C_{var}}{\frac{3}{8}C_{var} + C_{var}} = 1.36. \qquad (3.15)$$

Hence, the theoretical tuning limit of the conventional structure is reduced from 50%

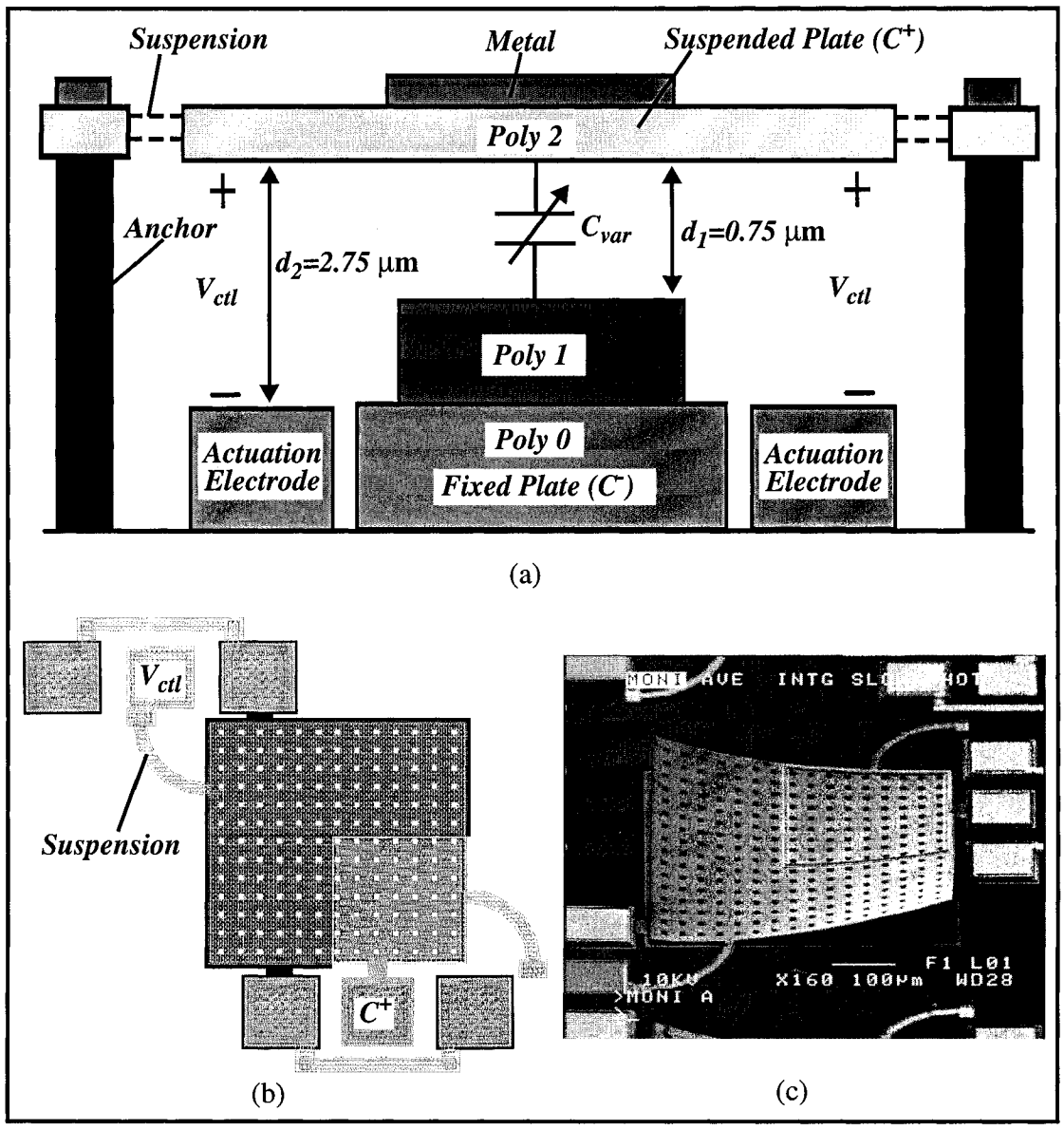


**Figure 3.14 The (a) cross-sectional, (b) top, and (c) SEM views of a tunable capacitor (Type 3).**

to 36% when including the parasitics.

In order to exceed the tuning limit of 50%, two new structures have been implemented in this MUMPs process. Both structures have the characteristics of separating the actuation and capacitance tuning electrodes, as well as having different spacings between the capacitor plates. Fig. 3.13 shows the cross-sectional, top, and SEM views of such a tunable capacitor structure (Type-2).

In this structure, the variable capacitor is formed between the suspended and fixed

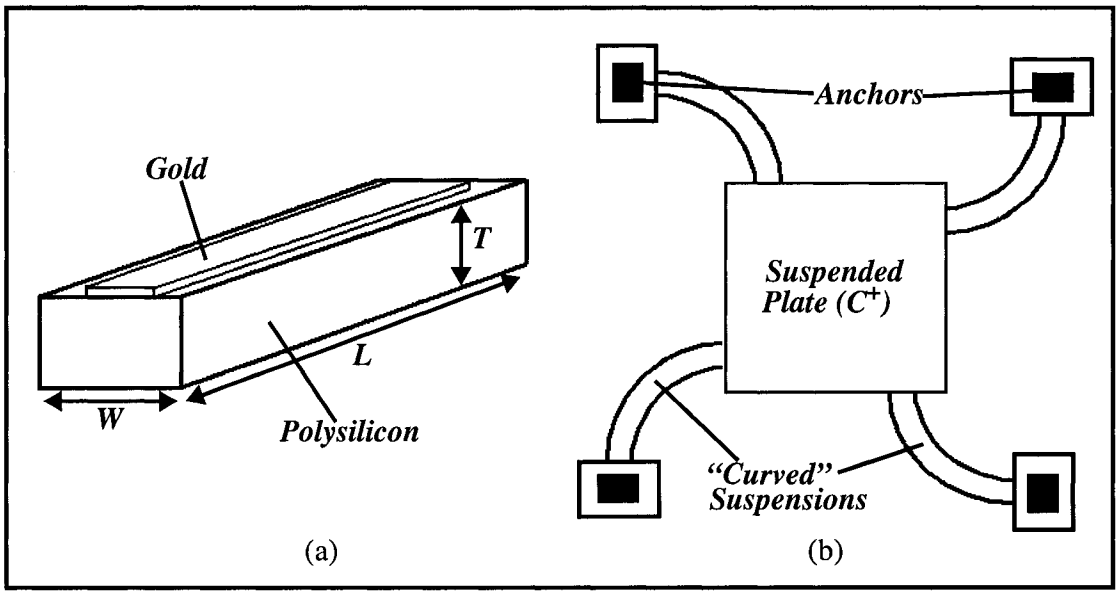


**Figure 3.15 (a) The schematic of the suspension. (b) The top view of the tunable capacitor.**

plates with a spacing $d_1$ of 2 μm. The capacitance is tuned by the actuation electrodes with a spacing $d_2$ to the suspended plate of 2.75 μm. Limited by the pull-in effect, the spacings at the actuation electrodes can be reduced by 1/3. Hence, they can only be adjusted from $d_2$ to 2/3 of $d_2$. Since the actuation and capacitance tuning electrodes are separated, the capacitance tuning is not limited by its pull-in effect (i.e $d_1/3$) but rather restricted by the actuation electrodes (i.e. $d_2/3$). As a result, a much greater tuning range of higher than 50% can be achieved. Based on equation 3.14, the tuning range of this structure can be expressed in terms of the spacings as follows:

$$Tuning\ range = \frac{1/(d_1 - d_2/3)}{1/d_1} = \frac{3d_1}{3d_1 - d_2};\quad \left(d_1 > \frac{d_2}{3}\right) \tag{3.16}$$

where $d_1$ is the spacing at the capacitance tuning electrode, and $d_2$ is the spacing at the actuation electrode. For the spacings of $d_1 = 2$ μm and $d_2 = 2.75$ μm, the theoretical limit on the tuning range of the type-2 capacitor structure is about 84.6%, exceeding the conventional limit of 50%.

The idea of the type-2 capacitor structure can further be exploited to increase its tuning range. Fig. 3.14 shows the cross-sectional, top, and SEM views of such a tunable

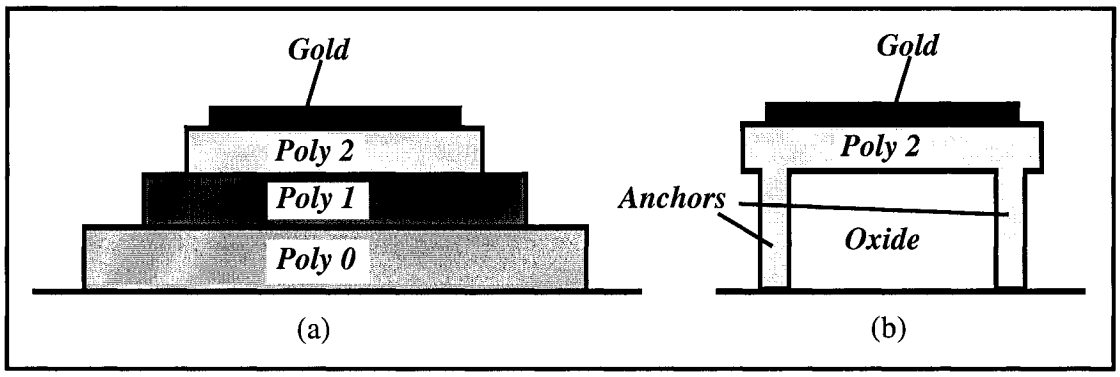


**Figure 3.16 The cross-sectional views of the (a) conventional and (b) low parasitic pad structures.**

capacitor structure (Type-3). The main difference between the type-2 and type-3 structure is the spacing at the capacitance tuning electrode (i.e. $d_1$). In the type-3 structure, the spacing $d_1$ is much smaller than the one in the type-2 structure. Furthermore, the spacing $d_1$ is smaller than 1/3 of the actuation spacing $d_2$ ($d_2/3$ is the limit imposed by the pull-in effect). This allows for the suspended plate to move much closer to the fixed plate, resulting in a considerably large increase in capacitance. Theoretically, this structure has an infinite tuning range and is summarized as follows:

$$Tuning\ range \Rightarrow \infty; \quad \left(d_1 < \frac{d_2}{3}\right) \quad . \tag{3.17}$$

With the spacings of $d_1 = 0.75\ \mu m$ and $d_2 = 2.75\ \mu m$, the type-3 structure satisfies the condition in equation 3.17 and ideally has an infinite tuning range.

**(c) Suspension Design** - Suspensions are used to support the top plate of the variable capacitor. The spring constant ($k$) of a suspension can be expressed as:

$$k = \frac{E_{poly} W T^3}{L^3}, \tag{3.18}$$

where $W$, $T$, $L$ are the width, thickness, and length of the suspension (Fig. 3.15(a)), respectively, and $E_{poly} = 160\ GPa$, is the Young's modulus of polysilicon. Gold is deposited on top of the suspensions in order to minimize the parasitic series resistances. The deposition of gold on the suspensions is not expected to have significant effects on

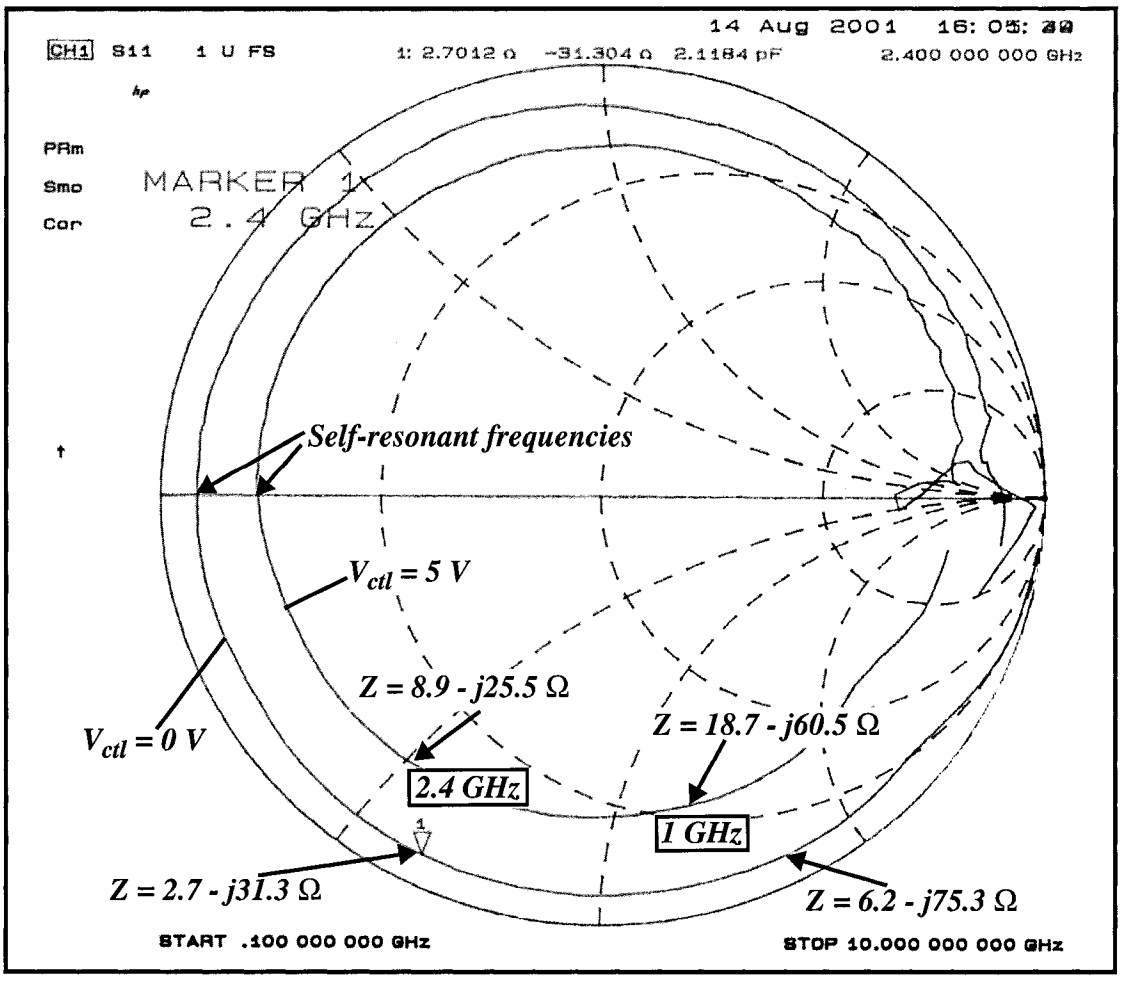


**Figure 3.17 The measured $S_{11}$ of the type-1 tunable capacitor.**

the overall spring constant since the thicknesses and widths of the gold traces are much smaller than the polysilicon structures.

The suspensions are designed with the objective of reducing the residual stresses. Thermal stresses develop since the suspensions consist of layers of polysilicon and gold, which have different thermal expansion coefficients. This results in warping in the suspended plates. "Curved" suspensions, shown in Fig. 3.15(b), are used in all structures, as an attempt to absorb some of the stresses by allowing horizontal rotational movement in the top plate.

**(d) Pad Design** - The parasitic capacitances of the pads have a major impact on the performance of the test structures, especially at RF. In traditional IC processes, only the top metal layer is used for RF pad structures in order to minimize parasitics to the

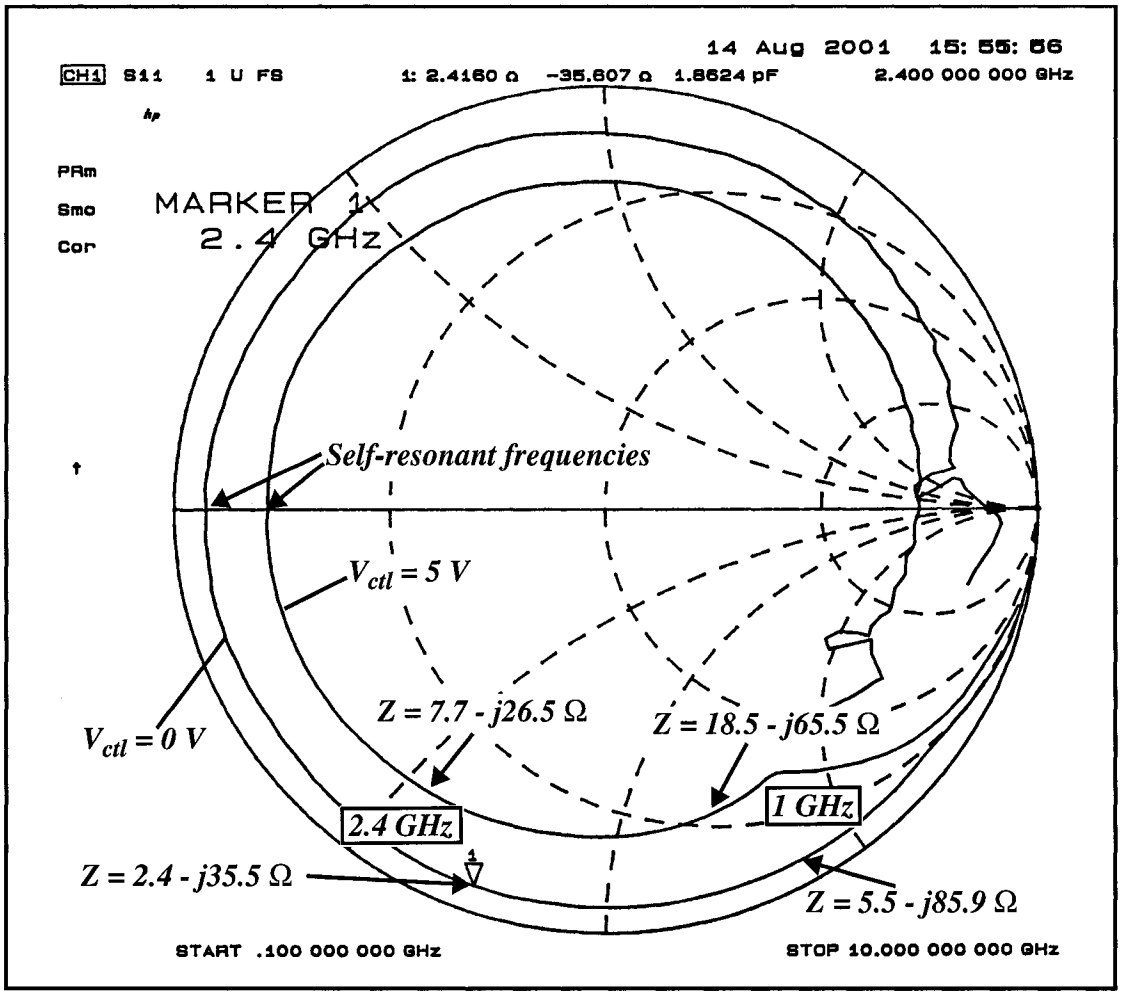


**Figure 3.18 The measured $S_{11}$ of the type-3 tunable capacitor.**

substrate. A similar approach has been adopted in this MUMPs process: poly 2 and gold layers are used to implement the pad structures. The cross-sectional view of the low parasitic pad structure as well as the conventional one are shown in Fig. 3.16.

**(e) Measurement Results** - In a traditional IC process, deembedding is essential to remove the effects of the test setup parasitics (e.g. pad parasitics) when characterizing devices. However, it is not necessary to do deembedding in this MUMPs process, since the test structures, including the test setup, are all to be integrated onto another substrate, by using techniques such as flip-chip and wire bonding. Hence, all the test setup parasitics become part of the test structure.

Several test structures were implemented and characterized in this work. The main objective was to investigate the RF performances of the test structures, in terms of their

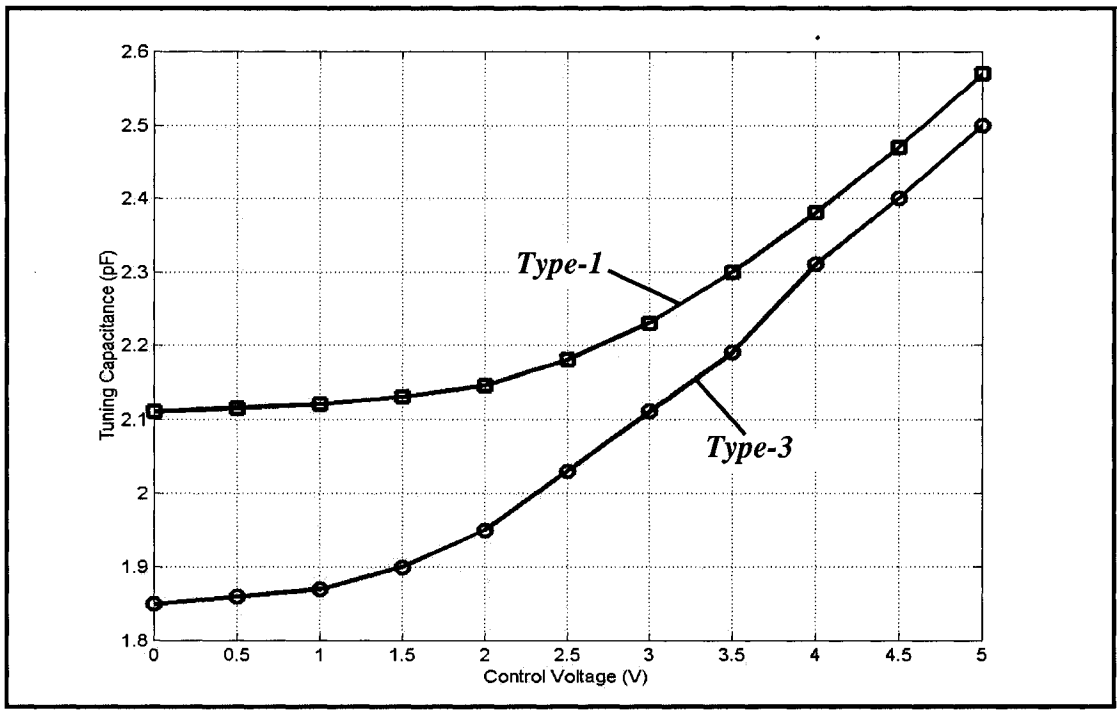


**Figure 3.19 Tuning characteristics of type-1 and type-3 micromachined tunable capacitors.**

quality factors and tunability. Fig. 3.17 shows the measured results of the type-1 tunable capacitor structure, plotted on a smith chart. The capacitor, in the initial state (i.e $V_{crt} = 0\ V$), has a quality factor of 11.6 and 12.1 at 2.4 GHz and 1 GHz, respectively. The self-resonant frequency is about 4 GHz. When a zero bias voltage is applied, the measured capacitance is 2.12 pF. The measured capacitance is about 2.57 pF when $V_{crt} = 5$ V is applied. Hence, the tuning range of the type-1 micromachined variable capacitor is 1.21:1 or 21.3%, which is smaller than the theoretical limit of 50% in an ideal case, or 36% when incorporating pad parasitics. Furthermore, the quality factors reduce to about 3 when set to the maximum tuning capacitance at both 2.4 GHz and 1 GHz.

Fig. 3.18 shows the measured $S_{11}$ of the type-3 tunable capacitor structure. The capacitor has a quality factor of 14.8 and 15.6 at 2.4 GHz and 1 GHz, respectively, at zero bias voltage (i.e $V_{crt} = 0\ V$). The self-resonant frequency is about 4 GHz. The measured capacitance is 1.85 pF at the initial state. When a control voltage of 5 V is applied, the measured capacitance is 2.50 pF. Hence, the tuning range of this structure is about 1.35:1 or 35.1%. In order to avoid break down of the polysilicon structures at high

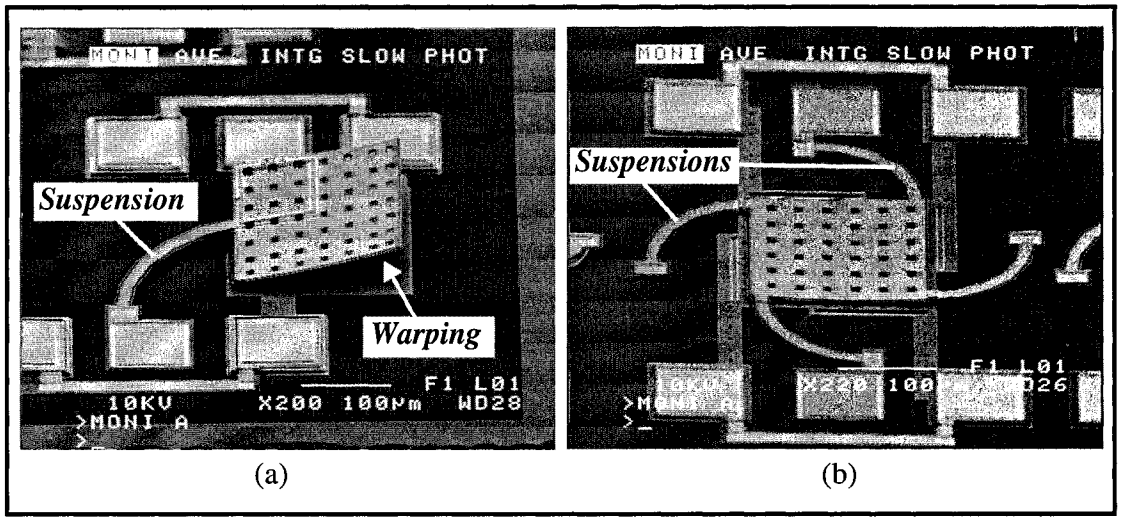


**Figure 3.20 The effects of warping due to residual stresses in MEMS-based tunable capacitors - a) high stress and b) low stress.**

voltages, the control voltage is limited to 5 V in all measurements. Similar to the case of the type-1 capacitor structure, the quality factors degrade significantly to 4.7 and 3.5 at 2.4 GHz and 1 GHz, respectively, at the maximum tuning capacitance value. The tuning characteristics of both type-1 and type-3 tunable capacitor structures are summarized in Fig. 3.19.

Due to some layout errors in the type-2 tunable capacitor, measured results have shown that the structure is not tunable. These layout errors caused the suspended plate not to be exposed by the HF release, resulting in a non-movable structure.

### 3.3.3 - Limitations of the RF MEMS Varactors Presented

(a) Residual Stress - As can be seen from the measured results, the tuning ranges of all the capacitor structures deviate significantly from the theoretical limits. This is mainly caused by residual stresses in the MEMS structures. Residual stresses, caused by the difference in the thermal expansion of materials in the polysilicon and metal layers, result in warping in the capacitor plates, which effectively affect the spacings between the capacitor plates (i.e. $d_1$ and $d_2$), and hence the tuning ranges. The degrees of warping due to residual stresses vary and depend on the physical structures. Fig. 3.20 illustrates the effects of warping for different number of suspensions. With only one suspension, shown in Fig. 3.20(a), the effect of the residual stress remains high. Hence, the spacing between

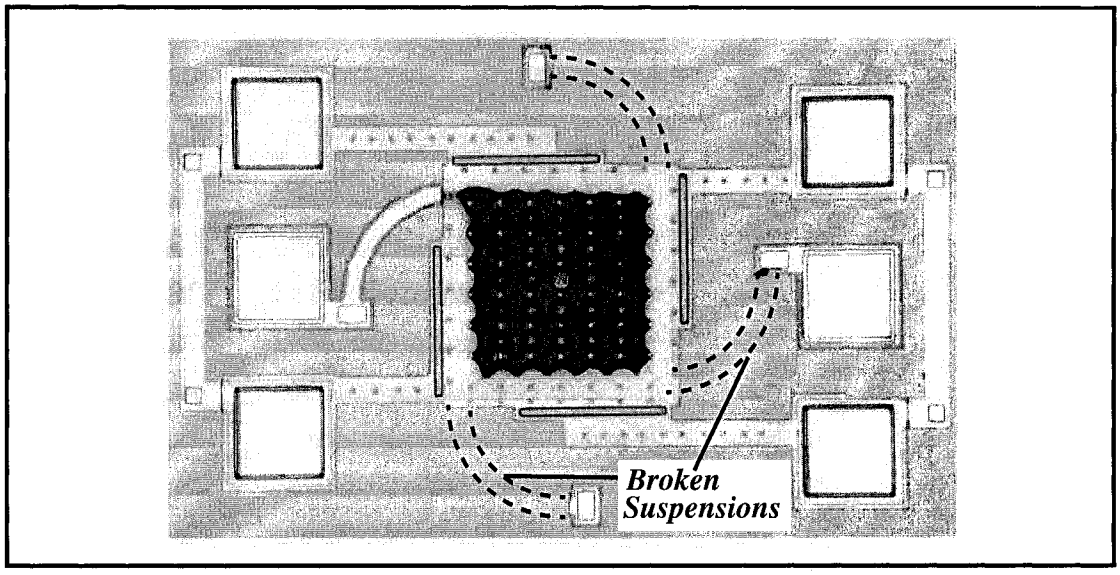


**Figure 3.21 A MEMS-based tunable capacitor with damaged suspensions.**

the capacitor plates varies significantly and is unpredictable. Much of the residual stress has been suppressed when four suspensions were used, as evident in Fig. 3.20(b). However, using more suspensions, effectively increases the overall spring constant ($k$), and would result in the need for a higher control voltage in order to achieve the same tuning characteristics (equation 3.6). One of the key factors to reduce warping is to use symmetric structures. Since symmetries will cancel out some of the opposite forces due to residual stresses. In reality, process variations limit the symmetries and still result in finite residual stresses.

**(b) Quality Factor** - From the measurement results in Fig. 3.17 and Fig. 3.18, it can been seen that the quality factors degrade significantly at the maximum tuning capacitances. The degradations in the quality factors are due to the increase in the series resistances of the structures, which are caused by the bending of the suspensions during actuation. As the thickness of the suspensions and the displacements of the actuation (i.e. spacings $d_1$ and $d_2$) are in the same order of magnitude, bending has a significant impact on the effective length of the suspensions, resulting in an increase of the overall series resistance. Wider suspensions should be used in order to reduce the series resistances. This comes at the expense of a higher actuation voltage, which is not desirable in today's low-voltage RF applications.

**(c) Reliability** - Reliability is always an important issue when implementing MEMS

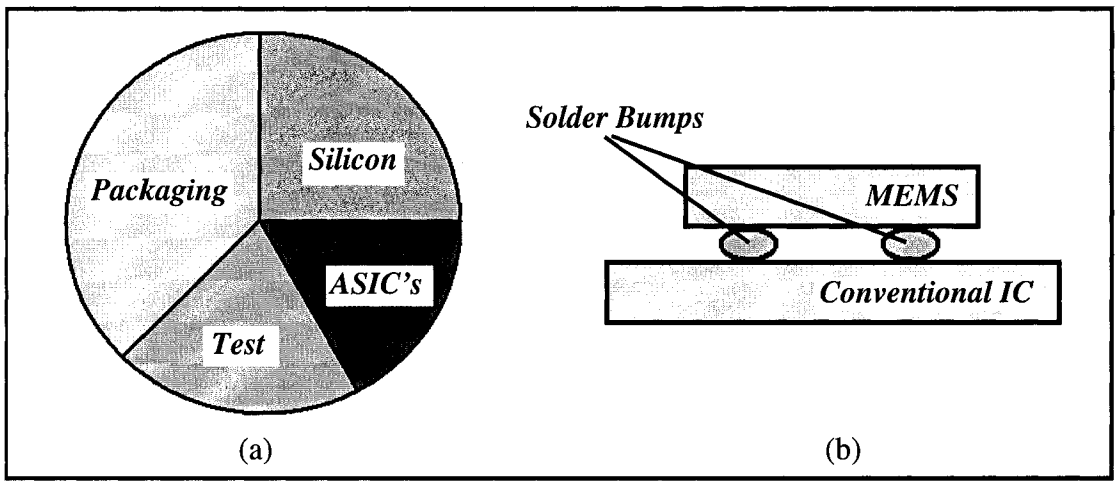


**Figure 3.22 (a) Relative cost of test, packaging, and ASIC's in a MEMS structure. (b) Flip-chip bonding technology.**

structures. Unlike traditional IC processes, MEMS devices are fragile and susceptible to mechanical shocks. Proper handlings of MEMS chips are critical. Improper handling of the structures results in damaged parts, such as the one showing in Fig. 3.21. The damages were caused by the laboratory technicians when taking the microphotographs. Special handling and assembling protocols, which are different from traditional IC's, are required to ensure the reliability of the MEMS structures. For instance, during device shipment, MEMS structures should be placed in gel-packs with foam cushions, in order to minimize shocks due to collisions with adjacent devices. All this imposes great challenges for commercial uses.

**(c) Packaging** - Packaging is another important issue when implementing MEMS structures. Silicon is only a small part of the final cost of a MEMS structure, as illustrated in Fig. 3.22(a). Packaging and test accounts for more than 60%, while the overall cost jumps up to 75% when including ASIC's. MEMS packaging requires full custom development, making it quite expensive. Furthermore, being able to integrate MEMS structures with traditional IC processes is the key to success. One of the promising approaches is flip-chip bonding (e.g. [69], [70]). In this approach, MEMS structures are bonded on top of traditional IC's, as illustrated in Fig. 3.22(b). MEMS technology is still in its infancy stage. Future advancement and process maturity of MEMS anticipate the presence of commercial MEMS products with low cost, high reliability and high integrability.

# Chapter 4 - Sub-1 V, > 5.8 GHz, Tunable LNA Measurement Results

Designing CMOS RF circuits operating at frequencies greater than 1 GHz in a standard CMOS process requires the following: i) Proper modeling of high quality passive components (i.e. inductors and capacitors), as described in the last chapter, and ii) good RF layout techniques, in order to minimize performance degradation. In this chapter, the layout techniques adopted in this work are addressed. Detailed measurement results of three sub-1 V CMOS LNA's are presented, including a frequency and gain tunable LNA.

## 4.1 - RF Layout Techniques

Apart from proper modeling of integrated passives, layout is another important step in optimizing high frequency designs. Poor layout could result in large discrepancies between the actual and expected performance, and could even result into a non-working circuit. The layout of a 5.8 GHz CMOS LNA is shown in Fig. 4.1, and is used to illustrate the RF layout techniques used in this work.

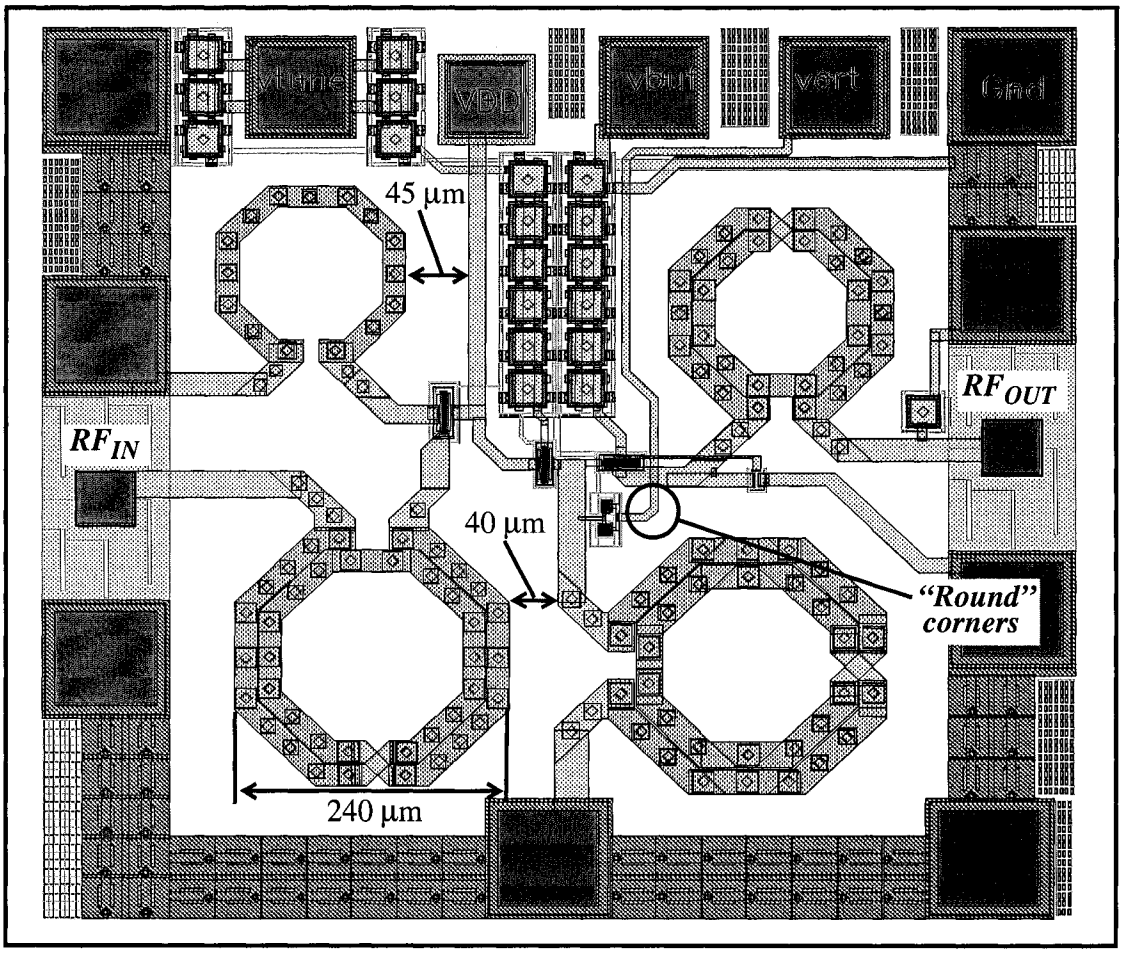


**Figure 4.1 Layout of a 5.8 GHz CMOS LNA.**

The layout is done in a uni-directional fashion, i.e. no signal returns close to its origin, in order to avoid coupling back to the input. The RF input and output ports are placed on opposite sides of the chip to improve port-to-port isolation. Since on-chip probing is used to measure the performance of this LNA, standard Ground-Signal-Ground (GSG) probes are used at both the input and output RF ports. The signal pads (i.e. RF input and output) are implemented using the top metal layer only, attempting to reduce the impact of their parasitic capacitances on the RF performance. In order to minimize the effect of substrate noise on the system, a solid ground plane constructed using a low resistivity metal-1 material is placed between the signal pads (metal-6) and the substrate.

Since the operation of inductors involves magnetic fields, they can affect nearby signals and circuits, and cause interference. Therefore, inductors are placed far apart from

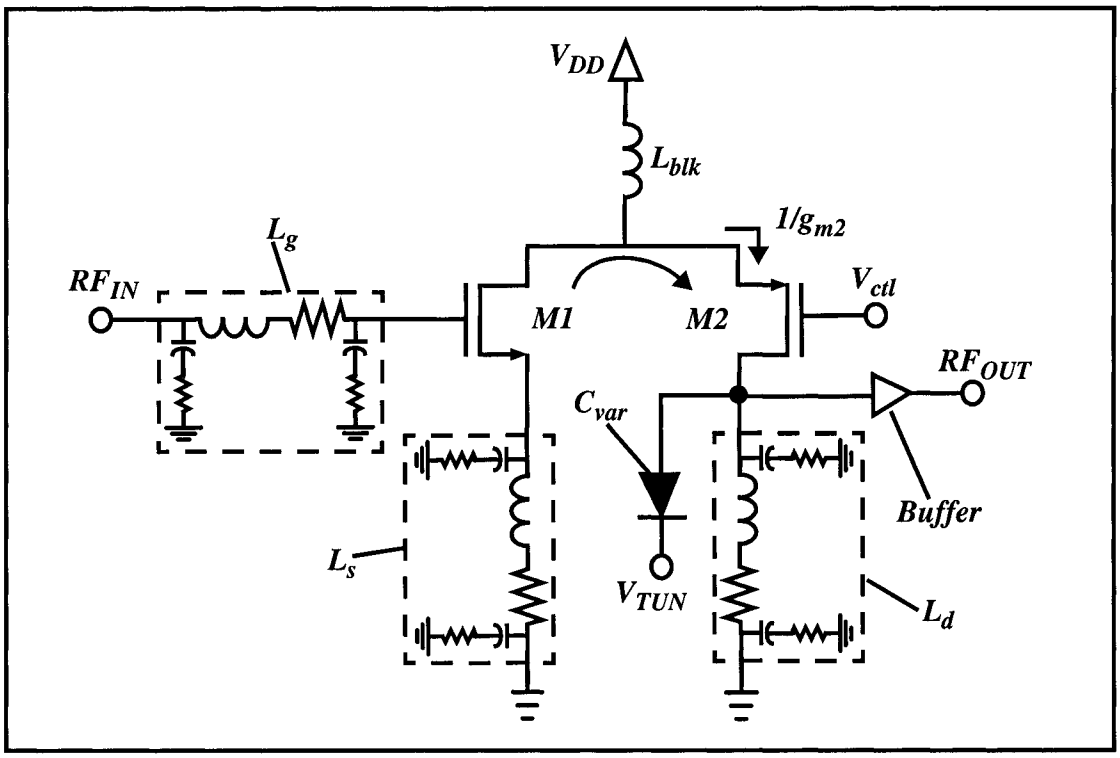


**Figure 4.2 Schematic of the gain and frequency tunable sub-1 V CMOS LNA.**

each other, as well as from the main circuit components, with reasonable distances. Furthermore, traces connected to all inductors are made wide enough to minimize the series parasitic resistances and inductances, and thus avoid inductor Q degradation. Ideally, all interconnections should be as short as possible in order to minimize their impact. However, this is not always possible, especially due to the large geometrical structure of the inductors when compared to other components such as transistors and resistors. When long interconnects become unavoidable in the layout, an in-house high frequency modeling routine is used [71] in order to accurately estimate the parasitics introduced. The main purpose of this routine is to increase the accuracy between the simulated and measured RF performances, by incorporating unexpected layout dependent parasitics (e.g. inductances and resistances). Finally, line widths are set according to RF design guidelines, keeping DC traces thin to present high impedances to RF signals, and AC connections wide and as short as possible. "Round" corners are used, instead of sharp ones, for interconnects in order to minimize signal reflections at RF, as illustrated in Fig. 4.1.

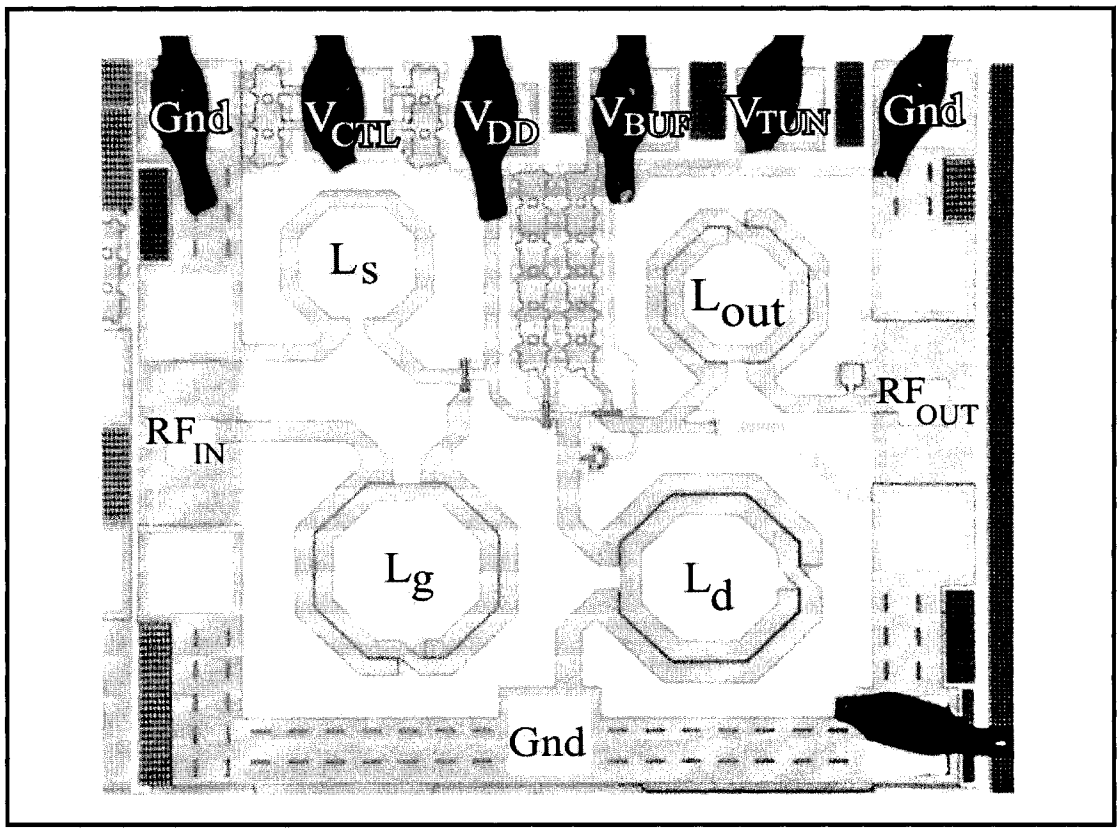


**Figure 4.3 Microphotograph of the tunable sub-1 V 5.8 GHz CMOS LNA.**

## 4.2 - Tunable Sub-1 V 5.8 GHz CMOS LNA

Rapid development towards higher carrier frequencies and low-voltage designs for wireless applications have been the main motivation behind this implementation. The objective of this design is to implement a state-of-the-art LNA in a standard CMOS process, targeting 5-6 GHz wireless LAN systems such as the IEEE 802.11a and HIPERLAN industry standards, with a strong focus on low-voltage operation.

As discussed in chapter 2, there are several LNA topologies which are suitable for low-voltage applications. The schematic of a gain and frequency tunable sub-1 V CMOS LNA is shown in Fig. 4.2. It is based on the folded cascode architecture, with the introduction of slight modifications in order to make it suitable for narrowband RF applications. This is a promising low-voltage structure, well-balanced in terms of stability, noise, and gain performances, with an inherent advantage of gain controlability

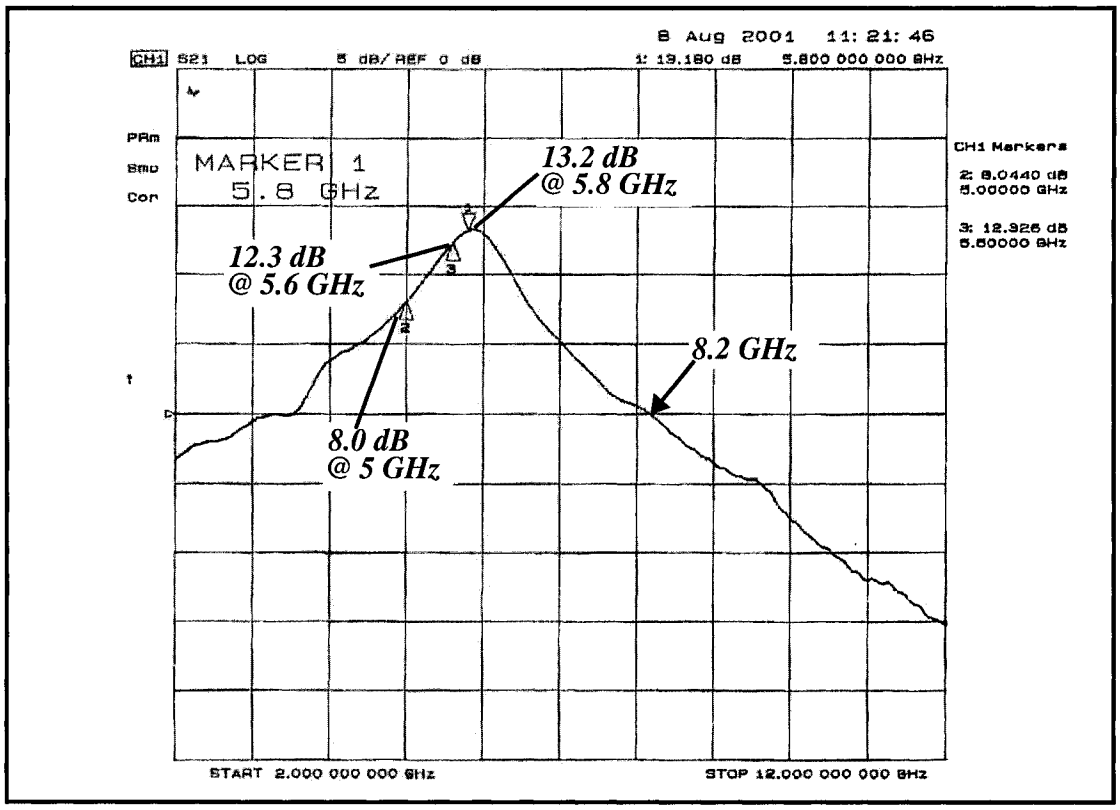


**Figure 4.4 Measured power gain of the sub-1 V 5.8 GHz CMOS LNA.**

over other architectures.

The LNA is implemented in a standard 0.18 μm CMOS process, targeting at a center frequency of 5.8 GHz with a supply voltage of 1 V. It has both gain and frequency tuning capabilities. The microphotograph of the LNA is shown in Fig. 4.3. The layout was done according to the RF layout techniques which were outlined in the previous section.

The experimental results of the 5.8 GHz CMOS LNA were measured on wafer using GGB Industries Inc. picoprobes and a 20 GHz Agilent 8720ES vector network analyzer. Standard Short-Open-Load-Through (*SOLT*) calibration procedures were performed. The forward transmission ($S_{21}$) plot is shown in Fig. 4.4. With a power consumption of 22.2 mW from a 1 V supply, a power gain of 13.2 dB is achieved at 5.8 GHz, with a noise figure of 2.5 dB. The LNA exhibits a power gain of 12.3 dB and 8.0 dB at 5.6 GHz and 5 GHz, respectively. The upper unity gain frequency of the LNA is at 8.2 GHz. The input and output reflection coefficients are below -5 dB and -10 dB respectively, as shown in Fig. 4.5. The LNA exhibits a power gain greater than 7 dB even at an extremely

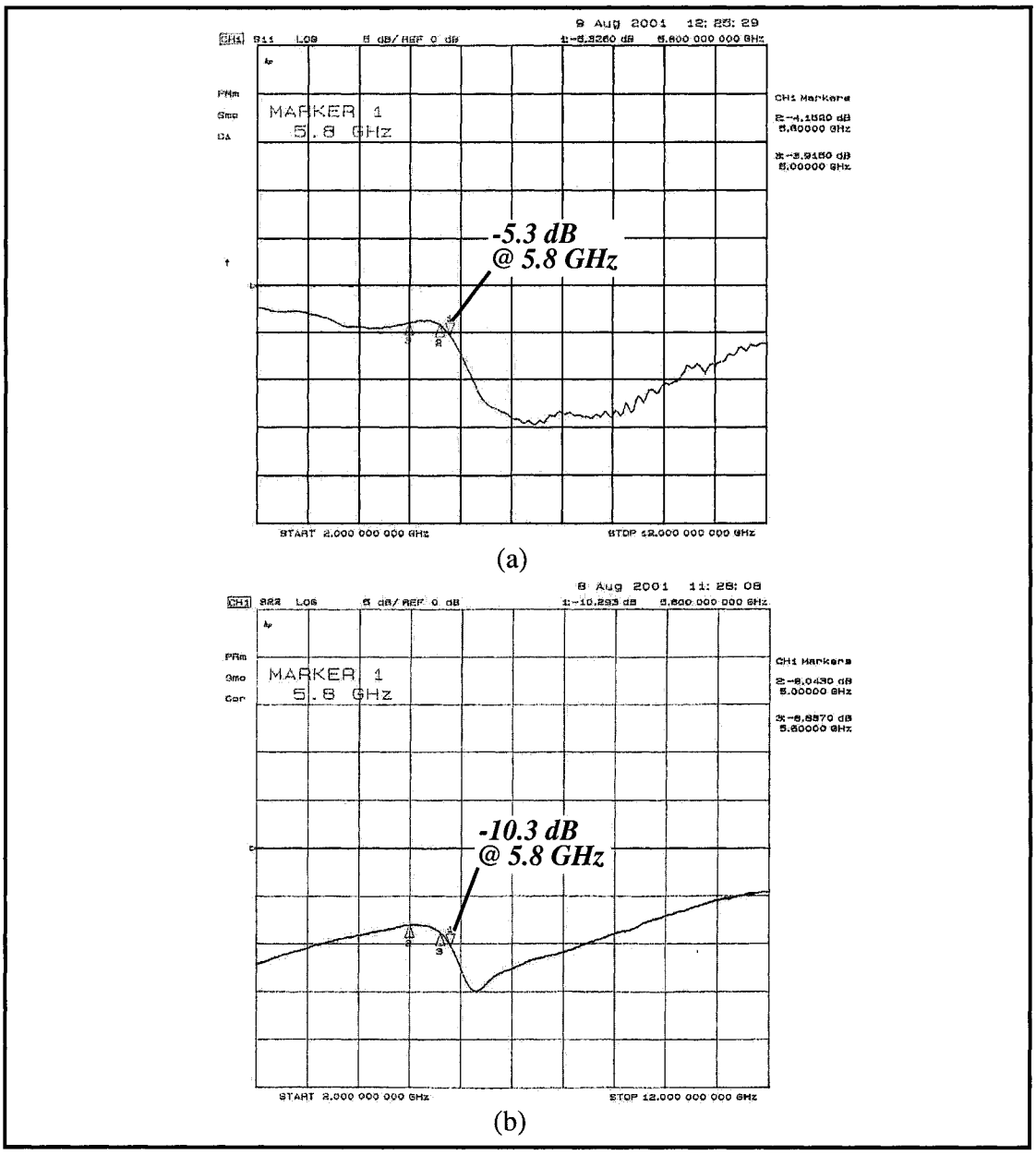


**Figure 4.5 Measured (a) input and (b) output reflection coefficients of the tunable sub-1 V 5.8 GHz CMOS LNA.**

low voltage supply of 0.7 V, with a power consumption of 12.5 mW and a noise figure of 2.68 dB. Fig. 4.6 shows the power gain of the LNA with a 0.7 V supply voltage.

Gain control is achieved by controlling the gate voltage ($V_{ctl}$) of the PMOS transistor M2, hence adjusting the overall gain of the LNA by varying the impedance looking into the source of transistor M2 (i.e.$1/g_{m2}$). Gain control is done without affecting the input noise and impedance matching which are independently set by the input NMOS transistor

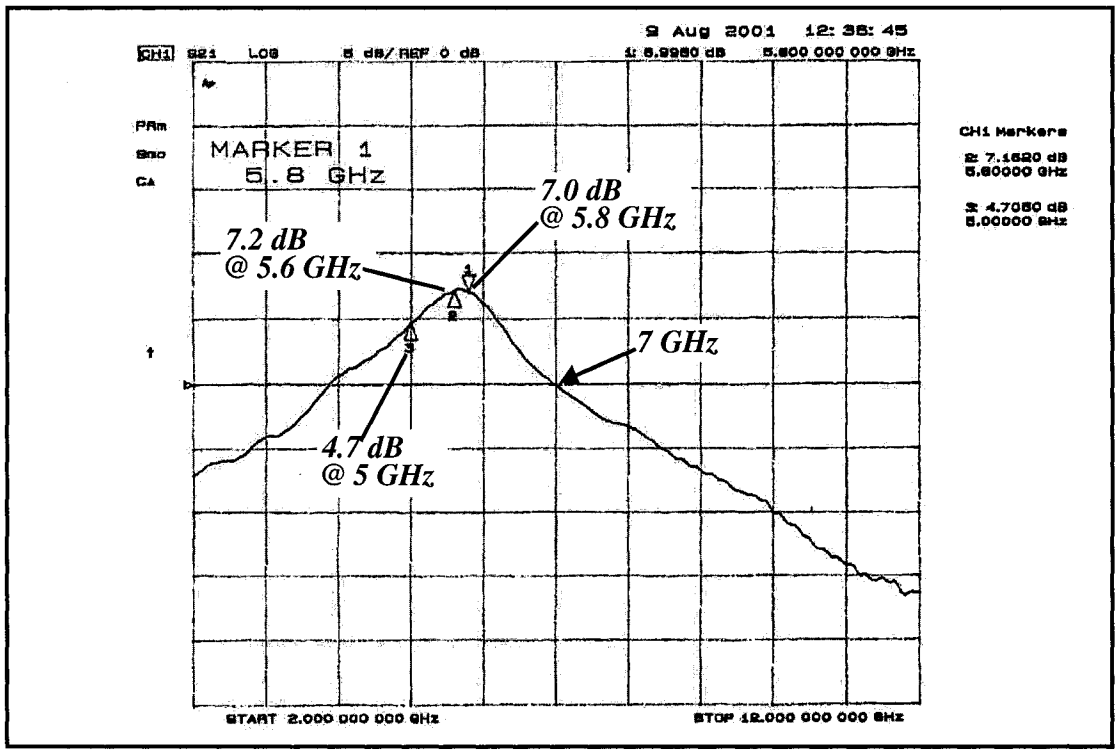


**Figure 4.6 Measured power gain with a supply voltage of 0.7 V.**

M1. The measured gain tuning characteristics of the LNA is shown in Fig. 4.7(a). A gain control of over 12 dB is achieved, without affecting the optimum noise performance.

A plot showing the frequency tunability of the LNA is presented in Fig. 4.7(b). A continuous frequency tuning of 360 MHz, from 5.6 GHz to 5.96 GHz, is achieved with the use of a simple varactor. This corresponds to a total tuning range of about 6%. An accumulation-mode varactor is used in the design, as outlined in section 3.2.4. This structure has been reported to provide a wider tuning range (i.e. 30%) and a better quality factor in comparison to other PN or $P^+N$ junction-based varactors. A stand-alone varactor structure, which was fabricated on the same run as the LNA design, was characterized. The measured capacitance tuning characteristics and quality factor of the accumulation-mode varactor are shown in Fig. 4.8. The measured tuning capacitance range is about 19%, which is smaller than the expected range of 30%. Furthermore, the measured quality factor of the varactor is much lower than expected, and varies between 8 and 14. These differences are mainly attributed to inaccurate initial varactor modeling, and to the additive parasitic capacitances resulting after laying out the varactor. The reduced

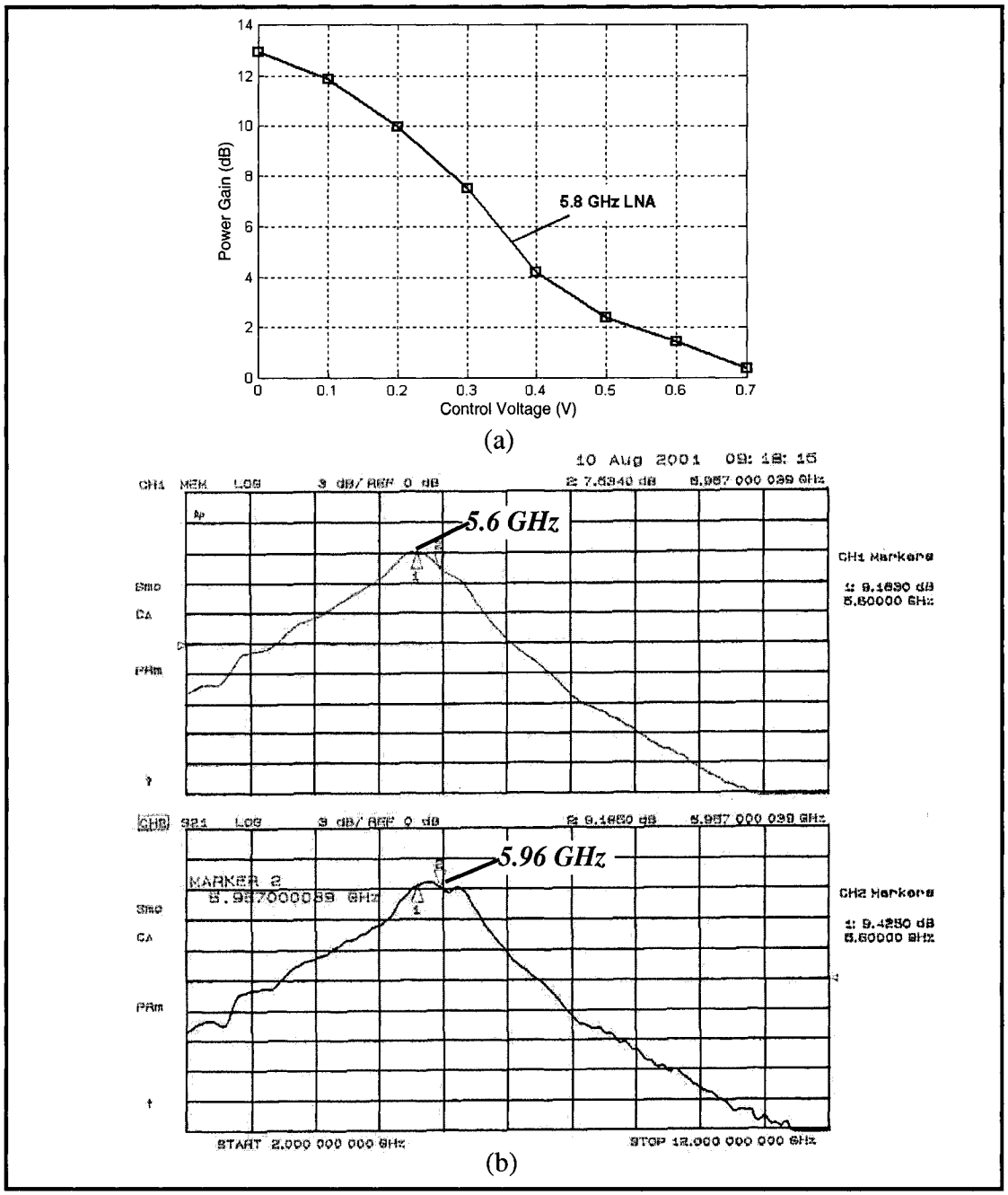


**Figure 4.7 (a) Gain and (b) frequency tuning characteristics of the LNA.**

capacitance tuning of the varactor limits the frequency tuning capability of the LNA, from 5.6 GHz to 5.96 GHz. It was designed to cover the entire 5-6 GHz frequency band. The unexpected low quality factor of the varactor has a slight impact on the resonant tank of the LNA: By using equation 3.4, the estimated quality factor of the resonant tank ($Q_{tank}$) of the LNA is about 5.8. This is lower than similar implementations in the

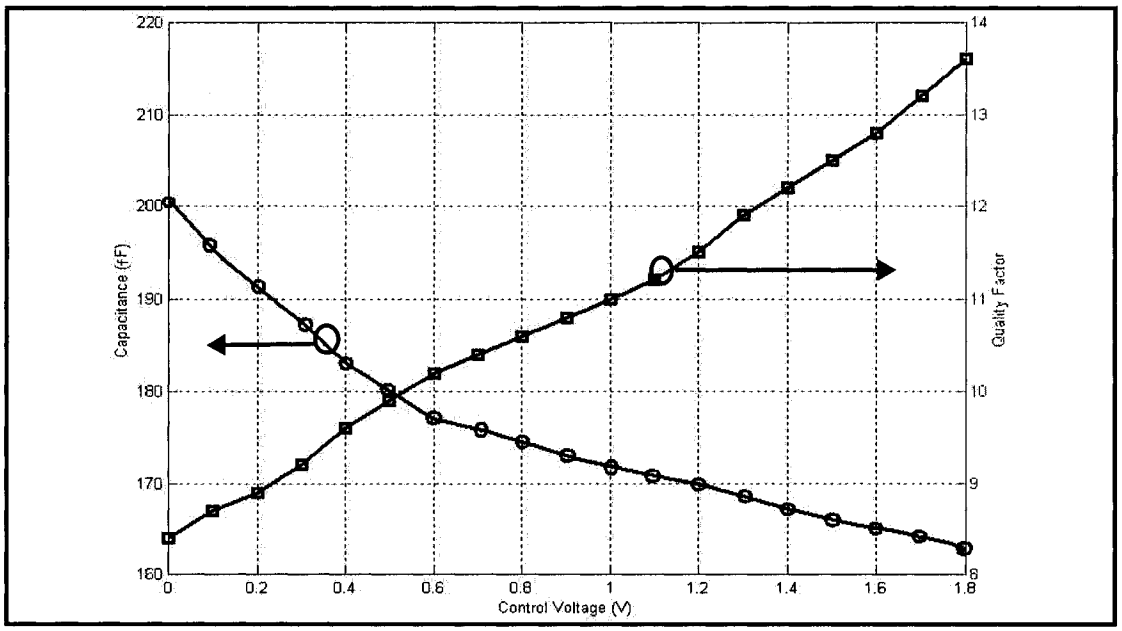


**Figure 4.8 Capacitance tuning characteristics and quality factor of the varactor.**

literature.

The 1-dB compression point ($P_{1\text{-}dB}$) was measured by increasing the input power level until the overall gain of the LNA became 1 dB lower than its theoretical value. With a 1 V supply, the input referred 1-dB compression point of the LNA is at -14 dBm, as shown in Fig. 4.9.

The performance summary of the LNA under different operating conditions, and a comparison to other low-voltage LNA's operating above 5 GHz are shown in Table 4.1. As can be seen, the RF performances of this implementation are comparable to those implemented in other high-cost technologies (e.g. Si BJT and SiGe). This shows the great potential of standard CMOS processes for high performance RF circuits.

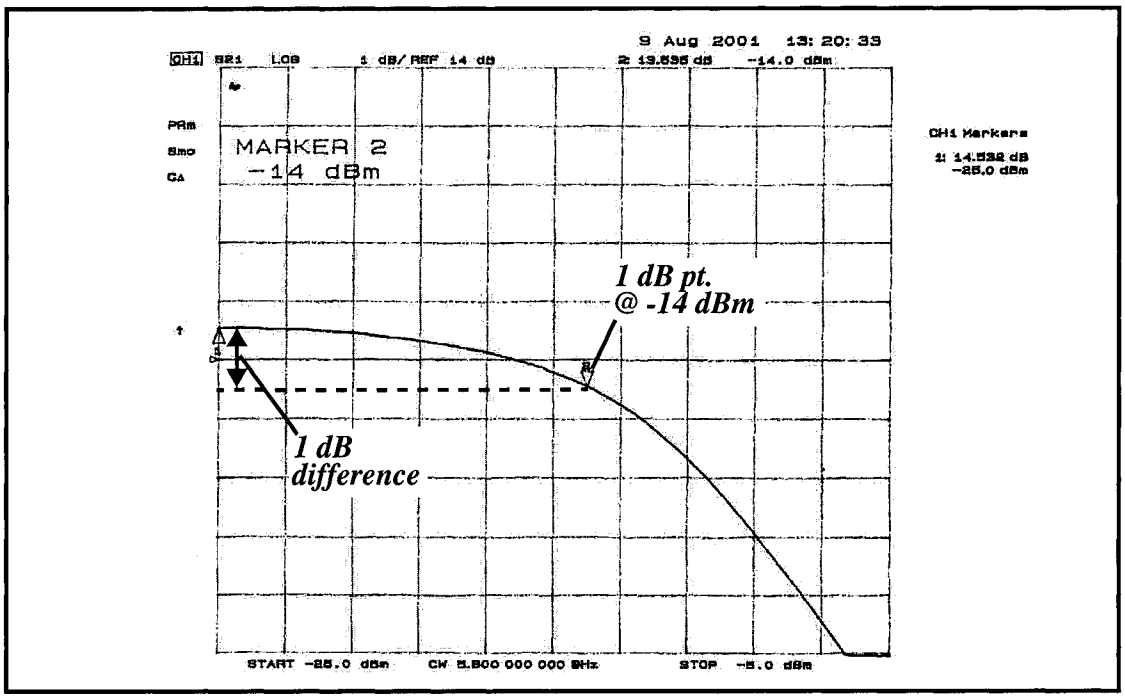


**Figure 4.9 1-dB compression point of the tunable 5.8 GHz CMOS LNA.**

| | This work | | [25] | [35] | [72] |
|---|---|---|---|---|---|
| Technology | CMOS 0.18 μm | | CMOS 0.35 μm | Si BJT 0.5 μm | SiGe HBT |
| Center Frequency ($f_o$) | 5.8 GHz | | 5.2 GHz | 5.8 GHz | 5.8 GHz |
| $V_{dd}$ | 1 V | 0.7 V | 1 V | 1 V | 1 V |
| $S_{21}$ | 13.2 dB | 7.0 dB | 7.87 dB | 11.5 dB | 6.9 dB |
| $S_{11}$ / $S_{22}$ | -5.3 / -10.3 dB | -7.1 / -12.3 dB | -16.1 / -18.7 dB | -9 / -13.7 dB | -6 / -28 dB |
| $P_{dd}$ | 22.2 mW | 12.5 mW | 12.4 mW | 6 mW | 13 mW |
| NF | 2.5 dB | 2.68 dB | 5.6 dB | 4 dB | 2.1 dB |
| $P_{in\text{-}1\ dB}$ | -14 dBm | -9 dBm | -6.2 dBm | -19 dBm | -20 dBm |
| Gain Tuning | 12.6 dB's | 7.0 dB's | None | None | None |
| Frequency Tuning | 360 MHz 5.6 - 5.96 GHz | | None | None | None |

**Table 4.1 - Performance summary and comparison to other low-voltage LNA's operating above 5 GHz.**

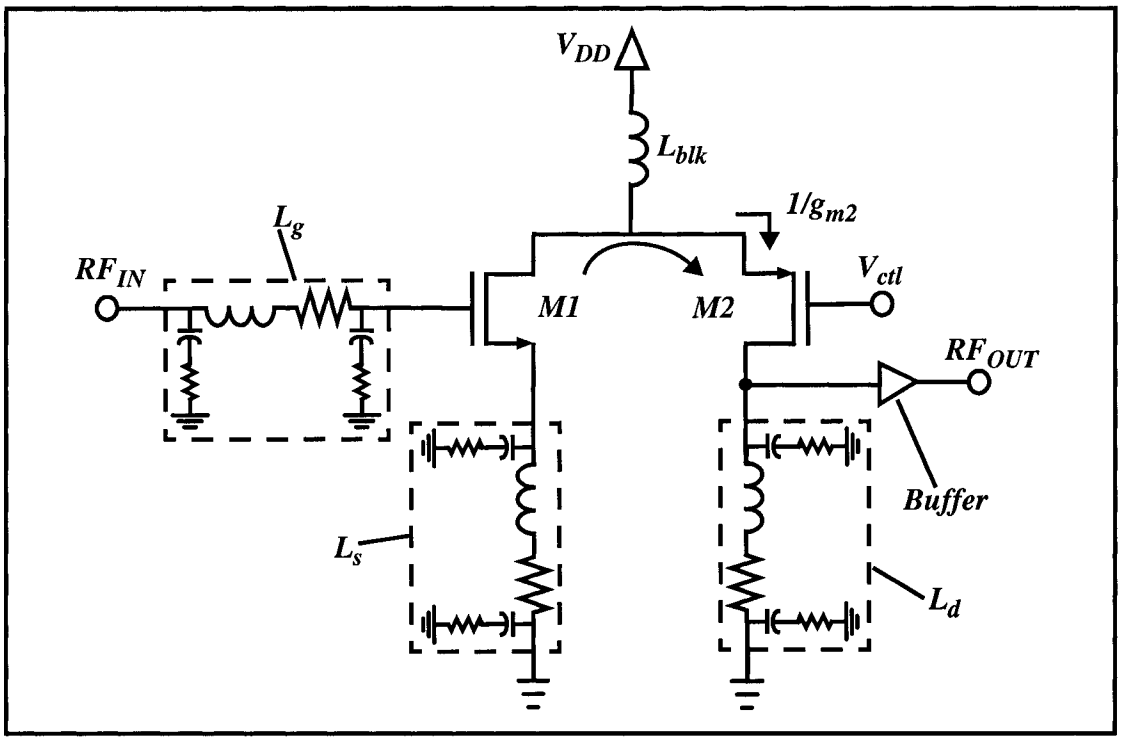


**Figure 4.10 Schematic of the gain controllable sub-1 V CMOS LNA.**

## 4.3 - Integrated 8 and 9 GHz CMOS LNA's

The CMOS LNA implementation described in the previous section was mainly targeted for 5-6 GHz WLAN applications, with a strong emphasis on low voltage operation. Attempting to push the frequency limit of current CMOS technologies, for applications where the use of higher carrier frequencies and low-voltage techniques are expected, two additional LNA's were implemented in a standard 0.18 μm CMOS process.

Following the excellent performance obtained from the 5.8 GHz LNA, the two implementations were designed and fabricated based on the same narrowband folded cascode topology. The designs were targeted for the 8-9 GHz range, operating with a voltage supply of 1 V, with gain controllability. The main difference between the two prototypes is the use of different inductor sizes. Based on the inductors design and optimization approach outlined in section 3.2.2, two and three layer inductors were used, attempting to maximize their quality factors in the 8-9 GHz frequency range. In

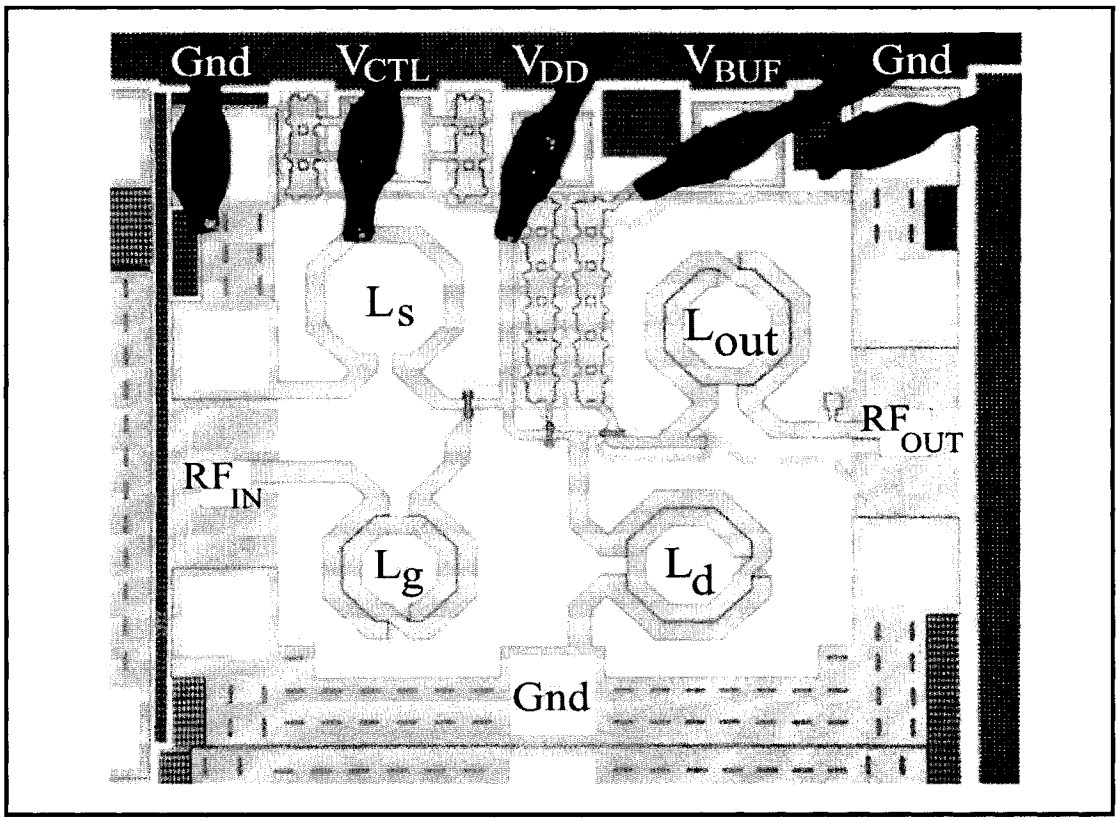


**Figure 4.11 Microphotograph of the sub-1 V 9 GHz CMOS LNA.**

particular, the top two metal layers (i.e. metal 5-6) were used for the 8 GHz LNA, while the top three layers (i.e. metal 4-5-6) were employed in the 9 GHz LNA. Frequency control was not implemented, due to the expected low quality factors and tuning ranges of the varactors, as became evident from the 5.8 GHz prototype. The schematic of the gain controllable sub-1 V CMOS LNA is shown in Fig. 4.10. Similar to the 5.8 GHz prototype, the layouts of these two designs were done according to the RF layout techniques outlined in section 4.1. The microphotograph of the 9 GHz LNA is shown in Fig. 4.11. The layout of the 8 GHz implementation is almost identical to the 9 GHz one, except for the use of different inductors, hence it is not shown here.

On-chip measurements with standard SOLT calibration were performed. The forward transmission ($S_{21}$) plots of both designs are shown in Fig. 4.12. With a power consumption of around 20 mW from a 1 V supply, both prototypes achieve a power gain of 12-13.5 dB at the frequency of interest, with a noise figure of 3.2-3.7 dB. Furthermore, both prototypes exhibit power gains greater than 10 dB over the frequency ranges of 6.7-

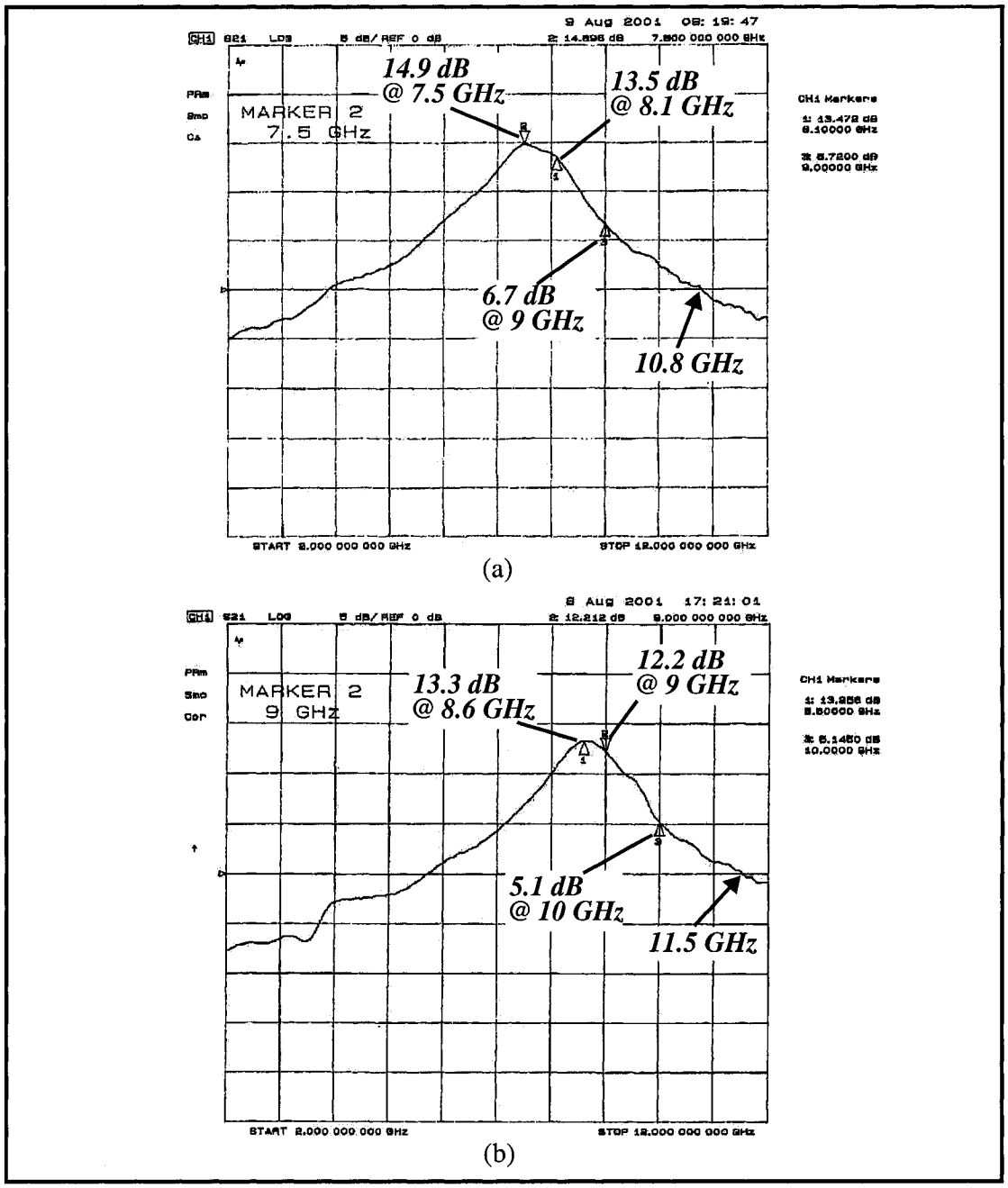


**Figure 4.12 Measured power gain of the (a) 8 GHz and (b) 9 GHz CMOS LNA's.**

8.6 GHz and 8.0-9.4 GHz, with upper unity gain frequencies of 10.8 GHz and 11.5 GHz, respectively. The input and output reflection coefficients of the two prototypes are below -5 dB and -13 dB, respectively. The input and output matching characteristics of the 9 GHz LNA are shown in Fig. 4.13. Both LNA's exhibit power gains greater than 5 dB at an extremely low voltage supply of 0.7 V, with power consumption of around 10 mW.

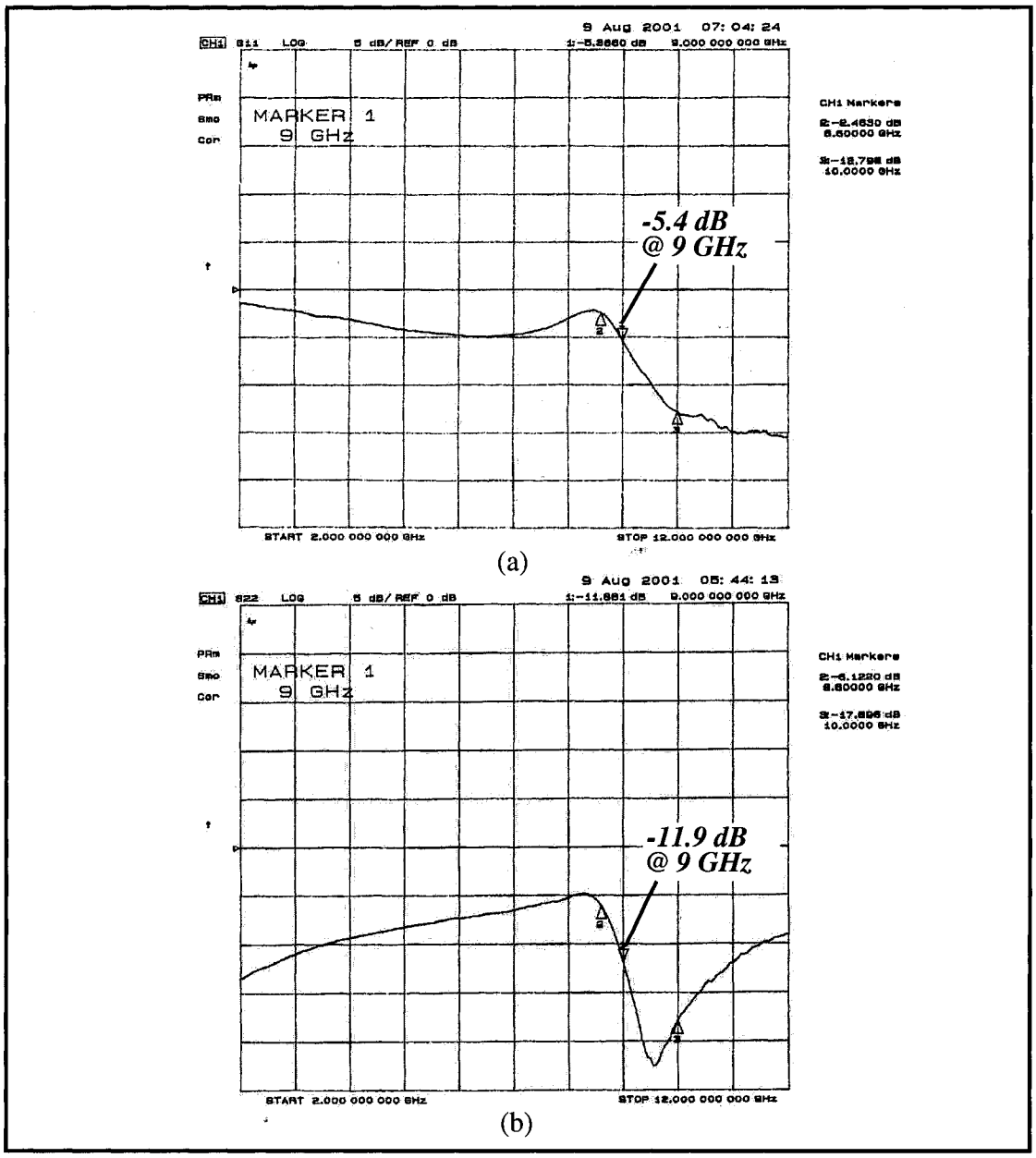


**Figure 4.13 Measured (a) input and (b) output reflection coefficients of the sub-1 V 9 GHz CMOS LNA.**

Fig. 4.14 shows the power gains of the LNA's with a 0.7 V supply voltage.

Gain control is achieved by controlling the gate voltage ($V_{ctl}$) of the PMOS transistor M2. A gain control of over 10 dB is achieved without any increase in circuit complexity, as pointed out in section 2.4.4. The gain tuning characteristics are shown in Fig. 4.15.

With a power supply of 1 V, the input referred 1-dB compression point of the LNA is at -13.2 dBm for the 8 GHz prototype, and at -8.9 dBm for the 9 GHz design. Fig. 4.16

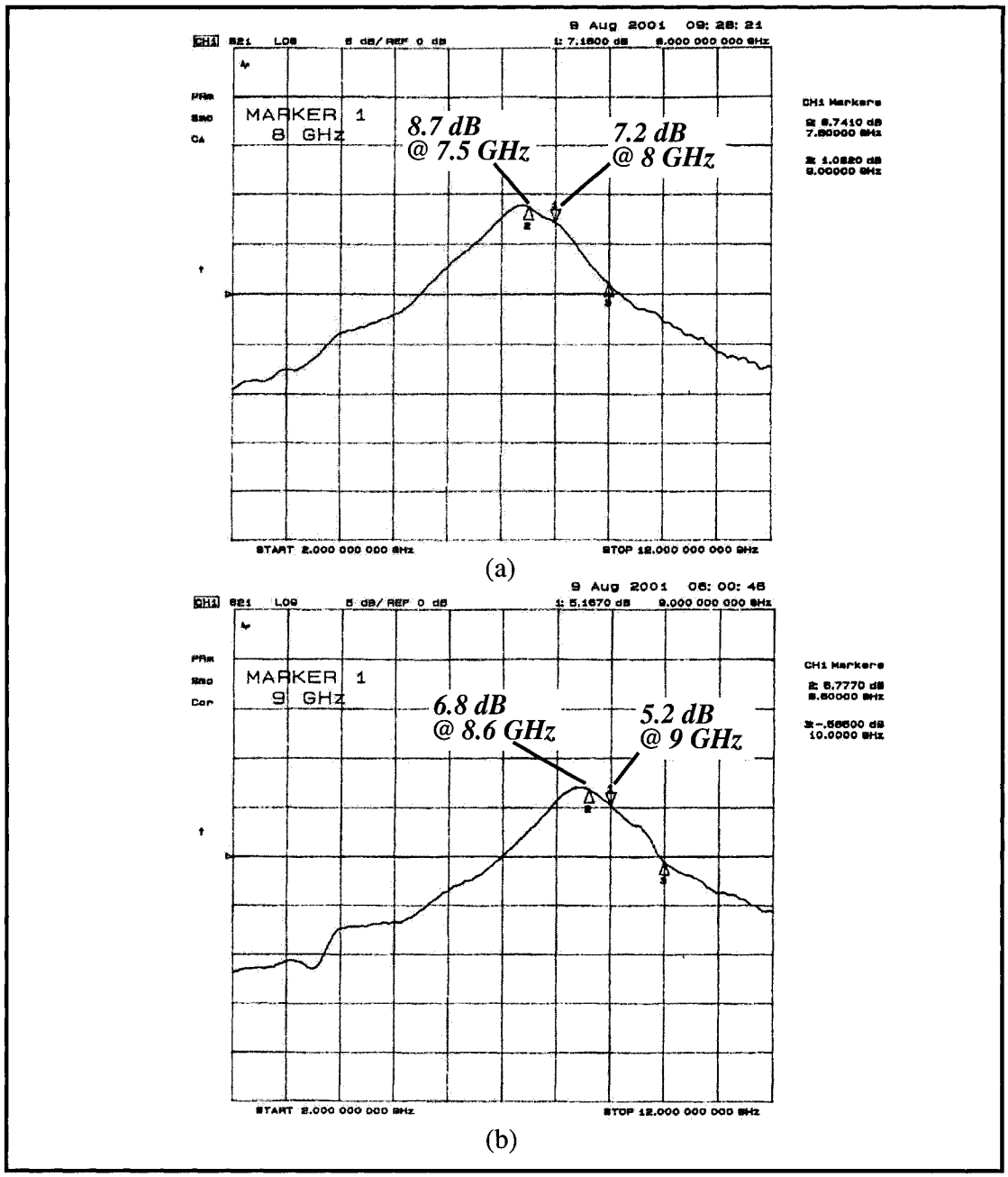


**Figure 4.14 Measured power gain of the (a) 8 GHz and (b) 9 GHz CMOS LNA's with a supply voltage of 0.7 V.**

shows the measured $P_{1\text{-}dB}$ of the 9 GHz CMOS LNA.

Despite the higher operating frequency of the 9 GHz LNA, it has a relatively narrower bandwidth when compared to the 8 GHz LNA. This is mainly due to the use of combined three metal layers (metal 4-5-6) for the inductors in the 9 GHz prototype as opposed to the top two metal layers (metal 5-6) used in the 8 GHz LNA. This supports the fact that

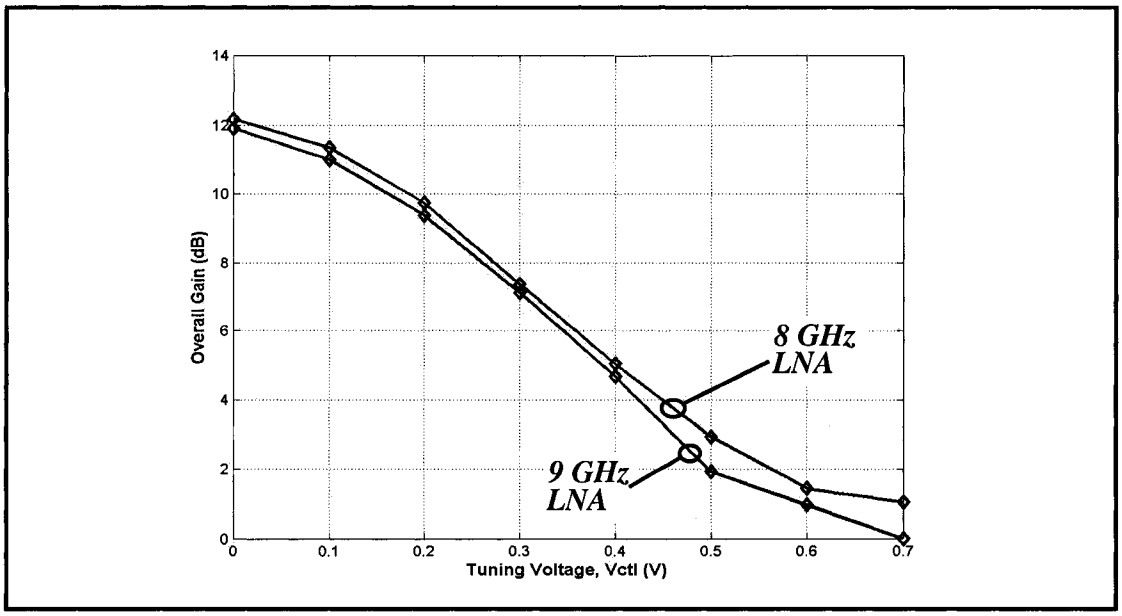


**Figure 4.15 Gain tuning characteristics of the 8 GHz and 9 GHz LNA's.**

inductors with higher Q can be realized in CMOS by stacking more metal layers to emulate thicker conductors. By using equation 3.4, the estimated quality factor of the resonant tanks ($Q_{tank}$) of the 8 GHz and 9 GHz CMOS LNA's are 6.2 and 6.6, respectively. Recall that the $Q_{tank}$ of the 5.8 GHz prototype was about 5.8, which is lower than these two implementations operating at higher frequencies. The Q degradation is mainly attributed to the varactors.

The performance summary of the last two LNA's under different conditions are shown in Table 4.2, and compared to the LNA in [34]. These two LNA's are CMOS designs, operating at the highest operating frequencies reported in the literature to-date. They have demonstrated that the current CMOS technology is capable of delivering high performance RFIC's for future wireless applications.

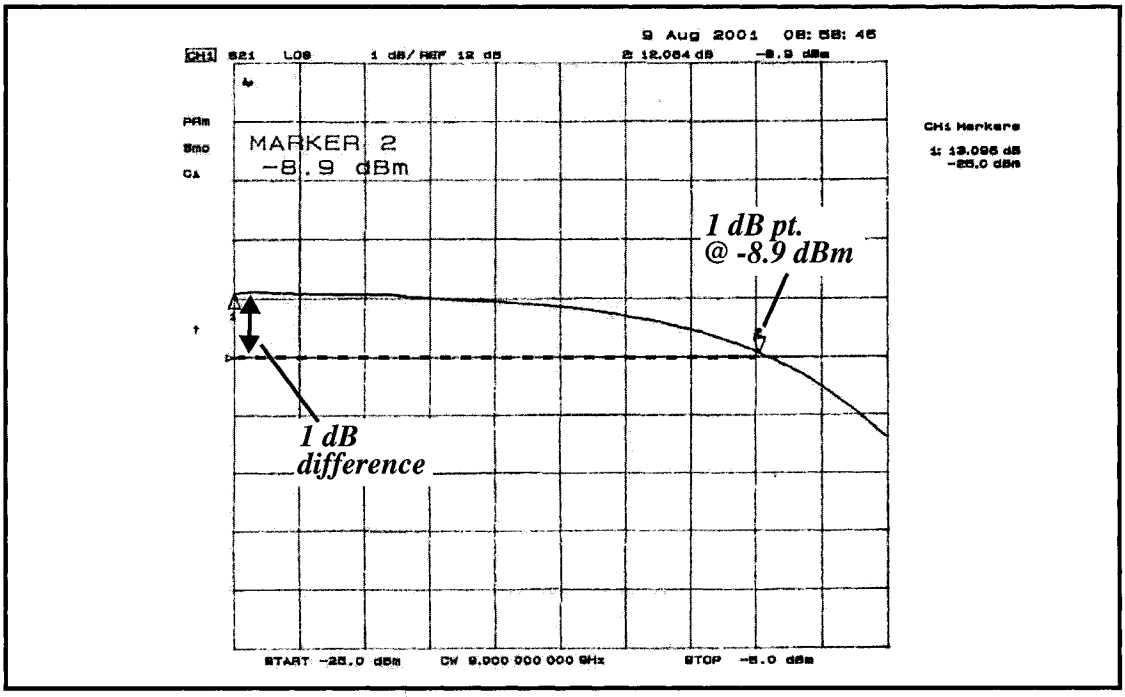


Figure 4.16 1-dB compression point of the 9 GHz CMOS LNA.

| | This Work 8 GHz LNA | | This Work 9 GHz LNA | | [34] 7 GHz LNA |
|---|---|---|---|---|---|
| Technology | CMOS 0.18 μm | | CMOS 0.18 μm | | CMOS 0.25 μm |
| $V_{dd}$ | 1 V | 0.7 V | 1 V | 0.7 V | 2 V |
| $S_{21}$ | 13.5 dB | 7.1 dB | 12.2 dB | 5.2 dB | 6.9 dB |
| $S_{11}$ / $S_{22}$ | -5.8 / -13.9 dB | -10.9 / -17 dB | -5.4 / -11.9 dB | -9 / -12.9 dB | - |
| $P_{dd}$ | 22.4 mW | 10.7 mW | 19.6 mW | 9 mW | 13.8 mW |
| $NF_{50\ \Omega}$ | 3.2 dB | 4.1 dB | 3.7 dB | 4.7 dB | 3.3 dB |
| $P_{in\text{-}1\ dB}$ | -13.2 dBm | -8.6 dBm | -8.9 dBm | -4.3 dBm | -1.6 dBm |
| Gain Tuning | 11.4 dB's | 7.1 dB's | 11.2 dB's | 5.2 dB's | - |

Table 4.2 - Performance summary of the two CMOS LNA's, and comparison to [34].

# Chapter 5 - Conclusion

## 5.1 - Summary

The growing demand for wireless mobile communications has pushed IC designs towards low voltage, low power, and high frequency of operation. CMOS is a reliable and cost effective solution for today's complex digital circuits. With a rapid advancement in CMOS technology, it is also becoming a contender for RF applications, offering the possibility for higher level of integration of the analog RF front-ends and the baseband digital circuitries.

This thesis was concerned with the design of low-voltage high frequency CMOS low noise amplifiers (LNA's). In chapter 1, an overview of the current technology choices for RFIC's, particularly in the context of LNA designs, was presented. The motivation, challenges, and need for integrated CMOS LNA's operating at the 5-10 GHz frequency band, with a strong emphasis on low-voltage topologies, were addressed.

In chapter 2, basic theory and important parameters for designing LNA's were introduced. Trade-offs between different low-voltage LNA topologies were discussed. The chosen topology, namely the narrowband folded cascode structure, was shown to be a well-balanced architecture in terms of stability, noise, and gain performances.

In chapter 3 and 4, design strategies for optimizing RF passive devices beyond 5 GHz were presented. Important RF layout issues were also addressed. The effectiveness of these RF layout techniques and optimization were supported and demonstrated by the

excellent RF performances of three successful LNA implementations. This also demonstrated that current state-of-the-art CMOS technologies are adequate for today's, as well as for future wireless applications. Furthermore, it was shown that the chosen topology is suitable for low-voltage high performance sub-1 V RF applications, with the added inherent advantage of gain control capability. Table 5.1 summarizes the performances of the three CMOS LNA's in this work, as well as that of the bipolar LNA which was implemented at early stages of this research work.

Apart from the discussion of integrated RF passives in CMOS, structures implemented in novel processes such as RF MEMS were investigated. Several successful tunable capacitor structures were implemented in a MUMPs technology. Measurements have shown that it is feasible to implement RF passives in MEMS. Further advancement and maturity of MEMS technology anticipates the ability to implement high performance RF passives in the future.

| Design | 8 GHz LNA [37] | | 9 GHz LNA [37] | | 5.8 GHz LNA [36] | | 5.8 GHz LNA [35] |
|---|---|---|---|---|---|---|---|
| Technology | CMOS 0.18 μm | | CMOS 0.18 μm | | CMOS 0.18 μm | | Bipolar 0.5 μm |
| $V_{dd}$ | 1 V | 0.7 V | 1 V | 0.7 V | 1 V | 0.7 V | 1 V |
| $S_{21}$ | 13.5 dB | 7.1 dB | 12.2 dB | 5.2 dB | 13.2 dB | 7.0 dB | 11.5 dB |
| $P_{dd}$ | 22.4 mW | 10.7 mW | 19.6 mW | 9 mW | 22.2 mW | 12.5 mW | 6.6 mW |
| $NF_{50\,\Omega}$ | 3.2 dB | 4.1 dB | 3.7 dB | 4.7 dB | 2.5 dB | 2.68 dB | 4 dB |
| $P_{in\text{-}1\,dB}$ | -13.2 dBm | -8.6 dBm | -8.9 dBm | -4.3 dBm | -14 dBm | -9 dBm | -19 dBm |
| Gain Tuning | 11.4 dB's | 7.1 dB's | 11.2 dB's | 5.2 dB's | 12.6 dB's | 7.0 dB's | - |
| Frequency Tuning | - | - | - | - | 360 MHz 5.6 - 5.96 GHz | | - |

**Table 5.1 - LNA performance summary in this work.**

## 5.2 - Topics for Future Research

This thesis has presented several key ideas which include: i) Standard CMOS processes are capable of delivering adequate performance for RF circuits operating at 5-10 GHz such as low noise amplifiers, ii) the chosen topology, the narrowband folded cascode architecture, is suitable for high performance low-voltage (< 1 V) RF applications, and iii) the feasibility of using MEMS for next generation RF passives. While the results of this work are promising, they only act as the first step towards more challenging and exciting research areas.

**(a) Fully Integrated and Packaged Designs** - In this thesis, all the implementations were designed for on-chip measurement purposes. They were implemented for proof of concept, hence were far from commercial standards. Fully integrated and packaged designs are highly valuable but impose new challenges in CMOS RFIC's, including the effect of package parasitics at RF, and robust temperature insensitive biasing schemes.

**(b) Enhanced Functionality with Novel Circuit Topologies** - The CMOS LNA's presented differ from other existing LNA's, featuring a new and very simple gain control mechanism, without jeopardizing the noise and linearity performances. With the increasing demand for dual- and tri-band designs, multi-band functionality can be easily incorporated in this architecture, for instance, by switching different resonant tanks of the circuit.

**(c) Fully Integrated Low-Voltage CMOS Transceivers** - The CMOS LNA's presented were targeted at a nominal supply voltage of 1 V, and remained functional even at a low supply voltage of 0.7 V. The chosen architecture is not only limited to LNA designs, but can also be generalized to other RF building blocks such as mixers and oscillators. Hence, a fully integrated sub-1 V CMOS transceiver can be realized.

**(d) Research on RF MEMS** - Several micromachined tunable capacitors were implemented in this work. Their characteristics were examined. While current process maturity limits their usage for RF applications, future technology advancements anticipate high performance and more reliable structures, which are suitable for wireless communications. Nonetheless, packaging and integrability remain key challenges in the research on RF MEMS.

# References


[1] C. K. T. Chan and C. Toumazou, "Design of a Class E Power Amplifier with Non-Linear Transistor Output Capacitance and Finite DC-Feed Inductance", *2001 IEEE International Symposium on Circuits and Systems (ISCAS 01)*, vol. 2, pp. 129-132, May 2001.

[2] H. L. Tu and C. Toumazou, "Low-Distortion CMOS Complementary Class E RF Tuned Power Amplifiers", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, pp. 774-779, May 2000.

[3] C. J. Debono, F. Maloberti, and J. Micallef, "A 1.8 GHz CMOS Low Noise Amplifier", *2001 IEEE International Conference on Electronics, Circuits and Systems (ICECS 2001)*, vol. 3, pp. 1391-1394, September 2001.

[4] C. J. Debono, F. Maloberti, and J. Micallef, "A 900 MHz, 0.9 V Low-Power CMOS Downconversion Mixer", *2001 IEEE Conference on Custom Integrated Circuits (CICC 2001)*, pp. 527-530, May 2001.

[5] M. Stanacevic and G. Cauwenberghs, "Charge-based CMOS FIR Adaptive Filter", *Midwest Symposium on Circuits and Systems*, vol. 3, pp. 1410-1413, August 2000.

[6] D. H. Goldberg, G. Cauwenberghs, and A. G. Andreou, "Analog VLSI Spiking Neural Network with Address Domain Probabilistic Synapses", *2001 IEEE International Symposium on Circuits and Systems (ISCAS 01)*, vol. 2, pp. 241-244, May 2001.

[7] L. E. Larson, "Integrated Circuit Technology Options for RFIC's - Present Status and Future Directions", *IEEE Journal of Solid-State Circuits,* vol. 33, pp. 387-399, March 1998.

[8] E. A. McShane and K. Shenai, "Technologies and Design of Low-Power RF Microsystems", *22nd International Conference on Microelectronics*, vol. 1, pp. 107-115, May 2000.

[9] K. C. Hwang et al., "Very High Gain Millimeter-Wave InAlAs/INGaAs/GaAs Metamorphic HEMT's", *IEEE Electron Device Letters*, vol. 20, no. 11, pp. 551-553, November 1999.

[10] A. Gruhle, "Prospects for 200 GHz on Silicon with SiGe Heterojunction Bipolar Transistors", *Proceedings of the 2001 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 19-25, October 2001.

[11] L. F. Tiemeijer et al., "A Record High 150 GHz $f_{max}$ realized at 0.18 μm Gate length in an Industrial RF-CMOS Technology", *Technical Digest of 2001 IEEE International Electron Devices Meeting*, pp. 10.4.1-10.4.4, September 2001.

[12] T. Matsumoto et al., "70 nm SOI-CMOS of 135 GHz $f_{max}$ with Dual Offset-Implatnted Source-Drain Extension Structure for RF/Analog and Logic Applications", *Technical Digest of 2001 IEEE International Electron Devices Meeting*, pp. 10.3.1-10.3.4, September 2001.

[13] J. R. Long, "A Low-Voltage 5.1 - 5.8 GHz Image-Reject Downconverter RF IC", *IEEE Journal of Solid-State Circuits,* vol. 35, pp. 1320-1328, September 2000.

[14] M. Copeland, S. Voinigescu, D. Marchesan, P. Popescu, and M. Maliepaard, "5-GHz SiGe HBT Monolithic Radio Transceiver with Tunable Filtering", *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp. 170-181, February 2000.

[15] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF Front-End IC", *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 350-355, March 1994.

[16] R. G. Meyer, W. D. Mack, and J. J. Hageraats, "A 2.5-GHz BiCMOS Transceiver for Wireless LAN's", *IEEE Journal of Solid-State Circuits,* vol. 32, pp. 2097-2014, December 1997.

[17] H. S. Momose et al., "High Frequency AC Characteristics of 1.5 nm Gate Oxide MOSFETs", *Technical Digest of 1996 IEEE International Electron Device Meeting*, pp. 105-108, December 1996.

[18] J. Crols and M. Steyaert, "A Single-Chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology", *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 1483-1492, December 1995.

[19] A. A. Abidi, "CMOS Wireless Transceivers: The New Wave", *IEEE Communications Magazine*, vol. 37, pp. 119-124, August 1999.

[20] M. Steyaert, "Single Chip CMOS RF Transceivers: Wishful Thinking or Reality", *IEE Seminar on Low Power IC Design*, ref. no. 2001/04208, 2001.

[21] A. Ajjikuttira et al., "A Fully-Integrated CMOS RFIC for Bluetooth Applications", *IEEE International Solid-State Circuits Conference,* pp. 198-199, February 2001.

[22] R. A. Rafla and M. N. El-Gamal, "2.4 - 5.8 GHz CMOS LNA's using Integrated Inductors", *Midwest Symposium on Circuits and Systems*, vol. 1, pp. 302-304, August 2000.

[23] A. H. Mostafa and M. N. El-Gamal, "A Fully Integrated Sub-1 V 4 GHz CMOS VCO, and a 10.5 GHz Oscillator", *26th European Solid-State Circuits Conference,* pp. 312-315, September 2000.

[24] P. Leroux and M. Steyaert, "High-Performance 5.2 GHz LNA with On-chip Inductor to Provide ESD Protection", *Electronic Letters*, vol. 37, pp. 467-468, March 2001.

[25] C. Tang and S. Liu, "Low Voltage CMOS Low Noise Amplifier Using Planar Interleaved Transformer", *Electronic Letters*, vol. 37, pp. 497-498, April 2001.

[26] A. H. Mostafa and M. N. El-Gamal, "A CMOS VCO Architecture Suitable for Sub-1 Volt High-Frequency (8.7-10 GHz) RF Applications", *International Symposium on Low Power Electronics and Design ISLPED'01*, pp. 247-250, August 2001.

[27] "X Band Low Noise Amplifier - XLNA2S.02", *Rockwell Scientific*, URL: <http://www.rsc.rockwell.com/phemt/index.html>.

[28] "AMF Low-Noise Amplifier - AMF-1F-058065-10-5P", *Miteq*, URL: <http://www.miteq.com/micro/amps/amfamps/lownoise/lowframe.htm>.

[29] B. G. Choi et al., "A Low Noise On-Chip Matched MMIC LNA of 0.76 dB Noise Figure at 5 GHz for High Speed Wireless LAN Applications", *GaAs IC Symposium* 2000, pp. 143-146, October 2000.

[30] Y. Aoki et al., "A 1.4 dB NF Variable-Gain LNA with Continuous Control for 2 GHz Band Mobile Phones using InGaP Emitter HBTs", *2001 Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 231-234, May 2001.

[31] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier", *IEEE Journal of Solid-State Circuits,* vol. 32, pp. 745-759, May 1997.

[32] E. H. Westerwick, "A 5 GHz Band CMOS Low Noise Amplifier with a 2.5 dB Noise Figure", *2001 International Symposium on VLSI Technology, Systems, and Applications,* pp. 224-227, June 2000.

[33] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8 dB NF ESD-Protected 9 mW CMOS LNA", *IEEE International Solid-State Circuits Conference,* pp. 410-411, February 2001.

[34] R. Fujimoto and K. Kojima, "A 7-GHz 1.8 dB (minimum) NF CMOS Low Noise Amplifier", *27th European Solid-State Circuits Conference,* September 2001.

[35] T. K. K. Tsang and M. N. El-Gamal, "A Fully Integrated 1 V 5.8 GHz Bipolar LNA", *2001 IEEE International Symposium on Circuits and Systems (ISCAS 01)*, vol. 2, pp. 843-845, May 2001.

[36] T. K. K. Tsang and M. N. El-Gamal, "Gain and Frequency Controllable Sub-1 V 5.8 GHz CMOS LNA", *2002 IEEE International Symposium on Circuits and Systems (ISCAS 02)*, accepted May 2002.

[37] T. K. K. Tsang and M. N. El-Gamal, "Gain Controllable Very Low Voltage (< 1 V) 8-9 GHz Integrated CMOS LNA", *2002 Radio Frequency Integrated Circuits (RFIC) Symposium*, accepted June 2002.

[38] T. H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits", *Cambridge University Press*, 1998.

[39] A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions", *IEEE Transactions on Electron Devices*, vol. ED-33, pp. 1801-1805, November 1986.

[40] B. Razavi, R. H. Yan, and K. F. Lee, "Impact of Distributed Gate Resistance on the Performance of Noise Devices", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, pp. 750-754, November 1994.

[41] H. T. Friis, "Noise Figures of Radio Receivers", *Proceedings of the IRE,* vol. 32, pp. 419-422, July 1944.

[42] B. Razavi, "RF Microelectronics", *Prentice Hall PTR*, 1998.

[43] T. Manku, G. Beck, and E. Shin, "A Low-Voltage Design Technique for RF Integrated Circuits", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, pp. 1408-1413, November 1998.

[44] E. Abou-Allam, J. J. Nisbet, and M. C. Maliepaard, "Low-Voltage 1.9 GHz Front-End Receiver in 0.5 μm CMOS Technology", *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 1434-1443, October 2001.

[45] B. Ray, T. Manku, R. Beards, T. Nisbet, and W. Kung, "A Highly Linear Bipolar 1 V Folded Cascode 1.9 GHz Low Noise Amplifier", *Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 157-160, September 1999.

[46] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", *4th edition Oxford University Press*, 1998.

[47] F. Beaudoin and T. K. K. Tsang, "The Design of a 1 V 5.8 GHz Cascode CMOS LNA", *VLSI Design Project*, McGill University, June 2001.

[48] S. Pennisi, S. Scaccianoce, and G. Palmisano, "A New Design Approach for Variable-Gain Low Noise Amplifiers", *2000 Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 139-142, June 2000.

[49] E. Sacchi, I. Bietti, F. Gatta, F. Svelto, and R. Castello, "A 2 dB NF, Fully Differential, Variable Gain, 900 MHz CMOS LNA", *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 94-97, June 2000.

[50] A. Niknejad, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF ICs", *Master's Thesis*, University of California, Berkeley, 1997.

[51] K. B. Ashby et al., "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process", *IEEE Journal of Solid-State Circuits,* vol. 31, pp. 4-9, January 1996.

[52] J. Burghartz, M. Souyer, and K. Jenkins, "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, pp. 100-104, January 1996.

[53] J. Y. Chang, A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2-μm CMOS RF Amplifiers", *IEEE Electron Device Letters*, vol. 14, pp. 246-248, May 1993.

[54] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's", *IEEE Journal of Solid-State Circuits,* vol. 13, pp. 743-752, June 1998.

[55] C-K Kim et al., "High-Performance Electroplated Solenoid-type Integrated Inductor Si for RF Applications using Simple 3D Surface Micromachining Technology", *Technical Digest of the 1998 International Electron Devices Meeting*, pp. 544-547, December 1998.

[56] C-K Kim et al., "Surface Micromachined Solenoid on-Si and on-Glass Inductors for RF Applications", *IEEE Electron Device Letters*, pp. 487-489, September 1999.

[57] A. Niknejad and R. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF ICs", *IEEE Journal of Solid-State Circuits,* vol. 33, pp. 1470-1481, October 1998.

[58] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked Inductors and Transformers in CMOS Technology", *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 620-628, April 2001.

[59] R. Rafla, "Integrated Inductor Modeling and CMOS Low Noise Amplifier for Radio-Frequency Applications", *Master's Thesis*, McGill University, 2001.

[60] P. Andreani and S. Mattisson, "On the Use of MOS Varactors in RF VCO's", *IEEE Journal of Solid-State Circuits,* vol. 35, pp. 905-910, June 2000.

[61] T. Soorapanth, C. Yue, D. Shaeffer, T. Lee, and S. Wong, "Analysis and Optimization of Accumulation-Mode Varactors for RF ICs", *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 32-33, June 1998.

[62] R. Castello, P. Erratico, S. Manzini, and F. Svelto, "A +/- 30% Tuning Range Varactor Compatible with Future Scaled Technologies", *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 34-35, June 1998.

[63] "Accelerometers - ADXL202", *Analog Devices*,
URL: <http://www.analog.com/technology/mems/accelerometers/index.html>.

[64] J. Y. Park and M. K. Allen, "Packaging-Compatible High Q Microinductors and Microfilters for Wireless Applications", *IEEE Transactions on Advanced Packaging*, vol. 22, pp. 207-213, May 1999.

[65] A. Dec and K. Suyama, "Micromachined Electro-Mechanically Tunable Capacitors and Their Applications to RF IC's", *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 2587-2596, December 1998.

[66] D. Young and B. Boser, "A Micromachined Variable Capacitor for Monolithic Low-Noise VCOs", *IEEE Solid-State Sensor and Actuator Workshop*, pp. 86-89, June 1996.

[67] K. E. Petersen, "Silicon as a Mechanical Material", *Proceedings of the IEEE,* vol. 70, pp. 420-457, May 1982.

[68] D. A. Koester, R. Mahadevan, B. Hardy, and K. W. Markus, "MUMPs Design Handbook Rev. 7.0", *Cronos Integrated Microsystems,* 2001.

[69] R. Irwin, W. Zhang, K. Harsh, and Y. Lee, "Quick Prototyping of Flip Chip Assembly with MEMS", *Proceedings of 1998 IEEE Radio and Wireless Conference (RAWCON 98)*, pp. 293-296, August 1998.

[70] K. Harsh, W. Zhang, V. Bright, and Y. Lee, "Flip-Chip Assembly for Si-Based RF MEMS", *Proceedings of 1999 IEEE International Conference on Microelectromechanical Systems (MEMS 99)*, pp. 273-278, January 1999.

[71] H. Zhang, "High Frequency Parasitic Modeler", *VLSI Design Project*, McGill University, September 2001.

[72] M. Soyuer, J. Plouchart, H. Ainspan, and J. Burghartz, "A 5.8 GHz 1 V Low Noise Amplifier in SiGe Bipolar Technology", *1997 Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 19-22, June 1997.