Silicon Subwavelength Grating Structures For Mode-division-multiplexed Silicon Photonic Switches

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Abstract

The ever-increasing demand for bandwidth density and internet protocol (IP) traffic causes a bottleneck in inter and intra-datacenter communication systems. This imposes a challenge in bandwidth density, communication speed, and power consumption. As a promising solution, complementary metal oxide semiconductor (CMOS) compatible silicon-on-insulator (SOI) technology offers low absorption loss, high index contrast between core and surrounding oxide, and high bandwidth data transmission capability which improves the performance of data center interconnects in terms of energy consumption per bit transfer. The bandwidth density can be further increased by employing multiplexing techniques such as polarization division multiplexing (PDM), wavelength division multiplexing (WDM), and mode division multiplexing (MDM). Recently, MDM has received significant attention as an enabling technology to send multiple data streams over a channel using a single wavelength.

On the other hand, subwavelength grating (SWG) structures in SOI technology are opening numerous opportunities to contribute to the design of more complex photonic integrated circuits. SWG structures enable us to control the refractive index, birefringence, and dispersion of optical materials such as silicon in SOI technology. This helps us to design and optimize silicon photonics (SiPh) structures for specific requirements of applications.

In some fabrication processes, the SiO_2 cladding may not fully fill the small gap between the fine features of SWG structures which results in buried air gaps (voids) in the cladding of the

structure. We investigate the voids' impact on several common SiPh structures including SWGs by simulation and experiment. Considering Applied NanoTools (ANT) center as the accessible fabrication facility, we characterize the ANT process voids using the focused ion beam-helium ion microscopy (FIB-HIM) methodology. We find out that the voids' cross-section area in this process is less than 500 nm^2 which is very low compared to other reported studies. Investigating the impact of such small voids verified by both simulation and experiment, demonstrate that ANT voids do not have a significant impact on the performance of our designs. We then proceed with fabricating our SWG designs at the ANT center.

As an essential part of multimode switches, we design and characterize a multimode compact and broadband SWG power splitter. The use of SWG structures is not only reducing the overall length of the power splitter by 66% but also increases the bandwidth from 40 nm to 100 nm compared to conventional structures. The total experimental insertion loss in the experiment is less than 0.1 dB and 0.65 dB for TE0 and TE1, respectively, and the intermodal crosstalk is measured to be less than -17 dB for both input modes.

Next, we utilize the designed SWG-based power splitter to design a dual-mode broadband compact switch (DBcS) capable of simultaneously transferring the first two transverse electric (TE) modes. The switch worst-case insertion loss is measured to be less than -1.3 dB. In addition, the crosstalk within the wavelength range from 1500 nm to 1600 nm is below -13 dB for both TE0 and TE1input modes. Open eye diagrams for 10 Gb/s non-return-to-zero (NRZ) data transmission for single-mode and multimode transmission demonstrates the capability of the switch in handling multiple data streams simultaneously using a single wavelength laser. The bit error rate (BER) power penalty tests are performed and an error-free BER of 10^{-12} for both single-mode and multimode transmission is demonstrated.

We believe that such experimentally demonstrated multimode switch benefiting from a compact and broadband design combined with WDM techniques may have potential applications in high data rate MDM-WDM switches for optical interconnects.

Abrégé

La demande croissante de densité de bande passante et de protocole IP (Internet Protocol) provoque un goulot d'étranglement dans les systèmes de communication. La technologie du silicium sur isolant (SOI) permet une faible perte d'absorption, un contraste d'indice élevé entre le noyau et l'oxyde environnant, ainsi qu'une transmission de données de bande passante élevée qui améliore la performance énergétique par bit des interconnexions du centre de données. La densité de bande passante peut être augmentée davantage en employant des techniques de multiplexage telles que le multiplexage par division de polarisation (PDM), le multiplexage par répartition en longueur d'onde (WDM) et le multiplexage par division modale (MDM). Dernièrement, le MDM a reçu beaucoup d'attention puisqu'il permet l'envoi de plusieurs flux de données sur un canal en utilisant une seule longueur d'onde.

D'autre part, les structures de réseau de sous-longueurs d'ondes dans la technologie du SOI ouvrent la porte à la conception de circuits intégrés photoniques plus complexes. Les structures de réseau de sous-longueurs d'ondes nous permettent de contrôler l'indice de réfraction, la biréfringence et la dispersion de matériaux optiques tels que le silicium dans la technologie du SOI.

Dans certains processus, le revêtement SiO_2 peut ne pas remplir complètement les petits espaces entre les composants délicats des structures de réseau de sous-longueurs d'ondes. Cela cause des bulles d'air bloquées (vides) dans le revêtement de la structure. Nous étudions l'impact de ces

vides sur plusieurs structures courantes de la photonique sur silicium. Nous avons défini les vides pour le centre Applied NanoTools (ANT) en utilisant la méthode du faisceau d'ions focalisé et la microscopie à ions hélium (FIB-HIM). Nous avons trouvé que la section transversale des vides dans ce processus est inférieure à 500 nm^2, ce qui est très faible par rapport aux autres études rapportées. Nous avons étudié l'impact de ces petits vides sur nos conceptions par simulation et expérimentation et avons trouvé que les vides d'ANT n'avaient pas d'impact significatif sur les performances de nos conceptions.

Ensuite, nous avons conçu et caractérisé un diviseur de puissance de réseau de sous-longueurs d'ondes qui était à la fois multimodale, ultra-compacte et à haut débit. L'utilisation des structures de grille sous-longueur d'onde a augmenté la bande passante de 40 nm à 100 nm. De plus, elle a permis la réduction de la taille totale du diviseur de puissance de 66 %. L'affaiblissement d'insertion totale dans l'expérience était inférieur à 0,1 dB et à 0,65 dB pour TE0 et TE1 respectivement. La diaphonie modale était inférieure à -17 dB pour les deux modes d'entrée.

Ensuite, nous avons utilisé le diviseur de puissance basé sur la réseau de sous-longueurs d'ondes pour concevoir un commutateur bimode compact à haut débit capable de transférer simultanément les deux premiers modes électriques transversaux (TE). L'affaiblissement d'insertion du commutateur était inférieur à -1,3 dB dans le pire des cas et la diaphonie modale pour les modes d'entrée TE0 et TE1 était <-13 dB pour une longueur d'onde allant de 1500 nm à 1600 nm. Les diagrammes à œil ouvert à partir de la transmission de données non-retour à zéro (NRZ) à 10 Gbit/s pour la transmission monomode et multimode démontrent la capacité du commutateur à gérer simultanément plusieurs flux de données à l'aide d'un seul laser à longueur d'onde unique. Les tests de pénalité de puissance du taux d'erreur sur les bits (BER) ont été effectués et un BER sans erreurs de 10^{-12} pour les transmissions monomodes et multimodes a été démontré.

Nous pensons qu'un commutateur multimode compact à haut débit, comme démontré à l'aide des expérimentations combinées aux techniques de WDM, pourrait trouver sa place et son emploi dans les commutateurs des MDM-WDM à haute vitesse de transfert pour les interconnexions optiques.

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List of Acronyms

ANT	Applied NanoTools
AC	adiabatic coupler
ADC	asymmetric directional coupler
BER	bit error rate
BOX	buried oxide layer
CMOS	complementary metal oxide semiconductor
CVD	chemical vapor deposition
CW	continuous wave
DBcMMI	dual-mode broadband compact MMI
DBcS	dual-mode broadband compact switch
DPWA	densely packed waveguide arrays
DUV	deep ultraviolet
EBL	electron beam lithography
EDFA	erbium-doped fiber amplifier
ER	extinction ratio
FDTD	finite difference time domain
FIB-HIM	focused ion beam-helium ion microscopy
ICP-RIE	inductively coupled plasma-induced reactive ion etching
IL	insertion loss
IP	Internet Protocol
LD	laser diodes
MDM	mode division multiplexing

MMI	multimode interference
MPW	multi-project wafer
MZI	Mach-Zehnder interferometer
NRZ	non-return-to-zero
PC	polarization controller
PD	photodetector
PDL	polarization-dependent loss
PDM	polarization division multiplexing
PECVD	plasma-enhanced chemical vapor deposition
PIC	photonic interconnect
PPG	pulse pattern generator
PRBS	pseudorandom binary sequence
SEM	scanning electron microscopy
SMF	single-mode fiber
SOA	semiconductor optical amplifier
SOI	silicon on insulator
SWG	subwavelength grating
TE	transverse electric
TiW	titanium - tungsten
TM	transverse magnetic
VLSI	very large scale integration
VOA	variable optical attenuator
WDM	wavelength division multiplexing

Chapter 1

Introduction

The new advances in technology such as 5G, machine learning, cloud computing, social networking are causing a bottleneck in bandwidth density, communication speed, and overall energy consumption in data centers. The number of devices connected to the global internet protocol (IP) networks will exceed three times the global population by 2023 [1]. During the past two decades, the performance of computing systems has been expanding with a factor of 1000 every 10 years. Amdahl balanced system law implies that the system bandwidth scales accordingly; thus, the system bandwidth of datacenter networks should approach exascale by 2024 [2, 3].

Modern conventional technologies still rely on electrical wiring where cheap and reliable copper wires link large quantities of transistors and the circuit connectivity on the ever-smaller chips since the 19th century. However, with the new advances, we are approaching the bottlenecks of copper wires such as limited bandwidth, current leakage, large power consumption, and heat dissipation.

The main problem here is that conventional electronic systems must charge and discharge the wires to send a bit of data to the destination. Even in microscopic scales inside CPU and RAM, this charge-discharge cycle takes energy and time.

Moore's law in 1965 says the number of transistors in the dense integrated circuit doubles every two years [4]. By increasing lithography precision and with minimum feature sizes down to 5 nm, and the advancements in multicore processes, the development of modern processors can still scarcely follow Moore's law [5]. However, with the ever-increasing data rate and bandwidth density, the parasitic effects in conventional systems are the main barrier to further improvements.

One promising solution is optical interconnects that the data is transmitted using optical signals, i.e., photons. Zero mass and charge photons travel as fast as light. Therefore, optical systems can transmit signals with a much higher data rate.

Photonic applications are going beyond this with new advances including logic processing as well as quantum computing which lie to the near future. Photonic interconnects are available today with advantages including capacity, scalability, energy efficiency, and high speed.

1. 1 Silicon-on-Insulator (SOI)

The term silicon-on-insulator refers to the use of a layer of silicon dioxide (SiO_2) under the silicon layer as shown in Fig. 1.1. Another layer of SiO_2 as cladding may be used on top of the waveguides protecting the Si layer and engineering the refractive index difference. The SiO_2 underneath the waveguide layer, called the box, is usually different than the SiO_2 of the cladding as they are formed through different processes. Therefore, the refractive index of the box and cladding might be slightly different, while foundries try to keep them close as much as possible. There is a Si substrate layer underneath the box. The thickness of the substrate is usually larger than 600 μm to avoid fracturing during dicing of the wafer into small dies or pick and placements. The silicon handling layer mainly does not have a considerable impact unless in some specific applications such as grating couplers, and edge couplers.

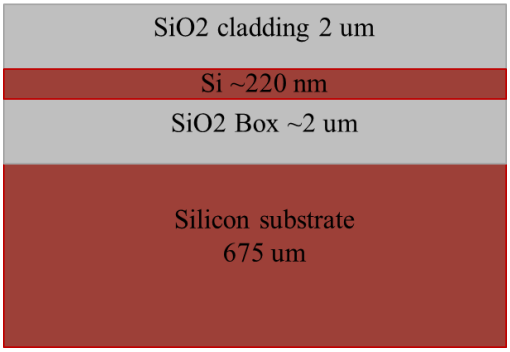

Fig. 1.1. Cross-sectional of a standard SOI platform with thickness.

Titanium – tungsten (TiW) metal heaters may be used on top of the silicon waveguides as shown in Fig. 1.2 to apply thermo optic phase shift in silicon photonic structures.

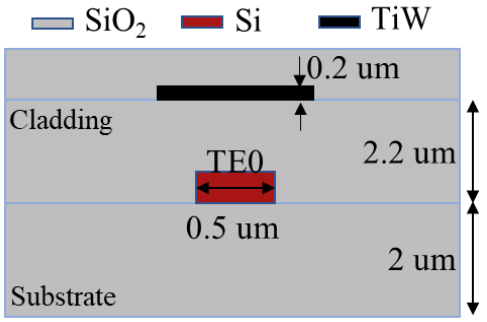

Fig. 1.2 Cross-sectional of an SOI platform showing a single-mode waveguide and a TiW metal heater.

The refractive indexes of silicon and silicon dioxide are around 3.4 and 1.4, respectively, resulting in a total internal reflection in the silicon waveguide core. Such high refractive index contrast highly confines the light in the waveguide core which helps us to realize compact structures.

Silicon has a transparent window in the wavelength range 1100 nm to 7000 nm, approximately, which completely covers the near-infrared communication band of 1300 nm to 1500 nm. Some excellent optical properties, like large optical damage threshold and thermal conductivity, also appear in Si.

The development of Si photonics can be traced back to the pioneering work done by Soref et al. in the mid-1980s [6].

SiO_2 absorption loss is minimum around 1.31 ± 0.4 μm and 1.55 ± 0.4 μm wavelength ranges. Therefore, optical fibers must operate in these regions to minimize the loss. Silicon is transparent through the whole band from 1.3 μm to 1.6 μm. However, SiPh chips should be finally connected to optical fiber communication systems; thus, we design SiPh structures in 1.31 μm and 1.55 μm bands. Optical fibers have a minimum loss in the 1.55 um region. Therefore, for long-distance connections, designers choose 1.55 μm to minimize the loss.

There are other factors that make the 1.31 μm band a more favorable option in short reach connections (<10 km). Table 1.1 shows losses in a specific kind of G.652 single-mode fiber (SMF) [7]. As shown in Table 1.1, the loss difference at 1310 nm and 1550 nm wavelengths is insignificant for distances less than 10 km whereas in longer distances the loss difference is significant making the 1550 nm more desirable.

Table 1.1 G.652 SMF losses at different wavelengths

Wavelength	Absorption loss				
	500 m	2 km	10 km	40 km	80 km
1310 nm	0.21 dB	0.84 dB	4.2 dB	16.8 dB	33.6 dB
1550 nm	0.14 dB	0.56 dB	2.8 dB	11.2 dB	22.6 dB

In many applications, people need to integrate III-V lasers with SiPh chips to make integrated compact optical transceivers. III-V lasers working at 1310 nm wavelength are cheaper and more stable. Therefore, in laser-chip integration applications, 1310 nm is more desirable in short reach communication systems.

In silicon photonics modulators at 1310 nm, there is a 30% weaker plasma dispersion electro-optic coefficient and a 35% lower absorption loss compared to 1550 nm. Silicon photonic waveguides have better light confinement at 1310 nm resulting in more compact SiPh structures. Figure 1.4 shows the simulated effective index of the first few TE and transverse magnetic (TM) modes in a 220 nm thick SiPh waveguide as a function of waveguide width. As shown, for a given width, the effective index of the mode at 1310 nm is higher than what we have at 1550 nm. This shows that the light is more confined in the waveguide at 1310 nm. Typical design values for a width of a single-mode waveguide are 0.35 μm and 0.5 μm at 1310 nm and 1550 nm wavelengths, respectively.

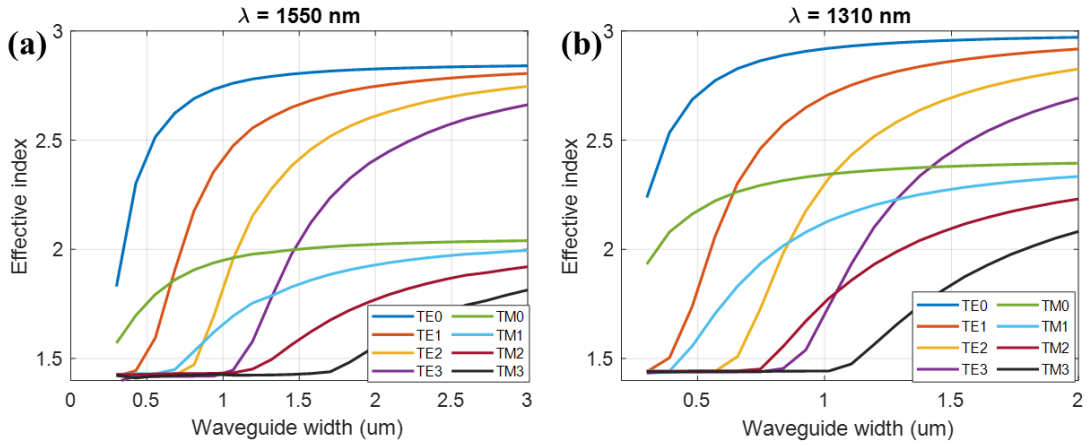

Fig. 1.3 Simulated effective index of the first three TE and TM modes in a 220 nm thick SOI waveguide as a function of waveguide width for (a) λ=1550 nm, and (b) λ=1310 nm.

Waveguides are the most basic elements in silicon photonic chips which guide the light. Their performance is evaluated by size and propagation loss. Propagation loss includes intrinsic loss (such as carrier absorption) and extrinsic loss such as sidewall scattering and radiation into the substrate. The intrinsic loss is the main source of the loss in doping-based waveguides, and radiation loss becomes significant when the size of the waveguide becomes small such as in the SOI platform (0.5 um) due to the roughness at the silicon interface [8]. The roughness in sidewalls and the top of the waveguides are different. The top of the waveguides usually has less roughness

as the design is patterned on pre-ready 220 nm-thick silicon wafers. The scattering loss in a common 500 nm-wide and 220 nm-thick waveguides are as follows [9]:

Table 1.2 Typical scattering losses in an SOI waveguide at λ =1550 nm [9]

	Straight 500 nm-wide waveguide	Bent 500 nm-wide 10 μm-radius waveguide
TE	5.9 dB/cm	7 dB/cm
TM	1.2 dB/cm	2.6 dB/cm

The TM electric fields exhibit vertical orientation touching the top surface of the waveguide while TE modes are oriented in the horizontal direction touching sidewalls of the waveguide. Figure 1.5 shows the scanning electron microscopy (SEM) of a fabricated SOI waveguide. As shown in Fig. 1.5, usually the sidewalls of a photonic waveguide have more roughness due to etching [10].

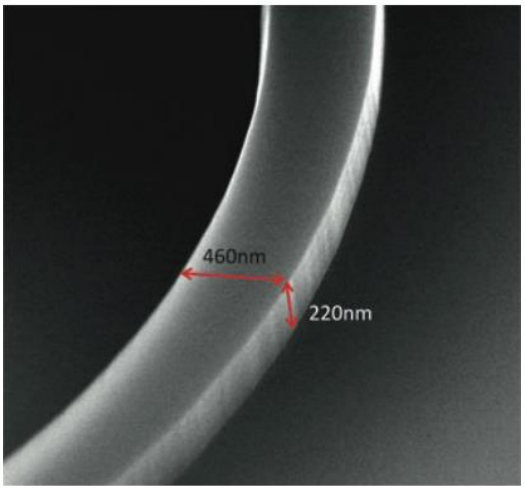

Fig. 1.4. SEM view of a fabricated photonic wire waveguide. The sidewall roughness is clearly visible [10].

Several approaches are currently available to smooth this sidewall roughness including thermal oxidation [11] and surface encapsulation [12, 13].

The strong confinement of light makes it possible to scale down the size of waveguide modes to about 0.1 um^2 which aligns with requirements for compatibility with CMOS modern technology. However, the mode of the single-mode optical fiber devices is typically about 80 um^2. The difference in dimension makes fiber-to-chip coupling challenging. The fiber to SiPh chips coupling can be generally split into two categories: edge couplers, and grating couplers. Edge couplers typically have broad bandwidth, low insertion loss, and low polarization-dependent loss (PDL); however, this requires additional expensive fabrication processes such as precise etching and edge polishing. Grating coupler devices offer lower coupling efficiency and bandwidth and are usually polarization-dependent. A comprehensive overview of different strategies for fiber-chip coupling is presented in [14].

Another promising alternative for the chip-to-chip and fiber-to-chip coupling is to use photonic wire bonds made by low index contrast polymer waveguides. Recently coupling loss as low as 0.4- dB between InP chips and SiPh chips has been demonstrated [15].

1. 2 On-chip laser sources in SOI platform

Laser light sources are a substantial element in optical data communication systems. The integration of on-chip laser sources on SiPh circuits can theoretically decrease the overall power consumption of the optical communication systems. However, the low cost and technically feasible integration of laser light sources into SiPh circuits are challenging. Various solutions are available to realize such an on-chip laser source including III−V compound semiconductors, Raman Si lasers, and Ge-on-Si lasers [16-18]. Raman Si lasers may be inexpensive and low loss on-chip sources. However, the realization of Raman Si lasers is hard because of the indirect bandgap of silicon [19, 20]. Recently minimization of fluctuations in frequency spacing between two high-quality resonant modes in a Raman Silicon Nanocavity Laser is investigated [18]. III−V

compound laser chips can be integrated with SiPh chips using various methods including external coupling, wafer bonding, and direct growth [21, 22]. Epitaxially growth is an attractive and low-cost approach since it enables higher integration densities [21, 23, 24]; however, heteroepitaxy usually suffers from the crystalline defect density issue due to the large lattice mismatch of the materials, polar-nonpolar nature of the materials, and difference in thermal expansion coefficients which degrades the device performance [22]. This approach is not compatible with standard CMOS technology. Additional thermal engineering is required to make thermal contact between the laser and substrate [25]. Moreover, preprocessing of the light sources before integration is not possible. Thus, a reliable controlled process is required to maintain a good yield. In contrast, in hybrid integration [26], pre-processed and tested III–V lasers and SiPh dies are placed either on top or next to it to each other and integrated.

1. 3 Silicon photonic for interconnect applications

The concept of optical interconnects in very large-scale integration (VLSI) was proposed in 1984 [27]. Interconnects include both communications within a multi-core processor and communication links between chips. The modern microprocessors constructed from micron-thick copper wires are as dense as one line per micron. Off-chip transmission links have a coarser density of one line per 200 microns [28]. Different materials have been used in realizing photonic interconnect including InP/GaAs (III-V), polymer, silica, silicon nitride, and SOI. The SOI platform is highly preferred since it is more compatible with the modern CMOS process; therefore, it can be fabricated in established CMOS foundries in the world resulting in mass-producible and high-yield integration of photonics and electronics in a single chip [29]. Also, the large index difference between core and cladding in SOI enables compact and dense photonic integrate (PIC) systems.

The application and scope of silicon photonic in VLSI systems have widely been investigated in recent years [27, 28, 30]. Silicon photonics is a viable alternative solution to achieve a compact, energy-efficient, and cost-effective platform for optical interconnect.

Because of the indirect bandgap of silicon, the realization of optical gain is difficult. Therefore, semiconductor optical amplifiers (SOAs), and laser diodes (LD) are usually implemented in the III-V platform and then integrated with the SOI platform as presented in Fig. 1.7 [31].

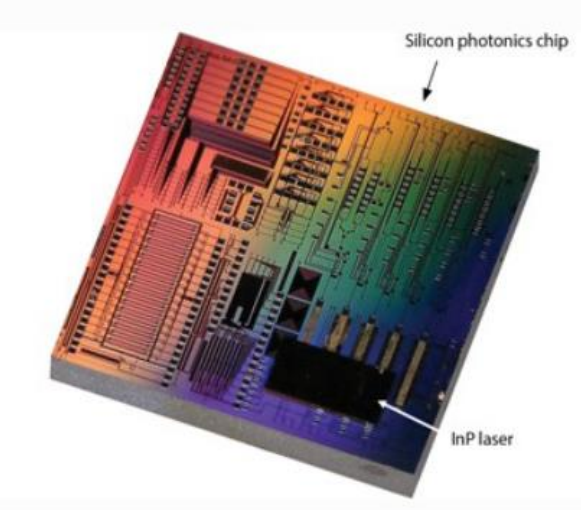

Fig. 1.5. Silicon photonics chip with 3-D hybrid integrated InP laser array [31].

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1. 4 Silicon photonic optical switches

Currently, electrical switches are playing a dominant role in data center switching applications. In electronic switching, the input optical data from the fiber is first converted to electrical signals using standardized transceiver modules (e.g., CFP2). The electronic signal goes through signal processing steps and switching, and then converted back to optical signals at the output using the same transceiver modules. However, there are several drawbacks to this platform. Indeed, the power consumption of the electronic switching systems is doubled every three years and

performance is degrading because of increasing temperature [32]. Two major drawbacks are mentioned here leading to that increase in power consumption.

1- These transceivers at both ends of each electrical switch bring significant additional power consumption to the system.

2- The platform is not well adapted to WDM technology. A pair of wavelength multiplexer and demultiplexers are needed at both ends of the electrical switch, demultiplexing each wavelength on a separate channel before the switch and, again, multiplexing data on a common channel after the switch. This makes the platform more complicated and, thus, adds to the overall power consumption of the system.

On the other end, optical switching does not require optical-electrical converter modules which greatly reduces the cost, power consumption, and overall complexity of the systems. In this platform, the energy consumption is aimed to be lowered to a picojoule-per-bit (PJ/bit) scale and the cost at the level of cents/Gb/s [32].

Typically, an MZI switch is constructed using two 3 dB couplers connected in series with two waveguide arms in between, as shown in Fig. 1.6. A phase shifter is fabricated on one of the arms to change the light phase. Silicon has an excellent thermo-optic effect (1.86×10^{-12} K^{-1}) [33] which helps us to realize thermo optic phase shifters. Further, the plasma dispersion effect and free-carrier absorption [34] help to realize p-i-n junction diode phase shifters. Thermo-optic MZI switches are demonstrated in [35, 36]. Owing to spiral phase shifters, power-efficient thermo-optic switches were demonstrated in [37-39]. A compact thermo-optic switch with a doped silicon heater with a switching time as fast as 2.4 µs is demonstrated in [40].

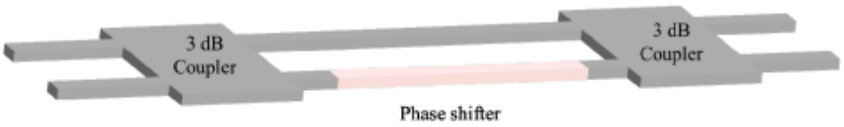

Fig. 1.6 A typical 2 × 2 MZI switch consists of two 3 dB couplers and a phase shifter [33].

Micro ring resonator (MRR) switches shown in Fig. 1.7 enable wavelength selective switching applications in WDM systems [41]. However, MRR-based switches are not a popular choice due to two significant challenges. First, the resonance wavelength is very sensitive to fabrication non-uniformities, and surrounding temperature changes; therefore, a thermal tuning heater is required to tune the resonance wavelength and compensate for the fabrication errors. Second, MRRs have low transmission bandwidth which limits the bandwidth of the whole system. To increase the optical bandwidth of MRR switches, high-order cascaded MRRs are demonstrated by different research groups [42-47].

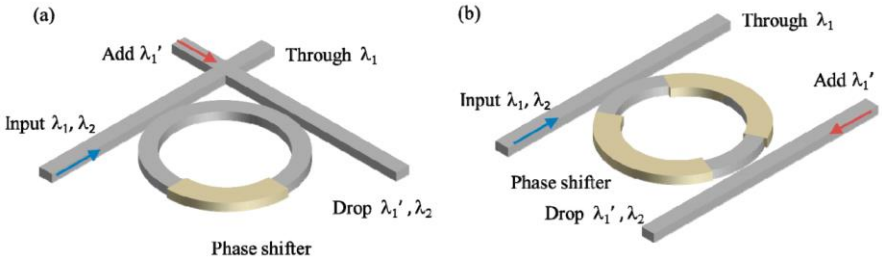

Fig. 1.7 Microring resonator-based switches with (a) crossed IOs; (b) parallel IOs [33].

Broadband optical switches play an important role in high-speed DWDM based optical communication systems. Using 2 × 2 bent directional couplers, a broadband switch is proposed using the metal heater and doped silicon waveguides in [48] and [49], respectively. Based on tapered adiabatic directional couplers, optical bandwidth more than 120 nm was demonstrated [49]. Using hybrid plasmonic waveguides broadband switching over 400 nm bandwidth was demonstrated in [50]. Bent directional couplers are sensitive to fabrication errors and adiabatic

directional couplers usually require long coupling length challenging their implementation in dense optical integrated circuits.

1. 4. 1 Silicon photonic multimode switches

Mode division multiplexing (MDM) is a promising technology to increase the bandwidth density over a single wavelength; thus, reducing the number of lasers and the overall power consumption. Multimode switches are attracting more and more attention recently. Various MDM-based switches are previously proposed. MDM switches based on MRRs are designed and characterized in [51, 52]. Using MMI couplers and a PN doped phase shifter, a high-speed mode switch for the first two TE modes is demonstrated [53]. Using MMI couplers and single-mode phase shifters, intermodal switching operations are proposed in [54]. A two-mode switch is also proposed based on densely packed waveguide arrays [55]. MDM-based matrix switches are proposed based on multiplexing/demultiplexing strategies [56-58].

The MDM switches which use demultiplexing – multiplexing strategy in the switching section usually require a high number of (de)multiplexers which adds to the overall insertion loss, modal crosstalk, sensitivity to fabrication errors, and complexity. For example, the 2 × 2 multimode switch in [57] consists of eight modes (de)multiplexers inside the switch and several multimode crossings which makes the structure design relatively complex. MDM switches based on MMIs usually have significantly longer lengths and narrower bandwidth [59]. MRR based multimode switches are compact, but still, have narrow bandwidth and sensitive to fabrication errors. For instance, the MMR-based switch demonstrated in [51] shows the high insertion loss of 9 dB over a narrow bandwidth of 13 GHz in characterization. One way to realize compact broadband switched based on MMIs is to use SWG structures which we study in this research. These SWG-

based multimode designs proposed here have multimode components and do not follow demultiplexing – multiplexing strategy.

1. 5 Motivation

Over the past decades, silicon photonics technology has received a great deal of attention. The unique properties of this technology such as ultra-high bandwidth capacity, low-loss transmission, immunity to electromagnetic fields, and lightweight have made this technology a viable solution in a wide range of applications ranging from communication systems to biosensors.

Non-blocking high radix switches play an important role in data center interconnects routing high-speed data packets between servers [60]. Silicon photonic optical switches which can be fabricated in available CMOS foundries have a compact footprint and low-loss performance, are a promising solution to ever-increasing bandwidth demand for both long-haul and short-reach interconnects.

For a large radix network switch, thermal management becomes challenging, and thermal crosstalk becomes important due to ineffective localized heating. Low-loss silicon photonic optical switches have been demonstrated [61-63]. However, further scalability and higher power efficiency of these switches are challenging to achieve due to the problems associated with large radix switches such as the increasing number of modulators, photodetectors, lasers, and I/O interfaces. Several multiplexing technologies including WDM, MDM, PDM are proposed to increase the bandwidth and data rate transmission to reduce the circuit complexity.

In the mode division multiplexing platform, multiple streams of data are sent through a multimode waveguide which significantly reduces device footprint leading to higher scalability. Low crosstalk, energy-efficient MDM structures can be implemented in the SOI platform due to its high index contrast between core and cladding. Therefore, integrated MDM switches can be a

feasible solution to realize scalable and energy-efficient optical switches. Compared to single-mode PICs, the multimode systems are more susceptible to intermodal crosstalk especially when the number of guided modes increases. Low loss and low crosstalk MDM switches which include three modes (TE0, TE1, TE2) have been successfully demonstrated [64]. Scaling the system to higher-order modes requires tight process variation control and reducing sidewall roughness.

MZI based switches are one of the most promising approaches to realize on-chip SiPh switches. The MMI power splitter is an important element in the MZI switch. Conventional multimode MMI power splitters have significantly large lengths as previously demonstrated in [59]. Also, the bandwidth of the structure is limited due to the dispersion characteristics of the silicon. Increasing the bandwidth of the optical switch can be useful to increase the number of WDM channels in a dense wavelength division multiplexing (DWDM) system. As a novel approach in the design of MDM switches, here, we use SWG-based multimode interference (MMI) structures in their design. The motivation of the thesis is to take advantage of the broadband response and compact footprint of SWG MMIs together with the advantage of doubling the data rate in a multimode MMI in SOI platform. As such, we design a compact broadband dual-mode insensitive MMI power splitter and multimode MZI building block, a crucial element in high radix PIC switches.

The term SWG is referred to a periodic arrangement of multiple optically transparent material (Si) at subwavelength scale with a period, Λ, which is small enough to avoid diffraction and reflection effects. As a result, the light can pass through the SWG structure with a low propagation loss. The period and filling factor of the structure is designed to control the effective index of the light propagating through the SWG waveguide and the equivalent refractive index of the medium. This control can be used to design various novel broadband and compact structures.

1. 6 Objectives and contributions

The objective of this thesis is to design and experimentally validate broadband multimode SiPh optical switch based on SWG MMI structures. The ANT process in which we wanted to fabricate our SWG designs is first characterized using FIB-HIM analysis. In particular, the effects of buried air gaps under the cladding of SiPh chip on SWG structures are studied and experimentally investigated. Results are presented in chapter 3. Then, the dual-mode SWG power splitter, an essential block in multi-mode switches, is designed and characterized in chapter 4. In chapter 5, the MMI power splitter is used in a dual-mode MZI switch. The switch is characterized using continuous wave (CW), and payload data transmission analysis. The contributions of this thesis are highlighted and summarized in the following:

- **Impact of SiO2 cladding voids in SiPh building blocks:** Buried air gaps (voids) under the SiO_2 cladding of SiPh chips may have a considerable impact on the performance of SWG designs. The voids in SiPh chips fabricated through the ANT center were characterized, and their impact was investigated by simulation and measurement. The volume of the buried air gaps depends on several factors including plasma-enhanced chemical vapor deposition (PECVD) of the SiO_2 cladding, the air pressure, the sidewall angles of Si blocks, and the distance between the two neighboring Si blocks. The void cross-sectional areas in the chips fabricated through the ANT electron beam lithography (EBL) process are evaluated and found to be less than 500 nm^2. The final investigation indicates that when the cross-section of the voids in a process exceeds 1500 nm^2, they have a considerable impact on the device's performance. In this case, the voids should be considered in the design phase or the foundry should modify the process specifications to reduce the voids. This work was done in collaboration with Dr. Jocelyn Bachman, and Dr. Cong Jin from ANT, and the results were presented at the IEEE Photonics Conference (IPC) 2020. The designs of the SiPh structures

for their characterizations were done by myself, Hatef Shiran. The characterization of voids in the ANT process using focused ion beam-helium ion microscopy (FIB-HIM) was done by Dr. Cong Jin and Dr. Jocelyn Bachman from ANT. I would like to thank Professor Odile Liboiron-Ladouceur and Dr. Hassan Rahbardar Mojaver for providing valuable insights and directions in this research contribution.

- **Design and characterization of dual-mode insensitive broadband compact SWG MMI power splitter:** MMI couplers are important elements in optical MZI switches. The mode insensitive compact MMI was designed in the SOI platform and characterized using CW measurements. The MMI has a broadband uniform response over 100 nm for the first two TE input modes. The total footprint is 42 μm × 5 μm. The overall structure exhibits 0.1 dB and 0.65 dB insertion loss for TE1, and TE2 over a 100 nm bandwidth in simulation. The measured crosstalk is less than -17 dB. The component is used in the design of the MZI switch in the following chapter. Part of this work was submitted to OSA Optics Express on March 12, 2021 (Manuscript submission ID 423882). The designs and characterizations were done by myself, Hatef Shiran. I would like to thank co-authors Mr. Guowu Zhang and Professor Odile Liboiron-Ladouceur for providing directions and vision during this research contribution.
- **Design and characterization of broadband compact three-mode insensitive MZI switch:** A compact broadband mode insensitive switch is proposed and experimentally demonstrated on the SOI platform using the compact broadband mode insensitive MMIs designed in the previous step with a mode insensitive phase shifter for on-chip MDM interconnects. The design simultaneously switches the first two TE modes over a 100 nm bandwidth centered at 1500 nm. Owing to the use of the SWG MMIs, the switch design footprint is reduced by 25%. The MDM system insertion loss is less than 1.6 dB and modal crosstalk is less than -13 dB. Payload transmission and BER measurements are also conducted using nonreturn-to-zero

pseudorandom binary sequence (PRBS-31) data signals at 10 Gb/s for single-mode transmission and simultaneous two modes transmissions. In all scenarios, open eyes are observed. A BER below 10^{-12} was observed both for single-mode and multimode transmission. The largest power penalty is 0.2 dB (4.2 dB) for single-mode (multi-mode) transmission. A manuscript is in preparation with a plan to submit to the IEEE Photonics Technology Letters. I would like to thank Dr. Kaveh Rahbardar Mojaver for the worthful tutorials on payload data transmission measurements, and for providing valuable directions regarding payload data transmissions in this work. Also, I would like to thank my supervisor for providing directions and guidance during the process.

1. 7 Organization of the thesis

The objective of the works presented in this thesis is to study the SWG structures with a focus on the MDM applications in a set of proof-of-concept experiments. Chips are fabricated through the ANT EBL process using 193 nm deep ultraviolet (DUV) lithography through cost-effective multi-project wafer (MPW) services.

In chapter 1, the need for optical interconnects in near future in terms of data rate and energy consumption was discussed. A brief overview of silicon photonics was also discussed. The research contribution of the candidate, Hatef Shiran, was presented.

Chapter 2 provides an overview of the background knowledge related to the subject of this M.Sc. research contribution. We discuss the theory and applications of the SWG structures. Second, the geometry, physics, and basic characteristics of periodic subwavelength grating structures are presented. In addition, an overview of the MDM on-chip interconnects systems is presented.

In Chapter 3, we describe the effects of buried air gaps in the cladding of SiPh chips on the performance of the SWG designs. First, their effects are described using Finite difference time domain (FDTD) simulations. Second, the voids under the cladding of SiPh chips fabricated through a commercial EBL process, ANT, are analyzed using the focused ion beam-helium ion microscopy (FIB-HIM) method and results are presented.

Chapter 4 describes the structure, theory, and measurement results of our work on a novel design of broadband mode insensitive compact broadband MMI that takes advantage of SWG structure in its design.

In chapter 5, an experimental demonstration of a dual-mode broadband MZI switch build using the SWG MMI designed in chapter 4 is presented. Theory and design are discussed. CW measurements and RF measurements are presented.

In chapter 6, a conclusion of the thesis is presented, and the key findings are highlighted and summarized. The challenges and scopes of the works presented in each chapter are discussed. Finally, future works to continue and improve the study in this thesis are presented.

Chapter 2

Background

Subwavelength grating (SWG) structures are opening more and more opportunities in the integrated SiPh platform. SWGs consist of a periodic arrangement of small silicon features with a period, Λ, much smaller than the wavelength of the input light. With such a small period, the SWG structure acts as a homogenous structure, and diffraction effects are suppressed and reflection effects do not constructively enhance each other. SWG structures help us to design and engineer the refractive index and dispersion of the medium to realize more advanced designs [65, 66]. These structures are utilized in a variety of applications including fiber-to-chip coupling [67, 68], wavelength multiplexing [69], polarization splitting [70, 71], among other innovations.

SWGs can be implemented on a standard SOI platform by standard lithographic patterning and etching alongside other conventional silicon components. They provide the ability to control the refractive index such as in the case of edge couplers [14], birefringence such as in the case of polarization splitters using SWG tilted MMI [72], and dispersion as in the broadband compact SWG MMIs [73].

The confinement of the light in an SWG waveguide is lower than in slab waveguides. Such low confinement allows for enhanced sensitivity to the changes in the cladding refractive index, which makes the SWGs an ideal candidate for integrated SiPh optical sensors [74], fiber edge couplers, and grating couplers with a large fiber mode, modulators, directional couplers, and polarization splitters.

2. 1 Principles and formulas

The schematic of a basis SWG structure is presented in Fig. 2.1. This is a periodic SWG waveguide in the *z*-direction consisting of segments with refractive index n_1 (typically Si), n_2 (SiO_2 cladding), and n_3 (SiO_2 Box). The variable Λ indicates the period of the structure, a and H represent the width and height of SWG features. The duty cycle of the SWG is defined as $f = \frac{a}{\Lambda}$.

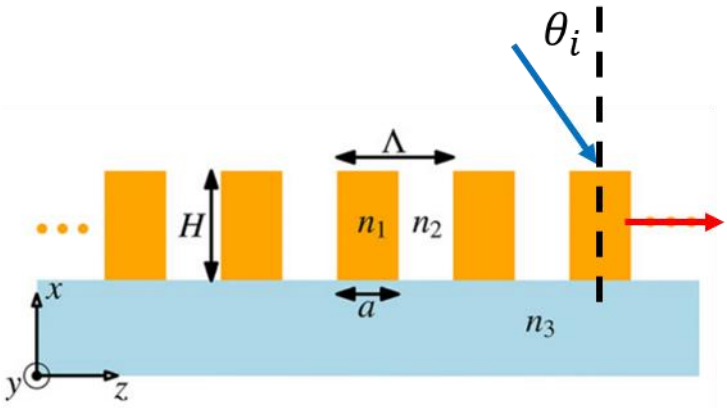

Fig. 2.1 Cross-section overview of a *z*-periodic waveguide where H is the height of the blocks, a is the width of the blocks, Λ is the period, and θ_i is the angle of incident light [66].

In the above geometry, we have two types of structures: (i) crosswise structures where light is polarized in *z*-direction and travels along the *x* or *y*-axis, and (ii) lengthwise structures where light passes through the *z*-direction and is polarized among the x or y-axis [66].

Suppose that the incident light is the blue arrow with the θ_i angle in the structure depicted in Fig. 2.1. Whether or not the diffraction order propagates along the *z*-direction is determined by the following grating equation [75]:

$$n_t \sin\theta_m - n_i \sin\theta_i = \frac{m\lambda}{\Lambda} \tag{2.1}$$

where $n_i = n_2$ is the incident medium refractive index, n_t is the refractive index of the transmitting medium where *m*th order is propagating. θ_m is the angle of the *m*th order diffracted light as measured from the grating's surface normal (black dash line in Fig. 2.1), λ is the incident light wavelength, and Λ is the period of the grating.

If all diffraction orders $m \geq 1$ are suppressed for a given free-space wavelength of the light, λ, and for all incident angles θ_i, up to a maximum angle of incidence θ_{max}, Eq. 2.1 can be formed into the inequality expressed in the following equation to give an upper bound for the grating period-to-wavelength ratio, $\frac{\Lambda}{\lambda}$ [75]:

$$\frac{\Lambda}{\lambda} < \frac{1}{n_t \sin\theta_m + n_i \sin\theta_{max}} \tag{2.2}$$

Diffraction orders propagate into the incident medium with refractive index n_2 or in the box with refractive index n_3 ($n_t = n_2$ *or* n_3). The inequality expressed in Eq. 2.2 is always satisfied, for all incident angles θ_i, up to a maximum angle of incidence θ_{max}, when the wavelength of the incident angle is less than the pitch of the periodic grating structure. With this condition, all diffraction orders $m \geq 1$ are suppressed, and the structure is called sub-wavelength grating.

2. 1. 1 Floquet-Bloch modes

For the lengthwise structure (when light travels through the *z*-direction in Fig. 2.1), its propagation is formulated using the Bloch–Floquet theory described in [76]. Propagation of the light, within a single period, through the segmented structure shown in Fig. 2.1 can be expressed as:

$$E(x, z + \Lambda) = E_B(x, z)\, exp(-\Upsilon_B \Lambda) \quad (2.3)$$

where E_B(x, z) is the Bloch mode electric field distribution and $\Upsilon_B = \alpha_B + j(\frac{2\pi}{\lambda})n_B$ is its complex propagation constant, where α_B and $k_B = (\frac{2\pi}{\lambda})n_B$ are the attenuation and propagations constants and n_B is the effective index of the Bloch mode.

The Υ_B, the complex propagation constant of the periodic structure, is highly dependent on the free-space wavelength, λ. The operation is generally divided into the following three regimes:

a) Subwavelength regime: at long wavelengths $\lambda > \Lambda$ (according to Eq. 2.2) diffraction orders will fail in phase matching with the guided modes inside the segmented region. Therefore, such diffraction orders will not exist. Also, when $\lambda \geq 2 \times n_B \times \Lambda$ repetitive back reflections do not enhance each other. Given this condition, the light propagates through the structure as such in conventional waveguides. This is called the subwavelength regime, and when $\lambda \gg \Lambda$, the structure operates in a deep subwavelength regime. In the subwavelength regime, as $\bar{\lambda} = \frac{\lambda}{\Lambda}$ decreases, the Bloch mode effective index n_B increases and the propagation constant $k_B = \frac{2\pi}{\lambda} n_B$ increases monotonically.

In this thesis, we are specifically interested in the subwavelength regime. When the wavelength of the light is much greater than the period of the blocks and the grating extends infinitely in x and

y directions, the SWG structure can be modeled by equivalent homogenous medium with the following refractive indices [66] given by Rytov's formulas [77]:

$$n_0^2 = \frac{a}{\Lambda}.n_{si}^2 + \left(1 - \frac{a}{\Lambda}\right).n_{sio2}^2 \tag{2.3}$$

$$\frac{1}{n_e^2} = \frac{a}{\Lambda}\frac{1}{n_{si}^2} + \left(1 - \frac{a}{\Lambda}\right).\frac{1}{n_{sio2}^2} \tag{2.4}$$

where n_0 and n_e are called ordinary and extraordinary refractive indices, respectively, and Λ is the SWG duty cycle and a is the width of silicon blocks. The n_0 is the effective index of fundamental TE mode traveling along *z*-direction and polarized along the *y* axis, and n_e is the effective index of the fundamental TE mode traveling along the *y*-direction and polarized along the *z*-axis. The diagonal refractive indices for TE polarization with the electric field along the y-direction can be written as:

$$n = diag[n^{xx}, n^{yy}, n^{zz}] = diag[n_e, n_0, n_0] \tag{2.5}$$

Rytov's formulas are based on the assumption that the ratio $\lambda/\Lambda \to \infty$ while the structure is infinite in the x and y directions. Higher-order approximations that improve the accuracy of the calculated effective refractive index for smaller values of wavelength to pitch ratio can be found in [78, 79]. When the structure is finite in the x and y directions, waveguide effects need to be considered, explained in [66]. In this thesis, as the structures are finite in lateral directions, for designing the SWG structures, the initial values are first calculated based on Eq. 2.4 and 2.5. Then the structure is further optimized using 3D FDTD methods.

b) Reflection regime: As shown in Fig. 2.2, in this regime, as the $\bar{\lambda} = \frac{\lambda}{\Lambda}$ is decreased, the n_B is decreased linearly and $k_B = \frac{2\pi}{\lambda} n_B$ remains constant with the wavelength to pitch ratios $\bar{\lambda}_1 < \bar{\lambda} < \bar{\lambda}_2$ and we have:

$$k_B = K_{Brag} = \frac{\pi}{\Lambda} \leftrightarrow \lambda = 2 \times \Lambda \times n_{B,Brag} \quad (2.7)$$

Successive reflections from the grating periodic structure can constructively strengthen each other creating strong Bragg reflections backward.

c) **Diffraction regime:** if the wavelength of the light is less than the pitch of the segmented waveguide, the power in the guided modes will be coupled out to the radiation modes out in the cladding or substrate, and the light is diffracted out of the periodic structure as shown in Fig. 2.2(d). This is called the diffraction regime. The Bloch mode effective index increases as the wavelength to pitch ratio $\bar{\lambda}$ is decreased.

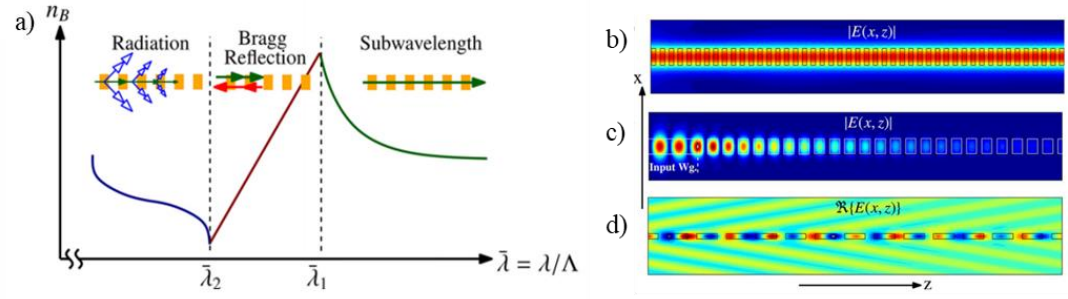

Fig. 2.2. (a) Floquet mode index (n_B) of a periodic waveguide as a function of the wavelength-to-pitch ratio $\bar{\lambda} = \frac{\lambda}{\Lambda}$. Propagation of light through the structure in Fig 2.1 while (n_2=n_3) for (b) subwavelength regime ($\lambda \gg \Lambda$) where the structure behaves as a conventional waveguide; (c) in the Bragg Reflection regime where $\lambda = 2 \times \Lambda \times n_{B,Brag}$, and light is reflected to the non-segmented waveguide; (d) for wavelengths near to the pitch of the structure, light is diffracted out and one diffraction order is propagating [66].

2. 2 Propagation and polarization-dependent loss

In theory, SWG structures are lossless in the lack of fabrication errors [80]. However, sidewall roughness in fabricated SWG structures results in scattering loss. It has been proven that SWGs propagation loss can be as low as 2.6 dB/cm which is comparable to conventional slab waveguides with polarization-dependent loss PDL as low as 0.5 dB/cm [80].

To integrate SWG waveguides and conventional strip waveguides, the optical mode in SWG waveguides and photonic conventional strip waveguides can be transformed into each other using an adiabatic coupler structure, as shown in Fig. 2.3. The operating principle of the coupler is a gradual modification of the grating period and duty cycle to gradually changing the effective index of light from the SWG section to match the effective index of the light in the strip waveguide section. The intrinsic coupler loss of 0.23 dB for TE polarized light and 0.48 dB for TM is reported in [65].

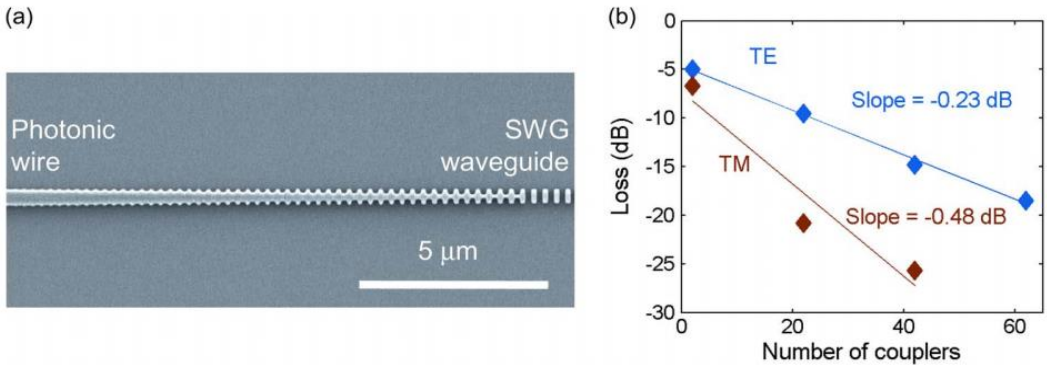

Fig. 2.3 (a) Scanning electron micrograph of SWG waveguide to strip waveguide coupling structure. (b) The measured transmission loss of concatenated coupling structures as a function of the number of couplers with linear fits [65].

We also have simulated the converter coupler loss for the first two lowest order TE modes (TE0 and TE1) using the commercial solver (Lumerical FDTD solution) as shown in Fig. 2.4.

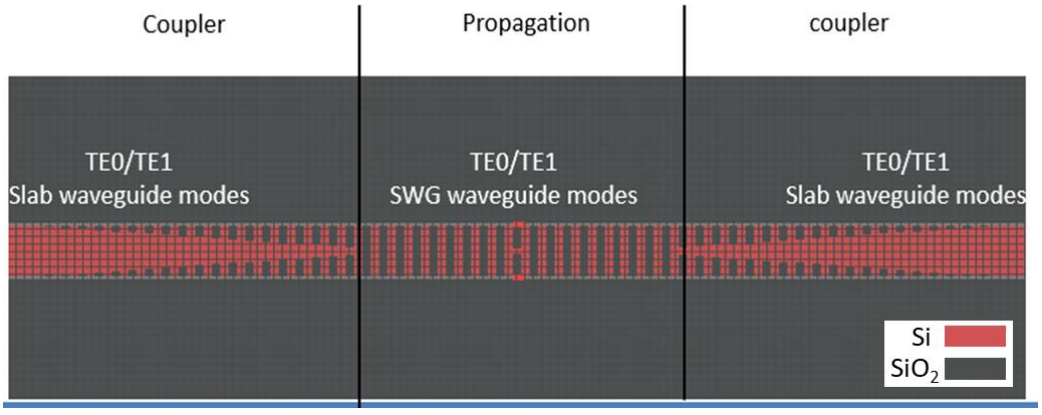

Fig. 2.4 Snapshot of the simulated structure in Lumerical FDTD solution.

In the above-shown structure, light in slab waveguide mode is injected from the left and measured from the right. The slab mode is passed through a coupler and couples to Bloch mode in the SWG section and then is coupled back to the slab waveguide mode using the coupler in right. Simulation results shown in Fig. 2.5 presents the coupling loss per one coupler for different coupler lengths (L_T) while the SWG waveguide length is maintained to 8 µm.

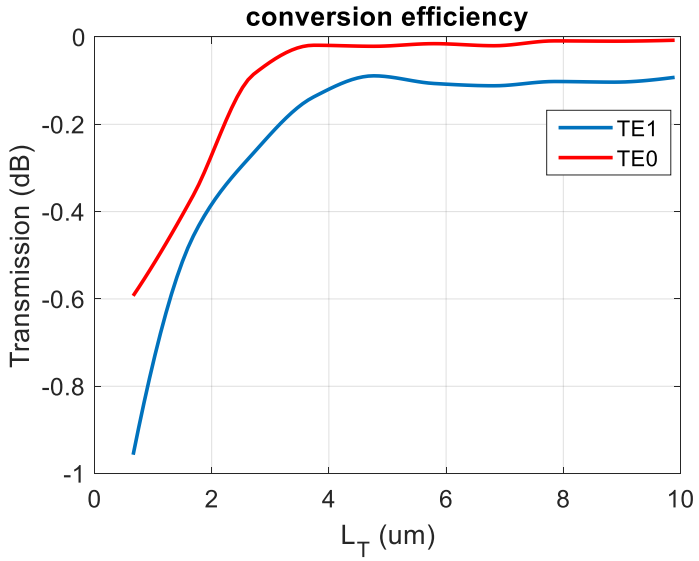

Fig. 2.5 Simulated transmission of the coupler for the first two TE input modes with respect to the coupler lengths.

This thesis studies the use of subwavelength grating structures in multimode systems such as power splitters and switches. A short background on MDM systems is presented in the following.

2. 3 Mode division multiplexing

MDM is a kind of space-division-multiplexing technique for enhancing the link capacity of data transmission with multiple mode channels [81]. One of the most important things in MDM systems is effective mode manipulation. Because of high-index contrast in silicon photonic, MDM silicon photonic is getting more and more attention as the effective mode manipulation is strong. Figure 2.6 presents dispersion curves for a typical silicon-on-insulator slab waveguide with a 220-nm-

thick top-silicon layer and 2 μm SiO_2 cladding. It can be seen that SOI strip nanowires usually have ultrahigh birefringence and very strong mode confinement.

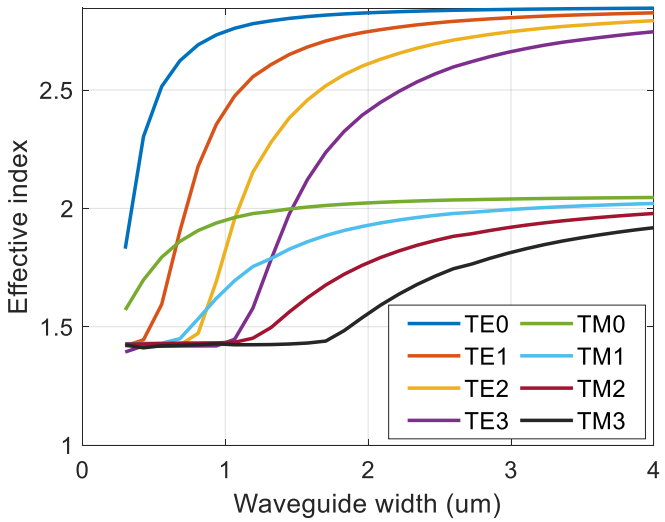

Fig. 2.6. Simulated effective index of the first three TE and TM modes with respect to waveguide width.

Therefore, the realization of low-loss and low crosstalk mode-selective manipulation for all the guided modes in a multimode SOI photonic wire is feasible although these guided modes are overlapped.

Over the past years, people have demonstrated various multimode silicon photonics structures including on-chip mode (de)multiplexers [82-85], multimode waveguide bends [86-88], multimode waveguide crossings [89], and multimode switches [53, 64, 90]. The great potential of MDM in increasing bandwidth density together with the advances in MDM silicon photonic structures shows that MDM silicon photonic is indeed a promising solution to increase data rates in chip-scale communication systems.

Figure 2.7 shows an example of an MDM communication link [91]. The incoming power from the CW on-chip laser source is divided by power 1×N power splitter where the N is the number of communication channels on which different data streams are modulated. The data can be passed

through a polarization rotator to double the data rate by exploiting TM and TE modes. Data is then converted to different modes by a mode multiplexer and then passed through the multimode switch. On the receiver side, data is then demultiplexed and converted to single modes and detected using on-chip photodiodes. As can be seen, by using MDM technology, a single multimode switch route the data compared with single-mode technology where four switches are needed to route such data. Thus, MDM systems, considerably have higher energy efficiency and more compact footprints.

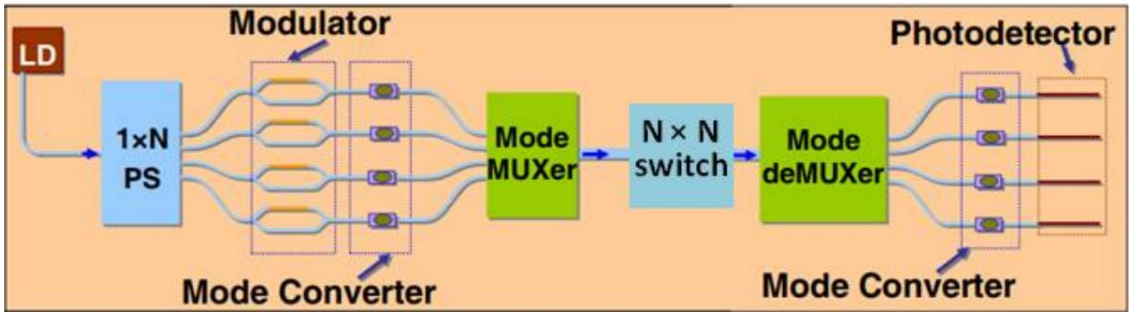

Fig. 2.7. Schematic of an MDM interconnect system [91].

There are various solutions to realize on-chip higher-order modes. The two most common methods are multimode grating couplers and mode (de)multiplexers.

Figure 2.8 shows the schematic of the on-chip mode multiplexing using the grating coupler method. In this method [92], optical HE_{11} coming out of fiber is coupled to the multimode grating coupler, and then light travels with TE_1 mode is the SiPh waveguide. In the second approach [82-85, 93], the grating coupler is single-mode, and light is coupled with TE_0 mode inside the SiPh waveguide. Later, light is passed through an on-chip mode multiplexer in which the TE_0 is converted to TE_1. The second approach is more desirable since it includes a simpler design, and the design is easily expandable to higher-order modes. The schematic of this method is shown in Fig. 2.9.

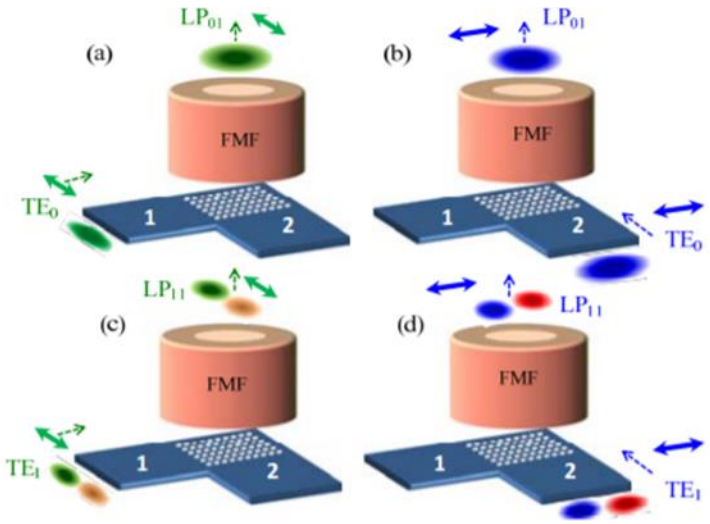

Fig. 2.8. Schematic of the multimode mode fiber grating coupler. TE0 light from (a) input 1 and (b) input 2 is coupled out from the grating and coupled to the LP01 modes of the few-mode fiber with different polarizations. TE1 light from (c) input 1 and (d) input 2 are coupled out from the grating and coupled to LP11 modes of the few-mode fiber with different polarizations [92].

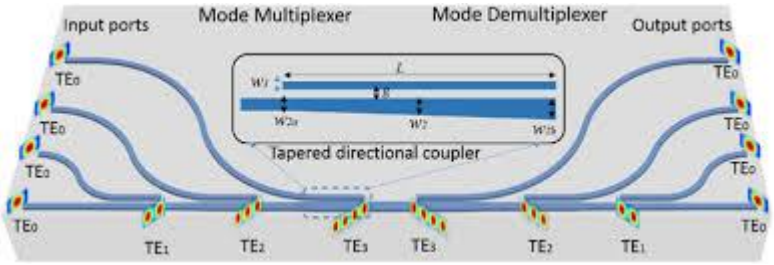

Fig. 2.9 Schematic of an on-chip four-mode MDM system [93].

2. 4 Summary and conclusion

In this chapter, the theory and principles of SWG structures are discussed. When the propagating light wavelength is more than the pitch size of the SWG structures, they act as a homogenous medium with low loss. SWG structures provide us with the ability to control the refractive index, birefringence, and dispersion of the guiding medium. Dispersion engineering helps us to design broadband structures. This is the design principle of the broadband designs presented in chapters 4 and 5.

In addition, the overview of MDM systems is presented. The most interesting benefit of MDM systems is the ability to modulate different data streams using a single-wavelength laser. One of the most well-known ways of realizing a multimode signal is using on-chip mode multiplexers. Realizing MDM systems in SOI platforms with low crosstalk is feasible due to the large index difference between the Si core and cladding.

The dispersion engineering characteristics of SWGs help us to make broadband MDM designs and the lower refractive index of the SWG medium helps us to design the compact multimode MMIs presented in chapter 4.

Chapter 3

Impact of SiO_2 Cladding Voids in SiPh Building Blocks

Buried air gaps (voids) in the cladding of SiPh chips, depending on their volume, have a critical impact on the performance of the SiPh building block such as SWG structures, directional couplers, and ring resonators. These voids can be considered in the simulation and design phase [73]. Since we wanted to characterize our SWG designs at the Applied Nanotools center in Alberta (ANT) center, we decided to analyze the voids in the cladding of ANT chips before submitting our final SWG designs. In this chapter, we present the analysis of the impact of buried air gaps in the SiO_2 cladding voids on SiPh building blocks using simulation and experiment. The voids in the cladding of chips were fabricated through a commercial EBL lithography process, ANT evaluated them using a focused ion beam—helium ion microscopy (FIB-HIM) analysis. Results show that the voids cross-section area in the ANT process is less than 500 nm^2. This work was done in collaboration with Dr. Jocelyn Bachmann, and Dr. Cong Jin from ANT who provided the FIB-

HIM imaging of the voids. Part of this work was presented at the 2020 IEEE Photonics Conference (IPC) [94].

3. 1 Introduction

Silicon-on-Insulator (SOI) substrates are used to fabricate silicon (Si) waveguides, which guide light. A layer of SiO_2 covers the Si waveguide as the cladding, protecting the silicon layer and engineering the refractive index difference. In several components such as SWG structures, fiber grating couplers, directional couplers, mode multiplexers, and ring resonator couplers, silicon structures in close proximity allow light to couple and permit engineering of the effective refractive index. In such cases, the SiO_2 upper cladding may not properly fill the gap between the silicon features, resulting in an air gap buried under the cladding. These air gaps, which we call voids, might change the experimental performance significantly depending on their volume, position, and shape. Their volume depends on the PECVD process of the cladding, and the distance between the silicon structures. The characteristics of the fabricated design can considerably be different from the design values if those voids are neglected in the design phase. Voids can be considered in the simulation and design phase [73]. Here, we investigate through simulations the impact of voids on some common structures including fiber grating couplers, directional couplers, and SWG MMI couplers. Experimental characterization of a broadband SWG MMI sensitive to voids fabricated through the ANT foundry is also presented.

Figure 3.1 shows an SWG structure, directional coupler, and ring resonator where there is a narrow gap between the silicon segments that the SiO_2 cladding may not be able to fill. The amount of trapped air is usually represented by the area of the void in the longitudinal cross-section area of the device $(x \times z)$ as indicated in the inset of fig. 3.1(a) with the light guided in the x-direction.

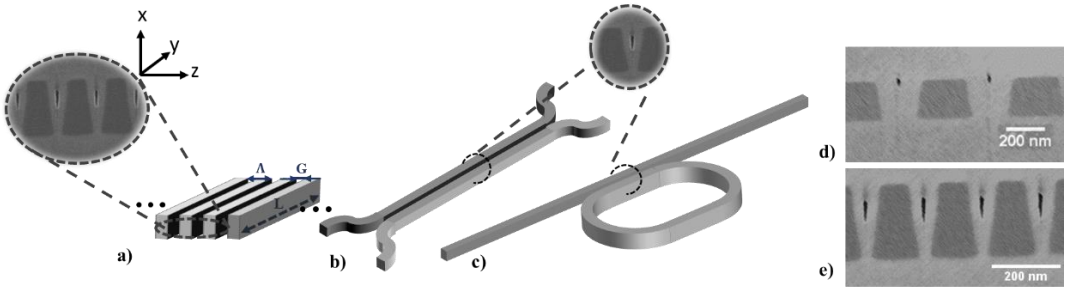

Fig. 3.1. a) A sub-wavelength grating structure where L is the length, G is the gap between the blocks, and Λ is the period of the grating; b) directional coupler; c) ring resonator. Insets: voids in the SiO_2 cladding measured via helium ion microscope (HIM) images of the voids in SiO_2 cladding prepared by a Ga-FIB from ANT. HIM images from ANT showing d) small voids; e) worst-case voids with an area less than 500 nm^2.

3. 2 Impact of voids on SiPh building blocks.

There are several SiPh building blocks susceptible to the impact of voids. Sub-wavelength grating couplers are among one of the most well-known solutions to implement fiber-to-chip coupling. Equation 3.1 presents the central wavelength (λ) as a function of the effective index of the SWG structure (n_{eff}), the refractive index of cladding (n_c), and the light output angle from cladding (θ_c) [95].

$$\lambda = \Lambda(n_{eff} - n_c \sin\theta_c) \tag{3.1}$$

The presence of voids lowers n_{eff} and, consequently, the central wavelength for a fixed output angle of light. Figure 3.1(a) shows the shift of the peak wavelength relative to different volumes of voids. The directional coupler presented in Fig. 3.1(b) usually has trenches with a width ranging from 100 nm to 150 nm. Results in Fig. 3.2(b) show the impact of voids on peak wavelength transmission. The SWG MMI shown in Fig. 3.2(c) is a solution to get ultra-broadband flat response over a 300 nm wavelength. However, the presence of voids causes additional loss, especially in the cross port of the MMI coupler. The structures are simulated with voids' area ranging from 3500 nm^2 to 7500 nm^2 which are realistic numbers in processes and reported in [73].

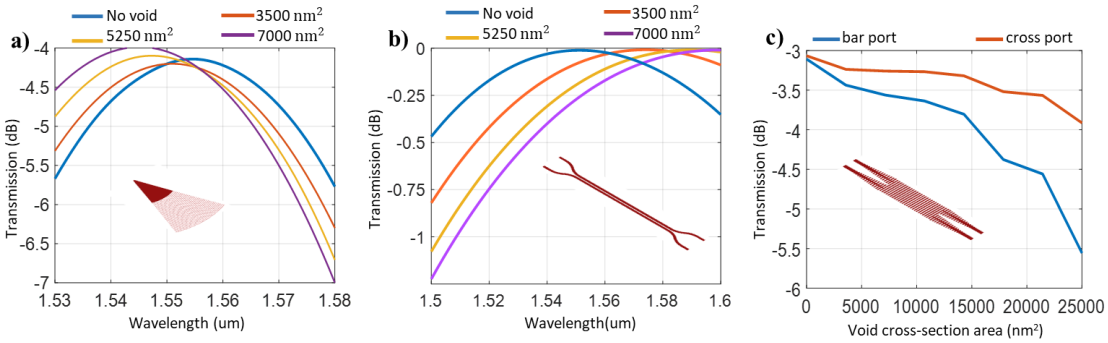

Fig. 3.2 Simulation results of the impact of voids for different SiPh building blocks: a) grating coupler; b) directional coupler; c) simulation of transmission response of an SWG MMI design with respect to different voids cross-section area at λ=1550 nm.

3. 3 Experimental results

To assess the presence of voids in the ANT process, the characterization of a broadband SWG 2 × 2 MMI power splitter is presented. The design in Fig. 3.3(a) is derived from [73]. The simulation results presented in Fig. 3.3(c) show the excess loss of the structure with respect to different void cross-sectional areas in the cladding of the structure. The voids are modeled in simulation as shown in Fig. 3.3(b). Characterization results of the fabricated structure (solid blue line in Fig. 3.3(a)) align with simulation results considering no voids in the cladding. We conclude that there is not a considerable volume of voids in the cladding. The later FIB-HIM study on sub-wavelength structures with various gaps (G in figure 3.1(a)) fabricated through this process confirmed this finding. It is worth noting that a thin coating of at least 10 nm of silicon dioxide on all silicon features may be preventing the voids from directly contacting the silicon features which likely reduces the impact of the voids.

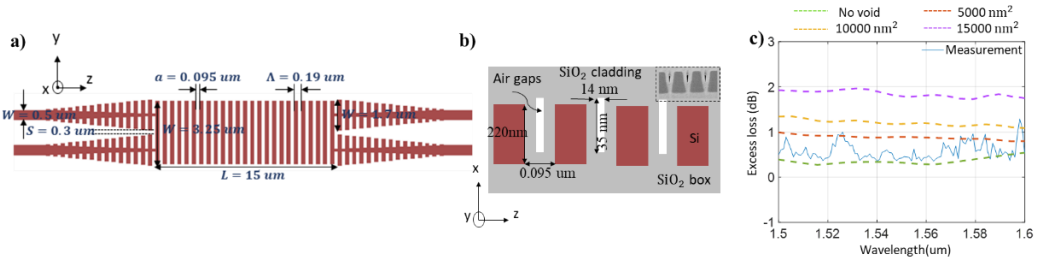

Fig. 3.3. a) The layout of the simulated and fabricated SWG MMI; b) side view of the structure showing modeled 15000 nm^2 upper cladding voids; c) measured and simulated performance of the broadband MMI where the blue line shows the experimental characterization of the structure fabricated through ANT and each dashed line represents the simulated excess-loss of the MMI considering different void cross-sectional areas in the upper cladding of the chip.

We investigated the impact of ANT voids on the performance of the dual-mode broadband compact MMI (DBcMMI) designed and characterized in chapter 4. The layout of the structure is shown in Fig. 3.4(a). The DBcMMI is a 3 dB power splitter that splits the first two TE input modes simultaneously. Since the structure is multimode design, the two most important factors in performance characteristics are the insertion loss and modal crosstalk. We considered 500 nm^2 air voids in the cladding of the structure the same way as presented in Fig. 3.3(b). Simulation results in Fig. 3.4(b,c) and show that such small voids will add to the insertion loss by 0.2 dBm. The modal crosstalk will increase from -40 dBm to -30 dBm which is not a significant impact on the performance of the structure.

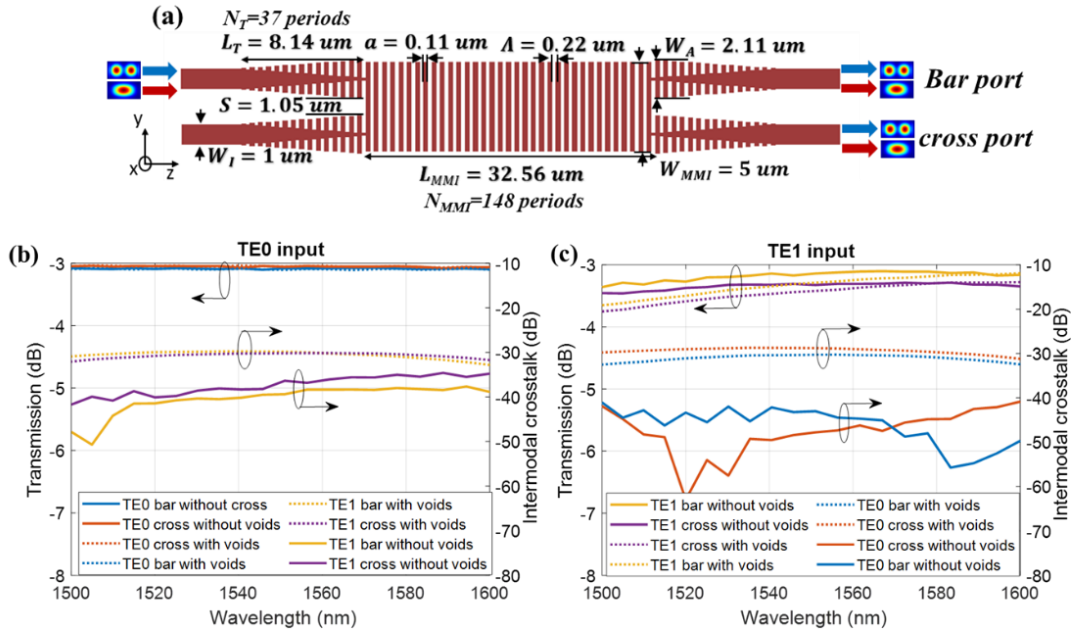

Fig. 3.4 (a) The layout of the simulated and fabricated SWG DBcMMI presented in chapter 4. Simulation results of the impact of ANT voids on the transmission of the proposed design in chapter 4 for (b) TE0 input; (c) TE1 input.

3. 4 Analysis of the voids in ANT chips

To characterize the voids in fabricated ANT chips, we took the structure shown in Fig. 3.4 which is covered by 2.2 µm SiO_2 cladding. The structure contains grating features with sizes ranging from 1 µm to 50 nm with an SWG duty cycle of approximately 50%. The built-up ion charges on top of the chip surface will affect the precision and resolution of the cutting line; therefore, a gold anti charging layer on top of the SiO_2 cladding layer is sputtered to reduce the charging effects during the cutting process. The structure is cut along the blue line using a focused ion beam and cross-sections are obtained using a helium ion microscope (HIM).

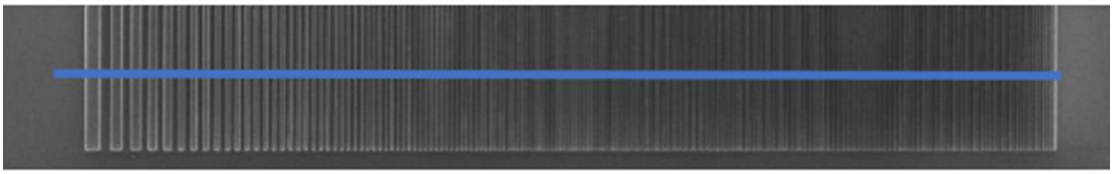

Fig. 3.5 Grating structures with sizes ranging from 1 μm to 50 nm (50% duty cycle). FIB cross-section is cut along the blue line.

The images were taken at a horizontal tilt of 1.45 degrees, which is why the images are rotated slightly. This introduces an error factor of 1.0003 to the horizontal measurements. In other words, the horizontal dimensions measured from the images should be multiplied by 1.0003 to obtain the true physical value. This is a very small error factor and is negligible.

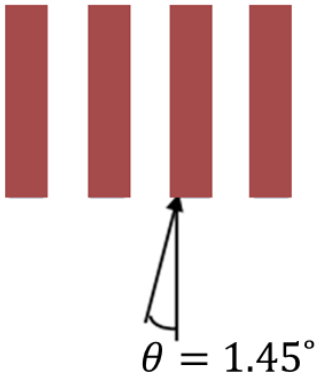

Fig. 3.6 Image angle of helium ion beam: 1.45 degrees

The vertical tilt of the images is 46 degrees. This adds an error factor of 1.39 to the images, which means that vertical measurements should be multiplied by 1.39 to account for the tilt of the sample.

Fig. 3.7. 46-degree vertical tilt

For the largest gratings, voids began to appear when the gratings are less than 316 nm wide, and the gaps are less than 293 nm wide. The first voids are between 10 nm to15 nm wide.

Fig. 3.8 Cross-section image of the voids when the grating size and spacing are 316 nm and 293 nm wide, respectively.

When the measured size and spacing of the grating couplers is 100 nm and 60 nm, the voids are between 8 nm and 11 nm wide. The voids are between 82 nm to 93 nm tall (corrected for tilt).

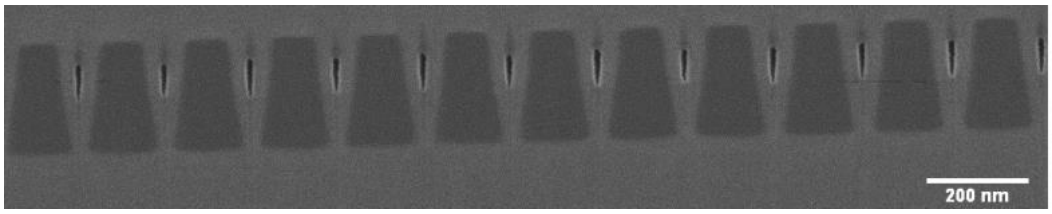

Fig. 3.9. Cross-section image of the voids when the grating size and spacing are 100 nm and 60 nm wide, respectively.

When the measured size and spacing of the gratings is between 60 nm and 70 nm, and the gap spacing is between 20 nm and 25 nm, the void width is between 5 nm and 12 nm, and the void height is between 70 nm and 90 nm (corrected for tilt).

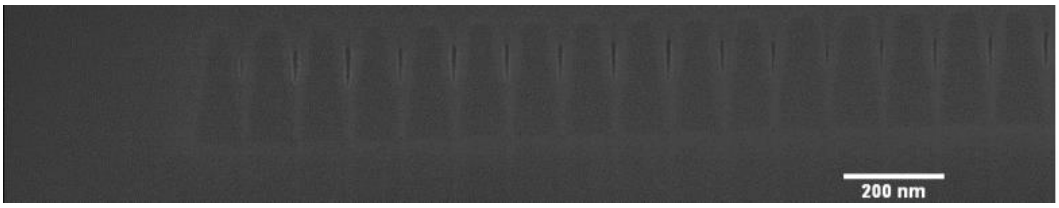

Fig. 3.10 Cross-section image of the voids when the grating size and spacing is 60-70 nm and 20-25 nm wide, respectively.

The width of the voids appears to be consistent as the grating width and spacing decreasing until the gratings become quite small. At this point, the smaller gratings have slightly narrower voids. The void height shows the opposite trend, with the height being very small for the wide gratings with large spacing, so that the voids appear nearly circular. As the grating width decreases, the voids become taller. In all cases, the voids do not directly contact the silicon. There is a thin

coating of at least 10 nm of silicon dioxide (SiO_2) on all silicon features, which likely reduces the effect of voids on the device's performance.

3. 5 Conclusion

The above-mentioned voids, depending on their volumes, may have a critical impact on SiPh designs where close proximity silicon blocks exist. Their volume depends on several factors including the distance between silicon blocks and the PECVD deposition of the fabrication process causing significant fabrication non-uniformity effects between processes. When the void cross-sectional area exceeds 1500 nm^2, they must be taken into account at the design phase.

Chapter 4

Broadband Compact Mode Insensitive MMI Power Splitter

As discussed in chapter 1, the multimode MMI power splitter is an essential component in MDM switches. We design and characterize a broadband compact dual-mode MMI power splitter based on SWG structures. The MMI works with the two lowest-order TE polarization modes. By engineering the dispersion characteristics, the optimized dual-mode MMI is three times more compact than its conventional mode insensitive MMIs and shows low loss and low crosstalk flat response over 100 nm bandwidth.

In recent years, people have developed various multimode silicon photonics structures including on-chip mode (de)multiplexers [82-85], multimode waveguide bends [86-88], multimode waveguide crossings [89], multimode switches [53, 64, 90], and multimode power splitters [96-100]. Among all, the multimode power splitter is the fundamental photonic building block to simultaneously split all the input modes with a 3 dB splitting ratio which is essential for multimode switching. Such power splitting is experimentally demonstrated by asymmetric

directional couplers in [96, 97]. However, such structures are wavelength sensitive due to the limited bandwidth of asymmetric directional coupler (ADC) structures. The adiabatic coupler (AC) can convert the input modes into the corresponding super-modes and realize the multimode power splitting with enhanced bandwidth [98]. However, the adiabatic mode conversion process requires a long coupling length (>800 μm). A waveguide integrated SWG transflecter simultaneously reflects and transmits light in [99]. However, the device length in the proposed structure is more than 300 μm challenging its implementation for applications such as photonic integrated switch matrices. In [100], such power splitting is achieved using a shallow etch MMI requiring two-step etching, adding to the complexity of fabrication. Noticeable in [98-100] is the relatively high intermodal crosstalk observed in simulation. As no experimental performance was reported for these structures, one may expect the intermodal crosstalk to be even higher in practice. In [97], the reported measured crosstalk is -15.7 dB, an insufficient performance for practical integrated MDM systems. Indeed, to maintain a BER of 10^{-12} for a 10 Gb/s NRZ payload transmission, the intermodal crosstalk should be less than -22 dB [101]. Therefore, the realization of a compact and broadband multimode power splitter with low intermodal crosstalk requires innovative solutions in their development.

In this chapter, we demonstrate an on-chip broadband multimode power splitter based on SWG MMI structures. The structure's total footprint is 5 × 40 μm. The total excess-loss and intermodal crosstalk is less than 0.4 dB (0.65 dB), and -32 dB (-17 dB) in simulation (experiment) for the two lowest TE modes (TE0 and TE1) over an optical bandwidth of 100 nm. The results demonstrate improvement in compactness, insertion loss, and intermodal crosstalk over past published works. Part of this work was submitted to OSA Optics Express journal for publication on 2021-03-12 under submission ID 423882.

4. 1 Design and working principle of the dual-mode SWG MMI

The SWG MMI is designed for the TE polarization using 220 nm-thick channel waveguides surrounded by a 2-μm buried oxide layer (BOX) and 2.2 μm oxide top cladding. The single-mode waveguide width is set to be 0.5 μm. The dual-mode waveguide width is selected to be 1 μm to support both TE0 and TE1. Fig.4.1(b) shows the simulated effective index as a function of waveguide width using a commercial CAD tool (Lumerical Mode solution) for the first three TE modes.

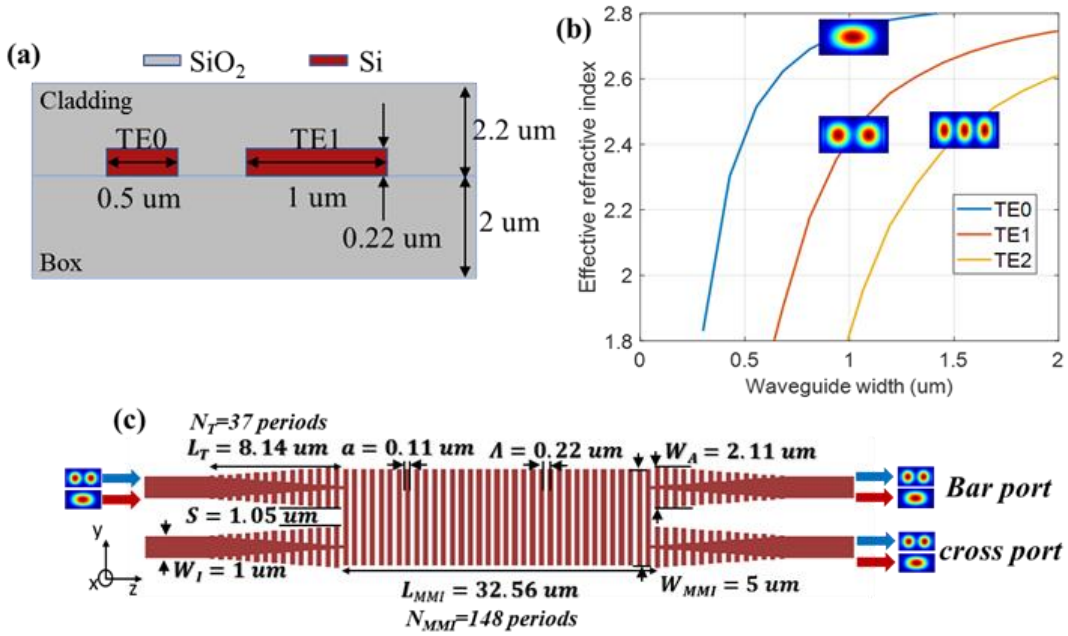

Fig. 4.1(a) Cross-section of single-mode waveguide (TE0), and dual-mode waveguide (TE1); (b) simulated effective refractive index as a function of waveguide width; (c) schematic of the proposed broadband dual-mode MMI power splitter.

Figure 4.1(c) schematically shows the dual-mode broadband compact MMI (DBcMMI) optical power splitter, where L_{MMI} and W_{MMI} are the length and width of the multimode region. N_{MMI} and N_T are the number SWG blocks in the multimode region and tapers, respectively. W_A is the width of the input and output tapers connecting to the multimode region (also referred to as the access waveguide width). L_T is the length of the input and output tapers which are separated by the

distance *S*. The pitch and width of the silicon blocks are noted by Λ and a, respectively. Light at any of the two input ports with TE0 and TE1 modes is passed through the structure and split at the output ports. The MMI is working following the general interference mode principle and optimized to generate two-fold images for two input modes. The principle for an MMI with multiple input modes has been previously derived in [102]. The input transverse electric modes, TEm where $m = 1$ or 2 representing the mode order, excite multiple modes in the MMI region. The input mode can be defined as the sum of all the excited modes:

$$\psi_m(x, y, 0) = \sum_{v=0}^{v=v_m-1} c_v \varphi_v(x, y) \tag{4.1}$$

where $\psi_m(x, y, 0)$ is the mode profile of order m in the input waveguide and $\varphi_v(x, y)$ represents the mode profile of order v in the MMI region. Due to the constructive and destructive interference in the multimode region, the N-fold images where integer N corresponds to the N^{th} formed at a deterministic MMI length. For general interference, the first N-fold images position forms at $3L_\pi/N$ where L_π is the beat length defined as follows for both input modes TE0 and TE1.

$$L_{\pi,q}(\lambda) = \frac{\pi}{\beta_0(\lambda) - \beta_1(\lambda)} \tag{4.2}$$

where β_0 and β_1 are the propagation constants of the fundamental and first-order modes, respectively in the multimode region. In the SOI platform used in this work, the waveguide thickness is 220 nm with modes that are formed in the horizontal direction with similar beat length. To find L_π, the propagation constants in the SWG multimode region of the MMI need to be calculated. The beat length depends on the wavelength as the propagation constant is a function of wavelength. The wavelength dependence of the beat length, Eq. (4.2), suggests that the MMI may

not be broadband. However, by the proper choice of the grating period, Λ, the dispersion of the SWG material is engineered to relax this dependency, *i.e.*, the denominator term, $\beta_1(\lambda) - \beta_2(\lambda)$, in Eq. (4.2) remains relatively constant from 1500 nm to 1600 nm wavelengths.

The effective refractive indices of the SWG anisotropic metamaterial can be obtained using effective medium theory [66, 103] as follows:

$$n_0^2 = \frac{a}{\Lambda}.n_{si}^2 + \left(1 - \frac{a}{\Lambda}\right).n_{sio2}^2 \tag{4.3}$$

$$\frac{1}{n_e^2} = \frac{a}{\Lambda}\frac{1}{n_{si}^2} + \left(1 - \frac{a}{\Lambda}\right).\frac{1}{n_{sio2}^2} \tag{4.4}$$

where n_0 and n_e are the ordinary and extraordinary refractive indices, respectively, and a/Λ is the SWG duty cycle where a is the width of silicon blocks. According to Eq. (4.3) and (4.4), the effective refractive index can be engineered by tuning the duty cycle.

The design parameters W_{MMI}, W_A, and S are initially set to values corresponding to the conventional dual-mode MMI design. The SWG pitch Λ is initially set small ensuring that the design works in the sub-wavelength regime. The initial value for L_{MMI} is calculated based on the above-presented formulas. The entire structure is finally optimized using Lumerical 3D FDTD simulations. By setting the SWG duty cycle $f = \frac{\mathrm{a}}{\Lambda}$ to be 0.5, the ordinary and extraordinary refractive indices are calculated based on Eq. (4.3) and Eq. (4.4). These values are imported into Lumerical Mode solutions and the propagation constants of the first two modes, $\beta_0(\lambda)$ and $\beta_1(\lambda)$, in the multimode region are calculated. The length of MMI, L_{MMI}, is initially approximate to be $3L_\pi/2$ according to Eq. (4.2) to form the first 2-fold image before performing the 3D optimizations. Figure 4.2 shows the simulated transmission obtained for the top input port to the

bar/top output port of the MMI for four possible pitch sizes. The result shows that for a pitch of 220 nm, the structure provides the flattest response for both input modes from 1500 nm to 1600 nm. According to simulations, the TE1 transmission is more sensitive to the changes in the beat length compared to TE0. A pitch of 240 nm does not lead to a relatively constant value for the beat length from 1500 nm to 1600 nm as the TE1 transmission deteriorates.

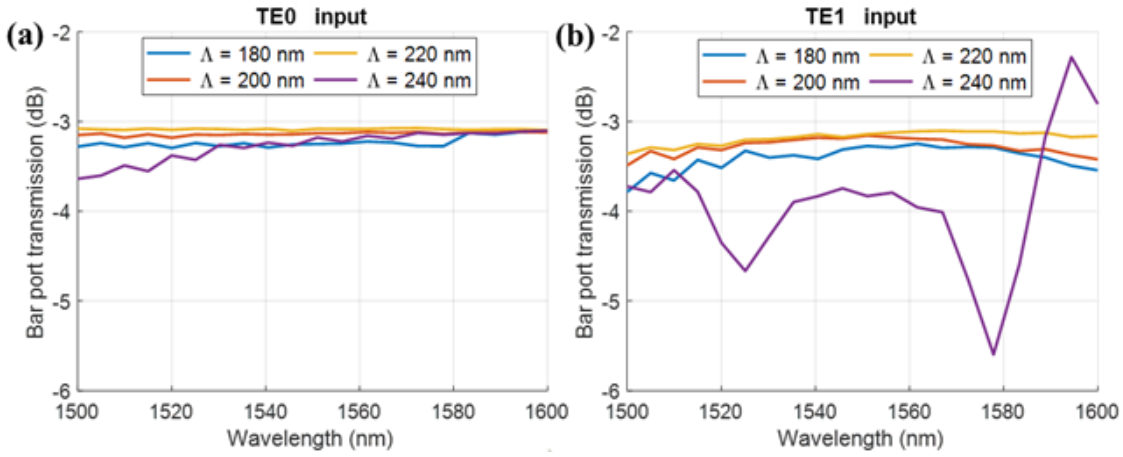

Fig. 4.2. Simulated transmission from the input port to the bar output port of the MMI with respect to different pitch sizes. (a)TE0 input; (b)TE1 input.

The adiabatically tapered input access waveguides are optimized next. The taper length is optimized to be long enough to ensure the transition of both input modes (TE0 and TE1) while kept compact. The taper length is optimized at $L_T = 8\ \mu m$ leading to less than 0.1 dB IL for both input modes.

We then optimized the access waveguide width W_A to support both modes. The separation S should be kept as small as possible; however, it also requires to be large enough to ensure that there is no coupling between the parallel input and output waveguides. Figures 4.3 and 4.4 show the simulation results for optimizing the W_A and S parameters. The design parameters are optimized to give the lowest possible loss and imbalance for both input modes. Results show that TE1 excess loss and imbalance are more sensitive to changes in design parameters. A higher number of modes

in the multimode region are required to create the 2-fold image for TE1 leading to higher sensitivity and loss. The TE1 slab to SWG waveguide mode conversion at the input and output tapers has 0.1 dB additional loss per conversion. This also contributes to a higher loss for TE1 mode.

The excess loss and imbalance used to characterize the MMI for each input mode where P_{in} the input power is P_{in} = 1 mW is defined as:

$$Excess\ loss_m = \left|10 \times log_{10}\left(\frac{T_{b,m} + T_{c,m}}{P_{in}}\right)\right| \tag{4.5}$$

$$Imbalance_m = 10 \times log_{10}\left(\frac{T_{c,m}}{T_{b,m}}\right) \tag{44.6}$$

where $T_{b,m,}$ and $T_{c,m}$ are the transmission power of the input mode with order m at the bar and cross output ports of the MMI, respectively.

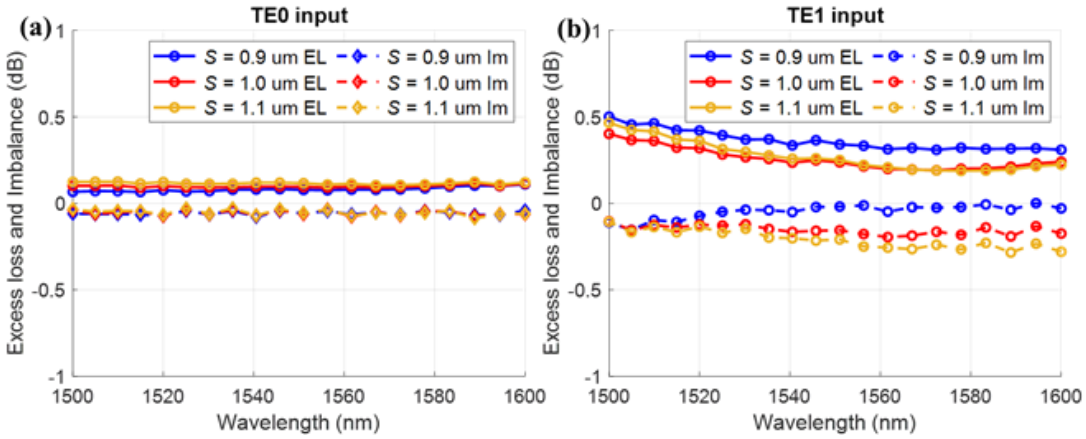

Fig. 4.3 Simulation of the excess loss and imbalance of the proposed design as a function of wavelength for different *S* design values while other parameters are kept constant as noted in Table. 1; a) TE0 input and b) TE1 input.

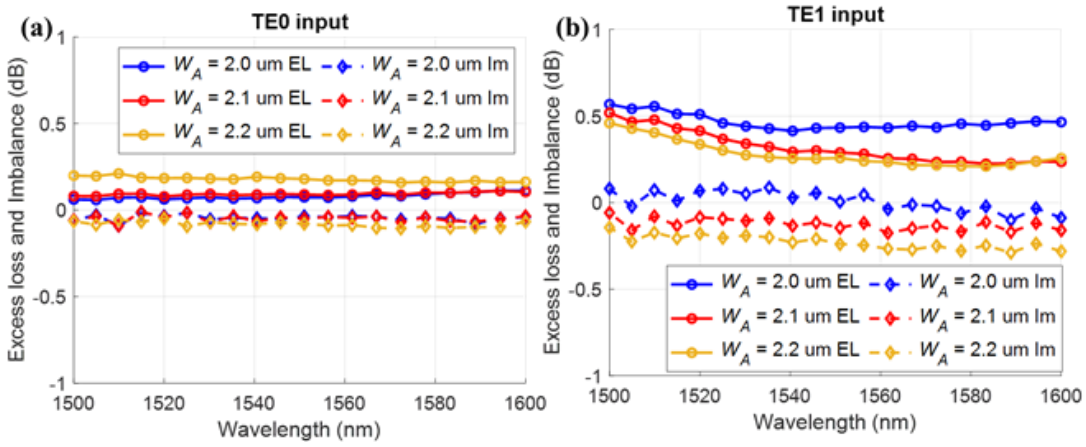

Fig. 4.4 Simulation of the excess loss and imbalance of the proposed design as a function of wavelength for different W_A design values, while other parameters are kept constant as noted in Table 1, (a) TE0 input; (b) TE1 input.

Careful calibration of lithography and etching is required to meet these duty-cycle and width specifications. The recommended minimum feature size and spacing in the foundry used is 70 nm. Therefore, the SWG duty cycle design value, *f*, should not be less than 0.32 or more than 0.68. In simulations, we observed that $f = 0.5$ has the lowest excess loss and imbalance for both input modes. Table 1 summarizes the final optimized values for the fabricated structure.

Table 4.1 Final optimized values of the proposed structure

Design Parameter	Optimized value (μm)
Input width (W_I)	1
Access width (W_A)	2.11
Taper length (L_T)	8.14 (N_T = 37 periods)
Input/output waveguide Separation (S)	1.05
Width MMI (W_{MMI})	5
Length MMI (L_{MMI})	32.56 (N_{MMI} = 148 periods)

Figure 4.5 shows the simulated electric field distribution for TE0 and TE1 input modes through the structure. The input mode profiles are reproduced at the output ports at the same relative position. Figure 4.6 shows the excess loss, imbalance, and modal crosstalk of the designed

structures for both input TE0 and TE1 modes over the 100 nm bandwidth from 1500 nm to 1600 nm. The highest modal crosstalk in simulation is -32 dB in Fig 4.6(a) likely caused by the non-perfect 2-fold imaging of the MMI. Ideally, a perfect 2-fold image of input modes is created at the output ports. However, in practice, the multimode region supports a finite number of modes which results in non-perfect 2-fold imaging.

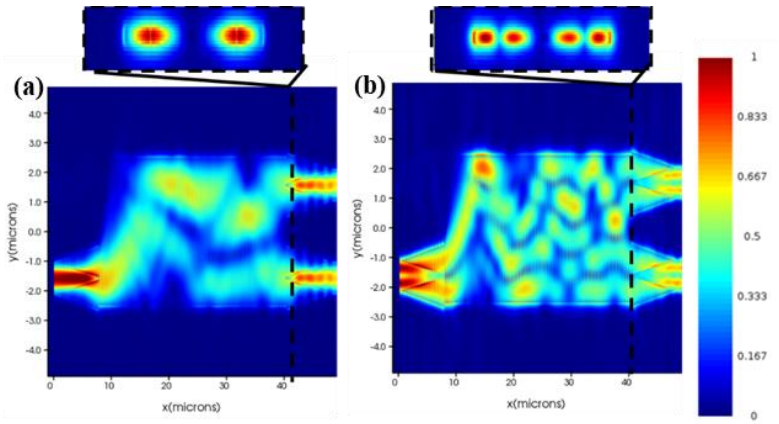

Fig. 4.5 Electric field propagation in the designed DBcMMI for (a) TE0 input; (b)TE1 input. Inset: The constructed 2-fold image at the shown cross-section, the end of the multimode section.

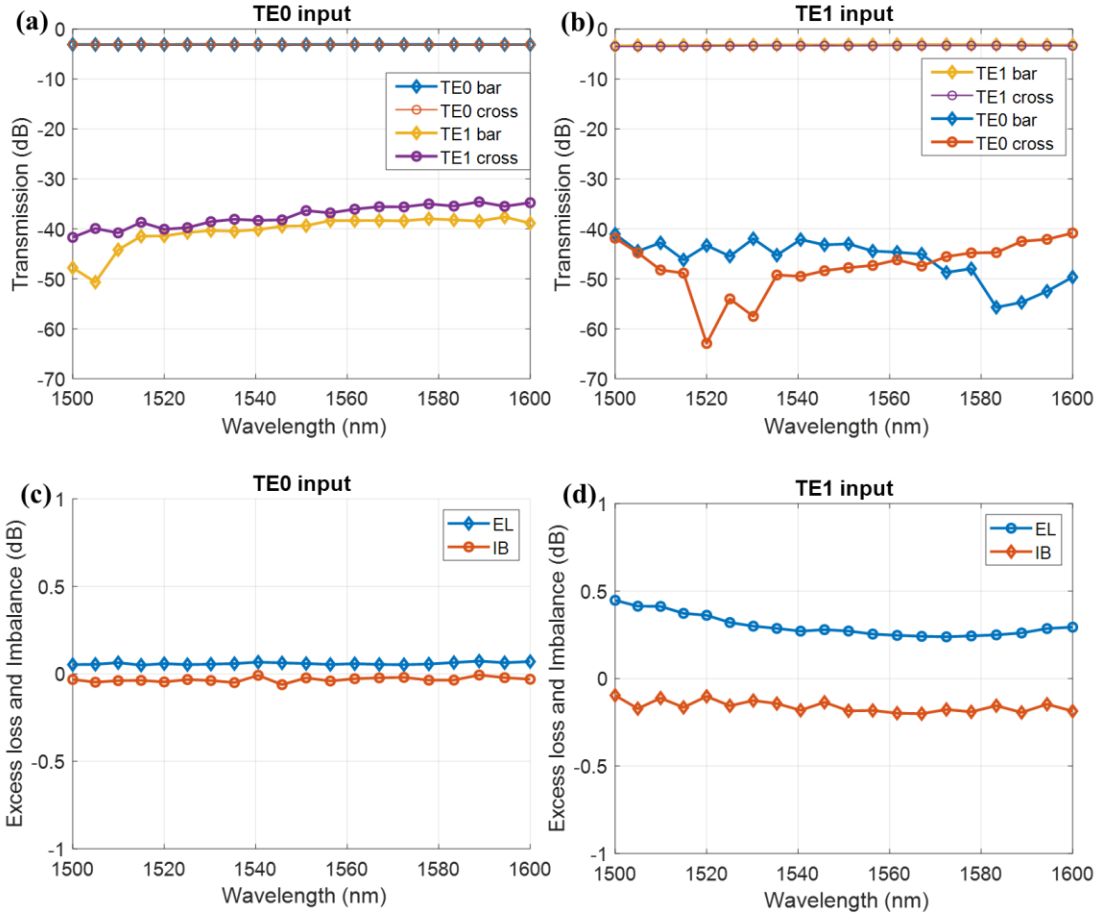

Fig. 4.6 Simulated transmission spectra of the proposed design for (a) TE0 input, (b) TE1 input modes; simulated excess loss and imbalance for (c) TE0 input, and (d) TE1 input modes

4. 2 Fabrication and characterization of the dual-mode broadband compact MMI

The DBcMMI is fabrication through Applied Nanotools Inc in Alberta (ANT), Canada. The silicon device layer is patterned using a 100 KeV electron-beam lithography (EBL) followed by an inductively coupled plasma-induced reactive ion etching (ICP-RIE) process. The design is characterized using continuous wave (CW) optical input. The polarization-controlled input light from a tunable C-band laser source (Yenista Tunics T100R) is swept from 1500 nm to 1600 nm. The light from the polarization controller (PC) is coupled into the chip using a grating coupler

(GC). To realize a multimode input signal, we used an on-chip mode (de)multiplexer before and after the structure as shown in Fig. 4.7. The light coming from the GC is multiplexed into TE0 and TE1 modes in a multimode waveguide and is passed through the DBcMMI design and then demultiplexed into two TE0 modes before coupling out to a fiber array for measurement. The output light from the GC is measured using an optical power meter (ILX Lightwave FPM- 8200). A single-mode waveguide connected to two single-mode surface grating couplers is fabricated on the same chip to normalize the loss of the design. The optical micrograph image of the fabricated structures is shown in Fig. 4.7.

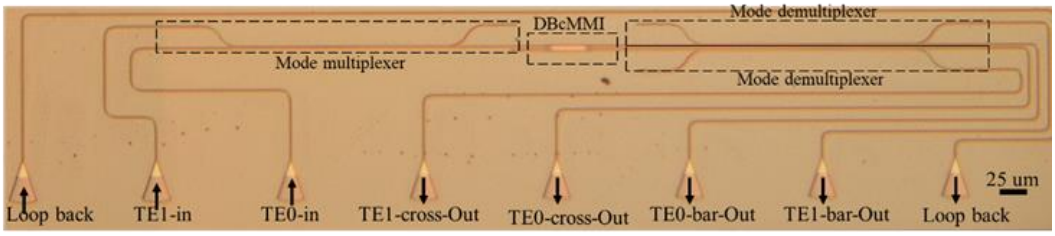

Fig. 4.7 Optical microscope image of the fabricated structure showing the mode multiplexer, power splitter, and the mode demultiplexers.

4. 2. 1 Optical transmission characterizations and intermodal crosstalk analysis

A test structure consisting of an ADC-based 2-mode multiplexer cascaded with a demultiplexer is first characterized by a CW optical input. The worst IL of the mode multiplexer is 0.34 dB and 1.04 dB for TE0 and TE1 input modes from 1500 nm to 1600 nm wavelength operating range, and the worst and highest crosstalk is 19.66 dB.

The normalized optical transmissions of the DBcMMI as a function of wavelength from 1500 nm to 1600 nm are presented in Fig. 4.8 (a) and (b) for TE0 and TE1 input modes. The measured excess loss of the DBcMMI for TE0 and TE1 input modes is 0.28 dB and 0.65 dB for TE0 and TE1 input modes, respectively, excluding the loss of the mode (de)multiplexers before

and after the DBcMMI. The modal crosstalk of the DBcMMI in the experiment is -17 dB. The modal crosstalk originates from the mode (de)multiplexers and the DBcMMI itself. To reduce modal crosstalk, further optimization of the mode (de)multiplexers is necessary.

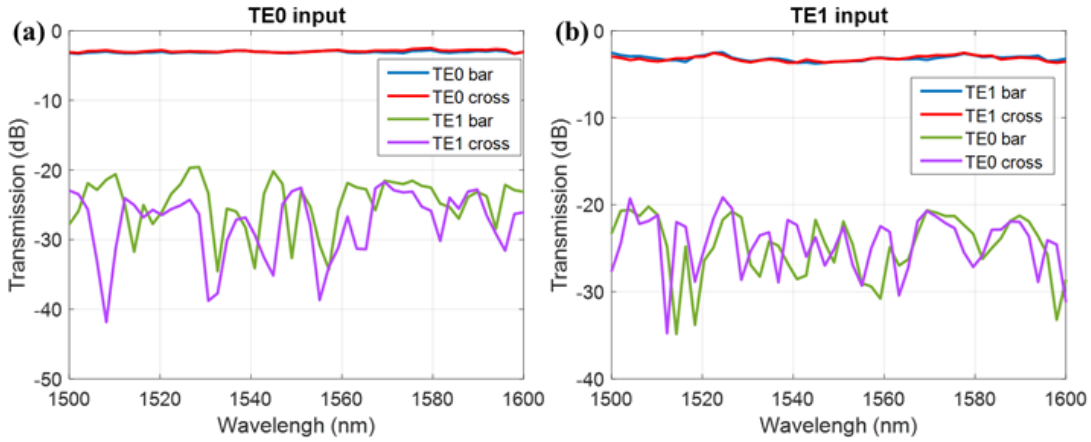

Fig. 4.8 Measured normalized transmission as a function of wavelength for (a) TE0 input; (b) TE1 input.

Recently, several mode-insensitive power splitters have been demonstrated [68-72]. The comparison is presented in Table 4.2. As shown, our characterized design has a more compact footprint, lower loss, and crosstalk, and a broader bandwidth compared to these works.

Table 4.2 Performance comparison of several multimode power splitters.

Ref	Number of modes	Device size (μm^2)	Excess loss (dB)		Modal crosstalk (dB)		Bandwidth (nm)	
			Simulation	Experiment	Simulation	Experiment	Simulation	Experiment
[96]	2	80 × 13	0.47	0.86	-28	-20	100	80
[97]	2	25 × 15	0.1	0.7	-17	-14.3	60	30
[98]	3	800 × 2.4	0.2	-	-18.5	-	180	-
[99]	3	300	0.5	-	-20	-	415	-
[100]	2	145 × 15	2	-	-21	-	100	-
This work	2	48 × 5	0.4	0.65	-32	-17	100	100

4. 2. 2 The sensitivity of the design and analysis of the crosstalk

We further investigated the origin of modal crosstalk in the DBcMMI using 3D simulation tools. The results show that the crosstalk induced by the DBcMMI is sensitive to the length of the multimode region (L_{MMI}). Figure 4.9 shows the simulation results of the transmission of the design with respect to the different number of SWG blocks (N_{MMI}) in the multimode section which relates to the length of the multimode region (L_{MMI}). From the results, we see that a small change in the number of SWG periods in the multimode region from 146 to 150 increases the modal crosstalk by 10 dB. Although the modal crosstalk is still low, the change is important as the modal crosstalk is a key factor in multimode systems to maintain a low BER. Due to the improper length of MMI (L_{MMI}), we have non-perfect 2-fold imaging at the outputs. The non-perfect field exits as higher-order modes, adding to the crosstalk.

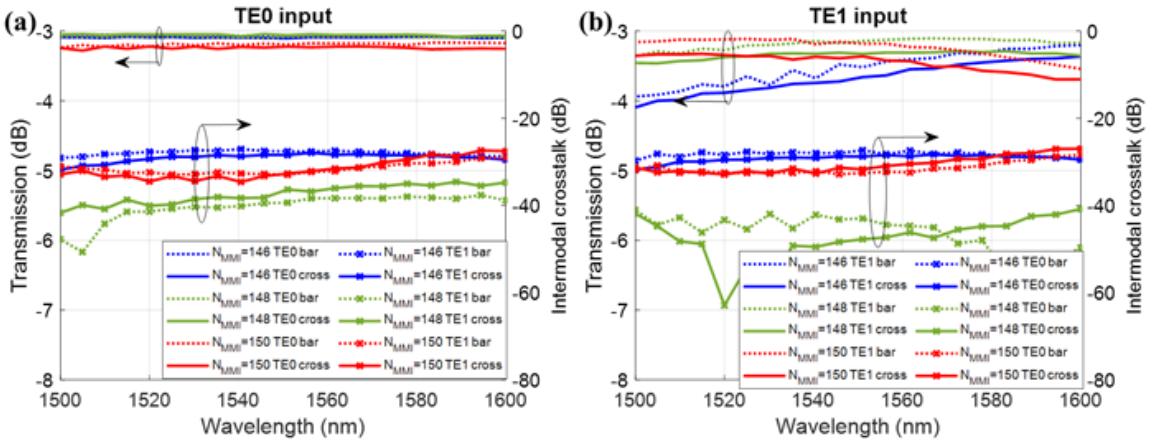

Fig. 4.9 Simulated transmission response of the DBcMMI for a different number of SWG blocks in the multimode section.

4. 3 Conclusion

To summarize this chapter, we designed and characterized a dual-mode broadband 2 × 2 power splitter using SWG structures which is the fundamental block for the MDM switch presented in the next chapter. The wavelength dependence of the beat length is inhibited by dispersion

engineering in the SWG structures. The footprint of the designed structure is as small as 5 μm × 48 μm (including the adiabatic taper-mode converters) which is small compared to other multimode power splitters. The measurement shows low insertion loss < 1 dB and low intermodal crosstalk < -17 dB for both input modes over a 100 nm bandwidth which is a significant improvement over past published works. By further optimizing the DBcMMI length and mode (de)multiplexers, the modal crosstalk can be improved. As the horizontal modes in a standard 220 nm-thick waveguides share a common beat length, the proposed multimode power splitter can be scaled up to split higher order TE modes (e.g., TE3 and TE4) by following the design procedure explained in section 4.1. We believe such a device could find its applications in the high-performance WDM-compatible multimode circuits. Part of this work is submitted for publication on OSA Optics Express journal on 2021-03-12 under submission ID 423882 with the manuscript title: Broadband compact 2 × 2 multimode optical power splitter using sub-wavelength metamaterial structures.

Chapter 5

Broadband compact dual-Mode switch

The broadband compact dual-mode MMI, previously presented in chapter 4, is the key element in multimode switches. A compact broadband mode insensitive switch is proposed and experimentally demonstrated on an SOI platform using the compact broadband mode insensitive MMIs, as in chapter 4, along with a mode insensitive phase shifter for on-chip MDM interconnects.

Various MDM-based switches are already proposed. MDM switches based on MRRs are designed and characterized in [51, 52]. Using MMI couplers and PN doped phase shifters, high-speed mode switch between two fundamental TE modes demonstrated in [53]. Using MMI couplers and single-mode phase shifters, intermodal switching operations are proposed in [54]. A two-mode switch is also proposed based on densely packed waveguide arrays [55]. MDM-based matrix switches are proposed based on multiplexing – demultiplexing strategies [56-58].

The MDM switches which use demultiplexing – multiplexing strategy in the switching section usually suffer from a high number of (de)multiplexers which adds to the overall insertion loss, modal crosstalk, sensitivity to fabrication errors, and complexity. For example, the multimode 2×2 switch proposed in [57] consists of 8-mode (de)multiplexers inside the 2×2 switch and lots of

multimode crossings which makes the structure design very complex. MDM switches based on MMIs usually have significantly longer lengths and narrower bandwidth [59]. MRR based multimode switches are compact, but still, have narrow bandwidth and sensitive to fabrication errors. For instance, The MRR-based MDM switch with more than 9 dB loss over a very narrow bandwidth of 13 GHz was is characterized [51]. One way to realize compact broadband MDM switches based on MMIs is to use SWG structures which make the design compact and broadband. These SWG-based multimode switch presented in this work has multimode components and does not follow demultiplexing – multiplexing strategy.

In this chapter, we design and experimentally demonstrate a broadband mode insensitive MZI switch that is capable of switching the first two TE modes, simultaneously. By taking advantage of dispersion engineered SWG MMIs, the switch operates over a 100 nm bandwidth centered at 1550 nm. By using a two-mode insensitive phase shifter, the modes share the same phase shifter resulting in low power consumption with the same V_{π}. The switch was designed in the SOI platform with a waveguide thickness of 220 nm and fabricated through the ANT center and characterized in our lab.

Switching of the first two TE modes consuming less than 250 mW power is demonstrated. The corresponding crosstalk is less than -13.4 dB (-13 dB) within a 100 nm wavelength range (1500 nm to 1600 nm) for the cross (bar) states, respectively. The whole system exhibits approximately 1.9 dB and 1.6 dB IL for the TE0 and TE1 modes at 1550 nm, respectively. Payload transmission and BER measurements are also performed using nonreturn-to-zero PRBS-31 data signals at 10 Gb/s for single-mode transmission and simultaneous two modes transmissions. For all scenarios, open eyes are observed. The BER less than 10^{-12} were measured both for single-mode and multimode transmission. The largest power penalty is 0.2 dB (4.2 dB) for single-mode (multi-

mode) transmission. Part of this work is in preparation with a plan to be submitted for publication at the Photonic Technology Letters journal.

5. 1 Design and working principle of the switch.

The cross-section of the waveguides for the single-mode and dual-mode as well as the TiW metal phase shifter is shown in Fig. 5.1(a).

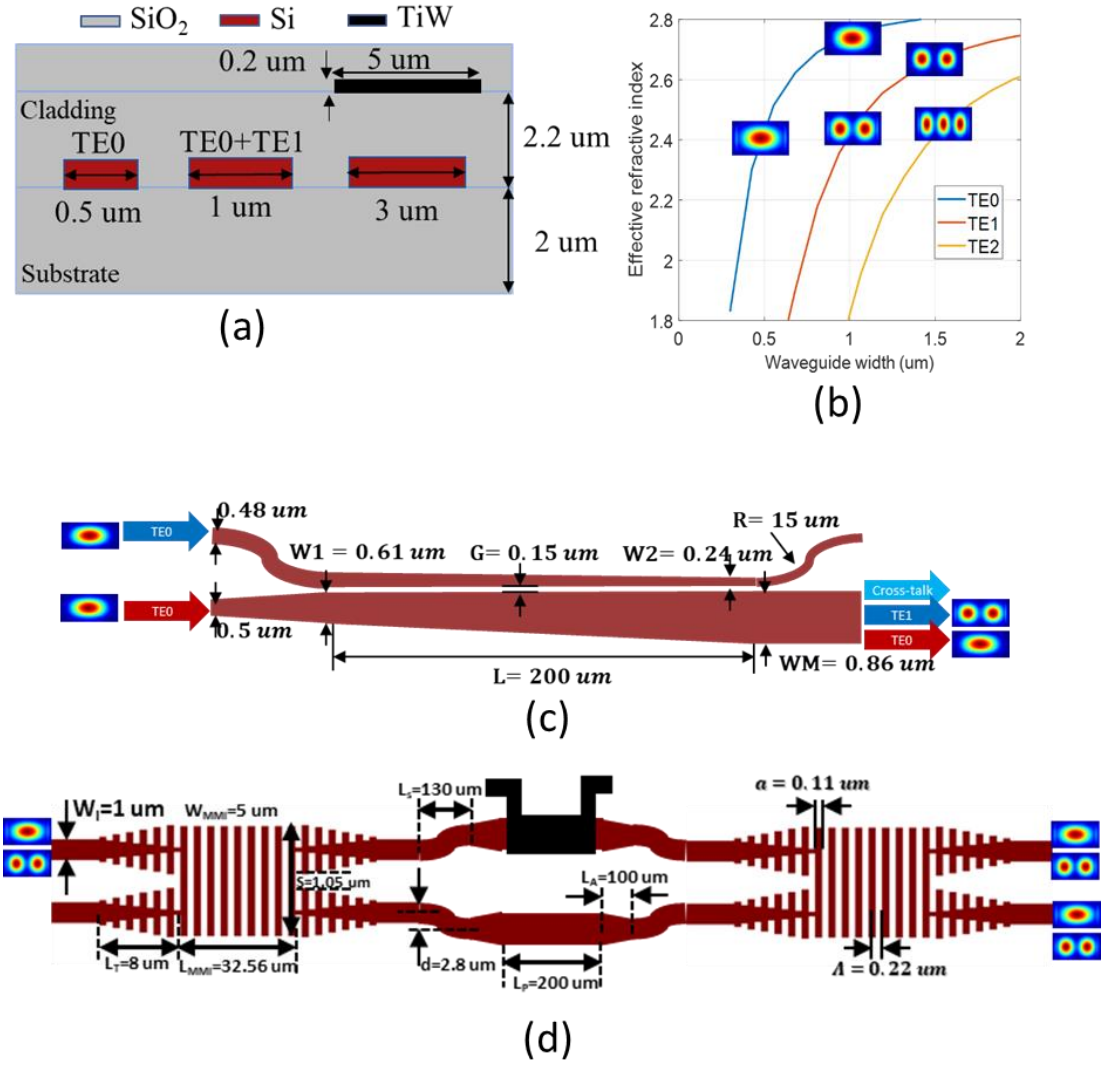

Fig. 5.1 Cross-section of the fundamental mode (TE0), and two-mode (TE0, TE1) waveguides and TiW phase shifter; (b) Simulated effective refractive index as a function of the width of the waveguide; (c) Schematic of the mode (de)multiplexer; (d) Schematic of the proposed dual-mode broadband compact MZI switch.

The waveguide widths for TE0 and TE1 are optimized to be 0.5 μm and 1 μm, respectively, according to eigenmode simulation using a commercial CAD tool (Lumerical Mode solution) as shown in Fig. 5.1(b). The input optical beam is converted to higher-order mode optical beams using the mode multiplexer shown in Fig 5.1 (c). The output beam of the mode multiplexer enters into the dual-mode broadband compact switch (DBcS) as illustrated in Fig 5.1(d). The DBcS consists of two DBcMMI designed and characterized in chapter 4, S-bends, and dual-mode phase shifters. The distance between the outputs of the DBcMMI is increased using a multimode S-bend to make sure the separation of the two arms of MZI is large enough for low thermal crosstalk. The radius and length of the S-bend are chosen to be 900 μm and 130 μm, respectively, to lower the intermodal crosstalk while keeping the footprint as low as possible. Then, the dual-mode phase shifter is used to change the phase of both TE0 and TE1 modes, simultaneously. The output of the phase shifter is then connected to the same DBcMMI again. The output of the switch is then demultiplexed using the same structure that was used to multiplex the input modes. The details on the design and characterization of the DBcMMIs are discussed in chapter 4. The S parameters of the DBcMMI and phase shifter and S-bends are simulated using the commercial tool (Lumerical FDTD) and imported to the Lumerical Interconnect solution to simulate the DBcS performance. Figure 5.2 represents the simulated transmission performance of the DBcS as a function of wavelength for both input modes.

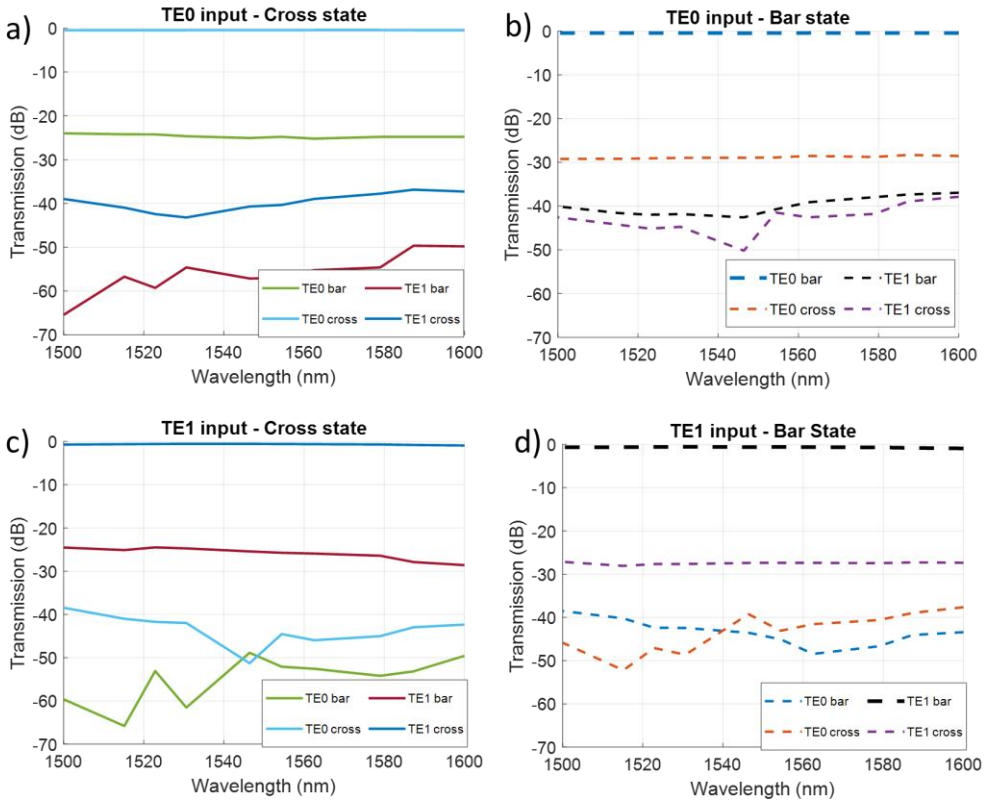

Fig. 5.2 Simulated transmission performance of the DBcS in bar-state and cross-state for: (a) TE0 input cross-state; (b) TE0 input bar state; (c) TE1 input cross-state; (d) TE1 input bar state.

The approximate losses for TE0 and TE1 input modes are 0.5 dB and 1 dB, respectively. As discussed in chapter 4, part of the loss for TE1 input originates from the mode conversion of TE1 strip waveguide to TE1 SWG waveguide using tapers at the input and output arms of the DBcMMIs. Exerting TE0 and TE1 input modes, the highest crosstalk values are -24 dB (-30 dB) and -23 dB (-28 dB) for the cross (bar) states, correspondingly. Ideally, a perfect image of the input modes is expected to be created at the output ports of DBcMMIs. However, in practice, the MMI region only supports a finite number of modes resulting in non-perfect imaging. Due to the existence of non-perfect imaging, the output field contains undesired modes adding the crosstalk.

We deployed the same design procedure as in our previous work [59] to design the dual-mode phase shifter. We designed the waveguide width under the phase shifter to be 3 µm so that the

$\frac{dn_{eff}}{dT}$ for both TE0 and TE1 input modes corresponds almost to the same value with less than 2% difference. We chose the width and length of the heater to be 5 μm, and 200 μm, respectively, to keep the phase shifter mode insensitive while minimizing the heater power consumption. The cross-section of the heater is shown in Fig 5.1(a).

5. 2 Fabrication and characterization of the DBcS

The DBcS is fabrication through Applied Nanotools Inc in Alberta, Canada. The silicon device layer is patterned using a 100 Kev EBL followed by an inductively coupled plasma-induced ICP-RIE process. The TiW thin film as a metal heater and aluminum thin film for metal routing is deposited using electron beam evaporation. A thin (300 nm) SiO_2 passivation layer is deposited by chemical vapor deposition (CVD) to protect the metal layers. The footprint of the proposed DBcS structure is 1800 μm × 140 μm. The optical micrograph image of the fabricated structures is shown in Fig. 5.3.

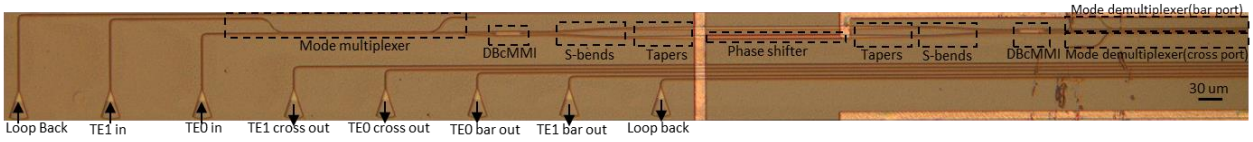

Fig. 5.3. Optical microscope image of the fabricated structure showing the mode multiplexers, power splitters, S-bends, tapers, and the mode demultiplexers.

The design is characterized using CW optical input. The polarization-controlled input light from a tunable C-band laser source (Yenista Tunics T100R) is swept from 1500 nm to 1600 nm and light is measured using an optical power meter (ILX Lightwave fpm-8200). Straight single-mode waveguides connected to two single-mode surface grating couplers were fabricated on the same chip around the structure. All CW measurements are normalized to the loopback structure. The measured IL for the loopback structure is approximately -15 dB at 1550 nm.

Figure 5.4 shows the normalized output power of the DBcS as a function of applied voltage at 1550 nm. The TE0 and TE1 modes coming out of the mode multiplexer are fed to the upper port of DBcS. When no voltage is applied to the phase shifter, the DBcS works in the cross-state and both modes will be directed to the lower port of the switch. The switch bar state requires the phase of the light in one of the MZI arms to be changed by π which is performed by applying a proper voltage V_π to the phase shifter. In the cross-state, the TE0 extinction ratio (ER) is at most 20 dB when the input voltage is 1.18 V, and the TE1 ER is at the maximum of 38 dB when the input voltage is set to 0.92 V. In the bar state, the TE0 ER is at most 37 dB when the input voltage is 3.28 V, and the TE1 ER is at most 29 dB when the input voltage is set to 3.22 V.

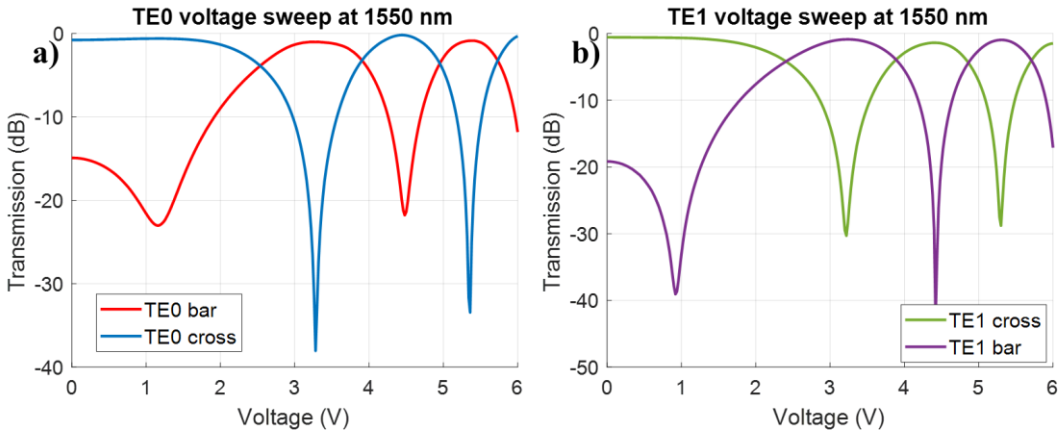

Fig. 5.4. Measured normalized transmission response as a function of applied voltage for (a)TE0 input; (b)TE1 input.

Figure 5.5 shows the corresponding transmission spectrum response of the switch when the switch is working in cross and bar states. A bias voltage of 1 V and 3.22 V is applied when measuring cross and bar states, respectively.

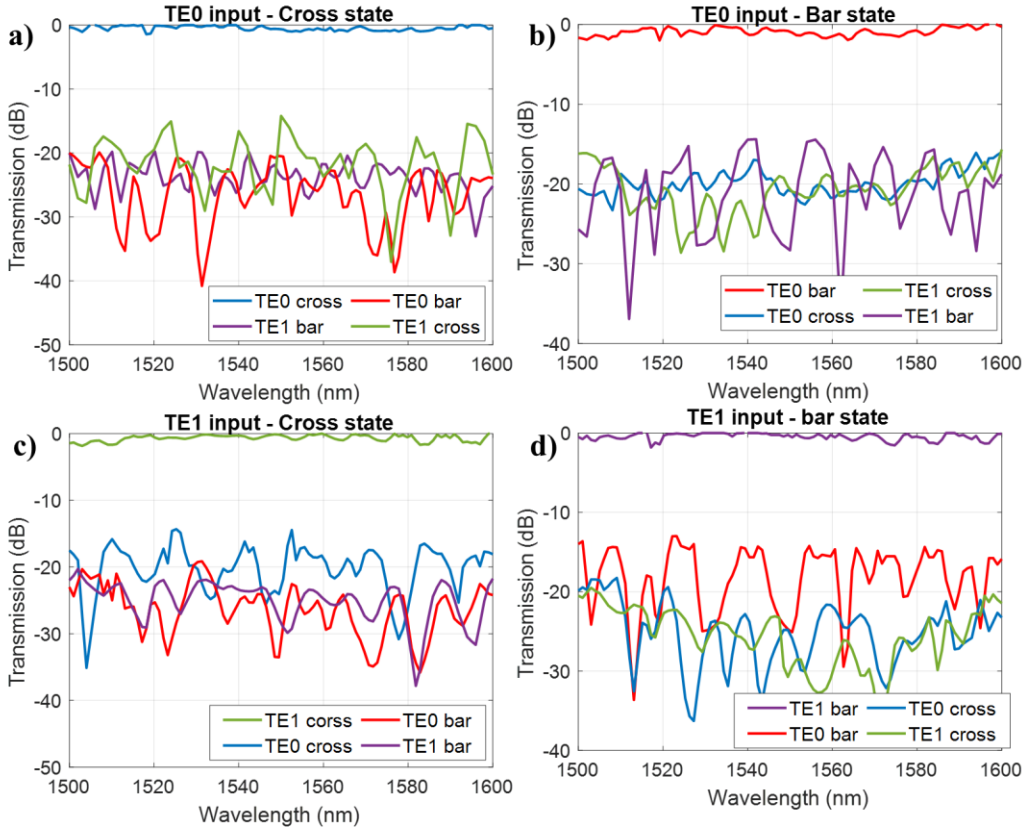

Fig. 5.5 Measured normalized transmission spectrum response as a function of wavelength for (a) TE0 input cross state; (b) TE0 input bar state; (c) TE1 input cross state; (d) TE1 input bar state.

The DBcS insertion loss is 1.0 dB (1.3 dB) and 0.3 dB (0.5 dB) for TE0 and TE1 input modes, respectively, in cross (bar) states. The modal crosstalk for both TE0 and TE1input modes is approximately $< -14\ dB$ dB and $< -13\ dB$ dB for the cross and bar states, respectively, within the wavelength range from 1500 nm to 1600 nm. The summary of the experimental results is represented in Table 5.1.

Table 5.1 Experimental results of the DBcS at 1550 nm

	Input mode			
	TE0 cross	TE0 bar	TE1 cross	TE1 bar
Insertion loss (dB)	1.0	1.3	0.3	0.5
Extinction ratio (dB)	20	37	38	29
Crosstalk (dB)	-14	-13	-14	-13
Bandwidth (nm)	100	100	100	100

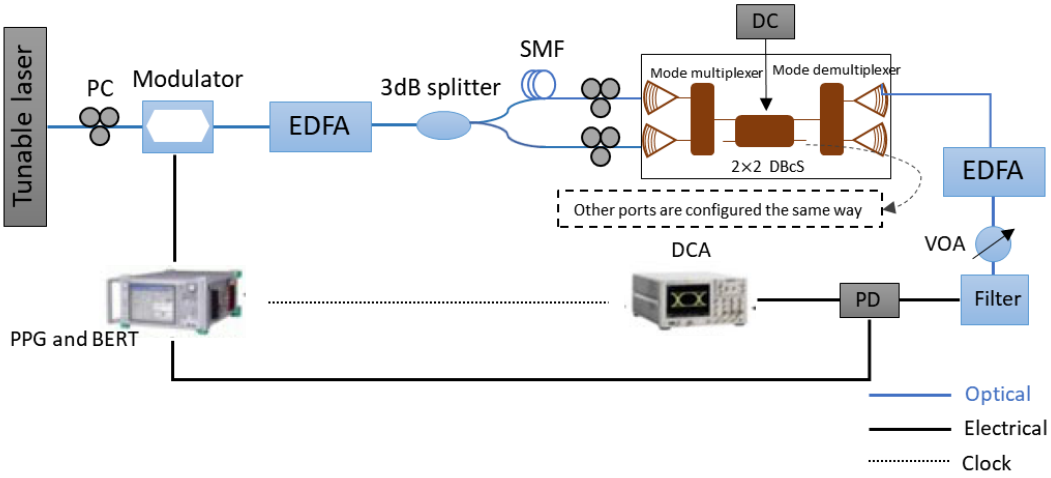

Fig. 5.6 Experimental setup for validation of the proposed insensitive switch. The black solid, black dotted, and the solid blue line represents the electrical signal, clock, and optical signals, respectively. PC: polarization controller, SMF: single-mode fiber, EDFA: erbium-doped fiber amplifier, DCA: digital communication analyzer, PPG: pulse pattern generator, BERT: bit error rate tester.

Using the experimental setup shown in Fig. 5.6, 10 Gb/s NRZ PRBS31 payload transmission is performed to demonstrate the switch performance in the multimode transmission state. To investigate the crosstalk impact, the switch is tested both in single-mode transmission (when either TE0 or TE1 mode is transmitted), and in the multimode state (when both modes are simultaneously transmitted through the switch). The laser output is sent to the polarization controller, then modulated by a 10 Gb/s NRZ PRBS31 electrical signal from pulse pattern generator (PPG) using a modulator with 12.5 GHz 3dB bandwidth. The modulated signal is split into two signals using a

1×2 3 dB power splitter to create two signals. One of the signals is decorrelated by passing it through a 250 m single-mode fiber. Before the fiber array connection, another PC is used for each of the channels to ensure that only TE mode is coupled to the chip. The light is coupled into the chip using grating couplers. The coupling loss is 8 dB per grating coupler. To compensate for the excess loss of the coupling, the output of the chip is passed through an erbium-doped fiber amplifier (EDFA). The EDFA amplified signal is connected to a photodetector (PD) (Finisar XPDV2320R) with a variable optical attenuator (VOA) (JDS Fitel HA9) in between. The EDFA output power is 8 dBm. Using a VOA, we attenuate the signal power to 3 dBm and record the eyes observed using the digital communication analyzer (DCA). The eye diagrams are presented in Fig.5.7.

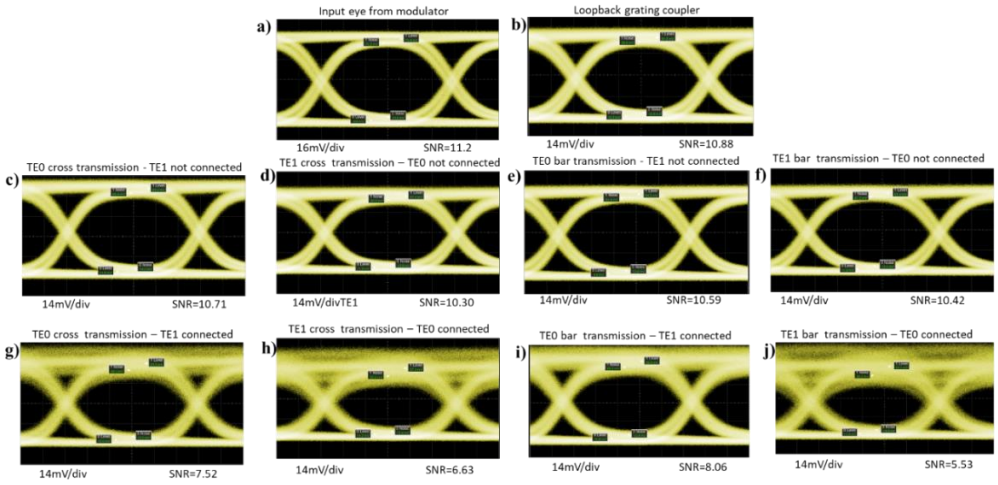

Fig. 5.7 Eye diagrams when PD input is 3 dBm for (a) directly from modulator to PD; (b) grating coupler loopback structures; (c) Single-mode TE0 cross transmission; (d) single-mode TE1 cross transmission; (e) single-mode TE0 bar transmission; (f) single-mode TE1 bar transmission; (g) multimode TE0 cross transmission; (h) multimode TE1 cross transmission; (i) multimode TE0 bar transmission; (j) multimode TE1 bar transmission.

Both in single-mode and multimode transmission, open eye diagrams are observed. For the multimode transmission, eye diagrams are distorted by the crosstalk from the other mode. The TE0 impact on TE1 transmission is higher because of the loss of mode demultiplexer on TE1

transmission. The performance can be improved by further optimizing the DBcMMIs and the mode multiplexers before and after the switch.

To measure the BER, the output signal of the PD is passed through an RF amplifier to increase the peak-to-peak voltage to meet the sensitivity range of the BER tester. The BER is tested in both single-mode and transmission both in cross and bar states. The corresponding BER power penalties are presented in Fig 5.7.

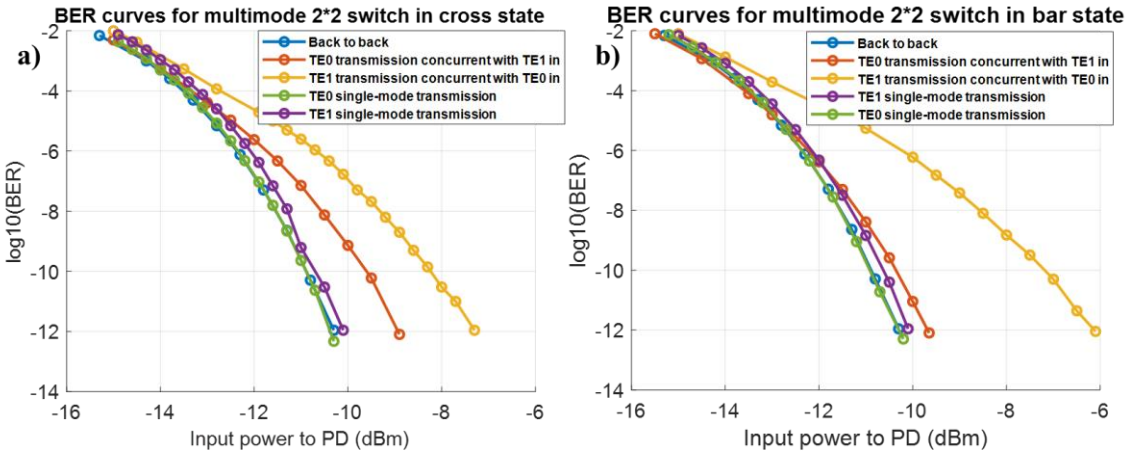

Fig. 5.7 Logarithmic BER as a function of input power to PD in single-mode and multimode transmission of the switch for (a) Cross-state; (b) Bar state

As shown in Fig. 5.7, the power penalty for single-mode TE0 and TE1 transmission is <0.05 dB (<0.05 dB) and 0.2 dB (0.2 dB) in cross (bar) states, respectively. The multimode transmission power penalty is 1.4 dB (0.65 dB) and 3 dB (4.2 dB) for TE0 and TE1, respectively, in cross (bar) states. The higher power penalty for TE1 compared to TE0 transmission results from the insertion loss of the mode (de)multiplexers in TE1 transmission before and after the switch.

5. 3 Conclusion

In conclusion, we proposed and experimentally demonstrated a dual-mode broadband compact switch for MDM systems using SWG structures. The deployment of SWG structures is the enabling reason not only to decrease the multimode power splitters length by 66% (and overall

switch length by 25 %) but also to increase the bandwidth of the switch to 100 nm. The DBcS insertion loss is 1.0 dB (1.3 dB) and 0.3 dB (0.5 dB) for TE0 and TE1 input modes, respectively, in cross (bar) states. The crosstalk for both TE0 and TE1input modes is approximately less than −14 dB and −13 dB for the cross and bar state within the wavelength range from 1500 nm - 1600 nm. Open eye diagrams from 10 Gb/s NRZ data transmission for single-mode and multimode transmission demonstrate the capability of the switch in handling multiple data streams simultaneously using a single wavelength laser. The BER power penalty tests are performed and the error-free transmission with BER less than 10^{-12} for both single-mode and multimode transmission was observed. The power penalty for single-mode TE0 and TE1 transmission is < 0.05 dB and < 0.2 dB in cross and bar states, respectively. The multimode transmission power penalty is 1.4 dB (0.65 dB) and 3 dB (4.2 dB) for TE0 and TE1, respectively, in cross (bar) states. BER power penalty results show that for multimode transmission the laser power needs to be increased by 4 dBm to transfer simultaneously two different data streams using a single wavelength source. By further optimizing the DBcMMIs and mode multiplexers, we can lower this power penalty. The proposed switch structure can be scaled up to higher-order modes (TE2, TE3, and TE4) by further optimizing the multimode power splitter and the phase shifter. Part of this work is planned to be submitted for publication in IEEE Photonic Technology Letters.

Chapter 6

Conclusion and future works

6. 1 Conclusion

This thesis studies the silicon photonic SWG-based multimode on-chip power splitters and MZI switches. Chapter 1 discusses the importance, applications, and principles of SiPh platform. Chapter 2 provides an overview of basic theory and design principles in SWG structures and MDM interconnect communication systems. In chapter 3, the impact of buried air gaps between the fine features of SWG structures is investigated by simulation and experiment. The voids in a commercial beam process, applied nanotools Alberta (ANT), are analyzed using the FIB-HIM method. In chapter 4, a multimode SWG-based power splitter is designed, fabricated at ANT, and characterized using CW measurement. In chapter 5, a multimode MZI switch was designed using the multimode power splitter in chapter 4, a multimode phase shifter, and multimode S-bends. The switch was characterized using CW measurements. Payload transmission tests, as well as CW characterization, were performed to demonstrate the capability of the switch in transmitting different data streams on different modes using a single wavelength. In more details, the main contributions are listed in the following:

a) **Impact of SiO_2 cladding voids on SiPh structures:** we investigated the impact of voids on several common SiPh structures like directional couplers, and ring resonators as well as SWG-based structures like SWG MMIs, and SWG fiber chip couplers. We then analyzed the voids in the cladding of the chips fabricated through a commercial EBL process, ANT. We characterized the voids cross-section area between the gratings with various pitches and grating sizes. Our characterization showed that the voids' cross-sections area in the fabricated chips through this process is less than 500 nm^2 which was small compared to the voids reported in other foundries [73]. Our simulations and characterizations showed that the voids in the ANT process do not have a significant impact on the characterization of the structures. Our simulations showed that when the voids' cross-section area exceeds 1500 nm^2, the voids must be considered in simulation at the design phase. Part of this work was presented at IEEE photonic conference 2020 [94].

b) **Dual-mode broadband compact MMI power splitter:** A 2×2 multimode power splitter is an essential element in MDM switching interconnects. As the beat length of a multimode MMI is usually several times greater than a single-mode MMI [59], dispersion-engineered SWG-based MMIs can be used to reduce the beat length by 66%. Here, we proposed and successfully characterized a dual-mode broadband compact MMI power splitter with a total length of fewer than 42 μm. The insertion loss and modal crosstalk in this proposed design are less than 0.65 dB and -17 dB, respectively, over 100 nm of wavelength from 1500 nm to 1600 nm. The proposed MMI could be scaled up to higher-order modes (TE2, TE3) by further optimizing the multimode region width and length for higher-order modes. We believe that such a device could find many applications in high-performance WDM-MDM compatible switches. Part of this work was submitted for publication in the optics express journal on 2021-03-12 with the submission ID 423882.

c) **Dual-mode broadband compact MZI switch:** to demonstrate the important application of the multimode power splitter in the previous section, we designed and successfully characterized a dual-mode switch with less than 1.3 dB loss and -13 dB modal crosstalk over a 100 nm wavelength from 1500 nm to 1600 nm. We performed NRZ 10 Gb/s payload transmission to demonstrate the capability of the switch transferring multiple data streams simultaneously over a single-wavelength carrier. Open eye diagrams and error-free transmission with BER $<10^{-12}$ were demonstrated both in single-mode and multimode states. Part of this work is in preparation with a plan to submit to the Photonic Technology Letter journal.

6. 2 Future work

Building upon ideas and demonstrations discussed in this thesis, the following directions are suggested for future research:

6. 2. 1 SWG-based compact multimode power splitter MMI for higher-order modes.

In this thesis, we focused on only the first two TE modes in an SOI waveguide. To utilize the great advantages of the MDM platform, scaling up the power splitter to higher-order modes is necessary. One can increase the multimode region width and length and follow the design procedure explained in chapter 4 to make the design working for higher-order modes (e.g., TE2, TE3). Scaling up to higher-order modes makes intermodal crosstalk engineering more complicated. Thus, we also suggest using the design procedure explained in [104] to design an SWG-based polarization-insensitive multimode MMI power splitter. TM modes have the advantage that they have low crosstalk with TE modes. Therefore, one can design a power splitter working with the first three TE and TM modes (TM2, TM1, TM0, TE0, TE1, TE2), simultaneously. Such a great

design provides the capability of sending six data streams on a single wavelength without making a complex design for only one polarization.

6. 2. 2 SWG-based compact mode insensitive switch for higher-order modes:

To design an MZI switch for higher-order modes (TE2, TE3), the power splitter in the previous section (6.2.1) along with a phase shifter designed for higher-order modes can be used. By increasing the width of the phase shifter and following the design procedure in chapter 5, the phase shifter for higher-order modes can be designed. Compared to a single-mode phase shifter, a phase shifter for higher-order modes consumes more power because of the required wider metal heater. Thus, one can combine the design procedure for single-mode spiral power-efficient phase shifters presented in Fig. 6.1 [105] and the procedure for designing a multimode phase shifter in chapter 5, to design a multimode power-efficient phase shifter for higher-order modes. The spiral phase shifters increase the optical interaction length of light with the heating region; thus, will lower the required power to change the phase. It should be noted that multimode bends have more specific designs than single-mode bends and the bend in the multi-mode spiral phase shifter should be specifically designed. For designing a compact multimode bend one can follow the work presented in [106]. The designed lateral offsets in the bends shown in Fig. 6.1 are an effective way to lower the mode mismatch loss in bends. Multimode polarization-insensitive phase shifters along with multimode polarization-insensitive MMIs discussed in section 6.2.1 can be used to make an MZI switch capable of transferring several data streams on several modes on both TE and TM polarizations.

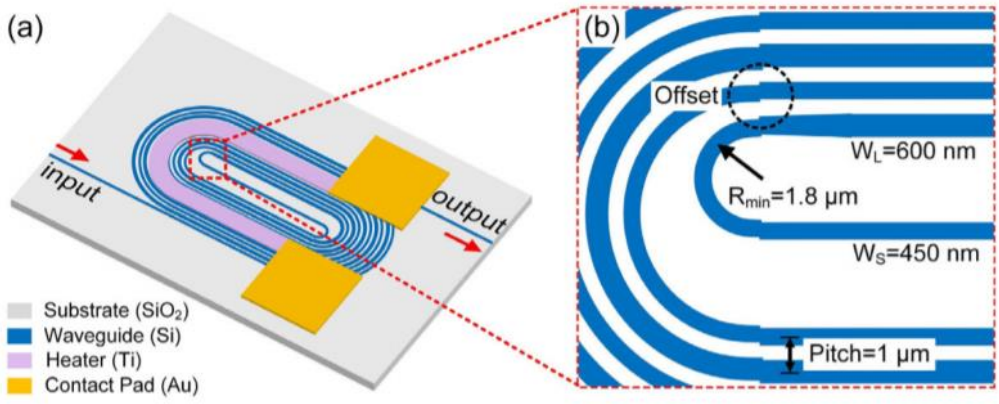

Fig. 6.1 Schematic of the spiral silicon thermo-optic phase shifter using a spiral waveguide; (b) zoom-in showing the spirals and the offset parts [105].

6. 2. 3 Ultra-low crosstalk on-chip mode (de)multiplexer

The mode (de)multiplexer is the heart of an MDM system. Any modal crosstalk from the on-chip mode multiplexers before and demultiplexers after the MDM system propagates through the communication links, adds up to the crosstalk of the MDM system, and will distort the data signals. For achieving a lower power penalty for multimode transmission an ultra-low crosstalk mode (de)multiplexer is needed. Figure 6.2 shows a recent experimentally demonstrated 10-channel dual-polarization mode (de)multiplexer [84]. The crosstalk in this work is less than -15 dB which is not adequate for an MDM system with several higher-order modes to achieve a low-power penalty [101]. One can further optimize the structure using coupled-mode theory [107] to design a three-mode dual-polarization mode (de) multiplexer with lower crosstalk. In summary, the coupled-mode theory states that for achieving an efficient coupling from a single-mode waveguide to a multimode signal the multimode waveguide bus, the effective index of the single-mode light signal should be equal to the effective index of the multimode signal. In practice, there might be several factors that make these effective indices slightly different than the design values. These factors might include the imprecise value of the Si and SiO_2 refractive indices in cladding and

box, sidewall angles of the etched waveguides, any trapped air (voids discussed in chapter 3) between the coupling gap region during SiO_2 cladding deposition, calculation errors, etc. All contributing factors must be investigated to optimize an on-chip mode multiplexer with ultra-low modal crosstalk specific to the fabrication process.

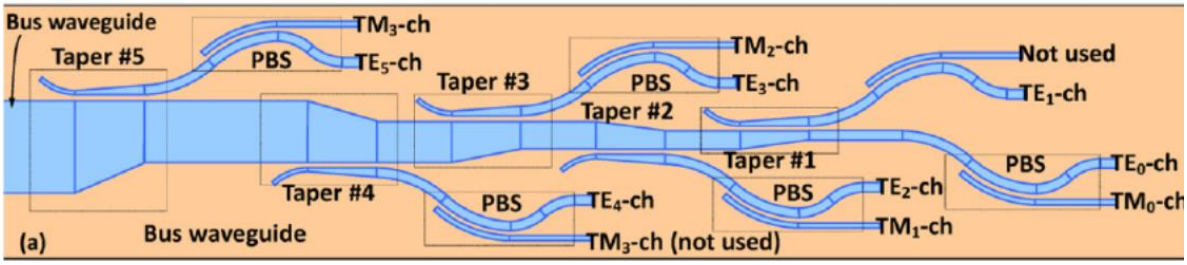

Fig. 6.2 Schematic of a 10-channel dual-polarization mode (de)multiplexer [84].

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