Digital Architectures For Analog Signal Generation

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Abstract

Analog and mixed-signal testing is far more complex than its digital equivalent. This thesis will identify the analog test requirements through an extensive analysis of integrated circuit testing, possible error sources, and the different levels of test hierarchy. The results will show that analog testing requires spectrally pure, high-quality predictable test signals. These signals are most robust when reproduced through digital techniques such as direct digital frequency synthesis. Delta-sigma ($\Delta\Sigma$) modulation is perhaps the most versatile technique, as it can precisely encode arbitrary analog waveforms into an pulse-density modulated (PDM), infinite-length, single bit-wide pattern. The noise-shaping characteristics of the $\Delta\Sigma$ modulator also allow for simple reconstruction of the embedded signal. Unfortunately, on-chip signal generation using this method is currently hindered by the high area overhead and limited programmability of $\Delta\Sigma$ modulation oscillators. We will introduce the concept of forcing the PDM pattern to be finite in length and thus periodic. Although other periodic encoding algorithms exist, forced-periodic PDM patterns will be shown to be far superior for their precise control over signal amplitude, frequency, phase, and also for their ability to encode an arbitrary waveform. Its effectiveness will be demonstrated with several experiments of single- and multi-tone waveforms of varying degrees of complexity. By creating a fixed-length pattern, we can take advantage of many common digital built-in self-test (BIST) concepts such as scan and RAMBIST, found on most digital and mixed-signal integrated circuits, to supply the necessary hardware. We will show how analog signal generation can be integrated into digital ICs using any or all of the IEEE 1149.1-1990 standard, embedded RAMs, and scan chains. These applications will indeed prove that with very little additional hardware, on-chip, high-quality analog signal generation is possible and that mixed analog-digital built-in-self-test is feasible in today's IC technologies.

Résumé

La vérification de circuits analogiques et hybrides analogiques/numériques est beaucoup plus difficile que la vérification de circuits exclusivement numériques. Ce mémoire identifie les ressources nécessaires pour la vérification des circuits analogiques par une analyse détaillée de la vérification des circuits intégrés en général et des sources d'erreurs potentielles, en tenant compte des différents niveaux de vérification. Les résultats démontrent que la vérification de circuits analogiques requiert des signaux de qualité supérieure. Or, ces signaux sont plus stables lorsque produits à l'aide de techniques numériques. La modulation delta-sigma est probablement la technique la plus versatile puisqu'elle permet de coder un signal arbitraire en une séquence infinie de bits. De plus, puisque le bruit généré par la quantization est localisé hors de la bande passante, le signal peut être récupéré facilement. Malheureusement, la production de signaux de cette façon directement sur le substrat du circuit à vérifier entraîne un coût exagéré et souffre d'une versatilité limitée. Nous présentons une méthode pour contraindre les séquences de bits à une longueur limitée et ainsi les rendre périodiques. Bien que d'autres algorithmes permettant de coder un signal sur une séquence périodique existent, notre méthode est supérieure de par son contrôle précis de l'amplitude, de la fréquence et de la phase de même que pour la possibilité de coder une grande variété de signaux. Son efficacité est démontrée par plusieurs expériences reproduisant des signaux de complexité variable. En créant une séquence de longueur définie, il devient possible de réutiliser plusieurs outils de vérification numérique. Nous démontrons comment notre méthode de génération de signaux analogiques peut être intégrée sur un circuit numérique par le standard IEEE 1149.1-1990, par un bloc de mémoire vive ou à l'aide d'une chaîne de vérification. Ces applications prouvent qu'avec peu de matériel additionnel, la génération de signaux analogique de haute-qualité et l'auto-vérification de circuits hybrides analogiques/ numériques sont possibles à l'aide de la technologie actuellement disponible.

Acknowledgments

The single name on this thesis does not do justice to the several people who have contributed their knowledge, experience, and support over the past two years to assist in my pursuit of original and purposeful ideas.

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Chapter 1 - Introduction

The purpose of this thesis is to focus on the generation of digital signals for use in analog testing and their integration into the testing environment. Research in the area by Lu et al [1] provided the basis for area-efficient analog signal generation using digital encoding. The concept of mixed analog-digital built-in-self-test (MADBIST) introduced by Toner and Roberts [2] combined the signal generator with data collection methods to demonstrate the feasibility of BIST for mixed-signal ICs. We plan to build on this previous work to introduce two major advancements in the area. The first demonstrates the creation of finite-length digital patterns which eliminate the need for an on-chip analog signal generator. The second focusses on the applications of digital-encoded signals. The first describes a system designed as a stand-alone test circuit or as a sub-system that can retrofit a digital tester for analog or mixed-signal IC testing. The second application focusses on the mixed analog-digital built-in self test (MADBIST) application with the introduction of two on-chip signal sequencers that integrate into current digital DFT techniques. These configurations allow for the generation of on-chip stimuli with very little and in some cases, no additional area overhead.

1.1 - Motivation

Digital integrated circuit (IC) manufacturers have incorporated built-in-self-test (BIST) schemes into the design process in an attempt to minimize production costs and improve quality. BIST creates a methodical approach to the detection and isolation of manufacturing defects. Today, the most accepted forms of digital BIST are based on the interface set out in the IEEE 1149.1-1990 Standard, specifically boundary scan. Other types of IC BIST include internal scan and memory tests that verify RAM functionality (RAMBIST).

Analog or mixed-signal ICs, on the other hand, rely mostly on ad hoc, unstructured test methodologies. Analog test stimuli are most often generated off-chip in a traditional test setup as shown in Fig. 1.1. In a production environment, the test station includes a test module consisting of a digital signal generator, high-precision digital-to-analog and analog-to-digital converters (DACs and ADCs), and a test head fixture. The remote location of the test station with respect to the circuit under test exposes the circuit to parasitics present in the test apparatus and the in interconnect between the circuit and the test module. This is true even if the test module is located on the test head. The interconnect is potentially quite long (with respect to the wavelength of the test signals) and, as a result, the signals carried through them are susceptible to signal degradation. As circuit speed increases, greater attention is placed on board layout in order to minimize energy reflection, noise, and other effects not directly related to the circuit itself. These effects must be accounted for when performing tests. Thus, the manufacturing and test processes for these ICs often require extensive setup time for proper device characterization and very expensive test equipment to guarantee high noise immunity and to minimize the change on the circuit behaviour it is testing. Addressing these complexities makes the mixed-signal test field a very promising and active area of research.

One way to minimize the complexity and expense of the traditional analog test method is to place the test apparatus directly on-chip as a built-in-self-test, or BIST. Alternatively, one could avoid signal degradation over the interconnect by digitally encoding the analog test stimuli, provided little complexity is required at the test fixture to decode it. Toner and

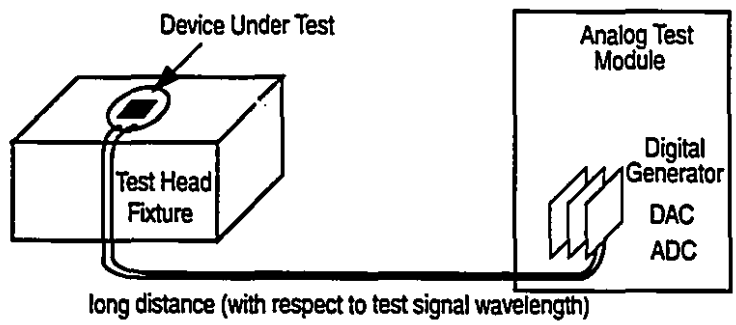


Fig. 1.1 - Typical Analog Test Station

Roberts [2] have proposed MADBIST, and have shown that the above two concepts are feasible. Research in this area is based on the digital encoding of analog signals using delta-sigma ($\Delta\Sigma$) modulation techniques and serves as the basis for the work set out in this thesis.

$\Delta\Sigma$ modulation allows us to transform a multi-bit digital pattern into a single-bit pattern through the principles of oversampling with a pulse-density modulation (PDM) coding scheme. PDM serves as a practical method to encode an analog signal in a digital one [3], with simple reconstruction of the original signal [4]. This pattern is, unfortunately, of infinite length and requires the use of an area-intensive $\Delta\Sigma$ oscillator for on-chip signal generation. Our previous research indicates, however, that we can create an approximate finite-length digital bit pattern that contains the desired analog test signal [5]. Having obtained a pattern of reasonable length, we can now integrate analog signal generation into existing digital BIST hardware. In particular, we can utilize the scan chain configuration and controller logic set out in IEEE Standard 1149.1 or even use existing RAMBIST logic to minimize hardware overhead. This now makes MADBIST a practical method of performing analog BIST.

We can make further progress into minimizing test complexity and cost by simplifying the traditional analog setup described earlier. Now that signal generation can be achieved reliably with little hardware in the digital domain, relatively cheap digital testers can be retrofitted to perform the tasks once dedicated to analog testers. This is possible since a modified test head can hold the minimal additional logic, and only digital signals need be exchanged between the test head and the digital test module as shown in Fig. 1.2.

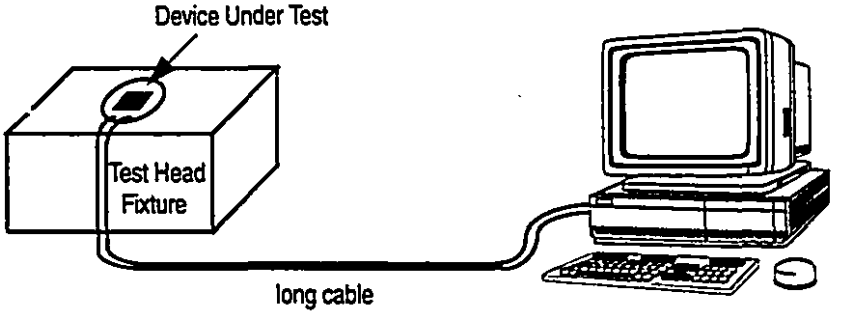


Fig. 1.2 - Digital Test Station Retrofitted for Analog Testing

1.2 - Integrated Circuit Testing

Testing in its simplest form is the stimulation and observation of the pins of an electronic device. This is termed the "black box" method of testing (as depicted in Fig. 1.3) in which there is no knowledge of the inner workings of the circuit (nor is there a need to know), just the knowledge of the overall function of the circuit and its input and output signals. The circuit performs a known function, and it is the job of the test engineer to determine whether or not the circuit performs its function within an acceptable tolerance level. For digital devices, the circuit output response is either a logic-0 or logic-1. Hence there is a zero tolerance level. Analog or mixed-signal circuits, on the other hand, may have a range of output values within which the measured output is acceptable. This type of stimulation and response analysis is known as functional testing. In all cases however, as design complexity grows, functional testing becomes increasingly costly to perform. Sophisticated digital circuits, for example, require several lengthy test patterns or long circuit preparation time to mimic a particular circuit function. Analog circuits require very accurate and precise test equipment to not only generate realistic input signals but also to capture and process output data to verify circuit behaviour. These situations require extensive preparation and test execution time to maximize circuit fault coverage. The culmination of test preparation, lengthy test times, and complex output analyses make the functional testing approach an expensive task. Thus one must consider possible alternatives.

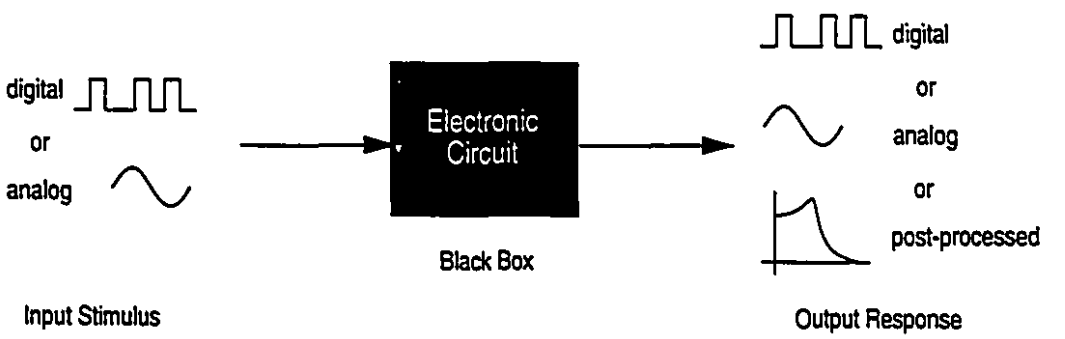


Fig. 1.3 - Black Box Functional Test Configuration

1.3 - Sources of Error

In determining alternatives, we must first examine likely sources of error. We can categorize errors into two different types: functional errors and manufacturing defects.

1.3.1 - Functional Errors

Simply put, functional defects are errors in the operation of the circuit caused by an error made during the design phase. In the digital domain, the cause is easily identifiable: the designer either misinterpreted the functional specification or made a careless mistake, causing an outcome different from the desired result (e.g. a logic-1 was observed when a logic-0 was expected). While the analogy holds true for the analog circuits, the designer assumes a greater responsibility in the functional performance of the circuit by practising analog design techniques such as symmetrical layout, component isolation to avoid coupling effects, and ensuring current operation within IC manufacturing tolerances. Assuming the designer is competent at his or her job, we turn our attention to the other error source, that is, defects caused by the manufacturing process.

1.3.2 - Manufacturing Defects

We define manufacturing defects as being those created during the fabrication process, and are beyond control of the designer. There are generally two types of manufacturing defects: those caused by environmental impurities and those caused by process variation.

One example of an environmental defect is a piece of dust or debris originating, for example, from the gears driving the conveyer belt and landing on a die. This can cause two types of component failures (as shown in Fig. 1.4): catastrophic and parametric. A catastrophic failure is one in which a component simply does not change state. Using a transistor as an example, it is either stuck on (shorted) or off (open-circuited). A parametric failure, on the other hand, is one in which the component appears to function, but may not be within tolerances. Such would be the case for a transistor that may turn on and off but carries less current than is typical.

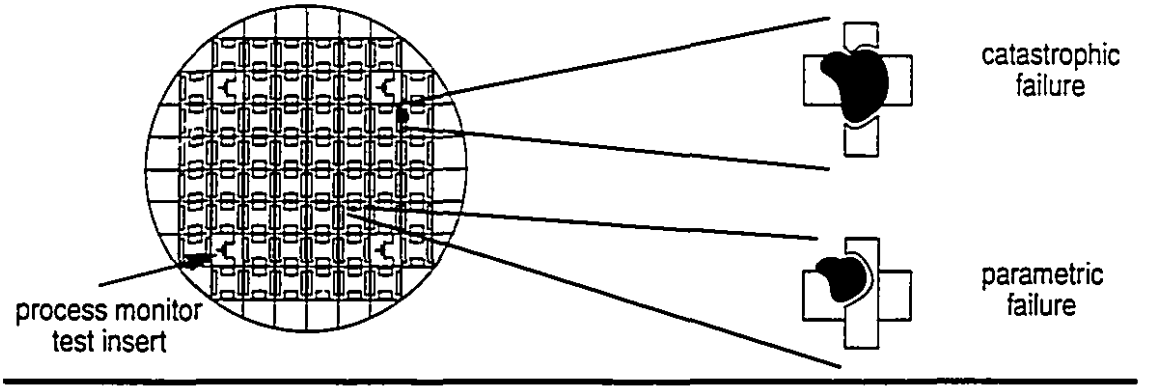


Fig. 1.4 - The Two Failure Modes Due To Manufacturing Defects

Process variation is the change of layer depositions due to fluctuation of equipment alignment or performance. One example would be the variation of oxide thickness over a die or wafer, as illustrated in Fig. 1.5. Caused by a machine drift or alignment skew, differing oxide thicknesses occur at various points on the wafer. Where the thickness is minimal, there is increased risk of a non-functional transistor and reduced reliability (i.e., pin holes through the oxide). At the other extreme, where the oxide is thicker than the nominal value, the speed of the device is degraded due to reduced drain-to-source current.

Process variation can be categorized into two types: global and local variation. Global variation (in the gate oxide example) focusses on the oxide thickness across the entire wafer, with the assertion that so long as the geographical extrema of the wafer fall within specifications, adjacent dies have a strong likelihood of also being within specifications. Consequently, all ICs, be they digital, analog, or mixed-signal, must be monitored for global variation to provide a confidence level for a properly manufactured wafer or die. This can be done through strategically-placed test monitor inserts (see Fig. 1.4). Local variation (again using the gate oxide example) is the difference in oxide thickness among adjacent dies on the wafer or among components on the same die. Local variation measurements give no indication as to the overall wafer yield; rather they quantify the variability between adjacent components. This is useful information for circuits based on component-matching, i.e., designed by ratios.

Now that we have covered the different types and causes of manufacturing defects, we will study the significance of each on both digital and analog integrated circuits.

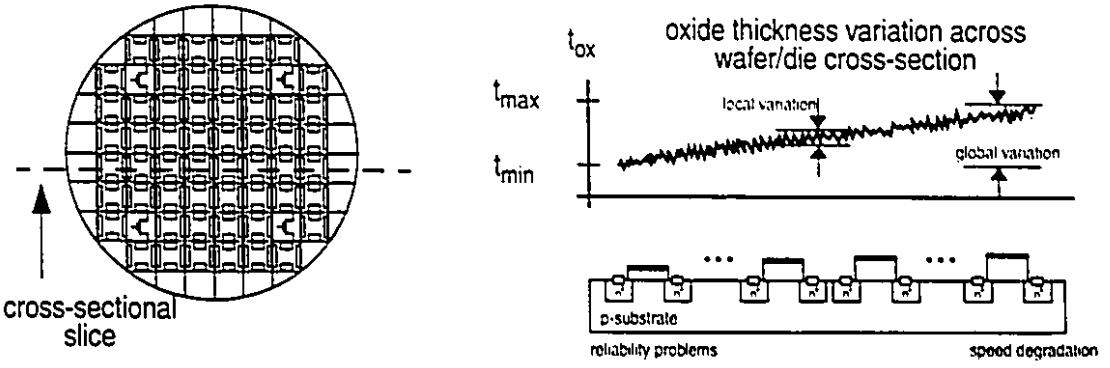


Fig. 1.5 - Effect of Oxide Thickness Due To Process Variation

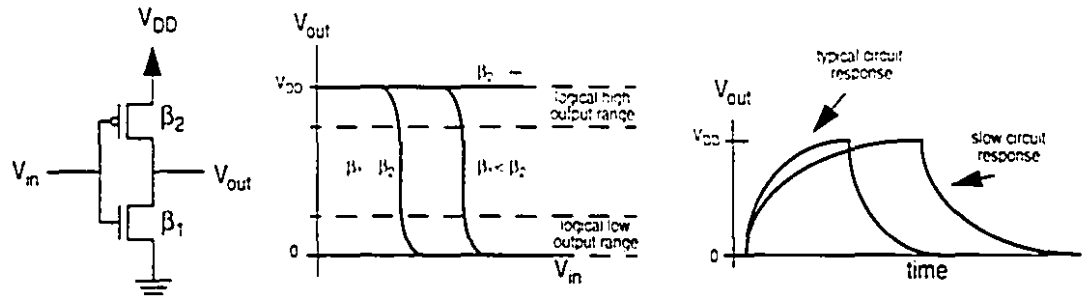
1.4 - Impact of Defects on Digital Circuits

To observe the effects of the different manufacturing defects, consider the typical MOS inverter, given in Fig. 1.6(a), with transistor gain factors β_1 and β_2. Due to local process variation, β_1 will differ slightly from β_2, and result in the skewed transfer characteristic as shown in Fig. 1.6(b). However, as long as the output logic levels fall within an acceptable range, the circuit will function properly. Thus the logic function is insensitive to device mismatches caused by local process variation.

Since parametric deficiencies due to environmental contamination directly affect the gain factor of the transistor, digital circuits are somewhat immune to parametric failures. This depends, of course, on the transistor β still yielding sufficient drive capability and the circuit response, typified in Fig. 1.6(c), falling within the required timing specifications. Fortunately, these failures can still be identified by an incorrect logic level in a given time interval (i.e., the failure is considered catastrophic).

When there are significant differences between the transistor gain factors, for example, β_2 approaching ∞, the affected transistor is now short-circuited, and the device logic function fails to operate correctly. Thus, the logic function is sensitive to catastrophic failures.

Since digital devices are sensitive to catastrophic failures, digital test methods concentrate on incorrect logic function, rather than on device mismatch effects. Note that as digital



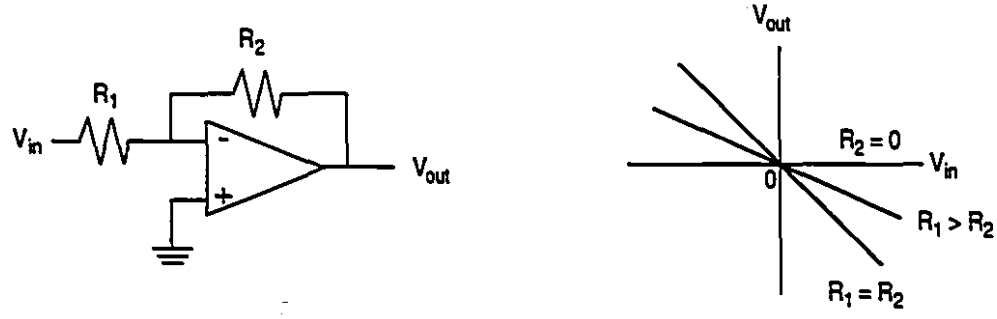
(a) MOS inverter (b) inverter transfer characteristic (c) output response

Fig. 1.6 - Effect of Device Mismatch on a Digital MOS Inverter

designs approach the sub-micron technology, analog design techniques such as interconnect matching are practised, and thus the characteristics of analog behaviour on digital circuits are of importance. The impact of defects on analog circuits are discussed in the following section.

1.5 - Impact of Defects on Analog Circuits

Unlike digital circuits, the function of analog circuits are sensitive to device mismatches. Consider the analog inverter shown in Fig. 1.7(a). Ideally, R_1 and R_2 are equal. Due to local process variation, however, it is not likely that an IC containing this circuit will have equal resistors. The end result is a deviation from the expected transfer characteristic illustrated in Fig. 1.7(b).



(a) analog inverter (b) inverter transfer characteristic

Fig. 1.7 - Effect of Device Mismatch on an Analog Inverter

Analog designers have acknowledged that the output response may vary from ideal. Therefore, in an attempt to minimize signal variability, great importance is placed on design layout. Techniques such as designing circuits so that their characteristics depend on a ratio of components (design by ratios), symmetrical component layout, matched interconnect lengths, and impedance matching are employed as good design practice for this reason. In addition, the tolerances and variability of the manufacturing process must be minimized in order to maximize yield. The above practices serve to minimize the effect of local process variation on an analog circuit. Parametric failures in which the device still functions can be treated as a local variation.

Like the digital circuit, analog circuits are also sensitive to catastrophic errors. Revisiting the inverter example, it is obvious that a large change in one of the resistors (like say, R_2 approaching ∞) will prevent correct circuit function. In general, however, components such as resistors and capacitors are large in comparison to minimum device sizes and, as a result, catastrophic failures are less likely to occur.

A third exposure in analog design is component limitation, such as non-linearities and noise. Higher-order effects may yield a different function for a given component that was designed as a linear element, introducing a degree of uncertainty to the expected results. Analog components are susceptible to noise, may generate noise themselves, and/or couple with neighbouring components to create spurious noise -- all which may degrade IC performance.

Because of the dependency on component mismatches and component limitations, analog test methods focus on these effects. Of course, catastrophic failures are equally as important; yet the discovery of catastrophic errors is an artifact of mismatch/limitation testing and does not normally require an extra suite of tests. Unfortunately, no simple method exists to provide fault coverage for mismatch/limitation testing. It is the position of the author that functional testing must be performed to ensure correct device functionality and to identify parametric and catastrophic errors.

1.6 - The System Hierarchy

Another aspect to consider is the practicality and complexity of testing at different levels of the design hierarchy, from the component level (within a single IC) to an entire multi-function chip or multi-chip system. Consider an electronic system consisting of three levels of hierarchy, shown in Fig. 1.8. The lowest level is the component level, indicated in Fig. 1.8(a). These are building blocks, and their individual behaviours may interact to form the desired function of a larger block. For example, the behaviour of two resistors in series is based on the sum of the two -- not on their individual absolute values. The next level of hierarchy is the sub-system level in Fig. 1.8(b). A sub-system is a building-block whose behaviour is *not* designed to interact with other sub-systems in order to achieve a desired behaviour. An example of a sub-system would be the receive and transmit circuits of a telephony coder-decoder (CODEC); it is undesirable to have the function of one affect the function of the other. The third and highest level is the system level as in Fig. 1.8(c). It is comprised of multiple sub-systems to perform a desired function or number of functions. Again, it is undesirable to have any interaction between blocks here. We now have to ascertain what information is contained in the tests performed at the different hierarchical levels.

At the component level, we can obtain the absolute values and hence the variation of each individual element. However, because of the behavioural interaction of components at the next hierarchical level (sub-system), individual component variation is not sufficient to

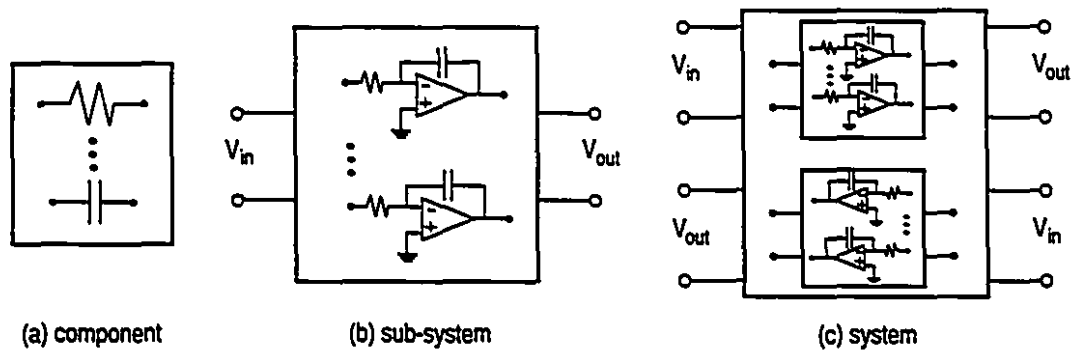
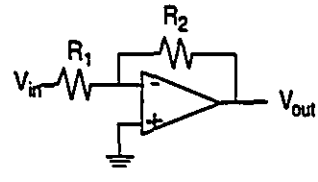


Fig. 1.8 - The Hierarchical Levels of an Electronic System

deduce individual sub-system acceptability. That is, rejection of individual components may unnecessarily lower the yield by rejecting components which, while individually falling out of tolerance specifications, collectively combine to form an acceptable device at the sub-system level. This is evident if we examine the resistors of an analog inverter in Fig. 1.9. Here we have specified typical design tolerances on the individual resistors of ±20%, and an inverter transfer function tolerance of ±3%. Consider Case 1: due to manufacturing error, the resistors individually fall outside their specified tolerance level; yet the inverter falls within specifications. Using component tests as a guide, a properly functioning inverter would have been rejected. Conversely, consider Case 2: the individual components fall well within specification but in opposite tolerance directions; in this case, the inverter falls outside of its acceptable tolerance range. Component testing would have passed a non-functional circuit. Thus, testing at the component level does not ensure a properly functioning circuit.

The sub-system level, as described earlier, has no intended interaction between sub-systems to produce the desired circuit behaviour. As a result, tests performed at this level verify sub-system function and also guarantee correct sub-system function at the system level. As illustrated in Fig. 1.9, the sub-system is tolerant to individual component variation, provided the components are affected in the same manner. Immunity to component variation can, however, be maximized during the layout phase of the design.



Specifications:
individual component tolerances: ± 20%
inverter (sub-system) design tolerance: ± 3%

Ideal transfer function:

$$TF_{ideal} = \frac{V_{out}}{V_{in}} = -\frac{R_{2ideal}}{R_{1ideal}}$$

Case 1:

$R_1 = R_{1ideal} + 25\%$ R_1 component failure ✗
$R_2 = R_{2ideal} + 22\%$ R_2 component failure ✗

$$\frac{V_{out}}{V_{in}} = -\frac{R_{2ideal}}{R_{1ideal}} \cdot \frac{1.22}{1.25} = TF_{ideal} - 2.4\%$$ sub-system pass ✓

Case 2:

$R_1 = R_{1ideal} + 3\%$ R_1 component pass ✓
$R_2 = R_{2ideal} - 2\%$ R_2 component pass ✓

$$\frac{V_{out}}{V_{in}} = -\frac{R_{2ideal}}{R_{1ideal}} \cdot \frac{1.03}{0.98} = TF_{ideal} + 5.1\%$$ sub-system failure ✗

Fig. 1.9 - Component Variation Effects on Sub-System Design Tolerances

Table 1.1 - Typical Parameter Tolerances For Various Monolithic Devices

Component Type	Parameter/Material	Absolute Value Tolerance	Matching Tolerance
NPN Transistor	β	±20%	±5%
	V_{BE}	±20mV	±1mV
NMOS Transistor	V_T	±100mV	±10mV
	k_p	±20%	±5%
Resistor	p-type diffused	±20%	±1%
	epitaxial	±30%	±5%
	thin film	±5% - ±10%	±1% - ±2%
Capacitor	MOS	±20%	±0.1% - ±1%
	poly-poly	±20%	±0.1% - ±1%

Table 1.1 exemplifies the advantages of designing by ratios to utilize the component-matching attributes of the fabrication process. Note the obvious reduction in matching tolerances versus absolute value tolerances.

Sub-systems are often partitioned by their intended behaviour. That is, functional partitioning is analogous with sub-system partitioning. This suggests that functional testing is best performed at the sub-system level. Several advantages to functional testing exist at the sub-system level. First, there is inherent fault isolation since sub-systems are partitioned by function. Second, functional testing serves to characterize the circuit by its functional black-box behaviour, thereby eliminating the need to manually probe (and potentially disturb) internal nodes to characterize circuit performance. Finally, since functional testing and device characterization are performed simultaneously, there is a reduction in test time and complexity.

System level testing encompasses the entire multi-function chip or multi-chip circuit. Tests at this level appear similar to actual field usage of the device, except that they may push the limits of system characteristics, such as data throughput, signal quality, noise immunity, and temperature stresses. This technique is known as "soaking" the circuit. Often this is done to ensure compliance with governing standards. While system testing is the only manner in which to guarantee an end-to-end functional product, it is not intended to characterize its sub-systems or attempt to detect its faults. The complexity of a circuit

consisting of multiple sub-systems and countless components makes complete fault detection cost- and time-prohibitive at this level. In larger circuits consisting of thousands or millions of individual elements, the interaction of all components makes this task virtually impossible. Thus, in order to minimize test complexity and effort, testing should be done at the sub-system level.

1.7 - Thesis Overview

We have just brought forth the importance of performing functional tests on analog circuits at the sub-system level. This necessitates the requirement for high-quality analog signals as test stimuli. It will be our mandate to create a signal generator using digital circuitry in order to achieve spectrally pure signals and have precise control over amplitude and frequency. Moreover, we will arrive at a technique which minimizes the area a signal generator requires so that it can be placed on-chip for BIST and other test or signal generation applications. We will also integrate the method into today's digital test architectures to facilitate its introduction to industry and simplify its implementation.

This thesis will continue by introducing the concept of MADBIST. The idea of performing on-chip BIST for mixed-signal ICs in a simple and area-efficient manner is ground-breaking research which this thesis uses as the basis for development. We will describe three main types of analog signal encoding, all of which endeavour to embed an analog signal into a bit-wide digital pattern, and justify our decision to favour pulse-density modulation (PDM) as the most powerful and versatile encoding scheme available today. We will also demonstrate the use of PDM in an analog signal generator known as the $\Delta\Sigma$ oscillator.

Chapter 3 will highlight several applications of the $\Delta\Sigma$ oscillator, including the dedicated test system which creates a simple yet effective analog IC tester. We will also describe two fabricated oscillator ASICs and provide simulation and experimental results.

Chapter 4 will introduce our first original concept: the forced-periodic PDM bit pattern. We will describe how to establish the minimum bit pattern required to encode an analog

signal using PDM techniques, examine the effects of truncating an infinitely-long bit pattern, and demonstrate its versatility in encoding both simple and complex analog waveforms.

Chapter 5 will focus on the application of finite-length PDM patterns. Here we provide two unique and original techniques for integrating analog signal generation into the current digital test architectures. Using such test logic as the 1149.1-1990 IEEE JTAG interface and RAMBIST, we introduce various hardware configurations that make MADBIST a feasible concept in today's mixed-signal ICs, and put analog signal generation on an IC with virtually no additional logic.

This thesis will conclude with a summary of the work that has been introduced thus far. We feel the originality of truncating PDM patterns and integrating analog test generation into digital test architectures creates several new opportunities for further research and will propose a few ideas that can make use of the powerful techniques described herein.

1.8 - Test and Data Collection Environment

Unless otherwise indicated, all experimental results given in this thesis were collected with a test station as indicated in Fig. 1.10. Data patterns were generated on an HP E1445A arbitrary function generator. When required, a Krohn-Hite 3202 maximally-flat lowpass filter was included in the signal path. Graphs and other data collection were obtained from an HP 54510A digitizing oscilloscope and an HP 3588A spectrum analyzer.

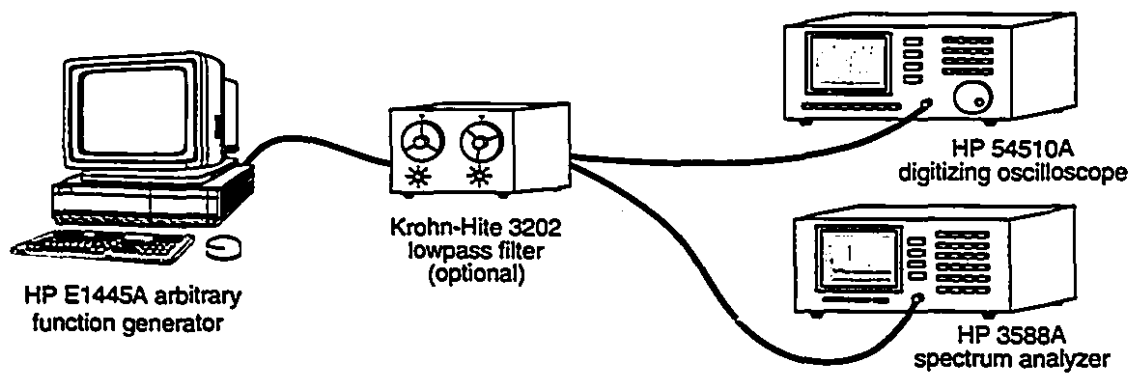


Fig. 1.10 - Test Station for Conducting Experiments

Chapter 2 - MADBIST and Analog Signal Encoding

One of the primary applications for advancements in the area of digitally-encoded analog signals is mixed analog-digital built-in self-test, or MADBIST. This chapter will explain the concept of MADBIST and the variety of methods to digitally-encode an analog signal.

2.1 - The MADBIST Method of IC Self-Test

The MADBIST scheme, as set out in [1], is directed towards the self-testing of a mixed-signal IC consisting of an analog-to-digital converter (ADC), a digital signal processing (DSP) unit, and a digital-to-analog converter (DAC), each of which is classified as a sub-system. Generally, a generic mixed-signal IC has an analog signal that passes through the ADC, is processed in the digital domain using a DSP unit, and is converted back to an analog signal using a DAC as shown in Fig. 2.1.

One method to test all sub-systems of the IC is to place the device in a loop-back mode, as shown in Fig. 2.2. Here, the DSP unit generates a signal which is passed through the DAC and is looped back to the ADC input. The digital signal of the ADC is then passed on to the DSP unit for comparison with the original digital pattern. This test mode is not conclusive, however, since errors in the DAC may be masked by errors in the ADC. Consequently, it is not an acceptable test method, according to the CCITT standards body.

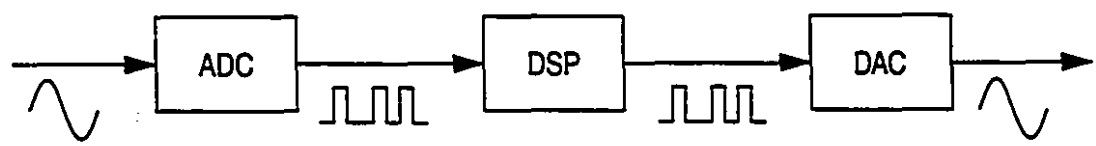


Fig. 2.1 - Signal Flow for a Generic Mixed-Signal Integrated Circuit

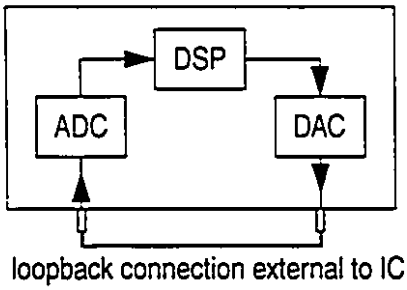


Fig. 2.2 - Mixed-Signal IC in a Self-Test Loopback Configuration

MADBIST proposes a test method which verifies the functionality of the IC by testing each sub-system individually. The key element is the PDM signal generator in which, if the ADC utilizes a $\Delta\Sigma$ modulator, there is little additional area overhead associated with the setup. Figure 2.3 shows the required modifications. The test sequence is described below.

First, the DSP unit and any other digital circuitry on the IC is tested using normal digital BIST techniques. Next, the digital components are configured to generate a PDM bit pattern, within which is encoded an analog signal, and is multiplexed into the ADC. The anti-aliasing filter of the ADC extracts the analog signal from the digital bit pattern. In cases where the ADC input cannot handle a rail-rail input digital input, a simple filter (such as a passive RC) with a cut-off frequency at the bandedge can reduce the signal levels considerably. The filter may exist on- or off-chip (for the purposes of a pure BIST it would of course, reside on-chip and preferably part of the input stage of the anti-aliasing filter). The digitized signal output from the ADC is then fed back into the DSP unit for comparison with the original signal. Through a variety of tests, the ADC may be completely exercised in this manner.

With the functionality of the ADC verified, PDM stream generation is disabled, and the DAC is placed in normal operating mode. A loopback configuration is then established through the switch and multiplexer internal to the chip. Since the DSP unit and the ADC have passed their tests, the DAC can now be fully tested without the risk of any errors being masked. The performance of each component has now been individually

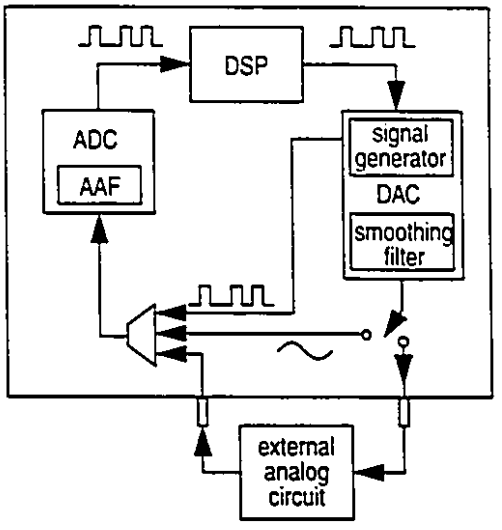


Fig. 2.3 - MADBIST IC Test and Component Structure

characterized. Assuming all tests were satisfactorily completed, the chip as a whole has passed its BIST and can now be used for testing analog circuits external to the IC.

The MADBIST configuration relies on a relatively powerful digital processing unit to perform the certain analyses necessary for performance measurements. For example, industrial tests such as frequency response, gain tracking, and signal-to-noise ratio measurements require post-processing of the digital bit stream for parameter extraction. Such measuring techniques include the Fast Fourier Transform (FFT) or a narrowband digital filter. Currently, the hardware overhead associated with such techniques can be significant and must be considered at the design stage. However, it is anticipated that further research in the area can produce smaller, more efficient data extraction methods. For the purposes of the MADBIST discussion, we will assume a narrowband digital filter is used [2].

The key element in MADBIST is the use of a one-bit digital signal stream to represent an analog signal. The signal generator is also the most area-intensive component of the system. If the ADC uses oversampling logic (i.e., it consists of a $\Delta\Sigma$ modulator), then that same modulator can be shared with a $\Delta\Sigma$ oscillator to convert a multi-bit digital signal to a one bit-wide, over-sampled data stream. This may not always be the case however; more generally, we should examine the various techniques of digitally encoding an analog

signal to determine which may be the most useful or practical while minimizing costs due to additional hardware overhead and complexity. A variety of signal generation methods will be discussed in the following section.

2.2 - Digital Encoding of Analog Signals

There are various techniques to encode an analog signal into a digital bit pattern. For instance, a multi-bit representation that quantizes the infinitely-variable analog signal into a digital word is often used in digital signal processing but requires sophisticated A/D and D/A converters for encoding and decoding. We must not forget that we are focussed on testing these converters and thus cannot use them for test signal generation. Moreover, it would be much more convenient if the encoded signal were embedded in a single-bit rather than multi-bit representation. Intuitively, we would expect the extraction of the encoded signal to be an easier procedure.

Three common methods of generating a single-bit pattern to represent an arbitrary analog waveform exist: pulse generation, multi-frequency binary sequence (MBS) generation, and pulse-density modulated (PDM) signal generation. These will now be examined in greater detail.

2.2.1 - Pulse Generation

The simplest form of analog signal generation is the creation of an analog signal by simply applying and repeating periodic bit pattern composed of a single pulse. The fundamental frequency is given by

$$f_t = \frac{f_s}{N}, \tag{2.1}$$

where N is the pattern length in bits and f_s is the sampling frequency. A total of N-1 tones exist over the frequency range f_s, occurring at

$$f_{tones} = f_s - kf_t, 1 \le k \le N-1 \tag{2.2}$$

Figure 2.4 shows an example of a pulse pattern (a) and its spectrum (b) over the bandwidth, f_s. Here we have a periodic 8-bit pattern containing a single +1 and seven -1s clocked at a rate of 1 MHz. Thus,

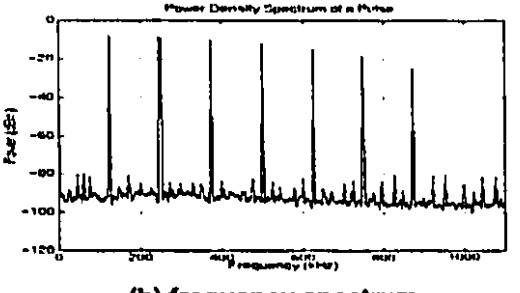
$$f_t = \frac{1MHz}{8} = 125kHz.$$

As expected, the frequency spectrum consists N-1, or seven tones: a fundamental at 125 kHz followed by six harmonics every 125 kHz thereafter over the frequency range of 1 MHz.

This approach has applications in frequency-domain system identification, where a system under test is subjected to multiple frequencies simultaneously. We, on the other hand, are interested in a technique that will generate high-quality signals that are easy to reconstruct from the pattern in which they are embedded. Unfortunately, signal generation by pulses suffers from a few deficiencies in our desired application that we must consider. First, for single-tone generation, a selectable high-order filter is required to isolate the desired tone. It must be especially acute at low frequencies. Second, if the environment is such that the binary signal generator cannot vary the amplitude of the pulse train (such as in a fixed 5 V digital system), one has no control over the amplitude of the extracted signal. Third, each tone has a different amplitude -- for multitone signal generation, the variance may be intolerable. However, for simple test schemes where the user can manage with some or all of these parameters fixed, this method of analog signal generation may be the most compact.

+1, -1, -1, -1, -1, -1, -1, -1

(a) logic data pattern



(b) frequency spectrum

Fig. 2.4 - Example of a Pulse Waveform and Its Frequency Spectrum

Implementation of the pulse generator can take several forms. One application requires the use of a counter to keep track of the number of +1s or -1s, as in Fig. 2.5(a). By programming the counter to vary the number of ±1s, the user obtains frequency selectivity, albeit a limited range. The alternative is a pattern storage approach. The first is a simple chain of memory elements such as flip-flops as in Fig. 2.5(b). The pattern is loaded into the chain which is then configured into a loop so that the sequence can repeat itself. Next, the pattern is serially shifted out to generate the pulse train for a filter to select the appropriate tone or collection of tones with which the device under test will be stimulated. Alternatively, one can store and play back the pattern in a RAM as in Fig. 2.5(c). Read and write addresses are generated by a sequential address controller. We will refer to the approach of filling a scan chain or memory with a digital data pattern for analog signal generation as a memory-based generation technique, which could conceivably be used wherever analog signal generation is required. This will be examined more closely in *Chapter 4 - Forced-Periodic PDM Patterns.*

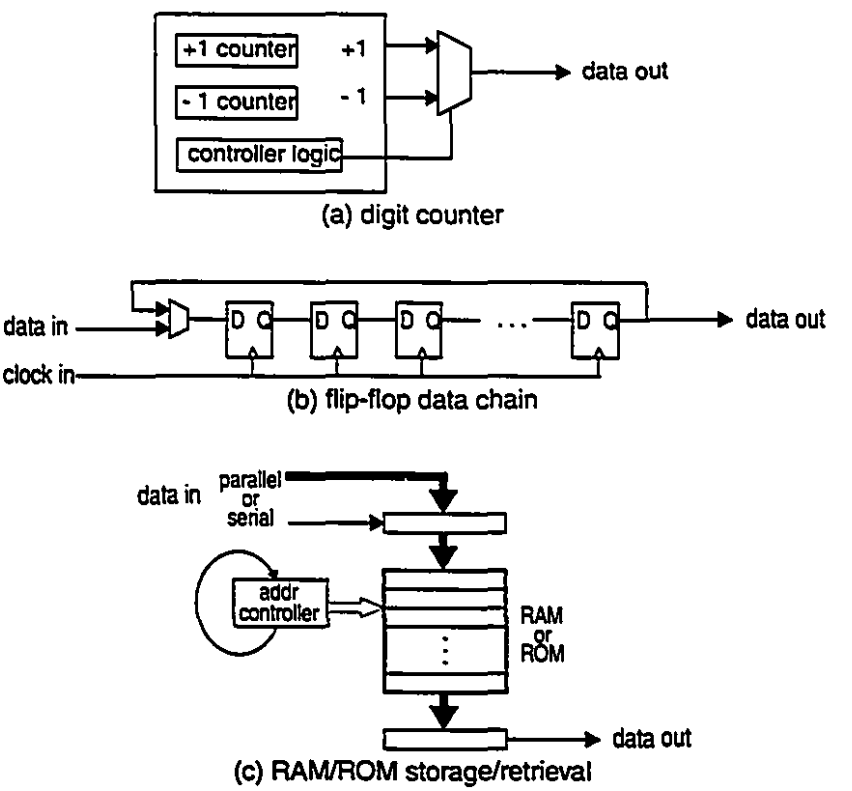


Fig. 2.5 - Bit Pattern Storage and Retrieval

Note that one could manipulate the bit pattern and add more +1s or -1s in different locations to generate different spectra and vary the power distribution. This is the basis behind multifrequency binary sequence signals and is discussed in the following section.

2.2.2 - MBS Generation

An extension of pulse generation is the binary representation of analog signals by multi-frequency binary sequence (MBS) generation, commonly used for multi-frequency test signals. MBS signals are periodic with an even number of bits per period and have a mean value of zero with their energy concentrated in a limited number of harmonics [6].

As an example, consider the case where one desires a signal containing six selected frequencies, one octave apart [7]. Assuming we let the function be even, and that we choose the Fourier series coefficients to all be equal, we arrive at the pattern $u(t)$, where

$$u(t) = \cos\frac{2\pi t}{T} + \cos\frac{2\pi 2t}{T} - \cos\frac{2\pi 4t}{T} + \cos\frac{2\pi 8t}{T} - \cos\frac{2\pi 16t}{T} + \cos\frac{2\pi 32t}{T},$$

and T is subdivided into N intervals. The binary signal is determined to be ± 1 depending of the polarity of $u(t)$, or equivalently, $sgn[u(t)]$[1] evaluated for each interval. For a total of 128 intervals, we find the first half of the even pattern to be:

$$5^+\,2^-\,14^+\,6^-\,1^+\,7^-\,1^+\,7^-\,2^+\,1^-\,7^+\,6^-\,2^+\,2^-\,1^+,$$

where the integer preceding the sign is the number of bits of that polarity. For example, 3^+ indicates three consecutive +1 bits. The resulting signal spectrum is given in Fig. 2.6.

For the simplest case (i.e. a single-tone frequency spectrum), consider the signal $s(t)$, where

$$s(t) = \sin\left(\frac{2\pi t}{T}\right).$$

1. Recall that the sgn function has the following definition:

$$\mathrm{sgn}(x) = \begin{cases} 1, & x > 0 \\ 0, & x = 0 \\ -1, & x < 0 \end{cases}$$

Let N be the number of points over the interval of interest (i.e., one period of the waveform). The sign of the function evaluated at each interval $t = k/N$, $k = 0, 1, 2, \ldots, N$, determines the binary representation via the *sgn* function. Since the signal is a sine wave, exactly $N/2$ bits are +1 and $N/2$ bits are -1. This generates the fundamental tone at $1/(NT)$ Hz, but unfortunately places harmonics at every integer multiple of twice the fundamental. This is illustrated in Fig. 2.7. Here, we encode the sine wave according to the MBS strategy and get the even function coding pattern of $32^{+}\ 32^{-}$. This creates a 128-bit pattern, which places the fundamental at $f_t = \frac{1}{128} f_s$. In Fig. 2.7, f_s = 1 MHz, placing the fundamental at f_t = 7.8125 kHz, and the harmonics at integer multiples of $2f_t$, or every 15.625kHz thereafter.

MBS is most often used for the generation of multi-frequency signals. While the opportunity exists for distributing the power over the harmonics of interest [7], optimization techniques must be used to achieve this. Again, unwanted harmonics that fall within the band of interest are generated. One advantage that MBS has over the pulse technique is that since MBS signals are even functions in time, only half of the full pulse train need be stored.

Those deficiencies that exist in the pulse method, however, also exist in MBS. For arbitrary analog signal generation, the amplitude is fixed unless the pulse train amplitude can be varied. Also, there lies difficulty in signal extraction from the bit pattern. Consider the previous example in which a sine wave was generated. From the frequency spectrum, we can see that a filter could extract the fundamental tone to yield a high-quality sine

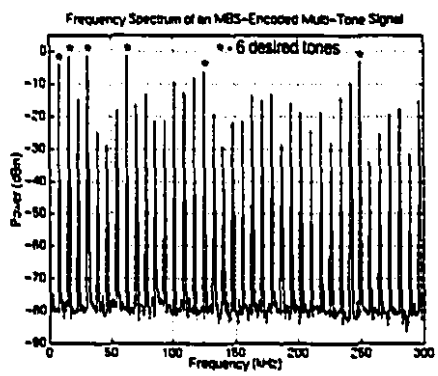


Fig. 2.6 - Spectrum of an MBS-Encoded 6-Tone Signal

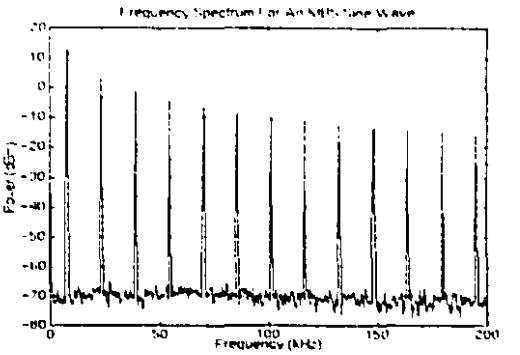


Fig. 2.7 - Spectrum of an MBS-Encoded Sine Wave

wave. Unfortunately, this requires a precise, tunable, high-order lowpass filter in order to remove the harmonics from the passband.

Implementation of the pulse generator and the MBS signal generator would typically be done using memory elements on an IC, such as a chain of flip-flops that would be loaded with the bit pattern and then configured in a loop to repeat itself. Alternatively, a RAM or counter logic (as described in *Section 2.2.1 - Pulse Generation*) could be used.

Ideally, we would like a bit pattern in which we can vary the amplitude of the encoded signal while maintaining a constant pulse train amplitude (e.g., 5 V for a digital IC application). We would also like to have frequency selectivity and be able to remove the harmonic noise from the band of interest so that the analog signal can be easily extracted. We may also want to create sophisticated multi-tone signals. All of this can be accomplished with pulse-density-modulation encoding, the subject of the next section.

2.2.3 - PDM Signal Generation

Pulse density modulation is the pattern generator of choice for oversampling D/A and A/D converters using single-bit $\Delta\Sigma$ modulation [3]. A typical modulator has the structure shown in Fig. 2.8(a), consisting of a summer, a linear filter, and a one-bit quantizer. By modelling the quantizer as an additive white noise source, we can obtain the linear model as in Fig. 2.8(b), and describe the modulator in terms of its signal transfer function (STF) and noise transfer function (NTF) in the z-domain:

$$Y(z) = STF(z)X(z) + NTF(z)Q(z)$$
$$NTF(z) = \frac{1}{1 + H(z)} \qquad (2.3)$$
$$STF(z) = 1 - NTF(z).$$

For the modulator to be stable, the NTF must be bounded at all physical frequencies. Stability has been shown to exist for $NTF < 2.0$ [8]. A modulator can realize any NTF whose numerator and denominator have identical orders and leading coefficients, i.e., for $NTF(z)|_{z=\infty} = 1$ [9]. It is desirable to have an STF equal to one so that the signal is not attenuated or amplified in any way. Such a modulator has the structure as shown in Fig. 2.9(a).

An example of a first-order, single-bit, digital ΔΣ modulator is given in Fig. 2.9(b). It is made up of a multi-bit summer and integrator, a multi-to-single-bit quantizer block, and a single-to-multi-bit digital-to-digital converter. The integrator consists of a multi-bit summer and a delay element, denoted by its z-domain representation, z^{-1}. The delay element is simply a data register or bank of flip-flops. The function of the quantizer is to set the output to a logic-1 if its input is greater than a set threshold, and a logic-0 otherwise. The digital-to-digital (D/D) converter performs a code conversion by converting the output signal to a multi-bit signal (either the largest or smallest number in the number system being used), and feeding it back to the modulator input. This introduces an error signal -- the difference between the single-bit output signal and the multi-bit input signal. The output of the modulator is now a single-bit representation of the multi-bit input signal, with the encoded signal embedded in a PDM representation. That

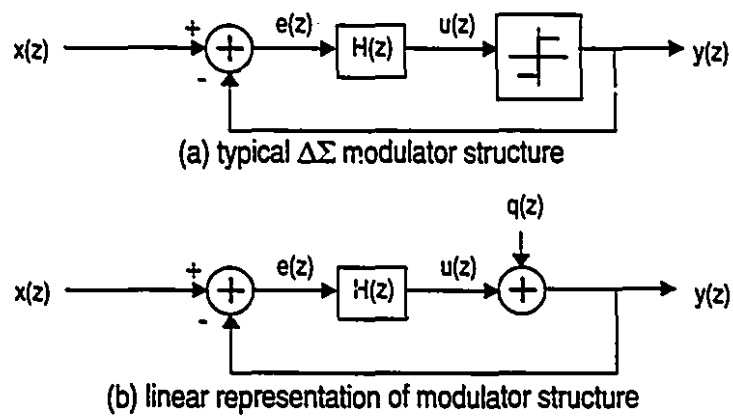
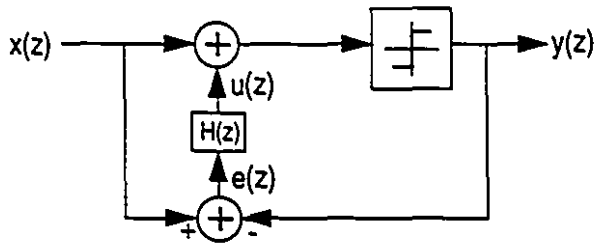


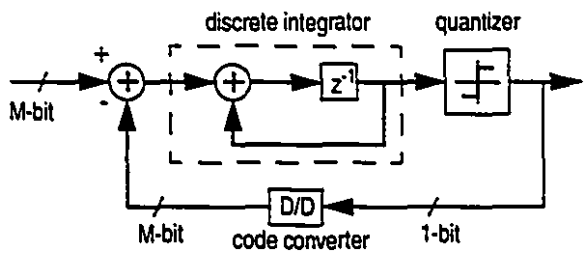
Fig. 2.8 - Typical and Linear Modulator Structures

is, the greater the amplitude of the signal, the more logic-1s used to represent it. Conversely, the smaller the amplitude, the more logic-0s used. Higher order modulators can also be created, such as the second-order design shown in Fig. 2.9(c). These better approximate the error signal fed back to the modulator input and, as a result, decrease the amount of inband error noise.

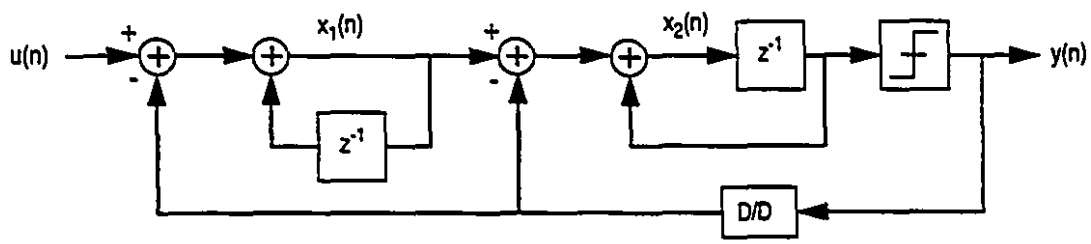
Figure 2.10(a) illustrates the conversion of a sinusoidal input signal into a PDM bit pattern. The input sinusoid has an amplitude of A and a frequency f_t that has been greatly oversampled (i.e., $f_s >> f_t$). The output signal of amplitude Δ, provided in Fig. 2.10(b),



(a) unity STF $\Delta\Sigma$ modulator structure



(b) quantized 1st-order $\Delta\Sigma$ modulator



(c) 2nd-order $\Delta\Sigma$ modulator

Fig. 2.9 - First- and Second-Order Modulator Structures

shows the digital pattern that represents the input sinusoid by the density of logic-1s and 0s. It is important to note that the ΔΣ modulator is based on an infinite-impulse response system which maps the input signal to an infinitely-long series of bits. Thus, the pattern does not repeat itself [3]. Another characteristic of the ΔΣ modulator is fact that the quantization noise is orthogonal to the input signal and thereby occupies a different frequency region. In the case of a lowpass modulator, the majority of the noise occurs at higher frequencies. This characteristic is known as "noise shaping". A typical power spectral density (PSD) plot of the output is given in Fig. 2.10(c).

Since quantization noise is orthogonal to the inband tones, signal extraction from the digital pattern is very easy. For a lowpass modulator, such as in the previous example, one simply passes the data pattern through a lowpass filter with a cutoff frequency f_B, as shown in Fig. 2.11. Note that the order of the modulator dictates the noise shape, i.e. the rate at which the noise increases out-of-band. This places the requirement that the filter be of at least the same order (preferably greater) to completely filter the out-of-band noise. However, it cannot remove the in-band noise as this noise cannot be removed from the signal by simple filtering.

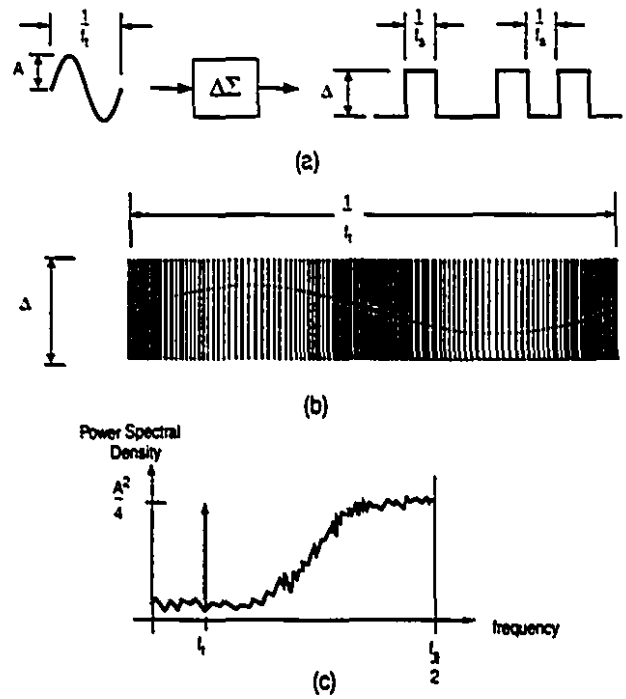


Fig. 2.10 - Modulator-Based Encoding of a Sinusoid

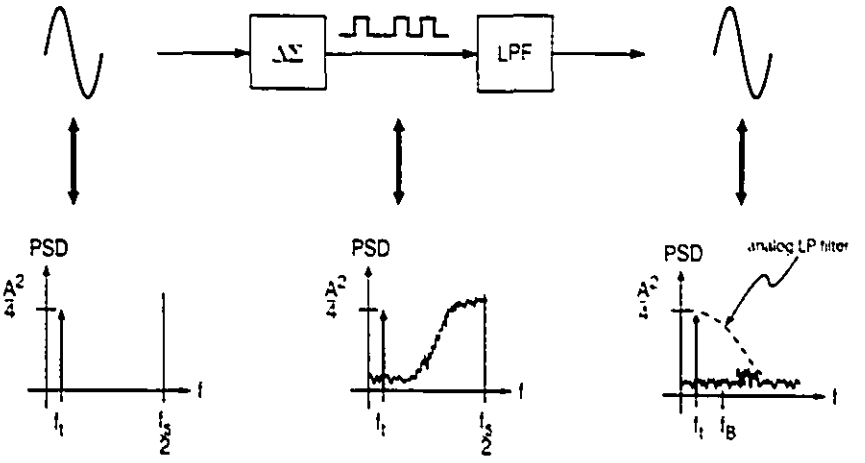


Fig. 2.11 - Analog Signal Recovery

The in-band noise can be reduced by using a higher-order modulator which better approximates the quantization error and thus results in a lower in-band noise floor. This is exemplified in Fig. 2.12. Note how the power density spectrum of the second-order lowpass modulator has a higher noise floor in the passband versus the fourth-order modulator. The simulation of a fourth-order design yielded a 30 dB increase in dynamic range to 110 dB. Another alternative for reducing the noise component is to increase the oversampling ratio (OSR), defined as $\frac{f_s/2}{f_B}$, where f_s is the sampling frequency and f_B is the modulator bandwidth. For a second-order design, the signal-to-noise ratio in decibels as a function of the OSR can be expressed as:

$$SNR = 15\log_2 OSR + 6\log_2\left(\frac{A}{\Delta}\right) - 8 . \qquad (2.4)$$

The above equation suggests that the higher the OSR, the closer the conversion is to ideal.

Perhaps the most powerful property of PDM encoding is that signal amplitude and frequency are completely programmable and can be recovered with a fixed-bandwidth filter. That is, we can place a signal (or group of signals) anywhere within the passband and recover it with a fixed filter tuned to the bandedge; it is not necessary for the filter to track the signal. This is demonstrated experimentally in Fig. 2.13. Here we show reconstructed signals of differing amplitude (a) and differing frequency (b), all generated within a 10 kHz passband region.

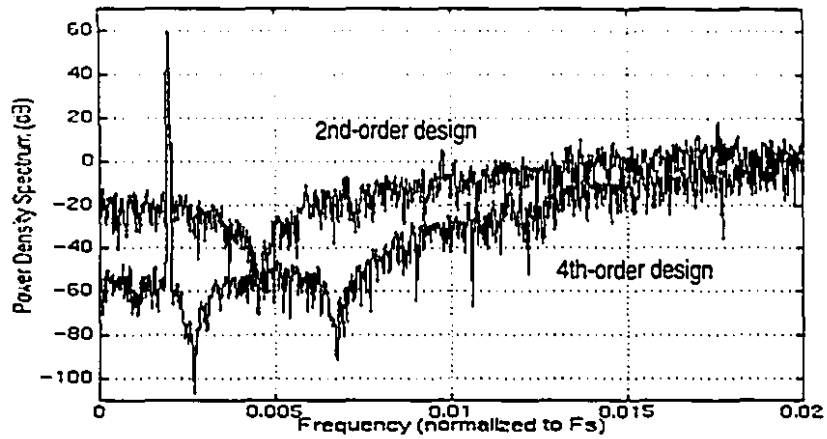
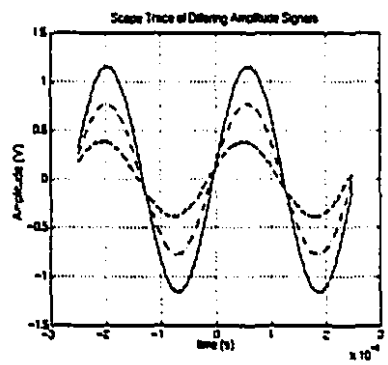


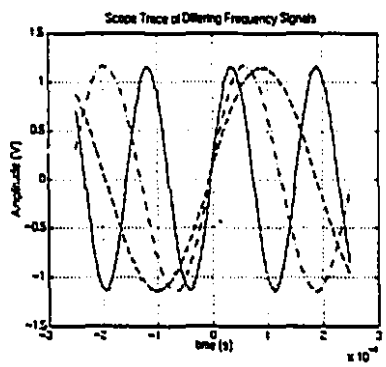
Fig. 2.12 - Second- and Fourth-Order Modulator Inband Power Spectra

PDM has the advantage of being able to encode other types of waveforms, such as multi-tone and triangular signals via $\Delta\Sigma$ modulation as illustrated in Figs. 2.14(a) and (b). It is important to ensure that the modulator bandwidth is sufficiently wide to include all of their harmonics, since these signals have significant power at higher-frequencies. However, since the quantization noise power increases with frequency, a fundamental trade-off exists between signal purity and noise [10].

The versatility of $\Delta\Sigma$ modulators makes them the preferred analog signal encoding scheme of the author for many reasons. First, the user has amplitude and frequency selectivity of the signal to be encoded. Second, the noise-shaping characteristic ensures that only the



(a) differing amplitude



(b) differing frequency

Fig. 2.13 - Amplitude and Frequency Variability Over a Fixed Bandwidth

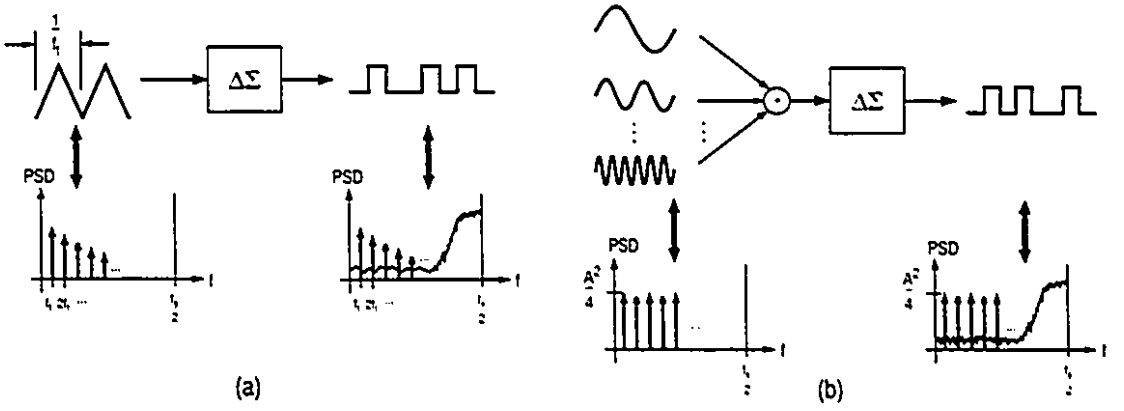


Fig. 2.14 - Encoding Other Types of Analog Signals

signal tone(s) exists in the passband region (plus, of course, a minimal amount of quantization noise). Third, ΔΣ modulators permit the encoding of virtually any waveform into a single-bit pattern. And finally, signal reconstruction is achieved simply by using a filter of a fixed bandwidth, unlike that required by the pulse and MBS signal generation methods. In the following section, we will focus on a primary use of the ΔΣ modulator -- the ΔΣ oscillator.

2.3 - Delta-Sigma Oscillator

Previous work on analog oscillators introduced the concept of using ΔΣ modulators in digital resonator circuits [1] and can be summarized with the following example. Figure 2.15(a) shows a second-order digital resonator circuit made up of two integrators in a loop, with a characteristic equation given by:

$$z^2 + (a_{12}a_{21} - 2)z + 1 = 0 . \qquad (2.5)$$

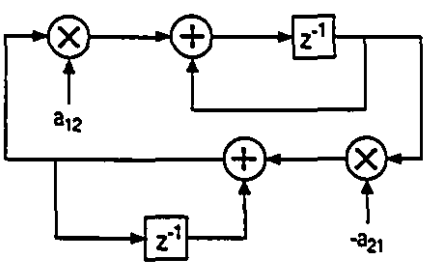
With some flow graph manipulation and the introduction of a ΔΣ modulator, we arrive at the circuit shown in Fig. 2.15(b). Keeping in mind that we wish to fabricate this design on a monolithic IC, it is desirable to keep the hardware complexity to a minimum (and also minimize logic area). Logic subject to minimization is the multipliers. By forcing the coefficient a_{12} to be a power of two, we can remove the first multiplier, as a power-of-two

multiplication is simply a wire-mapping in hardware. Next, realizing that the output of the modulator is either a logic-1 or 0, the second multiplier can be simplified to a two-input multiplexer which chooses between either $-a_{21}$ or $+a_{21}$. The end result is the minimized circuit shown in Fig. 2.15(c).

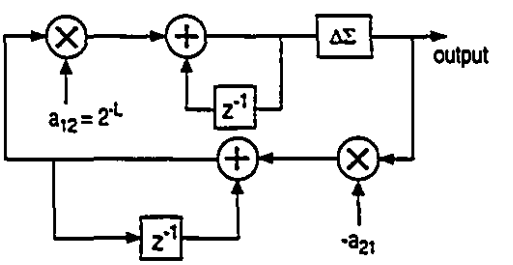
The memory elements in each integrator set the initial conditions of the resonator (denoted x_1 and x_2 in Fig. 2.15(c)). These, combined with coefficient a_{21} (which we will subsequently refer to as the loop coefficient k), create the variables that allow for very accurate frequency and amplitude tuning. The frequency of oscillation f, and the amplitude A, of the encoded signal are related to the loop coefficient and the initial register conditions by the following set of expressions:

$$\begin{aligned} k &= 2(1-\cos 2\pi f) \\ x_2(0) &= A \\ x_1(0) &= \frac{k}{2}x_2(0) \end{aligned} \qquad (2.6)$$

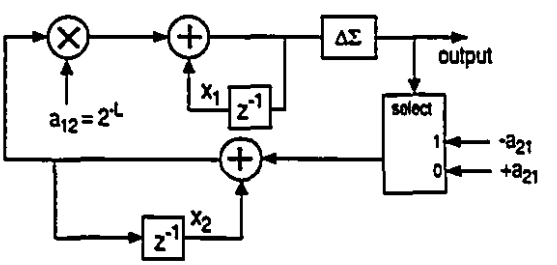
The $\Delta\Sigma$ oscillator has several advantages with the main ones discussed next.



(a) 2nd-order digital resonator circuit



(b) resonator with $\Delta\Sigma$ modulator and power of 2 multiplier



(c) multiplierless $\Delta\Sigma$ modulation oscillator

Fig. 2.15 - Design of a Multiplierless Delta-Sigma Oscillator

Signal generation logic is self-contained.

That is, all logic and frequency selectability can be built into a single resonator-$\Delta\Sigma$ modulator structure. This lends itself to IC fabrication, most likely on a single die. With programmable registers, arbitrary signal frequencies (within the predetermined passband) and amplitudes can be generated. Thus the need for external, off-chip signal generation equipment is eliminated.

The PDM stream is repeatable.

Since the start-up states of each integrator in the oscillator design are known, the bit pattern is completely deterministic. With the same initial conditions, the output stream can therefore be reproduced.

However, the oscillator, having many predetermined attributes such as order, bandwidth, and the number of simultaneous tones, suffers from the following disadvantages:

Signal quality and bandwidth are fixed.

The bandwidth of the passband and the dynamic range of the generated signal are functions of the order of the modulator and its coefficients, and thus are determined beforehand. As a result, one must carefully select the desired order and modulator characteristics for a desired SNR during the design phase of the oscillator.

Higher-order structures require large increases in area.

Generally, a desired increase in bandwidth or SNR requires an increase in the order of the oscillator. Frequency selectivity also necessitates an increase in register length (data bus width) to minimize the effect truncation noise has in increasing the signal noise floor. In addition, the generation of multiple tones or complex waveforms require and bandwidth extension at the expense of SNR and more logic. As order (and hence area) increases, the feasibility of oscillators for MADBIST applications decrease i.e., the MADBIST overhead is no longer a negligible amount.

It is difficult to ensure stability for a given modulator design.

As one attempts to maximize the SNR for a given order or modulator structure, the potential for instability (i.e. an overflow condition) increases. One limiting factor is the amplitude of the encoded signal. In general, the amplitude is kept low to ensure stability. Presently, there is no easy way to guarantee stability other than through very long simulations or bench-testing.

The coefficients (initial conditions and loop coefficient) must be kept small for a high OSR.

The fact that the coefficients must be small in our number system requires the use of larger bus widths to minimize the effect of truncation noise, since we are using fixed-point arithmetic.

Despite these deficiencies, the ΔΣ oscillator has some very practical applications. Research in the area of ΔΣ modulators by Haurie and Roberts has revealed an area-efficient, multiplier-free structure for arbitrary-order modulators [9]. This design algorithm has been conveniently packaged in a software application written in Matlab, called DSMOD [10]. One advantage of the software is the ability to generate ΔΣ oscillators using an area-efficient structure, as introduced in [11]. This software has proved to be a very useful ΔΣ modulator and oscillator design tool. Two applications using the ΔΣ oscillator will be discussed in detail in the following chapter.

Chapter 3 - Applications of the Delta-Sigma Oscillator

This section highlights applications utilizing the ΔΣ oscillator. The MADBIST proposal introduced in *Section 2.1 - The MADBIST Method of IC Self-Test* covers one such application in detail and will not be covered here. Instead we will focus on applications in which logic area is not a constraint -- that is, where a single IC or significant portion of an IC is dedicated to the oscillator.

This chapter will introduce the dedicated test system, which is directed at the analog tester market. High precision analog testers have a purchase price in the vicinity of $1 million. In contrast, digital testers cost approximately $100,000. With the proposed dedicated test system (that could be mass-produced for say, $20), the test engineer can equip the digital tester to perform functions normally reserved for the analog test unit. We will examine a dedicated test system for use either as an on-board unit or as a retrofit for a digital tester.

The following sections will also introduce two oscillator ASICs, fabricated in the Nortel 0.8μ BiCMOS fabrication process. The first is an all digital, fourth-order lowpass ΔΣ oscillator. The second consists of the same oscillator, a one-bit DAC, and a sixth-order lowpass reconstruction filter to form a complete analog signal generation unit.

3.1 - The Dedicated Test System

One application for the ΔΣ oscillator in the context of analog signal testing is in a test system consisting of one or more dedicated ICs to perform the signal generation and data collection functions. An example of such a system is shown in Fig. 3.1. Although represented in the context of a board system, the entire system can be fabricated on a

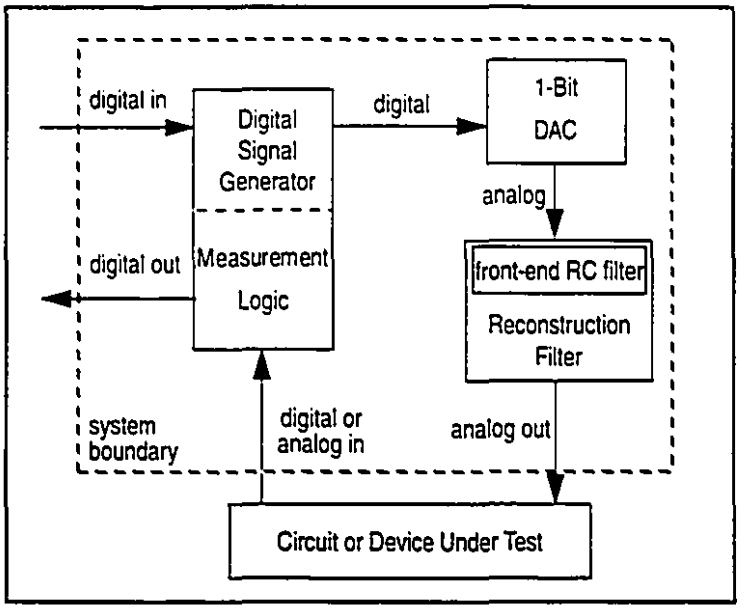


Fig. 3.1 - Block Diagram of a Test System

single die, yielding a single test-chip retrofitting solution. The operation of the test system is described below.

The test system can be designed with either a memory- or oscillator-based signal generation approach or conceivably both. First, a digital controller, typically a processor or a digital test head, communicates with the signal generator to either load a serial bit pattern (in the memory-based configuration) or the initial conditions necessary for an oscillator to generate a test signal. That resulting serial output is then fed into a one-bit DAC.

The purpose of the DAC is twofold. First, the DAC can clean up the edges of the digital input signal, providing a signal with sharper level transitions. Second, the DAC can change the coding of the digital signal from its typical 0 to 5V non-return-to-zero scheme to one that has better characteristics. Using a bipolar, return-to-zero bit coding pattern reduces distortion by equalizing rise and fall times. For example, to reconstruct a high-quality analog signal, it is critical that the rise and fall shape of the digital signal be as similar as possible i.e., the area under each pulse is identical. Figure 3.2 illustrates this in detail. Note that pulse 1 does not have the same area as pulse 3, since pulse 3 is followed

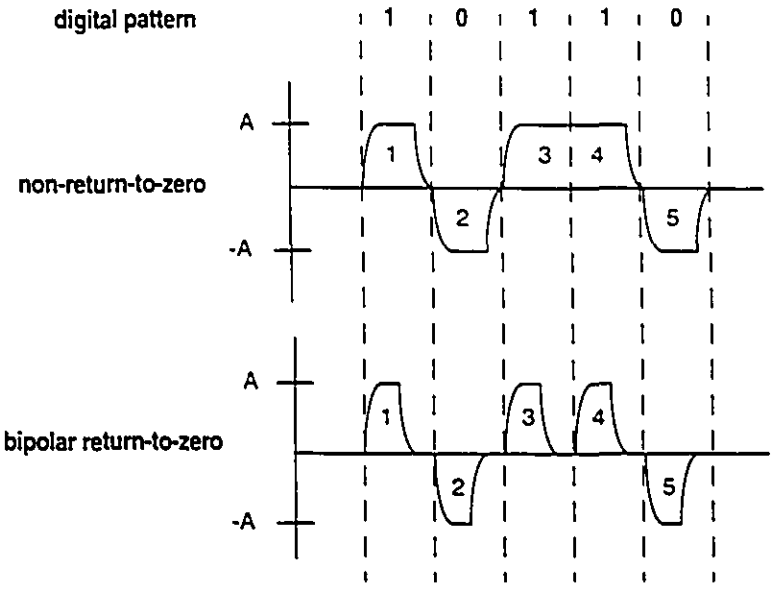


Fig. 3.2 - Bipolar Non-Return-to-Zero and Return-to-Zero Coding Schemes

by another pulse of the same polarity. As a result, pulse 3 does not need to discharge towards zero. This gives the appearance that pulse 4 has a zero-time rising edge. A bipolar return-to-zero coding pattern forces each pulse, regardless of polarity, to return to zero halfway through the period of the pulse. This ensures each pulse has one rising and one falling edge, minimizing the area differences. A bipolar coding scheme also removes the DC bias associated with 0-5 V coding, as the average will be zero (assuming an equal number of logic-1 and 0s[1]). The DAC can also provide a high output impedance for the reconstruction filter. This minimizes the loading placed on the filter by the output stage of the previous circuit.

The next stage is the reconstruction filter. This filter is generally a lowpass[2] structure that has its cutoff frequency at the bandedge of the frequency spectrum of interest. It is this filtering action that extracts the analog signal from the digital bit stream. The output of the filter is the reconstructed analog signal that is then sent to the analog device under test (DUT). As the out-of-band noise from a $\Delta\Sigma$ modulator will increase at a rate that is

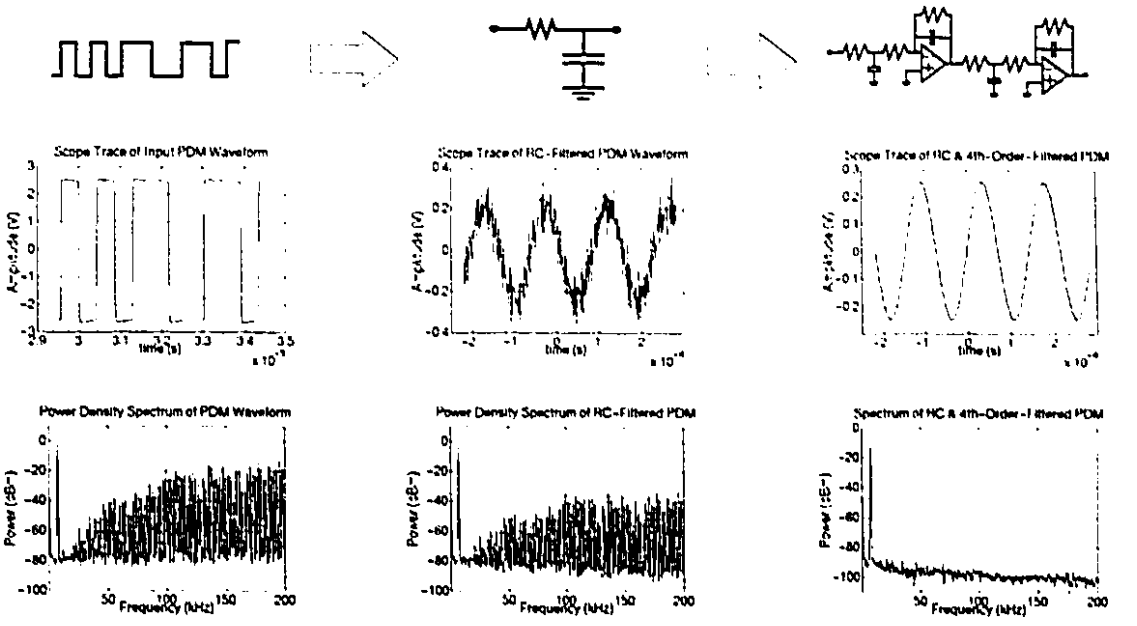
1. Recall that in a ±1 bipolar coding scheme, a logic-0 is coded as -1.
2. Note that with just a change of filter, the system could make use of $\Delta\Sigma$ bandpass signals. This would prove effective in high-frequency testing such as in wireless applications. See [12] for further details.

proportional to the order of the modulator, it is advisable to make the filter at least one order above the maximum order of the modulator used. This will minimize the amount of noise that accompanies the signal.

If the reconstruction filter cannot handle the rail-to-rail swing from the DAC, then a simple fixed-bandwidth filter structure can be used to reduce the signal input amplitude (as introduced in *Section 2.1 - The MADBIST Method of IC Self-Test*). Note that this filtering circuit should be part of the design constraints for the front end of the reconstruction filter and used regardless of the mode of operation (normal or test mode). Alternatively, a simple passive RC structure could be used if BIST were added to an existing design. This significantly reduces the output amplitude and relaxes the steep slope of the digital signal to an input level which the filter could easily handle. An experimental demonstration of signal reduction possible with use of an RC filter is provided in Fig. 3.3.

Using a 7 kHz PDM bit pattern from a third-order modulator with a bandedge of 18 kHz, a ±2.5 V signal PDM bit pattern (and its frequency spectrum) is generated as shown in Fig. 3.3(a). The input is then fed into a first-order RC circuit with a cutoff frequency of 18.8 kHz. The waveform in the time and frequency domains is given in Fig. 3.3(b). Note the substantially-reduced signal waveform from a 5 V swing to approximately a 0.7 V swing as well as a noticeable attenuation of higher-order frequencies in the spectrum plot. To complete the signal reconstruction, the output of the RC filter is fed into a fourth-order lowpass filter with a cutoff frequency of 18 kHz. Figure 3.3(c) shows the end result: a reconstructed sine wave with a 0.25 V amplitude and a dynamic range of approximately 75 dB.

The final component of the dedicated test system is the measurement logic. It is designed to receive either a digital or analog input and characterize the performance of the DUT through a quantitative measurement. Such functions may include a Fast Fourier transform (FFT) or narrow-band filter [2]. It is anticipated that further research in the area will lead to simple and compact data measurement schemes.



(a) input PDM stream (b) RC-filtered PDM stream (c) reconstructed analog signal (4th-order lowpass filter)

Fig. 3.3 - Use of an RC Filter To Reduce Input Signal Amplitude

Up until now, we have only considered the type of signal being generated. However, we need to understand the requirements of the input device we are stimulating. That is, we must decide whether we require a voltage or current signal source. We will show in the following section how a PDM output can be configured for either mode of operation.

3.2 - Voltage and Current Signal Generation

Depending on the device under test, it may be necessary to drive the circuit with either a voltage or current signal. This requires the appropriate interface between the PDM pattern generator logic and the device. When an input voltage signal is required, we require an output stage that has a low output resistance to prevent changing the circuit characteristics. This can be accomplished with a buffer circuit such as the type shown in Fig. 3.4(a). It is the familiar class B amplifier configuration. An amplifier of the class A type could also be used, but is less power-efficient. When an input current signal is required, we need a circuit with a very high output impedance. The solution is to use a circuit similar to that shown in Fig. 3.4(b), consisting of several analog switches and current sources. With a low

input logic level, a current of I_o is pushed into the input node of the device under test. Conversely, with a high input logic level, a current of I_o is pulled from the input node. Alternatively, if good control can be exercised over the digital signal that drives the analog switches, then we could replace the circuit of Fig. 3.4(b) with the simple CMOS inverter circuit shown in Fig. 3.4(c). The inclusion of an inverter circuit maintains the overall digital nature of the signal generator and avoids complicated current source design. With an input signal level of V_{DD} applied to the inverter circuit, the current pulled from the input terminal of the device under test will be given by

$$i_o = \left(\frac{W}{L}\right)_n \mu_n C_{ox}(V_{DD} - V_t)^2 . \tag{3.1}$$

Conversely, with an input signal level of V_{SS}, the current pushed into the device will be

$$i_o = \left(\frac{W}{L}\right)_p \mu_p C_{ox}(V_{SS} - V_t)^2 . \tag{3.2}$$

The level of the output current can therefore be set by the aspect ratio of the NMOS and PMOS devices. It is inevitable that some mismatch will result between the two output current levels, as they depend directly on device parameters which are process and temperature dependent. However, through careful simulation or prototyping, we can compensate for this error by encoding a digital offset signal into the PDM stream.

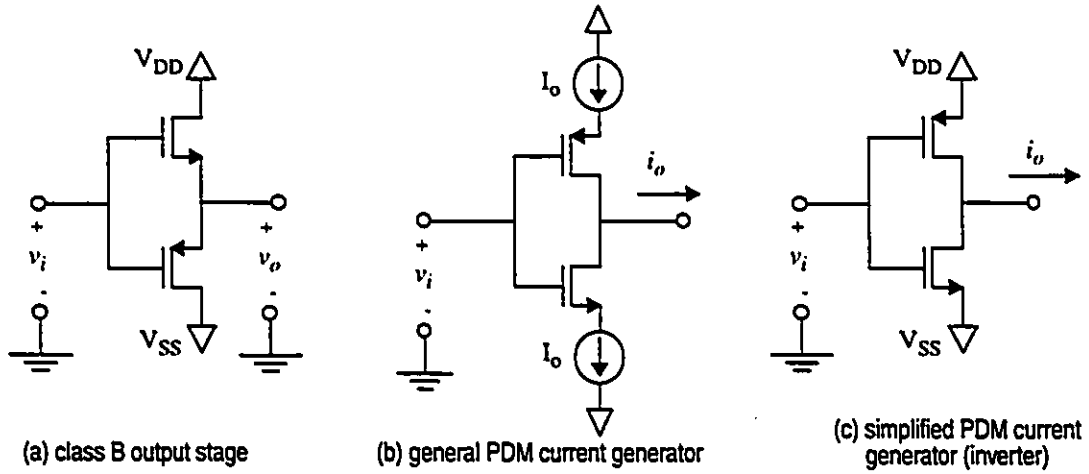


Fig. 3.4 - PDM Current Signal Circuits

3.3 - Delta-Sigma Oscillator ASICs

This section focusses on the design of two $\Delta\Sigma$ oscillator ASICs that were fabricated using the Nortel 0.8µ BiCMOS process through the Canadian Microelectronics Corporation. The purpose of these designs was to fabricate an oscillator to perform on-chip analog signal generation through PDM-encoding. One application would be the digital signal generator block in the test system of Fig. 3.1.

3.3.1 - Delta-Sigma Oscillator Structure

The modulator structure chosen for fabrication in both ASICs is a fourth-order lowpass design, as highlighted in [9]. It has the signal flow graph as shown in Fig. 3.5. Each boxed z-domain expression can be modelled as an either a non-delayed or delayed integrator. These are referred to as the forward and backward Euler integrators, respectively, and are represented by the signal flow graphs in Fig. 3.6. The bus widths of the oscillator are set at 26 bits (25-bit mantissa, one sign bit) for the resonator circuit and 29 bits (25-bit mantissa, 3-bit integer, one sign bit) for the modulator. It was determined through simulation that 25 bits would provide the desired SNR and bandwidth and that four integer bits would prevent an overflow condition in the modulator.

The coefficients are selected to provide a normalized bandwidth given by $\frac{f_{3dB}}{f_S} = 0.0075$, or $f_{3dB}=150\ kHz$ for an f_S of $20\ MHz$, the specified circuit clock rate. These coefficients are given in Table 3.1 and all are powers of two. This eliminates the need for an area-consuming multiplier, since a power-of-two multiplication or division is simply a rewiring of a data bus in the digital domain (a shift-left or shift-right). Note the extra set of coefficients, denoted B'. These are the product of the A_n and B_n coefficients and are used to multiply the output of the integrator to generate a result equivalent to having multiplied by the A and B coefficients sequentially. This is done to avoid truncation errors caused by large divisions and multiplications being performed sequentially on small numbers.

Table 3.1 - Fourth-Order Modulator Coefficients

A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	B_1'	B_2'	B_3'	B_4'
2^{-10}	2^0	2^{-11}	2^0	2^9	2^8	2^{16}	2^{14}	2^{-1}	2^8	2^5	2^{14}

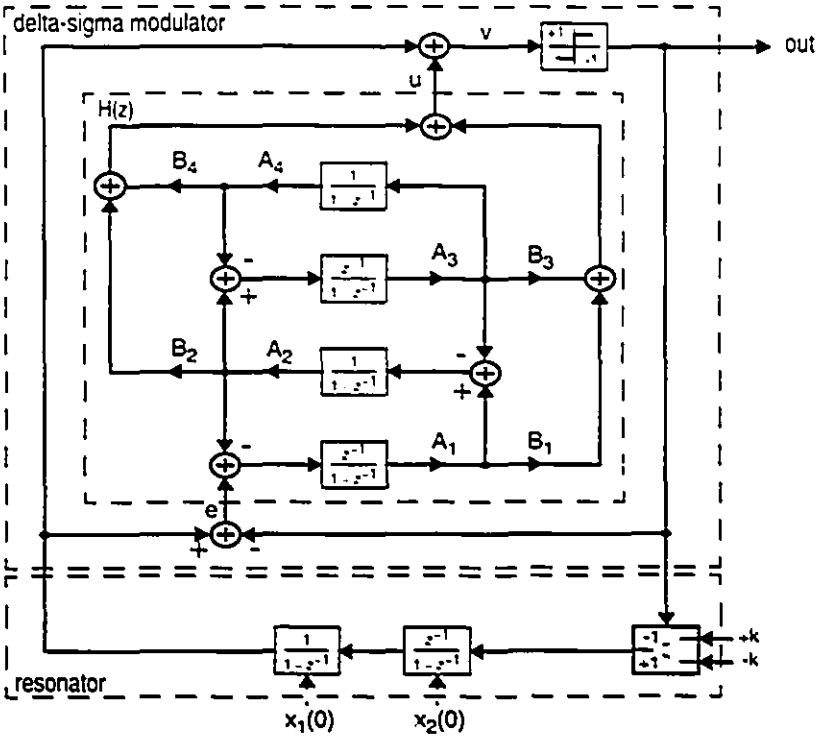
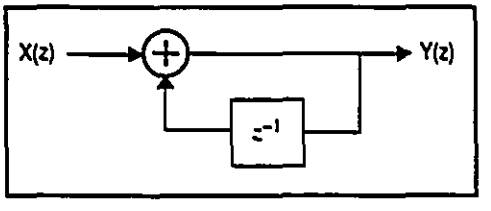


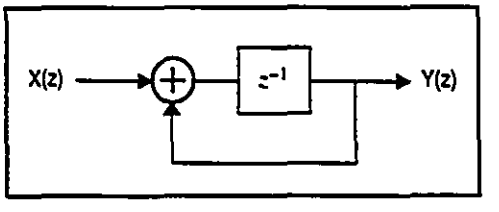
Fig. 3.5 - Signal Flow Graph for a Fourth-Order Delta-Sigma Oscillator

While the modulator structure is identical to that prescribed in [9], the resonator component has a slight modification. It was found through logic synthesis that reversal of the initial condition integrators yielded a shorter critical path, despite these integrators not being in the critical path themselves. The critical path is one major drawback of this modulator structure, as it limits the maximum sampling frequency. These and other inadequacies of the ΔΣ oscillator are highlighted in the following section.



$$G_F(z) = \frac{Y(z)}{X(z)} = \frac{1}{1-z^{-1}}$$

(a) forward Euler (non-delayed) integrator



$$G_B(z) = \frac{Y(z)}{X(z)} = \frac{z^{-1}}{1-z^{-1}}$$

(b) backward Euler (delayed) integrator

Fig. 3.6 - Forward and Backward Euler Integrators

3.3.2 - Deficiencies of the Delta-Sigma Oscillator

The greatest drawback to the concept of the on-chip $\Delta\Sigma$ oscillator is the area consumed by higher-order designs. With the structure described above, the total core area is approximately 6 mm^2 in a 0.8µ standard cell BiCMOS process. Total area consumption is driven mainly by two parameters: modulator order and bus width. Both are required for high SNR and bandwidth.

Another concern regarding higher-order designs is the critical path (the longest combinational path between storage elements), which grows with both the modulator order and the bus width. The critical path of the fourth-order design is highlighted in Fig. 3.7. As indicated in the figure, the critical path encompasses eight 29-bit adders. This long path of combinational logic limits the maximum clock speed at which the circuit can run. Simulation results have shown the maximum rate to be approximately 20 MHz under

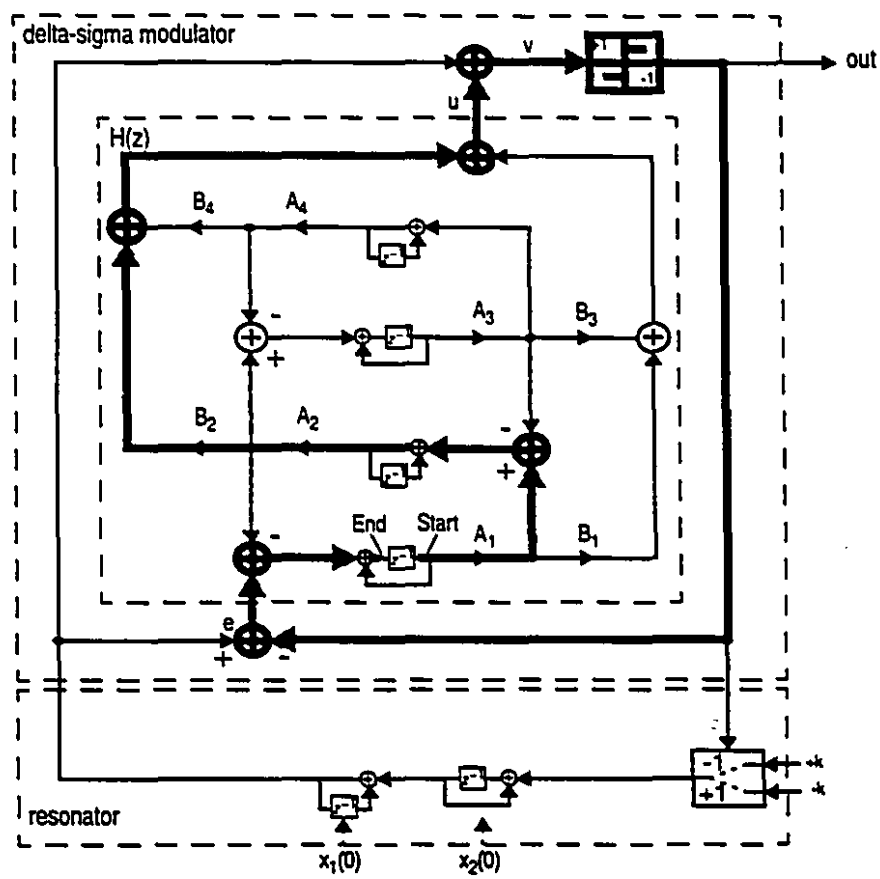


Fig. 3.7 - Critical Path for a Fourth-Order Delta-Sigma Oscillator

worst case conditions. There are several methods for improving the this design to maximize the clock rate (and thus increase the bandwidth or OSR). Three of the most practical methods will be discussed next.

Design into a faster technology.

The smaller intrinsic delays for individual elements in a standard cell process will improve the critical path. However, the increased costs (and decreased yields) make this an impractical solution for maximizing circuit speed. Note that custom layout should improve the critical path. However, the author suggests this route not be taken, as the intent of an oscillator design is that it be easily modified for varying specifications such as SNR, bandwidth, and area requirements.

Use more sophisticated data processing schemes.

Datapath techniques, such as the time-scheduling of adders, can be used to minimize area though not necessarily maximize speed. A note should be made about datapath pipelining: pipelining is a simple technique that minimizes critical paths by introducing delay elements into the datapath. Although this effectively increases datapath latency, latency is generally not an issue when designing DSP structures. Unfortunately, it is not easy to pipeline circuits that have feedback paths in them. Because of the main feedback structure that returns the modulator output to the resonator, it is believed impossible to pipeline the above structure.

Redesign the modulator structure.

An improved modulator structure will attempt to minimize the critical path at the expense of increased area. A structure with a smaller critical path than that used above has been proposed in [4][1]. Because of the availability of DSMOD, the $\Delta\Sigma$ modulator design program [10], the above structure was selected.

1. Unfortunately, the design highlighted in [4] does not have unity gain.

3.3.3 - Delta-Sigma Oscillator ASIC

An ASIC (chip code IBAMGOSC) was created using the ΔΣ oscillator described in the previous section. The intention of this design was to create a chip that contained just the PDM pattern generator. With respect to the dedicated test system of Fig. 3.1, it would represent the digital signal generator. The functional block diagram of the ASIC is given in Fig. 3.8.

The chip is comprised of four main sections. The first is the initial condition interface. It contains the resonator portion of the oscillator and the input data bus through which the initial condition registers, denoted $x_1(0)$ and $x_2(0)$, and the loop coefficient k can be programmed. This gives the oscillator arbitrary tone frequency and amplitude selectability. The second block is the ΔΣ modulator and is the same structure as illustrated in Fig. 3.5. The third block is the overflow detector. By exclusive-noring the integer bits of the output of a modulator integrator, an overflow condition can be detected. An overflow condition occurs when, for each integrator, its integer bits are not all the same. For example, if one of the modulator integrators has an output which has three 1s and one 0 comprising its four integer bits, it has overflowed. The last block is the clock driver. The circuit is designed to operate at 20 MHz and thus requires a clock driver capable of driving all memory elements in the design. A cascaded buffer structure ensures this.

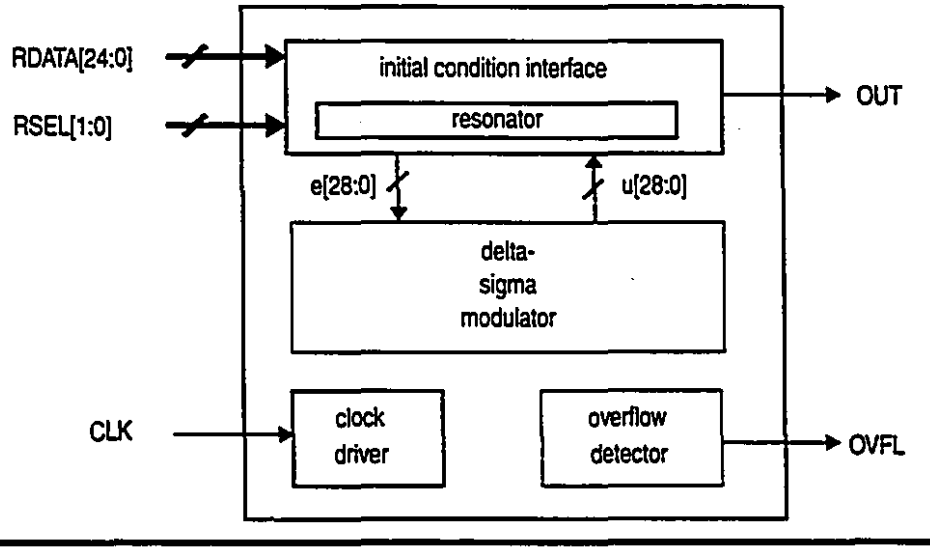


Fig. 3.8 - IBAMGOSC ASIC Functional Block Diagram

The ASIC was fabricated using BATMOS, a 0.8μ BiCMOS process of Nortel, and packaged in a 68-pin pin grid array. An illustration of the layout is given in *Appendix A.1*. For the detailed specifications of the IBAMGOSC ASIC, see [13]. Total core area is 2.6 mm x 2.3 mm with the area increasing to 3.9 mm x 3.5 mm when the I/O pads are included. As discussed previously, it is this large core area that makes higher-order oscillators impractical for use in MADBIST unless the modulator already exists elsewhere in the circuit and can be shared. In addition, the oscillator is fixed in its bandwidth and capable of only generating single-tone sine waves. Even with these limitations, its use in a dedicated test system is still very practical. The following section will present another ASIC that contains more components of the dedicated test system that collectively comprise a monolithic analog signal generator.

3.3.4 - Analog Signal Generator ASIC

In order to consolidate the analog signal generation operations into a single IC package, the one-bit digital-analog converter and reconstruction filter must be added to the design. This was the exercise explored in the mixed-signal ASIC (chip code IBAMGODF) [14]. In addition to the fourth-order ΔΣ oscillator, this chip contains a one-bit DAC and a sixth-order reconstruction filter. It thus contains all signal generation components and all elements of the dedicated test system of Fig. 3.1, with the exception of test measurement logic. The functional diagram of the chip is shown in Fig. 3.9 and has several different modes of operation.

The structure of the oscillator portion of the chip is very similar to IBAMGOSC; it contains the initial condition interface, which controls initial condition register and loop coefficient programming, and identical resonator and modulator structures. In addition to the single-bit output of the oscillator, we have an output bus tapped off the resonator. The bus outputs a multi-bit digital representation of the analog signal for use wherever a digital sine wave is required. The function of the clock driver and overflow circuitry are identical to that as before. The additional components are the one-bit DAC, which serves to clean up the digital signal, and the sixth-order lowpass reconstruction filter, which extracts the analog signal from the PDM bit stream.

In normal or self-contained mode, the output of the oscillator is fed into the DAC, which cleans the edges of the digital signal and reduces the signal amplitude so it does not overdrive the input stage of the filter. The DAC output can be fed into the filter by shorting the DOUT and FIN pins together. The resulting output on pin FOUT is the reconstructed sine wave which can be fed directly to the analog device under test (DUT). The ASIC has been designed so that each component can be run individually or as a combination of the other components. For instance, the DAC input can arrive off-chip from another signal source, be it a PDM signal or other digital representation of an analog signal. Its output can be sent off-chip for filtering or filtered on-chip as in normal mode. The filter can also be run individually, receiving its input off-chip, filtering the signal, and directing it towards the DUT. The availability of the above configurations not only gives the test engineer the versatility to conduct various test setups using all or part of the IC, but also simplifies the testing of this ASIC.

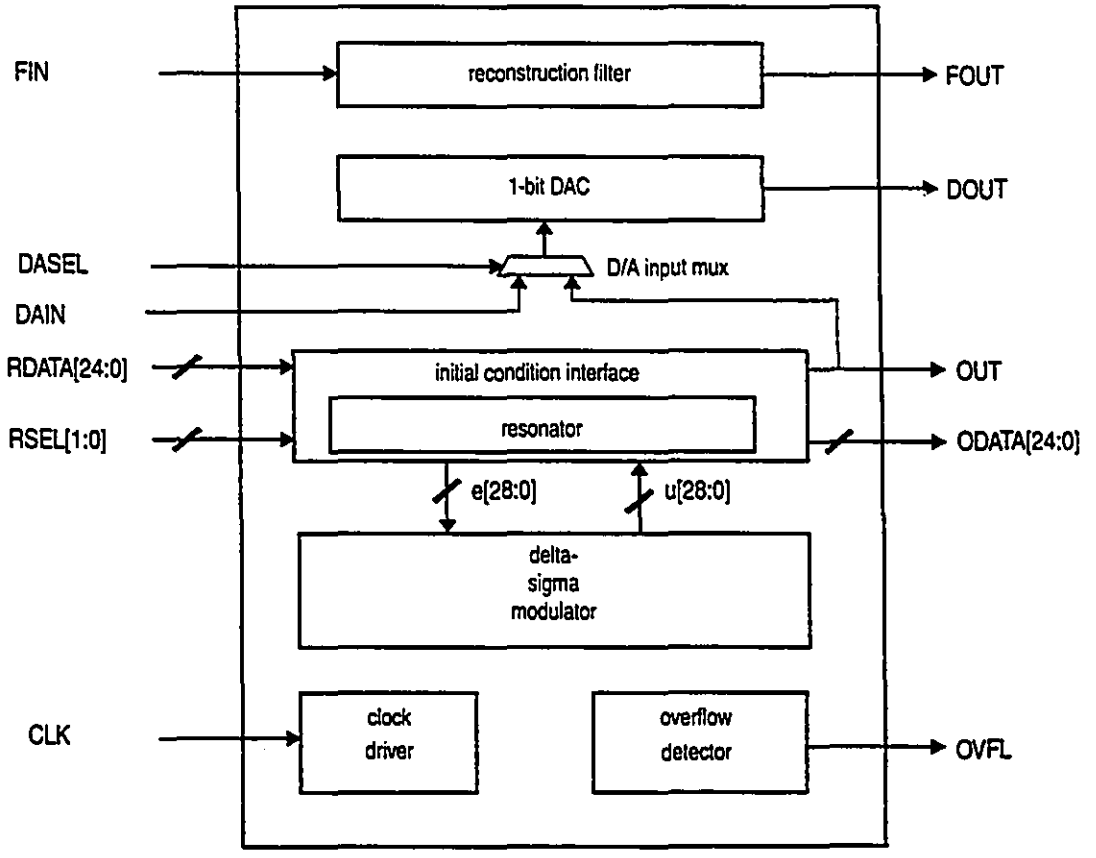


Fig. 3.9 - IBAMGODF ASIC Functional Block Diagram

The one-bit DAC was designed and laid out by Ara Hajjar of McGill University. It has a NRZ, bipolar output, centered about 2.5 V, so that its substrate will share the same potential as the digital circuitry. Note, however, that it has its own power supplies. This minimizes the possibility of digital switching noise degrading DAC performance. Its schematic is given in Fig. 3.10, with an illustration of the layout given in *Appendix A.3*. For a detailed description of the DAC, consult [15].

The reconstruction filter was designed and laid out by Vincent Leung, also of McGill University. It is a sixth-order lowpass structure, created by the cascading of three second-order biquad filters, and has six poles at 100 kHz. The biquad filters consist of RC circuitry surrounding an operational transconductance amplifier. A single biquad filter is shown in Fig. 3.11(a) with the transistor schematic of the biquad and its biasing circuitry given in Fig. 3.11(b). The 3 dB frequency of the filter is 35 kHz. Its layout is as shown in *Appendix A.4*, and has an approximate area of 1120 µm x 343 µm. For an in-depth description of the reconstruction filter, refer to [16].

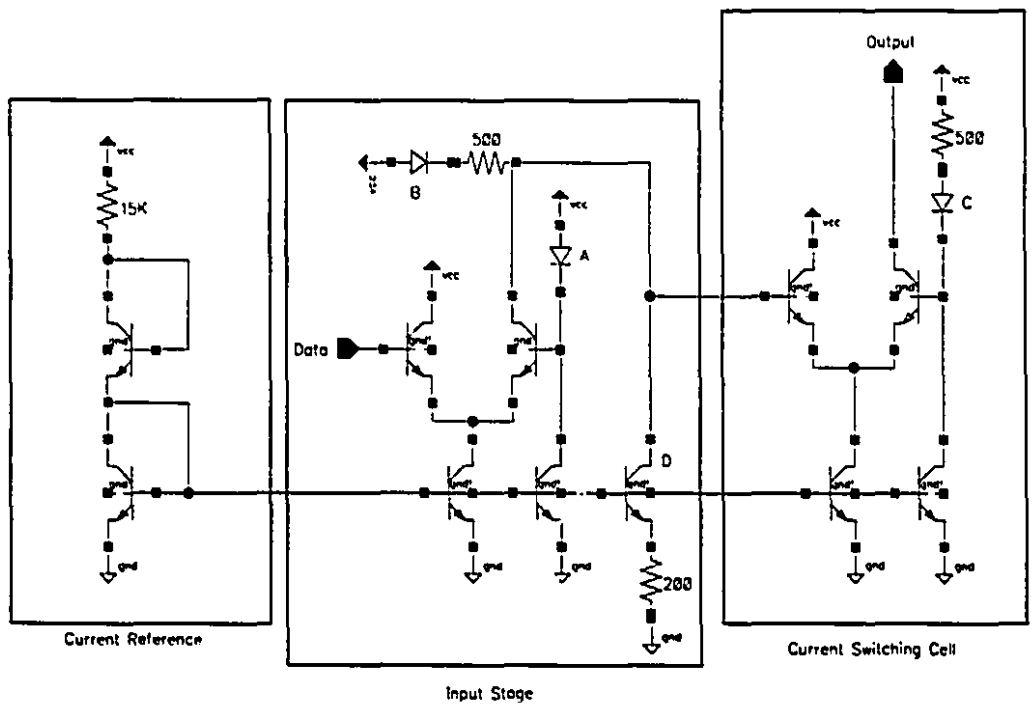
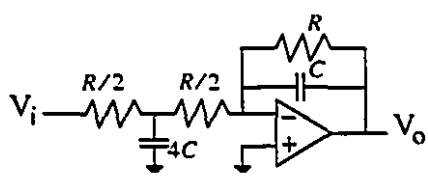


Fig. 3.10 - Schematic of BiCMOS One-bit DAC

Like the previous ASIC, the main disadvantage of this chip is area consumption and lack of programmability. The total area is 2.5 mm x 2.7 mm for the core and 4.6 mm x 4.3 mm for the entire die. The layout is given in *Appendix A.2*. While the complete analog generator is now fitted into a single package, the oscillator is limited to a fixed bandwidth (150 kHz at a 20 MHz clock rate) and fixed order (fourth-order $\Delta\Sigma$ modulator). It is capable of generating only single-tone sine waves. For complete design information on the ASIC, consult [14].

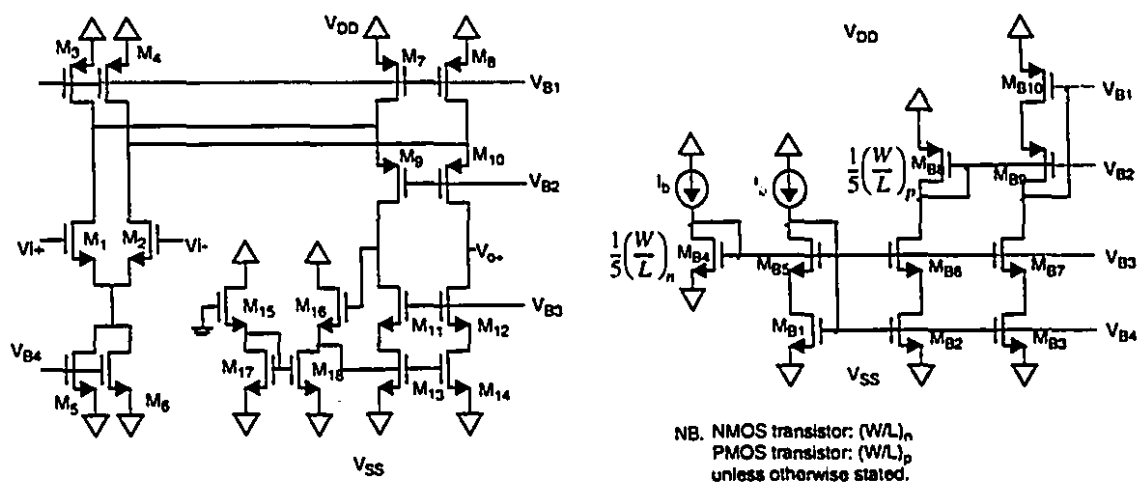
3.3.5 - Simulation/Experimental Results

A summary of the simulation results are covered in this section, and are broken down by component. Bench-testing of the ASICs yielded unacceptable results, as will be discussed in each section. However, the conclusion drawn from the experiments point to a failure of the chips caused by a problem in fabrication rather than a design error.



$$\frac{V_o}{V_i} = -\frac{1}{(1+sRC)^2}$$

(a) 2nd-order biquad filter and its transfer function



(b) OTA and bias circuit transistor-level schematic

Fig. 3.11 - Second-Order Biquad Filter Schematic

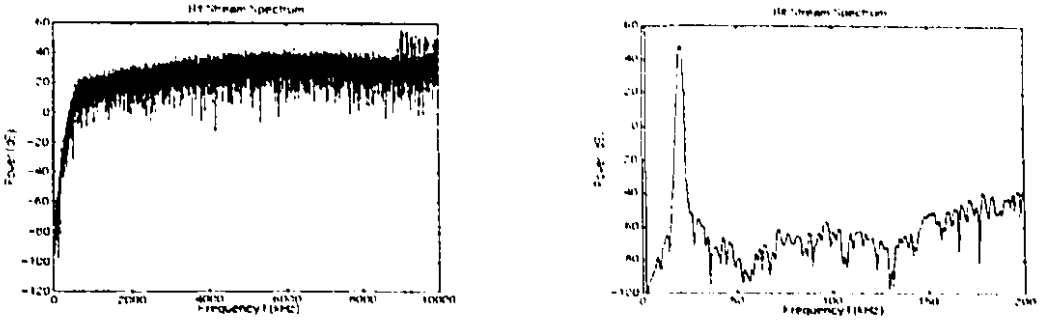
Delta-Sigma Oscillator

The digital portion of the ICs are identical and hence have identical performance characteristics. The oscillator has a bandwidth of 150 kHz at a clock rate of 20 MHz. Three benchmark simulations were conducted using worst-case models to establish the performance of the ΔΣ oscillator. They are tone generation at 20 kHz (the upper edge of the audio band), 100 kHz (the cutoff frequency of the reconstruction filter), and 150 kHz (the bandedge of the oscillator). Simulations were performed on the netlist extracted from the layout and the output was post-processed using a cosine window and Fourier transform in Matlab. The test procedure involves loading the loop coefficient and both initial condition registers and collecting the output bit pattern. Since the ASIC is designed to reset the values of all other integrators, the output PDM bit pattern is deterministic as soon as the initial conditions are loaded. Table 3.2 shows the relevant input data and results obtained from simulation. For each simulation, there are two spectral plots: the output spectrum up to $f_s/2$ and a magnified plot showing the single tone at f_t, indicating the desired sine wave.

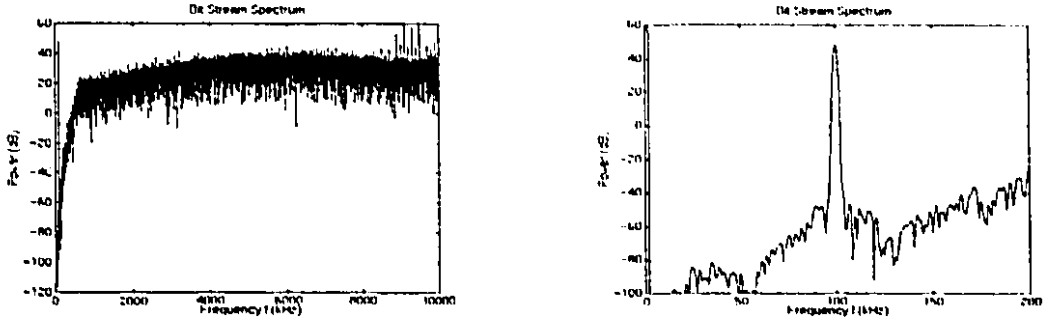
Functional bench testing of both ASICs did not pass. Tests indicated that the oscillator would go into an overflow condition soon after start-up. However, the results were not continuously reproducible i.e. they would vary from one execution to another of the same test. Tests were conducted at various clock rates ranging from 4 Hz to 20 MHz. Those that did pass verified the performance of two flip-flops, a multiplexer, and the enable signal.

Table 3.2 - Functional Simulation Results

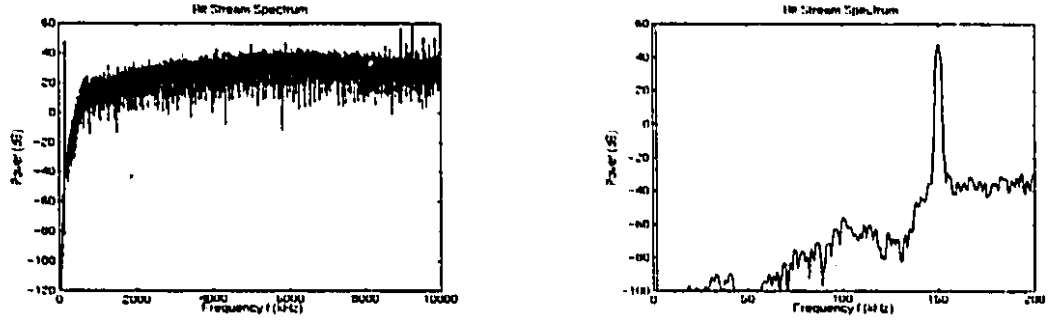
f_s (MHz)	f_t (kHz)	Figure	Dynamic Range (dB)
20	20	3.12(a)	110
20	100	3.12(b)	100
20	150	3.12(c)	90



(a) frequency spectrum for f_t = 20 kHz



(b) frequency spectrum for f_t = 100 kHz



(c) frequency spectrum for f_t = 150 kHz

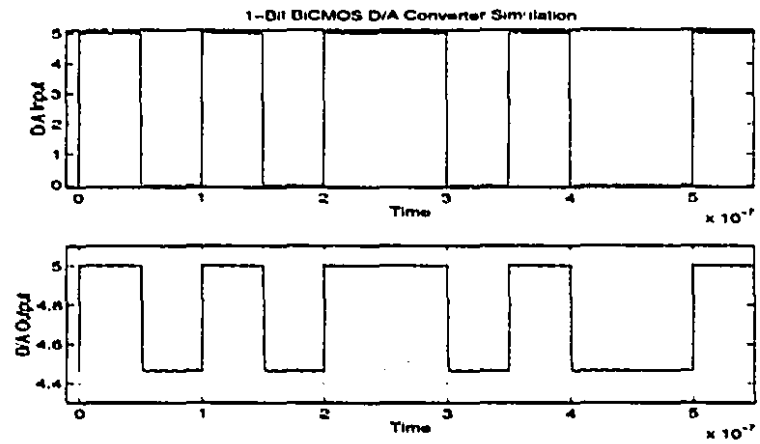
Fig. 3.12 - Fourth-Order Oscillator Simulation Results

One-bit Digital-to-Analog Converter

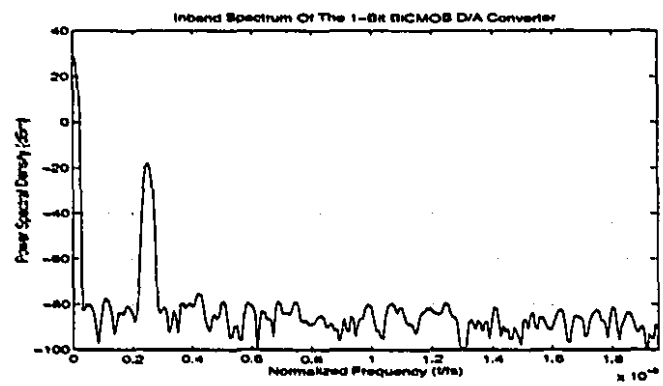
Simulations were run on the DAC to observe its output and measure its harmonic distortion. A sample of the DAC output at 20 MHz is shown in Fig. 3.13. This was conducted with a 50 ohm load designed to simulate the coaxial cable impedance used in the test environment. The linearity of the DAC was measured by inputting a 110 dB

(dynamic range) PDM-encoded sinewave from a fourth-order ΔΣ oscillator. The passband spectrum is given in Fig. 3.13. Its total harmonic distortion is -56.9 dB (0.14%). It is the opinion of the designer that the performance of the DAC can be improved by using a return-to-zero coding scheme, as shown in Fig. 3.2.

This component of IBAMGODF was tested by inputting a pattern through the auxiliary input of the ASIC that feeds the DAC directly. The DAC appeared to be functional in the sense that it output a PDM pulse train. However, its performance was significantly degraded. A comparison to the digital output of the chip (recall that the bit pattern fed into the DAC also appears on the digital output pin) is provided in Fig. 3.14, and indicates that the signal is better conditioned when output from the digital circuitry. As a result, the bench test of the DAC was declared a partial failure.

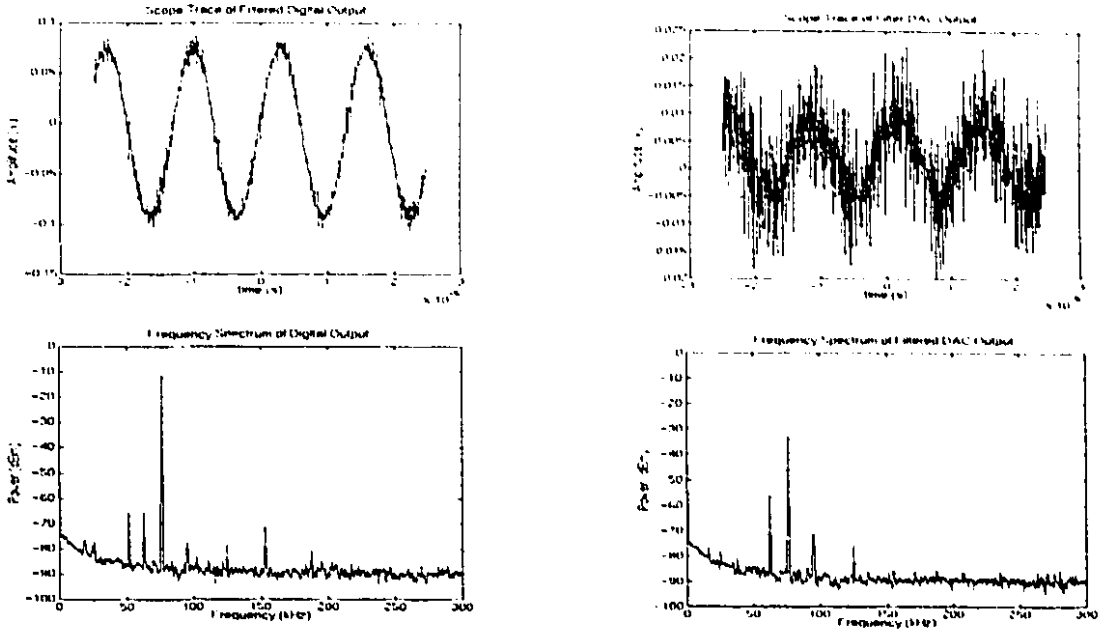


(a) DAC waveform simulation output



(b) DAC harmonic distortion spectrum

Fig. 3.13 - DAC Simulation Results



(a) filtered digital output

(b) filtered DAC output

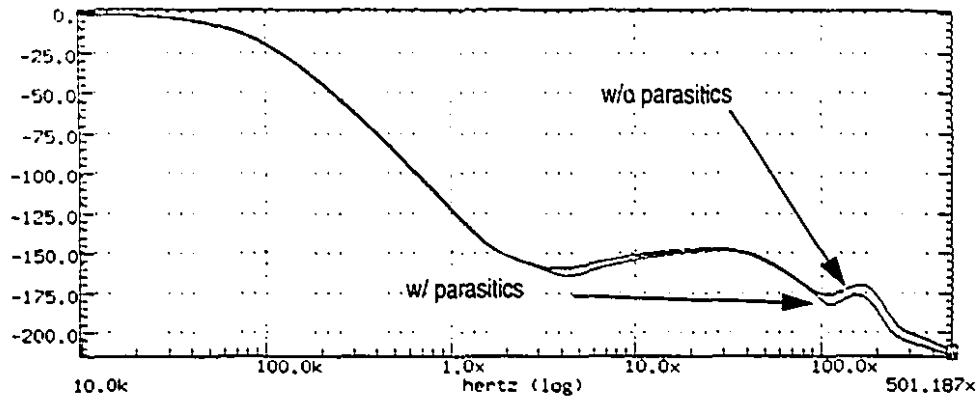
Fig. 3.14 - Comparison of Filtered DAC Output vs. Digital Output

Sixth-Order Reconstruction Filter

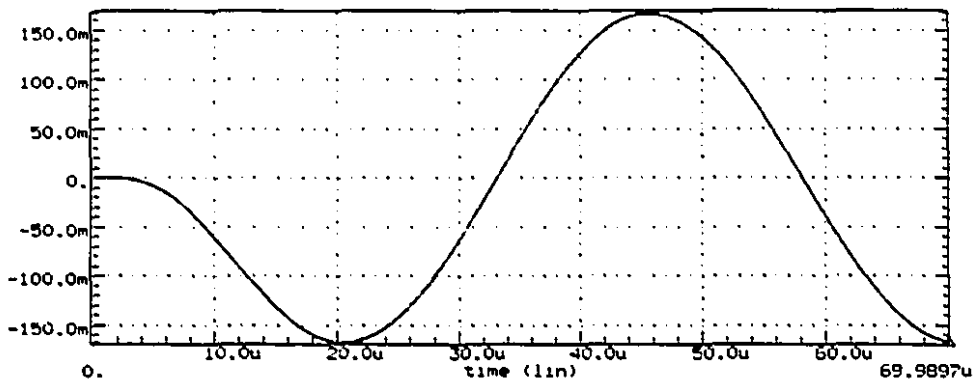
The filter was tested for its frequency response and its transient analysis. HSpice simulations were conducted on the layout: an AC sweep was run to achieve the frequency response shown in Fig. 3.15(a); a transient analysis was performed by inputting a 100 kHz PDM signal. The resulting plot is given in Fig. 3.15(b). Simulations were also conducted on the chip layout to verify the interconnect between the I/O pads and the filter.

The filter was bench-tested by inputting a sweeping-frequency sine wave to obtain its frequency response. It had no output, and drew 0.4 A from its negative power supply. Consequently, this test also failed.

Based on the culmination of these failure modes and a comprehensive study of the failures of all four components (two oscillators, the DAC, and filter), we drew the conclusion that both chips were not fabricated properly. The fact that this particular fabrication run had been redone to address low-yielding wafers also questions the reliability of the fabrication process.



(a) frequency response



(b) transient response

Fig. 3.15 - Frequency and Transient Response of the Reconstruction Filter

Nevertheless, the above simulation results give us a good indication of the best performance attainable with the oscillator and DAC/filter configurations. To summarize its main deficiencies, we note that both chips consume significant amounts of area -- too much if desired for a MADBIST application. They are also limited in their programmability to just single tone sinusoid signal generation over a fixed bandwidth. In the following chapter, we will examine in detail the results of our research: a new application for the $\Delta\Sigma$ modulator, which gives us complete programmability to create arbitrary waveforms at any frequency and can be integrated into existing digital hardware with little or no overhead. We achieve this area-efficient technique using forced-periodic PDM patterns.

Chapter 4 - Forced-Periodic PDM Patterns

The alternative to the oscillator method of on-chip PDM signal generation is the memory-based storage concept [5]. This approach is based on the principle that the aperiodic bit stream generated by a ΔΣ modulator can be truncated and forced to be periodic by cycling through the captured bits. In doing so, the bit pattern can be stored in traditional memory devices such as on-chip RAMs, ROMs, or even flip-flops, and written/read only when necessary i.e. when the analog device is under test.

4.1 - Periodic PDM Pattern

As described in *Chapter 2 - MADBIST and Analog Signal Encoding*, a ΔΣ modulator is based on an infinite-impulse response system whose output maps the input signal into an infinitely-long sequence of bits. As a result, the output bit pattern based on a periodic input, such as a sinusoid shown in Fig. 4.1(a), does not repeat itself [3]. That is, there is no

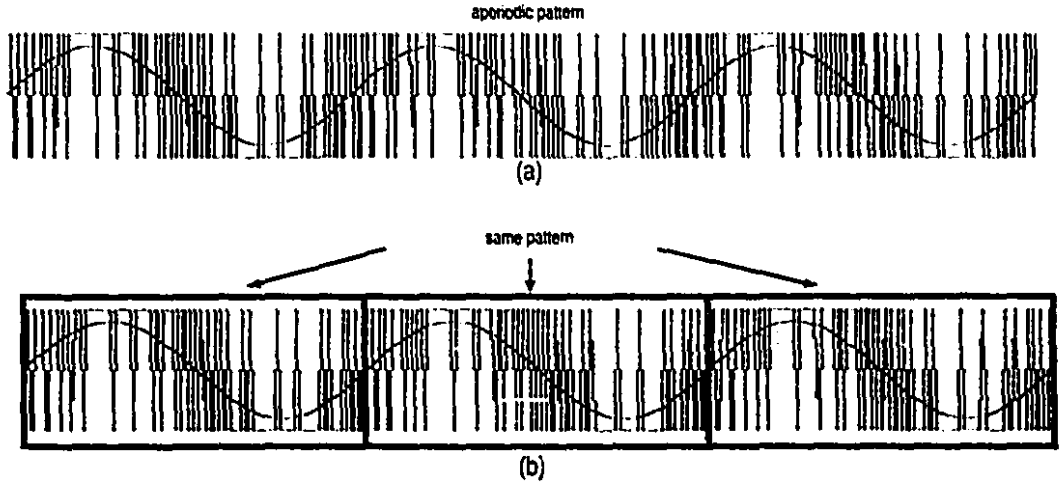
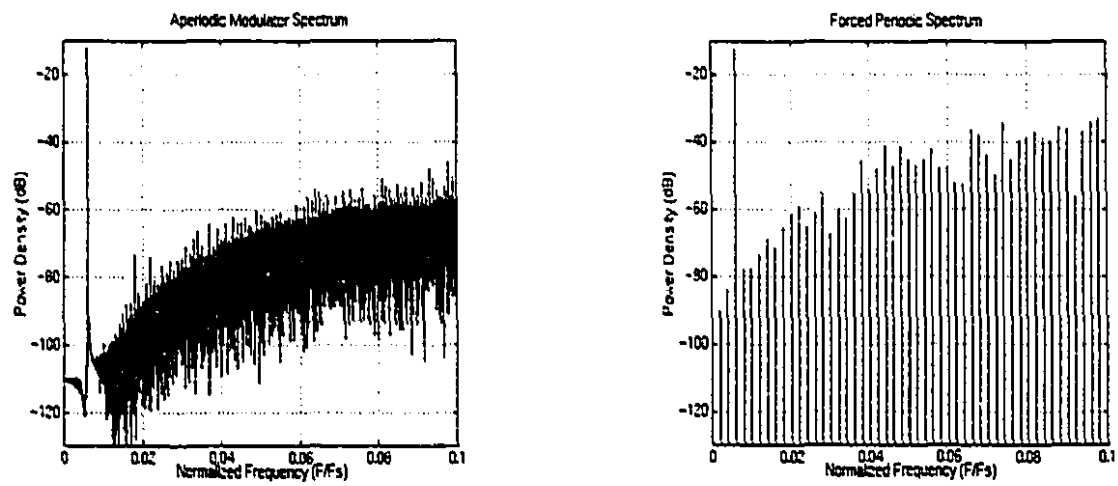


Fig. 4.1 - An Aperiodic Sine Wave and Its Periodic Approximation

one finite sequence of bits that can be extracted from the pattern which represents the input periodic signal. Nonetheless, we can come up with an approximation. By ensuring that the input signal completes an integer number of cycles within the PDM pattern, as in Fig. 4.1(b), the output bit pattern will closely approximate the original PDM signal. Though we have no formal proof to substantiate this claim, experimental results have demonstrated that this approximation is indeed a close representation of the original.

The following is an example of a PDM approximation made by truncating the waveform and forcing it to be periodic. The experiment is conducted in Matlab, using a fourth-order modulator to generate a tone at a normalized frequency of 0.00600, with a bandedge of 0.0078125. By performing a Fourier transform on over 300,000 points (using a rectangular windowing operation), the spectrum in Fig. 4.2(a) is obtained. We now take a 500-point sampling (500 points ensures we have an integer number of cycles in the bit pattern), and generate its spectrum by repeating the pattern 600 times for a comparable total of 300,000 points. Its spectrum is given in Fig. 4.2(b). Note that the aperiodic pattern has a dynamic range of approximately 90 dB versus 72 dB for the periodic pattern over the passband region. Further experiments using inband sinusoidal patterns generated by various modulator orders and oversampling ratios were conducted. Their results are summarized in Table 4.1. Again, over 300,000 points were collected for aperiodic pattern



(a) aperiodic frequency spectrum **(b) forced periodic frequency spectrum**

Fig. 4.2 - Spectra of Aperiodic and Forced Periodic PDM Pattern

to ensure a fair comparison. The periodic pattern was 1000 bits in length, repeated 300 times. Note that the periodic pattern shows a slight reduction in dynamic range for higher-order modulators. This is due to the relatively small bit length and the fact that an inband signal requires a longer pattern than a bandedge tone. Collecting a longer pattern would yield a greater dynamic range. The 90 dB plateau with the aperiodic pattern is caused by limitations in the data collection and processing method. The results, however, still indicate that the signal quality of the approximation obtained from a forced periodic PDM pattern is comparable to that from an infinite-length pattern.

The selection of the bit pattern is essentially arbitrary. That is, once the $\Delta\Sigma$ modulator has overcome its start-up transient condition, any sequential collection of bits, so long as there is an integer number of cycles within the bit pattern, will suffice. One measure, however, can yield a better approximations. That is, we must ensure that the $N+1th$ bit of the sequence from which the N bits are being extracted is the same as the first bit of the pattern. This will minimize the discontinuity between the end of the pattern and the start of its repetition. Fig. 4.3 illustrates the difference in dynamic range between a fourth-order, 1000-bit pattern that is matched by the $N+1th$ bit and one that is not matched. Measurements show an increase of approximately 15 dB (from 65 dB to 80 dB) of the matched pattern over the other.

Table 4.1 - Periodic vs. Aperiodic Dynamic Range Comparison[a]

Order - OSR	Dynamic Range	
	Aperiodic	Periodic
2 - 64	80	64
2 - 128	90	80
4 - 64	90	80
4 - 128	90	75
6 - 64	90	75
6 - 128	90	75

a. all tones are generated with an amplitude of 0.2, at a normalized frequency of 0.003.

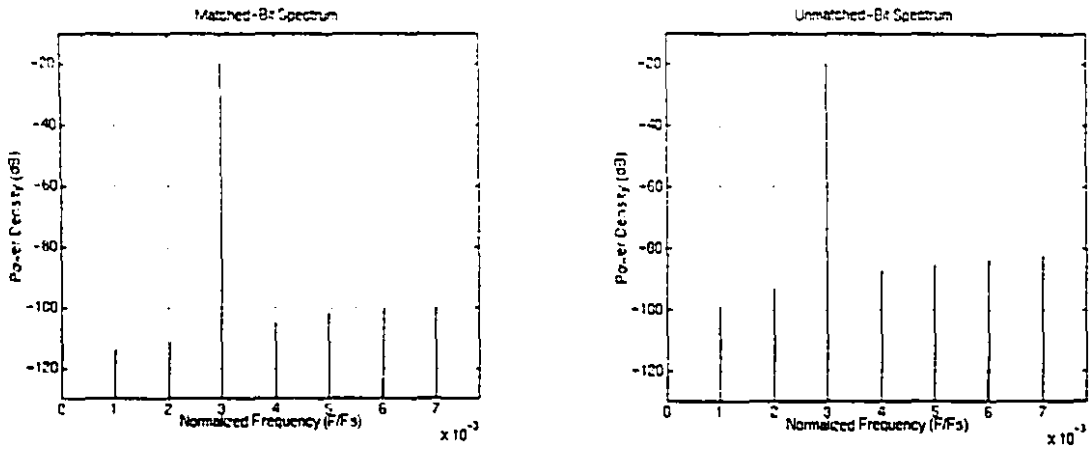


Fig. 4.3 - Comparison of Matched-Bit and Unmatched-Bit Pattern Spectra

As noted earlier, the pattern length of the periodic signal can change the quality of the generated signal. Indeed, there is a minimum number of bits required to reproduce the signal. This will be the focus of our next section.

4.2 - Determining Minimum Bit Pattern Length

In order to determine the minimum bit pattern length possible for signal encoding and reproduction, we must take into account the SNR and the desired signal attributes such as frequency and amplitude. Conversely, if we have a fixed number of memory elements (for example, a fixed scan chain of 500 flip-flops), we would like to know the available frequency resolution and the number of tones we can generate for a given SNR. We will develop the minimum pattern length in the context of generating perhaps the most common analog signal -- the single-tone sine wave.

To ensure that an integer number of cycles of the test signal is embedded in the PDM bit stream, the test frequency f_t should be chosen as a submultiple of the sampling frequency f_s according to the rules of coherent sampling [17], which is encapsulated by the expression:

$$f_t = \frac{M}{N} f_s \tag{4.1}$$

where M and N are integers. With $M=1, 2, 3$, etc., the test frequency f_t will be an integer multiple of the primitive frequency, f_s/N. In other words, the test frequency should consist of only those frequencies that are harmonically related to the primitive frequency. This also suggests that the primitive frequency limits the frequency resolution of the signal generation scheme. For a fixed sampling frequency, the resolution can only be improved by increasing the sequence length. Finally, to encode the test signal into a PDM stream, it is essential that the signal lies within the bandwidth of the ΔΣ modulator, i.e.,

$$f_t \le f_B. \tag{4.2}$$

According to our previous development for a second-order modulator in *Section 2.2.3 - PDM Signal Generation*, the SNR obtainable over this bandwidth with a signal of amplitude A embedded in a one-bit stream with a peak-to-peak pulse amplitude of Δ is given by Eqn. (2.4). So, for a desired SNR, the bandwidth f_B of the ΔΣ modulator can be expressed as

$$f_B = f_s \cdot 2^{-\frac{1}{15}\left(SNR + 23 - 6\log_2\left(\frac{A}{\Delta}\right)\right)}. \tag{4.3}$$

Substituting (4.1) and (4.3) into (4.2) gives us

$$\frac{M}{N} f_s \le f_s \cdot 2^{-\frac{1}{15}\left(SNR + 23 - 6\log_2\left(\frac{A}{\Delta}\right)\right)}, \tag{4.4}$$

or, with f_s eliminated, we obtain

$$\frac{M}{N} \le 2^{-\frac{1}{15}\left(SNR + 23 - 6\log_2\left(\frac{A}{\Delta}\right)\right)}. \tag{4.5}$$

Equation (4.5) provides the basic relationship between the sequence length N, the test tone frequency index M, the signal quality denoted by SNR over the modulator bandwidth of f_B, the amplitude of the encoded test signal A, and the modulator output level Δ.

As an example, consider an existing design that has a scan chain of 392 registers and runs at a frequency of 1.3 MHz. Let us assume that a signal with an amplitude of 0.7 V is to be generated using a ΔΣ modulator with an output of ±1.5 V (i.e., $\Delta = 3$ V). Then, according to (4.5), with $N = 392$,

$$M \leq 392 \cdot 2^{-\frac{1}{15}(SNR + 35.6)}.$$

Clearly, a trade-off exists between the number of available frequencies that can be generated and their signal quality. For instance, if an SNR of 65 dB is desired, then test frequencies corresponding to M less than 3.75 are possible. Thus, M can take on integer values between 1 and 3 and the corresponding test frequencies that can be generated using a 1.3 MHz clock are 3.32 kHz, 6.64 kHz, 9.96 kHz, as the primitive frequency is 1.3 MHz/392, or approximately 3.32 kHz. The experimental results for a 9.96 kHz tone based on this example are given in Fig. 4.4. The measured inband SNR is approximately 60 dB and agrees reasonably well to that predicted.

Normally, the cut-off frequency of the analog reconstruction filter is placed at the bandedge of the modulator f_B which, in this case, is 12.43 kHz. However, if we are generating only the above inband tones, the SNR can be maximized by placing the cut-off frequency of the filter at the highest tone i.e., 9.96 kHz.

By altering the PDM sequence length, other test frequencies can be generated. For instance, if 500 memory elements of the scan chain are used, then the primitive frequency becomes 2.6 kHz. Thus, using Eqn. (4.5), we find that M must be less than 4.79 to maintain an SNR of 65 dB, resulting in the following four test frequencies: 2.6 kHz, 5.2 kHz, 7.8 kHz, and 10.4 kHz. It is interesting to note that all of these signals can be simultaneously encoded into a single PDM pattern thereby forming a multi-tone signal.

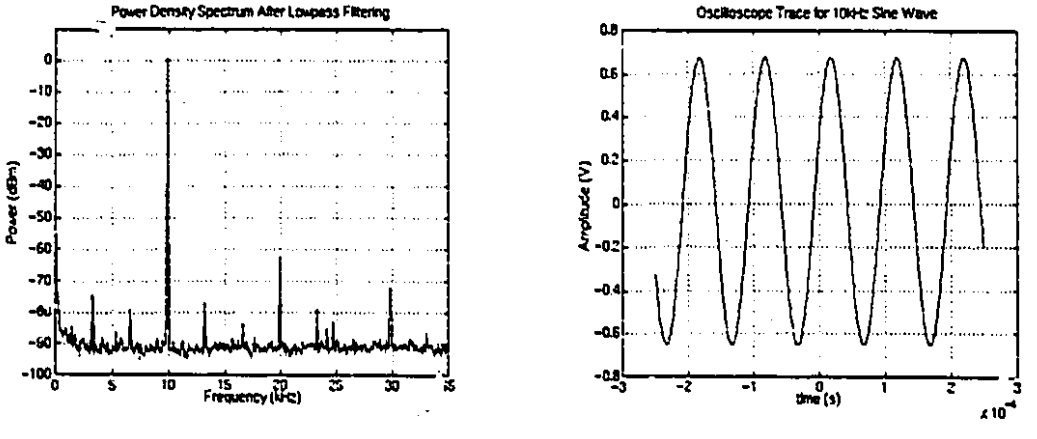


Fig. 4.4 - 392-Bit Sinusoidal Waveform

Such signals are essential for intermodulation distortion measurements. We will look further at multi-tone signals in *Section 4.4 - Arbitrary Waveform Generation.*

If we continue along these lines and further decrease the PDM sequence length in order to generate other test frequencies, we eventually come to a point where, for a given SNR, Eqn. (4.5) is no longer meaningful, i.e., M is constrained to be less than one. When M equals one, the PDM sequence has its minimum length. This is the situation where only one test frequency can be generated with the desired SNR. Thus, substituting $M = 1$ into Eqn. (4.5) leads to the expression for the minimum PDM sequence length, given by

$$N_{min} \leq 2^{\frac{1}{15}\left(SNR + 23 - 6\log_2\left(\frac{\Lambda}{\Delta}\right)\right)}. \qquad (4.6)$$

This is the optimum situation for the second-order modulation encoding process, as it uses the least number of storage elements to generate the desired test tone. It is possible, however, to reduce this minimum further if we make use of $\Delta\Sigma$ modulators of higher-orders in the encoding process. Interested readers can consult [18] for further details. For the same example given previously, the minimum sequence length required to generate a single test tone with an SNR of 65 dB is 105. The resulting test frequency is then 3.32 kHz.

Another option available to the test engineer is the creation of a test signal embedded in a bit stream that has been encoded by a bandpass $\Delta\Sigma$ modulator instead of a lowpass one. In doing so, higher test frequencies relative to the sampling frequency can be generated with an SNR identical to that achieved in the lowpass case. This, of course, assumes that a bandpass recovery filter is used with the appropriate bandwidth [12]. Equation (4.5) applies in exactly the same way, except that once M is determined, it must be added or subtracted from $N/4$ to compensate for the location of the band-centre of the bandpass $\Delta\Sigma$ modulator. The resulting test frequencies can then be located at either $(N/4 + M)f_s/N$ or $(N/4 - M)f_s/N$ on account of the symmetrical transfer characteristics of the bandpass modulator.

For example, using the previous scan chain consisting of 500 registers clocked at 1.3 MHz, it was found that test frequencies corresponding to M less than 4.79 could be

generated with an SNR of 65 dB. Thus, using a bandpass ΔΣ modulator with its bandpass region centered around $f_s/4$, test frequencies of

$$(500/4\pm4)\cdot 1.3MHz/500 = 314.6kHz, 335.4kHz$$
$$(500/4\pm3)\cdot 1.3MHz/500 = 317.2kHz, 332.8kHz$$
$$(500/4\pm2)\cdot 1.3MHz/500 = 319.8kHz, 330.2kHz$$
$$(500/4\pm1)\cdot 1.3MHz/500 = 322.4kHz, 327.6kHz$$

can be generated individually or collectively as a multi-tone signal. We will demonstrate bandpass signals in *Section 4.5 - High Frequency Tone Generation*

Note that if we wish to use the analog signal as a test tone, we may want to conform to the rules of coherent sampling for test signals in which we maximize the signal information by selecting the number of cycles of the embedded waveform, M, and the total number of points in the pattern, N, so that they share no common factors i.e. they are relatively prime.

We shall conclude this section by saying that the formulas presented here are approximate and are to be used as guide only. Experiments show that the SNR will usually be somewhat less than that predicted by the above theory.

4.3 - Finite Length Effects

Because the PDM stream is aperiodic, we must consider the ramifications of truncating the stream to a bit pattern holding an integer number of periods of the embedded signal and repeating this pattern to mimic the original stream.

4.3.1 - Periodic Noise

The ΔΣ modulator used to generate a PDM stream operates on the feedback of a one-bit signal and thus obviously contains an error component. Because of the aperiodicity of the PDM stream, the error term component is random in nature and can be characterized as white noise. Thus, we expect some random error to be present in every period of the embedded signal. In forcing the bit pattern to be periodic, however, the error term is no longer random, but is periodic with the signal. Since we do not have the advantage of long-term error cancellation or smoothing that was present in the original aperiodic bit

pattern, the error energy will be focussed at certain frequencies and will be periodic. That is, the error terms will appear as harmonics.

Now that we know the error is periodic, we can predict its location in the power density spectrum. Since the frequency resolution of a fixed-length pattern is determined by the primitive frequency, f_s/N, the harmonics that appear will be at integer multiples of this frequency. That is,

$$f_{\varepsilon_i} = k\frac{f_s}{N}, k = 1, 2, \ldots, k \leq \frac{N}{2}. \tag{4.7}$$

over the Nyquist interval. As N approaches infinity, we have the original infinitely-long PDM bit stream, with the error term spread over an infinite number of frequencies, thus the error is minimized. Conversely, as N gets smaller, the errors are concentrated at fewer frequencies. Recall the finite pattern still exhibits the noise-shaping characteristic of an infinite-length PDM stream; it just now manifests itself in harmonics at every frequency multiple of f_s/N. This can be observed in the following examples.

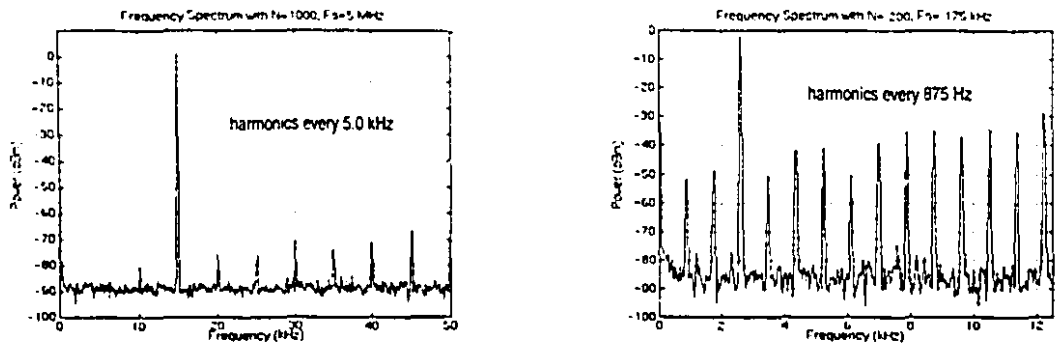
Consider a midband 15 kHz signal generated with 1000 bits, with a sampling frequency of 5 MHz. According to (4.7), we expect to see harmonics at every multiple of

$$\frac{f_s}{N} = \frac{5MHz}{1000} = 5.0kHz.$$

The non-filtered spectrum in Fig. 4.5(a) confirms this assertion, with a harmonic at every multiple of 5 kHz, (although the 5 kHz harmonic is barely perceptible in the lower passband). Another example is given in Fig. 4.5(b). This time, we used a sampling frequency of 175 kHz and a 200-bit pattern. As expected, we have harmonics located every

$$\frac{f_s}{N} = \frac{175kHz}{200} = 875Hz.$$

Therefore, the concentration of error manifests itself in harmonics at predictable frequencies. Because we know the location of the unwanted harmonics, we might want to reduce them, thus improving the quality of our desired signal. This topic is addressed in the following section.



(a) harmonics at every f_S/N = 5.0 kHz (b) harmonics at every f_S/N = 875 Hz

Fig. 4.5 - Frequency Spectra Illustrating Harmonic Placement

4.3.2 - Error Detection and Correction

Now that the result of errors generated by finite-length approximation have been discovered, we can now examine their source and explore methods of correction.

As explained in the previous section, the truncation effect introduces error signals that are harmonically related to the sampling frequency and the number of bits rather than part of a white noise spectrum. The energy in each error harmonic is a combination of previous inband white noise concentration and the addition of some small out-of-band noise. Since the PDM stream is considered to be of infinite length, we can arbitrarily extract a bit pattern to represent the embedded signal and expect to find differences (in the sequence of ±1s) between the patterns. If we, however, extract sequential patterns i.e. one pattern after the next, we expect to see only a few differences in the bit pattern (on the order of 4 to 20 bits in a pattern length of 128 from a second-order modulator). We consider these bits to be a portion of the error signal.

Ideally, we would like to move the power of the unwanted harmonics outside of the passband. If we were to focus on manipulating the pattern by actively flipping the bits we believe are part of the error signal, we can change the noise content in the bit pattern to hopefully create a smoothing effect on the noise, thus minimizing the noise in the passband and improving signal quality. This process is known as "dithering". While it will not be explored in this thesis, the periodic PDM pattern work presented here may benefit

from dithering algorithms that could distribute harmonic noise throughout the passband or, if possible, force it outside the band, as the original noise-shaping process does. Dithering is hardly a new process of distributing power by manipulating bits. However, most applications take a random approach to the process, injecting a pseudo-random signal (such as that generated with a linear feedback shift register) in an attempt to break up idle tones in the quantization noise floor [19]. It is reasonable to assume that the application of this research to finite-length patterns will also improve signal quality.

One alternative for improving the signal quality of a bit pattern is to create a return-to-zero (RZ) bit sequence from the non-return-to-zero (NRZ) pattern, as discussed in *Section 3.1 - The Dedicated Test System*. There are two simple ways to achieve this. Assuming the data stream consists of a bipolar pattern such as ±1, an RZ pattern can be created by simply inserting a zero in between each bit. The disadvantage to this, however, is that it effectively cuts the sampling frequency in half, thereby lowering the frequency of the embedded tone, doubling the bit pattern length, and halving the signal power. Another approach is to logic-AND the output data pattern with the sampling clock, as shown in Fig. 4.6. In doing so, the data pattern is forced back to a logic-0 half-way through the clock period. If necessary, the clock can be buffered in order to delay its arrival at the gate and prevent a transition on the data signal while the clock is high. Note that any potential variance in the duty cycle of the clock or rise and fall times of the AND gate do not affect the PDM signal quality since our only requirement is that the PDM pulses be of equal area. The only foreseeable disadvantage is, like the previous method, a reduction of the signal power by one-half.

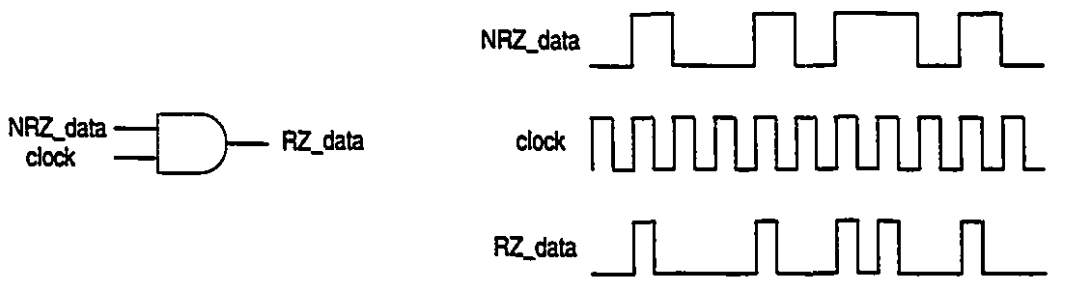


Fig. 4.6 - A Simple NRZ-to-RZ Coding Circuit

Though we have provided a few ideas for minimizing the error found in finite-length PDM sequences, we are only fond of those that are simple in their implementation, for the power of PDM encoding lies in the ability to encode and reconstruct arbitrary waveforms easily. We will demonstrate this characteristic in the follow section with several examples of the finite-length PDM encoding of arbitrary signals.

4.4 - Arbitrary Waveform Generation

Up until now, we have shown only single-tone sinusoidal signals using the forced-periodic PDM technique. This is by no means a limitation with a truncated PDM pattern. Previously, in *Section 2.2.3 - PDM Signal Generation*, we described how $\Delta\Sigma$ modulators could be used to digitally-encode virtually any bandlimited analog waveform. In this section, we will demonstrate the ability of the truncated bit pattern to reproduce multi-tone waveforms such as a two-tone sinusoidal and sawtooth pattern.

4.4.1 - Multi-tone Encoding

With the exception of the single-tone sinusoid, all waveforms are multi-tone signals with their power concentrated at selected frequencies to generate the desired pattern. When considering multi-tone signals in the context of sampled-data systems, the number of tones that can be generated in a given bandwidth are limited. The frequency resolution (the number of possible tones) over a band of interest is given by:

$$\Delta f = \frac{f_s}{N}. \tag{4.8}$$

Recall that the oversampling ratio is related to the sampling frequency and the cutoff frequency of the modulator by:

$$OSR = \frac{f_s/2}{f_B}. \tag{4.9}$$

By rearranging (4.9), we can describe the bandwidth as

$$BW = f_B = \frac{f_s}{2 \cdot OSR}. \tag{4.10}$$

Combining (4.8) and (4.10), we can determine the total number of tones that can be encoded within the bandwidth, i.e.

$$n_{tones} = \frac{BW}{\Delta f} = \frac{N}{2 \cdot OSR}. \tag{4.11}$$

Thus, the maximum number of tones are limited to the number of bits we collect, N, and the oversampling ratio. Let us now consider two examples of multi-tone signals.

4.4.2 - Two-tone Sinusoid

The two-tone sinusoid is used frequently in characterizing the intermodulation distortion generated by an analog circuit. We can generate its PDM pattern by summing two sinusoids prior to inputting them into a $\Delta\Sigma$ modulator, as previously shown in Fig. 2.14(b). In selecting the bit pattern length, we must now ensure that both sinusoids complete an integer number of cycles within the bit pattern. That is, the number of cycles of each waveform in the PDM pattern, M_1 and M_2, are integers.

Consider the following example. We wish to generate two tones, one around 3 kHz and the other near 5 kHz. Using a second-order modulator, we can generate the tones with 1024 points. If we let $M_1=3$ and $M_2=5$, and a sampling frequency of 1 MHz, we generate the following frequencies:

$$f_{t1} = \frac{M_1}{N} f_s = \frac{3}{1024} 1MHz = 2.93kHz$$

$$f_{t2} = \frac{M_2}{N} f_s = \frac{5}{1024} 1MHz = 4.88kHz.$$

The pattern is passed through a lowpass filter set to the bandedge, 7.8 kHz. The resulting spectrum and scope trace of the 1024-bit pattern are given in Fig. 4.7. The above procedure can be extended to include as many tones as required.

4.4.3 - Sawtooth Waveform

The sawtooth waveform serves as a good example of the versatility of $\Delta\Sigma$ modulator encoding and the power of the finite-length bit pattern approximation. We must realize,

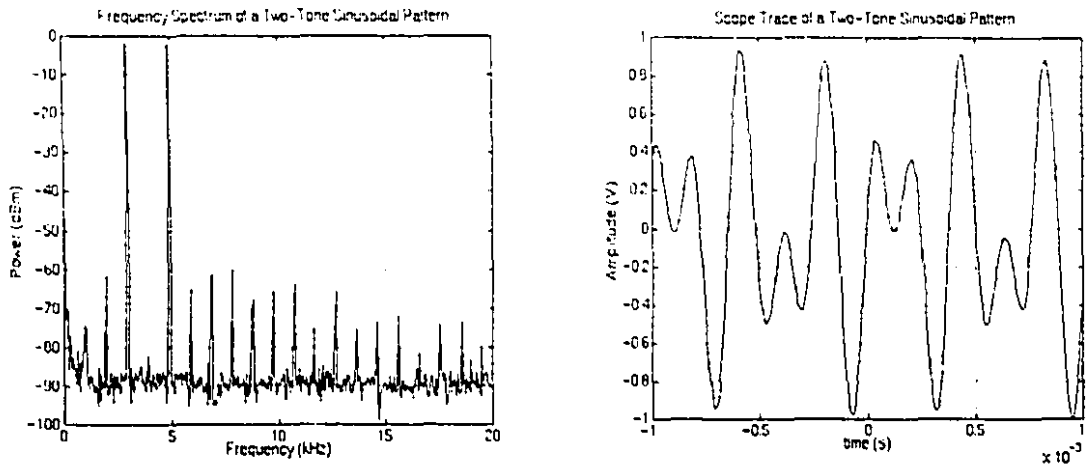


Fig. 4.7 - Two-Tone Sinusoidal Waveform Extracted From 1024 Bits

though, that we are limited by the fact that the bandwidth of the modulator can only encode a fixed number of tones of a specified resolution, while a sawtooth pattern contains an infinite sequence of harmonically-related tones. Keeping this in mind, we can still create the sawtooth waveform, and one such example follows. Here we have a pattern length of 8192 bits containing three cycles of the waveform. Clocking the bits at a sampling frequency of 2 MHz, we get a waveform with a sawtooth frequency of approximately 732 Hz. The frequency spectrum and scope trace are illustrated in Fig. 4.8. Note the clarity of each individual tone in the spectrum and the sharpness of the transitional edges in the time domain, indicative of a high-quality pattern. Disregarding the voltage spikes present at the discontinuities of the waveform, the maximum voltage magnitude of the waveform appears constant. The spikes are likely a result of the Gibbs' phenomenon where a truncated Fourier series is used to approximate a discontinuity. It may be possible to reduce the level of these spikes by altering the shape of the original signal that is encoded in the bit pattern.

4.5 - High Frequency Tone Generation

Up to this point, we have focussed on generating waveforms that were encoded with a lowpass $\Delta\Sigma$ modulator. This, however, restricts the maximum frequency of the tone we can generate. As pointed out earlier, we can use other shaping modulators, such as

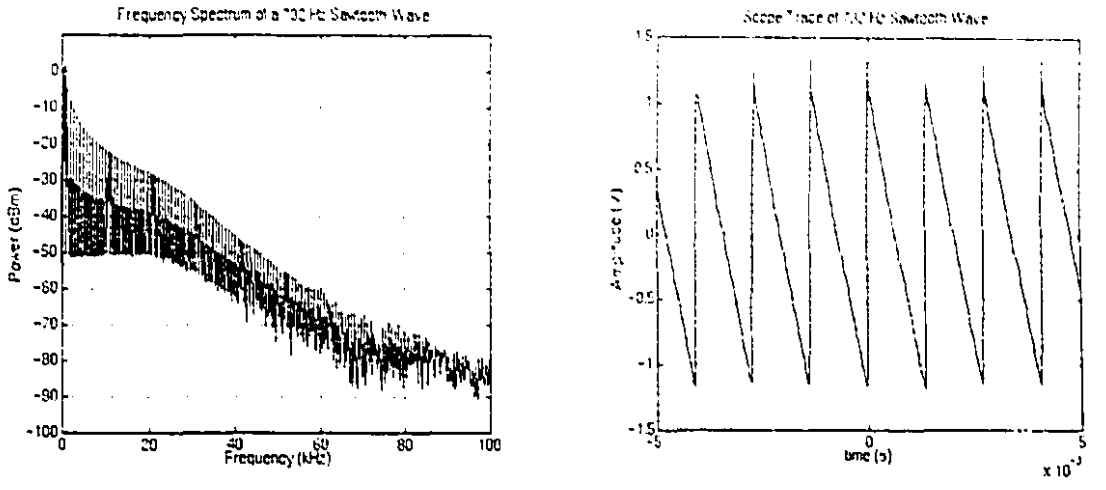


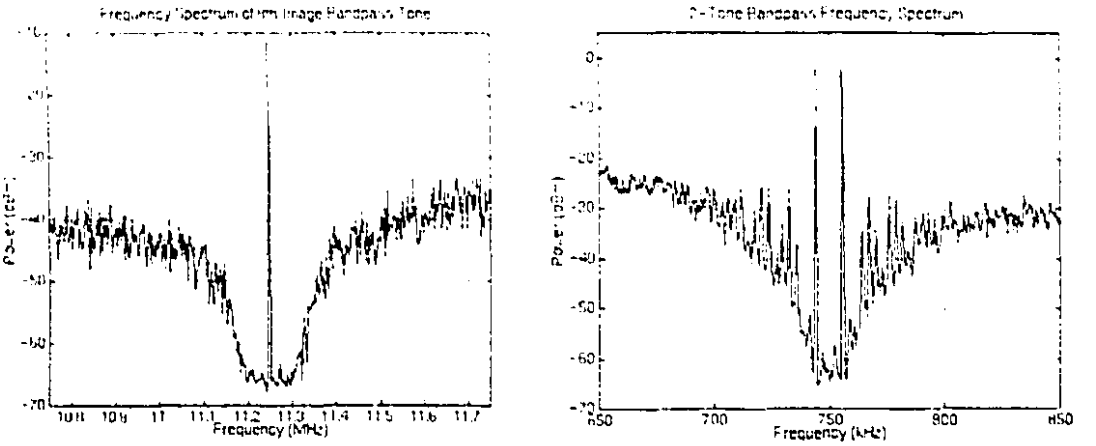
Fig. 4.8 - 732 Hz Sawtooth Waveform

bandpass or even highpass designs to focus on different frequency regions. Perhaps the most beneficial coding scheme for higher-frequency systems such as wireless communication systems (which are inherently bandpass), is the bandpass modulator. With it, we can make use of the sampled-data images to extract high-frequency signals [20]. The following example highlights this.

With an 8th-order bandpass modulator generating a pattern with an *M/N* ratio of 2047/8192, this generates a fundamental tone at 1.249 MHz when sampled at 5 MHz. By taking the 8th image as shown in Fig. 4.9(a), we can create a tone at 11.24 MHz with a dynamic range of approximately 55 dB.

We can also combine bandpass modulation and multi-tone signals to supply high-frequency multi-tone patterns as shown in Fig. 4.9(b). Here, we have taken an image at 3/4 of the sampling frequency, resulting in tones at approximately 744.0 kHz and 755.8 kHz. A pattern length of 32,768 bits gave us approximately 60 dB of dynamic range.

Now that we have established the viability of using a forced-periodic PDM pattern to generate test signals, we can take advantage of all the noise-shaping benefits of modulator-based waveforms. We will now revisit our pattern-based generation circuitry, as shown in Fig. 2.5, to form a simple yet elegant and easy-to-implement test pattern generator. We



(a) higher-image tone spectrum (b) multi-tone bandpass spectrum

Fig. 4.9 - Frequency Spectrum of a 8th Image Bandpass Tone

term the combination of pattern storage and retrieval and periodic PDM patterns the "memory-based storage" technique. In the following chapter, we will highlight some of its many advantages that it has over the oscillator-based method of analog signal generation. In addition, we will demonstrate how it can easily be integrated into today's digital test structures.

Chapter 5 - Memory-Based Storage

The alternative to the oscillator method of on-chip PDM signal generation is the memory-based storage concept [5]. Such an approach utilizes the principle that the aperiodic bit stream generated by a $\Delta\Sigma$ modulator can be truncated and forced to be periodic by cycling through the captured bits. In doing so, the bit pattern can be stored in traditional memory devices such as on-chip RAMs, ROMs, or even flip-flops, and written/read only when necessary i.e. when the analog device is in test mode. The end result is a high-quality analog signal generator with virtually no hardware overhead since existing logic is used for bit storage and retrieval. While this technique is applicable to any finite-bit pattern signal generator such as those described in *Section 2.2 - Digital Encoding of Analog Signals*, we will concentrate only on the application of memory-based storage with finite-length PDM patterns, as we feel this is the most versatile method of encoding analog signals.

5.1 - Advantages of Memory-Based Storage

Many advantages exist over the on-chip method of signal generation highlighted in *Chapter 3 - Applications of the Delta-Sigma Oscillator*. Some of the more relevant ones will be closely examined below.

Area overhead associated with PDM bit pattern generation is reduced.

Since the creation of the PDM stream occurs off-chip and prior to stimulating the circuit, the costs associated with oscillator design, such as logic complexity and layout effort, are eliminated completely. Thus we can completely do away with the high area usage and design effort as required for the fabricated ASICs detailed in *Section 3.3 - Delta-Sigma Oscillator ASICs*.

Existing on-chip circuitry can be used for storing and retrieving the bit pattern.

The main component requirements are either a RAM, ROM, or a sufficiently long chain of sequential circuitry, such as in Fig. 2.5. Since a RAM is common in most digital ICs, little additional overhead is required. Address generation and sequencing circuitry can usually be found where RAM built-in self-test (RAMBIST) circuitry is used. Also, because the addressing requirements are simply a loop-around counter, the addition of logic is minimal should it not already be available.

Should the delay of loading the bit pattern into the RAM be intolerable, a dedicated ROM can be used to store one or multiple test patterns. Alternatively, flip-flops, prevalent in the majority of digital designs, can be configured to form a long serial chain into which the data pattern can be loaded. Note that this configuration adds little overhead, as serial chain configurations are used with the 1149.1-1990 IEEE Standard in digital test environments.

Sophisticated signals (including multi-tone) can be generated.

Because this method only requires the bit pattern to recreate the signals, greater emphasis can be placed on generating the pattern beforehand using normal DSP or non-real-time computing power. The method allows the test engineer to create various waveforms outside of the usual single-tone sinewave, such as triangular or sawtooth, or conceivably any multi-tone signal that can be reproduced within a finite bandwidth.

A test library can be generated beforehand.

Since the test patterns will be generated most likely in software utilizing signal processing techniques, a suite of tests can be created and maintained on typical mass storage devices such as magnetic or optical media. When tests are to be conducted on a device, a selection of the relevant tests can be downloaded to the appropriate on-board memory element, whether it be a RAM, ROM, or even processor memory for subsequent relocation elsewhere (such as in the case of loading an embedded RAM or scan chain). Note that, given sufficient on-chip memory, several tests could be loaded in one batch operation.

The versatility of finite-pattern signal generation is even more apparent when we consider the ease with which it can be integrated into various digital and digital test architectures. We will now examine some of the different hardware configurations possible for integration of the forced-periodic PDM analog signal generator.

5.2 - RAM-Based Signal Generation

In integrating the memory-based signal generation technique into existing digital structures, we naturally require memory elements. One of the more common mass-storage memory elements located on a digital or mixed-signal chip or on a circuit board is a random-access memory, or RAM. Although the application works equally as well in an embedded RAM or a separate, off-chip dedicated RAM, we will focus on the embedded RAM structure, as it is conducive to the MADBIST scheme. The idea is simple: the finite-length PDM pattern is loaded into memory and is sequentially read out when activated.

The RAM-based method also has several advantages. First, the use of a RAM allows us to store bit patterns of varying length, giving us greater versatility in the number or type of signals generated. Also, since most RAMs, even of the smallest size, are capable of holding several thousand bits, a very large bit pattern (necessary for complex or very high quality waveforms) or even multiple patterns can be stored. The ability of storing multiple patterns in memory at one time addresses one of the criticisms of the memory storage pattern method. That is, the long time required to load a new pattern between tests is eliminated as the new pattern is sequenced immediately when the address controller is set to a different memory space. Finally, since data is often stored in RAMs in multi-bit lengths known as "words", and we output the PDM pattern sequentially, we could undergo a significant sampling rate increase through the parallel-to-serial conversion. As a simple example, consider a RAM with a 16-bit word that can be accessed within one period of a 75 MHz master clock. Provided we have supporting parallel-to-serial and high-speed sequential-output hardware, we could conceivably output the serial bit stream at a rate of 16 x 75 MHz, or 1.2 Gbps.

We will address two basic types of embedded RAM configurations. The first is where the RAM can be accessed directly through a processor interface (processor-accessible RAM). The other situation is where no on-chip processor interface exists, or where the processor cannot access the embedded memory (hardware-accessible RAM).

5.2.1 - Processor-Accessible RAM

A typical application of a processor-accessible RAM is shown in Fig. 5.1. In this case, an off-chip processor or test hardware is used to access the RAM via a processor interface (which has read/write control of the RAM). Notification is given to the processor interface block that a PDM pattern is being loaded. This invokes a RAM address generator that supplies the RAM with a memory address along with the data word to be written. The operation is repeated until the entire bit pattern is loaded into memory.

When the user is ready to generate the PDM pattern, a command is given to the processor interface to invoke PDM output mode. Provided the processor interface is sufficiently fast, the processor or test hardware can also control read operations of the RAM. Otherwise, a faster operation, such as an on-chip address counter, may be used to improve the output data rate. Note that in Fig. 5.1, the inclusion of an optional high-speed interface is

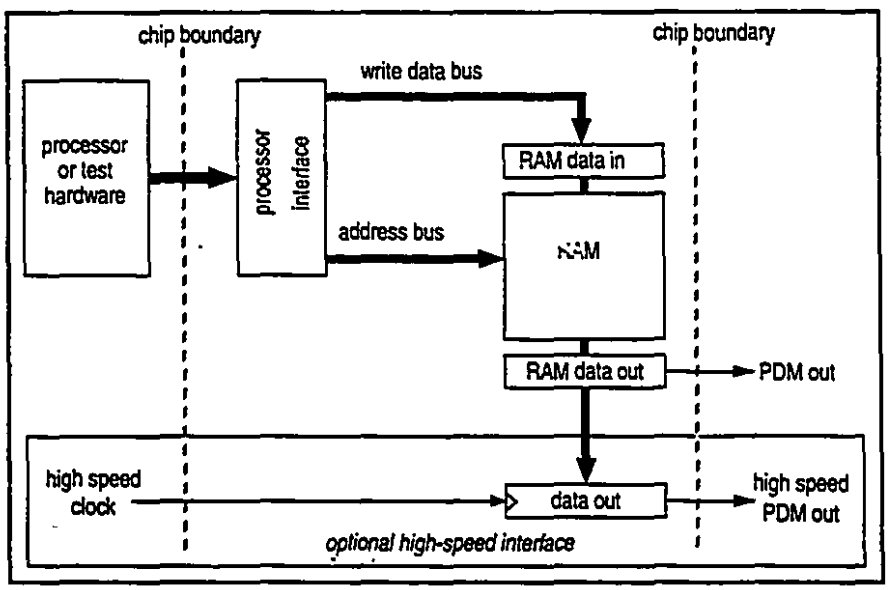


Fig. 5.1 - Finite-Length PDM Controller Utilizing a Processor Interface

specified. This refers to the potential data rate increase that the PDM pattern can experience when undergoing a parallel-to-serial conversion. The chip would require a high-speed clock and circuitry to output the data as fast as the product of the RAM access rate and the bit word length.

5.2.2 - Hardware-Accessible RAM

In certain applications, the RAM is not accessible by a processor interface, or an interface may not even exist, such as in Fig. 5.2. Here, we can make use of existing hardware that is fast becoming standard on digital integrated circuits, namely the JTAG controller (as per IEEE Standard 1149.1-1990) and the RAM Built-In-Self-Test (RAMBIST) controller. The 1149.1-1990 IEEE Standard allows the addition of user-defined registers and instructions [21, 22]. By designing the appropriate instructions and necessary logic into the JTAG controller, we can use the TDI input to serially load the PDM pattern into the RAM. While it is acknowledged that serial loading can be time-consuming, it is loaded at most only once for each test conducted. However, if multiple patterns are read in at the same time and stored for later usage, the time overhead associated with loading the pattern becomes negligible. While RAM address generation could be controlled by a dedicated PDM controller, we could also make use of what often resides on chips with embedded memory

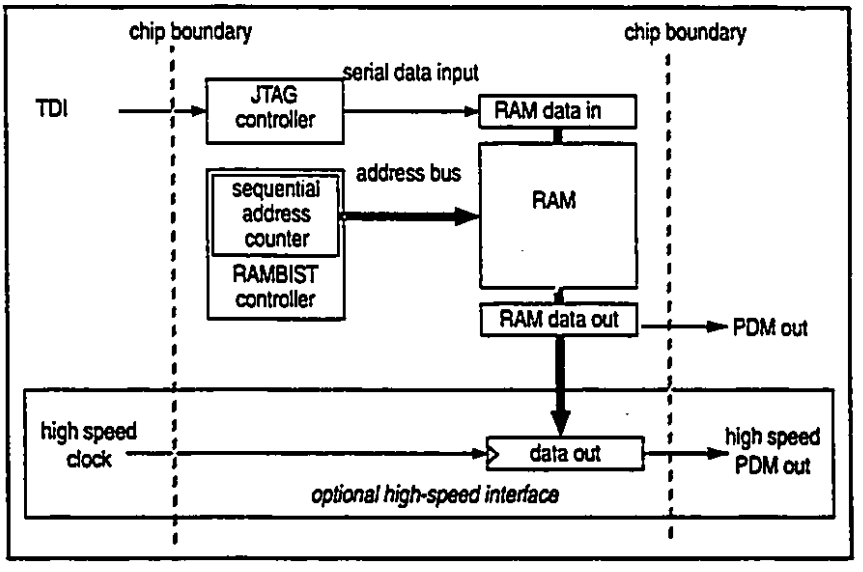


Fig. 5.2 - Finite-Length PDM Controller Utilizing Existing On-Chip Test Logic

-- RAMBIST controllers. Many of the current RAMBIST controllers use a sequential memory address counter for automated address generation during the testing of an embedded RAM. We can use this counter to generate the read and/or write addresses for pattern loading or output sequencing. This assumes, of course, that sequential addressing is used for PDM pattern storage which, while minimizing hardware complexity, is not a requirement.

Once the pattern is downloaded into memory, the user can initiate PDM sequencing by issuing a command to the JTAG controller. This command would simply engage the circulating address counter, place the RAM into read mode, and serially shift the data words out of the IC. Again, the opportunity exists for an increase in output data rate due to the parallel-to-serial conversion.

A more detailed example of an application with the relevant pin-out is shown in Fig. 5.3. In this case, we are using the RAMBIST address counter to cycle the address bus and the

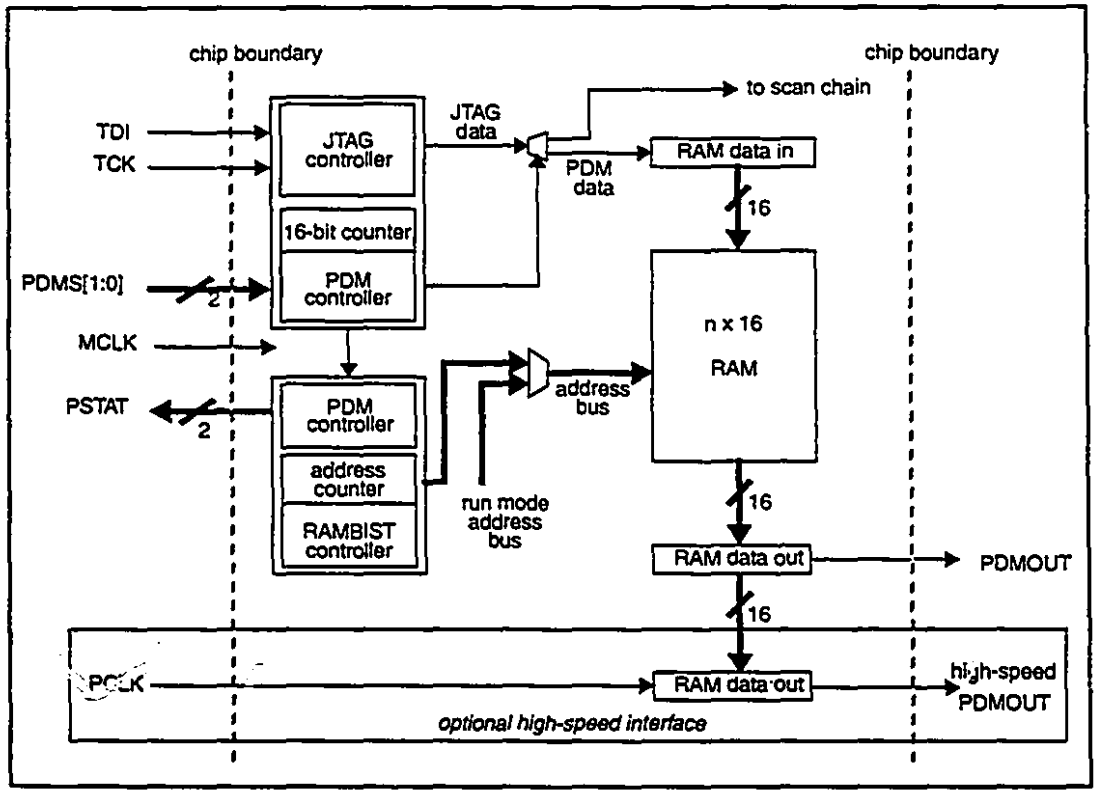


Fig. 5.3 - PDM Controller Utilizing JTAG and RAMBIST Controllers

TDI signal of the JTAG controller to input the data stream[1]. The operation of the address counter is to simply roll-over on read operations (to cause continuous sequential reading of the data pattern) and to lock on write operations to indicate the RAM is loaded. For the present example, we have assumed the RAM word size is 16 bits. The setup of Fig. 5.3 requires the following pins:

- MCLK (input): the system clock;
- TCK (input): the JTAG controller clock;
- PCLK (input): PDM serial stream output clock, if different from MCLK or TCK (if hardware speed permits, the preferred rate would be PCLK = MCLK × RAM word size. This would be the maximum rate at which we could run the above circuit);
- PDMS (input): PDM mode select;
- PSTAT (output): PDM status indicator.

The pin mapping for PDMS and PSTAT is given in Table 5.1. The above situation assumes that the pattern length is fixed and that only one pattern is loaded at a time. If we wish to allow variable lengths with multiple patterns, then additional logic would be necessary to control the address counter start and stop points. Note that since the hardware required for the above setup is not much more than controller logic, the hardware overhead is minimal.

Table 5.1 - PDMS and PSTAT Pin Mapping

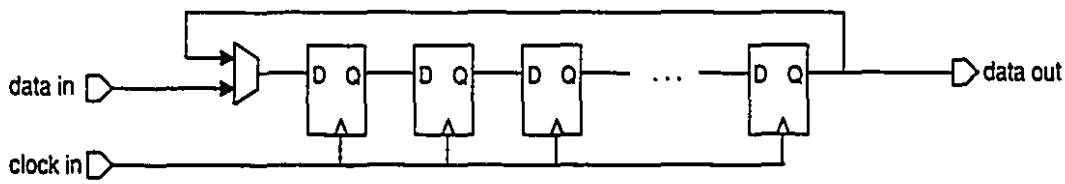
PDMS[1:0]	Action	PSTAT[1:0]	Action
C0	PDM Off	00	PDM off
01	PDM Write	01	PDM loading
10	PDM Read	10	PDM reading
11	not used	11	RAM loaded

1. Though not indicated in Fig. 5.3, should there exist an auxiliary scan-dedicated pin bus, the RAM could be loaded in a parallel manner. This would greatly decrease the amount of time required to load the RAM and may also reduce the required PDM controller logic.

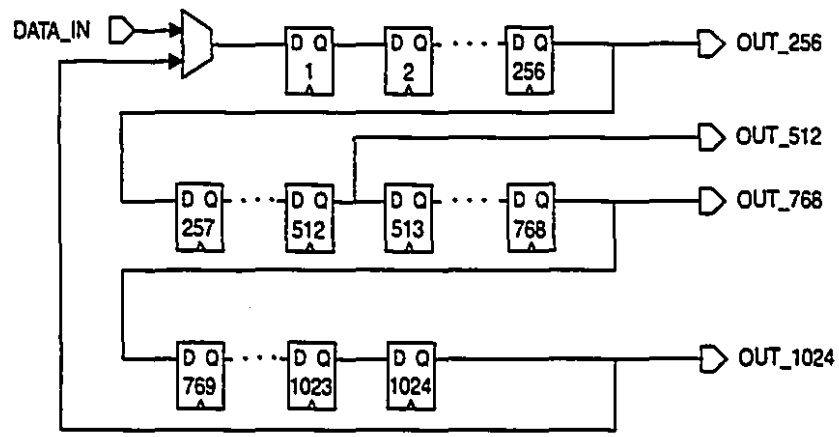
5.3 - Flop-Based Signal Generation

One of the more common memory elements located on a digital or mixed-signal chip is the flip-flop. And growing in popularity is the scan chain, used for BIST and in applications of the 1149.1-1990 Standard. Fortunately, we can make use of these scan chains as a simple built-in PDM pattern storage device. The premise behind their usage is that the flip-flops of an IC are configured in a serial chain with a multiplexer which feeds around the output back to the input. A PDM pattern is injected into the chain and, when shifting is invoked, the output is the encoded signal. A typical scan chain configured for sequencing a PDM pattern is shown in Fig. 5.4(a).

Certain advantages of the scan-based application exist over the oscillator or RAM-based storage technique. For example, varying phases of the output signal can be created simply by tapping off the appropriate flip-flop in the chain. In the context of quadrature signals for instance, waveforms that are 90 degrees out of phase with each other are required. This is accomplished by taking the output of every quarter of the chain, as shown in Fig. 5.4(b). If



(a) typical scan chain configured for PDM pattern sequencing



(b) scan chain tapping for multi-phase signal generation

Fig. 5.4 - Scan Chain Configurations

the total chain length is 1024, then by driving outputs with the 256th, 512th, 768th, and 1024th flip-flops, we have four identical signals, each 90 degrees out of phase with the next. Figure 5.5 shows the four sinusoids and the appropriate phase differences, created with a 1024-bit pattern. By tapping off selected flip-flops, arbitrary phase angles (within the resolution factor dictated by scan chain length, *360°/N*) can be obtained. The scan chain can also be run at data rates much faster than the typical oscillator design, as the only combinational logic in the register chain is a two-input multiplexer in the feedback path that is situated in front of the first flip-flop.

There are basically two types of scan-based applications which we want to highlight. The first makes use of a test scan chain configuration, while the other is a dedicated scan chain created specifically to output PDM patterns at very high rates of speed.

5.3.1 - Scan Chain Sequencing

Certain test configurations common on digital and mixed-signal ICs provide an ideal resource for fixed-length PDM signal generation. Such include internal scan and boundary scan. Internal scan chains test logic between memory elements by configuring a serial connection of all flip-flops in the core-logic of the IC. Depending on the flop count of the IC, multiple chains may be used. Boundary scan, on the other hand, is used for the testing

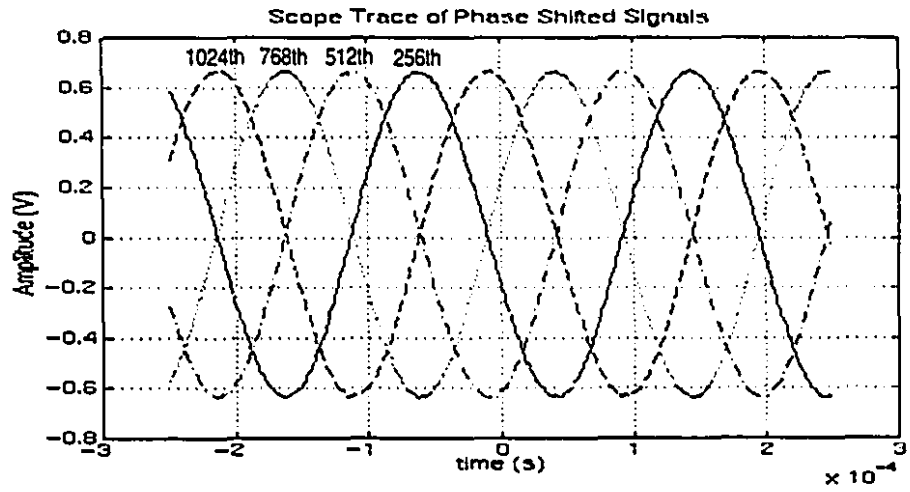


Fig. 5.5 - Phase-Shifted Signals Created By Tapping The PDM Chain

of pad-to-pin bonding wires within the IC, and external wire traces between ICs. Here, the memory elements are close to the pads on the die. These tests are generally controlled through the JTAG controller, in compliance with the 1149.1-1990 IEEE Standard.

The availability of several chains of memory elements allow for various PDM pattern chain lengths by simply connecting as many chains in series as required. All loading and configuration commands can also be controlled with user-defined instructions and/or registers in the JTAG controller. One such configuration is shown in Fig. 5.6. In this instance, a boundary scan chain and an internal scan chain are concatenated to provide bit pattern storage and sequencing while the IC is in PDM sequencing mode. Note the loopback multiplexer is under the control of the JTAG controller. When the chain is being loaded, the mux chooses the input from the JTAG block. When the chain is filled, the mux then selects the input from the end of the scan chain to provide the loop-around configuration necessary for pattern cycling.

The operation is as follows. First, a command is sent to the JTAG controller to place the IC into a user-defined mode, which we will call analog pattern configuration mode. The next command will select the required chains, concatenate them if necessary, and prepare them for data loading. If boundary scan flops are used, it may be necessary to issue additional commands to tri-state the pads to ensure that no pin drive conflicts or undesirable outputs occur. Once the chain is configured, and the multiplexer set to take the TDI input, data is serially shifted in via the TDI pin and clocked with the JTAG clock, TCK. When the data

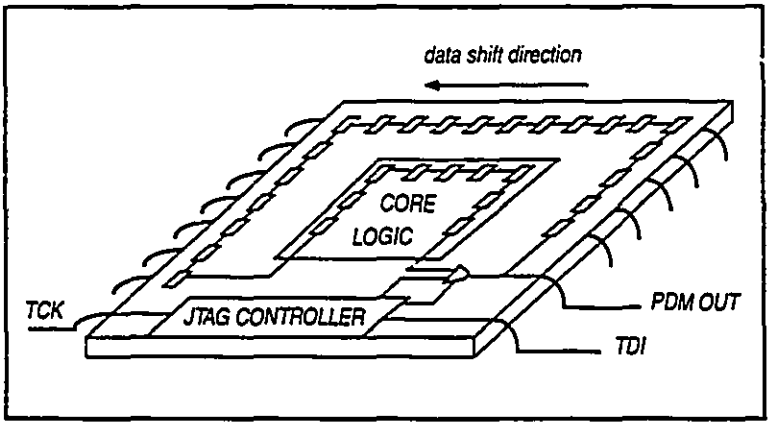


Fig. 5.6 - PDM Chain Configured Over Existing Scan Chains

shifting is complete, an instruction is issued to shift the mux input setting to create the loopback. If applicable, the PDM output driver is activated, and PDM pattern sequencing may commence. If the desired sampling rate using TCK is not fast enough (since TCK is generally a slower rate than the master clock), we can use the system clock to achieve better performance. Though this application drives the PDM pattern to a device under test that resides off-chip, it is possible to modify the configuration appropriately to conform to the requirements for MADBIST i.e. the generated pattern is used to excite circuits that exist on the same chip.

For circumstances that require a very long PDM pattern (or in the case that very few memory elements exist on the IC), we can extend the concept to span several ICs. That is, the chain is configured over multiple ICs via the test access ports, TDI and TDO, as in Fig. 5.7. Here we create a single scan chain over four ICs, with one dedicated test pin. Existing traces on the board can be used for interconnect between the ICs or, if necessary, a maximum of just one additional trace between each IC and two dedicated test pins per IC (one input, one output) will ensure a complete data path.

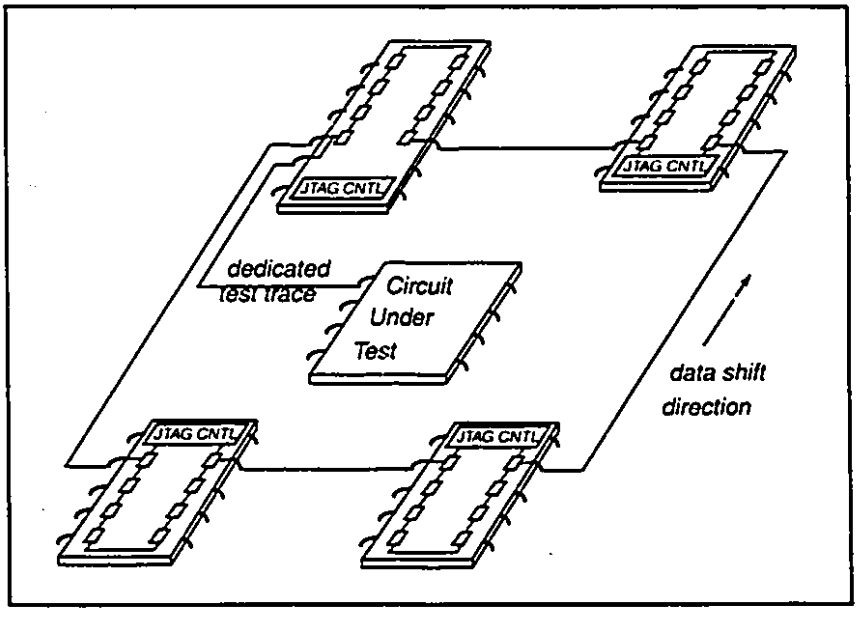
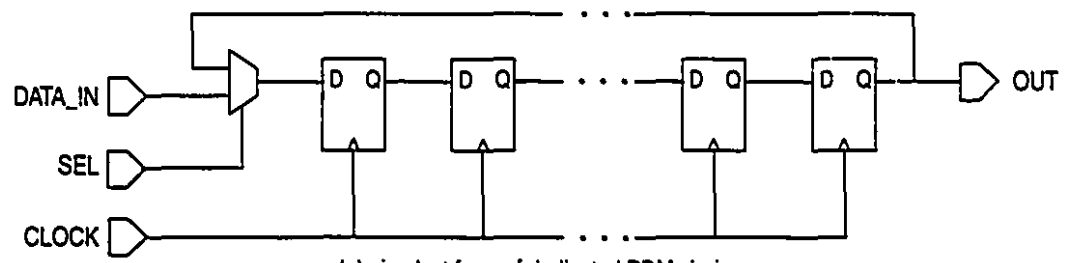


Fig. 5.7 - PDM Chain Configured Over Multiple ICs

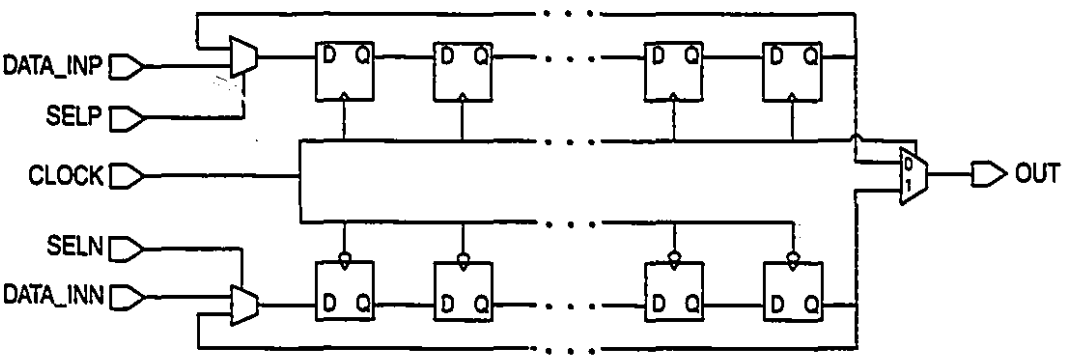
5.3.2 - Dedicated Chain Sequencing

An extension of the scan chain method is the design of a flip-flop chain dedicated for sequencing PDM patterns. This allows maximum-rate PDM generation since, as mentioned earlier, the only combinational logic is the feedback multiplexer. The pursuance of high sampling rates is purposeful, as the greater the sampling rate, the greater the frequency range of signal generation for a given SNR.

In the simplest case, the dedicated chain is designed as illustrated in Fig. 5.8(a). It consists of simply an *N*-bit flip-flop chain, a loop mux to select between the feedback signal and the loading input, and the sampling clock. The fact that the scan chain is dedicated for a simple shifting operation, however, allows us to use more sophisticated clocking and timing techniques. An example of such is given in Fig. 5.8(b). Here, we use both positive and negative-edge flip flops, effectively doubling the output data rate. The data stream is written into each register bank in an alternating pattern through the DATA_INP and DATA_INN pins on the positive clock edge and negative edge, respectively. Once loaded, the multiplexers are configured for loop-around mode and pattern shifting commences.



(a) simplest form of dedicated PDM chain



(b) dedicated PDM chain using both clock edges

Fig. 5.8 - Dedicated Chain Circuits

The output mux is triggered off the opposite polarity of the clock than the data being output (i.e., data from the positive-edge flops are output when the clock is a logic-0), thereby maximizing the data rate at which the circuit can run. Although not indicated above, any rise/fall time discrepancies could be minimized by appending a buffer or inverter to the output, as described previously in *Section 3.2 - Voltage and Current Signal Generation*.

A circuit similar to the schematic of Fig. 5.8(b) was designed into the Nortel 0.8µ BiCMOS standard cell fabrication process to provide area estimates for a typical design. The chain length was 128 bits i.e., each of the two chains was 64 flip-flops long. The layout of the circuit (complete with pads) is given in *Appendix A.5*. The total core area is approximately 0.46 mm^2. Because of the regularity and simplicity of the design, the area can easily be estimated for larger chains. For example, a chain length of 1024 bits would have an approximate area of 0.46 x 1024/128, or 3.68 mm^2. Verilog simulations of the above circuit showed a maximum data rate of approximately 250 Mbps, using worst-case models. Note that the above example used a fairly simple clocking scheme. By partitioning the chain into multiple sub-chains and using multi-phase clocks, higher data rates are possible.

5.4 - Design Considerations

There exist three main design considerations that influence the choice of architecture: area overhead, power consumption, and maximum output data rate. These considerations will be discussed for each architecture in the following sections.

5.4.1 - Area Overhead

With the exception of the dedicated chain, all architectures utilize existing hardware in some aspect. The dedicated chain requires a flip-flop for each bit to be stored. That is, for an *N*-bit pattern, *N* storage elements are required. The intent is that the dedicated chain will not be used for other functions on the chip. Thus, the greatest area overhead is associated with this architecture. The scan chain approach is based on pre-existing

boundary or internal scan chains. Since the serial chain configuration is already present, and can be loaded through the JTAG interface, there is negligible area overhead. It is thus the most area-efficient design.

Because of the logic requirements to control read/write addresses and a parallel-to-serial output conversion, the additional area of the RAM-based configurations is generally greater than the scan chain, but less than the dedicated chain. Between the processor- and hardware-accessible RAM configurations, the processor-accessible RAM is the most area-efficient since all read/write control hardware already exists on-chip. Conversely, the hardware-accessible RAM requires a JTAG data input interface for a write operation in addition to an on-chip address sequencer for read/write operations.

5.4.2 - Power Consumption

The differentiation between architectures in terms of power consumption lies in the method in which the data is transported. Since every single memory element in a chain is switching, serial chain configurations consume the most power per clock cycle. Generally, the larger the chain, the greater the power consumption. If the rest of the IC remains idle during sequencing, however, power consumption should be less than the normal operating modes of the IC. The dedicated chain, assuming a custom and compact layout, will consume less power than a scan chain of equivalent chain length.

The RAM-based applications, while having an increase in controlling complexity, move data bits in blocks (i.e. memory words) and thus consume less power than the chain architectures. Differences between the two RAM-based techniques are in the controller architecture. Since the hardware-accessible RAM has less complexity than the processor-accessible configuration, it will generally consume less power.

5.4.3 - Maximum Data Throughput Rate

The configuration with the highest sequencing rate is the one with the least amount of combinational logic or lengthy interconnect in the data path. Because the dedicated chain has the most regular structure with the least amount of controlling logic, it will generally

be the fastest sequencer. By contrast, the scan chain may suffer from long interconnect delays that may make it the slowest design.

The RAM configurations potentially provide the best data rates as the output data undergoes a parallel-to-serial conversion during which the clock rate can be significantly increased. It is anticipated however, that the slowest architecture is the processor-driven RAM technique, as the processor may not be able to generate read addresses fast enough. With address generation on-chip, as in the hardware-accessible RAM, that bottleneck is removed and data rates as high or higher than the dedicated chain could potentially be attained.

The performance of the architectures with respect to each design consideration is summarized in Table 5.2. A "1" indicates the highest ranking for a design. While there is no clear "winner", if the supporting hardware is already in place, and a parallel-to-serial conversion can be accompanied by a higher-speed data output clock, the ranking suggests that a hardware-accessible RAM-based architecture provides the best compromise of all three design considerations.

Table 5.2 - Performance Summary

Design Consideration	RAM-Based		Flop-Based	
	processor	hardware	scan	dedicated
area	2	3	1	4
power consumption	2	1	4	3
output data rate	4[a]	2	3	1

a. assuming a slow processor interface

The memory-based storage concepts presented in this work enable us to store and sequence finite patterns on-chip using the most common of memory devices: RAMs/ROMs and flip-flops. However, perhaps the key element is not which device is used but rather how the device configuration and sequencing can be integrated into virtually any digital IC. More specifically, the ability to use BIST logic gives the test engineer a familiar environment in which to move and/or generate test stimuli within an IC, among several ICs, or even across circuit boards. In addition, certain advantages

become available, such as the parallel-to-serial data rate increase with the RAM-based technique, or the concatenation of several chains for long pattern lengths, as in the scan chain approach. Also, the compactness of a dedicated chain is beneficial. Thus, we now have a very powerful and versatile analog signal generator that can easily be integrated into digital architectures.

Chapter 6 - Conclusions

In this chapter we will summarize this thesis, highlight the most critical concepts, and identify the original ideas and contributions which we feel will have the greatest impact on the mixed-signal test industry. We will conclude with some recommendations for further research. We feel the work presented here has created many opportunities for advancement in a variety of areas where analog signal generation is required.

6.1 - Summary

We began this thesis with a thorough study of integrated circuit testing. By defining and categorizing the different sources of error, we can now understand the different types of failure modes. A comprehensive examination of the impact of defects on both digital and analog circuits helped us appreciate their susceptibility to the different failure modes. A study of the electronic system hierarchy has better defined our test goals which will ensure maximal fault coverage with the least amount of effort. The culmination of the study of error sources, the impact of defects, and test hierarchies established the requirement for functional analog testing using precise analog signal generators. Thus, our desire to arrive at a precise, tunable, and compact signal generator is justified.

We introduced the reader to MADBIST -- a concept that is revolutionary in the mixed-signal test area -- but can benefit from a more compact signal generator. Next, the pulse, MBS, and PDM methods of bit-wide signal-encoding were studied. The premise here is that we want to encode an arbitrary analog waveform into a digital pattern. This allows the signal to traverse an unlimited number of circuits, ICs, or electronic media without any risk of signal degradation. The noise-shaping characteristic of the $\Delta\Sigma$ modulator, coupled with its ability to tune signal amplitude and frequency over a fixed bandwidth, makes PDM the preferred method for signal encoding.

Several applications of the $\Delta\Sigma$ oscillator were undertaken. In particular, the dedicated test system exemplified how a digital tester could be retrofitted to perform the tasks of a much more expensive analog tester. Refinements to PDM pattern and test circuitry were studied, such as the significance of a bipolar return-to-zero coding scheme and the use of a simple RC filter structure to limit input signal amplitude. The design of voltage and current signal generators was also introduced. The final application focussed on the design and simulation of two $\Delta\Sigma$ oscillator ASICs which, unfortunately, failed bench-testing, most likely due to improper fabrication.

An original concept, the forced-periodic PDM pattern, was then introduced. We can now benefit from all the positive attributes of a PDM-encoded signal with a compact and finite-length bit stream. Two approaches in determining the minimum pattern length, one the absolute smallest pattern for a given frequency and the other the smallest pattern for a given SNR, were developed and demonstrated how only a few bits can be used to encode an analog signal. A study of the effects of truncating the once-infinite PDM pattern was also put forth and various techniques were highlighted which can be used to improve the signal quality of a finite-length PDM pattern. Finally, waveform generation -- perhaps the greatest advantage with using a PDM coding scheme -- was examined. Through experimental results, we demonstrated the generation of multi-tone signals such as two-tone and sawtooth waveforms and showed how, by taking higher-spectrum images, finite-length PDM encoding can be used to generate high-frequency signals.

This thesis concluded with our second original contribution, namely applications for the forced-periodic PDM pattern using memory-based storage. We showed how analog signal generation can be integrated into digital architectures presently found on most ICs. The RAM-based approach utilizes an existing RAM or ROM structure to store and play back a finite-length PDM pattern. Using the logic found in the 1149.1-1990 IEEE Standard JTAG controller and/or RAMBIST controller, analog signal generation can be simply added to any IC. The RAM application also benefits from the parallel-to-serial conversion on output which serves as an excellent opportunity to increase the data sampling rate. This yields increased signal quality through a greater oversampling ratio or an increase in

signal bandwidth. Another application uses the flip-flop scan chain structure. Again, by utilizing the power of the JTAG controller, one or several scan chains spanning one or more ICs can be configured to sequence a PDM pattern for analog signal generation. This is achievable with no additional area overhead. Alternatively, one can design the dedicated scan chain which allows the designer to use sophisticated clocking techniques resulting in maximum data sequencing throughput limited only by technology.

The concepts presented here are anticipated to make a significant contribution to the mixed-signal test field. With compact pattern sequencers, MADBIST now consumes even less area and is thus more feasible. But perhaps most importantly, analog signals can now be integrated into virtually any digital environment and have the potential to become a standard for analog signal generation in any analog or mixed-signal application.

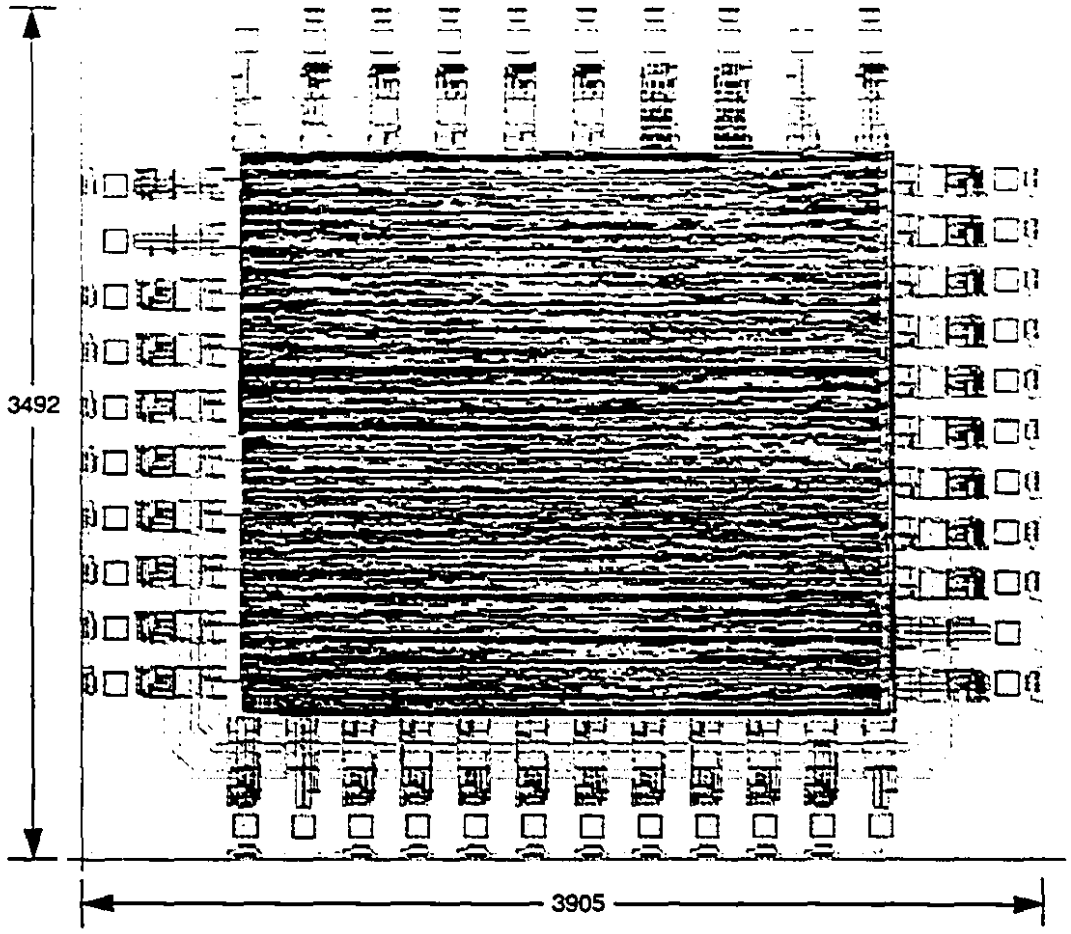
6.2 - Recommendations For Further Research

The research and development of finite-length PDM patterns and their applications have exposed certain areas in which further work would be most welcome. First, there exists the opportunity for improved signal quality by capturing a bit pattern on which dithering has been applied. Dithering is currently being used on $\Delta\Sigma$ modulators in an attempt for better performance, so it seems reasonable that the techniques presented in this thesis could benefit. Second, further research on integrating a PDM controller into the 1149.1 interface will certainly warrant the attention of test engineers and ensure the integration of memory-based storage techniques into the digital test architectures of today. Third, work on data collection and measurement techniques will complete the entire dedicated test system and MADBIST packages. Presently, measurement techniques require either extensive computing power or cumbersome digital filters. Advancements leading to a logic reduction will be a significant contribution to the mixed analog-digital test environment. Finally, truncated PDM patterns are not limited only to test applications. They provide a very compact and simple method of generating waveforms that could be used wherever analog signal generation is required. This creates a whole new area of research to be explored.

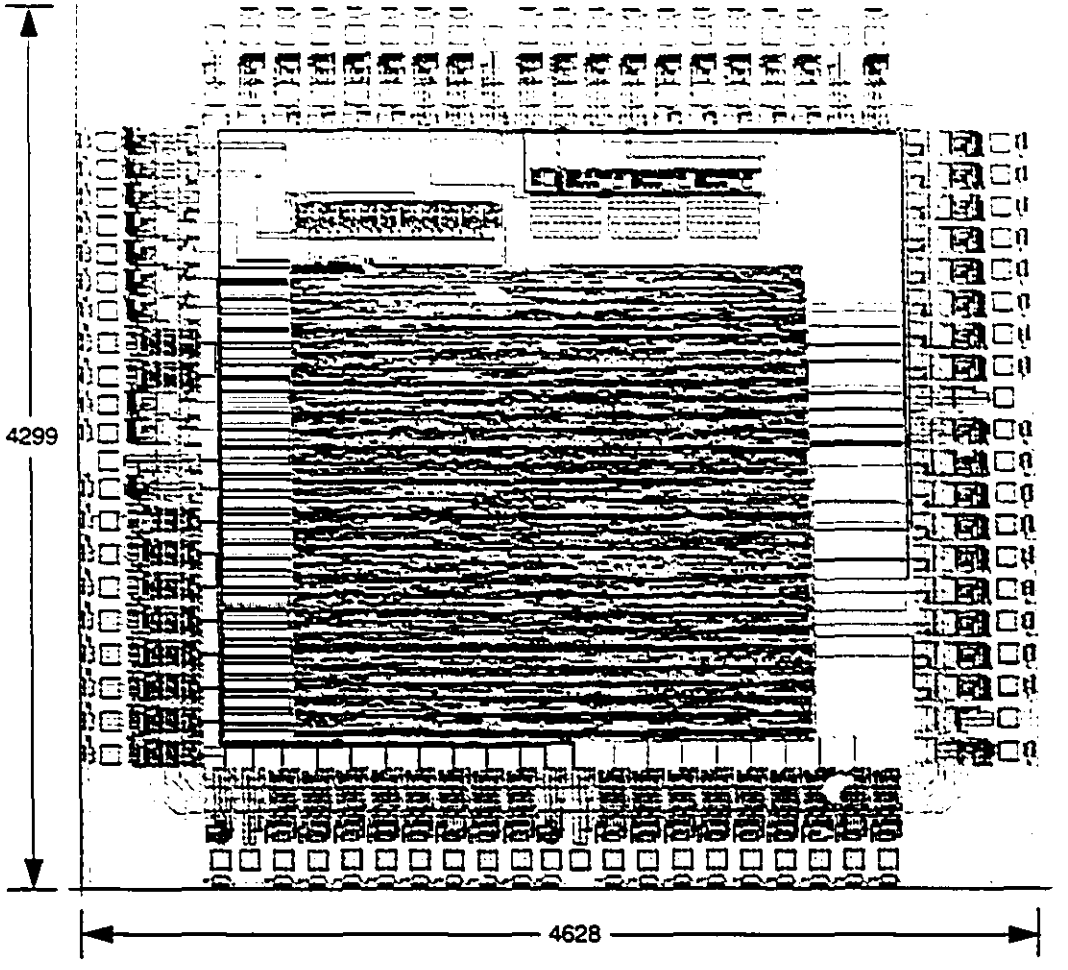
Appendix A - ASIC Layouts

This section contains layouts of various ASICs and components. The first is chip code IBAMGOSC, a fully digital fourth-order modulation oscillator ASIC. The second layout is chip code IBAMGODF, a fourth-order modulation oscillator, a one-bit D/A converter, and a sixth-order lowpass reconstruction filter. Included are also the layouts of the DAC and reconstruction filter, as used in IBAMGODF. Both ASICs were fabricated using the Nortel 0.8µ BiCMOS process. The final illustration is a layout of a dedicated flop chain. Note that this circuit was not fabricated; rather, the circuit was designed as an exercise to demonstrate the area efficiency of a dedicated chain approach as a memory-based storage technique. All dimensions are in micrometers (µm).

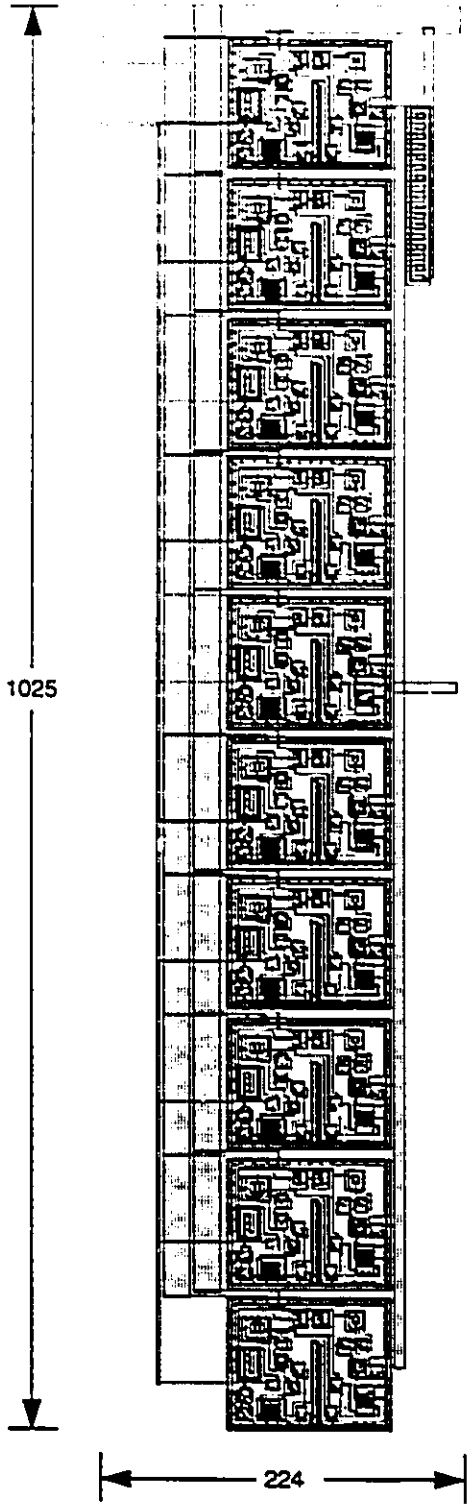
A.1 - IBAMGOSC ASIC



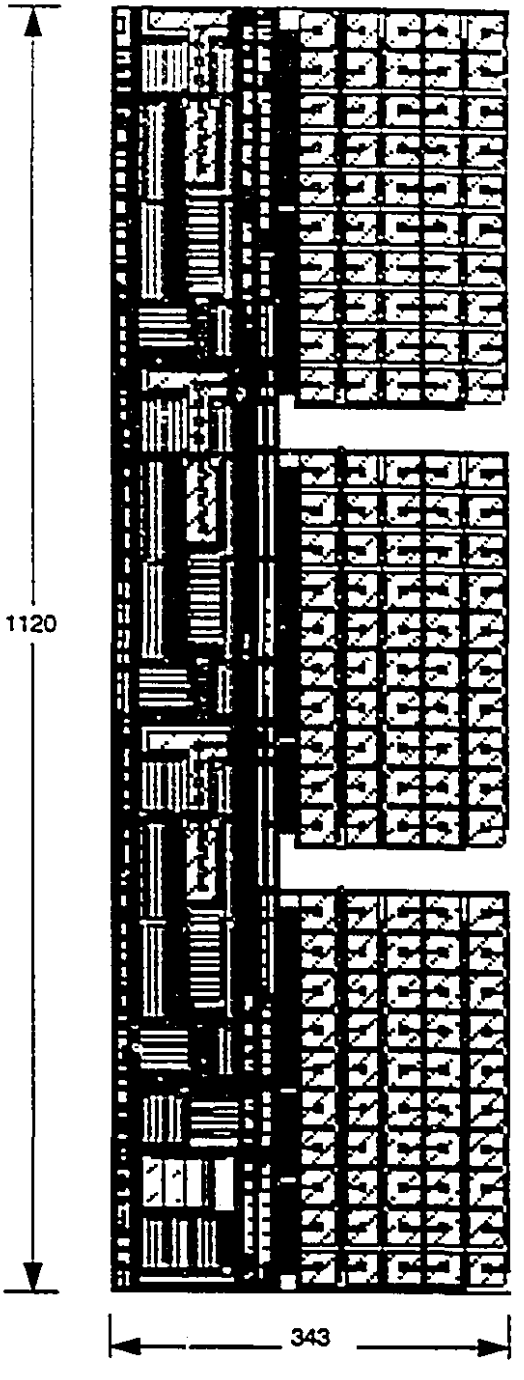
A.2 - IBAMGODF ASIC



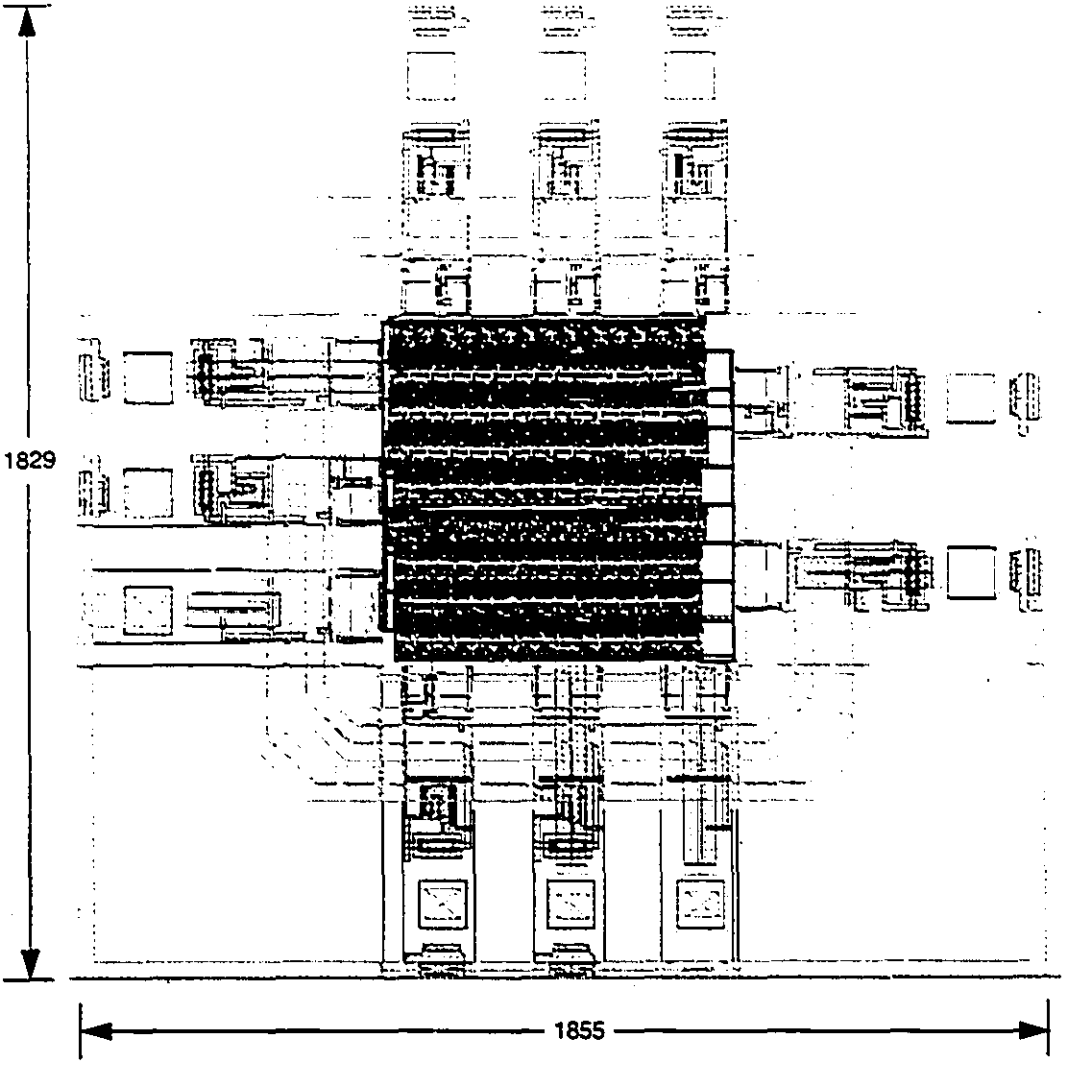
A.3 - One-Bit Digital-to-Analog Converter



A.4 - Sixth-Order Reconstruction Filter



A.5 - Dedicated Flip-Flop Chain



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