DC Power Flow Controller and Marx DC-DC Converter for Multiterminal HVDC System

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A thesis submitted to McGill University in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

Abstract

This thesis presents the concept of the dc power flow controller to address the power flow control issues inside a multiterminal High Voltage Direct Current (HVDC) system. The controller is connected in series on the HVDC transmission line and it is presented as a small appendage of a voltage source converter (VSC) station. The operation and the stability are shown via simulations of a 3-terminal and a 7-terminal HVDC grid. The controller increases the flexibility and the region of operation of the multiterminal HVDC system.

The integration of an offshore wind farm into a multiterminal HVDC system is also studied. By using a dc collector network for the aggregation of power produced by the wind turbines, the high civil engineering cost of an offshore platform to support heavy ac transformers required by the converter station for HVDC transmission can be avoided. The challenge is to bridge the two dc voltages without ac transformers.

This thesis introduces and analyzes a new dc-dc converter topology which is based on the Marx generator concept. The concept consists of charging capacitors in parallel followed by reconnection in series of the capacitors to create higher dc voltage. The converter with a multi-stage configuration is simulated for proof of concept. Design guidelines are developed and a 5kW prototype has been constructed to verify experimentally the converter topology. The stability of the converter is analyzed using a sampled-data approach and the power ratings of the semiconductor switches and passive components are evaluated.

For offshore wind farm application, the Marx dc-dc converter is combined with a step-up converter to form the Marx offshore station which bridges the 10kV dc collector network to the 250kV HVDC transmission line. The Marx offshore station is simulated with an offshore wind farm and an onshore VSC inverter station.

The two parts of the thesis, the dc power flow controller and the Marx dc-dc converter, are integrated within a complete multiterminal HVDC system. The simulated system comprises six VSC terminal stations, the Marx offshore station with an offshore wind farm and the dc power flow controller. Both the dc power flow controller and the Marx dc-dc converter enlarge the scope of multiterminal HVDC system.

Abrégé

Cette thèse présente le concept d'un contrôleur de transit de puissance afin de résoudre la problématique de contrôle des mouvements d'énergie dans un réseau multiterminal à courant continu à haute tension (CCHT). Le contrôleur est installé en série sur la ligne de transport CCHT et il est présenté comme un module ajouté à une station convertisseur à CCHT. Le fonctionnement et la stabilité sont démontrés à l'aide de simulations dans des systèmes multiterminaux de 3 et de 7 terminaux. Le contrôleur augmente la flexibilité et l'étendue de l'exploitation d'un système multiterminal CCHT.

L'intégration d'un parc éolien installé en mer avec un système multiterminal CCHT est aussi étudiée. En utilisant un réseau à courant continu (cc) pour collecter la puissance produite par les éoliennes, les coûts d'infrastructure associés au support de lourds transformateurs à courant alternatif (ca) requis pour la station du convertisseur servant au transport CCHT peuvent être évités. Le défi consiste à relier les deux tensions cc en omettant l'utilisation de transformateurs ca.

Cette thèse introduit et analyse une nouvelle topologie de convertisseurs cc-cc qui est basée sur le concept du générateur Marx. Ce concept consiste à charger des condensateurs en parallèle pour ensuite les connecter en série afin de créer une tension cc plus élevée. Un convertisseur avec une configuration multi-étapes est simulé pour une démonstration de faisabilité. À partir de balises de conceptions, un prototype de 5kW a été conçu, simulé et construit afin de vérifier expérimentalement la topologie du convertisseur. La stabilité de la topologie a été analysée en utilisant une approche de données échantillonnées et des caractéristiques nominales des semiconducteurs de puissance et des composants passifs sont évaluées.

Pour l'application dans un parc éolien installé en mer, le convertisseur cc-cc Marx est jumelé avec un hacheur survolteur afin de former une station Marx qui lie le réseau collecteur cc de 10kV au réseau de transport CCHT de 250kV. La station Marx est simulée avec un parc éolien et un convertisseur onduleur.

Les deux parties de cette thèse, soit le contrôleur de transit de puissance et le convertisseur cc-cc Marx, sont regroupés dans un même système multiterminal CCHT. Le réseau simulé comprend six stations convertisseurs de type "voltage source converter", la station Marx avec le parc éolien installé en mer et le contrôleur de transit de puissance. Le contrôleur de transit de puissance et le convertisseur cc-cc élargissent la portée du système multiterminal CCHT.

Acknowledgements

I would like to thank my thesis supervisor, Professor Boon Teck Ooi, for his guidance and support throughout my doctoral studies. I am honoured to have had the opportunity to work with such a wise man of great knowledge and experience. He challenged me with his continuous flow of new research ideas and concepts. I have really enjoyed our discussions on research, politics and worldwide history during his daily visits in the laboratory.

I want to express my gratitude to Professor Peter Lehn, from the University of Toronto, for welcoming me into his research facility for my experimental work. I would like to thank him for the time he had accorded to me, despite his busy schedule. A special thanks to my good friend Damien Frost for his technical and entertainment expertise in the laboratory during my time at the University of Toronto.

I am also grateful to Professor Benoit Boulet from my Ph.D. supervisory committee for providing constructive inputs during our yearly meetings. I also want to express my gratitude to my friends and colleagues in the McGill Power Group for their help and advice throughout these past few years.

I would like to acknowledge many institutions that have provided me with financial support for the duration of this work: the FQRNT[1] for the Bourse de doctorat en recherche, McGill University for the McGill Engineering Doctoral Award (MEDA) and for the GREAT Awards[2], and the Walter C. Sumner Foundation for the Walter C. Sumner Fellowship.

Finally, I would like to express my sincerest thanks to my parents, Lise and Rhéaume, and my family for their constant encouragement and support over the years. More importantly, my deepest gratitude goes to my lovely fiancée, Annie.

Étienne Veilleux
Winter 2013

"*If I have seen further it is by standing on the shoulders of giants.*"
Sir Isaac Newton, 1676.

[1]Fonds Québécois de la Recherche sur la Nature et les Technologies
[2]Graduate Research Enhancement and Travel Awards

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List of Acronyms

AC or ac	Alternating Current
DC or dc	Direct Current
FACTS	Flexible AC Transmission System
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate-Commutated Thyristor
MMC	Modular Multilevel Converter
MPPT	Maximum Peak Power Tracking
MTDC	Multiterminal HVDC
PMSG	Permanent Magnet Synchronous Generator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

Chapter 1

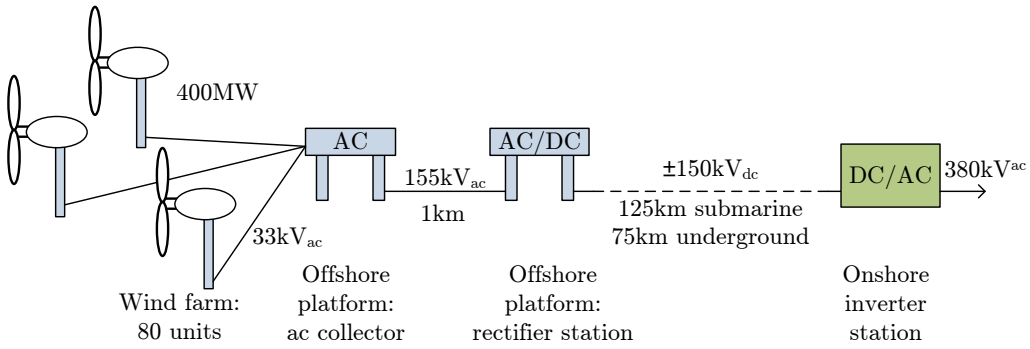
Introduction

1.1 Background

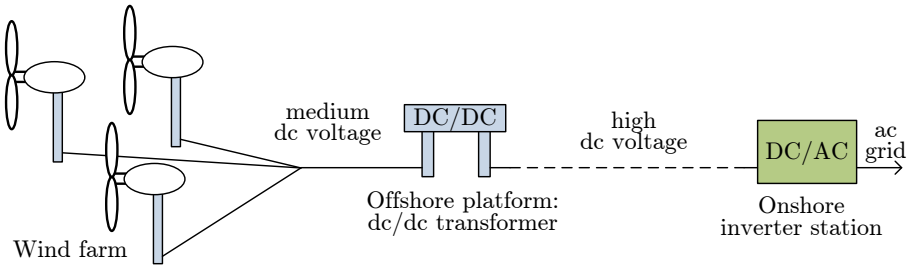
High Voltage Direct Current (HVDC) technology has been applied mainly in two aspects of power engineering: bulk power transmission over long distance and interconnection between two ac networks of different frequencies or same frequency but different phase angles. The development of self-commutating power electronics switches suitable for high power and high voltage has extended the range of application of HVDC. For example, the recent submarine link in the San Francisco region is using HVDC with self-commutating technology [1,2]. Similar technology is used for offshore wind farms like the BorWin1 project linking the BARD Offshore 1 wind farm to Germany [3].

Multiterminal HVDC (MTDC) has been of interest since the earliest days of HVDC transmission [4,5]. HVDC then was based on current source converters of line-commutated thyristors. As current source converters are not suitable for parallel connection, MTDC based on them came to a halt. With the arrival of voltage source converters (VSC) based on self-commutating switches (GTOs, IGBTs, IGCTs, etc), HVDC has a revival, for example, under the tradename like *HVDC Light*® (ABB) or *HVDC PLUS* (Siemens). As VSCs are suitable for parallel connection across the dc terminals, VSCs are considered as the technology for providing a HVDC grid. MTDC is a serious contender for future transmission projects especially the ones related to renewable energy.

Supergrids have proposed MTDC to bring offshore wind farm power onshore, to transmit solar energy produced in north Africa to Europe and to create power transfer corridors [6–9]. The rationale for considering the self-commutating converter family for MTDC is that their dc sides are ideal-current



(a) BARD Offshore 1 wind farm project.



(b) Offshore wind farm with dc collector bus.

Figure 1.1: Examples of offshore wind farm arrangements.

sources and, therefore, they can be connected in parallel naturally.

There are still many challenges that need to be addressed in order to put in operation such MTDC. Among them, the limitation regarding the power flow control is major obstacle as discussed in [10]. As opposed to ac network where both the voltage magnitude and the angle can be controlled, only the voltage magnitude can be regulated in a MTDC.

A suitable MTDC system should offer enough flexibility to control the power flow without imposing limitations on transmission lines connected to a terminal station. To address this issue, the addition of an auxiliary dc voltage controller is proposed in this thesis. By doing so, the MTDC power flow controllability is improved.

The application of MTDC for offshore wind farm is also studied. The aggregation and transmission of wind power from offshore to the mainland remains a technical challenge. Actual configuration includes the construction of offshore platforms to install equipment required for transmitting power onshore. Figure 1.1(a) shows the example of the BARD Offshore 1 wind farm project where two platforms were required [3, 11, 12]. It would be an advantage to avoid such arrangement by having a configuration that would allow

transmission with the need of only one offshore platform. The ac transformers on the offshore platform are the largest single equipment installed [13] and it requires expensive structural design to support its heavy weight.

By eliminating the ac collector offshore platform, the structural requirement for heavy ac transformers can be avoided but the challenge is to bridge the two voltages without ac transformers but rather with dc-dc transformer as shown in Figure 1.1(b). A dc collector bus would then be required to gather the wind power to the dc-dc transformer platform. In this research, an offshore wind farm configuration is developed to interconnect wind turbines and to transmit power onshore. A dc-dc converter topology suitable for this application is presented in this thesis.

1.2 Scope

The scope of the thesis is to develop two aspects of MTDC system: improve power flow controllability and aggregation method for offshore wind farm. An overview of the HVDC grid is illustrated in Figure 1.2. The power flow controllability is achieved by developing an auxiliary dc controller to be inserted on the HVDC grid to add control flexibility. The offshore wind farm is based on a dc collector network where the configuration includes the innovative dc-dc converter topology.

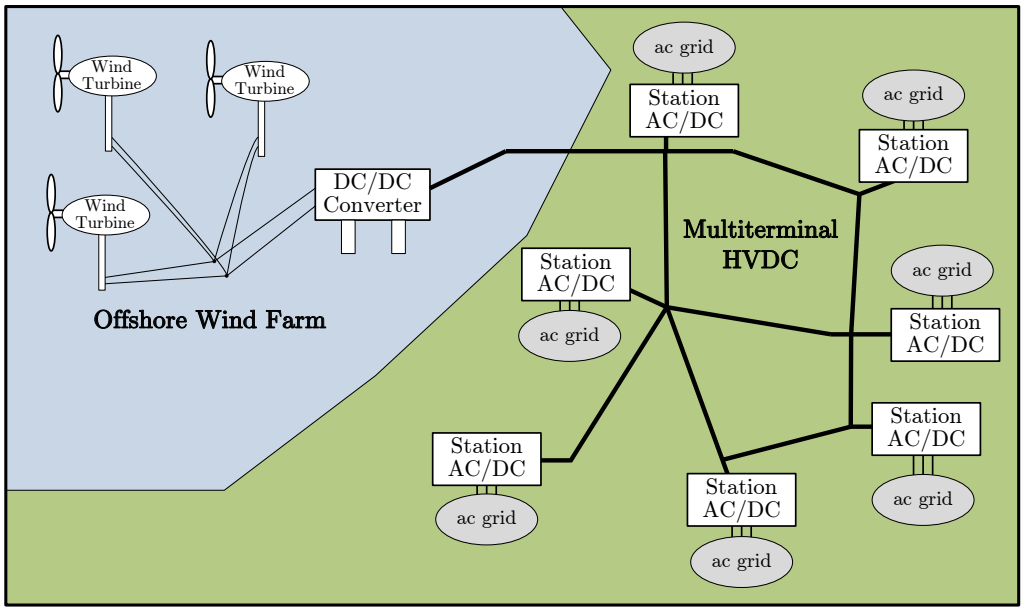


Figure 1.2: Multiterminal HVDC with offshore wind farm.

1.3 Literature Review

1.3.1 HVDC Grid

Three main converter topologies are currently used for HVDC system. The thyristor-based converter, also called conventional HVDC, is used for bulk power transmission system [14]. It is a mature technology that has proven its robustness through the years. Originally around ±400kV, the voltage rating can go up to ±800kV in Ultra High Voltage Direct Current system (UHVDC). However, this converter topology requires a strong ac grid voltage since it is a line-commutated converter and it consumes reactive power.

Initially constructed for low and medium voltage, the VSC based on IGBTs has entered the high voltage range. It has the advantage of having better control of its reactive power consumption and it can be connected to a weak ac system [15]. The typical voltage range is around ±250kV but it can go higher.

The third topology is a configuration based on multilevel converter. The modular multilevel converter (MMC) is based on half-bridge submodules connected in series [16, 17]. The modularity of the concept makes it a very attractive solution to the industry. The operation advantages are similar as for the VSC since it also uses IGBTs as power electronics switches.

In developing HVDC grid, VSC and MMC are both expected to be involved. In this thesis, MTDC is based on VSC terminal stations but the conclusions obtained can be extended to MMC-based HVDC grid.

Among the challenges of developing HVDC grid, the behaviour of the converter under faulty conditions is of particular interest. As opposed to ac, dc current does not pass by zero periodically which makes it difficult to break the dc fault current. This issue is out of the scope of the thesis but it is worth mentioning that many researchers are addressing the situation and they have proposed various analysis and solutions [18–23].

The limitation of only controlling the dc voltage magnitude has an impact on the power flow control of the HVDC grid [6, 10]. In MTDC with thyristor-based converter, power flow control using telecommunication and central reference balancer has been suggested in [24]. However, it is desirable to have the controls independent of telecommunication link especially in the perspective of a large MTDC. Recent proposals have suggested the use of master/slave control [25, 26] and voltage droop control [27–31]. In both approaches, the

control strategy varies but the MTDC remains with the same limited number of controls.

Another approach to redistribute the power transmitted on HVDC lines is to insert a device for additional voltage control into the HVDC grid. The installation of an auxiliary dc voltage controller at one end of the line can influence the power flow if it can vary the voltage on that line. The thesis presents a solution for this power flow control problem through an auxiliary dc voltage controller inserted in a dc transmission line.

The controls of ac system and dc grid are different. AC bus has two degrees of freedom: ac voltage magnitude and phase angle. They enable PQ control and there are four different types of buses used in power flow analysis. More precisely, they are voltage-controlled (PV), load (PQ), device (special type like HVDC converters) and slack (swing) buses [32]. Each bus has parameters which define voltage magnitude, voltage angle, real power and/or reactive power. In contrast, only the dc voltage can be controlled in MTDC systems. So, three different categories of terminal stations can be defined for HVDC systems:

1. *Voltage regulator* acts as the dc bus reference. It is also called the "slack bus" because it controls the ac active power, P_{slack}, so that the algebraic sum of power in the HVDC grid is zero. The Q control on the ac side supports the ac voltage.

2. *Controlled power injection* has a specific power contribution into the HVDC grid. It can be either positive (generation) or negative (load). It is also called complex power dispatcher because the converter regulates both the real and reactive power on the ac side (PQ control).

3. *AC bus reference* regulates the ac side voltage and frequency. Commonly used for wind farm where it serves the equivalent of an infinite ac bus.

Table 1.1 summarizes the categories and their control references. In this thesis, only the first two types of terminal stations are used.

Connecting offshore wind farms to a HVDC grid poses interesting challenges [33, 34]. Conventional arrangement, as shown in Figure 1.1(a), involves many power conversion steps from ac to dc and vice-versa. The wind turbine outputs ac at varying frequency which is then converted to ac at fixed frequency via an ac-dc-ac converter. The power from the wind turbines of the

Table 1.1: Control references of HVDC terminal station

	AC Side		DC Side
Voltage Regulator	P_{slack}	Q^{ref}	V_{dc}^{ref}
Controlled AC Power Injection	P^{ref}	Q^{ref}	V_{dc} from dc circuit analysis
AC bus reference	V^{ref} P and Q vary	f^{ref}	V_{dc} from dc circuit analysis

wind farms is collected in ac and then it is rectified to dc for HVDC transmission. By avoiding the intermediate ac collector network, the wind turbines are interconnected using dc link [35]. The elimination of the wind turbine ac transformer can improve the overall efficiency of the unit by up to 1.4% [36]. The wind farm configuration used for this research is parallel connection of wind turbine units [37–39]. The units are connected to a common dc link and there is a converter station with a dc-dc converter to bridge the dc collector network to the HVDC grid for transmission purposes.

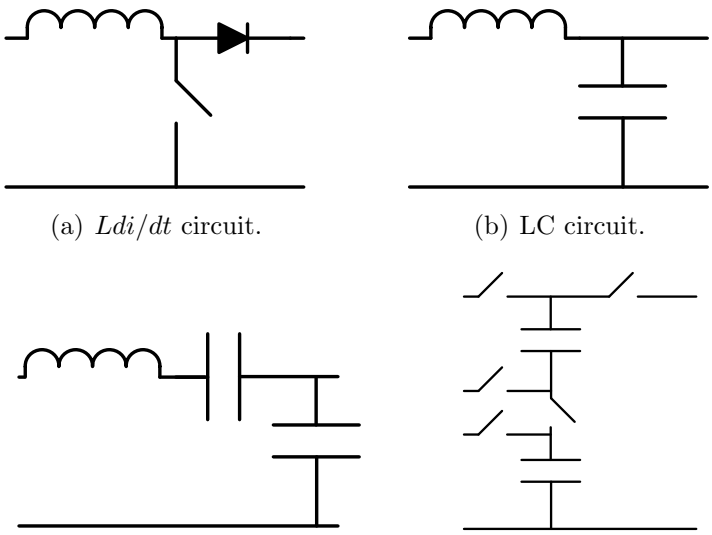
1.3.2 DC-DC Converter

High voltage, high dc power supplies are used in scientific, medical and military community for applications in systems related to X-ray, radar, travelling wave tubes (TWT) and TEA lasers. The power levels range from 120mW to 150kW with voltages from few volts to 500kV for airborne, satellite and space station environment where iron core transformers are to be avoided.

The technologies which can step-up to very high voltages without transformers make use of Ldi/dt boost voltages [40–42], LC resonance [41,42], LCC resonance [40] or switched-capacitor converter [43].

The topologies using Ldi/dt take advantage of the rapid change of current in an inductor to create a large voltage. The stepped-up voltage is then captured at an output stage. The example of the conventional step-up (boost) converter is shown in Figure 1.3(a). Topologies using LC and LCC resonances create an oscillatory environment to amplify the voltage. Figure 1.3(b) shows a parallel tank circuit for LC and Figure 1.3(c) shows an arrangement for LCC resonance. The topologies using switched-capacitor creates higher voltage by connecting capacitors in series. An example is shown in Figure 1.3(d).

This thesis revisits the Marx generator concept which was invented in Ger-



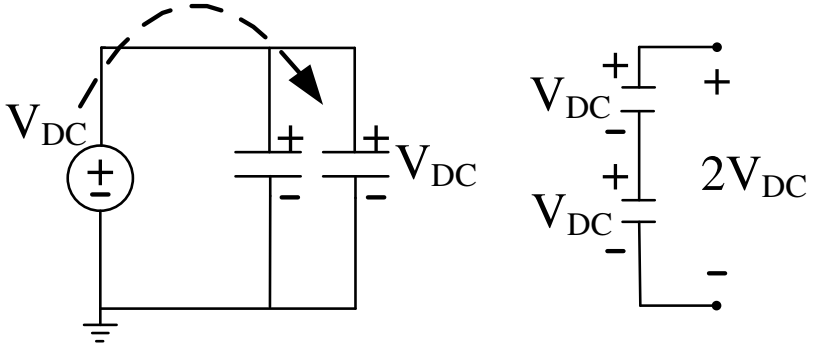
(a) Ldi/dt circuit.

(b) LC circuit.

(c) LCC circuit.

(d) Switched-capacitor.

Figure 1.3: Examples of dc voltage step-up topologies without transformer.



(a) Capacitors in parallel during charging phase.

(b) Capacitors in series to create higher voltage.

Figure 1.4: Marx generator concept.

many by Erwin Marx around 1923 [44,45]. The concept of the Marx generator is shown in Figure 1.4 for a dc amplification of 2. It consists of charging capacitors in parallel, shown in Figure 1.4(a), followed by a reconnection in series for creating higher output voltage, shown in Figure 1.4(b). The classical Marx generator uses spark gaps to connect capacitors in series and to create a single high voltage pulse. Adaptations of the original topology have been made for insulation testing of high voltage equipment [46] and X-ray generation [47].

Nowadays with solid-state switches, modern topologies based on the same principle of connecting capacitors in series and in parallel have been presented in [48–61]. The application varies from research laboratory [56, 57] to photovoltaic [58] and even inverter converter [53]. However, most of the topologies presented are pulse generation type of converter and they are not suitable for continuous high power application. The research of this thesis is oriented toward applications where heavy ac transformer should be avoid but dc voltage step-up is still required to bridge the low voltage of offshore wind turbine to the high voltage of HVDC grid.

The objective of the thesis is to develop a high power Marx converter suitable for continuous current operation. In order to reach very high dc voltage gain at economical cost, the concept of cascading stages is incorporated into the research [62–65]. By doing so, an overall dc gain of M^N can be achieved by using N stages of Marx modules, each having a gain of M. The research in the thesis resides in the new dc-dc converter topology developed.

1.4 Research Objectives

The objective of the thesis is to improve power controllability of the HVDC grid. Unlike ac systems which have two degrees of controllability (P and Q), the HVDC grid depends on the value of the dc voltage at the terminals [10]. The thesis proposes the dc power flow controller to address this deficiency in Chapters 2 to 4.

The next issue relates to offshore wind farm which transmits dc power. Because the weight of iron transformer add to civil engineering cost, the thesis investigates the possibility of dc-dc conversion with dc voltage amplification without ac transformer. The solution proposed is the Marx dc-dc converter of Chapters 5 to 9.

1.5 Thesis Contributions

The items listed below are original contributions in the area of power engineering, HVDC systems and dc-dc converter.

1.5.1 DC Power Flow Controller

- The DC Power Flow Controller, as an auxiliary controller of a VSC station, based on thyristor-based dual-converter. The DC Power Flow Controller is inserted in a dc transmission line to increase the controllability of a dc grid based on multiterminal HVDC. (Chapters 3 and 4)

- Apart from the realization of the controller, the research has evaluated that the controller does increase the feasible region of operation of the dc grid thus justifying its presence. (Chapter 2)

1.5.2 Marx DC-DC Converter

- The innovative dc-dc converter, which has been adapted from the well known Marx generator to serve as a continuous high voltage, high power dc-dc converter. Besides simulation, experimental prototypes have been constructed and tested for proof of concept. (Chapters 5-7)

- Innovation, which consists of electric charge transfers from the input end to the output end using L-C resonance with a diode to the inductor to ensure continuous, unidirectional power transfer. (Chapters 5 and 6)

- Innovation, which consists of design equations for determining the capacitor size for dc voltage gain M. (Chapter 6)

- Innovation, which consists of applying cascading stages to the Marx dc-dc converter. As the dc voltage increases in each stage, it has a corresponding current decrease whereby the VA rating is constant at each stage. (Chapters 5 and 6)

- An innovative method of asymptotic stability analysis based on solving linear equations $\dot{x} = Ax + Bu$ in each sub-period of IGBT switching and integrating the output states at the end of the kth sub-period as the initial state of the (k+1)th sub-period. Stability is assured when the

eigenvalues are lying within the unit circle in the complex plane. (Section 8.1 of Chapter 8)

- A method of cost evaluation for the choice of N (the number of cascading stages) and M (the dc voltage gain of each stage) to achieve an overall dc voltage gain of M^N. The method depends on deriving equations for components based on the voltage and current ratings at each stage. (Section 8.2 of Chapter 8)

1.6 Thesis Overview

The thesis is organized such that the dc power flow controller is explained in Part I (Chapters 2 to 4) and the dc-dc converter topology is described in Part II (Chapters 5 to 9). Finally, in Part III (Chapter 10), the dc power flow controller and the dc-dc converter topology are integrated to form a complete MTDC system with offshore wind farm integration and power flow controllability.

1.6.1 Part I: DC Power Flow Controller

Chapter 2 presents the concept and the benefits of the dc power flow controller. The operation of the controller within a MTDC is described and it is shown for 3-terminal and 4-terminal HVDC grids. Chapter 3 details the hardware realization of the dc power flow controller. Control strategy is presented and implemented on a 3-terminal HVDC system. The system is fully modeled with VSC stations and the dc power flow controller. Chapter 4 studies a larger MTDC composed of 7 terminal stations. Various scenarios are discussed including transmission line contingency.

1.6.2 Part II: Marx DC-DC Converter

Chapter 5 describes the basic configuration of the Marx dc-dc converter. Models for single-stage and cascade configuration are analyzed. Chapter 6 introduces design guidelines. The analysis includes considerations such as losses and dead-time requirements. Chapter 7 shows the 5kW prototype constructed. Laboratory test results are obtained to demonstrate the operation of the converter. Chapter 8 analyzes the stability of the converter through piecewise

linear approach. In addition, parameters ratings are evaluated for the semiconductor switches and passive components (inductors and capacitors). Chapter 9 describes a 200MW offshore wind farm connected to a VSC station via a Marx offshore station.

1.6.3 Part III: Complete Multiterminal HVDC System

Chapter 10 shows a complete system composed of a 7-terminal HVDC grid with a dc power flow controller and a 200MW offshore wind farm. The chapter integrates the two research topics addressed in Parts I and II of the thesis.

Finally, the conclusion is in Chapter 11. It provides a summary of the thesis, conclusions from the research of this thesis, the list of original contributions and it discusses of future work. The associated publications related to this work are listed in Appendix A.

Part I

DC Power Flow Controller

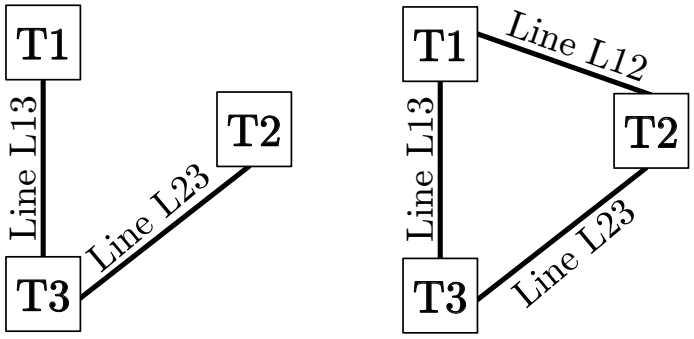
Chapter 2

DC Power Flow Controller: Concept and Benefits

In this chapter, the concept of the dc power flow controller is explained. A simple 3-terminal system is described to give a good picture of the situation. The 3-terminal system has initially two transmission lines and it is upgraded to three lines. The 3-line 3-terminal system is introduced with the dc power flow controller and the benefits are evaluated using the region of operation. Then, a 4-terminal system is explored. The objective of the chapter is to evaluate the benefits of a dc power flow controller inserted on a transmission line using two case studies: a 3-terminal grid with three lines and a 4-terminal grid with five lines.

2.1 System Description

In the 3-terminal system shown in Figure 2.1(a), terminal stations T1 and T2 are fixed-power terminal stations and terminal station T3 is the voltage regulator. The scenario can be an interconnection between two countries (terminal stations T1 and T2) via submarine dc cables (link L13) and a wind farm (T2) is connected onshore to T3 by link L23. In the perspective of developing a HVDC grid, a third line can be installed between terminal stations T1 and T2 as shown in Figure 2.1(b). In the proposed scenario, the justification can be to maximize the use of the already built link L23 when low wind power is produced. For the benefit of the argument, it is assumed that the addition of the line L12 would be less costly than a new line from T1 to T3. By doing so, it offers the ability to transmit power from T1 to T3 via the link L12-L23.



(a) 2-Line HVDC grid. (b) 3-Line HVDC grid.

Figure 2.1: MTDC grid configurations with 3 terminal stations.

Table 2.1: 3-Terminal - transmission line parameters.

Transmission Line	**Distance** [km]	**Resistance** [Ω]	**Current Limits** [kA]
L13	413	5	0.87
L23	248	3	0.44
L12	330	4	0.4

Another advantage would be to satisfy N-1 contingency requirement to the system.

2.1.1 From 2-Line to 3-Line

The HVDC grid without the dc power flow controller is solved with two lines and then with three lines. The transmission line parameters are listed in Table 2.1. Details and references about the transmission line model can be found in Section C.3 of Appendix C. In this scenario, the dc voltage of T3 is regulated at 250kV, terminal station T1 supplies 200MW and terminal station T2 injects 100MW. The results for the HVDC grid with two and three lines without a dc power flow controller "M" are given in Table 2.2.

2.1.2 3-Line 3-Terminal HVDC Grid

The analysis of the 3-terminal system, shown in Figure 2.1(b), is done by solving power equations. The starting point is the voltage of the dc voltage regulator ($V_{T3} = 250kV$). Routines are executed to find terminals' voltages for a range of powers for terminal station T1 (P_{T1}) and terminal station T2

Table 2.2: 3-Terminal - scenarios.

	2-Line Fig. 2.1(a)	**3-Line no M** Fig. 2.1(b)	**3-Line with M** Fig. 2.4(a)	**3-Line with M** Fig. 2.4(b)
P_{T1} [MW]	200	200	200	↑ 220
P_{T2} [MW]	100	100	100	↓ 80
V_{T3} [kV]	250	250	250	250
M	-	-	0.989	↑ 0.991
V_{T1} [kV]	253.9	252.8	254.0	253.9
V_{T2} [kV]	251.2	251.9	251.2	251.2
I_{L12} [kA]	0.788	0.561	0.792	0.776
I_{L23} [kA]	0.398	0.627	0.394	0.410
I_{L12} [kA]	-	0.230	-0.004	0.091

(P_{T2}). To determine if the operating point is valid, line currents are calculated and it is determined if currents are exceeding the limits listed in Table 2.1. The calculation algorithm and details are given in Appendix B. In a HVDC grid, the currents are calculated using voltages and line resistances only. The equations of the currents are:

$$I_{L13} = \frac{V_{T1} - V_{T3}}{R_{L13}} \tag{2.1}$$

where the current limit is 0.87kA,

$$I_{L23} = \frac{V_{T2} - V_{T3}}{R_{L23}} \tag{2.2}$$

where the current limit is 0.44kA,

$$I_{L12} = \frac{V_{T1} - V_{T2}}{R_{L12}} \tag{2.3}$$

where the current limit is 0.4kA. Using those equations, the power equations for terminal stations T1 and T2 are given as:

$$P_{T1} = V_{T1}^2 \left[\frac{1}{R_{L13}} + \frac{1}{R_{L12}}\right] + V_{T1} \left[\frac{-V_{T3}}{R_{L13}} + \frac{V_{T2}}{R_{L12}}\right] \tag{2.4}$$

$$P_{T2} = V_{T2}^2 \left[\frac{1}{R_{L23}} + \frac{1}{R_{L12}}\right] + V_{T2} \left[\frac{-V_{T3}}{R_{L23}} + \frac{V_{T1}}{R_{L12}}\right] \tag{2.5}$$

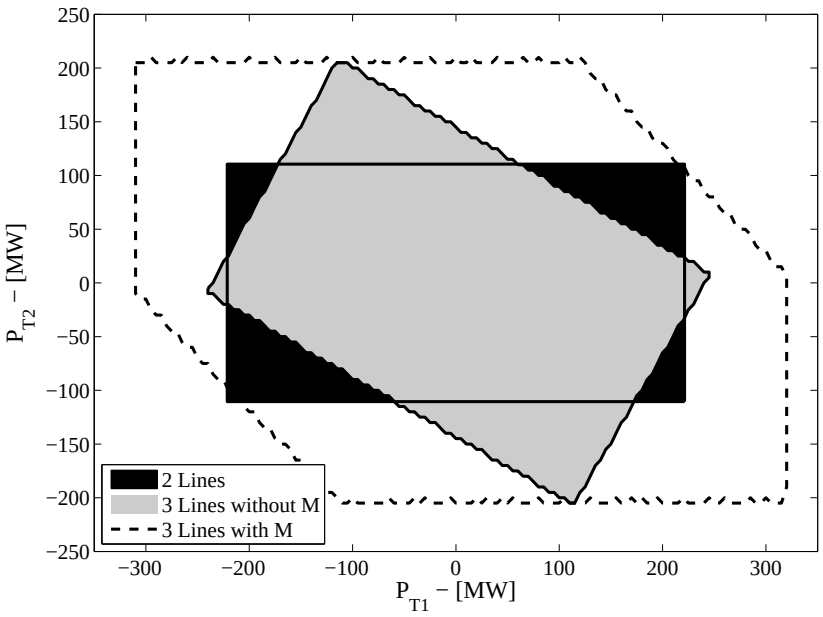


Figure 2.2: Region of operation for the 3-terminal HVDC grid.

The region in gray of Figure 2.2 is the operable region of the 3-line system. The figure also depicts in black the region of operation for the 3-terminal system with only two lines.

2.2 DC Power Flow Controller

2.2.1 Description

The dc power flow controller is conceived as a mean to change the voltage at the dc terminals of a VSC station by a ratio M. The dc power flow controller can be modeled either as an ideal converter ($P_{in} = P_{out}$) or as some kind of power injection device. In this chapter, the dc power flow controller is modeled as an ideal converter whose input is VSC terminal voltage V_{VSC} and whose output is dc line voltage V_{line}. The practical implementation is described in Chapter 3. The ratio M is the output-to-input voltage ratio of the ideal converter as given in Equation (2.6).

$$M = \frac{V_{line}}{V_{VSC}} \tag{2.6}$$

Among many requirements, the dc power flow controller has to be economical in order to be viable. It can be rated for only a fraction of the terminal converter ratings because line currents are very sensitive to voltage

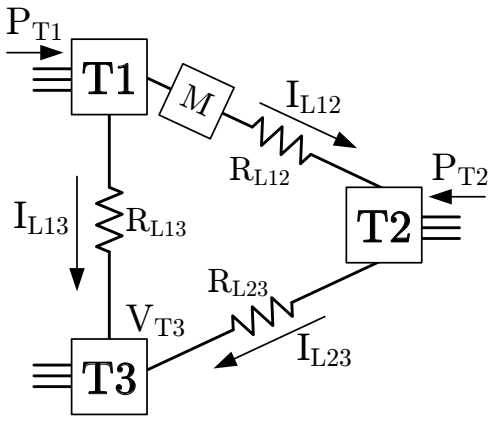
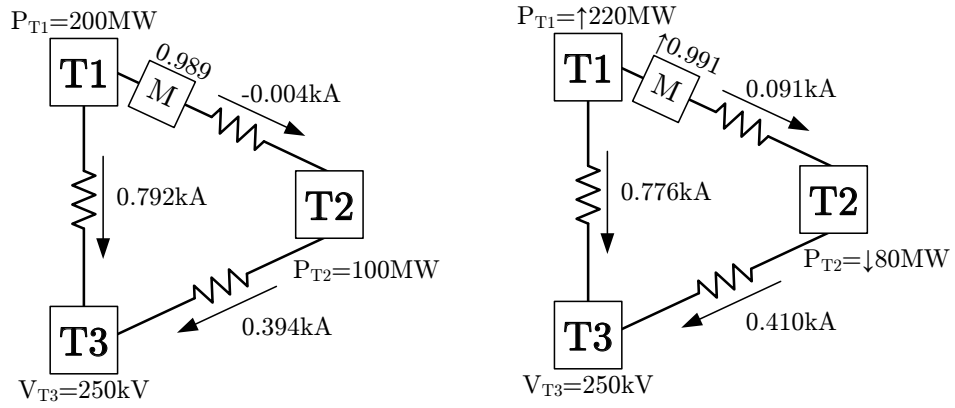


Figure 2.3: 3-terminal HVDC grid with a dc power flow controller M.



(a) With M=0.989, the operation is similar to the 2-line configuration.

(b) Variation in power injection.

Figure 2.4: Example of the interaction with dc power flow controller.

variations due to the low line resistances. Therefore, a variation of voltage of only 5%(±2.5%) is considered in this project.

2.2.2 Benefits

The 3-line system shown in Figure 2.1(b) is upgraded with a dc power flow controller "M" as illustrated in Figure 2.3. The ratio M is adjusted to force the HVDC grid to operate back with the same current values as with 2 lines (Figure 2.1(a)). A ratio of 0.989 makes the current in the link L12 almost zero, which reproduces the initial conditions. This situation is illustrated in Figure 2.4(a).

In the event that the wind farm (terminal station T2) production reduces to 80MW instead of 100MW, the terminal station T1 is able to increase its

power injection by 20MW to compensate the reduction. However, it is required that the 20MW of extra power is transmitted via the L12-L23 link and not L13 because line L12 is already at its nominal capacity. Then, the dc power flow controller is adjusted to 0.991 which forces the 20MW to flow via link L12-L23 as shown in Figure 2.4(b). More details about currents, voltages and powers for both scenarios are given in Table 2.2.

This simple example describes the operation and benefits of the inserted dc power flow controller on the HVDC grid. The extra contribution of 20MW by terminal station T1 might appear to be unrealistic for an already installed converter with established power ratings. However, in the vision of a future HVDC grid, it is most likely that a terminal station T1, for example, will branch out to many converters and several dc power flow controllers may be installed. In that case, the requirement of additional power controllability would be served.

2.2.3 Region of Operation

As expected, the restricted region enlarges with the addition of the dc power flow controller. The dc power flow controller is inserted in the HVDC grid on line L12 between terminal stations T1 and T2 as in Figure 2.3. The equation of the current in line L12 becomes,

$$I_{L12} = \frac{MV_{T1} - V_{T2}}{R_{L12}} \tag{2.7}$$

where M is the output-to-input ratio of the dc power flow controller. The system is solved by updating Equations (2.4) and (2.5) to:

$$P_{T1} = V_{T1}^2 \left[\frac{1}{R_{L13}} + \frac{M^2}{R_{L12}}\right] + V_{T1}\left[\frac{-V_{T3}}{R_{L13}} + \frac{MV_{T2}}{R_{L12}}\right] \tag{2.8}$$

$$P_{T2} = V_{T2}^2 \left[\frac{1}{R_{L23}} + \frac{1}{R_{L12}}\right] + V_{T2}\left[\frac{-V_{T3}}{R_{L23}} + \frac{MV_{T1}}{R_{L12}}\right] \tag{2.9}$$

The boundary of the region of operation is the dotted line in Figure 2.2. This illustrates that the insertion of the dc power flow controller indeed enlarges the area offering more options to transmit power. The increase is significant compared to the system without M; it increases by 112% for the four quadrants.

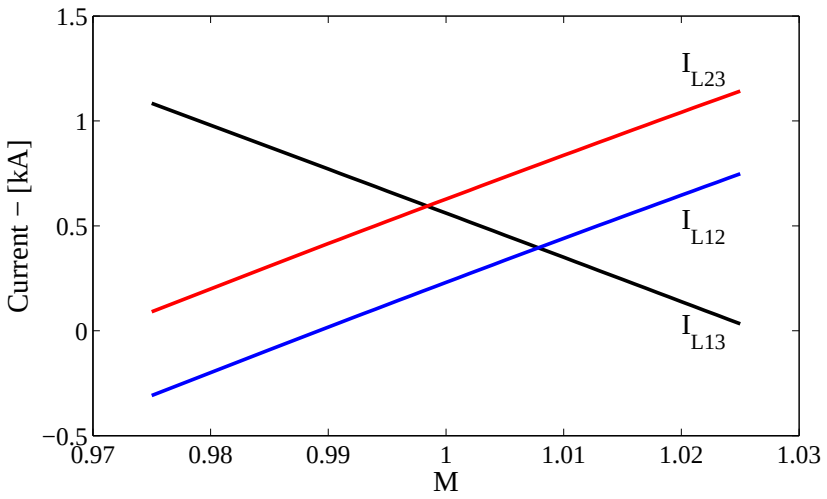


Figure 2.5: Line current variations with respect to M with P_{T1}=200MW and P_{T2}=100MW for the 3-terminal 3-line HVDC grid.

Although the dc power flow controller is installed on one line, variations of M produce changes to all three lines as shown in Figure 2.5. For the given P_{T1} and P_{T2}, 200MW and 100MW respectively, multiple operating points are possible depending on the value of M. Using Figure 2.5, if M is set to 0.975, transmission line L13 exceeds its current limits of 0.87kA. Therefore, by adjusting M to 0.99, all lines are within their respective boundaries. This means that for a given P_{T1} and P_{T2} there is a range of M where all line currents are within their respective constraints.

Under certain power injections (P_{T1} and P_{T2}), there are always one or multiple lines that exceed their limits regardless the range of M. The lines responsible for the limits of the region of operation are shown in Figure 2.6. The lines responsible for the boundary are identified and in the event of concurrent exceeding lines, an "×" is used.

2.2.4 Current Sensitivity

As stated previously, line currents are very sensitive to the ratio M. As shown in Figure 2.5, a variation of only 1% in the ratio M produces a change of around 20% in the three currents. More precisely, the current sensitivity can be calculated by doing the partial derivative of the current Equations (2.1), (2.2) and (2.7). The results are shown in Equations (2.10), (2.11) and (2.12).

$$\frac{\partial I_{L13}}{\partial M} = \frac{1}{R_{L13}} \frac{\partial V_{T1}}{\partial M} - \frac{1}{R_{L13}} \frac{\partial V_{T3}}{\partial M} \tag{2.10}$$

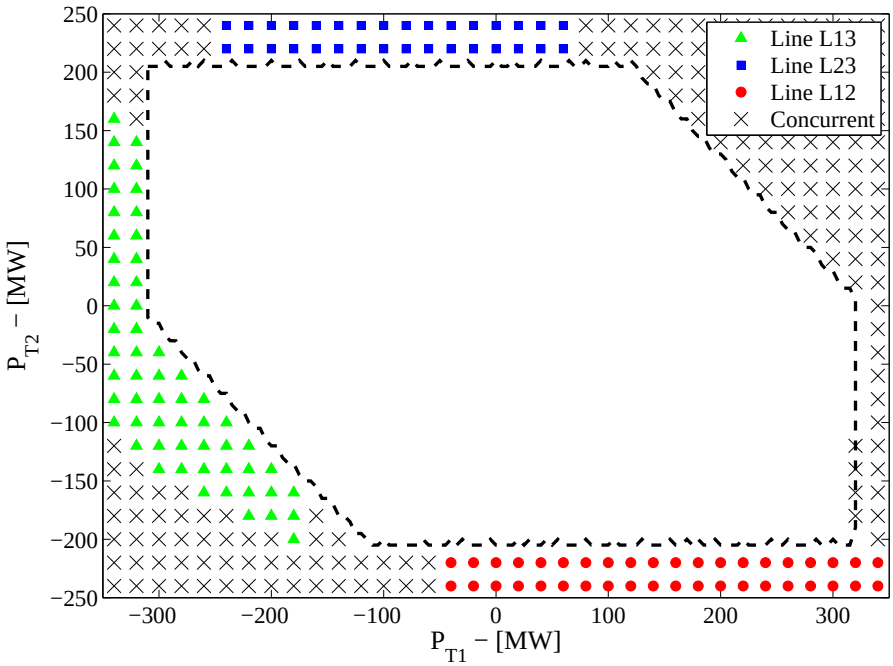


Figure 2.6: Boundary analysis: line limits for the 3-terminal 3-line HVDC grid.

$$\frac{\partial I_{L23}}{\partial M} = \frac{1}{R_{L23}}\frac{\partial V_{T2}}{\partial M} - \frac{1}{R_{L23}}\frac{\partial V_{T3}}{\partial M} \tag{2.11}$$

$$\frac{\partial I_{L12}}{\partial M} = \frac{M}{R_{L12}}\frac{\partial V_{T1}}{\partial M} - \frac{1}{R_{L12}}\frac{\partial V_{T2}}{\partial M} + \frac{V_{T1}}{R_{L12}} \tag{2.12}$$

Since the dc voltage of the voltage regulator terminal station, V_{T3}, is constant, its partial derivative with respect to M is zero $\left(\frac{\partial V_{T3}}{\partial M} = 0\right)$. The power equations of terminal stations T1 and T2, Equations (2.8) and (2.9), are used to find numerically the value of $\frac{\partial V_{T1}}{\partial M}$ and $\frac{\partial V_{T2}}{\partial M}$. Details about this approach are given in Section B.2.2 of Appendix B. Those calculations for P_{T1}=200MW and P_{T2}=100MW give a slope $\Delta I_L/\Delta$M around the operating point M=1 of $-21.03kA$, $21.03kA$ and $21.13kA$ for I_{L13}, I_{L23}, I_{L12} respectively. Those numbers also match the calculated slopes using the linear fitting curve of Figure 2.5. This analysis confirms the high sensitivity of the line currents with respect to the dc power flow controller. Therefore, it justifies the need of only a small voltage variation. It can be noted that the current change is almost linear. In the event where more degrees of freedom would be required, the addition of more modules can result in an increase of the possibilities.

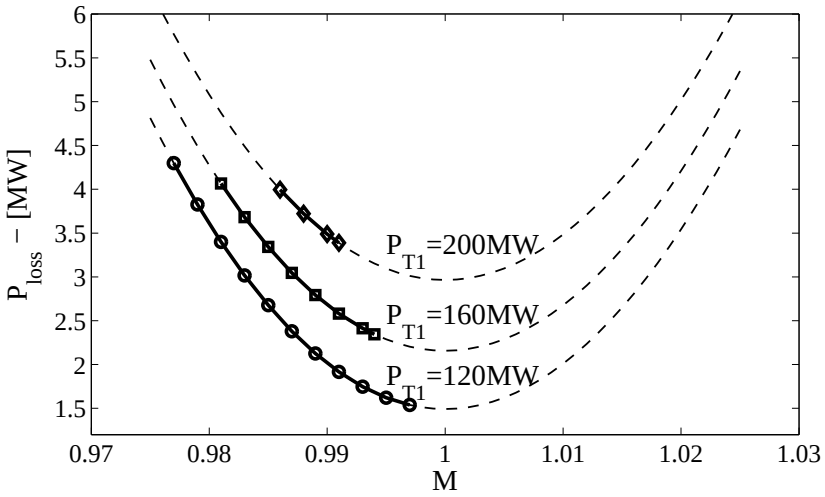


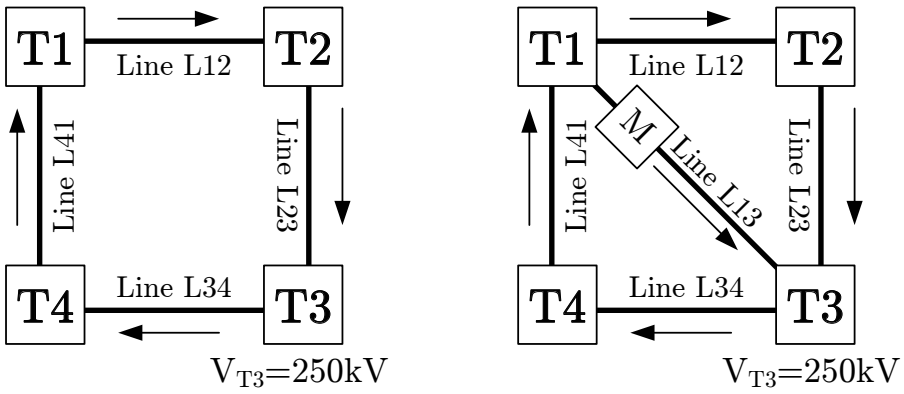
Figure 2.7: Transmission losses with respect to M for the 3-terminal 3-line HVDC grid with $P_{T2} = 100MW$.

2.2.5 Transmission Losses

Since the dc power flow controller changes the line currents, it also influences transmission losses. Figure 2.7 shows the transmission losses with respect to the ratio M for a fixed power injection from terminal station T2 with three different values for terminal station T1. It is expected that the lowest point is at M=1 (or when no dc power flow controller is inserted) since, from circuit theory, electrons naturally go through lowest resistance. However, because of transmission line limits, such operating point (M=1) might not always be possible. In Figure 2.7, the continuous lines with markers are the operable region. In all three cases, it is not possible to operate at minimal losses with M=1. Nevertheless, it is possible to adjust M in order to minimize the transmission losses but it seems to be a very limited application.

2.3 4-Terminal HVDC Grid

A similar analysis is performed to a HVDC grid with four terminal stations as suggested in [10]. The initial 4-terminal system is composed of four transmission lines system as shown in Figure 2.8(a). The scenario is described as three terminal stations (T1,T2,T4) supplying power to one voltage regulator point (T3). Terminal stations T1, T2 and T4 supply 100MW each which gives a total of 300MW injected to terminal station T3 (neglecting transmission losses). The results for that scenario are given in Table 2.4. The line current capacities



(a) 4-Line HVDC grid. (b) 5-Line HVDC grid.

Figure 2.8: MTDC grid configurations with 4 terminal stations.

Table 2.3: 4-Terminals - transmission line parameters.

Transmission Line	**Distance** [km]	**Resistance** [Ω]	**Current Limits** [kA]
L12	248	3	0.25
L23	165	2	0.7
L34	165	2	0.6
L41	413	5	0.2
L13	248	3	0.5

are listed Table 2.3. Details and references about the transmission line models are found in Section C.3 of Appendix C.

A fifth line with a dc power flow controller is added to the HVDC grid between terminal stations T1 and T3 as shown in Figure 2.8(b). By adjusting the ratio M to 1.002, it is possible to divert almost all the current injected by terminal station T1 to line L13. Results are shown in Table 2.4. The set of equation for calculation about this system is given in Section B.3 of Appendix B.

In this section, only the region of operation and the current sensitivity are analyzed due to the increase of complexity generated by the augmented grid size.

Table 2.4: 4-Terminals - scenarios.

	4-Line Fig. 2.8(a)	**5-Line no M**	**5-Line with M** Fig. 2.8(b)
P_{T1} [MW]	100	100	100
P_{T2} [MW]	100	100	100
P_{T4} [MW]	100	100	100
V_{T3} [kV]	250	250	250
M	-	-	1.002
V_{T1} [kV]	252.0	251.6	250.7
V_{T2} [kV]	251.3	251.11	250.8
V_{T4} [kV]	251.1	250.9	250.8
I_{L12} [kA]	0.23	0.04	-0.01
I_{L23} [kA]	0.63	0.44	0.39
I_{L34} [kA]	-0.56	-0.43	-0.39
I_{L41} [kA]	-0.17	-0.03	0.01
I_{L13} [kA]	-	0.33	0.42

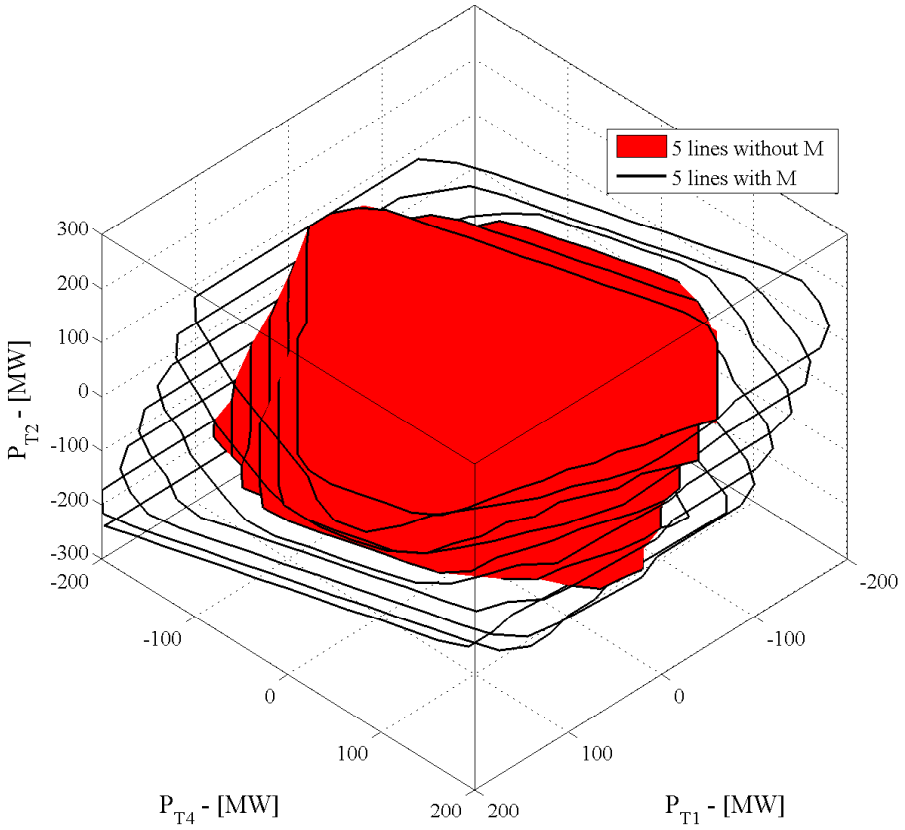


Figure 2.9: Region of operation for the 4-terminal HVDC grid with five lines. The inside volume is without dc power flow controller M and the expanded volume is with the controller.

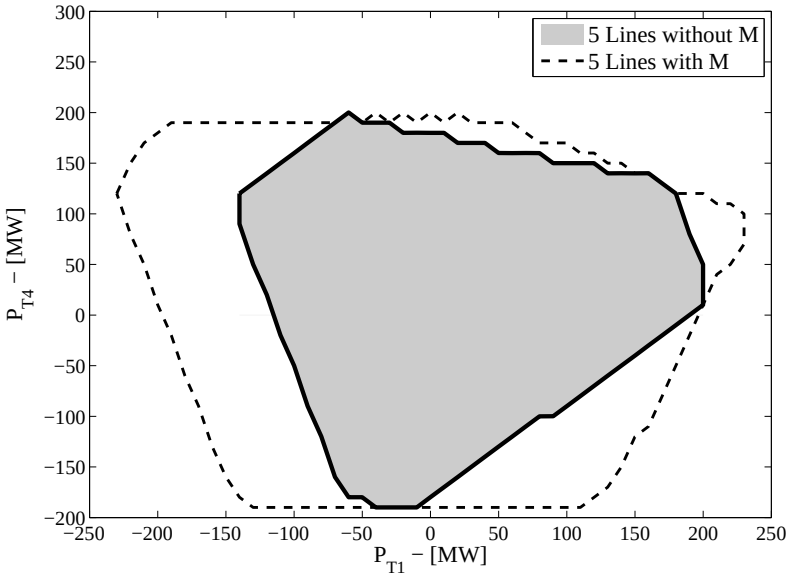


Figure 2.10: Region of operation with P_{T2}=100MW.

2.3.1 Region of Operation

Using the same procedure as for the 3-terminal HVDC grid, the region of operation is calculated for a HVDC grid composed of four terminal stations and five transmission lines for two cases: with and without the dc power flow controller on line L13 at terminal station T1. Since the set of points is composed of three variables (P_{T1},P_{T2},P_{T4}), it is natural to represent the region of operation in terms of volume as shown in Figure 2.9. The inside volume is the 5-line system without the dc power flow controller and the contour lines shows the operating region with it. It is clear that the volume has expanded. A slice of the volume for P_{T2}=100MW is shown in Figure 2.10. The area is larger but not significantly in the first quadrant (positive P_{T1} and P_{T4}). This situation can be possibly explain by not having the dc power flow controller at the optimal location in the HVDC grid. Nevertheless, the insertion of the dc power flow controller improves the operability over the four quadrants.

2.3.2 Current Sensitivity

Current sensitivities are calculated using partial derivatives of line current equations as described in Section B.3.2 of Appendix B. The slopes give an insight about how the current changes in their respective transmission line with respect to the ratio M. The calculated slopes $\Delta I_L/\Delta$M for P_{T1}=100MW,

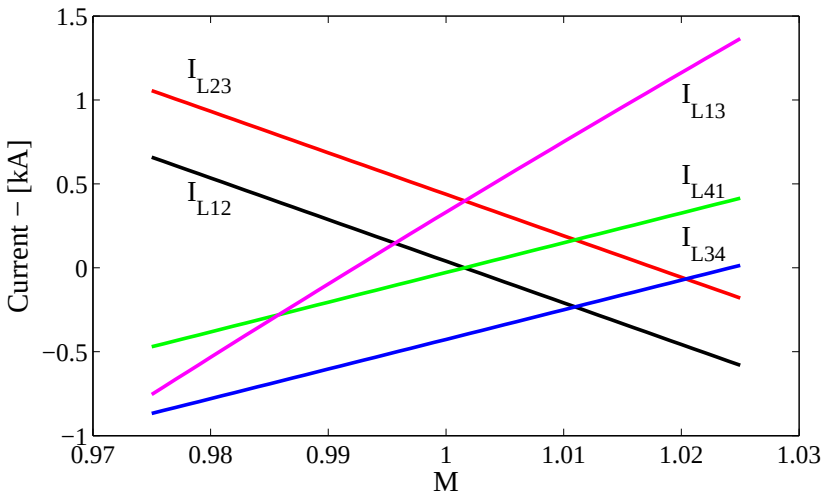


Figure 2.11: Current variations with respect to M with P_{T1}=100MW, P_{T2}=100MW and P_{T4}=100MW for the 4-terminal 5-line HVDC grid

P_{T2}=100MW and P_{T4}=100MW around the operating point M=1 are -24.8kA, -24.7kA, 17.7kA, 17.7kA and 42.4kA for I_{L12}, I_{L23}, I_{L34}, I_{L41} and I_{L13} respectively. Those results agree with slopes extracted from Figure 2.11. As M increases, I_{L12} and I_{L23} decreases while the others increases. Even though they are not exactly parallel, it is interesting to note that I_{L12} and I_{L23} have almost the same current sensitivity. This observation also applies to the pair I_{L34} and I_{L41}.

2.4 Chapter Summary

This chapter has investigated the use of a dc power flow controller in a MTDC grid to evaluate its benefits on the power flow distribution. Using two different scenarios, it has been shown that a wider range of power can be transmitted within defined transmission line limits. The first scenario consists of a 3-terminal grid with three transmission lines. It is a simple example that illustrates the operation of the HVDC grid and the benefits of the dc power flow controller. The second HVDC grid is larger with four terminal stations and five transmission lines. The region of operation is shown using a volume figure.

Chapter 3

DC Power Flow Controller: Hardware Realization and Implementation

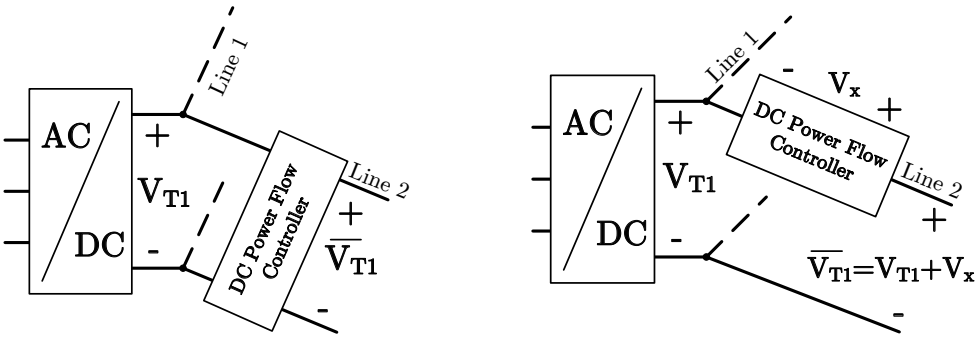
In the previous chapter, it has been shown that the domain of power flow controllability is enlarged by dc power flow controllers. The next step is to develop the hardware realization. This chapter presents the circuitry, controls and simulations as proof of principle.

The possible forms of dc power flow controller are examined. From the examination, a thyristor-based controller is adopted for implementation. Simulation results are obtained to evaluate the performance of such dc power flow controller.

3.1 Configuration

In designing a dc power flow controller, one looks to Flexible AC Transmission System (FACTS) for guidance. In general, controllers of FACTS derive their flexibility by managing reactive powers. But there is no reactive power in the HVDC grid to manage. Therefore, the dc power flow controller must manage by inverting (or rectifying) active real power to (or from) the ac-side. This does not affect the efficiency (except for ohmic losses in the components) because the rectified (or inverted) ac power is taken from (or returned) to the ac-side.

The dc power flow controller is treated as an appendage of a VSC-HVDC station. The VSC-HVDC provides the dc voltage lift, for example to $V_{T1} =$



(a) Shunt controller. (b) Series controller.

Figure 3.1: DC Power Flow Controller: (a) shunt; and (b) series.

$250kV_{\mathrm{DC}}$, and the dc power flow controller provides a continuous variation within 5%(±2.5%), so that the range of controllable dc voltage in the example is $244kV \leq \overline{V_{T1}} \leq 256kV$. As shown in the previous chapter, the dc transmission line resistance is low, therefore, a small change in the dc voltage generates a significant dc current variation. Two types of connection are possible for such controller: shunt connected, shown in Figure 3.1(a), and series connected, shown in Figure 3.1(b).

3.1.1 Shunt Connected

The shunt controller in Figure 3.1(a) is essentially a dc-dc transformer with input/output voltages bearing the relation:

$$\overline{V_{T1}} = MV_{T1} \tag{3.1}$$

where M is the voltage transformer ratio as defined in the previous chapter.

DC-DC transformers are widely used in low power electronics. A recent proposal for high power applications is based on resonant converters [66]. However, the design of [66] is to step-up voltages from 22kV to 250kV. In dc power flow controller application, the desired voltage step-up ratio is of the order of M=0.975 to 1.025. Therefore, the design of [66] has not been pursued for this application.

Another objection is that $\overline{V_{T1}}$, the voltage output of the controller, must be rated at around dc line voltage. As line current is also around 1pu, the MVA rating of the shunt controller is of the order of 100% and not 5%.

3.1.2 Series Connected

As illustrated by Figure 3.1(b), the series connected DC Transmission Controller adds V_X to V_{T1}:

$$\overline{V_{T1}} = V_{T1} + V_X \tag{3.2}$$

Equation (3.2) can be mapped to a similar ratio by defining M as:

$$M = 1 + \frac{V_X}{V_{T1}} \tag{3.3}$$

and it can be used in the form as defined in the previous chapter.

As the controller which produces V_X is series connected, it is necessary to choose a current source converter. As thyristor converters belong to the current source family and it has a long history of reliable operation, this work adopts it although it seems out of place in the MTDC with VSC-HVDC system.

Many series connected HVDC-taps of point-to-point thyristor HVDC have been proposed and they take advantage of transformer insulation to provide galvanic isolation so that the rating of the thyristor bridge is required to withstand the low voltage of V_X only [67–71]. The thyristors have to withstand the full dc current including during fault events.

3.2 Thyristor Power Flow Controller

Figure 3.2 shows the block diagram of the thyristor power flow controller (as a part of a VSC-HVDC station) inserted in series in a dc transmission line of the MTDC grid. To ensure bidirectional current flow, the thyristor power flow controller is made up of two 6-pulse thyristor converters connected in a dual-converter configuration [72]. For a given direction of dc current flow, each converter has the capability to inject positive or negative dc voltage V_X by operating either as a rectifier or as an inverter. The thyristor power flow controller has, therefore, 4-quadrant operation. Both converters are connected by 3-phase ac lines, through 3-phase transformer, to the ac inputs of the VSC.

As mentioned in Section 3.1.2, the galvanic isolation of the high dc voltage from the ac system is provided by the insulation of the transformers. The thyristor power flow controller is considered to be an auxiliary module of the VSC of the MTDC system. In varying V_X to control the dc power flow of the line, ac power is rectified or inverted. This ac active power is part of the same

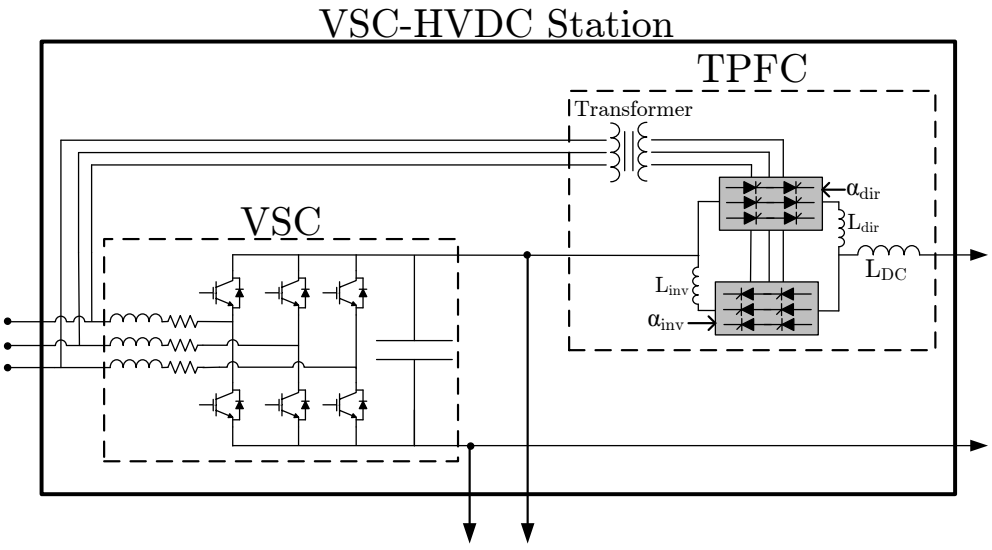


Figure 3.2: Thyristor power flow controller (TPFC) as an auxiliary controller of VSC-HVDC station.

ac power input of the overall VSC-HVDC station.

Thyristor-bridges produce a significant amount of harmonics on the ac side [14]. The overall ac harmonics produced by the thyristor power flow controller at the point of common coupling will not be severe because its power rating is only 5% of the rating of the VSC-HVDC station. Harmonic content is discussed and evaluated in simulation test 6 in Section 3.5.6.

3.3 3-Terminal HVDC Grid

3.3.1 Description of MTDC Grid

In the interest of gaining insights, the HVDC grid chosen for study is small: a 3-terminal stations VSC-HVDC grid shown in Figure 3.3. The dc voltage of the HVDC grid is referenced from terminal station T3 which operates as a dc voltage regulator to maintain a constant dc voltage of 250kV across its nodes. Terminal station T3 is the dc power slack bus and it ensures that dc power balance is maintained in the HVDC grid. The voltages of the other nodes depend on Ohm's Law, being different by the $I \times R$ voltage drops across the resistances R of the dc lines. Terminal stations T1 and T2 are operated as active power dispatchers. Each injects a regulated dc power determined by its reference setting P^{ref}. In addition, terminal station T1 has the thyristor

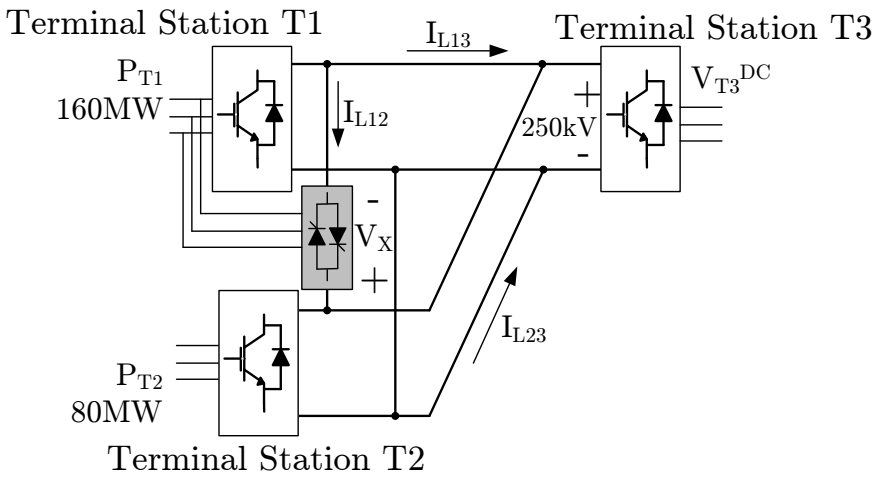


Figure 3.3: Multiterminal HVDC formed from 3 VSC terminal stations.

Table 3.1: System parameters.

DC Cable Parameters	Line L13	Line L23	Line L12
Distance [km]	248	83	165
Resistance [Ω]	3	1	2
Inductance [mH]	26.2	8.8	17.4
VSC Parameters	VSC T1	VSC T2	VSC T3
AC Voltage [kV]	83	83	83
AC Frequency [Hz]	50	50	50
DC Capacitor [mF]	0.2	0.2	0.4
Switching Frequency [kHz]	1.5	1.5	1.5
Thyristor Power Flow Controller			
DC inductance L_{DC} [mH]			100
DC inductance $L_{\text{dir}}, L_{\text{inv}}$ [mH]			50

power flow controller to inject V_X in line L12. For simulation tests, the transmission line parameters are given in Table 3.1. Details and references about the transmission line model can be found in Section C.3 of Appendix C.

3.3.2 Preliminary Design to Rate Thyristor Power Flow Controller

The design of the thyristor power flow controller requires computation of the voltages V_{T1}, V_{T2} and V_{T3} of terminal stations T1, T2 and T3 and the dc currents of lines L12, L13 and L23. The rated power for terminal stations T1 and T2 are chosen to be 160MW and 80MW, respectively. The thyristor

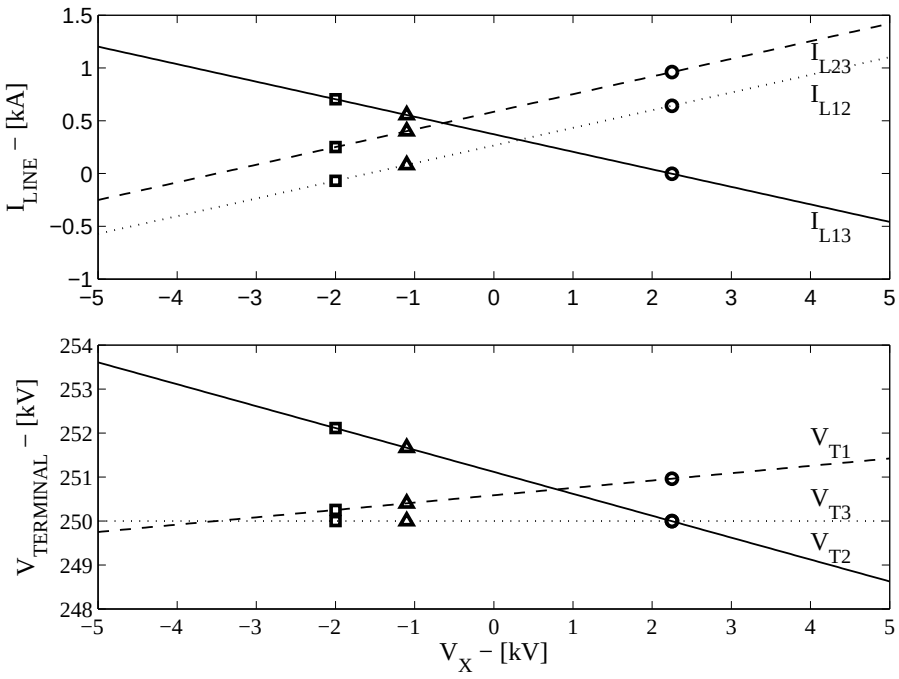


Figure 3.4: Line currents-vs-V_X and Node voltages-vs-V_X for $P_{T1} = 160$MW and $P_{T2} = 80$MW

power flow controller is designed to inject a voltage which varies from -5kV to +5kV. Using the same algorithm described in Appendix B, the computed line currents and the terminal dc voltages are shown in Figure 3.4. As V_X increases, a portion of current in the line L13 is redirected to terminal station T3 via the route L12-L23. The largest current which flows in line L12 is 1.1kA when V_X=+5kV. Therefore, each converter of the thyristor power flow controller should be rated for 5.5MW. The dual-converters require 11.0MW which is less than 7% of the 160MW rated converter of terminal station T1. The maximum current rating is 1.1kA.

3.4 Implementation of Control

As the thyristor power flow controller of Figure 3.2 is tested and evaluated in the MTDC system of Figure 3.3, it is necessary to describe briefly the controls of the VSC station and the thyristor power flow controller.

Table 3.2: Mode of operation of converters.

	d-axis controller	**q-axis controller**
VSC T1 (rectifier)	Power	Reactive current
VSC T2 (rectifier)	Power	Reactive current
VSC T3 (inverter)	DC voltage 250kV	Reactive current
TPFC	Current Control	

3.4.1 Voltage Source Converter (VSC) Station

The operation of VSC is well known and the dq-controller approach is used in this thesis. The VSC model and the control structure are described in Section C.1 of Appendix C. Detailed parameters of the VSC used in this chapter are given in Section C.4 but the main parameters are listed in Table 3.1.

The modes of operation of the VSCs are summarized in Table 3.2. Terminal stations T1 and T2 are under constant active power control and terminal station T3 is in dc voltage regulator mode. The setting of q-axis current control is i_q^{ref}=0.0 for all VSCs.

3.4.2 Operation of Thyristor Power Flow Controller

The thyristor power flow controller is composed of two thyristor-bridges that are connected back-to-back as shown in Figure 3.5. Each bridge allows only unidirectional dc current flow [14, 72]. Its dc output voltage V_d can be positive or negative depending on the firing angle α_1 in the equation:

$$V_d = \frac{3\sqrt{2}}{\pi} V_{ac} \cos(\alpha_1) \tag{3.4}$$

where V_{ac} is the rms value of the line-to-line voltage from the transformer. Figure 3.6 shows V_d as a function of α_1 under the label "direct". For $0 \leq \alpha_1 \leq 90°$, V_d is positive and the converter is rectifying. $90° \leq \alpha_1 \leq 180°$, V_d is negative and the converter is inverting. Each bridge is capable of only 2-quadrant operation.

A second converter is required to enable the dc current to flow in the opposite direction. The V_d-vs-α_1 relationship of the second converter is labeled "in-

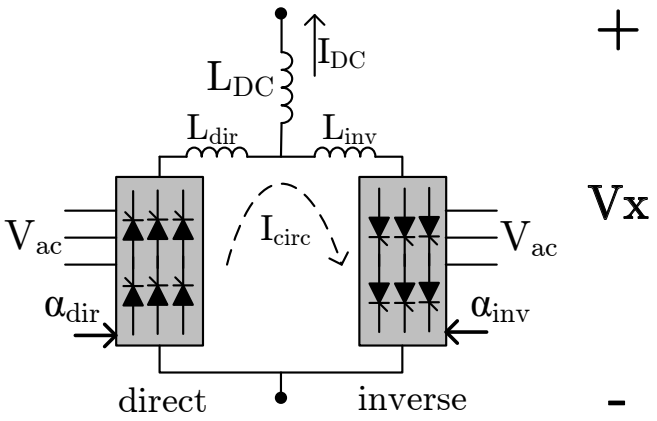


Figure 3.5: DC power flow controller: thyristor-based dual-converter.

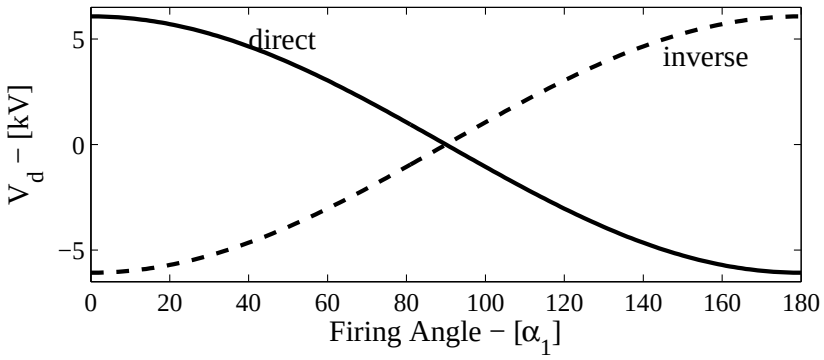


Figure 3.6: Relationship between voltage and firing angle.

verse" in Figure 3.6. With both converters, the thyristor power flow controller enables 4-quadrant operation. V_X is taken from V_d ("direct" or "inverse") depending on the direction of dc current flow.

The controller consists of a single branch where the direct output is α_{dir} and α_{inv} is calculated using Equation (3.5).

$$\alpha_{\text{dir}} + \alpha_{\text{inv}} = 180^{\circ} \tag{3.5}$$

By satisfying Equation (3.5), both converters generate the same dc voltage which allows the dc current to flow in either direction [72]. However, only one converter is in operation at any time instant because the other converter is blocked by the direction of current flow. The only instance when both converters operate at the same time is when the dc current changes direction, passing from one polarity to the opposite direction. During this transition, there must be dc reactors to limit the circulating current. The region of con-

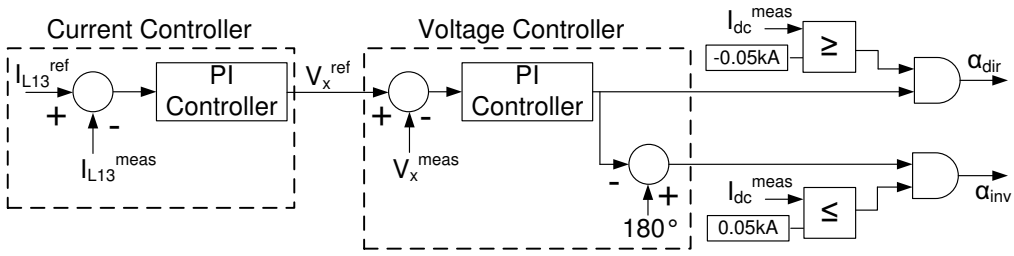


Figure 3.7: Thyristor power flow controller control diagram.

current operation is selected to be when the dc current is between -0.05kA and +0.05kA.

The block diagram of Figure 3.7 describes the implementation of the control. The starting point is the reference setting of the current in the line L13. The thyristor power flow controller is installed on the secondary dc line L12 to minimize the risk of interruptions of the principal link L13. The controller is implemented such that the thyristor power flow controller regulates its voltage injection and as a result maintain the current in the line L13 at the reference setting. The implementation consists of two sections: the first section is a feedback loop to produce the desired injected voltage V_X^{ref}. The second section produces the firing angle α_{dir} and α_{inv}. Comparison with the limits -0.05kA and +0.05kA and logic elements are used to identify the current direction ("direct" or "inverse") as well as the concurrent region of operation. The inner-loop is the voltage controller and the outer-loop is the current controller. The complete details about the model and the controllers are given in Section C.4 of Appendix C

3.5 Simulation Results

The validation tests on the thyristor power flow controller are done by simulation using PSCAD-EMTDC software package, an industry-grade software for high voltage power electronic research. Because the major interest is on the performance on the dc-side, the ac systems are modeled as infinite buses in tests 1 to 5. The viability of the system when the ac systems are more fully modeled is reported in test 6. The simulation test 6 consists of a simulation with a weak ac-side system.

Table 3.3: Simulation Test 1.

	Theoretical	PSCAD Results (Fig. 3.8)	
	(Fig. 3.4)	mean	ripple (peak-peak)
V_{T1} [kV]	252.1	252.1	0.77
V_{T2} [kV]	250.3	250.3	0.39
V_{T3} [kV]	250.0	250.0	0.57
V_X [kV]	-2.0	-2.0	1.15
I_{L13} [kA]	0.704	0.704	0.002
I_{L23} [kA]	0.250	0.250	0.002
I_{L12} [kA]	-0.069	-0.070	0.01

3.5.1 Simulation Test 1 - Steady-State Operation

The benchmark on the steady-state operation test is the set of predictions obtained from the analysis shown in Figure 3.4 and identified by the square markers. Table 3.3 summarizes (i) the very good agreement between the mean of the simulated steady-state waveforms in Figure 3.8 with the square marker predictions in Figure 3.4 and (ii) the peak-to-peak values of the voltages and currents.

In this test, the injected power for terminal stations T1 and T2 are 160MW and 80MW, respectively. The thyristor power flow controller operates from a voltage reference V_X^{ref}=-2kV so as to conform to the conditions of Figure 3.4.

The context of the operating conditions can be viewed as: currents-order of 0.7kA in line L13, voltages-order of 250kV. The 6th harmonic in the current of line L12 is very noticeable but it is because the mean current is only around -0.07kA and the scale of the y-axis. Figure 3.9 is presented to show that the injected voltage, whose mean is 2kV, has a large ripple. But the voltage ripples is dwarfed by the large 250kV voltage rating of the MTDC.

As such the Total Harmonic Distortion (THD) standards in currents and voltages are easily satisfied. The definition of THD in percent for an ac-system is given as [41]:

$$THD = \sqrt{\sum_{h \neq 1} \left(\frac{y_h}{y_1} \right)^2} \times 100 \tag{3.6}$$

where y_1 is the fundamental component of the signal. For THD evaluation of dc signal, the fundamental component used is the dc component.

Figure 3.10 identifies the three currents of terminal station T1 on its ac-side. The THD for the thyristor power flow controller (i_{TPFC}) relative to

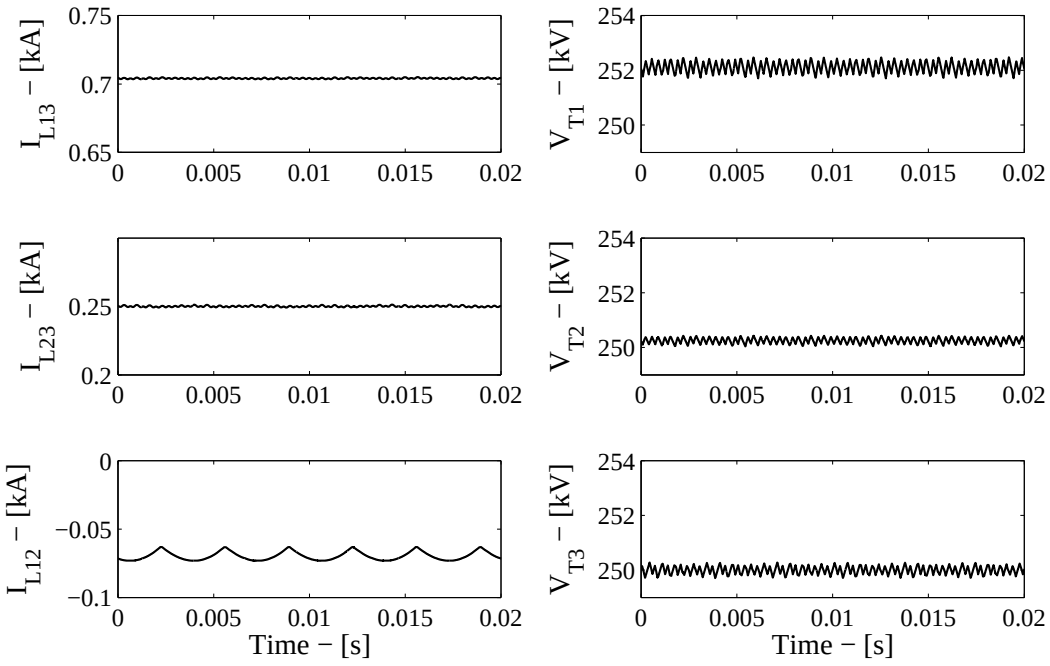


Figure 3.8: Simulation Test 1 results: dc line currents and terminal voltages.

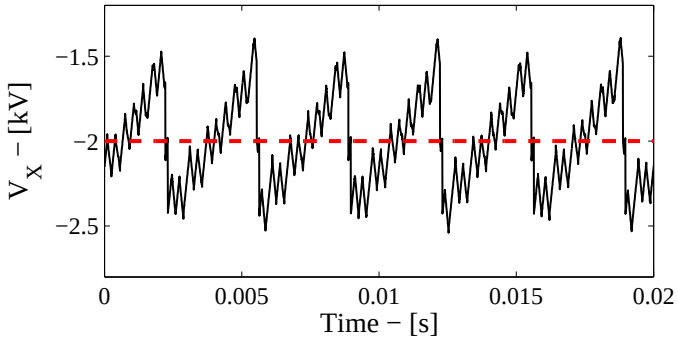


Figure 3.9: Simulation Test 1 results: thyristor power flow controller voltage.

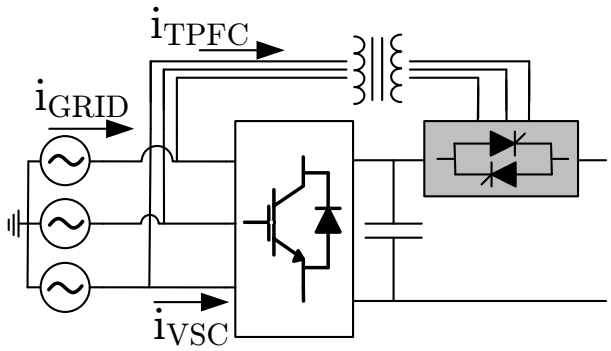


Figure 3.10: Terminal station T1 ac-side arrangement.

the fundamental ac current at the point of common coupling from the source branch (i_{GRID}) is 0.08%. For the dc voltages, the largest harmonics come from the thyristor power flow controller with 6^{th} and 12^{th} harmonic injection. Even though, the THD of the dc voltage on line L12 is 0.08%. As mentioned, the injection voltage is small compared to the operating dc voltage of the MTDC.

The results of this test show that: (i) the power injected by the thyristor power flow controller is 0.14MW and therefore only a small fraction of the power rating of terminal station T1; (ii) although the thyristor power flow controller has large voltage ripples, the THDs are satisfied because of its fractional size.

3.5.2 Simulation Test 2 - Stability Test by Step change in P1

The step change is a small-signal stability test of the thyristor power flow controller. The thyristor power flow controller operates with only the voltage controller. The step change consists of 10% increase of the injected power from terminal station T1 at $t = 0.2$s. Before the step change, $\text{P}_{\text{T1}}^{\text{ref}}$=150MW, $\text{P}_{\text{T2}}^{\text{ref}}$=80MW and the voltage reference of the thyristor power flow controller is $\text{V}_{\text{X}}^{\text{ref}} = -2kV$. The simulation test results for $t \leq 0.2$s in Figure 3.11, show the line currents and the nodal voltages. The line currents distribution are determined by the setting of $\text{V}_{\text{X}}^{\text{ref}} = -2kV$. In particular, the current in line L12 is negative.

At $t = 0.2$s, a step change is introduced to the active power reference setting of terminal station T1 from $\text{P}_{\text{T1}}^{\text{ref}}$=150MW to $\text{P}_{\text{T1}}^{\text{ref}}$=165MW. All other reference settings are held constant. The simulation results for $t \geq 0.2$s in

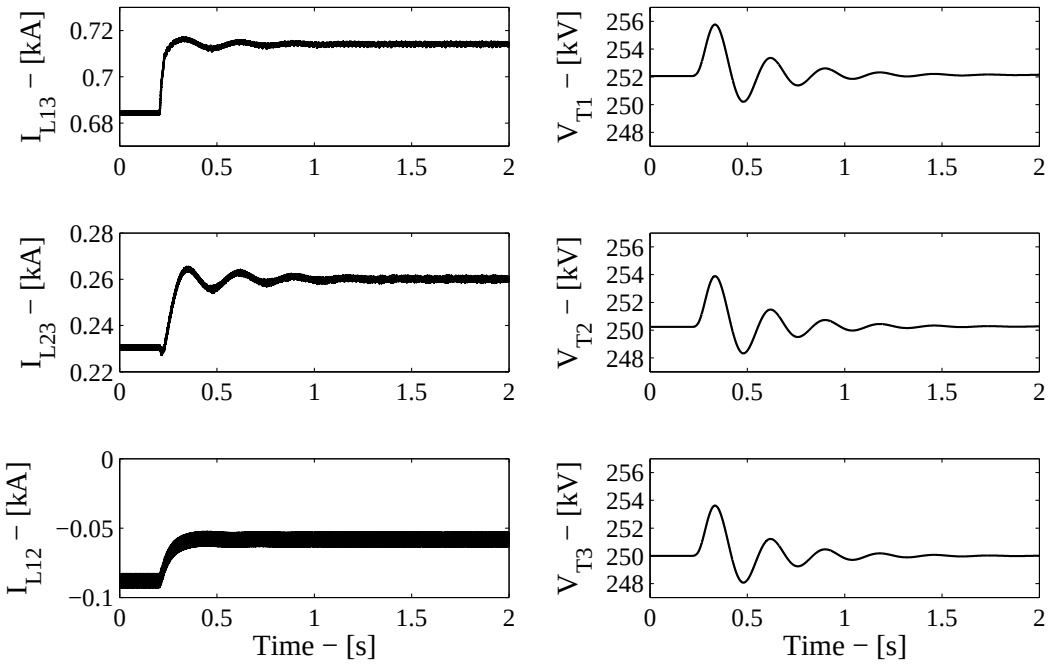


Figure 3.11: Simulation Test 2 results: dc line currents and terminal voltages.

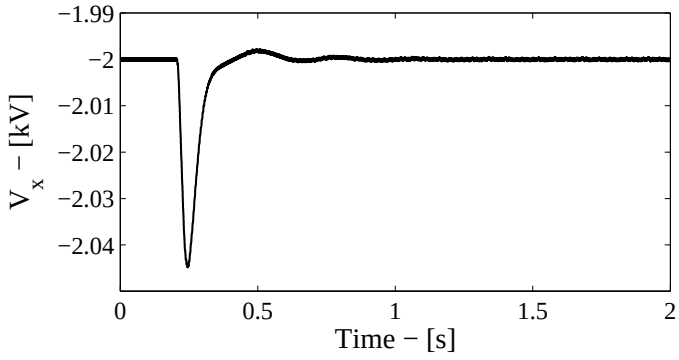


Figure 3.12: Simulation Test 2 results: Thyristor power flow controller voltage.

Figure 3.11 show that the system is stable. The voltages and currents settle to steady-state solutions which can be determined by dc load flow studies of Appendix B. The transient for the dc line currents has duration of 0.6s with low overshoot. It is interesting to note that the terminal voltages for the three terminal stations follow the transient of the voltage regulator (V_{T3}). The overshoot for the voltage regulator is 1.6% with a settling time of 1 second. From the point of view of terminal station T3, the power changes from 230MW to 245MW which represents an increase of 6.5%.

The injected voltage by the thyristor power flow controller is shown in Figure 3.12. The thyristor power flow controller has a feedback loop in which V_X is measured and compared with $\mathrm{V_X^{ref}}$. As in feedback systems, its voltage droop is a consequence of the differential equations. For the purpose of this test, it is heartening that the overvoltages in V_X and the dc voltages of the VSC stations are within the tolerance of the solid-state switches.

3.5.3 Simulation Test 3 - Bidirectional Operation with Line Current Regulator

The current controller is introduced in the control of the thyristor power flow controller (see Figure 3.7). The reference current for the line L13 is set to 0.55kA. Therefore, the module controller should adjust the injected voltage, V_X, on line L12 in order to ensure that the current in line L13 remains at 0.55kA. The simulation is arranged such that initially 160MW of power is injected at terminal station T1. Under this condition, the VSC at terminal station T1 injects 0.64kA where 0.55kA flows through line L13 and 0.09kA is "exported" through line L12. In order to do so, the thyristor power flow controller has to inject -1.1kV to maintain those line currents as calculated and identified in Figure 3.4 with circle markers.

Then, the injected power from terminal station T1 decreases from 160MW to 100MW over a 2 seconds period. As a consequence, the current going out of the VSC of terminal station T1 is 0.4kA. In order to fulfill the requirements of 0.55kA on line L13, the thyristor power flow controller has to allow reverse current direction. During this transition, the current flowing through the thyristor power flow controller goes from 0.08kA to -0.15kA. This simulation demonstrates bidirectional operation. The results are shown in Figure 3.13 for the terminal voltages and the line currents.

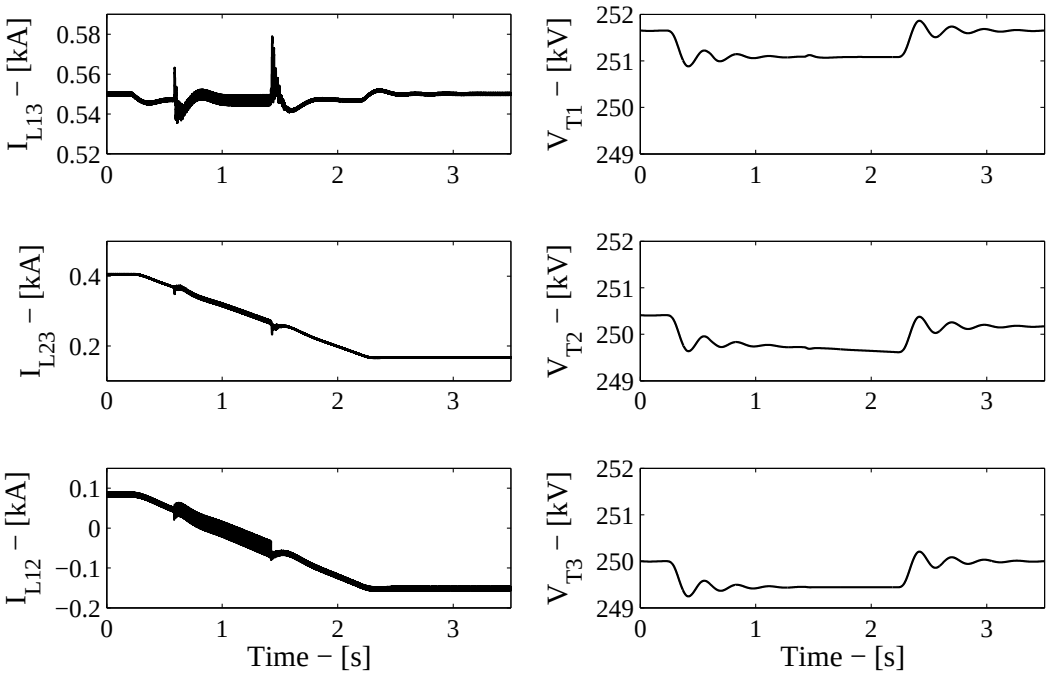


Figure 3.13: Simulation Test 3 results: dc line currents and terminal voltages.

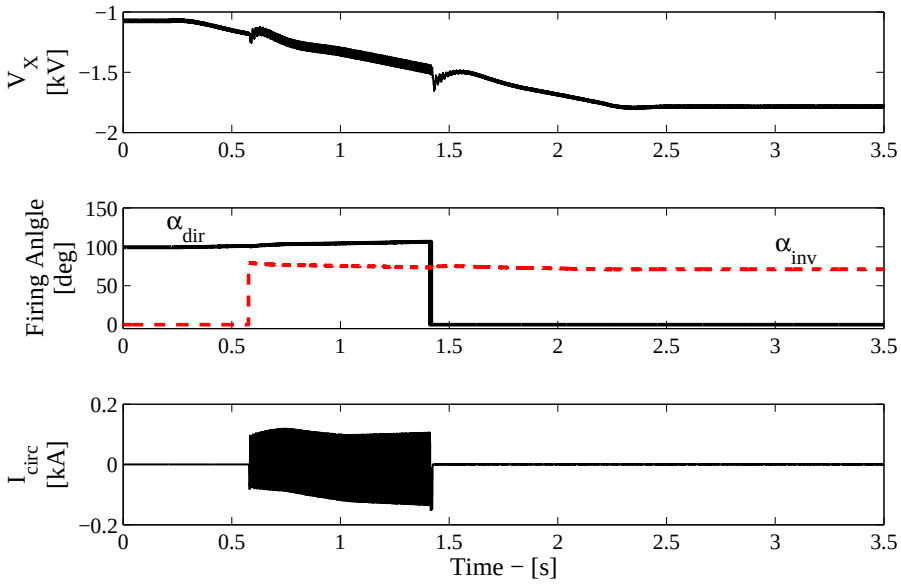


Figure 3.14: Simulation Test 3 results: thyristor power flow controller voltage, current and firing angle.

The current in line L12 decreases and at 0.58s the thyristor power flow controller enters in dual mode with circulating current. The overlap of the firing angles is shown in Figure 3.14. During that period, both 6-pulse bridges operate simultaneous. The magnitude of the circulating current is ±0.2kA which is within thyristor current ratings. During the transition the voltage reference decreases to 249.4kV and as soon as the injected power P_{T1} is stabilized, the voltage is back to 250kV within 1s.

This simulation explores the functionality of the current controller as well as the bidirectional operation of the thyristor power flow controller. During the transition period, the circulating current is observed. Its amplitude is limited by dc reactors in each branch and it remains within tolerable boundaries.

3.5.4 Simulation Test 4 - Terminal Station Loss with Line Current Regulator

This scenario is an abrupt shut down of the VSC at terminal station T2. The thyristor power flow controller is implemented with the line current regulator. At 0.2s, ac breakers at terminal station T2 opens and the firing pulses of the VSC are blocked. From that point on, no energy conversion is performed at terminal station T2 but the converter remains connected on the dc side with the HVDC grid. No dc breaker nor disconnect switch are used in this simulation.

As shown in Figure 3.15, large oscillations are produced on the line L23 from 0.2s to 0.6s. However, those oscillations remain positive. The reference terminal voltage drops from 250kV to 230kV but regulates back within 0.6sec and the overvoltage created by the recovery process is only of 4%. At terminal station T3, this perturbation is a variation in the incoming power from 240MW to 160MW which represents a loss of 33%. At 0.8s, the HVDC grid is back in normal operation with only two converters. The current in line L13 is regulated at 0.55kA and the link L12-L23 remains operational despite the fact that terminal station T2 is out of service.

Figure 3.16 shows the voltage reference generated by the current controller, V_X^{ref}, and how it influences the firing angle α_{dir}. The behaviour of the MTDC under the loss of one terminal station has been demonstrated in this simulation. The HVDC grid remains stable and recovers from this perturbation.

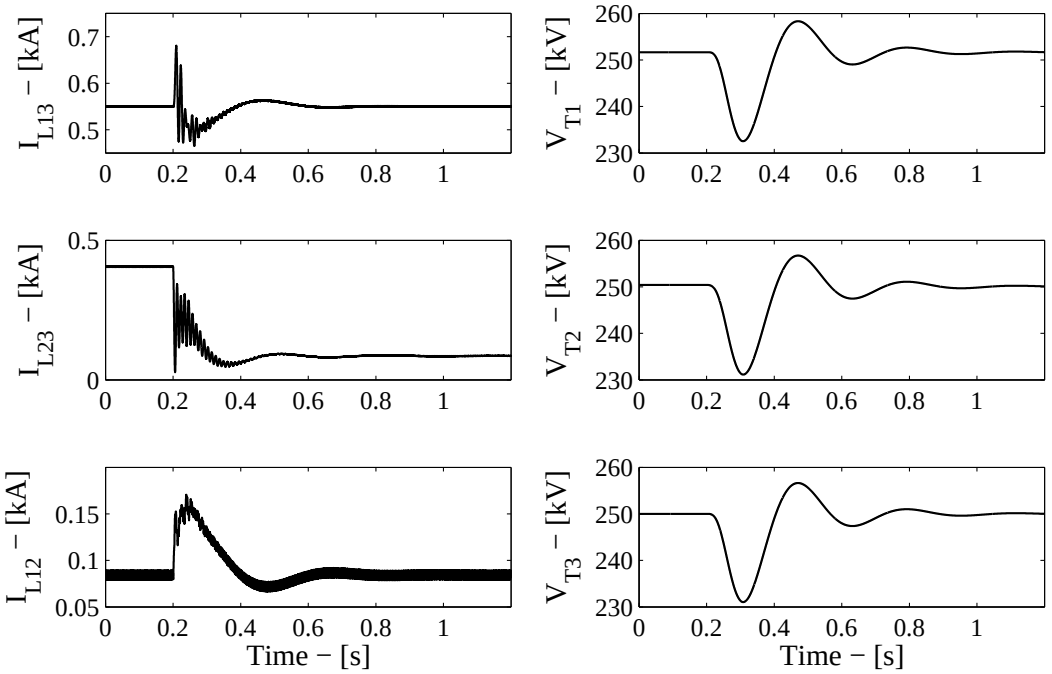


Figure 3.15: Simulation Test 4 results: dc line currents and terminal voltages.

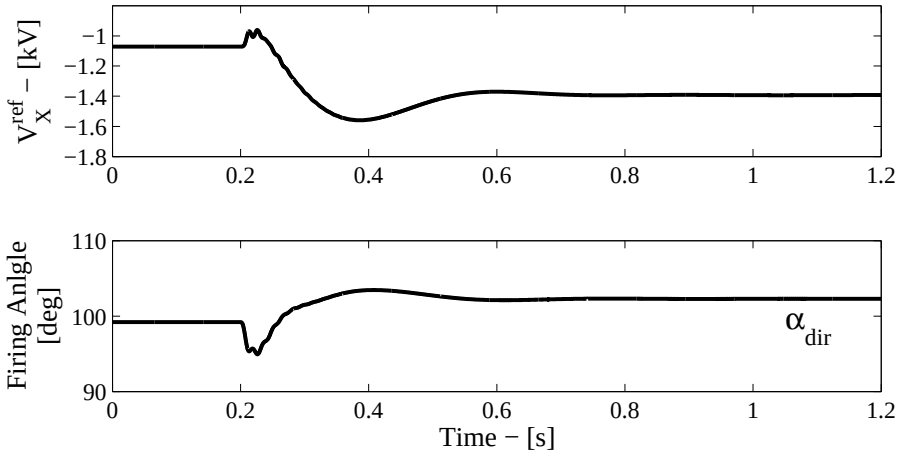


Figure 3.16: Simulation Test 4 results: thyristor power flow controller voltage and firing angle.

3.5.5 Simulation Test 5 - Operation with Positive V_X

This simulation test demonstrates the operation of the thyristor power flow controller with positive voltage injection. The reference current value is set to zero for the line current L13. By doing so, all the power produced by terminal station T1 is forced to transmit via line L23. The required injected voltage is established at 2.25kV as displayed in Figure 3.4 with triangle markers. The steady-state operation results are shown in Figure 3.17. The injected voltage is shown in Figure 3.18 with an average of 2.25kV.

The system is stable and the terminal voltage ripple is less than 0.2%. The current flowing in the thyristor power flow controller is 0.64kA which is in the upper limit range of operation according the results given in Figure 3.4.

The test demonstrates the operation of the thyristor power flow controller in the first-quadrant operation. The system is able to divert almost all the current from flowing in line L13. Such operating point can be used when a line needs to be smoothly disconnected, in a maintenance routine for example.

3.5.6 Simulation Test 6 - Weak AC System

VSC does not depend on strong ac system to operate. However, thyristor-based converter is sensitive to the strength of the ac grid. Weak ac system can lead to commutation failures of the thyristor-based converter [73]. The operation of the system is evaluated when VSC at terminal station T1 is connected to a weak ac system as shown in Figure 3.19. The setting points are $\mathrm{P}_{\mathrm{T1}}^{\mathrm{ref}} = 160MW$, $\mathrm{P}_{\mathrm{T2}}^{\mathrm{ref}} = 80MW$ and the voltage reference of the thyristor power flow controller is $\mathrm{V}_{\mathrm{X}}^{\mathrm{ref}} = -2kV$.

The short-circuit ratio (SCR) is used to determine if an ac system is weak or strong. Possible problems related to weak ac system includes commutation failure, harmonic resonance and instability. It is defined as [73]:

$$SCR = \frac{V_{ac}^2}{P_{dc} Z_{ac}} \tag{3.7}$$

where V_{ac} is the line-to-line rms ac voltage at the point of common coupling (PCC), P_{dc} is the dc power transmitted and Z_{ac} is ac impedance of the source. In general, weak ac system has a short-circuit ratio (SCR) lower than 2. For $\mathrm{V}_{\mathrm{LL}}^{\mathrm{RMS}}$=83kV and P_{dc}=160MW, a short-circuit ratio of 1.9 gives a line inductance L_{ac} of 72mH.

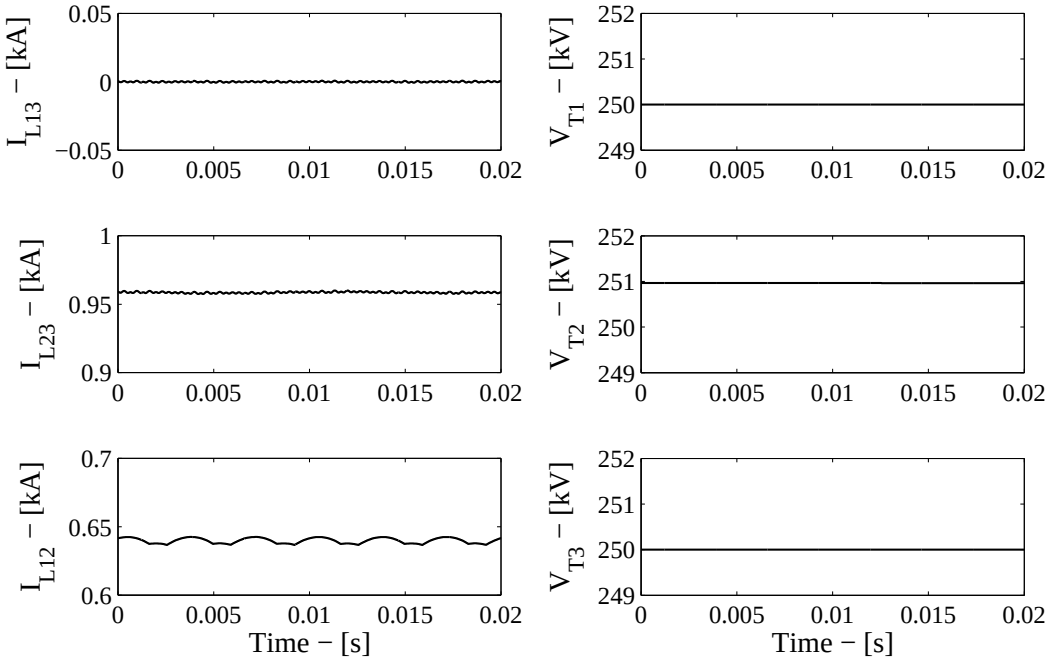


Figure 3.17: Simulation Test 5 results: dc line currents and terminal voltages.

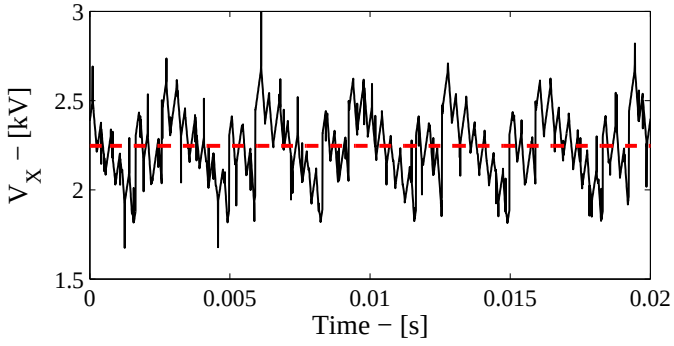


Figure 3.18: Simulation Test 5 results: thyristor power flow controller voltage.

As shown in Figure 3.19, a three-phase series RLC filter tuned to filter the harmonic content around the switching frequency is connected at the point of common coupling (PCC) [74]. Filter parameters are C_f=5uF, L_f=2.3mH and R_f=2Ω. By including the harmonic filter, the effective short-circuit ratio (ESCR), given in Equation (3.8), becomes 1.97. In addition to the filter, the q-axis reference of the VSC controller provides ac voltage support. In this scenario, i_q^{ref} is set to 1.25kA.

$$ESCR = \left(\frac{1}{Z_{ac}} + \frac{1}{Z_f}\right)\frac{V_{ac}^2}{P_{dc}} \tag{3.8}$$

where Z_f is the impedance of the harmonic filter.

The combined actions of the ac filter and the q-axis controller are effective and the THD is reduced to 2.45%. The voltage waveform at the point of common coupling is shown in Figure 3.20(a). The harmonic content of the voltage is shown in Figure 3.20(b). The magnitude is expressed as a ratio with respect to the magnitude at the fundamental frequency of the system (50Hz). All individual harmonics are below 1.25%.

From the 6-pulse thyristor-bridge of Figure 3.5, the ac harmonics are the 5^{th} and the 7^{th}. They are noticeable in Figure 3.20(b). The other harmonics are the well known side-bands of the triangular carrier frequency (1.5kHz) of the sinusoidal pulse width modulation (SPWM) of the VSC-HVDC station. They are the first side-bands (28^{th} and 32^{nd}) and the second side-bands (59^{th} and 61^{st}).

There is always concern regarding commutation failure when α_1 in Figure 3.6 approaches 180° for "direct" operation (using the forward current converter) or 0° for "inverse" operation (using the reverse direction current converter). Weak ac lines aggravate the commutation failure problem because the ac voltage (the line-voltage which does the commutation) has drooped, requiring a bigger margin so that α_1 is limited to 160°, for example, and not to 170° as might have been used for strong lines. But because VSC-HVDC station has voltage support, ac weak line is not important in implementing thyristor power flow controller.

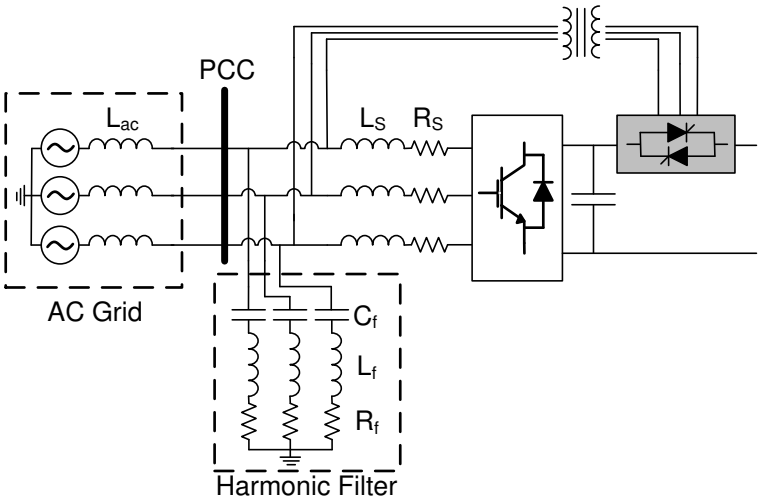
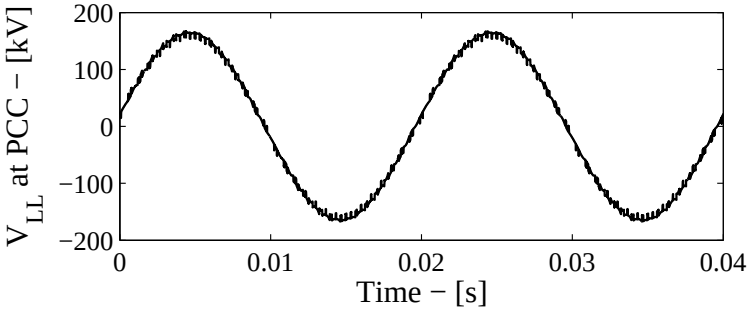
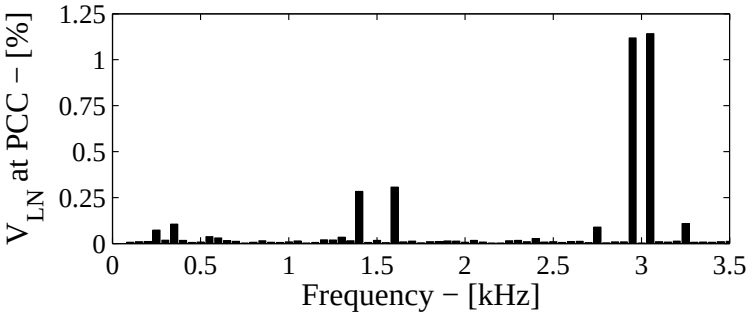


Figure 3.19: VSC-Terminal station T1 connected to weak ac grid.



(a) AC voltage waveform.



(b) Harmonic distribution of the line-neutral voltage at the PCC with magnitude relative to the fundamental frequency of the ac grid (50Hz).

Figure 3.20: Simulation Test 6 results.

3.6 Chapter Summary

This chapter has presented a dc power flow controller under the name of "thyristor power flow controller". The thyristor power flow controller consists of two 6-pulse thyristor-bridges connected in a dual-converter configuration so that it has 4-quadrant control. It benefits from being a small appendage of a VSC-HVDC station which lifts it to the high voltage of the dc line. It also takes advantage of the relatively small dc line resistance so that by inserting only a small dc voltage a very much larger dc power is controlled. Its smallness also means that its contribution to harmonic distortion is also small.

The thyristor power flow controller has been tested by simulations (PSCAD-EMTDC software package) in a 3-terminal HVDC system. Tests include: step power injection, loss of a terminal station as well as operation with weak ac line. The results show that the thyristor power flow controller is fast and stable. Total Harmonic Distortion (THD) and individual harmonic requirements are satisfied.

Chapter 4

DC Power Flow Controller: 7-Terminal HVDC Grid

The dc power flow controller topology described in Chapter 3 is integrated in a larger MTDC grid composed of 7 terminal stations. One of the 7-terminal HVDC station is equipped with the thyristor power flow controller and two terminal stations serve as dc voltage regulators. The redundancy of dc voltage regulators and transmission line reliability are also discussed.

Because of the increased system dimensions, the simulation in this chapter is performed on a multi-core (parallel processing) simulator called Opal-RT along with the related software package RT-LAB. The simulation platform uses the MATLAB / Simulink interface and simulations can be done either in real-time or offline [75]. The Opal-RT environment has been adapted to perform fixed time-step simulation that take advantage of parallel computation over multiple cores to reduce significantly the simulation duration.

4.1 Description

The 7 VSC-HVDC stations, identified as T1 to T7, are interconnected as shown in Figure 4.1. Terminal stations T1 and T6 are selected to represent offshore wind farms. The other terminal stations are onshore. The grid structure offers redundancy which contributes to satisfy the N-1 reliability criterion. For redundancy, terminal stations T2 and T5 are selected to be dc voltage regulators. All other terminal stations of the MTDC grid, including offshore wind farm terminal stations T1 and T6, are performing power control. The control reference for the VSC of each terminal station is given in Table 4.1.

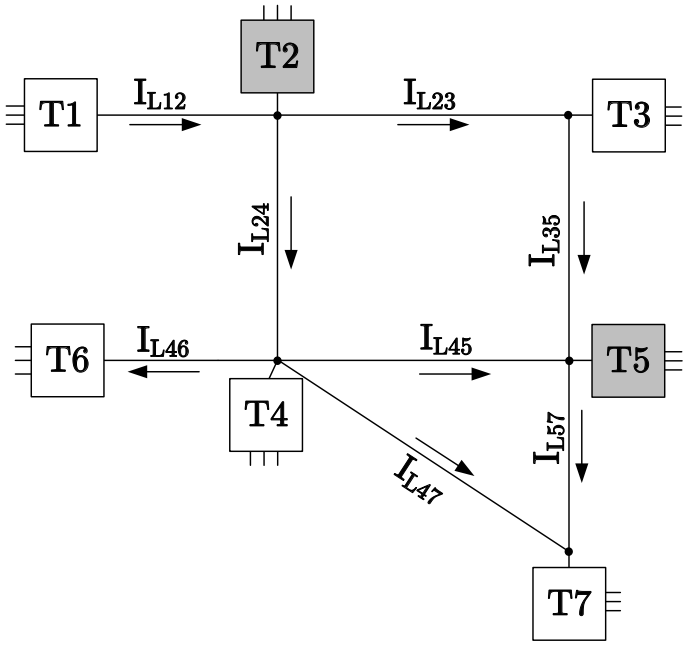


Figure 4.1: 7-Terminal HVDC grid configuration.

Table 4.1: VSC control references

Terminal station	Control mode	Control reference
T1	Power	$P_{\text{rated}} = +\ 200\text{MW}$
T2	Voltage	$V_{\text{rated}} = 250\text{kV}$
T3	Power	$P_{\text{rated}} = +\ 150\text{MW}$
T4	Power	$P_{\text{rated}} = -\ 200\text{MW}$
T5	Voltage	$V_{\text{rated}} = 250\text{kV}$
T6	Power	$P_{\text{rated}} = +\ 100\text{MW}$
T7	Power	$P_{\text{rated}} = -\ 50\text{MW}$

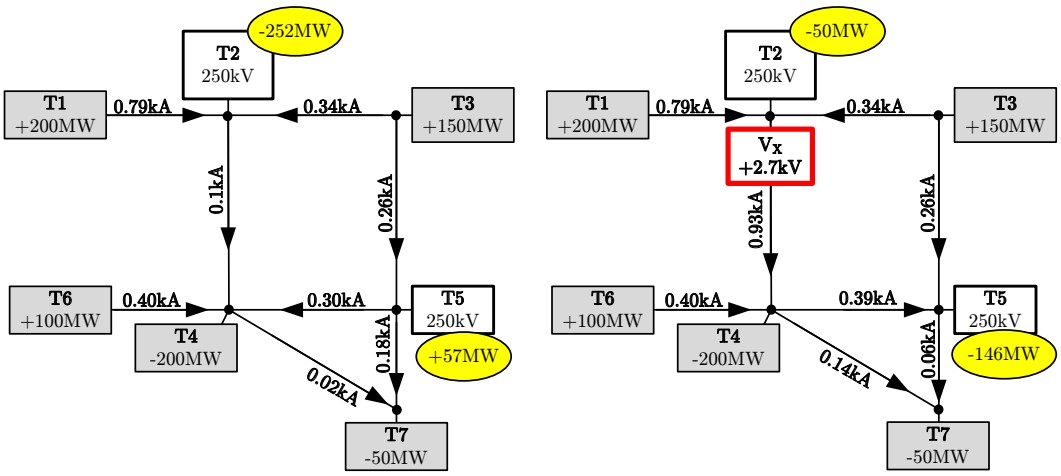
A positive power refers to power injection to the HVDC grid as opposed to negative value which refers to power extraction from the HVDC grid. The transmission lines parameters are given Table 4.2. Details and references about the transmission line model can be found in Section C.3 of Appendix C.

The operating conditions of the MTDC grid without a dc power flow controller are summarized in Figure 4.2(a). It can be noted that terminal station T2, a dc voltage regulator, has to extract 252MW in order to maintain the power balance while terminal station T5 should inject 57MW. The extraction of 252MW may be too large for T2 whereas T5 is underutilized.

A dc power flow controller is inserted at terminal station T2 on line L24 as shown in Figure 4.2(b). By injecting $V_X = +2.71kV$, the power flow around

Table 4.2: Transmission line parameters

Lines	L12	L23	L24	L35	L45	L46	L47	L57
Distance [km]	413	248	207	331	83	207	289	165
Resistance [Ω]	5	3	2.5	4	1	2.5	3.5	2
Inductance [mH]	44	26	22	35	9	22	31	17



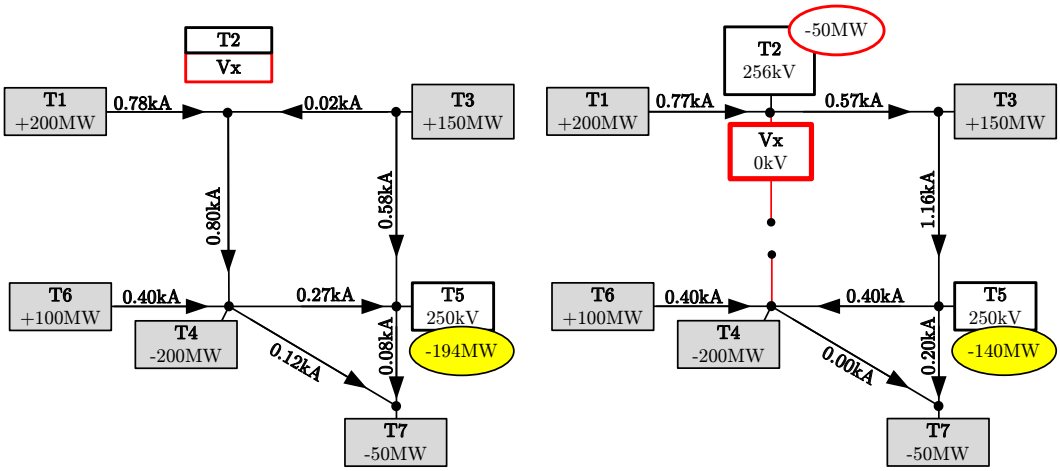
(a) without dc power flow controller. (b) with power flow controller.

Figure 4.2: Normal operation of the 7-terminal HVDC grid

terminal station T2 is changed and the power extracted by terminal station T2 is reduced from 252MW to 50MW. What was 252MW in T2 is now shifted to T5 which now has to extract 146MW. The re-routing of dc power is evident by comparing the transmission line currents in Figures 4.2(a) and 4.2(b). The VSCs at terminal stations T2 and T5 continue to perform dc voltage regulator at 250kV and it is V_X of the dc power flow controller which diverts the power flow. The other terminal stations are still performing power injection based on their reference values.

4.2 Redundancy in DC Voltage Regulator

The presence of two dc voltage regulators, T2 and T5, makes the MTDC more reliable in case of failure of one of the voltage reference terminal stations. For example, the loss of terminal station T2 allows the MTDC grid to operate normally and steady-state currents are shown in Figure 4.3(a). For this scenario, it has been assumed that the VSC as well as the dc power flow controller at



(a) loss of a dc voltage regulator terminal station.

(b) loss of a dc transmission line.

Figure 4.3: 7-Terminal HVDC grid under different contingencies.

terminal station T2 are out of service but the dc connection remains for the transmission lines. However, it is important to note that in the situation depicted in Figure 4.3(a), terminal station T5 has to compensate for the loss of terminal station T2. Therefore, it has to absorb the power that was previously extracted by terminal station T2 in order to maintain power balance in the dc grid. The operation described inhere focuses on the ability of concurrent operation of two dc voltage regulators inside the same MTDC grid and the redundancy benefit.

4.3 N-1 Contingency

The MTDC grid should be able to operate under the N-1 contingency requirement. Lines L12 and L46 are excluded from this analysis since terminal stations T1 and T6 have no line redundancy. Therefore, six cases need to be analyzed to ensure normal operation under the interruption of dc lines: L23, L24, L35, L45, L47 or L57. The results for each scenario are listed in Table 4.3.

A special consideration has to be made for the outage of line L24 (scenario 2). Since the dc power flow controller V_X is located on that line, its interruption results in the loss of this control variable in the system. As a result, the power flow cannot be redirected around terminal station T2. If left as this, terminal station T2 should extract 282MW and terminal station T5 would have to

Table 4.3: N-1 contingency scenarios

Scenario	V_X [kV]	L23	L24	L35	L45	L47	L57
1	+1.56	OUT	0.59	0.59	0.10	0.09	0.11
2*	OUT	0.57	OUT	1.16	-0.40	0.00	0.20
3	+3.56	-0.60	1.18	OUT	0.60	0.18	0.02
4	+4.85	-0.34	0.93	0.26	OUT	0.53	-0.33
5	+2.85	-0.34	0.93	0.26	0.53	OUT	0.20
6	+2.65	-0.34	0.93	0.26	0.33	0.20	OUT

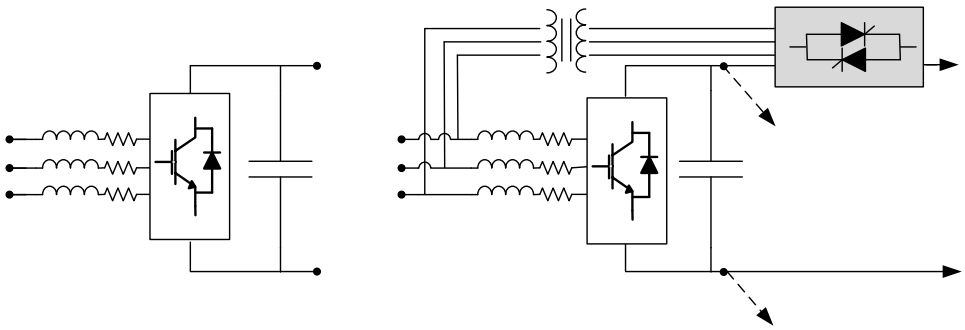
*Terminal station T2 control changes to constant power control

inject 87MW. This is beyond the power rating of 50MW initially planned for terminal station T2 converter. Suggested solutions are: i) the installation of a second dc power flow controller on line L23 for redundancy or ii) a change in the mode of operation of terminal station T2 under this circumstance only. Terminal station T2 would change from dc voltage regulator to constant power extraction of 50MW. The redundancy in the dc voltage regulator and the flexibility of the terminal station control settings allow the MTDC grid to operate in this manner as shown in Figure 4.3(b). This analysis confirms that the MTDC under study is capable of operating in agreement with the N-1 criterion of a power system.

4.4 Simulation Results

Each terminal station is composed of a VSC model as shown in Figure 4.4(a). In addition to the VSC, terminal station T2 has the thyristor power flow controller based on the thyristor topology described in Chapter 3 and it is shown in Figure 4.4(b). Complete details about the VSC model and their controllers are given in Section C.5 of Appendix C.

The analysis of the results is divided into three segments. The first segment, ranging from t=0s to t=2s, is the steady-state operation of the MTDC grid. It demonstrates the normal operation conditions shown in Figure 4.2(b). Terminal station powers, voltages and transmission line currents are shown in Figures 4.5(a), 4.5(b) and 4.6(a), respectively. Terminal stations T2 and T5 succeed to maintain their dc-side voltages at 250kV. All the other terminal stations regulate at their power reference values. The transmission line currents are in agreement with the theoretical values shown in Figure 4.2(b).



(a) Terminal stations T1 to T7, except T2.

(b) Terminal station T2.

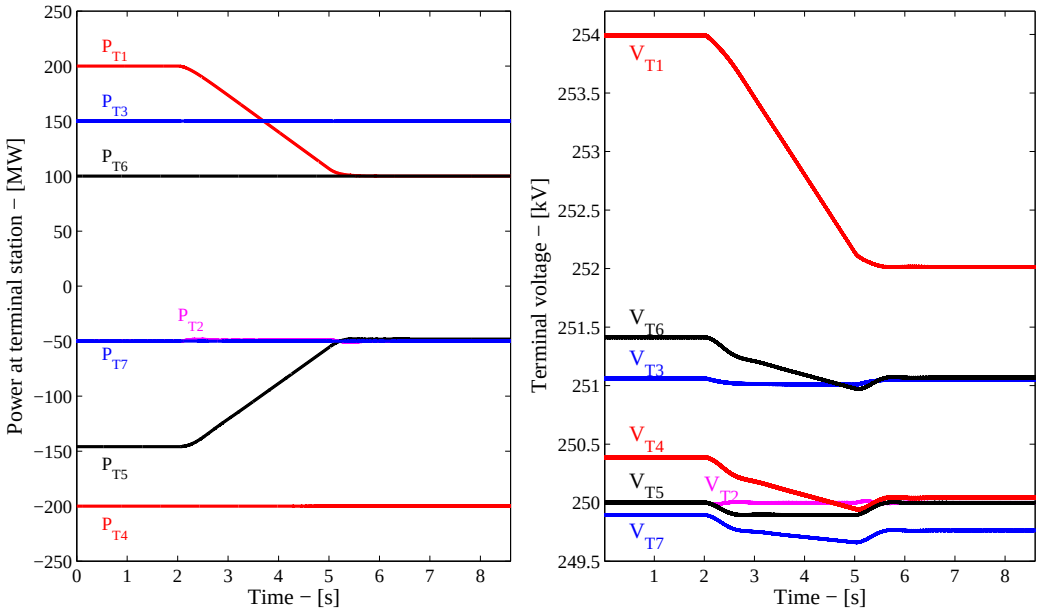
Figure 4.4: VSC Topology.

Figure 4.6(b) shows also two parameters of the dc power flow controller. The upper figure shows the two firing angles of the dual converter. Since the current never changes direction, only one part of the dual-converter is operating. In this simulation, only the "direct" thyristor-bridge is activated. The injected voltage V_X, shown in Figure 4.6(b), is regulated at +2.74kV as initially calculated.

The second segment ranges from t=2s to t=5s. During this period, terminal station T1 experiences a reduction in its power production going from 200MW to 100MW. This is intended to represent a decrease of production from an offshore wind farm. The dc power flow controller is adjusted to maintain the power extraction of terminal station T2 at 50MW while terminal station T2 maintain the dc voltage at 250kV. Terminal voltage at T5 drops slightly during the transition. The dc voltage quickly resumes to 250kV at terminal station T5 once the transition is over.

The third segment is the operating condition established after the new power contribution from terminal station T1. The segment ranges from t=5s to the end. The MTDC grid remains stable and all the other terminal stations continue to inject/extract as before. The main change is on the power extracted from terminal station T5 where it varies from 146MW to 48MW.

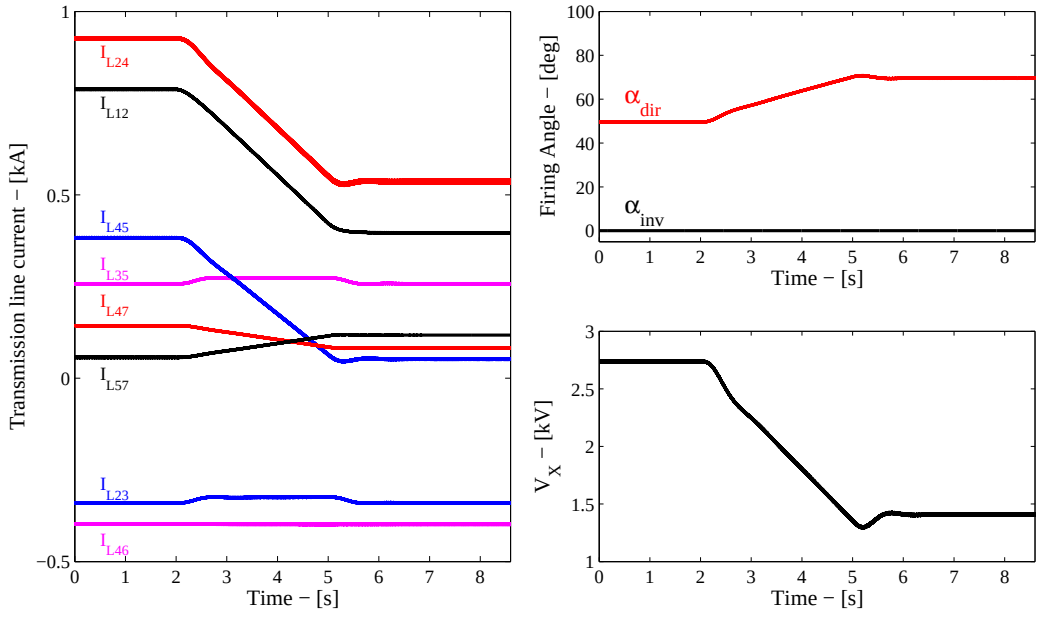
This simulation demonstrates the operation of a 7-terminal HVDC grid where power injected by one terminal station decreases by half over a 3 second period. The simulation results confirm proper operation of the dc power flow controller inside the MTDC grid.



(a) Power injection/extraction.

(b) Terminal dc voltages.

Figure 4.5: 7-Terminal HVDC grid simulation results: power injection/extraction and terminal dc voltages.



(a) Transmission line currents.

(b) DC power flow controller.

Figure 4.6: 7-Terminal HVDC grid simulation results: transmission line currents and dc power flow controller.

4.5 Chapter Summary

This chapter has presented a 7-terminal VSC-HVDC grid. It has been developed with an analysis on the dc voltage regulator redundancy as well as on the N-1 contingency criterion. This 7-terminal HVDC grid with VSC models has been simulated on a multi-core platform to show stable operation under steady-state and dynamic condition.

Part II

Marx DC-DC Converter

Chapter 5

Marx DC-DC Converter: Concept and Operation

A dc-dc converter serves the function of changing the output to input dc voltage ratio. This chapter introduces the concept and the topology of the Marx converter as a continuous dc-dc converter. The topology is described for single-stage and cascaded-stage configurations. The operation is demonstrated through simulation of a cascaded converter.

5.1 Single-Stage Marx Converter

5.1.1 Basic Marx Converter Operation

The topology of the proposed single-stage converter is shown in Figure 5.1. The concept consists of charging capacitors in parallel and reconnecting them in series. The input is a dc voltage source (V_S) and the load is modeled by a resistor (R_{load}). For purpose of illustration, the number of capacitors C_1 is M=3 to create a voltage amplification of 3. The switching components are IGBTs and fast recovery diodes. The periodicity of operation is t_{sw} second, divided into two equal sub-periods of duration $t_{sw}/2$ s.

In the first sub-period, the capacitors C_1 are charged in parallel as illustrated in Figure 5.2(a). The charging currents flow through S_1, D_1, (D_A, S_A), (D_B, S_B) and directly to the three capacitors connected between L_1 and the ground. In the second sub-period, the capacitors are connected in series to create a high voltage, $3V_S$, as shown in Figure 5.2(b). This is initiated by switching IGBTs S_{AA} and S_{BB} ON and S_A and S_B OFF.

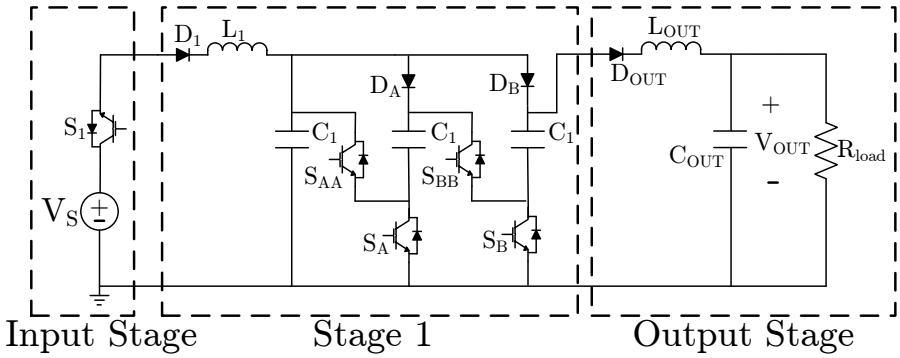
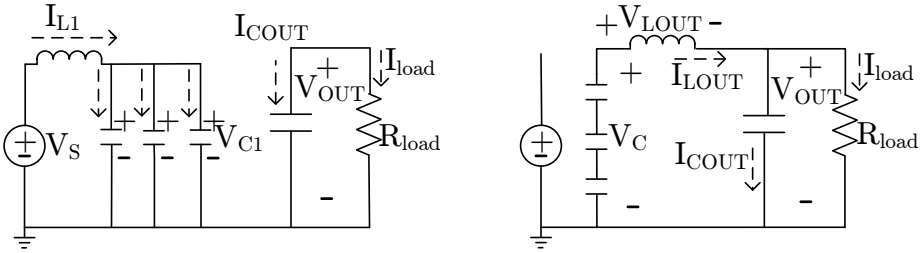


Figure 5.1: Single-stage Marx converter.



(a) Charging of C_1 in parallel.

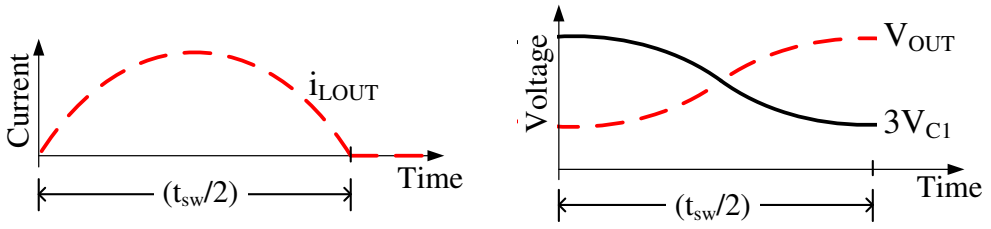
(b) Discharging of C_1 in series.

Figure 5.2: Operation states of the single-stage Marx converter.

5.1.2 Method of Electric Charge Transfer

The inter-stage inductor (L_{OUT}) is required to limit the current amplitude when the electric charges are transferred from the three series-connected capacitors C_1 to C_{OUT}, as shown in Figure 5.2(b). Without its presence, a large current surge will occur during the discharge of C_1. By neglecting the output load dynamic, the equivalent capacitor C_{eq} (formed by $C_1/3$ and C_{OUT} in series) resonates with L_{OUT}. The inductor-capacitor combination must be designed so that the resonance period is slightly less than t_{sw}.

As shown in Figure 5.3(a), the inductor current i_{LOUT} is initially zero but as $3V_{C1}$ is larger than V_{OUT}, the resonating current, flowing through diode D_{OUT}, increases. As part of the $L_{OUT} - C_{eq}$ resonance, V_{OUT} increases and $3V_{C1}$ decreases sinusoidally as illustrated in Figure 5.3(b). Meanwhile, as Figure 5.3(a) shows, the resonating inductor current increases to a peak and then it decreases towards negative values. But as the current begins to reverse in direction, the diode D_{OUT} blocks the current flow. The blocking terminates the resonance. The transferred charge in C_{OUT} is "sealed" by the diode D_{OUT}, reversed biased by the voltage ($V_{OUT} - 3V_{C1}$). In order to succeed in this,



(a) Inductor current.

(b) Capacitor and output voltages.

Figure 5.3: Voltage and current waveforms for the discharge from C_1 in series to C_{OUT}. The voltage waveforms neglect the output load dynamic.

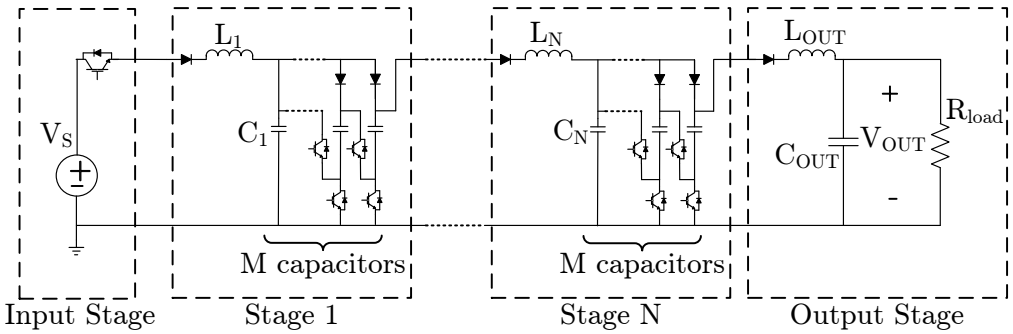


Figure 5.4: Generalized Marx Converter with multiple stages (N) composed of M capacitors per stage.

the inductor-capacitor combination must be designed so that the resonance frequency is less than $1/t_{sw}$.

The repeated charging of C_1 in parallel and discharging in series enables the Marx converter to deliver power with a voltage gain of M=3 in the example of Figures 5.1 and 5.2. The capacitor C_{OUT} serves as charge storage for continuous delivery. It has to be large enough with respect to the switching frequency, $f_{sw} = 1/t_{sw}$, so that the load current, I_{load}, has low ripples.

5.2 Multiple Stage Converter

5.2.1 Basic Structure of Cascaded Stages

Figure 5.4 shows N stages of the Marx converter connected in cascade. There is a common grounding point for the input voltage source, the intermediate stages and the load. The topology of every stage is identical but the sizes of components are tailored to the current carrying capacity and the voltage withstand required for the particular stage. The topology of the input stage

(n=0) and the output stage (n=N+1) is the same as in Figure 5.1.

The presentation is made simpler by specifying the number of stages to N=3 and the number of capacitors per stage to M=3. The overall dc voltage gain is $M^N = 3^3 = 27$. The voltage gain can easily generalize for different values of M and N. For N=3 in Figure 5.4, the inter-stage inductances are L_1, L_2, L_3, L_{OUT} and the capacitances of the 3 stages are C_1, C_2, C_3. The resistances in the inductors are neglected in the first instance so that the principles of the method are more easily understood. The resistances are reinstated in the analysis in the next chapter.

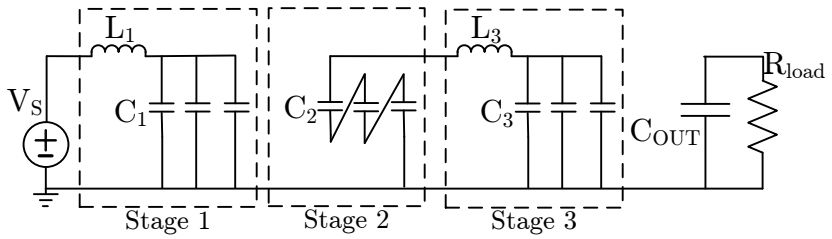
5.2.2 "Bucket Brigade" Electric Charge Transfers

The method of transferring the electric charge from the voltage source V_S to the load R_{load}, resembles the bucket brigade used in putting out fires. The solid-state switches in the odd-numbered stages (n=1,3,...) follow the logic notation S and the even-numbered stages (n=2,4,...) come under the logic notation $\overline{S}$. When S is 1, $\overline{S}$ is 0 and vice versa.

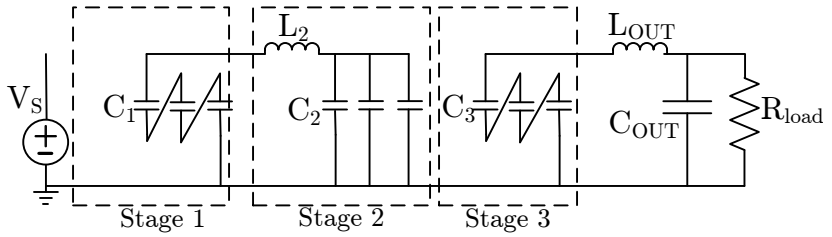
When S=1, the odd-numbered stages are getting charged by having their capacitors connected in parallel. Their capacitors have been charged by the series-connected capacitors of the previous even-numbered stages except for stage 1 where it is from the input voltage source V_S. This operation is illustrated in Figure 5.5(a). The charging currents flow through L_1 and L_3. There is no current flowing in L_2 and L_{OUT}.

When S=0, the odd-numbered stages are discharging to the following even-numbered stages by having their capacitor connected in series. The even-numbered stages are configured with the capacitor connected in parallel. This operation is illustrated in Figure 5.5(b). The charging currents flow through L_2 and L_{OUT}. There is no current flowing in L_1 and L_3. In this example, the output stage is on the sequence of an even-numbered stage ("stage 4"), which means that it is getting charged when S=0.

The cascaded Marx converter operates by periodic alternate switching: S=1, S=0, S=1, S=0,... The electric charges are transferred from the source, V_S, to stage n=1 and then to stage n=2... until they reach R_{load}, as in a bucket brigade. The diodes which are in series with the inter-stage inductors ensure unidirectional charge transfer.



(a) Configuration when S=1.



(b) Configuration when S=0.

Figure 5.5: The arrangements for the two sub-periods of equal duration $t_{sw}/2$.

5.3 Analysis of Multi-Stage Marx Converter

For clarity in presentation, Figures 5.1, 5.2 and 5.5 have been drawn with M=3 capacitors for every stage. In order to derive formulas that will be generally useful in design, this section and subsequent sections of this chapter return to the algebraic M. It is assumed that periodic steady-state has already been reached.

At this point, it is necessary to clarify the subscripts n and $n+1$ in the definition of the equivalent capacitor symbol $C_{eq-n-n+1}$ which will be used. They designate the equivalent capacitor formed by connecting M series capacitors of size C_n (of the n^{th} stage) to M parallel connected capacitors of size C_{n+1} (of the $(n+1)^{th}$ stage) as shown in Figure 5.5.

For the multiple-stage system of Figure 5.4, the dc voltages increase as by the geometric series. The output voltage gain of the n^{th} stage is by the relation:

$$V_{Cn} = MV_{C(n-1)} \tag{5.1}$$

So the output voltage is:

$$V_{OUT} = M^N V_S \tag{5.2}$$

5.3.1 Charging of Stage n=1 by V_S

When S_1, S_A and S_B are ON during the charging phase, the input voltage V_S is higher than the capacitor voltages (which have been discharged previously to $V_S - 0.5\Delta V_{C1}$, where ΔV_{C1} is the peak to peak ripple voltage on capacitor C_1). Therefore, diodes D_1, D_A and D_B are forward biased and conduct. Thus, the M parallel capacitors in Stage n=1, whose equivalent value is $C_{eq-0-1} = MC_1$. For resonant period $t_{sw} = 2\pi/\omega$, it is necessary to choose the L_1 to satisfy

$$\omega = \frac{1}{\sqrt{L_1 C_{eq-0-1}}} \tag{5.3}$$

For an L-C resonant circuit, the solution of voltage is $A\sin(\omega t)+B\cos(\omega t)+C$, where the coefficients A, B and C are determined by the initial conditions. At t=0, it is assumed that capacitor C_1 has discharged to C_2 so $v_{C1}(0) = V_S - 0.5\Delta V_{C1}$ and $i_{L1}(0) = 0$ (see Stage 1 of Figure 5.5(b)). The solutions of voltage and current for $t > 0$ are:

$$v_{C1}(t) = V_S - 0.5\Delta V_{C1}\cos(\omega t) \tag{5.4}$$

and

$$i_{L1}(t) = I_{L1}^P \sin(\omega t) \tag{5.5}$$

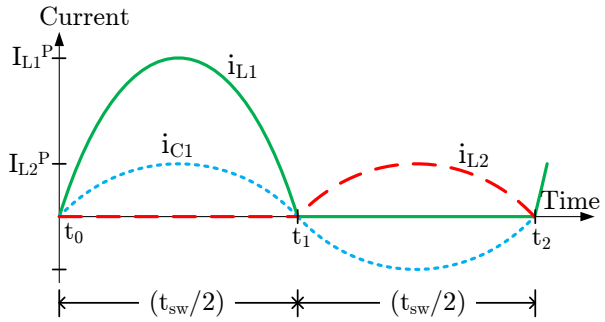
where I_{L1}^P is the peak inductor current.

Figure 5.6 shows their waveforms. For $t_0(=0) \leq t \leq t_1(=t_{sw}/2)$ the inductor current i_{L1} is a positive half-sine wave during the charging phase and reaches zero at $t = t_{sw}/2$ as shown in Figure 5.6(a). The inductor current i_{L1} divides into M to charge C_1 through capacitor current i_{C1}. When i_{L1} reverses direction, the diode D_1 blocks and prevents the current from flowing back to the source. Figure 5.6(b) shows the voltage of C_1 rising from $V_S - 0.5\Delta V_{C1}$ to $V_S + 0.5\Delta V_{C1}$. At the instant $t = t_{sw}/2$, IGBTs S_A, S_B are turned OFF.

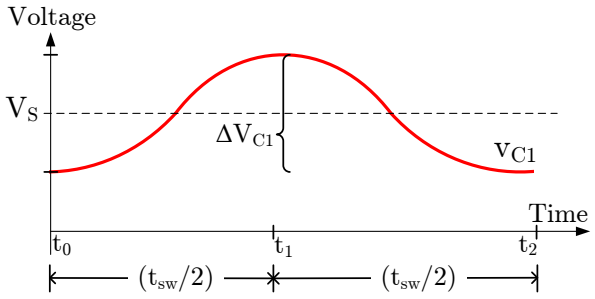
5.3.2 Charging of Stage n=2 by Stage n=1

When S_{AA}, S_{BB} are turned ON, the voltage across the M-series connected C_1 is

$$Mv_{C1}(0.5t_{sw}) = M\left(V_S + 0.5\Delta V_{C1}\right) \tag{5.6}$$



(a) Current.



(b) Capacitor voltage.

Figure 5.6: Ideal resonant waveforms for the currents and voltages.

As illustrated in Figure 5.5(b), the M parallel connected capacitors C_2 of Stage 2 are charged by the M series connected capacitors C_1 of Stage 1. The equivalent capacitance is:

$$C_{eq-1-2} = \frac{(C_1/M)(MC_2)}{C_1/M + MC_2} \tag{5.7}$$

The inductance L_2 is chosen so that the resonance frequency remains the same as that for Equation (5.3); that is:

$$\omega = \frac{1}{\sqrt{L_2 C_{eq-1-2}}} \tag{5.8}$$

Figures 5.6(a) and 5.6(b) show the waveforms of the currents i_{C1}, i_{L2} and of the voltage v_{C1}. In Stage 2, for $t_1 \leq t \leq t_2$, the inductor current $i_{L2} = -i_{C1}$ divides into M to charge C_2. Because the charging current of C_2 is reduced by M, in order to maintain the relative voltage ripple $(\Delta V_{C2}/V_{C2})$ the same as with $(\Delta V_{C1}/V_{C1})$ for capacitor C_1, it is necessary to make $C_2 = C_1/M^2$. By doing so, the voltage ripple for capacitor C_2 is:

$$\Delta V_{C2} = M\Delta V_{C1} \tag{5.9}$$

5.3.3 Definition of General Time Axis

Since odd-numbered stages alternate in time with even-numbered stages, a new time variable t' is defined so that equations can be written for both logic states S=1 for Figure 5.5(a) and S=0 for Figure 5.5(b). When even-integer stages charge odd-integer stages as just described, the origin of time $t'\,(0.0 \leq t' \leq 0.5t_{sw})$ coincides with t_0 in Figure 5.6. When odd-integer stages charge even number stages as currently under discussion, the origin of time $t'\,(0.0 \leq t' \leq 0.5t_{sw})$ coincides with t_1 in Figure 5.6.

Using this new time axis, at $t' = 0$, the initial conditions are:

$$
\begin{aligned}
&i_{L2}(0) = 0.0 \;\text{ for the inductor } L_2\\
&MV_{C1}(0) = M(V_S + 0.5\Delta V_{C1}) \;\text{ for the M-series connected } C_1\\
&V_{C2}(0) = M(V_S - 0.5\Delta V_{C1}) \;\text{ for the M-parallel connected } C_2
\end{aligned}
$$

(In the previous half-cycle, the capacitors C_2 have been connected in series to transfer charges to C_3. Its value at the end of the discharge is $V_{C2}(t_1) = M(V_S - 0.5\Delta V_{C1})$.) With these initial conditions, the voltage of C_2 is,

$$v_{C2}(t') = M\left[V_S - 0.5\Delta V_{C1}\cos(\omega t')\right] \tag{5.10}$$

and the current through L_2 is:

$$i_{L2}(t') = I_{L2}\sin(\omega t') \tag{5.11}$$

As shown in Figure 5.6, $i_{L2}(t')$ begins to reverse direction at $t' = t_{sw}/2$. The diode D_2 blocks and isolates stage n=2 from stage n=1.

5.3.4 Charge Transfer from Stage $(n-1)$ to Stage n

5.3.4.1 Capacitor Size

The energy inside the capacitor is given as:

$$W_n(t') = \frac{1}{2}C_n V_{Cn}^2(t') \tag{5.12}$$

So, the energy at time $t' = 0$ is:

$$W_n(0) = \frac{1}{2}C_n\left[V_{Cn} - 0.5\Delta V_{Cn}\right]^2 \tag{5.13}$$

Similarly, the energy at time $t' = t_{sw}/2$ is:

$$W_n(t_{sw}/2) = \frac{1}{2} C_n \left[V_{Cn} + 0.5\Delta V_{Cn}\right]^2 \tag{5.14}$$

Therefore, the energy transferred in a given sub-period is calculated as:

$$\Delta W_n = W_n(t_{sw}/2) - W_n(0) = C_n V_{Cn} \Delta V_{Cn} \tag{5.15}$$

Using Equation (5.15), the energy transferred for stage $(n-1)$ is:

$$\Delta W_{n-1} = C_{n-1} V_{C(n-1)} \Delta V_{C(n-1)} \tag{5.16}$$

By having the same relative capacitor voltage ripple between stages, Equation (5.17) is obtained.

$$\frac{\Delta V_{Cn}}{V_{Cn}} = \frac{\Delta V_{C(n-1)}}{V_{C(n-1)}} \tag{5.17}$$

Assuming conversation of energy, it is possible to equate Equations (5.15) and (5.16). When it is combined with Equations (5.1) and (5.17), the capacitor size is expressed as:

$$C_n = \frac{C_{n-1}}{M^2} \tag{5.18}$$

or in terms of C_1:

$$C_n = \frac{C_1}{M^{2n-2}} \tag{5.19}$$

The equivalent capacitance C_{eq-n} when charging capacitors of stage n with capacitors of stage $(n-1)$ is:

$$C_{eq-n} = \frac{M C_{n-1} C_n}{C_{n-1} + M^2 C_n} \tag{5.20}$$

substituting Equation (5.19) in Equation (5.20),

$$C_{eq-n} = \frac{1}{2} \frac{C_1}{M^{2n-3}} \tag{5.21}$$

5.3.4.2 Capacitor Voltage

The voltage across capacitor C_n is of the form:

$$v_{Cn}(t') = M^{n-1} V_S - 0.5\Delta V_{Cn} \cos(\omega t') \tag{5.22}$$

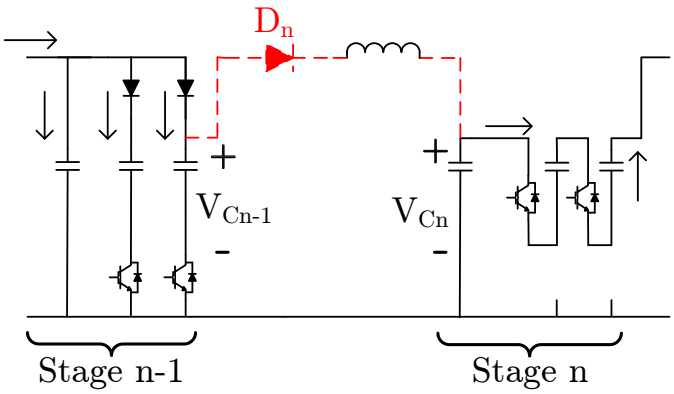


Figure 5.7: Configuration when stage $(n-1)$ is charging (parallel connection) and stage n is discharging (series connection).

where the capacitor peak to peak voltage ripple ΔV_{Cn} is

$$\Delta V_{Cn} = M^{n-1} \Delta V_{C1} \tag{5.23}$$

which gives the general expression,

$$v_{Cn}(t') = M^{n-1} \left[V_S - 0.5 \Delta V_{C1} \cos(\omega t') \right] \tag{5.24}$$

Therefore at $t' = 0$,

$$v_{Cn}(0) = M^{n-1} \left[V_S - 0.5 \Delta V_{C1} \right] \tag{5.25}$$

and at $t' = 0.5 t_{sw}$,

$$v_{Cn}(0.5 t_{sw}) = M^{n-1} \left[V_S + 0.5 \Delta V_{C1} \right] \tag{5.26}$$

An additional requirement has to be set regarding the allowed capacitor voltage ripple. Figure 5.7 shows the configuration of the converter when stage $(n-1)$ is charging (parallel connection) and stage n is discharging (series connection). It is important that diode D_n remains reverse biased and it is done by ensuring that $V_{C(n-1)} < V_{Cn}$. The critical instant occurs when stage $(n-1)$ is at its peak voltage ripple and stage n is at its lowest voltage ripple. The relationship is shown in Equation (5.27) and it leads to a limit on the capacitor voltage ripple.

$$M^{n-2} V_S + \frac{\Delta V_{C(n-1)}}{2} < M^{n-1} V_S - \frac{\Delta V_{Cn}}{2} \tag{5.27}$$

For the same relative capacitor voltage ripple, Equation (5.23) is inserted in Equation (5.27) to obtain the requirements in terms of ΔV_{C1}:

$$\frac{\Delta V_{C1}}{2} < \frac{M-1}{M+1} V_S \tag{5.28}$$

The closer boundary occurs when $M = 2$ and the capacitor voltage ripple should not exceed $\pm 33\%$ of the input voltage V_S.

5.3.4.3 Capacitor Current

Applying $C_n \frac{dv_{Cn}(t)}{dt}$ and substituting Equation (5.19), the discharging current of C_n is:

$$i_{Cn}(t') = \frac{0.5 \Delta V_{C1} \omega C_1 \sin(\omega t')}{M^{n-1}} \tag{5.29}$$

It is also the current of inductor L_{n+1} for the sub-period when stage $(n+1)$ is charged. i.e. $i_{Ln+1}(t') = -i_{Cn}(t')$ for $t_{sw}/2 < t' < t_{sw}$.

5.3.4.4 Inductor Size

Generalizing from Equation (5.8) and applying Equation (5.21), in order to ensure identical resonant periods, the inductance L_{n+1} between stage n and stage $(n+1)$ is:

$$L_{n+1} = \frac{2M^{2n-1}}{C_1} \left(\frac{t_{sw}}{2\pi} \right)^2 \tag{5.30}$$

5.3.5 Power Delivered

Substituting Equations (5.24) and (5.29), the power delivered by the M series-connected C_n is:

$$p_n(t') = [M v_{Cn}(t')]\, i_{Cn}(t') = M \left[V_S - \frac{\Delta V_{C1}}{2} \cos(\omega t') \right] \left[\frac{\Delta V_{C1}}{2} \omega C_1 \sin(\omega t') \right] \tag{5.31}$$

As the formula of $p_n(t')$ in Equation (5.31) is independent of n, this shows that by sizing the capacitors and the inductances according to Equations (5.19) and (5.30) respectively, the transfer of power through all the converter stages are identical. Integrating Equation (5.31) in the half-period, $0.5t_{sw}$, and taking the average for the complete switching cycle:

$$P_n = \frac{1}{t_{sw}} M V_S C_1 \Delta V_{C1} \tag{5.32}$$

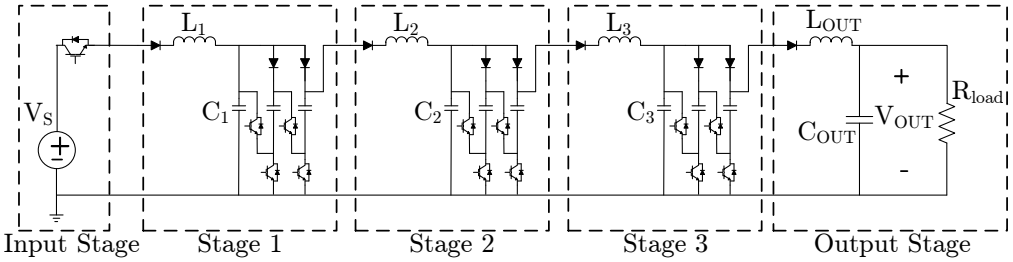


Figure 5.8: Marx converter with 3-stage and 3 capacitors per stage (N=3, M=3).

Table 5.1: Simulation parameters

Configuration			
Number of stage N	3		
Number of steps M	3		
Power Ratings			
Rated power - P_{rated} [MW]	1		
Input voltage - V_S [kV]	1		
Average output voltage - V_{OUT} [kV]	27		
Output load - R_{load} [Ω]	729		
Switching frequency - f_{sw} [kHz]	2		
Capacitors		**Inductors**	
C_1 [uF]	833.33	L_1 [uH]	2.53
C_2 [uF]	92.59	L_2 [uH]	45.59
C_3 [uF]	10.29	L_3 [uH]	410.35
C_{OUT} [uF]	1.89	L_{OUT} [mH]	3.83

For a given input voltage V_S, capacitor value C_1 and switching frequency, the power transferred depends on ΔV_{C1}, the voltage ripple. The formula (5.32) is useful in the design.

5.4 Simulation Results

Verification of the operation and of the formulas derived is done using digital simulations via PSCAD-EMTDC software package, an industry-grade software for high voltage power electronic research. The configuration tested is a 3-stage converter with 3 capacitors per stage (N=3, M=3) as shown in Figure 5.8. The system parameters used in the simulation are listed in Table 5.1.

5.4.1 Steady-State Operation

The simulated inductor current waveforms and the capacitor voltage waveforms are shown in Figures 5.9(a) and 5.9(b), respectively. In the first sub-period, the logic notation is S=1 and Figure 5.5(a) depicts the circuit connection. The solid-state switches connect the source voltage V_S to the capacitors C_1 in stage 1. Figure 5.9(a) shows the charging current I_{L1}. As shown in Figure 5.9(b), V_{C1} increases because the capacitors C_1 are charged in parallel.

In the same sub-period, stage 2 is connected to stage 3. Capacitors C_2 are connected in series and its electric charges are transferred to parallel connected capacitors C_3 as shown by the inductor current I_{L3} in Figure 5.9(a). Figure 5.9(b) shows the decreasing V_{C2}, the voltage of C_2, as they are discharged and the increasing V_{C3} as C_3 are charged.

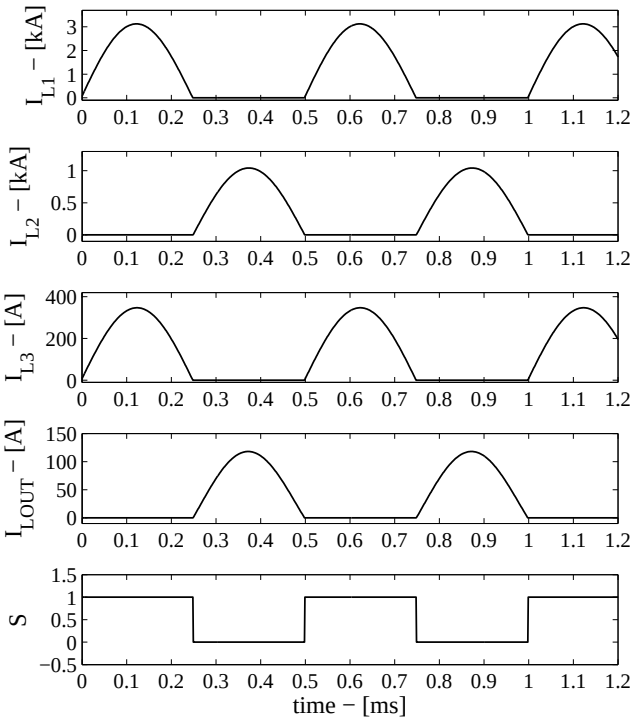
The stored charges in capacitor C_{OUT} feeds the output resistance R_{load}. The decreasing capacitor voltage V_{OUT}, as it discharges stored energy to the resistive load is shown in Figure 5.9(b). Throughout this time, stage 1 is isolated from stage 2 while stage 3 is isolated from the load so that the inductor currents $I_{L2} = I_{LOUT} = 0$.

In the next sub-period, the logic notation is S=0 and Figure 5.5(b) depicts the circuit connection. Thereafter, the switching alternates with the logic states, S, $\overline{S}$, S, $\overline{S}$, S... The waveforms in Figures 5.9(a) and 5.9(b) confirm "bucket brigade" concept of transferring electric charge from the source V_S to the output C_{OUT}.

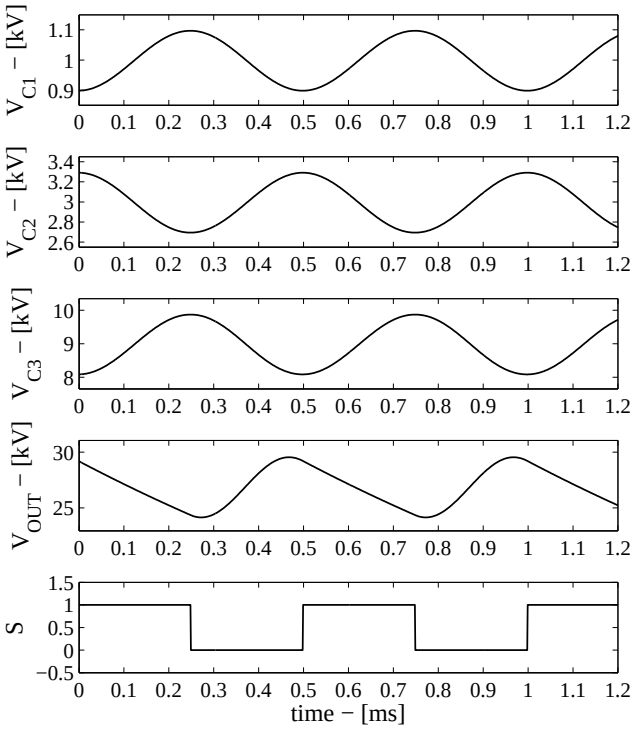
From Figure 5.9(a), the peaks of currents decrease in multiples of 1/3: $I_{L1} = 3.13kA$, $I_{L2} = 1.04kA$, $I_{L3} = 347A$, $I_{LOUT} = 118A$. From Figure 5.9(b), one sees that the average dc voltages increases in multiples of 3: $V_{C1} = 1kV$, $V_{C2} = 3kV$, $V_{C3} = 9kV$ and $V_{OUT} = 27kV$. Thus the kVA requirement of each stage remains constant. As cost of power electronic switches and diodes are related to kVA, one sees that the cost increases with the number of stages whereas the dc voltage gain increases geometrically. Further analysis about power ratings of components is introduced in Chapter 8.

5.4.1.1 Output Stage

The output stage is modeled by a resistance and simulation results of V_{OUT} are displayed in Figure 5.9(b). The output voltage and output power are shown for an expanded time scale in Figure 5.10. The output power has an average



(a) Inductor currents.



(b) Capacitor voltages.

Figure 5.9: Simulation results in the two sub-periods S=1 and S=0.

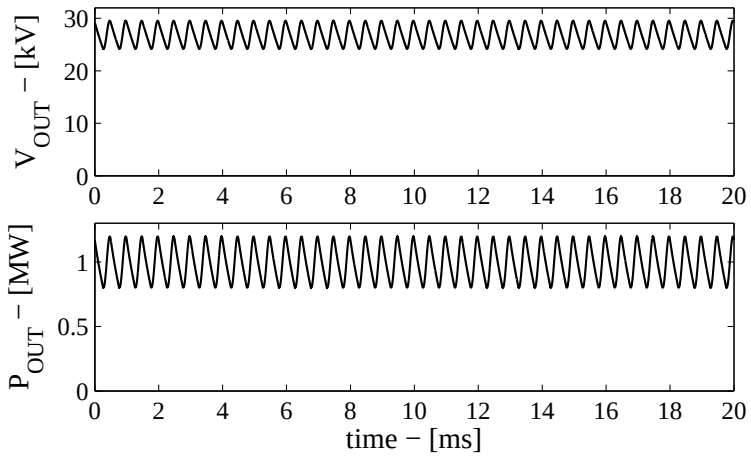


Figure 5.10: Simulation results showing ripples on the output voltage and output power. The ripples are associated with alternate switching states of the converter.

Table 5.2: Design values and simulation results

Average voltage			**Voltage ripple**		
	Design	Simulation		Design	Simulation
V_{C1} [kV]	1	1.00	ΔV_{C1} [kV]	0.2	0.20
V_{C2} [kV]	3	2.99	ΔV_{C2} [kV]	0.6	0.60
V_{C3} [kV]	9	8.98	ΔV_{C3} [kV]	1.8	1.79
V_{COUT} [kV]	27	26.82	ΔV_{COUT} [kV]	-	5.39

of 0.99MW, close to the designed 1MW power rating. The size of ripples can be reduced by increasing C_{OUT}.

Table 5.2 lists under the column labelled "Design" the values computed from the analytical solution. By their side are the simulated values. They show agreement to within 0.7% in accuracy. The discrepancy is mainly due to small resistances of the IGBT switches which have been omitted in the analytical formulas but included in the simulation.

5.4.2 Transient Operation

In evaluating the transient response characteristics, two simulation runs have been performed: (i) step-change on load side; (ii) step-change on source side.

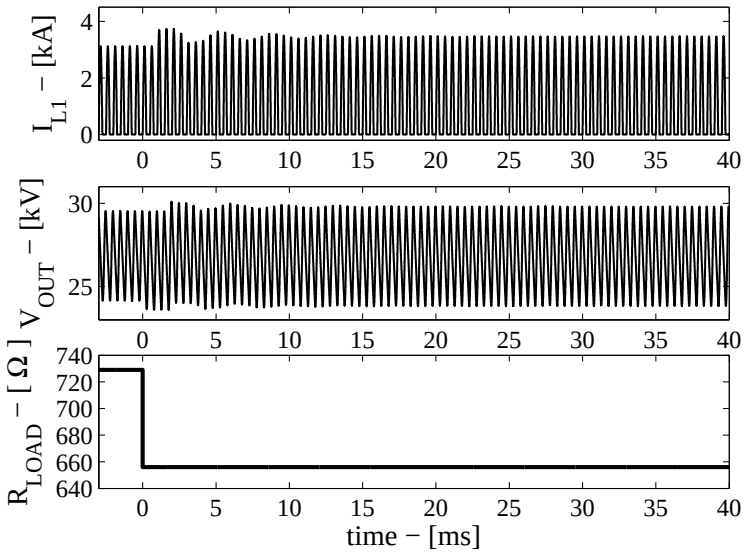


Figure 5.11: Simulation results for inductor L_1 current and output voltage V_{OUT} for a step-change in load.

5.4.2.1 Step-Change on Load Side

A 10% step-change in the load is simulated by changing R_{load} from 729 ohms to 656 ohms. The response is recorded in Figure 5.11. As to the load voltage, the average output voltage remains at 26.78kV which is consistent with the unchanged input voltage multiplied by a gain of $M^N = 27$. The ripple ΔV_{OUT} has an increase of 11%, from 5.39kV to 6.00kV. This result is in agreement with the formula derived in Equation (5.32).

The step change does not generate a large transient in the current I_{L1}, the current in inductor L_1. The transient appears only at the third cycle after the change because it takes a number of sub-periods for the step-change to propagate upstream to inductor L_1. The settling time is about 15ms.

5.4.2.2 Step-Change at Input Side

The step change test on the input side consists of decreasing V_S from 1kV to 0.9kV. As shown in Figure 5.12, initially the average of V_{OUT} is 27kV and settles to an average of 24kV. Both averages are consistent with the theoretical amplification ratio of 27. It takes about 30ms for the transients to disappear.

The initial non-conduction periods of I_{L1} suggest that the voltages across C_2 have been higher than the voltages of series connected C_1 so that the diode D_2 has been reverse biased. After few cycles, the voltages across capacitors

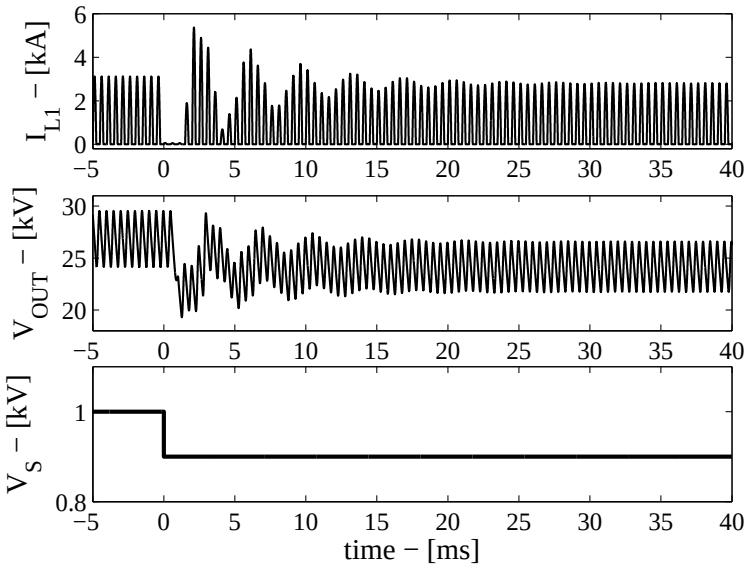


Figure 5.12: Simulation results for inductor L_1 current and output voltage V_{OUT} for a step change in the input voltage.

have decreased from the output stage up to the first stage to reengage the charge transfer cycles.

5.5 Chapter Summary

The Marx converter topology presented in this chapter is shown to be capable of providing high power after stepping up to high dc voltage. Stepping up to high dc voltage follows the classic Marx concept of capacitor charging in parallel followed by reconnection of the charged capacitors in series. The transfer of electric charge from the input capacitor to the output capacitor is by L-C resonance and an inductor-in-series-with-a-diode between capacitors. The diode ensures that the charge transfer of each cycle is unidirectional. The operation has been validated by simulation using PSCAD-EMTDC software package.

Chapter 6

Marx DC-DC Converter: Converter Design Guidelines

This chapter presents design guidelines for the presented Marx converter. The analysis is intended to develop tools to select adequate inductor and capacitor values depending on design requirements such as voltage ripples. The analysis includes loss resistances associated with switches and passive components as well as turn-off margin for switching events.

At the end of the chapter, the design of a 5kW converter is done. This 5kW converter design will be used for the construction of the prototype presented in the following chapter.

6.1 Initial Configuration

This section will go through the design steps of a converter with N-stages and M-capacitors per stage as shown in Figure 6.1. The analysis assumes the converter is in steady-state.

The switching frequency is f_{sw}, therefore, a switching period of $t_{sw}(= 1/f_{sw})$. Each sub-period is of duration $t_{sw}/2$. A turn-off margin, also called dead-time, can be introduced in the design to ensure that the resonance is terminated before the next switching event occurs. As soon as the inductor current reaches zero, the series diode is reversed biased which creates the dead-time. It is shown in Figure 6.2 and the dead-time period is identified as t_{dead}. The period used in the resonance calculation from the L-C parameters is t_{res}

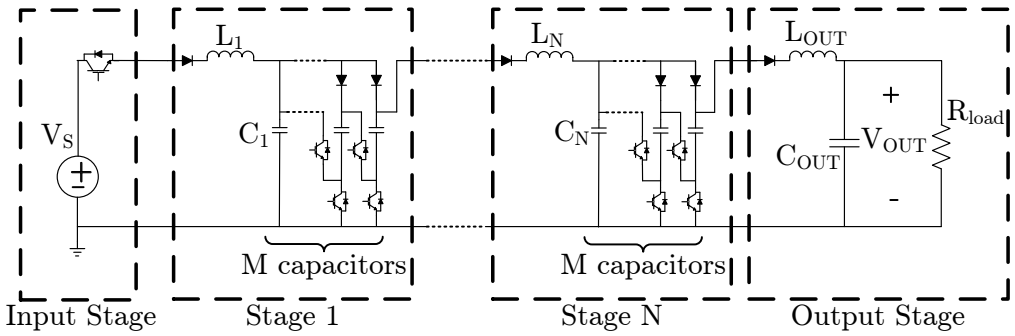


Figure 6.1: Marx converter topology with N cascaded stages and M capacitors per stage.

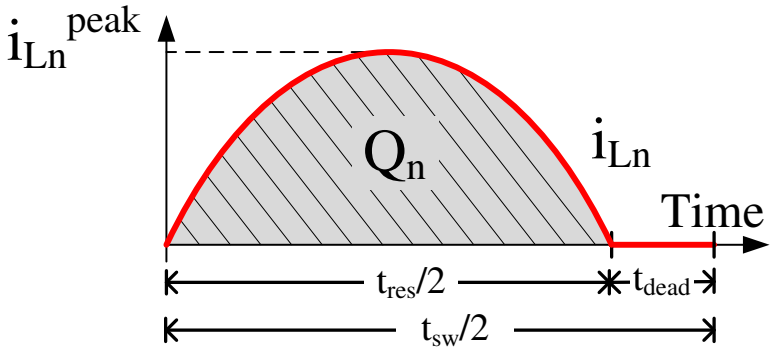


Figure 6.2: Inductor current waveform with dead-time period.

and it is defined as:

$$\frac{t_{res}}{2} = \frac{t_{sw}}{2} - t_{dead} \tag{6.1}$$

where t_{dead} is the dead-time requirement within the sub-period.

By neglecting the losses and the impact of the dead-time, the capacitor voltage at each stage, as recalled from Chapter 5, is:

$$V_{Cn} = M^{n-1} V_S \tag{6.2}$$

where n is the stage index number which excludes the output stage. For the output voltage, it can be calculated using simply:

$$V_{OUT} = M^N V_S \tag{6.3}$$

where V_S is the input voltage, M is the number of capacitors per stage and N is the total number of stages excluding the input and output stages. Based on the designed rating of the converter, the output resistance, modeling the load,

is:

$$R_{load} = \frac{V_{OUT}^2}{P_{rated}} \tag{6.4}$$

where V_{OUT} is the average output voltage and P_{rated} is the rated power of the converter.

6.2 Capacitor Sizing

The amount of charge required by the load is used in the evaluation of the capacitor sizing. The amount of charge in a complete switching period t_{sw} at the load is:

$$Q_{load} = \frac{V_{OUT}}{R_{load}} t_{sw} \tag{6.5}$$

By combining Equations (6.3) and (6.4), Equation (6.5) can be rewritten as:

$$Q_{load} = \frac{P_{rated}}{M^N V_S} t_{sw} \tag{6.6}$$

6.2.1 Stage 1 to N

The first step consists of determining the capacitor value based on the desired capacitor voltage ripple. The voltage ripple for capacitor at each stage is given as:

$$\Delta V_{Cn} = \frac{Q_n}{MC_n} \tag{6.7}$$

where n is the stage index number, Q_n is the amount of charge transferred for that stage and ΔV_{Cn} is the peak to peak voltage ripple in volts. The relationship between Q_n and Q_{load} is:

$$Q_n = M^{N-n+1} Q_{load} \tag{6.8}$$

By using Q_{load} and the voltage ripple, the capacitance at stage n can be calculated by using:

$$C_n = \frac{Q_{load}}{\Delta V_{Cn}} M^{N-n} \tag{6.9}$$

6.2.2 Output Stage

The results obtained from Equation (6.9) are not accurate for the output stage. It can be explained by looking at the output capacitor voltage waveform

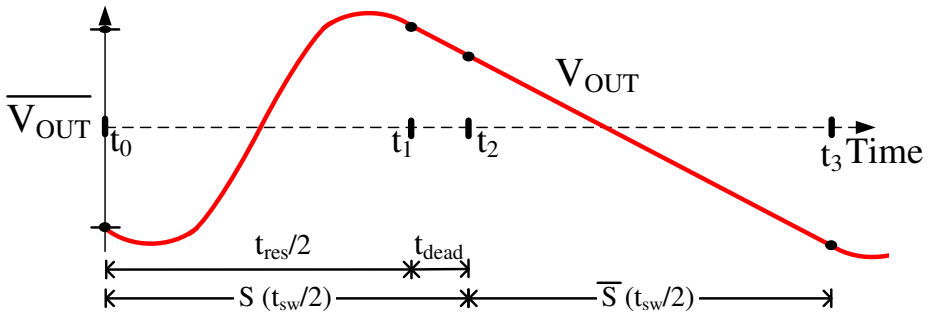


Figure 6.3: Output voltage V_{OUT} waveform in the two state configurations: the charging (S), followed by the discharge ($\overline{S}$). The dead-time occurs between (t_1 to t_2).

displayed in Figure 6.3. In the figure, the charging phase is associated to sub-period S and the discharging phase to sub-period $\overline{S}$. The circuit associated with charging phase in shown in Figure 6.4(a). The dead-time occurs between t_1 and t_2 and the arrangement is shown in Figure 6.4(b). It is composed of simply the output capacitor C_{OUT} connected in parallel with the load resistance R_{load}. This arrangement remains the same during the discharge phase, $\overline{S}$, as shown in Figure 6.4(c).

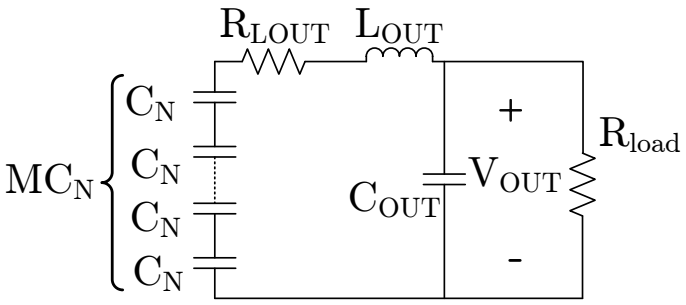
The output voltage waveform during the charging process does not have the sinusoidal shape of other stages as shown in Figure 6.3. It can be analyzed by linear superposition of the sinusoidal waveform related to the charge transfer from stage N to output stage and of the discharging waveform from the R-C circuit with the load. This relationship is shown in Equation (6.10). Since the time constant T_{RC} ($= R_{load}C_{OUT}$) is much larger than $t_{res}/2$, the discharge from the load can be linearly approximated and the voltage waveform of the output capacitor being charged can be approximated using Equation (6.11) for $t_0 < t < t_1$.

$$V_{OUT}(t) = \frac{Q_{load}}{2C_{OUT}}\left[1 - \cos\left(\frac{2\pi}{t_{res}}t\right)\right] + \left[V_{OUT}(t_0)e^{-t/T_{RC}}\right] \tag{6.10}$$

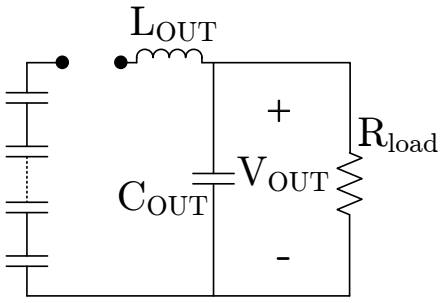
$$V_{OUT}(t) = \frac{Q_{load}}{2C_{OUT}}\left[1 - \cos\left(\frac{2\pi}{t_{res}}t\right)\right] + \left[V_{OUT}(t_0) - \frac{Q_{load}}{C_{OUT}}\frac{t}{t_{res}}\right] \tag{6.11}$$

By taking the first derivative of Equation (6.11), the first local minimum can be found at:

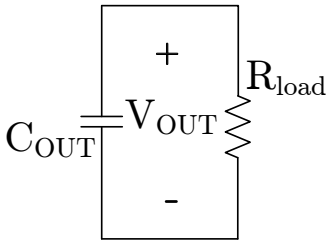
$$t_{min} = \sin^{-1}(\frac{1}{\pi})\frac{t_{res}}{2\pi} \tag{6.12}$$



(a) Charging phase (t_0 to t_1).



(b) Dead-time period (t_1 to t_2).



(c) Discharging phase (t_2 to t_3).

Figure 6.4: Output stage configuration.

and first local maximum at:

$$t_{max} = \left[\pi - \sin^{-1}(\frac{1}{\pi})\right] \frac{t_{res}}{2\pi} \tag{6.13}$$

The peak to peak voltage ripple on the output capacitor can be calculated with:

$$\Delta V_{OUT} = V_{OUT}(t_{max}) - V_{OUT}(t_{min}) \tag{6.14}$$

Using Equations (6.11), (6.12), (6.13) and (6.14), the output capacitor value can be calculated using the expression:

$$C_{OUT} = \frac{Q_{load}}{2\pi\Delta V_{OUT}} \left[2\sqrt{\pi^2 - 1} - \pi + 2\sin^{-1}(\frac{1}{\pi})\right] \tag{6.15}$$

where ΔV_{OUT} is the desired peak to peak voltage ripple on the output capacitor voltage.

6.3 Inductor Sizing

The inductor is tailored such that the resonance in all configuration states S and $\overline{S}$ is $t_{res}/2$. It is important to note that, unlike the capacitors, each inductor is used only during one sub-period, S or $\overline{S}$. The equations are derived based on the L-C configuration for each state. A resistance, labelled R_{Ln}, in series with the inductor is included in the analysis. It is intended to model various resistances present in the system including inductor, IGBT, diode and wire losses.

6.3.1 Stage 1 to N

For stage 1 to N, the circuit equivalent model is simply composed of an equivalent capacitance, the inductance and a resistance. This resistance introduces a damping factor ζ in the system [76, 77]. More specifically, the resonance frequency can be calculated using:

$$\omega_{res} = \omega_0 \sqrt{1 - \zeta^2} \tag{6.16}$$

where ω_0 is the undamped natural frequency calculated by,

$$\omega_0 = \frac{1}{\sqrt{L_n C_{eq-n}}} \tag{6.17}$$

where L_n is the inductor and C_{eq-n} is the equivalent capacitance of the state configuration. The damping factor ζ is calculated using:

$$\zeta = \frac{R_{Ln}}{2} \sqrt{\frac{C_{eq-n}}{L_n}} \tag{6.18}$$

where R_{Ln} is the loss resistance.

Using Equation (6.16) along with Equations (6.17) and (6.18), the inductor for stage n can be calculated using:

$$L_n = \frac{1}{8\pi^2} \frac{t_{res}^2}{C_{eq-n}} \left[1 + \sqrt{1 - \left(\frac{2\pi}{t_{res}} C_{eq-n} R_{Ln} \right)^2} \right] \tag{6.19}$$

where the equivalent capacitor for the stage 1 is:

$$C_{eq-1} = MC_1 \tag{6.20}$$

and for stages 2 to N, it is:

$$C_{eq-n} = \frac{MC_{n-1}C_n}{C_{n-1} + M^2C_n} \tag{6.21}$$

6.3.2 Output Stage

Mathematical complication arises for the computation of the output inductor L_{OUT} because the output load is modeled by a resistance R_{load}. By using Figure 6.3, the output stage is charged from t_0 to t_1. The electric charge in the series connected capacitors C_N are transferred through inductance L_{OUT} to capacitor C_{OUT} which is connected in parallel to the load resistance R_{load}. The circuit is shown in Figure 6.4(a).

In order to size the output inductor, recursive numerical computation is used to solve this third order system. By using linear state-space equations, the state configuration can be written in the form:

$$\frac{d}{dt}x(t) = [A]x(t) \tag{6.22}$$

where $x(t) = [i_{LOUT} \quad V_{CN} \quad V_{OUT}]^T$ and $[A]$ is a 3x3 time-invariant matrix obtained from the three linear ordinary differential equations associated with the state configuration S from t_0 to t_1. They are given in Equations (6.23), (6.24) and (6.25).

$$\frac{d}{dt}i_{LOUT} = \frac{1}{L_{OUT}}\{-i_{LOUT}R_{LOUT} + MV_{CN} - V_{OUT}\} \tag{6.23}$$

$$\frac{d}{dt}V_{CN} = \frac{1}{C_N}\{-i_{LOUT}\} \tag{6.24}$$

$$\frac{d}{dt}V_{OUT} = \frac{1}{C_{OUT}}\left\{i_{LOUT} - \frac{V_{OUT}}{R_{load}}\right\} \tag{6.25}$$

Therefore, matrix $[A]$ is given as:

$$[A] = \begin{bmatrix} -\frac{R_{LOUT}}{L_{OUT}} & \frac{M}{L_{OUT}} & -\frac{1}{L_{OUT}} \\ -\frac{1}{C_N} & 0 & 0 \\ \frac{1}{C_{OUT}} & 0 & -\frac{1}{R_{load}C_{OUT}} \end{bmatrix} \tag{6.26}$$

The solution for initial states, $x(t_0)$, is:

$$x(t) = e^{[A](t)}x(t_0) \tag{6.27}$$

Using Figure 6.3 as guide, the state configuration S corresponds to ($t_0 \leq t \leq t_2$). $V_{OUT}(t)$ has discharged and takes a value $V_{OUT}(t_0)$ at the beginning of the sub-period. The diode has blocked previously and, therefore, inductor current $i_{LOUT}(t_0) = 0.0$. The capacitors C_N have previously been charged in parallel to $\left(M^{N-1}V_S + 0.5\Delta V_{CN}\right)$ by stage N-1. Therefore, the initial state vector is:

$$x(t_0) = \begin{bmatrix} 0.0 \\ M^{N-1}V_S + \frac{\Delta V_{CN}}{2} \\ V_{OUT}(t_0) \end{bmatrix} \tag{6.28}$$

The initial conditions of i_{LOUT} and V_{CN} are known but the value of $V_{OUT}(t_0)$ is unknown. Its value is required in order to compute a precise value of L_{OUT}.

At time $t = t_1$, the voltage of C_{OUT} has been recharged to $V_{OUT}(t_1)$ and the diode stops conducting. The voltage for one series connected capacitor C_N has fallen to $M^{N-1}V_S - 0.5\Delta V_{CN}$. It is desirable that current $i_{LOUT}(t_1) = 0.0$. The state vector x at t_1 is:

$$x(t_1) = \begin{bmatrix} 0.0 \\ M^{N-1}V_S - \frac{\Delta V_{CN}}{2} \\ V_{OUT}(t_1) \end{bmatrix} \tag{6.29}$$

The relationship between $V_{OUT}(t_1)$ and $V_{OUT}(t_0)$ is made using remainder of state configuration S (dead-time period) and the second state configuration $\overline{S}$ where there is only the output capacitor and the load. The previously charged capacitor C_{OUT} is being discharged by the load resistance R_{load}. The well known solutions of R-C circuit in parallel are:

$$V_{OUT}(t) = V_{OUT}(t_1)e^{\frac{-t}{T_{RC}}} \tag{6.30}$$

where the time constant $T_{RC} = R_{load}C_{OUT}$ and ($t_1 \leq t \leq t_3$). The exponentially decaying output voltage $V_{OUT}(t)$ resembles a straight line in Figure 6.3 for time ($t_1 \leq t \leq t_3$). From periodicity, $V_{OUT}(t_3) = V_{OUT}(t_0)$, and using Equation (6.30) for a duration of $t_3 - t_1 = t_{dead} + 0.5t_{sw}$, Equation (6.31) is

obtained.

$$V_{OUT}(t_3) = V_{OUT}(t_0) = V_{OUT}(t_1)e^{-\frac{t_{dead}+0.5t_{sw}}{T_{RC}}} \tag{6.31}$$

By using Equation (6.27), the solution for the charging phase from t_0 to t_1 is:

$$x(t_1) = e^{[A](0.5t_{res})}x(t_0) \tag{6.32}$$

By combining Equations (6.28), (6.29), (6.31) and (6.32), it gives:

$$\begin{bmatrix} 0.0 \\ M^{N-1}V_S - \frac{\Delta V_{CN}}{2} \\ V_{OUT}(t_0)e^{\frac{t_{dead}+0.5t_{sw}}{T_{RC}}} \end{bmatrix} = e^{[A](0.5t_{res})} \begin{bmatrix} 0.0 \\ M^{N-1}V_S + \frac{\Delta V_{CN}}{2} \\ V_{OUT}(t_0) \end{bmatrix} \tag{6.33}$$

The matrix $e^{[A](0.5t_{res})}$ is a 3x3 matrix of 9 constant real numbers which are evaluated using MATLAB. Equation (6.33) yields a linear algebraic system of three equations where the unknown $V_{OUT}(t_0)$ can be found. By defining $\Gamma = e^{[A](0.5t_{res})}$, $V_{OUT}(t_0)$ is calculated as:

$$V_{OUT}(t_0) = \frac{\Gamma_{(3,2)}\left(M^{N-1}V_S + \frac{\Delta V_{CN}}{2}\right)}{e^{\frac{t_{dead}+0.5t_{sw}}{T_{RC}}} - \Gamma_{(3,3)}} \tag{6.34}$$

where $\Gamma_{(i,j)}$ is the element at location (i,j) in the matrix Γ.

The iterative design steps are:

1. Construct matrix [A], Equation (6.26), for a selected L_{OUT} value.
2. Compute $V_{OUT}(t_0)$ using Equation (6.34) and use it to create the state vector $x(t_0)$ with Equation (6.28).
3. Calculate $x(t_1)$ using Equation (6.32) and $x(t_0)$ from step 2.

The inductor current i_{LOUT} should be zero at t_1. Thus, the value of L_{OUT} is refined and iterative computations are done until the requirement is met.

6.4 Capacitor Voltage and Inductor Current

6.4.1 Capacitor Voltage

The capacitor sizing has been selected based on the approximation of the voltage with neglecting the voltage drop associated with the resistance R_{Ln}

and the dead-time impact. The approach described in Section 6.2 is adequate to select the capacitor values and then in Section 6.3 the inductor values are calculated to create the adequate resonance period. However, it is possible to refine the calculations to get an accurate value of the capacitor voltages and the peak inductor current values.

The waveform for the inductor current is shown in Figure 6.2. It has a sinusoidal shape with a peak current labelled I_{Ln}^{peak}. The voltage drop associated with this current flowing through the resistance R_{Ln} is calculated using the root-mean-square value and it gives:

$$\Delta V_{Ln} = \left(\frac{I_{Ln}^{peak}}{\sqrt{2}} \right) R_{Ln} \tag{6.35}$$

The area under the inductor current curve equals the amount of charges that is transferred and the relationship is given in Equation (6.36).

$$Q_n = \frac{t_{res}}{\pi} I_{Ln}^{peak} \tag{6.36}$$

By combining Equations (6.8), (6.35) and (6.36), ΔV_{Ln} is formulated as:

$$\Delta V_{Ln} = \frac{\pi}{\sqrt{2}\ t_{res}} M^{N-n+1} R_{Ln} Q_{load} \tag{6.37}$$

Since the voltage drop occurs at each stage transfer, the capacitor voltage at stage n is based on the cumulative drop from previous stage. For example:

$$\overline{V_{C1}} = V_S - \Delta V_{L1} \tag{6.38a}$$

$$\overline{V_{C2}} = M\overline{V_{C1}} - \Delta V_{L2} = M\left(V_S - \Delta V_{L1}\right) - \Delta V_{L2} \tag{6.38b}$$

A general expression which includes the cumulative drop is given Equation (6.39).

$$\overline{V_{Cn}} = M^{n-1} V_S - \Delta V_{Ln} - M\Delta V_{Ln-1} - ... - M^{n-1}\Delta V_{L1} \tag{6.39}$$

With Equation (6.37), the average capacitor voltage becomes:

$$\overline{V_{Cn}} = M^{n-1} V_S - \frac{\pi}{\sqrt{2}\ t_{res}} Q_{load} \Upsilon_n \tag{6.40}$$

where Υ_n is the cumulative parameter defined as:

$$\Upsilon_n = \left[M^{N-n+1}R_{Ln} + M^1 M^{N-(n-1)+1}R_{L(n-1)} + ... + M^{n-1}M^N R_{L1}\right] \quad (6.41)$$

Similarly for the output voltage,

$$\overline{V'_{OUT}} = M^N V_S - \frac{\pi}{\sqrt{2}\ t_{res}} Q_{load}\Upsilon_{OUT} \quad (6.42)$$

with,

$$\Upsilon_{OUT} = \left[R_{LOUT} + M^2 R_{L(n-1)} + ... + M^{2N}R_{L1}\right] \quad (6.43)$$

However, the output capacitor is also affected by the dead-time period as shown in Figure 6.3 and discussed in Section 6.3.2. Therefore, Equation (6.42) needs to be multiplied by $e^{(-t_{dead}/R_{load}C_{OUT})}$ obtained from Equation (6.30). It is important to note that only the output voltage is affected by the dead-time period. Therefore, the average output voltage is calculated with:

$$\overline{V_{OUT}} = e^{\frac{-t_{dead}}{R_{load}C_{OUT}}}\overline{V'_{OUT}} \quad (6.44)$$

Substituting Equation (6.5) for Q_{load} and using Equation (6.42), Equation (6.44) becomes:

$$\overline{V_{OUT}} = \frac{M^N V_S}{\left[e^{\frac{+t_{dead}}{R_{load}C_{OUT}}} + \frac{\pi}{\sqrt{2}}\frac{t_{sw}}{t_{res}}\frac{1}{R_{load}}\Upsilon_{OUT}\right]} \quad (6.45)$$

An update value for Q_{load} can be calculated using Equation (6.5) along with the updated output voltage from Equation (6.45):

$$\overline{Q_{load}} = \frac{\overline{V_{OUT}}}{R_{load}}t_{sw} \quad (6.46)$$

The updated charge $\overline{Q_{load}}$ can be substituted back in Equation (6.40) for an improved calculation of the capacitor voltage as given in Equation (6.47).

$$\overline{V_{Cn}} = M^{n-1}V_S - \frac{\pi}{\sqrt{2}}\frac{t_{sw}}{t_{res}}\frac{\overline{V_{OUT}}}{R_{load}}\Upsilon_n \quad (6.47)$$

Similarly for the capacitor voltage ripple with Equation (6.9), it gives Equation

(6.48).

$$\overline{\Delta V_{Cn}} = \frac{\overline{V_{OUT}}}{R_{load}} \frac{M^{N-n}}{C_n} t_{sw} \tag{6.48}$$

Because of the presence of the resistance R_{LOUT}, a precise evaluation of the output capacitor voltage ripple cannot be done using an updated version of Equation (6.15). Instead, iterative calculations using Equation (6.27) is used to find local minimum and local maximum and then to evaluate the voltage ripple.

6.4.2 Inductor Peak Current

The peak current of the inductor is also calculated by making use of the sinusoidal shape of the inductor current. By using Equations (6.8), (6.36) and (6.46), the peak current can be calculated using:

$$I_{Ln}^{peak} = M^{N-n+1} \frac{t_{sw}}{t_{res}} \frac{\pi}{R_{load}} \overline{V_{OUT}} \tag{6.49}$$

where n is stage number and, for L_{OUT}, n is assigned N+1.

6.5 Prototype Design

The design of a 5kW prototype is described using the above procedures. The prototype has been constructed and tested and it is discussed in the next chapter. The input voltage, V_S, is 110V and the converter has 2 stages with 2 capacitors per stage (N=2, M=2) as shown in Figure 6.5. The load, R_{load}, is 38.72Ω and the converter operates at 1949Hz with a conservative dead-time of 5μ seconds.

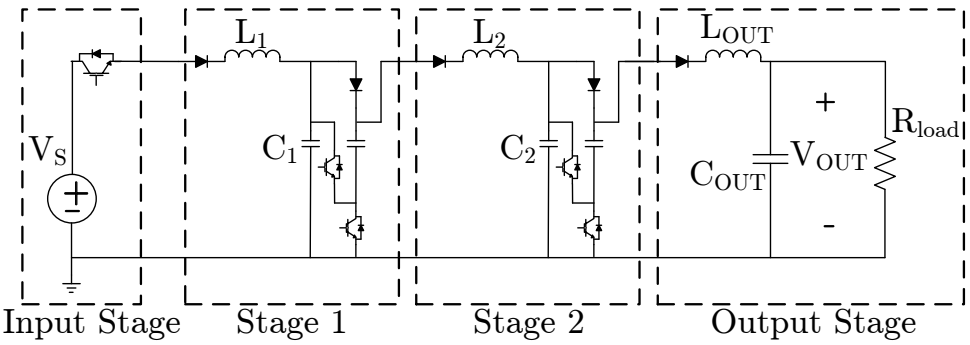


Figure 6.5: Prototype configuration with N=2 and M=2.

Table 6.1: Design parameters.

Capacitor				
	Design		**Selection**	
	voltage ripple [V]	capacitor value [uF]	capacitor value [uF]	voltage ripple [V]
C_1	33	353	360	32.4
C_2	33	176	160	36.4
C_{OUT}	15	214	230	14.0

Inductor		
	Design and selection	
	inductor value [uH]	resistance [Ω]
L_1	8.8	0.01
L_2	55.6	0.01
L_{OUT}	97.0	0.01

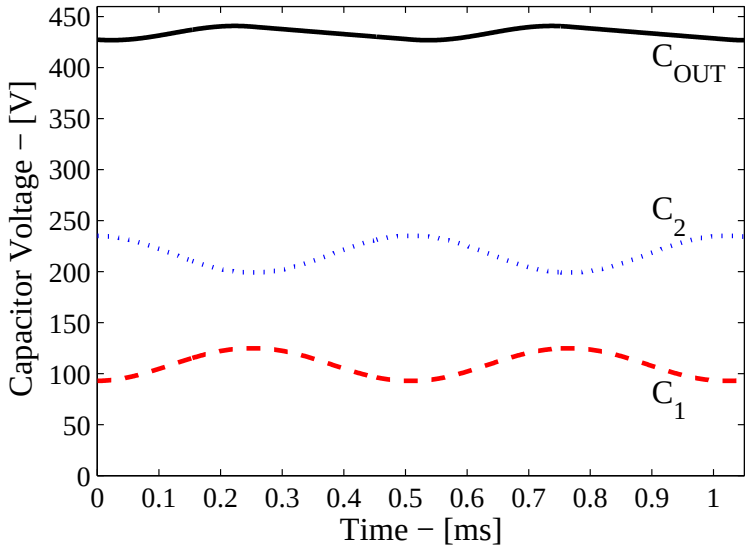
The capacitors are selected based on the initial desired voltage ripple shown under "design" in Table 6.1. However, only a discrete range of capacitor values are commercially available which forces designers to have certain margin in the selection process. A higher capacitor value will reduce the voltage ripple but it will affect the inductor design by increasing its required value. Using Equations (6.9) and (6.15), the computed capacitor design values are listed in Table 6.1. The closest commercially available capacitors are listed beside it. The voltage ripple is then calculated back based on the selected commercially available capacitor value.

By using Equation (6.19) with Equations (6.20) and (6.21), the inductor value for L_1 and L_2 are calculated and they are listed under "design" in Table 6.1. The output inductor L_{OUT} is calculated using the iterative procedure described earlier.

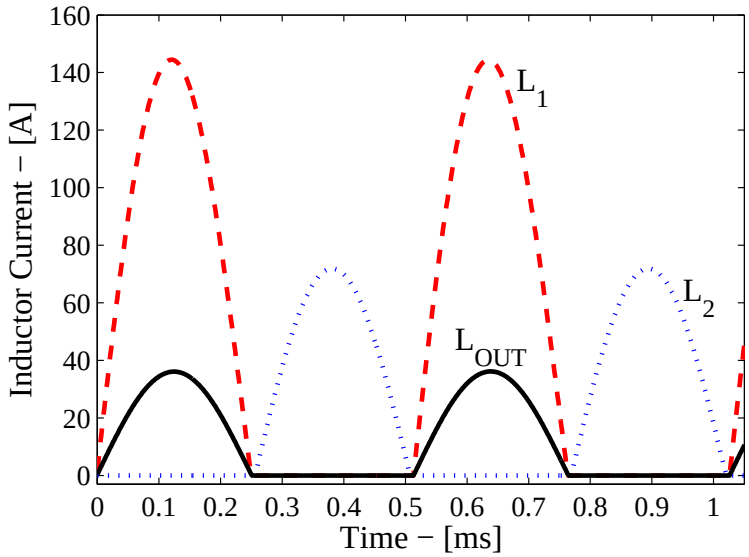
Table 6.2 lists capacitor voltages and inductor currents calculated using equations from Section 6.4. The average capacitor voltages are calculated using Equations (6.45) and (6.47). The capacitor voltage ripple is calculated using Equation (6.48) and the iterative approach discussed for $\overline{\Delta V_{COUT}}$. The peak currents are also calculated for all the inductor using Equation (6.49).

6.5.1 Simulation Results

The converter has been simulated in PSCAD-EMTDC software package, an industry-grade software for high voltage power electronic research, using the



(a) Capacitor voltages.



(b) Inductor currents.

Figure 6.6: Simulation results for the prototype design.

parameters obtained from the prototype design. The capacitor voltages and the inductor currents are shown in Figure 6.6. The inductor currents, shown in Figure 6.6(b), show adequate resonance and the current reaches zero before the end of each the switching period. The dead-time requirement is respected with dead-time of 6μs for I_{L1} and 5μs for I_{L2} and I_{LOUT}.

In Tables 6.2, the capacitor voltages and the peak currents are noted under the "simulation results" column and the difference with the design value is shown. The average capacitor voltages are within 0.5% of the expected value from the design. By including the losses and the dead-time, the dc voltage obtained from the simulation is 3.97 as opposed to the theoretical 4. The capacitor voltage ripple is very accurate for the all stages with results within 0.1V. Regarding the inductor peak current, it is also close to the design value with difference within 1%. A peak current of 145A is expected for the input stage in the prototype construction. The peak current decreases by a factor of 2 for each following stages.

Table 6.2: Capacitor voltages and inductor currents.

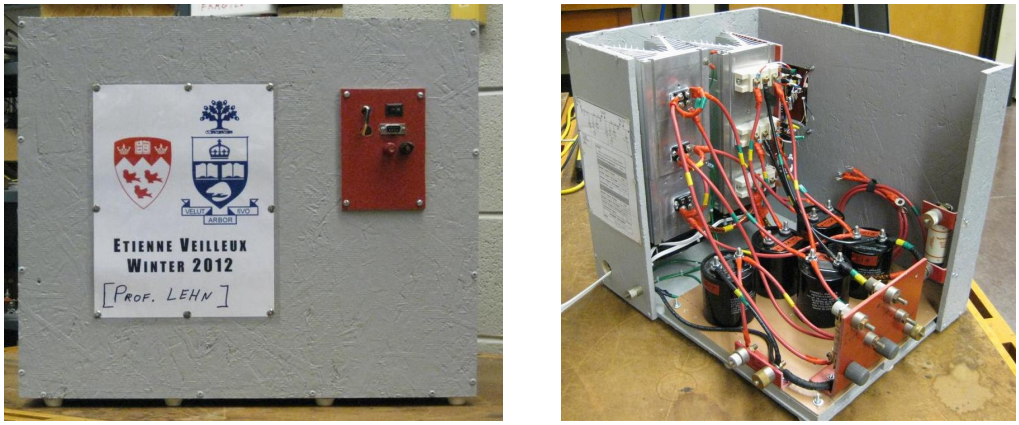
Average Capacitor Voltage			
	Expected from design	Simulation results	difference
$\overline{V_{C1}}$ [V]	109.0	109.2	0.2%
$\overline{V_{C2}}$ [V]	217.5	216.9	0.3%
$\overline{V_{COUT}}$ [V]	434.4	434.0	0.1%
Ripple Capacitor Voltage			
	Expected from design	Simulation results	difference
$\Delta\overline{V_{C1}}$ [V]	32.0	32.0	0.0%
$\Delta\overline{V_{C2}}$ [V]	36.0	36.0	0.0%
$\Delta\overline{V_{COUT}}$ [V]	14.0	14.1	0.7%
Inductor Peak Current			
	Expected from design	Simulation results	difference
I_{L1}^{peak} [A]	143.8	144.6	0.6%
I_{L2}^{peak} [A]	71.9	71.9	0.0%
I_{LOUT}^{peak} [A]	35.9	36.2	0.8%

6.6 Chapter Summary

This chapter has presented a design approach for the Marx converter topology. The design considers the resistances of the components by modeling them as an added resistance which affects the resonance. It also introduces a dead-time requirement in the operation of the converter. The design of the prototype is used to validate the design guidelines. The prototype is rated for 5kW with 2 stages and 2 capacitors per stage. A good agreement is observed between the design and the results obtained from the simulation.

Chapter 7

Marx DC-DC Converter: Experimental Results



(a) Front side of converter.

(b) Back side of converter.

Figure 7.1: Prototype converter.

A 5kW prototype converter, shown in Figure 7.1, has been constructed to acquire experimental results. The experiment has been carried in the power laboratory at University of Toronto under the supervision of Professor Lehn. The prototype has been constructed based on the design previously obtained in Section 6.5 of Chapter 6. However, the inductor has been manually wounded to respect the resonance period on the setup itself. The discrepancy in the inductor values between the design and the experiment comes from the imperfection of the components which influences the operation of the converter. For example, the capacitors have a manufacture tolerance from its rated capacitance value and the switches have forward voltage drops as well as additional

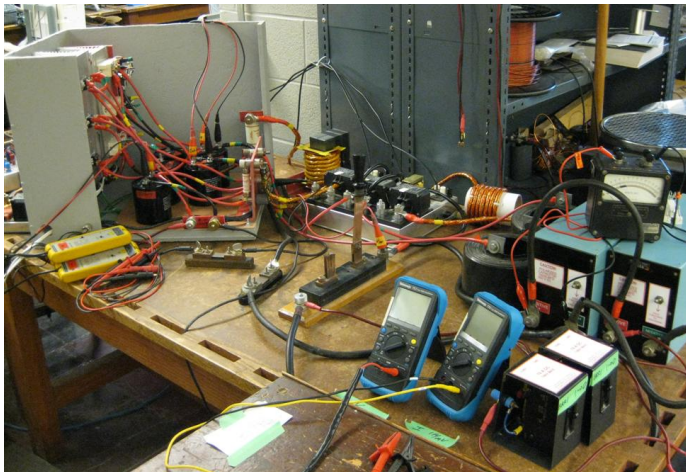


Figure 7.2: Experimental setup for 5kW prototype converter with two stages and two capacitors per stage.

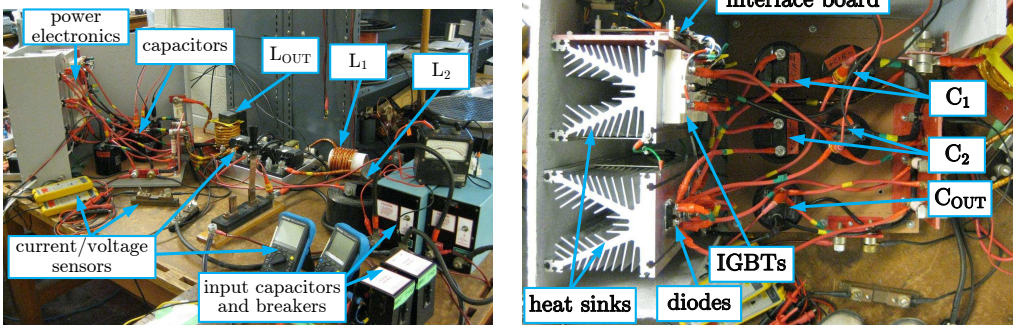
resistances that have not been modeled. The experimental setup is shown in Figure 7.2. The prototype has been constructed in two steps: one stage and then upgraded to two stages. For each step, the converter has been fully tested and results were acquired. The complete lists of components as well as detailed drawings are included in Appendix D which also shows additional pictures and details about the prototype.

In this chapter, the construction process is discussed briefly to familiarize readers on the work. Then, the 1-stage converter is introduced along with experimental results. Finally, the 2-stage converter is presented. The amplification gain, the efficiency and the influence of the switching frequency are among the factors that are analyzed.

7.1 Setup Assembly

The preliminary work consists of designing and simulating the converter as described in Chapter 6. From the simulation results, the components can be selected accordingly. For example, the input switch connected to inductor L_1 is expected to withstand a peak current of as much as 145A. This is not negligible and failure to consider it would result in catastrophic destruction of the switching device. Therefore, IGBT of rating 200A/600V has been selected to give adequate safety margin.

An important consideration for power electronics components is heat dissipation. To do so, the switching devices need to be installed on heat sinks



(a) Prototype converter with inductor and measurement devices.

(b) Top view of prototype converter with capacitors and power electronics.

Figure 7.3: Details on experimental setup.

to avoid over-heating. Different models are offered depending on the type of cooling [78]. The most common is air-cooling with natural or forced convection. In this project, an air-cooled extrusion heat sink with forced convection is used and it is shown in the picture of Figure 7.3(b).

The triggering of the IGBTs is done through a gate driver interface board. The gate driver interface board has to receive small gating signals from an external controller and to send the high current triggering pulses to the IGBTs. The gate driver interface board is composed of the gate drivers, which amplify and isolate the gating signal for each IGBT, and the external circuitry to interface. For this project, a 6-channel gate driver has been purchased which provides the required isolation and good performance for triggering the IGBTs. It is still necessary to design and construct the interface board to supply power and to set threshold values for dead-time and for levels of protection for the IGBTs.

A custom-made enclosure has been constructed around the platform upon which the prototype is built so as to provide necessary safety. One of the objective in the design is to minimize the distance between the power electronic components and the capacitors. The inductance of long wire with the capacitor can create resonance which can impact the behaviour of the power electronic component. The items located inside the enclosure are: gate driver interface board, power electronic switches installed on heat sinks, capacitors and fuses. The components connected outside are: inductors, current sensors and load.

Prior to operating the converter, a start-up procedure has been determined and tested in simulation software. The start-up procedure is intended to pre-

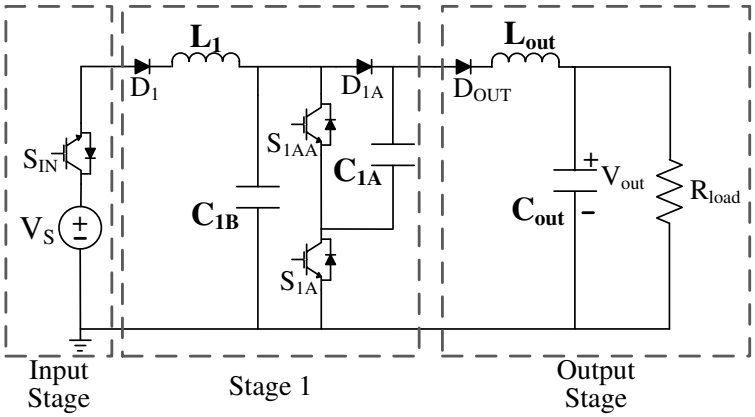


Figure 7.4: 1-Stage prototype configuration.

vent inrush current which can damage the prototype. The procedure consists of gradually increasing the input voltage so as to gradually charge the capacitors.

In Section D.1 of Appendix D, detailed schematics are included for the 1-stage and 2-stage configuration. It has a listing of parts, electrical circuit diagrams and construction drawings. The dimensions of the box is also included as well as additional information such as the start-up procedure. Figure 7.3 shows the arrangement with identification of some key components. Additional pictures can be found in Section D.2 of Appendix D.

7.2 Prototype Converter: 1-Stage

The first step is to build the prototype with one stage only. The schematic of the converter is shown in Figure 7.4 and the main parameters are listed in Table 7.1. The operation in steady-state at rated power is observed and the performance under different loads is studied.

7.2.1 Steady-State at Rated Power

The converter is operated close to the rated power of 5kW. Some measurements are given in Table 7.2. The waveforms of the inductor currents and the capacitor voltages are shown in Figure 7.5. The dc amplification gain of the prototype is 1.82 as opposed to the theoretical gain of 2. The voltage drop associated with the IGBTs and the diodes explains in part that discrepancy. A voltage drop of 1V from the input switch S_{IN} is almost a 1% drop right at

Table 7.1: 1-Stage prototype: parameters.

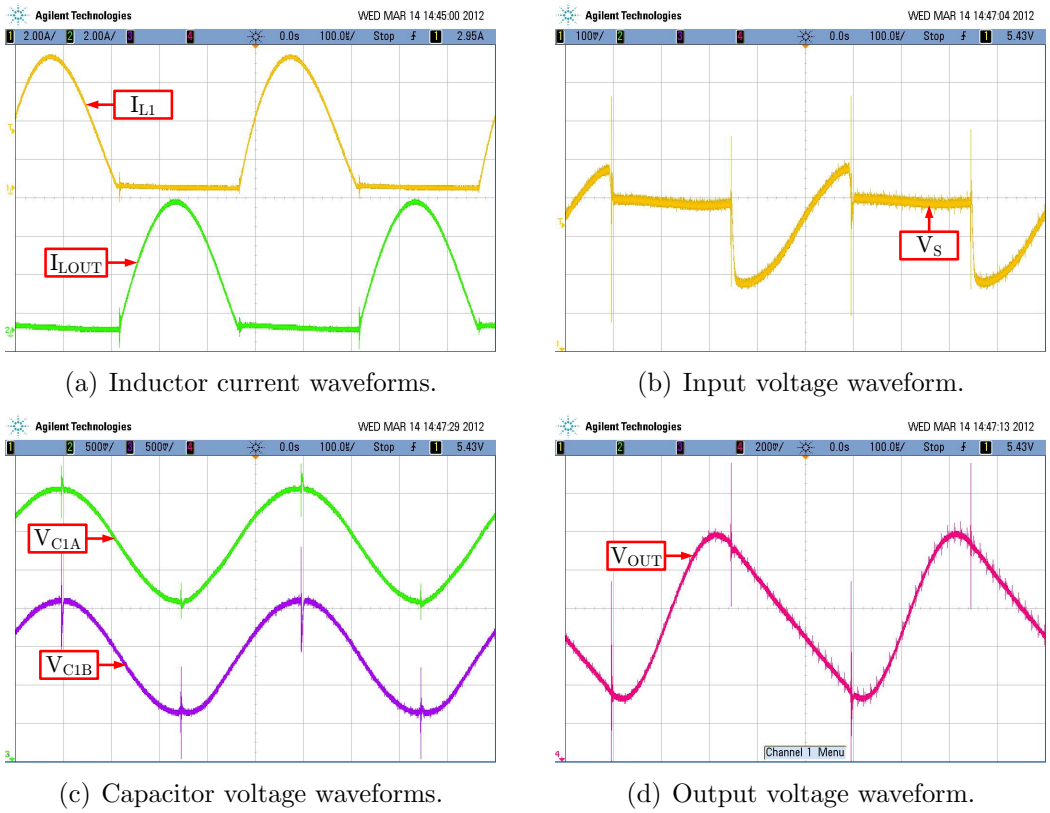
Parameters	**Value**
Input voltage V_S [V]	110
Switching frequency [Hz]	2000
Dead-time t_{dead} [us]	4.5
Number of stage N	1
Capacitor per stage M	2
C_{1A},C_{1B} [uF]	366 / 366
C_{OUT} [uF]	233
L_1 / R_{L1} [uH / mΩ]	4.9 / 3
L_{OUT} / R_{LOUT} [uH / mΩ]	50 / 4
Load R_{LOAD} [Ω]	9.3

Table 7.2: 1-Stage prototype: steady-state measurements.

Measurements	**Value**
Average input voltage V_S [V]	110.0
Average capacitor voltage V_{C1B} [V]	104.6
Average output voltage V_{OUT} [V]	200.6
Average input power P_{IN} [kW]	4.72
Average output power P_{OUT} [kW]	4.33
Peak current I_{L1}^{peak} [A]	137.4
Peak current I_{LOUT}^{peak} [A]	66.9

the beginning in this prototype. By considering all the switches in the circuit, it certainly influences the overall dc gain. However, by operating at higher voltage ratings, the forward voltage drops associated with the switching devices would be mitigated and it would be expected to have a lower impact on the dc gain. Nevertheless, the amplification has been demonstrated by having the average voltage at 105V at stage 1 and at 201V for the output capacitor. The inductor peak currents are 137A and 67A for L_1 and L_{OUT}, respectively.

The inductor currents are shown in Figure 7.5(a). The two complementary conducting periods for the inductors are clearly shown. The input voltage, shown in Figure 7.5(b), is not an ideal constant voltage source. In this experiment, the dc voltage source is a dc generator and it is loaded only when stage 1 is charging ($S = 1$). Therefore, it has to supply all the energy only half the switching period so when it is connected, a large amount of power is required. As a result, a voltage drop is experienced at the input even with the insertion of two large capacitors at the input to minimize this behaviour. The



(a) Inductor current waveforms.

(b) Input voltage waveform.

(c) Capacitor voltage waveforms.

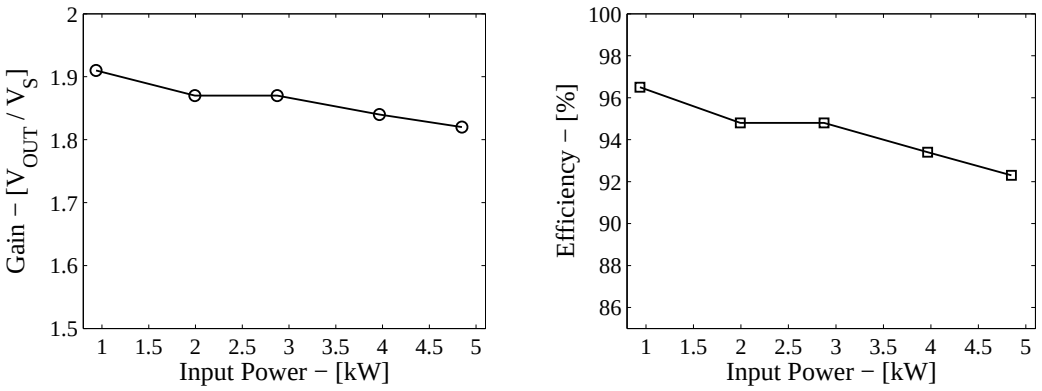
(d) Output voltage waveform.

Figure 7.5: Experimental results for 1-stage prototype at 5kW.

charging/discharging of the two converter capacitors, C_{1A} and C_{1B}, is shown in Figure 7.5(c). It is important to note that only the voltage ripples of each capacitor are shown. The offset between the two waveforms have been manually adjusted to display both distinctly. Similarly, the output voltage, shown in Figure 7.5(d), depicts the predicted waveform of the charging phase and the almost linear discharge. The results obtained from the 1-stage converter experiment confirms the behaviour of the converter. The waveforms are as expected and the designed voltage amplification is obtained.

7.2.2 Gain and Efficiency

The converter performance under different load has been tested. The converter gain and efficiency are shown in Figures 7.6(a) and 7.6(b), respectively. At low power, the gain is around 1.91 and it decreases to 1.82 at rated power. The reduction is in the order of 5%. Similarly, the efficiency gradually decreases from 96.5% to 92.3%. As the power increases, the current is higher which creates larger voltage drops and higher losses which explains the decrease of



(a) Gain at different operating points. (b) Efficiency at different operating points.

Figure 7.6: 1-Stage prototype: gain and efficiency.

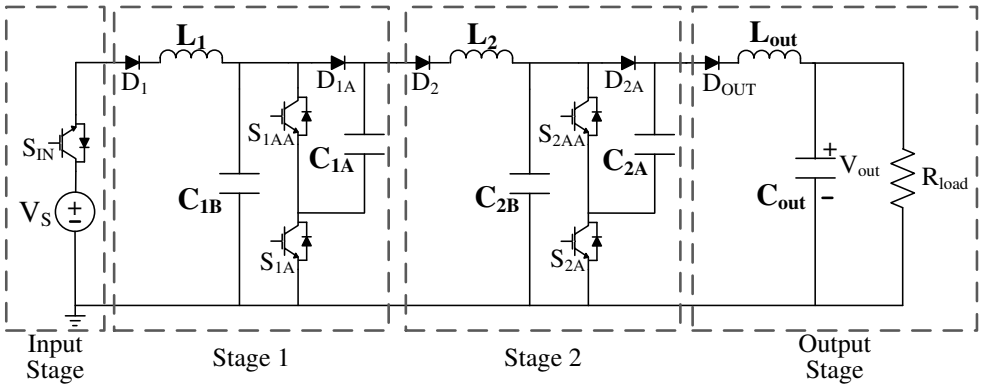


Figure 7.7: 2-Stage prototype configuration.

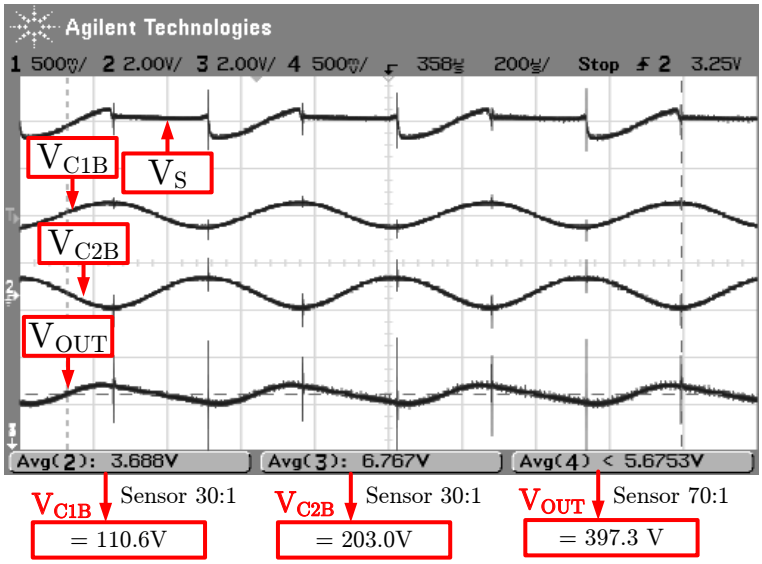
the gain and the efficiency.

7.3 Prototype Converter: 2-Stage

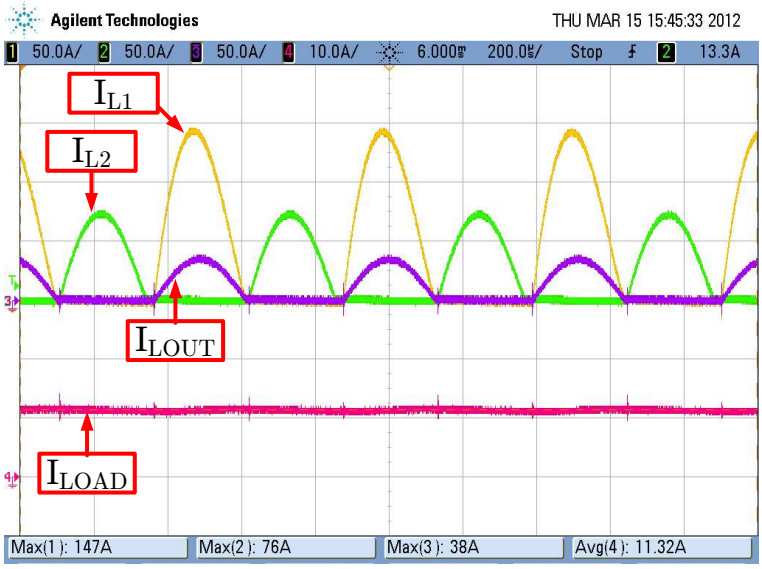
After the successful operation of the 1-stage configuration, the prototype is upgraded to two stages as shown in Figure 7.7. The main parameters are listed in Table 7.3. The operation in steady-state at rated power is analyzed as well as the gain and efficiency under different loads are also studied. In addition, the performance of the converter under a load step change and the operation at various switching frequency is observed in this section.

7.3.1 Steady-State at Rated Power

The operation of the 2-stage converter at 5kW is studied and some measurements are listed in Table 7.4. The waveforms of the capacitor voltages and



(a) Voltage waveforms (manual adjustment of the y-axis scale and offset for each signal).



(b) Inductor current waveforms.

Figure 7.8: Experimental results for 2-stage 5kW prototype.

Table 7.3: 2-Stage prototype: parameters.

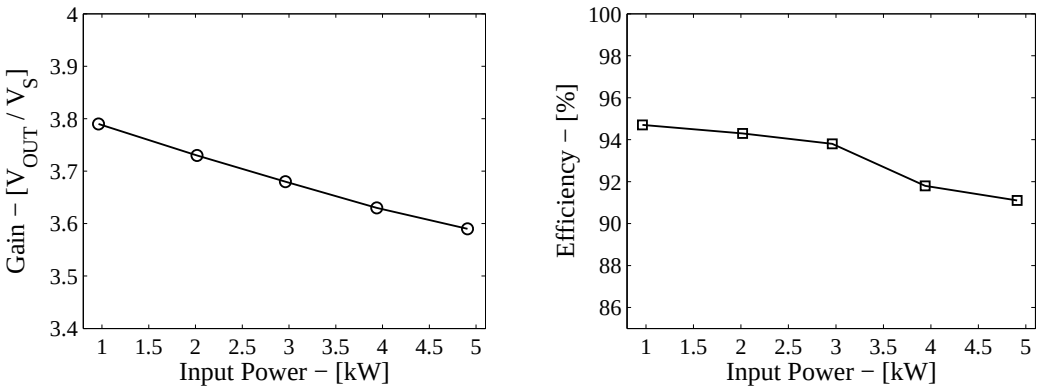
Parameters	**Value**
Input voltage V_S [V]	110
Switching frequency [Hz]	1949
Dead-time t_{dead} [us]	4.5
Number of stage N	2
Capacitor per stage M	2
C_{1A},C_{1B} [uF]	366 / 366
C_{2A},C_{2B} [uF]	151 / 152
C_{OUT} [uF]	233
L_1 / R_{L1} [uH / mΩ]	4.9 / 3
L_2 / R_{L2} [uH / mΩ]	50 / 4
L_{OUT} / R_{LOUT} [uH / mΩ]	95.3 / 4
Load R_{LOAD} [Ω]	34.7

Table 7.4: 2-Stage prototype: steady-state measurements.

Measurements	**Value**
Average input voltage V_S [V]	108.8
Average capacitor voltage V_{C1B} [V]	101.5
Average capacitor voltage V_{C2B} [V]	197.4
Average output voltage V_{OUT} [V]	389.9
Average input power P_{IN} [kW]	4.63
Average output power P_{OUT} [kW]	4.38
Peak current I_{L1}^{peak} [A]	146.8
Peak current I_{L2}^{peak} [A]	74.4
Peak current I_{LOUT}^{peak} [A]	36.1

inductor currents are shown in Figure 7.8. The dc amplification gain of the prototype is 3.58 as opposed to the theoretical gain of 4. The amplification has been demonstrated by having the average voltage at 102V at stage 1, 197V at stage 2 and at 390V for the output capacitor. Figure 7.8(a) shows that when C_{2B} is charging, C_{1B} is discharging and vice-versa. The input voltage V_S and the output voltage V_{OUT} have the waveforms similar to Figures 7.5(b) and 7.5(d) respectively.

Figure 7.8(b) shows the current waveforms. The inductor currents of the odd-numbered stages (I_{L1} and I_{LOUT}) are shown to occur at the same instant. The even-numbered stage current (I_{L2}) flows in the complementary period. The inductor currents reach zero before the end of the next switching event in



(a) Gain versus power operating point.

(b) Efficiency versus power operating point.

Figure 7.9: 2-Stage prototype: gain and efficiency.

all three cases. The peak currents are 147A, 74A and 36A for L_1, L_2 and L_{OUT}, respectively. Their values are close to the expected values obtained from the design done in Section 6.5 of Chapter 6.

7.3.2 Gain and Efficiency

The converter gain and efficiency for different load have been tested and the results are shown in Figure 7.9. The converter gain decreases more linearly than for the 1-stage observation. The converter gain decrease by 5% when comparing the gain under low and rated load condition. The efficiency is at 95% at low load and it reaches 91% at full load. Nevertheless, the efficiency is above 90% which is good according that the converter is a prototype and it has not been optimized to minimize losses.

7.3.3 Load Step Change

A disturbance has been applied to the system to evaluate its stability. A step change has been performed at the output load and the response is shown in Figure 7.10. The load has been decreased from 66Ω to 36Ω which represents an increase in power from 2.8kW to 4.9kW. From Figure 7.10, the output current I_{LOAD} has a step increase corresponding to the step increase in the load. The large drain in current from the output capacitor decreases the output voltage V_{OUT}. It takes two cycles for the change to appear at the input current, I_{L1}. The delay corresponds to the number of stages in the system.

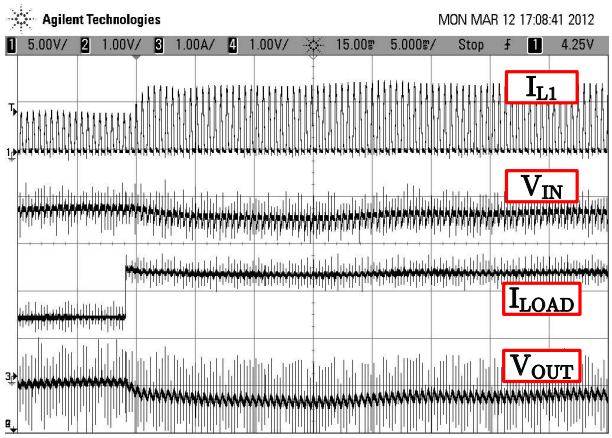
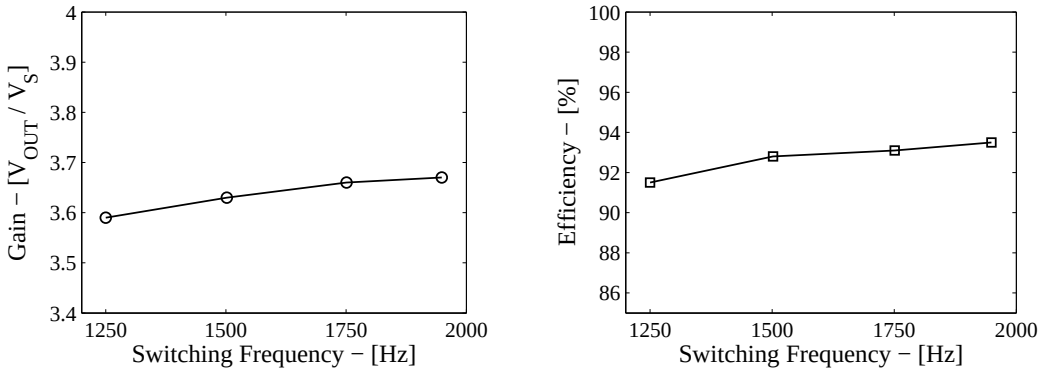


Figure 7.10: 2-Stage prototype: load step change.



(a) Gain versus operating frequency.

(b) Efficiency versus operating frequency.

Figure 7.11: 2-Stage prototype: different switching frequencies.

The system settles to steady-state after few cycles. The subsequent low frequency ripple is more a property of the dc generator used in the experiment as the input voltage V_S. The dc generator is driven by a motor which slows down after meeting a large counter-torque from the increased load. The slowing decreases the input voltage V_S. The dynamics of the motor-generator is of no interest. The principal objective of the test shows that the system is stable under a significant perturbation.

7.3.4 Different Switching Frequencies

The operation under different switching frequencies has been explored. The performance of the converter, operating at around 3kW, is displayed in Figure 7.11. The figure shows the converter gain and efficiency for various switching frequencies. By reducing the switching frequency, the switching period be-

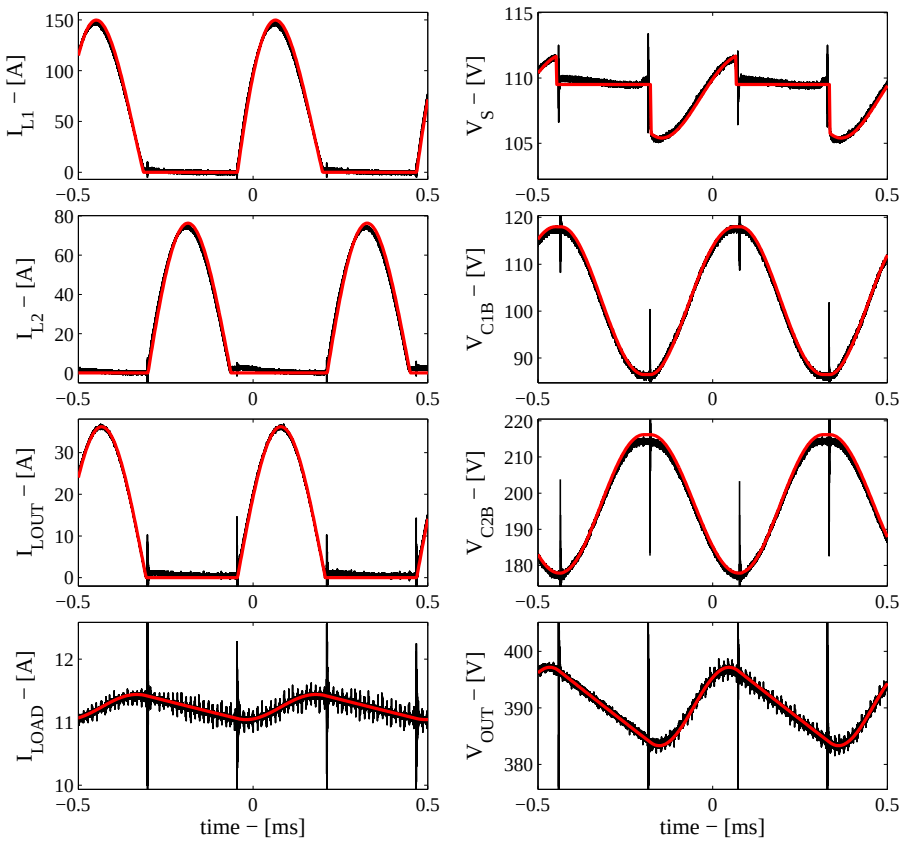


Figure 7.12: Simulation results for accurate model of the prototype.

comes longer but the resonance period remains the same. As a result, a longer non-conducting period is created. The converter gain slightly decreases as the switching frequency decreases. This is to be expected since the charging period remains the same but load remains connected for a longer duration. The efficiency of the converter is also slightly influenced by the switching frequency. This test demonstrates stable operation under lower switching frequency which results in longer non-conducting period. This aspect is analyzed further in Chapter 8.

7.4 Simulation Model

A detailed model has been developed in PSCAD-EMTDC software package to reproduce as closed as possible the laboratory results. The modelling has been done based on measurements of some components and on fitting the components that are not measurable to match experimental results. The complete list of parameters are given in Section D.3 of Appendix D. There is a very

good agreement between the simulation model and the recorded data. The validity of the model has been compared with the steady-state operation as shown in Figure 7.12. The errors are within 1% for most signals and the main discrepancy is located in the peak inductor current. Some of the discrepancies can be explained by the non-linear behaviour of the components with respect to thermal impact. Nevertheless, the accurate model could be used for future study of the prototype.

7.5 Chapter Summary

In this chapter, a 5kW prototype converter has been presented. Initially, the converter has been tested for one stage before upgrading to the 2-stage configuration. The 2-stage configuration has two capacitors per stage for a theoretical dc voltage gain of four. Operation under different loads, different switching frequency and load step change are among the tests performed on the prototype. The prototype is stable and it amplifies the dc voltage as expected. The laboratory experiment is very successful with respect to the concept and design of the converter.

Chapter 8

Marx DC-DC Converter: Stability Analysis and Parameter Ratings

This chapter presents the stability analysis of the Marx converter. Simulation and experimental results have shown the converter to be stable but it has been observed only for a short period of time. The stability analysis tests the system for $t \to \infty$ with the objective to determine if the system is asymptotically stable [76]. Firstly, the operation under continuous conduction mode is explored and followed by the discontinuous conduction mode. In both modes, it is shown that the converter is stable.

The second part of the chapter presents a guide to the evaluation of the parameter ratings. Equations are derived which give good estimations of the component ratings for a Marx converter of N stages with M capacitors per stage. The components evaluated are: IGBTs, diodes, inductors and capacitors.

8.1 Stability Analysis

A stability analysis is performed to evaluate the dynamic behaviour of the system. The analysis is similar to sampled-data approach used in control theory since the converter operates in repetitive sequence of states of equal duration [76]. In each state configuration, or sub-period, the system is composed of a set of linear equations.

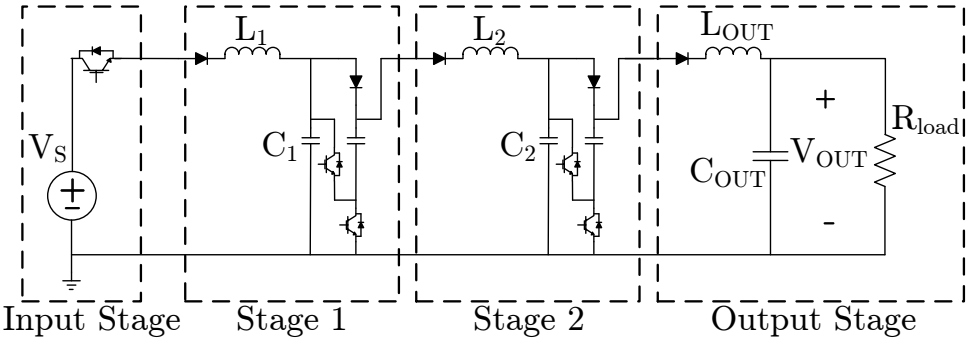


Figure 8.1: Prototype configuration with N=2 and M=2.

When the inductor current reaches zero exactly at the end of the switching half-period, the converter is operating at the boundary of the continuous conduction mode and the discontinuous conduction mode [40]. In this thesis, it is defined that the converter operating at that boundary is identified as operating in continuous conduction mode.

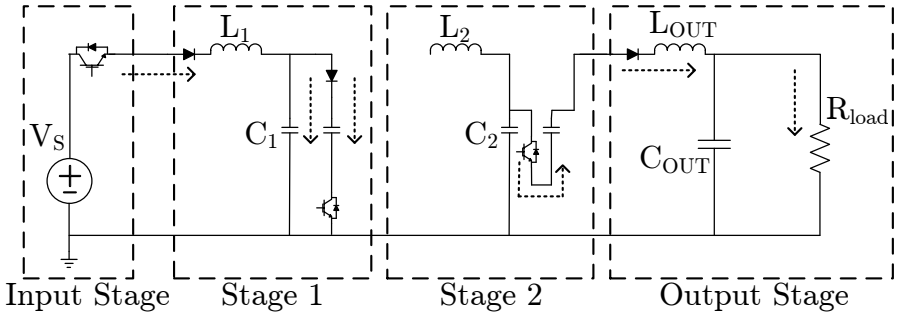
The discontinuous conduction mode is defined as when the inductor current reaches zero before the end of the switching half-period. The discontinuous conduction mode has been observed previously by introducing the dead-time requirement. The stability in this mode is analyzed in Section 8.1.3.

The analysis is derived for the same configuration as for the prototype (N=2, M=2), shown in Figure 8.1, but the methodology can applied to any configuration with N stages and M capacitors per stage. The parameters used are the same as the model in Section 6.5 of Chapter 6. The inductor resistances are considered and it is assumed that the system is in steady-state.

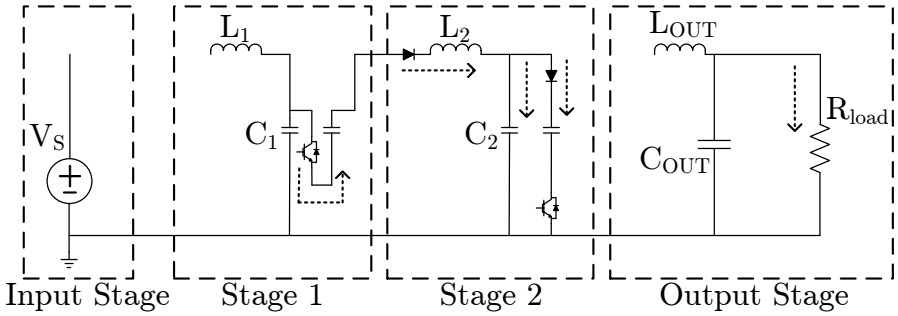
8.1.1 Continuous Conduction Mode of Operation

The first state is identified by the logic state S and the IGBTs are activated so that configuration is shown in Figure 8.2(a). The second state configuration is identified by logic state $\overline{S}$ and it is shown in Figure 8.2(b). In both Figures 8.2(a) and 8.2(b), the conducting switches are shown while the non-conducting ones are omitted.

The two state configurations, S and $\overline{S}$, can be expressed by linear ordinary differential equations in the state-space representation $\dot{x} = Ax + Bu$ where $x = [\ i_{L1}\ v_{C1}\ i_{L2}\ v_{C2}\ i_{LOUT}\ v_{COUT}]^T$ and $u = V_S$. Each state configuration has different matrices A and B. The solution to the differential equations has the



(a) Configuration with logic state S.



(b) Configuration with logic state $\overline{S}$.

Figure 8.2: Converter state configurations with conducting switches displayed.

form:

$$x(t) = Ux(t_0) + Vu(t_0) \tag{8.1}$$

where,

$$U = e^{A(t-t_0)} \tag{8.2}$$

and

$$V = A^{-1}\left(e^{A(t-t_0)} - I\right)B \tag{8.3}$$

The matrix A needs to be non-singular to compute its inverse in Equation (8.3). However, the inductors are used only during one of the two state configurations of the converter operation. As a result, the matrix A becomes singular because of zero rows/columns associated with the current i_L of the disconnected inductor. To encounter this computation issue, the inverse is done by using the Moore-Penrose generalized inverse, also known as pseudoinverse, which makes use of the least squares solution of the set of equations [79]. In this situation, the solution is equivalent to matrix manipulations of eliminating zero vectors prior to invert, followed by reconstructing from the inverted matrix to match initial matrix size.

The matrix notation for the system in state configuration S is A_1, B_1, U_1

and V_1. Similarly for state configuration $\overline{S}$, matrices have notation A_2, B_2, U_2 and V_2. The operation of the converter is divided into two states of equal duration $t_{sw}/2$. Starting in state configuration S at t=0, the solution is:

$$x\left(\frac{t_{sw}}{2}\right) = U_1 x(0) + V_1 u(0) \tag{8.4}$$

where $U_1 = e^{A_1 \frac{t_{sw}}{2}}$ and $V_1 = A_1^{-1}\left(e^{A_1 \frac{t_{sw}}{2}} - I\right) B_1$. Then, from $t = t_{sw}/2$ to $t = t_{sw}$, the converter is in state configuration $\overline{S}$. It gives:

$$x\left(t_{sw}\right) = U_2 x\left(\frac{t_{sw}}{2}\right) + V_2 u\left(\frac{t_{sw}}{2}\right) \tag{8.5}$$

where $U_2 = e^{A_2 \frac{t_{sw}}{2}}$ and $V_2 = A_2^{-1}\left(e^{A_2 \frac{t_{sw}}{2}} - I\right) B_2$. From Figure 8.2(b), it is clear that the input voltage source V_S is disconnected during $\overline{S}$. Therefore, the matrix V_2 is zero because B_2 is a zero vector. Therefore, Equation (8.5) is simplified and by combining with Equation (8.4), it gives:

$$x\left(t_{sw}\right) = U_2 U_1 x(0) + U_2 V_1 u(0) \tag{8.6}$$

By defining $\psi = U_2 U_1$ and $\Phi = U_2 V_1$, Equation (8.6) is rewritten as:

$$x\left(t_{sw}\right) = \psi x(0) + \Phi u(0) \tag{8.7}$$

A general solution is obtained with $q = nt_{sw}$, n being an integer number:

$$x(q+1) = \psi^{q+1} x(0) + \psi^q \Phi u(0) + \psi^{q-1} \Phi u(1) + \cdots + \Phi u(q) \tag{8.8}$$

For the case under study, the input u is the constant voltage source V_S, so Equation (8.8) is rearranged to:

$$x(q+1) = \psi^{q+1} x(0) + \left\{I + \psi^1 + \cdots + \psi^{q-1} + \psi^q\right\} \Phi V_S \tag{8.9}$$

The finite geometric series $\{I + \psi^1 + \cdots + \psi^{q-1} + \psi^q\}$ equals to [80]:

$$\sum_{n=0}^{q} \psi^n = (I - \psi)^{-1}\left[I - \psi^{q+1}\right] \tag{8.10}$$

If $q \to \infty$, the series converges if and only if $|\psi| \leq 1$. Using Equation (8.10),

Equation (8.9) becomes:

$$x(q+1) = \psi^{q+1}x(0) + (I-\psi)^{-1}\left[I-\psi^{q+1}\right]\Phi V_S \tag{8.11}$$

Stability is determined by the eigenvalues of ψ. By having the eigenvalues of ψ within the complex unit circle, the converter is stable. Even if the system is continuous within each state configuration, the analysis is referring to discrete instant or more precisely every switching period as stated for Equation (8.11). Therefore, the unit circle in the complex plane is used for stability instead of the jω-axis.

8.1.2 Example

The stability analysis is applied to the prototype model. Because this analysis considers continuous conduction mode, the duration t_{res} will be considered instead of t_{sw} because the selected t_{sw} included a dead-time segment. By doing so, the switching frequency used is 1988Hz instead of 1949Hz.

For the system in state configuration S, referring to Figure 8.2(a), the matrices A_1 and B_1 are:

$$A_1 = \begin{bmatrix} \frac{-R_{L1}}{L_1} & \frac{-1}{L_1} & 0 & 0 & 0 & 0 \\ \frac{1}{MC_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{C_2} & 0 \\ 0 & 0 & 0 & \frac{M}{L_{OUT}} & \frac{-R_{LOUT}}{L_{OUT}} & \frac{-1}{L_{OUT}} \\ 0 & 0 & 0 & 0 & \frac{1}{C_{OUT}} & \frac{-1}{C_{OUT}R_{load}} \end{bmatrix} \tag{8.12}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{8.13}$$

For state configuration $\overline{S}$, referring to Figure 8.2(b), the matrices A_2 and B_2 are:

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{M}{L_2} & \frac{-R_{L2}}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & \frac{1}{MC_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{OUT}R_{load}} \end{bmatrix} \tag{8.14}$$

$$B_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{8.15}$$

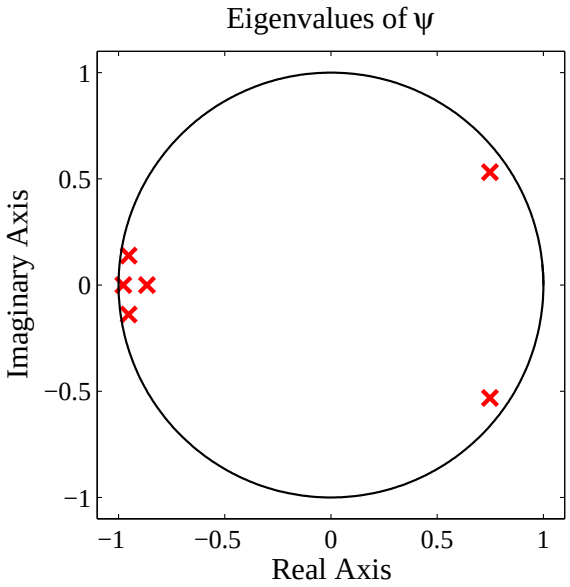


Figure 8.3: Eigenvalues of ψ for operation in continuous conduction mode.

Table 8.1: Eigenvalues of ψ and $\overline{\psi}$.

	Continuous conduction mode ($f_{sw} = 1988$Hz)		**Discontinuous conduction mode** ($f_{sw} = 1789$Hz)	
$\lambda_{1,2}$ ($\lvert\lambda_{1,2}\rvert$)	0.748 ± i0.531	(0.918)	0.746 ± i0.530	(0.916)
$\lambda_{3,4}$ ($\lvert\lambda_{3,4}\rvert$)	-0.953 ± i0.138	(0.963)	-0.952 ± i0.138	(0.962)
λ_5 ($\lvert\lambda_5\rvert$)	-0.867	(0.867)	-0.867	(0.867)
λ_6 ($\lvert\lambda_6\rvert$)	-0.978	(0.978)	-0.978	(0.978)

Based on Equation (8.11), the eigenvalues of ψ is calculated and it is given in Table 8.1 under the column continuous conduction mode. It can be seen that all eigenvalues are within the complex unit circle, as shown in Figure 8.3, which confirms stability of the converter. The eigenvalues are very close to the unit circle and it is due to the small resistance in the system. By increasing R_L, the eigenvalues have been observed to move toward the center.

8.1.3 Discontinuous Conduction Mode of Operation

The converter enters in discontinuous conduction mode of operation when the inductor current reaches zero prior the end of the switching instant. The inductor waveforms of the converter in discontinuous conduction mode are shown in Figure 8.4. Each state configuration of duration $\overline{t_{sw}}/2$ is now subdivided

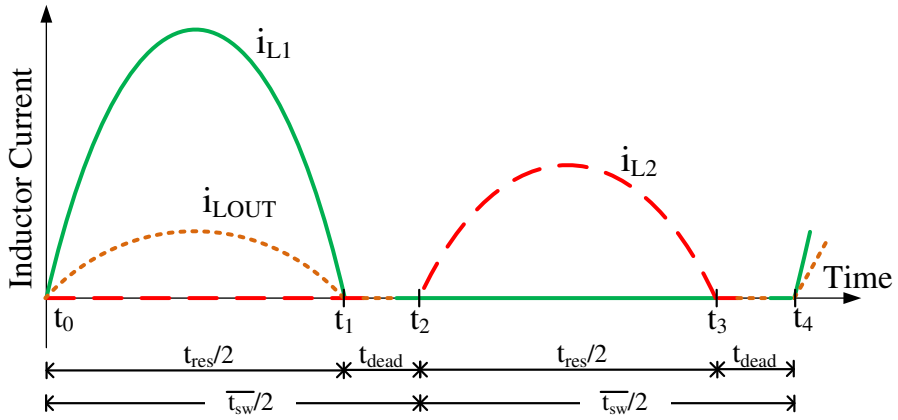


Figure 8.4: Inductor current waveforms of converter operating in discontinuous conduction mode of operation.

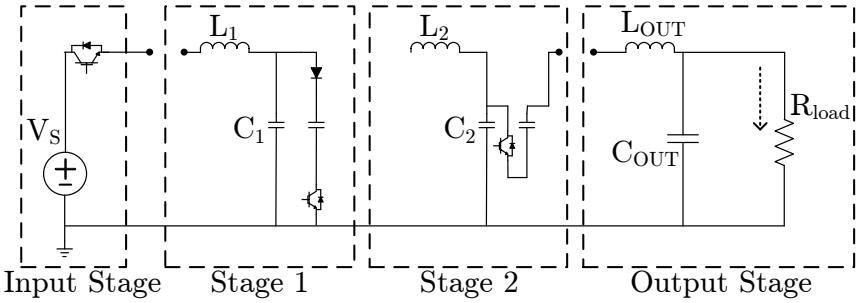
into two other configurations: conducting ($t_{res}/2$) and non-conducting (t_{dead}) segments. In order to analyse the stability in this mode of operation, the same parameters of the converter are used but the switching frequency is simply reduced to $\overline{f_{sw}}$ ($=1/\overline{t_{sw}}$). By doing so, the converter operates in discontinuous conduction mode.

The state configuration S is from t_0 to t_2 with duration $\overline{t_{sw}}/2$, where $\overline{t_{sw}}/2$ is the new longer period. From t_0 to t_1, the converter has the same configuration as previously described in continuous conduction mode. The instant t_1 is $t_{res}/2$ from the resonance period. From t_1 to t_2, the diodes D_1 and D_{OUT} are reverse biased and the converter configuration is only the load connected to the output capacitor as shown in Figure 8.5(a).

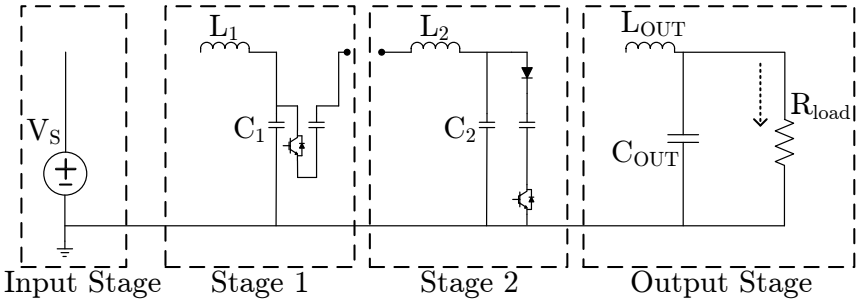
Similarly for state configuration $\overline{S}$, from t_2 to t_4, the converter has the resonance until t_3. From t_3 to t_4, diode D_2 stops conducting and the converter configuration is also only the load connected to the output capacitor as shown in Figure 8.5(b).

The state configurations in the discontinuous periods are the same for both S and $\overline{S}$. Therefore, the same matrix is developed and used to analyse the stability in this mode of operation. More precisely:

$$A_{DCM} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{OUT}R_{load}} \end{bmatrix} \tag{8.16}$$



(a) Discontinuous conduction configuration with logic state S



(b) Discontinuous conduction configuration with logic state $\overline{S}$.

Figure 8.5: State configurations for discontinuous conduction segment of the converter in during logic states S and $\overline{S}$.

$$B_{DCM} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{8.17}$$

The discontinuous segment is the same in both cases. Therefore, they have the same U_{DCM} where:

$$U_{DCM} = e^{A_{DCM}(t_{dead})} \tag{8.18}$$

The new matrix $\overline{\psi}$ becomes:

$$\overline{\psi} = U_{DCM}U_2U_{DCM}U_1 \tag{8.19}$$

where U_1 and U_2 were defined for the continuous conduction mode.

Using the same model for the continuous conduction mode example, the switching frequency is decreased to 1789Hz to analyse the stability of the converter operating in discontinuous conduction mode. The relative discontinuous period for the converter becomes 10%. The new eigenvalues of $\overline{\psi}$ are listed in Table 8.1. The magnitudes of $\lambda_{1,2}$ and $\lambda_{3,4}$ are slightly decreasing and they all remain inside the unit circle. The eigenvalues λ_5 and λ_6 are not affected by the discontinuous mode. This analysis confirms the stability of the system in both continuous and discontinuous conduction modes.

8.2 Parameter Ratings

This section evaluates the power rating of the components in the Marx converter topology. The analysis covers a configuration of N stages with M capacitors per stage. The volt-amp rating is evaluated by the peak current flowing in the component and the maximum withstand voltage across the component. The general expression is:

$$\mathrm{VA}_{RATING} = [I^{peak}] \times [V^{max}] \tag{8.20}$$

The voltage withstand considered is the voltage across the device. The voltage with respect to ground is related to insulation coordination and it is not in the scope of this thesis. Some assumptions and approximations are made in the analysis which are:

- Each stage has the same number of capacitor M.
- The converter is assumed to operate in steady-state.
- Inductor losses and dead-time requirements are neglected.
- When two components are connected in series, voltage sharing is not considered. It is assumed that each component should withstand the complete voltage.
- The voltage ripple ΔV_{Cn} is the peak to peak voltage ripple and the same relative voltage ripple is assumed. Recalling Equation (5.23), the relation for the same relative capacitor voltage ripple is:

$$\Delta V_{Cn} = M^{n-1} \Delta V_{C1} \tag{8.21}$$

The base current for the peak current evaluation is the peak current of inductor in stage 1. It is labelled as "I^P" in this analysis and it is calculated using Equation (8.22) derived from Equations (6.3) and (6.49) with the assumptions given preivously.

$$I^P = M^{2N} \pi \frac{V_S}{R_{load}} \tag{8.22}$$

The power electronic components evaluated are IGBTs and diodes. For the passive components, capacitors and inductors are considered. Figure 8.6 shows a detailed model of stage n with M capacitors. Each capacitor is located on

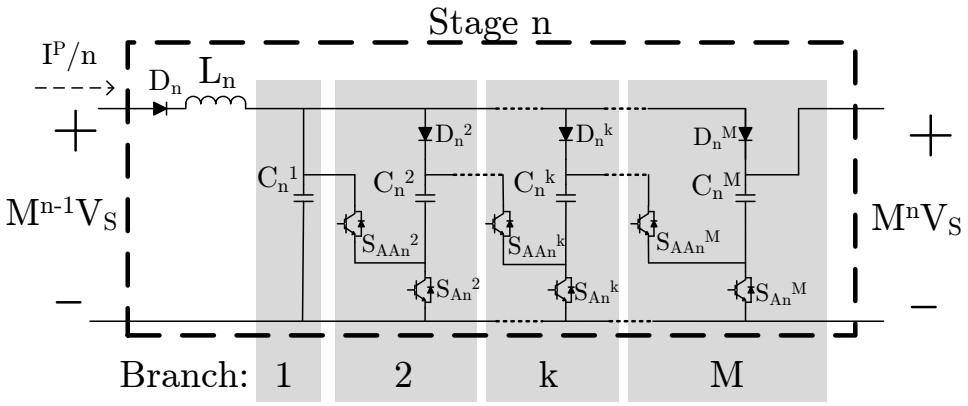


Figure 8.6: Detailed stage with components labelling.

a branch labelled k and it has its associated power electronic devices. It is important to note that branch k=1 (capacitor C_n^1) has no power electronic component, the latter begins at branch k=2.

For each component, a short description of the analysis is given along with tables that formulate the current and voltage requirements. Then, a total estimate is calculated for each component.

8.2.1 IGBT

The input switch, S_1, is carrying the complete inductor current of stage 1. Since it is connected to a fix voltage source, it has to withstand only half the voltage ripple of C_1. Using Figure 8.6, for IGBT S_{An}^k (k=2,3,...M), the incoming inductor current is divided among the parallel-connected capacitor. However, the voltage withstand increases at each branch k within stage indexed by n. For IGBT S_{AAn}^k (k=2,3,...M), the current is the same as for S_{An}^k but the voltage is independent of the branch k. Equations for the parameter ratings of IGBTs are given in Table 8.2.

Table 8.2: IGBT ratings.

IGBT	Current	Voltage
Input Stage		
S_1	I^P	$\Delta V_{C1}/2$
Stage n for k=[2,M]		
S_{An}^k	I^P/M^n	$(k-1)\left(M^{n-1}V_S + \Delta V_{Cn}/2\right)$
S_{AAn}^k	I^P/M^n	$M^{n-1}V_S + \Delta V_{Cn}/2$

The general expressions for volt-amp rating are:

$$\mathrm{VA}_{S1} = \left[I^P\right]\left[\Delta V_{C1}/2\right] \tag{8.23}$$

$$\mathrm{VA}_{SA}(n,k) = \left[\frac{I^P}{M^n}\right]\left[(k-1)\left(M^{n-1}V_S + \Delta V_{Cn}/2\right)\right] \tag{8.24}$$

for $n = [1:N]$ and $k = [2:M]$,

$$\mathrm{VA}_{SAA}(n,k) = \left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right] \tag{8.25}$$

for $n = [1:N]$ and $k = [2:M]$. The volt-amp rating of IGBT VA_{SA} per stage is:

$$\begin{aligned}\mathrm{VA}_{SA}(n) &= \Sigma_{k=2}^{M}\mathrm{VA}_{SA}(n,k)\\ &= \Sigma_{k=2}^{M}(k-1)\left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right]\end{aligned} \tag{8.26}$$

The arithmetic series $\Sigma_{k=2}^{M}(k-1)$ can be expressed as [80]:

$$\Sigma_{k=2}^{M}(k-1) = \frac{1}{2}M(M-1) \tag{8.27}$$

which gives:

$$\mathrm{VA}_{SA}(n) = \frac{1}{2}M(M-1)\left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right] \tag{8.28}$$

Similarly, for $\mathrm{VA}_{SAA}(n)$:

$$\begin{aligned}\mathrm{VA}_{SAA}(n) &= \Sigma_{k=2}^{M}\mathrm{VA}_{SAA}(n,k)\\ &= (M-1)\left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right]\end{aligned} \tag{8.29}$$

The sum of $\mathrm{VA}_{SA}(n)$ and $\mathrm{VA}_{SAA}(n)$ gives an expression of the volt-amp rating of IGBT at stage n:

$$\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{IGBT}}(n) = (\frac{1}{2}M+1)(M-1)\left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right] \tag{8.30}$$

for $n = [1, N]$. By using the assumption of the same relative capacitor voltage ripple, Equation (8.21) is substituted in Equation (8.30) to get Equation (8.31)

which is the volt-amp rating per stage independent of the stage number.

$$\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{IGBT}}(n) = (\frac{1}{2}M+1)(M-1)\frac{1}{M}\left[I^P\right]\left[V_S+\Delta V_{C1}/2\right] \tag{8.31}$$

Therefore, the total volt-amp rating of IGBTs for N stages including the input stage is:

$$\begin{aligned}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{IGBT}} &= \mathrm{VA}_{S1} + \Sigma_{n=1}^{N}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{IGBT}}(n) \\ &= \left[I^P\right]\left[\underbrace{\frac{N}{M}(\frac{M}{2}+1)(M-1)\left(V_S+\Delta V_{C1}/2\right)}_{S_A+S_{AA}} + \underbrace{\Delta V_{C1}/2}_{S_1}\right]\end{aligned} \tag{8.32}$$

8.2.2 Diode

For each stage, there are two sets of diode that need to be analyzed. The first set is the series diode which is connected in series with the inductor. This component has to carry the inductor current and to withstand the voltage difference between two stages. The largest voltage difference occurs at the end of the charging phase: the capacitor of stage n is reaching its peak voltage ripple while the capacitor of previous stage $n-1$ is at its lowest. For the diode at the output stage, the same estimate is used despite the different waveform of the output voltage as discussed in Chapter 6. As a result, the voltage withstand obtained for the output diode in this section is slightly higher than results obtained from simulations.

The second set of diodes is the branch diodes connected to capacitors from branches 2 to M. The current rating is the same as for IGBT S_{An}^k. As the diode is located in farther branch (close to M), the larger the voltage withstand is required. Equations for the parameter ratings of diodes are given in Table 8.3.

Table 8.3: Diode ratings.

Diode	Current	Voltage
Series diode: Stage 1 / Stage n / Output stage		
D_1	I^P	$\Delta V_{C1}/2$
D_n	I^P/M^{n-1}	$M^{n-2}(M-1)V_S + \Delta V_{Cn}/2 + \Delta V_{Cn-1}/2$
D_{OUT}	I^P/M^N	$M^{N-1}(M-1)V_S + \Delta V_{CN}/2 + \Delta V_{COUT}/2$
Branch diode: Stage n for k=[2,M]		
D_n^k	I^P/M^n	$(k-1)\left(M^{n-1}V_S + \Delta V_{Cn}/2\right)$

The general expressions for volt-amp rating of series diode are:

$$\mathrm{VA}_{D1}^{series} = \left[I^P\right]\left[\Delta V_{C1}/2\right] \tag{8.33}$$

$$\mathrm{VA}_{D}^{series}(n) = \left[\frac{I^P}{M^{n-1}}\right]\left[M^{n-2}(M-1)V_S + \Delta V_{Cn}/2 + \Delta V_{Cn-1}/2\right] \tag{8.34}$$

for $n = [2:N]$,

$$\mathrm{VA}_{DOUT}^{series} = \left[\frac{I^P}{M^{N}}\right]\left[M^{N-1}(M-1)V_S + \Delta V_{CN}/2 + \Delta V_{COUT}/2\right] \tag{8.35}$$

By using the assumption of the same relative capacitor voltage ripple, Equation (8.21) is substituted in Equations (8.34) and (8.35) to derive Equation (8.36), valid for $n = [2:N]$, and Equation (8.37).

$$\mathrm{VA}_{\mathrm{RATING}}^{series}(n) = \left[I^P\right]\left[\left(1-\frac{1}{M}\right)V_S + \left(1+\frac{1}{M}\right)\Delta V_{C1}/2\right] \tag{8.36}$$

$$\mathrm{VA}_{DOUT}^{series} = \left[I^P\right]\left[\left(1-\frac{1}{M}\right)V_S + \left(1+\frac{1}{M}\right)\Delta V_{C1}/2\right] \tag{8.37}$$

The volt-amp rating for the branch diode is:

$$\mathrm{VA}_{D}^{branch}(n,k) = \left[\frac{I^P}{M^{n}}\right]\left[(k-1)\left(M^{n-1}V_S + \Delta V_{Cn}/2\right)\right] \tag{8.38}$$

for $n = [1:N]$ and $k = [2:M]$. The volt-amp rating for the branch diode per stage is:

$$\begin{aligned}\mathrm{VA}_{\mathrm{RATING}}^{branch}(n) &= \Sigma_{k=2}^{M}\mathrm{VA}_{D}^{branch}(n,k)\\ &= \Sigma_{k=2}^{M}(k-1)\left[\frac{I^P}{M^{n}}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right]\end{aligned} \tag{8.39}$$

Using Equation (8.27), it gives:

$$\mathrm{VA}_{\mathrm{RATING}}^{branch}(n) = \frac{1}{2}M(M-1)\left[\frac{I^P}{M^{n}}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right] \tag{8.40}$$

By using the assumption of the same relative capacitor voltage ripple, Equation (8.21) is substituted and Equation (8.41) is obtained.

$$\mathrm{VA}_{\mathrm{RATING}}^{branch}(n) = \frac{1}{2}(M-1)\left[I^P\right]\left[V_S + \Delta V_{C1}/2\right] \tag{8.41}$$

The total volt-amp rating of diodes for N stages including the input and output stages is:

$$\begin{aligned}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{diode}} &= \mathrm{VA}_{D1}^{series} + \Sigma_{n=2}^{N}\mathrm{VA}_{\mathrm{RATING}}^{series}(n) + \mathrm{VA}_{DOUT}^{series} + \Sigma_{n=1}^{N}\mathrm{VA}_{\mathrm{RATING}}^{branch}(n) \\ &= \left[I^P\right]\Bigg[\underbrace{\frac{N}{2}(M-1)\left(V_S+\Delta V_{C1}/2\right)}_{\text{branch}} + \underbrace{\Delta V_{C1}/2}_{\text{series } D_1} \\ &+ \underbrace{N\left[(1-1/M)V_S + (1+1/M)\Delta V_{C1}/2\right]}_{\text{series } D_{2:N}+D_{OUT}}\Bigg] \end{aligned} \tag{8.42}$$

8.2.3 Capacitor

With the exception of the output stage, the current requirement for the capacitor is the same as for the branch diode. For the output capacitor, the current is evaluated as the peak inductor current from L_{OUT} minus the average load current. The voltage rating is based on the capacitor voltage ripple. Equations for the parameter ratings of capacitor are given in Table 8.4.

Table 8.4: Capacitor ratings.

Capacitor	Current	Voltage
Stage n for k=[1,M] / Output stage		
C_n^k	I^P/M^n	$M^{n-1}V_S + \Delta V_{Cn}/2$
C_{OUT}	$I^P/M^N - M^N V_S/R_{load}$	$M^N V_S + \Delta V_{COUT}/2$

The general expressions for volt-amp rating of capacitor are:

$$\mathrm{VA}_C(n,k) = \left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right] \tag{8.43}$$

for $n = [1:N]$ and $k = [1:M]$,

$$\mathrm{VA}_{COUT} = \left[\frac{I^P}{M^N} - \frac{M^N V_S}{R_{load}}\right]\left[M^N V_S + \Delta V_{COUT}/2\right] \tag{8.44}$$

The total volt-amp rating for capacitor per stage is:

$$\begin{aligned}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{capacitor}}(n) &= \Sigma_{k=1}^{M}\mathrm{VA}_C(n,k) \\ &= M\left[\frac{I^P}{M^n}\right]\left[M^{n-1}V_S + \Delta V_{Cn}/2\right]\end{aligned} \tag{8.45}$$

By using the assumption of the same relative capacitor voltage ripple, Equation (8.21) is substituted in Equations (8.44) and (8.45) to derive Equation (8.46), valid for $n = [1 : N]$, and Equation (8.47).

$$\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{capacitor}}(n) = \left[I^P\right]\left[V_S + \Delta V_{C1}/2\right] \tag{8.46}$$

$$\mathrm{VA}_{COUT} = \left[I^P - \frac{M^{2N}V_S}{R_{load}}\right]\left[V_S + \Delta V_{C1}/2\right] \tag{8.47}$$

The total volt-amp rating of capacitor for N stages with M capacitor per stage and including output stage is:

$$\begin{aligned}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{capacitor}} &= \Sigma_{n=1}^{N}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{capacitor}}(n) + \mathrm{VA}_{COUT} \\ &= \underbrace{\left[I^P\right]\left[N\left(V_S + \Delta V_{C1}/2\right)\right]}_{C_{1:N}} + \underbrace{\left[I^P - \frac{M^{2N}V_S}{R_{load}}\right]\left[V_S + \Delta V_{C1}/2\right]}_{C_{OUT}}\end{aligned} \tag{8.48}$$

8.2.4 Inductor

The current requirement for the inductor is the peak current from the charge transfer. As mentioned before, the inductor has to withstand the full voltage regardless the diode connected in series. Therefore, it has the same voltage rating as the series diode. Equations for the parameter ratings of inductor are given in Table 8.5.

Table 8.5: Inductor ratings.

Inductor	Current	Voltage
Stage 1 / Stage n / Output stage		
L_1	I^P	$\Delta V_{C1}/2$
L_n	I^P/M^{n-1}	$M^{n-2}(M-1)V_S + \Delta V_{Cn}/2 + \Delta V_{Cn-1}/2$
L_{OUT}	I^P/M^N	$M^{N-1}(M-1)V_S + \Delta V_{CN}/2 + \Delta V_{COUT}/2$

The general expressions for volt-amp rating of inductor are:

$$\mathrm{VA}_{L1} = \left[I^P\right]\left[\Delta V_{C1}/2\right] \tag{8.49}$$

$$\mathrm{VA}_{L}(n) = \left[\frac{I^P}{M^{n-1}}\right]\left[M^{n-2}(M-1)V_S + \Delta V_{Cn}/2 + \Delta V_{Cn-1}/2\right] \tag{8.50}$$

for $n = [2 : N]$,

$$\mathrm{VA}_{LOUT} = \left[\frac{I^P}{M^N}\right]\left[M^{N-1}(M-1)V_S + \Delta V_{CN}/2 + \Delta V_{COUT}/2\right] \tag{8.51}$$

By using the assumption of the same relative capacitor voltage ripple, Equation (8.21) is substituted in Equations (8.50) and (8.51) to derive Equation (8.52), valid for $n = [2 : N]$, and Equation (8.53).

$$\mathrm{VA}_L(n) = \left[I^P\right]\left[\left(1 - \frac{1}{M}\right)V_S + \left(1 + \frac{1}{M}\right)\Delta V_{C1}/2\right] \tag{8.52}$$

$$\mathrm{VA}_{LOUT} = \left[I^P\right]\left[\left(1 - \frac{1}{M}\right)V_S + \left(1 + \frac{1}{M}\right)\Delta V_{C1}/2\right] \tag{8.53}$$

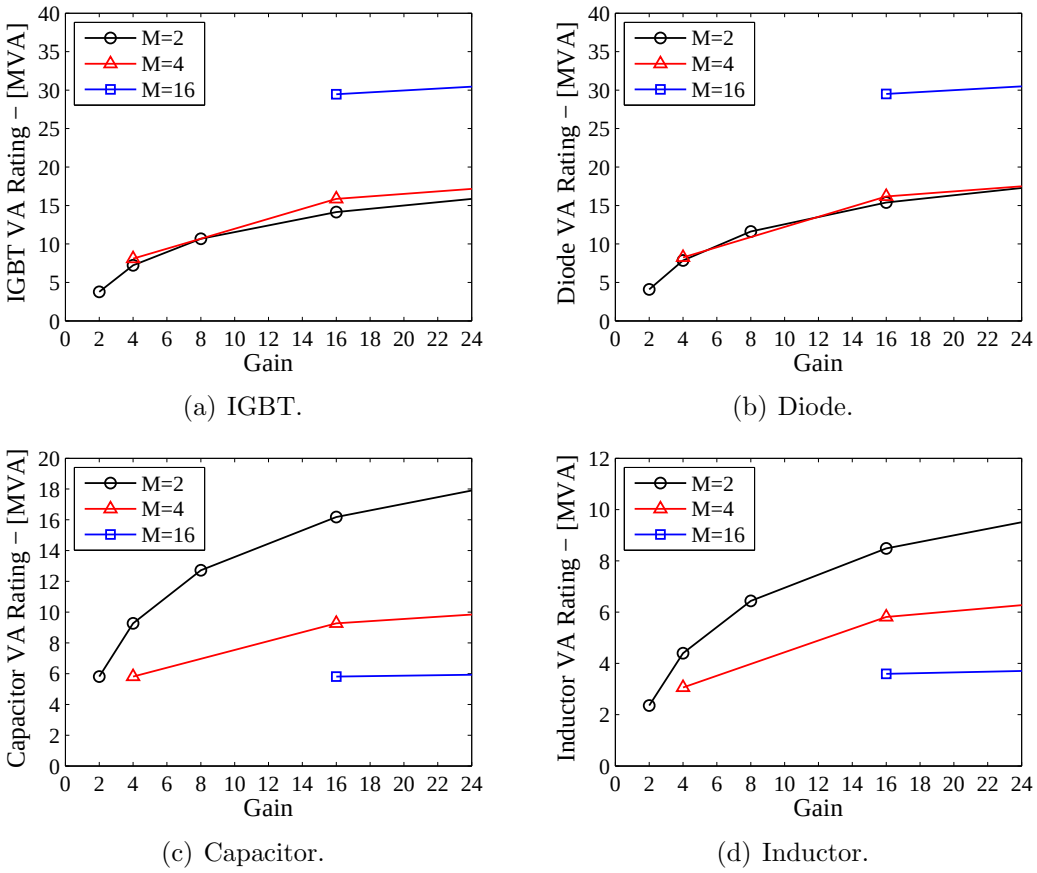
The total volt-amp rating for the inductor is:

$$\begin{aligned}\mathrm{VA}_{\mathrm{RATING}}^{\mathrm{inductor}} &= \mathrm{VA}_{L1} + \Sigma_{n=2}^{N}\mathrm{VA}_L(n) + \mathrm{VA}_{LOUT} \\ &= \left[I^P\right]\left[\underbrace{\Delta V_{C1}/2}_{L_1} + \underbrace{N\left[(1 - \frac{1}{M})V_S + (1 + \frac{1}{M})\Delta V_{C1}/2\right]}_{L_{2:N}+L_{OUT}}\right]\end{aligned}$$

8.2.5 Configuration Comparison

Figure 8.7 shows the volt-amp rating of the components for three different values of capacitor per stage (M). The graphs are with respect to the converter gain which depends directly on the number of stages (N). From the power electronics point of view, the configuration with two capacitors per stage requires lower volt-amp rating as shown in Figures 8.7(a) and 8.7(b) for IGBT and diode, respectively. As for passive component, the advantage is on the configuration with larger amount of capacitors. It is shown in Figures 8.7(c) and 8.7(d).

A comparison between three configurations of the same gain is done to evaluate the best option regarding the component rating requirements. The configurations are: four stages with two capacitors per stage (N=4, M=2), two stages with four capacitors per stage (N=2, M=4) and one stages with 16 capacitors per stage (N=1, M=16). They all produce a dc amplification of 16. The volt-amp rating for each configuration is shown in Table 8.6. The difference is significant for the power electronics of the one stage with 16 capacitors



(a) IGBT. (b) Diode.

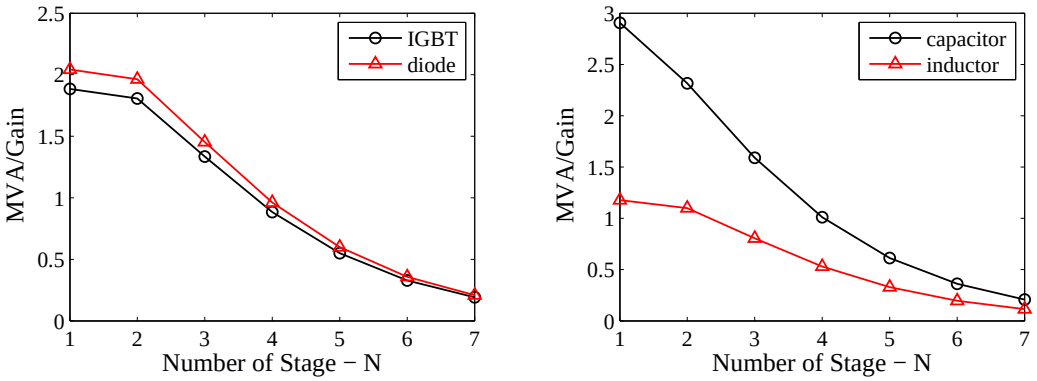
(c) Capacitor. (d) Inductor.

Figure 8.7: Component volt-amp ratings for M=2, 4 and 16.

Table 8.6: Volt-amp rating comparison for converter gain of 16.

	Configuration		
Number of stage - N	4	2	1
Number of capacitor - M	2	4	16
Converter dc gain	16	16	16
	[MVA]	[MVA]	[MVA]
IGBT	14.1	15.9	29.5
Diode	15.4	16.2	29.5
Capacitor	21.8	14.9	11.4
Inductor	8.5	5.8	3.6

compared to the other two cases. The MVA requirement is almost double. Alternatively, the volt-amp rating for the passive component is half for the one stage with 16 capacitors compared to four stages with two capacitors per stage. By comparing the three configurations, the converter with two stages with four capacitors per stage is having a slight advantage.



(a) Power electronics. (b) Passive components.

Figure 8.8: Ratio MVA/Gain for configuration with M=2.

Depending on the relative cost of each component, a weighted factor could be included in each component calculation so that the best configuration can be selected for a given converter. Example of factors are the cost of raw material (i.e. copper), the availability of the components and installation cost associated with each of them. It is expected that the power electronics will be the most heavily weighted.

Figure 8.8 evaluates the volt-amp rating as a ratio of the MVA power ratings over the converter gain. The analysis is done for a configuration with two capacitors per stage (M=2). The advantage of the cascade configuration is shown by having a "MVA cost per gain" decreasing as the number of stages increases. The ratios are very similar between the power electronics components. It is different between the passive components with few stages. However, with seven stages, the ratios for the passive components are almost the same.

8.2.6 Soft Switching

Each sub-period ends with the inter-stage currents reversing their directions and being blocked by the inter-stage diodes. Attention is drawn to the fact after the diodes have blocked, the currents within each stage are all zero. Thus, the IGBTs, which have been ON, are turned OFF without switching loss. The next event undergoes lossless switching also: when the IGBTs, which have been OFF, are turned ON to begin the next sub-period. Therefore, the IGBTs are operating with zero-current switching.

8.3 Chapter Summary

In this chapter, a stability analysis has been performed for the converter operating in both continuous conduction mode and discontinuous conduction mode. Results have shown that the converter is stable in both modes. In addition, the power rating of the converter has been estimated. The estimation evaluates individually the volt-amp ratings of IGBTs, diodes, capacitors and inductors. The derived equations are valid for a generalized configuration of a converter with N stages and M capacitors per stage. From this analysis, a comparison between 3 configurations that produce the same dc voltage gain has been performed.

Chapter 9

Marx DC-DC Converter: Wind Farm Application

In Chapters 5 to 8, the Marx converter has been presented, analyzed and tested. Its application to an offshore wind farm is introduced in this chapter. As discussed in the introduction of the thesis (Chapter 1), the need of heavy ac transformer can be avoided by using a dc collector network instead of an ac bus in the offshore wind farm. As a result, it reduces the cost of structural support related to the ac transformer in the offshore platform. The Marx converter is used to step-up the low dc voltage from the wind turbine converters to the high dc voltage of the MTDC. The overall wind farm is described and the role of each part is explained.

A 5MW wind turbine and its ac-dc-dc converter topology are described. Then, the Marx converter is adapted for wind farm application. The operation of the receiving-end VSC is briefly explained. Finally, a 200MW offshore wind farm connected to an onshore VSC station via the Marx converter is simulated to demonstrate the operation of such system.

9.1 System Description

The configuration of the wind farm with the Marx converter is shown in Figure 9.1. Wind farms are unidirectional power generators and, therefore, they do not require bidirectional VSC-HVDC station to service them. Furthermore, as much wind power as can be captured by maximum peak power tracking (MPPT) is outputted by each wind turbine. The unregulated power from each wind turbine is summed at the input of the Marx offshore station which

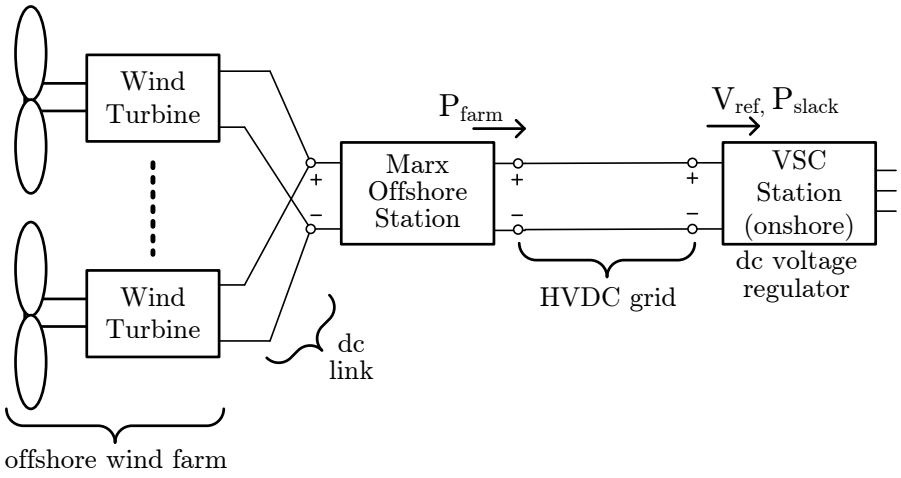


Figure 9.1: Offshore wind farm with Marx converter station to connect on HVDC grid.

amplifies the low dc voltage to high output dc voltage of the HVDC grid. In this chapter, the system has a single onshore VSC but in the next chapter the offshore wind farm is integrated to the 7-terminal HVDC grid. The onshore VSC is the dc voltage regulator of the HVDC grid and the power slack which absorbs as much power as produced by the wind farm. Thus, the Marx offshore station is required only to transmit all the power outputted by the wind turbines to the HVDC grid.

The offshore wind turbines are connected through a dc link to the Marx offshore station. The output of the Marx offshore station is accepted by onshore VSC. This study considers a 200MW wind farm composed of forty (40) 5MW wind turbines. The dc link voltage for the wind power collection is regulated at 10kV by a step-up stage included in the Marx offshore station. The regulation feedback of the step-up stage ensures that all the power outputted by the wind turbines is transferred to the HVDC grid. The Marx offshore station bridges 10kV to the 250kV of the HVDC grid with a dc amplification of 25. On the HVDC grid side, the VSC regulates the dc voltage level at 250kV.

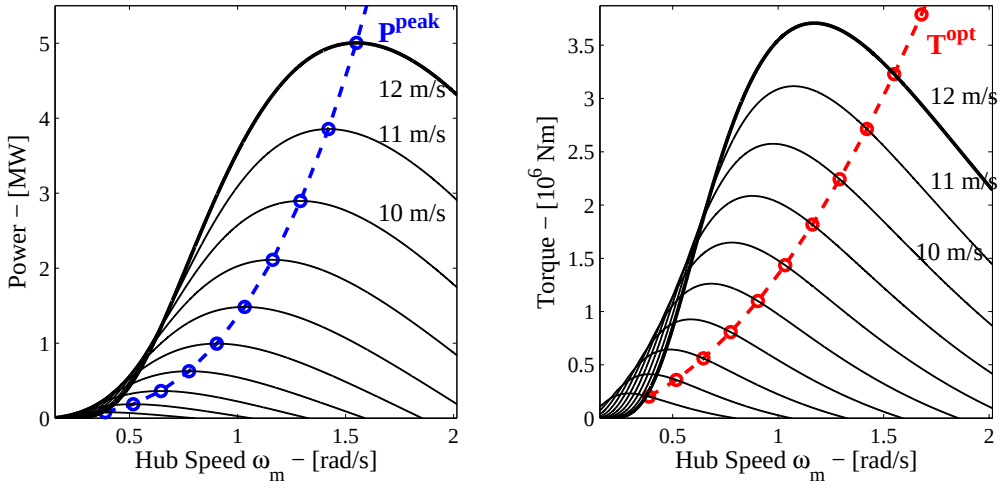
9.2 Wind Turbine

9.2.1 Wind Turbine Characteristics

The wind turbine characteristics are taken from [81, 82]. Each wind turbine drives a 5MW permanent magnet synchronous generator (PMSG) and the

Table 9.1: Wind turbine and generator parameters

Wind Turbine	
Rated power [MW]	5
Rated wind speed [m/s]	12
Cut-in wind speed [m/s]	3
Rated shaft speed [rad/s]	1.55
Rated frequency [Hz]	35.77
Rated torque [Nm]	3.226×10^6
Rotor and turbine inertia J (2.55sec)	1.06×10^7
Generator	
Induced voltage E_{PM} $[kV_{LN}^{RMS}]$	2.89
Synchronous inductance L_S [mH]	6.77



(a) Power with peak power identified.

(b) Torque with optimal torque curve.

Figure 9.2: Wind turbine characteristic curves for fix pitch angle ($\beta = 0$).

main parameters are listed in Table 9.1. The wind turbine power and torque characteristics for various wind speeds are shown in Figure 9.2. The optimal torque curve T^{opt} for MPPT is also shown in Figure 9.2(b).

The wind turbine converter, shown in Figure 9.3, is composed of a diode rectifier to rectify the variable frequency ac generated power from the PMSG to dc. The diode rectifier is robust and not expensive. The control of the PMSG is performed by the attached step-up (boost) converter [83]. The step-up converter regulates the current I_{DR} at the output of the diode rectifier which has a direct relationship with the ac current on the PMSG. By doing so, the torque of the machine can be regulated to operate at MPPT.

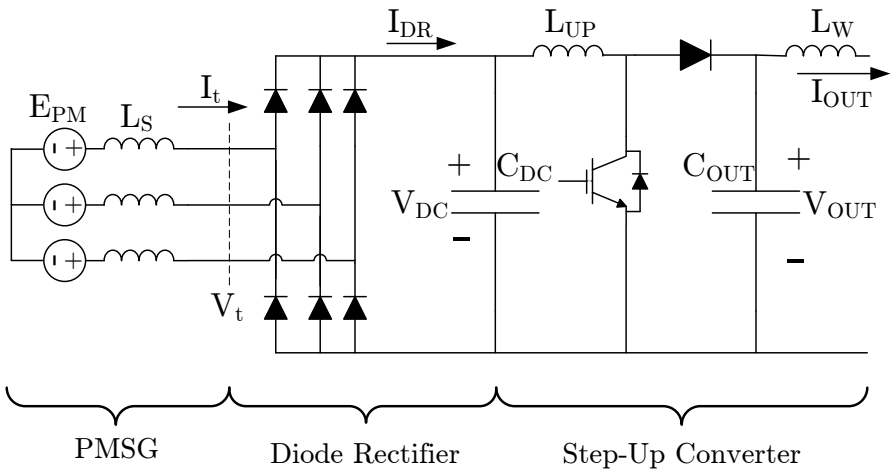


Figure 9.3: Wind turbine converter.

The mechanical dynamics of the wind turbine are modeled using first order Equation (9.1). The objective is to regulate the generator electrical torque T_e such that it follows the optimal torque curve T^{opt} given in Figure 9.2(b) for a given hub speed ω_m.

$$J\frac{d\omega_m}{dt} = T_m - T_e \tag{9.1}$$

A set of equations needs to be derived in order to operate the wind turbine as expected with the step-up converter. The induced voltage by the PMSG is directly proportional to the mechanical speed ω_m and the stator field constant k_{PM} as given in Equation (9.2).

$$E_{PM} = k_{PM}\omega_m \tag{9.2}$$

Similarly, the electrical frequency ω_e of the PMSG varies with respect to the mechanical speed ω_m and the relationship is:

$$\omega_e = \frac{P}{2}\omega_m \tag{9.3}$$

where P is the pole number. The electrical torque of the PMSG is calculated using:

$$T_e = \frac{P_e}{\omega_m} \tag{9.4}$$

where P_e is the electrical power defined as:

$$P_e = 3E_{PM}I_t\cos\psi \tag{9.5}$$

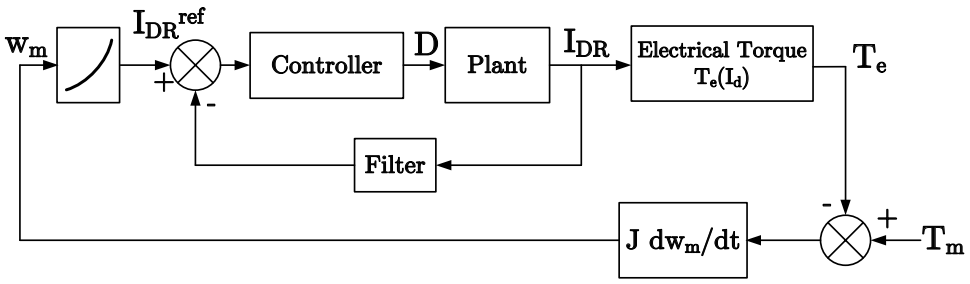


Figure 9.4: Wind turbine control diagram.

where E_{PM} is the line-to-neutral rms induced voltage, I_t is the rms ac line current and $\cos\psi$ is the power factor. Unity power factor is imposed at the diode rectifier point of connection. The power factor at the PMSG can be calculated using:

$$\cos\psi = 1 - \frac{\omega_e L_S I_{DR}}{\sqrt{6} E_{PM}} \tag{9.6}$$

where L_S is the ac inductance and I_{DR} is the dc current at the output of the diode rectifier. The rms ac line current I_t can be expressed in terms of I_{DR} using diode rectifier Equation (9.7).

$$I_t = \frac{\sqrt{6}}{\pi} I_{DR} \tag{9.7}$$

By combining Equations (9.2) to (9.7), it is possible to express the electrical torque in terms of the controlled current I_{DR} and it is given in Equation (9.8).

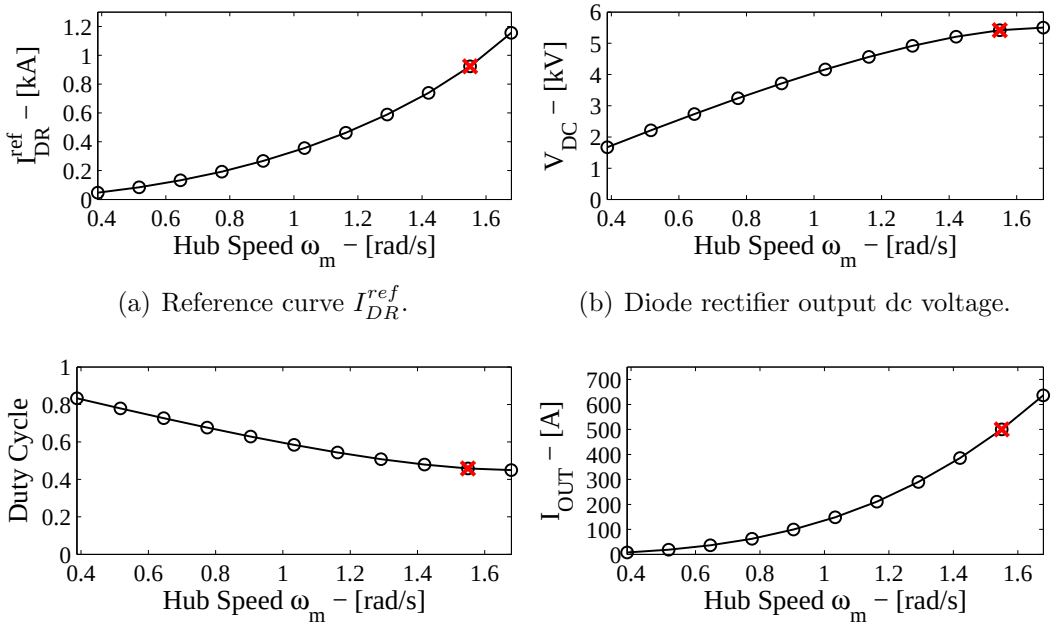
$$T_e = \frac{3\sqrt{6}}{\pi} k_{PM} I_{DR} - \frac{3}{\pi}\frac{P}{2} L_S I_{DR}^2 \tag{9.8}$$

In order to operate at MPPT, the electrical torque T_e shall follow the optimal curve shown in Figure 9.2(b). Therefore, for $T_e = T_e^{opt}$, I_{DR}^{opt} is calculated using:

$$I_{DR}^{opt} = \frac{\frac{3\sqrt{6}}{\pi} - \sqrt{\frac{54}{\pi^2} k_{PM}^2 - \frac{12}{\pi}\frac{P}{2} L_S T_e^{opt}}}{\frac{6}{\pi}\frac{P}{2} L_S} \tag{9.9}$$

which gives the reference curve I_{DR}^{ref}. The reference curve is shown in Figure 9.5(a) and it is used as a look-up table in the wind turbine controller shown in Figure 9.4.

By neglecting losses and the voltage drop associated with commutation current, the voltage at the output of the diode rectifier, V_{DC}, can be approximated



(a) Reference curve I_{DR}^{ref}.

(b) Diode rectifier output dc voltage.

(c) Step-up converter duty cycle.

(d) Output current to dc link.

Figure 9.5: Wind turbine converter characteristics when operating at MPPT.

using:

$$V_{DC} = \frac{P^{peak}}{I_{DR}^{opt}} \tag{9.10}$$

where P^{peak} is the peak power identified in Figure 9.2(a). The results of Equation (9.10) is shown in Figure 9.5(b).

The gain of the step-up converter operating in continuous conduction mode is [40]:

$$M = \frac{V_{OUT}}{V_{DC}} = \frac{1}{1-D} \tag{9.11}$$

where D is the duty cycle of the step-up converter. By neglecting the voltage drop associated with the dc link transmission line, the capacitor voltage V_{OUT} is assumed to be at the dc link voltage of 10kV. The duty cycle can be calculated using Equation (9.11) and V_{DC} from Figure 9.5(b). The step-up converter duty cycle is shown in Figure 9.5(c). By neglecting losses, the injected current from each wind turbine into the dc link is estimated by simply dividing P^{peak} by the dc link voltage. The results are given in Figure 9.5(d).

The step-up inductor L_{UP} is selected to ensure that the step-up converter remains in continuous conduction mode. The converter does so when [40]:

$$K > K_{crit} \tag{9.12}$$

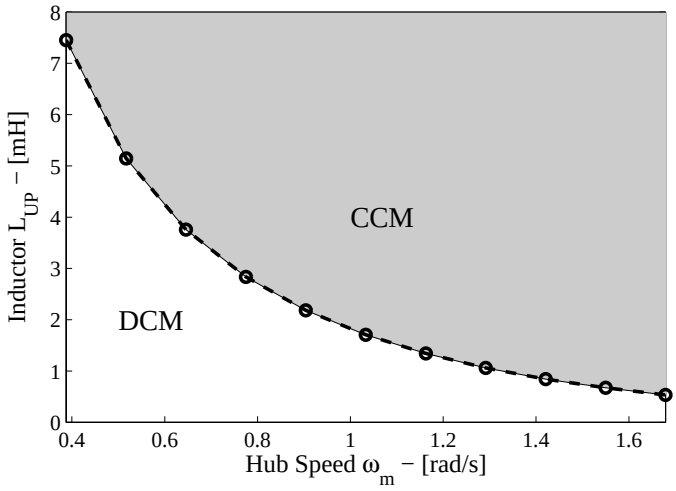


Figure 9.6: Wind turbine converter boundary for continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

where

$$K = \frac{2L_{UP}}{R_{OUT}T_S} \tag{9.13}$$

and

$$K_{crit} = D(1-D)^2 \tag{9.14}$$

The inductor value has to be large enough such that Equation (9.12) is satisfied at low power (cut-in wind speed) as well as high power (rated wind speed). In Equation (9.13), the resistance R_{OUT} is calculated using:

$$R_{OUT} = \frac{P^{peak}}{V_{link}^2} \tag{9.15}$$

By combining Equations (9.12) to (9.15), the requirement for the inductor L_{UP} becomes:

$$L_{UP} > \frac{1}{2}R_{OUT}T_S D(1-D)^2 \tag{9.16}$$

The boundary is drawn in Figure 9.6 for the switching frequency of 2kHz ($T_s = 500\mu s$). From the figure, an inductor value of 8uH will ensure operation in continuous conduction mode in all range of operation of the wind turbine. The parameters for the wind turbine converter is given in Table 9.2. The components of the wind turbine converter are selected to ensure adequate performance of the unit with low voltage ripple on the capacitor.

Table 9.2: Wind turbine converter parameters

Diode Rectifier	
C_{dc} [mF]	1
Step-Up Converter	
L_{UP} / R_{LUP} [mH / Ω]	8 / 0.02
C_{OUT} [mF]	1
L_W / R_W [mH / Ω]	30 / 0.08
Switching frequency F_S [Hz]	2000
Controller gain [K_P / a]	0.02 / 100

9.2.2 50MW Wind Turbine Upgrade

Due to simulation limitations, the 40 wind turbines of 5MW of the wind farm have been modeled with four scaled-up units rated for 50MW. In compacting 40 wind turbines to four scaled-up units, the same wind turbine dynamics is preserved. The parameters of the scaled-up wind turbine is listed in Table 9.3.

Table 9.3: 50MW wind turbine

Wind Turbine	
Rated power [MW]	50
Rated wind speed [m/s]	12
Rated shaft speed [rad/s]	1.55
Rated frequency [Hz]	35.77
Rated torque [Nm]	3.226×10^7
Rotor and turbine inertia J (2.55sec)	1.06×10^8
Generator	
Induced voltage E_{PM} [kV_{LN}^{RMS}]	2.89
Synchronous inductance L_S [mH]	0.677
Diode Rectifier	
C_{dc} [mF]	10
Step-Up Converter	
L_{UP} / R_{LUP} [mH / Ω]	0.8 / 0.002
C_{OUT} [mF]	10
L_W / R_W [mH / Ω]	3 / 0.008
Switching frequency F_S [Hz]	2000
Controller gain [K_P / a]	0.002 / 100

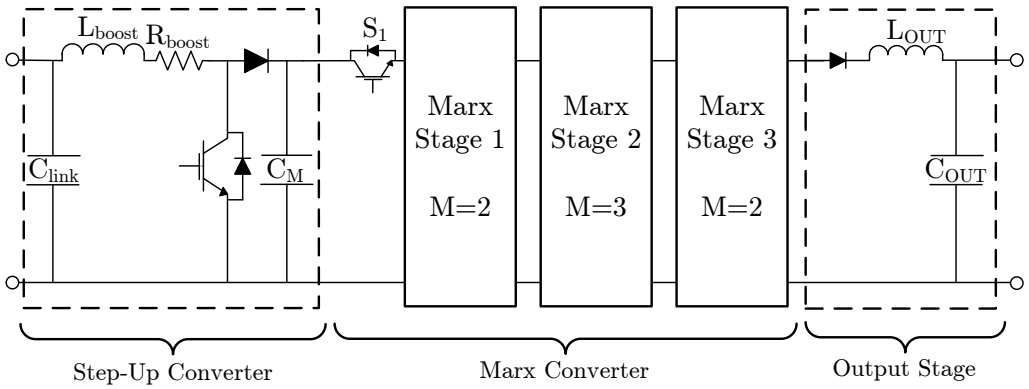


Figure 9.7: Marx offshore station.

9.3 Marx Offshore Station

The Marx dc-dc converter by itself does not have the regulator property; it only amplifies its input voltage by the designed gain. As a result, it is necessary to add an additional stage at the input that will provide the control variable to maintain the wind farm dc link at 10kV. A step-up (boost) converter is inserted at the input stage. The step-up converter combined with the fixed structure of the Marx converter provides a variable range of amplification. The Marx offshore station is the combination of the step-up converter and the Marx converter as shown in Figure 9.7.

The Marx converter is composed of three stages in which two of them is composed of two capacitors (gain of M=2) and one stage is composed of three capacitors (gain of M=3). For the Marx converter, the dc gain is $2 \times 3 \times 2 = 12$. In order to bridge the 250kV dc grid and the 10kV dc link, the step-up converter is expected to amplify by a factor around 2.

The inductor and capacitor values are selected to ensure proper resonance for the Marx converter operation as described in Chapter 6. Among the design requirements, a dead-time of 5μs is considered and the capacitor voltage ripples are $\pm 10\%$ for stages 1 to 3. For the output capacitor, the same capacitor value as for the VSC terminal station is used. For the step-up converter, the inductor is selected to have low current ripple. The complete list of parameters is given in Table 9.4.

The role assigned to the step-up converter is to maintain the dc link voltage at 10kV. The current flowing out of the Marx offshore station depends on the difference between its output voltage and the onshore VSC (dc voltage

Table 9.4: Marx offshore station parameters

Input reactor [mH / Ω]	1.2 / 0.02
Step-Up Converter	
C_{link} [mF]	40
L_{boost} / R_{boost} [mH / Ω]	2 / 0.02
C_M [mF]	10
Switching frequency F_S [kHz]	2
Controller gain [K_P / a]	0.005 / 150
Marx Converter	
Number of stages	3
Number of steps M_1, M_2, M_3,	2, 3, 2
Switching frequency - f_{sw} [kHz]	2
Dead-time - t_{dead} [μs]	5
L_1 / R_{L1} [uH / Ω]	5 / 0.01
C_1 [uF]	625
L_2 / R_{L2} [uH / Ω]	38.5 / 0.01
C_2 [uF]	105
L_3 / R_{L3} [uH / Ω]	342.5 / 0.01
C_3 [uF]	18
L_{OUT} / R_{LOUT} [uH / Ω]	684.5 / 0.01
C_{OUT} [mF]	0.4
Output reactor L_{reac} [mH / Ω]	2 / 0.02

regulator). If the step-up converter increases its amplification, the output voltage of the Marx offshore station increases which results in higher power outputted.

When more power is produced by the wind turbines, the increased output currents from the wind turbines charge the dc link capacitor to a voltage higher than 10kV. From the schematic of Figure 9.8, the step-up converter control adjusts the duty cycle D to increase the output voltage of the step-up converter which is the input voltage of the Marx converter and thereby increase the dc power outputted into the HVDC link. When the power outputted by the Marx offshore station is equal to the power outputted by the wind farm, the 10kV is regulated.

9.4 VSC Terminal Station

The VSC terminal station at the receiving end has the same parameter as terminal station T2 used in the simulations of Chapter 4. From the dq-axis

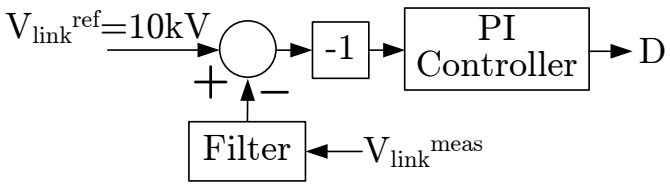


Figure 9.8: Control diagram of the step-up converter included in the Marx offshore station.

controller, the d-axis control is applied in negative feedback to regulate the dc voltage at V_{ref} which is set to 250kV. The parameters can be found in Table C.3 of Appendix C.

9.5 Simulation Results

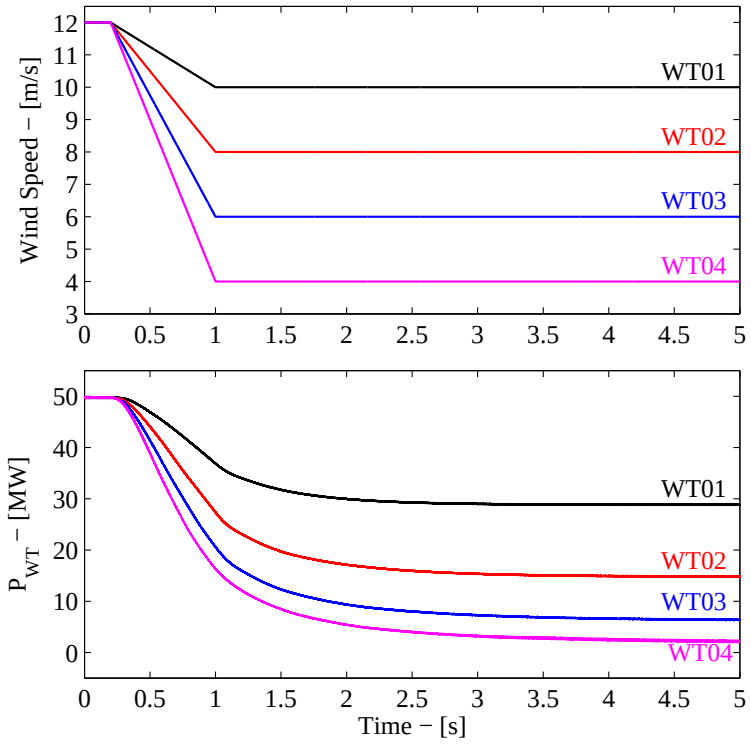
The system of Figure 9.1 has been simulated in the PSCAD-EMTDC software package, an industry-grade software for high voltage power electronic research. It is composed of a 200MW offshore wind farm modeled with 4 scaled-up wind turbines (50MW each), the Marx offshore station and the onshore VSC station. The transmission line parameters are given in Table 9.5.

In the beginning of the simulation, the wind turbines are operating at rated wind speed of 12m/s. Figure 9.9(a) shows their respective wind speeds and output power P_{WT}. Figure 9.9(b) shows the total wind power from the Marx offshore station received by the onshore VSC station. The lower graph shows the voltage at the terminal of the VSC station with the regulator reference set at 250kV.

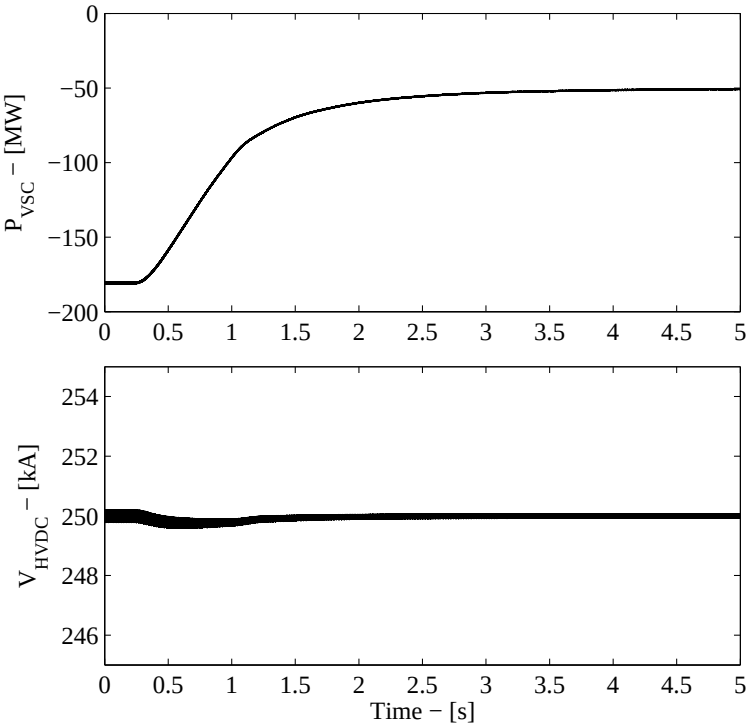
Then, the wind speed decreases to different values for each wind turbine. The power produced by the wind turbines decreases also and the total power injected in the dc grid changes from 200MW to 52MW. The average voltage in steady-state at the Marx offshore station is listed in Table 9.6. The dc link

Table 9.5: Transmission line parameters

	Distance [km]	Resistance [Ω]	Inductance [mH]
Wind Turbine (50MW) to Marx offshore station	1	0.0012	0.0106
Marx offshore station to onshore VSC station	413	5	44



(a) Wind turbine operation. For each wind turbine, the wind speed is shown and the power injection from each unit.



(b) HVDC transmission with power extracted at receiving end and dc voltage.

Figure 9.9: Simulation results for operation of the system from high wind to low wind condition.

Table 9.6: Simulation results at low wind condition

V_{link}	V_M	V_{C1}	V_{C2}	V_{C3}	V_{COUT}	V_{VSC}
10.00	21.04	20.96	41.85	125.55	251.02	250.00

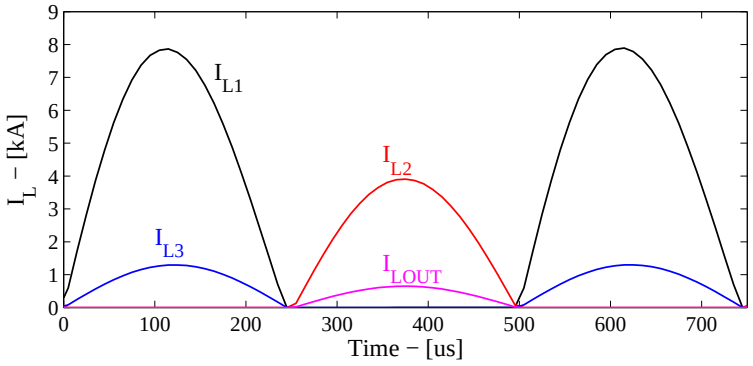


Figure 9.10: Simulation results of the Marx converter inductor waveforms at low wind condition.

voltage is maintained at 10kV. The step-up converter amplifies from 10kV to 21kV which becomes the input voltage for the Marx converter. The voltage increases from 21kV to 42kV between stage 1 to stage 2, from 42kV to 125kV between stage 2 to stage 3 and from 125kV to 251kV from stage 3 to output stage. Therefore, the Marx offshore station bridges the 10kV dc link of the wind farm to the 250kV HVDC grid system.

Figure 9.10 shows the waveforms of the currents in the inter-stage inductors at steady-state. At each successive stage, the currents I_{L1}, I_{L2}, I_{L3}, I_{LOUT} decrease by a factor of 1/M as the voltages increase by M.

9.6 Chapter Summary

This chapter shows the operation of an offshore wind farm connected to an onshore VSC station. The wind farm is connected to the HVDC grid via the Marx offshore station: a dc-dc converter system which collects the power produced from the wind turbines and amplifies the voltage to HVDC transmission level. The VSC station is set to regulate the dc voltage on the HVDC grid. Simulation results show that such system is capable of managing varying wind power as well as maintaining a stable HVDC grid. In the next chapter, the offshore wind farm and the Marx offshore station are introduced to a larger HVDC grid.

Part III

Complete Multiterminal HVDC System

Chapter 10

Complete Multiterminal HVDC System

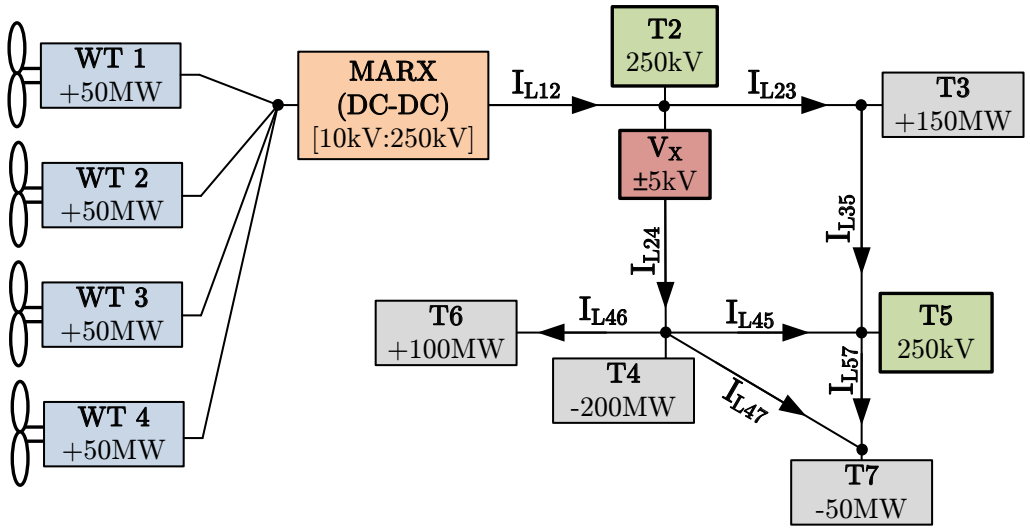


Figure 10.1: Complete multiterminal HVDC system with dc power flow controller and Marx offshore station.

The concept of a large multiterminal with power flow controllability and the integration of an offshore wind farm using dc collector network is presented in this chapter. The complete 7-terminal HVDC system of the thesis is simulated in PSCAD-EMTDC software package, an industry-grade software for high voltage power electronic research. It comprises six VSC terminal stations (two dc voltage regulators and four constant power dispatchers), the thyristor-based dc power flow controller and the Marx offshore station with an offshore wind farm of four units. The overall system is shown in Figure 10.1.

Table 10.1: Simulation results of the power at terminal stations.

	low wind t=0s [MW]	transition t=(1→3)s	**high wind** t=6.5s [MW]
Wind Turbine 1	29	$V_{\text{wind}} = 10 \rightarrow 12\text{m/s}$	49
Wind Turbine 2	21	$V_{\text{wind}} = 9 \rightarrow 12\text{m/s}$	49
Wind Turbine 3	10	$V_{\text{wind}} = 7 \rightarrow 12\text{m/s}$	49
Wind Turbine 4	4	$V_{\text{wind}} = 5 \rightarrow 12\text{m/s}$	49
Marx Offshore Station	61	$\longrightarrow$	181
VSC Terminal Station T2	-50	$\longrightarrow$	-50
VSC Terminal Station T3	150	$\longrightarrow$	150
VSC Terminal Station T4	-200	$\longrightarrow$	-200
VSC Terminal Station T5	-9	$\longrightarrow$	-125
VSC Terminal Station T6	100	$\longrightarrow$	100
VSC Terminal Station T7	-50	$\longrightarrow$	-50

The simulation model is based on the 7-terminal HVDC system presented in Chapter 4. Terminal station T1 is replaced by the offshore wind farm of Chapter 9. The objective of the chapter is to validate the operation of the complete system via simulations.

10.1 Simulation Results

The simulation scenario consists of a ramp from low wind condition to high wind condition. Initially, the wind turbines are operating at low wind speeds. Then, the units experience a wind increase up to rated wind speed. Terminal stations T2 and T5, which are dc voltage regulators, are expected to maintain their dc voltage at 250kV. As discussed in Section 4.1 of Chapter 4, the dc power flow controller installed on line L24 is adjusted to maintain the power extraction of terminal station T2 at 50MW. The excess wind power has to be absorbed by the other slack bus: terminal station T5. Terminal stations T3, T4, T6 and T7 maintain their constant power injection/extraction operation. The power at each terminal station from the simulation results is listed in Table 10.1. At the beginning, the Marx offshore station injects only 61MW and terminal station T5 extracts 9MW. However, at high wind, the wind farm injects 181MW and terminal station T5 extracts 125MW while it maintains the dc link voltage at 250kV.

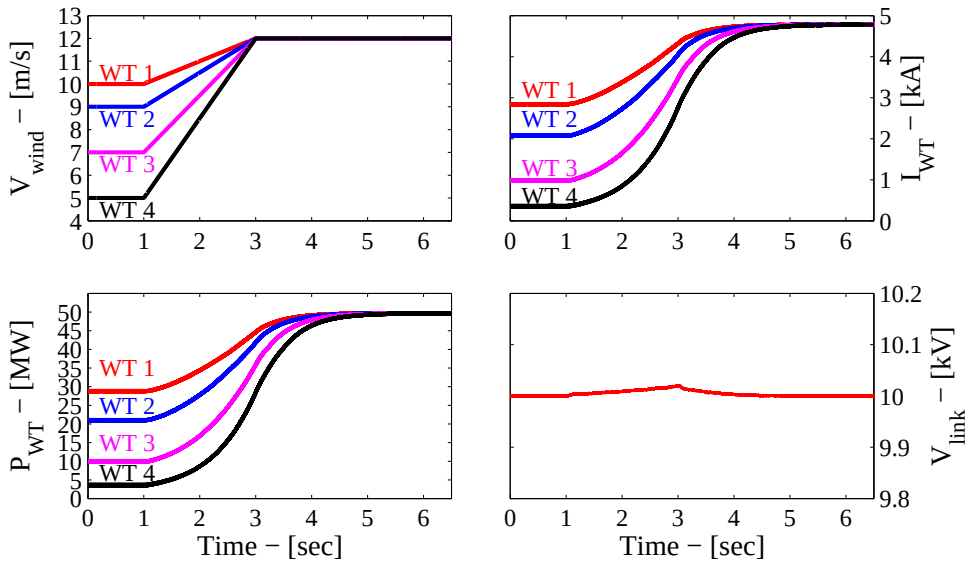


Figure 10.2: Simulation results of the offshore wind farm.

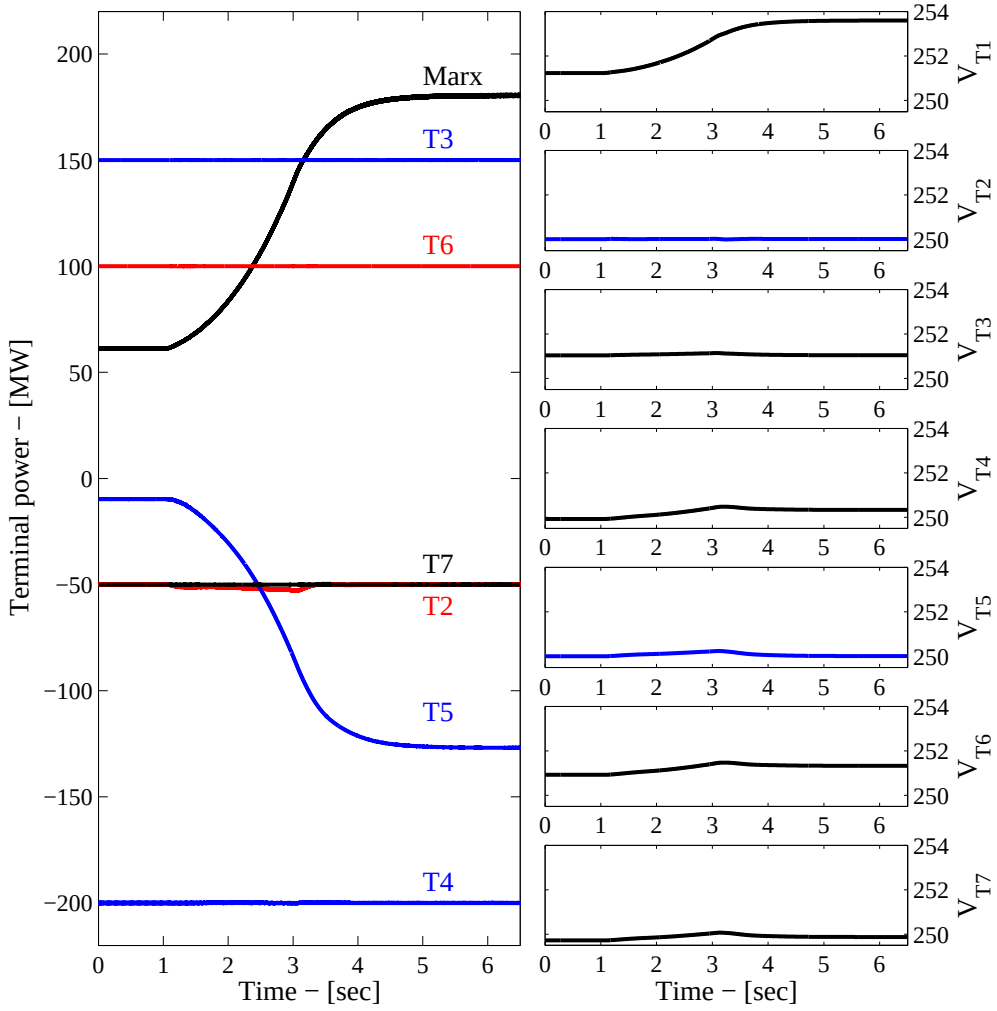


Figure 10.3: Simulation results for power and voltage at terminal stations.

The simulation results for the wind turbines are shown in Figure 10.2. Initially, wind turbines operate at different wind speed. The current I_{WT} injected by each wind turbine into the 10kV dc link depends on their power production. Then, the wind speeds increase so that all wind turbines operate at rated wind speed after the transition. As shown in Figure 10.2, the increase is smooth and the wind turbines remain stable. The Marx offshore station is capable of maintaining the dc link voltage at 10kV. A slight increase in the dc link voltage is observed during the transition but it resumes rapidly.

Figure 10.3 gives a good overview of the operation of the MTDC by showing the power at each terminal station and their respective terminal voltages. Positive power represents injection into the MTDC and negative power is associated with power extraction from the MTDC. The powers remain constant for all terminal stations except for the Marx offshore station and terminal station T5. The power injected by the Marx offshore station increases as the wind farm produces more power; the Marx offshore station links the wind farm and the HVDC grid. Without the dc power flow controller, the increasing wind power would have been distributed among the two slack buses terminal stations T2 and T5. However, with the dc power flow controller, the power extracted by terminal station T2 is maintained at 50MW and terminal station T5 is extracting the rest of the injected wind power. The dc power flow controller succeeds in diverting the power from terminal station T2 to terminal station T5. The terminal voltages are shown to remain stable and terminal stations T2 and T5 regulate the HVDC grid voltage at 250kV.

The transmission line currents are shown in Figure 10.4 and the power flow pattern can be interpreted. Most of the excess power produced by the wind farm is transmitted through path L24-L45 instead of L23-L35. The current in transmission line L45 changes direction as the wind power increases. Line L24 has more ripple and it comes from the harmonics created by the dc power flow controller as studied in Chapter 3. The transmission line currents for low wind and high wind conditions are shown in Table 10.2. The table also includes the power transmitted through each line and the changes are indicated with $\uparrow$ or $\downarrow$. Within the eight transmission line currents, four are increasing, three do not vary and one is decreasing.

The response of the dc power flow controller is shown in Figure 10.5. The reference for the outer loop controller is the power of terminal station T2 at -50MW. During the transition, there is a decrease by 3MW but it resumes

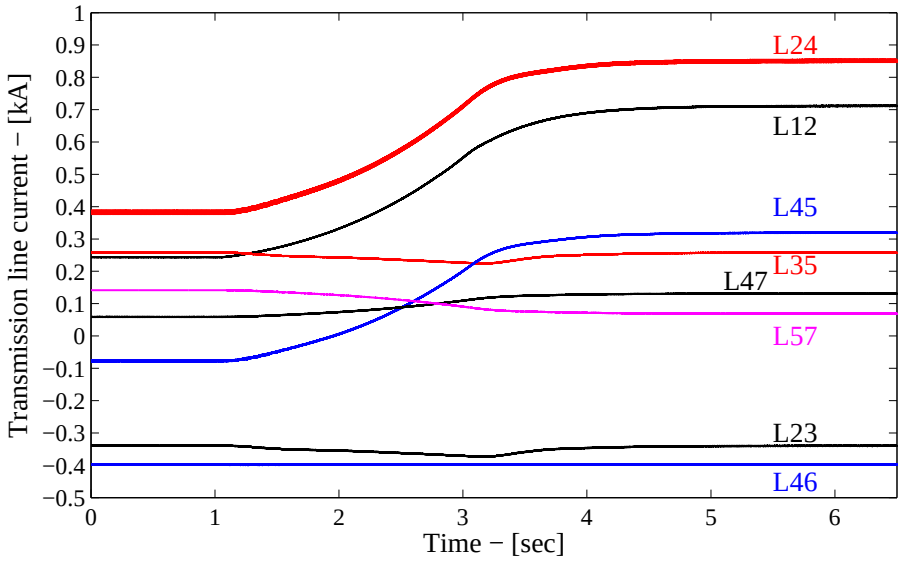


Figure 10.4: Simulation results of the transmission line currents.

Table 10.2: Simulation results for transmission line currents and powers.

	L12	L23	L24	L35	L45	L46	L47	L57
low wind								
Current [kA]	0.24	-0.34	0.38	0.26	-0.08	-0.40	0.06	0.14
Power [MW]	61	85	95	65	20	100	15	35
high wind								
Current [kA]	0.70↑	-0.34	0.84↑	0.26	0.31↑	-0.40	0.13↑	0.07↓
Power [MW]	178↑	85	211↑	65	78↑	100	32↑	18↓

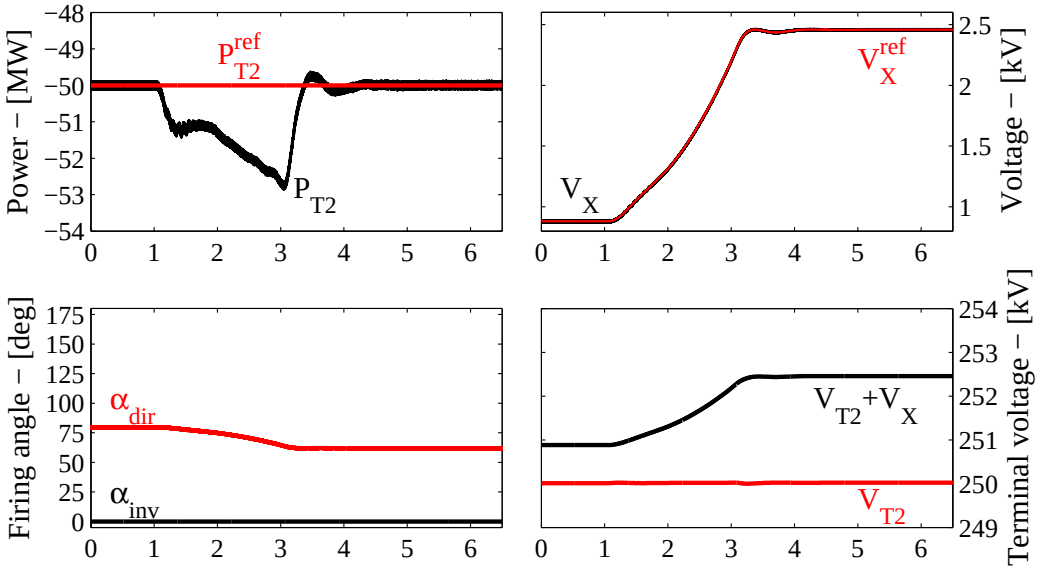


Figure 10.5: Simulation results of dc power flow controller response.

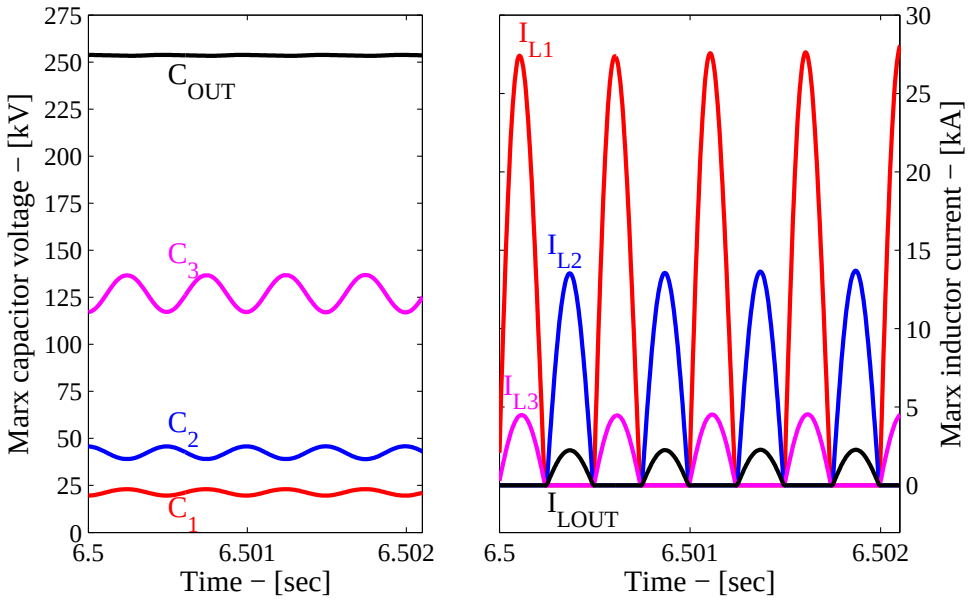


Figure 10.6: Simulation results of the Marx converter operating at high wind.

quickly after the transition. From the inner loop controller, the injected voltage V_X follows precisely its reference signal V_X^{ref}. The firing angle is also shown in Figure 10.5. The voltage at terminal station T2, V_{T2}, and the voltage with the injected voltage V_X are shown. Voltage V_{T2} is stable at 250kV and the combined voltage, $V_{T2} + V_X$, follows the transition.

Capacitor voltages and inductor currents for the Marx converter inside the Marx offshore station are shown in Figure 10.6. The waveforms are shown for the system in steady-state at high wind conditions. The voltage amplification is shown: dc gain of two from V_{C1} to V_{C2}, dc gain of three from V_{C2} to V_{C3} and dc gain of two from V_{C3} to V_{COUT}. From Figure 10.6, the inductor currents show good resonance period. The sequence of odd-numbered stages and even-numbered stages operating in different sub-period is clearly displayed.

The average voltage and the capacitor voltage ripple are listed in Table 10.3. The ripples are within the designed value of $\pm 10\%$. The voltage ripple on output capacitor is very small to ensure smooth power transmission. The table also shows the inductor peak current decreasing between each stage.

10.2 Chapter Summary

This chapter has presented the operation of a multiterminal HVDC system which integrates the dc power flow controller developed in Chapter 3 and

Table 10.3: Simulation results of the Marx converter.

Capacitor Voltage			
Average		**Ripple**	
V_{C1} [kV]	21.5	ΔV_{C1} [kV | %]	3.5 | ±8.1%
V_{C2} [kV]	42.5	ΔV_{C2} [kV | %]	6.8 | ±8.0%
V_{C3} [kV]	127.3	ΔV_{C3} [kV | %]	20.0 | ±7.9%
V_{COUT} [kV]	253.5	ΔV_{COUT} [kV | %]	0.5 | ±0.1%
Inductor Peak Current			
I_{L1}^{peak} [kA]			28.3
I_{L2}^{peak} [kA]			13.8
I_{L3}^{peak} [kA]			4.6
I_{LOUT}^{peak} [kA]			2.3

the offshore wind farm presented in Chapter 9. The offshore wind farm is connected to the MTDC via a dc-dc converter station based on the Marx converter topology. The scenario for the wind turbines going from low wind to high wind is simulated. The simulation results show stable operation of the MTDC and the ability of the Marx offshore station to inject wind power inside the HVDC grid. In addition, the dc power flow controller has demonstrated its capability of redirect the power flow inside the MTDC system.

Chapter 11

Conclusion

11.1 Thesis Summary

This thesis has introduced the concept of the dc power flow controller inside a HVDC grid to address the power flow control issue. It consists of inserting on a dc transmission line a device in series that varies the dc voltage on that specific line. By doing so, the transmission line current can be adjusted and the power flow varied. Because the dc line resistance is small, the inserted voltage variation does not have to be large.

Before proceeding to realizing the dc power flow controller, its benefits to power flow controllability need to be determined first. This is initially evaluated for a 3-terminal HVDC grid and then for a 4-terminal HVDC grid. The evaluation shows significant increase in the region of operation for each system which justifies proceeding to the next phase of hardware realization.

The proposed dc power flow controller consists of two 6-pulse thyristor-bridges connected in a dual-converter configuration so that it has 4-quadrant control. It is connected in series on the dc line and it is presented as a small appendage of a VSC-HVDC station. The thyristor power flow controller has been simulated in a 3-terminal HVDC grid and it is shown to be fast and stable. Then, a 7-terminal HVDC grid is presented. The HVDC grid is shown to benefit from having the dc power flow controller to supplement the controllability of two HVDC stations operating as dc voltage regulators. N-1 contingency for dc transmission lines is studied and the operation of the system is simulated.

In addition to the dc power flow controller, a new dc-dc converter topology has been presented. The dc-dc converter is capable of changing the output to input dc voltage ratio. The topology is based on the Marx generator concept

of charging capacitors in parallel followed by reconnection in series of the capacitors to create higher dc voltage. The electric charge transfer is done via L-C resonance and a diode ensures that the charge transfer of each cycle is unidirectional. The converter topology can have multiple cascaded stages to reduce VA requirement in component size while obtaining high dc voltage amplification. The converter with a configuration of $N = 3$ stages with $M = 3$ dc voltage gain per stage, for an overall gain of $M^N = 3^3 = 27$, is simulated for proof of concept.

A detailed analysis of the Marx converter topology is presented. The analysis results in design guidelines intended for proper component sizing. Among the design requirements, losses and dead-time for switching events are considered.

From the design, a prototype has been constructed to verify experimentally the converter topology. The construction has been done gradually with $N = 1$ stage with dc amplification of $M = 2$ and subsequently upgraded to $N = 2$ stages with $M = 2$. The rating of the prototype converter is 5kW with input voltage of 110V and a theoretical dc voltage gain of $M^N = 4$. The experimental work has demonstrated dc voltage amplification and the stable operation of the converter. Among the tests performed, a load step change has been applied and operation at different switching frequencies has been tested.

A stability analysis of the topology has been developed based on sampled-data approach. It evaluates the eigenvalues of the converter operating in continuous and discontinuous modes. Additionally, parameter ratings are evaluated with derived equations. The evaluation covers IGBT switches, diodes, inductors and capacitors.

The Marx converter is adapted for offshore wind farm application. The adaptation recognizes that the Marx converter has only a fix dc gain. Therefore, a boost step-up converter is added in series to give a degree of dc gain controllability. The combination is given the name “Marx offshore station” in the thesis.

A software model, composed of a 200MW offshore wind farm, a Marx offshore station and an onshore VSC station, has been developed for simulation. The offshore wind farm is based on wind turbines driving permanent magnet synchronous generators. Diode rectifiers and boost dc-dc converters aggregate wind power to a 10kV dc collector network. The Marx offshore station bridges the 10kV dc link to the 250kV HVDC transmission line. This approach avoids

the high civil engineering cost of an offshore platform capable of supporting heavy ac transformers which are required for HVDC transmission. Simulation results show stable operation of the wind turbine during wind change and confirm the Marx offshore station to be capable of bridging the two dc networks.

Finally, the two parts of the research of this thesis are integrated within a complete multiterminal HVDC system. It is a 7-terminal HVDC grid which has a dc power flow controller and an offshore wind farm including the Marx offshore station. This large multiterminal HVDC system is simulated and each part developed in this work performs as expected and jointly.

11.2 Conclusions

The research has shown that a dc power flow controller increases the flexibility and the region of operation of MTDC. The design of the dc power flow controller based on two 6-pulse thyristor-bridges has been proven to be adequate to the tasks.

Simulation results and the hardware prototype have demonstrated that the Marx dc-dc converter is capable of high power, high dc voltage operation. The Marx dc-dc converter is shown to be suitable for offshore wind farm to deliver wind farm power from its low dc voltage bus to the high dc voltage of the MTDC grid.

Both the dc power flow controller and the Marx dc-dc converter enlarge the scope of MTDC.

11.3 Thesis Contributions

The items listed below are original contributions.

11.3.1 DC Power Flow Controller

- The DC Power Flow Controller, as an auxiliary controller of a VSC station, based on thyristor-based dual-converter. The DC Power Flow Controller is inserted in a dc transmission line to increase the controllability of a dc grid based on multiterminal HVDC. (Chapters 3 and 4)

- Apart from the realization of the controller, the research has evaluated that the controller does increase the feasible region of operation of the dc grid thus justifying its presence. (Chapter 2)

11.3.2 Marx DC-DC Converter

- The innovative dc-dc converter, which has been adapted from the well known Marx generator to serve as a continuous high voltage, high power dc-dc converter. Besides simulation, experimental prototypes have been constructed and tested for proof of concept. (Chapters 5-7)

- Innovation, which consists of electric charge transfers from the input end to the output end using L-C resonance with a diode to the inductor to ensure continuous, unidirectional power transfer. (Chapters 5 and 6)

- Innovation, which consists of design equations for determining the capacitor size for dc voltage gain M. (Chapter 6)

- Innovation, which consists of applying cascading stages to the Marx dc-dc converter. As the dc voltage increases in each stage, it has a corresponding current decrease whereby the VA rating is constant at each stage. (Chapters 5 and 6)

- An innovative method of asymptotic stability analysis based on solving linear equations $\dot{x} = Ax + Bu$ in each sub-period of IGBT switching and integrating the output states at the end of the kth sub-period as the initial state of the (k+1)th sub-period. Stability is assured when the eigenvalues are lying within the unit circle in the complex plane. (Section 8.1 of Chapter 8)

- A method of cost evaluation for the choice of N (the number of cascading stages) and M (the dc voltage gain of each stage) to achieve an overall dc voltage gain of M^N. The method depends on deriving equations for components based on the voltage and current ratings at each stage. (Section 8.2 of Chapter 8)

11.4 Future Research

HVDC technology is developing in many directions through technological innovation (e.g. MMC) and network expansion (e.g. HVDC grid). Before the potential of HVDC grid is exploitable, more research has to be done. For example, the CIGRÉ study committee B4 (HVDC and Power Electronics) has six active Working Bodies to address various issues such as feasibility, control and protection, design and "grid code" [84].

Regarding the work in this thesis, future research would include:

11.4.1 DC Power Flow Controller

- Consider IGBT and IGCT families of current-source converters.
- Apply the dc power flow controller to the upcoming DC Grid CIGRÉ Benchmark model developed by the Working Body B4-52. The latter is expected to be released soon.
- Study operation of the dc power flow controller under MTDC fault scenarios.
- Develop analysis to obtain optimal location of the dc power flow controller inside a MTDC.
- Study the interactions and the benefits of having the interconnection of two large electrical networks of different technologies (ac and dc). The situation can be studied from the electrical network stability and the economical points of view.

11.4.2 Marx DC-DC Converter

- Develop adaptations of the topology for bidirectional capability.
- Study response of the converter with internal and external fault cases.
- Evaluate quantitatively the efficiency of the converter with optimization tool to minimize losses.
- Study the feasibility for other application such as solar panel.

Appendix A

Associated Publications

A.1 Journal Article

- E. Veilleux and B.-T. Ooi, "Multiterminal HVDC with Thyristor Power-Flow Controller," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1205-1212, July 2012.

A.2 Conference Proceedings

- E. Veilleux and B.-T. Ooi, "Multi-Terminal HVDC Grid with Power Flow Controllability," in *CIGRÉ 2012 Session*, Paris, August 26-31, 2012.
- E. Veilleux and B.-T. Ooi, "Power Flow Analysis in Multi-Terminal HVDC Grid," in *IEEE PES Power Systems Conference & Exposition*, Phoenix, AZ, USA, March 20-23, 2011.

A.3 Submitted for Publications

- E. Veilleux and B.-T. Ooi, "A DC-DC Converter using Marx Generator Concept." Submitted to *IEEE Transactions on Power Delivery*.
- E. Veilleux, B.-T. Ooi and P. Lehn, "Marx DC-DC Converter for High Power Application," Submitted to *IET Power Electronics*.
- E. Veilleux and B.-T. Ooi, "Marx-dc-dc Converter for Connecting Off-shore Wind Farms to Multiterminal HVDC," Submitted to *2013 IEEE PES General Meeting*, Vancouver, BC, Canada, July 21-25, 2013.

Appendix B

DC Power Flow Controller: Calculation Derivations

B.1 Algorithm

A routine algorithm is used to calculate the region of operation. The pseudocode is given as follow:

SET input variables:
    line resistance and current limits
    dc voltage regulator ($V_{T3} = 250kV$).
FOR range of P_{T1}
  FOR range of P_{T2}
    FOR range of P_{T4} (if 4-terminal HVDC grid)
      FOR range of M
        Compute terminals' voltage (Newton-Raphson method)
        Compute transmission line currents (Ohm's Law)
        Compute P_{T3}
        Check if $I \leq I_{LIMIT}$ for all lines

In the case where no dc power flow controller is present, the variable M is set to 1.

B.1.1 Voltage Calculation

The voltages are computed using iterative calculations with the Newton-Raphson method [85], it is defined as :

$$V_T(i+1) = V_T(i) + J^{-1}(i)\left\{\overline{P} - P\left(V_T(i)\right)\right\} \tag{B.1}$$

where V_T is the iterative computed terminal voltage, J is the Jacobian matrix, $\overline{P}$ is the fix power level and P is the power calculation function.

B.2 Equations for 3-Terminal 3-Line MTDC

The equations for the 3-terminal 3-line system are recalled from Chapter 2. More precisely, recalling Equations (2.1), (2.2) and (2.7) for the line currents:

$$I_{L13} = \frac{V_{T1} - V_{T3}}{R_{L13}} \tag{B.2}$$

$$I_{L23} = \frac{V_{T2} - V_{T3}}{R_{L23}} \tag{B.3}$$

$$I_{L12} = \frac{MV_{T1} - V_{T2}}{R_{L12}} \tag{B.4}$$

and Equations (2.8) and (2.9) for the terminal powers:

$$P_{T1} = V_{T1}^2\left[\frac{1}{R_{L13}} + \frac{M^2}{R_{L12}}\right] + V_{T1}\left[\frac{-V_{T3}}{R_{L13}} + \frac{MV_{T2}}{R_{L12}}\right] \tag{B.5}$$

$$P_{T2} = V_{T2}^2\left[\frac{1}{R_{L23}} + \frac{1}{R_{L12}}\right] + V_{T2}\left[\frac{-V_{T3}}{R_{L23}} + \frac{MV_{T1}}{R_{L12}}\right] \tag{B.6}$$

B.2.1 Jacobian Matrix

The Jacobian matrix for the 3-terminal 3-line system is defined as:

$$J = \left[\begin{array}{c|c} \partial P_{T1}/\partial V_{T1} & \partial P_{T1}/\partial V_{T2} \\ \hline \partial P_{T2}/\partial V_{T1} & \partial P_{T2}/\partial V_{T2} \end{array}\right] \tag{B.7}$$

where the partial derivatives are derived using Equations (B.5) and (B.6). It gives:

$$\frac{\partial P_{T1}}{\partial V_{T1}} = 2V_{T1}\left[\frac{1}{R_{L13}} + \frac{M^2}{R_{L12}}\right] + \left[\frac{-V_{T3}}{R_{L13}} + \frac{MV_{T2}}{R_{L12}}\right] \tag{B.8}$$

$$\frac{\partial P_{T1}}{\partial V_{T2}} = \left[\frac{MV_{T1}}{R_{L12}}\right] \tag{B.9}$$

$$\frac{\partial P_{T2}}{\partial V_{T1}} = \left[\frac{MV_{T2}}{R_{L12}}\right] \tag{B.10}$$

$$\frac{\partial P_{T2}}{\partial V_{T2}} = 2V_{T2}\left[\frac{1}{R_{L23}} + \frac{1}{R_{L12}}\right] + \left[\frac{-V_{T3}}{R_{L23}} + \frac{MV_{T1}}{R_{L12}}\right] \tag{B.11}$$

B.2.2 Current Sensitivity

The numerical calculation of $\frac{\partial V_{T1}}{\partial M}$ and $\frac{\partial V_{T2}}{\partial M}$ is done using partial derivatives of the two power equations of terminal stations T1 and T2 given in Equations (B.5) and (B.6). It uses the fact that those terminal stations are performing constant power injection, which means that it does not vary with respect to change of M $\left(\frac{\partial P_T}{\partial M} = 0\right)$. Recalling that terminal station T3 has constant voltage $\left(\frac{\partial V_{T3}}{\partial M} = 0\right)$, it gives:

$$\begin{aligned}\frac{\partial P_{T1}}{\partial M} = 0 = &\left[\frac{2V_{T1}}{R_{L13}} + \frac{2V_{T1}M^2}{R_{L12}} - \frac{V_{T3}}{R_{L1}} - \frac{MV_{T2}}{R_{L12}}\right]\frac{\partial V_{T1}}{\partial M} \\ &+ \left[\frac{-MV_{T1}}{R_{L3}}\right]\frac{\partial V_{T2}}{\partial M} + \left[\frac{2V_{T1}^2 M}{R_{L12}} - \frac{V_{T1}V_{T2}}{R_{L12}}\right]\end{aligned} \tag{B.12}$$

and

$$\begin{aligned}\frac{\partial P_{T2}}{\partial M} = 0 = &\left[\frac{-MV_{T2}}{R_{L3}}\right]\frac{\partial V_{T1}}{\partial M} + \left[\frac{-V_{T1}V_{T2}}{R_{L12}}\right] \\ &+ \left[\frac{2V_{T2}}{R_{L23}} + \frac{2V_{T2}}{R_{L12}} - \frac{V_{T3}}{R_{L2}} - \frac{MV_{T1}}{R_{L12}}\right]\frac{\partial V_{T2}}{\partial M}\end{aligned} \tag{B.13}$$

Using Equations (B.12) and (B.13), it is easy to compute numerically the value of $\frac{\partial V_{T1}}{\partial M}$ and $\frac{\partial V_{T2}}{\partial M}$ using an operating point (M=1). By doing so, a set of two equations with two unknowns is created. The calculated values of $\frac{\partial V_{T1}}{\partial M}$ and $\frac{\partial V_{T2}}{\partial M}$ are used in Equations (2.10), (2.11) and (2.12) in the current sensitivity analysis.

B.3 Equations for 4-Terminal 5-Line MTDC

The equations for the 4-terminal 5-line system is given for the HVDC grid composed with the dc power flow controller. As for the 3-terminal HVDC grid, the dc voltage regulator is terminal station T3. More precisely, the equations

for the currents are:

$$I_{L12} = \frac{V_{T1} - V_{T2}}{R_{L12}} \tag{B.14}$$

$$I_{L23} = \frac{V_{T2} - V_{T3}}{R_{L23}} \tag{B.15}$$

$$I_{L34} = \frac{V_{T3} - V_{T4}}{R_{L34}} \tag{B.16}$$

$$I_{L41} = \frac{V_{T4} - V_{T1}}{R_{L41}} \tag{B.17}$$

$$I_{L13} = \frac{MV_{T1} - V_{T3}}{R_{L13}} \tag{B.18}$$

The power equations are:

$$P_{T1} = V_{T1}^2 \left[\frac{1}{R_{L12}} + \frac{1}{R_{L41}} + \frac{M^2}{R_{L13}}\right] + V_{T1}\left[-\frac{V_{T2}}{R_{L12}} - \frac{V_{T4}}{R_{L41}} - \frac{MV_{T3}}{R_{L13}}\right] \tag{B.19}$$

$$P_{T2} = V_{T2}^2 \left[\frac{1}{R_{L12}} + \frac{1}{R_{L23}}\right] + V_{T2}\left[-\frac{V_{T1}}{R_{L12}} - \frac{V_{T3}}{R_{L23}}\right] \tag{B.20}$$

$$P_{T3} = V_{T3}^2 \left[\frac{1}{R_{L23}} + \frac{1}{R_{L34}} + +\frac{1}{R_{L13}}\right] + V_{T3}\left[-\frac{V_{T2}}{R_{L23}} - \frac{V_{T4}}{R_{L34}} - \frac{MV_{T1}}{R_{L13}}\right] \tag{B.21}$$

$$P_{T4} = V_{T4}^2 \left[\frac{1}{R_{L34}} + \frac{1}{R_{L41}}\right] + V_{T4}\left[-\frac{V_{T3}}{R_{L34}} - \frac{V_{T1}}{R_{L41}}\right] \tag{B.22}$$

As previously mentioned, in the case where the HVDC grid would have to be studied without the dc power flow controller, the value of M has to be set to 1 in order to reproduce such circuit.

B.3.1 Jacobian Matrix

The Jacobian matrix for the 4-terminal 5-line system used in the algorithm described in Section B.1 is given as:

$$J = \left[\begin{array}{c|c|c} \partial P_{T1}/\partial V_{T1} & \partial P_{T1}/\partial V_{T2} & \partial P_{T1}/\partial V_{T4} \\ \hline \partial P_{T2}/\partial V_{T1} & \partial P_{T2}/\partial V_{T2} & \partial P_{T2}/\partial V_{T4} \\ \hline \partial P_{T4}/\partial V_{T1} & \partial P_{T4}/\partial V_{T2} & \partial P_{T4}/\partial V_{T4} \end{array}\right] \tag{B.23}$$

where the partial derivatives are derived using Equations (B.19), (B.20) and (B.22). It gives:

$$\frac{\partial}{\partial V_{T1}}\begin{bmatrix} P_{T1} \\ P_{T2} \\ P_{T4} \end{bmatrix} = \begin{bmatrix} 2V_{T1}\left(\frac{1}{R_{L12}}+\frac{1}{R_{L41}}+\frac{M^2}{R_{L13}}\right)-\frac{V_{T2}}{R_{L12}}-\frac{V_{T4}}{R_{L41}}-\frac{MV_{T3}}{R_{L13}} \\ -\frac{V_{T2}}{R_{L12}} \\ \frac{V_{T4}}{R_{L41}} \end{bmatrix} \tag{B.24}$$

$$\frac{\partial}{\partial V_{T2}}\begin{bmatrix} P_{T1} \\ P_{T2} \\ P_{T4} \end{bmatrix} = \begin{bmatrix} -\frac{V_{T1}}{R_{L12}} \\ 2V_{T2}\left(\frac{1}{R_{L12}}+\frac{1}{R_{L23}}\right)-\frac{V_{T1}}{R_{L12}}-\frac{V_{T3}}{R_{L23}} \\ 0 \end{bmatrix} \tag{B.25}$$

$$\frac{\partial}{\partial V_{T4}}\begin{bmatrix} P_{T1} \\ P_{T2} \\ P_{T4} \end{bmatrix} = \begin{bmatrix} -\frac{V_{T1}}{R_{L41}} \\ 0 \\ 2V_{T4}\left(\frac{1}{R_{L34}}+\frac{1}{R_{L41}}\right)-\frac{V_{T3}}{R_{L34}}-\frac{V_{T1}}{R_{L41}} \end{bmatrix} \tag{B.26}$$

B.3.2 Current Sensitivity

The current sensitivity analysis for 4-terminal HVDC grid uses the same approach as in Section B.2.2. Again, only the terminal station with constant power injection (P_{T1}, P_{T2}, P_{T4}) are used and terminal station T3 has constant voltage $\left(\frac{\partial V_{T3}}{\partial M}=0\right)$. The partial derivatives of Equations (B.19), (B.20) and (B.22) are performed which gives:

$$\frac{\partial}{\partial M}\begin{bmatrix} P_{T1} \\ P_{T2} \\ P_{T4} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} A_1 & A_2 & A_3 \\ B_1 & B_2 & B_3 \\ C_1 & C_2 & C_3 \end{bmatrix}\begin{bmatrix} \frac{\partial V_{T1}}{\partial M} \\ \frac{\partial V_{T2}}{\partial M} \\ \frac{\partial V_{T4}}{\partial M} \end{bmatrix} + \begin{bmatrix} A_4 \\ B_4 \\ C_4 \end{bmatrix} \tag{B.27}$$

where for $\frac{\partial P_{T1}}{\partial M}$ it is,

$$\begin{aligned} A_1 =& \frac{2V_{T1}}{R_{L12}}+\frac{2V_{T1}}{R_{L41}}+\frac{2V_{T1}M^2}{R_{L13}}-\frac{V_{T2}}{R_{L12}}-\frac{V_{T4}}{R_{L41}}-\frac{V_{T3}M}{R_{L13}} \\ A_2 =& -\frac{V_{T1}}{R_{L12}} \\ A_3 =& -\frac{V_{T1}}{R_{L41}} \\ A_4 =& \frac{2V_{T1}^2M}{R_{L13}}-\frac{V_{T1}V_{T3}}{R_{L13}} \end{aligned}$$

and for $\frac{\partial P_{T2}}{\partial M}$ it is,

$$\begin{aligned} B_1 =& -\frac{V_{T2}}{R_{L12}} \\ B_2 =& \frac{2V_{T2}}{R_{L12}} + \frac{2V_{T2}}{R_{L23}} - \frac{V_{T1}}{R_{L12}} - \frac{V_{T3}}{R_{L23}} \\ B_3 =& 0 \\ B_4 =& 0 \end{aligned}$$

and for $\frac{\partial P_{T4}}{\partial M}$ it is,

$$\begin{aligned} C_1 =& -\frac{V_{T4}}{R_{L41}} \\ C_2 =& 0 \\ C_3 =& \frac{2V_{T4}}{R_{L34}} + \frac{2V_{T4}}{R_{L41}} - \frac{V_{T3}}{R_{L34}} - \frac{V_{T4}}{R_{L41}} \\ C_4 =& 0 \end{aligned}$$

In the system under study, terminal stations T1, T2 and T4 are performing constant power injection, therefore, $\frac{\partial P_{T1,T2,T4}}{\partial M} = 0$. By using Equation (B.27), a set of 3 equations is constructed to compute $\frac{\partial V_{T1}}{\partial M}$, $\frac{\partial V_{T2}}{\partial M}$ and $\frac{\partial V_{T4}}{\partial M}$ for a given operating point. By doing so, it can be substituted in the current sensitivity equations of Equation (B.28).

$$\frac{\partial}{\partial M}\begin{bmatrix} I_{L12} \\ I_{L23} \\ I_{L34} \\ I_{L41} \\ I_{L13} \end{bmatrix} = \begin{bmatrix} \frac{1}{R_{L12}} & \frac{-1}{R_{L12}} & 0 \\ 0 & \frac{1}{R_{L23}} & 0 \\ 0 & 0 & \frac{-1}{R_{L34}} \\ \frac{-1}{R_{L41}} & 0 & \frac{1}{R_{L41}} \\ \frac{M}{R_{L13}} & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{\partial V_{T1}}{\partial M} \\ \frac{\partial V_{T2}}{\partial M} \\ \frac{\partial V_{T4}}{\partial M} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{V_{T1}}{R_{L13}} \end{bmatrix} \tag{B.28}$$

Appendix C

DC Power Flow Controller: Model parameters

Models of the converters used in this work are detailed in this Appendix. The objective is to develop common circuits and controllers used for models across the thesis where only parameter values are needed in each situation. The models for the VSC, the thyristor power flow controller and the transmission lines are introduced. Parameter values for simulations of Chapters 3 and 4 are listed in Sections C.4 and C.5, respectively. Parameters in Section C.5 are also used for the simulation of Chapter 10.

C.1 Voltage Source Converter

The VSC model is shown in Figure C.1. The ac voltage source is identified as V_{ac} and its value is given in volts line-to-line rms value. On the ac side, there are also the ac inductance L_S along with the resistance R_S. AC filters to remove the PWM harmonics are not included. The IGBT and diode models are almost ideal with negligible losses. On the dc side, there is the output capacitor C_{DC}. In some situations, a dc reactor might be implemented to smooth the output dc current. If it is the case, the reactor is installed and it is identified as L_{reac}.

The operation of VSC is well known with many good references such as [14] and [74]. The VSC controller uses the dq-transform approach and the control diagram is shown in Figure C.2.

In general, the q-axis controller regulates the ac voltage magnitude for unity power factor operation. A fix reference value is used in this thesis ($i_q^{ref} = 0$).

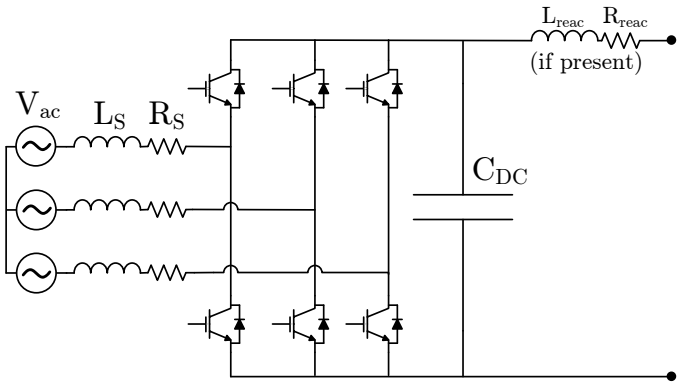


Figure C.1: VSC model.

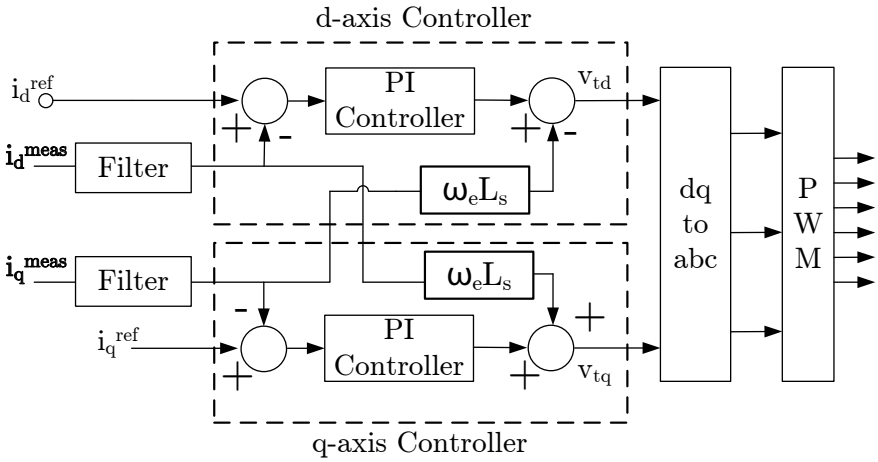


Figure C.2: VSC dq-controller.

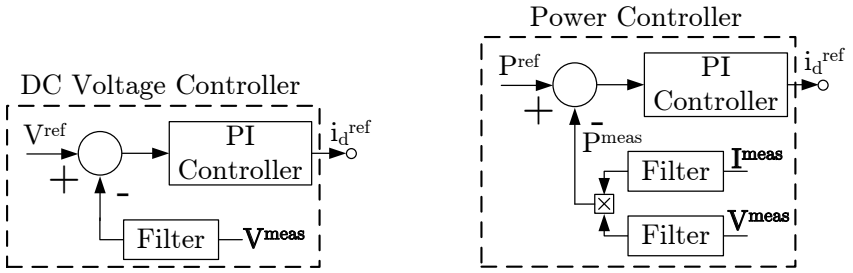
For the d-axis controller, there are two different outer loop controller options: dc voltage regulator (V^{ref}) and constant power controller (P^{ref}). They are both shown in Figure C.3.

The regulators are PI controllers where the parameters are given in the form:

$$K_P \frac{s+a}{s} \tag{C.1}$$

and the input filters for the measured signals are in the form:

$$\frac{\omega_{filter}}{s+\omega_{filter}} \tag{C.2}$$



(a) DC voltage controller (V^{ref}). (b) Power controller (P^{ref}).

Figure C.3: VSC d-axis controller options.

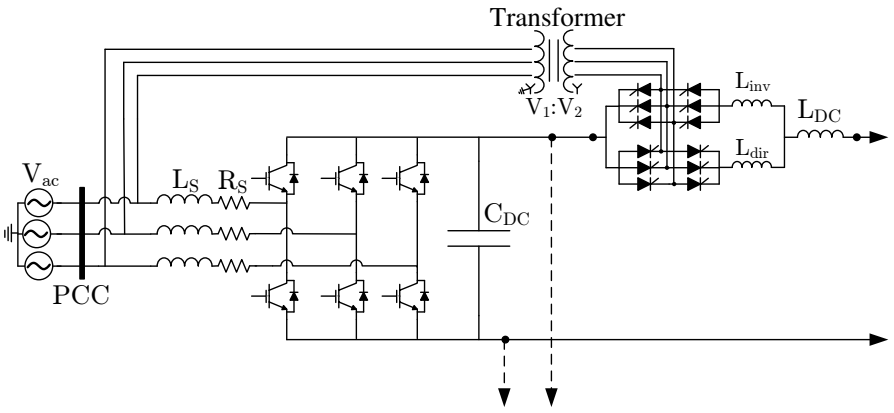


Figure C.4: VSC and thyristor power flow controller configuration.

C.2 Thyristor Power Flow Controller

The thyristor power flow controller connected to a VSC-HVDC station is shown in Figure C.4. It is connected at the point of common coupling (PCC) of the VSC via an ac transformer. The transformer has a power rating of $S_{transfo}$ in MVA and the voltage ratio $V_1 : V_2$ should be given. The leakage reactance of the transformer model is set to 0.18pu. The connection of the transformer is Y-Y where only the primary side is grounded. Each thyristor bridge has its own dc reactor labelled: L_{dir} and L_{inv}. In addition, a main dc reactor is connected at the output of the dual configuration and it is identified as L_{DC}.

The control schematic is illustrated in Figure C.5. The PI controllers are given in the form:

$$K_P \frac{s+a}{s} \tag{C.3}$$

and the input filters for the measured signals are in the form:

$$\frac{\omega_{filter}}{s+\omega_{filter}} \tag{C.4}$$

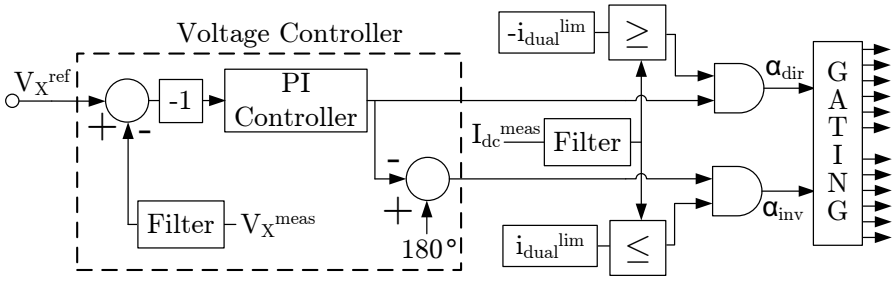
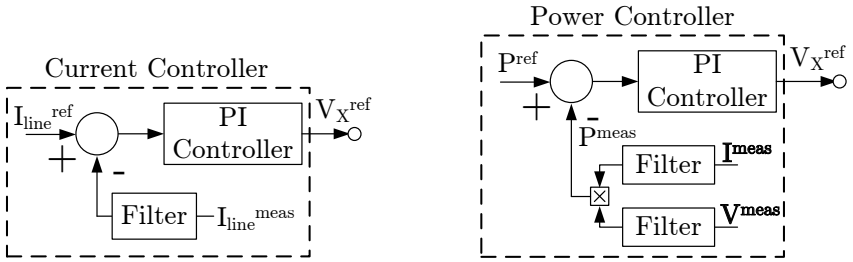


Figure C.5: Thyristor power flow controller: voltage controller.



(a) current controller. (b) Power controller.

Figure C.6: Thyristor power flow controller: V_X^{ref} controller options.

The outer loop controller options for V_X^{ref} are current and power controllers and they are both shown in Figure C.6.

C.3 HVDC Transmission Line

The transmission line model used in this work is the simple RL model with a resistance and an inductance connected in series. The transmission line parameters are taken from [86] and they are given for a voltage rating of 320kV. Although the voltage rating used in the thesis is 250kV, the parameters are still used since it gives a good approximation of the order of the parameters. Table C.1 lists the parameters on a per kilometer basis.

Table C.1: HVDC transmission line parameters

Parameter	Value	[Units]
Resistance R_{line}	0.0121	$[\Omega/km]$
Inductance L_{line}	0.1056	$[mH/km]$

C.4 3-Terminal DC Grid (Chapter 3)

This section details in Table C.2 all the parameters for the simulations of Chapter 3 done in PSCAD-EMTDC software package.

Table C.2: Simulation parameters of Chapter 3.

VSC Parameters			
	T1	T2	T3
V_{ac} $[kV_{LL}^{RMS}]$	83	83	70
f_{ac} [Hz]	50	50	50
L_s / R_s [mH/Ω]	48.88/0.92	48.88/0.92	48.88/0.92
C_{DC} [mF]	0.2	0.2	0.4
$f_{switching}$ [kHz]	1.5	1.5	1.5
d-axis / q-axis controllers			
PI Controller: K_P / a	10.8 / 18.8	10.8 / 18.8	10.8 / 18.8
ω_{filter} [rad/s]	400	400	400
Reference i_q^{ref}	0.0	0.0	0.0
d-axis outer-loop controller			
Type	P^{ref}	P^{ref}	V^{ref}
Reference	$160MW$	$80MW$	$250kV$
PI Controller: K_P	10^{-4}	10^{-4}	0.025
PI Controller: a	3.3×10^3	3.3×10^3	20
ω_{filter} [rad/s]	150	150	150

Thyristor Power Flow Controller Parameters	
L_{DC} [mH]	150
$L_{\text{dir}}, L_{\text{inv}}$ [mH]	50
Transformer $[V_1 : V_2]$	83:4.5
$S_{transfo}$ [MVA]	2.7
voltage controller	
PI Controller: K_P / a	10 / 15
ω_{filter} [rad/s]	63
i_{dual}^{lim} [kA]	0.05
current controller	
PI Controller: K_P / a	2.1 / 55
ω_{filter} [rad/s]	63

Transmission Line Parameters			
	Line L13	Line L23	Line L12
Distance [km]	248	83	165
Resistance [Ω]	3	1	2
Inductance [mH]	26.2	8.8	17.4
L_{reac} [mH]	20	20	20

C.5 7-Terminal DC Grid (Chapter 4)

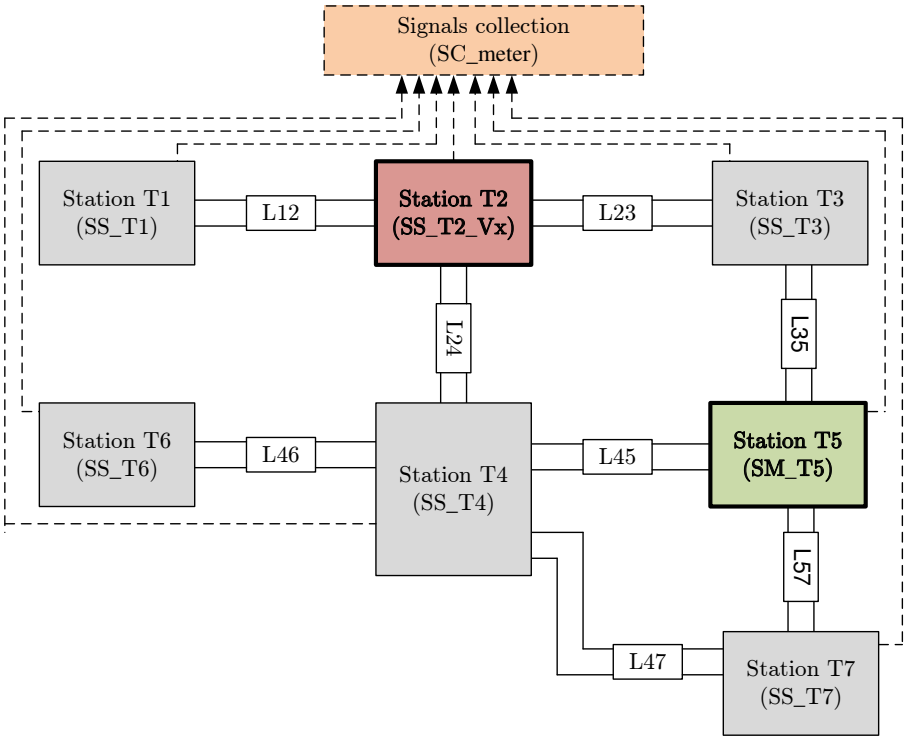


Figure C.7: Implementation overview on Opal-RT system.

This section details in Tables C.3 and C.4 all the parameters for the simulations of Chapter 4 done on the Opal-RT system. Figure C.7 shows an overview of the implementation of the MTDC grid on the multi-core application. The model is constructed such that each terminal station is implemented on an individual core. The thyristor power flow controller is included with terminal station T2.

Some adjustments have been made to adapt the simulation to the RT-LAB environment. Among them, the VSC model used is the "RTE-Drive 2-Level Time Stamped Bridge" block instead of the conventional IGBT/diode construction. For this application, the block offers good performance and it eases the VSC control interface. The VSC dq-controllers remain as previously described and implemented. For the thyristor power flow controller, conventional thyristor blocks are used.

The same parameters are used in the simulations of Chapter 10 done in PSCAD-EMTDC software package. It is important to note that VSC models for Chapter 10 are fully detailed models as described in Section C.1.

Table C.3: Simulation parameters of Chapter 4.

VSC Parameters		
	T2	T5
V_{ac} $[kV_{LL}^{RMS}]$	83	83
f_{ac} [Hz]	50	50
L_s [mH]	48.88	48.88
R_s [Ω]	0.92	0.92
C_{DC} [mF]	0.4	0.4
L_{reac}/R_{reac} [mH/Ω]	2/0.02	2/0.02
$f_{switching}$ [kHz]	1.5	1.5
d-axis / q-axis controllers		
PI Controller: K_P	28	10.8
PI Controller: a	29	18.8
ω_{filter} [rad/s]	400	400
Reference i_q^{ref}	0.0	0.0
d-axis outer-loop controller		
Type	V^{ref}	V^{ref}
Reference [kV]	250	250
PI Controller: K_P	0.32	0.32
PI Controller: a	15.6	9.4
ω_{filter} [rad/s]	150	150

	T1	T3	T4	T6	T7
V_{ac} $[kV_{LL}^{RMS}]$	83	83	83	83	83
f_{ac} [Hz]	50	50	50	50	50
L_s [mH]	48.88	48.88	48.88	48.88	48.88
R_s [Ω]	0.92	0.92	0.92	0.92	0.92
C_{DC} [mF]	0.4	0.4	0.4	0.4	0.4
L_{reac}/R_{reac} [mH/Ω]	2/0.02	2/0.02	2/0.02	2/0.02	2/0.02
$f_{switching}$ [kHz]	1.5	1.5	1.5	1.5	1.5
d-axis / q-axis controllers					
PI Controller: K_P	36	10.8	16	36	36
PI Controller: a	22.6	18.8	20	22.6	22.6
ω_{filter} [rad/s]	400	400	400	400	400
Reference i_q^{ref}	0.0	0.0	0.0	0.0	0.0
d-axis outer-loop controller					
Type	P^{ref}	P^{ref}	P^{ref}	P^{ref}	P^{ref}
Reference [MW]	200	150	-200	100	-50
PI Controller: K_P $[\times 10^{-5}]$	2	2	3	2	1
PI Controller: a $[\times 10^{3}]$	2.5	2.5	0.5	2.5	5
ω_{filter} [rad/s]	150	150	150	150	150

Table C.4: Simulation parameters of Chapter 4.

Thyristor Power Flow Controller Parameters								
L_{DC} [mH]	150							
$L_{\text{dir}}, L_{\text{inv}}$ [mH]	50							
Transformer $[V_1 : V_2]$	83:5							
$S_{transfo}$ [MVA]	5							
voltage controller								
PI Controller: K_P	10							
PI Controller: a	240							
ω_{filter} [rad/s]	62.8							
i_{dual}^{lim} [kA]	0.05							
ω_{filter} [rad/s]	62.8							
power controller								
Reference: P_{T2}^{ref} [MW]	-50							
PI Controller: K_P	3×10^{-5}							
PI Controller: a	15×10^{3}							
ω_{filter} [rad/s]	150							
Transmission Line Parameters								
Lines	L12	L23	L24	L35	L45	L46	L47	L57
Distance [km]	413	248	207	331	83	207	289	165
Resistance [Ω]	5	3	2.5	4	1	2.5	3.5	2
Inductance [mH]	44	26	22	35	9	22	31	17

Appendix D

Marx DC-DC Converter: Prototype Details

D.1 Nameplate and Drawings

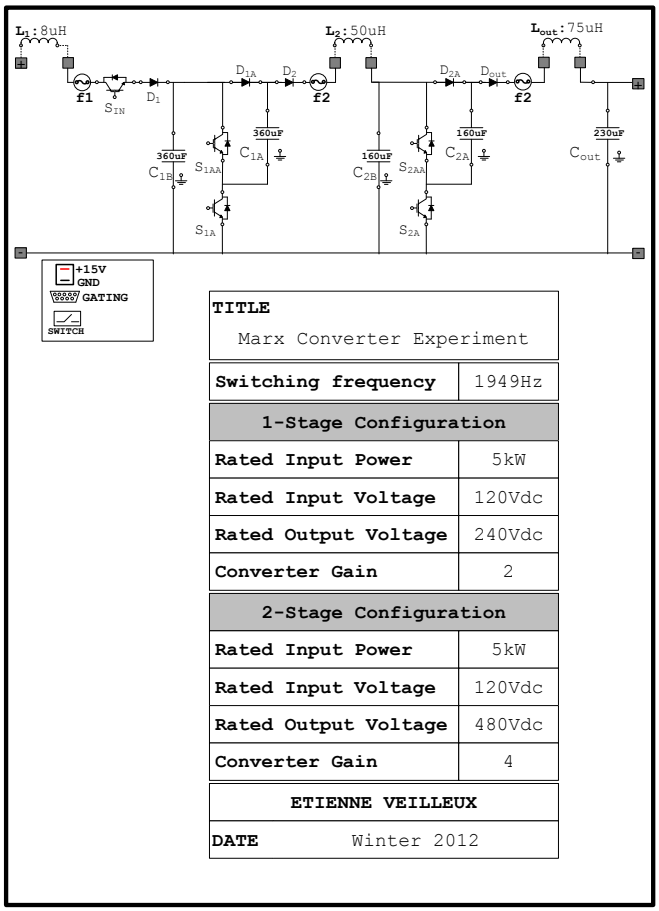
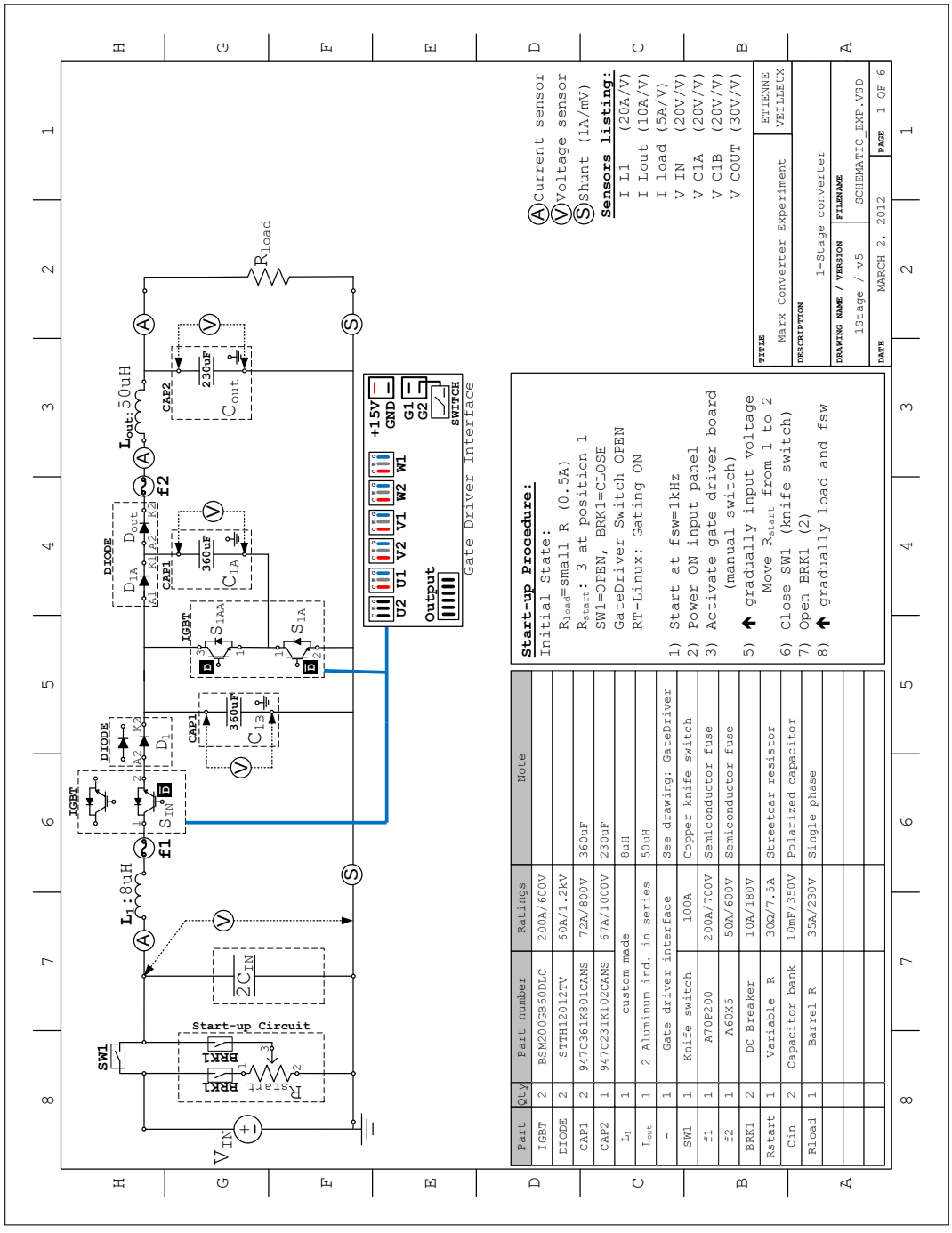
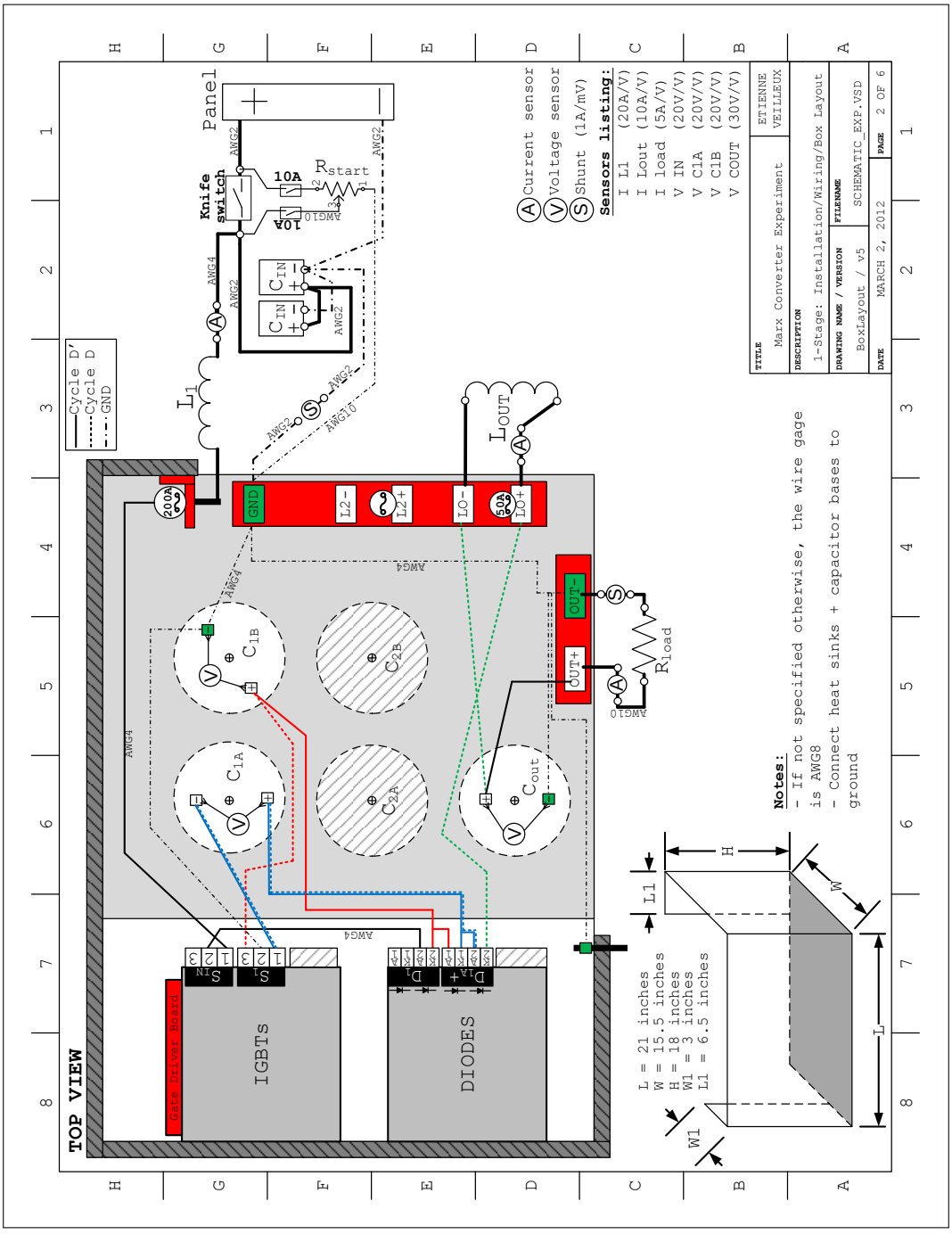
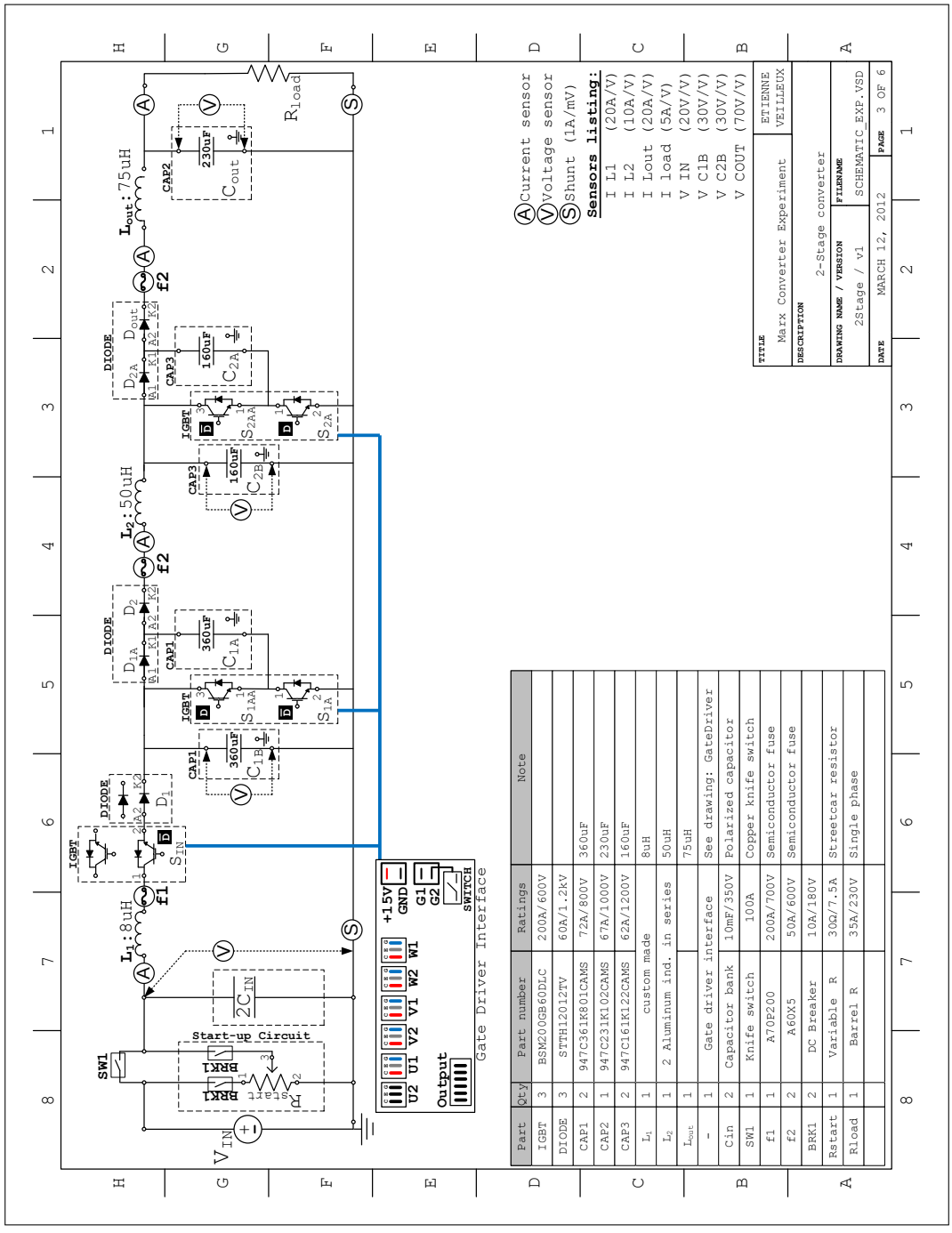


Figure D.1: Prototype nameplate.

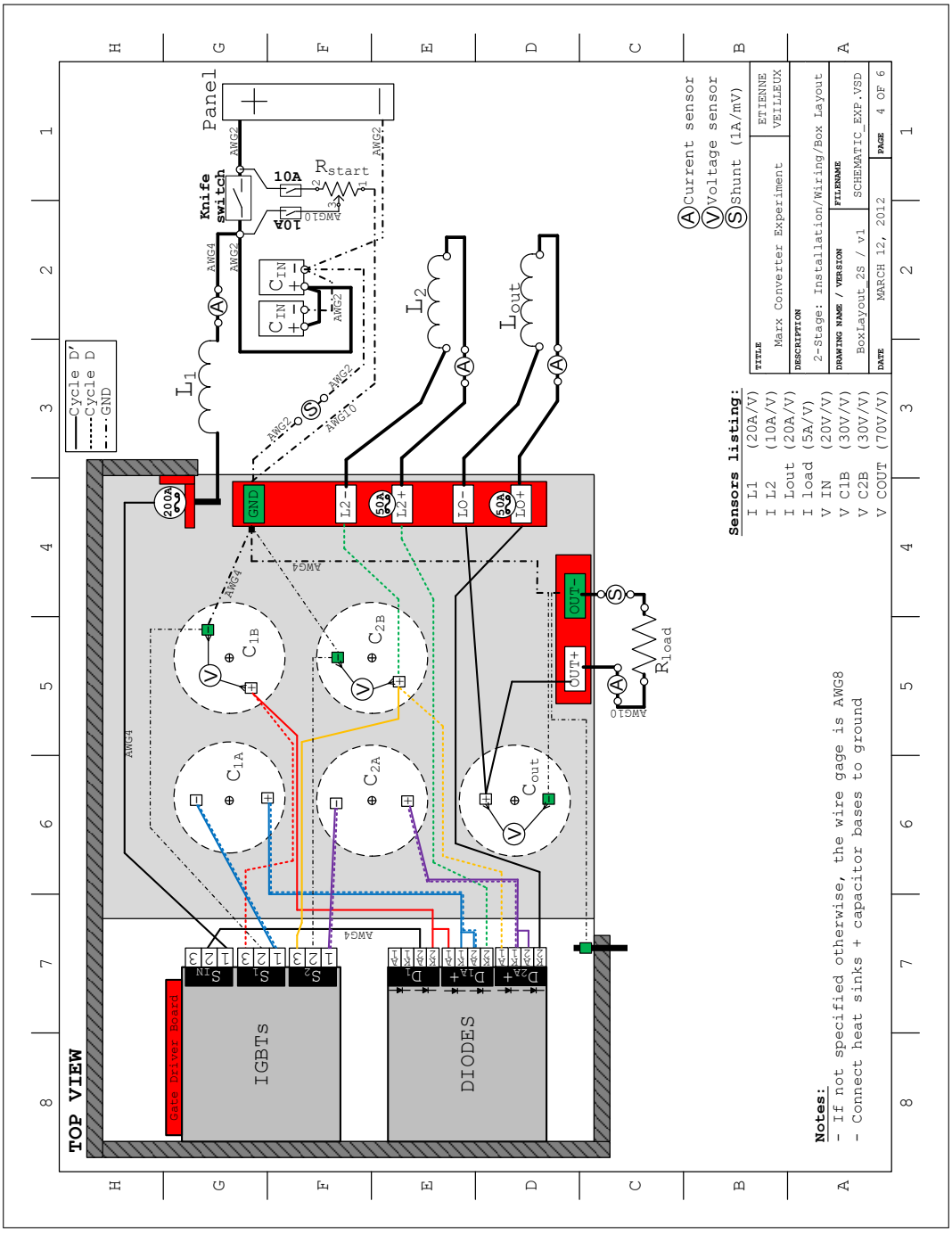


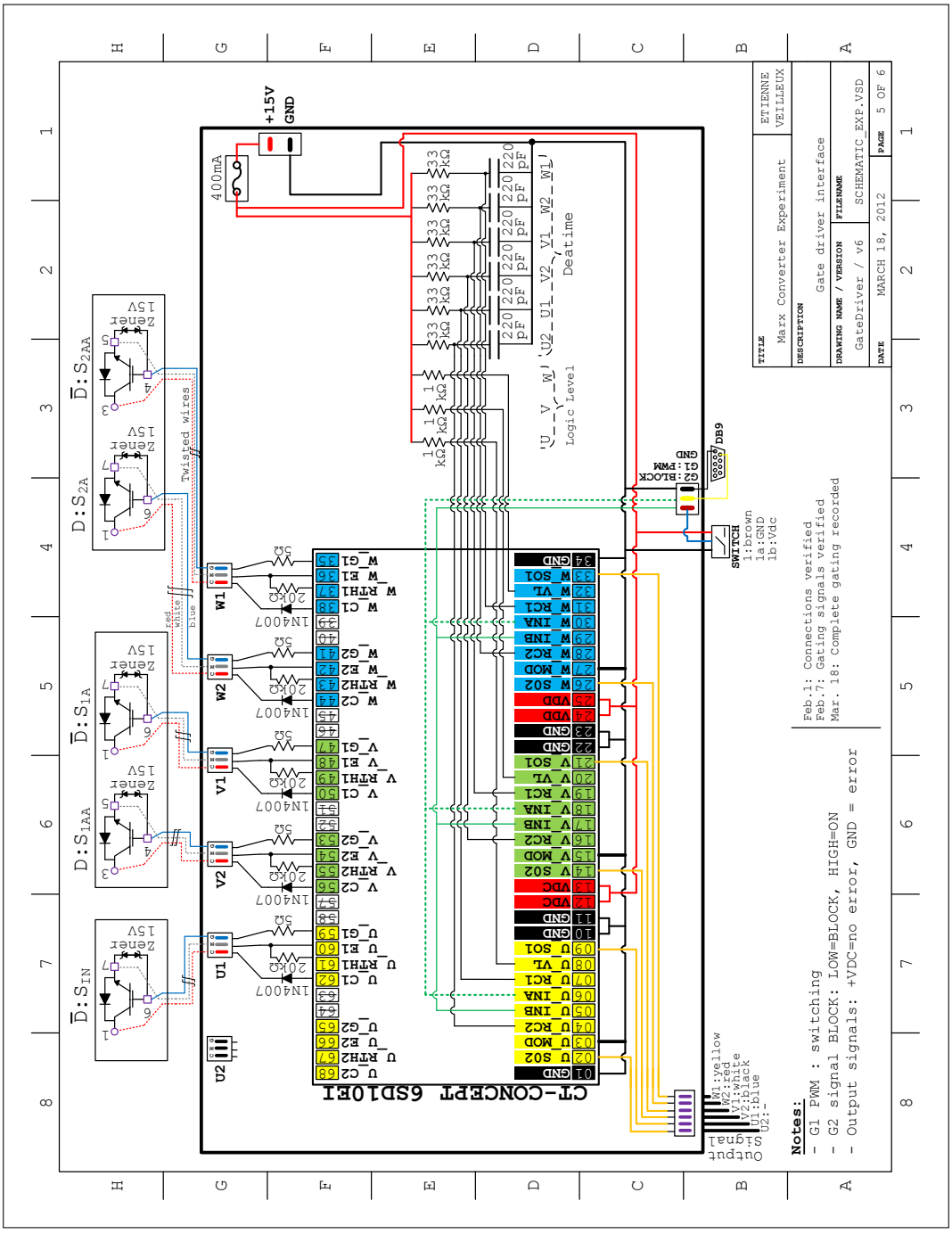
Part	Qty	Part number	Ratings	Note
IGBT	2	BSM200GB60DLC	200A/600V	
DIODE	2	SITH120120TV	60A/1.2kV	
CAP1	2	947C361K801CAMS	72A/800V	360uF
CAP2	1	947C231K102CAMS	67A/1000V	230uF
L_{1}	1	custom made		8uH
L_{out}	1	2 Aluminum ind. in series		50uH
-	1	Gate driver interface		See drawing: GateDriver
SW1	1	Knife switch	100A	Copper knife switch
f1	1	A70P200	200A/700V	Semiconductor fuse
f2	1	A60X5	50A/600V	Semiconductor fuse
BRK1	2	DC Breaker	10A/180V	
Rstart	1	Variable R	30Ω/7.5A	Streetcar resistor
Cin	2	Capacitor bank	10mF/350V	Polarized capacitor
Rload	1	Barrel R	35A/230V	Single phase

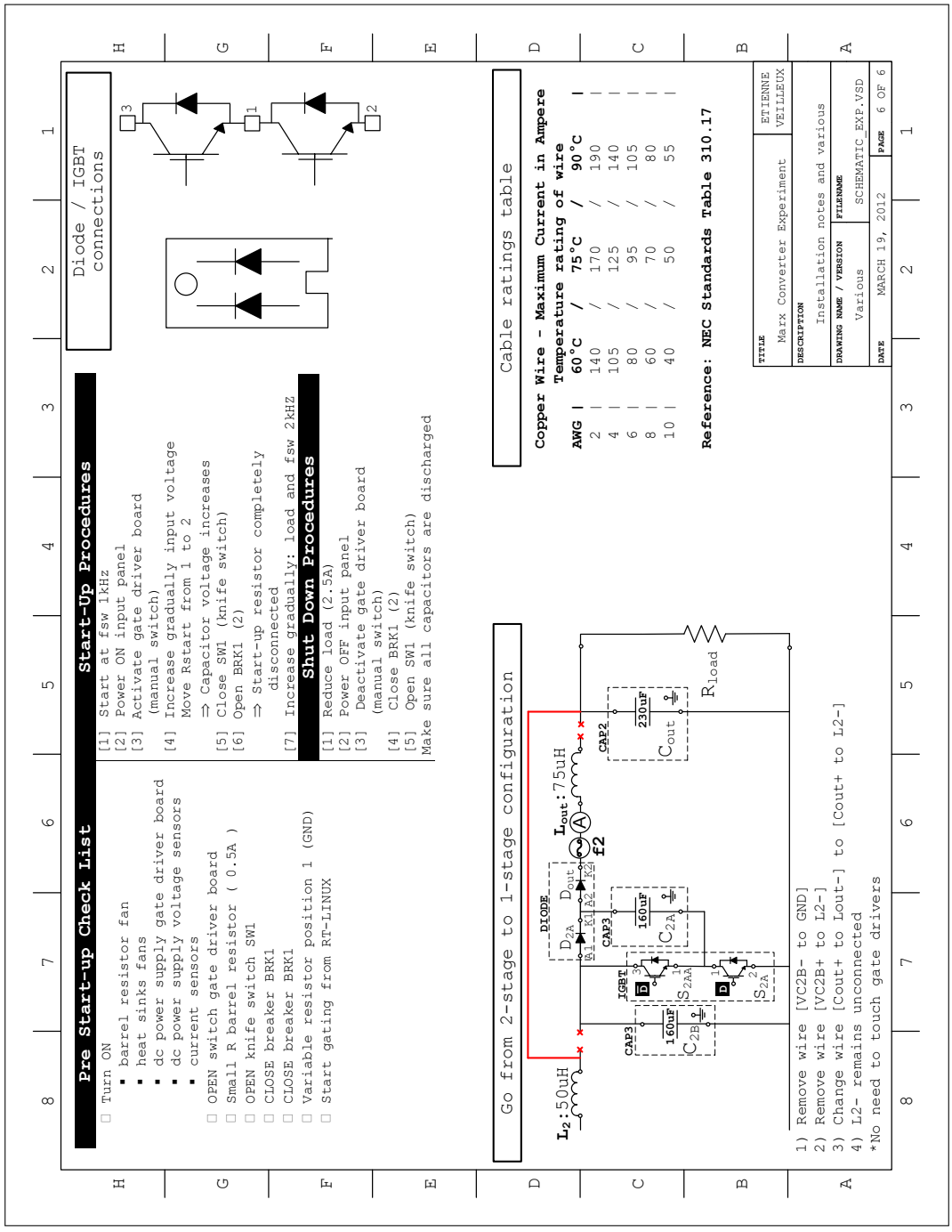

TOP VIEW
IGBTs
DIODES
Gate Driver Board
Panel
Knife switch
10A
Rstart
CIN
L1
LOUT
Rload
C1A
C1B
C2A
C2B
Cout
GND
L2-
L2+
LO-
LO+
OUT-
OUT+
200A
50A
AWG2
AWG4
AWG10
Cycle D'
Cycle D
GND
Current sensor
Voltage sensor
Shunt (1A/mV)
Sensors listing:
I L1 (20A/V)
I Lout (10A/V)
I load (5A/V)
V IN (20V/V)
V C1A (20V/V)
V C1B (20V/V)
V COUT (30V/V)
Notes:
- If not specified otherwise, the wire gage is AWG8
- Connect heat sinks + capacitor bases to ground
L = 21 inches
W = 15.5 inches
H = 18 inches
W1 = 3 inches
L1 = 6.5 inches
TITLE
Marx Converter Experiment
ETIENNE VEILLEUX
DESCRIPTION
1-Stage: Installation/Wiring/Box Layout
DRAWING NAME / VERSION
BoxLayout / v5
FILENAME
SCHEMATIC_EXP.VSD
DATE
MARCH 2, 2012
PAGE
2 OF 6



Part	Qty	Part number	Ratings	Note
IGBT	3	BSM200GB60DLC	200A/600V	
DIODE	3	SITH120120TV	60A/1.2kV	
CAP1	2	947C361K801CAMS	72A/800V	360uF
CAP2	1	947C231K102CAMS	67A/1000V	230uF
CAP3	2	947C161K122CAMS	62A/1200V	160uF
L_1	1	custom made		8uH
L_2	1	2 Aluminum ind. in series		50uH
L_{out}	1			75uH
-	1	Gate driver interface		See drawing: GateDriver
Cin	2	Capacitor bank	10mF/350V	Polarized capacitor
SW1	1	Knife switch	100A	Copper knife switch
f1	1	A70P200	200A/700V	Semiconductor fuse
f2	2	A60X5	50A/600V	Semiconductor fuse
BRK1	2	DC Breaker	10A/180V	
Rstart	1	Variable R	30Ω/7.5A	Streetcar resistor
Rload	1	Barrel R	35A/230V	Single phase


TOP VIEW
Gate Driver Board
IGBTs
DIODES
Panel
Knife switch
10A
10A
Rstart
L1
L2
Lout
CIN
CIN
Cycle D'
Cycle D
GND
Current sensor
Voltage sensor
Shunt (1A/mV)
Sensors listing:
I L1 (20A/V)
I L2 (10A/V)
I Lout (20A/V)
I load (5A/V)
V IN (20V/V)
V C1B (30V/V)
V C2B (30V/V)
V COUT (70V/V)
Notes:
- If not specified otherwise, the wire gage is AWG8
- Connect heat sinks + capacitor bases to ground
TITLE
Marx Converter Experiment
ETIENNE VEILLEUX
DESCRIPTION
2-Stage: Installation/Wiring/Box Layout
DRAWING NAME / VERSION
BoxLayout_2S / v1
FILENAME
SCHEMATIC_EXP.VSD
DATE
MARCH 12, 2012
PAGE 4 OF 6


+15V
GND
400mA
33 kΩ
220 pF
1 kΩ
Logic Level
Deatime
U_V_W1'U2_U1_V2_V1_W2_W1'
CT-CONCEPT 6SD10EI
SWITCH
1:brown
1a:GND
1b:Vdc
G2:BLOCK
G1:PWM
GND
DB9
Twisted wires
red
white
blue
Zener 15V
D:S2AA
D:S2A
D:S1A
D:S1AA
D:SIN
W1
W2
V1
V2
U1
U2
1N4007
20kΩ
52Ω
W_C1
W_RTH1
W_E1
W_G1
W_C2
W_RTH2
W_E2
W_G2
V_C1
V_RTH1
V_E1
V_G1
V_C2
V_RTH2
V_E2
V_G2
U_C1
U_RTH1
U_E1
U_G1
U_C2
U_RTH2
U_E2
U_G2
01 GND
02 U_S02
03 U_MOD
04 U_RC2
05 U_INB
06 U_INA
07 U_RC1
08 U_VL
09 U_SO1
10 GND
11 GND
12 VDC
13 VDC
14 V_S02
15 V_MOD
16 V_RC2
17 V_INB
18 V_INA
19 V_RC1
20 V_VL
21 V_SO1
22 GND
23 GND
24 VDD
25 VDD
26 W_S02
27 W_MOD
28 W_RC2
29 W_INB
30 W_INA
31 W_RC1
32 W_VL
33 W_SO1
34 GND
Output signal
W1:yellow
W2:red
V1:white
V2:black
U1:blue
U2:-
TITLE
Marx Converter Experiment
DESCRIPTION
Gate driver interface
DRAWING NAME / VERSION
GateDriver / v6
FILENAME
SCHEMATIC_EXP.VSD
DATE
MARCH 18, 2012
PAGE 5 OF 6
ETIENNE VEILLEUX
Feb.1: Connections verified
Feb.7: Gating signals verified
Mar. 18: Complete gating recorded
Notes:
- G1 PWM : switching
- G2 signal BLOCK: LOW=BLOCK, HIGH=ON
- Output signals: +VDC=no error, GND = error


Pre Start-up Check List
Turn ON
▪ barrel resistor fan
▪ heat sinks fans
▪ dc power supply gate driver board
▪ dc power supply voltage sensors
▪ current sensors
OPEN switch gate driver board
Small R barrel resistor (0.5A)
OPEN knife switch SW1
CLOSE breaker BRK1
CLOSE breaker BRK1
Variable resistor position 1 (GND)
Start gating from RT-LINUX
Start-Up Procedures
[1] Start at fsw 1kHz
[2] Power ON input panel
[3] Activate gate driver board (manual switch)
[4] Increase gradually input voltage Move Rstart from 1 to 2
⇒ Capacitor voltage increases
[5] Close SW1 (knife switch)
[6] Open BRK1 (2)
⇒ Start-up resistor completely disconnected
[7] Increase gradually: load and fsw 2kHz
Shut Down Procedures
[1] Reduce load (2.5A)
[2] Power OFF input panel
[3] Deactivate gate driver board (manual switch)
[4] Close BRK1 (2)
[5] Open SW1 (knife switch)
Make sure all capacitors are discharged
Diode / IGBT connections
Cable ratings table
Copper Wire - Maximum Current in Ampere
Temperature rating of wire
AWG | 60°C / 75°C / 90°C
2 | 140 / 170 / 190
4 | 105 / 125 / 140
6 | 80 / 95 / 105
8 | 60 / 70 / 80
10 | 40 / 50 / 55
Reference: NEC Standards Table 310.17
Go from 2-stage to 1-stage configuration
L2:50uH
Lout:75uH
f2
DIODE
D2A
Dout
K1 A2 K2
CAP3
160uF
C2A
IGBT
S2AA
S2A
C2B
CAP2
230uF
Cout
Rload
1) Remove wire [VC2B- to GND]
2) Remove wire [VC2B+ to L2-]
3) Change wire [Cout+ to Lout-] to [Cout+ to L2-]
4) L2- remains unconnected
*No need to touch gate drivers
TITLE
Marx Converter Experiment
ETIENNNE VEILLEUX
DESCRIPTION
Installation notes and various
DRAWING NAME / VERSION
Various
FILENAME
SCHEMATIC_EXP.VSD
DATE
MARCH 19, 2012
PAGE 6 OF 6

D.2 Pictures

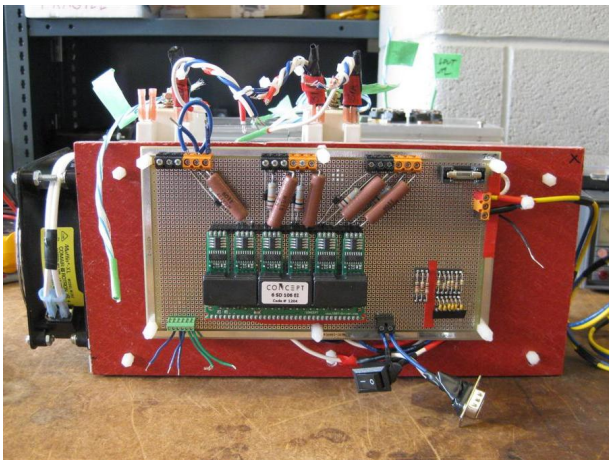


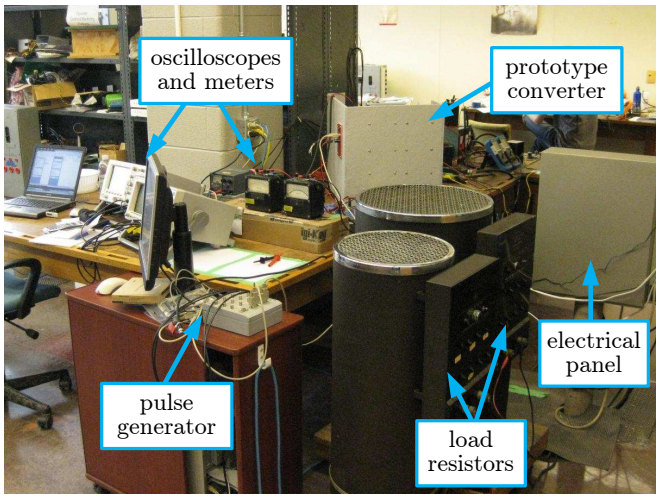
Figure D.2: Gate driver interface board.

(a) L_1: custom-made air-core inductor made with Litz wire.

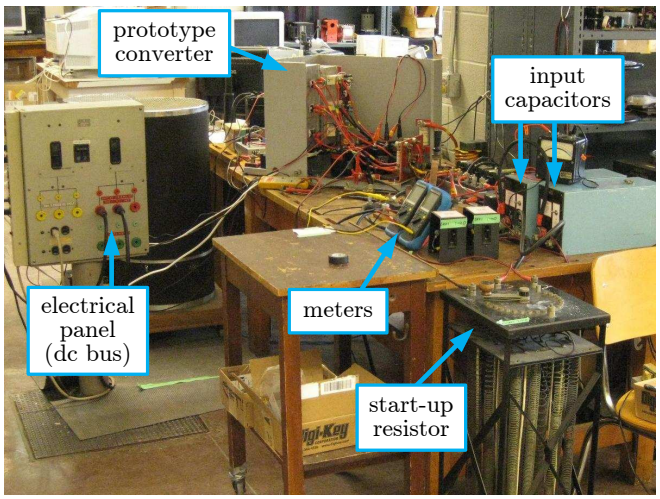
(b) L_{OUT}: custom-made ferrite-core inductor made with Litz wire.

(c) L_2: air-core inductor made with aluminum.

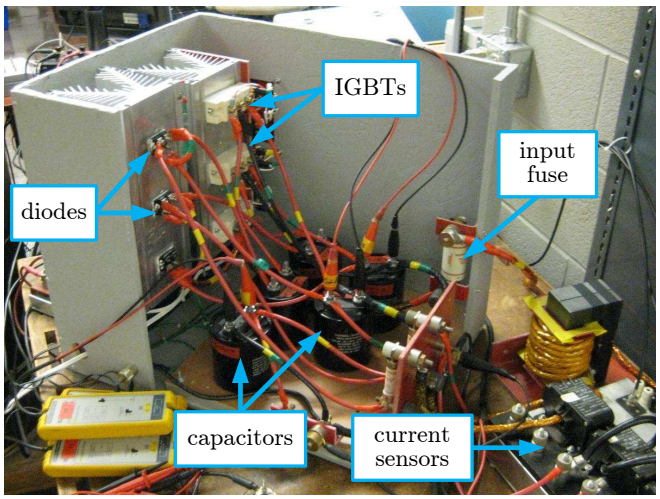
Figure D.3: Inductors used for experimental work.



(a) Measurement and control side.



(b) Complete setup arrangement.



(c) Prototype converter.

Figure D.4: Pictures of laboratory setup for prototype experiment.

D.3 Simulation Model

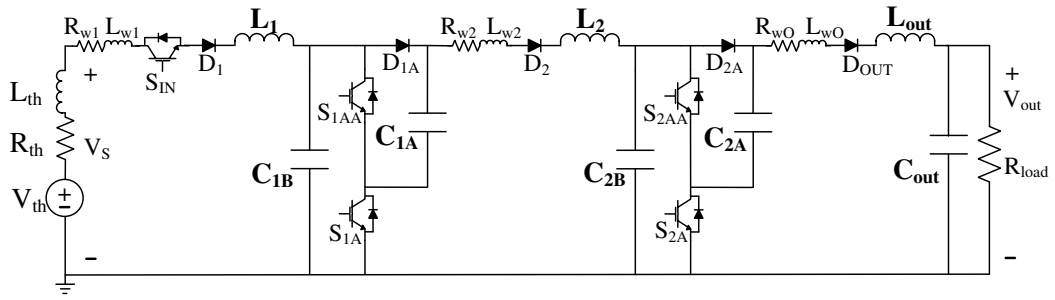


Figure D.5: Detailed simulation model implemented in PSCAD-EMTDC software package.

Table D.1: Simulation model parameters.

Capacitors		**IGBTs**	
C_{1A} [uF]	366	S_{IN}	
C_{1B} [uF]	366	ON resistance [mΩ]	6
C_{2A} [uF]	151	Foward voltage drop [V]	1.8
C_{2B} [uF]	152	S_{1AA}, S_{1A}, S_{2AA}, S_{2A}	
C_{OUT} [uF]	233	ON resistance [mΩ]	6
Inductors		Foward voltage drop [V]	0.6
L_1 / R_{L1} [uH / mΩ]	4.9 / 3	**Diodes**	
L_2 / R_{L2} [uH / mΩ]	50 / 4	D_1	
L_{OUT} / R_{LOUT} [uH / mΩ]	95.3 / 4	ON resistance [mΩ]	6
Wires		Foward voltage drop [V]	1.37
L_{w1} / R_{w1} [uH / mΩ]	1.6 / 1	D_{1A}, D_2, D_{2A}, D_{OUT}	
L_{w2} / R_{w2} [uH / mΩ]	0 / 60	ON resistance [mΩ]	6
L_{wO} / R_{wO} [uH / mΩ]	6 / 30	Foward voltage drop [V]	0.7
Input Source		**Output Load**	
(Thévenin-equivalent)		R_{LOAD} [Ω]	34.72
V_S [V]	109.5		
R_{th} [mΩ]	16		
L_{th} [uH]	1.5		

Bibliography

[1] Siemens, "Siemens to deliver new HVDC technolgy for low-loss power supply via submarine cable to San Francisco," [Press release], Available: www.energy.siemens.com.

[2] S. P. Teeuwsen, "Modeling the Trans Bay Cable Project as Voltage-Sourced Converter with Modular Multilevel Converter Design," in *IEEE Power and Energy Society General Meeting*, July 2011.

[3] ABB, "Grid connection of offshore wind farms - BorWin1," [Brochure], Available: www.abb.com/hvdc.

[4] U. Lamm, E. Uhlmann, and P. Danfors, "Some Aspects of Tapping H.V.D.C. Transmission Systems," *Direct Current*, vol. 8, no. 5, pp. 124–129, May 1963.

[5] R. Foerst, G. Heyner, K. Kanngiesser, and H. Waldmann, "Multiterminal operation of hvdc converter stations," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-88, pp. 1042–1052, 1969.

[6] G. Asplund, B. Jacobson, B. Berggren, and K. Lindén, "Continental Overlay HVDC-Grid ," in *CIGRÉ 2010 Session*, 2010.

[7] S. Gordon, "Supergrid to the rescue," *PowerEngineer*, vol. 20, no. 5, pp. 30–33, 2006.

[8] P. Fairley, "A Supergrid for Europe," *Technology Review*, March 2006.

[9] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 9, pp. 3156–3163, 2010.

[10] G. Asplund, "HVDC grids - possibilities and challenges," in *CIGRÉ SC B4 2009 Bergen Colloquium*, 2009.

[11] BARD Engineering GmbH, "Electricity from the SEA," *BARD Magazine*, no. 12, pp. 4–7, July 2010. [Online]. Available: www.bard-offshore.de

[12] Tennet TSO B.V., " BorWin1 The world's longest direct current connection ," [Brochure], Available: www.tennettso.de.

[13] CIGRÉ Working Group B3.26, "Guidelines for the Design and Construction of AC Offshore Substations for Wind Power Plants," *Brochure 483*, Dec. 2011.

[14] J. Arrillaga, Y. H. Liu, and N. R. Watson, *Flexible Power Transmission: The HVDC Options*. John Wiley & Sons, 2007.

[15] N. G. Hingorani and L. Gyugyi, *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*. John Wiley & Sons, 2000.

[16] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *IEEE Bologna PowerTech Conference*, vol. 3, 2003.

[17] S. Allebrod, R. Hamerski, and R. Marquardt, "New Transformerless, Scalable Modular Multilevel Converters for HVDC-transmission," in *IEEE Power Electronics Specialists Conference*, June 2008, pp. 174–179.

[18] L. Tang and B. T. Ooi, " Protection of VSC-multi-terminal HVDC against DC faults," in *IEEE 33rd Annual Power Electronics Specialists Conference*, vol. 2, June 2002, pp. 719–724.

[19] C. Meyer, M. Kowal, and R. W. De Doncker, "Circuit breaker concepts for future high-power DC-applications," in *14th Industry Applications Society Annual Meeting*, vol. 2, Oct. 2005, pp. 860–866.

[20] J. Yang, J. E. Fletcher, and J. O'Reilly, "Multiterminal DC Wind Farm Collection Grid Internal Fault Analysis and Protection Design," *IEEE Trans. on Power Del.*, vol. 25, pp. 2308–2318, Oct. 2010.

[21] J. Häfner and B. Jacobson, "Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids," in *CIGRÉ 2011 Bologna Symposium*, 2011.

[22] C. M. Franck, "HVDC Circuit Breakers: A Review Identifying Future Research Needs," *IEEE Trans. on Power Del.*, vol. 26, pp. 998–1007, April 2011.

[23] J. Descloux, P. Rault, S. Nguefeu, J. Curis, X. Guillayd, F. Colas, and B. Raison, "HVDC meshed grid: Control and protection of a multi-terminal HVDC system," in *CIGRÉ 2012 Session*, 2012.

[24] D. G. Chapman, J. B. Davies, J. R. McNichol, E. M. Gulachenski, S. Doe, and N. J. Balu, "Test experience with multiterminal HVDC load flow and stability programs," *IEEE Trans. Power Del.*, vol. 3, pp. 1173–1181, July 1988.

[25] C. D. Barker and R. Whitehouse, "Autonomous converter control in a multi-terminal HVDC system," in *IET International Conference on AC and DC Power Transmission*, Oct. 2010.

[26] J. Liang, T. Jing, O. Gomis-Bellmunt, J. Ekanayake, and N. Jenkins, "Operation and Control of Multiterminal HVDC Transmission for Offshore Wind Farms," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2596–2604, Oct. 2011.

[27] D. Jovcic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *IEEE Trans. Power Del.*, vol. 25, pp. 2535 –2543, Oct. 2010.

[28] E. Prieto-Araujo, F. D. Bianchi, A. Junyent-Ferre, and O. Gomis-Bellmunt, "Methodology for Droop Control Dynamic Analysis of Multiterminal VSC-HVDC Grids for Offshore Wind Farms," *IEEE Trans. Power Del.*, vol. 26, pp. 2476–2485, Oct. 2011.

[29] C. Dierckxsens, K. Srivastava, M. Reza, S. Cole, J. Beerten, and R. Belmans, " A distributed DC voltage control method for VSC MTDC systems," *Electric Power Systems Research*, vol. 82, no. 1, pp. 54–58, Jan. 2012.

[30] T. M. Haileselassie and K. Uhlen, "Precise control of power flow in multi-terminal VSC-HVDCs using DC voltage droop control," in *IEEE Power and Energy Society General Meeting*, July 2012.

[31] F. Schettler, G. Balzer, M. Hyttinen, S. E. Rye, and T. Westerweller, "Technical guidelines for first HVDC grids - A European study group based on an initiative of the German commission for electrical, electronic & information technologies," in *CIGRÉ 2012 Session*, 2012.

[32] P. Kundur, *Power System Stability and Control*. McGraw-Hill, 1994.

[33] M. Liserre, R. Cardenas, M. Molinas, and J. Rodriguez, "Overview of Multi-MW Wind Turbines and Wind Parks," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 1081–1095, April 2011.

[34] T. K. Vrana and O. B. Fosso, "Technical aspects of the North Sea Super Grid," *Electra*, no. 258, pp. 5–19, Oct. 2011.

[35] C. Meyer, M. Höing, A. Peterson, and R. W. De Doncker, "Control and Design of DC Grids for Offshore Wind Farms," *IEEE Trans. on Ind. Appl.*, vol. 43, pp. 1475–1482, Nov./Dec. 2007.

[36] P. K. Steimer and O. Apeldoorn, "Medium voltage power conversion technology for efficient windpark power collection grids," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems*, June 2010.

[37] J. Robinson, D. Jovcic, and G. Joos, "Analysis and Design of an Offshore Wind Farm Using a MV DC Grid," *IEEE Trans. Power Del.*, vol. 25, pp. 2164 –2173, Oct. 2010.

[38] S. M. Muyeen, R. Takahashi, and J. Tamura, "Operation and Control of HVDC-Connected Offshore Wind Farm," *IEEE Trans. Sustainable Energy*, vol. 1, pp. 30–37, April 2010.

[39] F. Deng and Z. Chen, "An Offshore Wind Farm with DC Grid Connection and Its Performance under Power System Transients," in *IEEE Power and Energy Society General Meeting*, July 2011.

[40] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Springer, 2001.

[41] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. John Wiley & Sons, 2002.

[42] D. W. Hart, *Introduction to Power Electronics*. Prentice Hall, 1997.

[43] F. L. Luo and H. Ye, *Advanded DC/DC Converters*. CRC Press LLC, 2004.

[44] E. Marx, *Verfahren zur Schlagprüfung von Isolatoren und anderen elektrischen Vorrichtungen*. German Patent 455933, 1923.

[45] E. Marx, "Versuche über die Prüfung von Isolatoren mit Spannungsstößen," *Elektrotechnische Zeitschrift*, vol. 45, pp. 652–654, June 1924.

[46] ABB Power T&D Company Inc., *Electrical Transmission and Distribution Reference Book*, 5th ed. ABB Power T&D Company Inc., 1997.

[47] C. G. Clayton, "The generation of recurring high-voltage X-ray impulses," *Proceedings of the IEE - Part I: General*, vol. 119, pp. 206–213, Sept. 1952.

[48] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, pp. 1098–1102, Aug. 2003.

[49] J. W. Baek, D. W. Yoo, G. H. Rim, and J. Lai, "Solid State Marx Generator Using Series-Connected IGBTs," *IEEE Trans. Plasma Sci.*, vol. 33, pp. 1198–1204, Aug. 2005.

[50] L. M. Redondo, J. F. Silva, P. Tavares, and E. Margato, "All Silicon Marx-bank Topology for High-voltage, High-frequency Rectangular Pulses," in *IEEE 36th Power Electronics Specialists Conference*, June 2005, pp. 1170–1174.

[51] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched Capacitor DC-DC Converters," *IEEE Trans. Power Electon.*, vol. 23, pp. 841–851, March 2008.

[52] L. M. Redondo and J. F. Silva, "Repetitive High-Voltage Solid-State Marx Modulator Design for Various Load Conditions," *IEEE Trans. Plasma Sci.*, vol. 37, pp. 1632–1637, Aug. 2009.

[53] S. Bae, A. Kwasinski, M. M. Flynn, and R. E. Hebner, "High-Power Pulse Generator With Flexible Output Pattern ," *IEEE Trans. on Power Electron.*, vol. 25, pp. 1675–1684, July 2010.

[54] L. M. Redondo, "A DC Voltage-Multiplier Circuit Working as High-Voltage Pulse Generator," *IEEE Trans. Plasma Sci.*, vol. 38, pp. 2725–2729, Oct. 2010.

[55] S. Zabihi, Z. Zabihi, and F. Zare, "A Solid-State Marx Generator With a Novel Configuration," *IEEE Trans. Plasma Sci.*, vol. 39, pp. 1721–1728, Aug. 2011.

[56] M. A. Kemp, A. Benwell, C. Burkhart, R. Larsen, D. MacNair, M. Nguyen, and J. Olsen, "Status Update on the Second-Generation ILC Marx Modulator Prototype," in *IEEE Int. Power Modulator and High Voltage Conf.*, 2010, pp. 23–26.

[57] M. A. Kemp, A. Benwell, C. Burkhart, R. Larsen, D. MacNair, M. Nguyen, and J. Olsen, "Final Design of the SLAC P2 Marx Klystron Modulator," in *2011 IEEE Pulsed Power Conf.*, 2011, pp. 1582–1589.

[58] J. J. Cooley and S. B. Leeb, " Per panel photovoltaic energy extraction with multilevel output DC-DC switched capacitor converters," in *26th Annu. IEEE Applied Power Electronics Conf. and Expo.*, 2011, pp. pp.419–428.

[59] A. Lopez, R. Diez, G. Perilla, and D. Patino, "Analysis and Comparison of Three Topologies of the Ladder Multilevel DC/DC Converter," *IEEE Trans. on Power Electron.*, vol. 27, pp. 3119–3127, July 2012.

[60] S. B. Ok, H. J. Ryoo, S. R. Jang, S. H. Ahn, and G. Goussev, "Design of a High-Efficiency 40-kV, 150-A, 3-kHz Solid-State Pulsed Power Modulator," *IEEE Trans. on Plasma Sci.*, vol. 40, pp. 2569–2577, Oct. 2012.

[61] T. Sakamoto, A. Nami, M. Akiyama, and H. Akiyama, "A Repetitive Solid State Marx-Type Pulsed Power Generator Using Multistage Switch-Capacitor Cells," *IEEE Trans. on Plasma Sci.*, vol. 40, pp. 2316–2321, Oct. 2012.

[62] R. D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," *IEEE Trans. Power Electron.*, vol. 3, pp. 484–488, Oct. 1988.

[63] J. A. Morales-Saldana, E. E. C. Gutierrez, and J. Leyva-Ramos, "Modeling of switch-mode dc-dc cascade converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, pp. 295–299, Jan. 2002.

[64] F. L. Luo and H. Ye, "Positive output cascade boost converters," *IEE Proc. - Electric Power Applications*, vol. 151, no. 5, pp. 590–606, Sept. 2004.

[65] M. G. Ortiz-Lopez, J. Leyva-Ramos, E. E. Carbajal-Gutierrez, and J. A. Morales-Saldana, "Modelling and analysis of switch-mode cascade converters with a single active switch," *IET Power Electronics*, vol. 1, no. 4, pp. 478–487, Dec. 2008.

[66] D. Jovcic and B. T. Ooi, "Tapping on HVDC lines using DC transformers," *Electric Power Systems Research*, vol. 81, no. 2, pp. 561–569, Feb. 2011.

[67] W. F. Long, J. Reeve, J. R. McNichol, M. S. Holland, J. P. Taisne, J. LeMay, and D. J. Lorden, "Application aspects of multiterminal DC power transmission," *IEEE Trans. Power Del.*, vol. 5, pp. 2084–2098, Oct. 1990.

[68] A. Ekstrom and P. Lamell, "HVDC tapping station: power tapping from a DC transmission line to a local AC network," in *International Conference on AC and DC Power Transmission*, Sept. 1991, pp. 126–131.

[69] Z. Zhao and M. R. Iravani, "Application of GTO voltage-source inverter for tapping HVDC power," *IEE Proc. - Generation, Transmission and Distribution,*, vol. 141, no. 1, pp. 19–26, Jan. 1994.

[70] M. R. Aghaebrahimi and R. W. Menzies, "Small power tapping from HVDC transmission systems: a novel approach," *IEEE Trans. Power Del.*, vol. 12, pp. 1698–1703, Oct. 1997.

[71] G. Asplund and A. Williamson, "A novel approach to providing on route power supplies to rural and urban communities in close proximity to the

extra high voltage DC transmission line," in *IEEE PES Conference and Exposition in Africa*, July 2007.

[72] P. C. Sen, *Thyristors DC Drives*. Wiley-Interscience, 1981.

[73] C.-K. Kim, V. K. Sood, G.-S. Jang, S.-J. Lim, and S.-J. Lee, *HVDC Transmission: Power Conversion Applications in Power Systems*. Wiley-IEEE Press, 2009.

[74] A. Yazdani and R. Iravani, *Voltage-Sources Converters in Power Systems: Modeling, Control and Applications*. John Wiley & Sons, 2010.

[75] Opal-RT Technologies, "RT-LAB Version 10.2 User Guide," 2007.

[76] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 5th ed. Prentice Hall, 2009.

[77] R. E. Thomas and A. J. Rosa, *The Analysis and Design of Linear Circuits: Laplace Early*, 4th ed. John Wiley & Sons, 2004.

[78] S. Lee, "Optimum design and selection of heat sinks," *IEEE Trans. Compon. Packag. Manuf. Technol. A*, vol. 18, pp. 812–817, Dec. 1995.

[79] D. S. Watkins, *Fundamentals of Matrix Computations*, 2nd ed. John Wiley & Sons, 2002.

[80] I. N. Bronshtein, K. A. Semendyayev, G. Musiol, and H. Muehlig, *Handbook of Mathematics*, 5th ed. Springer, 2007.

[81] E. Veilleux and P. W. Lehn, "Interconnection of direct-drive wind turbines using a distributed HVDC converter station," in *35th Annual Conference of IEEE Industrial Electronics*, Nov. 2009.

[82] E. Veilleux, "Interconnection of Direct-Drive Wind Turbines Using a Series Connected DC Grid," Master's thesis, University of Toronto, 2009.

[83] Z. Chen and E. Spooner, "Grid Power Quality with Variable Speed Wind Turbines," *IEEE Trans. Energy Convers.*, vol. 16, pp. 148–154, June 2001.

[84] CIGRÉ Working Group B4, "Study committee B4 Annual Report 2011," *Electra*, no. 262, pp. 17–21, June 2012.

[85] J. D. Glover, M. S. Sarma, and T. J. Overbye, *Power System Analysis and Design*, 4th ed. Thomson, 2008.

[86] D. Van Hertem, M. Ghandhari, J. B. Curis, O. Despouys, and A. Marzin, "Protection requirements for a multi-terminal meshed DC grid," in *CIGRÉ 2011 Bologna Symposium*, 2011.