Modular Multilevel Converter HVDC Based on Harmonic Function Analysis

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Abstract

Modular Multilevel Converter (MMC) features many advantages for high-voltage direct current (HVDC) transmission. Using modulation by phase-shifted triangular carrier, MMC has low switching loss and low harmonic distortion in the high frequency spectrum. While the low frequency distortions, especially the 2nd harmonics, proliferated by single-phase ac power, have to be filtered by large capacitors in the sub-modules. In this thesis, harmonic function analysis is applied to pin-point the source of 2nd harmonic circulating current in MMC. After extending harmonic function analysis, a feed-forward elimination method is proposed by modifying the modulation signal. Analytical insight enables the 2nd harmonic circulating current to be eliminated at the source and, in turn, other low-order harmonic voltages which are proliferated from the 2nd. In order to prevent large fault currents to overcharge the sub-module capacitor and ensure the viability of the feed-forward elimination method, deadbeat control is incorporated in MMC. With deadbeat, MMC becomes a reference current regulator; the ac currents in tracking the current references do not rise to destructively large values during ac faults. Likewise, inherent MMC 3rd harmonic currents on the ac-side cannot flow. This frees MMC from the necessity of having delta or open wye connected transformers. Simulation studies validate the predictions and claims with Simulink of MATLAB.

By introducing harmonic function analysis of MMC, this thesis also shows that on the dc side, the equivalent circuit of each phase consists of ideal voltage sources, which suggests that MMC has a future role as Ultra-HVDC for higher voltage dc transmission. Meanwhile, power balance equation inherent in MMC ensures its feasibility for parallel connection to form multi-terminal HVDC networks. Simulation results verify the viability of MMC for the application of Ultra-HVDC and multi-terminal HVDC. Moreover, a mathematical model suitable for load-flow analysis of multi-terminal HVDC networks in steady-state is developed and validated. Performance of MMC back-to-back HVDC under parallel computation condition is evaluated by RT-LAB.

Résumé

Le convertisseur modulaire à multiple niveau (MMC) dispose de nombreux avantages pour la transmission de courant continu haute tension (CCHT), en anglais High Voltage Direct Current (HVDC). Utilisant la modulation par porteuse triangulaire à changement de phase, le MMC a une perte faible de commutation et distorsion harmonique dans le spectre à haute fréquence. Alors que les distorsions de basse fréquence, en particulier les $2^{èmes}$ harmoniques, proliféré par une alimentation en courant alternatif monophasé, doivent être filtrées par les gros capaciteurs dans les sous-modules. Dans cette thèse, l'analyse harmonique fonctionnelle est appliquée afin de pointer la source de courant du $2^{ème}$ harmonique circulant dans le MMC. Après l'extension de l'analyse harmonique fonctionnelle, un procédé d'élimination commande anticipatrice est proposé en modifiant le signal de modulation. Un aperçu analytique permet l'actuel courant circulant du $2^{ème}$ harmonique à être éliminés à la source et, à leur tour, d'autres tensions harmoniques d'ordre faible qui se multiplient de la $2^{ème}$. Afin d'éviter les grands courants de défaut de surcharger le capaciteur du sous-module et d'assurer la viabilité de la méthode d'élimination commande anticipatrice, un contrôle deadbeat est incorporé dans la console MMC. Avec le deadbeat, le MMC devient un régulateur de courant de référence; les courants alternatifs dans le suivi des courants de références n'atteignent pas des grandes valeurs destructives durant les courants alternatifs défectifs. De même, les courants harmoniques inhérents des MMC du côté du courant alternatif ne peuvent pas circuler. Du coup, cela libère le MMC de la nécessité d'avoir des transformateurs delta ou en étoile ouvert reliés. Des études de simulation avec Simulink de MATLAB valident les prédictions.

En introduisant l'analyse harmonique fonctionnelle de MMC, cette thèse démontre également que sur le côté du courant direct, le circuit équivalent de chaque phase se compose de sources de tension idéales, ce qui suggère que le MMC a un rôle futur d'ultra-HVDC pour la transmission d'une tension plus élevée. Pendant ce temps, l'équation de

bilan de puissance inhérente du MMC assure sa faisabilité pour une connexion en parallèle afin de former des réseaux multi-terminaux de HVDC. Les résultats de simulation vérifient la viabilité de MMC pour l'application de l'ultra-HVDC et d'HVDC à multi-terminaux. En outre, un modèle mathématique adapté à l'analyse d'écoulement de puissance dans des réseaux HVDC multi-terminaux en état d'équilibre est élaboré et validé. La performance de MMC dos-à-dos d'HVDC sous condition est évaluée par RT-LAB.

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Table of Contents

List of Figures

List of Tables

List of Symbols

C	MMC sub-module capacitor
$Count$	Counter
f_c	Triangular carrier frequency
$f_{triangle}$	Triangular carrier
i_{ac}	MMC output ac current
i_{cir}	Circulating current
i_{com}	Common mode current
i_d, i_q	d-q components of 3-phase ac currents
i_{diff}	Differential mode current
i_u, i_l	Current of upper arm, lower arm
$i_{2\omega}$	2^{nd} harmonic circulating current
I_{ac}	Magnitude of ac output current
$\tilde{I}_{ac}$	AC current phasor
I_d	One phase dc current of MMC
I_{dc}	DC current of MMC
L_{ac}	AC system inductance
L_0	MMC arm inductor
m	Modulation index
m_{mod}	Modulating signal
m_u, m_l	Modulating signal of upper arm, lower arm
n_{arm}	Number of sub-modules connected with ‘on state’
n_u, n_l	Sub-module number with ‘on state’ in the upper arm,
N	Total number of sub-modules in one arm of MMC lower arm of MMC
P, Q, S	Active power, reactive power, complex power
q	Electric charge of a capacitor

R_{ac}	AC system resistance
R_r	Current limiting resistor for MMC start-up stage
R_0	MMC arm equivalent resistance
$T_{triangle}$	Period of the triangular carrier
$T_{A, B, \ldots J}$	Voltage terms from extended harmonic function analysis
$T_{1, 2, \ldots 8}$	Voltage terms from harmonic function analysis
u_a, u_b, u_c	MMC output ac voltage (3-phase)
u_{add}	Proposed 2nd harmonic circulating current elimination
u_d, u_q	d-q components of 3-phase ac voltages
u_{ref}	MMC reference voltage
u_{upper}, u_{lower}	Voltage of upper arm, lower arm
U_c	Sub-module capacitor voltage
U_{dc}	MMC dc voltage
$U_{dc\text{-}m}$	Measured dc voltage
U_{ref}	Magnitude of reference voltage
U_{SM}	Output voltage of sub-module
v_{aca}, v_{acb}, v_{acc}	AC system ac voltage (3-phase)
v_{PCC}	Voltage of the point of common coupling
$\tilde{V}$	MMC ac output voltage phasor
$\tilde{V}_{ac}$	AC system voltage phasor
X	Magnitude of 2nd harmonic circulating current
Y	Magnitude of u_{add}
ω	Angular velocity (in radians per second)
δ	Phase angle of reference voltage
γ	Phase angle of u_{add}
φ_{ac}	Phase angle of ac output current
φ_2	Phase angle of 2nd harmonic circulating current signal (added in the modulating signals)

List of Acronyms

AC, ac	Alternating Current
BTB	Back-to-back
CDSM	Clamp Double Sub-module
DC, dc	Direct Current
FACTS	Flexible AC Transmission Systems
FBSM	Full-Bridge Sub-module
FFT	Fast Fourier Transform
HBSM	Half-Bridge Sub-module
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
MMC	Modular Multilevel Converter
MVA	Mega Volt Ampere
PCC	Point of Common Coupling
P-I	Proportional-Integral
PSC-PWM	Phase-Shifted Carrier Pulse Width Modulation
p. u.	Per Unit
PWM	Pulse Width Modulation
SCR	Silicon Controlled Rectifier
SM	Sub-module
SPS	SimPowerSystem
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator

SVC	Static Var Compensator
THD	Total Harmonic Distortion
VAR, var	Volt-Ampere Reactive
VSC	Voltage-Source Converter

Chapter 1 Introduction

1.1 Background

George Westinghouse's ac transmission system won over Thomas Edison's dc transmission system because high voltage is required to overcome network impedance which increases with transmission distance. The ac transformer raises transmission voltage economically. When transmission distance reaches around 600 miles, the series inductive reactance of the transmission line lowers the transient stability limit and therefore dc transmission is reconsidered because there is zero inductive reactance in it. For underwater crossing by cables, the metal conductor is enclosed in dielectric tube which electrically is modeled as a shunt capacitor. The capacitive volt-ampere reactive (VAR) occupying the cable leaves little room for active power to get across. Again dc offers an advantage because shunt capacitive reactance is infinite.

But an economical converter is still required to raise the dc voltage high enough for long distance transmission. The technology of dc amplification was initially developed around vacuum tubes. The discovery that ionized gas in the vacuum enclosure increase conductivity led to the thyratron and later to mercury arc rectifiers. The first generation High Voltage Direct Current (HVDC) made use of mercury arc rectifiers [1, 2].

Vacuum tube technologies were supplanted by the invention of the transistor, based on the silicon based 3-layer PNP or NPN junctions. Putting PNP and NPN transistors together to form a 4-layer PNPN device, the Silicon Controlled Rectifier (SCR) came into existence. The SCR was conceived with the power application of the thyratron in mind. As the SCR has the same properties as the *thyratron*, its official name given to it now is *thyristor*.

The thyistor has 3 terminals: anode, cathode and gate. The bulk output current flows from the anode to the cathode, after it has been triggered ON by a low-level power signal at the gate terminal. Although a signal to the gate can turn it ON, a gate signal cannot turn it OFF. The thyristor is turned OFF only by applying a reversed voltage across the anode

and cathode. The family of converters using this turn OFF method is given the name line commutation converters (LCC).

Over the years, through continuing research, solid-state switches which can be turned ON and turned OFF at the gate such as insulated-gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT) have evolved and they have given birth to the 3rd generation of HVDC (1st generation—mercury arc rectifiers, 2nd generation—thyristor).

1.2 Literature Review

1.2.1 Line Commutated Converter HVDC (LCC-HVDC)

LCC-HVDC which is also known as classic HVDC [3, 4] began in 1954 in Gotland, Sweden. World-wide, HVDC transmission is still dominated by LCC-HVDC. It is applied to transmit bulk power across distances greater than 2000km in Canada, Brazil, USA, Russia, India, China, which span extensive geographical terrain. HVDC is applied to transmit electricity by overhead lines or underwater cables.

HVDC in back-to-back (BTB) arrangements (ac rectified to dc to be inverted back to ac again in the same location) are used as:

(i) phase-shifters which are used to connect two ac systems of the same frequency but at widely differing voltage angle (example---Quebec to New Brunswick link in Eel River Crossing);

(ii) frequency changers (example---islands in Japan which have 50 Hz and 60 Hz standard; uniting weak regional ac grids in India whose frequencies vary highly in the course of a single day).

Decades ago, extensive research had been conducted on multi-terminal HVDC [5-9]. An example is the Quebec-New England multi-terminal transmission system, which was put into service in 1992 with capacity of 2000 MW.

Recently, by raising the dc transmission voltage (Ultra High Voltage DC), distances around 2000km become possible and there are installations in China and India [3, 4].

Pioneering research on LCC appeared in Direct Current, a publication which is no longer available. A summary of the knowledge resides in E. W. Kimbark's, "Direct Current Transmission" [10].

1.2.2 Voltage Source Converter HVDC (VSC-HVDC)

Because of the high cost of HVDC stations, they were built only where the great distances and the size of power transmitted justify the cost. But the versatility of HVDC (noted above) has applications which have not been implemented because the cost cannot be justified.

The advent of IGBTs, IGCTs, etc. has given rise to VSC-HVDC, the 3rd generation. Because Voltage Source Converters have already a history of application in variable speed ac motor drives, many of the concepts which are now in [11] have been borrowed and adapted. One adaptation consists of designing the control so that the VSC HVDC station [12] operates like a synchronous generator, that is, reactive power is controlled by the voltage magnitude (field excitation control) and active power is controlled by the voltage phase angle (governor control). As to the control of the IGBT or IGCT switching, Sinusoidal Pulse-Width Modulation (SPWM) technique is applied so that the VSC behaves as a Switch Mode Linear Amplifier [13]. Sufficient frequency bandwidth is required in the linear amplifier to ensure fast response in the control.

From the adaptation, VSC-HVDC, which is inherently immune to commutation failure, has other attractive features: (i) decoupled P-Q control; (ii) protection against large ac short circuit current by deadbeat control; (iii) lower cost because of reduction in size of filters; (iv) parallel connection on the dc side to form multi-terminal VSC-HVDC [14-22]. The proprietary name, HVDC-LIGHT, given to it by multinational equipment manufacturer ABB, is an indicator of the market orientation—smaller size affordable HVDC links.

Presently, many of the sales are for applications as:

(i) Submarine power transmission;

(ii) Frequency changers to convert variable frequency power of wind-turbine to 50 or 60 Hz utility grid;

(iii) Flexible controllers for delivering power to different markets in energy trading.

1.2.3 Modular Multilevel Converter

IGBTs, IGCTs or other solid-state switches have individual voltage ratings of around 5kV. Although their voltage rating keeps increasing with progress, the dc voltage of HVDC

transmission is in the order of several hundreds of kV. In order to switch at such high voltages, hundreds of solid-state switches have to be connected to switch in unison. This requires the high dc voltages to be equally shared by each solid-state switch. Auxiliary R-C circuits to ensure equal voltage sharing by the solid-state switches, in steady-state and in transient, must be developed and successfully tested. In addition, when any solid-state switch in the series string fails, it must fail as a short-circuit. The R&D cost is beyond most budgets except those of a few industry giants.

Research in multilevel converters is one way of overcoming the road block for small budget players. The capacitor voltage across the solid-state switch in each multilevel converter layer is easier to equalize in one of the three multilevel topologies: (i) diode clamped neutral; (ii) flying capacitor; (iii) cascaded H-bridge. Of the many publication, the most influential is [23]. A typical application is for Static Var Compensators (SVCs) [24].

But as there are 4 times as many solid-state switches as VSC-HVDC, Cascaded H-bridges is not considered to be price-competitive.

In 2001, German Professor Marquardt halved the number solid-state switches by using sub-modules consisting of half-H-bridges in his invention, MMC [25]. A few years later, outline of the invention was disclosed in [26-31]. These seminal publications have opened a new field of research: on applications of MMC to STATCOMs [32], medium voltage applications [33-35] and HVDC [36-39]. Since MMC is relatively new, there is still more to be discovered. In the past decade, the advance can be classified under: 1) MMC modulation methods; 2) MMC capacitor voltage equalizing methods; 3) MMC model; 4) MMC low-order harmonic suppression technique.

The modulation methods are: Pulse Width Modulation (PWM) and Voltage Level Modulation. PWM is already widely used in multilevel converters. [40] introduced the PWM technique to MMC control. [41] proposed Voltage Level Modulation and successfully produced N+1 level of output voltage. In 2012, [42] and [43] brought improved PWM methods respectively which could raise the output voltage to 2N+1 level with N sub-modules in each arm, however, small dc voltage ripple will be introduced.

In practical application, usually dozens or even several hundreds of sub-modules are connected in series in each arm. When the MMC is in operation, the capacitor voltage of

each sub-module can be unbalanced in magnitude. When voltage imbalance grows, overvoltage occurs in some sub-modules and exceeds the safe voltage rating of the solid-state switch. Therefore, a capacitor voltage equalizing algorithm is required for MMC operation. An easy way to balance the capacitor voltage was proposed in [44], which has been greatly successful. A research group from the Royal Institute of Technology (KTH), Sweden has proposed an alternative method which they have shown to be successful in experimental tests carried out in their MMC prototype [45].

As to mathematical modeling of MMC, the definitive analytical model was introduced in [46]. There have been experimental and simulation validation of the model in [46-50]. Different from the analytical model of MMC of [46], several accelerated or averaged models have been proposed to speed up the computer simulation. [51] introduced an accelerated model of MMC which can drastically reduce the computer simulation time. J. Peralta and H. Saad proposed both averaged [52] and simplified [53] models suitable for MMC simulation involving large numbers of sub-modules.

The connection of the number of sub-modules to form an arm of one of the MMC phases is determined by the ON/OFF switching of the solid-state switches of any one sub-module. For low switching loss, its insertion into the string and its disconnection from the string should be the lowest possible rate. Insertion and disconnection respectively adds and subtracts the capacitor voltage to the voltage of the arm. The ultimate aim of the modulation signal is to form a sinusoidal waveform for the ac-side terminal from the steps of capacitor voltages. Because MMC has many sub-modules, the sinusoidal voltage waveform is constructed by timing the insertion/disconnection of sub-modules, one-at-a-time, to follow the desired waveform closely. The algorithm used is the Phase shifted carrier PWM (PSC-PWM). The attraction of MMC lies in: (i) low switching loss from the lowest rate of insertion and disconnection; (ii) excellent Total Harmonic Distortion (THD) factor because the sinusoidal waveform can be closely approximated by timing the insertion/disconnection.

Although high frequency harmonics are not present, MMC has inherent 2^{nd} harmonic circulating current and 3^{rd} harmonic current on the ac-side. Hitherto, the effects of the 2^{nd} and other low frequency harmonics are minimized by increasing the size of capacitors in the MMC sub-modules. The 3^{rd} harmonic is prevented from flowing by transformer

connection which does not have a ground.

Research in [54] has already been initiated to suppress the 2nd harmonic by *negative feedback*. Li Z. et al. [55] have successfully applied a digital-filter-based inner circulating current suppressing method to MMC. Nevertheless, both of the suppressing methods mentioned above do not identify the origin of the circulating current.

1.3 Thesis Statement

The author extends the harmonic function analysis, which has begun in [48]. With harmonic function analysis as the theoretical base, mathematical formulas have been derived. The mathematical formulas offer analytical insights, which enable the origin of 2nd harmonic circulating current to be pin-pointed and to show how the origin can be annulled by added voltage components in the modulation signal. This thesis presents a feed-forward method to reduce the 2nd harmonic component of single-phase ac power which is the root of the low-order harmonic proliferation in MMC.

As the equivalent circuits on both the ac side and the dc side are ideal voltage sources, the thesis shows that it is feasible to connect MMC stations on the dc sides (which are ideal voltage sources) in series to increase the voltage of the dc bus in point-to-point dc transmission. This feasibility is confirmed by simulations, demonstrating that MMC has a future in Ultra HVDC.

Presently, there is more interest on the feasibility of operating MMC by parallel connection on the dc sides as multi-terminal MMC HVDC. Having ideal voltage sources as equivalent circuits on the dc-sides raises doubts. After all, multi-terminal VSC HVDC is generally thought to be trouble-free because the equivalent circuit of a VSC is an ideal current source on the dc-side. The mathematical formulas reveal that the ideal voltage source V_{ac} on the ac side has a counter-part ideal voltage source U_{dc} on the dc side which satisfies power balance $V_{ac}I_{ac} \Leftrightarrow U_{dc}I_d$. For ac power $V_{ac}I_{ac}$, there is a current $I_d=V_{ac}I_{ac}/U_{dc}$ injected at the location of the dc side ideal voltage U_{dc} in the same way as current injected by a VSC station.

1.3.1 Research Objectives

The objectives of this thesis are:

(1) Develop and extend MMC harmonic function analysis.

(2) Develop a control method for MMC to reduce 2nd harmonic circulating current and other low-order harmonics proliferated from 2nd harmonic.

(3) Implement a control method that rescues low-order harmonic reduction methods from ac faults.

(4) Investigate the feasibility of MMC for series connection to form Ultra HVDC.

(5) Investigate the feasibility of MMC for parallel connection for multi-terminal HVDC applications.

(6) Evaluate a commercial software package that applies parallel computing to simulate MMC in real-time.

1.3.2 Research Methodology

A. Mathematical Analysis

The author follows harmonic function analysis to develop formulas and equivalent circuits of MMC on both the ac and the dc sides, which is the mathematical basis for the MMC applications for Ultra HVDC and multi-terminal HVDC. A mathematical model of MMC is also obtained. With mathematical formulas, the origin of 2nd harmonic circulating current has been pin-pointed. Analytical insights from extended harmonic function analysis enable a feed-forward or feedback method that reduces the 2nd harmonics and other low-order harmonics proliferated from it at the source.

B. Simulation

This author uses Simulink/MATLAB as the simulation tool to verify the proposed methods. Simulink/MATLAB uses an accurate general purpose state-space solver. Each MMC station and power grid applied in this thesis is simulated in detailed models of IGBT, diode, inductor, capacitor, resistor, transformer and voltage source selected from the SimPowerSystem library. Harmonic components of the simulation results are evaluated by fast Fourier transform (FFT) analysis embedded in Simulink/MATLAB. The same results would have been obtained by other traditional simulation software, such as PSCAD which uses unified accurate solvers.

A commercial program based on parallel processor to simulate MMC in real time is evaluated in Chapter 7. This research is pursued for future research in Ultra-MMC HVDC and multi-terminal MMC HVDC. The many MMCs involved in the systems will require powerful simulators to simulate the large number of sub-modules.

1.3.3 Contributions

As far as the author knows, the original contributions of this thesis are:

- Harmonic function analysis of MMC has been developed and extended. Mathematical formulas from harmonic function analysis show that the equivalent circuit of MMC consists of ideal voltage sources connected in series in both the ac side and the dc side.
- From extended harmonic function analysis, a novel feed-forward method of eliminating the 2^{nd} harmonic circulating current at the source by modifying the modulation signal is developed. In addition, a novel mathematical model of 2^{nd} harmonic circulating current which provides an important guideline for sub-module capacitor and arm inductor value selection is derived.
- Joint control of deadbeat and low-order harmonic reduction method is implemented, which prevents MMC from destructive currents under ac fault conditions. Moreover, combining a feed-forward 2^{nd} harmonic circulating current reduction method with a feedback one enhances the reliability.
- The model of MMC as ideal voltage sources indicates that MMC is suitable for series connection to form Ultra HVDC. Key formulas from harmonic function analysis show that MMC is also suitable for parallel connection for multi-terminal HVDC applications.
- An accurate mathematical model (taking capacitive reactance voltage into account) for power-flow analysis of MMC multi-terminal HVDC in steady-state is developed.

1.4 Outline of the Thesis

The research in this thesis is conducted by mathematical analysis and simulation. The outline of the chapters in this thesis is shown as:

Chapter 2: Modular Multilevel Converter

A brief introduction of 3-phase MMC configuration as well as its operation principle is given. Modulation techniques popularly used in MMC are discussed concisely. Through basic circuit theory, equivalent circuits of MMC on both the ac side and the dc side are derived.

Chapter 3: MMC Harmonic Function Analysis

This chapter begins with fundamental circuit theory to introduce harmonic function analysis in the perspective of capacitor modulation. It is shown that the equivalent circuits, on both the ac side and the dc side, comprise ideal voltage sources. Mathematical formulas derived from harmonic function analysis unveil the properties of MMC, which until now are unchartered. By classifying mathematical formulas in terms of frequencies, the ac-side consists of fundamental frequency and odd order harmonics components whereas the dc-side consists of dc and even order harmonic components. Finally, for dynamic analysis, a model based on nonlinear ordinary differential equations has been derived and verified by Simulink/MATLAB.

Chapter 4: Low-Order Harmonic Reduction of MMC

Following the harmonic function analysis, the origin of 2^{nd} harmonic circulating current is pin-pointed. It is a 2^{nd} harmonic voltage source inherent in MMC. This chapter proposes a novel feed-forward method to produce a counter MMC voltage which cancels the inherent 2^{nd} harmonic voltage source so that there is no resultant driving voltage to cause the flow of circulating current. The counter MMC voltage can only be produced by the modulation signal.

This chapter pursues further harmonic function analysis to show that the counter MMC voltage can be produced by addition of a 2^{nd} harmonic modulating signal. Simulations show that the feed-forward method does eliminate of 2^{nd} harmonic circulating current and other low-order harmonics proliferated by it. This means that the size of sub-module capacitors can be reduced, thus saving equipment space and cost.

Chapter 5: Incorporate Deadbeat and Low-Order Harmonic Reduction in MMC

This chapter shows that MMC has one channel to implement deadbeat control and another

one to implement low-order harmonic reduction control. The two independent channels are discovered based on harmonic function analysis in Chapter 3 and 4.

The knowledge that a 2nd harmonic modulating signal commands a counter MMC voltage sheds understanding of the "mechanism" of feedback methods used in the pioneering publications [54]. Noting that the filtering methods of feedback in [54] are complicated, this chapter proposes an original simpler feedback filter based on the complement of the Fliege Notch Filter.

The research then shows that the feed-forward method and the Complement-Fliege Filter feedback method can operate simultaneously together. The objective is to ensure redundancy. If one method is incapacitated, the other is still in place.

Low-order harmonic reduction control enables the hitherto oversized capacitors of the sub-modules to be reduced. However, during ac short circuit faults for example, the large fault currents may cause the capacitor voltages to be overcharged to damage IGBTs.

The research turns to implementing ac current reference control by MMC to rescue the low-order harmonic reduction methods from ac faults. When the ac current is regulated to track the reference, the ac current should not have enormously large values during faults. This chapter adopts individual phase deadbeat as ac reference current control. By tracking the reference current, deadbeat is also capable of reducing 3rd and odd harmonics generated by MMC on the ac side.

Simulation results show that joint implementation of feed-forward and feedback low-order harmonic reduction methods in MMC can be protected by deadbeat.

Chapter 6: MMC Ultra HVDC and Multi-Terminal HVDC

This chapter shows that quantitative modeling of ac and dc systems interconnected by MMC is accurate enough only when the capacitive reactance voltages (predicted by the mathematical formulas) are taken into account.

Since the dc side of MMC are modeled as ideal voltages, this chapter verifies that MMC is suitable for series connection to form Ultra HVDC by simulation.

This chapter also shows that MMC is also suitable for parallel connection on their dc sides as Multi-terminal MMC HVDC. Although the equivalent circuits are ideal voltage sources, a dc current is injected into the dc-side as a consequence of the ac-to-dc power

balance equations derived from harmonic function analysis.

For completeness, this chapter presents simulations of the sequences of MMC start-up from “cold” when the capacitors are uncharged. Initially, the modulation controls are not activated. The capacitors are charged through external resistance banks to limit the size of inrush currents which would otherwise destroy the anti-parallel diodes.

Chapter 7: Performance of MMC BTB HVDC under Parallel Computing Condition

This chapter briefly evaluates the performance of MMC back-to-back HVDC under parallel computing condition. By comparing simulation results from detailed Simulink/MATLAB model of MMC, it shows that the parallel computing model of MMC developed by Opal-RT Technologies is accurate enough and, in addition, capable of running simulation in real time, which can save the simulation time considerably.

Chapter 8: Conclusions

This chapter summarizes the thesis and provides suggestions for future research direction.

Chapter 2 Modular Multilevel Converter

2.1 Introduction

With recent advancement of controllable power electronic technology, High Voltage Direct Current (HVDC) transmission has taken considerable strides forward, especially for the voltage source converter (VSC) based HVDC (VSC-HVDC). Insulated-gate bipolar transistors (IGBTs) are widely used in the VSC topology transmission systems [39, 56, 57]. Modular Multilevel Converter (MMC), as a new invention [25] for high-voltage applications, has drawn the attention of many researchers owing to its merits, such as: low output harmonics in the high frequency spectrum, low switching loss, easy scalability, no requirement of filters.

This chapter introduces the configuration of 3-phase MMC. Each phase of the MMC consists of half-bridge sub-module connected in series. Therefore, the operating states of the half-bridge sub-module are examined in detail. After describing the operation principle of MMC, its modulation methods are briefly discussed. The equivalent circuits of MMC on both the ac and the dc sides are derived according to basic circuit theory.

2.2 Configuration of 3-phase MMC

Fig. 2-1 (a) illustrates the schematic diagram of 3-phase MMC. Each phase is composed of two arms, the upper arm and the lower one. Inductor L_0 and its equivalent resistance R_0 are connected in series with each arm. Besides assisting in power control, the arm inductor L_0 suppresses the circulating current as well as limiting the short circuit fault current on either ac or dc side. Normally N identical sub-modules (SM) are connected in series in each arm. Several types of SM could be applied for MMC. They are half-bridge SM (HBSM), full-bridge SM (FBSM) and clamp double SM (CDSM) as shown in Fig. 2-1 (b), (c) and (d) respectively.

In this thesis, only HBSM is studied. And thus ‘HBSM’ would be referred to as ‘SM’ hereafter.

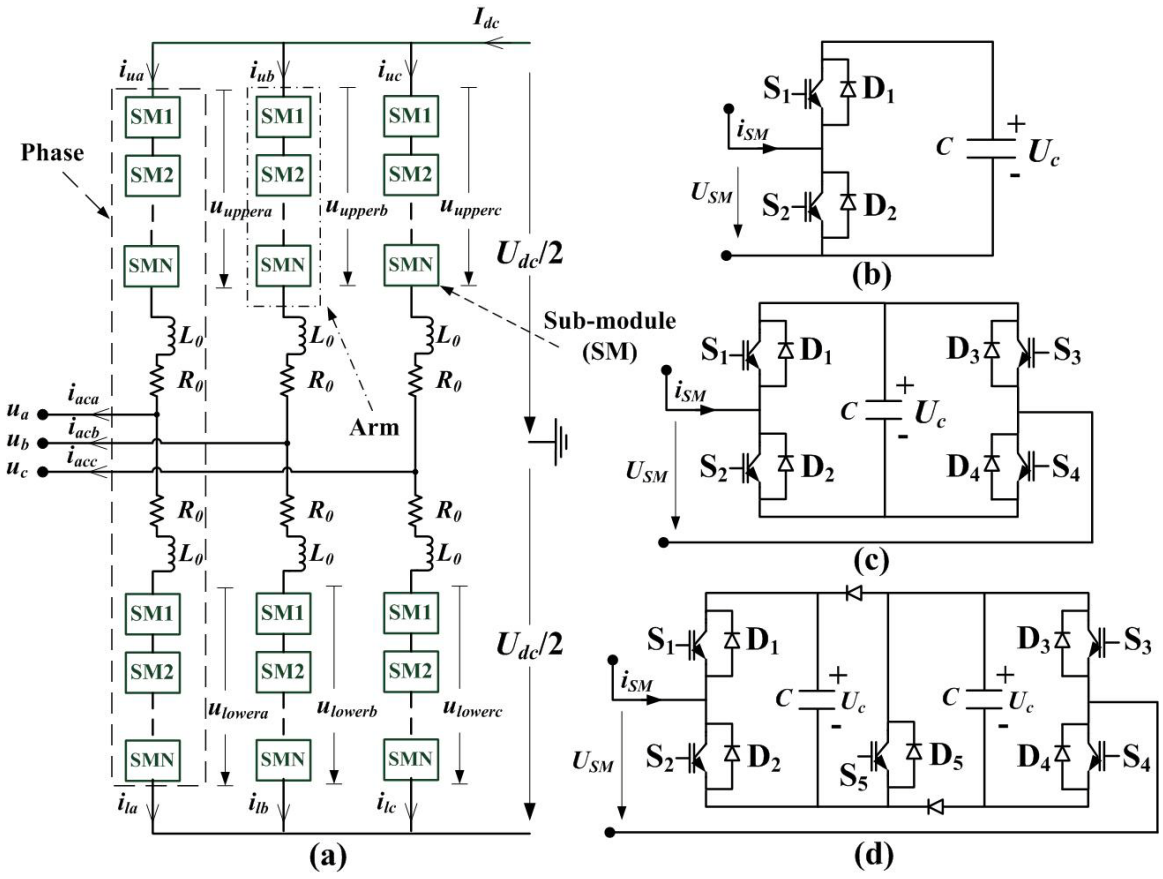


Fig. 2-1 (a) Configuration of 3-phase MMC; (b) half-bridge SM; (c) full-bridge SM; (d) clamp double SM

Fig. 2-1 (b) displays the SM internal structure. It is favoured because it has the least IGBTs and diodes and therefore more economical. IGBTs serve as two switches S_1 and S_2. D_1 and D_2 are two anti-parallel diodes. C is a dc capacitor with corresponding voltage of U_c. The output voltage of the SM is defined as U_{SM}. By switching S_1 and S_2 in different patterns, the SM would be in different states.

Fig. 2-2 shows three SM operation states based on current direction. We define the current i_{SM} to be positive when it flows from '+' to '-' and negative when it flows in the reverse direction. In state 1 (Fig. 2-2 (a)), S_1 and S_2 are both applied with switch-off signals and two operation modes exist corresponding to the current directions. When i_{SM} is positive, D_1 will be conducting and the capacitor C will be charged by i_{SM}. When i_{SM} is negative, it goes through D_2 and bypasses C. This operation state can only be applied for MMC start-up period to charge SM capacitor. Under MMC normal operation condition, state 1 is undesirable and is named as 'abnormal state'.

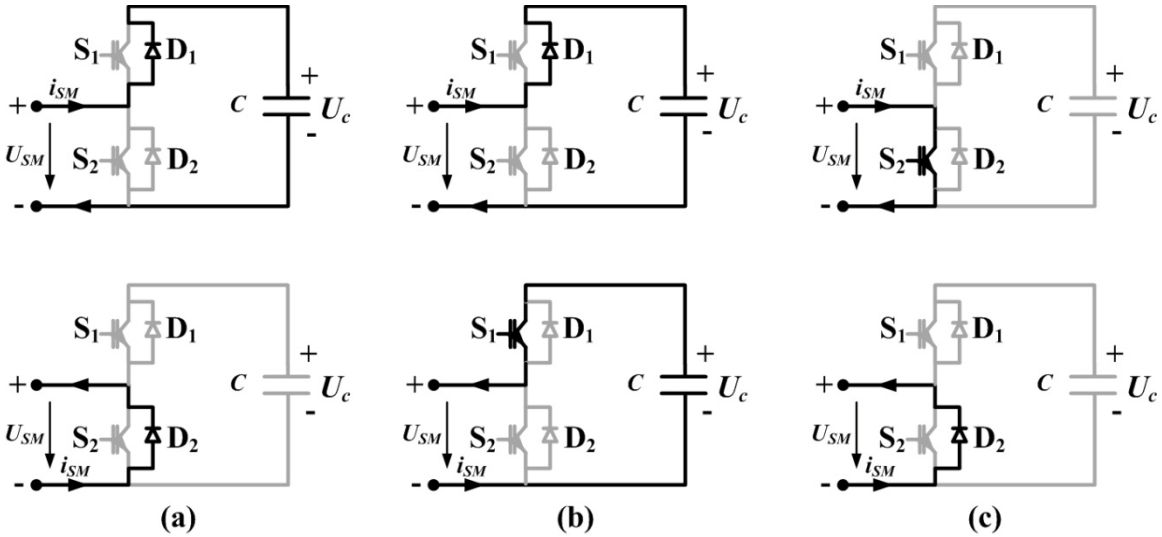


Fig. 2-2 Sub-module operation states: (a) state 1: gate signal of S_1 is OFF, gate signal of S_2 is OFF; (b) state 2: gate signal of S_1 is ON, gate signal of S_2 is OFF; (c) state 3: gate signal of S_1 is OFF, gate signal of S_2 is ON

When S_1 is with a turn-on signal and S_2 is given a turn-off signal, SM operation state 2, shown in Fig. 2-2 (b), is reached. S_2 stays in the off-state because of its 'off' gating signal and D_2 cannot conduct due to reverse voltage. According to the current direction, there are two operation modes in state 2 as well. When i_{SM} is positive, D_1 conducts. The voltage across conducting D_1 is reverse biasing S_1 so that S_1 cannot turn on. Therefore, C will be charged by i_{SM} through D_1. When i_{SM} is negative, S_1 turns on to discharge C. In state 2, the SM, with its corresponding voltage of U_c, is inserted into an arm of MMC. We call state 2 the 'insert state' or 'on state'.

SM operation state 3 (Fig. 2-2 (c)) represents the state when S_1 is given a turn-off signal and S_2 is given a turn-on signal. D_1 cannot conduct due to reverse voltage and S_1 stays in the off-state because of its 'off' signal. Still, there are two operation modes in this state. Positive current i_{SM} goes through switch S_2 to bypass C and negative i_{SM} flows through D_2 to bypass C. Both of the modes show that in state 3, the SM is bypassed with zero output voltage across it. Thus, this SM operation state is called state 3, the 'bypass state' or 'off state'.

According to the description discussed above, insert/on state and bypass/off state are the two required states for normal operation of MMC. The discussion is summarized in Table 2-I. In this table, '1' represents turn-on gate signal and '0' refers to turn-off gate

Table 2-I Sub-module operation states

State	Gate Signal of S_1	Gate Signal of S_2	S_1	S_2	D_1	D_2	Current	Capacitor *C* State	U_{SM}
abnormal	0	0	off	off	ON	off	Positive	Charge	U_c
			off	off	off	ON	Negative	Bypass	0
insert/on	1	0	off	off	ON	off	Positive	Charge	U_c
			ON	off	off	off	Negative	Discharge	U_c
bypass/off	0	1	off	ON	off	off	Positive	Bypass	0
			off	off	off	ON	Negative	Bypass	0

signal. Table 2-I shows that when gate signal of S_1 is 1 and gate signal of S_2 is 0, the SM is inserted in the system. When gate signal of S_1 is 0 and S_2 is 1, the SM is bypassed. Thus, by controlling the gate signals to the two switches, each SM is inserted in or bypassed from any arm of Fig. 2-1(a) to generate to the voltage across the arm.

2.3 Operation Principle of MMC

2.3.1 Basic Operation Principle

Whereas conventional VSCs operate by "chopping" a dc voltage into voltage pulses of constant magnitude but variable widths to represent amplitude varying waveform requested by the modulation signal, MMC creates its output voltage by connecting different numbers of 'on state' SMs in series.

To illustrate the "insertion of 'on states' " and "bypass" concepts, Fig. 2-3 reproduces Fig. 2-1 using four SMs to represent the upper arm and the lower arm of each phase. In Fig. 2-3 U_{dc} represents the total dc voltage and U_c denotes the balanced capacitor voltage per SM. The output voltages of the j^{th} phase is u_j (j=a, b, c) with the arm voltages created by SM strings are written as u_{upperj} (j=a, b, c) for the upper arm and u_{lowerj} (j=a, b, c) for the lower arm. Fig. 2-4 depicts the voltage u_{uppera} of the upper arm, u_{lowera} of the lower arm and the phase voltage output u_a corresponding to the four SM of in the arms of phase-a of the MMC of Fig. 2-3. In the full cycle of the "sine" wave voltage output u_a, the operation period is divided into eight sections (from I to VIII in Fig. 2-4). Each section corresponds to the operation pattern of one arm formed by a string of SMs.

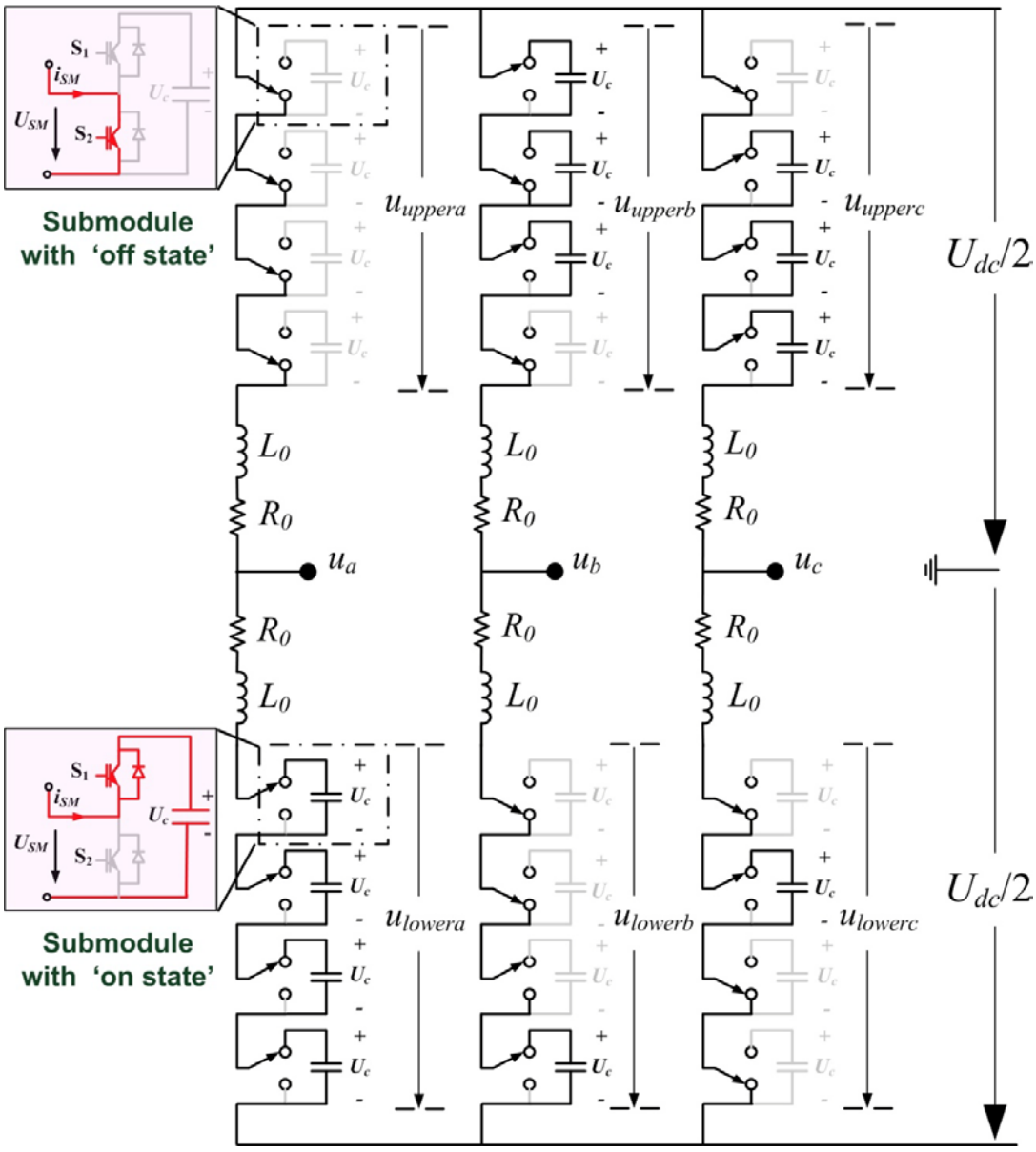


Fig. 2-3 Illustration of MMC operation, each arm having four SMs. MMC operation is based on SM IGBTs bypassing the capacitors or connecting the apacitors in series to form a string

For instance, section I of Fig. 2-4 refers to the pattern that all SMs in the upper arm being in the 'off state' and all SMs in the lower arm being in the 'on state' (displayed in Fig. 2-3 of phase-a). In this case, voltages generated in the upper arm and lower arm are zero and U_{dc} respectively. According to the circuit theory, at this time section, the output voltage of phase-a, which is measured at the mid-point between the upper and lower arm is $U_{dc}/2$. Detailed information about the arm SM string operation pattern in the eight sections is listed in Table 2-II.

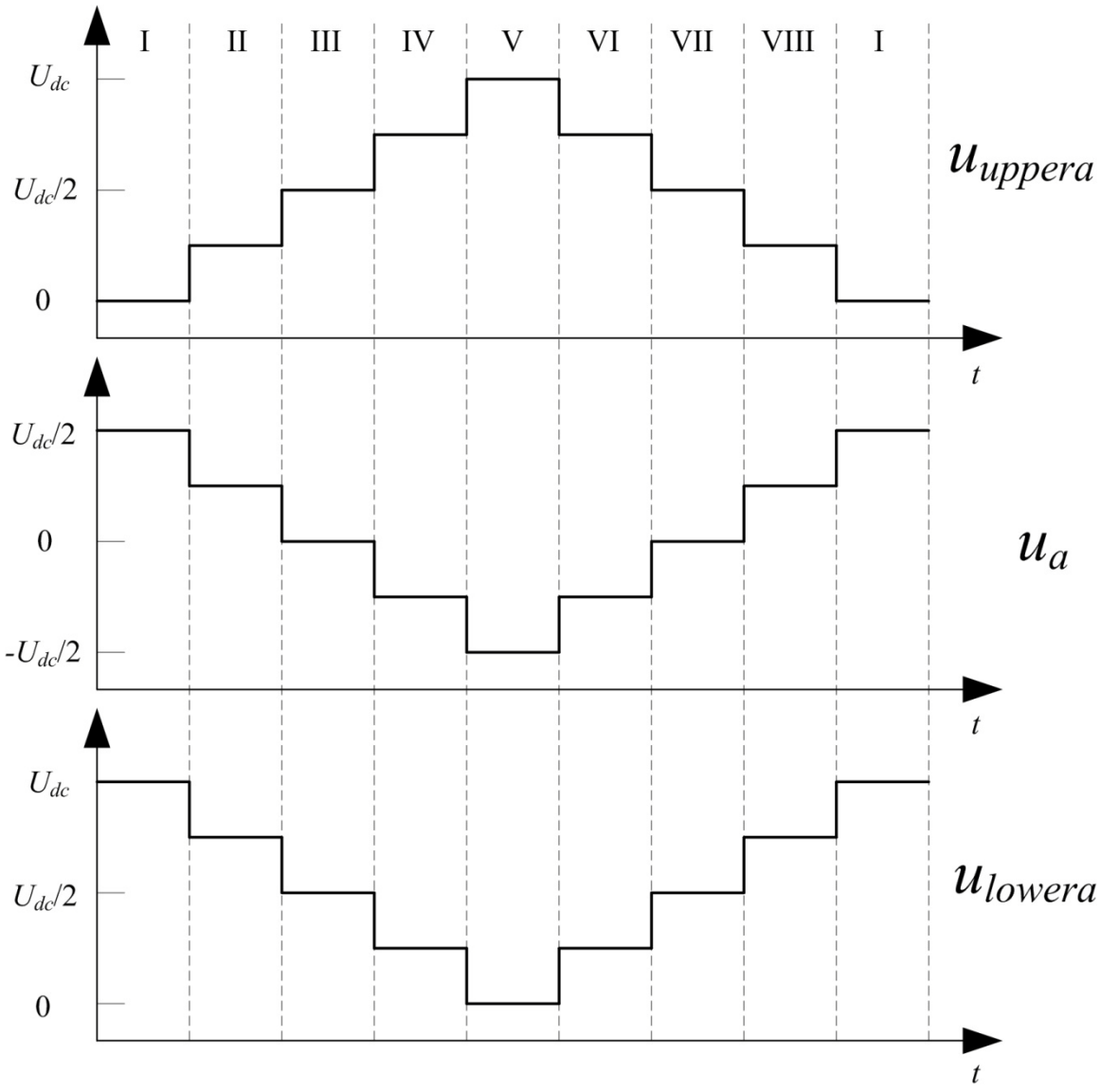


Fig. 2-4 Illustration of a four SM MMC voltage waveforms of phase-a

Clearly shown in Fig. 2-4 and Table 2-II, a four SM MMC produces five-level output voltage. An MMC with *N* SMs in each arm in general generates *N*+1-level output voltage. The relationship between dc voltage and SM capacitor voltage is:

$$U_c = \frac{U_{dc}}{N} \tag{2-1}$$

The bigger *N* becomes, a better output waveform MMC is produced. In order to make the dc voltage to be constant, at any time of the operation, the total number of SMs in

Table 2-II Phase-a voltage ua produced by Sub-Modules in Upper and Lower Arms

	Section							
	I	II	III	IV	V	VI	VII	VIII
Number of SM with 'on state' in the upper arm	0	1	2	3	4	3	2	1
Number of SM with 'on state' in the lower arm	4	3	2	1	0	1	2	3
Total number of SM with on state in one phase	4	4	4	4	4	4	4	4
Output voltage u_a	$U_{dc}/2$	$U_{dc}/4$	0	$-U_{dc}/4$	$-U_{dc}/2$	$-U_{dc}/4$	0	$U_{dc}/4$
DC voltage	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}

operation in one phase has to be equal to N which is the number of SMs in each arm. It follows that (2-2):

$$n_u + n_l = N \tag{2-2}$$

In equation (2-2), n_u represents the number of SMs with 'on state' in the upper arm. Similarly, n_l denotes the SM number with 'on state' in the lower arm of the same phase. From (2-2), it is noted that SMs in the upper and lower arm of the same phase are switched as a *complementary pair*, such could be used for modulation method which is about to be explained in the following section.

2.3.2 Modulation Methods

Modulation method is used to determine the number of SMs working at 'on state' in either arm of one phase. Up to now, two types of modulation method are commonly used in MMC:

1) Staircase Modulation[58]

2) Pulse Width Modulation (PWM)

The operation principle of Staircase Modulation is shown in Fig. 2-5. It uses stair waveforms created by each SM to fit the output reference as closely as possible. When N is big enough, Staircase Modulation could produce satisfying output waveform.

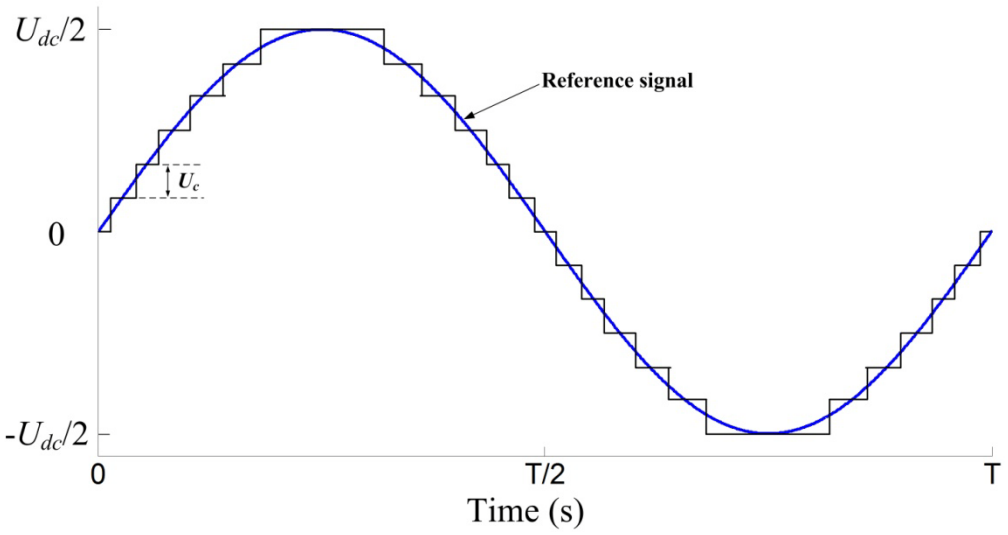


Fig. 2-5 Operation principle of Staircase modulation

Unlike Staircase Modulation, PWM technique works well regardless of the SM number.

Up to now, several PWM methods are available for MMC such as sinusoidal PWM (SPWM) [39], calculated PWM [59], phase shifted carrier PWM (PSC-PWM) [54, 60].

Since PSC-PWM is the modulation method adopted throughout the thesis, the method is elaborated here.

A. Sinusoidal Pulse Width Modulation (SPWM)

The connection of a SM to form a capacitor string is based on comparing modulating signal $m_{mod}(t)$ with a triangular carrier $f_{triangle}(t)$. Their operating limits are $0 < m_{mod}(t) < m_{mod\text{-}MAX}$ and $0 < f_{triangle}(t) < f_{triangle\text{-}MAX}$. When $m_{mod}(t) > f_{triangle}(t)$, the IGBT switchings insert (connect a SM into the string). A number 1 is entered to a counter $Count_j$=1. When $m_{mod}(t) < f_{triangle}(t)$, the setting of the counter is $Count_j$=0.

B. Phase Shifted Carrier PWM (PSC-PWM)

When there are N SMs in an arm, SPWM is refined by considering N sets modulation computations. The modulation signal $m_{mod}(t)$ is identical to each set (j=1,2..N) of computations. However, the triangular carrier of the jth set is delayed as

$$f_{triangle\text{-}j}(t) = f_{triangle}(t - \frac{(j-1)T_{triangle}}{N}) \quad j = 1, 2, \ldots N \tag{2-3}$$

where $T_{triangle}$ is the period of the triangular carrier. Based on $m_{mod}(t) > f_{triangle\text{-}j}(t)$, the number 1 is entered to the counter of the jth computation as: $Count_j$=1, otherwise $Count_j$=0. The jth level has a counter $Count_j$. When all the N sets of modulation computations have been executed, the number of SMs which are connected to the arm is:

$$n_{arm} = \sum_{j=1}^{N} Count_j \tag{2-4}$$

The total number of SMs with 'on state' in one arm could be obtained by comparing the corresponding arm reference signal with N phase shifted carriers. At the same time, according to complementary switching principle in (2-2), the total number of SMs with 'on state' in the other arm of the same phase could be derived.

C. Sorting Algorithm for Capacitor Balancing

Up to this point, the number of capacitors to be connected to an arm has been determined by n_{arm} of (2-4). A Sorting Algorithm has to be followed in connecting specific capacitors in series so that n_{arm} capacitors are connected in series. Otherwise, the capacitor voltage in each SM will be unbalanced and may diverge in long term operation. At the beginning of every PWM period, the capacitor voltage of each SM is measured and sorted in the following order based on the arm current direction [44]:

1) When the arm current is positive (charge the capacitor), put required number of SMs, n_{arm}, with lowest voltages on 'on state'

2) When the arm current is negative (discharge the capacitor), put required number of SMs, n_{arm}, with highest voltages on 'on state'

D. Summary of Modulation (PSC-PWM) Process

The flow chart of Fig. 2-6 summarizes processes already described on the computation of phase-shifted triangle carrier PWM, the sorting algorithm and implementation as gating signals.

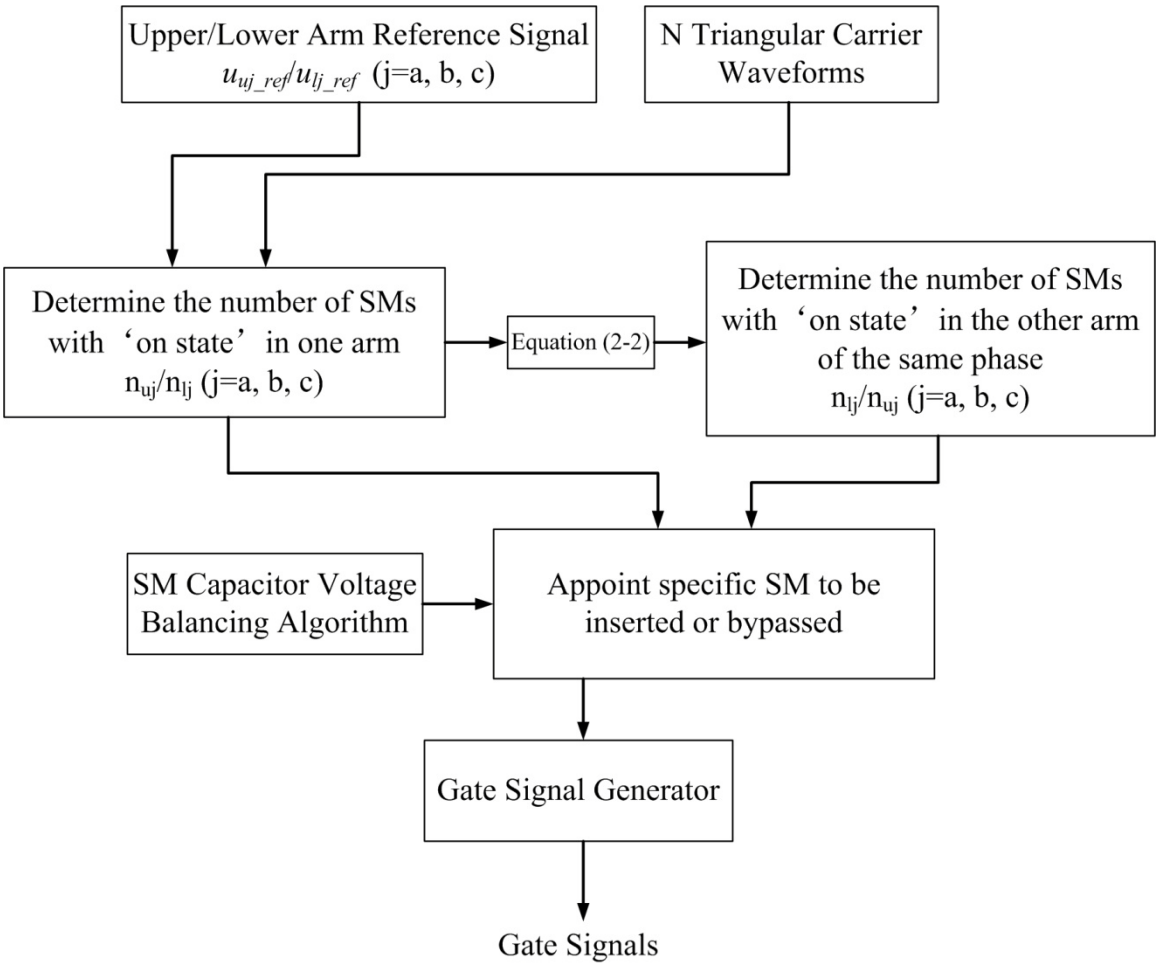


Fig. 2-6 Flow chart of implementation of modulation

Fig. 2-7 shows operation principle of PSC-PWM for MMC of phase-a. u_{ua_ref} is the upper arm modulation reference signal of phase-a and its corresponding number of SMs with 'on state' is denoted as n_{ua}. Here, carrier frequency f_c=250 Hz, which is five times that of the modulation signal. SM number in each arm is twelve (N=12). Fig. 2-8 displays the Fast Fourier Transform (FFT) of u_a in Fig. 2-7 (c). It is noted that the harmonics are mostly spread around Nf_c=12×250=3000Hz, and thus they could be easily filtered out by system impedance. Moreover, these harmonics can be moved to higher spectrum by increasing N or f_c, which makes the removal work even easier. In practical application, N is usually considerable. Taking the Trans Bay Cable project [61] (the world first HVDC system using MMC) for example, it applies 200 SMs in each arm. Hence, harmonics caused by PSC-PWM switching is no longer a concern of MMC in practical application.

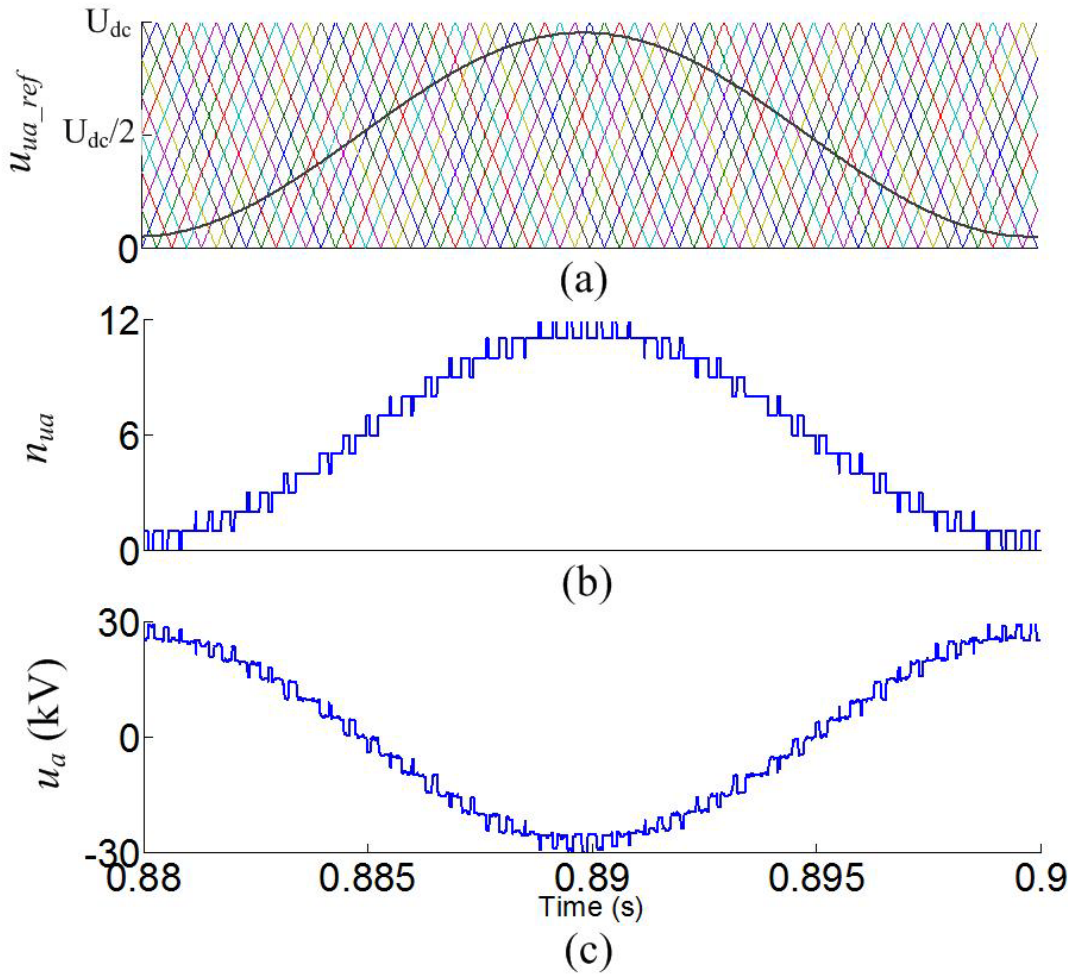


Fig. 2-7 Illustration of PSC-PWM for MMC of phase-a: (a) modulation signal (sinusoid) against phase shifted carriers (triangles); (b) number of SMs with 'on state' in the upper arm; (c) output voltage

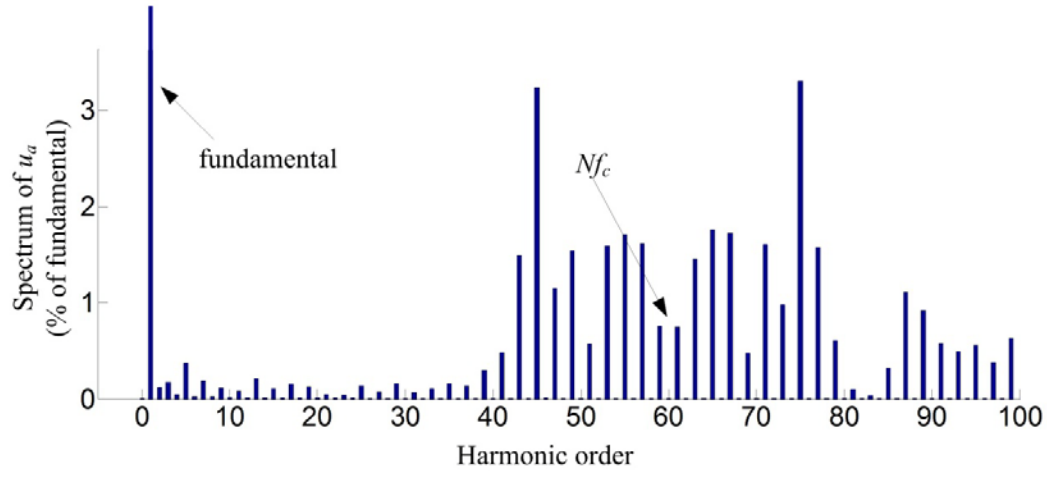


Fig. 2-8 FFT of u_a in Fig. 2-7 (c)

2.4 MMC Equivalent Circuit

In Fig. 2-1 (a), arm currents are denoted as i_{uj} and i_{lj} (j=a, b, c) where subscripts '*u*' and '*l*' represent upper arm and lower arm respectively and arm voltages generated by string of SMs are represented with u_{upperj} and u_{lowerj} (j=a, b, c). u_j (j=a, b, c) is the output voltage and i_{acj} (j=a, b, c) is the output current of each phase. The voltage across dc bus is U_{dc}. According to Kirchhoff's voltage law (KVL), the upper arm voltages are:

$$\frac{U_{dc}}{2} - u_j - L_0 \frac{di_{uj}}{dt} - R_0 i_{uj} = u_{upperj} \qquad (j = a, b, c) \tag{2-5}$$

Similarly, the lower arm voltages can be derived as:

$$\frac{U_{dc}}{2} + u_j - L_0 \frac{di_{lj}}{dt} - R_0 i_{lj} = u_{lowerj} \qquad (j = a, b, c) \tag{2-6}$$

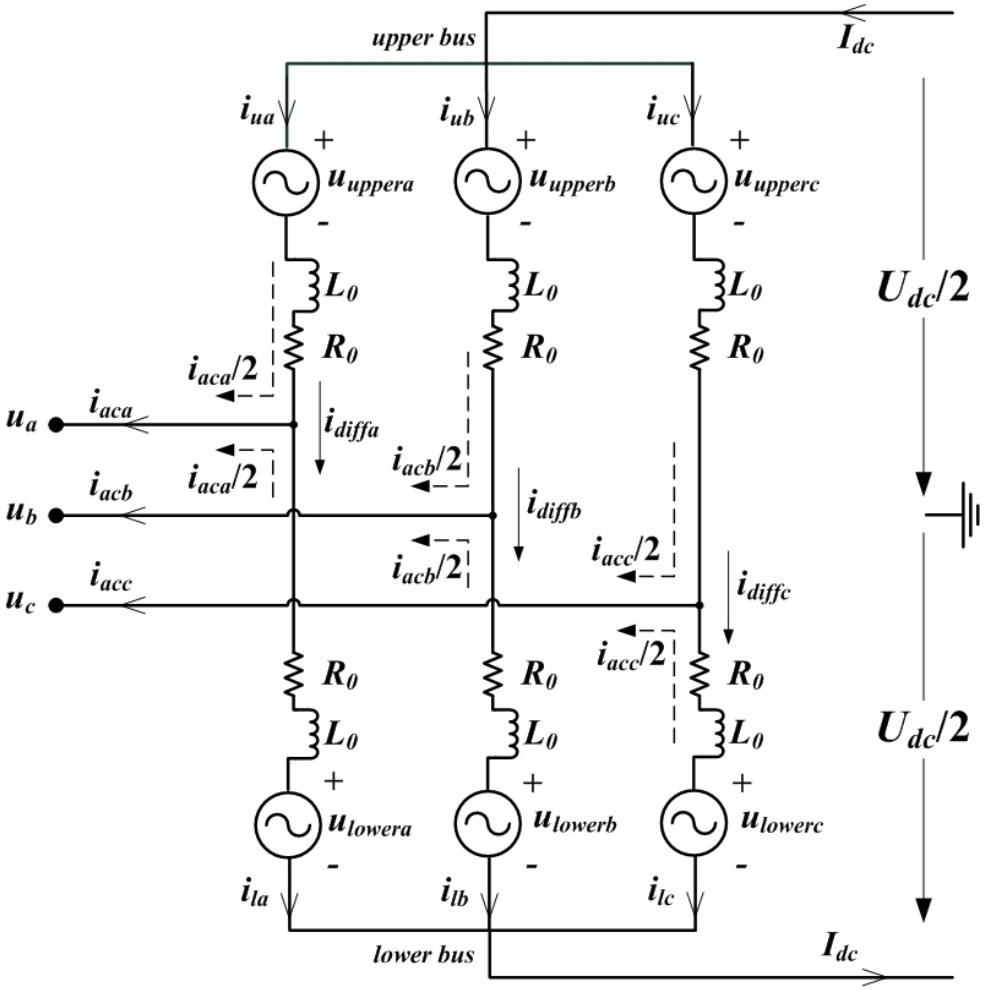


Fig. 2-9 Simplified circuit of 3-phase MMC

Common Mode and Differential Mode Decomposition

It is assumed that

$$i_{uj} = i_{diffj} + i_{comj} \qquad (j = a, b, c) \tag{2-7}$$

and

$$i_{lj} = i_{diffj} - i_{comj} \qquad (j = a, b, c) \tag{2-8}$$

i_{diffj} and i_{comj} represent differential mode current and common mode current respectively.

From Kirchhoff's Current Law at the node of the upper bus

$$\sum_{j=a,b,c} i_{uj} = \sum_{j=a,b,c} i_{diffj} + \sum_{j=a,b,c} i_{comj} = i_{dcu} \tag{2-9}$$

From Kirchhoff's Current Law at the node of the lower bus

$$\sum_{j=a,b,c} i_{uj} = \sum_{j=a,b,c} i_{diffj} - \sum_{j=a,b,c} i_{comj} = i_{dcl} \tag{2-10}$$

where i_{dcu} and i_{dcl} are the instantaneous currents of the upper and lower dc buses.

At the node between the upper and the lower arms, the ac currents are:

$$i_{acj} = i_{uj} - i_{lj} \qquad (j = a, b, c) \tag{2-11}$$

It follows that

$$i_{comj} = \frac{i_{acj}}{2} \qquad (j = a, b, c) \tag{2-12}$$

In balanced 3-phase operation,

$$\sum_{j=a,b,c} i_{acj} = 0 \tag{2-13}$$

Therefore

$$\sum_{j=a,b,c} i_{comj} = 0 \tag{2-14}$$

Substituting (2-14) in (2-9) and (2-10)

$$\sum_{j=a,b,c} i_{diffj} = i_{dcu} = i_{dcl} \tag{2-15}$$

In general, for balanced 3-phase operation the fundamental waveforms of the 3-phases are apart by t, t-T/3 and t-2T/3 where T is the period of the line frequency. Therefore, if the harmonic decomposition is

$$i_{diffa} = I_{diff\,0} + \sum_{M=1}^{\infty} C_M \cos\left[M(\omega t + \alpha_M)\right] \tag{2-16}$$

Here, I_{diff0} denotes the dc component of differential mode current; M represents the harmonic order; ω is fundamental frequency angular velocity (radian per second) and α is the corresponding angular displacement. Then for the b-phase

$$i_{diffb} = I_{diff\,0} + \sum_{M=1}^{\infty} C_M \cos\left[M(\omega t + \alpha_M - \frac{2\pi}{3})\right] \tag{2-17}$$

and for the c-phase

$$i_{diffc} = I_{diff\,0} + \sum_{M=1}^{\infty} C_M \cos\left[M(\omega t + \alpha_M - \frac{4\pi}{3})\right] \tag{2-18}$$

Referring to (2-15),

$$\sum_{j=a,b,c} i_{diffj} = 3I_{diff\,0} + \sum_{M=1}^{\infty} C_M \left\{ \begin{array}{l} \cos\left[M(\omega t + \alpha_M)\right] + \cos\left[M(\omega t + \alpha_M - \frac{2\pi}{3})\right] \\ + \cos\left[M(\omega t + \alpha_M - \frac{4\pi}{3})\right] \end{array} \right\} \tag{2-19}$$

$$= i_{dcu} = i_{dcl}$$

When m is not a multiple of 3,

$$\cos\left[M(\omega t + \alpha_M)\right] + \cos\left[M(\omega t + \alpha_M - \frac{2\pi}{3})\right] + \cos\left[M(\omega t + \alpha_M - \frac{4\pi}{3})\right] = 0 \tag{2-20}$$

Existing operational practice in MMC is to exclude triplen harmonics by connecting the ac-side in delta or open (ungrounded) wye.

During steady-state operation

$$i_{dcu} = i_{dcl} = I_{dc} \tag{2-21}$$

From (2-19)

$$I_{diff\,0} = \frac{I_{dc}}{3} \tag{2-22}$$

When the triplen harmonics are excluded, $i_{cirj}=i_{diffj}-I_{diff0}$ where i_{cirj} (j=a, b, c) is the circulating current of phase-j. i_{cirj} is given the name circulating current because $\sum_{j=a,b,c}(i_{diffj}-I_{diff0})=0$.

The upper and lower arm currents can be described as:

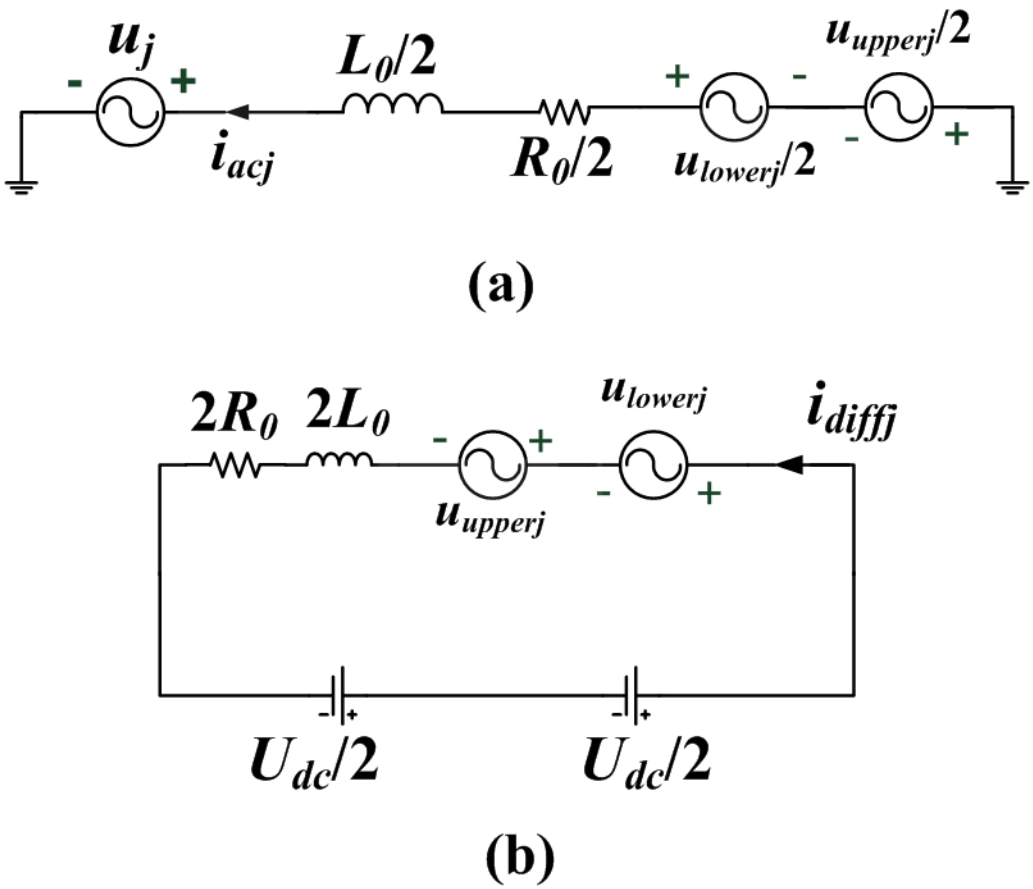


Fig. 2-10 MMC equivalent circuit of phase-j, j=a, b, c. (a) equivalent circuit on ac side; (b) equivalent circuit on dc side

$$i_{uj} = \frac{I_{dc}}{3} + \frac{i_{acj}}{2} + i_{cirj} \qquad (j = a, b, c) \tag{2-23}$$

$$i_{lj} = \frac{I_{dc}}{3} - \frac{i_{acj}}{2} + i_{cirj} \qquad (j = a, b, c) \tag{2-24}$$

The inner difference current is defined as [48, 54]

$$i_{diffj} = \frac{i_{uj} + i_{lj}}{2} = \frac{I_{dc}}{3} + i_{cirj} \qquad (j = a, b, c) \tag{2-25}$$

Substituting (2-25) into (2-23) and (2-24)

$$i_{uj} = \frac{i_{acj}}{2} + i_{diffj} \qquad (j = a, b, c) \tag{2-26}$$

$$i_{lj} = -\frac{i_{acj}}{2} + i_{diffj} \qquad (j = a, b, c) \tag{2-27}$$

The simplified circuit of 3-phase MMC is shown in Fig. 2-9.

According to equation (2-5) -(2-27), the voltages on the ac side are given by

$$u_j + \frac{L_0}{2}\frac{di_{acj}}{dt} + \frac{1}{2}R_0 i_{acj} = \frac{u_{lowerj} - u_{upperj}}{2} \qquad (j = a, b, c) \tag{2-28}$$

Voltages on the dc side are

$$U_{dc} - 2L_0\frac{di_{diffj}}{dt} - 2R_0 i_{diffj} = u_{upperj} + u_{lowerj} \qquad (j = a, b, c) \tag{2-29}$$

MMC equivalent circuits on the ac and the dc sides of phase-j can be obtained from (2-28) and (2-29) respectively, which are displayed in Fig. 2-10.

2.5 Conclusion

The configuration of 3-phase MMC has been described in this chapter. Focusing on half-bridge sub-module, its three operation states are elaborated. Among them, two are expressed as the normal operation states which are ‘insert/on state’ and ‘bypass/off state’. Different levels of voltage can be generated via inserting and bypassing the SMs in each arm. By introducing the basic operation principle for each phase of MMC, it is noted that the number of SMs with ‘on state’ in one arm is complementary with the ‘on state’ number in the other arm of the same phase. And this principle could be applied in PSC-PWM modulation method.

As the harmonics created by PSC-PWM can be pushed to high frequency spectrum by increasing either number of SMs or carrier frequency, these harmonics could be easily removed and out of concern for MMC practical applications.

In the last part of this chapter, the equivalent circuits of MMC on both ac and dc sides have been derived through basic circuit theory. On the basis of that, further analysis could be carried on.

Chapter 3 MMC Harmonic Function Analysis

3.1 Introduction

The methodology of research in MMC is based on building laboratory prototypes and evaluating their performance by simulations and experiments. Recently there has appeared what can be a definitive mathematical model of MMC [46] from the Royal Institute of Technology (KTH) Sweden. The mathematical model has been followed by harmonic function analysis [47, 48, 62] and applied to dynamic analysis [49] and global asymptotic stability analysis [63], [64]. The mathematical model has been validated by simulations and experiments.

This chapter contributes to harmonic function analysis [47, 48] by taking a different approach. Whereas KTH leaves the formulation in mathematical abstraction, the thesis has different objectives: (1) it gives an explanation of the formulation of in terms of capacitor modulation; (2) it delves into the mathematical formulas derived from capacitor modulation and relates them to the performance of MMC; (3) it applies the mathematical expressions to improve the design of MMC. These mathematical formulas are listed in Table 3-II and Table 3-III.

At this point, it is helpful to readers to know ahead of the text of the chapter that the mathematical formulas of primary modulation in Table 3-II and Table 3-III are voltages classified under frequencies: dc, fundamental harmonic, the 2^{nd} and the 3^{rd} harmonics. The inherent 2^{nd} harmonic component of single-phase ac power produces extraneous terms and hitherto unaccounted for dc, fundamental harmonic, 2^{nd}, 3^{rd} and other low frequency harmonics. This chapter shows that these extraneous and unwanted voltage and current originate from certain 2^{nd} harmonic voltages and by cancelling these 2^{nd} harmonic voltages, the extraneous unwanted terms can be eliminated.

This chapter reaches back to circuit theory fundamentals in Section 3.2 to clarify the bookkeeping of voltages charged across time-varying capacitors. Harmonic function

analysis is used in the bookkeeping and the development also leads to a model of MMC dynamics expressed in nonlinear ordinary differential equations. Simulation results validate the differential equation model in Section 3.3. Conclusions are presented in Section 3.4.

3.2 Harmonic Function Analysis of MMC

Unlike VSCs, which apply pulse width modulation (PWM) to control IGBTs to produce voltage pulses of varying widths, the IGBTs of MMC play the role of connecting and disconnecting integral numbers of charged capacitors in a series string. The operation of MMC is based on modulating the size of the resultant capacitor in a series string. For instance, if N capacitors, each of size C are strung in series, from circuit theory the equivalent capacitor is C/N.

When $n(t)$, the number of capacitors each of size C in a series string is time varying, the capacitor size is $C/n(t)$. If $u(t)$ is the voltage of the arm, from circuit theory its electric charge $q(t)$ is:

$$q(t) = \frac{C}{n(t)} u(t) \tag{3-1}$$

The current $i(t)$, which flows through the equivalent capacitor, is:

$$\frac{dq(t)}{dt} = i(t) \tag{3-2}$$

Substituting (3-1) in (3-2)

$$\frac{C}{n(t)} \frac{du(t)}{dt} + u(t) \frac{d\left(C \diagup n(t)\right)}{dt} = i(t) \tag{3-3}$$

The second term on the left hand side of (3-3) is $-[Cu(t)/n^2(t)]\times[dn(t)/dt]$. Although $n(t)$ is treated as a continuous time function in this chapter, in reality it consists of time functions in discrete steps. Between the instants of step changes, $n(t)$ is constant so that $dn(t)/dt=0$. Therefore the contribution of the second left hand term is zero most of the time.

One is left with the instants of switching, when $dn(t)/dt$ is an impulse function (obtained by differentiating a step function). The main interest in the theory is the voltage $u(t)$ of the arm which is solved by integration of the first term on the left hand side of (3-3).

Moving the impulse function to the right hand side of the equality sign, it is to be noted that an impulse function occupies a vanishingly small time span and its time integral is unity. The unity area is weighted by $-[Cu(t)/n^2(t)]$. Although $u(t)$ is still unsolved, $u(t)$ is finite in value. Because $n(t)$ makes one step change at a time, the result of integration cannot be large.

It is not necessary to evaluate the value exactly. Because the impulse functions occur at the instants of switching, they can be classified under switching noise. From the excellent agreement between the theory developed and simulation results, the author reaches the conclusion that the contributions of impulse functions are negligibly small in the low frequency spectrum.

Neglecting the effects of variation of $d[\frac{C}{n(t)}]/dt$ in (3-3), the equation reduces to

$$\frac{C}{n(t)}\frac{du(t)}{dt} = i(t) \tag{3-4}$$

Because the left side contains time varying quantities $u(t)$ and $n(t)$, the integration is performed in a few steps, each of which cannot be faulted. First, it is recalled that $n(t)$ is determined by the modulating signal $m(t)$ (< 1) in the formula $n(t)=Nm(t)$, where N is the total number of sub-modules in one arm. Substituting the formula in (3-4) and multiplying both sides by $m(t)$, (3-4) becomes

$$\frac{C}{N}\frac{du(t)}{dt} = i(t)\,\mathrm{m(t)} \tag{3-5}$$

As there is uncertainty as to what $u(t)$ stands for, one considers $i(t)m(t)$ flowing through one capacitor. The voltage $u^1(t)$ across a single capacitor is solved from

$$C\frac{du^1(t)}{dt} = i(t)\,\mathrm{m(t)} \tag{3-6}$$

Writing the symbol $u^N(t)$ as the voltage across N capacitors, $u^N(t) = Nu^1(t)$. The value of N capacitors connected in series is C/N. Therefore the voltage in (3-5) is $u^N(t)$, the voltage across N capacitors in series. As (3-5) is an important equation, it is rewritten as

$$\frac{C}{N}\frac{du^N(t)}{dt} = i(t)\,\mathrm{m(t)} \tag{3-7}$$

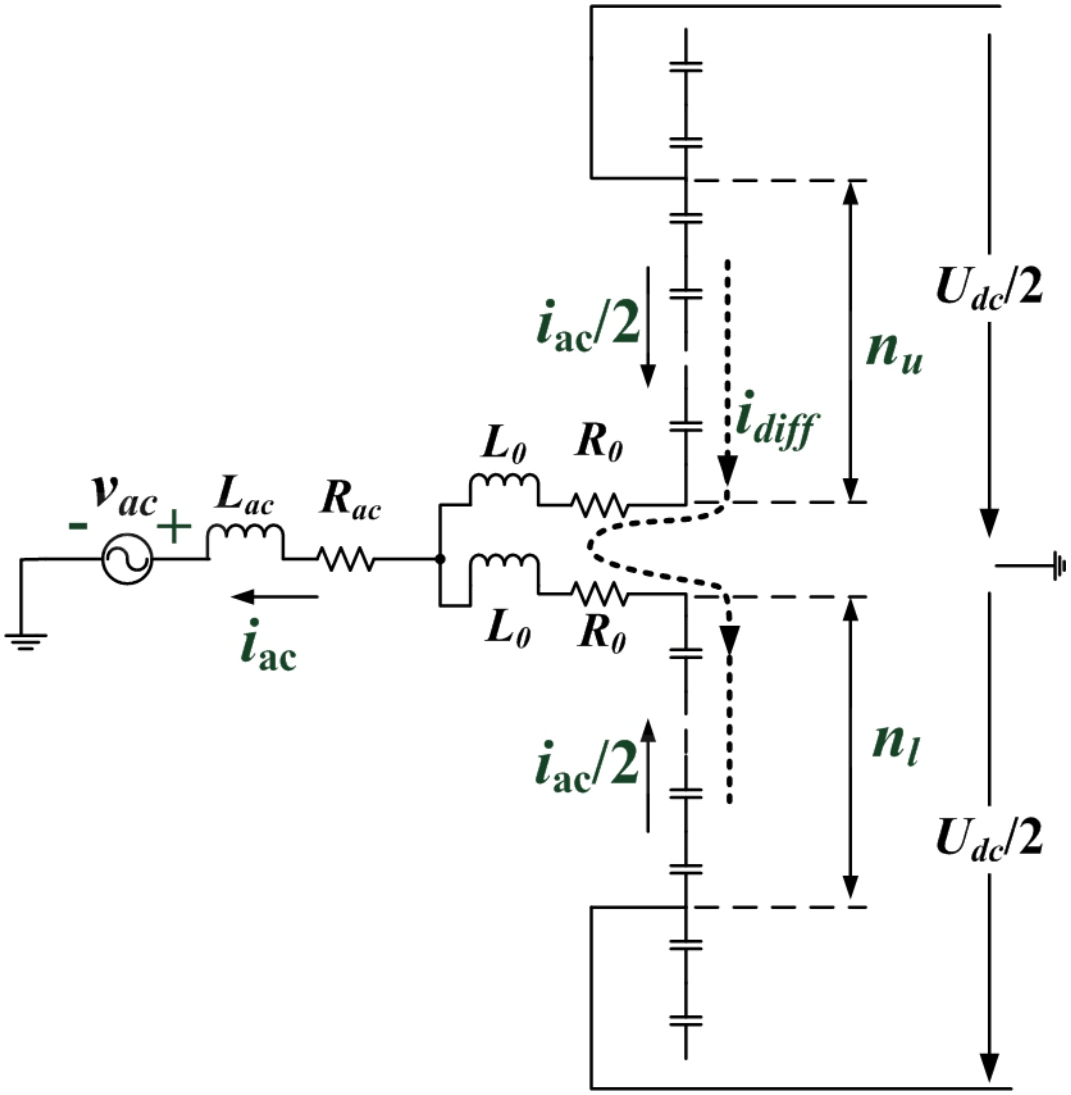


Fig. 3- 1 Charging of $n_u(t)$ and $n_l(t)$ capacitors of one MMC phase

3.2.1 One Phase Analysis of 3-phase MMC

Apart from the 120 degrees phase difference in each reference voltage, each phase of 3-phase MMC is identical. Therefore, to avoid repetitive formulation only the analysis of one phase is conducted.

MMC operation is based on modulating signals $m_u(t)$ and $m_l(t)$ sent to the upper arm and the lower arm of one phase respectively. Applying Phase Shifted Carrier PWM (PSC-PWM) described in Chapter 2, $n_u(t)$ and $n_l(t)$ capacitors are connected in a series string as illustrated in Fig. 3- 1. Subscripts u and l denote the upper arm and the lower arm respectively. Individual capacitor voltages are balanced by using a sorting algorithm from

[44] which has already been described in the last chapter. In Fig. 3- 1 v_{ac} denotes the voltage, L_{ac} represents the inductance and R_{ac} is the resistance of one phase of the ac system. The currents flowing through the capacitors are half of the ac current, $i_{ac}/2$, and differential mode current i_{diff} with the directions indicated.

A. Analysis of Upper Arm

The voltage reference is defined as:

$$u_{ref}(t) = U_{ref}\cos(\omega t + \delta) \tag{3-8}$$

U_{ref} is the magnitude of reference output voltage of one phase, ω is the reference voltage angular velocity (in radians per second) and δ represents the phase angle of reference voltage.

For modulating signal

$$m_u(t) = \frac{1}{2} - \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta) \tag{3-9}$$

applied to the upper arm, the PSC-PWM strategy connects $n_u(t)$ capacitors (each of size C) in series

$$n_u(t) = N[\frac{1}{2} - \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)] \tag{3-10}$$

where N is the total number of sub-modules in each arm.

The voltage $u^1{}_u(t)$ across single capacitor in the upper arm is based on integrating equation (3-6) with the currents in Fig. 3- 1.

$$C\frac{du^1{}_u(t)}{dt} = \frac{n_u(t)}{N}\left[0.5i_{ac}(t) + i_{diff}(t)\right] \tag{3-11}$$

Substituting (3-9) and (3-10) into (3-11), it becomes:

$$C\frac{du^1{}_u(t)}{dt} = m_u(t)\left[0.5i_{ac}(t) + i_{diff}(t)\right] \tag{3-12}$$

For bookkeeping convenience, the voltage $u^N{}_u(t)$, voltage across an equivalent capacitor of constant size C/N , is calculated at first. $u^N{}_u(t)$ is expressed as:

$$u^N{}_u(t) = Nu^1{}_u(t) \tag{3-13}$$

and thus

$$\frac{du^N{}_u(t)}{dt} = \frac{N}{C} m_u(t)\left[0.5 i_{ac}(t) + i_{diff}(t)\right] \tag{3-14}$$

For the reference ac voltage in (3-9), the steady-state ac current in (3-14) takes the form:

$$i_{ac}(t) = I_{ac}\cos(\omega t + \varphi_{ac}) \tag{3-15}$$

where I_{ac} is the magnitude of the ac current and φ_{ac} represents the phase shift of the ac current.

It is assumed that differential mode current i_{diff} consists of a dc current I_d and a 2nd harmonic circulating current $i_{2\omega}$:

$$i_{diff}(t) = I_d + i_{2\omega}(t) \tag{3-16}$$

$$I_d = \frac{I_{dc}}{3} \tag{3-17}$$

$$i_{2\omega}(t) = X\cos(2\omega t + \varphi_2) \tag{3-18}$$

Here, I_{dc} is the total dc current of 3-phase MMC; I_d denotes the dc current of one phase; X is the magnitude of 2nd harmonic circulating current and φ_2 is the phase shift of 2nd harmonic circulating current. I_d, X and φ_2 are unknowns to be solved. The reduced number of unknowns (in contrast to the infinite series of [48]) trades mathematical preciseness for analytical insights.

Substituting (3-9), (3-15)-(3-18) into (3-14)

$$\frac{du^N{}_u(t)}{dt} = \frac{N}{C}\left[\frac{1}{2} - \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)\right]\cdot\left\{\frac{I_{ac}}{2}\cos(\omega t + \varphi_{ac}) + \left[I_d + X\cos(2\omega t + \varphi_2)\right]\right\} \tag{3-19}$$

For bookkeeping convenience, the voltage $u^N{}_u(t)$ is decomposed as:

$$u^N{}_u(t) = 2T_1 + 2T_2 + 2T_3 + 2T_4 \tag{3-20}$$

The decomposition is not unique. It is the sum of the components which matters.

The integration of (3-19) consists of:

$$\frac{d\,2T_1}{dt} = \frac{N}{C}\left[\frac{I_{ac}}{4}\cos(\omega t + \varphi_{ac})\right] \tag{3-21}$$

$$\frac{d\,2T_2}{dt} = \frac{N}{C}\left[\frac{I_d}{2} - \frac{U_{ref} I_{ac}}{4U_{dc}}\cos(\delta - \varphi_{ac})\right] \tag{3-22}$$

$$\frac{d\,2T_3}{dt} = \frac{N}{C}\left[\frac{X\cos(2\omega t + \varphi_2)}{2} - \frac{U_{ref} I_{ac}}{4U_{dc}}\cos(2\omega t + \varphi_{ac} + \delta)\right] \tag{3-23}$$

$$\frac{d2T_4}{dt} = \frac{N}{C}\left[I_d + X\cos(2\omega t + \varphi_2)\right]\cdot\left[\frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)\right] \tag{3-24}$$

The right hand side of (3-24) contains products of $cos(m\omega t+\gamma_m)$ and $cos(n\omega t+\gamma_n)$. From trigonometric identity, the product yields $0.5cos[(m+n)\omega t+(\gamma_m+\gamma_n)]+0.5cos[(m-n)\omega t+(\gamma_m-\gamma_n)]$. The sum $(m+n)$ and the difference $(m-n)$ of harmonics are the "mechanisms" of harmonic proliferation.

On integration, the voltage terms T_1, T_2, T_3 *and* T_4 are listed in Table 3-I.

It needs to be stressed that $u^N{}_u(t)$ is the voltage across N capacitors. For modulating signal of (3-9), $n_u(t)$ capacitors of (3-10) are connected in series as illustrated in Fig. 3- 1. Therefore, the voltage $u_{upper}(t)$ (actual operating upper arm voltage) across $n_u(t)$ capacitors is

$$\begin{aligned} u_{upper}(t) &= n_u(t)\frac{u^N{}_u(t)}{N} \\ &= \left[\frac{1}{2} - \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)\right]\cdot 2\left(T_1 + T_2 + T_3 + T_4\right) \\ &= T_1 + T_2 + T_3 + T_4 + T_5 + T_6 + T_7 + T_8 \end{aligned} \tag{3-25}$$

where

$$T_{y+4} = -\frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)\cdot 2T_y \qquad for\ y = 1, 2, 3, 4 \tag{3-26}$$

T_5, T_6, T_7 and T_8 are also in Table 3-I. The proliferation from 4 to 8 terms in (3-25) is again due to the product of trigonometric functions described by (3-26).

B. Analysis of Lower Arm

The modulating signal of the lower arm is:

$$m_l(t) = \frac{1}{2} + \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta) \tag{3-27}$$

Table 3-I Arm voltage terms from T_1 to T_8

Voltage Term	Expression
T_1	$\frac{NI_{ac}}{8\omega C}\sin(\omega t+\varphi_{ac})$
T_2	$\frac{N}{2C}\int_{-\infty}^{t}\left[\frac{I_d}{2}-\frac{U_{ref}I_{ac}}{4U_{dc}}\cos\left(\delta-\varphi_{ac}\right)\right]\cdot d\tau$
T_3	$\frac{NX}{8\omega C}\sin\left(2\omega t+\varphi_2\right)-\frac{NU_{ref}I_{ac}}{16\omega CU_{dc}}\sin\left(2\omega t+\delta+\varphi_{ac}\right)$
T_4	$-\frac{NU_{ref}I_d}{2\omega CU_{dc}}\sin(\omega t+\delta)-\frac{NU_{ref}X}{4\omega CU_{dc}}\sin(\omega t+\varphi_2-\delta)-\frac{NU_{ref}X}{12\omega CU_{dc}}\sin(3\omega t+\varphi_2+\delta)$
T_5	$-\frac{NU_{ref}I_{ac}}{8\omega CU_{dc}}\sin\left(\varphi_{ac}-\delta\right)-\frac{NU_{ref}I_{ac}}{8\omega CU_{dc}}\sin\left(2\omega t+\delta+\varphi_{ac}\right)$
T_6	$-\frac{NU_{ref}}{CU_{dc}}\cos(\omega t+\delta)\cdot\int_{-\infty}^{t}\left[\frac{I_d}{2}-\frac{U_{ref}I_{ac}}{4U_{dc}}\cos\left(\delta-\varphi_{ac}\right)\right]\cdot d\tau$
T_7	$-\frac{NU_{ref}X}{8\omega CU_{dc}}\sin\left(\omega t+\varphi_2-\delta\right)+\frac{NU_{ref}^2I_{ac}}{16\omega CU_{dc}^2}\sin\left(\omega t+\varphi_{ac}\right)$ $-\frac{NU_{ref}X}{8\omega CU_{dc}}\sin\left(3\omega t+\varphi_2+\delta\right)+\frac{NU_{ref}^2I_{ac}}{16\omega CU_{dc}^2}\sin\left(3\omega t+2\delta+\varphi_{ac}\right)$
T_8	$\frac{NU_{ref}^2X}{4\omega CU_{dc}^2}\sin\left(\varphi_2-2\delta\right)+\frac{NU_{ref}^2I_d}{2\omega CU_{dc}^2}\sin\left(2\omega t+2\delta\right)$ $+\frac{NU_{ref}^2X}{3\omega CU_{dc}^2}\sin\left(2\omega t+\varphi_2\right)+\frac{NU_{ref}^2X}{12\omega CU_{dc}^2}\sin\left(4\omega t+\varphi_2+2\delta\right)$

Because of the reversal in direction of i_{ac} in the lower arm of Fig. 3- 1 and the sign change of the term of U_{ref} in (3-27), the voltage $u^N{}_l(t)$ across N capacitors of the lower arm is:

$$\frac{du^N{}_l(t)}{dt}=\frac{N}{C}m_l(t)\left[-0.5i_{ac}(t)+i_{diff}(t)\right] \tag{3-28}$$

Substituting (3-27), (3-15)-(3-18) in (3-28)

$$\frac{du^N{}_l(t)}{dt} = \frac{N}{C}\left[\frac{1}{2} + \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)\right] \cdot \left\{-\frac{I_{ac}}{2}\cos(\omega t + \varphi_{ac}) + \left[I_d + X\cos(2\omega t + \varphi_2)\right]\right\} \quad (3\text{-}29)$$

Similarly, voltage $u^N{}_l(t)$ is decomposed as:

$$u^N{}_l(t) = -2T_1 + 2T_2 + 2T_3 - 2T_4 \quad (3\text{-}30)$$

which is with same terms from T_1 to T_4 except that T_1 and T_4 are with opposite signs. The voltage $u_{lower}(t)$ (actual operating lower arm voltage) across $n_l(t)$ capacitors is:

$$\begin{aligned} u_{lower}(t) &= n_l(t)\frac{u^N{}_l(t)}{N} \\ &= \left[\frac{1}{2} + \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta)\right] \cdot 2\left(-T_1 + T_2 + T_3 - T_4\right) \\ &= -T_1 + T_2 + T_3 - T_4 + T_5 - T_6 - T_7 + T_8 \end{aligned} \quad (3\text{-}31)$$

The lower arm voltage contains the same eight terms as the upper arm one, though four of them are with opposite sign.

C. Equivalent Circuit Based on Voltage Sources

According to the analysis in section 2.4 of Chapter 2, the equivalent voltage of upper and lower arms on ac side is

$$u_{ac-side}(t) = \frac{1}{2}\left[u_{lower}(t) - u_{upper}(t)\right] \quad (3\text{-}32)$$

The equivalent voltage of upper and lower arms on dc side is

$$u_{dc-side}(t) = u_{upper}(t) + u_{lower}(t) \quad (3\text{-}33)$$

Substituting (3-25) and (3-31) into (3-32) and (3-33)

$$u_{ac-side}(t) = -(T_1 + T_4 + T_6 + T_7) \quad (3\text{-}34)$$

$$u_{dc-side}(t) = 2(T_2 + T_3 + T_5 + T_8) \quad (3\text{-}35)$$

Fig. 3- 2 (a) shows the voltage components T_1, T_2,…T_8 of the upper and lower arm of Fig. 3-1 connected together with +ve and –ve polarities clearly marked. According to equation (3-34) and (3-35), the ac-side and the dc-side equivalent circuits take the forms of Fig. 3- 2 (b) and (c) respectively. From Table 3-I, it is noted that four terms (T_1, T_4, T_6 and T_7) which appear on the ac side only consist of fundamental frequency and third harmonic components whereas the other four terms (T_2, T_3, T_5 and T_8) on the dc side are comprised of dc components and even order harmonics. That is to say, when transferring

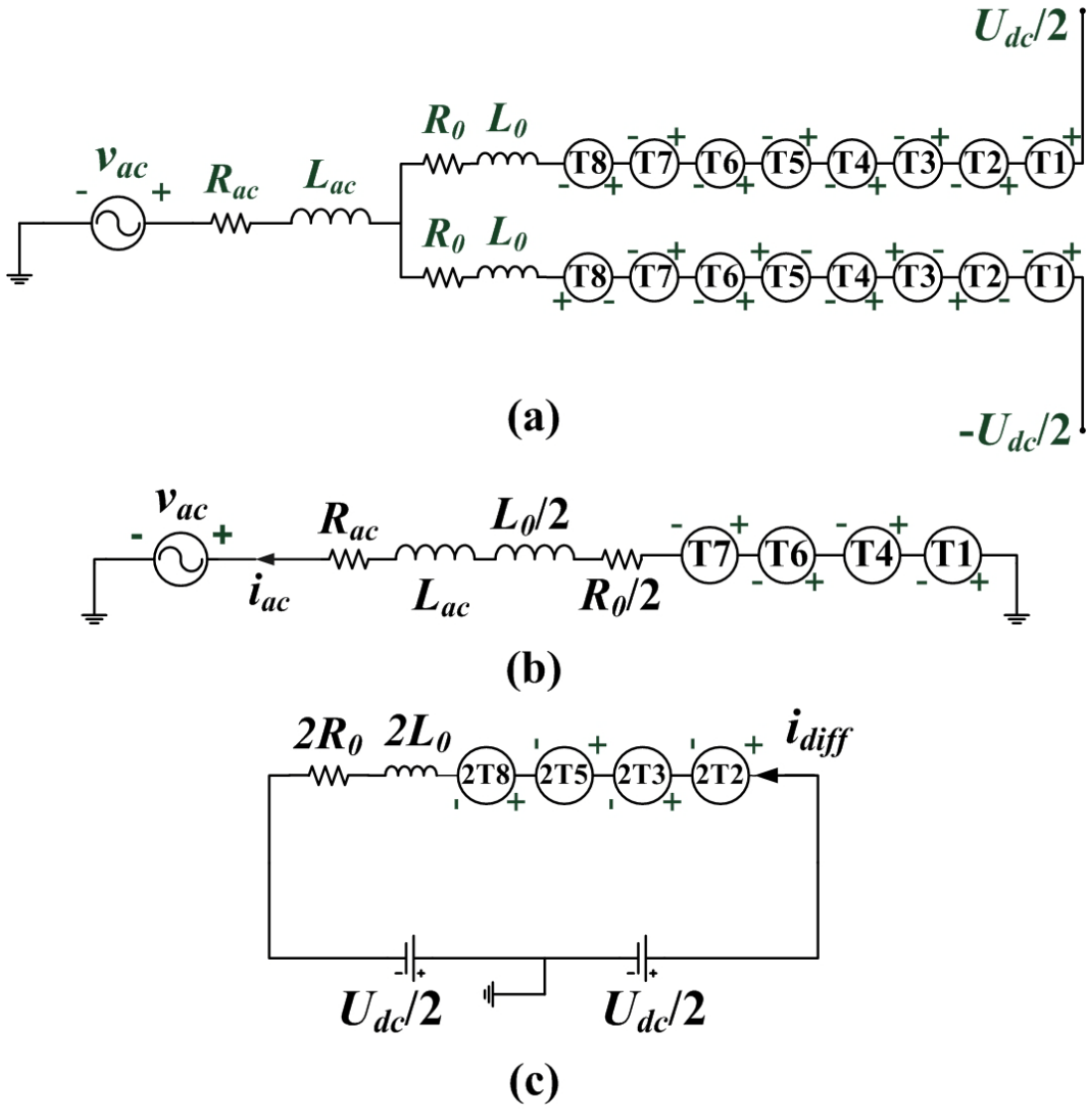


Fig. 3- 2 MMC equivalent circuit based on voltage sources in Table 3-II and Table 3-III: (a) upper and lower arms; (b) ac-side; (c) dc-side

power from dc side to ac side or the other way around, the even-order harmonics and odd-order harmonics are separated to line up on the dc and ac sides respectively.

The columns in Table 3-II and Table 3-III classify the formulas of T_y, y=1, 2,...8 according to their harmonic content. Further subscripts are added to y. For example in Table 3-II: $T_{4\text{-}\omega}$ and $T_{4\text{-}3\omega}$ are the fundamental and the 3rd harmonic component of T_4. In Table 3-III, $T_{8\text{-}2\omega\text{-}i}$ and $T_{8\text{-}2\omega\text{-}ii}$ are two 2nd harmonic terms of T_8. Error, inherent in the arbitrary truncation of harmonics at the 3rd, is acceptably small as the simulation results shown in the section 4.4 of Chapter 4.

Table 3-II AC-side equivalent voltage components

	ω	3ω
T_1	$\frac{NI_{ac}}{8\omega C}\sin(\omega t+\varphi_{ac})$	--
T_4	$-\frac{NU_{ref}I_d}{2\omega CU_{dc}}\sin(\omega t+\delta)$ $-\frac{NU_{ref}X}{4\omega CU_{dc}}\sin(\omega t+\varphi_2-\delta)$	$-\frac{NU_{ref}X}{12\omega CU_{dc}}\sin(3\omega t+\varphi_2+\delta)$
T_6	$-\frac{NU_{ref}}{CU_{dc}}\cos(\omega t+\delta)\cdot$ $\int_{-\infty}^{t}\left[\frac{I_d}{2}-\frac{U_{ref}I_{ac}}{4U_{dc}}\cos(\delta-\varphi_{ac})\right]\cdot d\tau$	--
T_7	$-\frac{NU_{ref}X}{8\omega CU_{dc}}\sin(\omega t+\varphi_2-\delta)$ $\frac{NU_{ref}^2I_{ac}}{16\omega CU_{dc}^2}\sin(\omega t+\varphi_{ac})$	$-\frac{NU_{ref}X}{8\omega CU_{dc}}\sin(3\omega t+\varphi_2+\delta)$ $\frac{NU_{ref}^2I_{ac}}{16\omega CU_{dc}^2}\sin(3\omega t+2\delta+\varphi_{ac})$

Table 3-III DC-side equivalent voltage components

	dc	2ω
T_2	$\frac{N}{2C}\int_{-\infty}^{t}\left[\frac{I_d}{2}-\frac{U_{ref}I_{ac}}{4U_{dc}}\cos(\delta-\varphi_{ac})\right]\cdot d\tau$	--
T_3	--	$\frac{NX}{8\omega C}\sin(2\omega t+\varphi_2)$ $-\frac{NU_{ref}I_{ac}}{16\omega CU_{dc}}\sin(2\omega t+\delta+\varphi_{ac})$
T_5	$-\frac{NU_{ref}I_{ac}}{8\omega CU_{dc}}\sin(\varphi_{ac}-\delta)$	$-\frac{NU_{ref}I_{ac}}{8\omega CU_{dc}}\sin(2\omega t+\delta+\varphi_{ac})$
T_8	$\frac{NU_{ref}^2X}{4\omega CU_{dc}^2}\sin(\varphi_2-2\delta)$	$\frac{NU_{ref}^2I_d}{2\omega CU_{dc}^2}\sin(2\omega t+2\delta)$ $\frac{NU_{ref}^2X}{3\omega CU_{dc}^2}\sin(2\omega t+\varphi_2)$

D. Major Entries on DC and AC sides of Tables

1). On DC Side

Voltage T_2

Referring to Table 3-III, T_2 comes from charging of the capacitors by the time invariant component of one phase ac power which is converted to dc power $I_d U_{dc}$. The voltage T_2 increases or decreases until power balance is established.

$$\frac{I_d}{2} = \frac{U_{ref} I_{ac}}{4U_{dc}} \cos(\delta - \varphi_{ac}) \tag{3-36}$$

In power balance

$$P_{ac} = \frac{U_{ref} I_{ac}}{2} \cos(\delta - \varphi_{ac}) = U_{dc} I_d = P_{dc} \tag{3-37}$$

Since T_2 dominates the dc side voltage in terms of value, one concludes that

$$2T_2 \approx U_{dc} \tag{3-38}$$

Voltage T_5

T_5 comes from multiplying $2T_1$ with $-U_{ref}cos(\omega t+\delta)/U_{dc}$ shown in equation (3-26),

$$T_5 = T_{5-dc} + T_{5-2\omega} = -\frac{NU_{ref} I_{ac}}{8\omega C U_{dc}} \sin\left(\varphi_{ac} - \delta\right) - \frac{NU_{ref} I_{ac}}{8\omega C U_{dc}} \sin\left(2\omega t + \delta + \varphi_{ac}\right) \tag{3-39}$$

When dc current I_d flows across $2T_{5\text{-}dc}$, there is a new time-invariant power term

$$P_{T_{5-dc}} = \frac{NU_{ref} I_{ac} I_d}{4\omega C U_{dc}} \sin(\delta - \varphi_{ac}) \tag{3-40}$$

Its corresponding ac voltage source term $T_{4\text{-}\omega\text{-}i}$ on the ac side as will be discussed shortly.

Voltages T_3, T_5, T_8

The double frequency terms in Table 3-III are $T_{3\text{-}2\omega\text{-}i}$, $T_{3\text{-}2\omega\text{-}ii}$, $T_{5\text{-}2\omega}$, $T_{8\text{-}2\omega\text{-}i}$ and $T_{8\text{-}2\omega\text{-}ii}$. They can be divided into two groups: (1) terms devoid of '*X*' ($T_{3\text{-}2\omega\text{-}ii}$, $T_{5\text{-}2\omega}$ and $T_{8\text{-}2\omega\text{-}i}$); (2) terms with '*X*' ($T_{3\text{-}2\omega\text{-}i}$ and $T_{8\text{-}2\omega\text{-}ii}$), which will be discussed in detail in section 4.2 of Chapter 4. The '*X*' terms come from the mathematical unknown in (3-18): $i_{2\omega}(t)=Xcos(2\omega t+\varphi_2)$.

2). On AC Side

Voltage T_4

T_4 has two fundamental frequency voltages and a 3rd harmonic voltage. The fundamental component $T_{4\text{-}\omega\text{-}i}$

$$T_{4-\omega-i} = -\frac{NU_{ref}I_d}{2\omega CU_{dc}}\sin(\omega t+\delta) \tag{3-41}$$

is a new ac side voltage source beside the voltage controlled by u_{ref}. It originates from I_d and lags u_{ref} by 90 degrees.

When ac current of $I_{ac}cos(\omega t+\varphi_{ac})$ flows through $T_{4\text{-}\omega\text{-}i}$, the time invariant power is

$$P_{T_{4-\omega-i}} = -\frac{NU_{ref}I_{ac}I_d}{4\omega CU_{dc}}\sin(\delta-\varphi_{ac}) \tag{3-42}$$

Referring to the formula in (3-40)

$$P_{T_{4-\omega-i}} + P_{T_{5-dc}} = 0 \tag{3-43}$$

The power balance in (3-43) shows that the ac power associated with $T_{4\text{-}\omega\text{-}i}$ is converted to dc power. Substituting (3-42) and (3-37) together with (3-36), one obtains the ratio

$$\frac{P_{T_{5-dc}}}{P_{ac}} = \frac{NI_d}{2\omega CU_{dc}}\frac{\sin(\delta-\varphi_{ac})}{\cos(\delta-\varphi_{ac})} = \frac{NU_{ref}I_{ac}}{4\omega CU_{dc}^2}\sin(\delta-\varphi_{ac}) \tag{3-44}$$

Because of U^2_{dc} in the denominator, (3-44) is very small. Although interesting, one concludes that the voltages of $T_{4\text{-}\omega\text{-}i}$ and $T_{5\text{-}dc}$ can be neglected.

Voltage T_6

According to (3-26), T_6 is equal to $2T_2$ multiplied by $-U_{ref}cos(\omega t+\delta)/U_{dc}$. As $2T_2 \approx U_{dc}$ according to equation (3-38), T_6 is the ac voltage reference of (3-9) amplified by gain U_{dc}.

Voltage T_1, T_7 (Fundamental Harmonic Terms)

The voltages $T_{1\text{-}\omega}$ and $T_{7\text{-}\omega\text{-}ii}$ mean that portions of the capacitor C of SMs form a series capacitive reactance in the ac circuit of Fig. 3- 2 (b). Because the ac current is a cosine function given by (3-15) and $T_{1\text{-}\omega}$ and $T_{7\text{-}\omega\text{-}ii}$ are sine functions, they are capacitive reactance voltages. They can be used for series capacitor compensation. Incorporating them, the reactance in the ac-line is:

$$X_{ac} = \omega(L_{ac} + \frac{L_0}{2}) - (\frac{NU_{ref}^2}{16\omega C U_{dc}^2} + \frac{N}{8\omega C}) \tag{3-45}$$

Voltages T_4, T_7 (3^{rd} Harmonic Terms)

The 3rd harmonic voltage terms in Table 3-II are $T_{4\text{-}3\omega}$, $T_{7\text{-}3\omega\text{-}i}$ and $T_{7\text{-}3\omega\text{-}ii}$. $T_{4\text{-}3\omega}$ and $T_{7\text{-}3\omega\text{-}i}$ carry the 'X' of the 2nd harmonic current mathematical unknown assumed in (3-18). This implies that when the 2nd harmonic circulating current is eliminated, the 3rd harmonic voltage of $T_{4\text{-}3\omega}$ and $T_{7\text{-}3\omega\text{-}i}$ disappears. The term without 'X' in T_7 is a very small term because the denominator U_{dc}^2 is very large.

Voltage Terms with U_{dc}^2 in Denominator

In Table 3-II and Table 3-III, all terms carrying U_{dc}^2 are small and can be neglected. The square term of U_{dc} in the denominator originates from (3-26).

Voltage Term with 'X'

Voltage terms carrying 'X' come from 2nd harmonic proliferation. When the 2nd harmonic circulating current is eliminated, all these terms are also eliminated.

3.2.2 Nonlinear Ordinary Differential Equation Model of MMC

This sub-section develops the ordinary nonlinear differential equations which can be used to predict the transient behavior and the stability of MMC. Although the symbols used are different, the formulation is the same as used in [46, 48, 62].

Equation (3-19) is generalized as:

$$\frac{du^N_{uj}(t)}{dt} = \frac{N}{C}\left[\frac{1}{2} - \frac{u_{refj}(t)}{U_{dc}}\right]\left[\frac{i_{acj}(t)}{2} + i_{diffj}(t)\right] \qquad (j = a, b, c) \tag{3-46}$$

where $u_{refj}(t)=U_{refj}cos(\omega t+\delta_j)$ for j=a, b, c. For balanced three phase system, $U_{refa}=U_{refb}=U_{refc}$, $\delta_a = \delta_b+120° = \delta_c+240°$.

The corresponding equation for the lower arm is

$$\frac{du^N_{lj}(t)}{dt} = \frac{N}{C}\left[\frac{1}{2} + \frac{u_{refj}(t)}{U_{dc}}\right]\left[-\frac{i_{acj}(t)}{2} + i_{diffj}(t)\right] \qquad (j = a, b, c) \tag{3-47}$$

Corresponding to (3-25) and (3-31)

$$u_{upperj}(t) = \left[\frac{1}{2} - \frac{u_{refj}(t)}{U_{dc}}\right] u^N_{uj}(t) \qquad (j = a, b, c) \tag{3-48}$$

$$u_{lowerj}(t)=\left[\frac{1}{2}+\frac{u_{refj}(t)}{U_{dc}}\right]u^{N}{}_{lj}(t) \qquad (j=a,b,c) \tag{3-49}$$

According to (3-32)

$$u_{ac-sidej}(t)=\frac{1}{4}\left[u^{N}{}_{lj}(t)-u^{N}{}_{uj}(t)\right]+\frac{u_{refj}(t)}{2U_{dc}}\left[u^{N}{}_{uj}(t)+u^{N}{}_{lj}(t)\right] \qquad (j=a,b,c) \tag{3-50}$$

For the ac side illustrated by Fig. 3- 2 (b), the ac current $i_{acj}(t)$ is solved by

$$\begin{aligned}\frac{di_{acj}(t)}{dt}&=\frac{1}{L_{ac}+0.5L_0}\left[-v_{acj}(t)-u_{ac-sidej}(t)-(R_{ac}+0.5R_0)i_{acj}(t)\right]\\&=\frac{1}{L_{ac}+0.5L_0}\left\{-v_{acj}(t)-\left\{\frac{1}{4}\left[u^{N}{}_{lj}(t)-u^{N}{}_{uj}(t)\right]+\frac{u_{refj}(t)}{2U_{dc}}\left[u^{N}{}_{uj}(t)+u^{N}{}_{lj}(t)\right]\right\}\right.\\&\qquad\left.-(R_{ac}+0.5R_0)i_{acj}(t)\right\}\\&\qquad(j=a,b,c)\end{aligned} \tag{3-51}$$

According to(3-33), the dc voltages sum to

$$u_{dc-sidej}(t)=\frac{1}{2}\left[u^{N}{}_{uj}(t)+u^{N}{}_{lj}(t)\right]-\frac{u_{refj}(t)}{U_{dc}}\left[u^{N}{}_{uj}(t)-u^{N}{}_{lj}(t)\right] \qquad (j=a,b,c) \tag{3-52}$$

For dc side circuit of Fig. 3- 2 (b), the current $i_{diffj}(t)$ is solved from

$$\begin{aligned}\frac{di_{diffj}(t)}{dt}&=\frac{1}{2L_0}[U_{dc}-i_{diffj}(t)R_0-u_{dc-sidej}(t)]\\&=\frac{1}{2L_0}\left\{U_{dc}-i_{diffj}(t)R_0-\frac{1}{2}\left[u^{N}{}_{uj}(t)+u^{N}{}_{lj}(t)\right]+\frac{u_{refj}(t)}{U_{dc}}\left[u^{N}{}_{uj}(t)-u^{N}{}_{lj}(t)\right]\right\}\\&\qquad(j=a,b,c)\end{aligned} \tag{3-53}$$

The 4 state variables are i_{acj}, i_{diffj}, $u^{N}{}_{uj}$ and $u^{N}{}_{lj}$ are solved from the 4 nonlinear ordinary differential equations(3-46), (3-47), (3-51) and (3-53) with $u_{refj}(t)$ as input. Although the symbols are different, this formulation corresponds to that in [46].

3.3 Simulation Results

The MMC based on the configuration of Fig. 2-1 (a) is simulated in the Simulink/MATLAB environment. In the simulations, PSC-PWM technique convert $m_u(t)$ and $m_l(t)$ to $n_u(t)$ and $n_l(t)$ capacitors. Individual capacitor voltages are balanced by using a sorting algorithm from [44]. The parameters of the main circuit are shown in Table 3-IV.

Table 3-IV Parameters used in the 3-phase MMC simulation

Items	Values	Items	Values
DC Bus Voltage U_{dc}	60 kV	Reference Voltage Magnitude U_{ref}	27 kV
Number of SMs per Arm N	12	Frequency f	50 Hz
SM Capacitance C	10 mF	AC System Voltage v_{ac}	25 kV (peak value)
Arm Inductance L_0	3 mH	AC System Inductance L_{ac}	10 mH
Arm Equivalent Resistance R_0	0.3 Ω	AC System Resistance R_{ac}	0.5 Ω

3.3.1 Validation of Nonlinear Ordinary Differential Equation Model of MMC

Nonlinear ordinary differential equation model of is verified in this section. Fig. 3- 3, Fig. 3- 4 and Fig. 3- 5 show the comparison test results of the four sets of state variables i_{acj}, i_{diffj}, u^N_{uj} and u^N_{lj} between simulation results and calculated results. Fig. 3- 6 presents the results of MMC upper and lower arm voltages of phase a. Simulation results (blue solid line) are obtained through Simulink Model which is using detailed models of IGBT, diode, inductor, capacitor and other components included in the SimPowerSystem model library of Simulink/MATLAB. Calculated results (red dashed line) are from the solution of four nonlinear differential equations (3-46), (3-47), (3-51) and (3-53) (Function Analysis Model). All the parameters used are listed in Table 3-IV. Curves obtained from Simulink Model correspondingly coincide with the ones from nonlinear ordinary differential equation model, which demonstrates the correctness of the latter model.

3.4 Conclusion

Starting with circuit theory fundamentals, this chapter introduces harmonic function analysis by charging across a constant sub-module capacitor. Mathematical formulas derived from harmonic function analysis are listed in Table 3-II and Table 3-III, which enable the complexity of MMC to be pried apart for understanding. For instance, the equivalent circuit of MMC on both the ac side and the dc side are ideal voltage sources. It has implications as to whether MMC is suited for series or parallel connection on the dc side. Moreover, nonlinear ordinary differential equation model of MMC is obtained. Simulation results verify the correctness of the differential equation model.

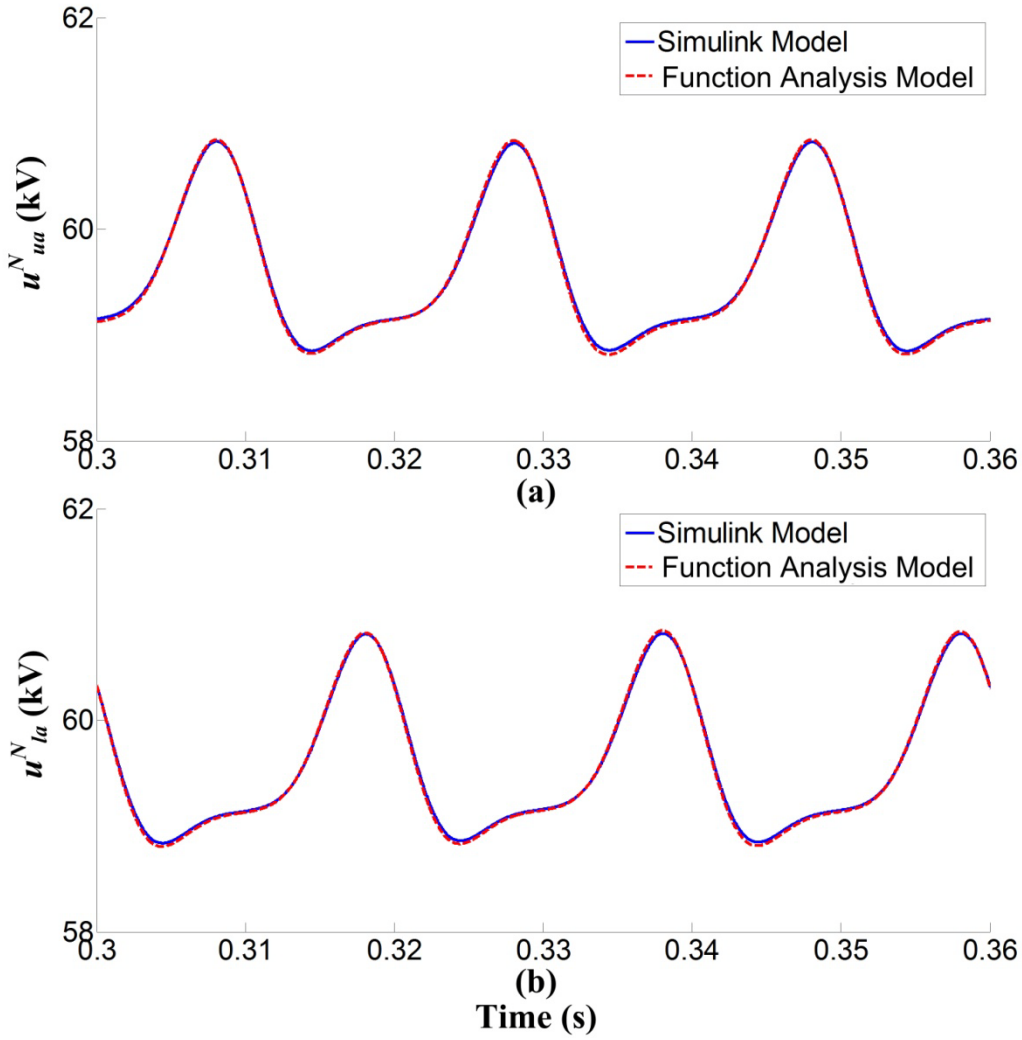


Fig. 3- 3 MMC voltage across N capacitors in each arm of phase a: (a) upper arm; (b) lower arm

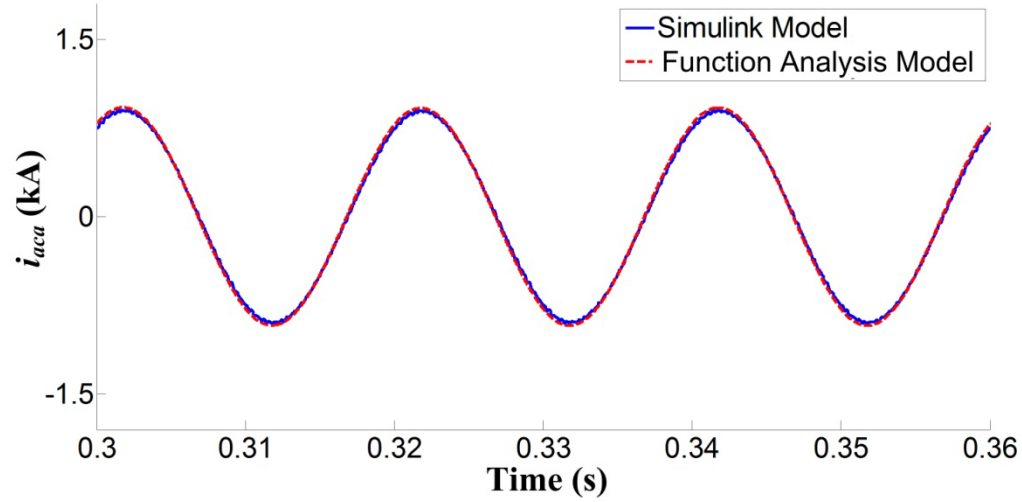


Fig. 3- 4 MMC output ac current of phase a

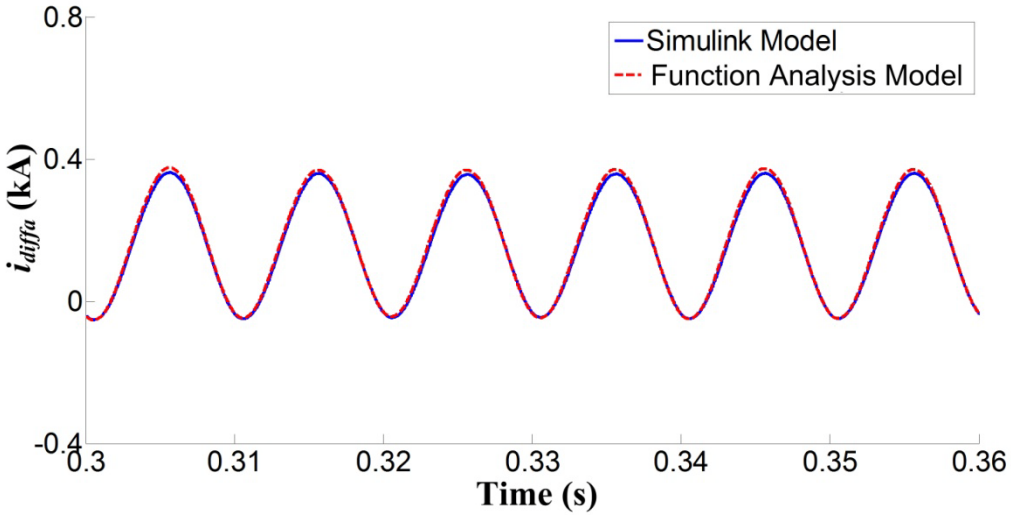


Fig. 3- 5 MMC difference current of phase a

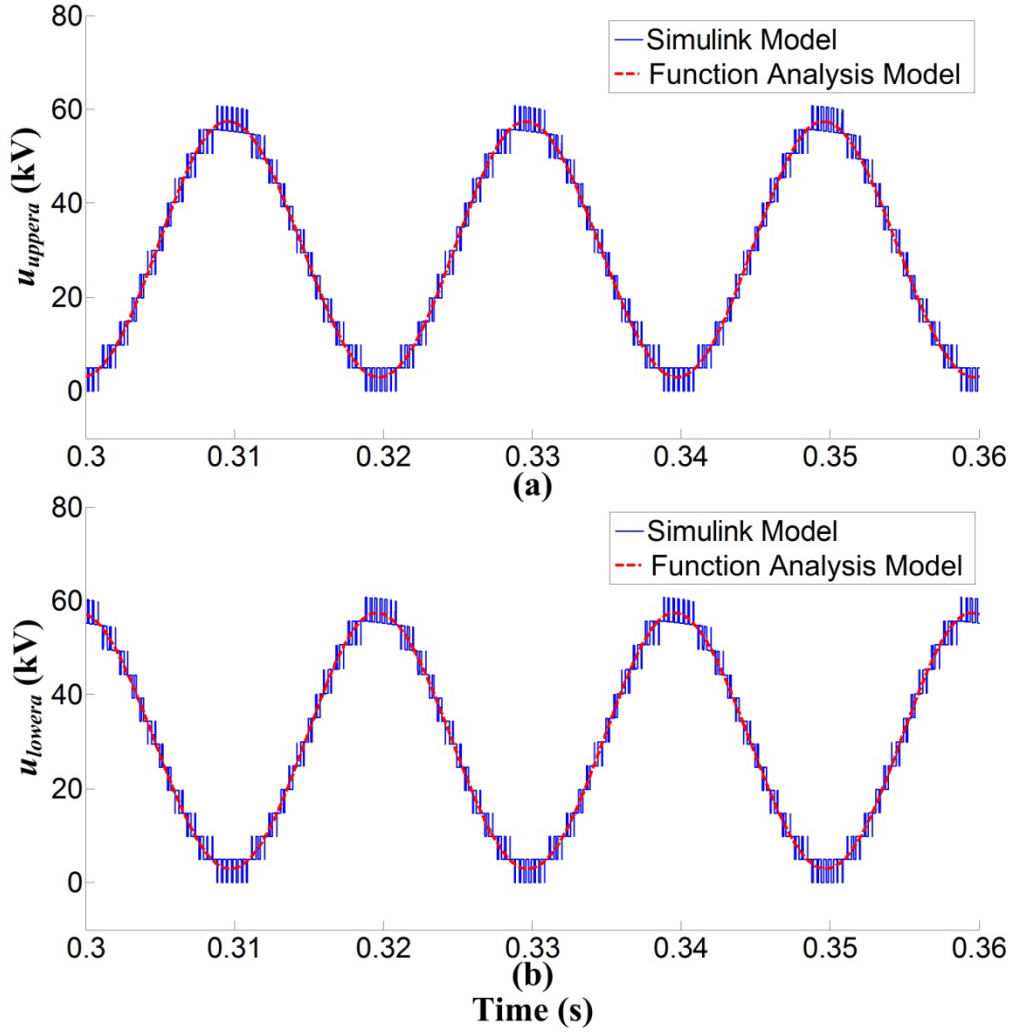


Fig. 3- 6 MMC arm voltages of phase a: (a) upper arm voltage; (b) lower arm voltage

Chapter 4 Low-Order Harmonic Reduction of MMC

4.1 Introduction

One major advantage of the modular multilevel converter is that the switching rate at each sub-module can be very low thus keeping switching loss to a minimum. Because phase shifted carrier PWM (PSC-PWM) can be applied, switching harmonics of the resultant voltage waveform have been shifted to high frequency spectrum.

MMC has its down side which comes from the fact that the capacitor of each sub-module belongs to one particular phase. The double-frequency component of single-phase ac power is retained in the phase and is the cause of low-order harmonics. Hitherto, MMC HVDC is viable because the low frequency harmonics are "filtered". Low frequencies are more expensive to filters because the components of filters are large and costly. The objective is to reduce the low frequencies by feed-forward or feedback thus lowering the size of the capacitors and the cost of MMC. Research has already been initiated to suppress the 2nd harmonic by negative feedback [54]. To complement the feedback method, this chapter describes a feed-forward method from insights offered by harmonic function analysis. It also shows that in reducing the 2nd harmonic circulating current, the MMC is cleansed of other low-order harmonics.

This chapter makes use of the mathematical formulas of Table 3-II and Table 3-III to identify the origin of low-order harmonic proliferation. In Chapter 3, single-phase ac power is assumed to produce an unknown 2nd harmonic current $i_{2\omega}(t)=X\cos(2\omega t+\varphi_2)$ of (3-18). In Table 3-II and Table 3-III, one sees that 'X' is proliferated in all the columns. It is to be noted that all entries are voltages. Therefore, one has to locate and design a voltage which cancels the source of $i_{2\omega}$. This voltage can only be generated from the reference signal similar to $u_{ref}(t)$ of (3-8) of the modulation signal of (3-9) and (3-27). Since the voltage to be cancelled is a 2nd harmonic voltage, a signal additional to $u_{ref}(t)$ is proposed which takes the form $u_{add}(t)=Y\cos(2\omega t+\gamma)$. In including the supplementary signal, the derivation of Table 3-II and Table 3-III is repeated and the additional terms due

to $u_{add}(t)$ are put in Table 4-I and Table 4-II. In Table 4-II, $u_{add}(t)=Y\cos(2\omega t+\gamma)$ appears as voltage term. This term can be applied to implement feed-forward and/or feedback.

In Section 4.2, the origin of 2nd harmonic circulating current is derived together with the analytical expression of 2nd harmonic circulating current. Section 4.3 presents the analysis of modification of the modulating signal by a second harmonic supplementary signal. The supplementary signal can be from feed-forward or feedback to eliminate the 2nd harmonic circulating current. Section 4.4 presents results of simulation tests which validate the feed-forward method under steady-state and dynamic operation. Conclusions are presented in Section 4.5.

4.2 2nd Harmonic Circulating Current Origin and Its Analytical Expression

Section 3.2.1 highlights the magnitude of 2nd harmonic circulating current of (3-18) with '*X*' so that its presence in the dc, fundamental, 2nd and 3rd harmonic columns in Table 3-II and Table 3-III is easily spotted. This section continues harmonic function analysis in one phase with focus on double frequency terms in Table 3-III. It is noted that '*X*' does not appear in voltage terms $T_{3\text{-}2\omega\text{-}ii}$, $T_{5\text{-}2\omega}$ and $T_{8\text{-}2\omega\text{-}i}$, which means that they are not coming from 2nd harmonic circulating current. Thus, these three voltage terms are considered as the forcing voltage of 2nd harmonic circulating current, or in other words, the origin of 2nd harmonic circulating current. On the dc side, $T_{3\text{-}2\omega\text{-}ii}$, $T_{5\text{-}2\omega}$ and $T_{8\text{-}2\omega\text{-}i}$ sum to:

$$\begin{aligned} u_{Force-2\omega}(t) &= 2T_{3-\omega-ii} + 2T_{5-2\omega} + 2T_{8-2\omega-i} \\ &= \frac{NU_{ref}^2 I_d}{\omega C U_{dc}^2}\sin(2\omega t + 2\delta) - \frac{3NU_{ref} I_{ac}}{8\omega C U_{dc}}\sin(2\omega t + \delta + \varphi_{ac}) \end{aligned} \tag{4-1}$$

where $u_{Force\text{-}2\omega}(t)$ is the forcing voltage of the 2nd harmonic circulating current of (3-18).

The non-source second harmonic terms, bearing '*X*' in Table 3-III, sum to:

$$u_{2\omega C}(t) = 2\left[\frac{N}{3\omega C}\frac{U_{ref}^2}{U_{dc}^2} + \frac{N}{8\omega C}\right] X\sin(2\omega t + \varphi_2) \tag{4-2}$$

Applying KVL around the equivalent circuit of Fig. 3- 2 (c) and applying the Principle of Superposition so that the 2nd harmonic can be treated in isolation.

$$
\begin{aligned}
&u_{Force-2\omega}(t)+u_{2\omega C}(t)+2R_0 i_{2\omega}(t)+2L_0\frac{di_{2\omega}(t)}{dt}\\
&=u_{Force-2\omega}(t)+(\frac{2N}{3\omega C}\frac{U_{ref}^2}{U_{dc}^2}+\frac{N}{4\omega C})i_{2\omega}(t)+2R_0 i_{2\omega}(t)+2L_0\frac{di_{2\omega}(t)}{dt}=0
\end{aligned}
\tag{4-3}
$$

Substituting (4-1), (4-2) and (3-18) into (4-3),

$$
\begin{aligned}
&\frac{3U_{ref}I_{ac}}{2U_{dc}}\sin(2\omega t+\delta+\varphi_{ac})-\frac{4U_{ref}^2 I_d}{U_{dc}^2}\sin(2\omega t+2\delta)\\
&=\left[1+\frac{8U_{ref}^2}{3U_{dc}^2}-\frac{16\omega^2 L_0 C}{N}\right]X\sin(2\omega t+\varphi_2)+\frac{8R_0\omega C}{N}X\cos(2\omega t+\varphi_2)
\end{aligned}
\tag{4-4}
$$

Equation (4-4) enables 'X' to be solved. Because 'X' is undesirable and will be eliminated, readers may wish to stride past equations from (4-5) to (4-9). In case they will be needed, the analytical expression of 'X' can be derived by following the steps below:

$$
\begin{cases}
a\sin(2\omega t+\delta+\varphi_{ac})-b\sin(2\omega t+2\delta)=X\sin(2\omega t+\varphi_2+\eta)\\
a=\dfrac{1}{\sqrt{A^2+B^2}}\dfrac{3U_{ref}I_{ac}}{2U_{dc}}\\
b=\dfrac{1}{\sqrt{A^2+B^2}}\dfrac{4U_{ref}^2 I_d}{U_{dc}^2}\\
A=1+\dfrac{8U_{ref}^2}{3U_{dc}^2}-\dfrac{16\omega^2 L_0 C}{N}\\
B=\dfrac{8R_0\omega C}{N}\\
\eta=\cos^{-1}(\dfrac{A}{\sqrt{A^2+B^2}})
\end{cases}
\tag{4-5}
$$

Fig. 4-1 shows the phasor diagram of 2nd harmonic in steady state operation. This is by writing (4-5) as $X\sin(2\omega t+\varphi+\eta)$=Real{-j $\tilde{X}\ e^{j2\omega t}$ }, where

$$\tilde{X}=Xe^{j(\varphi_2+\eta)} \tag{4-6}$$

According to Law of cosines and MMC steady state power balance equation (3-36):

$$
\begin{aligned}
X&=\sqrt{a^2+b^2-2ab\cos(\varphi)}\\
&=\frac{1}{\sqrt{A^2+B^2}}\frac{3U_{ref}I_{ac}}{2U_{dc}}\sqrt{1+\frac{16U_{ref}^4\cos^2(\varphi)}{9U_{dc}^4}-\frac{8U_{ref}^2\cos^2(\varphi)}{3U_{dc}^2}}
\end{aligned}
\tag{4-7}
$$

where $\varphi=\delta-\varphi_{ac}$ is the phase angle between current i_{ac} and voltage u_{ref}. It shows that the magnitude of 2nd harmonic circulating current is in proportion to the magnitude of ac current when MMC runs at constant power factor. Moreover, when power factor is the only variable, '*X*' reaches its minimum value at $cos\varphi=1$ (MMC does not generate or absorb reactive power).

In equation (4-5), it is noted that '*A*' may become zero for certain value of L_0C at fundamental frequency ω. In this case, the magnitude of 2nd harmonic circulating current '*X*' reaches its peak value and is mainly limited by resistance R_0 which is quite small so as to achieve high efficiency of the converter. Therefore, in order to avoid relying heavily on resistance R_0, the value of L_0C should be chosen as:

$$L_0C \neq \frac{N}{16\omega^2}\left(1+\frac{8U_{ref}^2}{3U_{dc}^2}\right) \tag{4-8}$$

Since arm inductor L_0 is good for limiting fault current and relatively large SM capacitor can relieve the voltage pressure on switches, the SM capacitor and arm inductor are assigned with the constraint:

$$L_0C > \frac{N}{16\omega^2}\left(1+\frac{8U_{ref}^2}{3U_{dc}^2}\right) \tag{4-9}$$

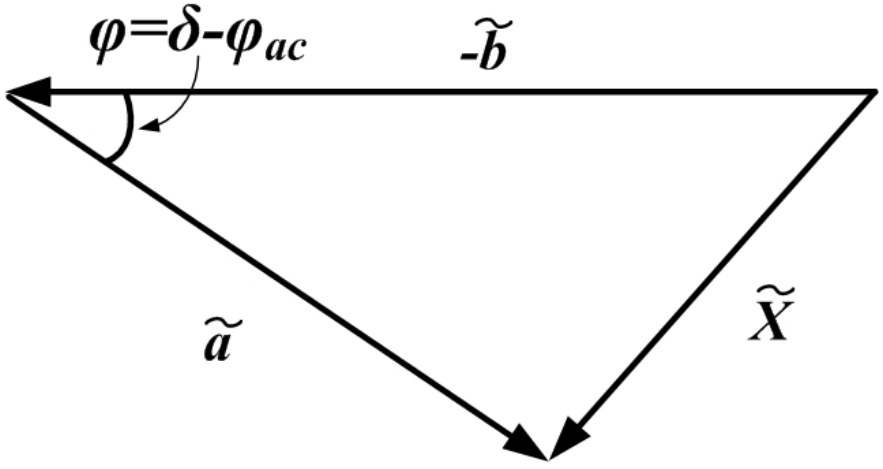


Fig. 4-1 Phasor diagram of 2nd harmonic (not to scale)

4.3 2nd Harmonic Circulating Current Elimination

The 2nd harmonic circulating current elimination method is based on inserting a 2nd harmonic voltage u_{insert}, so that (4-3) becomes:

$$\left[u_{insert}(t)+u_{Force-2\omega}(t)\right]+\left(\frac{2N}{3\omega C}\frac{U_{ref}^2}{U_{dc}^2}+\frac{N}{4\omega C}\right)i_{2\omega}(t) + (2R_0+R_{dc})i_{2\omega}(t)+2L_0\frac{di_{2\omega}(t)}{dt}=0 \tag{4-10}$$

when

$$u_{insert}(t)+u_{Force-2\omega}(t)=0 \tag{4-11}$$

'X' of $i_{2\omega}$ in (4-10) becomes zero.

Since u_{insert} has to be a second harmonic voltage, the proposed elimination signal is:

$$u_{add}(t)=Y\cos(2\omega t+\gamma) \tag{4-12}$$

which is added to the modulation signals of (3-9) and (3-27) of the upper and lower arm respectively. Y denotes the magnitude of u_{add} and γ is its angular displacement.

4.3.1 Modification of Modulation by Feed-forward Signal

Since the components of $u_{Force\text{-}2\omega}$ come from the voltages in Table 3-III of Chapter 3, u_{add} must come from a similar voltage component from a modulating signal component.

A. Upper Arm

By adding u_{add} of (4-12) to the modulating signal of (3-9), the number of switched capacitors in the upper arm is modified from (3-10) to

$$n_u(t)'=N\left[\frac{1}{2}-\frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta)+\frac{Y}{U_{dc}}\cos(2\omega t+\gamma)\right] \tag{4-13}$$

where superscript ' represents signal after modification.

So as to reduce bookkeeping, $i_{2\omega}$ of (3-18) is set as zero. Thus (3-19) is changed to

$$\frac{du^N{}_u(t)'}{dt}=\frac{N}{C}\left[\frac{1}{2}-\frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta)+\frac{Y}{U_{dc}}\cos(2\omega t+\gamma)\right]\cdot\left[\frac{I_{ac}}{2}\cos(\omega t+\varphi_{ac})+I_d\right] \tag{4-14}$$

On integrating (4-14),

$$u^N{}_u(t)'=2T_1+2T_2+2T_3+2T_4+2T_A+2T_B \tag{4-15}$$

where two new voltage component T_A and T_B arise from the term $Ycos(2\omega t+\gamma)/U_{dc}$ in (4-14).

Following from (3-25)

$$\begin{aligned} u_{upper}(t)' &= n_u(t)'\frac{u^N{}_u(t)'}{N} \\ &= \left[\frac{1}{2}-\frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta)+\frac{Y}{U_{dc}}\cos(2\omega t+\gamma)\right]\cdot 2\left(T_1+T_2+T_3+T_4+T_A+T_B\right) \\ &= T_1+T_2+T_3+T_4+T_5+T_6+T_7+T_8 \\ &\quad +T_A+T_B+T_C+T_D+T_E+T_F+T_G+T_H+T_I+T_J \end{aligned} \tag{4-16}$$

The terms T_1, T_2 …T_8 are not changed except that all terms with 'X' become zeroes. Aside from T_A and T_B, there are 8 new terms:

$$T_C+T_D=-\frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta)\cdot 2(T_A+T_B) \tag{4-17}$$

$$T_E+T_F+T_G+T_H+T_I+T_J=\frac{Y}{U_{dc}}\cos(2\omega t+\gamma)\cdot 2\left(T_1+T_2+T_3+T_4+T_A+T_B\right) \tag{4-18}$$

B. Lower Arm

The number of switched capacitors in the lower arm is

$$n_l(t)'=N\left[\frac{1}{2}+\frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta)+\frac{Y}{U_{dc}}\cos(2\omega t+\gamma)\right] \tag{4-19}$$

Following the same development of the upper arm

$$\begin{aligned} u_{lower}(t)' &= n_l(t)'\frac{u^N{}_l(t)'}{N} \\ &= \left[\frac{1}{2}+\frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta)+\frac{Y}{U_{dc}}\cos(2\omega t+\gamma)\right]\cdot 2\left(T_1+T_2+T_3+T_4+T_A+T_B\right) \\ &= -T_1+T_2+T_3-T_4+T_5-T_6-T_7+T_8 \\ &\quad +T_A-T_B-T_C+T_D-T_E+T_F+T_G-T_H+T_I-T_J \end{aligned} \tag{4-20}$$

The formulas of T_A, T_B, ...T_J are listed in Table 4-I and Table 4-II.

C. AC-Side Equivalent Circuit

The voltage components on the ac-side are:

$$u_{ac-side}(t)' = \frac{1}{2}\left[u_{lower}(t)' - u_{upper}(t)'\right] = -(T_1 + T_4 + T_6 + T_7) - (T_B + T_C + T_E + T_H + T_J) \quad (4\text{-}21)$$

D. DC-Side Equivalent Circuit

The voltage components on the dc-side are

$$u_{dc-side}(t)' = u_{upper}(t)' + u_{lower}(t)' = 2(T_2 + T_3 + T_5 + T_8) + 2(T_A + T_D + T_F + T_G + T_I) \quad (4\text{-}22)$$

The equivalent circuits are similar to Fig. 3- 2 (b) and (c) except that the voltage terms with Roman subscripts are added as required by (4-21) and (4-22).

Table 4-I AC-side equivalent voltage components after modulating signal modification

	ω	3ω
T_B	$\frac{NYI_{ac}}{8\omega CU_{dc}}\sin(\omega t + \gamma - \varphi_{ac})$	$\frac{NYI_{ac}}{24\omega CU_{dc}}\sin(3\omega t + \gamma + \varphi_{ac})$
T_C	$-\frac{NU_{ref}YI_d}{4\omega CU_{dc}^2}\sin(\omega t + \gamma - \delta)$	$-\frac{NU_{ref}YI_d}{4\omega CU_{dc}^2}\sin(3\omega t + \gamma + \delta)$
T_E	$-\frac{NYI_{ac}}{8\omega CU_{dc}}\sin(\omega t + \gamma - \varphi_{ac})$	$\frac{NYI_{ac}}{8\omega CU_{dc}}\sin(3\omega t + \varphi_{ac} + \gamma)$
T_H	$\frac{NU_{ref}YI_d}{2\omega CU_{dc}^2}\sin(\omega t + \gamma - \delta)$	$-\frac{NU_{ref}YI_d}{2\omega CU_{dc}^2}\sin(3\omega t + \gamma + \delta)$
T_J	$-\frac{NY^2I_{ac}}{12\omega CU_{dc}^2}\sin(\omega t + \varphi_{ac})$	$\frac{NY^2I_{ac}}{8\omega CU_{dc}^2}\sin(3\omega t + 2\gamma - \varphi_{ac})$

Table 4-II DC-side equivalent voltage components after modulating signal modification

	dc	*2ω*
T_A	--	$\frac{NYI_d}{4\omega CU_{dc}}\sin\left(2\omega t+\gamma\right)$
T_D	$-\frac{NU_{ref}YI_{ac}}{8\omega CU_{dc}^2}\sin\left(\gamma-\varphi_{ac}-\delta\right)$	$-\frac{NU_{ref}YI_{ac}}{24\omega CU_{dc}^2}\sin\left(2\omega t+\gamma+\varphi_{ac}-\delta\right)$ $-\frac{NU_{ref}YI_{ac}}{8\omega CU_{dc}^2}\sin\left(2\omega t+\gamma-\varphi_{ac}+\delta\right)$
T_F	--	$Y\cos\left(2\omega t+\gamma\right)$
T_G	$-\frac{NU_{ref}YI_{ac}}{16\omega CU_{dc}^2}\sin\left(\delta+\varphi_{ac}-\gamma\right)$	--
T_I	--	--

E. Relative Magnitudes of Voltage Terms

The voltage terms T_1, T_2, T_3 and T_4 in Table 3-II and Table 3-III, consist largely of voltage drops of kth harmonic currents across capacitive reactance ($N/k\omega C$). The magnitudes of T_5, T_6, T_7 and T_8 terms are modified by multiplication of U_{ref}/U_{dc} of (3-26).

In contrast, the voltages in Table 4-I and Table 4-II are smaller. Using '*Y*' of $T_{F\text{-}2\omega}$ as reference, the other terms are attenuated by (Y/U_{dc}), which is small. The terms with $(Y/U_{dc})^2$ are smaller still. Apart from '*Y*' of $T_{F\text{-}2\omega}$, the terms in Table 4-I and Table 4-II are small and therefore do not produce undesirable side-effects, as borne out by simulation results.

F. Insights from Harmonic Function Analysis

Interpreting the mathematical formulas in Table 3-II, Table 3-III, Table 4-I and Table 4-II allows the component interactions of MMC to be understood. Because each MMC arm is a single phase ac power, it has inherent 2nd harmonic power component. In (3-18), the 2nd harmonic circulating current has been highlighted by '*X*' to identify its contribution in spreading to other harmonics in the Tables. The strategy is to eliminate "*X*" at the

source by adding a modulation signal u_{add} which has been highlighted by '*Y*' for easy identification. After the low-order harmonics associated with '*X*' have been eliminated using the method described in Section 4.3.2, an equivalent circuit is presented of the MMC in Section 4.3.3. In the equivalent circuit, an ac voltage T_{ac} has a dc voltage counterpart T_{dc} through *average* power balance: $T_{ac}i_{ac} \Leftrightarrow T_{dc}I_d$. This is strong confirmation on the correctness of harmonic function analysis.

4.3.2 Designing Feed-forward Control to Eliminate 2nd Harmonic Circulating Current

A. Complete Elimination

The term "complete" is used here to distinguish it from Approximate Elimination in sub-section B. It is "complete" because $T_{A\text{-}2\omega}$, $T_{D\text{-}2\omega\text{-}i}$, $T_{D\text{-}2\omega\text{-}ii}$ in Table 4-II are included. But it is still not "exact" elimination because the method is based on a truncated infinite series. In order to eliminate the 2nd harmonic circulating current, the 2nd harmonic voltage terms in Table 3-III voltages must sum to zero as in (4-11):

$$(2T_{A-2\omega} + 2T_{D-2\omega-i} + 2T_{D-2\omega-ii} + 2T_{F-2\omega}) + u_{Force-2\omega}(t) = 0 \tag{4-23}$$

where

$$(2T_{A-2\omega} + 2T_{D-2\omega-i} + 2T_{D-2\omega-ii} + 2T_{F-2\omega}) = u_{insert}(t) \tag{4-24}$$

One solves (4-23) in terms of a phasor of $e^{j2\omega t}$. This is by writing (4-12) as u_{add}=Real{ $\tilde{Y}$ $e^{j2\omega t}$ }, where

$$\tilde{Y} = Ye^{j\gamma} \tag{4-25}$$

Converting $u_{Force\text{-}2\omega}$ as a phasor

$$\tilde{U}_{Force-2\omega} = -j\left[\frac{NU_{ref}^2 I_d}{\omega CU_{dc}^2}e^{j2\delta} - \frac{3NU_{ref}I_{ac}}{8\omega CU_{dc}}e^{j(\delta+\varphi_{ac})}\right] \tag{4-26}$$

Converting ($T_{A\text{-}2\omega} + T_{D\text{-}2\omega\text{-}i} + T_{D\text{-}2\omega\text{-}ii} + T_{F\text{-}2\omega}$) as phasors, one has

$$\begin{aligned}\tilde{Y}\tilde{D} &= \tilde{Y}\left\{2 - j\left[\frac{NI_d}{2\omega CU_{dc}} - \frac{NU_{ref}I_{ac}}{12\omega CU_{dc}^2}e^{j(\varphi_{ac}-\delta)} - \frac{NU_{ref}I_{ac}}{4\omega CU_{dc}^2}e^{j(\delta-\varphi_{ac})}\right]\right\} \\ &= \tilde{U}_{insert}\end{aligned} \tag{4-27}$$

Adding (4-26) to (4-27) to form (4-23) as a phasor equation, the solution is

$$\tilde{Y} = \frac{-\tilde{U}_{Force-2\omega}}{\tilde{D}} \tag{4-28}$$

Therefore u_{add} of (4-12) has the solution:

$$u_{add}(t) = \mathrm{Re}\,al\left[\tilde{Y}e^{j2\omega t}\right] \tag{4-29}$$

Equations (4-24)-(4-29) show how the "complete" 2nd harmonic elimination by (4-23) is carried out.

B. Approximate Elimination

Approximate elimination consists of omitting $T_{A\text{-}2\omega}$, $T_{D\text{-}2\omega\text{-}i}$, $T_{D\text{-}2\omega\text{-}ii}$ in (4-23) leaving $T_{F\text{-}2\omega}$ so that (4-11) is approximated as:

$$u_{insert}(t) = 2T_{F-2\omega} = 2Y\cos(2\omega t + \gamma) = -u_{Force-2\omega}(t) \tag{4-30}$$

Substituting (4-1) to (4-30),

$$\begin{aligned} u_{insert}(t) &= 2Y\cos(2\omega t + \gamma) \\ &= -\frac{NU_{ref}^2 I_d}{\omega C U_{dc}^2}\sin(2\omega t + 2\delta) + \frac{3NU_{ref} I_{ac}}{8\omega C U_{dc}}\sin(2\omega t + \delta + \varphi_{ac}) \\ &= 2u_{add}(t) \end{aligned} \tag{4-31}$$

The block diagram in Fig. 4-2 shows how $u_{add}(t)$ of (4-31) is incorporated in the modulating signals $m_u(t)$ of (3-9) and m_l(t) of (3-27). From ωt (obtained from phase locked loop PLL) to which δ (voltage angle of reference) is added, the function generators "sin" and "cos" produce $sin(\omega t+\delta)$ and $cos(\omega t+\delta)$. The magnitude control U_{ref} is multiplied to $cos(\omega t+\delta)$ to form u_{ref} of MMC ac voltage references of (3-9) and (3-27).

The 2nd harmonic circulating current elimination signal u_{add} of (4-31) is inserted in the modulating signals to produce $n_u(t)$' of (4-13) and $n_l(t)$' (4-19). The signal u_{add} requires the formation of $sin(2\omega t+2\delta)$ and $sin(2\omega t+\delta+\varphi_{ac})$. Multiplying $2sin(\omega t+\delta)$ to $cos(\omega t+\delta)$ yields $sin(2\omega t+2\delta)$. This function, suitably scaled by I_d, produces the first right term of (4-31).

Multiplying $2sin(\omega t+\delta)$ to the measurement of the ac current of (3-15), yields $I_{ac}cos(2\omega t+\delta+\varphi_{ac})$ and a dc term which is filtered. The double frequency remainder is multiplied by the coefficients of the second right term of (4-31). The *feed-forward* implementation in Fig. 4-2 is referred to as the "approximate" method.

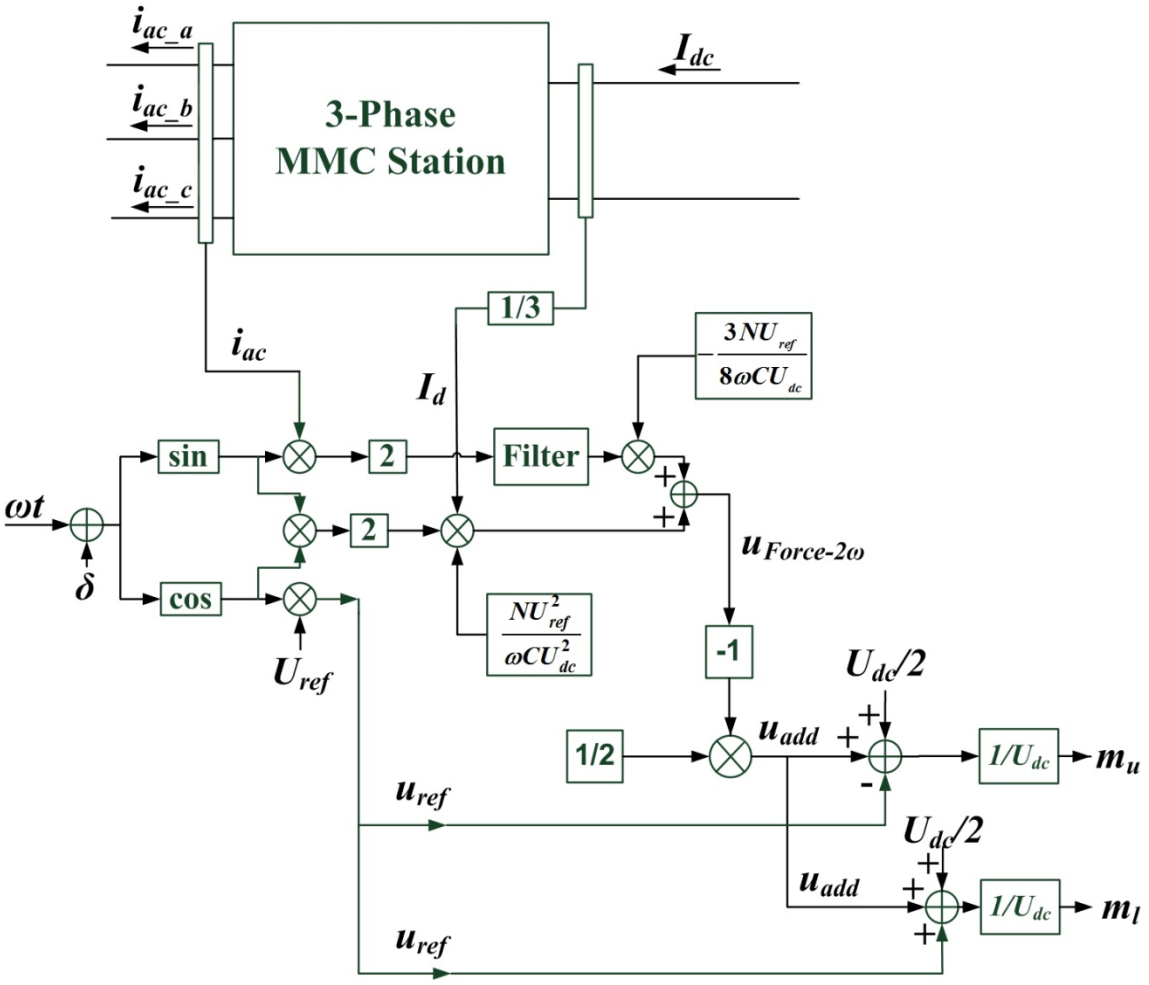


Fig. 4-2 Block diagram of modulating signal with *feed-forward elimination method*

Section 4.4.2 describes the simulation results based on "complete 2nd harmonic elimination" and "approximate 2nd harmonic elimination". Because the "*complete method*" the and the "*approximate method*" of Fig. 4-2 reduces the 2nd harmonic circulating current by a factor of 0.0196 and 0.0311 respectively shown in Table 4-IV, the "*approximate method*" of Fig. 4-2 is considered adequate.

4.3.3 Equivalent Circuit and Phasor Diagram after 2nd Harmonic Elimination

Fig. 4-3 shows the composite voltage and current phasor diagram and the composite equivalent of an MMC arm connected to the ac-side of Fig. 3- 2 (b) and the dc-side of Fig. 3- 2 (c). Fig. 4-3 is constructed from Table 3-II, Table 3-III, Table 4-I and Table 4-II after '*X*' components have been eliminated and only the dc and fundamental frequency columns

remain. Scaling is not followed in the phasor diagram to enable small voltage phasors such as T_4 and T_{C+H} to be represented clearly.

Counterpart Voltages from Power Balance

In the MMC equivalent circuit, an ac voltage T_{ac} can have a dc voltage counterpart T_{dc} through *average* power balance: $T_{ac}i_{ac} \Leftrightarrow T_{dc}I_d$. Fig. 4-3 places T_{ac} right above its dc counterpart T_{dc}.

Dominant MMC Voltages on AC and DC-sides

The dominant dc-side voltage is $U_{dc}=2T_2$. The magnitude of T_2 is determined by the power balance within the integral symbol. The ac voltage $-T_6$ bears the same integral as the dc-voltage T_2. Ones sees that it is the ac reference signal of (3-8) amplified by U_{dc}.

AC Voltage from I_d

$T_{4\text{-}\omega}$ lags $-T_6$ by 90°. Its counterpart is T_5. Unlike T_6, T_4 is not amplified by U_{dc}. Substituting numerical values in Table 4-III, T_5 is a small voltage of hundreds of volts compared to 27 kV of $-T_6$.

Capacitive Reactance Voltage

T_1+T_7 forms a capacitive reactance voltage in series with the inductive reactance of $\omega(L_{ac}+0.5L_0)$. As T_1 comes from the residual line frequency voltage in SM capacitor, it cannot be large without increasing the voltage rating of the IGBTs in the SMs. As reactive voltages, T_1 and T_7 have no dc counterparts.

Modulation Modification

In the fundamental frequency column of Table 4-I, u_{add} affects

$$T_{C+H} = T_{C-\omega} + T_{H-\omega} = \frac{NU_{ref}YI_d}{4\omega CU_{dc}^2}\sin(\omega t + \gamma - \delta) \tag{4-32}$$

This is because as

$$T_{B-\omega} + T_{E-\omega} = 0 \tag{4-33}$$

In the dc column in Table 4-II

$$2T_{D+G} = 2T_{D-\omega} + 2T_{G-\omega} = -\frac{NU_{ref}YI_{ac}}{8\omega CU_{dc}^2}\sin(\gamma - \varphi_{ac} - \delta) \tag{4-34}$$

Because it is a second order term in Y, $T_{G\text{-}dc}$ has been omitted. From (4-33) and (4-34), T_{C+H} is a counterpart of $2T_{D+G}$. Both voltages are negligibly small.

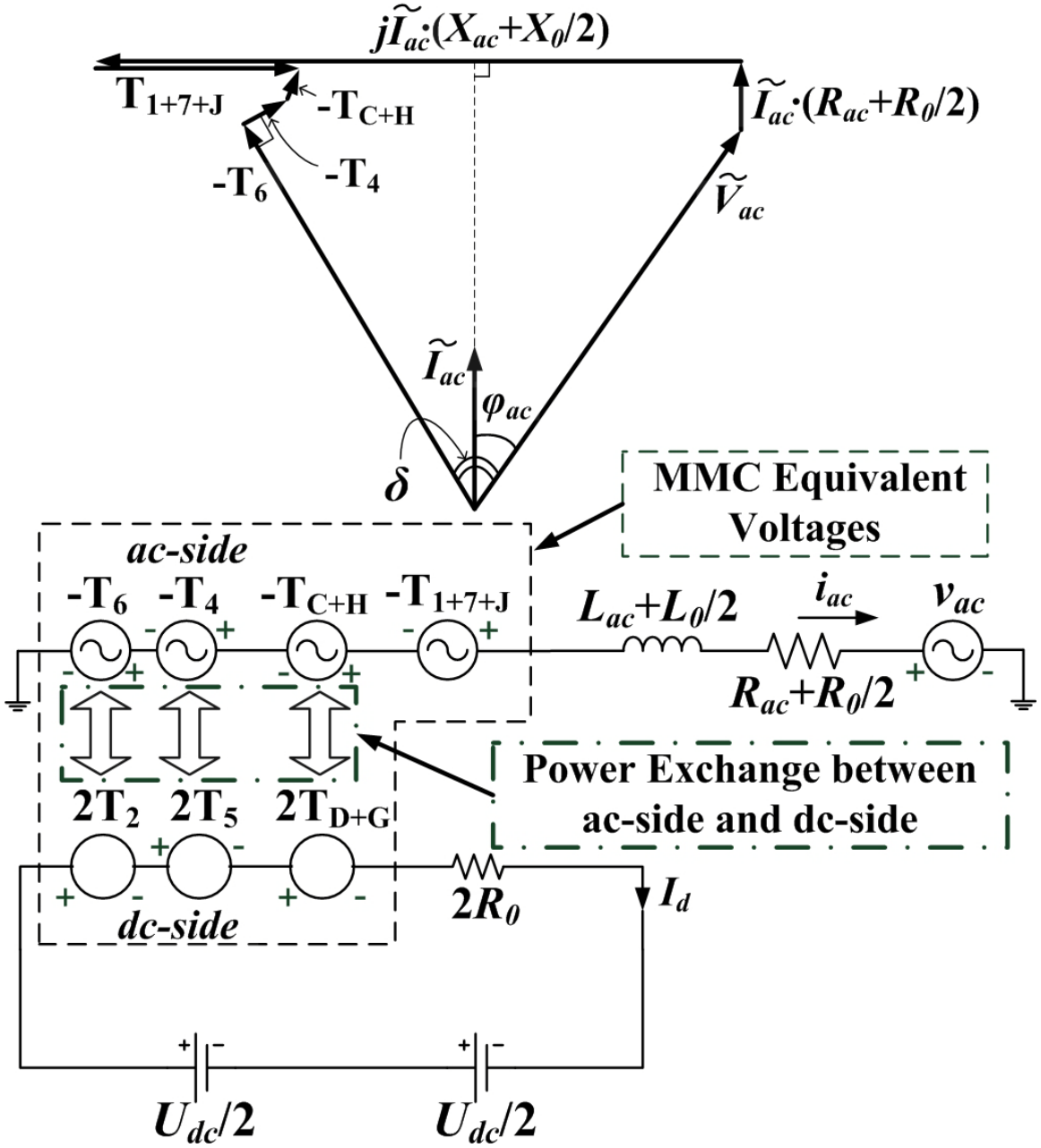


Fig. 4-3 Composite voltage and current phasor diagram (not to scale). Composite functional equivalent circuit of ac-side and dc-side connected by MMC

4.4 Simulation Results

The MMC model of Fig. 2-1 (a) is simulated by the Simulink/MATLAB. In the simulations, Phase shifted carrier PWM (PSC-PWM) technique converts the modulation signals $m_u(t)$ and $m_l(t)$ to the number of capacitors $n_u(t)$ and $n_l(t)$ respectively in series.

Table 4-III Parameters used in the 3-phase MMC simulation

Items	Values	Items	Values
MMC Nominal Power S_b	50 MVA	AC System Nominal Voltage V_b	35 kV (Vrms phase-phase)
DC Bus Voltage U_{dc}	60 kV	Reference Voltage Magnitude U_{ref}	27 kV
Number of SMs per Arm N	12	Frequency f	50 Hz
SM Capacitance C	10 mF	AC System Voltage v_{ac}	25 kV (peak value)
Arm Inductance L_0	3 mH	AC System Inductance L_{ac}	10 mH
Arm Equivalent Resistance R_0	0.3 Ω	AC System Resistance R_{ac}	0.5 Ω

Individual capacitor voltages are balanced by using a sorting algorithm from [44]. The parameters of the main circuit are shown in Table 4-III.

4.4.1 Validation of 2nd Harmonic Circulating Current Analytical Expression

The analytical expression (4-7) implies that there is a L_0C resonant value which renders the peak magnitude of 2nd harmonic circulating current. When using parameters in Table 4-III, referring to (4-9), L_0C resonant value at fundamental frequency (f=50 Hz) is

$$\frac{N}{16\omega^2}\left(1+\frac{8U_{ref}^2}{3U_{dc}^2}\right)=11.7026\times10^{-6} \tag{4-35}$$

With arm inductance L_0=0.003 H, the peak value of 2nd harmonic circulating current is expected to appear when SM capacitance is 0.0039 F. To verify this, pure resistance load is employed in the simulation. Varying the capacitance from 2mF to 20mF, the magnitude of 2nd harmonic circulating current is shown in Fig. 4-4. The expected peak is around 3.9mF, which coincides with the analytical expression analysis.

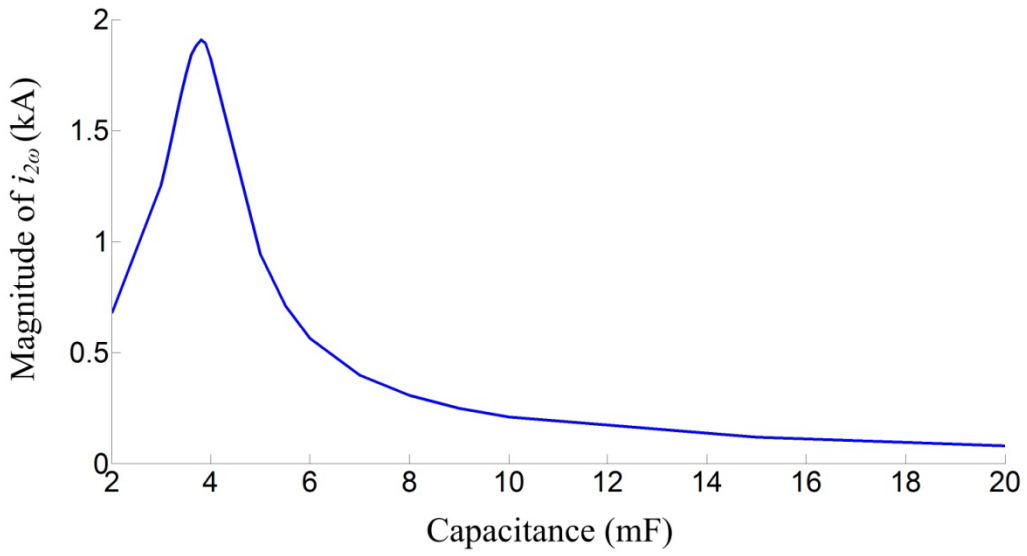


Fig. 4-4 Magnitude of 2nd harmonic circulating current versus SM capacitance

4.4.2 2nd Harmonic Circulating Current Elimination

A. Comparison of Complete Elimination and Approximate Elimination

In the test, all the parameters used are listed in Table 4-III except that the SM capacitor is set with a low value, *C=5* mF. Simulation results shown in Fig. 4-5 and Fig. 4-6 suggest that 2nd harmonic circulating current can be significantly reduced by both complete and approximate elimination methods. Since it is difficult to distinguish the results with naked eyes, Fast Fourier Transform (FFT) analysis of 2nd harmonic circulating current waveforms is conducted and the result is shown in Table 4-IV. It is noted that reduction with 'complete' and 'approximate' is by a factor of 0.0196 and 0.0311 respectively.

As the approximate elimination method is, from performance, as good as the complete elimination method while reducing computation complexity, it is better for potential application. Hereinafter, the 2nd harmonic circulating current elimination method (feed-forward elimination) refers to the approximate method.

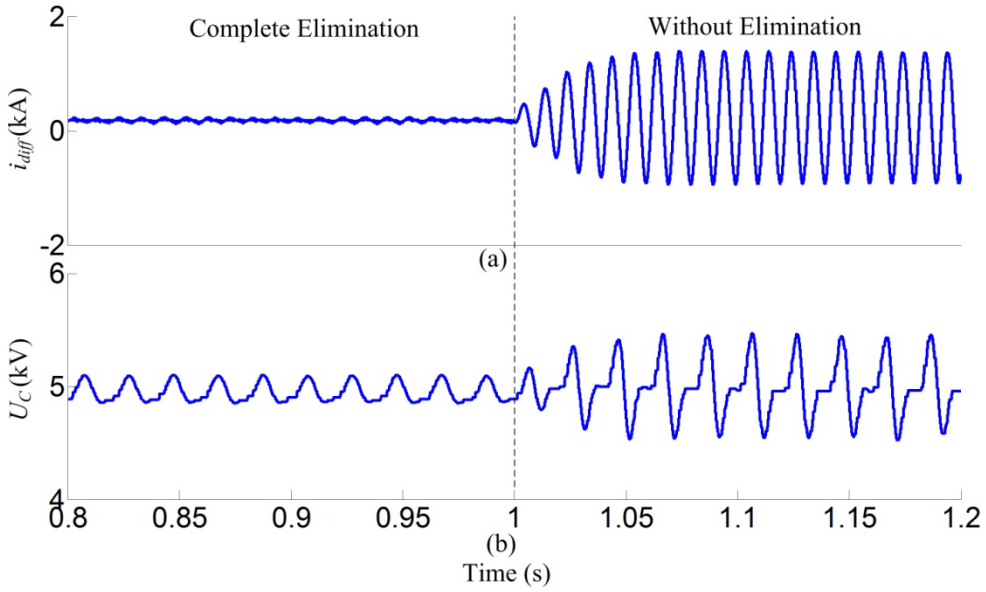


Fig. 4-5 Simulation results from complete elimination method. (a) diffential mode current i_{diff}; (b) one SM capacitor voltage

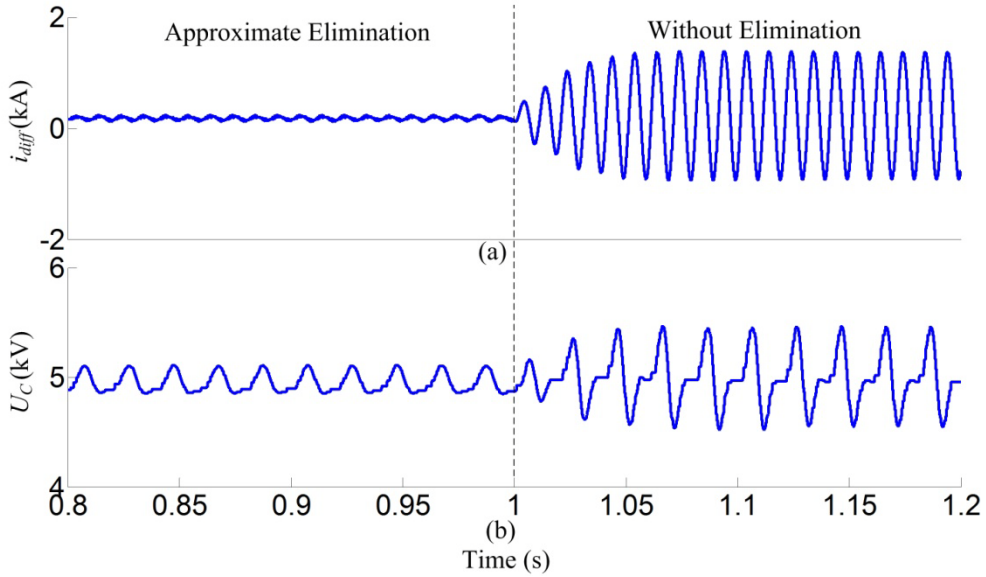


Fig. 4-6 Simulation results from approximate elimination method. (a) differential mode current i_{diff}; (b) one SM capacitor voltage

Table 4-IV FFT measurements of 2nd harmonic circulating current

	Without Elimination	Complete Elimination	Approximate Elimination
$i_{2\omega}$ (Normalized)	1	0.0196	0.0311

B. Test of Feed-forward Elimination under Steady-State Operation

In the test, in order to show the 3rd harmonic reduction, the transformers on ac side are wye-connected with grounded neutral to allow the flow of 3rd harmonic current. The test results in Fig. 4-7 consist of two graphs from predictions of harmonic function analysis and from simulations of the software model of Fig. 2-1 (a) by Simulink/MATLAB. The overlapping waveforms demonstrate the correctness of function analysis 'before' and 'after' 2nd harmonic circulating current elimination.

For $t > 0.5$ s after the activation of the feed-forward control in Fig. 4-2, the 3rd harmonic in the ac current in Fig. 4-7 (a), the 2nd harmonic in $i_{diff}(t)$ in Fig. 4-7 (b), and the harmonics in individual capacitor voltages $U_c(t)$ in Fig. 4-7 (c) are significantly reduced.

B-1. 3rd Harmonic Current Reduction

After 2nd harmonic circulating current is eliminated, 3rd harmonic current on the ac side has been reduced from 7.72% to 0.87% as shown in the histogram of FFT in Fig. 4-8. The residual 3rd harmonic current is coming from 'non-*X*' term $T_{7\text{-}3\omega\text{-}ii}$ in Table 3-II. The Total Harmonic Distortion (THD) of the ac current is reduced from 7.77 % to 0.91%.

B-2. Sub-Module Capacitor Voltage

The histogram of Fig. 4-9 compares the FFT analysis of the capacitor voltages of Fig. 4-7 (c) *before* and *after* activation of feed-forward elimination. For comparison, 1.0 pu is assigned to the fundamental frequency voltage component *after* 2nd harmonic circulating current elimination. From (3-20), the capacitor voltage is due to voltage components of T_1, T_2, T_3 and T_4. In Table 3-II, '*X*' is present in the fundamental frequency term $T_{4\text{-}\omega\text{-}ii}$, the 3rd harmonic term in $T_{4\text{-}3\omega}$. In Table 3-III, '*X*' is present in the 2nd harmonic terms $T_{3\text{-}2\omega\text{-}ii}$. Fig. 4-9 shows that when '*X*' is eliminated, the "*after*" voltage components are the residual 'non-*X*' terms.

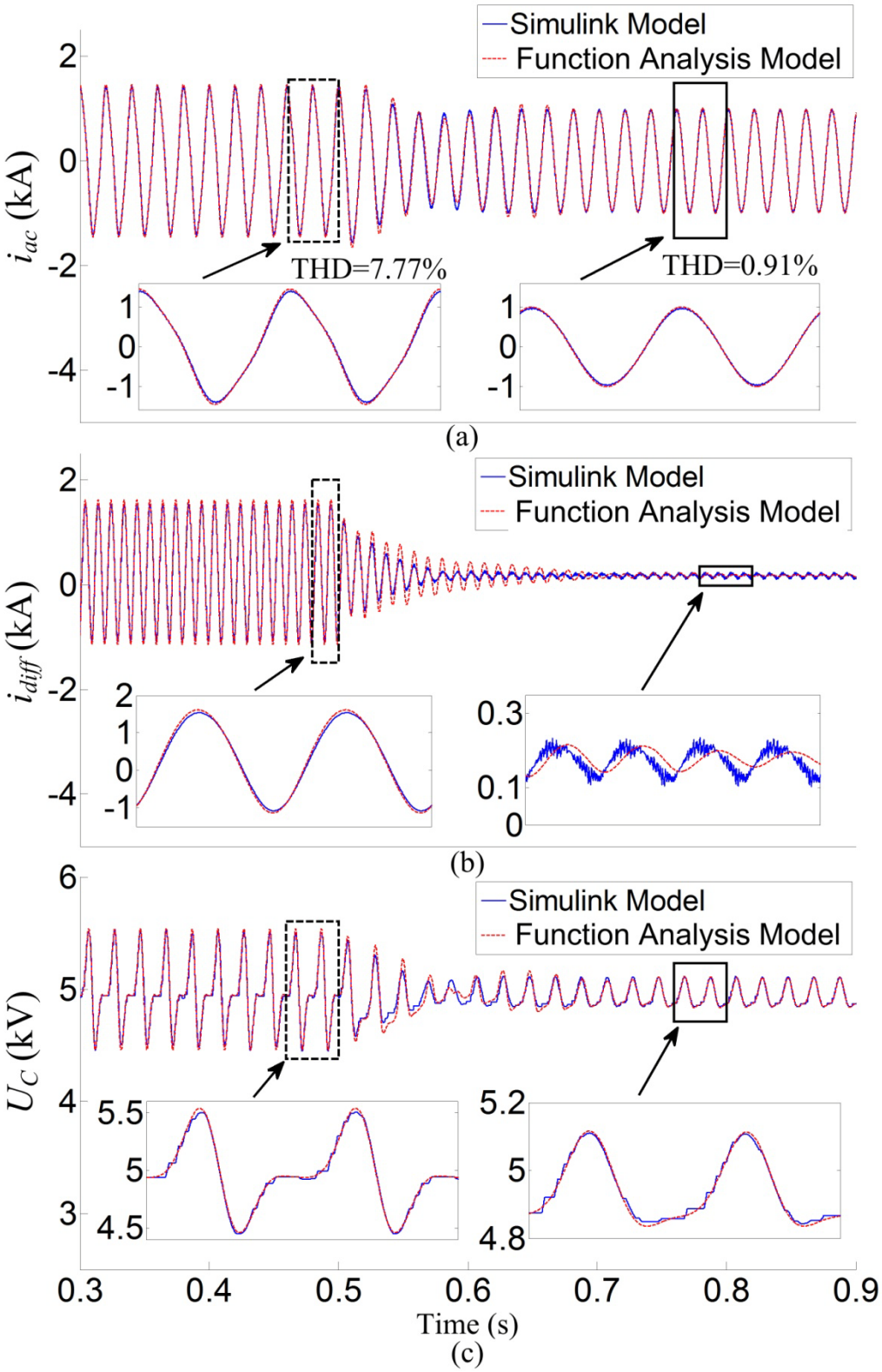


Fig. 4-7 Composite Simulation test results of 2nd harmonic elimination. (a) ac current of phase a; (b) differential mode current i_{diff} of phase a; (c) capacitor voltage of one sub-module of phase a, upper arm

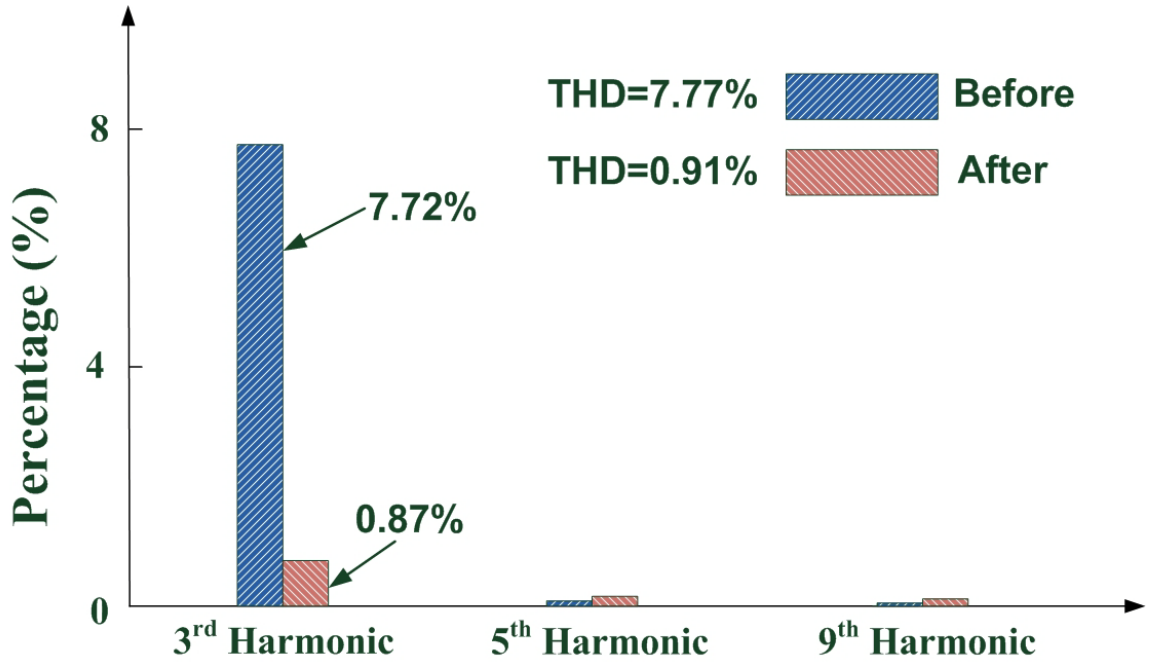


Fig. 4-8 Comparison FFT of 3rd harmonic current magnitude "before" and "after" 2nd harmonic circulating current elimination

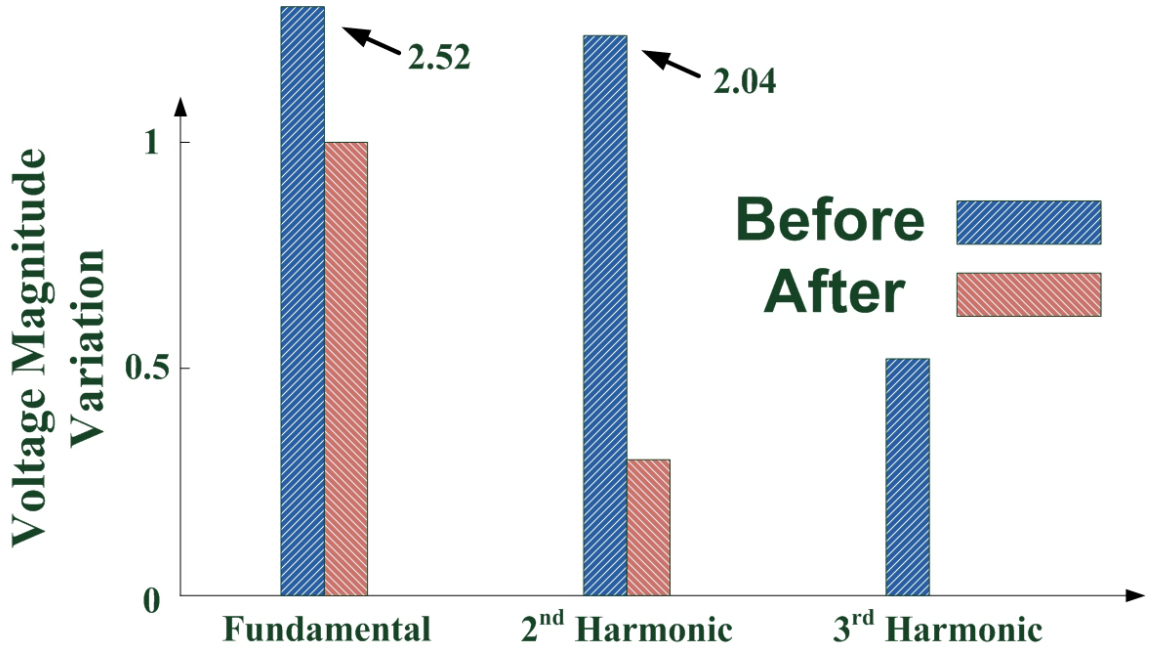


Fig. 4-9 Comparison FFT of capacitor voltage magnitude variation "before" and "after" 2nd harmonic circulating current elimination

C. Fundamental Harmonic Voltage Components

On eliminating '*X*' in the fundamental frequency column of Table 3-II, the remaining voltage components are $T_{1\text{-}\omega}$, $T_{4\text{-}\omega\text{-}i}$, $T_{6\text{-}\omega}$ and $T_{7\text{-}\omega\text{-}ii}$. The voltage $T_{6\text{-}\omega}$ is, in fact, the ac

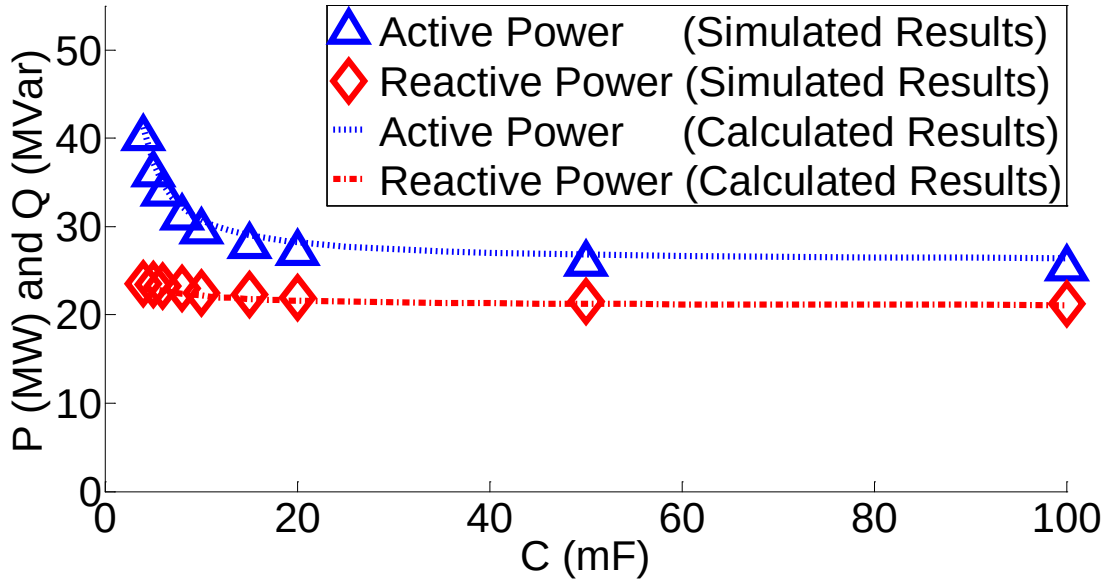


Fig. 4-10 Power Factor Correction: *P*-vs-*C* and *Q*-vs-*C* (L_{ac}+0.5L_0 =7.5 mH)

voltage output $U_{ref}cos(\omega t+\delta)$ of the MMC specified by the reference in the modulating signals of (3-9) and (3-27).

The voltage $T_{1\text{-}\omega}$ lags the ac current of (3-15) by 90 degrees and therefore can be considered as the voltage drop of the ac current flowing across the capacitors of the series connected sub-modules of Fig. 3- 1. On the ac side, $T_{1\text{-}\omega}$ and $T_{7\text{-}\omega\text{-}ii}$ contribute to series capacitive reactance compensation of the inductive reactance for power factor improvement. This is confirmed in the test results in Fig. 4-10.

C-1. Capacitive Reactance Compensation Test

Decreasing capacitance in Fig. 4-10 corresponds to increasing the size of $T_{1\text{-}\omega}$ and $T_{7\text{-}\omega\text{-}ii}$ or the equivalent capacitive reactance $-jX_C$ in the ac-side. On decreasing C, the total line reactance $j[\omega(L_{ac}+0.5L_0)-X_C]$ decreases so that the ac current increases in magnitude. The close agreement (3%) between simulated and calculated values validates the formulas in the Table 3-II. As C is reduced, P increases while Q remains roughly constant so that power factor is improved. Reduction of C requires higher cost IGBTs because they have to withstand higher peak voltages as illustrated in Fig. 4-7 (c).

D. Tests on Range of Elimination Capability (Steady-State)

The "before" and "after" curves in Fig. 4-11 and Fig. 4-12 validate the claim on feed-forward elimination as viewed in the domain of *modulation index* $2U_{ref}/U_{dc}$ and *angle* δ. Fig. 4-13 presents more validation tests as viewed in the domain of active power P and reactive power Q. Close agreement with simulation results validates the correctness of harmonic function analysis.

In order to verify the feed-forward elimination method thoroughly, one more set of test is conducted. This test is set to check the performance of feed-forward elimination with different number of SMs per arm. Referring to (4-9), the product of SM capacitance and arm inductance is in proportion to SM number per arm. Thus, SM capacitance is selected accordingly while keeping arm inductance as a constant. Simulation results are shown in Table 4-V, which displays the effectiveness of proposed elimination method.

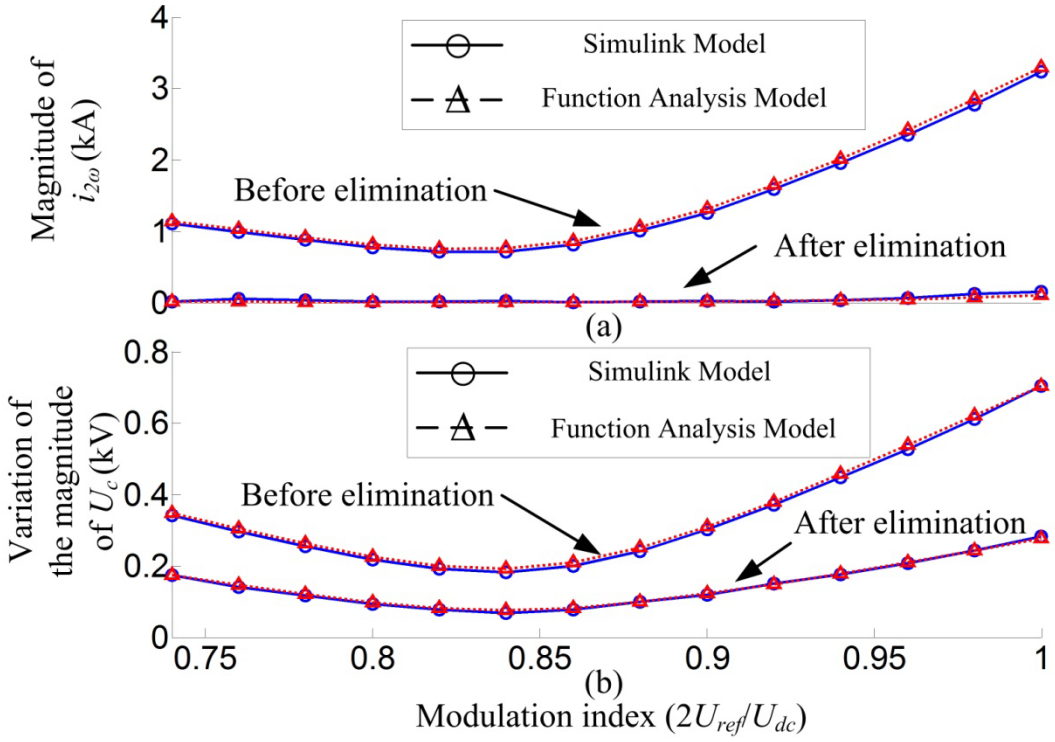


Fig. 4-11 Validation test results on feed-forward elimination method of Fig. 4-2. (a) Magnitude of 2nd harmonic circulating current and (b) Magnitude of capacitor voltage plotted as a function of modulation index $2U_{ref}/U_{dc}$

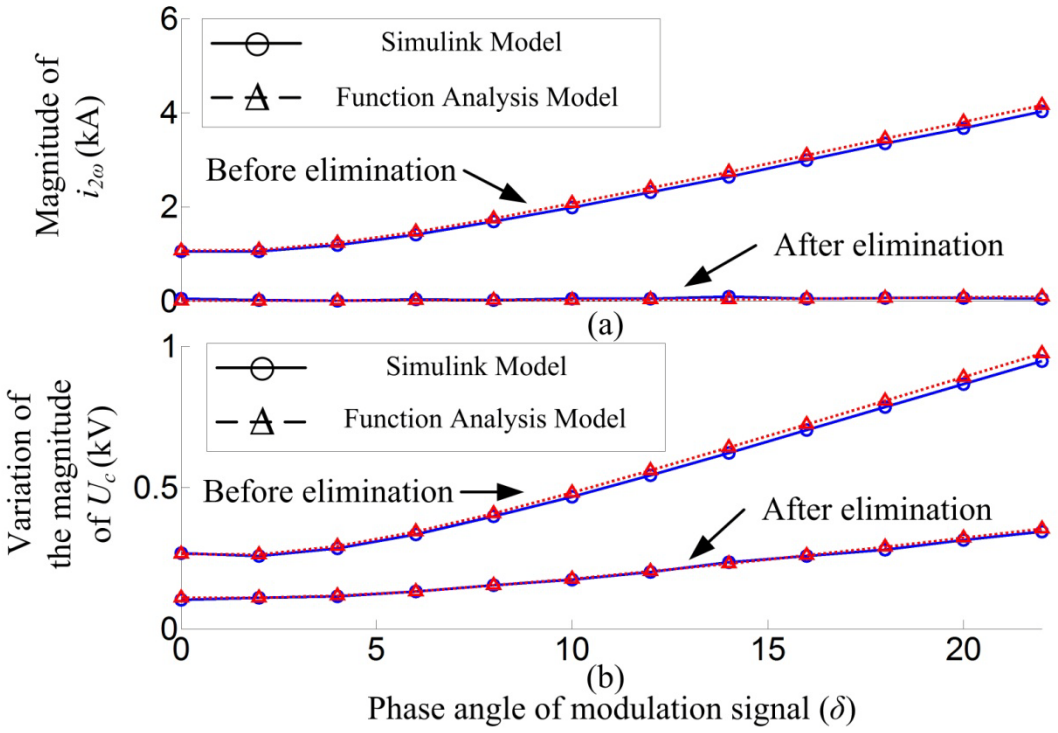


Fig. 4-12 Validation test results on feed-forward elimination method of Fig. 4-2. (a) Magnitude of 2nd harmonic circulating current and (b) Magnitude of capacitor voltage plotted as a function δ

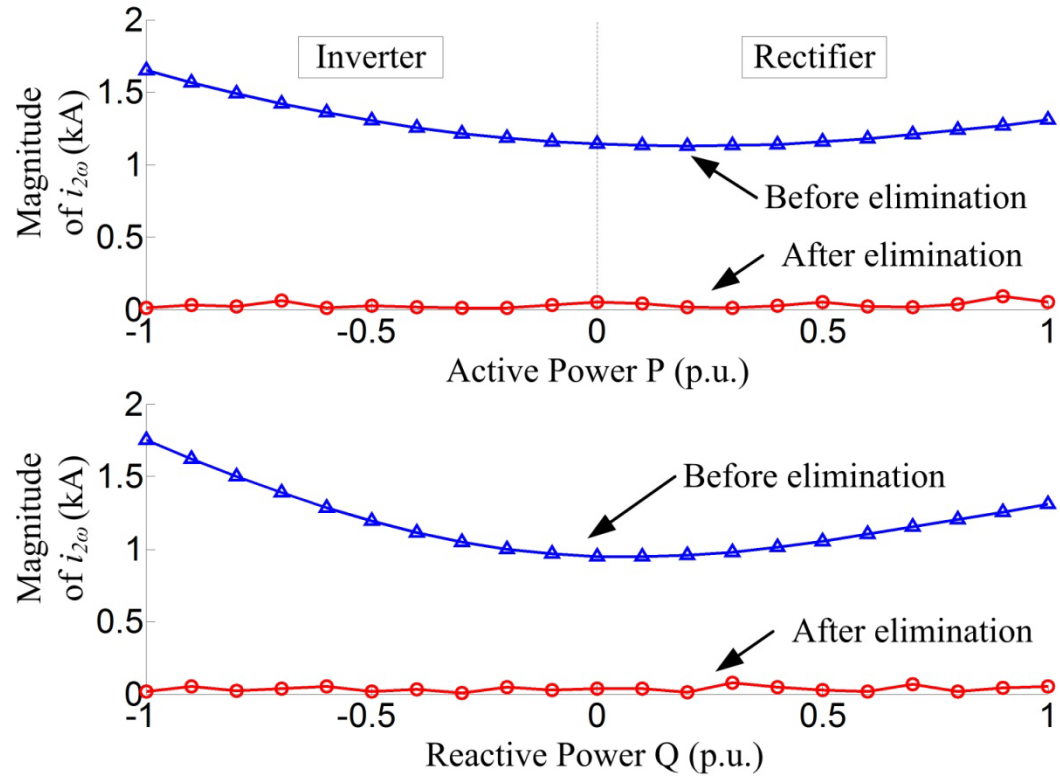


Fig. 4-13 Validation test results on feed-forward elimination method of Fig. 4-2. Magnitude of 2nd harmonic circulating current (a) as function of Active Power and (b) as function of Reactive Power

Table 4-V FFT of 2nd harmonic circulating current with different SM number per arm

SM number per arm		6	12	24	36	48
SM capacitance (mF)		2.5	5	10	15	20
Arm inductance (mH)		3	3	3	3	3
$i_{2\omega}$ (Normalized)	Before elimination	1	1	1	1	1
	After elimination	0.0305	0.0311	0.0304	0.0307	0.0316

E. Test on Dynamic Elimination Capability

The simulation test results in Fig. 4-14 and Fig. 4-15 show that the feed-forward control of Fig. 4-2 has dynamic harmonic elimination capability under severe active and reactive power reversal tests. Until t=0.6s, the feed-forward control is not activated. At t=0.8s, Fig. 4-14 is given a ramp of active power reversal, P from -1 to 0.4 p.u. and Fig. 4-15 is given a ramp of reactive power reversal, Q from 0.8 p.u. to -0.8 p.u..

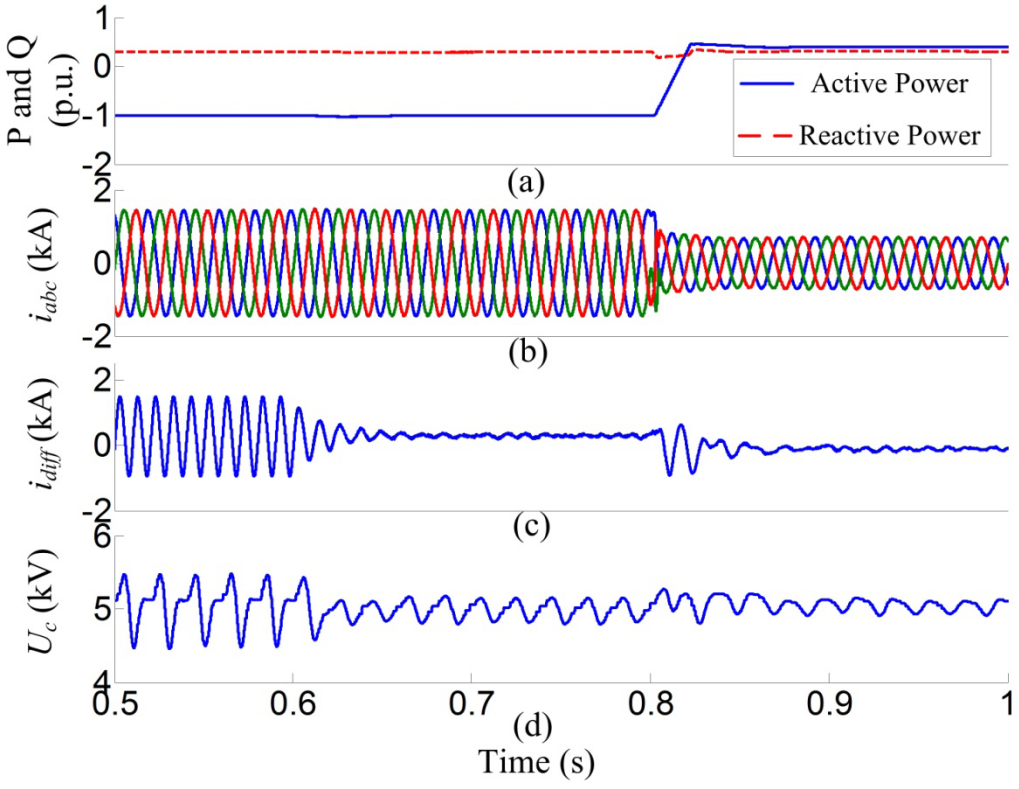


Fig. 4-14 Simulation results showing dynamic 2^{nd} harmonic elimination capability when P ramps from -1 *to* 0.4 p.u. at time t= 0.8s. (a) P and Q; (b) three phase ac currents; (c) differential mode current i_{diff} of phase a; (d) individual capacitor voltage of phase a, upper arm

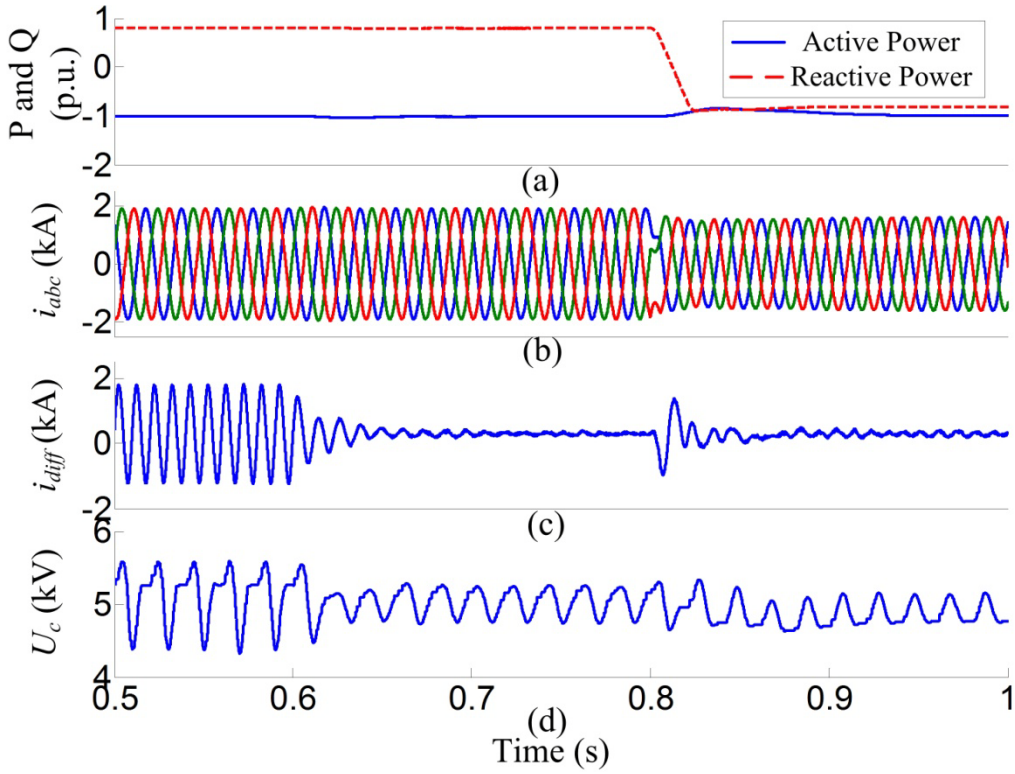


Fig. 4-15 Simulation results showing dynamic 2^{nd} harmonic elimination capability when Q ramps from 0.8 *to* -0.8 p.u. at time t= 0.8*s*. (a) P and Q; (b) three phase ac currents; (c) differential mode current i_{diff} of phase a; (d) individual capacitor voltage of phase a, upper arm

4.5 Conclusion

This chapter has used the mathematical formulas to gain analytical insights, which enable the origin of 2^{nd} harmonic circulating currents to be pin-pointed and to indicate how the origin can be annulled by added voltage components.

By extending the harmonic function analysis, which [48] has begun, this chapter comes up with a feed-forward method to reduce the 2^{nd} harmonic component of single-phase ac power which is root of the complexity in MMC. With 2^{nd} harmonic circulating current elimination, the undesirable low frequency harmonic voltages proliferated by it are also eliminated. The benefits are: (i) over-sized capacitors in the sub-modules can be reduced; (ii) enhanced protection by grounding of transformer neutrals is feasible. The feed-forward method is shown to be effective under dynamic conditions. In addition to deriving mathematical formulas of harmonic voltage components of "open loop" control, the chapter has made original contributions by deriving formulas which include feed-forward.

The formulas in Table 4-I and Table 4-II enable the complexity of MMC to be pried apart for understanding. For instance, the formulas show that the capacitors of the sub-modules appear as series capacitor reactance on the ac side which can be used for power factor improvement as demonstrated in Fig. 4-10.

Chapter 5 Incorporating DEADBEAT and Low-Order Harmonic Reduction in MMC

5.1 Introduction

Reference Current Control is important in protecting converters from ac faults. When ac currents are regulated at reference values, they are prevented from growing to destructive levels during faults. Using deadbeat control to make VSCs operate under Reference Current Control is a frequent practice [65-72]. Under deadbeat, the VSCs are with fast response, delay of 2 computation steps for example. Deadbeat in VSCs prevents harmonics from the dc side from crossing over to the ac-side [71]. Deadbeat, in enforcing reference signal tracking, should stop 3rd and odd harmonics generated by nonlinearities of MMC from emerging on the ac currents. But does MMC accept deadbeat control? This chapter answers in the affirmative. However as [73] shows, research on deadbeat for MMC has only just begun.

Since the even harmonics in the circulating current are on the dc side, deadbeat cannot eliminate them. Therefore, in order to reduce the size and cost of large sub-module capacitors which are required to filter the even harmonics, the feedback methods of [54, 55, 74-77] and the feed-forward method in Chapter 4 have to be used. These harmonic elimination methods come to naught, if during faults the ac fault currents charge the capacitors of reduced size, so that their dc voltages rise above the safe voltage limit of IGBTs. Deadbeat rescues the elimination methods by preventing large fault currents. But can MMC implement both deadbeat and harmonic elimination together?

The joint implementation of deadbeat and harmonic elimination methods by MMC is possible by following the results of harmonic function analysis of Chapter 3 and Chapter 4, which have shown that MMC has two decoupled amplification channels: (i) a fundamental frequency channel of the modulation signal to produce an amplified voltage of $U_{ref}cos(\omega t+\delta)$ on the ac side; (ii) a 2nd harmonic channel of the modulation signal

'$Ycos(2\omega t+\gamma)$' which produces an amplified voltage on the dc side. Deadbeat is implemented in the fundamental frequency channel whereas harmonic elimination is implemented in the 2nd harmonic channel of $Ycos(2\omega t+\gamma)$. The theoretical base of this chapter depends on Table 3-II, Table 3-III, Table 4-I and Table 4-II of Chapter 3 and Chapter 4.

The objectives of this chapter are to show how both: (i) deadbeat, in open loop and with closed loop current feedback; and (ii) feed-forward and feedback to eliminate low frequency harmonics, can be implemented by MMC.

The multiple objectives are fulfilled as follows: Section 5.2 briefly introduces the two channels of control: (i) deadbeat and (ii) low frequency harmonic reduction. Section 5.3 presents the principles of deadbeat. Section 5.4 reviews the feed-forward method of Chapter 4 and presents a feedback method based on the innovative Complement Notch Filter to identify the 2nd harmonic as the "error" for negative feedback elimination. Section 5.5 presents simulation results of successful deadbeat implementation as well as the joint application of deadbeat, feedback and feed-forward harmonic elimination. Conclusions are presented in Section 5.6.

5.2 Two Channels of Control

The objective of this section is to show that MMC has one channel to implement deadbeat and another channel to implement harmonic elimination. The two independent channels are found in the formulas of Table 3-II and Table 3-III of Chapter 3, and Table 4-I and Table 4-II of Chapter 4. To avoid repetition, the analysis of only one phase is conducted. Fig. 5-1 (a) shows the ac-side of one MMC phase represented by ideal voltage v_{ac} on the ac side and T_1, T_4, T_6 and T_7 voltages inside the MMC. The voltage at the point of common coupling (PCC) is v_{PCC}; $U_{dc}=(T_1+T_4+T_6+T_7)$ denotes the dc system voltage; L_0 and R_0 represent MMC arm inductance and its equivalent resistance; L_{ac} and R_{ac} are the ac system inductance and equivalent resistance. Fig. 5-1 (b) shows the dc side equivalent circuit with ideal voltages sources $2T_2$, $2T_3$, $2T_5$ and $2T_8$.

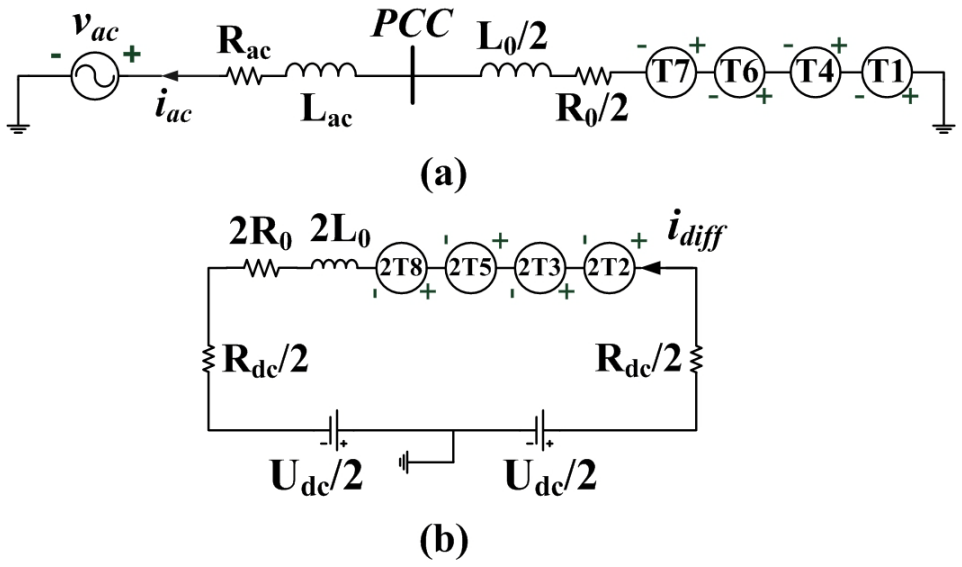


Fig. 5-1 MMC phase represented by ideal voltages: (a) ac side; (b) dc side

E. Fundamental Frequency Channel of $U_{ref}cos(\omega t+\delta)$

As discussed in Chapter 3, the modulation signals of the upper arm and lower arm of one phase on MMC are:

$$m_u(t) = \frac{1}{2} - \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta) \tag{5-1}$$

$$m_l(t) = \frac{1}{2} + \frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta) \tag{5-2}$$

Referring to Fig. 5-1(b) and Table 3-III, on the dc side the significant voltage is T_2.

$$T_2 = \frac{N}{2C}\int_{-\infty}^{t}[\frac{I_d}{2} - \frac{U_{ref}I_{ac}}{4U_{DC}}\cos(\delta - \varphi_{ac})]d\tau \tag{5-3}$$

T_2 is the voltage of ac-to-dc power balance. In steady-state, $2T_2 \approx U_{dc}$.

Referring to Fig. 5-1(a) and Table 3-II, the significant voltage on the ac side is T_6

$$\begin{aligned} T_6 &= -\frac{NU_{ref}}{CU_{dc}}\cos(\omega t + \delta)\cdot\int_{-\infty}^{t}[\frac{I_d}{2} - \frac{U_{ref}I_{ac}}{4U_{DC}}\cos(\delta - \varphi_{ac})]d\tau \\ &= -\frac{U_{ref}}{U_{dc}}\cos(\omega t + \delta).2T_2 = -U_{ref}\cos(\omega t + \delta) \end{aligned} \tag{5-4}$$

From (18), one concludes that the sinusoidal component of the modulation signal $(U_{ref}/U_{dc})\cos(\omega t+\delta)$ has T_6 as its amplified voltage on the ac side.

F. Double Frequency Channel of $Y\cos(2\omega t+\gamma)$

Chapter 4 considers adding $u_{add}(t)=Y\cos(2\omega t+\gamma)$ to the modulation signal to $m_u(t)$ and $m_l(t)$ so that they take the forms of:

$$m_u(t)' = \frac{1}{2} - \frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta) + \frac{Y}{U_{dc}}\cos(2\omega t+\gamma) \tag{5-5}$$

$$m_l(t)' = \frac{1}{2} + \frac{U_{ref}}{U_{dc}}\cos(\omega t+\delta) + \frac{Y}{U_{dc}}\cos(2\omega t+\gamma) \tag{5-6}$$

where superscript ' redefines the modulation signals after modification.

As elaborated in Chapter 4, by following the same procedure in deriving Table 3-II and Table 3-III, two new tables of Table 4-I and Table 4-II are obtained when applying the modified modulation signals (5-5) and (5-6). To simplify bookkeeping, it is assumed that the second harmonic currents bearing '*X*' have already been eliminated. In order that the effect of $u_{add}(t)$ stands out, '*Y*' has been given as its amplitude. There are entries bearing '*Y*' everywhere in Table 4-I and Table 4-II. All terms bearing '*Y*' are numerically small compared to T_F.

$$T_F = Y\cos(2\omega t+\gamma) \tag{5-7}$$

T_F, on the dc side, is the amplified voltage of the 2nd harmonic modulation signal in (5-5) and (5-6). Therefore MMC has an independent channel whereby T_F is applied through feed-forward or feedback to counteract the source 2nd harmonic voltages in Table 3-III.

5.3 Single-Phase Deadbeat Control

Deadbeat control makes use of a modified input signal to reach the optimal step response. Most texts on deadbeat apply sampled data formulations and z-transforms. For readers, who are more familiar with the time-domain, this section presents the principles of deadbeat from linear system theory where the transfer function $H(s)$ is the Laplace Transform of the impulse response $h(t)$. A distinctive feature of the deadbeat control in this chapter is that it does not require d-q transformation. As an individual phase controller, it handles asymmetric operating conditions, such as a single-line fault. [Notations used in this section: $u_{-1}(t)$, $u_0(t)$ are symbols of step, impulse function. $du_{-1}(t)/dt=u_0(t)$]

A. Open Loop Deadbeat

Fig. 5-2 is used to present the principles of deadbeat in time domain. "Plant", in deadbeat terminology, consists of "*L*" and "*R*" in Fig. 5-2. Referring to Fig. 5-2 (a), $L=L_0/2$, $R=R_0/2$. In Fig. 5-2 (a), the "plant" lies between $v_{PCC}(t)$, the voltage of the point of common coupling (PCC), and $v(t)=T_6$, the voltage produced by the $U_{ref}cos(\omega t+\delta)$ channel. The current $i_c(t)$ in the "plant" is $i_{ac}(t)$.

1). *Reference Current Control*

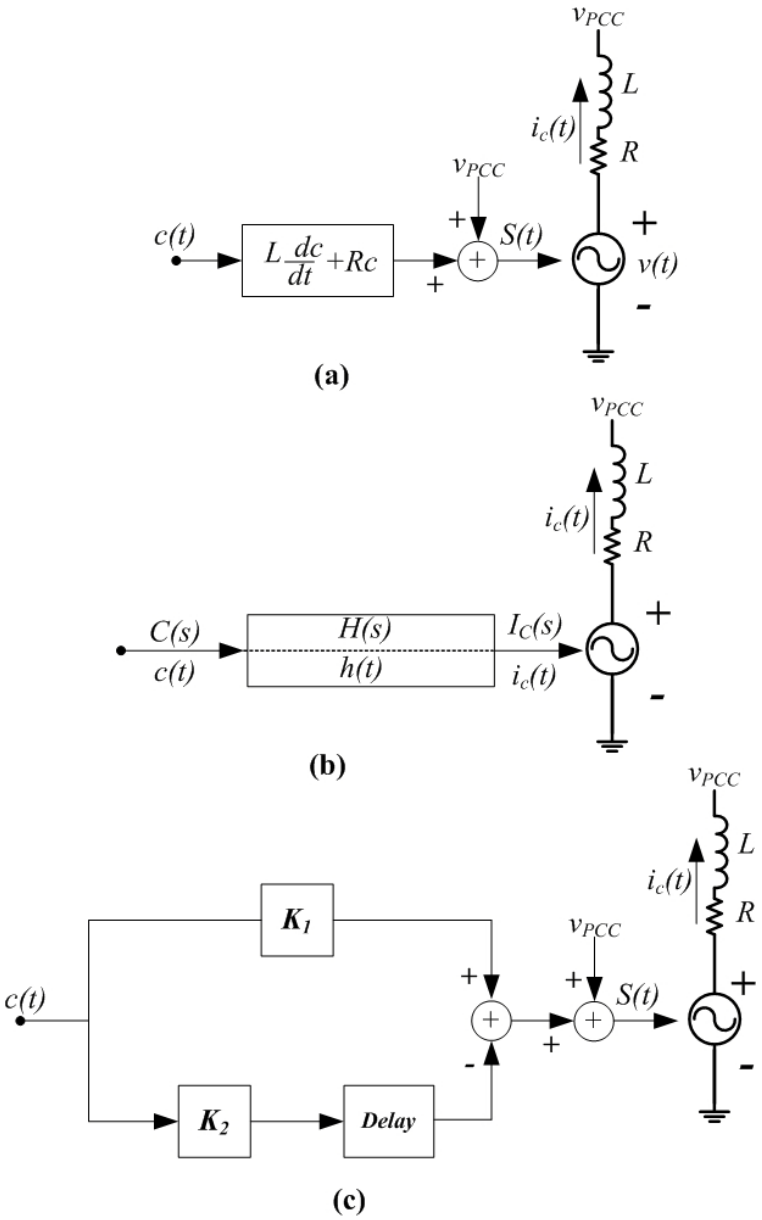


Fig. 5-2 Reference Current Control: (a) Ideal implementation; (b) Transfer Function of Implementation; (c) Deadbeat Implementation

In *Reference Current Control*, an ideal voltage source $v(t)$ is required to produce a current $i_c(t)$ in response to reference current command $c(t)$. In Fig. 5-2 (a), from KVL, the current $i_c(t)$ is solved from

$$L\frac{di_c}{dt}(t)+Ri_c(t)=v(t)-v_{PCC}(t) \tag{5-8}$$

On the ac side of the MMC, $v_{PCC}(t)$, the voltage measured at the PCC, is a sinusoidal voltage at line frequency. When the reference current $c(t)$ is also a line frequency sinusoidal signal, the sinusoidal component of the modulation signal $S(t)$ is also a line frequency sinusoidal term. Writing

$$S(t)=\frac{1}{A}\left[L\frac{dc(t)}{dt}+Rc(t)+v_{PCC}(t)\right] \tag{5-9}$$

where A is the amplification gain and substituting $v(t)=AS(t)$ in (5-8)

$$L\frac{di_c(t)}{dt}+Ri_c(t)=L\frac{dc(t)}{dt}+Rc(t) \tag{5-10}$$

The equality in (5-10) means that the plant current $i_c(t)$ tracks the current reference signal $c(t)$, that is

$$i_c(t)=c(t) \tag{5-11}$$

Because $Ldc(t)/dt$ cannot be implemented accurately, the deadbeat method serves as a good approximation.

2). *Transfer Function Approach*

Taking the Laplace Transform by which $i_c(t)\rightarrow I_C(s)$, $c(t)\rightarrow C(s)$, (5-11) is expressed by the transfer function relationship as:

$$I_C(s)=H(s)C(s) \quad \text{where} \quad H(s)=1 \quad \text{for } -j\infty \le s \le +j\infty \tag{5-12}$$

The time domain equivalent of (5-12) is the convolution integral relationship

$$i_c(t)=\int_{-\infty}^{t} c(\tau)h(t-\tau)d\tau \tag{5-13}$$

where $h(t-\tau)$ is the impulse response of $H(s)$. For $H(s)=1$, the impulse response has to be the impulse function, that is $h(t-\tau)=u_0(t-\tau)$.

Fig. 5-2 (b) shows the relationship of (5-12) and (5-13) in block diagram form. An impulse is a waveform with infinitesimally narrow width w and height $1/w$ so that the area of the pulse is 1. When $h(t-\tau)$ is the impulse function $u_0(t-\tau)$ in (5-13), then $i_c(t)=c(t)$. This

is because the impulse function $u_0(t-\tau)$ is zero everywhere from $\tau=-\infty$ to $\tau=t$ so that the integral in (5-13) is zero everywhere except at $\tau=t$. At $\tau=t$, because $u_0(t-\tau)$ has unity area. When multiplied by c(τ), the integral yields $i_c(t)=c(t)$.

The deadbeat method, implemented as shown in Fig. 5-2 (c), is based on creating a very narrow current pulse whose area is unity, thereby approximating the impulse response of the transfer function $H(s)=1$.

3). *Constructing Deadbeat Control Block*

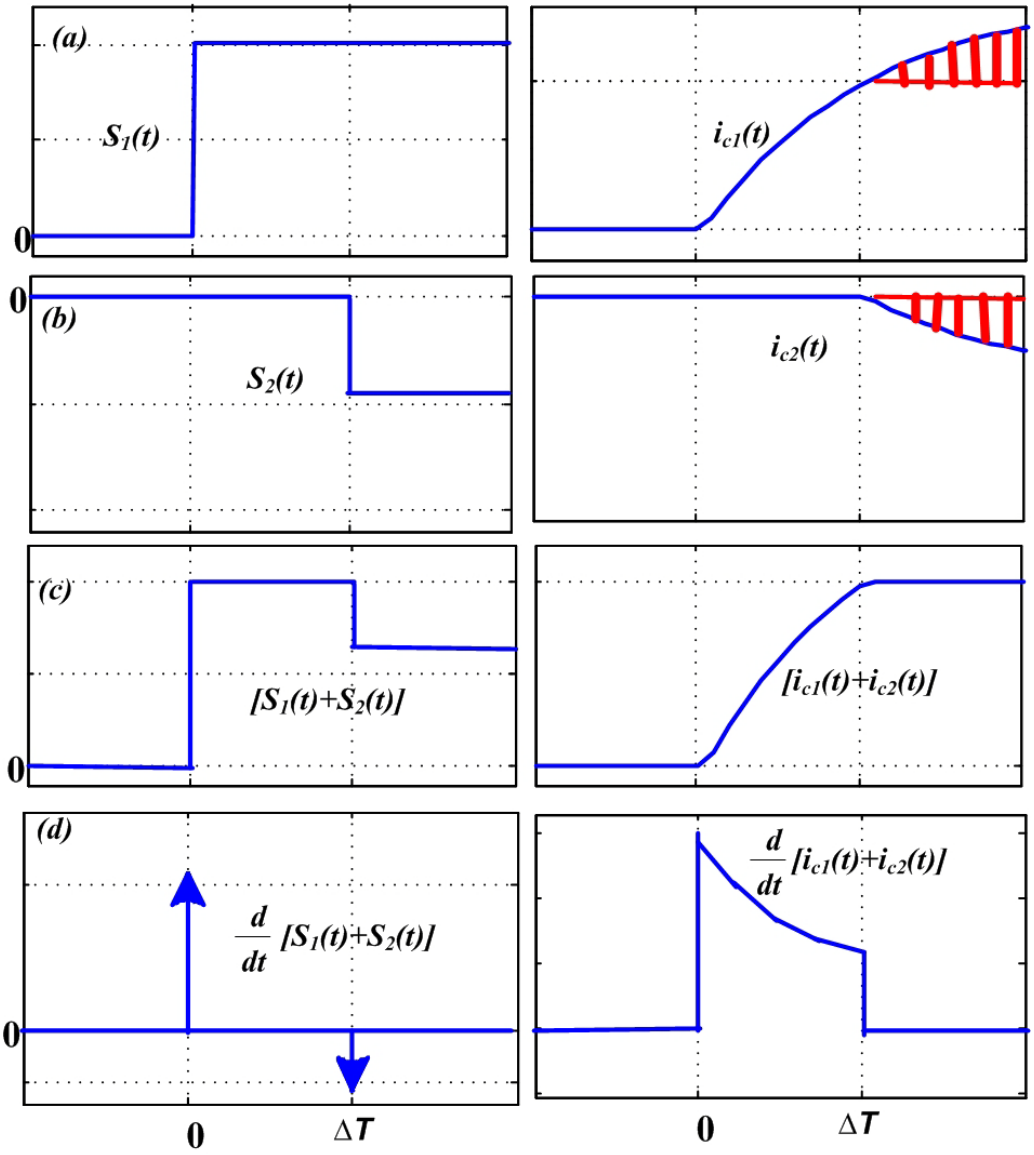


Fig. 5-3 Illustrations of construction of dead-beat block diagram. (*a*) step input $S_1(t)$; (*b*) delayed step input $S_2(t)$; (*c*) $S_1(t)+S_2(t)$; (*d*) $d[S_1(t)+S_2(t)]/dt$.(left) voltage waveforms; (right) response waveform of current in "*L-R* plant"

The blocks in Fig. 5-2 (c) precondition the current reference $c(t)$ so that its output when added to feed-forward voltage $v_{PPC}(t)$ becomes the modulation signal '$S(t)$'. As the voltage at the PCC is equal and opposite to the feed-forward component $v_{PPC}(t)$ in $v(t)$, the gains K_1, K_2 and the delay are designed to ensure that for input as an impulse current reference $c(0)=u_0(0)$, the voltage source $v(t)$ outputs current which is a close approximation of $i_c(t)= u_0(0)$.

The steps to the construction of the block of K_1, K_2 and the delay are illustrated in Fig. 5-3. The graph on the left of Fig. 5-3 (a) illustrates a step input to the modulation signal, $S_1u_{-1}(0)$. In response to the step voltage

$$v(t) = AS_1u_{-1}(0) \tag{5-14}$$

From T_6 of (5-4), the amplification gain $A=U_{dc}$ and the well-known solution of the differential equation (5-10), the current to the step voltage is

$$i_{c1}(t) = U_{dc}\frac{S_1}{R}(1-e^{-\frac{R}{L}t}) \tag{5-15}$$

The long time response of the current, illustrated on the graph on the right, is reduced by adding a time-delayed negative step input $S_2u_{-1}(-\Delta T)$ (magnitude S_2 after delay of ΔT) as illustrated in the left of Fig. 5-3 (b). Its current response is shown on the right of Fig. 5-3 (b).

Using the formula of (5-15) to scale S_2 with respect to S_1 and ΔT so that the shaded portion of the current in Fig. 5-3 (b) cancels that of Fig. 5-3 (a), the slow response is lopped off as shown on the right of Fig. 5-3 (c). The modulation signal which produces the current is $S_1u_{-1}(0)+S_2u_{-1}(-\Delta T)$, the sum of the inputs of Fig. 5-3 (a) and Fig. 5-3 (b) as illustrated on the left of Fig. 5-3 (c).

From system theory, an impulse function is obtained by differentiating a step function. The left of Fig. 5-3 (d) illustrates the two impulses obtained by differentiating the step functions in the left of Fig. 5-3 (c). Also, the current output in Fig. 5-3 (d) is the differentiated form of the current on the right of Fig. 5-3 (c). On differentiating (5-15)

$$\frac{di_c(t)}{dt} = U_{dc}\frac{S_1}{L}e^{-\frac{R}{L}t} \qquad 0 \le t \le \Delta T \tag{5-16}$$

For small ΔT, the narrow pulse has an approximate area of $\Delta T U_{dc} S_1 / L$ which has the dimension of the current. The narrow pulse of Fig. 5-3 (d) can be approximated as an impulse. Since the area is the gain, it follows that

$$\left|H(j\omega)\right| = U_{dc} S_1 \frac{\Delta T}{L} \tag{5-17}$$

The block diagram of Fig. 5-2 (c) is developed from Fig. 5-3. The formulas of K_1 and K_2 are derived as [72]:

$$K_1 = R \frac{1}{1 - e^{-\frac{R}{L}\Delta T}} \tag{5-18}$$

$$K_2 = R \frac{e^{-\frac{R}{L}\Delta T}}{1 - e^{-\frac{R}{L}\Delta T}} \tag{5-19}$$

The "delay" block contains ΔT. Since $c(t)$ and $v_{PCC}(t)$ are fundamental frequency waveforms, $S(t)$ has the functional form of $U_{ref} cos(\omega t + \delta)$ in (5-1). The MMC produces this voltage as T_6.

B. Close-Loop Deadbeat

MMC has to operate in the face of uncertainties. The voltages $v_{PCC\text{-}a}(t)$, $v_{PCC\text{-}b}(t)$ and $v_{PCC\text{-}c}(t)$ at the points of common coupling immunize, to some extent, the uncertainties in the ac-circuits outside the MMC. Because the components (arm inductance and its equivalent resistance) belong to the manufacturer and can be measured precisely, deadbeat can be designed with confidence. But parameters change with temperature and other climatic factors. Close-loop feedback control, in general, makes performance insensitive to parameter variations. Closed loop feedback control is implemented as shown in Fig. 5-4 [72].

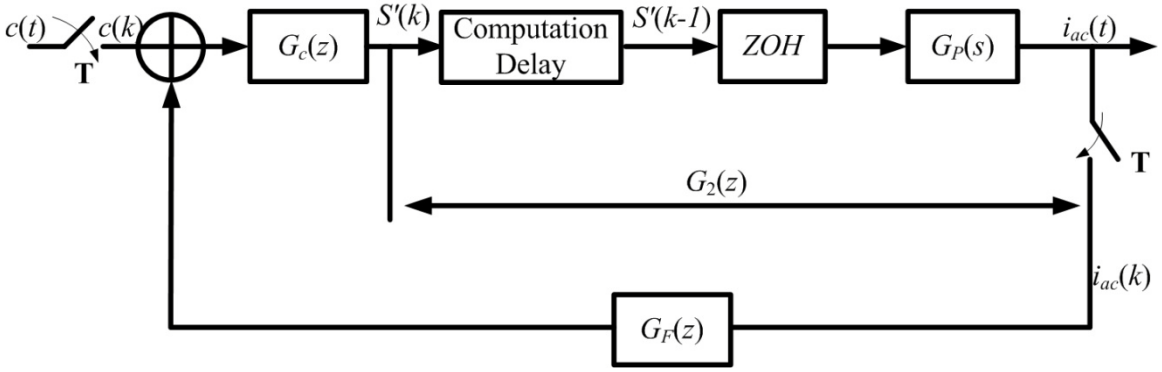


Fig. 5-4 Schematic of local current feedback of deadbeat

Because of a delay block has to be represented by exponential transfer function $e^{-a\Delta T}$, analysis is easier by passing from the "s-domain" to the "z-domain" of sampled data analysis. In the feedback block diagram shown in Fig. 5-4, the implementation of sampling is illustrated by the opening and closing of switches "*T*" so that $c(t)$ becomes $c(k)$. The objective is to design the closed loop deadbeat to have delay of $2\Delta T$. The overall transfer function is z^{-2}.

In Fig. 5-4, its output $S'(k)$ is added to $v_{PCC}(t)$. Their sum becomes the sinusoidal component of the modulation signal $S(t)$ in Fig. 5-2 (c).

In continuous frequency domain, the zero-order-hold (ZOH) block and the plant (L-R) in Fig. 5-2 are:

$$G_{ZOH}(s)=\frac{1-e^{-s\Delta T}}{s} \tag{5-20}$$

$$G_P(s)=\frac{b}{s+a} \tag{5-21}$$

Here, $a=R/L$, $b=1/L$. Taking the Z transform of $G_{ZOH}(s)G_P(s)$,

$$G_{ZOH}(z)G_P(z)=\frac{b}{a}\frac{1-e^{-a\Delta T}}{1-e^{-a\Delta T}z^{-1}}z^{-1} \tag{5-22}$$

Including the computational delay of z^{-1} in Fig. 5-4, the overall transfer function is designed to be:

$$G(z)=\frac{G_C(z)z^{-1}G_{ZOH}G_P(z)}{1+G_F(z)G_C(z)z^{-1}G_{ZOH}G_P(z)}=z^{-2} \tag{5-23}$$

which has a sampling delay of two sampling periods. The controller blocks $G_C(z)$ and $G_F(z)$ can be derived as:

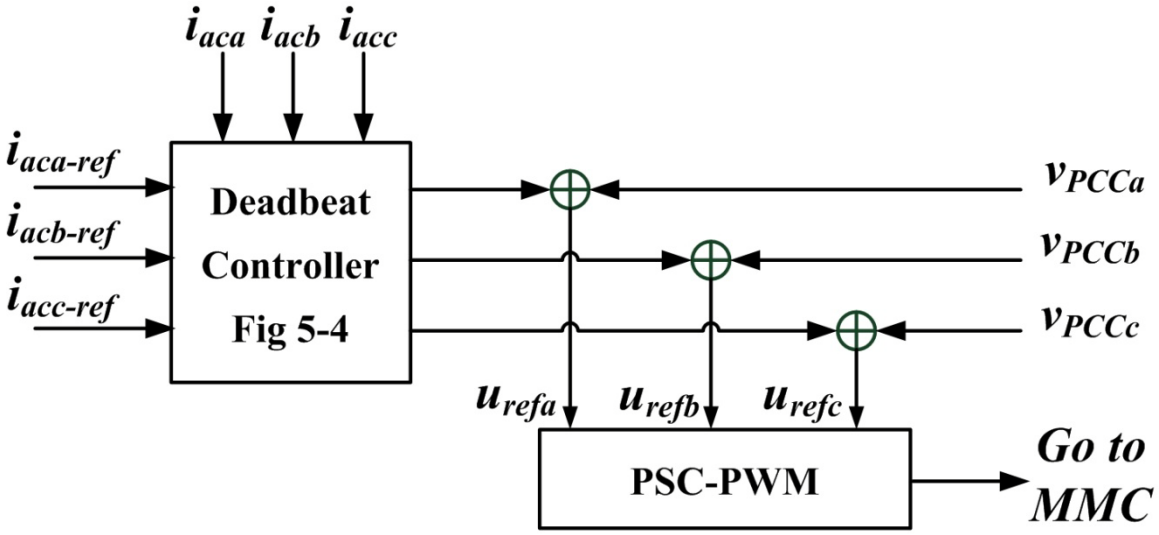


Fig. 5-5 Block diagram of closed loop deadbeat control for MMC

$$G_C(z) = \frac{a}{b}\frac{1}{1-e^{-a\Delta T}}\frac{1}{1+e^{-a\Delta T}z^{-1}} \tag{5-24}$$

$$G_F(z) = e^{-2a\Delta T} \tag{5-25}$$

Detailed derivation of closed loop blocks [72] is given in Appendix A.

Fig. 5-5 shows the block diagram of closed-loop deadbeat control for 3-phase MMC. i_{acj} represents the feedback ac current; $i_{acj\text{-}ref}$ is the reference current; v_{PCCj} denotes the voltage at PCC; u_{refj} is the MMC reference voltage forming the modulation signal (j=a, b, c). As discussed above, theoretically, digital closed-loop deadbeat control only introduces two sample delays, whereas when it is applied in MMC with PSC-PWM modulation technique, more delays are brought about. Since the triangular carriers are with limited magnitude, when modulation signal exceeds the maximum value of the carriers, saturation occurs. That means the MMC is not an ideal actuator and may not respond optimally. Nevertheless, the simulation results in Section 5.5 indicate that the response of the closed loop deadbeat controller is still fast enough and the ac currents can track the reference within half period.

5.4 Feed-forward and Feedback Low-order Harmonic Elimination

Harmonic function analysis in Chapter 3 and Chapter 4 shows that the origin of low frequency harmonics comes from voltage components without '*X*' in T_3, T_5 and T_8 in the

2nd harmonic column of Table 3-III. Their voltages cause the flow of 2nd harmonic circulating current $i_{2\omega}(t)=X\cos(2\omega t+\varphi_2)$. The 2nd harmonic circulating current then proliferates to other low frequency harmonic voltages in Table 3-II and Table 3-III, identified by '*X*'. Therefore if a voltage can be introduced which cancels the 2nd harmonic voltage sources, then not only is the 2nd harmonic eliminated but the other low-order harmonics proliferated by it as well.

A. Feed-forward Method

As discussed in Chapter 4, the voltage components $T_{3\text{-}2\omega\text{-}ii}$, $T_{5\text{-}2\omega}$ and $T_{8\text{-}2\omega\text{-}i}$ in Table 3-III are considered to be the original source of 2nd harmonic because they do not bear the '*X*' term. The 2nd harmonic current is eliminated at the source if the voltage T_F controlled by $u_{add}(t)=Y\cos(2\omega t+\gamma)$ cancels the total source voltages:

$$\begin{aligned} T_F &= -[T_{3-2\omega-ii} + T_{5-2\omega} + T_{8-2\omega-i}] \\ &= -\frac{NU_{ref}^2 I_d}{2\omega C U_{dc}^2}\sin(2\omega t + 2\delta) + \frac{3NU_{ref} I_{ac}}{16\omega C U_{dc}}\sin(2\omega t + \delta + \varphi_{ac}) \end{aligned} \tag{5-26}$$

In Chapter 4, the effectiveness of the feed-forward elimination method has been demonstrated for extensive ranges of operations.

B. Feedback Method

Feedback likewise makes use of $u_{add}(t)=Y\cos(2\omega t+\gamma)$. The signal for feedback method (name it as $u_{add\text{-}b}(t)$) is obtained from a P-I controller which takes 2nd harmonic circulating current $i_{2\omega}(t)$ as the input. This section shows two approaches to extract $i_{2\omega}(t)$ from the differential mode current $i_{diff}(t)$ of Fig. 5-1 (b).

1). *Feedback method 1*

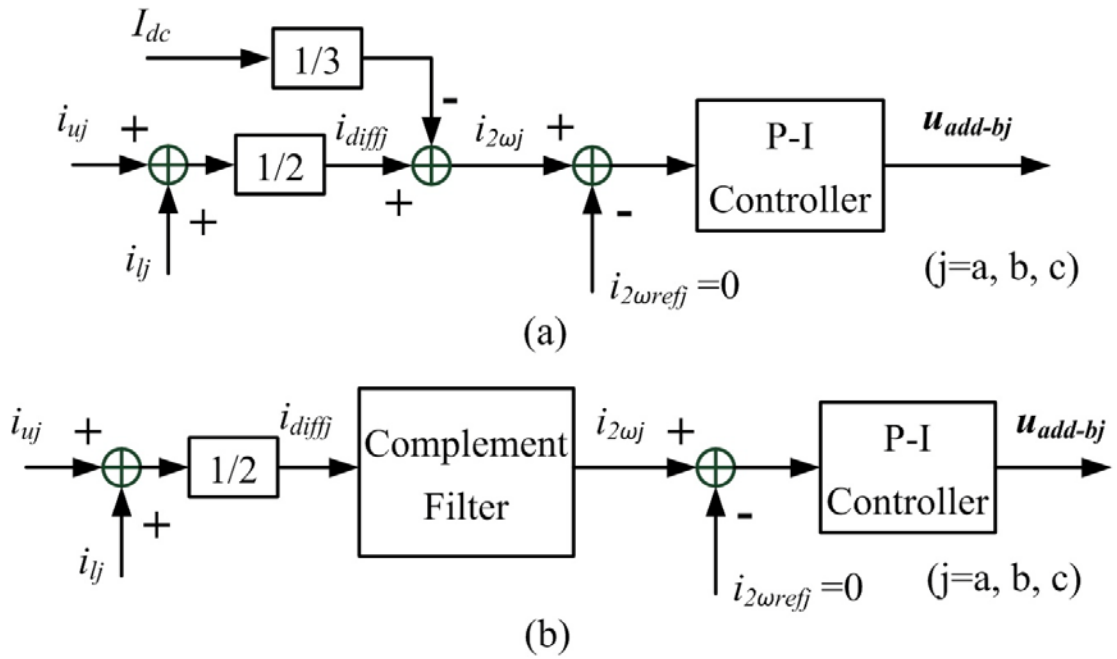


Fig. 5-6 Block diagram of feedback control of low-order harmonic reduction. (a) feedback method 1; (b) feedback method 2

As shown in Fig. 5-6 (a), the 2nd harmonic circulating current of each phase is obtained from half of the sum of the corresponding upper arm and lower arm currents. This yields $i_{diffj}=i_{2\omega j}+(I_{dc}/3)$. Then one third of the dc output current I_{dc} is subtracted. After passing a P-I controller, $u_{add\text{-}b}(t)$ of each phase is sent to the modulation signal. This method is named as feedback method 1 or feedback 1.

2). *Feedback method 2*

In case the a-, b- and c-phase are unbalanced, it is not possible to depend on the dc phase current of the jth phase being one third of the total dc output current. In this case, $i_{2\omega j}$ is selected from i_{diffj}. This method is referred to as feedback method 2 or feedback 2.

The overall block diagram is shown in Fig. 5-6 (b). It makes use of an innovative complement notch filter as to extract the 2nd harmonic circulating current from $i_{diff}(t)$. Along the lower path of Fig. 5-7 (a), $i_{diff}(t)$ passes that through the Fliege Notch Filter, tuned to the 2nd harmonic. Fig. 5-7 (b) and Fig. 5-8 (a) respectively show the schematic of the Fliege Notch Filter [78] and its Bode diagram. f_0 is the center frequency of the filter which is tuned by resistor R_0 and capacitor C_0. The output of the lower path is subtracted from unfiltered $i_{diff}(t)$ of the upper path. The result is a band pass filter centered at the 2nd harmonic whose Bode diagram is shown by Fig. 5-8 (b) the complement of the “notch” of

Fig. 5-7 (b). (Because it has better characteristics, the Fliege Notch Filter has been chosen over the Twin-Tee Notch filter [78].)

As shown in Fig. 5-6 (b), the difference of the reference and 2nd harmonic extract of $i_{diff}(t)$ becomes negative feedback error. The feedback error, after passing through a P-I block, is used as the modification component of the modulation signal $u_{add\text{-}b}(t)$.

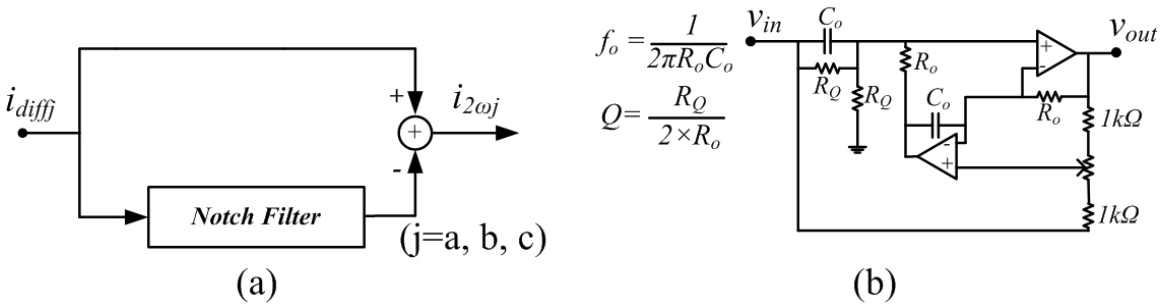


Fig. 5-7 (a) Complement Notch Filter; (b) Fliege Notch Filter

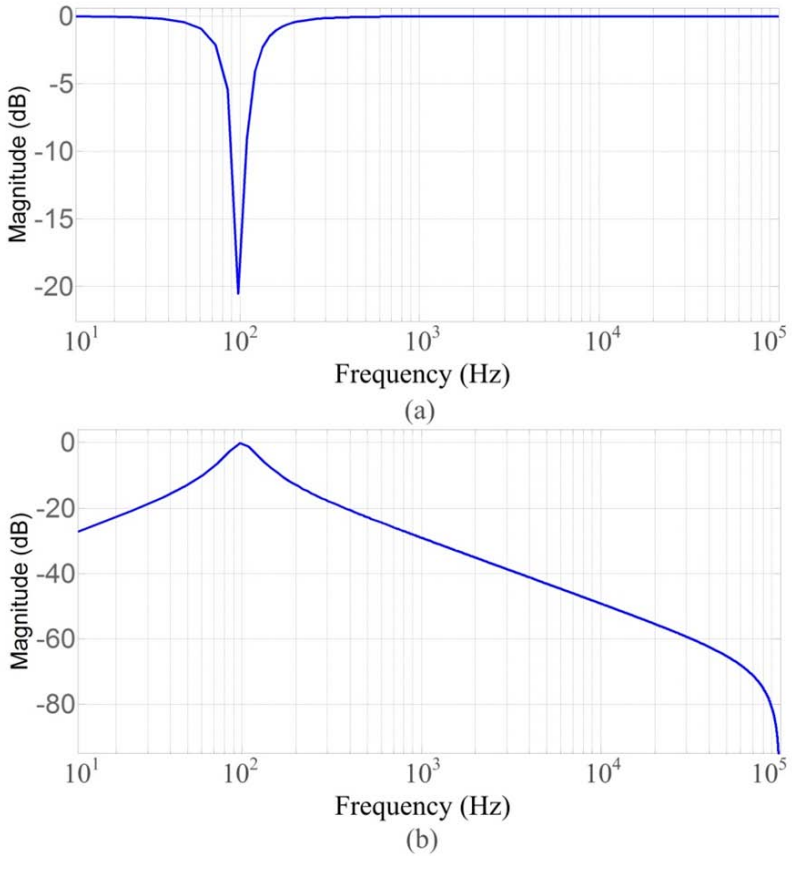


Fig. 5-8 (a) Magnitude-vs-frequency of Fliege Notch Filter; (b) Magnitude-vs-frequency of Complement Notch Filter

Table 5-I Parameters used in the simulation tests

Parameter	Value	Parameter	Value
Rated Power P	50 MW	SM capacitance	5 mF
DC voltage U_{dc}	60 kV	Number of SM per arm	12
Arm inductance L_0	3 mH	AC voltage V_{ac}	25 kV
Arm equivalent resistance R_0	0.3 Ohm	Transformer leakage inductance L_T	1 mH

5.5 Simulation Results

Simulation tests have been conducted for a 3-phase MMC station of Fig. 2-1 (a). Table 5-I lists the parameters used for the 12 SM MMC station. The simulation software Simulink/MATLAB goes to the detail of "Phase shifted carrier Pulse Width Modulation (PSC-PWM)" and the sorting algorithm, taken from [44], to ensure that the voltages of the capacitors of each string are balanced.

5.5.1 Test on Capability of Closed Loop Deadbeat to Eliminate Harmonics

T_4 and T_7 in Table 3-II of Chapter 3 have 3rd harmonic voltage components on the ac side. Normally, the ac sides of MMC stations are connected to transformers in delta or open wye to exclude the 3rd harmonic current generated by T_4 and T_7. The simulation test consists of connecting the MMC to transformers in wye with the neutral grounded so that 3rd harmonic currents can flow. As shown in Fig. 5-9 (a), the 3-phase current waveforms have large 3rd harmonics, confirming the predictions of the formulas. When the MMC station operates under deadbeat with current feedback as shown in Fig. 5-5, the 3rd harmonic is not noticeable in Fig. 5-9 (b). This confirms experience with VSCs in [71]; closed loop deadbeat prevents harmonics from flowing to ac side. The current THD is reduced from 10.7 % to 2%.

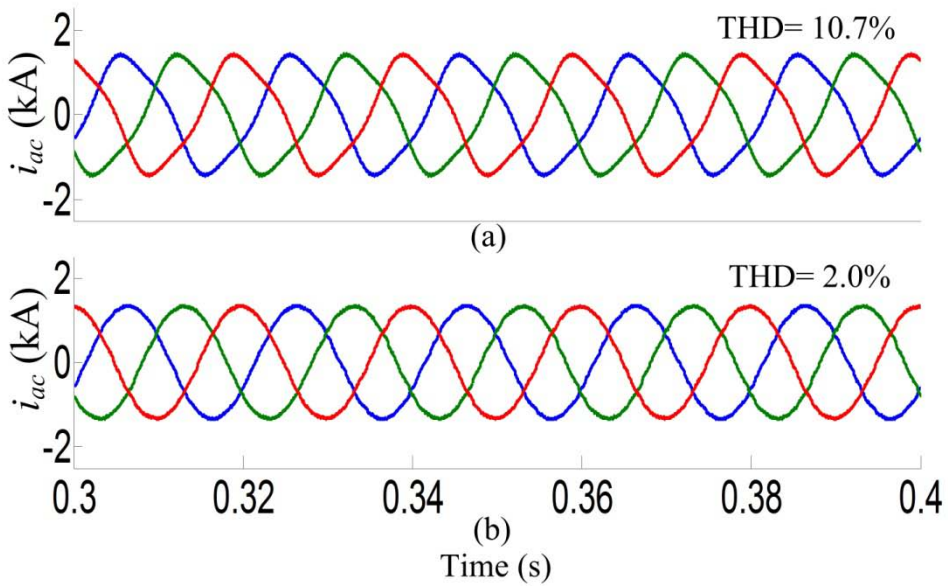


Fig. 5-9 Simulated 3-phase ac currents when ac-side transformers have grounded wye connection. (a) without deadbeat control; (b) under closed-loop deadbeat control

5.5.2 Test on Capability of Deadbeat to Protect MMC against Ground Fault

Under deadbeat control, the ac phase current (red) tracks the current reference (blue) even when the severe single-line to ground fault occurs at PCC during 0.8s $\leq t \leq$ 0.9s as shown in Fig. 5-10. This is because the measured voltage at the point of common connection $v_{PCC}(t)$ is feed-forward as shown in Fig. 5-1(a). As $v_{PCC}(t)$ drops to ground voltage, the ac-side voltage $v(t)$ in Fig. 5-1(a) consists only of $(U_{ref}/U_{dc})\cos(\omega t+\delta)$ of T_6. The ac-side voltage $v(t)$ drops to a value just sufficient to drive $i_c(t)$ across L and R. The simulation result verifies the fast response of closed-loop deadbeat control. The ac current tracks the reference within half period.

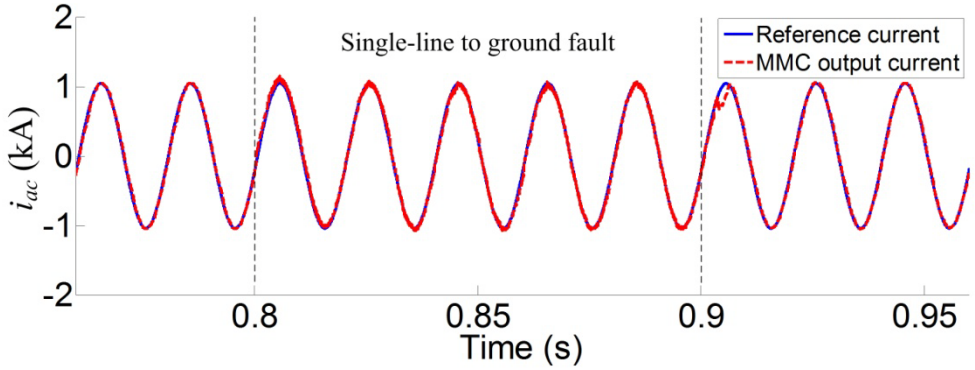


Fig. 5-10 Ac current of one MMC phase tracking Current Reference during a single-line to ground fault 0.8$s \leq t \leq$0.9s

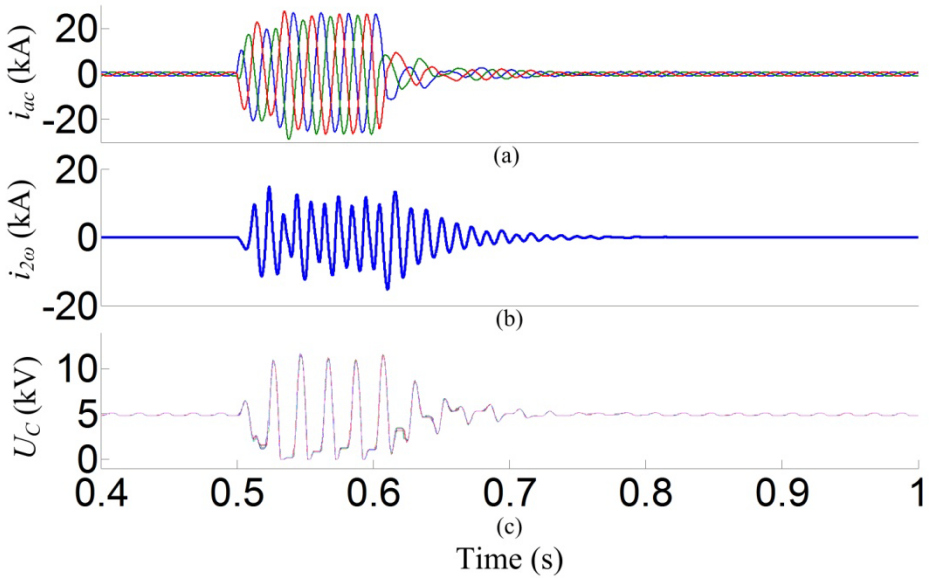


Fig. 5-11 Robustness test: 3-phase line-to-ground short circuit 0.5s ≤ t ≤ 0.6s. Feed-forward elimination activated, Deadbeat not activated. (a) 3-phase ac current; (b) 2nd harmonic current component; (c) voltages across capacitor (12 sub-modules superposed)

5.5.3 Robustness Test on Feed-forward 2nd Harmonic Elimination

Fig. 5-11 displays in (a) the 3-phase current, in (b) the second harmonic current $i_{2\omega}(t)$ of (7), in (c) $U_c(t)$, the capacitor voltage in each sub-module of phase a of the upper arm. Because deadbeat is not activated, the 3-phase ac currents reach very high values when a severe 3-phase line-to-ground fault at PCC is simulated between t=0.5s and t=0.6s. Although the 2nd and low frequency harmonics in (b) and (c) are reduced by feed-forward elimination, the fault currents charge the capacitors to levels above the voltage rating of IGBTs.

5.5.4 Test showing 2nd Harmonic Feed-forward & Feedback Elimination

In the test of Fig. 5-12, harmonic elimination has not been activated until t=0.4s. Fig. 5-12 shows in (a) the 3-phase ac currents, (b) differential mode current i_{diff}, (c) U_c, the voltage across one sub-module capacitor. In (c), the voltage U_c fluctuates around the 5 kV average as the capacitor is charged by the 50 Hz of 0.5 i_{ac} and the 2^{nd} and even harmonics of i_{diff}.

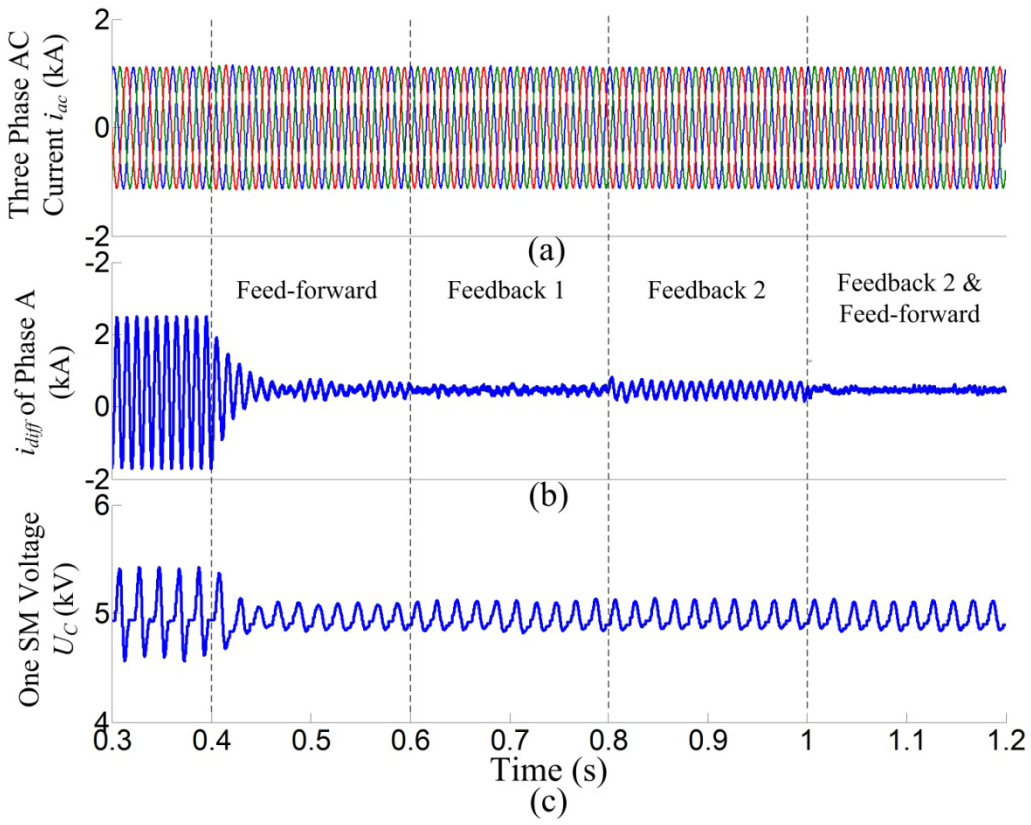


Fig. 5-12 2nd harmonic current elimination by feed-forward; feedback 1; feedback 2; then feedback 2 & feed-forward. (a) 3-phase MMC output currents; (b) differential mode current i_{diff} of phase a; (c) capacitor voltage of one sub-module of phase a, upper arm

At t=0.4s, feed-forward, based on (5-26), is activated. The reduction of 2nd harmonic, associated with '*X*' in Table 3-III, is apparent in (b) and (c). At t=0.6s, feed-forward method is disabled, instead, feedback 1 of Fig. 5-6 (a) is activated. At t=0.8s, feedback 2 using complement notch filter of Fig. 5-7 (a) is activated to replace feedback 1. At t=1.0s, feed-forward method is activated to reduce 2nd harmonic circulating current together with feedback 2. The simulation result shows that all the low-order harmonic reduction methods can reduce 2nd harmonic circulating current effectively. Feed-forward contributes by first reducing the size of the "error" before the feedback stage. Thus the gain of the negative feedback stage does not have to be large. One rule of the thumb is not to use large feedback gain to avoid instability. The simulation demonstrates that MMC accepts both feed-forward and feedback so that should one signal is lost, low frequency harmonics continue to be reduced.

5.5.5 Test showing Deadbeat protecting 2nd Harmonic Feed-forward & Feedback Elimination

The graphs displayed in Fig. 5-13 are of the same variables as in Fig. 5-12. In addition to the feedback 2 & feed-forward 2nd harmonic elimination of Fig. 5-12, deadbeat is activated. At t=0.6s, the current references of MMC step down to display the fast response of deadbeat and this is shown in Fig. 5-13. A 3-phase line-to-ground fault at PCC is simulated during $0.8s \leq t \leq 0.9s$. The simulation shows that deadbeat control keeps the ac current at values set by the current references as shown in Fig. 5-13 (a). Therefore in spite of the fault, differential mode current i_{diff} in Fig. 5-13 (b) and U_c in Fig. 5-13 (c) are kept at safe values.

5.6 Conclusion

This chapter shows that MMC can simultaneously implement deadbeat and low frequency elimination by feed-forward and feedback. With deadbeat, MMC becomes a reference current regulator; the ac currents in tracking the current references do not rise to destructively large values during ac faults. Likewise, inherent MMC harmonic currents on the ac side cannot flow. This frees MMC from the necessity of having delta or open wye connected transformers—a measure presently taken to suppress the aforesaid MMC 3rd harmonics.

Following Chapter 4, this chapter shows that the 2nd and other low-order harmonics proliferated by the 2nd harmonic current can be reduced by feed-forward and feedback, singly or jointly. Deadbeat in preventing large fault currents to overcharge the capacitor voltages ensures the viability of the elimination methods.

The methods developed have multiple safeguards in harmonic elimination. Eliminating 2nd harmonics at the source by a combination of feed-forward and feedback offers enhanced reliability. The elimination reduces the even harmonics on the dc side and the 3rd and odd harmonics on the ac side which are proliferated by the 2nd harmonic. In addition deadbeat suppresses harmonics on the ac side.

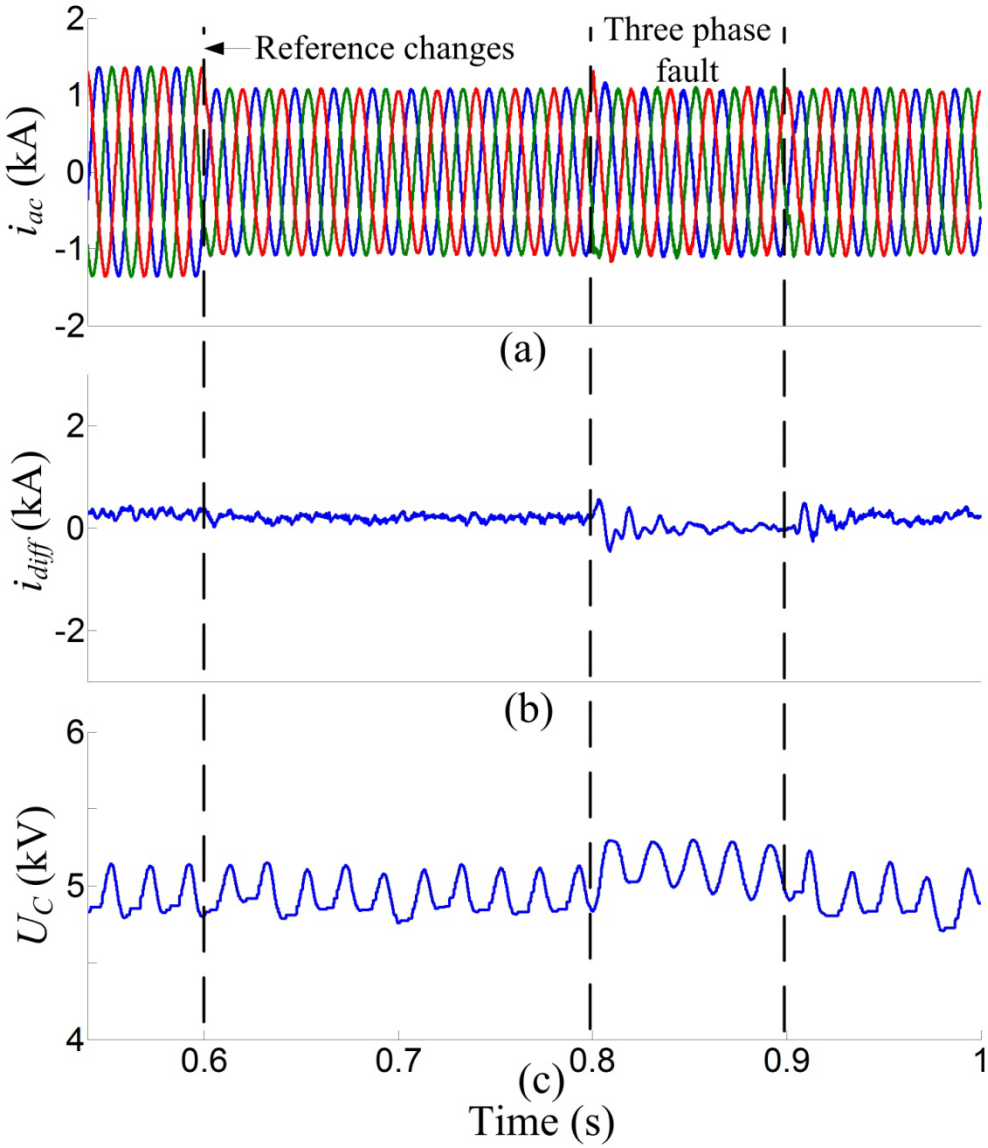


Fig. 5-13 Performance of the 2nd harmonic current elimination method when current reference changes at time 0.6s and under 3-phase line-to-ground fault condition (from time 0.8s~0.9s). (a) three phase MMC output currents; (b) differential mode current i_{diff} of phase a; (c) capacitor voltage of one sub-module of phase a, upper arm

Chapter 6 MMC Ultra HVDC and Multi-Terminal HVDC

6.1 Introduction

MMC is considered as belonging to the VSC family, and thus its suitability for multi-terminal HVDC operation is anticipated. In fact, there is a claim, witnessed by a third party, that a three-terminal MMC dc grid ±160kV/200MW-100MW-50MW has been commissioned in December 2013.

As understanding of the properties of MMC unfolds, it is now apparent that its operation is not based on "chopping" the dc capacitor voltage into a time-series of positive and negative voltage pulses of variable pulse widths for each of the three phases. In MMC, the phase-shifted triangular carrier PWM technique is used to determine the numbers of sub-modules (and the capacitors in them) to be connected in series to form the upper and lower arms of each phase. Therefore, the operation of MMC is based on capacitor modulation rather than pulse width modulation.

In the perspective of capacitor modulation, harmonic function analysis in Chapter 3 shows that the equivalent circuit of MMC consists of ideal voltage sources connected in series in both the ac side and the dc side. The dc side equivalent circuit of line-commutated thyristor (LCC) HVDC is also a voltage source and a pole of Ultra HVDC consists of 8 stations connected in series. Therefore MMC stations have the potential for this market. This chapter presents successful simulations of 4 MMC stations to form a single pole system, thus validating the prediction.

Multi-terminal HVDC has been associated with VSC since their dc sides are modeled as ideal current sources. Therefore, MMC having ideal voltage sources as equivalent circuits on the dc side raises questions on how they can be connected in parallel to be successful as a multi-terminal HVDC. Table 3-II and Table 3-III of Chapter 3 show that the dominant line frequency ideal voltage source T_{ac} on the ac side has a counter-part ideal

voltage source T_{dc} on the dc side which satisfies power balance $T_{ac}i_{ac} \Leftrightarrow T_{dc}I_d$. For ac power $T_{ac}i_{ac}$, there is a current $I_d = T_{ac}i_{ac}/T_{dc}$ injected at the location of the dc side ideal voltage T_{dc} in the same way as current injected by a VSC station.

This chapter is organized as follows: Section 6.2 develops the analysis of the combined ac-dc systems at the fundamental frequency. Section 6.3 shows that series-connected MMC stations have a future in Ultra HVDC. MMC multi-terminal HVDC and its power flow calculation based on composite ac-dc system are presented in Section 6.4. Section 6.5 introduces the control strategy used in MMC Ultra HVDC and MMC multi-terminal HVDC. As an MMC station has to be pre-charged to a desired dc voltage value to put into operation, this section includes the start-up stage to charge the MMC smoothly. Simulation results verify the claims and predictions in Section 6.6. Section 6.7 presents conclusions.

6.2 Composite AC Side and DC Side Load Flow

Attention is drawn to the symbols in *List of symbols* as they facilitate following the formulas in Table 3-II and Table 3-III of Chapter 3. The control reference used to modulate the ac voltage is $U_{ref}cos(\omega t+\delta)$. The ac current is $I_{ac}cos(\omega t+\varphi_{ac})$ with direction shown by the arrows in Fig. 3- 1. Because the 2nd and 3rd harmonic terms in Table 3-II and Table 3-III are made negligibly small by (i) using high capacitances in the sub-modules, or (ii) by feed-forward or feedback reduction and (iii) by blocking the 3rd harmonic with delta transformer or ungrounded wye connections, this section is left with the line frequency voltages on the ac side and the dc on the dc side. Terms with U_{dc}^2 in the denominators are also considered negligibly small.

Dominant Equivalent Circuit of MMC

Fig. 6-1 is the resultant equivalent circuit, taken from the dominant dc and fundamental frequency terms. Above the equivalent circuit is a composite diagram of the ac side voltage phasors and the current phasor (fundamental frequency). Scale is not followed to allow T_4, which is negligibly small, to be represented.

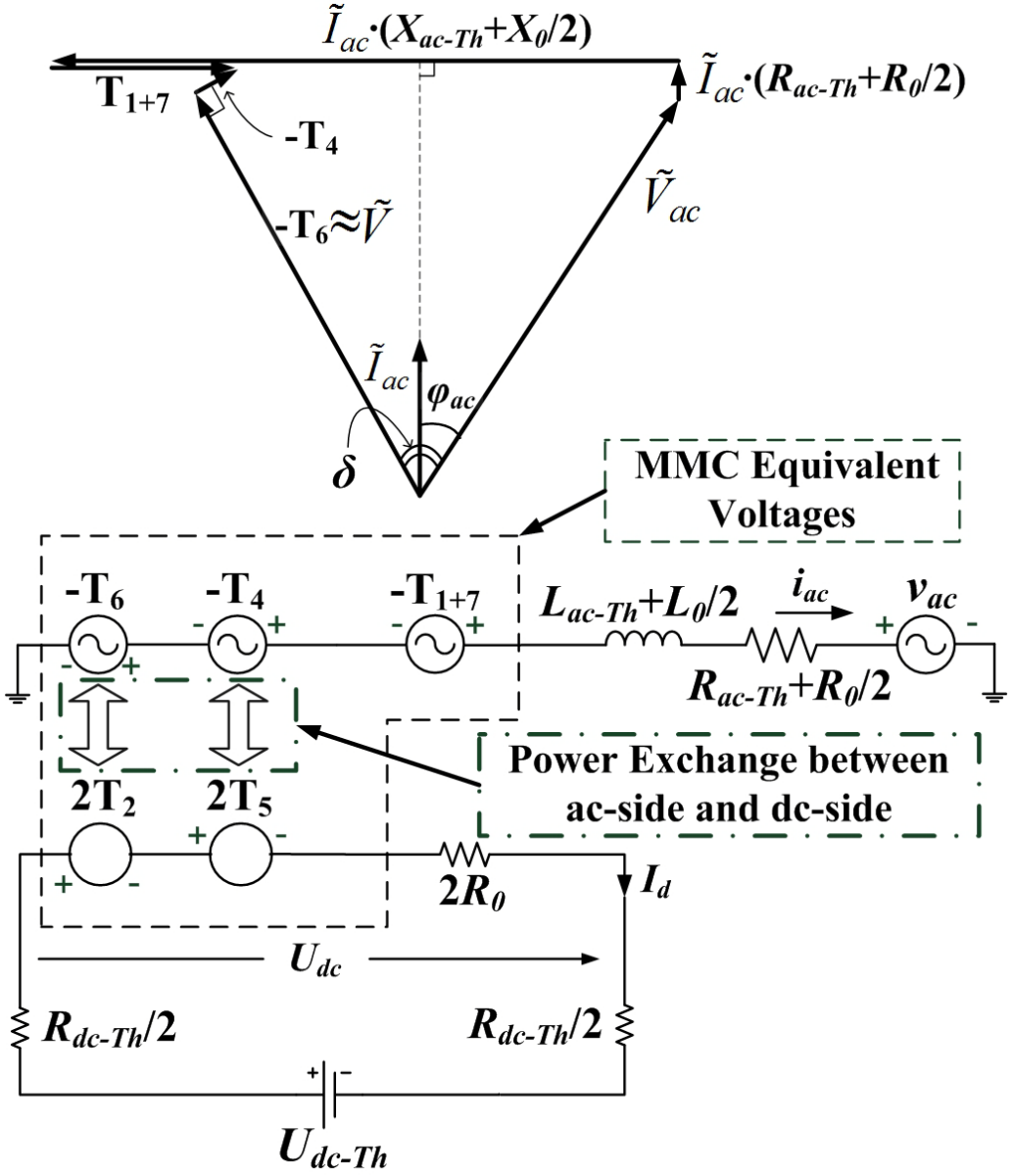


Fig. 6-1 One phase of MMC composite voltage and current phasor diagram (not to scale) and resultant equivalent circuit, taken from the dominant dc and fundamental frequency terms

Counterpart Voltages of ac-to-dc power balance

Ac voltage T_6 in Table 3-II has a dc voltage counterpart T_2 in Table 3-III through *average* power balance: $T_6 i_{ac} \Leftrightarrow 2T_2 I_d$, Fig. 6-1 places T_6 right above its dc counterpart T_2. Although they are very small numerically, the existence of counterpart voltages ($-T_4$, $2T_5$), which also satisfies ac-to-dc power balance, constitutes a strong mathematical check that the capacitor modulation derivation is correct.

Dominant MMC Voltages on ac and dc sides

In Fig. 6-1, the dominant dc side voltage is $2T_2=U_{dc}$.

From Table 3-III,

$$U_{dc}=\frac{N}{C}\int_{-\infty}^{t}[\frac{I_d}{2}-\frac{U_{ref}I_{ac}}{4U_{dc}}\cos(\delta-\varphi_{ac})]d\tau \tag{6-1}$$

Equation (6-1) implements average single phase *ac-to-dc power balance* because when U_{dc} reaches a constant value, ac power $0.5U_{ref}I_{ac}cos(\delta-\varphi_{ac})$ is equal to dc power $U_{dc}I_d$.

In Fig. 6-1, T_6 is the ac voltage produced by the modulating signal. It is approximately equal to MMC ac output voltage $v(t)$ produced by the voltage reference, $0.5U_{ref}cos(\omega t+\delta)$, in the modulating signals.

$$T_6=-\frac{m}{2}\cos(\omega t+\delta)U_{dc}\approx -v(t) \tag{6-2}$$

where the modulation index m is

$$m=\frac{2U_{ref}}{U_{dc}} \tag{6-3}$$

The reference signal of the modulating signal is amplified by the dc side voltage U_{dc}.

AC Voltage from I_d

The fundamental frequency voltage component from I_d is T_4. T_5 is its dc counter-part. T_4 and T_6 are 90 degrees apart and are illustrated in the phasor diagram of Fig. 6-1. Unlike T_6, T_4 is not amplified by U_{dc} of (6-1) and is numerically small. As both T_4 and T_5 are numerically small, they can be neglected.

Capacitive Reactance Voltage

The fundamental frequency components T_1 and T_7 together form T_{1+7}. Because T_{1+7} lags the ac current $I_{ac}cos(\omega t+\varphi_{ac})$ by 90 degrees, it is a capacitive reactance voltage. In Fig. 6-1, T_{1+7} is drawn in the opposite direction to the inductive reactance of $\omega(L_{ac-Th}+0.5L_0)$. Because T_1 and T_7 are reactance voltages, they do not have dc counter-parts. Neglecting this T_{1+7} term results in an inaccurate quantitative model of MMC.

AC Side Power

In Fig. 6-1, $\tilde{V}_{ac}$ is the Thevenin Voltage and $R_{ac-Th}+jX_{ac-Th}$ is the Thevenin Impedance on the ac side of the MMC station. The total equivalent impedance on the ac side is:

$$R+jX=(R_{ac-Th}+\frac{R_0}{2})+j[X_{ac-Th}+\frac{X_0}{2}-\frac{N}{8\omega C}(1+\frac{m^2}{8})] \tag{6-4}$$

The terms $0.5R_0$, $0.5L_0$ are shown in Fig. 6-1. The capacitive reactance voltage in (6-4) comes from T_{1+7} .

Writing $\tilde{V}$ and $\tilde{V}_{ac}$ as the MMC ac side output voltage phasor and ac system voltage phasor respectively, from (6-2)

$$\tilde{V} = \frac{m}{2}[\cos\delta + j\sin\delta]U_{dc} \tag{6-5}$$

Assuming the phase angle of ac system voltage to be zero,

$$\tilde{V}_{ac} = V_{ac}[\cos 0^\circ + j\sin 0^\circ] = V_{ac} \tag{6-6}$$

For inverter operation, KVL on the ac side is:

$$\tilde{V} = (R + jX)\tilde{I}_{ac} + \tilde{V}_{ac} \tag{6-7}$$

Solving for the current in (6-7)

$$\tilde{I}_{ac} = \frac{\tilde{V} - \tilde{V}_{ac}}{(R + jX)} \tag{6-8}$$

The complex power at the ac terminals is

$$S = \frac{3}{2}(\tilde{V}\tilde{I}_{ac}^{\ *}) = P_{ac} + jQ_{ac} \tag{6-9}$$

$$P_{ac} = \frac{3\frac{m}{2}U_{dc}(XV_{ac}\sin\delta + R\frac{m}{2}U_{dc} - V_{ac}R\cos\delta)}{2(R^2 + X^2)} \tag{6-10}$$

$$Q_{ac} = \frac{3\frac{m}{2}U_{dc}(X\frac{m}{2}U_{dc} - V_{ac}X\cos\delta - RV_{ac}\sin\delta)}{2(R^2 + X^2)} \tag{6-11}$$

DC Side Power

On the dc side, it is assumed the MMC terminal voltage is U_{dc}. In Fig. 6-1, the dc network is represented by the dc side Thevenin Voltage $U_{dc\text{-}Th}$ and Thevenin resistance $R_{dc\text{-}Th}$.

For operation as a 3-phase MMC inverter

$$U_{dc} = U_{dc-Th} - R_{dc-Th}I_{dc} \tag{6-12}$$

$$I_{dc} = \frac{U_{dc-Th} - U_{dc}}{R_{dc-Th}} \tag{6-13}$$

Ac to dc power balance (assuming no power loss)

$$U_{dc} I_{dc} = P_{ac} \tag{6-14}$$

$$\frac{P_{ac}}{U_{dc}} = \frac{U_{dc-Th} - U_{dc}}{R_{dc-Th}} \tag{6-15}$$

Substituting P_{ac} from (6-10)

$$\frac{3\frac{m}{2}(XV_{ac}\sin\delta + R\frac{m}{2}U_{dc} - V_{ac}R\cos\delta)}{2(R^2 + X^2)} = \frac{U_{dc-Th} - U_{dc}}{R_{dc-Th}} \tag{6-16}$$

For open loop control, specified by m and δ, the unknown U_{dc} can be solved from (6-16):

$$U_{dc} = \frac{\frac{U_{dc-Th}}{R_{dc-Th}} + \frac{3m(V_{ac}R\cos\delta - V_{ac}X\sin\delta)}{4(R^2 + X^2)}}{\frac{3Rm^2}{8(R^2 + X^2)} + \frac{1}{R_{dc-Th}}} \tag{6-17}$$

Substituting (6-17) in the power balance of (6-14), the dc terminal is virtually injecting a dc current

$$I_{dc} = P_{ac}\frac{\frac{3Rm^2}{8(R^2 + X^2)} + \frac{1}{R_{dc-Th}}}{\frac{U_{dc-Th}}{R_{dc-Th}} + \frac{3m(V_{ac}R\cos\delta - V_{ac}X\sin\delta)}{4(R^2 + X^2)}} \tag{6-18}$$

into the dc grid much in the same way as the ideal current source equivalent circuit in VSC. This feature makes MMC suitable for parallel connection in multi-terminal MMC HVDC.

6.3 Ultra HVDC by Series Connected MMC

From MMC equivalent circuit shown in Fig. 3- 2, the dc side of each phase consists of dc or even harmonic ideal voltage sources T_2, T_3, T_5 and T_8. Because the even harmonic currents of balanced 3 phase sum to zero and because the triplen harmonic currents are prevented from flowing by delta or open wye transformer connections, only the dc current I_{dc} emerges from the dc bus of a single MMC station. Therefore, MMC stations are suitable for series connection as in the single pole, point-to-point HVDC link illustrated in Fig. 6-2. MMC Station 1 and MMC Station 2 at one end and MMC Station 3 and MMC Station 4 at the other end are connected in series to double the dc voltage of the dc transmission line.

Manufacturers have the know-how to insulate transformer windings and bushings with high dc voltage offsets. For example, Ultra HVDC uses four thyristor stations in series at each end to reach 800kV DC. Eventually, higher voltages based on four MMC stations in series will be considered. MMC has the advantages over classic thyristor HVDC in that: (i) there is no equivalent to commutation failure; (ii) power reversal takes place by reversal of current direction; (iii) costly dc side and ac side filters are not required. In addition, there is the possibility of configuring multi-terminal Ultra HVDC by MMC stations.

When the dc voltages of the 4 MMC stations are U_{dc-n}, n=1, 2, 3, 4 from KVL, the current of the dc transmission line is

$$I_{dc-line} = \frac{\sum_{n=1}^{4} U_{dc-n}}{R_{dc-line}} \tag{6-19}$$

When U_{dc-n} n=1, 2, 3, 4 have harmonic voltages, the harmonic current components in $I_{dc-line}$ which flow across the transmission line impedances flow through all the MMC stations.

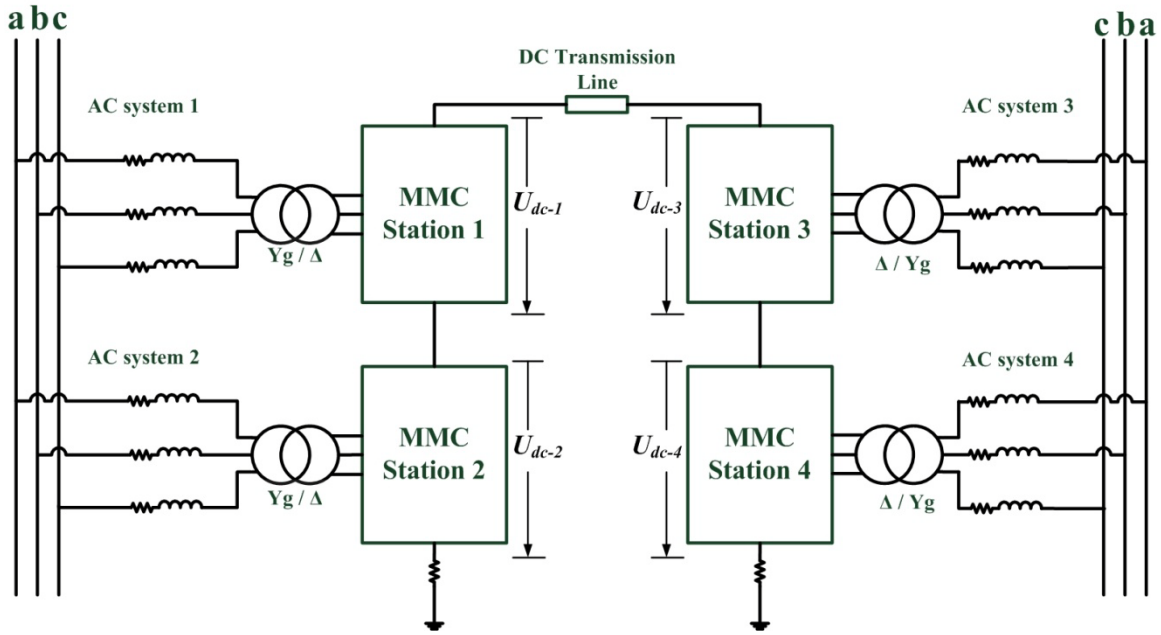


Fig. 6-2 Single-pole, point-to-point HVDC transmission based on series connected MMC

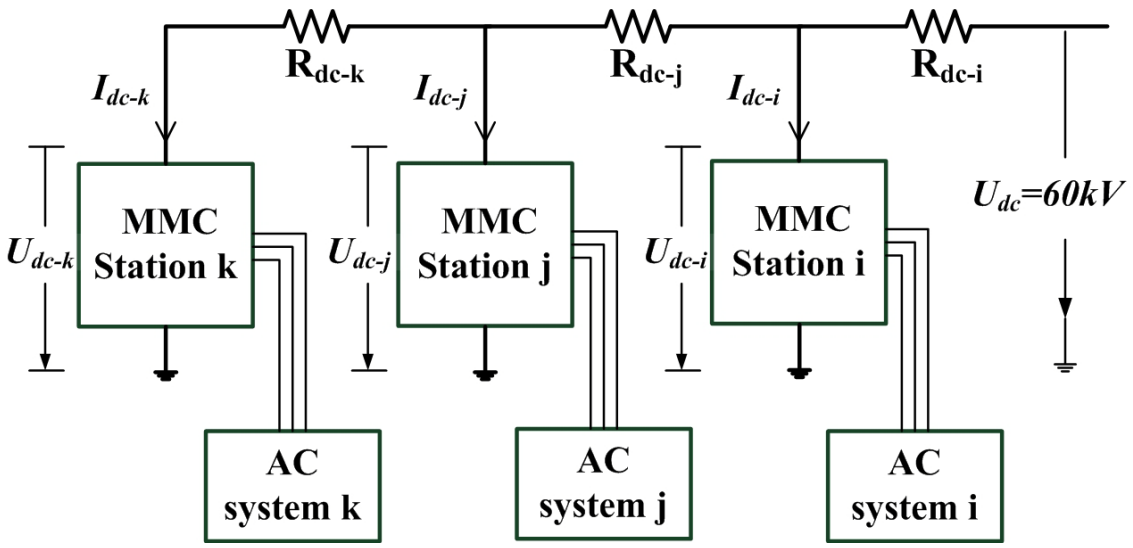


Fig. 6-3 Radial dc line of MMC stations i, j, k connected to DC Voltage Regulator

6.4 Multi-Terminal HVDC by Parallel Connected MMC

DC grids can be radial, mesh or combinations of radial and mesh. The example considered in this chapter is a radial dc grid which consists of 3 MMC stations connected to a DC Voltage Regulator represented by an ideal voltage source U_{dc}. MMC stations i, j, and k, with unknown dc terminal voltages $U_{dc\text{-}i}$, $U_{dc\text{-}j}$ and $U_{dc\text{-}k}$, are interconnected by equivalent resistances $R_{dc\text{-}i}$, $R_{dc\text{-}j}$, $R_{dc\text{-}k}$ as illustrated by Fig. 6-3. $I_{dc\text{-}i}$, $I_{dc\text{-}j}$ and $I_{dc\text{-}k}$ refer to the individual MMC station dc current.

On the ac side, the total resistances are $R_{ac\text{-}i}$, $R_{ac\text{-}j}$, $R_{ac\text{-}k}$ and the total reactances are $X_{ac\text{-}i}$, $X_{ac\text{-}j}$, $X_{ac\text{-}k}$. The modulation indexes of MMC station i, j and k are m_i, m_j, m_k and the corresponding reference voltage angles are δ_i, δ_j, δ_k. Ac system voltage magnitudes are $V_{ac\text{-}i}$, $V_{ac\text{-}j}$ and $V_{ac\text{-}k}$ and with angle $\delta_{ac\text{-}i}=\delta_{ac\text{-}j}=\delta_{ac\text{-}k}=0°$. The active powers at the ac terminals are denoted by P_i, P_j, P_k.

According to Kirchhoff's Current Law (KCL),

$$I_{dc-i}=\frac{U_{dc}-U_{dc-i}}{R_{dc-i}}+\frac{U_{dc-j}-U_{dc-i}}{R_{dc-j}} \tag{6-20}$$

$$I_{dc-j}=\frac{U_{dc-i}-U_{dc-j}}{R_{dc-j}}+\frac{U_{dc-k}-U_{dc-j}}{R_{dc-k}} \tag{6-21}$$

$$I_{dc-k} = \frac{U_{dc-j} - U_{dc-k}}{R_{dc-k}} \tag{6-22}$$

Multiplying (6-20), (6-21) and (6-22) with $U_{dc\text{-}i}$, $U_{dc\text{-}j}$ and $U_{dc\text{-}k}$ respectively and neglecting the power loss,

$$U_{dc-i} I_{dc-i} = U_{dc-i} \frac{U_{dc} - U_{dc-i}}{R_{dc-i}} + U_{dc-i} \frac{U_{dc-j} - U_{dc-i}}{R_{dc-j}} = P_i \tag{6-23}$$

$$U_{dc-j} I_{dc-j} = U_{dc-j} \frac{U_{dc-i} - U_{dc-j}}{R_{dc-j}} + U_{dc-j} \frac{U_{dc-k} - U_{dc-j}}{R_{dc-k}} = P_j \tag{6-24}$$

$$U_{dc-k} I_{dc-k} = U_{dc-k} \frac{U_{dc-j} - U_{dc-k}}{R_{dc-k}} = P_k \tag{6-25}$$

Substituting the active power equation (6-10) into (6-23), (6-24) and(6-25), we have

$$\begin{aligned} & U_{dc-i} \frac{U_{dc} - U_{dc-i}}{R_{dc-i}} + U_{dc-i} \frac{U_{dc-j} - U_{dc-i}}{R_{dc-j}} \\ & = \frac{3\frac{m_i}{2} U_{dc-i} (X_{ac-i} V_{ac-i} \sin\delta_i + R_{ac-i} \frac{m_i}{2} U_{dc-i} - V_{ac-i} R_{ac-i} \cos\delta_i)}{2(R_{ac-i}^2 + X_{ac-i}^2)} \end{aligned} \tag{6-26}$$

$$\begin{aligned} & U_{dc-j} \frac{U_{dc-i} - U_{dc-j}}{R_{dc-j}} + U_{dc-j} \frac{U_{dc-k} - U_{dc-j}}{R_{dc-k}} \\ & = \frac{3\frac{m_i}{2} U_{dc-j} (X_{ac-j} V_{ac-j} \sin\delta_j + R_{ac-j} \frac{m_j}{2} U_{dc-j} - V_{ac-j} R_{ac-j} \cos\delta_j)}{2(R_{ac-j}^2 + X_{ac-j}^2)} \end{aligned} \tag{6-27}$$

$$\begin{aligned} & U_{dc-k} \frac{U_{dc-j} - U_{dc-k}}{R_{dc-k}} \\ & = \frac{3\frac{m_i}{2} U_{dc-k} (X_{ac-k} V_{ac-k} \sin\delta_k + R_{ac-k} \frac{m_k}{2} U_{dc-k} - V_{ac-k} R_{ac-k} \cos\delta_k)}{2(R_{ac-k}^2 + X_{ac-k}^2)} \end{aligned} \tag{6-28}$$

Here, the ac side total resistance $R_{ac\text{-}i}$, $R_{ac\text{-}j}$, $R_{ac\text{-}k}$ and total reactance $X_{ac\text{-}i}$, $X_{ac\text{-}j}$, $X_{ac\text{-}k}$ are obtained from equation (6-4).

It is noted that each of the equations (6-26), (6-27) and (6-28) has a common dc voltage $U_{dc\text{-}i}$, $U_{dc\text{-}j}$ and $U_{dc\text{-}k}$ on the left-side and the right-side of each equation. Therefore, after cancelling the dc voltages, the three quadratic equations are reduced to three linear

equations. The voltages $U_{dc\text{-}i}$, $U_{dc\text{-}j}$ and $U_{dc\text{-}k}$ are solved from three simultaneous linear equations.

6.5 Control Strategy

The MMC overall control strategy applied in both the multi-terminal MMC HVDC and the MMC Ultra HVDC of this thesis mainly comprises of three parts: (i) Start-up stage control; (ii) Active power and reactive power control; (iii) 2nd harmonic circulating current reduction control. The control block diagram is shown in Fig. 6-4. When MMC station is ready to put into operation, the control mode switch connects to the start-up stage control to block or generate modulating signal of upper arm m_{uj} and lower arm m_{lj} of each phase (j=a, b, c). $U_{dc\text{-}m}$ denotes the measured dc voltage. After $U_{dc\text{-}m}$ reaches the expected value U_{dc}, the start-up stage is over and the control mode switch connects to active and reactive power control to put MMC station into normal operation. Since the harmonic reduction control has been discussed in detail in Chapter 4, this section is focusing on start-up stage control and power control.

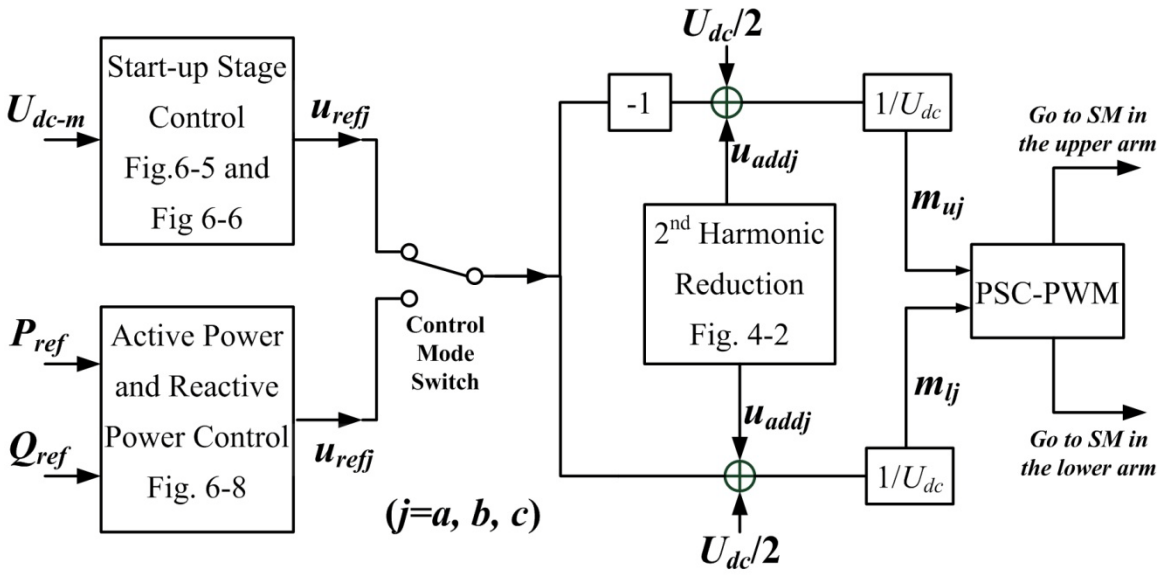


Fig. 6-4 Overall control block diagram

6.5.1 Start-up Stage Control

Before connecting to the HVDC network, MMC has to be pre-charged in the start-up stage. The system configuration and the current path when SM switch signals are blocked are shown in Fig. 6-5. In order to simplify the diagram, the currents driven by line voltage u_{ab} flowing through only one SM in each arm are depicted in Fig. 6-5. The current path in red or purple depends on the polarity of u_{ab}. Same in each phase, L_0 and R_0 denote the arm inductor and its equivalent resistance respectively. R_r represents the current limiting resistor of each phase.

Usually the start-up stage control requires three steps to reach the expected dc voltage:

1). Block all the SM switch signals and close ac breaker 1 to charge SM capacitors through the current limiting resistor R_r;

2). Close ac breaker 2 to bypass R_r and charge SM capacitors further;

3). Activate SM switch signals and charge the SM to desired value by control system.

During step one and two, the current flows through anti-parallel diodes to charge SM capacitors. According to basic circuit theory, the dc voltage reaches the peak line-to-line voltage on the ac side after step two is over. In order not to overcharge SM capacitors, it requires the ac line voltage to be smaller than the rated dc voltage.

Fig. 6-6 shows the control block diagram implemented in step three. $U_{dc\text{-}m}$ and U_{dc} denote measured dc voltage and reference dc voltage respectively. With the difference value between $U_{dc\text{-}m}$ and U_{dc}, proportional-integral (P-I) controller produces i_{dref} which is the direct axis (d-axis) reference current based on direct-quadrature (d-q) frame. Since start-up stage control only builds up desired dc voltage, the quadrature axis (q-axis) reference current i_{qref} is set to be zero. The inner current control loop applied in Fig. 6-6 is the same as the one in the decoupled P-Q control system which will be discussed in detail in section 6.5.2.

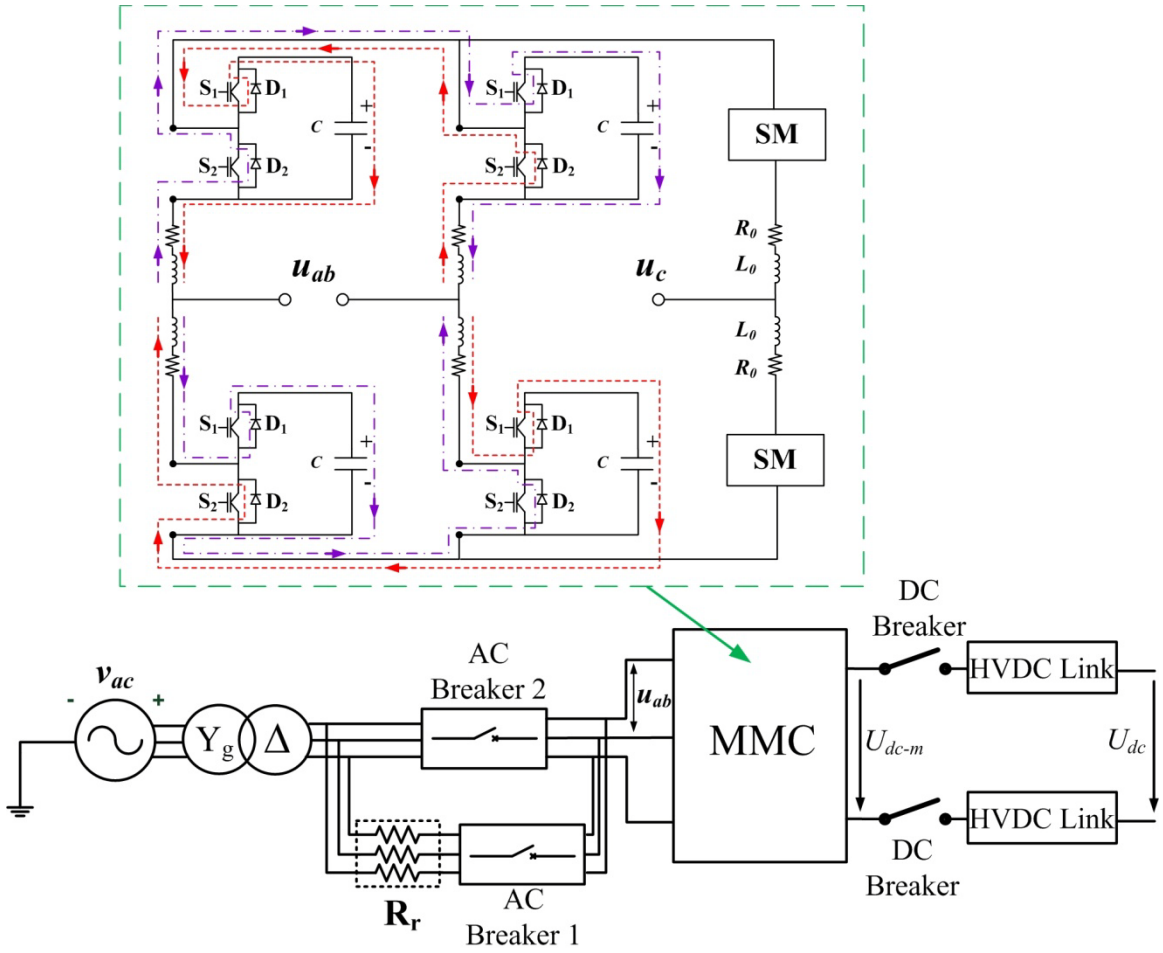


Fig. 6-5 Pre-charging current path when all SM switch signals are blocked

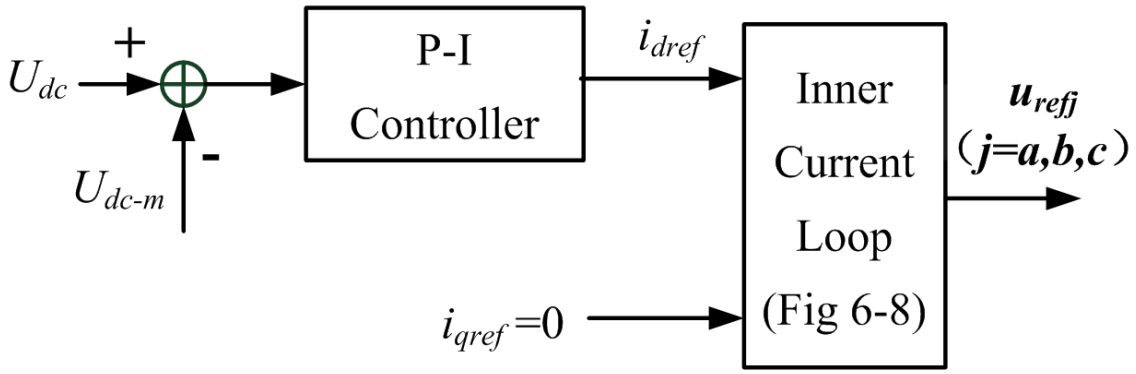


Fig. 6-6 MMC start-up stage control system

6.5.2 Decoupled P-Q Control

In order to control active power and reactive power independently, decoupled P-Q control is introduced in this section.

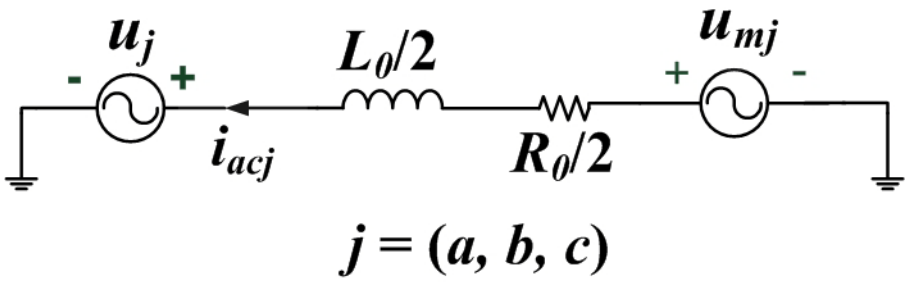


Fig. 6-7 3-phase MMC equivalent circuit on the ac side

In the 3-phase MMC equivalent circuit on the ac side shown in Fig. 6-7, the voltage u_{mj} represents MMC output voltage of phase j and u_j denotes ac system voltage of phase j (j=a, b, c). L_0 is the arm inductor and R_0 is its equivalent resistance. Ac current is represented by i_{acj} (j=a, b, c) and its direction is indicated in Fig. 6-7.

The essence of decoupled P-Q control is that the control system simplifies three phase ac quantities to two dc quantities by creating a d-q frame, where a 3-phase Phase Lock Loop (PLL) is required to ensure that the d-axis of the d-q frame is aligned with the ac system voltage.

After d-q transformation (also known as Park's transformation), (u_{ma}, u_{mb}, u_{mc}) and (u_a, u_b, u_c) are transformed to (u_{md}, u_{mq}) and (u_d, u_q) respectively (see Appendix B). The subscript d and q denote d-axis and q-axis of the d-q frame.

Now the instantaneous power on the ac system side can be written as:

$$S = \frac{3}{2}UI^* = \frac{3}{2}(u_d + ju_q)(i_{acd} + ji_{acq})^* = P + jQ \tag{6-29}$$

where S represents the complex power, superscript '*' denotes the complex conjugate.

Active power P is,

$$P = \mathrm{Re}[\frac{3}{2}(u_d + ju_q)(i_{acd} - ji_{acq})] = \frac{3}{2}(u_d i_{acd} + u_q i_{acq}) \tag{6-30}$$

Reactive power Q is,

$$Q = \mathrm{Im}[\frac{3}{2}(u_d + ju_q)(i_{acd} - ji_{acq})] = \frac{3}{2}(-u_d i_{acq} + u_q i_{acd}) \tag{6-31}$$

When d-axis is aligned with u_a (the ac system voltage of phase a), u_q becomes zero (u_q=0). The active power P and reactive power Q become

$$\begin{cases} P = \dfrac{3}{2} u_d i_{acd} \\ Q = -\dfrac{3}{2} u_d i_{acq} \end{cases} \tag{6-32}$$

In equation (6-32), u_d can be obtained from the d-q transformation of measured ac system voltage (u_a, u_b, u_c). By controlling i_{acd} and i_{acq} separately, independent control of active power P and reactive power Q is realized.

In the dq frame, it follows:

$$\begin{bmatrix} u_{md} \\ u_{mq} \end{bmatrix} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_{acd} \\ i_{acq} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{acd} \\ i_{acq} \end{bmatrix} + R \begin{bmatrix} i_{acd} \\ i_{acq} \end{bmatrix} \tag{6-33}$$

where, $L=L_0/2$, $R=R_0/2$.

The value of the differential term in equation (6-33) can be replaced with a P-I controller output as follows:

$$L \frac{d}{dt} \begin{bmatrix} i_{acd} \\ i_{acq} \end{bmatrix} = K_p \begin{bmatrix} i_{dref} - i_{acd} \\ i_{qref} - i_{acq} \end{bmatrix} + K_i \int \begin{bmatrix} i_{dref} - i_{acd} \\ i_{qref} - i_{acq} \end{bmatrix} dt \tag{6-34}$$

where i_{dref} and i_{qref} are reference current in the d-q frame.

Substituting (6-34) into (6-33),

$$\begin{bmatrix} u_{mdref} \\ u_{mqref} \end{bmatrix} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_{acd} \\ i_{acq} \end{bmatrix} + K_p \begin{bmatrix} i_{dref} - i_{acd} \\ i_{qref} - i_{acq} \end{bmatrix} + K_i \int \begin{bmatrix} i_{dref} - i_{acd} \\ i_{qref} - i_{acq} \end{bmatrix} dt + R \begin{bmatrix} i_{acd} \\ i_{acq} \end{bmatrix} \tag{6-35}$$

Thus, reference value of (u_{md}, u_{mq}) which is represented by (u_{mdref}, u_{mqref}) can be calculated by reference current (i_{dref}, i_{qref}), measured current (i_{acd}, i_{acq}) and measured ac system voltage (u_d, u_q).

Applying the control law (6-32) and (6-35), decoupled P-Q control is able to control the active power and reactive power independently by the reference current (i_{dref}, i_{qref}) in the d-q frame. Fig. 6-8 shows the decoupled P-Q control block diagram. Reference voltage (u_{mdref}, u_{mqref}) in the d-q frame is transformed to voltage u_{refj} in the stationary a-b-c frame by the following equations:

$$\begin{cases} U_{mag} = \sqrt{u_{mdref}^2 + u_{mqref}^2} \\ \delta = \tan^{-1}\left(\dfrac{u_{mqref}}{u_{mdref}}\right) \end{cases} \tag{6-36}$$

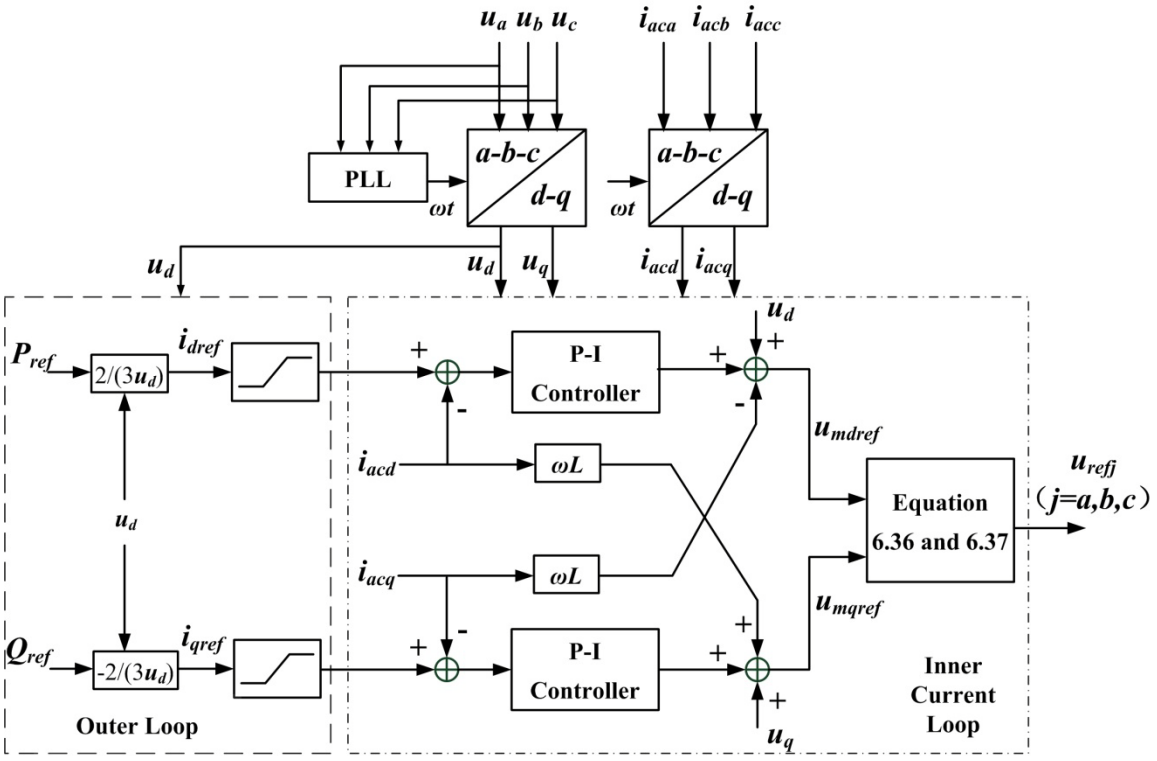


Fig. 6-8 Decoupled P-Q control block diagram

$$\begin{cases} u_{refa} = U_{mag}\cos(\omega t + \delta) \\ u_{refb} = U_{mag}\cos(\omega t + \delta - 120^{\circ}) \\ u_{refc} = U_{mag}\cos(\omega t + \delta - 240^{\circ}) \end{cases} \tag{6-37}$$

where U_{mag} and δ are the magnitude and the phase angle of the reference voltage in a-b-c frame respectively.

6.5.3 Voltage Equalizing Control for Series Connected MMC

When MMC stations are connected in series to build Ultra HVDC transmission, on the power dispatcher side, voltage equalizing control is required to balance dc voltages between the two series connected MMC stations. In Fig. 6-2, the MMC station 3 and 4 are working as power dispatcher. Equalizing consists of measuring the dc voltages of the upper station (station 3) and the lower station (station 4) and applying the active power of the stations to "null" the difference in voltage measurements by negative feedback shown in Fig. 6-9. The equalizer outputs $i'_{dref\text{-}3}$ and $i'_{dref\text{-}4}$ will be added up with $i_{dref\text{-}3}$ and $i_{dref\text{-}4}$ respectively to form the final reference current in the d-axis.

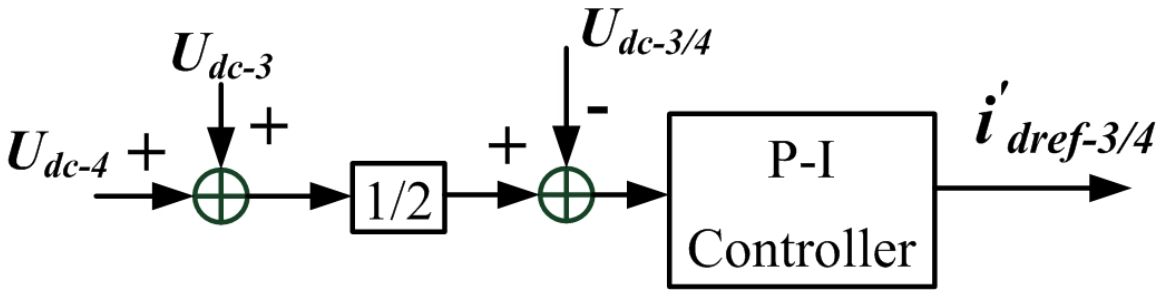


Fig. 6-9 Voltage equalizer of MMC connected in series

Table 6-I Parameters of the single MMC station and ac system

Parameter	Value	Parameter	Value
MMC station		AC system	
Nominal Power S_b	50 MW	AC Voltage (peak value)	25 kV
DC Reference Voltage of Each MMC station	60 kV	Current Limiting Resistor R_r	18 Ohm
Arm Inductor L_0	3 mH	Frequency f	50 Hz
Arm Resistance R_0	0.3 Ohm	$L_{ac\text{-}Th}$	10 mH
Capacitor	15 mF	$R_{ac\text{-}Th}$	0.5 Ohm

6.6 Simulation Results

The validation of load flow and performance of MMC Ultra-HVDC and MMC multi-terminal HVDC are evaluated in this section. Each of the MMC stations is based on the configuration of Fig. 2-1 (a) and all the tests are simulated in the Simulink/MATLAB environment. Parameters of each MMC station and its corresponding ac system are listed in Table 6-I. Since the 2nd harmonic circulating current reduction control has already been validated through a number of tests in Chapter 4, feed-forward and feedback to eliminate 2nd harmonics are not activated in all the simulation tests of this section. The filtering is accomplished by capacitors whose size is increased to 15mF.

6.6.1 Validation of AC Side and DC Side Load Flow

Validation of the equivalent circuit of Fig. 6-1 is established by Fig. 6-10 and Fig. 6-11 which show close agreement between the predictions of active power P and reactive power Q by equation (6-4), (6-10), (6-11) and (6-17) (calculated results) and

measurements of P and Q by detailed Simulink MMC model (simulation results). The tests are performed in open loop control and system parameters are listed in Table 6-I. P is varied by changing δ with the modulation index m kept constant at 1.0 in Fig. 6-10 and at 0.9 in Fig. 6-11. There is poor agreement when the capacitive voltage of T_{1+7} is not represented in (6-4). This is an important proof of the value of the formulas of Table 3-II and Table 3-III. Fig. 6-10 and Fig. 6-11 together show that for the same active power P, the reactive power Q can take a different value by control of modulation index m. The two degrees of control, m and δ, allow decoupled P, Q control to be implemented.

Although the agreement in Fig. 6-10 and Fig. 6-11 is good, it is still imperfect. This is because there are 'X' terms in T_4 and T_7 which are not represented in (6-4). As explained in Chapter 4, the 'X' terms proliferate from the second harmonic power of single-phase ac. When the 'X' terms are removed by eliminating the source by feed-forward as explained in Chapter 4 the agreement as shown in Fig. 6-12 is better than Fig. 6-11.

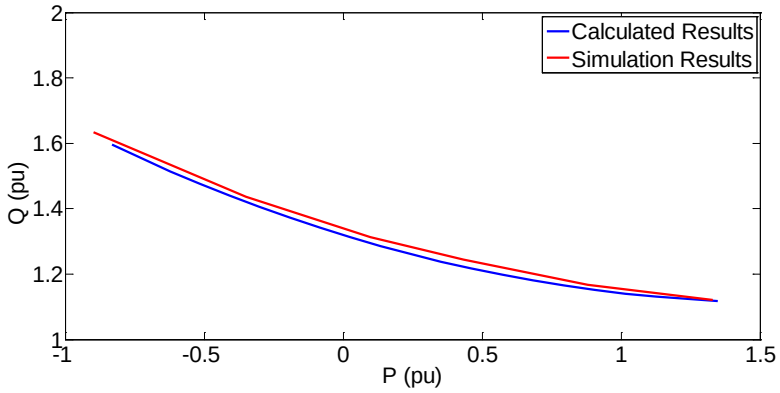


Fig. 6-10 Q-vs- P (capacitor size=15mF, U_{dc}=1.0 pu, m (modulation index) =1.0)

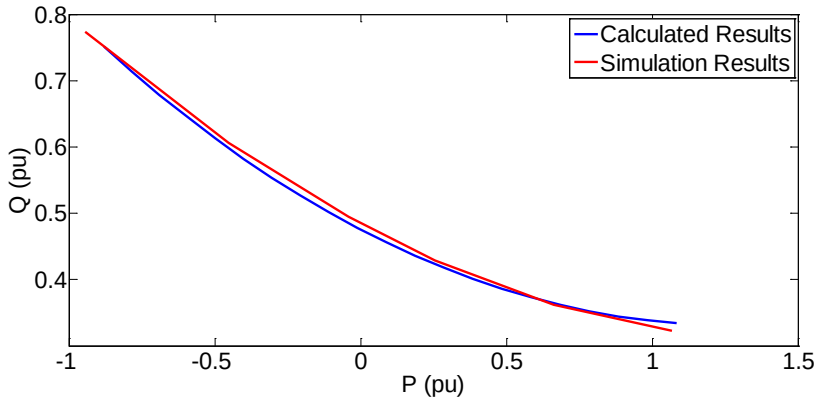


Fig. 6-11 Q-vs-P (capacitor size=15mF, U_{dc}=1.0 pu, m (modulation index) =0.9)

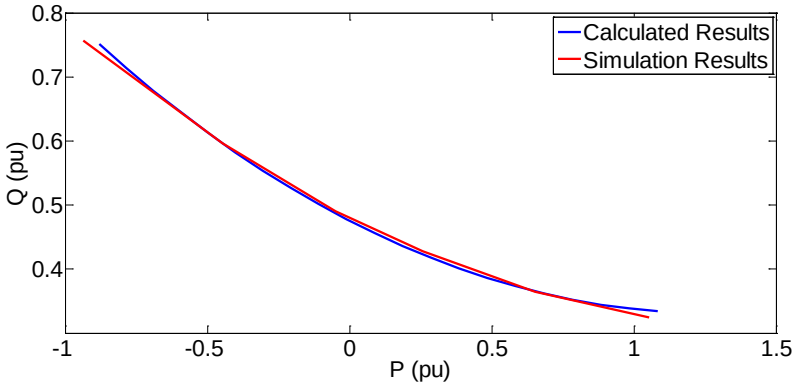


Fig. 6-12 *Q*-vs-*P* (capacitor size=15mF, U_{dc}=1.0 pu, *m* (modulation index) =0.9 with 2nd harmonic elimination)

6.6.2 Performance of Start-up Stage Control

The performance of the start-up stage control of MMC is shown in Fig. 6-13. For $t < 0.2$s, the MMC is isolated from both the ac and the dc side. At $t = 0.2$s, ac breaker 1 shown in Fig. 6-5 is closed, ac current charges SM capacitors through current limiting resistor R_r (R_r is 18 ohm in this test). After 0.6 seconds, SM capacitors are charged further more by closing ac breaker 2 to bypass resistor R_r.

At the time $t = 1.3$s, SM switching signals are activated and SM capacitors are charged to desired value by control strategy shown in Fig. 6-6. As shown in Fig. 6-13 (a), (b) and (c), the measured dc voltage and SM capacitor voltage are smoothly charged to the desired value with charging currents constrained within around ± 1 p. u. Fig. 6-13 (d) presents the active power (in solid blue line) and reactive power (in dashed red line) accompanied by the start-up pre-charging stage. The simulation results indicate that the current limiting resistor R_r and start-up stage controller are adequately designed. When dc voltage maintains at desired value, dc breaker can be closed and MMC is ready to put into operation.

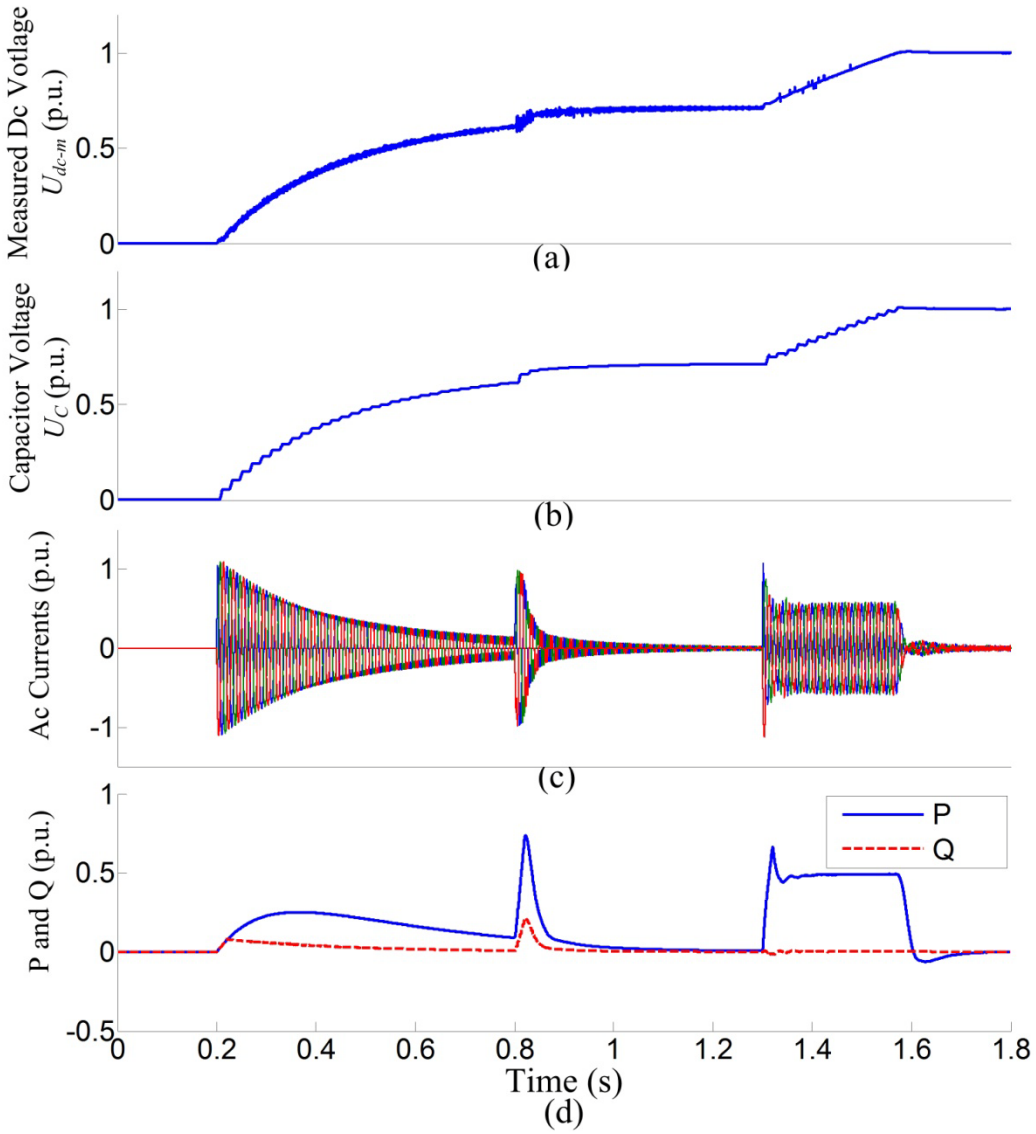


Fig. 6-13 Start up stage waveforms. (a) MMC dc voltage; (b) One SM capacitor voltage; (c) Three-phase ac currents i_{acj} (j=a, b, c); (d) Active power and reactive power MMC absorbed

6.6.3 Performance of MMC Ultra HVDC under Normal Conditions

A. Voltage Equalizer

Left to themselves the "Power Dispatchers" do not share the dc bus voltage equally. This is shown by the blue hatched lines in Fig. 6-14. Equalizing consists of measuring the dc voltages of the upper and the lower station and applying the active power of the stations to "null" the difference in voltage measurements by negative feedback shown in

Fig. 6-9. The red lines in Fig. 6-14 show that equal sharing is achieved by the equalizing control.

B. Power Reversal

The feasibility test makes use of simulation models of Fig. 2-1 (a) to represent MMC station 1 to MMC station 4. Table 6-I lists the principal parameters used in the simulations. The feedback control method of Station 1 and Station 2 maintain the dc voltages at the reference settings so that the terminal operates as a dc voltage regulator shown in Fig. 6-15 (a). Station 3 and 4 are "Power Dispatchers" shown in Fig. 6-15 (b).

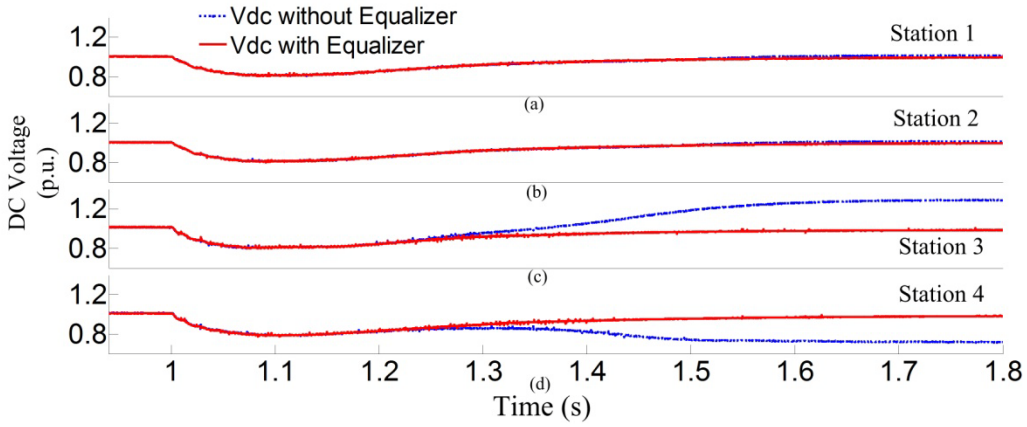


Fig. 6-14 DC voltage of Station 1, 2, 3 and 4 during reversal of power flow, activated at *t*=1.0s. Blue (hatched) line: without dc equalizing; red (solid) line: with dc voltage equalizing control

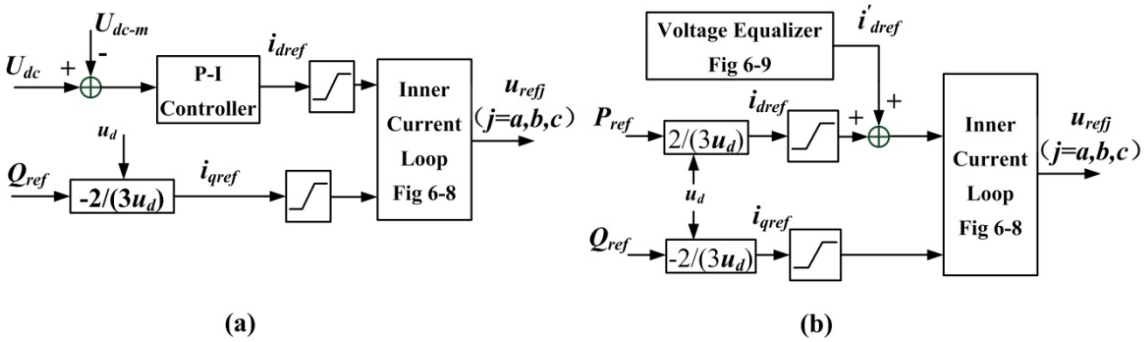


Fig. 6-15 Control methods of MMC Ultra-HVDC: (a) voltage regulator (Station 1 and 2); (b) power dispatcher (Station 3 and 4)

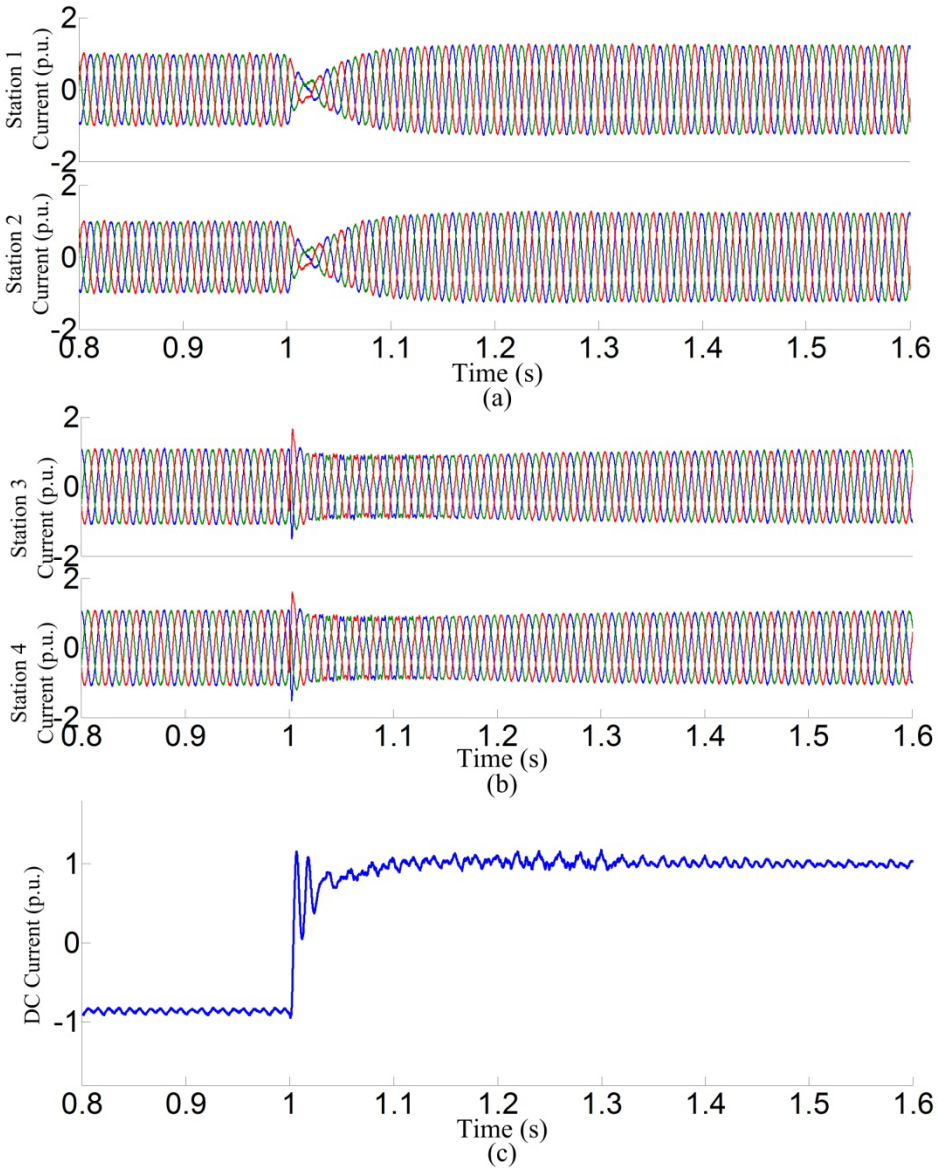


Fig. 6-16 3-phase ac currents of Station 1, 2, 3 and 4 and dc current; for a step command to reverse power flow.

Fig. 6-16 shows the simulation results of 3-phase ac currents of the 4 MMC stations and the dc current during a step reversal of power (activated at t=1s). The dc current changes from -0.9 pu to +1.0 pu.

6.6.4 Performance of MMC Multi-Terminal HVDC under Normal Conditions

A. Validation of Multi-Terminal MMC HVDC

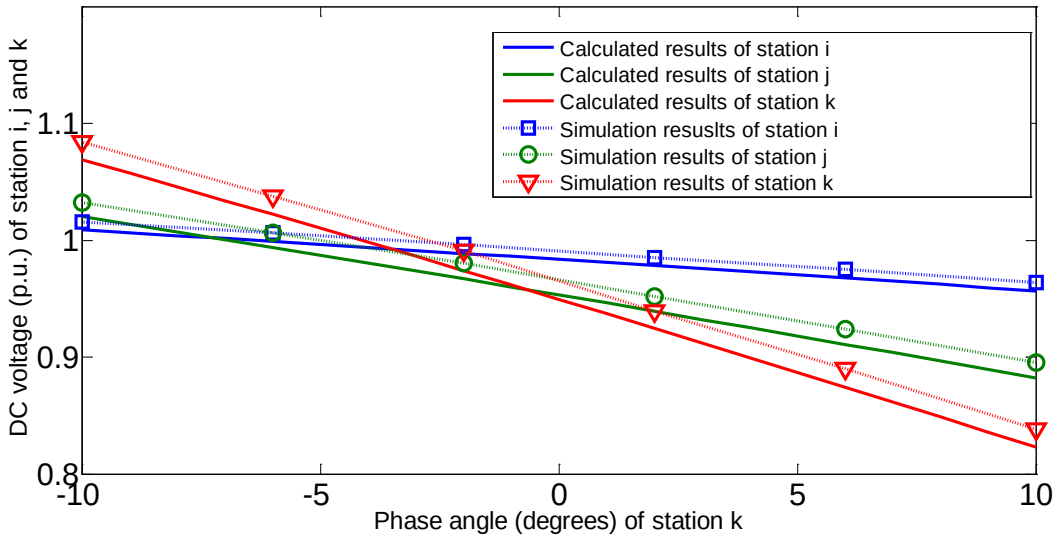


Fig. 6-17 DC voltages of MMC station i, j, k as function of δ_k (agreement to 1.5%)

The radial dc grid of Fig. 6-3 is tested by simulations and compared with the values computed from the mathematical equations of section 6.2 and 6.4 in the open control loop. The 3 MMC stations are modeled as ideal voltage sources and the test parameters are: modulation index m_i=m_j=m_k=0.9; SM capacitor size C_i=C_j=C_k=0.015F; L_0=3mH; R_0=0.2Ohm; $L_{ac\text{-}Th}$=10mH; $R_{ac\text{-}Th}$=0.6 ohm; $R_{dc\text{-}i}$=2 ohm; $R_{dc\text{-}j}$=3 ohm; $R_{dc\text{-}k}$=3 ohm. The voltage angle of δ_k is varied while the voltage angles of MMC Station i and j are kept constant at δ_i=-2.0° and δ_j=3.0°.

AC systems of i, j and k operate with voltage magnitude $V_{ac\text{-}i}$=$V_{ac\text{-}j}$=$V_{ac\text{-}k}$=25kV and voltage angle $\delta_{ac\text{-}i}$=$\delta_{ac\text{-}j}$=$\delta_{ac\text{-}k}$=0°. Other system parameters are listed in Table 6-I.

Fig. 6-17 presents the dc voltages of stations i, j and k as a function of δ_k. The 1.5% agreement between the prediction and the simulation can only be achieved by including the capacitive reactance voltages of T_{1+7}. The excellent agreement establishes the correctness of the mathematical formulas of Table 3-II and Table 3-III and the method of integrating the ac side to the dc side through equation (6-26), (6-27) and (6-28).

B. Transient Test on Multi-Terminal MMC HVDC

The multi-terminal MMC HVDC grid of Fig. 6-3 is tested with decoupled P-Q control of Fig. 6-8. In the test, power with positive sign means the MMC station is on the rectifier mode; otherwise, MMC is on the inverter mode.

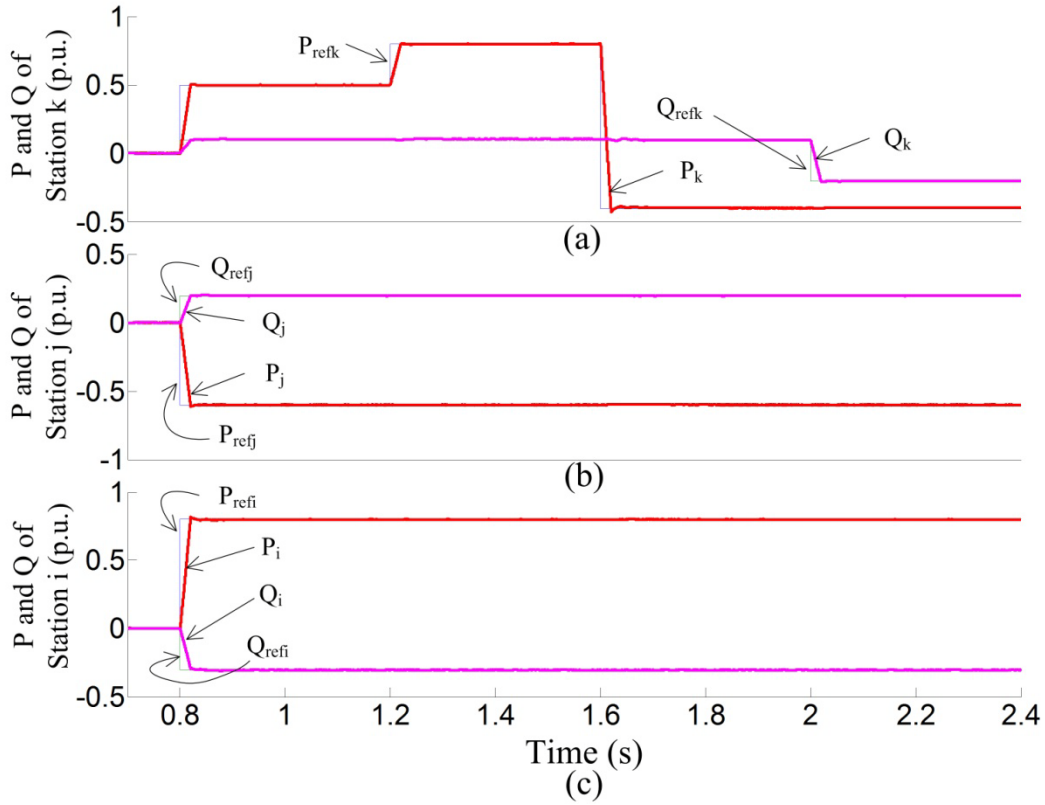


Fig. 6-18 Active power and reactive power of MMC station i, j, k, when power step changes in MMC station k. (a) P and Q of station k; (b) P and Q of station j; (c) P and Q of station i

Initially, the complex power references of stations i, j and k are zero shown in Fig. 6-18. The 4th station is an ideal voltage source (active power slack). At *t*=0.8s, MMC station k is given an active power reference P_{refk} step up change of 0.5 p.u. and a reactive power reference Q_{refk} step up change of 0.1 p.u.; MMC station j is given an active power reference P_{refj} step down change to -0.6 p.u. and a reactive power reference Q_{refj} step up change of 0.2 p.u.; MMC station i is given an active power referernce P_{refi} step up change of 0.8 p.u. and a reactive power reference Q_{refi} step down change of 0.3 p.u. The active power reference of station k steps up to 0.8 p.u. and reverses to -0.4 p.u. and the reactive power reference of station k steps down to -0.1 p.u at *t*=1.2s, *t*=1.6s and *t*=2.0s respectively.

The active power and reactive power of the three stations follow the references quickly and closely. The active and reactive power changes in station k do not affect the other two stations because they are regulated to follow their *P* reference and *Q* reference. The

changes in P_k are absorbed by the 4th station which is a dc voltage regulator and therefore an active power slack.

6.7 Conclusion

Simulations validate the predictions from harmonic function analysis that MMC can be connected in series so that MMC has potential in Ultra HVDC and MMC can be connected in parallel as multi-terminal MMC HVDC. The series connection capability follows from the equivalent circuit of the MMC as ideal voltage-sources on the ac-side and dc-side. The parallel connection capability follows from the power balance relationship $T_6 i_{ac} \Leftrightarrow 2T_2 I_d$, by which the MMC injects dc-side current $I_d=P_{ac}/U_{dc}$ much in the same way as the ideal current source equivalent in VSCs. Harmonic function analysis also predicts that MMC has a capacitive reactance voltage, whose existence is proven indirectly. This is because quantitative agreement between theory and simulations cannot be found until capacitive reactance voltage is included.

Additionally, this chapter has shown what the start-up stages of MMC consist of and how decoupled P-Q control is implemented.

Chapter 7 Performance of MMC BTB HVDC under Parallel Computing Condition

7.1 Introduction

MMC features many advantages for HVDC transmission. Recently, several MMC projects are in operation or in development over the world. For instance, there are already two 400 MW, ±200 kV commercial MMC-HVDC installations [79] in service and Siemens is doing an MMC-HVDC project INELFE between France and Spain with rated power of 2×1000 MW. It is no doubt that prior to these projects, simulations have to be conducted to provide informative references and testing guidance. However, with a large number of sub-modules (SMs) in the system, computational time for the simulation is becoming unacceptable for the analysis and optimization of complex systems under several contingencies. Furthermore, problems related to excessive simulation time will increase with the use of MMC Ultra HVDC or multi-terminal MMC HVDC grids. Several research works have been presented to accelerate the simulation of large MMC converter simulations, such as in [37], a method based on partitioning the system's admittance matrix and developing a Thevenin equivalent for the converter was proposed to reduce the computational time.

Yet, these models are implemented in traditional single-processor simulation software such as EMTP and PSCAD. Therefore, the simulation time increases with the number of MMC and number of cells per converter, which increases the time required for parameter optimization and to analyze hundreds of normal operation and fault contingencies. Such excessive simulation time may force the use of simplified MMC average models with lower number of cells than the number used in actual systems or very simplified approximate models.

The technique of using simplified models is acceptable for several cases. Nevertheless, most manufacturers, R&D organizations and future owners of MMC systems prefer to test

system performance with the most detailed models in real-time, which requires the use of MMC models designed to take advantage of parallel processing offered by modern multi-core processors.

This chapter presents one model developed by Opal-RT Technologies Inc. with the capability of real time simulation of multi-terminal MMC systems with the detailed simulation of a large number of cells. In order to test the accuracy of the real time model, a reference model with same parameters are built with detailed components in SimPowerSystem (SPS) of Simulink/MATLAB. Both of the two models are introduced in Section 7.2. The computational performance of the models as well as the verification study made by comparing the results of the fast parallel MMC model with detailed SPS model are presented in Section 7.3. Conclusion is presented in Section 7.4.

7.2 Model Description

Fig. 7- 1 shows a back-to-back (BTB) bi-pole MMC HVDC system connecting two ac networks with a rated power of 200MW. MMC Stations 1 and 2 are with the same topology as shown in Fig. 2-1 (a). This type of ac-dc-ac system could be used to transfer power between two ac networks with different operation frequencies or between a grid and wind farms. The same MMC could be used to implement multi-terminal dc grids.

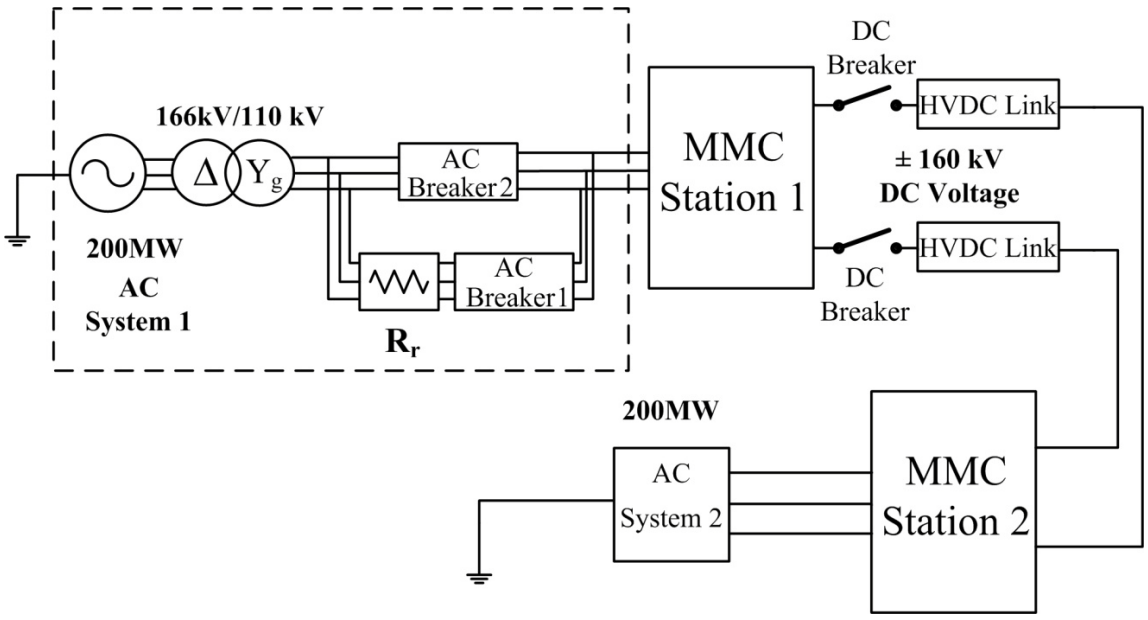


Fig. 7- 1 MMC based back-to-back HVDC system

The next sub-sections presents the fast (real time) MMC model of the above MMC systems as well as the reference model used to validate the accuracy of real time model.

A. MMC SPS Reference Model

The MMC SPS model is used as the reference model. It uses an accurate general purpose state-space solver. Each MMC sub-module and power grid is simulated in detail using pre-made models of IGBT, diodes, inductor, capacitors, transformers and sources included in the SPS model library. SPS automatically generates the state-space system of the global circuit and uses standard MATLAB variable or fixed-step solvers simulate system.

As for any simulation software, the solver and simulation time step must be adequately selected to obtain accurate results and numerical stability. For the present case, a time step of 20 microseconds with the trapezoidal solver was selected following some tests to compare the results obtained with smaller time step values.

One must note that the SPS reference model does not use any artificial delays to split the state-space system into several independent state-space systems to accelerate the simulation. The main idea is to get the best possible reference results to validate the models presented below designed to accelerate the simulation. It is believed that the same reference results would have been obtained with other traditional simulation software like EMTP and PSCAD which are also using unified accurate solvers.

B. MMC RT-LAB CPU Model for Real-Time Simulation

The MMC RT-LAB CPU model used:

1) Simulink to implement the mathematical equation of each SM one-by-one and connected in series like in actual systems;

2) SPS to simulate the remaining components and power grids.

The MMC SM subsystem is however interconnected with the power grid using either controllable voltage source or controllable current source. The state-space system is therefore separated into two independent subsystems using artificial delays, which accelerate the simulation but induces an error.

Table 7- I Parameters of the back-to-back HVDC

Parameter	Value	Parameter	Value
DC system		MMC station	
Power	200 MW	SM Capacitor Value	1456 μF
DC Voltage	±160 kV	Arm Inductor Value	360 mH
AC system		DC cable	
AC Voltage	166 kV	Inductance	100 mH
MVA	200 MW	Capacitance	0.004 μF
Resistor R_r	126 Ohm	Resistance	0.05 Ohm
Frequency f	50 Hz		
Transformer Voltage Rating	160 kV: 110 kV		

Using artificial delays enables to reduce the total processor memory requirements and also enables parallel processing, which increases simulation speed by a large factor as this will be demonstrated in section 7.3. Consequently, engineers must compromise between accuracy and speed, as is the case for several analyses.

7.3 Simulation Results

The system simulated in this chapter is shown in Fig. 7- 1 with 200MW, ±160kV bipolar HVDC link. On the ac side, 166kV/110kV, Δ/Yg connected transformer is applied in the system to limit the zero sequence. The MMC capacitor value is 1456 uF and arm inductor is 360 mH, which is satisfying its required minimum value requirement [80, 81]. All the parameters are listed in Table 7- I. As described in Chapter 6, ac breaker 1 and 2 are used to charge the MMC capacitor step by step during the start-up period with the purpose of suppressing the charging surge current.

7.3.1 Case Description

A. STATCOM Operation

The case studied consists of energizing the MMC converter and stepping up the reactive power to 0.2 p.u. The dc breakers in Fig. 7- 1 are kept in ‘open’ state, therefore the MMC station is operating as a STATCOM. Initially, all SMs switching pulses are

disabled (IGBTs are kept open) and all the capacitors in MMC stations are fully discharged (the dc voltage is zero at the simulation starting point).

The simulation case is divided into several operating scenarios or steps as follows:

Step 1) From time 0s to 0.5s, all the breakers remain open; MMC station 1 is isolated from the ac and dc network.

Step 2) At time 0.5s, ac breaker 1 closes. Ac system 1 charges MMC station 1 through a large resistor R_r (Here, R_r=126 Ohm), this can be called as diode mode.

Step 3) At time 2.5s, ac breaker 2 closes. The resistor R_r is bypassed. ac system 1 charges MMC station 1 directly.

Step 4) At time 3s, IGBT switching pulses are enabled.

Step 5) At time 5s, reactive power reference steps up by 0.2 p.u. (assuming that the positive direction of power flow is from the MMC station 1 to the grid), this can be called as STATCOM mode.

B. BTB Operation

After the MMC is well pre-energized and the dc voltage maintains at the desired value, the dc breakers in Fig. 7- 1 can be closed for BTB HVDC operation to transfer power between MMC station 1 and 2. MMC station 1 is set to be the power dispatcher and MMC station 2 is operating as voltage regulator.

The simulation case contains 2 steps as follows:

Step 1) When dc voltages of MMC station 1 and 2 maintain at the desired value, after 2.5 seconds, close dc breakers;

Step 2) At time 4s, active power reference of MMC station 1 steps up by 0.1 p.u. (positive direction of power flow is defined the same as STATCOM operation, which means in this scenario active power is transferred from MMC station 2 to MMC station 1).

7.3.2 Simulation running time

The circuits for RT-LAB CPU model (off-line) and SPS reference model are simulated on the computer with 3.4-GHz Intel i7 CPU, 8G RAM.

In order to show the simulation efficiency, the MMC HVDC system shown in Fig. 7- 1 was simulated with each model with a number of cell modules varying from 8 to 48 per arm (16 to 96 cells per phase) for the STATCOM operation of 8 seconds described above. The time step for both the SPS reference model and the RT-LAB CPU off-line model is 20 microseconds for power grid and MMC sub-modules.

From Table 7- II and Fig. 7- 2, it is noted that the SPS reference model simulation time increases exponentially with the increased number of MMC cells. This is dues to the increasing size of the state-space matrices.

On the other hand, the simulation time for the RT-LAB CPU model simulated at the same desktop computer rises slightly with the number of cells. The simulation time increases by only 30% (344s to 426s) while the number of cells per arm increased 6 times (from 8 to 48). This is due to the fact that the MMC arm model is implemented directly in C Code outside the main state-space system. Therefore, the RT-LAB CPU model significantly reduces the simulation running time when applying large number of cells per arm even if only one processor is used. Moreover, parallel processing is used to further increase the simulation speed and the model can reach real time speed simulation when implemented at a real time simulator since the SM models and the power grid models are simulated in independent state-space system. The controller is also simulated on a separate processor core.

Table 7- II Model simulation performance: Wall clock time (second) used for simulation of 8 seconds phenomena

Number of SM per arm	CPU Model		SPS Reference Model
	On a real time simulator (sec)	On a desktop Computer (off-line, sec)	On a desktop Computer (sec)
8	8	344.4	326.1
16	8	359.6	640.2
32	8	396.4	3154.9
48	8	426.5	9746.4

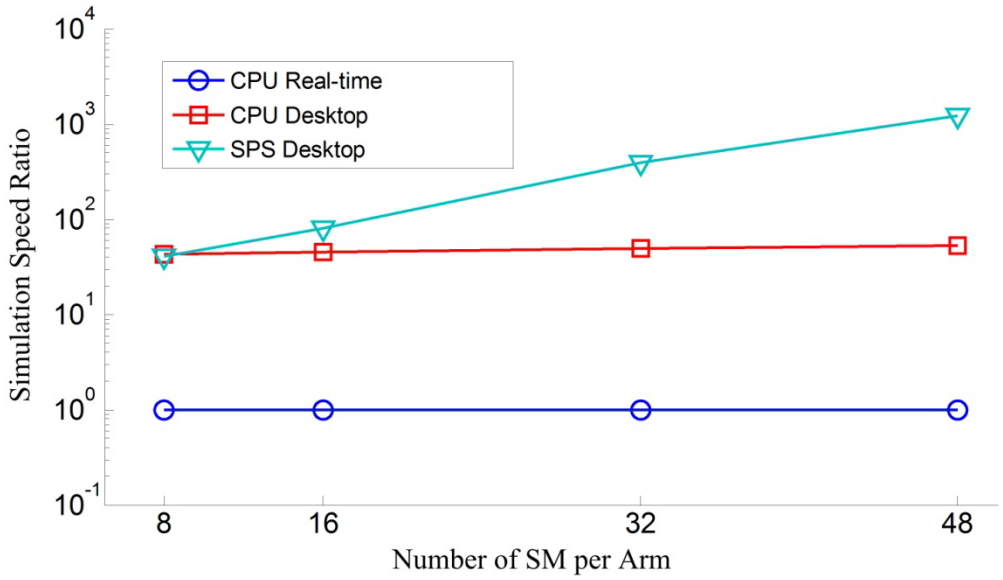


Fig. 7- 2 Simulation speed ratio (Wall clock time over simulation time) for models with different number of SM

Consequently, the RT-LAB CPU model implemented on a standard 12-core computer can simulate the system in real-time speed, which is very useful to optimize control system, implemented in Simulink.

7.3.3 Validation of Accuracy

In order to evaluate the simulation accuracy of the real-time CPU model, two sets of comparisons are conducted and all the models are with 8 sub-modules per arm. For the first comparison, the off-line simulation (on a desktop computer) results from the real-time CPU model are compared with those obtained from SPS reference model during the STATCOM operation. The simulation time step is 20 microseconds for both models. The second comparison work is between the results from CPU model and those from SPS model during BTB operation with the same simulation time step as first comparison for both models.

Simulation results from CPU model and SPS model are presented in Fig. 7- 3, Fig. 7- 4, Fig. 7- 5, Fig. 7- 6 and Fig. 7- 7 in the aspects of dc voltage, MMC sub-module capacitor voltage, MMC output ac voltage, ac current and system active and reactive power of MMC station 1, which are denoted by V_{dc}, V_{cap}, V_{abc}, I_{abc}, P and Q respectively.

All legends with suffix "_ reference" are indicating results from SPS reference model and the legend with suffix "_CPU" indicate results from RT-LAB CPU model.

A. Comparison between CPU Model and SPS Model during STATCOM Operation

Fig. 7- 3, Fig. 7- 4 and Fig. 7- 5 present the simulation results from MMC STATCOM operation. Fig. 7- 3 shows the overall simulation results of MMC capacitor voltage of phase a in the upper arm, SM1. Fig. 7- 4 and Fig. 7- 5 present the zoomed-in results of steady-state in simulation scenario 2 and 5 of STATCOM operation described in section 7.3.1, which indicates that each pair of corresponding results could be superimposed. The main difference lies in the dc voltage when no pulses are enabled.

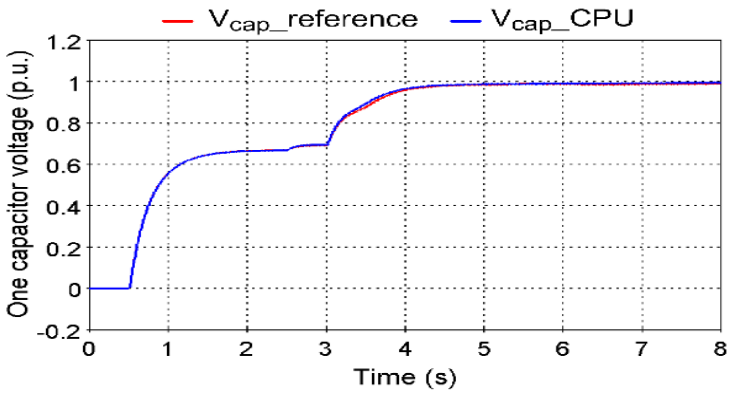


Fig. 7- 3 Overall simulation resulsts of MMC station 1 (Reference model vs. CPU model), capacitor voltage of phase a, upper arm, SM1

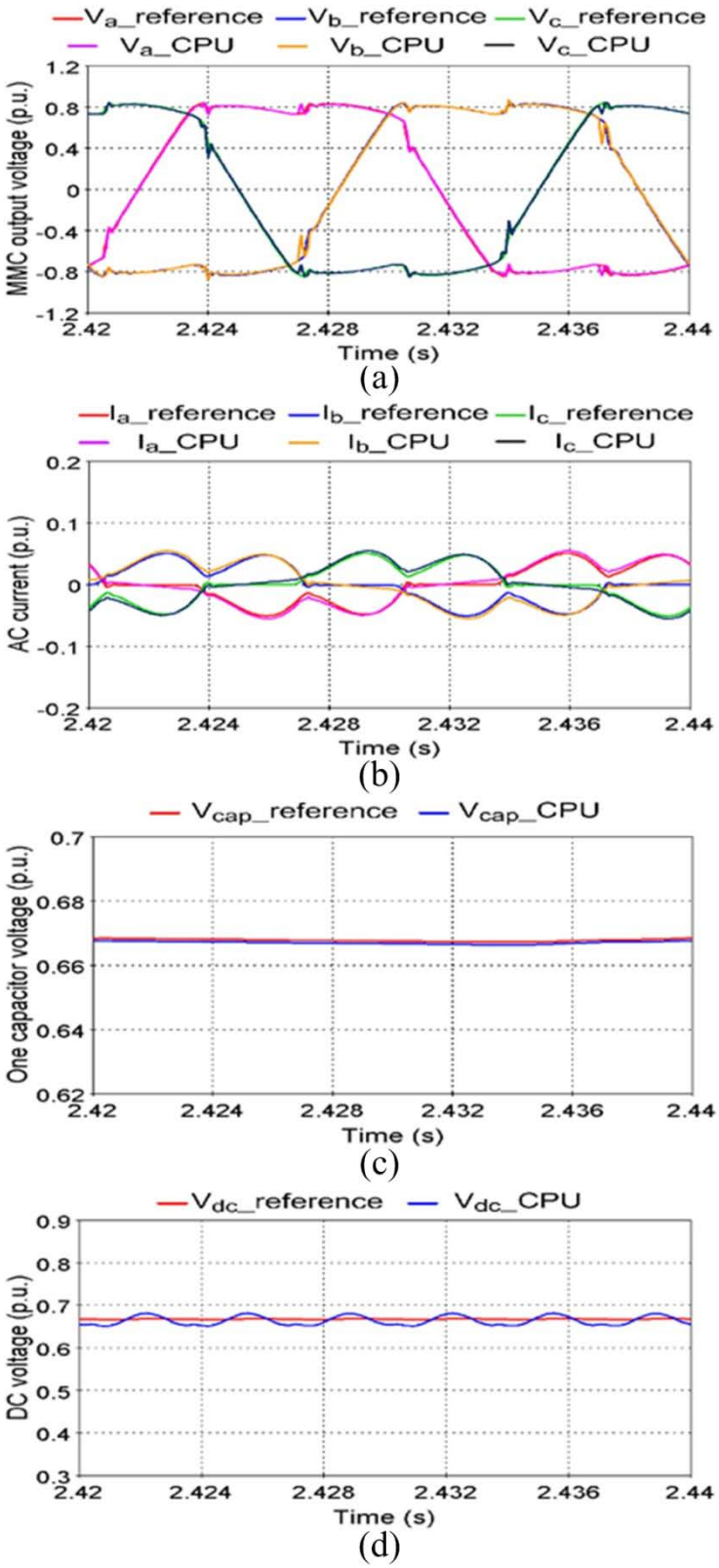
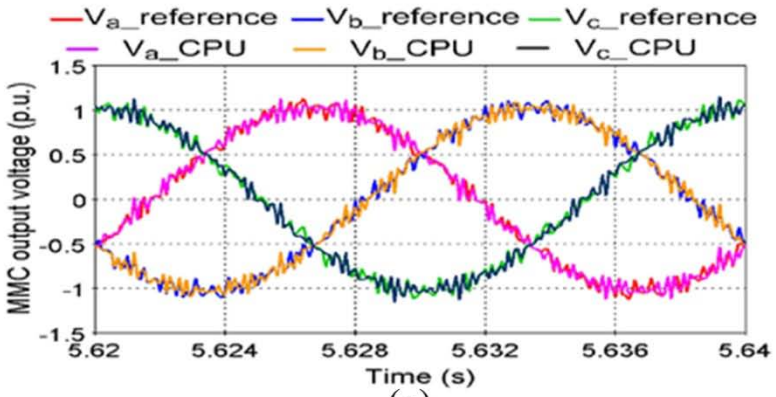
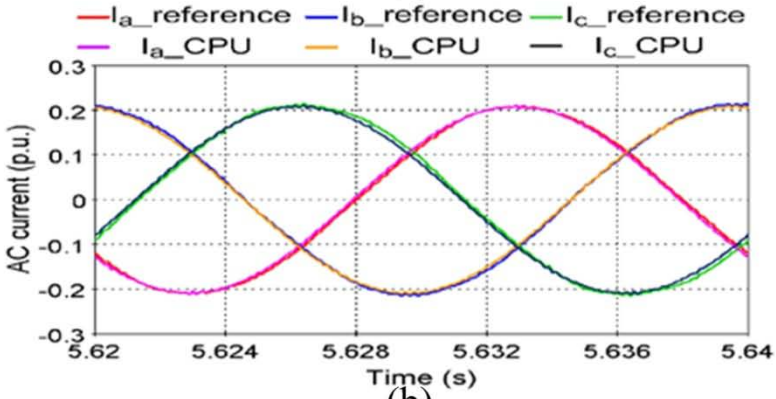


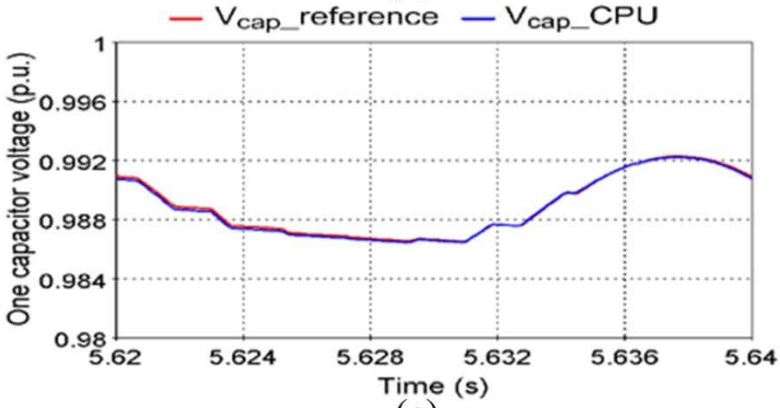
Fig. 7- 4 MMC charging (diode mode) through a charge resistor. (a) Three-phase MMC output voltage; (b) Three-phase ac current; (c) Capacitor voltage of phase a, upper arm, SM1; (d) dc pole-to-pole voltage


Va_reference
Vb_reference
Vc_reference
Va_CPU
Vb_CPU
Vc_CPU
MMC output voltage (p.u.)
1.5
1
0.5
0
-0.5
-1
-1.5
5.62
5.624
5.628
5.632
5.636
5.64
Time (s)

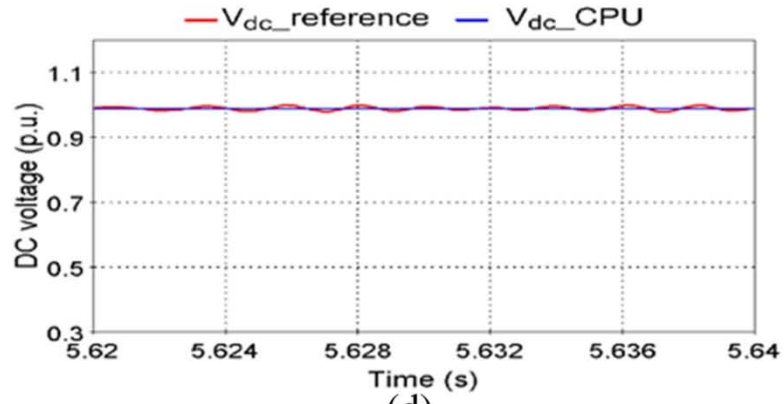
(a)


Ia_reference
Ib_reference
Ic_reference
Ia_CPU
Ib_CPU
Ic_CPU
AC current (p.u.)
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
5.62
5.624
5.628
5.632
5.636
5.64
Time (s)

(b)


Vcap_reference
Vcap_CPU
One capacitor voltage (p.u.)
1
0.996
0.992
0.988
0.984
0.98
5.62
5.624
5.628
5.632
5.636
5.64
Time (s)

(c)


Vdc_reference
Vdc_CPU
DC voltage (p.u.)
1.1
0.9
0.7
0.5
0.3
5.62
5.624
5.628
5.632
5.636
5.64
Time (s)

(d)

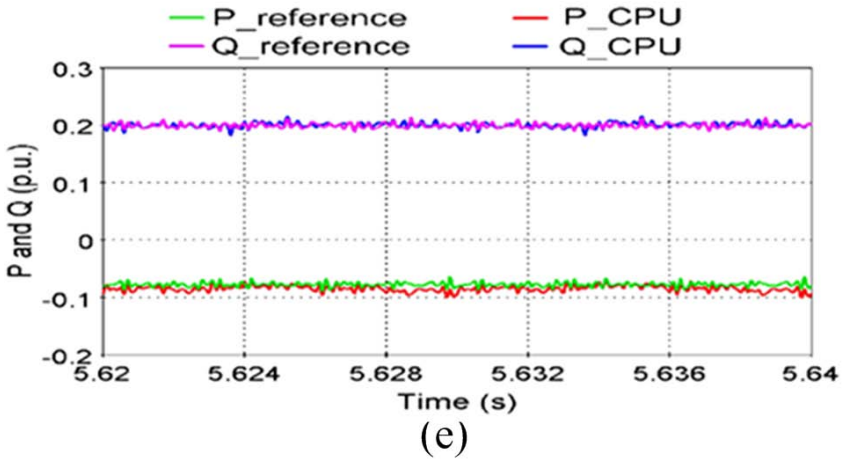


Fig. 7- 5 MMC operating at STATCOM mode with P_{ref}=0, Qr_{ef}=0.2 p.u.. (a) Three-phase MMC output voltage; (b) Three-phase ac current; (c) Capacitor voltage of phase a, upper arm, SM1; (d) dc pole-to-pole voltage; (e) P and Q

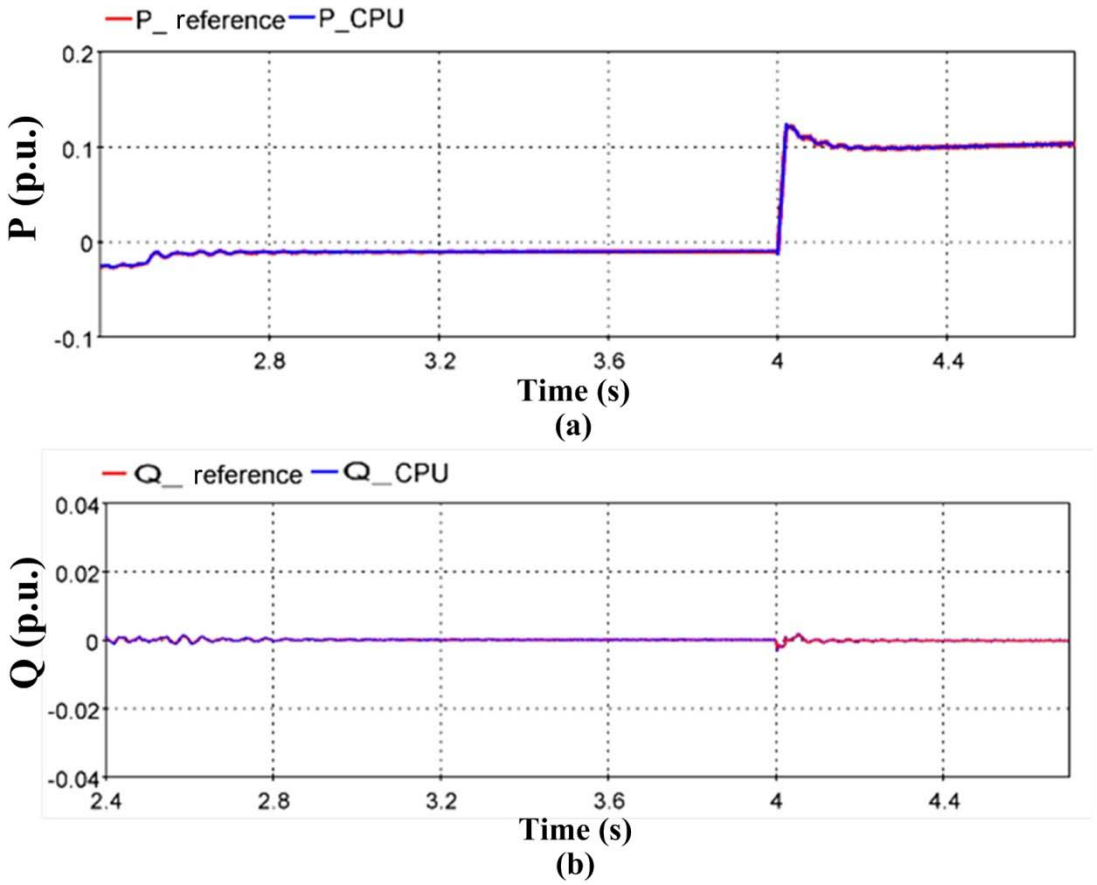


Fig. 7- 6 MMC working in the back-to-back operation case with Q_{ref}=0, P_{ref} steps up at 4s by 0.1 p.u. (a) active power P of MMC station 1; (b) reactive power Q of MMC station 1

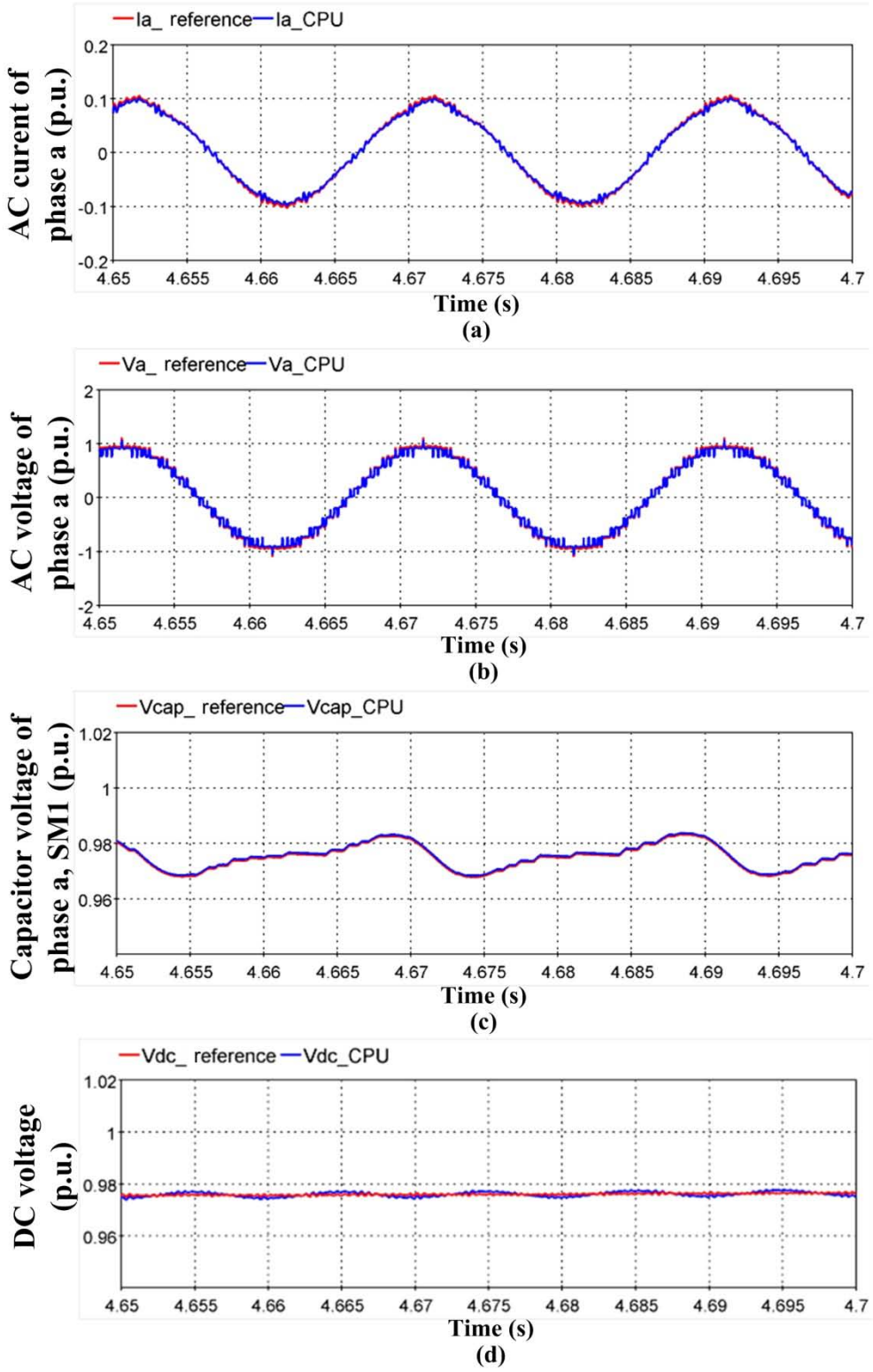


Fig. 7- 7 MMC station 1 absorbing power from MMC station 2. (a) ac current of MMC station 1, phase a; (b) output voltage of MMC station 1, phase a; (c) capacitor voltage of MMC station 1, phase a, upper arm, SM1; (d) dc voltage of MMC station 1

B. Comparison between CPU Model and SPS Model during BTB Operation

Simulation results from CPU model and SPS model during the BTB operation are presented in Fig. 7- 6 and Fig. 7- 7. Simulation case description is shown in section 7.3.1. Fig. 7- 6 displays the active power and reactive power of MMC station 1 after dc breakers are closed. At t=4s, MMC station 1 absorbs 0.1 p.u. active power from MMC station 2. Fig. 7- 7 presents the zoomed-in results of steady-state in simulation scenario 2 of BTB operation. Each pair of corresponding simulation results overlap with each other, which verifies the correctness of the CPU model.

7.4 Conclusion

In this chapter, one MMC model from OPAL-RT Technologies has been introduced. CPU model developed by Opal-RT Technologies is capable of running simulation in real time. The CPU model can run with a time step of 20 to 25 microseconds with about 100 SMs per phase, which could drastically save the simulation time and enable users to perform more tests in less time.

The simulation result accuracy of CPU model has been validate during the MMC STATCOM operation and BTB operation by comparing their results with a SPS reference model using a general purpose accurate state-space solver.

Chapter 8 Conclusions

8.1 Conclusions

Capacitor Modulation Concept

The research has yielded a concept of the operation on MMC based on varying the number capacitors connected in series to form the upper arm and the lower arm of one of the three phases of an MMC station. From this capacitor modulation concept, harmonic function analysis is applied to derive equivalent circuits of the MMC and mathematical formulas. The equivalent circuits and the formulas offer analytical insights to predict potential applications of MMC, to explain its shortcomings and to propose methods to the overcome the shortcomings.

The body of the thesis has consisted of using the equivalent circuits and the mathematical formulas to predict potential applications (MMC Ultra HVDC, MMC multi-terminal HVDC), to reveal discoveries (capacitive reactance voltages for power factor correction) and to eliminate 2^{nd} harmonic circulating current (by feed-forward and feedback methods). The validation of all the claims by digital simulations leaves little doubt to the correctness of the concept.

Joint Feed-Forward and Feedback Elimination of Circulating Current

An MMC station consists of 3 isolated single-phase ac-to-dc converters. Each phase retains the double frequency component of single-phase ac power. This has resulted in large circulating currents which, because they are of low frequencies, have to be filtered by large expensive capacitors. The derived mathematical formulas pin-point the 2^{nd} harmonic voltages at the source and a feed-forward method is implemented to cancel it. For added reliability, both feed-forward and feedback methods have been developed, which operate singly or jointly, to eliminate the 2^{nd} harmonic circulating current. The feed-forward and feedback methods should enable the capacitor size to be reduced thus reducing the cost and the size of the MMC station.

Robust Protection of Feed-Forward and Feedback Methods by Deadbeat

For added robustness, the research shows that reference current control (in contrast to reference voltage control) by the deadbeat technique can be implemented in the MMC to prevent large fault currents from overcharging the sub-module capacitor beyond the safe voltage rating of IGBTs of each sub-module.

Capacitive Reactance Voltage on AC-Side

The mathematical formulas reveal that the ac-side has capacitive reactance voltages which must be taken into account for accurate quantitative predictions. The capacitive reactance voltages can contribute to power factor improvement. On the other hand they can lead to inadvertent resonance.

MMC Ultra HVDC

As the equivalent circuits of MMC on both the ac side and dc side are ideal voltage sources, there is the potential of connecting MMC stations in series on their dc sides to form Ultra HVDC. This possibility is confirmed by simulation.

MMC Multi-terminal HVDC

At the same time, the formulas from harmonic function analysis also show that the dc sides of MMC stations are also suitable for parallel connection for multi-terminal HVDC applications. Performance of MMC Ultra HVDC and MMC multi-terminal HVDC has been evaluated under normal operating conditions.

Below are summaries of each chapter.

Chapter 2: Modular Multilevel Converter

The 3-phase half-bridge sub-module MMC configuration as well as its operating principle is briefly introduced. PSC-PWM modulation technique and capacitor balancing algorithm applied for MMC are discussed concisely. Through KVL, equivalent circuits of MMC on both the ac side and the dc side are derived.

Chapter 3: MMC Harmonic Function Analysis

This chapter introduces harmonic function analysis in the perspective of capacitor modulation. Mathematical formulas derived from harmonic function analysis unveil the mysteries of MMC for easy understanding. By regrouping mathematical formulas of both

ac and dc side in terms of the frequency order, it shows that the fundamental frequency component and odd order harmonics all gather on the ac side while leaving dc component and even order harmonics on the dc side. Moreover, both the ac side and the dc side comprise of ideal voltage sources. Finally, nonlinear ordinary differential equation model of MMC is obtained and verified.

Chapter 4: Low-Order Harmonic Reduction of MMC

Following the harmonic function analysis developed in Chapter 3, the origin of 2^{nd} harmonic circulating current is pin-pointed. The model of 2^{nd} harmonic circulating current is derived as well. The prediction of the size of circulating current presently guides the selection of MMC arm inductance and sub-module capacitance. By extending the harmonic function analysis, this chapter proposes a novel feed-forward method to reduce 2^{nd} harmonic circulating current at the source. With the elimination of 2^{nd} harmonic circulating current, other low-order harmonics proliferated from it are also eliminated, so that sub-module capacitor size can be reduced. Extensive simulation tests have been conducted to verify the effectiveness of the proposed feed-forward method.

Chapter 5: Incorporating Deadbeat and Low-Order Harmonic Reduction in MMC

This chapter shows that MMC can have two control channels: one is s fundamental frequency channel to implement deadbeat control and anther double frequency channel to implement low-order harmonic reduction control. The two independent channels are discovered based on harmonic function analysis in Chapter 3 and 4. Low-order harmonic reduction control enables the use of size reduced sub-module capacitors; however, during fault conditions the large fault currents may cause capacitor voltage to be overcharged to damage IGBTs. As a current reference control, deadbeat prevents MMC from destructive fault currents under ac fault conditions. Deadbeat can therefore rescue low-order harmonic reduction methods from large ac fault currents. By tracking the reference, deadbeat is also capable of reducing 3^{rd} and odd harmonics generated by MMC on the ac side. In addition, this chapter shows that 2^{nd} harmonic and other low-order harmonic proliferated from it can be reduced by feed-forward method and feedback method, singly or jointly. When combining feed-forward and feedback low-order harmonic reduction methods together, it offers enhanced reliability.

Simulation results show that deadbeat, feed-forward and feedback harmonic reduction methods can be jointly implemented by the MMC.

Chapter 6: MMC Ultra HVDC and Multi-Terminal HVDC

Based on harmonic function analysis, this chapter shows that quantitative modeling of ac and dc systems interconnected by MMC is accurate enough only when the capacitive reactance is taken into account. Since the dc side of MMC can be modeled as ideal voltages, this chapter verifies that MMC is suitable for series connection to form Ultra HVDC by simulation. Moreover, this chapter shows that MMC is also suitable for parallel connection for multi-terminal HVDC applications with ac-to-dc power balance equations derived from harmonic function analysis as the theoretical basis.

Additionally, MMC start-up stage control aiming at charging MMC stations to a desired dc voltage value before putting into operation and MMC decoupled P-Q control implemented through modulation signals under normal conditions are introduced in this chapter.

Chapter 7: Performance of MMC BTB HVDC under Parallel Computing Condition

This chapter briefly evaluates the performance of MMC back-to-back HVDC under parallel computing condition. It shows that the parallel computing model of MMC developed by Opal-RT Technologies can save simulation time significantly. Moreover, the simulation results from parallel computing model are accurate enough compared with the ones from reference model built in Simulink/MATLAB.

8.2 Suggestions for Future Work

Based on harmonic function analysis, the thesis shows that MMC Ultra HVDC and MMC multi-terminal HVDC perform well under normal operating conditions. Research topic on both MMC Ultra HVDC and MMC multi-terminal HVDC applications under fault conditions is yet to be studied. Besides, research on applying MMC stations to renewable energy networks such as wind farms and photovoltaics (PV) stations needs to be explored.

Appendix-A: Digital Closed Loop Deadbeat Controller

The block diagram of a digital closed loop deadbeat control system is shown in Fig. A-1. $i_{acref}(t)$ and $i_{ac}(t)$ represent reference current and feedback current in the continuous time domain respectively. The control forward path consists of control block G_C(z), computation delay block, zero-order-hold (ZOH) block and the plant block G_P(z). The block in the feedback path is G_F(z). The design of the digital closed loop deadbeat controller is to obtain the unknown blocks G_C(z) and G_F(z), so that the overall discrete transfer function G(z) is z^{-2}.

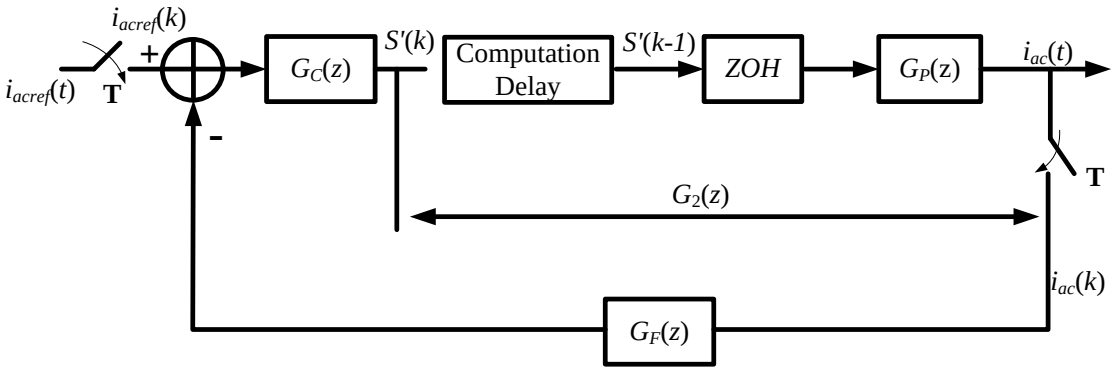


Fig. A-1 Block diagram of a digital closed loop deadbeat control system

In continuous frequency domain, the ZOH block and the plant (*L*-*R*) in Fig. A-1 are:

$$G_{ZOH}(s) = \frac{1 - e^{-s\Delta T}}{s} \tag{A-1}$$

$$G_P(s) = \frac{b}{s + a} \tag{A-2}$$

Here, a=R/L, b=1/L. Taking the Z transform of $G_{ZOH}(s)G_P(s)$,

$$G_{ZOH}(z)G_P(z) = \left(1 - z^{-1}\right) Z\left\{ L^{-1}\left[\frac{G_P(s)}{s} \right] \right\} = \frac{b}{a} \frac{1 - e^{-a\Delta T}}{1 - e^{-a\Delta T} z^{-1}} z^{-1} \tag{A-3}$$

As shown in Fig. A-1, G_2(z) is defined as the combination blocks of computation delay, zero-order-hold and the plant.

$$G_2(z) = z^{-1}G_{ZOH}(z)G_P(z) = \frac{b}{a}\frac{1-e^{-a\Delta T}}{1-e^{-a\Delta T}z^{-1}}z^{-2} \tag{A-4}$$

Since the overall transfer function is designed to be z^{-2},

$$G(z) = \frac{G_C(z)G_2(z)}{1+G_F(z)G_C(z)G_2(z)} = z^{-2} \tag{A-5}$$

which has a sampling delay of two sampling periods.

Assuming $G_C(z)$ and $G_F(z)$ are with the formation:

$$G_C(z) = \frac{N_C(z)}{D_C(z)} \tag{A-6}$$

$$G_F(z) = \frac{N_F(z)}{D_F(z)} \tag{A-7}$$

where $N(z)$ and $D(z)$ are the numerator and the denominator (in the polynomial form of z^0, z^{-1}, z^{-2}, … z^{-n}) of the transfer function respectively. Subscript C and F represent control block and feedback block respectively. Substituting (A-6) and (A-7) into (A-5),

$$\begin{aligned} G(z) = \frac{G_C(z)G_2(z)}{1+G_F(z)G_C(z)G_2(z)} &= \frac{\dfrac{N_C(z)}{D_C(z)}\dfrac{\left(\dfrac{b}{a}1-e^{-a\Delta T}\right)z^{-2}}{1-e^{-a\Delta T}z^{-1}}}{1+\dfrac{N_C(z)}{D_C(z)}\dfrac{N_F(z)}{D_F(z)}\dfrac{\left(\dfrac{b}{a}1-e^{-a\Delta T}\right)z^{-2}}{1-e^{-a\Delta T}z^{-1}}} \\ &= \frac{N_C(z)D_F(z)\left(\dfrac{b}{a}1-e^{-a\Delta T}\right)}{D_F(z)D_C(z)\left(1-e^{-a\Delta T}z^{-1}\right)z^2 + N_F(z)N_C(z)\left(\dfrac{b}{a}1-e^{-a\Delta T}\right)} = \frac{1}{z^2} \end{aligned} \tag{A-8}$$

Thus,

$$N_C(z)D_F(z)\left(\frac{b}{a}1-e^{-a\Delta T}\right)=1 \tag{A-9}$$

$$D_F(z)D_C(z)\left(1-e^{-a\Delta T}z^{-1}\right)z^2 + N_F(z)N_C(z)\left(\frac{b}{a}1-e^{-a\Delta T}\right) = z^2 \tag{A-10}$$

Setting $D_F(z)=1$ [72], then

$$N_C(z) = \frac{1}{\left(\dfrac{b}{a}1-e^{-a\Delta T}\right)} = \frac{a}{b}\frac{1}{1-e^{-a\Delta T}} \tag{A-11}$$

Substituting (A-11) into (A-10),

$$D_C(z)\left(1-e^{-a\Delta T}z^{-1}\right)z^2 + N_F(z) = z^2 \tag{A-12}$$

When D_C(z) is chosen to be

$$D_C(z) = 1 + e^{-a\Delta T}z^{-1} \tag{A-13}$$

Then,

$$N_F(z) = e^{-2a\Delta T} \tag{A-14}$$

Therefore, the unknown blocks G_C(z) and G_F(z) are obtained as,

$$G_C(z) = \frac{\frac{a}{b}\frac{1}{1-e^{-a\Delta T}}}{1+e^{-a\Delta T}z^{-1}} \tag{A-15}$$

$$G_F(z) = e^{-2a\Delta T} \tag{A-16}$$

Appendix-B: D-Q Transformation

Fig. B-1 shows a 3-phase ac circuit. Voltages at the sending and receiving ends are represented by u_{ma}, u_{mb}, u_{mc} and u_a, u_b, u_c, respectively. The ac currents are denoted by i_{aca}, i_{acb}, i_{acc} which flow through an inductor (L) and a resistor (R).

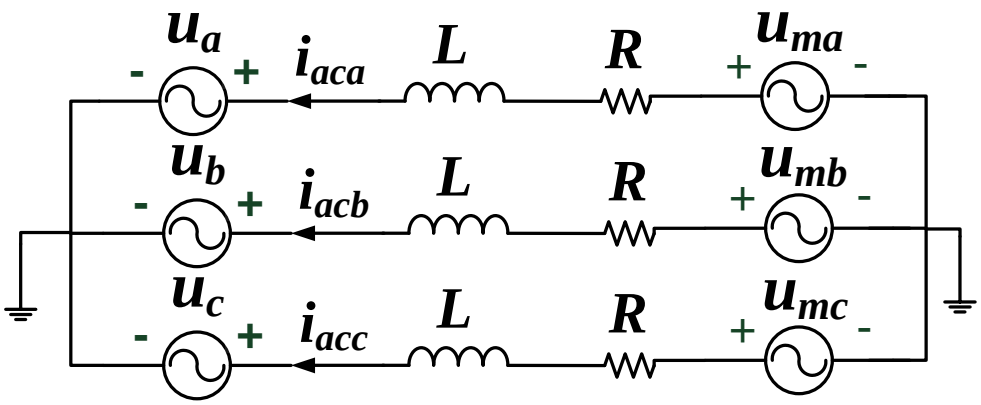


Fig. B-1 3-phase ac circuit schematic

According to Kirchhoff's voltage law,

$$\begin{bmatrix} u_{ma} \\ u_{mb} \\ u_{mc} \end{bmatrix} = R\begin{bmatrix} i_{aca} \\ i_{acb} \\ i_{acc} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{aca} \\ i_{acb} \\ i_{acc} \end{bmatrix} + \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{B-1}$$

With a-b-c to d-q transformation matrix (also known as Park's transformation matrix), variables of the stationary a-b-c frame can be converted into their equivalent variables of the rotating d-q frame:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = [P]\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{B-2}$$

where [P] is Park's transformation matrix and expressed as

$$[P]=\frac{2}{3}\begin{bmatrix}\cos(\omega t) & \cos(\omega t-120°) & \cos(\omega t+120°)\\ -\sin(\omega t) & -\sin(\omega t-120°) & -\sin(\omega t+120°)\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix} \tag{B-3}$$

The inverse of Park's transformation matrix which can be applied to transform variables of the rotating d-q frame back into the equivalent variables of the stationary a-b-c frame is

$$[P]^{-1}=\begin{bmatrix}\cos(\omega t) & -\sin(\omega t) & 1\\ \cos(\omega t-120°) & -\sin(\omega t-120°) & 1\\ \cos(\omega t+120°) & -\sin(\omega t+120°) & 1\end{bmatrix} \tag{B-4}$$

Since

$$[P][P]^{-1}=[P]^{-1}[P]=[I] \tag{B-5}$$

where [*I*] is the identity matrix, (B-1) can be rewritten as

$$\begin{aligned}&[P]^{-1}[P]\begin{bmatrix}u_{ma}\\ u_{mb}\\ u_{mc}\end{bmatrix}=R[P]^{-1}[P]\begin{bmatrix}i_{aca}\\ i_{acb}\\ i_{acc}\end{bmatrix}+L\frac{d}{dt}\left\{[P]^{-1}[P]\begin{bmatrix}i_{aca}\\ i_{acb}\\ i_{acc}\end{bmatrix}\right\}+[P]^{-1}[P]\begin{bmatrix}u_a\\ u_b\\ u_c\end{bmatrix}\\ &=[P]^{-1}\begin{bmatrix}u_{md}\\ u_{mq}\\ u_{m0}\end{bmatrix}=R[P]^{-1}\begin{bmatrix}i_{acd}\\ i_{acq}\\ i_{ac0}\end{bmatrix}+L\frac{d}{dt}\left\{[P]^{-1}\begin{bmatrix}i_{acd}\\ i_{acq}\\ i_{ac0}\end{bmatrix}\right\}+[P]^{-1}\begin{bmatrix}u_d\\ u_q\\ u_0\end{bmatrix}\\ &=R[P]^{-1}\begin{bmatrix}i_{acd}\\ i_{acq}\\ i_{ac0}\end{bmatrix}+L[P]^{-1}\frac{d}{dt}\begin{bmatrix}i_{acd}\\ i_{acq}\\ i_{ac0}\end{bmatrix}+L\left\{\frac{d[P]^{-1}}{dt}\right\}\begin{bmatrix}i_{acd}\\ i_{acq}\\ i_{ac0}\end{bmatrix}+[P]^{-1}\begin{bmatrix}u_d\\ u_q\\ u_0\end{bmatrix}\end{aligned} \tag{B-6}$$

where $d[P]^{-1}/dt$ is

$$\frac{d[P]^{-1}}{dt}=\begin{bmatrix}-\omega\sin(\omega t) & -\omega\cos(\omega t) & 0\\ -\omega\sin(\omega t-120°) & -\omega\cos(\omega t-120°) & 0\\ -\omega\sin(\omega t+120°) & -\omega\cos(\omega t+120°) & 0\end{bmatrix} \tag{B-7}$$

Multiplying [*P*] in (B-6),

$$[P][P]^{-1}\begin{bmatrix} u_{md} \\ u_{mq} \\ u_{m0} \end{bmatrix} = R[P][P]^{-1}\begin{bmatrix} i_{acd} \\ i_{acq} \\ i_{ac0} \end{bmatrix} + L[P][P]^{-1}\frac{d}{dt}\begin{bmatrix} i_{acd} \\ i_{acq} \\ i_{ac0} \end{bmatrix} + L[P]\left\{\frac{d[P]^{-1}}{dt}\right\}\begin{bmatrix} i_{acd} \\ i_{acq} \\ i_{ac0} \end{bmatrix} + [P][P]^{-1}\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} \tag{B-8}$$

Since

$$[P]\left\{\frac{d[P]^{-1}}{dt}\right\} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120°) & \cos(\omega t + 120°) \\ -\sin(\omega t) & -\sin(\omega t - 120°) & -\sin(\omega t + 120°) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} -\omega\sin(\omega t) & -\omega\cos(\omega t) & 0 \\ -\omega\sin(\omega t - 120°) & -\omega\cos(\omega t - 120°) & 0 \\ -\omega\sin(\omega t + 120°) & -\omega\cos(\omega t + 120°) & 0 \end{bmatrix} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{B-9}$$

(B-8) can be rewritten as

$$\begin{bmatrix} u_{md} \\ u_{mq} \\ u_{m0} \end{bmatrix} = R\begin{bmatrix} i_{acd} \\ i_{acq} \\ i_{ac0} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{acd} \\ i_{acq} \\ i_{ac0} \end{bmatrix} + \begin{bmatrix} 0 & -\omega L & 0 \\ \omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{acd} \\ i_{acq} \\ i_{ac0} \end{bmatrix} + \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} \tag{B-10}$$

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