Development of SOA-based Space Switches and Photonic Integrated Circuit Interface for Optical Interconnection Networks

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Abstract

With the explosive increase of internet service and diverse applications ranging from video streaming, social networking and cloud computing, the requirements of modern computing platforms keep increasing to satisfy the demand for fast computation, data analysis and processing. This situation poses challenging requirements to the data center/HPC network in terms of throughput, scalability, and power consumption. Optical interconnection network has been proposed as a promising means to meet the increase of communication bandwidth and data throughput with low power consumption.

Energy-proportional optical interconnections are enabled by semiconductor optical amplifiers (SOAs) remaining off (or idle) when not routing data. In this work, the physical layer scalability of SOA-based optical space switches configured with different gain and loss is assessed using an experimental recirculating loop. Results demonstrate that for a 13.0-dB gain/loss configuration, optical multi-channel packets successfully propagate through a series of 14 SOAs with a BER $< 10^{-9}$, which indicates that a single-stage space switch can scale up to 10^9 ports. Scalability improves for lower gain/loss configuration at the cost of more SOAs per routing path. As expected, scalability is limited by cross-gain modulation (XGM) and optical signal-to-noise ratio (OSNR) degradation, but their detrimental impact depends on the architecture configuration. Furthermore, an SOA model used as a tool to predict the performance degradation of SOA-based space switches is developed and validated.

Given the potential on-chip large-scale integration of SOA-based space switches or other optical interconnection networks, high density optical connections are required. In that context, an ultra dense silicon photonics interface for the coupling between optical fiber and photonic integrated circuits (PICs) is designed and fabricated. The designed optical interface consists of compact grating coupler array and nanophotonic waveguides. The simulation results and experimental characterization of chip performance are presented, indicating a potential high capacity optical connection for off-chip and on-chip communications.

Abrégé

Avec l'augmentation explosive des services Internet et des applications diverses allant des vidéos en continu, aux réseaux sociaux en passant par l'informatique en nuage, les exigences pour les plates-formes informatiques modernes ne cessent d'augmenter pour satisfaire la demande pour le calcul rapide et l'analyse et le traitement de données. Cette situation crée des exigences complexes sur les centres de données et réseaux HPC en terme de débit, d'extensibilité et de consommation d'énergie. Un réseau d'interconnexion optique à faible consommation d'énergie est proposé comme moyen prometteur pour répondre à l'augmentation de la bande passante et du débit de données pour les communications.

Les interconnexions optiques à énergie proportionnelle sont activées par des amplificateurs optiques à semiconducteur (SOA) et sont fermés (ou au repos) lorsqu'elles ne transfèrent pas de données. Dans cette thèse, l'extensibilité de la couche physique des commutateurs optiques spatiaux basés sur des SOA et configurés pour différents gains et pertes est évaluée à l'aide d'une boucle de recirculation expérimentale. Les résultats montrent que pour une configuration de gain/perte de 13.0 dB, des paquets de données optiques et multi-canaux se propagent avec succè s à travers une série de 14 SOA avec un taux d'erreur binaire (BER) de moins de 10^{-9}, ce qui indique qu'un commutateur spatial en une seule étape peut s'échelonner jusqu'à 10^9 ports. L'extensibilité s'améliore pour des configurations à moindre gain/perte, au coût de plus de SOA par chemin de routage. Tel que prévu, l'extensibilité est limitée par la modulation par saturation de gain (XGM) et la dégradation du rapport signal sur bruit optique (OSNR), mais leur impact négatif dépend de l'architecture. En outre, un modèle SOA est élaboré et validé comme outil pour prédire la dégradation de la performances des commutateurs spatiaux SOA.

Compte tenu de l'intégration à grande échelle de commutateurs spatiaux SOA ou autres réseaux d'interconnexion optiques sur puce, des connexions optiques à haute densité sont nécessaires. Dans ce contexte, une interface photonique ultra dense sur silicium pour le couplage entre une fibre optique et des circuits photoniques intégrés (PIC) a été conçue et fabriquée. L'interface optique conue est composée de coupleurs à réseaux compacts et de guides d'onde nanophotoniques. Les résultats de simulation et la caractérisation expérimentale des performances de la puce sont présentés, indiquant une potentielle connexion optique à haute capacité pour les communications sur puce et hors puce.

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List of Acronyms

HPC	High performance computing
CMOS	Complementary metal oxide semiconductor
SOI	Silicon on insulator
PWM	Passive wavelength-striped mapping
SOA	Semiconductor optical amplifier
WDM	Wavelength division multiplexing
XGM	Cross-gain modulation
ASE	Amplified spontaneous emission
BER	Bit error rate
PROFA	Pitch reducing optical fiber array
PIC	Photonic integrated circuit
FPGA	Field programmable gate array
PDG	Polarization dependent gain
OSNR	Optical signal-to-noise ratio
TDM	Time division multiplexing
ROADM	Reconfigurable optical add/drop multiplexers
AWG	Arrayed-waveguide grating
WSS	Wavelength selective switch
MEMS	Micro-electro-mechanical systems
OXC	Optical cross-connects
OPS	Optical packet switching
MZI	Mach-Zehnder interferometer
SMF	Single-mode fiber
DFB	Distributed-feedback laser

NRZ	Non-return-to zero
PRBS	Pseudo-random bit sequence
PPG	Pulse pattern generator
OSA	Optical spectrum analyzer
BPF	Band-pass filter
PD	Photodetector
ED	Error detector
NF	Noise figure
CW	Continuous wave
FDTD	Finite difference time domain
FSR	Free spectral range
EDFA	Erbium doped fiber amplifier

Chapter 1

Introduction

The steady growth of the Internet combined with increasingly complex networking and telecommunication applications poses more and more challenging requirements of high bandwidth, throughput, and low latency for modern high performance computing (HPC) platforms, (*e.g.,* supercomputers, data center and telecommunication core routers) [1]. However, with the immense growth in network traffic and required computation capacities, conventional electronic interconnection networks have nearly reached its capacity limit and been trapped in bottleneck [2]. Furthermore, while the bandwidth and throughput are required to be improved to satisfy the demand for fast computation and data processing, the power consumption also becomes an issue due to thermal constraint with electronics. As such, optical technology has been proposed as a promising solution to meet the increase of communication bandwidth and data throughput while maintaining low power consumption in interconnection networks [3].

1.1 Optical interconnection networks

Optical networks have been widely used in the long-haul telecommunication networks over the past decades, providing high bandwidth, low latency and low power consumption. It is well established that optical data transmission and the utilization of fiber-optic photonic media can be a novel alternative technology in interconnection networks [4]. Until now, the optical technology has been utilized only for point-to-point links (fiber optics) to connect electrical switches. However, the power hungry electrical-to-optical (E/O) and optical-to-electrical (O/E) transceivers will be required for switching in electrical domain such as

SFP+ transceivers [3].

With regard to optical interconnection networks, the switching is required to perform at the optical domain for all the network topologies thus removing E/O/E transceiver and electrical switches. A typical optical interconnection network for data center is shown in Fig. 1.1, where optical switches play a key role in the interconnectivity between servers.

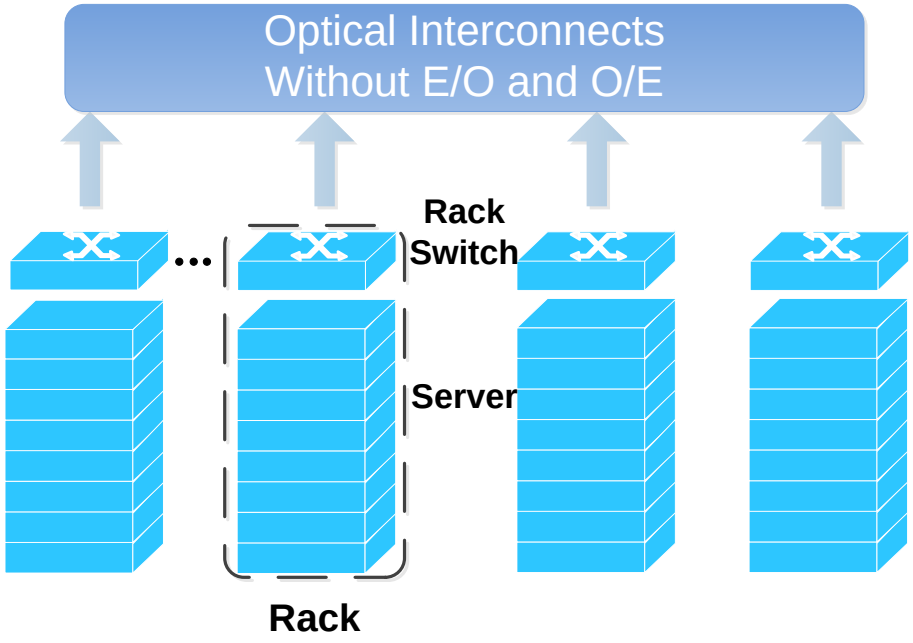


Fig. 1.1 Optical interconnection for data centers.

1.2 Silicon photonics interconnect

Exploiting the low cost and matured complementary metal oxide semiconductor (CMOS) fabrication facilities, silicon photonics has become one of the leading technologies for integrated photonics, which can be applied in high performance computing, optical telecommunication and data communication, optical sensors, and on-chip optical interconnect [5]. Recently, diverse silicon photonics devices integrated on silicon on insulator (SOI) have been demonstrated by academic groups and companies. It is the very low losses and high optical mode confinement of silicon waveguides that drive these innovations [6].

Due to the interest spurred by the vision of achieving a high-density optoelectronic integrated circuit, silicon photonics based device capabilities and manufacturability are advancing rapidly including the improvement in: 1) ring resonators, 2) integrated switch fabrics, and 3) hybrid silicon technology. The development of functional devices pave the way for on-chip interconnects based on silicon photonics. IBM, Intel and other companies turn to silicon photonics to solve the electronic limitations one after the other. A prototype that can shuffle data with fiber optics using silicon switches has been developed by Intel, as shown in Fig. 1.2. To realize various functionalities of silicon nanophotonic devices, high-density connection of optical inputs/outputs is necessary.

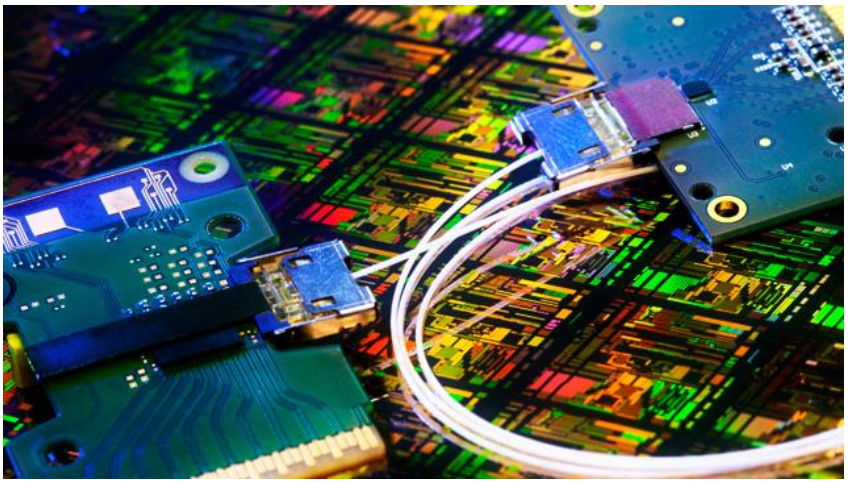


Fig. 1.2 A prototype that can shuffle data with fiber optics using silicon switches.

1.3 Motivations and contributions

An innovative scalable space-time multi-plane optical interconnection network was proposed using energy-efficient enabling technologies in [7]. The key technologies for the implementation of space-time architecture are the integrated passive devices and an M×M space-switch interconnection. The former integrated passive device, namely passive wavelength-stripped mapping (PWM), has already been designed and fabricated, while the latter space-switch is still under consideration.

The considered M×M space-switch interconnection consists of a broadcast-and-select implementation with M switches (1×M) and M couplers (M:1) configured in a tree structure. Semiconductor optical amplifiers (SOAs) have been deployed as gating elements and amplifiers in the space switch. Power consumption is reduced considerably by improving the energy proportionality with self-enabled SOAs. The impact of multiple cascaded SOAs on packets is an important requirement to assess in scalable optical space switch configurations. Due to parabolic gain profile, nonlinearities (*e.g.,* cross-gain modulation), and noise figure, the scalability of SOA-based optical switches becomes a challenge as the number of cascaded SOAs in the routing path increases.

An experimental recirculating loop is exploited to assess the scalability of multi-wavelength (WDM) energy-proportional optical space switches with different SOA gain/loss configurations [8]. Degradation due to cross-gain modulation (XGM) and amplified spontaneous emission (ASE) noise accumulation is evaluated in terms of bit-error-rate (BER) performance to assess port scalability. The impact of architecture configuration on scalability and energy efficiency is further evaluated. This investigation is agnostic to the architecture such that the results can be interpreted for different interconnection architectures by translating the number of cascaded SOAs to the corresponding number of port of a specific optical space switch configuration.

Along with the fiber-based components to implement the space switch, the SOA-based space-switch interconnection can also be integrated on chip. A large number of optical input and output (I/O) channels are needed to achieve large-scale integration of optoelectronic devices with silicon photonics. Recently, a pitch reducing optical fiber array (PROFA) with multi-channel optical input/output has been produced by Chiral Photonics for the fiber-to-chip and fiber-to-optical waveguide applications [9]. In order to increase the density of on-chip optical I/Os, an ultra dense silicon photonics interface of fibers and chips/photonic integrated circuits (PICs) is designed and fabricated. This PROFA interface can potentially enable a high-capacity on-chip optical interconnection.

1.4 Thesis overview

The thesis consists of five chapters including the introduction. In Chapter 2, the background of optical interconnection networks is presented. An overview of the optical interconnects for data center and several proposed interconnect schemes is given. The optical space switches are then discussed in terms of the architectures, particularly SOA-based configuration and the scalability and energy efficiency. The optical interconnects based on silicon photonics are discussed as well.

Chapter 3 investigates the development of FPGA controlled SOA-based optical space switch. The methodology employing a recirculating switching loop is illustrated. The experiment results on scalability are presented including the impact of polarization dependent gain (PDG), space switch scalability, XGM effect as well as architecture scalability and energy efficiency. Besides, some simulation results on optical-signal-to-noise ratio (OSNR) prediction and the cosimulation with OptiSystem using the SOA model are also presented.

Chapter 4 discusses the implementation of ultra dense silicon photonics interface, ranging from the on-chip PROFA and PIC interface, the design and simulation to the experimental results and analysis. The details on the modelling, grating coupler array and PROFA interface, and device layout are provided as well.

The last chapter presents a conclusion of the thesis work and discusses future research on SOA-based optical space switch and potential high capacity optical link.

Chapter 2

Optical interconnection networks

Over the last few years, the explosive increase of internet service driven from applications, such as streaming video, social networking and cloud computing creates, the demand for high bandwidth, throughput interconnection networks. As conventional electronic interconnections have reached its capacity limit, it is rather challenging to improve the performance of throughput and latency while maintaining low power consumption [10]. Optical interconnection network is a promising means of high bandwidth and low latency routing for future high performance computing platforms. Optical technologies have been deployed in the long-haul communication systems with fiber optic networks across the world. Different schemes have been proposed to exploit the light's high bandwidth such as Time Division Multiplexing (TDM), Wavelength Division Multiplexing (WDM) and diverse advanced modulation formats. Currently in data center, optical technology has been utilized only for point-to-point links to connect electrical switches, which employs power hungry E/O and O/E transceivers. Therefore, all optical networks using optical cross-connect, optical switches and reconfigurable optical add/drop multiplexers (ROADM) are required for higher bandwidth, reduced power consumption and reduced operation cost [11].

2.1 Optical interconnects for data center/HPC

A data center consists of computer systems and associated components used for high performance computing. The high level block diagram of a typical data center is demonstrated in Fig. 2.1 [3]. The emergence of cloud computing and other web applications leads to a dramatic increase of the network traffic inside data center [12]. As current technologies

based on electrical switches cannot face the network increase due to limited bandwidth and power consumption issue, optical interconnects become a promising solution.

There are two main requirements of data center in the near future, namely the traffic requirements and power consumption requirements. The immense web applications will keep increasing the internet network traffic resulting in a larger volume of network traffic inside the data centers. Besides, power consumption of the infrastructure leading to high operation cost is a major concern in the design of data centers as well [3].

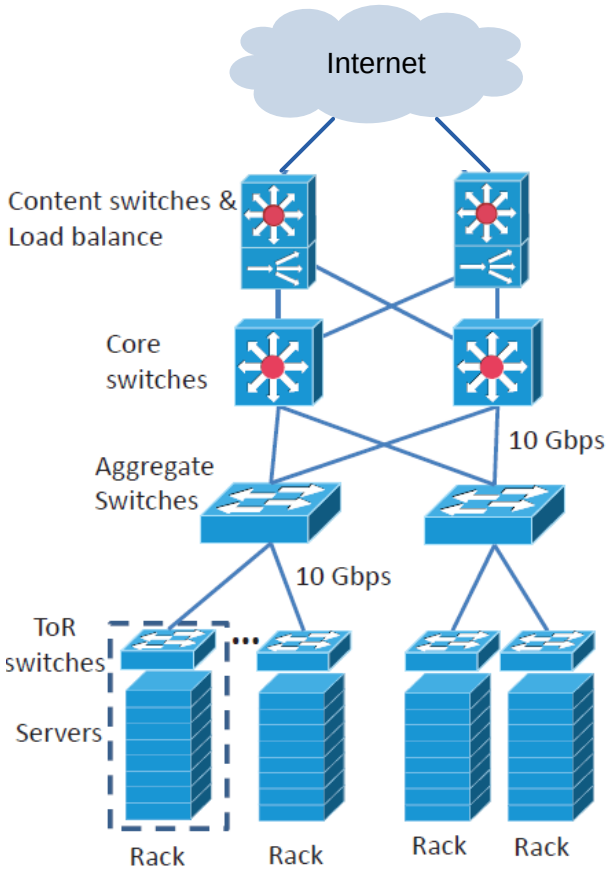


Fig. 2.1 Architecture for current data center [3].

The majority of optical interconnection architectures for data center are based on devices used in optical communication networks. The fundamental optical modules required for the implementation of optical interconnects are indicated.

1) *Splitter and Combiner:* A splitter or combiner is a passive device used to split or

combine optical signals in the optical network.

2) *Arrayed-Waveguide Grating (AWG):* AWGs are passive bit-rate transparent optical devices. They are used for routing each wavelength of an input to a different output.

3) *Wavelength Selective Switch (WSS):* WSS is a typical 1×N optical component that is used to partition the incoming set of wavelengths to different ports.

4) *Micro-Electro-Mechanical Systems switches (MEMS-switches):* MEMS optical switches are mechanical devices that physically rotate mirror arrays redirecting the lightwave to establish a connection between the input and the output.

5) *Semiconductor Optical Amplifier (SOA):* SOAs are optical amplifiers that can amplify input light through the injected carriers generated by a pump current.

6) *Tunable Wavelength Converter*: A tunable wavelength converter can generate a configurable wavelength for an incoming optical signal.

2.2 Optical interconnects schemes

With the advantage of high bandwidth and reduced power consumption, optical interconnection networks have attracted more and more interests for data center/HPC. Recently, diverse optical interconnects schemes have been proposed for data center networks. A general overview of several major architectures (*e.g.,* Helios, OSMOSIS project, Space-Wavelength) is provided below.

1) Helios: A hybrid optical electrical switch
N. Farrington *et al.* from UCSD, presented a hybrid electrical/optical switch architecture for modular data centers based on WDM named Helios [13]. Helios schemes utilize the architecture of typical 2-layer data center networks, consisting of top of rack switches and core switches. Top of rack switches are electrical switches while core switches can be electrical packet switches or optical circuit switches. The traditional electrical switches are used for the communication of all pod switches. The optical circuit switches are used to slowly change the communication between pod switches for high bandwidth. A small example of Helios architecture is depicted in Fig. 2.2.

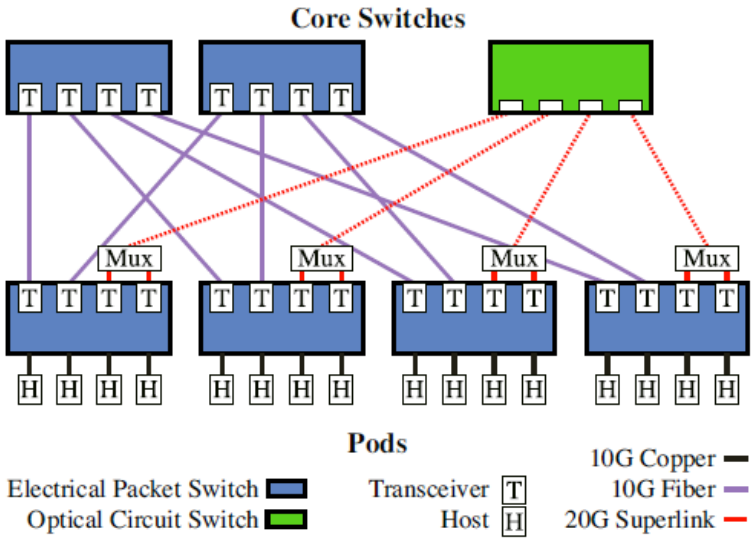


Fig. 2.2 Helios: a 2-layer network of pod switches and core switches [13].

2) The OSMOSIS project

In 2004, IBM and Corning together developed the Optical Shared Memory Supercomputer Interconnect System (OSMOSIS) project. The project is a low-latency optical broadcast-and-select (B&S) architecture using wavelength- and space-division multiplexing [14]. There are two different stages in the broadcast-and-select architecture. First, multiple wavelengths are multiplexed in a WDM line and are broadcasted to all the modules of the second stage using a coupler. SOAs are used as fiber-selector gates to select the wavelength that will be forwarded to the output in the second stage. The critical role of optical-switching technologies in large-scale parallel HPC systems is illustrated in this project. Fig. 2.3 is an overview of OSMOSIS system.

3) Space-time architecture

Liboiron-Ladouceur *et al.* have proposed an interconnection network based on space-time switching for data center [7]. In time-switched architecture, the packet is first compressed by expanding serial packets through wavelength-striped techniques and then switched among different ports. While in space-switched architecture, one fixed laser per port is required and a non-blocking SOA-based switch is used for establishing the connections in each time slot. This scheme combines the time and space switching efficiently. The schematic of space-time interconnection network is shown in Fig. 2.4.

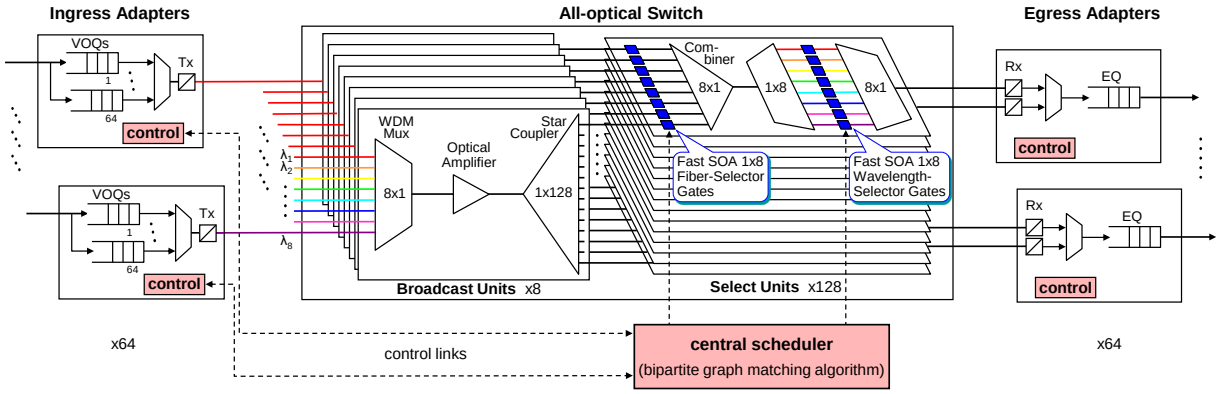


Fig. 2.3 An overview of OSMOSIS architecture [14].

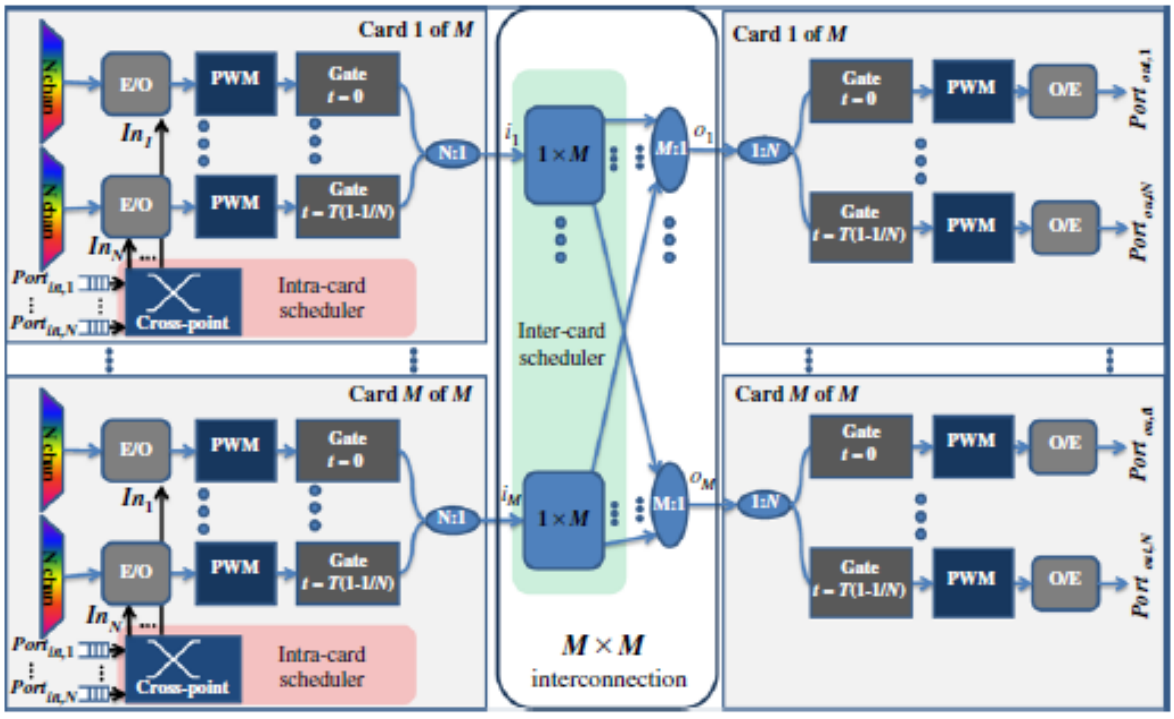


Fig. 2.4 Space-time interconnection network architecture for M cards and N ports [7].

4) Data vortex

Bergman *et al.* from Columbia University have presented a distributed interconnection network named Data Vortex, which targets HPC systems and data center interconnects [15]. The network consists of nodes that will route both packet and circuit switched traffic simultaneously using SOAs in a configurable manner. The SOAs are organized in a gate-array configuration and act as optical switching elements. A data vortex system composed of 12 input ports and 12 output ports has been implemented, as shown in Fig. 2.5.

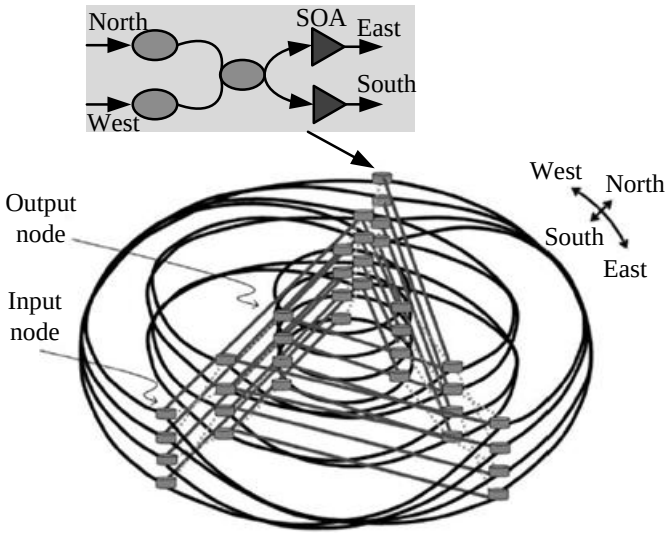


Fig. 2.5 The data vortex architecture [15].

Table 2.1 Summary of optical interconnect schemes

Architecture	Technology		WDM	Capacity limit	Scalability
	hybrid	all-optical			
Helios	Y		Y	Transceivers	Low
OSMOSIS		Y	Y	SOA	Medium
Space-time		Y	Y	SOA	High
Data vortex		Y		SOA	High

A qualitative comparison on the features of these schemes is provided in table 2.1. More details on different optical interconnects schemes can be found in [3].

2.3 Optical space switches

Optical space switches are key subsystems in optical cross-connects (OXCs) and ROADMs. These optical switches also have applications in more long-term communications scenarios such as optical packet switching (OPS). With the development of optical interconnection networks, optical space switches potentially play an important role in the interconnectivity between servers [16]. The main benefit of optical switching is to enable the routing of optical signals from an input to an output port without the need for conversion to electrical signals. The transfer function from electronics to optics makes optical switches independent of data rates and data protocols and leads to a reduction in the network equipment, an increase in the switching speed, and thus network throughput, and a potential decrease in power consumption.

SOA-based optical switches are one of the most common optical switching technologies. Different architectures can be employed to build large-scale switches. The scalability and energy efficiency are key factors to be considered when evaluating an optical switch.

2.3.1 SOA-based optical switch

SOA switches are one of the most common used optical switching technologies today [17]. The main technologies of current optical switching include:

1) *Micro-electro-mechanical System Devices:* Micro-electro-mechanical systems (MEMS) use tiny reflective surfaces to redirect the light beams to a desired port by either ricocheting the light off of neighboring reflective surfaces to a port or by steering the light beam directly to a port.

2) *Electro-optic Switches:* A 2×2 electro-optic switch is comprised of a directional coupler whose coupling ratio is changed by tuning the refractive index of the material in the coupling region. Lithium Niobate ($LiNbO_3$) is one of the commonly used materials.

3) *Thermo-optic Switches:* The principle of such switch is based on the thermo-optic effect. The effect consists of the variation of the refractive index of a dielectric material due to temperature variation of the material itself.

4) *Acousto-optic switches:* The operation of acousto-optic switches is based on the acousto-optic effect, which is the interaction between sound and light.

5) *Semiconductor Optical Amplifier (SOA) Switches:* An SOA can be used as an ON-OFF switch by changing the injected current. If there is no injected current, no population inversion is achieved and the input signal is absorbed by the device.

Most of optical switches discussed above have millisecond switching speed except for electro-optic and SOA switches. For the data center application, as switches typically handle packetized data and operate on a packet time-scale, SOAs with nanosecond response time have been proposed as gating elements to minimize the guard time penalty. Their inherent amplification characteristics also allow SOAs to act as amplifiers compensating for losses in the space switch. Besides, SOAs are mature components that do not suffer from path-dependent impairments and are integrable. Large size SOA-based space switches have been designed with different configurations.

2.3.2 Space switch architectures

As indicated in [18], small switches (*e.g.,* 1×2 and 2×2) are the basic elements for switch fabrics. Large-scale switches can be realized by cascading small-size switches. Different architectures can be utilized to build large SOA-based switches, namely single-stage (Spanke) and multi-stage (crossbar, Beneš, Spanke-Beneš) [18] [19].

1) *Spanke:* The Spanke architecture shown in Fig. 2.6(a) is suitable for building large nonintegrated switches. The architecture is strict-sense non-blocking, which means an unused input port can be connected to any unused output port. An n×n switch is made by combining n 1×n switches, along with n n×1 switches. Thus, 2n (n-1)×2 switches are required and each path has a length of $2\log_2(n)$.

2) *Crossbar:* A n×n crossbar consists of n^2 2×2 switches, as shown in Fig. 2.6(b). By approximately setting the states of the 2×2 switches, the interconnection between the inputs and the outputs can be achieved. The crossbar architecture is wide-sense non-blocking. One of the main drawbacks of the crossbar architecture is different path lengths.

3) *Beneš:* The Beneš switching architecture shown in Fig. 2.6(c) is rearrangeably non-blocking and is one of the most efficient architectures in terms of the required number of 2×2 switches to build larger scale switches. A n×n Beneš switch requires $(n/2)(2\log_2(n) - 1)$ 2×2 switches, n being a power of 2. The loss is the same for each path in the switch. But there are two main drawbacks: it is not wide-sense non-blocking and a number of waveguide crossovers are required.

4) *Spanke-Beneš:* It is a good compromise between the crossbar and Beneš switch architectures shown in Fig. 2.6(d). Spanke-Beneš is rearrangeably non-blocking and requires n(n-1)/2 switches. It is not wide-sense non-blocking and the path length is not uniform.

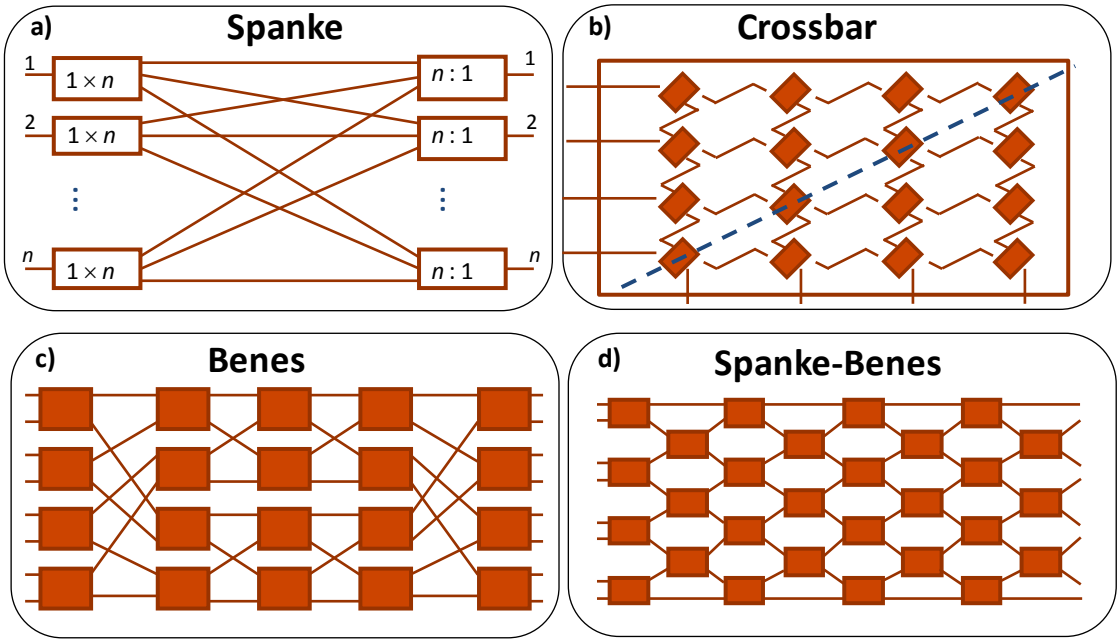


Fig. 2.6 Space switch architectures: (a) n×n Spanke, (b) 4×4 Crossbar, (c) 8×8 Beneš, and (d) 8×8 Spanke-Beneš [18].

With regard to SOA-based space switch in single-stage structure, SOAs are employed as gating or switching element for only one stage while large amount of SOAs are used to compensate for the split/combine loss. The number of cascaded SOAs is reduced but the total number of SOAs is increased. Instead, the total number of SOAs is limited for

multi-stage space switch while larger number of cascaded SOAs is needed to compensate for the smaller loss between adjacent gating elements.

2.3.3 Scalability and energy efficiency

The performance of an optical switch is determined by many parameters. One of the most important parameters is the switching time. The requirement of switching time is different for different applications. Other important parameters of a switch are insertion loss, crosstalk, extinction ratio (on-off ratio) and polarization dependent loss (PDL), *etc.*

Nowadays, scalability and energy efficiency become more and more important in data centers and are imposing tight constraints on the networking infrastructure connecting numerous servers. The scalability refers to the ability to build switches with large port counts that can perform adequately under an increased load. The energy efficiency can be assessed by the energy consumption per bit of the switch.

Along with the increase of server size, the power drained by the servers is growing even faster. Although the server computational performance improves by a factor of three every two years, the energy efficiency of servers is unable to keep up the same rate (limited to approximately double every two years [20]). Besides, the low server utilization and non-trivial amount of power drained by the networking infrastructure make the situation even worse. These pose challenging design requirements of high throughput and scalable architectures for the optical interconnection networks with power consumption limited and proportional to the utilization of the network [21–23].

2.4 Silicon photonics for optical interconnects

Silicon is the workhorse of the semiconductor industry, which serves as the optical medium for silicon photonics. Silicon photonics offers many unique advantages compared to other photonic platforms. Its extremely high contrast between the refractive index of the core and the surrounding cladding enables optical modes to be confined and guided by devices with sub-wavelength dimensions. Silicon photonics is compatible with standard CMOS fabrication process, enabling dense integration with advanced microelectronics and low-cost mass volume production.

Enabled by silicon photonics technology, optical interconnects can potentially play a key role in computing and communication industries. The enduring pursuits of computing performance improvement, combined with stringent requirement of power consumption, has fostered the ever-growing parallel computation associated with chip multiprocessors, memory systems, data centers and HPC systems. Brand new ideas for on- and off-chip communications are needed to sustain the parallelism growths. Chip-scale silicon photonic interconnection networks offer extremely high bandwidth scalability and meet the power constraints. High-performance silicon photonic devices have been produced by the existing photonic platform to realize different types of networks. Furthermore, the coupling between nanophotonic waveguides and SM fibers has been developed simultaneously.

2.4.1 Silicon photonic building blocks

Nearly all required functionalities of silicon photonics for optical interconnection networks have been demonstrated in recent years. Some of the basic silicon photonic devices are [24].

1) *Silicon waveguides:* The waveguide is the fundamental silicon photonic component that can carry high-speed optical data from one point to another. Wavelength-parallel optical signal with terabit-per-second (Tb/s) can be transported through silicon waveguides across the entire chip.

2) *Silicon electro-optic modulators:* The electro-optic modulator is a critical device to enable high-speed E/O conversion, typically encoding data on a single-wavelength channel that can be multiplexed with other optical signals through WDM, forming a cohesive wavelength-parallel optical signal. The most common silicon electro-optic modulators are Mach-Zehnder interferometer and ring resonator based modulators.

3) *Silicon electro-optic switches:* There are mainly two kinds of silicon photonics switches. One is based on Mach-Zehnder interferometer. The wavelength insensitive MZI optical switch is reported with wavelength insensitive directional couplers to increase spectral bandwidth. The other one is the microring resonator electro-optic broadband switches, which embraces the advantages of ultrahigh bandwidth and low energy dissipation.

4) *Photodetectors:* The photodetectors are used to translate an incoming high-speed optical signal into the electrical signal at the end of the optical communication link.

Both Germanium and Silicon with crystal defects can be utilized to produce the photodetector for silicon photonics.

5) *Couplers:* Couplers are critical silicon photonic devices allowing on-chip devices to interface with off-chip components. Because of the high index contrast between the silicon core and silicon dioxide cladding, the optical mode size for single-mode operation is extremely small in silicon waveguide. Therefore, an efficient coupling between the optical mode of waveguides and single-mode fibers is challenging to obtain.

2.4.2 Coupling between nanophotonic waveguide and optical fiber

Exploiting the high refractive index contrast on silicon photonic waveguides enables a drastic scaling down of the footprint of integrated optical components. However, interfacing on-chip nanophotonic devices with SM fiber becomes rather challenging due to the huge mismatch in mode size between optical fiber and silicon waveguide, especially for large-scale integration of optical functions [25].

The key parameters in developing adequate coupling techniques are insertion loss, integration density, bandwidth density, crosstalk, reflectivity and scalability. Various promising fiber-chip coupling methods have been proposed in the literature, mainly lateral and vertical techniques. One common solution is to use a spot size converter to transform the size of mode of the nanophotonic waveguide to that of the optical fiber [26]. A three-dimensional adiabatic taper structure can be used as the spot size converter. However, this technology requiring a tilted facet by etch process is not CMOS compatible. The second approach is to change the spot size using a lateral inverted taper structure [27]. To interface with a SM fiber, a low refractive index waveguide with cross-sectional dimensions comparable to that of the SM fiber core is required. This approach suffers from two significant disadvantages. A huge topography is required as well as a taper structure of thousands of micrometers in length on the photonic integrated circuits.

Another kind of optical interface between a standard SM fiber and nanophotonic waveguide circuit is to use diffractive grating structures [28]. The lateral adaptation of the mode size is realized by a conventional in-plane taper structure in these coupling structures. However, the interfacing with the optical fiber is obtained by redirecting the light exiting the on-chip integration out of the plane of the photonic integrated circuit, using a diffrac-

tion grating (vice versa for the optical coupling from SM fiber to the photonic integrated circuits). The schematic lateral view of three approaches discussed above for fiber-chip coupling is illustrated in Fig. 2.7.

According to the IMEC passive fabrication specifications, 31% (-5dB) coupling efficient and 3-dB bandwidth of 60 nm can be realized between the single mode fiber and strip waveguide. This is achievable without additional process such as epitaxy, deposition or etching.

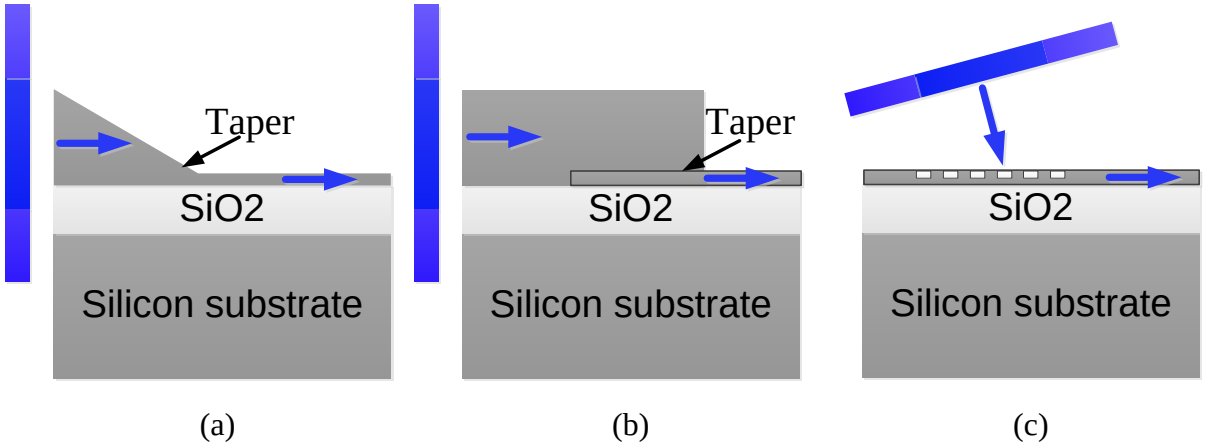


Fig. 2.7 Comparison of two spot-size converter approaches (a) 3D adiabatic tapering, (b) lateral inverted tapers, and (c) diffractive grating based coupling.

2.5 Conclusion

An overview of optical interconnection networks is given, including optical interconnects for data center/HPC systems and several proposed optical interconnects schemes. One of commonly used optical interconnects, SOA-based optical space switches, is discussed in detail. Different architectures and key performance parameters of space switch are presented. Besides, recent development of silicon photonics for optical interconnects is introduced. The basic silicon photonics building blocks are presented as well as the coupling between nanophotonic waveguide and standard optical fiber.

Chapter 3

Scalability of SOA-based optical space switch

As mentioned in chapter 1, an innovative scalable space-time multi-plane optical interconnection network is proposed using energy-efficient enabling technologies in [7]. For the interconnection network, multi-plane architectures are organized in cards, each one with multiple ports that match well with the modular architecture paradigm for data center [13]. The control of the network is realized by a two-step (Inter-Card and Intra-Card) scheduler [29] based on a field-programming gate array (FPGA). One key technology for the implementation of space-time architecture is an M×M SOA-based optical space switches.

In the optical space switch, SOAs act as both gating elements and amplifiers. The impact of multiple cascaded SOAs on signal performance is an important requirement to assess in scalable optical space switch configurations. Because of parabolic gain profile, nonlinearities (*e.g.,* cross-gain modulation (XGM)), and noise figure, the scalability of SOA-based optical switches becomes a challenge with a large number of cascaded SOAs in each routing path. However, few investigations have studied the effect of a series of SOAs in the routing path on multi-channel (WDM) optical packets. The physical layer scalability has been investigated at fixed gain in [30] and in the context of SOA-based ROADM [31]. Further, energy efficiency of the space switch also becomes a key issue for large-scale interconnection networks.

3.1 M×M space switch interconnection

The M×M space switch interconnection consists of a broadcast-and-select implementation with M switches (1×M) and M couplers (M:1) configured in a Spanke architecture. Each 1×M space switch is configured in a binary tree structure, while each M:1 combiner is another binary tree structure with SOAs, as shown in Fig. 3.1.

The SOAs on the terminal branches of 1×M space switch act as amplifiers as well as switches that can enable or block the incoming optical signal. Additional SOAs are required after several stages to compensate for the splitting/combining losses. The inter-card scheduler decides that which input port (*e.g.*, i_k) to be connected to the output port o_n during a given time-slot. Only the SOAs in the routing path with data transmission are enabled to achieve an energy-efficient implementation, while no current is driving the unused SOAs, dissipating minimum power. The SOAs in the 1×M space switch are gated by the FPGA-based scheduler while the SOAs in the M:1 combiner are controlled by a self-enabled mechanism to minimize the power consumption.

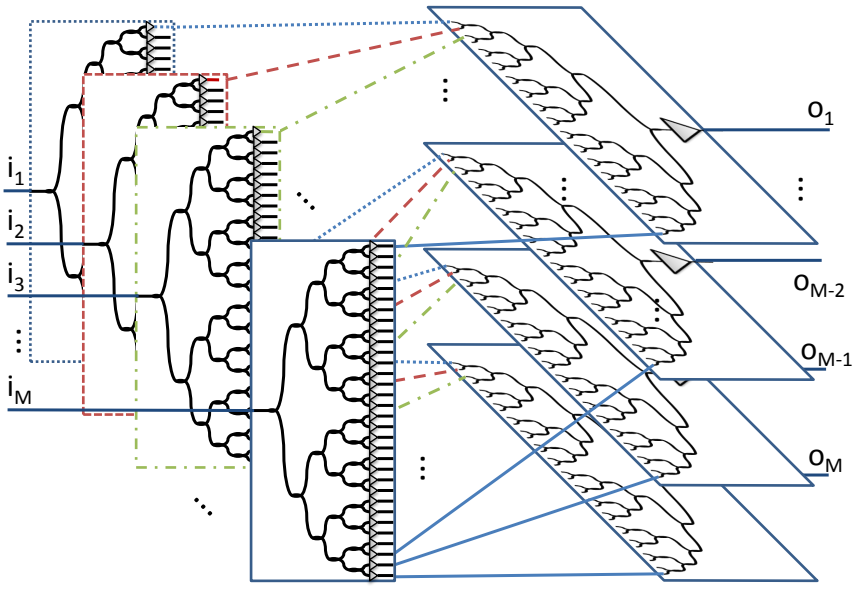


Fig. 3.1 Illustration of M×M space-switch interconnection [7].

Fig. 3.2 illustrates the working principle of the self-enabled SOA. A small amount (*e.g.*, 10%) of optical power of the incoming packets is detected and an electrical signal with a

pulse width equal to the propagating packet length is generated. The generated electrical signal is sent to the current driver that injects current in the SOA active region to provide the necessary gain to the input signals. Since the photodetector exhibits dark current in the order of nA, powering the photodetector consumes less power compared to powering the SOA with driving current in the order of mA.

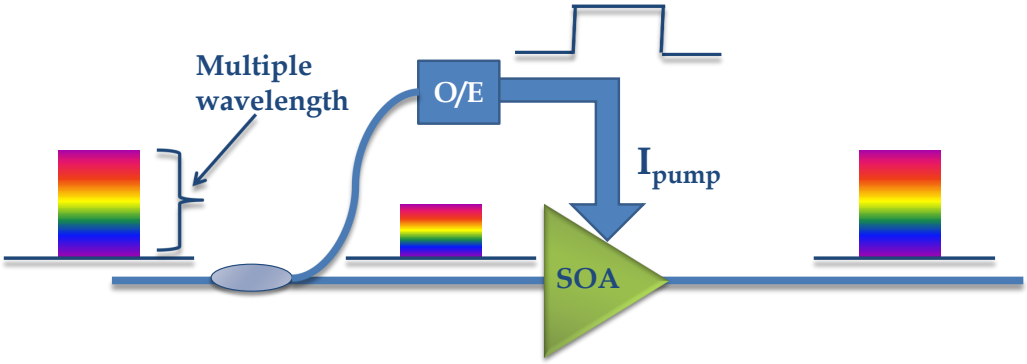


Fig. 3.2 Energy-efficient self-enabled SOA [7].

3.2 FPGA-controlled recirculating switching loop

With large number of SOA gates acting both as switches and amplifiers of WDM signals, the physical layer scalability becomes a challenge in the interconnection architecture. An experimental recirculating loop using FPGA- or self-enabled SOAs is exploited to assess the scalability of multi-wavelength energy-proportional optical space switches [8].

3.2.1 Methodology

Given a specific architecture for the SOA-based space switch (*e.g.,* single-stage Spanke architecture as shown in Fig. 3.3(a) and 3.3(b) respectively), the number of ports corresponds to a number of SOAs in series in the data path between two interconnected ports. Scalability of the space switch in terms of number of ports translates into number of cascaded SOAs. Here assuming that the number of crossed SOAs is uniform for any given paths, and the loss and gain between each switching stage is the same (Fig. 3.3(b)).

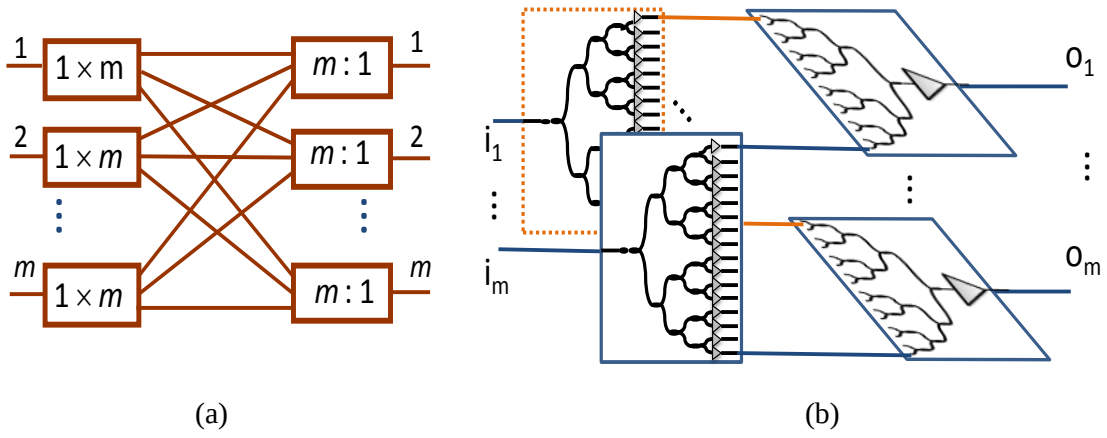


Fig. 3.3 (a) Single-stage optical space switch architecture, and (b) SOA-based m×m space switch design for m=16.

3.2.2 Recirculating loop test-bed

The recirculating loop of a few-meter length shown in Fig. 3.4 can be used to evaluate the scalability of space switch by propagating the optical signals into a predetermined number of loops corresponding to the number of SOAs in series.

The transmitter (TX) is composed of four distributed-feedback (DFB) lasers externally modulated at 10 Gb/s (non-return-to-zero, NRZ) with a pseudo-random bit sequence (PRBS, 2^{10}-1 bits) generated by a pulse pattern generator (PPG). The four channels (1546.62∼1549.02 nm, $\triangle\lambda$=0.8 nm) are decorrelated by slightly more than one bit with an 8.3-km-long single mode fiber (141 ps/nm). Note that more precise (multiple of the bit period) and longer decorrelation would be required to properly represent completely uncorrelated data transmission. The inset in Fig. 3.4 shows the control and gating digital signals generated by an Altera Cyclone IV Field Programmable Gate Array (FPGA) clocked at 50 MHz by the PPG. A 40-ns optical packet is generated by the SOA labeled *Gating SOA*. The packets are injected into the 80-ns-long recirculating loop every 2 μs enabling a maximum of 25-loop propagation. The optical packets exit the loop through the SOA labeled *Output SOA*. Controlled by the FPGA representing a scheduler, the SOA in the loop (*Loop SOA*) follows the energy-proportionality concept where it remains off (or idle) when not routing packets. The SOA can also be self-enabled by the propagating packet detected by a photodiode (O/E) as depicted in [7]. The *Output SOA* is enabled by the gating pulse regenerated by the FPGA from the incoming packet. The commercial SOAs (Alphion 02P262) have a

saturation output power of 8.3 dBm, a maximum polarization dependent gain (PDG) of 0.6 dB, an average noise figure of 8.3 dB and a gain recovery time of 140 ps. Further, the measured on/off contrast ratio is 40 dB such that crosstalk can be considered negligible in this investigation. The small signal bandwidths (*i.e.*, 3-dB bandwidth) of the SOAs are 75 nm and 60 nm in the linear and saturation regimes, respectively. The SOA gain compensates for the loss in the loop based on the Spanke configuration under study. When disabled, no current is driving the SOA.

On the receiver side (RX), the optical spectrum is measured by an Optical Spectrum Analyzer (OSA) with a resolution of 0.1 nm. An optical bandpass filter (BPF) with a bandwidth of 0.3 nm is used in front of the photodetector (PD) with an electrical gain of 20 dB and a bandwidth of 15 GHz. BER measurements on all WDM channels are carried out by an externally gated error detector (ED).

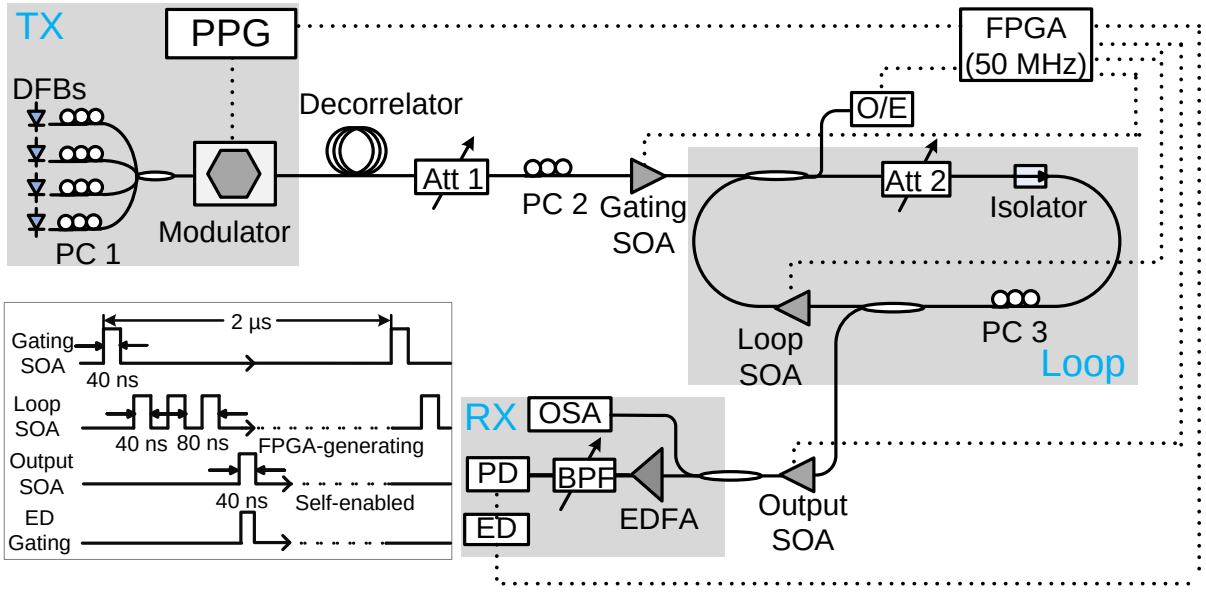


Fig. 3.4 Recirculating loop test-bed (inset: FPGA generated control and gating signals).

3.3 Experimental scalability results

The scalability of SOA-based optical space switches is assessed by determining the maximum number of loops the multi-channel optical packet propagates through while maintain-

ing a BER performance below 10^{-9}. The number of loops corresponds to the maximum number of cascaded SOAs (minus one (*Output SOA*)). Three gain/loss configurations (8.5 dB, 11.0 dB, and 13.0 dB) representative of different interconnection networks are investigated by adjusting the gain of *Loop SOA*and the loss between SOAs (*Att 2*). The SOA compensates for the loss introduced by couplers and connectors in a given architecture. For all configurations, the total output power after the SOA (*Loop SOA*) for the first loop is set to -2.0 dBm, ensuring that the SOA initially operates in the linear regime. Consequently, the input channel power differs for each of the gain/loss configuration: -16.5 dBm (8.5 dB), -19.0 dBm (11.0 dB), and -21.0 dBm (13.0 dB). Note that after few loops the operating regime of the SOA changes to saturation as ASE noise accumulates at each loop.

3.3.1 Impact of polarization dependent gain

As SOA exhibits PDG, the accumulation of even small PDG becomes significant in optical space switches with multiple crossed SOAs [32]. Also, PDG is random in a real system, which makes the loop to test the worst case scenario. By adjusting the polarization controller in the loop (*PC 3* in Fig. 3.4), the power difference between maximum and minimum cumulative PDG increases after each loop and depends on the gain/loss configuration (Fig. 3.5). After 15 SOAs, the signal power difference for the three configurations is: 5.6 dB or 0.4 dB/SOA at 8.5 dB (black), 1.5 dB or 0.1 dB/SOA at 11.0 dB (blue), and 2.8 dB or 0.2 dB/SOA at 13.0 dB (red). This indicates that cumulative PDG strongly depends on the SOA gain. As PDG depends on compressive or tensile strain of bulk materials in the active region, it can be set for a specific current injection [33]. Thus, the impact of cumulative PDG on the physical layer scalability of space switch can be reduced through proper active region design for an expected SOA gain. In such context, the scalability assessment is evaluated for the average of the two extreme cases (dashed lines in Fig. 3.5).

3.3.2 Space switch scalability

The BER performance as a function of the number of cascaded SOA gates for the least performing channel (1547.42-nm) is reported in Fig. 3.6. In fact, the performance difference of different channels is mainly caused by the parabolic shape of the SOA gain. The least performing channel is the one with a wavelength that is the furthest away from the peak gain. The signal degradation caused by XGM and ASE accumulation is evident in the eye

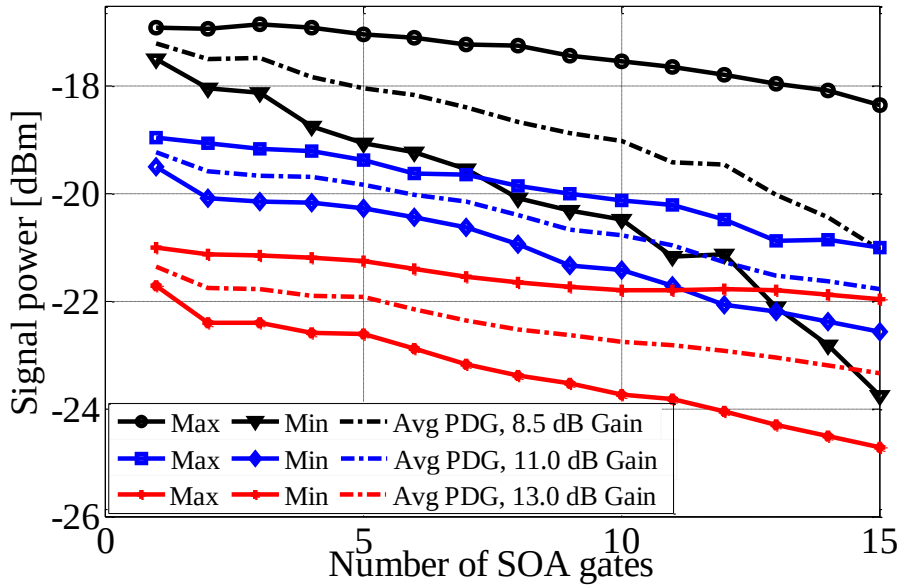


Fig. 3.5 Optical signal power versus number of cascaded SOAs for three configurations.

diagrams. Greater scalability at lower gain is attributed to lower ASE noise accumulation delaying the onset of saturation, but leading to enhanced XGM detrimental effect. It is also important to point out that the input OSNR is larger at lower gain as the same SOA output power is maintained for three gain/loss configurations. Consequently, the optical signal is more robust to the overall signal degradation at lower gain than at higher gain.

The OSNR penalty as a function of the number of cascaded SOAs and the BER as a function of measured OSNR are shown in Fig. 3.7(a) and 3.7(b). Table 1 summarizes the key points from the measurements. It can be observed that though the measured noise figure (NF) is slightly smaller at higher gain (7.0 dB vs. 7.6 dB), the SOA saturates more rapidly leading to lower scalability (14 vs. 19 cascaded SOAs). The input power dynamic range is narrow at the scalability limit, but increases to more than 2 dB by reducing the number of cascaded SOAs by two. The OSNR penalty is similar regardless of the gain/loss configuration (9.5 dB) due to the optimized input OSNR. However, the corresponding OSNR for BER below 10^{-9} differs by up to 2 dB between low and high gain/loss configurations. This results from the impact of XGM, which is quantified next by analyzing the amplitude histogram of the eye diagram.

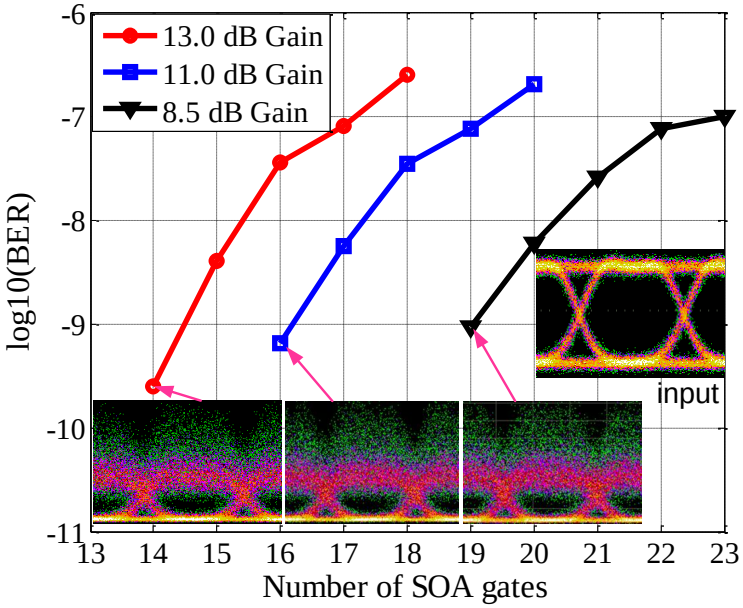


Fig. 3.6 Measurement for the three configurations: BER measurements versus number of cascaded SOAs with corresponding optical eye diagrams (BER$< 10^{-9}$).

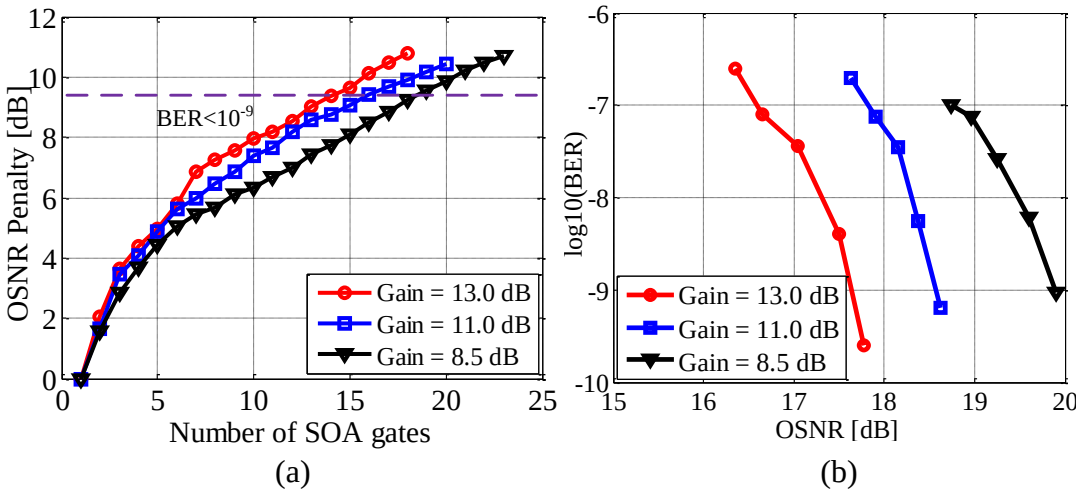


Fig. 3.7 Measurement for the three configurations: (a) OSNR penalty as a function of cascaded SOAs, (b) BER versus OSNR.

Table 3.1 Performance for the different gain/loss configurations

Parameters / Gain	8.5 dB	11.0 dB	13.0 dB
Max. number of cascaded SOAs (BER< 10^{-9})	19	16	14
OSNR(BER< 10^{-9}) [dB]	19.8	18.6	17.8
OSNR Penalty [dB]	9.5	9.4	9.4
Input Dynamic Range [dB]	0.5	0.4	0.25
Max. SOAs × Gain [dB]	161.5	176	182
Measured NF [dB]	7.6	7.2	7.0
Input Saturation [dBm]	-1.2	-2.0	-2.6
Injection Current [mA]	92	110	132

3.3.3 Cross gain modulation effect

As indicated in [34] [35], the amplitude histogram of the transmitted signal follows a non-central chi-squared distribution when optical amplifiers are the dominant source of noise. Fig. 3.8 presents the amplitude histogram of the captured signal for the 8.5 dB gain/loss configuration (BER< 10^{-9}). The right tail of the occurrence distribution corresponds to the overshoot in the signal. The amplitude of the overshoot can be investigated to understand XGM as optical packets propagate through a series of SOAs. In this methodology, the overshoot amplitude corresponds to the standard deviation of signals covering the entire occurrence greater than the mean amplitude for a logical bit one. In Fig. 3.9, the overshoot amplitude is plotted as a function of the number of cascaded SOAs through which the signal propagated. The comparison of overshoot between single-channel and multi-channel optical packets under the same conditions of OSNR and signal power. A polynomial fit is revealing the trends whereas the difference is shown in the figure inset and reveals the degradation caused by XGM.

Common to all configurations, the amplitude of overshoot first increases with the number of cascaded SOAs until it reaches a peak value. Then as the SOA reaches saturation and a limited gain is provided to the channel, the amplitude of overshoot decreases as the signal power drops since the loss is no longer fully compensated. For lower gain, the amplitude of overshoot increases faster with the number of cascaded SOAs and becomes

larger compared to the high gain/loss configuration. This indicates the important finding that the impact of XGM is more severe at lower gain in spite of higher OSNR. The reason is mainly due to the higher input channel power to the SOA leading to more XGM. The OSNR optimization at lower gain is necessary to overcome the degradation of ASE noise accumulation for best BER performance. Greater scalability is possible by increasing the input power while maintaining the total optical power under the nonlinear threshold [31].

In fact, there is an optimum input channel power for each gain/loss configuration balancing the impact of XGM and OSNR degradation from ASE noise accumulation. For the lower gain/loss configuration of 8.5 dB, the measured OSNR for a performance of BER $< 10^{-9}$ (after 19 cascaded SOAs) is higher compared to other gain/loss configurations. This indicates that degradation due to XGM is mainly responsible for limiting the BER performance rather than OSNR. Hence, the maximum number of cascaded SOAs can be predicted if both XGM and OSNR degradation are taken into account.

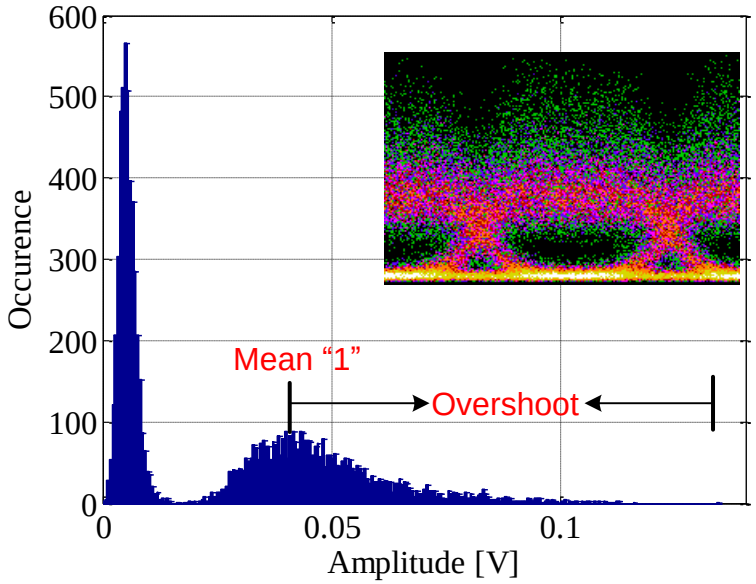


Fig. 3.8 Amplitude histogram of signal after 19 SOAs (BER$< 10^{-9}$), inset: corresponding eye diagram.

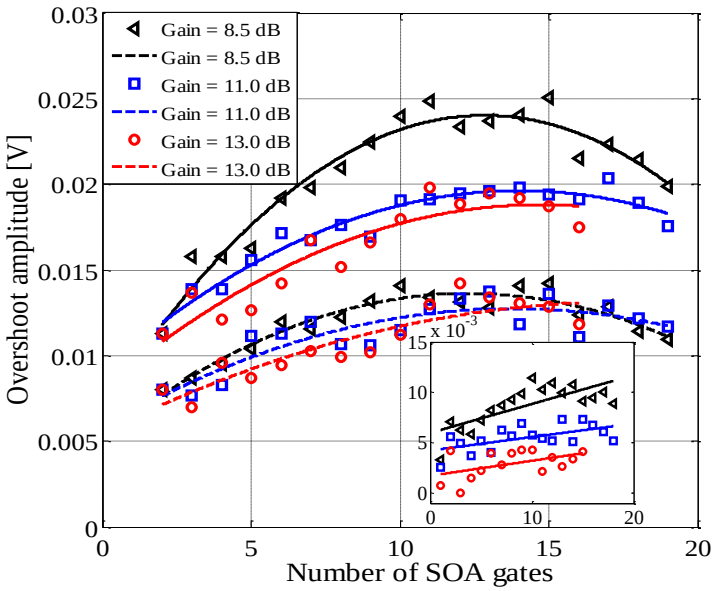


Fig. 3.9 Overshoot of optical signals vs. cascaded SOA gates for single channel (dashed lines) and multi-channel (solid lines). (Inset: difference between the overshoot)

3.3.4 Architecture scalability and energy efficiency

Despite larger number of cascaded SOAs possible at lower gain, better performance is not necessarily obtained when considering the total power consumption. For a given single-stage architecture and port number, lower gain SOA leads to more cascaded SOAs required to compensate for the passive splitters and combiner losses in a given optical space switch architecture. This configuration increases the total number of SOAs potentially leading to greater energy consumption [36]. Thus, high gain SOA should be used in single-stage optical space switch architectures. Lower gain SOA should be used in multi-stage switch architecture where more cascaded SOAs are required. For the same number of port, the required number of cascaded SOAs in the routing path and the total number of SOAs depend on the space switch architectures.

Regarding to single-stage architecture, a small number of high-gain cascaded SOAs can enable large port count. In proposed architectures in [7] [36], a path crossing 14 SOAs for a 13.0-dB gain/loss configuration corresponds to a 10^9 port space switch. For the same number of ports, eight additional SOAs would be required in each routing path for

a lower gain/loss configuration (8.5 dB) to compensate for the loss without better BER performance. Such architecture would obviously be more complex and lead to an overall higher power consumption. Higher gain/loss configuration should be favored combined with self-enabled techniques for an energy-proportional consumption [36]. On the other hand, in multi-stage space switches (*e.g.,* Beneš), the losses between gating elements (SOAs) are inherently small and multiple cascading switching stages are required. Thus lower SOA gain is preferred to compensate for the smaller SOA to SOA losses and enhance the scalability.

3.4 Simulation results

From the discussion above, it is known that the OSNR degradation and penalty of an SOA-based space switch act as significant predictors of their scalability, especially operating at high gain. Although the behavior of single SOA is well understood and accurately modeled, the increased ASE noise as a result of the concatenation of multiple SOAs should also be taken into account in the model. The WDM signals accompanied with increasing noise will change the behavior of cascaded SOAs. Besides, such SOA model can be applied to simulate the entire proposed space switch effectively combined with other tools.

3.4.1 OSNR prediction based on SOA model

An SOA model has been developed based on the steady-state wideband SOA model [37]. The model enables a numerical evaluation of signal power degradation resulting from ASE accumulation for a cascade of SOAs. Fig. 3.10 presents the number of SOA gates as a function of signal power (top figure) and ASE noise power (bottom figure) at 13.5-dB gain for the 1547.42-nm channel. The measurements of signal and noise powers are performed without adjusting the polarization in the loop. Although PDG leads to the variation in the signal power (pink circles and triangles in Fig. 3.10) as before, a good agreement between experiment and simulation results is clearly visible. As the number of SOA gates increases to 15, the ASE noise power increases by 8.5 dB and the signal power degrades by 2.5 dB corresponding to an 11.0-dB OSNR degradation. The optical spectrum representing output signals of all channels are indicated in Fig. 3.11, where the OSNR penalty can be easily calculated. The inset in Fig. 3.11 is the optical spectrum covering the C-band. Thereupon, the scalability at each gain can be predicted from the OSNR penalty induced by the cascade of SOA gates for the worst performing channel of the WDM packet.

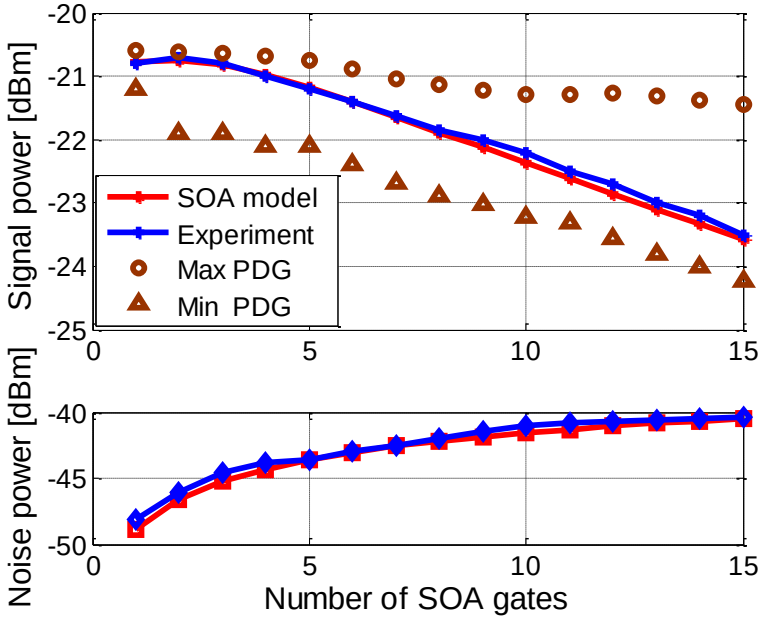


Fig. 3.10 Degradation of signal power and accumulation of ASE noise power versus number of SOA gates obtained from the SOA model and experiment.

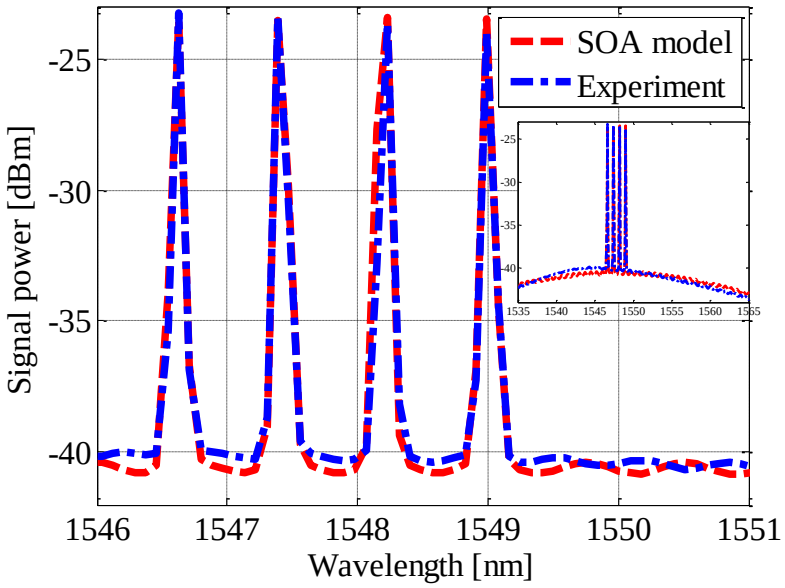


Fig. 3.11 Output optical spectrum from SOA model and experiment results.

3.4.2 Cosimulation between SOA model and OptiSystem

OptiSystem developed by Optiwave is a commercial simulation software for optical communication system and practical applications of optical networks. It can be used to plan, test and simulate optical links in the transmission layer. The developed SOA model based on Matlab is able to be incorporated into OptiSystem to assess the performance of the SOA-based optical space switches.

The characterization of the SOA model including the gain profile and ASE spectrum is performed compared to the characteristics of the wideband traveling wave SOA in OptiSystem. The schematic of simulation setup is illustrated in Fig. 3.12. The input power (continuous wave (CW)) and injected current to the SOA are -20 dBm and 150 mA. The structure parameters are set to be the same for the SOA model and wideband travelling wave SOA. The obtained gain profile and ASE spectrum from simulation and experiment are presented in Fig. 3.13 and Fig. 3.14.

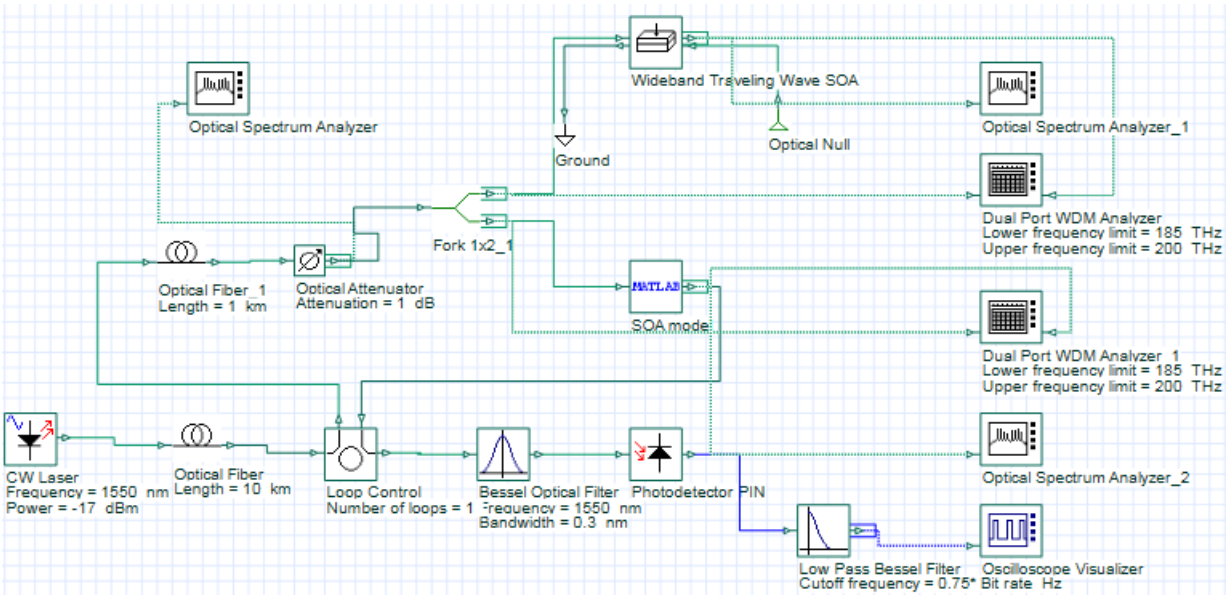


Fig. 3.12 Schematic of simulation setup with OptiSystem.

A good match between the developed SOA model and experiment is achieved from the gain profile and ASE spectrum in Fig. 3.13 and 3.14. However, the gain is much higher while the ASE power is much lower for the wideband SOA in OptiSystem compared to the SOA model. The main reason for this difference is that the SOA model is developed based

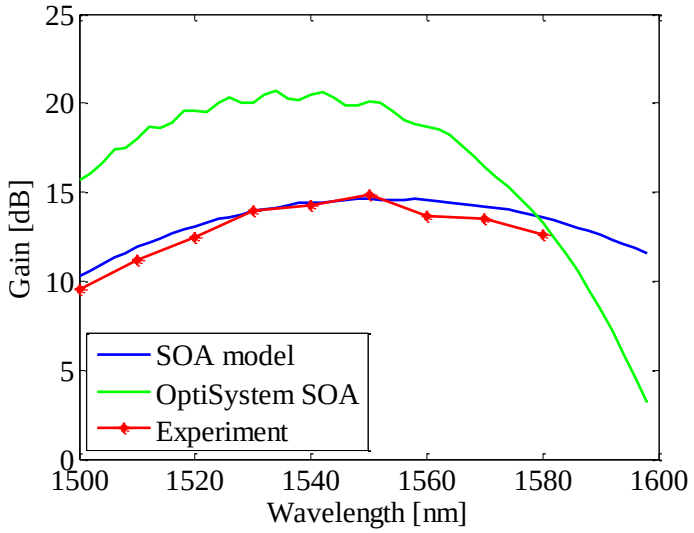


Fig. 3.13 The obtained gain profile of SOA from simulation and experiment.

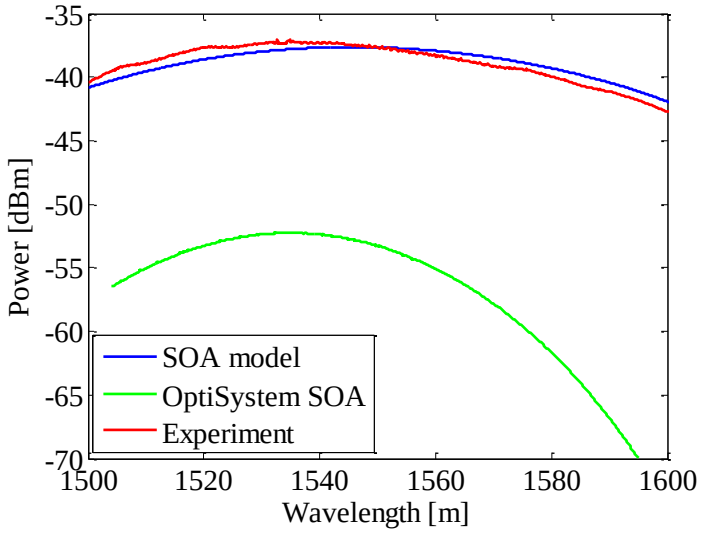


Fig. 3.14 The obtained ASE spectrum of SOA from simulation and experiment.

on the performance characterization of the same SOAs in experiment while the wideband SOA in OptiSystem is modeled by Optiwave separately. Such characterization will enable a better match between the simulation of the proposed SOA-based architecture and the corresponding experiment using the developed SOA model.

The cosimulation between the developed SOA model and OptiSystem has not been completed yet. Ideally, to fully assess the performance of the SOA-based space switch transmitting modulated optical signals, the dynamic performance of SOAs is required to be modeled as well as the nonlinear effects such as cross phase modulation and XGM in SOAs. Because both of them have not been characterized in the developed model, further investigation is needed to model the dynamic performance and nonlinear effects.

3.5 Conclusion

In this chapter, the evaluation of the scalability of SOA-based optical space switch based on a recirculating loop with FPGA-controlled and self-enabled SOAs is presented. The M×M space switch interconnection and FPGA-controlled recirculating switching loop test-bed are discussed in detail.

The experiment assessed the maximum numbers of cascaded SOAs that a multi-channel optical packet can propagate while maintaining a BER below 10^{-9}. The scalability limitation is mainly caused by the impact of XGM and OSNR degradation from ASE noise accumulation. At high gain, the signals suffer from the OSNR degradation. However, XGM plays a more detrimental role in the performance with greater pre-balanced input power as the gain is reduced. The results also confirm that the scalability of space switches with high gain/loss configuration remains possible (up to 14 SOAs at BER $< 10^{-9}$) leading to more energy-efficient single-stage space switch as less SOAs are needed. Lower gain/loss configuration leads to enhanced scalability (up to 19 SOAs) and can be recommended for multi-stage switching architectures.

An SOA model as OSNR predictor has been discussed as well. A good agreement between experiment and simulation results on OSNR evolution with cascaded SOAs is achieved. Besides, some simulation results on the cosimulation between SOA model and OptiSystem have been presented.

Chapter 4

Ultra dense silicon photonics interface

4.1 On-chip PROFA and PIC interface

Silicon-on-insulator (SOI) is one of the most important technologies that enable the large-scale photonic integrated circuits (PICs). The basic building blocks of PICs are nanophotonic waveguides. To achieve large-scale integration of optical functions, the interface with optical fiber becomes an important issue due to the mismatch in mode size between the optical fiber and nanophotonic waveguide. As mentioned in section 2.4, different solutions to the coupling problem have been proposed [25]. One approach is to make use of a spot size converter. A second approach is to change the spot size with an in-plane inverted lateral taper. However, the former is not CMOS compatible and the latter requires a huge topography, compromising further processing. Another approach is to use the diffractive gratings that can overcome the limitations above. An efficient, compact, alignment-tolerant and relatively broadband optical coupling can be achieved by such coupling structure.

A grating coupler is a periodic structure that can diffract light in a certain direction. The guided-mode resonance device couples light into a waveguide guided mode when Bragg condition is met. Fig. 4.1 presents the principle of the light coupling between waveguide and fiber through grating coupler [38]. The coupling efficiency and 3 dB bandwidth of the designed grating coupler by IMEC are 31% (-5 dB) and 60 nm, respectively.

The Pitch Reducing Optical Fiber Array (PROFA), produced by Chiral Photonics, is a high density, multi-channel optical input/output for fiber-to-chip and fiber-to-optical waveguide applications. As shown in Fig. 4.2, PROFA has a dramatically reduced channel spacing and scalable channel count. The total channel number is up to 61 and the typical pitch is $30 \sim 50$ μm. For each channel with 10 wavelengths operating at 25 Gb/s, the bandwidth density of 61 channels can be

$$10 \times 25 \text{ Gb/s} \times 61 \text{ / } (620\mu m/2)^2 \text{ / } \pi \approx 0.5 \text{ Tb/s}/mm^2$$

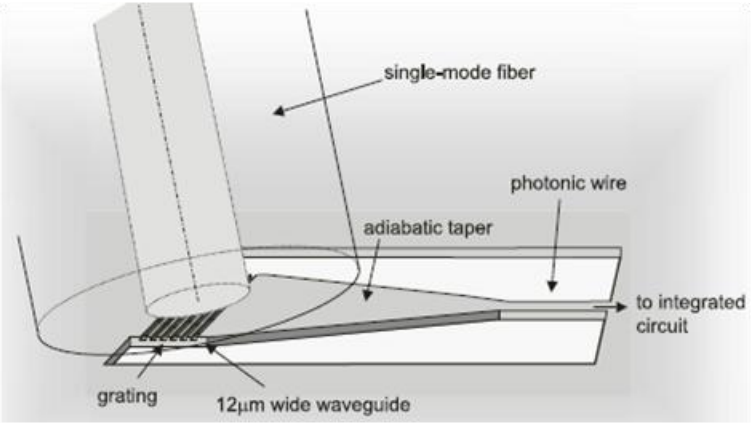


Fig. 4.1 Principle of grating coupler for light coupling between photonic waveguide and fiber [38].

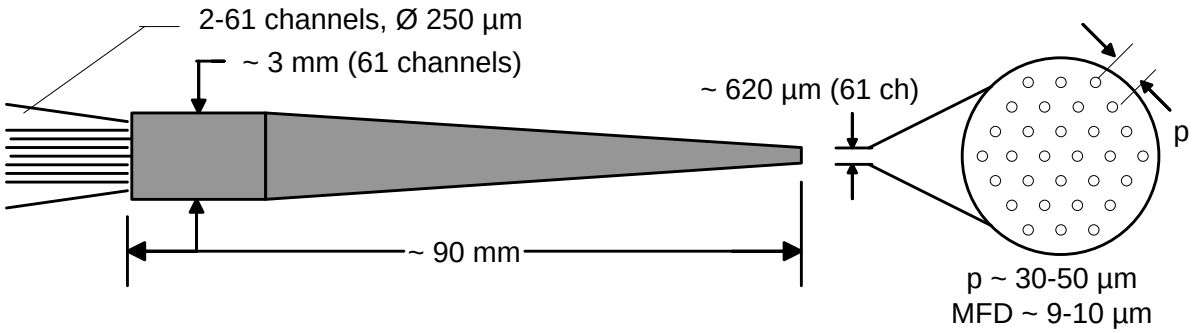


Fig. 4.2 Features of the high channel density PROFA (Chiral Photonics).

PROFA can dramatically increase the density of the optical I/O for photonic integrated circuits. To make use of the PROFA, an interface for the coupling of low loss and wide bandwidth between PROFA and PICs is necessary. The coupling interface between the PROFA and PICs based on vertical grating couplers with a loss of 3 dB and standard

deviation of coupling loss of 0.7 dB across 37 channels has been demonstrated in [39]. In parallel, a coupling interface based on the grating coupler array on SOI platform is proposed and designed. The proposed design of the coupling interface is shown in Fig. 4.3. There are mainly two components:

1) *Focusing grating coupler:* It is the basic element of the designed chip. Because of the reduced channel spacing of PROFA, ccompact focusing grating couplers are utilized to reduce the footprint and enable low loss (-5 dB) and broadband (60 nm 3-dB bandwidth) coupling without performance penalty.

2) *Waveguide:* At the output side of the gratings, all grating couplers are guided with the bent waveguides and aligned to the output facet.

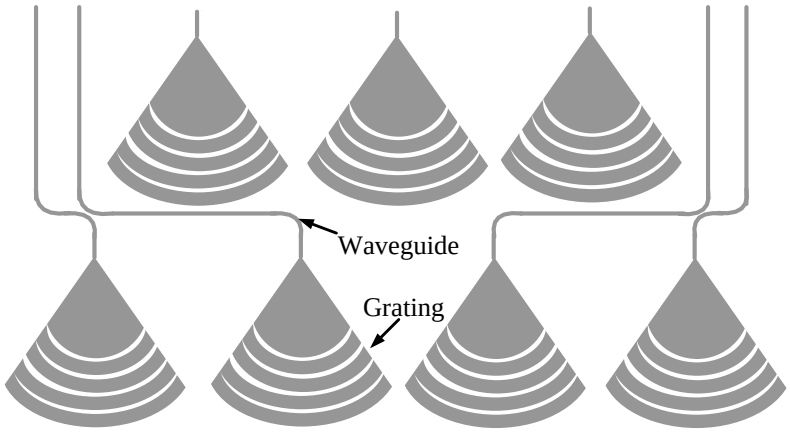


Fig. 4.3 Proposed design of coupling interface with grating coupler array.

4.2 Optical interface design and simulation

As the channel spacing of PROFA is around 40 μm, compact focusing grating coupler with small size should be utilized. Fig. 4.4 illustrates the schematic of the focusing grating coupler and structure parameters [40]. The Lumerical FDTD Solutions is used for the simulation of the designed grating coupler. Based on the theory of gratings, the modelling of the grating coupler is as follows:

1) The 2D FDTD is used to estimate the original structure parameters, namely a) incident angle, b) grating period, c) fill factor and d) etch depth at the desired wavelength (1550 nm) for the simplicity of simulation. These parameters are then optimized based on the coupling efficiency, 3-dB bandwidth and back-reflection.

2) As dimensions of the grating element have the most significant impact on device performance, the simulation of the optimal grating using 3D FDTD is investigated.

3) The space distribution of the grating coupler array will also be estimated since the crosstalk and alignment tolerance depend on the channel spacing.

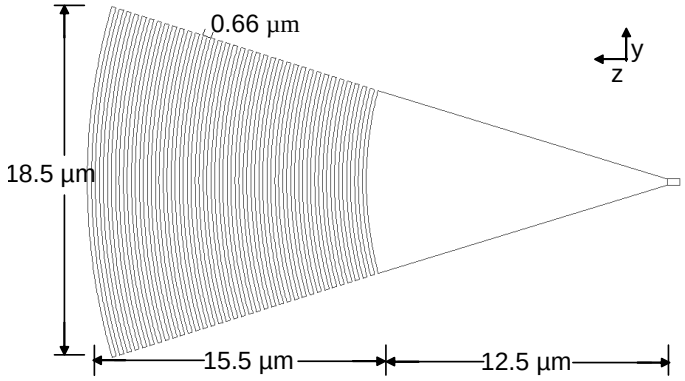


Fig. 4.4 Focusing grating coupler on SOI with a short taper [40].

4.2.1 Modelling and simulation

It is known that a grating coupler is used to diffract light in a certain direction. Some basic concepts are introduced according to [41]. Fig. 4.5 is the schematic of a detuned shallow etched grating coupler with useful parameters. P_{wg} is the input power, P_{up} and P_{down} are the power goes up and penetrates down. The effective index of the core, top and bottom layer of the waveguide are denoted by n_g, n_t, and n_b. Λ is the period of the grating. W is the width of the grating tooth. W/Λ equals to the duty cycle. The etch depth of grating is indicated as *ed*. The angle between surface normal and the propagation direction of diffracted light is θ.

I Design considerations

The limitation of fabrication process needs to be considered to design a grating coupler.

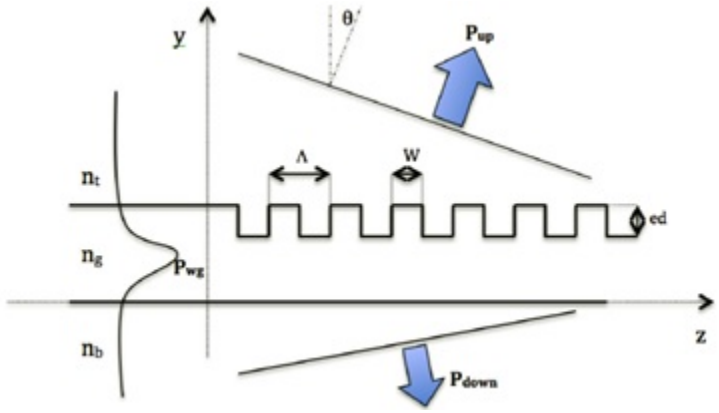


Fig. 4.5 Schematic of the detuned shallow etched grating coupler [41].

Some basic characteristics are illustrated below. The polarization of the input light is quasi-TE and the desired central wavelength is 1550 nm. The incident angle is 17 degree. For the fabrication process assuming that,

1) Two etches for the grating coupler: a shallow etch of 70 nm for grating fingers and a full etch for the strip waveguide.

2) Starting material is an SOI wafer with a 220-nm thick silicon and 2-μm thick SiO_2.

3) The grating is clad with air.

4) Minimum feature size is 120 nm and minimum pitch is 280 nm for IMEC standard.

II 2D FDTD simulation

To start 2D FDTD simulation, initial design is estimated based on the Bragg condition. Using the effective index method, the effective index of slabs for 220-nm thick is 2.875 and for 150-nm thick is 2.617. The initial duty cycle (fill factor) is 50%. Thus, the initial period of the grating is estimated to be 0.63 μm and the width of grating tooth is 0.32 μm according to Eq 4.1 to 4.4.

$$k_x = \beta - m \times 2\pi/\Lambda \tag{4.1}$$

$$sin(\Theta) = k_x/k_0 \tag{4.2}$$

$$k_0 = 2\pi/\lambda_0 \tag{4.3}$$

$$\beta = 2\pi \times n_{eff}/\lambda_0 \tag{4.4}$$

where λ_0=1550 nm, m=1, θ=17 deg.

With the parameters defined above, 2D FDTD simulation is carried out to assess the transmission of the grating coupler. A maximum coupling efficiency of 44% is achieved and the central frequency is around 1550 nm based on Bragg condition theory. There are several parameters that determine the performance of grating coupler including a) incident angle, b) period, c) duty cycle, d) etch depth, e) number of grating period and f) input light source position. Among them, the most important parameters are period, duty cycle and etch depth. To obtain the optimal performance of grating coupler for a specific parameter based on the initial design, the single variable optimization is adopted to optimize the incident angle, period, fill factor, and etch depth.

The optimization of these parameters with the maximum coupling efficiency of 47% and 3-dB bandwidth of 75 nm are indicated in Fig. 4.6 and the optimal design parameters from 2D simulation are listed in table 4.1. As shown in Fig. 4.6(a), the far field projection indicates around 20 degree emission at 1550 nm. Thus, the incident angle of the input light is set to be 20 degree. Fig. 4.6(b) indicates that the grating coupler has the largest transmission when the period is 0.66 μm. Similarly, Fig. 4.6(c) shows the largest transmission occurs when the grating tooth is 0.33 μm (ff = 0.5). While in Fig. 4.6(d), when the etch depth equals to 70 nm, the transmission of grating coupler has the best performance.

Table 4.1 Parameters of the optimized grating coupler

Incident angle (deg)	Period (μm)	Grating tooth (μm)	Etch depth (nm)
20	0.66	0.33	70

With the optimized parameters above, the transmission and back reflection of the grating coupler are calculated, as shown in Fig. 4.7. Comparing the transmission before and after optimization, it is clear that the coupling efficiency becomes much higher and the central wavelength shifts to 1550 nm. The back reflection in Fig. 4.7(b) indicates the reflection at 1550 nm is less than 2%, which is rather small. Note that the back reflection can be reduced using index matching fluid.

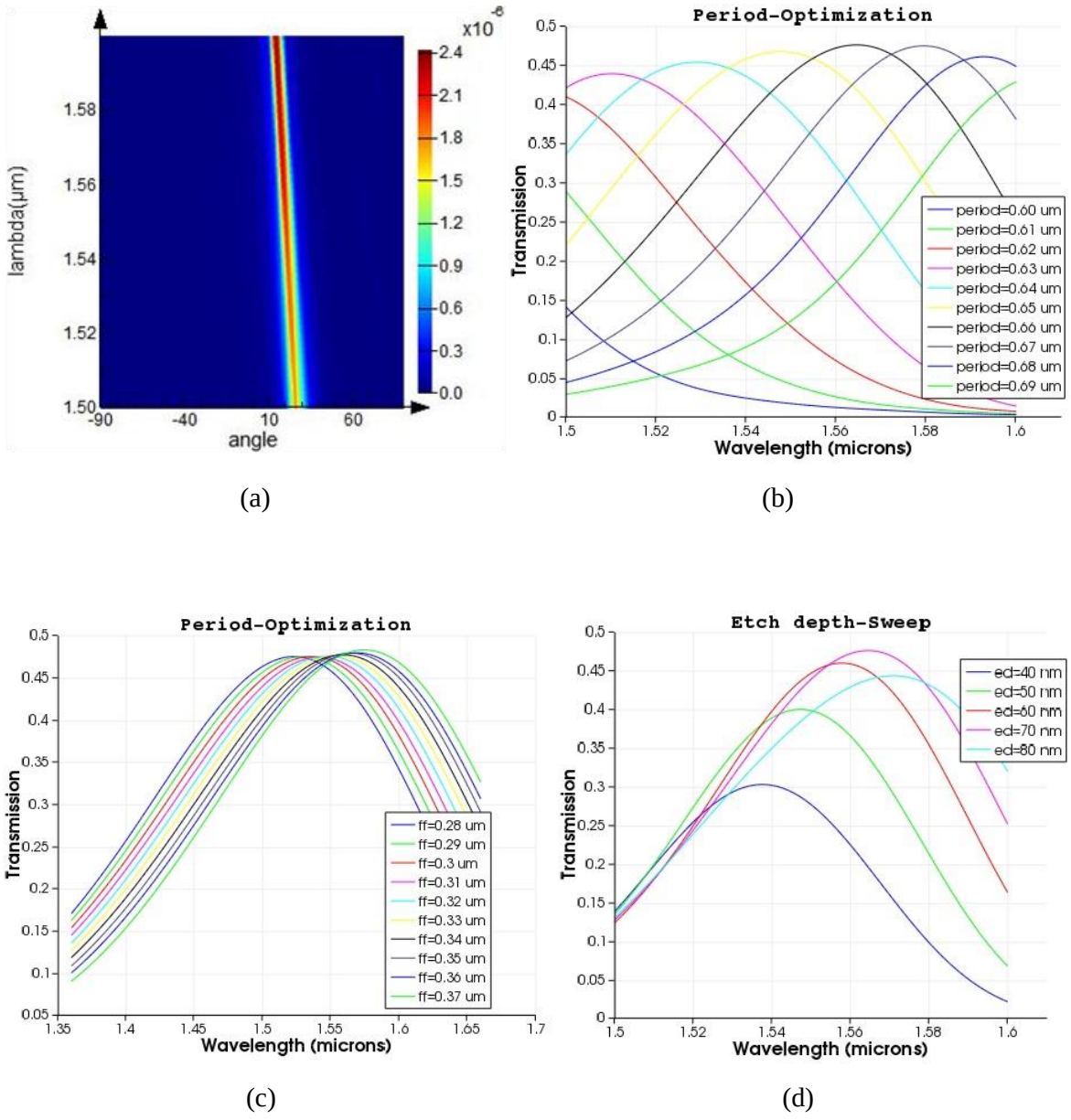
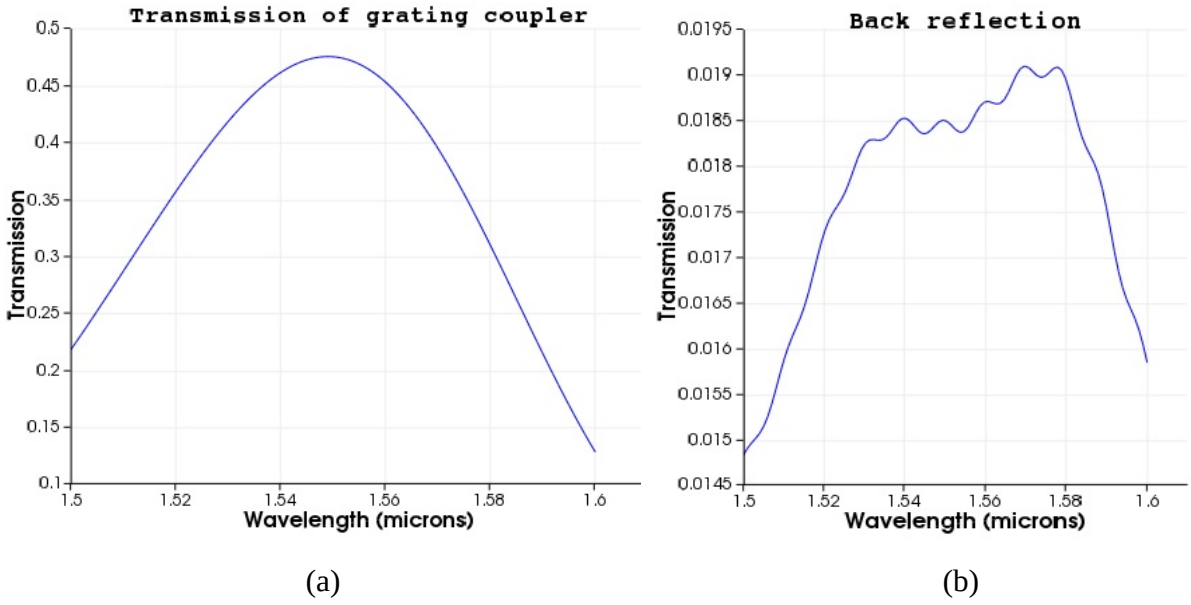


Fig. 4.6 2D Optimization results of (a) incident angle, (b) period, (c) fill factor, and (d) etch depth.



(a) (b)

Fig. 4.7 (a) Transmission and (b) back reflection of the optimized gating.

III 3D FDTD simulation

Although 2D simulation provides fast simulation time when not considering the structure width, it leads to lower accuracy in the simulation results. 3D FDTD simulation is performed to verify the obtained results. Based on the initial optimization from 2D FDTD, 3D FDTD simulation is performed to verify the obtained results. Because the grating couplers with straight-line gratings require a long taper (around 300 μm) to convert the fiber mode to the waveguide mode, it could not be applied for PROFA interface with the reduced channel spacing. Therefore, compact focusing grating couplers are utilized, which can shrink the footprint and enable broadband coupling without performance penalty [41]. As shown in [42], the focusing grating can be obtained by curving the grating line in Eq 4.5:

$$q\lambda_0 = n_{eff}\sqrt{x^2 + y^2} - z \times n_t \times cos(\theta_c) \tag{4.5}$$

where q is an integer number of each grating line, θ_c is the angle between the fiber and chip surface, n_t is the reflective index of the environment, λ_0 is the vacuum wavelength, and n_{eff} is the effective index of the grating. The grating lines are ellipses with common focal point that is also the optical focal point of the coupler. The focal distance can be obtained through the minimal line number.

Regarding to the 3D FDTD simulation of the focusing grating coupler, the initial design on SOI is determined according to the 2D optimization and IMEC standard passives with a 0.66-μm period, 50%-duty cycle, 70-nm etch depth, 2-μm SiO_2 glass and silicon substrate. Moreover, referred to the example of 3D focusing grating coupler from Lumerical, the initial length, width of the grating and taper length are determined. The total length equals to the sum of the grating length and taper length. The initial structure parameters of 3D focusing grating coupler are given in table 4.2. The schematic of the focusing grating coupler with initial structure parameters is shown in Fig. 4.8(a). Fig. 4.8(b) shows the transmissions of the 2D optimization and initial 3D design. Their profiles are similar to each other but the coupling efficiency of 3D simulation is much lower. Also, there is a small redshift of the central wavelength.

Table 4.2 Initial structure parameters of focusing gratings

Period (μm)	Duty cycle	Etch depth (nm)	Width (μm)	Length (μm)	Taper length (μm)
0.66	50%	70	30	25	25

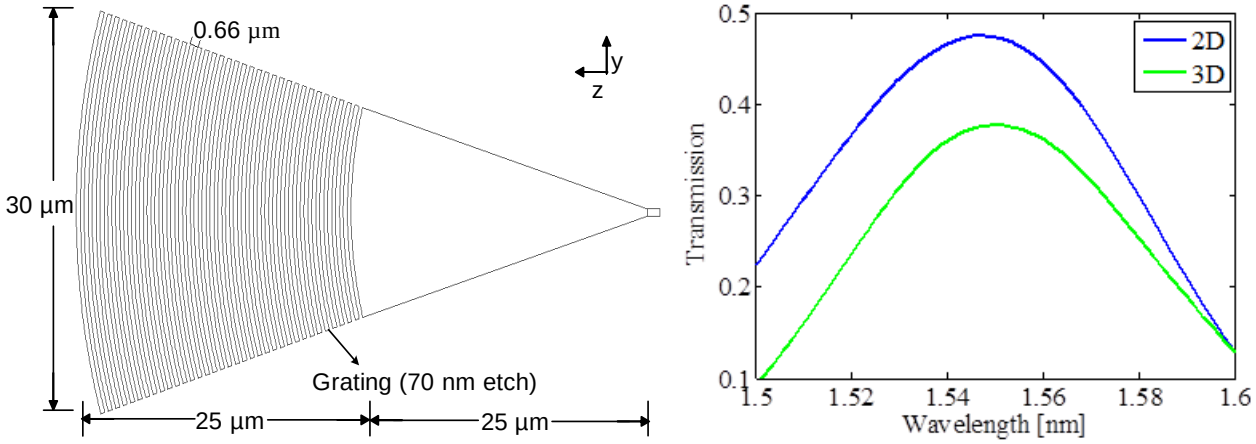


Fig. 4.8 (a) Initial structure parameters and (b) transmission of the grating.

Optimizations of the grating structure parameters with 3D simulation are implemented in order to verify the optimum structure parameters obtained from 2D simulation. The

results are shown in Fig. 4.9. In Fig. 4.9(a), the best performance occurs when the period equals to 0.66 μm at 1550 nm. Fig. 4.9(b) shows that the transmissions with different duty cycle change slightly except for a small shift of the central wavelength. Consequently, the duty cycle keeps 50%. Considering the IMEC standard passives, the etch depth maintains the standard of 70 nm, which ensures the functionality of the fabricated device.

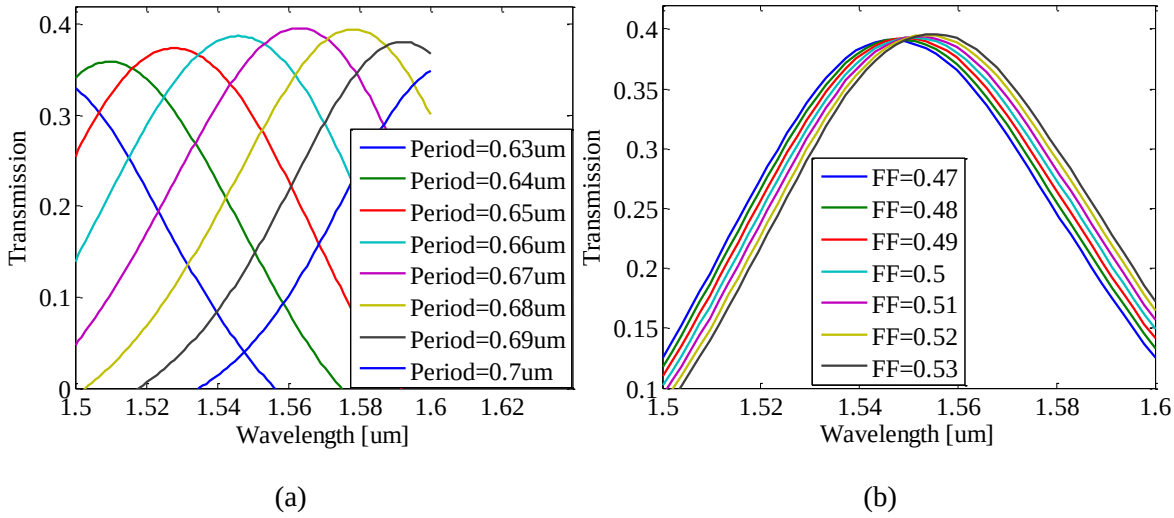


Fig. 4.9 Transmission of focusing grating coupler with (a) period and (b) duty cycle.

As the dimensions of the grating element have key impact on the chip performance, the width, length and taper length of 3D focusing grating coupler element are further investigated. It is reported that the coupling efficiency of gratings can reach 30% with an 18.5-μm width, 15.5-μm length and 12.5-μm taper length, which can almost satisfy the strict requirement of ultra small footprint [42]. Hence, the optimization of grating dimensions is implemented based on the above-mentioned structure parameters. Besides, a 1-μm straight waveguide is inserted at the output of gratings.

The optimization results of dimension are presented in Fig. 4.10. In Fig. 4.10(a), when the width is larger than 16 μm, the variance of transmission among different width becomes relatively small. While the coupling efficiency decreases with the grating width below 16 μm. Because the strict requirement of chip test can be relaxed with larger gratings, gratings with width greater than 16 μm will be fabricated. While in Fig. 4.10(b), as long as the

length of grating is larger than 10 μm, the transmission stays unchanged. The reason is that the input fiber source can be perfectly located in the grating coupler without any deviation in simulation. Gratings with length ranging from 10 μm to 20 μm are selected. The transmission performance improves when the taper length increases from 9 μm to 14 μm in Fig. 4.10(c). However, if the taper length is too long, the grating element becomes too large to meet the requirements of PROFA interface. Due to this trade-off, gratings with taper length from 10 μm to 15 μm will be tested.

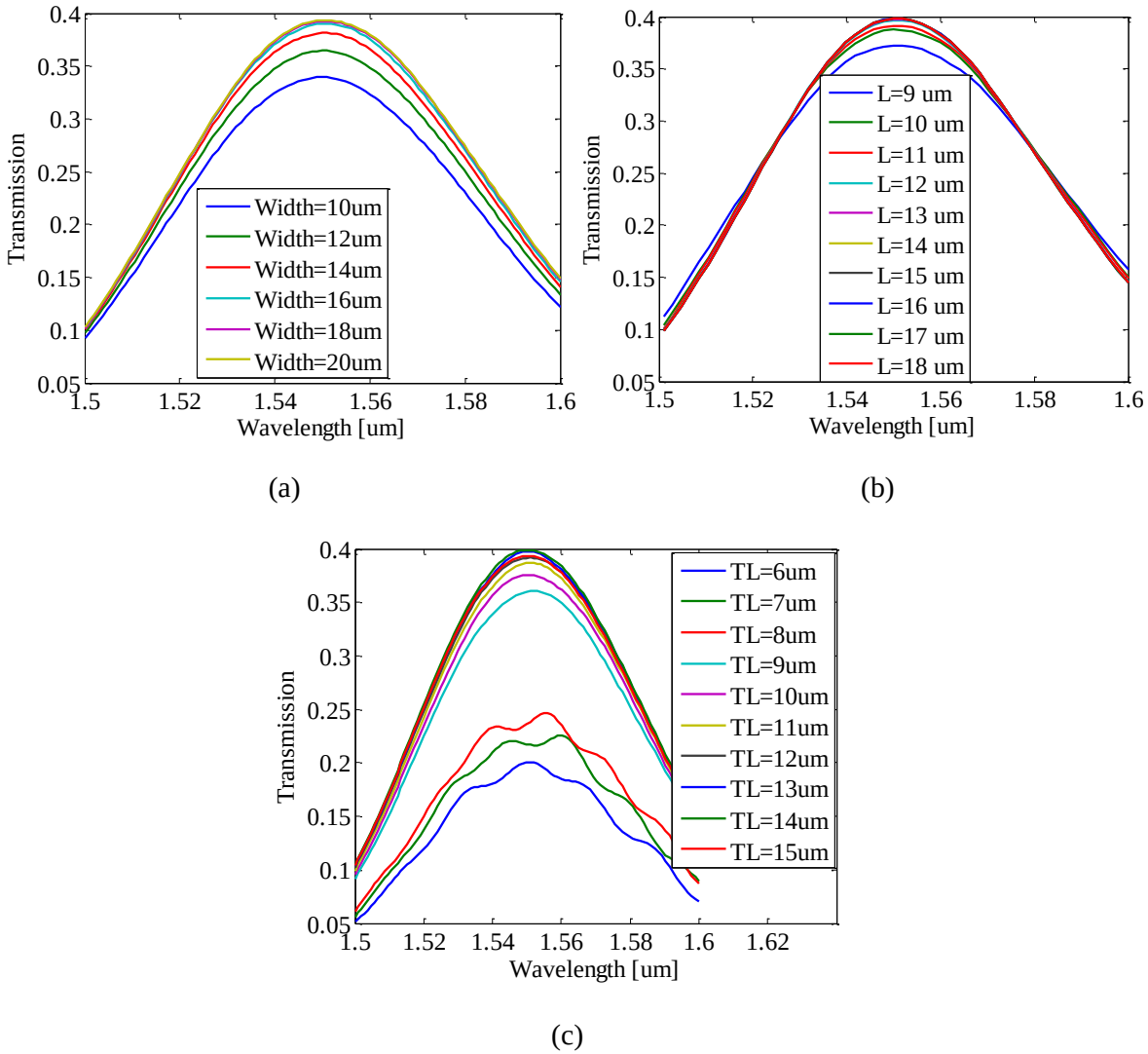


Fig. 4.10 Transmission of grating coupler with different (a) width, (b) length, (c) taper length.

In summary, structure parameters of designed 3D focusing grating couplers based on the optimization are listed in table 4.3. Fig. 4.11(a) shows one 3D grating coupler with the optimum structure parameters and Fig. 4.11(b) and Fig. 4.12(a) are the transmissions in linear and log scale, respectively. The back reflection is shown in Fig. 4.12(b). In Fig. 4.11(b), the coupling efficiency at 1550 nm is 40%, which is 7% lower compared to 2D simulation. The reason is that 3D simulation is more accurate but it takes more time. In addition, as shown in Fig. 4.12(a), the 3-dB bandwidth of the designed grating coupler is around 70 nm. The back reflection in Fig. 4.12(b) indicates the reflection at 1550 nm is around 2.74%, which is similar to that of 2D simulation. Also, the performance of grating couplers can be enhanced by adding the index matching fluid (n_{eff}=1.46) at the interface of air gap and gratings. The transmission and back reflection with index matching fluid are shown in Fig. 4.12(c) and 4.12(d), where the maximum transmission increases to 43.6%.

Table 4.3 Optimized structure parameters of gratings

Period (μm)	Duty cycle	Etch depth (nm)	Width (μm)	Length (μm)	Taper length (μm)
0.66	50%	70	16∼20	10∼20	10∼15

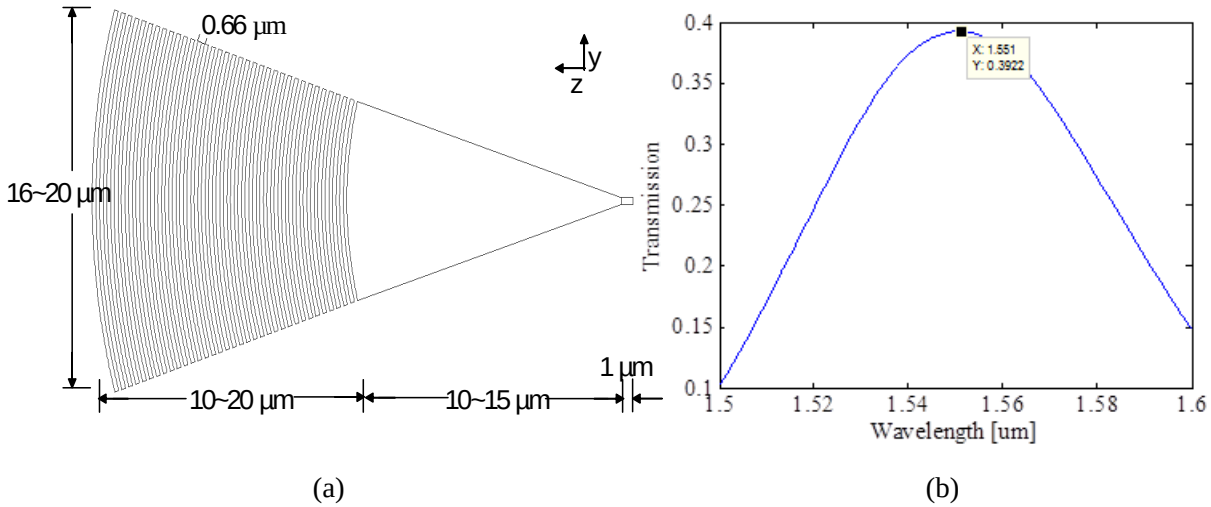


Fig. 4.11 (a) The structure parameters of designed 3D focusing grating and (b) the corresponding transmission in linear scale

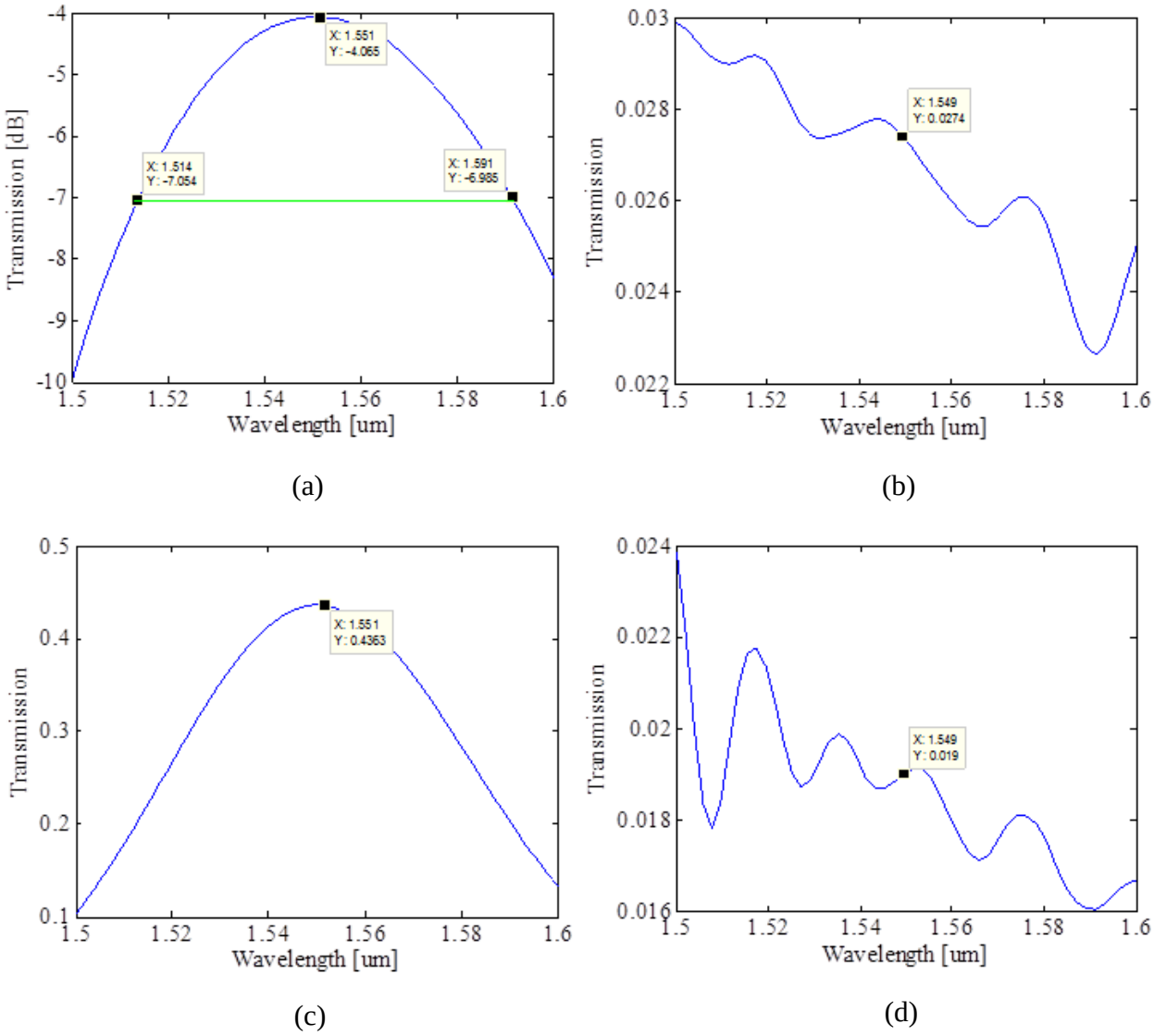


Fig. 4.12 (a) The transmission in log scale, (b) back reflection, (c) transmission and (d) back reflection with index matching fluid.

Except for the structure parameters and dimensions of grating elements, the position of the input fiber source also impacts the chip performance. Therefore, alignment tolerance is also investigated in simulation through sweeping the X and Y positions of the mode source. The focal point of gratings is set to be the origin. The results are shown in Fig. 4.13. As indicated in Fig. 4.13(a), there is an optimal light source position which gives the highest coupling efficiency. The optimal X position is approximately 14 μm for 10-μm taper length. While in the Y direction as shown in Fig. 4.13(b), the transmission dramatically decreases as the light source deviates from the center of the grating. Hence the alignment tolerance will be reduced as the grating shrinks to certain size and the acceptable alignment deviation becomes stricter in terms of the grating coupler array.

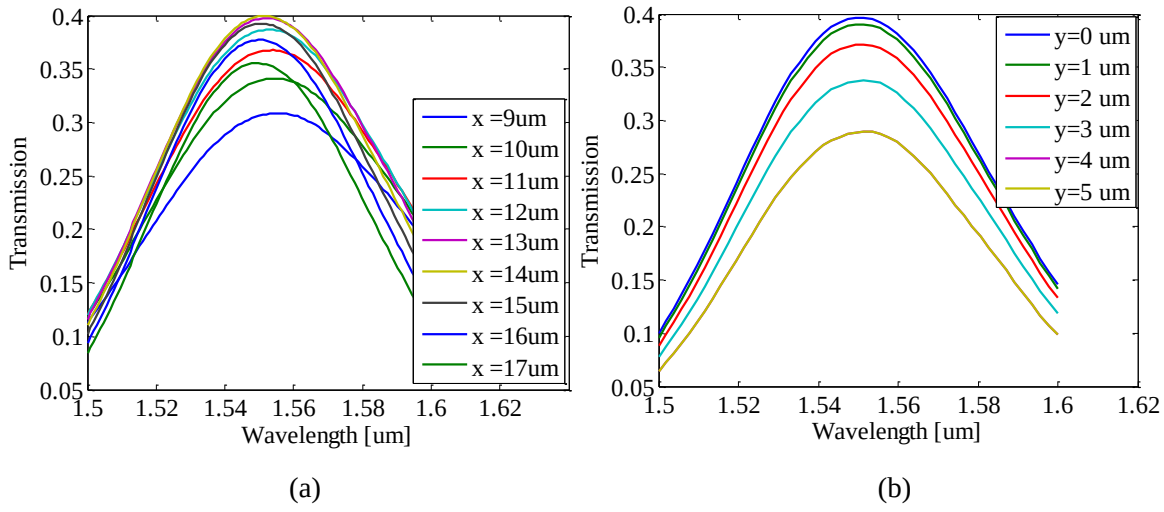


Fig. 4.13 Transmissions with different (a) X and (b) Y axis for input source.

4.2.2 Grating coupler array and PROFA interface

The coupling interface between silicon photonic integrated circuits and the 61-channel Pitch Reducing Optical Fiber Array (PROFA) can be achieved based on the optimized focusing grating element. As each channel requires a unique grating, 61 focusing grating couplers are horizontally distributed in plane to match the exact features of the specific PROFA. When designing the structure of the interface, the measurement of nanophotonic devices should also be taken into account. Since the pitch of the PROFA can be set from 30 μm to 50 μm according to Chiral Photonics and the commercial fiber array with a 127/250-μm

pitch is available in the lab, a 42.33-μm wide PROFA pitch (channel spacing) is selected so that every three input/output gratings will have a pitch of 127 μm and testing with the fiber array can be done prior to testing the interface with the PROFA.

To connect the focusing grating elements with on-chip devices, all gratings are guided with the bent waveguides and aligned to the output facet. To ensure chip performance as well as exploit the high density of the PROFA, waveguides with 5-μm bent radius are utilized spaced by 1 μm, 2 μm or 2.5 μm depending on the designed structures. In addition, as the incident angle affects the performance of the grating coupler array, the PROFA should be polished at a specific angle. In order to have a 20 degree incident angle with air cladding, the polished angle should be approximately 13 degree. This is based on Snell's law, as shown in Fig. 4.14. The output facet of PROFA being a two-dimensional structure, there is a stretching effect of the pitch along the z-axis. As illustrated in Fig. 4.15, the Y-axis is vertical to the polishing direction and the pitch stretching should be taken into account after polishing. Therefore, the height (NHeight) between two neighboring cores aligned in the z-direction of the PROFA interface after polishing is calculated by Eq (4.6).

$$NHeight = Height/cos(\theta) \tag{4.6}$$

where θ is the polishing angle and the original height can be calculated by Eq (4.7).

$$Height = \sqrt{3} \times Pitch \tag{4.7}$$

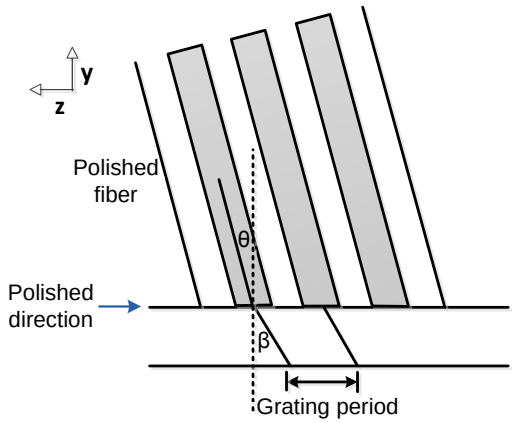


Fig. 4.14 Schematic of polished fiber

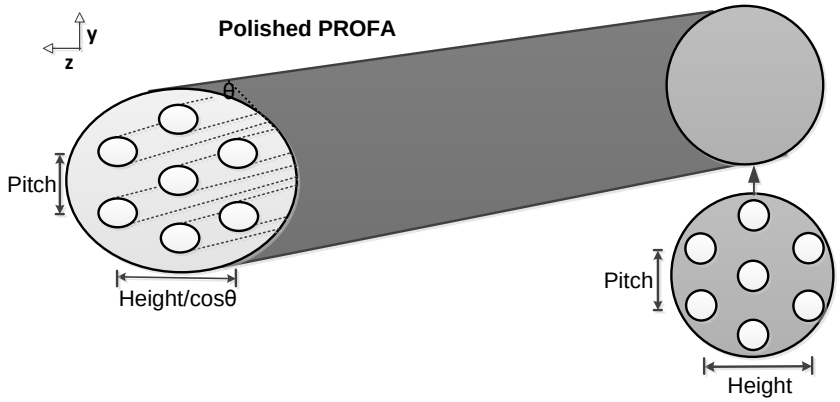
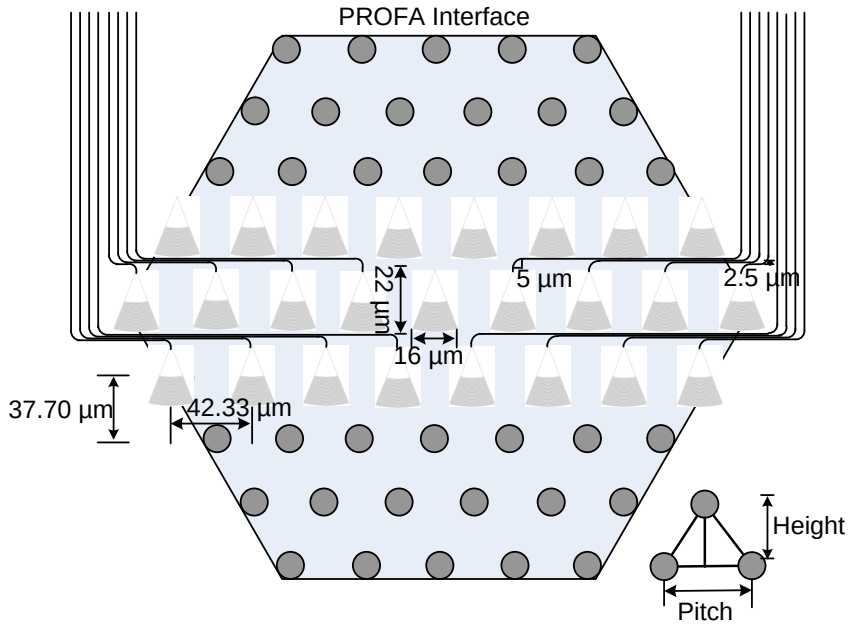
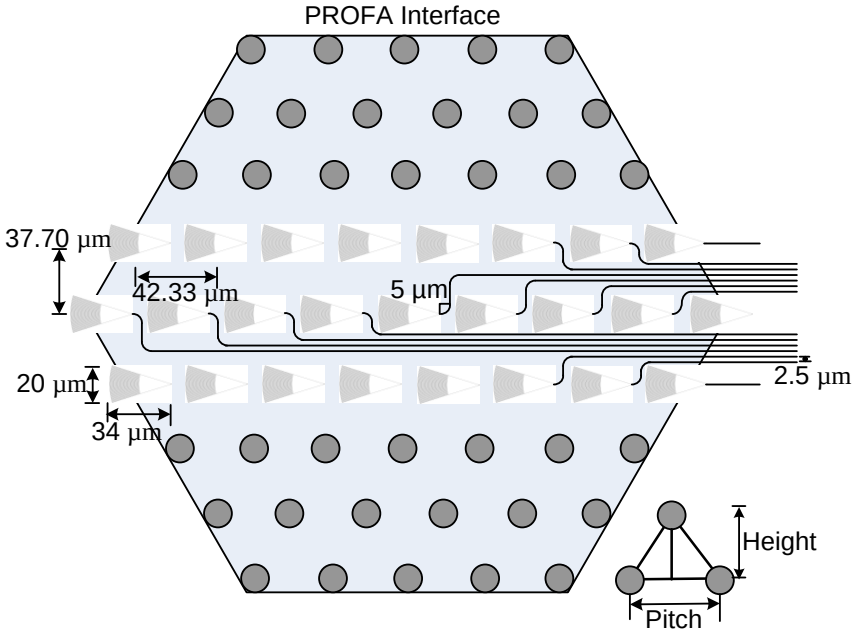


Fig. 4.15 The effect of pitch stretching after polishing for PROFA.

Considering the features of the PROFA, there are mainly two possible interface configurations with different dimensions of grating coupler elements. The schematic of the two coupling interfaces with the pitch are shown in Fig. 4.16. For the structure shown in Fig. 4.16(a), all gratings are aligned vertically to one of the six edges (*e.g.,* top edge). As mentioned earlier, one advantage of this configuration is that every three gratings can initially be tested with a fiber array with a pitch of 127 μm. However, the distance between two adjacent columns after polishing is 37.70 μm which is shorter than the 42.33-μm pitch. Thus, taking the bent radius and the space between adjacent guiding waveguides into account the grating couplers are limited to a length of approximately 20 μm in order to make use of as many channels as possible. Such a small length of grating coupler will be rather challenging to achieve high coupling efficiency and large alignment tolerance in experiment. While for the second structure shown in Fig. 4.16(b), the direction of all gratings is along the diagonal of the hexagonal PROFA interface. The advantage of diagonal alignment is that the grating length can be as large as 35 μm compared to 20 μm for the design in Fig. 4.16(a) relaxing the design and test requirements of compact gratings for PROFA interface. However, the second structure cannot be tested with a fiber array with a pitch of 127 μm and must be directly attached to a PROFA.



(a)



(b)

Fig. 4.16 Schematic of part of the coupling interface (a) vertical alignment (b) diagonal alignment.

4.2.3 Device layout

As shown in Fig. 4.17, the total area of one PROFA interface (box labelled 5) based on grating coupler array is 0.6 mm×0.5 mm. Along with the PROFA interface, different functional modules are added to test the chip for each variation as shown in Fig. 4.17. The main purpose of adding different functional blocks is to test the PROFA interface and the functional blocks (*e.g.*, delay line, ring resonators) are common devices from the PDK or general design. There are 10 variations in total for the whole chip with different dimensions of grating couplers for the PROFA interface. Below are the functional modules added with their corresponding box labelled numbers:

1) *Delay line (DL):* Different lengths of waveguides are added to measure the insertion loss of the waveguide (*e.g.,* 1 cm to 5 cm). Such long waveguides are realized through circulating waveguides.

2) *Bend waveguide (Bend WG):* Since there will be extra loss induced by small bend waveguides, a range of small and 10-μm bend waveguides with the same length are added. The latter is used as a reference for the case without bending loss.

3) *Ring resonator (RR):* Ring resonators are used to test the input/output of different channels. Four different ring resonators are designed and the corresponding structure parameters are illustrated in table 4.4. The number in the first column corresponds to the number of variation where the ring resonator (RR) is placed. The structure parameters of RR3 and RR4 are the same, so are RR5 and RR6.

4) *Multiplexer/Demultiplexer:* Mux/Demux based on the ring resonators mentioned above is designed to increase the total capacity. There are three or five inputs/outputs for each Mux/Demux.

5) *PROFA interface:* I/Os. The grating couplers in one PROFA interface are the same, denoted as GCVi where i denotes the variation of PROFA interface ($i = 1$ to 6) (*e.g.,* GCV1 means the grating couplers placed in the PROFA interface of variation 1).

6) *Grating coupler arrays:* Different structure parameters and dimensions of grating couplers including grating couplers in the PROFA interface are listed in table 4.5. The *Standard* grating coupler is the design from IMEC process development kit (PDK).

There are two types of testing grating couplers for each variation: 1) GCViL, and 2) GCViR (*e.g.,* GCV1L means the grating coupler at the left side (L) of the PROFA interface for variation $i = 1$).

Note: although the PROFA interface configuration is vertically aligned (Fig. 4.16(a)), the fiber array cannot be used to characterize the Mux/Demux as well as ring resonators. These structures require the PROFA.

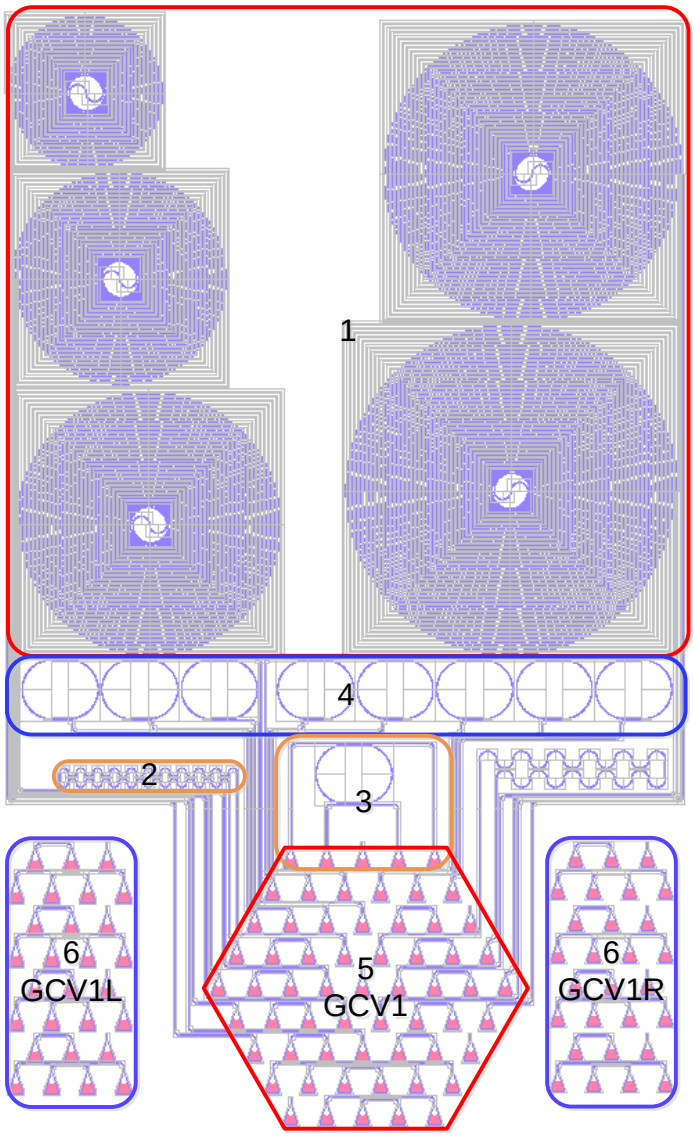


Fig. 4.17 Designed layout of one of the 10 variations (Variation $i = 1$).

Table 4.4 The structure parameters of designed ring resonators

Ring resonator (RR)	Radius (μm)	Coupling length (μm)	Gap (μm)	FSR (nm)	BW (nm)
1	34.85	20	0.22	2.81	0.4
2	39.63	5	0.22	2.0	0.8
3	25.89	5	0.22	3.0	0.6
4	34.85	5	0.22	3.0	0.6
5	14.29	20	0.22	5.6	0.7
6	14.29	20	0.22	5.6	0.7

Table 4.5 Gratings with different structure parameters and dimensions

Dimensions Grating(GC)	Width (μm)	Length (μm)	Taper length (μm)	Total length (μm)	Incident angle (deg)	Layout position
1	15.0	9.9	10.1	20.0	20	V4R/V5L
2	15.2	10.56	10.44	21.0	20	V1R/V5
3	16.0	10.56	11.44	22.0	20	V2R
4	16.0	11.88	10.12	22.0	20	V1
5	18.0	11.22	10.78	22.0	20	V6R
6	20.0	11.88	10.12	22.0	13	V3R/V6L/V6
7	18.0	10.56	12.44	23.0	20	V2
8	20.0	11.88	11.12	23.0	20	V3/V4
9	20.0	13.2	10.8	24.0	20	V1L
10	20.0	13.2	11.8	25.0	20	V3L
11	16.0	15.18	11.82	27.0	20	V4L
12	16.0	15.84	13.16	29.0	20	V7
13	18.0	19.8	13.2	33.0	20	V8
14	20.0	19.8	14.2	34.0	20	V9
15	20.0	20.46	13.54	34.0	20	V10
Standard	27.0	21.78	20.22	42.0	20	V2L/V5R

The grating coupler pairs with 127-μm spacing characterized with a fiber array for each variation of PROFA interface are shown in Fig. 4.18. There are 10 labelled grating pairs in the PROFA interface plus testing grating arrays on both sides of PROFA interface (labelled 6 in Fig. 4.17). Testing devices between each grating coupler pairs are listed in table 4.6. Note that the number in the first column means grating pairs labelled j in Fig. 4.18.

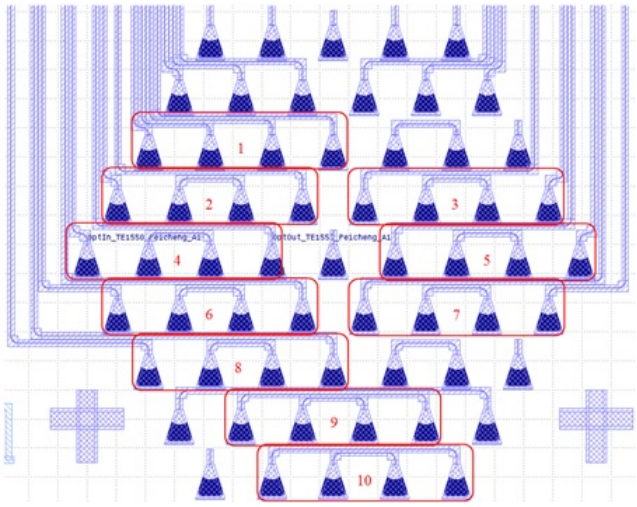


Fig. 4.18 Grating coupler pairs for one variation with 127-μm spacing.

Table 4.6 Testing devices between each grating coupler pairs

Grating pair	Testing devices
9/10	Waveguide
1	Ring resonator
2	5-μm bend WGs
3	10-μm bend WGs
4	3-cm delay line (DL)
5	5-cm delay line (DL)
6	2-cm delay line (DL)
7	4-cm delay line (DL)
8	1-cm delay line (DL)

The 61 channels of PROFA interface labelled from 1 to 61 as inputs/outputs to be tested with the corresponding PROFA for each variation are shown in Fig. 4.19. The functionality of 61 channels as I/Os is shown in table 4.7.

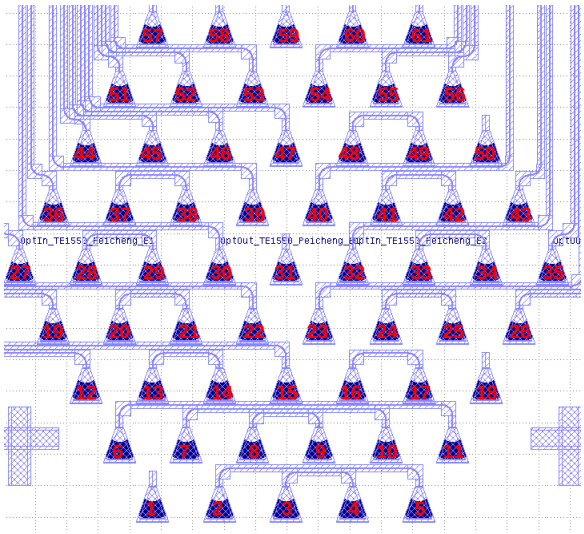


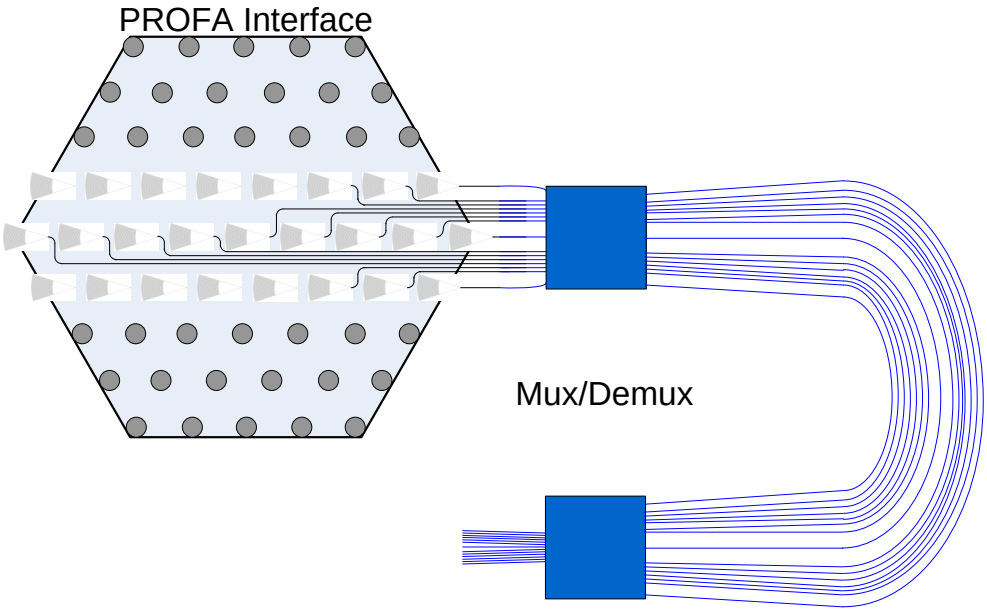
Fig. 4.19 Labelled 61 channels as inputs/outputs tested with the PROFA

Table 4.7 The functionality of 61 channels as Input/Outputs (I/Os)

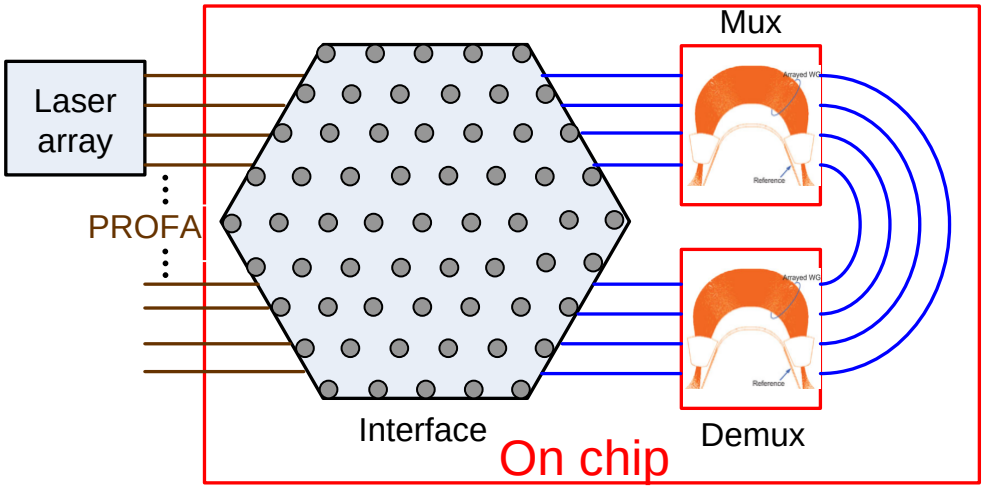
Channel Number	I/O functionality
1, 18, 31, 50, 59	No connection
(2, 5), (3,4), (6, 11), (7,10), (8,9), (13,14), (16,17), (20,21), (24,25), (28,29)(33,34), (37,38), (41,42)	I/Os with direct connection (GC pairs)
(12,15)	I/Os for 1-cm DL
(19,22)	I/Os for 2-cm DL
(23,26)	I/Os for 4-cm DL
(27,30)	I/Os for 3-cm DL
(32,35)	I/Os for 5-cm DL
(36,39)	I/Os for 5-μm BG
(40,43)	I/Os for 10-μm BG
(44,45,46,47)	I/Os for 3 cascaded RR based Mux/Demux, (Input: 44, 45, 46, Output: 47 or vice verse)
(51,52,53,54,55,56)	I/Os for 5 cascaded RR based Mux/Demux, (Input: 52,53,54,55,56, Output: 51 or vice verse)
(57,58,60,61)	I/Os for 1 RR (e.g., Input: 57, through: port 61 and drop port: 60)

4.3 High bandwidth Tb/s optical link

With the designed PROFA interface based on the grating coupler array, 61 input/output channels can be uniquely connected to the chip/PICs. It is reported that using a 10-channel SiN arrayed-waveguide grating (AWG) with 100-GHz spacing, 250 Gb/s aggregated capacity on a 5×8 mm^2 has been achieved [43]. With the designed PROFA interface, Tb/s optical link can be achieved based on silicon photonics. The PROFA interface can be integrated with proper Multiplexer/Demultiplexer to achieve even higher capacity in a much smaller footprint, as shown in Fig. 4.20(a). Assuming each channel operating at 20 or 50 Gb/s, the PROFA is capable to reach 1 Tb/s using 50 or 20 channels. Fig. 4.20(b) presents the potential high capacity on-chip system with the designed device as the input/output coupling interface.



(a)



(b)

Fig. 4.20 (a) Integration of PROFA interface and Mux/Demux, and (b) high capacity on-chip system with PROFA interface.

4.4 Experimental results and analysis

4.4.1 Testing results with fiber array

The fiber array with 127-μm spacing is used to test the PROFA interface of vertical alignment. The parameters can be measured including:

1) Incident angle. It can be estimated based on the shift of the central wavelength.

2) Insertion loss of grating coupler.

3) Bandwidth of grating coupler.

4) Insertion loss of waveguide and bend waveguide.

The equipment required for chip test are

1) Thorlabs and manual stage.

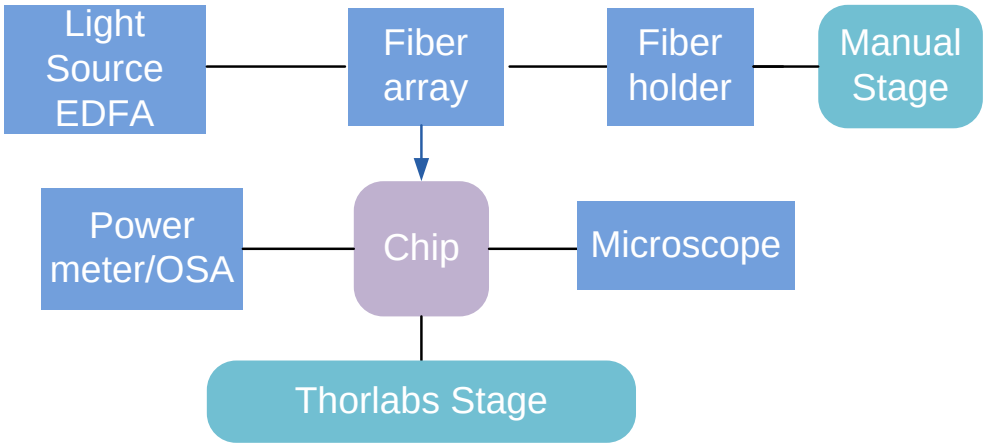
2) Light source(EDFA).

3) Fiber array.

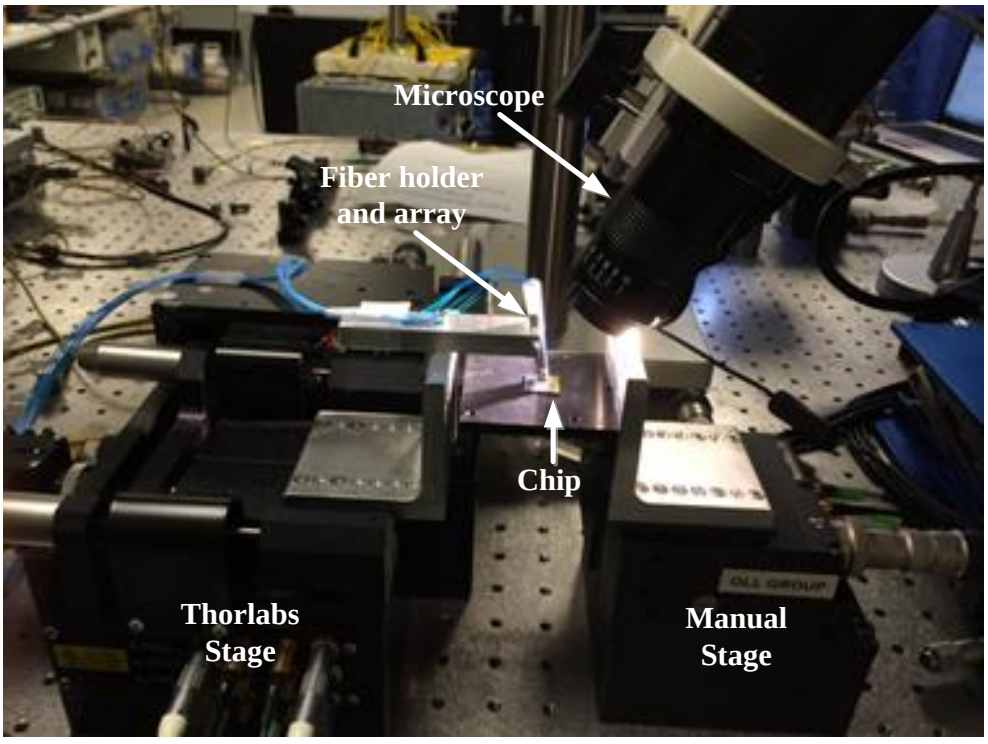
4) Microscope.

5) OSA/Optical power meter.

The schematic of the chip measurement and experimental setup are illustrated in Fig. 4.21(a) and 4.21(b). The picture of the chip under test captured through the microscope is shown in Fig. 4.22.



(a)



(b)

Fig. 4.21 (a) Schematic of chip measurement, and (b) experimental setup.

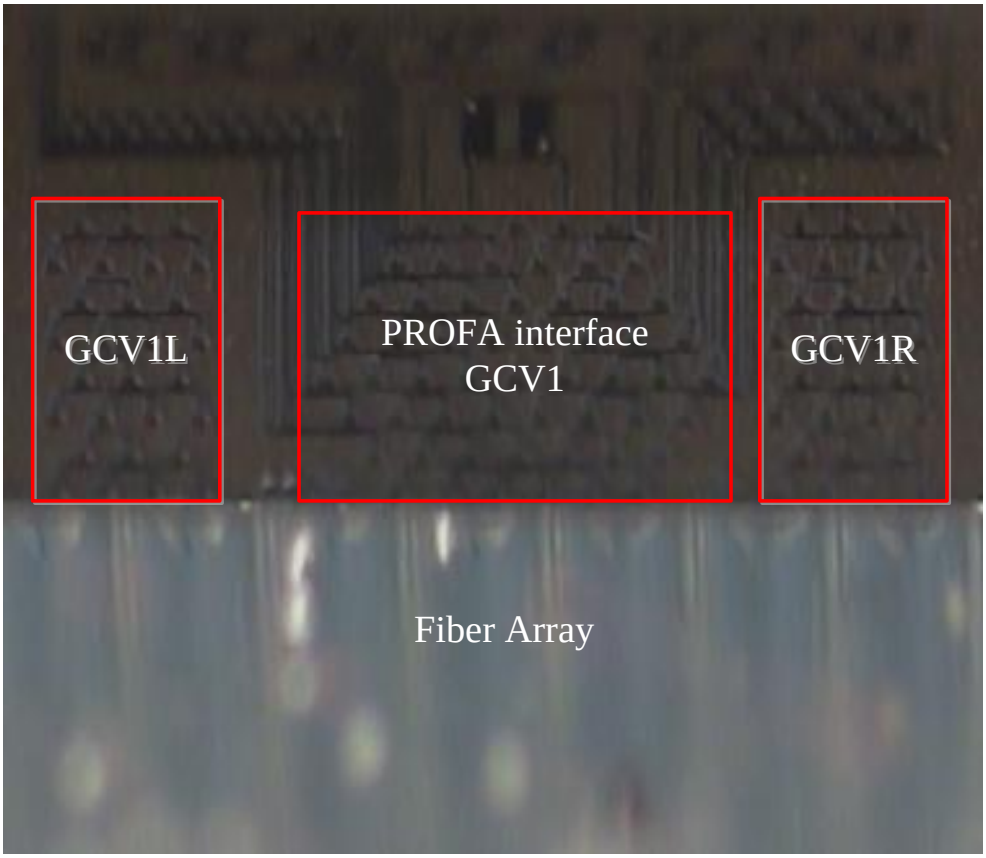


Fig. 4.22 Photo of chip under test. GCV1L(R) means the grating pair on the left (right) side for variation 1.

The grating couplers with different structure parameters and dimensions are tested using the fiber array. The minimum insertion loss (IL), 3-dB bandwidth (BW) and central wavelength from fiber to fiber are presented in table 4.8. In addition, the transmissions for part of the testing grating couplers are shown in Fig. 4.23. GC 12 to GC 15 can only be tested with the PROFA attached to the chip. As can be seen from table 4.8, the minimum insertion loss from fiber to fiber for the standard grating couplers is 11.3 dB. While the minimum insertion loss of the designed grating couplers is 12.5 dB (6.25 dB per grating coupler), which is 1.2 dB higher than that of the standard grating coupler. The difference between the maximum and minimum insertion loss of the designed grating couplers is 1.4 dB. With index matching fluid, the performance of grating couplers should be improved based on the simulation.

Table 4.8 Measurement results of testing grating couplers (fiber-to-fiber)

Dimensions Grating(GC)	Width (μm)	Length (μm)	Taper length (μm)	Total length (μm)	Min IL/BW @WL (dB/nm/nm)
1	15.0	9.9	10.1	20.0	12.7 / 50.0 / 1548
2	15.2	10.56	10.44	21.0	13.0 / 49.0 / 1550
3	16.0	10.56	11.44	22.0	13.0 / 49.0 / 1550
4	16.0	11.88	10.12	22.0	12.6 / 50.0 / 1556
5	18.0	11.22	10.78	22.0	13.0 / 49.0 / 1550
6	20.0	11.88	10.12	22.0	12.8 / 57.0 / 1520
7	18.0	10.56	12.44	23.0	12.7 / 50.0 / 1548
8	20.0	11.88	11.12	23.0	12.7 / 50.0 / 1550
9	20.0	13.2	10.8	24.0	12.5 / 50.0 / 1551
10	20.0	13.2	11.8	25.0	13.9 / 53.0 / 1550
11	16.0	15.18	11.82	27.0	12.7 / 50.0 / 1550
12	16.0	15.84	13.16	29.0	-
13	18.0	19.8	13.2	33.0	-
14	20.0	19.8	14.2	34.0	-
15	20.0	20.46	13.54	34.0	-
Standard	27.0	21.78	20.22	42.0	11.3 / 48.0 / 1562

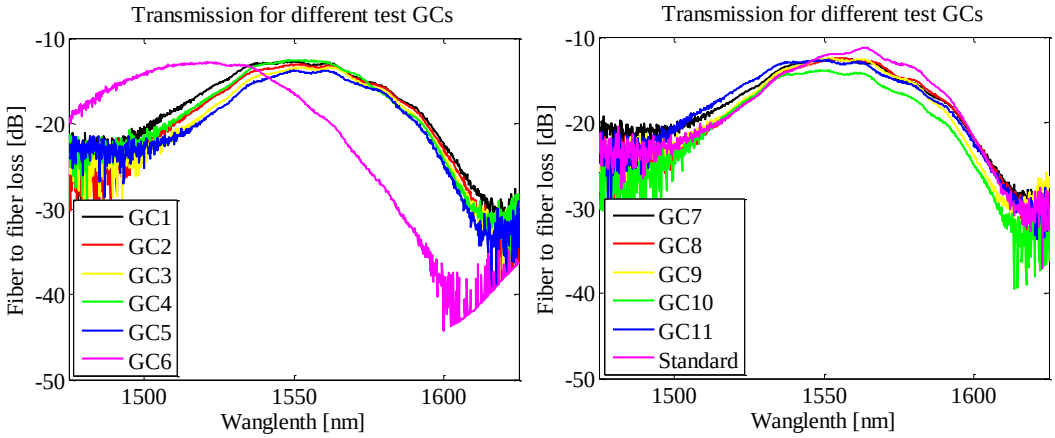


Fig. 4.23 Transmission of testing GCs (GC1 to 11 and the standard design).

The characterization results of the grating coupler pairs for six PROFA interfaces with the design of vertical alignment using fiber array are presented in table 4.9, including the insertion loss, 3-dB bandwidth (BW) and central wavelength. The transmissions of grating pairs (j = 2-9) for variation 1 and the corresponding zoom-in transmission are shown in Fig. 4.24(a) and 4.24(b). Fig. 4.24(c) shows the transmission of grating pairs (j = 10) for variation i = 1 to 6. In addition, the output spectrum, as well as the zoom-in spectrum, of designed ring resonators is shown in Fig. 4.25 (note: the fluctuation on both sides is due to the limitation of OSA sensitivity). The insertion losses of corresponding devices calculated from test results are presented in table 4.10.

Table 4.9 Characterization result of gratings for six PROFA interfaces

GC pair	1	2	3	4	5	6	7	8	9/10		
Variation	IL (dB)	IL (dB)	IL (dB)	IL (dB)	IL (dB)	IL (dB)	IL (dB)	IL (dB)	IL (dB)	BW (nm)	Central WL (nm)
1	∞	13.5	15.0	34.8	∞	26.7	38.2	22.3	12.6	50.0	1556
2	22.1								12.7	50.0	1548
3	∞								12.7	50.0	1550
4	21.9								12.7	50.0	1550
5	23.7								13.0	49.0	1550
6	19.0								12.8	57.0	1520

Table 4.10 The insertion loss of corresponding devices for variation 1

Testing device	RR2	RR4	RR5	RR6	1-cm DL	2-cm DL	3-cm DL	4-cm DL	5-cm bend WG	10-μm bend WG
Insertion loss (dB)	9.4	9.2	10.7	5.2	9.7	14.1	22.2	25.6	0.03	0.02

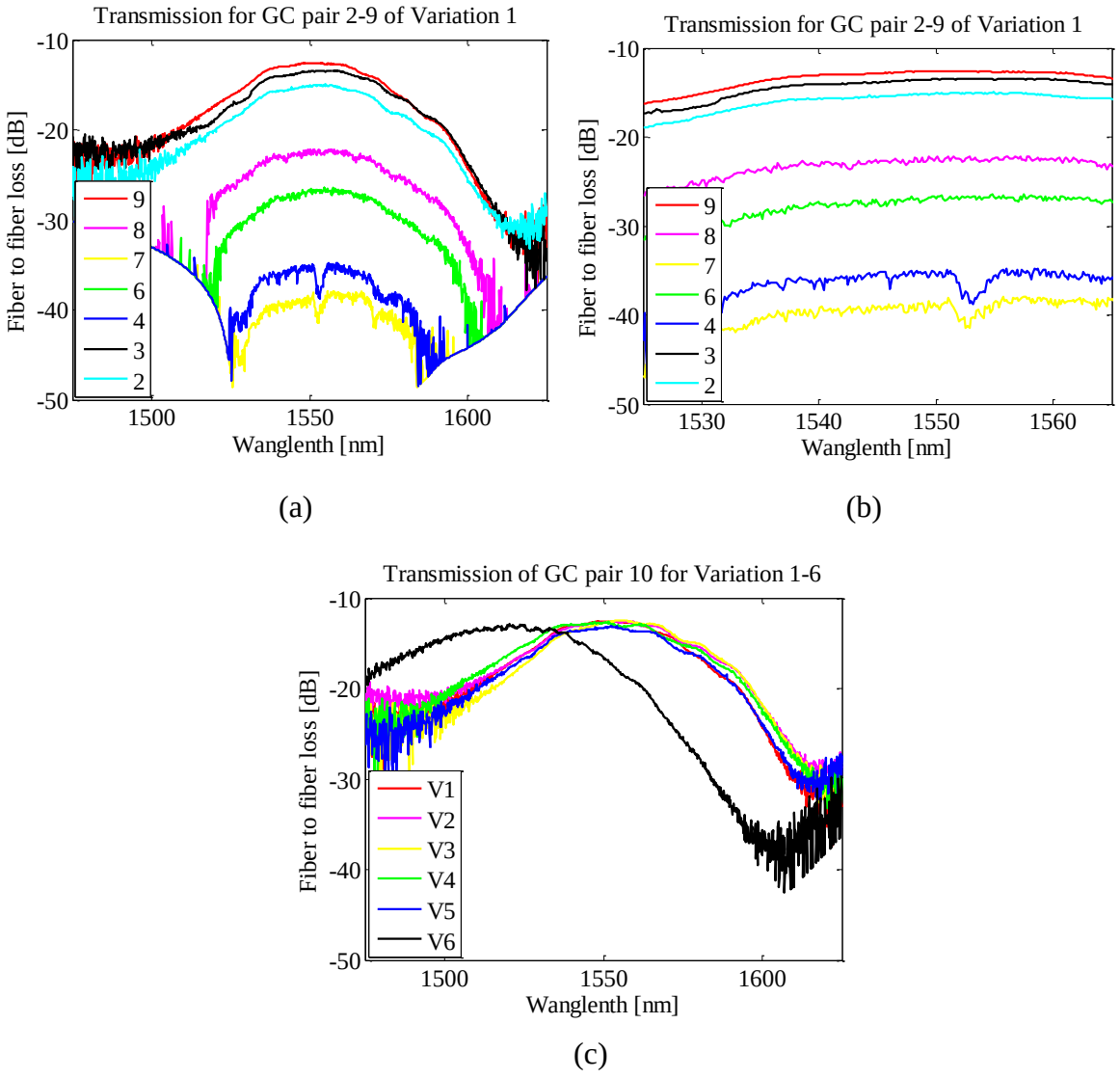


Fig. 4.24 Transmission of (a) grating pairs (j = 2-9), (b) the corresponding zoom-in for variation 1, and (c) grating pair 10 for variation (i = 1-6).

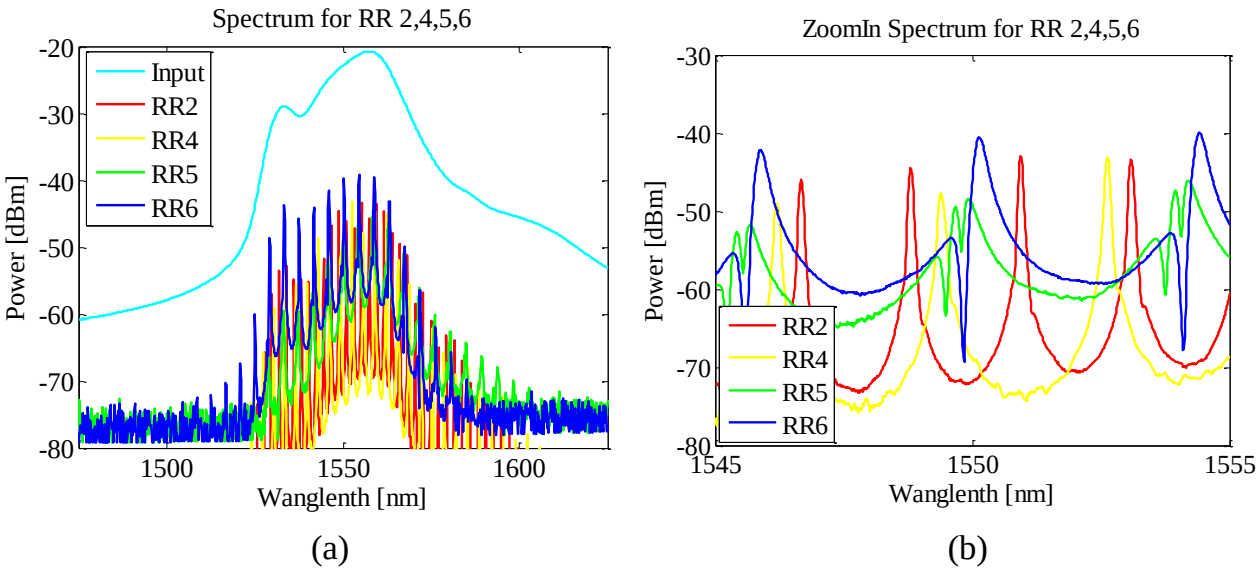


Fig. 4.25 (a) The output spectrum and (b) the corresponding zoom-in of ring resonators 2, 4, 5, 6.

4.4.2 Testing results with PROFA

The PROFA with 42.33-μm pitch and 13 degree polishing angle is utilized to test the PROFA interface with vertical alignment. Key parameters to be characterized include:

1) Insertion loss of grating couplers

2) Bandwidth of grating couplers

3) Cross talk of the PROFA interface

The equipment required for chip test are

1) Testing stages

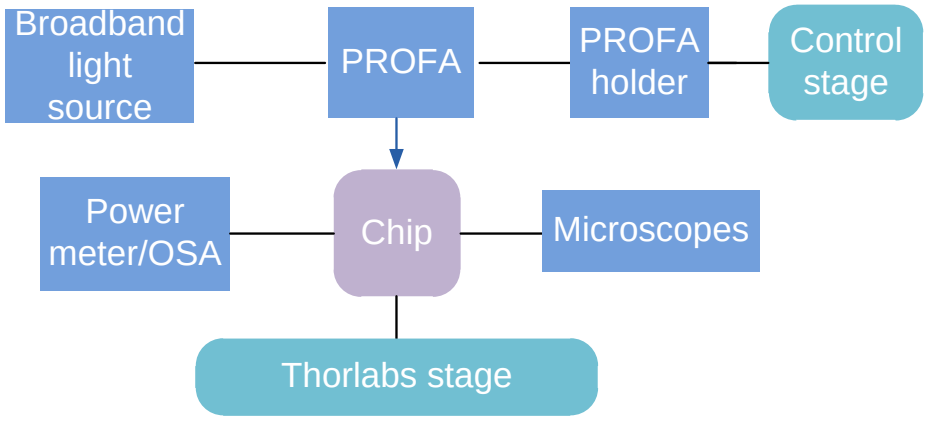
2) Broadband light source

3) PROFA

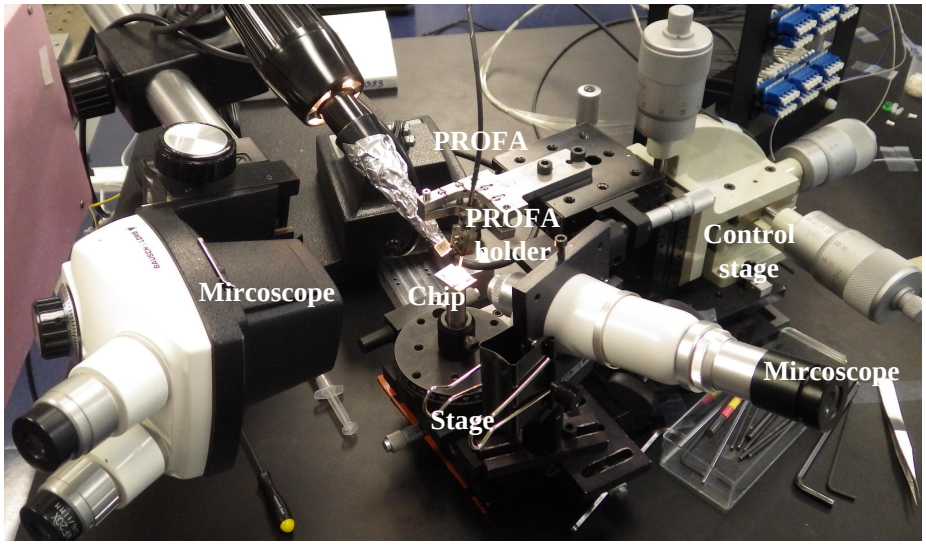
4) Microscopes

5) OSA/Optical power meter

The schematic of the chip measurement and experimental setup using the PROFA are illustrated in Fig 4.26(a) and 4.26(b). The picture of the chip under test captured through another microscope is shown in Fig 4.27.



(a)



(b)

Fig. 4.26 (a) Schematic of the chip measurement and (b) experimental setup with PROFA.

The grating couplers of PROFA interface for variation 2 are tested using the corresponding PROFA. The minimum insertion loss, 3-dB bandwidth (BW) and central wavelength from fiber to fiber are presented in table 4.11. In addition, the transmission for part of the testing grating couplers is shown in Fig 4.28.

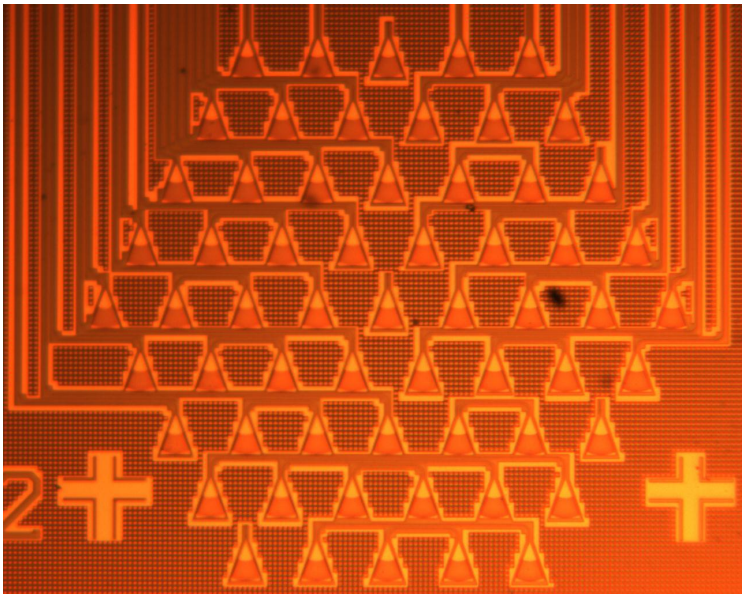


Fig. 4.27 The picture of variation 2 for the chip under test.

As can be seen, the minimum insertion loss for the designed grating couplers from fiber to fiber is 9.0 dB (4.5 dB per grating coupler), which is 0.5 dB higher compared to the simulation result. And the difference of insertion loss across the 61 channels is less than 1.5 dB. The 3-dB bandwidth is approximately 50 nm. The central wavelength is around 1550 nm with the incident angle equal to the polishing angle. The crosstalk of the adjacent channels is less than -50 dB, as shown in Fig 4.29.

Table 4.11 The test results of grating couplers with PROFA (fiber-to-fiber)

Grating couplers	Min IL [dB]	3-dB BW [nm]	Central WL [nm]
(3,4)	10.4	45	1550
(8,9)	10.1	48	1554
(16,17)	9.0	50	1553
(20,21)	9.7	50	1551
(33,34)	9.4	52	1553
(37,38)	10.4	45	1550
(48,49)	10.2	46	1555

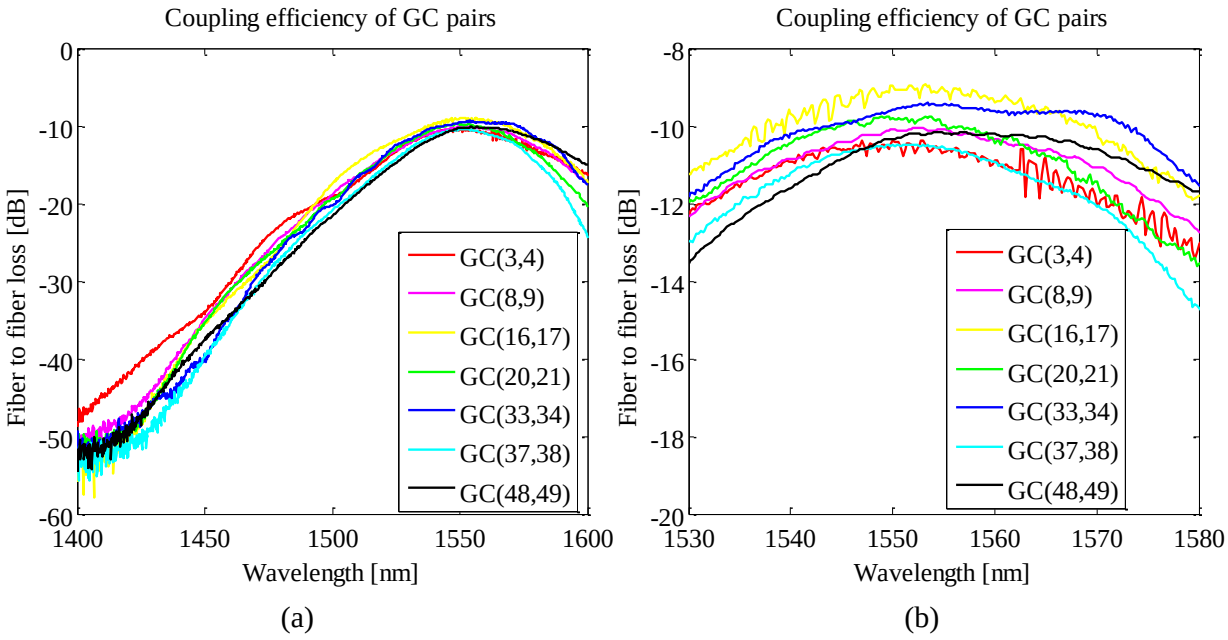


Fig. 4.28 (a) Transmission for GC pairs across PROFA interface and (b) the zoom-in of the spectrum.

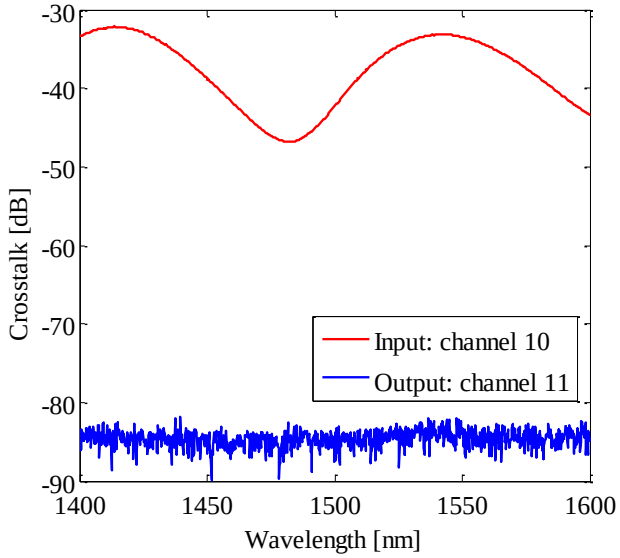


Fig. 4.29 Crosstalk of adjacent channels (10,11).

4.4.3 Test results analysis

With air cladding in simulation, the maximum coupling efficiency per grating coupler is -4 dB, which is 2.25 dB and 0.5 dB higher than that of the designed grating measured by fiber array and PROFA, respectively. The obtained 3-dB bandwidth of both measurement is approximately 50 nm, which is 20-nm narrower compared to the simulated value of 70 nm. And the crosstalk of the adjacent channels is less than -50 dB. There are mainly two reasons leading to the extra 1.75 dB loss measured by the fiber array

1) Misalignment. There are mainly angular (tilt) and positional alignment errors in terms of alignment tolerance. As the designed grating coupler size is much smaller, it is rather difficult to obtain an optimal alignment between the fiber array and grating couplers.

2) Air gap. The effect of the distance between the fiber array facet and gratings depends on the diffraction of the Gaussian beam for the input source. According to [38], the additional coupling loss is negligible for distance below 15 μm. But the additional loss reaches 0.5 dB for a distance of 55 μm. Large air gap between the fiber array and grating couplers will increase the measured insertion loss while nearly seamless horizontal contact enable low insertion loss using the exact matching PROFA.

Based on the experiment results, it can be found that the grating coupler dimensions have insignificant effect on the insertion loss (*e.g.,* width, taper length and grating length). In simulation, the transmission almost stays the same when the following conditions are met.

$$\text{Width} > 16\ \mu\text{m}$$
$$\text{Taper length} > 10\ \mu\text{m}$$
$$\text{Grating length} > 10\ \mu\text{m}$$

As such, the impact of the dimensions on transmission is trivial if the grating dimensions satisfy those requirements.

In addition, a central wavelength shift around 35 nm can be seen for the designed grating coupler with a 13-degree incident angle (GC6). This corresponds to a wavelength shift of approximately 5.0 nm/deg. While in simulation, the wavelength shift is about 7.0

nm/deg. The mismatch between the simulation and experiment could be caused by the imperfect alignment and fabrication errors. Also, as the light source (EDFA) is within C-band, there might be some errors for measurements when the central wavelength is out of C-band. Further, the chip with oxide cladding has been tested. Through adjusting the incident angle, performance is similar for grating couplers with air and oxide cladding.

As can be seen in table 4.10, ring resonator 6 has the maximum coupling efficiency. However, there are detrimental dips near the resonance wavelength. There are approximately 9.2-dB insertion loss for both ring resonator 2 and 4 with good transmission. With regard to the bending waveguides, the bending losses are 0.03 dB and 0.02 dB for 5-μm and 10-μm bend waveguides, respectively. As the bending loss increases with smaller bend radius, the bend radius is required to be larger than 5 μm. Besides, the calculated insertion loss of silicon waveguide is approximately 6.4 dB per cm, which is around 3 dB higher than the value reported by IMEC. This should result from the bending loss and scattering loss of the delay line consisting of a large number of bend waveguides.

Based on the test results using the fiber array and PROFA, the minimum insertion loss of the designed grating coupler is 4.5 dB without extra processing. As long as the dimensions meet the minimum size of 16-μm width, 10-μm grating length and 10-μm taper length, the effect on insertion loss is minimized. Nearly seamless horizontal contact with PROFA leads to insertion loss of approximately 4.5 dB and a bandwidth of approximately 50 nm compared to the simulation results of 4-dB loss and 70-nm bandwidth. The crosstalk of the adjacent channels is less than -50 dB. Some structures incorporated in the designed interface can be further characterized with the corresponding PROFA.

4.5 Conclusion

An ultra dense silicon photonics interface is designed and fabricated. The on-chip coupling interface between PROFA and PICs based on grating coupler array is introduced. The design and simulation of the optical interface are presented in detail, including the modelling and simulation of grating couplers, grating coupler array and PROFA interface and final device layout. Moreover, a high bandwidth Tb/s on-chip optical link is proposed based on the PROFA interface.

Experiment results show that the minimum insertion loss of the designed grating coupler is 4.5 dB, which is 0.5 dB higher than the simulation. As long as the dimensions meet the minimum size of 16-μm width, 10-μm grating length and 10-μm taper length, the impact on insertion loss is insignificant. Seamless horizontal contact between the PROFA and designed interface leads to insertion loss of approximately 4.5 dB and a bandwidth of approximately 50 nm compared to the simulation results of 4-dB loss and 70-nm bandwidth. The crosstalk of the adjacent channels is less than -50 dB. Some structures incorporated in the designed interface can be further characterized with the corresponding PROFA.

Chapter 5

Conclusions

The thesis research is related to optical interconnection networks, which are proposed as a promising solution to meet the increase of communication bandwidth and data throughput with low power consumption. The investigation develops an energy-proportional SOA-based optical space switches and exploits an experimental recirculating loop to assess the scalability. The investigation is agnostic to the architecture such that the results can be interpreted for different interconnection architectures utilizing SOAs as gating elements or optical amplifiers.

Moreover, an ultra dense silicon photonics interface for the coupling between PROFA and photonic integrated circuits is designed and fabricated. The performance of PROFA interface indicates a potential high capacity optical connection for off-chip and on-chip communications.

5.1 Thesis summary

The background of optical interconnection networks is introduced as well as silicon photonics interconnect in chapter 1. The recent development on optical interconnects is also discussed in this chapter.

In chapter 2, an overview of optical interconnection networks including optical interconnects for data center/HPC systems and several optical interconnect schemes is provided from the literature. An SOA-based optical space switch combined with different imple-

mentation architectures and key performance parameters of space switch is presented. In addition, enabling technologies of silicon photonics for optical interconnects are discussed with regard to basic silicon photonics building blocks and the coupling between nanophotonic waveguide and standard optical fiber.

In chapter 3, the scalability of SOA-based optical space switch has been evaluated using a recirculating loop with FPGA-controlled and self-enabled SOAs. The M×M space switch interconnection and FPGA-controlled recirculating loop test-bed are elaborated. Moreover, the impact of PDG, space switch scalability, XGM effect, together with architecture scalability and energy efficiency, are discussed in detail. An SOA model as OSNR predictor has been discussed indicating a good agreement between experiment and simulation results on OSNR evolution with cascaded SOA gates.

An ultra dense silicon photonics interface is designed and fabricated in Chapter 4. The drive for on-chip PROFA and PIC interface is introduced. The modelling and simulation of grating couplers, grating coupler array and PROFA interface and final device layout are presented as well. Experimental results show that a minimum insertion loss of 4.5 dB and a bandwidth of approximately 50 nm of designed grating couplers are realized. A promising high bandwidth on-chip optical link can be obtained using the designed PROFA interface.

5.2 Outlook

The future research related to the thesis work is presented based on the current progress in this section.

5.2.1 On-chip SOA-based optical space switch

As mentioned in section 1.3, the SOA-based optical space switch is implemented with the fiber-based components in the current work. With the development of hybrid sources and efficient devices in silicon photonics towards a high-density optoelectronic integrated circuits, the application of integrated switching fabrics are advancing rapidly. Several monolithic switches using SOAs as switching elements have already been demonstrated in [19] [44]. The scalable energy-proportional SOA-based space switch can be integrated on chip to dramatically scale down the footprint while improving the energy efficiency.

Further, the performance, containing the scalability and energy efficiency, of large-scale on-chip SOA-based space switches can be experimentally assessed exploiting the presented methodology. A more complete SOA model taking into account the dynamic performance and nonlinear effect can also be utilized to simulate the performance of on-chip space switches with OptiSystem.

5.2.2 Investigation of high capacity optical link

The designed PROFA interface has been partly tested with the fiber array of 127-μm channel spacing. Some structures (*e.g.,* Mux/Demux) incorporated in the designed interface should be further characterized with the corresponding PROFA. As such, the characterization of insertion loss, bandwidth, crosstalk and alignment tolerance of PROFA interface as well as other testing functional blocks should be completed next. Based on the characterization of the designed grating coupler array and ring resonators, the integration of PROFA and Mux/Demux can be implemented to achieve an ultra high capacity on-chip optical connection.

References

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