

PERFORMANCE MONITORING OF PDP-11 COMPUTERS

by

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ABSTRACT

Various system monitors and performance analysis methods have been surveyed. Software and hardware techniques are compared with reference to certain applications. An investigation of a general model for performance measurement tools has resulted in the development of HIMOS, a hybrid interactive monitor system. It is designed for a PDP-11 minicomputer installation. The software and hardware parts of the monitor are controlled from another PDP-11 computer. The system can work in sampling and event driven mode. Its ability to interfere actively with the performance of the measured system can be used for dynamic changes of the measurement session. The control system provides online and offline analysis of event reports. Monitor output is directed to a graphic display unit and can be concurrently recorded on tape or disk. The usage of the monitor in several application fields is illustrated through examples.

RESUME

Plusieurs moniteurs de système d'ordinateurs ainsi que des méthodes d'analyse de performance ont été étudiés. Des techniques de programmation et d'électronique ont été comparées. Un modèle général d'instrument de mesure de performance a été examiné et il en a résulté le développement de HIMOS, un système de moniteur hybride et interactif. Il est conçu pour une installation de mini-ordinateur PDP-11. Le programme et l'électronique du moniteur sont contrôlés par un autre PDP-11. Le système peut prendre des échantillonnages ou réagir sur des événements. Il peut intervenir sur la performance de l'ordinateur observé, changeant ainsi la séance de mesure. Le système de contrôle permet l'analyse des rapports d'événements en ligne ouverte ou fermée. Les résultats sont dirigés sur un écran cathodique et peuvent être enregistrés simultanément sur bande ou sur disque. L'emploi du moniteur est illustré par différents exemples.

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CHAPTER 1

Introduction to Performance Evaluation

1.1 Need for Evaluation

Prior to the description of the implementation and application of a practical tool for performance measurements in a computer system a discussion of the more general aspect of performance evaluation for which those tools are required will be presented.

The need for performance evaluation has not always been as apparent as it is today. First generation computer systems had a very simple structure and the central processor unit (CPU) was the dominant part of the installation. Peripheral devices such as magnetic tape drives, paper tape readers and punches were mainly used to maintain the traffic of program, data, and results between the system and the outside world. The devices were under direct control of the CPU. Computation and I/O were not overlapping because the CPU was dedicated at any time to one or the other activity. For scientific applications the power of a system was mainly dependent on the CPU speed. For commercial use the processing speed was generally limited by the performance of peripheral equipment.

The manager of a computer centre was able to charge his customers by the clock on the wall. His main concern was to insure the availability of his system. Availability can be defined as a measure of the likelihood that a system is operating properly at a given moment, or as the percentage

of time during which it is working properly.

With the advent of second and third generation systems, the complexity of information processing systems has grown considerably. For a human observer it became impossible to determine which job was executing at a certain time in a multiprogrammed environment. A scientific user could no longer expect the execution time of his program to decrease by factor two when the processing speed of the CPU was doubled. The interactions between hardware, system software, and user programs are far too complex as to allow this kind of simplified deduction.

It was not only for accounting purposes that a whole industry for performance measurement tools came into existence. Very soon it was felt that it was not enough just to write system and user software with the only goal to make it work. As the cost for maintaining computer systems went up one became more concerned about their efficient use. The performance of an existing installation had to be increased and criteria for future hard and software development had to be gathered. As a large variety of systems is offered on the market, there must be a method to compare the different products with regard to the intended application.

With the growing complexity of modern operating systems it is difficult to fully understand their behaviour. A system analyst has to know which parameters affect which aspect of the performance if he wants to tune a system. He may be confronted with side effects which he did not expect. His decisions have to be based on information that he can only

obtain through performance measurements.

1.2 Some Definitions

In order to define performance of information processing systems some terms have to be introduced first.

Throughput is the rate at which a given workload can be handled by the system. The workload can consist of payroll processing where throughput would measure the number of payroll statements per hour. If we consider a network node, this measure indicates the number of messages switched per hour. In a University environment we would be interested in the number of ALGOL or FORTRAN statements compiled per minute. A detailed discussion of workload characterization is given by Ferrari [1].

Depending on the application, another measure can be more important: Turnaround time is defined as the delay between the presentation of input to a system and the receipt of output from it [2, p.13]. Turnaround time is mostly used in connection with batch processing systems where it can specify the time span from putting cards into the hopper of a card reader and getting a complete listing on the line printer. Other papers include human factors such as operator handling time, think time, debugging time etc. into their definition (see for example [3, p.262]). But in this case we should speak about the time which is required for one test and debugging cycle.

Closely related to turnaround time is the term "response time". However this applies more to real time applications. For industrial process control response time could measure

the time elapsed between the arrival of a signal indicating the position of a work piece and the emission of some correcting signal from the computer. In a time sharing environment, response time gives the period between a user's request from the terminal and the moment at which the system is able to service this request.

It should be pointed out, that system overhead (the processing time which is spent in the operating system as opposed to the time spent in a user program) is not a fundamental measure of performance. The goal of performance improvement is not to decrease overhead but to increase throughput and to decrease response time. Overhead can be used as a descriptive parameter but it does not necessarily affect performance.

In the previous examples, the term "performance" has been used in different ways. Intuitively we can have a certain feeling for what it stands. However performance as an independent entity does not exist. It can be discussed only in the context of a specific application or a set of applications.

For example a high level language compiler may be judged by its compilation speed. This is an adequate measure in an educational environment whereas other users are much more concerned about the quality of the object code produced or the storage requirements for the compiler.

In a commercial computer center, performance is related to cost effectiveness. However this measure has to be interpreted carefully with regard to the individual application [3]. A fairly basic measure of performance,

giving the mean cost of delay to each job is suggested by Greenberger [4]. Generally we want some measure of effectiveness that is related to the ability to process jobs where jobs can be user programs or operating system tasks.

1.3 Performance Evaluation Techniques

One approach to performance evaluation is to describe the target system by means of an equivalent model. A model is an abstraction of the real system containing only the significant variables and relations. It is usually much simpler than the system it models. On one hand, the input to the model can consist of data about the actual workload of an existing computer installation. On the other hand information about the expected task volume of a projected computer system can be used. As this technique has to employ some simplifications in order to keep the volume of the model at a feasible size, the result can only give an approximation of the real performance. This method is widely used in the field of system design and research.

More precise results about the performance of a working system can be obtained from the analysis of performance measurements. Especially for the application in computing centres where observations about the actual system usage are necessary, this technique has known a growing popularity during the last ten years.

Calingaert [2] has given a very good review of the different performance evaluation techniques. The decision to use one or the other of those methods depends on the individual application.

1.3.1 Analytic Models

In analytic models, the relation between system variables and performance parameters is described by a set of mathematical equations. In accordance with real system behaviour it is assumed that events such as the arrival of a new job at the input appear in a stochastic manner. This means that variables can change their values in a random fashion but the range of values and the probability of the occurrence of a certain value is known.

We may for example know a given workload for the system but we cannot predict the sequence in which the jobs of this workload will arrive at the input. Let us consider a simple model of a batch processing system given by Graham [5,p.406]. In figure 1.1 new jobs which enter the system at the input are stored in a first-in, first-out (FIFO) queue. Time is divided into units called quanta, each of which is exactly 0 seconds long. At the end of each quantum a new job can arrive at the tail of the queue. The job at the head of the queue is allocated to the processor where it is executed until completion. Once the execution is terminated it leaves the system at the output and the next job is shifted to the head of the queue. If the queue is empty, the processor remains idle.

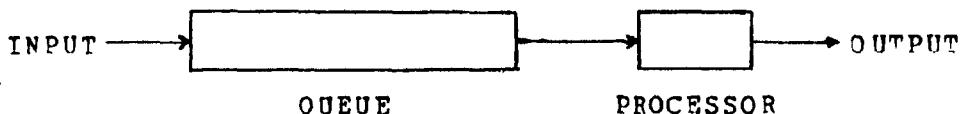


Figure 1.1

To construct an analytical model, the job arrival time and the execution times for each job are expressed by probability distributions rather than in absolute terms. For example it can be assumed that a new job arrives in the system at the end of each quantum Q with probability pQ . The resulting job arrival distribution is a special case of the discrete Bernoulli distribution. The job's execution time can be chosen independently from a geometric distribution, s , assuming that each job requires an exact multiple of Q for processing. The probability that a job requires n quanta for execution is then expressed by $s(n)$.

We can modify the previous model to study the round-robin scheduling policy which may be used in time-sharing systems (fig.1.2). In this case the processor is only allocated to one job for exactly one quantum of time. If the execution was not completed at the end of one quantum the job is fed back to the end of the queue. There it waits together with other incomplete or newly arrived jobs for its next time slice in the processor. Assuming that a job's execution time is exactly nQ , it will have travelled n times though the system before it has completed.

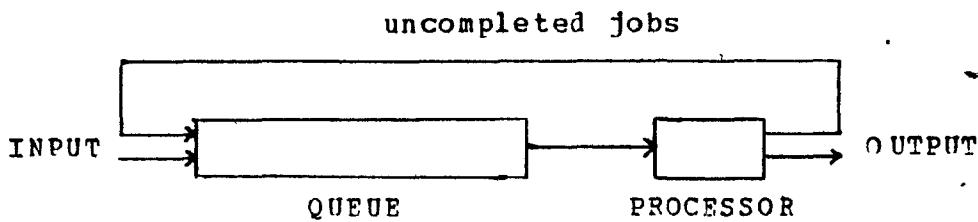


Figure 1.2

Another version where this model is extended by a second queue to buffer the incoming jobs is given by Blatney et al. [6,p.412]. According to a selection algorithm, jobs are chosen from this auxiliary store to be placed at the end of the queue of the previous example which now serves as intermediate storage area for uncompleted jobs. Further levels of detail can easily be added to the model, but as is shown in the above mentioned paper, a deep analysis of the model can already become quite complex.

For the first two examples, Kleinrock [7] has derived equations for the expected total time that a job spends in the system under the above stated assumptions.

A more complex model which analyzes the system throughput as a function of input/output and processing overlap is described by Hellerman and Smith [8]. Several simplifying assumptions had to be adopted to keep the mathematical framework within practical limits. This shows already a severe drawback from the technique of analytical models. For complex systems, the relation between different variables may even not be expressable by mathematical functions.

Analytic models are most useful for the evaluation of subsystems of limited size (e.g. drum paging efficiency

[9]). As they need a certain degree of detail for their descriptive parameters they are in general used for evaluation of existing systems. At earlier stages of system development where this information is not available, the simulation technique is more appropriate.

1.3.2 Logical Models

While for analytical models, the system structure has to be translated into mathematical terms the logical model reflects this structure more directly. There are several different ways to express a system structure.

The directed graph model is very similar to a flowchart of some software. System states are represented by nodes and transitions from one state into another are shown as directed arcs. More details on this technique can be found in the literature [10,11].

Another interesting approach to logical modelling is in the use of Markovian models. Foley [13] has described such a model, using a discrete time semi-Markov chain where the time interval between successive state transitions is fixed. The chain is described by a transition probability matrix whose elements are the probabilities of entering a certain state from the current state of the system. The transition probabilities can either represent expected or estimated values, or they can be obtained from measurements on the executing target system.

Simulation which is the most frequently used technique among logical models will be discussed in more detail in the following section.

The first step in simulation is to define a dynamic model of the investigated computer system. The model consists of classes of entities, the attributes of these classes, a set of activities, and a set of events. A job that is to be executed by the system represents, for example, one class of entities. It can be described by attributes such as memory requirement, I/O activities, execution time etc. Activities are, for example, arithmetic computations or waiting for I/O completion. A job that enters the system causes an event; I/O interrupts can also be classified as an event. Events have no duration but in general they induce some activity.

The basic concept of simulation is time. Although simulation time is usually not equal to the real system time, the simulator controls events and activities with regard to its own time scale. Thus the simulator follows the sequence of events which indicate changes of the system state over time. Models for simulation of digital computer systems increment time in discrete intervals whose length correspond to the simulation time between consecutive events.

To simulate a system, a set of different experiments is conducted on the model. In other words, a sequence of different workloads is presented to the input of the model and results about the system performance on this input are obtained.

Another way to drive the model is to measure certain parameters such as job arrival time, distribution of page faults etc. in a real system and to use this data as input to the model. During simulation, other performance

parameters can be varied to find their optimal values. In this case we speak about trace driven modelling.

If required, the simulation results of a series of experiments can be formulated as mathematical equations describing the relationship between system variables and performance parameters. This abstraction can then be used to carry out further experiments more economically. This indicates that there is no absolute separation between analytic models and simulation models. For example, some subcomponents of a system can also be described analytically within a simulator. Of course, it is much easier to modify some aspects of the system in a simulation model just by replacing attribute definitions than by modifying the complex equations of the other model. In simulation no attempt is made to isolate relations between variables; observations are merely carried out on how they change their values with time.

In practice, the task of creating a simulation model is simplified by special purpose simulation languages such as GPSS (General Purpose Simulation System) or CSS (Computer System Simulator) [14]. Those languages provide facilities for varying parameters, for different experiments.

Especially at the planning stage of computer system development the simulation model represents the most convenient technique for performance evaluation. It is not only the most flexible of all models but it also can be constructed to any level of detail. Concurrency of activities can easily be modelled whereas analytic models are not able to express this feature which is becoming more

and more important in modern computing systems.

However all modelling techniques have common disadvantages. The obtained results can only be as good as the model. Analytical models are often oversimplified to reduce their complexity whereas simulation models are very expensive. Simplifications and assumptions in less known areas of the system can lead to undetected distortion of results. The validity of a model can be examined by comparing the results with those obtained on a real system but of course this is only possible if this system already exists. As the performance of a system is a function of the input, the experiments have to be designed at least as carefully as the model.

1.3.3 Performance Evaluation Programs

The techniques described in this paragraph apply to installed operational systems. They are mainly used to compare performance of different systems or to verify expected improvements of system behaviour. Executing the same assembly run on two different machines, we may observe different execution times just by looking at our watch. But even by timing the runs with a clock with a resolution of one microsecond would not tell us why machine A is faster than machine B. If we did the same test with another sample job we could obtain the opposite result, computer B being the faster one. In order to achieve more objective results, artificial workloads consisting of special programs or sequences of programs have been developed to evaluate the performance of computing systems.

The simplest technique in the class of performance evaluation programs is the instruction mix. The frequency of a machine instruction is derived from a dynamic trace under real workload. In the instruction mix, each instruction execution time is then weighted by a coefficient based on the frequency measurements. A table of instruction weights for a scientific and for a commercial mix are given in [15]. Knowing the instruction execution times of the target CPU a value representing the CPU performance can easily be calculated. The result depends on the dynamic trace which determines the relative importance of each instruction with regard to the overall performance.

The kernel technique uses another attempt to define a representative workload. It is composed of one or more assembler routines, each of which solves a specific computational problem, e.g. matrix inversion or evaluation of a polynomial. The set of problems that form a kernel is considered to be representative of the predominant application of the system.

The kernel technique has the advantage in that it is more CPU independent than the instruction mix as it tests performance on a task level rather than on the instruction level. However an objective comparison of different CPU's depends on the objective programming. The advantages and disadvantages of the last two techniques are discussed further in [2].

So far, the I/O characteristics of a system have not been evaluated. Benchmark problems include this feature in their workload definition. A popular benchmark problem for

commercial installations is the file updating program [16]. A processor reads a master file from disk or tape, updates it according to a detail file and produces a report file containing a record of each transaction performed.

Many attempts have been made to standardize benchmarks, but in general, they still reflect a special application. This technique may be valuable to gain insight into the expected performance of a system mainly used for a particular application environment but it cannot give a global measure of system performance.

Synthetic jobs as proposed by Buchholz [17] are more flexible than benchmarks. In those programs, written in high level languages, various resources may be parametrically changed to fit the characteristics of a real workload. This is done by several tasks which are executed cyclically. As every task requests for another resource (memory, CPU-time, I/O channels, etc.), the loop parameters can be adjusted to the system size and the workload to be simulated.

The techniques described so far evaluate system performance under the condition that the test program is the only one executed in the system. In this case the execution time of the job is used for evaluation or comparison. For timesharing systems we would rather want to measure the response time under an artificial workload. This means several users have to be simulated submitting different tasks concurrently to the system. A description of an internal driver simulating interactive users for the MULTICS time sharing system is outlined in [18]. Each user is

simulated by a process which can be considered an interactive benchmark consisting of a fixed sequence of commands and fixed think times.

Criticizing performance evaluation programs, one can say they rather define performance than evaluate it. Yet, if well understood, they can give some information about performance with regard to the yielded application. If they are used along with performance measurement techniques (which will be discussed in the next chapter), the obtained results can help to improve system performance under a well defined workload.

CHAPTER 2

Performance Measurement Techniques

Performance measurement or monitoring can be defined as the process of obtaining useful information on the performance of software and software controlled computer hardware. The earliest measurement tools were developed around 1956. They were able to supply information such as job execution time or core utilization which was obtained by core resident software monitors. In 1958 IBM developed the first laboratory version of an external hardware device for performance measurement. Tables A.1 and A.2 give a historical overview of some of the monitoring tools and their capabilities that have been implemented so far.

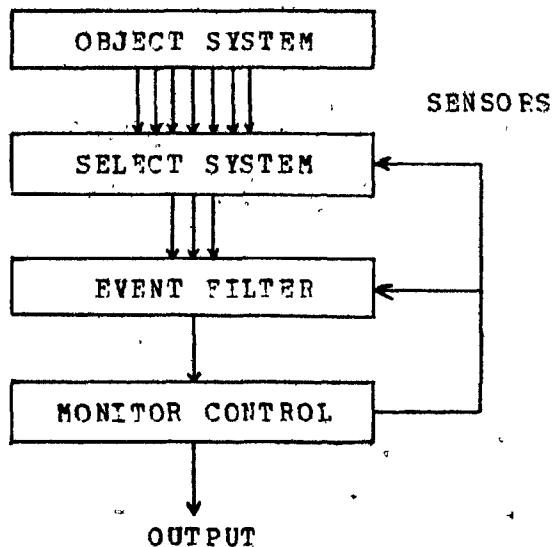


Figure 2.1: General model of a system monitor

The basic structure of a monitoring facility can be

described by the model in figure 2-1, regardless of hardware or software being used to extract the information. The computer system which is to be measured is called the object or host system. Sensors collect signals which indicate changes in the state of this system. These changes are also called events. The sensors can be implemented by software or hardware. Their implementation will be discussed in more detail in the following chapters. A hardware sensor for example can indicate if the wait light on the computer console is on or off. On the other hand, a software sensor can give an interrupt to the monitor whenever execution of a program passes over a predefined point in the code. The select system chooses desired observation points at times when their states are of interest. The measurements then proceed through the next stage where the flow of events is filtered so as to reject signals that are irrelevant for the particular monitoring session. Both selecting systems are supervised by the monitor control which receives the preprocessed signals and produces some sort of output.

Early monitoring devices in general recorded the collected data on magnetic tape. Programs were written to process these tapes after a monitoring session, reducing the large amount of data and creating statistical reports. The problem of interpreting monitor results is considered in [31]. Later monitors reduce and process the incoming data in real time besides producing a detailed record on mass storage. Graphic displays provide a convenient way of visualizing immediately system activities as they take place.

2.1 Objectives for Monitoring

Monitoring is used to obtain exact information about the various activities in a computing system while it is executing some tasks. One of these tasks is the operating system itself which normally is the most complex program of a given system. In general computer manufacturers offer a range of operating systems for different applications. However the detailed specifications which depend on the individual computing environment have to be entered in the form of parameters to the system. Many of these values, e.g. the maximum number of connected terminals or the number of tape and disk drives can be determined right at the beginning. However for tuning the operating system to achieve optimal execution a system monitor is almost indispensable.

2.1.1 Measurement of System Activities

Before optimizing system or user software we have to get a picture of the real system activities during execution. Measurements can give a utilization report for the different modules of an operating system. Based on this information, more frequently used modules can be made core resident while others can be stored on disk or drum. The statistical analysis of a disk usage report could show a high probability that module B is accessed immediately after module A on the same device. In this case seek times can be reduced by locating both files in the sequence A,B close together on the same device.

Many times device bottlenecks have slowed down a whole computer system. It can be very painful to pinpoint the source of troubles if no monitoring facilities are available. Using a monitor, an unexpected overload of an input/output channel can easily be detected just by sampling the channel activities during peak periods. This can also lead to predicting future facility requirements of the computing centre.

System measurement may also help to improve the coding of software. Cantrell and Ellison [19] talk about "performance bugs" by which they mean errors in evaluation or judgement of performance optimization. If the performance of some software is important it should be performance debugged by measurement and analysis. Inefficient parts of the program can be detected and recoded.

Another way to use monitors which have already been proved to be useful is in connection with simulation to produce what is called "trace driven modelling" [15]. A very detailed profile of the job stream, down to an almost microscopic level is observed and supplied as input to the simulation model.

Most operating systems are documented by numerous manuals and even if their descriptions are accurate (which is not always the case), system understanding is better facilitated by monitoring devices that show what really happens in the computer. A performance monitor with graphical output can help teach different aspects of operating systems. Such a device could also be used as feedback to the operators enabling them to make decisions.

The main objective of monitoring in this thesis is to offer a tool for operating system research and development. The monitor can be used to verify the efficiency of algorithms for paging or task scheduling. For the MULTICS operating system [20] this application has proved to be very useful [18]. Performance measurement can also be used for general software research such as program correctness proofs, automatic flowcharting, tracing, and debugging (see for example the SNUPER COMPUTER project [21]). Some of these possibilities are discussed further in chapter 6.

2.1.2 Prevention, Detection and Recovery from Failures

As mentioned in the last chapter, availability is an important factor in computer system performance. The conventional way to increase availability is to schedule certain maintenance periods during which the system is not accessible to users.

Permanent monitoring of the activity of system devices, including the CPU can help reduce maintenance time and yet insure high reliability of the system. Most operating systems are already able to capture fault conditions and produce a corresponding message. Monitoring facilities can go a step further, producing a precise report on all error conditions to show the maintenance personal where to concentrate their efforts. Further improvements are obtained when the monitor analyzes fault conditions and executes some of the diagnostic routines on the devices that reported failures. When this is done during idle time of the system, the time for maintenance can be reduced even

further.

In every computing system there are some resources which are vital to its operations. If the disk drive which contains operating system modules, part of main memory or even the CPU itself is working improperly then the system is "down". At installations that control important processes such as air traffic control or centrals for electric power switching, backup equipment for the most important resources is indispensable. In these systems a monitor could quickly detect an error condition and initiate the necessary actions to replace the defective device by its backup. In computer networks a node causing problems can be located and messages can automatically be routed through another path avoiding this node.

With the growing complexity of operating systems and multiprocessor hardware the reliability of computer installations becomes an increasing problem. Many times users are frustrated by system crashes which are due to implementation errors. For the system manager it is often a very difficult task to reconstruct and analyze the reasons for the malfunction. Dynamic verification and consistency checks by a measurement device could help analyze and even prevent such events. Plausibility checks can, for example, detect unreasonable overusage of resources which may be a hint for failure in the near future. This situation is typical for deadlocks which occur when the resource requirements of different tasks cannot be resolved. One approach for dynamic verification of operating system decisions is described by Fabry in [22].

2.2 Software Monitors

The earliest monitoring techniques developed used programs in core to monitor what the system was doing. These monitors are an integral part of the host system, i.e. the system that is to be analyzed. Thus, the monitor is both logically and physically a part of this system. The primary attribute of an internal software measurement technique is that it has access to and can selectively record system data stored in memory or CPU registers (depending on the computer architecture, device registers and buffers can be examined too).

When activated, the monitor interferes with the system operation to record and analyze values of interest. This leads to some considerations for the development of software monitors:

- The monitor must not alter any system variables except the ones that belong to the monitor itself.
- Resources used by the monitor, e.g. CPU time, memory space, I/O channels have to be well defined.
- The presence of the monitor must be logically invisible to the system.

Normally a software monitor is written in assembly language. The reasons for this are twofold: first, the execution time can be kept at a minimum and second, the access routines to system registers and memory locations have to be written in a low level language.

A survey of existing software monitors is given in appendix A, table A.1.

2.2.1 Sampling Technique

The basic idea of the sampling technique is to interrupt the normal flow of execution at periodic intervals where control of the system is passed to the measurement routine. The intervals can be determined by a clock or a combination of events in the system that meet some criterion. The best choice for the sampling rate would be a random time schedule which is known to be statistically independent of any natural execution pattern in the program to be analyzed. This avoids synchronization effects between the monitor and the sampled events which otherwise could amplify or zero out the recording of periodic events.

To obtain a compute time profile of a program, that program is loaded and run in its normal fashion without any modifications and without any need for prior knowledge of any of its characteristics. At the time of a sample, execution is interrupted and values of interest are recorded by the monitor. Some of the typical information gathered at this point is given in the following list:

CPU active

Location of next instruction to be executed

Instruction code

Location of data referenced by the instruction

Processor status word (PSW)

Status of channels, control units, and devices

I/O originators.

This information, recorded on tape along with the sample, time is sometimes called a "system's snapshot". At the

completion of the run this tape can, for example, be sorted by interrupt location address and the resulting frequency distribution printed. The accuracy of the sampling technique is based on the central limit theorem [23]. The central limit theorem states that the accuracy achieved improves as the number of random samples increases. If 8000 samples are taken, the probability that we will be within 2% of the actual value is 99.99%. After approximately 26000 samples, there is no substantial improvement in accuracy.

2.2.2 Intercept Technique

Another approach to software monitoring is to place intercept points (or hooks) at strategic locations in system software and application programs. When the monitor is enabled and execution passes over such a point, control is passed to the measurement program which records interesting values just as in the sampling mode before passing control back to normal execution. Contrary to the method described in the last chapter the intercept technique is very operating system and machine dependent. This is mainly reflected in the way how the hooks can be placed. In systems with many different vectored interrupts where each of them is responsible for a small group of peripheral devices, the interrupts can be intercepted to obtain information about I/O activity. If additionally the operating system and user programs exchange information by means of some sort of supervisor calls which cause interrupts, there is a convenient way of monitoring this type of activity with the intercept method. In some systems

an entire class of interrupts may be matched into a unique address. Generally within the system architecture there is further information which identifies the specific nature of the interrupt.

To create intercept points for events other than interrupts, the source code has to be modified by insertion of special intercept code at interesting points of the program. This is for example used to monitor if certain locations such as branch entry points or subroutines are executed. Details of the implementation of sampling and intercept monitors are described in chapter 4.

With the intercept technique the requirement for software monitors to be logically invisible to the system when the monitor is not active is more difficult to meet. While there are no problems to deactivate hooks which capture interrupts just by resetting the original addresses in the interrupt vectors, this can cause more problems for hooks that were placed into the code. As changing the source code to remove those points is impractical, a way has to be found to change the hook command into a NOP (no operation) command. In bigger systems like the IBM 370 series, this can be done by the EXECUTE instruction which has the ability to define a hook instruction either to be an interrupt creating one or to be just a NOP. Microprogrammable machines can support the same feature in a similar way just by redefining a micro instruction. For computers from Digital Equipment (PDP11 family) the problem has to be solved in a different way which will be shown in chapter 4. Another technique which is for example used at the McGill

computing centre should be mentioned. The software monitor (SLACMON, [51]) is invoked whenever the CPU is idle in order to use up all "spare" time. During those periods, a counter is incremented at a fixed rate. The counter value gives then a measure of the CPU load.

2.2.3 Comparison of Sampling and Intercept Methods

In a commercial computing environment where only the overall system behaviour has to be controlled, the sampling monitor would be a sufficient tool. It is relatively easy to handle and the degree of detail can be adjusted simply by changing the sample frequency. On a CPU with an average instruction time of one micro second and a sample rate of one milli second, statistically relevant information can be obtained after only 10 seconds with a maximum of 1000 instructions between two successive samples. In practice this means that a system profile can be updated in 10 second intervals. However the choice of the sampling frequency is not a trivial one and depends upon the yielded information. Another problem with sampling monitors is their low degree of flexibility. The set of values collected per sample during one session is mostly invariable. The selection will have to be general enough to give all the required information but it has to be detailed enough to minimize redundancy in this information. The number of values recorded per sample cannot be too large to keep the ratio of recording time to sampling period reasonably low and thus limit the overhead.

For applications where specific problems in a system have

to be analyzed and where each occurrence of certain events has to be recorded, the intercept monitor is the more appropriate tool. At initialisation a set of events can be defined along with an individual description of the information to be recorded for each of the events. This feature increases the flexibility of that monitor type and decreases the amount of redundant data recorded.

Assuming we want to monitor disk arm movement to find an optimal arrangement of files on that disk we can specify that only values like physical disk address, seek time and originator identification be recorded. If, in the same run, paging activity is to be monitored, the events indicating page faults etc. can produce a completely different set of values. This distinction cannot be made in sampling monitors where we would have to record the union of both sets for every event which of course increases the impact that the monitor imposes on the system.

In general, the main advantage of the intercept technique is the ability to concentrate on a clearly defined range of system activities and to generate a reproducible report.

The monitor overhead in the sampling technique is readily defined by the sampling rate and the number of values recorded per sample. This is not so easy in the case of the intercept technique. Actually the overhead is a function of the event occurrence. Additionally, an exhaustive overall system profile based on a statistical evaluation cannot be obtained.

As long as events can refer to interrupts, the installation of an intercept monitor is no problem: the corresponding

interrupt vectors just have to be modified to point to the monitor routine. But the installation, activation, and deactivation of hooks in the software code can cause some headaches. As mentioned in chapter 2.2.2 this depends on the system layout.. A quite unproblematic solution for computers in the PDP 11 family is shown in chapter 4.

All software monitors require host system resources such as CPU time, core memory, buffer space, I/O channel time, and mass storage. This of course is a disadvantage as the monitor's operation may distort the normal system activities and thus may lead to a situation which is known as the Heissenberg uncertainty. Therefore the impact of the monitor imposed on the measured system has to be investigated carefully before the results of a monitoring session can be analyzed.

2.3 Hardware Monitors

2.3.1 Architecture of Hardware Monitors

In the previous section we have seen that software monitors use resources of the host system. Among other reasons this was one of the drawbacks that led to the development of hardware measurement techniques. Table A.2 shows some of the hardware monitors developed during the last 18 years. A good description of the history of hardware measurement techniques is given in [24].

Hardware monitors collect electrical signals that indicate the state of the host system. Probes are attached to test

points or pins on the back panel of the computer system. These high impedance probes are completely passive to the host system. In other words, they do not affect the performance of the computer in any way. Hardware monitors usually operate in sampling mode rather than in the event driven fashion. In the second case an event is caused by the occurrence of an electrical signal at a probe point.

Once signals are presented to the monitor, they are generally made available at some form of logic plugboard. This is used to accomplish first level data reduction on the signals to determine states of coexistence and mutual exclusiveness. If, for example, the overlap of CPU and I/O channel activity has to be measured, we would "OR" the active signals of all channels and combine this output via a logical "AND" with the CPU active signal. More examples for the use of logical data reduction in hardware monitors are listed in [25].

The resultant signals are directed to several counters or recorded together with a time stamp on a storage media. Some of the more recent hardware monitors perform some real time evaluation of the incoming signals and update the result periodically on a display unit.

The method by which the signals are evaluated and recorded constitutes the major difference between early monitors and those available today. It also defines the type of measurement which the monitor can perform and thus is a means of classifying hardware monitors into major subgroups.

2.3.2 Summary Devices

The earliest hardware monitors developed by IBM were summary type monitors (see appendix A, table A.2). They recorded signals either by timing their duration or counting the number of times they occurred. The counter contents was periodically read out and written on tape. Thus, the summary type monitor could give information about the percentage of time a signal was active over the monitoring period. When counting the signals it gave the frequency of occurrence for the measured events.

It is important to note that, any dynamic properties of the system activities were lost in the accumulated information. However for computing systems in the early 1960's this monitor type was good enough to give a clue to what was happening in the computer. At many installations this technique is still used to produce overall system utilization reports.

2.3.3 Dynamic Monitors

With the increasing complexity of computer systems the need for more detailed activity reports became imperative. Information was required for input to various simulation programs whose accuracy depended on the actual distribution of I/O and computing activities. The summary type monitor would indicate the CPU being much more utilized than expected but the cause of the inefficiency remained unknown. One of the early attempts to overcome this problem by using a dynamic monitor is given in [26]. A dynamic trace of the

event "Jump instruction executed" was used to follow the execution flow and to detect loops.

Instead of merely accumulating the events, dynamic monitors provide a trace in time of events as they occur. The major problem in implementing these devices is that the computer is generally able to change its state faster than the monitor can record it. There are mainly two solutions to the problem: either the monitor's resolution is kept at a frequency at which the storage facilities are capable of registering the events or as in [27] the monitor is given the ability to stop the host system at certain times to follow up with the recording activity. However, the interruption of the host computer is against the principle of noninterference as stated above for the basic hardware monitors. Furthermore it can hardly be tolerated in commercial installations. Different buffering techniques have been implemented to increase the resolution of dynamic monitors without losing too much information.

2.3.4 Modes of Operation

Modern hardware monitors combine dynamic as well as summarizing features to provide information about different aspects of the host system activities. Corresponding to the measurements made by the early monitors there are basically three modes of operation:

1. Event mapping (E-MAP) mode: In this mode the counters used by the early summary monitors are replaced by words in the monitor's random access memory. The address of a memory word is given by the code of the event. The

contents of each memory cell represents either the accumulated count of the events or the total time a particular event is active. In the first case, the content of the according memory cell is incremented by one every time the event occurs. In the second case, the monitored signals are sampled at regular intervals as specified by an internal clock.

2. Time mapping (T-MAP) mode: While an input signal is active, a counter is incremented at a rate determined by an internal clock. When the specified signal becomes inactive a memory location whose address is given by the counter value is incremented by one. The monitor's memory then represents a frequency distribution for the duration of the observed signal. In practise this could be used to obtain the seek time distribution of a disk unit.

3. Store mode (S-MODE): The store mode corresponds to the trace measurements described in chapter 2.3.3. The event codes are simply written in consecutive memory locations as they occur or at the frequency determined by the internal sampling clock. The memory is divided into buffer zones which are periodically dumped on tape to free the storage space. The choice of one of the monitor modes depends on the information requirements. Several examples how these features of hardware monitors can be used are presented by Epstein [28].

2.4 Hybrid Monitors

While hardware monitors can virtually measure any significant physical machine event, they can capture logical events only in some cases. Protect key activity on IBM 360 systems for example is strictly a logical function of the operating system, but the register that contains the code for the protect key of the controlling task is in a fixed machine location and can therefore be monitored.

A number of extremely important system characteristics are never reflected directly in the hardware. Thus there is no efficient way for a hardware monitor to determine how much memory is occupied by user programs, how many jobs are currently in the job queue, the reasons why many jobs may wait for resource allocation before being initiated or how long a particular executive routine may reside in core.

The most evident advantage of hardware monitors is that they do not affect the host system in its performance. They are capable of sensing a wide variety of hardware and even some software events but they are limited in their ability to detect the stimulus for a set of responses. This cause and effect relationship can be better established by software monitors which take advantage of the fact that they reside within the host system. They have access to virtually any parameter which is controlled by the operating system software. Especially in multiprogramming systems, the latter technique can be used to investigate the system's task table and correlate the location of an event with the identification of the originating program. Physical machine

events, however, are beyond the reach of software monitors. In table 1.3 three monitoring techniques are compared with regard to the most important criteria.

Fortunately, the capabilities of hardware and software monitors complement each other and thus suggest a solution to this problem. The resulting type of systems monitor is called a hybrid monitor. The underlying premise of the hybrid monitor is that a hardware monitoring device is not invisible to the operating system, but instead, it is treated as an "intelligent" peripheral device.

This concept has been implemented at the MIT Lincoln Laboratory [2^a] where sensors and event counters are allocated to user programs under the control of software. The user can define which activities are to be sensed and the hardware device interrupts the user program as soon as it recognizes one of these events. The device has been used to derive an online histogram of the subroutine utilization, to investigate virtual memory performance of a single program and other similar tasks.

The distinguishing characteristic of hybrid monitors is that software can be used to determine activities which are to be measured by the hardware device. This implies that the commands to a hardware monitor are no longer given by buttons on the front pannel but they are dynamically supplied and altered by a software program. In table 3 the different monitoring techniques are compared.

For example, suppose the memory activity of a certain program is to be monitored. Soft hooks can be established in the supervisor's dispatching module to detect when the

program is about to be executed. At this point the software monitor can take control and transmit to the hardware the base address and size of the program. Since memory activity is to be monitored it also directs the hardware to select the memory address register as the source for the measurements.

One of the first hybrid monitors for systems with virtual memory is the DSP-1 [30] which is currently used at the McGill computer centre. It reduces the monitor overhead in the above mentioned example in the following way: A map of memory areas that have to be monitored is established by software and sent to the device which then continuously samples the content of the program counter (PC) and compares this value to the ones in the map. As soon as the PC enters one of the specified memory areas, the monitor starts to record predefined system variables.

As we have seen, the monitoring devices have become more sophisticated with increasing complexity of computer systems. While the first monitors purely recorded everything they were able to measure, the more advanced techniques concentrate on the problem of screening the sensed signals to eliminate redundant or unwanted information prior to the recording. Plugboard logic and event filters were improved but at the end it became obvious that many problems could be solved if a second processor were used to perform the preliminary data reduction. This has led to the last generation of performance measurement tools which will be the subject of discussion in the

following chapters.

CHAPTER 3

Monitoring with External Processors3.1 A General Instrumentation System

The DSP-1 mentioned in the last chapter is an elaborate tool for performance measurements. The sensory system which had to be programmed for different logical combinations on bulky plugboards in earlier systems is now controlled by commands on a console. However, the most important feature of the DSP-1 is the possibility to transmit those commands in remote mode from the host system, i.e. software residing in the monitored computer can define the preliminary data reduction and other parameters that control the monitor's operation.

As it has been shown, hybrid monitors combine the advantages of hard and software monitors but they are not flexible enough to change the monitoring mode dynamically as a function of the incoming events or to perform more complex real time data reduction. Due to the storage requirements of the map and store modes, memories were added to monitor devices. Their internal control structure required an increasing amount of hardware to supervise the data flow. The DSP-1 monitor incorporates already a special purpose processor to take care of these functions.

In this chapter one further step will be taken and a more flexible instrumentation system will be discussed which includes its own processor and software residing in the

monitor's memory. This model is, at the same time, the basis on which a performance monitor was developed and which will be the subject of the remaining chapters.

3.1.1 The General Model

Logically the monitor consists of three parts as shown in figure 3.1. The software monitor, operating in sampling or event driven mode, resides within the host system where it extracts information which is available in the host memory. The hardware monitor collects electrical signals with its sensory system and performs first level data reduction. Both units send the preprocessed information to the control or supervisor system. On the other hand, the control system has the ability to send data back to either of the monitors, interrupt their operation via control lines and also interrupt the host system itself. This last point is usually not found in commercial monitor devices. However, it has proven to be very useful for applications in research and development. Finally, after having processed the data, the control unit communicates the result over the I/O bus to some peripherals.

In the following three paragraphs we will take a closer look at each of the components. A functional drawing of the configuration is given in appendix A, figure A.1.

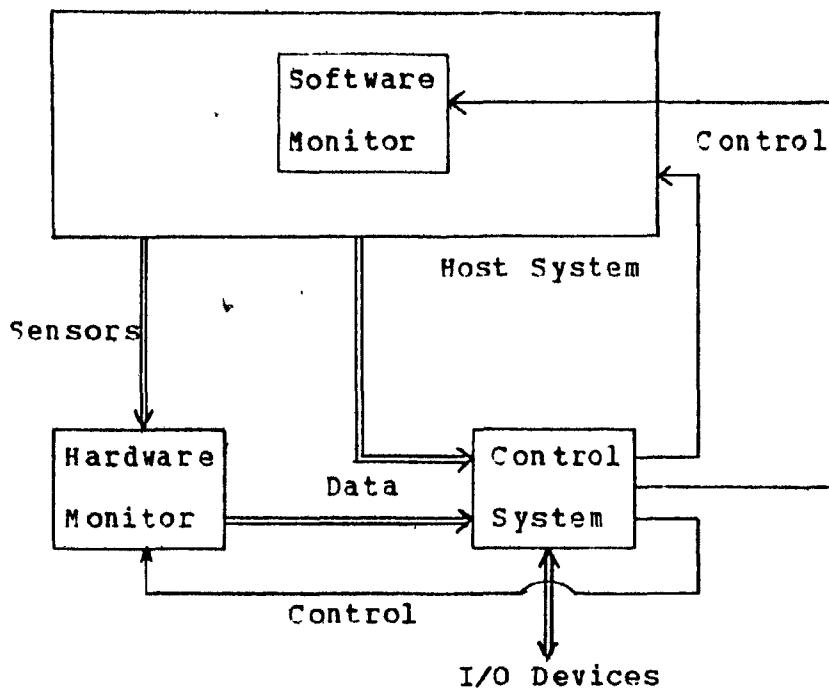


Figure 3.1: General Monitor Model

3.1.2 Software Monitor

This part of the performance measurement system resides in the host memory. For normal applications, the software monitor runs in the intercept mode because the data gathered in sampling mode can be extracted more efficiently by the hardware sensors.

As early as in 1967, as part of the "Snuper Computer" project [21], Estrin developed an idea for hybrid monitors which has been included in this system. Instead of inserting softhooks at strategically important points of programs which are to be monitored, the software is analyzed at compile time and the relative program counter value for those points is determined. The technique used by Estrin is

very similar to those used for program correctness proofs [35] (see also Chapter 5). At load time the absolute PC values of the event locations are determined and passed on to the sensory system which reports an event as soon as one of those locations appears in the PC during execution.

Of course, the method is not easy to implement as it requires changes in the operating system software, namely the compilers and loaders. It has the advantage that the system degradation is placed into utility tasks and the program to be observed can run without any interference. It is also a typical example for a situation where the distinction between operating system and software monitor begins to disappear.

When the monitor, running in intercept mode, has recognized an event it will collect relevant data and send it together with the event identification to the control CPU. This transmission can be done over a standard I/O channel of the host system. The same channel is used in the other direction to send information about the operating mode to the monitor. This has to include interrupt vector locations, a breakdown of events to be captured per interrupt if the vectors are used for multiple functions, and details about the required data per event.

3.1.3 The Sensory System

High impedance probes capture signals that indicate the state of the host CPU and its devices. In practice, a set of probe points is amplified in so called concentrators before the signals arrive at the sensory system. More about

hardware probe points can be found in the literature [32,33]. The signals then pass through logic circuits where the first level data reduction takes place. The combinatorial logic can take many forms. Generally speaking some logical relationship between the signals is determined. Instead of using a plugboard to specify which signals have to be compared and which logical function is to be used, the combinations are defined by the control processor. Additionally this remote technique makes quick changes during a monitoring session possible. The resulting signals are then presented at the input of buffer registers, counters or comparators. In the first case the data is ready to be transmitted to the control CPU or directly stored into memory by means of a DMA channel. Otherwise signals are either counted directly or used to open a gate to increment the counter with a fixed frequency during the signal duration. These two techniques correspond to the STORE or E-MAP mode and the T-MAP mode respectively.

Although the control CPU maintains its own time base it can be useful to send the host time to the monitor. Provided both systems increment time at the same rate, only an initial synchronization is necessary.

Apart from checking the input signals, the use of comparators leads to a new data reduction technique called sequencing. The first monitored value is compared to the contents of a series of registers. The index of the first matching register is remembered. In case there is no match at all, the value is ignored, otherwise the next value is compared with the register following the remembered one and

if the test is successful again, the index of the currently matching register is stored. This can be carried out a certain number of times depending on the size of the sequencer or infinitely if the comparator series is logically closed to form a loop. In a linear arrangement the result of this procedure indicates if a predefined sequence of values occurred in the host system or not. In the case of a closed sequence, a counter can keep track of how many times a loop was executed.

This idea can be carried further to analyze more complex sequences with alternative branches by arranging the comparator registers in the form of a finite state automaton. For any state there is a predefined set of events which can move the automaton in one of the successor states. If the received signal does not belong to the set or if the automaton enters a trap state the sequence of signals is rejected as not belonging to the language (in terms of the theory of formal languages) which was defined by the automaton.

Finally the circuit can have a "learning" ability if the first sequence of n values defines the comparators and is checked against the next n values. In the case of a match, a loop is detected and the comparator values can be transmitted to the control processor to identify the loop or else the second n values are used to redefine the comparator values.

However these attractive features require complex hardware and for economical reasons their implementation will have to wait for further innovations in hardware technology.

3.1.4 The Control Processor

The choice of the control CPU is no easy task. The CPU should have the following properties:

1. Execution speed similar to the host system
2. Fast I/O channels
3. A minimum of 32K words of memory

In general the control system is of a magnitude smaller than the one to be measured. This means that, for example, an IBM 360 installation should be monitored by a mini computer or if a mini computer is to be supervised, it would require a micro computer in the control system. This, however, creates difficulties regarding the first point stated above. In most cases the speed of a CPU decreases with the size. The reason for this lies in the architecture of the central processor control. Large scale systems have many functional units working in parallel. Medium and especially small scale CPU's have a sequential microprogrammed controller which makes them easier to implement but slower in execution. This problem is inherent in all processor controlled monitors. If the control processor is not especially designed for this application, the solution can only be found in the sensory system itself and in alternating or rotating data buffers.

The main bottleneck of monitors lies in the transmission of data between the sensory system and the control processor. This is why most hardware monitors perform some preliminary data reduction with combinatorial logic. This measure is still insufficient for systems which produce events at an

cessive rate. For this reason it is desirable to have a set of high speed registers in the sensory system which can be used as buffers when data bursts arrive at the input. If this is still insufficient there is only one way out of it, namely to interrupt the host system until the monitor has caught up. The interrupt should be directed to the software monitor which can inhibit any processor activity until it gets the signal to release the CPU over the control/host communication channel. At installations where this cannot be tolerated, at least a data overrun indication is recorded along with the data.

A second speed problem can occur at the output channel when data is recorded on mass storage. However, the situation becomes only serious when the monitor is running in store mode where every event is recorded without any data reducing transformation. The monitor speed would then be limited by the speed of the recording device. In all other modes this problem is not very likely to occur as first and second level data reduction as well as buffering techniques should decrease the data rate so that it can be handled easily.

The memory requirement stated in the third point is due to several considerations. First, memory has to hold the decision and evaluation software. Second, it has to provide enough space for buffer zones and third, it has to have room for the E-Map, T-MAP or STORE modes. Some of the information that reaches the monitor does not have to be processed immediately. In this case the operation speed can be accelerated when the processor and its I/O channels are bypassed and the data is stored via direct memory access.

(DMA).

Apart from managing the data flow from the monitor units the control processor has several other tasks. It has to perform second level data reduction and on-line evaluation and present the results mostly in statistical form to the user. CRT displays or line printers can be used as output devices. At the same time a more detailed record of system events has to be buffered in the control memory to be dumped periodically on a mass storage device, e.g. a magnetic tape.

Finally the processor has to accept commands from a keyboard. This enables the user to set the monitoring mode, the display mode, and other parameters to specify the operations of the whole performance measurement system. A desirable feature would be to have not only a manufacturer supplied set of software routines but a "monitoring operating system" which incorporates the basic tasks of data acquisition. In the CPM-X monitor [34], the most frequently used routines for data reduction are programmed in firmware, which again helps to increase the processing speed of the CPU. The user should have the possibility to write his own evaluation software on top of the utility routines. A considerable amount of flexibility would be added to the system and programs to track down special problems or to modify the evaluation techniques could be written according to individual requirements.

3.2 Application of the System

The interactive nature of this system offers a range of new applications. The most difficult part of a monitoring session is to set up the probe points, define the logic combinations in the sensory system and to specify the events to be intercepted by the software monitor. Finally the secondary data reduction procedure in the control processor has to be chosen. Experience has shown that the first setup never exactly gives the desired information. Several test and correction cycles have to be carried out before the result is satisfactory. With the monitoring system developed in this chapter, the adjustments can be done interactively from the monitor's keyboard.

Let us consider a typical example. During system profile measurements a significant operating system overhead is observed in one of the utility programs. Without relocating probe points, or inserting new hooks in the software, the monitor can supply the identification of the troublesome routine as soon as it is loaded from disk to core by associating the physical disk address with the name of the accessed module, assuming that the system device directory is available for the monitor. Knowing the size of the identified routine a sampling run can be set up to observe PC activity for the corresponding core segment. The start of the sampling session can be defined as the event of loading the routine the next time into core. The resulting execution profile will then show which parts of the routine are responsible for the low performance. Commands for this

tracing procedure can be given in a simple language (possibly similar to BASIC) and the complete process can be supervised from the monitor's console.

The centralized control over the measurement system also enables non specialists to handle the monitor. Operators can ask for continuous feedback for their decisions at the host system console and can immediately see if the system load is optimal. The real time display showing the different system activities is a valuable tool for teaching purposes. The pedagogical value of a dynamic display is obviously better than static explanations on the blackboard.

Finally the interactive monitor is an efficient tool for system development and research. In the experimental computing environment the host system can be interrupted or slowed down. While events have to be otherwise captured "on the fly" and the results are displayed in summary form or evaluated offline, in this application a detailed online analysis is possible. The monitor can be regarded as a sophisticated debugging routine. The hardware probes allow an instruction trace much faster than any conventional trace routine. If the monitor has the ability to alter the state of the host system, e.g. changing the PC, stack pointers etc., all the requirements for a powerful debugging tool are met.

CHAPTER 4

HIMOS - Hybrid Interactive Monitor System4.1 Purpose of HIMOS

One of the initial objectives of the design of a monitoring system for the mini computer installation in the School of Computer Science at McGill University was to provide a method to increase the availability of the computers. It was planned to develop a technique for automatic loading and execution of diagnostic programs as soon as a system failure was detected. During the analysis of the problem the idea was abandoned for several reasons. First it turned out that monitoring was a prerequisite to accomplish the original goal. Although there was a multitude of literature on computer system instrumentation, the subject seemed promising for further research. Second it was found that problems other than availability, yet related to monitoring, were more pressing. At the same time the project offered the possibility to test the real time capability of the mini computer used to control the monitoring process.

The resulting objective was to design an interactive hybrid monitor, controlled by a dedicated processor as outlined in figure A.1. Because the monitored system was underutilized most of the time, the improvement of performance characteristics was not one of the prime considerations although with the increasing workload, this may become an

important point in the future. But, as mentioned before, monitors can be used in many other applications. During the last year mainly three directions emerged for research on the mini computer installation:

1. Multiprocessor systems: This subject is specially attractive as there are already two mainframes available in the department. In the long run it is planned to extend the system by several micro computers to build a network for research purposes which could be supervised by the monitor.
2. Operating systems: Apart from the system software required for point one, there are projects on paging algorithms and task scheduling routines in progress. Recently two new time sharing systems (UNIX [36] and concurrent PASCAL [37]) were acquired and the monitor should be of help in understanding and extending those systems which are not very well documented.
3. Programming languages: This field offers a wide range of monitor applications. It is planned that one of the projects uses the monitor to produce flowcharts dynamically according to the real execution. This topic is closely related to the problem of program correctness proofs for which the monitor offers some practical possibilities (see ch. 5).

These three points can only give a rough overview of the possible applications. One side effect of the monitoring system for example showed up during the development of the monitor itself. The currently used operating system, RT-11 (supplied by Digital Equipment [38]), employs several

techniques which were not described in the accompanying manuals. Already the very first version of the monitor detected several unknown scheduling techniques and the knowledge of their existence induced new implementation ideas.

Finally the monitor will assist in teaching several hardware and software courses. For a course in introduction to computer architecture, hardware probes can be connected to the host system and dynamic changes of the machine state can be demonstrated under reduced execution speed on the graphic display. For students in software oriented courses, the real time creation of the execution profile for a sample program will aid in understanding the relation between static and dynamic program structures. The computer will no longer appear as the "mystic black box" and terms like program counter or interrupt will become more realistic once they are visualized.

4.2 Computing Environment

4.2.1 System Configuration

The computing facilities in the School of Computer Science are subject to continuous improvements in soft and hardware. Therefore references to the system configuration are as of March 1976.

The complete computing equipment was manufactured by Digital Equipment Corporation (D.E.C.). There are mainly two independent systems. One is based on a PDP 11/20 processor with 28 * K words of core memory, one 2.5 Megabyte

disk drive, two 288 Kilobyte DEC-tape drives and a Tektronix 4012 graphic display which serves as a console device. This installation is used as the control system for HIMOS.

The host system is built around a PDP 11/45 CPU with 40 K words of core memory, a memory management unit, one floating point processor, one 2.5 Megabyte disk drive and two system consoles consisting of a 300 baud hardcopy terminal (DEC-Writer) and a 1200 baud video display (Beehive).

The two systems are physically located close together. They are connected via two communication channels. One consists of two interconnected serial asynchronous interfaces operating at approximately 10 Kilobaud; the second link operates by means of two parallel asynchronous 16 bit interfaces at an average transmission rate of 40,000 words per second. A third parallel interface establishes the communication between the PDP 11/20 and the hardware monitor. All interfaces were originally designed by DEC but were modified to fit the special needs for high reliability and increased data transfer rates.

The complete system configuration is shown in the appendix, figure 1.2.

4.2.2 PDP 11 Family

In order to fully understand some of the monitoring techniques applied in HIMOS, it is necessary to have a basic knowledge of the PDP 11 system architecture. This paragraph will only highlight the features which are relevant to monitor implementation, especially with regard to the PDP 11/45 structure as this computer was chosen for the host.

system. Further details about the PDP 11 structure, the corresponding processor handbooks should be consulted ([39] and [40]). A detailed description of peripherals and interfaces can be found in [41].

The PDP 11/45 is a 16 bit parallel processor which can run in kernel, supervisor or user mode. It can perform DMA data transfer as well as CPU controlled interrupt or flag driven I/O. The interrupt system has a 4 level priority scheme and the CPU can be on one of 8 different priority levels. The 16 general purpose registers (GPR's) are functionally divided into two sets of 6 registers each, 3 stackpointers (SP), each for one of the three different operating modes and the program counter (PC). The address space ranges from 0 to 32 K words and can be extended up to 128 K words under memory management. The upper 4 K of address space are reserved for I/O devices and the lower 256 words are used for interrupt vectors. The CPU interprets 78 instructions which can be used in 12 different addressing modes.

One of the most important features of the PDP 11 design is the UNIBUS concept: All system components and peripherals are connected to a single bidirectional asynchronous bus, called the UNIBUS. Since all system elements, including the CPU, communicate with each other in identical fashion via the UNIBUS, no distinction can be made between memory access or input/output operations. Although this technique facilitates programming it caused some problems for the monitor implementation.

The HIMOS intercept technique is based on the interrupt mechanism of PDP 11 computers. Interrupts can be caused by

peripheral devices or the CPU itself. A hardware interrupt occurs when a device wishes to indicate that a specific condition has occurred. The relative priority of the request is determined by the processor's priority and the level at which the request is made. If the device's priority is higher than the current processor level the following actions take place:

1. The processor relinquishes control of the bus passing it over to the requesting device.
2. The device sends a unique memory address as base of the interrupt vector. The first word of the vector contains a pointer to the interrupt service routine, while the second location holds the new processor status word (PS).
3. The CPU stores the current PS and PC in temporary registers.
4. The new PC and PS are taken from the interrupt vector. The old PS and PC are pushed in that order onto the current stack and the service routine is initiated.

Upon the RTI command (return from interrupt) these actions are executed in the reverse order.

The following commands in the PDP 11 instruction set can cause an interrupt sequence:

BPT, IOT (Breakpoint and I/O traps):

The first command is used for debugging techniques where breakpoints can be created by substituting the original instruction by the BPT code. IOT can be used to schedule I/O actions.

EMT, TRAP (Emulator trap and trap):

Those two instructions are used for several dispatching techniques. The high byte contains the operation code while the low byte contains a user defined constant in the range from 0 to 377 (octal). In RT-11 the EMT instruction is used as supervisor call.

PIRQ (Programmed interrupt request):

This instruction offers another way for task dispatching. The request is treated in a similar way as device interrupts because the priority level can be specified.

Finally there are 3 important vector locations reserved for processor fault conditions. As soon as one of the conditions occurs, the processor traps to the corresponding vector.

Trap to 4:

Most novice programmers are confronted with this error condition. It indicates the processor "time out" signal. The reasons can be access to nonexisting memory or device locations and odd address in a word instruction.

Trap to 10:

The processor has encountered an illegal operation code. This situation is typical for attempts to execute data instead of program code.

Trap to 24:

Whenever the power drops beyond a certain limit the processor traps to this location to initialize the power fail routine. When power is restored a trap to

the same location will start the power-up routine.

() 4.2.3 The RT-11 Operating System

Originally it was intended to monitor the PDP 11/45 under the UNIX time sharing system. However, for technical reasons the UNIX system generation was delayed. At the beginning of 1976 the implementation of HIMOS was started under RT-11 (Version 02B-SJ) which is, at this time, the only available operating system.

RT-11 is a single user operating system for computers of the PDP 11 series. On the PDP 11/45 and 11/70 the CPU is permanently kept in kernel mode while executing RT-11 or user tasks scheduled by the system. It requires a minimum of 8 K words of core and can handle a maximum of 32 K words address space. It is designed for program development and real time applications. It supports PAL-11 and MACRO, the PDP 11 assembler languages, FORTRAN IV and BASIC. Several utility programs are available such as the text editor (EDIT), and on line debugging aid (ODT), a file handler (PIP), several device handlers and a batch utility. It can accept device interrupts and service the two most important error traps (trap to 4 and 10).

In the following some of the aspects of RT-11 which are important for monitoring will be discussed. Further information can be obtained from the manuals [38, 42].

When RT-11 is booted it determines the physically available core (the maximum for RT-11 is 28 K words) and loads itself on top of the memory. The resident system part needs approximately 4 K words. The trap vectors and the most

important device vectors are then initialized. When device handlers are brought into core, RT-11 locates them just below the system. Normally, user programs are loaded at address 1000 (this and following addresses and memory values are given in octal if not stated otherwise). The resulting memory layout is given in figure 4.1.

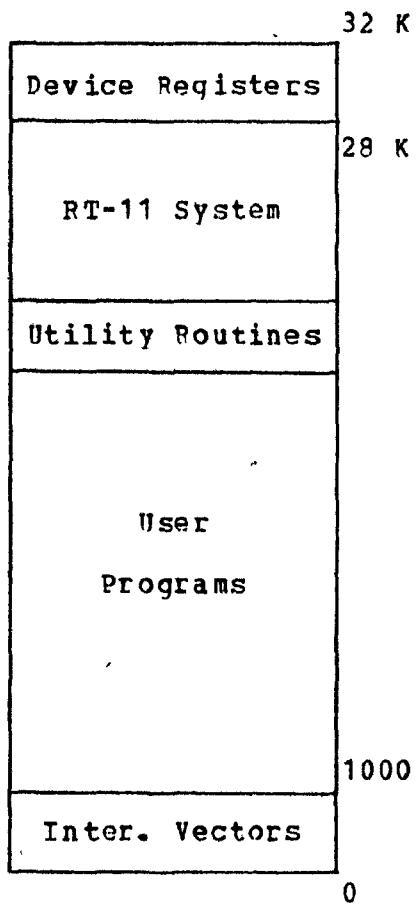


Figure 4.1: Memory Layout under RT-11

An executable program image is called a SAV-module. It always represents core locations from zero to the high limit of the code. This enables a programmer to define certain vector values statically in his program. To make sure that no vital system vectors are erased when a user program is

loaded, the system resets some vectors after a program load. The vectors to be restored are indicated in a protection table within the system. This technique is obviously not the most elegant way of system protection. On the other hand, RT-11 cannot take advantage of a hardware memory protection as this is not a standard item and is only supplied with the memory management unit. Therefore RT-11 can only protect itself at program load time and also against keyboard commands from the console (like Examine or Deposit). This is not the case during run time. A user program has access to any existing address within 32-K. The subject of memory protection has considerably influenced the implementation of HIMOS.

The communication between the operating system and a user program as well as internal RT-11 scheduling is performed via EMT-calls. The use of the EMT instruction is therefore exclusively dedicated to system actions. A large macro library contains all system utility routines, for example, READ and WRITE requests. The macros use EMT-calls to transmit a command via software interrupts to RT-11. For example the EXIT macro call at the dynamic end of a program is translated into an "EMT 350" instruction where the number 350 serves as a function code for RT-11.

Disk and tape storage is blocked into records of 256 (decimal) words. On RK05 cartridge disks this corresponds to one sector. At the beginning of a tape or disk a file directory is located. It contains starting address and lengths of the files on the device. Files are stored sequentially but after several file manipulations there may

be gaps between individual files.

RT-11 has no file protection. Each user can access any information on a device. Only the directory is protected, provided system macros for file manipulation are used.

4.3 Concept of HIMOS

The HIMOS system was specially developed for the system configuration described above. However it can be used to monitor any other computer within the PDP 11 family, provided a second CPU for the control system is available. System dependency is introduced by the software monitor which is designed to operate under RT-11. The hardware monitor part is more flexible although some of its logic has to meet special requirements of the PDP 11/45 architecture.

The PDP 11/45 was chosen to be the host system which is monitored under control of the 11/20. This choice is due to the fact that the bigger 11/45 has more components of interest such as the floating point processor and the memory management unit. Originally it was planned to execute the control software on the recently announced LSI-11 micro computer (manufactured by DEC) but it was not available on time. However, the control program can easily be transferred at any time since the instruction set is compatible.

HIMOS was implemented in three steps. A first version of the software monitor allowed some initial experiments to become familiar with various problems. This version ran like the early software monitors on the host system which was used at the same time to analyze events and to output

the results. Second, the hardware monitor was designed and third the control system was implemented on the 11/20. This approach led to a modular design of the instrumentation system. Each monitor can operate on its own. Only the supervisor CPU is necessary to receive information and to control the operating modes.

4.3.1 Software Monitor Functions

The software monitor (S-MON) is core resident in the host system where it is protected by RT-11. When a specified event occurs it is captured by S-MON which accumulates pertinent information in a buffer before transmitting the complete event record to the control system (CS). The event record is headed by the event code (EC) and can virtually contain an unlimited number of additional words indicating the state of the host system at the time of the event. In a commercial environment S-MON would release the CPU after having gathered the information and would transfer the record concurrently with the continued execution of the interrupted task. In HIMOS however, the record is transmitted and a response from the control system has to be received before S-MON releases the CPU. Although this technique increases the monitor overhead, it is necessary to allow interactive response from the supervisor. If a special event is detected in the control system, the monitor mode may be changed, the hardware monitor initialized etc, before the host system changes its state. This feature opens a wide field of applications for HIMOS which are not possible in most other monitor

implementations. Any hard or software event may be dynamically declared as a special event. The list of these EC's is kept in the control system.

From its design the software monitor uses exclusively the intercept technique. As will be shown later, even the sampling mode is implemented using the same technique. At initialization time the vectors for all interrupts to be recorded are replaced by pointers into the monitor program. The original vector values are saved in S-MON. The choice of the vectors can be interpreted as the first level of data reduction (as a matter of fact it is data elimination). At the same time a list of items has to be specified which are to be recorded upon the occurrence of an event. Every individual event can have its own set containing items of interest. This gives the second level of data reduction.

At this point it is helpful to follow an event through the software monitor (see fig. 4.2). Let us assume "trap to 10" is specified as an event. As soon as the CPU encounters an illegal instruction code, the execution flow is interrupted and control is passed to the location pointed at by memory address 10. As a result the PC will contain the entry point of S-MON. The event code is computed and used in the main dispatcher as an index to call the corresponding event handler (EH). There, the system state, according to a specification list, is stored into a buffer and the complete record is sent to the supervisor system. Assuming that the event analysis did not indicate a special event, the supervisor simply sends an acknowledgement and S-MON will transfer control back to RT-11, as indicated by the original

contents of the interrupt vector.

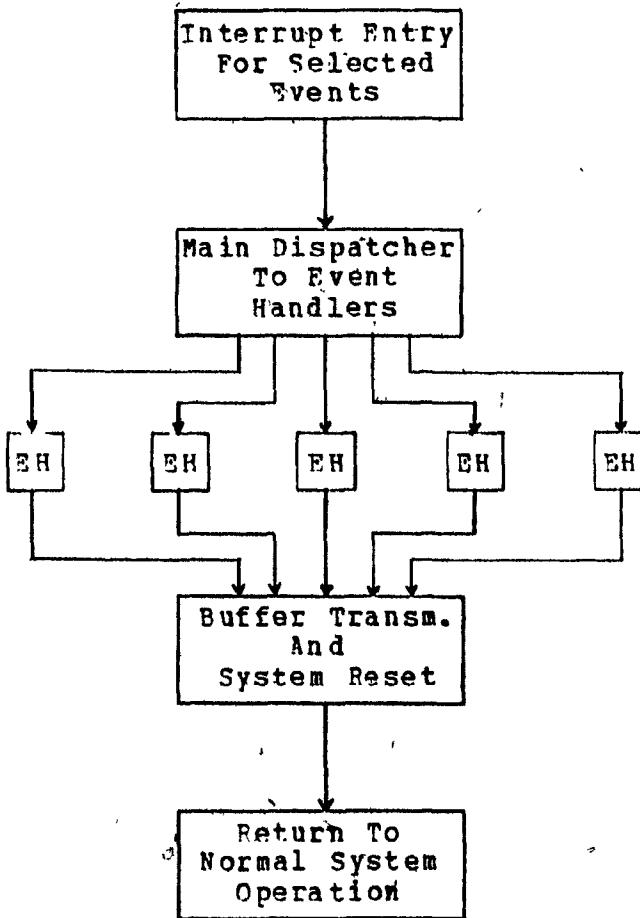


Figure 4.2: Functional Diagram of S-MON

The procedure is completely transparent to the user and to RT-11, as long as the event is acknowledged by the control system. If a special event was detected the control CPU has the possibility to change the system state in the host in which case HIMOS interferes activly with the host performance.

As mentioned before, the sampling mode is handled in a similar way: the 11/45 clock interrupt is intercepted and the event is reported to the supervisor. To transfer

control back to the point where a task was interrupted the necessary information is taken from the system stack. This solution offers the possibility to combine interrupt and sampling techniques during the same monitor session. For example device and CPU activity can be monitored while every second a sample interrupt is created. This can be used to monitor if the system is still in working order or if, for example, the CPU was stopped by a HALT instruction.

4.3.2 Hardware Monitor Design

The design of a hardware device to monitor PDP 11 computers requires some special considerations. Mainly the way how I/O activity is handled causes practical problems. Any I/O operation is performed on the UNIBUS and except for interrupts it cannot be distinguished from a regular memory access. Further difficulties are due to the fact that there are not many meaningful probe points available at the CPU backplane. To monitor, for example, the PS or PC requires complex and dangerous manipulation on the CPU boards. It is desirable that the computer design for next generation systems take that problem into account and bring out sufficient probe points for easy access. However some of the important signals in PDP 11 CPU's are brought to a plug which is used for maintenance purposes. This has simplified access to a subset of important probe points.

A general design of the hardware monitor (H-MON) was given to the Department of Electrical Engineering at McGill where it should have been implemented as part of a course project. Due to problems with the delivery of components the

implementation has not been possible so far. Based on a detailed design together with the engineering drawings, the function of the device will be discussed in a later chapter. Possible applications of the hardware monitor will be considered although results of practical experiments are not available.

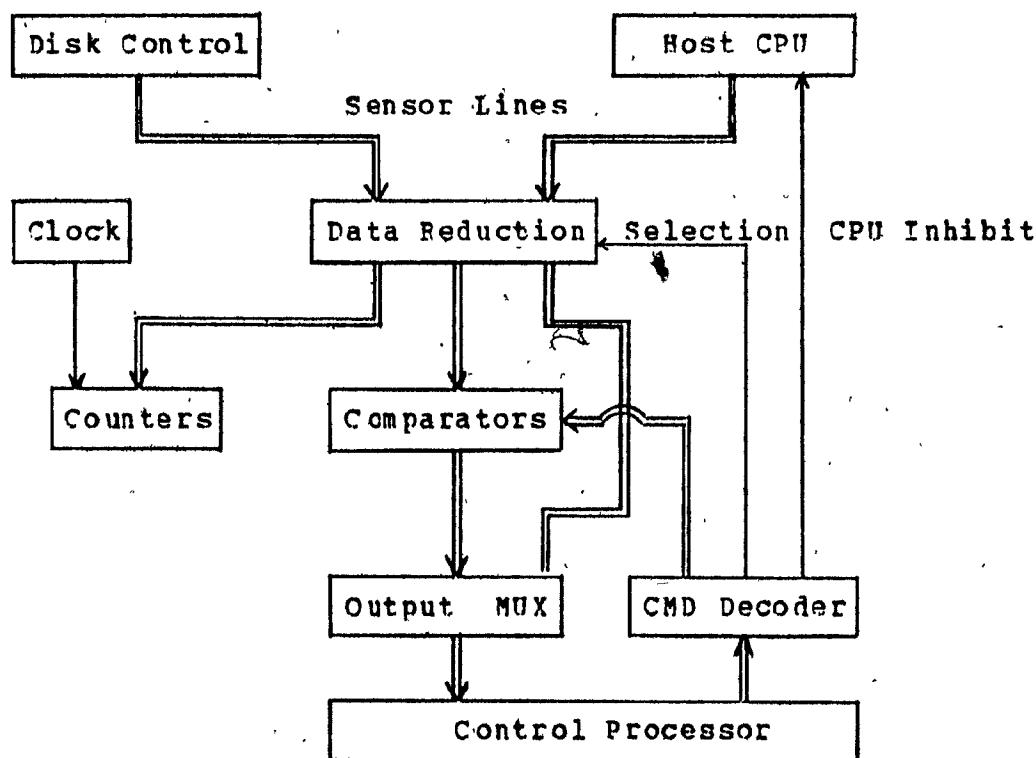


Figure 4.3: Hardware Monitor

According to the initial design, the hardware monitor has several groups of sensors which can be connected to probe points of the host CPU and the disk controller (see fig. 4.3). The signals are then supplied to a data reduction logic which is controlled by the supervisor system. Hardware counters can accumulate signals at high speed or they can be used to time events with the internal frequency

generator. The device operates in different modes which can be changed dynamically by the control system. Results are transmitted over a modified parallel interface for further processing.

4.3.3 Monitor Control and Output

The supervisor system, implemented on the PDP 11/20, has complete control over all monitoring actions. Its command interpreter accepts a large set of instructions which can be grouped into three parts:

- a. Display and recording mode
- b. S-MON control
- c. H-MON control.

(Any references to software features for the control of the hardware monitor imply that the relevant task entries exist in the supervisor system, but the corresponding code has been replaced by a NOP instruction.) To facilitate the definition of a monitoring session, command (CMD) files for each of the three groups can be created for repeated use.

The control system (CS) can interrupt and redefine the operation of S-MON and H-MON at any time either as a function of received data or according to a keyboard command. It analyses event records and stores them by means of an alternating buffering mechanism. Buffers can periodically be dumped on tape or disk. At the same time the CS displays the events in two different ways. For detailed information the complete record for every event is written out in numeric form. As this happens in real time and because the transmission to the terminal operates at

2,400 baud, the host activity has to be slowed down according to the event density and the number of items to be listed per event. In the graphic display mode where the occurrence of an event updates a histogram in real time, the monitor overhead is practically limited by the record transmission between the host and the CS.

Further tasks of the CS are to maintain the system time relative to the monitor initialization and to start and stop the monitor session in a remote way.

It may be instructive to follow up the example of an event occurrence given in section 4.3.1 with regard to the supervisor system (see fig. 4.4). As soon as the event record is received at the S-MON interface it passes through the event filter. The event code (EC) is compared to the list of special events. If the list is empty or if the EC does not match, the filter will send an acknowledgement to S-MON to release the host CPU. The system control will then direct the record to the output handler if real time output is specified. Otherwise the CS operation is finished. A buffer overflow is automatically resolved in the receiver program by switching the buffers and the filled buffer is recorded on mass storage at a later time when the CS is idle. If numerical or graphical display was specified the output handler will perform the necessary data transformation.

In case the event filter finds the EC in its list, the special event sequence is invoked. The display will give a numeric output of the event record (no matter in which mode it was running) and indicate that this is a special event.

During that time the host is suspended and S-MON is in receiving mode, waiting for further instructions, the operator can react in different ways. He may release the host immediately and thus terminate the special event sequence. He also can change the H-MON or S-MON mode according to new requirements for the succeeding analysis, or he decides to terminate the monitor session.

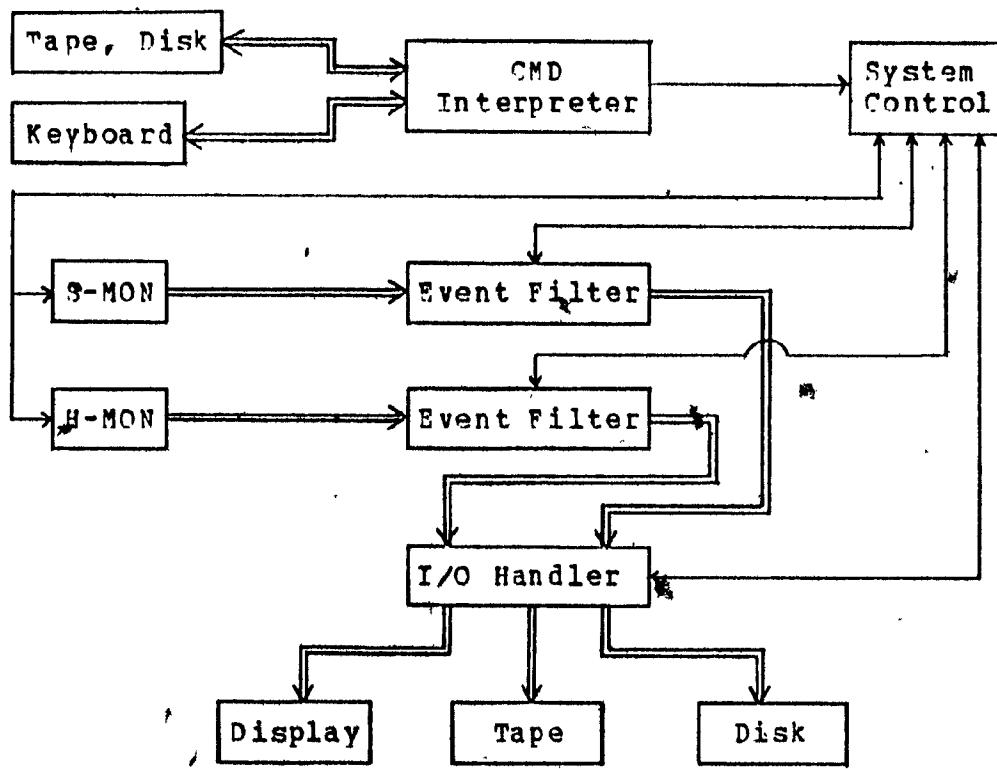


Figure 4.4: Monitor Control System

Other possibilities are left open for future extensions. As the receiving program in S-MON is a flexible, command code driven dispatching routine, other commands to S-MON like "examine location X" or "change value of X to Y" may be added.

4.4 Monitor Implementation

The two chapters on the soft and hardware implementation of HIMOS will give a comprehensive description. Further details on the software can be found in appendix B which contains the complete source listings. Appendix C gives a documentation of the hardware monitor and the communication link.

4.4.1 Software Monitor (S-MON)

S-MON is coded in PDP 11 MACRO assembler and consists of one load module of approximately 2 K words. In order to make S-MON core resident and protect it against user program as well as RT-11 access, the operating system bootstrap had to be modified. The idea is to load the executive not completely on top of the existing memory space but to leave some room for S-MON right above RT-11. In the current configuration RT-11 is located below 24 K. As a result RT-11 assumes that 24 K is the physical limit of available core and will not access higher locations. Furthermore it will abort attempts to modify the top area from the system console. A description of how to change the bootstrap can be found in the software support manual [42].

Another system modification was necessary to preserve the communication channel for the control system. As mentioned earlier, RT-11 loads every executable program starting from physical location 0 and resets afterwards important vector locations between 0 and 1,000. The restoring is performed in accordance with the system protection map. This map is

dynamically changed by S-MON as soon as the monitor is started. The following vectors are protected:

trap vector, loc. 34

clock vector, loc. 104

communication link vector, loc. 450.

User programs are usually terminated by transferring control back to the operating system with the EXIT macro call (EMT 350). If register 0 is cleared at this moment, RT-11 will execute a RESET instruction which disables all interrupts before reenabling the vital interrupts for the system. This however would harm the monitor operations because first, S-MON cannot receive supervisor commands any more and second, if it is in sampling mode, the clock interrupts would be turned off and the timer registers would be reset to 0. For these reasons, S-MON changes the RESET instruction in RT-11 to a NOP. This modification does not distort the performance of RT-11 but it insures full protection for the monitor activities.

4.4.1.1. Event_and_Data_Selection

Software events are defined as interrupts which are intercepted by S-MON. A total of 32 events can be specified which is enough to cover all possible interrupts in the PDP 11/45. At initialization time, S-MON exchanges the content of an interrupt vector with a new PC and PS, and saves the original vector in a monitor table (VECSAV). To identify an interrupt, an event code (EC) is assigned to it. A convenient place for the identification was found in the condition code which resides in the 4 least significant bits

of the PS. As we have 32 possible EC's and only 16 can be specified using the condition code, two different interrupt entries were created in S-MON. This means that the new PC for events in group 0 points to ENTRY0 in S-MON and the PC for group 1 points to ENTRY1 (fig. 4.5). Each group can accept a maximum of 16 different interrupts. The EC is then defined as group index times 16 plus the interrupt index given in PS. This gives a total range of 0 - 37 in octal. Table A.4 in appendix A lists the event codes with the corresponding interrupt and vector locations.

Two mask words (MASK0, MASK1) are used to specify which of the 32 interrupts are to be captured. For example, if bit 3 in MASK1 is set, event 23 will be activated. To define a monitoring session, the mask words can be specified either at the host console when S-MON is started or interactively from the control system. If the command sequence at the beginning of S-MON is skipped, a default configuration will be assumed in which traps to location 4 and 10 (EC 1 and 2) are intercepted.

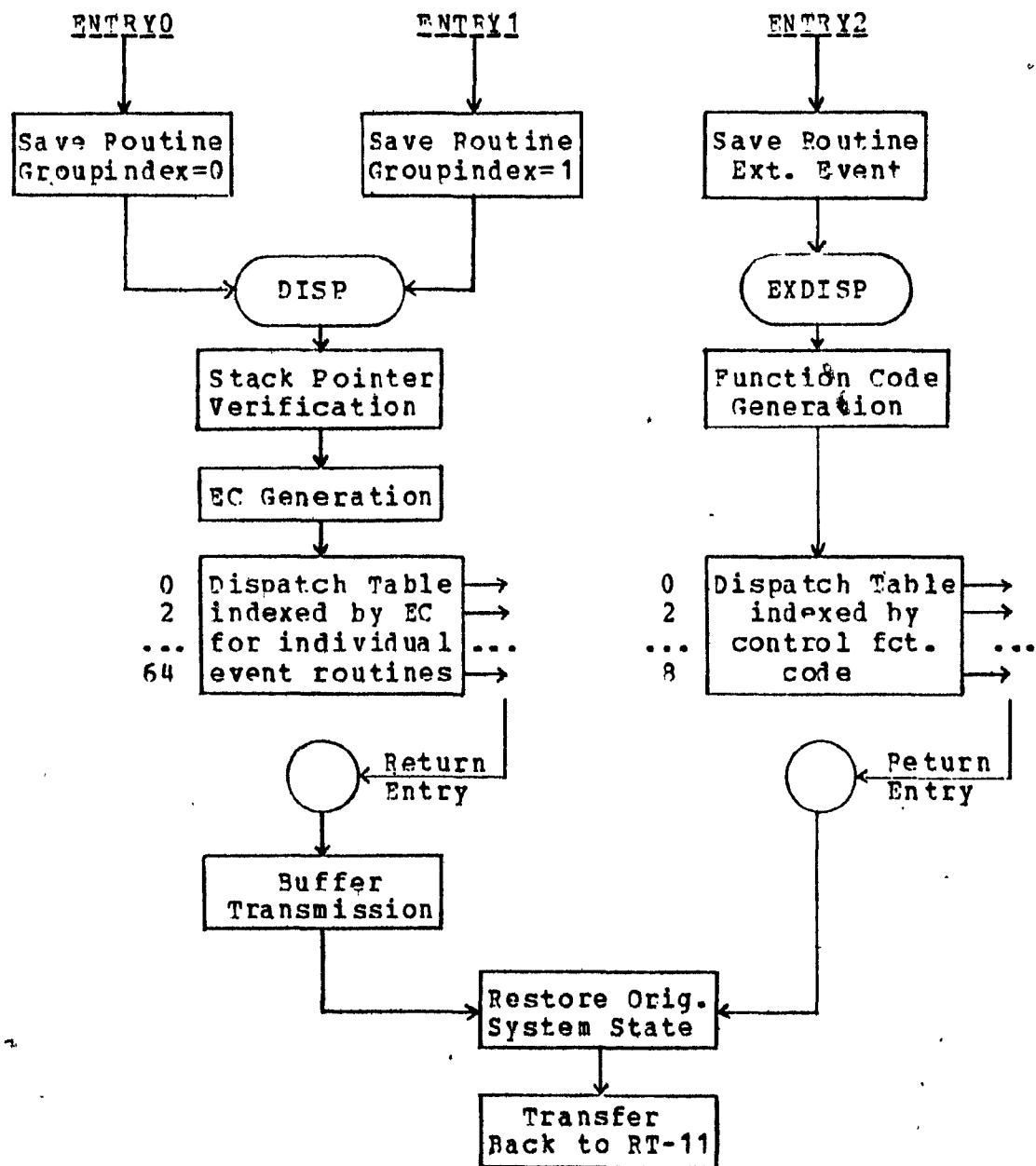


Figure 4.5: Core Resident Part of S-MON.

When an event arrives, the monitor creates a so called event record which contains information about the system state at the time of the interrupt. For every event, different system variables may be of interest and the monitor overhead would be increased considerably if all possible variables were recorded each time. Therefore S-MON

offers the possibility to define individual event records to meet the information requirements for every event. The desired record for each event is defined in the submask (SM) words. The minimum record for all events contains the three most important system parameters, i.e. the PC, PS, and SP. Most events can report additional values such as register content, buffer contents and RT-11 parameters. The exact assignment for the submasks is given in table A.5. For example, SMO is responsible for the records of event 1 to 5. The low byte covers T4, T10, and the first two values of BPT, the high byte gives the last BPT bit and specifies the records for IOT and power fail. A value is included in the record when the corresponding bit is set.

More information can be reported for the EMT's. As this is a one word instruction [PC-2], the contents of the program counter before it was incremented will be the EMT code along with the function code which serves to distinguish 256 different FMT calls. For example, "104013" shows that an EMT 13 was executed. Because the EMT is used as a supervisor call in RT-11, the error code (ERC) can give valuable information.

The submasks SM2 to SM6 correspond to events in group 1 which are device interrupts. Depending on the device, register and buffer content can be included in the event report. The matching register addresses are contained in the device table of S-MON which is indexed by the EC.

The most important device is the RK-11 disk controller. SM6 is fully dedicated to define the event record for the RK-11 interrupt. It contains the basic processor

information plus the content of 5 disk registers (the register assignment is given in [41]). R3 which originally contained the word count was redefined. This can be justified because normally the word count is 0 when an interrupt occurs. It now contains the block number of the accessed file on the disk which can be obtained by transforming the physical disk address in R5. In the new representation, the disk address can immediately be used to refer to the directory dump where the relevant file name can be found.

Some events like EMT's and disk interrupts occur very frequently and it is desirable to perform preliminary data reduction on the host system before reporting the events to the supervisor. This eliminates unnecessary transmission time and decreases the input load at the control system. The submasks SM1 through SM6 contain one additional bit (bit 0 in each byte) for every event to indicate a preselection. If the bit is set, S-MON will examine one of the values in the event record and compare it to the content of a list of values, the so called select words. If the EC is found the event will be reported; otherwise it is ignored. As shown in table A.5, select words 0 to 3 can hold up to 7 FMT function codes (a function code can be specified in one byte). The end of the table has to be marked by a 0 entry. Select words 4 - 7 are used for TRAP codes. If no trap codes are specified the list can be used for another 7 EMT codes if necessary. The selection for disk events is kept as flexible as possible. Each item in the list specifies first the register number and second the value to be

compared. Thus, the criterion to report a disk event can, for example, be the disk error word or the physical address. TRAP or EMT codes can be extended over select words 11 - 20 if no disk selection is specified. This gives a maximum of 31 FMT codes or 23 TRAP codes which can be listed.

Every event record is headed by the corresponding event code. If specified, the content of the high speed clock buffer can be appended as the last transmitted value. This is important when program segments are to be timed.

All tables in the S-MON data structure are indexed by an even multiple of the EC. In conjunction with the masking technique, this has considerably helped to keep the execution time within reasonable limits.

4.4.1.2 S-MON ROUTINES

When the software monitor is started, it will print an identification on the system console and enter the command interpreter. This routine is responsible for the event and record definition. The execution is controlled by 4 dispatch tables which makes the program fast and easy to understand. The command interpreter (CMDI) is used to define the two mask and the seven submask words and to enter values for the select words. When the index for a mask word is entered, the mask word as it was defined previously is printed and modifications can be specified in the following line. For select words, CMDI distinguishes between SM0-10 and SM11-20. The first group is updated in byte form, i.e. for every word index two new byte values are requested. The second group is word oriented. For every index the two

error checks (e.g. CRC or LSC) could be used.

The speed of the parallel link is only limited by the UNIBUS speed, interrupt latency, and time requirements for the interrupt handler. In HIMOS the transmission rate is approximately 40,000 words/sec. This allows to transmit an average event record of 20 words in 0.5 ms.

HIMOS uses a simple protocol to transmit event records and specification tables over the communication link. The host system terminates an event record by the transmission of EOT and then waits to receive an acknowledgement (ACK) from the control station. When the host tables are updated interactively from the supervisor, the host sends the old table content, terminated by ETX. After the update, the control system issues an enquiry (ENQ) signal before transmitting the new table which is again terminated by ETX. All protocol and function codes are verified in both stations. A wrong function code will dispatch an error routine to generate a corresponding message. An erroneous protocol will cause a retransmission of the last record.

H-MON uses a parallel interface, similar to the ones described above, to transmit data to the control system. For this application, a DMA-channel would provide much better results but the corresponding interfaces were not available.

4.5 Control System Implementation

4.5.1 Program Control Structure

The control system (CS) program consists of 3 object modules: LOG, LOGIO, and LOGGRF (for listings, see appendix B.2). LOG is the main program and the other two modules contain basic I/O routines and subroutines for graphic display on the Tektronix terminal, respectively. To execute the CS program, the three object decks are linked together and loaded at starting address 1000.

After initialization of system parameters and interrupt vectors (S-MON, H-MON, clock), LOG enters the main dispatcher at WAITLP. This is the busy wait state in which the system waits for interrupts and schedules various tasks. During execution of this loop, the program examines the content of a dispatch word (DISPWD) and if one or more bits are set, the corresponding tasks are called (see fig. 4.6). Every time an event record is received, up to 3 bits in the dispatch word can be set in the event record processor (FILTER):

- bit 1: record buffer
- bit 2: print event record on terminal
- bit 3: update graphic output.

The corresponding programs are discussed in chapter 4.5.4. Each of these routines will clear its own dispatch bit before returning control to the wait loop. The S-MON interrupt service routine (RCVREC) sets bit 0 in DISPWD to

schedule FILTER.

The second possibility to leave the loop is given by the reception of a command from the keyboard. This event transfers control to the system command interpreter (SYSCMD) which will analyze the command and schedule the according subroutine. Timer interrupts are directed to the line clock handler (LCLK) where the system time is updated.

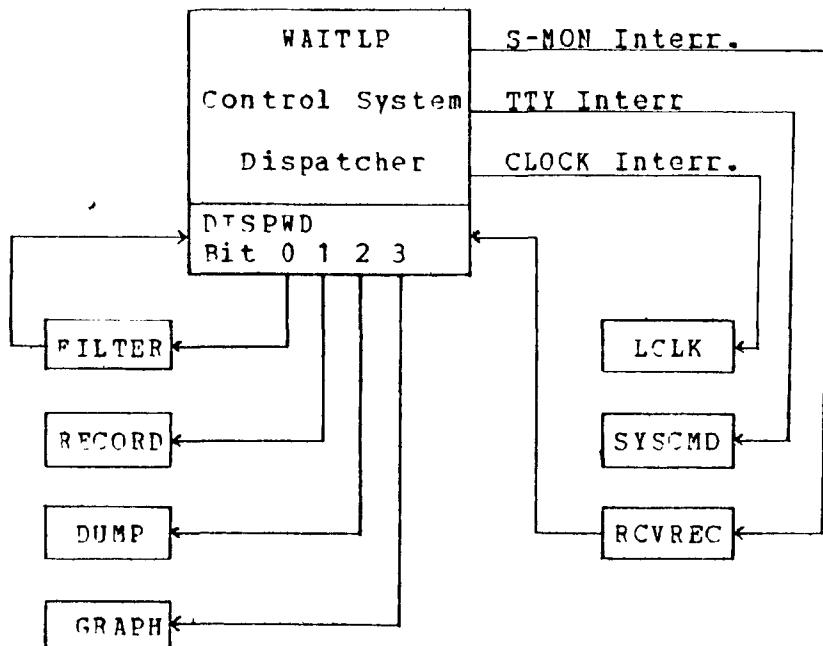


Figure 4.6: Control System Dispatcher

The centralized dispatching technique has helped to keep the program structure modular and easy to follow up. This is especially important in a system where different interrupts can occur at unpredictable times. Further program extensions can be introduced via unused bits in DISPWD without affecting the control structure.

LOG handles three input/output files:

Command File (SPC)

Table File (TAB)

Logging File (LOG).

Default extensions for file names are given in brackets. The command file contains all necessary specifications to define the supervisor system mode. It is created by the system command interpreter which accepts specifications either from the keyboard or from a previously generated command file. The table file is used in a similar way and keeps information regarding the host system mode, i.e. which interrupts are to be intercepted and what information is to be reported for every event. Both files help to simplify the use of HIMOS. Different monitoring sessions can be predefined to standardize frequently used operating modes. To invoke one of those sessions, the operator has only to know a small part of the full instruction set.

The logging file contains the event records as they were received from S-MON. A program (LOGPRT) was written to print this file in a readable form on line printer or data terminals. For performance evaluation which implies a statistical analysis of this file, other programs can be written according to the individual requirements. All HIMOS files can be stored on tape or disk units of the control system.

4.5.2 Command Interpreter and Operating Modes

The control system has three operating modes which specify the form of the event record output. For a detailed online analysis, the records can be displayed in numerical

form at the terminal. The record is headed by the EC and all following values are preceded by a two letter identification, explained in table A.6. Alternatively, the events can be presented in graphical form. A histogram is drawn dynamically in which a maximum of 21 different EC's can be entered along the X-axis. The Y-axis shows the number of occurrences for each event. The initial maximum on the Y-axis is set to 56. Every time one of the columns becomes too big, the picture is rescaled by factor of two. Concurrently with one of the display modes, the system can record incoming events in a logging file on tape or disk. Other display and storing features are explained below along with the corresponding control commands.

The operating mode of the control system can be defined by commands from the keyboard. The command interpreter (SYSCMD) accepts strings of virtually unlimited length but only the first character is significant to specify a command. New input is accepted in the system command mode which is indicated by an asterisk as the response character on the terminal. Commands that are given during other system activity, e.g. event analysis or output on the display, are stored for later processing. The corresponding delay is normally not significant because of the centralized dispatching technique which ensures that pending terminal input is served immediately after the last scheduled task. The first character of an input string is compared to a list of valid commands and the list index is used to dispatch the according task. If the character is not found, an error message is printed, followed by another asterisk on the next

line. In the following, the meaning of all valid system commands as they are listed in appendix A, table A.7 will be discussed. If necessary, further explanations for the corresponding operation mode are given.

W: This command suppresses graphical or numerical terminal output. Recording and counting of event information will be continued according to previous mode specifications. This feature is useful to give the operator some time to observe results on the screen before they are overwritten.

P: Graphic and numeric terminal output are resumed if they were previously suspended by the "Wait" (W) command. Output will continue with the next record after P is given.

E: Once this command is given, event reception is temporarily stopped and the user can enter a list of event codes, called special events. After termination of this input mode, CS will continue to receive events and compare every new EC to the list of special events. If the EC matches, a message announcing a special event along with the complete event record is printed. The "Wait" command is ignored in this case. Simultaneously, the host system is stopped until a "Continue" (C) is entered.

C: If the host was suspended due to a special event, this command will release execution. If the host was not disabled, an error message will be printed.

B: If graphic output was specified, the command will reset the counters of the graphic routine and a coordinate system with the initial scale for histograms will be drawn

on the Tektronix screen. It is recommended to issue this command before the graphic output mode is entered.

A: In graphic mode the screen will be erased and the histogram is drawn again with all columns as they were given before. This feature is necessary because the display cannot be erased partially. Although three quarters of the screen are reserved for command and output text, it can happen that the picture is overwritten.

D: After erasing the screen, a summary count of all events received so far in this session is displayed on the terminal.

S: The command interpreter for the host table update routine is invoked. The command structure is the same as it was described for S-MON. Any host system activity (except \$-MON) is interrupted during this procedure until the new event configuration is established.

H: The hardware monitor control word can be defined and a new H-MON mode started. This command has not been implemented so far and does not cause any actions.

L: This command is used to define the logging mode for hard and software events by means of a subcommand interpreter (CSIL). A self explanatory message will ask for further specifications. The operator has the following three possibilities:

OLD: An existing specification file can be used to define the logging mode. The corresponding file name has to be entered and, if desired, the file can be altered.

NEW: A new mode is defined from the terminal. Consequently the operator can specify if the session is to be

recorded and/or displayed in numerical or graphical form. For the recording mode an output file name has to be entered.

UPDATE: The current mode is displayed and for each item as discussed in the last case, a new specification can be entered. The possibility to open a new output file is given.

After the command sequence for one of the three possibilities, the mode specification can be saved on a new command file or in the case of "OLD" it can be rewritten in the unchanged or altered form on the original file. Upon termination of CSIL the new logging mode is active.

While processing the commands, SYSCMD suspends any logging action and in some cases it blocks host activities by disabling its S-MON interface. Although this solution interferes with the operation of the host, it was chosen to insure a well defined state of HIMOS during and after modifications of its operation mode. For commercial applications another method could have been used (e.g. resetting the host to the unmonitored state before processing any commands), but for research and development environment, the technique implemented has proven to be sufficient and necessary when the system state has to be preserved until a new mode is defined.

4.5.3 Event Record Processing

Upon reception of the first interrupt from S-MON which announces the transmission of a new event record, control is passed to the receiving routine (RCVREC). Two alternating buffers of 256 words each are available to store incoming data. A flag indicates the current input buffer and a pair of pointers delimit the last received record within one buffer. As soon as one buffer is filled, RCVREC sets bit 1 in DISPWD to schedule the buffer recording routine (RECORD) if recording mode was specified. Record and buffer output can be processed concurrently with the reception of new records.

After receiving one record RCVREC sets bit 0 in DISPWD to schedule the FILTER and returns control to the main dispatcher. The wait loop will then continue to examine the dispatch word bit by bit in a round robin fashion and invoke the corresponding tasks. If, for example, it was interrupted before processing bit 2, it will first invoke the terminal output routines to process the previous event record before calling FILTER to analyse the just received record. This technique insures that no information is lost. If more than two records arrive at the input before the previous one was processed, reception is disabled until the CS has caught up. This only happens for high event density or when one of the slow terminal output modes is specified. More than two records cannot be buffered prior to the analysis because the system would lose its capability to react in real time upon the occurrence of special events.

If the "Wait" (W) command was given, FILTER will skip the terminal output dispatcher. Otherwise bit 2 or 3 are set according to the mode specification. In case special events were defined, the event table is searched and if the EC was found, a message is printed and the numeric output routine (DUMP) is scheduled via bit 2. The acknowledgement signal to release the host is only transmitted if the event was not found in the table. Otherwise the host keeps waiting for this signal until the "Continue" command (C) is entered from the keyboard.

Finally the current system time is appended to the event record and the count table for the summary report (command D) is updated before FILTER returns control to the wait loop. To reduce the monitor overhead, only one real data reduction is performed in FILTER, namely the special event feature which is especially useful when terminal output was suppressed via the "Wait" command. In this case only the special events are reported in real time while there is still the possibility to record a detailed report of the session on tape or disk for later analysis.

The two terminal output routines DUMP and GRAPH find the record in one of the two buffers according to the pointers which were set as record delimiters in RCVREC. DUMP transforms the record into a readable form and prefixes every value by a two letter identification. Each record is printed on a new line.

Subroutines for the graphic output are found in the object module LOGGRR. The program maintains its own table (ECTAB) to count received events. Every EC which is not yet entered

in the table will display the new identification along the X-axis, print the initial column increment, and open a new table entry. Upon overflow of one of the event columns, all counts in ECTAB are divided by two and the Y-axis of the display is rescaled. The column increment per event occurrence depends on the current scaling factor.

If no detailed information about host activities is required, the graph mode provides a convenient summary report. The histogram which is updated in real time shows not only what the host is doing but also in what sequence the events happen. It is mainly used to get a first impression of the monitored process and it helps to define the monitoring session for a more detailed analysis.

CHAPTER 5

Application of HIMOS5.1 Execution Analysis under RT-11

One of the design goals of HIMOS was to develop a technique for real time and off line analysis of program execution. There are chiefly two approaches to this problem labelled the active and the passive methods. The latter one consists in the application of standard features provided by the monitor. System events such as I/O activity, executive calls, error traps, etc. can be intercepted. To obtain statistical information, the PC and other important system variables can be sampled. In both cases the target program does not need to be changed.

The active method requires certain changes in the observed program. Check points or hooks are inserted to the source code in order to emit a hook identification to the monitor when they are executed. (This method is similar to the break point technique used in debugging routines). For PDP 11 assembler programs, the TRAP instruction is used to identify a softhook. TRAP works in the same way as the EMT instruction; only it uses a different vector location. The high byte contains the operation code while the low byte holds the user defined hook identification. When, for example, TRAP 123 is executed, an interrupt to location 34 is generated and control is transferred to S-MON which will record event 7 with identification 123.

The TRAP instruction was chosen for several reasons to implement software hooks. It offers the programmer a quick and easy way to identify strategical parts of his program with a one word instruction. Once the hooks are inserted in a given routine, they can be disabled just by replacing the S-MON address in location 34 by an address containing a RTI instruction. Substituting the TRAP code by a NOP instruction eliminates the hook completely without affecting the program performance. Another low level hook technique should be mentioned in case the TRAP instruction is used for other purposes. Interrupts to S-MON can be created by an additional interface. The hook identification can then be transmitted by moving the desired code into the output buffer which is fed back in a closed loop to the interface input buffer from where S-MON can take the information.

To monitor execution of FORTRAN programs, two subroutines (INEMIT, EMIT) were written and can be linked to the main program. Both subroutines are listed in appendix B.3. EMIT finds the hook identification as the first argument of the call in the FORTRAN linkage table and uses it to form the corresponding TRAP instruction. INEMIT has to be called for initialization purposes before EMIT is invoked the first time. This is necessary because FORTRAN alters the TRAP vector for its runtime error message handler. EMIT calls should therefore only be used in fully debugged programs. Where this is not possible, the software hooks have to be implemented by means of the above mentioned alternative.

Software hooks are a valuable tool for many applications. They can be used to time execution over critical parts of a

program as will be shown in chapter 5.2.1. When they are placed on top of the executable code, they can emit a task identification for accounting purposes. If, additionally, event 6 (EMT) with subselection for EMT 350 (EXIT) is monitored, the time between the EMT call and EC 6 gives the total execution time of a job.

Under the RT-11 operating system, S-MON offers different possibilities to measure "productive" CPU time. The busy wait loop of RT-11 can be recognized by alternating calls of EMT 340 and EMT 360. Another approach is given by sampling the PC activity. With regard to CPU activity the memory can be grouped into several regions:

1000 - X	:	User program execution
X - Y	:	I/O handlers
122222 - 124154	:	RT-11 EMT handler
(if booted for 24K of core)		

The values of X and Y depend on the individual program and can be specified via system macro calls. During execution the value of Y can be found in location 50 where it is stored by RT-11 at load time.

In any case, the definition of "productive" CPU time is relative. A true wait state as it is known in other systems does not exist under RT-11. Similar problems arise when I/O time is to be determined. Sampling the I/O handler space in core is one possibility. In chapter 5.2.2 another approach is taken. Disk access time is obtained as the difference between EMT 375 and a disk interrupt. EMT 375 invokes the I/O dispatcher in RT-11 which initiates a disk action. When the disk controller has found the addressed track and

transferred the complete record as it was specified in the word count, it gives an interrupt (EC 30). It was found that the average delay between those two events is in the range of 35 - 45 ms depending on the occupied disk space. This value is in accordance with RK-11 specifications. Undoubtedly the hardware monitor will be very useful to complement these results for more detailed investigations.

Generally, several steps are necessary to monitor a given process. An initial approach is to display global execution characteristics in graphical form on the terminal. Based on this first impression, more detailed measurements can be specified and event records can be directed in numerical form to the terminal or to mass storage for off line evaluation. Figure 1.5 shows a histogram obtained during the execution of a test batch stream. Event 5 (power fail) was specified as a special event. It occurred at the end of the batch stream when the 11/45 power was turned off.

5.2 Results of two Monitoring Sessions

The following two paragraphs will give examples of monitoring sessions using the active and the passive methods of execution analysis. In both cases, the machine level representation of the programs is unknown and any observed PC values cannot be matched readily to a functional entity of the code.

5.2.1 FORTRAN_Program_Execution

A program (SAMGEN) was written to produce J random numbers in the range from 0.00 to 99.99. When the routine is entered, the value of J is requested from the terminal. In the following, the program executes J times a loop in which a random number is generated and immediately written onto disk. The random numbers are obtained from the FORTRAN function "RAN". It should be noted that the program was written to give an example for the possibilities of HIMOS and not to optimize a given problem. A listing of SAMGEN can be found in appendix B.4.

The program was executed twice, each time producing 20 samples. For the first run, SAMGEN was linked with a FORTRAN library which replaced all floating point instructions by software routines. The second time the floating point processor was used which improved the execution time but did not change other characteristics of the execution profile.

In figure A.7 the monitor output for a SAMGEN execution using the floating point processor is listed. The HIMOS command sequence to define this session on the control system is shown in figure A.8. When the command "RUN SAMGEN" is given, RT-11 executes several EMT calls to load the program into core (EMT 374, 375). The first TRAP (EC 7) identifies the EMIT call with argument 0 which can be found in the low byte of CP (content of PC). A delay of approximately 2 seconds follows, during which a message is printed and J read from the terminal. EMIT (1) and EMIT (2)

are produced before and after the first random number generation. During the following 6 EMT's the output file is opened and at EMIT (3) the first random number is written on disk. These three emitter calls appear another 10 times during the loop execution before EMIT (4) indicates the end of the program. Six EMT calls are issued to close the output file and enter it into the disk directory before EMT 350 indicates the PT-11 EXIT call.

For the first run (run A) an execution time of 234 ms (excluding terminal I/O and file handling) was calculated. The second run using FPP (run B) took 193 ms. This difference is due to the fast performance of the floating point processor but it also reflects a certain delay for the disk output. The latter factor was excluded by averaging the time intervals between EMIT (1) and EMIT (2). After subtraction of 2.36 ms per event for HIMOS overhead, the final result shows a random number generation time of 0.270 ms for run A and 0.100 ms for run B. The difference of 170 micro seconds per random number generation can be attributed to the processing time improvement for floating point operations.

5.2.2 FORTRAN Compiler Analysis

In the following example, a short FORTRAN program was compiled under several HIMOS modes to obtain insight into the RT-11 FORTRAN compiler characteristics. The test program HISTO is listed in appendix B.4. It can be used to read a file of sample values from disk and to print a distribution of these values in the form of a horizontal

histogram on the terminal. At the same time, a second file containing the values in ascending order is created.

RT-11 supports a multipass FORTRAN IV compiler. It consists of a root segment and several overlays which are dynamically loaded in core. The core resident part comprises of the root and one overlay, the system stack, device handlers, symbol table, and an internal representation of the source program. During the monitoring sessions it was discovered that the compiler uses no scratch files, only overlays are swapped between core and disk. A high level description of the compiler can be found in RT-11 manuals [52, 53].

Because no source listings of the compiler were available, the analysis was done in a top down fashion. In the first step a graphic performance profile was produced on the Tektronix screen (fig. A.6). The histogram shows five different events:

- EC 24 : Timer interrupts
- EC 20 : Terminal input
- EC 21 : Terminal output
- EC 30 : Disk interrupts
- EC 6 : RT-11 calls for file handling.

EC 21 is more than twice as high as EC 20, because every typed character is echoed together with one additional filler character. The graph gave an impression of the amount of events and their relation in time.

For the second monitor session it was decided to select only disk interrupts and to record the protocol on disk. Figure A.9 shows the corresponding HIMOS output. The first

11 events report directory access for the source file HISTO.FOR and the output file HISTO.OBJ, both located in the 4th directory segment (block 16). At system time (ST) 103.18, five blocks of compiler overlay are read in before at ST 103.24 the source program is loaded from disk address (R3) 6531. (All file references were confirmed by comparison with the directory listing). After having read two more overlays, the compiler writes the first block of object code at ST 103.50 on disk. The content of R4 (bus address register) shows that the compiler uses always the same buffer at location 10520 to store one block of produced object code. Compilation is continued by alternating overlay input and object output until ST 106.06 when the last FORTRAN overlay is loaded into core. It is probably used to generate completion messages. Accesses to disk address 116 and 143 show that RT-11 utility routines for terminal I/O are brought into core. Eight directory accesses starting at ST 106.21 close the source and object files.

Already this simple monitoring session shows several performance bugs in RT-11 and the compiler. Directory access time can be reduced when the search is started within the last directory segment which is still in core. The probability of finding a file entry close to the last accessed one is higher than to find it in the beginning of the directory. A similar technique is found in memory paging algorithms where it is known as the "least recently used" method (see for example [37]). Further I/O time could be saved if the object code buffer size in the FORTRAN

compiler is increased. Corresponding changes in PT-11 and the compiler would reduce the compilation time at least by 12% in this example. The fact that all disk interrupts occurred while the PC was pointing to RT-11 indicates that the compilation process is I/O bound. The program transfers control back to RT-11 for the next I/O request before the previous one is terminated. PT-11 executes a wait loop between locations 127130 and 127124 until the next interrupt arrives.

To obtain more details on the relationship between I/O and computing activity, the compilation was sampled at different frequencies. Figure A.10 shows the HIMOS output for 40 ms samples and fig. A.11 lists the corresponding commands for this session. The PC values show that less than one fifth of execution time is spent in the FORTRAN compiler. Another sampling session with 10 ms intervals confirmed this result. As expected, the compiler is only active immediately after disk interrupts.

The overhead imposed by HIMOS during the sampling sessions amounted to 5% of the total compilation time. It is interesting to see that the monitor overhead did not increase significantly with a higher sampling rate. This can be attributed to the fact that most samples were taken during I/O wait periods.

A last experiment was done to check if compilation time could be reduced by locating the FORTRAN compiler and the object file on the disk closer together. The disk space between the two files was reduced by 1172 blocks which corresponds to 45 tracks. As a result, the compilation was

400 ms quicker. Because the disk arm moved 12 times from one file to the other, the average saving per arm movement is approximately 33 ms.

5.3 Further Possibilities for HIMOS Assisted Research

Apart from the possibilities demonstrated in the last chapter, there are mainly three research topics which have influenced the implementation of HIMOS. The following paragraphs will point out how the monitoring system can be used to assist this research.

During the past few years, several techniques have been developed to prove the correctness of a given high level language program. One method, called the "deductive theory" was presented by Hoare and Lauer [35]. The meaning of a language is defined by axioms together with rules of inference. Theorems are derived from the axioms by means of these rules. The basic axiom of the theory is written as $P\{Q\}R$ where P and R are assertions about the memory state before and after execution of the statement (or program) Q. P states the necessary entry conditions for Q, and R is calculated from P and Q using the theorems of the deductive theory. If Q terminates and if P was true before execution, then R will be true when execution is complete. Given a linear sequence Q of statements without branches or entry points, logical expressions for P and R can be established. When the sequence is executed on the host machine, memory values can be monitored to compute the expression for P. When R is true upon exit from Q, the sequence has been executed correctly according to the programmer's intentions.

If, for example, a programmed loop (L) is observed, two software hooks are sufficient to verify the correctness of execution no matter how many statements are involved. The first hook is located in front of L and causes the verification of P in the control system. If P is not true, the process should be aborted because the termination of the loop cannot be guaranteed. The second hook is inserted immediately after the exit of L. At this point, the evaluation of R will show if the loop was executed correctly. Memory values that are necessary to compute the assertions can be obtained at interrupt time either through the hardware monitor directly from memory or by means of the software monitor from general purpose registers.

This method has the advantage of verifying correctness of programs during execution without producing an excessive amount of data as the trace technique does. It also reduces the necessary preparation time for the calculation of assertions which is required for purely theoretical correctness proofs.

The prevention and detection of deadlocks constitutes another promising application field for monitors. Although HIMOS was implemented for RT-11 which is a single user system under which this problem cannot be encountered, it is felt that a short discussion of this topic is justified by the importance of the problem. A deadlock is a situation in which parts of, or even all system activities are blocked due to an erroneous scheduling decision. A fatal deadlock situation may, for example, arise when the spooling space becomes completely filled with input records for jobs

waiting to execute and with output records for jobs not finished executing. In many systems there is no way to recover the spooling space which is occupied by a partially executed job. Several ad hoc methods have been employed to reduce the probability for deadlocks without giving a guarantee for their complete elimination. Other approaches, mostly based on graph models (see for example [54]), attempt to formalize the problem and to construct detection and recovery algorithms. Hybrid monitors offer a compromise in the detection and prevention of deadlocks. The software part can observe the task arrangement in waiting queues of the system as well as possible relations between those tasks. This may lead to the detection of situations in which tasks are waiting for each other without being able to resolve their requirements. The workload of critical resources can be observed by the hardware monitor. If, for example, the utilization of spooling space becomes too high and the monitor control system obtains at the same time the information that the waiting queue for this resource is growing, an imminent deadlock is indicated. In such situations a warning can be displayed at the operator's console or the monitor can supply a corresponding message directly to the operating system.

Finally, HIMOS can give practical assistance for efficiency analysis of paging algorithms. The memory management unit in the PDP 11/45 divides the full address range of 128 K words into 48 pages of 32 to 4096 words each. When a location outside of the current page limits is accessed a trap to address 250 is generated. When this trap vector is

intercepted by S-MON, the occurrence of page faults can be monitored. In sampling mode, S-MON can examine the content of the page address registers to record the current memory partitions. This information can be complemented with a memory utilization report from H-MON when it is sampling the PC activity.

The examples outlined in this and the previous chapter are far from giving a complete survey of applications for HIMOS. Individual requirements and practical experience with the system should motivate exploration of further possibilities of the monitor.

CHAPTER 6

Evaluation and Conclusion6.1 Evaluation of HIMOS

The monitor has proven to be a reliable tool for performance measurements. Once acquainted with the system, the user can dispense with a large set of control commands. Several command files provide the possibility to predefine various monitoring sessions which can be evoked without profound knowledge of system internal details. All monitor results reflect exactly the host computer activities and HIMOS reports are reproduceable at any time. The system's greatest successes have been the following:

- a. Its centralized control allows the specification of all functions from the terminal at the supervisor system. Erroneous command input or ambiguous instructions (such as two different output modes on the same terminal) are detected and comprehensive error messages are generated. System internal plausibility checks recognize software and hardware errors.
- b. Real time data filtering reduces the amount of recorded and displayed information. Only pertinent data is retained for further analysis.
- c. Its interactivness enables the user to redefine a monitor session according to new requirements while host activities are suspended at a defined state. Host execution can be slowed down to follow up event occurrences in real

time on the display.

d. Three different output modes of which two can be handled concurrently, satisfy all needs for online and offline analysis. The graphic output produces a dynamic picture of system activities. A modular implementation facilitates future extensions for other integrated evaluation features.

e. Most failures of the host CPU and any peripherals attached to it can be reported. Analysis of such events is assisted by the accompanying status report.

f. All necessary information for various applications is supplied, namely:

- Performance improvement
- System profile, activity log
- Problem oriented sessions (debugging)
- Activity reports for simulation model input.

Yet, HIMOS also has some deficiencies, specifically:

a. The command handler for host system mode specifications accepts a very abbreviated form of input. Some familiarisation is required to define the host tables.

b. The monitor overhead is relatively high. Creation and transmission of one event record takes from 1.43 ms to 3.14 ms, depending on the length of the record. During this time the host computer is exclusively dedicated to monitor activities. This time requirement is explained by the following 3 reasons:

1. To maintain the capacity of interactive response to special events, monitor actions cannot overlap with

host operations to serve user or RT-11 tasks.

- (C) 2. Event records are encoded into ASCII prior to their transmission.
3. Event records are analyzed in the control system to detect special events before the host system is released for normal execution.
- c. Because S-MON was implemented under RT-11 its possibilities are limited to applications within a single user system.
- d. The operating system has to be slightly modified to allow undisturbed operation of S-MON. With the exception of the FORTRAN run time error message handler, the changes do not affect any system properties.

The hardware monitor will most probably be implemented by the end of this year. Because of time and equipment limitations, many desirable features were excluded in the final design. Due to the interrupt latency of the PDP 11/20 CPU, the maximum sampling frequency had to be limited to 10 KHz. A DMA link between H-MON and the control system would offer a variety of further applications. As the control software includes already all necessary routine entries to handle the communication to and from H-MON, its adaptation to HIMOS will not create major problems.

6.2 Conclusion

Measuring computer performance during program execution can be compared with taking the blood pressure of a man under effort. Monitoring can actually be compared to

medicine. The only major difference lies in the complexity of the observed systems. In both cases, the performance is evaluated and important points for improvement or reasons for failure can be found.

The necessity to monitor activities in large computer systems has been generally recognized. The objectives are not only to increase cost efficiency of an installation but also to ensure reliability and to obtain hints for further efforts in research and development.

Mini computers have conquered an important market place during the past decade. Among other applications they are especially well suited for real time applications in process control. In this environment high reliability is an essential factor and monitors are a valuable tool to insure this objective.

During the implementation of HIMOS, several deficiencies in the design of computer hardware and software became evident. It is hoped that future hardware design will consider probe point requirements for hardware monitors. Especially with regard to the increasing trend of miniaturization and large scale integration there is a danger that many important signals become buried in a single chip. Monitor facilities should be a part of the standard equipment of CPU and peripheral hardware. One step in this direction has, for example, been taken by DEC. The KL10 processor produced by this company incorporates a PDP 11/40 CPU which is partly used to monitor hardware signals.

The same arguments can be cited for the development of operating system software. Information from monitoring

devices is useful to assist operating system decisions. Especially when software reaches the magnitude of OS/360, additional observation tools are indispensable.

Consequently two different approaches can be stated for system development with respect to monitors. The monitor can form an integral part of the system's hard and software. This approach was, for example, taken during the development of "Multics". However, this solution seems to have some dangers. It is quite possible that weak points in the system are only confirmed by corresponding deficiencies in the monitor, especially if the same team is responsible for implementing both parts.

A modular approach using distinct systems seems therefore more promising. It is quite possible that the standard configuration of future computer installations will dedicate one processor exclusively to control and measure the remaining system components. This method was adopted for the implementation of HIMOS. It is believed that HIMOS will constitute a valuable tool for future projects on the mini computer installation at McGill.

"The purpose of measurement is insight, not numbers."

(R.W. Hamming)

APPENDIX A

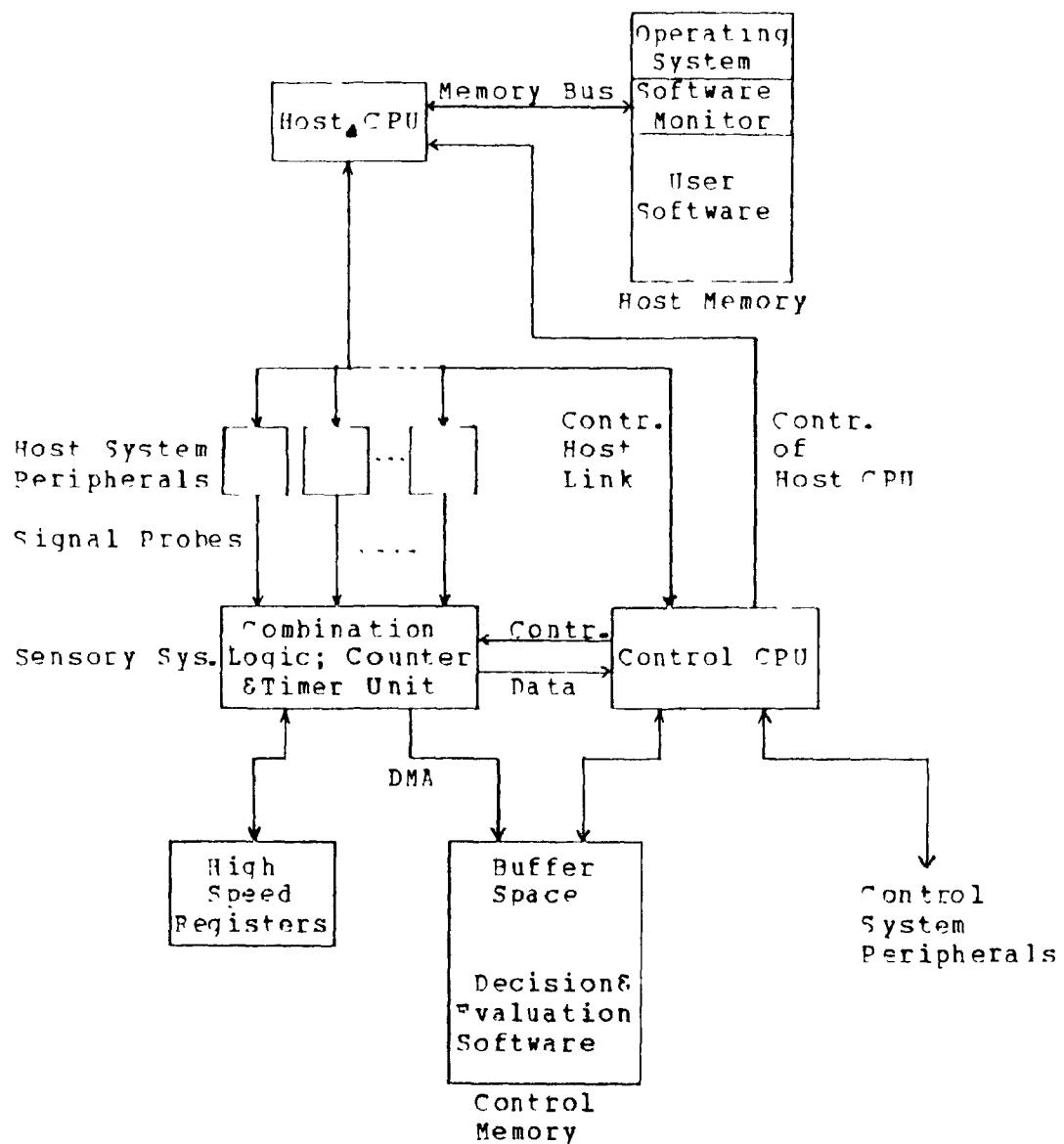
Figures and Tables

Figure A.1: A General Instrumentation System

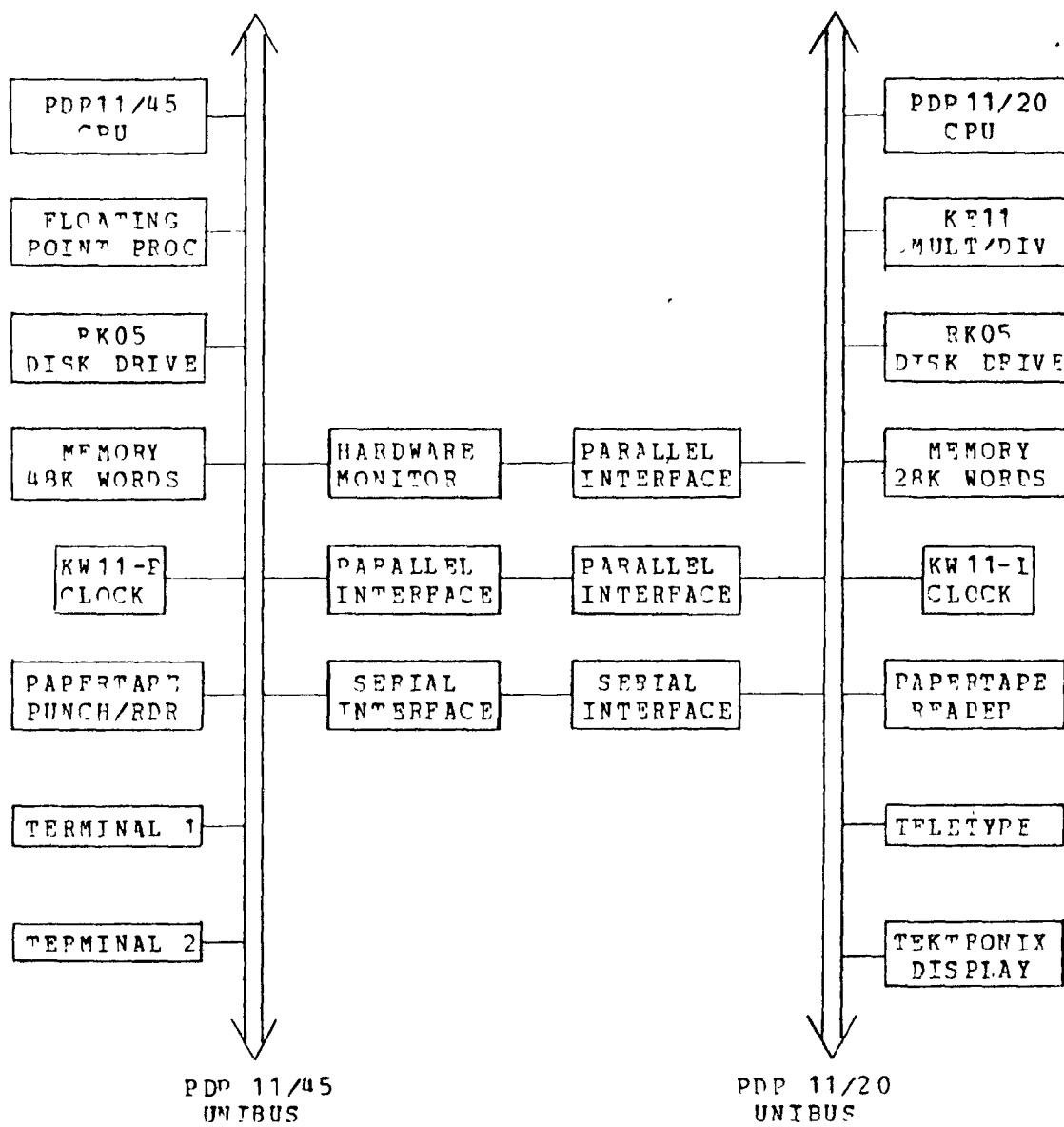


Figure A.2: System Configuration

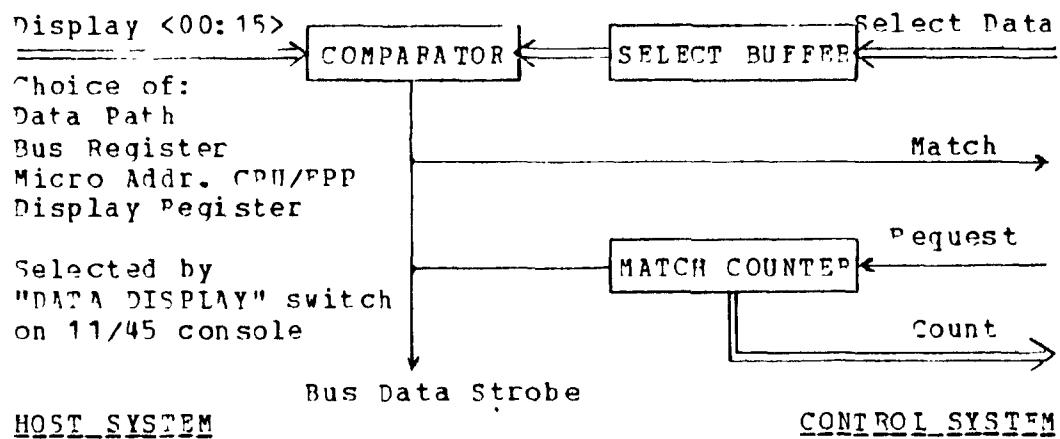


Figure A.3: Display Comparator

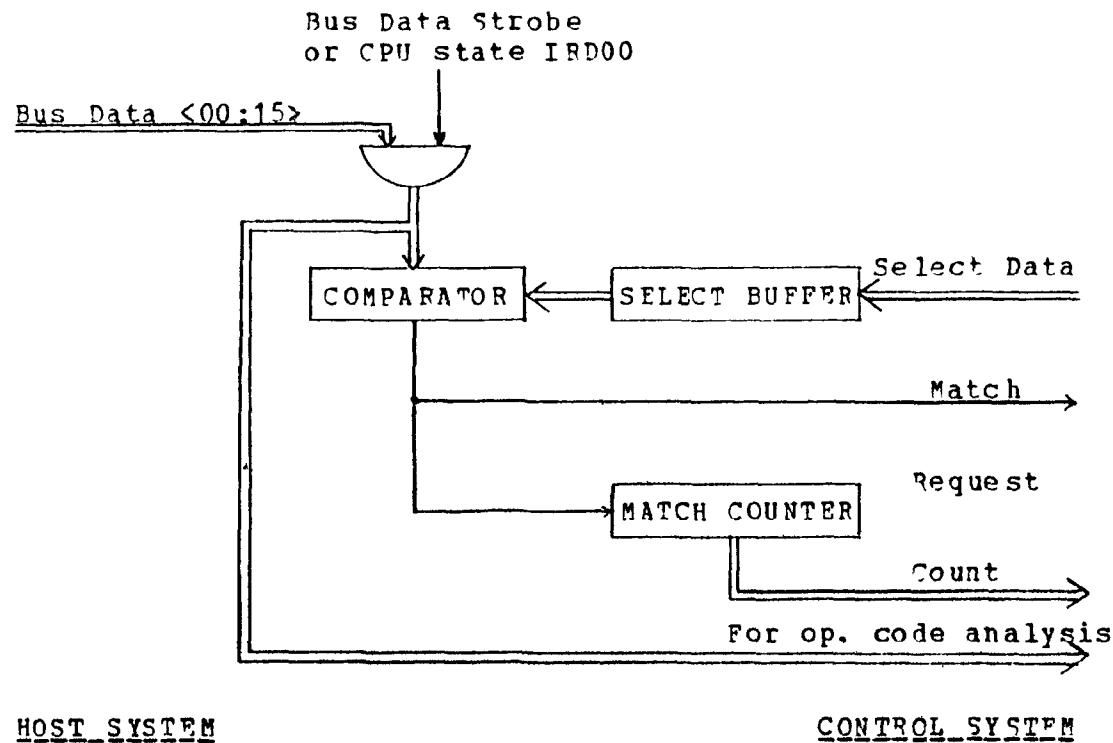
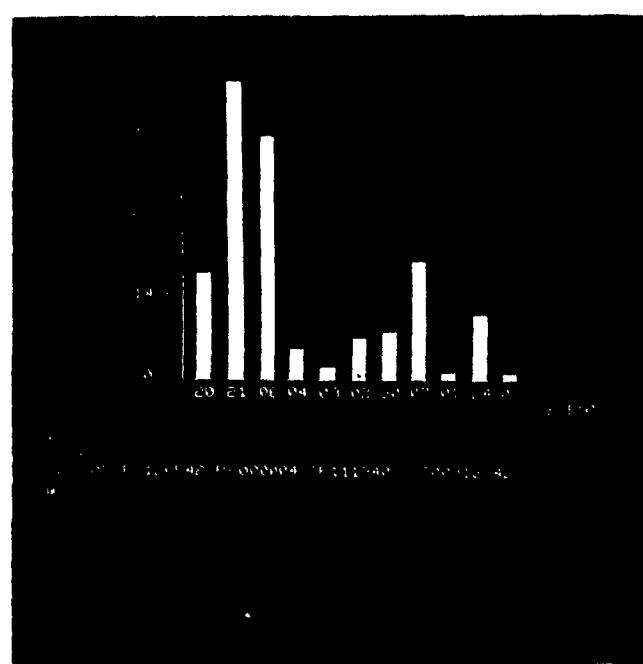


Figure A.4: Operation Code Analysis on UNIBUS Data Lines.



HIMOS LOG 14-7-76, 15:43, SAMGEN RUN UNDER FPP . ECG, 7

000006	PC106004	CP104374	EW000000	HT152345	ST00275. 11
000006	PC115546	CP104375	EW000000	HT152407	ST00275. 12
000006	PC115546	CP104375	EW000000	HT154216	ST00275. 17
000006	PC115546	CP104375	EW000000	HT155135	ST00275. 20
000006	PC115546	CP104375	EW000000	HT156042	ST00275. 23
000006	PC115546	CP104375	EW000000	HT156250	ST00275. 23
000006	PC013354	CP104375	EW000000	HT162405	ST00275. 36
000006	PC013420	CP104375	EW000000	HT162437	ST00275. 36
000007	PC001506	CP104400	HT162516	ST00275	37
000007	PC001506	CP104401	HT030077	ST00277.	32
000007	PC001506	CP104402	HT030130	ST00277	32
000006	PC005160	CP104375	EW000000	HT034073	ST00277. 44
000006	PC005160	CP104375	EW000000	HT035200	ST00277. 47
000006	PC005160	CP104375	EW000000	HT036120	ST00277. 50
000006	PC005160	CP104375	EW000000	HT037012	ST00277. 53
000006	PC005160	CP104375	EW000000	HT037241	ST00277. 54
000006	PC005160	CP104375	EW000000	HT037727	ST00277. 56
000006	PC005160	CP104375	EW000000	HT040152	ST00277. 56
000006	PC005160	CP104375	EW000000	HT040706	ST00277. 59
000007	PC001506	CP104403	HT043213	ST00278	.06
000007	PC001506	CP104401	HT043242	ST00278	.06
000007	PC001506	CP104402	HT043275	ST00278	.06
000007	PC001506	CP104403	HT043345	ST00278.	06
000007	PC001506	CP104401	HT043374	ST00278	.07
000007	PC001506	CP104402	HT043427	ST00278.	07
000007	PC001506	CP104403	HT043477	ST00278	.07
000007	PC001506	CP104401	HT043526	ST00278.	07
000007	PC001506	CP104402	HT043561	ST00278.	07
000007	PC001506	CP104403	HT043631	ST00278	.07
000007	PC001506	CP104401	HT043660	ST00278.	08
000007	PC001506	CP104402	HT043713	ST00278	.08
000007	PC001506	CP104403	HT043771	ST00278	.08
000007	PC001506	CP104401	HT044020	ST00278.	08
000007	PC001506	CP104402	HT044052	ST00278.	08
000007	PC001506	CP104403	HT044123	ST00278.	09
000007	PC001506	CP104401	HT044152	ST00278.	09
000007	PC001506	CP104402	HT044204	ST00278.	09
000007	PC001506	CP104403	HT044261	ST00278.	09
000007	PC001506	CP104401	HT044311	ST00278.	09
000007	PC001506	CP104402	HT044342	ST00278.	09
000007	PC001506	CP104403	HT044375	ST00278.	10
000007	PC001506	CP104401	HT044447	ST00278.	10
000007	PC001506	CP104402	HT044507	ST00278.	10
000007	PC001506	CP104403	HT044563	ST00278.	10
000007	PC001506	CP104401	HT044613	ST00278	.10
000007	PC001506	CP104402	HT044645	ST00278.	11
000007	PC001506	CP104403	HT044716	ST00278.	11
000007	PC001506	CP104401	HT044745	ST00278.	11
000007	PC001506	CP104402	HT044777	ST00278.	11
000007	PC001506	CP104403	HT045053	ST00278.	11
000007	PC001506	CP104401	HT045107	ST00278.	12
000007	PC001506	CP104402	HT045171	ST00278.	12
000007	PC001506	CP104403	HT045230	ST00278.	12

Figure A.7: Event Report for "SAMGEN" Execution under FPP (1)

HIMOS LOG 14-7-76, 15:43, SAMGEN RUN UNDER FPP . EC6, 7

000007	PC001506	CP104401	HT045260	ST00278	12
000007	PC001506	CP104402	HT045312	ST00278.	12
000007	PC001506	CP104403	HT045367	ST00278	13
000007	PC001506	CP104401	HT045417	ST00278	13
000007	PC001506	CP104402	HT045451	ST00278.	13
000007	PC001506	CP104403	HT045525	ST00278.	13
000007	PC001506	CP104401	HT045555	ST00278	13
000007	PC001506	CP104402	HT045607	ST00278.	13
000007	PC001506	CP104403	HT045664	ST00278.	14
000007	PC001506	CP104401	HT045714	ST00278.	14
000007	PC001506	CP104402	HT046035	ST00278.	14
000007	PC001506	CP104403	HT046112	ST00278.	15
000007	PC001506	CP104401	HT046142	ST00278	15
000007	PC001506	CP104402	HT046174	ST00278.	15
000007	PC001506	CP104403	HT046250	ST00278.	15
000007	PC001506	CP104401	HT046300	ST00278.	15
000007	PC001506	CP104402	HT046332	ST00278.	16
000007	PC001506	CP104403	HT046407	ST00278	16
000007	PC001506	CP104401	HT046437	ST00278	16
000007	PC001506	CP104402	HT046471	ST00278.	16
000007	PC001506	CP104403	HT046546	ST00278.	17
000007	PC001506	CP104401	HT046713	ST00278.	17
000007	PC001506	CP104402	HT046745	ST00278.	17
000007	PC001506	CP104403	HT047021	ST00278.	17
000007	PC001506	CP104404	HT047051	ST00278.	18
000006	PC005160	CP104375	EW000000	HT055734	ST00278. 39
000006	PC005160	CP104375	EW000000	HT056614	ST00278 41
000006	PC005160	CP104375	EW000000	HT057044	ST00278. 42
000006	PC005160	CP104375	EW000000	HT057764	ST00278. 45
000006	PC005160	CP104375	EW000000	HT060670	ST00278. 48
000006	PC005160	CP104375	EW000000	HT061110	ST00278. 48
000006	PC006430	CP104350	EW000000	HT063437	ST00278. 56

Figure A.7: Event Report for "SAMGEN" Execution under FPP (2)

```

*L
LOG MODE DEFINITION
H-LOG OR S-LOG SPECS (H,S) : S
OLD, NEW OR UPDATE (O,N,U) : N
LOG RECORDING (Y,N) : YES
NUMERIC DISPLAY (Y,N) : N
GRAPHIC DISPLAY (Y,N) : N
SAVE FILE (Y,N) : Y
    OUTPUT FILE FOR SPECS
*SES1=
    OUTPUT FILE FOR LOG RECORDING
*LOG5=

*S
HOST TABLE UPDATE
SPEC FILE-OLD OR UPDATE (O,U) : U

MASK UPDATE (Y,N)? : Y
GIVE INDEX OR T
#0
7654321076543210
0000000000001110
000000011001110
#T

SUBMASK UPDATE (Y,N)? : Y
GIVE INDEX OR T
#1
7654321076543210
0001001000110010
0001001000110011
#T

SELECT WORD UPDATE (Y,N)? : Y
GIVE INDEX OR T
#0
350 :
351 : 343
#1
340 : 374
341 : 375
#T

TIMER FREQUENCY (>3: NO TIME LOG): 1
TIMER COUNT      : 0
SAVE FILE (Y,N) : NO
*D

EVENT COUNT:

01:000000 02:000000 03:000000 04:000000 05:000000
06:000027 07:000076 10:000000 11:000000 12:000000
13:000000 14:000000 15:000000 16:000000 17:000000
20:000000 21:000000 22:000000 23:000000 24:000000
25:000000 26:000000 27:000000 30:000000 31:000000
32:000000 33:000000 34:000000 35:000000 36:000000

```

Figure A.8: Command Sequence for HIMOS Session of Fig. A.7

HIMOS LOG 12-7-76, 16 12, FORTRAN COMPILE HISTO FOR, EC30

000030	PC127130	R3	000010	R4	113366	HT155506	ST00102	52
000030	PC127130	R3	000012	R4	113366	HT156426	ST00102	55
000030	PC127130	R3	000014	R4	113366	HT157345	ST00102	58
000030	PC127130	R3	000020	R4	113366	HT157552	ST00102	59
000030	PC127124	R3	000016	R4	113366	HT160265	ST00103	01
000030	PC127130	R3	000016	R4	113366	HT161103	ST00103	03
000030	PC127124	R3	000010	R4	113366	HT161411	ST00103	04
000030	PC127124	R3	000012	R4	113366	HT162331	ST00103	07
000030	PC127130	R3	000014	R4	113366	HT163251	ST00103	10
000030	PC127120	R3	000020	R4	113366	HT163455	ST00103	11
000030	PC127124	R3	000016	R4	113366	HT164170	ST00103	13
000030	PC127130	R3	001007	R4	006400	HT165664	ST00103	18
000030	PC127130	R3	006531	R4	012654	HT167626	ST00103	24
000030	PC127130	R3	001014	R4	006632	HT174304	ST00103	38
000030	PC127130	R3	001021	R4	007010	HT176205	ST00103	42
000030	PC127130	R3	007267	R4	010520	HT000354	ST00103	50
000030	PC127124	R3	001026	R4	007152	HT002356	ST00103	56
000030	PC127130	R3	007270	R4	010520	HT005136	ST00104	05
000030	PC127124	R3	001033	R4	006344	HT007345	ST00104	12
000030	PC127130	R3	007271	R4	010520	HT011717	ST00104	19
000030	PC127130	R3	001040	R4	006502	HT014332	ST00104	27
000030	PC127124	R3	001045	R4	006604	HT016233	ST00104	32
000030	PC127130	R3	001052	R4	007144	HT020123	ST00104	38
000030	PC127124	R3	001060	R4	007360	HT021257	ST00104	42
000030	PC127130	R3	001063	R4	004316	HT023055	ST00104	47
000030	PC127130	R3	001066	R4	004646	HT024036	ST00104	50
000030	PC127130	R3	001073	R4	006406	HT026554	ST00104	59
000030	PC127124	R3	001101	R4	007520	HT030515	ST00105	04
000030	PC127130	R3	001105	R4	005624	HT031537	ST00105	08
000030	PC127130	R3	007272	R4	010520	HT033645	ST00105	14
000030	PC127124	R3	001112	R4	007204	HT036526	ST00105	22
000030	PC127130	R3	007273	R4	010520	HT042676	ST00105	36
000030	PC127124	R3	001120	R4	007276	HT045207	ST00105	47
000030	PC127130	R3	007274	R4	010520	HT047460	ST00105	50
000030	PC127130	R3	007275	R4	010520	HT050236	ST00105	52
000030	PC127130	R3	007276	R4	010520	HT051215	ST00105	56
000030	PC127130	R3	007277	R4	010520	HT052073	ST00105	58
000030	PC127130	R3	001126	R4	007330	HT054507	ST00106	06
000030	PC127124	R3	001002	R4	006500	HT055324	ST00106	08
000030	PC127130	R3	000116	R4	121366	HT057370	ST00106	15
000030	PC127130	R3	000143	R4	121366	HT060657	ST00106	19
000030	PC127130	R3	000016	R4	113366	HT061434	ST00106	21
000030	PC127120	R3	000010	R4	113366	HT061743	ST00106	22
000030	PC127124	R3	000012	R4	113366	HT062662	ST00106	25
000030	PC127130	R3	000014	R4	113366	HT063602	ST00106	28
000030	PC127130	R3	000020	R4	113366	HT064007	ST00106	29
000030	PC127130	R3	000016	R4	113366	HT064522	ST00106	30
000030	PC127130	R3	000016	R4	113366	HT065337	ST00106	33
000030	PC127130	R3	000116	R4	121366	HT067176	ST00106	38

Figure A.9: Disk Activity Report for a FORTRAN Compilation

HIMOS LOG 12-7-76, 18 03, FORTFAN COMPILE EC30, 24(40MS

000024 PC126532 ST0018E 39
000030 PC127130 R3 000010 ST00194 01
000030 PC127130 R3 000012 ST00194 04
000024 PC127130 ST00194 05
000030 PC127124 R3 000014 ST00194 07
000024 PC127124 ST00194 08
000030 PC127124 P3 000020 ST00194 08
000030 PC127130 R3 000016 ST00194 10
000024 PC116574 ST00194 10
000030 PC127130 R3 000016 ST00194 12
000024 PC127130 ST00194 12
000030 PC127130 P3 000010 ST00194 12
000024 PC127130 ST00194 15
000030 PC127130 R3 000012 ST00194 16
000024 PC127124 ST00194 17
000030 PC127124 R2 000014 ST00194 19
000024 PC127130 ST00194 20
000030 PC127130 P3 000020 ST00194 20
000030 PC127130 R3 000016 ST00194 22
000024 PC127124 ST00194 22
000024 PC127130 ST00194 24
000030 PC127130 R3 001007 ST00194 27
000024 PC126572 ST00194 27
000024 PC127130 ST00194 29
000024 PC127130 ST00194 32
000030 PC127130 R3 006531 ST00194 32
000024 PC005616 ST00194 34
000024 PC006266 ST00194 36
000024 PC006260 ST00194 39
000024 PC127124 ST00194 41
000024 PC127130 ST00194 44
000024 PC127130 ST00194 46
000030 PC127130 R3 001014 ST00194 47
000024 PC127130 ST00194 48
000024 PC127130 ST00194 51
000030 PC127130 R2 001021 ST00194 53
000024 PC127130 ST00194 53
000024 PC127130 ST00194 56
000024 PC127130 ST00194 58
000030 PC127130 R3 007306 ST00195 00
000024 PC127124 ST00195. 00
000024 PC127124 ST00195. 03
000024 PC127130 ST00195 05
000024 PC127130 ST00195 08
000030 PC127130 R3 001026 ST00195. 08
000024 PC127130 ST00195 10
000024 PC127124 ST00195 12
000030 PC127130 R3 007307 ST00195 14
000024 PC127124 ST00195. 15
000024 PC127124 ST00195 17
000024 PC127130 ST00195 20
000030 PC127130 R3 001033 ST00195. 21

Figure A.10: Sampling Session with 40 ms Periods (1)

HIMOS LOG 12-7-76, 18 03, FORTRAN COMPILE EC30, 24(40MS)

000024 PC127130 ST00195 24
000024 PC127130 ST00195 27
000030 PC127124 R3 007310 ST00195 29
000024 PC127130 ST00195 29
000024 PC127124 ST00195 32
000024 PC127130 ST00195 34
000030 PC127130 R3 001040 ST00195 36
000024 PC006350 ST00195 36
000024 PC004422 ST00195 39
000024 PC127124 ST00195 41
000030 PC127130 R3 001045 ST00195 42
000024 PC127124 ST00195 44
000024 PC127130 ST00195 46
000030 PC127130 R3 001052 ST00195 48
000024 PC003556 ST00195 48
000024 PC127130 ST00195 51
000030 PC127130 R3 001060 ST00195 51
000024 PC002642 ST00195 53
000024 PC127124 ST00195 56
000030 PC127124 R3 001063 ST00195 56
000024 PC003426 ST00195 58
000030 PC127130 R3 001066 ST00195 59
000024 PC003720 ST00196 00
000024 PC004152 ST00196 01
000024 PC127130 ST00196.05
000030 PC127124 R3 001073 ST00196 08
000024 PC125612 ST00196 08
000024 PC127130 ST00196.10
000024 PC127130 ST00196.12
000030 PC127124 R3 001101 ST00196 14
000024 PC003356 ST00196 15
000030 PC127130 R3 001105 ST00196 17
000024 PC002426 ST00196 17
000024 PC127130 ST00196 20
000024 PC127124 ST00196 22
000030 PC127130 R3 007311 ST00196 24
000024 PC002676 ST00196 24
000024 PC127130 ST00196.27
000024 PC127130 ST00196.29
000024 PC127124 ST00196 32
000030 PC127124 R3 001112 ST00196 32
000024 PC004700 ST00196.34
000024 PC006284 ST00196 36
000024 PC127124 ST00196.39
000024 PC127124 ST00196.41
000024 PC127130 ST00196.44
000030 PC127130 R3 007312 ST00196.46
000024 PC127130 ST00196.46
000024 PC127130 ST00196.48
000024 PC127130 ST00196.51
000030 PC127130 R3 001120 ST00196.52
000024 PC005340 ST00196.53
000024 PC127130 ST00196.56

Figure A.10: Sampling Session with 40 ms Periods (2)

HIMOS LOG 12-7-76, 18 02, FORTRAN COMPILE EC30, 24(40MS)

000030 PC127130 R3 007313 ST00197 00
000024 PC005340 ST00197. 00
000030 PC127130 R3 007314 ST00197 02
000024 PC003506 ST00197. 03
000030 PC127124 R3 007315 ST00197 05
000024 PC125612 ST00197 05
000024 PC127130 ST00197 08
000030 PC127124 P3 007316 ST00197. 08
000024 PC127130 ST00197 10
000024 PC127124 ST00197 12
000024 PC127130 ST00197 15
000030 PC127120 R3 001126 ST00197 15
000024 PC127124 ST00197 17
000030 PC127124 R3 001002 ST00197 17
000024 PC127130 ST00197 20
000024 PC127130 ST00197 22
000030 PC127130 P3 000116 ST00197 24
000024 PC127130 ST00197 24
000024 PC127130 ST00197 27
000030 PC127130 P3 000143 ST00197 28
000024 PC127130 ST00197 29
000030 PC127124 R3 000016 ST00197 30
000030 PC127130 R3 000010 ST00197 31
000024 PC127130 ST00197. 32
000030 PC127124 R3 000012 ST00197 34
000024 PC125612 ST00197 34
000024 PC127130 ST00197. 36
000030 PC127124 R3 000014 ST00197 37
000030 PC127130 R3 000020 ST00197 38
000024 PC127130 ST00197. 39
000030 PC127130 R3 000016 ST00197 40
000024 PC127124 ST00197. 41
000030 PC127130 R3 000016 ST00197. 42
000024 PC127124 ST00197 44
000024 PC127130 ST00197 46
000030 PC127130 R3 000116 ST00197 48
000024 PC122344 ST00197 48
000024 PC122344 ST00197. 51
000024 PC124062 ST00197. 53
000024 PC126534 ST00197. 56
000024 PC122326 ST00197. 58
000024 PC122440 ST00198. 00
000024 PC122436 ST00198. 03
000024 PC123366 ST00198. 05
000024 PC122332 ST00198. 08
000024 PC122444 ST00198. 10
000024 PC124114 ST00198. 12
000024 PC122326 ST00198. 15
000024 PC126606 ST00198. 17
000024 PC126614 ST00198. 20
000024 PC122316 ST00198. 22
000024 PC126604 ST00198. 24
000024 PC126542 ST00198. 27

Figure A.10: Sampling Session with 40 ms Periods (3)

*L
LOG MODE DEFINITION
H-LOG OR S-LOG SPECS (H,S) : S
OLD, NEW OR UPDATE (O,N,U) : UPD
NO LOG SPECIFIED
LOG RECORDING (Y,N) : N? : Y
NUMERIC DISPLAY (Y,N) : N? : N
GRAPHIC DISPLAY (Y,N) : N? : N
SAVE FILE (Y,N) : N
CONT. OUTPUT ON OLD FILE (Y,N) : N
OUTPUT FILE FOR LOG RECORDING
*LOG2=

*S
HOST TABLE UPDATE
SPEC FILE-OLD OR UPDATE (O,U) : U

MASK UPDATE (Y,N)? : Y
GIVE INDEX OR T
#1
7654321076543210
0000000000000000
0000000100010000
#T

SUBMASK UPDATE (Y,N)? : N

SELECT WORD UPDATE (Y,N)? : N

INTERR. FREQUENCY: 1 "=-10KHZ"
TIMER COUNT : 620 "DIV. BY 400 => 40MS SAMPLE RATE"
SAVE FILE (Y,N) : NO
*C
SP.EV. TABLE UPDATE:
GIVE EVENTS (* OR T)
#1
#2
#T
STOP ON HARD EVENT (Y,N) : N
*
SP.EV.:
000001 PC000007 PS000004 SP007124 ST00331.40
*C "TO RELEASE HOST SYSTEM"
*

Figure A.11: Command Sequence for HIMOS Session of Fig. A.10

<u>NAME</u>	<u>REF.</u>	<u>YEAR</u>	<u>PROPERTIES</u>
SNIFER	[21]	1967	Intercept monitor (first phase)
GECOS II	[43]	1968	Event and sample driven; output on printer or tape.
CUB	[24]	1969	Sampling monitor; distributed by Bool and Babbage Inc.
SIRE	[44]	1969	Event driven; output on tape.
PPE	[24]	1970	Sampling monitor; distributed by Bool and Babbage Inc.
SPY	[45]	1970	Sampling monitor; output on paper tape or display; controlled by PDP-9.
MULTICS	[18]	1970	Event driven; graphic display; controlled by PDP-8.
SLACMON	[51]	1970	Sampling or event driven; monitors IBM/360 under OS/MVT.

Table A.1: Survey of Pure Software Monitors.

<u>NAME</u>	<u>REF.</u>	<u>YEAR</u>	<u>PROPERTIES</u>
--	[24]	1958	First hardware monitor by IBM for laboratory use.
POEM	[24]	1963	Program oriented event monitor
SNUPER	[21]	1967	Event driven, preset by host software (second phase).
SPAP	[27]	1967	Accumulating monitor, possibl. to interrupt host system.
SUM	[24]	1969	First commercially distributed hardware monitor.
NEUPOTRON	[46]	1971	Minicomputer controlled; output on display and tape.
CPM-X	[34]	1972	Event driven; interaction with host software; minicomputer controlled.
DYNAPROBE	[47]	1972	Sampling and event driven; minicomputer controlled.
MICROSUM	[48]	1973	Accumulating monitor; real time display.
DSP1	[49]	1974	Accumulating and sampling; interaction with host software; output on display and tape.

Table A.2: Survey of Hardware and Hybrid Monitors

	<u>HARDWARE</u>	<u>SOFTWARE</u>	<u>HYBRID</u>
Host system degradation	none	medium to high	very low
Level of detail	medium	high	high
Operating sys. dependent	no	yes	less than soft. mon.
Training required	extensive	limited	extensive
Monitoring of op. sys. parameters	very diffic.	easy	easy
Software monit. capability	none	good	very good
Global system profile	good	medium	very good
Interrupt recognition	dep. on system	yes	yes
Device monitoring	yes	difficult	yes
Cost: Development Maintenance	high high	medium low	high high

Table A.3: Comparison of Monitoring Techniques.

<u>FC</u>	<u>Vector</u>	<u>Event</u>
-----------	---------------	--------------

Group 0:

00	--	not used
01	04	Trap to 4
02	10	Trap to 10
03	14	BPT
04	20	IOT
05	24	Power fail
06	30	EMT
07	34	TRAP
10-17	--	not used

Group 1:

20	300	Console Keyboard
21	304	Console Printer
22	70	Paper Tape Reader
23	74	Paper Tape Punch
24	104	KW-11P Clock
25-27	--	not used
30	220	RK 11 disk
31	240	PIRQ
32	244	FPP (floating point proc.)
33	250	MMU (memory management)
34-37	--	not used

Table A.4: Event Code Interpretation.

Event Masks:

bit	7	6	5	4	3	2	1	0	
high	-	-	-	-	-	-	-	-	GROUP0
low	TRAP	EMT	PWPL	IOT	BPT	T10	T4	-	
high	-	-	-	-	MMU	PPP	PIRQ	RK	GROUP1
low	-	-	-	KW	PP	PR	TP	TK	

Submasks:

bit	7	6	5	4	3	2	1	0	
high	-	SP	PS	PC	SP	PS	PC	SP	PWPL, IOT
low	PS	PC	SP	PS	PC	SP	PS	PC	BPT, T10, T4
high	-	-	-	[PC-2]	SP	PS	PC-2	SEL	TRAP
low	-	-	ERC	[PC-2]	SP	PS	PC-2	SEL	EMT
high	-	-	-	[REG]	SP	PS	PC	SEL	TP
low	-	-	[BUF]	[REG]	SP	PS	PC	SEL	TK
high	-	-	-	[REG]	SP	PS	PC	SEL	PP
low	-	-	[BUF]	[REG]	SP	PS	PC	SEL	PR
high	-	-	-	-	SP	PS	PC	SEL	KW-11 CLOCK
low	-	-	[BUF]	[REG]	SP	PS	PC	SEL	
<u>SM5</u> - not used -									
high	-	-	-	-	-	RS	R4		RK 11 disk
low	R3	R2	R1	RO	SP	PS	PC	SEL	controller

Select Words

Selw. 0-3 : 7 EMT codes, one 0 as endmarker

Selw. 4-10: 7 TRAP codes, one 0 as endmarker

Selw. 11-20: 4 pairs of the form: Reg. number
Reg. value

Table A.5: Event Specifications

ID	<u>EXPLANATION</u>
PC	Program Counter
PS	Processor Status word
SP	Stack Pointer (=R7)
CP	Content of Program counter (=op. code for 1 wrd instr.)
EW	Error Word (=content of #52) for EMT calls
SR	Device Status Register
BF	Device Buffer Content
Rn	Register n of disk controller
HT	Host Time (content of host clock buffer)
ST	Supervisor Time (in sec. relative to start of session)

Table A.6: Value Identification for Numeric Display

<u>CMD SUBPROG</u>	<u>EXPLANATION</u>
W WAITUP	Terminal output is disabled
P PROC	Terminal output is enabled after W
E SPEVUP	Special event table update mode
C CONT	Continue after special event occurrence
B INPICI	Initialize histogram, draw coordinates
A DRPICI	Erase Screen and draw histogram as it was
D CNTOUT	Frase screen and print event summary report
S CSIS	CMD interpreter for S-MON mode definition
H CSIH	CMD interpreter for H-MON mode def. (not impl.)
L CSIL	CMD interpreter for logging mode definition
T TERM	Terminate session and print summary report

Table A.7: Control System Commands

```

1 .TITLE S-MON12 INTERACTIVE SOFTWARE MONITOR
2 *****  

3  

4 // THIS PROGRAM IS PART OF THE MONITOR SYSTEM "MIMOS".
5 // THE FIRST PART IS NONRESIDENT AND ONLY USED FOR INITIALISATION.
6 // THE SECOND PART IS RELOCATED ABOVE RT11 STARTING AT 134000
7 // FROM WHERE SYSTEM ACTIVITIES ARE MONITORED.
8 // S-MON IS A PURE INTERCEPT TYPE MONITOR WHICH CAN ANALYZE
9 // ANY VECTORED EVENT.
10 // PART ONE STARTS AT "START"
11 // PART TWO STARTS AT "STRES"
12 //  

13 *****  

14  

15 .MCALL .PRINT,,REGDEF,,EXIT,,INITBUF,,UEH,,SEND,,RECV,,DEF
16 .MCALL .TTYIN,,ITYOUT
17 .DEF
18 .REGDEF
19 .ASELECT
20 .=1000           LOAD POINT
21 .TITLE CONSTANT DEFINITIONS
22 *****  

23  

24  

25 M#1                   1#1 GROUPS
26 M#MAXM#M#4
27 N#16,<<M#1>>      N# = TOTAL NUMBER OF TESTED VECTORS
28  

29 EDT#6
30 ACK#6
31 BH7#340
32 PSH#177776
33 TTYOUT#177564          TTY OUTPUT STATUS
34 TbUF#172542            TTY/FK LMT BUFFER
35 TSTATE#172540           TTY/FK STATUS REGISTER
36 PLIV#520                VECTOR FOR PARALLEL LINK
37 PLSH#164020
38 PLDB#164022
39 PLIB#164004
40 IIS#PLSW                ISTATUS REG. -->
41 IOS#PLSK
42 IIB#PLTB
43 IOB#PLDD
44 IIV#PLIV
45 IOV#PLIV+4
46 COMCHI#115               ISTATUS REG. OF COMM. CHANNEL IN
47 COMCHG#105
48 BEGIN#134000              ISTART ADDR. OF RES. ROUTINE
49 NEWSTR#BEGIN
50 DIST#BEGIN-STRFS         ISR DURING MONITORING
51
52 IRELOCATED VARIABLES
53
54 XBLANK#BLANK+DIST
55 XAST#AST+DIST
56 XCHLF#CHLF+DIST
57 XREG#REG#+DIST           IUELIMETER FOR PRINT
                           ISAVE LOC FOR RD

```

1. Software Monitor (S-MON)

Software Documentation

CONSTANT DEFINITIONS RT-11 MACRO VM82-89 08111126 PAGE 1+

```

58      148824      XREGS=REGS+DIST
59      137046      XTXTBF=TX[BUF+DIST
60      134872      XENTRY0=ENTRY0+DIST
61      134874      XENTRY1=ENTRY1+DIST
62      134886      XENTRY2=ENTRY2+DIST
63      149236      XPSAV=PS$SAV+DIST
64      137412      XVECSV=VECSAV+DIST
65      137012      XVECT0=VECTAH+DIST
66      137170      XMSK0=MASK0+DIST
67      136390      XNPL=RPLACEMENT+DIST
68      140831      XDJK=DJHGT+DIST
69      137030      XQUES=QUES+DIST
70      137032      XMPC=MPC+DIST
71      137034      XMP5=MP5+DIST
72      137036      XMSP=MSP+DIST
73      137340      XMLPC=MLPC+DIST
74      157002      XPS2=MS2+DIST
75      137224      XS0060=SLE060+DIST
76      134702      XDE=DÉ+DIST
77      130700      XSG09=S60H+DIST
78      135070      XSG01=S001+DIST
79      135300      XSG10=S610+DIST
80      135450      XSG11=S611+DIST
81      135760      XSG12=S612+DIST
82      134450      XTABUP=TABUPG+DIST
83      130410      XHANG=HANG+DIST
84      137300      XUSPT0=USPT0+DIST
85      137400      XUSPT2=USPT2+DIST
86      137240      XS1100=S1100+DIST
87      137284      XMS101=MASK101+DIST
88      137712      YOSFAT=YSTAT+DIST
89      140656      XHTII=HTII+DIST
90      137260      XMK005=M5A05+DIST
91      134700      XENDR0=ENDR0+DIST
92      137392      XEUDCH=EUUCDH+DIST
93      130426      XCONT=CONT+DIST
94      137266      XTHMON=THMON+DIST
95      137276      XTHT1=THT1+DIST
96      137390      XTHT2=THT2+DIST
97      137272      XTHREG1=THREG1+DIST
98      137274      XTHREG2=THREG2+DIST
99
100
101
102
103
104
105
106
107
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109
110
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112
113
114

.TITLE MACRO DEFINITIONS
*****  

.MACRO .OCOUT
    JSR PC,OPRINT
.JSR PC,OPUT
.ENDM

.MACRO .OCHOUT
    JSR PC,PRINT
.JSR PC,PUT
.ENDM

```

MACRO DEFINITIONS

RT-11 MACRO VM02-09

08311125 PAGE 8+

115		
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126
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128
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130
131
132
133

.MACRO .SNDWRD
TST #4PL5K
BHI ,=4
MOV R0,#4PL0B
.ENDM

.MACRO .RCVWRD
TSTU #4PL5R
BPL ,=4
MOV #4PL1B,R0
.ENDM

.MACRO .BUFOUT
PJSR PC,PRNTBF
JSR PC,SEND0F
BIT #2,R4
.ENDM

TRANSMIT ONE WORD IN SUPERV.
IF WAS PREVIOUS WORD RECEIVED?
WAIT IF NOT
STORE WORD IN R0

RECEIVE ONE WORD FROM SUPERV.
IF IS THERE A NEW WORD
WAIT IF NOT
STORE WORD IN R0

TRANSMISSION OF ONE EVENT RECORD
ENDMARKER SET?

I/O SUBROUTINES - NON RESIDENT RT-11 MACRO VME2-B9 00:11:26 PAGE 2

1
2
3
4
5 001000
6
7. 001000
8 00100c 105737 177564
9 00100b 100375
10 001010 0d0287
11
12
13 001012
14
15
16 00101c 910346
17 001014 005001
18 001016 005003
19 001024 005046
20 001022
21 001026 042700 000000
22 001032 122700 000012
23 001036 001402
24 001040 010046
25 001042 000767
26 001044 005126
27 001046 005116
28 001050 001416
29 001052 0e2716 000124
30 001056 001410
31 001060 102716 000000
32 001064 011600
33 001066 072603
34 001070 000001
35 001072 002703 000003
36 001076 000762
37 001078 012700 177777
38 001074 010757
39 001106 005703
40 001110 001002
41 001112 052700 177775
42 001116 005726
43 001120 012603
44 001122 000007
45
46
47 001124
48
49
50 001124 010146
51 001126 000246
52 001130 042700 177400
53 001134 012701 000003
54 001140 000404
55
56 001142
57

1 TITLE I/O SUBROUTINES - NON RESIDENT
2 *****
3 PRINTI: IPRINT TEXT STARTING AT (R0)
4 *****
5 PRINT3: TSTB #TTYOUT
6 RPL PRINT3
7 RTS PC RETURN FROM PRINT
8 *****
9 OCRD0: IREAD OCTAL NUMBER; LINKAGE: PC
10 ***** T=0=-3 IF T, -2 IF EMPTY; RESULT IN R1
11
12
13 OCRD1: TTYIN
14 CLR R1
15 CLR R3
16 CLR -(SP) ISHIFT COUNTER
17 ISTART MARKER ON TOP
18 OCRD1S: TTYIN
19 BIC #200,RR
20 CMPB #12,RR
21 BEQ OCRD0
22 MOV R0,-(SP) ISTACK NUMBER
23 BH OC RD01
24 OC RD02: TST (SP)+
25 TST (SP) STOP OF STACK?
26 BEQ OC RD05 IYES
27 CMP #124,(SP) IT?
28 BEQ OC RD04
29 SUH #60,(SP) I CONVERT
30 MOV (SP),RR
31 ASH R3,RR I SHIFT-NB N TIMES LEFT
32 RIS RR,1
33 ADD #3,R3 I INC R SHIFT CNT
34 BR OC RD03
35 OC RD04: MOV 4-1,RR I-3 IF T
36 BEQ OC RD03
37 OC RD05: TST R3
38 GNE OC RD06
39 BIS #177775,RR I-2 IF EMPTY
40 OC RD06: TST (SP)+
41 MOV (SP)+,R3
42 RTS PC RETURN FROM OCIN
43 *****
44 PRTBYT: IPRINT BYTE OCTAL; LINKAGE: PC
45 ***** VALUE IN R0
46
47
48
49
50
51
52
53
54
55
56
57

PRTWRD: IPRINT WORD OCTAL; LINKAGE: PC
***** VALUE IN R0

I/O SUBROUTINES - NON RESIDENT RT-11 MACRO VM02-09 06:11:26 PAGE 2+

58			
59	001142	010146	MOV R1,-(SP)
60	001144	010246	MOV R2,-(SP)
61	001146	012701	MOV R6,R1
62	001152	013102	TYP1: MOV R1,R2
63	001154	010246	TYP2: MOV R6,-(SP)
64	001156	042716	BIC #177770,(SP)
65	001162	002241	CLC
66	001164	006400	RUR R6
67	001166	006200	ASR R6
68	001170	002200	ASR R6
69	001172	005301	DEC R1
70	001174	001367	BNE TYP2
71	001176	012600	TYP3: MOV (SP)+,R6
72	001200	005102	DEC R2
73	001202	001400	BED TYP4
74	001204	005701	TST R1
75	001206	031602	BLE TYP4
76	001208	005730	TST R2
77	001212	001406	BEG TYP5
78	001214	002700	AUD #60,R6
79	001220		,TT1OUT
80	001224	000001	WATT
81	001226	007201	INC R1
82	001230	005102	TST R2
83	001232	001361	BNE TYP3
84	001234	012602	MOV (SP)+,R2
85	001236	012601	MOV (SP)+,R1
86	001240	-RC0207	RTS PC
87			RETURNS FROM PRTRYT/WRD
88			
89	001242		
90			
91			
92	001262	010306	IN***: HREAD WORD BTNARY1 LTHKAGE: PC
93	001264	010246	IN***: SWORN ADDR1: R1
94	001266	005202	
95	001268	005203	
96	001270		
97	001270	043100	MOV R5,-(SP)
98	001272	122700	MOV R2,-(SP)
99	001266	001410	CLR R2
100	001270	005203	CLR R3
101	001272	006302	BINR01: .TTYIN
102	001274	122700	BIC #e000,R0
103	001300	001764	CHPB #15,R0
104	001302	002702	BEG BINR01
105	001306	002761	INC R3
106	001310	005705	ASL R2
107	001312	001401	CHPB #P0,R0
108	001314	010231	REG BINR01
109	001316		HIS #1,R2
110	001322	012602	BR BINR01
111	001324	012603	BINR01: TST R3
112	001326	000207	REG BINR04
113			MOV R6,(1)
114			BINR04: .TTYIN
			MOV (SP)+,R2
			MOV (SP)+,R3
			RTS PC
			RETURNS FROM BINR0

00011126 PAGE 2 OF 10 QUESTIONS - NON RESIDENT RT-11 MURDO WMS-99

BINPARTS: /PRINT MHD BINARY; LINKAGE: PCL
 /OWNER: AUDH: R1

```

115 30133d   BINPUT: IPRINT WORD BINARY; LINKAGE: PC
116          JUMPEW WORD: R1
117          JUMPEW WORD: R1

118 00133d   B10106   B02453   B02453   BPRINT BIT IDENTIFIER STRING
119 001132   B27700   B02453
120 001130   B02453   B02453
121 001154d  B02453b  B02453b
122 001154d  B12791   B02474
123 001154d  B32703   B02474
124 001154d  B01463   B02474
125 001154d  B12721   B02474
126 001154d  B01462   B02474
127 001154d  B12721   B02474
128 001154d  B02474
129 0011572   B02474
130 0011570   B02474
131 0011569   B02474
132 0011464   B02474
133 0011419   B12701
134 0011412   B02474
135
136 0011414   B12701   B02474
137 0011420   B02474
138 0011420   B02474

          MOV BX,-(SP)           BPRINT BIT IDENTIFIER STRING
          MOV SI,BP,ES,RB
          JSR PC,PRINT
          MOV (1),ES
          MOV ABTS,RI
          RINPTI: BIR ABTS,ES,RB
          JCHECK LEFTMOST BIT
          HEO BX,ES,RB
          MOVS BX,(1)+

          BH B10106
          BINPUTT2: MOVS BX,(1)+

          BINPUTT3: ABT BX
          CHB R1,BITS+16
          BNE BINPUTT1
          MOV ABTS,RI
          JSR PC,PRINT
          MOV (SP)+,RI
          RETS PC

          JRETFUN4 FROMBINPUTT
          ***** ENTRY POINT *****

          STANT: MOV $102453,SP
          TST $0010
          JLLEN INPUT BUFFER

```

SPECIFICATION OF SP-MON MODE RT-11 MACRO VME2300 02:11:26 PAGE 3

```

1      *TYPE: SPECIFICATION OF SIMON MODE
2
3
4
5
6      * 001424 005005
7
8      * 001426 012706 002515
9      * 001427 177342
10
11      * 001432 001402
12      * 001426 012706 002515
13      * 001432 004767
14
15      * 001436
16
17      * 001436 002260
18      * 001442 122703 000003
19      * 001448 001402
20      * 001452 001402
21      * 001454 001401
22      * 001455 000767
23      * 001463
24      * 001464 122701 000116
25      * 001470 001401
26      * 001472 003175 0034624
27      * 001476 122701 000111
28      * 001482 001406
29      * 001514 002671
30      * 001515 003175 177264
31      * 001515 003175 003182
32
33      * 001530
34
35      * 001535 002108 002545
36      * 001534 0004167 117298
37      * 001530 012703 002663
38      * 001534 0004167 117298
39      * 001540 0004167 117298
40      * 001540 0004167 117298
41      * 001540 002112
42      * 001540 0004175 0031046
43      * 001540 0004175 0031046
44
45      * 001566
46
47      * 001569 000101
48      * 001562 000201
49      * 001564 000201
50      * 001564 000201
51      * 001574 000767 177942
52      * 001560 001753
53
54
55      * 001502 016551 006254
56      * 001504 000701
57

```

;SET LOOP SWITCH

CLR PS

;CHO10: *SubMask UPDATE*

;MOV *SubMask*,R1

;JBN PC,PRINT

;CHO11: *Set V/N INTERPRETER*

;RTTYN

;BIC #0000,RA

;CMPS #15,R3

;BEQ CM012

;MOV #00,AL

;AN CR011

;CMD12: RTTYN

;CM013: CMPS #16,R1

;BNE CM014

;JMP #CM015

;JMP #CM016

;CM014: CMPS #15, R1

;AN CR011

;MOV #CVER, R0

;JSW PC,PRINT

;JMP #CM017

;CHO15: *Set INDEX INPUT*

;MOV #REGARE

;JSW PC,PRINT

;CHO16: *Set ADDRESS & R1*

;MOV #CR015, R1

;JSR FC,PRINT

;JSW PC,PRINT

;TST R1

;BLT CM017

;JMP #CM018

;JSW PC,PRINT

;JMP #CM019

;CHO17: *Set MASK L/D*

;JSR MASK L/D

;ASL PI

;ASL R1

;ADD #MASK, R1

;JSW PC,PRINT

;BSR QWORD

;CHO19: *Set SubMask*

;JSW PC,PRINT

;ADD #MASK

;JSW PC,PRINT

;BSR QWORD

;CHO20: *Set R1*

;JSW PC,PRINT

;ADD #MASK

;JSW PC,PRINT

;BSR QWORD

SPECIFICATION OF S-MON MODE RT-11 MACRO VMB2-69 08111126 PAGE 5+

SPECIFICATION OF S-MON MODE RT-11 MACRO VM02-09 00:11:26 PAGE 3+

115	002026	005267	004334		CLR TREG1	
116	002112	002167	000020	004230	BIT #20,MASK1	SET THE INTERRUPT?
117	002020	001420			BED CM0119	END-ASK FOR TIMING
118						
119						*** TIME INTERR. MODE ***
120						
121	002022	012700	002703		MOV #TIMSTL,R0	IGET FREQUENCY
122	002325	004767	175706		JSR PC,PRINT	
123	002032	004767	176754		JSR PC,UCHO	READ A-3,
124	002030	002031			ASL R1	
125	002043	002701	000010		BIS #10,R1	
126	002044	002167	004276		BIS R1,TREG1	SET MHR. MODE DOWN
127	002050	005267	004266		INC TMON	SCHA. INTERRU. AFTER FARM
128	002054	002700	002777	CM01181	MOV #TIMSTT,R0	IGET COUNT
129	002063	004767	176714		JSR PC,PRINT	
130	002064	004767	176722		JSR PC,UCHO	
131	002070	001167	004254		MOV R1,TREG2	ISET CNT
132	002074	002421			BR CM0120	END OF TMR, TIMING
133						
134	002076	012700	002731			CM0119: *** TIME LOG MODE ***
135						
136	002076	012700	002731		MOV #TIMST2,R0	IGET FREQUENCY
137	002102	004767	176672		JSR PC,PRINT	
138	002106	002071	176700		JSR PC,UCHO	
139	002112	002161	000003		CMP #3,R1	S>3
140	002116	002040			BHT CM0120	SYS-NO TIME LOG
141	002120	006151			ASL R1	
142	002122	002701	000031		BIS #31,R1	START REP. MODE UP
143	002126	005267	004214		BIS R1,TREG1	
144	002132	005267	004206		INC TMLG	ISET TIME LOG MODE
145	002136	002706			BR CM0118	LOG, GET CNT
146						
147	002140			CM0120: *** TRAP INIT ***		
148						
149	002140	012737	140036	000034	MOV #YRTII,#34	L+RS-SET HTI AND. IN VECTOR
150	002146	005237	000036		CLR #36	
151						
152	002152			CM0121: *** VECTOR PROTECTION ***		
153						
154	002152	013700	000054		MOV #S9,R2	
155	002156	002760	177777	000326	BIS #177777,326(2)	ISPAR VECT. PROTECTION
156	002164	002760	177777	000332	BIS #177777,332(0)	ALLCP VECT. PROTECTION
157	002172	002760	177777	000332	BIS #177777,342(2)	LC7AM. CH. VECT. PROTECTION
158	002200	012737	000240	146762	MOV #240, #146762	CHANGE SYS. RESET TO HIGH
159						
160						

INITIALISATION PROGRAM RT-11 MACRO VMS2-06

00:11125 PAGE 4.

TITLE INITIATION PROGRAM

```

        .EXIT
      RIS RISSTAT
      REG FIN
      TST TIMEON
      HDY DUMP
      ISEL MARS FDH .EXIT
      ICLUS47
      ING TIME INTENQUIP
      INSTAK CLKU INTENQ. MODE

```

INITIALISATION PROGRAM RT-11 MACRO VM922-09

00:11:26 PAGE 4+

```

58 002621 015 012 123 SELWIN: ASCII <15><12>/SELECT AND UPDATE (Y,N)? & /<27E>
59 002661 015 012 043 CROSS: ASCII <15><12>/& /<27D>
60 002665 048 072 045 GAP: ASCII / : /<27D>
61 002571 077 111 114 CHDERR: ASCII /711L CHD2/
62 002745 015 012 111 TIMST1: ASCII <15><12>/INTERVAL FREQUENCY /<26B>
63 002751 025 012 124 TIMST2: ASCII <15><12>/TIMER FREQUENCY (SS: NO TIME L76): /<27B>
64 002771 124 111 115 TIMCNT: ASCII /TIME COUNT : /<27B>
65 002777 111 115 EVEN
CMDT11 CM0110
CMDT12 CM0112
CMDT13 CM0117
CMDT21 CM012
CMDT22 CM0122
CMDT31 CM0131
CMDT32 CM0132
CMDT33 CM0133
CMDT41 CM0141
CMDT42 CM0142
CMDT51 CM0151
CMDT52 CM0152
CMDT61 CM0161
CMDT62 CM0162
CMDT71 CM0171
CMDT72 CM0172
CMDT81 CM0181
CMDT82 CM0182
CMDT91 CM0191
CMDT92 CM0192
CMDT101 CM01A1
CMDT102 CM01A2
CMDT111 CM01B1
CMDT112 CM01B2
CMDT121 CM01C1
CMDT122 CM01C2
CMDT131 CM01D1
CMDT132 CM01D2
CMDT141 CM01E1
CMDT142 CM01E2
CMDT151 CM01F1
CMDT152 CM01F2
CMDT161 CM01G1
CMDT162 CM01G2
CMDT171 CM01H1
CMDT172 CM01H2
CMDT181 CM01I1
CMDT182 CM01I2
CMDT191 CM01J1
CMDT192 CM01J2
CMDT201 CM01K1
CMDT202 CM01K2
CMDT211 CM01L1
CMDT212 CM01L2
CMDT221 CM01M1
CMDT222 CM01M2
CMDT231 CM01N1
CMDT232 CM01N2
CMDT241 CM01O1
CMDT242 CM01O2
CMDT251 CM01P1
CMDT252 CM01P2
CMDT261 CM01Q1
CMDT262 CM01Q2
CMDT271 CM01R1
CMDT272 CM01R2
CMDT281 CM01S1
CMDT282 CM01S2
CMDT291 CM01T1
CMDT292 CM01T2
CMDT301 CM01U1
CMDT302 CM01U2
CMDT311 CM01V1
CMDT312 CM01V2
CMDT321 CM01W1
CMDT322 CM01W2
CMDT331 CM01X1
CMDT332 CM01X2
CMDT341 CM01Y1
CMDT342 CM01Y2
CMDT351 CM01Z1
CMDT352 CM01Z2
CMDT361 CM01AA1
CMDT362 CM01AA2
CMDT371 CM01AB1
CMDT372 CM01AB2
CMDT381 CM01AC1
CMDT382 CM01AC2
CMDT391 CM01AD1
CMDT392 CM01AD2
CMDT401 CM01AE1
CMDT402 CM01AE2
CMDT411 CM01AF1
CMDT412 CM01AF2
CMDT421 CM01AG1
CMDT422 CM01AG2
CMDT431 CM01AH1
CMDT432 CM01AH2
CMDT441 CM01AI1
CMDT442 CM01AI2
CMDT451 CM01AJ1
CMDT452 CM01AJ2
CMDT461 CM01AK1
CMDT462 CM01AK2
CMDT471 CM01AL1
CMDT472 CM01AL2
CMDT481 CM01AM1
CMDT482 CM01AM2
CMDT491 CM01AN1
CMDT492 CM01AN2
CMDT501 CM01AO1
CMDT502 CM01AO2
CMDT511 CM01AP1
CMDT512 CM01AP2
CMDT521 CM01AQ1
CMDT522 CM01AQ2
CMDT531 CM01AR1
CMDT532 CM01AR2
CMDT541 CM01AS1
CMDT542 CM01AS2
CMDT551 CM01AT1
CMDT552 CM01AT2
CMDT561 CM01AU1
CMDT562 CM01AU2
CMDT571 CM01AV1
CMDT572 CM01AV2
CMDT581 CM01AW1
CMDT582 CM01AW2
CMDT591 CM01AX1
CMDT592 CM01AX2
CMDT601 CM01AY1
CMDT602 CM01AY2
CMDT611 CM01AZ1
CMDT612 CM01AZ2
CMDT621 CM01BA1
CMDT622 CM01BA2
CMDT631 CM01CA1
CMDT632 CM01CA2
CMDT641 CM01DA1
CMDT642 CM01DA2
CMDT651 CM01EA1
CMDT652 CM01EA2
CMDT661 CM01FA1
CMDT662 CM01FA2
CMDT671 CM01GA1
CMDT672 CM01GA2
CMDT681 CM01HA1
CMDT682 CM01HA2
CMDT691 CM01IA1
CMDT692 CM01IA2
CMDT701 CM01JA1
CMDT702 CM01JA2
CMDT711 CM01KA1
CMDT712 CM01KA2
CMDT721 CM01LA1
CMDT722 CM01LA2
CMDT731 CM01MA1
CMDT732 CM01MA2
CMDT741 CM01NA1
CMDT742 CM01NA2
CMDT751 CM01OA1
CMDT752 CM01OA2
CMDT761 CM01PA1
CMDT762 CM01PA2
CMDT771 CM01QA1
CMDT772 CM01QA2
CMDT781 CM01RA1
CMDT782 CM01RA2
CMDT791 CM01SA1
CMDT792 CM01SA2
CMDT801 CM01TA1
CMDT802 CM01TA2
CMDT811 CM01UA1
CMDT812 CM01UA2
CMDT821 CM01VA1
CMDT822 CM01VA2
CMDT831 CM01WA1
CMDT832 CM01WA2
CMDT841 CM01XA1
CMDT842 CM01XA2
CMDT851 CM01YA1
CMDT852 CM01YA2
CMDT861 CM01ZA1
CMDT862 CM01ZA2
CMDT871 CM01AA1
CMDT872 CM01AA2
CMDT881 CM01AB1
CMDT882 CM01AB2
CMDT891 CM01AC1
CMDT892 CM01AC2
CMDT901 CM01AD1
CMDT902 CM01AD2
CMDT911 CM01AE1
CMDT912 CM01AE2
CMDT921 CM01AF1
CMDT922 CM01AF2
CMDT931 CM01AG1
CMDT932 CM01AG2
CMDT941 CM01AH1
CMDT942 CM01AH2
CMDT951 CM01AI1
CMDT952 CM01AI2
CMDT961 CM01AJ1
CMDT962 CM01AJ2
CMDT971 CM01AK1
CMDT972 CM01AK2
CMDT981 CM01AL1
CMDT982 CM01AL2
CMDT991 CM01AM1
CMDT992 CM01AM2
CMDT1001 CM01AN1
CMDT1002 CM01AN2
CMDT1011 CM01AO1
CMDT1012 CM01AO2
CMDT1021 CM01AP1
CMDT1022 CM01AP2
CMDT1031 CM01AQ1
CMDT1032 CM01AQ2
CMDT1041 CM01AR1
CMDT1042 CM01AR2
CMDT1051 CM01AS1
CMDT1052 CM01AS2
CMDT1061 CM01AT1
CMDT1062 CM01AT2
CMDT1071 CM01AU1
CMDT1072 CM01AU2
CMDT1081 CM01AV1
CMDT1082 CM01AV2
CMDT1091 CM01AW1
CMDT1092 CM01AW2
CMDT1101 CM01AX1
CMDT1102 CM01AX2
CMDT1111 CM01AY1
CMDT1112 CM01AY2
CMDT1121 CM01AZ1
CMDT1122 CM01AZ2
CMDT1131 CM01BA1
CMDT1132 CM01BA2
CMDT1141 CM01CA1
CMDT1142 CM01CA2
CMDT1151 CM01DA1
CMDT1152 CM01DA2
CMDT1161 CM01EA1
CMDT1162 CM01EA2
CMDT1171 CM01FA1
CMDT1172 CM01FA2
CMDT1181 CM01GA1
CMDT1182 CM01GA2
CMDT1191 CM01HA1
CMDT1192 CM01HA2
CMDT1201 CM01IA1
CMDT1202 CM01IA2
CMDT1211 CM01JA1
CMDT1212 CM01JA2
CMDT1221 CM01KA1
CMDT1222 CM01KA2
CMDT1231 CM01LA1
CMDT1232 CM01LA2
CMDT1241 CM01MA1
CMDT1242 CM01MA2
CMDT1251 CM01NA1
CMDT1252 CM01NA2
CMDT1261 CM01OA1
CMDT1262 CM01OA2
CMDT1271 CM01PA1
CMDT1272 CM01PA2
CMDT1281 CM01QA1
CMDT1282 CM01QA2
CMDT1291 CM01RA1
CMDT1292 CM01RA2
CMDT1301 CM01SA1
CMDT1302 CM01SA2
CMDT1311 CM01VA1
CMDT1312 CM01VA2
CMDT1321 CM01WA1
CMDT1322 CM01WA2
CMDT1331 CM01XA1
CMDT1332 CM01XA2
CMDT1341 CM01YA1
CMDT1342 CM01YA2
CMDT1351 CM01ZA1
CMDT1352 CM01ZA2
CMDT1361 CM01AA1
CMDT1362 CM01AA2
CMDT1371 CM01AB1
CMDT1372 CM01AB2
CMDT1381 CM01AC1
CMDT1382 CM01AC2
CMDT1391 CM01AD1
CMDT1392 CM01AD2
CMDT1401 CM01AE1
CMDT1402 CM01AE2
CMDT1411 CM01AF1
CMDT1412 CM01AF2
CMDT1421 CM01AG1
CMDT1422 CM01AG2
CMDT1431 CM01AH1
CMDT1432 CM01AH2
CMDT1441 CM01AI1
CMDT1442 CM01AI2
CMDT1451 CM01AJ1
CMDT1452 CM01AJ2
CMDT1461 CM01AK1
CMDT1462 CM01AK2
CMDT1471 CM01AL1
CMDT1472 CM01AL2
CMDT1481 CM01AM1
CMDT1482 CM01AM2
CMDT1491 CM01AN1
CMDT1492 CM01AN2
CMDT1501 CM01AO1
CMDT1502 CM01AO2
CMDT1511 CM01AP1
CMDT1512 CM01AP2
CMDT1521 CM01AQ1
CMDT1522 CM01AQ2
CMDT1531 CM01AR1
CMDT1532 CM01AR2
CMDT1541 CM01AS1
CMDT1542 CM01AS2
CMDT1551 CM01AT1
CMDT1552 CM01AT2
CMDT1561 CM01AU1
CMDT1562 CM01AU2
CMDT1571 CM01AV1
CMDT1572 CM01AV2
CMDT1581 CM01AW1
CMDT1582 CM01AW2
CMDT1591 CM01AX1
CMDT1592 CM01AX2
CMDT1601 CM01AY1
CMDT1602 CM01AY2
CMDT1611 CM01AZ1
CMDT1612 CM01AZ2
CMDT1621 CM01BA1
CMDT1622 CM01BA2
CMDT1631 CM01CA1
CMDT1632 CM01CA2
CMDT1641 CM01DA1
CMDT1642 CM01DA2
CMDT1651 CM01EA1
CMDT1652 CM01EA2
CMDT1661 CM01FA1
CMDT1662 CM01FA2
CMDT1671 CM01GA1
CMDT1672 CM01GA2
CMDT1681 CM01HA1
CMDT1682 CM01HA2
CMDT1691 CM01IA1
CMDT1692 CM01IA2
CMDT1701 CM01JA1
CMDT1702 CM01JA2
CMDT1711 CM01KA1
CMDT1712 CM01KA2
CMDT1721 CM01LA1
CMDT1722 CM01LA2
CMDT1731 CM01MA1
CMDT1732 CM01MA2
CMDT1741 CM01NA1
CMDT1742 CM01NA2
CMDT1751 CM01OA1
CMDT1752 CM01OA2
CMDT1761 CM01PA1
CMDT1762 CM01PA2
CMDT1771 CM01QA1
CMDT1772 CM01QA2
CMDT1781 CM01RA1
CMDT1782 CM01RA2
CMDT1791 CM01SA1
CMDT1792 CM01SA2
CMDT1801 CM01VA1
CMDT1802 CM01VA2
CMDT1811 CM01WA1
CMDT1812 CM01WA2
CMDT1821 CM01XA1
CMDT1822 CM01XA2
CMDT1831 CM01YA1
CMDT1832 CM01YA2
CMDT1841 CM01ZA1
CMDT1842 CM01ZA2
CMDT1851 CM01AA1
CMDT1852 CM01AA2
CMDT1861 CM01AB1
CMDT1862 CM01AB2
CMDT1871 CM01AC1
CMDT1872 CM01AC2
CMDT1881 CM01AD1
CMDT1882 CM01AD2
CMDT1891 CM01AE1
CMDT1892 CM01AE2
CMDT1901 CM01AF1
CMDT1902 CM01AF2
CMDT1911 CM01AG1
CMDT1912 CM01AG2
CMDT1921 CM01AH1
CMDT1922 CM01AH2
CMDT1931 CM01AI1
CMDT1932 CM01AI2
CMDT1941 CM01AJ1
CMDT1942 CM01AJ2
CMDT1951 CM01AK1
CMDT1952 CM01AK2
CMDT1961 CM01AL1
CMDT1962 CM01AL2
CMDT1971 CM01AM1
CMDT1972 CM01AM2
CMDT1981 CM01AN1
CMDT1982 CM01AN2
CMDT1991 CM01AO1
CMDT1992 CM01AO2
CMDT2001 CM01AP1
CMDT2002 CM01AP2
CMDT2011 CM01AQ1
CMDT2012 CM01AQ2
CMDT2021 CM01AR1
CMDT2022 CM01AR2
CMDT2031 CM01AS1
CMDT2032 CM01AS2
CMDT2041 CM01AT1
CMDT2042 CM01AT2
CMDT2051 CM01AU1
CMDT2052 CM01AU2
CMDT2061 CM01AV1
CMDT2062 CM01AV2
CMDT2071 CM01AW1
CMDT2072 CM01AW2
CMDT2081 CM01AX1
CMDT2082 CM01AX2
CMDT2091 CM01AY1
CMDT2092 CM01AY2
CMDT2101 CM01AZ1
CMDT2102 CM01AZ2
CMDT2111 CM01BA1
CMDT2112 CM01BA2
CMDT2121 CM01CA1
CMDT2122 CM01CA2
CMDT2131 CM01DA1
CMDT2132 CM01DA2
CMDT2141 CM01EA1
CMDT2142 CM01EA2
CMDT2151 CM01FA1
CMDT2152 CM01FA2
CMDT2161 CM01GA1
CMDT2162 CM01GA2
CMDT2171 CM01HA1
CMDT2172 CM01HA2
CMDT2181 CM01IA1
CMDT2182 CM01IA2
CMDT2191 CM01JA1
CMDT2192 CM01JA2
CMDT2201 CM01KA1
CMDT2202 CM01KA2
CMDT2211 CM01LA1
CMDT2212 CM01LA2
CMDT2221 CM01MA1
CMDT2222 CM01MA2
CMDT2231 CM01NA1
CMDT2232 CM01NA2
CMDT2241 CM01OA1
CMDT2242 CM01OA2
CMDT2251 CM01PA1
CMDT2252 CM01PA2
CMDT2261 CM01QA1
CMDT2262 CM01QA2
CMDT2271 CM01RA1
CMDT2272 CM01RA2
CMDT2281 CM01SA1
CMDT2282 CM01SA2
CMDT2291 CM01VA1
CMDT2292 CM01VA2
CMDT2301 CM01WA1
CMDT2302 CM01WA2
CMDT2311 CM01XA1
CMDT2312 CM01XA2
CMDT2321 CM01YA1
CMDT2322 CM01YA2
CMDT2331 CM01ZA1
CMDT2332 CM01ZA2
CMDT2341 CM01AA1
CMDT2342 CM01AA2
CMDT2351 CM01AB1
CMDT2352 CM01AB2
CMDT2361 CM01AC1
CMDT2362 CM01AC2
CMDT2371 CM01AD1
CMDT2372 CM01AD2
CMDT2381 CM01AE1
CMDT2382 CM01AE2
CMDT2391 CM01AF1
CMDT2392 CM01AF2
CMDT2401 CM01AG1
CMDT2402 CM01AG2
CMDT2411 CM01AH1
CMDT2412 CM01AH2
CMDT2421 CM01AI1
CMDT2422 CM01AI2
CMDT2431 CM01AJ1
CMDT2432 CM01AJ2
CMDT2441 CM01AK1
CMDT2442 CM01AK2
CMDT2451 CM01AL1
CMDT2452 CM01AL2
CMDT2461 CM01AM1
CMDT2462 CM01AM2
CMDT2471 CM01AN1
CMDT2472 CM01AN2
CMDT2481 CM01AO1
CMDT2482 CM01AO2
CMDT2491 CM01AP1
CMDT2492 CM01AP2
CMDT2501 CM01AQ1
CMDT2502 CM01AQ2
CMDT2511 CM01AR1
CMDT2512 CM01AR2
CMDT2521 CM01AS1
CMDT2522 CM01AS2
CMDT2531 CM01AT1
CMDT2532 CM01AT2
CMDT2541 CM01AU1
CMDT2542 CM01AU2
CMDT2551 CM01AV1
CMDT2552 CM01AV2
CMDT2561 CM01AW1
CMDT2562 CM01AW2
CMDT2571 CM01AX1
CMDT2572 CM01AX2
CMDT2581 CM01AY1
CMDT2582 CM01AY2
CMDT2591 CM01AZ1
CMDT2592 CM01AZ2
CMDT2601 CM01BA1
CMDT2602 CM01BA2
CMDT2611 CM01CA1
CMDT2612 CM01CA2
CMDT2621 CM01DA1
CMDT2622 CM01DA2
CMDT2631 CM01EA1
CMDT2632 CM01EA2
CMDT2641 CM01FA1
CMDT2642 CM01FA2
CMDT2651 CM01GA1
CMDT2652 CM01GA2
CMDT2661 CM01HA1
CMDT2662 CM01HA2
CMDT2671 CM01IA1
CMDT2672 CM01IA2
CMDT2681 CM01JA1
CMDT2682 CM01JA2
CMDT2691 CM01KA1
CMDT2692 CM01KA2
CMDT2701 CM01LA1
CMDT2702 CM01LA2
CMDT2711 CM01MA1
CMDT2712 CM01MA2
CMDT2721 CM01NA1
CMDT2722 CM01NA2
CMDT2731 CM01OA1
CMDT2732 CM01OA2
CMDT2741 CM01PA1
CMDT2742 CM01PA2
CMDT2751 CM01QA1
CMDT2752 CM01QA2
CMDT2761 CM01RA1
CMDT2762 CM01RA2
CMDT2771 CM01SA1
CMDT2772 CM01SA2
CMDT2781 CM01VA1
CMDT2782 CM01VA2
CMDT2791 CM01WA1
CMDT2792 CM01WA2
CMDT2801 CM01XA1
CMDT2802 CM01XA2
CMDT2811 CM01YA1
CMDT2812 CM01YA2
CMDT2821 CM01ZA1
CMDT2822 CM01ZA2
CMDT2831 CM01AA1
CMDT2832 CM01AA2
CMDT2841 CM01AB1
CMDT2842 CM01AB2
CMDT2851 CM01AC1
CMDT2852 CM01AC2
CMDT2861 CM01AD1
CMDT2862 CM01AD2
CMDT2871 CM01AE1
CMDT2872 CM01AE2
CMDT2881 CM01AF1
CMDT2882 CM01AF2
CMDT2891 CM01AG1
CMDT2892 CM01AG2
CMDT2901 CM01AH1
CMDT2902 CM01AH2
CMDT2911 CM01AI1
CMDT2912 CM01AI2
CMDT2921 CM01AJ1
CMDT2922 CM01AJ2
CMDT2931 CM01AK1
CMDT2932 CM01AK2
CMDT2941 CM01AL1
CMDT2942 CM01AL2
CMDT2951 CM01AM1
CMDT2952 CM01AM2
CMDT2961 CM01AN1
CMDT2962 CM01AN2
CMDT2971 CM01AO1
CMDT2972 CM01AO2
CMDT2981 CM01AP1
CMDT2982 CM01AP2
CMDT2991 CM01AQ1
CMDT2992 CM01AQ2
CMDT3001 CM01AR1
CMDT3002 CM01AR2
CMDT3011 CM01AS1
CMDT3012 CM01AS2
CMDT3021 CM01AT1
CMDT3022 CM01AT2
CMDT3031 CM01AU1
CMDT3032 CM01AU2
CMDT3041 CM01AV1
CMDT3042 CM01AV2
CMDT3051 CM01AW1
CMDT3052 CM01AW2
CMDT3061 CM01AX1
CMDT3062 CM01AX2
CMDT3071 CM01AY1
CMDT3072 CM01AY2
CMDT3081 CM01AZ1
CMDT3082 CM01AZ2
CMDT3091 CM01BA1
CMDT3092 CM01BA2
CMDT3101 CM01CA1
CMDT3102 CM01CA2
CMDT3111 CM01DA1
CMDT3112 CM01DA2
CMDT3121 CM01EA1
CMDT3122 CM01EA2
CMDT3131 CM01FA1
CMDT3132 CM01FA2
CMDT3141 CM01GA1
CMDT3142 CM01GA2
CMDT3151 CM01HA1
CMDT3152 CM01HA2
CMDT3161 CM01IA1
CMDT3162 CM01IA2
CMDT3171 CM01JA1
CMDT3172 CM01JA2
CMDT3181 CM01KA1
CMDT3182 CM01KA2
CMDT3191 CM01LA1
CMDT3192 CM01LA2
CMDT3201 CM01MA1
CMDT3202 CM01MA2
CMDT3211 CM01NA1
CMDT3212 CM01NA2
CMDT3221 CM01OA1
CMDT3222 CM01OA2
CMDT3231 CM01PA1
CMDT3232 CM01PA2
CMDT3241 CM01QA1
CMDT3242 CM01QA2
CMDT3251 CM01RA1
CMDT3252 CM01RA2
CMDT3261 CM01SA1
CMDT3262 CM01SA2
CMDT3271 CM01VA1
CMDT3272 CM01VA2
CMDT3281 CM01WA1
CMDT3282 CM01WA2
CMDT3291 CM01XA1
CMDT3292 CM01XA2
CMDT3301 CM01YA1
CMDT3302 CM01YA2
CMDT3311 CM01ZA1
CMDT3312 CM01ZA2
CMDT3321 CM01AA1
CMDT3322 CM01AA2
CMDT3331 CM01AB1
CMDT3332 CM01AB2
CMDT3341 CM01AC1
CMDT3342 CM01AC2
CMDT3351 CM01AD1
CMDT3352 CM01AD2
CMDT3361 CM01AE1
CMDT3362 CM01AE2
CMDT3371 CM01AF1
CMDT3372 CM01AF2
CMDT3381 CM01AG1
CMDT3382 CM01AG2
CMDT3391 CM01AH1
CMDT3392 CM01AH2
CMDT3401 CM01AI1
CMDT3402 CM01AI2
CMDT3411 CM01AJ1
CMDT3412 CM01AJ2
CMDT3421 CM01AK1
CMDT3422 CM01AK2
CMDT3431 CM01AL1
CMDT3432 CM01AL2
CMDT3441 CM01AM1
CMDT3442 CM01AM2
CMDT3451 CM01AN1
CMDT3452 CM01AN2
CMDT3461 CM01AO1
CMDT3462 CM01AO2
CMDT3471 CM01AP1
CMDT3472 CM01AP2
CMDT3481 CM01AQ1
CMDT3482 CM01AQ2
CMDT3491 CM01AR1
CMDT3492 CM01AR2
CMDT3501 CM01AS1
CMDT3502 CM01AS2
CMDT3511 CM01AT1
CMDT3512 CM01AT2
CMDT3521 CM01AU1
CMDT3522 CM01AU2
CMDT3531 CM01AV1
CMDT3532 CM01AV2
CMDT3541 CM01AW1
CMDT3542 CM01AW2
CMDT3551 CM01AX1
CMDT3552 CM01AX2
CMDT3561 CM01AY1
CMDT3562 CM01AY2
CMDT3571 CM01AZ1
CMDT3572 CM01AZ2
CMDT3581 CM01BA1
CMDT3582 CM01BA2
CMDT3591 CM01CA1
CMDT3592 CM01CA2
CMDT3601 CM01DA1
CMDT3602 CM01DA2
CMDT3611 CM01EA1
CMDT3612 CM01EA2
CMDT3621 CM01FA1
CMDT3622 CM01FA2
CMDT3631 CM01GA1
CMDT3632 CM01GA2
CMDT3641 CM01HA1
CMDT3642 CM01HA2
CMDT3651 CM01IA1
CMDT3652 CM01IA2
CMDT3661 CM01JA1
CMDT3662 CM01JA2
CMDT3671 CM01KA1
CMDT3672 CM01KA2
CMDT3681 CM01LA1
CMDT3682 CM01LA2
CMDT3691 CM01MA1
CMDT3692 CM01MA2
CMDT3701 CM01NA1
CMDT3702 CM01NA2
CMDT3711 CM01OA1
CMDT3712 CM01OA2
CMDT3721 CM01PA1
CMDT3722 CM01PA2
CMDT3731 CM01QA1
CMDT3732 CM01QA2
CMDT3741 CM01RA1
CMDT3742 CM01RA2
CMDT3751 CM01SA1
CMDT3752 CM01SA2
CMDT3761 CM01VA1
CMDT3762 CM01VA2
CMDT3771 CM01WA1
CMDT3772 CM01WA2
CMDT3781 CM01XA1
CMDT3782 CM01XA2
CMDT3791 CM01YA1
CMDT3792 CM01YA2
CMDT3801 CM01ZA1
CMDT3802 CM01ZA2
CMDT3811 CM01AA1
CMDT3812 CM01AA2
CMDT3821 CM01AB1
CMDT3822 CM01AB2
CMDT3831 CM01AC1
CMDT3832 CM01AC2
CMDT3841 CM01AD1
CMDT3842 CM01AD2
CMDT3851 CM01AE1
CMDT3852 CM01AE2
CMDT3861 CM01AF1
CMDT3862 CM01AF2
CMDT3871 CM01AG1
CMDT3872 CM01AG2
CMDT3881 CM01AH1
CMDT3882 CM01AH2
CMDT3891 CM01AI1
CMDT3892 CM01AI2
CMDT3901 CM01AJ1
CMDT3902 CM01AJ2
CMDT3911 CM01AK1
CMDT3912 CM01AK2
CMDT3921 CM01AL1
CMDT3922 CM01AL2
CMDT3931 CM01AM1
CMDT3932 CM01AM2
CMDT3941 CM01AN1
CMDT3942 CM01AN2
CMDT3951 CM01AO1
CMDT3952 CM01AO2
CMDT3961 CM01AP1
CMDT3962 CM01AP2
CMDT3971 CM01AQ1
CMDT3972 CM01AQ2
CMDT3981 CM01AR1
CMDT3982 CM01AR2
CMDT3991 CM01AS1
CMDT3992 CM01AS2
CMDT4001 CM01AT1
CMDT4002 CM01AT2
CMDT4011 CM01AU1
CMDT4012 CM01AU2
CMDT4021 CM01AV1
CMDT4022 CM01AV2
CMDT4031 CM01AW1
CMDT4032 CM01AW2
CMDT4041 CM01AX1
CMDT4042 CM01AX2
CMDT4051 CM01AY1
CMDT4052 CM01AY2
CMDT4061 CM01AZ1
CMDT4062 CM01AZ2
CMDT4071 CM01BA1
CMDT4072 CM01BA2
CMDT4081 CM01CA1
CMDT4082 CM01CA2
CMDT4091 CM01DA1
CMDT4092 CM01DA2
CMDT4101 CM01EA1
CMDT4102 CM01EA2
CMDT4111 CM01FA1
CMDT4112 CM01FA2
CMDT4121 CM01GA1
CMDT4122 CM01GA2
CMDT4131 CM01HA1
CMDT4132 CM01HA2
CMDT4141 CM01IA1
CMDT4142 CM01IA2
CMDT4151 CM01JA1
CMDT4152 CM01JA2
CMDT4161 CM01KA1
CMDT4162 CM01KA2
CMDT4171 CM01LA1
CMDT4172 CM01LA2
CMDT4181 CM01MA1
CMDT4182 CM01MA2
CMDT4191 CM01NA1
CMDT4192 CM01NA2
CMDT4201 CM01OA1
CMDT4202 CM01OA2
CMDT4211 CM01PA1
CMDT4212 CM01PA2
CMDT4221 CM01QA1
CMDT4222 CM01QA2
CMDT4231 CM01RA1
CMDT4232 CM01RA2
CMDT4241 CM01SA1
CMDT4242 CM01SA2
CMDT4251 CM01VA1
CMDT4252 CM01VA2
CMDT4261 CM01WA1
CMDT4262 CM01WA2
CMDT4271 CM01XA1
CMDT4272 CM01XA2
CMDT4281 CM01YA1
CMDT4282 CM01YA2
CMDT4291 CM01ZA1
CMDT4292 CM01ZA2
CMDT4301 CM01AA1
CMDT4302 CM01AA2
CMDT4311 CM01AB1
CMDT4312 CM01AB2
CMDT4321 CM01AC1
CMDT4322 CM01AC2
CMDT4331 CM01AD1
CMDT4332 CM01AD2
CMDT4341 CM01AE1
CMDT4342 CM01AE2
CMDT4351 CM01AF1
CMDT4352 CM01AF2
CMDT4361 CM01AG1
CMDT4362 CM01AG2
CMDT4371 CM01AH1
CMDT4372 CM01AH2
CMDT4381 CM01AI1
CMDT4382 CM01AI2
CMDT4391 CM01AJ1
CMDT4392 CM01AJ2
CMDT4401 CM01AK1
CMDT4402 CM01AK2
CMDT4411 CM01AL1
CMDT4412 CM01AL2
CMDT4421 CM01AM1
CMDT4422 CM01AM2
CMDT4431 CM01AN1
CMDT4432 CM01AN2
CMDT4441 CM01AO1
CMDT4442 CM01AO2
CMDT4451 CM01AP1
CMDT4452 CM01AP2
CMDT4461 CM01AQ1
CMDT4462 CM01AQ2
CMDT4471 CM01AR1
CMDT4472 CM01AR2
CMDT4481 CM01AS1
CMDT4482 CM01AS2
CMDT4491 CM01AT1
CMDT4492 CM01AT2
CMDT4501 CM01AU1
CMDT4502 CM01AU2
CMDT4511 CM01AV1
CMDT4512 CM01AV2
CMDT4521 CM01AW1
CMDT4522 CM01AW2
CMDT4531 CM01AX1
CMDT4532 CM01AX2
CMDT4541 CM01AY1
CMDT4542 CM01AY2
CMDT4551 CM01AZ1
CMDT4552 CM01AZ2
CMDT4561 CM01BA1
CMDT4562 CM01BA2
CMDT4571 CM01CA1
CMDT4572 CM01CA2
CMDT4581 CM01DA1
CMDT4582 CM01DA2
CMDT4591 CM01EA1
CMDT4592 CM01EA2
CMDT4601 CM01FA1
CMDT4602 CM01FA2
CMDT4611 CM01GA1
CMDT4612 CM01GA2
CMDT4621 CM01HA1
CMDT4622 CM01HA2
CMDT4631 CM01IA1
CMDT4632 CM01IA2
CMDT4641 CM01JA1
CMDT
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RESIDENT ROUTINES

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```

1      TITLE RESIDENT ROUTINE
2
3      0031054 0000200
4
5      0031054 0000200
6      0031054 0000200
7      0031054 0000200
8      0031054 0000200
9      0031054 013737 177776 1400026  ENTRY#; MOV #PSS, #EXPSSAV
10     0031054 013737 177776 1400026  ENTRY#; MOV #PSS, #EXPSSAV
11     0031054 010567 0000020 0000020  ISAVE PSS WITH I-CODE
12     0031054 010567 0000020 0000020  IIN SIMULATE JSW
13     0031054 012342 0000000 0000000  INDICATE GROUP INDEX
14     0031054 012342 0000000 0000000  AR DISP
15
16
17
18
19     0031054 013737 177776 1400026  ENTRY#; MOV #PSS, #EXPSSAV
20     0031054 010567 0000020 0000020  ISAVE PSS WITH I-CODE
21     0031054 010567 0000020 0000020  IIN SIMULATE JSW
22     0031054 000015 0000001 0000001  INDICATE GROUP INDEX
23     0031054 012342 0000001 0000001  AR DISP
24     0031054 0000311
25
26
27
28
29     0031054 013737 177776 1400026  ENTRY#; MOV #PSS, #EXPSSAV
30     0031054 0000100 1600000 0000000  ISAVE PSS WITH I-CODE
31     0031054 0000100 1600000 0000000  IIN SIMULATE JSW
32     0031054 010767 0000000 0000000  AR DISP
33     0031054 010767 0000000 0000000  AR DISP
34     0031054 0000001 0000001 0000001  AR DISP
35     0031054 0000001 0000001 0000001  AR DISP
36
37
38     0031054 2000200 0000000 0000000  SAVE:   NOP
39     0031054 0000000 0000000 0000000  ISAVE GPRS
40     0031054 012175 1400012 0000000  MOV #XHGTGR, RS
41     0031054 012175 1400012 0000000  MOV R0, (RS)+*
42     0031054 010162 010125 0000000  MOV R1, (RS)+*
43     0031054 010162 010125 0000000  MOV R2, (RS)+*
44     0031054 010162 010125 0000000  MOV R3, (RS)+*
45     0031054 010170 0000000 0000000  ADD 20, #EJADN
46     0031054 010170 0000000 0000000  ADD 20, #EJADN
47     0031054 0000000 0000000 0000000  IIN BEYOND OR INSTR
48     0031054 0000000 0000000 0000000  IIN SIMULATE RTS

```

EVENT HANDLER DISPATCH RT-11 MACRO VM82-09

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1 .TITLE EVENT HANDLER DISPATCH
2 ======
3
4 003204 000240 DISPI NOP
5 003204 005004 CLR R4 IFLAG REGISTER
6
7
8 003210 010601
9 003212 002701 100000 BIC #1000000,RI
10 003210 020127 000500 CMP RI,-4,R1
11 003222 100004 BPL SVSTK
12 003224 052704 000001 BIS #1,RI
13 003230 012701 001000 MOV #1000,RI
14 003234 010106 MOV RI,SP
15 003236 005111 CLR (RT)
16 003246 010607 003602 SVSTK: MOV SP,ULUSTK
17 003244 012706 134000 MOV ULNEWSTK,SP
18)
19
20 003250 072027 000004 ASH #4,RI
21 003254 042737 177/60 140026 BIC #17/760,EXPSSAV
22 003262 003700 140026 ADD EXPSSAV,RI
23 003266 0100A5 MOV RI,RS
24 003270 000240 NOP
25 003272 010237 177570 MOV RI,#177570 ITFT
26
27
28 003276 006300 ASL #6
29 003300 004770 137304 JSR PC,EXUSPTB(a)
30 003304 .BUFOUT
31
32
33 003314 000240 RESTOR: NOP
34 003310 006305 ASL RS
35 003320 006305 ASL RS
36 003322 010500 MOV RS,RI
37 003324 016701 003556 MOV OLUSTK,RI
38 003334 162701 000004 SUB #4,RI
39 003334 010167 003546 MOV RI,OLUSTK
40 003340 016021 137412 MOV YVELSV(RI),(R1)+
41 003344 045720 TST (R1)+
42 003346 016011 137412 MOV YVELSV(RI),(R1)
43 003352 000767 000750 JSR PC,UNSAVE
44 003356 016706 003524 MOV OLUSTK,SP
45 003362 000240 NOP
46 003364 105767 002530 TSTG TRAP
47 003370 001403 RD RESTRI
48 003372 105667 002522 CLR# TRAP
49 004376 012700 003536 MOV #...KA
50 004342 104350 EHT 331
51 004340 000002 RESTRI: RTS
52)
14* EVENT CODE
FOLD STACK AND
FINISH FOR ADDITIONAL VECTOR
SAVE STACK AND FOR RTS
MOVE SAVED VECTOR ON STACK
JRFST SP
ISET H83/% FOR .EXIT
RETURN TO SYSTEM

```

1           .TITLE CONTROL COMMAND HANDLER
2           ****
3           ****
4           ****
5 003406      EXDISPE IDISPATCHER FOR SUPERVISOR COMMANDS
6           ****
7           ****
8 003406 005224          CLR R4
9 003410 010667 003472          MOV SP,OLDSTK      ;SAVE STACK
10 003414 012736 134000          MOV #XEA5TK,SP    ;SET NEW STACK
11 003428          REVWHD
12 003432 012737 000777 177570          MOV #777,#177570   ;TEST
13 003440 004770 137400          JSR PC,EXDSP1C(0) ;DISPATCH SUPERVISOR COMMAND
14 003444 000256          JSR PC,LSAVE
15 003450 016786 003432          MOV OLDSTK,SP
16 003454 002737 000100 164000          BIS #10,PC=COMCHI ;ENABLE SUP. INTENR.
17 003462 000002          RTI                   ;RETURN TO SYSTEM
18
19
20 003464      HANG:  ;WAITLOOP FOR FURTHER SUP. CMDS
21
22
23 003464          REVARD
24 003470 004770 137400          JSR PC,EXDSP2(0)   ;WAIT FOR A CMD
25 003502 000297          CONT:  RTS PC       ;DISPATCH NEXT CMD
26
27
28 003504      TABUP0: ;UPDATE OF MONITOR TABLES
29
30 003504 012737 000047 177570          MOV #7,#177570   ;TEST
31 003512 005237 140004          INC #XDIRH
32 003516 004767 001552          JSR PC,EXCH
33 003522 012731 137170          MOV #XDIRH,R1
34 003526 012732 137304          MOV #1#XDCM+2,R2
35 003532 012100          MOV (1)+,R2
36 003534          SND-RD
37 003546 020192          CMP R1,R2
38 003553 003370          BNE TABUP1
39 003552 012737 000070 177570          MOV #7#177570   ;TEST
40 003560          REVARD
41 003572 022700 000006          INC #XDIRH
42 003576 0014P1          BNE TABUP2
43 003600 000000
44 003632 012701 137170          TABUP2: MOV #XHSD,R1
45 003606 012702 137304          MOV #XENDCM+2,R2
46 003612 012737 000700 177570          MOV #7P2,#177570   ;TEST
47 003620          TABUP3: REVARD
48 003632 010021          MOV R1,(1)+
49 003634 020192          CMP R1,R2
50 003636 001373          BNE TABUP3
51 003640 012737 007000 177570          MOV #7P2,#177570   ;TEST
52 003646 022722 000003          CMP R1,R2
53 003652 001401          REQ TABUP4
54 003654 000000
55 003656 005057 148030          HALT
56 003662 005777 157266          TABUP4: CLR #XDTA
57 003666 001406          TST #XINTENR
                                BEQ TABUP5

```

CONTROL COMMAND HANDLER RT-1.1 MACRO VM02-09 00:11:26 PAGE 7+

58 003678 013737 137276 000104 MOV #EXTINT1, #0104
59 003676 013737 137300 000106 MOV #EXTINT2, #0106
60 003704 004767 001364 TABUPSI JSR PC, EXCH
61 005710 013737 137274 172542 MOV #EXTHEG2, #BTBUF
62 003716 015737 137272 172540 MOV #EXTHEG1, #BTSTAT
63 005724 002207 RTS PC
64
65
66
67 003726 000249 UNSAVE: NOP
68 005750 012775 140012 MOV #XREGd, RS
69 003734 012500 MOV (RS)+, R0
70 005736 012501 MOV (RS)+, R1
71 005740 012502 MOV (RS)+, R2
72 003742 012503 MOV (RS)+, P3
73 005744 012504 MOV (RS)+, R4
74 005746 016705 003126 MOV REG5, RS
75 003752 000207 RTS PC
76
77
78 003754 ENDRUN: (RESET SYSTEM) TERMINATE MONITORING SESSION
79 *****
80
81 003754 012706 134000 MOV #NEWSTK, SP
82 003760 012737 000001 140050 MOV #1, #XD1R
83 003766 004767 001302 JSR PC, EXCH
84 003772 005037 172540 CLR PATSTAT
85 003776 005037 164000 CLR #COMCH1
86 004002 004767 177720 JSR PC, UNSAVE
87 004206 016706 003074 MOV OLDSTA, SP
88
89 004012 005008 CLR R0
90 004014 .EXIT
91

150

INIT SYSTEM AT .EXIT

EVENT HANDLERS RT-11 MACHO YM02-09

0011126 PAGE 5

1 .TITLE EVENT HANDLERS
2 *****
3
4
5 0044816
6
7 004016 004767 001024
8 004022 012700 137030
9 004426
10 004332 000207
11
12
13 004034
14
15
16 004234 000767 001006
17 004040 016701 002210
18 004044 012702 000001
19 004450 P20205
20 004052 001040
21 004454 012127 177775
22 004060 005202
23 004062 002772
24 004064 032701 000001
25 004070 001043
26 004072 004467 000770
27 004076 002008
28 004130 P32701 000002
29 004104 001402
30 004135 004767 001000
31 004112 P32701 000000
32 004116 001040
33 004120 004767 001014
34 004124 004767 001120
35 004130 P20207 000003
36 004134 P22007
37 004136 145267 001756
38 004142 000207
39
40
41 004144
42
43
44 004144 00701 002106
45 004150 012702 137224
46 004154 022705 000006
47 004160 001043
48 004162 000501
49 004164 002702 000010
50 004174 002701 000001
51 004174 001043
52 004176 004767 000036
53 004202 000207
54
55 004204 017703 002676
56
57 004204 017703 002676

RES: IDISPATCH ERROR, WRONG EV CODE
RES: JSR PC,ECOUT ISEND EVENT CODE
RES: MOV #XQUES,R0 ISEND QUESTION MARK
RES: CHOUT RETURN FROM DE
RES: RTS PC
RES: *****
RES: SG001: IEV1-EV5: TRAP 4,TRAP 16, RPT, ID1, PAPL
RES: ISELECTION: PC,PS,SP
RES: JSR PC,ECOUT ISEND EVENT CODE
RES: MOV MSK005,R1 IGET SPEC MASK
RES: MOV #1,K2 STARTING WITH EV 1
RES: CMP R2,R5 ILLOOK FOR EV CODE
RES: REQ SG002
RES: ASH #3,R1 ISHIFT 3 RIGHT
RES: INC R2
RES: BR SG001
RES: BIT #1,K1 IFEV?
RES: BEQ SG003 IMO
RES: JSR R4,PCOUT
RES: LDRO 0
RES: SG003: BIT #2,K1 IFPS?
RES: BEQ SG004 IMO
RES: JSR PC,PSOUT
RES: SG004: BIT #4,K1 IFP?
RES: BEQ SG005 IMO
RES: JSR PC,SPOUT
RES: SG005: BIT #5,K3 IFAS IT EV.1 OR 2?
RES: BEQ SG026 IMO
RES: INC# TRAP
RES: SG006: RTS PC RETURN FROM SG008
RES: *****
RES: SG011: IEV6-EV7 EMT, TRAP - WITH SUR SELECTION
RES: ISELECTION : PC=2, PS, SP, (PC-2), (S<)=EMT ONLY
RES: MOV MSK007,R1 IGET MASK
RES: MOV #X5,000,R2 IGET AHDR, OF 1ST SEL BYTE
RES: CMP #6,N5 DETERMINE IF 6 OR 7
RES: BEQ SG011
RES: SAB R1 ISHIFT EV7 MASK IN LOW BYTE
RES: ADD #8,R2 IF 8 SEL BYTES PER EV ??
RES: SG011: BIT #1,K1 ISELECTION?
RES: BEQ SG012 IFYES-GOTO SUBSELECTION
RES: JSR PC,SG012 IMO-GOTO REPORT PROCESSING
RES: RTS PC RETURN FROM SG011
RES: *****
RES: SG012: PSUBSELECTOR
RES: *****
RES: MOV SOLUSLK,RS IGET EMT/TRAP CODE

EVENT HANDLERS RT=11 MACRO VM82-09 00111126 PAGE 8+

```

58 004210 005743      TST -(3)          REV INSTR., SEL INSTR.?
59 004212 011303      MOV (3),R3      END
60 004214 000240      NOP
61 004216 1d4312      CMPB R3,(2)
62 004220 001003      BLE SG010
63 004222 004767 000012  JSR PC,SG01A
64 004226 000207      RTS PC
65 004230 005202      INC R2
66 004232 1d5712      TSTB (2)
67 004234 001367      BLE SG013
68 004236 000207      RTS PC
69
70 000240
71
72 004240 004767 000602  ;*** REPORT PROCESSING FOR SG01 ***
73 004244 032701 000002  ;SEL EVENT CODE?
74 004250 001403      BEQ SG01A1
75 004252 004467 000610  JSR R4,PCOUT
76 004254 000002      ,WHDN 2
77 004260 032701 000004  ;PC?
78 004264 001402      BEQ SG01A2
79 004266 004767 000620  JSR PC,PSOUT
80 004272 032701 000010  ;SP?
81 004276 001402      BEQ SG01A3
82 000300 004767 000630  JSR PC,SPOUT
83 004304 032701 000020  ;(PC-B)?
84 004310 001403      BEQ SG01A4
85 004312 004467 000644  JSR R4,PCOUT
86 004316 000002      ,WHDN 2
87 004320 032701 000040  ;PC-2
88 004324 001402      BEQ SG01A5
89 004326 012700 137002  PEG SG01A5
90 004332
91 004336 013700 000052  MOV #x52,R0
92 004342
93 004346 004767 000676  ;CHDUT
94 004352 000207      MOV #x52,R0
                           ;GCOUT
                           ;RTS PC
                           ;RETURN FROM SG01A
95
96
97 004354
98
99
100 004356 010500      SG101: REV20-EV21: TK, TP, PR, PP, KW11-P.
101 004356 0042700 177771  J*****: ;SELECTION! PL,PS, SP, (REG), (BUF).
102 004362 016201 137204
103 004366 032705 000001
104 004372 001401
105 004374 002301
106 004376 010503
107 004410 006303
108 004402 004767 000640
109 004406 032701 000002
110 004412 001403
111 004414 004467 000446
112 004420 00P040
113 004422 032701 000004
114 004420 001402      SG102: MOV R5,RM
                           RIC #17771,R0
                           MOV #x5101(0),R1
                           BIT #1,R5
                           BEQ SG102
                           SWAB R1
                           ASL R3
                           JSR PC,ECOUT
                           BIT #2,R1
                           BEQ SG102
                           JSR R4,PCOUT
                           ,WHDN 0
                           BIT #4,R1
                           BEQ SG102
                           ;PC OF NEXT INSTR.
                           ;PC?
                           ;END
                           ;RTS PC
                           ;RETURN FROM SG01A

```

EVENT HANDLERS RT-11 MACRO VM92-89

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115 00443d 034767 000456
 116 004434 032701 00001d
 117 00444d 001402
 118 004442 034767 000472
 119 00444d 032701 000020
 120 004452 001406
 121 004454 001732 137712
 122 004463 004467 000544
 123 004464 000000 200
 124 004465 000000 200
 125 00447d 032701 000040
 126 004474 001412
 127 004476 000002 137712
 128 004502 000000 200
 129 00453d 001122
 130 00453d 004467 000516
 131 004512 000000 200
 132 004514 000000 200
 133 004516 004467 000526
 134 004522 004467
 135
 136
 137 004524
 138
 139
 140 004524 0016721 0001500
 141 00453d 001146
 142 004532 032701 000001
 143 004536 001114
 144 00454d 0012621
 145 004542 004467 000300
 146 004546 000000 200
 147 00455d 032701 000001
 148 004559 000000 200
 149 00455d 004467 000300
 150 004562 000000 200
 151 004564 000001
 152 004566 032701 000001
 153 004572 001402
 154 004574 004467 000312
 155 00460d 000001
 156 004602 032701 000001
 157 004606 001402
 158 004610 000000 200
 159 004614 001203 000000
 160 004620 000000 200
 161 004622 000000 200
 162 004624 0016505 137712
 163 00463d 000000 200
 164 004632 032701 000001
 165 004636 001412
 166 004660 001367 000015
 167 004604 000000 200
 168 004650 001416
 169 004652 001122
 170 00465d 004467 000350
 171 00467d 000000 200

JSR PC,PSOUT
 SG1021 BIT #14,R1
 BEQ SG103
 JSR PC,SPOUT
 SG1031 BIT #20,R1
 BEQ SG104
 MOV #0,STAT(3),R2
 JSR R4,REGOUT
 .BYTE 46,200
 .WORD 0
 SG1041 BIF #40,W1
 BEQ SG105
 MOV #0,STAT(3),R2
 TST (2)+
 MOV (21),R2
 JSR R4,REGOUT
 .BYTE 47,200
 .WORD 0
 JSR PC,11HOUT
 RTS PC
 ;RETURN FROM SG10
 ;
 ;
 SG1051 JEV301 RK DISK1 WITH SUB SELECTOR
 ;SEL1 PC, PS, SP, REGs...REGs,
 ;
 MOV #5K110,W1
 MOV R1,-(SP)
 BIT #1,W1
 HNE SG117
 SG1101 MOV (SP)+,R1
 JSR PC,ECOUNT
 ;SEND EVENT CODE
 ASR R1
 BIT #1,W1
 BEQ SG111
 JSR R4,REGOUT
 .WORD 0
 SG1111 ASW R1
 BIT #1,W1
 BEQ SG112
 JSR PC,PSOUT
 SG1121 ASR R1
 BIT #1,W1
 BEQ SG113
 JSR PC,SPOUT
 SG1131 MOV #60,R2
 MOV R5,-(SP)
 ASL R5
 MOV XDSTAT(5),RS
 SG1141 ASR R1
 BIT #1,W1
 BEQ SG116
 MOVB RS,SG115+1
 CMP L65,RS
 BEQ SG114A
 MOV (5),R2
 JSR R4,REGOUT
 SG114C1 .BYTE 5F,0

EVENT HANDLERS RT=1 MACRO VH02-09

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172 004662 043 200
173 004664 005725
174 004666 005235
175 004670 022773 000066
176 004674 001355
177 004676 004161 000546
178 004702 012e75
179 004704 000f27

SG1161 TST (5)+
INC R3
CMP #65,R3
BNE SG114
JSR PC,TIMOUT
MOV (SP)+,R5
RTS PC

RETURNS FROM SG111

180
181 004706 **** COMPUTE BLOCK NO. (LAST BLK+1 OF ACCESSFD FILF)***
182
183
184 004706 010146
185 004710 010500
186 004712 022324
187 004714 011670
188 004716 010525
189 004720 072127 177773
190 004724 002771 177400
191 004730 005371
192 004732 006371
193 004734 032773 000020
194 004740 001401
195 004742 005201
196 004744 070127 700014
197 004750 002702 177760
198 004754 000401
199 004756 002701 200030
200 004762 010102
201 004764 012601
202 004766 000732

SG1148 MUL #14,R1
BIC #177760,R6
ADD R6,R1
ADD #30,R1
MOV R1,R2
MOV (SP)+,R1
BR SG114C

SHFT CYL ADDR. RIGHT BOUNDED
DEC R1
ASL R1
BIT #20,R0
REQ SG114B
INC R1
ADD 1 TRACK
#14
MASK SECTOR
ADD SECTOR
ADD FOR DIRECTORY OF 2 TRACKS
READY TO SEND STUFF OUT

190 BACK FOR OUTPUT
END OF BLOCK NUMBER CALCULATION

203
204
205
206 004770
207
208 004770 010500
209 004772 006302
210 004774 016003 157712
211 005000 012731 137246
212 005004 012772 200004
213 005010 012103
214 005012 006303
215 005014 000003
216 005016 011304
217 005020 004214
218 005022 021304
219 005024 001245
220 005026 017213
221 005030 012601
222 005032 000277

SG1171 ****SUB SELECTOR FOR EV30****

SG1181 MOV (17)+,R3
ASL R3
MOV X05STAT(0),R0
MOV #4\$1100,R1
MOV #4,R2
INC R1
SHFT REG NO.

ADD R0,R3
MOV (3),R4
BIC (1)+,R4
CMP (3),R4
BNE SG1110
SCB Rd,SG118
MOV (SP)+,R1
RTS PC

REG. ADDR.
REG. COUNT.
END ALL "0X".

REPORT PROCESSING
END IF 4 FILES
END FV REPORT PRODUCED-CORR. STACK
RETURN FROM SG11

223
224
225 005034
226
227 005034 004767 000006
228 005040 004767 000269
229 005044 000277

SG121 JSR PC,ECOUT
SG122 JSR PC,TIMOUT
RTS PC

154

```

1      1 TITLE BUFFER ROUTINES
2      2 *****+
3      3
4      4
5 005046
6 045006 012700 136440
7 0050452
8 0050456 010500
9 0050464 010227
10 0050464 200227
11 0050464 200227
12
13
14 0050466
15
16 0050466 012700 137032
17 0050472
18 0050476 017100 002600
19 005102 102400
20 005104
21 005110 000200
22
23
24 005112
25
26 005112 012700 137034
27 005116
28 005122 016700 0001700
29 005126 005720
30 005130 011000
31 005132
32 005136 020207
33
34
35 005140
36
37 005140 012700 137036
38 005144
39 005148 016700 0001732
40 005154
41 005160 000207
42
43
44 005162
45
46 005162 012700 137040
47 005166
48 005172 017100 001710
49 005176 102400
50 005200 002700 0000001
51 005204 001405
52 005208 012700 137020
53 005214
54 005216 000403
55 005220 011004
56 005222
57 005226 020204

*****+
ECOUT: T OUTPUT OF EVENT CODE; LINKAGE: PC
*****+
MOV #XCRLF,R0
.CHOUT
MOV HS,R0
.OCOUT
RTS PC
LOG EVENT CODE
RETURNS FROM ECOUT

*****+
PCOUT: T OUTPUT OF PC-K; K1ST ARG.; LINKAGE: R4
*****+
MOV #XMPC,R0
.TSEND 1 FOR PC
.CHOUT
MOV #OLDSTK,R0
.SGET EV-PC-K
SUB (4)+,R0
JUSE 1ST ARG,
.OCOUT
RTS R4
RETURNS FROM PCOUT

*****+
PSOUT: T OUTPUT OF EVENT PSA; LINKAGE: PC
*****+
MOV #XMPS,R0
.TSEND * FOR PS
.CHOUT
MOV #OLDSTK,R0
.SGET EV PS
TST (R1)
MOV (R1),R0
.OCOUT
RTS PC
RETURNS FROM PSOUT

*****+
SPOUT: T OUTPUT OF EVENT SP; LINKAGE: PC
*****+
MOV #XMSP,R0
.TSEND * FOR EVENT SP
.CHOUT
MOV #OLDSTK,R0
.OCOUT
RTS PC
RETURNS FROM SPOUT

*****+
CPCOUT: T OUTPUT OF EVENT (PC-K); LINKAGE: R4
*****+
MOV #XMPC,R0
.TSEND 3 FOR (PC-K)
.CHOUT
MOV #OLDSTK,R0
SUB (4)+,R0
TST ARG,
JPC 0002
BEQ CPC01
MOV #XAST,R0
.TYES-SEND *PARA
.CHOUT
BH CPC02
MOV (R1),R0
.OCOUT
RTS R4
RETURNS FROM CPCOUT

```

BUFFER ROUTINES RT-17 MACRO VM02-09

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58				
59				
60	005239			
61				
62				
63	005230	010000		
64	005232			
65	005230	022424		
66	005246	010200		
67	005242			
68	005246	009204		
69				
70				
71	005250			
72				
73	005230	005767	001078	
74	005254	001486		
75	005256	013782	172544	
76	005262	004467	177742	
77	005266	052.	200	200
	005271	200		
78	005272	000207		
79				

 REGOUT: REGISTER OUTPUT LINKAGE: RA
 ***** WORD IN R2; IDENTIFIER IN -(RA)

 MOV R4,R0 TADDR,OF IDENTIFIER
 JC OUT
 CMP (414,(A)) ISKIP ARGUMENTS
 MOV R2,R0 GET VALUE OF WORD
 JC OUT
 RTS R4 RETURN FROM REGOUT

 TIMOUT1: ISEND TIME FROM KW11-P

 TST TIMLG TIME LOG?
 BEQ THOUT1 IGO
 MOV #172544,R2 SET CNT
 JSR R4,REGOUT ISEND II
 BYTE 52,200,200,200 FIDENIT,I

 THOUT1: RTS PC RETURN FROM THOUT

REPLACEMENT PROCEDURE RT-11 MACRO VM82-Q9 00:11:26 PAGE 10

TITLE REPLACEMENT PROCEDURE
XXXXXXXXXXXXXXXXXXXXXX

1
2
3
4
5 005274 005002
6
7 005278 012700 137170
8 005302 060208
9 005304 011003
10 005306 005201
11 005310 032700 000001
12 005314 001402
13 005316 004707 000032
14 005322 022201 000017
15 005326 001403
16 005330 005201
17 005332 006208
18 005334 000705
19 005336 022702 000004
20 005342 001403
21 005344 002702 000004
22 005350 000752
23 005352 000207
24
25
26 005354
27
28
29
30 005354 010203
31 005356 006303
32 005360 006303
33 005362 000103
34 005364 006303
35 005366 010304
36 005370 022704 137612
37 005374 006303
38 005376 010305
39 005380 002705 137412
40 005400 001403
41 005406 005737 148938
42 005412 001015
43 005414 012325
44 005416 011315
45 005420 005743
46 005422 012704 137170
47 005426 000204
48 005430 005720
49 005432 011423
50 005434 012704 000300
51 005440 000104
52 005442 010413
53 005444 000207
54 005446 012523
55 005450 011513
56 005452 000207
57

EXCH1 CLR R2
REPL13 MOV #XMSKB,R0
ADD R0,R0
MOV {R},R0
CLR R1
REPL2: BIT #1,R0
BEQ REPL3
JSR PC,REPLAC
REPL3: CMP #15,R1
BEQ REPL4
INC R1
ASR R0
BH REPL2
REPL4: CMP #MAX4H,R2
BEQ REPL5
ADD #4,R2
BR REPL1
REPL5: RTS PC

REPLACE: JSUBROUTINE TO REPLACE VECTOR I (=R1)
IN GROUP J (=R2/4), THE DIRECTION OF THE
REPLACEMENT IS SPECIFIED IN DIRECT

MOV R2,R3
ASL R3
ASL R3
ADD R1,R3
ASL R3
MOV R3,R4
ADD #XVECTB,R4
ASL R3
MOV R3,R5
ADD #XVECSV,R5
MOV -(4),R3
TST #0X0010
BNE SAVBAK
MOV {3},{5}+
MOV {3},{5}
TST -(3)
MOV #XMSKB,R4
ADD R2,R4
TST -(4)+
MOV -(4),(3)+
MOV #H7,R4
ADD R1,R4
MOV R4,(3)
RTS PC

SAVBAK: MOV {5},{3}+
MOV {5},{3}
RTS PC

REPLAC: JGROUP INDEX B-M
IGET DEVICE MASK J
ICOUNT 0-15
NEXT DEVICE SET?
NO
YES DO EXCHANGE
SEND UP MASK?
YES
NO
SHIFT MASK
TALL GROUPS DONE?
YES - DONE
INC R MASK OFFSET
NEXT GROUP
RETURN FROM EXCH

FACLC. OFFSET IN VECTAB
J(J+16*I)+2*#VECTAB

I=2 FOR WORD

SUFFS. IN VECsav=(J+4*I)=4

LOAD. OF VECTOR
WHICH WAY?
SAVE ORIG. VECT. IN VECsav

JGET PC(J)
LOAD. OF REPLACEMENT PC

JREPLACE PC(J)
LOAD PS=PHI+I

JREPL,PS(J)

JREST, SAVED VECT. TO ORIG.

JRETURN FROM REPLAC

REPLACEMENT PROCEDURE RT-11 MACRO YM02-02 06:11:26 PAGE 18+

58 005454 DUMP: JUMPS N LINES (N=R2) OF 6 WORDS
59 FROM STARTING ADD IN R1
60 MOV R3,-(SP)
61 005456 010346 DUM1: MOV #10,R3 16 WORDS
62 005462 012148 DUM2: MOV (R1)+,R3
63 005464 004767 JSR PC,OCPUT
64 005470 077344 SOR R3,DUM2
65 005472 012700 136448 MOV #XCHLF,X0
66 005476 004767 000112 JSR PC,TXTPTR
67 005522 004767 JSR PC,SFN08P
68 005526 077215 SOR R2,DUM1
69 005514 012603 MOV (SP)+,R3
70 005512 000247 RTS PC
71 005514 000600 CRLF: .WORD 0
72 005516 040 200 BLANK: .BYTE 40,200
73
74 005524 010046 OCPUT1: MOV R0,-(SP)
75 005522 010146 MOV R1,-(SP)
76 005524 010246 MOV R2,-(SP)
77 005526 012702 000006 MOV #6,R2 16 DIGITS
78 005532 010001 OCPUT1B: MOV R0,R1
79 005534 002701 177770 RIC #177770,R1
80 005540 002701 000060 ADD #0,R1
MOV R1,-(SP)
81 005540 110146 RUR R0
82 005546 006000 RUR R0
83 005550 006200 ASR R0
84 005552 006200 ASR R0
85 005554 077212 SOR R2,OCPUT1
86 005556 012702 000006 MOV #6,R2
87 005562 112677 000454 OCPUT2: MOV #8,(SP)+,#TXTPTR INPUT NUMBER IN BUFFER
88 005566 005267 000450 INC TXTPTR
89 005572 077205 SOR R2,OCPUT2
90 00574 012700 136442 MOV #1BLANK,R0
91 005620 .CHOUT
92 005604 012602 MOV (SP)+,R2
93 005604 012601 MOV (SP)+,R1
94 005610 012600 MOV (SP)+,R0
95 005612 000247 RTS PC RETURN FROM OCPUT
96
97
98 005614 121027 000200 CHPUT1: CMPB -(R0),#200 RETX?
99 005620 001422 BEQ CHPUT2 RETS
100 005622 121027 000000 CMPB (R0),#0 RETX WITH CRLF?
101 005626 001405 BEQ CHPUT1
102 005630 112677 000406 MOVEB (R0)+,#TXTPTR INPUT CHAR
103 005634 005267 000472 INC TXTPTR
104 005640 000765 BR CHPUT
105 005642 112777 000015 000372 CHPUT1: MOVEB #15,#TXTPTR INPUT CRLF
106 005654 005267 000366 INC TXTPTR
107 005654 112777 000012 000368 MOVEB #12,#TXTPTR
108 005662 005267 000354 INC TXTPTR
109 005666 000207 CHPUT2: RTS PC RETURN FROM CHOUT
110
111 .TITLE TRANSMISSION ROUTINE
112 *****
113
114

TRANSMISSION ROUTINE RT-11 MACRO VME2-89 08:11:26 PAGE 13+

115 025678 018046
116 025672 010146
117 025674 #127337 052525 177570
118 025702 #427337 000100 164000
119 025710 #127041 137046
120 025714 #20167 000322
121 025720 #01002
122 025722 #00167 000124
123 025726 #32767 000001 - 000306 SEND08:
124 025734 #01205
125 025736 112777 000001 000276
126 025744 #05267- 000272
127 025750 #12180
128 025752
129 025764 #20147 000252
130 025770 #01367
131 025772 #32737 000001 177570
132 026000 #01472
133 026002 #52784 000002
134 026020 #12708 000000
135 026012
136 026024
137 026036 #12737 177777 177570
138 026044 #12767 137046 000170
139 026052 #12601
140 026054 #12600
141 026056 #52737 000100 164000
142 026064 #000248
143 026066 #000240
144 026074 #000248
145 026072 #000277

SEND08: MOV R0,-(SP)
MOV R1,-(ESP)
MOV #52525, #177570
BIC #100, #FC00CHI
MOV #XTXTBF,R1
CMP R1,TXTPT4
BNE SEND09
JMP SEND05
TEST
FGET START ADDR. OF BUFFER
ANY TEXT TO SEND?
YES
END-EXIT
NEXT FREE=000?
NO
YES, PUT FILLER IN HIGH BYTE
AND SET EVEN BOUNDARY
ISEND 4 WORD
.SEND09: MOV (R1)+,R0
.SEND10: MOV R1,TXTPT4
BNE SEND11
BIT #1, #177570
BEQ SEND02
BIS #2,R4
SEND02: MOV #EOT,R0
.SEND11: RCVWHD
.RCVWHD
WAIT FOR ACK
IFST
RESET TEXT POINTER
SEND03: MOV (SP)+,R1
MOV (SP)+,R0
BIS #100, #FC00CHI
N0P
N0P
N0P
RTS PC

ENABLE SUPER INTERR.
RETURN FROM SEND08

651

RESIDENT DATA SECTION RT-11 MACRO VH02-89 08:11:26 PAGE 11+

56	006336	008	000	SLE103I	.BYTE 0,0	117
57	006340	008	000		.BYTE 0,0	120
58	006342	000000		TIMED0I	.WORD 0	
59	006344	000000		TIMLG1	.WORD 0	
60	006346	000000		TREG0I	.WORD 0	
61	006350	000000		TREG2I	.WORD 0	
62	006352	100036		TINT1I	XRTI	
63	006354	000346		TINT2I	0K7	
64	006356	000003		ENDCOMM	.WORD 3	
65						

TIME INTERR. TO GUNNY NTI
TIME INTERR. AT PRIO. 7
END OF GUNNY AREA

RESIDENT DATA SECTION RT-1T MACRO VH82-89 0011126 PAGE 12

1			
2	006360	134762	DISPT01 XDE JEV 0, DISPATCH ERROR
3	006362	134762	XSG08 JEV 1, TRAP #
4	006364	134762	XSG08 JEV 2, TRAP 13
5	006366	134762	XSG08 JEV 3, BPT
6	006370	134762	XSG08 JEV 4, IDI
7	006372	134762	XSG08 JEV 5, PWFL
8	006374	135070	XSG01 JEV 6, EMT
9	006376	135070	XSG01 JEV 7, TRAP
10	006400	134742	XDE JEV 10,
11	006402	134742	XDE J
12	006404	134742	XDE J
13	006406	134742	XDE J
14	006410	134742	XDE J
15	006412	134742	XDE J
16	006414	134742	XDE J
17	006416	134742	XDE J
18	006420	135300	DISPT1: XSG1R JEV 20, TX
19	006422	135300	XSG1R JEV 21, TP
20	006424	135300	XSG1R JEV 22, PR
21	006426	135300	XSG1R JEV 23, PP
22	006430	135300	XSG1R JEV 24
23	006432	135300	XSG1R JEV 25
24	006434	135300	XSG1R JEV 26
25	006436	135300	XSG1R JEV 27
26	006438	135460	XSG1R JEV 30, RX
27	006442	135760	XSG1R JEV 31, PIR
28	006444	134742	XDE J
29	006446	134742	XDE J
30	006450	134742	XDE J
31	006452	134742	XDE J
32			

RESIDENT DATA SECTION RT-11 MACRO VN02-09 08/11/26 PAGE 13

1
2 006454 134742
3 006456 134438
4 006460 134610
5 006462 134780
6 006464 134626

DISPT2: XDE
XTABUP
XHANG
XENDRU
XCONT

100 DISP, ERROR
102 TABLE UPDATE
104 SUSPEND HOST
106 TERMINATE SESSION
110 CONTINUE AFTER HANU

7
8 006466
9
10
11
12
13
14 006666 000000
15 006670 000004
16 006672 000412
17 006674 000014
18 006676 000020
19 006700 000024
20 006702 000030
21 006704 000034
22 006726
23
24
25
26 006726 000380
27 006730 000304
28 006732 000070
29 006734 000074
30 006736 000124
31 006740 000000
32 006742 000008
33 006744 000008
34 006746 000220
35 006750 000200
36 006752 000244
37 006754 000250
38 006756 000000
39 006760 000200
40 006762 000000
41 006764 000200

VECSAV: LBLKH N=2
VECT. ADDR.
*** GROUP 0 ***
VECTABE 0
0 70 2 NOT IMPLEMENTED
1 70 1 TRAP 4
2 70 2 TRAP 10
3 70 3 BPT
4 70 4 IOT
5 70 5 PONFL
6 70 6 EMT
7 70 7 TRAP
44+16, RESERVED FOR 8 VECT. IN GRP 0
*** GROUP 1 ***
300 71 P TX
304 71 1 IP
308 71 2 PR
312 71 3 KP
316 71 4 KW11-P
320 71 5
324 71 6
328 71 7
332 71 10 RKLI
336 71 11 PTNO
340 71 12 FPP
344 71 13 JHU
348 71 14
352 71 15
356 71 16
360 71 17

DEVICE STATUS REGISTER TABLE

45 006766 007026
46 007d26 177560
47 007030 177564
48 007d32 177550
49 007d34 177554
50 007036 172540
51 007040 000000
52 007042 000000
53 007244 000000
54 007446 177470
55 007450 177772
56 007452 000000
57 007454 177572

OVSTAT1 0,+32,
177560 71 0 TKS
177564 71 1 TPS
177550 71 2 PRS
177554 71 3 PPS
172540 71 4 KW11-P
0 71 5
0 71 6
0 71 7
177400 71 19 RKCS
177772 71 11 PIHQ
0 71 12 FLT ERR
177572 71 13 MMU SVA

RESIDENT DATA SECTION RT-II MACRO VM82-89 08111626 PAGE 134

58	RES7066
59	RES7066
60	RES7066
61	RES7066
62	RES7066
63	RES7066
64	RES7066
65	RES7066
66	RES7066
67	RES7066
68	RES7066

RESERVE 161116
 REGISTER SAVE AREA
 PLOAD A
 PLOAD B
 PLOAD C
 PLOAD D
 DIRECT 161116
 OLOAD A
 OLOAD B
 RETADR 161116
 RTLL 161116
 ENDADR 161116
 ENDADR 161116
 TITLE S-MQN
 END START

*RESERVE 161116
 REGISTER SAVE AREA
 PLOAD A
 PLOAD B
 PLOAD C
 PLOAD D
 DIRECT 161116
 OLOAD A
 OLOAD B
 RETADR 161116
 RTLL 161116
 ENDADR 161116
 TITLE S-MQN
 END START

2. Control Program (LOG)

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LOGIS: INTERACTIVE SYSTEM MONITOR RT-11 MACRO VM02-W9 00015855 PAGE 1

```
1 .TITLE LOGIS: INTERACTIVE SYSTEM MONITOR
2 *****+
3 *+
4 * CONTROL AND LOGGING PROGRAM FOR MONITOR SYSTEM "RT-11"
5 * LOG IS THE MAIN PROGRAM AND HAS TO BE LINKED TO
6 * THE OBJECT MODULES LOGIO AND LOGIURF.
7 * ALL ENTRIES AND ROUTINES FOR THE HARDWARE MONITOR ARE
8 * FORESEEN, THE CORRESPONDING LINE IS TO BE PLACED BY MDP'S.
9 *
10 ****+
11 *
12 .GLOBAL TTYOUT,OPRINT,OPRD,PRTBTT,o[INP]
13 .GLOBAL BIR,PKT,BITPOS,BITS,DEC,DECODE,INERK,INERS
14 .GLOBAL INDR1,PUTWD,CUDIN,CUDERW,INER2
15 .GLOBAL CNTOUT,PNT,T,PNTA,B,TINLUG,LCLK
16 .GLOBAL LOICHI,F,TINU,F,TIX,TINL,T,CLK
17 .GLOBAL HAIK,TRIEND,SRPRT,SRPFC,DISRAD
18 .GLOBAL ESEUT,SBUF4,SBUF1,SHFCP,SHAM1
19 .MCALL .PRINT,,READYF,,EXIT,,WTRF,,UFF,,SEMU,,RECV,,DEF
20 .MCALL .TTYIN,,TTYOUT,,WHITF,,WP2,,TTLINK,,WHITR,,READY
21 .MCALL .CSDIN,,TSISPC,,CLOSE,,WAIT,,FETCH4,FUTER,,RELEASE
22 .V2,,
23 .HFGDEF
24 .ASECT
25 .=1670
26 TPS1/7564
27 FUF=04
28 ACK=06
29 RRF=349
30 BRF=340
31 PSW=177776
32 HIGHMA
33 TBUFS172542
34 TSTAT172540
35 PLIV=320
36 PLS4=1640000
37 PLD0=164042
38 PLT0=164004
39 TSS=PLSH
40 IOD=PLSH
41 IIR=PLIP
42 IOM=PLUB
43 IIV=PLIV
44 IOV=PLIVED
45 COMCH1=IT5
46 COMCH2=IT5
47 CUMCH1=IT5
48 TTYOUT=177564
49 MAXCMD=22
50 MAXEVIO
51 LSFILE=0,+MAXEV
52 HSFILE=ENDCOM-MASK#+2
```

IMMON TIP. STATUS
TBUFS172542 TTY IN CHT BUFFER
TSTAT172540 TSTAT REGISTER
PLIV=320 SELECTOR FOR PARALLEL LINK
PLS4=1640000 TSTATUS REG. -+-
PLD0=164042 TINPUT REG. -+-
PLT0=164004 TINPUT BUF. -+-
TSS=PLSH TREADY POSITION FOR PAP. LINK
IOD=PLSH
IIR=PLIP
IOM=PLUB
IIV=PLIV
IOV=PLIVED
COMCH1=IT5 TSTATUS REG. IF C. W. CHANNEL 14
COMCH2=IT5 C. W.
TTYOUT=177564 TTY OUTPUT STATUS
MAXCMD=22
MAXEVIO
LSFILE=0,+MAXEV
HSFILE=ENDCOM-MASK#+2

INIT AND WAITLP RT-11 MACRO VHS2-09 00:15:55 PAGE 2

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```

1   TITLE INIT AND WAITLP
2   *****
3   ;NLIST OF
4   ;
5   ;MACRO .SNHWRD
6   TST #ePLSK
7   HMI ,#4
8   MOV R2,ePLDR
9   ;ENOM
10  ;
11  ;
12  ;MACRO .SYREWARD
13  TSTB #P159
14  HPL ,#4
15  MOV #ePLIG,R2
16  ;ENOM
17  ;
18  18  #001000 012706 001002
19  #001004 005005
20  #001008 012707 #011134 -010112
21  #001014 012708 007249
22  #001020 004767 PUPING
23  #001024 004737 000100: 164000
24  #001032 012737 005620 000520
25  #001040 012737 000520 000522
26  #001044 004767 000004
27  ;
28  START: MOV R2,SP
29  CLR R5
30  MOV #SRUFI,SBPTH
31  MOV #STAR,RW
32  JSR PC,FIRIT
33  BIC RIC,F10S
34  MOV PRVKEY,#IV
35  MOV RLRB,F11V+2
36  JSR PC,INIT
37  ;
38  *****
39  19  #001052 005037 177776
40  #001058 183402
41  #001060 004767 001062
42  ;
43  CLR RPSH
44  TSTW
45  BLS WAITI
46  JSR PC,SYSCHD
47  ;
48  *****
49  41  #001066 005767 012174
50  #001072 001767
51  #001074 005006
52  #001076 012705 #000421
53  #001102 130567 #012160
54  #001106 001006
55  #001110 010008
56  #001112 010546
57  #001114 000774 012722
58  #001120 012605
59  #001122 012604
60  #001124 000291
61  #001126 006505
62  #001130 105150
63  #001132 044124
64  #001134 000762
65  ;
66  WAITI: TST DISPHD
67  BEQ WAITLP
68  CLW R4
69  MOV #A1,RS
70  WAITP: BICR RS,DISPHD
71  BEQ WAITS
72  MOV R4,-(SP)
73  MOV RS,-(SP)
74  JSR PL,SH1SHTD(4)
75  MOV (SP)+,RS
76  MOV (SP)+,RS
77  WAITS: CLC
78  ASL R5
79  BCS WAITLP
80  TST (4)+
81  BEQ ALTP
82  ;
83  *****
84  ;TJS PREVIOUS WORD RECEIVED
85  ;INIT IF NOT
86  ;SEND WORD IN R4
87  ;
88  ;TJS THERE A NEW WORD
89  ;INIT IT NOT
90  ;STORE WORD IN RA
91  ;
92  *****
93  ;INIT. BUFFER POINTER
94  ;
95  ;INIT LOC. VECTOR
96  ;
97  ;INITIALIZE PARAMS AND TABLES
98  ;
99  *****
100 ;WAITLP: SYSTEM WAIT LOOP AND TASK DISPATCHER
101 ;
102 ;
103 ;
104 ;
105  *****
106  ;PRIGA/C-BITS CLEAR
107  ;TJS THERE SOME TTY INPUT?
108  ;F10L
109  ;TJS=ANALYZE AND DISPATCH END
110  ;
111  *****
112  ;SCAN DISPATCH WORD AND BISH. SCHEDULED TASK ARE
113  ;
114  ;
115  ;INITIALIZING THEREBY
116  ;DISPATCH WAITING
117  ;TJS
118  ;TJS= LOWER BYTE OF DISPATCH
119  ;F10L
120  ;SAVE REGS
121  ;
122  ;TJS=DISPATCH TASK
123  ;
124  ;
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UTILITY TASKS RT-11 MACRO VM02-09

00:15:55 PAGE 3

TITLE: UTILITY TASKS

XXXXXXXXXXXXXX

INITI: ;INITIALIZE SYSTEM PARAMS AND TABLES

CLP #*177546 ;INIT LINE CLOCK

MOV \$120,LLCXV1

MOV ALCKR,\$0000

MOV RFLDN,RC

TST {W}+ ;CLEAR TIME COUNTER

MOV #32000,{W}+ ;MOV #32000,{W}+

MOVb #400,{W}+ ;MOV #400,{W}+

TSTB {W}+ ;SKIP PEPINU

MOV #500,{W}+ ;MOV #500,{W}+

MOV #C00,{W}+ ;MOV #C00,{W}+

TSTC {W}+ ;CLEAR EJENI COUNTERS

MOV #55,{W}+ ;MOV #55,{W}+

CLR {W}+ ;DEC {W}+ ;BRE INITI

TST CALL ;TST CALL

HIS \$120,#*177546 ;HIS \$120,#*177546

HIS \$120,\$AC00CH1 ;HIS \$120,\$AC00CH1

RTS PL ;RTS PL

PRINTB: ;PRINT R12 CHARS. STARTING AT (RS)

MOV RD,-(SP) ;MOV RD,-(SP)

MOV R12,-(SP) ;MOV R12,-(SP)

MOV R3,-(SP) ;MOV R3,-(SP)

MOV R4,-(SP) ;MOV R4,-(SP)

MOV R5,-(SP) ;MOV R5,-(SP)

MOV R6,-(SP) ;MOV R6,-(SP)

MOV R7,-(SP) ;MOV R7,-(SP)

MOV R8,-(SP) ;MOV R8,-(SP)

MOV R9,-(SP) ;MOV R9,-(SP)

MOV R10,-(SP) ;MOV R10,-(SP)

MOV R11,-(SP) ;MOV R11,-(SP)

MOV R12,-(SP) ;MOV R12,-(SP)

JSR PC,PRINT ;JSR PC,PRINT

HK PATHS ;HK PATHS

L1001: ;L1001 {L1}+ ;LABEL SE CHAR

HUB {L1},RD ;HUB {L1},RD

HIC #177546,RQ ;HIC #177546,RQ

SHM R4,R4 ;SHM R4,R4

HLT PATH ;HLT PATH

HEP R4,R4 ;HEP R4,R4

APL PATH2 ;APL PATH2

ASL R4 ;ASL R4

CIP R4,R4 ;CIP R4,R4

HPL PATH2 ;HPL PATH2

SUS R4 ;SUS R4

RTS {L1}+ ;RTS {L1}+ ;RTS {L1}

DEC R3 ;DEC R3

HDP PATHS ;HDP PATHS

HIC PATH1 ;HIC PATH1

UTILITY TASKS RT-11 MACRO VME2-09
00:15:55 PAGE 30

	RT-11 MACRO VME2-09	00:15:55 PAGE 30
58	001356	105137
59	001362	105175
60	001364	105184
61	001366	105194
62	001370	105203
63	001372	105205
64	001374	105206
65		105205

TSTB \$RPS
BPL *-4
PRTB3:
MOV (SP)+, R4
MOV (SP)+, R3
MOV (SP)+, R1
MOV (SP)+, R0
RIS R5
IRETUN FROM PRINTB

CMDI FOR HOST MODE SPEC'S

RT-11 MACRO VM82-09 001155 PAGE 4

		TITLE CMDI FOR HOST MODE SPEC'S	
1			
2			
3			
4			
5			
6	0011376	310096	
7	0011376	310096	
8	0011440	2101446	
9	0011440	2101446	
10	0011442	2102446	
11	0011444	2102446	
12	0011446	2102446	
13	0011448	2102446	
14	0011448	2102446	
15	0011448	2102446	
16	0011448	2102446	
17	0011448	212793	006674
18	0011448	204167	204167
19	0011448	204167	204167
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48	0011448	204167	204167
49	0011448	204167	204167
50	0011448	204167	204167
51	0011544	006521	
52	0011544	006521	
53	0011546	206521	
54	0011546	206521	
55	0011546	206521	
56	0011546	206521	
57	0011546	206521	

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CMDI FOR HOST MODE SPECS

RT-11 MACRO.VH02-09 08:15:55 PAGE 4*

58
59 00156a
60
61 00156b 006371
62 00157d 002771 011016
63 001574 004761 0000000G
64 00157d 004761 0000000G
65 001574 001743
66
67 001626
68
69 00156c 005725
70 001610 012700 006704
71 001614 004767 0000000G
72 001620 00167 177576
73
74 001624
75
76 001624 005725
77 001626 012700 007000
78 001632 004767 0000000G
79 00156b 00167 17756b
80
81 001642
82
83 001642 006371
84 001644 011022
85 001640 002771 0000000G
86 001652 002475
87 001654 012703 00000002
88
89 001660
90
91 00166d 005020
92 001662 116202 011002
93 001666 01107 0000000G
94 001672 012703 007000
95 001674 004767 0000000G
96 001702 004767 0000000G
97 001700 005773
98 001710 002402
99 001712 116202 011042
100 001716 005020
101 001724 005373
102 001722 00135b
103 001724 227673
104
105 001726
106
107 001726 016202 011042
108 001732 004767 0000000G
109 001730 012702 0067000
110 001742 004767 0000000G
111 001746 004767 0000000G
112 001752 005773
113 001754 100157
114 001750 116202 011064

1 CMIDI9: *** SUBMASK I/O ***
;
; ASL R1
; MOV #MSK02G,R1
; JSR PC,BTRPH
; JSR PC,BTRPU
; BX C0016
; FINDINDEX
; TADUR, OF SUBMASK
; SPINIT TASK
; SPREAD NEW MASK
; SPREAD NEXT INDEX
;
CMIDI10: *** SUBMASK UPDATE ***
;
; TST (5)+
; MOV #MSK1N,R0
; JSR PC,PRINT
; JMP C0011
; SPREAD Y/N
;
CMIDI12: *** SELECT WORD UPDATE ***
;
; TST (5)+
; MOV #SELWIN,R0
; JSR PC,PRINT
; JMM C0011
; SPREAD Y/N
;
CMIDI14: *** SELECT WORD I/O ***
;
; ASL R1
; MOV R1,R2
; CMP #2X,R1
; BLT C0011b
; MOV R2,R3
; FINDINDEX
; SAVE INDEX
; INDEX+1#
; TES->JMP BTRU I/O
; PROCESS 2 OF TEs
;
CMIDI15: *** BYTE I/O ***
;
; CLR R2
; MOVD SL3660(2),R0
; JSR PC,PRINT
; MOV R2,R0
; JSR PC,PRINT
; JSR PC,UCHD
; TST R0
; BMI C0015A
; MOVD R1,SL3660(2)
; JSR PC,PRINT
; MOVD R1,SL3660(2)
; JSR PC,PRINT
; INC R2
; DEC R3
; BE C00115
; BX C0016
;
CMIDI16: *** WORD I/O ***
;
; MOVD SL3660(2),R0
; JSR PC,PRINT
; MOV R2,R0
; JSR PC,PRINT
; JSR PC,UCHD
; TST R0
; BMI C0016
; MOVD R1,SL3660(2)
; JSR PC,PRINT
; MOVD R1,SL3660(2)
; JSR PC,PRINT
; INC R2
; DEC R3
; BE C00115
; BX C0016

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Right ready

LOG OUTPUT ROUTINES

RT-11 MACRO VM82-09 0015:55 PAGE 10

1
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5 *****
6 006214 105267 005044 REC01: LOGIC CHASY
7 006220 0042767 000002 005040 TSTB SLGREC
8 006226 105767 005062 HED REC4
9 006232 001445 TSTB SHUF5H
10 006234 105767 002665 REC02: HED REC1
11 006240 001445 MOV #SHUF2, R3
12 006242 012703 012134 CLRB SHUF5H
13 006246 105767 002053 BX HFC2
14 006252 000002 011134 REC03: MOV #SHUF1, R3
15 006254 012703 011134 REC04: WRITB NAMEA, #4, R3, #256, ,BLKCNT
16 006260 103084 REC05: ACC PEC5
17 006262 004567 000000 JSR RS,10ERK
18 006268 000000 000000 BYTE 4,M
19 006274 103084 REC06: BX HFC4
20 006276 004726 REC07: INC BLKENT
21 006282 004567 000000 REC08: CLR CHASY
22 006292 000000 000000 TSTB DYNUNT
23 006334 000000 000000 REC09: HED REC5
24 006336 005267 004726 REC10: MOV #880,-,(SP)
25 006342 105767 004716 REC11: MOV #HECS,-,(SP)
26 006346 105767 005001 REC12: JMP RCVROR
27 006352 001445 REC13: RTS PC
28 006354 012746 000300 REC14: DUMP LOG RECORD AS IS ON TERMINAL
29 006360 012746 006370 REC15: DUMP LOG RECORD AS IS ON TERMINAL
30 006364 029167 177240 REC16: DUMP LOG RECORD AS IS ON TERMINAL
31 006370 000207 REC17: DUMP LOG RECORD AS IS ON TERMINAL
32
33
34 006372 REC18: DUMP LOG RECORD AS IS ON TERMINAL
35
36
37 006372 105267 004666 REC19: INCB CHASY
38 006376 0042767 000004 004662 REC20: PIC #4,DISPBD
39 006404 016701 022522 REC21: MOV SHFLC2,R1
40 006410 022167 022514 REC22: CTR H1,SHFL1
41 006414 100412 REC23: BTI DUMP1
42 006416 166701 000000 REC24: SUR SHFL1,R1
43 006422 010103 000000 REC25: MOV H1,R3
44 006424 016767 002500 000004 REC26: MOV SHFL1,DUMP1
45 006432 024567 172610 REC27: JSR RS,PRINTH
46 006436 000000 000000 DUMP01: LDAD A
47 006448 000000 000000 BX DUMPS
48 006448 012702 013134 DUMP11: MOV #SHUF1,R2
49 006446 106702 000000 SUR SHFL1,R2
50 006452 010203 000000 MOV R2,R3
51 006454 016767 002450 000004 REC28: MOV SHFL1,DUMP1D
52 006462 024567 172560 REC29: JSR RS,PRINJH
53 006466 000002 000000 DUMP1B: LDAD A
54 006470 162701 011134 SUR #SHUF1,R1
55 006474 016103 000000 MOV R1,R2
56 006476 012767 011134 000004 REC30: MOV #SHUF1,DUMP1A
57 006476 024567 172536 REC31: JSR RS,PRINJH

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LOG OUTPUT ROUTINES RT-II MACRO VM02-09 00:15:55 PAGE 104

58 006516 000000
59 006512 105267 004546
60 006516 105767 004631
61 006522 001406
62 006524 012746 00038H
63 006524 012746 006540
64 006534 028167 177072
65 006540 000207
66
67
68
69
70 006582
71
72 006542 105267 004516
73 006546 002767 000010 004512
74 006554 016700 002350
75 006560 005120
76 006584 004767 000000G
77 006566 002701 17748D
78 00657C 010100
79 006574 004767 000000G
80 006600 105267 004460
81 006604 105767 004543
82 006610 001406
83 006612 012746 00038H
84 006616 012746 006626
85 006622 002167 177082
86 006620 000207
87
88

DUMP10: WORD 0
DUMP3: CLR B CHSY
TST B OVHLN
REQ DUMP8
MOV #06,-(SP)
MOV #DUMP4,-(SP)
JMP RLVHOR
RTS PC

DUMP10:
/
/
/
/
GRAPH: DISPLAY DATA GRAPHICALLY

INCB CHSY
BIC #14,DISPM0
MOV SNEC1,R0
TST R0,
JSR PC,UECODE
BIC #17/40,R1
MOV R1,R0
JSR PL,CPAHM1
CLR B CHSY
TST B OVHLN
REQ GRPHC
MOV #06,-(SP)
MOV #GRPH10,-(SP)
JMP RCYHOR
RTS PC

1045 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1046 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1047 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1048 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1049 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1050 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1051 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1052 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1053 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1054 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1055 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1056 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1057 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1058 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1059 THERE DATA OVERRUN
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SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1060 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1061 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1062 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1063 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1064 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1065 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1066 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1067 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

1068 THERE DATA OVERRUN
END
SYS-SET UP NEW STACK
FROM ATI IN PVNEC
PANU JUMP THERE
RETURNS FROM JUMP

TITLE DATA SECTION

DATA SECTION	RT-11 MACRO VM02-09	001155 PAGE 11
1		
2		
3		
4		
5		
6		
7		
8	700638 000000	
9	326632 d67	SPSAYI .R0KU 0
10	300655 060	BLPNS: .ASCII /7654321076543210J/
11	026674 015	RISI: .ASCII 415><12>MASK UPDATE (Y,N)?: /<200>
12	026624 107	RSKIN: .ASCII 415><12>ACTIVE INDEX OR T<>ONE?
13	326704 015	IRG: .ASCII 415><12>SUBMASK UPDATE (Y,N)? : /<20?>
14	326736 015	SLSIN: .ASCII 415><12>SELECT CI WHICH UPDATE (Y,N)? : /<2?>
15	031444 015	SIM: .ASCII 415><12>/<2?>
16	031244 043	HASH: .ASCII 415><12>/<2?>
17	93244 033	SUFN: .BYTF 3,14,52,20
18	041052 040	CALF1: .ASLII /
19	701054 015	CHSS: .ASLII 415><12>/<2?>
20	031460 040	GAP: .ASCI 4 <END>
21	041264 077	CHERR: .ASCII 415><12>LMU/
22	041776 015	TIMST: .ASCII 415><12>INTERFERE, FREQUENCY: /<22.0>
23	051124 015	W12: .ASCII 415><12>TIME PERIOD FREQUENCY (355 AN TIME LENGTH): /<20.0>
24	041172 124	TIMCNT: .ASLII 415><12>NUMBER COUNT : /<1?>
25	041216 111	IGER1: .ASCII 415><12>FAREA ON LH :
26	091230 054	TOEK2: .BYTE ?54
27	0417240 040	ASLII / ERR, END. /
28	0017252 0000	WORD 0,0,0,0
29	0017262 077	SYCME: .ASCII 271 L SYS LM02<15><12>/<2?>
30	041515 014	HE51: .ASCII ALIAS -LINE
31	0417327 055	HE51: .ASCII ALIAS -LUS ON
32	0417365 016	HE52: .ASCII ALIAS -LFW IN UPDATE (N,H,W) : /<20?>
33	041423 016	HE53: .ASCII ALIAS LOG SPECIFIED/
34	0317404 125	HE54: .ASCII SPECFILE FOR SURF, LINE/
35	041474 125	HE55: .ASCII ALIAS FILE FOR SURFACE : /<2?>
36	0417520 117	HE56: .ASCII ALIAS FILE ON CH-7/
37	041751 014	HE57: .ASCII ALIAS FILE FOR SURFACE : /<2?>
38	0416062 116	HE58: .ASCII ALIAS FILE FOR SURFACE : /<2?>
39	031033 137	HE59: .ASCII ALPHANUMERIC DISPLAY (Y,N) : /<2?>
40	031064 120	HE60: .ASCII AUTOMATIC DISPLAY (Y,N) : /<2?>
41	041707 123	HE61: .ASCII SAVE FILE (Y,N) : /<2?>
42	0017177 040	HE62: .ASCII ASYNC FILE NOT FOR OUTPUT, ERASE NEW FILE (Y,N) : /<2?>
43	0174426 103	HE63: .ASCII ASYNC FILE FOR SERIAL/
44	0112470 040	HE64: .ASCII ASYNC OUTPUT FILE (Y,N) : /<2?>
45	0110127 103	HE65: .ASCII ASYNC FILE FOR SERIAL/
46	010144 145	HE66: .ASCII ASYNC FILE FOR SERIAL/
47	0116164 105	HE67: .ASCII ASYNC FILE FOR SERIAL/
48	012174 114	HE68: .ASCII ASYNC FILE FOR SERIAL/
49	014216 123	HE69: .ASCII ASYNC FILE FOR SERIAL/
50	0112257 124	HE70: .ASCII ASYNC FILE FOR SERIAL/
51	012275 125	HE71: .ASCII ASYNC FILE FOR SERIAL/
52	011524 101	HE72: .ASCII ASYNC FILE FOR SERIAL/
53	010555 123	HE73: .ASCII ASYNC FILE FOR SERIAL/
54	010375 107	HE74: .ASCII ASYNC FILE FOR SERIAL/
55	011422 123	HE75: .ASCII ASYNC FILE FOR SERIAL/
56	010446 015	HE76: .ASCII ASYNC FILE FOR SERIAL/
57	0110171 114	HE77: .ASCII ASYNC FILE FOR SERIAL/

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DATA SECTION

```

58 010516      052    280    280    IDER:   *BYTE 52,204  IERRON IN TO CODE
59 010524      120    163    120    IDPC:   *ASCII /PC/2W9>
60 010523      120    123    123    IDPSI:  *ASCII /PS/2W9>
61 010526      125    125    124    IDSP1:  *ASCII /SP/2W9>
62 010531      173    173    120    IDCP:   *ASCII /CP/240>
63 010534      105    127    200    IDEW1:  *ASCII /EW/2W9>
64 010537      123    122    200    IDEW2:  *ASCII /SW/2W9>
65 010532      162    162    166    IDSF1:  *ASCII /HF/2C0>
66 010545      122    280    122    IDU1:   *ASCII /R/450>
67 010547      116    124    280    IDMT1:  *ASCII /HT/2W6>
68 010552      123    280    1051:  *ASCII /ST/200>
69 010555      033    014    CNTM0:  *ASCII <13><14><12><0>
70               060    060    060    CNTX1:  *ASCII / 08<42B0>
71 010576      048    048    048    EVEN:   *ASCII /<42B0>
72               053    060    060    TFIELD: *ASCII <02><55>/ACB00>?Y/<03><4><2D>
73 010594      040    040    040    SSPEV:  *BYTE 0
74 010621      040    040    040    SSPEV:  *BYTE 0
75 010622      080    080    080    SET:    31: SFT SP EV. SET
76 010623      080    080    080    SUSPNO: *BYTE 0
77 010624      131    077    040    Y:     31: HARU SP EV. SET
78 010632      116    077    040    SUSPENET HOST MN SP EV.
79 010640      077    060    060    QUES:  *ASCII /h? : /<2Ph>
80               060    060    060    EVEN:   *ASCII /?/?/
81 010642      001606  001606  001606  CM011:  CMD110
82 010644      001606  001606  001606  CM0112: CMD111?
83 010646      001704  001704  001704  CHOT2:  CM010P
84 010654      001612  001612  001612  CHOT2:  CM010P
85 010652      001616  001616  001616  CHOT1:  CM011
86 010654      001626  001626  001626  CHOT3:  CM0113
87 010656      001606  001606  001606  CHOT3:  CM0110
88 010660      001620  001620  001620  CHOT12: CM0112
89 010662      001704  001704  001704  CHOT17: CM0117
90 010664      001704  001704  001704  CM014:  CM011A
91 010666      001666  001666  001666  CM019:  CM0119
92 010670      001642  001642  001642  CM0114
93               000104
94               000104
95               000104
96               000104
97 010672      000127  000127  SYMBAB: 127
98 010674      000166  000166  SYMBAB: 127
99 010676      000123  000123  SYMBAB: 127
100 010700      000210  000210  SYMBAB: 127
101 010722      000114  000114  SYMBAB: 127
102 010704      000120  000120  SYMBAB: 127
103 010706      000124  000124  SYMBAB: 127
104 010710      000103  000103  SYMBAB: 127
105 010712      000132  000132  SYMBAB: 127
106 010714      000105  000105  SYMBAB: 127
107 010716      000104  000104  SYMBAB: 127
108               000104
109               000104
110               000104
111 010720      005776  005776  DISPATCH TABLE FOR WAITLP
112 010722      000214  000214  DISPATCH: FILEN
113 010724      000372  000372  RECORD
114 010726      000342  000342  DUMP
115               000342
116               000342

```

DISPATCH TABLE FOR WAITLP
FILEN
RECORD
DUMP
GRAPH

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115
116
117
118 010730 002326
119 010732 002334
120 010734 002506
121 010736 003214
122 010740 003216
123 010742 005114
124 010744 005166
125 010746 005122
126 010750 005574
127 010752 005476
128 010750 0002226
129
130
131
132
133

DISPATCH TABLE FOR SYSMD INDEX
DISPTIS WAITUP 1018
SETFLG 112
CSIS 124
CSIM 126
CSIL 132
PHOC 117
TERM 114
CONT 116
ENAS 121
SPEVUP 142
ENTOUT 144

IDENTIFIERS FOR NUM DUMR INDEX
NAME INDEX
IDADDI TDER 13
IDPC 12 PC
IDPS 14 PS
IDSP 15 SP
IDCP 16 CP
IDEW 112 CW
IDSK 114 SW
IDRF 116 HF
IDP 163 H
IDER 162 E
IDHT 164 H1
IDST 165 H1

BEGINNING OF COMMUNICATION AREA

MASK01 WORD 7B00000000000000
PC01 WORD 0
MASK02 WORD 7B00000000000000
PC02 WORD 0

SUPERMASK INDEX
MSK005 WORD 7001111111111111 11 MASK PC,PS,SP FMK EV 1-5
MSK067 WORD 6920100012001100 18 MASK SEL,PL-2,PS,SH,(PL-2),(52) EV6,7
MSK101 WORD 7000011100011110 12 MASK SEL,PL,PS,SF,(HEGJ),(HUFJ),EV 20,21
MSK123 WORD 7000110010001110 13 MASK SEL,PL,PS,SF,(HEGJ),(HUFJ),EV 20,21
MSK105 WORD 7001110010001110 14 MASK "-" FMK EV 24,25
MSK167 WORD 7000110010001110 15 MASK "-" FMK EV 24,25
MSK110T WORD 7000000011111111 16 MASK SEL,PL,PS,SH,HBG-HEGJ, HUFK
MSK111 WORD 0 17 TEV 31EPI40
MSK112 WORD 0 18 TEV 32EPI40
MSK113 WORD 0 19 TEV 33EPI40

SELECT WORDS FOR CONDITIONAL EVENT REPORT

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172	011042	000	Storage: BYTE 0,0	RTSEL EMT CODE FOR EV 0
173	011044	000	BYTE 0,0	RTSEL
174	011046	000	BYTE 0,0	RTSEL
175	011048	000	BYTE 0,0	RTSEL TRAP CODE FOR EV 7
176	011050	000	BYTE 0,0	RTSEL
177	011052	000	BYTE 0,0	RTSEL
178	011054	000	BYTE 0,0	RTSEL
179	011056	000	BYTE 0,0	RTSEL
180	011058	000	BYTE 0,0	RTSEL
181	011060	000	BYTE 0,0	RTSEL
182	011062	000	BYTE 0,0	RTSEL
183	011064	000	BYTE 0,0	RTSEL
184	011066	000	BYTE 0,0	RTSEL
185	011068	000	BYTE 0,0	RTSEL
186	011070	000	BYTE 0,0	RTSEL
187	011072	000	BYTE 0,0	RTSEL
188	011074	000	BYTE 0,0	RTSEL
189	011076	000	BYTE 0,0	RTSEL
190	011078	000	BYTE 0,0	RTSEL
191	011080	000	BYTE 0,0	RTSEL
192	011082	000	BYTE 0,0	RTSEL
193	011084	000	BYTE 0,0	RTSEL
194	011086	000	BYTE 0,0	RTSEL
195	011088	000	BYTE 0,0	RTSEL
196	011090	000	BYTE 0,0	RTSEL
197	011092	000	BYTE 0,0	RTSEL
198	011094	000	BYTE 0,0	RTSEL
199	011096	000	BYTE 0,0	RTSEL
200	011098	000	BYTE 0,0	RTSEL
201	011100	000	BYTE 0,0	RTSEL
202	011102	000	BYTE 0,0	RTSEL
203	011104	000	BYTE 0,0	RTSEL
204	011106	000	BYTE 0,0	RTSEL
205	011108	000	BYTE 0,0	RTSEL
206	011110	000	BYTE 0,0	RTSEL
207	011112	000	BYTE 0,0	RTSEL
208	011114	000	BYTE 0,0	RTSEL
209	011116	000	BYTE 0,0	RTSEL
210	011118	000	BYTE 0,0	RTSEL
211	011120	000	BYTE 0,0	RTSEL
212	011122	000	BYTE 0,0	RTSEL
213	011124	000	BYTE 0,0	RTSEL
214	011126	000	BYTE 0,0	RTSEL
215	011128	000	BYTE 0,0	RTSEL
216	011130	000	BYTE 0,0	RTSEL
217	011132	000	BYTE 0,0	RTSEL
218	011342	000	BYTE 0,0	RTLOG MODE IS DEFINED.
219	011343	000	BYTE 0,0	RTLOG FALL UPDATE.
220	011344	000	BYTE 0,0	RTLOG LOADING OF MASS STORAGE.
221	011345	000	BYTE 0,0	RTLOGIC BUS INTERFACE.
222	011346	000	BYTE 0,0	RTLOGIC BUS DISPLAY.
223	011347	000	BYTE 0,0	RTLOGIC BUS ANALOG & ON X
224	011348	000	BYTE 0,0	RTLOGIC LOGIC UNIT & ON Y
225	011349	000	BYTE 0,0	RTLOGIC INPUT ON A IN SCS.
226	011350	000	BYTE 0,0	RTLOGIC OUTPUT ON B IN SCS.
227	011352	000	BYTE 0,0	RTLOGIC OF KEYBOARD INPUTS FROM X-
228	011354	000	BYTE 0,0	RTLOGIC KEYBOARD INPUTS FROM Y-

LOG SPECIFICATION FILE, LENGTH=16SPFIL

SLGSP1: BYTE 0,0

SLGSP2: BYTE 0,0

SLGSP3: BYTE 0,0

SLGSP4: BYTE 0,0

SLGSP5: BYTE 0,0

SLGSP6: BYTE 0,0

SLGSP7: BYTE 0,0

SLGSP8: BYTE 0,0

SLGSP9: BYTE 0,0

SLGSP10: BYTE 0,0

SLGSP11: BYTE 0,0

SLGSP12: BYTE 0,0

SLGSP13: BYTE 0,0

SLGSP14: BYTE 0,0

SLGSP15: BYTE 0,0

SLGSP16: BYTE 0,0

SLGSP17: BYTE 0,0

SLGSP18: BYTE 0,0

SLGSP19: BYTE 0,0

SLGSP20: BYTE 0,0

SLGSP21: BYTE 0,0

SLGSP22: BYTE 0,0

SLGSP23: BYTE 0,0

SLGSP24: BYTE 0,0

SLGSP25: BYTE 0,0

SLGSP26: BYTE 0,0

SLGSP27: BYTE 0,0

SLGSP28: BYTE 0,0

SLGSP29: BYTE 0,0

SLGSP30: BYTE 0,0

SLGSP31: BYTE 0,0

SLGSP32: BYTE 0,0

SLGSP33: BYTE 0,0

SLGSP34: BYTE 0,0

SLGSP35: BYTE 0,0

SLGSP36: BYTE 0,0

SLGSP37: BYTE 0,0

SLGSP38: BYTE 0,0

SLGSP39: BYTE 0,0

SLGSP40: BYTE 0,0

SLGSP41: BYTE 0,0

SLGSP42: BYTE 0,0

SLGSP43: BYTE 0,0

SLGSP44: BYTE 0,0

SLGSP45: BYTE 0,0

SLGSP46: BYTE 0,0

SLGSP47: BYTE 0,0

SLGSP48: BYTE 0,0

SLGSP49: BYTE 0,0

SLGSP50: BYTE 0,0

SLGSP51: BYTE 0,0

SLGSP52: BYTE 0,0

SLGSP53: BYTE 0,0

SLGSP54: BYTE 0,0

SLGSP55: BYTE 0,0

SLGSP56: BYTE 0,0

SLGSP57: BYTE 0,0

SLGSP58: BYTE 0,0

SLGSP59: BYTE 0,0

SLGSP60: BYTE 0,0

SLGSP61: BYTE 0,0

SLGSP62: BYTE 0,0

SLGSP63: BYTE 0,0

SLGSP64: BYTE 0,0

SLGSP65: BYTE 0,0

SLGSP66: BYTE 0,0

SLGSP67: BYTE 0,0

SLGSP68: BYTE 0,0

SLGSP69: BYTE 0,0

SLGSP70: BYTE 0,0

SLGSP71: BYTE 0,0

SLGSP72: BYTE 0,0

SLGSP73: BYTE 0,0

SLGSP74: BYTE 0,0

SLGSP75: BYTE 0,0

SLGSP76: BYTE 0,0

SLGSP77: BYTE 0,0

SLGSP78: BYTE 0,0

SLGSP79: BYTE 0,0

SLGSP80: BYTE 0,0

SLGSP81: BYTE 0,0

SLGSP82: BYTE 0,0

SLGSP83: BYTE 0,0

SLGSP84: BYTE 0,0

SLGSP85: BYTE 0,0

SLGSP86: BYTE 0,0

SLGSP87: BYTE 0,0

SLGSP88: BYTE 0,0

SLGSP89: BYTE 0,0

SLGSP90: BYTE 0,0

SLGSP91: BYTE 0,0

SLGSP92: BYTE 0,0

SLGSP93: BYTE 0,0

SLGSP94: BYTE 0,0

SLGSP95: BYTE 0,0

SLGSP96: BYTE 0,0

SLGSP97: BYTE 0,0

SLGSP98: BYTE 0,0

SLGSP99: BYTE 0,0

SLGSP100: BYTE 0,0

SLGSP101: BYTE 0,0

SLGSP102: BYTE 0,0

SLGSP103: BYTE 0,0

SLGSP104: BYTE 0,0

SLGSP105: BYTE 0,0

SLGSP106: BYTE 0,0

SLGSP107: BYTE 0,0

SLGSP108: BYTE 0,0

SLGSP109: BYTE 0,0

SLGSP110: BYTE 0,0

SLGSP111: BYTE 0,0

SLGSP112: BYTE 0,0

SLGSP113: BYTE 0,0

SLGSP114: BYTE 0,0

SLGSP115: BYTE 0,0

SLGSP116: BYTE 0,0

SLGSP117: BYTE 0,0

SLGSP118: BYTE 0,0

SLGSP119: BYTE 0,0

SLGSP120: BYTE 0,0

SLGSP121: BYTE 0,0

SLGSP122: BYTE 0,0

SLGSP123: BYTE 0,0

SLGSP124: BYTE 0,0

SLGSP125: BYTE 0,0

SLGSP126: BYTE 0,0

SLGSP127: BYTE 0,0

SLGSP128: BYTE 0,0

SLGSP129: BYTE 0,0

SLGSP130: BYTE 0,0

SLGSP131: BYTE 0,0

SLGSP132: BYTE 0,0

SLGSP133: BYTE 0,0

SLGSP134: BYTE 0,0

SLGSP135: BYTE 0,0

SLGSP136: BYTE 0,0

SLGSP137: BYTE 0,0

SLGSP138: BYTE 0,0

SLGSP139: BYTE 0,0

SLGSP140: BYTE 0,0

SLGSP141: BYTE 0,0

SLGSP142: BYTE 0,0

SLGSP143: BYTE 0,0

SLGSP144: BYTE 0,0

SLGSP145: BYTE 0,0

SLGSP146: BYTE 0,0

SLGSP147: BYTE 0,0

SLGSP148: BYTE 0,0

SLGSP149: BYTE 0,0

SLGSP150: BYTE 0,0

SLGSP151: BYTE 0,0

SLGSP152: BYTE 0,0

SLGSP153: BYTE 0,0

SLGSP154: BYTE 0,0

SLGSP155: BYTE 0,0

SLGSP156: BYTE 0,0

SLGSP157: BYTE 0,0

SLGSP158: BYTE 0,0

SLGSP159: BYTE 0,0

SLGSP160: BYTE 0,0

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 229 013345 000
 230 013346 000
 231 013347 000
 232 .EVEN
 233 013350 0000200
 234
 235 ; END OF LOG SPEC FILE
 236
 237 013352 000
 238 013353 000
 239 .EVEN
 240 013354 0000000
 241 013355 .BLKW 4000
 242 016016 .BLKW 4000
 243 016010 074503
 244 016020 074523
 245 .BLKW 2
 246 016026 046537
 247 016034 046537
 248
 249 016036 07452
 250 016040 07452
 251
 252 016046 .BLKW 100
 253 016164 120200
 254 016166 01n125 052450 021420
 255 .EVEN
 256 .TITLE LOG - HINOS CONTROL PRGR.
 257 001000*

SMIEV1 .BYTE 0
 SMDEW1 .BYTE 0
 SMIEV1 .BYTE A
 .WORD 0
 ;TRIGGER EV FOR MODE 0:
 ;DISPLAY MODE 0
 ;EVENT FOR Y IN MODE 0
 SUPDFL1 .BYTE 0
 OVRUNS1 .BYTE 0
 .WORD 0
 LCKSV1 .WORD 0
 DSKHNO1 .BLKW 4000
 ITYH401 .BLKW 4000
 F4T1 .RA050 "SPEC"
 .RA050 "SPC"
 .BLKW 2
 EXT21 .RA050 "LOG"
 .RA050 "LOG"
 .BLKW 2
 EXT31 .RA050 "TAH"
 .RA050 "TAH"
 .BLKW 2
 OUTSPC1 .BLKW 100
 TT4PEC1 .RA050 "TT"
 .RA050 "DUMMY, EXT"
 .EVEN
 ;END START

T61

LOGIO: I/O ROUTINE FOR LOG

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1 .TITLE LOGIO: I/O ROUTINE FOR LOG
2 *****
3 ** THIS PROGRAM CONTAINS I/O ROUTINES FOR "MIMOS"
4 ** MOST OF THEM ARE OF GENERAL USE AND CAN BE EMPLOYED
5 ** FOR ANY OTHER PROGRAM. THOSE ARE LISTED IN THE FOLLOWING:
6 ** LCLK : 11/2W LINE CLOCK HANDLE; PERIOD TIME IN SECS AND
7 ** 6TH OF SECS.
8 ** PRINT : SUBSTITUTE FOR RT-11 ".PRINT" MACRO, AVOIDING TROUBLES
9 ** DPRINT1: PRINT A DIGIT OCTAL NUMBER IN RT
10 ** DECODE1: PRINT NUMBER IN RT WITH FIELD LENGTH IN RT TO LEFT-AL
11 ** DCRD : READ OCTAL NUMBER FROM TERMINAL INTO RT
12 ** BIRD : READ BINARY NUMBER FROM TERMINAL INTO >R1
13 ** BIRPRT: PRINT NUMBER IN R1 IN BINARY
14 ** DECODE2: CONVERT ASCII NUMBER INTO BINARY; RESULT IN R1
15 ** CMDIN : READ ONE LETTER THRU FROM TTY AND COMPUTE INDEX
16 ** ACCORDING TO ARGUMENT LIST OF VALID COMMANDS.
17
18
19
20
21
22
23
24
25
26
27
28
29 00000000
30 01000000
31 00000000
32
33
34 00000000
35
36 00000000 01000000
37 00000002 01010000
38 00000004 01020000
39 00000006 01030000
40 00000010 01040000
41 010412 012737 000100 00000000
42 010420 012740 00000000
43 00000024 000767 00000000
44 00000030 012703 00000000
45 00000034 011270 00000000
46 00000040 012710 00000000
47 00000044 012714 00000000
48 00000050 012701 00000000
49 00000054 012702 00000000
50 00000060 012713 00000000
51 00000064 105213
52 00000066 005521
53 00000072 001424
54 00000072 102713 00000000
55 00000076 001173
56 00000080 102713 00000000
57 00000084 107143

1. GLOBAL TTYOUT,OPRINT,URPN,PRTBYT,LINRQ,HT,PR
2. GLOBAL BTPSS,MITS,DFLCDE,INHRR,INER3,INHRI
3. GLOBAL PUT40,CMDIN,CMDPRT,INER2
4. GLOBAL CNTOUT,PRNT,PRNTW,TI,LOG,LCLK
5. GLOBAL CNTCH,CNTHD,CNTIX,COUNT,CNTL
6. GLOBAL HANG,THIELU,SHPTR,SHF2,DISP
7. GLOBAL CSQUP,SHFSW,SHFLASHFCP
8. MFAIL,MEGLER,MEK,TTYOUT,ITYIN
9. REDEF
10. DEF
11. LSELECT LOGIO
12.
13. CNTOUT: PRINT COUNT TABLE
14. ADD RD,-(SP)
15. MOV RI,-(SP)
16. MOV R2,-(SP)
17. MOV R3,-(SP)
18. MOV R4,-(SP)
19. RIC #13H,&CNCHT
20. MOV #CNCHT0,R0 ;PRINT HEADING
21. JSR PC,PRINT
22. MOV SCNTIX+1,R0
23. MOVB #6,(D)+
24. MOVB #PC,(Z)
25. MOV #CNCPT+2,R0
26. MOVB #32,,#1
27. CNTOT1: MOV >5,R2 ;IP COUNTS
28. CNTOT2: MOV >5,R3 ;IN EVENTS PER LINE
29. INCB (5)
30. DEC RI
31. BNE CNTOT4
32. CMPB #16,(R3) ;OVERFLOW?
33. MLE CNTOTS
34. MOVB #6,(3)
35. INKA -(5)
36. ****
37. FINISHED
38. NOVERFL0-2
39. NO
40. PIFS

LOG10: I/O ROUTINE FOR LOG

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161
58 000106 012700 000000G CNTOT31 MOV #CNTLIX,R0
59 000112 004767 000272 JSR PC,PRINT
60 000116 012400 MOV (4)+,R0
61 000120 004767 000352 JSR PC,OPRINT
62 000124 005302 DEC R2
63 000126 001354 BNE CNTOT2
64 000134 012700 000000G MOV #CHLF,R0
65 000136 004767 000250 JSR PC,PRINT
66 000140 002745 RR CH10T1
67 000142 012700 000000G CNTOT43 MOV #CHLF,R0
68 000146 004767 000236 JSR PC,PRINT
69 000152 002737 000100 000000G RIS #JWR, #COMCH1
70 000160 012604 MOV (SP)+,R0
71 000162 012603 MOV (SP)+,R3
72 000164 012602 MOV (SP)+,R2
73 000166 012601 MOV (SP)+,R1
74 000170 012600 MOV (SP)+,R0
75 000172 000207 RTS PC RETURN FROM CNTOUT
76
77
78 000174 TIMLOG: TAPPEND SYS-TIME TO A RECORD
79
80 000174 010146 MOV R1,-(SP)
81 000176 010246 MOV R2,-(SP)
82 000233 105767 000000G TSTB HANG
83 000244 001643 BNE THLOG5
84 000206 012701 000000G MOV #TFIELD,R1
85 000212 010202 000000G MOV SPTR,R0
86 000216 005302 DEC R2
87 000220 020227 000000G THLOG11 CMP R2, #SEBUF
88 000224 001303 PNE THLOG2
89 000226 002767 000000G HIS #2,DISPWD
90 000234 020227 000000G THLOG21 CMP R2, #ESBUF
91 000240 001415 BEQ THLOG4
92 000242 101222 000000G THLOG32 MOVG (1)+(2)+
93 000244 101127 000204 CMPG (1), #200
94 000250 001363 BNE THLOG1
95 000252 002702 000001 HIT #1, #2
96 000256 001401 BEQ THLOG4
97 000260 105322 CLRH (2)+
98 000262 010267 000000G THLOG33 MOV R2, #BPTH
99 000266 010267 000000G MOV R2, #4EC2
100 000272 000210 RR THLOG5
101 000274 002767 000000G THLOG44 HIS #2,DISPWD
102 000302 012702 000000G MOV #340F1,R2
103 000306 105267 000000G INCQ SHUF54
104 000312 000753 RR THLOG5
105 000314 012602 THLOG55: MOV (SP)+,R2
106 000316 012601 MOV (SP)+,R1
107 000320 000207 RTS PC RETURN FROM THLOG5
108
109
110 000322 LCLK1: ITLRF CLOCK INTERRUPT HANDLER
111
112 000322 010206 LCLK1: ITLRF CLOCK INTERRUPT HANDLER
113 000324 012700 0000011G MOV R0,-(SP)
114 000330 105210 MOV #1FIELD+11,R0
115 000331 105210 ITLRF

LOGIC:I/O ROUTINE FOR LOG RT-II MACRO VMA2-09 00:10:01 PAGE 1+

```

115 Q00332 122710 0000072          CHP0 072,(0)      I/OVERFL0?:
116 000150 001001  BEQ LCL41      LCL41:      IF3
117 020340 000021  OR LCL5      MOVA 4,(R)      I/O-NONE
118 000242 112710 0000060      LCKK:      INCA *(R)
119 000340 1052008     TNOA *(R)
120 000340 122710 0000060     CIPB #0001(R)
121 000242 001401  AED 1CT,(R)
122 000250 0020412      OR LCL5
123 000340 112710 0000060      LCLK2:      MOVA #001,(R)
124 000340 105700  TSTA *(R)
125 000360 0000402      BN LCL41
126 330073 112710 0000060      LCLK3:      MOVA #001,(R)
127 240314 1052403     INCA -(R)      LCLK4:      I/OVFL0?:
128 000376 122710 0000072      CHP0 072,(0)
129 000322 001772      BN LCL5
130 000340 1126002      MOV (SP)+,R0
131 000490 0002302      RET
132
133
134
135
136 0000410      PHINT:  IPRINT TEXT STARTING AT (SP)
137 000410 0101405      PHINT:
138 000012 010021      PHINT:  MOVA R1,-(SP)
139 000014 1121008      PHINT:  MOVB R0,R1
140 000016
141 000422 105717 0000060      TSTB #11,-R0
142 000426 1057375      TSTB #0
143 000426 1057375      TSTB #0
144 000430 001400      AED PHINT1
145 000430 001400      CHP0 #200,PC
146 000334 1227003      AED PHINT2
147 000334 001411      AED PHINT3
148 000340 000764      BH PHINT2
149 000340 112770 0000015      PRINT1: MOVA R15,R1
150 000450 000450      TTRNU1
151 000450 112770 0000012      MOVA #12,R0
152 000460
153 000464 105737 0000060      PHINT2: TSTB #11,R0
154 000470 000375      APL +4
155 000372 0120031      MOV (SP)+,R1
156 000474 0002302      RTS PC
157
158 0000476      PHINT:  IPRINT OCTAL NR. n DIGITS IN R0
159
160 000476 0100046      PHINT:  MOV R0,-(SP)
161 000000 010100      MOV R1,-(SP)
162 000000 010200      MOV R2,-(SP)
163 000004 0103005      MOV R3,-(SP)
164 0000506 0121003      MOV #001100,PC
165 000512 0127002      MOV R6,R2
166 000516 1127003 0000000      MOVA #001,-(SP)
167 000522 112743 0000000      MOV R7,R1,-(SP)
168 000520 0100001      DPRINT1: MOV R0,R1
169 000530 0427001 117770      DIC #117770,PC
170 000734 0027001 0000000      ADD 2,R1
171 000734 1121003      MOVA R1,-(SP)

```

195

LOGIC: I/O ROUTINE FOR LOG RT-11 MACRO VM02~69 gen:1a:51 PAGE 1+

Right copy

196

LOGID: I/O ROUTINE FOR LOG RT-11 MACRO VMS2-E9 07/14/51 PAGE 1+

LOGIO: I/O ROUTINE FOR LOG

RT-11 MACRO VM82-69 08:14:51 PAGE 1+

344 001526 000760
345 001530 005726
346 001532 012603
347 001534 012600
348 001536 000207
349
351
352
353 001340
354
355
356 001340 01P046
357 001342 010146
358 001344 002715 000068
359 001350 112567 0000006
360 001354 005205
361 001356 013700 000052
362 001362 012701 0000006
363 001366 004767 000010
364 001372 012700 0000006
365 001376 000767 177006
366 001402 012601
367 001404 012600
368 001406 000205
369
370
371 P01410
372
373
374 001410 010246
375 001412 012702 3000006
376 001416 010046
377 001420 002716 177770
378 001424 002716 000006
379 001430 000241
380 001432 0006000
381 001434 0006200
382 001436 0006200
383 001440 0005302
384 001442 001365
385 001444 012702 0000006
386 001450 112621
387 001452 0005302
388 001454 001375
389 001456 012602
390 001460 000207
391
392 001462
393
394
395 001462 010146
396 001464 010206
397 001466 0005001
398 001470 0005002
399 001472
400 001476 002700 000200
401 001502 122700 0000000

BR DECODE2
DECODE3: TST (SP)+
MOV (SP)+,R3
MOV (SP)+,R0
RTS PC //RETURN FROM DECODE

I0ERR1: //CREATE TEXT FOR I/O ERRORS ON CHANNEL 1

I0CH=NR=1ST ARG., LINKAGE RS

MOV R0,-(SP)
MOV R1,-(SP)
ADD #60,(S)
MOV #0,(S),I0ERR2 //GET CH-NR
INC RS //INCORECT LINKAGE REG.
MOV #52,R0 //JUFI I/O ERROR WORD
MOV #I0ERS,R1 //STARTING ADD. OF BUFFER
JSR PL,PUTWD0
MOV #I0ER1,R0 //PRINT ERROR MSG
JSR PC,PRINT //PRINT ERROR MESSAGE
MOV (SP)+,R1
MOV (SP)+,RS
RTS RS //RETURN FROM I0ERR

PUTWD0: //PUT RM CONV. TO 6 DIGIT ASCII IN LOC

I0STARTING AT R11 LINKAGE: PC

MOV R2,-(SP)
MOV #0,R2 //6 DIGITS
PUTWD01: MOV R0,-(SP) //START THEM DOWN
 #177770,(SP)
 ADD #0,(SP) -
 CLC
 RDR R0
 ASH R0
 ASR R0
 DEC R2
 BNE PUTWD1
 MOV #0,R2 //TOP REVERSED SEQUENCE
PUTWD02: MOVH (SP)+,(1)+
 DEC P2
 RNE PUTWD2
 MOV (SP)+,R2
RTS PC //RETURN FROM PUTWD

CMDIN: //CMD INPUT: LINKAGE: RS

I0RESULT IN R0:=1FERR, R1:=EH, T=CMD(I)

MOV R1,-(SP)
MOV R2,-(SP)
CLR R1
CLR R2
CMDIN1: .TTYPE //GET CMD CHARACTER
 #IC #200,R0
 CPB #40,R0

LOGIO:1/I/O ROUTINE FOR LOU RT-11 MACHO VM32-W9 HP:14:S PAGE 1+

002	001500	231771	0000015
003	001710	122169	0000015
004	001214	001102	0000015
005	001520	025202	0000015
006	001520	001102	0000015
007	001522	122715	0220002
008	001526	001104	0000015
009	001530	001201	0000015
010	001532	120325	0000015
011	001534	001104	0000015
012	001536	000771	0000015
013	001540	012791	177777
014	001544	000704	0000015
015	001546	105P15	0000015
016	001550	001102	0000015
017	001552	005205	0000015
018	001554	000714	0000015
019	001556	002795	0000015
020	001562	201261	0000015
021	001564	005205	0000015
022	001566	005205	0000015
023	001570	005102	0000015
024	001572	001007	0000015
025	001574	000704	0000015
026	001600	0042100	0000000
027	001604	122100	0000015
028	001610	001102	0000015
029	001610	001102	0000015
030	001616	010100	0000015
031	001620	012602	0000015
032	001622	012001	0000015
033	001624	005100	0000015
034	001626	100001	0000015
035	001630	000005	0000015
036	001632	012700	0000015
037	001636	000767	165000
038	001642	012700	177777
039	001646	000005	0000015
040	001648	012700	0000015

LOGGRFI GRAPHICS FOR LOGGING RT-11 MACRO VM82-09 09:49:04 PAGE 1

```
1          .TITLE LOGGRFI GRAPHICS FOR LOGGING
2
3          *****
4
5          // ROUTINES FOR GRAPHIC DISPLAY OF 3-MIN EVENTS TO "PHIUSP"
6          // A HISTOGRAM IS DRAWN IN THE TEKTRONIX 4212 SCREEN.
7          // EVENTS ARE ENTERED ALONG THE X-AXIS, TAIFIR FREQUENCY IS
8          // PLOTTED ON THE Y-AXIS.
9          // UPON OVERFLOW, THE PICTURE IS RESCALED BY FACTOR 2.
10
11
12
13          //MCALL ,REGDEF,,TTYIN,,ITYOUT,,DEF
14          //GLOBAL DECOUT,OCASIV,ATEXT,PRINT
15          //GLOBAL GRIM1,PICT1,DRAWM1
16          //RDEF
17          //OFF
18          //STACK=SP
19
20          .TITLE PLOTTING TWO QUANTITIES
21
22
23
24
25 000003 CHINI INPUT AN 8 BIT CHAR FROM TEKTRONIX
26
27 000003
28 000004 RTS R5
29
30
31 000005 CHOUT: INPUT AN 8 BIT CHAR. TO TEKTRONIX
32
33 000006
34 000012 015737 177564
35 000016 140575
36 000020 040c75
37
38
39 040022 SAVR: SAVE REGISTERS
40
41 000022 010267 001656
42 000026 012703 001706
43 000032 011F1D0
44 000034 01222C0
45 000036 01032D0
46 000040 01042D0
47 000042 01052D0
48 000044 010227
49
50
51 000046 UNSAVE: RESTORE REGISTERS
52
53 000046 012703 001706
54 000052 012201
55 000054 012002
56 000056 012103
57 000060 012104
```

PLOTTING I/O ROUTINES RT-11 MACRO VH02-09 00109100 PAGE 1+

```

58 000062 012005          MOV (B)+,RS
59 000064 016700 001614    MOV SAVAR,R0
60 000070 000207          RTS PC

61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82 000072 010067 001622  TPLOT:   MOV     R0,TPTMOD      ;CHECK REG 2,TPTMOD
83 000076 010046          MOV     R0,(SP)      ;SAVE R0 ON STACK
84 000100 001425          BEQ    TPTDV      ;JUMP IF INIT. AND DARK VELT
85 000102 100010          BPL    TPTNRM      ;JUMP IF NORMAL VELT
86 000104 012700 000037
87 000110 004567 177072
88
89 000114 012700 000035
90 000120 004567 177062
91
92 000124 012500          TPTDV:   MOV     #055,RA      ;OUTPUT A GS TO INITALIZE
93 000126 100001          JSR    X5,CHOUT
94 000130 005000
95 000132 002027 002000  TPTNRM:  MOV     (RS)+,R0      ;GET X COORD TO REG 0
96 000136 100402          BPL    TPT11J      ;JUMP IF REG 0
97 000140 012700 001777  TPT11P:   CMP     R0,1023,        ;CHECK FOR 0, SCREEN
98 000144 010007 001552  TPT11Z:   B7J    TPT11Z      ;JUMP IF IN RANGE
99
100 000150 012500          TPT12:   MOV     (RS)+,R0      ;SET TO EDGE IF TOO HIGH
101 000152 100001          JSR    X5,CHOUT
102 000154 004000
103 000156 020027 001415  TPT14S:   CMP     R0,8781,        ;CHECK FOR TOO LARGE Y
104 000162 100402          BMI    TPT15H      ;JUMP IF IN RANGE
105 000164 012700 001414  TPT15:   MOV     #101,RA      ;MOVE TO EDGE OF SCREEN
106 000170 010067 001530  TPT16:   MOV     R0,TPTY      ;SAVE Y VALUE
107
108 000174 016700 001524  TPTPNT:  MOV     TPTY,R0      ;GET Y VALUE
109 000200 0026100         ROL    <0           ;MOVE UPPER 5 BITS
110 000202 0026100         ROL    R0           ;TO UPPER BYTF
111 000204 006100
112 000206 0020500
113 000210 0027400 177740  SHAR   R0           ;SHARE UPPER AND LOWER BYTE
114 000214 0027400 000040  BIC    #177740,R0      ;MASK OFF EXTRA
                                         BIS    #000040,R0      ;SET IN HT Y TAG

```

PLOTTING F/G ROUTINES

RT=111 MACRO V1002-49

```

115 000220 004567 177562
116 000224 016100 201474
117 000232 042700 177742
118 000234 052700 002100
119 000243 005567 177562
120
121 000246 016100 201452
122 000250 006100
123 000252 056100
124 000254 006100
125 000256 006300
126 000260 042700 177742
127 000264 052700 004562
128 000274 004567 177512
129 000274 016100 201422
130 000274 042700 177742
131 000284 052700 006100
132 000294 004567 177472
133 000314 005567 001422
134 000322 160003
135 000322 005567 201372
136 000326 006722
137
138 000330 012600
139 000332 006245
140

```

```

JSR      HS,CHROUT
MOV      TPIY,R0
HIC      A17740,RP
BIS      005562,RP
JSR      HS,CHROUT
MOV      IPTX,R0
ROL      R0L
R0L      R0
HOL      H0L
SWAB    RP
HIC      #177742,RP
VIS      006100,RP
JSR      HS,CHROUT
MOV      IPTX,R0
HIC      #177740,RP
BIS      006245,RP
JSR      TST
TST      IPTX,R0
BPL      CLW
CLW      BR
BR      RTN!
RTN!   (SP)+,RP
RTS      HS

```

202

;RESTORE RP AND EXIT
THEIR FROM TBLT

GRAPH ROUTINES RT=11 MACRO V102-09 00:09104 PAGE 2

TITLE GRAPH ROUTINES

GRAPH ROUTINES RT-11 MACRO VM02-09

00:09:00 PAGE 2+

```

50 000550 000767 0000006 JSH PC,DECOUT
59 000554 000763 PICT151 MUV AGAP,R0
60 000450 012700 002120* PICT151 MUV AGAP,R0
61 000302 004767 0000006 JSH PC,PRINT
62 000406 016703 001374 MOV ITEM,H5
63 000512 005002 CLR R2
64 000574 005713 PICT161 TST 94
65 000536 005410 AGO PICT17
66 000500 016200 001474* NOV EUTAR(?) ,R0
67 000504 005547 0000006 JSR PS,OCUITY
68 000510 CLR/RV2
69 000512 P05743 TST -15
70 000514 P05722 TST (2)+1
71 000516 P05766 BR PICT16
72 000520 P12130 PICT171 NOV SC4F,R0
73 000524 P-4767 0000006 JSH PC,PRINT
74 000635 P12700 001751 MOV AB63KA
75 000634 P04767 AGP,DONE
76 000640 P12190 MOV PTEXT,TA
77 000644 P04767 AGP,DONE
78 000650 P05500 CLP R6
79 000652 P04567 JSR H5, PLOT
80 000656 P04262 MOVD 178.
81 000661 P121414 MOVD 1220.
82 000662 P05500 IFC R2
83 000664 P04567 177202 JSR RS,PLOT
84 000670 P04262 MOVD 178.
85 000672 P04262 MOVD 529.
86 000674 P04367 JSR RS,PLOT
87 000678 P12170 MOVD 1220.
88 000682 P05501 MOVD 329.
89 000684 P05501 PICT111 CMP ITEM,R1
90 000691 P12101 CLW R1
91 000692 P121434 PICT111 INC PICT13
92 000694 P05942 CLW R2
93 000695 P06113 MOV YPT(1),R3
94 000696 P06117 Q01544* P000336
95 000697 P06167 P01544 P000242
96 000698 P06167 P06167 MOV XPT(1),PICT1C
97 000699 P06167 26A/28 ADD 10FM,PICT1C
98 000700 P06164 P12167 MOV Z55A,PICT1D
99 000702 P12167 P06112 MO00822 PICT121 CLR R6
100 000704 P06162 P06162 PICT121 JSR RS,PLOT
101 000706 P06160 PICT121 MOVD 0
102 000708 P06160 PICT121 MOVD 0
103 000710 P06160 P06160 IFC R6
104 000714 P06167 177072 PICT121 MOVD A
105 000716 P06167 P06167 PICT121 INC PICT16
106 000718 P06167 P06167 TAC PICT16
107 000720 P06167 P06167 TAC PICT16
108 000722 P06167 P06167 TAC PICT16
109 000724 P06167 P06167 TAC PICT16
110 000726 P06167 P06167 TAC PICT16
111 000728 P06167 P06167 TAC PICT16
112 000730 P06167 P06167 TAC PICT16
113 000732 P06167 P06167 TAC PICT16
114 000734 P06167 P06167 TAC PICT16

```

204

GRAPH ROUTINES RT-11 MACRO VM92-04

08109104 PAGE 2*

```

115 001032 000000 *WORD
116 001034 00P562 *WORD 242,
117 001036 012768 002147* MOV ALPHA,RA
118 001038 004767 00P006 ISET ALPHA MODE
119 001040 004767 17674 JSR PIC,PRINT
120 001052 000000 JSR PIC,UNSAVE
121
122 001294 000000 RTS PC
123 001294 000000 RETUREN FROM PICT!
124
125 001054 010046 DRAWN: DRAWN COLUMN INCREMENT FROM JKAPE UNDE 1
126 001050 010176 REC IN KAP LINKAGE: PC
127 001050 010176
128 001060 010246
129 001062 010546
130 001064 000001
131 001066 026701 000574 DRN11: DRN11: DRN11:
132 001072 001005 CMP ITEM,RI
133 001074 026261 001474* ADD RMH2,
134 001076 001049 000000 CMP RECTAB(1)
135 001078 005721 TST (1),
136 001084 00P770 DRN12: CMP RI,442,
137 001086 020127 000052 HMI (KAP) 000000
138 001112 140406 DRN13: DRN13: DRN13:
139 001114 012170 002046* DRN14: DRN14: DRN14:
140 001120 004767 000000 RETUREN FROM PICT!
141 001124 000000
142 001130 002167 000000
143 001130 002167 000000
144 001130 010061 001474, DRN13: DRN13: DRN13:
145
146 001142 016102 001540* ADD #2,ITEM
147 001148 102702 000000 MOV XPT(1),#2
148 001152 010267 000000 SUB #3,R2
149 001176 005200 000000 MOV R2,URH1
150 001180 004567 176176 DRN14: CLR R2
151 001184 000000 JSR RS,IPFL01
152 001190 000000
153 001174 012700 002147* DRN15: DRN15: DRN15:
154 001174 005167 000000 JSR ALPHA,RA
155 001200 016102 001474, JSR PL,MIN
156 001200 004567 176176 HMI ECTAB(1),RA
157 001204 000000 JSR RS,URQIV
158 001210 000000
159 001212 026127 001614* 0000000 DRN14: CHA VPT(1),#452,
160 001220 100004 000000 A-L DIVIDE
161 001222 016102 000036 000002 DRN15: DRN15: DRN15:
162 001226 016167 001644 000052 HMI APT(1),URH1A
163 001234 016167 000046 000052 HMI APT(1),URH1B
164 001242 006167 0000422 HMI APT(1),URH1C
165 001250 012167 000012 000032 HMI APT(1),URH1D
166 001256 012767 000012 000032 HMI APT(1),URH1E
167 001264 006167 000014, ADD VPT(1),URH1F
168 001272 006167 001614, ADD VPT(1),URH1G
169 001280 005167 DRN15: CLW RA,URH1H
170 001302 004567 176564 JSR R,IPFL01
171 001306 000000 DRN15: DRN15: DRN15:

```

POSITION VECTOR

PLOT

PLOT

GRAPH ROUTINES RT-11 MACRO VM82-89

06:03:14 PAGE 2+

```

    172 001318 00000000          DRM18:  BORR A
    173 001312 005200          INC R4
    174 001314 004367 176552      JSR RS,TPLOT
    175 001320 00000000          DRM1C:  WORD 0
                                WORD 0
    176 001322 005200          DRM1D:  WORD 0
                                WORD 0
    177 001324 005201 001114*    INC YPT(R)
    178 001326 005267 17754      INC DRM1
    179 001328 005267 177762      INC DRM10
    180 001340 005302          INC DRM10
    181 001342 00196          BNE DRM15
                                WORD 0
    182 001344 005202          CLR RU
    183 001346 004367 176520      JSR RS,TPLOT
    184 001350 004367          WORD A
    185 001352 00000000          WORD A
    186 001354 00000000          WORD A
    187 001356 00196          WORD 42*
    188 001362 004167 002247*    HUV ALPHA,HW
    189 001366 004167 00000000    JSR PC,PRINT
    190          004167          JHP DRM11
    191 001372 00196          DRM16:  CMP DIVSR,R1
    192 001400 00196          BYE DRM17
    193 001402 002100 002212*    HUV STERJAKA
    194 001406 004167 00000000    JSR PL,PRINT
    195 001412 00196          JHP DRM11C
    196          004167          DRM17:  ASR DIVSR
    197 001418 006267 30000000    CLR RU
    198 001422 006260          DRM18:  ASL YPT(R)
    199 001424 006260 001672*    TST (0)+
    200 001430 005120          TST (0)+
    201 001432 002101 000010          CMP RG,+R5
    202 001436 001372          AND DRM12
                                WORD 0
    203          001372          DRM19:  INC DRM1
    204 001438 00500000          CLR RU
    205 001438 006263 001672*    ASR YPT(R)
    206 001438 005120          TST (0)+
    207 001438 00000000          CMP RP,ITEM
    208 001438 001372          AND DRM19
                                WORD 0
    209 001438 001372 177600,    DRM10:  JSR F-C,PILT1
    210 001442 0012605          MOV (SP)+,R3
    211 001444 0012602          MOV (SP)+,R2
    212 001446 0026001          MOV (SP)+,R1
    213 001450 0026000          MOV (SP)+,R0
    214 001452 0026007          RTS PC
                                WORD 0

```

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DATA SECTION 87-11 MACRO VMS2-09 09/09/92 084 PAGES

DATA SECTION RT-11 MACRO VM02=09 00:09:04 PAGE 3+

DATA SECTION		020	195	126	XTEXT: *ASCII / EVENT / <200>
26	002111	d40	116	124	
	002112	d40	040	040	
	002115	125	040	040	
	002120	340	270	015	*ASCII: <12<15>/
	002123	270	012	015	/ <200>
27	002124	012	040	240	
	002127	d40	040	040	
	002132	d40	040	040	
	002133	d40	040	040	
	002142	d40	040	040	
	002143	d40	210	CRLF:	*BYTF 15*12
	002145	215	012	ALPHA:	*BYTE 17,00
28	002147	237	240	EVEN:	*EVEN
29	002147	34			
31		31			
32		32			
33		33			
		accept			*TITLE LOGGRF
					*END

3. LOGPRT - Printing Routine for Offline Output of HIMOS Reports

```

LOGPRT : HIMOS OUTPUT INTERPRETER MACRO VM82-09 08:10:25 PAGE 1

1   .TITLE LOGPRT : HIMOS OUTPUT INTERPRETER
2
3
4
5
6
7
8
9
10
11
12
13
14 000400
15 000600
16      177564
17      177564
18      000066
19      000000
20      000000
21 001000 012706 001000
22 001024
23 001016
24 001034 103761
25 001036 012705 000066
26 001042 004767 000114
27 001000 005002
28
29 001050
30 001114 103094
31 001116 005737 000052
32 00112d 001411
33 001124 008725
34 001126 012703 001000
35 001132 012701 003144
36 001136 004767 000106
37 001142 005272
38 001144 007743
39
40 001146
41 001160
42
43
44 001162
45
46 001162 012702 000160
47 001166
48 001172 002700 000200
49 001176 100022
50 001200 122700 000012
51 001204 001570
52 001206 005312
53 001210 012702 000156
54 001214 004767 000002
55 001220 000207
56
57 001222

***** THIS PROGRAM PROCESSES "HIMOS" LOG FILES
***** THE FILES ARE TRANSFORMED INTO READABLE FORM AND
***** PRINTED ON THE SYSTEM IFRM1HAL, ONE RECORD PER LINE.
***** THE FIRST VALUE IS THE EC, THE REMAINING ITEMS ARE
***** EXPLAINED BY A LEADING 2 LETTER ID. CODE.

***** MCALL ,PRINT,,RFDEF,,EXIT,,RFAD7,,V2,,  

***** MCALL ,CSIGEN,,CLOSE,,TTYOUT,,TTYIN,,EXIT  

***** V2..  

***** RFDEF  

***** TTYOUT=177564  

***** TPS=TTYOUT  

***** LINES=54,  

***** ASCTT  

***** E100J  

***** START: MOV R1,SP  

***** CLOSE #3  

***** CSIGEN #0$KHNN,#EXT,,#R  

***** RCS START          OPEN ERROR,TRY AGAIN  

***** MOV #LINES,R5          SET LINE CNT  

***** JSR PC,GETLIN          JSR LINE CNT  

***** CLR R2          CLEAR CNT  

***** RDBLK: RFADW #AREA,#3,#BUFF,#256,,R2  READ ONE BLOCK  

***** BCC R0OK          IFADJ OK  

***** TST #F52          IFD?  

***** BEQ TERM          SYS-TERMINATE  

***** BR START          IFU-HANU ERROR  

***** PBOOK: MOV #512,,R3          512 BYTES  

***** MOV #BUFF,R1          STARTING AT BUFF  

***** JSR PC,PRINTB          PRINT AND UCBUF  

***** INC R2          IFADJ ENT CNT  

***** PK HDBLK          PK HDBLK  

***** TERM: CLOSE #3  

***** EXIT  

***** GETLINE: READ HEADING LINE  

***** GETLIN: MUV #LINH,F,R2  

***** GETLIN: TTYIN  

***** BIC #254,R2  

***** MOVA R2,(R2)+  

***** CHRA #12,R2  

***** BNE GETLIN  

***** CLR B (2)  

***** MUV #CRLF,R0  

***** JSR PC,PRINT  

***** RTS PC          RETURN FROM GETLIN  

***** PRINT: IPRINT TEXT STARTING AT (R2)

```

LOGPRT : MIMOS OUTPUT INTERPRET RT-11 MACRO VM#2=09 09:10:25 PAGE 1

```

58 001222 010146      INSTR   MOV R1,-(SP)    00
59 001223 010201      INSTR   MOV R0,R1
60 001224 112150      INSTR   PRINT01: MOVA (1)+,R0
61 001225 112150      INSTR   TTOUT
62 001233 105737 177564      INSTR   TSTB *TTOUT
63 001234 100375      INSTR   BPL , -4
64 001240 105737 177564      INSTR   STA R0
65 001242 105737      INSTR   BEQ PRNT1
66 001244 001404      INSTR   CMPB #200,R0
67 001246 122733 000200      INSTR   BEG PRNT2
68 001252 001411      INSTR   RR PRNT0
69 001254 002164      INSTR   PRINT1: MOVB 612,RR
70 001256 112712 000015      INSTR   TTOUT
71 001262            INSTR   MOVB #12,R0
72 001266 112702 000012      INSTR   TTOUT
73 001272            INSTR   PRINT2: TSTB *TTOUT
74 001276 105737 177564      INSTR   BPL , -4
75 001302 100375      INSTR   MOV (SP)+,R1
76 001304 012601      INSTR   RTS PC
77 001306 002227      INSTR   INTRUN FROM PRINT
78 001310            INSTR   PRNTB: IPRINT R3 CHARS, STARTING AT (R1)
79 001310            INSTR   INTRUN
80 001310            INSTR   MOV R0,-(SP)
81 001310            INSTR   MOV R1,-(SP)
82 001310            INSTR   MOV R3,-(SP)
83 001310            INSTR   MOV R4,-(SP)
84 001310            INSTR   MOV R5,-(SP)
85 001310            INSTR   MOV R6,-(SP)
86 001310            INSTR   PRNTB: IPRINT R1+
87 001310            INSTR   MOVB (1),R4
88 001314 002714 177460      INSTR   HIC #17462,R4
89 001343 100400 000000      INSTR   SUB #0, R4
90 001343 100410 000000      INSTR   RMI PRTB2
91 001342 001413 177564      INSTR   HED PRTB2
92 001344 020427 000010      INSTR   CMP R4,R4
93 001352 100010 000000      INSTR   ABS R4
94 001354 010400 000000      INSTR   MOV ILADD(2),R4
95 001356 006167 177564      INSTR   JSR PC,PRNT
96 001364 102121 000000      INSTR   TSTB (1)+,R4
97 001366 005223 000000      INSTR   DEC R4
98 001370 001424 000000      INSTR   ADD PRTB3
99 001372 122711 000012      INSTR   CMPB #12,(1)
100 001376 001410 000000      INSTR   BNE PRTB2A
101 001460 005223 000000      INSTR   DEC R3
102 001462 001412 000000      INSTR   HAE PRTB2A
103 001464 001420 000000      INSTR   MOV AMEMD,R4
104 001410 004767 177606      INSTR   JSR PC,PRNT
105 001414 012152 004160      INSTR   MOV RLHUF,R0
106 001424 004167 177576      INSTR   JSR PC,PRNT1
107 001425 010425 000066      INSTR   MOV RLHFS,R5
108 001450 005223 000000      INSTR   PRTB2A: DEC R3
109 001452 001412 000000      INSTR   HNE PRTH1
110 001454 122737 177564      INSTR   TSID #2TPS
111 001456 100515 000000      INSTR   BPL , -4
112 001462 010414 000000      INSTR   MOV (SP)+,R4
113 001464 012073 000000      INSTR   MOV (SP)+,R4
114 001466 012073 000000      INSTR   MOV (SP)+,R4

```

LOGPAT : MIMOS OUTPUT INTERPRET AT-II MACRO VM82-89 UNIT:0:05 PAGE 1+

				MOV (SP)+,R3 RTS PC		RETURNS FROM PRINTA	
4	115	001450	012688				
	116	001452	0039267				
	117						
	118	001454					
	119	001114	006537				
	120						
	121	001124					
	122	001144					
	123	001144	0115	0112	0112	HEAD0	
	124	001147	0112	0112	0112	0112	
	125	001151	0112	0112	0112	0112	
	126	001154	0112	0112	0112	0112	
	127	001156	0000020				
	128	001164					
	129	001420	000050				
	130	001422	000052				
	131	001422	000052				
	132	001424	000055				
	133	001426	000058				
	134	001430	000063				
	135	001432	000066				
	136	001434	000071				
	137	001436	000074				
	138	001439	000077				
	139	001440	000079				
	140	001444	000071				
	141	001446	000074				
	142						
	143						
	144	001450	0052	200	10ER:	BYTE 52,200 RETURN IN TO CODE	
	145	001452	120	195	10PC:	-ASCII /PC<200>	
	146	001455	120	195	10PS:	-ASCII /PS<200>	
	147	001460	120	200	10SP:	-ASCII /SP<200>	
	148	001465	103	120	10CP:	-ASCII /CP<200>	
	149	001466	195	127	10E:	-ASCII /EP<200>	
	150	001471	123	122	200	10SR:	-ASCII /SC<200>
	151	001474	132	136	200	10BF:	-ASCII /BF<200>
	152	001477	122	120	10RI:	-ASCII /RC<200>	
	153	001481	112	112	200	10MI:	-ASCII /MC<200>
	154	001484	125	124	200	10ST:	-ASCII /ST<200>
	155						

.END START

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4. FORTRAN Subroutines EMIT and INEMIT

SOFTHOOK IDENTIFICATION EMITTER RT-11 MACRO VMA22-69 40107719 PAGE 1

```

1      TITLE SOFTWARE IDENTIFICATION EMITTER
2
3      SUBROUTINE FOR FLATTRAN EMIT CALLS
4
5
6
7
8      MCALL ,PCGOT
9      .NIGHT
10     00000000
11     00510000
12     012701 00000000
13     012702 011521 00000000
14     012703 112711 00000000
15     012704 00000000
16     012705 00000000
17     00000000

```

HIMOS INIT FOR EMIT UNDER FORTH RT-11 KARFO VMA22-69 40107722 PAGE 1

```

1      TITLE HIMOS 1-11 FOR FLAT JUNKIE FLATRAY
2
3
4      THIS ROUTINE WAS TO BE CALLED PRIOR TO THE FIRST EMIT CALL
5      IT RESETS THE TRAP VECTOR TO POINT TO THE INIT
6
7
8
9      .CSECE Init
10    00000000 012737 154002 00000000
11    00000000 012737 00000000 00000000
12    00000000 00000000 00000000
13    00000000

```

HIMOS INIT FOR EMIT UNDER FORTH RT-11 KARFO VMA22-69 40107722 PAGE 1

```

1      TITLE HIMOS 1-11 FOR FLAT JUNKIE FLATRAY
2
3
4
5
6
7
8
9      .CSECE Init
10    00000000 012737 154002 00000000
11    00000000 012737 00000000 00000000
12    00000000 00000000 00000000
13    00000000

```

5. Program Examples for Monitor Sessions

5.1 HISTO - Program for Compiler Analysis

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```

RT-11 FORTRAN IV      V016-08

C PROGRAM TO PRINT A DISTRIBUTION HISTOGRAM
C SAMPLE VALUES ARE READ FROM THE INPUT FILE F111.DAT
C THE SORTED ARRAY IS STORED IN F112.DAT
0001    LOGICAL STA1(80)
0002    REAL ARRAY(200)
0003    INTEGER HIST(10)
0004    DATA STA1/80*' '
0005    DU 10 101 200
0006    READ (1,2),END=132  ARRAY(1)
0007    20  FORMAT (F5.2)
0008    15  CONTINUE
0009    138  ISIZE=1
0010    DU 120 101,ISIZE=1
0011    DU 118 K=1,1,ISIZE
0012    IF (ARRY(1).GE.ARRAY(K)) GO TO 110
0013    TMP=ARRY(1)
0014    TMP=ARRY(JJ)
0015    ARRAY(JJ)=ARRY(K)
0016    AMRAY(K)=TMP
0017    110  CONTINUE
0018    120  CONTINUE
0019    DU 123 K=1,ISIZE
0020    125  WRITE(12,2)ARRAY(K)
0021    DU 126 K=1,10
0022    126  HIST(K)=0
0023    DU 126 K=1,ISIZE
0024    N=IF(1,ARRAY(K))/10+1
0025    130  HIST(N)=HIST(N)+1
0026    WRITE(1,135)
0027    135  FORMAT (IX,'DISTRIBUTION IN INTERVALS OF 10.000000,/')
0028    DU 156 K=1,10,N,1
0029    JAK=16
0030    WRITE (1,140)HIST(K/10),/1,K
0031    140  FORMAT ('/1X,13',VALUES,RANGE,'/13,',TO '13,13')
0032    IF (HIST(K/10).EQ.0) GO TO 136
0033    WRITE(1,145) (STA1(M),M=1,HIST(K/10))
0034
0035    145  FORMAT ('1H*,24,62A1')
0036    150  CONTINUE
0037    WRITE (1,160) ISIZE
0038    160  FORMAT ('1/1X,TOTAL NUMBER OF SAMPLES: ',13)
0039    CALL EXIT
0240

```

5.2 SAMGEN - Random Number Generator for FPP Performance Analysis

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```

AT-11.FORTRAN IV 4 V01B-08
C. PROGRAM TO GENERATE J RANDOM NUMBERS IN THE RANGE 0-99.99
C. FURK EMIT CALLS ARE INSERTED FOR MONITORING *MAN* PERFORMANCE

      REAL MAX,MIN
      CALL IACM1T
      CALL EMIT()
      WRITE (7,20)
 20  FORMAT (1X,A, OF SAMPLES: ',')
      READ (5,30) J
 30  FORM4 '(15.3'
      MIN=0
      MAX=99.99
      LSD=1
      NEW=0
      DO 100 K=1,J
 100  CALL SMIT(1)
      X=RAND(MAX-MIN)+MIN
      CALL EXIT(2)
      WRITE (1,40) X
      CALL EXIT(3)
 40  FORMAT (F5.2)
 50  CONTINUE
 60  CALL EXIT(4)
 70  CALL EXIT(5)
 80  END
 90 22

```

APPENDIX C

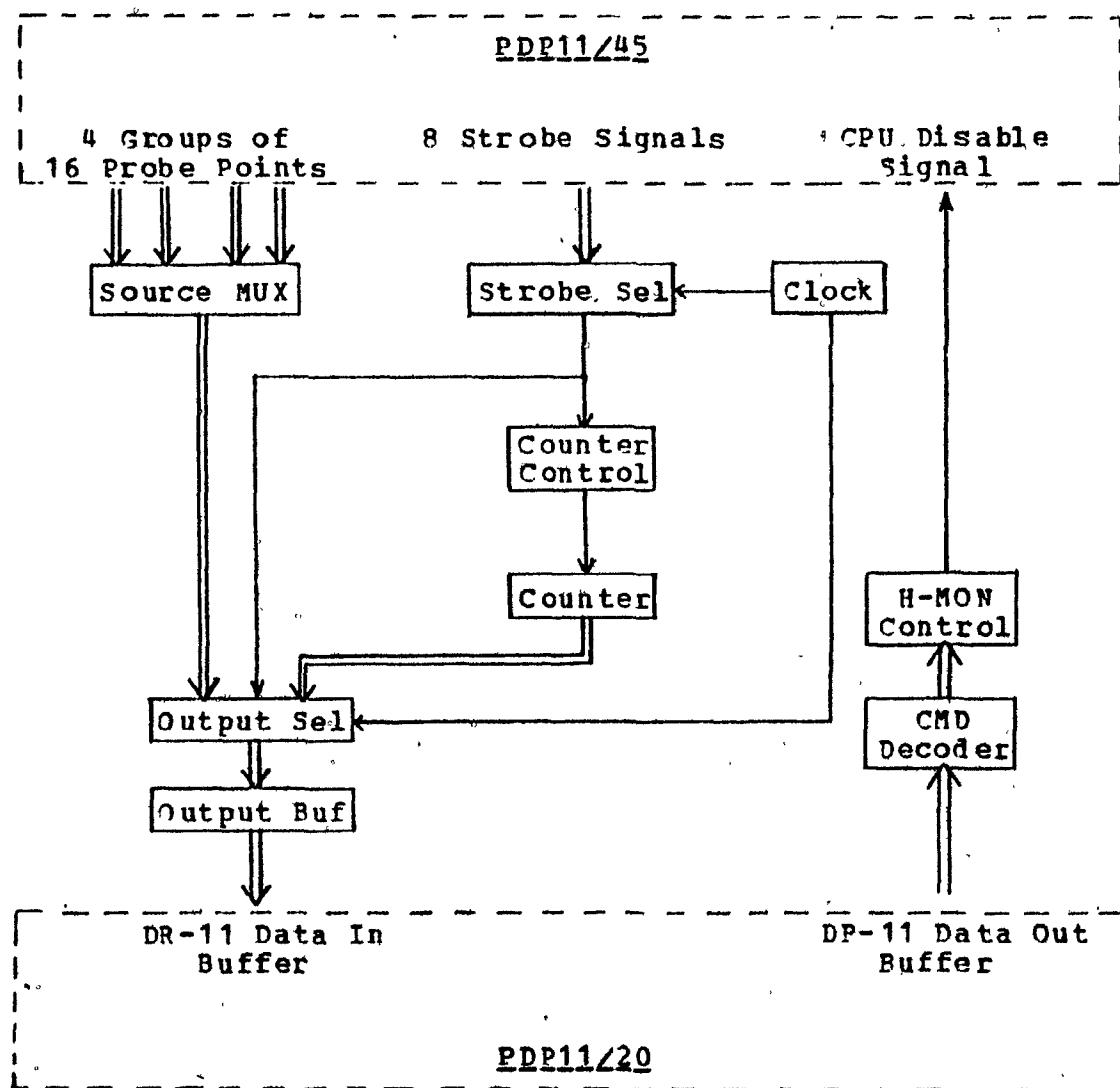
Hardware DocumentationC.1 Hardware Monitor Design

Figure C.1.1: H-MON, Data and Control

BIT	0	2	3	4	5	7	8	-	9	11	12	15
Mode SEL <0..2>	Source SEL <0..1>	CLK SEL <0..2>		STOP/START	STROBE SEL <0..2>		RESERVED					
000 TRACE	00 SEL SOURCE 0	000	10 KHz	0 STOP	000 SEL STROBE 0							
001 COUNT	01 " " 1	001	5 KHz	1 START	001 " " 1							
010 EVENT DRIVEN	10 " " 2	010	2.5 KHz		010 " " 2							
011 TIME	01 " " 3	011	1.25 KHz		011 " " 3							
100 NOT VALID		100	500 Hz		100 " " 4							
101 NOT VALID		101	250 Hz		101 " " 5							
110 SAMPLE		110	125 Hz		110 " " 6							
111 FAST COUNT		111	62.5 Hz		111 " " 7							

Fig. C.1.2: H-MON Control Word, Bit Assignment.

C.2 Parallel communication Link

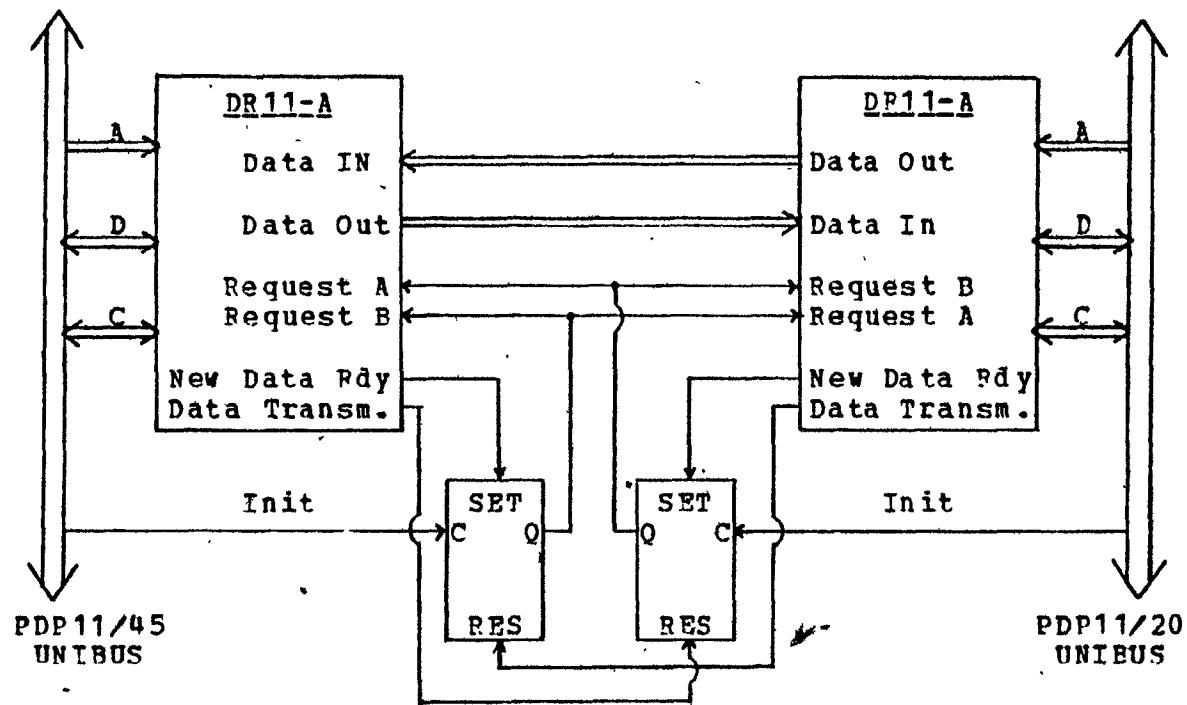


Figure C.2.1: Communication Link

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