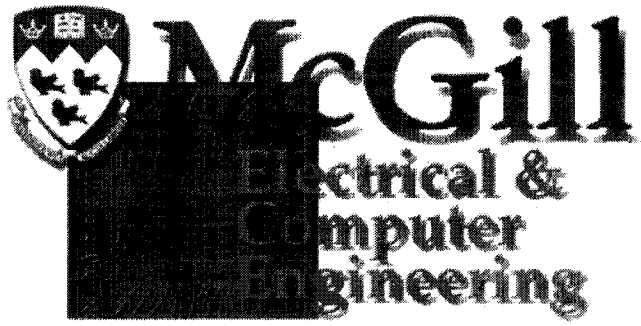

BISMUTH BASED NANOELECTRONIC DEVICES

By

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Abstract

Bismuth (Bi) is a unique electronic material with small effective mass (~0.001m_e) and long carrier mean free path (100 nm at 300K). It is particularly suitable for studying nano scale related phenomena such as size effect and energy level spacing. In this thesis work, bismuth based nanoelectronic devices were studied. Devices were fabricated using a combination of electron beam (e-beam) writing and thermal evaporation techniques. Dimensions of the fabricated devices were in the order of 100 nm. All structures were optimized for individual electrical characterization. Three types of devices were studied: Bi nanowires, Bi nanowires with dual side-gate structures and Bi nanodot structures. In the study of Bi nanowires, metal-to-semiconductor transition phenomenon and size effect were observed. The conduction behavior of Bi nanowires changed from metallic to semiconductor when the device's critical dimension was reduced to below 50 nm. It is a solid experimental evidence of the quantum confinement-induced bandgap theory. Additionally, it has been found in the present work that resistivity of individual Bi nanowire increased as linewidth decreased indicating size effect occurred in the Bi nanowires. Dual side-gate structures were formed adjacent to the Bi nanowires in an attempt to modulate the current. Measurements showed a 7% of current modulation. The small current modulation suggested the high carrier density in the nanowire which has prevented the full depletion of free carriers. 100 nm-diameter Bi nanodot structures were fabricated utilizing proximity effect of e-beam writing. Precise control of electron doses and process conditions led to the successful fabrication of sub-nanometer tunneling junctions to the nanodots. Significant non-linear current-voltage (I-V) characteristic was observed at low temperatures. The step like I-V characteristic was a strong indication of

energy level spacing in the zero-dimensional nanodot structure. The successful observation of energy level spacing in a relatively large nanodot is due to the small effective mass of bismuth material which leads to a measurable energy level spacing.

Résumé

Bismuth (Bi) est un matériel électronique unique qui a une petite mass effective ($\sim 0.001 m_e$) et un long parcours moyen de porteur (100 nm à 300K). Il est particulièrement approprié pour l'étude de phénomènes à l'échelle nano comme l'effet de la taille et l'espacement de niveaux d'énergie. Dans cette thèse, des dispositifs nanoélectroniques basés sur le Bismuth ont été étudié. Ces dispositifs ont été fabrique à l'aide d'une combinaison de deux techniques : l'écriture par faisceau électronique et l'évaporation thermique. Les dimensions des dispositifs fabriques ont été dans l'ordre de 100 nm. Toutes les structures ont été optimisées pour la caractérisation électrique individuelle. Trois types de dispositifs ont fait l'objet de cette étude : des nano-fils Bi, des nano-fils Bi avec double-grille latérale et des nano-points Bi. Dans l'étude de nano-fils Bi, le phénomène de la transition métal-à-semiconducteur et l'effet de la taille ont été observés. Le comportement de la conduction des nano-fils Bi a changé de métallique à semiconducteur quand la dimension critique du dispositif a été réduite au dessous de 50 nm. Cette dernière est une forte évidence expérimentale pour la théorie sur l'induction de bandes interdites par l'emprisonnement quantique. De plus, au cours de cette recherche, il a été constaté que la résistivité individuelle des nano-fils Bi augmente à mesure que la largeur est diminuée, indiquant l'occurrence de l'effet de la taille sur les nano-fils Bi. Des structures à double-grille latérale ont été formées auprès de nano-fils dans une tentative pour moduler le courant. Les mesures ont démontrées une modulation de courant de 7%. Cette petite modulation de courant suggère l'existence d'une haute densité de porteur dans le nano-fil qui prévient l'appauvrissement complète de porteurs libres. Des structures nano-points Bi de 100 nm en diamètre ont été fabriquées à l'aide de

l'effet de proximité de l'écriture à faisceau électronique. Un control précis de la dose d'électrons et des conditions du processus ont permis la fabrication avec succès de jonctions a effet tunnel sous-nanomètre aux nano-points. Une importante caractéristique non-linéaire du courant-tension (I-V) a été observée a des basses températures. Une caractéristique I-V a échelon est une forte indication de l'espacement de niveaux d'énergie dans la structure zéro-dimensionnelle du nano-point. L'observation de l'espacement de niveaux d'énergie dans un nano-point relativement large est possible grâce à la petite masse effective du matériel bismuth qui rend l'espacement de niveaux d'énergie mesurables.

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Chapter 1: Introduction

1.1 The quest for nanoelectronic devices

Over the past 30 years, the performance of digital integrated circuits (ICs) has improved enormously. The computational power of modern computer doubled every two years. This amazing increase of "digital" power brought a better, more efficient and more comfortable life to everybody in the world. Behind this remarkable result, scientists and engineers in the solid-state device community played an important role. The community devoted to build a faster IC with more functionality and at lower cost. To achieve theses goals, they decided to reduce the size of the key component of the ICs, metal oxide semiconductor field effect transistor (MOSFET). The result was astonishing, the size of a state-of-the-art MOSFET logic cell shrank by half and the number of MOSFETs that can integrate into an IC doubled every 24 months [1.1]. This trend has been continued for the past few decades. Currently, the fabrication processes of an advanced commercial MOSFET reach the deep sub-micron region. This is also known as the ultra-large-scale integration (ULSI) era. The feature size of a MOSFET has reached 90 nm in the 4^{th} quarter of 2005 (Intel Corp.) and it operated at a frequency in the giga hertz domain. However, this dramatic increase of MOSFET performance is not without a cost. As the size of MOSFETs reduced, the fabrication cost of ICs increased significantly. A deep sub-micron fabrication facility could cost several hundred millions of dollars. In addition to the cost problem, the shrank MOSFET had many size related operational problems such as source and drain current tunneling, thin gate oxide current leakage, dopant non uniformity, and threshold voltage variation [1.2 – 1.4]. To overcome these issues, the

solid-state device community has developed various techniques to solve these size related problems. It included device structure engineering, such as double-gate field effect transistor, ultra-thin body silicon on insulator (SOI) and band-engineered strained silicon channel transistor; and the introduction of new materials, such as high-K gate dielectric materials and copper interconnection. Nevertheless, the improved MOSFET is still operated based on the bulk-effect which is to manipulate the movement of a large amount of electrons in a silicon crystal. It is predicted as the feature size of MOSFETs reduces to the nanometer region, charge quantization and quantum tunneling will become severe problems in the bulk-effect MOSFETs. Eventually, quantum effects will cause unacceptable statistical variations in the characteristics of the MOSFET and the ICs will fail to operate. Knowing these problems, researchers have invented alternative nanoelectronic devices that can perform logic function in the nanometer scale region to replace or co-operate [1.5] with the MOSFETs. There are several novel nanoelectronic devices proposed with very different operating principles. These novel nanoelectronic devices can generally be divided into two main categories: quantum-effect nanoelectronic devices and molecular nanoelectronic devices [1.6 – 1.8]. Quantum-effect nanoelectronics operate based on the quantum mechanics principle such as tunneling and charge quantization. The proposed quantum-effect nanoelectronics included quantum wire transistors, quantum dots devices, resonant tunneling devices (RTD) and single-electron devices (SED) [1.9, 1.10]. On the other hand, molecular nanoelectronics operate based on the interaction of molecules. The proposed molecular nanoelectronics included carbon nanotube FET and electric field molecular switch [1.11, 1.12]. Presently, both quantum-effect nanoelectronics and molecular nanoelectronics are still in their early research stages. Certain experiments have been conducted in laboratories to demonstrate

the basic functions of these novel nanoelectronic devices. Some researchers have even demonstrated simple logic functions. But most of them are still looking for the right materials, the proper fabrication processes and the optimal device structure. It is believed that nanoelectronic devices will not become a major component in the IC market until the next decade. The road to realize nanoelectronic devices is still long and rough. The solid-state device community again devoted their efforts, and for many researchers, their whole career life, in researching the next generation nanoelectronic devices.

1.2 Bismuth material and quantum-effect nanoelectronics

Bismuth (Bi), a group V semi-metal element, is a very special material. It has been known for a long time for its enormous diamagnetism [1.13]. It has a large electrical resistance and has the highest Hall effect compared to all other known metals (i.e., the greatest increase in electrical resistance when placed in a magnetic field) [1.14]. Because of its unique properties, magneto-resistance effect in bismuth has been under intensive investigation for many years. This material is also used to form superconductor when alloyed with other materials because of its huge diamagnetism. Apart from its special magnetic characteristic, it has another unique electrical property which gives it additional scientific research value. This unique electrical property is the very small electron effective mass (m_e^*). The reported Bi effective mass is in the order of $0.001m_e$ [1.15] depending on the crystal orientation. Owning to the extremely small effective mass, bismuth is the ideal material to study quantum-effects. In order to study the quantum-effects, device dimensions have to be reduced to values in the order of the material's carrier mean free path. For example, devices fabricated from silicon need to have a dimension of a few nanometer in order to allow the quantum-effects to be observed. The fabrication of these ultra small devices is one of the major obstacles to study the topic in most of the materials. Thanks to the small effective mass of bismuth material and the corresponding long carrier mean free path (in the order of 100 nm), it is possible to observe the quantum-effects in a relatively large bismuth device. By employing modern fabrication equipment and processes, bismuth based nanoelectronics can be fabricated reliably and defectlessly. Nanoelectronics which operate based on the quantum-effects make perfect match with bismuth which provides an easy access to the

quantum-effects. Bi nanoelectronics are believed to be one of the most suitable known devices for studying the quantum-effect nanoelectronics.

Recently, single crystal Bi nanowires with diameters less than 100 nm have been fabricated successfully by a group of researchers at MIT led by Dr. Dresselhaus [1.16]. The research group has been studying Bi nanoelectronics for almost a decade. They have studied the transport property, the thermoelectric property [1.17-1.20] and the magneto-resistance property of Bi nanowires [1.21-1.22]. One of their most significant achievements was the understanding of metal-to-semiconductor transition in low dimensional Bi nanoelectronics. They found that bandgap can be created in Bi nanoelectronics if the critical dimension of the device is less than 50 nm. The above conclusion was supported by both theoretical and experimental results. Sparked by their discovery, more researchers around the world have joined the research in Bi nanoelectronics. Their works are not focused only on electrical properties of Bi nanowires but a wide range of topics such as optical properties of Bi nanowires [1.23], Bi ballistic devices [1.24], as well as the continuation study of Bi alloyed superconductors. With the efforts from these brilliant brains and the global attention on nanotechnology, it is believed that breakthroughs in bismuth based devices will be achieved in the foreseeable future.

1.3 Thesis objectives

The main objective of this thesis is to study the non-classical electrical properties of bismuth based devices. The present work emphasizes on the fabrication and the electrical characterization of individual Bi nanoelectronic devices in the Electronic Devices and Materials laboratory (EDM Lab.) at McGill University. Dimensions of the fabricated device are in the order of 100 nm. In order to study different aspects of Bi nanoelectronics, the thesis work has been divided into three phases. Each phase has a particular goal and is consisted of a combination of experimental work, computational work and numerical simulation. The goal of each phase is specified below:

- Phase I (Chapter 3): In the first phase, the thesis work is focused on Bi nanowires. The goal is to observe and study nano scale related phenomena, namely the size effect and the metal-to-semiconductor transition. It consists of experimental and computational works.
- Phase II (Chapter 4): In the second phase, work is focused on Bi nanowires with dual side-gate structures. The goal is to study the effect of external voltage coupling to the nanowire current. Potential is coupled from the side-gates to individual Bi nanowire. It consists of experimental work and numerical simulation.
- Phase III (Chapter 5): In the last phase, research work is focused on Bi nanodots. The goal is to study the energy level spacing and non-linear current-voltage characteristic of Bi nanodots. It consists of mainly experimental works.

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Chapter 2: Properties of Bismuth

2.1 Crystal structure

Bismuth (Bi) has a rhombohedral crystal structure. A schematic diagram of the rhombohedral structure is shown in Figure 2.1. It has three equal axes of length *a* inclined at the same angle α to one another [2.1]. For Bi, the value of *a* is 4.74 Å and the angle α is 57°16'. Figure 2.2 shows a bismuth unit cell which contains two atoms with lattice basis of (*u, u, u*) and (*-u, -u-, -u*). *u* has a value of 0.237. Each atom has three nearest neighbors at a distance *d* (3.11 Å) and three far neighbors at a distance *d'* (3.47 Å) [2.2]. A Bi atom contains 83 electrons in six energy levels while only 5 electrons are situated in the outer most energy level [2.3]. The number of electrons occupying each energy level and the electron configuration are summarized in Table 2.1a and 2.1b respectively. Bi has a Brillouin zone which can accommodate exactly five valence electrons. A reduced Bi Brillouin zone is shown in Figure 2.3 [1.14]. The energy discontinuities around the Brillouin zone are sufficiently large to maintain a low number of vacancies in the zone. With the help of external energy such as thermal energy, some of the electrons in the Brillouin zone are capable of crossing to the next zone and become free electrons. The number of electrons per atom in the upper zone is small resulting in a low free carrier density. The free carrier density is in the order of 10^{17} cm^{-3} at low temperatures [1.15].

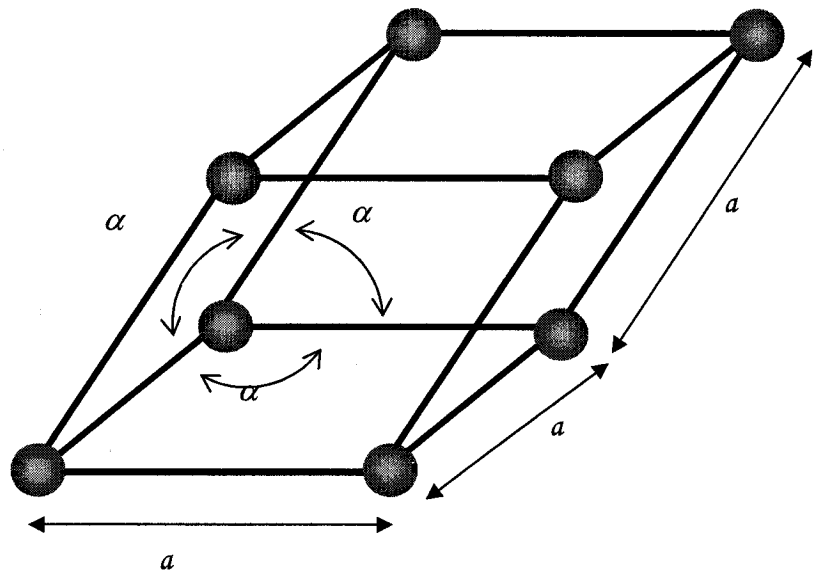

Figure 2.1: A rhombohedral structure.

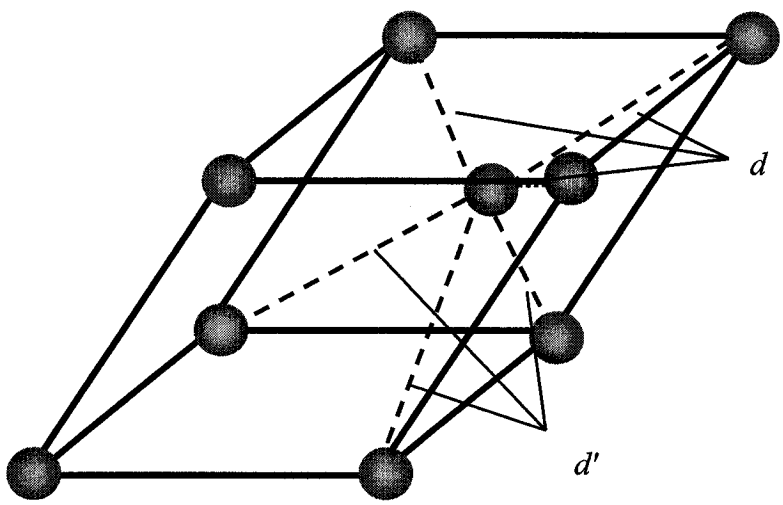

Figure 2.2: A bismuth unit cell.

Table 2.1a: Electron distribution in the energy levels in bismuth.

Energy level	**Number of electrons**
First energy level	2
Second energy level	8
Third energy level	18
Fourth energy level	32
Fifth energy level	18
Sixth energy level	5

Table 2.1b: Bismuth electron configuration [2.11].

Quantum number	**Electron configuration**
$n = 6, l = 1$	[Xe] $4f^{14}.5d^{10}.6s^{2}.6p^{3}$

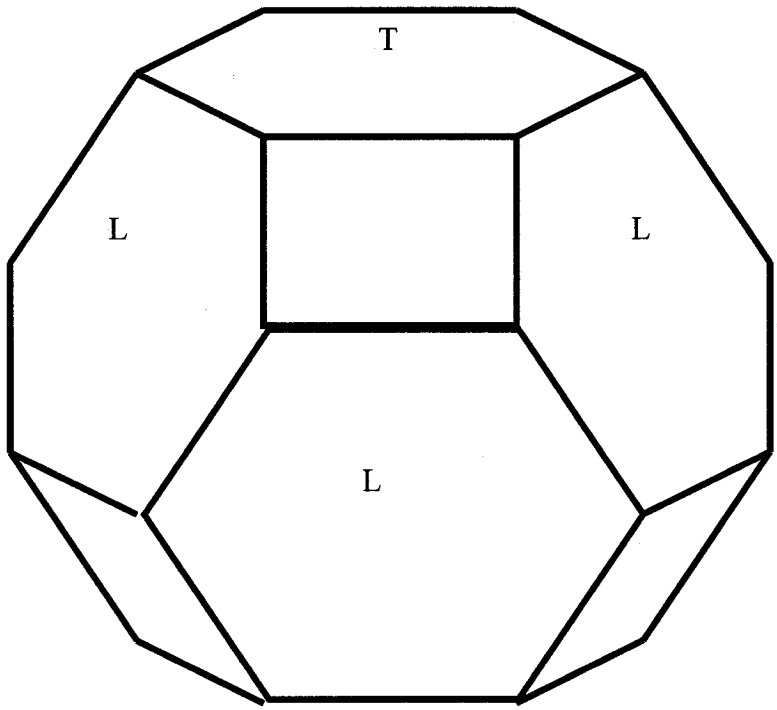

Figure 2.3: Bismuth structure Brillouin zone showing L points of conduction band and T points of valence band.

2.2 Electrical properties of bulk bismuth

The energy band structure of Bi has a Fermi surface consisting of three electron ellipsoids and one hole ellipsoid. Electrons are distributed in the three ellipsoids at the L-points of the Brillouin zone and the holes are situated at the T-point. There is an energy overlap of 38 meV between the L and T points in the bulk Bi material. This small overlap of the conduction band and valence band dictates the metallic conduction characteristic of bulk Bi material. A simplified energy band diagram for bulk Bi is shown in Figure 2.4. Bi is known to have a very small effective mass. Extensive study on Bi effective masses has been carried out in the 70s [1.15, 2.4]. The effective mass was found to be in the order of $0.001 m_e$ depending on the crystal orientation. Electron and hole effective mass tensors in the trigonal axis system normalized to the free electron mass (m_e) are shown in Equation 1 [2.12]. Other materials with small effective masses are summarized in Table 2.2 for comparison purpose.

$$m_e^* = \begin{bmatrix} 0.00119 & 0 & 0 \\ 0 & 0.1175 & 0 \\ 0 & 0 & 0.00516 \end{bmatrix} \quad m_h^* = \begin{bmatrix} 0.064 & 0 & 0 \\ 0 & 0.064 & 0 \\ 0 & 0 & 0.69 \end{bmatrix} \qquad \text{(Eq. 1)}$$

The carrier density of Bi is in the order of 10^{17} cm^{-3} and it is temperature dependent. The computed carrier density is 3 x 10^{17} cm^{-3} at 4.2 K , 4.55 x 10^{17} cm^{-3} at 77 K and 24.5x10^{17} cm^{-3} at 300 K [2.5, 2.6]. The carrier density is much less than other metals (~10^{20} cm^{-3}) but larger than intrinsic semiconductor (~10^{10} cm^{-3}). Because of this "intermediate" carrier density, Bi is categorized as semi-metal material. The extremely small effective mass and unusual low carrier density in bismuth resulted in an exceptionally long carrier mean free path. The mean free path is ~ 0.1 mm at 4 K to ~ 100 nm at 300 K [1.14].

Correspondingly, the carrier mobility decreases by ~3500 times at the same temperature range, $\mu_l = 110 \times 10^6$ cm^2/V-sec at 4.2 K and $\mu_l = 3.2 \times 10^4$ cm^2/V-sec at 300 K [1.14]. Because of this temperature-dependent mobility, the resistivity decreases linearly with reducing temperature. It is thus evident that Bi bulk material exhibits metallic conduction behavior. Experimental [2.7] and theoretical studies [2.8] have both shown a linear relationship between the resistivity of Bi bulk material and temperature as described in Equation 2.

$$\rho_{bulk} = 3.88 \times 10^{-7} T(\Omega \cdot cm) \quad \text{(Eq. 2)}$$

This temperature-dependent metallic conduction behavior in bulk Bi material suggests that the temperature dependent carrier transport is mainly due to mobility rather than electron density. This is because the mobility value increases by 2 orders of magnitude as the temperature is decreased from 300 K to 4 K while the carrier density remains in the same order of magnitude. However, as Bi device dimensions are reduced to nanometer scale, the carrier transport mechanism changes dramatically. The carrier transport mechanism changes from metallic conduction behavior to semiconductor conduction behavior. Carrier transport is no longer dominated by mobility but by the carrier density. The device resistivity does not decrease but increase with reducing temperature. The conductivity behavior of Bi "nano" devices is completely opposed to its bulk material counterpart. This unique "nano scale" behavior is the main investigation area of Phase I of this thesis. Details on the investigation of Bi "nano scale" device carrier transport mechanism are presented in the next chapter on Bi nanowires.

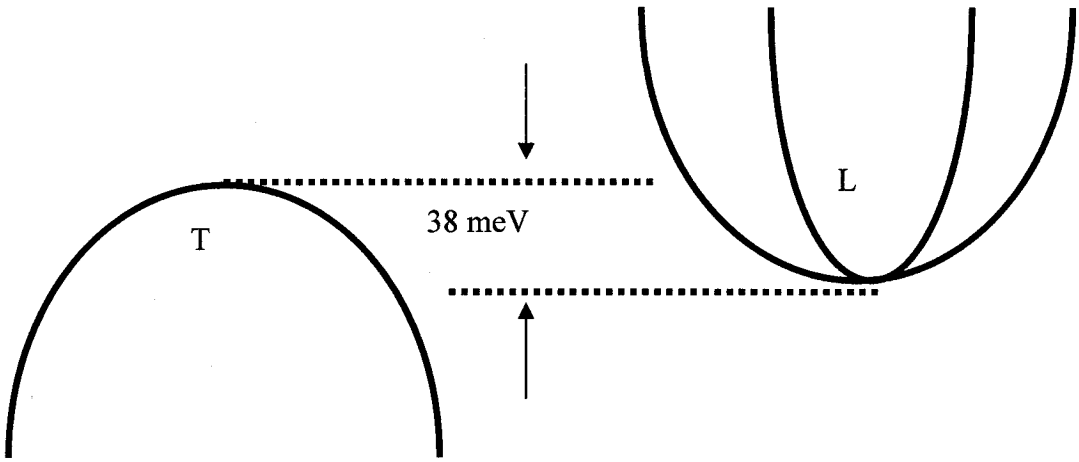

Figure 2.4: An energy band diagram for the heavy and light electrons and for holes in bulk Bi material.

Table 2.2: Materials with small effective masses.

Material	**Transverse electron mass ($m_{e,t}$*) at 300 K**	**Reference**
Bi	$0.00119m_e$	[1.18]
InSb	$0.014\ m_e$	[2.9]
InAs	$0.023\ m_e$	[2.9]
GaAs	$0.063\ m_e$	[2.9]
InP	$0.080\ m_e$	[2.9]
Ge	$0.082\ m_e$	[2.10]
Si*	$0.190\ m_e$	[2.10]

*Si is not considered to have small effective mass. The indicated value is for comparison purpose only.

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Chapter 3: Bi Nanowires

A Bi nanowire is a very interesting device for scientific electronic research. This is because of its unique small electron effective mass (~0.001 m_e) and very long mean free path (100 nm at 300 K). The dimension for Bi based devices to observe "nano scale" behavior is in the order of 100 nm. This critical dimension is much larger than those required for devices using other materials such as silicon (Si) and metals. For Si based devices, the critical dimension is in the order of 1 nm while for metal based devices, value is below 0.1 nm. Obviously, Bi has a clear advantage on the fabrication restriction over other materials. This is because Bi based devices with 100 nm-dimension can be fabricated relatively reliably and reproducibly by using advanced fabrication equipment and processes. Not surprisingly, researchers have already acknowledged the advantages of Bi material and have fabricated Bi nanoelectronic devices, namely Bi thin films and nanowires for research purposes. Recently, high quality single crystal Bi nanowires have been fabricated successfully by vapor/liquid phase injection to anodic alumina templates [1.16] and by electrodeposition into membranes with nanometer size pores [3.1, 3.2]. Bi nanowires fabricated by these methods were embedded in the hosting templates/membranes. Early characterizations of Bi nanowires were in bundle measurements only. The electrical contacts were made on both sides of the templates/membranes to connect a bundle of Bi nanowires. Electrical measurements were then performed on this bundle of Bi nanowires. Characteristics of single Bi nanowire were deduced from the measurements by dividing the number of nanowires connected in the bundle. Therefore, the characteristics of single Bi nanowire measured using the above method were estimation only and not results of an individual

characterization. Nevertheless, the bundle measurement had demonstrated semiconductor conduction behavior in the Bi nanowires. This behavior is opposite to the metallic conduction behavior observed in bulk Bi devices. The change of conduction behavior is an evidence of energy band gap creation. This band gap creation has been predicted by solid-state theory [1.17, 1.18] and now supported by the experimental results [1.20, 1.21]. Characterizations of a single Bi nanowire have been attempted [3.2 – 3.5]. The single Bi nanowire was extracted from the hosting templates/membranes and electrical contacts were formed on the nanowire. It was found that the contact resistance between the Bi nanowire and contact pads was significant and various methods were attempted to form good contacts.

In this work, Bi nanowires were fabricated using a combination of electron beam (e-beam) writing and thermal evaporation techniques. The Bi nanowires were formed across pre-fabricated Bi bonding pads in an attempt to minimize the contact resistance. The nanowires formed using this method had rectangular cross-sections. The dimensions of the cross-sections were 50 nm by 70-200 nm (thickness by width). Although the fabricated Bi nanowires were believed to have a polycrystalline structure, they exhibited electrical properties similar to the single crystalline Bi nanowires. They both have semiconductor conduction behavior. This semiconductor behavior suggested that the band gap creation also took place in the polycrystalline Bi nanowires with a rectangular cross-section. In addition, size effect, a unique phenomenon to nano scale device, was also observed. The measurement results were compared to established mathematical size effect models, Dingle model [3.6] and MS model [3.7]. In their models, it has been suggested that the carrier mobility of the fabricated Bi nanowires was grain boundary scattering dominated. Details of the Bi nanowire carrier transport properties, fabrication

processes and characterizations of this work are discussed in the following sections in this chapter.

3.1 Bi Nanowires carrier transport

Size effect

Size effect, also known as ordinary or classical size effect, is one of the unique electrical phenomena in nano scale electronic devices. This effect is the shortening of electron mean free paths by collisions with the boundaries of the low dimensional devices. The resultant characteristic is the increase of carrier scattering from the device boundary which leads to the increase of resistivity. Investigation of this effect dated back to 1938, when Fuchs [3.8] first derived an expression for the resistivity of thin films. He found that the resistivity of thin films increased with the decrease in thickness. After the discovery of the effect, the study of size effect on different materials was continued by several researchers. The materials studied include indium [3.9], gold [3.10], copper [3.11, 3.12], and bismuth [3.13]. Compared to the above materials, bismuth has unique characteristics of long electron mean free paths and has been selected for the present research (refer to section 2.2). Because of the very long mean free path, Bi based devices can have large critical dimensions in order of 100 nm still exhibiting the size effect. This large critical dimension can be obtained using controlled film deposition or advanced lithography techniques. Early studies of size effect in Bi have focused on Bi thin films [3.14, 3.15] where researchers measured the change of resistivity with different film thicknesses. With the help of modern fabrication equipments, Bi nanowires with diameters less than 100 nm can be fabricated. Consequently, the size effect of Bi nanowires was studied in several experiments [3.13, 3.16 and 3.17]. It was found that the

resistivity of cylindrical Bi nanowires increases with the decrease in the wire diameter when the diameter is less than the carrier's mean free path (~100 nm).

The increase of resistivity is due to the wire/grain boundary scattering and ionized impurity scattering. In an effort to compare the measurement results with the size effect theory and to extract material parameters, mathematical models of the size effect were proposed. Two of the most commonly used size effect models were Dingle model [3.6] and MS model [3.7]. In Dingle model, electron scattering at the wire boundary was considered to be either elastic or inelastic. For elastic scattering, electrons bouncing back from the wire boundary did not lose any momentum and continue to travel in the wire. In this case, the resistivity did not change. For inelastic scattering, an electron lost momentum after colliding with the wire boundary and the carrier mean free path reduced. In this case, the resistivity is given by:

$$\frac{\rho_o}{\rho} = k - \frac{3}{8}k^2\left(\ln\frac{1}{k} + 1.059\right) - \frac{2k^3}{15} \quad \text{(Eq. 3)}$$

$$k = \frac{d}{l} \quad \text{(Eq. 4)}$$

where k is the ratio of wire diameter d to electron mean free path l and ρ_0 is bulk material resistivity. In the case of elastic scattering, the ρ/ρ_o value is equal to 1. The Dingle model is used to distinguish the scattering characteristic of electrons at the wire boundary. While inelastic scattering is almost always observed, Dingle model alone did not provide the complete picture of carrier transport mechanism in the nano scale devices. But the model can be used in conjunction to another model, the MS model, to fully explain the carrier transport characteristic under the influence of size effect. In the MS model, Mayadas and Shatzkes observed that electron scattering not only happened at the device

boundary, but also at the grain boundary leading to a further increase in the electrical resistivity. As a result, they introduced the scattering probability at the grain boundary in their model. The resultant resistivity equation for the MS model is:

$$\frac{\rho_o}{\rho} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right] \quad \text{(Eq. 5)}$$

$$\alpha = \frac{l}{d}\frac{R}{1-R} \quad \text{(Eq. 6)}$$

where l is the electron mean free path, d is the average grain diameter, R is reflection coefficient representing the probability of an electron is reflected at a grain boundary and ρ_0 is bulk material resistance. The MS model provided a sophisticated equation for studying size effect of polycrystalline devices where electron reflected from grain boundary cannot be ignored. Since the two models, Dingle model and MS model, described different scattering mechanisms, they did not contradict each other and can be combined to form a grand model. The model is formed by adding the two resistivities from the two models together. This combined model considered both inelastic scattering and grain boundary scattering. Although it has a potential to over estimate the effect of scattering, the combined model can be treated as the upper limit of the size effect in a nano scale device. On the other hand, the elastic version of Dingle model can be used as the lower limit since it assumed perfect collisions. By using the lower and upper limits of the size effect model, as well as the MS model, experimental results can be fitted using the equations and the scattering parameters can be extracted. Accordingly, the scattering mechanism of a particular nano scale device under the influence of size effect can be determined.

Metal-to-semiconductor transition

Bismuth, a semimetal material, exhibits metallic conduction behavior when it is in bulk material form. Its conduction carrier transport is mobility dependent and the transport mechanism is governed by phonon scattering. As temperature increases, phonon scattering due to thermal vibrations also increases and it leads to a reduction of carrier mobility [3.18]. On the other hand, carrier density is relatively independent of temperature due to the overlap of conduction band and valance band (refer to Figure 2.4). Because of the temperature dependent mobility and temperature independent carrier density, bulk Bi material conductivity acts like metal. The resultant conductivity characteristic is the decrease of conductivity as the temperature is raised. In 1988, a group of researchers at Massachusetts Institute of Technology led by Dr. Dresselhaus observed metal-to-semiconductor transition in Bi nanowires with diameters less than 100 nm due to quantum confinement of energy levels [1.17]. They suggested that when the one dimensional electron gas is confined inside a cylindrical potential well (in this case nanowire), the energy level E_{ij} for electrons and holes to occupy are quantized due to the quantization of the transverse momentum. This is known as quantum confinement effect. The energy level can be determined using Equation 7:

$$E_{ij} = \frac{\hbar^2 k_z^2}{2m_z^*} + \frac{\hbar^2 \chi_{ij}^2}{2m_d^* d^2} \qquad \text{(Eq. 7)}$$

where $\hbar$ is Planck's constant, k_z and m_z^* are the momentum and the effective mass of the electron along the nanowire axis, m_d^* is the dynamic electron effective mass, d is the diameter of the nanowire and χ is the roots of Bessel function. The quantization of energy level forces the energy band position to rely on the nanowire diameter and crystal

orientation. For a sufficiently small diameter, the energy band spacing can be large enough such that the valence band no longer overlaps with the conduction band. With this critical diameter, a bandgap is created and the Bi nanowire changes from metal to semiconductor. Figure 3.1 shows a simplified band diagram showing the shift of energy levels in the Bi nanowire. Since the energy level spacing is dependent on the electron effective mass which is crystal orientation dependent, the critical diameter for the metal-to-semiconductor transition is also crystal orientation dependent. A mathematical model has been developed by the same group to visualize the bandgap creation of Bi nanowires [1.18]. The mathematical model of the quantum confinement-induced bandgap considered the non-parabolic conduction band for the Bi nanowires. Assuming the electrical current is flowing along the trigonal (z) direction, the conduction subband extrema can be computed as:

$$\Delta E_{e,mn} = -\frac{E_g}{2} + \frac{1}{2}\sqrt{E_g^2 + 2E_g\hbar^2\left[\frac{k_{x,m}^2}{m_1} + \frac{k_{y,m}^2}{m_2}\right]} \quad \text{(Eq. 8)}$$

where the k vector is quantized in the x and y direction, $k_{x,m}=m\pi/a$ and $k_{y,n}=n\pi/a$ with m, n = 1, 2, 3,..., a = nanowire diameter, E_g = 13.8 meV is the L-point direct bandgap and m_1 = $0.00119m_o$, m_2 = $0.1175m_o$ are the effective mass elements where m_o is the free electron mass. The quantum confinement for the T-point valence band is computed using parabolic band approximation. The quantum confinement-induced bandgap as a function of Bi nanowire diameter at 77 K for nanowires along the trigonal direction is shown in Figure 3.2. The critical diameter for the metal-to-semiconductor transition is approximately at 50 nm where the bandgap overlap is reduced to 0 meV. The computed critical diameters for Bi nanowires with different crystal orientations are summarized in

Table 3.1 [1.18]. The carrier transport of Bi nanowires with diameter less then the critical dimension does not have metallic conduction behavior. This is due to the creation of bandgap causing a reduction in the number of conduction electrons. As the temperature decreases, less electrons are available in the conduction band for electrical conduction. At the same time, the electron mobility is limited by the low dimension nanowire due to size effect where the electron mean free path is restricted. The resultant characteristic is the decrease of resistivity as temperature is increased. This characteristic is exactly opposite to the one of bulk Bi material. The Bi nanowires are said to have semiconductor conduction behavior once they reached the metal-to-semiconductor transition point.

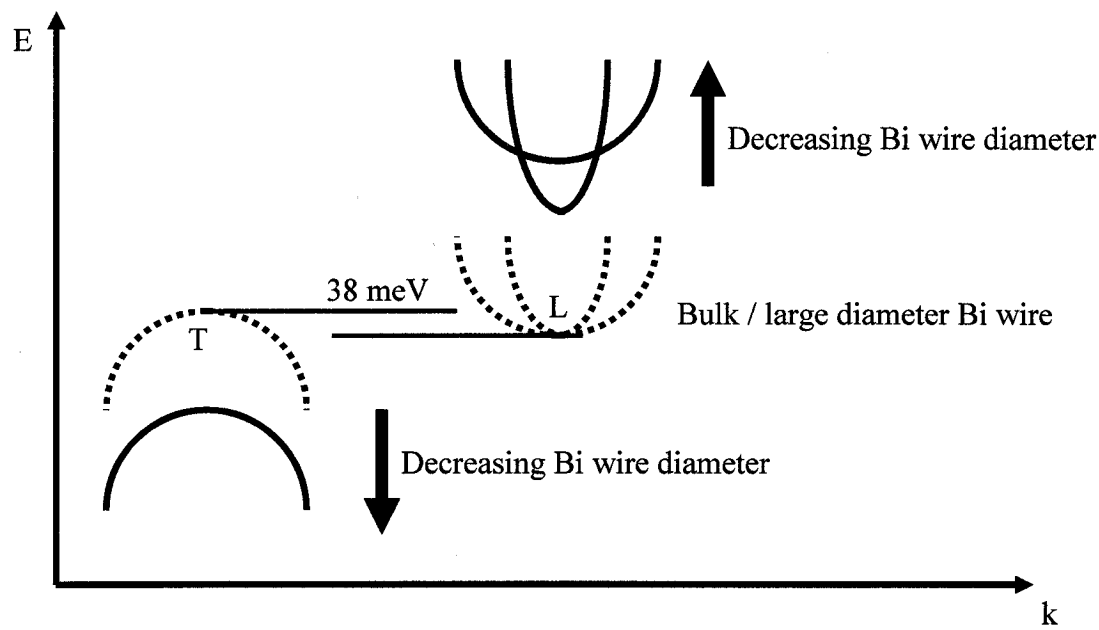


Figure 3.1: A simplified energy band diagram for Bi nanowires.

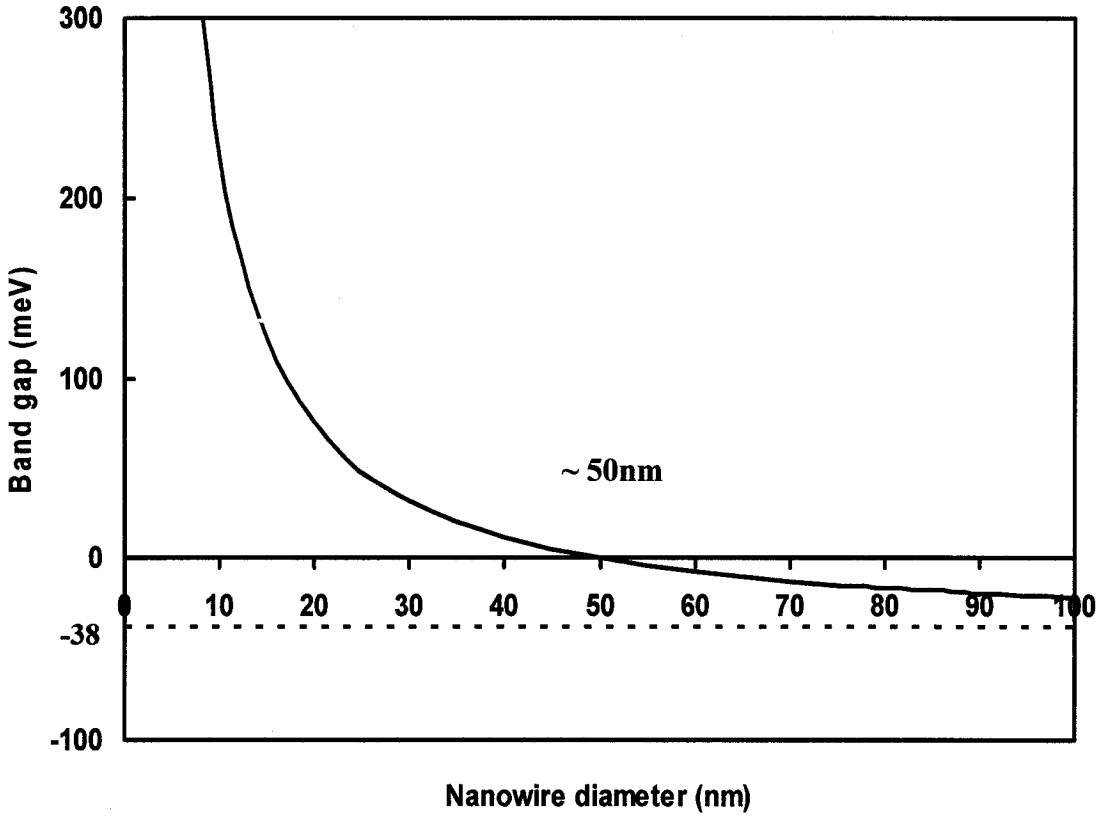


Figure 3.2: The quantum confinement-induced bandgap (Eq. 8) as a function of Bi nanowire diameter at 77K for nanowires along the trigonal direction. The critical diameter for the metal-to-semiconductor transition is approximately at 50 nm where the bandgap overlap is reduced to 0 meV. [1.18]

Table 3.1: Metal-to-semiconductor transition diameter of Bi nanowires [1.18].

Nanowire principle direction	**Critical diameter (nm)**
Trigonal wires	52.1
Binary wires	34.5
Bisectrix wires	41.3

3.2 Bi nanowires fabrication

Bi nanowires can be fabricated using various methods. The methods include direct patterning using advanced lithography system, vapor/liquid phase injection to anodic alumina templates [1.16], electrodeposition into membranes with nanometer size pores [3.1, 3.2] and, in some cases, exotic fabrication techniques such as the stretch of bulk material using scanning tunneling microscope (STM) [3.19]. Different fabrication methods will result in different Bi nanowires of different qualities. The vapor/liquid phase injection and electrodeposition methods have been reported to provide high quality single crystal Bi nanowires [1.16]. However, the nanowires fabricated using these methods were always in a bundle form. It is difficult to extract the bundled nanowires and the characterization of individual nanowire required extra manipulation. As a result, bundles of Bi nanowires were characterized together. Characteristic of a single Bi nanowire was then deducted from the bundle measurements. Since the exact number of Bi nanowires in a bundle was uncertain, the estimated single Bi nanowire characteristic could be under or over estimated. Alternatively, direct pattering of Bi nanowires may provide high level of position control. Nanowires can be placed in selected locations for individual characterization. However, direct patterned Bi nanowires were usually in polycrystalline form. Electron beam (e-beam) writing technique is one of the most commonly used advanced direct pattering methods. It can be used to define nanowires at selected positions with excellent control of linewidth and length. This method is very suitable for the fabrication of individual Bi nanowire for characterization. In this work, e-beam writing technique was used to fabricate Bi nanowires with rectangular cross-sections. The linewidth of Bi nanowires were controlled by adjusting the electron dose of

e-beam writing. The fabricated linewidth ranged from 70 to 200 nm. The thickness of the nanowires was 50 nm, a value equal to the critical dimension of metal-to-semiconductor transition value (refer to Table 3.1). The thickness was controlled by the thermal evaporation technique. Each Bi nanowire was fabricated across two Bi bonding pads which were intended for individual characterization. The complete Bi nanowires fabrication process was developed in the Electronic Devices and Materials Laboratory (EDM Lab.) in McGill University. Two key fabrication techniques used were thermal evaporation and e-beam writing. The details of each technique are discussed in the following sections.

Thermal evaporation

Thermal evaporation is one of the physical vapor deposition techniques for depositing metal thin films. The principle of thermal evaporation is simple; material to be evaporated is placed on a heating element inside a vacuum chamber, it is then heated to a temperature often high than the boiling point. The evaporated material condenses on samples positioned above the heating element to form a layer of thin film. This simple technique provides an easy method to deposit thin films. In this method, the thickness of thin film is conveniently controlled by the amount of material evaporated as well as the position of samples. The more material evaporated and the closer the samples placed to the heating element, the thicker the film. However, placing the samples too close to the heating element will result in films with non uniform thicknesses. The optimal distance between the samples and the heating element varies in different thermal evaporation systems. Normally several trial runs are required to determine the right amount of material to be evaporated and the correct position for the samples.

In the Bi nanowires fabrication processes developed in the EDM Lab., Si substrates were used. The evaporation process was performed in a KEY high vacuum system model KV-301. Carefully measured Bi powder was placed in a molybdenum (Mo) boat which was connected to two current electrodes. Samples were mounted 10 cm upside down from the Mo boat. A schematic diagram of the thermal evaporation system is shown in Figure 3.3. Photographs of the KEY system and the Mo boat structure are shown in Figure 3.4. After loading of the powder and substrates, the chamber was first brought to a pressure of 3×10^{-5} torr. At this pressure, the mean free path of atoms or molecules is around 500 cm [3.20], which is much larger than the distance between the Bi

powder and the samples. Hence, the un-wanted interactions between the Bi atoms and residual gases in the chamber can be minimized. The kinetic data for air at room temperature is summarized in Table 3.2. In order to evaporate the Bi powder, a high current was allowed to pass through the Mo boat and heat up the entire structure. Bi powder placed on the Mo boat was evaporated at about 1837 K. Part of the Bi vapor was transferred to the samples above the Mo boat and condensed on the surface to result in a uniform Bi thin film. Several trial runs have been performed in order to determine the optimal conditions for the evaporation process. The amount of Bi powder used in the experiments ranged from 5.0 to 50.0 mg and the corresponding Bi thin film thickness were 50 to 110 nm. An amount of less than 5.0 mg has been observed to result in films with non uniform thickness and non reproducible results. Experimental thickness data on the deposited Bi thin films with various amounts of Bi powder is summarized in Figure 3.5. Scanning electron microscope (SEM) photographs of the deposited films with 5.0 and 40 mg of Bi powder are shown in Figure 3.6. Both photographs showed uniform thin films with no visible defects on the samples. It is noted that an amount of 5.0 mg was selected to deposit thin films with a thickness of 50 nm for subsequent the Bi nanowires fabrication process. The selected conditions provided a reproducible and defect free Bi thin films.

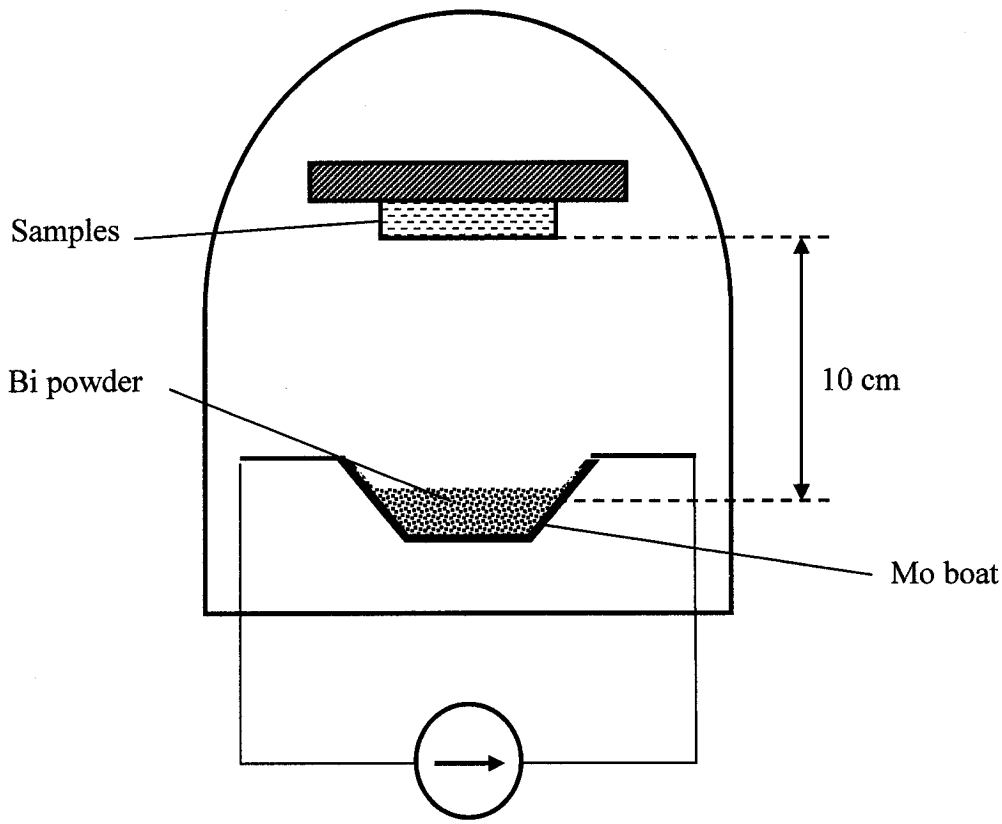
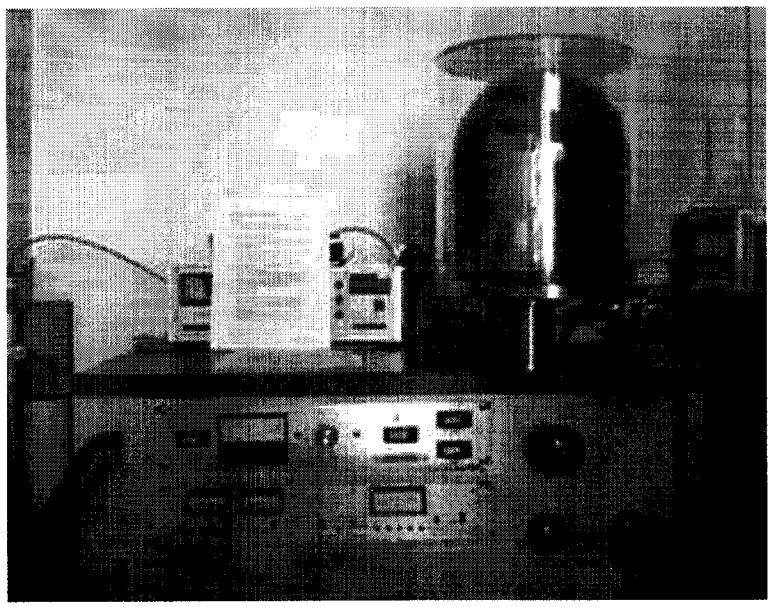
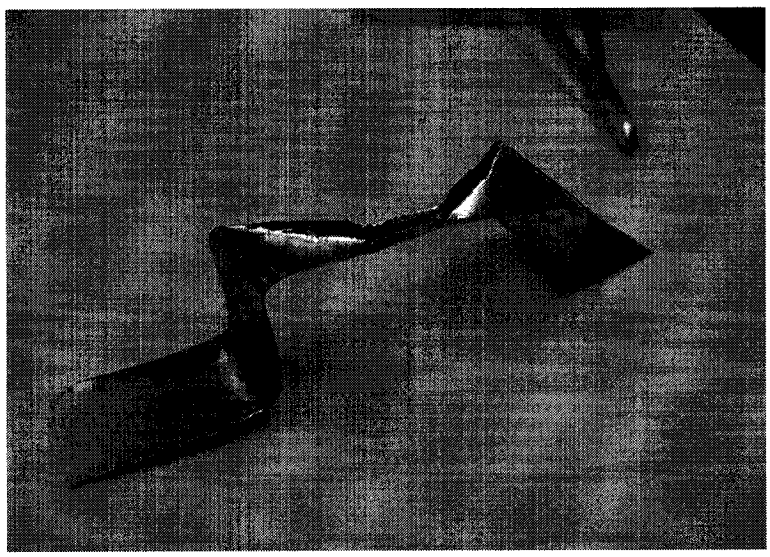


Figure 3.3: A schematic diagram of the thermal evaporation system.



(a)



(b)

Figure 3.4: (a) KEY high vacuum system model number KV-301; and (b) Mo boat structure for the evaporation of Bi powder.

Table 3.2: Kinetic data for air as a function of pressure [3.20].

Pressure (torr)	**Mean Free Path (cm)**
10^{1}	0.5
10^{-4}	51
10^{-5}	510
10^{-7}	5.1×10^{4}

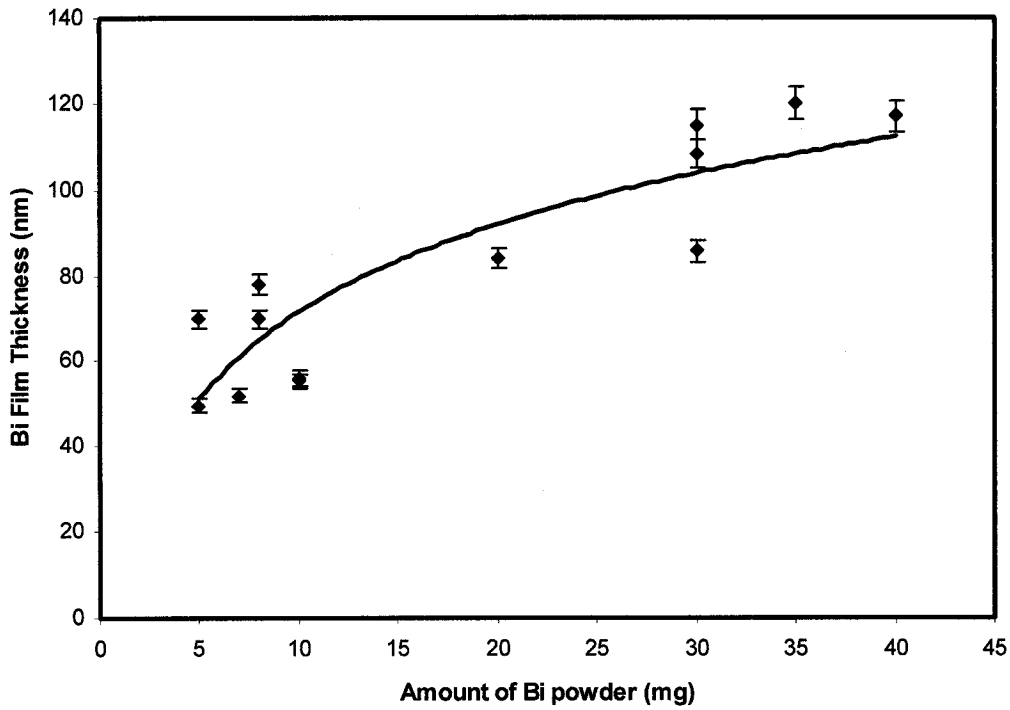
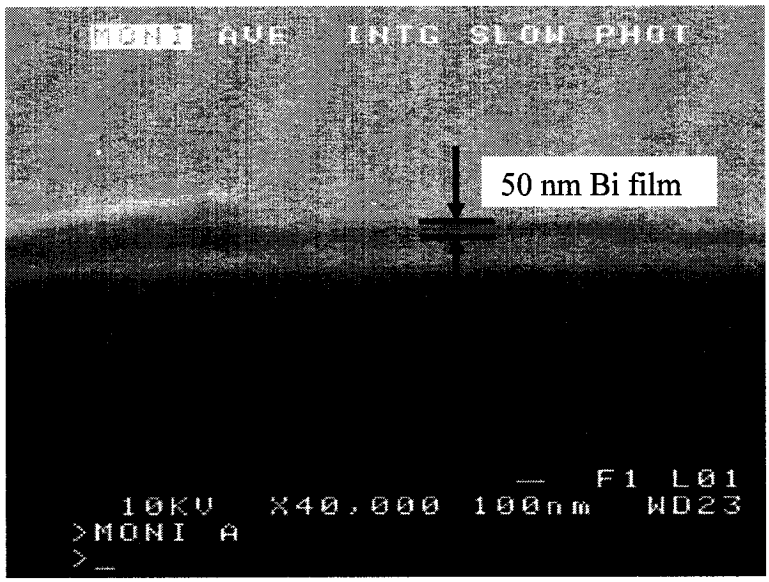
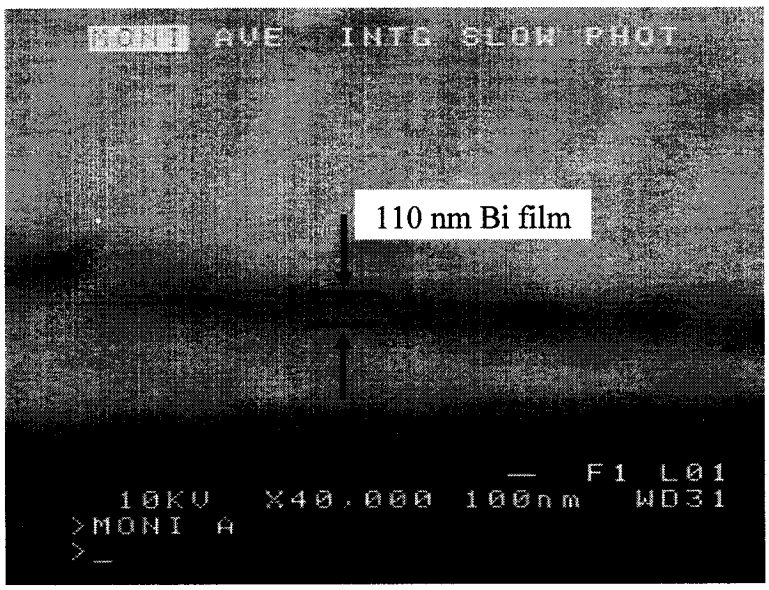


Figure 3.5: Variation of thickness of the Bi thin film with the amount of Bi powder used in the deposition. Data showed with 3% measurement error. Line fitted with logarithmic equation (Arrhenius behaviour [3.25]).



(a)



(b)

Figure 3.6: SEM photographs of Bi thin films formed with (a) 5.0 mg of Bi powder and a thickness of 50 nm; (b) 40 mg of Bi powder and a thickness of 110 nm.

Electron beam writing

Electron beam (e-beam) writing is a very useful technique to define high-resolution patterns. Unlike optical lithography, resolution in e-beam writing is not limited by the diffraction of light, but by electron scattering in the target materials and by the aberrations of the electron optics. In the Bi nanowires fabrication process, the e-beam writing was used to define the linewidth and shape of nanowires. The e-beam writing system used in this work in the EDM Lab. is a custom built system consisting of two main units: a JEOL SEM model number JSM-6100 and a nanometer pattern generation system (NPGS) by J. C. Nabity Lithography System [3.21]. A photograph of the actual system is shown in Figure 3.7. The SEM provided all the e-beam writing hardware such as electron emitter, control stage and electron optics. The NPGS provided software design patterns and the control of electron beam. In the system, electrons were accelerated from the tungsten filament emitter with energy in the order of keV, and then focused and directed to the sample. The linewidth resolution achievable by the system was determined by the scattering of secondary electrons in the sample. As the energetic electrons penetrate the sample, they lose energy by scattering from valence and core electrons while creating secondary electrons at the same time. Consequently, these energetic electrons slowed down in the material as they lose energy. Furthermore, some of the energetic electrons may collide with the nuclei within the semiconductor atoms and scattered to a path different from their original trajectories. The result of the scattered electrons is the creation of secondary electrons not only under the electron beam focus point, but also around the perimeters. This region of scattered secondary electron was called the generation volume. The generation rate is highest in the area close to the

surface directly under the electron beam and is lower in the surrounding regions. The generation volume was visualized by Cohn and Caledonia [3.22]. In their experiments, a collimated electron beam was used to ionize a gaseous material and the fluorescent radiation emission caused by the electron beam was measured. A contour plot based on their result is illustrated in Figure 3.8. The contour plot can be universally applied to solid semiconductor with the distance scaled to the electron range R_e, which is the depth that an average electron could penetrate without large angle scattering. This generation volume dictates the resolution of e-beam writing. As a result, the linewidth of the nanowires relied not only on the focusing condition of the e-beam, but also depended on the scattering of secondary electrons. In the Bi nanowires fabrication processes, electron scattering was controlled by carefully adjusting the electron energy and by controlling the amount of electrons, also referred to as electron dose, incident into the samples.

In a typical electron beam writing process, polymethylmethacrylate (PMMA) is used as a positive e-beam resist. A thin layer of PMMA is usually applied on the sample by spray or spin method. Electron beam is then focused on to the sample to irradiate the PMMA according to the designed patterns. By controlling the electron beam energy and dose, a high-resolution pattern can be obtained [3.23]. In the Bi nanowires fabrication process, a solution of 2% PMMA in chlorobenzene was spun coat on the sample. The PMMA layer thickness was approximately 150 nm. The sample was baked in an oven at 170 °C for 30 minutes to evaporate the solvent. E-beam writing was then performed in the sample chamber of SEM. The electron beam and dose were controlled by NPGS through a hosting computer. Several electron beam energies and doses were used to determine the optimal conditions for the nanowire patterns. Experimental data of linewidth versus electron dose for different electron beam energies is shown in Figure

3.9. It was found that 20 keV electron beam energy with 2 nC/cm of electron dose provide a stable and reproducible results. After the e-beam writing, the sample was developed in Methyl Isobutyl Ketone (MIBK): 2 Propanol (IPA) at a ratio of 1 to 3 for 60 seconds in order to define the patterns. Next, a layer of 50 nm thick Bi thin film was deposited on the sample by the thermal evaporation technique described before. Afterward, a lift-off process using acetone (ACE) was performed to remove the un-wanted Bi regions and to leave behind the Bi nanowire structures. Using these conditions, nanowires with linewidth as small as 70 nm can be achieved using our writing system. SEM photographs of several fabricated Bi nanowires with linewidths of 200, 100 and 70 nm are shown in Figure 3.10.

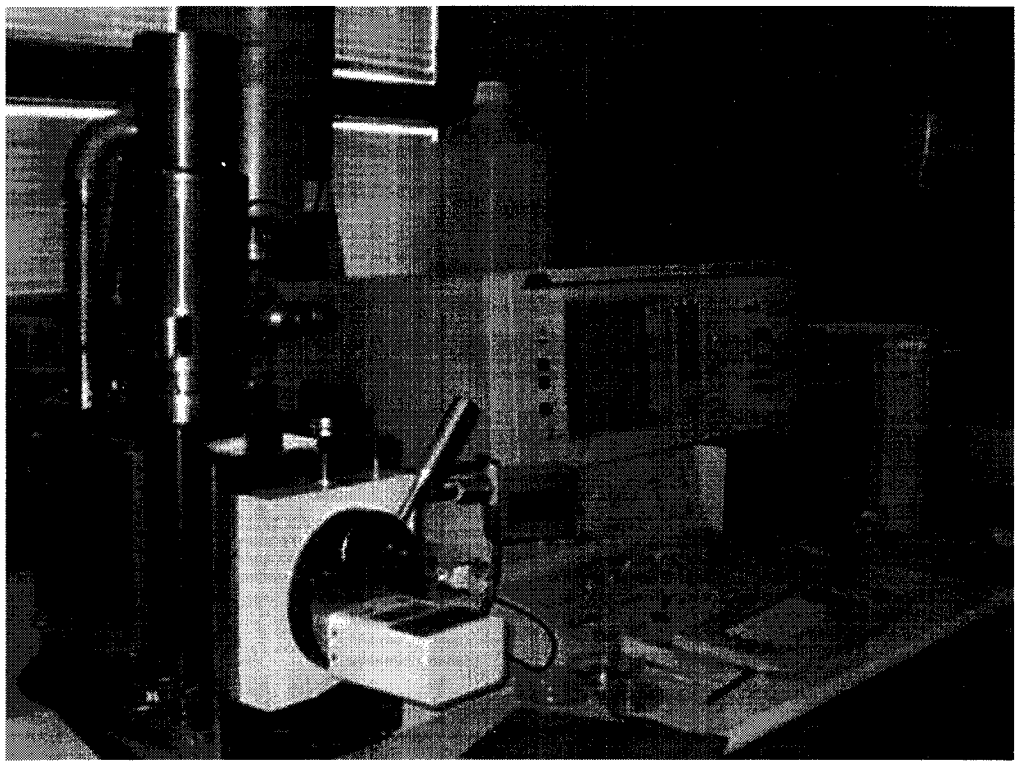


Figure 3.7: Electron beam (e-beam) writing system at EDM Lab. The system includes a JEOL 6100 SEM and a computer controlled nanometer pattern generation system (NPGS) (right hand side of the picture).

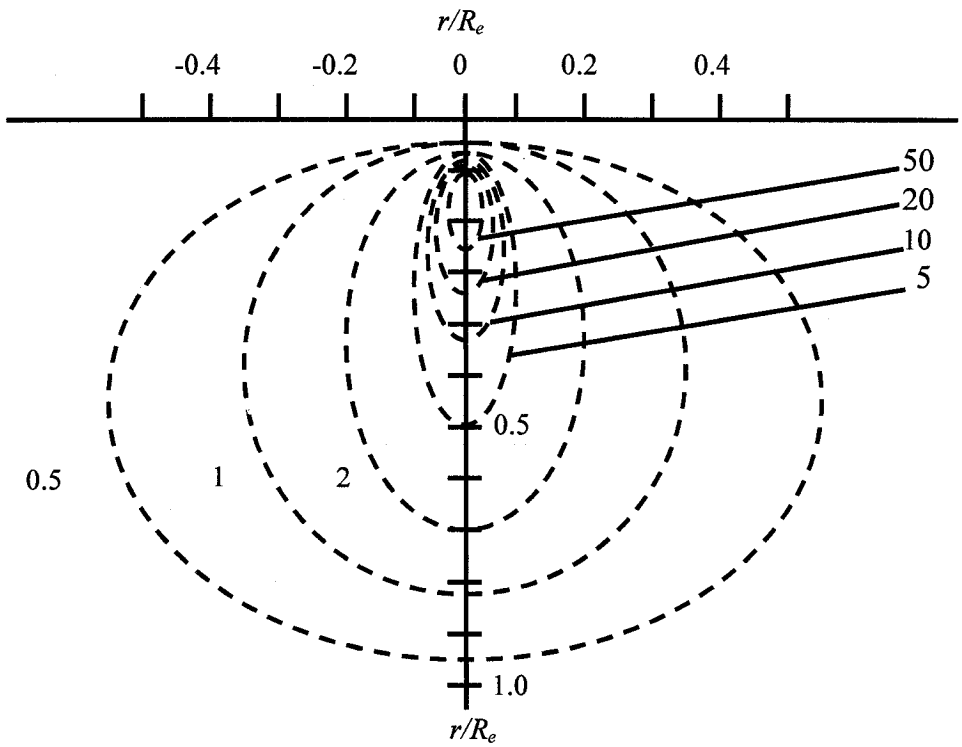


Figure 3.8: A contour plot based on Cohn and Caledonia s' results showing the ionization rate of a gaseous material by a focus electron beam. The distance scales are normalized to the electron range R_e. [3.22]

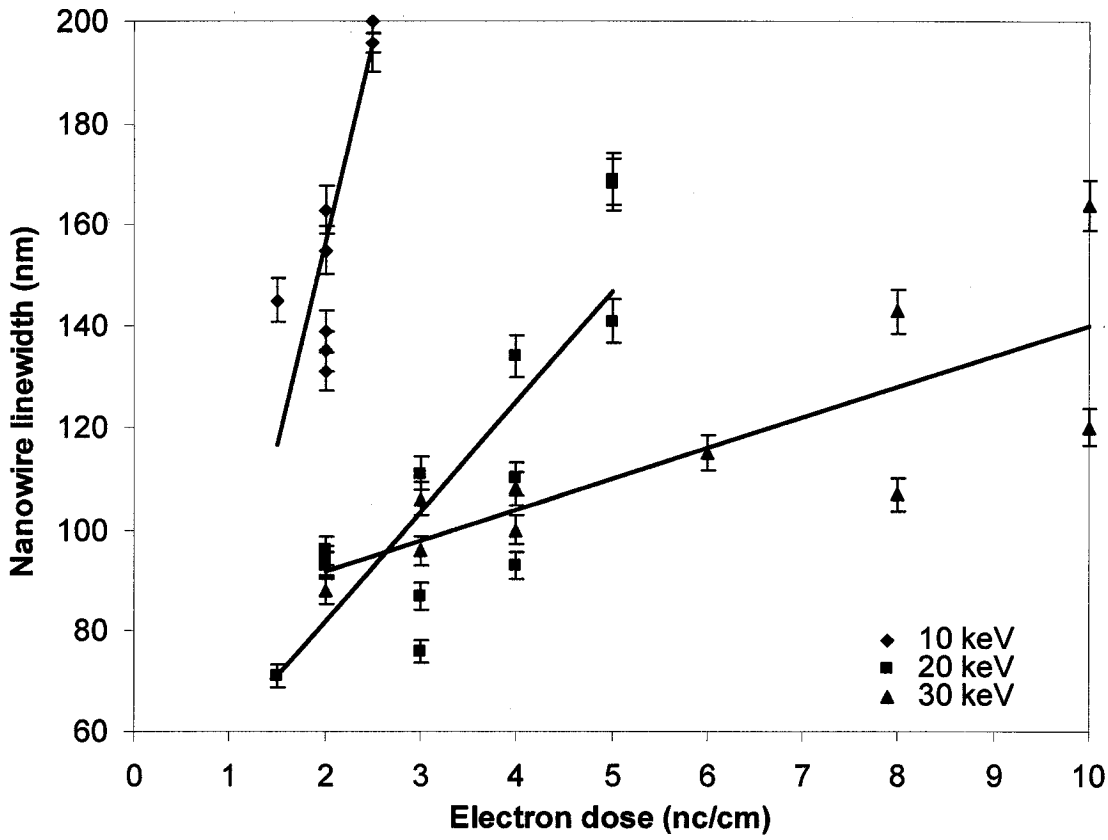
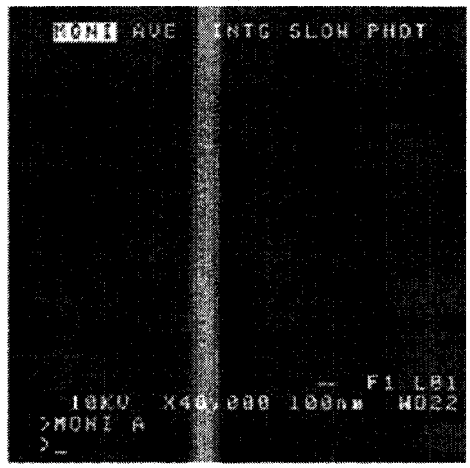


Figure 3.9: Variation of the experimental nanowire linewidth with the electron dose at different electron beam energies. Measurement data were taken from samples S8, S9, S11, S12, S14, S15 and S16. Data showed with 3% measurement error due to thickness measurement.

(a)



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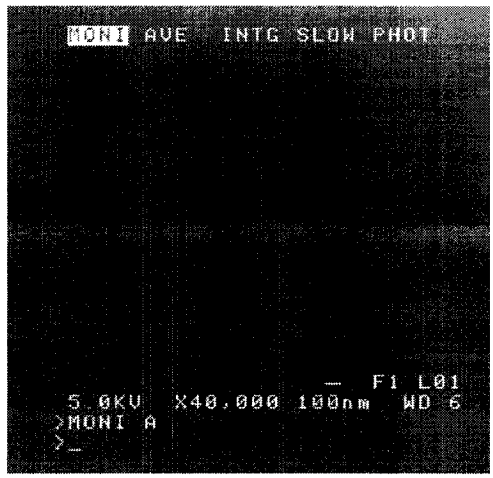


(c)

Figure 3.10: Photographs of the fabricated Bi nanowires with linewidth of a) 200 (S27-A2); b) 100 (S30-B3); and c) 71 nm (S38-B2).

Bi nanowire fabrication process details

The fabrication processes of the Bi nanowires were optimized after several runs of fabrication. In an effort to bridge the nanowire to the bonding pads, triangular-shape extensions were added at the ends of nanowire (Figure 3.11a) by electron beam writing. Therefore, the actual e-beam writing pattern consisted of one 20 μm-long line and two triangular extensions at the ends of the line with a dimension of 50 μm-base and 50 μm-height. In order to obtain a low nanowire to bonding pad contact resistance, a large portion of the triangular extensions were allowed to overlap with the prefabricated Bi bonding pads (Figure 3.11b). Since the overlapped area was much larger than the Bi nanowire, the contact resistance between the extensions and the bonding pad can be neglected. The measured parasitic resistance of the whole structure was less then 10 ohm while the nanowire resistance was in the order of kilo ohm. Hence the measurement error due to the contact resistance is less than 1%. A total of 46 batches of Bi nanowire samples were fabricated in the present study. Each sample contained 9 nanowire devices. A fabrication log and remarks are shown in Table 3.3. Every device was registered using its corresponding sample number and device position. For example device in sample 10, positioned in first row (letter) and second column (number) was registered as S10-A2. This naming method was used throughout the thesis. Yield of the fabrication was around 80% after the process conditions have been optimized. The final fabrication process details are shown in the subsequence paragraph and the corresponding steps are illustrated graphically in Figure 3.12.

Bi nanowires fabrication process:

a) Wet oxidize n-type Si wafer [111] at 1150 °C with oxygen flow of 1.5 cubic feet per hour for 3 hours.

b) Evaporate 30 mg of Bi powder (film thickness ~ 100 nm) and define 1 x 1 mm^2 square bonding pads using standard lithography process.

c) Spin coat 2% 400 kMW PMMA in chlorobenzene on Si substrates at 2500 rpm for 45 sec.

d) Bake samples in oven at 170°C for 30 minutes.

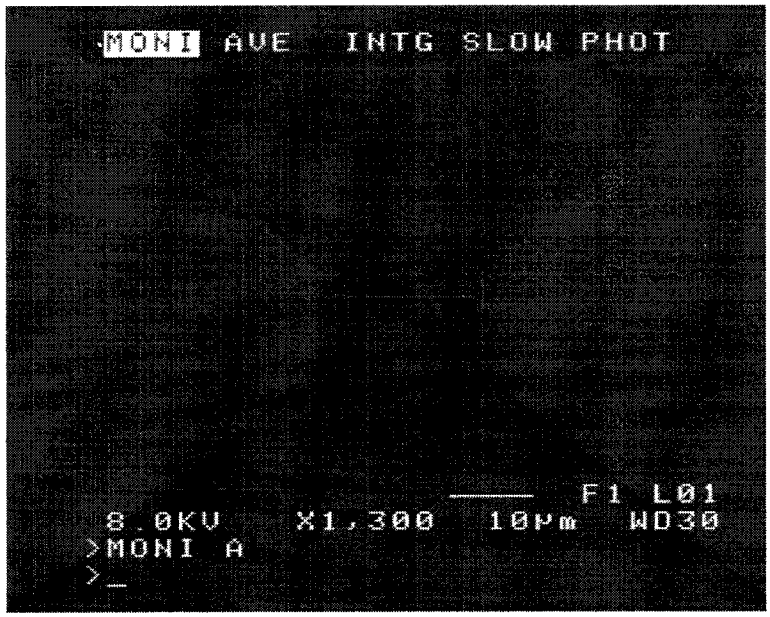
e) Perform electron beam writing with electron beam energy of 20 keV and electron dose of 2 nC/cm.

f) Develop samples in Methyl Isobutyl Ketone (MIBK): 2 Propanol (IPA) at a ratio of 1 to 3 for one minute.

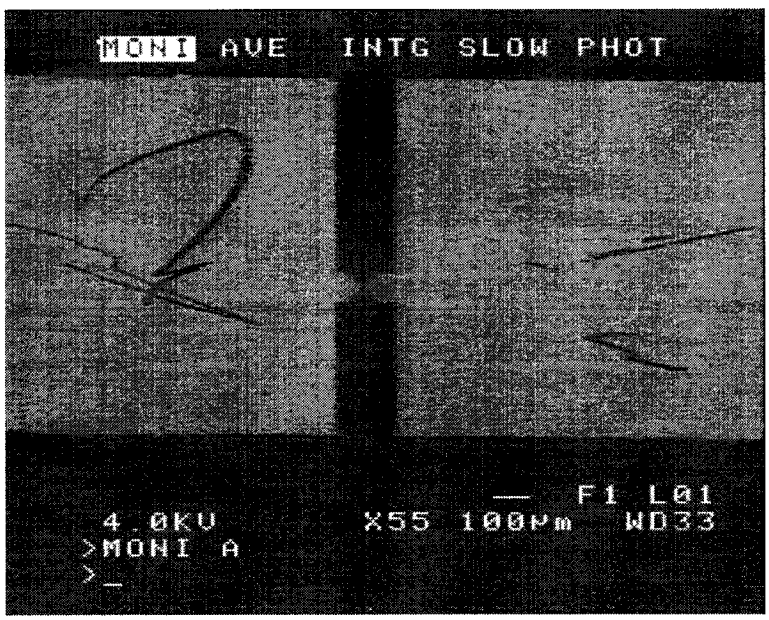
g) Clean samples using de-ionized water.

h) Evaporate 5.0 mg Bi powder on the sample (thickness ~ 50 nm).

i) Perform lift-off process in acetone solution (Immerse the solution in ultra sonic bath if necessary)



(a)



(b)

Figure 3.11: a) A Bi nanowire with triangular extensions (S34-C2); b) A Bi nanowire with triangular extensions connected to bonding pads (S34-C2).

Table 3.3: Bi nanowire samples log.

Sample number	Remarks
S1	PMMA evaluation.
S2	PMMA evaluation.
S3	Electron beam writing evaluation.
S4	Electron beam writing evaluation.
S5	Nanowire design.
S6	Nanowire design.
S7	Nanowire design.
S8	Electron beam energy evaluation.
S9	Electron beam energy evaluation.
S10	Process failed.
S11	Dose evaluation.
S12	Dose evaluation.
S13	Process failed.
S14	Electron beam energy evaluation.
S15	Dose evaluation.
S16	Dose evaluation.
S17	Nanowire fabrication. (trial)
S18	Nanowire fabrication. (trial)
S19	Nanowire fabrication. (process evaluation)
S20	Nanowire fabrication. (process evaluation)
S21	Nanowire fabrication. (process evaluation)
S22	Nanowire fabrication. (process optimization)
S23	Thin nanowire fabrication.
S24	Thin nanowire fabrication.
S25	Thin nanowire fabrication.
S26	Thick nanowire fabrication. (For comparison)
S27	Fabrication successful. Current-voltage measurement.
S28	Fabrication successful.

S29	Process failed.
S30	Fabrication successful. Current-voltage measurement.
S31	Fabrication successful.
S32	Fabrication successful. Current-voltage measurement.
S33	Fabrication successful. Current-voltage measurement.
S34	Fabrication successful with 76 nm linewidth. Current-voltage measurement.
S35	Fabrication successful. Current-voltage measurement.
S36	Fabrication successful with 83 nm linewidth. Current-voltage measurement.
S37	Fabrication successful. Current-voltage measurement.
S38	Fabrication successful with 71 nm linewidth. Current-voltage measurement.
S39	Fabrication successful.
S40	Process failed.
S41	Fabrication successful. Current-voltage measurement.
S42	Fabrication successful. Current-voltage measurement.
S43	Fabrication successful with 75 nm linewidth. Current-voltage measurement.
S44	Fabrication successful.
S45	Fabrication successful. Current-voltage measurement.
S46	Fabrication successful. Current-voltage measurement.

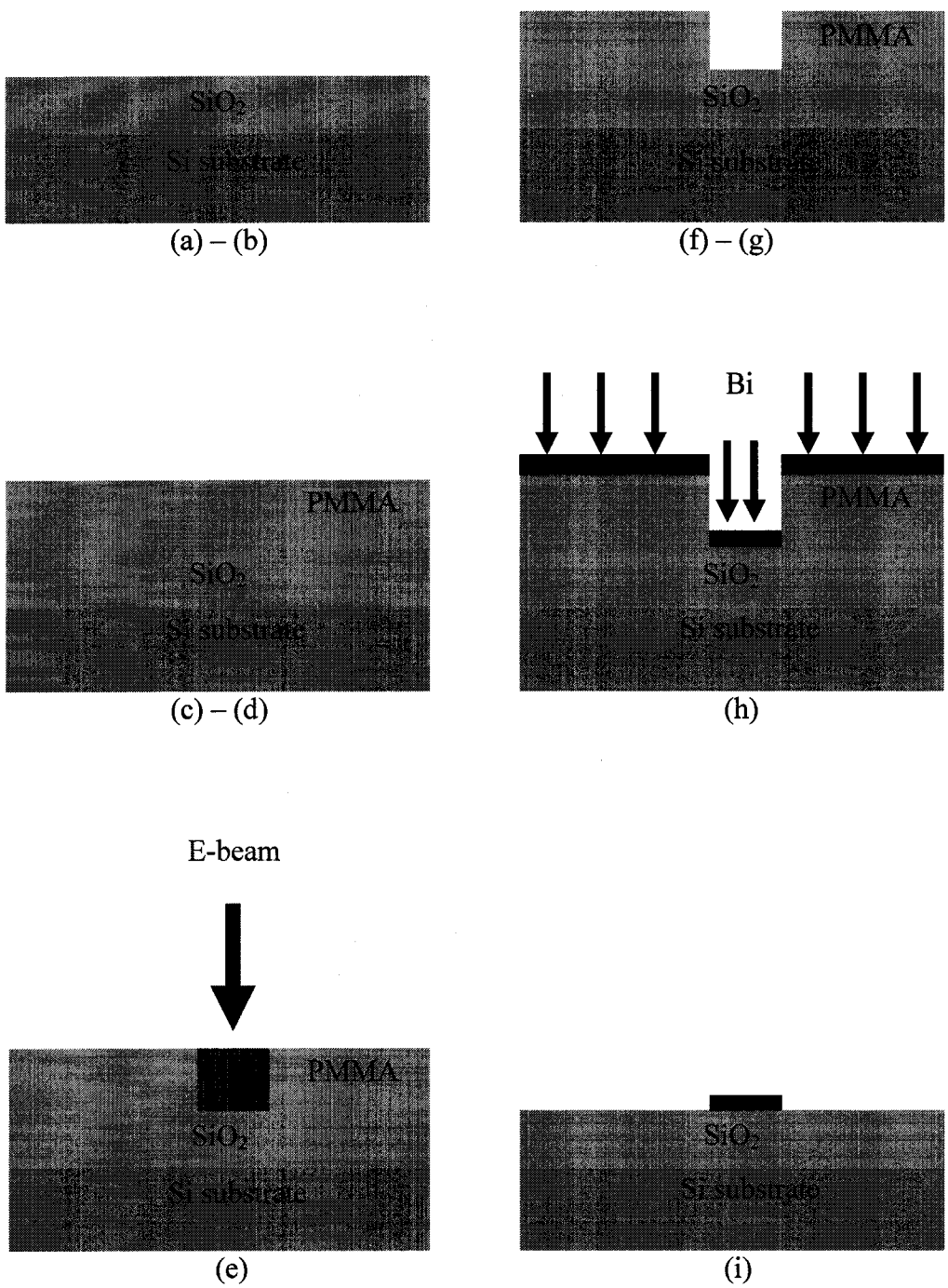
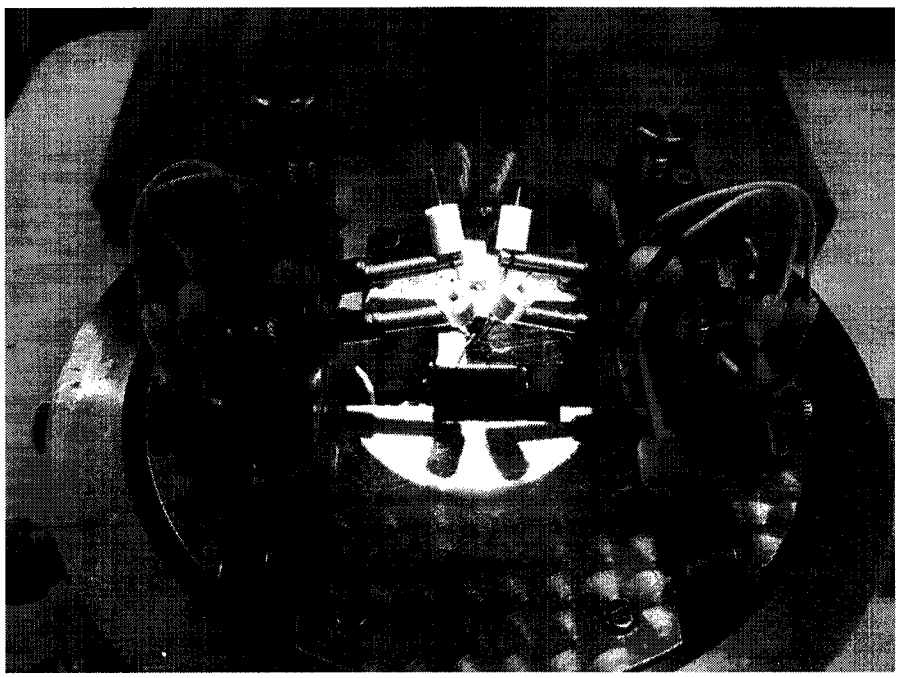


Figure 3.12: Bi nanowires fabrication steps corresponding to the process details.

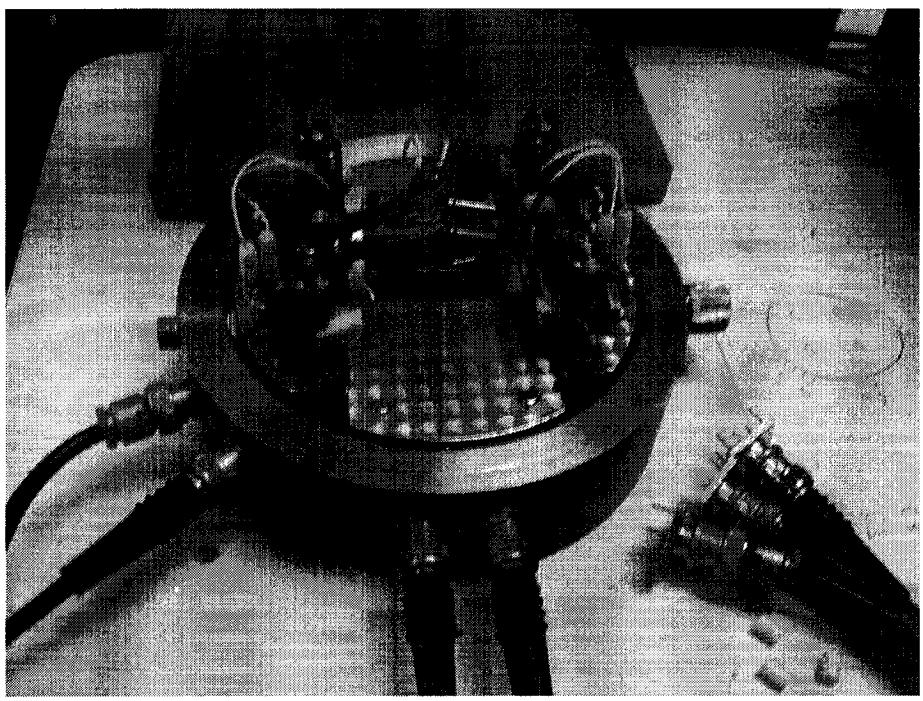
3.3 Bi nanowires characterizations

After the successful fabrication of Bi nanowires, all of the fabricated devices were examined using SEM and optical microscope. Defect free devices were selected for individual characterization. Current-voltage characterization was performed on the selected Bi nanowires. Two types of characterizations were performed, nanowire resistance as a function of temperature and nanowire resistivity as a function of linewidth. Individual characterization was performed in the vacuum/sample chamber of a cryostat (Polaron S4660 shown in Figure 3.13). The chamber pressure was brought down to approximately 10^{-2} torr during measurements to avoid the oxidation of bismuth. The cryostat also served as a temperature controller utilizing liquid nitrogen. Liquid nitrogen was pumped from a container to the base of the measurement chamber to chill the sample while a small heating element located beneath the sample was used to heat up the stage. The amount of liquid nitrogen flow and the temperature of the heating element were controlled by the cryostat. It has the ability to control the sample temperatures precisely ranged from 77 K to 350 K with 0.5 K resolutions. An HP 4145A semiconductor parameter analyzer was used for performing the current-voltage measurements. The parameter analyzer has a measurable current resolution of pA and a voltage resolution of mV. Special precautions were taken to minimize the noise of the system since low level measurement was expected. The parameter analyzer was connected to the sample stage of the cryostat via shielded coaxial cables to avoid ambient noises. The outer shield of the cryostat was connected to a common ground in order to keep the measurement noise to a minimum level. The liquid nitrogen pump was shut down temporarily during the measurement since the rotary motor created electro-magnetic noise when in operate

mode. The leakage/noise current of the whole measurement setup was measured. The measurement value was less than the resolution limit (pA) of the parameter analyzer. It is thus believed that the setup had a noise resolution less than the measurement limit (less than pA). Four-point probe measurements could not be performed due to the system configuration. However, the parasitic resistance of the system has been measured (~10 ohm) and was insignificant compared to the nanowire resistance value (~10 kOhm). Combining the parasitic resistance, noise fluctuation and equipment limitation, the measurement error of the system should be approximately 3% of the measured data. The estimated measurement error also applied to subsequent measurement data in chapters 4 and 5.



(a)



(b)

Figure 3.13: Cryostat sample chamber (cover not shown). (a) Sample on the stage; (b) Coaxial cables connected to sample chamber.

Resistance vs. Temperature (Metal-to-semiconductor transition)

Resistance values of individual Bi nanowire with different linewidths as a function of temperature were obtained. Measurement results for the 75, 145, 163 and 200 nm-wide nanowires are shown in Figure 3.14. The data values were normalized to the resistance at 300 K and denoted by R(T)/R(T=300 K). The flatten normalized resistance at temperatures below 150 K of all the measured samples had a profile similar to the polycrystalline Bi nanowires results obtained by Lin et al [1.20] shown in Figure 3.14 inset. By comparing the similar profile of the measurement, it is deduced that the crystal structure of fabricated Bi nanowires were in the polycrystalline regime. It is also supported by the fact that thermally evaporated metal thin films are typically polycrystalline due to the rapid condensation of metallic vapor on samples. The measurement results revealed that the resistance of all nanowires rose as temperature decease. This is exactly opposite to the metallic conduction behavior in bulk Bi (also shown in Figure 3.14) where phonon scattering is dominant in this temperature range. The increase of resistance in the nanowire at low temperatures was due to the reduction of free carriers in the conduction band. Under this situation, only the carriers with enough energy could stay in the conduction band for electrical conduction. The rapid drop of carrier density at low temperatures suggested that the overlap of conduction band and valance band has been diminished. Since the two energy bands were no longer overlapped, thermal energy (temperature) was the only factor to determine the free carrier density (refer to the metal-to-semiconductor transition section in chapter 3.1). This transport behavior indicated that the carrier transport in Bi nanowires with rectangular cross-section was carrier dominated and they exhibited semiconductor conduction

behavior. The measurement results confirmed that the fabricated Bi nanowires have undergone the metal-to-semiconductor transition and bandgaps were created due to the quantum confinement. These results agreed with the quantum confinement-induced bandgap model (Eq. 8) shown in Figure 3.2 where it indicated that the energy bands overlap diminished at a critical dimension of 50 nm. The temperature-dependent resistance of Bi nanowires was also size dependent. The size effect of Bi nanowire is studied in details in the next section.

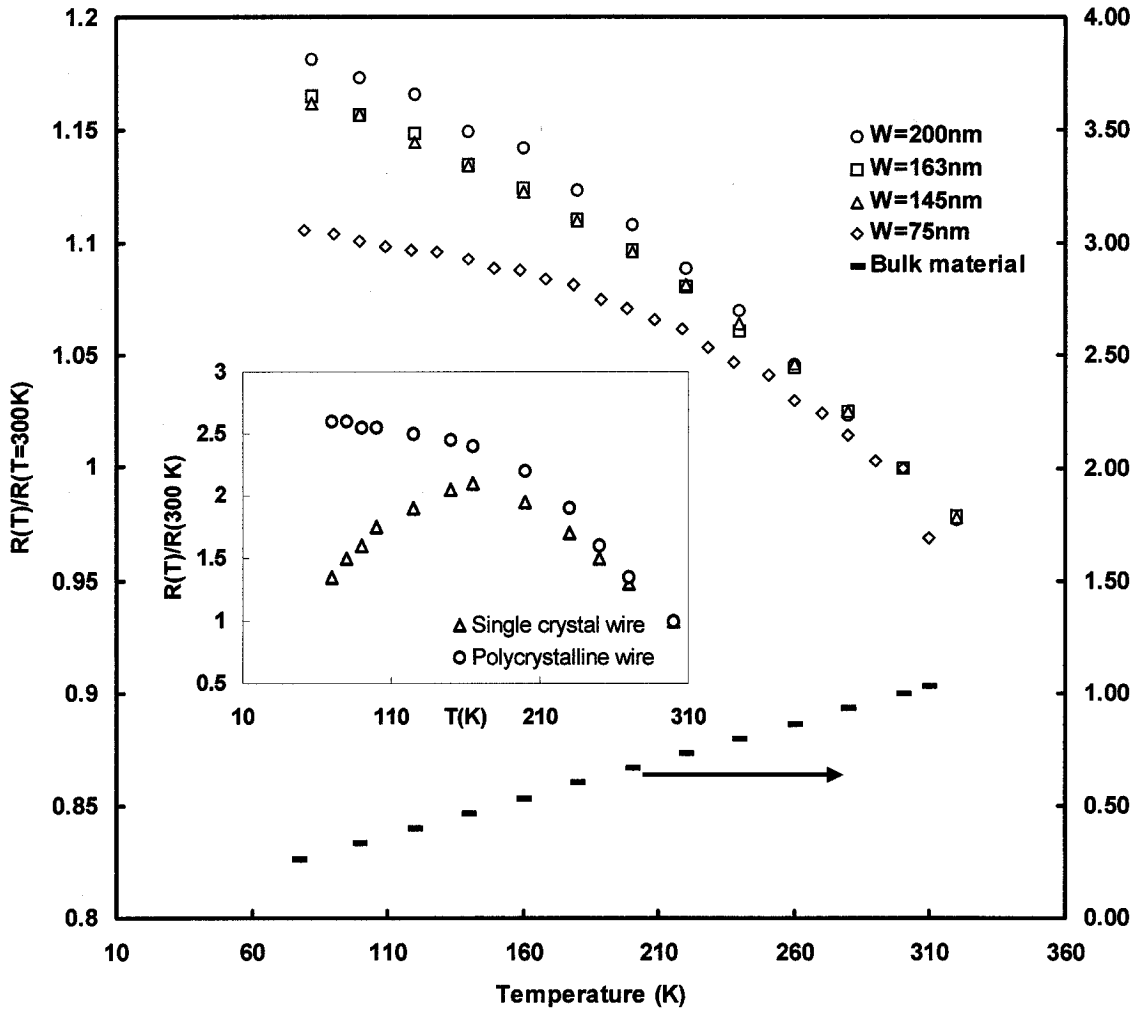


Figure 3.14: Temperature dependence of Bi nanowire resistance R(T)/R(T=300K) with cross-sectional dimensions of 50 nm by 200, 163, 145 and 75 nm (thickness by linewidth). Measurement data were taken from devices S41-C2, S43-A2, S43-B2 and S46-B1. Measurement error of the raw resistance data is 3%. (Inset: Temperature dependence resistance for 70-nm diameter single-crystalline and polycrystalline Bi nanowire by Lin et al. [1.20]).

Resistivity vs. Linewidth (Size effect)

Resistivities of the Bi nanowires were computed based on the measurement data using Equation 9:

$$\rho = \frac{AR}{L} \qquad \text{(Eq. 9)}$$

where L is the length, A is the cross-sectional area and R is the measured resistance value. The computed values for Bi nanowires with different cross-sectional dimensions are shown in Figure 3.15. Resistivity of 75, 145 and 200 nm-wide nanowire was 4.05×10^{-3}, 2.87×10^{-3} and 2.30×10^{-3} Ω-cm at 300 K. All nanowire resistivities were higher than the resistivity of bulk Bi, 1.2×10^{-4} Ω-cm. The corresponding Bi nanowire mobility at 77 K was ranged from 3048 to 5715 $cm^2/V\text{-}s$ at 77 K (Table 3.4). From Figure 3.15 and Table 3.4, it is clear that the Bi nanowire with small cross-section has a larger resistivity (lower mobility) than the one with large cross-section. The increase of resistivity can be explained by the size effect (refer to the size effect section in section 3.1). Given that the cross-section of the nanowire was less than the carrier mean free path, a further reduction in the cross-section of the nanowire resulted in an increase of wire scattering (both grain boundary scattering and surface scattering). The enhanced carrier scattering reduced the mobility of the nanowire and thus lead to the increase in the resistivity. It is obvious that this size dependent resistivity occurred in nanowires with critical dimensions in the order of carrier mean free path. In order to determine the carrier scattering mechanism of the fabricated nanowires, measurement data was compared to established mathematic size effect models, MS model [3.7] and Dingle model [3.6]. Figure 3.16 displays the nanowire resistance per unit length against linewidth as well as different computation

models for nanowire resistance with the consideration of grain boundary scattering mechanism (MS model: Eq. 5 and Eq. 6) and surface scattering mechanism (Dingle model: Eq. 3 and Eq. 4). MS model considered electron scattering at the grain boundaries of the nanowires while Dingle model considered the scattering of electron at the wire surface. In both models, the intrinsic resistivity, ρ_0, was assumed to be 1.79×10^{-3} Ω-cm which was the evaporated Bi thin film resistivity measured by a four-point probe system. A combined model was also constructed by adding the two scattering mechanisms together. Figure 3.16 shows that both elastic and inelastic Dingle models (surface boundary model) have under-estimated the resistance of the nanowire with linewidth below 150 nm. This is the region where the linewidth is equal to or less than the mean free path. As a result, carrier scattering at grain boundary has to be included. The grain boundary scattering model (MS model) matched closely with the experimental results while the combined MS + Dingle model over-estimated the nanowire resistance. MS model (Eq. 5 and 6) with matched experimental data parameters are shown in Table 3.5. From the Table, one can see that the reflection coefficient is 0.5 representing a 50% probability of an electron being scattered at a grain boundary. The average grain boundary value used in the model is equal to the linewidth of the nanowire showing that the grain size is limited by the linewidth itself. A hypothetical nanowire with grain size indication for the MS model is shown in Figure 3.17. The Figure showed that the grain size is limited by the linewidth and the nanowire is connected by one grain to another. For an electron attempts to travel along the nanowire, it will have to cross the grain boundaries and will have 50% chance of being scattered at each boundary. All these results led to a conclusion that the scattering mechanism in the rectangular cross-section

nanowires fabricated by electron beam writing system was mainly grain boundary scattering. The domination of grain boundary scattering in Bi nanowire resulted in a higher than bulk material resistivity.

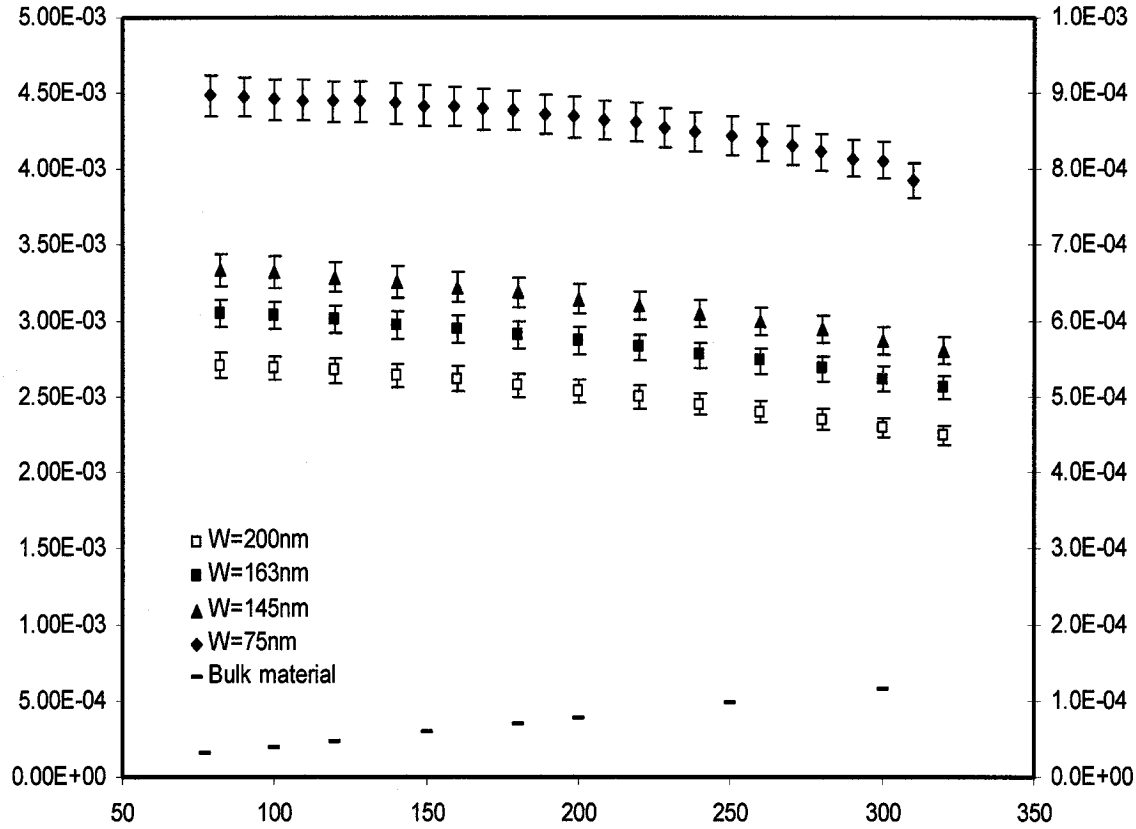


Figure 3.15: Temperature dependence of Bi nanowire resistivity with cross-sectional dimensions of 50 nm by 200, 163, 145 and 75 nm (thickness by linewidth). Measurement data were taken from devices S41-C2, S43-A2, S43-B2 and S46-B1. Measurement error is 3%.

Table 3.4: Fabricated Bi nanowire mobility at 77K.

Nanowire linewidth (nm)	**Mobility (cm^2/V-s) (Measurement Error)**
200	5715 ± 172
163	4572 ± 137
145	4156 ± 125
75	3048 ± 91
50-nm thick thin film	7663 ± 230
Bulk	45915 (Eq. 2)

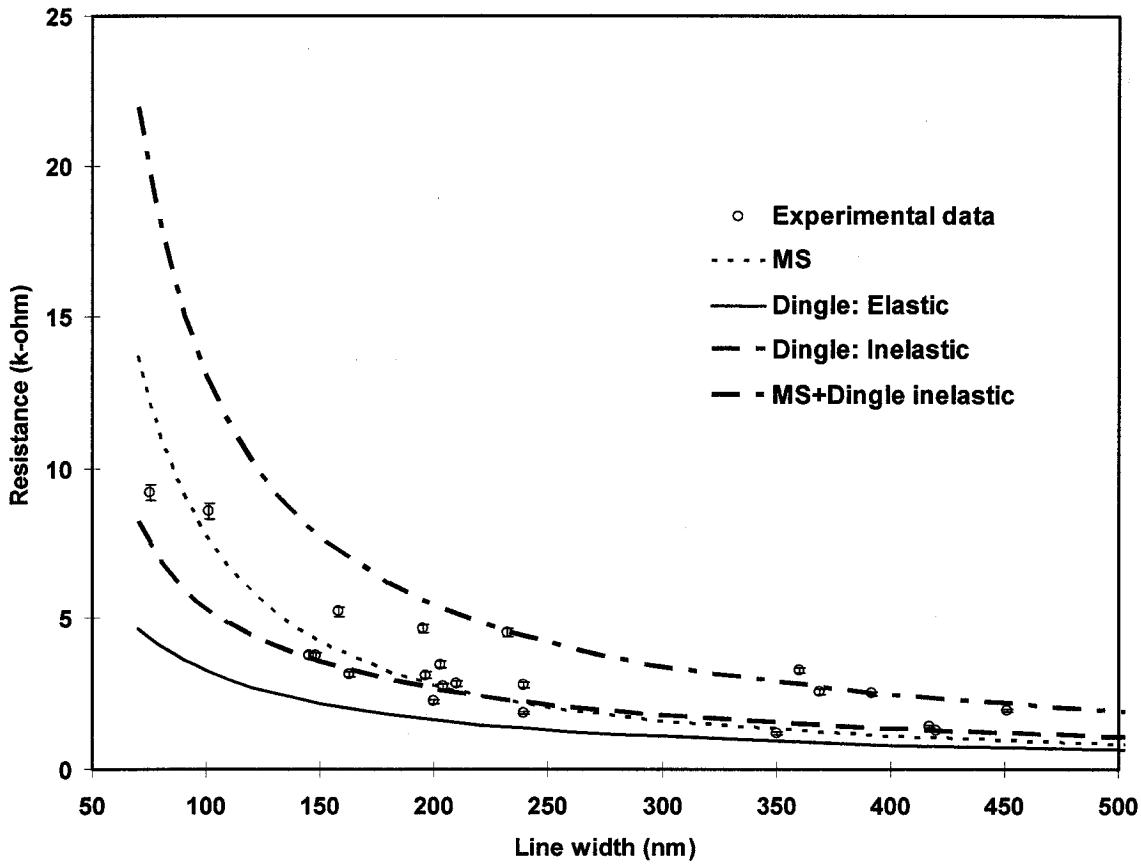


Figure 3.16: Measured resistance per unit length of Bi nanowires at room temperature (circular dots) compared with wire boundary scattering model (Dingle model), grain boundary scattering model (MS model) and combined model (Dingle + MS model). Measurement data were taken from samples S27, S30, S34, S38, S43 and S46. Data showed with 3% measurement error.

Table 3.5: MS model parameters (Eq. 5 and 6).

MS model parameter	**Parameter value**
Mean free path, l	100 nm
Average grain diameter, d	= linewidth
Reflection coefficient, R	0.5

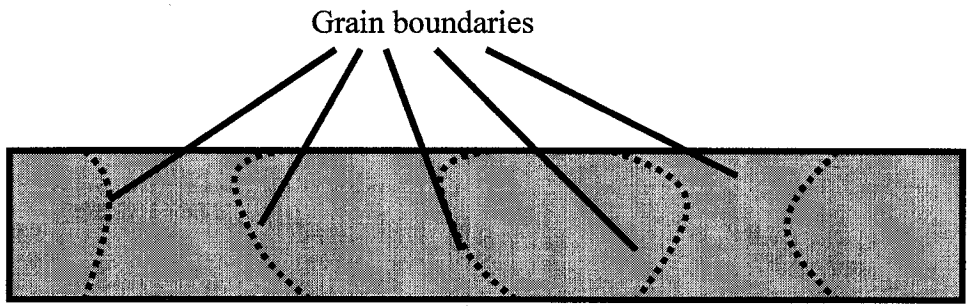


Figure 3.17: A hypothetical nanowire with grain size indication for the MS model with matched experimental data parameters. The grain size is limited by the linewidth and the nanowire is connected by one grain to another.

3.4 Chapter summary

In the phase I of the thesis work, Bi nanowires with rectangular cross-sections have been successfully fabricated using a combination of e-beam writing and thermal evaporation techniques. The fabricated Bi nanowires had dimensions of 50 nm by 70 to 200 nm (thickness by linewidth). Thermal evaporation technique was used to control the film thickness while e-beam writing was utilized to define the linewidths. The established nanowires fabrication process has the ability to position nanowires precisely at the desired spot and therefore provided an easy approach for individual device characterization. In the actual work, nanowire was placed across two Bi bonding pads to facilitate individual device current-voltage measurement. In the study of carrier transport, two nano scale phenomena were observed; they were metal-to-semiconductor transition and size effect. It was found that all fabricated Bi nanowires exhibited a semiconductor conduction behavior where the resistance rose with decreased temperature. The change from metallic to semiconductor conduction behavior was due to the creation of bandgap as the nanowire reached the critical dimension of 50 nm. The measurement results were supported by the quantum confinement-induced bandgap model (Eq. 8). It also revealed that the carrier transport mechanism in the fabricated Bi nanowire was carrier dominated. This carrier domination of transport is another evidence of the diminishment of the overlap of energy bands. In addition, resistivity versus linewidth measurement was performed. Measured resistivity increased significantly as linewidth is reduced. The results indicated that size effect took place in the fabricated devices. The smaller than mean free path nanowire cross-section confined the movement of carriers in one direction along the wire axis. The confinement of carriers led to an increase of scattering. In order

to determine the scattering mechanism, size effect models, MS model and Dingle model, were established to compare with the measurement data. MS model matched closely with the experimental data. From the computational models, it is suggested that the scattering mechanism in the rectangular cross-section nanowires was mainly grain boundary scattering and carrier has a 50% chance of being scattered at each grain boundary. It also indicated that the grain size in the nanowire is limited by the linewidth and the fabricated nanowire is consisted of a series of inter-connected grains. The MS models also reconfirmed the poly-grains (polycrystalline) nature of the fabricated Bi nanowires.

Most of the previous works on Bi nanowires were in bundle measurement format. Although individual device characterization had been reported, it is believed that the present work is the first complete carrier transport mechanism study on individual Bi nanowire fabricated using the presented method. The results on the metal-to-semiconductor transition and the size effect of Bi nanowires were presented in both conference presentations and technical journal format. Part of the results was presented at the American Physics Society March meeting 2004 at Palais des Congres de Montreal, Montreal, Quebec. A technical paper based on the research results was published in the November issue of Nanotechnology Journal in 2004 [3.24].

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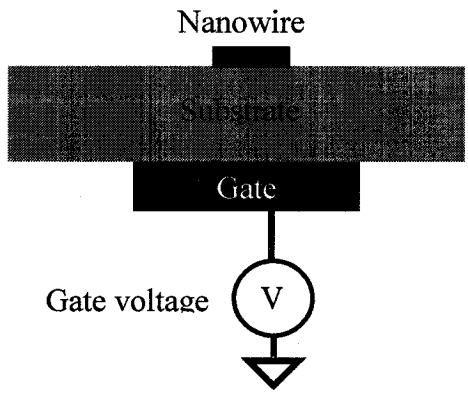
Chapter 4: Bi nanowires with dual side-gate structures

The carrier transport and scattering mechanisms of Bi nanowires have been studied in details in the first phase of the thesis. Individual Bi nanowire under no external influence proofed to have semiconductor conduction behavior. Its resistivity is size and temperature dependent. In the second phase of the thesis, we moved one step forward to study the change of Bi nanowire conductance under the influence of an external voltage. Dual side-gate structures were formed close to the middle section of the nanowires. Devices were fabricated using a modified Bi nanowire fabrication process. The gate-to-nanowire spacing was approximately 100 nm. Using this structure, potential applied to the gates can be coupled to the nanowires effectively. Bi nanowires conductance changed as the potential coupled into the devices. In order to study the effectiveness of the dual side-gate structure, numerical simulations on the potential distribution of the device structures were conducted. The measurement and simulation results as well as the fabrication process are discussed in details in the following sections.

4.1 Nanowires with gate structures

Nanowires with gate structures are often referred to nanowire transistors. Typical nanowire transistors are made of semiconductor materials such as Si [4.1, 4.2], Ge [4.3], GaAs [4.4] and GaN [4.5]. The nanowire transistors can be doped or kept intrinsic. Gate structures are formed close to the nanowire in order to couple potential into the devices. There are many types of gate structures, which can be very simple and easy to make or require complicated fabrication steps. A simple gate structure can be a back gate structure [4.3, 4.5] where gate potential is applied from the back side of the sample (Figure 4.1a). This is the simplest form of gate structure, however the coupling effect of this structure is very inefficient. A significant amount of applied potential is distributed within the substrate instead of inside the nanowire. Since the loss of potential in the substrate is large, usually a very large gate bias is required to compensate for the loss in the back gate structure device. A more robust form of gate structure is the top gate structure (Figure 4.1b) [4.3]. In top gate structure devices, a dielectric material is deposited on top of the nanowire and a gate electrode is formed above it. This gate structure is an effective way to couple potential into the nanowire. But the extra steps of depositing a dielectric material and the lithography process may degrade the nanowire device through the heating and chemical immersion processes. The top gate structure is commonly used in mature devices or devices requiring very efficient gate coupling. Another popular gate structure is the side gate structure (Figure 4.1c) [4.1, 4.2]. It is a relatively simple to fabricate structure, yet provides a reasonable efficiency to couple the gate potential. In this structure, the gate electrode is formed on the same substrate as the nanowire. It is placed very close to the nanowire so that the potential can be coupled into

the nanowire horizontally. In order to increase the coupling effect, side gates can be formed on both sides of the nanowire. This simple and effective gate structure is very suitable for researching novel devices where extra effort on gate structure is not desired. In any type of gate structures, potential applied to the gate can be coupled into the nanowires. This externally applied potential changes the transport characteristic of the nanowires. The changes can be either increase or decrease of conductance. This change of conductance sparked the motivation of making nanowire transistors logic. Nanowire transistors logic has an advantage of simple structure and high device density. However, the high gate bias and the incapability to fully turn off the device are the major obstacles for forming nanowire transistors logic. As a result, nanowire transistors remained mostly a pure academic research topic. In this work, a side gate structure was selected to form Bi nanowire transistors. This simple and efficient structure provided an effective way to study the topic.



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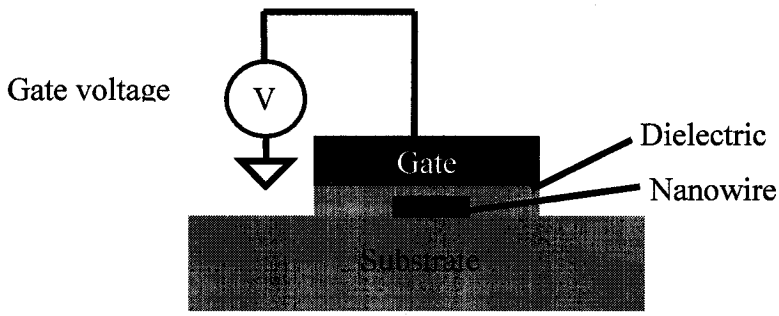

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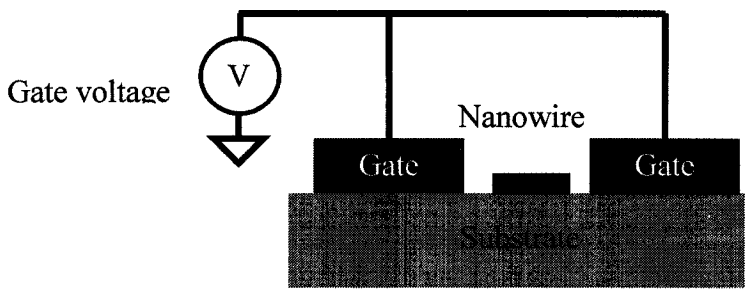


(c)

Figure 4.1: Different gate structures for nanowire transistors. (a) Back gate structure; (b) Top gate structure; (c) Side gate structure (Dual side gates shown)

4.2 Bi nanowires with dual-side gate structures fabrication

Dual side-gate structures

Bi nanowires with dual-side gate structures were fabricated using a modified Bi nanowires fabrication process (refer to Section 3.2). The fabrication hardware and the process procedures remained the same. Devices were fabricated using a combination of e-beam writing and thermal evaporation techniques. NPGS [3.21] was used to control the e-beam writing process. But the patterns and the e-beam writing conditions were revised and optimized for the creation of side-gate structures. The structures were designed using computer aided design (CAD) software. The actual CAD pattern is shown in Figure 4.2. The targeted gate-to-nanowire spacing was 100 nm. However, because of proximately effect (refer to Figure 3.8), the designed gate-to-nanowire spacing pattern cannot be 100 nm, a larger spacing was required to compensate for the effect. In addition, the electron dose, 2 nC/cm, used in the nanowire fabrication process was in line-dose format and was suitable for writing line structures only. Different electron dose format was needed to form the large side-gate structure. Array of rectangular patterns were created to test the optimal electron dose for the gate structure. A test sample of the rectangular patterns with different electron area-doses is shown in Figure 4.3. After several trial fabrication runs and modification of design patterns, area-dose of 70 uC/cm^2 and gate-to-nanowire spacing of 300 nm were selected to form the side gate structures.

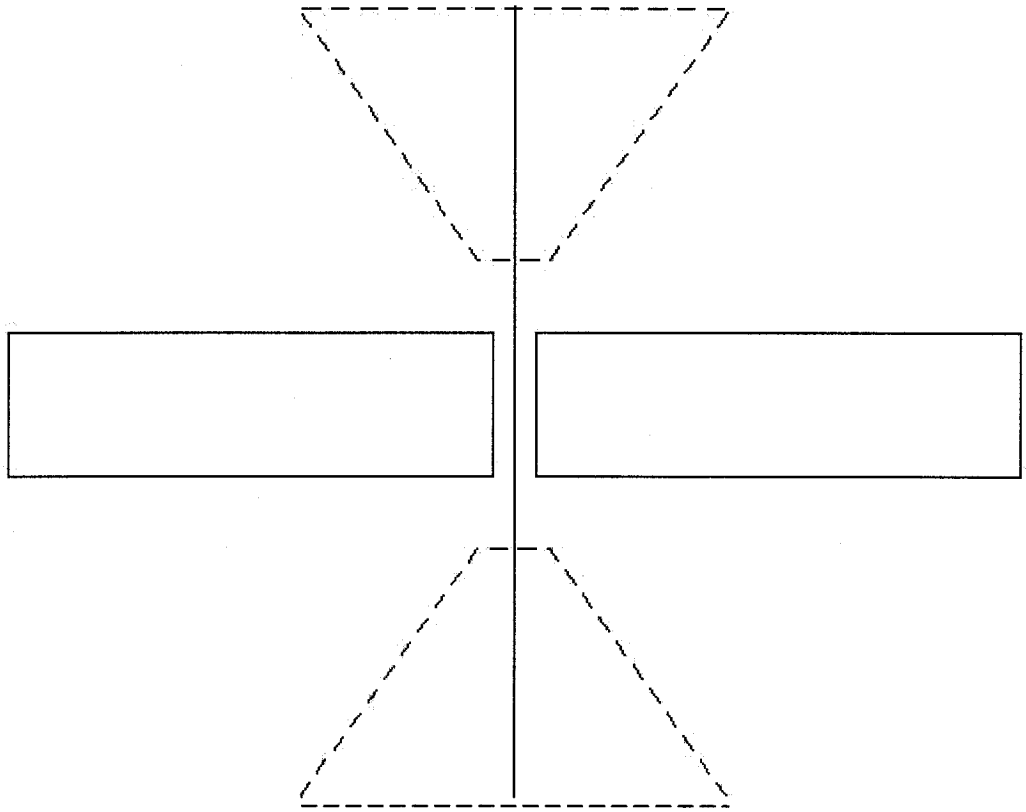


Figure 4.2: CAD pattern for nanowire with dual side-gate structures. The designed gate-to-nanowire spacing was 300 nm to compensate for the proximity effect.

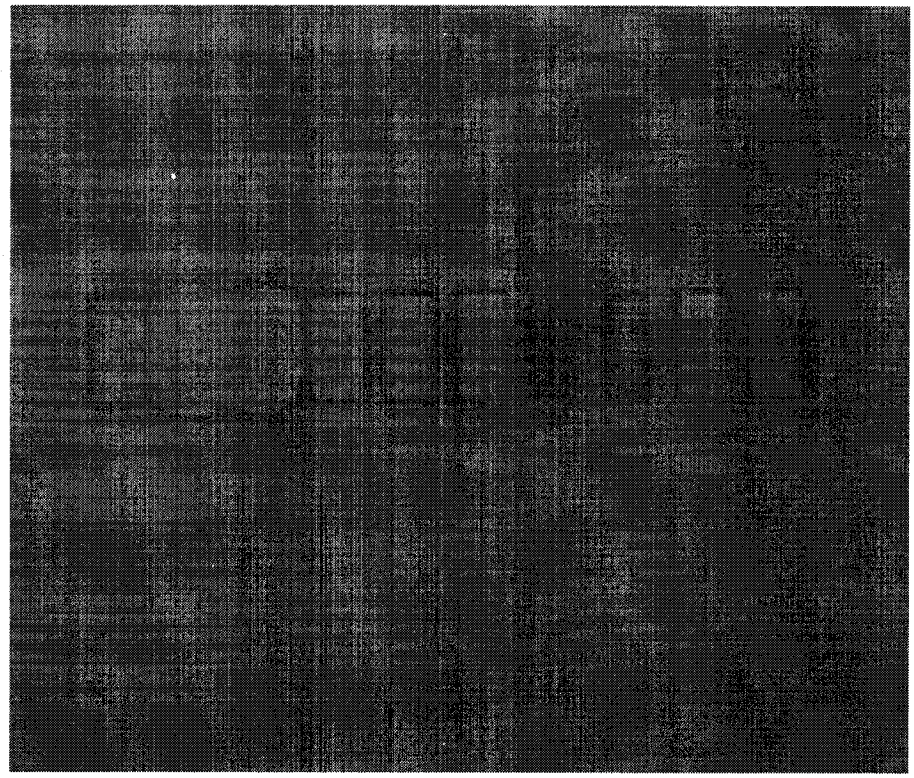


Figure 4.3: Array of rectangular patterns (sample S52) with electron area-dose of 70, 150, 100, 80, 70, 60, 20, 40, 60, and 80 $\mu C/cm^2$ (from left to right).

Bonding pad consideration

In the final fabrication process, the bonding pad material was changed from bismuth to gold (Au) and chromium (Cr). Cr was the seed layer and Au was the top contact layer. Both layers were deposited using thermal evaporation technique by Prof. Shih in the EDM Lab.. The change of the bonding pad material eased the testing process because the Bi bond pad was fragile and easy to damage after a few test probing. The damage of Bi bonding pad is visible in Figure 3.11b. Au and Cr bonding pad are widely used in device testing due to their stability and rigid structure. The use of different materials might introduce contact resistance between the devices and the bonding pads. After serious consideration and study of the possible effects on the accuracy of measurement, the drop of the Bi bonding pad was preferred. Firstly, considering that the objective of phase II was to study the change of conductance due to external potential (unlike in phase I where the study of device resistivity was the objective), a small increase of contact resistance should have no effect on the results (the total measured resistance might increase but the change of resistance due to external potential remained the same). Secondly, the work functions of Bi and Au (4.3 and 5.1 respectively [4.6]) are reasonable close. The contact between the two materials should form an ohmic contact and is suitable for the measurement. Based on the two points, the used of Au and Cr bonding pad was justified.

Bi nanowires with dual-side gate structures fabrication details

The fabricated device structure consisted of a nanowire with dimensions of 50 nm x 100 nm x 4 μm (thickness x width x length) and a 2 μm wide gate with a gate-to-nanowire spacing of 100 nm. A total of 26 batches of samples were fabricated and the fabrication log is shown in Table 4.1. Each sample had 9 devices. The yield of functional devices was approximately 15% in optimized processing conditions. SEM photographs of the fabricated device are shown in Figure 4.4. The fabrication details of the Bi nanowires with dual side-gate structures are shown below:

Bi nanowires with dual side-gate structures fabrication process:

a) Wet oxidize n-type Si wafer [111] at 1150 °C with oxygen flow of 1.5 cubic feet per hour for 3 hours.
b) Define 1 x 1 mm^2 square Au and Cr bonding pads using standard lithography process.
c) Spin coat 2% 400 kMW PMMA in chlorobenzene on Si substrates at 2500 rpm for 45 sec.
d) Bake samples in oven at 170°C for 30 minutes.
e) Perform electron beam writing with electron beam energy of 20 keV. The writing of nanowire uses electron line-dose of 2 nC/cm and the writing of gate structures use electron area-dose of 70 uC/cm^2.
f) Develop samples in Methyl Isobutyl Ketone (MIBK): 2 Propanol (IPA) at a ratio of 1 to 3 for one minute.
g) Clean samples using de-ionized water.

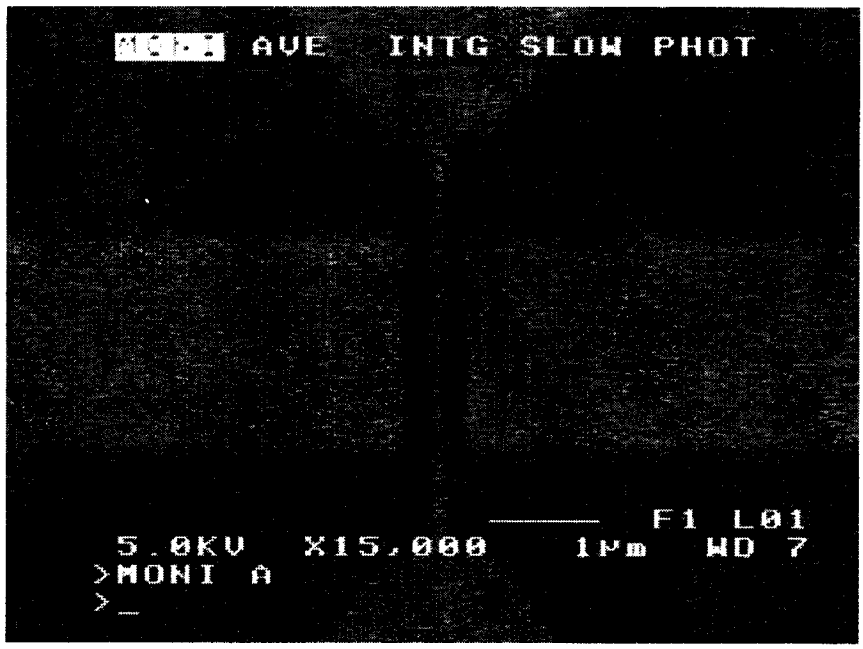
h) Evaporate 5.0 mg Bi powder on the sample (thickness ~ 50 nm).

i) Perform lift-off process in acetone solution (Immerse the solution in ultra sonic bath if necessary).

Table 4.1: Bi nanowires with dual side-gate structure samples log.

Sample number	Remark
S47	Structure design.
S48	Structure design.
S49	Structure design.
S50	Area dose evaluation.
S51	Structure design.
S52	Area dose evaluation.
S53	Structure design.
S54	Structure design.
S55	Area dose evaluation.
S56	Structure design.
S57	Area dose evaluation.
S58	Sample fabrication. (process evaluation)
S59	Sample fabrication. (process evaluation)
S60	Process failed
S61	Bonding pad evaluation.
S62	Bonding pad evaluation.
S63*	Sample fabrication. (process optimization)
S64*	Fabrication successful. Current-voltage measurement. Device failed after high current measurement.
S65*	Process failed
S66*	Fabrication successful.
S67*	Fabrication successful. Current-voltage measurement. Device failed after high current measurement.
S68*	Process failed
S69*	Fabrication successful. Current-voltage measurement.
S70*	Fabrication successful.
S71*	Fabrication successful. Current-voltage measurement.
S72*	Fabrication successful. Current-voltage measurement.

*Sample also contained trial fabrication of nanodot structures.



(a)

(b)

Figure 4.4: (a) A Bi nanowire with dual side-gate structure (S64-C2). The nanowire is 50 nm thick, 100 nm wide and 4 μm long; (b) An enlarged view of the dual side-gate structure. The side-gate is 2 μm wide and the gate-to-wire spacing is approximately 100 nm.

4.3 Bi nanowires with dual-side gate structures characterization

After the successful fabrication, devices were inspected visually using optical microscope and SEM. Devices with clean lift-off process had no visible metallic debris on the surface. Current-voltage measurements were performed on selected devices. The device measurement setup was the same as that described in Section 3.3. It consisted of an HP 4145A semiconductor parameter analyzer and a Polaron S4660 cryostat with vacuum chamber for measurements. All the precautions on noise reduction such as shielded cables and grounded chamber chassis were carefully performed. The measured resistivity of Bi nanowires (S69-B1) was approximately 3×10^{-3} Ω-cm which agreed with the higher than bulk resistivity value reported in previous chapter (Figure 3.15). By comparing the device resistivity (3×10^{-3} Ω-cm) to the reported values ($2.5 - 4.5 \times 10^{-3}$ Ω-cm) in Fig. 3.15, it is believed that the large resistivity value in the fabricated devices was also due to size effect (refer to Section 3.1). Current-voltage characteristics of a Bi nanowire with different gate voltages, V_g, applied to both side-gates at room temperature are plotted in Figure 4.5. The measurement results showed a small but consistence reduction of nanowire current with the increase of negative gate voltage. At a gate voltage of -10 mV, the nanowire current reduced 7% when biased at 20 mV. Further increase of the gate voltage resulted in unstable nanowire current. It is evident that the nanowire current was affected by the gate voltage through electrostatic potential coupling. The potential was coupled to the nanowire from the closely positioned side-gates, as a result the potential distribution within the nanowire was distorted. The distortion of potential led to a reduction of carrier flow and a decrease of current. Current-voltage

characteristics similar to the ones described above were observed at nanowire bias voltages larger than 20 mV. However, the devices failed (devices from samples S64 and S67) at currents higher than 200 nA due to excess heating at localized spots within the nanowire. The same measurements were performed on other fabricated devices (S69-C1 and S72-A2) yielding similar results.

The small change of nanowire current suggested that the applied gate bias was not able to fully deplete the free carriers in the nanowire. If free carriers were depleted by the gate potential, the nanowire current would be much smaller. Although the measurement results showed that the nanowire current did response to the applied gate voltage, it is believed that the change of current was mainly due to the distortion of potential distribution within the nanowire instead of the depletion of carriers. Free carriers were still abundance for current conduction when the gate voltage was applied. The change of current was too small to construct a functional nanowire transistor with current-off ability. The failure to turn off Bi nanowire current maybe due to the fact that the fabricated Bi nanowire has a carrier density a few orders of magnitude higher than that in other reported semiconductor nanowire transistors [4.1, 4.3 and 4.5]. Parameters of reported nanowire transistors as well as the fabricated Bi device are shown in Table 4.2. From the Table, it is clear that Bi device has a higher carrier density and lower on/off current ratio. The high carrier density in Bi nanowires made the control of carriers by applying gate bias difficult. Investigation on the potential distribution of the gate biased nanowire was performed in an attempt to understand the carrier transport in the nanowire under the influence of gate voltage.

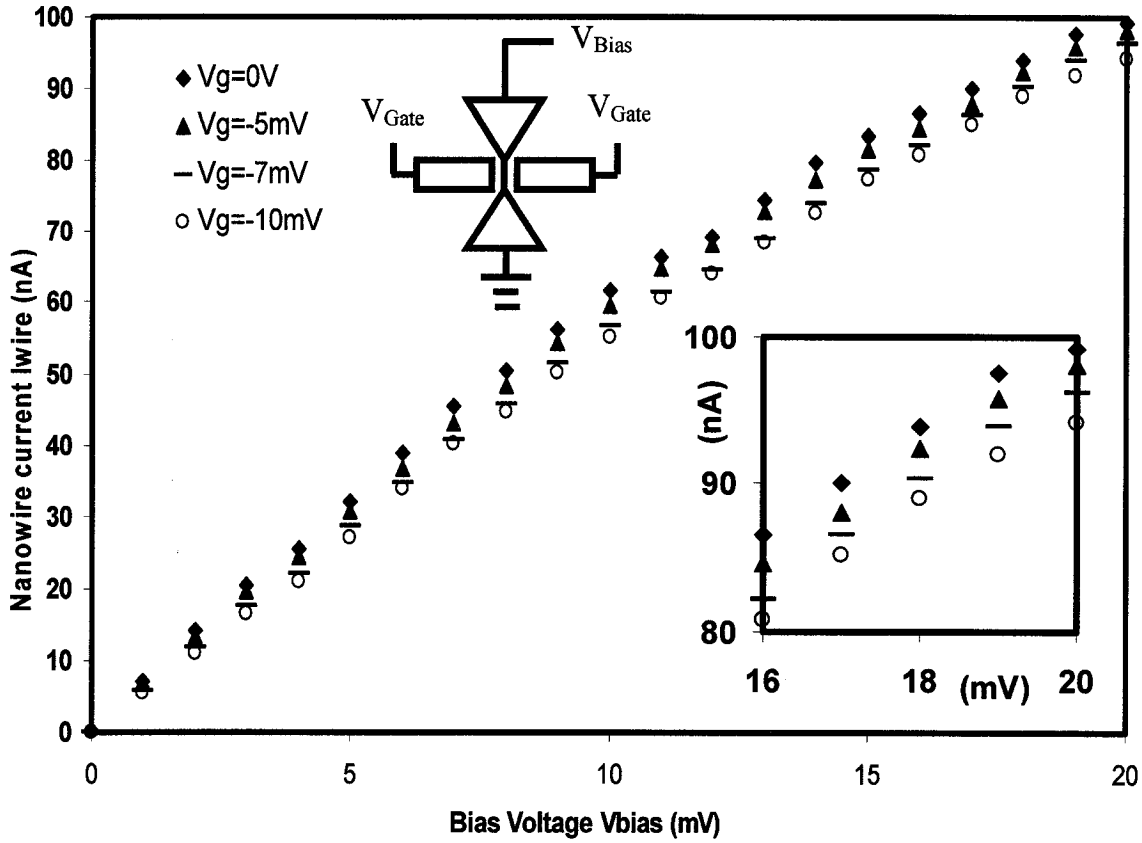


Figure 4.5: Current-voltage characteristics of a Bi nanowire with dual side-gate structure at different gate voltages. (Inset: an enlarged view of current-voltage characteristics from 16 to 20 mV) Measurement data were taken from device S69-B1 with 3% measurement error.

Table 4.2: Reported nanowire transistors.

Nanowire transistor material	**Structure**	**Carrier density**	**On/Off current (Ratio)**
Ge [4.3]	Top gate	Not reported Intrinsic carrier density $= 2.4 \times 10^{13}$ cm^{-3}	2.5/0.1uA (25)
GaN [4.5]	Back gate	4.9×10^{5} cm^{-1} – 6.6×10^{7} cm^{-1} (Estimate: 1×10^{9} - 10^{11} cm^{-3})	30/2 nA (15)
Si [4.1]	Side gate	4.58×10^{9} cm^{-3}	0.3/0.2 pA (1.5)
Bi (present work)	Dual side gate	3×10^{17} cm^{-3}	99/94 nA (1.05)

4.4 Electrostatic potential distribution of the dual side-gate structures

Potential distribution within the nanowire was analyzed in order to study the effect of nanowire current reduction. As a negative voltage was applied to both side-gates, potential was coupled into the nanowire situated between the side-gates due to the electrostatic potential from the closely spaced side-gates. The magnitude of potential coupled into the nanowire depended on the gate-to-wire spacing. A numerical simulation was performed using FlexPDE 3 software package [4.8] to compute the potential distribution within the nanowire.

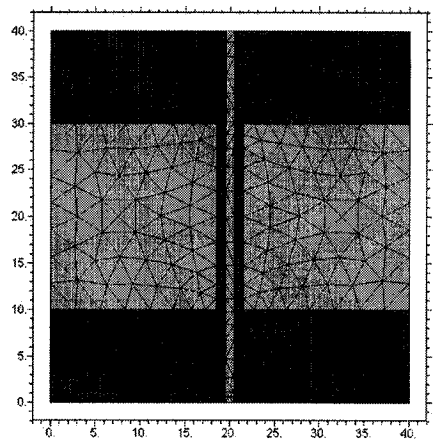
Electrostatic potential distribution along the nanowire axis

Graphical representation of the simulation models are shown in Figure 4.6. A simulation model consisted of a nanowire and dual side-gates with dimensions same as the fabricated devices. In addition, models with different gate-to-wire spacings were established to compare the effect of side-gate structures to the potential distribution. Four gate-to-wire spacings (sp = 0.1 μm, 1 μm, 2 μm and infinity) were used in the simulation. Assuming the permittivity value of nanowire and gate regions to be 20 times higher than the surrounding, and the gate voltage and the nanowire bias were -10 mV and 20 mV respectively, the electrostatic potential distribution can be computed using following equation:

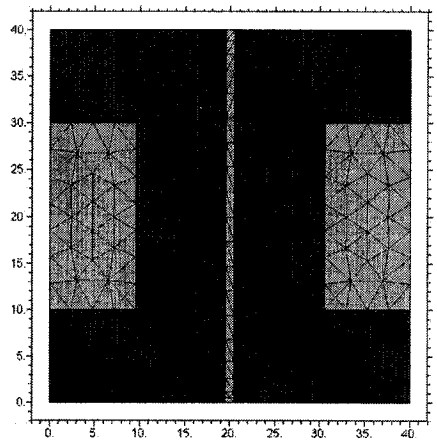
$$\nabla \cdot (\epsilon \nabla V) = 0 \quad \text{(Eq. 10)}$$

where ϵ is the permittivity (F/cm) and V is the electrostatic potential (V). The computed results are shown in Figure 4.7. From the simulation results, it is clear that only the device structure with the smallest gate-to-wire spacing (sp = 0.1 μm) is able to couple potential into the nanowire effectively. The potentials at both ends of the nanowire were fixed at 2 mV and 0 mV due to the nanowire bias itself, while the potential in the middle section (nanowire position 1 to 3 μm) of the nanowire was affected significantly by the side-gate structures. The applied negative gate voltage was coupled into the nanowire effectively from both side-gates. The resulting electrostatic potential distribution within the nanowire was a distortion of potential in the middle section; a negative potential barrier formed in the nanowire at position 1 to 3 μm. On the other hand, with the gate-to-wire spacing equaled to infinity (sp = infinity, no side-gate structures), the potential

distribution within the nanowire was almost a straight line showing a constant electric field along the nanowire with no indication of potential coupling from the side-gates. The reduction of nanowire current with negative gate voltage from the current-voltage measurement results was caused by the distortion of potential distribution. The applied negative gate voltage coupled into the middle section of the nanowire created a negative potential barrier. Electrons traveling to this section of the nanowire experienced the potential barrier. Only those electrons acquired enough energy can overcome the potential barrier, thus the overall mobility of the gate-affected nanowire decreased which led to a reduction of nanowire current.



(a)



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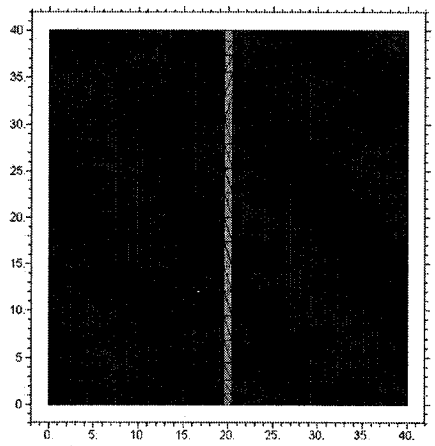

(c)

Figure 4.6: Simulation models with gate-to-nanowire spacing of (a) 0.1 μm; (b) 1 μm; (c) 2 μm (gate voltage applied at the edge of the model) and infinity (no gate voltage applied).

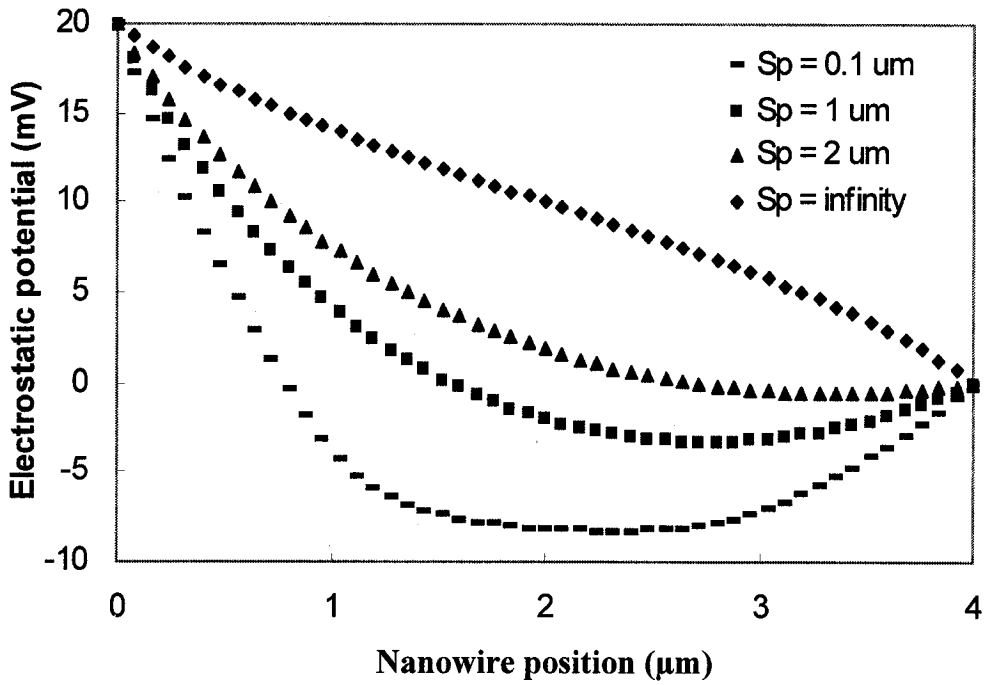

Figure 4.7: Simulation results for the electrostatic potential distribution along the nanowires with different gate-to-wire spacings, sp. The nanowires were biased at 20 mV with a gate voltage of -10 mV. The model with gate-to-wire spacing equal to 0.1 μm clearly showed the potential barrier created in the middle section of the nanowire (1 to 3 μm) due to the side-gates potential coupling.

4.5 Chapter summary

In the second phase of the thesis, Bi nanowires with dual side-gate structures were fabricated successfully using a modified nanowire fabrication process. The fabricated device consisted of a nanowire with dimensions of 50 nm x 100 nm x 4 μm (thickness x width x length) and a 2 μm wide gate with gate-to-nanowire spacing of 100 nm. The devices were fabricated across Au/Cr bonding pads. Current-voltage measurements revealed that a small reduction of nanowire current took place when a negative bias was applied to the gate. The nanowire current reduced 7% when biased at 20 mV with -10 mV gate voltage. This small current reduction observed suggested that the applied gate bias was not capable of turning off the device by fully depleting the free carriers. Instead, carriers transport was affected by the distorted potential distribution. The distorted potential distribution was visualized by numerical simulation of the device structure. The simulation resulted showed the 100 nm gate-to-nanowire spacing structure was able to couple gate potential effectively into the middle section of the nanowire. A negative potential barrier was created in the nanowire and reduced the nanowire current flow.

The inability in forming a functional Bi nanowire transistor in this phase of work was mainly due to the high carrier concentration in the Bi nanowire. The carrier concentration is many orders higher than that in the reported semiconductor nanowire transistors (Table 4.2). The applied gate voltage was not able to fully deplete the high carrier density of Bi nanowire by field effect. The inability of fully controlling the carriers by the applied gate voltage has prevented turning off the device. Part of the research results from this chapter has been presented in the second McGill NanoEngineering Workshop in May 2005 at McGill University and in the Canadian

Semiconductor Technology Conference in August 2005 at the Fairmont Château Laurier hôtel of Ottawa.

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Chapter 5: Bi nanodot structures

In the previous two phases of this work, we had explored the carrier transport properties of Bi nanowires and Bi nanowires with dual side-gate structures. Because of the small effective mass of the Bi material, energy levels are quantized in the 1-dimensional nanowire. The quantization of energy levels led to the creation of quantum confinement-induced bandgap. Through experimental results, Bi nanoelectronic devices proved to have semiconductor conduction behavior when the critical dimension was less then 50 nm. External potential coupled into the nanowire from the side-gate structures changed the conductance of the nanowire by a few percents. In phase III of the thesis work, an even lower dimensional device was fabricated to further study the energy level quantization in Bi nanoelectronic devices. As stated before, Bi is a very attractive material to form quantum effect devices due to its metallic bulk material nature and simple processing technology. In this work, a more elaborate fabrication process was developed to fabricate Bi nanodot structures. Bi nanodots with diameters of 100 nm were fabricated. Different from the 1-dimensional nanowire, the 0-dimensional nanodot confined electrons in all 3 dimensions. The confined electrons are allowed to stay in only discrete energy levels. The energy levels spacings in the nanodot are dictated by the size of the nanodot itself. The influence of energy level quantization can be qualitatively understood by examining its effect on the density of states. The density of states function is a measure of the allowed energy levels [1.9, 5.1]. In bulk material, electrons can travel in all 3 dimensions inside the material. The density of states increases as the square root of the energy (Figure 5.1a). In a 2-dimensional structure such as thin film or quantum well, electrons can only travel freely on a plane in two directions. In this case, the

density of states function became a "step" function (Figure 5.1b). For a nanowire or quantum wire device, electron can only travel back and forward in one direction (1-dimensional device). The density of states drops at each energy levels (Figure 5.1c). For a 0-dimensional device such as nanodot or quantum dot, electrons are restricted in certain energy levels only. Energy areas beyond the discrete energy levels are forbidden for electron to stay. The density of states in this structure becomes a delta function (Figure 5.1d).

In the present work, a further improved Bi nanoelectronic fabrication process was developed aiming to fabricate 0-dimensional nanodots with discrete energy level quantization. Bi nanodots were fabricated by an elaborate combination of e-beaming writing, thermal evaporation and the utilization of proximity effect. Unlike in the fabrication of nanowire with gate structures where the proximity effect was an unwanted effect and patterns were designed to compensate it; in the fabrication of Bi nanodots, the proximity effect was actually utilized to form the nanodot structure. The fabricated device consisted of a 100 nm-diameter Bi nanodot and electrodes placed very close to it to allow electron tunneling from/to the nanodot. In order to form tunneling contacts, electrodes have to place a few nanometers from the nanodot. This nanometer spacing is not achievable by direct e-beam writing. Proximity effect is then utilized to form the tiny gap between the nanodot and electrodes. The conduction behavior of Bi nanodot was expected to be semiconductor due to the quantum confinement-induced bandgap. Current-voltage measurements at different temperatures were performed on the fabricated Bi nanodots. "Staircase" conductance characteristic was observed due to the discrete energy levels of the nanodots. In the following sections, a brief review of nanodot (quantum dot) devices, the single electron transistors (SET) will be described. The SETs

operate based on the principle of energy quantization, the theories of Coulomb blockade and Coulomb staircase effect. Different types of nanodot structures will also be discussed briefly. In the later sections, the fabrication and characterization of Bi nanodot will be presented in details.

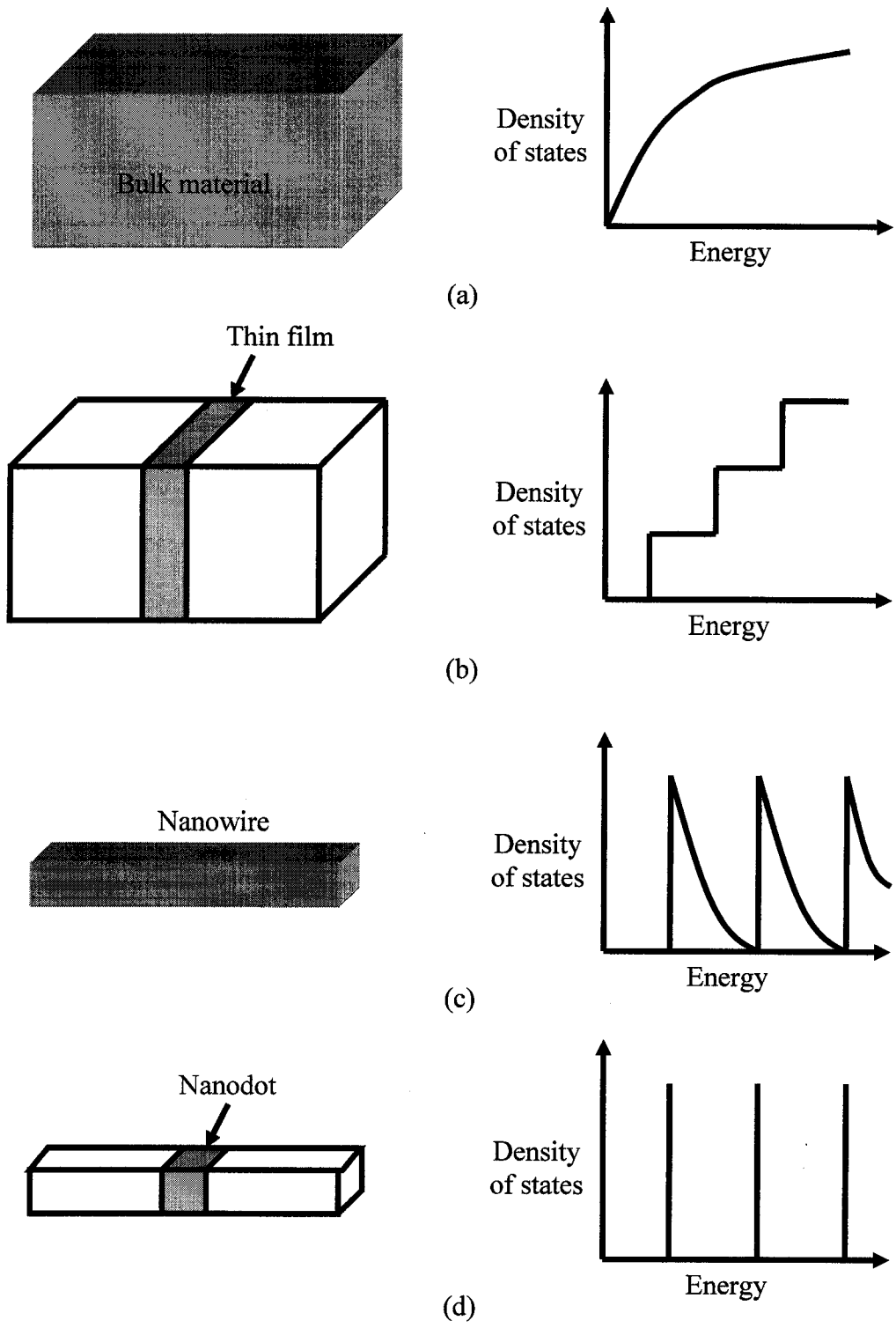


Figure 5.1: Density of states for (a) 3-D device; (b) 2-D device; (c) 1-D device; (d) 0-D device.

5.1 Devices based on nanodots

Nanodots, also known as quantum dots or artificial atoms, have been well studied for their unique energy level quantization characteristics. Sizes of nanodots range from a few nanometers to tens of nanometers depending on the material parameters and fabrication techniques. Typically, a smaller nanodot has a larger energy level quantization. Because of this size dependent energy level quantization, nanodot size can be tuned to a desired energy level and devices based on specific energy level can be built. Using the advanced fabrication technologies of the semiconductor industry, scientists can now routinely integrate nanodots into functional electronic devices. With the integration of nanodots, the performance of bulk devices can be enhanced. Practical devices based on the energy quantization of nanodots have been developed for various functions. One of the most commonly used devices in this area is the quantum dot laser [5.2]. With the introduction of quantum dots in the active region of the laser, electrons can occupy only discrete energy levels in the population inversion region. It leads to a more efficient recombination of electrons and holes and emits a more discrete wavelength. The quantum dot laser also has a smaller threshold current and larger differential gain than its bulk counterparts. The operation of quantum dot laser is well studied in the laser research community. Details on the principles of quantum dot laser can be found in many semiconductor laser text books. A well written book on the topic is published by A. E. Zhokov [5.3]. Due to the page limitation of the thesis, the principles of quantum dot laser are not discussed here.

In addition to the enhancement of bulk electronic devices, nanodots can be used to form novel electronic devices operate based on the quantum effect. One of the most

promising nanoelectronic device based on nanodots is the single electron transistor (SET). In SET, electrons tunnel into/from an isolated island (nanodot) in a controlled manner. The flow of electrons is controlled by an external gate. In the next few pages, a brief overview of the operation of SET is presented.

Single electron transistor

Single electron transistor (SET) is one of the most fundamental devices related to the nanodots. SET is a three-terminal device that has the ability to control the flow of electrons through a conducting nanodot. The nanodot in a SET is usually referred to as an island or coulomb island. In the SET, electrons are trapped on the island and can only escape the island by tunneling. The theoretical study of single electron devices was well established in the last decade [5.5 – 5.8]. The first SET was fabricated successfully in 1987 [5.9, 5.10]. The key element in a SET is a small conduction island. The size of the conduction island ranges from 10 nm to 100 nm depending on the island materials. The small island is surrounded by potential barriers. Insulator material such as oxide is a common potential barrier in SET. Typical thickness of the insulator layer is 5 – 10 nm to allow electrons tunneling. Different materials have been used to form SET. These materials included semiconductors and metals. Reported island and barrier materials for SETs are summarized in Table 5.1 [5.5].

A SET device consists of three terminals, similar to the conventional MOSFET, they are source (S), drain (D) and gate (G). Source and drain terminals are fabricated close to the conduction island to form tunneling junctions. Gate terminal is placed adjacent to the structure for gate potential coupling with minimum leakage current. An equivalent circuit of a SET is shown in Figure 5.2. SET can regulate the flow of electrons from the source to the drain terminals. Electrons tunnel from the source terminal to the conduction island, and then tunnel from the island to the drain terminal one by one. To control the flow of electrons, SET exploits the Coulomb blockade for manipulating the tunneling electrons. Coulomb blockade is a phenomenon on the

conduction island that repulses any electrons trying to flow into the island by a Coulomb repulsive force. It is obvious that the Coulomb blockade is the key physical effect that facilitates the operation of SETs. In the next section, principles of Coulomb blockade are discussed.

Table 5.1: Reported SET island and barrier materials [5.5].

Island material	**Barrier material**
Al	AlO_x
CdSe	Organics
Ti	Si
Carboran molecule	Carboran molecule
Si	SiO_2
Nb	NbO_x

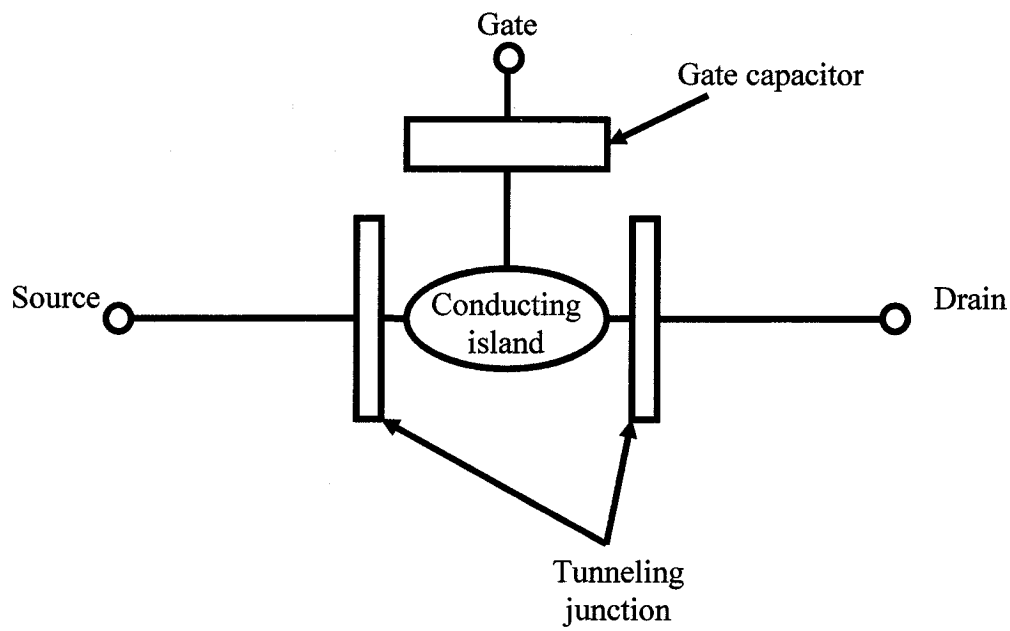


Figure 5.2: An equivalent circuit of a SET.

Coulomb blockade

To understand the operation principles of Coulomb blockade, one has to first understand how charge transfers on a conduction island. For a very small conduction island surrounded by insulator where Coulomb force is significant, charges repulse each other and accumulate on the surface of the island against the insulating layer [5.5]. At equilibrium, a fixed number of charges, N, stabilizes on the surface. On the other hand, quantum mechanics tells us that only an integer number of charge can be transferred between materials. If an additional electron (charge number N+1) try to tunnel through the insulator layer and inject on the island, the total surface charge of the island will have to change exactly by e (one charge). However, if the island is already stabilized and is electrostaticaly stable, the incoming electron will experience repulsive Coulomb force from the charges staying on the surface of the island. Without additional energy, the incoming electron cannot overcome this Coulomb repulsive force and cannot inject on the island. This Coulomb repulsive force is known as the Coulomb blockade. The Coulomb blockade simply blocks all the electrons from tunneling onto the island by the Coulomb repulsive force. The strength of Coulomb blockade is the electrostatic potential of the conduction island that an electron needed to overcome to inject on the island. The value of Coulomb blockade can be calculated from the island structure [5.11]. The island structure can be modeled as a capacitor with capacitance C_{total} which consists of capacitances across all the barriers. The electrostatic potential of the island for N electrons is

$$\mu_{dot}(N) = E_N + \frac{(N - N_o - 1/2)e^2}{C_{total}} - e\frac{C_g}{C_{total}}Vg \quad \text{(Eq. 11)}$$

where E_N is the single-particle state for N^{th} electron measured form the bottom of the conduction band. C_g is the gate capacitance. V_g is the gate voltage and N_o is the number of electrons on the island at zero gate voltage. The Coulomb blockade is the change of electrostatic potential of the island structure when the N+1 electron is added to the system. This change of potential is modeled by

$$\mu_{dot}(N+1) - \mu_{dot}(N) = \Delta E + \frac{e^2}{C_{total}} \qquad \text{(Eq. 12)}$$

where ΔE is the energy level difference between the 0-dimensional energy states and is equal to

$$\Delta E = E_{N+1} - E_N \qquad \text{(Eq. 13)}$$

To simplify the equation, we can assume ΔE is very small and is negligible. This is the case of metallic nanodot where ΔE is usually in the order of uV. (Another model which considered non negligible ΔE is presented in the non-linear current-voltage characteristics section.) Then the Coulomb blockade is simplified to

$$\text{Coulomb blockade} = \frac{e^2}{C_{total}} \qquad \text{(Eq. 14)}$$

Because the Coulomb blockade is the energy that an electron required to inject onto the island, therefore it can be represented by an energy gap in the tunneling density of states on the conduction island shown by Figure 5.3.

It is understandable that Coulomb blockade is an off-state of the SET where no current flow is allowed. In order for electrons to tunnel onto the island, one needs to disrupt the stable electrostatic energy of the system. The system becomes unstable only when the electrostatic energy of the system increases or decreases by half of the Coulomb blockade energy $e^2/2C_{total}$. At this moment, the additional energy attracts electrons from

outside of the island to tunnel into the system. Under this circumstance, the Coulomb blockade of the island diminishes and an electron with charge e can tunnel onto the conduction island. Because the half Coulomb blockade energy is required to allow the flow of electrons and turn on the SET, it is also referred to as the activation energy of the SET. A diagram showing the diminishment of Coulomb blockade is shown in Figure 5.4. In a practical SET, the activation energy is provided by the gate voltage from the gate terminal. In order to observe the Coulomb blockade in a SET, the Coulomb blockade energy have to be large enough to be measured by equipment. Thermal fluctuation is a significant problem in realizing SETs. As a rule, the thermal fluctuation energy has to be a few orders or magnitude smaller than the Coulomb blockade to form a practical SET:

$$\frac{e^2}{C_{total}} >> k_B T \quad \text{(Eq. 15)}$$

where k_B is the Boltzmann's constant and T is temperature in Kevin. Previously defined equation (Eq. 14) tells us that Coulomb blockade is inversely proportional to the total capacitance of the island structure. Therefore, the only way to increase Coulomb blockade is to minimize the island capacitance. For a disk shape island and a sphere island, the island capacitance is

$$\textit{Disk shape island: } C_{total} = 8\,\varepsilon_r \varepsilon_o R \quad \text{(Eq. 16)}$$

$$\textit{Sphere island: } C_{total} = 4\pi\,\varepsilon_r \varepsilon_o R \quad \text{(Eq. 17)}$$

where R is the radius of the island. In order to have an operational SET, one must either minimize the size of the island significantly or reduce the operation temperature dramatically.

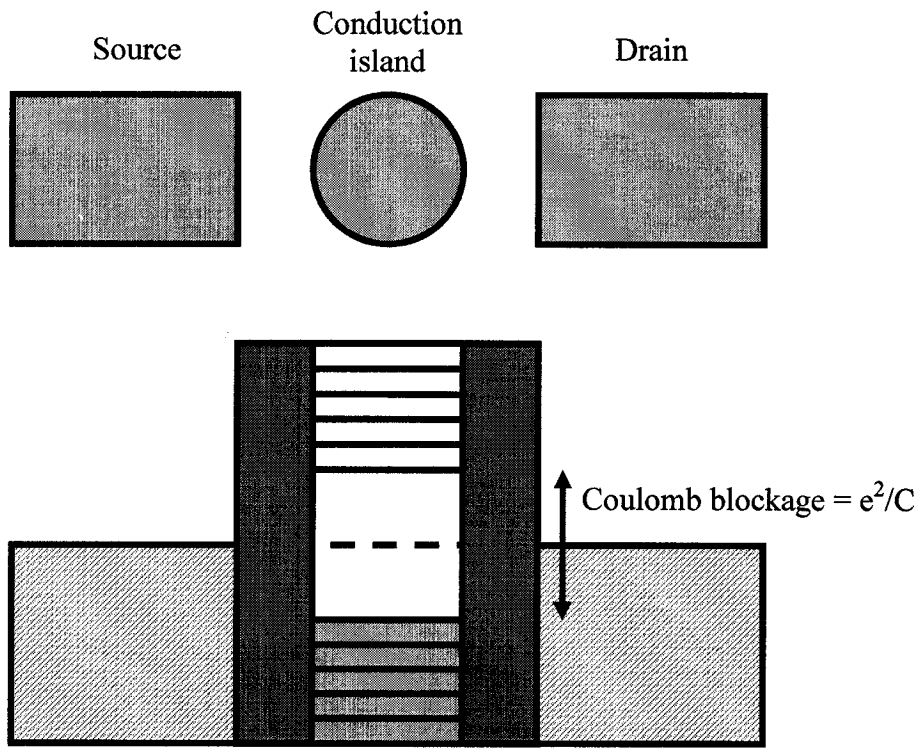
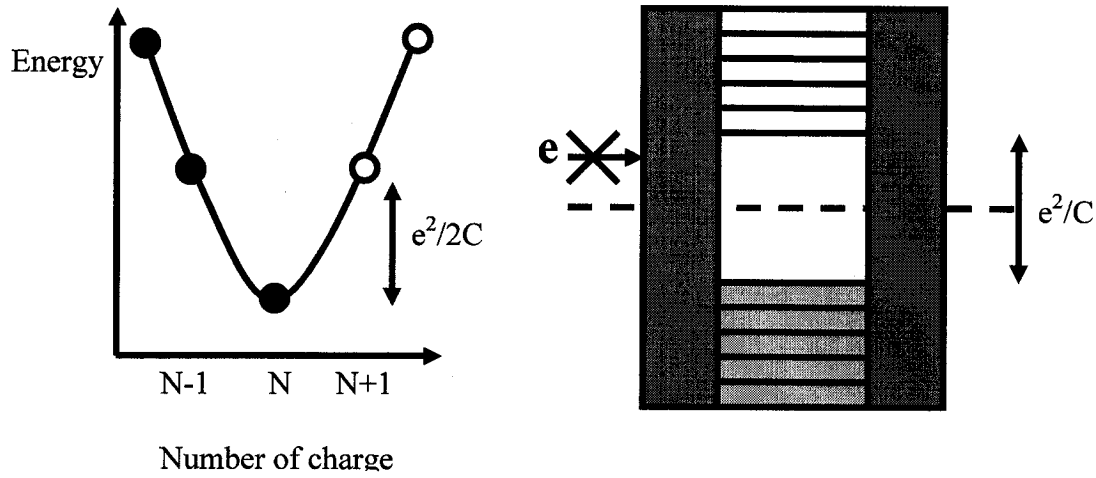
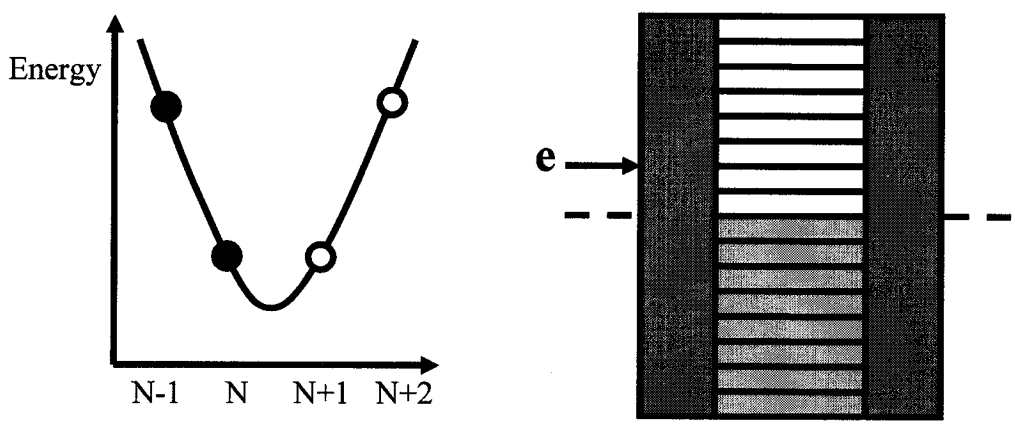


Figure 5.3: Energy state diagram of a Coulomb blockade system. Top: Conduction island and source/drain terminals. Bottom: energy level spectrum for the system, showing filled (grey) and empty (white) levels. The Coulomb blockade energy e^2/C is represented by the empty space between the filled and empty levels.



(a)



(b)

Figure 5.4: The diminishment of Coulomb blockade of a conduction island. (a) The system is stable with Coulomb blockade established, preventing electrons from entering the island; (b) The introduction of half Coulomb blockade energy $e^2/2C$ causes the diminishment of Coulomb blockade and allows electrons to tunnel onto the island.

Non-linear current-voltage characteristics

In the Coulomb blockade equation (Eq. 14), we assumed the energy level spacing ΔE on the island is small and negligible. However in certain materials, the energy level spacing can be significant and measurable. This large energy level spacing leads to a different current-voltage characteristic of the SET. Not surprisingly, bismuth material investigated in the previous two chapters has very small effective mass and large energy level spacing due to the quantum confinement effect. Electrons residing in a nanodot structure can occupy only quantized energy levels. The level spacing at the Fermi energy for a box of size L is given by the inverse of the density of states and is size dependent. ΔE can be computed by Equation 18:

$$\Delta E = (N/4)\hbar^2\pi^2/m_eL^2 \qquad \text{1D} \qquad \text{(Eq. 18a)}$$

$$= (1/\pi)\hbar^2\pi^2/m_eL^2 \qquad \text{2D} \qquad \text{(Eq. 18a)}$$

$$= (1/3\pi^2N)\hbar^2\pi^2/m_eL^2 \qquad \text{3D} \qquad \text{(Eq. 18c)}$$

where N is the energy level, m_e is the effective electron mass and L is the dimension. Note that for a 1-D box, the energy level spacing actually grows for increasing N. The characteristic energy scale is $\hbar^2\pi^2/m_eL^2$ and is approximately the level spacing for the lowest 2 levels in a 0-D box. The value of a measurable energy level spacing is temperature dependent and is generally following the rule that $\Delta E > k_BT$. For a Bi nanodot with a diameter of 100 nm and reported effective mass of $0.001m_e$, the energy level spacing is 75.2 meV which is large enough to be observed even at room temperature at least in theoretical computation.

To observe the energy levels on a nanodot, one can monitor the drain current while increasing the source/drain (S/D) voltage. For a nanodot with significant Coulomb blockade but very small energy level spacing, the drain current should not increase until the S/D voltage is larger than the $e/2C_{total}$ level. A further increase in S/D voltages leads to an exponential increase of the current. This current-voltage characteristic can be explained by the energy diagram of the system in Figure 5.5. When the S/D voltage is below the $e/2C_{total}$ threshold (Figure 5.5a), electrons are not allowed to flow due the Coulomb blockade on the island. Once the S/D voltage is above the $e/2C_{total}$ threshold, electrons in the source terminal is aligned with the first energy level above the Coulomb blockade on the island and is allowed to tunnel through the island (Figure 5.5b). A further increase in the S/D voltage will open up more paths (more energy levels) for electrons to flow through the island. If the energy level spacing is very small, the increase of electron flow paths is not measurable and the increase of current is continuous (Figure 5.5c). However, for a structure with significant energy level spacing such as the Bi nanodot structure, the increase of electron flow paths is measurable due to the large energy level spacing. Therefore, the resultant current-voltage plot should have a pronounced step like characteristic (Figure 5.5d). Each step in the current-voltage plot corresponds to one additional energy level opened up for electrons to flow. This step like characteristic in SETs is known as Coulomb staircase [5.14]. Because of the symmetric nature of the nanodot structure, current-voltage characteristic is also symmetric at zero voltage axis.

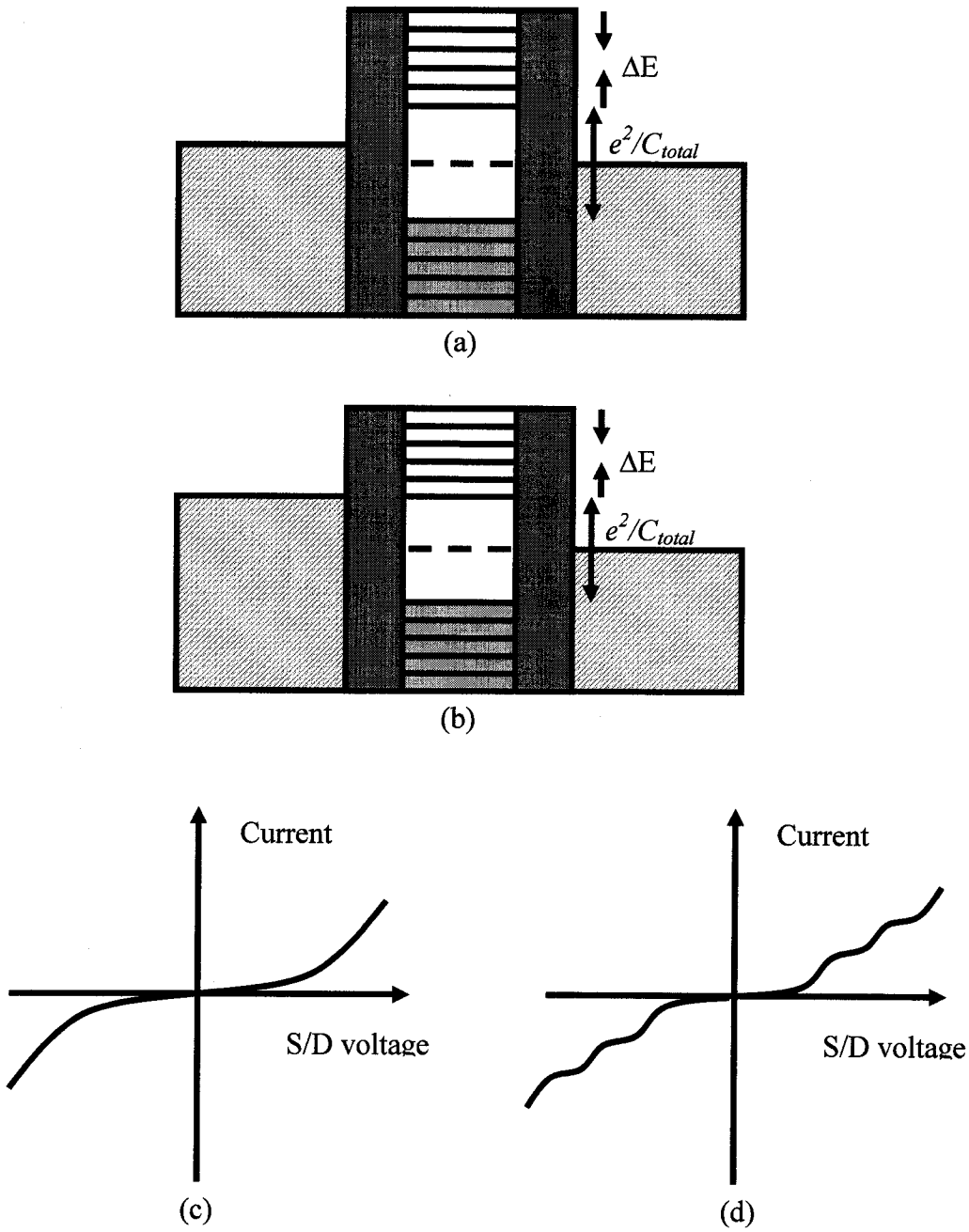


Figure 5.5: (a) S/D voltage below $e/2C_{total}$ threshold with no conducting path for electrons flow; (b) S/D voltage above $e/2C_{total}$ threshold with conducting path for electrons flow; (c) Small energy level spacing ΔE resulted in continue increase of current; (d) Large energy level spacing ΔE resulted in Coulomb staircase characteristic. [5.14]

5.2 Different nanodot structures

The nanodot structure in a SET is the most important structure in the device. The size of nanodot dictates the strength of Coulomb blockade and energy level quantization; hence it determines the overall current-voltage characteristic of the device. In addition, nanodot size also influences the device immunity to external thermal fluctuation. This is because a smaller nanodot has a smaller total capacitance C_{total}, and Eq. 15 tells us that a small C_{total} is desired to have a high operational temperature and better immunity to thermal fluctuation. It is doubtless that a small nanodot is preferred to form a functional SET. However, even with today's advanced fabrication equipment, nanodots with diameters ranging from 10 to 100 nm cannot be realized without innovative device structures and fabrication skills. Scientists have invented several methods to fabricate SETs with different nanodot structures and materials. In general, the SET fabrication methods can be categorized into two groups; one with electrical confinement of Coulomb island and the other with physical formation of conduction island. Both methods are intended for research purposes with low throughput. Scientists have yet to find methods to fabricate SET in a large volume with high yield.

Electrically confinement of Coulomb island

In this method, nanodot is achieved by confining electrons in a piece of semiconductor [5.15]. The electrons confinement takes place in a thin layer of semiconductor grown on a substrate. Very often III/V materials with heterostructures are used to form the thin semiconductor layer. But with the advances in non-conventional silicon processing, silicon on insulator (SOI) layer becomes more and more popular in forming the SETs. Within the thin semiconductor layer formed on the substrate, electrons are already confined in the 2-dimensional layer. In order to form a nanodot structure, electrodes are placed on top of the semiconductor layer in such a way that when a voltage is applied to these electrodes, electric field generated from these electrodes extends into the semiconductor layer and repulse free carriers. A well designed electrode configuration can manipulate electrons by carefully controlling the applied voltage and confine them in a small area. Coulomb island is formed when electrons are confined in this small area. A star shape configuration of electrodes shown in Figure 5.6 is a commonly used structure. Recently, a SET with electrically formed Coulomb island on SOI has been reported [5.16, 5.17].

The electrical confinement of Coulomb island method provides an easy way to create a Coulomb island without the need of high resolution lithography equipment. This method eases the high cost and low yield problem associate with the SET processes. However, using this method Coulomb island can only be formed in the semiconductor layer. It restricts the choice of island materials to semiconductor only. Metallic island or materials that can not be deposited on substrates cannot be formed using this method.

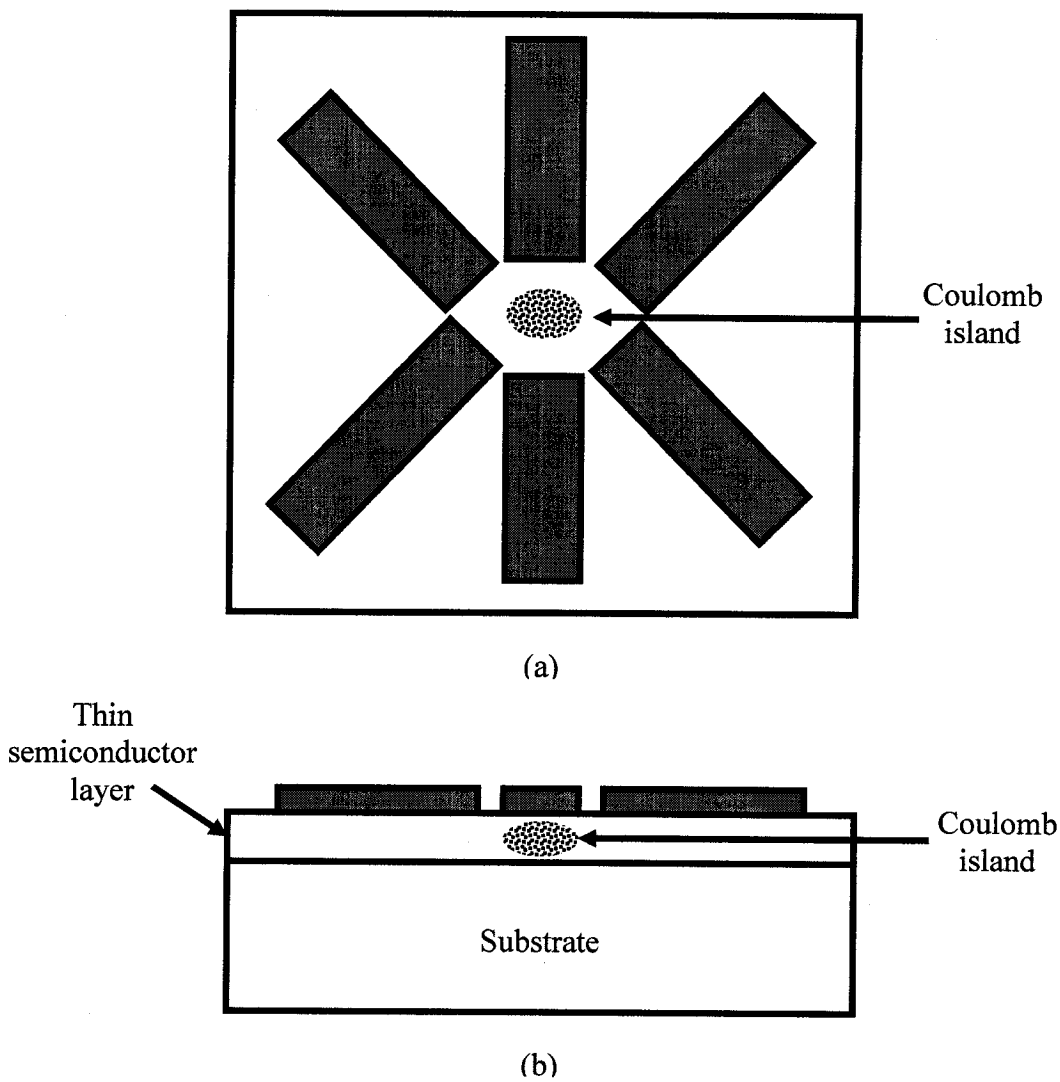


Figure 5.6: (a) A top view of a star shape configuration of electrodes; and (b) a cross-sectional view of the star shape configuration of electrodes.

Physical formation of conduction island

In the physical formation method, the conduction island is fabricated in a straight forward approach. The island is defined by a high resolution lithography process such as sub-micron optical lithography or e-beam writing. In such method, choice of island material is flexible. The island can be either semiconductor or metal. The island material can be deposited before or after the island definition process. For depositing material before the lithography step, an etching process is required to etch away the unwanted material. On the other hand, for depositing the island material after the definition of island, a lift-off process is needed to form the conduction island. Both semiconductor [5.18] and metallic [5.19-5.20] SETs have been fabricated successfully using this method.

The physical formation of conduction island method provides a straight forward means of forming conduction island with wide ranges of island material choices. However, this method is heavily depended on the used of high resolution lithography system and limited in throughput. In addition, even with the advanced lithography system, the fabrication of nanometer size islands is difficult to control and hence the yield of functional devices is generally low.

In the phase III of the thesis, the physical formation of conduction island method is chosen to form Bi nanodot structure. This is simply because bismuth material is metallic in bulk form and very suitable for vacuum deposition. With the use of e-beam writing system and proximity effect, 100 nm-diameter Bi nanodots are successfully fabricated. The fabrication processes and device characterization are presented in the next two sections.

5.3 Bi nanodot fabrication

Bi nanodot structures studied in this work were fabricated using the proximity effects (refer to Figure 3.8) of e-beam writing technique. Bi nanodots were fabricated by performing e-beam writing on a 200 nm-thick oxide layer grown on top of p-type Si substrates. Gold and chromium bonding pads were formed on the substrates using standard lithography and etching processes. Device structures defined by the e-beam writing contained a 100 nm-diameter nanodot, two electrodes placed closely to the nanodot and dual-side gates situated on both sides. A SEM photograph of a device structure is shown in Figure 5.7. The e-beam writing system used is same as the one used in the previous two chapters. It consisted of a JEOL 6100 SEM with NPGS package [3.21]. The system has a patterning resolution of 100 nm which is too large for defining the electrode-to-nanodot spacing. The spacing needed to be less than a few nm in order for electrons to tunnel in and out of the nanodot through the electrodes. To overcome this problem, we relied on the proximity effects of the e-beam writing to bridge the nanodot from both electrodes. The nanodot pattern was designed using CAD software and consisted of a 50 nm diameter nanodot and 50 nm electrode-to-nanodot spacing from both electrodes. By carefuliy controlling the amount of electron dose during e-beam writing process and developing conditions, nanodot and electrode patterns extended by 25 nm in all directions, forming a 100 nm-diameter nanodot and few nanometer electrode-to-nanodot spacing. A SEM picture of the nanodot structure and the corresponding CAD design pattern are shown side by side in Figure 5.8. It was found that the optimized electron dose was 4 nC/cm with 20 keV acceleration voltage and the developing time is 60 second in MIBK:IPA (methylisobutylketone:isopropanol) (1 : 3) solution with 100

nm-thick PMMA (polymethyl methacrylate) e-beam writing resist. After the e-beam writing process, a 50 nm-thick Bi thin film was evaporated over the sample in a vacuum system with a base pressure of 10^{-5} torr and with the sample substrate heated to 100 °C. A lift-off process was then performed to leave behind the Bi nanodot structures.

The Bi nanodot fabrication process is heavily depended on the proximity effect and process control. Specifically, a precise control on the electron dose is needed. A small variation in electron dose resulted in the failure of forming conduction island with tunneling contacts with electrodes. SEM pictures of over- and under-dosed structures are shown in Figure 5.9. Additionally, the thermal evaporation step has been improved in the Bi nanodot fabrication process. In previous chapters, Bi film was evaporated on substrates without heating. The deposited films had a coarse surface similar to the one shown in Figure 5.9a. Fortunately this coarse film surface did not have significant effect on the fabrication of nanowires. However in the fabrication of nanodot structure, the lift-off process had a very high failure rate due to the unevenness of the film surface. The nanodot area either cannot be formed clearly (Figure 5.10a) or the deposited material torn off (Figure 5.10b) from the substrate completely. It was suspected that the uneven thickness of the film in the defined nanodot area has caused the failure in the lift-off process. To overcome this problem, the sample substrate temperature was increased before the evaporation process. The heated substrate led to a slower cool down time of the evaporated film and resulted in a smoother surface as shown in Figure 5.9b. With the introduction of heated substrate, sample yield has been improved to approximately 10% or 1 functional device in each batch of sample (9 devices in each batch). A total of 10 samples (S73-S82) with the Bi nanodot structures were fabricated. Prior to this, a number of trial devices were fabricated in conjunction with earlier samples (S63 – S72). A

fabrication log of the Bi nanodot structure is shown in Table 5.2. Details of the Bi nanodot fabrication processes are shown below:

Bi nanodot structures fabrication details

a) Wet oxidize n-type Si wafer [111] wafer at 1150 °C with oxygen flow of 1.5 cubic feet per hour for 3 hours.

b) Define 1 x 1 mm^2 square Au and Cr bonding pads using standard lithography process.

c) Spin coat 2% 400 kMW PMMA in chlorobenzene on Si substrates at 2500 rpm for 45 sec.

d) Bake samples in oven at 170°C for 30 minutes.

e) Perform electron beam writing with electron beam energy of 20 keV. The writing of nanodot and electrodes use electron line-dose of 4 nC/cm and the writing of gate structures use electron area-dose of 70 uC/cm^2.

f) Develop samples in Methyl Isobutyl Ketone (MIBK): 2 Propanol (IPA) at a ratio of 1 to 3 for one minute.

g) Clean samples using de-ionized water.

h) Load the sample upside down in the evaporation chamber.

i) Bring the evaporation chamber pressure to 10^{-5} torr and heat the sample to 100 °C.

j) Evaporate 5.0 mg Bi powder on the sample (thickness ~ 50 nm).

k) Perform lift-off process in acetone solution (Immerse the solution in ultra sonic bath if necessary).

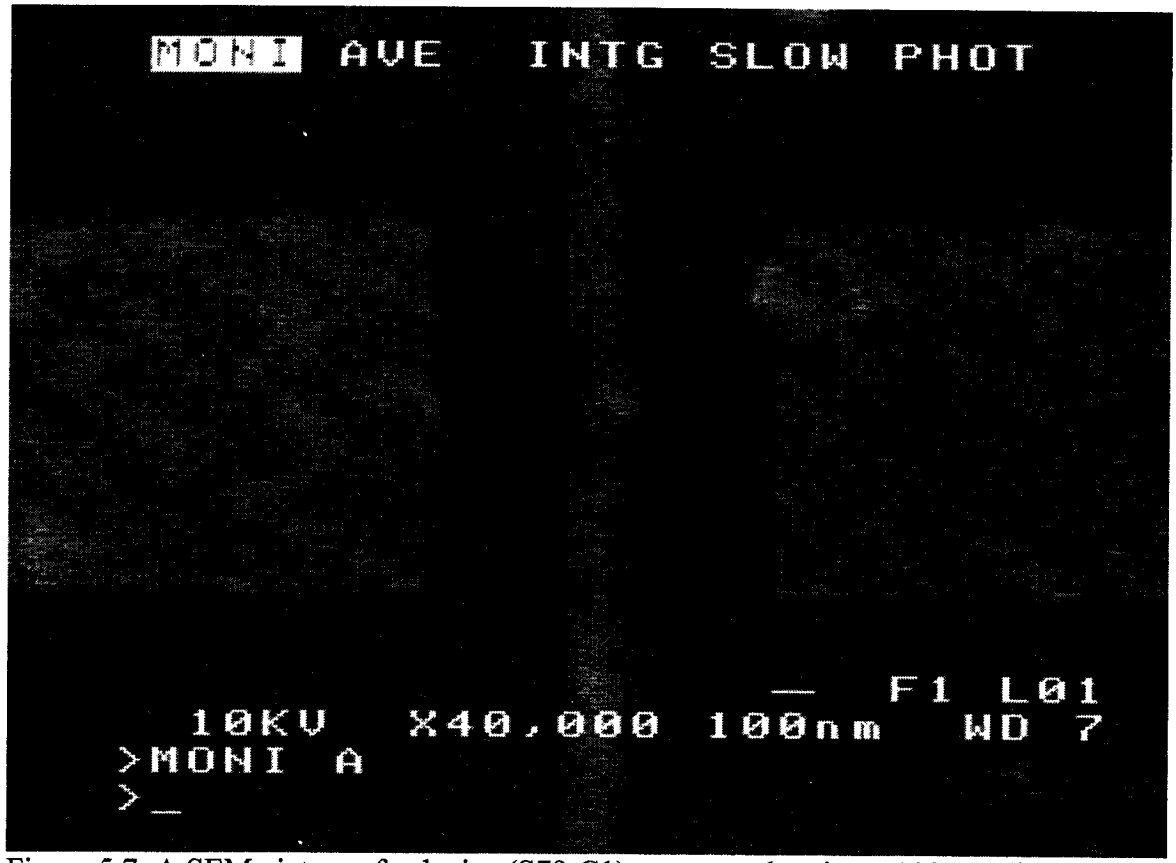


Figure 5.7: A SEM picture of a device (S79-C1) structure showing a 100 nm diameter nanodot, two electrodes and dual-side gates.

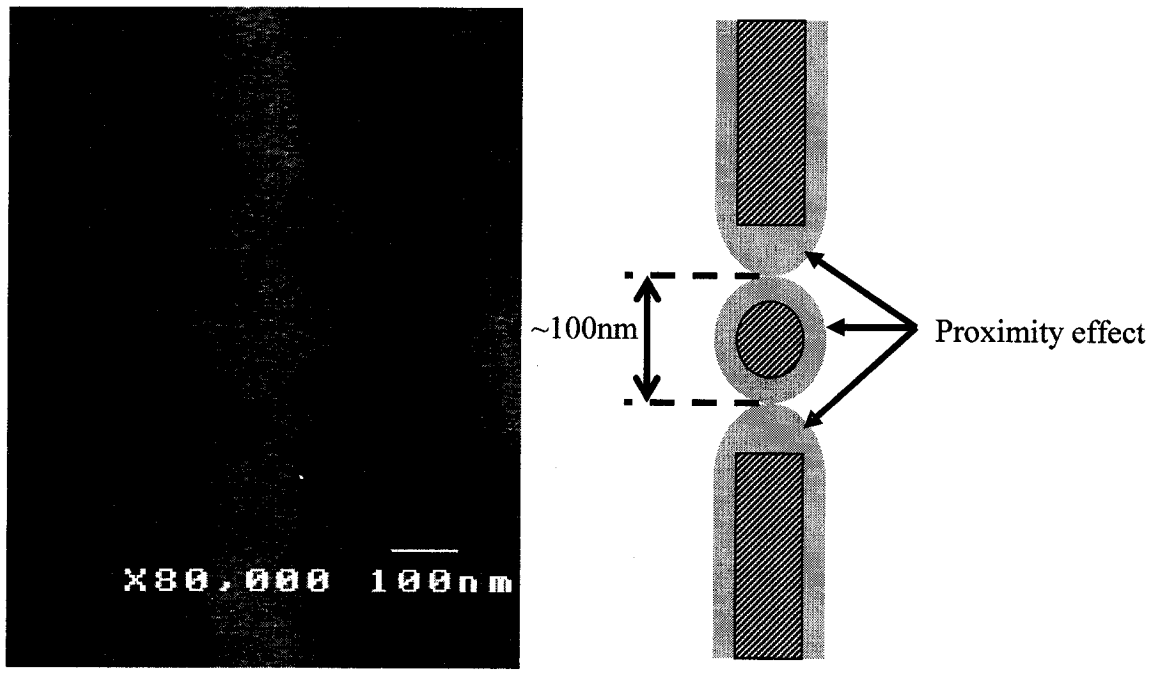
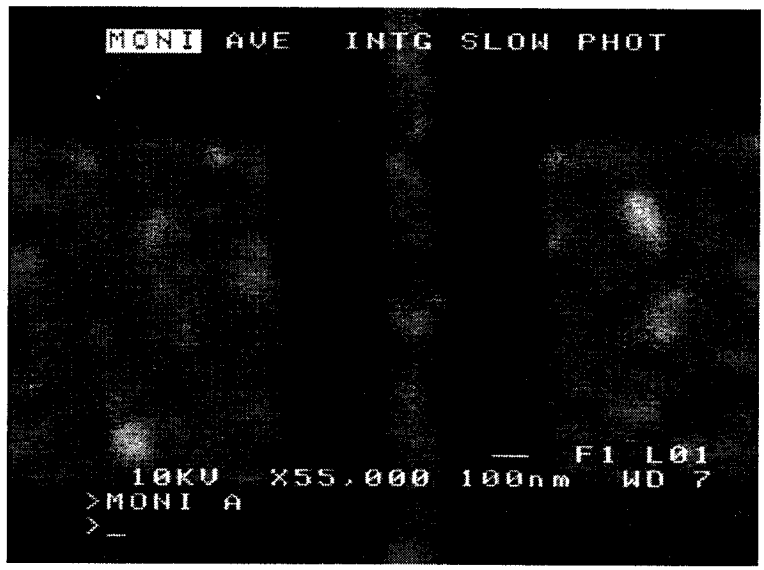
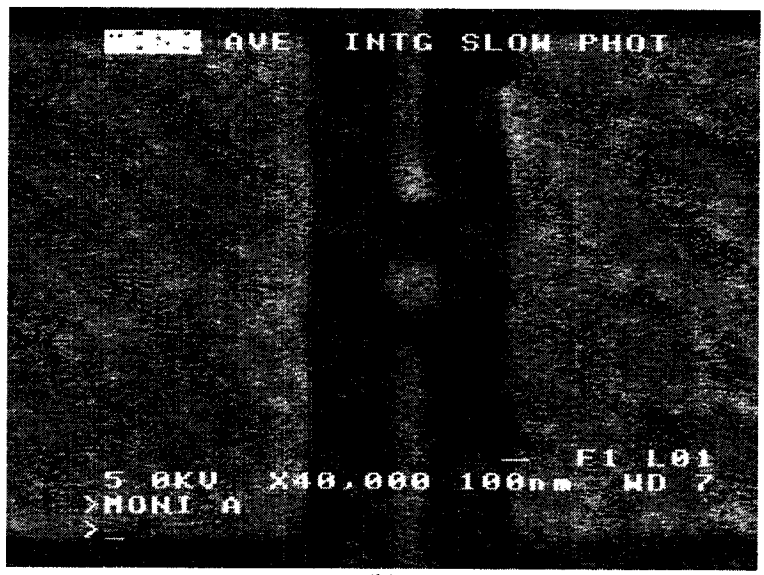


Figure 5.8: A SEM photograph of a nanodot structure (S79-C1) and the corresponding CAD design pattern (strip areas) with the associated proximity effect (shadow areas).

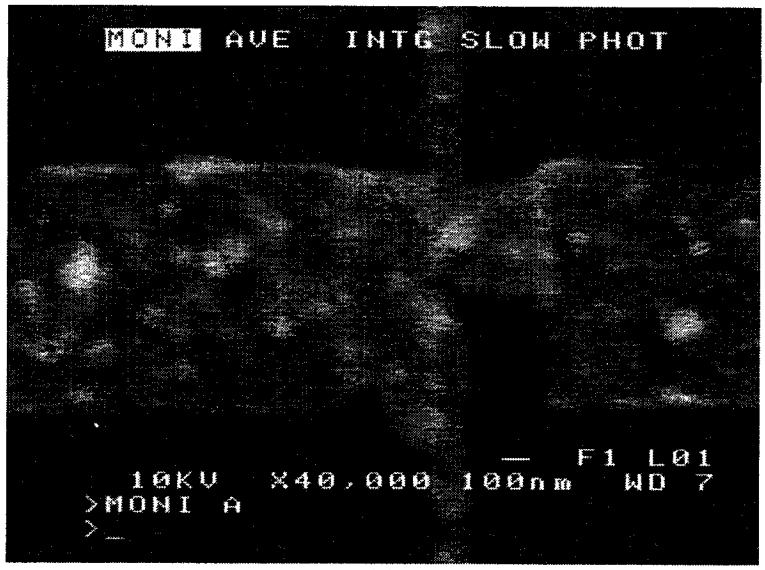


(a)



(b)

Figure 5.9: SEM photographs of non-functional samples. (a) Over-dosed nanodot structure (S70-A2) with the conduction island merged with electrodes. The coarse device surface is a result of evaporation on non-heated substrate. (b) Under-dosed nanodot structure (S72-C3) with large gap between the conduction island and electrodes. The smooth device surface is a result of evaporation on heated substrate.



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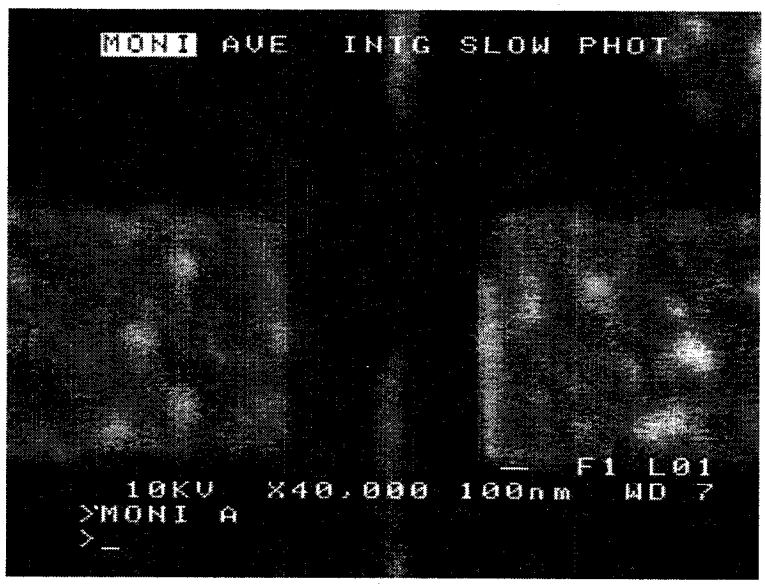

(b)

Figure 5.10: SEM photographs non-functional samples due to the coarse surface of deposited Bi film. (a) Unsuccessful lift-off process (S74-A1); and (b) nanodot structure torn off (S74-C1) from the substrate.

Table 5.2: Bi nanodot structures fabrication log.

Sample number	Remark
S63*	Structure design.
S64*	Structure design.
S65*	Proximity effect evaluation.
S66*	Proximity effect evaluation.
S67*	Structure design.
S68*	Proximity effect evaluation.
S69*	Structure design.
S70*	Proximity effect evaluation.
S71*	Structure design.
S72*	Proximity effect evaluation.
S73	Sample fabrication (process evaluation)
S74	Process failed.
S75	Sample fabrication (process evaluation)
S76	Process failed.
S77	Sample fabrication (process evaluation with heated substrate)
S78	Sample fabrication (process evaluation with heated substrate)
S79	Fabrication successful. Current-voltage measurement.
S80	Fabrication successful. Current-voltage measurement. Non-linear characteristic observed in two devices.
S81	Fabrication successful. Current-voltage measurement.
S82	Fabrication successful. Current-voltage measurement.
S83	Fabrication successful. Current-voltage measurement. Non-linear characteristic observed.

* Trial devices were fabricated in conjunction with Bi nanowire with dual side-gate structures samples.

5.4 Bi nanodot structure characterizations

The electrical characteristics of the fabricated nanodot structures were measured at temperatures from 77 to 300 K using a Hewlett-Packard HP 4145A semiconductor parameter analyzer. The measurement system is the same as the one used in the previous two chapters. Devices were characterized under low vacuum condition (~10^{-2} torr) in a cryostat to avoid reaction between bismuth and oxygen to form bismuth-oxide during the measurements. The two-terminal current-voltage characteristics of a device (S80-A2) at different temperatures are shown in Figure 5.11. The results clearly indicated a strong nonlinear I-V relationship with step-like characteristic for both positive and negative bias voltages at temperatures below 150 K. This step-like I-V characteristic is an evidence of an increase of resistance. Resistance values of the nanodot structure at different bias voltages were calculated based on the I-V measurement data and are shown in Figure 5.12. The resultant plot indicated clear symmetric resistance peaks at ± 2.5 to 5.0 mV bias voltages. The resistance peaks became more significant at lower temperatures. Similar non-linear I-V characteristics have been observed in other devices in the same sample (S80-C1) and in the subsequence sample (S83-C3).

These measurement results suggested that energy level quantization occurs in the present Bi nanodot structures. It is believed that electrons tunneled freely from the electrode to the nanodot at bias voltages below 2.5 mV where the energy states were available near Fermi level. At elevated bias values, the energy level spacing within the nanodot provided no additional energy states for electron tunneling and led to resistance peaks. A further increase of bias voltage overcame the energy level spacing and provided energy states for tunneling again. An energy level diagram of the Bi nanodot structure

and the corresponding current-voltage characteristic is shown in Figure 5.13. The measured resistance peaks corresponding to biasing voltage step of 2.5 mV which is much smaller than the computed energy level spacing (75.2 mV from Eq. 18) (refer to section 5.1). However, the computed value assumed the effective electron mass to be $0.001m_e$ (Eq. 1) which is only valid for electron travels at the trigonal axis. Electron travels in different direction can have a larger mass component. Therefore, the computed energy level spacing (75.2 mV) showed only the best case scenario. For a non-ideal case situation where crystal orientation is not controllable, computation model should use an average value of effective masses from the two lowest conduction bands ($m_e^1 = 0.00119$ m_e and $m_e^3 = 0.00516$ m_e from Eq. 1). The average effective mass is 0.003175 m_e, and the corresponding energy level spacing is 23.7 mV (Eq. 18). In addition, the lowest measurement temperature obtained from this work was at 77 K which contributed to a thermal fluctuation, k_BT, of 13.2 mV of and resulted in a reduction of measurable energy level spacing. Thermal fluctuation should take into account in the comparison of measurement results. Energy level spacing values obtained from the best case theoretical value, non-ideal case theoretical value and measured value with and without thermal fluctuation compensation are summarized in Table 5.3. From the Table, it is found that the measured value with thermal fluctuation, k_BT, compensation (15.8 mV at 77 K and 28.4 mV at 150 K) matched to the non-ideal case theoretical value (23.7 mV). Though this comparison, the observed energy level spacing is justified. The successful observation of staircase (step-like) I-V characteristic at relatively high temperatures in the present work is due to the unique small effective mass of bismuth material. A summery of reported staircase I-V characteristic devices with the corresponding material, island size and measurement temperature is shown in Table 5.4.

Coulomb blockade has not been observed in the devices due to the yet too large nanodot structures. For a measurable coulomb blockade at room temperature, the nanodot diameter needs to be less than 16 nm with a total capacitance (C_{total}) of 0.88 aF [5. 12]. It is noted that the nanodot structure fabricated in the present experiments has a C_{total} of 3.54 aF assuming flat disk structure [Eq. 16] or 5.56 aF assuming sphere structure [Eq. 17]. The Fabricated nanodots have a capacitance value larger than the required value (0.88 aF) thus coulomb blockage was not observable in the devices. Capacitance values for different nanodot structures are summarized in Table 5.5.

During the experiments, a gate voltage was applied to both side-gates in an attempt to shift the resistance peaks by biasing the nanodot. The measurement results showed no shifting. It is suspected that the dual side-gate structure cannot provide an effective confined voltage coupling to the nanodot area and the potential is dispersed in the surrounding electrodes to result in no potential shift between the nanodot and electrodes. As a result, the resistance peaks remained at the same position even with the gate voltage applied.

Other gate electrode configurations such as bottom gate structure (Figure 4.1a) and top gate structure (Figure 4.1b) had been considered. Bottom gate structure uses the back side of the substrate as gate electrode. Similar to the side-gate structure, the gate voltage cannot be confined to the nanodot area and is dispersed around the entire device. Thus, the structure is not a feasible option. Top gate structure with the gate electrode placed directly over the nanodot area is a possible option in theory. In such a structure, the gate voltage can be confined precisely in the nanodot area with minimum dispersion to the surroundings regions. However, with bismuth as seed material, gate dielectric formation is a foreseeable problem. This is because the melting temperature of bismuth is

very low in terms of material processing conditions. The melting temperature is around 272 ^{o}C at atmospheric pressure. The deposition of dielectric layer usually requires a few hundred degrees Celsius or higher. The high temperature dielectric deposition process simply melts the Bi device. Novel materials such as spin-on-glass (SOG) or materials deposited by low temperature PECVD (plasma enhanced chemical vapor deposition) might be a feasible way to form dielectric layers on bismuth. Unlike silicon devices, very few pure bismuth devices have been reported and there is no report on dielectric deposition technique associated with bismuth. Without the previous know-how on Bi device processing, the deposition of dielectric layers is a big technical challenge and a potential topic for future research.

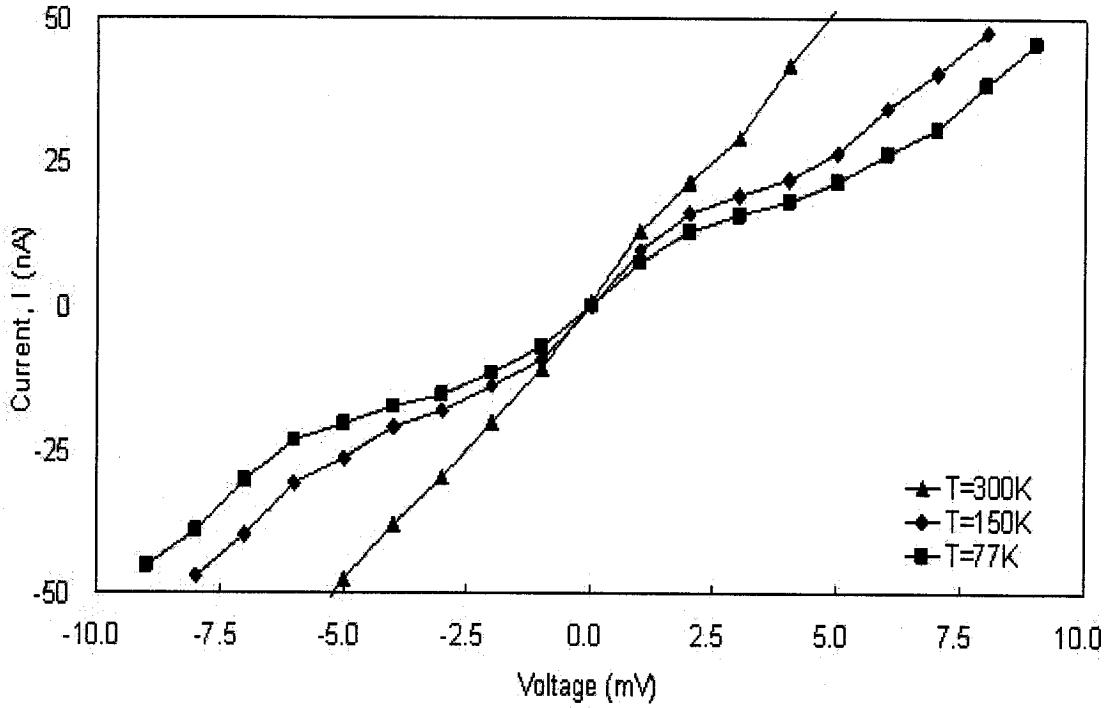

Figure 5.11: Current-voltage characteristics of Bi nanodot (S80-A2) at different temperatures, showing a strong non-linearity with step-like characteristic at both positive and negative bias voltages at temperatures below 150 K. Measurement error is 3%.

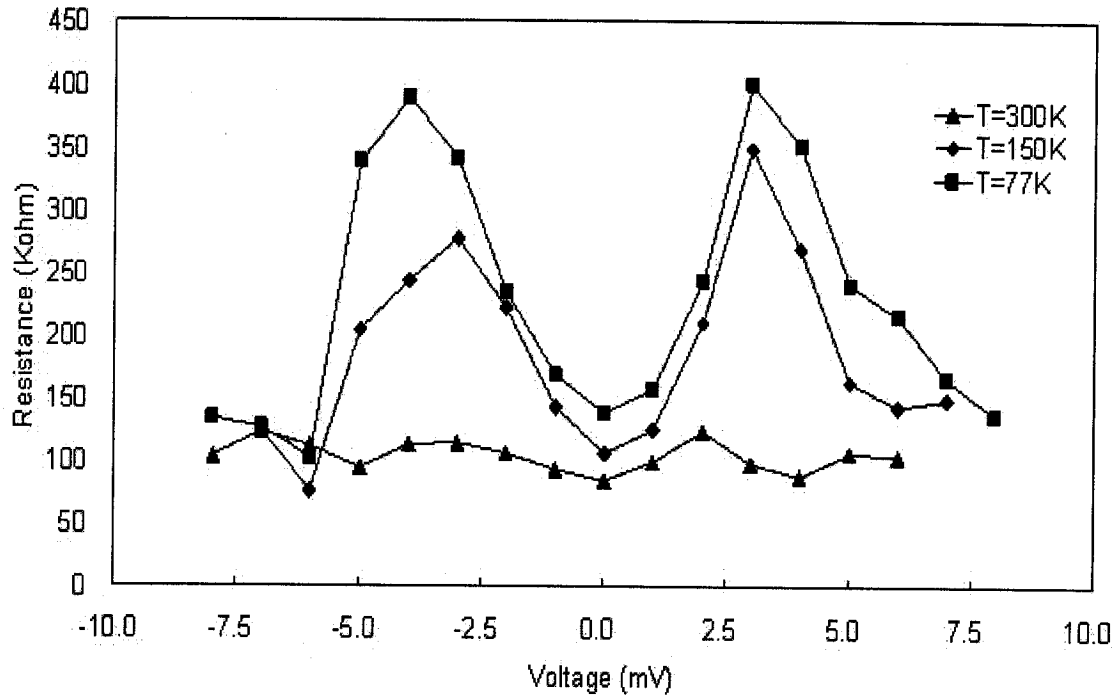

Figure 5.12: Resistance values of the nanodot structure (S80-A2) at different temperatures showing symmetric resistance peaks at ± 2.5 to 5.0 mV bias voltages. Energy level spacing in the Bi nanodot is evident. Measurement error is 3%.

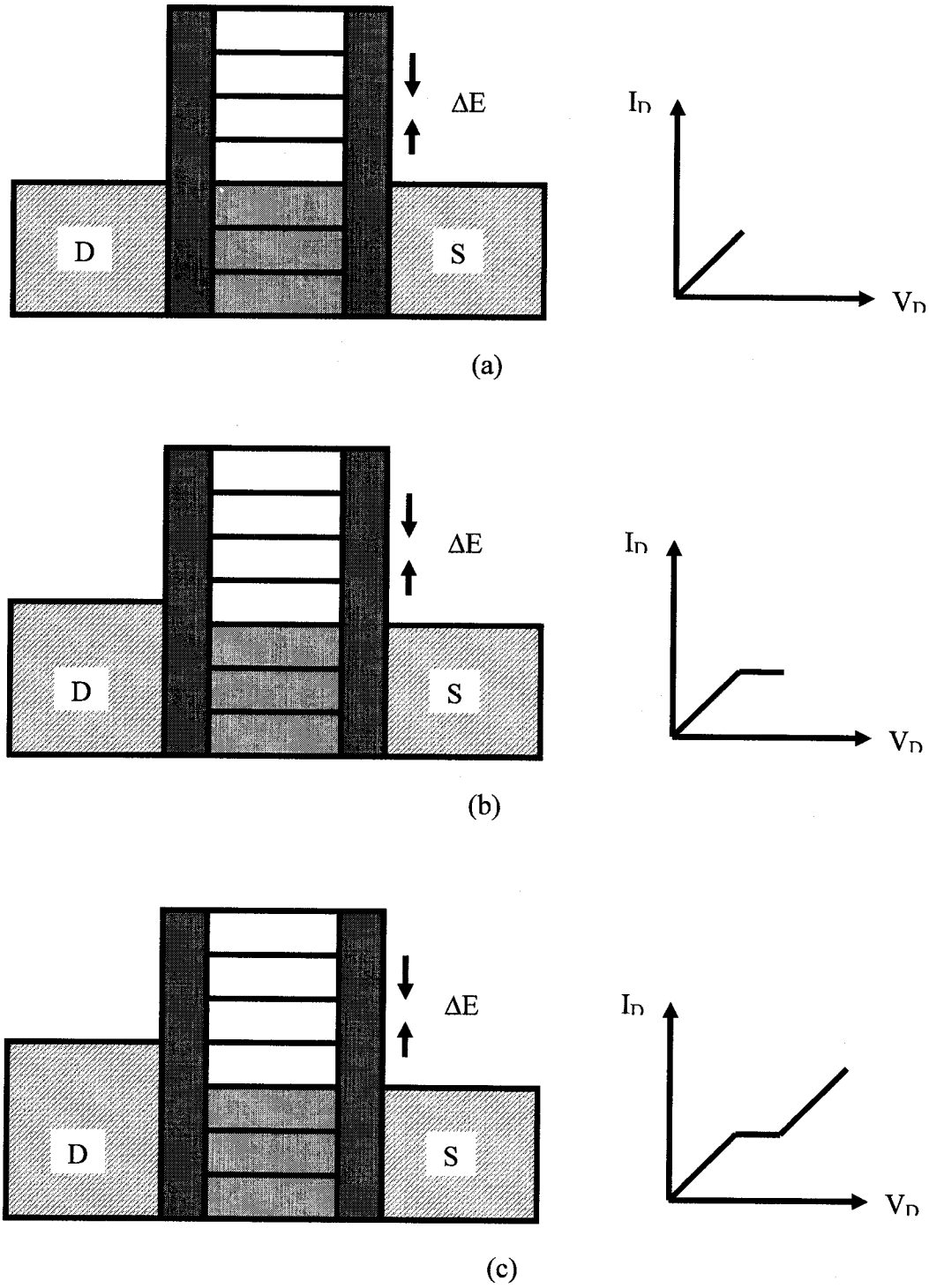

Figure 5.13: Energy level diagram and the corresponding I-V characteristic of a Bi nanodot structure. (a) V_D closes to Fermi level, I_D increases linearly; (b) $V_D < \Delta E$, I_D does not increase; (c) $V_D > \Delta E$, I_D increases again.

Table 5.3: Bi nanodot energy level spacing values obtained from different methods.

Measurement method	**Energy spacing value (mV)**
Best case theoretical value (Eq. 18)	75.2
Non-ideal case theoretical value (Eq. 18)	23.7
Measured value (raw data)	2.5
Measured value with 77 K thermal fluctuation compensation, k_BT.	15.8
Measured value with 150 K thermal fluctuation compensation, k_BT.	28.4

Table 5.4: Reported nanodot structures with staircase I-V characteristic.

Island material	**Island size (nm)**	**Measurement temperature (K)**
Ti [5.19]	100	4.2
Si [5.18]	100	6
Si [5.16]	40 – 190	15
Poly-Si [5.22]	39	35
Bi (present work)	100	77
Si [5.12]	30	300

Table 5.5: Capacitance values of different nanodot structures.

Structure	**Equation**	**Capacitance value (aF)**
Maximum size to observe coulomb blockage at T = 300K	$e^2/2C_{total} > 3.5kT$ [5.12]	< 0.88
Fabricated structure with 50 nm radius (assuming disk structure)	$C_{total} = 8 \varepsilon_r \varepsilon_o R$ [Eq. 16]	3.54
Fabricated structure with 50 nm radius (assuming sphere structure)	$C_{total} = 4\pi \varepsilon_r \varepsilon_o R$ [Eq. 17]	5.56

5.5 Chapter summary

In the phase three of the present thesis work, Bi nanodot structures have been studied in details. Bi nanodots with 100 nm-diameter and sub-nanometers tunneling electrodes were fabricated successfully using the proximity effect of e-beam writing. The challenges in fabricating the sub-nanometer tunneling contacts and nanodot structures have been overcome by carefully adjusting the process conditions and optimizing the electron dose in the e-beam writing process. From the measurement results, it is found that the current-voltage relationship of the nanodots was strongly nonlinear with step-like characteristic. Symmetric resistance peaks were observed at the same bias voltages at different temperatures. These resistance peaks were evidence of energy level spacing of the Bi nanodot that prevented electrons from tunneling. The successful observation of energy level spacing in a relativity large nanodot structure is due to the small electron effective mass of bismuth material. The small effective mass leads to measurable energy level spacing without the need to fabricate very small nanodot or significantly lower the operation temperature. Initial measured energy level spacing value (2.5 mV) did not match the best case theoretical value (75 mV). But by introducing the non-ideal case situation in the theoretical model and the thermal fluctuation compensation to the measured value, the theoretical value (23.7 mV) and the measured value (15.8 to 28.4 mV) converged to a matched level. The non-ideal theoretical model suggested that the crystal orientation in the bismuth nanodot is randomized and resulted in a larger overall effective mass (0.003175 m_e). On the other hand, the thermal fluctuation compensation in the measured value indicated the temperature sensitive nature of the nanodot devices. Unfortunately, Coulomb blockade was not observed in the

present structure due to the yet too large nanodot diameter. A smaller nanodot or different structure [5.19] is needed for realizing functional Bi SETs in our laboratories.

Although metallic Coulomb islands and SETs have been reported previously [5.19 -5.20], no study on fabricating or testing Bi nanodot structures has been found. Additionally, the non-linear I-V characteristic of Bi conduction islands has not been reported before at the time of thesis writing. It is believed that research results from the phase three of the thesis work are original and novel materials in the bismuth research community. A technical manuscript based on the research results obtained from this chapter has been published in the Applied Physics Letters [5.21].

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Chapter 6: Conclusions

The research of Bi nanoelectronic devices is a very interesting subject in the solid-state research community. Because of Bi material's unique properties such as small effective mass and long carrier mean free path, Bi devices have characteristics different from conventional semiconductor devices. One of the most interesting characteristics is the ability to create band gap when the device dimension is in the nanometer region. In this thesis, the author has exploited these special characteristics and studied different aspects of the non-classical electrical properties of bismuth based nanoelectronic devices. Bi devices with dimensions in the order of 100 nm were successfully fabricated in the EDM lab. at McGill University. Devices were realized by mastering the e-beam writing system and fine tuning the process conditions. Special physical effect such as proximity effect was utilized to form the sub-nanometer tunneling contacts. All the devices were designed for individual characterization. Three types of Bi nanoelectronic devices were studied, Bi nanowires, Bi nanowires with dual side-gate structures and Bi nanodot structures.

In the study of Bi nanowires, devices with rectangular cross-sections of different linewidths were fabricated. In this study, two nano scale phenomena were observed: metal-to-semiconductor transition and size effect. It was found that the conduction behavior of the device changed from metal to semiconductor when the critical dimension of the devices was reduced to below 50 nm. This change of conduction behavior is a solid experimental evidence of the quantum confinement-induced bandgap theory (Eq. 8). It was also found that the resistivity of Bi nanowire increased with the decrease in the linewidth. The one dimensional nanowire confined electrons and increased resistivity of

the devices due to the size effect. Different computational models of size effect such as Dingle model (Eq. 6 and 7) and MS model (Eq. 8 and 9) were adopted to compare with the measurement data. The MS model matched closely to the measurement data. The results obtained suggested that the scattering mechanism in the rectangular cross-section nanowires was mainly grain boundary scattering and the grain size was limited by the linewidth. Carriers had a 50% chance of being scattered at each grain boundary. It also confirmed the poly-grains nature of the evaporated films. The present work is the first complete study of the carrier transport mechanism of individual Bi nanowire fabricated with the presented method.

In the study of Bi nanowires with dual side-gate structures, external gate voltage was coupled into the nanowires in an attempt to modulate the I-V characteristics. Experimental results showed only 7% of current modulation. Numerical simulations on the electrostatic potential distribution of the device structures were performed to study the gate voltage coupling efficiency. The simulation results confirmed that the fabricated devices were effective structures. It is believed that the high carrier density of bismuth material is responsible for the inability to fully deplete free carriers in the nanowires by the external gate voltage, resulted in a small current modulation.

In the study of Bi nanodot structures, proximity effect of e-beam writing was utilized to form the 100 nm-diameter nanodots with sub-nanometer tunneling junctions. Significant non-linear I-V characteristic was observed at low temperature. The step like I-V characteristic is a strong indication of energy level spacing in the zero-dimensional (0D) nanodot structures. The initial measured energy level spacing value is 2.5 mV at 77 K. Considering the thermal fluctuation compensation, the energy level spacing value is 15.8 mV at 77 K and 28.4 mV at 150 K. These values matched to the non-ideal

theoretical value, 23.7 mV, which considered the non-ideal crystal alignment of the Bi nanodot structure. The successful observation of energy level spacing in a relatively large nanodot is due to the small effective mass of bismuth material which leads to a measurable energy level spacing. The non-linear I-V characteristic of Bi nanodot structure observed in this thesis work is the first reported energy level quantization led characteristic in the Bi devices research.

The main challenges in studying bismuth based nanoelectronics are the difficulty and lack of knowledge in bismuth based device processing. Bi based devices research is not a very popular topic in the solid-state device research community where silicon based technology dominates. Process technologies and experiences in fabricating such devices are not common. Deposition techniques on bismuth material are limited to basic evaporation or electroplating techniques. Furthermore, dielectric material of good quality that can be grown on bismuth film has not been reported. These constraints limit the research on novel Bi device structures. Even though with all these limitations, scientists continue to work on novel Bi devices in a slow but progressing pace. By accumulating small drops of experience, research on the Bi nanoelectronics can be advanced. The author hopes that results from this thesis can contribute to the Bi research community, and he hopes to see a functional Bi based logics in the foreseeable future.

6.1 Achievements

Research results obtained from this thesis have been published (or submitted) in two technical journals [3.24, 5.21]. Oral and poster presentations have been presented in several international and regional conferences [6.1–6.7]. Based on the research results of this thesis work, the author wishes to claim the following achievements:

I. The development of a process to fabricate Bi nanowires and Bi nanowires with dual side-gate structure using e-beam writing and thermal evaporation technique. The fabrication process has the ability to control the linewidth of the nanowire structure down to 70 nm and the thickness to 50 nm. It can also position individual device and facilitate direct individual device characterization without the need of additional chemical and/or physical etching processes.

II. First complete carrier transport mechanism study of individual Bi nanowire with a rectangular cross-section fabricated using the presented process (Point I). In this work, the author successful observed two nano scale related phenomena, size effect and metal-to-semiconductor transition, in Bi nanowires. The study revealed the carrier transport in the presented Bi nanowires is dominated by grain boundary scattering. The grain size is linewidth limited and carriers have a 50% scattering probability at each grain boundary. Part of the research results are published in the November issue of Nanotechnology Journal in 2004 [3.24].

III. The development of a process to fabricate Bi nanodot structures with sub-nanometer tunneling junctions using the proximately effect of e-beam writing technique and thermal evaporation technique. The fabricated tunneling junctions have an electrode-to-electrode spacing of less 5 nm. The invented nanodot structure

fabrication process provides a direct top-to-down approach to form nanodot structures with the flexibility to position devices at desired location.

IV. First observation of energy level quantization led non-linear current-voltage characteristic in Bi nanodot structures. The measurement result is supported by the energy level quantization theory [5.14]. A smaller than best case theoretical energy level spacing value is observed in the present work. It revealed the non-ideal crystal alignment of the fabricated bismuth nanodot structures and the temperature sensitive nature of the devices. The measurement result is justified by the non-ideal theoretical model and the temperature compensation model. Part of the work is published in the February issue of the Applied Physics Letters in 2006[5.21].

6.2 Future works

Bi based nanoelectronic devices research is an on going research topic. There are several aspects that the author would like to suggest for future works. As mentioned in the conclusions, Bi processing technology is not very common. Future works can be focused on the development of Bi based fabrication processes and materials. Recent advances in bismuth deposition by vapor/liquid phase injection to anodic alumina templates [1.16] is a good foundation in the development of single crystal Bi devices. Bi compatible dielectric materials and deposition methods are good topics for future research. In addition to the fabrication process, nano scale device structure is also an important topic. Because of the semiconductor conduction behavior of Bi material in nano scale, devices with novel nano structures could have interesting behavior. For Bi SETs, smaller island size always benefits the device performance. High resolution lithography systems such as field-emission SEM (FE-SEM) or atomic force microscope (AFM) can be used to reduce further the island size. Alternate SET structures such as serial islands formation can be attempted to improve the Coulomb blockade of the Bi SET without reducing the island size.

One of the most promising applications for Bi nanoelectronic devices is the memory application [5.13]. Nanodot device can provide a very high device density circuit [5.5] as compared to CMOS device. The total device area for a Bi nanodot is approximately 100 x 100 nm^2, while it is a few μm^2 for a CMOS device. In addition, the quantization of energy level in a Bi nanodot could be utilized to construct multi-value logic where one device can contain more than just 0 and 1 data. These advantages in Bi device could lead to a future Bi based high density memory application.

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Appendix A: List of acronyms

ACE	Acetone
AFM	Atomic force microscope
Au	Gold
Bi	Bismuth
CAD	Computer aided design
Cr	Chromium
E-beam writing	Electron beam writing
EDM Lab.	Electronic Devices and Materials Laboratory
FE	Field emission
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
Ge	Germanium
ICs	Integrated circuits
I-V	Current-voltage
Mo	Molybdenum
MOSFET	Metal oxide semiconductor field effect transistor
PECVD	Plasma enhanced chemical vapor deposition
RTD	Resonant tunneling diode
S/D	Source and drain
SED	Single electron device
SEM	Scanning electron microscope
SET	Single electron transistor
STM	Scanning tunneling microscpe
Si	Silicon
SOG	Spin on glass
SOI	Silicon on insulator
ULSI	Ultra-large-scale integration

Appendix B: List of symbols

a	Lattice constant
A	Cross-sectional area
C	Capacitance
C_{total}	Conduction island capacitance
d	Nanowire diameter
E	Energy
E_f	Fermi energy level
E_g	Energy bandgap
ΔE	Energy level spacing
$\hbar$	Planck's constant
I	Current
k	Carrier momentum
k_B	Boltzmann constant
l	Carrier mean free path
L	Confined dimensional length
L_D	Debye lenght
m_e	Electron mass
m_e*	Effective electron mass
m_h	Hole mass
m_h*	Effective hole mass
n	Density of free electrons
n_i	Intrinsic density
N	Energy state level
ρ	Resistivity
ρ_0	Intrinsic resistivity
P	Density of free hole
r	Radius
R	Resistance
R_e	Electron range
sp	Gate-to-wire spacing
q	Magnitude of electronic charge
T	Temperature
V	Voltage
∇	Gradient
ϵ	Dielectric constant
μ	Mobility
μ_{dot}	Electrostatic potential of nanodot

Appendix C: Physical constants

Angstrom unit	Å	$1 Å = 10^{-10} m$
Boltzmann constant	k_B	1.38066×10^{-23} J/K
Elementary charge	q	1.60218×10^{-19} C
Electron rest mass	me	0.91095×10^{-30} kg
Electron volt	eV	$1eV = 1.60218 \times 10^{-19}$ J
Permittivity in vacuum	ϵ_o	8.85418×10^{-14} F/cm
Planck's constant	$\hbar$	1.05458×10^{-34} J-s