ANALOG-DIGITAL CONVERTER : STRIP CHART TO PUNCHED CARD

Joseph E. Michalski, B.Eng.

ANALOG-DIGITAL CONVERTER : STRIP CHART TO PUNCHED CARD

Electrical Joseph E. Michalski, B.Eng. M.Eng.

ABSTRACT

An interface between a graphical-to-digital converter and a standard I B M keypunch machine is developed. Inputs to the converter consist of strip-chart recordings. An optical scanning technique is employed to convert the analogue information into a series of pulse trains. Graphical data, transformed in this manner is then processed by a logic unit contained within the interface and subsequently transcribed onto data cards. The overall procedure is completely automatic.

Inherent in any optical digitization scheme are errors, caused in part by the inability of the system to discriminate between lines which form the actual analog information and noise. In this case noise is attributed to the optical scanning mechanism, to the presence of grid lines, dirt or other spurious markings on a chart recording, and to the texture of the recording paper.

To reduce the errors introduced by the scanning mechanism the system optics were improved. This significantly enhanced the accuracy of digitization.

Normally, little or no control may be had over errors caused by the quality of recording paper. Therefore, additional logic circuitry, incorporated within the interface transcribes, upon detecting such errors, appropriate error codes onto the data cards.

ANALOG-DIGITAL CONVERTER : STRIP CHART TO PUNCHED CARD

by

Joseph E. Michalski, B.Eng.

Department of Electrical Engineering

McGill University,
Montreal, Canada.

July, 1971.

ANALOG-DIGITAL CONVERTER : STRIP CHART TO PUNCHED CARD

by

Joseph E. Michalski, B.Eng.

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Engineering.

Department of Electrical Engineering,
McGill University,
Montreal, Canada.

July, 1971.

ABSTRACT

An interface between a graphical-to-digital converter and a standard I B M keypunch machine is developed. Inputs to the converter consist of strip-chart recordings. An optical scanning technique is employed to convert the analogue information into a series of pulse trains. Graphical data, transformed in this manner is then processed by a logic unit contained within the interface and subsequently transcribed onto data cards. The overall procedure is completely automatic.

Inherent in any optical digitization scheme are errors, caused in part by the inability of the system to discriminate between lines which form the actual analog information and noise. In this case noise is attributed to the optical scanning mechanism, to the presence of grid lines, dirt or other spurious markings on a chart recording, and to the texture of the recording paper.

To reduce the errors introduced by the scanning mechanism the system optics were improved. This significantly enhanced the accuracy of digitization.

Normally, little or no control may be had over errors caused by the quality of recording paper. Therefore, additional logic circuitry, incorporated within the interface transcribes, upon detecting such errors, appropriate error codes onto the data cards.

ACKNOWLEDGEMENTS

The author would like to express his very sincere appreciation to Dr. G.L. d'Ombrain, who supervised the research, for his guidance and encouragement, and to Mrs. P. Hyland, for her aid in the preparation of this thesis. Thanks are also due to the technical staff of the Electrical Engineering Department. The author also wishes to express his gratitude for the financial assistance provided by the National Research Council.

TABLE OF CONTENTS

CHAPTER I

INTRODUCTION

1.1 General Background

The relative availability of digital computers is imposing new and increasingly varied demands on the concept of the man-machine interface. An important aim - that of direct audio/visual communication with a computer shows great promise, owing to recent developments in the field of Pattern Recognition.

A device, enabling analog information pre-recorded on strip charts to be automatically digitized and stored in a form suitable for direct entry into a computer has many applications. Research in the areas of Medicine, Process Control, Pattern Recognition, etc., yields experimental results which in many cases are most conveniently displayed by conventional recorder techniques. More often than not the data requires additional analysis best carried out by a digital computer. To digitize graphical information manually is tedious and time-consuming. Semi-automatic digitizers are available commercially [1], [2], [3]. Their initial cost is typically $25,000. To digitize a graph requires an operator who manually aligns a cursor over the graph. The displacement of the cursor represents the value of the ordinate. The ordinate and abscissa are then recorded and the abscissa is advanced one unit. The digitized data is recorded on data cards, magnetic tape, disks, or paper tape.

In order to realize a fully automatic graph reading process two graphical - to - digital converters were developed, for comparison purposes at McGill University - one by C. Rosza and G.L. d'Ombrain [4], the other by L.A. Cox and G.L. d'Ombrain [5].

The first graph reader is based on an electro-mechanical scanning principle. Briefly, this consists of a small spot of light traversing a sample of graph paper. The amount of light reflected from the paper is detected by a photomultiplier tube. A "video" pulse is electronically derived from the output of the photomultiplier whenever the scanning spot crosses a line on the paper. The video output is gated with "marker" pulses and stored on magnetic tape. The frequency of the marker pulses is such that the occurrence of each successive marker pulse represents a 0.01 inch movement of the scanning spot along the paper. At the end of a scan the graph is automatically advanced by one millimeter and another scan then takes place. Once an entire graph has been read and stored in this manner, an intermediate stage of data processing is then necessary. The format of the graphical information stored on magnetic tape is such that it is not as yet suitable for direct entry to a digital computer. The original tape is therefore processed at a computing center to produce a new tape. A computer program is then used, together with the new tape to obtain the abscissa and ordinate values of the graph stored therein. To do this, the computer counts the number of marker pulses which occur on tape from the point where the light spot first "hits" the graph paper up to the occurrence of a video pulse. To account for the finite width of the graph line the number of marker pulses occurring in coincidence with a video pulse is halved. The abscissa is obtained by simply maintaining a count of the number of scans recorded on the tape, as each scan is processed by the computer.

The second graph reader employs a closed-circuit television camera. A graph is scanned by the camera and the image stored on the camera tube. A magnetic tape transport is then started and the stored image is scanned by the camera deflection circuits. Associated pulse circuitry produces three output signal levels, corresponding to white, grey and black and writes in appropriate code onto tracks of the tape. The white and grey levels represent blank paper and graph lines respectively, whereas the black level represents three small black dots drawn at the origin and X and Y axes of a graph. The dots are used to correct for any misalignment of a graph with respect to the axis of the camera. The graph remains fixed throughout the entire scanning process. When the whole graph has been read the procedure is then somewhat similar to that outlined above for the electromechanical reader, where a new tape is processed and the abscissa and ordinate values then determined through a computer program. The Y amplitude is obtained by counting the pulses from the tape unit write pulse generator which are gated by camera tube generated pulses. The X amplitude is determined as before. In addition, the computer program corrects for misalignment of the graph with respect to the camera's coordinate system and non-linearities introduced by the camera tube and associated deflection coils, circuits, etc.

Common to both readers described above is the fact that graphical information, by undergoing a digitizing process, assumes the form of pulses and is stored as such on magnetic tape. The tape then requires two stages of manipulation at a computer center whereby are ultimately determined the X and Y values of a graph. From several viewpoints this procedure is inconvenient. Any data reduction process

which entails several stages of manipulation at a computer center inevitably falls, in a sense, into the throes of a self-imposed bureaucracy. Furthermore the initial step - that of writing on magnetic tape does not provide a researcher with an accurate "instant replay" of stored information. Only a fractional check may be had by monitoring with an oscilloscope the tape tracks containing graphical data.

There are several ways whereby the short-comings inherent in the present arrangement can be eliminated. The ideal procedure would be to :

(i) do away with the necessity for intermediate processing of graphical data after it is digitized and stored, and

(ii) to store the digitized data in a manner which would permit an immediate and direct access to it.

The solution to (i) is to replace software - consisting of computer programs by a hardware logic unit. The inputs to the logic unit would consist of the pulses which emanate from the graphical - to - digital conversion process while a graph is being read. The logic unit would then manipulate this digitized information to the extent that at the output terminals of this unit would be accessible the X and Y values of a graph presently obtainable only through the use of a computer.

To satisfy (ii) requires a storage medium other than magnetic tape. No doubt magnetic tape is preferable where speed and density requirements are mandatory however, it is felt that these are of secondary importance here. A reasonable sub-

stitute for magnetic tape is the punched data card. A way of incorporating data cards into the present scheme is to link a standard keypunch machine to the output of the logic unit proposed above. As a result the coordinate values may be punched onto cards as a graph is being digitized, thereby offering a comparatively instantaneous display of digitized information. There are several advantages to using data cards. Once data is transcribed onto cards any subsequent need to refer to a graph is made rapidly and without the use of additional equipment. Furthermore, the use of data cards as computer input is virtually universal and unless utterly destroyed their duplication is but a simple matter.

An important aim of this thesis is to interface one of the graphical - to - digital converters described earlier with a keypunch machine. In the next section reasons are given why one of the converters is more suitable for this purpose.

1.2 The Adaptability of the Graphical-to-Digital Converters to a Keypunch Machine

In the previous section a brief description of two graphical-to-digital converters was given. The concluding remarks inferred that it would be more convenient to transcribe graphical information directly onto data cards. The ensuing discussion begins by defining the basic properties native to any graph reader. The two graph readers are compared in terms of these properties. The complexity of the logic unit required to interface either of the readers with a keypunch machine is also

studied. The discussion culminates with the selection of the graph reader which can more readily be interfaced with a standard keypunch machine.

Several characteristics intimate the usefulness of a graph-reading device - resolution, sensitivity and accuracy being perhaps the more significant ones. Resolution is defined here as the thinnest graph line which may be read. The resolution of the electromechanical reader is in the order of 0.01 inch, as compared with 0.02 inch for the vidicon reader. Sensitivity refers to the detection process whereby is sensed a line on a graph. A graph line having a thickness satisfying the resolution may not be detected if the line itself is too faint. The governing factor with regard to sensitivity is the signal-to-noise ratio of the detection process. Of the two machines the electromechanical reader has the better signal-to-noise ratio.

To evaluate the accuracy of the electromechanical reader a statistical analysis of data digitized thereby was carried out. It was found that 94 % of the digitized data fell to within 0.25 % of the actual plotted graph [4]. No statistical analysis was carried out for the vidicon reader. The accuracy of the two readers was therefore compared on a visual basis. In order to do this a graph was digitized by each of the graph readers. The digitized data thus obtained was then replotted on the original graph. For the electromechanical reader, by superimposing the two graphs it was not possible to observe any difference between the original and the reproduction [4]. On the other hand noticeable discrepancies were evident in the results obtained in this manner by means of the vidicon reader [5].

In addition to those mentioned above two more characteristics are worthwhile comparing here - input format and digitization speed. The electro-mechanical reader accepts strip chart recordings of the hot-stylus Sanborn type, up to 6.1 inches in width and up to 60 feet in length. The vidicon device is limited to graphs up to 8 1/2" x 11". On a per-foot basis, the digitization speed is in the order of 20 seconds for both machines.

Thus far the comparison of the two readers indicates that the electromechanical one is, in terms of the characteristics listed above, the better of the two. However, before arriving at a decision as to which reader is in every respect more conveniently adaptable to a keypunch machine one more point need be considered : the complexity of the logic unit necessary in order to interface the reader with the keypunch. As mentioned earlier it is intended to accomplish this interface in such a way as to eliminate the intermediate processing of digitized graphical data. Understandably the complexity of the logic unit will be proportional to the complexity of the computer programs which at present form part of this processing stage. Although the computer programs associated with both readers are essentially similar, in that each involves a counting of "marker" pulses in the determination of the ordinate value, the vidicon program is, for two reasons more complex. This increased complexity is due to the fact that the vidicon program has to correct for the possible misalignment of a graph with respect to the camera's coordinate system and for non-linearities introduced by the camera tube and associated deflection coils, circuits, etc.

On the basis of the arguments presented above it was decided to interface the electromechanical graph reader with a keypunch machine, for not only is this system superior to the vidicon reader in terms of resolution, sensitivity and accuracy, but also in the amount of logical hardware necessary to realize the interface.

1.3 Statement of the Problem

The primary aim of this project then is to interface the electromechanical graph reader with an IBM keypunch machine. This involves the design and construction of a digital control system by means of which graphical information, upon being digitized is punched directly onto data cards. The punched data should be such that it requires no subsequent manipulation - in the form of correction factors, etc.

In the present work the number of lines on a graph is constrained to two, where one line is assumed to be a base or reference line. Similar logic could be developed to read graphs containing more than two lines.

The logic unit should contain an error detection scheme. Briefly, this means that if during a scan a graph line is not detected by the graph reader an appropriate error code should be punched out on the data card. Alternately, if more than the allowable number (2) of lines is detected another error code is to be punched out.

A test circuit, together with a visual display unit is to be built and used as an aid in diagnosing possible faults within the logic unit. The advantage of the test circuit is that it would enable the logic to be checked independently - without the graph - reading unit.

The external controls to the overall system (graph reader and logic unit combined) should be minimal. In this way very little prior experience would be necessary to operate the system.

The optics of the graph reader are to be investigated, with the aim of improving the signal-to-noise ratio (SNR) of the graphical detection process. With an improved SNR it would be possible for the graph reader to :

(i) consistently detect thinner and fainter graph lines on high-reflectivity recording paper,

(ii) consistently detect graph lines on a paper having low reflectivity and poor contrast .

The resolution of 0.01 inch native to the electromechanical reader is to be retained in the proposed system. It is hoped that the full-scale accuracy of ± 0.25 % will also be retained.

CHAPTER II

ELECTROMECHANICAL GRAPHICAL-TO-DIGITAL CONVERTER

2.1 Introduction

In Chapter I it is mentioned that graphical information, by undergoing a process of conversion assumes the form of pulses. The ensuing discussion describes this process as it occurs in the electromechanical converter.

The converter, depicting its present form (solid lines) and proposed additions (dotted lines) is shown in Figure 2.1.1. The converter outputs - three distinct pulse trains are derived as follows :

(i) Video Pulses

A drum (1) on which is cut a spiral slit (2) is rotated at approximately 790 RPM by a motor (3). A light source (a high-pressure mercury arc lamp) (4) is located inside the drum. Light emerging from the spiral slit impinges on a stationary slit (5) parallel to the drum axis. The resulting light spot scans a graph (6). Reflected light - decreased in intensity whenever the spot traverses a graph line is detected by (7) a photomultiplier tube. The output of the photomultiplier is first pre-amplified and then amplified non-linearly yielding as a result the video pulses.

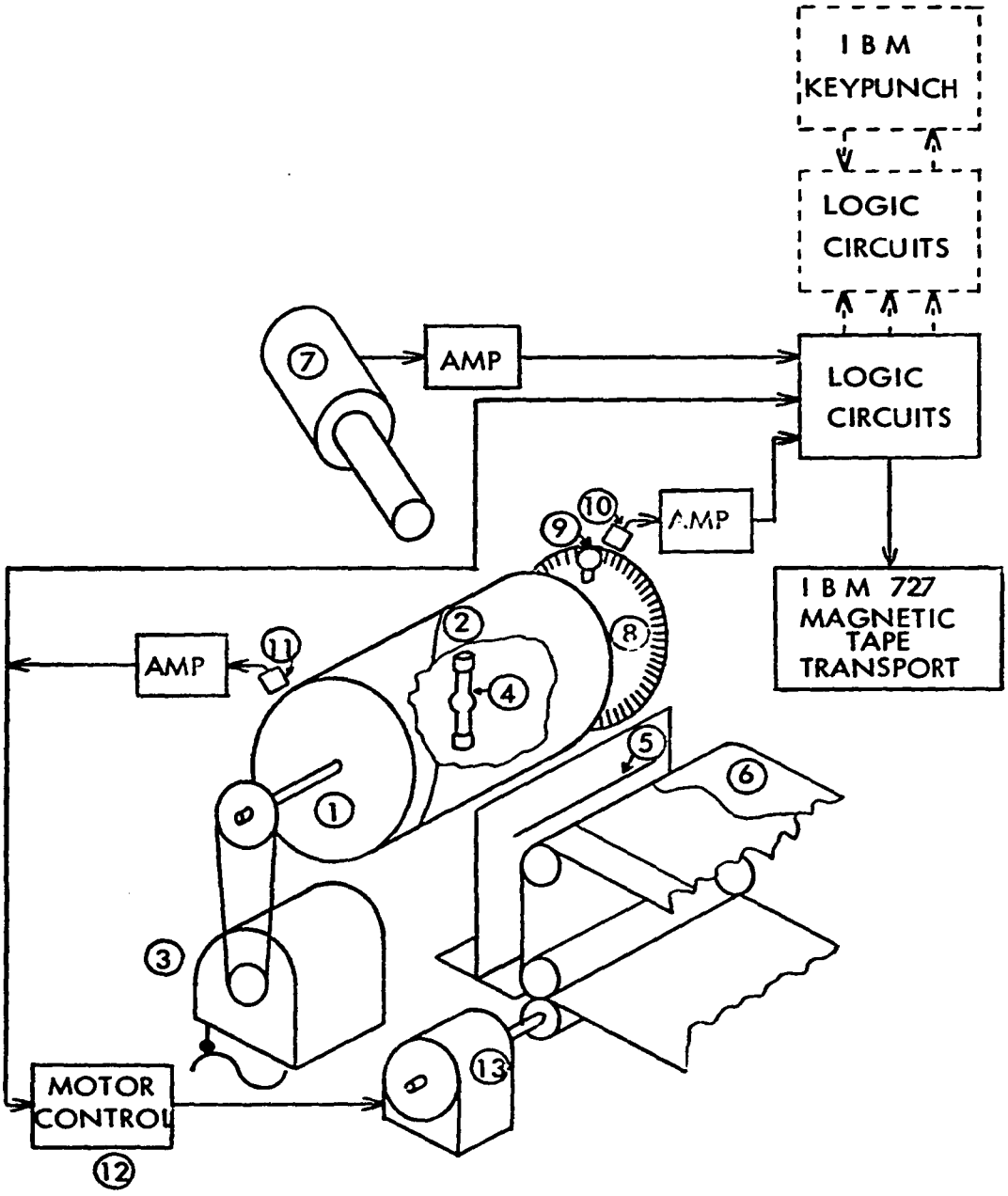


FIGURE 2.1.1. ELECTROMECHANICAL GRAPHICAL-TO-DIGITAL CONVERTER.

(ii) Marker Pulses

A plastic disc (8) coupled to the drum shaft contains 740 equally spaced marks. A light source (9) is interrupted by these marks and the resulting "modulated" light is then sensed by a phototransistor (10). The phototransistor output undergoes amplification and waveshaping which produces pulses occurring at a frequency of 9743 HZ. These are subsequently used to calibrate the y axis of a graph in increments of 0.01 inch.

(iii) End of Scan Pulses

Another phototransistor (11) detects light from an orifice in the circumference of the drum. Its output is subject to amplification and waveshaping - producing a pulse for each revolution of the drum. This "end of scan"pulse is used to trigger the control circuit (12) of a stepping motor (13) so that each revolution of the drum enables a graph to advance by one millimeter in the X direction. This arrangement provides a perfect zero-order hold sampling technique [4].

2.2 The I B M Keypunch Machine - General Information

An I B M Keypunch Machine is normally used to transcribe numerical and/or alphabetical information onto I B M data cards. The machine, consisting in part of a standard alpha-numeric keyboard may also be set to operate under "program control" by affixing a coded I B M card onto a "program" drum. In simple applications, for example the punching of numerical data cards, a program control is not necessary. In this latter mode depressing an alpha/numeric key on the keyboard effectively closes a contact or combination of contacts. Closure of a contact (s) initiates a "punch cycle". The duration of this cycle is 100 milliseconds for an I B M type 26 keypunch [6] and 56 milliseconds for a newer model - the I B M 29 [7]. It is during the punch cycle that a hole is punched in one column of a card.

The fact that a punch cycle is initiated by closing (a) contact (s) is significant here. If, for example the number 26 is to be automatically punched on a card, this could be done by simply placing in sequence a short circuit (by means of a relay contact) across the contact (s) which ordinarily would be closed upon depressing the numeric 2 and 6 keys respectively.

When the last column (80) of a card has been punched a new card is fed and registered into place. If the AUTO-FEED (Automatic-Feed) switch of the keypunch is ON, a new card is automatically fed and registered. The total time elapsed during this feed and register cycle is about 250 milliseconds.

A card-feed cycle may be detected by monitoring the status of a contact within the keypunch. A closed contact indicates that the machine is in a feed cycle. The reason for detecting this cycle is explained in Chapter III.

2.3 Graphical Converter-to-Keypunch Interface - General Considerations

In the following discussion it is shown how the pulses described in Section 2.1 may effectively be used to interface the electromechanical graphical-to-digital converter with an I B M keypunch machine.

The manner in which the ordinate value of a graph may be determined is illustrated with the aid of Figures 2.3.1 (a) through (e). In Figure 2.3.1 (a) is drawn a sample of graph paper containing two lines. The waveforms of Figures 2.3.1 (b), (c) and (e) depict the video, marker and end of scan pulses corresponding to a single scan of the graph. Recall that the frequency of the marker pulses is such that the distance between each successive marker pulse is equivalent to an interval of 0.01 inch along a graph. To obtain the value of the ordinate (Y in Figure 2.3.1 (a)) waveforms (b) and (c) are combined in such a way as to yield waveform (d). The pulses of waveform (d) are fed to a binary-coded-decimal (BCD) counter. The counter is initially reset to zero, prior to the occurrence of waveform (d). Each of the pulses occurring in waveform (d) is then counted. At the negative-going edge of the second video pulse the counter therefore contains, in hundredths of an inch the distance between the mid-points of two successive graph lines.

The example shown above is a relatively simple one, where the number of marker pulses coincident with each video pulse is even (2) and equal. In this case, wherever coincidence occurs the frequency of the marker pulses is halved prior to being counted. Each marker pulse occurring between video pulses increases the counter

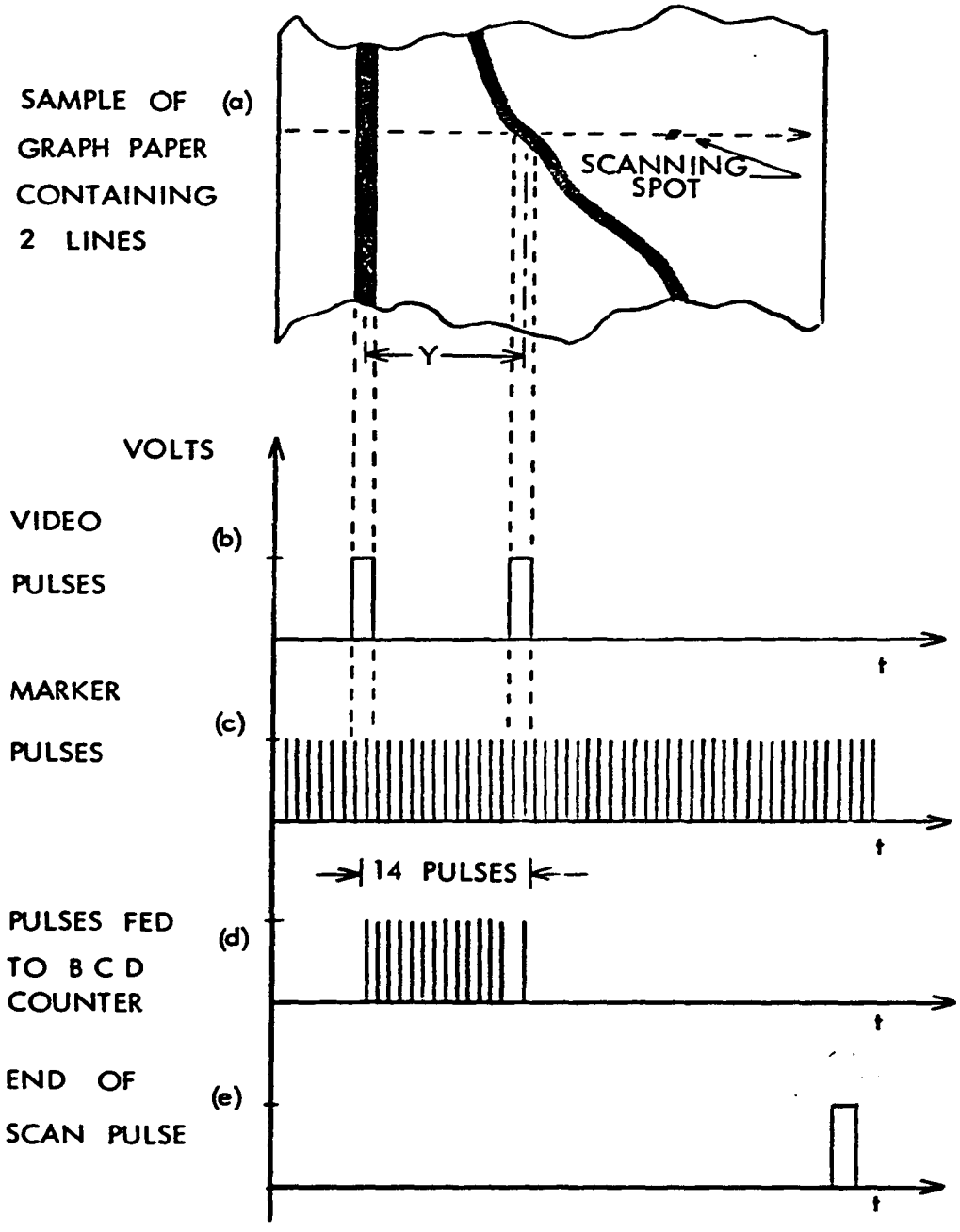


FIGURE 2.3.1. DETERMINATION OF THE ORDINATE (Y) VALUE OF A GRAPH.

content by one. For the sample of Figure 2.3.1 (a) the counter would contain the number 0.140 at the end of a scan. Situations will of course arise where the number of marker pulses coincident with the video pulses may be an odd-even, even-odd, or odd-odd combination. The solution of this problem is relegated to Chapter III.

Recall that the end of scan pulse, occurring once for every revolution of the converter drum is used to actuate a stepping motor - advancing in turn a sample of graph paper by one millimeter at the end of each scan. For the present purposes, it is intended that this pulse perform two functions :

(i) Advance a sample of graph paper by some preset increment (1 to 9 millimeters) - the size of the increment being left to the discretion of the operator.

(ii) Serve as a source of alternately occurring punch and shift pulses.

These functions may best be described by briefly summarizing one cycle of the digitization process. This consists of :

1. The stepping motor advancing the graph paper by a preset amount. The stepping motor drive pulses are fed also to a binary-coded-decimal counter. In this way a record of the number of abscissa increments, and hence the X value of a graph, is retained.

2. A graph is then scanned once and the ordinate value obtained as outlined previously.

3. At the termination of a scan the contents of the two counters (abscissa, or present X value and ordinate, or present Y value respectively) are shifted into a temporary memory - a parallel-in, serial-out register. Within the register the graphical data is stored in binary-coded-decimal form.

4. The digitization process then enters its final phase, during which the graphical data stored in the register is punched out on a data card. To illustrate this let us assume that after a particular scan the register contains the numbers 13425870. This means that X = 1342 millimeters and Y = 5.870 inches.

The outputs of the four flip-flops which contain the most significant value of X in binary-coded-decimal form are inputs to a binary-coded-decimal-to-decimal decoder. Each of the decoder outputs serves as an input to one of ten logical AND gates. The other input to each AND gate is a PUNCH pulse. The output of each AND gate is connected to a relay coil. Each normally-open contact of the ten relay coils parallels a keypunch machine contact which ordinarily would close when a numeric key is depressed. In the example cited above the most significant value of

X is 1. This means that line 1 of the ten (0 to 9) decoder outputs is enabled. When a PUNCH pulse occurs AND gate 1 energizes relay 1 and the contact of this relay closes, initiating in turn a punch cycle within the keypunch. During this cycle the digit 1 is punched in a column of a data card. When the punch cycle terminates a SERIAL SHIFT pulse occurs. This pulse shifts the data within the register to the left so that the digit 3 in the example now occupies the position which the digit 1 occupied prior to the occurrence of the shift pulse. Another PUNCH pulse then occurs and the digit 3 is punched in the next column of the data card. In this way eight PUNCH pulses and seven SERIAL SHIFT pulses are required to punch out the eight digits stored in the register. Both the PUNCH and the SERIAL SHIFT pulses are derived from the END OF SCAN pulses.

The format of the digitized data punched out on cards is fixed. Each set of coordinate values occupies 8 columns (4 for X and 4 for Y) of a standard I B M data card. In this way each card contains ten sets of X and Y values.

CHAPTER III

LOGIC CIRCUITS

3.1 General Considerations

The previous chapters, introductory in nature presented a broad picture of two independent, non-interacting machines. The latter part of Chapter II outlined a scheme whereby the two machines, acting jointly, transfer graphical information onto data cards. It is intended presently to describe the interface circuitry required to link the Graphical to Digital Converter with the IBM keypunch machine.

The output of the graph reader, consisting of three distinct pulse trains implies that the interface circuitry is digital. Furthermore, it is subsequently shown that it consists of basic units intrinsic in any digital computer : memory, counters and control unit.

Selection of "hardware" for this work was dictated by perhaps four main considerations : reliability, economy, limitations of space, and availability. The first three, being engineering generalizations are in this case synonymous with such terms as switching speed,noise immunity, logic (voltage, current) levels, fan in / fan out capabilities, power dissipation, packaging, temperature dependence, etc.

The decision to employ digital integrated circuits as fundamental logic blocks in the interface was based in part on a study of specification notes issued by Texas Instruments Incorporated - then prime manufacturer of these devices. The apparent facility in adapting them to the work far outweighed a lack of application data avail-

able at the time. Understandably, with the increasing trend of late towards integrated electronics, much has been published to remedy this latter situation.

3.2 Theory

3.2.1 A Pertinent Survey of Recent Switching Theory

The development of digital integrated circuitry has had a significant impact on the field of switching theory. The typical NAND / NOR structure of combinational (gates) hardware, be it discrete (transistorized) or integrated, along with the variety and compactness of integrated memory devices (Delay, Set - Reset, Trigger and J - K Flip-Flops) available for sequential circuits have allowed novel approaches to logical design. The basic aim nevertheless is still minimization.

In sequential circuits the problem is two-fold and interacting : minimization of memory elements and of combinational elements. The classical approach however, that of essentially resolving a sequential machine to the extent where combinational techniques may be utilized is still prevalent. First introduced by Huffman [8] as a systematic means of realizing asynchronous sequential machines using relays, the theory was then extended by Mealy [9] to include synchronous circuits.

To minimize a synchronous machine, the major problem is that of assigning an optimal binary variable code to the internal states (memory elements) of the machine. In the last decade a few significant contributions have been made - notably by Hartmanis and Stearns [10], [11]. Proposing a state assignment whereby

"next states", $X_{t_{n+1}}$, $Y_{t_{n+1}}$, ... etc. for example, are least dependent on present internal states X_{t_n} , Y_{t_n} , ... of a machine, it was shown that a good assignment could be achieved. To select such an assignment, the algebra of Partitions was applied. Proceeding on the same criterion Dolotta and McCluskey [12] introduced a systematic method. While differing from Hartmanis and Stearns in the manner whereby a good code may be realized, their technique yielded "encodings which are as good as, and often better than, those obtained by experienced logical designers". An algorithm of Weiner and Smith [13] assigns, by a partition approach "the input, state and output symbols of a given machine so as to minimize the total logic, i.e. reduced dependencies of both state and input variables are optimized". Significantly, their method yields an optimal assignment in one iteration.

A definite drawback in the aforementioned work([9] to [13]) is the constraint that all memory elements be delay (D) flip-flops. This means that once a state assignment is made, the combinational flip-flop input equations derived therefrom correspond to delay elements. Humphrey, in his text [14] presents an extension to Mealy's theory. By rigorously following Mealy in the formulation of a state diagram and transition table [9] , he illustrates a technique whereby flip-flop input equations may be derived. Although he restricts himself to S - R flip-flops the procedure is nevertheless valid for other memories [14] (D, T, J - K). Briefly, it involves the fabrication, from a state assignment of a set of Karnaugh maps. In this case, two maps are required per flip-flop - one for the Set, the other for the Reset input. The maps are then factored, yielding the required equations. The output expression(s) is (are)

similarly derived. Again, the selection of the state assignment determines the "degree" of optimality of the combinational circuitry, for in no way does this method ensure unique minimal logic functions [14]. As an aid in "converging" sensibly to a good state assignment, Humphrey indirectly applies the next state independency principle [10], [11]. Work by Curtis [15], part of which has recently been published apparently promises to resolve this latter difficulty. Curtis generalizes the methods of Dolotta and McCluskey, and Weiner and Smith. He then obtains directly good realization of sequential machines using, for example Trigger (T) Flip-Flop memory or even a combination of T and S - R, or T and J - K elements.

In 1963 Todd [16] prepared a bibliography consisting of 63 references to papers dealing with NAND - NOR combinational theory. Since then very much more has been published on the topic.

Earle [17] presented a technique of factoring a combinational switching function on a Karnaugh map which yields the same expression in minimal Stroke (NAND) or Dagger (NOR) "form". This does not necessarily lead to a minimal NAND or NOR gate realization of a given function. This together with additional work [18] culminated in a text by Maley and Earle [19].

In marked contrast to Earle's work, recent contributions on the subject are very algorithmic in nature and geared primarily for a computer. Most of the algorithms are similar in principle. Based on a minimal cost criterion, where cost most frequently infers some combination (linear [20], for example) of gates and gate inputs, any combinational switching function may optimally be synthesized by means of NAND

or NOR elements. Constraints are incorporated and usually consist of restrictions on fan-in, fan-out and the number of gating levels. Some of the algorithms include the case of multiple outputs [20], [21].

A conceivable parallel exists in the development of NAND - NOR combinational theory when compared with sequential machine theory. Both areas indicate a trend towards an algorithmic, computer - oriented design approach. As a result, the logic designer is less and less frequently asked to rely upon his intuition. Davidson [20] states with some uncertainty that "the apparently nonintuitive nature of NAND logic design to the human designer makes an algorithmic approach to design imperative" - he may be right. The selection by known techniques of a good state assignment in sequential machine design is seemingly even less intuitive.

3.2.2 Design Philosophy of the Interface Logic Circuitry

On a chronological basis, the widespread use of digital integrated circuits occurred before the terms optimal or minimal as applied to pertinent design theory held any direct practical significance. When confronted with a sequential machine of reasonable complexity the designer usually resolved the machine into a set of smaller, more expedient machines. The procedure then was to minimize each of these with the hope that the entire machine would approach optimality. It is upon this premise that the interface circuitry in the present work was built. Even by present day design standards this is the most realistic technique.

More often than not a digital machine is in its final test stages when changes, - perhaps in the form of additional logic, need to be implemented. If the original machine is truly optimal it is highly unlikely that optimality is then retained, unless the machine is redesigned in its entirety.

With reference to the present work, it was convenient to subdivide the machine into three sections, consisting of a control unit, counters and a register. A further subdivision was then made, resulting in a decomposition of the control unit into three subsections, namely Controls A, B and C. "Partitioning" the machine in this manner simplified its overall structure considerably.

To adopt the algorithm of Dolotta and McCluskey [12] as a design vehicle at this stage was considered impractical. Aside from the restrictive and non-optimal nature of their technique the overall effort of programming it for a computer was deemed unrealistic. Furthermore, the logic unit, if viewed from its proper perspective formed but part of the graphical-to-digital conversion process described earlier. Of paramount importance then, was that a working model of the overall system be implemented. To accomplish this within a reasonable span of time a primarily intuitive approach to logical design was adopted. In specific instances, for example "Control B" and in the design of the binary-coded-decimal (BCD) counters the direct extension to Mealy's theory [14] was applied. One advantage of this method was that it offered the possibility of reasonably good sequential machine realization by longhand "computation". Comparatively, the algorithm of Dolotta and McCluskey proved far too cumbersome when applied manually to a 5 - state machine.

To implement minimally combinational switching functions by means of NAND gates, the catalog of three-variable NAND logic circuits compiled by Hellerman [22] proved quite useful, as did the techniques of Maley and Earle [17], [18], [19].

In practice a minimal logic structure is not always desirable from a reliability viewpoint. Examples of this, together with methods used to circumvent such implied "hazards" are relegated to Sections 3.4.2 et seq.

3.3 Hardware

3.3.1 Layout of the Logic Circuitry

The interface circuitry is almost exclusively comprised of the Texas Instruments 74 N series type of digital integrated modules. This series consists of general purpose Transistor - Transistor logic (TTL) circuits mounted within 14 or 16 pin plastic packages. In several instances, such as translation of voltage (logic) levels, driver stages and other "special" circuitry, these devices are supplemented by discrete resistor - transistor components.

The logic is contained on eighteen rack - mounted veroboards. Fourteen and sixteen pin sockets, when affixed to the boards permit rapid insertion and removal of integrated devices and eliminate any possibility of heat damage to them when solder connections are made. Discrete circuitry is also mounted in veroboards. Wherever possible, interconnections are made by means of the 106 mil copper strips on the

boards or otherwise teflon - insulated wire. To ensure reliable operation of the logic circuits special wiring techniques are suggested in Applications Manuals [23], [24], [25].

Pictures P 3 - 1 and P 3 - 2 illustrate both sides of a typical veroboard respectively.

3.3.2 The 74N Digital Integrated Circuits

The 74N series includes a variety of logic devices. The types utilized in the present work are categorized as follows:

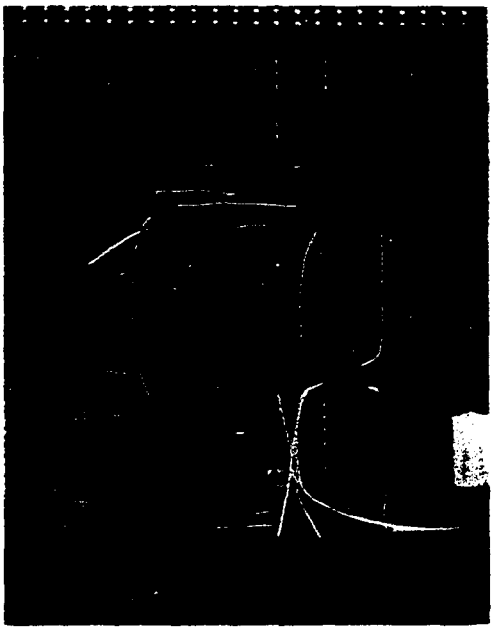
(a) NAND Gates.

(b) Flip-Flops.

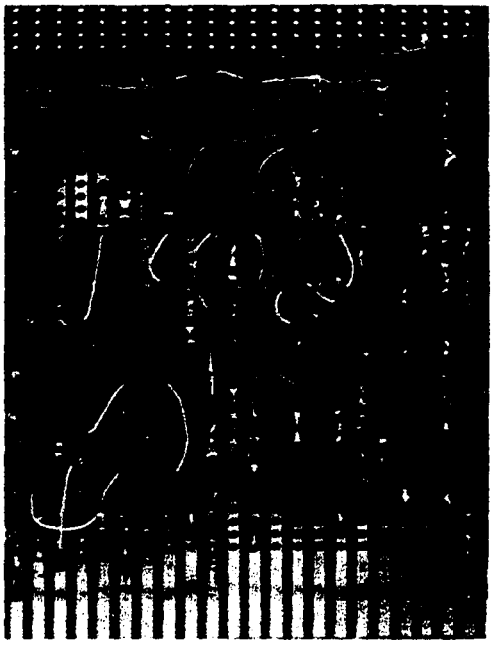
(c) Special Devices : a "packaged" combination of (a) and / or (b), these consist of decade counters and binary-coded-decimal (BCD) - to - decimal decoder / drivers.

An attempt to completely characterize these here would result in a a duplication of manufacturer specifications. It is therefore felt that a brief description of the devices from a "systems" viewpoint will be sufficient.

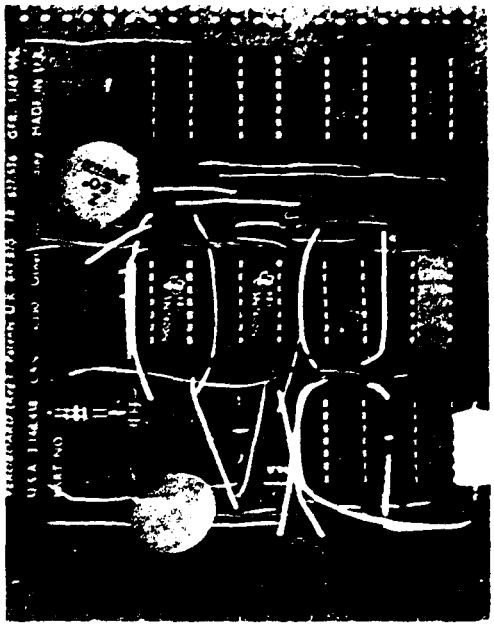
Several characteristics are common to (a), (b) and (c) above. The series 74N logic is defined in terms of standard POSITIVE LOGIC using the following definitions [26]:



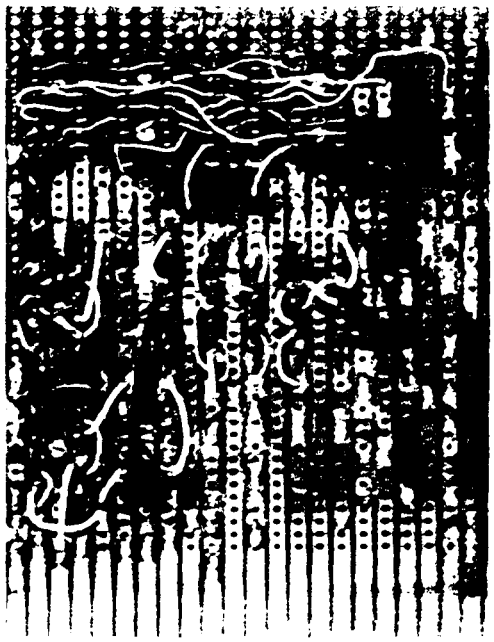
P 3.1. TOP VIEW OF CIRCUITRY MOUNTED ON VEROBOARD.



P 3.2. VIEW ILLUSTRATING BOTTOM SIDE OF VEROBOARD.



P 3.1. TOP VIEW OF CIRCUITRY MOUNTED ON VEROBOARD.



P 3.2. VIEW ILLUSTRATING BOTTOM SIDE OF VEROBOARD.

LOW VOLTAGE ≡ LOGICAL 0

HIGH VOLTAGE ≡ LOGICAL 1

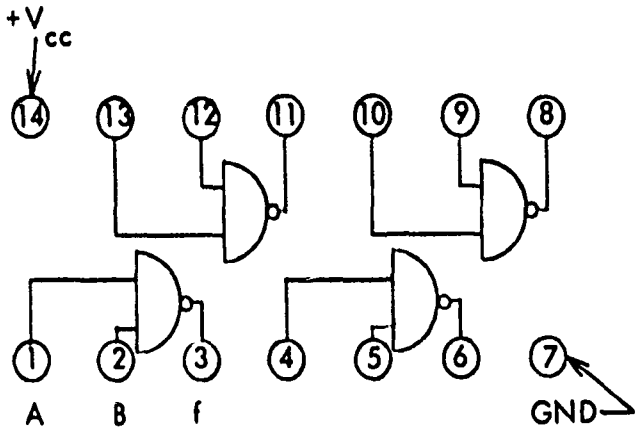
When the devices are operated with a recommended DC supply of 5.2 volts, output logic levels of 0.4 volts (logical 0) and 4 volts (logical 1) are typical. To drive the logic circuitry a regulated DC supply [27], [28] was designed and built. The circuit diagram of the supply is shown as Figure A.1.1 in the Appendix.

(a) Nand Gates

Four types of NAND gates are found in the logic circuitry. These are illustrated in Figure 3.3.1. The first three - the SN 7400N, SN 7410N and SN 7420N differ insofar as the number of gate inputs are concerned. The fourth, an SN 7440N, contains two - 4 input NAND gates and is distinguished from the SN 7420N in that the output of each of its gates has a fan-out of 30. The gate outputs of the first three units have a fan-out of 10. Fan-out reflects the ability of an output to sink current from a number of loads at a logical 0 voltage level and to supply current at a logical 1 voltage level [26].

For each of the gates the propagation time to a logical 0 is typically 8 nanoseconds, while the propagation time to a logical 1 is 18 nanoseconds. These delays are illustrated in Figure 3.3.2.

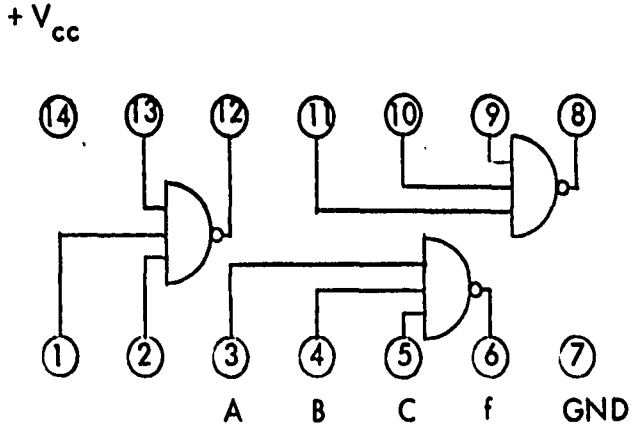
The NAND gates are utilized primarily to implement combinational switching functions. In some instances it was convenient to extend their use into other applications. An example of this is shown in Figure 3.3.3 (a), where two



f = (AB)'

SN 7400 N

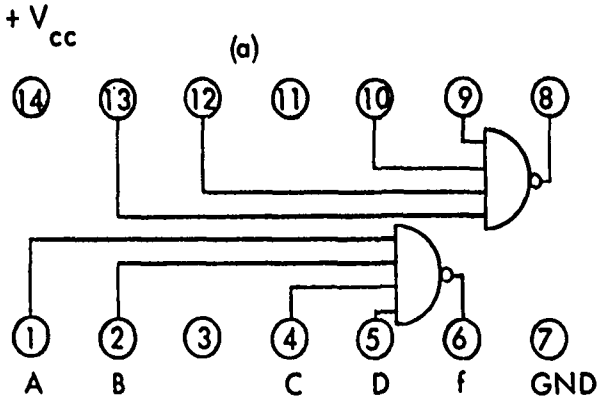
(a)



f = (ABC)'

SN 7410 N

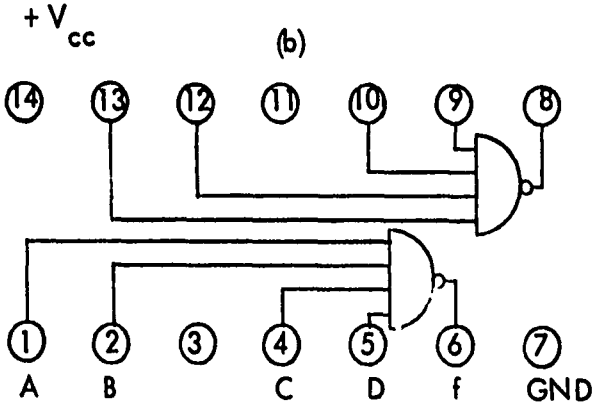
(b)



f = (ABCD)'

SN 7420 N

(c)



f = (ABCD)'

SN 7440 N

(d)

FIGURE 3.3.1. SERIES 74 N NAND GATES.

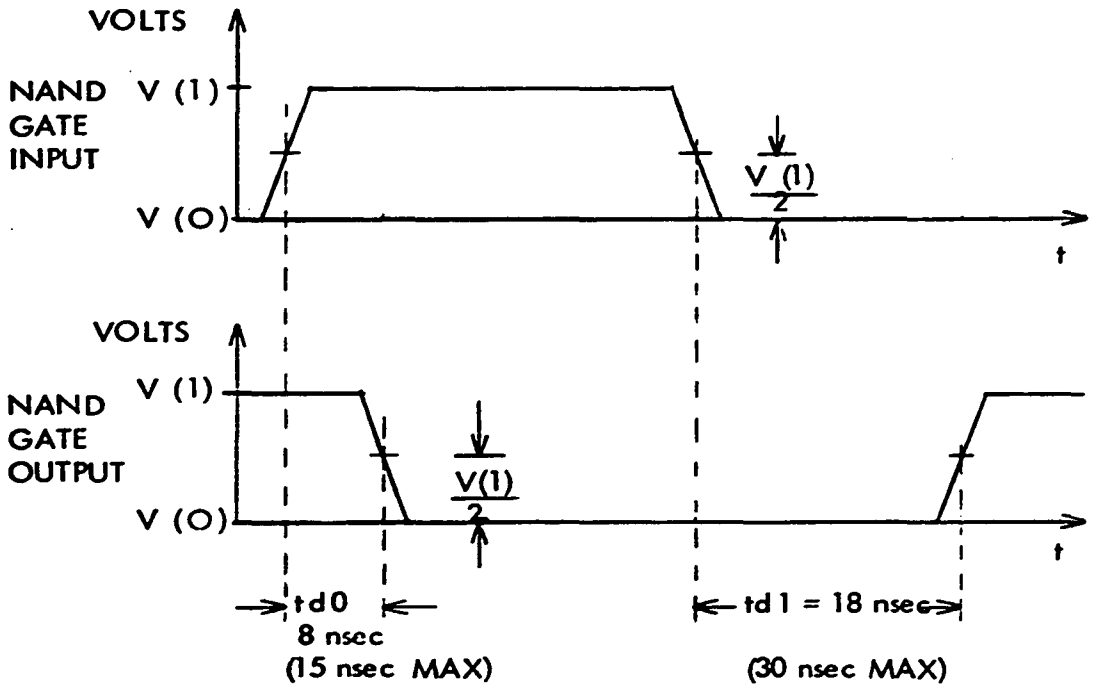


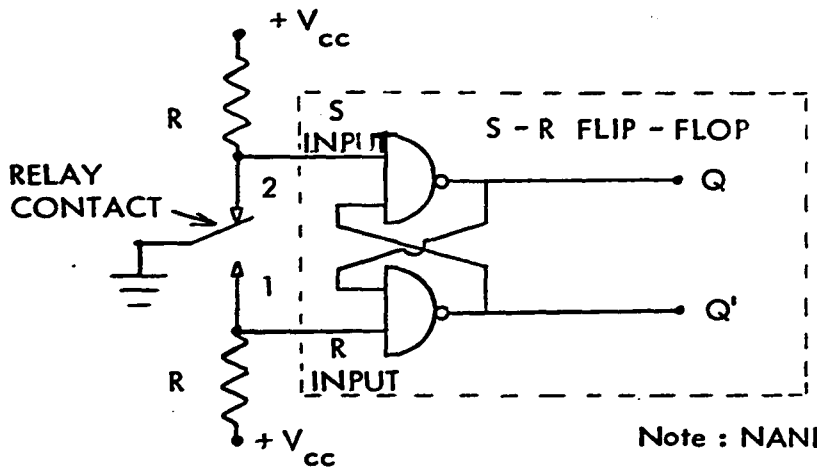
FIGURE 3.3.2. PROPAGATION DELAY TIMES OF SERIES 74N NAND GATES.

NAND gates are combined to form a direct SET - RESET flip-flop. This arrangement also serves as an effective interface between relay or switch contacts and integrated circuitry in that it eliminates the undesirable effects of contact bounce [29]. The truth table of the SET - RESET flip-flop is shown in Figure 3.3.3 (b). The waveform of Figure 3.3.3 (c) depicts the output Q of the flip-flop when it is used in conjunction with a relay contact.

Monostable (ONE-SHOT) and astable multivibrators are also made up of NAND gates. The ONE-SHOT, shown in Figure 3.3.4, is triggered on the negative-going edge of the input pulse. The width of the output pulse is approximately 1.4 RC [30]. In the astable multivibrator of Figure 3.3.5, R_2 and C control the frequency of oscillation whereas pulse width is adjusted by means of R_1 [31].

(b) Flip - Flops

Three types of flip-flops are employed in the logic circuitry : the SN 7470N, the SN 7472N and the SN 7474 N. The first two are J - K types whereas the third is a D - flip-flop. The flip-flops, along with their truth tables are shown in Figures 3.3.6 (a), (b) and (c). In Figures 3.3.6 (a) and (b) each J and K input is derived from three separate inputs gated by an AND gate. In the SN 7470N a J input and a K input are inverted, so that $J = J_1 J_2 J'$ and $K = K_1 K_2 K'$. Each of the flip-flops is reset by a logical 0 voltage applied to the clear input. Conversely, the flip-flops are set to a logical 1 by applying a logical 0 voltage to the preset input.



Note : NAND Gates are SN7400N types.

FIGURE 3.3.3 (a) .

S t_n	R t_n	Q t_n	Q t_n
0	0	0	x
0	0	1	x
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Note : x denotes an indeterminate state.

FIGURE 3.3.3 (b) .

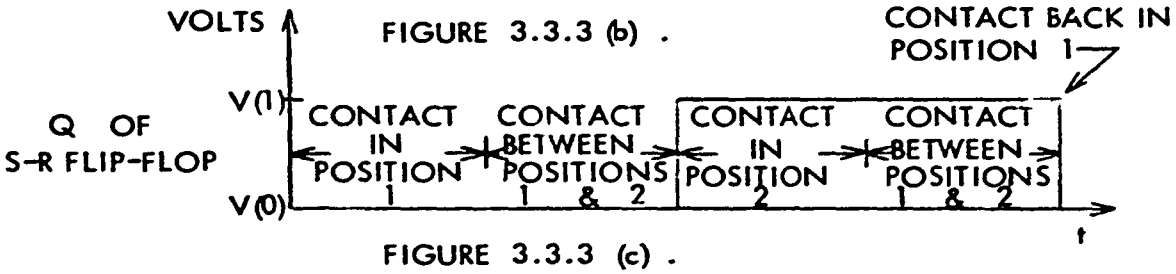
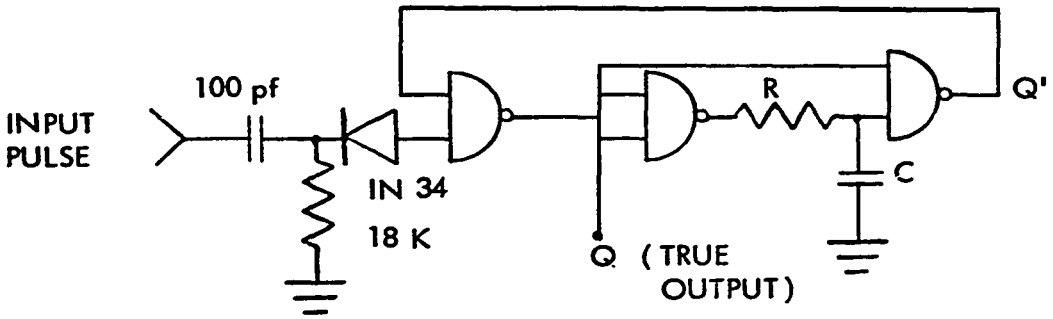


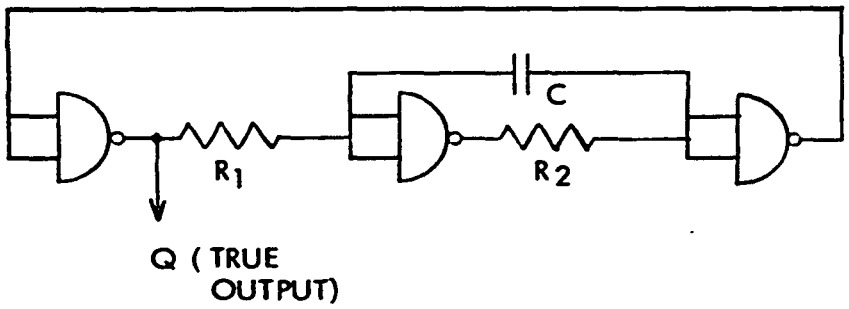
FIGURE 3.3.3 (c) .

FIGURE 3.3.3. S - R FLIP - FLOP COMPOSED OF SERIES 74 N NAND GATES.



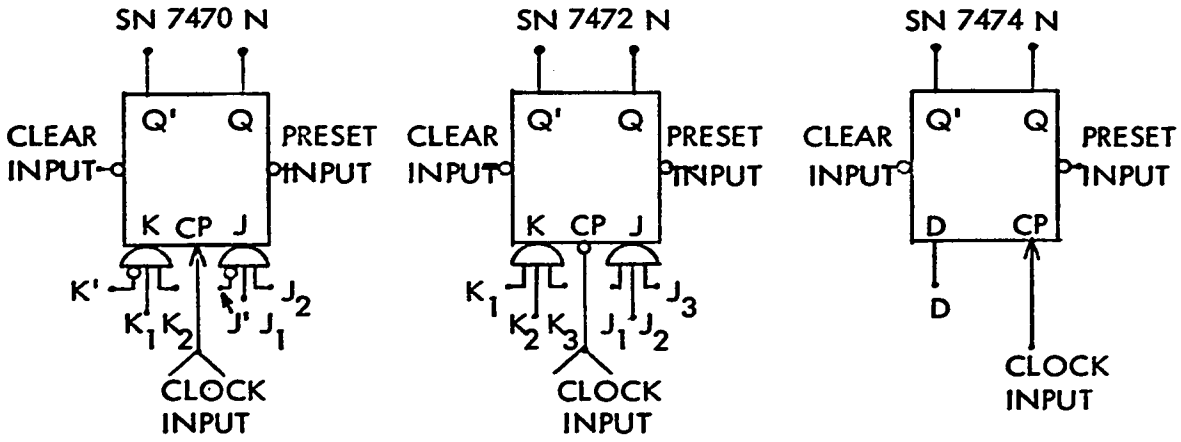
Note : NAND Gates are SN7400N types.

FIGURE 3.3.4. ONE-SHOT COMPOSED OF NAND GATES.



NOTE : NAND Gates are SN7400N types.

FIGURE 3.3.5. ASTABLE MULTIVIBRATOR COMPOSED OF NAND GATES.



t_n		t_{n+1}
J	K	Q
0	0	$Q\,t_n$
0	1	0
1	0	1
1	1	$Q'\,t_n$

$J = J_1\ J_2\ J'$

$K = K_1\ K_2\ K'$

t_n		t_{n+1}
J	K	Q
0	0	$Q\,t_n$
0	1	0
1	0	1
1	1	$Q'\,t_n$

$J = J_1\ J_2\ J_3$

$K = K_1\ K_2\ K_3$

t_n	t_{n+1}	
Input Q	Output Q	Output Q'
0	0	1
1	1	0

General Notes :

Low Input to Preset Sets Q to Logical 1 .

Low Input to Clear Sets Q to Logical 0 .

t_n = Bit Time Before Clock Pulse.

t_{n+1} = Bit Time After Clock Pulse.

FIGURE 3.3.6 (a) FIGURE 3.3.6 (b) FIGURE 3.3.6 (c)

FIGURE 3.3.6. SERIES 74 N FLIP - FLOPS.

Both the SN 7470N and the SN 7474N flip-flops are triggered on the positive-going edge of the input clock pulse. The J, K or D inputs are "read" while the clock is low and transferred to the output on the positive edge of the clock pulse. In the SN 7472 N flip-flop the J and K data is read into a temporary memory while the clock input is high and is transferred to the output on the negative edge of the clock pulse. A restriction on the SN 7470N requires that the clock input be at a logical 0 prior to the application of a clear or preset pulse.

The switching times [26] for the SN 7470N flip-flop are shown in Figure 3.3.7. Waveform (a) represents the clock pulse. The clock pulse must have a width, t_p, of at least 20 nanoseconds and a risetime not exceeding 150 nanoseconds. The maximum allowable clock frequency is 35 MHZ. In waveform (b), t_{set-up} is the time that an inverting J' or K' input is to be set to a logical zero prior to the occurrence of a clock pulse in order to cause a change in the output (Q or Q') state of the flip-flop. In waveform (c), t_{hold} implies that a non-inverting J or K input must be held at a logical 1 for at least 15 nanoseconds into the clock pulse in order to cause a change in the output state of the flip-flop. Both t_{d0} and t_{d1}, the propagation delay times, are typically 30 nanoseconds, as shown in waveforms (d) and (e) respectively.

The switching times for the SN 7472N and the SN 7474N flip-flops are shown in Figures 3.3.8 and 3.3.9 respectively. The maximum allowable clock repetition rate is 14 MHZ for the SN 7472N and 25 MHZ for the SN 7474N.

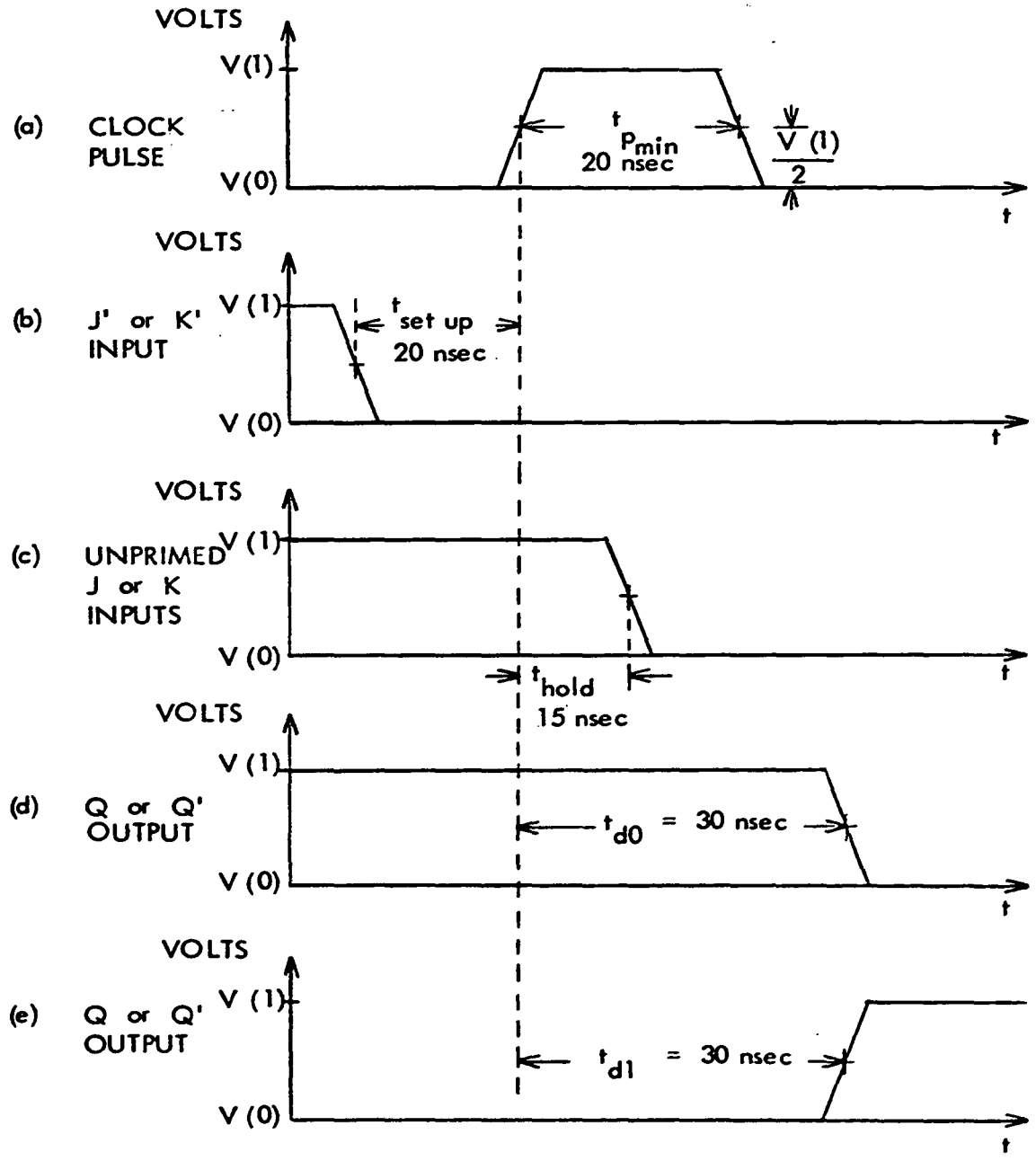


FIGURE 3.3.7. TYPE SN 7470N FLIP-FLOP SWITCHING TIMES.

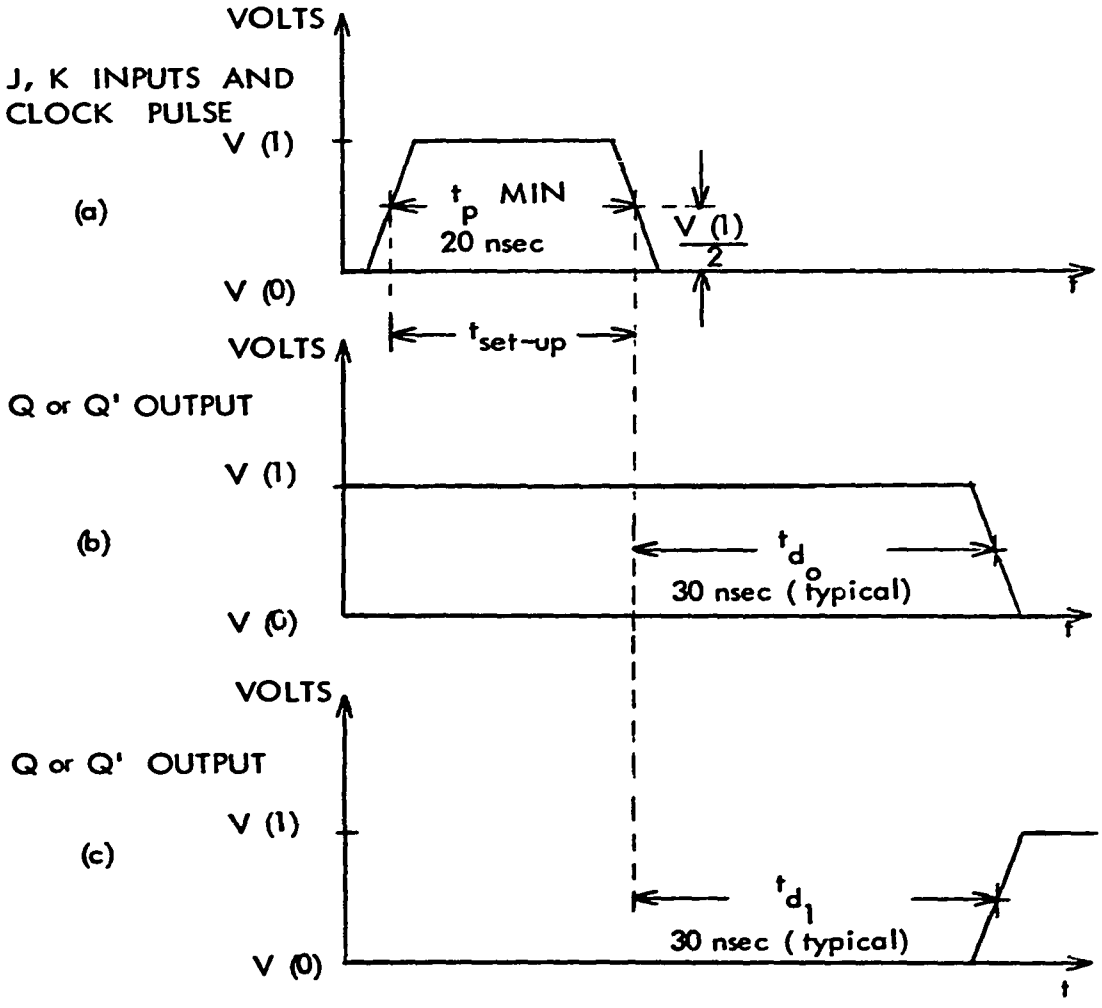


FIGURE 3.3.8. TYPE SN 7472N FLIP-FLOP SWITCHING TIMES.

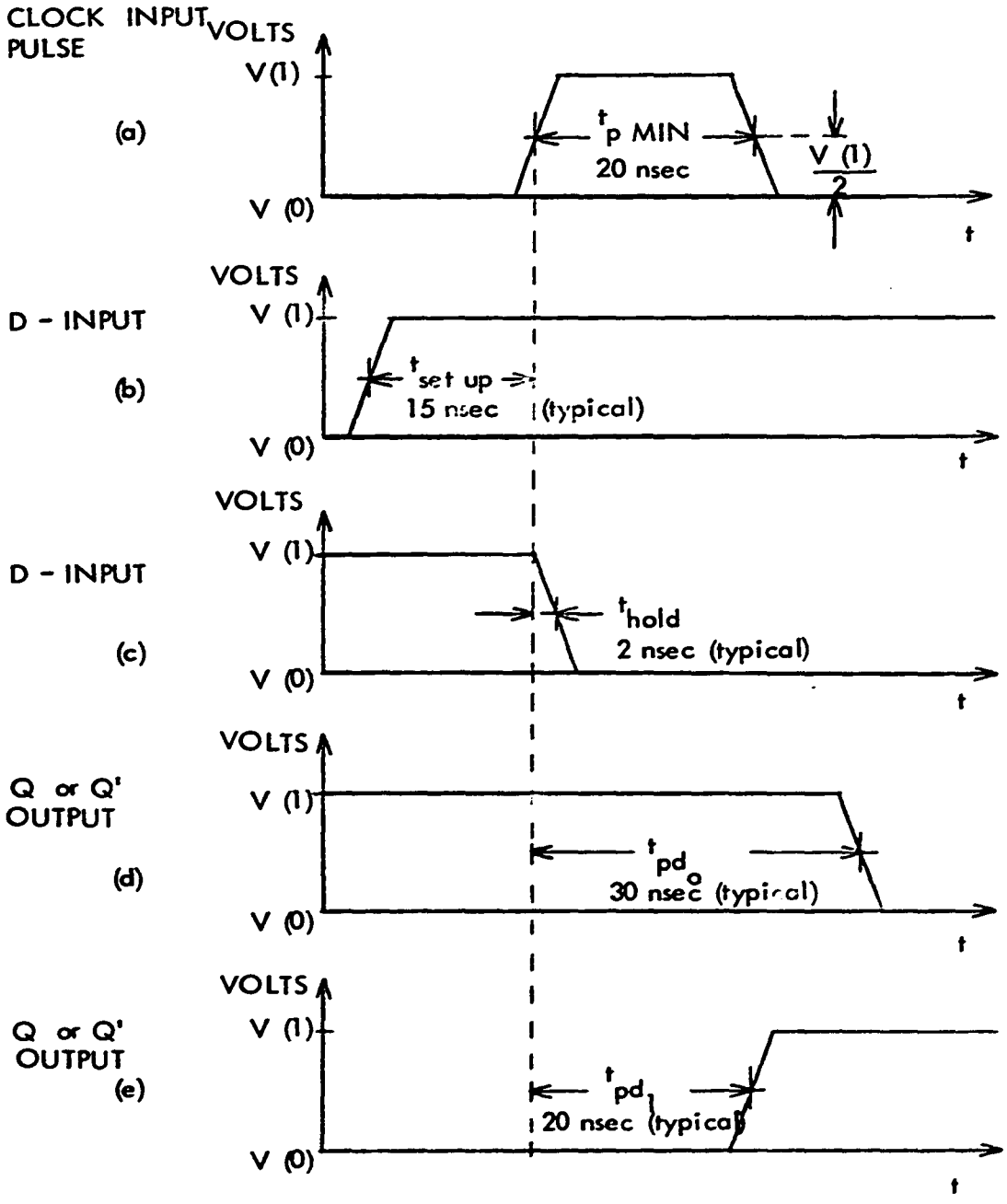


FIGURE 3.3.9. TYPE SN 7474N FLIP-FLOP SWITCHING TIMES.

(c) Special Devices

The special devices consist of the SN 7490N counter and the SN 7441N BCD-TO-DECIMAL DECODER / DRIVER. The SN 7490N is shown in Figure 3.3.10 (a). When used as a binary-coded-decimal (BCD) decade counter the BD input is externally connected to the A output. Input A receives the incoming count and a sequence is obtained in accordance with the BCD count sequence truth table of Figure 3.3.10 (b). The counter may be reset according to the RESET / COUNT table in Figure 3.3.10 (c).

The SN 7441N decoder is depicted in Figure 3.3.11. The accompanying truth table relates the decimal output lines, 0 through 9, to the binary inputs A, B, C and D. The decoder is designed to function primarily as a lamp or relay driver. As such, an output line which is ON is at a logical 0, in accordance with the truth table. The remaining lines are at a high, or logical 1 voltage level.

3.4.1 The Operation of the Logic Circuits

The remaining sections of this chapter illustrate the operation of the logic circuitry. The control logic, as previously mentioned is subdivided into three distinct units, namely CONTROL A, CONTROL B and CONTROL C. The logic within CONTROL A advances a sample of a graph paper by a preset amount. A scan of the graph is then made and the ordinate of the graph determined by CONTROL B.

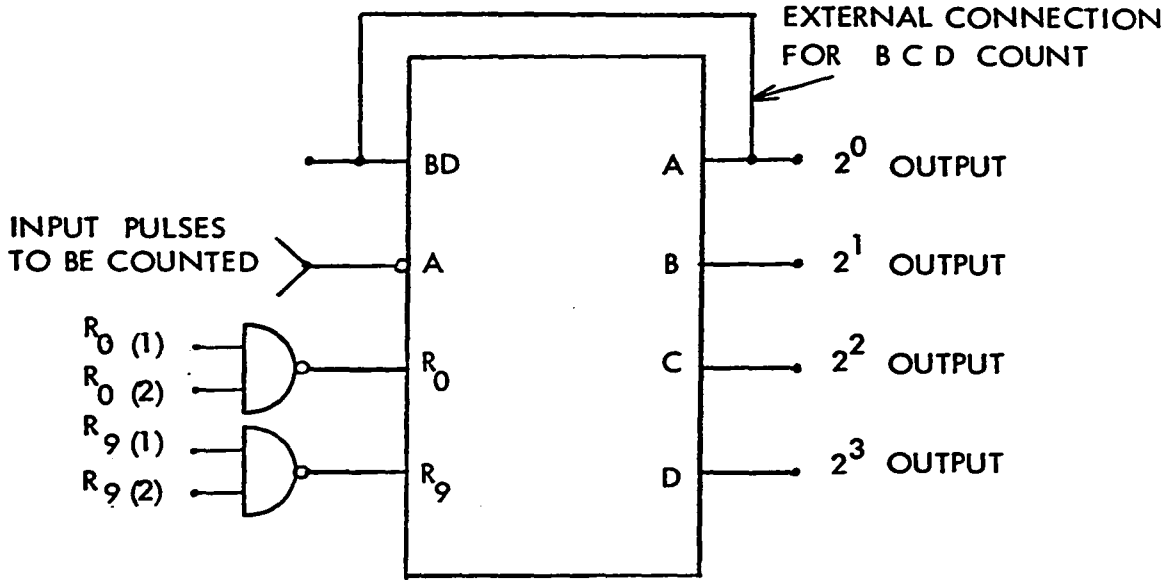


FIGURE 3.3.10 (a). SN 7490N DECADE COUNTER.

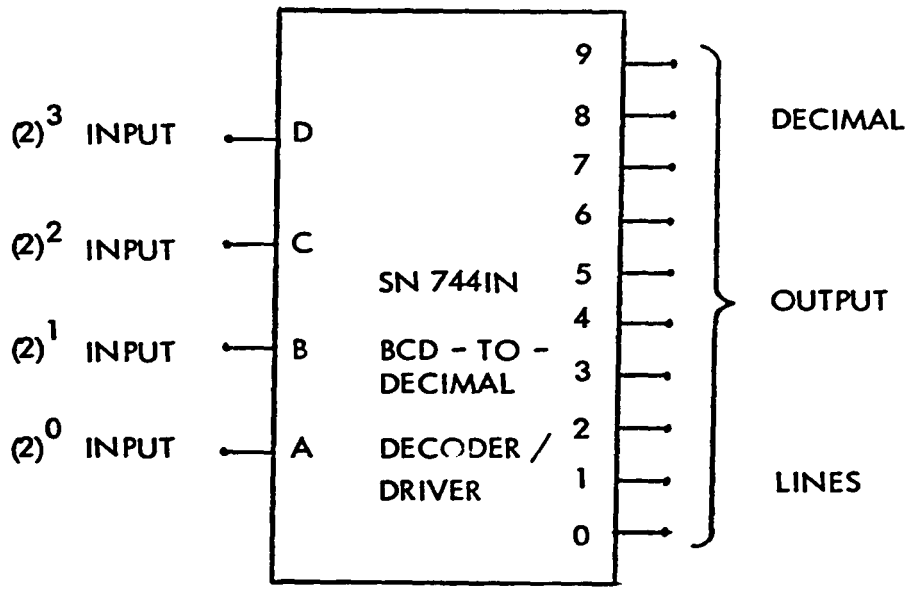
DECIMAL COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

FIGURE 3.3.10 (b). COUNT SEQUENCE OF SN 7490N DECADE COUNTER.

RESET INPUTS				OUTPUT			
R_{0} (1)	R_{0} (2)	R_{9} (1)	R_{9} (2)	D	C	B	A
1	1	0	ø	0	0	0	0
1	1	ø	0	0	0	0	0
ø	0	1	1	1	0	0	1
0	ø	1	1	1	0	0	1
1	1	1	1	1	0	0	1
ø	0	ø	0	COUNT			
0	ø	0	ø	COUNT			
0	ø	ø	0	COUNT			
ø	0	0	ø	COUNT			

NOTE : ø denotes a "DON'T CARE" condition.

FIGURE 3.3.10 (c). SET - RESET TRUTH TABLE OF SN 7490 N DECADE COUNTER.



TRUTH TABLE OF SN 7441 N

INPUT				DECIMAL OUTPUT LINE ON
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

FIGURE 3.3.11. SN 7441N BCD - TO - DECIMAL DECODER / DRIVER.

At the end of a scan digitized information is punched out on a data card. CONTROL C regulates this punching operation.

Simplified circuit diagrams, together with timing diagrams are used to explain the logic operations within each control unit.

3.4.2 Control A

The actual logic circuit comprising control A is shown in Figure 3.4.1 (a). In Figure 3.4.1 (b) is a simplified "functional" version of the same circuit. This, together with the timing diagram of Figure 3.4.2 is presently used to illustrate the operation of Control A .

Of the three graph reader outputs previously defined, only two will be considered here : the END of SCAN (Figure 3.4.2 (a)) and the VIDEO (Figure 3.4.2 (b)) pulses. Since their voltage levels are 0 or -15 volts, and hence incompatible with the integrated circuit level requirements, level shifting is done by means of the Voltage Translators in Figure 3.4.1 (b), SECTION 1 D. The translated outputs (0 → 4 volts) and (-15 → 0 volts) are depicted in Figure 3.4.2 (f) and Figure 3.4.2 (i), respectively.

In the timing diagram, it is arbitrarily assumed that the graph reader power is turned on first, at T_o , and the logic circuits power later, at T_{1a} . It is convenient for the present purposes to further assume that at T_o , the sample of graph paper in the reader is as shown in Figure 3.4.3. In this figure, the paper is so posi-

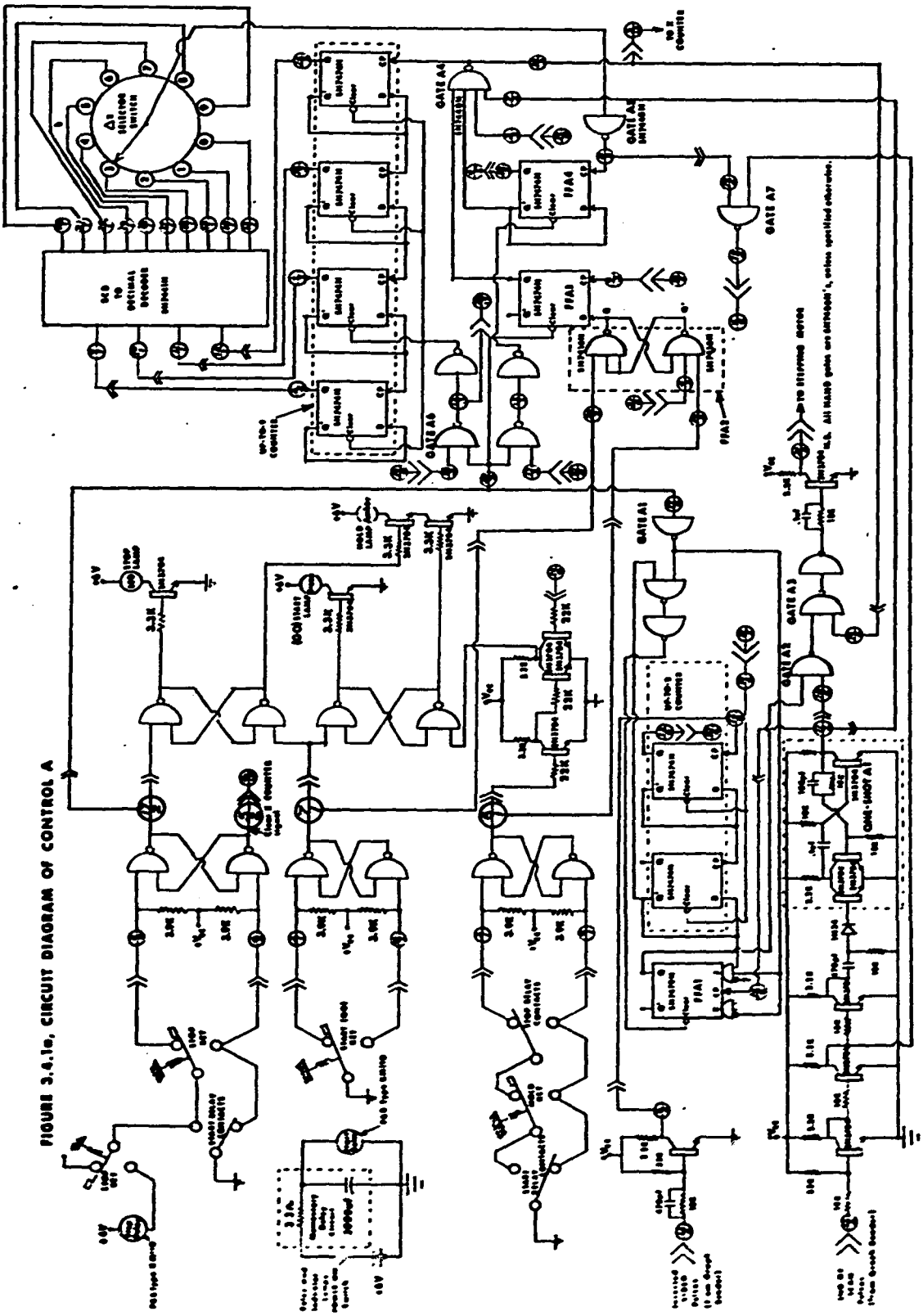


FIGURE 3.4.1a, CIRCUIT DIAGRAM OF CONTROL A

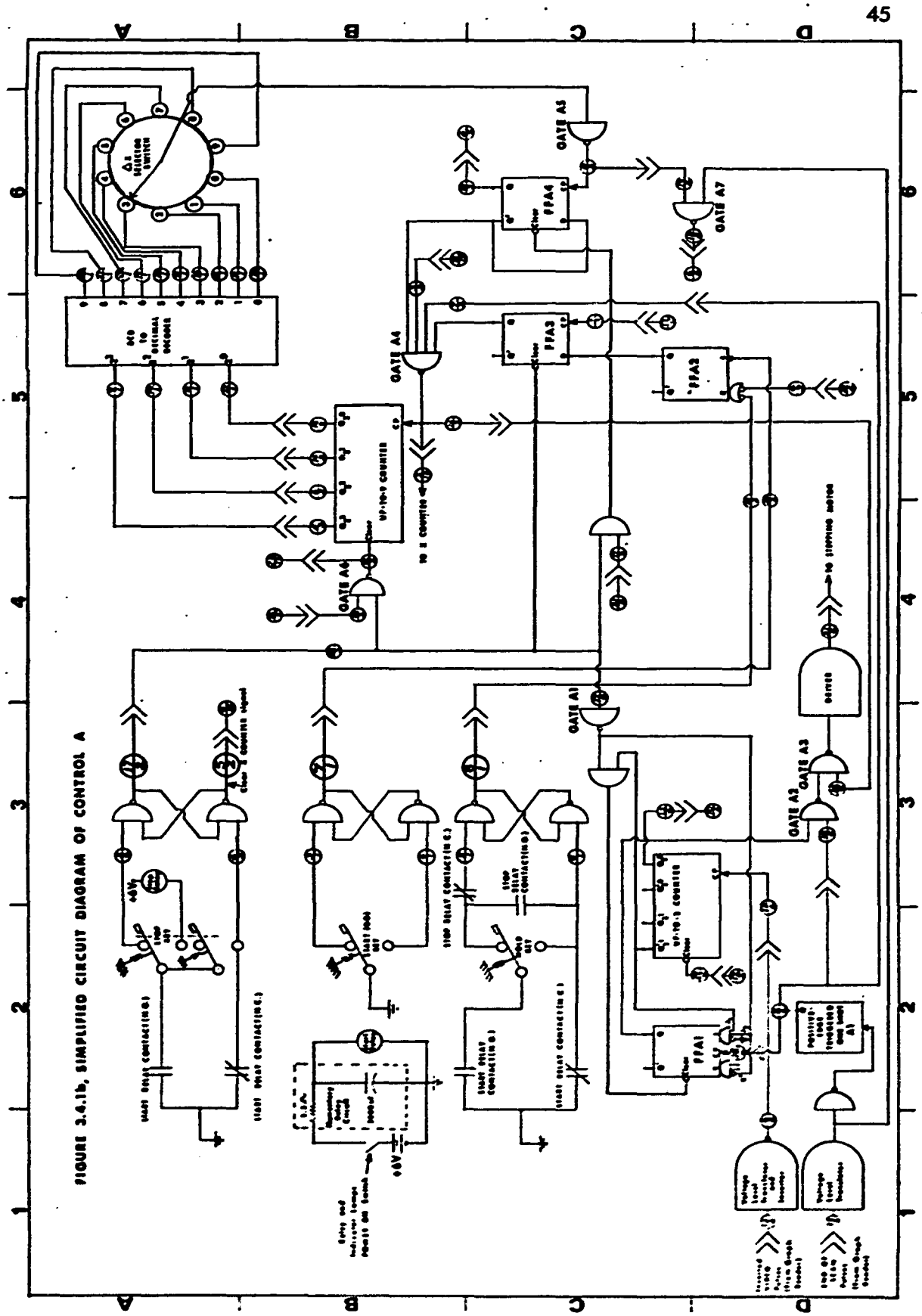
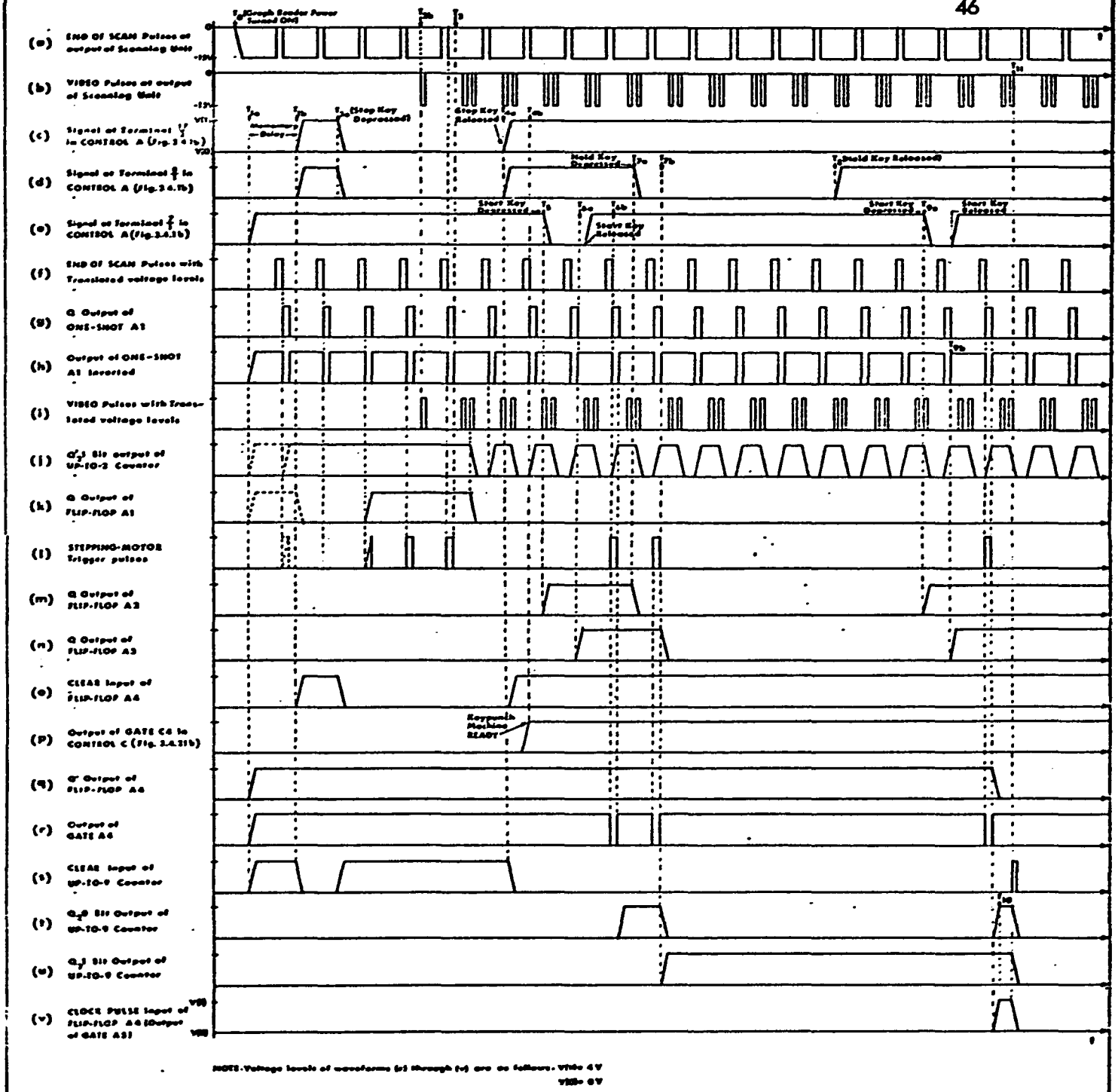


FIGURE 3.4.1b, SIMPLIFIED CIRCUIT DIAGRAM OF CONTROL A



NOTE: Voltage levels of waveforms (a) through (v) are as follows: VDD= 4 V
VSS= 0 V

FIGURE 3.4.2, TIMING DIAGRAM OF CONTROL A

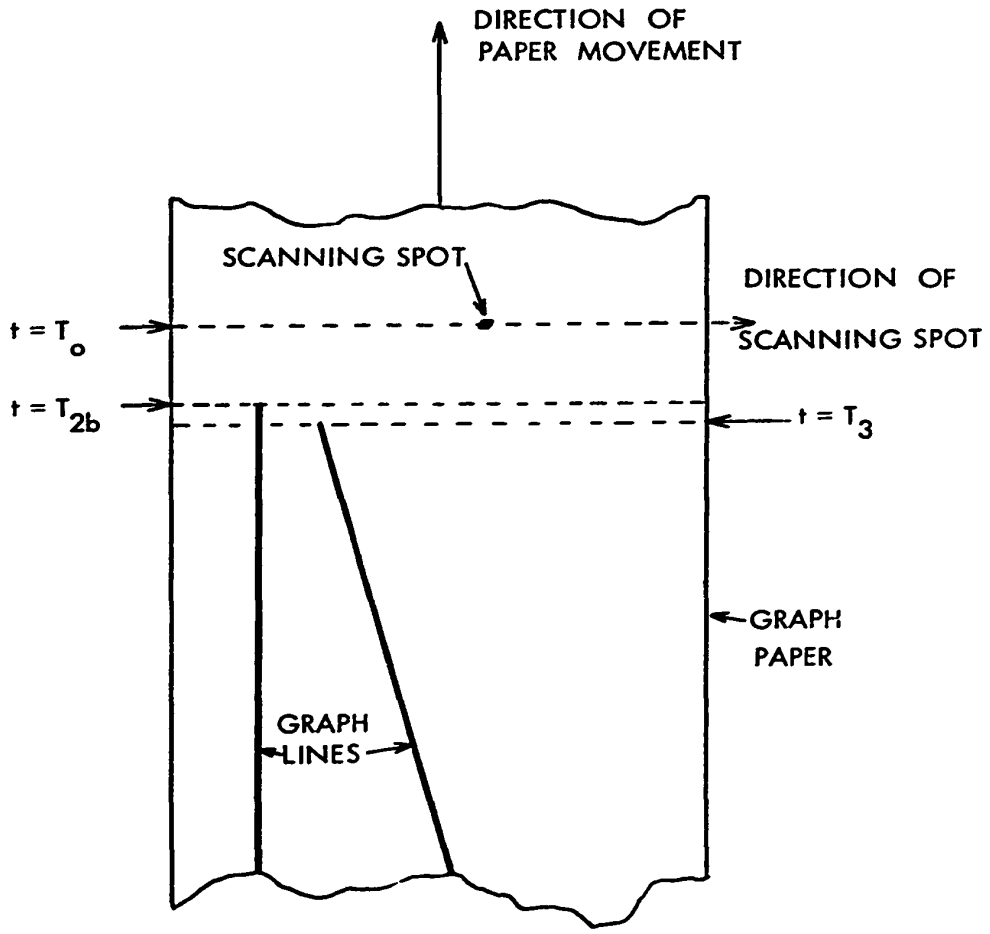


FIGURE 3.4.3. GRAPH SAMPLE USED TO ILLUSTRATE THE AUTOMATIC GRAPH - ADVANCE FEATURE IN CONTROL A.

tioned that the scanning spot is traversing a blank section. Hence for $T_o \leq t < T_{2b}$ no VIDEO pulses are shown in Figure 3.4.2 (b), (i).

To ensure that the logic is in a RESET, or CLEARED state after its power is turned on at T_{1a}, the START RELAY (Figure 3.4.1 (b), SECTION 2B), is energized through a simple R - C delay circuit. Because of this momentary delay, power is supplied to the integrated circuits before the contacts of the START RELAY open / close. In this way, a momentary "low" (logical 0) is present at outputs $\frac{17}{2}$* and $\frac{8}{1}$* (Figure 3.4.2 (c and d)). As is shown in Figure 3.4.1 (b), SECTIONS 4B, 5C, 6C, 5D and 2C, $\frac{17}{2}$ and $\frac{8}{1}$ are used as RESETS (CLEAR inputs to counters and flip-flops).

It was mentioned above that the sample of graph paper in the reader is as shown in Figure 3.4.3. The fact that at T_o, the scanning spot is not traversing (a) graph line(s) is due to the difficulty in aligning the line(s) with the spot when loading the paper, and is a typical situation. In order that digitization may begin at the point where two graph lines first occur (T_3 in Figure 3.4.3), provision is made to automatically advance the paper to T_3. This is done by means of flip-flop (FF) A 1, the UP - T0 - 2 counter and the DRIVER of Figure 3.4.1(b), SECTIONS 2, 3, 4 - C and D. The clock pulse (CP) input to the counter consists of the VIDEO PULSES (Figure 3.4.2 (i)). The counter simply records the number of VIDEO PULSES occurring during one revolution of the drum (between two successive END of SCAN pulses, Figure 3.4.2 (f)). The clear input to the counter is the pulse train of Figure 3.4.2 (h), which is simply the pulse of Figure 3.4.2 (g) inverted. Both g and h are derived

---

* $\frac{17}{2}$, $\frac{8}{1}$ et al denote terminals within the logic unit. As an example $\frac{17}{2}$ denotes terminal 17 on veroboard 2 .

from f by means of ONE-SHOT A1. Hence, the counter is reset once for every drum revolution. If the number of VIDEO PULSES in one scan is less than two, the false output of the 2^1 bit of the counter ($Q'_2 1$) will be high (logical 1). This output is fed into the J_1 input of FFA1, input J_2 being derived from $\frac{17}{2}$ (Figure 3.4.2 (c)). The true output Q of FFA1 is normally low (logical 0), since its RESET input is also derived from $\frac{17}{2}$ through the inverting gate A1. If, however, the STOP key is depressed (T_{2a}), the output of gate A1, and hence the clear, J_2, and K1 inputs are high. The clock pulse input of FFA1 is waveform g of Figure 3.4.2. The J (J_1 J_2 J') input will be high whenever J_1 input is high, providing the STOP key remains depressed. The inverting J input (J') is simply connected to ground (logical 0). The K input is low, since a high is being applied to its inverting input K'. Hence, if J is high at the occurrence of the clock pulse, the true output Q of FFA1 is set to a logical 1, as shown in Figure 3.4.2 (k). This output, gated with the ONE-SHOT A1 output of Figure 3.4.2 (g) by means of gates A2 and A3 (Figure 3.4.1 (b), SECTION 3D) is shown in Figure 3.4.2 (l) and, via a driver is used to trigger the stepping motor. In this way the stepping motor keeps advancing the paper until T_3, in steps of one millimeter. For $t > T_3$, i.e., when two video pulses occur in one scan, this process ceases, since the J_1 input to FFA1 is no longer high during the positive - going edge of its clock input. The STOP key is then released at T_{4a}, as shown in Figure 3.4.2 (c).

After the STOP key is released, the system is at rest, in that no digitization is yet taking place. It is arbitrarily assumed that the I B M keypunch machine is "ready" at time T_{4b}, in that it is loaded with data cards. The waveform of Figure

3.4.2 (p) is derived from the keypunch machine. The level of p is a logical 1 if a card is ready to be punched, and 0 otherwise.

To select the X increment (ΔX, in millimeters) desired between successive digitizations, the ΔX SELECTOR SWITCH of Figure 3.4.1 (b), SECTION 6 A is set to some position $1 \leq \Delta X \leq 9$. In the figure it is arbitrarily at 3.

The START key is depressed at T_5, causing a low at $\frac{7}{1}$, Figure 3.4.1 (b), SECTION 3B. This low sets the Q output of FFA2 to a logical 1. The output of FFA2 is coupled to the D input of FFA3. The clock pulse input to FFA3 is that of Figure 3.4.2 (h). The true output Q of FFA3 is then set to 1 at the positive-going edge of this clock pulse at time T_{6a}. Flip-flops A2 and A3 are combined in this manner so that the START key may, in a sense by synchronized with the ONE-SHOT output of Figure 3.4.2 (h), as is shown in Figure 3.4.3 ((m) and (n)). The false output Q' of FFA4 is initially high, the flip-flop having previously been cleared by the waveform of Figure 3.4.2 (o). Gate A4 has as its inputs Q of FFA3, Q' of FFA4, the waveform of Figure 3.4.3 (p) (derived from the keypunch machine) and the ONE-SHOT A1 output (Figure 3.4.2 (g)). The output of gate A 4 is shown in Figure 3.4.2 (r) and is used, in part, to advance the graph paper by the amount set at the ΔX selector switch. This is done by triggering the stepping motor through gate A3 and the DRIVER of Figure 3.4.1 (b), SECTION 4D. An UP - TO - 9 counter keeps track of the number of these triggering pulses. The true outputs Q_20, Q_21, Q_23 and Q_22 of the counter are inputted to a binary-coded-decimal (BCD) - to - decimal decoder, SECTION 5A in Figure 3.4.1 (b). The decimal ($0 \rightarrow 9$) outputs of the decoder are coupled to the ΔX selector switch.

In the timing diagram, it is shown that the process of advancing the graph paper by 3 millimeters is interrupted after the second pulse has been applied to the stepping motor. This is done here to illustrate the effect of the HOLD key. The function of the HOLD key is to provide a pause in the digitization process, if so desired. It simply halts, in this case, the paper advance process. When the HOLD key is depressed at T_{7a}, output $\frac{8}{1}$ of the HOLD circuit resets output Q of FFA2 to 0. The Q output of FFA3 however is set to 0 only at the next occurrence of the positive edge of its clock pulse, at T_{7b}. Until the START key is depressed again at T_{9a}, the paper - advance mechanism is inhibited. At T_{9b}, the Q output of FFA3 is again set to 1, thus enabling one more pulse to advance the step motor. At T_{10}, the contents of the UP - TO - 9 counter is 3 and the output of gate A5 goes high (Figure 3.4.2 (v)). This sets the Q' output of FFA4 to 0, thus inhibiting any more pulses from occurring at the output of gate A4. The output of gate A4 is also applied to the 'ΔX' counter, which simply keeps a record of the current X value. At T_{11}, the UP - TO - 9 counter is cleared. Note that this is done at the negative going edge of the second video pulse. The pulse is derived from ONE-SHOT B2 in control B and is an input to gate A6 in Figure 3.4.1 (b), SECTION 4 B. It is during the time $T_{10} < t < T_{11}$ that the distance between two graph lines, Y in Figure 3.4.3, is obtained and stored in a register, together with the current X value as contained in the ΔX counter. For $t > T_{11}$, this data is punched onto cards. When the punch cycle is completed, the graph paper is advanced again, starting at T_{6b} in Figure 3.4.2.

The circuitry involved in the determination of the Y value and the punch cycle is covered in the next sections - Control B and Control C respectively.

3.4.3 Control B

In the previous section the logic involved in advancing a sample of graph paper by preset increments was presented. These increments were recorded in a counter - the contents of this counter thus retained the current abcissa or X value of a graph sample.

The ordinate, or Y value of a graph is determined by means of the circuitry contained in Control B. Before discussing this it is worthwhile here to briefly review the detection process whereby is sensed a line(s) on graph paper. In Chapter II it is mentioned that lines on a graph are detected by a photomultiplier tube. Whenever the scanning spot traverses a line, less light is reflected from the paper. This reflected light is sensed by the photomultiplier. Video pulses are derived from the photomultiplier output by means of additional circuitry. In Figure 3.4.4 (a) is shown a sample of paper containing two lines, line A being a reference X - axis. The photomultiplier output, depicted in Figure 3.4.4 (b) shows a sharp transition from a dark level at "a", where the spot first hits the paper. The darker levels at "b" and "d" occur when the spot traverses the lines. Point "c" represents the brightest level mainly because reflected light is here normal to the photomultiplier lens. It is in the region about "c" that the detection process is most sensitive and hence most susceptible to noise - in the form of dirt or alien

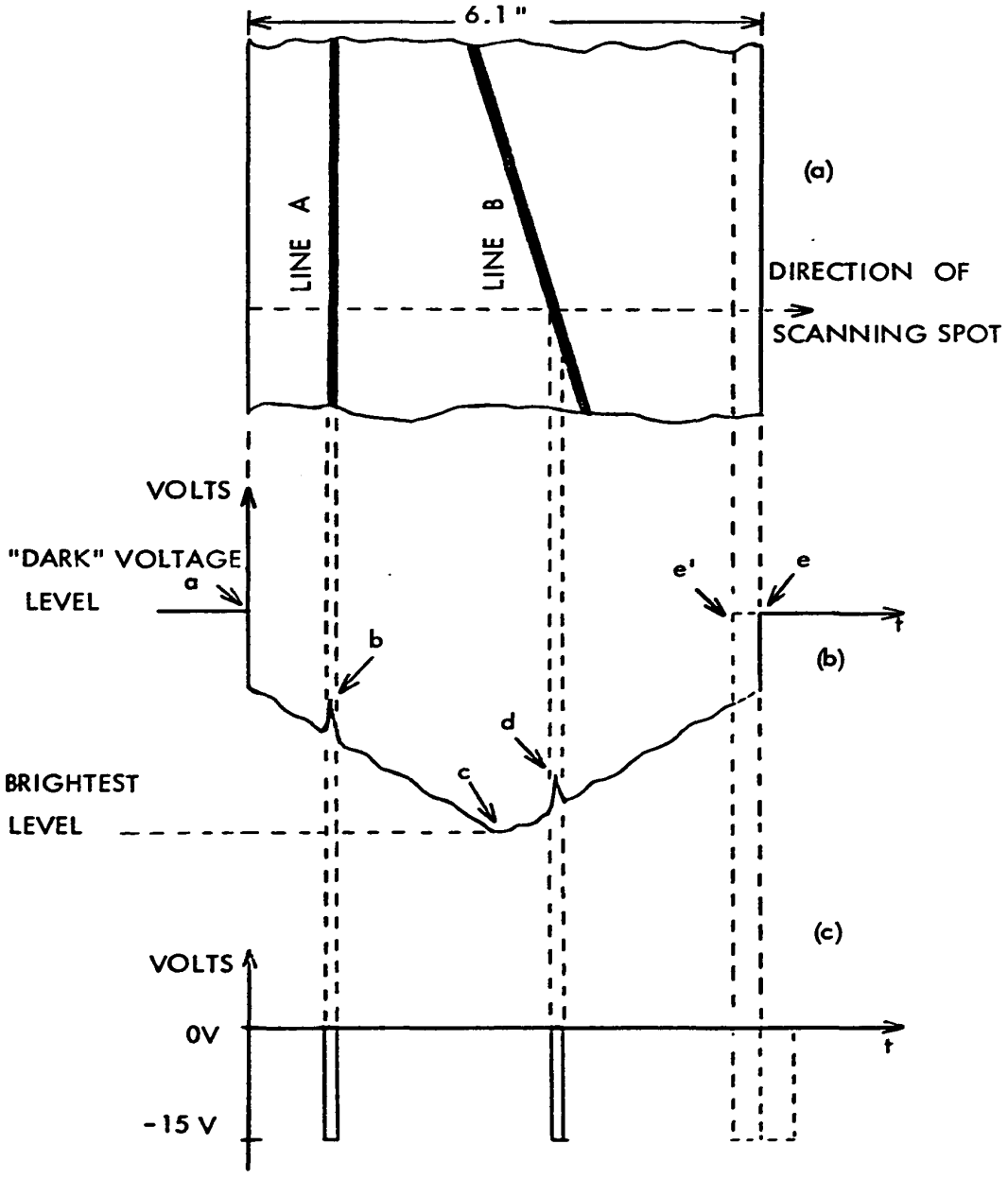


FIGURE 3.4.4. (a) SAMPLE OF GRAPH PAPER.

(b) PHOTOMULTIPLIER OUTPUT VOLTAGE.

(c) VIDEO PULSES.

markings on a graph sample. At "e" a sharp transition into the dark level occurs. The total distance traversed by the scanning spot is 6.1 inches. If the sample of paper is 6.1 or more inches wide then transition "e" represents the termination of a scan - in that the scanning spot no longer exists. When the paper is less than 6.1 inches wide then the transition occurs at " e '" - because the spot is then scanning the black background in the darkroom where the paper is contained.

In Figure 3.4.4 (c) are shown the video pulses corresponding to the photomultiplier output. In addition to pulses representing the occurrence of graph lines it is probable that yet a third pulse may occur due to the transition into the dark level at "e" or "e'" . In either case (e or e') the probability of occurrence depends on the sensitivity to which the detection process is preset. As an example, the sensitivity may be increased by increasing the intensity of the scanning spot. Sensitivity is discussed more fully in the next chapter.

The circuitry of Control B is shown in Figure 3.4.5 (a). In the present discussion reference will be made to its simplified version, Figure 3.4.5 (b). The timing diagram of Control B - Figure 3.4.6, assumes a graph sample similar to that of Figure 3.4.4 (a) and the photomultiplier output is repeated in Figure 3.4.6 (a). The video pulses are shown in Figure 3.4.6 (i).

In the concluding remarks on Control A it is mentioned that the value of Y is obtained during time : $T_{10} < t < T_{11}$. Recall that by time T_{10} , the paper had been advanced by a preset amount of 3 millimeters. This caused the output of gate A 5 in Figure 3.4.1 (b) to go high. This output, again shown in Figure 3.4.6 (g)

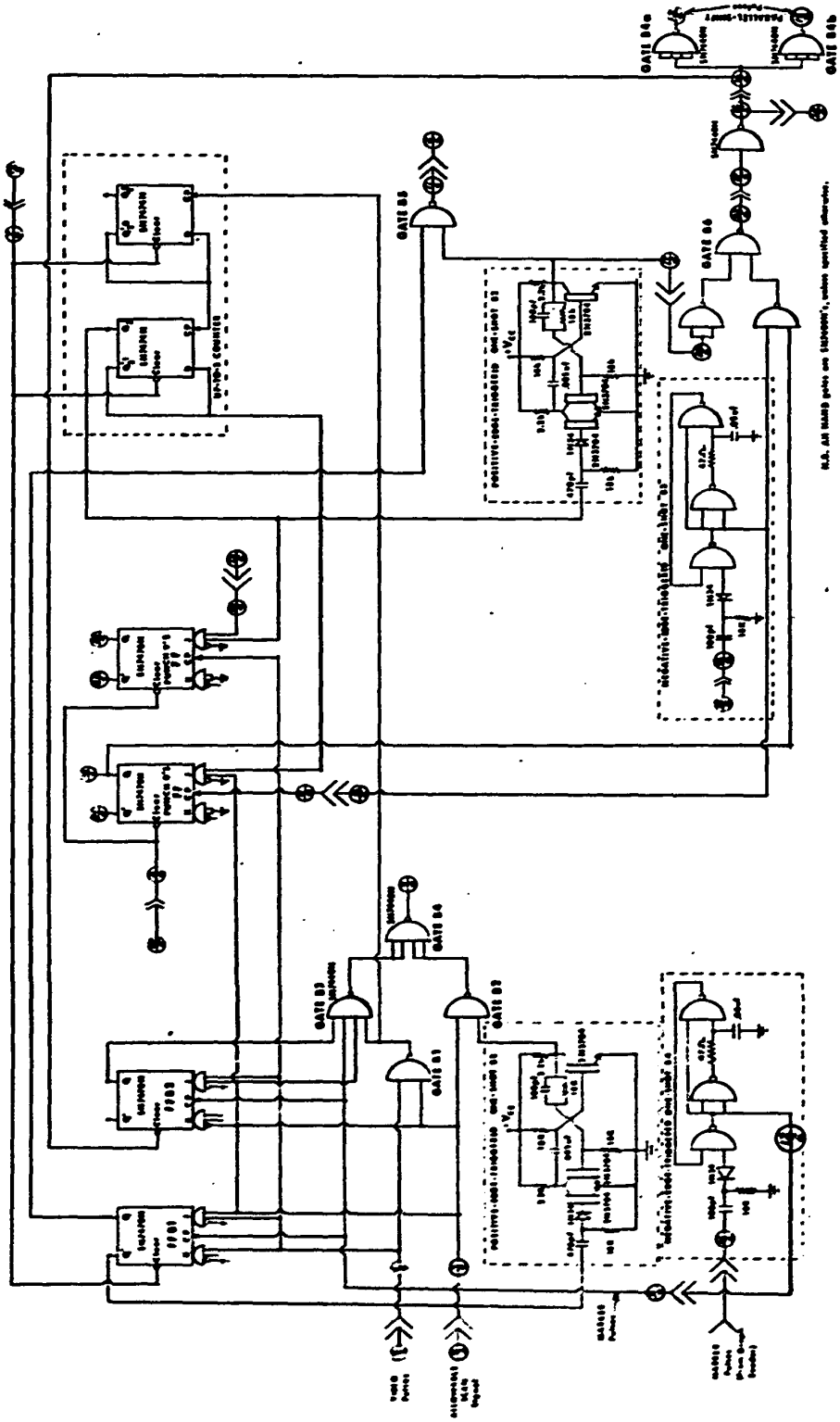


FIGURE 3.4.5a, CIRCUIT DIAGRAM OF CONTROL B

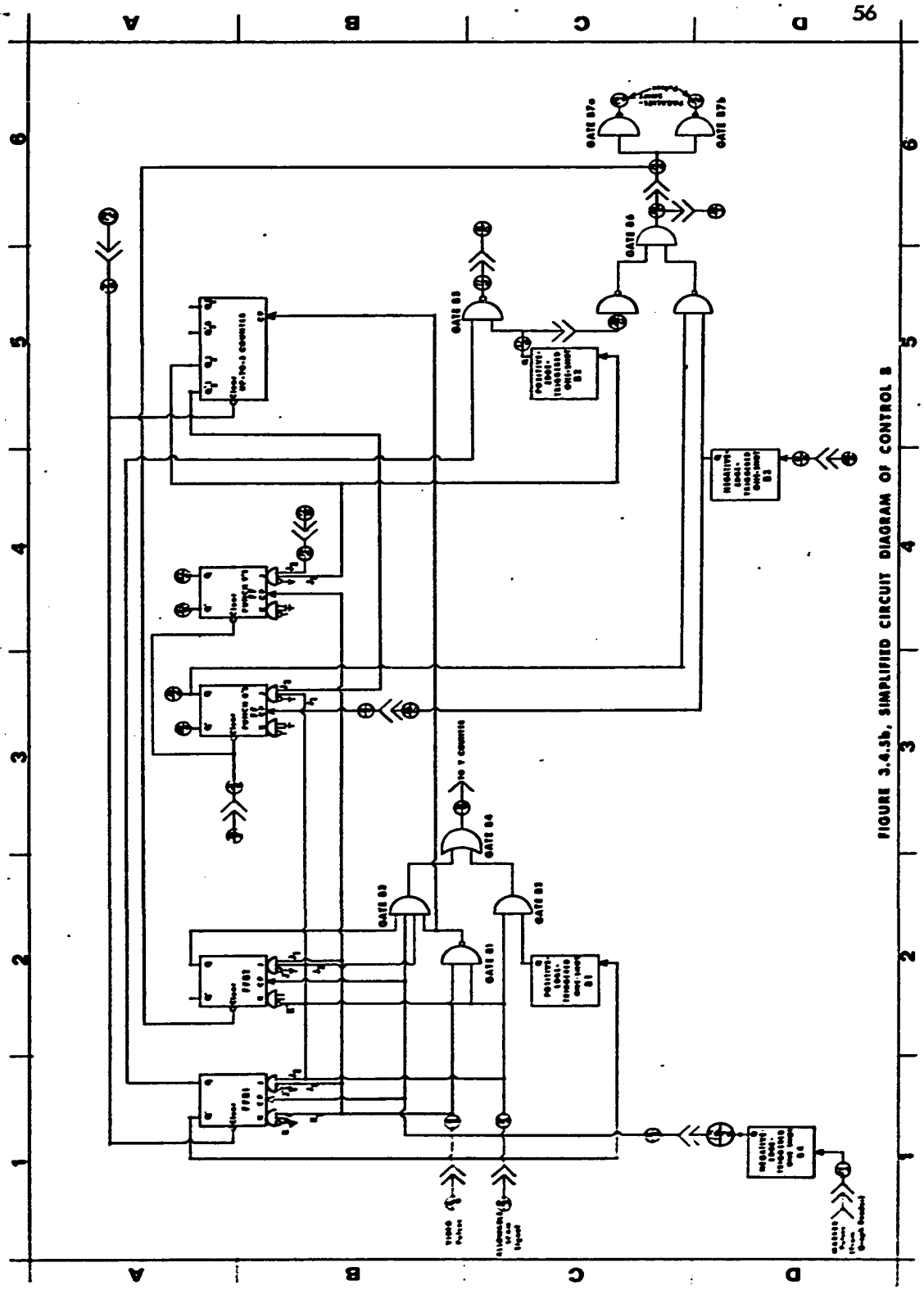


FIGURE 3.4.5b, SIMPLIFIED CIRCUIT DIAGRAM OF CONTROL B

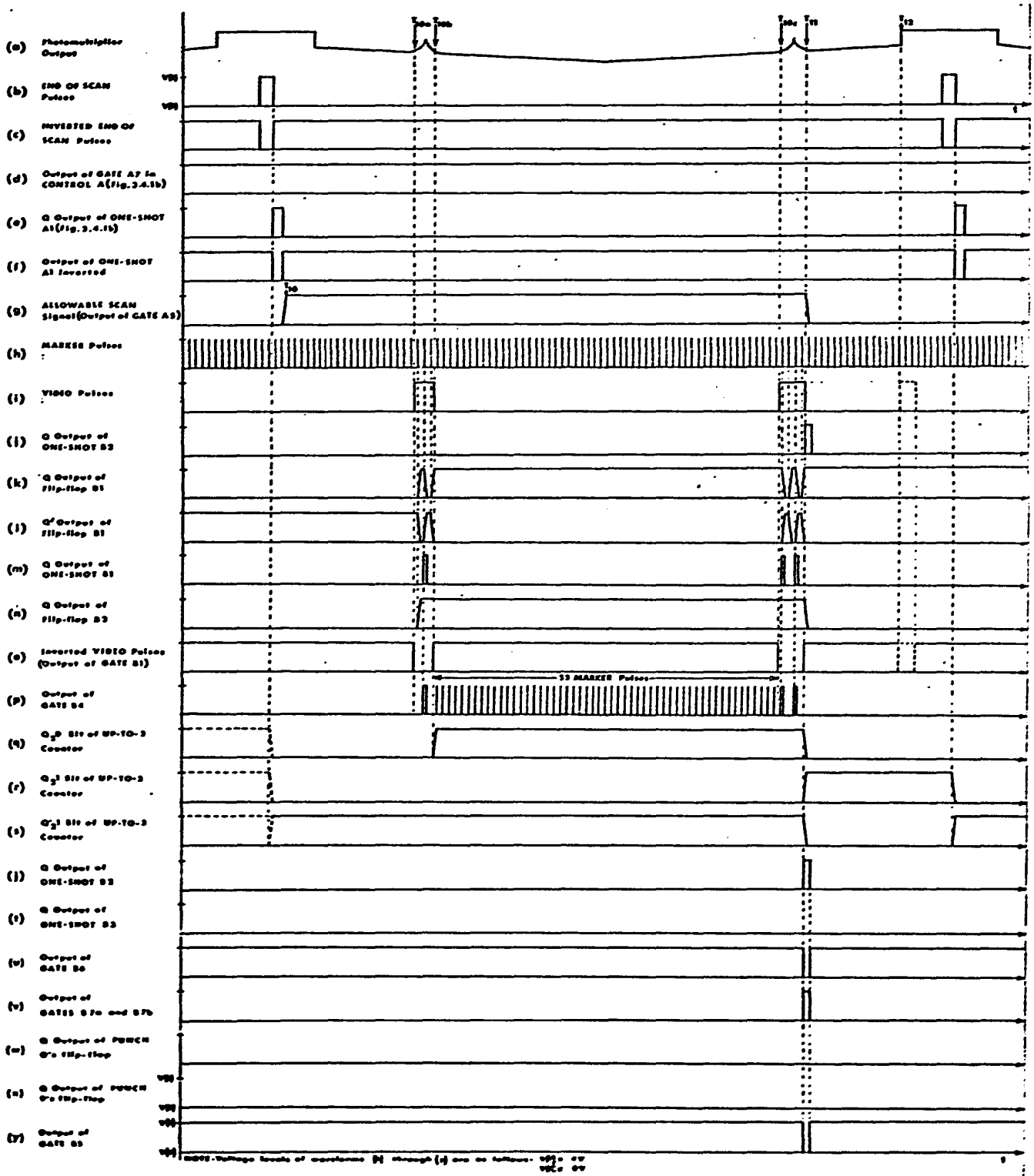


FIGURE 3.4.6. TIMING DIAGRAM OF CONTROL B

goes low at the negative going edge of the second video pulse (T_{11}). This is done by means of GATE B 1 (SECT'ON 2 B), the UP-TO-3 COUNTER (SECTION 5A) and the POSITIVE-EDGE-TRIGGERED ONE-SHOT B2 (SECTION 5C) in Figure 3.4.5 (b). The inputs to GATE B1 are the video pulses and the output of gate A5. The NAND operation on these inputs yields inverted video pulses shown in Figure 3.4.6 (o) . This serves as the clock input to the UP-TO-3 counter. The true output of the 2^1 bit of this counter, waveform r , goes high on the second positive-going edge of the output of gate B1 and triggers ONE-SHOT B2 . The output of the ONE-SHOT is inverted and, via gate B6 (SECTION 5C) is obtained the pulse of Figure 3.4.6 (u). This pulse clears the UP-TO-9 counter of Control A. Recall that the input to gate A5 was derived from the counter, via the BCD-TO-DECIMAL decoder and subsequently the ΔX selector switch.

In ensuing discussions the output of gate A5 is referred to as the ALLOWABLE SCAN, in that whenever this signal is at a logical 1 it is then that the Y value of a graph is determined. To obtain Y a count of marker pulses occurring during and between two video pulses is recorded.

The marker pulses, shown in Figure 3.4.6 (h) , are generated by means of a marker disc, in the manner described earlier in Section 2.1 (ii). Relative to the speed of the scanning spot the marker frequency (9743 Hz) is such that the distance between successive marker pulses is 0.01 inches.

As was the case with the END OF SCAN and VIDEO pulses, it was necessary to translate the voltage level of the MARKER PULSES

to + 4 volts and 0 volts respectively. This is done by means of the NEGATIVE-EDGE-TRIGGERED ONE-SHOT B4 (SECTION 1D) of Figure 3.4.5 (b). The marker pulses emanating from the marker disc (Figure 2.1.1) are fed to ONE-SHOT B4. The true output (Q) of the ONE-SHOT is shown in Figure 3.4.6 (h) and is used as the marker pulse source for the logic within Control B .

The marker pulse counter, which stores the Y value of a graph has as its input the output of gate B4 (SECTION 3B) in Figure 3.4.5 (b). The pulses to be counted are obtained by means of FLIP-FLOP B1 (FFB1), FFB2, ONE-SHOT B1 and the AND-OR gate structure of Sections 2B, 2C and 3B in Figure 3.4.5 (b). To account for the width of a graph line and hence of a video pulse, the number of marker pulses occurring during video pulses is halved. In between video pulses, each marker pulse increments the Y - counter content by one. This means that at time T_{11} the contents of the marker pulse counter (Y - counter) contains, in hundredths of an inch the distance between the mid-points of two video pulses.

During the occurrence of a video pulse the marker frequency is halved by means of FFB1. The clock pulse (CP) input to this flip-flop consists of the markers. The video pulses serve as the K_1 and J_1 inputs. The J_2 input is the ALLOWABLE SCAN - i.e., waveform g in Figure 3.4.6. The inverting inputs - K' and J' are kept at ground (logical 0) and K_2 is maintained high. Therefore whenever both J and K are high, that is when video pulses occur and waveform g is a logical 1, the frequency of the Q and Q' outputs of FFB1 is one-half the marker frequency. These outputs are shown as waveforms k and l in Figure 3.4.6. The false output Q'

is used to trigger the POSITIVE-EDGE-TRIGGERED ONE-SHOT B1. The ONE-SHOT output (waveform m), together with the ALLOWABLE SCAN signal are inputs to AND gate B2. Whenever a video pulse occurs the output of AND gate B3 is low because one of its inputs is the inverted video pulse waveform, i.e., waveform o. Thus by time T_{10b} only one pulse has been inputted to the Y - counter via OR GATE B4. During the occurrence of the second video pulse the ONE-SHOT generates, in the same manner, two more pulses as shown in waveform m of Figure 3.4.6. In the timing diagram then, the total contribution to the Y value due to line thickness is three hundredths of an inch. Note however that the total number of marker pulses coincident with video pulses is seven - hence the contribution to Y should be three and a half hundredths of an inch. This means that whenever the sum of the marker pulses occurring coincidentally with the first two video pulses is odd, it is necessary to increase the value of Y contained within the counter by 0.005. This is done by means of FLIP-FLOP B1 (SECTION 1A), POSITIVE-EDGE-TRIGGERED ONE-SHOT B2 (SECTION 5C) and NAND GATE B5 (SECTION 5C) in Figure 3.4.5 (b). Waveform k in Figure 3.4.6 depicts the true output (Q) of FLIP-FLOP B1. If an odd number of marker pulses occurs during the two video pulses the true output of FFB1 at time T_{11} is high. The true output of FFB1, along with the output of ONE-SHOT B2 are fed into NAND GATE B5. Recall that from ONE-SHOT B2 is derived a pulse at time T_{11}, on the negative-going edge of the second video pulse. Hence if Q of FFB1 is high at time T_{11}, the output of NAND GATE B5 consists of a negative - going pulse, as shown in Figure 3.4.6 (y). When the number of marker pulses coincident with the video pulses is even, the true output

of FFB1 is low at time T_{11} and no pulse occurs at the output of NAND GATE B5. The output of NAND GATE B5 serves as a preset input to two flip-flops within the PARALLEL - IN SERIAL - OUT register. As mentioned in Chapter II, it is into this register that are shifted the contents of the X and Y counters. The two flip-flops preset by the output of NAND GATE B5 represent the least significant decimal value of Y. Thus if an odd number of marker pulses occurs in coincidence with the two video pulses the least significant digit of Y (the thousandths digit) is set to 5. Alternately, if the number of marker pulses so occurring is even, then the least significant digit is set to 0. A detailed description of the register is given in Section 3.4.5.

In between two video pulses, $T_{10b} < t < T_{10c}$, each marker pulse increments the Y counter by 1. This is done with FFB2 and GATE B3. The clock pulse input to FFB2 consists of the marker pulses. The K' (inverting) input is the ALLOWABLE SCAN signal. Therefore, K' will be high whenever the ALLOWABLE SCAN is low - the other K inputs being kept at a logical 1. The J_1 and J_2 inputs are the video and ALLOWABLE SCAN pulses respectively. The J' (inverting) input is grounded. Prior to time T_{10} the ALLOWABLE SCAN signal (waveform g) was at a logical 0. Therefore the K input to FFB2 was 1 and J a 0. Since the clock input consists of the marker pulse the true output (Q) then is low at T_{10}. Output Q of FFB2 is set to 1 whenever its J input is high. This occurs during the first video pulse since the ALLOWABLE SCAN signal is also high at that time. The flip-flop may be reset to 0 by the first marker pulse occurring after the ALLOWABLE

SCAN signal has gone low since K then is high and J low. Strictly speaking, this makes the clear input to FFB2 redundant. The true output of FFB2 is shown as waveform n in Figure 3.4.6. AND GATE B3 has as its inputs Q of FFB2, the marker pulses, the ALLOWABLE SCAN signal and the inverted video waveform of Figure 3.4.6 (o). The outputs of gates B3 and B2 go into OR gate B4. The OR gate output is shown in Figure 3.4.6 (p). In this waveform it is seen that 53 marker pulses occurred between video pulses, i.e., at the output of GATE B3, and the contribution at gate B2 was 3 pulses during the occurrence of the video pulses. The contents of the Y counter is therefore 0.56 at time T_{11}.

Recall that at time T_{11}, ONE-SHOT B2 is triggered on the negative-going edge of the second video pulse. The output of the ONE-SHOT is used, in part as a parallel shift pulse, that is, it transfers the contents of the X and Y counters into the PARALLEL-IN - SERIAL-OUT register. In this case an ordinate (Y) value of 0.56 inches is transferred into the register from the Y counter. However, as mentioned earlier, the least significant (thousandths) digit of Y within the register is set to 5 whenever an odd number of marker pulses occurs in coincidence with the two video pulses. In the present example the number of marker pulses so occurring is 7 (odd). The register therefore contains a Y value of 0.565 inches. After the graphical data has been shifted into the register the graphical - to - digital conversion process is then ready to enter its third and final phase - that of punching the contents of the register onto data cards. This is covered in Section 3.4.4.

In Figure 3.4.6 (i) a dotted video pulse is shown occurring at time T_{12}. A previous discussion revealed that this pulse may or may not occur, depending on the sensitivity to which the graph line detection process is preset. The logic described above gives the distance between the first two video pulses occurring in one complete scan. Therefore in Figure 3.4.6 (i) the probable occurrence of a third pulse at T_{12} is redundant in that it has no effect on the Y value.

It is quite possible that at times the sensitivity of the detection process may be set too low or the darkness of graph lines may not be uniform throughout a sample of graph paper. Alternately the sensitivity may be too high and / or the graph may be dirty - yielding false video pulses. To take into account these eventualities an "error - detection" scheme is incorporated into the logic of control B.

The scheme is based on the same principle as the automatic paper advance feature discussed in control A. A count of the number of video pulses in one complete scan is made. If this count is less than two - then corresponding to the particular value of X at which this occurs the value of Y is set to 0. This means that on a data card will be punched the current X value along with a Y value of 0. After this information is punched out the logic is automatically set to the HOLD condition - the reason for this being that the absence of video pulses may also indicate that the entire graph has been read. At this point, if the START key is depressed the paper is advanced, another scan takes place and the punch cycle repeated. A way of overcoming this uncertainty is to measure the length of a graph before entering it into the reader. The last value of X punched out on the data card should then approximately equal this predetermined length.

Whenever more than three video pulses occur in a complete scan the value of Y is set to 9.999 inches and is punched out along with the current X. The logic is not reset to a HOLD condition in this case. It may of course be argued that since the logic of control B gives the distance between the first two video pulses it is possible that the false video outputs due to noise may occur only after the second video pulse and, in this case a meaningful value of Y is discarded. Recall however that with reference to Figure 3.4.4 it was noted that the most sensitive region of the detection process is about point "c", i.e., the middle portion of graph paper. In most instances graph lines will be on either side of this region. Therefore it is more probable that false video outputs occur between the first and second video pulses - representative of the actual graph lines.

The value Y = 0 is selected when less than two video pulses occur since it is assumed that two lines will never meet. Alternately a value 9.999 is attributed to Y when more than three video pulses occur because the maximum possible value of Y is normally 6.100 inches.

To detect the presence of less than two video pulses in a scan the PUNCH " O's" flip-flop (SECTION 3A and B), the UP-TO-3 counter (SECTION 5A) and the NEGATIVE-EDGE-TRIGGERED ONE-SHOT B3 (SECTION 4D) of Figure 3.4.5 (b) are used. The K input to the flip-flop is kept at a logical 0 . Input J_1 is the ALLOWABLE SCAN pulse and J_2 is the false output $Q'_2 1$, of the UP-TO-3 counter. The clear input is derived initially from the STOP key and thereafter from a pulse which occurs every time a card-punch cycle is completed. The UP-TO-3 counter is cleared

once for every drum revolution by the inverted output of ONE-SHOT A1, i.e., waveform f in Figure 3.4.6. The timing diagram of Figure 3.4.7 illustrates how the true output of the PUNCH "O's" FF is set to 1 whenever none, or one video pulse occurs in a scan. The fact that one video pulse may occur at T_{12} in Figure 3.4.7 is of no consequence in this case. Output $Q_2'1$ of the UP-TO-3 counter is at a logical one. The ALLOWABLE SCAN pulse is still a logical one at time T_{12} because, as previously mentioned two video pulses need occur in one scan to set it to zero. Hence at time T_{12} the J input to the flip-flop is high as shown in Figure 3.4.7 (l). The clock input to the flip-flop is obtained from ONE-SHOT B3. The ONE-SHOT is triggered by the output of NAND GATE A7 in control A. The gate has as its inputs the END of SCAN pulse of Figure 3.4.7 (b) and the ALLOWABLE SCAN signal - waveform 3.4.7 (e). The output of this gate is shown as waveform m in Figure 3.4.7 and on its NEGATIVE - GOING edge triggers ONE-SHOT B3. The output of the ONE-SHOT now sets the true output of the PUNCH "0's" FF to 1. Whenever this flip-flop is high the value of Y is set to 0 in the X Y register. A detailed account of this is given in Section 3.4.5 of this chapter. In addition to serving as a clock input to the PUNCH "0's" FF, ONE-SHOT B3 also performs any resetting functions normally done by ONE-SHOT B2, via gate B6 (SECTION 6C) in Figure 3.4.5 (b).

In the timing diagram of Figure 3.4.8 waveform a shows the photo-multiplier output of a noisy scan. The corresponding video output is waveform f. The PUNCH " 9's "FF (SECTION 4A, B) of Figure 3.4.5 (b) has as its clock input the

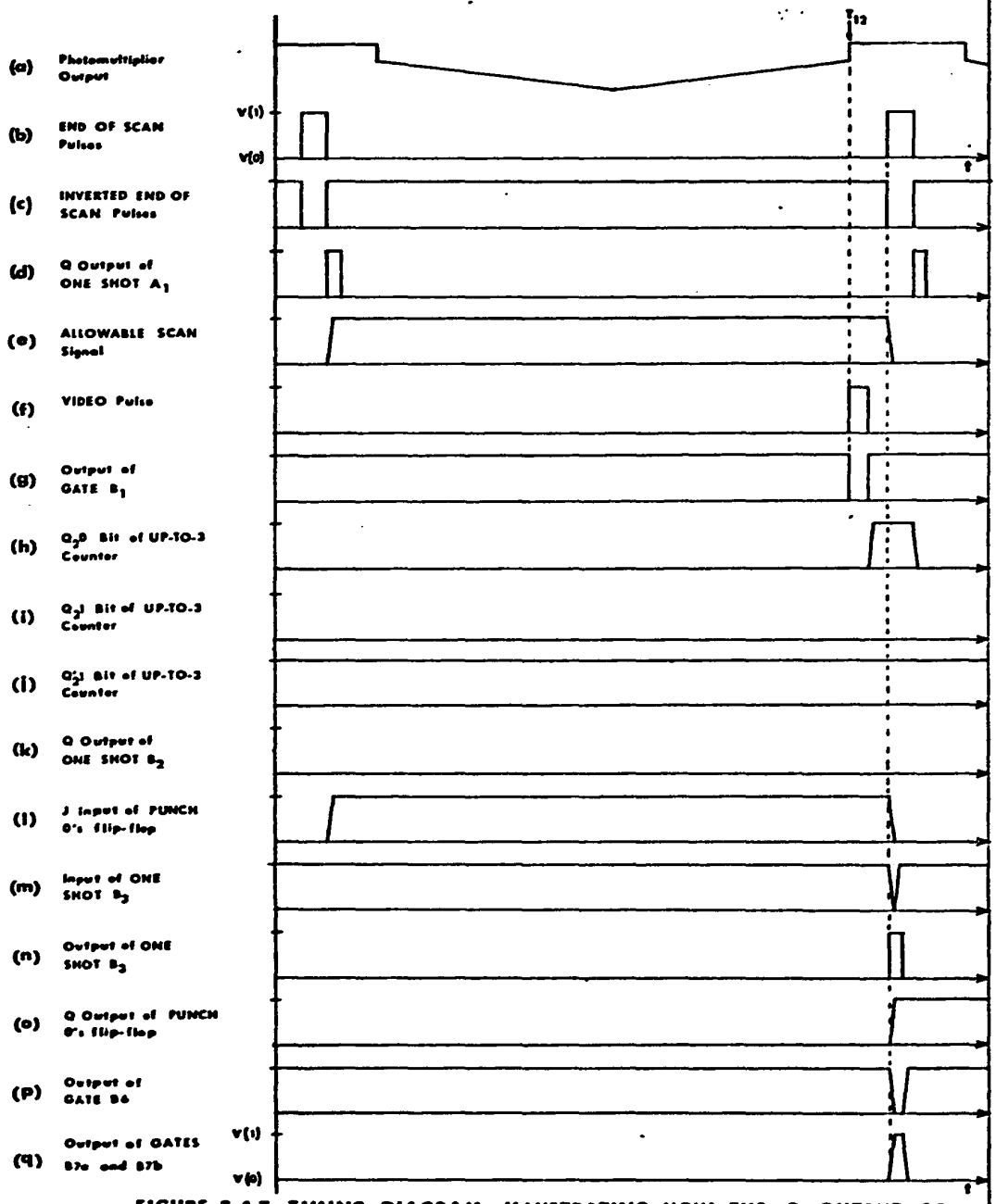


FIGURE 3.4.7, TIMING DIAGRAM ILLUSTRATING HOW THE Q OUTPUT OF THE "PUNCH 0'S" FLIP-FLOP IS SET TO 1 WHENEVER ONE OR LESS VIDEO PULSES OCCUR IN A SINGLE SCAN

NOTE: Voltage levels of waveforms (b) through (q) are as follows: V(0) = 4V
V(1) = 2V

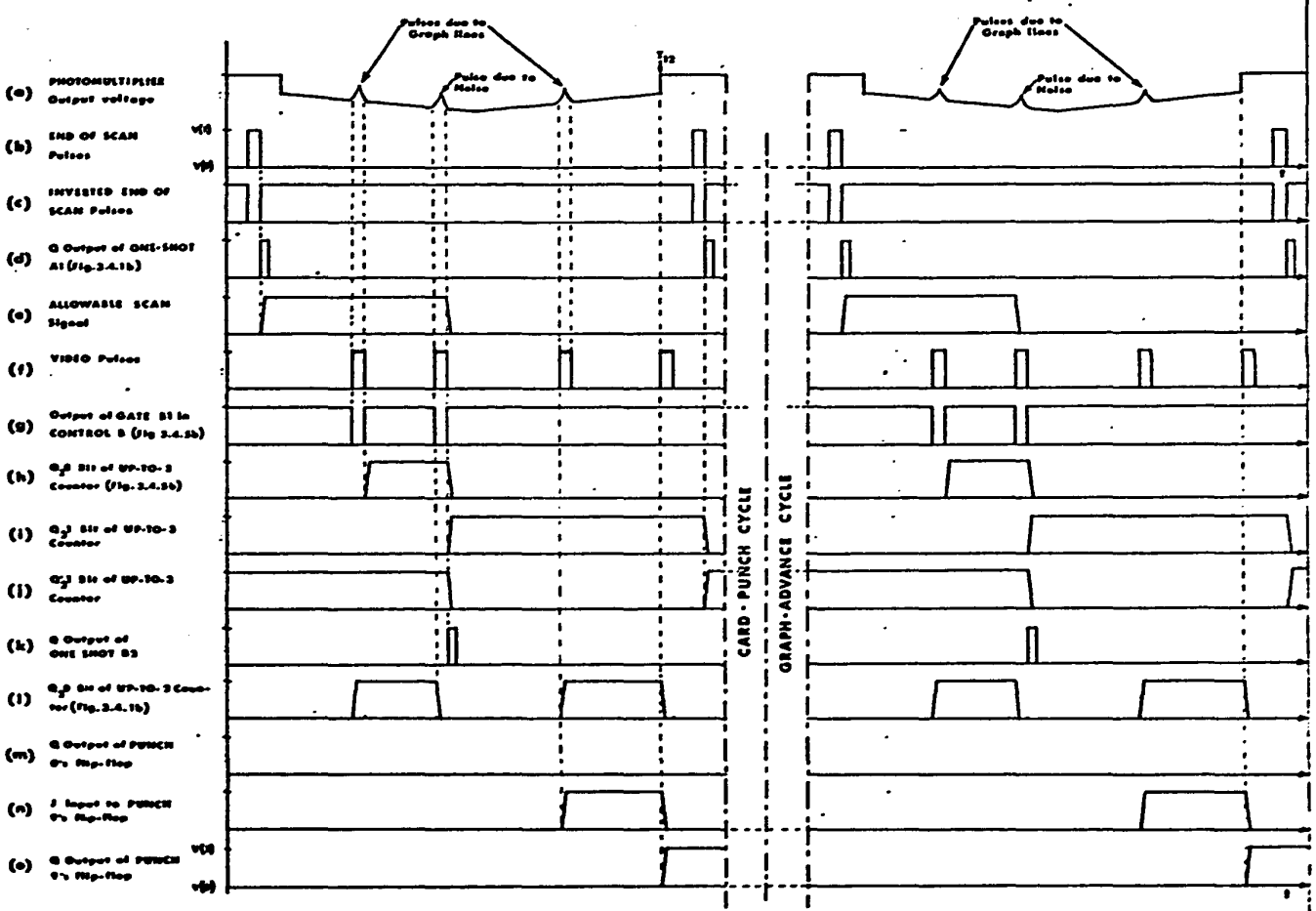


FIGURE 3.4.8. TIMING DIAGRAM ILLUSTRATING HOW THE Q OUTPUT OF THE "PUNCH 9'S" FLIP-FLOP IS SET TO 1 WHENEVER MORE THAN THREE VIDEO PULSES OCCUR IN A SINGLE SCAN

NOTE: Voltage levels of waveforms (b) through (o) are as follows: v(1) = 4V
v(0) = 0V

video pulses and the K input is kept low. Input J_1 consists of the true output $Q_2{}^1$ in the UP-TO-3 counter and is shown in Figure 3.4.8 (i). J_2 is obtained at the $Q_2{}^0$ output of the UP-TO-TWO counter of control A, i.e., waveform l in Figure 3.4.8. Waveform n is then the resulting J input. At T_{12} the fourth video pulse sets the true output of the PUNCH " 9's " flip-flop to 1 . Whenever Q is high the value of Y is set to 9.999 in the X Y register, regardless of what its contents may be prior to time T_{12} . In Figure 3.4.8, it is shown that after the punch and advance cycles are completed the conversion process continues - unlike the case when less than two video pulses occur in one scan, where the logic automatically assumes the HOLD condition upon completing a punch cycle.

3.4.4 Control C

The third and final phase of the graphical-to-digital conversion process involves the transfer of digitized graphical information onto data cards. Since it is primarily through CONTROL C that the actual punching of cards is realized it is expedient here to discuss in pertinent detail the operation of the keypunch machine.

Originally the graph reader was linked to an IBM type 26 keypunch. However, a changeover in keypunches required that the reader be adapted also to a newer model - the IBM 29 .

Since both machines are quite similar in terms of circuitry and hence in basic operation the following discussion, although centered on the IBM 29 may readily be applied to the older model.

3.4.4 (a) The I B M Keypunch Machine

The primary function of a standard IBM keypunch machine is to manually transcribe data, in the form of punched holes, onto IBM cards.

Before any punching can take place a data card must be fed into position at a PUNCH STATION in the machine. Normally a stack of cards is placed into a hopper, as shown in Figure 3.4.9. A FEED key is then depressed, thus initiating a CARD-FEED cycle. The FEED key completes a circuit to a CARD FEED CLUTCH magnet in Figure 3.4.10. When the magnet is energized a "dog" unlatches from the magnet-armature tip. The dog then drops into a tooth of a continuously running ratchet. This turns with the ratchet and rotates a card-feed drive mechanism. The CARD-FEED CLUTCH makes one revolution and then latches up if the magnet is not re-energized. During this cycle the feed mechanism transfers one data card from the hopper into POSITION 2 of Figure 3.4.9. To advance the card to the normal punch position, that being POSITION 4 the FEED key is again depressed. During this second feed cycle the card is transferred to the punch position ; a second card is drawn from the hopper and set into POSITION 2. The lower edge of the card in POSITION 4 presses against a CARD LEVER switch and thus causes it to close. A camshaft, part of the FEED mechanism, in making one revolution during each feed cycle operates a set of contacts. One of the cams, CF 3 in the schematic of Figure 3.4.11, closes its contact after the camshaft has revolved 75° and re-opens it at 285°. Therefore, during the second feed cycle, when the card in position 4 closes the DETAIL CARD LEVER switch, the contact actuated by CF 3 completes a circuit

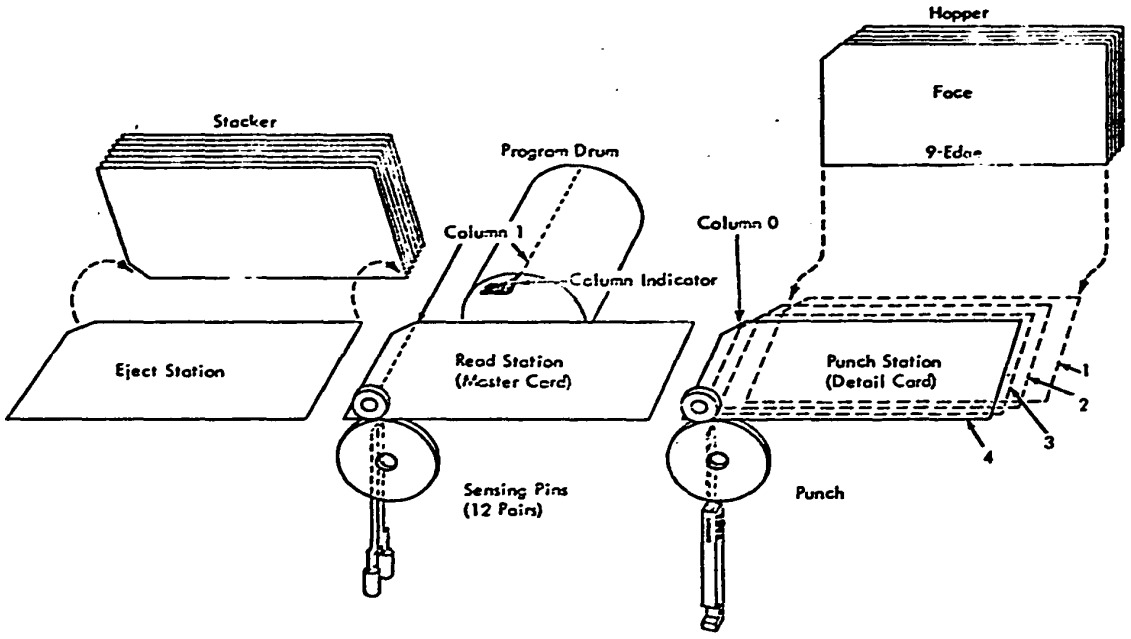


FIGURE 3.4.9. REGISTRATION AND CARD PATH THROUGH MACHINE.

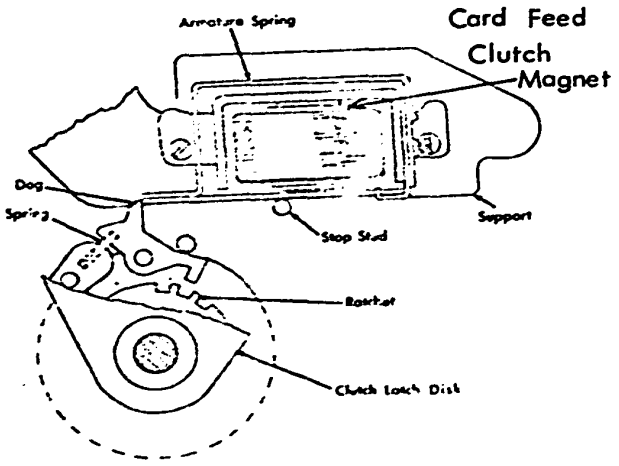


FIGURE 3.4.10. CARD-FEED CLUTCH ASSEMBLY.

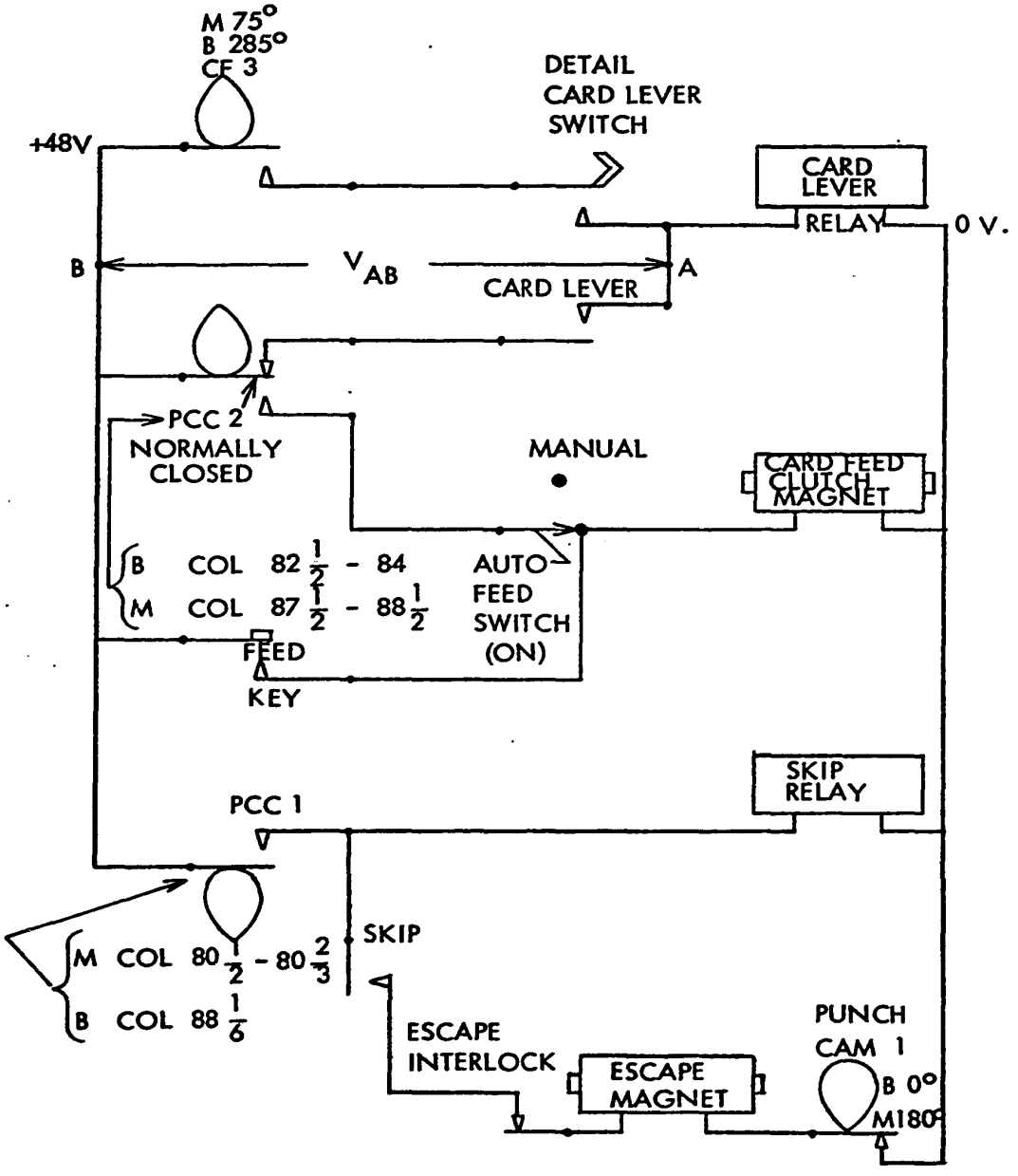


FIGURE 3.4.11. CARD - FEED CIRCUIT OF THE I B M 29 KEYPUNCH.

to energize the CARD LEVER relay in Figure 3.4.11. An interlock, via a normally open CARD LEVER relay contact keeps the relay energized through the normally closed contact PCC2. When the CARD LEVER relay is energized the PUNCH mechanism is enabled.

As each column of a card is punched, a PROGRAM DRUM (Figure 3.4.9) rotates by the equivalent of one card column. The circumference of this drum is such that it comprises the equivalent of 88 columns of a standard data card. This means that to completely envelope the periphery of the drum an "imaginary" 88 column card need be affixed along its circumference.

The drum basically performs three functions :

(1) Together with a column indicator (Figure 3.4.9), it designates the number of the column which will next be punched when the punch mechanism is activated.

(2) The keypunch machine may be set under "program control". This is done by punching onto a data card a specified code and then affixing it to the drum. A set of STAR WHEEL contacts is then lowered onto the drum. As the drum rotates while a card is being punched the STAR WHEELS sense the code on the program card. One example of program control is the automatic skipping of certain columns of a card. When the STAR WHEELS sense a skip code, the keypunch automatically skips through the corresponding columns of the card at the PUNCH STATION.

(3) When the last column (80) of the card at the PUNCH STATION is punched a cam on the PROGRAM DRUM, shown in Figure 3.4.12 operates a set of PROGRAM-CAM contacts : PCC 1 and PCC 2 . PCC1, shown in the schematic of Figure 3.4.13 makes at about column $80\frac{1}{2}$ along the rotating PROGRAM DRUM and energizes a SKIP relay. A SKIP contact then completes a circuit through PCC 1 and the normally closed ESCAPE INTER-LOCK and PUNCH CAM NO. 1 contacts to energize an ESCAPE MAGNET. The armature of the ESCAPE MAGNET, shown in Figure 3.4.14 normally rests within a tooth of an ESCAPE WHEEL, also shown in the figure and thus prevents it from rotating. When the magnet is energized its armature is released from the tooth and the ESCAPE WHEEL rotates. The wheel is geared to the PROGRAM DRUM and to the CARD FEED wheels. As each tooth on the ESCAPE WHEEL moves past the ESCAPE MAGNET armature tip the PROGRAM DRUM rotates by the equivalent of one column of a card. When the DRUM rotates to the equivalent of column $82\frac{1}{2}$ along its circumference the PROGRAM CAM operates PCC 2. This completes a circuit, through an AUTOMATIC FEED switch to the CARD FEED CLUTCH magnet in Figure 3.4.11 and therefore automatically initiates a CARD FEED

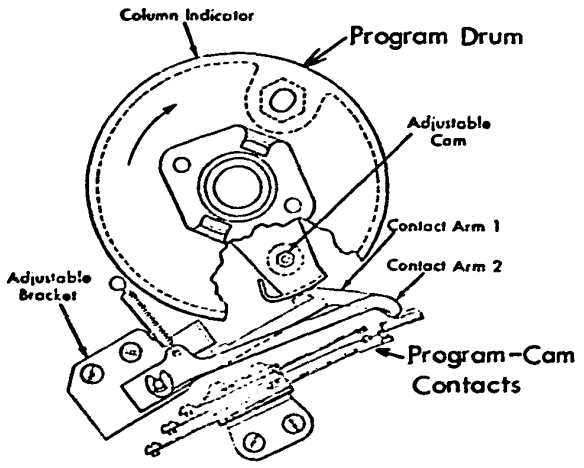


FIGURE 3.4.12. PROGRAM-CAM CONTACTS

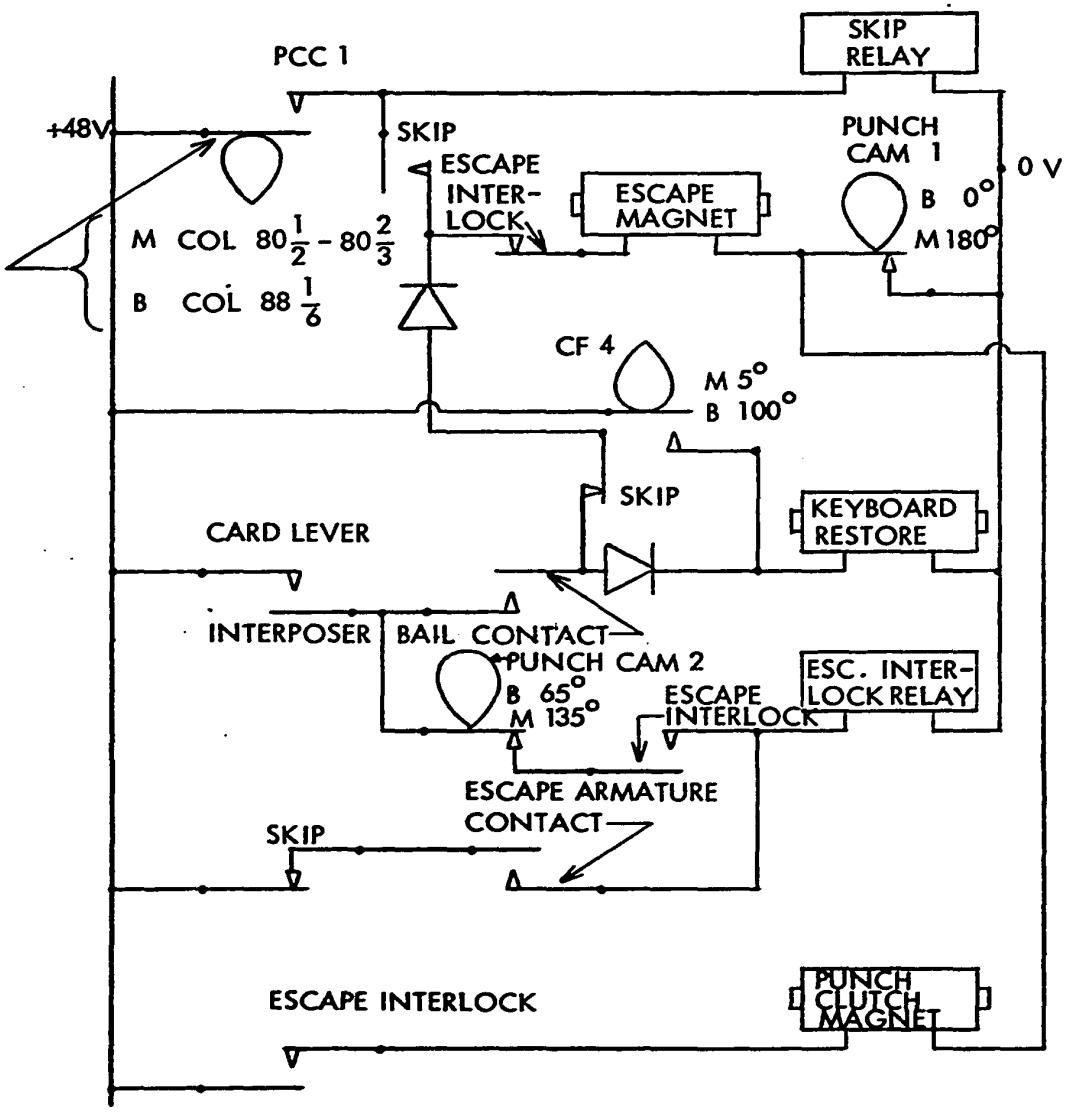


FIGURE 3.4.13. CARD-PUNCH CIRCUIT OF I B M 29 KEYPUNCH.

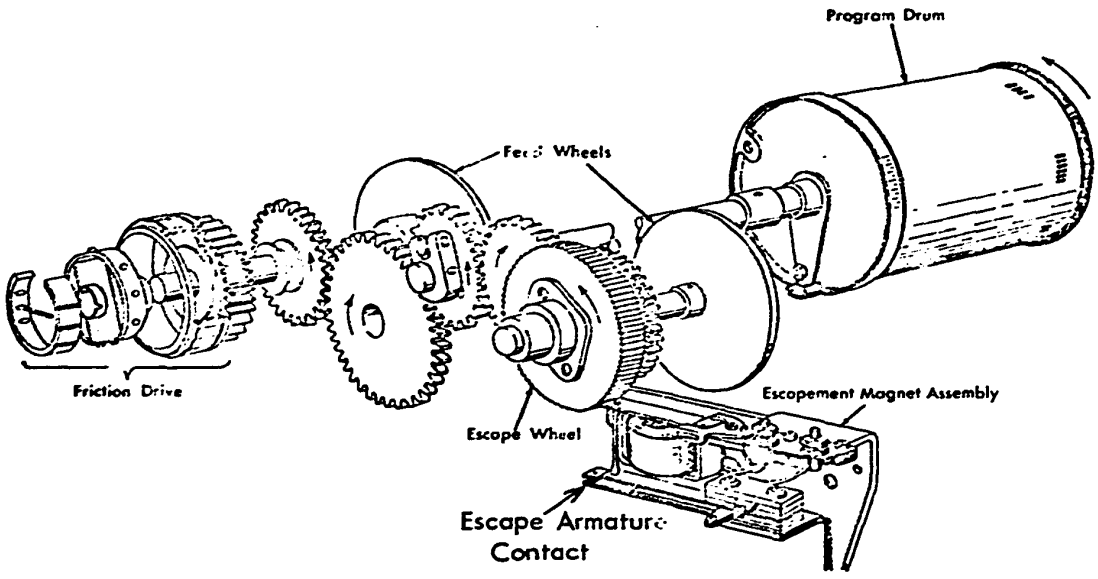


FIGURE 3.4.14. FRICTION DRIVE TO ESCAPEMENT.

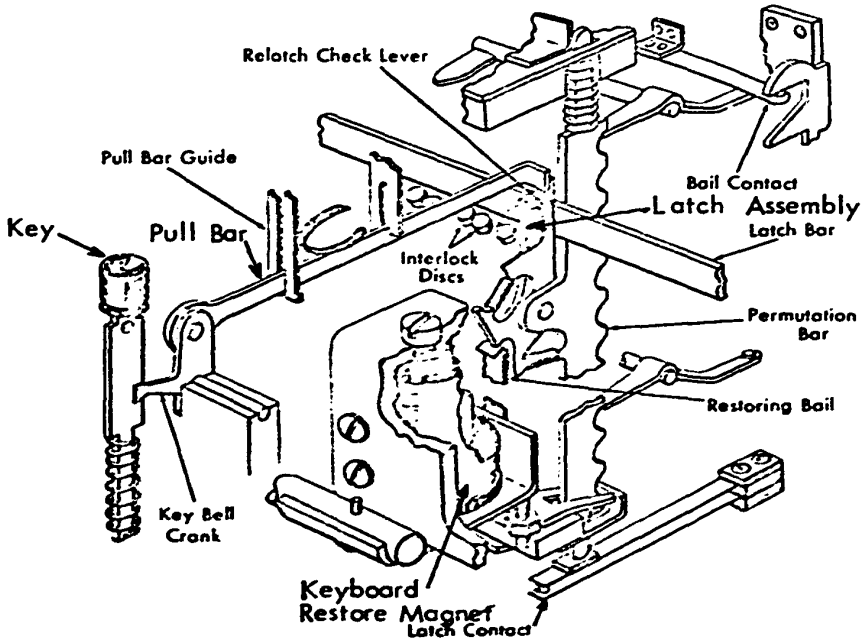


FIGURE 3.4.15. KEYBOARD OPERATION.

cycle. When PCC 2 is operated the CARD LEVER relay is de-energized and therefore inhibits any card punching from taking place during this part of the FEED cycle. At about column 88 along the rotating PROGRAM DRUM the PROGRAM CAM contacts are restored to their normal state - i.e., PCC 1 opens and PCC 2 closes. The armature of the ESCAPE magnet then relatches into a tooth on the ESCAPE wheel and stops the PROGRAM DRUM in column 1 - that is, the column indicator points to column 1 in Figure 3.4.9. During this automatic feed cycle, the punched card leaves the PUNCH STATION and enters the READ STATION (Figure 3.4.9). The card previously in POSITION 2 is transferred to POSITION 4 and a new card is moved from the hopper to POSITION 2. The movement of cards at the PUNCH STATION keeps the DETAIL CARD LEVER switch closed. Therefore the CARD LEVER relay is re-energized by CF 3 while the card is moved from the hopper and into POSITION 2. This enables the punch mechanism.

The automatic feed cycle inhibits the punching mechanism for 0.25 seconds. This is the time required to exit the punched card from the PUNCH STATION and transfer a new card from POSITION 2 to POSITION 4.

To initiate a PUNCH cycle and hence punch a column of a data card a key on the ALPHA / NUMERIC keyboard of the keypunch is depressed. The key mechanism is shown in Figure 3.4.15. When the key is depressed the pull bar disengages the latch assembly from a fixed latch bar. This action drops a permutation bar onto a LATCH CONTACT, causing it to close. The permutation bar, in dropping, also operates a lever which in turn closes a keyboard BAIL CONTACT.

When the data to be punched consists of numbers only, the closure of a latch contact completes a circuit and energizes one INTERPOSER magnet, shown in Figure 3.4.16 and in the schematic of Figure 3.4.17. This causes a PUNCH INTERPOSER to unlatch from a notch on the armature of the INTERPOSER magnet. A spring enables the PUNCH INTERPOSER to lift the INTERPOSER BAIL and, at the same time to latch onto the PUNCH BAIL, thus positioning it onto the PUNCH OPERATING CAMS. The upward movement of the INTERPOSER BAIL closes the INTERPOSER BAIL CONTACTS. This closure completes two circuits, as shown in the schematic of Figure 3.4.13. One circuit energizes the KEYBOARD RESTORE MAGNET. A RESTORING BAIL coupled to the armature drives the keyboard LATCH ASSEMBLY and PERMUTATION BAR back onto the LATCH BAR. If the key is held depressed while this happens a RELATCH CHECK LEVER prevents the PULL BAR from relatching onto the LATCH ASSEMBLY. This implies that if a key is depressed and held in that position only one column of a card is punched. When the key is released the PULL BAR relatches onto the LATCH ASSEMBLY. The other circuit provides an impulse to the ESCAPE magnet. This is done through three normally-closed contacts : a SKIP contact, an ESCAPE INTERLOCK contact and the PUNCH CAM No. 1 contact. Recall that when the ESCAPE magnet is energized its armature unlatches from a tooth of the ESCAPE wheel, causing it to rotate. Here the ESCAPE magnet is so impulsed that its armature relatches into the next tooth of the ESCAPE wheel. This means that the PROGRAM DRUM and the data card in the PUNCH STATION advance by only one column. In addition the ESCAPE magnet armature closes the ESCAPE ARMATURE CONTACT thus energizing an ESCAPE INTERLOCK relay. The relay stays energized

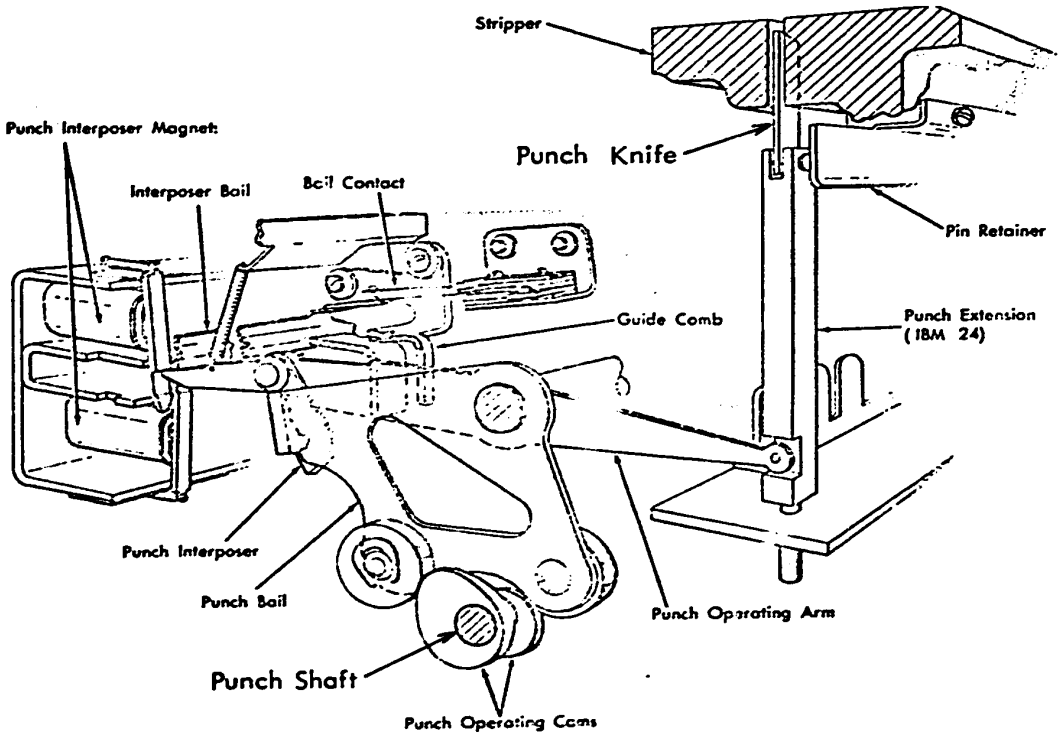


FIGURE 3.4.16. PUNCH OPERATION.

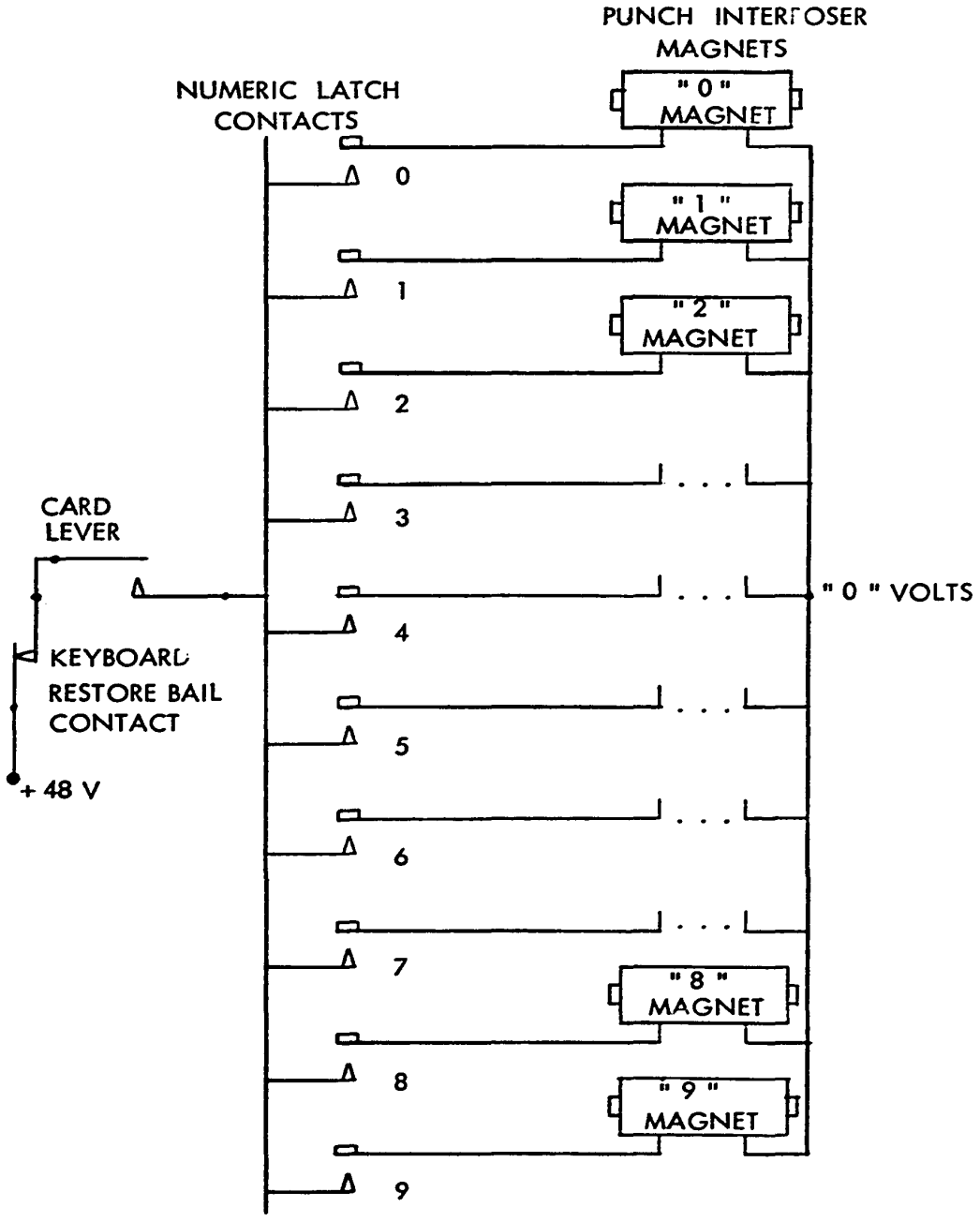


FIGURE 3.4.17. SCHEMATIC OF THE KEYBOARD LATCH CONTACTS AND INTERPOSER MAGNETS IN THE I B M KEYPUNCH.

via its ESCAPE INTERLOCK contact and the normally-closed PUNCH CAM No. 2 contact. The ESCAPE MAGNET is then de-energized because the normally-closed ESCAPE INTERLOCK contact in series with it is now open. Another normally- open ESCAPE INTERLOCK contact completes a circuit to the PUNCH CLUTCH mechanism shown in Figure 3.4.18.

The armature of the PUNCH CLUTCH magnet unlatches from a step on the CLUTCH SLEEVE. This action couples the CLUTCH SPRING to the continuously rotating DRIVE PULLEY and DRIVE SLEEVE thus causing the PUNCH SHAFT to rotate. A PUNCH OPERATING CAM on the PUNCH SHAFT then drives the PUNCH BAIL in Figure 3.4.16, moving the PUNCH OPERATING ARM and PUNCH KNIFE up, punching a hole in a card column. As the PUNCH SHAFT rotates, two other cams on the shaft - PUNCH CAMS No. 1 and No. 2 (Figure 3.4.13) operate their normally closed contacts. CAM No. 1 opens its contact at 0°, i.e., as soon as the PUNCH SHAFT starts rotating and hence de-energizes the PUNCH CLUTCH magnet. At 65° PUNCH CAM No. 2 opens its contact and de-energizes the ESCAPE INTERLOCK RELAY. While the PUNCH SHAFT completes one revolution the remainder of the PUNCH MECHANISM is restored back to its normal state.

The punch cycle time is 100 milliseconds for the I B M 26 and 56 milliseconds for the I B M 29 .

The I B M punch code is such that in order to represent an alphabetic character on a card, two holes or more, must be punched in one column. A special symbol, for example the plus (+) sign requires three holes in a column. To punch two holes in one

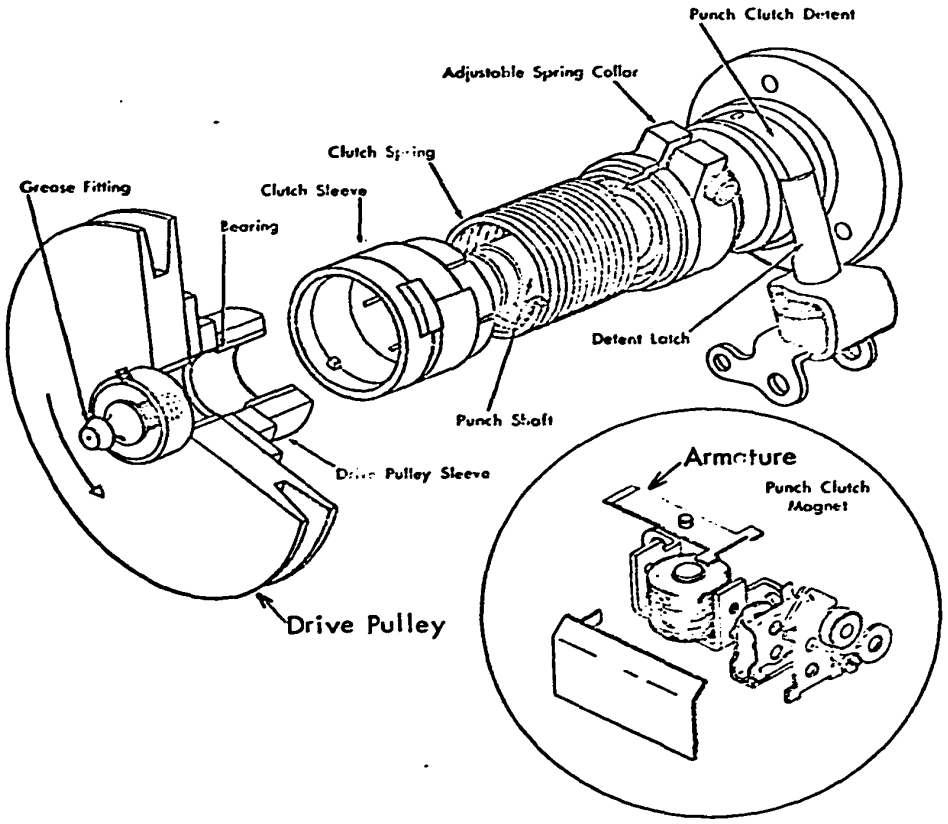


FIGURE 3.4.18. PUNCH - CLUTCH ASSEMBLY.

column, two INTERPOSER magnets need be energized, and so on. When non-numerical characters are punched a combination of keyboard LATCH CONTACTS and keyboard BAIL CONTACTS act to energize more than one INTERPOSER MAGNET. However, as previously mentioned, the punching of numerical data requires only the closure of LATCH CONTACTS. When numerical data is punched manually a NUMERIC key is held depressed while the ALPHA/NUMERIC keys are being depressed. The numeric key simply breaks a circuit common to all keyboard BAIL CONTACTS. The LATCH CONTACTS together with the INTERPOSER magnets used in NUMERIC punching are shown in the schematic of Figure 3.4.17. Note the CARD LEVER and KEYBOARD RESTORE contacts. The former inhibits punching during CARD FEED cycles and the latter - part of the KEYBOARD RESTORE magnet assembly inhibits punching when the RESTORE magnet is energized.

3.4.4 (b) The Automatic Punching of Data Cards

To apply the keypunch in a process where data is to be punched automatically the timing inherent in the two basic keypunch operations - those of punching and feeding is significant. The duration of a punch cycle limits the rate at which successive columns of a card may be punched. During a feed cycle, the punch mechanism is restricted. Furthermore, the feed time is greater than the punch cycle time. This means that if data is to be automatically punched at approximately the maximum punch rate - the data flow must be interrupted during a feed cycle in order to prevent any loss of information.

It has been shown that numeric punching is normally initiated by depressing a key and hence closing a LATCH contact. Once the contact closes the punch cycle "automatically" ensues. Therefore by paralleling each LATCH contact with the normally open contacts of ten relays and then activating a set of these in sequence a group of numbers may be transferred onto cards. In the process the keyboard keys are not disturbed and therefore the keyboard bail contacts do not close. This means that only one interposer magnet is energized at a time and no multiple punching (alphabetic) takes place. However, to prevent more than one column from being punched when a LATCH contact is shorted in this manner the contact closure time must be equal to, or less than the punch cycle time.

In two instances the transfer of data onto cards need be inhibited : (1) When the card supply at the keypunch is exhausted and (2) while the keypunch is in an automatic card-feed cycle. Since in this case numerical data is being fed from the logic unit of the graph reader an inhibiting signal - compatible with this unit must be derived from the keypunch. The signal is obtained by monitoring the voltage V_{AB} in Figure 3.4.11. V_{AB} is 0 volts when the CARD LEVER relay is energized and - 48 volts otherwise. A zero voltage indicates that the keypunch is ready in that a data card is in the PUNCH POSITION. A voltage of - 48 volts signifies either the absence of a card at the PUNCH STATION or a card - feed cycle. To make the keypunch logic levels compatible with those of the graph reader a special circuit is used. This circuit, fully discussed in Section 3.4.6 (a), also filters out any noise introduced by contact bounce and the inductance of the CARD LEVER coil. The input and output waveforms of the circuit are shown in Figure 3.4.19. The delays d_1 and d_2 are due to the filtering action incorporated into the circuit.

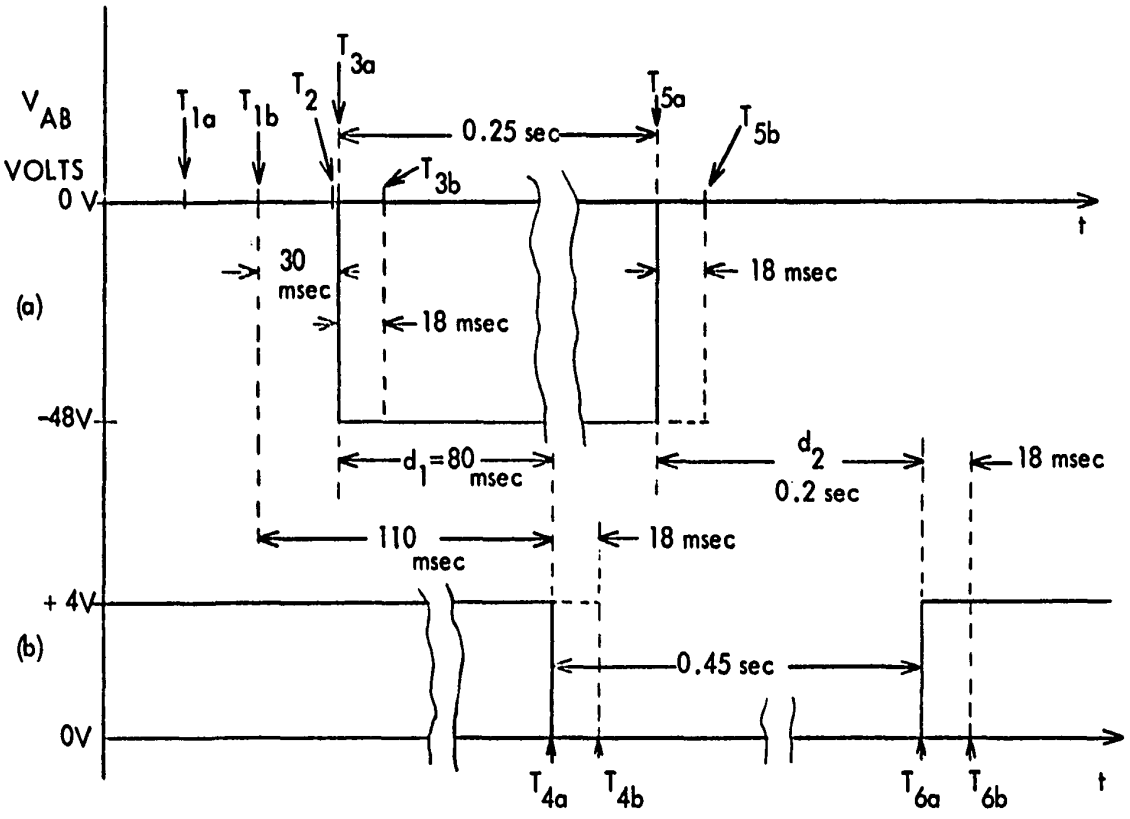


FIGURE 3.4.19 (a) . WAVEFORM OF VOLTAGE V_{AB} .

FIGURE 3.4.19 (b). OUTPUT VOLTAGE OF LEVEL-TRANSFORMING CIRCUIT.

In Figure 3.4.19 (a) time T_{1a} represents the initiation of a PUNCH cycle in column 80, ending 56 milliseconds later at T_2. Approximately half way through the cycle, at T_{1b} PUNCH CAM No. 1 re-closes its normally closed contact in the schematic of Figure 3. 4.13. Program Cam Contact 1 (PCC1) closes its contact in Column 80 ($80\frac{1}{2} - 80\frac{2}{3}$), energizing the SKIP relay. The ESCAPE magnet is therefore then energized. The ESCAPE wheel rotates past the ESCAPE magnet armature at the rate of 12 milliseconds per tooth. Therefore Program Cam Contact 2 (PCC 2), which breaks between columns $82\frac{1}{2}$ and 84, or 30 and 48 milliseconds after the ESCAPE magnet is energized, causes voltage V_{AB} to go to -48 volts at T_{3a} or T_{3b} in Figure 3.4.19 (a). The voltage level transforming circuit has here a delay (d_1) of 80 milliseconds. Therefore it drops from a logical 1 to a 0 at T_{4a} or T_{4b}, in Figure 3.4.19 (b). At T_{5a} or T_{5b}, 0.25 seconds later, Card Feed Cam (CF 3) closes, and through the DETAIL CARD lever switch (Figure 3.4.11) energizes the CARD LEVER relay. This brings V_{AB} back to 0 volts. Note that in going from a logical 0 to a logical 1 the level transforming circuit has a delay (d_2) of 0.2 seconds.

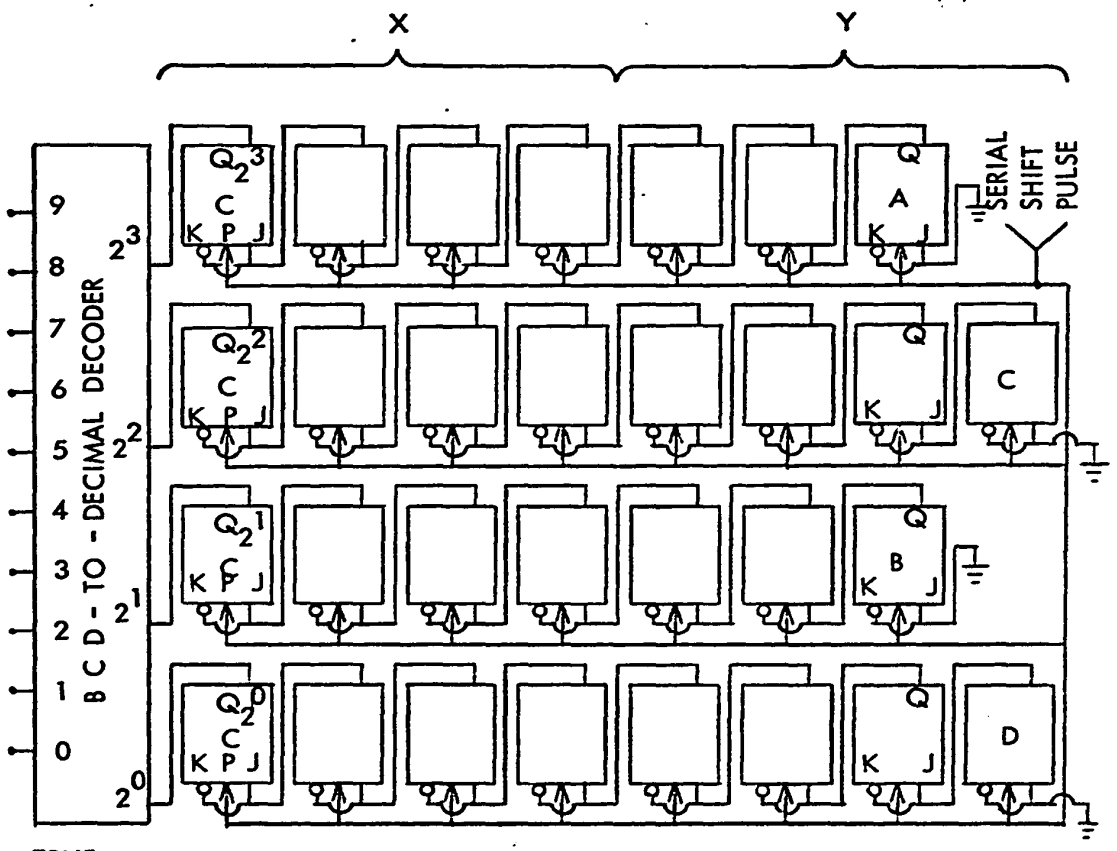
3.4.4 (c) The Logic of Control C

In the discussion on Control B is shown how a set of X and Y values is obtained and stored in a PARALLEL - IN - SERIAL - OUT register. A detailed discussion of this register is given in Section 3.4.5. For the present purposes only the

the simplified version as depicted in Figure 3.4.20 is necessary. In the figure it is assumed that a particular scan yields an X value of 9138 millimetres and a Y value of 5.865 inches. Recall that data is loaded into the register by means of a pulse derived from the negative going edge of the second video pulse. This so-called PARALLEL - SHIFT pulse simply transfers the contents of the X and Y counters into the register. The true outputs of each flip-flop after the occurrence of a PARALLEL - SHIFT pulse are included in the figure, along with their decimal equivalents. Each decimal digit is stored in binary - coded - decimal (BCD) form. The first sixteen flip - flops from left to right contain the value of X, and the remaining fourteen flip - flops, Y . The latter portion of the register requires only fourteen flip-flops (instead of sixteen) because the least significant (thousandths) digit of Y resulting from any scan of a graph is either 0 or 5. Therefore only two flip - flops are required to store this digit in BCD form. Recall that the thousandths digit of Y is set to 0 if an even number of marker pulses occurs coincidentally with two video pulses and to 5 if the number of markers so occurring is odd.

The true outputs of the flip-flops representing the most significant value of X are connected to a BINARY - CODED - DECIMAL (BCD) - TO - DECIMAL decoder. After the parallel shift pulse occurs output 9 of the decoder is at a logical 0, with the remaining decimal outputs (0 through 8) high. Eight alternate punch and shift cycles now take place - that is, the number 9 is first punched in a data card column and then the register contents is shifted left by a serial shift pulse. Line 1 of the decoder output is low after the occurrence of the first serial-

FIGURE 3.4.20. SERIAL SHIFTING OF DATA IN PARALLEL-IN-SERIAL-OUT REGISTER.



DECODER OUTPUT AFTER PARALLEL-SHIFT PULSE	TRUE FLIP-FLOP OUTPUTS	CONTENTS OF REGISTER AFTER PARALLEL SHIFT PULSE							
9	Q_2^3	1	0	0	1	0	1	0	0
	Q_2^2	0	0	0	0	1	0	1	1
	Q_2^1	0	0	1	0	0	0	1	0
	Q_2^0	1	1	1	0	1	0	0	1
	DECIMAL EQUIVALENT	9	1	3	8	5	8	6	5

← SERIAL DATA SHIFT

DECODER OUTPUT AFTER FIRST SERIAL-SHIFT PULSE		CONTENTS OF REGISTER AFTER FIRST SERIAL SHIFT PULSE							
1	Q_2^3	0	0	1	0	1	0	0	0
	Q_2^2	0	0	0	1	0	1	1	0
	Q_2^1	0	1	0	0	0	1	0	0
	Q_2^0	1	1	0	1	0	0	1	0
	DECIMAL EQUIVALENT	1	3	8	5	8	6	5	0

shift pulse. The number 1 is then punched in the next column, and so on - until all eight decimal digits representing an X - Y set are transferred onto 8 columns of a card. This permits ten sets of X - Y values to be punched on a standard 80 - column data card.

Strictly speaking only 7 serial shifts are necessary to punch out 8 decimal digits. An eighth pulse is included so that the register may be left completely cleared after each set of X and Y values is punched on a card. The clearing is done by means of flip-flops A, B, C and D in Figure 3.4.20, where the J inputs and the inverting K inputs are connected to ground. Therefore J is a logical 0 and K a logical 1. The first serial shift pulse sets these four flip-flops to 0. Each successive pulse thereafter simply shifts this set of zeros to the left and therefore after the eighth pulse the whole register contains zeros.

Punch and shift operations are regulated by the circuitry of Control C, shown in Figure 3.4.21 (a). The operation of Control C is explained by means of the simplified circuit diagram of Figure 3.4.21 (b) along with the timing diagram of Figure 3.4.22.

In the timing diagram waveform (a) depicts the output of ONE-SHOT A1. Recall that from this are derived the stepping motor pulses which advance a sample of graph paper by a preset amount. On the negative-going edge of the last stepping - motor - pulse, i.e., at T_{10} in Figure 3.4.22, the ALLOWABLE SCAN signal (waveform (e)) and the true output of flip-flop A 4 in Control A (waveform (f)) go high. The Y value of a graph is obtained when the ALLOWABLE -SCAN signal is high. On

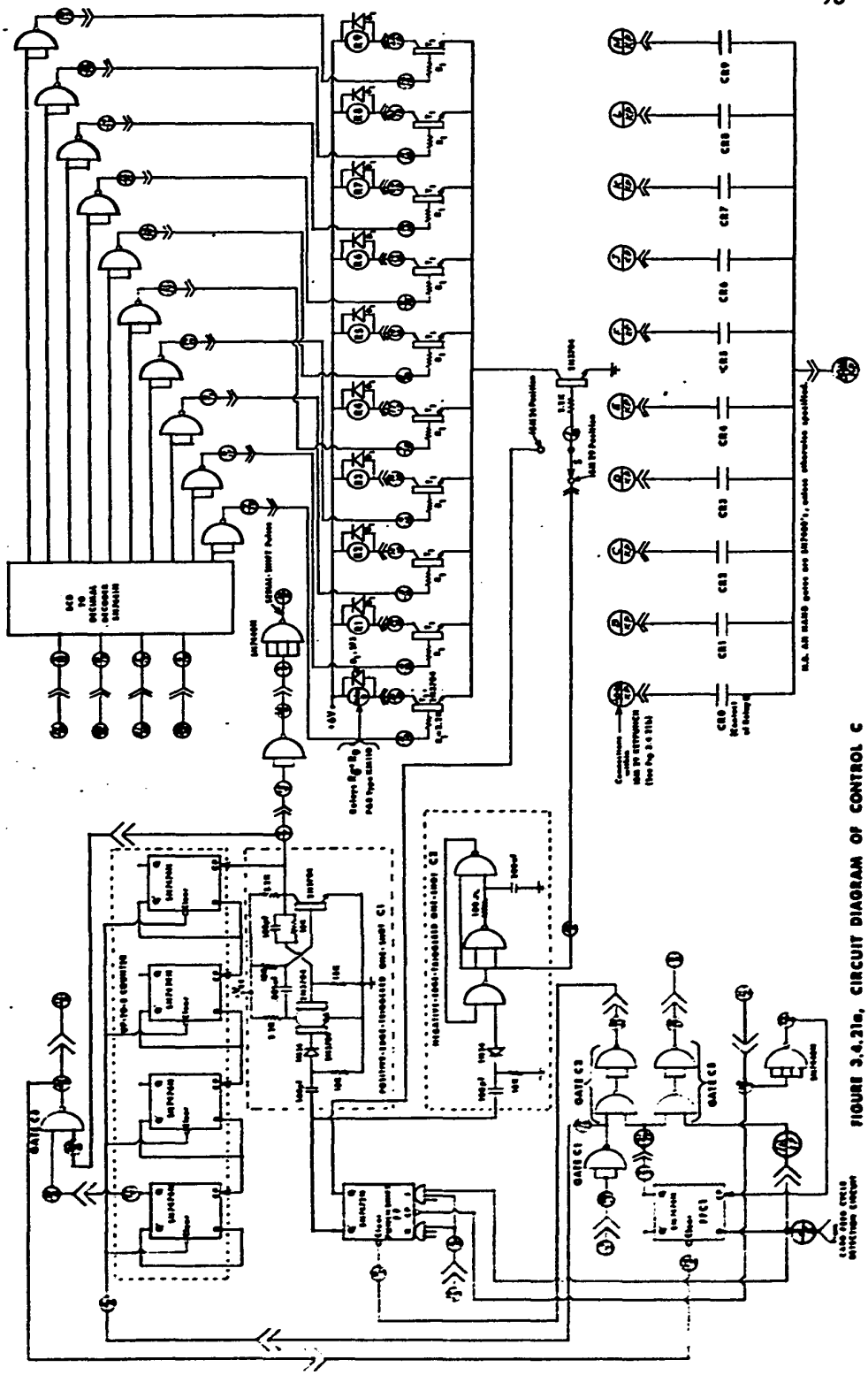


FIGURE 3.4.21a, CIRCUIT DIAGRAM OF CONTROL C

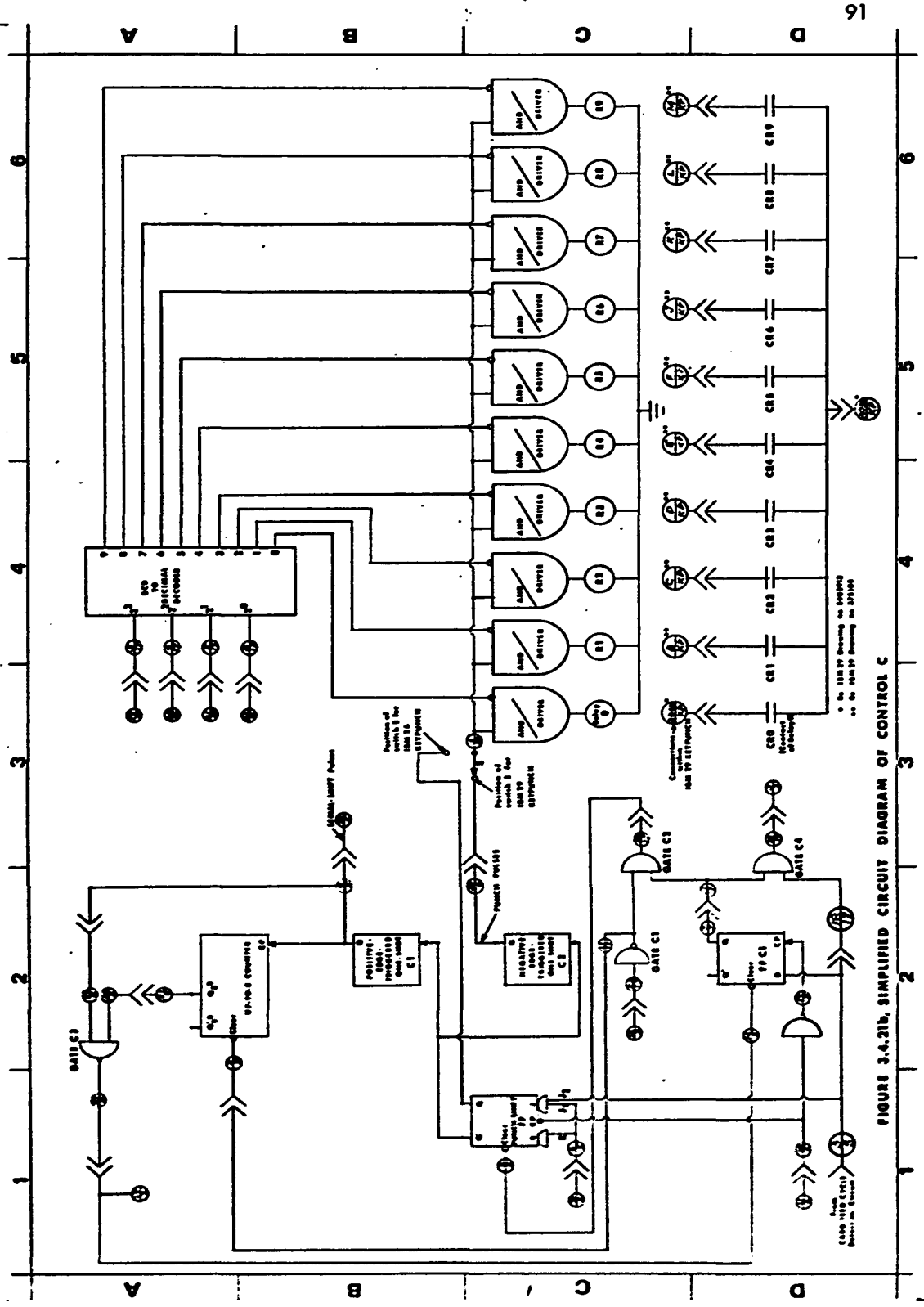


FIGURE 3.4.21b, SIMPLIFIED CIRCUIT DIAGRAM OF CONTROL C

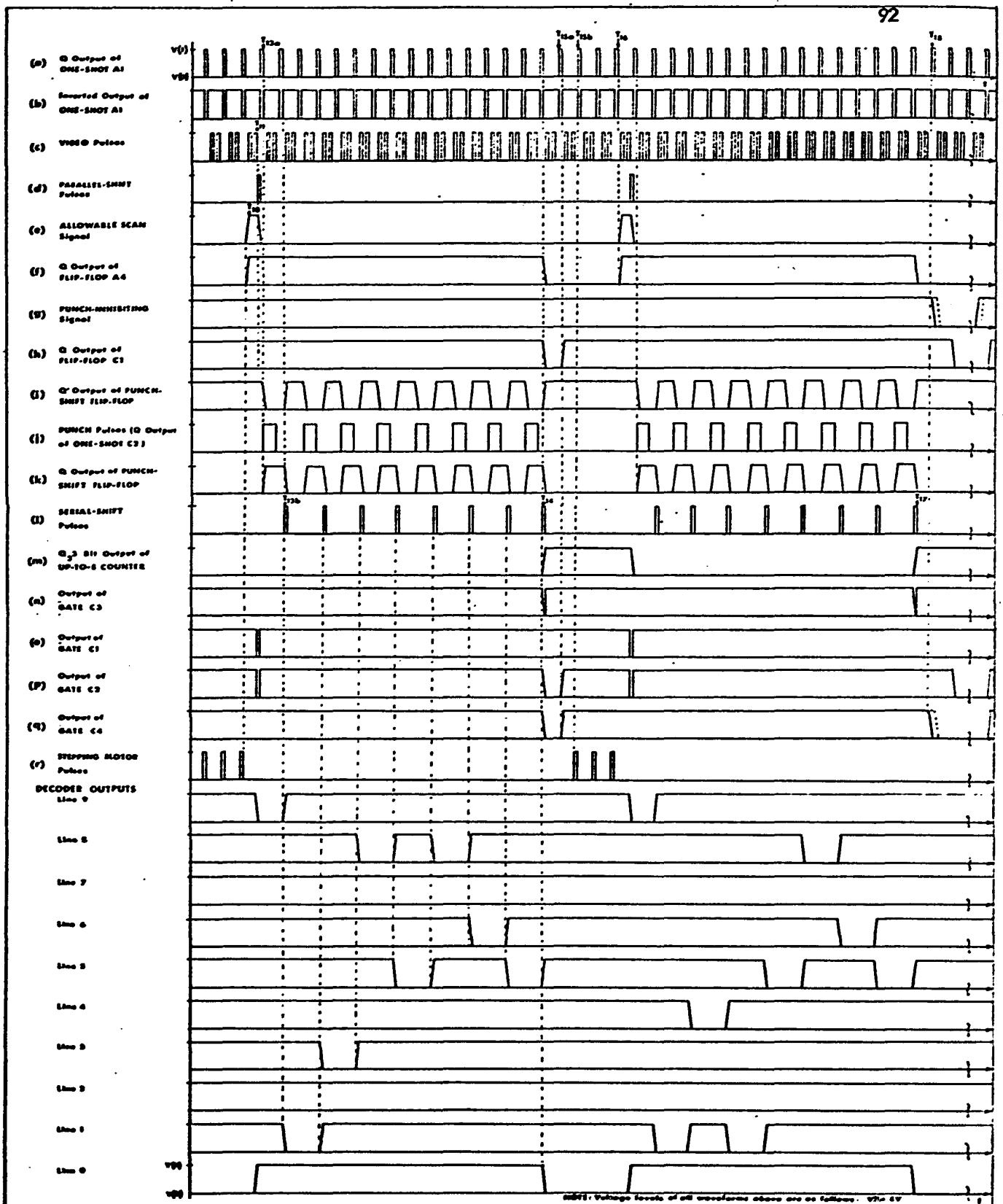


FIGURE 3.4.22. TIMING DIAGRAM OF CONTROL C

the negative-going edge of the second video pulse (waveform (c)) the parallel shift pulse is generated (waveform (d)). This pulse transfers the contents of the X and Y counters into the register of Figure 3.4.20. In addition, from the parallel-shift pulse is derived the reset input to an UP - TO - 8 counter (SECTION 2 A) and the PUNCH-SHIFT flip-flop (SECTION 1 C) of Figure 3.4.21 (b). The output of GATE C 1 (SECTION 2 C) is applied to the reset input of the counter. The input to the gate is obtained from Control A, GATE A 6 , and is high during the occurrence of a parallel-shift pulse or when the STOP key is depressed. The PUNCH-SHIFT flip-flop is reset by the output of AND GATE C 2 (SECTION 2 C). One input of GATE C 2 is the output of GATE C 1 and the other input consists of the true output (Q) of flip-flop C 1 (SECTION 2 D). The Clock Pulse (CP) input to F F C 1 is the inverted output of ONE-SHOT A1 in Figure 3.4.22 (b) and the D input is waveform (g). Waveform (g) is the inhibiting signal derived from the keypunch machine and is high whenever a data card is in the PUNCH STATION. In the timing diagram it is assumed that this is the case. Therefore Q of flip-flop C 1 is high at T_{11}, as shown in Figure 3.4.22 (h). The outputs of GATES C 1 and C 2 are waveforms (o) and (p) respectively.

The clock input to the PUNCH-SHIFT flip-flop is the Q output of ONE-SHOT A1. The K and J_1 inputs consist of the true output of flip-flop A 4 (waveform (f)). Input J_2 is waveform (g) and the remaining K and J inputs are left high. Therefore K and J are high if Q of F F A 4 is high and the keypunch is ready. Because the output of ONE-SHOT A 1 is inverted at the clock input the

PUNCH-SHIFT flip-flop is triggered at T_{13a} on the negative-going edge of this pulse. For $T_{13a} \leq t \leq T_{14}$ both J and K inputs to the flip-flop are high. Therefore during this time output Q yields waveform (k) in the timing diagram. The false output Q' is applied to two ONE-SHOTS : POSITIVE-EDGE-TRIGGERED-ONE-SHOT C 1 (SECTION 2 B) and a NEGATIVE-EDGE-TRIGGERED ONE-SHOT C2 (SECTION 2 C) . The output of ONE-SHOT C 1 is the SERIAL-SHIFT pulse and is shown in Figure 3.4.22 (l). Waveform (j) represents the output of the NEGATIVE-EDGE-TRIGGERED ONE-SHOT C2 .

With the exception of pulse width waveforms (j) and (k) are similar. The period of each is 152 milliseconds, which is twice the period of the END-OF-SCAN pulse and hence of one revolution of the graph reader drum. The pulse widths of waveforms (j) and (k) are 50 and 76 milliseconds respectively. Waveform (j) is used as the PUNCH PULSE. This means that whenever (j) is high a number is punched in a column of a data card. Switch S in SECTION 3 C of Figure 3.4.21 (b) implies that a PUNCH PULSE may be obtained from either the NEGATIVE-EDGE-TRIGGERED ONE-SHOT C2 or the PUNCH-SHIFT flip-flop. Strictly speaking the switch does not physically exist. It is included in the figure to point out the fact that originally, when an IBM 26 keypunch was used to transfer data onto cards the Q output of the PUNCH-SHIFT flip-flop served as the source of PUNCH PULSES. A changeover of keypunch machines to an IBM 29, with a punch cycle time of only 56 milliseconds required that the PUNCH PULSE be of shorter duration. The ONE-SHOT is used therefore to obtain a PUNCH PULSE of 56 milliseconds duration.

The BCD-TO-DECIMAL decoder of Figure 3.4.20 is redrawn in SECTION 4A, Figure 3.4.21 (b). Each decoder output enters the ten AND/DRIVER stages in the figure and is gated there with the PUNCH-PULSE. When a PUNCH PULSE occurs and one of the decoder outputs is low the driver stage energizes one of ten relay coils (R O → R 9). Each of the normally-open contacts of the relays is connected in parallel with the NUMERIC LATCH contacts in the keypunch.

The decoder outputs for the example cited earlier, i.e., for X = 9138 millimeters and Y = 5.865 inches are shown in the timing diagram. Prior to the occurrence of a parallel shift pulse at T_{11} the "0" output of the decoder is low. This simply means that the register is initially in a cleared state. When the parallel-shift pulse occurs the "9" output goes low, representing the most significant digit of the X value. A PUNCH PULSE occurs at $T_{13a} \leq t < T_{13b}$ and the digit 9 is punched in a card column. The serial shift pulse then occurs at T_{13b} (waveform (l)) and the " 1 " output of the decoder now goes low. Another punch pulse occurs thereafter, and so on.

The UP-TO-8 counter (SECTION 2 A) of Figure 3.4.21 (b) keeps track of the number of serial-shift pulses occurring from T_{13b} through and including T_{14}. At T_{14}, that is at the eighth occurrence of the pulse the Q_2^3 output of the counter goes high, as shown in Figure 3.4.22 (m). This output, together with the serial-shift pulse is gated via NAND GATE C 3 (SECTION 2 A, Figure 3.4.21 (b)). The output of the gate, waveform (n) resets flip-flops C 1 and A 4. Recall that the true output of F F A 4 is used as the J_1 and K input to the PUNCH-SHIFT

flip-flop. Since Q of F F A 4 is set to 0 by the output of GATE C 3, punch pulses are therefore inhibited for $T_{14} \leq t \leq T_{16}$. On the timing diagram then, T_{14} represents the end of a card-punch cycle.

Upon completion of a punch cycle the paper advance mechanism is delayed by 76 milliseconds, that is, by one drum revolution. This means the advance phase is initiated at T_{15b} instead of T_{15a}. The delay is obtained by means of flip-flop C 1 and AND GATE C 4 (SECTION 3 D). The flip-flop is reset to 0 at T_{14}, as previously mentioned. The true output of the gate serves as an input to the 4 - input GATE A 4 in Control A. Whenever the output of GATE C 4 is low, stepping motor pulses are inhibited by GATE A 4. The D - input to flip-flop C 1 is waveform (g) and the clock input waveform (b) in Figure 3.4.22. Since D is high at T_{15a} the flip-flop is then set to logical 1 on the positive-going edge of waveform (b). The true output (Q) of the flip-flop is shown in Figure 3.4.22 (h). When Q goes high, step-motor pulses are no longer inhibited as shown in waveform (r) of the timing diagram. The reason for the delay is discussed below.

In the timing diagram of Figure 3.4.22 is shown that a new scan starts at T_{16} and the accompanying PUNCH-SHIFT cycle terminates at T_{17}. It is convenient for the present purposes to assume that the 8 digits corresponding to the X - Y set for this scan are punched in the last eight columns of a data card, i.e., columns 71 through 80 .

Recall that upon punching column 80 the keypunch enters into an automatic feed cycle which in turn restricts the punch mechanism for 0.25 seconds.

If the graph reading process is not inhibited during this time it is possible that a loss of information may occur. An example of this would be the case where a ΔX increment of 1 mm is pre-selected. In this instance, once column 80 is punched the first punch pulse corresponding to the next scan would occur during the feed cycle and hence the most significant value of X would be lost. Furthermore a feed cycle introduces noise into the photomultiplier output via the mains. This is due to the unregulated plate voltage supply of the photomultiplier. For these reasons graph advancement, scanning and punching are inhibited during a feed cycle.

A card-feed cycle is detected by monitoring a voltage within the keypunch. It was shown, in Section 3.4.4 (b) and Figures 3.4.19 (a) and 3.4.19 (b) that because of the manner in which this detection is made, a maximum delay of about 128 milliseconds may occur between the time at which a feed-cycle actually begins in the keypunch and the time at which waveform (g) in the timing diagram of Figure 3.4.22 goes to 0. It is conceivable then that the graph-advance circuit may not be inhibited on the ONE-SHOT A 1 output pulse immediately following a PUNCH-SHIFT cycle. This would allow a stepping motor pulse to occur at T_{18} in the timing diagram, because the inhibiting waveform (g) may go low only after the occurrence of the ONE-SHOT A 1 output pulse. This is the reason for the fixed delay of 76 milliseconds at the end of every PUNCH-SHIFT cycle.

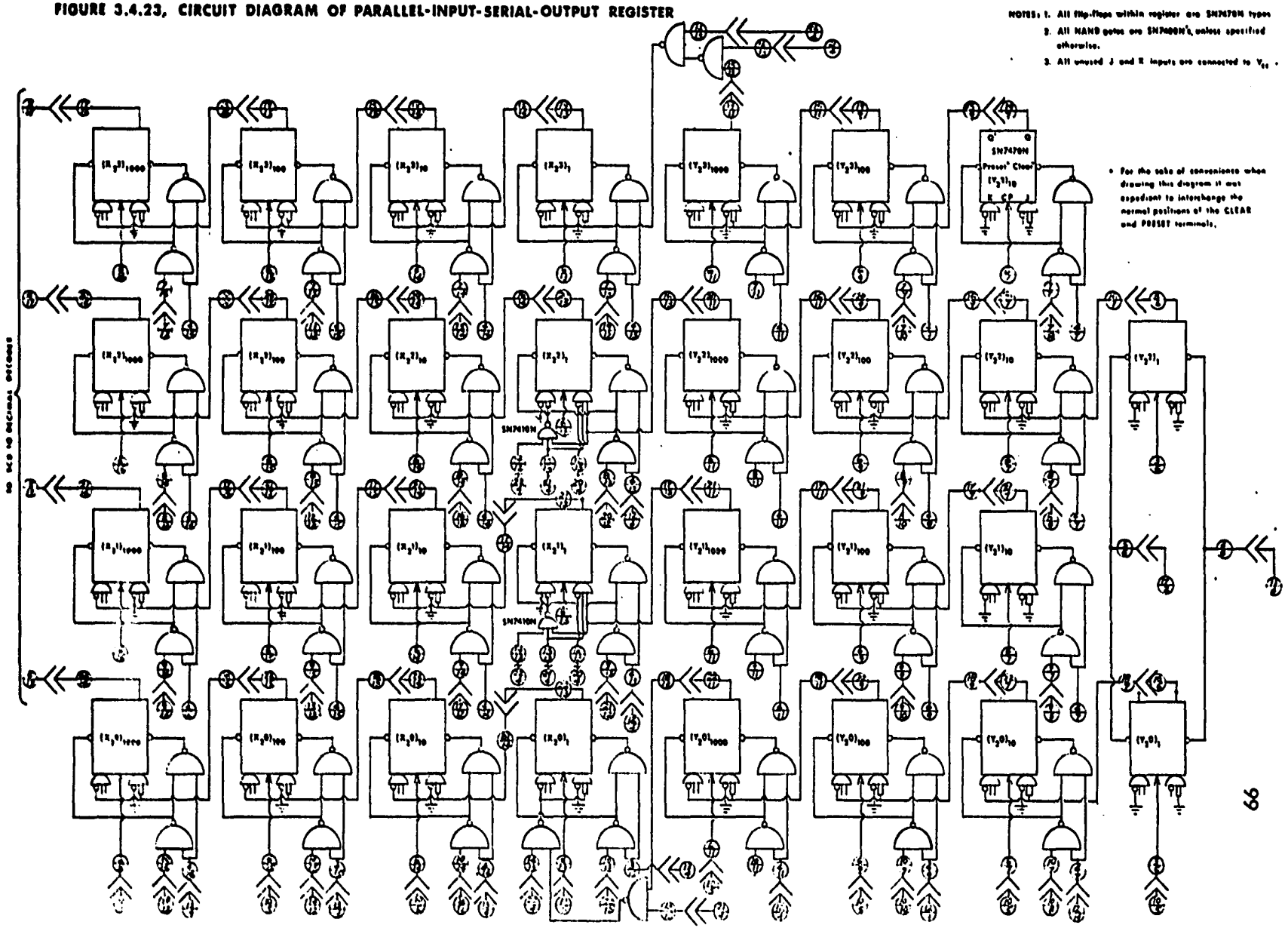
3.4.5 Register and Counters

The PARALLEL-IN-SERIAL-OUT register, in which are temporarily stored the X and Y values of a scan is shown in Figure 3.4.23. The register is comprised of 30 bits and is arranged to contain X and Y in Binary-Coded-Decimal (BCD) form. In the figure, the bits are labelled $(X_2 n)_p$ and $(Y_2 n)_p$. Flip-flop $(X_2 0)_{1000}$, for example, represents the least significant bit of the 4 bits containing the most significant decimal value of X.

The parallel transfer of data from the X and Y counters is achieved through the gating arrangement shown in Figure 3.4.24 (a). The gating is necessary because of the single-rail output nature of the X counter. The counter is comprised of four SN 7490 N binary-coded-decimal units. Only the true flip-flop outputs are available at the terminals of each unit. On the other hand, each decimal unit of the Y counter consists of four S N 7470 N flip-flops and as such both true (Q) and false (Q') outputs (double-rail) are available. However, to maintain a uniform circuit configuration with regard to the parallel shifting of data the entire register is geared to accept data emanating from a single-rail source.

In Figure 3.4.24 (a) one input to NAND GATE 1 is the true output of the $(X_2 0)_{1000}$ bit in the X counter. The other input is the PARALLEL SHIFT pulse. The outputs of GATES 1 and 2 serve as the PRESET (P) and CLEAR (C) inputs respectively of the $(X_2 0)_{1000}$ bit in the register. The waveforms in Figures 3.4.24 (b) and 3.4.24 (c) illustrate how a logical 0 or 1 is transferred from a bit in the counter to its corresponding bit in the register. Figure 3.4.24 (d) depicts the

FIGURE 3.4.23, CIRCUIT DIAGRAM OF PARALLEL-INPUT-SERIAL-OUTPUT REGISTER



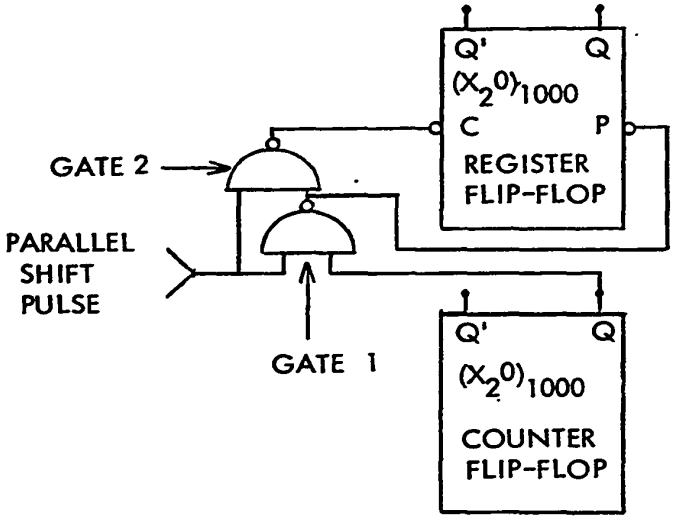


FIGURE 3.4.24 (a) .

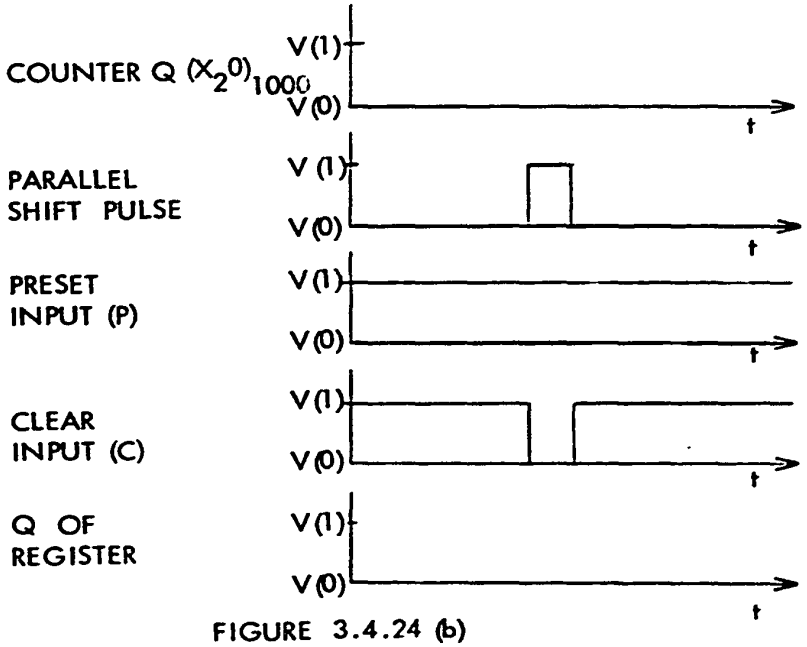


FIGURE 3.4.24 (b)

FIGURE 3.4.24. PARALLEL SHIFTING OF DATA FROM COUNTER TO REGISTER.

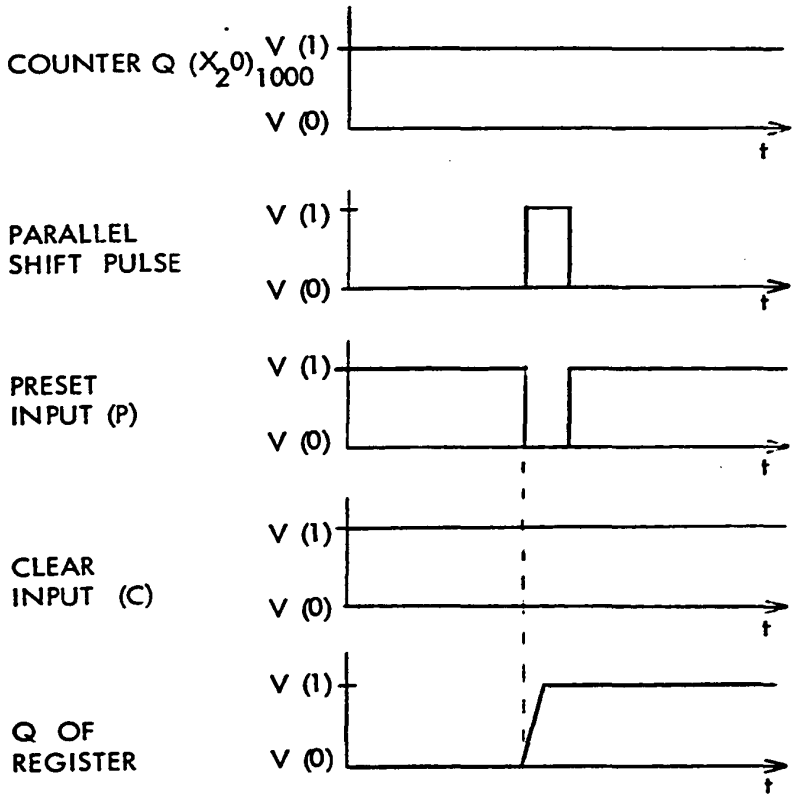


FIGURE 3.4.24 (c) .

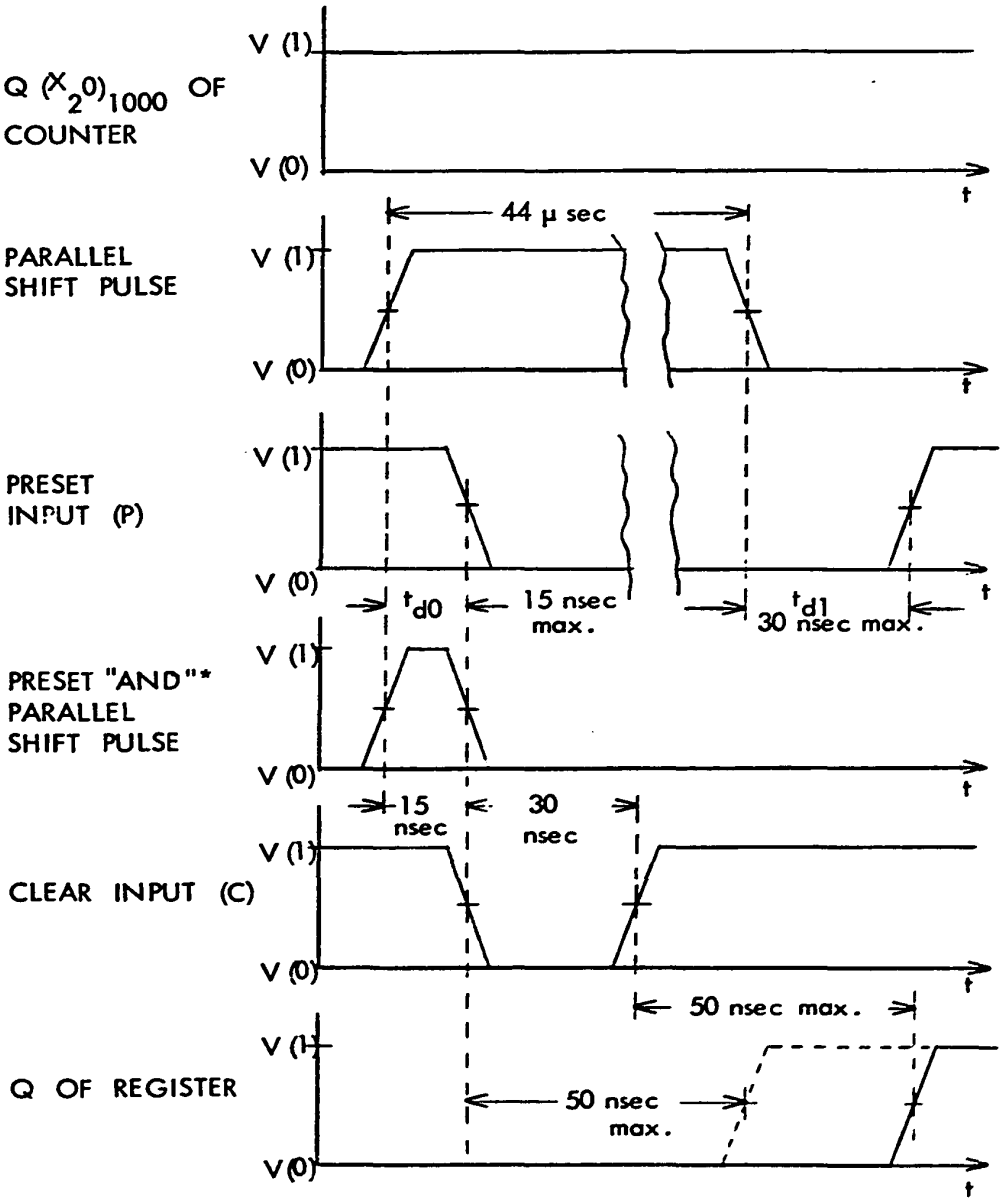


FIGURE 3.4.24 (d).

* "AND" implies the logical AND operation.

waveforms of Figure 3.4.24 (c) with the time scale expanded. The reason for this is to show that propagation delays in the gates yield a false pulse at the output of GATE 2 and thus results in the undesirable situation where inputs are applied simultaneously to both the PRESET (P) and CLEAR (C) terminals of the flip-flop. The output state (Q) during this time is indeterminate. The problem is resolved by ensuring that the PARALLEL-SHIFT pulse be of sufficient duration in that it extends beyond the false output " C " . Once the false output has occurred only the PRESET (P) input to the flip-flop is pulsed during the remaining part of the PARALLEL-SHIFT-PULSE.

With the exception of flip-flops $(Y_2 0)_1$, $(Y_2 2)_1$, $(Y_2 1)_{10}$, $(Y_2 3)_{10}$ and $(X_2 n)_1$, n = 0, 1, 2, 3, the serial shifting of data is realized by interconnecting the remaining flip-flops within the register as shown in Figure 3.4.25. The true output of flip-flop $(X_2 0)_{100}$ is connected to both the J and inverting K' inputs of flip-flop $(X_2 0)_{1000}$. The SERIAL-SHIFT pulse serves as the CLOCK input. If Q of flip-flop $(X_2 0)_{100}$ is high, then J is high and K is low in flip-flop $(X_2 0)_{1000}$. Therefore, once a SERIAL-SHIFT pulse occurs the true output of flip-flop $(X_2 0)_{1000}$ is high, regardless of its previous state. When Q of flip-flop $(X_2 0)_{100}$ is low then K is high and J low and hence Q of flip-flop $(X_2 0)_{1000}$ is low once the clock pulse occurs.

The flip-flops wherein are stored the hundredths and thousandths digits of the Y value are arranged as shown in Figure 3.4.26. As previously mentioned, the thousandths digit is set to 5 whenever the number of marker pulses occurring coinciden-

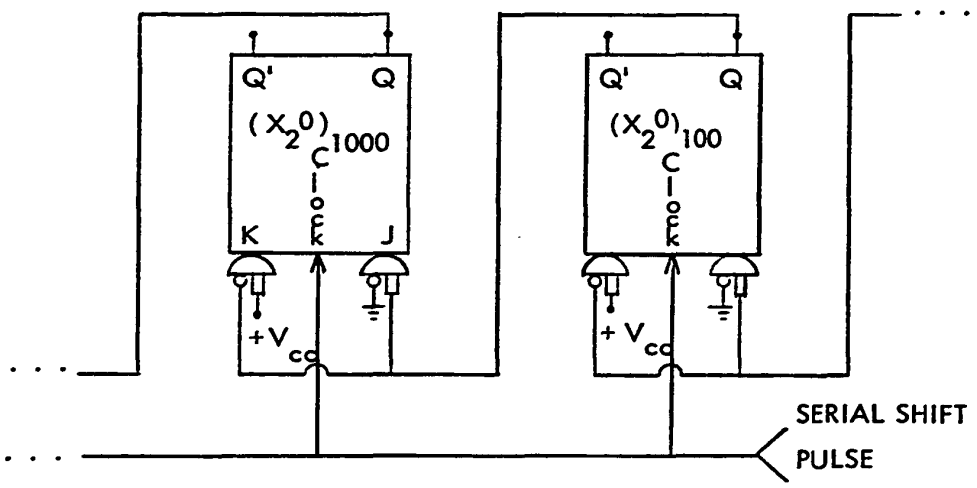


FIGURE 3.4.25. FLIP - FLOP CONNECTIONS FOR SERIAL - SHIFTING OF DATA.

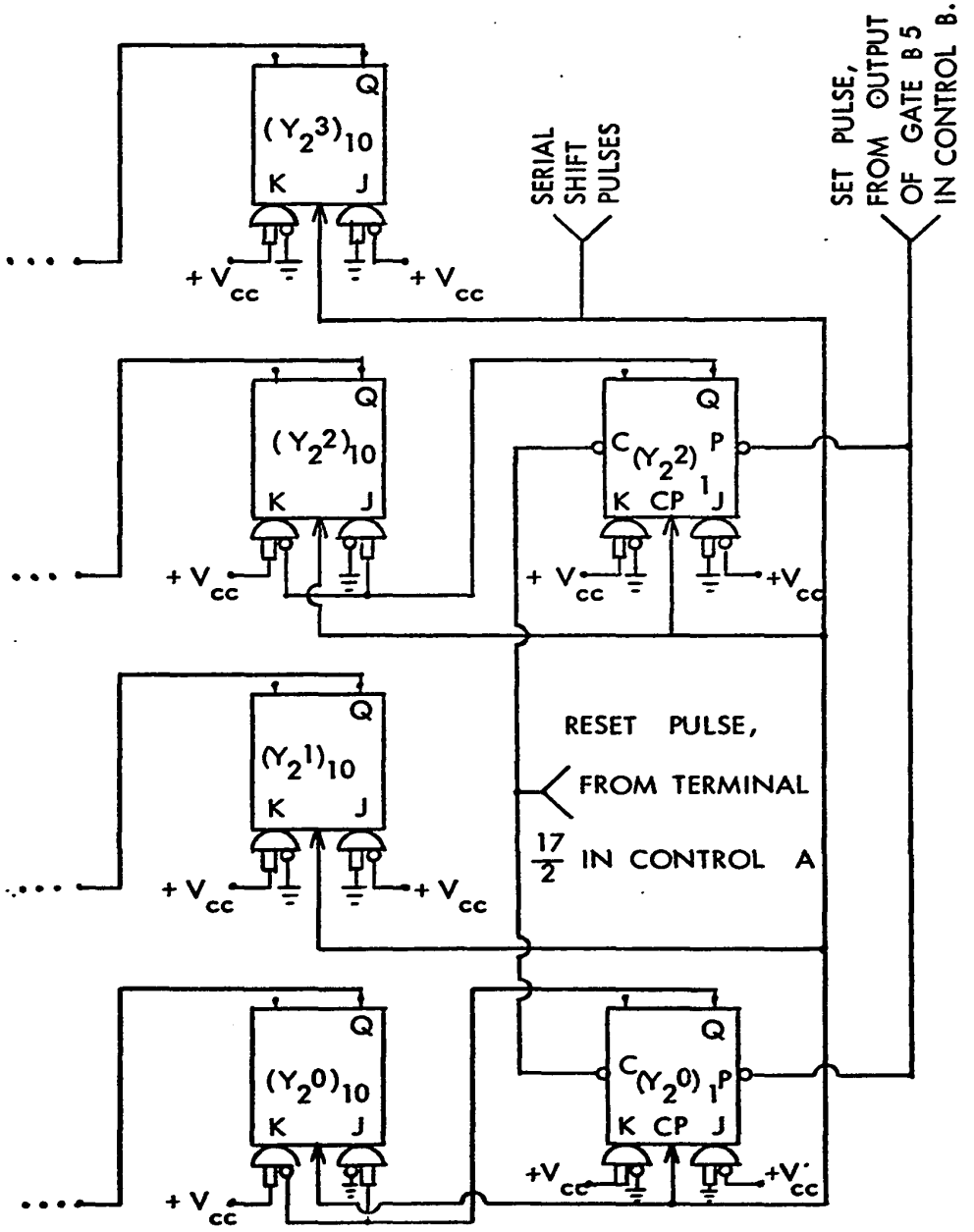


FIGURE 3.4.26. FLIP-FLOPS CONTAINING THE HUNDREDTHS AND THOUSANDTHS DIGITS OF THE ORDINATE (Y) VALUE WITHIN THE PARALLEL-IN - SERIAL -OUT REGISTER.

tally with two video pulses is odd. This is done by setting the true outputs of flip-flops $(Y_2\,0)_1$ and $(Y_2^2)_1$ in Figure 3.4.26 to a logical 1. The flip-flops are set to 1 by applying a logical 0 to the preset inputs. The preset inputs consist of the output of NAND GATE B 5 in Control B (SECTION 5 B), Figure 3.4.5 (b)). Recall that by means of this gate is derived a negative-going pulse (Waveform (y), Figure 3.4.6) whenever an odd number of marker pulses occurs in coincidence with two video pulses. To ensure that the two flip-flops are initially in a reset, or cleared state, a momentary logical 0 is applied to their clear inputs when power is first turned on. The resetting signal is obtained from terminal $\frac{17}{2}$ in Control A (SECTION 3A, Figure 3.4.1 (b)).

The J and K input connections of flip-flops $(Y_2\,1)_{10}$, $(Y_2\,3)_{10}$, $(Y_2\,0)_1$ and $(Y_2\,2)_1$ are also shown in Figure 3.4.26. The non-inverting J inputs are connected to ground so that J is a logical 0. The non-inverting K inputs are kept at a logical 1 whereas the inverting (K') inputs are grounded. Therefore J = 0 and K = 1 in each of these four flip-flops and when the first serial-shift pulse occurs the flip-flops are set to a logical 0. Each successive serial-shift pulse thereafter shifts the zeros contained within these flip-flops to the left. This, as mentioned in Section 3.4.4 automatically clears the register while data is being transferred onto cards.

For the bits in which the least significant decimal value of X is initially stored, i.e. $(X_2\,n)_1$, n = 0, 1, 2, 3, the serial-shift arrangement is more complex, as shown in Figure 3.4.27 (a). The additional gating is used in con-

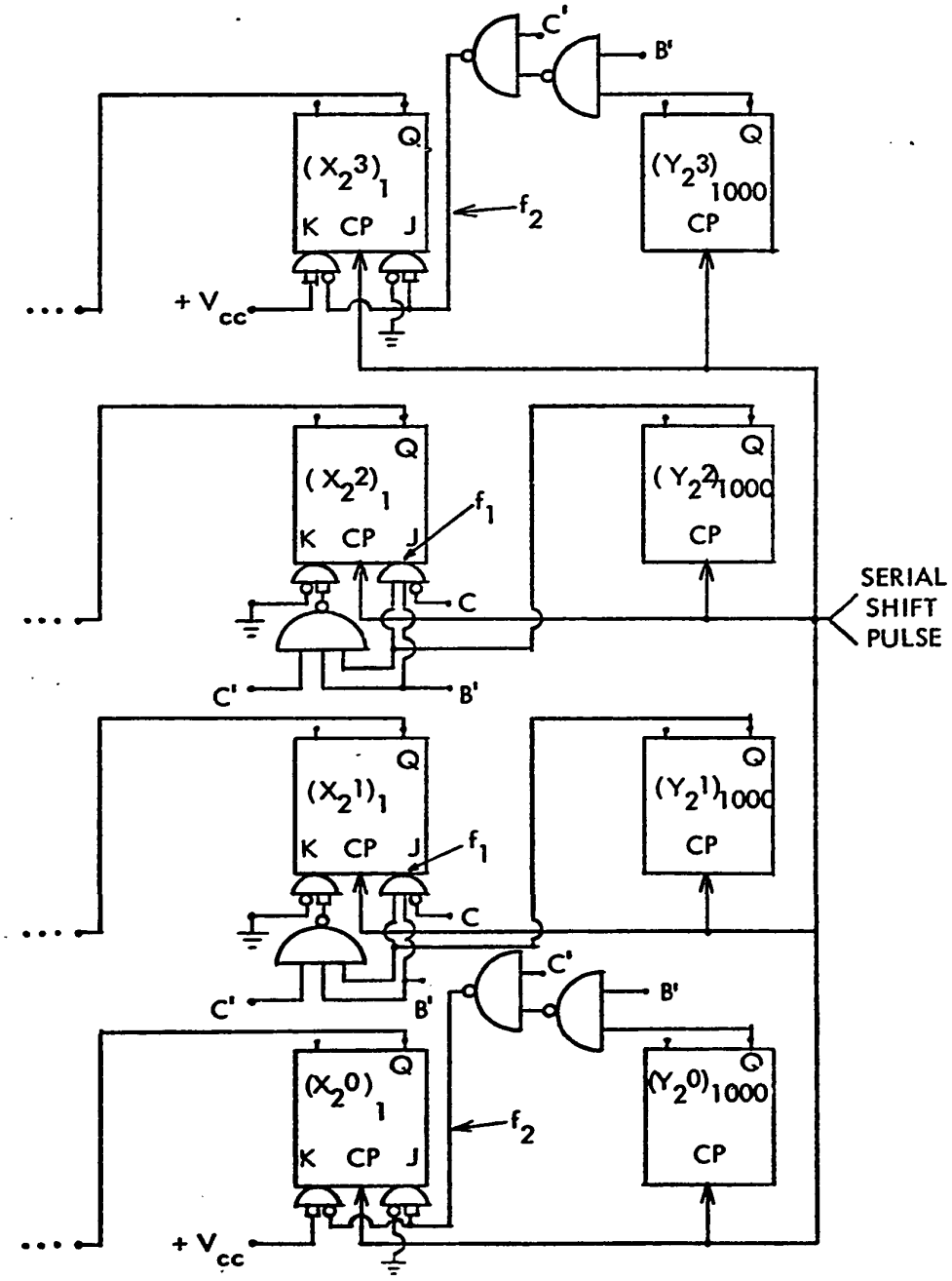


FIGURE 3.4.27 (a). ADDITIONAL GATING REQUIRED TO INCORPORATE ERROR DETECTION SCHEME WITHIN PARALLEL-IN-SERIAL-OUT REGISTER.

junction with the error-detection scheme discussed in Section 3.4.3 . Recall that if the number of VIDEO pulses occurring in one scan was less than two, it was decided that a Y value of 0.000 along with the current X be punched out on a card. Alternately, when more than three VIDEO pulses occurred in a scan a value of 9.999 was then assigned to Y .

The technique used to incorporate the error-detection scheme into the register is similar to the one discussed earlier, where the register is cleared by simply shifting a set of zeroes through it. The only difference is that a zero or a nine is now entered into the bits which initially store the least significant value of X. Figure 3.4.27 (b) illustrates this technique for the case when more than three video pulses occur in one scan. The contents of the X and Y counters and hence of the register at the occurrence of a parallel shift pulse are arbitrarily assumed to be 9138 and 2.185 respectively. The first three serial-shift pulses transfer the current X value onto the data card. The remaining shift pulses enable Y to take on the value 9.999, regardless of what Y was initially. Therefore, during this PUNCH-SHIFT cycle, the numbers 9138 9999 are punched.

When more than three video pulses occur in one scan the true output of the PUNCH 9's flip-flop within CONTROL B is high. Alternately the true output of the PUNCH 0's flip-flop is high if less than two video pulses occur. To set the least significant X bits to 9, J must be high and K low for flip-flops $(X_2\,0)_1$ and $(X_2\,3)_1$, while J should be low and K high for flip-flops $(X_2\,2)_1$ and $(X_2\,1)_1$. To set these four flip-flops to 0, each K input should be high and each J input low. Understandably,

	1	0	0	1	0	0	1	0	
	0	0	0	0	0	0	0	1	REGISTER CONTENTS
	0	0	1	0	1	0	0	0	AFTER PARALLEL-SHIFT
	1	1	1	0	0	1	0	1	PULSE.
DECIMAL EQUIVALENT	9	1	3	8	2	1	8	5	
	0	0	1	1	0	1	0	0	REGISTER CONTENTS
	0	0	0	0	0	0	1	0	AFTER FIRST SERIAL-
	0	1	0	0	0	0	0	0	SHIFT PULSE.
	1	1	0	1	1	0	1	0	
DECIMAL EQUIVALENT	1	3	8	9	1	8	5	0	
	0	1	1	1	1	0	0	0	REGISTER CONTENTS
	0	0	0	0	0	1	0	0	AFTER SECOND SERIAL-
	1	0	0	0	0	0	0	0	SHIFT PULSE.
	1	0	1	1	0	1	0	0	
DECIMAL EQUIVALENT	3	8	9	9	8	5	0	0	
	1	1	1	1	0	0	0	0	REGISTER CONTENTS
	0	0	0	0	1	0	0	0	AFTER THIRD SERIAL-
	0	0	0	0	0	0	0	0	SHIFT PULSE.
	0	1	1	1	1	0	0	0	
DECIMAL EQUIVALENT	8	9	9	9	5	0	0	0	
	1	1	1	1	0	0	0	0	REGISTER CONTENTS
	0	0	0	0	0	0	0	0	AFTER FOURTH AND
	0	0	0	0	0	0	0	0	THROUGH TO THE
	1	1	1	1	0	0	0	0	EIGHTH SERIAL-SHIFT PULSE.
DECIMAL EQUIVALENT	9	9	9	9	0	0	0	0	

FIGURE 3.4.27 (b). SERIAL SHIFTING OF DATA THROUGH REGISTER WHEN MORE THAN THREE VIDEO PULSES OCCUR IN ONE SCAN.

if an allowable number of video pulses occurs then each bit $(X_2\ n)_1$ depends on the contents of the bit preceding it in the chain, i.e. bit $(Y_2\ n)_{1000}$, $n = 0, 1, 2, 3$.

In the truth table of Figure 3.4.27 (c), the variables $Q\ (Y_2\ n)_{1000}$, B, C, f_1 and f_2 are defined as follows :

$Q\ (Y_2\ n)_{1000}$	represents the true output of flip-flop $(Y_2\ n)_{1000}$, $n = 0, 1, 2, 3$.
B	represents the true output of the PUNCH 0's flip-flop.
C	represents the true output of the PUNCH 9's flip-flop.
f_1	represents the J input to flip-flops $(X_2\ 1)_1$ and $(X_2\ 2)_1$.
f_2	represents the J input to flip-flops $(X_2\ 0)_1$ and $(X_2\ 3)_1$.

From the Table, $f_1 = Q\ (Y_2\ n)_{1000}\ B'\ C'$, $n = 1, 2$,

and $f_2 = C + Q\ (Y_2\ n)_{1000}\ B'$, $n = 0, 3$.

Therefore the J and K inputs for flip-flops $(X_2\ n)_1$ are summarized as follows :

	J INPUT	K INPUT
Flip-flop $(X_2\ 0)_1$	$C + Q\,(Y_2\ 0)_{1000}\,B'$	$[\,C + Q\,(Y_2\ 0)_{1000}\,B'\,]'$
Flip-flop $(X_2\ 1)_1$	$Q\,(Y_2\ 1)_{1000}\,B'\,C'$	$[\,Q\,(Y_2\ 1)_{1000}\,B'\,C'\,]'$
Flip-flop $(X_2\ 2)_1$	$Q\,(Y_2\ 2)_{1000}\,B'\,C'$	$[\,Q\,(Y_2\ 2)_{1000}\,B'\,C'\,]'$
Flip-flop $(X_2\ 3)_1$	$C + Q\,(Y_2\ 3)_{1000}\,B'$	$[\,C + Q\,(Y_2\ 3)_{1000}\,B'\,]'$

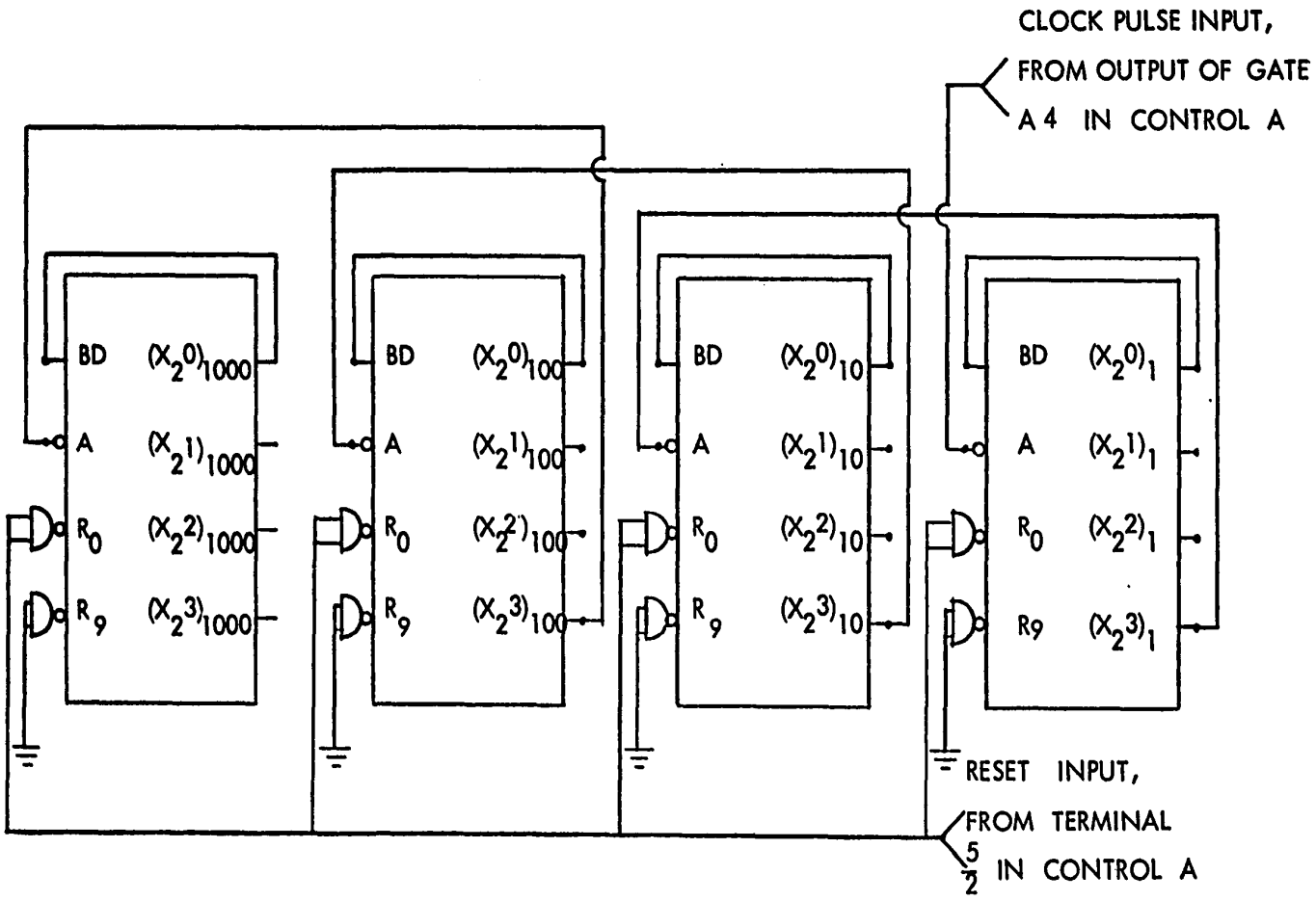
The gating necessary to implement these functions is shown in Figure 3.4.27 (a).

The circuit diagram of the X counter is shown in Figure 3.4.28. The counter consists of four SN 7490N binary-coded-decimal (BCD) counting units and hence the maximum possible X is 9.999 meters. The Clock Input (CP) to the first stage is the output of GATE A4 in CONTROL A. Recall that from the output of this gate are derived the stepping motor pulses. Therefore, the X counter is incremented by 1 every time the graph paper is advanced by one millimeter. Each of the four units is triggered on the negative-going edge of the clock input. To trigger the next unit in the chain the true output of the 2^3 bit in the unit preceding it is used. The RESET input is obtained from terminal $\frac{5}{2}$ in CONTROL A. This terminal is high whenever the graph reading process is in the STOP mode and low otherwise.

The Y counter is comprised of three BCD counting units. Each unit is made up of four SN7470N flip-flops interconnected as shown in Figure 3.4.29. The connections are made according to the flip-flop input equations derived by applying

$Q_{(Y_2^n)}$ 1000	B	C	f_1	f_2
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	1

FIGURE 3.4.27 (c). TRUTH TABLE DEFINING THE LOGIC REQUIRED TO INCORPORATE THE ERROR DETECTION SCHEME INTO THE PARALLEL-IN-SERIAL-OUT REGISTER.



NOTE : RESET INPUTS REQUIRE LOGICAL 1 VOLTAGE TO CLEAR COUNTER.

FIGURE 3.4.28. X COUNTER.

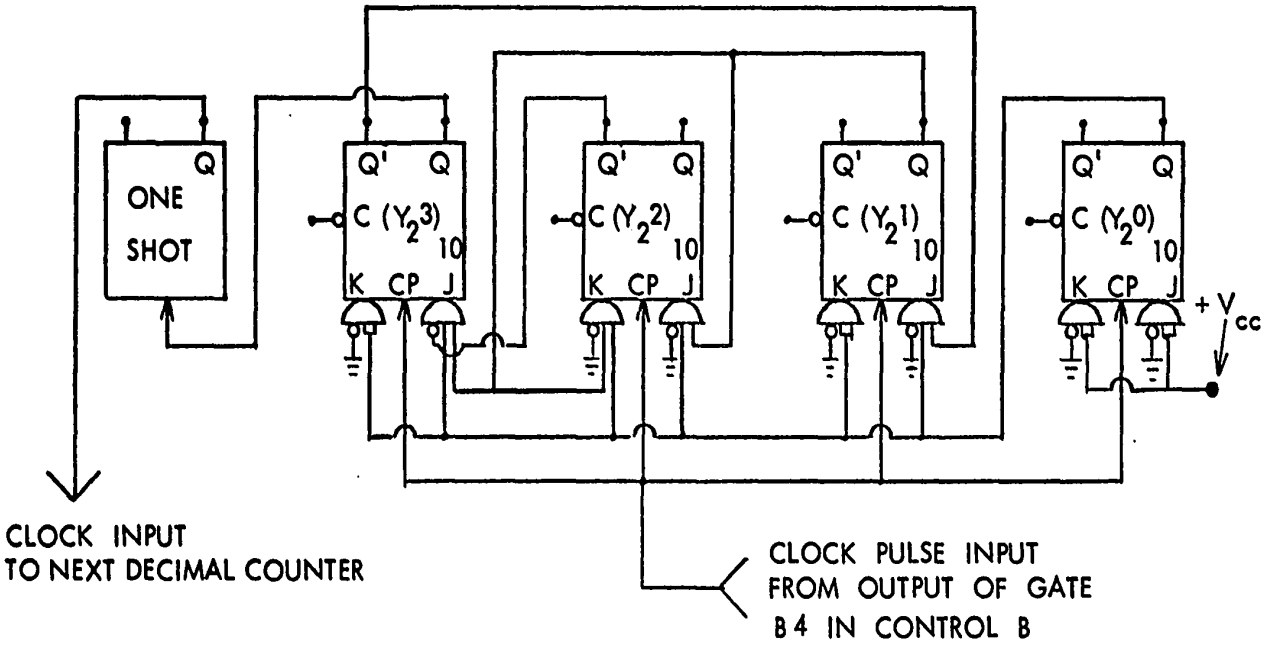


FIGURE 3.4.29. Y COUNTER.

the extension of Mealy's theory [14] in the design of synchronous counters. The input equations are :

$$J(Y_2\,0)_{10} = K(Y_2\,0)_{10} = 1 .$$

$$J(Y_2\,1)_{10} = Q(Y_2\,0)_{10} \cdot Q'(Y_2\,3)_{10} \; ; \; K(Y_2\,1)_{10} = Q(Y_2\,0)_{10} .$$

$$J(Y_2\,2)_{10} = K(Y_2\,2)_{10} = Q(Y_2\,1)_{10} \cdot Q(Y_2\,0)_{10} .$$

$$J(Y_2\,3)_{10} = Q(Y_2\,2)_{10} \cdot Q(Y_2\,1)_{10} \cdot Q(Y_2\,0)_{10}$$

$$K(Y_2\,3)_{10} = Q(Y_2\,0)_{10} .$$

The clock pulse to the first decimal counting unit, $(Y_2\,n)_{10}$ is the output of GATE B4 in CONTROL B. The clock pulse to each succeeding unit is obtained from a negative-edge-triggered one-shot. The input to the one-shot is the true output of the 2^3 bit of the preceding BCD unit, as shown in Figure 3.4.29. The one-shot is necessary because of a restriction regarding the application of the CLEAR signal to the SN 7470N flip-flop. The clock input to the flip-flop must be low when a clear signal is applied. If the 2^3 bit of each decimal unit is applied directly to the clock input of the next stage it is conceivable that the restriction may be violated and hence all flip-flops within the counter may not be reset to a logical 0 upon the application of the clear signal. The counter is cleared before any graph reading takes place by a signal derived from the STOP key. When a graph is being read the counter is reset at the end of every PUNCH-SHIFT cycle.

3.4.6 Special Circuits

3.4.6 (a) Card-Feed Cycle Detection Circuit

It is mentioned in Section 3.4.4 (b) that in two instances the punch mechanism within the IBM keypunch is restricted. This occurs when the supply of data cards is exhausted or during a card-feed cycle.

To inhibit the graph reading process during this time a voltage across a set of contacts in the keypunch is monitored and, through a voltage translating circuit is fed to the graph-reader logic unit. The circuit is shown in Figure 3.4.30 (a).

When a card is in the PUNCH STATION within the keypunch, voltage V_{AB} is 0 volts. Transistor Q_1 is then forward-biased into saturation. Transistor Q_2 is cut off since the input to its base is derived from the collector of Q_1. The reed relay in the collector of Q_2 is therefore not energized and its contact is in the normally-closed (N.C.) position. The operating arm of the contact is connected to ground and hence the output of NAND GATE 1 in the circuit is high.

During a card-feed cycle, or with no card in the PUNCH STATION path A B is open-circuited and V_{AB} is then -48 volts. Voltage V_{AB} is fed through a resistance divider into the base of Q_1, causing the transistor to be cut off. Q_2 then conducts and energizes the REED relay. The contact arm moves to the normally-open (N. O.) position and the output of NAND GATE 1 is then low. The output of GATE 1 is fed to the logic unit of the graph reader.

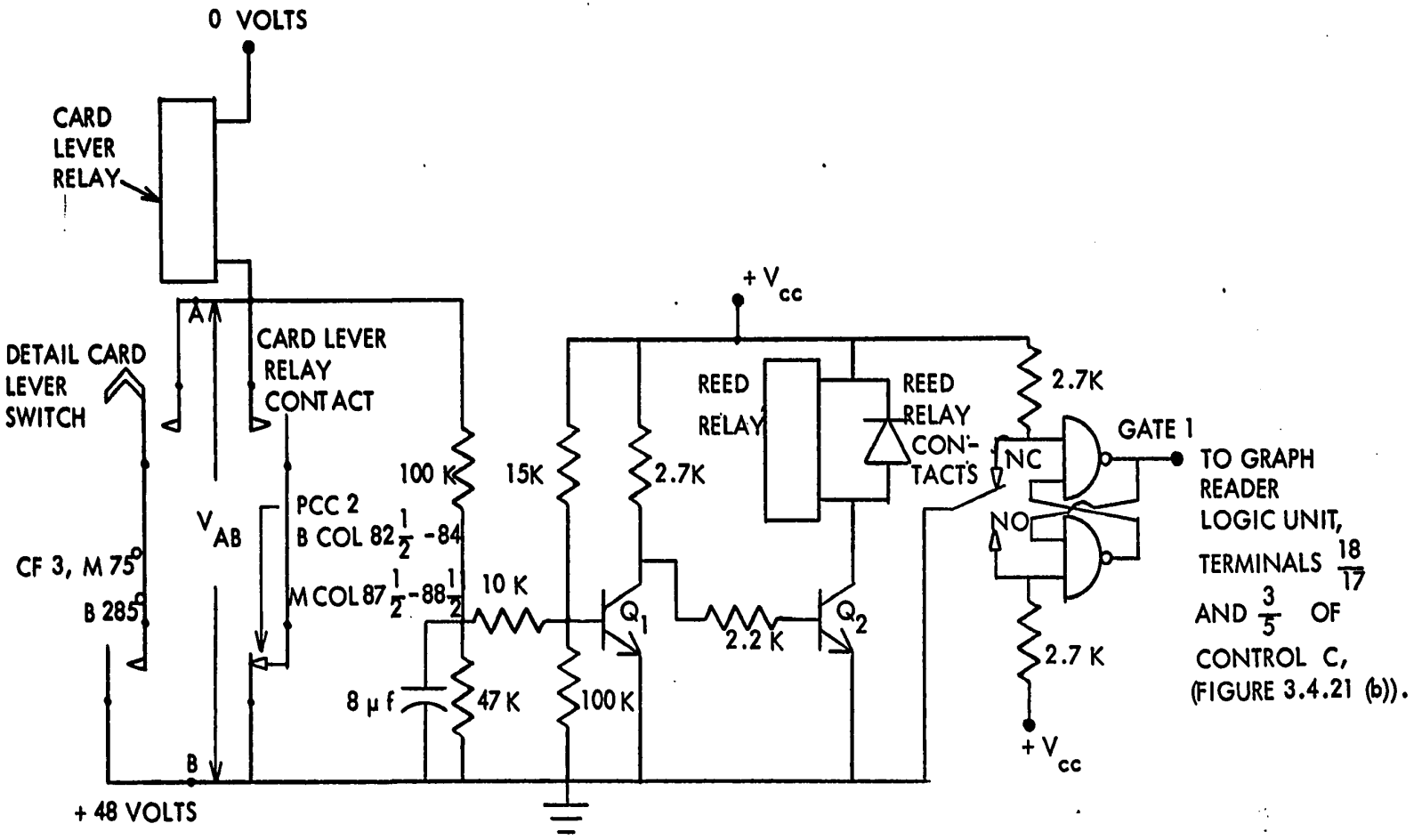


FIGURE 3.4. 30 (a). CARD-FEED CYCLE DETECTION CIRCUIT.

The 8 μf capacitor and the reed relay serve to prevent the noise inherent in signal V_{AB} from reaching the logic circuits. The noise is due primarily to contact bounce and the inductance of the CARD LEVER relay. Delays d_1 and d_2 shown in Figure 3.4.30 (b) are caused both by the unequal charge-discharge times of the 8 μf capacitor and the unequal open-close times of the reed relay contacts.

3.4.6 (b) Test Circuit

When a graph is read three pulse trains are generated photo-electrically in the scanning system and fed into the logic circuits. The function of the test circuit is to generate electronically, for diagnostic purposes a similar set of pulses. In this way the logic circuits may be tested independently, without resorting to the scanning unit.

The three pulses - the MARKER, END OF SCAN and VIDEO test pulses are derived from two oscillators in the test circuit. The oscillators are astable multivibrators and are made up of SN 7400N NAND gates, as was shown in Section 3.3.2 (a).

The MARKER pulses are derived from ASTABLE 1, shown in Figure 3.4.31, which oscillates at 10 K hz. The output of the astable is fed into a transistor stage (INVERTER / LEVEL SHIFTER) which shifts the oscillator voltage levels to 0 and -15 volts respectively. This is done in order that the voltage levels of the test signals conform with those appearing at the output of the scanning system. Waveforms

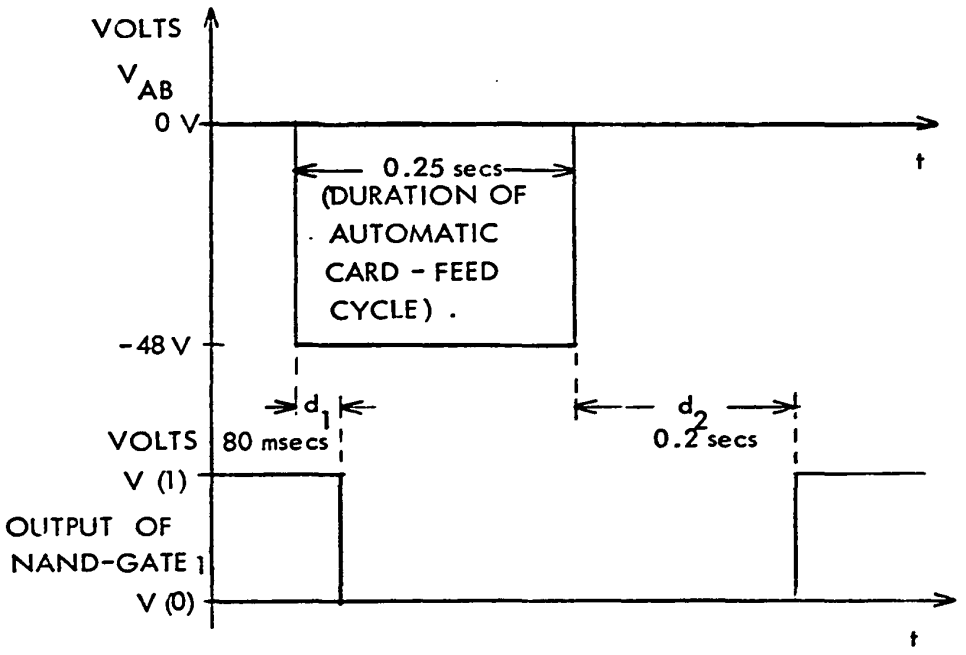


FIGURE 3.4.30 (b). INPUT AND OUTPUT VOLTAGES OF CARD-FEED CYCLE DETECTION CIRCUIT.

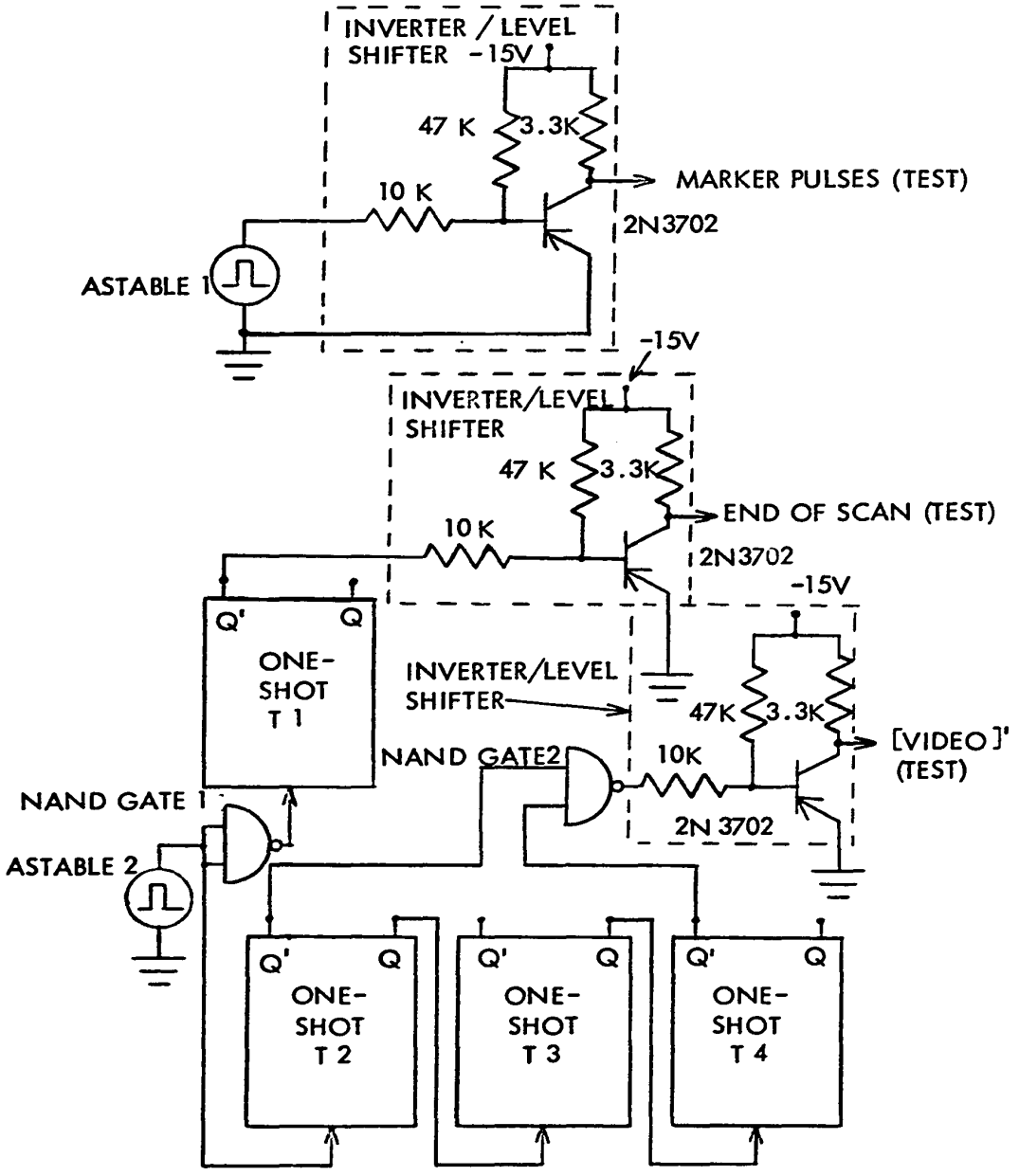


FIGURE 3.4.31. TEST CIRCUIT.

(a) and (b) in Figure 3.4.32 depict the oscillator and INVERTER / LEVEL SHIFTER outputs respectively. Waveform (b) is the MARKER test pulse.

The END OF SCAN test pulse is derived from ASTABLE 2. The oscillator output, waveform (c), is inverted by NAND GATE 1 and fed into the NEGATIVE-EDGE-TRIGGERED ONE-SHOT T_1. This one-shot, along with those mentioned below, are made up of SN 7400 N NAND gates, as shown in Section 3.3.2 (a). The false output Q' of the ONE-SHOT, Waveform (e), is inputted to another INVERTER / LEVEL SHIFTER transistor stage. The output voltage at the collector of the transistor - Waveform (f) is the END OF SCAN test pulse.

To generate VIDEO test pulses, the output of OSCILLATOR 2 is used to trigger NEGATIVE - EDGE - TRIGGERED ONE-SHOT T_2. Waveforms (g) and (h) depict the true and false outputs of the one - shot respectively. The true output is fed to NEGATIVE - EDGE - TRIGGERED ONE-SHOT T_3. The true output of one-shot T_3, Waveform (i), is fed to yet another one-shot - T_4. The false outputs of one-shots T_2 and T_4 (Waveforms (h) and (j)) are combined in NAND GATE 2. The output of the gate, Waveform (k), is fed to an INVERTER / LEVEL SHIFTER transistor stage. Waveform (l) depicts the output of the transistor stage and is the VIDEO test pulse. Note that the signal is inverted, as is the case with the VIDEO signal appearing at the output of the scanning system.

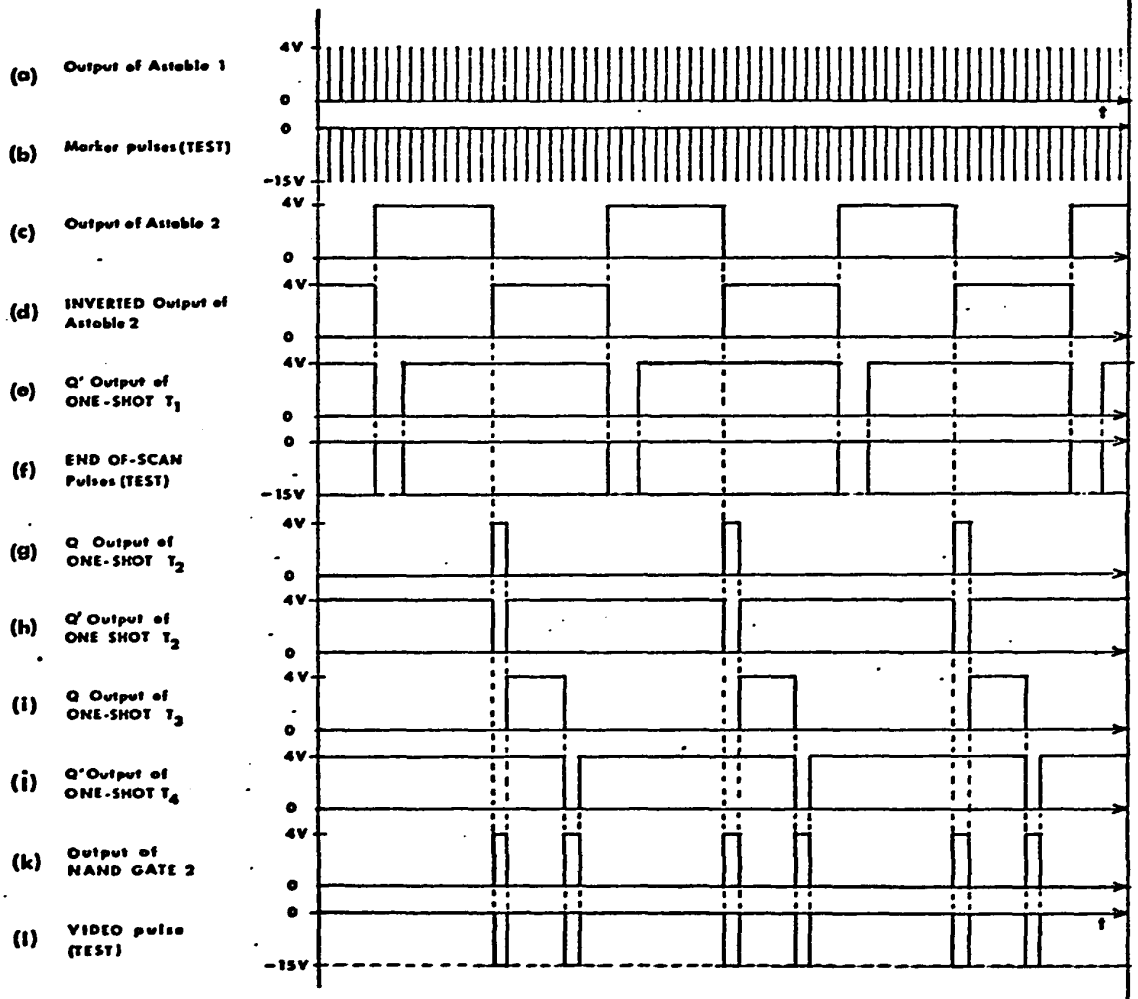


FIGURE 3.4.32, TEST CIRCUIT WAVEFORMS

3.4.6 (c) Visual Display Unit

The visual display unit consists of an array of 48 data lamps. The array is shown in Figure 3.4.33 (a). Each lamp is driven by the circuit of Figure 3.4.33 (b). The input to the base of the lamp - driving transistor is derived from the true (Q) output of a flip-flop.

The drive signals for the lamps in Section A of the array are derived from the flip-flops which constitute the Y counter and, as such, Section A represents in binary - coded - decimal form the contents of the Y counter. As an example, the lamps which are lit (denoted by X) in Section A represent a Y value of 3.625 inches.

In a similar manner Sections B and C in Figure 3.4.33 (a) represent the contents of the parallel - in - serial - out register. Section B is shown to contain an X value of 737 millimeters and Section C the Y value of 3.625 inches. Sections B and C are shown prior to the occurrence of the serial-shift pulses. Once these pulses occur the data within the register is shifted to the left, once for every occurrence of the pulse. While this shifting is taking place, the contents of Section A remains constant at 3.625 inches.

The visual display unit serves a dual purpose. While a graph is being read, the unit gives an instantaneous and continuous display not only of the X and Y values of a particular scan but also of the operation of the logic circuits. Secondly, the unit may be used with the test circuit as an aid in diagnosing faults within the logic unit.

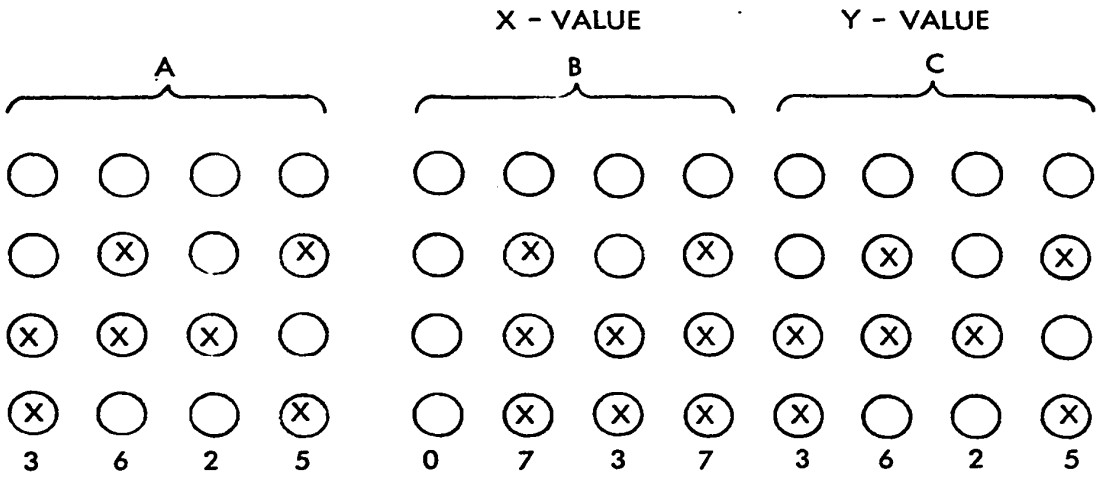


FIGURE 3.4.33(a). LAMP ARRANGEMENT OF VISUAL DISPLAY UNIT.

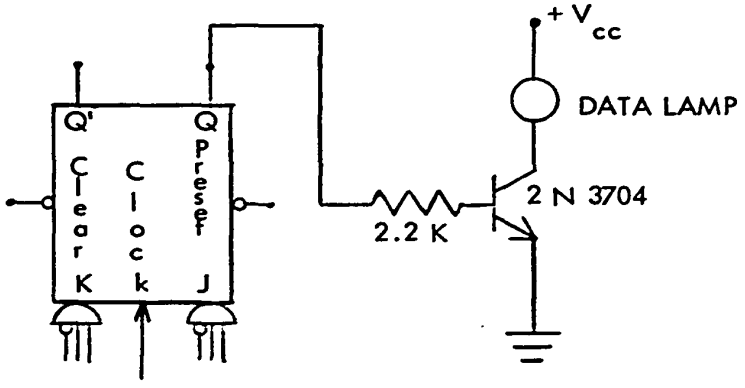


FIGURE 3.4.33 (b). VISUAL DISPLAY UNIT LAMP DRIVER CIRCUIT.

CHAPTER IV

THE OPTICS OF THE SCANNING SYSTEM

4.1 Introduction

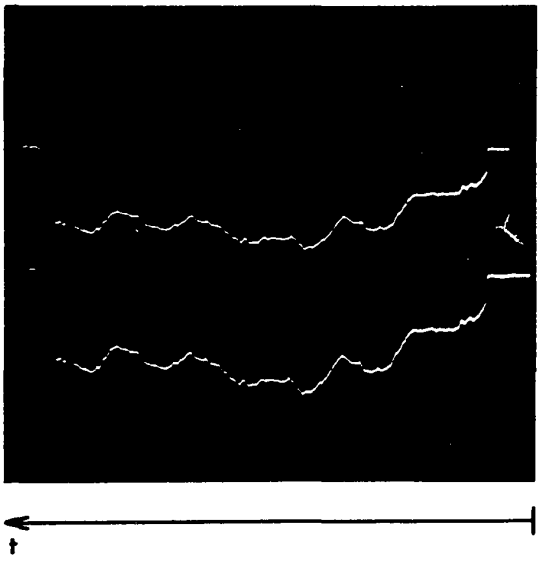
This chapter presents the work done to improve the optics of the graph reader scanning system.

The scanning principle, as described earlier in Section 2.1, consists of a moving spot of light produced electromechanically by means of two slits and a high-pressure mercury arc lamp.

As the spot traverses a graph, light reflected from the graph is sensed by a photomultiplier tube. The photomultiplier output voltage as obtained by Rosza [4] is shown in the upper trace of picture P 4.1. The photomultiplier output is amplified in a pre-amplifier and its output, in turn is shown as the lower trace of picture P 4.1. The paper being scanned was of the Sanborn type containing green grid lines.* No graph lines were on the graph in this case. When the spot is not scanning the paper the photomultiplier voltage is constant, at a "black" level. As soon as the light spot "hits" the paper a sharp transition into the "light" voltage level takes place. At the end of a scan a sharp transition back to the black voltage level occurs. The photomultiplier output is proportional to the intensity of the light spot as it moves across a paper. Because of its fixed position relative to the scanning spot the photomultiplier exhibits the " brightest " voltage level at approximately the center of a scan, where reflected light is normal to the photomultiplier lens. This is the most sensitive region of the detection process which senses a line on a graph.

---

* A green gelatin filter was on the photomultiplier lens while pictures P4.1 - P4.9 were taken.



t

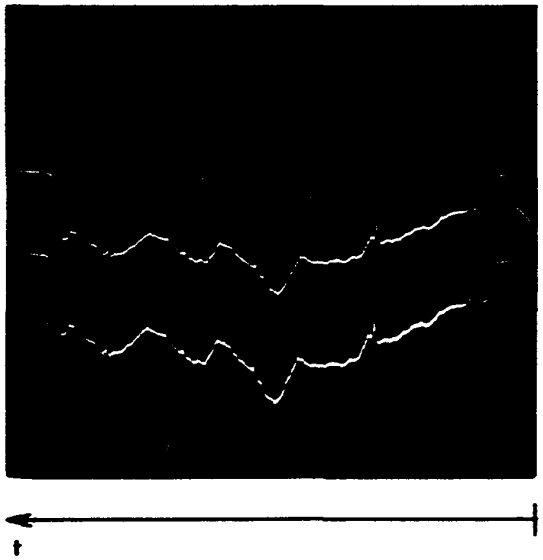
UPPER TRACE: PHOTOMULTIPLIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 100 m Volts / div.

LOWER TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT.: 1 Volt / div.

P 4.1. PHOTOMULTIPLIER AND PRE-AMPLIFIER OUTPUT SIGNALS CORRESPONDING TO A SCAN OF A GRAPH WHICH CONTAINS NO LINES.



t

UPPER TRACE : PHOTOMULTIPLIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 100 m Volts / div.

LOWER TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 1 Volt / div.

P 4.2. PHOTOMULTIPLIER AND PRE-AMPLIFIER OUTPUT SIGNALS CORRESPONDING TO A SCAN OF A GRAPH WHICH CONTAINS 2 LINES.

Two types of "background" signals are evident in picture P 4.1. The low frequency components, of a relatively high amplitude, were assumed to be caused by the unregulated DC supply used to power the mercury arc lamp [4]. This supply consists of a bridge rectifier and a simple RC filter.

Also present in the picture are high frequency background components. These Rosza [4] attributed both to changes in the reflection coefficient and presence of grid lines on the graph sample scanned.

Picture P 4.2 again illustrates the photomultiplier and preamplifier outputs respectively. The graph paper is again of the Sanborn type. In this case two pulses appear, in addition to the background components noted above. The two pulses are due to the fact that the light spot has traversed two lines on the graph paper.

Note the relative phasing of the low frequency background signals in pictures P 4.1 and P 4.2 - indicating that the line frequency components are out of phase with respect to the fundamental photomultiplier signal. To appreciate the significance of the background signals, i.e., both the low and high frequency components, a brief description of the circuitry involved in deriving video pulses from the photomultiplier output is now given.

4.2 Detection Circuitry

The block diagram of the circuitry with which are detected graph lines is shown in Figure 4.2.1. Of specific interest to the present discussion is the manner

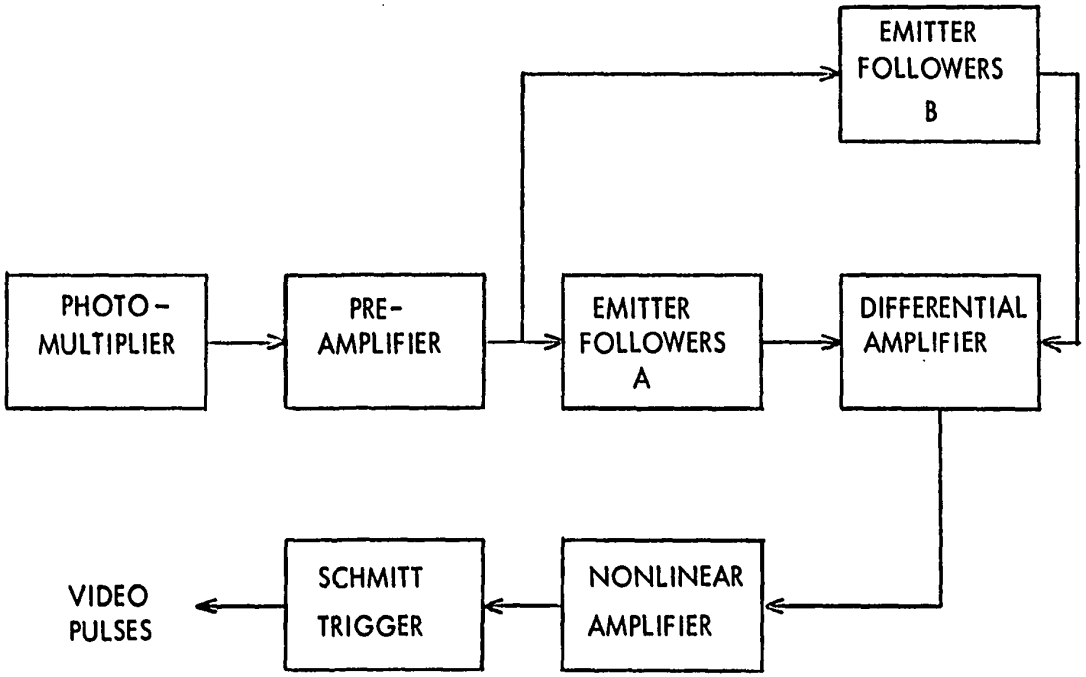


FIGURE 4.2.1. BLOCK DIAGRAM OF GRAPH - LINE DETECTION CIRCUITRY.

whereby the "useful" signals due to graph lines depicted in P 4.2 are extracted from the background noise (low and high frequency components).

To distinguish the useful signals from noise the output of the pre-amplifier is fed into two emitter-follower stages - A and B respectively. Circuits A and B are shown in Figure 4.2.2. The output of circuit A, e_{0A}, follows the pre-amplifier output with almost unity gain and serves as one input to a differential amplifier. The second input to the differential stage is e_{0B}, the output of circuit B. The function of circuit B is to produce a signal which contains only the background noise in the photomultiplier output. This is done by means of transistor Q_1 together with the 0.1 μf capacitor C in its emitter circuit. The capacitor is shunted by an 80 kΩ resistor and the input impedance of a succeeding emitter-follower stage. On the negative-going edge of the pre-amplifier output, shown in Figure 4.2.3 (a) transistor Q_1 charges capacitor C to an amount equal to the total negative excursion of waveform (a) less the base-to-emitter voltage V_{be}. The capacitor voltage then follows the relatively slow background noise due to the lamp supply and only negative-going high frequency noise components. However, any sudden positive-going changes in waveform (a) greater than V_{be} do not appear across the capacitor because the base-to-emitter diode of Q_1 then becomes reverse-biassed and hence cuts off the transistor.

The voltage appearing across capacitor C is fed into an emitter - follower stage. The output of this stage, e_{0B} (Figure 4.2.3 (b)), serves as the second input to the differential amplifier. The background signal, e_{0B}, is subtracted from e_{0A} by the differential amplifier, whose output is shown in Figure 4.2.3 (c). The lower trace of picture P 4.3 also depicts the output of the differential

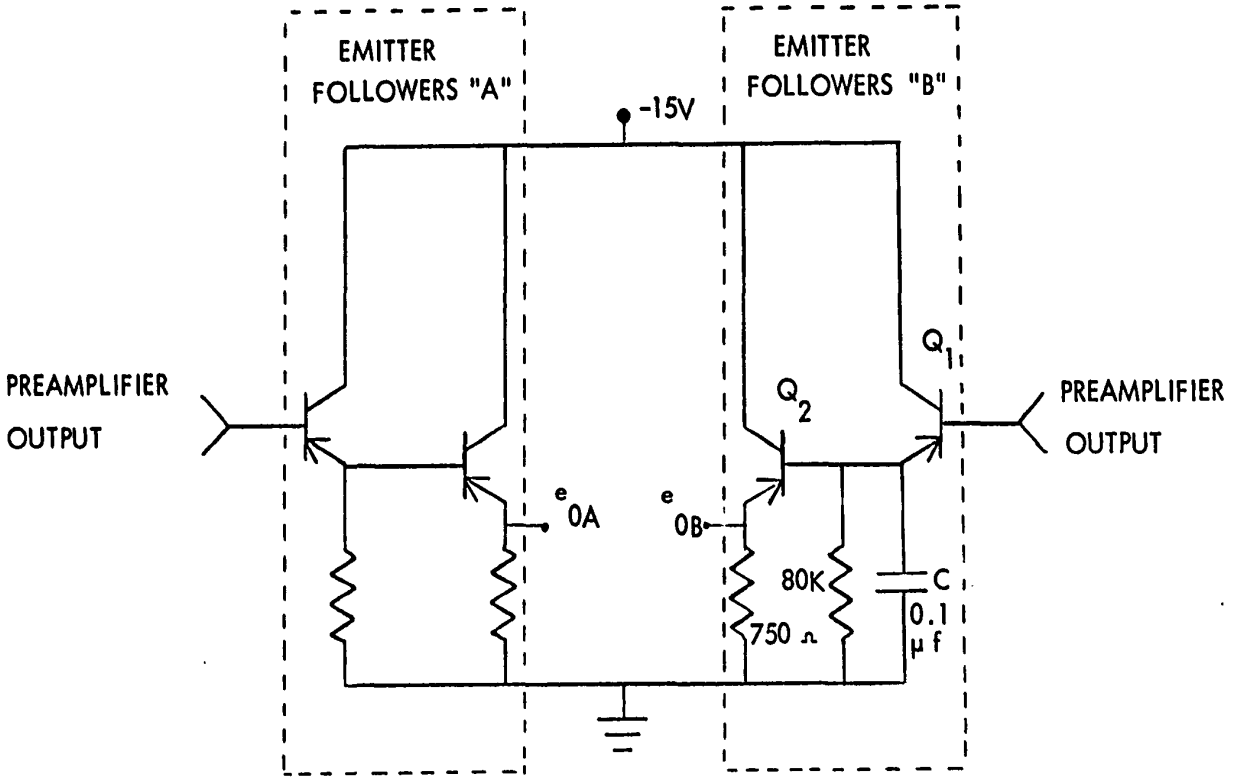


FIGURE 4.2.2. EMITTER - FOLLOWER STAGES " A " AND "B".

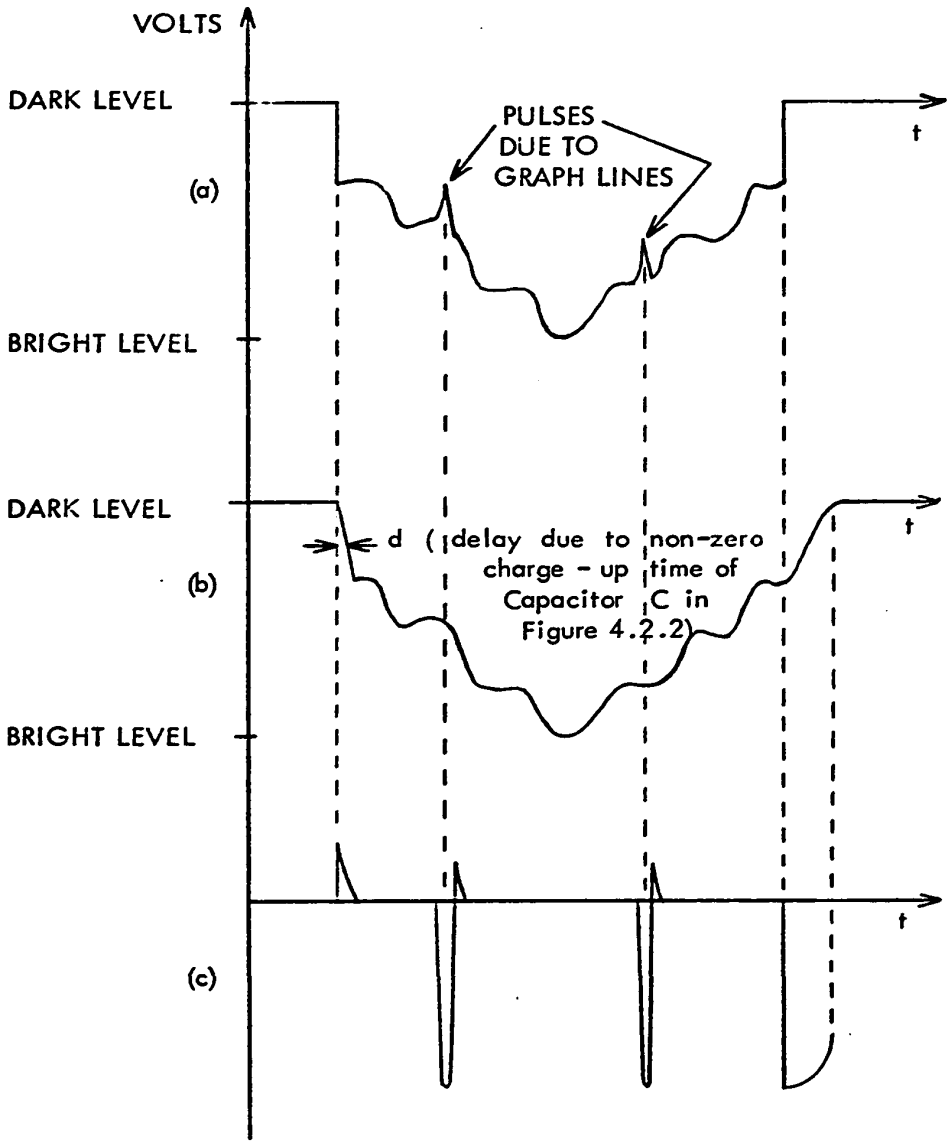
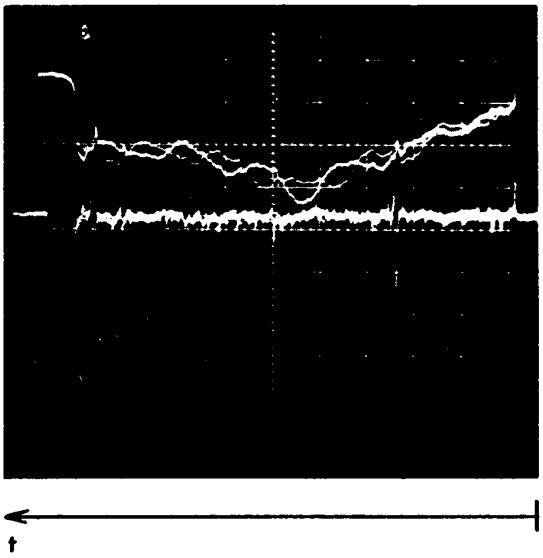


FIGURE 4.2.3.

(a) PREAMPLIFIER OUTPUT VOLTAGE.

(b) VOLTAGE e_{0B}.

(c) DIFFERENTIAL AMPLIFIER OUTPUT.



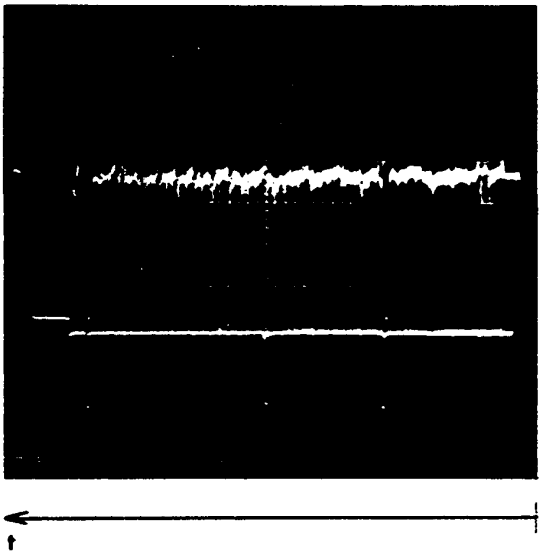
UPPER TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 1 Volt / div.

LOWER TRACE : DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 0.5 Volts / div.

P 4.3. PRE-AMPLIFIER AND DIFFERENTIAL AMPLIFIER OUTPUT SIGNALS CORRESPONDING TO A SCAN OF A GRAPH CONTAINING 2 LINES.



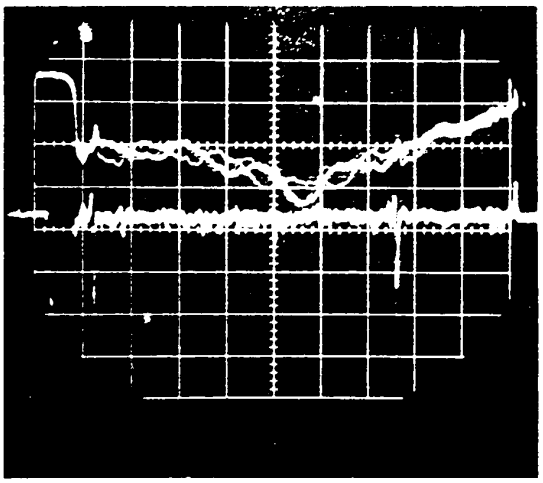
UPPER TRACE : OUTPUT VOLTAGE OF NON-LINEAR AMPLIFIER.

HOR. : 5 msec / div.
VERT. : 5 Volts / div.

LOWER TRACE : OUTPUT VOLTAGE OF SCHMITT TRIGGER.

HOR. : 5 msec / div.
VERT. : 5 Volts / div.

P 4.4. NON-LINEAR AMPLIFIER AND SCHMITT TRIGGER OUTPUT SIGNALS CORRESPONDING TO A SCAN OF A GRAPH CONTAINING 2 LINES.



t

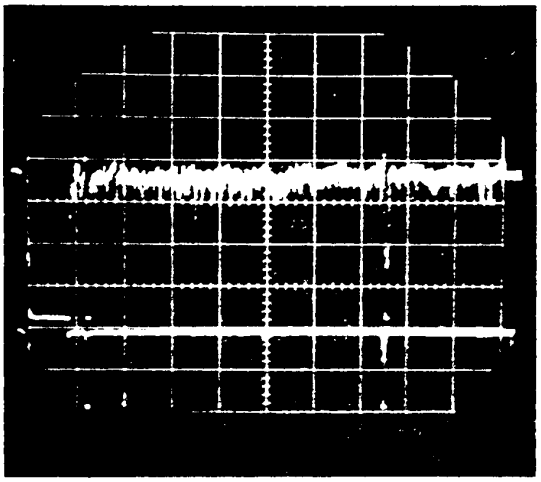
UPPER TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 1 Volt / div.

LOWER TRACE : DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE.

HOR. : 5 msec / div.
VERT. : 0.5 Volts / div.

P 4.3. PRE-AMPLIFIER AND DIFFERENTIAL AMPLIFIER OUTPUT SIGNALS CORRESPONDING TO A SCAN OF A GRAPH CONTAINING 2 LINES.



UPPER TRACE : OUTPUT VOLTAGE OF NON-LINEAR AMPLIFIER.

HOR. : 5 msec / div.
VERT. : 5 Volts / div.

LOWER TRACE : OUTPUT VOLTAGE OF SCHMITT TRIGGER.

HOR. : 5 msec / div.
VERT. : 5 Volts / div.

P 4.4. NON-LINEAR AMPLIFIER AND SCHMITT TRIGGER OUTPUT SIGNALS CORRESPONDING TO A SCAN OF A GRAPH CONTAINING 2 LINES.

amplifier. The two negative-going pulses of short duration represent the crossing of graph lines. The third pulse, occurring at the end of a scan (Figure 4.2.3 (c)) and of relatively greater width is due to the sharp positive-going edge of the pre-amplifier output at the end of a scan. This cuts off transistor Q_1 and C discharges through the 80 k Ω resistor shunted by the input impedance of the succeeding emitter-follower stage. The differential amplifier subtracts essentially this decaying voltage from the actual pre-amplifier output and therefore outputs a pulse until C discharges back to the dark voltage level. Recall that the occurrence of this third pulse was mentioned briefly in Section 3.4.3.

The output of the differential amplifier (lower trace of P 4.3) still contains line frequency and high frequency noise components. According to Rosza [4] the line frequency components still remaining are due to the non-infinite common mode rejection of the differential amplifier. The presence of the line frequency component varies the amplitudes of the signals representing graph lines. This phenomenon is most pronounced near the center of the scan, where the detection process is most sensitive.

The output of the differential amplifier is fed into two non-linear amplifier stages. In these amplifiers signals of low amplitude are attenuated whereas high amplitude signals are amplified. The output of the second non-linear stage, shown in the upper trace of picture P 4.4 is fed into a Schmitt trigger, whose output is the video pulses and is shown as the lower trace of picture P 4.4.

Mentioned earlier was the fact that the presence of line-frequency components in the output of the differential amplifier varied the amplitudes of the

signals representing graph lines. Because of this the width of the video pulses appearing at the output of the Schmitt trigger is modulated. This pulse-width modulation is in a sense random because the line frequency components are not synchronized with the rotation of the drum and hence with the scanning spot.

Rosza [4] maintained that the pulse-width modulation affected the accuracy of the graph reader. One of his test cases consisted of reading a graph containing two parallel lines, as shown in Figure 4.2.4. To obtain the distance ΔY, between the two lines his technique was to store on magnetic tape the values of Y_1 and Y_2. $\Delta Y = Y_2 - Y_1$ was then obtained through the software programs mentioned in Chapter 1. The first line, line 1, was drawn close to the edge of the graph paper, whereas line 2 was situated near the middle of the paper, where the sensitivity of the graph reader is greatest. Upon digitizing this graph Rosza noted that the digitized values of Y_2 showed a greater dispersion from the mean than those of Y_1. The reason for errors in both cases was attributed to the random-pulse-width modulation of the video pulses by the line frequency components. Accordingly, the dispersion was greater for the line (line 2) situated where the graph reading process is most sensitive because the amplitude of the line frequency component is greater in that region. Additional discussions on this and the effects upon digitization caused by high frequency noise components are relegated to Section 4.5.

4.3 The High-Pressure Mercury Arc Lamp

The mercury arc lamp is an OSRAM HBO 100 W/2, commonly employed in Honeywell visicorders. For a new lamp the rated current is 5 amps at an operating

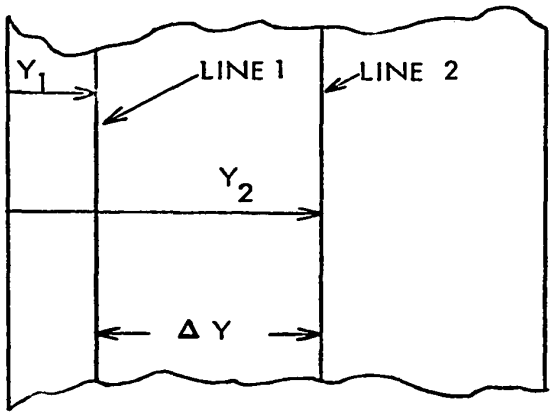


FIGURE 4.2.4. GRAPH SAMPLE ILLUSTRATING ROSA'S TECHNIQUE IN DETERMINING THE ORDINATE VALUE (Δ Y) .

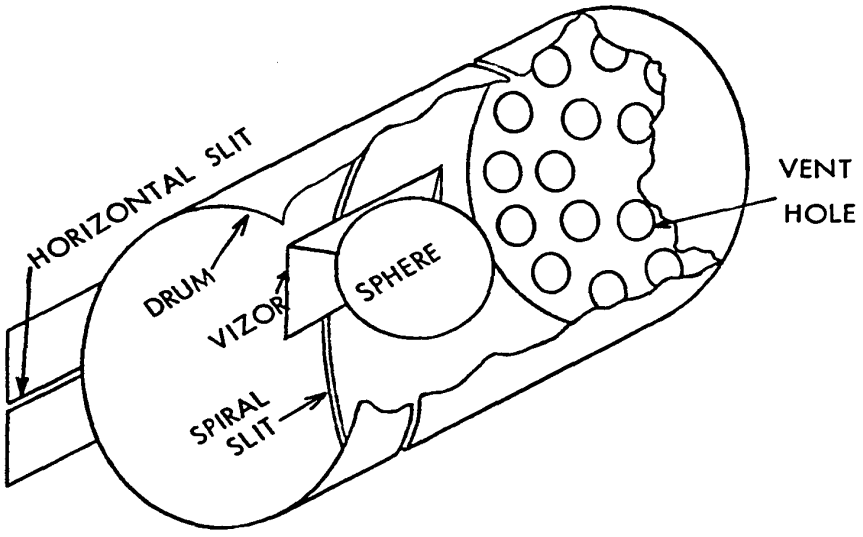


FIGURE 4.2.5. MERCURY ARC LAMP ENCLOSED WITHIN HOLLOW SPHERE.

voltage of 20 ± 4 volts. This operating point varies with age. The lifetime of the lamp depends essentially on the number of times the lamp is started. Frequent starting (establishing an arc across the electrodes of the lamp) tends to deteriorate the electrodes in the sense that the electrode spacing is increased. This alters the operating point of the lamp by increasing the operating voltage and decreasing the rated current. Honeywell recommends that a lamp be replaced once its operating point is 30 volts at 3.33 amps.

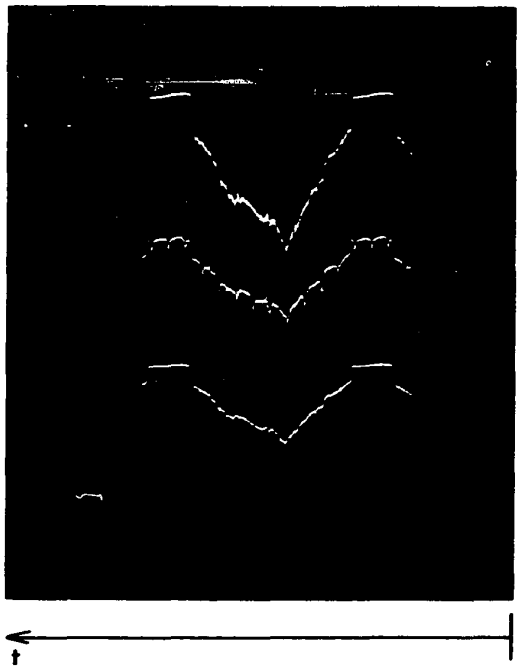
4.4 Elimination of the Line Frequency and Other Noise Components

To eliminate the effects of the line frequency components on the digitization process a regulated arc lamp power supply [27], [28] was designed and built. The circuit diagram of the supply is included in Figure A.1.2 of the Appendix. As mentioned earlier the original supply consisted of a bridge rectifier and a simple RC filter. The intensity of the arc lamp was therefore subject to variations because of the 120 H Z line ripple and variation in line voltage.

The regulated supply is designed with the intent of maintaining a constant current through the lamp. Since the lamp intensity is a function of the square of the current through it, the intensity is therefore constant when the current is constant. The regulated supply is capable of driving the lamp between the two extremes of voltage and current specified in Section 4.3. The lamp current may be adjusted by means of potentiometer P1 in Figure A.1.2. This is one way of controlling the sensitivity of the graph-reading process.

The top and bottom traces of picture P 4.5 illustrate the output of the pre-amplifier with the regulated power supply driving the arc lamp. Both traces are completely devoid of line frequency components. For the bottom trace the sensitivity of the oscilloscope was set to one-half of its value for the top trace. The paper within the graph reader in the case of picture P 4.5 was of the Esterline-Angus Company No. 4000X type of recording paper. This paper has no grid lines and its texture is moderately uniform.

The background signal in the top and bottom traces of picture P 4.5 contains both high and low frequency components. Because the paper scanned does not contain grid lines the high frequency background component is caused by other means. It will be shown shortly that this high frequency background component is due primarily to the texture of the paper being scanned. Another source of this background noise is now explained with the aid of the top and middle traces of picture P 4.5. On the left hand side in the upper trace of the picture appear three pulses, two of which occur on the grid lines of the oscilloscope. These occur coincidentally with three of the pulses evident in the middle trace of the picture. To correlate the top and middle traces it is necessary to mention a few words about the drum in which is housed the high pressure mercury arc lamp. At both ends of the drum are located vent holes for cooling the lamp. The middle trace of the picture was obtained by reflecting with a mirror, the light emerging from the vent holes. This reflected light was fed into the "darkroom", onto the paper being scanned. Thus the amount of light on the paper during a scan consisted of the scanning spot plus the light reflected onto the paper from the vent holes.



t

TOP TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR. : 10 msec / div.
VERT. : 0.5 Volt / div.

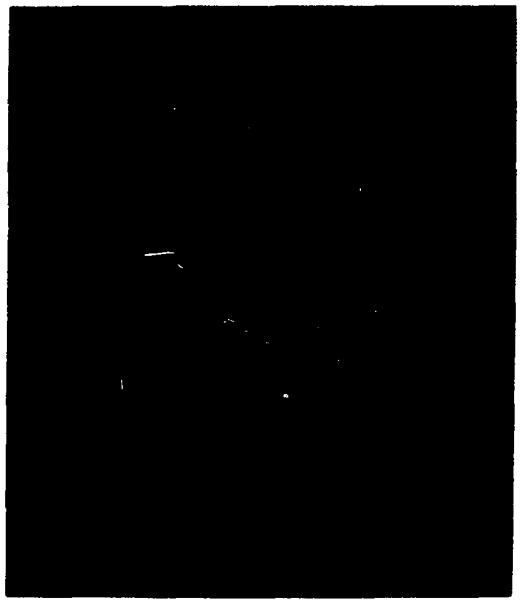
MIDDLE TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR. : 10 msec / div.
VERT.: 1 Volt / div.

BOTTOM TRACE : PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR.: 10 msec / div.
VERT.: 1 Volt / div.

P 4.5. PRE-AMPLIFIER OUTPUT SIGNALS SHOWING ELIMINATION OF LINE-FREQUENCY NOISE COMPONENTS.



t

HOR.: 10 msec / div.
VERT.: 1 Volt / div.

P 4.6. OUTPUT VOLTAGE OF PRE-AMPLIFIER WHEN MERCURY ARC LAMP IS ENCLOSED WITHIN HOLLOW SPHERE.

A fundamental difference between the three pulses in the upper trace and the corresponding ones in the middle trace is that the former pulses are directed up, towards the dark voltage level, whereas the latter are directed down, towards a brighter voltage level. The reason for the downward direction of the pulses in the middle trace is obvious. The fact that the three pulses in the upper trace are directed upward means that during their occurrence, less light is being reflected from the paper being scanned. This suggests one of two possibilities :

(i) During their occurrence, less light is falling onto the paper, or

(ii) less light is reflected because of the texture of the graph paper.

The coincidence of the three pulses in the upper trace with the corresponding ones in the middle trace makes (i) a more plausible cause. Recall that the scanning spot is produced by the interaction of two slits : a fixed horizontal slit and a spiral slit on the rotating drum. The mercury arc lamp is located within the drum and is assumed to be an ideal source of light. The inner surface of the drum is coated with a matte-black paint which, unfortunately does not completely absorb the light emanating from the source. As a result reflections occur within the drum and therefore the light leaving the spiral slit and subsequently impinging on the horizontal slit consists of both direct and reflected light. Furthermore, because the inner surface of the drum is irregular, the light reflected therefrom is not uniform. This is particularly true for both ends of the

drum where, as mentioned above, are located holes for ventilation purposes. The three pulses in the upper traces of picture P 4.5 are caused by the non-uniform reflections occurring at one end of the drum. Wherever the vent holes occur, light from the lamp exits the drum. As such the vent holes represent a reflection coefficient of zero. Otherwise the remaining inner surface of the drum has a non-zero reflection coefficient. The left side alone of the upper trace in picture P 4.5 is affected by this phenomenon because the mechanism which supports the mercury arc lamp within the drum is such that it prevents light from reaching the other end of the drum.

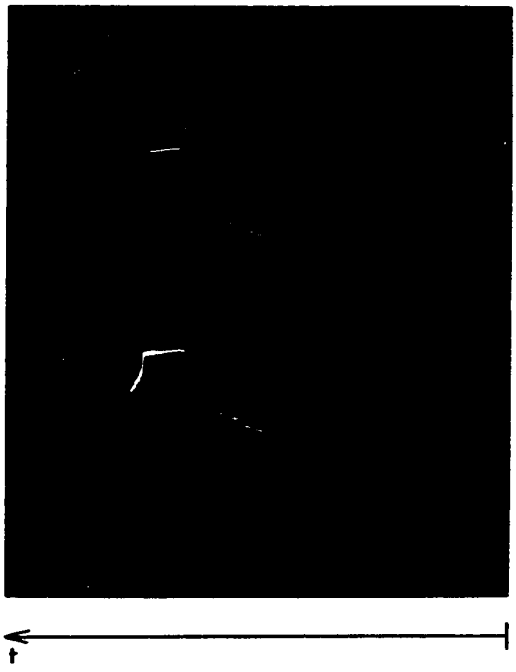
It is possible for the vent holes mentioned above to be the cause of yet another type of background component in the photomultiplier output signal. The graph reader as originally built was not light-proof in the sense that ambient light in the room where the reader was operated entered into the darkroom. This ambient light, due normally to the 60 HZ lamps which illuminate the room caused a line frequency component other than that previously described to be present in the photomultiplier output signal. To a considerable extent, this light entered the darkroom through the vent holes in the drum and subsequently through the two slits with which is produced the scanning spot. Because the room lights were turned off while the pictures referred to in the present discussion were taken the effect of extraneous light on the photomultiplier output signal is not in evidence.

It was decided that the first of the two parasitic effects attributed to the vent holes would be eliminated by enclosing the mercury arc lamp inside a hollow copper sphere. A small opening on the sphere would then permit only direct light to

impinge on the spiral slit of the drum. In this way no light is directed onto the ends of the drum, where the vent holes are located. Ideally, reflections occurring within the sphere would be directed back onto the light source and not out, onto the spiral slit.

To eliminate the second effect - that of extraneous light entering through the vent holes and subsequently into the darkroom it was decided to direct the beam of light emerging from the small opening on the sphere through a vizor which would extend out from the sphere and up close to the inner surface of the drum. The sphere and vizor arrangement is shown in Figure 4.2.5, and is such that the arc lamp, sphere, vizor and horizontal slit are on a common optical axis. Any ambient light which enters the drum is prevented from reaching the horizontal slit by the vizor.

Picture P 4.6 illustrates the output of the pre-amplifier after the addition of the sphere and vizor. Although the three pulses attributed to the vent holes are not in evidence the signal nevertheless possesses some high frequency background noise. Also evident about the point of maximum sensitivity are low frequency components. The high frequency background noise is due primarily to the texture of the paper being scanned. A good example of the effect of paper texture is shown in picture P 4.7. The two traces represent the pre-amplifier outputs obtained when two different sections of the same recording paper were scanned ! Note the difference in the high frequency noise content in the lower trace as compared with that of the upper trace. Another example of the effects of paper texture on the background signal is shown in picture P 4.8. This picture illustrates the pre-amplifier output when a Sanborn recording paper containing grid lines

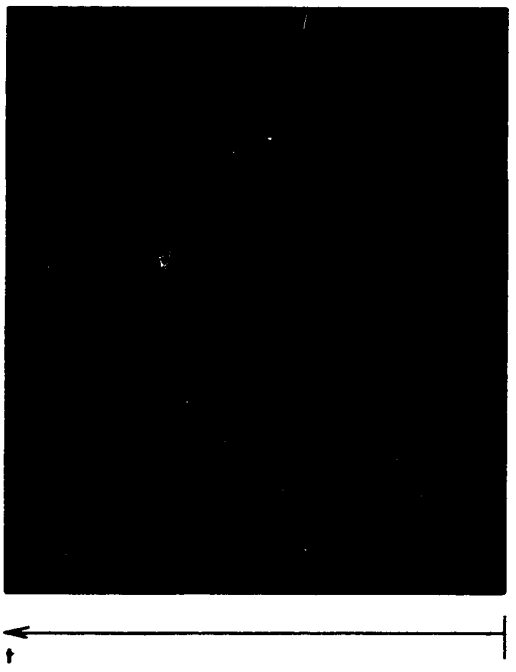


t

UPPER AND LOWER TRACES :
PRE-AMPLIFIER OUTPUT VOLTAGE.

HOR.: 10 msec / div.
VERT.: 1 Volt / div.

P 4.7. PRE-AMPLIFIER OUTPUT SIGNAL CORRESPONDING TO A SCAN OF 2 DIFFERENT SECTIONS OF ESTERLINE TYPE 1000 X RECORDING PAPER.



t

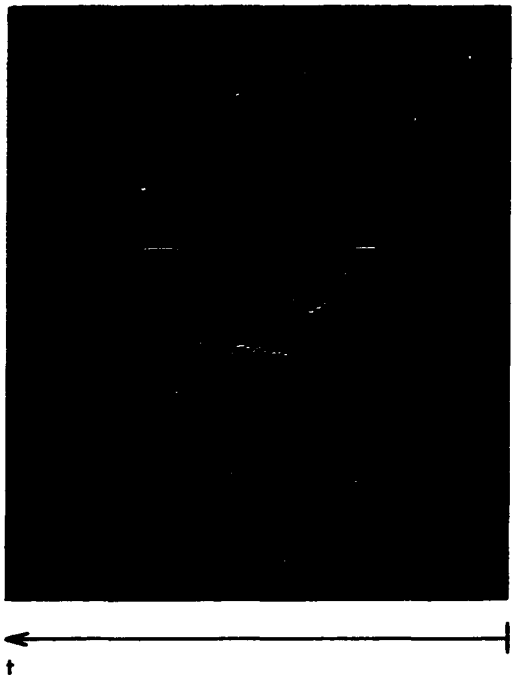
HOR.: 10 msec / div.
VERT.: 1 Volt / div.

P 4.8. PRE-AMPLIFIER OUTPUT SIGNAL CORRESPONDING TO A SCAN OF SANBORN TYPE 651-52 RECORDING PAPER.

is scanned. The scan is of shorter duration as compared with that in the pictures shown previously because Sanborn paper is not as wide as the Esterline type 1000 X.

Not much has thus far been mentioned about the low frequency background noise evident in pictures P 4.5 through P 4.8. The low frequency content in picture P 4.5 differs slightly from that in pictures P 4.6 through P 4.8. Nevertheless in both cases it seems to occur on both sides of a scan, near the more sensitive (middle) region . The fact that picture P 4.5 was taken before the sphere and vizor were installed and pictures P 4.6 through P 4.8 were taken with the sphere and vizor in place may explain why the low frequency content is different, but certainly does not justify its existence. At this time the cause of the low frequency component remains unknown.

An element of uncertainty existed before the sphere and vizor were installed. It was not known whether the mercury arc lamp would be sufficiently cooled once it was operated within the sphere. After about 50 hours of operation in this manner the preamplifier output signal deteriorated to the extent shown in picture P 4.9. The cause of this was determined to be a dark deposit which formed along the inner surface of the arc lamp in the manner shown in Figure 4.2.6. It was thought that the relatively short time (as compared with the specified lamp lifetime of a "few hundred hours") in which this took place was due to the fact that the operating temperature of the lamp was too high. To improve the ventilation it was necessary to replace the sphere and vizor with a semisphere as shown in Figure 4.2.7. This modified arrangement proved satisfactory in the



HOR.: 10 msec / div.
VERT.: 1 Volt / div.

P 4.9. PRE-AMPLIFIER OUTPUT SIGNAL SHOWING DETERIORATION OF PHOTO-MULTIPLIER OUTPUT SIGNAL CAUSED BY A DARK DEPOSIT WITHIN THE MERCURY - ARC LAMP.

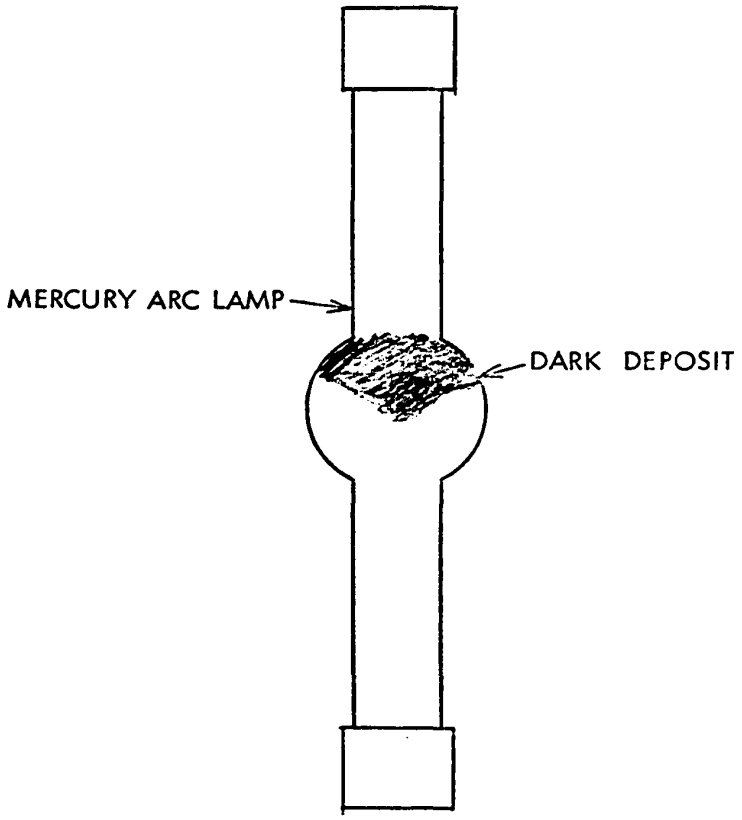


FIGURE 4.2.6. ILLUSTRATION OF DARK DEPOSIT FORMED WITHIN MERCURY ARC LAMP.

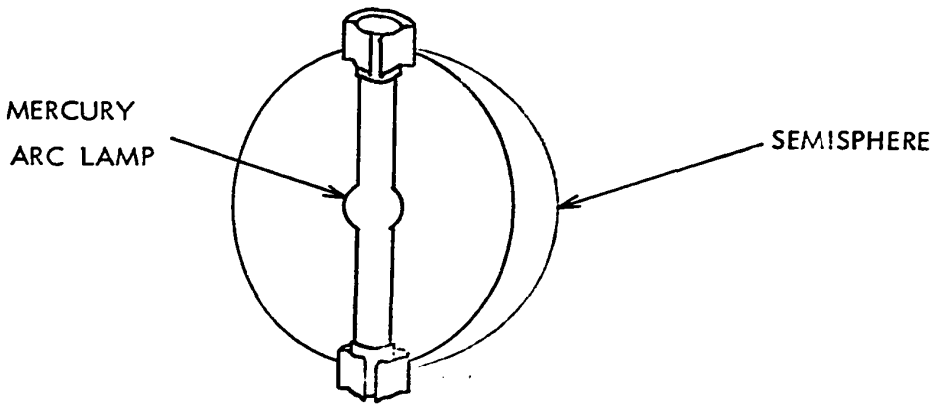


FIGURE 4.2.7. MERCURY ARC LAMP WITHIN SEMISPHERE.

sense that it properly cooled the lamp and at the same time prevented light from getting to the end of the drum and thus causing the reflection problem mentioned earlier. However, with the removal of the vizor the graph reader again became susceptible to the effect of extraneous ambient light. This problem was solved by installing the graph reader in a light-proof cabinet.

4.5 Effects of Noise on the Digitization of a Graph

In preceding sections of this chapter two types of "optical" noise were discussed. The low frequency type was comprised of two components - one asynchronous and the other synchronous with the fundamental photomultiplier signal. The second type - a higher frequency noise, is in synchronism with the photomultiplier signal.

To extract signals representing graph lines from the photomultiplier output Rosza [4] employed a filter consisting in part of two emitter-follower groups and a differential amplifier. In brief, the function of the filter was to suppress low frequency and negative-going high frequency noise components. Limitations inherent in the differential amplifier prevented a complete attenuation of low frequency components. This,together with the asynchronous nature of the low frequency component caused by an inadequately filtered power supply led to a significant dispersion of digitized graphical data. In the next chapter, results obtained by digitizing graphs after the inclusion of a well-regulated arc-lamp power supply indicate a marked improvement in the accuracy of digitization. From this, it is possible to conclude that

any dispersion effects caused by the synchronous low frequency component are negligible.

The crossing of graph lines by the scanning spot is represented on the photomultiplier output by sharp, positive-going pulses. Signals characterized by positive-going leading edges with low risetimes are not suppressed by the filter mentioned above and from these may ultimately be derived the video pulses. Because the high frequency background component exhibits somewhat similar characteristics it is conceivable that this noise might cause spurious video pulses to occur and thus lead to errors in digitized ordinate (Y) values. The probability of this depends on the sensitivity of the system, which may be controlled by the following :

(1) Arc-lamp intensity, and

(2) Photomultiplier plate voltage.

Increasing the sensitivity increases the amplitude of the noise signal and therefore increases the likelihood of false outputs. Alternatively, it may be stated that increasing the sensitivity lowers the signal-to-noise ratio (SNR) of the system, where the SNR in this case reflects the ability of the system to discriminate between pulses representing graph lines and noise.

Worthwhile mentioning here is the adverse effect of the original arc-lamp power supply on the signal-to-noise ratio. Nodes of the low frequency components evident in the photomultiplier output represent points of maximum arc lamp intensity and hence of scanning spot intensity. The amplitude of the high

frequency noise components occurring coincidentally with these "maximum" points is increased and this therefore lowers the signal-to-noise ratio of the system. Ostensibly, the inclusion of a well-regulated lamp power supply has improved the signal-to-noise ratio.

Several sources of high frequency noise were mentioned in preceding sections. Those caused by known deficiencies within the optical system were eliminated. The remaining sources, attributed to the surface quality of graph paper are listed as follows :

(1) presence of grid lines on graph paper,

(2) texture and reflectivity of graph paper, and

(3) dirt or other alien markings on graph paper.

Although the contribution to the noise caused by (1) can be minimized by affixing to the photomultiplier lens a suitable optical filter, very little control is possible over sources (2) and (3). Investigations carried out with different types of recording paper indicated that Sanborn Type 651 - 52 paper, because of its uniform texture and high reflectivity offers a comparatively high signal-to-noise ratio. When dark, well defined lines are contained on this type of paper it is possible to set the sensitivity controls to a minimum and thus optimize the SNR.

Since it is impossible to realize a very high SNR with the type of optical scanning system employed within the graph reader, false outputs will be inevitably occur. As an aid to locating and subsequently discarding erroneously

digitized data resulting from this limitation, the error detection scheme discussed in the previous chapter is incorporated within the interface circuitry.

CHAPTER V

RESULTS AND DISCUSSIONS

5.1 Operational Procedure

To operate the graph reader the drum motor is first turned on. The drum has a cooling fan affixed at one end to ensure proper cooling of the mercury arc lamp located within. Before the mercury arc lamp is turned on a protective resistor is manually switched into the arc lamp power supply circuit. The resistor, R_1 of Figure A.1.2 in the appendix is in series with the control transistor T_1. The function of the resistor is to limit the power dissipated in the collector of the transistor during the warm-up period of the arc lamp. Initially the lamp is cold when turned on. As such the voltage drop across it is in the order of a few volts, at the rated lamp current of 5 amps. In order to maintain a lamp current of 5 amps during the warm-up period requires a high collector-to-emitter voltage across the control transistor. Resistor R_1 ensures that this voltage is such that the rated collector dissipation is not exceeded. The warm-up period of the lamp is about ten minutes, at the end of which the voltage across the lamp reaches a steady state value of 20 volts. The protective resistor is then no longer required and is therefore short-circuited by means of switch S_1. While the lamp is warming up the length of the graph to be read is measured and the graph is then entered into position within the converter.

The I B M keypunch is next turned on and loaded with data cards. The AUTO-FEED switch on the keypunch is also turned on, and two data cards are forwarded to the PUNCH station by depressing the FEED key twice.

The sensitivity of the graph reader is adjusted by setting the arc lamp current and photomultiplier plate voltage potentiometers. These settings depend on the type of graph paper used and the darkness of the graph lines thereon.

The X increment is set to a desired value (1 mm $\leq \Delta x \leq$ 9 mm) with the 9-position Δ X selector switch. This controls the number of steps that a graph is advanced by the stepping motor before each scan.

The logic circuits and stepping motor power is next turned on. From hereon in the graph reading process is controlled by three illuminated pushbutton switches : STOP (red), HOLD (amber) and GO (green). When the logic circuits power is turned on the logic is automatically set into the STOP condition. The STOP key is then depressed and held thus to automatically advance the graph paper up to the point where, as discussed in Section 3.4.2, the graph reader first detects lines on the paper. After this, the GO pushbutton is depressed and graph reading commences.

While a graph is being read, two situations may arise : the process may stop, paradoxically, in a GO condition, or it may automatically transfer into a HOLD condition. In the former case the GO pushbutton remains illuminated, but no graph reading or card punching takes place. This means that the data card supply within the keypunch is exhausted. In this circumstance the process is set into a HOLD status by depressing the HOLD key. The keypunch is then loaded with data cards in the manner mentioned above. To re-commence graph reading the GO button is depressed. The latter case, where the process automatically assumes the HOLD

condition signifies that the graph reader has detected at most one graph line. This, by itself suggests one of two possibilities :

(i) The entire length of a graph has been read. To verify this the last value of X punched out on the data card is compared with the pre-measured length of the graph.

(ii) If (i) does not apply then the graph reader has failed to detect at least two graph lines during the last scan because one of the graph lines may have been too faint for the detection process. This occurs when the graph lines are not of a uniform darkness throughout the entire length of a graph. If this is the case then the sensitivity of the detection process is increased by increasing the arc lamp current and / or the photomultiplier plate voltage. The GO button is then depressed and the reading of a graph resumes.

As mentioned in earlier chapters the format of the graphical data punched out on the data cards is simple. Each coordinate set (X, Y) is contained on 8 columns of a card. The first four columns contain X, in millimeters and the next 4 columns Y, in inches. Therefore, 10 coordinate sets are contained on each 80-column card. Whenever the graph reader fails to detect the necessary number of graph lines (case (ii) above), the current X, along with a Y value of 0000 is punched. If more than three graph lines are detected during a particular scan the current X, along with a Y of 9999 is then punched.

5.2 Results

To evaluate the performance of the graph reader several types of curves were digitized. The curves were all drawn on SANBORN 2 - channel Type 651 - 52 recording paper. A green filter (KODAK No. 58 WRATTEN Gelatin Filter) was placed on the photomultiplier lens in order to minimize the parasitic effect of green grid lines contained on this type of recording paper. The digitization increment, ΔX, was set to 1 millimeter for each of the curves.

The graph sample of Figure 5.2.1 contains two parallel straight lines spaced 1 inch apart (drawn manually, with straight edge accuracy) for : $0 < X < 50$ millimeters. In the interval : 50 mm $< X <$ 53 mm, no lines were drawn, whereas the section $53 < X < 100$ mm again contains two parallel lines, along with a third line drawn at $70 < X < 80$ mm. This particular graph was digitized twice, in order to illustrate the following :

(1) The operation of the PUNCH 0's and the PUNCH 9's flip - flops described in Section 3.4.3.

(2) The possible occurrence of an extraneous pulse at the end of a scan, also mentioned in Section 3.4.3.

(3) The effect on the accuracy of digitization when the marker pulse generator is malfunctioning.

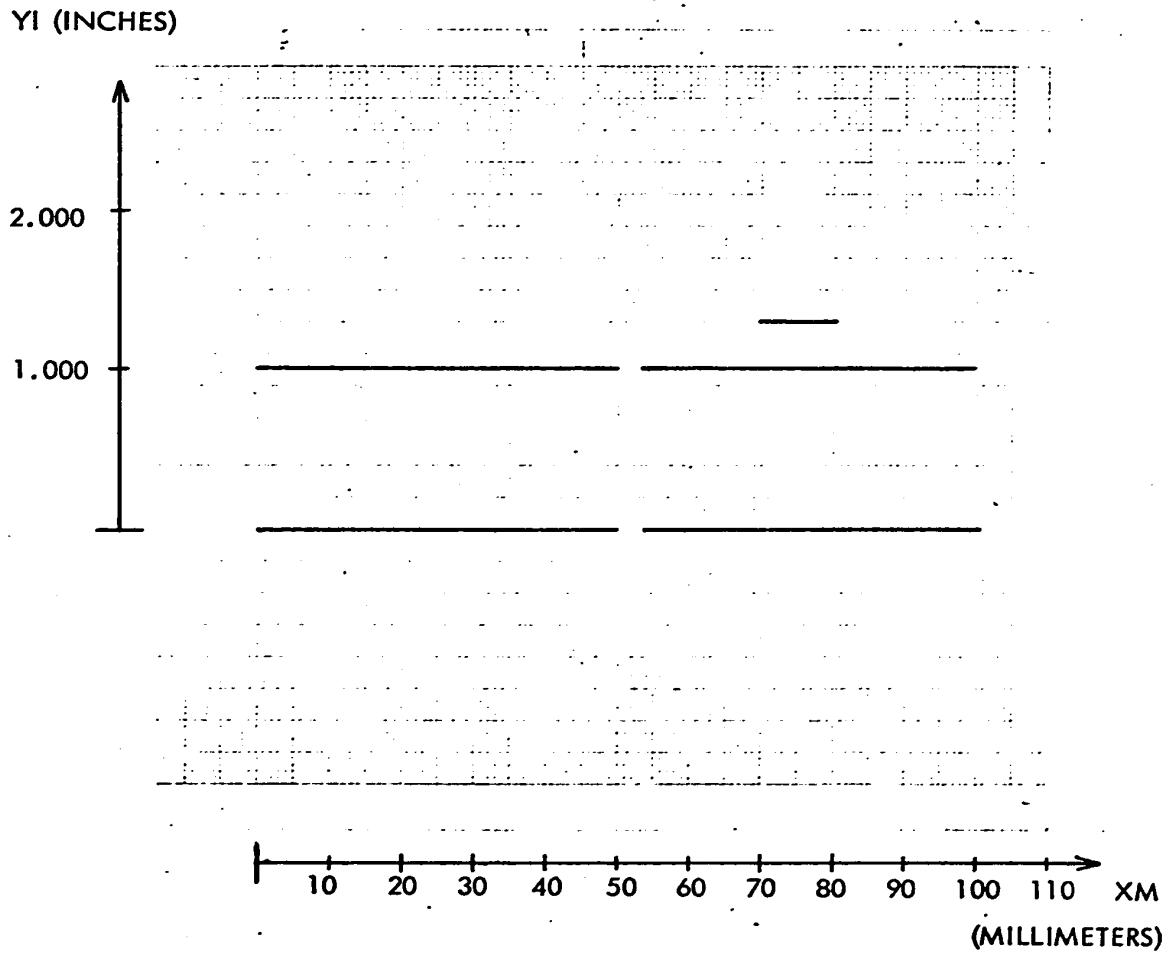


FIGURE 5.2.1. GRAPH SAMPLE CONTAINING PARALLEL LINES.

Before digitization was begun the graph sample was advanced to the point $X = 0$ (within one millimeter) by making use of the automatic advance feature outlined in the preceding section.

A listing of the data card output resulting from the first digitization is shown in Figure 5.2.2, where the column labeled XM lists the X values, in millimeters, and the column YI lists the corresponding digitized Y values in inches. The third column contains the deviation, ΔY, between YI and the actual value of Y, which is 1 inch.

For $0 < XM < 50$ mm, significant deviations occur at :

$XM = 12$ ($\Delta Y = -0.135$ inches)

$XM = 32$ ($\Delta Y = -0.020$ inches)

these will be discussed shortly.

For $49 \leq X \leq 52$, YI = 0.000 inches. Note that no graph lines are contained on the sample during this interval. Because less than two video pulses were detected in this interval, the PUNCH 0's flip-flop was automatically enabled, hence causing a value of YI = 0000 to be punched on the data card. After each set of 0's was punched, the logic assumed the HOLD condition. The GO (START) key was therefore depressed four times in order to proceed to XM = 53, where graph lines recur.

In the interval $53 \leq XM \leq 68$ mm, no significant deviations in the YI values occur, whereas for $69 \leq X \leq 79$ mm, YI is 9999. In this latter interval,

FIGURE 5.2.2. LISTING OF DATA OBTAINED FROM THE FIRST DIGITIZATION OF FIGURE 5.2.1.

XM	YI	ΔY
1,000	995	-0.005
2,000	1000	-0,000
3,000	995	-0.005
4,000	1000	-0,000
5,000	1000	-0,000
6,000	995	-0,005
7,000	1000	-0,000
8,000	1000	-0,000
9,000	1000	-0,000
10,000	995	-0,005
11,000	990	-0,010
12,000	865	-0,135
13,000	1000	-0,000
14,000	1000	-0,000
15,000	995	-0,005
16,000	1000	-0,000
17,000	1000	-0,000
18,000	995	-0,005
19,000	995	-0,005
20,000	995	-0,005
21,000	1015	0,015
22,000	995	-0.005
23,000	1000	-0,000
24,000	995	-0,005
25,000	995	-0,005
26,000	1005	0,005
27,000	1000	-0,000
28,000	1000	-0,000
29,000	1000	-0,000
30,000	1000	-0,000
31,000	1000	-0,000
32,000	980	-0,020
33,000	1000	-0,000
34,000	995	-0,005
35,000	1005	0,005
36,000	1000	-0,000
37,000	1000	-0,000
38,000	1000	-0,000
39,000	1000	-0,000
40,000	990	-0,010
41,000	1000	-0,000
42,000	1000	-0,000
43,000	1000	-0,000
44,000	1005	0,005
45,000	1005	0,005
46,000	1000	-0,000
47,000	1000	-0,000
48,000	1000	-0,000
49,000	0	*****
50,000	0	*****
51,000	0	*****
52,000	0	*****
53,000	1005	0,005
54,000	1005	0,005

55.000	1005	0.005
56.000	1005	0.005
57.000	1000	-0.000
58.000	1005	0.005
59.000	1005	0.005
60.000	1005	0.005
61.000	1005	0.005
62.000	1005	0.005
63.000	1005	0.005
64.000	1005	0.005
65.000	1005	0.005
66.000	1005	0.005
67.000	1000	-0.000
68.000	995	-0.005
69.000	9999	*****
70.000	9999	*****
71.000	9999	*****
72.000	9999	*****
73.000	9999	*****
74.000	9999	*****
75.000	9999	*****
76.000	9999	*****
77.000	9999	*****
78.000	9999	*****
79.000	9999	*****
80.000	985	-0.015
81.000	995	-0.005
82.000	995	-0.005
83.000	995	-0.005
84.000	995	-0.005
85.000	970	-0.030
86.000	995	-0.005
87.000	1000	-0.000
88.000	995	-0.005
89.000	995	-0.005
90.000	990	-0.010
91.000	995	-0.005
92.000	1000	-0.000
93.000	1005	0.005
94.000	1000	-0.000
95.000	1000	-0.000
96.000	1000	-0.000
97.000	995	-0.005
98.000	1000	-0.000
99.000	995	-0.005
100.000	3210	2.210
101.000	0	*****

FIGURE 5.2.2. (CONTINUED).

the PUNCH 9's flip-flop was automatically enabled because the scanning unit sensed more than three graph lines. A fourth video pulse occurred in this case because of the 5 inch width of the recording paper as compared with the scanning range of the light spot, which is 6.1 inches. As soon as the spot traversed the paper, it then scanned the matte-black background in the "darkroom" where the graph paper was contained. This black surface was "interpreted" by the scanning unit as a graph line (in the manner described in Section 4.2), thus resulting in the generation of a fourth video pulse.

The interval $80 \leq XM \leq 99$ mm contains one significant deviation at $XM = 85$, where $\Delta Y = -0.030$ inches. Note that this deviation, along with those at $XM = 12$ and $XM = 32$ are all negative. Due investigation revealed that these negative deviations were caused by a faulty lamp in the marker pulse generator (Figure 2.1.1). This malfunction caused a sporadic absence of marker pulses. The output of the generator was at times less than the 740 pulses which normally occur during one revolution of the marker disc.

Before the second digitization of Figure 5.2.1 is discussed it is worthwhile elaborating upon the value of $Y1$ for $XM = 100$, which is listed as 3.210 inches. A close scrutiny of the graph sample reveals that the lower line (X axis) is slightly longer than the upper one (at about $XM = 100$ mm). In this case, the scanning spot traversed the lower line, yielding one video pulse. The second video pulse was then, as mentioned above, generated as soon as the spot left the graph paper. $Y1 = 3.210$ inches is therefore the distance between the line representing the X axis and the mid-

point of the second video pulse. At X M = 101 mm a value of Y I = 0000 was punched, whereupon the logic automatically assumed the HOLD condition.

A listing of the data card output for the second digitization of the graph sample of Figure 5.2.1 appears in Figure 5.2.3. This digitization was made after a new lamp was placed in the marker pulse generator. The listing contains no significant deviations in Y I wherever two lines occur on the graph sample. At XM = 51 mm however, this second digitization has yielded a Y I value of 3.145 inches, as compared to a Y I of 0000 in the first digitization. Note the comparative similarity between this value of Y I = 3.145 inches and that obtained for X M = 100 millimeters : 3.210 inches for the first digitization and 3.215 inches for the second. This indicates that during the second run, the scanning unit has detected a graph line at X M = 51. In actual fact the X axis line was originally drawn (by error) without a discontinuity at $50 \leq XM \leq 53$ mm. In order to illustrate the operation of the PUNCH 0's flip-flop, this section was covered with SNOPAKE, a white paint-on product normally used by typists to correct typing errors. The SNOPAKE settled in the form of a small shiny lump on the graph sample. As the scanning spot traversed this lump, one of two things happened :

(1) The scanning spot "hit" the lump at an angle such that a relatively small amount of light was reflected back onto the photomultiplier lens or,

FIGURE 5.2.3. LISTING OF DATA OBTAINED FROM THE SECOND DIGITIZATION OF FIGURE 5.2.1.

XM	YI	ΔY
1,000	995	-0,005
2,000	1000	-0,000
3,000	1000	-0,000
4,000	1000	-0,000
5,000	1000	-0,000
6,000	1000	-0,000
7,000	1005	0,005
8,000	1005	0,005
9,000	1000	-0,000
10,000	1000	-0,000
11,000	1005	0,005
12,000	1000	-0,000
13,000	1000	-0,000
14,000	1000	-0,000
15,000	1005	0,005
16,000	1005	0,005
17,000	1005	0,005
18,000	1000	-0,000
19,000	1000	-0,000
20,000	1000	-0,000
21,000	1005	0,005
22,000	1005	0,005
23,000	1005	0,005
24,000	1000	-0,000
25,000	1005	0,005
26,000	1005	0,005
27,000	1005	0,005
28,000	1005	0,005
29,000	1005	0,005
30,000	1005	0,005
31,000	1005	0,005
32,000	1005	0,005
33,000	1000	-0,000
34,000	1000	-0,000
35,000	1005	0,005
36,000	1005	0,005
37,000	1000	-0,000
38,000	1005	0,005
39,000	1000	-0,000
40,000	1005	0,005
41,000	1005	0,005
42,000	1005	0,005
43,000	1005	0,005
44,000	1005	0,005
45,000	1005	0,005
46,000	1005	0,005
47,000	1005	0,005
48,000	995	-0,005
49,000	0	*****
50,000	0	*****
51,000	3145	2,145
52,000	0	*****
53,000	1000	-0,000
54,000	1000	-0,000

55.000	1000	-0.000
56.000	1000	-0.000
57.000	995	-0.005
58.000	1000	-0.000
59.000	995	-0.005
60.000	995	-0.005
61.000	995	-0.005
62.000	995	-0.005
63.000	995	-0.005
64.000	995	-0.005
65.000	995	-0.005
66.000	1000	-0.000
67.000	995	-0.005
68.000	995	-0.005
69.000	9999	*****
70.000	9999	*****
71.000	9999	*****
72.000	9999	*****
73.000	9999	*****
74.000	9999	*****
75.000	9999	*****
76.000	9999	*****
77.000	9999	*****
78.000	9999	*****
79.000	9999	*****
80.000	995	-0.005
81.000	995	-0.005
82.000	1000	-0.000
83.000	995	-0.005
84.000	995	-0.005
85.000	1000	-0.000
86.000	995	-0.005
87.000	1000	-0.000
88.000	995	-0.005
89.000	995	-0.005
90.000	995	-0.005
91.000	1000	-0.000
92.000	995	-0.005
93.000	1000	-0.000
94.000	1000	-0.000
95.000	995	-0.005
96.000	990	-0.010
97.000	995	-0.005
98.000	995	-0.005
99.000	995	-0.005
100.000	3215	2.215
101.000	0	*****

FIGURE 5.2.3. (CONTINUED).

(2) the thin but very sharp discontinuity in texture between the lump and the remainder of the graph paper was "interpreted" by the photomultiplier as a graph line.

In either case, a video pulse was generated at this point and, together with the second video pulse occurring at the edge of the paper yielded a Y I value of 3.145 inches at X M = 51 mm.

The second graph sample which was digitized consisted of the semi-circle shown in Figure 5.2.4. Before this graph was digitized, considerable difficulty was had in setting the graph sample exactly at the point where X = 0. This is due to the fact that the automatic paper advance mechanism is accurate to within one millimeter only, in that it has to first sense graph lines before it stops advancing the paper. To start digitization at X = 0, the true value of Y at X M = 1 mm was computed (Y = 0.395"). The paper was then repeatedly set (by trial and error) at approximately X M = 0 and the GO (START) key depressed until a value of Y I = 0.395 inches, corresponding to X M = 1 mm was indicated on the register of the graph reader.

The numerical data included in Figure 5.2.5, corresponding to the digitized semi-circle is labelled as follows :

X M represents the X value, in millimeters, along the diameter of the semicircle.

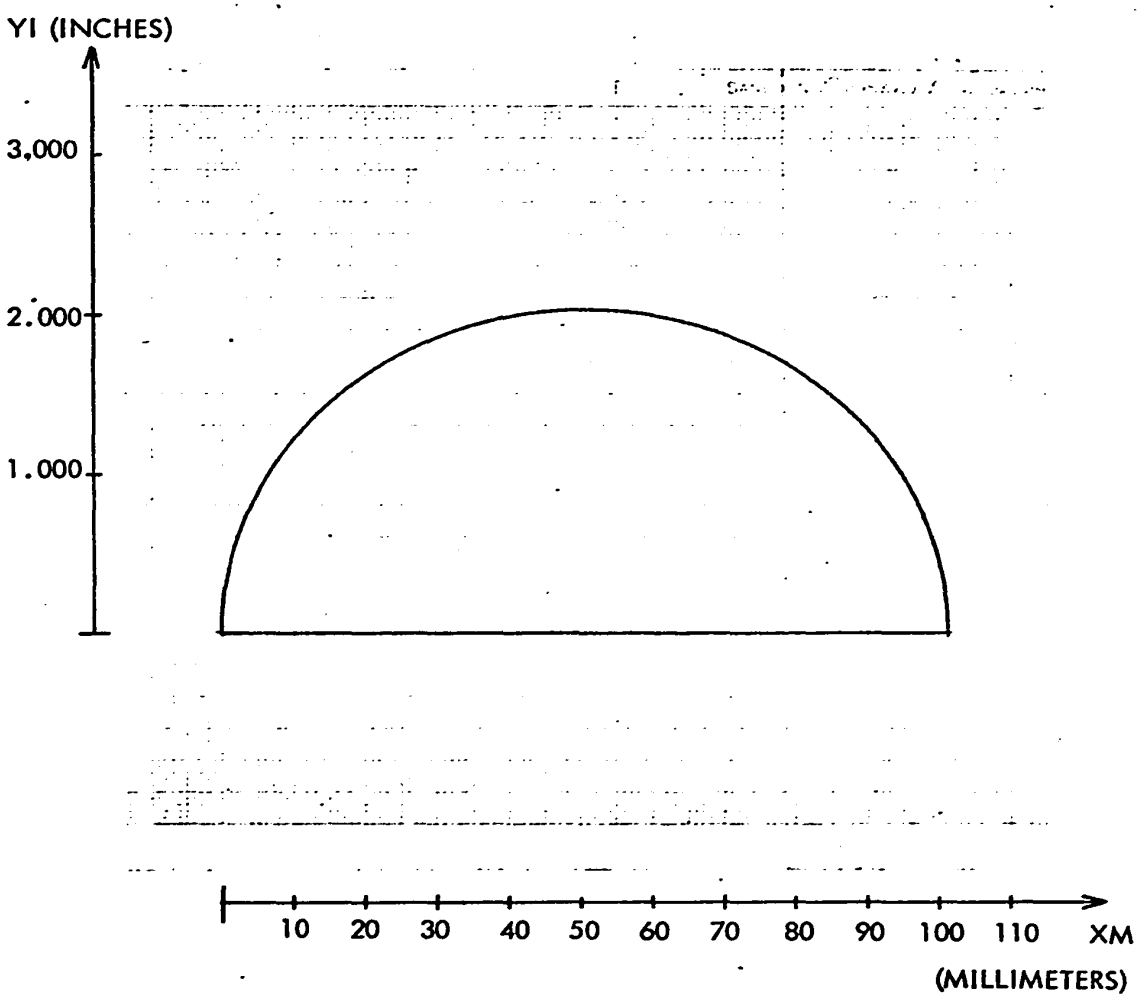


FIGURE 5.2.4. GRAPH SAMPLE CONTAINING SEMI-CIRCLE.

FIGURE 5.2.5. LISTING OF DATA OBTAINED BY DIGITIZING THE SEMI-CIRCLE OF FIGURE 5.2.4.

RADIUS = 2.000INCHES

XM	YT	YI	ΔY
1.000	0.395	395	0.000
2.000	0.556	560	0.004
3.000	0.677	675	-0.002
4.000	0.778	770	-0.008
5.000	0.865	855	-0.010
6.000	0.943	935	-0.008
7.000	1.013	1005	-0.008
8.000	1.077	1075	-0.002
9.000	1.137	1130	-0.007
10.000	1.192	1190	-0.002
11.000	1.243	1240	-0.003
12.000	1.291	1295	0.004
13.000	1.336	1340	0.004
14.000	1.379	1375	-0.004
15.000	1.419	1410	-0.009
16.000	1.457	1455	-0.002
17.000	1.493	1485	-0.003
18.000	1.527	1520	-0.007
19.000	1.560	1550	-0.010
20.000	1.590	1590	-0.000
21.000	1.620	1615	-0.005
22.000	1.648	1645	-0.003
23.000	1.674	1680	0.006
24.000	1.699	1695	-0.004
25.000	1.723	1715	-0.008
26.000	1.745	1740	-0.005
27.000	1.767	1765	-0.002
28.000	1.787	1780	-0.007
29.000	1.806	1800	-0.006
30.000	1.825	1820	-0.005
31.000	1.842	1835	-0.007
32.000	1.858	1850	-0.008
33.000	1.873	1870	-0.003
34.000	1.887	1885	-0.002
35.000	1.901	1910	-0.001
36.000	1.913	1910	-0.003
37.000	1.925	1920	-0.005
38.000	1.935	1935	-0.000
39.000	1.945	1945	-0.000
40.000	1.954	1955	0.001
41.000	1.962	1965	0.003
42.000	1.970	1970	0.000
43.000	1.976	1975	-0.001
44.000	1.982	1980	-0.002
45.000	1.987	1990	0.003
46.000	1.991	1990	-0.001
47.000	1.994	1990	-0.004
48.000	1.997	1995	-0.002
49.000	1.999	1995	-0.004
50.000	2.000	1995	-0.005
51.000	2.000	1995	-0.005
52.000	1.999	2000	0.001

53.000	1.998	2000	0.002
54.000	1.995	1995	-0.001
55.000	1.993	1995	0.002
56.000	1.989	1990	0.001
57.000	1.985	1980	-0.005
58.000	1.980	1980	0.000
59.000	1.974	1970	-0.004
60.000	1.967	1965	-0.002
61.000	1.959	1960	0.001
62.000	1.951	1950	-0.001
63.000	1.941	1945	0.004
64.000	1.931	1935	0.004
65.000	1.920	9999	*****
66.000	1.908	1915	0.007
67.000	1.896	1895	-0.001
68.000	1.882	1885	0.003
69.000	1.867	1870	0.003
70.000	1.852	1855	0.003
71.000	1.835	1840	0.005
72.000	1.818	1820	0.002
73.000	1.799	1810	0.011
74.000	1.779	1780	0.001
75.000	1.758	1770	0.012
76.000	1.737	1745	0.008
77.000	1.713	1725	0.012
78.000	1.689	1700	0.011
79.000	1.664	1670	0.006
80.000	1.637	1645	0.008
81.000	1.608	1610	0.002
82.000	1.578	1585	0.007
83.000	1.547	1545	-0.002
84.000	1.514	1515	0.001
85.000	1.479	1485	0.006
86.000	1.442	1445	0.003
87.000	1.403	1400	-0.003
88.000	1.362	1365	0.003
89.000	1.318	1310	-0.008
90.000	1.272	1275	0.003
91.000	1.223	1230	0.007
92.000	1.170	1170	-0.000
93.000	1.113	1115	0.002
94.000	1.052	1055	0.003
95.000	0.986	985	-0.001
96.000	0.913	915	0.002
97.000	0.832	825	-0.007
98.000	0.740	735	-0.005
99.000	0.632	630	-0.002
100.000	0.498	485	-0.013
101.000	0.307	300	-0.007

FIGURE 5.2.5. (CONTINUED).

Y I represents the Y value, in inches, obtained from the graph reader.

Y T represents the theoretical value of Y, in inches, obtained by solving for Y T, the equation $(X I - R)^2 + Y T^2 = R^2$, (R = 2 inches) by means of a computer program.

Δ Y represents the deviation between Y I and Y T .

Note that no deviation is included for X M = 65 mm, where a Y I = 9999 is listed. Since a Y value of 9999 is automatically punched whenever more than three video pulses occur in a single scan, the graph reader has, in this instance sensed at least one "spurious" graph line. This would result in a generation of at least 4 video pulses during this scan (2 representing the graph lines, 1 at the edge of the graph paper and 1 spurious pulse). This spurious output is due to the fact that the sensitivity of the graph line detection process was increased when the semi-circle was digitized because the lines defining the semi-circle and reference X axis were not as thick and dark as those contained on the graph sample of Figure 5.2.1.

Increasing sensitivity decreases the signal-to-noise ratio of the graph reader and thus increases the amplitude of spurious signals occurring on the output of the photomultiplier. In this case, no dirt or other markings are visible on the graph sample at X M = 65 mm. The most probable cause of the spurious signal is therefore

the texture of the graph paper along the path traversed by the light spot at XM = 65 mm. The possibility of the grid lines causing this noise is highly unlikely since it occurred only once in 102 scans !

Discounting the value of Y I = 9999 at X M = 65 mm, the remaining Y I values are quite accurate. The maximum deviation of $\Delta Y = -0.013$ inches occurs at X M = 100 mm. The digitized data was plotted (by hand) and is shown in Figure 5.2.6.

5.3 Accuracy

Upon performing a statistical study of digitized data obtained by his method, Rosza [4] formed the following conclusion with regard to the accuracy of the graph reader : 94 % of the data digitized by him was so done with an accuracy of 0.25 %. Since he calculated his error with respect to a scanning length of 6.0 inches, this means that 6 % of his data had a deviation in excess of 0.015 inches.

Referring to the three digitizations included in the present work the accuracy is as follows :

(1) Curve of Figure 5.2.1, RUN 1.

Discounting the points where Y I = 0000, Y I = 9999, Y I = 3.210 (at X M = 100 mm) and, because of the faulty marker pulse generator, those at

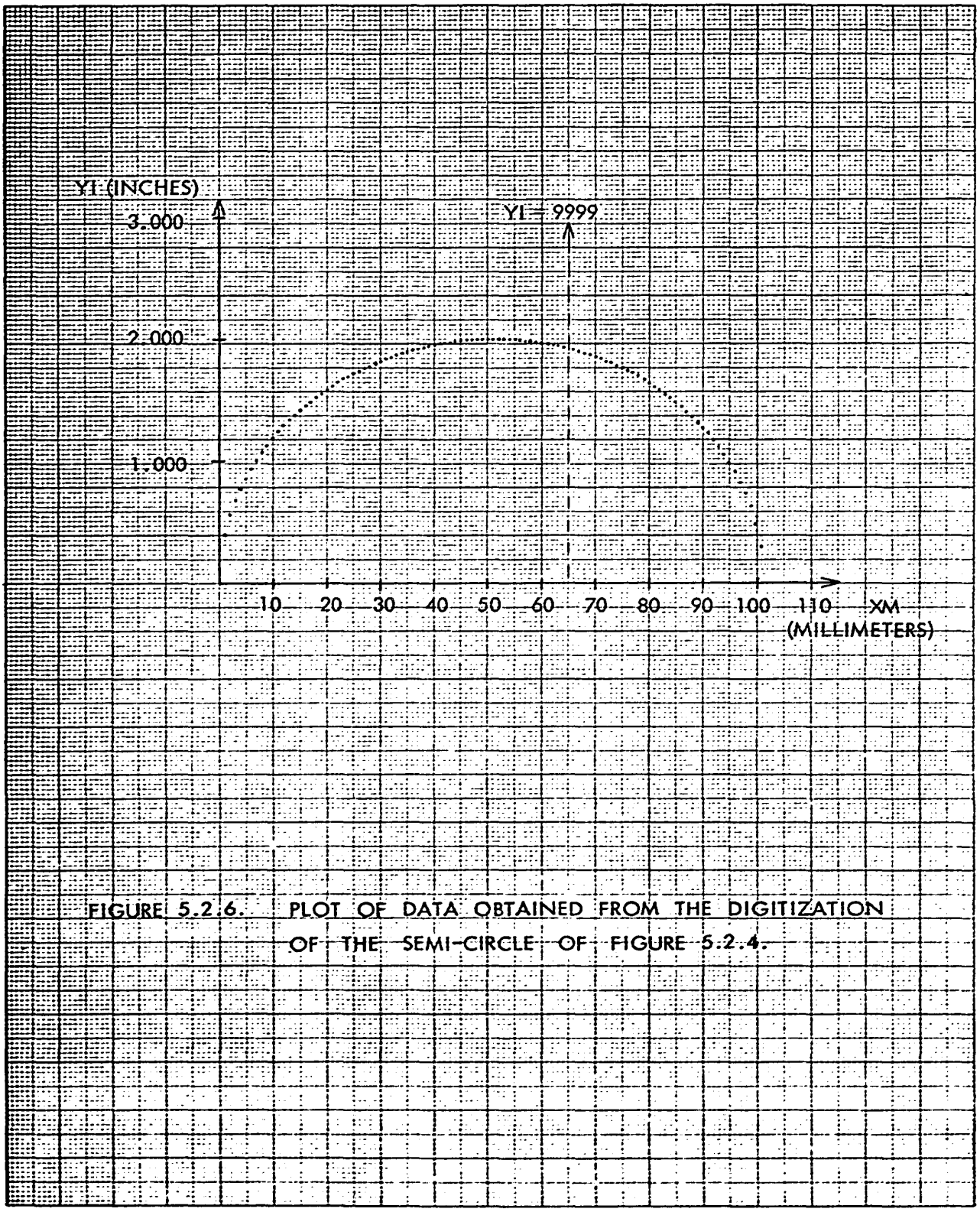


FIGURE 5.2.6. PLOT OF DATA OBTAINED FROM THE DIGITIZATION OF THE SEMI-CIRCLE OF FIGURE 5.2.4.

X M = 12, X M = 32, X M = 85 mm, the maximum deviation in this digitization is ΔY = 0.015 inches. Therefore of the 81 "legitimate" scans in this digitization it can be said that 100 % of the data is digitized with or within an accuracy of 0.25 % (based on a 6.0" scanning length) or 0.246 % if based on the actual scanning length of 6.1 inches.

(2) Curve of Figure 5.2.1, RUN 2.

Discounting the points where Y I = 0000, Y I = 9999, Y I = 3.215 (at X M = 100 mm) and Y I = 3.145 inches at X M = 51 mm, the maximum deviation is ΔY = -0.010 inches. Therefore of the 84 "legitimate" scans in this digitization, 100 % of the data is digitized with or within an accuracy of 0.16 %, if based on the actual scanning length of 6.1 inches.

(3) Curve of Figure 5.2.4.

Discounting the point at X M = 65 mm, where Y I = 9999, the maximum deviation is : ΔY = -0.013 inches, occurring at X M = 100 mm. This represents a maximum error of 0.213 % (based on a 6.1" scanning length) for 100 "legitimate" scans.

The three digitizations mentioned above represent a total number of 265 "legitimate" scans. Based on this number of samples it can be concluded that the maximum error is 0.246 %, and that 100 % of this graphical data has been digitized with this accuracy, as compared with 94 % in Rosza's case. Rosza's conclusions were based on approximately the same number of samples.

The improvement in accuracy is attributed to the regulated constant-current power supply which drives the arc lamp. Recall that the original lamp power was derived from a full-wave rectifier, the output of which was fed to a simple R-C filter. This, as illustrated in Chapter IV, caused significant line-frequency components to appear in the output signal of the photomultiplier. The ultimate effect of these line components was to modulate the width of the video pulses. This is illustrated in Figure 5.2.7, where waveform (a) depicts a photomultiplier output for two parallel lines at some time $T_m \leq t \leq T_n$, whereas waveform (c) depicts the photomultiplier output at another time, $T_i \leq t \leq T_k$. Line-frequency components are included in these waveforms. In waveform (e) is assumed the photomultiplier output resulting from an "ideal" scan. Waveforms (b), (d) and (f) show the video pulses derived from the three photomultiplier outputs defined above. Y_3 in waveform (f) represents the actual distance between the two lines from which the video pulses are derived, whereas Y_1 (waveform (b)) and Y_2 (waveform (d)) are in error due to video pulse width modulation.

Figures 5.2.8 and 5.2.9 depict in an indirect manner the effects of video pulse width modulation. The graph of Figure 5.2.8 was digitized and the digitized data plotted as shown in Figure 5.2.9. The dispersion of the plotted data is particularly noticeable at $14 < X < 35$ mm and $55 < X < 75$ mm, where the thickness of the lines representing the sawtooth waveform varies significantly in Figure 5.2.8. If the sawtooth of Figure 5.2.8 were ideal in that its line thickness was perfectly uniform, the effect of video pulse width modulation attributed to the original lamp power supply would be somewhat similar to that shown in Figure 5.2.9, although the dispersion would be more random in nature.

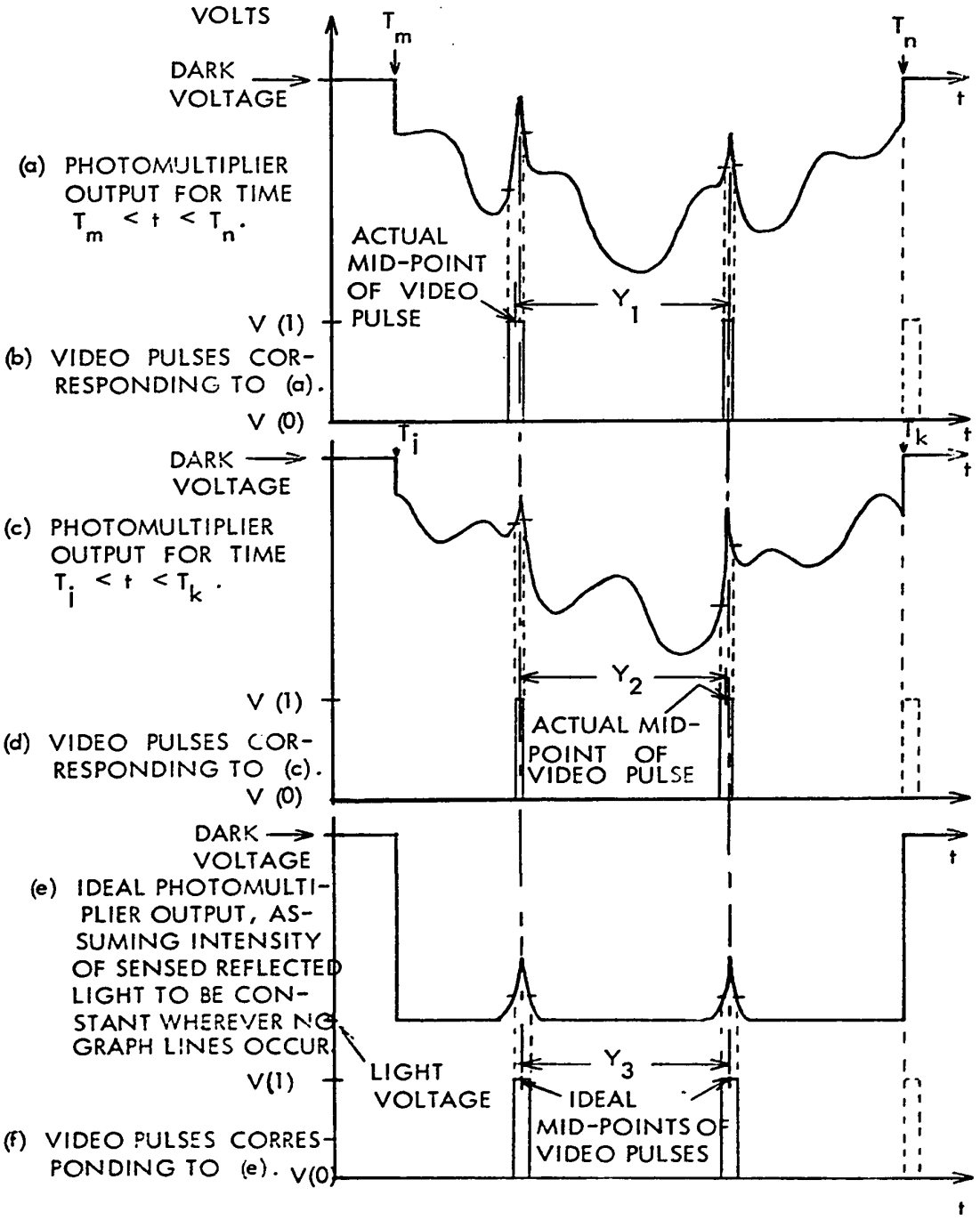


FIGURE 5.2.7. PULSE-WIDTH MODULATION OF VIDEO PULSES.

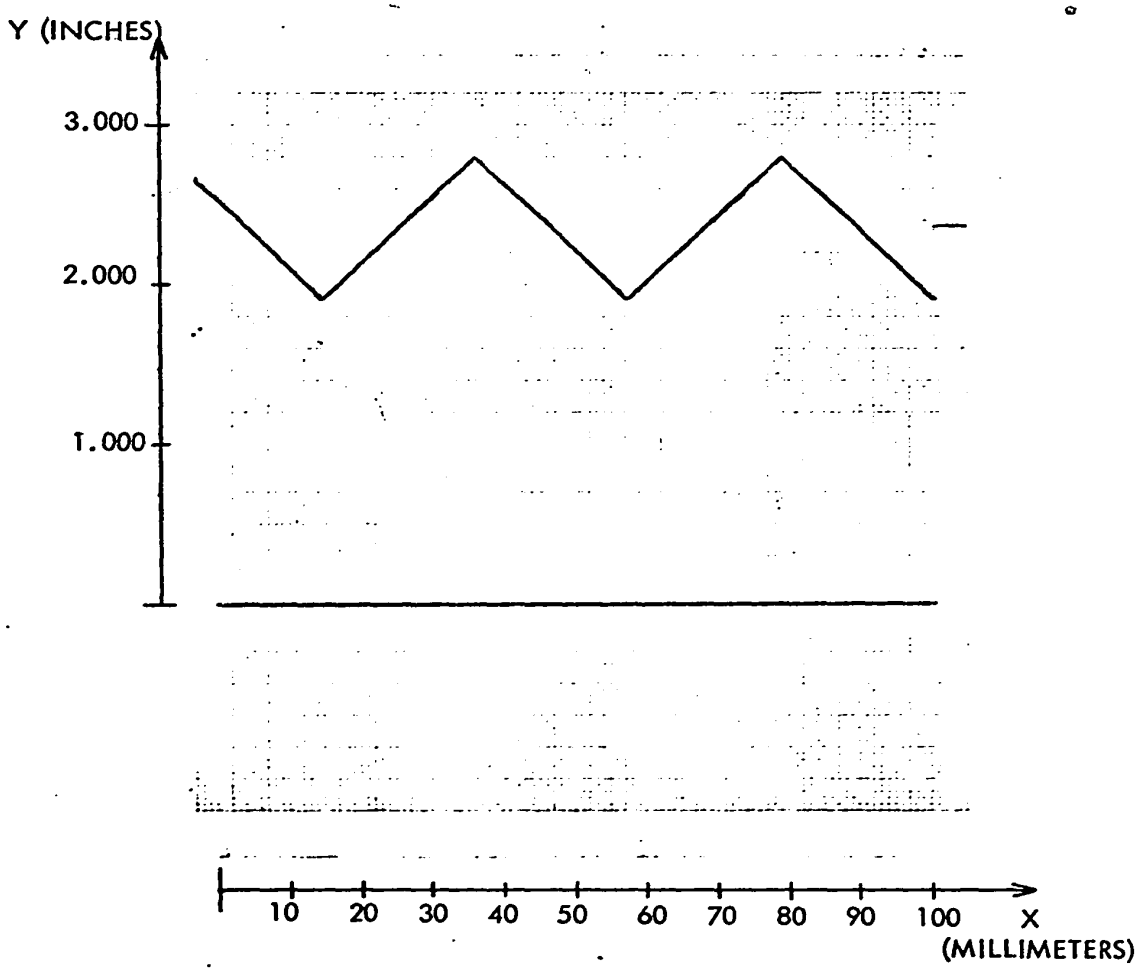


FIGURE 5.2.8. GRAPH SAMPLE CONTAINING SAWTOOTH WAVEFORM.

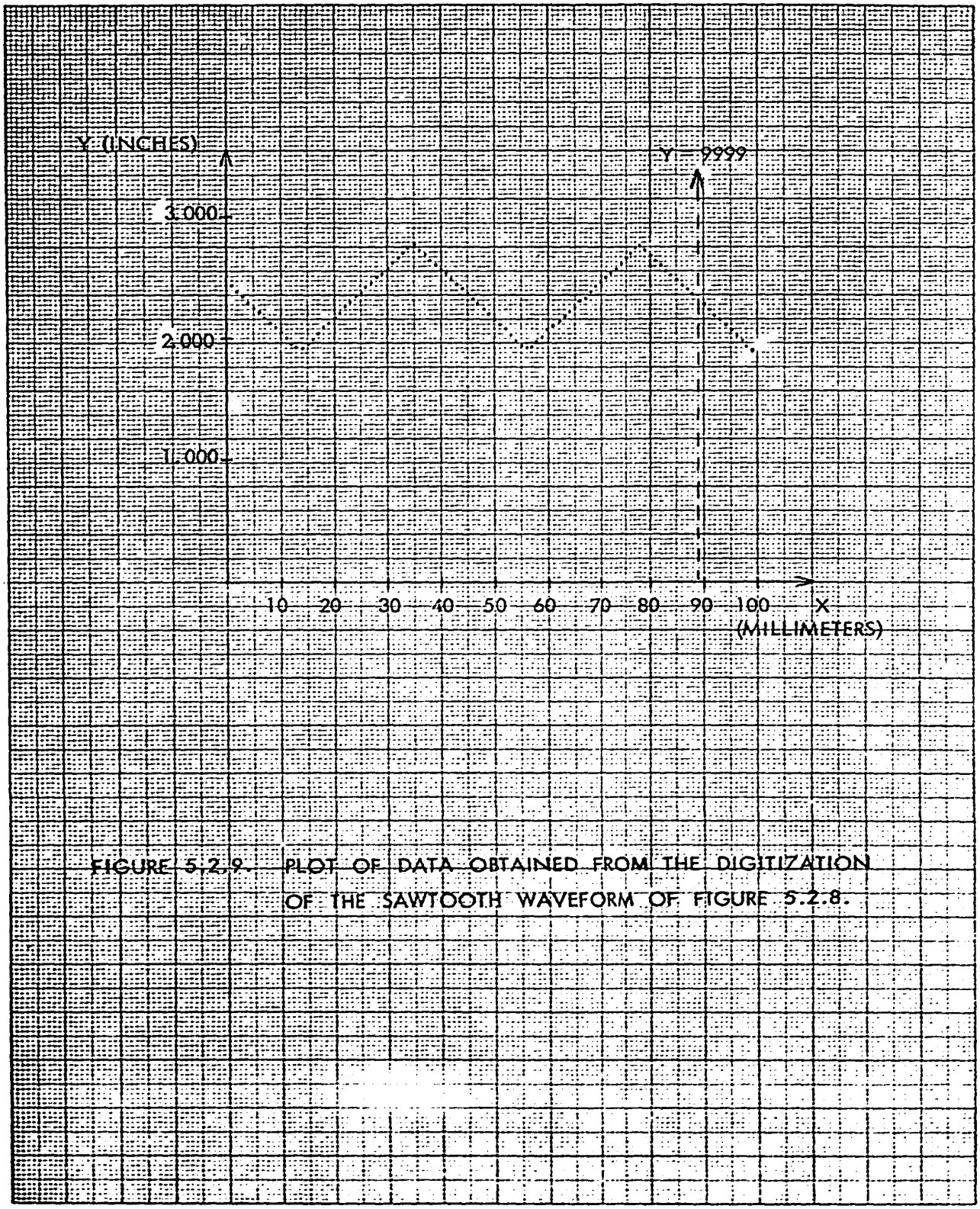


FIGURE 5.2.9. PLOT OF DATA OBTAINED FROM THE DIGITIZATION OF THE SAWTOOTH WAVEFORM OF FIGURE 5.2.8.

5.4 Comments on the Overall System

There are a few ways by which the graph reader could be improved.

(i) The resolution may be improved by doubling the frequency of the marker pulses. This cannot be done "mechanically", by increasing the number of markers on the marker disc. However, it can be accomplished electronically, by means of the circuit depicted in Figure 5.3.1.

In Figure 5.3.2 (a) are shown the marker pulses as they are derived from the marker disc. The pulse width is about 60 μ sec. Presently, marker pulses are fed to NEGATIVE-EDGE-TRIGGERED ONE-SHOT B 4 in Control B. (Figure 3.4.5 (b), Section I D). The output of the ONE-SHOT, shown in Figure 5.3.2 (b), serves through appropriate gating, as the input to the Y counter. Note that these markers are derived from the negative-going edge of waveform (a). To double the frequency, two additional ONE-SHOTS are required, along with an OR gate and an inverter / level translator. Marker pulses derived from the disc are fed into the inverter / level translator, whose output is shown as waveform (c). The output of the inverter / level translator is used to trigger the NEGATIVE-EDGE-TRIGGERED ONE-SHOT No. 1 in Figure 5.3.1. The "on - time" of the ONE-SHOT, T_{ON}, is varied by means of a potentiometer (P1),

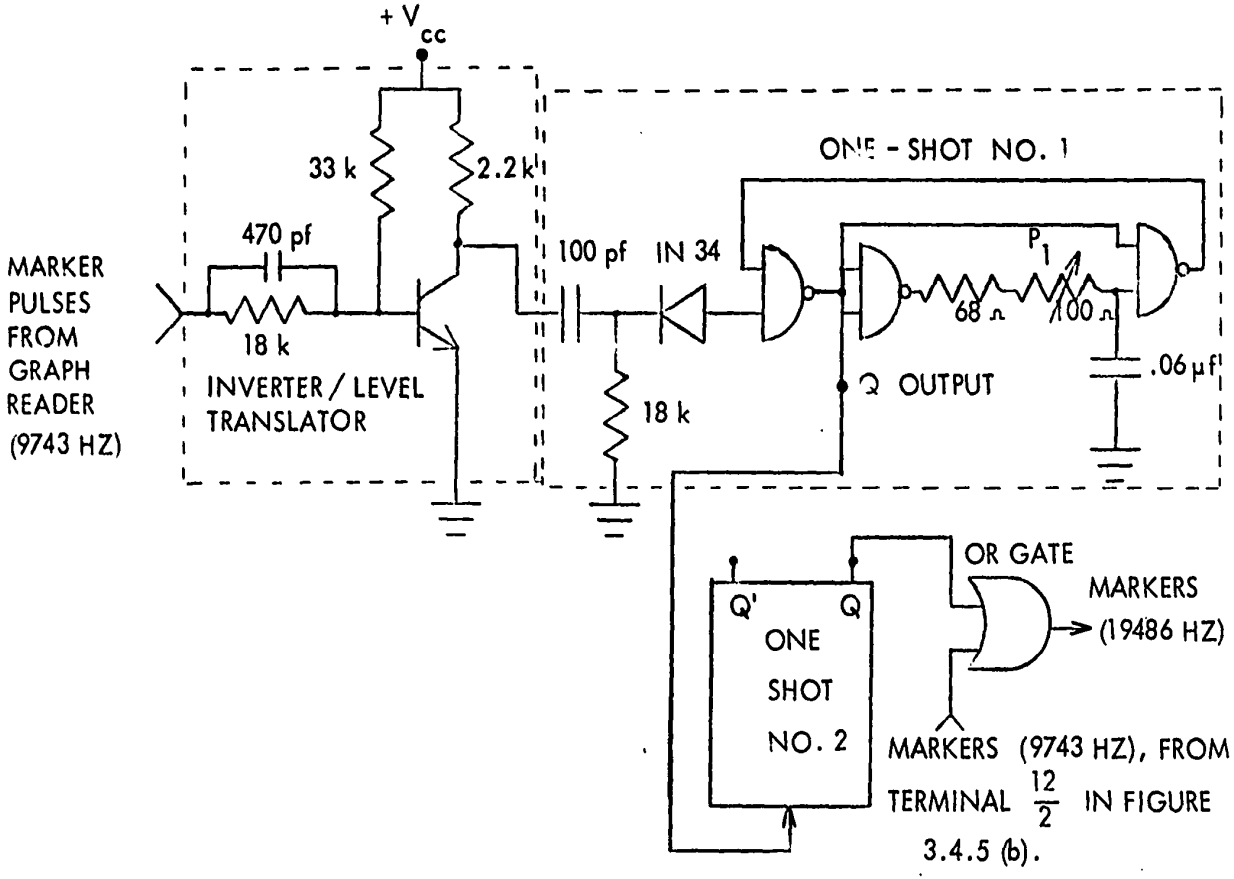


FIGURE 5.3.1. MARKER PULSE FREQUENCY DOUBLER CIRCUIT.

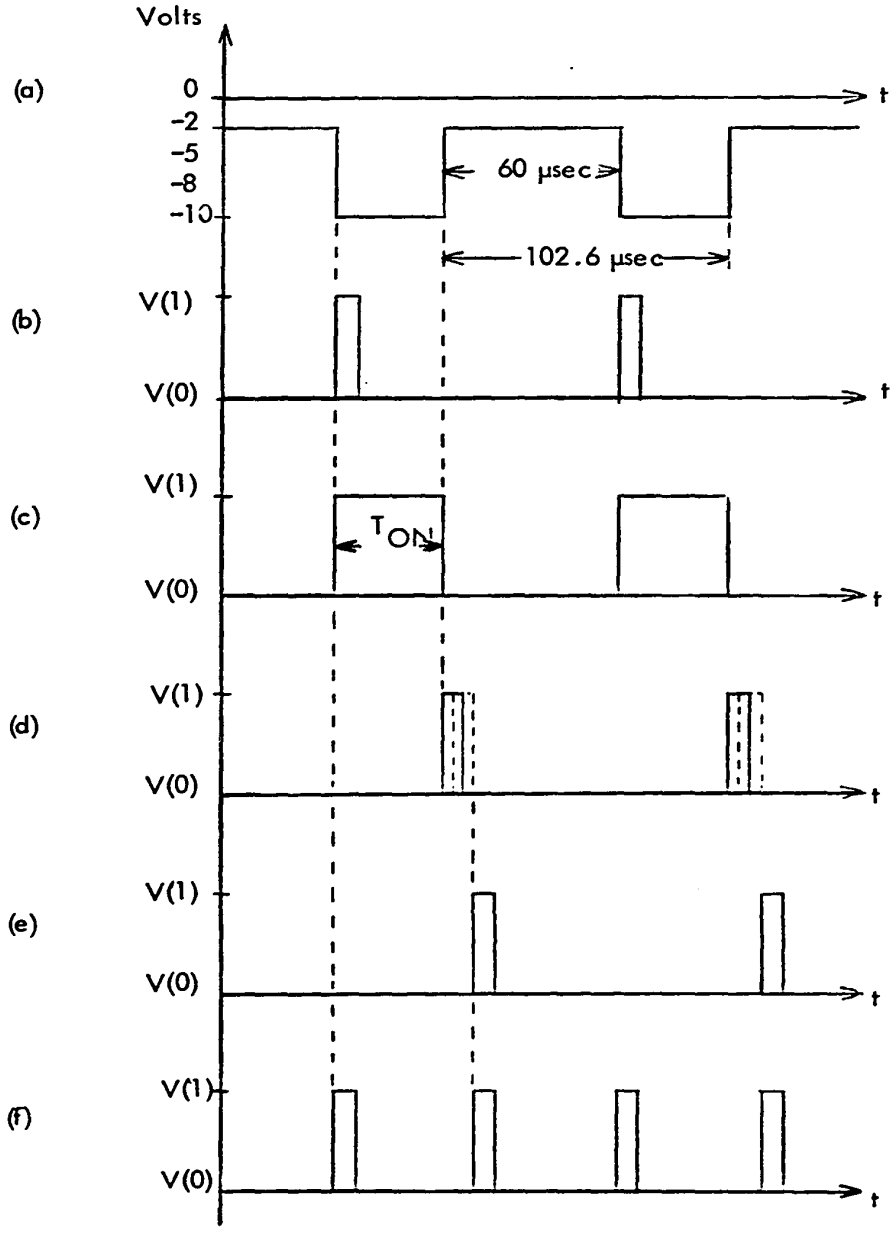


FIGURE 5.3.2. PULSE TIMING DIAGRAM OF MARKER PULSE FREQUENCY DOUBLER CIRCUIT.

so that the negative-going edge of its output may be set at a point mid-way between the marker pulses of waveform (b). The output of ONE-SHOT No.1 is fed to NEGATIVE-EDGE-TRIGGERED ONE-SHOT No. 2. The output of ONE-SHOT No. 2 and waveform (b) are fed to an OR gate. The output of the OR gate is shown as waveform (f) in Figure 5.3.2. The frequency of waveform (f) is twice that of waveform (b).

To adapt marker pulses occurring at twice their original frequency of 9743 HZ to the logic within Control B requires a few minor modifications. As outlined in Section 3.4.3, the present arrangement used in determining the ordinate (Y) value of a graph consists of counting each marker pulse which occurs between video pulses. When video pulses occur the marker frequency is halved, so that every second marker pulse increases the contents of the Y counter by one. The proposed arrangement, that is, with the marker pulses occurring at twice the original frequency would require that the frequency of the output of GATE B 4 (Figure 3.4.5 (b)) be halved before being fed to the Y counter in order that the counter may contain Y directly in inches. To account for the least significant value of Y additional gating is required. Recall that at present the least significant value of Y, in the Y register, is set to 5 if the sum of the number of marker pulses occurring coincidentally with video pulses is odd, and to 0 if the number of pulses so occurring is even.

The proposed modifications are shown in Figure 5.3.3.

For the present purposes flip-flop B1 and OR GATE B4 of Control B (Figure 3.4.5 (b)) are also included in this figure. Recall that the output of gate B 4 is presently fed to the Y counter. The true output Q of flip-flop B 1 is high if an odd number of marker pulses has occurred coincidently with video pulses during one scan, and low otherwise. In the new arrangement, marker pulses at double the frequency would be fed to the same inputs which presently accept marker pulses occurring at 9743 HZ, as shown in Figure 3.4.5 (b) of Control B. However, the output of gate B 4 would then serve as the clock input to flip-flop D 1. The waveforms of Figure 5.3.4 illustrate the process. Waveform (a) shows marker pulses occurring at 19,486 HZ. The video pulses are shown in waveform (b), whereas waveforms (c) and (d) represent the outputs of flip-flop B 1 and gate B 4 respectively. The output of ONE-SHOT D 1, which would be fed into the Y counter is waveform (f). For the situation depicted in Figure 5.3.4, 12 pulses are fed to the Y counter. However, the number of markers occurring between video pulses is 2. In addition, 7 marker pulses occur coincidentally with video pulses. Since each marker pulse, at a frequency of 19,486 HZ represents 0.005 inches along a graph the distance between the mid-points of the two video pulses should in this case be 0.1275 inches, or 0.128" when rounded off to the nearest

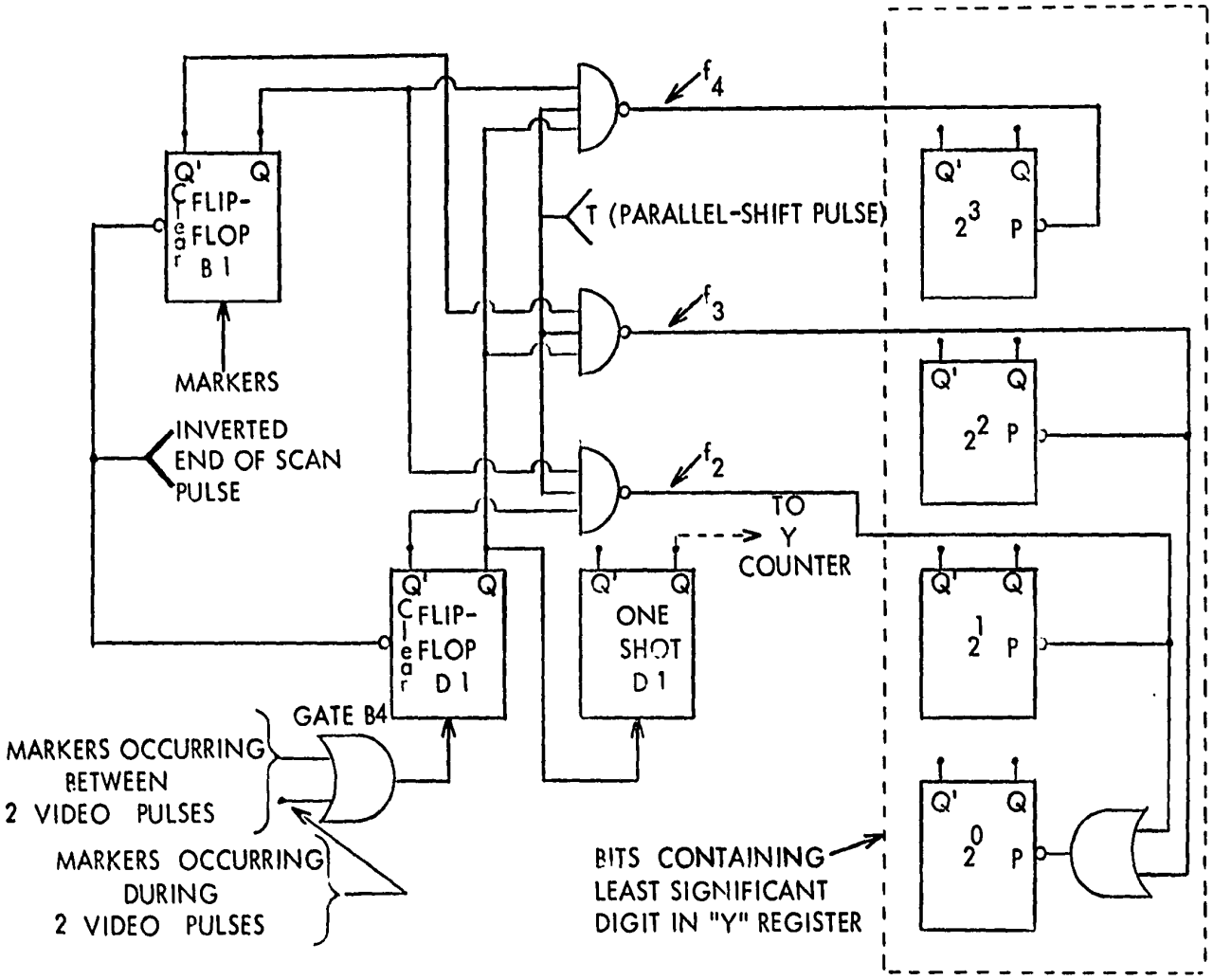


FIGURE 5.3.3. ADDITIONAL LOGIC REQUIRED IN CONTROL B TO INCORPORATE MARKER PULSE FREQUENCY DOUBLER CIRCUIT.

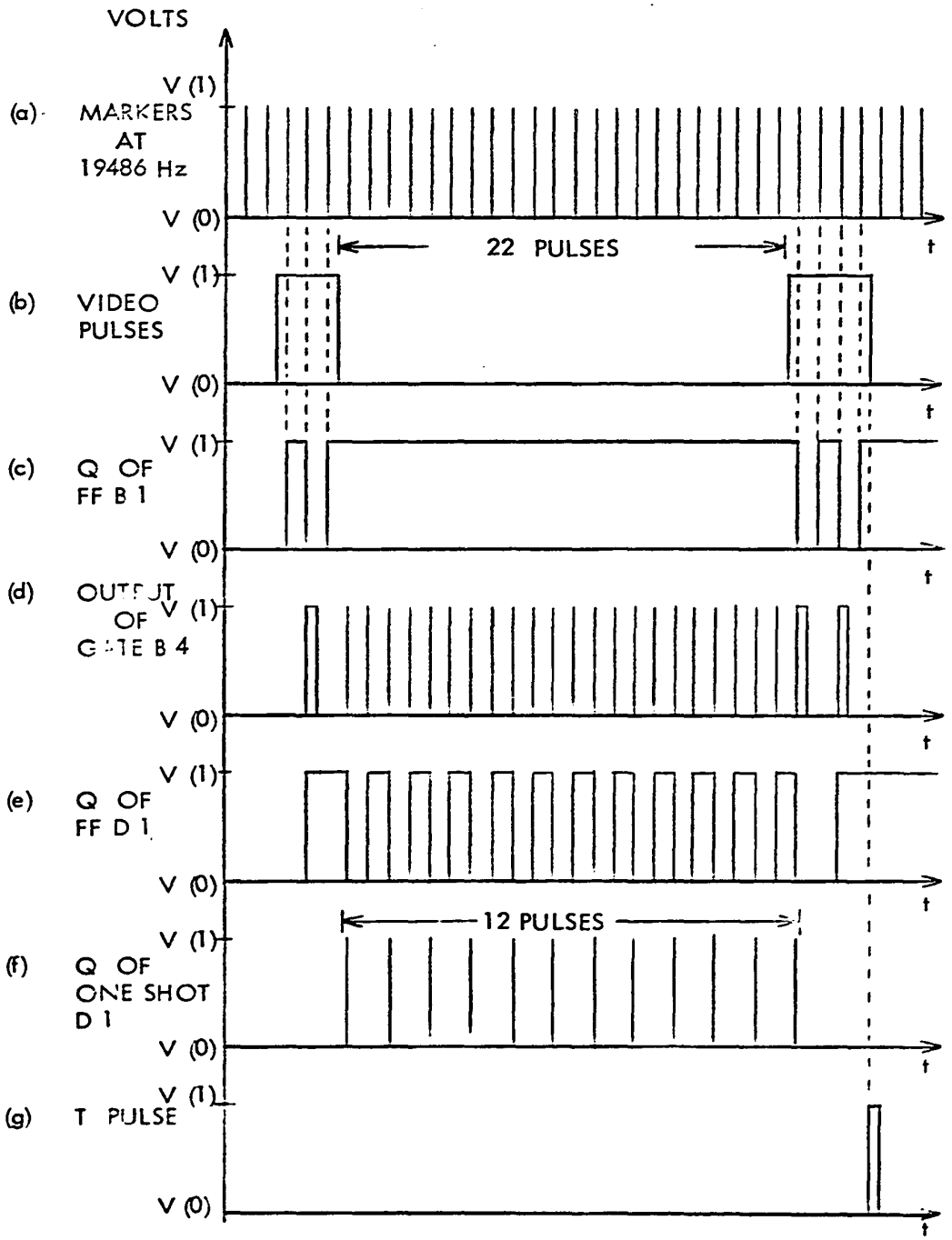


FIGURE 5.3.4. DETERMINATION OF THE ORDINATE (Y) VALUE OF A GRAPH IF MARKER PULSE FREQUENCY IS DOUBLED.

thousandth of an inch. However, as mentioned, the contents of the Y counter at the end of the second video pulse is 0.120 inches. To obtain the least significant figure, which is in this case the thousandths digit, the true outputs of flip-flops B 1 and D 1 are monitored. If, at the end of the second video pulse, the true output of flip-flop B 1 is high, then the number of marker pulses occurring coincidentally with video pulses was odd. If Q of flip-flop D 1 is high at the end of the second video pulse, then the total number of pulses fed into the flip-flop was odd. The thousandths, or least significant digit of the Y register is then set according to the truth table of Figure 5.3.5.

The truth table is interpreted as follows :

(a) If the true outputs of flip-flop D 1 and flip-flop B 1 are low at the end of the second video pulse then the thousandths digit of the Y value is set to 0. Therefore $f_1 = Q'_{FFD1}\, Q'_{FFB1}$. The gating necessary to implement f_1 is not included in Figure 5.3.3 because, as mentioned in Section 3.4.5, the entire X - Y register is always in a CLEARED (reset) state at the beginning of each scan. Therefore, to provide additional reset inputs to the thousandths bits within the register in this case would be redundant.

(b) If Q of flip-flop D 1 is low and Q of flip-flop B 1 is high, then the thousandths digit is set to 3. The digit 3 is simply 0.0025 rounded off to the nearest thousandth. Therefore $f_2 = Q'_{FFD1} \; Q_{FFB1}$.

(c) If Q of flip-flop D 1 is high and Q of flip-flop B 1 is low then the thousandths digit is set to 5. Therefore $f_3 = Q_{FFD1} \; Q'_{FFB1}$.

(d) If both true outputs are high, then the thousandths digit is set to 8. This represents 0.0075 rounded off to the nearest thousandth, and is applicable to the example shown in Figure 5.3.4, where the actual value of Y is 0.1275 inches. The number contained within the Y register in this case would be 0.128 inches. Therefore $f_4 = Q_{FFD1} \; Q_{FFB1}$.

The additional gating required to set the thousandths bits within the Y register is included in Figure 5.3.3. The gating pulse T, drawn as waveform (g) in Figure 5.3.4 is the pulse derived from the negative-going edge of the second video pulse, as mentioned in the discussion on Con-

$Q_{FF\ D\ 1}$	$Q_{FF\ B\ 1}$	f_1	f_2	f_3	f_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

FIGURE 5.3.5. TRUTH TABLE DEFINING PRESET INPUTS TO FLIP-FLOPS REPRESENTING THOUSANDTHS DIGIT IN FIGURE 5.3.3.

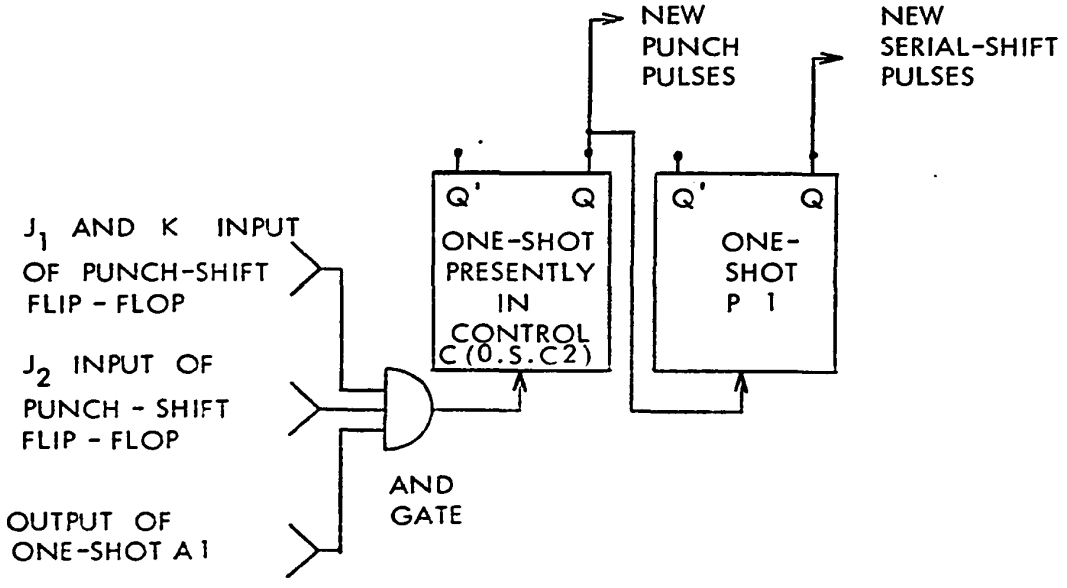


FIGURE 5.3.6. ADDITIONAL CIRCUITRY REQUIRED IN CONTROL C TO DOUBLE THE CARD - PUNCH SPEED.

trol B. Note that two additional flip-flops are required (2^1 and 2^3) in the thousandths position of the Y register in order to store the digits 0, 3, 5 and 8 in B C D form. Only two flip-flops are required if the marker frequency is not doubled because in that case the least significant (thousandths) digit of Y is either 0 or 5.

(ii) The digitization speed can be increased by doubling the rate at which a card is punched. This is possible only with an I B M Type 29 Keypunch machine, which has a punch cycle time of 56 milliseconds, as compared to 100 milliseconds for the I B M Type 26. Presently, data cards are punched at the rate of 1 column per 152 milliseconds - that is, one column for every two revolutions of the graph reader drum. Recall that punching is regulated by the logic within Control C (Figure 3.4.21 (b)). One column of a data card is punched for every occurrence of a PUNCH pulse. The PUNCH pulse is generated by means of NEGATIVE-EDGE-TRIGGERED ONE-SHOT C2. The ONE-SHOT is triggered by the Q' (false) output of the PUNCH-SHIFT flip-flop, and the PUNCH-SHIFT FF by the output of ONE-SHOT A1 (Figure 3.4.1 (b), Section 2D). ONE-SHOT A1 is itself triggered by the END OF SCAN pulse, which occurs once for every revolution of the graph reader drum. The PUNCH-

SHIFT FF halves the frequency of the output of ONE-SHOT A 1 and therefore the PUNCH pulse occurs once every 152 milliseconds. To double the punch rate requires that a punch pulse be generated once for every revolution of the drum, i.e., every 76 milliseconds. This can be done by replacing the PUNCH - SHIFT flip-flop of Control B by a 3 - input AND gate, shown in Figure 5.3.6. Two inputs to the proposed AND gate would consist of the J_1 , K and J_2 inputs which are presently applied to the PUNCH - SHIFT flip-flop and the third input would be the output of ONE-SHOT A 1. To generate the "new" punch pulses the output of the AND gate would be fed to NEGATIVE-EDGE-TRIGGERED ONE-SHOT C 2 in Control C which presently generates the punch pulses. SERIAL-SHIFT pulses can be derived by means of an additional NEGATIVE-EDGE-TRIGGERED ONE-SHOT, P 1 , in Figure 5.3.6 , having as its input the PUNCH pulse. In this way a SERIAL - SHIFT pulse would be generated on the negative-going edge of every PUNCH pulse. In Figure 5.3.7 waveforms (a) through (d) show the present PUNCH - SHIFT arrangement, while the proposed changes yield those shown in Figure 5.3.8, waveforms (a) through (d) .

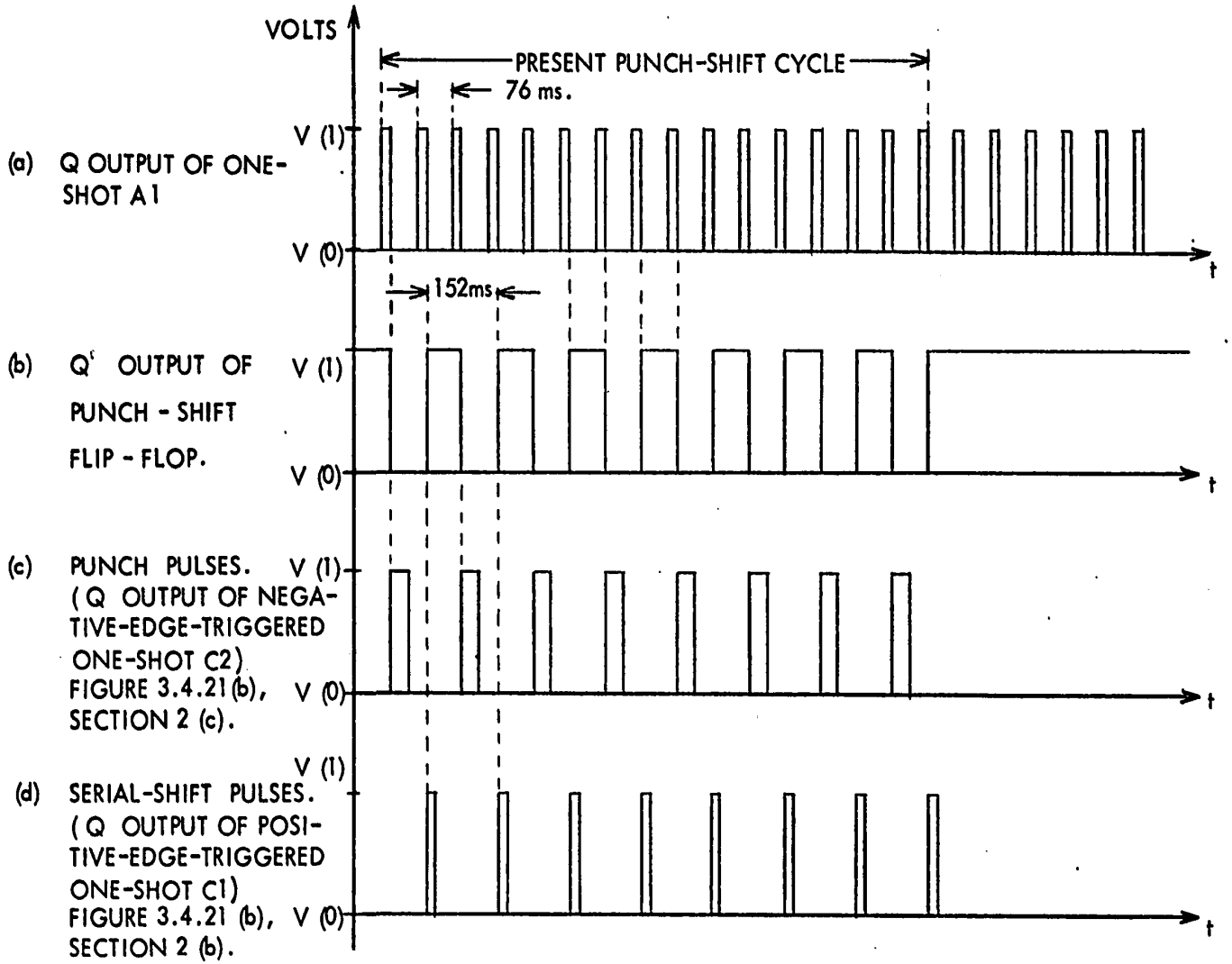


FIGURE 5.3.7. PULSE TIMING DIAGRAM OF THE PRESENT PUNCH - SHIFT ARRANGEMENT.

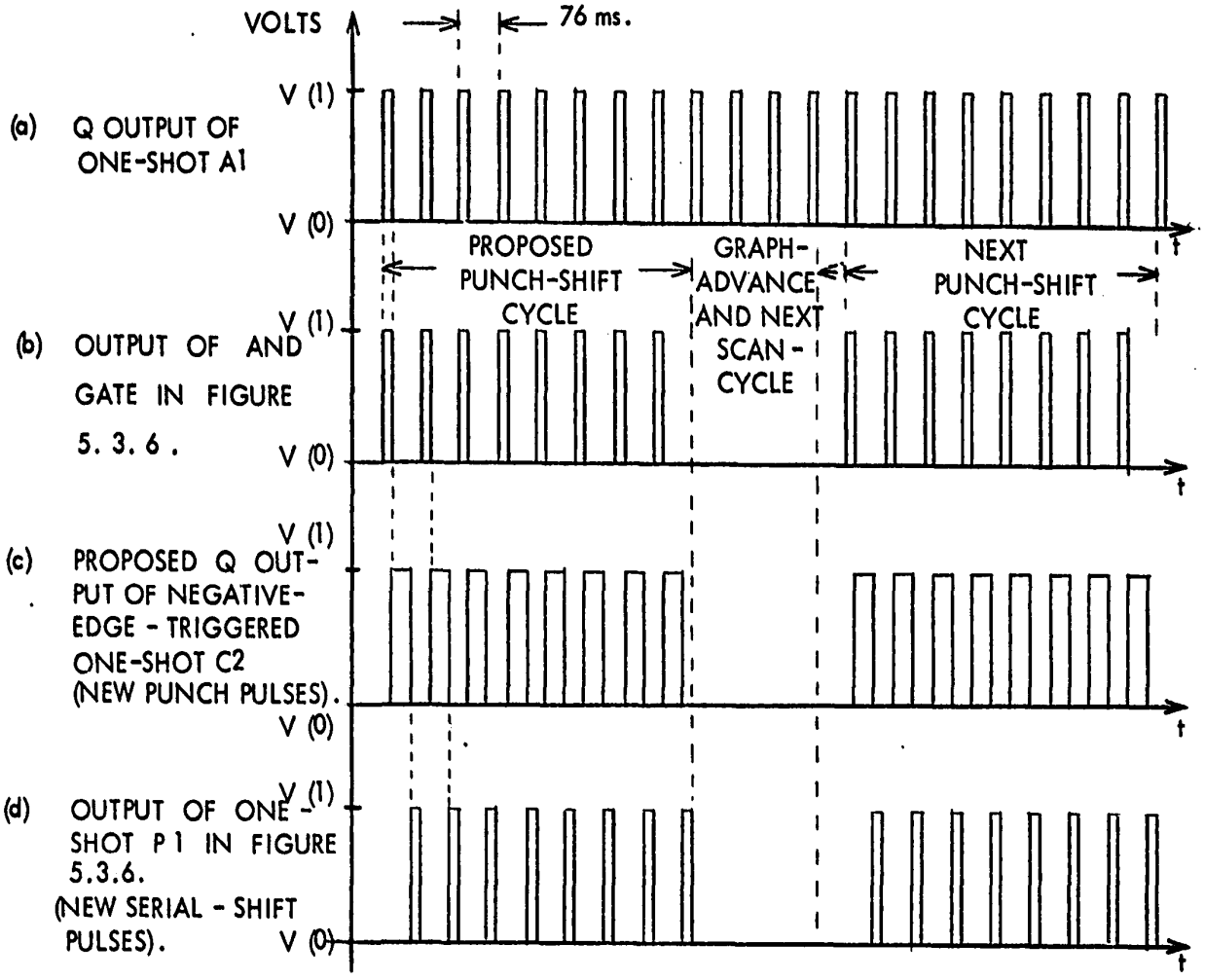


FIGURE 5.3.8. PUNCH-SHIFT CYCLE PULSE TIMING DIAGRAM IF PUNCHING SPEED IS DOUBLED.

(iii) At present the input to the graph reader is constrained to graphs containing two lines only. There are several ways of expanding the present logic so that graphs containing many lines can be read. One way of doing this would require that the present X - Y register be expanded.

Recall that in the X - Y register are stored the abscissa and ordinate values of a scan. The ordinate represents the distance between two lines on a graph, where one line is assumed to be a reference line. The proposed scheme would require an extra Y register for each additional line on a graph. In this way a graph containing n lines would require (n - 1) Y registers. The first register in the chain would contain the distance between the reference line and the first graph line ; the second register would contain the distance between the reference line and the second graph line, and so on. Each successive Y value would be obtained from the Y counter presently in use. The counter would simply keep counting throughout one entire scan. At the end of the second video pulse (representing the second graph line) the counter contents would be shifted into the first Y register ; at the end of the third video pulse the counter contents would be shifted into the second Y register, etc. The total number of video pulses, n, occurring in one scan would also be counted. At the end of a scan 4 n PUNCH pulses and 4 n

SERIAL -SHIFT pulses would be generated in order to transfer the contents of all the registers onto data cards.

In the case of multiple lines the data card format would have to be changed. A simple way of solving this problem is to let each data card contain graphical information pertaining to one scan only. In this way one 80 column data card could contain as many as 19 ordinate values, (corresponding to a graph which contains 20 lines) along with the corresponding abscissa value.

The main disadvantage of the above scheme is that it requires a large memory unit. Recall that the Y register consists of 14 flip-flops. For each additional graph line then, 14 flip-flops are required. A graph containing 20 lines would require 282 flip-flops altogether. (266 flip-flops for the ordinate values and 16 for the abscissa).

Another approach to the multiple line problem is now proposed. Its main advantage is that unlike the one discussed above, it does not require additional registers. By incorporating the circuit shown in Figure 5.3.9 to the present logic circuitry, graphs containing up to 5 lines may be read. The timing diagram of Figure 5.3.10 illustrates the operation of the circuit. The circuit was designed by

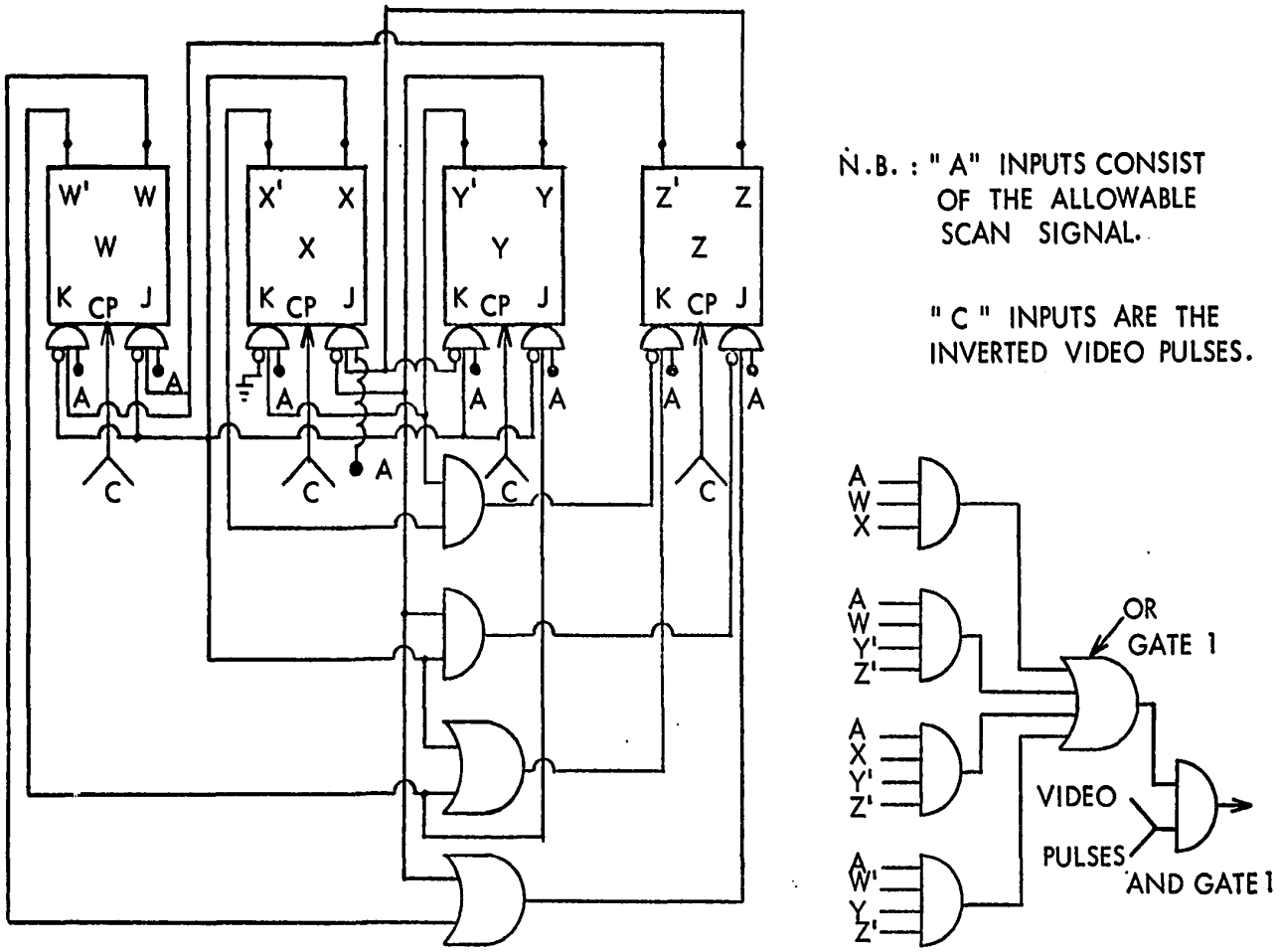


FIGURE 5.3.9. ADDITIONAL LOGIC REQUIRED IN CONTROL B TO DIGITIZE GRAPHS CONTAINING MORE THAN 2 LINES.

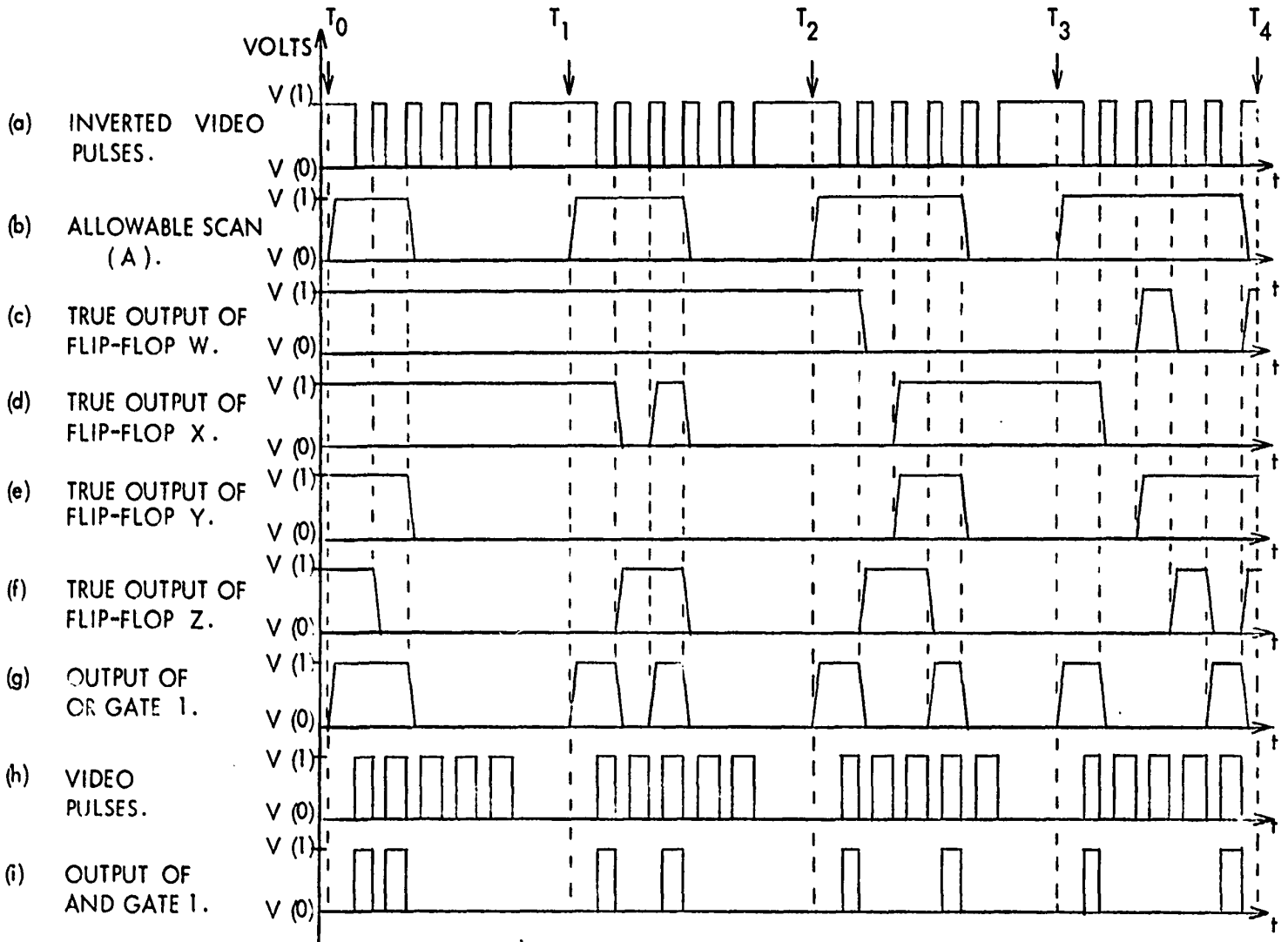


FIGURE 5.3.10. PULSE TIMING DIAGRAM OF THE CIRCUIT OF FIGURE 5.3.9.

applying the extension of Mealy's theory [14]. Waveform (a) in the timing diagram consists of inverted video pulses and waveform (b) is the allowable scan signal defined in Section 3.4.3. The true outputs of flip-flops W, X, Y and Z in Figure 5.3.9 are shown as waveforms (c) through (f) in the timing diagram. The clock pulse input to each flip-flop is waveform (a). The J and K inputs to the flip-flops are listed in Table 5.3.1. In the table, variable A represents the allowable scan signal whereas W, X, Y and Z are, as mentioned above, the true outputs of the flip-flops.

The output of OR GATE 1 in the circuit is shown on the timing diagram as waveform (g). This waveform, together with the video pulse waveform (h) are inputs to AND GATE 1 in Figure 5.3.9. The output of AND GATE 1 is waveform (i). A comparison of waveforms (h) and (i) for $T_o < t < T_4$ shows that for $T_o < t < T_1$, waveform (i) consists of the first two video pulses in waveform (h). For $T_1 < t < T_2$ waveform (i) consists of the first and third video pulses. Similarly, waveform (i) consists of the first and fourth video pulses during $T_2 < t < T_3$, and the first and fifth video pulses during $T_3 < t < T_4$. The first video pulse, as mentioned earlier, represents a reference line on a graph. When the circuit of Figure 5.3.9 is incorporated into the existing logic the system would function in the following manner.

TABLE 5.3.1.

J AND K INPUTS OF FLIP-FLOPS W, X, Y AND Z IN FIGURE 5.3.9.

J_W	=	A X 'Z'	K_W	=	A X' Z'
J_X	=	A Z Y'	K_X	=	A Y'
J_Y	=	A W 'X'	K_Y	=	A X Z'
J_Z	=	A [WY' + X'Y]	K_Z	=	A [X + W' Y]

OUTPUT OF AND GATE 1 = [W X + W Y 'Z' + X Y 'Z' + W' Y Z'] A C'

First the graph paper is advanced by a preset increment. A scan of the graph would then take place. This scan corresponds to $T_o < t < T_1$ in the timing diagram. The distance between the first two graph lines, represented by the two video pulses in waveform (i) would be determined and stored in the Y register. At the end of this first scan 8 PUNCH pulses and 8 SERIAL-SHIFT pulses would transfer the X and Y values onto a data card. At the end of this first punch cycle another scan would take place. During this second scan ($T_1 < t < T_2$) the distance between the first and third graph lines is obtained and stored in the X register. At the end of this scan 4 PUNCH pulses and 4 SERIAL-SHIFT pulses transfer the Y value onto the data card. This procedure would then continue until the distance between the first and fifth graph lines is determined and transferred onto the card. Once this is done, the graph paper would then be advanced by the preset increment and from then on the cycle described above would resume.

(iv) The reliability of the marker pulse generator can be improved by re-designing the enclosure within which is contained the light source. Recall that the generator consists of a lamp, a disc, and a phototransistor. Because the lamp is virtually unventilated within its present enclosure, its actual lifetime is considerably less than that specified by the manufacturer.

(v) The paper-drive mechanism which advances a graph sample by a preset amount prior to every scan consists of two adjacent steel rollers, one of which is geared to the stepping motor. Because the surface of the rollers was originally highly polished a considerable amount of slippage occurred as the graph paper passed through the rollers. The paper was therefore not advancing exactly by the amount preset by the ΔX (X - increment) selector switch. To overcome this problem the polished surface on the rollers was removed with emery paper. It is not inconceivable, however, that through extended use the roller surface will deteriorate to the extent where slippage will recur. It is therefore recommended that the steel rollers be replaced by rubber types, in an arrangement somewhat similar to that found in a . Sanborn Model 320 Recorder.

5.5 Summary

The primary aim of this research was to develop an interface between a graphical-to-digital converter and an I B M keypunch machine. This was accomplished through the design and construction of a digital control system. By employing integrated devices almost exclusively within the logic circuitry it was possible to include therein a high degree of reliability at a relatively low cost.

The optics of the scanning system were investigated. Modifications yielded an improvement in the accuracy of digitization to the extent where the maximum probable error is now 0.246 % .

Additional optical modifications were made, thereby moderately increasing the signal-to-noise ratio of the detection scheme which senses graph lines. Subsequent tests revealed that owing to the sensitivity of the detection method no further improvement in the SNR was possible. It was then concluded that in order to realize a reasonable SNR graphical data must be contained on paper possessing high reflectivity, uniform texture and must be devoid of dirt or other alien markings.

In practice it is not always possible to satisfy these somewhat stringent requirements. Therefore an error detection scheme was incorporated within the interface circuitry. As a result, whenever the scanning system fails to detect a graph line or detects "too many" lines, appropriate error codes are punched onto data cards. This enables erroneous digitizations to be either visibly located and rejected or through a simple subroutine if the data is destined for further analysis by a computer.

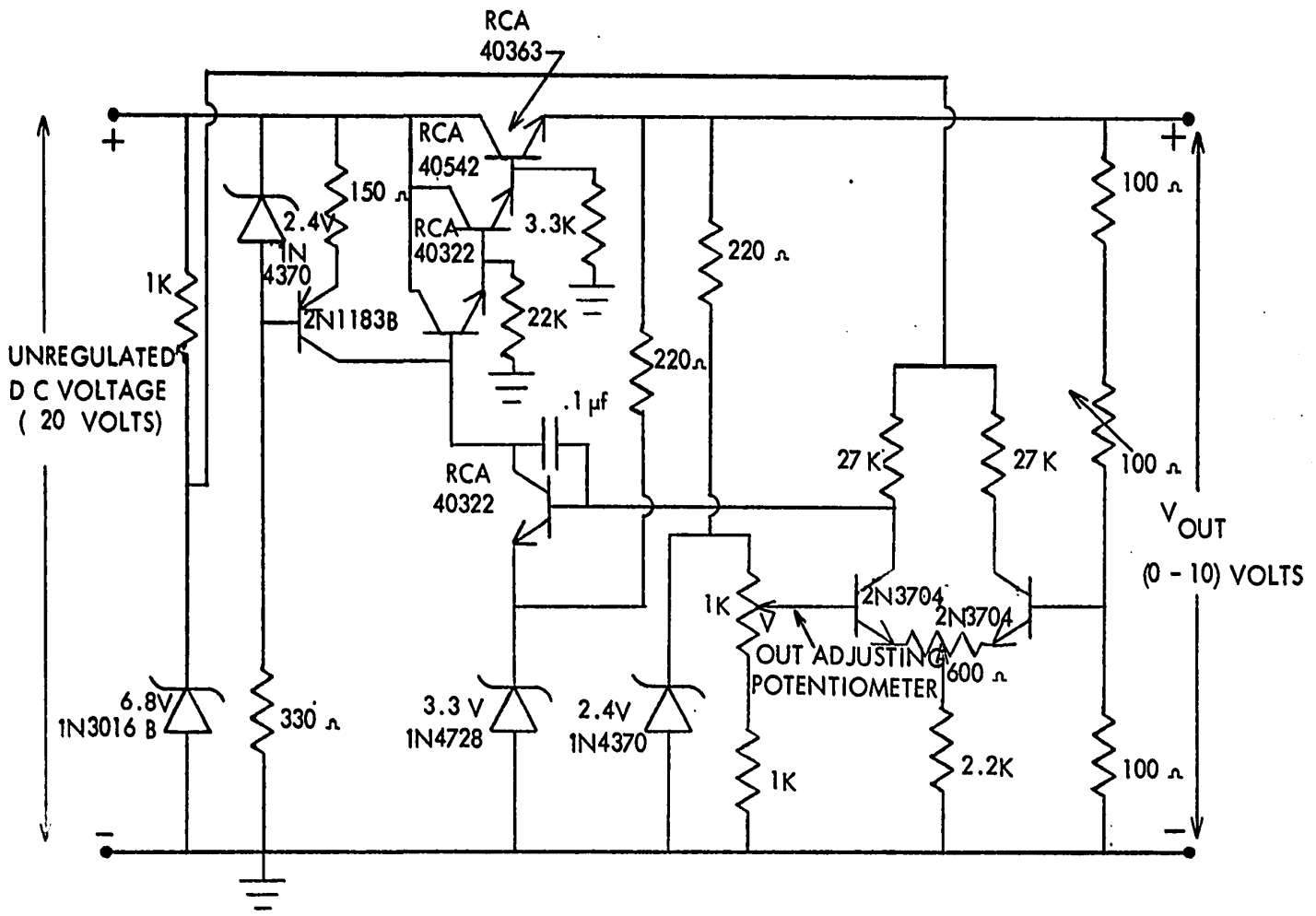


FIGURE A. 1. 1. LOGIC CIRCUITS POWER SUPPLY.

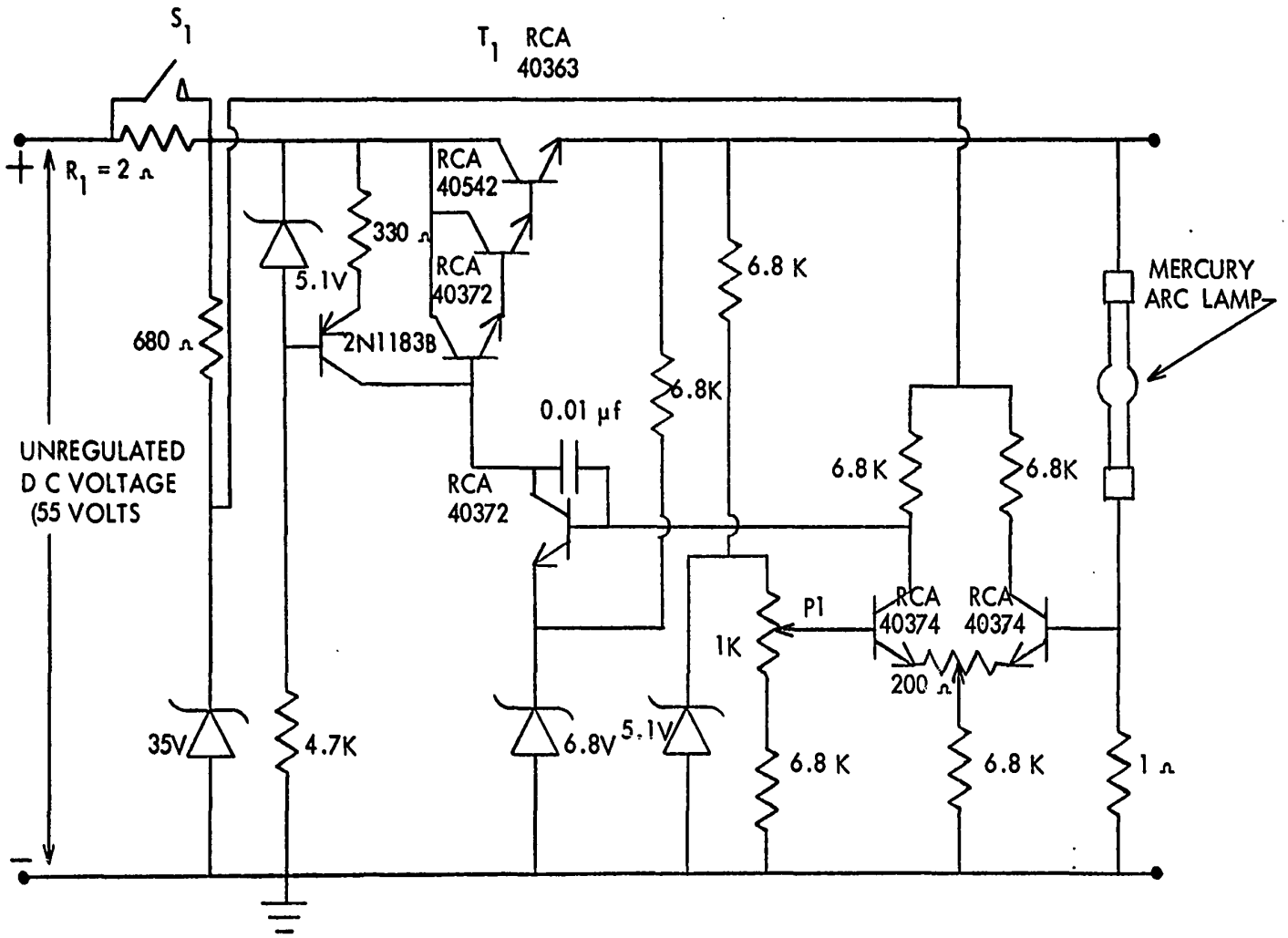


FIGURE A.1.2. MERCURY ARC LAMP POWER SUPPLY.

BIBLIOGRAPHY

[1] Auto-trol Corporation Staff, "Model 3400 High Speed Continuous Line Digitizer", Auto-trol Corporation Specification Data, Arvada, Colorado.

[2] Calma Company Staff, "Model 303 Digitizer", Calma Bulletin 303B, Santa Clara, California, October 1967.

[3] D - Mac Limited Staff, "D-Mac Pencil Follower Type PF. 10,000 Mark 1A", D-Mac Specification Data, Hillington, Glasgow.

[4] Rosza, C. and d'Ombrain, G.L., "Automatic Conversion of Diagram Data into Digital Form", Post-doctoral Research Dissertation, McGill University, Montreal, Quebec, May 1965.

[5] Cox, L. A. and d'Ombrain, G.L., "An Automatic Graph Reader", M.Eng. Dissertation, McGill University, Montreal, Quebec, October 1965.

[6] I B M Staff, "I B M Field Engineering Manual of Instruction - Type 26 Printing Card Punch", I B M No. 223 - 8318 - 9, January 1964.

[7] I B M Staff, "I B M Field Engineering Maintenance Manual - Type 29 Card Punch", I B M No. S 23 - 4035, January 1967.

[8] Huffman, D.A., "The Synthesis of Sequential Switching Circuits", Journal of the Franklin Institute, 257, pp. 161 - 190, 275 - 303, March and April 1954.

[9] Mealy, G.H., "A Method for Synthesizing Sequential Circuits", The Bell System Technical Journal, pp. 1045 - 1079, September 1955.

[10] Hartmanis, J. "On the State Assignment Problem for Sequential Machines, I", IRE Transactions on Electronic Computers, Vol. EC-10, pp. 157-165, June 1961.

[11] Stearns, R.E. and Hartmanis, J., "On the State Assignment Problem for Sequential Machines, II", IRE Transactions on Electronic Computers, Vol. EC-10, pp. 593-603, December 1961.

[12] Dolotta, T.A. and McCluskey, E.J., "The Coding of Internal States of Sequential Circuits", IEEE Transactions on Electronic Computers, Vol. EC-13, pp. 549-563, October 1964.

[13] Weiner, P. and Smith, E.J., "Optimization of Reduced Dependencies for Synchronous Sequential Machines", IEEE Transactions on Electronic Computers, Vol. EC-16, pp. 835-847, December 1967.

[14] Humphrey, W.S., Jr., "Switching Circuits", New York : McGraw-Hill, 1958, Chapter 10.

[15] Curtis, H.A., "Systematic Procedures for Realizing Synchronous Sequential Machines using Flip-Flop Memory : Part I", IEEE Transactions on Computers, Vol. C-18, pp. 1121-1127, December 1969.

[16] Todd, C.D., "An Annotated Bibliography on NOR and NAND Logic", IEEE Transactions on Electronic Computers, Vol. EC-12, pp. 462-464, October 1963.

[17] Earle, J., "Synthesizing Minimal Stroke and Dagger Functions", IRE Convention 1960, Part II, PGCT - Special Supplement, CT-7, August 1960.

[18] Earle, J., "Implementing NOR Logic", I B M TR 00.08000.697.

[19] Maley, G.A. and Earle, J., "The Logic Design of Transistor Digital Computers", New Jersey : Prentice-Hall, 1963, Chapters 5 and 6.

[20] Davidson, E.S., "An Algorithm for NAND Decomposition under Network Constraints", IEEE Transactions on Computers, Vol. EC-18, pp.1098-1109, December 1969.

[21] Schneider, P.R. and Dietmeyer, D.L., "An Algorithm for Synthesis of Multiple-Output Combinational Logic", IEEE Transactions on Computers, Vol. C-17, pp. 117-128, February 1968.

[22] Hellerman, L., "A Catalog of Three-Variable Or-Invert and And-Invert Logical Circuits", IEEE Transactions on Electronic Computers, Vol. EC-12, pp. 198-223, June 1963.

[23] Motorola Electronics Staff, "Motorola Digital Integrated Circuits", Motorola Technical Data No. 3506-2, September 1968.

[24] Signetics Corporation Staff, "Application Memos", pp. 2-1.27 - 2-1.43, September 1969.

[25] Texas Instruments Inc. Staff, "TTL Integrated Circuits Catalog from Texas Instruments", Texas Instruments Catalog CC201, pp. xii, August 1969.

[26] Texas Instruments Inc. Staff, "Series 74 High-Speed Saturated Digital Circuits for General-Purpose Industrial Applications", Texas Instruments Bulletin No. DL-S 657934, August 1965.

[27] The Engineering Staff of Texas Instruments Incorporated, "Transistor Circuit Design", New York : McGraw-Hill, 1963, Chapter 9 .

[28] Middlebrook, R.D., "Design of Transistor Regulated Power Supplies", Proc. IRE, Vol. 45, pp. 1502-1509, November 1957.

[29] Motorola Electronics Staff, "Integrated Circuits Products and Applications", Applications Manual, August 1967.

[30] Sandland, P., "Integrated Gates Form Fast Monostable Multivibrator", Electronics, pp. 108-109, June 26, 1967.

[31] Flint, Jr., O. Q., "Free-Running Multivibrator is Made with a NAND Gate", Electronics, pp. 95-96, January 6, 1969.