AN INEXPENSIVE SYSTEM OF GEOPHYSICAL DATA ACQUISITION

by

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ABSTRACT

In a preliminary development of an inexpensive system of geophysical data acquisition, 32K of Random Access Memory was added to a Commodore VIC-20 computer to store the sampled data. The present system comprises two independent units: 1) an eight-bit , 16-channel analog-to-digital converter interface. 2) a telemetry interface that uses frequency modulation over one channel. Laboratory and field tests confirmed the usefulness of the analog-to-digital converter in a large number of applications such as waveform digitization and event monitoring. Excellent transmission and reception of data was accomplished via cable links, over a distance of about 100 meters. Very short-range (<45 meters) radio telemetry over the Citizen's Band frequency was successful in general and where interference is low, error-free data reception can be extended to more than 120 meters. The development is continuing.

RÉSUMÉ

Au cours d'un essai préliminaire, pour le développement d'un système bon marché, de saisie des données géophysiques, 32 Ko de mémoires vives furent ajoutées à un ordinateur VIC-2Ø de Commodore, pour enregistrer les données. Le système actuel comprends deux unités indépendantes: 1) une interface de conversion analogique-numérique, ayant une resolution de 8 bits, et possèdant 16 canaux d'entrée. 2) une interface de télémètrie, utilisant la modulation de fréquence pour la transmission des données, sur un canal. Les essais de laboratoire et sur les lieux ont confirmé l'utilité du convertisseur analogique-numérique, dans un grand nombre d'applications telles que la numérisation des formes d'ondes et le contrôle des événements. D'excellentes transmissions et réceptions de données furent realisées par cable, sur une distance de 1ØØ mètres. La transmission par radio à très faible-portée (<45mètres) utilisant la Bande Publique, fut en général, une réussite, et où l'interférence est faible, la réception correcte des données peut être augmentée au-delà de 12Ø mètres. Le développement se poursuit.

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GENERAL INTRODUCTION

This thesis concerns the preliminary development and testing of a practical, inexpensive system of geophysical data acquisition, based on the Commodore VIC-2Ø microcomputer.

The use of computers in geophysical data acquisition has traditionally been tied to the field of seismology. The accuracy,acquisition speed, and volume of data required, whether in exploration seismology or in theoretical seismology, have prompted seismologists to resort to the most advanced electronic equipment to achieve their goals. Unfortunately, this complexity of design and higher performance are often translated directly into very high financial costs that inhibit wider use of these systems.

In the 198Øs, more and more mining geophysical exploration companies are attempting to catch up with the computer revolution. The most recent examples of this are a whole range of microprocessor-based geophysical measurement equipment, such as gravimeters, magnetometers and EM systems, marketed by Scintrex Inc. of Toronto.

Monitoring natural short and long-term events, such as weather changes and earthquakes has become common-place since World War II. All over the globe, computers now make it much easier to operate monitoring stations. For example

there is a dense network of more-or-less computerized earthquake monitoring stations in the United States, spread over zones of earthquake activity. In Quebec, however, there is a gap to be filled in this regard. Less expensive equipment would make it more feasible to construct a dense local network capable of recording earthquake activity in a given area, and then relaying the information to a central station for processing.

The main goal of this thesis was to assess the possibility of reducing the cost of geophysical data acquisition by using components developed for the consumer mass market. The system was to be constructed around an easily affordable computer, yet one powerful enough to carry out most of the functions required in a monitoring station, or in a simple data acquisition application. One additional goal was to try to use the system with data telemetered by Citizen's Band radio. Telemetry is important in that it allows one to have on-line access to the information acquired at a monitoring station, without having to be present on the site. Successful use of the Citizen's Band would much reduce the usual costs of radio telemetry.

The thesis is organized as follows:

CHAPTER ONE discusses the selection of the computer used in this work, and compares it to other microcomputers available in summer of 1985, when this project began.

CHAPTER TWO describes the computer, its hardware and memory layout. Here, the internal architecture of the computer is explained. All information on the characteristics of the

computer relevant to this project is given, and a discussion of the Input/Output and various Ports is also provided.

CHAPTER THREE discusses the Expansion Port of the computer and presents the detailed description of connections for additional memory.

CHAPTER FOUR is devoted to the analog-to-digital converter used in the system. Here, the major features of this single chip data acquisition component, and its interface to the User Port of the computer are explained. Also included in this chapter are details of how one must program the analog-to-digital converter, and of the VICMON program written specifically for data acquisition using this system.

CHAPTER FIVE presents the results obtained during laboratory experiments and field work to test the performance of the converter.

CHAPTER SIX concerns an important aspect of this project: telemetry. The emphasis in this chapter is on problems encountered during the course of development. Here, we adhere to the basic approach taken in this work and try to use inexpensive radio equipment to achieve the objective of data transmission.

CHAPTER SEVEN presents the radio telemetry data obtained during laboratory and field tests.

CHAPTER EIGHT presents the conclusions and recommendations concerning this work.

CHAPTER 1: SELECTION OF THE COMPUTER.

Since 1979, the year "microcomputer" became a common term, an increasing number of companies have offered the consumer affordable computers, computer peripherals and computer softwares. One can mention such familiar company names as Apple, Texas Instruments, Atari, Commodore, and Sinclair. At the higher-cost end, IBM dominated the market in the early 80s, with their more sophisticated and much more expensive Personal Computer (PC). This was aimed primarily at business rather than science. Since 1980 the computer market has evolved, and so has the awareness of the public toward computers. At the same time, groups of computer enthusiasts have been formed all over the world, around particular brands.

Objective examination shows that each brand of computer has its strong points and weak points, that make it more attractive to a particular group of consumers. The point to stress is that there is no "best", in absolute terms, in the computer field. The best computer is the one that for many different reasons, satisfies the needs of its user and has earned his or her respect and attention. These reasons could be availability of hardware, of software, of accurate information on every aspect of the computer, sentimental reasons, or company reputation.

In this work, the Commodore VIC-20 computer was chosen

as the base upon which the data acquisition system would be constructed. The information given here however, can be easily transferred to other microcomputers provided care is exercised when modifying the connections to suit a particular hardware. Because one of the primary objectives in building this data acquisition system was to be able to use it in the field as well as in the laboratory, the VIC-2Ø has a number of advantages over most microcomputers:

1) the computer is built in the keyboard case, which makes it compact, light and convenient to carry.
2) there is direct access to the different ports (Expansion Port, User Port, Serial Port, Cassette Port, and Game Port) without having to open the computer case.
3) the cassette tape recorder used to record information does not need an external power supply (it uses the 9V DC line provided on the cassette port). This is a definite advantage in the field.

Considering that the computer serves as a means to convey data from one medium (the outside world) to another (memory, tape, disk), other more expensive Commodore computers, such as Commodore 64 and 128, offer no advantage over the VIC-2Ø. Although Commodore Business Machines has discontinued the production of the VIC-2Ø computer, one can still obtain the computer mainly through User Groups in Canada and the United States. Moreover, because the VIC-2Ø runs faster than any other Commodore computer

(except Commodore 128 in the fast mode) it is the most suitable of all eight-bit Commodore computers to use in the present application. Of all the popular microcomputers on the market, one tends to single out the IBM PC as a very powerful computer. This may be true in many situations, since the IBM PC has a pseudo-sixteen-bit microprocessor, has more memory than all eight-bit computers, and is faster. Most important of all, it has excellent software programs that turn the machine into a sophisticated piece of technology. However, and this is the IBM PC's biggest handicap, it is an eight-bit machine at the hardware level. Internally, the 8088 microprocessor chip used in the IBM PC is a sixteen-bit device with an eight-bit data bus. This means that data transfer to and from the computer must take place eight bits at a time. Therefore, from this point of view, it has no advantage over an eight-bit computer, such as the VIC-20, for the kind of interfacing application envisaged in the present work. Writing programs in the IBM PC machine language, on the standard system, does not provide us with a significant increase in speed, as compared with the VIC-20 machine language. The reason for this is that, in general, it takes two-to-three times more cycles to execute an 8088 instruction than it takes an instruction on the 6502 chip used in the VIC-20. Therefore, the speed gained through the higher speed of the IBM computer clock (4.77 MHz compared to 1.022MHz for the VIC-20), is partly lost in the execution of more cycles for each instruction.

There is however, the question of memory: large memory space is one of IBM PC's strongest features, but is very scarce on the VIC-20 computer.

The most important point to consider, in the context of this work, is the price of an IBM PC computer: between two and three thousand dollars Canadian. Even an IBM PC "compatible" or "clone" is many times more expensive than the VIC-20 computer: approximately one thousand dollars compared to 50 dollars for the VIC-20.

Finally, a very important reason for choosing the VIC-20 computer is that technical books and literature on the computer, its 6502 microprocessor, and its peripheral chips abound. This simplified the task of interfacing and programming the computer.

CHAPTER 2: THE VIC-2Ø.

2.1) The computer

The Commodore VIC-2Ø computer, like many 8-bit "micros" (i.e. microcomputers) is based on the 65Ø2 microprocessor, a chip manufactured by Rockwell International Corporation. This is by far the most popular and widely-used microprocessor in the industry. Although it is not as powerful as the Z-8Ø or the 68ØØ families of microprocessors, it is preferred over others because of its low cost: at the time of this writing it is possible to purchase a 65Ø2 for less than $1Ø Canadian.

In the VIC-2Ø the microprocessor runs at 1.Ø2272 MHz clock speed. This speed proves to be fast enough for almost all interfacing jobs that can be implemented on this computer, provided machine language programming is used.

The VIC-2Ø has a 64K address space limited by the 16-bit word structure of the program counter of the 65Ø2. However, unlike its successor, the Commodore 64, it can not use all of this 64K of memory as Random Access Memory (RAM). The standard system comes with only 5K of RAM, 3.5K of which is available for storing BASIC or machine language programs. This small amount of RAM could be a very serious handicap in many geophysical applications. This problem has been overcome in the present application by adding more memory to

the system.

The power supply for the standard VIC-2Ø computer is provided externally; a transformer feeds the computer with 9V ACfrom the 117 V line supply. In turn, this 9V AC is reduced to 5V DC by a zener diode circuit. The power rating is 4ØW input and 7.5W output, and in principle, one should be able to run the computer by directly supplying 9V DC from a 12V battery using dropping resistors.

To operate the computer in the field, an ordinary car battery and a converter capable of supplying 12ØV AC/6Ø Hz was used. The converter chosen for field work was the HEATHKIT model MP-1Ø power converter. It proved to be extremely stable and reliable, and ran the computer and a 7" television monitor for many hours during field work. The converter does not need to be 12V to 117V AC, but only 12V DC to 9V AC. However, 12V DC to 9V AC inverters are not readily available, and the only real saving achieved would be in dispensing with the step-down transformer of the VIC-2Ø computer.

Three major chips are tied to the 65Ø2 microprocessor to make the VIC-2Ø one of the easiest computers to interface with the outside world. The first chip is the 656Ø Video Interface Chip (VIC) designed for color video graphics applications such as low-cost CRT terminals, biomedical monitors, control system displays and arcade and home video games. It provides all the circuitry necessary for creating color-programmable character graphics with high-resolution

screens. The VIC also incorporates sound effects and analog-to-digital converters for paddle-s and a light pen. Videotaping the VIC-20 output signal on a video cassette recorder is also possible since the manufacturer has incorporated NTSC standards in the system. The system clock that drives the 6502 microprocessor and the two 6522 peripheral chips (described below) is provided by the VIC chip. This is derived from a 14.31818 MHz crystal.

The remaining two chips are 6522 Versatile Interface Adapter (VIA) chips. Each provides the computer with two peripheral Ports with input latching, two powerful interval timers, and a serial-to-parallel/parallel-to-serial shift register. The latter, (the serial-to-parallel/parallel-to-serial register) is not used on the VIC-20.

In sections 2.2 and 2.3, the specifics of how one programs these chips are discussed. As preliminary background, it should be noted that the 6522 VIA chip registers, like those of the 6560 VIC, are actually located within the chips themselves. This means that no RAM memory location is required, nor allocated, for the sake of communicating with these chips. When WRITing or READing values, one is actually accessing the registers directly. As we will see later on, special rules are applied for READing from or WRITing to some of these registers.

2.2) 6522 Versatile Interface Adapter 2 (VIA #2)

The VIA #2 chip, as it is called in the VIC-20 literature, will not be discussed in great detail, because it was not specifically accessed in this project at all, and does not need to be used.

The reason for this is that the operating system is the sole user of the VIA #2. It is used by the VIC-20 for such important (or vital) operations as keyboard scanning, generating interrupts every 1/60 of a second, servicing serial devices, handling tape input/output and READing joystick #3.

VIA #2's Interrupt Request (IRQ) line is directly connected to the 6502's IRQ line. That is how normal interrupts are generated in the VIC-20. To enable or disable interrupts, one can clear or set the proper flag (I flag) in the processor status register (.P) located at $030F (783) [from now on, the address of every memory location, and every register will be given in hexadecimal/decimal format; the number preceded by the dollar sign is the hexadecimal, base 16, number and the number in brackets is the decimal, base 10, number]. One uses the following BASIC statements:

Poke 783,Peek(783) AND 251, to enable interrupts and
Poke 783,Peek(783) OR 4, to disable them.
The equivalent machine code instructions are CLI and SEI.

When tape operations are performed, e.g. LOAD/SAVE, the

operating system changes the IRQ vector at $Ø314-Ø315 (788-789), because tape input/output depends on precise timing to WRITE and READ bits of data to and from the cassette tape. Therefore, such normal activities as READing the keyboard and updating the BASIC software clock variables TI and TI$, are suspended for the duration of the tape input/output timing.

Except for four available lines, CA1, CA2, CB1 and CB2, all lines on the VIA #2 Ports are used heavily by the operating system, making it the least desirable chip to rely on for general-purpose interfacing and programming. For this reason, almost all interfacing applications make use of the VIA #1 chip and the User Port, as described in section 2.3, following.

2.3) 6522 Versatile Interface Adapter 1 (VIA #1)

This is the chip that controls all operations performed on the User Port/RS-232 lines, most Serial Port pins, most joystick pins, the light pen/fire button pin, and the tape switch and motor pins. Here, we will give a brief summary of all the computer Ports, and their associated bits in the VIA #1, in Tables 1 to 4. The emphasis will be on the User Port and its many powerful characteristics. This will show how the User Port was programmed to perform the desired functions for controlling the analog-to-digital converter and the telemetry circuit. For more information the reader is referred to References 5 and 6 in the Bibliography at the end of this thesis.

Table 1: Serial Port Pins

Port Pin	Port Bit/VIA line		Description
1	(VIA2,CB1)		serial request in
2			ground
3			serial attention in
	A7	PA7	serial attention out
4	AØ	PAØ	serial clock in
	(VIA2,CA2)		serial clock out
5	A1	PA1	serial data in
	(VIA2,CB2)		serial data out
6	RESET		reset

N.B. To provide an external RESET switch to perform the same task as a COLD START, all one has to do is to ground pin 6 of the Port by connecting it to pin 2.

Table 2: Game Port Pins

Port Pin	Port Bit/VIA line		Description
1	A2	PA2	joystick Ø
2	A3	PA3	joystick 1
3	A4	PA4	joystick 2
4	(VIA2,PB7)		joystick 3
5	VIC chip		potentiometer Y
6	A5	PA5	light pen/fire button
7			+5 VDC
8			ground
9	VIC chip		potentiometer X

Table 3: Tape Port Pins

Port Pin	Port Bit/VIA line	Description
A-1		ground
B-2		+5 VDC
C-3	CA1	tape motor
D-4	(VIA2,CA1)	tape READ
E-5	(VIA2,PB3)	tape WRITE
F-6	A6 PA6	tape switch

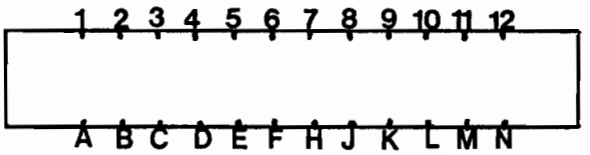
Table 4: User Port Pins

PORT A: TOP SIDE

Port Pin	Port Bit/VIA line		Description
1			ground
2			+5 VDC (1ØØ mA max.)
3			reset
4	A2	PA2	joystick Ø
5	A3	PA3	joystick 1
6	A4	PA4	joystick 2
7	A5	PA5	light pen/fire button
8	A6	PA6	tape sense switch
9	A7	PA7	serial attention out
1Ø			9V AC
11			9V AC
12			ground

PORT B: BOTTOM SIDE

A			ground
B		CB1	received data
C	BØ	PBØ	received data
D	B1	PB1	request to send
E	B2	PB2	data terminal ready
F	B3	PB3	ring indicator
H	B4	PB4	received line signal
J	B5	PB5	unused
K	B6	PB6	clear to send
L	B7	PB7	data set ready
M		CB2	transmitted data
N			ground



The User Port is a 24-pin (12/12) male edge connector on the VIC-2Ø. Facing the computer, the User Port is on the far left of the back. The User Port enables the VIC-2Ø to communicate with the outside world. The number and variety of lines available on this Port offer the possibility of implementing many interfacing projects. By referring to Table 4 on the previous page,or the complete memory maps of the computer on page 127, one sees that the VIA #1 is in control of the User Port. All the lines from this chip's Port B and some of the Port A lines are accessible to the user; without the User Port, most interfacing projects would be much more difficult to implement. Port A of the VIA #1 is on the top bank of the User Port, while Port B is located on the bottom.

2.3.1) VIA #1 Port A I/O register

This register is located at $9111 (37137).
Not all the Port's lines are available at the User Port. The following bit assignments will help in understanding what happens when one WRITEs to or READs from this location:

(PA7) bit7 = serial attention out; available on pin 9 of the User Port only: not used in this project.

(PA6) bit6 = cassette switch sense; available on pin F-6 of the Tape Port and pin 8 of the User Port. A value 1 here means that no tape buttons are down, while a value Ø means one or more cassette

tape buttons are down: not used in this project.

(PA5) bit5 = light pen/fire button; available on pin 6 of the Game Port and pin 7 of the User Port. A 1 in this bit means neither the light pen switch nor the fire button was pressed: not used in this project.

(PA4) bit4 = joystick 2; available on pin 3 of the Game Port and pin 6 of the User Port: used in this project to tie pin 6 of the User Port to pin 1B of the 2 by 4 decoder.

(PA3) bit3 = joystick 1;available on pin 2 of the Game Port and pin 5 of the User Port: used in this project to tie pin 5 of the User Port to pin 1A of the 2 by 4 decoder.

(PA2) bit2 = joystick Ø; available on pin 1 of the Game Port and pin 4 of the User Port: used in this project to tie pin 4 of the User Port to the START pin of the analog-to-digital converter.

(PA1) bit1 = serial data in; available on pin 5 of Serial Port only: not used in this project.

(PAØ) bitØ = serial clock in; available on pin 4 of the Serial Port only: not used in this project.

In order to alter or test the state of these bits, one can not directly WRITE to or READ from this location, i.e. $9111 (37137), before setting up the necessary bit conditions in the Data Direction Register (DDR). Each of the eight lines of this VIA #1 Port A is associated with a

corresponding bit in the eight-bit Data Direction Register A (DDRA) located at $9113 (37139). Basically, what this means is that the DDRA controls whether a line in its associated Data Register, in this case Port A, will serve as an input or an output. An example will further clarify this point. If a bit in the DDRA is zero, say bit 2, the corresponding line of Port A, in this case line PA2, or line 4 of the User Port, will be an input. Therefore one can only READ what is present on that line; WRITing this bit by WRITing to location $9111 (37137) will have no effect whatsoever on the state of the line or the bit itself. On the other hand, if a bit in the DDR is a one, the corresponding line of the Port will be an output, i.e. one can only WRITE to the Port; READing the Data Register can not be depended on to give the correct state of the line.

To repeat, in order to READ or WRITE Port A or Port B of a VIA one must use both the DDRA and the Data Register together.

Port A has two more lines, used for controlling external devices as explained below. These lines are called CA1 and CA2, and location $911C (37148) must be used to select their states. CA1 is directly wired to the RESTORE key of the keyboard for the purpose of generating a Non-Maskable Interrupt (NMI), every time the RUN/STOP and RESTORE keys are hit simultaneously. This will initiate a WARM START due to the fact that the VIA #1's interrupt line is connected to the 65Ø2's NMI line. A WARM START partially

resets the computer. The functions performed when a WARM START is signalled are as follows:

1) a call is made to the KERNAL CLRCHN routine that closes all files (KERNAL is the name given by Commodore to the table containing the vectors pointing to various operating system routines).
2) the default devices are reset, i.e. the keyboard as the input device and the screen as the output device.
3) the stack pointer is reset.
4) a jump is made to the READY routine to display the READY. message.

It is important to note that after a WARM START, the BASIC program and variables are preserved, and only the stack content is lost.

A transition from high to low or from low to high will generate the desired interrupt, given the correct bit setting of the Interrupt Enable Register (IER) located at $911E (37150). More about this is given in the section on Port B.

The CA2 line is used for tape motor control and is available on pin C-3 of the tape Port. Bits 1-3 of location $911C (37148) control CA2's status. Its bit settings are similar to those of CB2 line of Port B, although used to perform different functions. Since these two lines are not used in this project, we will skip over the details of their operations. For a complete description, see References 5

and 6 in the Bibliography.

2.3.2) VIA #1 Port B I/O register

This register is located at $911Ø (37136). All eight bits of this location have special meanings and are used by the operating system for the sole purpose of communicating with an RS-232 device such as a printer or a modem. VIC-2Ø has all the necessary software in its Read Only Memory (ROM) for this purpose. Because the RS-232 feature of the Port is not used for our purpose, we refer the reader to the books listed in the Bibliography. All the eight lines of the Port are accessible for use. When READing or WRITing this location, one has only to set the appropriate bits in the DDRB at $9112 or 37138, to accomplish the desired functions.

The other two lines of the Port are CB1 and CB2 as shownin Table 4 and in the memory maps of the computer on page 127. They are both used for "handshaking", although they perform in different ways. Handshaking is the term used when two devices communicate; it is necessary for each device to tell the other when data are to be sent or whether data have been received. Both CB1 and CB2 lines have special characteristics which make them suitable for handshaking. These two lines, like CA1 and CA2, can be accessed at location $911C (37148), called Peripheral Control Register (PCR). There is no DDR for this location, therefore WRITing to this location will effectively alter the state of each

bit. The bit allocations for the PCR are as follows:

Bits 7-5: **CB2 line control.** CB2 is used for serial data out, interrupt input, device output or shift register input or output. In the shift register cases these bits are ignored. The Interrupt Flag Register (IFR) is located at $911D (37149). Bit 3 of IFR is used for a CB2 interrupt. Bits 7 and 6 of the PCR control whether CB2 will be an output or an input. Bit 5 controls the setting of the CB2 line. The following is the detailed functional description of the CB2 control line. The binary number at the beginning of each paragraph shows the content of bits 7, 6 and 5 respectively.

ØØØ Interrupt Input Mode: this value sets IFR bit 3ona high-to-low transition ofthe CB2 line and clears the IFR bit 3 when Port B is READ or WRITten to.

ØØ1 Independent Interrupt Input Mode: this value sets IFR bit 3 on a low-to-high transition of the CB2 line, but does not clear IFR bit 3 when Port B is READ or WRITten to. IFR bit 3 is cleared by WRITing a 1 to it.

Ø1Ø Input Mode: this value sets IFR bit 3 on a low-to-high transition of the CB2 line and clears IFR bit 3 when Port B is READ or WRITten to.

Ø11 Independent Input Mode: this value sets IFR bit 3 on a low-to-high transition of the CB2 line,

but does not clear IFR bit 3 when Port B is READ or WRITten to. IFR bit 3 is cleared by WRITing a 1 to it.

100 Handshake Output Mode: this sets the CB2 line to low when Port B is WRITten to. CB2 will be set high when a CB1 transition occurs.

101 Pulse Output Mode: the CB2 line is set low for one cycle when Port B is WRITten to with this bit value.

110 Manual Output Mode: this value sets CB2 to be low.

111 Manual Output Mode: this value sets CB2 to be high. On power-on or when a reset is performed, these bits are set to one.

Bit 4: **CB1 control line.** CB1 is used to accept an interrupt for received data, as a transition of voltage on this line, and as output for the shift register clocking pulses at $911A (37146).

It is not possible to READ CB1 directly. The CB1 line is designed to set a flag (bit 4) in the IFR when a transition occurs on the CB1 line.

This bit (bit 4 of PCR) determines whether CB1 will set the flag on a low-to-high transition or on a high-to-low transition. Once the CB1 flag is set, it will stay set until it is cleared by a READ or WRITE to Port B. Moreover if bit 4 in the

Interrupt Enable Register (IER) is set and the interrupts are enabled, the transition will also cause an IRQ.

A zero here means that the IFR bit 4 is set on a high-to-low transition of CB1 when this bit is set to this value. This is the default setting of this bit.

A one in this position means that the IFR bit 4 is set on a low-to-high transition on the CB1 line.

Bits 3-0: **CA1 and CA2 control lines.** These bit settings were discussed in the previous paragraph.

One potential problem associated with the VIC-20 computer is that it has only one IRQ vector, located at $0314-0315 (788-789). However, there could be many sources of interrupt, if several devices are connected to the computer. Everytime an IRQ interrupt is signalled to the 6502 microprocessor, whether it is by an external device or the 6522 VIA #2 which is responsible for generating system interrupts every 1/60 of a second, the routine pointed to by the above IRQ vector is executed. This vector normally points to the KERNAL IRQ handler routine at $EABF (60095), which READs the keyboard and updates the TI and TI$ software clock variables, among other things. To be able to recognize interrupts from other sources, one must change the vector at $0314-0315 (788-789), to point to the machine language routine written specifically to execute the desired task. It

is therefore the responsibility of the programmer to identify the source of the interrupt and take the necessary steps to process it.

Besides the two Ports in the VIA #1, this chip contains a Shift Register, an Auxiliary Control Register and two Timers. Because the Shift and the Auxiliary Control registers do not take part in any stage of this project, they will be ignored. Of the two timers, the first one is of paramount importance to this project. Therefore, some time will be devoted to explaining how it works and how it can be programmed. The second timer, although almost as powerful and useful as the first timer, is not used by our system for reasons that will be explained in the chapter on telemetry (Chapter 6). Let us therefore describe VIA #1 TIMER 1. Referring to the computer's memory maps on page 127,one can note the following addresses:

$9114/37140 TIMER 1	least significant byte (LSB) of count.
$9115/37141 TIMER 1	most significant byte (MSB) of count.
$9116/37142 TIMER 1	(LSB) latch byte.
$9117/37143 TIMER 1	(MSB) latch byte.

The operating system uses this timer for RS-232 and User Port transmit/receive and tape WRITE timing. However, when an RS-232 device is not connected to the User Port, one can freely program TIMER 1.

TIMER 1 can operate in two different modes: the one-

shot time interval mode and the free-running mode. In the one-shot mode the programmer initializes the TIMER with the desired values and the TIMER starts counting down at the rate of the system clock. Once it reaches zero it stops. In the free-running mode, when the counter reaches zero, the values from the latch registers located at $9116 (37142) and $9117 (37143) are loaded into the the counter registers at $9114 (37140) and $9115 (37141), and the TIMER starts the countdown all over again for as long as the program allows it or the computer is powered ON.

To select the desired mode for TIMER 1, one has to set the proper bits in the Auxiliary Control Register (ACR), located at $911B (37147). It was stated that the ACR is not used and will not be discussed. This is the case because, on power-up, the values in this register are by default set for the free-running mode and no PB7 output pulses. This is exactly what is required in our application.

Here is how the TIMER 1 is programmed in the free-running mode:

(a)- Store the LSB (least significant byte) of the desired time period in location $9116 or 37142. This follows the 6502's representation of 16-bit numbers: low byte first and high byte second. As an example consider the number 1024 or $0400; this value is stored in memory as 00, 04 instead of 04, 00. Therefore, to find the most significant byte and the least significant byte of a 16-bit number, one can use the following formula:

high byte = INT(number / 256)

low byte = number - high byte * 256

(b)- Store the MSB of the desired time period in location $9115 (37141). At the same time the VIA #1 copies this value into location $9117 (37143), and starts the countdown of TIMER 1 at the rate of 1.Ø22720 MHz. This is preceded by copying the value in location $9116 (37142) into location $9114 (3714Ø), i.e. the low-order latch contents into the low-order counter. Also the flag register in IFR at $911D (37149), bit 6, is set to zero.

(c)- Load the latch registers (LSB) at $9116 (37142) and (MSB) at $9117 (37143) with a new value if desired. When the counts in the TIMER 1 (LSB) and (MSB) reach zero, the flag in IFR , bit 6, is set to 1, and an NMI interrupt is signalled to the 65Ø2 if bit 6 in the IER at $911E or 3715Ø allows it. By default, that bit is set to zero, thus disabling all interrupts; that is, an interrupt will not occur every time the count expires. This default value is not changed in our application.

(d)- Next, the values from the latches are automatically reloaded into the counter bytes, and the countdown starts once again.

(e)- It is, however, possible to check under software control to see whether the TIMER 1 count registers have expired, by testing bit 6 of IFR at $911D (37149).

(f)- READing the count register's (LSB) at $9114 (3714Ø) or WRITing the count register's (MSB) at $9115 (37141) will

clear bit 6 of IFR. After this bit has been cleared, one goes back to step (e) to test it, for as many times as it is required.

This allows one to set up a very precise interval timer for the purpose of sampling data coming from an external device such as an analog-to-digital converter. To calculate the values for the (LSB) and (MSB) of TIMER 1, so that the desired time interval between successive READings is obtained, one can use the following steps:

(a)- select the sampling frequency (SF) in Hertz.

(b)- calculate the time period corresponding to this:

$$T = 1 / SF \quad \text{seconds.} \tag{2.1}$$

(c)- calculate the number of counts (NC):

$$NC = (T * 1.02272E+6) - 2 \tag{2.2}$$

NC is the number that must be loaded into the TIMER 1 count registers so that when the countdown is over, a time period equal to T seconds has expired. The number 1.02272E+6 is the speed in Hertz of the clock that drives the microprocessor and the two VIA chips, as derived by the VIC chip from the 14.31818 megahertz two-phase oscillator clock.

The largest value the (LSB)/(MSB) registers can hold is $FFFF or 65535. By reversing the above formula (2.2), we can determine the amount of time this represents:

$$T = (NC + 2) / 1.Ø2272E+6 \qquad (2.3)$$

(655353 + 2) / 1.Ø2272E+6 = Ø.Ø64 seconds.

In the free-running mode, these registers are re-loaded from the latch registers. Because of this, larger time periods can be realized by counting the number of times the TIMER 1 registers reach zero. The subroutine DELAY, in the two programs VICMON, and VICTM (Chapters 4 and 6), written specifically for this project, sets up a 16-bit software register to do this. By carrying out the same calculation as above, one can determine the maximum time interval possible using a 32-bit number; thus, the largest number a 32-bit unsigned integer (16-bit software register plus 16- bit TIMER 1 count register) can hold is $FFFFFFFF or 4294967294. Putting this value in the above formula (2.3), one gets:

(4294967294 + 2) / 1.Ø2272E+6 = 42ØØ seconds.

= 7Ø minutes.

By loading the appropriate registers with the value above, i.e. 4294967294, one can sample data at a rate of one sample every 7Ø minutes or one hour and ten minutes. This represents the slowest sampling rate that one can use in the present configuration. At this rate, using all the 32K of memory buffer available, one could sample data for 4 years, 4 months, 12 days, 21 hours and 2Ø minutes. The fastest sampling rate is really dependent on the type and the speed

of the input device(s) one is working with. This particular point and examples of sampling rates, will be discussed in the sections on the analog-to-digital converter (Chapter 4) and the telemetry circuit (Chapter 6).

This completes the overview of the different Ports, chips and registers relevant to the interfacing works done using the VIC-20 computer. The next chapters will show exactly how these features of the computer were put to use to build the analog-to-digital converter and the telemetry circuit interfaces.

2.4) 6560 Video Interface Chip

Although the 6560 Video Interface Chip is one of the most important building blocks of the computer, with many interesting and powerful features such as sound, high resolution screens, programmable custom character and analog-to-digital conversion capability, we will not describe it because it does not have any direct bearing on the interfacing job we set out to do. The VICMON program, however, does use the custom character capability of the chip to set up a high resolution screen starting at $1800 (6144), in order to plot the sampled data obtained from the analog-to-digital converter.

Because the plotting routine written for this purpose is in machine code, and is therefore extremely fast, an interesting application would be to combine its speed with a faster conversion rate of the analog-to-digital converter chip, to effectively build a one-channel (or multi-channel)

digital oscilloscope, to display signals with a frequency of approximately one kilohertz or less. One would have to implement the proper amplitude scaling of the input signal in hardware, a task that could be realized fairly easily. A software program could then be written to shift the stored signal in any direction, and provide user-selectable scaling, resolution and most of the features conventional oscilloscopes offer.

2.5) Memory Maps

The detailed memory maps of the VIC-20 computer is given on pages 127 to 134 of Appendix A. For more information the reader is referred to References 5 and 9 as listed in the Bibliography.

The following is the modified memory maps of the computer, meant as a quick guide. It differs from the standard VIC-20 system,that is from the system with only 5K of memory. It shows which special blocks and locations have been set aside for use by the computer's operating system and how some of these locations are used in the context of this project.

$0000-$00FF: page zero.

Very important 256 bytes of memory in every eight-bit computer. VIC-20 reserves this area to keep vital registers and pointers used by BASIC ROM and the operating system.

VICMON and VICTM also make extensive use of these memory locations.

$0100-$01FF: page one.

Processor stack area.

$0200-$02FF: page two.

Used mainly to hold the input buffer, the keyboard buffer and some operating system registers.

The input buffer from $0200 (512) to $0258 (600) is used by VICMON and VICTM.

$0300-$03FF: page three.

Used exclusively to hold the table of vectors pointing to different BASIC ROM and operating system routines. It also contains a 194 byte buffer for tape input/output.

$0400-$0FFF: 3K expansion RAM area.

Not used in this project.

$1000-$11FF: screen memory.

$1200-$? : user BASIC area.

In this project the range $1200-$1FFF is used to hold the software program, a 1408-byte high-resolution screen and a 32-byte information storage buffer containing all parameters entered by the user.

$2000-$3FFF: 8K expansion RAM/ROM block 1.

Added to the system.

The first 512 bytes of this area are used by the VICMON program to set up a circular buffer.

$4000-$5FFF: 8K expansion RAM/ROM block 2.
Added to the system.

$6000-$7FFF: 8K expansion RAM/ROM block 3.
Added to the system.

$8000-$8FFF: 4K character generator ROM.

$9000-$93FF: I/O block 0.

$9400-$95FF: Location of colour RAM when additional RAM blocks 1, 2, or 3 are mapped in.

$9600-$97FF: Normal location of color RAM.

$9800-$9BFF: I/O block 2.
(not available in the standard system nor in the present configuration).

$9C00-$9FFF: I/O block 3.
(not available in the standard system nor in the present configuration).

$A000-$BFFF: 8K decoded block for expansion RAM/ROM.
Added to the system.

$C000-$DFFF: 8K BASIC ROM.

$E000-$FFFF: 8K KERNAL ROM (operating system).

CHAPTER 3: EXPANDING THE VIC-2Ø

3.1) Introduction

This chapter deals exclusively with the Expansion Port of the VIC-2Ø computer. Here we will present the signals available to the user on this Port, and show how memory was added to the system to increase the storage space for data. This Port could also be used to interface the computer with an external device or devices, such as the analog-to-digital converter discussed in Chapter 4. Although using this Port offers the possibility of putting all the circuits, i.e. the additional memory and the analog-to-digital converter, on one board, this economy in space could only be gained at the expense of more complicated circuits to match all the features the User Port provides. For this reason, this Port is only used for memory expansion in the present project.

3.2) Expansion Port

This Port is used for expansions of the system that require access to the address bus and the data bus of the computer. Caution must be exercised, when using this Port, because it is possible to damage the computer, if the connections are not made properly, or if the user equipment

malfunctions.

The expansion connector is a 44-pin (22/22) female edge connector, on the back of the computer. Facing the VIC-20 the Expansion Port is on the far right of the back. The Expansion Port signals are given in Table 5 on page 40. The following is the functional description of the Port's available signals:

Data bus: pins 2 to 9 inclusive.

The data bus is used to move data to and from additional memory or I/O devices.

BLK signals: pins 10 to 13 inclusive.

These four block signals are for memory expansions of the system. Each one provides a different 8K block of memory; the chip is active when these pins go low. Blocks 1, 2, and 3 can be used for RAM or ROM. If memory is added, these locations will be used by BASIC. Memory in block 5 can be used for RAM or ROM. However, if RAM is added, this area will not be accessible to BASIC. Only machine language programs will be able to use it.

RAM signals: pins 14 to 16 inclusive.

These are 3 more decoded active low signals. Each oftheRAM signals controls a 1K memory block. Therefore, if all the three lines are used, 3K of memory can be added to the system sitting at $0400 (1024).

Read/Write: pins 17 and 18.

the READ/WRITE signals are responsible for informing the memory or the device being addressed whether the system wants to READ data or WRITE data. If the line goes high, a READ is expected; if the line goes low, a WRITE is to be performed. The R/$\overline{W}$ signal on pin 17 is connected to the VIC chip (VR/$\overline{W}$). The other, on pin 18, is connected to the 65Ø2 microprocessor (CR/$\overline{W}$). Most memory expansion circuits will normally use the CR/$\overline{W}$ signal. There is a mistake regarding this point in the Programmer's Reference Guide (Reference 4); there it says that memory expansion normally uses VR/W, which obviously is incorrect.

Other devices may need to use the VR/$\overline{W}$ signal.

IRQ: pin 19.

This interrupt request line is used internally by the computer for keyboard scanning and the system clock.

Address bus: pins B to S inclusive.

These lines determine which memory locations or I/O device the computer will READ from or WRITE to. The actual address bus is 16 bits wide, but only 14 bits are available on the Port. The reason for this is that the other two bits are decoded into the block and I/O signals.

I/O: pins T and U.

Either or both of these signals can be used to add more I/O devices to the computer. It is perfectly possible to add a third 6522 VIA here, to provide some of the User Port's features.

S/O2: pin V.

The system clock is available on this line to run such devices as a 6522 VIAchip, as noted above.

NMI: pin W.

The non-maskable interrupt line here, can be used to trigger a WARM START, as when the RUN/STOP RESTORE keys are pressed simultaneously. This is done by grounding pin W.

RESET: pin X.

a COLD START is initiated when pin X is grounded This is equivalent to turning the computer off and back on again. Therefore, everything is reset including the memory, so in fact any program in the computer at the time of RESET is erased.

It must be clear by now that, without building an address decoding circuit, one can easily add 35K of RAM to the system. In the present project, only 32K of memory was added, using decoded block lines available on the Expansion Port. Hitachi's HM6264p-1Ø series static RAM chip was used to do the job. The specification sheet for this chip is given on page 137 in Appendix B. Page 136 shows the actual connection diagram for one 8K block. The four 8K blocks of

memory added share the same address bus and data bus. The chip select pin (CS1) of the memory chips (active low) is connected to each of the desired BLK lines of the Expansion Port. The truth table on the specification sheet shows when a READ or a WRITE can be performed. Since a WRITE is done when both the WRITE line (WE) of the chip, pin 27, and the output enable (OE), pin 22, are low, and a READ is done when the WE is high and OE is low, a hex inverter is used, as shown on the connection diagram.

When these four 8K blocks of memory are installed, the user BASIC area extends to more than 28K, and there is an 8K block of free RAM sitting at $A000 (40960), which could be used for storing data or for machine language programs. This area has the advantage of being out of BASIC's reach, therefore it will not be disturbed unless the user decides to WRITE to it or destroy it. The three 1K blocks were not used, first because of lack of room on the interface board, and secondly because the addition of 32K of memory was enough for our purposes.

There is the possibility of adding even more memory to the system, although this has not been attempted in the present work. Because the memory space the 6502 can address is limited to 64K, if more memory is required, it could be added in blocks of 64K. Because there are no decoded block signals for memory expansions besides those discussed in the paragraphs above, one must provide a new address decoding circuit. In theory one could have as many 64K blocks of

memory as required, provided one also adds the necessary bank switching circuit, that is the circuit that would allow one to selectively enable the desired block of added memory for storing or retrieving data. In this situation, direct READs or WRITEs from/to the extra memory would no longer be possible. Rather, one would have to move the desired block(s) of data from the expanded memory to the "old" memory space, before the desired operations could be performed on them. The added memory could only be used as a storage space for data, a possibility that might be attractive in many applications, especially in an extension of a project such as the one we have undertaken in the present work. The transfer of data from/to the extra memory could be made to execute extremely fast, provided the Direct Memory Access (DMA) chip chosen to do this job is fast. (Commodore Business Machines Inc. offers such a memory expansion cartridge for the Commodore 64 and 128 computers). Such a large memory space could offer one the possibility of monitoring a given event for a very long period of time, thus freeing the operator and the system from SAVing data to tape, which is a very slow process, every time a valid signal is recorded.

Table 5: Expansion Port.

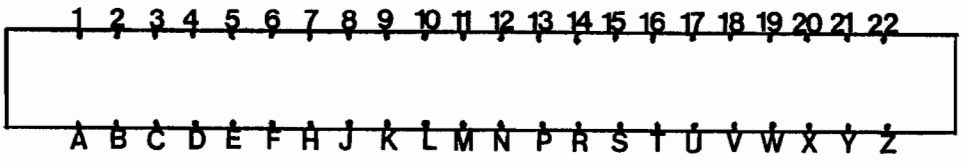
TOP SIDE

NAME	PIN#	DESCRIPTION
GND	1	system ground
CDØ	2	data bus bit Ø
CD1	3	data bus bit 1
CD2	4	data bus bit 2
CD3	5	data bus bit 3
CD4	6	data bus bit 4
CD5	7	data bus bit 5
CD6	8	data bus bit 6
CD7	9	data bus bit 7
$\overline{\text{BLK1}}$	1Ø	8K decoded RAM/ROM block 1, at $2ØØØ (active low)
$\overline{\text{BLK2}}$	11	8K decoded RAM/ROM block 2, at $4ØØØ (active low)
$\overline{\text{BLK3}}$	12	8K decoded RAM/ROM block 3, at $6ØØØ (active low)
$\overline{\text{BLK5}}$	13	8K decoded RAM/ROM block 5, at $AØØØ (active low)
$\overline{\text{RAM1}}$	14	1K decoded RAM block at $Ø4ØØ (active low)
$\overline{\text{RAM2}}$	15	1K decoded RAM block at $Ø8ØØ (active low)
$\overline{\text{RAM3}}$	16	1K decoded RAM block at $ØCØØ (active low)
VR/$\overline{\text{W}}$	17	READ/WRITE line from VIC chip (high READ/low WRITE)
CR/$\overline{\text{W}}$	18	READ/WRITE line from CPU (high READ/low WRITE)
IRQ	19	interrupt request line to 65Ø2 (active low)
(NC)	2Ø	no connection
+5V DC	21	+5V DC used by interfacing circuits
GND	22	system ground

Table 5: continued...

BOTTOM SIDE

NAME	PIN#	DESCRIPTION
GND	A	system ground
CA0	B	address bus bit 0
CA1	C	address bus bit 1
CA2	D	address bus bit 2
CA3	E	address bus bit 3
CA4	F	address bus bit 4
CA5	H	address bus bit 5
CA6	J	address bus bit 6
CA7	K	address bus bit 7
CA8	L	address bus bit 8
CA9	M	address bus bit 9
CA10	N	address bus bit 10
CA11	P	address bus bit 11
CA12	R	address bus bit 12
CA13	S	address bus bit 13
$\overline{\text{I/O2}}$	T	I/O block 2 at $9800
$\overline{\text{I/O3}}$	U	I/O block 3 at $9C00
S/O2	V	phase 2 system clock
$\overline{\text{NMI}}$	W	6502 non-maskable interrupt (active low)
$\overline{\text{RESET}}$	X	6502 reset pin (active low)
(NC)	Y	no connection
GND	Z	system ground



CHAPTER 4: THE ANALOG-TO-DIGITAL CONVERTER

4.1) Introduction

An analog-to-digital (A/D) converter, as its name implies, is a device that allows one to convert analog voltages generated by analog devices into a binary format that digital devices can understand. Although they have been around for a long time, recent advances in microelectronic technology have brought the hobbyist and the non-professional experimenters a new generation of A/D chips that are relatively inexpensive, and easy to interface and program.

One source of confusion when selecting an A/D converter is the variety of designs available to the experimenter. These chips use different techniques to achieve the same end result. The cost of these microchips follows directly the complexity of design and more importantly, the speed of conversion. Slow converters may be purchased for a few dollars, but the price tag on the ultra-fast converters may range in the thousands of dollars.

National Semiconductor markets a number of analog-to-digital converters, of which the model ADCØ816CCN was selected for this project. This converter provides a number of features including:

1) a single-chip data acquisition system;

2) a 16-channel input multiplexer that can directly access any one of the 16 single-ended analog signals;
3) easy interfacing to all microprocessors by providing latched and decoded multiplexer address inputs and latched TTL three-state outputs.

This advanced chip can especially be appreciated by anyone who has tried to build his or her own A/D board using the "old" technology of building the sample-and-hold circuit and all the rest. In order to come up with a board that has the capabilities of this chip, one would have to use a dozen IC components. At the time of writing, these A/D chips are available for less than $30 Canadian (e.g. at Hamilton-Avnet Inc.).

In this chapter, we will discuss all the major characteristics of the analog-to-digital converter, how it was interfaced with the User Port of the computer, how it is programmed, and how one must prepare and condition the desired signal(s) before they are fed to the analog-to-digital converter.

4.2) The NSADC0816CCN analog-to-digital converter

The ADC0816 and ADC0817 families of A/D converters are eight-bit converters; this means that they use 256 (two to the power of eight) steps or discrete values, for representing an analog voltage. This gives a dynamic range of 48 dB, approximately that of a home tape recorder.

The ADC0816 itself is accurate to plus-or-minus half-a-bit over a temperature range of about -40 to +85 degrees Celsius. The ADC0817, on the other hand, has plus or minus one bit accuracy over the same temperature range. One other reason for the selection of the ADC0816 eight-bit converter, is the fact that it matches the eight-bit structure of the 6502 data bus. This means one has to READ the chip only once to obtain the digital value, as opposed to converters with 12, 14, or 16 bit resolution, that require two consecutive READs to retrieve the data.

Pages 145 to 156 in Appendix C provide all the technical information needed to use this chip. The chip accepts input voltages between zero and V_{cc} only. V^{cc} can range from 4.75 to 5.35 Volts. If voltages outside this range are applied to any one of the converter channels, they will damage the chip. If V_{cc} is fixed at 5.12 volts (notice that 5.12 is an exact multiple of 256), the accuracy of the converter will be: 5.12 / 256 = 20 mV, precise enough for most but not all applications. In the petroleum industry for example, accuracies up to 14 or 16 bits are generally required; however a 16-bit converter with a conversion rate

similar to that of the ADCØ816 would be many times more expensive.

The chip uses the successive approximation technique to convert analog voltages (see Appendix C). The heart of this single chip data acquisition system consists of three important parts: a digital-to-analog converter (DAC), a successive approximation logic unit or register (SAL), and a comparator. The process of approximating the analog voltage is as follows:

Before the start of conversion the SAL and the DAC are at level zero. Once the conversion starts the SAL enables its bits and sends a bit pattern to the DAC. The DAC will generate a voltage whose value is compared to the input voltage. The comparison is done on a bit-by-bit basis, starting with the MSB (Most Significant Bit). If the input signal is greater than the DAC output, the corresponding bit in the SAL is set to a one. If the input is smaller, a zero is set in the corresponding bit. After all the bits have been tested, a new bit pattern is in place, which is sent again to the D/A. This will bring the D/A output voltage closer to the input voltage. When the D/A output is as close as it can be to the input voltage (i.e. within the resolution of the converter chip), the SAL sends out an End-Of-Conversion (EOC) signal. The rule is that for an n-bit converter n iterations are performed.

The accuracy of the converter is very much dependent on the performance of the comparator. Pin 19 (REF+) and pin 23 (REF-) are the reference voltage pins for the comparator. In

order to get precise results, these pins must be connected to a stable voltage source. One can build a power supply using the 9V AC output on pins 1Ø and 11 on the User Port. Because of lack of space on the main interface board, we decided to do without the power supply. Instead, the system voltage source, i.e. the system ground and positive 5V DC provided on the User Port, was used. The system ground and positive 5 volts proved to be stable enough for our purposes. For the detailed description of the interface, the reader is referred to paragraph C.1 of Appendix C on page 139.

The way the interface is currently built, the START and the ALE pins of the converter are wired to line 4 of the User Port. Bit 2 of the VIA #1 Port A controls the state of line 4. To initiate the conversion process, a positive pulse must be sent on line 4 of the User Port. To be exact, the start-of-conversion pulse must have a width of at least 8 microseconds as described in Appendix C on page 138. If the program that controls the converter is written in BASIC, raising line 4 and then lowering it immediately, to simulate a start pulse, requires two POKES. It takes VIC-2Ø far more than 8 clock cycles to execute those instructions. Indeed, it takes more than 1ØØ microseconds, the time required by the A/D chip to complete one conversion. Therefore, it is not at all necessary to wait and test for the EOC signal. After the start-of- conversion signal is sent, one can raise the CB2 line (line M of the User Port

wired to pin 21 of the A/D chip), READ the digitized value, lower the CB2 line, and start another conversion process if desired. If the program is written in machine code, however, one has to make sure that the start- of-conversion pulse has a width of at least 8 clock cycles and that one tests for the EOC signal. In the present configuration, as soon as the EOC signal is sent, the CB1 line (line B of the User Port), programmed to set the flag for a low-to-high transition, responds by setting bit 4 of the IFR at $911D (37149). Since 1ØØ microseconds is a lot of time to waste, while waiting for the A/D chip to finish the conversion and send the EOC signal, one can put the notion of parallel processing to work, if the software program is written in machine code. In fact, the program written for this project, VICMON, uses this principle to perform a whole range of housekeeping tasks, while the converter is busy carrying out its duties. These include, among other things, storing the previously READ data in the data buffer, checking whether the end of the buffer is reached, selecting the next channel to be sampled, and of course, waiting for the A/D chip to send the EOC signal. This means that the only overhead associated with monitoring the A/D chip is the retrieval of data after the EOC is detected, the loading of TIMER 1 registers with the appropriate values to perform a delay corresponding to the selected sampling rate, and the transmission of the new start-of-conversion pulse. "Overhead" refers to the time "wasted" in operations other than the basic time required by the converter chip to finish one conversion. In the case of

the ADCØ816, the conversion rate is 1ØØ microseconds; that is, in theory, one can sample a signal at the rate of one sample every 1ØØ microseconds. However, in practice, there are a certain number of operations that must be performed before and after the conversion process, as explained in the above paragraphs. These operations take time and will add to the basic conversion time required. Therefore, one will never be able to sample at a rate of exactly 1ØØ microseconds.

The VIC-2Ø Programmer's Reference Guide (Reference 4) has a section on machine language programming, where one can find how long it takes for a given instruction to execute. One therefore can calculate the amount of overhead added by the program to the 1ØØ microseconds it takes the converter to complete one conversion. The fastest sampling uses one channel only, without calling the DELAY subroutine. The overhead for this amounts to 156 microseconds, which means a maximum sampling rate of 6.41 KHz with the present configuration. Of course, one could increase this rate by increasing the clock speed of the converter and by rewriting the code to further reduce the overhead.

The values loaded into the TIMER 1 registers are calculated for a given sampling rate using the formula given in paragraph 2.3.2. However, one has to subtract from those values the amount of overhead associated with all the operations mentioned above, to get the exact number of counts for the TIMER 1 registers. This way, the time it

takes for TIMER 1 to count down to zero plus the overhead time will equal the time period T that must expire, if we are to achieve the exact sampling rate.

There are a number of additional details that one has to discuss. Notice that pins 15 and 18, Multiplexer Out and Comparator In respectively, of the A/D chip are tied together (see page 143). Remembering how the successive approximation technique works, one can easily understand that the input to the comparator, namely pin 18, is the voltage READ on the selected channel, i.e. line IN0 to IN15 of the A/D chip. The multiplexer, a 4-by-16 multiplexer, has 16 inputs, selected via pins 33 to 36 of the chip, but only one output, pin 15. It is this pin (pin 15) that presents the comparator with the voltage that we wish to digitize. What all this implies, is that whenever a channel is being read, the voltage present on that channel is also present at the output of the multiplexer.

An interesting characteristic of the ADC0816 chip is the possibility of including additional channels, if more than 16 channels are required. However, 16 channels are more than sufficient for the present objective. Therefore, the expansion capability of this chip was disabled by connecting pin 37 to positive 5 volts DC as recommended in the specification sheets.

Finally, to run the ADC0816 chip, one has to provide the converter with a square pulse generator. Typically (see Appendix C), the converter is driven by a 640 KHz clock. At this rate, the conversion time, under ideal conditions (see

Appendix C), is 100 microseconds (or 10 KHz sampling rate) exactly. This sampling rate is more than enough for most geophysical data acquisition and therefore this clock speed was implemented in the present work.

There are many ways of building a pulse generator, such as using the 555 timer or the 4001 Quad NOR gate or the 4011 Quad NAND gate. Because of space management considerations, a circuit with the fewest components and the best performance was chosen. This clock was built using the 74LS04 hex inverter, two resistors and a variable capacitor, though in the final version the capacitor was replaced by a fixed 1500 pF capacitor giving a clock speed close to the 640 KHz required. However, no change in the conversion time was observed.

As stated in the specification sheets, the clock speed of the A/D chip can be set to run from 10 to 1280 KHz. With a 1280 KHz clock speed, the conversion time drops to around 50 microseconds, although this may vary slightly from chip to chip. Some of these converters could even be run on a 2 MHz clock without damage to the chip, but one would have to test a number of these converters to find the one that performs well at that rate (National Semiconductor Sales Representative, personal communication, 1985). If a chip is found that can handle 2 MHz clock speed, then the conversion time will further drop to 35 microseconds.

4.3) Signal Conditioning and Input Protection

It was stated in the above section that the input voltages applied to the A/D's channels must not exceed TTL levels (i.e. voltages between zero and +5.25 volts). In many applications, one has to deal with voltages outside this range. In seismic work, the output of the geophones is of the order of millivolts. In heat flow measurements, the range of measured temperatures could be in hundreds or thousands of degrees. However, the transducer output voltage may be in microvolts, far too small to be measured directly by the converter without prior conditioning. There is also the question of input protection, that is making sure that once the signal to be measured is brought to the required levels, it does not go negative or exceed V_{CC}.

In the first case, i.e. signal conditioning, one can use the appropriate amplifiers for the work at hand. Amplifier design will be only discussed for applications considered in the present work. As for input protection there are a number of ways to achieve the desired results. One is to use current-limiting resistors and zener diodes to clip out all undesired amplitudes. Another way, followed in this project, is to use the LM3900 "NORTON" amplifier. This chip operates from a single polarity power supply, making it ideal for interfacing projects. It has an open-loop gain of 70 dB and a bandwith of 2.5 MHz, when operated asa unity gain amplifier. The most useful and interesting characteristic of this amplifier is that its ouput swings

between ground and V^{CC} minus one volt exactly. What this implies is that, when the chip is powered with a 6 volt battery or power supply, i.e. V^{CC} = 6V, the output will invariably oscillate between Ø and +5V DC. Voltages outside this range are clipped out right at these boundaries.

Many signals in the real world swing above and below ground, and to be able to measure these voltages with the analog-to-digital converter, one has to scale them in the range zero to V^{CC}. Using the LM39ØØ amplifier to design an AC amplifier whose output is biased to any desired DC level within the range of the output voltage swing, is straightforward. Moreover, AC gain is independent of biasing. The only disadvantage in using the LM39ØØ is that it is not suitable for ultra-low noise performance.

In all the experiments conducted in this work, an inverting AC amplifier with a biased output of +2.5volts, for Ø volts input, was used. The gain of the amplifier varied as was required by the type of work being carried out, but it never exceeded X2Ø amplification. The reason for a biased output of +2.5 volts is that it is mid-way between the lower and upper allowable input voltages to the A/D chip, i.e. Ø and +5 volts. Since the amplifier is used in the inverting mode, all the negative voltages are translated to positive voltages between +2.5 and +5 volts, and all the positive voltages are scaled between Ø and +2.5 volts. To clarify the matter, consider the following example. Suppose one is to measure a signal that ranges between -1 and +1 volts, and the amplifier is set to operate

in the inverting mode with a gain of 2.5. If the output is biased to +2.5 volts, at the output of the amplifier for an input voltage of -1 one would measure:

- (-1 * 2.5) + 2.5 = +5 volts,

and for an input of +1 volts one would get:

- (+1 * 2.5) + 2.5 = Ø volts.

The importance of the discussion in the previous paragraph becomes apparent when we try to calculate what values the A/D converter will produce, when the output of this amplifier is applied to one of its channels. Remembering that we are dealing with an eight-bit converter, the only possible discrete values one can obtain are in the Ø to 255 range, giving a total of 256 numbers (2 to the power of 8) altogether. For an input of Ø volts, the converter will translate this voltage into a decimal value of Ø. For an input voltage of V^{CC} volts, the decimal value output by the converter will be 255. Each intermediate voltage will have a decimal value between Ø and 255. The output of the converter is linearly proportional to the input analog voltage. Therefore, a voltage of $V^{CC}/2$ volts gives decimal 128. Now considering the voltages applied to the input of the amplifier, one can state the following: all the voltages between Ø and -1 volts will be converted to decimal values between 128 and 255 respectively, and all the voltages between Ø and +1 volts will have their decimal

values between 128 and Ø respectively. Therefore, once the digitized numbers are read in by the computer, if one wants to recover the true measured voltages (gain corrected), one can use the following formula. Considering that VL represents the digitized value:

$$\text{true voltage} = [\ (\ 128 - VL\ )\ *\ 2.5\ /\ 128\ ]\ /\ \text{gain} \qquad (4.1)$$

Figure C.2 on page 144 shows the amplifier designed for the present work. Since the input is capacitatively coupled, only AC signals are amplified. The output is biased from the same power supply that is used to operate the amplifier. The amount of bias introduced at the output is controlled by the ratio of R^f to R, where R = R1 + R2. The design relationship for the inverting mode is given by (Reference 18):

$$V^{odc} = (\ R^f\ /\ R\ )\ *\ V^+ \qquad (4.2)$$

where V^{odc} is the output of the amplifier for $V^{in=Ø}$

R^f is the feedback resistor

R is the bias resistor

V^+ is the power supply voltage

A 6-volt dry-cell battery was used as power supply, in all the applications. If ultracritical measurements are to be carried out, one should build a regulated 6-volt DC power supply unit, possibly using the 9V AC voltage line available

on pins 1Ø and 11 of the User Port. A point to stress is how to calculate the value of R, to produce a +2.5 volts DC bias output with a 6V DC power supply. Using the equation (4.2), we can find the exact value for the bias resistor:

$$R = (R^f / V^{odc}) * V^+ \qquad (4.3)$$

with $V^+ = +6.Ø$, $V^{odc} = +2.5$, and $R^f = 1$ M ,

R = 2.4 M .

Since 2.4 megohm resistors are not standard, a one megohm resistor (R1) and a variable two-megohm resistor (R2) were mounted in series, and R2 was adjusted to give+2.5 volts at the output of the amplifier with $V^{in} = Ø$ volts.

The gain of the amplifier is given by the relationship:

$$gain = R^f / R^{in} \qquad (4.4)$$

For the given values, i.e. $R^{in} = 1ØØK$ and $R^f = 1M$, the gain equals 1Ø.

In case AC ripple voltages are present on the V^+ power supply (we did not encounter this problem), they will couple to the output with a gain of 1/2.

4.4) The software: VICMON

The software developed for data acquisition using the analog-to-digital converter is VICMON. The present program is called VICMON because it is written for the VIC-2Ø computer and monitors all activated channels to sense and detect the incoming signals that meet the characteristics specified by the user. This is a 3.5K program, written entirely in machine code. This was done to save memory space and to avoid any interference with the memory added to store data. The program was developed on the Commodore 64 computer, using the Develop-64 assembler. The assembled program was then transferred to the VIC-2Ø computer using the tape recorder, for testing and debugging.

When the program is run for the first time, the main menu offers the following five options: CONFIGURE, MONITOR, SAVE, PLOT and EXIT. The functions of each of the options are detailed below.

4.4.1) CONFIGURE

First one has to select the CONFIGURE option, to initialize a number of important variables:

1) BUFFER SIZE
2) NUMBER OF CHANNELS
3) SAMPLING RATE
4) THRESHOLD
5) DATE
6) TIME

The first item in the list is BUFFER SIZE. The size of the buffer to hold the digitized data must be chosen in blocks of 8K; that is the buffer may be 8, 16, 24 or 32K long. If values other than those mentioned are entered, the computer will not reject them, because no input checking code is implemented in the current version (version 2.Ø) and the program will store the wrong buffer size.

The second variable to set is the NUMBER OF CHANNELS that must be sampled. This number can range from one to sixteen, although in the actual configuration only the first eight channels can be physically activated, because the remaining eight channels have not been connected to the A/D converter chip. Channel number one is always channel INØ of the A/D converter; channel number two is IN1 and so on.

The next item in the list is the SAMPLING FREQUENCY or sampling rate. The number entered here will be the sampling rate in Hertz for all the selected channels, that is all of them are sampled at the same selected rate. This restriction did not create any problem in this work, but there are applications where one might need to sample a particular channel at a different rate. In such situations, one would need to resort to other schemes in order to build a multi-channel data acquisition system, such as devoting one microprocessor to sample every one or two channels. Alternatively, one could implement in hardware many of the tasks that the software program executes, such as executing the time delay between each READ and storing the digitized

data in memory. Such a system would undoubtedly be more flexible, but obviously would be more difficult to build. It would also be extremely difficult, or even impossible to implement a multi-tasking program that would sample each channel at a specified rate on a computer like the VIC-2Ø. The most important shortcoming to implementing an effective multitasking program in an application such as the present one, is the slow speed of the microprocessor compared to the more advanced 16- or 32-bit-based microcomputers on the market.

The fourth parameter in the list is the THRESHOLD. This is needed for the computer to know whether a "valid signal" is detected. In many applications, one can not foresee accurately when the desired signals will reach the detectors. In such situations, one way of distinguishing between the signal one wishes to measure and other undesired signals, (e.g. background noise), is to wait until the incoming signal reaches a pre-specified level of energy before the whole system is triggered and the signals are sampled. In all such applications, in the present work, the energy was simply considered to be the square of the amplitude, to account for positive and negative voltage amplitudes. The THRESHOLD is the level of energy specified by the operator, so that any signal below this level would be ignored by the monitoring apparatus, until a valid signal is detected. In this manner one avoids storing every signal appearing at the system inputs.

The 65Ø2 chip can only add and substract numbers. To calculate the energy of a signal at any point in time, one must multiply the sampled amplitude by itself. To do so, one could implement a multiplication routine in software, but that would be extremely impractical and time-consuming. Moreover, the analog-to-digital converter can only deal with positive voltages, therefore we have to redefine slightly the previous interpretation of the word THRESHOLD in the context of this work. In the discussion of section 4.3, on signal conditioning, it was explained that in the current design, negative voltages are represented by numbers between 129 and 255. The first thing to notice about this set of numbers is that they all have their most significant bit, i.e. bit 7, set to one (128 is 2 to the power of 7). By the same token, the positive voltages are represented by the set of numbers, Ø to 127, excluding zero volts which is converted to 128. These numbers have their most significant bit cleared. Since the A/D converter is linear and we have the same number of values representing positive and negative numbers, it is very simple to go from the binary representation of a negative number to its positive counterpart and vice versa. All we have to do is to flip the sign of that number. This is most easily done in 65Ø2 machine language by calculating the "two's complement" (see any book on machine language programming for an explanation) of that number. Here, the THRESHOLD variable should be set to an integer between 128 (Ø volts) and 255 (most negative

voltage one is to measure). Because of the linearity of the A/D chip, the symmetry about the middle value 128 (which in the present configuration corresponds to the voltage amplitude of zero volt) is preserved. In this manner, both positive and negative voltages that exceed the THRESHOLD level in their absolute value will trigger the system. To leave a safe margin for error in many applications, the program only considers a signal or a trigger as valid, if three consecutive sample data exceed the selected threshold.

In general, one should monitor every activated channel to search for the trigger. The way the code is presently written one has to devote one specialized channel to detect a "valid signal" and when detected, one samples all other channels as well. By slightly modifying the existing code, one could add the possibility of monitoring either the specialized channel, or all the activated channels. This somewhat useful feature will be added in future enhancements of the program.

To monitor, a 512-byte circular buffer is set up by the VICMON program starting at $2000 (8192). This buffer is continuously refreshed, until the system is triggered. The signal is then sampled and stored in the rest of the data buffer. Then the data in this circular buffer are re-arranged so that the beginning of the 512-byte area of memory contains whatever the computer READ before the trigger, usually noise, and the few bytes at the end of this section of memory hold the data representing the onset of the valid signal detected on the specialized channel. In

earthquake monitoring, one would generally set the system to trigger on the high-amplitude surface waves measured by the seismometers. However, the most important part of the record is the first arrival time corresponding to primary P-waves. Therefore, it is crucial that the record of the first arrivals contained in the circular buffer, not be lost. The specialized channel is channel one of the A/D converter and should exclusively be used for this purpose, whenever the current version of the VICMON program is running.

Two other variables need to be initialized. These are the DATE and the TIME. The TIME, accurate to Ø.Ø16 of a second, is kept internally by the software clock of the computer and updated at every interrupt. It therefore is important that the interrupts not be disabled. This does not affect the accurate time delay routine for timing the sampling rate, because TIMER 1 runs independently of system interrupts.

When the sampling process is over, the program stores all the above variables, that is the BUFFER SIZE, NUMBER OF CHANNELS, SAMPLING RATE, THRESHOLD, DATE AND TIME, along with the time the last sampled datum was READ by the computer, in the 32 bytes of memory, just below $2ØØØ (8192). These data along with the sampled points are then used to process all or portions of the stored signal.

4.4.2) MONITOR

Selecting the MONITOR option from the main menu activates the specialized triggering channel and upon the detection of a valid trigger signal, all channels are sampled. When the data buffer is filled, a message is issued by the system notifying the operator that the sampling process is over, and then it waits for further instructions.

4.4.3) SAVE

When SAVE is selected, the sampled data along with the 32-byte information buffer are SAVEd to tape, as one block of program file. The present version of the program supports tape SAVEs only. If disk input/output is required, this feature can easily be added at additional cost.

4.4.4) PLOT

When the PLOT option is chosen from the main menu, the VICMON sets up a high-resolution screen, and asks for the channel number for which the data are to be plotted. It then READs the data corresponding to the selected channel from the data buffer and plots them to the screen.

4.4.5) EXIT

If this option is selected, the VICMON program jumps to the KERNAL routine that executes a COLD START, thus resetting the computer and erasing the contents of RAM. To re-enter VICMON, it must be loaded again from tape.

CHAPTER 5: A/D APPLICATIONS.

5.1) Introduction

This chapter presents the tests and experiments carried out, in the field and in the laboratory, to evaluate the potential and performance of the A/D board. The field tests spanned a period of approximately three months, from early August to mid-November of 1986.

5.2) Applications

5.2.1) Preliminary tests

The first series of tests was carried out in the laboratory; these tests consisted of continuously digitizing a 50 Hz sine wave at different sampling rates. The plot in Figure 5.1a on page 64 shows a 50-Hz sine wave having a peak-to-peak amplitude of 1 volt, sampled at a rate of 2500 Hz. That is, one cycle of the sinusoid is approximated by 50 points. This yields a very smooth sine wave. The digitized sine wave was generated by a Hewlett Packard model 200CD sine wave generator and was directly applied to the input of the signal conditioner without any filtering. Figure 5.1b on the same page is the plot of a 51.5 Hz synthetic sine wave (generated by the computer) sampled at the same 2500 Hz rate. If one superimposes the synthetic sinusoid over the digitized sine wave, the correspondence is exact. The

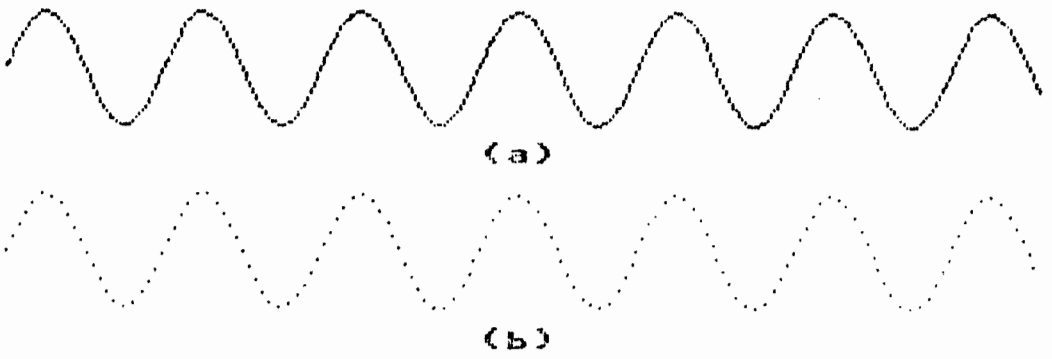


FIGURE 5.1: a) Reconstructed digitized sine wave (nominally 50 Hz), generated by a sine wave generator.

b) Matching computer generated sinusoid, having a frequency of 51.5 Hz.

(see text for details).

discrepancy in frequency, between the digitized sine wave and the synthetic one needed to match it, was found to be due entirely to the inaccurate output of the signal generator unit used. The frequency output of the generator needs to be re-adjusted, as was confirmed using a RACAL SA-52Ø digital frequency meter.

The A/D board was also tested using a vertical-type seismic exploration geophone having a resonant frequency of 45 Hz. The geophone output was amplified using the previously discussed LM39ØØ amplifier and then sent to the analog-to-digital converter. A series of taps was made on the laboratory bench and the amplified geophone output was digitized at the rate of one sample every 2 milliseconds, or 5ØØ Hz. The resulting data for one tap are shown in Figure 5.2 on page 66.

5.2.2) Digitization of analog seismic records

Under the direction of Professor Saull, David Lapierre (M.Sc., 1978) undertook the further development of an inexpensive seismic data recording system. He and Professor Saull used the system on the Island of Montreal to gather seismic data, using quarry blasts. Later, Professor Saull made additional measurements with the system in the interval Montreal-Mont Laurier. A large number of cassette tapes containing all these seismic data were provided by Dr. Saull. The principal objective in digitizing these records was to test and evaluate the performance of the A/D converter. The records that contained the most useful

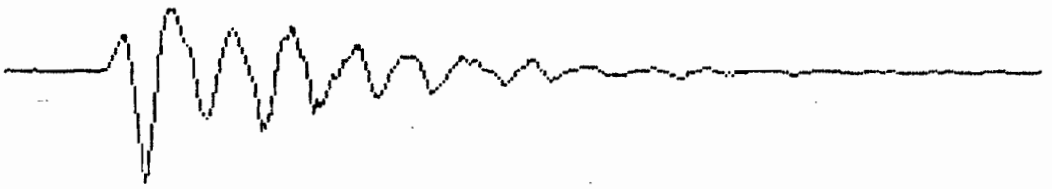


FIGURE 5.2: Response to a finger-tap of a vertical-type geophone, having a resonant frequency of 45 Hz. Record length: 0.64 seconds.

seismic information were singled out, by playing them and monitoring the output on an oscilloscope. A total of 35 records representing over 360K of data were digitized. In doing so, Lapierre's modified 2-channel tape recorder, along with the three stage amplifier designed specifically for his work, were used to extract the analog signals from the records. This analog signal, the output of the tape recorder, was then fed to the signal-conditioner circuit before it was routed to the analog-to-digital converter for sampling. The digital equivalent of the recorded analog signal may not be an accurate representation of the actual signal. We do not know whether the tape recorder used to record the signal ran at the same speed as the one used to play it back (the system that was used to record the quarry blast data often ran in very cold weather that slowed the tape drive). In that respect, there certainly is a slight distortion as far as the time index is concerned. Figures 5.3 to 5.6 show the plots of two of the seismic traces recorded from quarry blasts carried out on Montreal Island. Figures 5.3 and 5.5 show one seismic trace, divided into four parts due to lack of screen resolution. The August 16th 1978 record, obtained from a blast at Legendre, is particularly long. The data between the first trace and the second one, representing over 13 seconds, are not plotted. The January 14th 1977 record is from a blast at Francon quarry. It is 7.68 seconds long and Figure 5.3 shows all the information contained in the record.

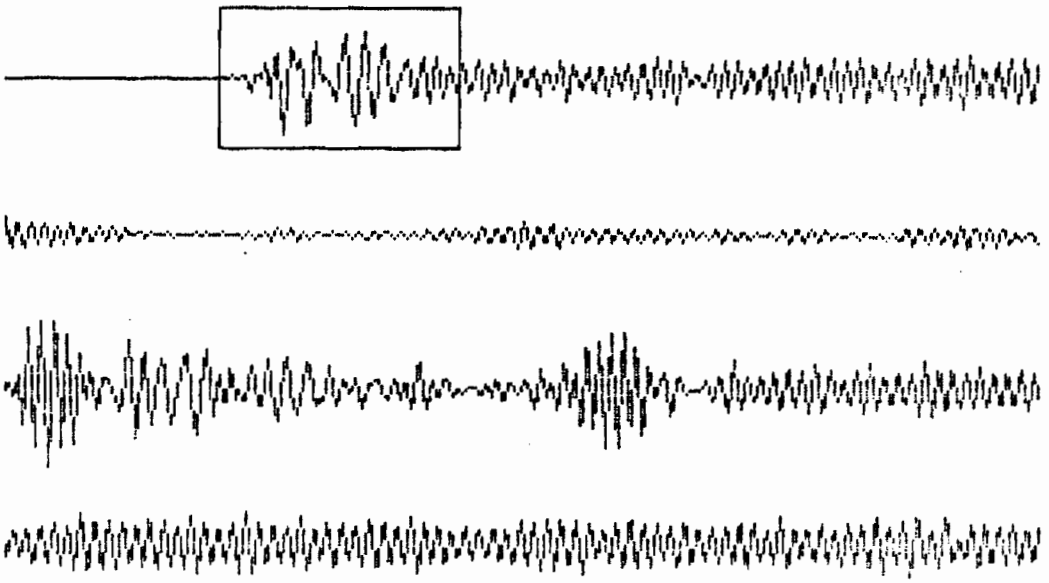


FIGURE 5.3: Reconstructed seismic trace recorded on January, 14th, 1977 at Francon Quarry. Record length: 7.68 seconds.

FIGURE 5.4: The framed seismic trace of FIGURE 5.3, plotted at three times its previous time scale and resolution.
Record length: 0.64 seconds.

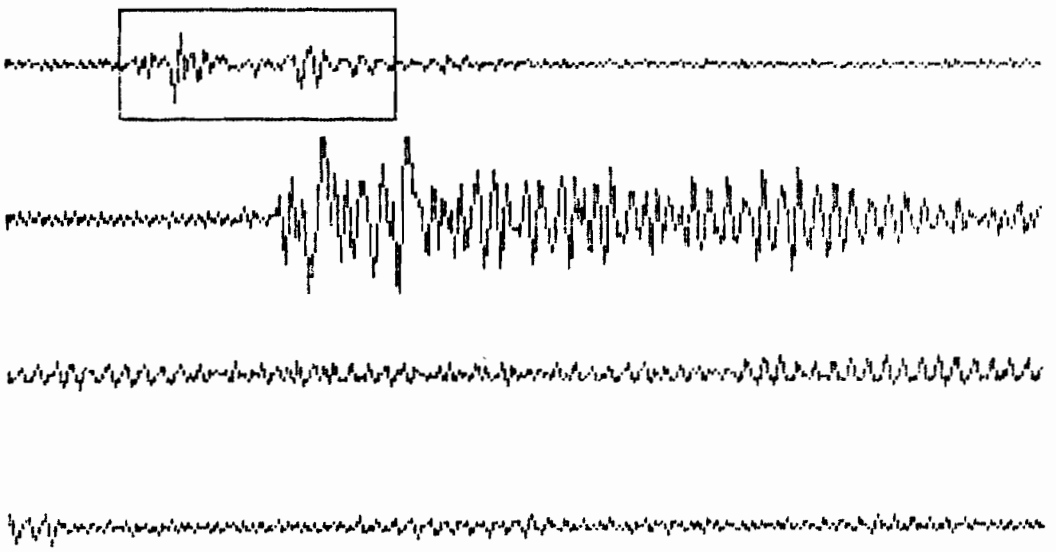


FIGURE 5.5: Reconstructed seismic trace recorded on August, 16th, 1978 at Legendre Quarry.
Record length: 13 seconds.

FIGURE 5.6: The framed seismic trace of FIGURE 5.5, plotted at three times its previous time scale and resolution. Record length: 0.64 seconds.

For comparison and processing purposes, these records can be "stretched" digitally to correct for the discrepancies in the time index. Benoy K. Ghose (Reference 7) has shown that one can stretch time series up to a certain degree (stretching factor < 2.5), without disturbing the data structure perceptibly, thus preserving its frequency content. Using this method of stretching, one could bring quarry records obtained at a given station from different quarry blasts, to the same time scale and then mix them, to get a better representation of the ground's impulse response at the recording site and more accurate reflection times. Stretching and mixing time series using analog devices alone is very impractical (V.A. Saull, personal communication, 1986).

Two quarry blast records, obtained on August 22nd 1978 are of particular interest. These were recorded close to the blast sites in Montreal North. Because of the very high degree of resemblance between the two records, the stretching technique was not used to mix the data. Instead, the two seismic traces were mixed by aligning the peaks of the main lobes, and the onset of the blast trace, and then adding the amplitudes. This produced the trace plotted in Figure 5.7 on page 73.

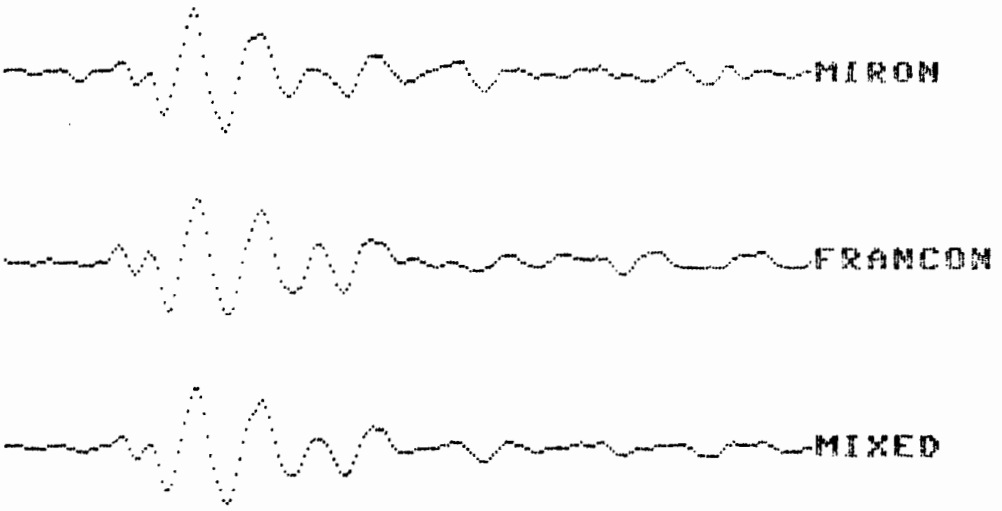


FIGURE 5.7: Blast records obtained on August, 22nd, 1978 at Miron and Francon Quarries. The third trace labelled MIXED, was obtained by averaging the Miron and Francon records.
Record Length: 0.64 seconds.

5.2.3) Field data

5.2.3a) Dropping weights

A series of tests was conducted in the West Island area of Montreal using dropping weights as seismic sources. One site selected was a football field on Rive-Boisée street in Pierrefonds. The transducer used in these tests was the L-4-3D, very low frequency, three directional seismometer, by MARK PRODUCTS Inc. This seismometer has a 1-Hz resonant frequency and measures the principal components of ground movement, namely the vertical, transversal, and longitudinal components. Before the signals ouput by the seismometer were fed to the analog-to-digital converter, they were amplified, using an amplifier provided by Professor O.G. Jensen, McGill University. This had been built specifically to operate with this seismometer. The signals were then transmitted using a long seismic cable over the length of the football field. Three channels were devoted to sampling and storing the vertical, transversal, and longitudinal components output by the seismometer. These traces were obtained by sampling each respective channel at the rate of one sample every 2 milliseconds or 500 Hz. Background noise at the Rive-Boisée football field was extremely low. The plots of the vertical, transversal, and longitudinal traces are shown in Figure 5.8 on page 75.

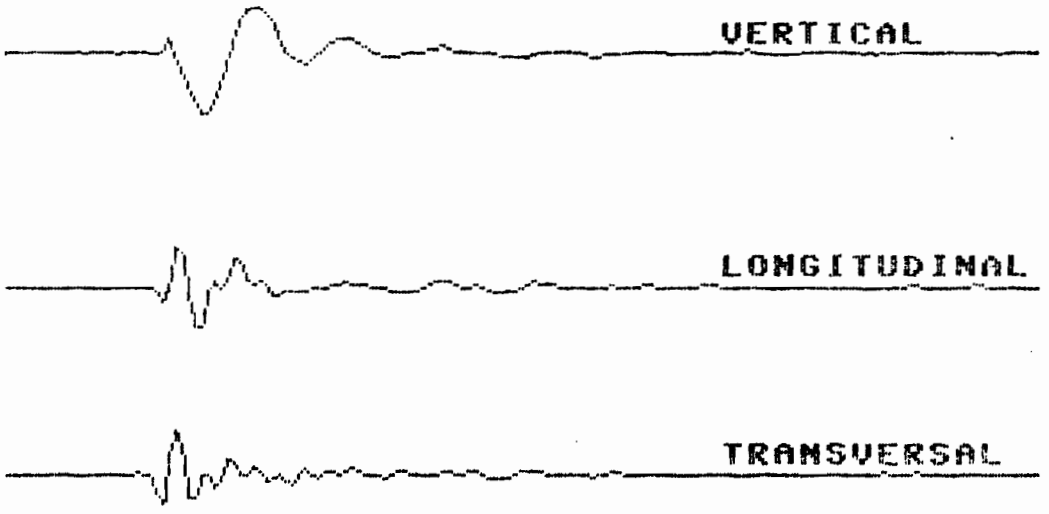


FIGURE 5.8: Response of the 1-Hz seismometer, to a 12-pound shot dropped near it, at Rive Boisee football field. Record length: 0.64 seconds.

5.2.3b) Quarry blasts

The construction work underway (Fall 1986) in downtown Montreal, necessitates the removal of a layer of hard limestone bedrock. Dynamitec Inc. is responsible for blasting at the construction site on St. Catherine street, about 400 meters from McGill University.

The blasting schedule was obtained from the employees working at the site. It rotated periodically from morning to late evening. The data acquisition system was set up in a room in the basement of the Frank Dawson Adams (F.D.A) building at Mc Gill university. Because of the building renovation on the campus, close to the F.D.A building, and the proximity of the room where the equipment was installed to University street, the system picked up a large number of false triggers during the day. To reduce this noise, it was decided to run the equipment only at night, and when the blasts were known to be scheduled. The blasts were scheduled to start sometime after 9:00 pm and continue at a rate of one blast every fifteen minutes. Neither the total number of blasts actually carried out nor the charge of each blast was made available precisely. From the information we were able to obtain at the construction site, it seems that a total of 30 to 40 explosions occured every evening, and that each time, roughly two pounds of dynamite were detonated. For two nights, the equipment monitored the blasting from 11:30 pm to 1:00 am and some interesting results were obtained. During this period a total of ten triggers were obtained. Of

these, we believe only two correspond to actual blasts. The remainder represent signals produced by vehicle traffic on University street or by masonry drilling within the building. One recording is of particular interest, because the time of explosion was recorded by the author at the blast site: 11:32 pm, October 24, 1986. This corresponds exactly to the time recorded by the computer for a valid trigger. This recorded signal resembles the trace extracted from the blast site tapes recorded on January 14th 1977, and shown in Figures 5.3 and 5.4. The plot of the actual seismic Dynamitec trace for the blast on October 24th 1986 and the Francon trace obtained on January 14nd 1977 are shown in Figure 5.9 on page 79.

The second seismic trace obtained during the night of october 24th 1986 is shown in Figure 5.10 on page 80. This trace may represent a blast, although it does not have any resemblance to the other records we have from blasts. This raises the question of discriminating or differentiating in an exact way, between quarry blast signals and other signals that might trigger the system. In general, if one knows exactly what is being sought, it is possible to construct a filter that would identify and record the desired signal and reject all others. The process of selecting such a signal, after it has been recorded is called "matched filtering". Knowing the exact shape, form and frequency content of a desired signal, one could design the inverse filter, so that when the recorded signal is convolved with the inverse filter, the result would be the delta function. One could

therefore pass the recorded signal through the inverse filter and find out whether the digitized signal is really what was sought. In case the answer is affirmative, the entire record is saved, otherwise the monitor is re-entered.

Matched filtering was not attempted, because the objective of this set of experiments was only to assess in a preliminary way the possibility of using the data acquisition system for monitoring. The way the VICMON software program is written reflects this point of view. The system is flexible enough for use in many monitoring applications where data are to be recorded over different channels.

Real-time processing of the digitized signals is not possible on a system such as the one we have built, because the VIC-2Ø computer was not designed to do data processing. In order to filter properly, one must be in possession of the complete record. This requires that one wait until the entire signal is digitized, then select the correct portion, and finally carry out the filtering process. If the code is written in BASIC, it would take too long to execute and while filtering data, other valid signals might be missed. Implementing the filtering portion of the code in machine language, to speed up the execution time would require more memory space than we currently have at our disposal.

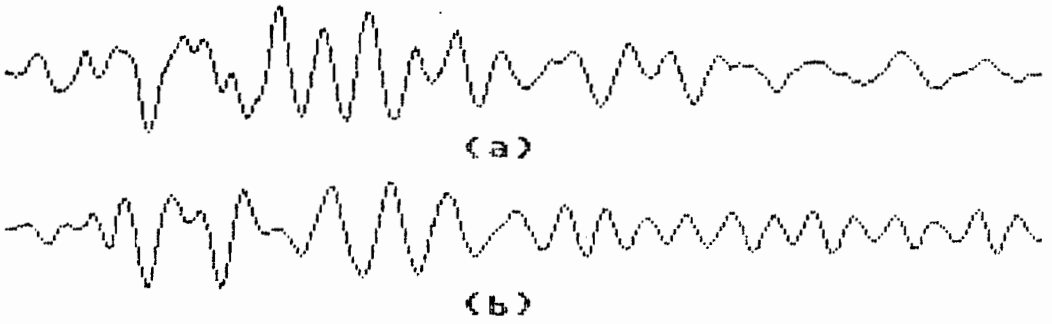


FIGURE 5.9: a) Trace obtained at McGill University, on October, 24th, 1986 from nearby construction blasts.
b) Trace of January, 14th, 1977 blast, recorded at Francon Quarry.

Record length: 0.64 seconds.

FIGURE 5.10: Trace recorded on October, 24th, 1986 at McGill University. This trace may be from construction blasts conducted in downtown Montreal; or from vehicular traffic noise.

Record length: 0.64 seconds.

CHAPTER 6: TELEMETRY.

6.1) Introduction

"Telemetry, as a name, designates a highly automated communications process, by which measurements are made and other data connected at remote or inaccessible points and transmitted to receiving equipment for monitoring, display and recording" (The New Encyclopaedia Britannica, 1981). The transmission may be done using connecting electrical or optical cables over the distance separating the measuring station and the receiving station. Alternatively, it could be done by radio or line-of-sight optical transmission, if for economical or other reasons, it becomes less practical to use optical or electrical cables. Obviously there are some advantages and disadvantages in using each of the above-mentioned methods. For instance, transmitting signals over cables is much easier, simply because the transmitting and the receiving stations will be directly connected together, thus avoiding a great amount of outside interference. However, one can not always use cables for data transmission (e.g. natural or man-made obstacles such as rough terrain or highways may be present). Although radio transmission is the least immune to noise, given a powerful transmitter one is able to send signals over much longer distances than practical for cables and at a fraction of the

cost. Optical transmission has the highest immunity to noise, and where the line of sight linking the transmitter and receiver is clear (no dust or smoke) it is practically noise-free.

6.2) Radio transmission

The principle behind radio transmission of data is simple; at least in concept. A radio telemetry system comprises a modulating circuit, a transmitter, a receiver and a demodulating circuit. The transmitter radiates a modulated high frequency carrier into space, as an electromagnetic wave, and the receiver captures and demodulates the signal, thus recovering the information sent by the transmitter.

Because radio signals are electromagnetic waves, they are a broad subset of the electromagnetic spectrum. The lowest frequencies used in radio communications are called VLF which stands for Very Low Frequency, and are in the lower tens of kilohertz. At the other end of the spectrum, radar applications use frequencies in the 30 gigahertz (30 E+9 Hz) and beyond. This range of frequencies is called SHF for Super High Frequency. In the lower regions of this range, that is slightly above 3 gigahertz, we find frequencies that are used in space and satellite communications.

In between these two extremes lies a very wide range of frequencies, divided into smaller ranges. Each of these subranges is reserved for a specific use, the choice of

which is governed by a number of factors. The most important of these is the propagation characteristics of the frequency range. The use of these available frequency ranges is tightly controlled by governments. There is, however, one unregulated frequency range, for general public use, called the Citizen's Band. This is a narrow frequency band around 27 megahertz, which is normally used in so-called "walkie talkies", for personal communication. For telemetry work, a narrow band above 450 megahertz is assigned exclusively to data transmission. To operate in this frequency range however, one needs to obtain a licence from the Federal government.

Page 170 in Appendix D shows the complete spectrum of the electromagnetic waves used in radio transmission, along with their limiting wavelengths and the principal services allocated.

6.3) Modulation

Modulation is the process whereby a particular property of the high frequency carrier is changed rapidly and continuously in time, in sympathy with a change in the voltage or the current of the signal to be transmitted. To convey information by radio, every piece of data must be converted into a voltage, called the modulating signal. This modulating signal could be derived from any one of a variety of sources: the human voice, wind, ground movement, or a digital counter.

There are several modulating techniques, three of which are especially common. The first is amplitude modulation or AM. In this case the modulating signal changes the peak amplitude voltage of the carrier. AM is commonly used in medium-wave broadcasting (carrier frequency 500 to 1600 kilohertz). The second method called FM, modulates the frequency of the carrier wave, that is the modulating signal changes the center frequency of the carrier within a pre-defined band. The center frequency is the frequency output when the modulating signal voltage is at zero volts.

A third method, exclusively used for data transmission is pulse-code modulation or PCM. In this, each sample is represented by a set of seven or more pulses (or spaces) that represent a binary code for the sample amplitude. This is a far better technique than the two previously mentioned methods, in terms of immunity to noise. However, the immunity to noise is achieved at the expense of higher pulse repetition and greater bandwidth, two reasons why it is not used all the time.

6.4) Demodulation

Demodulation is the process whereby the modulated high frequency carrier is passed through an electronic circuit to extract the information it carries. The signal captured at the receiving end of the radio system is not as strong as when it leaves the transmitter and must be amplified. After amplification, the signal is passed through a bandpass filter to discard all the unwanted frequencies picked up by

the receiver along the path of the transmitted signal. Further amplification may be required, depending on the type of application at hand.

In recovering an AM signal, the demodulation circuit integrates and stores the peak voltage of the carrier at every instant in time. This, in fact, produces the envelope of the carrier, which almost always contains a number of the carrier frequency harmonics. The envelope is then fed to a low-pass filter to further clean up the signal. Most circuits, at this stage, reproduce the positive DC copy of the modulating signal, which may or may not be desired. The average DC component of the signal can easily be removed, by passing the signal through a capacitor mounted in series.

The task of detecting an FM signal is somewhat more straightforward. Here, one can use either of the following two methods for demodulating the signal. First, a frequency-to-voltage converter (F/V) can be used. Most if not all the F/V converters make use of a phase-locked loop circuit (PLL). In using this method, the carrier is compared with a fixed reference clock, to recover the modulating signal's voltage. A different method, which in essence does the same thing, could use a frequency counter circuit. The circuit must have a reference clock with a frequency at least equal to the highest frequency contained in the carrier (see Figure D.3 on page 171). This way, one counts the number of pulses accumulated, for every cycle of the modulated carrier. By calibrating the system one can convert the

number of pulses into corresponding voltages later on.

In pulse code modulation, because data are transmitted bit by bit, using only two frequencies, (one to represent bit zero and the other bit one), the coded signal is easily detected and decoded accurately. Here, because of the nature of the signal and the system, the margin of error is very small.

6.5) Selection of the transmission technique

6.5.1) Amplitude Modulation

The possibility of transmitting data using Amplitude Modulation was investigated, but no serious effort was made to integrate AM as part of the system. The MC1495G balanced modulator-demodulator marketed by Motorola was tested in particular. The circuit built with this chip needed very fine tuning, but provided good linearity for inputs between zero and one volt. In future expansions of this system, further studies should be undertaken to determine the feasibility of AM data transmission.

Amplitude Modulation in data transmission is most commonly used in optical transmission (using fibre optics, visible light, or even infra-red transmission). Reference 2 in the Bibliography presents more information on infra-red transmission using IC chips designed for this purpose.

6.5.2) Pulse-Code Modulation

This technique requires that the digitized data be translated into a series of binary numbers before

transmission. The system would then use only two frequencies: one to represent the bit value one and the other for the bit value zero. This method is similar to that used in data transmission over a modem. Therefore, an additional computer would be required at the transmission end to operate the system. For this reason, PCM was not attempted in the present work.

6.5.3) Frequency modulation

Frequency modulation was considered to be the most suitable technique to use because of the variety of voltage-to-frequency IC chips and circuits available. In general, voltage-to-frequency converters offer some advantages over analog-to-digital converters, such as:

1) they are less expensive than the A/D chips;
2) continuous frequency variation is simple to implement in a digital system;
3) the analogue signal being sampled is automatically averaged over the counting period;

Therefore, in the present work Frequency Modulation was selected as the method to be tested for sending information by radio. The CMOS 4046 Phase-Locked Loop (PLL) was selected as the IC chip to be used for FM transmission.

6.6) The CMOS 4046 chip

The CMOS 4046 Phase Locked Loop (PLL) is probably the most versatile IC chip for PLL experimentation on the market. It contains two phase comparators, one Voltage Controlled Oscillator (VCO), one source follower, and a zener diode. The block diagram of this chip is shown on page 172 in Appendix D. Among the 4046 PLL features, one can mention the following:

1) ultra-low power drain;
2) VCO frequency setting using one resistor and one capacitor only;
3) frequency offset capability with only one resistor;
4) 50% duty cycle;
5) high maximum frequency (slightly greater than 1 megahertz);
6) linear frequency modulation within a limited range of input voltage;
7) high impedance control input.

The voltage-controlled oscillator is the most important part of the PLL circuit. To set the operating frequency of the VCO, one needs only to select the correct values for the resistor and the capacitor. For detailed information on the design equations and how the chip is used, see paragraph D.1) in Appendix D.

In this work, the 4046's internal VCO was used to convert transducer signal voltages into frequencies that

would be transmitted. The input of the VCO is modulated by the LM3900 operational amplifier, and the output of this op-amp swings between Vss and Vdd minus one volts, as already described in section 4.3 of Chapter 4. Because a six-volt dry-cell battery was used throughout the experiments, the output voltage was conditioned between 0 and +5 volts DC. The amplifier operated in the inverting mode, therefore all the discussions of paragraph 4.3 in Chapter 4 still apply.

In order to get the best possible performance out of the VCO, all the 4046 inputs must be connected to ground. This fact was discovered when experimenting with the chip. If one does not ground the inputs, the output frequency may lock into harmonics of the center frequency (see paragraph D.1 of Appendix D for further details).

There is a fairly serious problem regarding the linearity of the VCO. The VCO is linear for a small input voltage range between 2 and 3 volts, if a 5-volt power supply is used, but over the whole range, it is not linear. The situation gets worse when the input voltage falls below 1 volt: many of the chips tested in the laboratory failed to change their output frequency signal at all as the input voltage was decreased toward zero volt. For this reason, calibrating the VCO is extremely critical for faithful recovery of the modulated signal. Figure 6.1 on page103 shows the calibration curve, for the "best performing" chip that was calibrated, i.e. the chip that performed more linearly than others. The same highly non-linear

relationship is apparent when the input voltage is close to Vdd.

When this problem was discovered, a search was made to find better-performing chips. The Motorola 14433, and the Intersil 8053, were among those found. They utilize more elaborate VCO techniques, but they also have a very narrow ranges of input. Another chip (the Exar 8038 function generator), was specially tested, and provided excellent linearity over the entire input range. For a brief discussion of the Exar 8038 chip see paragraph D.2) on page 161. All these chips have one feature in common that makes them unattractive to use in this work: a narrow range of input (typically less than 2 volts when Vdd = 5 volts). Therefore because of time constraints, it was decided to abandon the idea of using other voltage-to-frequency converters and continue with the 4046 chip.

After the field work was completed, a paper by Q. Bristow was obtained (Reference 1) in which a system for the digital transmission of IP (induced polarization) data is presented. The system is based on a linear voltage-to-frequency converter with a wide range of input voltages. This IC chip, the DC537, could be a suitable replacement for the 4046 PLL used in the present work.

The output of the 4046's VCO is a square wave. This is excellent for the system we have designed, when used in the direct mode, that is when data are transmitted over a cable link. However, to transmit a signal via radio, the modulating signal must be a sinusoid: direct coupling of a

square wave with a sinusoidal carrier introduces undesirable harmonic frequencies into the transmitted signal. As an expedient, it was decided to round off the sharp corners of the square wave by shunting the signal by a capacitor before sending it to the transmitter. In future work however, the 4046 should be replaced by a voltage-to-frequency converter capable of producing sine waves only.

The last part in this section deals with the rest of the CMOS phase-locked loop. The purpose of using a PLL is to bring out frequencies hidden in a signal. As mentioned earlier, there are two phase detectors in this chip. Most often, phase comparator number one is used, because of its high immunity to noise. The phase comparator detects the "error" between the input signal phase and the phase of the VCO signal. Thus, the output of the comparator is a voltage that represents the phase difference between the input and the VCO ouput signal. It decreases when the phase difference decreases, and increases when the phase difference increases. In turn, this "error signal" is filtered, using a low-pass filter, and used to control the frequency of the voltage-controlled-oscillator by applying it directly to the VCO input. The reason for filtering is that the output voltage of the phase detector is not a DC voltage, but rather is composed of a complex series of pulses with varying widths. Since it is not possible to feed these pulses back to the VCO's input directly, the low-pass filter is used to recover an average DC voltage.

Further details regarding the operation of the PLL will not be given here, because a different scheme was used in this work for FM demodulation. The reason for using a different technique is that the PLL circuit for demodulating FM signals, similar to that shown in Figure D.4 on page 172, did not perform very well in trials. We were able to recover the modulating signal, but with a degree of accuracy that in our view was not satisfactory for use in a telemetry system. The circuit's poor performance may be attributed to a number of factors, such as the following:

1) The harmonic-sensitive VCO, when phase comparator one is used.

2) The input signal and the comparator input must be symmetric square wave signals, i.e. they must have a 50% duty cycle. The VCO does output a 50% duty cycle cycle, therefore when experimenting with the phase comparator number one, one has only to be concerned with the symmetry of the input signal.

3) The small tracking range of phase detector one which could hardly be extended to beyond 30 percent.

Phase comparator two has a number of significant advantages with regard to the points just mentioned, such as wide frequency range, and a VCO insensitive to harmonics of the center frequency. However, it has very poor immunity to noise. Therefore, for accurate demodulation applications, this comparator should not be used.

For these reasons, a different demodulation technique was selected. This technique has the advantage of using few

analog circuits, and therefore is most suitable for interfacing with a computer. Instead of demodulating the FM signal in hardware and then digitizing it, a frequency counter is used to measure one period of the modulated carrier. The value thus obtained gives the voltage amplitude during the period measured. The sampled signal is reconstructed later in software, from the calibrated VCO data.

6.7) Frequency counter

It was stated in section 2.3.2, without explanation, that the VIA #1's second timer was not used. This TIMER 2 of the VIA #1 consists of two eight-bit registers. Each one serves both as the counter and as the latch register. Therefore, the TIMER 2 low-order counter and LSB latch are both located at the same address, namely $9118 (37144). The TIMER 2 most-significant-byte for the counter and the latch register is found at $9119 (37145). The selection mode and the sequence of initialization of this timer are more or less similar to that of TIMER 1, as explained in section 2.3.2 in Chapter 2. Detailed descriptions of the timer's characteristics are given in References 5 and 6 in the Bibliography. There are two distinct differences between TIMER 2 and TIMER 1. When TIMER 1's count registers reach zero, the values from the latch registers are reloaded into the count registers and the countdown resumes at the rate of the system clock. In the case of TIMER 2, when the count

expires, the counter (a 16-bit counter), rolls over and starts the countdown from $FFFF (65535). In that respect TIMER 1 is more flexible by allowing us to change the values in the registers. The advantage of TIMER 2 is that it can be set to count pulses appearing on the User Port, from an external device. When the counter is set to operate in that mode, it does not count up as one would normally imagine. Rather, the program must initialize the counter to the desired number of counts and then the counter counts down from the initial value, every time a negative pulse is detected on PB6 of the User Port. This feature can be useful in many applications, such as in telecommunications using a modem or in interfacing parallel printers using the User Port. For these reasons, TIMER 2 was left unused for possible future expansions of the system.

Facing the problem of not having a general-purpose counter that would count normal pulses, (and not merely negative pulses), it was decided to build one. To do so, four 74LS161, 4-bit counters were assembled on the main interface board along with the analog-to-digital converter circuit. This gave a 16-bit counter that would be able to count pulses coming from almost any device. The counter also has a RESET option which can be selected in software. Paragraph D.3) in Appendix D, provides all the details for the frequency counter interface with the User Port of the computer.

The 16-bit general purpose counter lacks one important feature, which makes it undesirable to use in every

situation: input latching. Without latching, when we wish to READ the counter under computer control, occasionally, we may READ the wrong value. An example will clarify this point. Suppose the most significant byte of the counter holds the value 20 and the least significant byte the value 255. The actual number stored in the counter is 20*256 + 255 = 5375. Suppose the computer is instructed to READ the counter, starting with the most significant byte. The number 20 is READ, and stored somewhere in memory. At the same time, suppose a new pulse arrives at the input of the counter. The counter is incremented and the value it then holds is 5376. This corresponds to the number 21 in the most significant byte and the number 0 in the least significant byte of the counter. Now the computer READs the low-order byte of the counter, which contains a zero, and it stores the number in memory. The value just READ by the computer is then 20*256 + 0 = 5120 instead of 5375. Latching prevents this kind of mistake by retaining the value in the counter's least and most significant bytes, at the very moment a READ is done from one of its registers. Meanwhile the counter keeps updating its contents at the input frequency rate. When the READ is completed the latch registers update their values with the current values in the counter's registers.

The way the frequency counter is designed and programmed takes care of this potential problem automatically. The principal reason that the latch feature was not implemented, is that the interface board was too

small. The latch IC chips must be on the same board as the counter to ensure portability and convenience. In future work, the entire circuit for the analog-to-digital converter and the frequency counter, including the counter and its corresponding latch registers would be built on one board.

A frequency counter, as opposed to a frequency meter, gives the number of pulses counted during a fixed period of time. The basic circuit for a frequency counter must include a counter, a reference clock with a frequency at least equal to the highest frequency component within the signal being sampled, and some way of defining the correct time interval for each measurement. The counter may be 16 bits (or more). The reference clock should be extremely precise and stable, because the performance and the behavior of this clock are crucial to the ultimate accuracy of the frequency counter. Therefore, one should use a crystal clock for this purpose. For the project we used the crystal clock circuit given in Reference 12 in the Bibliography. The circuit uses only half of the 4001 quad NOR gate, two resistors, two capacitors, and the crystal.

The time interval needed to clock the transmitted signal is provided by the incoming pulses themselves. Every square pulse has a different period, which reflects the average voltage amplitude of the modulating signal over the period. Measuring this time interval allows one to recover the original signal. The description of how the time intervals are measured is given in paragraph D.4 in Appendix D.

The circuit designed for telemetry work, in this project, makes use of TTL and CMOS IC chips that are widely available. The design itself is a simple, yet very accurate frequency counter. Alternatively, entire frequency counters are now available on single chips, that could be assembled and used with fewer components. Intersil 7208 is one of these more advanced chips. The Reference 12 in the Bibliography gives all the details needed for building a frequency counter based on this chip. This is a seven-decade latched and multiplexed frequency counter with direct digit and display drive. It requires the Intersil 7207 time base chip as the reference clock of the frequency counter. These chips are not readily available and in Montreal must be ordered through Arrow Inc. Because the delivery period of the chip was several weeks, and more importantly, because our circuit performed very well, it was decided not to incorporate a more advanced design.

6.8) The Transmitter and Receiver

During the early stages of this project, two Radio Shack TRC-75 walkie talkies were used to transmit and receive data. These are 3-channel, 100 mW, Citizen's Band units. These radios are capable of transmitting voice over a distance of 500 meters or more, if used outside the city, in an area where the "airwaves" are quiet. The Citizen's Band of the radio frequency spectrum is around 27 megahertz (page 170 in Appendix D). Because these devices are for voice

communication, they are designed to transmit signals with frequencies in the audio range. To be able to transmit data, these radio were modified by cutting the microphone input and installing instead, a jack on the side of the plastic box, to serve as the input. The wires that connected the output of the microphone to the transmitting circuit are now tied to the jack, so that whenever the system is operated, the signal to be transmitted is connected to the jack via the proper adapter. At the other end, the received signal was displayed on an oscilloscope, using the earphone jack ouput, and the resulting signal was monitored on the oscilloscope. A one volt peak-to-peak sine wave from a function generator was input to the modified walkie talkie and the output was monitored to find the effective range of frequencies these walkie talkies can handle. It was found that between 1 and 4.5 kilohertz, the sine wave was faithfully reproduced.

The radios we have dealt with do not use FM modulation, but rather the amplitude of the carrier is modulated. If one selects a narrow band of audio frequencies, as we have, it is possible to transmit data from one radio to the other. The maximum distance separating the transmitting and receiving stations is primarily dependent on the power of the walkie talkies being used, and the amount of interference from other users and other devices.

In practice, the peak-to-peak voltage amplitude of the modulating signal need not to be as high as one volt. Laboratory measurements showed that the output amplitude of

the microphone in these devices is not more than few tenths of a volt. The modulating signal was scaled down to a little bit more that Ø.1 volt. After this conditioning, the signal was fed from the voltage-controlled oscillator of the 4Ø46 CMOS phase locked loop, which is set to operate between 125Ø Hz and 45ØØ Hz, for input voltages between Ø and 6 volts, to the transmitter. Because the amplifier used is the LM39ØØ, the output of the amplifier will swing between Ø and 5 volts, thus the upper limit for the VCO output frequency would be somewhat lower than 45ØØ Hz. Because the VCO is not linear over this range, one can not say what the upper limit will bé exactly, when a 5-volt signal is applied to the VCO's input, without calibration. In this particular case, the upper limit was found to be slightly above 44ØØ Hz. It was found that different 4Ø46 VCOs output different frequencies when the input range is held constant. Therefore, if for one reason or another the 4Ø46 chip one is working with becomes unusable, and it is replaced by another, one must recalibrate the new chip; the first step would be to adjust the resistors as shown in Figure D.4 on page 172, to reset the operating frequency of the VCO to the appropriate values.

Another issue that must be dealt with is the amount of overhead associated with the processing of each point, in relation to the over all delay required between each sample. In this case the "overhead" (see section 4.4.1 in Chapter 4 for an explanation) does not have a fixed value, as is the

case of the analog-to-digital converter. As explained in paragraph D.5) of Appendix D, this problem was solved by introducing an average value for calculating the sampling rate. This gave a maximum sampling rate of 2100 Hz.

If higher sampling frequencies are required, the basic system is quite able to accommodate them. The only problem lies with the radio system, because most walkie talkies do not allow frequencies above 5 kilohertz to be transmitted without distortion. Therefore the only practical solution would be to acquire a new radio system that could provide a wider range of frequencies.

The receiver circuit of the walkie talkie demodulates and filters the signal to bring it back to the audio frequency range and to recover the modulated signal. Filtering is required since the signal picked up by the antenna is somewhat corrupted, by the noise from other users or by natural interference. The recovered signal is fed from the earphone jack to an amplifier, built for this purpose around the LM3900, which further amplifies the signal to produce a square wave. The square wave is then passed through a 1-4.5 kilohertz band-pass filter. The signal is band-passed by first feeding it to a high-pass filter with a cut-off frequency of 1 kilohertz, and then a spike eliminator is used to stop all frequencies above 4.5 kilohertz. The definite advantage of the spike eliminator circuit is that, contrary to a low-pass filter where the transition region between the pass band and the stop band may be wide, it has an extremely sharp cut-off, simulating

an ideal low-pass filter. The circuit diagrams for the high-pass filter and the spike eliminator are shown in Figures D.5 and D.6 on pages 173 and 174. During the initial testing of the frequency counter circuit, it was found that a second stage of filtering enhanced the quality of the signal and provided more accurate results. After filtering, the signal is sent to the frequency counter for measurement. As will be discussed in the next paragraph, this scheme of demodulation offers satisfactory results in the laboratory, and under certain conditions, the data obtained in the field are equally good.

During field work, or when the distance separating the two radios becomes more than about 20 meters, the best results were obtained by setting the volume gain of the receiver to its maximum. Turning up the volume of the transmitter will not have any affect in this case, therefore all one needs is to have the radio switched on.

As was discovered during field tests, the range of our 100 mW walkie talkie is not great. In the field, reliable results were obtained at a maximum distance of 45 meters. Beyond this distance, the data become so corrupted with noise that it is impossible to recover the true signal. Subsequently, a second pair of walkie talkies was used: the model T606 by Fanon Corporation. This 6-channel, 1 W walkie talkie greatly improved the transmission range; however, it did not in general provide the expected results. Under special circumstances it does perform well, and we obtained

a considerable quantity of data with it.

Detailed descriptions of radio performance and the data obtained are given in the section on Field Work.

6.9) The software: VICTM

VICTeleMetry (VICTM) software is built on the same basic subroutines developed for the VICMON program. The only major change is in the sampling subroutine, where because of the hardware design and characteristics, it was necessary to rewrite many portions of the code. One other important difference stems from the fact that the VCO, over the range 0 to +5 volts, does not have a linear output. Therefore, recovering the original voltage values is not a simple task, as in the case of the analog-to-digital converter. To do this, the PLOT option is replaced by a PRINT option, where the user can actually have access to the raw data stored in the memory buffer.

Calibrating each 4046 is necessary for the accurate recovery of the transmitted data set. The calibration curve of the 4046 actually used, is shown in Figure 6.1 on page 103. What we have done is to fit a polynomial of degree six to the calibration data. The plot of the polynomial function for the same input, as obtained from the frequency counter isshown in Figure 6.2 on page 104. For this sixth degree polynomial, a goodness-of-fit (chi squared test) of better than 0.997 was obtained. Programming a sixth degree polynomial in machine language and calculating the answer for every data point is not a difficult task, because the

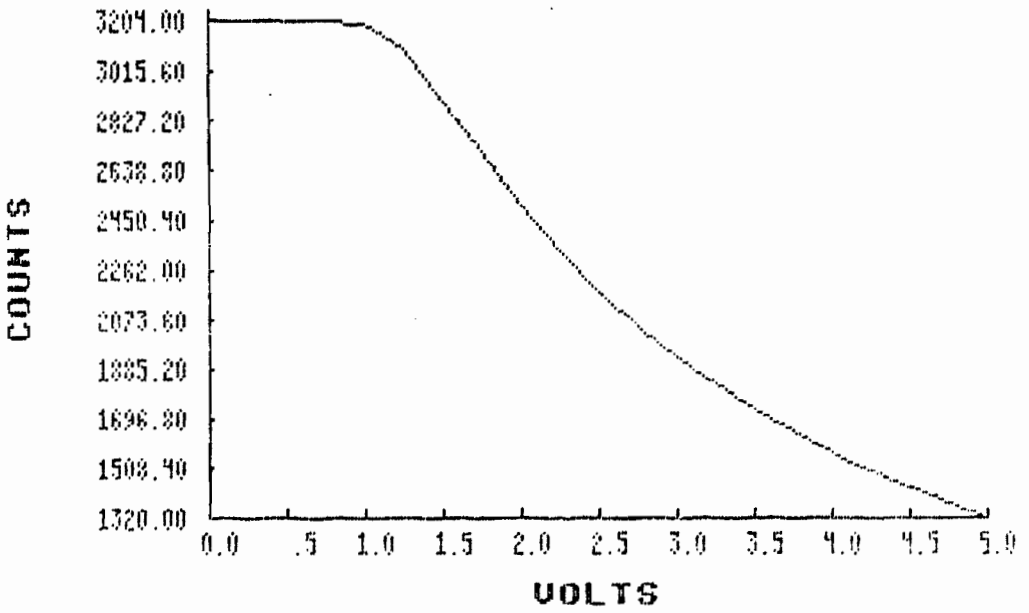


FIGURE 6.1: The calibration curve for the 4046 CMOS Phase-Locked Loop.

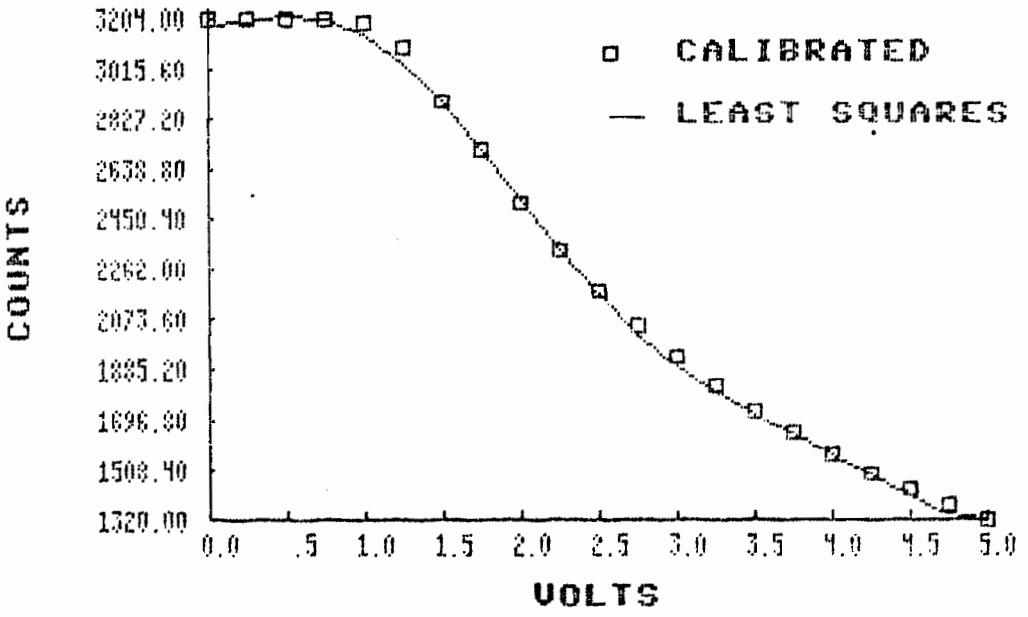


FIGURE 6.2: Plot of the calibrated VCO data shown in FIGURE 6.1, and the least-squares curve that fitted them.

VIC BASIC has all the necessary evaluation routines for this type of floating point arithmetic calculation. This feature of the system could use a machine language program to speed up the calculation time in evaluating a polynomial of any order. This was not done, because the subroutine that would be responsible for doing the calculations must fit with the rest of the program in the memory space below that assigned to the high resolution screen. This would require rewriting some of the other subroutines in a more compact fashion, and this was not possible within the time available.

Instead, a short BASIC program was written to do only the plotting. This program (VICTM.PLT) uses some of the machine code subroutines developed for VICMON. The BASIC portion of the program simply evaluates the polynomial for the given input.

The CONFIGURE subroutine is made shorter, in comparison with the VICMON program, mainly because we do not have to deal with the same number of parameters. The only relevant parameters are the BUFFER SIZE, and the SAMPLING RATE.

In future development of the interface board, after a more accurate VCO has been built, the sampling subroutine of the program should be upgraded to include the monitoring feature of the VICMON program. In this way, one would not have to be in constant communication with the person at the transmitting station, to inquire when data is to be sent and when receiving can be stopped, which is required, with the present configuration.

CHAPTER 7: TELEMETRY APPLICATIONS.

7.1) Introduction

The objective in the following series of tests was to evaluate the performance of the telemetry circuit by transmitting data over cable links and Citizen's Band radios. Although difficulties such as radio interference from other sources (e.g. private individuals) using Citizen's Band radios were anticipated at the beginning of this project, it was nonetheless decided to pursue the work to assess the use of this easily available frequency band for data transmission. The work was carried out from early August to mid-November of 1986. The sites of the field tests were downtown Montreal and the Rive-Boisée football field in the West Island area of Montreal.

7.2) Applications

7.2.1) Direct measurements

7.2.1a) Laboratory tests

In this series of tests, the pulses generated by the VCO were directly sent to the frequency counter circuit by cable. A series of sine waves, from a laboratory oscillator, were converted to evaluate the performance of the circuit. These sine waves are shown in Figure 7.1 on page 107. Next,

FIGURE 7.1: Plot of the sine wave sampled: direct connection between the transmitter and receiver.

the response of a vertical geophone having a resonant frequency of 45 Hz was measured. The geophone was set up on the laboratory bench and a series of finger taps was made near it. The output of the geophone was amplified and scaled so that the signal would swing between Ø and +5 volts. The signal was then fed to the VCO. The measured signal for one tap is shown in Figure 7.2b on page 109.

7.2.1b) Field tests

A slightly different version of the laboratory tests was carried out on the Rive-Boisée football field. In these, the distance between the measuring station and the computer was increased to about the length of the football field. The data were sent over a long twisted pair of conductors connecting the two stations. The signal in this instance was the output of a specially-constructed sine wave generator, whose cicuit diagram is given on page 175 in Appendix D. It uses one 741 op-amp and standard resistors and capacitors. The frequency of the sine wave was 25 Hertz and it was sampledat the rate of 1000 Hz. The results were similar to those obtained in laboratory, that is there was excellent transmission and reproduction of the sine wave.

7.2.2) Appraisal of test data

Comparing the output of the geophone in the laboratory experiment as shown on page 109, to that of the analog-to-digital converter shown on page 66, their near-perfect similarity is evident (see Figure 7.2 on page109). Along

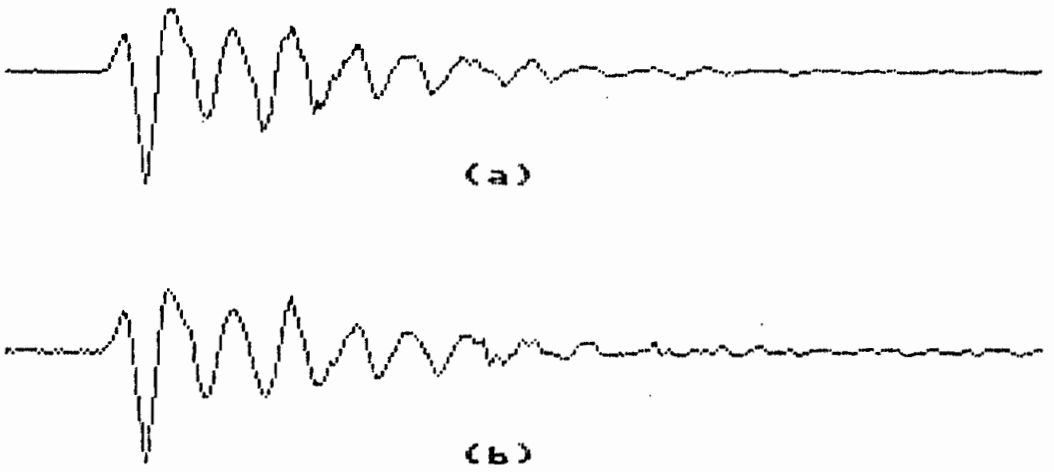


FIGURE 7.2: a) Response of the vertical-type geophone to a finger-tap. The trace was digitized using the A/D converter.
b) Response of the same geophone, recorded via the Telemetry Interface in the direct mode.
Record length: 0.64 seconds.

with the results obtained from the transmission of a sine wave over a cable, this confirmed that the circuit performs very well, and that it does not significantly distort the shape of an input signal.

7.2.3) Radio telemetry measurements

In the first phase of the radio telemetry measurements, a series of measurements was carried out in the laboratory over a distance of 10 meters separating the TRC-70 transmitter and receiver. The input signal was again the output of a vertical geophone having a resonant frequency of 45 Hz. The only problem encountered in this experiment was the presence of spurious data which we will refer to as spikes. The raw data for one of these tests are plotted in Figure 7.3a on page 111.As can be seen, these spikes are of equal amplitude, are spaced far from one another, and represent less than 10% of the total data READ by the computer. They can be removed from the record in software by replacing the bad data with the average of the two adjacent points. Although there are more advanced techniques of interpolating, such as polynomial curve fitting, this method was used because it is faster and in this case offers the same degree of accuracy. One should also note the output of the geophone compared to the one obtained in the direct mode experiment. The difference in the geophone's response is due to the fact that in order to obtain a separation of 10 meters for these experiments the geophone had to be set up

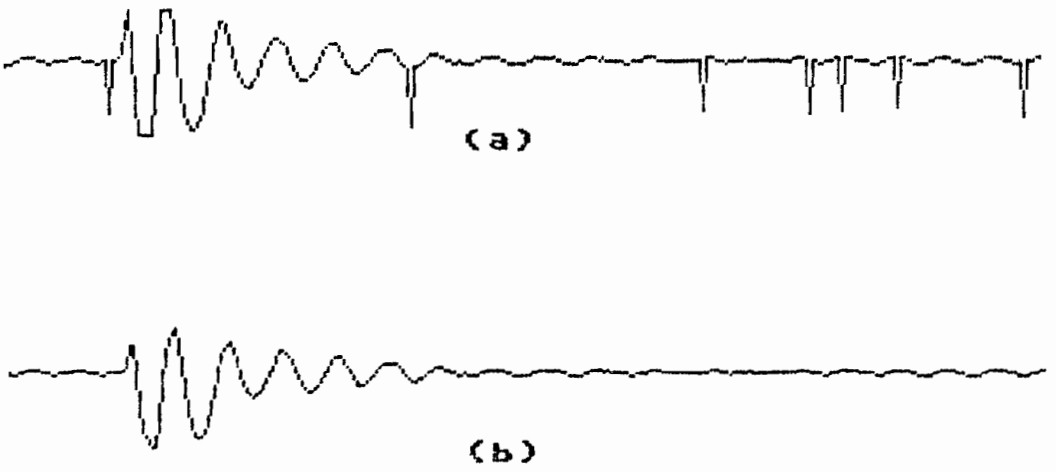


FIGURE 7.3: Response of the vertical-type geophone, transmitted via radio, over a distance of about 10 meters, and recorded using the Telemetry Interface.
a) Raw data.
b) Data corrected, by removing the spikes in software.
Record length: 0.64 seconds.

on a different table.

The same set of experiments was performed at Rive Boisée football field using the same radios and geophone. The geophone was placed on the football field, and five different sets of records were obtained. The signals were generated by stamping the ground near the geophone. For each test the distance between the receiving station and the transmitting station was increased by a factor of about two, starting at the edge of the football field. The first test was done at a distance of 15 meters, comparable to the distance between the two radios during the laboratory tests. The second transmission took place over a distance of 40 meters. The results from these two stations were identical and the data for one stamp at this station are shown in Figure 7.4. Note that in Figure 7.4 the raw data as READ by the computer are plotted. In Figure 7.5a the spikes have been removed in software and the data are plotted as a series of unconnected dots to show the difference between this trace and the one in Figure 7.5b. The trace shown in Figure 7.5b, is passed through a low-pass digital filter with a cut-off frequency of 105 Hz.

A distance of 40 meters is the limit at which the signal was received without any apparent loss of information. Beyond this range, the signal was corrupted to such a degree that the entire record looked like a series of random numbers. A typical record obtained at a distance of about 100 meters is shown in Figure 7.6 on page 115.

Considerable effort was employed to determine the

FIGURE 7.4: Response of the vertical-type geophone on Rive Boisée football field, transmitted via radio, over a distance of about 40 meters. Record length: 0.512 seconds.

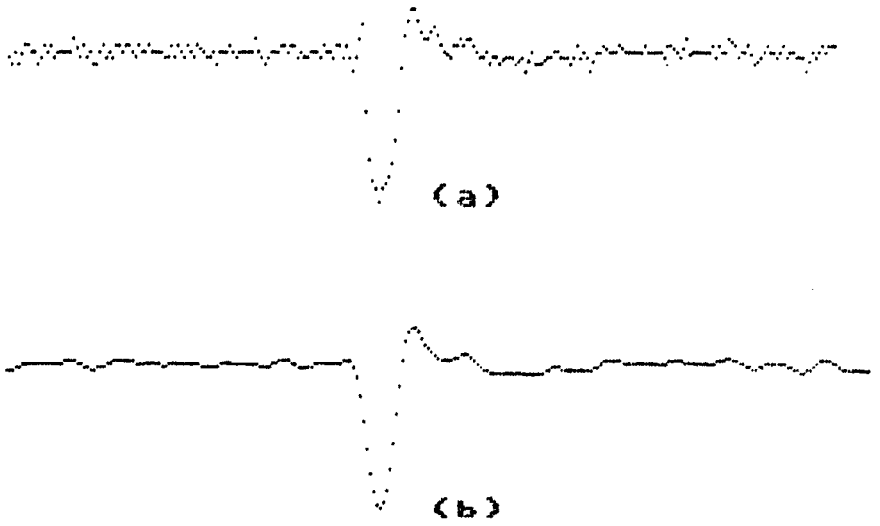


FIGURE 7.5: a) Software corrected data for the trace of FIGURE 7.4.
b) The trace a) passed through a digital low-pass filter, having a cut-off frequency of 105 Hz.
Record length: 0.512 seconds.

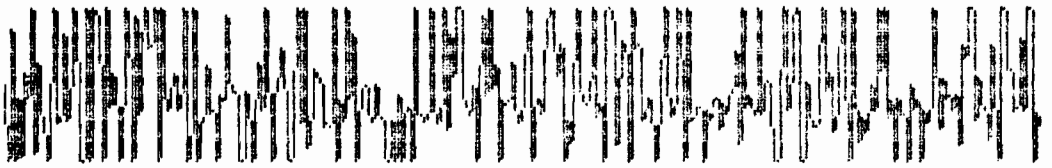


FIGURE 7.6: A sample of the radio-telemetered data obtained at a distance of about 100 meters, at Rive Boisée football field.

origin of the noise and to find ways to alleviate the problem. There are a number of reasons, which in our view, are responsible for the corruption of the transmitted signal. Most of the tests were done in an open field, at Rive Boisee. Although the test site is located outside Montreal, the area is not electromagnetically "quiet" and the volume of interference and noise was quite high. During every transmission, there was nearly constant CB traffic from different sources such as:

- private individuals
- Bell Canada technicians
- commercial trucks equipped with radio systems.

Moreover, most of the tests were done on one channel using a 27.355 megahertz crystal for the transmitter and a 26.9 megahertz crystal for the receiver. This turned out to be one of the most frequently-used Citizen's Band channels.

It was concluded, however, that the most important source of noise came from our system itself, specifically, the computer. That is, the VIC-20, or any computer for that matter, generates considerable RF noise when it is running. This is because of the large number of IC chips and circuits inside the computer. Moreover, the major chips in the computer that require an external clock to operate, such as the microprocessor, the two VIA chips and the VIC chip, are all driven by a 14.31818 megahertz crystal clock, which

irradiates some electromagnetic waves at that frequency. Remembering that the Citizen's Band lies near 27 megahertz in the radio frequency spectrum, we see that the carrier frequency of our Citizen's Band radio is close to the second harmonic of the computer's clock frequency. Since the receiving radio is close to the computer, and connected to the computer through the frequency counter circuit, the antenna could pick up the RF noise generated by the computer. Moreover, as the distance is increased between the two radios, the transmitted signal becomes weaker and more corrupted in comparison with the computer noise, and is ultimately overwhelmed by it. Because of the closeness of the two frequencies, i.e. the carrier frequency and the computer noise, it is very difficult to recover the desired information by filtering.

The problems of this type have been discussed by Tugal, D.A., Tugal, O., Reference 22. They emphasize that long distance high frequency radio transmission (i.e. frequencies from 3 to 30 megahertz) circuits rarely form part of a computer data transmission system, because the data error rate is extremely high and error detection and automatic retransmission are needed.

There are three possible approaches to solving this serious problem:

1) **Shielding:** this requires that one shield the computer, and every circuit and cable going in and out of the

computer, and also provide a solid ground for the entire system. This would require that special boxes be constructed for the equipment, using an electrically conductive material. This approach was tested in the field by placing the frequency counter circuit (not the receiving radio) in an iron container. The results were encouraging and indicate that shielding the entire system should prove to be an effective means for correcting the noise interference. The computer itself is the first thing that should be shielded, but this was not attempted.

2) **More powerful radio:** an alternative would be to use a more powerful radio. To examine the feasibility of this solution, the Fanon model T6Ø6, 1 W radio was used to transmit data. Because it is ten times more powerful than the previously used radio, we were able to transmit over a larger distance. However, when the same set of experiments was conducted in the field as before, the results were roughly the same; that is, the longest distance we were able to transmit without losing information was a little over 45 meters. The poor quality of data obtained in this set of experiments suggests that radio power has little to do with the problem.

An interesting dicovery was made when we tested the apparatus in downtown Montreal. The receiver was located in Room 3Ø8 of the F.D.A. building, while the transmitter was located in the back court between the F.D.A., the Macdonald

Harrington, and the McConnell buildings. The distance separating the transmitter and the receiver was about the length of a football field (i.e. approximately 120 meters). The signal transmitted was a 25-Hz sine wave generated by the circuit on page 175, and sampled at a rate of 1000 Hz. The results are plotted in Figure 7.7 on page 120. Notice that this sine wave is the signal picked up by the receiver, and sampled by the computer without providing any shielding. In this experiment, the success obtained in transmitting data over a distance of 120 meters, without any insertion of noise, is incompatible with the concept of computer RF interference discussed in the above paragraph. This shows that the computer is not the sole source of corruption. The entire length of the record was noise-free, and no spikes were present. The reason for such a faithful transmission and reception of the signal is thought to be that the path along which the signal travelled was surrounded by tall steel-frame buildings that helped to confine and shield the signal from noise and signals being aired by the CBC tower on Mount-Royal and by local Hospital transmitters. This experiment was carried out at different hours during the day and on different days, using both the Fanon and the Radio Shack radios. The results were similar: nearly noise-free transmission of the sine wave over a distance of 120 meters. We believe that under the same set of circumstances, using the Fanon radio system, the distance could be easily increased to twice this distance. To verify the hypothesis that these buildings helped in shielding the interference,

FIGURE 7.7: Raw data recorded by the computer, when a sine wave was transmitted via radio, over a distance of about 120 meters, in the back court of the F.D.A. building, McGill University.

the 1W transmitting apparatus was taken to the municipal reservoir, located between Pine, Peel and W. Penfield avenues. There, the equipment was not surrounded by nearby buildings and no shielding was provided against noise. Moreover, the line of sight is not clear between the reservoir and F.D.A. building. The results were convincing: the signal was corrupted just as the ones we obtained at Rive-Boisée.

The same series of tests was repeated, but the output of the receiver was recorded directly onto magnetic cassette tape. The tape was played back later, and the tape recorder output was amplified and filtered using the KROHN HITE Instrument CO's model 31C-AB variable band-pass filter. The signals displayed on the oscilloscope were similar to those recorded by the computer from the previous set of experiments.

Direct acoustic coupling between the radio transmitter microphone and the voltage-to-frequency converter output connected to a speaker was also attempted. This method did not produce any change in the quality of data obtained, compared to previous tests.

3) **Telemetry band:** the best way to eliminate interference would probably be to move to other bands in the radio spectrum; one such band at 450 megahertz, is dedicated exclusively to biomedical telemetry. This band would be free of personal communication, and should also ensure that the

computer noise would be less likely to corrupt the received signal, because the carrier frequency and the center frequency of the computer clock are spaced far apart from each other. To do this, one needs a transmitter and receiver capable of operating within this frequency range. Using this option, we feel, little or no special shielding would be required. However, this alternative needs to be tested, to confirm its feasibility.

CHAPTER 8: CONCLUSIONS AND RECOMMENDATIONS

The inexpensive data acquisition system built around the Commodore VIC-2Ø microcomputer is a portable unit that can be operated in the field as well as in the laboratory. The only addition made to the standard system is the memory expansion module which provides an extra 32K of Random Access Memory, used as buffer to hold digitized data.

The interface board comprises one analog-to-digital converter with 16-channel multiplex input, and one digital frequency counter circuit used to demodulate telemetered data.

In the current configuration, telemetered data reception takes place over one channel only, using the frequency modulation technique. The analog-to-digital converter however, accommodates a total of eight input channels. If more inputs are needed, one can easily provide the extra channels on the same interface board.

The various types of experiments carried out in this work, using the analog-to-digital converter, showed that this single chip data acquisition system can lend itself to a large number of applications. These include: simple waveform digitization in laboratory, event monitoring, and system control, although the latter was not the objective of the present work.

The telemetry circuit was used to transmit data over

cable links and inexpensive Citizen's Band radio. In the former case, the results were excellent: data were sent without any loss of information over the length of a football field. The quality of data obtained suggests that the distance separating the transmitter and receiver could easily be increased. Radio telemetry was not nearly as successful. However, we were able to transmit a sine wave via radio over a distance of about 120 meters, in a surrounded compound, where there was little interference. Under this special set of circumstances (low outside interference), Citizen's Band radio probably can be used to convey information over larger separations, although this needs to be investigated. The results show the feasibility of very short-range data transmission using inexpensive radio equipment, and acoustic FM.

Further investigation needs to be conducted with regard to the telemetry system. This should include the following:

1) The 4046 should be replaced with a linear phase-locked loop IC chip. The new chip must have a wide input range. The chip described in Reference 1 (the DC537) could prove a satisfactory device.
2) Using the new PLL chip, an attempt should be made to reconstruct the analogue voltage and subsequently to digitize the signal using the analog-to-digital converter. This would increase the sampling rate capability of the system, and introduce little or no

distortion in the sampled signal.

3) The entire system should be shielded, as discussed in Chapter 7, if the use of Citizen's Band radio is envisaged.

4) Use of the biomedical telemetry frequency band should be tested. This would necessitate acquisition of suitable radio equipment. It could prove to be the best solution, but would also be the most expensive.

5) Serious effort should be devoted to investigate the possibility of integrating AM transmission of data as part of the system. Because AM uses the carrier frequency only, to transmit data, one may be able to avoid spikes, present in the record, when FM is used.

APPENDIX A:

THE VIC-20 MEMORY MAPS

MEMORY MAPS

The following memory maps provide a guide which shows which special locations are set aside for use by the VIC's operating system . . . and what those locations are used for.

Memory Map

HEX	DECIMAL	DESCRIPTION
0000	0	Jump for USR
0001-0002	1-2	Vector for USR
0003-0004	'3-4	Float-Fixed vector
0005-0006	5-6	Fixed-Float vector
0007	7	Search character
0008	8	Scan-quotes flag
0009	9	TAB column save
000A	10	0 = LOAD, 1 = VERIFY
000B	11	Input buffer pointer/# subscript
000C	12	Default DIM flag
000D	13	Type: FF = string, 00 = numeric
000E	14	Type: 80 = integer, 00 = floating point
000F	15	DATA scan/LIST quote/memory flag
0010	16	Subscript/FNx flag
0011	17	0 = INPUT;$40 = GET;$98 = READ
0012	18	ATN sign/Comparison eval flag
0013	19	Current I/O prompt flag
*0014-0015	20-21	Integer value
0016	22	Pointer: temporary string stack
0017-0018	23-24	Last temp string vector
0019-0021	25-33	Stack for temporary strings
0022-0025	34-37	Utility pointer area
0026-002A	38-42	Product area for multiplication
*002B-002C	43-44	Pointer: Start of Basic
*002D-002E	45-46	Pointer: Start of Variables
*002F-0030	47-48	Pointer: Start of Arrays
*0031-0032	49-50	Pointer: End of Arrays
*0033-0034	51-52	Pointer: String storage (moving down)
0035-0036	53-54	Utility string pointer
*0037-0038	55-56	Pointer: Limit of memory
0039-003A	57-58	Current Basic line number
003B-003C	59-60	Previous Basic line number
003D-003E	61-62	Pointer: Basic statement for CONT
003F-0040	63-64	Current DATA line number
0041-0042	65-66	Current DATA address
*0043-0044	67-68	Input vector

* *Useful memory location*

HEX	DECIMAL	DESCRIPTION
0045-0045	69-70	Current variable name
0047-0048	71-72	Current variable address
0049-004A	73-74	Variable pointer for FOR/NEXT
004B-004C	75-76	Y-save; op-save; Basic pointer save
004D	77	Comparison symbol accumulator
004E-0053	78-83	Misc work area, pointers, etc
0054-0056	84-86	Jump vector for functions
0057-0060	87-96	Misc numeric work area
*0061	97	Accum#1: Exponent
*0062-0065	98-101	Accum#1: Mantissa
*0066	102	Accum#1: Sign
0067	103	Series evaluation constant pointer
0068	104	Accum#1 hi-order (overflow)
*0069-006E	105-110	Accum#2: Exponent, etc.
006F	111	Sign comparison, Acc#1 vs #2
0070	112	Accum#1 lo-order (rounding)
0071-0072	113-114	Cassette buffer length/Series pointer
*0073-008A	115-138	CHRGET subroutine (get BASIC char)
007A-007B	122-123	Basic pointer (within subroutine)
008B-008F	139-143	RND seed value
*0090	144	Status word ST
0091	145	Keyswitch PIA: STOP and RVS flags
0092	146	Timing constant for tape
0093	147	Load = 0, Verify = 1
0094	148	Serial output: deferred char flag
0095	149	Serial deferred character
0096	150	Tape EOT received
0097	151	Register save
*0098	152	How many open files
*0099	153	Input device (normally 0)
*009A	154	Output (CMD) device, normally 3
009B	155	Tape character parity
009C	156	Byte-received flag
009D	157	Direct = $80/RUN = 0 output control
009E	158	Tape Pass 1 error log/char buffer
009F	159	Tape Pass 2 error log corrected
*00A0-00A2	160-162	Jiffy Clock (HML)
00A3	163	Serial bit count/EOI flag
00A4	164	Cycle count
00A5	165	Countdown, tape write/bit count
00A6	166	Pointer: tape buffer
00A7	167	Tape Write ldr count/Read pass/inbit
00A8	168	Tape Write new byte/Read error/inbit cnt
00A9	169	Write start bit/Read bit err/stbit

* *Useful memory location*

HEX	DECIMAL	DESCRIPTION
00AA	170	Tape Scan;Cnt;Ld;End/byte assy
00AB	171	Write lead length/Rd checksum/parity
00AC-00AD	172-173	Pointer: tape buffer, scrolling
00AE-00AF	174-175	Tape end addresses/End of program
00B0-00B1	176-177	Tape timing constants
*00B2-00B3	178-179	Pointer: start of tape buffer
00B4	180	Tape timer (1 = enable); bit cnt
00B5	181	Tape EOT/RS-232 next bit to send
00B6	182	Read character error/outbyte buffer
*00B7	183	# characters in file name
*00B8	184	Current logical file
*00B9	185	Current secondary address
*00BA	186	Current device
*00BB-00BC	187-188	Pointer: to file name
00BD	189	Write shift word/Read input char
00BE	190	# blocks remaining to Write/Read
00BF	191	Serial word buffer
00C0	192	Tape motor interlock
00C1-00C2	193-194	I/O start addresses
00C3-00C4	195-196	KERNAL setup pointer
*00C5	197	Current key pressed
*00C6	198	# chars in keyboard buffer
*00C7	199	Screen reverse flag
00C8	200	Pointer: End-of-line for input
00C9-00CA	201-202	Input cursor log (row, column)
*00CB	203	Which key: 64 if no key
00CC	204	cursor enable (0 = flash cursor)
00CD	205	Cursor timing countdown
00CE	206	Character under cursor
00CF	207	Cursor in blink phase
00D0	208	Input from screen/from keyboard
*00D1-00D2	209-210	Pointer to screen line
*00D3	211	Position of cursor on above line
00D4	212	0 = direct cursor, else programmed
*00D5	213	Current screen line length
*00D6	214	Row where cursor lives
00D7	215	Last inkey/checksum/buffer
*00D8	216	# of INSERTs outstanding
*00D9-00F0	217-240	Screen line link table
00F1	241	Dummy screen link
00F2	242	Screen row marker
*00F3-00F4	243-244	Screen color pointer
00F5-00F6	245-246	Keyboard pointer
00F7-00F8	247-248	RS-232 Rcv pointer
00F9-00FA	249-250	RS-232 Tx pointer

* *Useful memory location*

HEX	DECIMAL	DESCRIPTION
*00FB-00FE	251-254	Operating system free zero page space
00FF	255	Basic storage
0100-010A	256-266	Floating to ASCII work area
0100-013E	256-318	Tape error log
0100-01FF	256-511	Processor stack area
*0200-0258	512-600	Basic input buffer
*0259-0262	601-610	Logical file table
*0263-026C	611-620	Device # table
*026D-0276	621-630	Secondary Address table
*0277-0280	631-640	Keyboard buffer
*0281-0282	641-642	Start of memory for op system
*0283-0284	643-644	Top of memory for op system
0285	645	Serial bus timeout flag
*0286	646	Current color code
0287	647	Color under cursor
*0288	648	Screen memory page
*0289	649	Max size of keyboard buffer
*028A	650	Key repeat (128 = repeat all keys)
*028B	651	Repeat speed counter
028C	652	Repeat delay counter
*028D	653	Keyboard Shift/Control flag
028E	654	Last keyboard shift pattern
028F-0290	655-656	Pointer: decode logic
*0291	657	Shift mode switch (0 = enabled, 128-locked)
0292	658	Auto scroll down flag (0 = on, <>0 = off)
0293	659	RS-232 control register
0294	660	RS-232 command register
0295-0296	661-662	Nonstandard (Bit time/2-100)
0297	663	RS-232 status register
0298	664	Number of bits to send
0299-029A	665-666	Baud rate (full) bit time
029B	667	RS-232 receive pointer
029C	668	RS-232 input pointer
029D	669	RS-232 transmit pointer
029E	670	RS-232 output pointer
029F-02A0	671-672	Holds IRQ during tape operations
02A1-02FF	673-767	Program indirects
*0300-0301	768-769	Error message link
0302-0303	770-771	Basic warm start link
0304-0305	772-773	Crunch Basic tokens link
0306-0307	774-775	Print tokens link
0308-0309	776-777	Start new Basic code link

* *Useful memory location*

HEX	DECIMAL	DESCRIPTION
030A-030B	778-779	Get arithmetic element link
030C	780	Storage for 6502 .A register
030D	781	Storage for 6502 .X register
030E	782	Storage for 6502 .Y register
030F	783	Storage for 6502 .P register
0310-0313	784-787	??
0314-0315	788-789	Hardware (IRQ) interrupt vector (EABF)
0316-0317	790-791	Break interrupt vector (FED2)
0318-0319	792-793	NMI interrupt vector (FEAD)
031A-031B	794-795	OPEN vector (F40A)
031C-031D	796-797	CLOSE vector (F34A)
031E-031F	798-799	Set-input vector (F2C7)
0320-0321	800-801	Set-output vector (F309)
0322-0323	802-803	Restore I/O vector (F3F3)
0324-0325	804-805	INPUT vector (F20E)
0326-0327	806-807	Output vector (F27A)
0328-0329	808-809	Test-STOP vector (F770)
032A-032B	810-811	GET vector (F1F5)
032C-032D	812-813	Abort I/O vector (F3EF)
032E-032F	814-815	user vector (FED2)
0330-0331	816-817	Link to load RAM (F549)
0332-0333	818-819	Link to save RAM (F685)
0334-033B	820-827	??
*033C-03FB	828-1019	Cassette buffer
0400-0FFF	1024-4095	3K expansion RAM area
1000-1DFF	4096-7679	User Basic area
1E00-1FFF	7680-8191	Screen memory
2000-3FFF	8192-16383	8K expansion RAM/ROM block 1
4000-5FFF	16384-24575	8K expansion RAM/ROM block 2
6000-7FFF	24576-32767	8K expansion RAM/ROM block 3

NOTE: When additional memory is added to block 1 (and 2 and 3), the KERNAL relocates the following things for BASIC:

1000-11FF	4096-4607	Screen memory
1200-?	4608-?	User Basic area
9400-95FF	37888 = 38399	Color RAM

8000-8FFF	32768-36863	4K Character generator ROM
8000-83FF	32768-33791	Upper case and graphics
8400-87FF	33792-33815	Reversed upper case and graphics
8800-8BFF	33816-35839	Upper and lower case
8C00-8FFF	35840-36863	Reversed upper and lower case
9000-93FF	36864-37887	I/O BLOCK O

* *Useful memory location*

HEX	DECIMAL	DESCRIPTION
9000-900F	36864-36879	Address of VIC chip registers
9000	36864	bits 0-6 horizontal centering bit 7 sets interlace scan
9001	36865	vertical centering
9002	36866	bits 0-6 set # of columns bit 7 is part of video matrix address
9003	36867	bits 1-6 set # of rows bit 0 sets 8 × 8 or 16 × 8 chars
9004	36868	TV raster beam line
9005	36869	bits 0-3 start of character memory (default = 0) bits 4-7 is rest of video address (default = F) BITS 3,2,1,0 CM starting address

		HEX	DEC
0000	ROM	8000	32768
0001		8400	33792
0010		8800	34816
0011		8C00	35840
1000	RAM	0000	0000
1001		xxxx	
1010		xxxx	unavail.
1011		xxxx	
1100		1000	4096
1101		1400	5120
1110		1800	6144
1111		1C00	7168

9006	36870	horizontal position of light pen
9007	36871	vertical position of light pen
9008	36872	Digitized value of paddle X
9009	36873	Digitized value of paddle Y
900A	36874	Frequency for oscillator 1 (low) (on: 128-255)
900B	36875	Frequency for oscillator 2 (medium) (on: 128-255)
900C	36876	Frequency for oscillator 3 (high) on: 128-255)
900D	36877	Frequency of noise source
900E	36878	bit 0-3 sets volume of all sound bits 4-7 are auxiliary color information
900F	36879	Screen and border color register bits 4-7 select background color bits 0-2 select border color bit 3 selects inverted or normal mode

HEX	DECIMAL	DESCRIPTION
9110-911F	37136-37151	6522 VIA#1
9110	37136	Port B output register (user port and RS-232 lines)

PIN ID	6522 ID	DESCRIPTION	EIA	ABV
C	PB0	Received data	(BB)	Sin
D	PB1	Request to Send	(CA)	RTS
E	PB2	Data terminal ready	(CD)	DTR
F	PB3	Ring indicator	(CE)	RI
H	PB4	Received line signal	(CF)	DCD
J	PB5	Unassigned	( )	XXX
K	PB6	Clear to send	(CB)	CTS
L	PB7	Data set ready	(CC)	DSR
B	CB1	Interrupt for Sin	(BB)	Sin
M	CB2	Transmitted data	(BA)	Sout
A	GND	Protective ground	(AA)	GND
N	GND	Signal ground	(AB)	GND

9111	37137	Port A output register (PA0) Bit 0 = Serial CLK IN (PA1) Bit 1 = Serial DATA IN (PA2) Bit 2 = Joy 0 (PA3) Bit 3 = Joy 1 (PA4) Bit 4 = Joy 2 (PA5) Bit 5 = Lightpen/Fire button (PA6) Bit 6 = Cassette switch sense (PA7) Bit 7 = Serial ATN out
9112	37138	Data direction register B
9113	37139	Data direction register A
9114	37140	Timer 1 low byte
9115	37141	Timer 1 high byte & counter
9116	37142	Timer 1 low byte
9117	37143	Timer 1 high byte
9118	37144	Timer 2 low byte
9119	37145	Timer 2 high byte
911A	37146	Shift register
911B	37147	Auxiliary control register
911C	37148	Peripheral control register (CA1, CA2, CB1, CB2) CA1 = restore key (Bit 0) CA2 = cassette motor control (Bits 1-3) CB1 = interrupt signal for received RS-232 data (Bit 4) CB2 = transmitted RS-232 data (Bits 5-7)
911D	37149	Interrupt flag register

HEX	DECIMAL	DESCRIPTION
911E	37150	Interrupt enable register
911F	37151	Port A (Sense cassette switch)
9120-912F	37152-37167	6522 VIA#2
9120	37152	Port B output register keyboard column scan (PB3) Bit 3 = cassette write line (PB7) Bit 7 = Joy 3
9121	37153	Port A output register keyboard row scan
9122	37154	Data direction register B
9123	37155	Data direction register A
9124	37156	Timer 1, low byte latch
9125	37157	Timer 1, high byte latch
9126	37158	Timer 1, low byte counter
9127	37159	Timer 1, high byte counter timer 1 is used for the 60 time/second interrupt
9128	37160	Timer 2, low byte latch
9129	37161	Timer 2, high byte latch
912A	37162	Shift register
912B	37163	Auxiliary control register
912C	37164	Peripheral control register CA1 Cassette read line (Bit 0) CA2 Serial clock out (Bits 1-3) CB1 Serial SRQ IN (Bit 4) CB2 Serial data out (Bits 5-7)
912D	37165	Interrupt flag register
912E	37166	Interrupt enable register
912F	37167	Port A output register
9400-95FF	37888-38399	location of COLOR RAM with additional RAM at blk 1
9600-97FF	38400-38911	Normal location of COLOR RAM
9800-9BFF	38912-39935	I/O block 2
9C00-9FFF	39936-40959	I/O block 3
A000-BFFF	40960-49152	8K decoded block for expansion ROM
C000-DFFF	49152-57343	8K Basic ROM
E000-FFFF	57344-65535	8K KERNAL ROM

APPENDIX B:

THE MEMORY EXPANSION MODULE

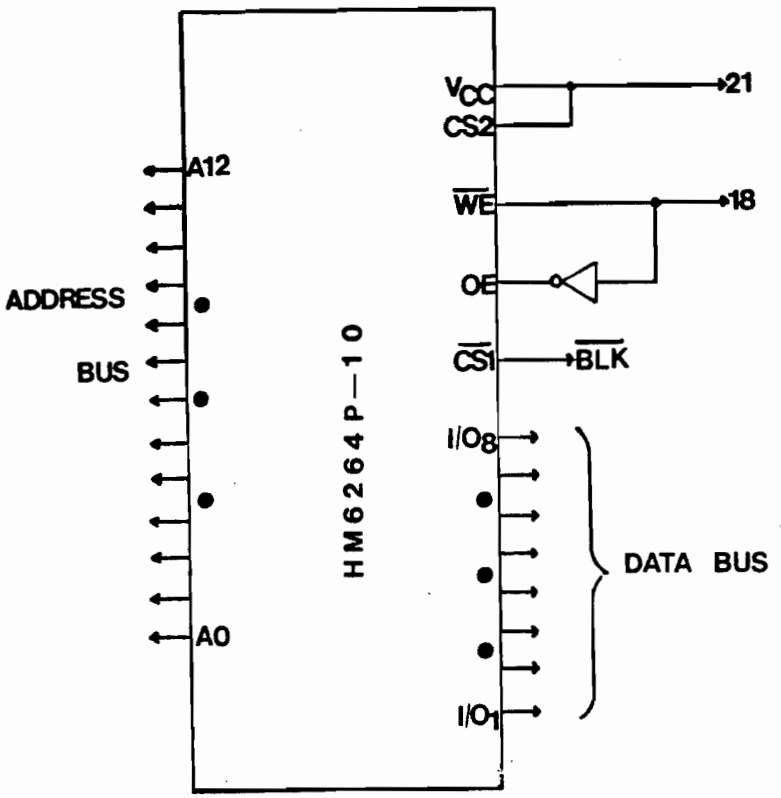


FIGURE B.1:· Typical connection diagram, showing how memory was added to the VIC-20 computer.

B.1) Specification sheet:

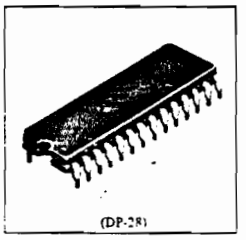
HITACHI IC MEMORIES
HM6264P-10, HM6264P-12, HM6264P-15

HITACHI

8192-word x 8-bit High Speed Static CMOS RAM

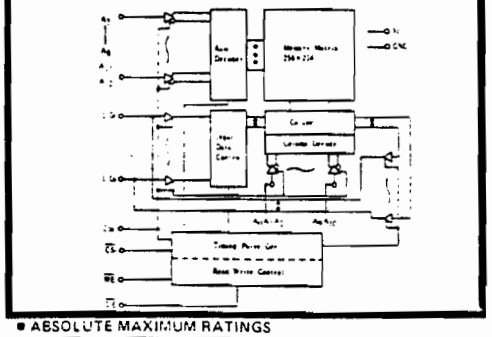
■ FEATURES

- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.1mW (typ.)
  Low Power Operation Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Inputs and Outputs
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

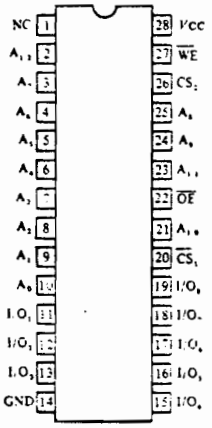


(DP-28)

■ BLOCK DIAGRAM



■ PIN APPRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns.

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

APPENDIX C:

THE ANALOG-TO-DIGITAL CONVERTER INTERFACE

C.1) The interface:

The block circuit diagram on page 143 shows a typical interfacing of the ADCØ816 to the User Port of the VIC-2Ø. The complete circuit as mounted on the interface board, is somewhat different. On the block diagram, some connections have been omitted; the reason for the omission is that the telemetry circuit shares the same data bus with the A/D chip, therefore some kind of buffering is required. The circuit on page 143 is fully operational. In fact, if the A/D circuit is the only device to be connected to the User Port this is how one would wire it.

The following is the detailed functional description of the interface, showing how the chip must be programmed for optimum performance. Turning to page 143, one can see that pins 16 and 32 -START and ALE (Address Latch Enable) respectively- are tied together. Both are then wired to pin 4 of the User Port, which is controlled by bit 2 of Port A register at $9111 (37137). The converter's address lines ADØ throughAD3,are connected to lines C through F of the User Port, controlled by bits Ø to 3 of Port B register located at $911Ø (37136). Before starting the conversion, one has to tell the chip which channel is to be READ. This is done by setting bits Ø through 3 of the DDR for Port B at $9112 (37138) for output, by storing a 1 in the corresponding bits. Next, we WRITE the channel number we wish to READ, i.e. one of channels Ø to 15 inclusively, to Port B of the VIA #1 at $911Ø (37136). To start the conversion sequence,

one must send a positive pulse. This must have a minimum width of 8 clock cycles, because of the present clock speed of 640 KHz going in the converter chip. To achieve this, we set bit 2 of Port A's DDR at $9113 (37139) for output, and then set bit 2 of Port A register located at $9111 (37137) to a 1, and then back to zero. At least eight clock cycles must have elapsed before resetting the bit to zero, or the start of conversion pulse will not be recognized by the chip. On the rising edge of the start of conversion pulse, i.e. when the ALE experiences a low-to- high transition, the binary code for the channel to be sampled is loaded from the four address lines A through D of the chip. At the same time the SAL is reset. When the START line of the chip experiences a high-to-low transition, on the falling edge of the start of conversion pulse, the analog-to-digital sequence begins.

The EOC pin of the chip, pin 13, is tied to line B of the User Port, which is controlled by the CB1 line of the VIA #1 Port B. When the conversion process is over, the SAL sends an end of conversion signal to the computer, by raising its EOC line, pin 13. As mentioned in the section on the VIA #1 Port B, one can select the CB1 to set the flag in the IFR on a low-to-high transition or on a high-to-low transition. Here, because the EOC line rises, one has to set the CB1 line to detect a low-to-high transition on line B of the User Port.

Pin 27 of the converter chip, named Output Enable, is wired to line M of the User Port, controlled by the CB2 line

of the 6522 VIA #1. After the EOC signal is detected, thus raising line M, by selecting the MANUAL OUTPUT MODE (high) as explained in paragraph 2.3.2 in chapter 2, the A/D chip will make the binary number corresponding to the input analog voltage available for READing on pins 25 to 31. These pins are connected to lines C through L of the User Port. To READ the binary data, one selects the DDR of Port B at $9112 (37138), for input, by setting all bits to zero, and then READs Port B at $911Ø (37136). The value present in this location is the same as the binary value on the converter data lines 25 through 31. After the value has been fetched, the CB2 line must be lowered, by selecting the MANUAL OUTPUT MODE (low) as explained in paragraph 2.3.2 of chapter 2. Subsequently, another conversion sequence may be started, if desired.

It is crucial that one does not attempt to READ the digitized value before the EOC signal is issued. It is equally important that one does not send a start-of-conversion pulse before the conversion process is finished. If either of these two conditions is violated, not only will the digitized value be an incorrect one, but there is a very good possibility of permanently damaging the chip. The latter case was experienced in the early development stages of the project, when because of the CB2 line's ability to output a pulse for the duration of one clock cycle, it was wired through a hex inverter to the START pin of the A/D chip. The program to test the chip's performance was written

in BASIC. After the start-of-conversion pulse was sent, an attempt was made to READ the digitized value, without checking the EOC signal. As mentioned earlier, a pulse with a width of one clock cycle is not enough to initialize the conversion completely. However, it is enough to trigger it partially. Because the start-of-conversion pulse sent was shorter than required, the subsequent READs rendered the chip unusable.

Subsequently, a series of tests was conducted to determine the minimum pulse width required to trigger the conversion process. The tests were designed to increase gradually the start-of-conversion pulse width, under machine language program control, until an EOC was sent by the converter. It turned out that a pulse width of 8 clock cycles was sufficient to trigger the conversion process. The specification sheet on page 147, Note 7, states that if the start pulse is asynchronous with the converter clock, as it would be every time one sends a start-of-conversion pulse, the minimum start pulse width is 8 clock cycles plus 2 microseconds. As mentioned above, it was found that 8 clock periods were enough to trigger the chip and this value was used in the VICMON program.

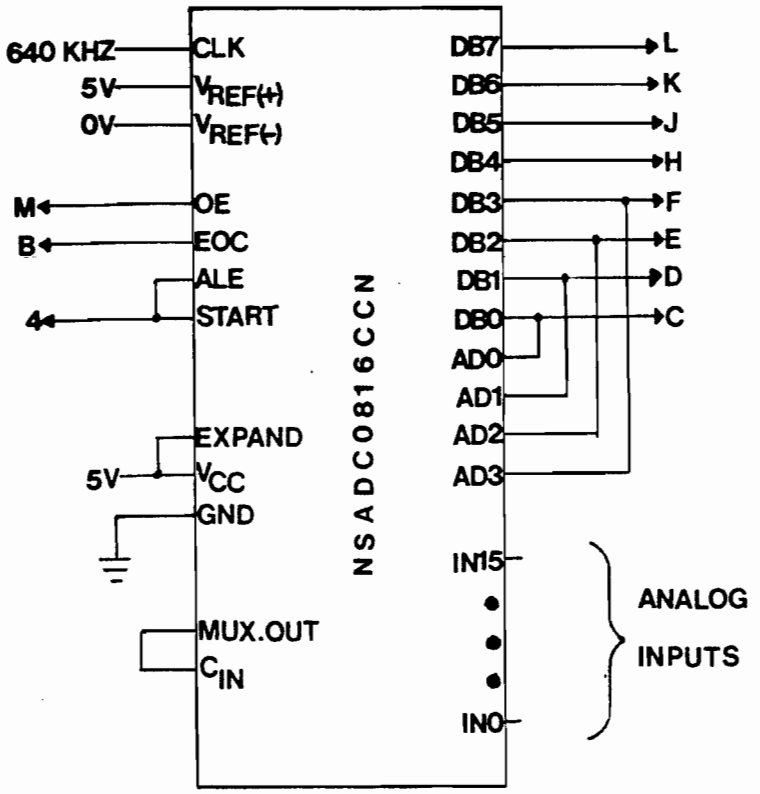


FIGURE C.1: Typical interface between the A/D chip and the User Port of the VIC-20 computer.

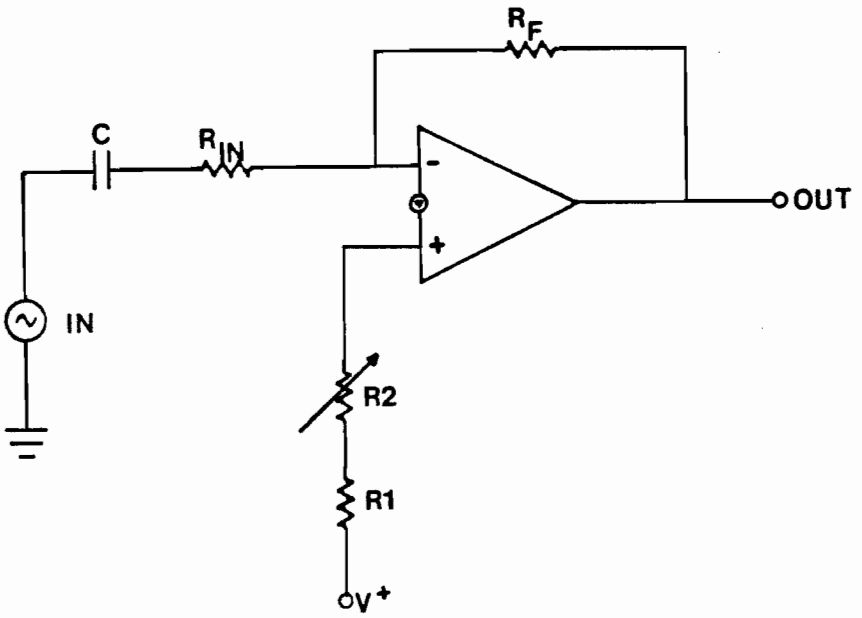


FIGURE C.2: Inverting AC amplifier built using the LM3900 chip.

National Semiconductor

April 1983

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

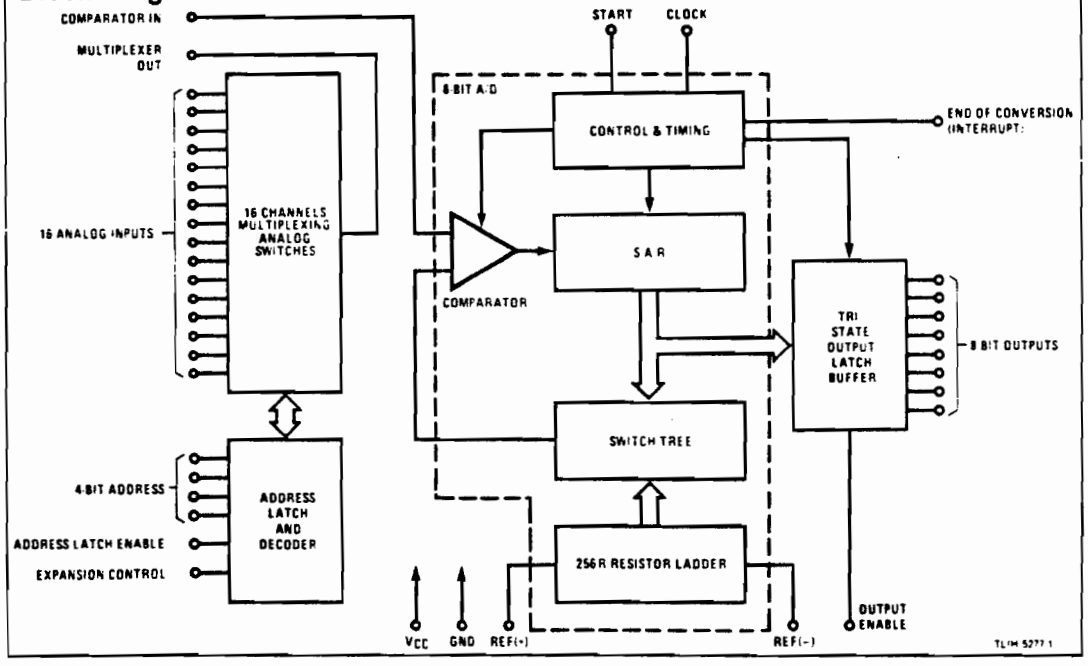
The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

TRI-STATE® is a registered trademark of National Semiconductor Corp.
Z80® is a registered trademark of Zilog Corp.

Block Diagram



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IM-B30M43/Printed in U.S.A

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	−55°C ≤ T_A ≤ +125°C
ADC0816CCJ, ADC0816CCN, ADC0817CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, V_{IN} = $V_{COMPARATOR\ IN}$, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			±1/2 ±3/4	LSB LSB
	ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			±1 ±1 1/4	LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN 4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) T_A = 25°C, R_L = 10k T_A = 85°C T_A = 125°C		1.5	3 6 9	kΩ kΩ kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) R_L = 10k		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C T_{MIN} to T_{MAX}	 −200 −1.0			 nA μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ—$4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN—$4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $T_A = 85°C$ $I_O = -300\ \mu A$, $T_A = 125°C$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = V_{CC}$ $V_O = 0$	 -3.0		3.0	μA μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)* (Note 7)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_S	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time from ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{HO}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_{1H}, t_{OH}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 8)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs (Note 8)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However if an all-zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: If start pulse is asynchronous with converter clock the minimum start pulse width is 8 clock periods plus 2 μs.

Note 8: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + 1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

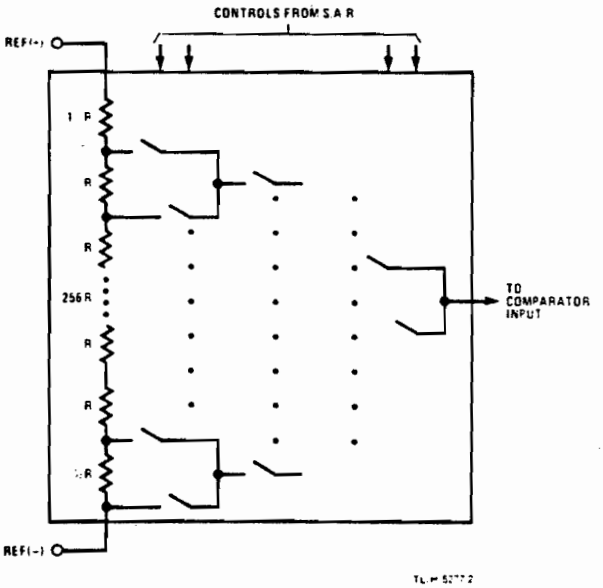


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

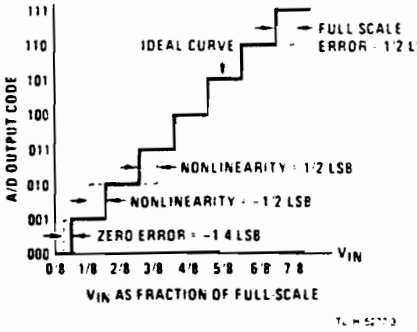


FIGURE 2. 3-Bit A/D Transfer Curve

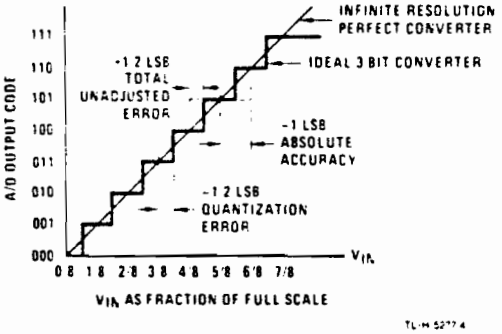


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

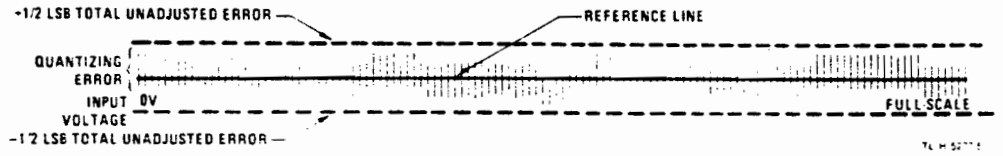
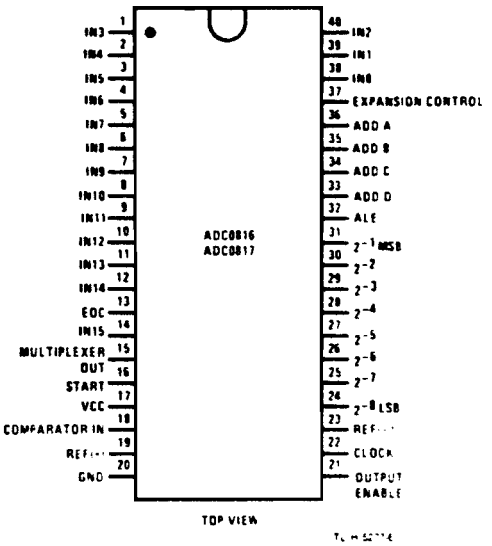


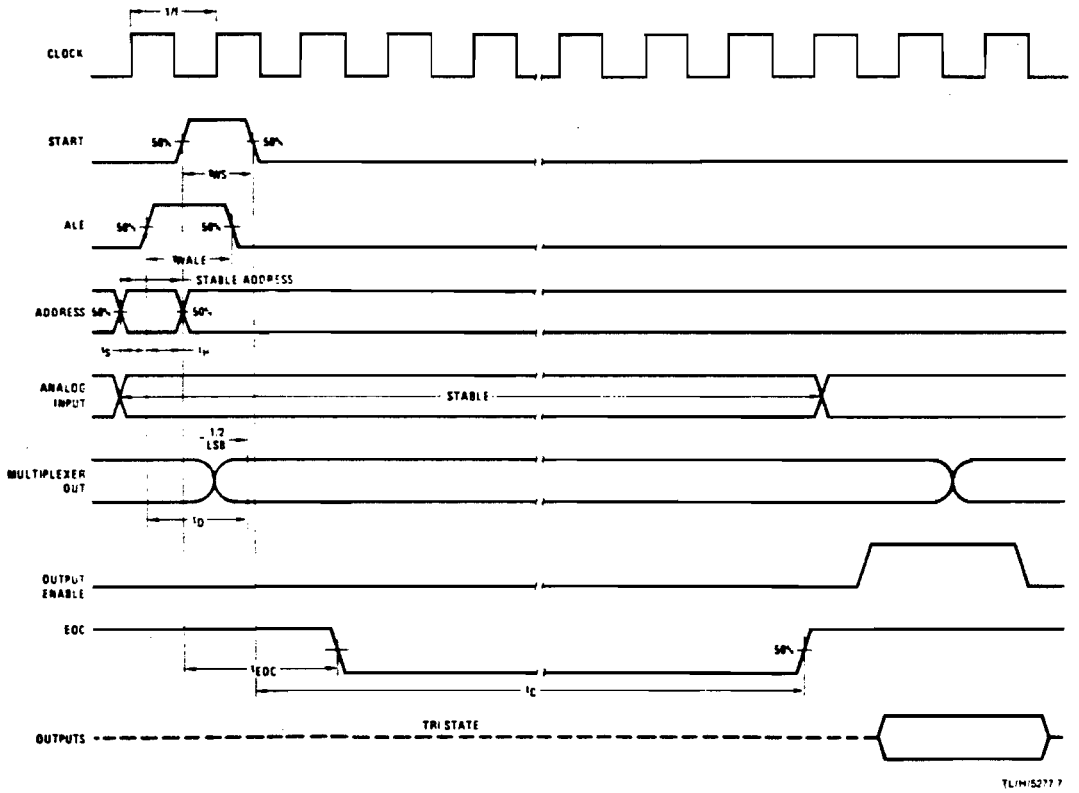
FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



Timing Diagram



TL/H/5277-7

FIGURE 5

Typical Performance Characteristics

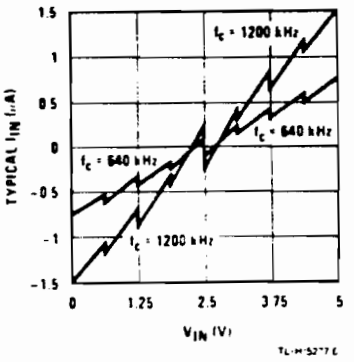


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

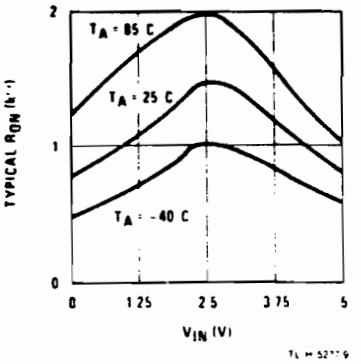


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

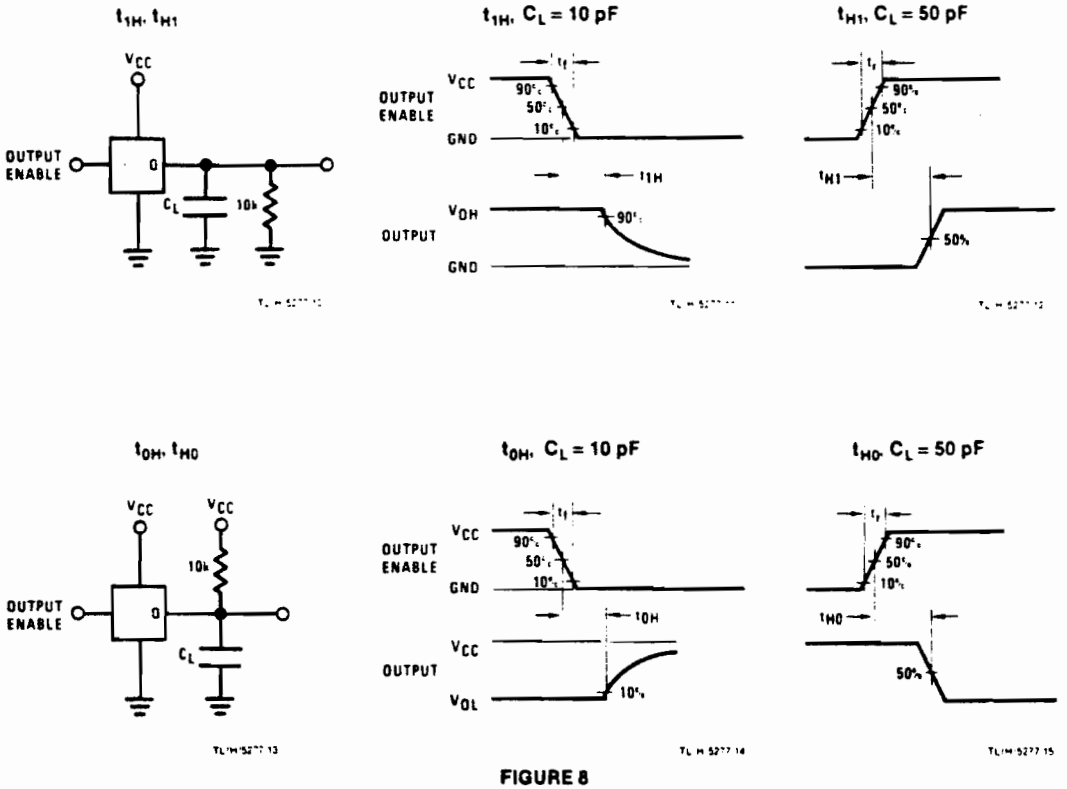


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs. *(Figure 9)*

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

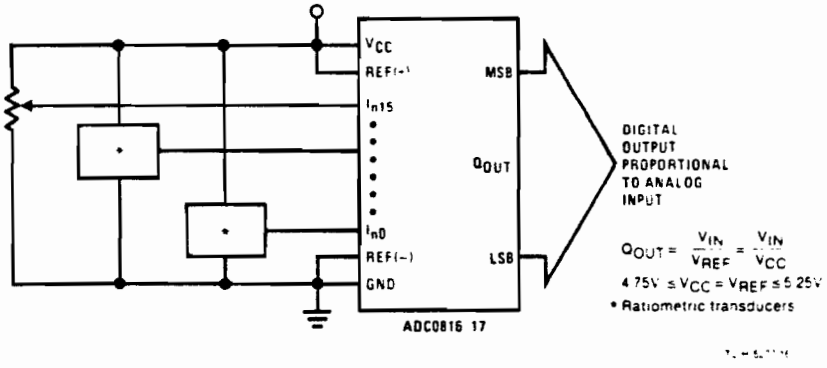


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.

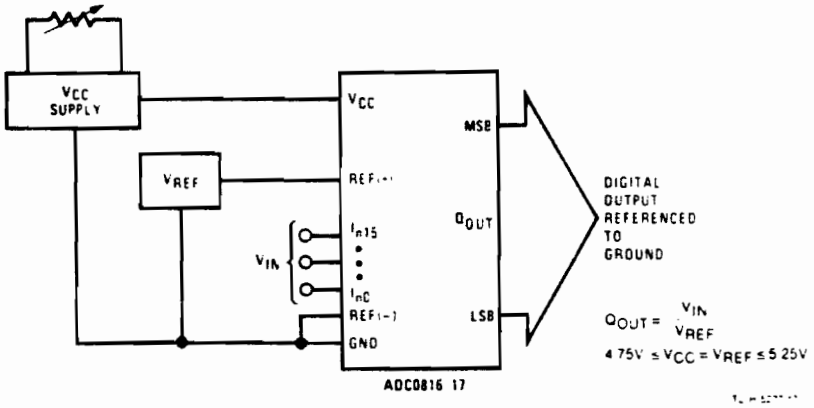


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

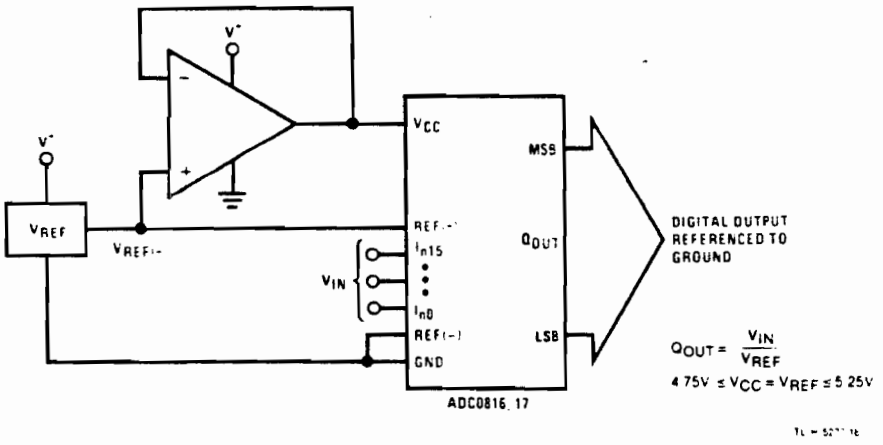


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

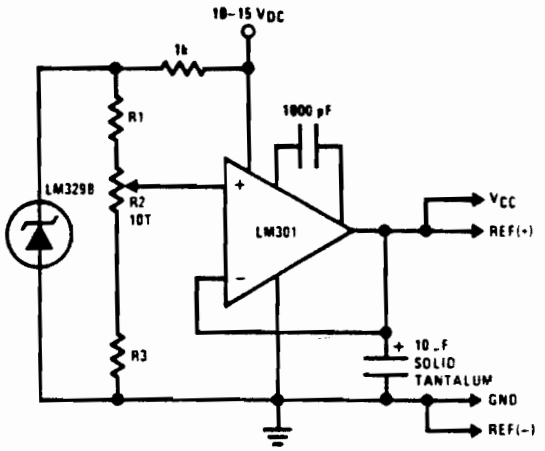


FIGURE 12. Typical Reference and Supply Circuit

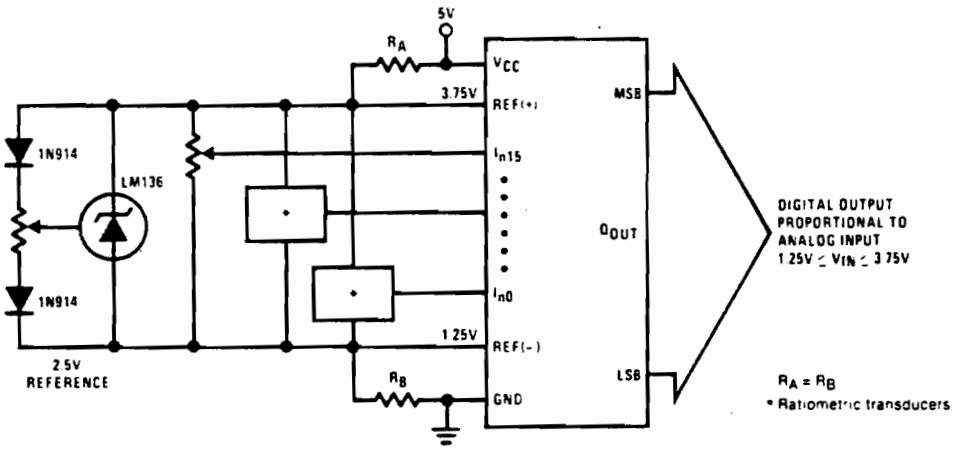


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

$V_{REF(+)}$ = Voltage at Ref(+)

$V_{REF(-)}$ = Voltage at Ref(–)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} - 512$)

Applications Information (Continued)

4.0 Analog Comparator Inputs

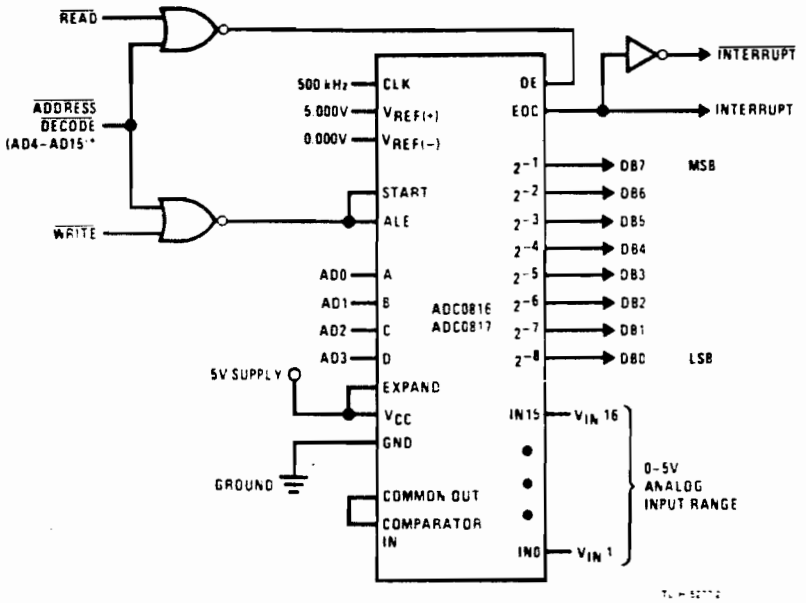
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

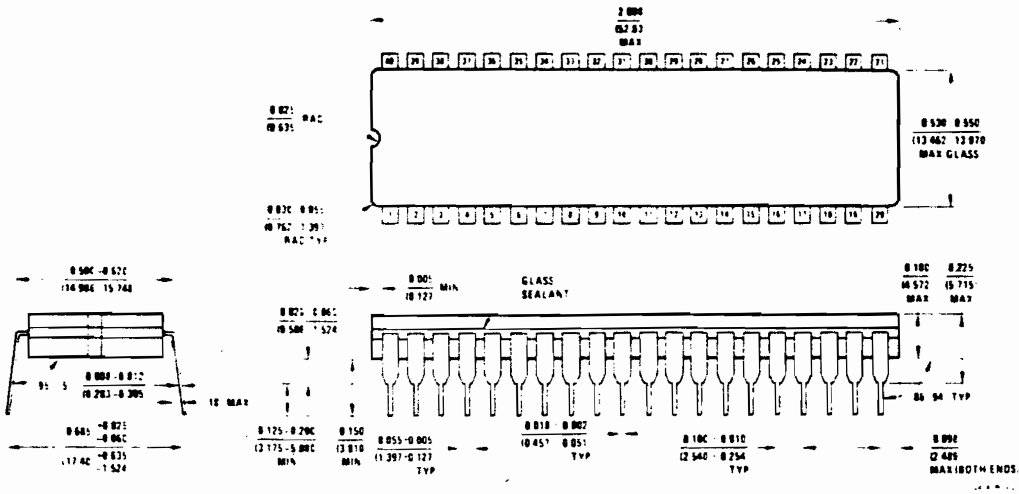
Microprocessor Interface Table

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•Φ2•R/W	VMA•Φ2•R/W	IRQA or IRQB (Thru PIA)

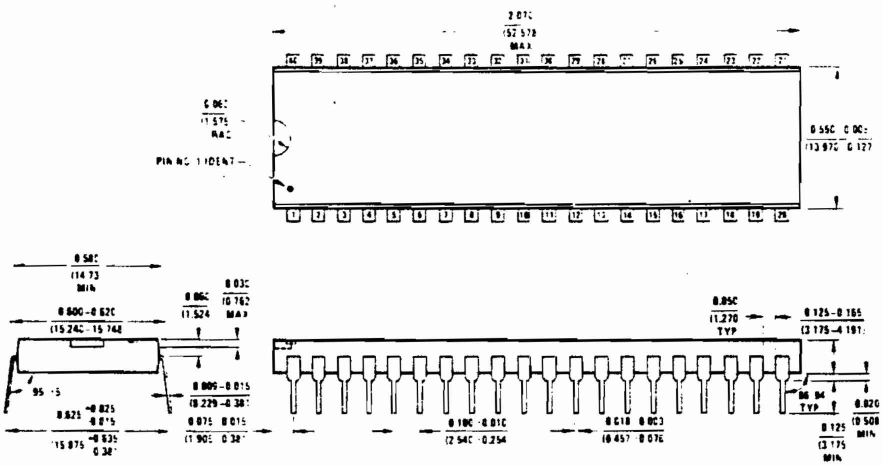
Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	± 1/2 Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	± 1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

Physical Dimensions inches (millimeters)



Cavity Dual-In-Line Package (J)
NS Package Number J40A



Molded Dual-In-Line Package (N)
NS Package Number N40A

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APPENDIX D:

THE TELEMETRY INTERFACE

D.1) The 4046 VCO

To set the operating frequencies of the voltage-controlled-oscillator, one only needs to use one resistor and one capacitor. As shown in Figure D.4 on page172,the capacitor is tied to pins 6 and 7, and the resistor R1, which must always be used, goes between pin 11 and ground. In some applications, a frequency offset is required; that is the VCO must output a certain frequency when the input is equal to zero volts. To provide this offset, a second resistor is needed between ground and pin 12. The input voltage to pin 9, (VCOin), which monitors the output frequency of the VCO, must be positive DC and be limited to the range Ø to Vdd. Vdd can be between 5 and 3Ø volts. There are also minimum values for the resistors R1 and R2, and for the capacitor C1, for good performance of the PLL circuit. The two resistors should not be less than 5 kilohms and the capacitor must be greater than 5Ø pF. The design equations for the VCO output frequency are given below:

$$F_{min} = 1 \,/\, [\, R2\ (\ C1 + 32pF\ )\ ] \qquad \text{(D.2)}$$

with $VCO_{in} = Vss$

$$F_{max} = 1 \,/\, [\, R1\ (\ C1 + 32pF\ )\ ] + F_{min} \qquad \text{(D.3)}$$

with $VCO_{in} = Vdd$

where : $5K < R1 < 1M$

$5K < R2 < 1M$

$5Ø\ pF < C1 < Ø.Ø1 \mu F$

The specification sheets in Reference 17 however, caution that these equations are intended only as design guides. Because both the manufactured and the calculated component values are usually somewhat in error, breadboard trimming is required to achieve the desired precise frequencies. What the specification sheets fail to mention is that the output frequency changes with the power supply voltage. This was discovered in the course of laboratory experimention with the chip. Therefore, a regulated power supply and variable resistors are strongly recommended for more stable and accurate results. To set the extreme frequencies of the VCO one can follow these steps:

(a)- to find the lower frequency limit, ground pin 9 of the 4046, and adjust potentiometer R2, until the desired frequency is obtained. Then the potentiometer must be left alone for the duration of the experiment.
(b)- to set the higher end of the VCO output frequency, connect pin 9 to Vdd and this time, adjust R1, until the desired frequency is reached.

Subsequently, varying the input voltage to pin 9 between Vss and Vdd should directly vary the output frequency accordingly, i.e. lower voltages should give lower frequencies and higher voltages should produce higher frequencies. It is important to bear in mind that if at any

moment, the input voltage exceeds the prescribed limits, it is probable that the chip will be damaged.

If an AC signal is the modulating signal, it should be biased and scaled to the proper levels, as described in paragraph 4.2 in Chapter 4, before it is fed to the VCO input. In that case, the input to pin 9 should be adjusted at Vdd/2 for zero volts input.

Another important point regarding the performance of the VCO is that all other unused inputs, namely pin 3 (PC2in) and pin 14 (PC1in) must be tied to an appropriate logic voltage level, i.e. Vss or Vdd. This is in accord with the series of precautions one must take when working with CMOS ICs. Here, the reason for doing so mainly concerns the Phase Comparator number one (PC1). Whenever PC1 is used, the VCO may lock into frequencies that are the harmonics of the center frequency. This point was tested many times after it was discovered in the early development stages of this project. When the modulating signal was being recovered at the receiving end, even if the input voltage was held at constant at zero volts, there were occasionally, frequencies with exactly twice that of the center frequency. The occurrence of this phenomenon was apparently random, and affected somewhat less than 10% of the data. By grounding the two inputs, i.e. pins 3 and 14, the problem was totally eliminated and no more harmonics of the center frequency were found in the data.

D.2) The Exar 8038 chip

The power supply limits for this chip are:

10 V < Vs < 30 V (single supply)

and

5 V < Vs < 15 (dual supply)

for good stability, i.e. 0.05% per volt.

The sweep voltage applied to the input is bounded by the following limits:

$(2/3\ Vs + 2\ V) < V_{sweep} < Vs$

Consider that the power supply is a 12 volts regulated battery; according to the relationship given above, the sweep voltage will only be:

$10 < V_{sweep} < 12$

which is very impractical. By increasing the supply voltage to the highest allowable voltage, which is 30 volts, the sweep voltage becomes:

$22 < V_{sweep} < 30$

This sweep range is much more practical to work with than the one in the preceding example. However, providing a 30

volt power supply and making sure that the input voltage does not fall outside the 22, 30 volts range, is not readily realized in the field.

D.3) The frequency counter interface

On the main board we have a 16-bit counter and one analog-to-digital converter, where all of them must share the same 8-bit data bus of the User Port. It is not possible to connect all of these lines to the data bus directly, because of interfering logic states. Therefore, a scheme is needed to allow one to choose selectively which device is to be READ, and when the desired device is selected, all other devices that share the data bus are inhibited. To do this, three 74LS245 octal bus transceivers were mounted on the main board, giving the user the possibility of choosing between the analog-to-digital converter, the low-order byte and the high-order byte of the 16-bit counter. When one the three devices is selected for a READ, the buffer between the User Port and that device's output lines is enabled, and the data flow directly from the device to the User Port. At the same time, the other two buffers must be disabled, to prevent any flow for data from their gates. The two disabled buffers will therefore have their output lines in a "floating" state. These bus transceivers can allow data to be transferred in either direction internally. The pin diagram for this chip is shown on page 178. One could provide the possibility of choosing the direction of data

transfer from within the software very easily, but in this project, this was not needed and the direction of flow was fixed in hardware, from the device toward the computer.

The enable line of each bus transceiver set allows one to enable or disable to entire chip. The chip is enabled by lowering (logic state zero), the enable line E, pin 19, and disabled by raising it, (logic level 1). This feature is implemented in hardware, and is selectable in software for obvious reasons.

The option of resetting the counters is provided in software. Three bus transceivers are used to buffer the incoming data. To be able to choose the status of each one of these chips one could devote one line of the User Port to control one device. Examining the User Port diagram, we see that the data bus of the User Port, or VIA #1's Port B lines have all been used for data transfer. The two CB1 and CB2 lines of Port B have specific tasks to perform. Therefore, all the lines on the bottom side of the User Port are taken. Turning to Port A, on the top side, we see that we have already used the JOYØ line, line 4 of the User Port, to connect to the START and the ALE lines of the analog-to-digital converter. There are two available lines remaining that could be used for general purpose interfacing and programming; these are the JOY1, and JOY2 lines, lines 5 and 6 of the User Port, controlled by bits 3 and 4 of VIA #1 Port A register at $9111 (37137).

We are left with two free lines on the User Port, but we have to control four devices. To overcome this obstacle,

we used the 2-by-4 74LS139 decoder/multiplexer. The pin diagram for this chip is given on page 179. The enable pin of the chip, pin 1, is connected to ground, so that the chip is enabled all the time. The two input or select lines 1A and 1B are tied to JOY1 and JOY2, lines 5 and 6 of the User Port respectively. The truth table on page 179 shows how the output lines are selected. In this case, the first pin, or 1YØ, is connected to the RESET pin of the four counters, and each one of the three subsequent data output lines of the decoder is tied to the enable line, pin 19, of the bus transceivers. In this manner, by controlling the states of JOY1 and JOY2 lines of the User Port, one automatically selects the desired device, while the chip disables all others connected to it. This scheme has the advantage that only one WRITE is required in order to enable the desired device for READ, at the same time disabling the others.

The decoder is also mounted on the main interface board, leaving enough room for one 16-pin socket, which serves as the input for all the measured signals. We used the Radio Shack's 4.5" X 4" board as the main interface board. After mounting the general purpose 16-bit counter, 4 IC chips, three octal bus transceivers, one two-by-four decoder, the analog to digital converter, the clock circuit for the A/D chip, and one empty socket for input, about 95% of the surface of the board is used up. The frequency counter circuit was constructed on a separate board, and connected to the main board using a flat cable and the empty

socket.

D.4) Measuring time intervals

The time period of the transmitted signal is measured in the following fashion. First, the output of the frequency clock was buffered to the counter, that is the counter is incremented only when the buffer is enabled. To sample data, the counter is reset to zero, and the buffer is enabled for one period of the input pulse. From the value then stored in the counter, because we know the frequency of the reference clock, the sampled period of the input square wave can easily be calculated. From that the frequency, and finally the voltage of the modulating signal can be obtained. The buffer is enabled on the rising edge of the pulse and disabled on the rising edge of the next pulse, using the 74LS74 D-flip flop. The software program VICTM, written for this purpose, resets the counter to zero, instructs the D-flip flop to enable the crystal clock buffer for the next time period only, READs the number of counts stored in the counter, performs the necessary delay corresponding to the sampling rate selected, and loops back to reset the counter. Because the computer must READ two values, LSB and MSB of the counter, to obtain the correct number of counts, two values must be stored in the data buffer, every time a datum is sampled. Therefore, the memory space is depleted twice as fast as it normally would be, in the case of the analog-to-digital converter, using the same sampling rate. This means that the buffer selected needs to be twice as big, if one

wishes to handle the same number of data.

D.5) Selection of the "overhead" time

In the case of the A/D converter, there was a fixed amount of time spent by the converter to digitize an analog signal, namely 1ØØ microseconds. In determining the period of a signal as above, it would take a different amount of time to get each value. This is because we are dealing with variable frequencies. Lower frequencies require more time to be detected than do higher frequencies. At the bottom of the scale, when the input voltage is zero, the output of the VCO is 125Ø Hz, (a 125Ø hz signal has a period of 1/125Ø = 8E-4 seconds). At the other end, when the input voltage is equal to +6 volts, the output of the VCO becomes 4.5 kilohertz, (which corresponds to a period of 2.2 E-4 seconds). Because of the different time delays imposed on the system, for detecting varying frequencies, it is very difficult to come up with a sampling rate as accurate as the one obtained using the analog-to-digital converter. It would be difficult to devise a system that would allow one to use a variable amount of overhead in this case. The next best solution is to choose a fixed time such as 1ØØ microseconds, as in the previous case. The value to choose may be the overhead corresponding to the time required to detect the smallest possible frequency output by the VCO corresponding to the largest time period. For that value, all subsequent pulses with a frequency equal to the smallest frequency of the VCO

will be sampled with the same time spacing between them. For larger frequencies, since the detection time is smaller, more data will be sampled than desired. This is an acceptable technique, because sampling faster avoids aliasing. This scheme will however have the inevitable effect of distorting and misrepresenting the shape and the frequency content of the sampled signal.

Consider the following example. Suppose we are to sample a low frequency sine wave, say 1 Hz, at a sampling frequency of 1000 Hz. The amplitude of the sine wave varies between 0 and +5 volts, and therefore the VCO output is between 1250 and 4400 Hz. Taking into account our previous discussion of the amount of overhead associated with the detection of each individual pulse period, it is evident that around that part of the cycle near the negative peak, we will sample more points than we really need. Note that the amplifier being used is operating in the inverting mode and biased to +2.5 volts. Therefore, the maximum negative voltages become +5 volts at the output of the amplifier. When one plots the data obtained in this fashion, if data points are spaced by one unit on the X axis, the bottom lobes of the digitized sine wave will be much wider than the top lobes, and therefore the shape of the sine wave will be distorted. Figure D.1 on page 168 illustrates this effect.

It would be impossible to choose an overhead time that would give the absolute answer to this problem. The best thing one can do under these circumstances is to compromise on the value and choose by trial and error an intermediate

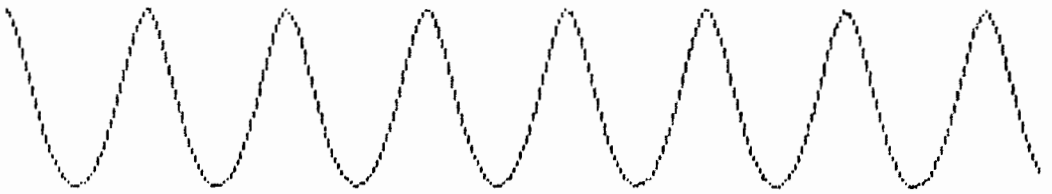


FIGURE D.1: Phenomenon, explained in section D.5, regarding the selection of the "overhead" time.

number that would represent an over all "fixed" overhead time for an accurate sampling rate. The middle value chosen will vary for each 4046 chip and should be selected only after the VCO is calibrated. The results obtained in this manner are not entirely satisfactory, strictly speaking, but as can be seen from the data obtained by sampling a 55 Hz sine wave, shown in Figure 7.1 on page 107, the plotted data are very similar to the digitized sine wave using the analog-to-digital converter shown in Figure 5.1 on page 64. Assuming the overhead in detecting every pulse is that of the pulse generated by the VCO when the input is 2.5 volts i.e. 2.2 kilohertz, we get a value of 4 E-4 seconds. Inserting this value in equation (2.2) we get a value of 2.1 kilohertz. That is, given the hardware design, and the input frequency range of our radios, the fastest sampling rate is 2100 hertz. This is half our sampling speed with the analog-to-digital converter given in Chapter 4. Except in seismic exploration, most geophysical work, deals with events that do not require fast sampling rates (above 1 KHz). Therefore the sampling rate the current telemetry circuit provides is quite adequate in many geophysical studies.

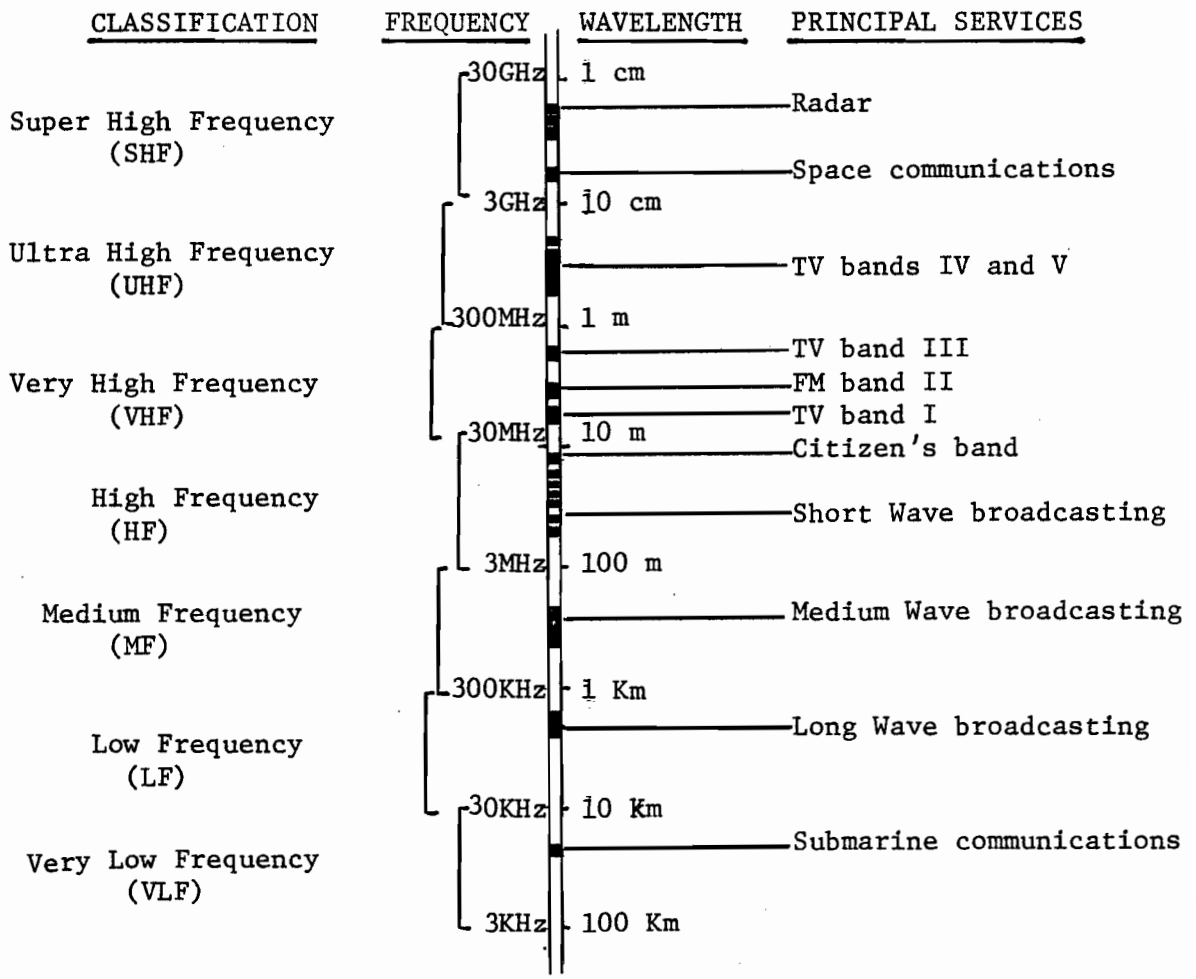


FIGURE D.2: The radio frequency spectrum

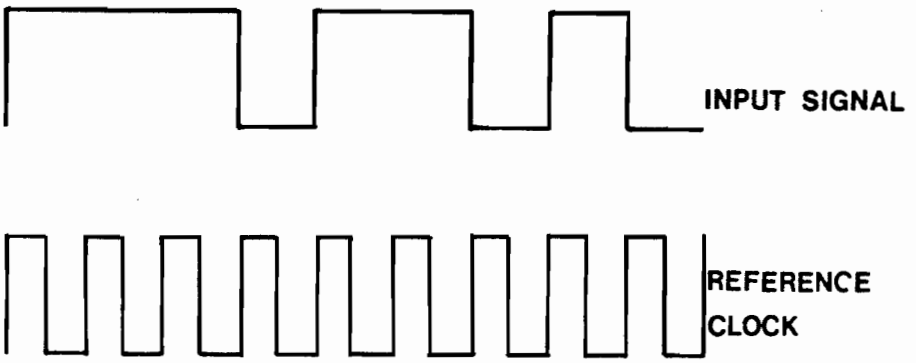


FIGURE D.3: Basis of the method used to recover transmitted signals.
(see sections 6.4 and D.4 for details.)

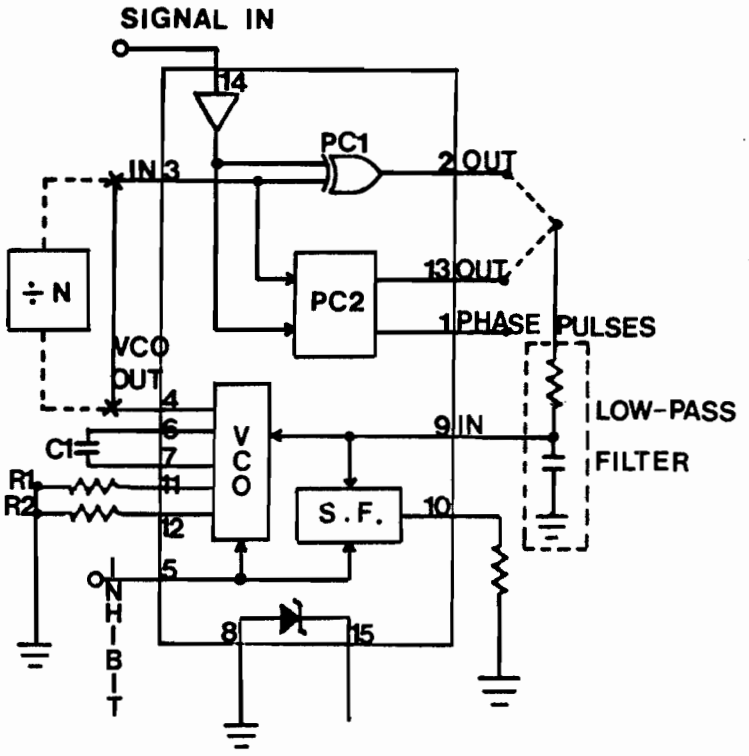


FIGURE D.4: Block diagram of the 4046 CMOS Phase-Locked Loop.

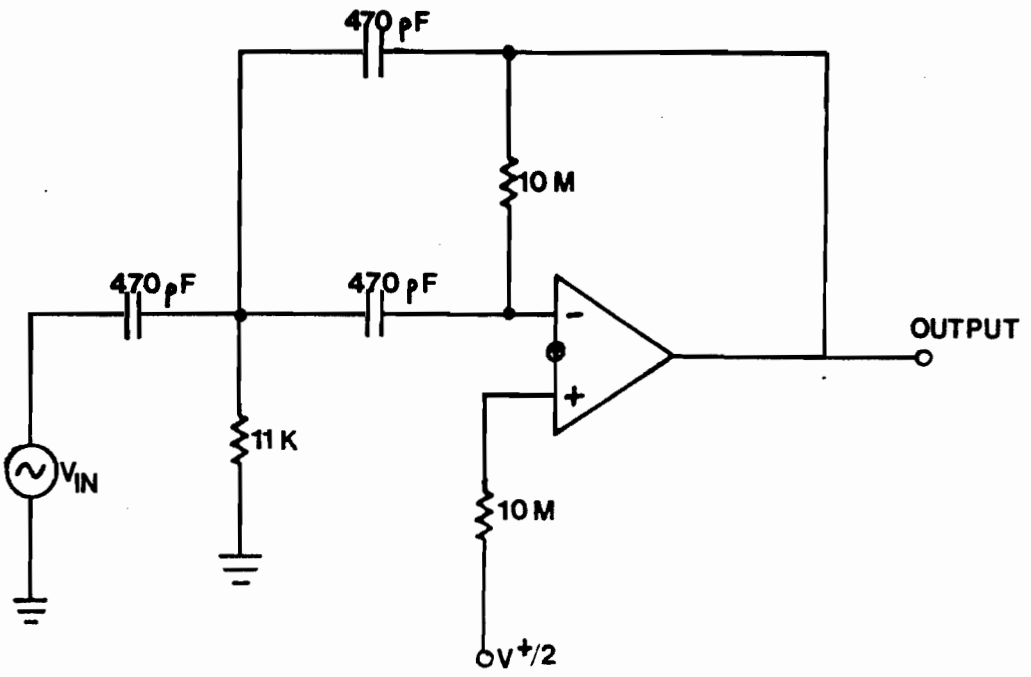


FIGURE D.5: High-pass filter built around the LM3900 amplifier. For the component values shown the cut-off frequency is 1KHz.

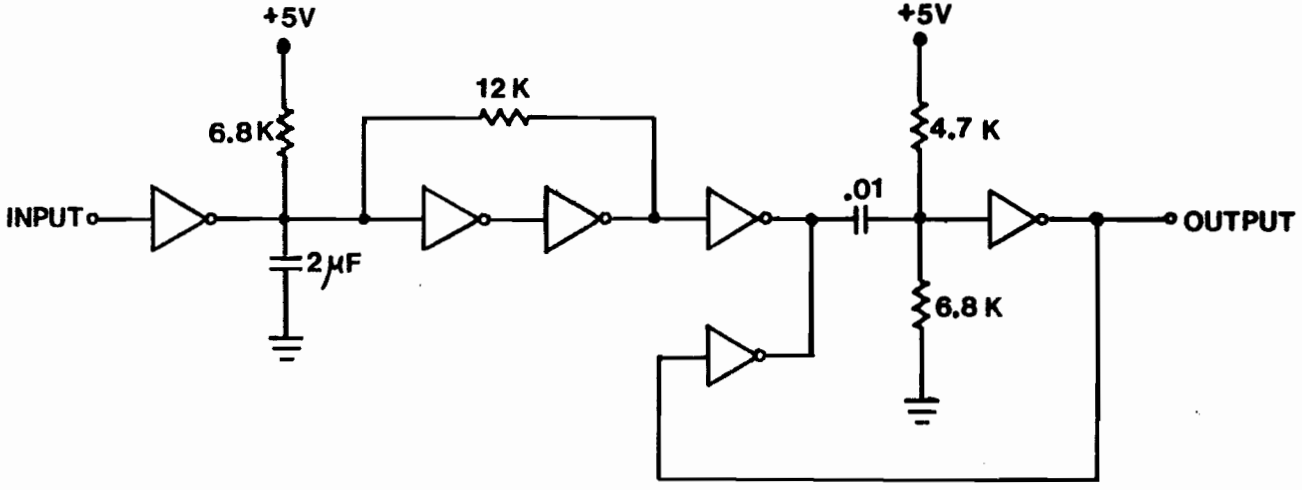


FIGURE D.6: The spike-eliminator circuit built. For the component values shown, the cut-off frequency is 4500 Hz.

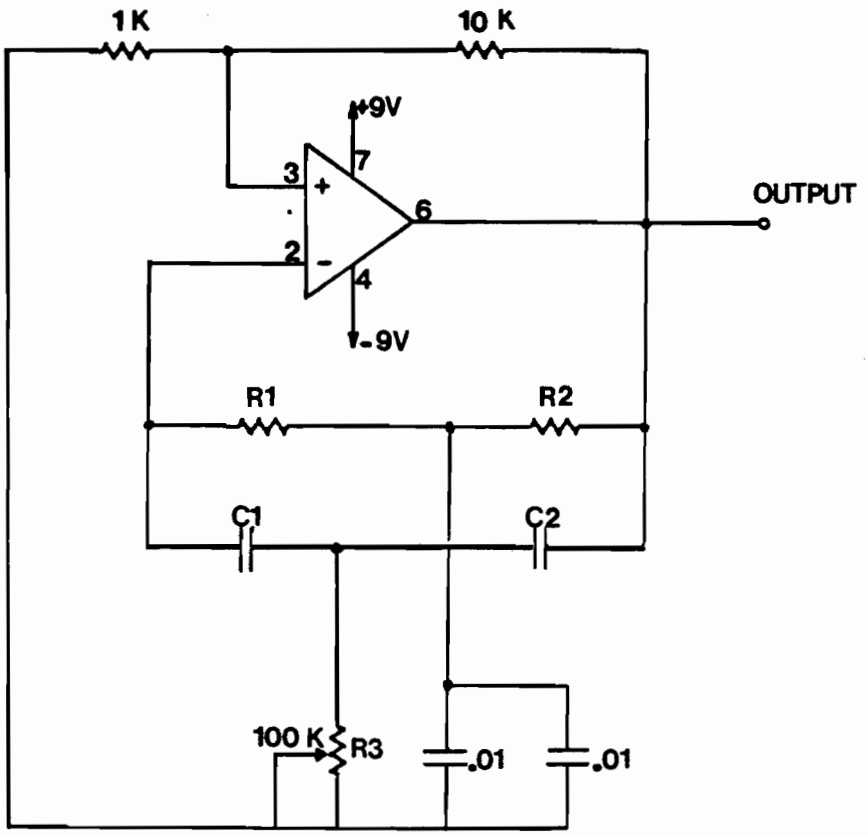


FIGURE D.7: The sine wave generator used in the Field Work. Potentiometer R3 must be adjusted until sine waves are produced. The output frequency is controlled by R1, R2, C1, C2.
$F = 1/2\pi RC$
$R = R1 = R2$
$C = C1 = C2$

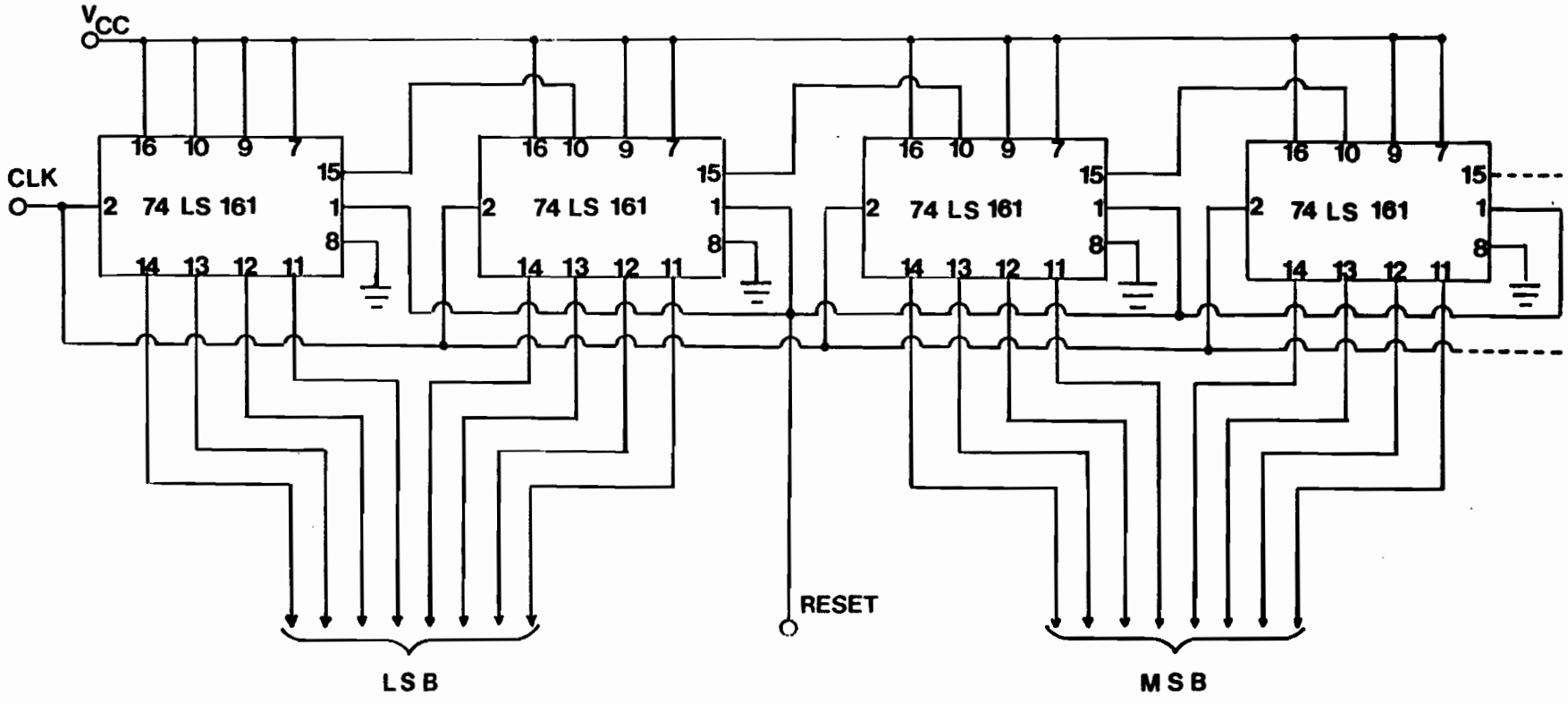


FIGURE D.8: The general-purpose 16-bit counter.

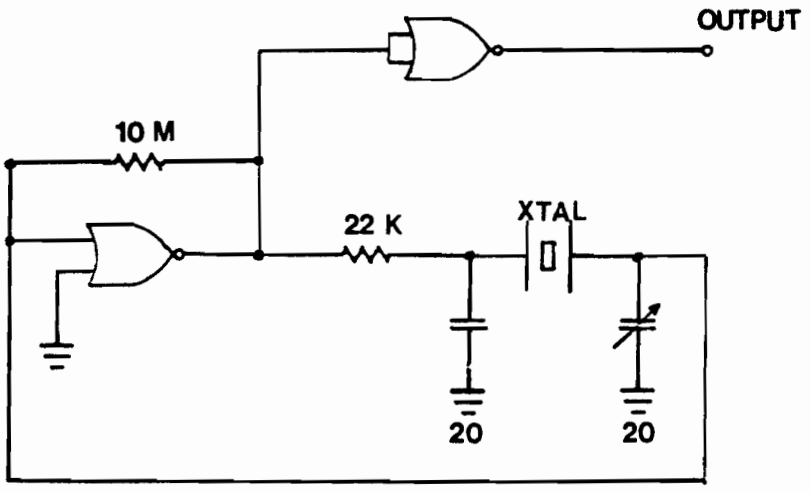


FIGURE D.9: A stable reference clock using two NOR gates and one crystal.

D.6) Specification sheets:

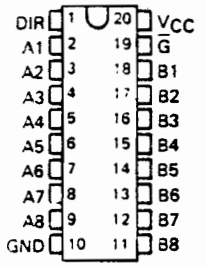
TYPES SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1976—REVISED APRIL

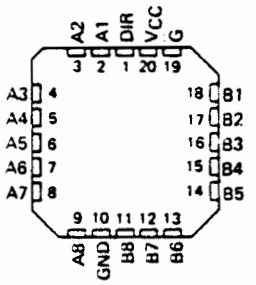
- **Bi-directional Bus Transceiver in a High-Density 20-Pin Package**
- **3-State Outputs Drive Bus Lines Directly**
- **PNP Inputs Reduce D-C Loading on Bus Lines**
- **Hysteresis at Bus Inputs Improve Noise Margins**
- **Typical Propagation Delay Times, Port-to-Port . . . 8 ns**

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	-12 mA
SN74LS245	24 mA	-15 mA

SN54LS245 . . . J PACKAGE
SN74LS245 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS245 . . FK PACKAGE
SN74LS245 . . . FN PACKAGE
(TOP VIEW)



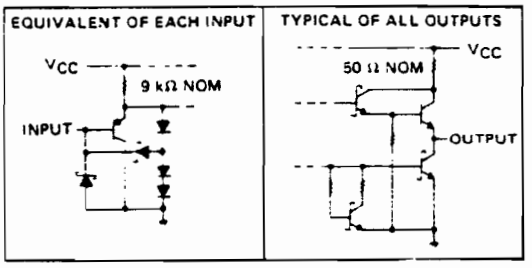
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

3 TTL DEVICES

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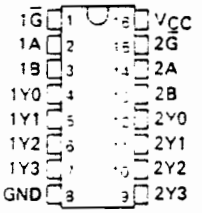
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54LS139A, SN54S139, SN74LS139A, SN74S139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

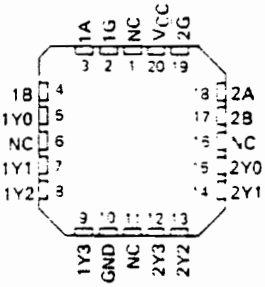
REVISED APRIL 1985

- **Designed Specifically for High-Speed:**
  Memory Decoders
  Data Transmission Systems
- **Two Fully Independent 2-to-4-Line Decoders/Demultiplexers**
- **Schottky Clamped for High Performance**

SN54LS139A, SN54S139 . . . J OR W PACKAGE
SN74LS139A, SN74S139 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS139A, SN54S139 . . . FK PACKAGE
SN74LS139A, SN74S139 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

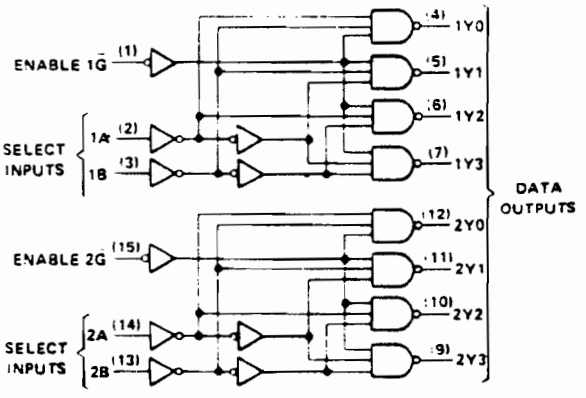
description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and SN54S139 are characterized for operation over the full military range of −55°C to 125°C. The SN74LS139A and SN74S139 are characterized for operation from 0°C to 70°C.

logic diagram



Pin numbers shown on logic notation are for D, J, N, and W packages.

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

TTL DEVICES

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TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74, SN7474, SN74H74, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

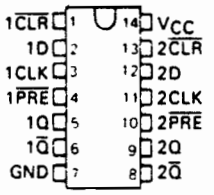
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

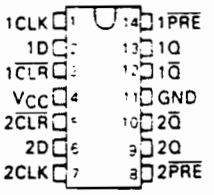
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

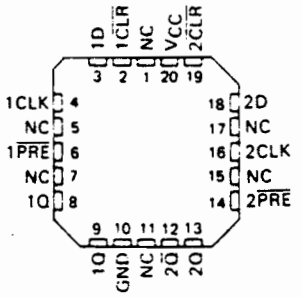
SN5474, SN54H74, SN54L74 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474, SN74H74 . . . J OR N PACKAGE
SN74LS74A, SN74S74 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5474, SN54H74 . . . W PACKAGE
(TOP VIEW)

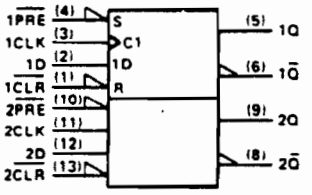


SN54LS74A, SN54S74 . . . FK PACKAGE
SN74LS74A, SN74S74 . . . FN PACKAGE
(TOP VIEW)



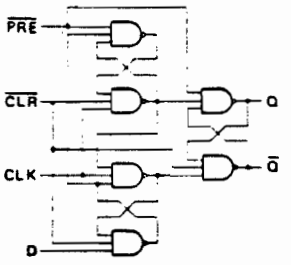
NC — No internal connection

logic symbol†



† Pin numbers shown on logic notation are for D, J or N packages.

logic diagram



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TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS

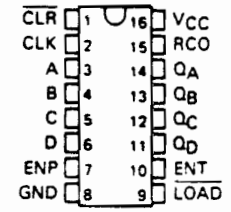
OCTOBER 1976–REVISED DECEMBER 1983

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

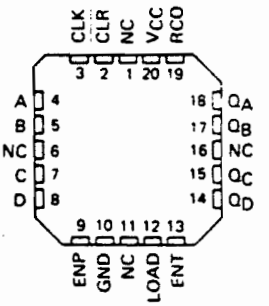
TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74' . . . J OR N PACKAGE
SERIES 74LS', 74S' . . . D, J OR N PACKAGE
(TOP VIEW)



NC–No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE
SERIES 74LS', 74S' . . . FN PACKAGE
(TOP VIEW)



NC–No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

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