A Development Platform for Embedded Wireless Systems

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Abstract

This thesis presents the steps and design decisions followed to develop the architecture of a low-power wireless systems design platform. The design tradeoffs are based on the following characteristics: easy to program interfaces, flexibility, expandability, low cost and low power. The intended users are researchers or students interested in using a robust and reliable platform that enables rapid validation of ideas. A method to integrate printed planar antennas directly on the PCB is also presented along with the analysis of its performance and benefits that it provides to the architecture. Applications using the design platform are also detailed.

Résumé

Ce mémoire de maîtrise présente les étapes de conception ainsi que les décisions prises dans le développement d'une architecture pour systèmes sans-fils à basse puissance. Les diverses contraintes fûrent : simplicité de programmation des interfaces, flexibilité, capacité d'expansion, faible coût et basse consommation d'énergie. Les utilisateurs ciblés sont des chercheurs ou des étudiants à la recherche d'une plate-forme robuste et éprouvée offrant la possibilité de valider rapidement leurs idées. Une méthode pour intégrer une antenne imprimée à même le circuit imprimé est aussi présentée suivie d'une analyse des performances ainsi que des bénéfices que cette méthode apporte à l'architecture. Finalement, des utilisations de la plate-forme de développement sont détaillées.

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Chapter 1

Introduction

1.1 Motivation

1.1.1 Overview

Recent advances in semiconductor technologies have successfully reduced the cost and size of micro-controllers and increased their level of integration to complete system-on-chips (SoC). The recent telecommunication boom has pushed enormous research and development investment in creating sophisticated wired and wireless algorithms and silicon intellectual property. The mass market adoption of wireless networking by personal computer users has pushed prices down and advanced research into the combination of typical radio frequency components on the same CMOS process as common microprocessors. This is transforming the wireless communication field by bringing a tremendous level of integration in off-the-shelf devices now available at very low price.

In parallel, small micro-controllers targeted at embedded systems are experiencing a change in focus. Whereas before manufacturers were pushing for higher clock speed and larger memories, a point has been reached where the complexity of the software and execution speed is secondary to power usage. Some micro-controllers are now aggressively reducing power by stopping some core operation and by dynamically reducing the supply voltage. Power savings are also being integrated in the higher levels of software architecture and in the networking protocols. All of these efforts contribute to create more energy-efficient systems, benefiting the industry and consumers.

The rapid changes in the way embedded systems are designed and the recent addition of

wireless networking capabilities create a need for undergraduate courses to expose students to new design trade-offs. This thesis proposes a flexible, robust and easy to use architecture that can be used for teaching low-power embedded micro-controllers and low-power inter-device wireless networking.

1.1.2 Sensor Networks

Until now, most embedded systems collecting information have to be connected to the central computer with a physical wire to report their data. Alternatively, the data could be recorded locally and stored on a non-volatile media to be later collected by a person and brought back for analysis. The developments in integrated radio frequency integrated circuits (RFIC), coupled with intelligent routing protocols allow clusters of small embedded devices to communicate and report their collected data to a central location. Furthermore, advances in routing algorithms and the higher memory capacity of micro-controllers enable the propagation of the information to be fully automated and fault tolerant. New standards are emerging aiming at simplifying the interconnection of heterogeneous hardware based on a unified protocol designed to support the low-power constraints of sensor nodes. This revolution in how small embedded devices will be able to communicate with each other and the implications that this will have in the marketplace is limited only by the imagination of those that will implement the wireless systems of the future.

1.1.3 Microelectronics Systems Education and Research Applications

Microelectronics systems eduction will have to adapt to new paradigms and ever increasing levels of complexity. Design goals change rapidly and undergraduate students need to know appropriate design methods to be be productive in the workforce. Knowledge of modern embedded systems with advanced networking capabilities must be introduced in the curriculum for the institution to maintain its competitive edge in a time of rapid international development and intense competition. The proposed architecture allows the teaching of the material to be ramped up rapidly while giving students all the required control of the hardware to build up their understanding of all key concepts of embedded systems programming. The platform is designed to support the design tools and hardware interfaces in an integrated fashion, allowing more time for application development and practical concepts assimilation.

The ability to re-program the system at home with a regular PC has numerous advantages for a student with limited time resources. This feature was integrated very early in this design, helping to reduce the requirement for large laboratories. The students only need to use the school lab facilities when major design problems are encountered and sophisticated equipment such as oscilloscopes and logic analyzers are required.

Graduate students can also benefit from a simple and expandable hardware platform for the implementation of embedded wireless systems. This project was done with the intent that anyone interested would have the full access to the documentation and design files to re-use or improve any parts of the current architecture. Most commercial education kits provide enough information for people to use their design kits, but never enough if someone wants to actually modify it or improve it.

This project and the key ideas are for everyone to re-use and improve. The documentation available include schematics, printed-circuit design files, supplier information, bill of materials, design notes and basic application software and demo programs.

Finally, in the spirit of unfettered access to the architecture, the micro-controller was carefully chosen such that the C compiler and assembler are available as open source and are free of charge.

1.2 Thesis Overview

Following the introduction, this thesis will follow with a literature review of the various architectures in the field of sensor networks, the selection of microcontroller and radio transceiver. This work was inspired by the latest development in sensor network infrastructures and Low-Rate Wireless Personal Area Networks (LR-WPAN) standards. The literature review will also reveal which architectures are used in microelectronic system education and how they compare to the proposed solution.

Chapter 3 will cover the architectural details and trade-offs. The various boards used in the architecture will be presented and their high-level design details will be discussed. The requirements for the liquid crystal display and Radio Frequency (RF) board will then be elaborated. The design of the RF board will be presented with an emphasis on the method used to integrate the antenna to the transceiver circuit board.

Chapter 4 will detail the architecture and cover all the key decisions and their implication on the final product. The numerous trade-offs that were required in the implementa-

tion of the final boards will be covered. Emphasis will be put on low-cost manufacturable prototypes and the methods developed for their assembly in an academic environment.

In Chapter 5 the resulting boards will be analyzed along with the various practical designs that were derived from this framework by undergraduate and graduate students.

Conclusion and suggestions for future work and improvements to the architecture and expansion modules will be given in Chapter 6.

Chapter 2

Literature Review

In creating the architecture for wireless embedded systems, the body of research in the field of wireless sensor network is a great source of inspiration. The newest architectures [2, 3] tend to use micro-controllers which consume little power during full-speed operation and also provide multiple control points to reduce the activity of the peripherals. The newest micro-controllers also support multiple clock sources as well as their dynamic selection during operation. Clock sources can be running at very low frequency allowing timers to continue their operation while the core of the micro-controller is completely disabled. Very long operating time, such as several years, is achievable using a simple coin cell battery if the software architecture is well designed for energy efficiency.

Recently, the term Motes or Smartdust have been used to describe tiny sensor devices attached with a power source, some controller and a wireless interface. While the devices are quite far from being the size of dust particles, the relentless pace of microelectronic development allows a steady reduction in size. The latest development in transceiver architectures available for commercial use include media access control built into the RFIC receiver allowing further power savings. This section will discuss the recent advances in the sensor network research field and will highlight the publications most relevant to this research. Following the sensor network discussion, the selection of micro-controllers and RF transceivers will be discussed based on relevant research in the field and evaluation of the devices available on the market. Finally, the use of wireless embedded systems in education will be reviewed.

2.1 Wireless Sensor Networks

Wireless Sensor Networks are small networking devices that can collectively interact together or report information through intelligent routing. The requirements for sensor networks are mostly focused on energy conservation and usually require low data rates which is an interesting aspect when used in teaching since they would not require expensive CPU resources to process the information.

Evolution in sensor network research have brought numerous potential applications and commercial products are available for research purpose such as Micaz [4] or Telos [5] which can be a source of inspiration for a platform used in teaching wireless embedded systems networking. Telos offers a better overall architecture due to its use of more modern 16-bit low-power micro-controllers and is thus a better system to adapt to a teaching environment. Recent use of Motes in undergraduate education [6] have shown that it is possible to use such devices in a classroom environment and get very encouraging and fruitful teaching opportunities.

2.1.1 Micro-controller Selection

At the heart of the wireless sensor unit is the micro-controller. Care must be taken in choosing the proper unit for the application as the semiconductor process used in the fabrication of micro-controller vary from ultra-low power to ultra-high speed. The target market for a particular micro-controller can be cost-sensitive mass market applications, specialized media devices for consumer products, automotive controllers, biomedical devices with extreme reliability requirements or military sensors. With each category, a different set of metrics can be used to evaluate the micro-controller fit for the application. In the context of education and research, extreme temperature tolerance of the availability of volume pricing for millions of units is not relevant. The focus is on low development tool cost (free is even better), ease of use and family expandability. The micro-controller central processing unit (CPU) must follow a simple and textbook-like architecture so that students can relate their code to computer architecture classes. Low prototyping cost is decisive, so is the availability of small quantities of devices.

Table 2.1 shows the most relevant families of micro-controllers that were considered. In the table are the specifications for parts that can be bought directly from a retailer and do not include the items that the manufacturer carries in their official product line (some

of which are nearly impossible to obtain for academic use). The distinction is important since the quantities for small production lots do not justify direct negotiations with the semiconductor vendor. Considering the technology evolution and the general trend 8-bit micro-controllers were not considered. This decision eliminated the Freescale HC11, Microchip PIC, Atmel AVR and the 8051 architecture. Pricing in the table is for quantities of 100 (in US dollar), which would be the typical volume an academic institution would purchase.

Table 2.1 Micro-controller Family Expansion Potential

Family	CPU Core	Price Range	Flash Range	RAM Range
Philips LPC21xx	ARM7TDMI	6.30-8.85	128kB – 512kB	16kB – 64kB
TI MSP430	MSP430	1.45-11.90	2kB – 60kB	128 B – 10kB
Freescale 68HCS12	HCS12	7.40-15.30	64kB – 256kB	4kB – 12kB

Table 2.2 Micro-controller Family Features

Family	GNU Compiler Support	CPU Debug	CPU Architecture
Philips LPC21xx	Yes	JTAG	32-bit RISC
TI MSP430	Yes	JTAG	16-bit RISC
Freescale 68HCS12	Yes (Limited)	Motorola BDM	16-bit CISC

Table 2.3 Micro-controller Family Memory Limits

Family	Architecture Max (Prog/Data)	Memory Space	Max Speed
Philips LPC21xx	4 GB / 4GB	Linear	60 MHz
TI MSP430	64 kB / 64 kB	Linear	8 MHz
Freescale 68HCS12	4 Mb / 1 Mb	Paged	25 MHz

Table 2.2 shows the high-level feature support of various micro-controllers that were researched. The support for GNU C Compiler (GCC) tool chain is deemed crucial because it brings tool vendor independence if desired, is freely downloadable and has no usage restrictions. For the TI MSP430 and Philips LPC21xx the GCC support is well established and widely used [7, 8]. The Freescale HCS12 support by GCC is very limited and buying the compiler suite from specialized compiler vendor is recommended. The antiquated architecture of the HCS12 and its small register count also limits the efficiency of 'C' programs.

All of the processors support freely available real-time operating systems (RTOS) such as FreeRTOS [9] or μCOS-II [10]. The Philips architecture further benefits from the support of the royalty-free eCOS operating system [11] which has a very large user base and is another open-source project. Table 2.3 illustrates the vast range of offerings in terms of addressable and available memory, the LPC21xx family from Philips leading the group because it is based on a 32-bit architecture and uses a very advanced manufacturing process. The MSP430 has limited addressing space mainly due to its internal architecture targeting the utmost in energy efficiency. Reduced size buses and limited RAM memory allow this device to offer the best low-power performance.

The Telos Mote from UC Berkeley uses the MSP430 since it is a natural fit for low-power sensor network. In addition, the architecture is suitable for relatively large software programs. Those need to use hardware abstraction layers to maintain portability of the upper application layers [3], which translates in more memory usage.

2.1.2 RF Transceivers

The frequency of operation of the RF Transceiver impacts the range of transmission that can be obtained using simple resonant antennas. Radio transceivers are available for operation in the 400MHz, 800MHz, 900MHz and 2.4GHz ranges. The higher the frequency, the smaller the antenna will be and the less energy it may capture. Therefore, with higher frequency transceivers, the range obtainable is consequently reduced. International regulations also play a major role in the selection of operating frequency of the transceiver. At this time, the 2.4 GHz industrial, scientific, and medical (ISM) band offer the best international operation due to the uniformity of the standard across the world. This is also the frequency band that offers the best data rate and the largest number of channels.

In wireless communications, power usage and bandwidth are always traded. While each design problem could use a specific modulation and coding scheme, a standard that allows inter-operation of various devices is preferable. WiFi (802.11) and Bluetooth are both very popular wireless standard, but are not suitable for sensor network [2] due to the complexity of the control software and their high data rate. Both of those factors contribute to higher power consumption and increased node price. The 802.15.4 standard [12] from the IEEE aims at promoting a way to inter-operate various transceivers from multiple vendors and set a level of performance which will make compliant devices useful in a variety of applications

requiring low power operation.

Ideally, the micro-controller die would integrate the RF transceiver and the complete system would be on a single chip. At this time, such solution is only beginning to appear in common-off-the-shelf (COTS) parts [13], but the micro-controller unit is very limited in its scope of possible applications due to its tiny amount of code space and RAM resources. It is mainly directed at low-cost, very simple applications such as wireless mouse and keyboard.

The only integrated 802.15.4 COTS transceiver available on the market at the time the architecture was conceived was the Chipcon CC2420 [14]. Only recently did other manufacturers release integrated and 802.15.4 compliant transceivers, but still only the CC2420 meets all the requirements in the 2.4 GHz band [15] while keeping the RF section simple with a single-antenna setup.

Other education platforms have used the older and more popular 802.11b standard in their architecture [16], but this standard does not target low-power systems. The modulation, data rate and beacon rate is targeted at high-speed wireless personal computer networking. Furthermore, the use of Bluetooth or 802.11b in an entry-level embedded systems course would overwhelm the students with the very complex software layers. 802.15.4 allows most of the concepts of wireless networking to be experienced while limiting the cost, complexity and overhead associated with higher speed protocols.

2.1.3 Battery Technology

As electronic devices are getting smaller and more portable, their power source must also scale down. While in microelectronics, the rate at which transistor can be shrinked is an impressive technological feat, the chemical and metallurgical elements of battery chemistry cannot follow that pace. There are numerous possible battery chemistries that can be considered for their use in wireless sensor networks. Older battery such as lead-acid or nickel-cadmium have some cost advantages due to their very well known characteristics and large production volume. However, their low energy density and low cell voltage make them less attractive for this project. Nickel Metal Hydride (NiMH) batteries offer very good charge density. Their main problem is a high self-discharge rate resulting in an empty battery after just a few months [1]. Their discharge rate is further worsened by higher ambient temperatures. Lithium and lithium-ion batteries offer some of the best charge density in the realm of widely used chemistries.

Table 2.4 Battery Technologies [1, Chapter 2]

	NiCd	NiMH	Li-ion	Li-ion Polymer
Energy Density (Wh/kg)	45–80	60–120	110–160	100–130
Overcharge Tolerance	moderate	low	very low	low
Self-Discharge (per Month)	20%	30%	10%	$\approx$ 10%
Cell Voltage (V)	1.25	1.25	3.6	3.6
Peak Current	20C	5C	>2C	>2C
Operating Temp (°C)	-40 to 60	-20 to 60	-20 to 60	0 to 60
Used Since	1950	1990	1991	1999

Lithium-ion and Lithium-ion polymer batteries come out as more technically advanced batteries when Table 2.4 is studied. Lithium-ion polymer batteries further offer the advantage of being very thin thus allowing them to be included in sensor nodes while occupying very little space. The very high energy density [17] of the newest lithium-based batteries require some protection circuit to be implemented to avoid potential destruction of the battery and risks of fire. The table also shows that lithium-ion polymer batteries cannot provide as large currents as NiCd or NiMH. Wireless sensor nodes may draw large current spikes when the transceiver and all the circuitry of the node is activated during a very short time. Some lithium batteries may actually perform better under those conditions [18]. If the current spike is very large when compared to the average current required for operation, supercapacitors can supplement the peak current, resulting in a smaller battery for the application.

2.2 Software Requirements

With any system-level design, the software requirements must be considered early in the process to ensure problem free integration. This thesis focuses mainly on the hardware design, but the resulting system must provide support for a substantial amount of software to fulfill its goals.

In order to guide the hardware decisions, the baseline standard of IEEE 802.15.4 [12] was considered early in the process and estimates were gathered on the code and RAM memory requirements. In the early phases of the project, the upper software layers requirements were based on the various design kits targeted at supporting the Reduced Function Device (RFD) of the Zigbee Specification [19]. The use of those standards as guidelines ensured

that the hardware architecture could support an advanced set of features while setting realistic guidelines for the amount of on-chip resources required.

2.3 Printed Circuit Board Design

The electronics components of the hardware platform rely on the Printed Circuit Board (PCB) for support, electrical connectivity and thermal dissipation. Since the PCB unites all the components of the hardware architecture, the design must ensure that the overall architecture is not compromised by bad design practices. PCB design rely on a set of rules [20, 21] that will not only fulfill the electrical requirements of the design, but also limit electromagnetic emissions and preserve the signal integrity along the various interconnections.

2.3.1 General Design for Manufacture and Assembly

The board must be fabricated in multiple copies for groups of students to benefit from it. Therefore, volume production of the PCB required special attention to the design-for-manufacturing aspects. Within the PCB design tool, a set of clearance such as trace to trace, pad to pad, hole to pad, hole to trace have to be defined based on the capabilities of the PCB manufacturer. The selection of the connecting structures between the layers (the vias) have to be selected such that the hole size is not too small (increase cost) or too big (increase the area wasted on the PCB). Publications [22] explaining the terminology and requirements of the PCB industry greatly helped in setting up the design tools to obtain satisfactory results.

Design-for-assembly is another very important element of mass produced hardware. While a single prototype can usually be made to work without any assembly considerations, the use of automated assembly equipment and the cost associated with each assembly step can significantly impact the project if the limitations and restrictions of the machinery is not considered in the design phase. Examples of considerations for automated assembly include the location of parts (top side only is cheaper), placement on a grid and size of the passive components. The use of surface mount parts allow fully-automated assembly, further reducing cost. Provision for optical alignment marks called fiducial on the PCB is important for accurate and reliable placement. A full list of constraints and requirements is available in reference material [23, 22, 20] on PCB design.

2.3.2 Printed Antenna Design

Printed antennas bring extra constraints on the PCB dielectric material and therefore require extra attention. Printed antennas are sensitive to variations in thickness and uniformity of the dielectric material, therefore using specialized material can reduce the design risks and improve the performance significantly. Numerous publications exist describing printed antennas and their radiation patterns. However, few or none of the publications proposed a proper method to integrate the printed antenna with the RF transceiver. To fill up this void, a comprehensive analysis of the design process and a design methodology [24] was published by our group at the 2005 International Design Automation Conference (DAC 2005). Our method combined the analysis from 2.5D and 3D electromagnetic simulators with the PCB design tools to create predictable nodes with printed antennas that meet stringent power and data transmission range goals.

2.4 Education

The use of practical hardware and micro-controllers in teaching wireless systems is still very limited. Future engineers will need adequate knowledge in this area to remain competitive. Attempts at using hardware infrastructure in wireless teaching has brought good results with 802.11b [16]. Some instructors have approached the problem using Motes [6] in their courses. The availability of complete networking layers made the approach more manageable for students with no previous background in programming embedded systems. We chose to avoid the Atmel AVR micro-controllers used in the Motes environment, because of their 8-bit architecture which we found to be outdated. Modern 16-bit micro-controllers do not support Dual In-Line Packages (DIP) and solder-less breadboards as it was the case with the 8-bit AVR-based Motes [6], so an alternative has to be explored in order to future-proof our architecture.

To solve the problem over the extinction of DIP packages in the marketplace, we designed a board with a soldered micro-controller and use a CPLD for prototyping some of the hardware features. With this approach, students do not build their design totally "from scratch", but they benefit from a similar level of flexibility from the integration of the CPLD. It also represent a more realistic approach since typical modern industrial designs rarely rely on breadboarding as a method of prototyping projects. With higher clock

speeds and smaller technology, this trend is not about to be reversed.

We found that our method offer many advantages to quickly bring students up-to-speed with the hardware. A detailed description of the education platform and its use was published in the 2005 International Conference on Microelectronic Systems Education [25] (MSE 2005). This thesis focuses more on the design details and architectural decisions.

Chapter 3

System Architecture

This chapter presents the overall architecture of the platform for embedded low-power wireless systems. The focus of this section is to explain the key decisions taken in designing the architecture of the system, leaving for the next chapter the implementation details.

3.1 System Overview

The system was designed with modularity and expandability in mind. By adding to the architecture of a typical sensor network node, a platform can be built for students to explore the various trade-offs in building a complete system. Add-ons such as keypads, touch screen panels with graphical displays, audio processing devices and more can later be designed to accompany the main board. Students can define and program the hardware abstraction layer firmware, the user interface, the communication protocol stack and core scheduling algorithm. At the same time, the limitations of an small embedded micro-controller with power, memory and speed constraints will contribute to illustrate the trade-offs always present in engineering designs. When the design platform is used to teach the laboratory classes, students must be able to complete their designs within a 4 months semester. Due to cost and time constraints, students cannot be taught to build PCB and design hardware expansion modules in such a short time. This architecture is meant to provide ample flexibility and eliminate the hardware and fabrication issues, while leaving to students the ability to make hardware decisions through the integration of programmable logic.

On the firmware and software side, a complete implementation of a standard like Zigbee would be too demanding. However, building an understanding of the underlying mecha-

nisms by which modern low-power wireless sensor network operate is achievable and can provide a rewarding experience. A standard such as Zigbee can be used as a reference and a subset containing the important characteristics can be worked out during a semester.

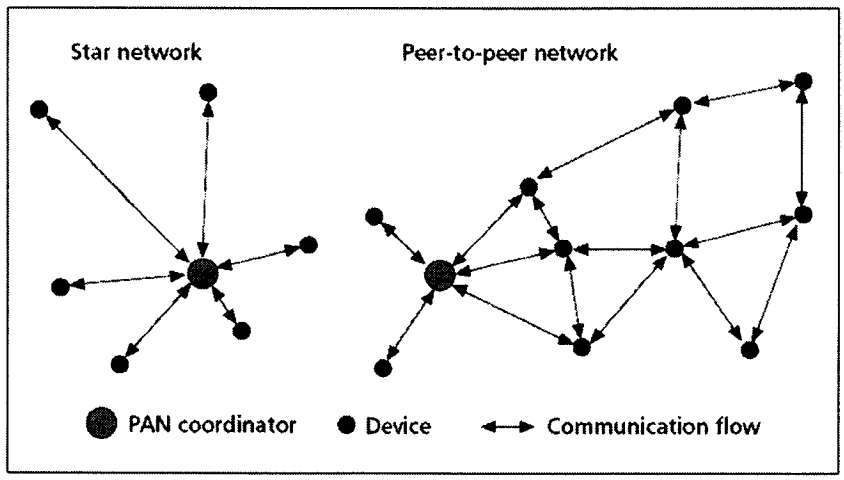


Fig. 3.1 Sensor Network Topology

Typical embedded sensor networks operate using a star or mesh topology with a central unit responsible for collecting, processing and forwarding the information as shown on Figure 3.1 [26]. The device in the center of the star network is called the Personal Area Network (PAN) coordinator and regulates the traffic within its immediate domain. The PAN coordinator is responsible for sending regular beacons. Inside those data frames, some network command can be sent to the nodes. This approach is a fundamental method implemented in low-power sensor network for saving energy and regulating the data flow. Simpler exercises and lab experiments can be done using the Star Network topology as it reduces the complexity on the routing algorithms and are therefore suitable as laboratory exercises.

The main concepts in sensor network technology such as beacon frames, sleep periods and association with the network coordinator can be taught in a short time frame without requiring the coding of very complex data structures. Having a single board that can implement either the network coordinator or the reduced function device offers the advantage of re-using the equipment. In a real industrial application, power considerations, price sensitivity and the complexity level difference between the PAN and the reduced function device will lead to two different architectures.

3.2 Laboratory Setup

Previously, the microprocessor systems laboratory had a setup for teaching on a Motorola 68HC12 platform. The first objective of the new architecture was to replace this outdated platform with one that can be used to introduce wireless embedded systems design and a more modern CPU architecture. Care was taken to avoid any unnessary capital expenditure by adapting the new design to the existing laboratory equipment infrastructure as much as possible.

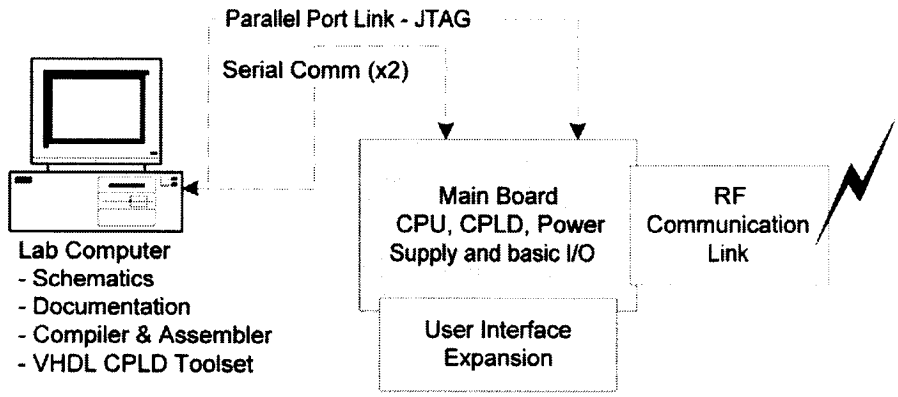


Fig. 3.2 Student Lab Setup

A typical student setup in the lab was envisioned to look like the one presented in Figure 3.2. The personal computer only requires 2 serial ports (RS-232 interface) and one parallel port, exactly like the previous lab configuration. The main board contains the required hardware for the device re-programming and debugging. Two serial channels are preferable, the first one is a direct connection to the PC acting as a terminal interface to the micro-controller board. The second channel allows extra information to be sent out for debugging or alternatively as a communication channel between two micro-controller boards to experiment with simple wired networks. For debugging wireless embedded systems, one of the serial channel would typically be used as a terminal interface and the second channel would be used to log a trace of the packets (a summarized version since the data rate on the wireless port will be higher than capacity of the RS-232 serial interface).

3.3 Main Board

In the initial phases of the research, a main board including a low-power micro-controller was developped. The purpose of this board is to bring students up to speed with embedded systems programming in assembler and in 'C'. The hardware was also designed to be used in a graduate research environment. This board would be a base platform that students would use to build their projects on and would be re-used at each semester. The microcontroller family was chosen to be the MSP430 by Texas Instruments.

In Chapter 2, the comparison between the Philips LPC21xx family and the MSP430 family suggests the use of the Philips ARM-based architecture instead of the MSP430. From a purely economical and performance point of view, the Philips ARM solution was better, having higher speed of operation (60 MHz compared to 8 MHz) and a future-proof 32-bit architecture.

However, the MSP430 is more suitable for battery operated devices when battery life is calculated in months instead of hours. Its architecture aiming for the highest energy efficiency and the energy savings of a 16-bit architecture make it a better candidate for wireless sensor device type of applications.

Furthermore, from an education perspective, the ARM architecture adds a layer of complexity due to the structure of the ARM processor Intellectual Property (IP) cores and their integration by different semiconductor companies. The documentation is divided into two main sets, one coming from ARM and the other coming from the semiconductor manfacturer, in our case Philips. The microcontroller manufacturer describes the operation of their microcontroller and cross-reference the ARM documentation for the details on the CPU core. This creates a complex set of documents that would delay the lab work and hamper the completion of the student's projects in a semester's time. In the laboratory course objectives, the students start with no code other than trivial examples and build all the device drivers, hardware abstraction layers and software architecture from the ground up. This offers a better teaching opportunity and through supervision allow for a better understanding of the methods used to architect embedded software. The MSP430 also benefit from a simplified interrupt mechanism, predictable code execution (no instruction or data caches) and simpler CPU register set.

Previously, the Microprocessor Systems lab used the MC68HC12 8-bit Complex Instruction Set Computer (CISC) architecture. It was not very power efficient and had numerous

reliability issues related to the socketed part on the development kit from Motorola. That problem made it compelling to solder the CPU permanently in the new architecture. The cost of sockets for small-pitch Surface Mount Technology (SMT) being so high that simply desoldering a damaged CPU and replacing it with a new one is more economical even when the manpower cost is included. The newer 16-bit Reduced Instruction Set Computer (RISC) architecture offered by the MSP430 is more in-line with the computer architecture courses students took and also offers more efficient support for higher-level languages such as 'C'.

3.3.1 Programmable Logic Integration

One very important aspect of learning to program embedded systems is the ability to make decisions on the partitionning of computations between hardware and software. The integration of programmable logic in the main board allows students to make those design decisions based on their estimate of the complexity and speed requirements of the problem they are solving. In a graduate research environment the programmable logic allows rapid prototyping of ideas and flexibility in designing expansion modules.

For this architecture, the 0.18um CoolRunner-II family [27] from Xilinx Inc. could have been a great programmable device. It combined flash-based programmable logic, low static and dynamic power consumption and was using a modern process technology. However, the laboratory has to re-use course pre-requisites, therefore the Altera MAX7000AE family [28] Complex Programmable Logic Device (CPLD) was chosen based on the student's previous experience with that particular family in the Digital Systems Design course. This older technology, despite its higher power usage and larger package size, have the benefit of 5V tolerance at the I/O pins with a core running at 3.3V. Therefore, it is compatible with older technology still using a 5V power supply, yet interface directly with the MSP430 running at 3.3V. This choice shows the design constraints imposed by the educational aspect of the architecture include requirements that are not necessarely based solely on technical considerations.

3.3.2 Built-in Programmer

A CPLD device programmer (Byteblaster MV [29]) and a JTAG programming adapter for the MSP430 (MSP430-JTAG [30]) were integrated to the design. This programming hard-

ware allows the re-configuration of the CPLD macrocells and perform in-system debugging and re-programming of the MCU. This reduces the cost of the kits and simplifies the user interface. It becomes possible to reprogram either the CPLD or the microcontroller through the same parallel port just by using the proper software on the PC.

3.3.3 User Interface and Sensor Connection

To allow variations in the design of laboratories, extra hardware was put on the main board. A simple 2-digit 7-segments LED display can offer a great introduction to hardware multiplexing by sharing the same LED segment lines, but rapidly alternating power to the common anodes of the display. The board also features a Multimedia Card [31] (MMC) connector allowing the possibility of an expansion card for this popular flash memory standard. An iButton [32] connector is also present on the main board allowing a number of modules to be connected such as temperature sensor or encryption keys. The iButton is a small metallic container that encloses an IC. The interface to the IC is done through a single pin which carries both the power and the bidirectional data signal. This interface is interesting because it is very robust and is a good fit for sensor network environments.

3.3.4 Power Supply

The main board includes the power supply regulation circuit and is responsible for powering the expansion cards. Three power supply modes are supported:

- External AC adapter providing regulated 5V DC through a 2.1mm center positive barrel jack.
- Battery or Power Supply. This option is very flexible, but carries the risk of burning the microcontroller and CPLD if the polarity is accidentally reversed. To prevent damage, a fused circuit was designed to protect the board's electronic components.
- Parallel port. This mode is reserved for low-current operation (typically the CPU alone) and the power comes from the parallel port interface. It allows students to re-program the microcontroller without having to supply additionnal power to the board. Power is parasitically taken from a selection of parallel port pins. It allows a convenient way to re-program the MCU using a laptop and a parallel cable.

A green LED indicate the proper operation of the power supply circuit. While this contributes to an increase in the standby power consumption, teaching material require this kind of visual feedback for rapid troubleshooting of power supply issues.

3.4 Screen Boards and Touch Panel

For the design of user interfaces, the 2-digit 7-segment LED display present on the main board is very limiting. A daughtercard featuring a graphical screen and touch panel interface was designed to improve the range of laboratories that can be generated using the development platform.

3.4.1 Liquid Crystal Display (LCD) Technology

LCD panels come in a variety of different technologies and form factors. In its simplest form, the LCD segments are connected directly to the Micro-Controller Unit (MCU) through conductive rubber (elastomeric connection) or pins as shown in the left side of Figure 3.3. The MCU can integrate a controller which will alternatively polarize the segment that need to be visible. The liquid crystal material can be damaged by DC currents, therefore, the MCU must constantly change the current direction. Typically, a hardware module within the MCU does this alternating current waveform, leaving processing power for other tasks. Alternatively such circuit can be implemented in a CPLD.

As the number of segments become larger, for example in a 128x64 graphical display (8192 segments), the number of pins required to drive the LCD matrix becomes overwhelming. Therefore, specialized IC can be attached to the display panel to handle the control and the multiplexing of all the segments. Newer technology called Tape Automated Bonding (TAB, see Figure 3.3 – Right) integrate the LCD segment driver and an intelligent controller directly in the ribbon connecting the MCU to the LCD panel. This considerably reduces the price of the LCD unit. The trade-off is that the assembly is more fragile since the ribbon contains a bare die and has very fine copper traces.

For larger LCD panels, such as a 160x160 display, the module may integrate only the segment drivers and no controller, leaving the selection and tradeoffs for the controller to the circuit designer. Data is then fed continuously to the LCD module with the help of a dedicated controller which can be an external IC or in high-end microcontrollers is integrated on the same die as the CPU. The controller can include static memory or an external

memory interface, character generators, graphic accelerations such as block copying and bit masking, gray scale support, and other advanced options. All those would contribute to reduce the load that the CPU has to handle for advanced graphical user interfaces.

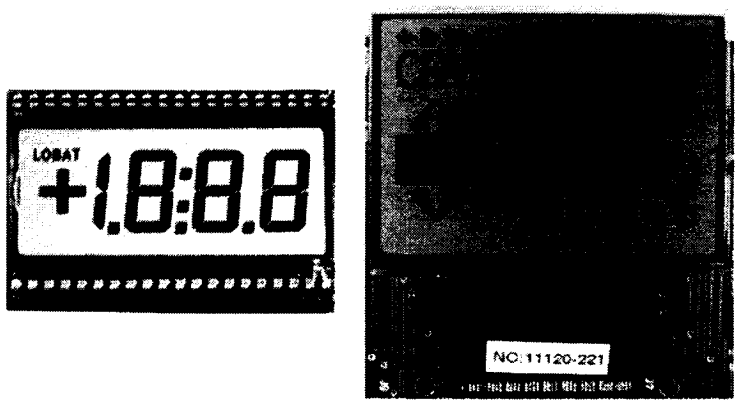


Fig. 3.3 LCD Segments and TAB LCD Unit

A 128x64 TAB LCD with integrated touch panel is designed for the initial laboratories since together they represent a complete embedded system and multiple laboratories can be built upon this platform [25]. The user interface board also included extra serial memory that could be used for students to store graphical items. The external memory shares the same SPI bus as other on-board peripherals such as the touch panel controller and serve as a good introduction to resource sharing and bus conflict resolution.

For our graduate research, a more powerful daughtercard screen board including a larger LCD panel (160x160) was designed. The larger panel however only had LCD segment drivers. An external controller (EPSON S1D13700) with 32kB of on-chip static RAM memory dedicated to buffer the display information was added to the board providing advanced graphical capabilities. This daughtercard also featured LCD bias voltage generation and a touch screen controller.

3.5 Radio Frequency Board

To preserve a certain independance and allow more experimentation to be performed in the wireless design, a RF daughter card was designed to integrate the wireless transceiver and antenna in an efficient and easy-to-use unit. This card can be attached to the Main Board

to turn the system into a complete wireless sensor node or PAN coordinator depending on the firmware programmed into the MCU.

This board required the most research and time to develop when compared to the other ones. First, selecting the transceiver while following the low-power constraints and embedded sensor network aspects required careful consideration of the devices available on the market since it would have the biggest impact in the design of the transceiver board. Secondly, we have decided that the antenna should be integrated on the PCB for cost and reliability reasons. However, to the author's knowledge, there was no literature available on the process of designing the antenna and then integrating it with a PCB design tool. Most publications in the antenna field focus only on the antenna itself, leaving the integration and board effects on the radiation pattern as an exercise for the readers. Most publications on PCB focus on reducing Electromagnetic Interference (EMI) problems and on how to *avoid* creating antennas into circuit boards. Our initial goal was thus to establish a methodology for integrating printed antennas on PCB while understanding the effects of the PCB on the antenna radiation pattern. Furthermore, we were also interested in analyzing how the printed antenna could exacerbate EMI produced by a microcontroller or clock generation circuit [24].

3.5.1 2.45 GHz Radio Transceiver

The main technique for the wireless operation to be low-power is to use of long sleep periods which are synchronized with beacon frames sent periodically by the network coordinator. During the sleep period, the power consumption is dominated by leakage current from the RF transceiver, the CPU, the sensors and peripherals.

It is well known from communication theory that the lower the data rate, the lower the power consumption, but one must be careful not to use an architecture which would require too much time to receive the information. As the data rate go down, the power consumption for the receiver and transceiver also scale down. At a certain point, the biasing required to power the analog and demodulation circuit consumes much of the power. From that point, lower transmission rate will actually increase the amount of energy required to transfer the information. It was found that in small and low-power wireless sensor radio frequency integrated circuits, the power consumption in receive mode is counterintuitively higher than in transmit mode. Since the sensor node is in receive mode for long periods,

the receiver energy consumption is a critical design characteristic.

Furthermore, most of the time sensor nodes are either in sleep mode or in receiving mode, listening to beacon messages from the PAN coordinator. The beacons duration must be short thus the importance of a high data rate. A lower data rate would keep the receiver active for longer periods and have a negative impact on the energy efficiency of the whole system.

In the study of RF transceivers, the nRF2401A [33] from Nordic VLSI stand out as an interesting candidate for wireless sensor networking. It uses high speed (1 Mbps) bursts of data to reduce the potential for packet collision as well as reduce the transceiver time to complete a transaction. The nRF2401A also features dual receiver capability which allows it to receive information from two sources at the same time. However, it is not compatible with the IEEE 802.15.4 standard due to its different modulation method. It also cannot support hardware acceleration of encryption, which we feel is important for research in secure wireless network deployment. Finally, while the nRF2401 can filter network addresses and perform hardware CRC computations, it cannot handle automatic acknowledgment of packets, which in sensor network is very beneficial as it reduces the energy used by the microcontroller and increases network reliability.

The CC2420 from Chipcon [14] addresses most of the above issues with a fully compliant IEEE 802.15.4 transceiver. The receive power consumption is slightly higher (19.7mA versus 18mA for the nRF2401), but the automatic packet acknoledgement, hardware encryption (AES-128) and the precise received power analysis features of this device make it an ideal candidate for wireless systems education and research. This transceiver was chosen for our wireless architecture.

To further reduce cost and board complexity, we have decided that the transceiver board would be on a 2-layer PCB instead of the recommendation that the PCB be 4-layers [14]. We used electromagnetic simulation tools when designing the PCB to avoid potential issues caused by the reduction in the number of layers.

Abstracting the RF circuitry and integrating it in a robust and low-cost manner was our primary intent. We aimed at providing seamless integration of the radio modules in the laboratories without the need for students to understand the intricacies of RF design. The radio transceiver unit is thus build on a separate printed circuit board to allow future upgrades of the RFIC while reducing the main board complexity and cost.

By building the antenna feed line using a microstrip line shielded with the bottom

grounding plane and a barrier of vias, we avoided EM waves from propagating into the dielectric near the digital connections [24]. The RF section of the design is thus isolated from the digital input lines. Therefore, the radio frequency board can be connected to the main board without significantly affecting the high frequency operation or the antenna radiation pattern.

Specialized dielectric materials were successfully used to integrate the transceiver and antenna, as will be shown in the next chapter. The laboratory measurements matched theoretical values, which validated the accuracy of the antenna model.

3.5.2 Printed Antenna

The true potential for wireless sensor networks and their application in large scale deployments can only be realized if one addresses the cost issues. The relatively high cost of coaxial cable, RF connectors and antennas capable of handling the 2.4GHz signal with minimal attenuation were identified as major cost elements in our design. For example, a single coaxial connector of the SubMiniature Version A (SMA) type such as those used to connect the coaxial cable to the antenna costs the same as the CC2420 transceiver IC. If one ever wishes to use wireless sensors to address practical problems, the mass production cost of the sensor nodes has to be as low as possible. This is the main motivation for printing the antenna directly on the circuit board.

System-level analysis is required to determine the network density as a function of antenna cost. Since sensor networks are spread over an area, a small increase in the link budget will translate into a quadratic decrease in the required number of sensor nodes to cover that area.

Key Antenna Parameters

The three key parameters in evaluating the coverage of a wireless link are the receiver sensitivity, the antenna gain and the antenna radiation pattern. Since we are using a commercial transceiver, the receiver sensitivity is a given parameter and we can only provide adequate power supply filtering based on the manufacturer's recommendations. On the other hand, the antenna gain and radiation patterns are all under the designer's control if the antenna is printed on the PCB.

Since our architecture targets the largest possible range of uses, we aimed for an omni-

directional antenna (power is radiated uniformly around the antenna) with a few decibels of gain in the horizontal plane. As mentioned previously, this small gain on the horizontal plane will translate in lower node density at the system level and will result in lower system costs.

3.6 Software Support Requirements

In embedded systems design, the software requirements must be taken into consideration to ensure that the hardware architecture aligned with the code that will be running on it. Instead of defining a new network architecture, we decided to follow an existing network protocol for Wireless Personal Area Network (WPAN). Following a standard provided a baseline for the memory and speed requirements and allowed hardware design trade-offs to be taken early in the design stages. As a baseline for the node capabilities, the Reduced Function Device (RFD) specifications from the IEEE 802.15.4 [12] standard was followed. This standard originates from the integration of the efforts of HomeRF and the IEEE 802 Working Group 15 and targets low-power and low-cost wireless networking [26]. Its focus is on low complexity and efficient energy usage. The data throughput is much lower than for protocols aimed at data communication such as those covered by the IEEE 802.11 standards. The low data rates are unlikely to be a limiting factor in the type of applications targeted by this architecture.

Furthermore, in the context of research and teaching, the IEEE 802.15.4 has been made publicly available at no fees for download. This contributes to making the research platform more affordable since access to standards is not typically purchased by university or libraries. The availability of a very complete technical standard will provide a great learning opportunity for anyone not familiar with the way standards are written and organized.

Figure 3.4 [12] illustrate the layers of the 802.15.4 protocol stack. The standard only covers the lower layers namely the Physical layer (PHY) and the Media Access layer (MAC). The upper layers are outside the scope of the standard, but could consist of a research or a student project such as testing a new routing algorithm or a novel application running on top of the MAC layer. The Chipcon CC2420 supports all the PHY requirements of the standard. Some of the MAC requirements are supported by the hardware, thus limiting the software cost and complexity. This allows small microcontrollers to perform quite complex

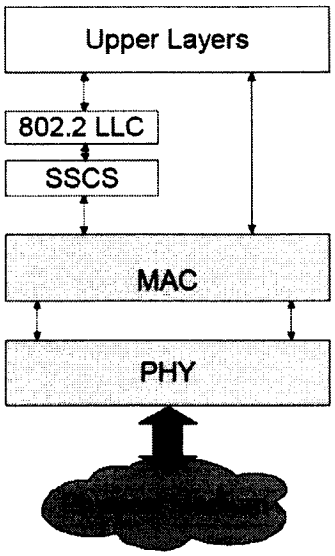


Fig. 3.4 802.15.4 Device Software Layers

operations on top of the PHY and MAC networking layers.

3.6.1 Memory Requirements

RAM Memory

In order to maintain the content in the memory, some static power must be supplied to the micro-controller even in sleep mode. This small current is integrated over long periods of time since the micro-controller in low-power wireless systems spends most of the time in a sleep state. This pose a significant challenge for the architecture since the RAM becomes the dominant energy user. As a consequence, ultra-low power microcontrollers typically have very little of it (a few kilobytes is typical). The small packet size (128 bytes) defined in the 802.15.4 standard ensure that a minimal amount of RAM is needed to handle incoming transactions. The memory requirements to support the MAC and PHY layers is further reduced since a large portion of the standard is handled by the transceiver IC, including the buffering and validation of incoming packets.

Flash Memory

The microcontroller on-board flash memory can be supplemented by external serial flash memory to further extend the capabilities of the system. For a small cost, the external flash memory can be much larger than the internal memory of the controller. It can be used to store firmware updates temporarely before the MCU Flash memory is updated. It can also be used to log data in the event of a disruption of the network. Counterintuitively, programming a byte of flash in an external device is less energy efficient than sending the same byte of information through the radio interface [34]. Therfore, for the longest battery life, the use of the wireless network is always preferred.

From our experience, around 20kB of flash memory and 1kB of RAM is sufficient for the sensor node to operate as a reduced function device. A few more kilobytes of flash memory would be sufficient to hold simple application software. However, the RAM requirements for supporting a PAN coordinator vary mostly on how many nodes can connect to the coordinator. Since the coordinator node has to build and maintain a table of the connected node, their internal addresses, pending messages and some routing information, the RAM memory requirements surpass the limits of low-power MCU for large networks. Our research group thus developed a dedicated PAN coordinator [35] using the Philips LPC2106 ARM-based microcontroller.

3.6.2 Remote Debugging Capability

The flash and debugging operations can be carried out through the JTAG chain. The processor choice in an environment requiring remote controlling of its operation was explored in the initial phases of this project. The architecture requirements for remote testing of the components in a network environment is detailed in the 2004 International Test Conference proceedings [36].

3.6.3 Validation Suite

A set of firmware drivers was developed to quickly test the board features. They were used to validate the correct operation of the boards after their manufacturing and is still used in between semesters to ensure that they still operate properly. The firmware framework also provides a base code structure for teacher assistants to quickly illustrate various board features and for class demonstrations.

Chapter 4

Design Details

This chapter will cover the design details and the various aspects considered for the development of the circuit boards of the wireless systems development platform. First, the Main Board, LCD Board and RF Transceiver Board will be detailed. Then, the PCB Design methods and their impact on the boards design will be elaborated.

4.1 Main Board

The McGill University Micro Processor Systems Version 1.0 (McGumps) main board was designed as a flexible and expandable platform for research and teaching. Figure 4.1 shows the block diagram of the McGumps board and highlights its key elements. This design reflects the architectural decisions described in the previous chapter. The diagram illustrates the logical view of the design elements as well as their approximate physical location. McGumps was designed to be used without any enclosure and rely on four aluminum standoffs located in each corner for support. The programming and communication cables come out from the back of the board (top of the diagram) and the power sources enter from the left side. This organization allows the board to be used on a lab bench while keeping the cable clutter to a minimum.

The printed circuit board was fabricated using a commercial process on a Flame-Retardant Level 4 (FR-4) dielectric. It features a top and bottom solder mask using the Solder Mask over Bare Copper (SMOBC) process, preventing oxidation and allowing high reliability assembly using either reflow or wave soldering. The board was assembled at a commercial facility based on a kit of parts and a generated placement file. One working,

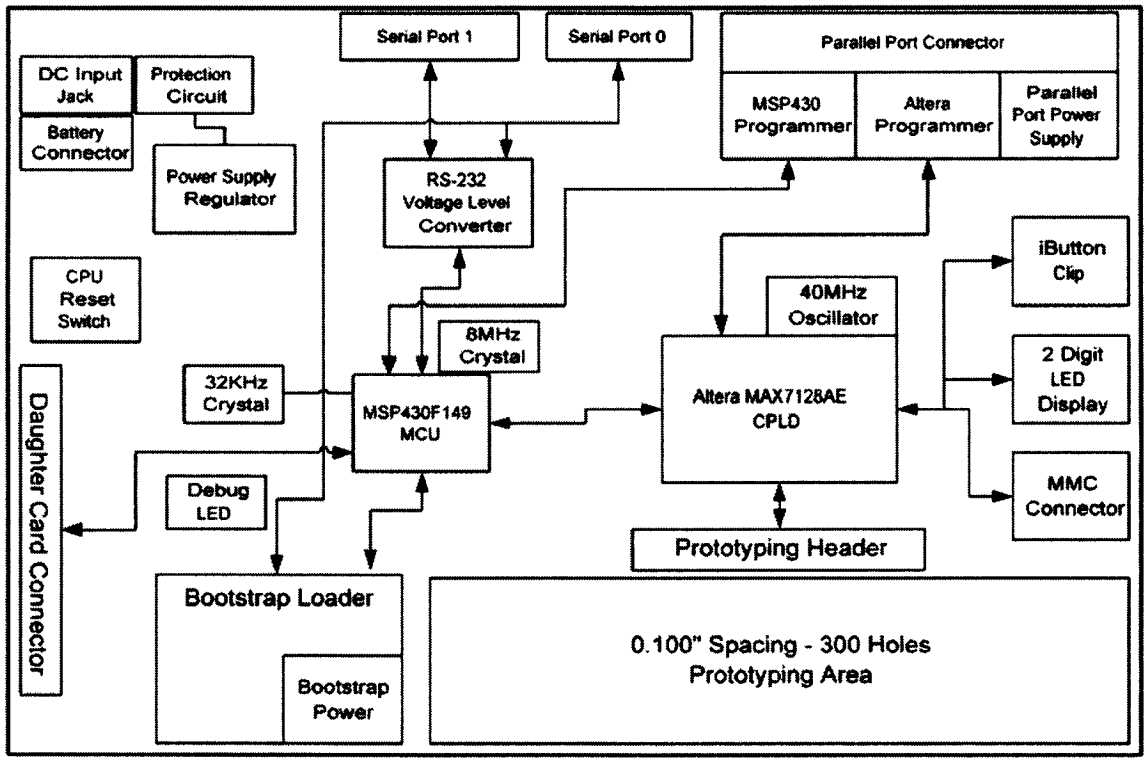


Fig. 4.1 Main Board (McGumps) Block Diagram

hand-assembled prototype was given to the production company as a reference to ensure that no errors existed in the automatic placement procedure. In total, 100 printed circuit boards (PCB) were manufactured and 50 complete student kits were produced. The extra blank PCB are stored at school for student projects or potential future production runs. The price to produce additional PCB is very low and the total price is dominated by the setup fee and PCB mask creation.

The schematics of this board are included in Appendix A.

4.1.1 Power Source Details

The McGumps supply voltage was chosen such that the CPLD and MCU would run at their highest noise margins. The platform needs a regulated 3.3V across the board for powering the electronic components. A direct connection to the power supply input line was provided to support older external peripherals (TTL or older CMOS logic). A second power rail nominally fed by a 5V regulated power supply is routed on the PCB and to the

expansion headers.

The decision to use 3.3V allows full-speed operation of the CPLD and MCU. However, this choice of supply voltage trades off power efficiency since the MCU could be operating at much lower voltages (down to 1.8V). The 3.3V operation of the MCU allows easier interface with older components, important for maximizing the flexibility of the teaching platform.

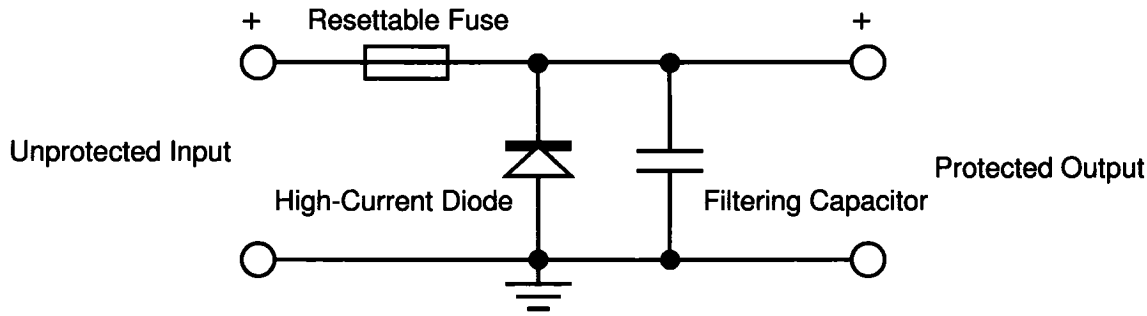


Fig. 4.2 McGumps Polarity Reversal Protection Circuit

As discussed previously, a fused protection circuit was built into the power circuit to prevent damage to the electronic components if the voltage source was accidentally reversed. The simplest protection circuit is a diode that could be inserted in series with the power line. However, the forward voltage drop of the diode introduces some losses and reduce the voltage level for the entire board. To avoid those problems, a diode is placed across the supply rail and ground but is kept reverse-biased in normal operation. To avoid short-circuiting the power source when the polarity is accidentally reversed, a positive temperature coefficient resettable fuse is inserted in series with the input power line. In the event of a power reversal, the fuse will rapidly heat up and open the circuit. A diagram of the circuit is shown in Figure 4.2. The advantage of a resettable fuse is that no technician time is required to fix the boards as a few seconds of delay will re-establish the circuit to its regular operation. At room temperature, the fuse internal resistance is very low, making the voltage drop negligible.

4.1.2 Microcontroller

Based on the review and requirements analysis done in Chapter 2, the MSP430F149 was chosen as the best fit for our application. It features 60k bytes of large block flash and 256

bytes of flash configuration memory along with 2k bytes of RAM. The power consumption is around 500uA at 3.3V for a clock frequency of 1MHz. This particular processor model offers:

- 5 power-saving modes allowing various power/performance tradeoffs to be chosen from;
- Short wakeup time (6 μs) from standby saving energy when using beacons in a sensor network type of application;
- 8 channels of 12-bit analog to digital converters for sensing applications; and
- Two hardware assisted serial communication interfaces supporting both asynchronous and synchronous transfer modes.

4.1.3 Microcontroller Peripherals

Hardware Timers

Hardware timers are necessary to support Carrier Sense Multiple Access with Collision Detection (CSMA-CD). The method allocate time slots for devices to access the communication medium. Accurate timekeeping on the nodes allows reduced timing guard bands and thus make more efficient use of the channel capacity. Thus, on the MSP430F149, a 32 kHz crystal oscillator was installed on the low-frequency oscillator port. This allows the MCU to perform timekeeping in a standby mode by programming an interrupt to occur when the preset timer expires. This feature is essential for beacon networks and the 32 kHz low-power driver is ideal for energy conservation. The timer peripheral can be programmed to run on the low-frequency clock while the CPU and all the internal modules are completely disabled.

Multiple Clock Sources

A second crystal oscillator was connected to the high-speed oscillator interface. It allows the MCU to run at 8 MHz which is the maximum recommended clock frequency. At this speed, the MCU consumes approximately 4mA of current at 3.3V, but can very quickly process information. This MCU can wake up from low-frequency operation, switch to high-frequency mode and perform some computations, for example packet processing or sensor

input gathering. When the processor is performing its operations, all the sensor elements on the node are likely to be active, therefore faster processing translates directly in power savings.

Hardware Watchdog Timer

A hardware watchdog timer is also required for software protection and to ensure that no node is locked up in the field. If the software happens to enter a deadlock state, the watchdog timer will reset the node, avoiding having to send someone to physically perform the reset. This feature becomes more critical if the MCU runs a real-time operating system. Many threads accessing multiple semaphores introduce the possibility of threads deadlocking, especially if the programmers did not anticipate certain combinations of events. The watchdog timer allows the system to return to normal operation after a short delay.

4.1.4 Serial Interface

The two hardware universial synchronous/asynchronous receive transmit (USART) module allows students to configure the module as an asynchronous serial interface to communicate with the PC through a serial line. Alternatively, they can configure the module for internal communication from the processor to peripheral devices. One serial interface is shared between the connection toward the MCU expansion port and toward the PC. The second interface is connected to a serial port going to the PC and to the CPLD. It is possible to program the CPLD as a serial peripheral interface (SPI) device and use it as an expansion module, timer or Pulse Width Modulation (PWM) generator, for example. The combination of a MCU and programmable logic offers the possibility to create multiple lab exercises with the same hardware.

4.1.5 Programmable Logic

Previously discussed was the motivation for including programmable logic in the design of the McGumps board to allow prototyping and expansion of the functionality. The CPLD has two dedicated clock inputs called the GCLK on pins 2 and 83 on the PLCC package. One of the clock input was fed a signal from a 40 MHz high-speed crystal oscillator. This provides accurate timing and fast data processing using the programmable logic cells. The

second clock input is connected to the clock output of the synchrous serial interface of the MCU. This allows high-speed (4 Mbps) transfers of data from the MCU to the CPLD.

The power consumption of the internal logic had to be estimated. Equation 4.1 [28] gives the internal power consumption of the device, assuming it's not driving any output signal.

$$P_{INT} = ICC_{INT} \times VCC \tag{4.1}$$

where

$$ICC_{INT}(mA) = (0.71 \times MC_{TON}) + (0.3 \times (MC_{DEV} - MC_{TON})) + (0.014 \times MC_{USED} \times f_{MAX} \times tog_{LC}) \tag{4.2}$$

And the parameters are given by :

- MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
- MC_{DEV} = Number of macrocells in the device (128 Macrocells in the MAX7128AE)
- MC_{USED} = Total number of macrocells in the design, as reported in the Report File
- f_{MAX} = Highest clock frequency to the device
- tog_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)

One can realize from equation 4.2 [28] that this particular CPLD family is outdated and not suitable for wireless sensor network applications because of its high leakage current at around $0.3 \times MC_{DEV} = 0.3 \times 128 \approx 38mA$. This power can be provided by an external power source such as the AC adapter. Battery powered CPLD applications are also possible but would not run a long time. Previous student experience with the Altera Max family was deemed more important than the technical specifications of the CPLD. On the other hand, the static current consumption from a newer family of CPLD, such as the Xilinx Coolrunner-II and similar 128-macrocell device, is around 30 μA. This represents over a thousand-fold increase in energy efficiency. Additionaly, the core voltage of the Coolrunner-II is set at 1.8V so the power savings of using such a family could have been tremendous. Knowing the energy inefficiency of the MAX7128AE, a jumper was installed on the PCB

to totally disable it when low-power consumption is required. This is feasible because the MAX7000AE tolerates voltages on the I/O pins even when the core is not powered (hot-socketing). A device without this feature will interfere with the operation of the board since the internal protection diodes on the CPLD I/O pads will become forward biased and indirectly power the core with an unstable voltage level leading to erratic operation or the logic elements inside the CPLD.

4.1.6 Integrated Device Programmer

The JTAG interface is a standard used for testing integrated circuits at the pin level. Lately, many microcontroller manufacturers have been adding to the JTAG test registers features to allow debugging of embedded microcontrollers. The JTAG can also be used to re-program configurable devices such as our Altera CPLD.

Using standard 74HC244 buffers, a voltage level translator was built based on reference designs published by Olimex [30] and Altera [29] to transfer the signals from the parallel port interface (5V) to the supply rail of the McGumps board (Nominally 3.3V). The main challenge was to merge the two interfaces in such a way that either one can be used to program the MCU or the CPLD without changing jumpers on the main board. Furthermore, an option was added in CPLD programming mode such that the JTAG chain can be made to pass first through the MCU and then through the CPLD in a daisy chain. This offers the opportunity to introduce the concept of JTAG device chain to students with a practical example. Unfortunately, the JTAG standard does not cover advanced modes such as MCU programming and debugging. Thus if two devices are present in the JTAG chain, the MSP430 software toolchain will not be able to debug the CPU and will signal an error to the user. Another jumper configuration separate the JTAG chains into two independant ones to avoid this issue.

4.1.7 Multimedia Card and iButton

The multimedia card (MMC) and iButton interfaces presented in Section 3.3.3 connect directly to the CPLD. It is then possible to implement a routing path from the MCU to the iButton or the MMC card. Another interesting use of the CPLD is to act as an expansion device translating the iButton interface to a serial interface compatible with the MCU. The flexibility inherent to the design allows many laboratories to be designed using

the two expansion connectors. In a sensor network type of application, the iButton can host encryption keys or a temperature sensor while the MMC card can be used to log data between transfers to the network coordinator.

4.2 Touch Screen Board and S1D13700 LCD Controller IC

This board was developed as an expansion module for the McGumps board, enabling the support of larger and more sophisticated user interfaces. It uses the Epson S1D13700 LCD controller chip which contains 32kB of screen buffer memory. It can drive large LCD panels up to 320x240 and supports grayscale display. The graphical display selected for our application is a 160x160 dot matrix panel with integrated touch panel.

4.2.1 Voltage Booster

The graphical display requires a relatively high voltage (around 20 V) to polarize the LCD segments, thus a voltage booster circuit was designed and added to the screen board. The voltage booster is based on a small oscillator IC and an inductor. The oscillator charges the inductor and then rapidly opens the circuit creating a voltage spike that is directed to an output capacitor through a Schottky diode. The oscillator circuit has a feedback input and uses Pulse Width Modulation (PWM) to regulate the output voltage. The voltage booster circuit can provide a few milliamperes of current at the high-voltage output, which is sufficient to supply the LCD bias current. Large resistors on the feedback network were put in place to reduce the static power consumption.

In series with the resistor network is a digital potentimeter that can be controlled by the MCU but also has internal wiper position memory. This setup is interesting because the voltage used to bias the LCD display also controls the contrast. Therefore the user's experience is enhanced by the presence of a digital trimmer which allows the user to set the contrast of the display from the application software. Furthermore, the digital potentiometer was selected with non-volatile wiper position memory such that when the device is powered down and up, it can maintain the same constrast level. A control input allowing the LCD bias generator to be de-activated was added to allow standby power savings under MCU control. The detailed schematic can be found in Appendix B.

4.2.2 LCD Panel Interface

The touch screen module is connected through a 18-pin flat ribbon cable that carries the digital pixel data stream, synchronization pulses, LCD bias voltage, and touch panel resistive readout. This single ribbon contains all the required signals and simplifies the installation and mounting of the LCD module.

4.3 RF Transceiver Board

The RF transceiver board was named McZig as a shorthand notation for the McGill University Zigbee board. It features a 40-pin keyed connector that fits into the McGumps main board, a RF transceiver and associated passive components, a balanced-to-unbalanced (balun) circuit and a small-footprint custom-designed printed antenna.

The CC2420 RF transceiver from Chipcon was selected because it features short startup times and fast frequency settling as described in the previous chapter. These features allow power savings since the transceiver would be stable and operative shortly after startup, thus usable for communication. The most problematic element in this choice of transceiver was the Quad Flat Pack No Lead (QFN) package type. The main concern was the assembly of the printed circuit board, which we had to be done in our school laboratory. After researching various techniques for soldering modern packages, it was decided that the transceiver board would be reflowed using a toaster oven with a controlled temperature profile similar to the one used in the industry on larger scale production lines. The only drawback from this method is the time taken to put the solder paste on the small surface mount pads, manual placement of parts and thourough inspection of the reflowed board. However, the cost and quick turnaround afforded by this technique makes it very suitable for this type of projects and allow modern packages to be economically prototyped.

This section will cover the antenna design methodology, the antenna selection and design and the balun circuit analysis. The reader may refer to Appendix C for the schematic and detailed layout of the McZig board.

4.3.1 Antenna Design Methodology

As discussed in Chapter 3, we have chosen to implement a printed antenna. The operation of the tranceiver at 2.45 GHz forces the designer to consider the high-frequency behavior of

the circuit. The PCB trace width, height above the ground plane and the PCB dielectric material all contribute to the PCB trace impedance. Variations in the impedance of the trace cause reflections in the power propagating in the traces, thus the impedance discontinuities must be minimized. At 2.45 GHz, the wavelength in free space is around 12.2 cm. The PCB's higher dielectric constant reduces the wavelength [37]. For the dielectric material used for the production of McZig, the dielectric constant was 3.48 resulting in a wavelength of about $\frac{\lambda_0}{\sqrt{\epsilon_r}} = \frac{12.2}{\sqrt{3.48}} \approx 6.54cm$. This reduction occurs as the wave travel inside the dielectric under the microstrip transmission line. Problems may arise when the length of printed traces become comparable to the wavelength and this makes the circuit analysis quite challenging.

The feed line to the antenna has a size which represents a significant portion of the wavelength λ. The transmission line effects further complicate the design of the circuit since the position of components along the length of the circuit has a significant impact on the circuit overall performance and characteristics. Computer Assisted Design (CAD) tools for microwave engineering offered tremendous assistance in helping to characterize the effect of the dielectric and trace geometry.

Performing full three-dimensional electromagnetic analysis contributes to a better understanding of the effect of the limited size of the ground plane. In the design of the transceiver circuit, the planar electromagnetic simulator [38] Agilent Momentum and the full wave simulator Ansoft from HFSS were used to characterize the printed antenna of the McZig board.

The transceiver board was designed following the design flow outlined in our publication presented at the 2005 Design Automation Conference [24]. To build the prototype, we have selected the following antenna to be integrated on the PCB: a dipole with built-in balun circuit based on a clever design from a Microwave Journal publication [39]. The antenna was improved by my colleague Chun Yiu Chu from the Computational Electromagnetic Software group at McGill University. The new design offers a much reduced PCB area usage while keeping most of the initial omnidirectionnal radiation pattern and antenna bandwidth.

4.3.2 Intrinsic Antenna Characteristics

For omnidirectional antennas, the gain is the most important parameter to consider since the antenna transmits in all directions with approximately the same intensity. Furthermore, the antenna efficiency and radiation pattern (especially the uniformity in the antenna directivity) were found to be the two most critical elements of an antenna used in wireless sensor networks. Although many antenna publications clearly illustrate the radiation pattern and other characteristics of their design, the antenna efficiency is seldom mentioned. Antenna manufacturer also tend to avoid publishing the efficiency, since it is not needed to compute the range. It is possible to recover the efficiency from a mathematical analysis of the radiation pattern, but this procedure is time-consuming and not so accurate if only a few "cuts" of the radiation pattern are given for the analysis. This information is nevertheless important to compare antennas.

Maximizing the antenna efficiency decreases the sensor node density, but that information is not always available. Since the efficiency of an antenna is a measure of intrinsic design considerations, commercial vendor have no incentive to mention it since there is nothing the buyer can do to improve it. However choosing to design a printed antenna directly on the sensor node PCB allows us to gain control over this parameter. As with any engineering designs, higher antenna efficiency translate into more expensive dielectric material and higher costs. On the other hand, integrating the antenna on the PCB reduces the bill of material (BOM) cost and the savings can be re-invested in improvements to the antenna efficiency.

To optimize the efficiency, the RO4350B dielectric material from Rogers Corporation was selected for its very low loss (low tan δ), relatively low cost and compatiblity with the FR4 manufacturing process. Table 4.1 illustrates the properties of selected dielectric materials suitable for PCB fabrication.

Table 4.1 PCB Materials Electrical Properties

Material	Tan δ	ϵ_r	ϵ_r tol
FR4	0.020	4.2-4.8	13.6%
RO4350B	0.0031	3.48	2.8%
RO3006	0.0020	6.15	4.8%
RO3010	0.0023	10.2	5.8%

The table also highlights the very high dielectic constant ϵ_r that is available to the

designer. A high dielectric constant translates into smaller antennas, which could be important when faced with tight area constraints. However, one must be aware that small antenna structures have narrow copper traces carrying the RF currents. This leads to higher resistance, therefore increases the antenna losses and consequently decreases the overall antenna efficiency. Specialized dielectric laminates also offer the advantage of tighter tolerances on the dielectric constant and the thickness of the dielectric, which ensures that the antenna will resonnate at a frequency close to the one predicted by the electromagnetic simulation model.

4.3.3 Antenna Range

Our printed antenna designed to fulfill the requirements of a low-cost and robust implementation of the wireless node was based on a target sensor node range of around 50 m. The tranceiver can provide an output power of 0 dBm[1] (P_t) at its maximum power level. The transceiver and receiver antenna gain G_t and G_r respectively can be assumed to be at least 0 dB, as a theoretical isotropic radiator. A conservative estimate of the balun loss at 1 dB must be deducted from the antenna gains. At a range of 100 m, we can obtain the received power P_r from Friis [37] transmission formula shown in Equation 4.3. R is the range in kilometers and f is the frequency of operation in megahertz, in our case 2450 MHz.

$$\begin{aligned} P_r(dBm) &= P_t(dBm) + G_t(dB) + G_r(dB) - 20 \times logR(km) - 20 \times logf(MHz) - 32.44 \\ P_r(dBm) &= 0\ dBm + (0-1) + (0-1) - 20 \times log0.1 - 20 \times log2400 - 32.44 \\ P_r(dBm) &= 0\ dBm - 1 - 1 + 20 - 67 - 32.44 \approx -81.4\ dBm \end{aligned} \quad (4.3)$$

The receiver sensitivity level of -90 dBm [14] minus the received power level of -81.4 dBm (approximately 7 pW) will result in a link margin of slightly less than 9 dB at a 100m range. In a typical environment, attenuation from walls and path reflections will reduce the link margin. Typical attenuation from walls can vary between 5 dB and 10 dB depending on the material and the presence of metallic reinforcements [40, p.166]. The above analysis shows that our 50m range goal is clearly acheivable and will result in roughly 15 dB of link margin at that range since halving the distance adds 6dB of received power.

[1]The dBm unit is a reference power level of 1 milliwatt, thus a 0 dBm power level is equivalent to a transmit power of 1 mW

The antenna gain can be designed to be greater than 0 dBi[2]. The best antenna for a general purpose wireless sensor node is a relatively omnidirectional antenna with some gain over the isotropic radiator. A printed dipole antenna is an interesting candidate for the wireless transceiver board as it offers around 3 dB of gain over the isotropic radiator (gain of 3dBi) while keeping an omnidirectionnal radiation pattern[3]

4.3.4 Balun Circuit

The RF transceiver has a differential antenna output. Differential antennas are expensive to characterize since the equipment for differential measurement is much more complex than for single-ended ones. We chose to integrate a balun circuit to convert the signal from differential to single-ended mode. The balun circuit is based on the manufacturer's reccomendation which also includes the DC biasing of the RF power amplifier integrated in the CC2420 transceiver. We have chosen to integrate a printed dipole antenna on the transceiver board because of its good radiation characteristics. Dipole antennas are differential by nature, thus a second balun is integrated into the antenna structure to convert from the single-ended propagation mode of the antenna feed line to the differential propagation mode in the dipole arms. The two transformations cancel out, but the benefit is that in the middle between the RFIC and the dipole arms, the signal is available in a single-ended mode that can be connected to lower cost RF equipment for analysis. The balun circuit and its integration is illustrated in Figure 4.3.

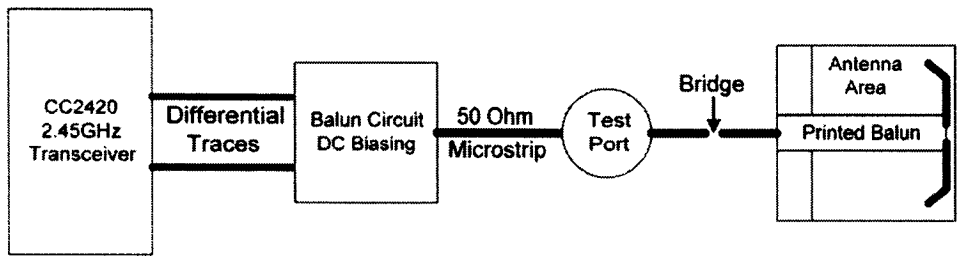


Fig. 4.3 System Level Balun Antenna Feed Network and Balun

The diagram shows a bridge in the antenna feed line[4]. In practice, the bridge must

[2]0 dBi is the power level when using an isotropic radiator antenna as a reference

[3]Most manufacturer's datasheet use the dBi unit, but sometimes, it is useful to see how the antenna gain compares to the ideal dipole since the isotropic radiator is not a physical device. In this case, the dBd unit uses the ideal dipole antenna as a reference

[4]The schematic annotates it as a 0 Ω 1206 package size resistor

be shorted with a short length of copper tape. The tape should be of the same width as the microstrip feed line and should be pressed hard against the dielectric to minimise the impedance discontinuity. There are two reasons for this jumper. The first is to allow the SMA test port to be used without having the antenna load when measuring the power output from the transceiver. The second reason is to avoid a Design Rule Check (DRC) error from the PCB design tool because our toolset is not aware of microwave component behavior. Since the antenna analyzed as a low-frequency lumped component is a short-circuit for the DRC program, a jumper has to be present to separate the net in two parts and allow the board to be routed.

Antenna Prototype

After the design process was completed, the McZig PCB were fabricated by a specialized company using the Rogers RO4350B dielectric PCB material. The assembly was done in the school laboratory using manual placement of the parts and "toaster oven" reflow soldering. Figure 4.4 shows the final transceiver board simulation model and photograph of the completely assembled McZig board.

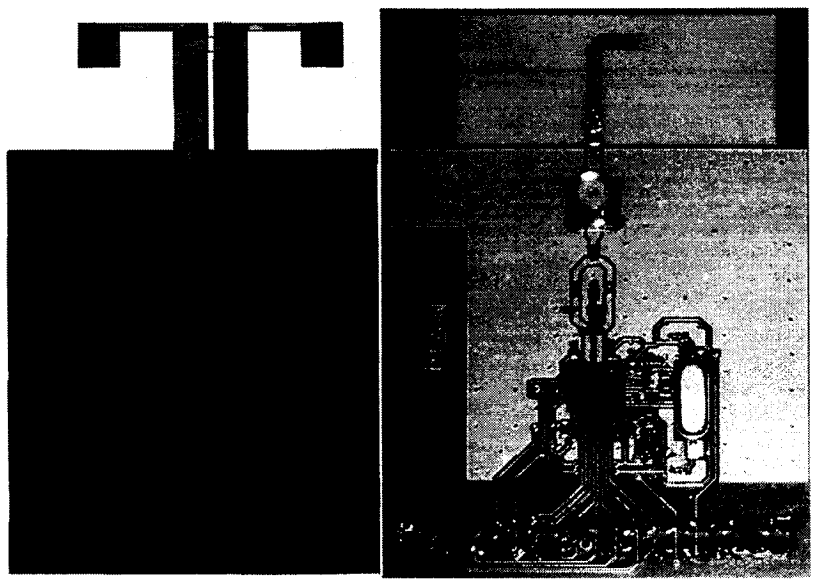


Fig. 4.4 McZig Simulation Model and Photograph

The simulation model shows peak current density and the lighter areas of the model represent the strongest current accumulation in the dipole resonnant mode of operation.

Note that in the figure, the model shows a slight design modification, the taper in the ground plane near the antenna feed connection. This was modeled after fabrication to slightly improve the match to the antenna by providing a smoother impedance transition. The photograph is representative of the unaltered McZig boards. Note also the removal of the green soldermask around the antenna. This was done to ensure a closer match between simulation and fabrication as the soldermasking process is not very well characterized and can introduce variations in the antenna resonnant frequency due to the added dielectric layer.

Antenna Input Reflection Coefficient

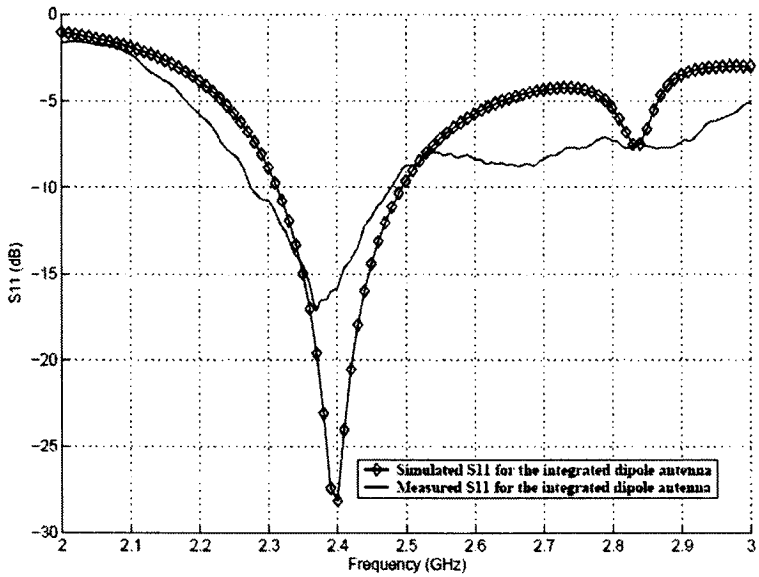


Fig. 4.5 Antenna predicted and Measured S11 Response

After fabrication, the capacitor at the balun output was removed to isolate the antenna and a measurement of the input reflection coefficient (S11) of the antenna was measured to validate the performance of the circuit and its match with the simulation model. Figure 4.5 shows the very good match between the model and the measured values. The main differences between the model and the measured values are caused by the reflections in the measurement room. In the simulation model, the boundary conditions are set to absorb all electromagnetic energy radiated from the antenna. Our university does not have an anechoic room to measure antenna performance, so any metallic objects present in the

measurement room (bench, wall struts) will reflect some of the power fed into the antenna by the vector network analyzer. This results in a reflection coefficient slightly lower than -15 dB at resonance compared to almost -30 dB for the model. For most practical purposes an antenna is considered well tuned when the S11 is below -10dB. Our antenna was designed to have a resonant frequency slightly under 2.45 GHz for the simple reason that if there was any discrepancy between the simulation model and the corresponding fabricated prototype, we wanted the resonant frequency to be lower than the actual center frequency of the 802.15.4 2.4 GHz band. It is much simpler to fix a low resonant frequency by removing some copper with a sharp knife, which would tune the antenna to a higher frequency. On the other hand, adding copper to the antenna elements would have been more problematic. In the resulting prototype, the measured resonant frequency is slightly lower than predicted by the electromagnetic simulator by 1.8%.

Antenna Radiation Pattern

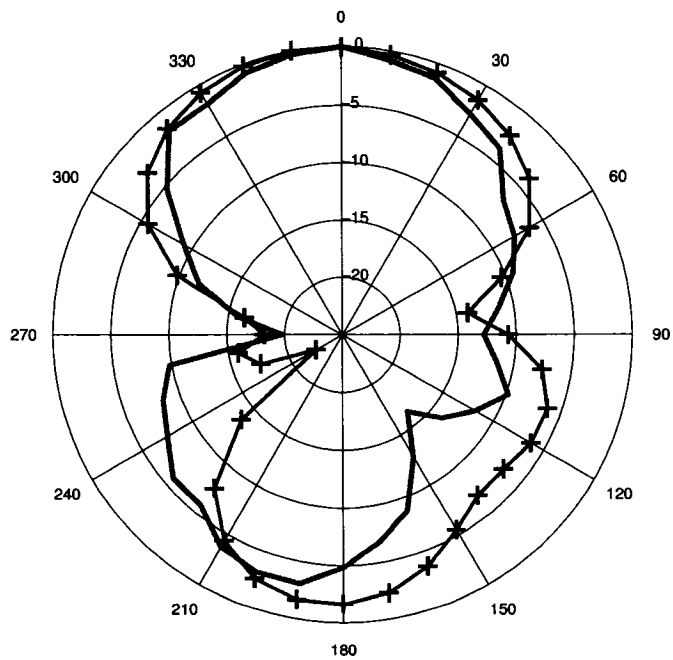


Fig. 4.6 Normalized E-Field Intensity Along the E-Plane (dB)

Figure 4.6 shows the electric far-field (E-Field) intensity pattern along the dipole electric plane (E-plane) obtained by simulation and lab measurements. The simulation and measured intensity are normalized to 0 dB at their peak (in this case at 0°). The two nulls

at around 90° and 270° are expected for the dipole antenna. The pattern should normally be totally symmetric at 0° and 180°, but the PCB ground plane of the transceiver introduces some distortion. Furthermore, the measurement room used to gather the data was not anechoic and contained metallic structures, therefore introduced some distortion in the measured radiation pattern. Nevertheless, the measurements do coincide well enough with the simulation within our measurement capabilities.

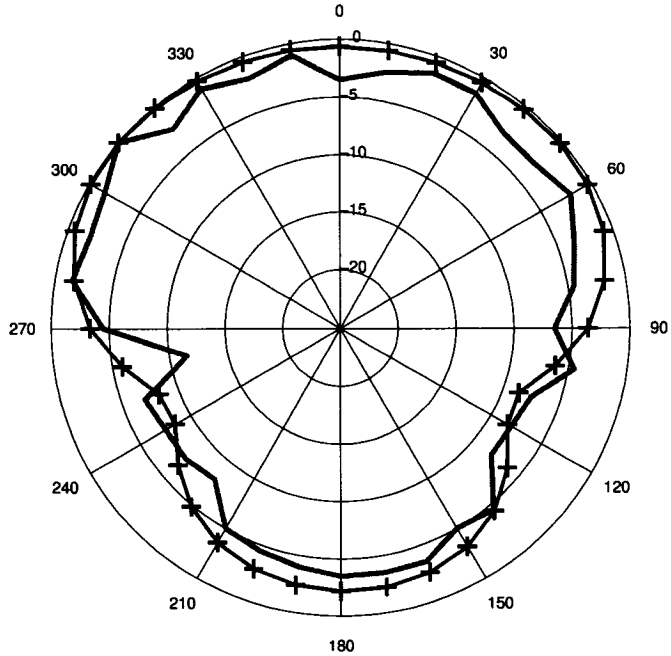


Fig. 4.7 Normalized E-Field Pattern on the H-Plane (dB)

Figure 4.7 shows the E-Field intensity measured and simulated but this time along the dipole magnetic plane (H-Plane)[5]. This measurement is the most relevant to the design of the sensor node. By design, the receiver antenna should be polarized such that it receives the E-Field from the dipole along the H-Plane. This offers the most omnidirectional radiation pattern and has no nulls in the angular coverage. The antenna model and the measurements did predict the slight frontal gain of the antenna. This is due to the ground plane of the PCB acting as a reflector to the dipole which redirects some of the energy towards the front.

This short analysis of the printed antenna and its measurements would not do justice

[5]For a complete discussion about dipole radiation measurements, the reader should refer to pages 24–37 of Antenna Theory and Design by Warren L. Stutzman [37]

to the complexity and large amount of work required to design and integrate the printed antenna. This joint effort between this author and Chun Yiu Chu from the computational electromagnetic group at McGill represents many months of research, prototype creation and testing. For a complete and in-depth analysis of the printed dipole, its integration, performance enhancements and CAD tools consideration, the reader is refered to Mr. Chu's master's thesis [41, Chapter 7].

4.3.5 Balun Circuit Performance Degradation and Analysis

After the fabrication of the wireless transceiver was completed, the power was measured at the output of the transceiver. The balun circuit was expected to lose a few tenth of a dB of power (a conservative loss of 1dB was estimated in our link budget). However, when the tranceiver output power was measured with a spectrum analyzer and the device put in single carrier test mode, the balun was found to lose about 8 dB. The balun circuit was given by Chipcon as a reference design, but no explanation was given for its operation. While the printed antenna performed very well, the overall loss in the system made an attainable range of 60 meters in a conference center environment. While this is not bad, considering that 50m is sufficient for our use of the transceiver, an analysis is necessary to find out why the balun circuit is so lossy.

Investigation

The only notable difference between the reference balun design [14, p. 19] and the McZig implementation was in the PCB layout of the balun circuit since all the components were identical. To pinpoint the problem, the balun circuit was drawn in Agilent Design System (ADS) and the model is shown in Figure 4.8. It includes parasitic elements for all components based on electronic models provided by the Murata company. At the left is the antenna port and at the right is the differential port with the 115+j180 Ω differential impedance modeling the CC2420 impedance. Added to the model are parasitic capacitance in the two differential line and on the antenna feed line.

The small trace length mismatch between the reference design and the fabricated board was not an issue. However, the parasitic capacitance introduced by the larger PCB traces did differ significantly between the fabricated transceiver board and the one estimated from

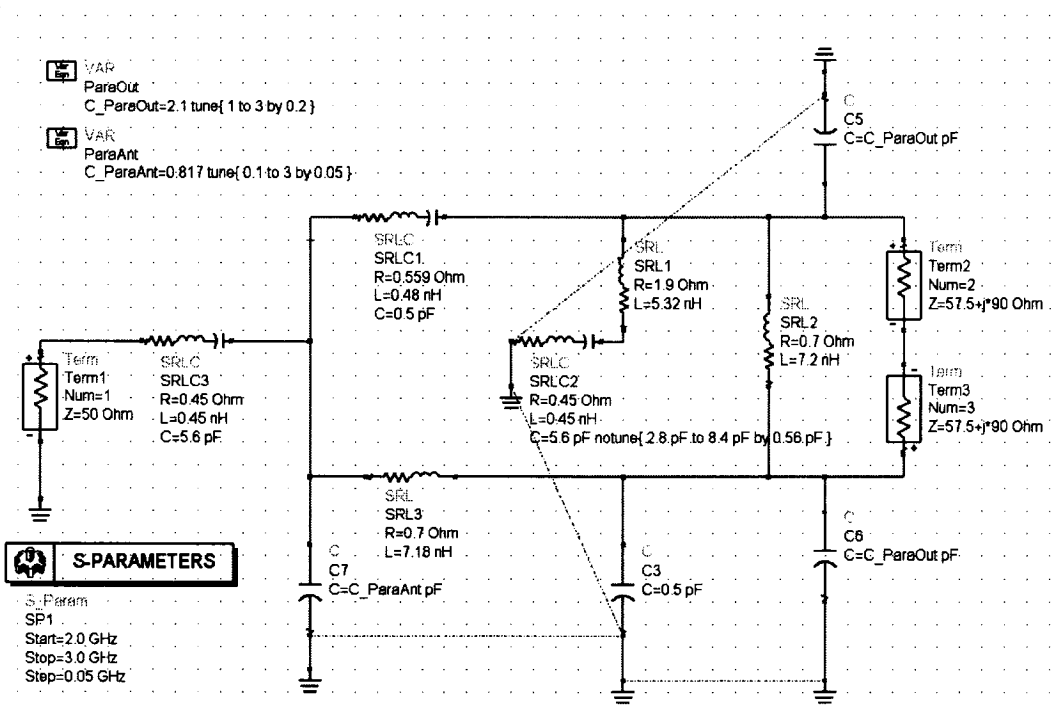


Fig. 4.8 ADS Model of the RF Transceiver Board Balun Circuit

the Chipcon reference design[6]. Using a very sensitive RLC meter, the parasitic capacitance on each branch of the differential portion of the balun circuit was measured to be around 3.5 pF. Figure 4.9 shows the balun circuit operation with a nominal 2.1 pF parasitic capacitance on each differential nets (connected to the differential port) of the balun circuit. The balun circuit is operating properly with that amount of parasitic capacitance. The two S11 curves show the center frequency of the balun circuit at 2.45 GHz with a 179.9 degrees phase opposition indicated by the markers M2 and M3 in the Smith chart plot. The balun has a 0.4dB loss in each branch since we do expect a -3dB drop due to the differential nature of the circuit (the power is split equally between each branch S12, S13). The small loss is due to the components whose models include resistive losses and to the inevitable impedance mismatch that occurs when commercial component values are used in the design.

However, by changing the model to include a 3.5 pF parasitic capacitance as measured

[6]The Chipcon reference design makes no mention the parasitic capacitance of the balun circuit PCB traces

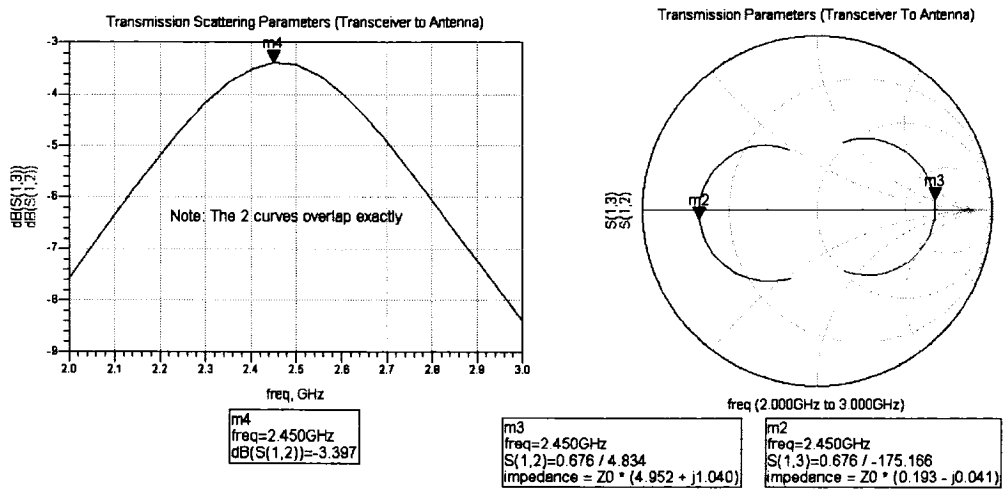


Fig. 4.9 Balun Circuit Simulation with 2.1 pF Parasitic Capacitance

on our prototype board, the balun circuit does not operate properly in the 2.4–2.5 GHz band as shown on Figure 4.10. The ADS model simulation identified the cause of the problem as an incorrect tuning of the balun circuit to a lower frequency of operation. Unfortunately, the high setup cost for production of PCB on specialized dielectric material and the good range of the current version of the McZig board (around 60m indoors) did not justify the fabrication of a new board with an improved balun circuit. The simulation of the balun components and the full modeling of the RF circuit is now part of our design methodology to avoid revisiting the same problems in future designs.

4.4 PCB Design

Leaving the microwave design techniques, this section elaborates on the methods used to design the digital PCB and the general rules applied to preserve the signal integrity and to limit electromagnetic emissions.

4.4.1 PCB Design Flow and Tools

The PCB Design tools used in this project was the Expedition PCB family of tools by Mentor Graphics. It provides support for large-scale design and incorporate a central li-

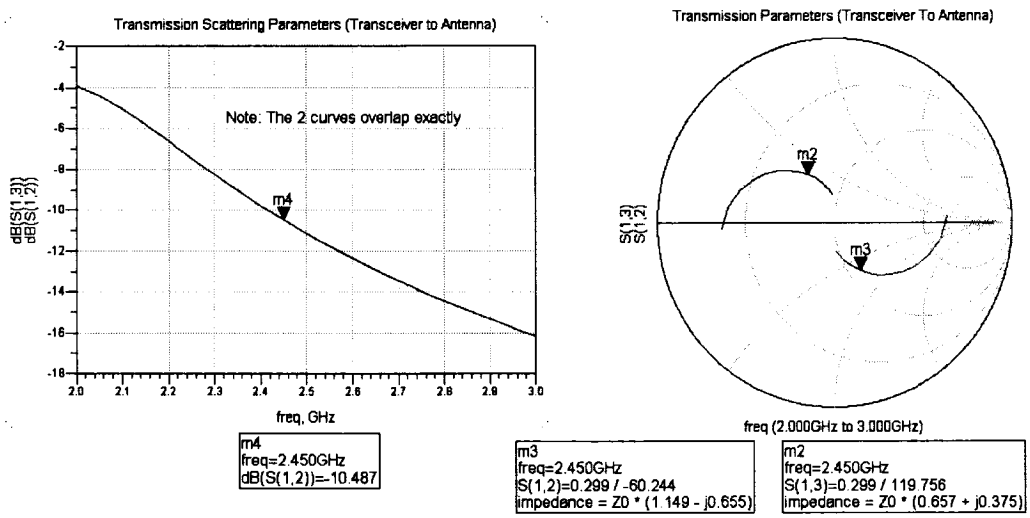


Fig. 4.10 Balun Circuit Simulation with 3.5 pF Parasitic Capacitance

brary to manage the parts and their associated information. This toolset is widely used in the industry to handle complex boards and challenging high-speed layouts. It supports hierarchical design methods and follows very strict schematic and layout rules. This considerably reduces the possibility of errors creeping into the design of the board. However the numerous safety mechanisms built in the toolset and its industry-oriented design flow made the learning curve quite steep and required many months of work to acheive an adequate level of proficiency.

4.4.2 Design Methods to Reduce Electromagnetic Interference (EMI)

At relatively low frequencies such as the 8 MHz, a PCB trace connecting two devices on a small board can be viewed as a wire and the complexity of the analysis is minimal. However, as the frequency increases or if the MCU or CPLD outputs very fast edges, the frequency content of the signal (harmonics) extend to very high frequencies. In that case, a more complete analysis is required.

Short Current Return Path

At high frequencies, it becomes important to provide a short return path for the current flowing in the PCB trace [20]. Failure to provide a short and low impedance return path will result in air being used as a return path, which in other words means that the board will be radiating some energy into space. This phenomenon is called Electromagnetic Interference (EMI). EMI reduction is a very complex process involving analysis at many levels of the design process.

Decoupling capacitors

Decoupling capacitors provide local storage of energy allowing shorter paths for power supply return currents. Current will flow from the decoupling capacitor to the device instead of coming from a more distant power supply line using a higher impedance path, resulting in significantly reduced EMI. At low frequency, capacitors act as low-pass filters.

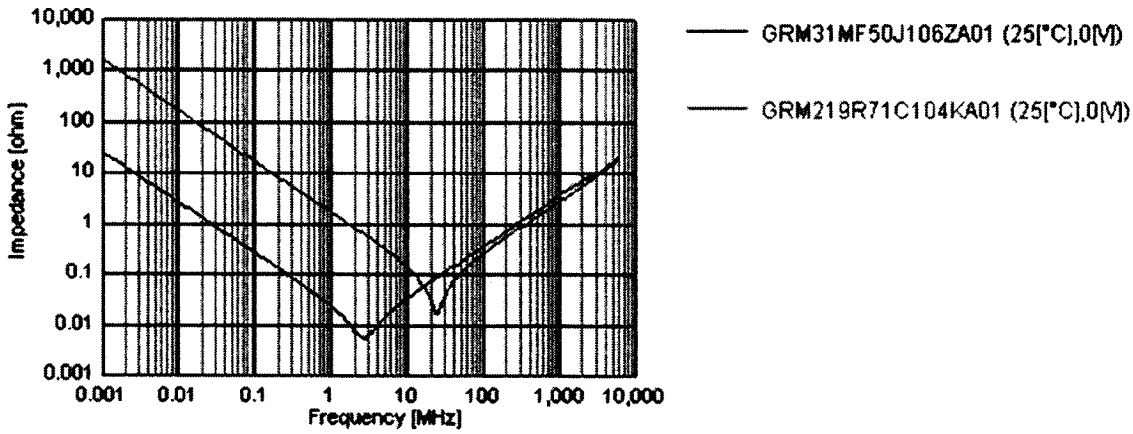


Fig. 4.11 Impedance of 10μF and 0.1μF versus frequency

However, when they operate above their resonnant frequency, they start to become inductive. This is unfortunate as it means that their decoupling effect is diminishing at high frequencies as shown in Figure 4.11 [42]. The figure shows the 10uF ceramic capacitor reaches a lowest impedance at around 3MHz, beyond which point, its impedance increases with frequency since its inductance starts to dominate. The 0.1uF plotted in Figure 4.11, counterintuitively has a lower impedance than the 10uF after around 15 MHz. Therefore, even with a much smaller capacitance, the decoupling effect of the 0.1uF is better at fre-

quencies around 20 MHz. The self-resonnant frequency of capacitors is dependant on their packaging (surface-mount is better than axial components with long inductive leads) and their internal dielectric material. Therefore for EMI reduction, proper selection of bypass capacitors requires careful analysis of which harmonics in the power supply one needs to attenuate.

Multi-layers PCB

Multi-layer PCB includes a Vcc and a Ground plane to further reduce EMI. The power and ground planes provide an uninterrupted return path for high-speed signals and a low impedance paths from the power source allowing significant reduction in EMI. The close proximity and large surface of the two planes also create a very high quality capacitor (high Q-factor). However, trying to following all the EMI reduction guidelines on a 2-layer PCB (used for cost reduction on the McGumps board) introduces many compromises. Keeping short return paths and providing proper decoupling is the only alternative to compensate for the missing power supply copper planes in a 2-layers board. Fortunately, the low-power design of the MCU and the very high noise margins afforded by the 3.3V supply allow compromises to be taken. Furthermore, the MCU does not have high slew-rate at its outputs and the CPLD can be programmed to increase the rise time of the output pad drivers, which limits the EMI emissions. Commercial products have to limit their emissions under certain levels and must therefore pay attention to EMI issues at the design level. Each country has their own limitations for compliance to their standards.

4.4.3 Signal Integrity

Reducing the radio emissions contributes to a better board signal integrity. Proper decoupling and small power loops reduce the tendency for signal transitions to use other signal lines as return paths for the current. The only area on the McGumps board where the frequency is very high is around the CPLD clock. The 40 MHz oscillator frequency is rather high for a 2-layer board, so care was taken to prevent any sensitive signals from crossing the oscillator clock path. Most designs using the CPLD would have the clock divided internally and use a lower-frequency derivative of the 40 MHz clock for its I/O operations.

4.5 Lithium-Ion-Polymer Ultra-Low Power Prototype

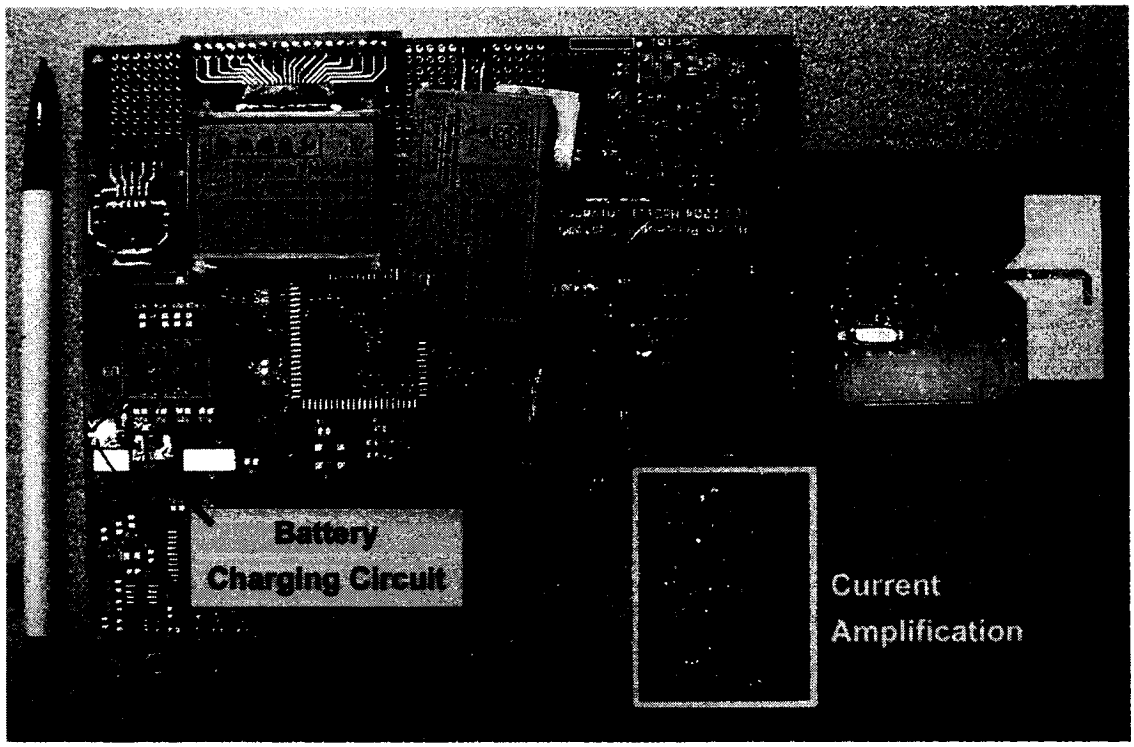


Fig. 4.12 Ultra-Low Power Version of McGumps with LCD Display

In order to pursue advanced research in ultra-low power systems for wireless sensor networks, a more power efficient design was created. The production version of McGumps was unsuitable due to its high static power consumption. Using an unpopulated McGumps PCB, a new experimentation platform was rapidly developed, re-using some portions of the layout. The resulting prototype is shown in Figure 4.12. Added to the McGumps board are: a low-power character-based LCD display with built-in controller, a rechargable lithium-ion polymer battery, a charging circuit, a McZig transceiver and a current measuring circuit.

Instead of the original MSP430F149, this board uses a pin-compatible MSP430F1612 microcontroller. It gives the sensor node more than twice the RAM memory allowing more complex algorithms to be implemented. To reduce power usage, the node operates at 2.7 V. This voltage level is adequate for both the McZig board and the LCD display. Most of the programming and CPLD hardware has not been included on this prototype in order to

reduce standby power consumption.

4.5.1 Lithium Battery and Charging Circuit

From the study detailed in Section 2.1.3, a lithium-based battery was selected as the best candidate for powering the new design. The lithium-ion battery is an OEM part used in the Nintendo GameBoy Advance SP, a commercial portable gaming console. The availability and the low price of these off-the-shelf batteries present numerous advantages should this unit be needed in large numbers. The battery provides 780 mAh of capacity at a nominal voltage of 3.5 V, which translates into approximately 40 hours of continuous operation with the RF transceiver and screen always active. Using low power modes and sleep periods, the battery life can be extended for such a long time that the self-discharge of the battery would start to dominate. For research purposes, 40 hours of full operation is sufficient and the battery is easily re-chargeable. In this prototype, a linear low-drop voltage regulator was used. For a better performance, a charge pump step-down regulator would provide higher conversion efficiency.

Rechargeable lithium based batteries need some very specific charging circuit to ensure a long lifetime due to its chemistry. Overcharging or over-discharging a lithium battery can lead to the formation of metallic lithium inside the battery and pose fire hazards. Therefore, in this experimental prototype, a charging circuit was built to ensure that the lithium-ion polymer battery would not suffer from overcharging. The design is based on a charge controller IC, the Maxim MAX1555. This device ensures that first, at low battery voltage, the charger only outputs a small current, around C/10 where C is the battery capacity. This is to ensure that deeply discharged cell's electrolyte is not damaged by strong initial currents. When the voltage reaches a certain threshold (in this case 2.9 V), the current can then be increased up to C. In our case, the maximum current provided by the charging circuit is around C/2 which means that the battery should be completely charged in about 2 hours. When the battery voltage reaches 4.0 V, the current decreases linearly until the voltage reaches 4.2 V. At that point the battery is completely recharged. Lithium-based batteries require very accurate charging and this IC provides all the required current limiting and voltage monitoring and occupy very little space on the PCB. Under-discharging the battery is prevented using the battery supply monitor provided on the MCU.

4.5.2 Current Measurement

The current amplification circuit consists of instrument amplifier and a precise shunt resistor. It provides a direct measure of the dynamic current used by the board by sampling the small voltage drop across the shunt resistor. The differential amplifier also removes the voltage offset present at the resistor terminals and effectively eliminates common mode noise. Figure 4.13 shows a typical capture of the current consumption during various modes of operation of the MCU and RF transceiver card. Some digital I/O ports of the MCU were used to indicate in which mode the processor was running by driving various constants during code execution.

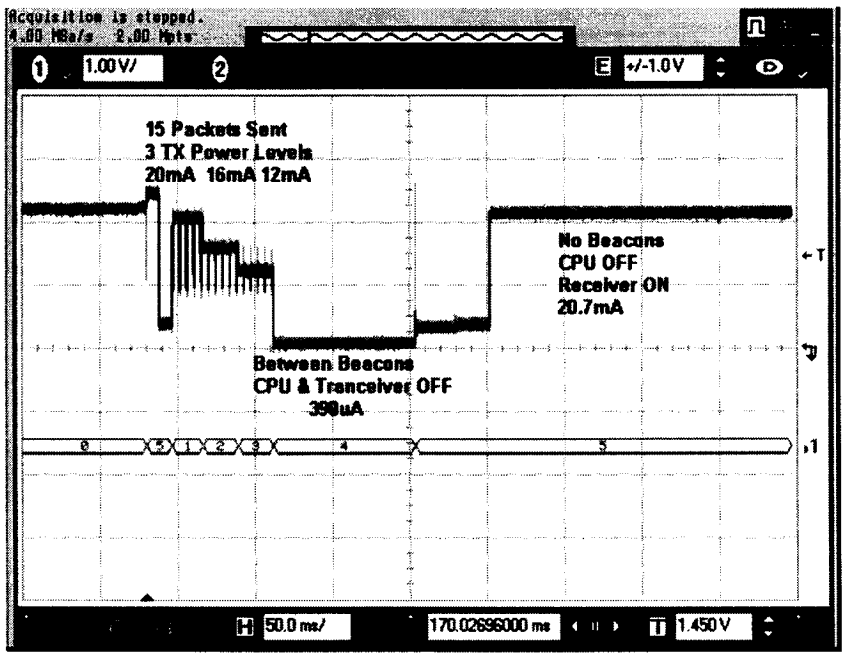


Fig. 4.13 Dynamic current consumption of Low-Power Sensor Node

Chapter 5

Applications of the Wireless Systems Development Platform

This chapter presents the applications that make use of the wireless systems development platform developped during this master's project.

5.1 Microprocessor Systems Teaching Kit

The McGumps board is designed to be the platform for teaching the microprocessor systems course and was used during three complete semesters by over 150 students. Only one defective board was found from the 50 manufactured boards and it was traced back to a cold solder joint on one of the expansion port pin. The problem was promptly fixed by the university technical staff and the board was put back in service. Figure 5.1 shows a complete lab kit including a McGumps board, small-screen LCD display with touch screen and McZig wireless board. At the time of this writing, students are only using the McGumps and LCD display since the McZig has not yet been mass produced. Figure 5.2 shows the easily noticeable kit box with bright red color and white lettering. This packaging primarily provides protection to the content and easy storage between semesters.

5.2 Microprocessor Systems Laboratory Course

The McGumps board is used to teach the fundamentals of assembly programming and 'C' programming on microcontrollers. Among other concepts, students are exposed to the

Fig. 5.1 Microprocessor Systems Teaching Kit

calling convention used by the 'C' compiler to pass and return parameters to assembly programs. The MSP430 architecture and its large number of registers allow students to experiment with a mix of 'C' and assembly without having to perform intricate context savings as it was the case with the Motorola HC12 architecture.

As the semester progresses, students are exposed to the various I/O registers present in the microcontroller along with the CPLD interface and a few assignments are designed for them to apply their hardware and software partitionning skills. The second half of the laboratory course is dedicated to a larger team project where students build a complete embedded systems with the McGumps board and LCD expansion board[1]. From semester to semester, the lab project features are modified to introduce fresh ideas every time and keep the course content diversified.

[1]This smaller LCD board using a 128x64 TAB integrated controller was designed and built by my colleagues Milos Prokic, Rong Zhang and myself

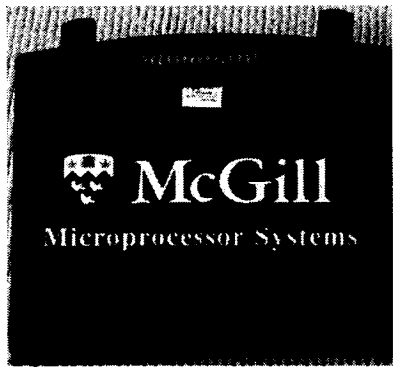


Fig. 5.2 Teaching Kit Packaging

5.2.1 Student Projects

With the combination of the McGumps board and the LCD display expansion module, the students have built some interesting applications under the supervision of Professor Zeljko Zilic and Professor Mark Coates in the Microprocessor Systems course. Following are a few of the term projects that were implemented on the development platform:

McPDA

This lab project required the students to write firmware drivers and a user interface for the LCD screen. External memory was provided on the LCD daughtercard in a serial flash memory for students to store the graphical elements of the user interface. The touch panel was used to access and control the various elements of the user interface.

Handwriting recognition

In another semester, student had to use the touch screen panel to code a handwriting recognition algorithm in the MSP430. Using the auxiliary serial channel, students had to send digits and short messages to another unit through the serial interface. The touch panel had to support calibration and students had the choice between using a dedicated touch screen controller running on the serial bus or the analog channels built into the development platform to perform the coordinate acquisition.

Secure Wireless Communication using RSA

In this application, students had to implement the RSA encryption algorithm in firmware on the MSP430. A small expansion board using the Nordic nRF2401A [33] was purchased and attached to the expansion port of the McGumps. A few groups of students experimented with software encryption and its computational overhead.

The new RF board based on the Chipcon CC2420 features hardware 128-bit AES encryption, thus reducing the load on the MCU. At this time, we have only a few of those boards since they were not yet mass produced for a teaching environment. Also, for debugging wireless systems, some extra equipment such as a spectrum analyzer is needed in the laboratory to facilitate system-level debugging of those wireless systems. At this time, the wireless boards based on the CC2420 are only used for graduate research and could be introduced for teaching in the future.

5.3 Integrated Application - Conference Manager

As a research project, a complete framework was build and tested to validate rapid deployment methodology of wireless sensor networks. The application made use of our 160x160 graphical display with touch panel and the 802.15.4 wireless interface. It was created to emulate a real problem : managing large venue conferences with multiple simultanous sessions [43].

At the heart of the system is one McGumps board with a wireless card attached to the expansion port. This McGumps board communicates through the main serial channel to a computer running a database and web server. A smaller battery-operated handheld unit based on a second McGumps board attached to a wireless card and large graphical LCD panel is used to enter conference information as the sessions are progressing. The complete handheld unit is shown in Figure 5.3.

The handheld locally collects the information about current topics, score cards and session timing and reports this to the PAN coordinator. Upon receiving the latest information, the PAN coordinator updates a small database and the information is then updated on the web server, which through a 2.4 GHz Wifi channel updates a projector displaying the session progress in the conference lobby.

The main objectives of this experiment was to show the simultaneous operation of the

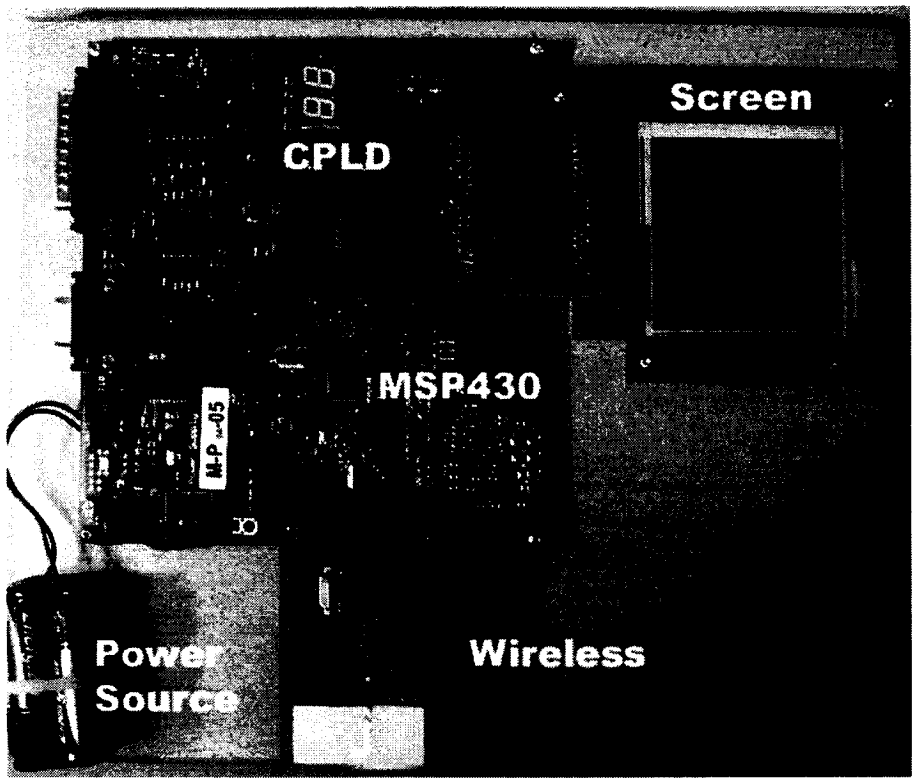


Fig. 5.3 Wireless Conference Manager Handheld Unit

802.15.4 wireless protocol and the larger bandwidth Wifi channel. We found that if the Wifi channel is selected to be in a different center frequency, the 802.15.4 can coexist with minimal impact on the range of transmission [44]. The setup was used at a large conference (ITC 2004 in Charlotte, North Carolina) and performed very well using a single PAN coordinator. The range was sufficient to cover most of the convention center. We noticed that elevator shafts produced a major attenuation of the 802.15.4 signal. A more robust implementation would require multiple PAN coordinator or relay nodes around large reinforced concrete obstacles if the system is used indoors. A complete description of the application and the rapid deployment methodology was presented at the 2005 Micronet Annual Workshop [45]. This architecture allowed our group to further gather statistics about packet loss, device range and network-level issues and compatibility with other common wireless standards.

Chapter 6

Conclusion and Future Work

6.1 Summary

In this master's project, a complete wireless platform was designed, built and tested. The main board was mass-produced and is used for teaching undergraduate courses at McGill university as well as in research projects on low-power wireless systems. The radio transceiver and integrated antenna showed great promise and the prototypes fabricated are used in several of our research group projects. The methodology developed for the integration of the radio transmitter, including the printed antenna and the accurate modeling of the RF circuit, has been demonstrated through fabrication and measurement of prototypes.

6.2 Future Work

Integrating the printed antenna, transceiver, rechargeable battery, micro-controller and low power display in the same board would contribute to lowering the cost of the complete system and expand its use in wireless sensor network research. Expanding on the design of the latest McGumps prototype by switching to a lower-power CPLD would increase the energy efficiency of the platform while keeping the flexibility provided by the programmable logic.

Using our antenna integration methodology, a new transceiver board can be designed on lower-cost FR4 PCB material. Correcting the balun circuit will increase the range of the antenna even if the new PCB material is more lossy. An antenna with larger bandwidth can be designed on the new transceiver module to accommodate dielectric constant variations

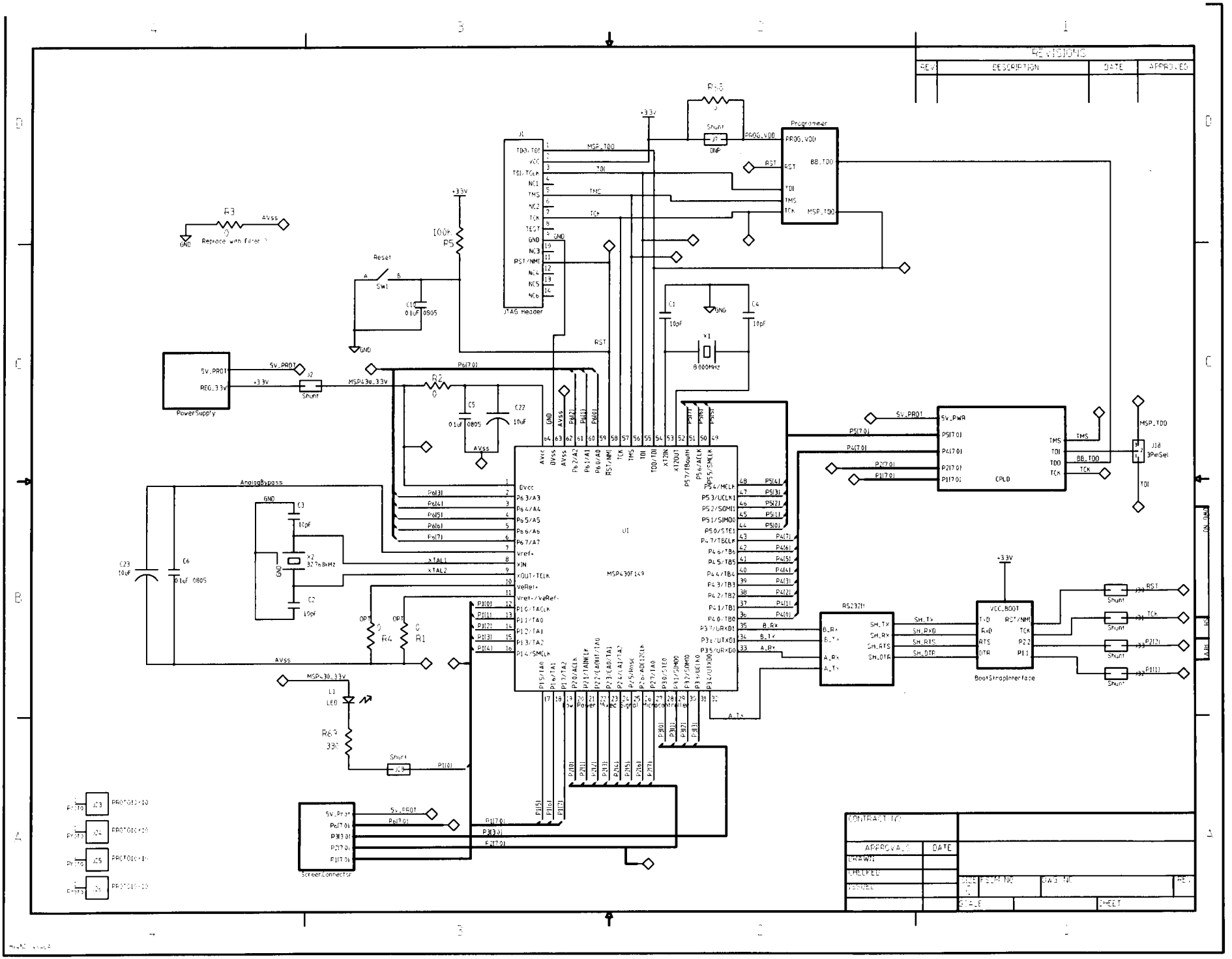
expected in lower-cost FR4.

Other improvements on the antenna could include two orthogonal printed dipoles and a RF switch to enable electronically programmable polarization of the antenna signal. Using this enhancement, the node orientation and therefore the electrical polarization could be dynamically tuned to optimize the antenna range since node orientation may not always be controlled when they are deployed.

Since electromagnetic tools are already being used in the design, the balun circuit could benefit from a microwave circuit re-engineering. By building it from PCB traces several discrete components could be removed from the bill-of-material. For operating at 2.45 GHz, the theoretical work [41, Chapter 8] shows that the circuit would not take a large PCB area. For the very large production volumes targeted by ubiquitous wireless sensor networks, every cost savings are crucial for the expansion of this new and exciting technology.

Appendix A

McGumps Schematics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Programmer
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Reset
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CPLD
RS232It
VCC_BOOT
BootStrapInterface
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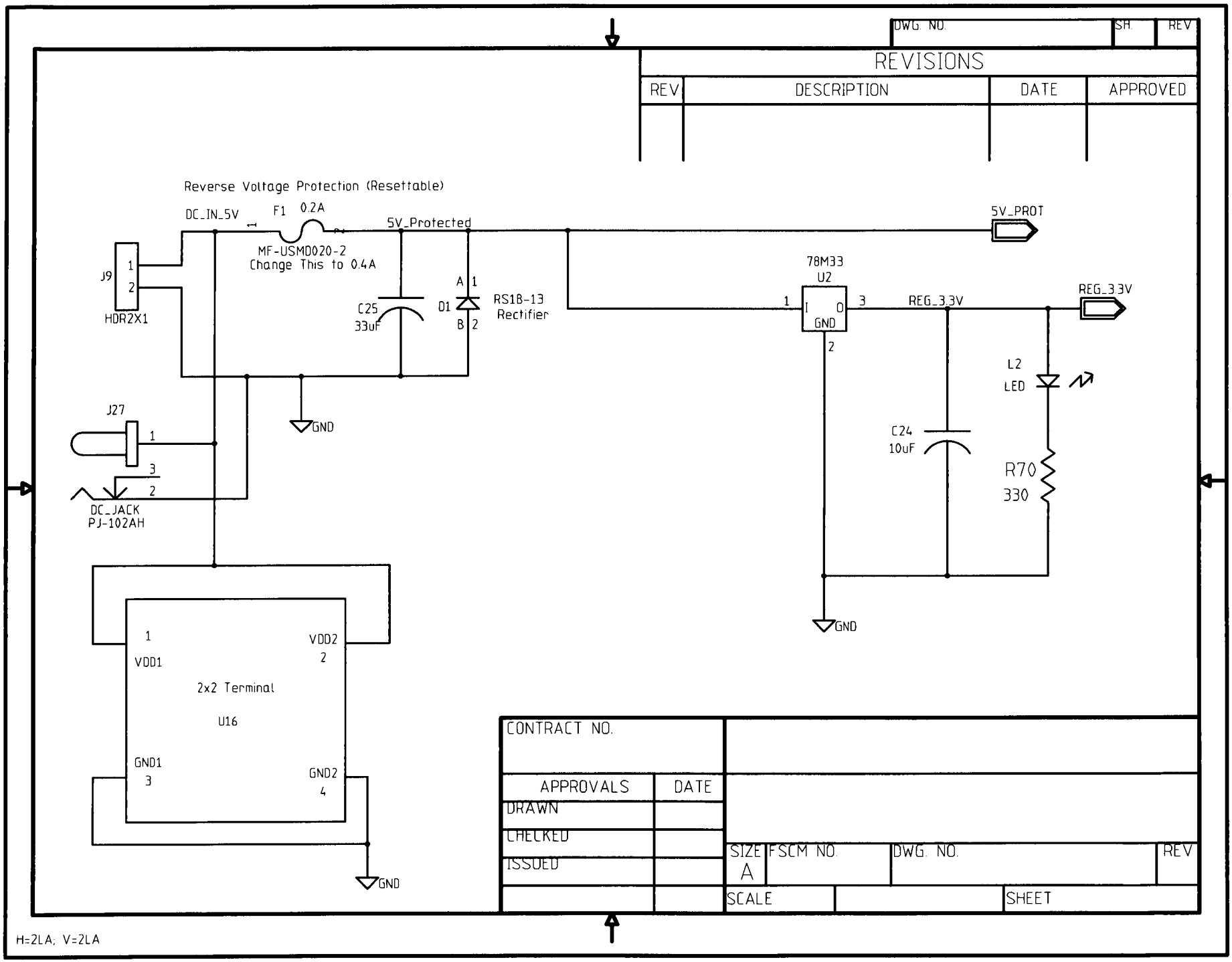
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MF-USMD020-2
Change This to 0.4A
5V_Protected
5V_PROT
J9
HDR2X1
C25
33uF
D1
RS1B-13
Rectifier
78M33
U2
REG_3.3V
GND
L2
LED
C24
10uF
R70
330
J27
DC_JACK
PJ-102AH
2x2 Terminal
U16
VDD1
VDD2
GND1
GND2
CONTRACT NO.
APPROVALS
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REV
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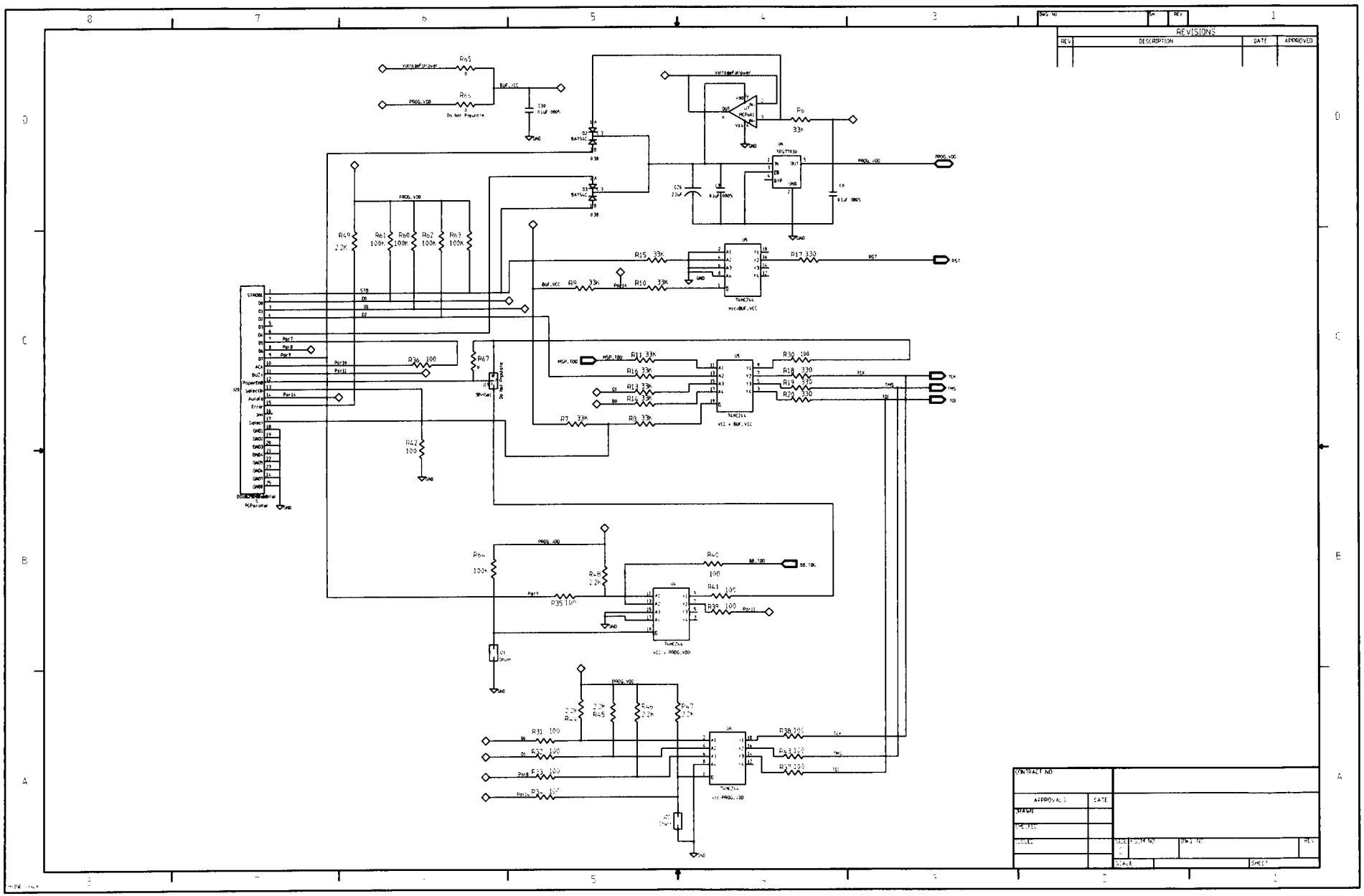
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DWG NO
REV
SCALE
SHEET
STROBE
R65
R66
Do Not Populate
R49
22K
R61
100K
R60
100K
R62
100K
R63
100K
R6
33K
R15
33K
R17
330
R9
33K
R10
33K
R36
100
R67
R42
100
R11
33K
R16
33K
R13
33K
R14
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R7
33K
R8
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R30
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R18
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R19
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R20
330
R64
100K
R48
22K
R35
100
R40
100
R41
100
R39
100
R31
100
R32
100
R33
100
R34
100
R45
R46
22K
R47
22K
R38
100
R43
100
R37
100
74HC244
VCC = BUF_VCC
VCC = PROG_VDD
TPS77830
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TDI
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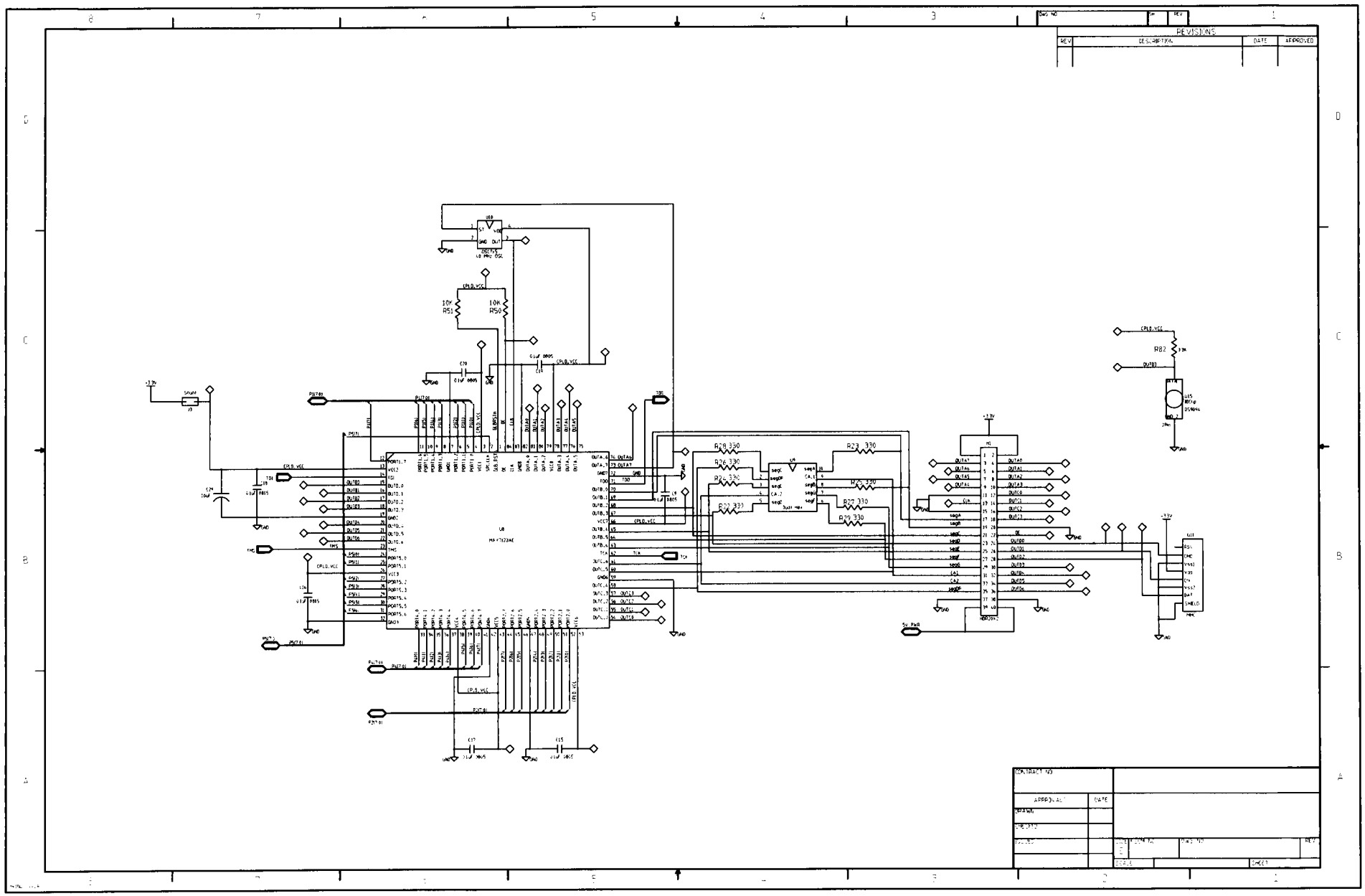
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U9
MAX7320AE
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DSC755
U15
DS9094
U11
NDR2092
R28 330
R26 330
R24 330
R22 330
R23 330
R25 330
R27 330
R29 330
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R51
R50
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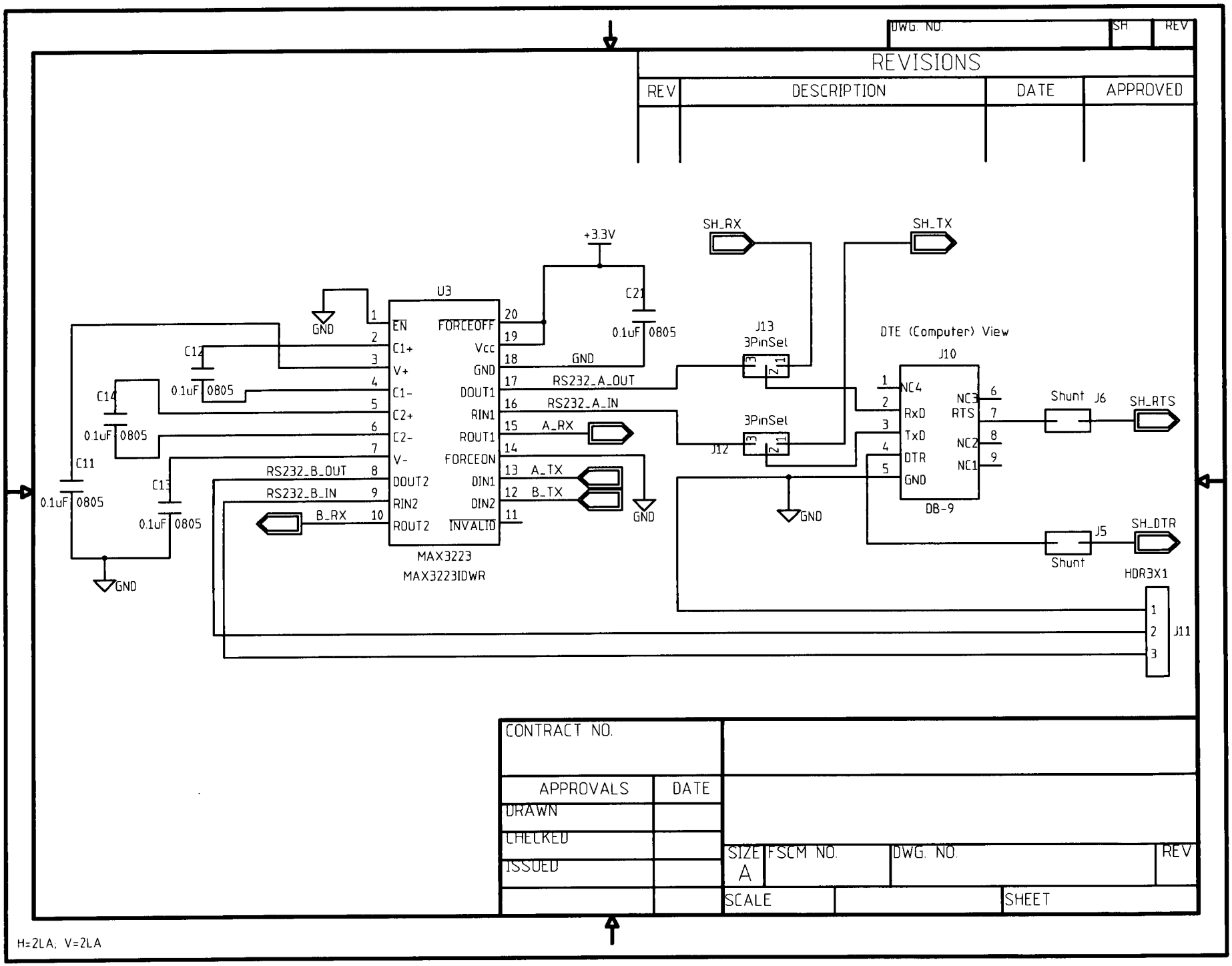
5V PWR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MAX3223IDWR
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V+
C1-
C2+
C2-
V-
DOUT2
RIN2
ROUT2
FORCEOFF
Vcc
GND
DOUT1
RIN1
ROUT1
FORCEON
DIN1
DIN2
INVALID
+3.3V
C21
0.1uF 0805
C12
0.1uF 0805
C14
0.1uF 0805
C11
0.1uF 0805
C13
0.1uF 0805
GND
RS232_A_OUT
RS232_A_IN
A_RX
A_TX
B_TX
RS232_B_OUT
RS232_B_IN
B_RX
SH_RX
SH_TX
J13
3PinSel
J12
3PinSel
DTE (Computer) View
J10
NC4
RxD
TxD
DTR
GND
NC3
RTS
NC2
NC1
DB-9
Shunt J6
SH_RTS
Shunt
J5
SH_DTR
HDR3X1
J11
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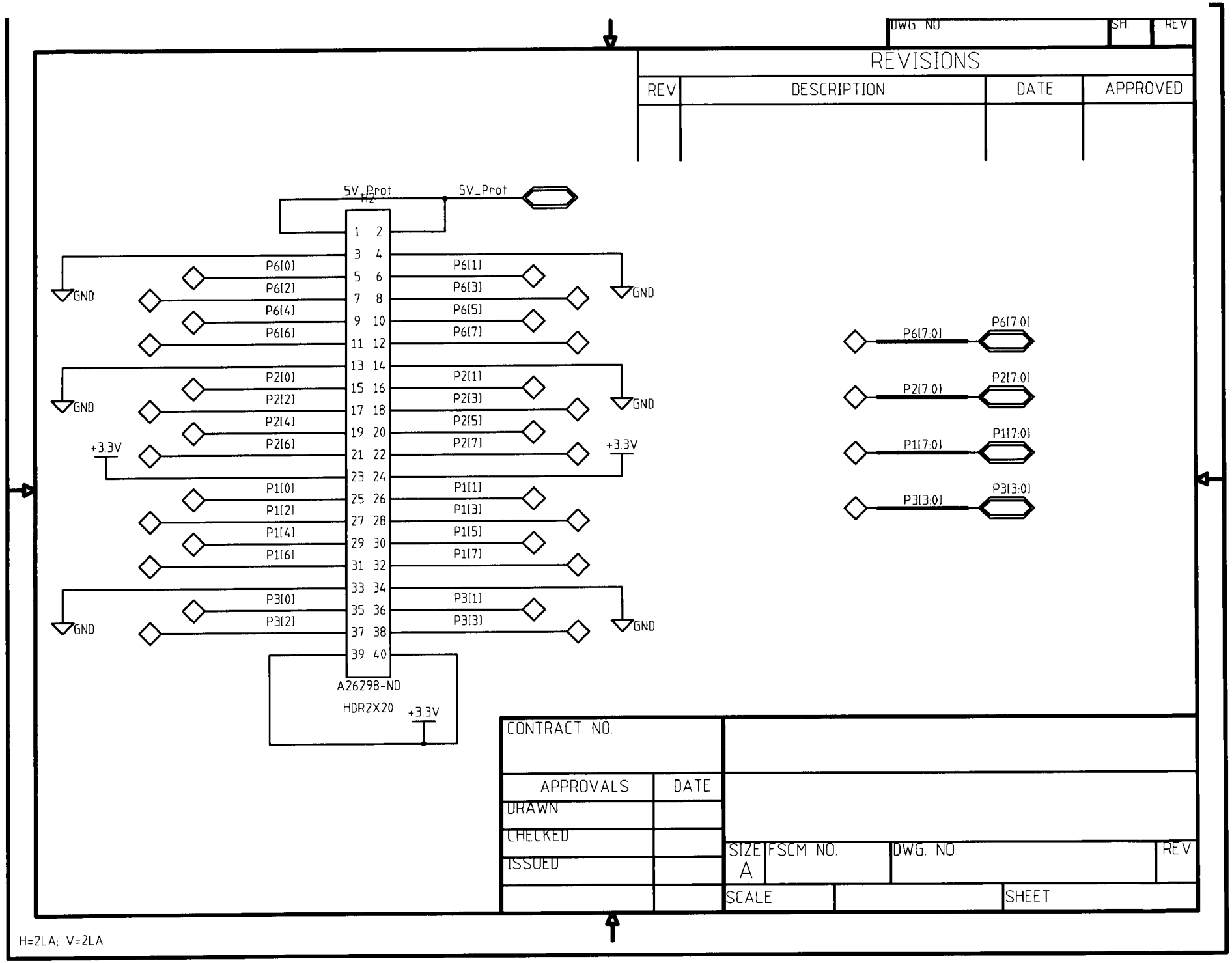
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5 6
7 8
9 10
11 12
13 14
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33 34
35 36
37 38
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HDR2X20
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P3[3:0]
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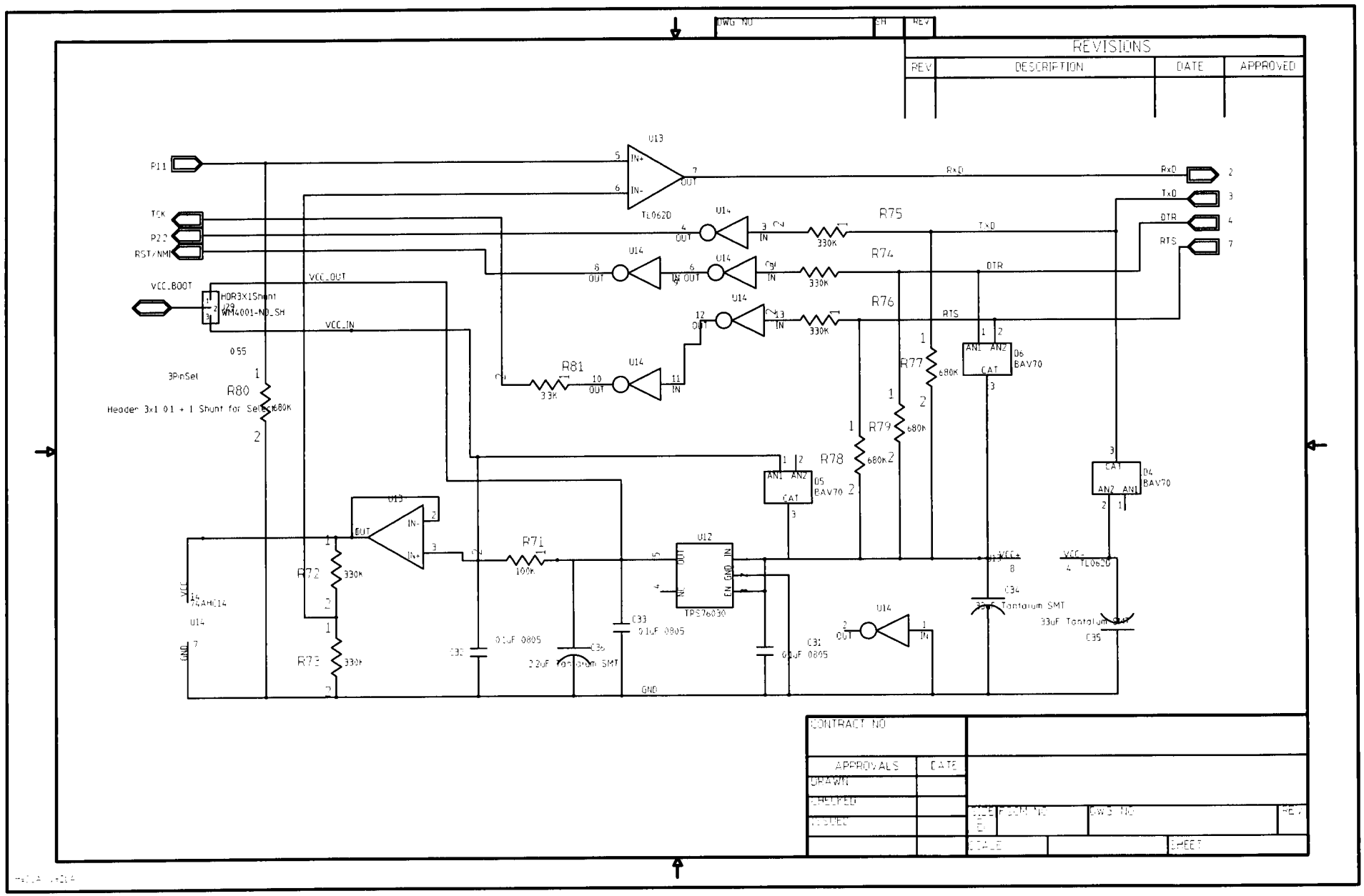
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P22
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HDR3X1Shunt
WM4001-ND_SH
VCC_OUT
VCC_IN
055
3PinSel
R80
680K
Header 3x1 01 + 1 Shunt for Sel
U13
TL062D
RxD
TxD
DTR
RTS
U14
R75
330K
R74
330K
R76
330K
R81
33K
R77
680K
R79
680K
R78
680K
D6
BAV70
D5
BAV70
D4
BAV70
R72
330K
R73
330K
R71
100K
U12
TPS76030
C33
0.1uF 0805
C36
22uF
C31
0.1uF 0805
C34
33uF Tantalum SMT
C35
33uF Tantalum SMT
74AHC14
GND
VCC
CONTRACT NO
APPROVALS
DATE
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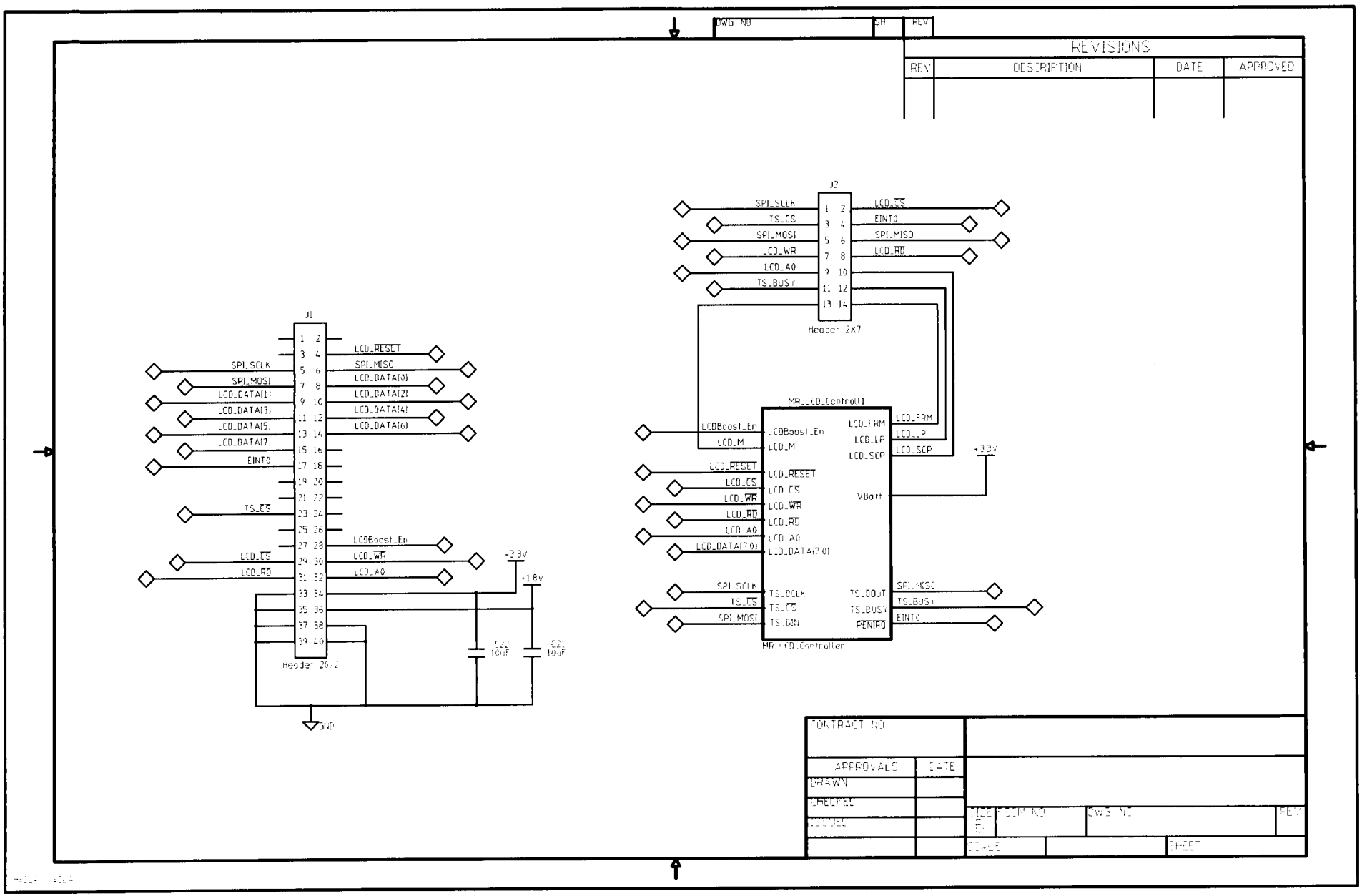
REV
SCALE
SHEET

Appendix B

Epson S1D13700 160x160 Screen Board Schematics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LCD_DATA[1]
LCD_DATA[2]
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LCD_DATA[4]
LCD_DATA[5]
LCD_DATA[6]
LCD_DATA[7]
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TS_CS
LCDBoost_En
LCD_CS
LCD_WR
LCD_RD
LCD_A0
+3.3V
+1.8V
C22
10UF
C21
10UF
GND
Header 20x2
J2
SPI_SCLK
TS_CS
SPI_MOSI
LCD_WR
LCD_A0
TS_BUSY
LCD_CS
EINT0
SPI_MISO
LCD_RD
Header 2x7
MR_LCD_Control U1
LCDBoost_En
LCD_M
LCD_RESET
LCD_CS
LCD_WR
LCD_RD
LCD_A0
LCD_DATA[7:0]
SPI_SCLK
TS_CS
SPI_MOSI
LCD_FRM
LCD_LP
LCD_SCP
VBort
TS_DCLK
TS_CS
TS_DIN
TS_DOUT
TS_BUSY
PENIRQ
SPI_MISO
TS_BUSY
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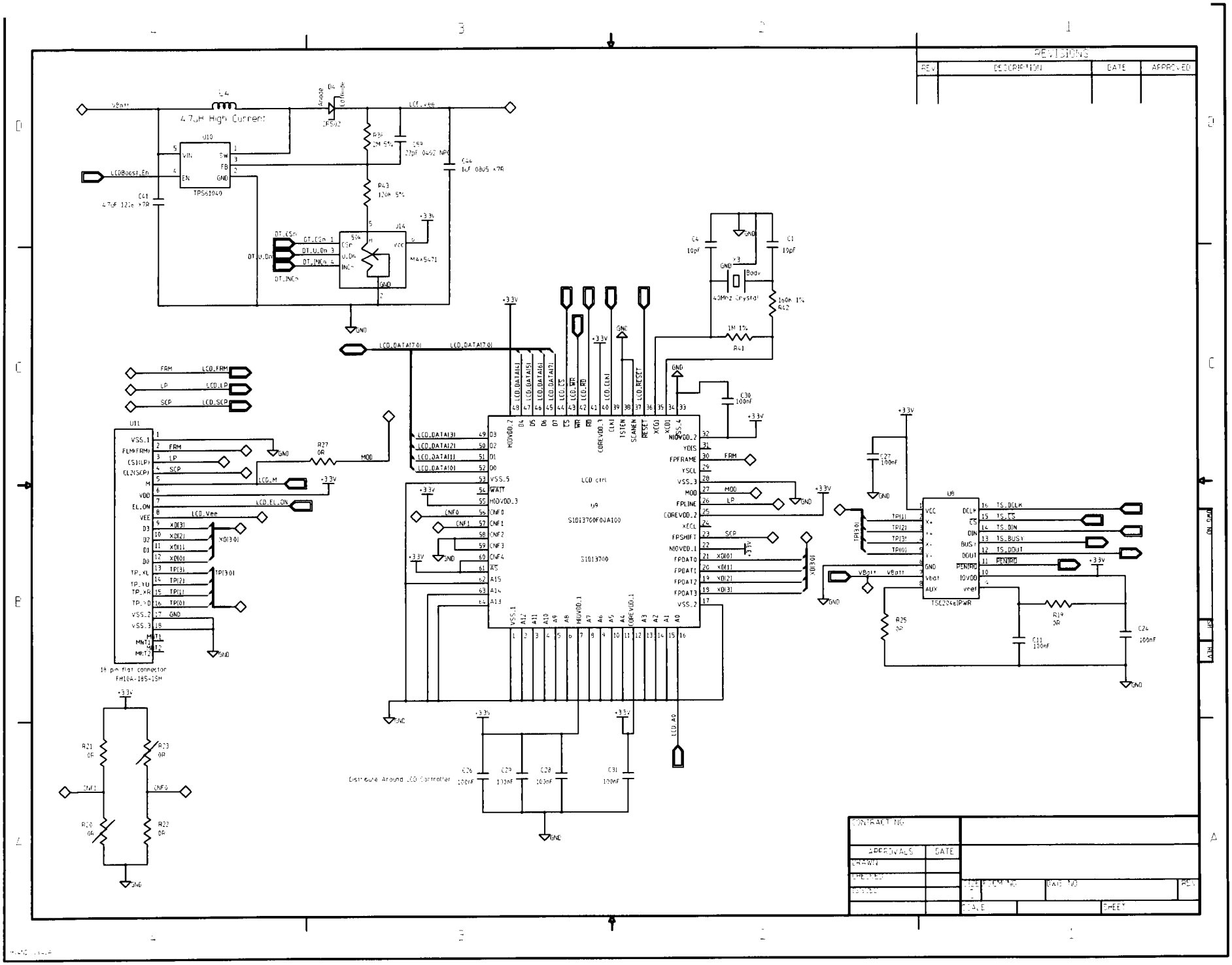
DWG NO
REV
SCALE
SHEET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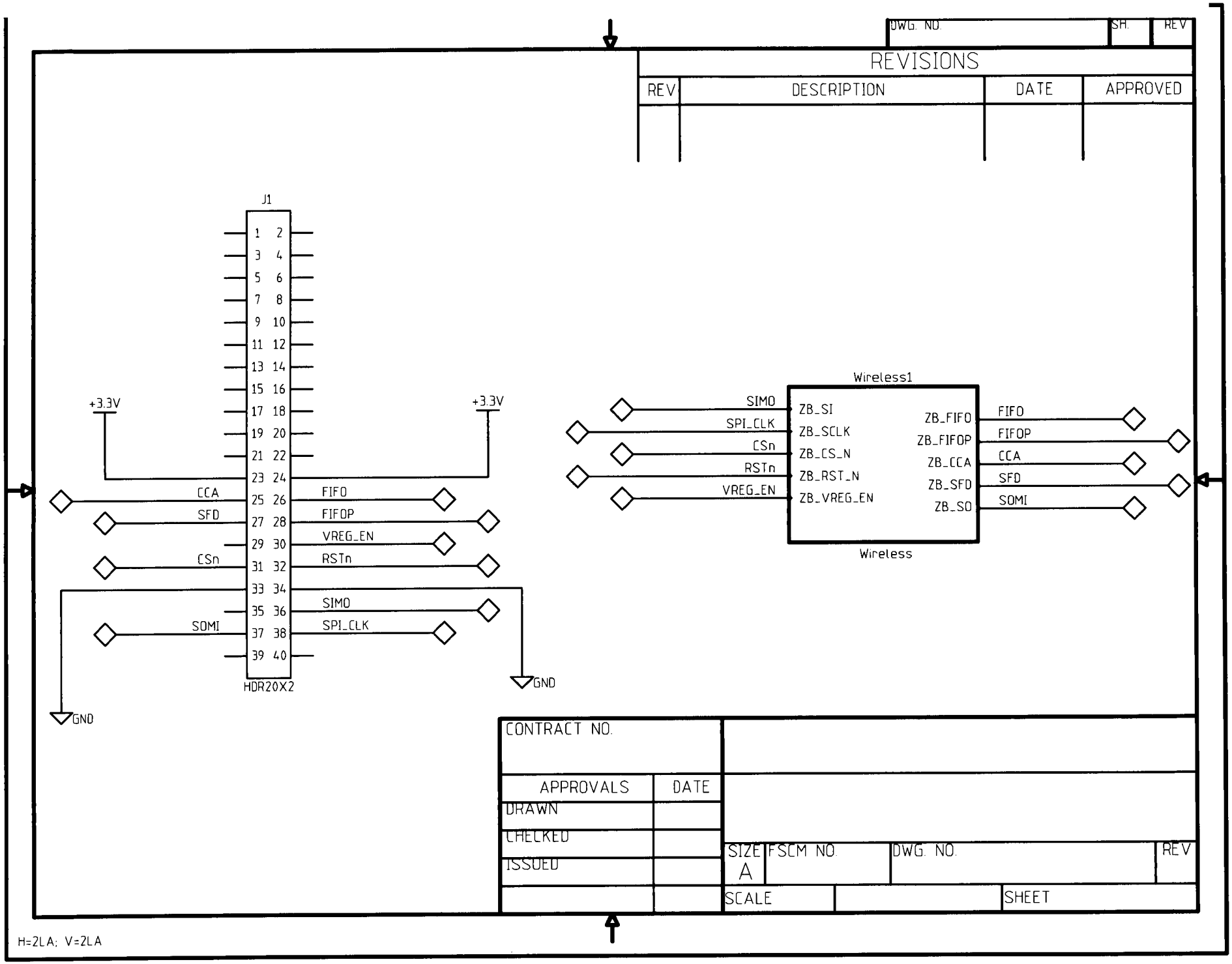
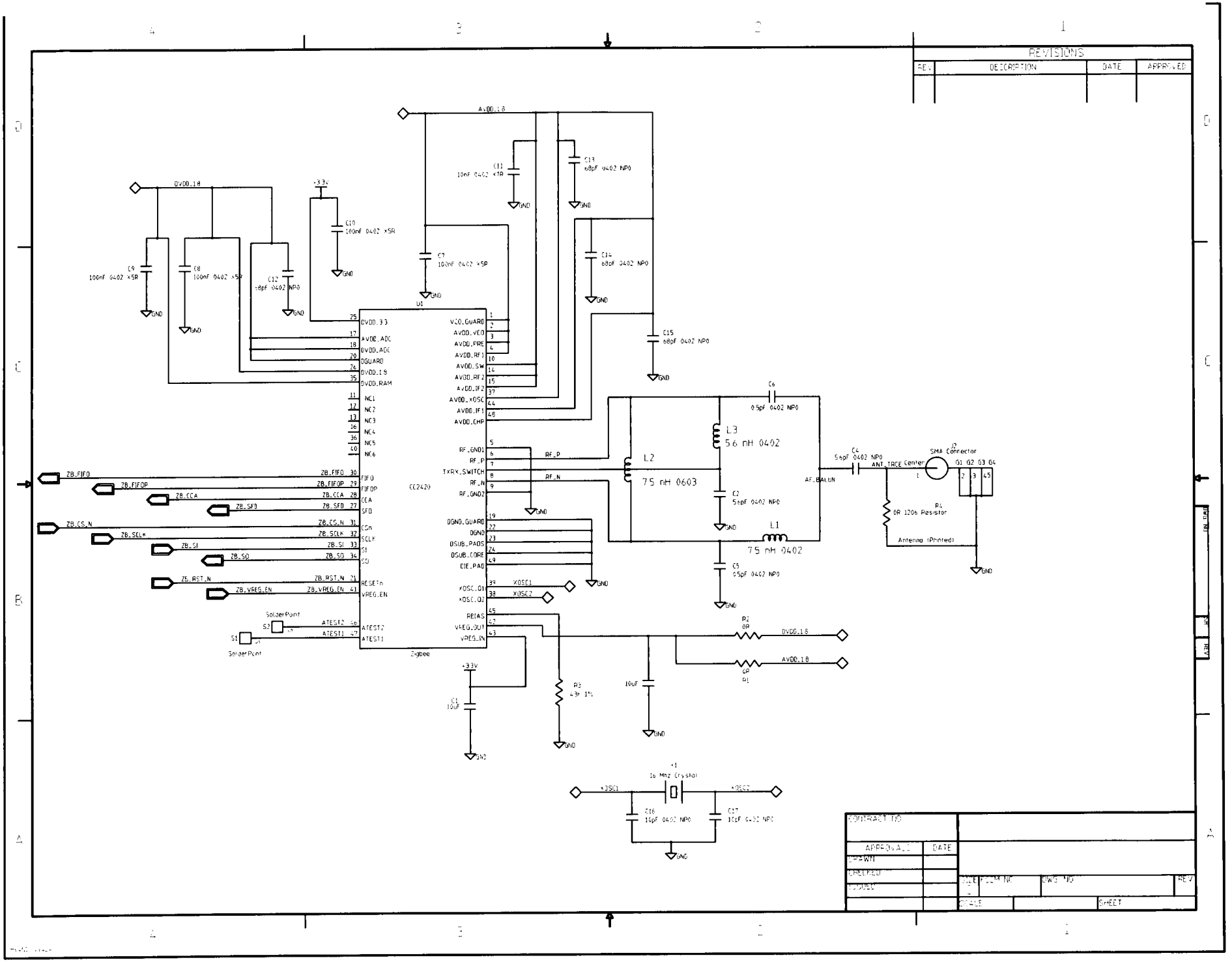
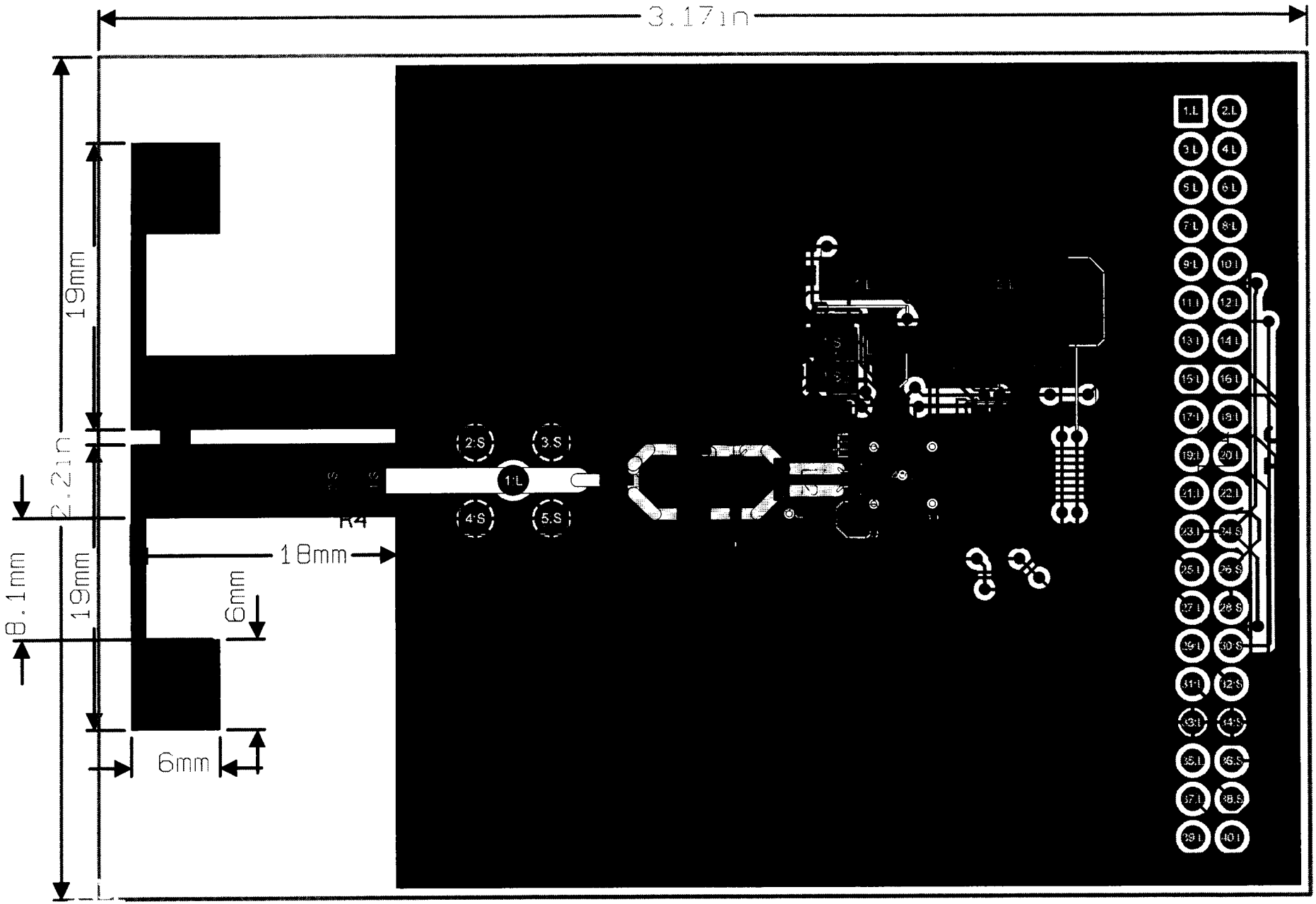
U14
MAX5471
U11
18 pin flat connector
FH10A-18S-1SH
U9
S1D13700F00A100
S1D13700
LCD ctrl
U8
TSC2046IPWR
Distribute Around LCD Controller
CONTRACT NO
APPROVALS
DATE
DRAWN
CHECKED
ISSUED
SIZE
FSCM NO
DWG NO
REV
SCALE
SHEET

Appendix C

McZig RF Screen Board Schematics and Layout


DWG. NO.
SH.
REV
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
J1
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
39 40
HDR20X2
+3.3V
+3.3V
CCA
SFD
CSn
FIFO
FIFOP
VREG_EN
RSTn
SIMO
SPI_CLK
SOMI
GND
GND
Wireless1
SIMO
SPI_CLK
CSn
RSTn
VREG_EN
ZB_SI
ZB_SCLK
ZB_CS_N
ZB_RST_N
ZB_VREG_EN
ZB_FIFO
ZB_FIFOP
ZB_CCA
ZB_SFD
ZB_SO
FIFO
FIFOP
CCA
SFD
SOMI
Wireless
CONTRACT NO.
APPROVALS
DATE
DRAWN
CHECKED
ISSUED
SIZE
A
FSCM NO.
DWG. NO.
REV
SCALE
SHEET
H=2LA; V=2LA


REVISIONS
REV
DESCRIPTION
DATE
APPROVED
AVDD_1.8
DVDD_1.8
+3.3V
C11
10nF 0402 X7R
C13
68pF 0402 NP0
C10
100nF 0402 X5R
C9
100nF 0402 X5R
C8
100nF 0402 X5R
C12
68pF 0402 NP0
C7
100nF 0402 X5R
C14
68pF 0402 NP0
C15
68pF 0402 NP0
U1
CC2420
DVDD_3.3
AVDD_ADC
DVDD_ADC
DGUARD
DVDD_1.8
DVDD_RAM
NC1
NC2
NC3
NC4
NC5
NC6
VCO_GUARD
AVDD_VCO
AVDD_PRE
AVDD_RF1
AVDD_SW
AVDD_RF2
AVDD_IF2
AVDD_XOSC
AVDD_IF1
AVDD_CHP
RF_GND1
RF_P
TXRX_SWITCH
RF_N
RF_GND2
DGND_GUARD
DGND
DSUB_PADS
DSUB_CORE
DIE_PAD
XOSC_Q1
XOSC_Q2
RBIAS
VREG_OUT
VREG_IN
ATEST2
ATEST1
FIFO
FIFOP
CCA
SFD
CSn
SCLK
SI
SO
RESETn
VREG_EN
ZB_FIFO
ZB_FIFOP
ZB_CCA
ZB_SFD
ZB_CS_N
ZB_SCLK
ZB_SI
ZB_SO
ZB_RST_N
ZB_VREG_EN
RF_P
RF_N
XOSC1
XOSC2
Zigbee
C6
0.5pF 0402 NP0
L3
5.6 nH 0402
L2
7.5 nH 0603
L1
7.5 nH 0402
C2
.5pF 0402 NP0
C5
.5pF 0402 NP0
C4
.5pF 0402 NP0
ANT_TRCE Center
ANT_BALUN
J2
SMA Connector
G1 G2 G3 G4
R4
0R 1206 Resistor
Antenna (Printed)
R2
0R
R1
0R
DVDD_1.8
AVDD_1.8
R3
43K 1%
C1
10uF
10uF
SolderPoint
S2
S1
SolderPoint
Y1
16 Mhz Crystal
XOSC1
XOSC2
C16
10pF 0402 NP0
C17
10pF 0402 NP0
GND
CONTRACT NO.
APPROVALS
DATE
DRAWN
CHECKED
ISSUED
SIZE
DWG NO.
REV
SCALE
SHEET


3.17in
19mm
2.21in
8.1mm
19mm
18mm
6mm
6mm
R4
1:L
2:S
3:S
4:S
5:S

References

[1] I. Buchmann, *Batteries in a Portable World.* Cadex Electronics Inc, second ed., 2001. Online Book at http://www.buchmann.ca/toc.asp. viii, 9, 10

[2] E. H. Callaway, *Wireless sensor networks: architectures and protocols.* Auerbach Publications, 2004. 5, 8

[3] V. Handziski, J. Polastre, J. Hauer, C. Sharp, A. Wolisz, and D. Culler, "Flexible hardware abstraction for wireless sensor networks," *Proceedings of the 2nd European Workshop on Wireless Sensor Networks (EWSN 2005)*, 2005. 5, 8

[4] Crossbow Technology Inc., "MPR2400 - MICAz ZigBee Series (Document 6020-0060-02 Rev B) ," 2005. http://www.xbow.com/ — MICAz_Datasheet.pdf. 6

[5] J. Polastre, R. Szewczyk, and D. Culler, "Telos: Enabling ultra-low power wireless research," *In Proceedings of the Fourth International Conference on Information Processing in Sensor Networks: Special track on Platform Tools and Design Methods for Network Embedded Sensors (IPSN/SPOTS)*, 2005. http://www.cs.berkeley.edu/ polastre/papers/spots05-telos.pdf. 6

[6] B. Hemingway, W. Brunette, T. Anderl, and G. Borriello, "The flock: mote sensors sing in undergraduate curriculum," *Computer*, vol. 37, no. 8, p. 72, 2004. 0018-9162. 6, 12

[7] GNU Software, "GNU ARM toolchain for Cygwin, Linux and MacOS," July 2005. http://www.gnuarm.com/. 7

[8] GNU Software , "The GCC toolchain for the Texas Instruments MSP430 MCUs," July 2005. http://mspgcc.sourceforge.net/. 7

[9] Richard Barry, "FreeRTOS," July 2005. http://www.freertos.org/. 8

[10] Micriμm Technologies Corporation, "μC/OS-II, The Real-Time Kernel," July 2005. http://www.micrium.com/. 8

[11] Red Hat Inc, "eCos, the Embedded Configurable Operating System," 2005. http://ecos.sourceware.org/. 8

[12] *Draft Standard for Part 15.4: Wireless Medium Access Control (*MAC*) and Physical Layer (*PHY*) specifications for Low Rate Wireless Personal Area Networks (*LR-WPAN*s).* IEEE, February 2003. 8, 10, 25

[13] Nordic Semiconductor, "Nordic Semiconductor nRF24E2 Datasheet," datasheet, 2005. http://www.nordicsemi.no/. 9

[14] Chipcon AS, "SmartRF CC2420 preliminary datasheet (rev 1.2)," datasheet, Gaustadalléen 21 NO-0349, Oslo, Norway, 2004. http://www.chipcon.com/. 9, 23, 39, 45

[15] P. Cross, "Zeroing in on zigbee (part 2)," *Circuit Cellar*, March 2005. http://www.circuitcellar.com/. 9

[16] B. Richards and B. Stull, "Teaching wireless networking with limited resources," *Proceedings of the 35th SIGCSE technical symposium on Computer science education*, 2004. 9, 12

[17] S. A. Megahed and W. B. Ebner, "Lithium-ion coin cells for electronic applications," *Battery Conference on Applications and Advances*, 1994. 10

[18] S. Park, A. Savvides, and M. B. Srivastava, "Battery capacity measurement and analysis using lithium coin cell battery," *ISPLED*, pp. 382–388, August 2001. 10

[19] Zigbee Alliance, "Zigbee specification version 1.0," June 2005. http://www.zigbee.org/. 10

[20] M. I. Montrose, *Printed circuit board design techniques for EMC compliance: a handbook for designers.* IEEE Press series on electronics technology, New York: IEEE Press. 11, 49

[21] H. W. Johnson, *High-speed digital design: a handbook of black magic.* Englewood Cliffs, N.J: Prentice Hall, 1993. 11

[22] C. F. Coombs, *Printed circuits handbook.* New York: McGraw-Hill, 4th ed., 1996. 11

[23] C. T. Robertson, *Printed circuit board designers reference.* Safari Tech Books Online collection, Prentice Hall Professional Technical Reference, 2004. http://www.safaribooksonline.com/. 11

[24] J.-S. Chenard, C. Y. Chu, Z. Zilic, and M. Popovic, "Design methodology for wireless nodes with printed antennas," *Design Automation Conference (*DAC*) Proceedings*, 2005. 12, 22, 24, 37

[25] J.-S. Chenard, U. Khalid, M. Prokic, R. Zhang, K.-L. Lim, A. Chattopadhyay, and Z. Zilic, "Expandable and robust laboratory for microprocessor systems," *International Conference on Microelectronic Systems Education Proceedings*, June 2005. 13, 21

[26] E. Callaway, P. Gorday, L. Hester, J. A. Gutierrez, M. Naeve, B. Heile, and V. Bahl, "Home networking with IEEE 802.15.4: A developing standard for low-rate wireless personal area networks," *IEEE Communications Magazine*, pp. 70–77, August 2002. 15, 25

[27] Xilinx Inc., "CoolRunner-II CPLD Family – Product Specification," 2005. http://www.xilinx.com/CoolRunner2/ (DS090 – Version 2.5). 18

[28] Altera Corporation, "MAX 7000A Programmable Logic Device Data Sheet," 2003. http://www.altera.com/literature/ds/m7000a.pdf (Version 4.5). 18, 33

[29] Altera Corporation, "ByteBlasterMV Parallel Port Download Cable Data Sheet." Version 1.01, June 1999. 18, 34

[30] Olimex Ltd., "MSP430 JTAG - JTAG for Programming and Flash Emulation ," 2002. http://www.olimex.com/dev/msp-jtag.html. 18, 34

[31] The Multimedia Card Association, 2005. http://www.mmca.org/home. 19

[32] Dallas Semiconductor – Maxim, "Book of iButton Standards," 2002. http://pdfserv.maxim-ic.com/en/an/appibstd.pdf. 19

[33] Nordic Semiconductor, "Nordic Semiconductor nRF2401A Datasheet," datasheet, 2004. (Version 1.0) http://www.nordicsemi.no/. 23, 57

[34] J. Polastre, R. Szewczyk, C. Sharp, and D. Culler, "The Mote Revolution: Low Power Wireless Sensor Network Devices," powerpoint, 2004. http://webs.cs.berkeley.edu/papers/hotchips-2004-motes.ppt. 27

[35] M. D. Prokic, "Low-rate wireless personal area network coordinator design and implementation," Master's thesis, McGill University, 2005. 27

[36] C. M. Wah, Z. Zilic, K. Radecka, and J. S. Chenard, "Architectures of increased availability wireless sensor network nodes," in *International Test Conference*, (Charlotte, NC), p. 1232, 2004. 27

[37] W. L. Stutzman and G. A. Thiele, *Antenna Theory and Design.* Wiley, second ed., 1997. 37, 39, 44

[38] Agilent, "Advanced design system 2003a documentation," product documentation, Agilent Technologies, 2003. 37

[39] D. Edward and D. Rees, "A broadband printed dipole with integrated balun," *Microwave J.*, pp. 339–344, May 1987. 37

[40] T. S. Rappaport, *Wireless Communications: Principles and Practice.* Upper Saddle River, New Jersey: Prentice Hall, 2nd ed., 2002. 39

[41] C. Y. Chu, "Printed dipole antenna for wireless communications," Master's thesis, McGill University, 2005. 45, 60

[42] muRata, "Murata Chip S-Parameter and Impedance Library Version 3.7.1." http://www.murata.com/designlib/mcsil.html. 49

[43] M. Prokic, J.-S. Chenard, R. Zhang, U. Khalid, and Z. Zilic, "IEEE 802.15.4 wireless conference manager system," tech. rep., IEEE International Midwest Symposium on Circuits and Systems, August 2005. 57

[44] I. Howitt and J. A. Gutierrez, "IEEE 802.15.4 low rate — wireless personal area network coexistence issues," *Wireless Communications and Networking*, pp. 1481–1486, 2003. 58

[45] M. Prokic, J.-S. Chenard, R. Zhang, U. Khalid, and Z. Zilic, "Methodology for rapid development and robust deployment of wireless sensor networks," Tech. Rep. 103 – 104, Micronet R&D Annual Workshop, May 2005. 58