Time-Mode Reconstruction IIR Filters for Sigma-Delta Phase Modulation Applications

Ali Ameri
Master of Engineering
Department of Electrical and Computer Engineering
McGill University, Montreal

A thesis submitted to McGill University in partial fulfillment of the requirements for the degree of Master of Engineering

June 2011

Abstract

The design of several low-pass IIR time-mode filters for use as reconstruction filters in digital-to-time conversion (DTC) applications is proposed. Previously, such reconstruction filters were implemented using phase-locked loops. The proposed filters are constructed from a simple digital-like structure involving voltage-controlled delay units. The resulting circuits require very small silicon area and consume very little power. A first-order filter design for wideband reconstruction applications was fabricated in a 0.13 μm CMOS process occupying a silicon area of 170 μm x 100 μm and consumes 670 μW. The results prove for the first time that the concept of time-mode filtering is feasible in a CMOS monolithic process. Another design, intended for narrowband sigma-delta phase signal generation applications, is proposed that utilizes similar building blocks but uses a filter topology that is better suited for implementations with transfer functions having low-frequency poles. High-order realizations can be constructed as a cascade of several first-order sections. Such an approach will be demonstrated in the design of a sigma-delta phase-encoding signal-generation scheme.

Abrégé

Dans cette dissertation nous proposons plusieurs filtres IIF passe-bas qui opèrent en mode temps. Ces dispositifs sont conçus pour être utilisé comme filtres de reconstruction dans les convertisseurs numérique-temps (CNT). Dans le passé, de tels filtres ont été implémenté à partir de boucles à verrouillage de phase. Les filtres proposés dans cette thèse sont construits à partir d'une simple structure numérique impliquant des unités de retards commandés en tension. Les circuits résultant de cette approche requièrent de petites surfaces sur silicium et consomment très peu d'énergie. Un filtre du premier ordre pour les applications larges bandes a été fabriqué dans un processus CMOS 0.13 µm. Le filtre occupe une surface de silicium de 170 µm x 100 µm et consomme 670 µW. Les résultats montrent pour la première fois que la notion de filtrage en mode temps est possible dans un processus CMOS monolithique. Un autre filtre destiné à des applications de génération de signal de phase sigma-delta à bande étroite est aussi proposé. Ce filtre utilise des blocs de construction similaire au premier mais utilise une topologie qui est mieux adapté pour les implémentations de fonctions de transfert ayant des pôles à forte valeur de Q. Les filtre d'ordre supérieur peuvent être construits en cascadant plusieurs filtres du premier ordre. Une telle approche sera démontrée par la conception d'un système de génération de signaux de phase codes en sigma-delta.

Acknowledgments

I am deeply indebted to my supervisor, Professor Gordon W. Roberts, for giving me the opportunity to study in his research group. I would not have been able to complete this thesis without his invaluable advice, his constant support, and his dedication. His guidance helped me in all the time of research and writing of this thesis. To all my great friends at McGill, I thank you for making my experience both exciting and enjoyable. I will miss all the wonderful moments. I would like to acknowledge the Canadian Microelectronics Corporation (CMC) for the use of their integrated circuit fabrication and testing facilities. I wish to thank my parents, my sister, and my brother for their endless love and support throughout my entire life.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

Time-mode signal processing (TMSP) has become a popular technology in which bulky and power hungry analog blocks are implemented using simple digital-like building blocks. In TMSP, voltage-mode sampled data is encoded in terms of a rising edge with respect to the rising edge of a reference clock. Three distinctive aspects of time-mode circuits enable compatibility with rapidly emerging deep submicron CMOS technologies: (1) familiar digital-like building blocks, (2) synthesizable designs using CAD tools, and (3) information is carried by noise-immune square-wave signals. One of the main features in advanced CMOS technologies is the reduction of the supply voltage due to advances in digital circuit integration. Often the supply voltage is the upper limit to the internal signal swings in an electronic circuit, thereby limiting the analog signal processing capability of the circuit. When transistors are stacked on top of one another for cascoding reasons, further reduction of internal signal swings will occur. All this is to

say that an electronic signal is forced to occupy less voltage headroom when the supply level is reduced. This reduces the signal handling capability of the circuit. For fixed noise levels, reducing the signal range reduces the maximum signal-to-noise ratio (SNR) attainable by the circuit; hence reducing its range of applicability.

In the case of TMSP, the signal handling range of operation is set by the distance between one rising edge with respect to another. As the distance between these two signals is independent of the supply voltage, one can argue that the signal handling capability of the time-mode (TM) circuit is unlimited; albeit, the bandwidth of the signals within this range will also be limited, i.e., time-bandwidth trade-off. In the case of a periodic square-wave signal as the reference, the signal range will be limited to one-half the reference period. Hence, the maximum signal handling capability of TM circuits is ultimately limited to its sampling frequency. With parallelism, multiple circuits running at low rates can be used to improve the signal handling capability of TM circuits while maintaining large signal bandwidth. Square-wave signals carrying TM information are less susceptible to amplitude-like noise sources, as the zero-crossing point of a square wave has very little cross-correlation with an additive random amplitude noise signal. TMSP can be performed with digital-like circuits that are small in silicon size and consume very little power. Moreover, biasing concerns are no longer an issue, as the TM building blocks always begin their dynamic operation from a known bias point, e.g. V_{DD} or V_{SS}. Adopting a digital approach enables existing computer-aided design tools to be used to synthesize TMSP circuits.

Previous works in TMSP have focused on various applications including the design of a time-based voltage comparator [1], a sigma-delta analog-to-digital converter [2], circuits for conversion between the voltage and time domains [3], and also an interface for a capacitive sensors for lab-on-chip applications [4]. Time-mode signal processing is a relatively new technology; it does not share the same building blocks as in voltage-domain signal processing. The purpose of this thesis is to shed light on some new aspects of this domain and also introduce some new TMSP building blocks. Specifically, the focus of this work will be on the development of TMSP building blocks based solely on delay elements constructed from digital-like inverter structures. Furthermore, these blocks are employed to construct more complex systems, more specifically, time-mode low-pass infinite impulse response (IIR) filters.

An important application of time-mode filters is in the area of anti-imaging or reconstruction filters in sigma-delta phase-modulation applications where picoseconds time delays are realized and used as a test stimulus [5]. In the past, a phase-lock loop (PLL) structure was used to remove the images associated with a phase-modulated signal generator. In this thesis we shall demonstrate the realization of two possible reconstruction filters constructed from the proposed TMSP building blocks. Here it will be shown that these filters require less silicon area and a lot less power than the PLL approach. One design will be better suited to small amplitude phase signals with wide bandwidths, whereas the other design is better suited to large amplitude phase signal with narrow bandwidths.

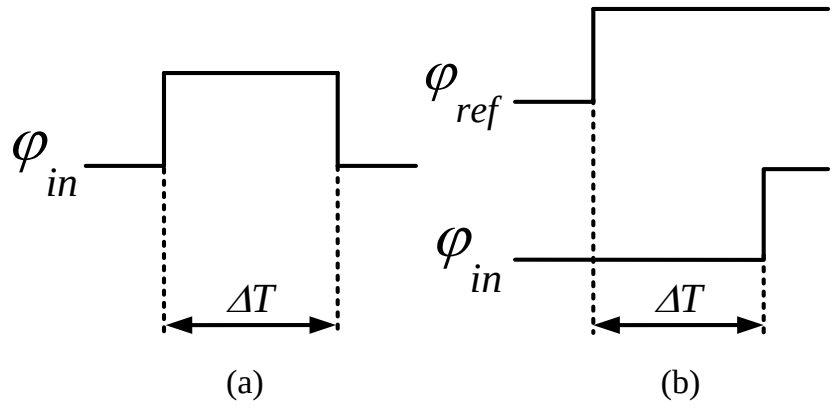


Figure 1-1: Time-mode signals, (a) one-signal representation, (b) two-signal representation.

1.2 Time-Mode Signals

Time-mode signals are the basic variables or carriers of information in TMSP, whose equivalents in the voltage-domain are voltage signals. Each time-mode signal specifies a time-difference variable defined as the quantity of time interval between (a) the rising and falling edges of a single pulse-shaped signal, or (b) the rising edges of a reference and data signal, as illustrated in Figure 1-1(a) and (b), respectively. The former signal representation is used in a pulse-width modulation-based system. The latter, which will be used throughout this work, represents a phase-modulated signal measured with respect to a reference edge. Note that even though time-mode signals have a digital shape in nature, they actually define discrete samples of analog information. In other words, there is a one-to-one mapping between time-mode and voltage-mode signals. Each time difference variable $\Delta T(n)$ is associated with the nth sample of an analog sequence.

Moreover, a time difference variable $\Delta T(n)$ can be related to its corresponding phase difference variable $\Delta\varphi(n)$ as follows,

$$\Delta\varphi(n) = 2\pi f_{clk}\ \Delta T(n) \tag{1.1}$$

where $\Delta\varphi(n)$ is expressed in radians and f_{clk} is the frequency of the reference clock.

1.3 Thesis Overview

This thesis is organized as follows. In Chapter 2, a broad study of the past works of the basic building blocks used in TMSP will be summarized. These blocks provide a means to convert time-mode signals to the analog or digital domain, and vice versa. The concept of aliasing in time-mode signals will be investigated and a circuit method to mitigate its effects is described. Furthermore, some newly developed circuits will be introduced that can perform basic arithmetic operations such as addition and scaling.

In Chapter 3, the arithmetic building blocks will be combined to realize a first-order low-pass filter circuit. A test chip was fabricated in a 0.13 micron IBM CMOS process. The results of the experimentation will be presented and analyzed. A fundamental limitation of this filter topology (i.e., limited signal handling capability) has been identified.

Chapter 4 introduces two new first-order filter topologies with signal handling capability that reaches the maximum available range of one-half the clock period. We limit our proof of concept to simulation results only as the discovery of these new filter

topologies came quite late in the thesis process. Nonetheless, they offer significant improvements to the filter design of Chapter 3 and need to be recognized. Extensions to high-order filter realizations are also presented in this chapter. These high-order structures are formed through a cascade of several first-order sections to realize very narrowband filters with maximum signal handling capability.

Chapter 5 will demonstrate the application of these very narrowband filters in a phase signal generation application. As the thesis title suggests, the main objective of this dissertation.

Finally, conclusions of this work and a discussion of possible future works are provided in Chapter 6.

Chapter 2

Building Blocks for Time-Mode Signal Processing

In this chapter the basic building blocks used in time-mode signal processing will be explored. These circuits either work as an interface between the voltage and time domains, or directly manipulate time-mode signals. Voltage-to-time converters, voltage-to-time adders, and voltage-to-time integrators are categorized as the interfaces between analog voltages and time-mode signals. Time-to-digital converters and digital-to-time converters are introduced as the interface between time and digital domains. Finally, time amplifiers, time-mode adders, time integrators, and unit delays are utilized in order to directly process time-mode signals. The functionality of these building blocks along with some circuit issues will be described in some detail in this chapter.

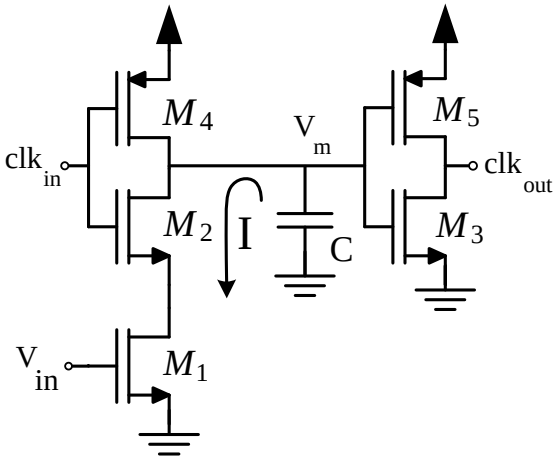
2.1 Voltage-to-Time Conversion

Voltage-to-time conversion can be easily realized using a voltage-controlled-delay unit, or VCDU for short. A VCDU takes a sample of an input voltage signal and translate this sampled value into the phase of a reference clock. A VCDU is usually constructed from a chain of inverters whose propagation delay is controlled by an

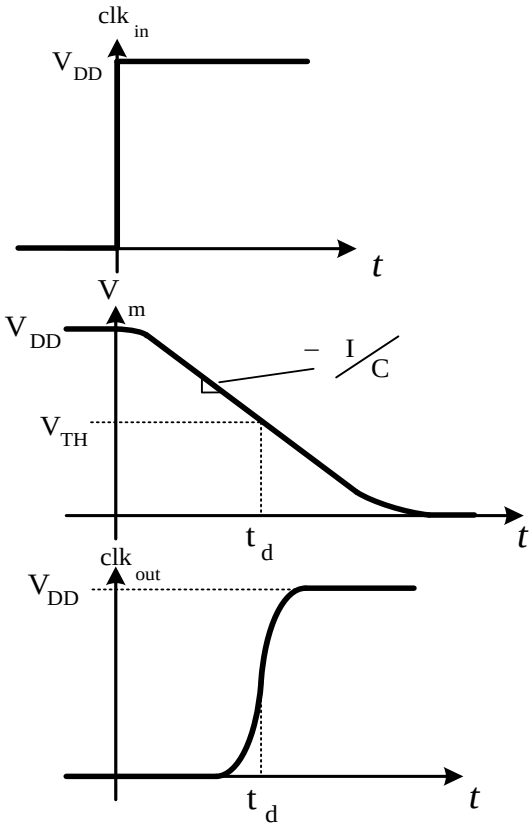
external voltage signal. The following subsections will describe two different ways of realizing this element.

2.1.1 Current-Starved-Based VCDUs

Figure 2-1(a) shows the circuit schematic of a VCDU consisting of a cascade of two inverter circuits with digital input clk_{in} and digital output clk_{out}. The output of the first inverter (denoted by V_m) is loaded with a physical lump capacitance C. An additional transistor M_1 whose gate voltage is controlled by an external voltage signal V_{in} is included with the front-end inverter to control its rate of discharge. Shown in Figure 2-1(b) is the timing diagram for this VCDU for the input clk_{in}, the output clk_{out} and the voltage across the capacitor is V_m. When the input signal at clk_{in} is low, the voltage across C is charged to V_{DD} and the output of the VCDU is low. When the input signal at clk_{in} goes high, the capacitor starts to discharge through M_1 and M_2 towards ground. As the voltage falls below the threshold (V_{TH}) of the second inverter circuit, the output signal clk_{out} goes high. As shown in the timing diagram, the time difference between the input and the output rising edges is t_d. The magnitude of t_d is established by the control voltage V_{in} on the gate of M_1. The larger the gate voltage, the faster the discharge. Assuming that capacitor C is discharged from V_{DD} to V_{TH} over a time period of t_d, together with the fact that M_1 operates as a constant current source I during this time, the capacitor discharge rate can expressed as $-I/C$ V/s. As the voltage change on the capacitor is V_{DD}-V_{TH}, the time to discharge the capacitor to this level t_d can be written as



(a)



(b)

Figure 2-1: Current-starved VCDU (a) Schematic, (b) Timing diagram.

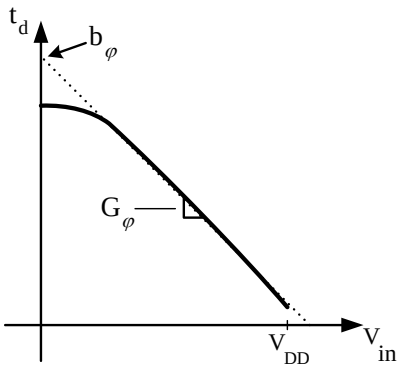


Figure 2-2: Transfer characteristic of the current-starved VCDU.

$$t_d = \frac{(V_{DD} - V_{TH})C}{I} \tag{2.1}$$

An approximate transfer characteristic of a VCDU is shown in Figure 2-2. This plot is obtained by measuring the VCDU propagation delay while sweeping the input control voltage V_{in}. For input levels below the threshold voltage of M_1, the delay is large, unreliable and, for the most part, unusable. As the voltage exceeds the V_{TH} of M_1, the delay begins to decreases in a linear way towards its minimum delay at V_{DD}. It is noteworthy that the VCDU should be operated well above the threshold voltage of M_1 to avoid nonlinearities in the delay-voltage transfer characteristic. A voltage-to-time conversion gain (G_φ) can be defined as the slope of this curve in its linear region, allowing one to describe the delay-voltage transfer characteristic as follows

$$t_d = G_\varphi V_{in} + b_\varphi \tag{2.2}$$

where b_φ is the y-intercept of the line fitted on the linear region.

The gain term G_φ can be controlled by M_1's sizing and will be used in the following chapters for scaling time-mode signals. Mathematically this parameter can be approximated as follows,

$$G_\varphi = \frac{\partial t_d}{\partial v_{in}} = \frac{\partial t_d}{\partial I} \cdot \frac{\partial I}{\partial v_{in}}, \tag{2.3}$$

where I is the discharging current flowing through M_1 in the saturation region. This current can be described as

$$I = \frac{1}{2} k_n^{'} \frac{W_1}{L_1} (v_{in} - V_{tn})^2 \tag{2.4}$$

where V_{tn} is the threshold voltage of M_1 as opposed to V_{TH} being the threshold of the gate. Taking the derivative of Equation (2.4), we get

$$\frac{\partial I}{\partial V_{in}} = k_n^{'} \frac{W_1}{L_1} (V_{in} - V_{tn}). \tag{2.5}$$

Similarly, taking the derivative of the delay expression seen in Equation (2.1) with respect to current I, we get

$$\frac{\partial t_d}{\partial I} = \frac{-C(V_{DD} - V_{TH})}{I^2} = \frac{-4C(V_{DD} - V_{TH})}{(k_n^{'} \frac{W_1}{L_1})^2 (V_{in} - V_{tn})^4} \tag{2.6}$$

Substituting Equations (2.5) and (2.6) into Equation (2.3) yields:

$$G_{\varphi} = \frac{\partial t_d}{\partial V_{in}} = \frac{-4L_1 C(V_{DD} - V_{TH})}{k_n' W_1 (V_{in} - V_{tn})^3} \tag{2.7}$$

It can be recognized from Equation (2.7) that the following relationships exist:

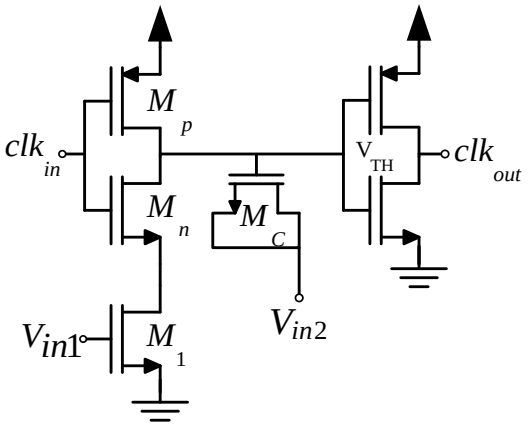
$$\left|G_{\varphi}\right| \propto L_1 \tag{2.8}$$

$$\left|G_{\varphi}\right| \propto {}^{1}/_{W_1} \tag{2.9}$$

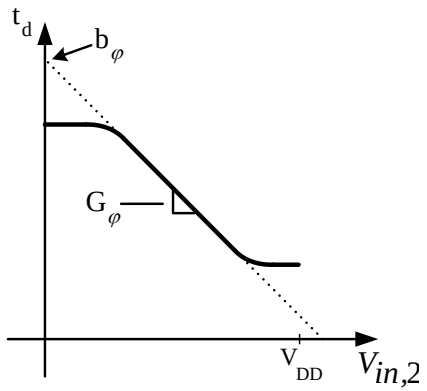
Equations (2.8) and (2.9) suggest that the conversion gain is directly proportional to M_1's length and inversely proportional to M_1's width. For instance, a long narrow device has to be used in a high gain VCDU. Since most building blocks in TMSP utilize VCDUs as their core elements, the above insights are useful when sizing the transistors of a VCDU.

2.1.2 Varactor-Based VCDUs

Another way of controlling the delay of a VCDU is shown in Figure 2-3(a). In this method the capacitor is replaced with a varactor connected between the internal node of the VCDU and an additional input voltage-controlled node denoted by $V_{in,2}$. As before, with a slight change of notation, the gate of M_1 is connected to input $V_{in,1}$. The two inputs $V_{in,1}$ and $V_{in,2}$, collectively control the propagation delay of the VCDU. In order to set the discharge current to a constant value, $V_{in,1}$ is normally set to a constant voltage, say V_b.



(a)



(b)

Figure 2-3: Varactor-based VCDU (a) Schematic, (b) Transfer characteristic.

The timing diagram associated with this varactor-based VCDU is identical to that for the current-starved VCDU shown in Figure 2-1(b). However, its transfer characteristic shown in Figure 2-3(b) has a slightly different appearance. Specifically, for input voltages approaching V_{DD}, the VCDU begins to saturate unlike the previous case.

Other linearity analysis reveals that the varactor-based VCDU has greater linearity for mid-range voltages.

The conversion gain of the varactor-based VCDU is found as follows; as the capacitance C_{var} of the varactor is proportional to V_m-$V_{in,2}$, we can write

$$C_{var} = \alpha W_c L_c \left(V_m - V_{in,2}\right) + C_{min} \tag{2.10}$$

Where W_C and L_C are the dimensions of the varactor transistor M_C, α is a proportionality factor, and C_{min} is the minimum capacitor present at that node. To simplify the analysis, we shall assume that the internal node voltage V_m is held constant at its precharge level of V_{DD} over the entire discharge cycle. Hence we can write the varactor capacitance as

$$C_{var} = \alpha W_c L_c \left(V_{DD} - V_{in,2}\right) + C_{min} \tag{2.11}$$

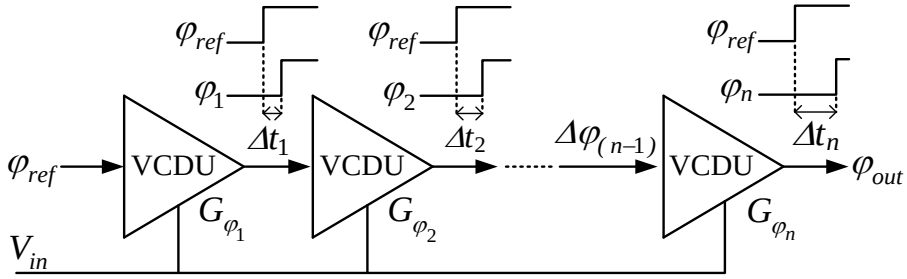
Substituting this result back into Equation (2.1), we obtain an expression for the propagation delay of the varactor-based VCDU as follows:

$$t_d = \frac{\alpha W_c L_c \left(V_{DD} - V_{in,2}\right)(V_{DD} - V_{TH})}{I} + \frac{C_{min}\,(V_{DD} - V_{TH})}{I} \tag{2.12}$$

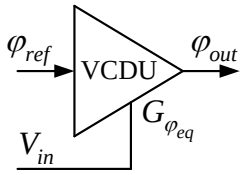
Here the second term on the right hand side of the equation is the fixed minimum propagation delay associated with the VCDU, while the first term is the controllable delay of this block which is a function of $V_{in,2}$. Therefore, the conversion gain can be approximated according to Equation (2.3) as follows

$$G_{\varphi} \equiv \frac{\partial t_d}{\partial V_{in,2}} \approx -\frac{\alpha W_c L_c (V_{DD} - V_{TH})}{I} \tag{2.13}$$

As is self-evident, the conversion gain G_{ϕ} is proportional to both W_c and L_c. Equation (2.13) suggests that a high conversion gain is achievable by using a long and wide device for M_C. However, this will cause the VCDU propagation delay t_d to increase according to Equation (2.12), which in turn increases the discharge time of the VCDU. This leads to longer wait times before the VCDU can be reused (i.e., reduced operating frequency).



(a)



(b)

Figure 2-4: Cascade of VCDUs (a) *n*-stage scheme, (b) equivalent scheme.

2.2 High-Gain VCDU

VCDUs usually provide conversion gains up to a few hundreds of picoseconds per volt in a 0.18/0.13 micron CMOS technology, although this may not be enough in some applications. A cascade of several VCDUs like the one depicted in Figure 2-4(a) can be utilized in order to boost up the gain. For an input control voltage Vin, the delay Δt_1 of the first VCDU can be described in terms of the conversion gain $G_{\varphi 1}$ and time offset b_{φ_1}, as follows

$$\Delta t_1 = G_{\varphi 1} \cdot V_{in} + b_{\varphi_1} \tag{2.14}$$

This time difference variable is given to the second VCDU as input, leading to the output delay Δt_2 of the second VCDU as

$$\Delta t_2 = \Delta t_1 + G_{\varphi 2} \cdot V_{in} + b_{\varphi_2} \tag{2.15}$$

where $G_{\varphi 2}$ and b_{φ_2} represents the conversion gain and time offset of the second VCDU. The delaying action goes forward to the end of VCDU chain where the final output Δt_n is generated. Using the same recursive notation, we write this total delay Δt_n in terms of the previous VCDU output delay as follows

$$\Delta t_n = \Delta t_{n-1} + G_{\varphi n} \cdot V_{in} + b_{\varphi_n} \tag{2.16}$$

where $G_{\varphi n}$ and b_{φ_n} represents the conversion gain and time offset of the nth-VCDU. Replacing the Δt_{n-1} by the previous equations describing *(n-1)*th, *(n-2)*th stages and so on, will result in

$$\Delta t_n = G_{\varphi 1} \cdot V_{in} + G_{\varphi 2} \cdot V_{in} + \cdots + G_{\varphi n} \cdot V_{in} + \sum_{i=1}^{n} b_{\varphi_i}$$

$$= \left(G_{\varphi 1} + G_{\varphi 2} + \cdots + G_{\varphi n}\right).V_{in} + \sum_{i=1}^{n} b_{\varphi_i} \tag{2.17}$$

where $\sum_{i=1}^{n} b_{\varphi_i}$ is basically the amount of fixed DC (or constant) delay introduced by the chain of VCDUs. Equation (2.17) reveals that the cascade of VCDUs acts as one equivalent delay block, shown in Figure 2-4(b), which has a net conversion gain equal to the summation of individual conversion gains, i.e.,

$$G_{\varphi_{eq}} = G_{\varphi 1} + G_{\varphi 2} + \cdots + G_{\varphi n} \tag{2.18}$$

Cascading VCDUs, in addition to increasing the overall conversion gain, acts as an adder of time-variables, e.g., $\Delta t_n = \Delta t_1 + \Delta t_2 + \ldots + \Delta t_{n-1}$. This idea will be extended later on in this chapter.

2.3 Voltage-to-Time Converter

A voltage-to-time converter (VTC) is used to convert analog input voltages to time-mode signals and it is constructed using a single VCDU structure as shown in Figure 2-5(a). The VCDU is fed with input voltage V_{in} and a reference clock denoted by φ_{ref}. On account of the propagation delay of the VCDU, the rising edge of the output signal φ_{out} relative to the edge of the input signal will appear some time later, say Δt_{out}, as shown in Figure 2-5(b). If we model the VCDU in a linear manner as described by Equation (2.2), the output time difference variable (Δt_{out}) can be described in terms of the input voltage V_{in} as follows

$$\Delta t_{out} = G_{\varphi} V_{in} + b_{\varphi} \tag{2.19}$$

where G_{φ} and b_{φ} is the conversion gain and time offset of the VCDU.

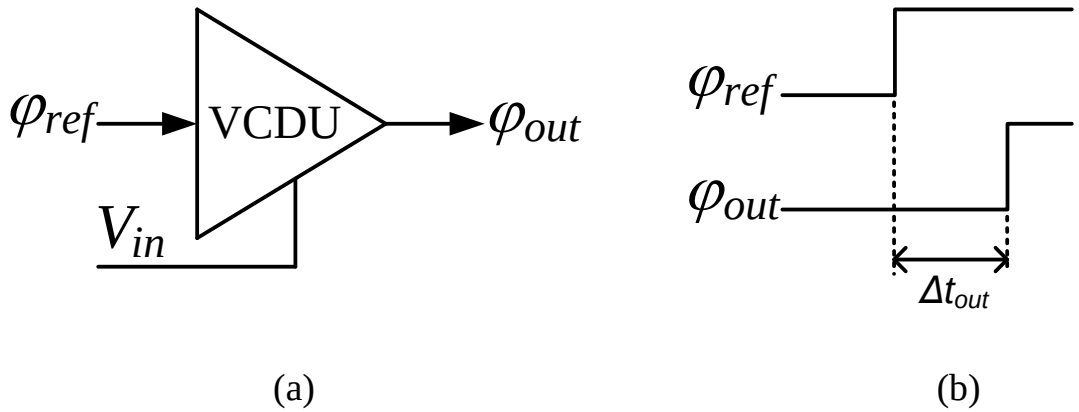


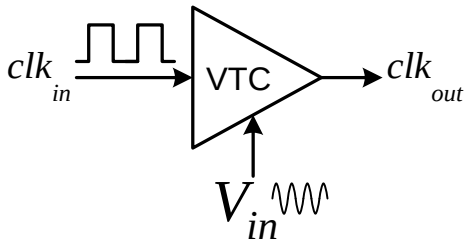
Figure 2-5: Voltage-to-Time Converter (VTC) (a) symbolic representation, (b) timing diagram.

2.3.1 Aliasing in TM-Signals

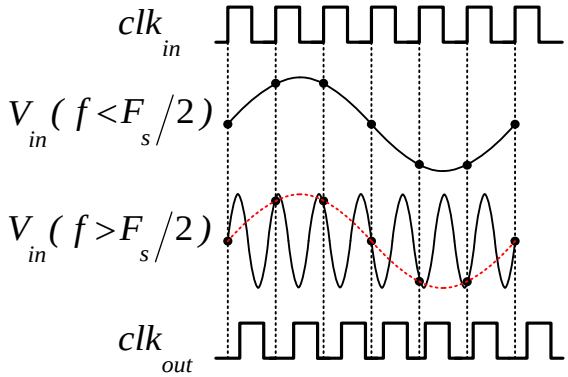
Due to the sampling action associated with the internal operation of a VCDU, one has to note that the maximum frequency component present in V_{in} must be less than one-half the sampling rate F_S according to the Nyquist sampling theorem. This implies that we cannot generate a time-mode signal that carries a message signal with frequency content above $F_S/2$. This concept is captured in both the time and frequency domains, shown in Figure 2-6. In part (a) the input and output clock signals from a VCDU are shown together with the input voltage signal for two different cases. The first case illustrates the input voltage signal that is sampled by the input clock that satisfies the Nyquist theorem, i.e., the sine wave is sampled with more than 2 points per period. The phase of the output clock is modulated with respect to these samples, i.e., the distance between the output edge and input reference edge is proportional to the sampled value. The second case illustrates the situation where the input signal has a frequency component that is above the Nyquist frequency $F_S/2$. When sampled by the input clock, the sample set contains less than 2 points per period but is equivalent to samples derived from the low frequency signal (i.e., aliased back) as shown in the middle diagram of Figure 2-6(a) as a dash line. As a result, the output signal is identical under the two separate input conditions.

Figure 2-6(b) illustrates the sampling and aliasing process in the frequency domain. Specifically, this figure illustrates how the high-frequency voltage domain signal

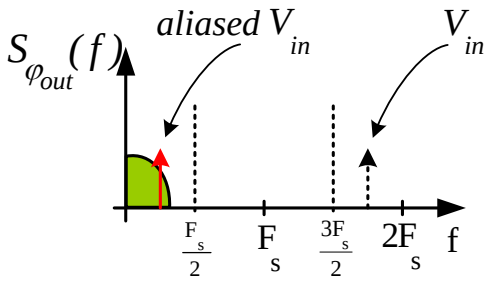
when sampled is translated back within the Nyquist interval of the sampling process. Like all sampling systems, the effects of aliasing must be eliminated through the appropriate filtering action prior to sampling.



(a)



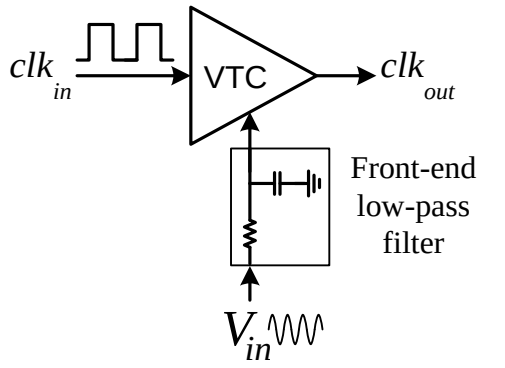
(b)



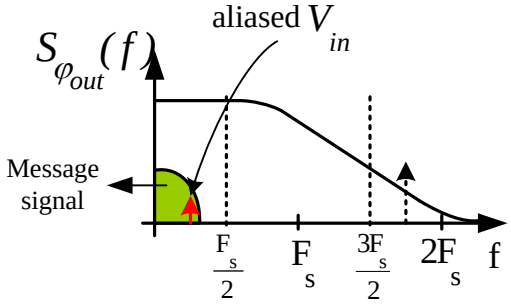
(c)

Figure 2-6: Time-mode signals generated by a VTC with and without aliasing (a) symbolic representation, (b) time domain representation, (b) in frequency domain representation.

One way of getting rid of out-of-band noise is to use an anti-aliasing voltage-mode low-pass filter with a bandwidth slightly greater than $F_S/2$ in series with the input voltage signal V_{in}. This technique is illustrated in Figure 2-7(a) with a simple first-order RC-filter. Here, the filter attenuates the out-of-band high-frequency components associated with the input voltage (V_{in}) while allowing the message signal to pass unchanged. Figure 2-7(b) illustrates the frequency spectrum of the output time-domain signal when the alias component has been significantly reduced due to the front-end voltage-domain filter.



(a)



(b)

Figure 2-7: Input voltage pre-filtering (a) schematic representation, (b) frequency domain illustration.

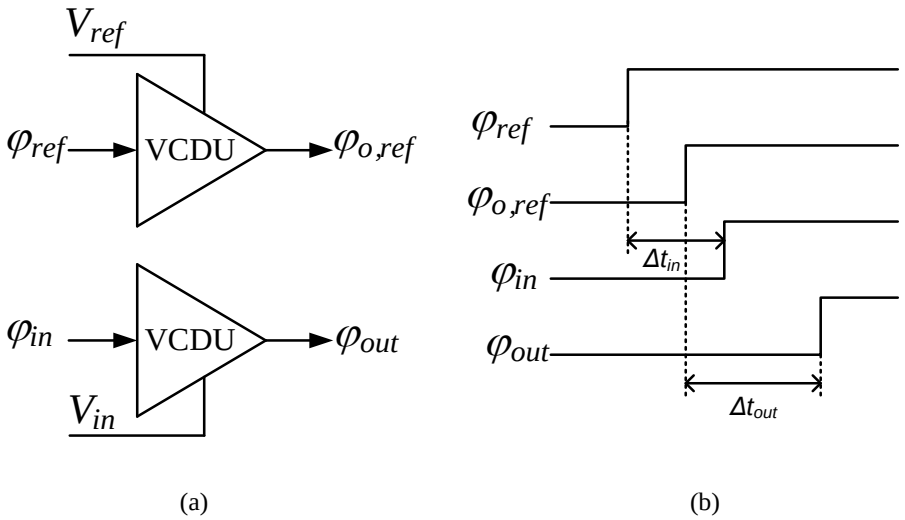


Figure 2-8: Voltage-to-time adder (a) symbolic representation, (b) timing diagram.

2.4 Voltage-to-Time Adder

Voltage-to-time addition is implemented using two VCDUs as shown in Figure 2-8(a). In this scheme two different input unit-step-like signals (φ_{ref} and φ_{in}) are used to excite two identical VCDUs, while they are fed with a reference voltage, V_{ref}, and V_{in}, respectively. Let us assume that the edge of the reference signal occurs at time t_{ref} and that of the input signal at time t_{in}. Consequently, the location of the edge of the two outputs from the VCDUs can be described as follows,

$$t_{o,ref} = t_{ref} + G_{\varphi} V_{ref} + b_{\varphi} \tag{2.20}$$

$$t_{out} = t_{in} + G_{\varphi} V_{in} + b_{\varphi} \tag{2.21}$$

Hence, the time difference between the two output edges (denoted as Δt_{out}) is given by

$$\Delta t_{out} = t_{out} - t_{o,ref} = (t_{in} - t_{ref}) + G_{\varphi}(V_{in} - V_{ref})$$

$$= \Delta t_{in} + G_{\varphi}(v_{IN}) \tag{2.22}$$

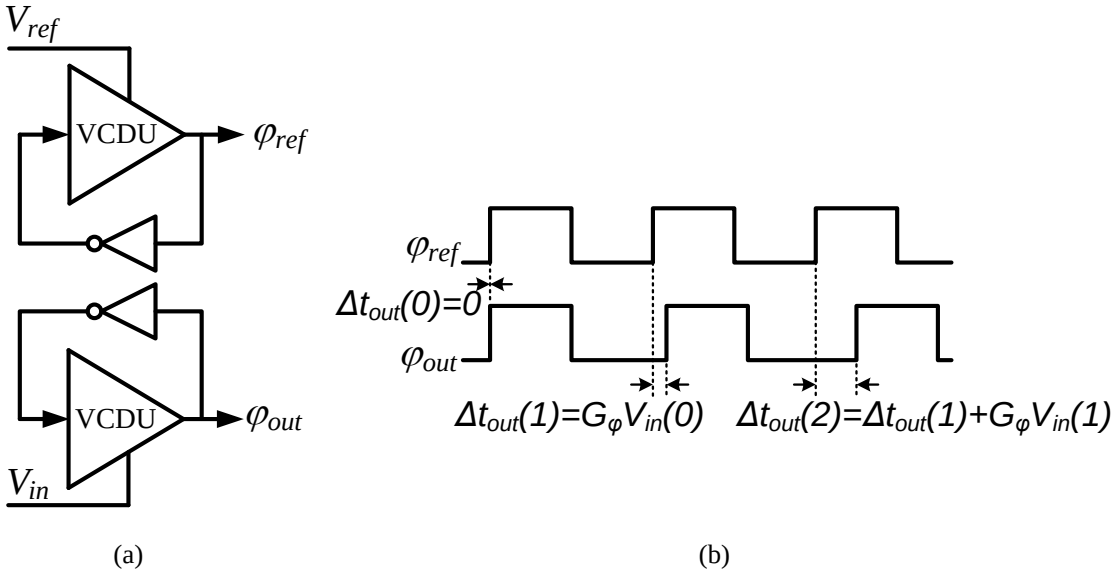
Here the input voltage is converted to a time-mode signal and added to the input time-mode signal.

2.5 Voltage-to-Time Integrator

Voltage-to-time integrator consists of a voltage-to-time adder whose outputs are fed back to its input through an inverter. It was first introduced and used in a time-mode first-order sigma-delta modulator [6]. This structure, shown in Figure 2-9(a), resembles two voltage-controlled oscillators. The top and bottom oscillators are controlled by V_{ref} and V_{in} generating the reference and output signals, φ_{ref} and φ_{out}, respectively. The frequency of oscillation is determined by the control voltages and sizing of the VCDUs and inverters. As illustrated in the timing diagram of Figure 2-9(b), during the first cycle, both the reference and output edges are aligned resulting in a zero time difference. For the second cycle, a delay is established between reference and output signals, φ_{ref} and φ_{out}, proportional to the previous voltage sample. From this point forward each output time difference consists of accumulation of previous time differences and the sampled

input controlled voltage scaled by G_φ. The following equation describes the general difference equation for this voltage-to-time integration operation,

$$\Delta t_{out}(n) = \Delta t_{out}(n-1) + G_\varphi V_{in}(n-1) \tag{2.23}$$



(a) (b)

Figure 2-9: Voltage-to-time integrator (a) symbolic representation, (b) timing diagram.

2.6 Time Amplifier

A time amplifier (TAMP), similar to its voltage-domain counterpart, is responsible for taking the time difference variable between two events, defined here as the difference between two rising edges of a reference and arbitrary signal, and scaling their difference by some scale factor G_{TA}. This operation is illustrated using the symbolic

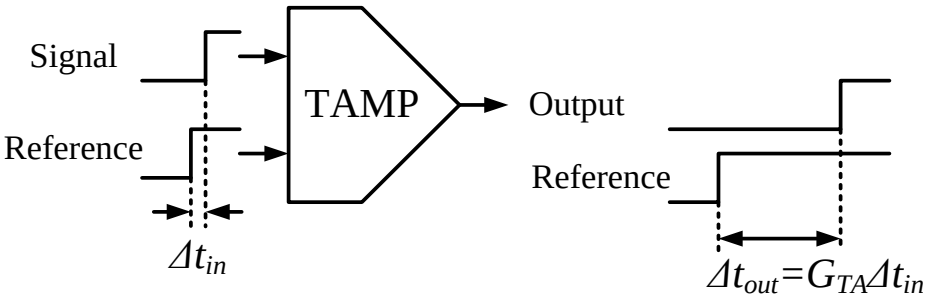


Figure 2-10: Symbolic representation of a time amplifier

representation shown in Figure 2-10 where the output time difference is expressed in terms of the input time difference according to

$$\Delta t_{out} = G_{TA}\Delta t_{in} \tag{2.24}$$

Time amplifiers can be used at the front-ends of time-mode circuits in order to increase the dynamic range of a data conversion system [7].

The concept of a time amplifier was first used back in the seventies by Hewlett Packard (HP) for time-stretching clock signals in order to determine their frequencies. At the time, HP referred to the circuit as a time-stretcher. Since that time, the idea was reinvented and re-labeled as a time-amplifier. The next reference to a time amplifier that appear in the open literature was that of A. M. Abas *et al* where a mutual-exclusive (MUTEX) circuit (Figure 2-11) was used [8]. In this circuit two cross-coupled NANDs together with the two cross-coupled inverter circuits are used to establish a bistable circuit whose output is proportional to the time difference between the two input signals. Unfortunately, this circuit exploits the meta-stable behavior of a bistable system whereby

large time amplification is possible only for very small input time-differences. This severely limits the dynamic range of this time amplifier.

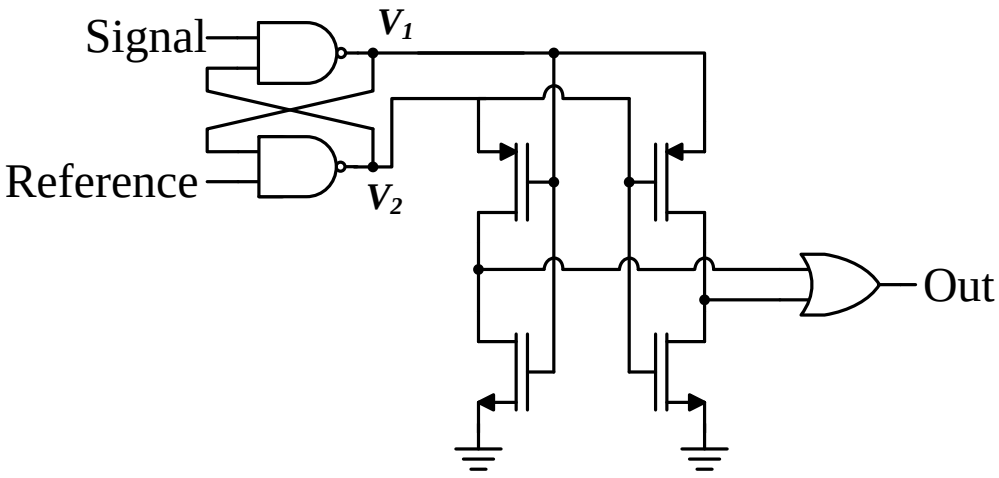
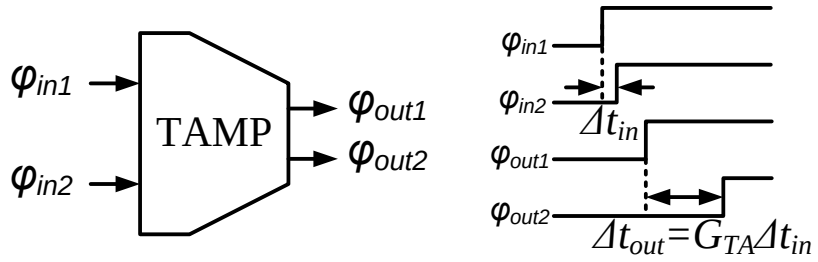


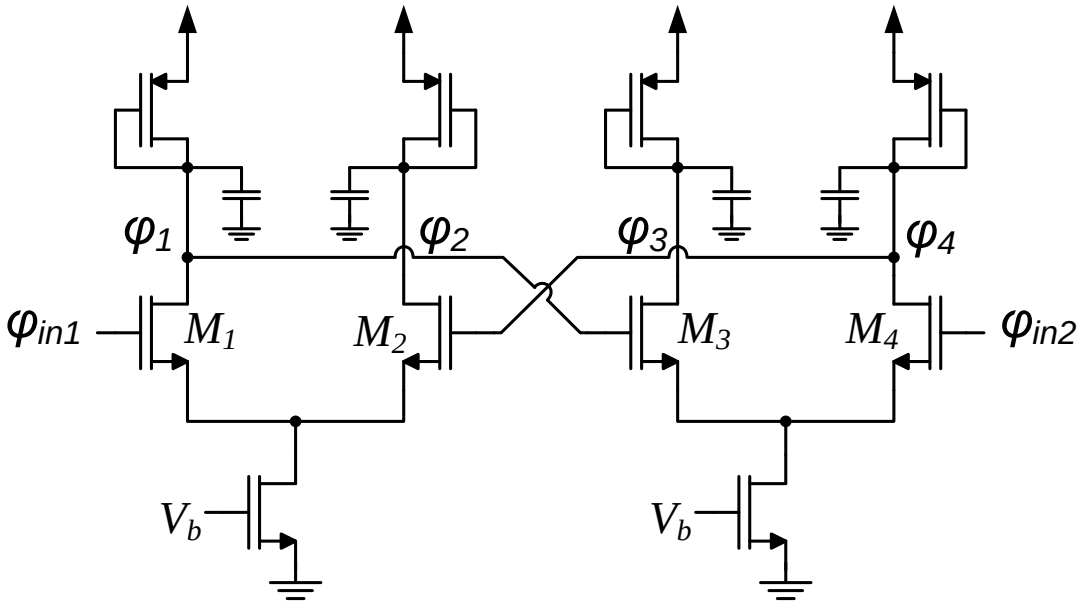
Figure 2-11: Circuit schematic of a MUTEX time amplifier

A second approach for time amplification was introduced in [7] and is illustrated in Figure 2-12. A block diagram of this TAMP is shown in Figure 2-12(a) where the time-difference between two input signals is scaled by some factor G_{TA} and captured by the time-difference between the output of two signals. This is in contrast to the previous TAMP of Figure 2-10 where the time difference is establish with respect to a reference signal.

The circuit diagram for this TAMP is shown in Figure 2-12(b). It consists of two cross-coupled differential pairs loaded by a diode-connected PMOS in parallel with a capacitor. The latter two components form an equivalent RC-circuit at each node of each differential pair and establish the charging/discharging rate of each node. Prior to the



(a)



(b)

Figure 2-12: Single-stage time amplifier (a) symbolic representation and timing diagram, (b) circuit schematic.

arrival of a rising transition at the input of the TAMP, the differential pairs are in a quite state, whereby the drain of M_1 and M_4 are in a logic high state, and the drain of M_2 and M_3 are in a logic low state. On the arrival of the first edge, say at the gate of M_1, the drain of M_1 is discharged towards ground and the drain of M_2 is charged towards V_{DD}. Some

time later, the second edge arrives on the gate of M_4 causing similar action to occur at the drain nodes of the M_3 and M_4. A sense circuit, specifically a voltage comparator, is connected to the output of each differential amplifier and creates the two output signals, φ_{out1} and φ_{out2}. The sense circuit simply looks for when the voltage difference between the drains of each differential amplifier equals one another. By sizing the loads of each differential amplifier, the gain G_{TA} of the TAMP can be established. Most importantly, the gain of this amplifier is independent of the input time-difference and thus has a wider dynamic range than the previous TAMP of Figure 2-11.

2.7 Time-to-Digital Conversion

Time-to-digital conversion (TDC) is the equivalent to analog-to-digital conversion (ADC), except that one operates with time-mode variables whereas the other uses voltage-domain variables. In the following subsections, the basic building blocks of the time-to-digital conversion process will be described. In addition, some time-to-digital converter (TDC) architectures will be studied.

2.7.1 Time Comparator

An important element of most time-mode signal processing algorithms is the ability to decide whether one time edge is ahead or behind another. The building block that is responsible for this decision is called a time comparator. This block can be easily realized with an edge-triggered D-type flip-flop, as shown in Figure 2-13, where the input

signal (φ_{in}) is connected to the D-input and the reference signal (φ_{ref}) is directed to the clock input. If the 0-1 transition of φ_{in} arrives before that of the φ_{ref}, the output of the flip-flop will be in the logic 1 state, otherwise it remains in the logic 0 state.

For very small time-differences, the D flip-flop will suffer from metastability, which may lead to a wrong decision. Time amplifiers can be effectively used in this case in order to alleviate this issue by pre-amplifying the input time-difference above the metastability region of the flip-flop [7].

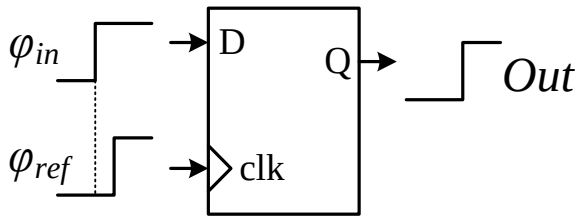


Figure 2-13: Time comparator implemented using an edge-triggered D flip-flop

2.7.2 Time-to-Digital Converter

Many of the TDCs in practice today involve the same signal processing algorithms as those used for ADCs. A popular TDC imitating a flash type of ADC architecture [9] is shown in Figure 2-14. Here a Vernier delay line is used to control the delay of two input signals. The delay associated with one side of the Vernier delay line is faster than the delay on the other side. By doing so, the time-difference of the signals arriving at the inputs of each flip-flop gets progressively shorter until the signals cross over one another. This comparison is made by each D-type flip-flop acting as a time

comparator whose output represents one bit in an *N*-bit thermometer code. This code can then be converted to a one-complement binary format using a Wallace adder. The output code represents the time difference between the input and reference edges. This technique achieves a time resolution equal to the time difference between the delay of the fast and slow delay elements making up the Vernier delay line. The whole circuit, especially the two delay lines, must be laid out carefully in order to reduce the local mismatches introduced during the manufacturing process. Global process variation is often tackled through the application of a delay-look loop technique, where each delay element is phase-locked to a reference oscillator. By doing so, a delay of say t_p seconds can be precisely controlled by an external crystal oscillator.

Many TDC architectures using a phase locking approach have been described such as [10], [11], and [12].

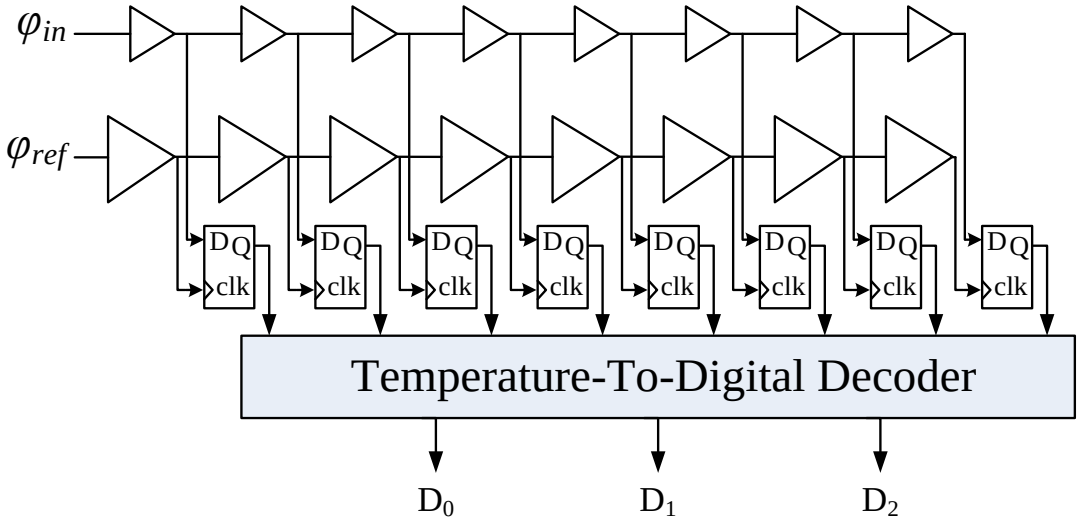
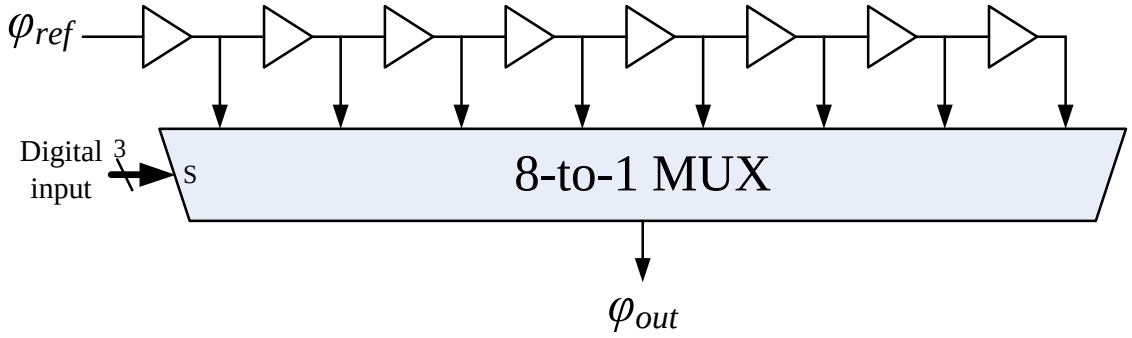
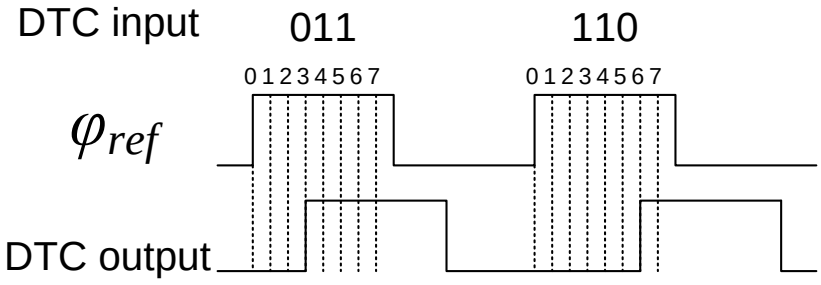


Figure 2-14: A 3-bit Vernier Delay based Flash Time-to-Digital Converter.



(a)



(b)

Figure 2-15: A 3-bit DTC (a) general scheme, (b) input-output relationship.

2.8 Digital-to-Time Conversion

Digital-to-time conversion is the reverse of the time-to-digital conversion process whereby a digital word is converted to high-precision TM signal. In the following section the general scheme of a digital-to-time converter (DTC) will be described.

2.8.1 Digital-to-Time Converter

Digital-to-time converters are critical components of automatic test equipments (ATE), measurement instruments and direct-digital synthesizers (DDS). A DTC as shown

in Figure 2-15(a) in its simplest form consists of a reference signal, a delay line and a multiplexer (MUX). The delay line consists of a number of delays elements, such as voltage buffers, which acts to delay the propagation of an input reference signal (φ_{ref}) across the inputs to an *N*-bit multiplexer (3-bit MUX is shown in the diagram). The MUX will select the appropriate delayed signal corresponding to the input digital code and pass that signal as its output. Figure 2-15(b) depicts a 3-bit DTC input-output relationship. A three-bit digital input requires eight specific levels in time, which are usually spread evenly across half a period of the reference signal. The DTC is responsible for placing the output edge at the correct point in time, determined by the digital input.

2.9 Multi-Input Time-Mode Adder

A multi-input adder circuit performs the function of adding several time-difference inputs together (e.g., $\varphi_1(n-1)$, $\varphi_2(n-1)$, …, $\varphi_n(n-1)$) and producing an output $\varphi_{out}(n)$ which is the sum of all input time-differences, i.e.,

$$\varphi_{out}(n) = K_1\varphi_1(n-1) + K_2\varphi_2(n-1) + \cdots + K_n\varphi_n(n-1) \tag{2.25}$$

Here K_i is the scaling coefficient of the *i*th-input. Taking the *z*-transform of each side of the Equation (2.25) results in

$$\Phi_{out}(z) = z^{-1}[K_1\Phi_1(z) + K_2\Phi_2(z) + \cdots + K_n\Phi_n(z)] \tag{2.26}$$

Figure 2-16 shows the block diagram of such a circuit, where input signals are weighted, added, and delayed by one clock cycle. The one period delay is necessary as will be described later in this section.

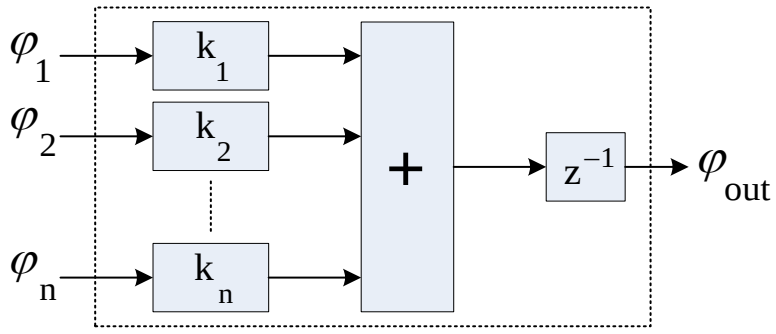


Figure 2-16: Block diagram of a multi-input TM adder.

2.9.1 Circuit Realization

The circuit realization of the adder is shown in Figure 2-17(a). Here the circuit consists of a cascade of VCDUs whose control voltage is a function of individual input time-differences taken with respect to a master clock, *clk*. The input to the first VCDU is a reference edge φ_{ref}, which is further delayed by an amount of time established by the gain of the VCDU. Its output is then fed into the input of the next VCDU stage, and so on. Time addition is in effect the act of moving the reference edge forward in time in direct proportion to the individual time-differences.

In Section 2.2 the cascade of a set of VCDUs all controlled from a single voltage level was investigated. Adopting a similar approach, but using separate control voltages for each VCDU, φ_{out} can be written as follows

$$\varphi_{out} = G_{\varphi 1} \cdot V_{C1} + G_{\varphi 2} \cdot V_{C2} + \cdots + G_{\varphi n} \cdot V_{Cn} + \sum_{i=1}^{n} b_{\varphi_i} \tag{2.27}$$

Here the control voltages V_{C1}, $V_{C2,}$ … and V_{Cn} are generated by a separate analog circuit or block that takes as input a time difference between a signal φ_i and a reference clock, *clk*. These control voltages are directly proportional to the input time-difference variable, φ_i's. Hence, one can write

$$V_{Ci} = k\varphi_i \tag{2.28}$$

where k is a proportionality factor that is the same for each VCDU. Replacing Equation (2.28) in Equation (2.27) yields:

$$\varphi_{out} = G_{\varphi 1} \cdot k \cdot \varphi_1 + G_{\varphi 2} \cdot k \cdot \varphi_2 + \cdots + G_{\varphi n} \cdot k \cdot \varphi_n + \sum_{i=1}^{n} b_{\varphi_i} \tag{2.29}$$

Substituting $K_i = kG_{\varphi i}$ for each stage, Equation (2.29) reduces to

$$\varphi_{out} = K_1 \cdot \varphi_1 + K_2 \cdot \varphi_2 + \cdots + K_n \cdot \varphi_n + \sum_{i=1}^{n} b_{\varphi_i} \tag{2.30}$$

By selecting the appropriate conversion gain (G_φ) for each VCDU using the design principles of Section 2.1, proper scaling and summation of several time-mode signals can be achieved.

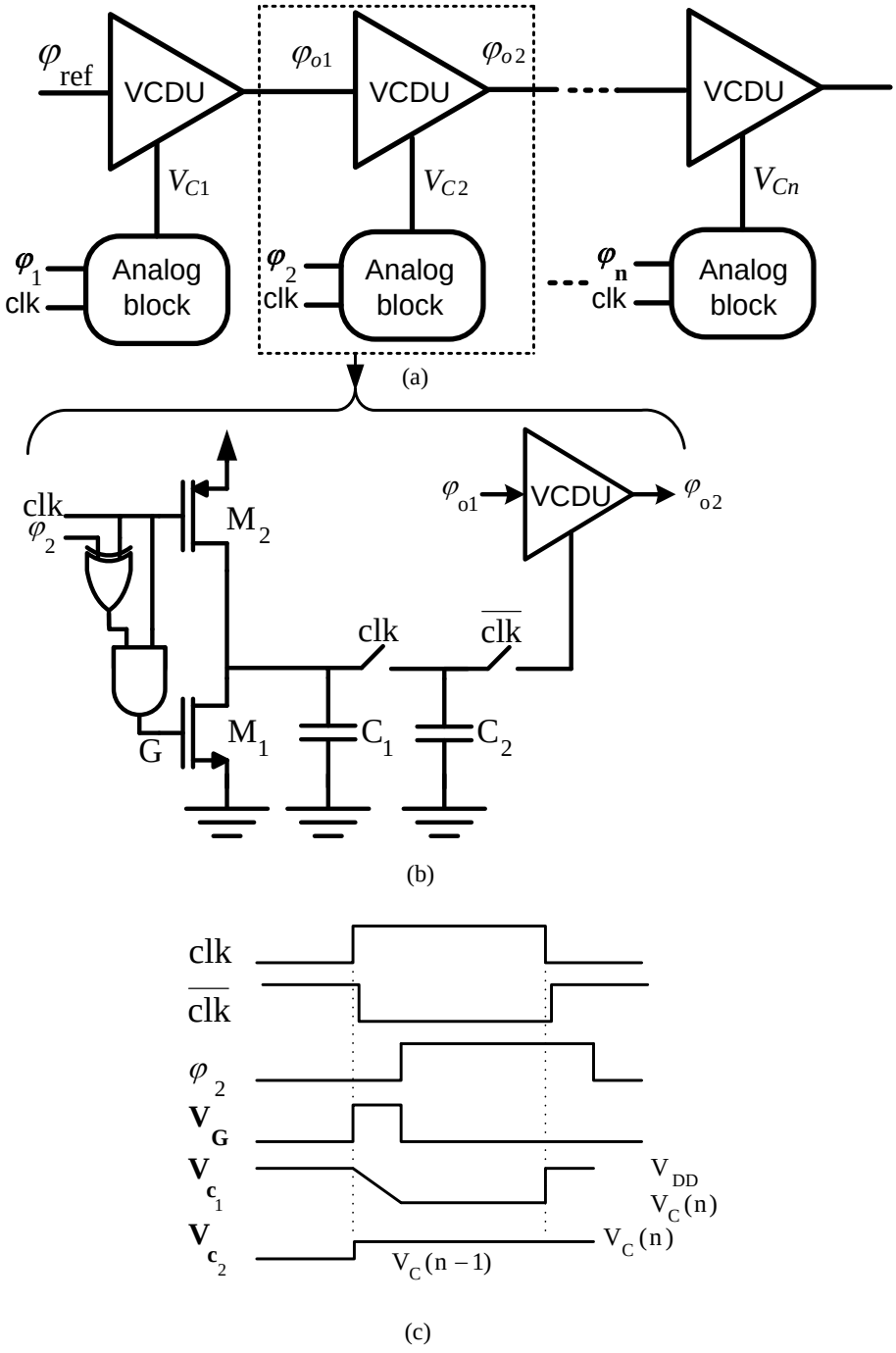


Figure 2-17: Multi-input time adder: (a) symbolic representation, (b) analog block schematic circuit, (c) timing diagram.

The circuit details of a single stage of the adder and its corresponding waveforms are illustrated in Figure 2-17(b) and Figure 2-17(c). This circuit extracts the input time difference signal using a few digital gates when the *clk* input is high and, subsequently, develops the appropriate voltage on capacitor C_1 by partially discharging it from a full charge. This voltage is at the same time copied onto capacitor C_2. When the *clk* input goes low, the resulting voltage level is applied to the VCDU, which sets its according to its transfer characteristic. For this application the VCDU introduced in Figure 2-1 is employed. As the linear region of this VCDU extends to V_{DD} but not V_{SS}, C_1 is precharged to V_{DD} in order to maximize its dynamic range of operation. The ratio of C_1 to C_2 has to be chosen carefully in order to reduce charge-sharing effects. The voltage established on C_2 is essentially the same as the voltage on C_1, as the sampling rate is high relative to the input signal bandwidth, i.e., high oversampling ratio. In other words, little charge sharing is observed in normal operation. The applied voltage on the VCDU's control line is sampled at the rising edge of the reference signal of each stage, i.e. φ_{ref}, φ_{o1}, φ_{o2}, etc..

In order to avoid casualty issues associated with the multi-input adder of Figure 2-17(a), several timing issues are imposed:

(1) Each VCDU of the multi-input adder is clocked with master clock, *clk*, and

(2) The input reference signal φ_{ref} is derived from an inverted version of the master clock, denoted as $\overline{clk}$.

In Equation (2.29), $\sum_{i=1}^{n} b_{\varphi_i}$ is a fixed amount of delay associated with the chain of VCDUs. Proper design of this variable enables the output edge of the adder φ_{out} to be available on the next rising edge of the master clock, *clk*. As a result, the output signal always lags behind the inputs by one period, which we refer to as the realizability constraint of TM adders.

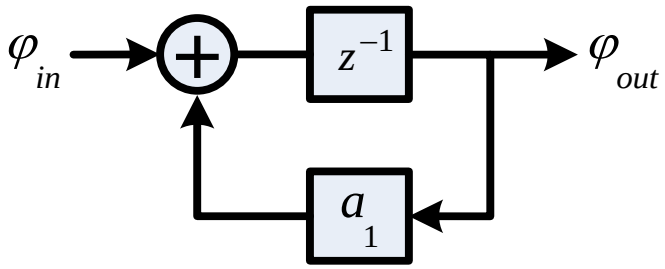
2.10 Time Integrator

A time integrator can be realized using a two-input adder in a feedback loop, where the input signal is connected to one input and the output of the adder is fed back into the other input. As shown in the signal flow graph of Figure 2-18(a), the inherent one period delay associated with a time adder is exploited here to form a damped integrator. One can easily show that the block diagram of Figure 2-18(a) has the following transfer function,

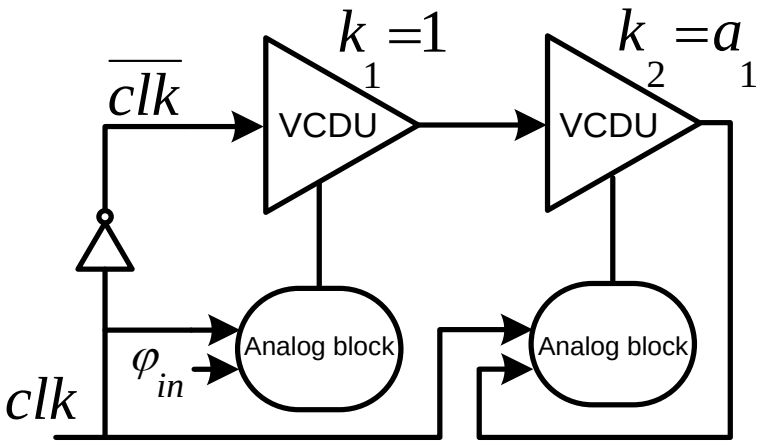
$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = \frac{z^{-1}}{1 - a_1 z^{-1}} \tag{2.31}$$

For stable operation, i.e., pole inside the unit circle, the condition $0 < a_1 < 1$ must be satisfied. Figure 2-18(b) illustrates a simplified representation of the integrator in term of

a two-input adder. Such a representation makes it easier to see the key details of the integrator. We shall make use of this representation again in Chapter 3.



(a)



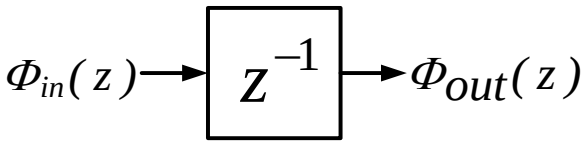
(b)

Figure 2-18: Time-mode integrator (a) block diagram, (b) symbolic representation.

2.11 Unit Delay

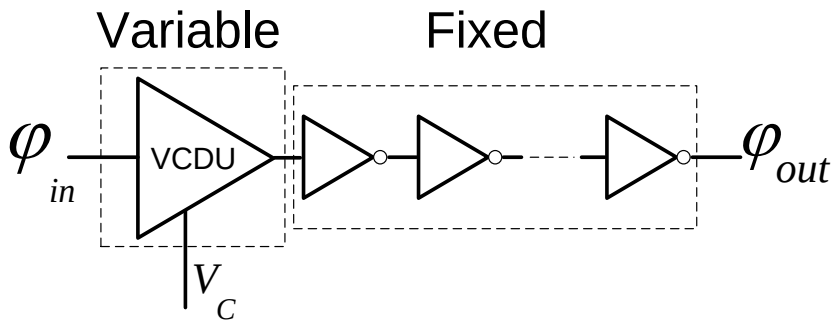
A unit delay block or circuit acts to delay its time-mode input signal by one complete clock cycle. Usually a VCDU followed by a chain of inverters are used to implement this block. The tuning ability of the VCDU is used to correct for errors in the

delay block that are caused by manufacturing processing effects. Figure 2-19(a) depicts the block diagram of a unit delay followed by its corresponding discrete-time equation, while Figure 2-19(b) shows the symbolic representation of this block.



$$\Phi_{out}(z) = z^{-1}\Phi_{in}(z)$$

(a)



(b)

Figure 2-19: Unit delay (a) block diagram, (b) symbolic representation.

2.12 Summary

In this chapter the basic building blocks used in TMSP were investigated at the block and circuit levels. These blocks are generally used for two purposes:

First, the conversion of time-mode signals to voltage-mode ones (and vice versa). Blocks that perform this function include voltage-to-time converters, time-to-digital converters, digital-to-time converters, voltage-to-time adders and voltage-to-time integrators.

Secondly, blocks that directly manipulate time-mode signals in some mathematical fashion. Such blocks described include time-mode adders, time amplifiers, time-mode integrators and unit delays.

These blocks will be used in the following chapters in order to build more complex time-mode circuits, specifically time-mode IIR low-pass filters.

Chapter 3

First-Order Time-Mode Filtering

Time-mode filtering was originally introduced in [13], in which filtering action takes place on time-difference signals. The concept of time-mode filtering is shown in Figure 3-1 where a low-pass time-mode filter is employed in a phase reconstruction application. Here the input is assumed to come from some digital-to-time conversion operation where the output signal is phase-encoded over a few discrete levels resulting in a staircase-like appearance. After passing through the linear time-domain filter with transfer function *H(z)*, the output signal is a smooth function of time, occupying almost any level bounded between its peak-to-peak value. This is a result of the averaging that takes place inside the time-domain filter using a real-value numbering system. It is noteworthy here to mention that time-mode filters have the same input-output functionality as a phase-lock loop but requires a lot less power and silicon area. This makes them ideal candidates for phase reconstruction applications. This is one of the main contributions of this thesis.

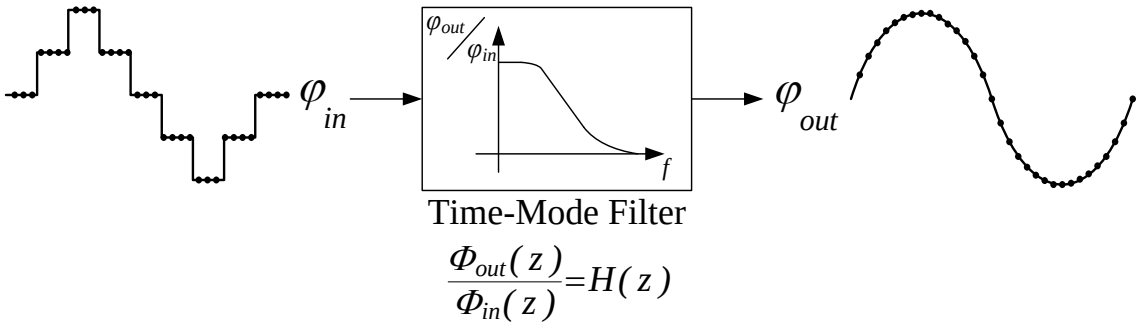


Figure 3-1: TM-filtering concept

In this chapter the required building blocks for realization of a 1st-order TM-filter will be explained. Next, this filter is modeled in MATLAB/Simulink in order to verify its functionality. Subsequently, experimental results captured from a fabricated IC prototype will be presented and compared to the ideal response and circuit level simulation results. Finally, a limitation of the proposed design will be identified and a solution to the problem will be described. Later chapters will address the use of these 1st-order filter circuits in the application of a phase reconstruction filter.

3.1 First-Order TM-Filter Realization

A first-order TM-filter can be constructed from two two-input adder circuits as shown in Figure 3-2(a), which realizes the following transfer function:

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \tag{3.1}$$

However, due to the realizability constraint on the output of each adder always lagging behind the input by at least one clock cycle, we must modify the block-diagram of this filter so that each multi-input adder includes this delay. The block diagram shown in Figure 3-2(b) achieves this. This circuit has the following first-order transfer function,

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \tag{3.2}$$

Here the transfer function is slightly different from that shown for the filter of Figure 3-2(a), but fully capable of realizing any bilinear filter function, albeit with an extra two clock delays.

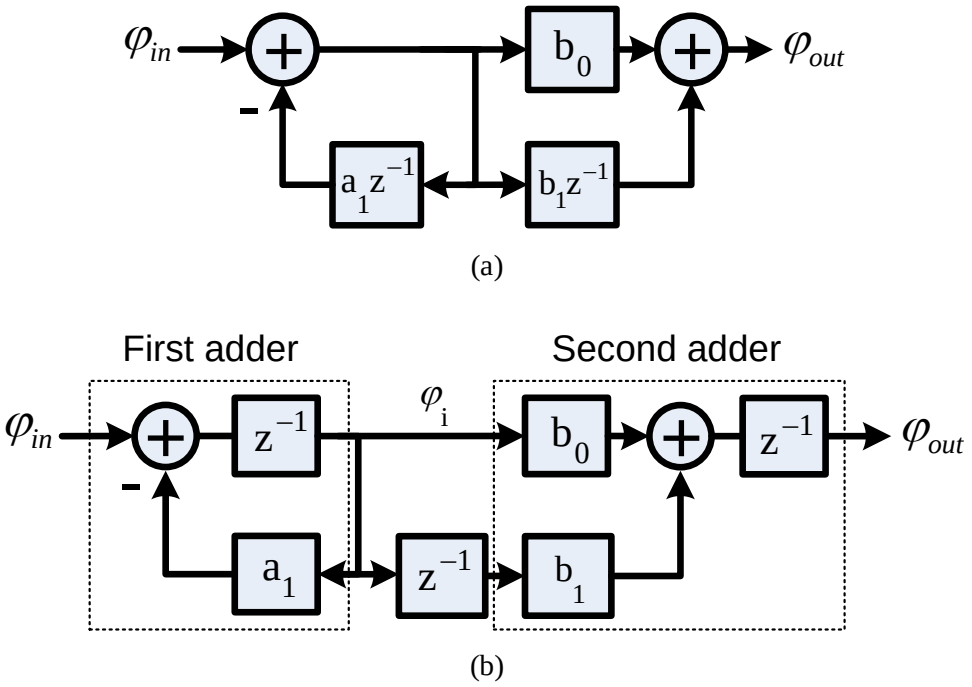


Figure 3-2: First-order TM-filter (a) general block diagram, (b) realizable block diagram.

3.2 MATLAB/Simulink Modeling

The multi-input TM adder was modeled and simulated in MATLAB and Simulink. In our model as shown in Figure 3-3, the time-difference between the edges of the reference clock clk_{ref} and each input signal $\varphi_{in,i}$ is converted into a digital number using a time-to-digital converter consisting of a XOR, AND, and a counter circuit driven by a high-speed clock clk_{fast} with period $T_{fast\text{-}clk}$. Each output of this TDC is scaled by a factor k_i and directed to a multi-input adder. The resultant sum is then de-normalized by the factor $T_{fast\text{-}clk}$ to establish the correct output value dimensionality. As the next clock edge of the reference clock must be delay by the amount determine by the adder, it is first sampled-and-held by a sampled-and-hold block and applied as the control variable of a delay block whose input is the clock reference, clk_{ref}. The resulting output is then the sum of all scaled input time-differences delayed by one clock cycle.

Some quantization noise will be injected during the process of converting the time-difference variable to a digital representation using the simulated TDC. Thus, the frequency of the fast clock has to be high enough in order to reduce the level of quantization noise to a reasonable level. Here a ratio of 1000 is used for 100 MHz reference clock, i.e. f_{fast_clk}=100 GHz. This gives us around 10 bits of resolution which means the output SNR will be limited to less than 62 dB.

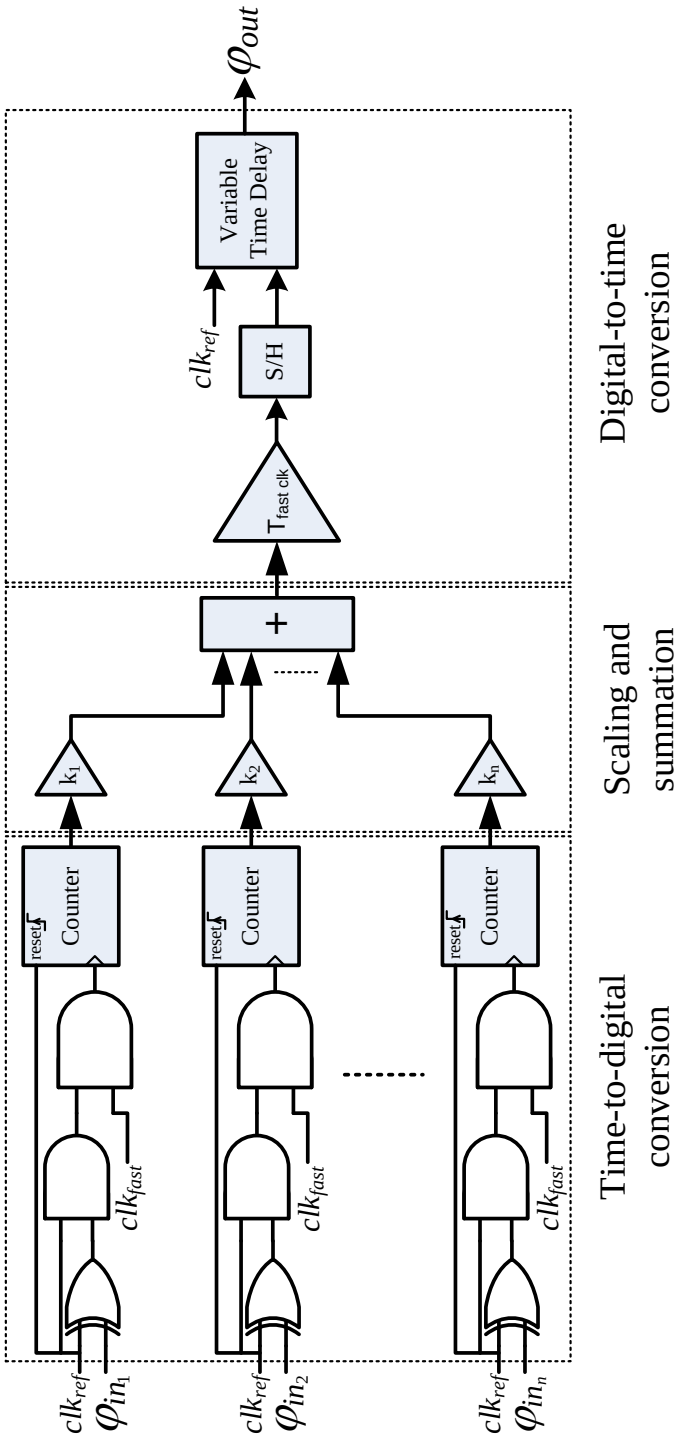


Figure 3-3: Simulink model of a multi-input TM adder

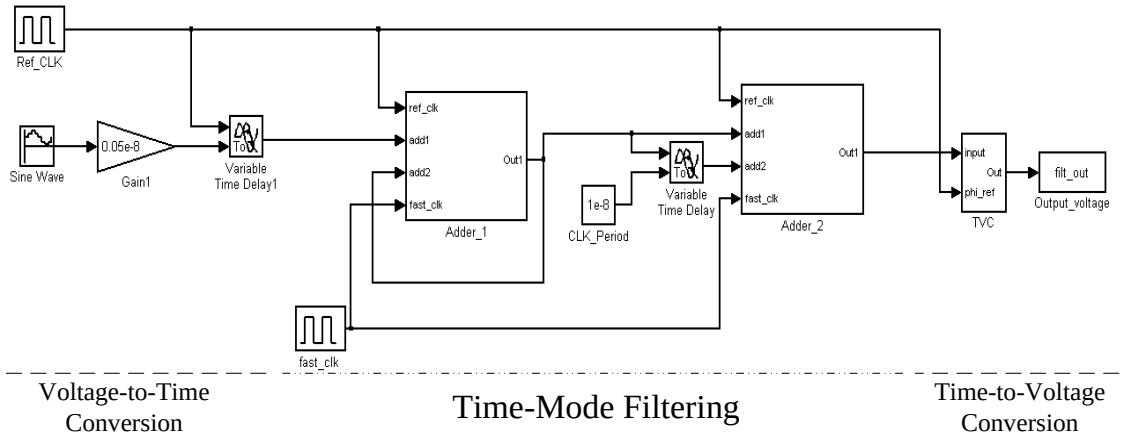


Figure 3-4: Simulink model for a 1st-order time-mode filter.

Using the MATLAB/Simulink model just proposed a 1st-order TM-filter can be modeled in software in order to verify its functionality and performance. This model, as illustrated in Figure 3-4, consists of three main stages: voltage-to-time converter, time-mode filter, and time-to-voltage converter. The first and third stages are merely interfaces between the voltage and time domains and facilitate the testing procedure. Observation and measurement of voltage-mode signals are generally much easier to generate and capture than time-mode ones. The middle stage contains the time-mode filter.

In the first stage an input voltage signal consisting of a sine wave with amplitude of 500 mV and DC voltage of 1 V is converted to a time-mode signal using a reference clock of 100 MHz and a variable delay line driven by a reference clock. The gain block that precedes the variable delay line establishes the conversion coefficient of the input voltage-to-time conversion process. The output of this stage is a clock-like signal whose

rising edge is delayed in proportion to the input voltage level taken at the rising edge of the reference clock.

The 1st-order low-pass time-mode filter making up the second stage of this system is composed of two weighted time-mode adders and a unit delay block. Each TM adder has two inputs, where the scaling factor for each input is determined by the filter transfer function. The unit delay can be realized as a z^{-1} block or as a variable delay line with its reference clock's period set to the desired delay.

Finally, the time-mode output signal of the filter has to be converted back into voltage domain for measurement purposes. Here the same idea used for modeling a multi-input time-mode adder is used (described above at the start of this subsection). The number of periods of a very fast clock (compared to reference clock frequency) running between rising edges of the reference and the output signal is counted. The result is multiplied by the period of the fast clock which returns a measure of the output time difference variable. This number is converted to the corresponding voltage level when scaled by the inverse of voltage-to-time conversion factor used in the first stage.

The filter frequency response is derived by sweeping the frequency of the input signal while measuring the ratio of the output-to-input amplitude. Figure 3-5 depicts the simulated frequency response of several 1st-order low-pass time-mode filters with different transfer functions (e.g., cut-off frequencies).

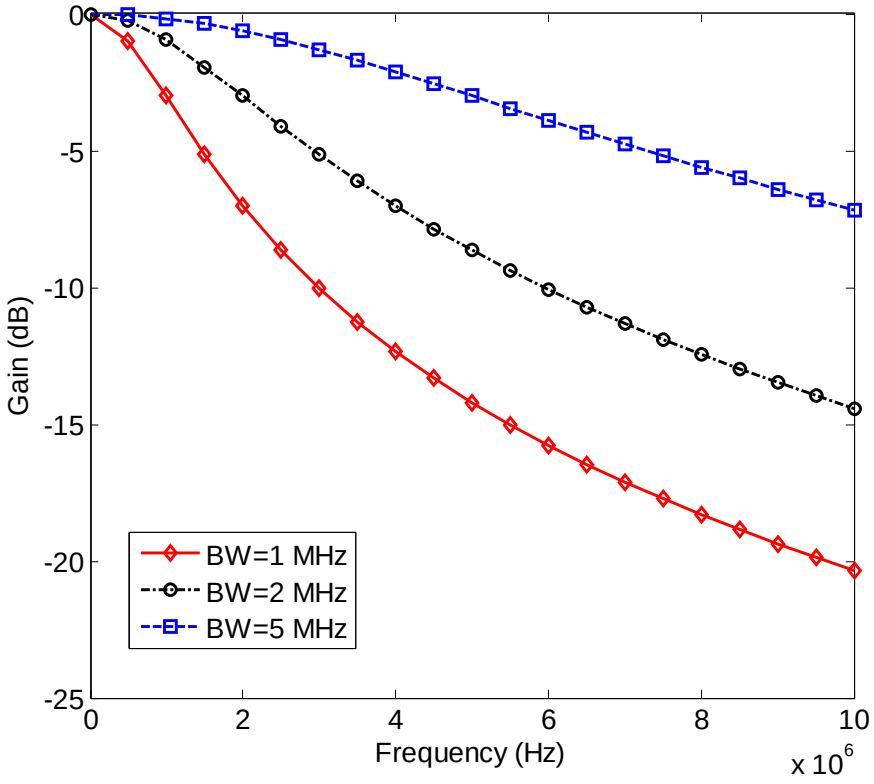


Figure 3-5: Frequency response of 1st-order low-pass filters with different cut-off frequencies simulated in Simulink (MATLAB).

3.3 A First-Order Transistor-Level Design Example

In the 1st-order filter shown in Figure 3-2(b), the front-end added labeled as the first adder is realized as shown in Figure 3-6(a). This adder consists of two stages; one has unity gain and the other has a gain of a_1. Interesting enough, this filter realization can be simplified to that shown in Figure 3-6(b). This simplification comes about because there is no need for gain in the first adder; resulting in one less VCDU and analog biasing block. To maintain equivalence, the original input signal φ_{in} is used as the reference edge

for the second VCDU instead of $\overline{clk}$. We shall make use of this modified adder in the realization of our TM-filter.

The second adder of Figure 3-2(b) was implemented using an ordinary two-input time-mode adder with the appropriate scale factors. The inputs to this second adder are derived from the output of the first adder, together with a delayed version of this same output.

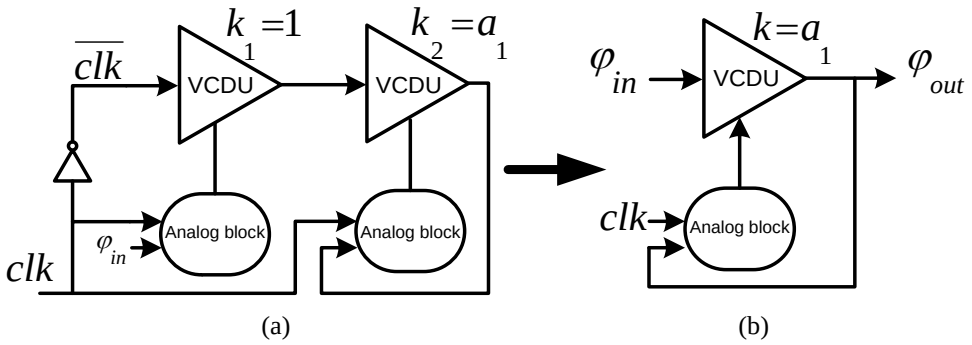


Figure 3-6: Realization of first-stage adder of the filter shown in Figure 3-2: (a) two-VCDU implementation of front-end adder, (b) simplified realization.

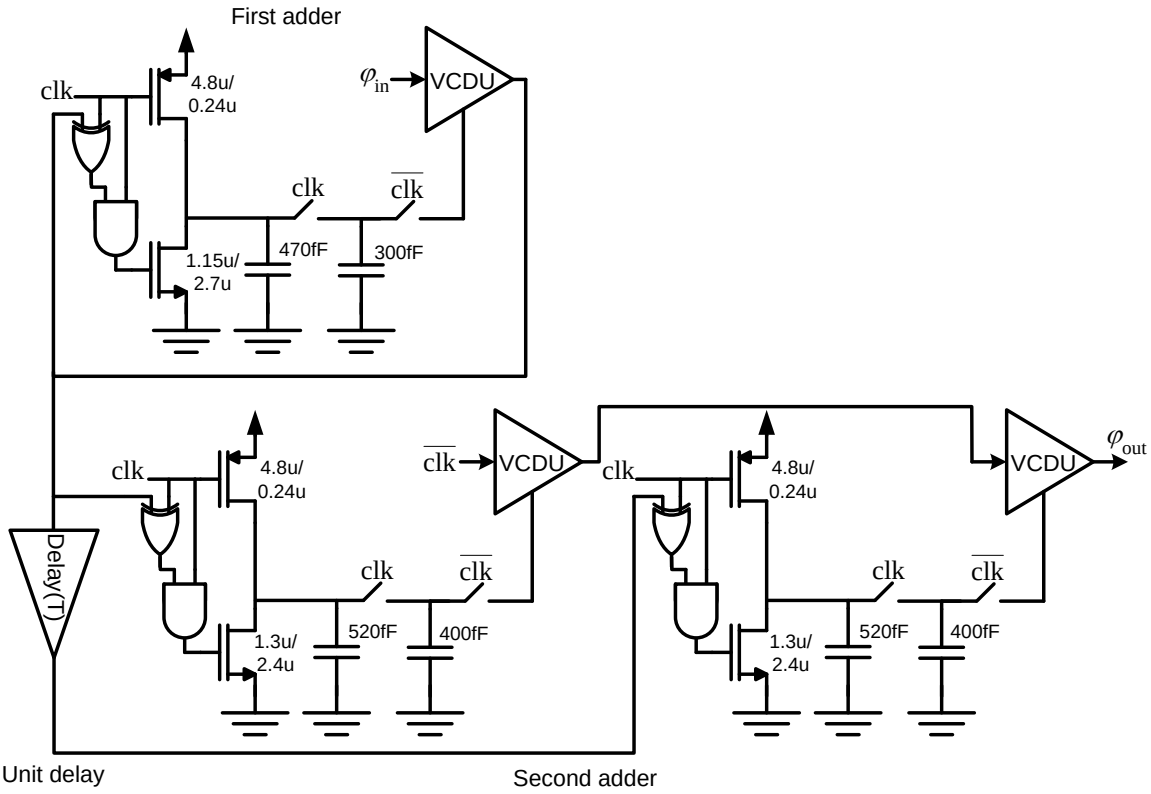
In order to verify the circuit realization of the previous section, a first-order low-pass maximally-flat Butterworth time-mode filter with a frequency response of

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{0.1367 + 0.1367z^{-1}}{1 - 0.7265z^{-1}} \tag{3.3}$$

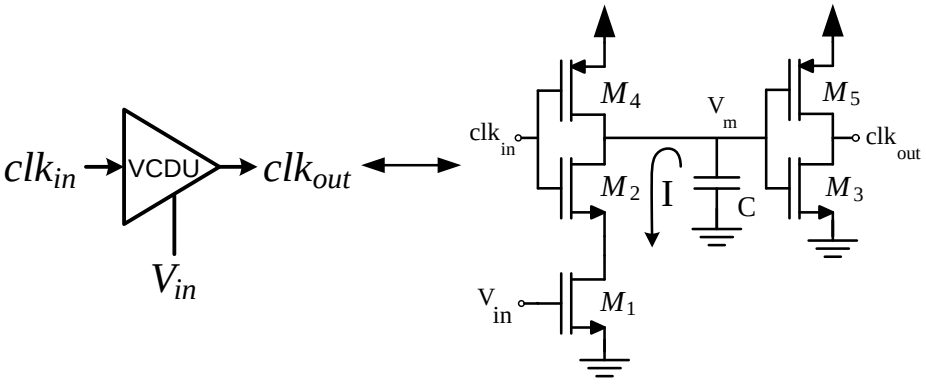
was designed for implementation in a 1.2-V, 0.13 micron, eight-metal CMOS process. The entire schematic of the TM-filter is shown in Figure 3-7. This filter is designed to

operate at 100 MHz clock frequency. As a result, the propagation delay of the unit delay block is set at 10 nsec. A voltage-to-time converter, composed of a VCDU, is used in the front-end of the time-mode filter in order to generate the input time signal φ_{in} from a voltage signal. However, the output of the filter φ_{out} is captured as a time-mode signal and post processed in MATLAB.

In this design, one should note that the capacitors are not ratio-ed to any particular component, and its size is set only by KT/C noise considerations. Likewise, the transistors are used for the most part as switches; hence their precise signal gain is not important for the TM operation, although enough time must be allocated for charging and discharging. As a result, the design is well suited to advance CMOS processes where signal gain reduces with feature size, but transistor speed increases.



(a)



(b)

Figure 3-7: Complete schematic of the first-order TM-filter: (a) transistor level implementation VCDU in symbolic form, (b) VCDU equivalent circuit representation.

3.4 Circuit and Layout Considerations

In this section, layout considerations of each block together with their circuit details such as transistors aspect ratios and capacitor values are summarized.

3.4.1 Front-End Voltage-to-Time Converter

The front-end VTC is implemented using a VCDU, like the one shown in Figure 3-7(b). The input voltage (V_{in}) and reference clock (clk_{in}) are delivered to the IC from off-chip signal sources. The output signal (clk_{out}) from the VCDU is buffered through two inverters to sharpen the rising edge before it is delivered to first-adder of the TM filter. Table 3-1 summarizes the transistor sizes and capacitor value used in this circuit. Figure 3-8 shows the layout view of this block, together with the rest of the circuits.

Table 3-1: Component specifications of the front-end VTC

Component	Aspect ratio/Value
M_1	1 um/480 nm
M_2	1 um/360 nm
M_3	0.8 um/240 nm
M_4	1.8 um/240 nm
M_5	1.2 um/240 nm
C	200 fF

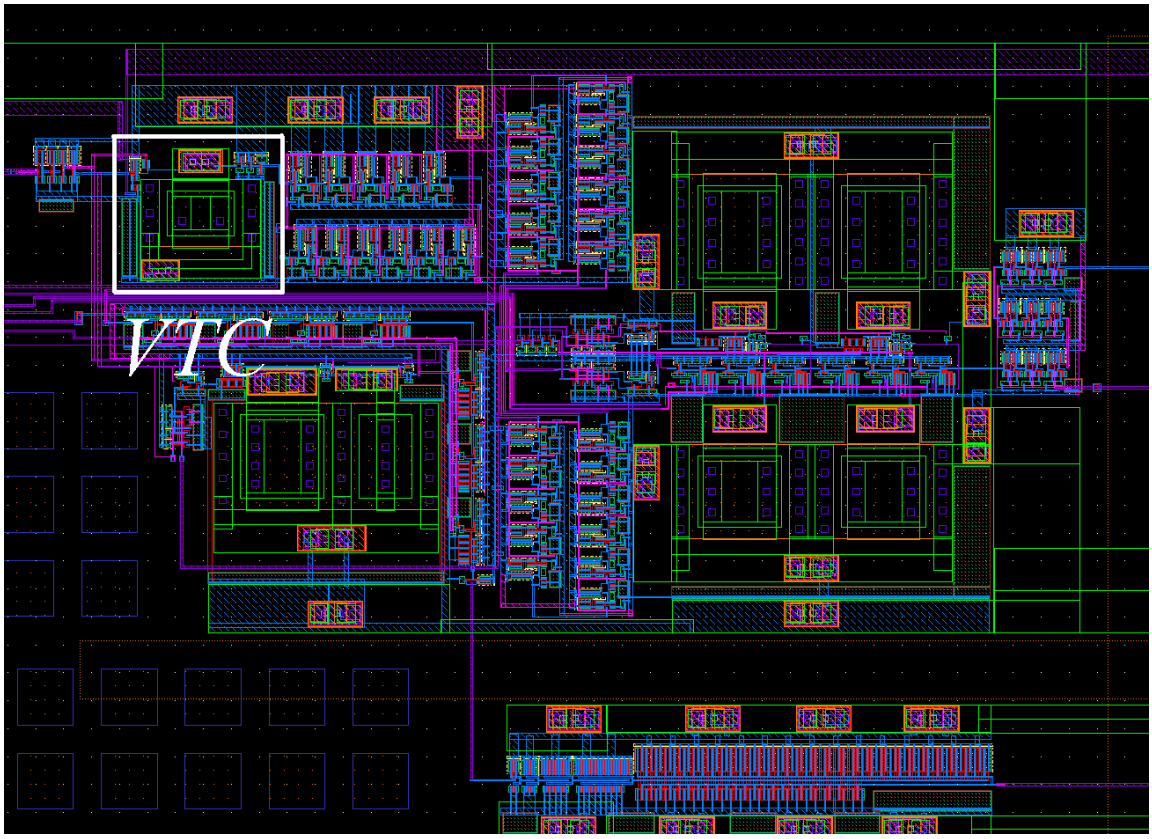


Figure 3-8: Layout view of the front-end VTC

3.4.2 First Adder

The front-end adder of the time-mode filter is realized using a VCDU line and an analog block as explained previously and shown in the top left-hand side of Figure 3-7(a). The layout view of this block is shown in Figure 3-9. While a single VCDU is shown in Figure 3-7(a), it is actually made from a cascade of seven individual VCDU in order to achieve a large conversion gain of approximately 3.5 ns/V. Individual VCDUs

have a nominal conversion gain of about 0.5 ns/V. Each VCDU is built using the same circuit as in the previous subsection except here the capacitor C is replaced by a transistor with its source and drain terminals shorted together. Table 3-2 contains the transistor sizing associated with this circuit and Figure 3-10 shows the schematic of each VCDU. Sizing for the other components making up the analog block are shown directly on the schematic of Figure 3-7(a).

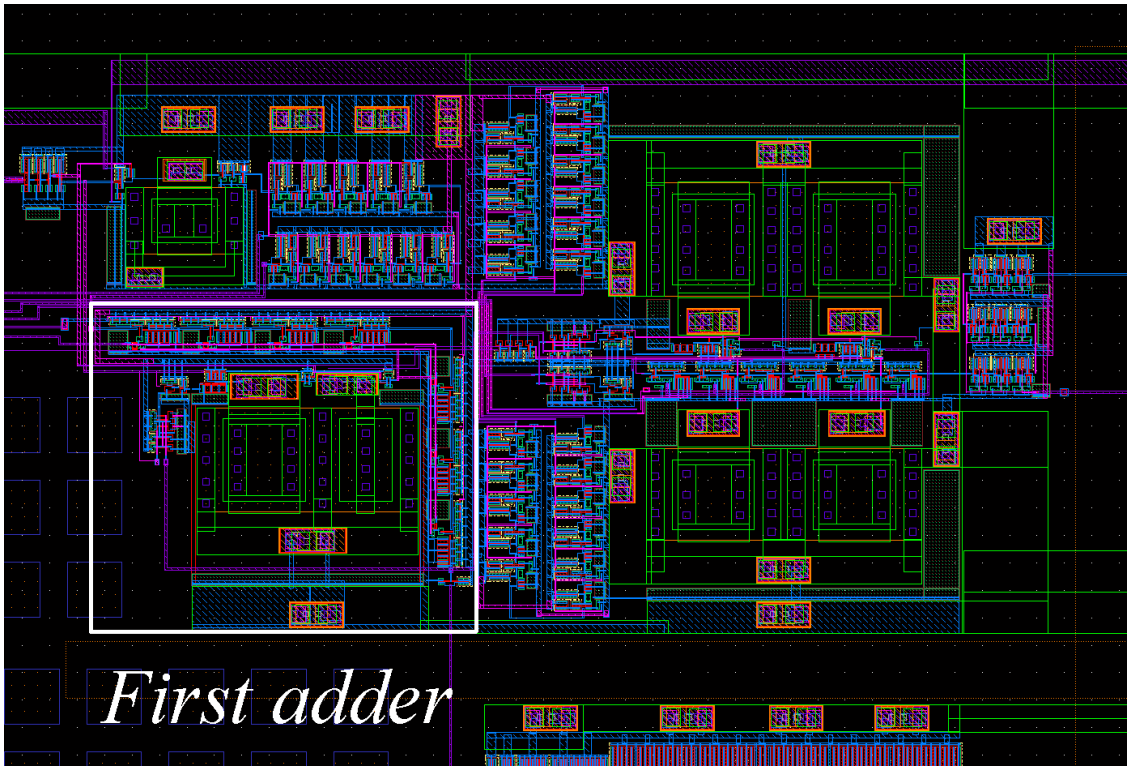


Figure 3-9: Layout view of the first adder

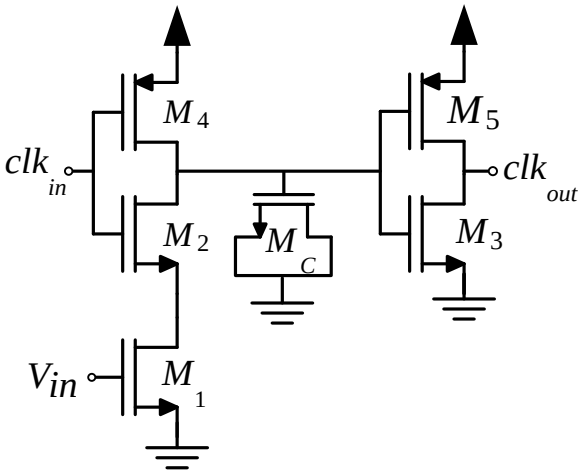


Figure 3-10: Schematic of each VCDU used in the first adder.

Table 3-2: Component specifications of the first adder

Component	Aspect ratio/Value
M_1	500 nm/500 nm
M_2	0.8 um/120 nm
M_3	2 um/240 nm
M_4	1.5 um/240 nm
M_5	3 um/240 nm
M_C	8 um/600 nm

3.4.3 Unit Delay

The unit delay shown in Figure 3-7(a) consists of a cascade of 20 VCDUs whose control voltages are connected to an off-chip source for the purpose of fine-tuning its propagation delay. It is important that this delay cell realize the inverse of the sampling rate F_s of the desired filter transfer function. In this particular case, the clock period was

set to 10 ns corresponding to a sampling rate of 100 MHz. The VCDUs used are identical to that shown in Figure 3-10. The layout view of this circuit is shown in Figure 3-11. Table 3-3 summarizes the component sizes used in this circuit.

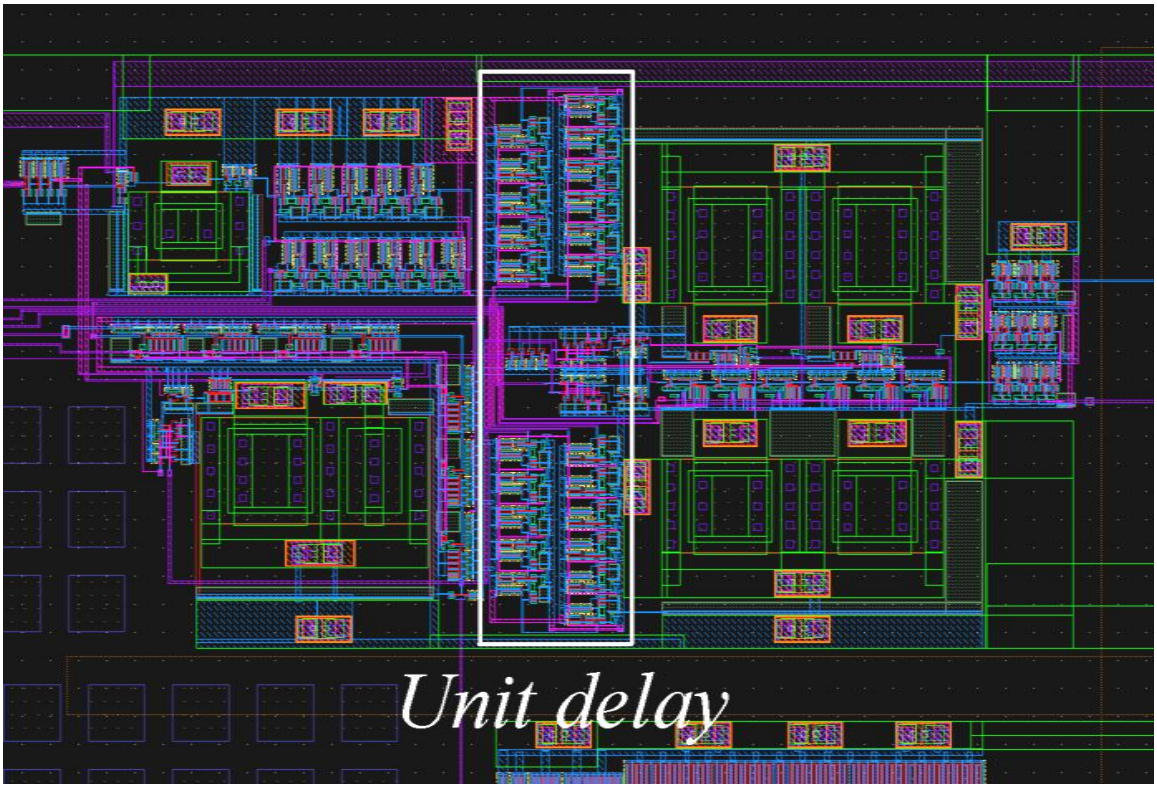


Figure 3-11: Layout view of the unit delay

Table 3-3: Component specifications of the unit delay

Component	Aspect ratio/Value
M_1	600 nm/600 nm
M_2	1 um/240 nm
M_3	2 um/240 nm
M_4	1.5 um/240 nm
M_5	3.6 um/120 nm
M_C	800 nm/ 240 nm

3.4.4 Second Adder

The second adder of the time-mode filter shown in Figure 3-7(a) is comprised of two VCDU lines having individual analog SC memory cells (referred to the analog block). Since b_0 and b_1 coefficients of the filter transfer function given by Equation (3.3) are equal, identical circuits are used to realize these scaling factors. Table 3-4 lists the transistor aspect ratios and Figure 3-12 depicts the layout view of this block.

Table 3-4: Component specifications of the unit delay

Component	Aspect ratio/Value
M_1	500 nm/500 nm
M_2	1.5 um/240 nm
M_3	2 um/240 nm
M_4	1 um/240 nm
M_5	3 um/240 nm
M_C	4 um/240 nm

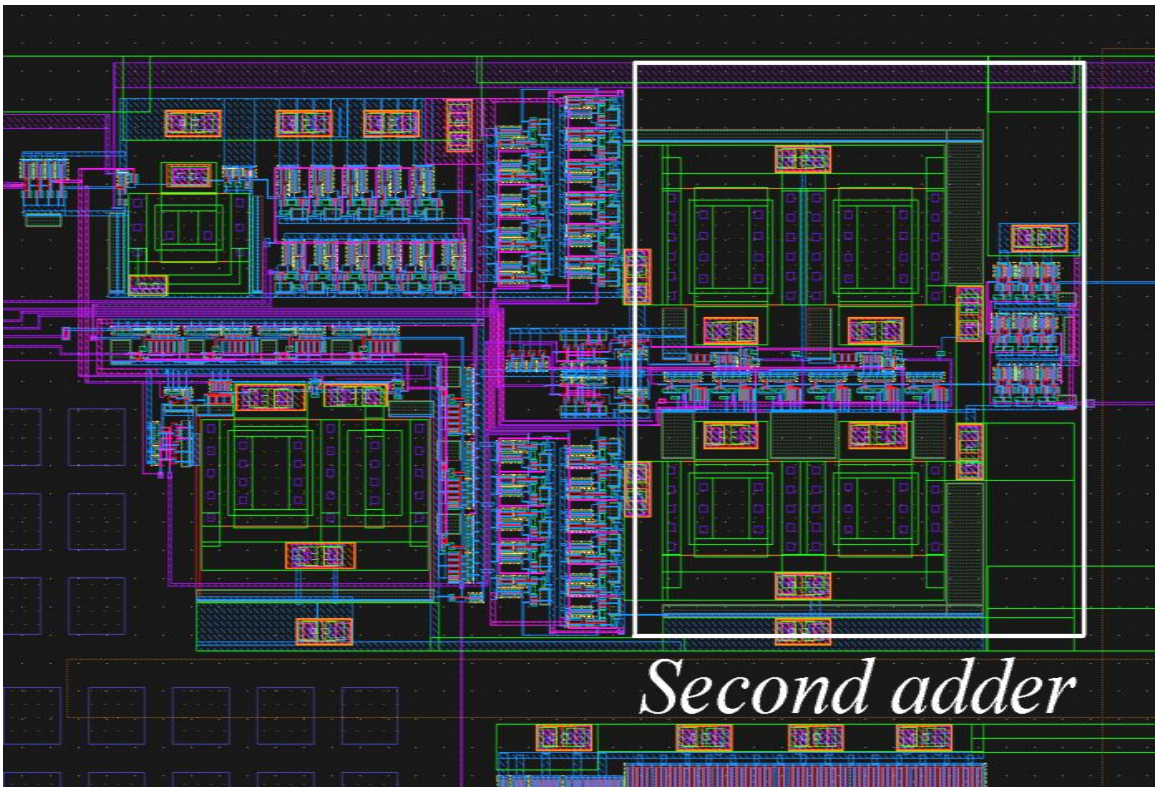


Figure 3-12: Layout view of the second adder

3.4.5 I/O Pads

In our design wire bond pads where used to connect the chip to the package. These pads are rectangular shape with dimensions of 108 um x 108 um. Figure 3-13 shows the layout view of a single pad. The pad is connected to the outermost metal layer (MA in a 0.13 micron IBM CMOS technology). The center-to-center space between two pads was set at 180 um, which satisfies the design rules and provide enough room for

wire bonding after fabrication. Each pad is immediately connected to an ESD protection circuit, which will be explained shortly.

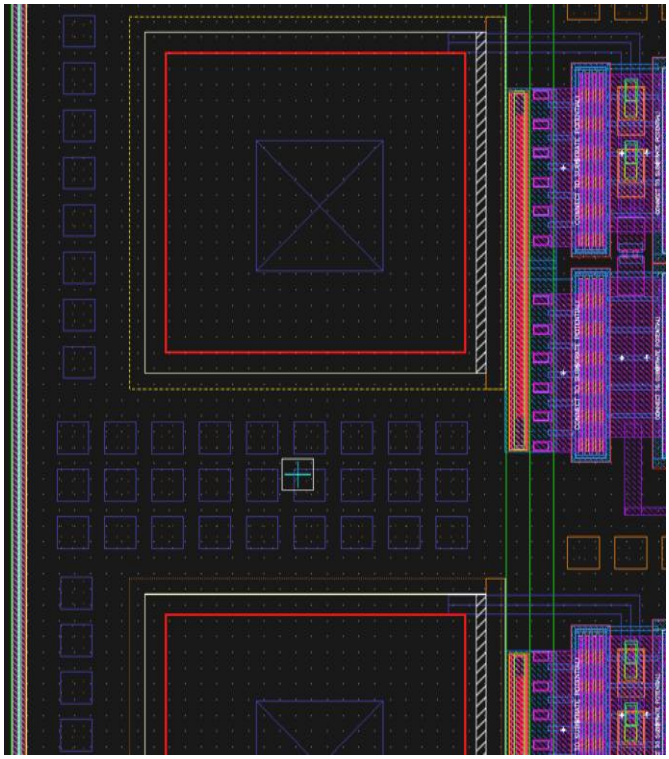


Figure 3-13: Layout view of wire bond pads.

3.4.6 ESD Protection Circuits

ESD circuits are required to protect the chip in the case of high current events occurring at various stages of processing and handling. The voltage levels that are developed during an ESD event can go way beyond the breakdown voltage of any device in submicron technology. The goal of an ESD protection circuit is to prevent the accumulation of charge on high-impedance nodes of a circuit by routing such charge build-up through alternative signal paths [14].

In this thesis two types of ESD circuits are used to protect the chip. One structure protects the pads connected to the input and output signal paths, while the other protects the pads connected to the DC power supplies. The first circuit is shown in Figure 3-14(a) which consists of two back-to-back diodes connected between the DC supplies with the input/output signal pads connected to the middle node. In normal operation these diodes are reverse biased and hence no current flows from V_{DD} to *GND* and vice versa. Also there is no current flowing from the I/O pads to the supplies. However, in the case of a high positive voltage, the top diode is forward biased directing the ESD current to V_{DD} protecting the internal circuitry. Likewise, when a high negative voltage hits the I/O pad the bottom diode is turned ON providing a very low resistance path to *GND*. It should be noted that the components used in ESD protection circuits should have extremely low series resistance in the on-state, so that high currents do not cause high voltage peaks on internal nodes.

The other ESD circuit protection used for the power supplies pads is shown in Figure 3-14(b). This circuit consists of a reversed-biased diode. This diode is responsible for redirecting the ESD current from *GND* to V_{DD} and preventing the unwanted current to flow into the rest of the circuit through the *GND* connections. A power clamp could be employed to protect the circuit for the reverse scenario (V_{DD} to *GND* discharge). However, the available cells in the kit did not match across the circuit and layout levels, so they were not used.

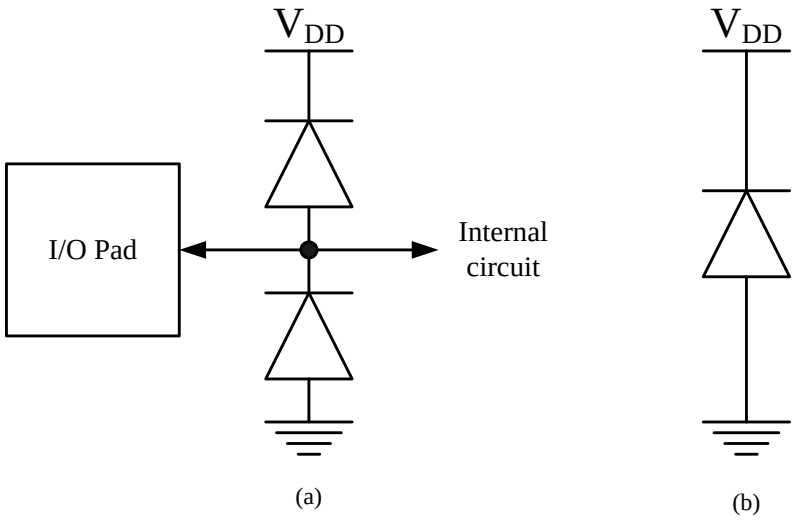


Figure 3-14: ESD circuit used for (a) I/O pads, (b) power supplies pads.

3.4.7 IC Overview

An overview of input-output pins of the first-order TM filter circuit is shown in Figure 3-15. An input voltage signal is applied to the input pin V_{in} and converted to a time-mode signal via a VTC circuit element. As bench-top AC signaling equipment is generally voltage-based, the inclusion of a VTC provides easier interfacing with such equipment. The time-mode signal output from the VTC is then directed to the first-order TM filter input. The filter is clocked with a 100 MHz off-chip clock signal. Six external control voltages are used to set the appropriate unit delays of the first and second adders. The output of the time-mode filter is first buffered through a chain of inverters before connecting to the output pad. In addition to the main output, some other intermediate signals inside the filter, such as the VTC output (acting as the input to the TM filter) and

first adder output are buffered and connected to the output pads. These signals help us to better monitor the functionality and performance of the filter.

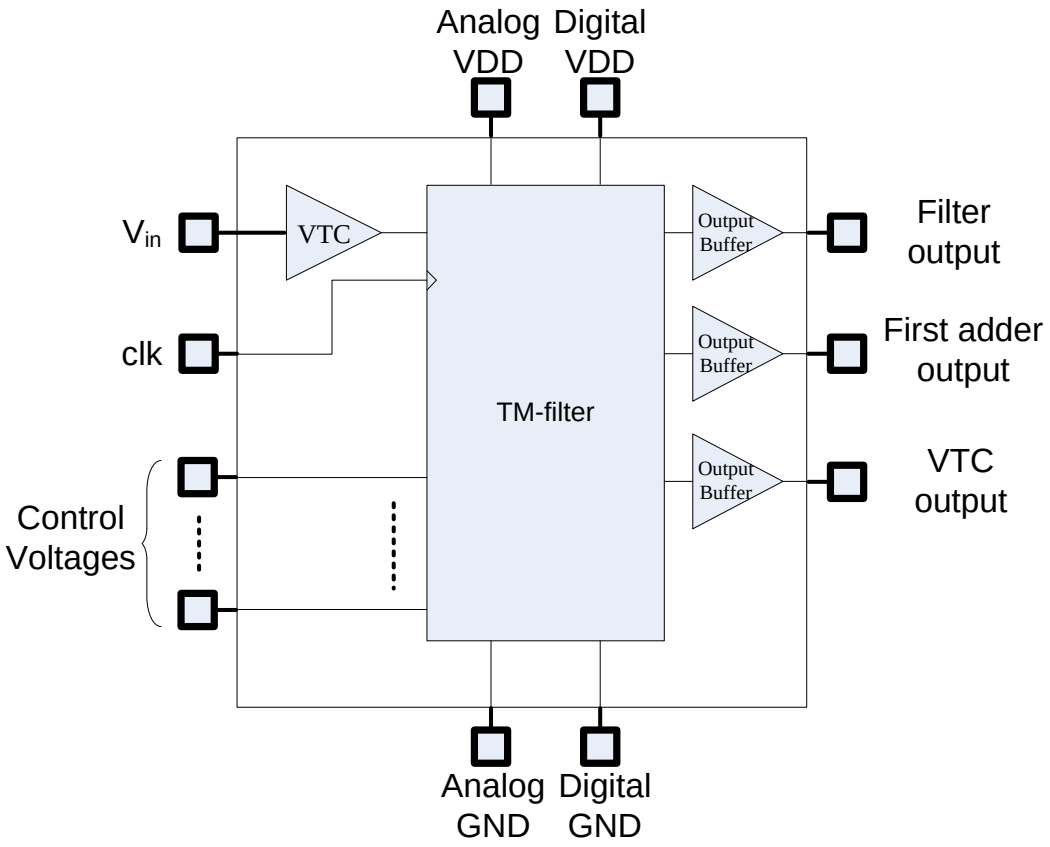


Figure 3-15: An overview of the input-output pins of the first-order TM filter circuit.

3.4.8 Transistor-Level Simulation Results

A set of extracted transistor level simulations was performed on the 1st-order TM filter circuit of Figure 3-7 using Spectre. While the operation of individual building

blocks was investigated, the results are not very interesting to show here; instead, the input-output frequency response behavior of the filter circuit was collected and shown in Figure 3-16. At each frequency, the ratio of output peak-to-peak amplitude to its corresponding input amplitude was captured and reported in terms of the filter gain as a function of frequency. The results were also compared to the magnitude response of the desired transfer function seen listed in Equation (3.3). As is clearly evident, no difference is visible over the range of frequencies selected (i.e., 100 kHz to 20 MHz).

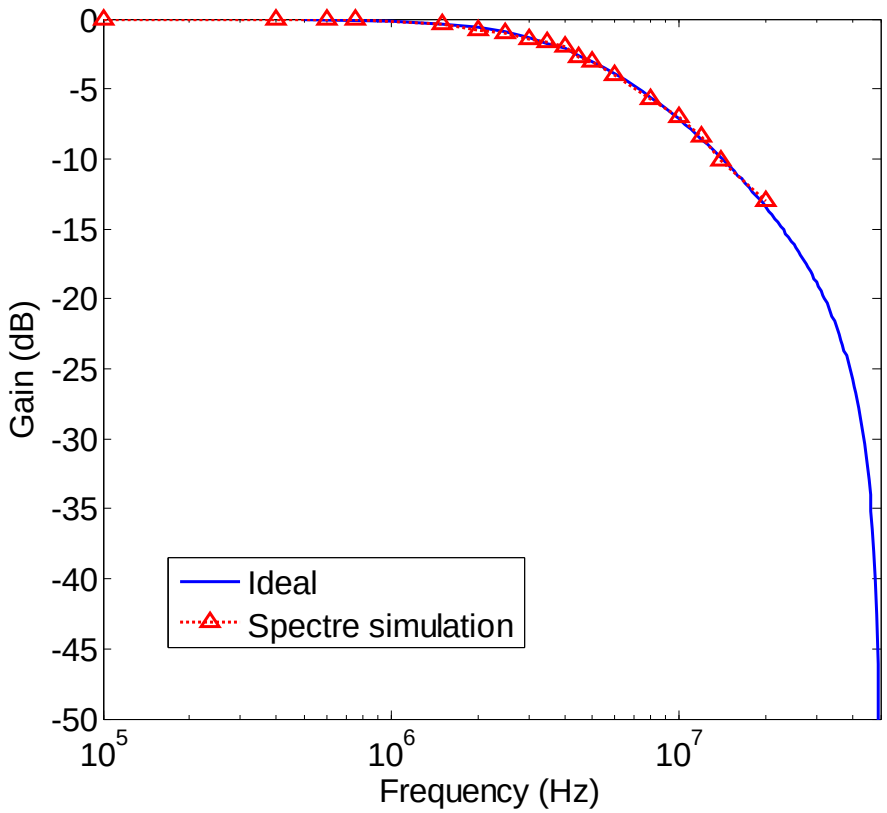


Figure 3-16: Ideal versus transistor level simulated frequency response of the 1st-order TM-filter circuit of Fig. 3-7.

3.5 Integrated Circuit Experimental Results

An IC containing the circuit of Figure 3-7 was fabricated in an IBM 0.13 micron CMOS process made available through the services of Canadian Microsystems Corporation (CMC). A micrograph of the IC is shown in Figure 3-17. It is made up of a VTC, TM-filter, input and output buffers. The whole circuit occupies an area of 170 µm x 100 µm excluding the pad frame. In comparison to other filter approaches, e.g., SC capacitor, this level of area utilization would be considered quite small. Ten packaged chips in a 44-pin Ceramic Quad Flat Packages (CQFP) were returned from CMC.

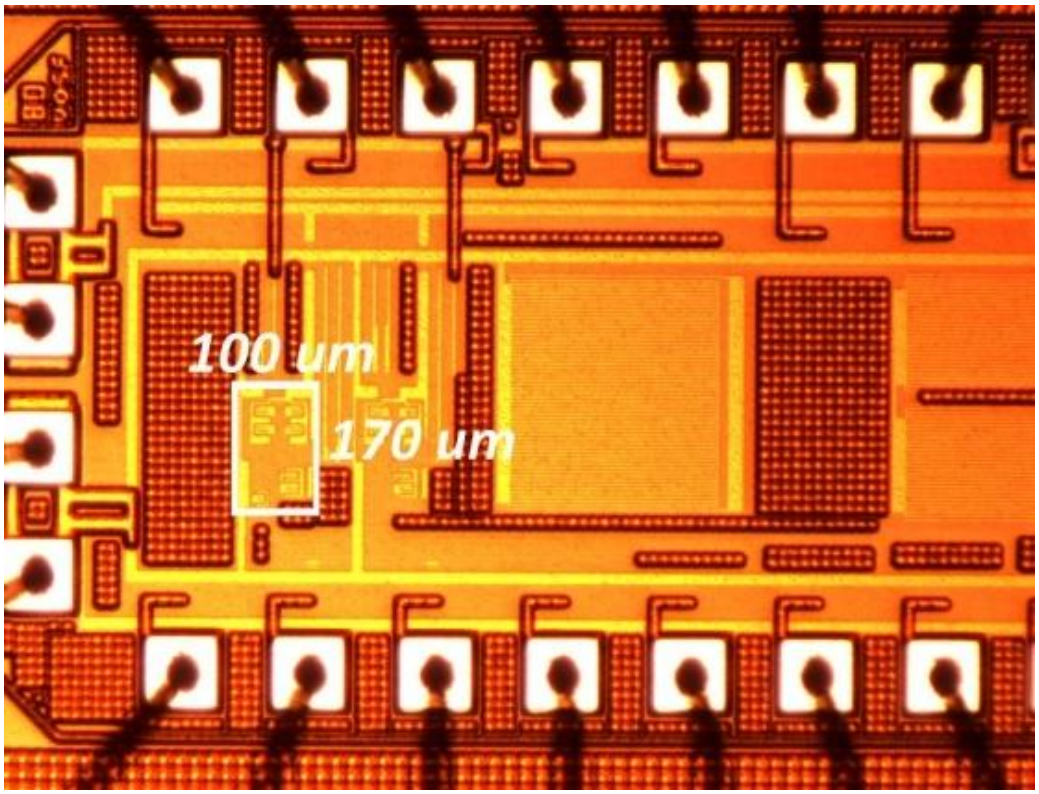


Figure 3-17: The chip micrograph

Figure 3-18 depicts the test set and external equipment used for testing the IC chip. The DC power supply and the DC control voltages for tuning the unit delays was derived from separate Agilent 33250 DC power supplies. The input AC voltage signal was generated by an Agilent E3648 arbitrary waveform generator. A Hewlett Packard 81130A pulse/pattern was used to generate the input clock signal. The time-mode output signal from the filter was captured and saved using an Agilent 54830D digital sampling oscilloscope. The saved data was then transferred to MATLAB/Simulink for further signal processing.

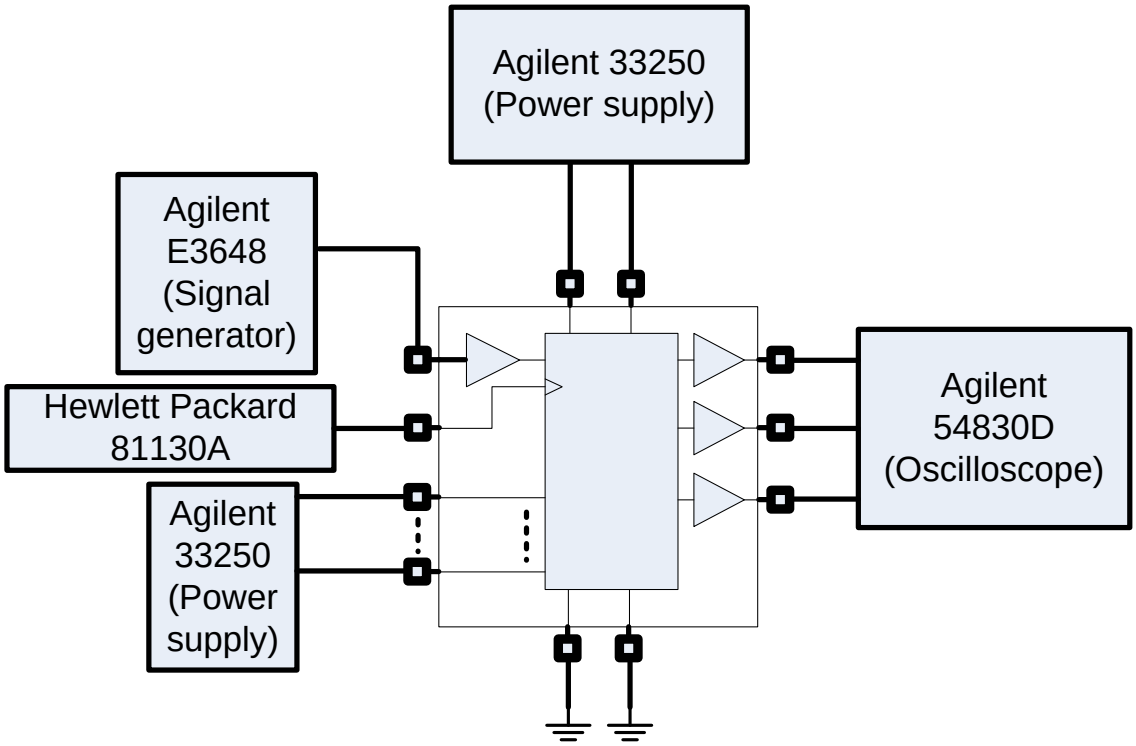


Figure 3-18: The chip and test Setup details (a) signal diagram inside each chip, (b) equipments used to test the chip.

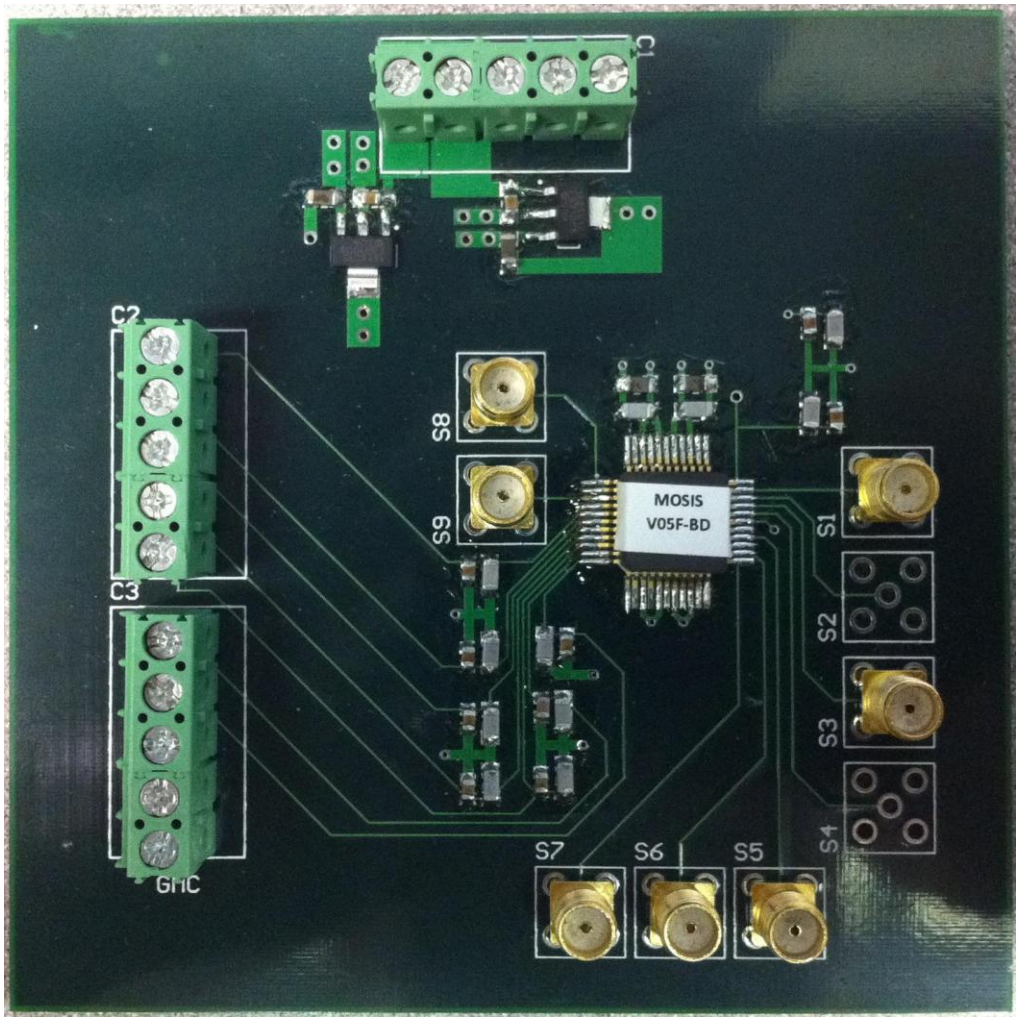


Figure 3-19: Custom PCB built for testing the chip.

A custom 4-layer FR4 PCB shown in Figure 3-19 was designed and manufactured to interface the test equipment to the IC. In this PCB all the DC voltages are connected to the board using thru-holed terminal wire-to-board connectors (C1, C2 and C3 shown in the figure). The input voltage and clock signals are connected to the PCB using SMA connectors. Also, other SMA connectors are used to connect the three output signals to

the oscilloscope. DC power regulators are used to set the DC voltage levels to the chip. Moreover, decoupling capacitors of 0.1 µF and 10 µF are employed at the output of regulators. These were placed very close to the V_{DD} pads of the IC to minimize stray inductive effects. Similar valued capacitors were also used to suppress any high frequency noise on the voltage control lines.

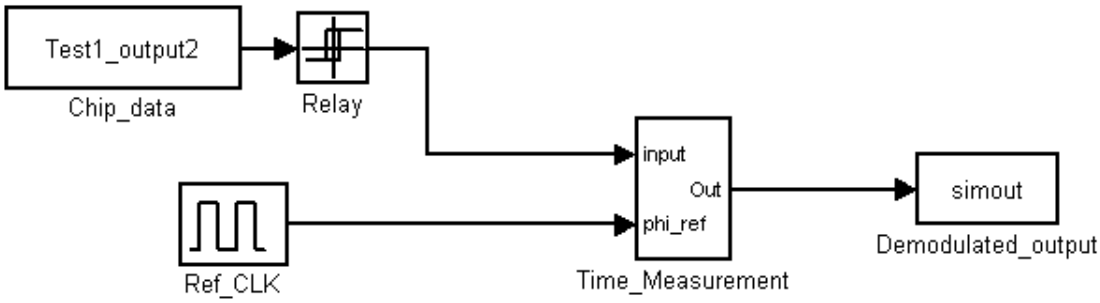


Figure 3-20: Output demodulator schematic implemented in Simulink to process the measured data.

Once the test data is collected from the TM filter, additional signal processing is required to phase demodulate the filter output so that the gain relative to the input signal level can be determined. While this operation was conducted previously on the transistor level Spectre simulation results within the Cadence framework, it should be noted that Cadence provides additional tools that perform this demodulation function directly. Rather than redirected the test data back into Cadence, the data was post-processed using MATLAB/Simulink using the phase demodulation block shown in Figure 3-20. This block consists of a relay with a switching point set to the half-full scale voltage, i.e., 0.6

V. Its purpose is to sharpen the output rising edge for easier comparison to the reference signal edge location. The demodulation operation is performed using the time-to-digital conversion block implemented in exactly the same manner as that described for one branch of the multi-input time-mode adder of Figure 3-3. To convert the digital representation of the time difference, the digital number derived directly from the TDC must be scaled by the period of the fast reference clock, clk_{fast}.

A series of single tone tests with peak-to-peak value of 300 mV riding on a DC voltage of 800 mV was applied to the input of the front-end VTC stage. The corresponding time-mode signals generated by the front-end VTC were captured by the Agilent 54830D oscilloscope and stored for future use in computing the frequency response of the filter. Similarly, the output TM signals from the filter were captured in the same way. After post-processing the test data, the frequency response of the TM filter was computed and plotted in Figure 3-21. Also shown in the plot, is the ideal frequency response together with that predicted by a MATLAB/Simulink simulation. As is evident, excellent correlation between the expected and measured results up to about 10 MHz exists (20% of the Nyquist interval). For higher frequencies, some magnitude response deviations as large a single dB is evident. As the amplitude of the output signal at these higher frequencies is quite small, the effect of clock-related noise is more pronounced. Hence, larger magnitude error is present.

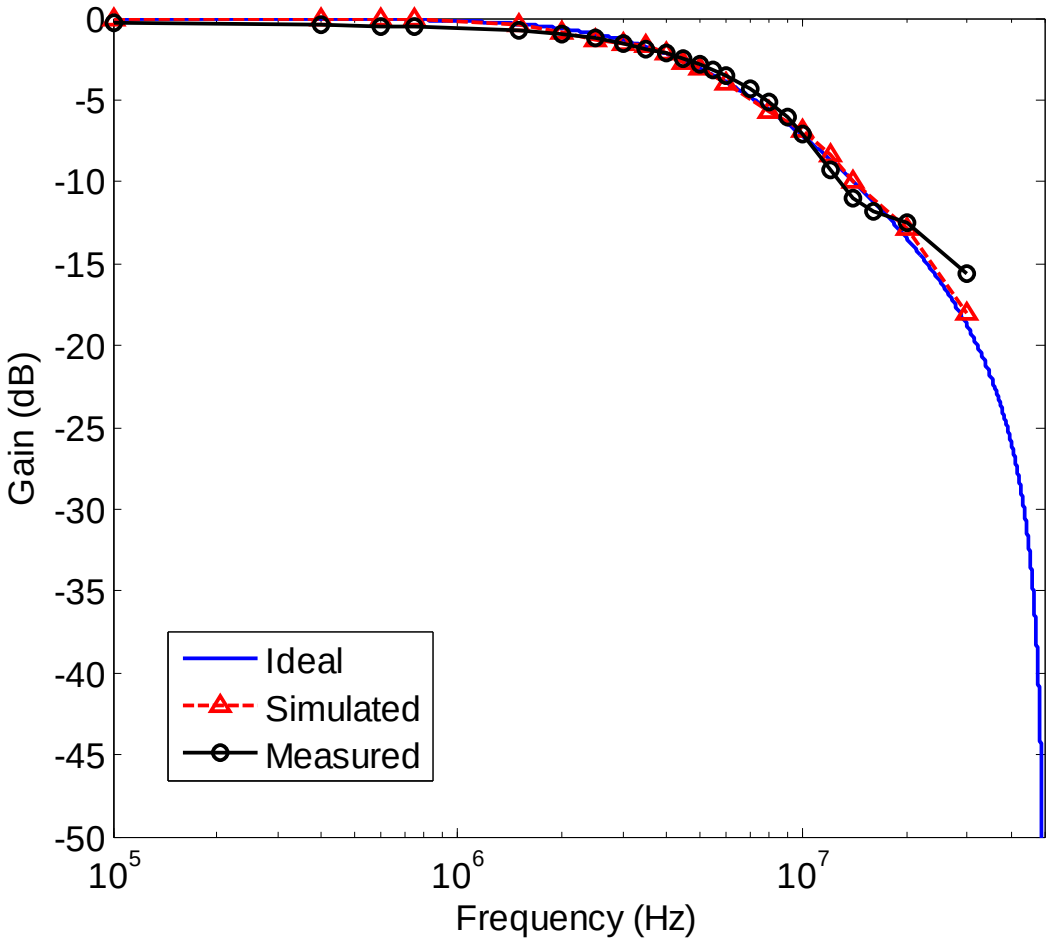


Figure 3-21: Ideal, Spectre simulated, and measured frequency response of the 1st-order TM-filter.

Further tests on the static power dissipation and maximum input signal level were performed and the results are summarized in Table 3-5. One surprising result was that when the input amplitude exceeds some level but within the expected linear range of the circuit, excessive distortion appears at the output. Specifically, it was discovered that the filter failed to operate when the sine wave input amplitude exceeded 600 ps peak-to-peak.

Further investigation revealed that the output of the first-adder saturated, i.e., output went flat, when the input exceeded 600 ps. This result was also confirmed after the fact using transistor level simulation. A solution to this problem is provided in the next chapter.

Table 3-5: Summary of TM-filter measured performance

Technology	0.13 µm
Supply Voltage	1.2 V
Core Area	170 µm x 100 µm
Power Dissipation	670 µW
Sampling Frequency	100 MHz
Max. Input Amplitude (p-p)	600 ps
3-dB Cut-Off Frequency	5 MHz

3.6 Summary

In this chapter the concept of time-mode filtering was introduced and investigated using a first-order filter structure. A CMOS realization was designed, laid out and fabricated in a 0.13 micron IBM CMOS process. The measured results agree with both the theoretical and transistor level simulations conducted with Spectre. These results prove for the first time that the concept of time-mode filtering is feasible in a CMOS monolithic process. While the previous work of [13] was the first to show the idea of time-mode filtering using IIR structures, the work was exclusively based on prototypes constructed using discrete components.

Chapter 4

High-Order Time-Mode Filters

In this chapter we shall investigate the saturation problem associated with the first-order TM filter discovered in Chapter 3. As we learned in that chapter, when the input to the TM filter exceeded some level, the output would essentially saturate or clip at a zero-voltage level. In this chapter we shall develop theory that accounts for this behavior and provide several topological solutions that avoids this saturation problem altogether. The strengths and weakness of these new filter topologies will be identified and used in the creation of high-order time-mode filter realizations suitable for advanced CMOS processes.

4.1 Saturation Effect Associated With the Original TM-Filter

A limitation of the TM-filter structure of Figure 3-2 became evident when a large step change in phase was applied to the input of the TM-filter. It was observed that the front-end adder of the TM-filter saturated whereby the output sat at a zero-voltage level even when the input was changing. On further investigation, using the first-order filter realization of Section 3.3, a Spectre transistor-level simulation revealed that the proposed

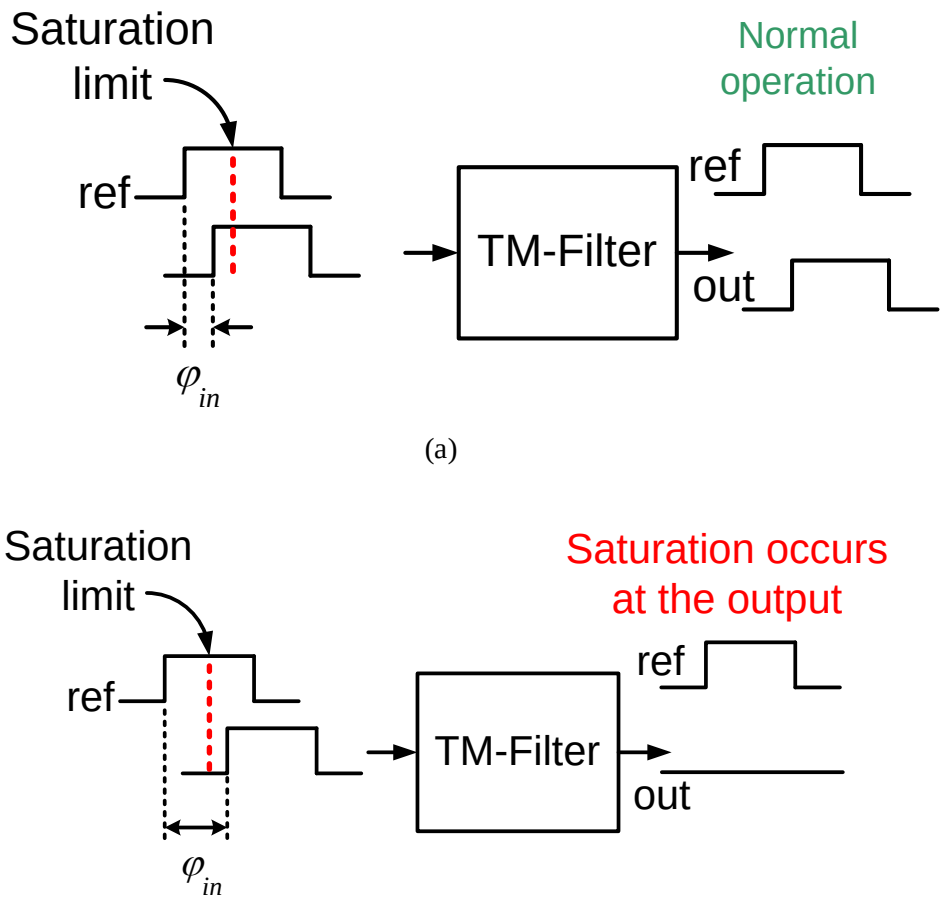


Figure 4-1: TM-filter suffering from saturation problem (a) normal mode, (b) saturation mode.

TM-filter would saturate with input time-steps were greater than 1.25 ns. The theoretical range of operation should be equal to at least one-half the clock period of 5 ns. This effect is illustrated in Figure 4-1 using two circuit conditions. In Figure 4-1(a), a small input time-step is applied to the TM filter within its linear region. Here we see the output signal has a valid signal representation with respect to the reference signal. In the case of the situation depicted in Figure 4-1(b), here it is shown that the input time-step goes

beyond the saturation limit and forces the output signal to disappear, i.e., no output edge appears.

On further investigation, as the cut-off frequency f_c of the filter was reduced, the point at which the input level would cause output saturation to occur appeared at lower input levels. This result clearly indicates that the proposed TM-filter of Section 3.3 would be limited to wideband filtering applications. This severely restricts the use of this technology and a new topology(s) is required to extend time-mode filtering to a wide range of applications, such as the reconstruction problem outlined in the introduction to this thesis. The following will investigate the source of this saturation problem and a method in which to eliminate it.

Saturation in time-mode signals is defined as the condition when one node goes beyond its available time range, i.e. $T/2$ where T is the clock period of the reference signal. Returning to the block diagram of the first-order TM filter of Figure 3-2(b), under conditions of narrowband, i.e., b_0 and $b_1 \ll 1$, and $a_1 \approx -1$, additional analysis reveals that the output of the filter, φ_{out}, is clipped at the same time when the signal from the first adder is saturated. As this first adder is incorporated into an integrator section, it is the act of integrating the input signal that causes the saturation problem. This leads us to conclude that the filter saturation problem lies within the front-end stage of this filter and not the second one.

To calculate the maximum input signal that can be applied to the TM filter, the

transfer function from input to the internal integrating node φ_i of Figure 3-2 was derived, and was found to be

$$\frac{\Phi_i(z)}{\Phi_{in}(z)} = \frac{z^{-1}}{1 + a_1 z^{-1}} = \frac{1}{z + a_1} \tag{4.1}$$

Replacing $z = e^{j\omega T}$ in Equation (4.1) and taking the magnitude of each side of the above equation results in

$$\left|\frac{\Phi_i}{\Phi_{in}}\right| = \frac{1}{|e^{j\omega T} + a_1|} \tag{4.2}$$

Substituting $e^{j\omega T} = cos\,\omega T + j\ sin\,\omega T$, Equation (4.2) reduces to

$$\left|\frac{\Phi_i}{\Phi_{in}}\right| = \frac{1}{\sqrt{(a_1 + cos\,\omega T)^2 + sin\,\omega T^2}} \tag{4.3}$$

On further trigonometric substitutions, Equation (4.3) can be re-written in terms of the magnitude of internal node signal as follows

$$|\Phi_i| = \frac{1}{\sqrt{a_1^2 + 2a_1\,cos\,\omega T + 1}} |\Phi_{in}| \tag{4.4}$$

Recognizing that the internal node saturates when its magnitude reaches $T/2$, this imposes the constraint on the internal node to be less than *T*/2, i.e.,

$$|\Phi_i| \leq \frac{T}{2} \tag{4.5}$$

This in turn imposes the following constraint on the input,

$$|\Phi_{in}| \leq \frac{T}{2}\sqrt{a_1^2 + 2a_1 \cos \omega T + 1} \tag{4.6}$$

To simplify our analysis, consider the saturation effects for a DC input. Equation (4.6) reduces to

$$\Phi_{in,max} = \frac{T(a_1 + 1)}{2} \tag{4.7}$$

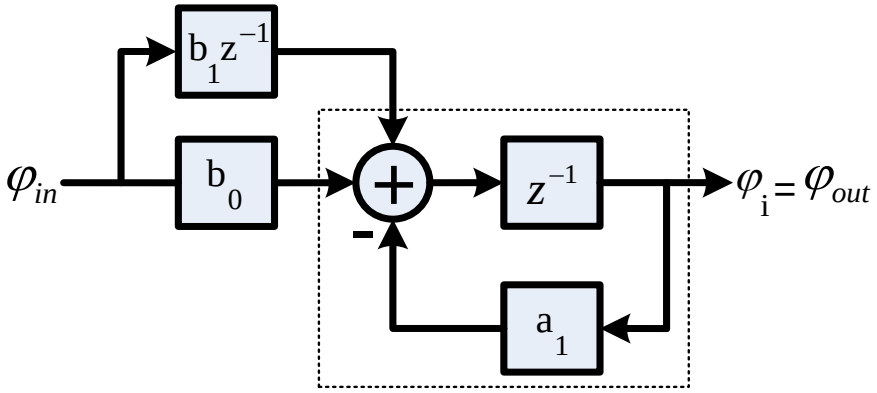
As the filter cut-off frequency decreases with a_1 approaching -1, Equation (4.7) reveals that the maximum input DC level that can be applied to the filter input reduces in the exact same way. In other words, very little input range is available as the filter bandwidth decreases. For low-pass filter realizations, the largest gain of the system occurs at DC. Hence, the above analysis is true for AC signals as well.

To get around this saturating problem, a new filter topology is required. In the process of discovery, two possible TM topologies were found and are shown in Figure 4-2. The block diagram of Figure 4-2(a) is a first-order TM filter realization involving a single adder. The transfer function of this filter realization is given by

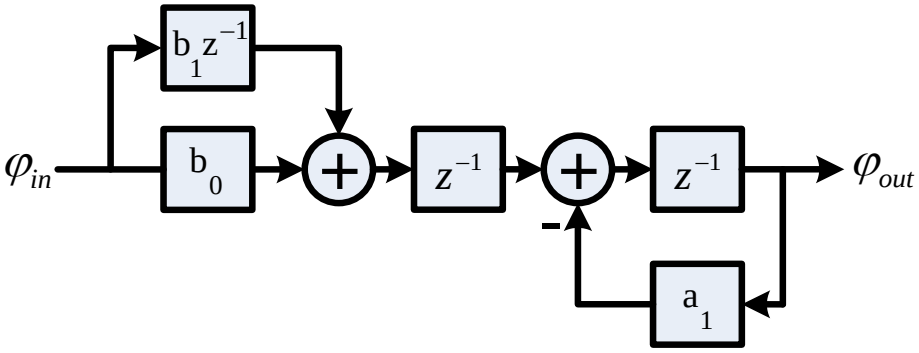
$$\frac{\varphi_{out}}{\varphi_{in}} = z^{-1}\frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \tag{4.8}$$

The block diagram of Figure 4-2(b) involves the use of two adders. The transfer function of this filter realization is given by

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \tag{4.9}$$



(a)



(b)

Figure 4-2: Two possible non-saturating TM-Filter topologies (a) single-adder realization, (b) two-adder realization.

In the case of the single-adder filter topology in Figure 4-2(a), the premature saturation problem was resolved by re-arranging the front-end summer block of the original design (Figure 3-2) so that only the difference of the input and past states are combined and held in the localized memory element. This reduces the size of the signal circulating around with the integration operation and helps to improve the saturation limits.

To quantify the above statement, we recognize that the output of the filter is also the integrator output, allowing us to write the relationship between the integrator output and the input signal as

$$|\Phi_i| = \left| z^{-1} \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \right| |\Phi_{in}| \tag{4.10}$$

If, as before, we impose the integrator saturation limit

$$|\Phi_i| \leq \frac{T}{2} \tag{4.11}$$

The bounds of the input signal then becomes

$$|\Phi_{in}| \leq \left| \frac{1 + a_1 z^{-1}}{b_0 + b_1 z^{-1}} \cdot \frac{1}{z^{-1}} \right| \frac{T}{2} \tag{4.12}$$

which further reduces to

$$|\Phi_{in}| \leq \left|\frac{1 + a_1 z^{-1}}{b_0 + b_1 z^{-1}}\right| \frac{T}{2} \tag{4.13}$$

For the special case of DC signals (the largest signals associated with a low-pass topology), we see the input saturation limit is given by

$$\Phi_{in,max} = \left|\frac{1 + a_1}{b_0 + b_1}\right| \frac{T}{2} \tag{4.14}$$

However, the term $\left|\frac{1+a_1}{b_0+b_1}\right|$ represents the inverse of the DC gain of the first-order filter function, so we can rewrite Equation (4.14) as

$$\Phi_{in,max} = \frac{1}{Gain_{DC}} \frac{T}{2} \tag{4.15}$$

For unity-gain filter functions, it is evident from the above expression that the saturation limit will be equal to the maximum available signal range set by the clock reference, e.g. T/2. Of course, for higher filter gains, the saturation limit is reduced by the same increase in the system gain. This fact is of course true for all signal-processing operations regardless of their representation, e.g., time-mode versus voltage-mode. Hence, the filter topology proposed here never saturates regardless of its input.

In the case of the second filter topology of Figure 4-2(b), the addition and integration operations are distributed across two separate adders with the integration

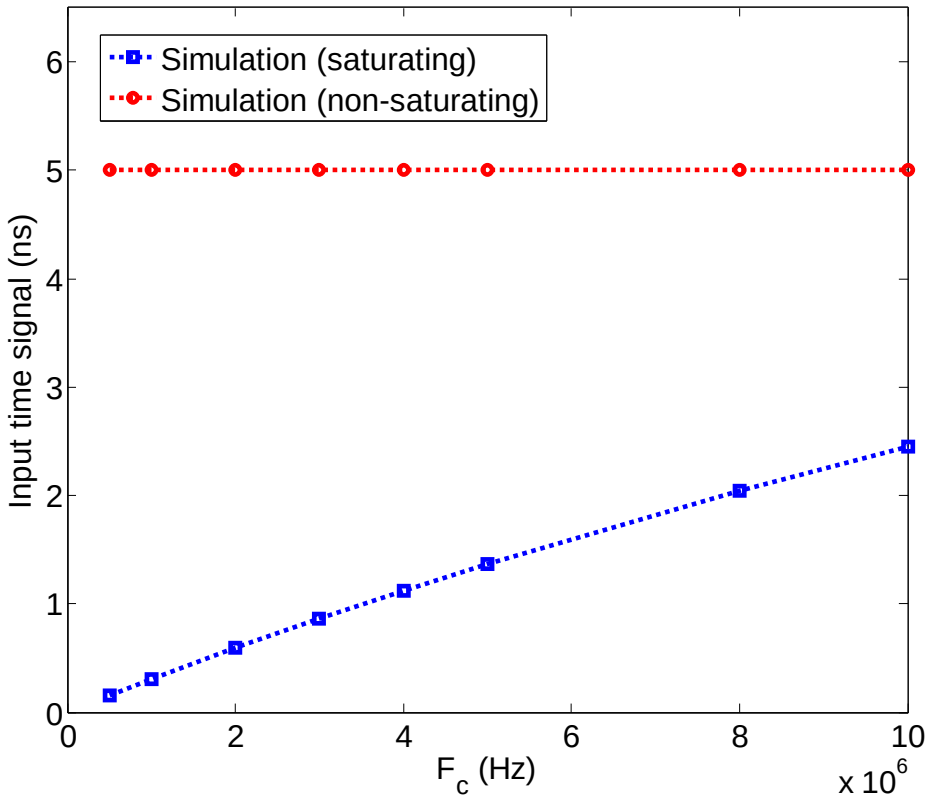


Figure 4-3: Maximum tolerable input time signal vs. filter cut-off frequency for non-saturating and saturating topologies (T/2=5 ns).

operation placed in the output stage. Here the addition and scaling operation using very small value coefficients (i.e., b_0 and b_1) reduces the magnitude of the signals seen by the integrator and helps to improve its saturation limits. A similar analysis of the input saturation limit leads to the same conclusion – the maximum signal range is set by *T/2*.

A set of transistor level simulations were conducted on each filter topology for the low-pass case. For each topology the filter cut-off frequency is changed from high to low values. At each step the maximum tolerable DC time-mode signal that results in a valid

output is measured. Figure 4-3 depicts the maximum input time-mode signal that can be handled in both topologies versus various cut-off frequencies. Simulation results 100% matches with the ones predicted by Equations (4.7) and (4.15).

In the next section, we shall make use of the filter realization of Figure 4-2(b) as a cascade of several first-order sections to realize a second and third-order transfer function. While either non-saturating filter topology of Figure 4-2 could be used, the structure of Figure 4-2(b) required the least amount of change to the original filter structure of Figure 3-2(b) and hence was selected for the remaining work of this thesis.

4.2 High-Order Time-Mode Filters

High-order filters are used in applications when very sharp stopband responses are required. As we know, the gain of a first-order filter drops at a rate of 20 dB/dec. However, in the case of second or third-order filters the drop increases to 40 or 60 dB/dec, respectively. By increasing the filter order, the filter frequency response approaches an ideal brick-wall like-shape.

In active IIR filter design, various methods are utilized to realize high-order filters, such as cascade of low-order stages, state-space realizations, and operational simulation of LC ladder networks. While the latter two methods provide greater flexibility and robustness in terms of component spreads and signal handling, at this point in time, it is unclear how these methods can be extended to a time-mode realization due

to the lack of negative numbering system, i.e. negative time-mode signals.

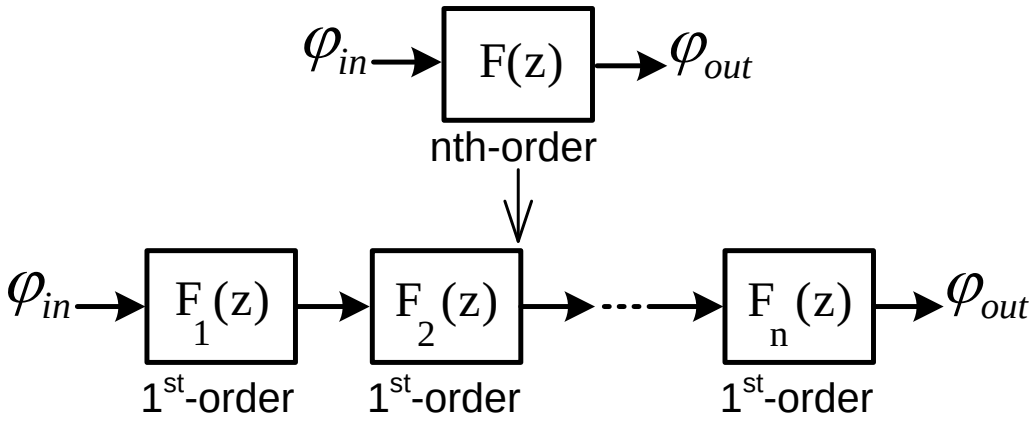


Figure 4-4: *N*th-order TM-Filter realization

Nonetheless, the method of cascading several first-order stages can be used to create high-order filter transfer functions even though it is well recognized that it is not the most efficient method of achieving controlled levels of attenuation. This method is depicted in Figure 4-4 where each first-order section would be realized with one of the two non-saturating filter topologies of Figure 4-2.

For instance, by cascading two identical first-order sections of Figure 4-2(b) together, each having transfer function

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \tag{4.16}$$

A second-order filter results with overall transfer function

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-4}\frac{b_0^2 + 2b_0b_1z^{-1} + b_1^2z^{-2}}{1 + 2a_1z^{-1} + a_1^2z^{-2}} \tag{4.17}$$

In general, cascading *N* identical first-order sections (Figure 4-2(b)) together results in the following *N*-th order transfer function,

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = \prod_{i=1}^{n} z^{-2}\frac{b_{0_i} + b_{1_i}z^{-1}}{1 + a_{1_i}z^{-1}} \tag{4.18}$$

As an example, two different filter realizations were created using the same first-order section. Specifically, a first-order unity-gain low-pass transfer function having a cut-off frequency of 1.5 MHz operating with a sampling rate of 100 MHz was used. Its transfer function is given by

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{0.04504 + 0.04504z^{-1}}{1 - 0.9099z^{-1}} \tag{4.19}$$

A second-order filter realization consisting of a cascade of two identical first-order sections leads to an overall transfer function of

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-4}\frac{0.002028 + 0.004056z^{-1} + 0.002028z^{-2}}{1 - 1.82z^{-1} + 0.828z^{-2}} \tag{4.20}$$

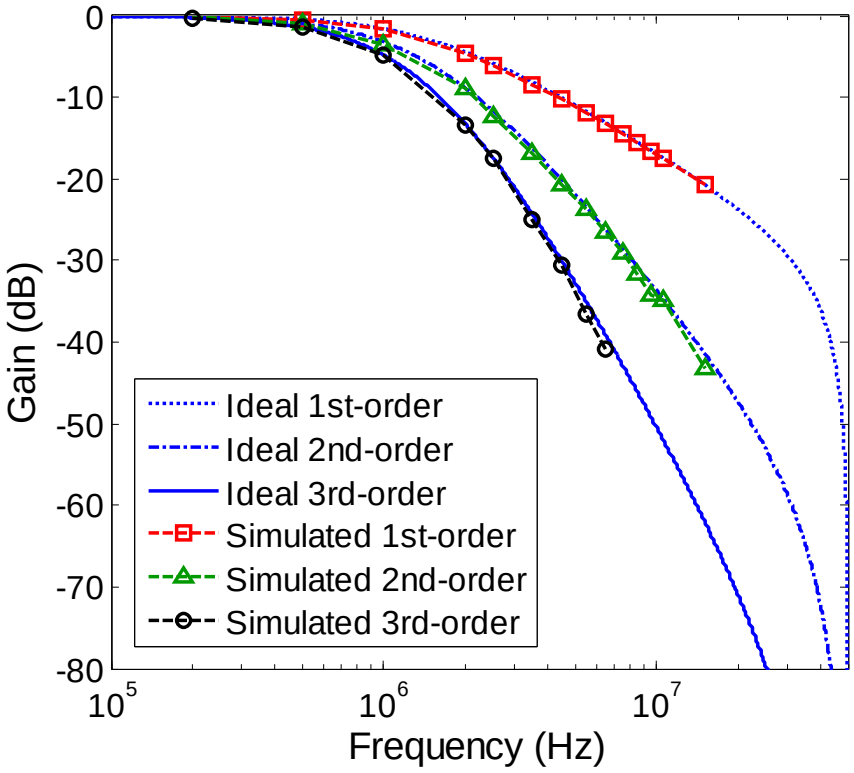


Figure 4-5: Frequency response of 1st, 2nd and 3rd-order TM-Filters.

Likewise, a third-order filter realization consisting of a cascade of three identical first-order transfer functions leads to an overall transfer function of

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-6}\frac{9.134\times10^{-5} + 2.74\times10^{-4}z^{-1} + 2.74\times10^{-4}z^{-2} + 9.134\times10^{-5}z^{-3}}{1 - 2.73z^{-1} + 2.484z^{-2} - 0.7534z^{-3}} \tag{4.21}$$

Figure 4-5 depicts the frequency response of 1st, 2nd, and 3rd TM-filters simulated at the transistor-level using Spectre along with their ideal response evaluated in MATLAB. As is evident, the transistor-level simulated results agree with theory. Spectre reveals that the high-order filter realizations do not experience any additional saturation effects; the

results are identical to those shown in Figure 4-3 for the non-saturating topology. Secondly, as the filter order increases, the rate of change of attenuation increases by 20 dB/dec for each additional filter order. However, the cut-off frequency decreases with increasing filter order. These two trade-offs are illustrated in Figure 4-6. The drop in filter bandwidth can easily be accommodated by selecting the first-order filter transfer function to have a larger cut-off frequency, or by selecting each stage to have different filter transfer functions. In the end, these results simply illustrate that high-order filter structures can be realized through the cascade of several first-order sections. The next chapter will illustrate an important application of reconstructing time-mode signals.

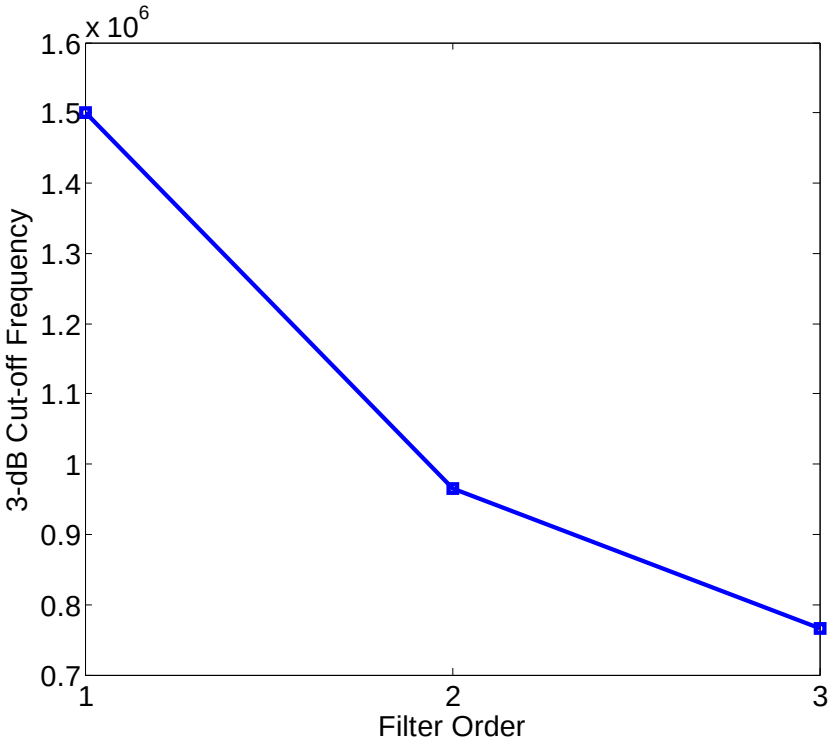


Figure 4-6: Filter cut-off frequency vs. order.

4.3 Summary

In this chapter, the saturation problem of the time-mode filter first proposed in Chapter 3 was investigated. The saturation effect took place in the front-end adder, which acts as a damped integrator. The input referred saturation point was derived mathematically and was shown to be correlated with the cut-off frequency of the filter function. By rearranging the order of integration and scaling internal to the filter, two new topologies were discovered that eliminated the saturation effect altogether. The new filter structures are capable of handling maximum sized input time-mode signals independent of the filter cut-off frequency. These were shown to be well suited for narrowband filter applications.

Another section of this chapter demonstrated the use of these non-saturating first-order filter sections for use in the realization of filter circuits with high-order transfer functions. The next chapter will demonstrate an important area where time-mode filters have useful applications in digital-to-time reconstruction operations.

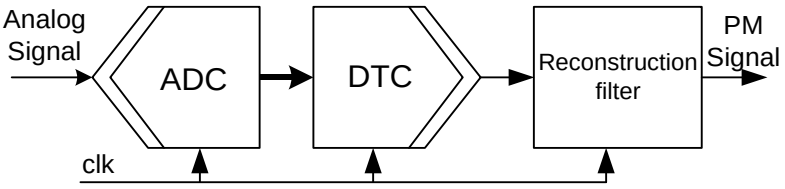
Chapter 5

Phase-Modulated Signal Generation Application

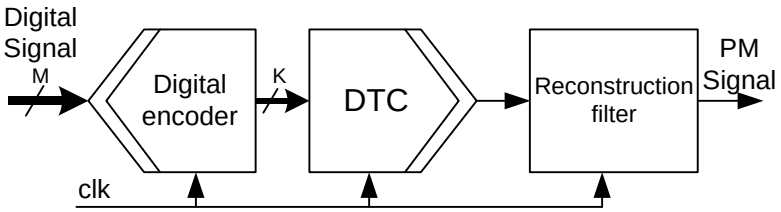
In this chapter we shall demonstrate the application of the time-mode filters of Chapters 3 and 4 for use as reconstruction filters in a phase-modulated (PM) signal generator. In previous PM signal generation works, the reconstruction operation was implemented using a high-order phase-lock loop (PLL). While a PLL is a very robust and reliable circuit element, it consumes large amounts of silicon area and power. In this chapter, it will be shown that time-mode filter circuits with lower power and silicon area requirements can replace the operation of a PLL. This chapter will begin by providing a brief review of the principles behind the phase-modulation signal generation method followed by a look at the use of a TM filter as a reconstruction filter.

5.1 Sigma-Delta Phase Modulation

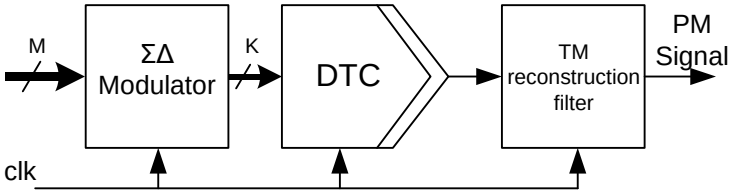
Time-mode circuits have recently been used for establishing picosecond time delays, as well in the synthesis of a wide range of clock signals with variable frequency [5], [15]. The basic idea as it applies to the synthesis of a phase-modulated (PM) signals is illustrated in Figure 5-1(a) where an ADC, DTC and reconstruction filter are used to



(a)



(b)



(c)

Figure 5-1: PM signal generation using TMSP for (a) analog inputs, (b) digital inputs.

convert an analog signal into the phase of some clock-like signal. Here an ADC digitizes the analog input and the output bits are converted to a time-domain signal using a DTC. The reconstruction filter acts to average out the variations in the phase steps so that it is a smooth function in phase. Similarly, this same procedure can be repeated on digital inputs, as shown in Figure 5-1(b). In the second approach, an M-bit wide input digital signal is mapped to a K-bit wide input to a K-bit resolution DTC. In this case, the phase output of the DTC can realize 2^K different phase levels. By replacing the encoding

operation by a M-to-K-bit sigma-delta modulation operation [5] as shown in Figure 5-1(c), the output of the DTC can be made to realize a much large number of phase steps. This is subject to the ability of the reconstruction filter removing the out-of-band excess quantization noise generated by the sigma-delta modulation operation. More specifically, the overall resolution of the digital-to-time conversion is a function of the SNR of the conversion process, typically expressed in terms of the equivalent number of bits, ENOB given by

$$ENOB = \frac{SNR - 1.76}{6} \tag{5.1}$$

5.1.1 ∑Δ-Modulator

As shown in Figure 5-1(c) a sigma-delta modulator can be employed to encode an M-bit digital signal to a K-bit one. As M is much greater than K, this encoding procedure will introduce some quantization noise. However, in virtue of the sigma-delta encoding process, this noise is pushed away from the signal bandwidth, where it can be removed by the reconstruction filtering operation. Collectively, the sigma-delta modulation operation combined with the reconstruction filtering operation establishes the overall maximum SNR of the conversion process (Equation (5.1).

Figure 5-2 illustrate the block diagram realization of a single-bit sigma-delta modulator. This structure is commonly used for software-based sigma-delta modulation [16], as it has a unity-gain signal transfer function and its noise transfer function is set

simply by selecting the appropriate value for the loop filter, H(z). It is the selection of H(z) that establishes one aspect of the maximum SNR value achievable by the DTC operation [17]. The other is the reconstruction filtering operation.

As mentioned before, the sigma-delta modulator is implemented in software (using MATLAB/Simulink). Here a CAD tool called DSMOD which implements a number of design algorithms, including sigma-delta modulators, allowing a quick comparison of theoretical and simulated behaviors [18].

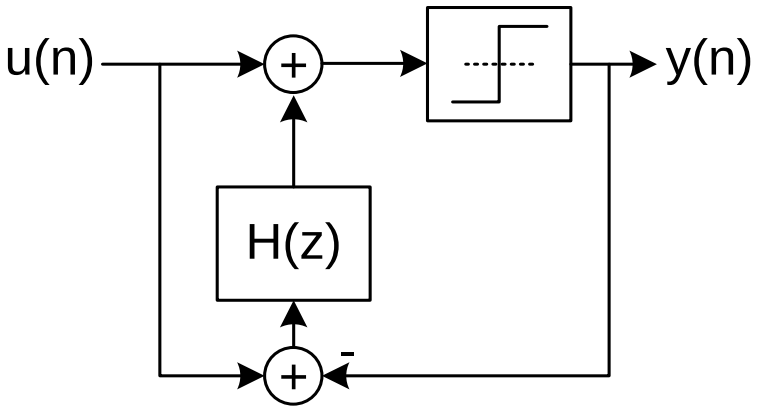


Figure 5-2: State-space realization of a single-bit ∑Δ modulator.

5.1.2 Digital-to-Time Converter (DTC)

A DTC, as explained previously in Section 2.8.1, converts a digital word into a time-domain signal by delaying a reference clock in proportion to the magnitude of the input digital word. For instance, in the case of a 1-bit DTC, a "1" input may shift the output by 45° with respect to the clock reference and a "0" input may cause no shift of

the reference at all. This is illustrated in Figure 5-3. Of course, any other combination of phases can also be used without loss of generality, as well as any additional number of discrete phase steps.

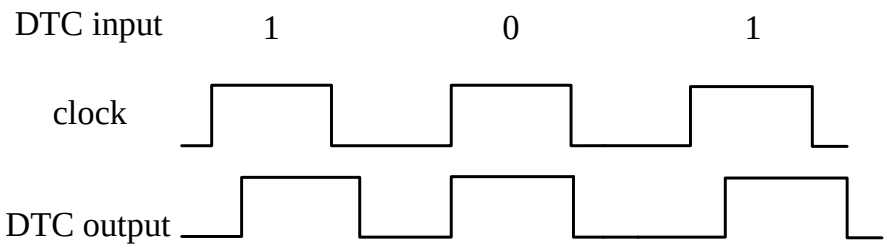


Figure 5-3: DTC output according to its input digital code.

5.1.3 Time-Mode Reconstruction Filter

In the phase modulation generation scheme proposed in Figure 5-1(c) only the reconstruction filter is physically required. Its sole purpose is to remove the out-of-band quantization noise added by the sigma-delta modulation process so as to average out the time-mode signal generated by the DTC. In [5] and [17], the reconstruction filter was realized using a high-order phase-locked loop (PLL) circuit constructed from discrete components. In that work, a 6^{th}-order type-II unity feedback PLL with a half-power bandwidth of 100 kHz was used. The complete schematic of this PLL is shown in Figure 5-4. The loop filter consists of a cascade of Tow-Thomas biquads and a first-order integrator circuit. It is important for the reader to recognize the complexity associated with this particular PLL. It consists of three main blocks: a phase detector, a loop filter and a VCO. While the phase detector is quite small, the loop filter requires a large

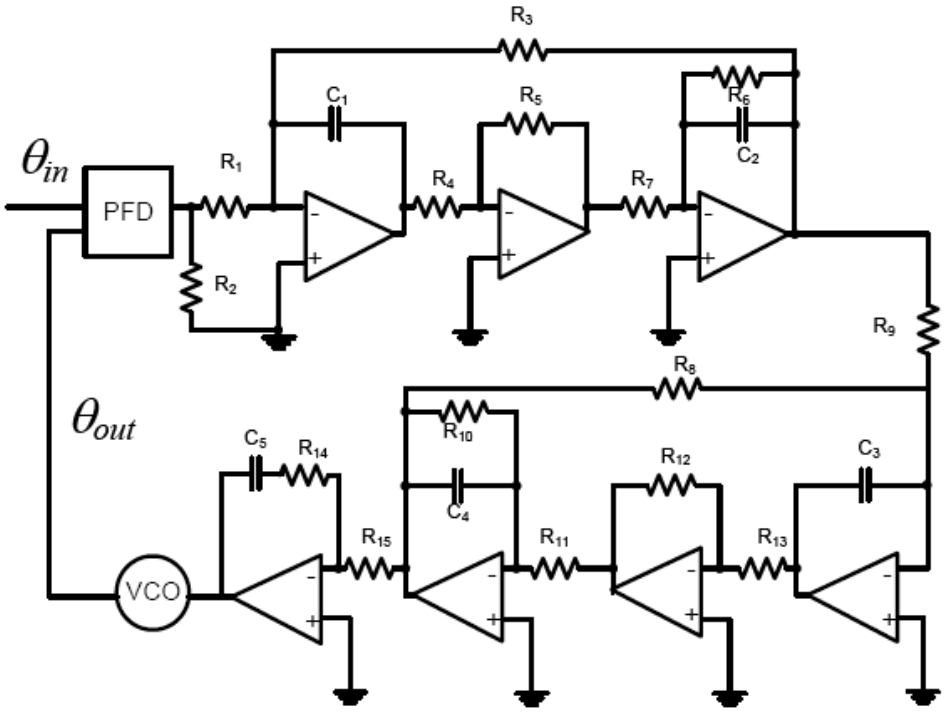


Figure 5-4: circuit schematic of a 6th-order PLL used in [5].

amount of silicon area, as it consists of 7 op amps. The VCO also requires a large amount of silicon area. In addition, the power requirement is quite large (i.e., on the order of tens of mW). While lower order PLL structures can be used, they too will require large amounts of silicon area and power. It is here where TM filters shine and is expected to outperform PLL circuits in general. Figure 5-5 shows the circuit schematic of a non-saturating TM filter used for phase signal generation. The dimension of this filter is the same as that of a saturating TM filter topology, since only the adders have been rearranged. Hence, the same silicon area will be occupied (i.e., 100 um x 1070 um) and the same power (i.e., 670 μW) will be consumed, which is considerably smaller.

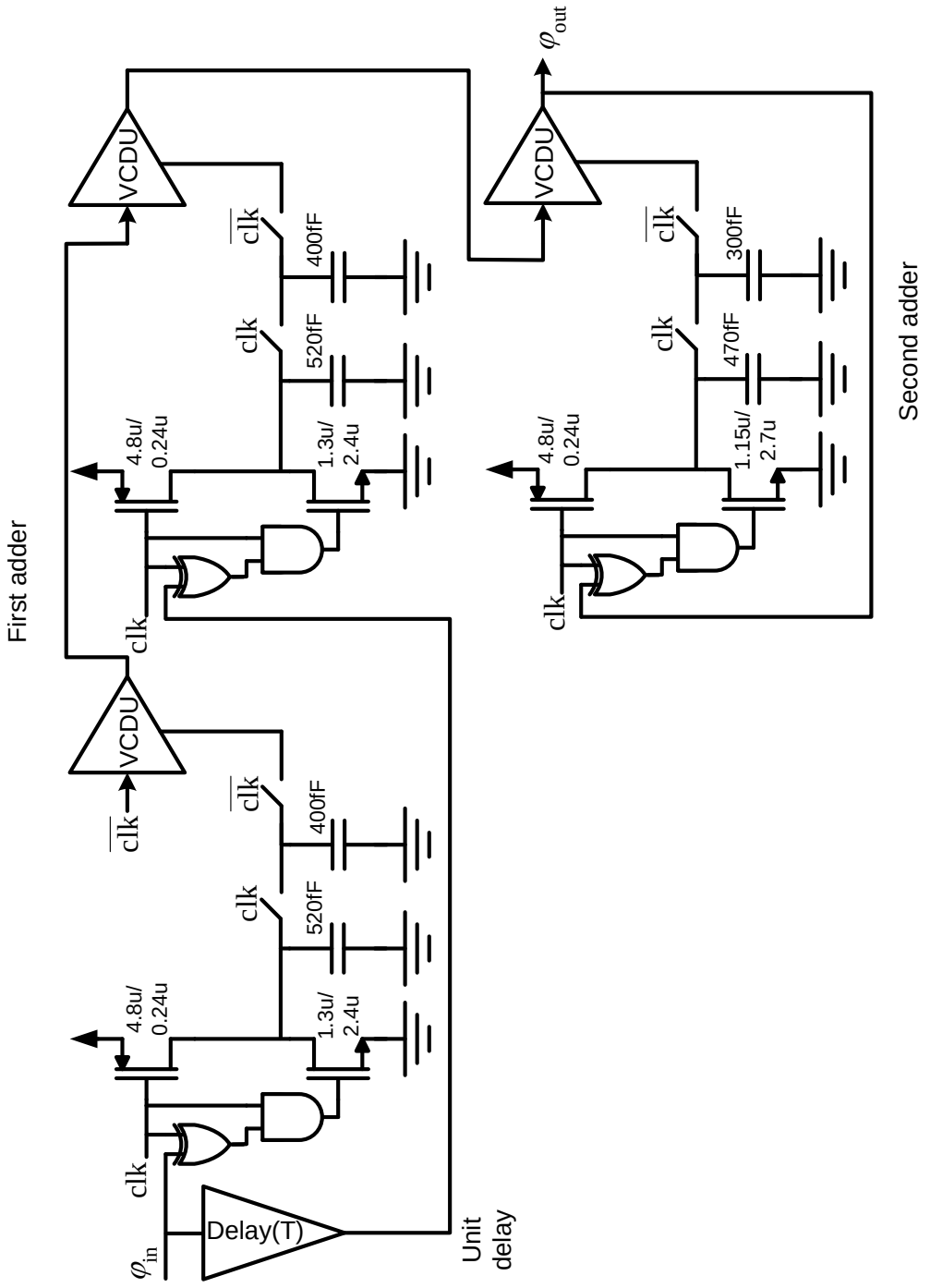


Figure 5-5: A TM filter realization used for phase signal generation.

5.2 TM – PLL Comparison and Overall Operation

In practice the phase generation scheme shown in Figure 5-1(c) is reduced to a memory and a phase reconstruction filter, as shown in Figure 5-6. The bits generated in software, which are the output of sigma-delta modulator and DTC, are stored in a circular memory. The output is then given to a reconstruction time-mode filter, implemented either using a PLL or a time-mode filter, which in turn produces the phase-modulated output signal.

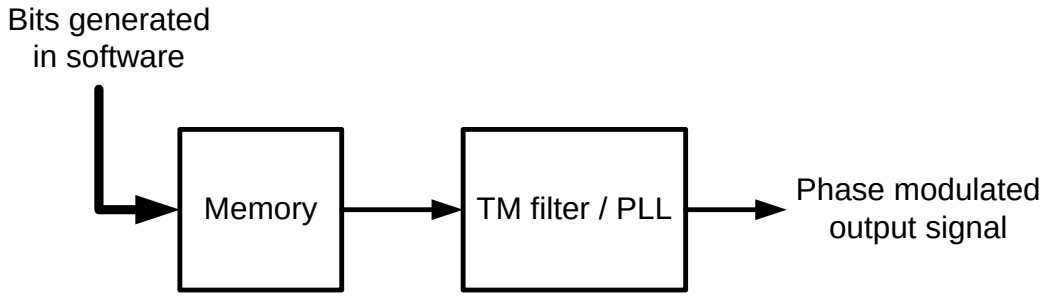


Figure 5-6: A practical phase signal generation scheme.

In [5] a 5^{th}-order sigma-delta modulator was used with an oversampling ratio of 64 along with a DTC with a 4-bit mapping scheme.

In this work, a 5^{th}-order one-bit $\sum\Delta$ modulator was implemented in MATLAB/ Simulink. Figure 5-7 shows the schematic view of this block. The discrete state-space representation of the transfer function, H(z), derived using the DSMOD software, is as follows:

$$A = \begin{bmatrix} 4.997323 & -9.991970 & 9.991970 & -4.997323 & 0.999996 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$C = [0.789734 \quad -2.856669 \quad 3.901665 \quad -2.382740 \quad 0.548619]$$

$$D = [0]$$

A switch is used as a single-bit quantizer. The input to our simulation is a sine wave signal with amplitude of 300 mV at 300 kHz. The output bits are captured in an array and used for further process in the DTC.

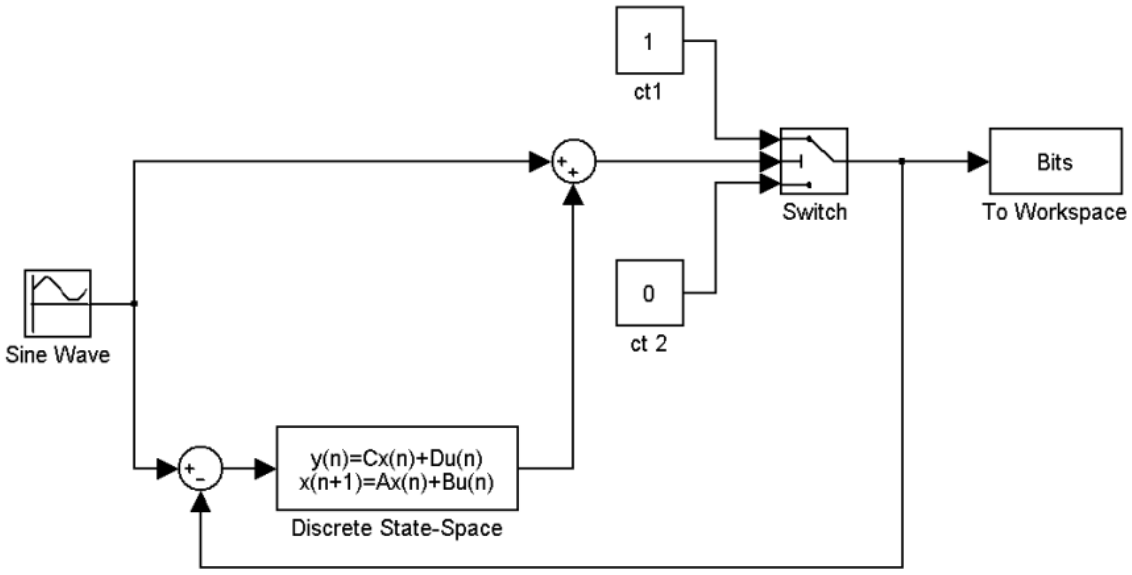


Figure 5-7: Schematic view of a single-bit ∑Δ modulator

The DTC is also implemented in software using a look up table. Note that even though a single-bit DTC is used in this work, an 8-bit phase shift representation is used that provides phase steps of 0^0 and 45^0. The conversion process is summarized in Table 5-1. Moreover, these phase shifts correspond to time delays of 0 and T/4 seconds.

Table 5-1: Bit mapping scheme

Digital input	DTC output
0	11110000 (0^o phase shift)
1	01111000 (45^ophase shift)

The output bits of the DTC are stored in a memory, where they are applied to the reconstruction filter at the appropriate frequency. Depending on the number of bits used to represent the phase of the clock signal, the bit rate must be adjusted to maintain the same clock rate uniformly throughout all bit transmissions. For the case described here using an 8-bit representation, the DTC must be clocked at 8 times the sampling frequency of the $\sum\Delta$ modulator/TM filter, i.e.,

$$F_{DTC} = F_{memory} = 8 \times F_S \tag{5.2}$$

First-order time-mode filters with a sampling frequency of 100 MHz are employed as the reconstruction filter. One should note that according to the bit-mapping scheme introduced in Table 5-1 a 45^o phase shift is equal to T/4 delay, which is 1.25 ns when operated from a 100 MHz clock. According to Figure 4-3 this amount of delay is

tolerated by TM filters with cut-off frequencies greater than 5 MHz when a saturating topology is used. However, tighter bandwidths can be achieved when a non-saturating topology is used. In the case of the saturating TM filter, it has transfer function

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{0.1367 + 0.1367z^{-1}}{1 - 0.7265z^{-1}} \tag{5.3}$$

while the non-saturating TM filter uses transfer function

$$\frac{\Phi_{out}(z)}{\Phi_{in}(z)} = z^{-2}\frac{0.03047 + 0.03047z^{-1}}{1 - 0.9391z^{-1}} \tag{5.4}$$

Figure 5-8 illustrates the PSD of the phase-modulated signal resulting from the set up shown in Figure 5-6 for a sinusoidal input using the above described design parameters corresponding to a filter cut-off frequency of 5 MHz. The simulation was repeated using a cut-off frequency of 1 MHz and the results superimposed onto the same PSD plot of Figure 5-6. As is evident, the filter with the 1 MHz bandwidth results in least amount of quantization noise at the output.

In addition, higher order filters can also be utilized in this application to further improve the output signal quality by rejecting more quantization noise. Figure 5-9 indicates the achieved SNR for different filter orders.

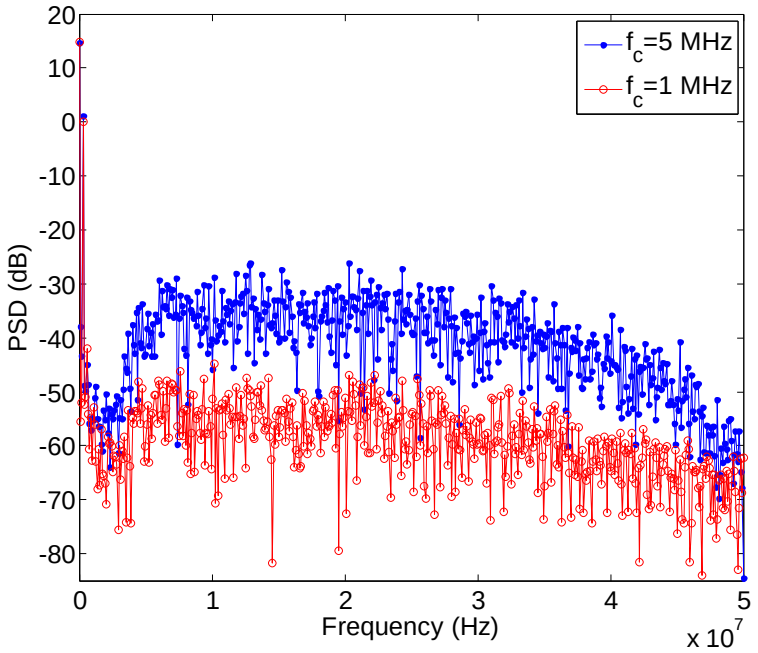


Figure 5-8: PSD of demodulated output signal for different cut-off frequencies corresponding to a first order filter.

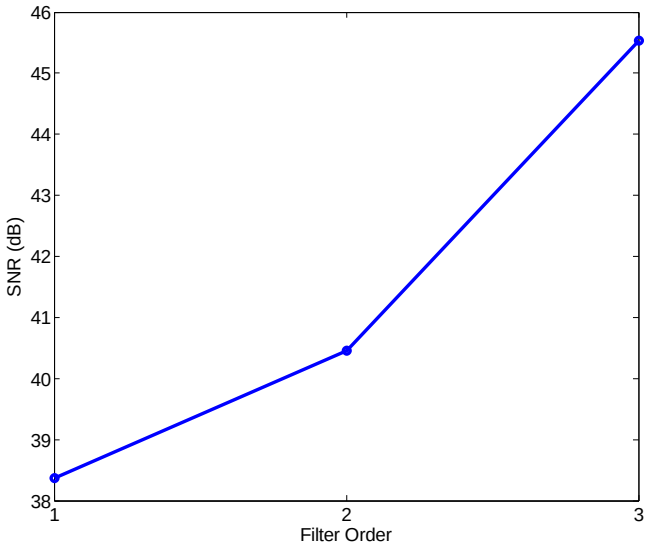


Figure 5-9: Output SNR vs. filter order.

5.3 Summary

In this chapter it was shown that TM filters could replace the operation of a PLL acting as a reconstruction filter in a sigma-delta phase signal generation scheme. Through various estimates, large amount of silicon area and static power can be saved using a TM filtering approach. This makes TM filters extremely valuable for future applications of phase-signal generation.

Chapter 6

Conclusion

6.1 Thesis Summary

A new set of time-mode signal processing building blocks, such as time-mode adders and time-mode integrators, were presented in this thesis. At the core of these building blocks are voltage-controlled delay units (VCDUs). These VCDUs were assembled into various basic mathematical operations of adding, scaling and integration. Using these building blocks, an IIR filter design methodology was proposed resulting in what is referred to in this thesis as time-mode (TM) filters. Beginning with the development of several first-order low-pass IIR filter topologies, these were cascaded to form a high-order filter realization. In the discovery of these filter topology, two classes of filter structures were recognized. One that was extremely sensitive to the magnitude of the input signal, called a saturating topology, and the other class insensitive to the magnitude of the input signal. This class of filter topology is referred to as a non-saturating structure. The impact of this sensitivity on the input signal level restricted the bandwidth of a saturating TM filter topology to be limited to wide bandwidth situation

having low-Q poles. In contrast, the non-saturating TM filter topology was capable of realizing very narrowband filters.

In order to investigate the behavior of these new filter structures, a first-order low-pass saturating TM-filter prototype was fabricated in a 0.13 µm CMOS technology from IBM. The IC occupied 170 µm x 100 µm of the silicon space and consumed 670 µW from a 1.2 V supply operating at a sampling frequency of 100 MHz. One should note that consideration of other filter metrics such as output noise and distortion is required to be able to clearly comment on whether performance is traded off against low power consumption. This prototype confirmed both the design methodology of positioning the pole-zero combination in the appropriate location in the z-plane, as well, the saturating problem mentioned above.

As the separation of saturating and non-saturating topologies was recognized very late in the prototyping phase, no IC implementation was constructed. Rather, our decisions relating to the non-saturating TM filter realization was based solely on transistor-level simulation. Based on preliminary data, this new non-saturating topology is expected to require similar levels of silicon area and static power. Owing to the fact that the non-saturating topology works with both wideband and narrowband situations, it is most likely the prefer topology for future TM filter realization.

High-order very narrowband filters can be synthesized using a cascade of first-order sections. While a cascade of first-order sections is not the most efficient means to

implement high-order filters, as the filler transfer function involves real poles only (instead of complex ones), it does nonetheless provide a practical filter solution.

One application of the narrowband TM filters is in the realization of a reconstruction filter for a sigma-delta phase modulation scheme. Here a high-quality arbitrary phase modulated signal is generated directly from a sequence of bits passing through the TM filter. Using a sigma-delta based encoding method, together with a DTC bit-mapping algorithm; a TM reconstruction filter is used to remove the excess quantization noise introduced by the sigma-delta modulation operation. In previous works, the reconstruction filter was implemented using a PLL. In comparison, the PLL is bulky, requires large amount of silicon area and consumed large amounts of static power. As a rough estimate, the power reduction is expected to be over two orders of magnitude using the TM filter realization. Estimate to the silicon area improvement is difficult to predicted at this time, as this PLL was constructed using discrete components. Nonetheless, large silicon area reduction is expected owing to the reduction in the number of op amps used.

6.2 Future work

Since time-mode signal processing is a relatively new technology, there are several future endeavors that one can follow from this work. For instance, voltage-mode sampled-data filters have been extensively studied and advanced over the past years; many high-performance techniques have been developed in order to construct these types

of filters. One could apply the same ideas to time-mode filters, opening a whole new direction for future research and work. One of the contributions of this work was to introduce time-mode filters as a replacement for PLLs in anti-imaging and phase reconstruction applications. One specific example was the sigma-delta phase-modulation scheme. However, one could envision other phase filtering or reconstruction applications in which a time-mode filter can be used. The following list summarizes some examples that can be followed to extend this work:

1. As explained before almost all the basic building blocks in TMSP are built based on delay elements, specifically VCDUs, even though they suffer from nonlinearities and low conversion gain. Conversion gain can be boosted up by cascading several stages; however, this approach occupies more circuit area and does not help with non-linearity issues. Linearization of VCDUs will be a great contribution.
2. The lack of simple and compact subtractors with signal scaling capability prevented us from constructing high-order filters with complex poles. Building such a block will complete the set of required mathematical operations needed in this domain.
3. Another important issue in TMSP is the lack of processing TM signals that lag the reference clock signal. In some literature, this referred to as the negative signal representation. In this thesis, all signal processing operations were performed by advancing the edge of a reference clock, instead of delaying it. If the roles of the

signal with respect to the reference clock could be reverse, this would enable a both positive and negative number representation. This in turn would enable the realization of negative feedback using TM structures. At this time, all designs so far have been positive feedback structures.

4. Construct a CMOS implementation of the class of non-saturating time-mode filters.
5. Investigate other applications where TM filters can be used.

References

[1] C.S. Taillefer and G. W. Roberts, "Process-Insensitive Modulated-Clock Voltage Comparator," in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 3910-3913, May 2006.

[2] C. S. Taillefer and G. W. Roberts, "Delta–Sigma A/D Conversion Via Time-Mode Signal Processing," *IEEE Transactions on Circuits and Systems*, vol. 56, no. 9, pp. 1908-1920, Sept. 2009.

[3] D. An and G. W. Roberts, "A metastability-independent time-to-voltage converter," in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 2298-2301, 2008.

[4] M. Ali-Bakhshian and G. W. Roberts, "A Semi-Digital Interface for Capacitive Sensors," in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 1957-1960, 2009.

[5] S. Aouini, K. Chuai, and G. W. Roberts, "A Low-Cost ATE Phase Signal Generation Technique for Test Application," in *IEEE International Test Conference*, Novemeber 2010.

[6] C. S. Taillefer and G. W. Roberts, "Delta-sigma analog-to-digital conversion via time-mode signal processing," in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 13–16, May 2007.

[7] M. Oulmane and G. W. Roberts, "A CMOS Time Amplifier for Femto-Second Resolution Timing," in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 509–512, May 2004.

[8] A. M. Abas, A. Bystrov, D. J. Kinniment, O. V. Maevsky, G. Russell, and A. V. Yakolev, "Time Difference Amplifier," *Electronic Letters*, vol. 38, pp. 1437-1438, November 2002.

[9] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 270-247, February 2000.

[10] P. Chen, C. C. Chen, and Y. S. Chen, "A Low-Cost Low-Power CMOS Time-to-Digital Converter Based on Pulse Stretching," *IEEE Transactions on Nuclear Science*, vol. 53, pp. 2215-2220, August 2006.

[11] I. Nissinen, A. Mantyniemi, and J. Kostamovaara, "A CMOS Time-to-Digital Converter Based on a Ring Oscillator for a Laser Radar," in *European Solid-State*

Circuits Conference, pp. 469–472, September 2003.

[12] P. Chen and S. L. Liu, "A Cyclic CMOS Time-to-Digital Converter with Deep Subnanosecond Resolution," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 605-608, May 1999.

[13] M. M. Guttman and G. W. Roberts, "Sampled-Data IIR Filtering Using Time-Mode Signal Processing Circuits," in *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 2285-2288, May 2009.

[14] CMRF8SF ESD Reference Guide, IBM, April 2005.

[15] S. Aouini and G. W. Roberts, "Frequency Synthesis Using Digital-to-Frequency Conversion and Filtering," *Electronics Letters*, vol. 46, no. 14, pp. 979-980, July 2010.

[16] X. Haurie and G. W. Roberts, "A Multiplier-Free Structure for 1-bit High-Order Digital Delta-Sigma Modulators," in *Proc. of the 38th Midwest Symposium on Circuits and Systems*, pp. 889-892, Aug. 1995.

[17] S. Aouini, K. Chuai and G. W. Roberts, "Anti-Imaging Time-Mode Filter Design Using A PLL Structure with Transfer Function DFT," *IEEE Transactions on Circuits and Systems - I*, March 2011 (in print).

[18] X. Haurie and G. W. Roberts, "A Design, Simulation and Synthesis Tool For Delta-Sigma-Modulator-Based Signal Sources," in *Proc. of the International Symposium on Circuits and Systems*, pp. 715-718, May 1996.