Frequency-Translating Delta-Sigma Modulation for Bandpass Analog-to-Digital Conversion of High-Frequency Signals

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Abstract

A traditional heterodyne receiver downconverts its input signal to one or more intermediate frequencies (IFs) before digitizing it at baseband. In a digital-IF receiver, the input signal is digitized directly at an IF using a bandpass analog-to-digital converter (ADC). Accordingly, the digital-IF receiver replaces the image-reject mixers and baseband filters of a heterodyne receiver with accurate and efficient digital functions, and therefore provides greater potential for reconfigurability. In order to maximize the advantages of a digital-IF receiver, a common design objective is to position the bandpass ADC as close as possible to the antenna, and to operate on the input signal at a high IF.

A bandpass ADC is efficiently implemented using a delta-sigma ($\Delta\Sigma$) modulator, which can provide high-resolution A/D (analog-to-digital) conversion over a relatively narrow band around an IF. In order to operate on high-IF signals, conventional bandpass $\Delta\Sigma$ modulators require high-frequency filters and high sampling rates, which can result in high sensitivity to circuit non-idealities and high power consumption. These disadvantages are addressed by the frequency-translating $\Delta\Sigma$ modulator, which uses downconversion mixing inside its $\Delta\Sigma$ loop to process high-IF signals using low sampling rates and primarily low-frequency filters.

This thesis investigates frequency-translating $\Delta\Sigma$ modulators for direct A/D conversion of high-IF signals. It first analyses the system architecture and performance limitations of an existing type of frequency-translating $\Delta\Sigma$ modulator that is based on image-reject mixing. This analysis is supported by an initial study on the effect of timing errors in a conventional $\Delta\Sigma$ modulator. The thesis then introduces a novel frequency-translating $\Delta\Sigma$ modulator that is based on single-path mixing. The advantages of the presented single-path architecture are demonstrated using an experimental $\Delta\Sigma$ modulator.

The experimental $\Delta\Sigma$ modulator is designed to digitize a 4 MHz input-signal band that is centred at an IF of 225 MHz. It uses a local oscillation signal with a frequency of 200 MHz to downconvert this input-signal band to an IF of 25 MHz inside its $\Delta\Sigma$ loop, and samples at 100 MHz. The experimental prototype was fabricated in a standard 65 nm CMOS process. It achieves a peak SNDR of 55 dB and a dynamic range of 57.5 dB, while consuming 13 mW from a 1-V power supply. It has a full-scale range of 700 $mV_{P\text{-}P}$.

Résumé

Un récepteur hétérodyne traditionnel transpose un signal en entrée vers une ou plusieurs fréquences intermédiaires (FI) avant de le numériser à la bande de base. Dans un récepteur numérique FI, le signal en entrée est numérisé directement à la fréquence FI à l'aide d'un convertisseur analogique-numérique passe-bande. Par conséquent, le récepteur numérique FI remplace les mélangeurs de réjection d'image et les filtres à bande de base d'un récepteur hétérodyne traditionnel par des fonctions numériques précises et efficaces. De ce fait, le récepteur numérique FI offre plus de possibilités de reconfiguration. Afin de maximiser les avantages d'un récepteur numérique FI, un objectif de conception fréquent consiste à placer le convertisseur analogique-numérique passe-bande aussi près que possible de l'antenne et de numériser le signal en entrée à une fréquence FI élevée.

Un convertisseur analogique-numérique passe-bande peut être réalisé efficacement en utilisant un modulateur delta-sigma ($\Delta\Sigma$). En effet, ce dernier procure une conversion A/N (analogique-numérique) à haute résolution sur une bande relativement restreinte centrée autour d'une fréquence FI. Afin de fonctionner sur des signaux à fréquences FI élevées, les modulateurs $\Delta\Sigma$ passe-bande classiques requièrent des filtres hautes-fréquences et des fréquences d'échantillonnage élevées, ce qui peut les rendre très sensibles aux non-idéalités du circuit et mener à une consommation électrique importante. Il est possible de remédier à ces inconvénients en utilisant un modulateur $\Delta\Sigma$ à transposition de fréquence. En effet, ce dernier utilise des mélangeurs dans sa boucle $\Delta\Sigma$ pour traiter des signaux à fréquence FI élevée à des fréquences d'échantillonnage faibles avec principalement des filtres basses-fréquences.

Cette thèse étudie l'utilisation de modulateurs $\Delta\Sigma$ à transposition de fréquence pour une conversion A/N directe de signaux à fréquence FI élevée. Elle analyse d'abord l'architecture et les limitations de performance d'un modulateur $\Delta\Sigma$ à transposition de fréquence basé sur un mélangeur de réjection d'image. Cette analyse est appuyée par une étude initiale effectuée sur l'effet d'erreurs d'horloge sur un modulateur $\Delta\Sigma$ classique. Cette thèse introduit ensuite un nouveau modulateur $\Delta\Sigma$ à transposition de fréquence basé sur un mélangeur de mono-trajet. Les avantages de cette architecture sont démontrés à l'aide d'un prototype de modulateur $\Delta\Sigma$.

Le prototype de modulateur $\Delta\Sigma$ est conçu afin de numériser une bande de signaux en entrée de 4 MHz centrée autour d'une FI de 225 MHz. Il utilise un signal à oscillation locale d'une fréquence de 200 MHz pour transposer cette bande de signaux en entrée vers 25 MHz à l'intérieur de sa boucle $\Delta\Sigma$ et effectue l'échantillonnage à 100 MHz. Ce prototype a été réalisé en utilisant un procédé CMOS standard de 65 nm. Il a un SNDR de 55 dB et une gamme dynamique de 57.5 dB tout en consommant 13 mW pour une alimentation de 1-V. Sa plage d'amplitude maximale est de 700 $\mathrm{mV_{P\text{-}P}}$.

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Claim of Originality

The research presented in this thesis is the result of two, largely separate, projects. Chapter 3 investigates the effect of timing errors in a conventional continuous-time $\Delta\Sigma$ modulator, and Chapters $4-8$ investigate a type of bandpass $\Delta\Sigma$ modulator that uses mixing in its feedback loop (i.e., a frequency-translating $\Delta\Sigma$ modulator). The main contributions of this thesis are summarized as follows:

- Chapter 3 presents a modeling technique to rapidly simulate the effect of timing errors introduced in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator. These errors are added directly to the input of the $\Delta\Sigma$ modulator and, therefore, can significantly limit its performance. The presented modeling technique offers a significant speed advantage over direct simulation methods and, as a result, is particularly useful for evaluating the performance loss due to clock jitter. The modeling technique presented in this chapter was published in [Cho07].

- The speed advantage of the presented modeling technique is also applied in Chapter 3 to simulate a variety of different rectangular DAC pulses, and to analyse their effect on the jitter sensitivity of both lowpass and bandpass $\Delta\Sigma$ modulators. The results of this analysis indicate that the jitter sensitivity of a lowpass architecture can be significantly reduced by imposing certain constraints on the timing of its DAC pulses, and by using multi-bit quantization. The results also indicate that the jitter sensitivity of a bandpass architecture cannot be improved using either technique. The analysis presented in this chapter was published in [Cho09a].

- Chapter 3 also presents a behavioural model, for Simulink, that directly represents the delay errors introduced in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator. This behavioural model is used to demonstrate both the accuracy and speed of the proposed modeling technique. It can be used in a wide variety of continuous-time $\Delta\Sigma$ modulators, including those not considered by the proposed modeling technique.

- Chapter 4 investigates an existing type of frequency-translating $\Delta\Sigma$ modulator that is based on *image-reject* mixing. It describes a synthesis procedure for this image-reject frequency-translating $\Delta\Sigma$ modulator, and derives a set of system-level constraints that must be satisfied to achieve this synthesis. These constraints affect the selection of the timing parameters, such as the sampling frequency, and the characteristic of the loop filter. They ensure that the feedback loop of an image-reject frequency-translating $\Delta\Sigma$ modulator is time-invariant and provides the correct noise-shaping characteristic. The developed constraints were published in [Cho09b].

- Chapter 4 also examines performance limitations of image-reject frequency-translating $\Delta\Sigma$ modulators. In particular, it demonstrates their sensitivity to path mismatch, which can be introduced by amplitude, phase, and delay errors in their timing signals, and by gain errors in their functional blocks.

- Chapter 5 proposes a novel type of frequency-translating $\Delta\Sigma$ modulator that is based on *single-path* mixing. It describes a synthesis procedure for this single-path frequency translating $\Delta\Sigma$ modulator, and develops a set of system-level constraints that must be satisfied to achieve this synthesis, as described above.

- Chapter 5 also proposes design techniques to enhance the performance of a single-path frequency-translating $\Delta\Sigma$ modulator. The presented techniques specify the topology of its loop filter, the properties of its noise-shaping characteristic, and the selection of its timing parameters. Chapter 5 further derives a complete set of design equations for the single-path frequency-translating $\Delta\Sigma$ modulator.

- Chapters 6, 7, and 8 present the system architecture, circuit-level implementation, and measured results of an experimental single-path frequency-translating $\Delta\Sigma$ modulator. This experimental $\Delta\Sigma$ modulator is used to validate the synthesis procedure and design techniques proposed in Chapter 5. In addition, its measured performance is competitive with state-of-the-art bandpass $\Delta\Sigma$ modulators. The system architecture and measured performance of the experimental prototype were published in [Cho11].

A significant portion of the work presented in this thesis has been published in refereed journals and conference proceedings. In particular, the single-path frequency-translating $\Delta\Sigma$ modulator described in Chapters 5 – 8 was presented at the 2011 Custom Integrated Circuits Conference (CICC), and received a student scholarship award from the CICC Committee for being one of the highest-rated student papers. Section 9.1 provides a list of the publications that resulted from the work presented in this thesis.

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α, β	normalized delay of the rising/falling edge of a DAC pulse
$\widehat{\alpha}$, $\widehat{\beta}$	normalized delay of the rising/falling edge of a DAC pulse with time-delay errors $\Delta\alpha$ and $\Delta\beta$
$\Delta\alpha$, $\Delta\beta$	time-delay error in the rising/falling edge of a DAC pulse
B	number of quantization bits
f_{B}	signal bandwidth
f_{C}	centre frequency of a conventional bandpass $\Delta\Sigma$ modulator
$f_{\mathrm{C}i}$, $f_{\mathrm{C}o}$	input/output centre frequency of a downconversion bandpass $\Delta\Sigma$ modulator (frequency-translating or subsampling)
f_{LO}	frequency of the LO signal
f_{S}	frequency of the sampling clock
k_{S}, k_{D}	parameter that constrains the period/delay of the sampling clock in a frequency-translating $\Delta\Sigma$ modulator
$H_{\mathrm{DAC}}(s)$	transfer function of the feedback DAC
$H_{\mathrm{IL}}(s)$	transfer function of the inner-loop filter
$H_{\mathrm{IL,B}}(s)$	feedback component of the inner-loop filter
$H_{\mathrm{IL,F}}(s)$	forward component of the inner-loop filter
$H_{\mathrm{L}}(s)$	loop transfer function of a continuous-time $\Delta\Sigma$ modulator
$\hat{H}_{\mathrm{L}}(s)$	effective loop transfer function of a frequency-translating $\Delta\Sigma$ modulator

$H'_{\mathrm{L}}(z)$	loop transfer function of a discrete-time $\Delta\Sigma$ modulator
$\widehat{H}'_{\mathrm{L}}(z)$	discrete-time loop transfer function that models timing errors
$H_{\mathrm{OL}}(s)$	transfer function of the outer-loop filter
$\hat{H}_{\mathrm{OL}}(s)$	effective transfer function of the outer-loop path
N	order of the loop filter
P_d	total distortion power
P_n	total noise power (quantization noise, circuit noise)
$P_{n,\,\mathrm{B}}$	total noise power in the signal band
P_q	quantization noise power
$P_{q,\,\mathrm{B}}$	quantization noise power in the signal band
P_s	signal power
P_{total}	total power consumption
Q	quality factor
$\hat{\mathrm{Q}}$	effective quality factor of the outer-loop path
σ_{J}	normalized clock jitter
σ_{M}	normalized DAC unit element mismatch
T_{LO}	period of the LO signal
T_{S}	period of the sampling clock
T_{D}	delay of the quadrature-path sampling instants in an image-reject frequency-translating $\Delta\Sigma$ modulator
θ_{D}, θ_{U}	phase of the LO signal applied to the downconversion/upconversion mixer in a frequency-translating $\Delta\Sigma$ modulator
θ_{M}	relative LO phase ($\theta_{\mathrm{U}} - \theta_{\mathrm{D}}$)

List of Acronyms

A/D	analog-to-digital
ADC	analog-to-digital converter
CMOS	complementary metal-oxide semiconductor
DAC	digital-to-analog converter
DR	dynamic range
ENOB	effective number of bits
FOM	figure of merit
IF	intermediate frequency
IIT	impulse-invariant transform
IM3	third-order intermodulation distortion
LO	local oscillation
LSB	least significant bit
NRZ	non-return-to-zero
NTF	noise transfer function
OSR	oversampling ratio
PLTI	periodically linear time-invariant
RF	radio frequency
RZ	return-to-zero
SDR	software-defined radio
SNR	signal-to-noise ratio
SNDR	signal-to-noise-and-distortion ratio
SQNR	signal-to-quantization-noise ratio
STF	signal transfer function

Chapter 1

Introduction

THE CURRENT generation of wireless communication devices must support a wide range of services, including cellular, local/wide area networks, and satellite. This requirement is the driving force behind the development of *multi-standard* receivers, which improve power efficiency through reconfigurability. The goal of such receivers is to make all standard-specific parameters programmable, so that the same receiver can be utilized to process any number of communication standards. A receiver that is completely programmable is often referred to as a software-defined radio (SDR) receiver [Mit95].

In general, a reconfigurable system is more efficiently implemented using digital circuitry than analog circuitry. Therefore, a common design objective for multi-standard receivers is to move the analog-to-digital converter (ADC) as close as possible to the antenna. This replaces analog signal processing with equivalent digital signal processing. In order to increase system integration and reduce fabrication costs, these receivers must further be implemented using a nanoscale digital[1] CMOS process. Both of these objectives can be facilitated by digitizing the radio-frequency (RF) input signal at an intermediate frequency (IF) rather than at baseband. A receiver that uses this approach is referred to as a digital-IF receiver [Sal03].

In a conventional digital-IF receiver, the input signal is digitized using a bandpass ADC, which provides high-resolution A/D (analog-to-digital) conversion within a relatively narrow band around a non-zero IF. A type of ADC that can focus its conversion effort in this way is the delta-sigma ($\Delta\Sigma$) ADC [Nor97].

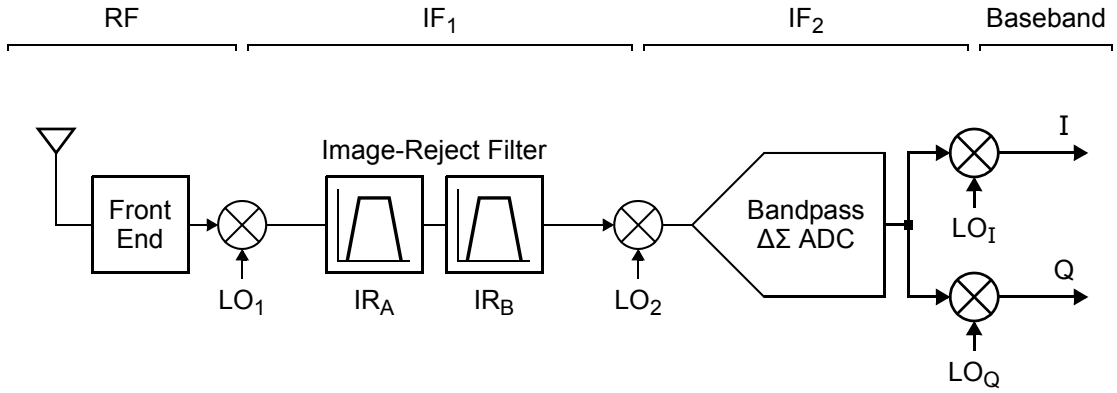
[1]The term *digital* CMOS is used throughout this thesis to refer to a process with no special options.

1.1 Motivation

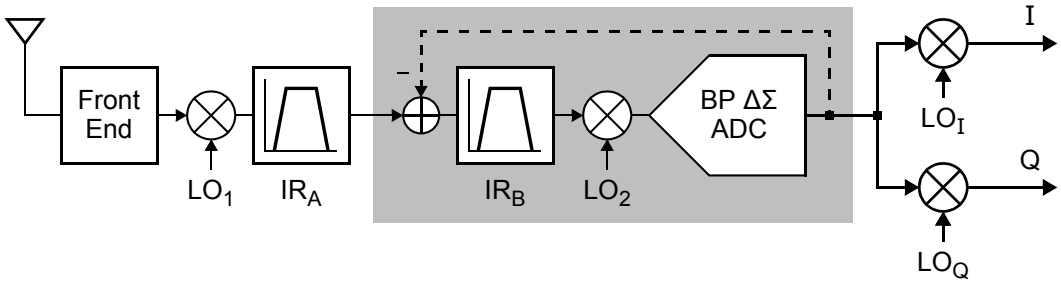
Figure 1.1(a) shows a system diagram for a conventional digital-IF receiver. Here, the input signal is first downconverted to a *high* IF (IF_1), and is then digitized at a *low* IF (IF_2) using a bandpass $\Delta\Sigma$ ADC. A digital-IF architecture replaces the image-reject mixers and baseband filters of a traditional heterodyne receiver with corresponding digital functions, which can be implemented with greater efficiency and accuracy [Raz98]. In addition, due to its increased use of digital processing, a digital-IF receiver can achieve a higher degree of reconfigurability than a heterodyne receiver, while maintaining the same advantages (i.e., high dynamic range and high immunity to interferers).

Figure 1.1(b) shows a block diagram for a corresponding digital-IF receiver that is based on the frequency-translating $\Delta\Sigma$ ADC proposed in this thesis. The proposed ADC combines bandpass A/D conversion with *single-path* downconversion mixing, while providing inherent filtering. In this way, it improves the linearity of the second downconversion mixer (LO_2), as compared to the conventional receiver shown in Figure 1.1(a), and reduces the requirements on the image-reject filter at the first IF (IF_1). Furthermore, it demonstrates a robust and low power CMOS implementation of a high-IF bandpass $\Delta\Sigma$ ADC.

There have been a number of recent examples of CMOS bandpass $\Delta\Sigma$ ADCs that operate on RF, or high-IF input signals by using *conventional* $\Delta\Sigma$ modulator architectures [Ryc10]. However, these bandpass $\Delta\Sigma$ modulators use high sampling rates and high-frequency filters, which can lead to high power consumption and high sensitivity to circuit-level non-idealities. In order to minimize these issues, a bandpass $\Delta\Sigma$ modulator can be designed with frequency downconversion inside its $\Delta\Sigma$ loop [Tao99a][Nam99]. Such architectures, which are referred to here as *downconversion* bandpass $\Delta\Sigma$ modulators, operate on high-frequency input signals, but use low sampling rates and primarily low-frequency filters.



(a)



(b)

Figure 1.1: Block diagrams for: **(a)** a conventional digital-IF receiver, and **(b)** a digital-IF receiver that is based on the frequency-translating $\Delta\Sigma$ ADC proposed in this thesis.

Downconversion bandpass $\Delta\Sigma$ modulators can implement frequency downconversion using mixing [Tao99a] or undersampling [Nam99]. In the literature, an undersampling architecture is referred to as a *subsampling* $\Delta\Sigma$ modulator, whereas a mixing architecture is referred to as a *frequency-translating* $\Delta\Sigma$ modulator.

1.2 Thesis Scope

This thesis investigates ADC architectures for *direct* digitization of high-frequency bandpass signals. It focuses on a particular type of bandpass $\Delta\Sigma$ modulator that uses downconversion mixing in its $\Delta\Sigma$ feedback loop in order to convert a high-frequency analog input signal into a corresponding low-frequency digital output signal. This architecture is generally referred to as the *frequency-translating* $\Delta\Sigma$ modulator.

The thesis first investigates the performance limitations of an existing type of frequency-translating $\Delta\Sigma$ modulator that is based on *image-reject* (quadrature) mixing. It analyses the system architecture of this image-reject frequency-translating $\Delta\Sigma$ modulator, and examines the impact of amplitude, phase, and delay errors in its timing signals, and gain errors in its functional blocks. These errors cause in-phase and quadrature path mismatch, time-variance issues, and system instability. In order to provide a basis for this analysis, this thesis further examines the effect of timing errors in a conventional $\Delta\Sigma$ modulator.

The thesis then investigates the practicality of a novel type of frequency-translating $\Delta\Sigma$ modulator that is based on *single-path* mixing. One of the main advantages of a single-path frequency-translating $\Delta\Sigma$ modulator is that it eliminates path mismatch, which can limit the resolution of an image-reject architecture. Here, specific research objectives are:

1. To investigate whether a single-path frequency-translating $\Delta\Sigma$ modulator can provide sufficient performance to make it a practical ADC architecture for direct digitization of high-frequency bandpass signals.

2. To examine the effect, on the performance of a frequency-translating $\Delta\Sigma$ modulator, of using single-path mixing rather than image-reject mixing.

3. To develop an optimized single-path frequency-translating $\Delta\Sigma$ modulator architecture that achieves low sensitivity both to timing errors, and to the additional mixing terms that are introduced inside its $\Delta\Sigma$ feedback loop.

1.3 Thesis Outline

The outline of this thesis is as follows:

Chapter 2 reviews the fundamental theory of $\Delta\Sigma$ modulation, and provides an overview of important system-level and circuit-level design considerations. It explains the concepts of quantization, oversampling, and noise shaping which, when combined, form the basis for a $\Delta\Sigma$ modulator. It also describes the advantages of discrete-time and continuous-time implementations, presents conventional $\Delta\Sigma$ modulator architectures, and reviews standard performance metrics.

Chapter 2 also presents an overview of downconversion bandpass $\Delta\Sigma$ modulators, and provides a survey of relevant literature. It outlines the advantages of a downconversion bandpass $\Delta\Sigma$ modulator, relative to a conventional architecture, and describes the two different types of downconversion architectures: frequency-translating $\Delta\Sigma$ modulators and subsampling $\Delta\Sigma$ modulators.

Chapter 3 describes the standard synthesis procedure for continuous-time $\Delta\Sigma$ modulators and reviews their primary timing errors, specifically excess loop delay and clock jitter. It then introduces a modeling technique that can be used to rapidly simulate the effect of these errors on the performance of a continuous-time $\Delta\Sigma$ modulator. The accuracy and speed of the presented modeling technique are demonstrated using a behavioural model that was developed in Simulink. The presented technique is then used to evaluate the clock-jitter sensitivity of various continuous-time $\Delta\Sigma$ modulators.

Chapter 4 investigates an existing type of frequency-translating $\Delta\Sigma$ modulator, which is based on *image-reject* mixing. It describes a synthesis procedure for the image-reject frequency-translating $\Delta\Sigma$ modulator, and derives a set of system-level constraints that must be satisfied to achieve this synthesis. This chapter also examines the performance limitations of the image-reject architecture, in particular its sensitivity to in-phase and quadrature path mismatch.

Chapter 5 introduces a novel type of frequency-translating $\Delta\Sigma$ modulator, which is based on *single-path* mixing. It presents a synthesis procedure for the single-path frequency-translating $\Delta\Sigma$ modulator, and develops a set of system-level constraints that must be satisfied to achieve this synthesis. This chapter also proposes several design techniques that can be used to improve the performance of a single-path architecture.

Chapter 6 presents the system architecture for an experimental frequency-translating $\Delta\Sigma$ modulator that is used to validate the synthesis procedure and design techniques that are described in Chapter 5. This chapter provides a complete set of design equations, and presents behavioural simulation results that demonstrate the ideal performance of the experimental $\Delta\Sigma$ modulator, as well as the effect of circuit non-idealities.

Chapter 7 presents the circuit-level implementation of the experimental $\Delta\Sigma$ modulator in a standard 1-V 65-nm CMOS process.

Chapter 8 presents the measured performance of the experimental $\Delta\Sigma$ modulator and then compares these results to state-of-the-art bandpass $\Delta\Sigma$ modulators.

Chapter 9 provides a summary of this thesis, as well as suggestions for future research.

Chapter 2

Bandpass $\Delta\Sigma$ Modulation

Delta-sigma ($\Delta\Sigma$) modulation is a popular technique for medium-to-high resolution analog-to-digital conversion of low-to-medium bandwidth signals. The $\Delta\Sigma$ modulator combines oversampling and feedback to improve the resolution of a coarse quantizer inside a relatively narrow bandwidth. It trades resolution in amplitude for resolution in time, which enables it to shift complexity from the analog domain into the digital domain. This reduces its sensitivity to analog component matching and amplifier gains, and makes it particularly suited to modern low-voltage nanoscale CMOS technologies [Joh97]. An additional advantage of $\Delta\Sigma$ modulators is that, through oversampling, they reduce the design requirements on the anti-aliasing filter at the input of an ADC.

This chapter reviews the fundamental theory of $\Delta\Sigma$ modulation and provides a summary of important system-level and circuit-level considerations. Section 2.1 explains quantization, oversampling, and noise shaping, which form the basis for a $\Delta\Sigma$ modulator. It then compares the advantages of discrete-time and continuous-time circuit implementations, and presents a number of conventional architectures. Section 2.2 reviews standard performance metrics for a $\Delta\Sigma$ modulator, focusing on bandpass architectures.

This chapter also provides an overview of downconversion bandpass $\Delta\Sigma$ modulators, and presents a survey of relevant literature. Section 2.3 describes the basic system architecture of the downconversion bandpass $\Delta\Sigma$ modulator and summarizes its advantages as compared to a conventional architecture. It then examines the two different downconversion architectures: subsampling $\Delta\Sigma$ modulators and frequency-translating $\Delta\Sigma$ modulators, which are based on undersampling and mixing, respectively.

2.1 Fundamentals of ΔΣ Modulation

This section reviews the fundamental theory of delta-sigma (ΔΣ) modulation. Section 2.1.1 outlines the concepts of quantization, oversampling, and noise shaping, which form the basis for a ΔΣ modulator. Sections 2.1.2 and 2.1.3 then discuss discrete-time and continuous-time circuit implementations, and compare standard architectures.

2.1.1 Operating Principles

This section presents the linear model for a uniform quantizer, and then uses this model to demonstrate the advantages of oversampling and noise shaping.

Quantization

Quantization is the process of converting a signal that has *infinite* amplitude resolution into a corresponding signal that has *finite* amplitude resolution. It is implemented using a *quantizer*, which generally operates with a uniform step size and a fixed sampling rate.

Figure 2.1(a) plots the input-output transfer characteristic of a uniform mid-rise quantizer that has B quantization bits. Here, the step size is defined as

$$\Delta \;=\; \frac{2V_{\mathrm{REF}}}{2^B - 1} \tag{2.1}$$

where V_{REF} is the reference level of the quantizer, and $2V_{\mathrm{REF}}$ is the full-scale range. The step size corresponds to the least significant bit (LSB) of the quantizer.

A quantizer introduces a deterministic error, which can be defined as

$$q(n) \;=\; y(n) - x_q(n) \tag{2.2}$$

Here, $x_q(n)$ and $y(n)$ represent the input and output signals, respectively. Figure 2.1(b) plots the quantization error $q(n)$ of the transfer characteristic in Figure 2.1(a) as a function of the input-signal amplitude. For an input signal between $\pm\,(V_{\mathrm{REF}} + \Delta/2)$, the error $q(n)$ is limited to $\pm\,\Delta/2$. This is referred to as the no-overload range of the quantizer, and $V_{\mathrm{OL}} \equiv V_{\mathrm{REF}} + \Delta/2$ is referred to as its *overload level*.

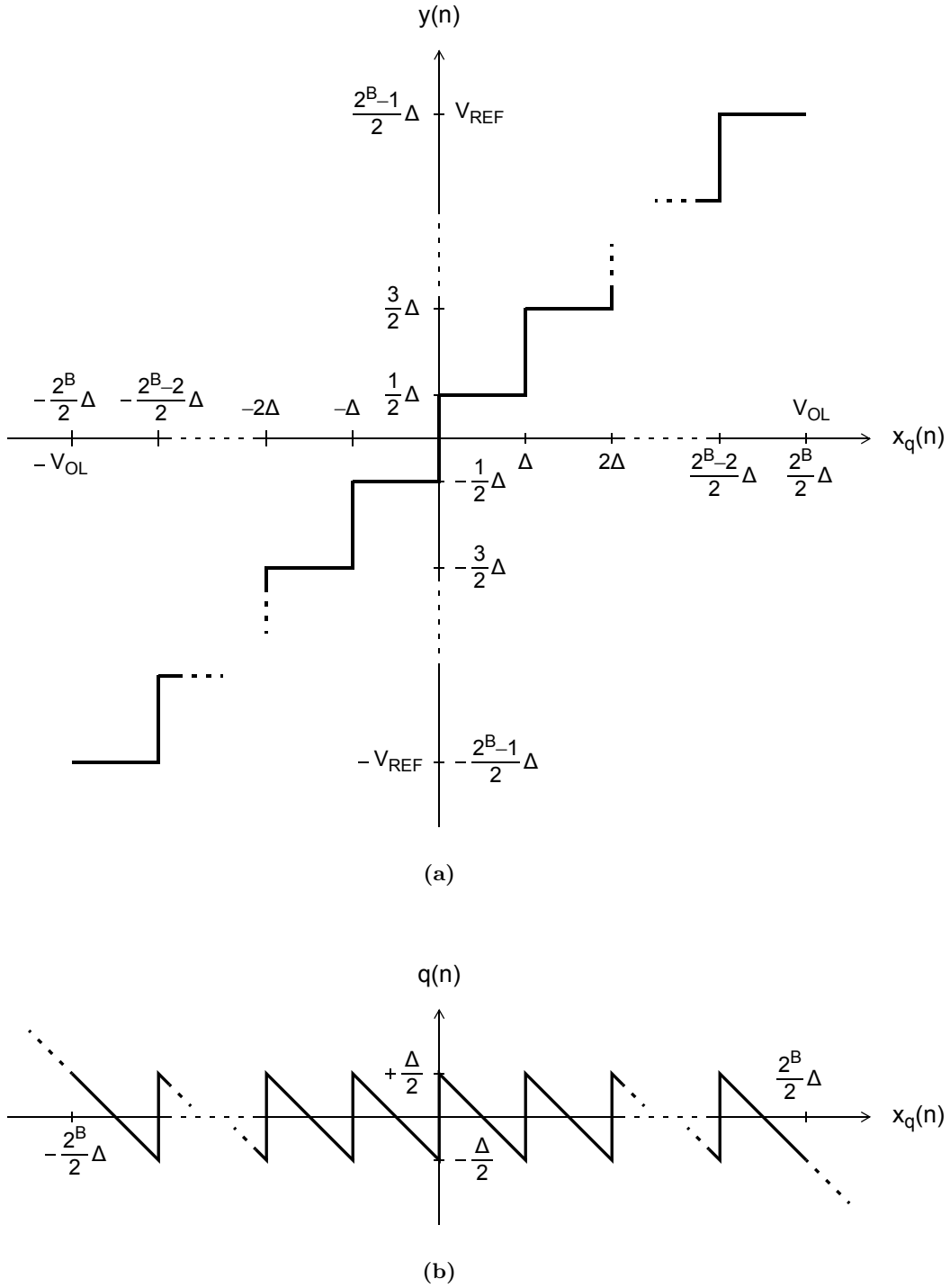


Figure 2.1: (a) The transfer characteristic of a uniform mid-rise quantizer that is designed with B quantization bits [Ham04], and **(b)** its associated quantization error.

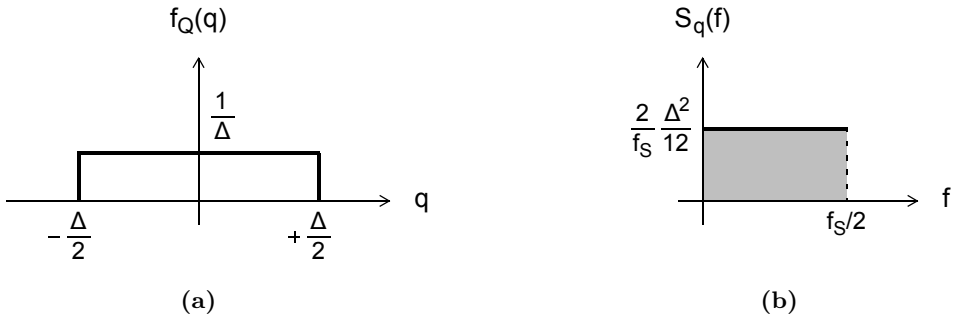


Figure 2.2: (a) The probability density function of the quantization error, and **(b)** its single-sided power spectral density under the additive white noise approximation.

If the sample-to-sample variation of the input signal $x_q(n)$ is sufficiently large, and it does not exceed the overload level of the quantizer, the resulting quantization errors $q(n)$ have an approximately uniform distribution between $\pm\,\Delta/2$. As a result, each $q(n)$ can be represented as a random variable with a uniform probability density function [Gra90]. Figure 2.2(a) plots the probability density function $f_Q(q)$ of this random variable, where its mean and variance can be derived as

$$\mu_Q \;=\; \int_{-\infty}^{\infty} q\, f_Q(q)\, \mathrm{d}q \;=\; \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q\, \mathrm{d}q \;=\; 0 \tag{2.3}$$

$$\sigma_Q^2 \;=\; \int_{-\infty}^{\infty} q^2 f_Q(q)\, \mathrm{d}q \;=\; \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2\, \mathrm{d}q \;=\; \frac{\Delta^2}{12} \tag{2.4}$$

The sequence of quantization errors $q(n)$ can be approximated as a random process with a white power spectral density [Gra90]. This *additive white noise approximation* models $q(n)$ as a set of independent and identically-distributed random variables that are independent of the input signal $x_q(n)$. The distribution of each $q(n)$ corresponds to $f_Q(q)$, and the total rms power (P_q) corresponds to σ_Q^2. This approximation replaces a deterministic non-linear block, the quantizer, with a stochastic linear block, where the corresponding quantization errors are referred to as *quantization noise*.

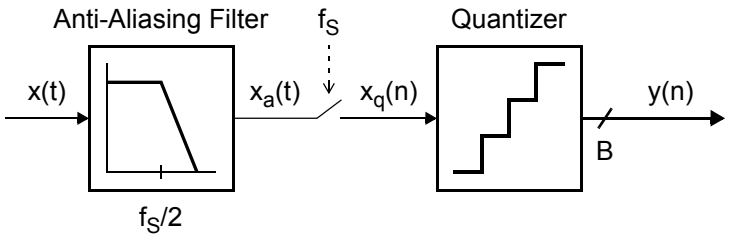


Figure 2.3: Block diagram for a Nyquist-rate ADC.

In a quantizer that satisfies the additive white noise approximation, the quantization noise power (P_q) is spread over the frequency range $[\,0\,,\,f_{\rm S}/2\,]$, where $f_{\rm S}$ is the sampling frequency of the quantizer. The corresponding power spectral density is equal to

$$S_q(f) \;=\; \frac{P_q}{f_{\rm S}/2} \;=\; \frac{2}{f_{\rm S}}\frac{\Delta^2}{12} \qquad ({\rm V}^2/{\rm Hz}) \tag{2.5}$$

where $S_q(f)$ is plotted in Figure 2.2(b).

Figure 2.3 shows a general block diagram for a Nyquist-rate ADC, which is composed of a quantizer, a sampler, and an *anti-aliasing* filter. The anti-aliasing filter is used to attenuate spectral components of the input signal above $f_{\rm S}/2$. These components *alias* into the Nyquist band $[\,0\,,\,f_{\rm S}/2\,]$ during sampling, causing *aliasing distortion*. Note that the anti-aliasing filter of a Nyquist-rate ADC ideally requires a zero-width transition band.

The peak signal-to-quantization noise ratio (SQNR) of an ideal ADC can be derived using a full-scale sinusoidal input signal. For the quantizer in Figure 2.1(a), a full-scale input signal has an amplitude equal to the overload level ($V_{\rm OL}$), and an rms power equal to

$$P_s \;=\; \frac{V_{\rm OL}^2}{2} \;=\; 2^{\,2B}\frac{\Delta^2}{8} \tag{2.6}$$

Using Equation (2.6), the peak SQNR of a Nyquist-rate ADC can be expressed as

$$\text{SQNR} \;=\; 10\log_{10}\!\left(\frac{P_s}{P_q}\right) \;=\; 10\log_{10}\!\left(\frac{3}{2}\,2^{\,2B}\right) \tag{2.7}$$

Therefore, each additional quantization bit B results in a 6 dB increase in SQNR.

Oversampling

The effective resolution of a quantizer can be improved by operating at a sampling frequency that is higher than the Nyquist frequency of its input signal. This technique is referred to as *oversampling* [Joh97].

In a quantizer that satisfies the additive white noise approximation, the total quantization noise power (P_q) is spread evenly over the Nyquist band $[\,0, f_S/2\,]$. Therefore, by oversampling the input signal, the fraction of P_q that is contained within its signal band[1] $[\,0, f_B\,]$ is reduced by a factor referred to as the *oversampling ratio* (OSR), where

$$\mathrm{OSR} \equiv \frac{f_S}{f_N} = \frac{f_S}{2f_B} \tag{2.8}$$

Here, f_B and f_N denote the bandwidth and Nyquist frequency of the input signal. Figure 2.4 illustrates the effect of oversampling on the in-band quantization noise.

In an oversampled system, the transition band of the anti-aliasing filter can span from f_B to $f_S - f_B$, since signals in this range do not fold into the signal band $[\,0, f_B\,]$ during sampling. This reduces the requirements on the anti-aliasing filter in an oversampling ADC, relative to a Nyquist-rate ADC. The remaining out-of-band signals $[\,f_B, f_S/2\,]$ are filtered at the output of the quantizer using a *decimation* filter, which also downsamples the corresponding digital signal by the OSR. Figure 2.5 shows a block diagram for an oversampling ADC.

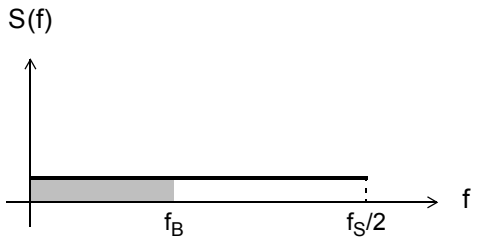


Figure 2.4: Power spectral density of the quantization error in an oversampling ADC.

[1] This result is valid independent of the position of the signal band within the Nyquist band.

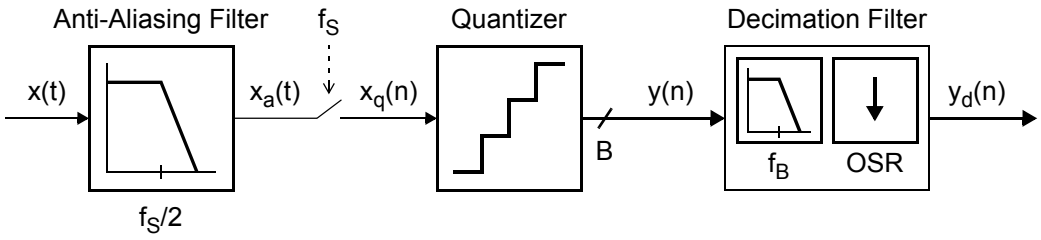


Figure 2.5: Block diagram for an oversampling ADC.

For an oversampling ratio of OSR, the in-band quantization noise power is reduced to

$$P_{q,\,\mathrm{B}} \;=\; \int_0^{f_\mathrm{B}} S_q(f)\,\mathrm{d}f \;=\; \int_0^{f_\mathrm{B}} \frac{2}{f_\mathrm{S}}\frac{\Delta^2}{12}\,\mathrm{d}f \;=\; \frac{1}{\mathrm{OSR}}\,\frac{\Delta^2}{12} \tag{2.9}$$

where $S_q(f)$ is derived in Equation (2.5). Using Equations (2.6) and (2.9), the peak SQNR of an oversampling ADC can be expressed as

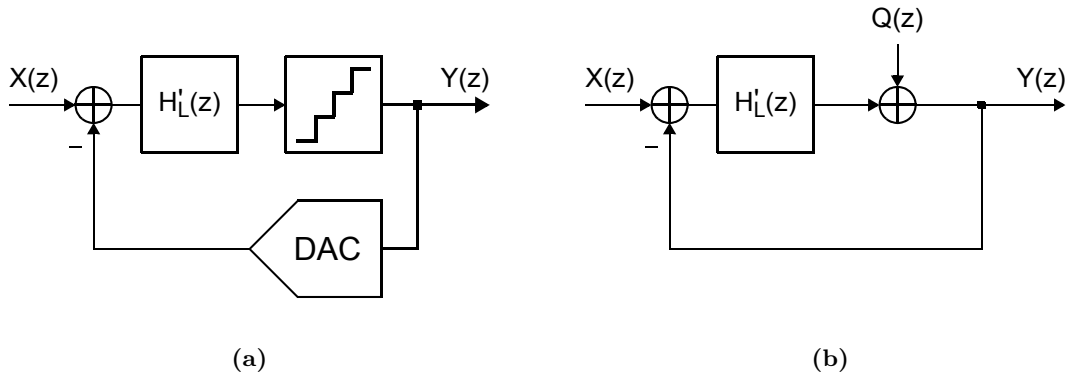
$$\mathrm{SQNR} \;=\; 10\log_{10}\!\left(\frac{P_s}{P_{q,\,\mathrm{B}}}\right) \;=\; 10\log_{10}\!\left(\frac{3}{2}\,2^{2B}\right) + 10\log_{10}(\mathrm{OSR}) \tag{2.10}$$

Therefore, each doubling of the OSR results in a 3 dB increase in SQNR.

Noise Shaping

The effective resolution of an oversampled quantizer can be further improved by placing it in negative feedback with a *loop filter*, as shown in Figure 2.6(a). This configuration is referred to as a delta-sigma (ΔΣ) modulator [Nor97].

In a ΔΣ modulator, the loop filter suppresses quantization errors inside the signal band, due to the feedback loop. This technique is referred to as *noise shaping*. Figure 2.7 illustrates the effect of noise shaping on the in-band quantization noise. The noise-shaping performance of a ΔΣ modulator can be evaluated using the *linear model* that is shown in Figure 2.6(b). Here, quantization errors are modelled by an additive white noise source $Q(z)$.



(a) **(b)**

Figure 2.6: Block diagrams for: **(a)** a ΔΣ modulator, and **(b)** its linear model.

The output of the linear model can be expressed as

$$Y(z) \equiv \mathrm{STF}(z)\,X(z) + \mathrm{NTF}(z)\,Q(z) \tag{2.11}$$

where the *noise transfer function* (NTF) and *signal transfer function* (STF) are defined as

$$\mathrm{NTF}(z) \equiv \left.\frac{Y(z)}{Q(z)}\right|_{X(z)=0} = \frac{1}{1+H'_{\mathrm{L}}(z)} \tag{2.12}$$

$$\mathrm{STF}(z) \equiv \left.\frac{Y(z)}{X(z)}\right|_{Q(z)=0} = \frac{H'_{\mathrm{L}}(z)}{1+H'_{\mathrm{L}}(z)} \tag{2.13}$$

As indicated in Equation (2.12), the zeros of the noise transfer function $\mathrm{NTF}(z)$ are set by the poles of the loop filter $H'_{\mathrm{L}}(z)$ or, equivalently, $\mathrm{NTF}(z)$ tends to zero at frequencies where $H'_{\mathrm{L}}(z)$ tends to infinity. Therefore, in order to suppress quantization errors, $H'_{\mathrm{L}}(z)$ must have a high gain over the required signal band, so that $\mathrm{NTF}(z)$ is approximately zero and $\mathrm{STF}(z)$ is approximately unity. In this way, quantization errors are significantly reduced, whereas the input signal is largely unaffected.

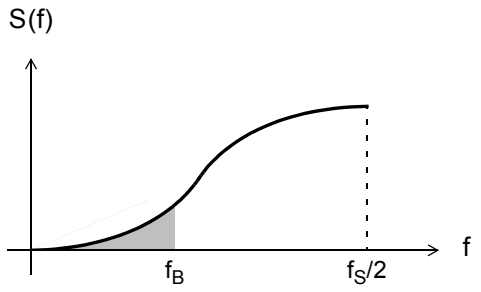


Figure 2.7: Power spectral density of the quantization error in a noise-shaping ADC.

Figure 2.8 shows a block diagram for a ΔΣ ADC, which is composed of a ΔΣ modulator, an anti-aliasing filter, a sampler, and a decimation filter. In order to achieve first-order noise shaping, the loop filter $H'_{\mathrm{L}}(z)$ of the ΔΣ modulator can be implemented using a discrete-time integrator, which results in an STF and NTF of

$$\mathrm{STF}(z) \;=\; z^{-1} \quad \text{and} \quad \mathrm{NTF}(z) \;=\; 1 - z^{-1} \tag{2.14}$$

Note that NTF(z) has a zero at dc (i.e., $z = 1$), and a pole at the origin (i.e., $z = 0$). This corresponds to *highpass* noise shaping of quantization errors.

For an oversampling ratio of OSR, the in-band quantization noise power[2] of a first-order lowpass ΔΣ ADC is reduced to

$$P_{q,\,\mathrm{B}} \;=\; \int_0^{f_{\mathrm{B}}} |\mathrm{NTF}(f)|^2\, S_q(f)\,\mathrm{d}f \;=\; \int_0^{f_{\mathrm{B}}} 4\sin^2\!\left(\frac{\pi f}{f_{\mathrm{S}}}\right)\frac{2}{f_{\mathrm{S}}}\frac{\Delta^2}{12}\,\mathrm{d}f \;\cong\; \frac{1}{\mathrm{OSR}^3}\,\frac{\pi^2}{3}\,\frac{\Delta^2}{12} \tag{2.15}$$

where $S_q(f)$ is given in Equation (2.5). Using Equations (2.6) and (2.15), the peak SQNR of a first-order lowpass ΔΣ ADC can be expressed as

$$\mathrm{SQNR} \;=\; 10\log_{10}\!\left(\frac{P_s}{P_{q,\,\mathrm{B}}}\right) \;=\; 10\log_{10}\!\left(\frac{3}{2}\,2^{2B}\right) + 10\log_{10}\!\left(\frac{3}{\pi^2}\,\mathrm{OSR}^3\right) \tag{2.16}$$

Therefore, each doubling of the OSR results in a 9 dB increase in SQNR.

[2]This derivation assumes a high OSR, so that $\sin(\pi f/f_{\mathrm{S}}) \cong \pi f/f_{\mathrm{S}}$ [Ort06].

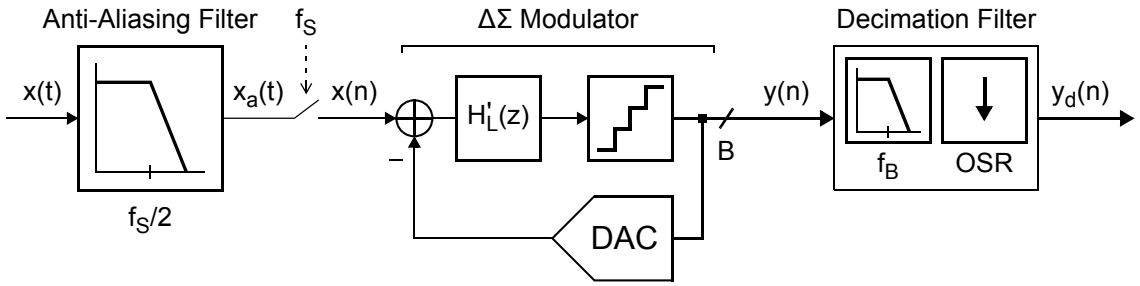


Figure 2.8: Block diagram for a ΔΣ ADC.

The loop filter of a ΔΣ modulator can be designed with a lowpass, bandpass, or complex-bandpass filtering characteristic, as described below.

Lowpass

In a lowpass ΔΣ modulator [Can85][Zwa96], quantization noise is suppressed inside a narrow band around dc. A lowpass loop filter is implemented using a cascade[3] of *integrators*, where each integrator introduces an NTF zero at dc. The signal band of a lowpass ΔΣ modulator is defined over $[\,0, f_{\mathrm{B}}\,]$, and its OSR is defined as in Equation (2.8).

Bandpass

In a bandpass ΔΣ modulator [Gai89][Sch89][Jan93], quantization noise is suppressed inside a narrow band around a non-zero centre frequency (f_{C}). A bandpass loop filter is implemented using a cascade of *resonators*, where each resonator introduces a pair of complex-conjugate zeros into the NTF. Therefore, a bandpass ΔΣ modulator of order $2N$ provides N zeros over its signal band, and requires $2N$ amplifiers. The signal band of a bandpass ΔΣ modulator is defined over $[\,f_{\mathrm{C}}-f_{\mathrm{B}}/2, f_{\mathrm{C}}+f_{\mathrm{B}}/2\,]$, and its OSR is defined as in Equation (2.8).

Bandpass ΔΣ modulators provide a number of advantages over lowpass ΔΣ modulators, including improved efficiency for bandpass signals, and reduced sensitivity to low-frequency signal impairments, such as flicker noise and dc offsets. In addition, bandpass ΔΣ modulators facilitate a shift of analog baseband processing into the digital domain [Jan93].

[3] A lowpass loop filter can also use resonators to spread the NTF zeros over the signal band [Lee87].

Complex-Bandpass[4]

In a complex-bandpass ΔΣ modulator [Jan94][Jan97], quantization noise is suppressed inside a narrow band around a non-zero centre frequency (f_C), similar to the bandpass architecture, however the noise-shaping characteristic is *asymmetric* around dc. A complex-bandpass loop filter is split into in-phase and quadrature signal paths, and is implemented using a cascade of *complex resonators*. A complex-bandpass ΔΣ modulator of order N provides N zeros over its signal band, however it still requires $2N$ amplifiers.

The signal band of a complex-bandpass ΔΣ modulator is defined in the same way as that of a bandpass ΔΣ modulator. However, since the Nyquist band of a complex system is double that of a real system, the OSR of a complex-bandpass ΔΣ modulator is twice as high as that of a lowpass or bandpass ΔΣ modulator [Sch06a]. A disadvantage of complex architectures is that they are sensitive to mismatch between their in-phase and quadrature paths. The effect of this mismatch is generally reduced by placing one of the NTF zeros in the image band of the ΔΣ modulator.

2.1.2 Loop-Filter Implementations

The loop filter of a ΔΣ modulator can be implemented using a *discrete-time* circuit topology or a *continuous-time* circuit topology. The primary difference between these implementations is the position of the sampling operation.

Figure 2.9(a) shows a block diagram for a discrete-time ΔΣ modulator. Here, the sampler is placed at the input of the ΔΣ modulator, and the loop filter $H'_L(z)$ is implemented using a discrete-time circuit topology (e.g., switched-capacitor, or switched-current). Figure 2.9(b) shows a block diagram for a continuous-time ΔΣ modulator. Here, the sampler is placed at the input of the quantizer, and the loop filter $H_L(s)$ is implemented using a continuous-time circuit topology (e.g., active-RC, gm-C, or LC). This section reviews the advantages and the disadvantages of discrete-time and continuous-time ΔΣ modulators, and discusses sampling issues, loop-filter issues, and matching issues.

[4]This architecture is sometimes referred to as a *quadrature-bandpass* ΔΣ modulator in the literature.

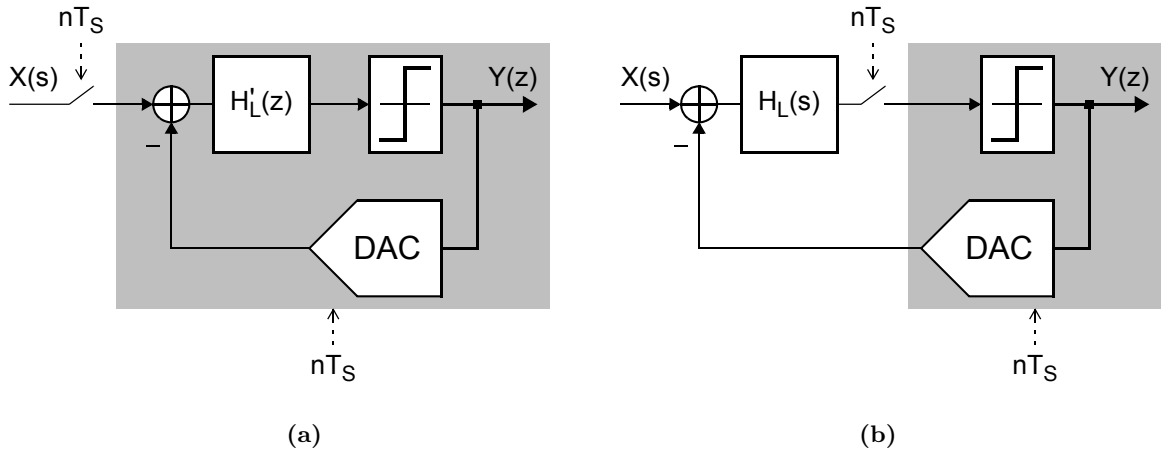


Figure 2.9: Block diagrams for: **(a)** a discrete-time ΔΣ modulator, and **(b)** a continuous-time ΔΣ modulator. Here, T_S represents the sampling period.

Sampling Issues

In a discrete-time ΔΣ modulator, sampling takes place immediately at the input. As a result, sampling errors that are introduced by switch non-linearity and clock jitter are added to the input signal, and can limit the resolution [Zwa96]. Note that once the input signal is sampled, it is effectively insensitive to timing errors. An additional disadvantage of a discrete-time loop filter is that the thermal noise introduced by the switches and operational amplifiers in each stage, and at the input, is folded into the signal band and increases the noise floor.

In a continuous-time ΔΣ modulator, sampling takes place at the output of the loop filter. As a result, sampling errors are suppressed by the gain of the loop filter and do not generally affect the performance. An additional advantage of sampling inside the ΔΣ loop is that the STF provides inherent filtering, which can be used to replace the external anti-aliasing filter, as outlined in Section 2.1.3. The primary disadvantage of sampling inside the ΔΣ loop is that the feedback path of the ΔΣ modulator must convert the discrete-time output signal into a corresponding continuous-time signal. The timing errors that are introduced by this process are added directly to the input of the ΔΣ modulator, and can therefore limit its resolution, as described in Section 3.2.

Loop-Filter Issues

The loop filter of a discrete-time ΔΣ modulator is normally implemented using a cascade of switched-capacitor integrators. The noise-shaping performance of a switched-capacitor filter is often limited by the settling accuracy of its operational amplifiers. The amplifier unity-gain frequency must generally be 3–5 times higher than the sampling frequency in order to achieve the required settling accuracy [Ort06]. This imposes a lower limit on the power consumption of a discrete-time ΔΣ modulator, and an upper limit on its sampling frequency.

The loop filter of a continuous-time ΔΣ modulator is normally designed using a cascade of active-RC or gm-C integrators. The noise-shaping performance of a continuous-time filter is often limited either by its linearity or its coefficient mismatch. The unity-gain frequencies of its amplifiers are generally only required to be 1–2 times higher than the sampling frequency in order to provide adequate gain across the signal band [Ort06]. As a result, continuous-time ΔΣ modulators can use higher sampling frequencies than discrete-time ΔΣ modulators, and can also achieve lower power consumption.

Matching Issues

The loop-filter coefficients of a discrete-time ΔΣ modulator are set using a ratio of similar circuit elements (i.e., capacitors). Therefore, the accuracy of a discrete-time loop filter is only limited by the *relative* component matching of a given technology, which is typically on the order of 0.1 % for integrated capacitors. As a result, discrete-time ΔΣ modulators implement highly-accurate loop filters that are robust to process variations.

The loop-filter coefficients of a continuous-time ΔΣ modulator are set by the product of dissimilar circuit elements (e.g., capacitors and resistors or transconductors). Therefore, the accuracy of a continuous-time loop filter is limited by the *absolute* component tolerances of a given technology, which are on the order of 10–20 % for integrated capacitors and resistors. As a result, continuous-time ΔΣ modulators generally require some form of tuning to correct for process variations.

2.1.3 High-Order ΔΣ Modulators

This section reviews the primary design considerations for the loop filter of a high-order ΔΣ modulator, focusing on continuous-time circuit implementations. It discusses the properties of the noise transfer function (NTF) and the signal transfer function (STF), and outlines the advantages and disadvantages of different loop-filter topologies.

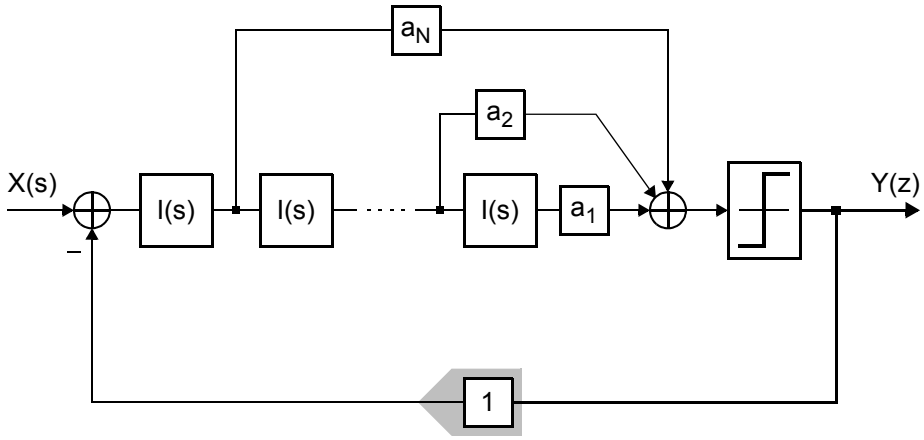
Noise Transfer Function

In a high-order ΔΣ modulator, the positions of the NTF zeros and poles determine both the noise-shaping performance and the maximum input signal.

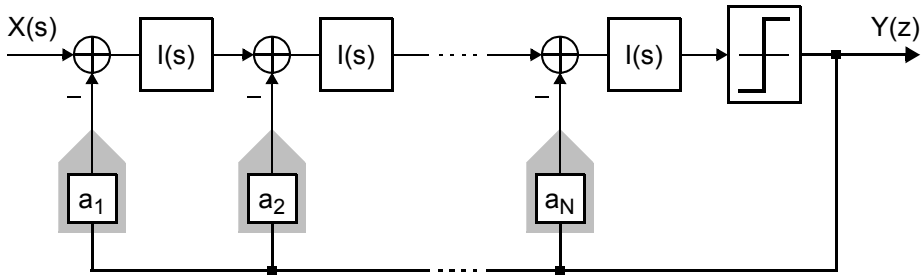
The *zeros* of the NTF are set by the functional blocks (i.e., integrators, resonators) of the loop filter: an integrator introduces a real zero at dc, whereas a resonator introduces a pair of complex-conjugate zeros at a non-zero centre frequency. The zeros of the NTF are generally spread over the signal band to improve the noise-shaping performance. Use of this technique is particularly important in a wideband ΔΣ modulator [Sch93].

The *poles* of the NTF are set by the coefficient paths of the loop filter. In a high-order ΔΣ modulator, the noise-shaping performance depends primarily on the *out-of-band gain*[5] of the NTF. For a given loop-filter order, increasing the out-of-band gain improves the noise-shaping performance, however it also increases the magnitude of the out-of-band quantization noise, and therefore limits the maximum signal amplitude that can be adequately processed by the ΔΣ modulator [Sch05]. Note that this increase in the quantization noise can be counteracted by using a multi-bit quantizer. The out-of-band gain of the NTF can be increased by moving its poles closer to the origin (i.e., $|z| = 0$). When all of its poles are positioned at the origin, the NTF has a finite impulse response, and achieves the maximum noise-shaping performance for a given loop-filter order.

[5]For a maximally-flat NTF, the *out-of-band gain* refers to the magnitude of the NTF at $f_S/2$. The out-of-band gain is sometimes denoted as $\|H\|_\infty$, which represents the *infinity norm*.



(a)



(b)

Figure 2.10: Block diagrams for: **(a)** a feedforward loop-filter topology, and **(b)** a feedback loop-filter topology. Here, $I(s)$ represents the transfer function of a continuous-time integrator.

Loop-Filter Topology

The loop filter of a high-order ΔΣ modulator can be designed with feedback coefficient paths, feedforward coefficient paths, or a combination of both. Figure 2.10 provides block diagrams for continuous-time ΔΣ modulators that are designed with strictly-feedforward and strictly-feedback loop-filter topologies. Both of these loop-filter topologies implement the same NTF, however each has different advantages and disadvantages.

In a strictly-feedback topology, sometimes referred to as *distributed feedback*, the feedback signal is subtracted from the input signal of each integrator. The result of each subtraction is reduced by the loop gain, due to feedback, and therefore each integrator must regenerate the full-scale input signal at its output. This can impose significant requirements on the linearity of each integrator, in particular on the first stage of the loop filter. The linearity requirements can be reduced by decreasing the feedback coefficients, however this increases the circuit noise contribution. The primary advantage of a feedback topology is that it improves the inherent anti-alias filtering in a continuous-time implementation.

In a strictly-feedforward topology, sometimes called *weighted feedforward summation*, the output of each integrator is summed at the input of the quantizer. The primary advantage of a feedforward topology is that it does not need to regenerate the input signal at the output of each integrator, which reduces its linearity requirements relative to a feedback topology. The primary disadvantages of a feedforward topology are that it requires an additional summing amplifier at the input of the quantizer, and that its associated STF contains peaking at high frequencies, as described next.

Signal Transfer Function

The STF of a continuous-time ΔΣ modulator provides significant attenuation of interferers around aliases of its signal band. This is referred to as the *inherent anti-aliasing* property of the continuous-time ΔΣ modulator [Can85][Sho95a] and is present in lowpass, bandpass, and complex-bandpass architectures. The filtering characteristic of the STF differs depending on whether the loop filter is implemented using a feedforward or feedback topology.

Figure 2.11(a) plots the STF of a 4th-order bandpass ΔΣ modulator that is implemented using a *feedback* loop-filter topology. Here, the STF has notches at aliases of the signal band, and its filtering characteristic has an Nth-order roll-off. Accordingly, it provides significant attenuation of out-of-band interferers [Bre01].

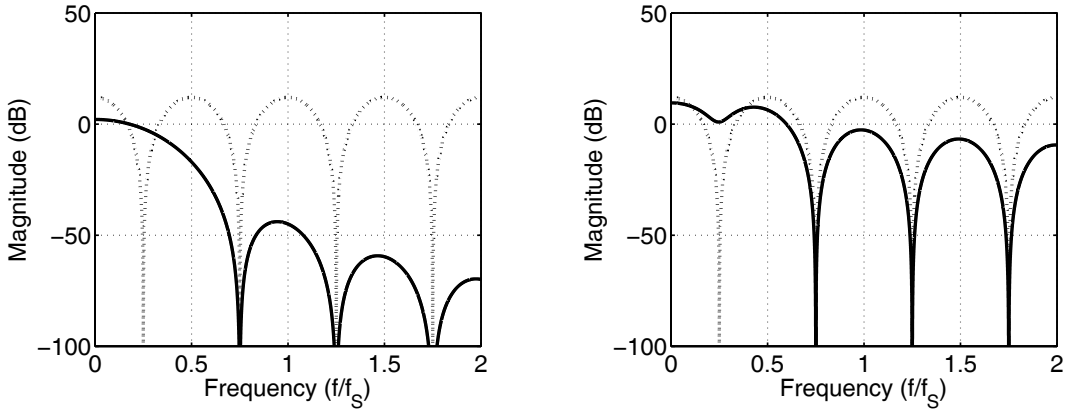


Figure 2.11: Simulated STF and NTF of a 4th-order bandpass $\Delta\Sigma$ modulator with: **(a)** a feedback loop-filter topology, and **(b)** a feedforward loop-filter topology. Here, the signal band of the bandpass $\Delta\Sigma$ modulator is centred at $1/4f_S$. (STF — and NTF $\cdots$)

Figure 2.11(b) plots the STF of a 4th-order bandpass $\Delta\Sigma$ modulator that is implemented using an equivalent *feedforward* loop-filter topology. Here, the STF has notches at aliases of the signal band, similar to a feedback topology, however its filtering characteristic only has a 1st-order roll-off. Accordingly, it provides limited attenuation of out-of-band interferers, and also has peaking that can amplify interferers [Bre01].

2.2 Performance Metrics

This section reviews the various metrics that are used in this thesis to evaluate and compare the performance of different bandpass $\Delta\Sigma$ ADCs. Note that the performance of a $\Delta\Sigma$ ADC is generally characterized using dynamic metrics (e.g., signal-to-noise ratio, dynamic range), rather than static metrics (e.g., offset, integral non-linearity).

Signal-to-Quantization-Noise Ratio

The signal-to-quantization-noise ratio (SQNR) is the ratio of the input-signal power (P_s) to the quantization noise power within the signal band ($P_{q,\,\mathrm{B}}$). It is expressed as

$$\mathrm{SQNR} \;\equiv\; 10\log_{10}\!\left(\frac{P_s}{P_{q,\,\mathrm{B}}}\right) \qquad (\mathrm{dB}) \tag{2.17}$$

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of the input-signal power (P_s) to the total noise power within the signal band ($P_{n,\,\mathrm{B}}$). It is expressed as

$$\mathrm{SNR} \;\equiv\; 10\log_{10}\!\left(\frac{P_s}{P_{n,\,\mathrm{B}}}\right) \qquad (\mathrm{dB}) \tag{2.18}$$

where P_n includes quantization noise and circuit noise (e.g., thermal noise, flicker noise), as well as noise introduced by clock jitter and other sources.

Signal-to-Noise-and-Distortion Ratio

The signal-to-noise-and-distortion ratio (SNDR) is the ratio of the input-signal power (P_s) to the sum of the noise power ($P_{n,\,\mathrm{B}}$) and the distortion power (P_d). It is expressed as

$$\mathrm{SNDR} \;\equiv\; 10\log_{10}\!\left(\frac{P_s}{P_{n,\,\mathrm{B}} + P_d}\right) \qquad (\mathrm{dB}) \tag{2.19}$$

Effective Number of Bits

The effective number of bits (ENOB) is an alternative expression for the peak SNDR. The ENOB represents the number of quantization bits would be required to achieve the specified peak SNDR in a corresponding Nyquist-rate ADC. It is expressed as

$$\mathrm{ENOB} \;\equiv\; \frac{\mathrm{SNDR}_{\mathrm{peak}} - 1.76}{6.02} \qquad (\mathrm{bits}) \tag{2.20}$$

Dynamic Range

The dynamic range (DR) is the ratio of the power ($P_{s,\,\max}$) of the maximum input signal to the power ($P_{s,\,\min}$) of the minimum input signal. It is expressed as

$$\mathrm{DR} \;\equiv\; 10\log_{10}\!\left(\frac{P_{s,\,\max}}{P_{s,\,\min}}\right) \qquad (\mathrm{dB}) \tag{2.21}$$

where $P_{s,\,\min}$ is the input-signal power that corresponds to an SNR of 0 dB, and $P_{s,\,\max}$ is the input-signal power that causes the SNR to drop by 3 dB from its peak value.

Intermodulation Distortion

The linearity of a bandpass ADC is generally evaluated using a two-tone input signal, which results in intermodulation distortion. The third-order intermodulation distortion (IM3) is the ratio of the power (P_t) of one tone of the input signal to the power ($P_{d,\,3}$) of the third-order distortion product. It is expressed as

$$\mathrm{IM3} \;\equiv\; 10\log_{10}\!\left(\frac{P_t}{P_{d,\,3}}\right) \qquad (\mathrm{dBc}) \tag{2.22}$$

where dBc denotes dB relative to the carrier.

Figure of Merit

A figure of merit (FOM) combines the relevant performance metrics of an ADC into a single expression, which is then used for comparison with different ADCs. In this thesis, ADCs are compared in terms of their energy efficiency. This FOM can be expressed as

$$\mathrm{FOM} \;\equiv\; \frac{P_{\mathrm{total}}}{2^{\,\mathrm{ENOB}}\cdot 2f_{\mathrm{B}}} \qquad (\mathrm{pJ/step}) \tag{2.23}$$

where P_{total} is the total power consumption of the ADC, and f_{B} is its signal bandwidth.

2.3 Downconversion Bandpass ΔΣ Modulators

In the past, the use of bandpass ΔΣ modulation was limited to low-frequency[6] input signals in CMOS technologies. Recently, owing to the high intrinsic bandwidths of MOS transistors in modern nanoscale technologies, bandpass ΔΣ modulators have been reported with centre frequencies above 1 GHz [Ryc10]. However, these *conventional* bandpass ΔΣ modulators use high sampling rates and multiple high-frequency resonators, which can result in high power consumption and high sensitivity to timing and coefficient errors. In order to minimize these issues, a bandpass ΔΣ modulator can be designed with frequency downconversion inside its feedback loop, as proposed in [Tao99a] and [Nam99]. These architectures, which are referred here as *downconversion* bandpass ΔΣ modulators, process high-frequency input signals, but use low sampling rates and primarily low-frequency loop filters.

2.3.1 Overview

This section provides an overview of downconversion bandpass ΔΣ modulators, and outlines their performance and implementation advantages compared to a conventional architecture. Figure 2.12 shows general block diagrams for conventional and downconversion bandpass ΔΣ modulators, and identifies important design parameters.

Definitions

A downconversion bandpass ΔΣ modulator utilizes frequency downconversion in its forward path and frequency upconversion in its feedback path. This enables it to shift its signal band from a high centre frequency at its input, down to a low centre frequency at its output. Here, the input and output centre frequencies of the signal band are denoted as f_{Ci} and f_{Co}.

[6] Bandpass ΔΣ modulators implemented in bipolar technologies were reported with centre frequencies around 1 GHz as early as [Gao97]. However, until recently [Ryc10], bandpass ΔΣ modulators implemented in CMOS technologies were limited to centre frequencies below 100 MHz.

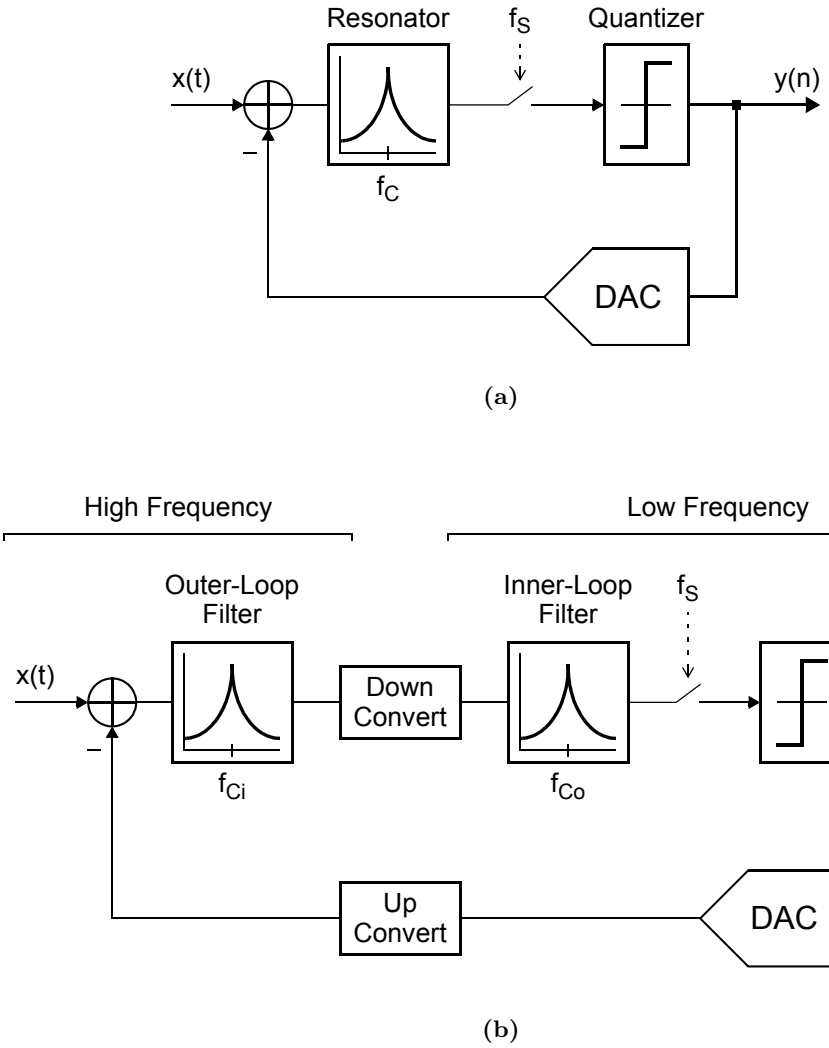


Figure 2.12: General block diagrams for bandpass ΔΣ modulators: **(a)** a conventional architecture, and **(b)** a downconversion architecture.

The loop filter of a downconversion bandpass ΔΣ modulator is generally split between a high-frequency section, which is centred at f_{Ci}, and a low-frequency section, which is centred at f_{Co}. The high-frequency section of the loop filter is referred to here as the *outer-loop* filter, denoted as H_{OL}, and the low-frequency section is referred to as the *inner-loop* filter, denoted as H_{IL}. In addition, the signal path between the input of the upconversion operation and the output of the downcownversion operation is referred to as the *outer-loop* path.

A downconversion bandpass ΔΣ modulator can implement frequency downconversion in its forward path using either mixing or undersampling. The mixing architecture is referred to here as a *frequency-translating* ΔΣ modulator, and the undersampling architecture is referred to as a *subsampling* ΔΣ modulator. Both architectures generally use upconversion mixing in their feedback path, and therefore require a local oscillation (LO) signal in addition to their sampling clock. Frequency-translating ΔΣ modulators are discussed further in Section 2.3.3, and subsampling ΔΣ modulators are discussed further in Section 2.3.2.

Comparison to Conventional Bandpass ΔΣ Modulators

This subsection outlines the advantages and disadvantages of downconversion bandpass ΔΣ modulators relative to conventional bandpass ΔΣ modulators. A downconversion architecture is less sensitive to timing and coefficient errors than a conventional architecture, and has the potential for lower power consumption and higher integration (i.e., reduced area). However, the downconversion architecture has additional constraints on its timing parameters.

As described previously, the loop filter of a downconversion bandpass ΔΣ modulator can be divided into a high-frequency section, which is centred at f_{Ci}, and a low-frequency section, which is centred at f_{Co}. Since errors in f_{Co} are smaller, relative to the signal bandwidth (f_B) of the ΔΣ modulator, than equivalent errors in f_{Ci}, the low-frequency section of the loop filter is less sensitive to errors in its centre frequency. Therefore, a downconversion bandpass ΔΣ modulator is less sensitive to coefficient errors than a conventional bandpass ΔΣ modulator, since the loop filter of a conventional architecture is centred only at f_{Ci}.

The low-frequency section of the loop filter can be implemented using any of a number of standard circuit topologies, which include active-RC, gm-C, and switched-capacitor, among others. The high-frequency section, however, can only be implemented using an LC topology [Sch06a]. Since an LC circuit topology requires one or more inductors, it is not as well-suited to integration as the aforementioned low-frequency topologies, which require only capacitors and resistors. Therefore, by implementing one section of their loop filter at a low frequency, downconversion bandpass ΔΣ modulators can generally achieve a higher level of integration than conventional architectures.

The sampling frequency (f_S) of a downconversion bandpass ΔΣ modulator can be reduced below its input centre frequency (i.e., $f_S < f_{Ci}$), and can therefore be significantly lower than that of a conventional architecture. The sampling frequency of a conventional bandpass ΔΣ modulator must be higher than the Nyquist frequency of its signal band (i.e., $f_S > 2f_{Ci}+f_B$) to avoid aliasing distortion, and is generally selected so that $f_S = 4f_{Ci}$. This maximizes the noise-shaping performance of its loop filter, and simplifies the implementation of its digital post-processing. A downconversion bandpass ΔΣ modulator can achieve the same advantages by selecting its sampling frequency so that $f_S = 4f_{Co}$.

By using a lower sampling frequency than a conventional architecture, a downconversion bandpass ΔΣ modulator can achieve reduced sensitivity to timing errors. Such errors can be classified either as dynamic (e.g., clock jitter) or static (e.g., variations in the loop delay). In a continuous-time ΔΣ modulator, jitter on the sampling clock modifies the response of the feedback DAC in such a way that out-of-band quantization noise is shifted into the signal band (Section 3.2.1). The in-band noise associated with a given rms jitter is proportional to the output rate of the feedback DAC, and therefore decreases with the sampling frequency. At high sampling frequencies, static variations in the loop delay become significant, and can reduce the noise shaping performance and stability of a ΔΣ modulator [Sch06c]. Again, the effect of a given delay error decreases with the sampling frequency.

In a high-frequency continuous-time ΔΣ modulator, the dynamic power of the quantizer, the digital logic, and the clock buffers accounts for a significant portion of the overall power consumption [Ryc09][Lu10]. Since the dynamic power of these circuits is proportional to the operating frequency, the overall power consumption of a high-frequency ΔΣ modulator can be reduced by decreasing its sampling frequency. Therefore, a downconversion bandpass ΔΣ modulator can achieve significant power savings over a conventional architecture.

A downconversion bandpass ΔΣ modulator can implement frequency downconversion by using either mixing or undersampling, as outlined previously. Since both operations are time variant, their introduction into the forward and feedback paths of a ΔΣ modulator causes its loop response to become time-variant. This time-varying loop response can shift out-of-band quantization noise into the signal band, resulting in performance loss or instability. However,

since both operations (mixing, undersampling) are also periodic, the sampling frequency of a downconversion bandpass ΔΣ modulator can be selected in such a way that its loop response is time-invariant after sampling. When the sampled response of a linear time-variant system is time-invariant, it is generally referred to as periodically linear time-invariant (PLTI) [Tao99a]. Sections 4.2.1 and 5.2.1 derive the sampling constraints that must be satisfied to implement frequency-translating ΔΣ modulators as PLTI systems.

2.3.2 Subsampling ΔΣ Modulators

A subsampling ΔΣ modulator uses *undersampling* to implement frequency downconversion in its forward path. Figure 2.13 shows a block diagram for a subsampling ΔΣ modulator. In a subsampling architecture, the inner-loop filter must be implemented using a discrete-time circuit topology, since downconversion and sampling must occur at the same time. Note that the upconversion mixer in the feedback path is sometimes excluded, in particular when the *undersampling factor*[7] is low [Koc04].

Subsampling ΔΣ modulators are generally designed using single-path architectures, since a sampling process cannot generate true quadrature phases of a signal. The subsampling ΔΣ modulator reported in [Ree07] approximated image-reject mixing using delayed in-phase and quadrature sampling clocks. This approach produced a frequency-dependent phase shift that only provided adequate image rejection within a narrow band of frequencies.

The following is a brief review of papers related to subsampling ΔΣ modulators that were important to this work, and does not represent an exhaustive list.

[Nam99] This paper presented the first implementation of a bandpass ΔΣ modulator that used undersampling inside its feedback loop. The reported architecture was designed to downconvert a 40 kHz signal band from 400 MHz to baseband, and used a reconstruction filter in its feedback path to improve the linearity of its downconversion mixer.

[7] The undersampling factor is defined as the ratio of the input centre frequency (f_{Ci}) to the output centre frequency (f_{Co}) [Bei09].

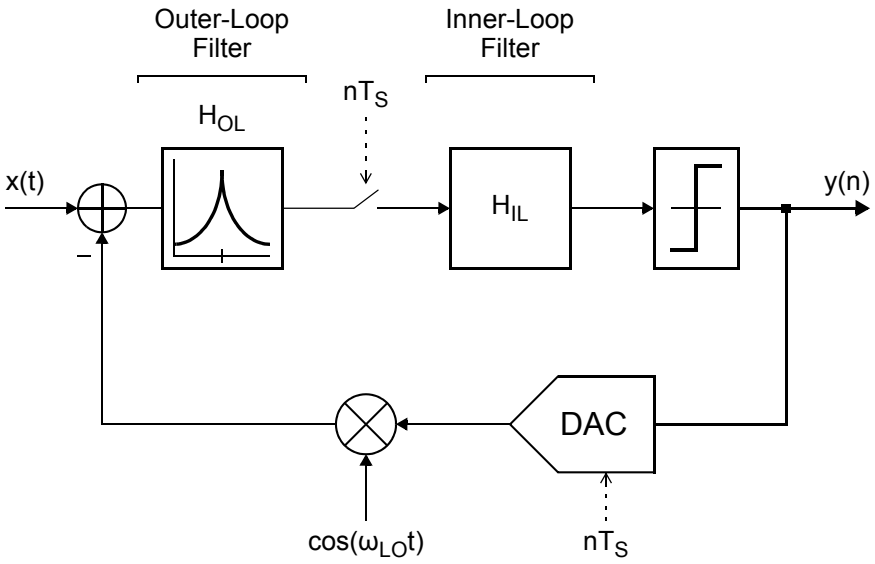


Figure 2.13: Block diagram for a subsampling ΔΣ modulator.

[**Hus00**] This paper derived a transfer function for the outer-loop path of a subsampling ΔΣ modulator, and examined its dependence on the phase of the LO signal applied to the upconversion mixer.

[**Koc04**] This paper proposed a *mirrored-image* subsampling ΔΣ modulator, where the input signal was downconverted from the first alias band (i.e., $f_{Co} = f_S - f_{Ci}$), and the loop filter did not include a low-frequency section. The presented architecture was designed with undersampling primarily to reduce its sampling frequency (Section 2.3.1), and was later implemented in [Ryc08] and [Bei09].

[**Ryc08**] This paper presented a 6th-order subsampling ΔΣ modulator that was designed to downconvert a 60 MHz signal band from 2.4 GHz to 600 MHz. The reported architecture was the first CMOS implementation of an RF bandpass ΔΣ modulator.

2.3.3 Frequency-Translating ΔΣ Modulators

A frequency-translating ΔΣ modulator uses *mixing* to implement frequency downconversion in its forward path. The frequency-translating ΔΣ modulator that is presented in this thesis is designed with *single-path* mixing, whereas frequency-translating ΔΣ modulators reported previously in the literature utilized *image-reject* mixing. Figure 2.14 shows a block diagram for an image-reject frequency-translating ΔΣ modulator.

The following is a review of papers related to frequency-translating ΔΣ modulators that were important to this work.

[Tao99a] This paper presented the first implementation of a bandpass ΔΣ modulator with mixers inside its feedback loop. The reported architecture used image-reject mixing to downconvert a 200 kHz signal band from 100 MHz to baseband, and was designed with discrete-time inner-loop filters. This paper also described the basic sampling constraint that is required to design a frequency-translating ΔΣ modulator as a PLTI system.

[Pul05] This paper proposed a modification to the architecture presented in [Tao99a] that replaced the discrete-time inner-loop filters with equivalent continuous-time filters. This substitution enabled the proposed architecture to achieve clock-jitter performance that is comparable to that of a lowpass ΔΣ modulator (Section 3.5).

[Kol10] This paper presented a 5th-order image-reject frequency-translating ΔΣ modulator that was designed to downconvert a 9 MHz signal band from 900 MHz to baseband. The reported architecture avoided the sampling constraints derived in [Tao99a] by filtering out-of-band quantization noise prior to its upconversion mixer.

Comparison to Subsampling ΔΣ Modulators

In terms of their implementation and performance, the most important difference between a frequency-translating ΔΣ modulator and a subsampling ΔΣ modulator is the position of the sampling operation. A subsampling architecture must perform downconversion and sampling simultaneously, whereas a frequency-translating architecture separates these operations.

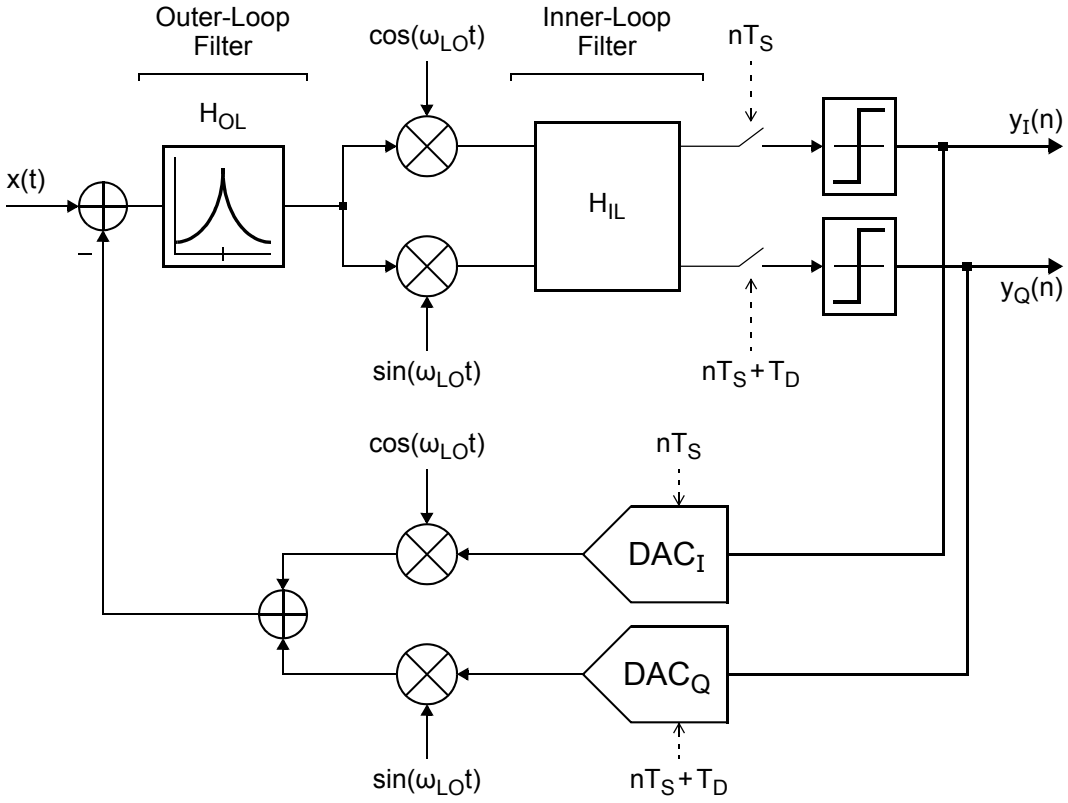


Figure 2.14: Block diagram for an image-reject frequency-translating ΔΣ modulator.

In a frequency-translating ΔΣ modulator, the low-frequency section of the loop filter can be implemented using a continuous-time circuit topology or a discrete-time circuit topology, whereas in a subsampling architecture, the low-frequency section must be implemented using a discrete-time topology. As described in Section 2.1.2, a continuous-time loop filter offers a number of advantages over a discrete-time loop filter, including inherent anti-alias filtering, suppression of sampling errors, and higher potential for low-power and high-speed design. In both architectures, the high-frequency section of the loop filter must be implemented using a continuous-time circuit topology. As a result, both have approximately the same sensitivity to clock jitter.

In a subsampling ΔΣ modulator, the bandwidth (f_{sw}) of the sampling switch should be higher than the input centre frequency (f_{Ci}) so that the input signal is not attenuated. Since this bandwidth requirement can result in $f_{\mathrm{sw}} \gg f_{\mathrm{S}}/2$, the performance of a subsampling ΔΣ modulator is significantly affected by out-of-band noise, which is folded into the signal band during sampling. In a frequency-translating ΔΣ modulator, the sampling bandwidth is only required to be higher than the output centre frequency (f_{Co}) to ensure that the input signal is not attenuated. Accordingly, a frequency-translating architecture is less sensitive to folded out-of-band noise than a subsampling architecture.

2.4 Summary

This chapter reviewed the fundamental theory of ΔΣ modulation. It explained the concepts of quantization, oversampling, and noise shaping, compared the advantages of discrete-time and continuous-time implementations, and reviewed conventional architectures. This chapter also provided an overview of downconversion bandpass ΔΣ modulators. It summarized their advantages relative to conventional architectures and examined the different downconversion architectures: subsampling ΔΣ modulators and frequency-translating ΔΣ modulators, which are based on undersampling and mixing, respectively.

Chapter 3

Timing Errors *in* Continuous-Time $\Delta\Sigma$ Modulators

The feedback loop of a continuous-time $\Delta\Sigma$ modulator performs a continuous-time to discrete-time signal conversion in its forward path at the sampler and a corresponding discrete-time to continuous-time conversion in its feedback path at the DAC. The accuracy of these conversions is limited by the timing accuracy of the sampling clock. Timing errors that are introduced at the sampler and feedback DAC decrease the noise-shaping performance of a continuous-time $\Delta\Sigma$ modulator, and can significantly limit its resolution [Che99a][Tao99b]. The timing errors that are introduced at the feedback DAC are particularly important, since they are not suppressed by the loop filter of the $\Delta\Sigma$ modulator.

This chapter presents a modeling technique that can be used to rapidly simulate the effect of timing errors in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator. In particular, the proposed technique is useful for evaluating the performance loss caused by clock jitter, since it offers a significant speed advantage over direct simulation methods [Cho07]. The proposed technique models *time-delay* errors in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator as *coefficient* errors in the loop filter of an equivalent discrete-time architecture. It is derived from the impulse-invariant transform, which is a standard synthesis tool for continuous-time $\Delta\Sigma$ modulators. In this chapter, the speed advantage of the proposed modeling technique is utilized to simulate a wide variety of rectangular DAC pulses.

This chapter is organized into six sections. Section 3.1 reviews a standard NTF synthesis procedure for continuous-time ΔΣ modulators, and discusses impulse invariance. Section 3.2 reviews the primary sources of timing errors in a continuous-time ΔΣ modulator, focusing in particular on clock jitter. Section 3.3 presents a technique to model the effect of these timing errors using an equivalent discrete-time ΔΣ modulator, and explains how this technique can be applied to simulate the performance loss caused by these errors. Section 3.4 demonstrates the speed and accuracy of the proposed technique using a Simulink behavioural model that directly represents timing errors. Section 3.5 then uses the proposed technique to analyse the effect of different rectangular DAC pulses on the clock-jitter sensitivity of a continuous-time ΔΣ modulator. Section 3.6 summarizes the results of the chapter.

3.1 NTF Synthesis

A common design procedure for continuous-time ΔΣ modulators is to start with a prototype discrete-time NTF that provides the required noise shaping performance, and then map it to a corresponding continuous-time architecture. This approach enables designers to utilize the wide range of design and simulation tools available for discrete-time ΔΣ modulators [Sch04]. In general, the required discrete-time to continuous-time transformation is carried out using the *impulse-invariant transform* [Gar86].

Figure 3.1 shows block diagrams for a continuous-time ΔΣ modulator and an equivalent discrete-time ΔΣ modulator. It also shows the loop feedback path of each architecture, from their output $y(n)$, to the input of their quantizers $v(n)$. Here, the loop transfer functions of the continuous-time and discrete-time ΔΣ modulators are represented as $H_{\mathrm{L}}(s)$ and $H'_{\mathrm{L}}(z)$, respectively. The loop transfer function of a discrete-time ΔΣ modulator can be expressed in terms of its associated NTF as

$$H'_{\mathrm{L}}(z) \;=\; \frac{1}{\mathrm{NTF}(z)} - 1 \tag{3.1}$$

where the design of $\mathrm{NTF}(z)$ is discussed in Section 2.1.3.

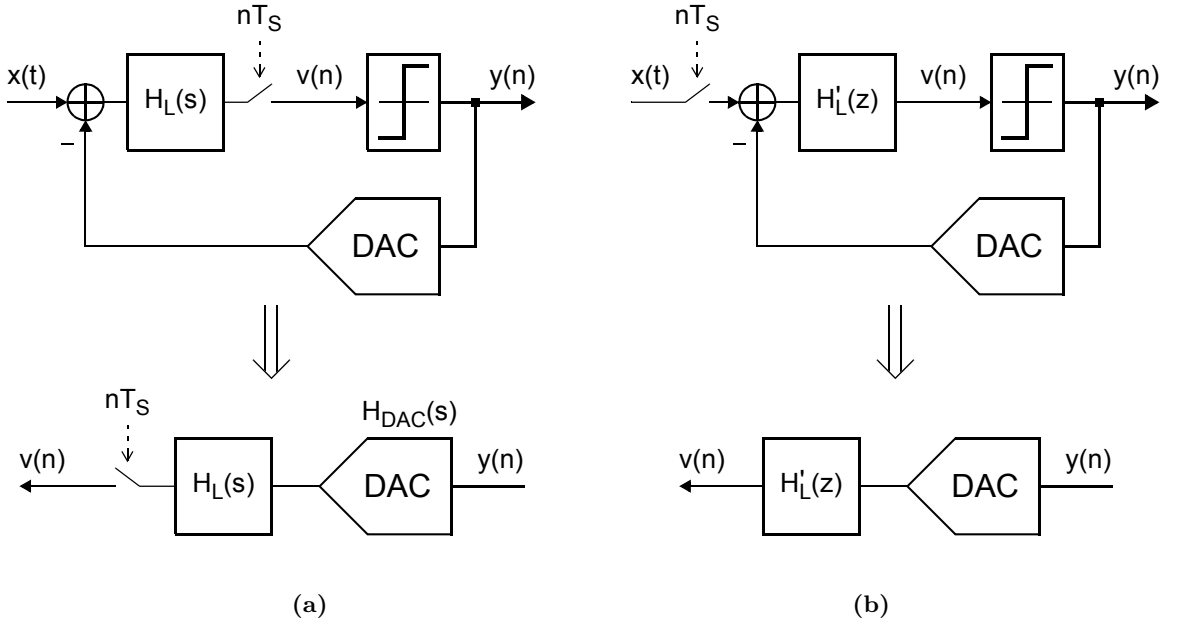


Figure 3.1: The loop feedback paths of: **(a)** a continuous-time $\Delta\Sigma$ modulator, and **(b)** an equivalent discrete-time $\Delta\Sigma$ modulator.

In order to replicate the NTF of a prototype discrete-time architecture, a continuous-time $\Delta\Sigma$ modulator must have the same loop response[1] at sampling instants [Che02]. This impulse equivalence can be achieved using the impulse-invariant transform, which is defined as

$$H'_{\mathrm{L}}(z) \;=\; \underset{s\,\to\,z}{\mathrm{IIT}}\Big\{H_{\mathrm{L}}(s)H_{\mathrm{DAC}}(s)\Big\} \;=\; \mathcal{Z}\Big\{\,\mathcal{L}^{-1}\big\{H_{\mathrm{L}}(s)H_{\mathrm{DAC}}(s)\big\}\big|_{t\,=\,nT_{\mathrm{S}}}\Big\} \tag{3.2}$$

Here, $\mathcal{Z}\{\cdot\}$ denotes the z-transform, $\mathcal{L}\{\cdot\}$ denotes the Laplace transform, and $\underset{s\,\to\,z}{\mathrm{IIT}}\{\cdot\}$ denotes an $s \to z$ impulse-invariant transform. In a continuous-time $\Delta\Sigma$ modulator, the DAC is used to convert each feedback sample into an equivalent continuous-time pulse. The shape of these pulses is set by the transfer function $H_{\mathrm{DAC}}(s)$ of the DAC [Ort06].

[1]The term *loop response* is used to refer to the impulse response of the loop feedback path of a $\Delta\Sigma$ modulator, from its output $y(n)$, to the input of its quantizer $v(n)$.

The loop transfer function of a continuous-time ΔΣ modulator can be expressed in terms of a prototype NTF by combining Equations (3.1) and (3.2). This results in

$$H_{\mathrm{L}}(s) \;=\; \underset{z\to s}{\mathrm{IIT}}\Big\{H'_{\mathrm{L}}(z)\Big\}\cdot\frac{1}{H_{\mathrm{DAC}}(s)} \;=\; \underset{z\to s}{\mathrm{IIT}}\left\{\frac{1}{\mathrm{NTF}(z)}-1\right\}\cdot\frac{1}{H_{\mathrm{DAC}}(s)} \tag{3.3}$$

where $\underset{z\to s}{\mathrm{IIT}}\{\cdot\}$ denotes an $z\to s$ impulse-invariant transform. An example of this transform is provided in Appendix A.1.

In Equation (3.3), it is important to note that the loop response of a continuous-time ΔΣ modulator depends on the response of its feedback DAC. This means that the noise-shaping performance of a continuous-time architecture is sensitive to timing errors in the pulses that are generated by its feedback DAC. These errors are discussed in Section 3.2.

3.1.1 Excess Loop Delay

In an ideal continuous-time ΔΣ modulator, the DAC output is updated on the same edge of the sampling clock that the associated input is sampled by the quantizer. Therefore, unlike a discrete-time architecture, a continuous-time ΔΣ modulator does not have an inherent delay in its feedback path, and must include an additional delay to provide time for its quantizer to settle and its mismatch shaping logic to operate. The non-zero delay between the time when the signal is sampled by the quantizer and when the corresponding pulse is generated by the feedback DAC is referred to as the *excess loop delay* [Che99b].

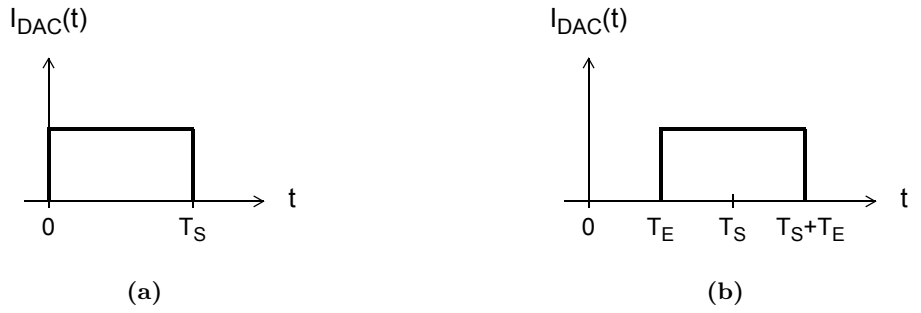


Figure 3.2: (a) An ideal non-return-to-zero (NRZ) DAC pulse, and **(b)** the DAC pulse shown in (a) with an excess loop delay of T_{E}.

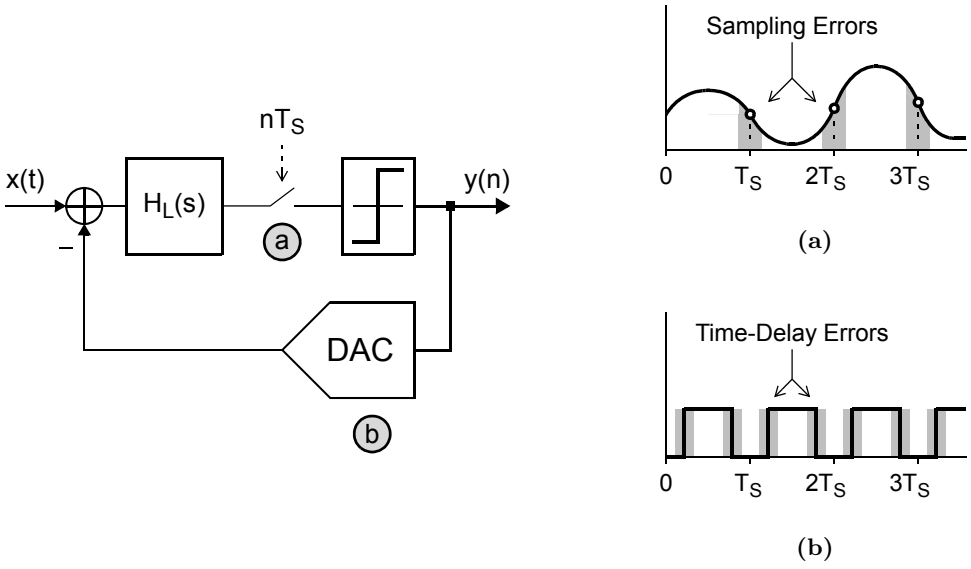


Figure 3.3: Timing errors in a continuous-time $\Delta\Sigma$ modulator: **(a)** sampling errors in the forward path, and **(b)** time-delay errors in the feedback DAC.

Figure 3.2 plots the response of a conventional non-return-to-zero (NRZ) feedback DAC when the excess loop delay is zero and when it is equal to T_{E}. As indicated in Equation (3.3), the NTF of a continuous-time $\Delta\Sigma$ modulator depends on the response of its feedback DAC. Therefore, the excess loop delay must be accounted for in the NTF synthesis by introducing a corresponding delay term into $H_{\mathrm{DAC}}(s)$. This modification is described in Section 6.1.4 for the experimental $\Delta\Sigma$ modulator.

3.2 Timing Errors

In a continuous-time $\Delta\Sigma$ modulator, timing errors in the sampling clock can affect both the forward and feedback paths, as depicted in Figure 3.3. In the forward path, timing errors in the sampling instants receive the same suppression from the $\Delta\Sigma$ loop as quantization errors, and do not significantly affect the resolution. In the feedback path, timing errors in the pulses generated by the feedback DAC are added to the input signal of the $\Delta\Sigma$ modulator, and can significantly reduce the resolution.

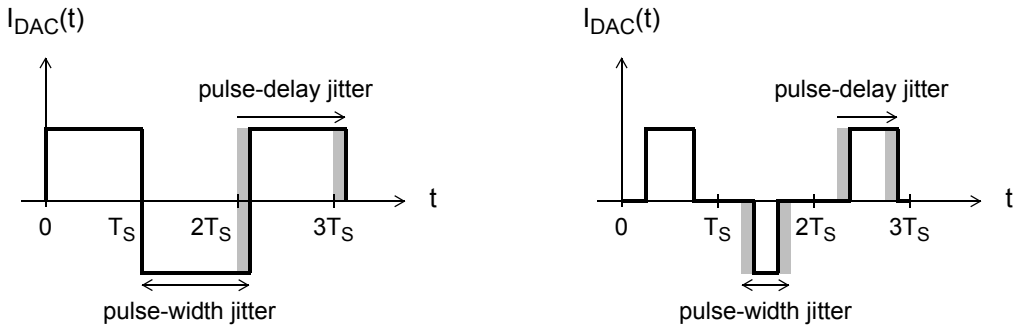


Figure 3.4: The effect of pulse-width and pulse-delay jitter on: **(a)** a non-return-to-zero (NRZ) pulse, and **(b)** a return-to-zero (RZ) pulse.

The timing errors introduced into the feedback path of a continuous-time ΔΣ modulator modify the response of its DAC, and therefore modify its NTF, where

$$\widehat{\mathrm{NTF}}(z) \;=\; \frac{1}{1+\widehat{H}'_{\mathrm{L}}(z)} \;=\; \frac{1}{1+\underset{s\,\to\,z}{\mathrm{IIT}}\Big\{H_{\mathrm{L}}(s)\widehat{H}_{\mathrm{DAC}}(s)\Big\}} \tag{3.4}$$

The $\widehat{\cdot}$ notation is introduced here to identify continuous-time and discrete-time expressions that model the effect of timing errors. In Equation (3.4), timing errors in the response of the feedback DAC are represented using $\widehat{H}_{\mathrm{DAC}}(s)$, and are mapped into the discrete-time domain using $\widehat{H}'_{\mathrm{L}}(z)$. The derivation of this *mapping term* is presented in Section 3.3.

3.2.1 Clock Jitter

The principal disadvantage of continuous-time ΔΣ modulators is their sensitivity to jitter on the sampling clock [Red07]. Clock jitter introduces *sampling* errors into the forward path of a continuous-time ΔΣ modulator, and *time-delay* errors into the pulses of its feedback DAC. As described previously, sampling errors receive the same suppression as quantization errors, and do not affect the resolution, whereas time-delay errors are added directly to the input of a continuous-time ΔΣ modulator, and can significantly limit its resolution.

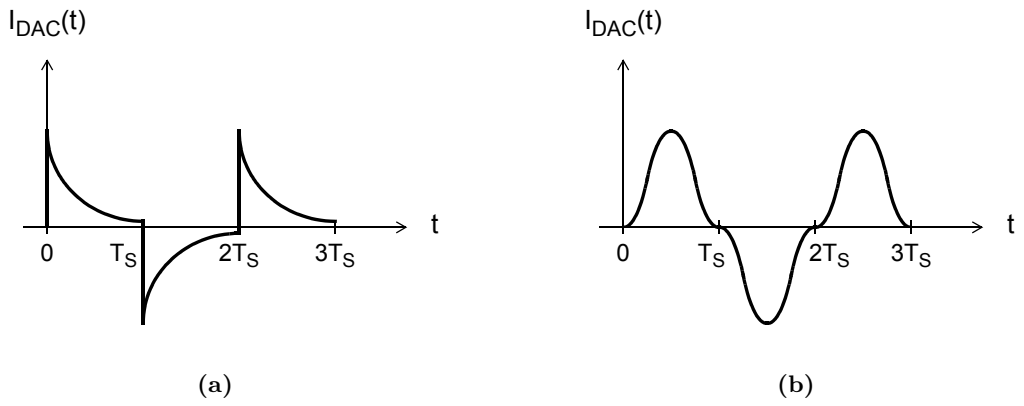


Figure 3.5: (a) An exponential DAC pulse, and **(b)** a raised-cosine DAC pulse.

The timing errors that are introduced into the pulses of the feedback DAC by clock jitter can be divided into *pulse-width* errors and *pulse-delay* errors [Oli98]. Figure 3.4 depicts these errors on conventional non-return-to-zero (NRZ) and return-to-zero (RZ) pulses. In general, a lowpass $\Delta\Sigma$ modulator is sensitive primarily to pulse-width jitter, whereas a bandpass $\Delta\Sigma$ modulator is sensitive to both types of jitter [Che99a][Tao99b]. Section 3.5 analyses the jitter sensitivity of lowpass and bandpass architectures for various rectangular DAC pulses.

The performance loss caused by clock jitter can be reduced by modifying the shape of the DAC pulse. This is generally referred to as *pulse shaping*. Figure 3.5(a) shows an example of *exponential* pulse shaping, which replicates the charge transfer phase of a switched-capacitor circuit [Vel03][Ort01]. By shifting the charge transfer to the start of the sampling period, an exponential pulse achieves reduced sensitivity to pulse-width jitter, and is therefore suitable for lowpass $\Delta\Sigma$ modulators. Figure 3.5(b) shows an example of *raised-cosine* pulse shaping, where the shaping signal is synchronized with the sampling clock so that its minimum value and its minimum slope occur when the DAC is updated [Lus04][Zha96]. When it is properly synchronized, a raised-cosine pulse achieves reduced sensitivity to both pulse-width jitter and pulse-delay jitter, and is therefore suitable for bandpass $\Delta\Sigma$ modulators.

3.3 Modeling Technique

The impulse-invariant transform of a continuous-time filter yields a discrete-time filter that has the same impulse response when the output of the continuous-time system is sampled at the same frequency [Gar86]. The transform is used to design continuous-time ΔΣ modulators from prototype discrete-time ΔΣ modulators, as described in Section 3.1.

The modeling technique presented in this section uses the impulse-invariant transform to map *time-delay* errors in the edges of the pulses that are generated by the feedback DAC of a continuous-time ΔΣ modulator to *coefficient* errors in the loop transfer function $H'_{\mathrm{L}}(z)$ of an equivalent discrete-time ΔΣ modulator (Figure 3.1). This mapping is possible because the start and end times of the rectangular pulses that are generated by the feedback DAC appear as parameters in the impulse-invariant transform.

Figure 3.6 shows timing diagrams for conventional NRZ and RZ DAC pulses. Here, α is used to represent the time delay between the start of the sampling period and the rising edge of the DAC pulse, and β is used to represent the time delay between the start of the sampling period and the falling edge of the DAC pulse. Using this notation, the transfer function of a rectangular DAC can be expressed, generally, as

$$H_{\mathrm{DAC}}(s) \;=\; \frac{1}{s}\Big(\mathrm{e}^{-s\alpha T_{\mathrm{S}}} - \mathrm{e}^{-s\beta T_{\mathrm{S}}}\Big) \tag{3.5}$$

Here, α and β are normalized with respect to the sampling period T_{S}.

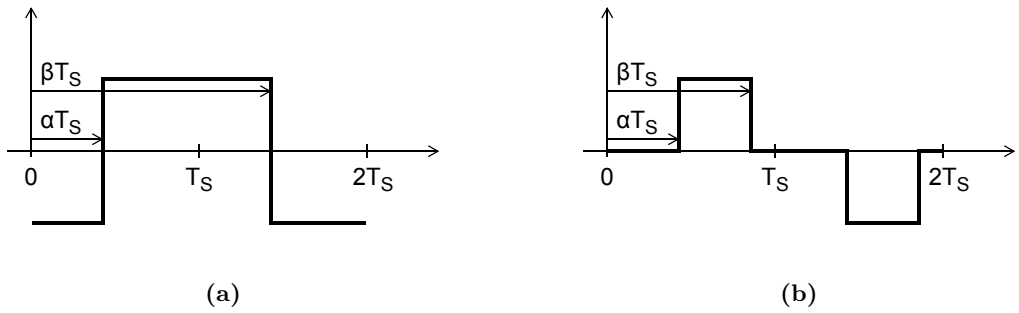


Figure 3.6: Timing diagrams for: **(a)** an NRZ pulse, and **(b)** an RZ pulse.

Accordingly, *additive* time-delay errors on the nominal edges, α and β, of the DAC pulse can be expressed, respectively, as

$$\widehat{\alpha}(n) \equiv \alpha + \Delta\alpha(n) \quad \text{and} \quad \widehat{\beta}(n) \equiv \beta + \Delta\beta(n) \tag{3.6}$$

Here, $\widehat{\alpha}(n)$ and $\widehat{\beta}(n)$ represent the normalized time delays for the rising and falling edges of the non-ideal DAC pulse during the nth clock cycle. It is assumed that

$$\widehat{\alpha}(n) \; > \; \widehat{\beta}(n-1) - 1 \quad \text{for RZ pulses, and} \tag{3.7}$$

$$\widehat{\alpha}(n) \; = \; \widehat{\beta}(n-1) - 1 \quad \text{for NRZ pulses.} \tag{3.8}$$

The time index n is not included in subsequent expressions for simplicity.

The modeling technique presented in this section represents continuous-time delay errors in the discrete-time domain using a series of z-domain error-mapping terms. These mapping terms transform *time-delay* errors, $\Delta\alpha$ and $\Delta\beta$, in the DAC pulses of a continuous-time $\Delta\Sigma$ modulator into corresponding *coefficient* errors in the loop transfer function of an equivalent discrete-time $\Delta\Sigma$ modulator. In order to demonstrate this technique, the 2nd-order mapping term is derived next.

3.3.1 Derivation of the Error-Mapping Terms

Given a prototype discrete-time loop transfer function $H'_{\mathrm{L}}(z)$, the first step in developing an equivalent continuous-time transfer function $H_{\mathrm{L}}(s)$ using the impulse-invariant transform is to split $H'_{\mathrm{L}}(z)$ into its constituent terms by way of a partial fraction expansion. An example of a 2nd-order term that can result from such an expansion is

$$H'_{\mathrm{L},\,2}(z) \; = \; \frac{c_2}{(z-1)^2} \tag{3.9}$$

where c_2 is its coefficient.

Using α and β to denote the nominal start and end times of the DAC pulse, $H'_{\mathrm{L},\,2}(z)$ can be transformed into an equivalent continuous-time filter by way of a $z \rightarrow s$ impulse-invariant transform. Such a transform results in

$$H_{\mathrm{L},\,2}(s) \;=\; \underset{z\,\rightarrow\,s}{\mathrm{IIT}}\Big\{H'_{\mathrm{L},\,2}(z)\Big\} \cdot \frac{1}{H_{\mathrm{DAC}}(s)} \;=\; \frac{b_1(sT_{\mathrm{S}}) + b_2}{(sT_{\mathrm{S}})^2} \tag{3.10}$$

where

$$\begin{aligned} b_1 \;&=\; \frac{1}{2}\frac{c_2\,(\alpha+\beta-2)}{\beta-\alpha} \\ b_2 \;&=\; \frac{c_2}{\beta-\alpha} \end{aligned}$$

and $H_{\mathrm{DAC}}(s)$ is defined in Equation (3.5).

The objective here is to modify the nominal transfer function $H'_{\mathrm{L},\,2}(z)$ in such a way that the loop response of the associated discrete-time ΔΣ modulator is equal to the loop response of an equivalent continuous-time architecture when the DAC pulses of the latter are affected by time-delay errors.

Assume that the rising and falling edges of the DAC pulses are independently shifted by time-delay errors $\Delta\alpha$ and $\Delta\beta$, as defined in Equation (3.6). The effect of these errors can be mapped into the discrete-time domain by performing an $s \rightarrow z$ impulse-invariant transform on $H_{\mathrm{L},\,2}(s)$ using non-ideal edge timing $\widehat{\alpha}$ and $\widehat{\beta}$. This transform results in

$$\widehat{H}'_{\mathrm{L},\,2}(z) \;=\; \underset{s\,\rightarrow\,z}{\mathrm{IIT}}\Big\{H_{\mathrm{L},\,2}(s)H_{\mathrm{DAC}}(s)\Big\} \;=\; \frac{d_1}{(z-1)} + \frac{d_2 z + d_3}{(z-1)^2} \tag{3.11}$$

where

$$\begin{aligned} d_1 \;&=\; b_1\Big[\,\widehat{\beta}-\widehat{\alpha}\,\Big] \\ d_2 \;&=\; \frac{1}{2}\,b_2\Big[\,\widehat{\beta}\,\big(2-\widehat{\beta}\,\big) - \widehat{\alpha}\,\big(2-\widehat{\alpha}\,\big)\,\Big] \\ d_3 \;&=\; \frac{1}{2}\,b_2\Big[\,\widehat{\beta}^{\,2} - \widehat{\alpha}^{\,2}\,\Big] \end{aligned}$$

and $H_{\mathrm{DAC}}(s)$ is defined in Equation (3.5).

Table 3.1: Error-mapping terms for poles at $z = 1$.

Nominal Term	Error-Mapping Term
$H'_{\mathrm{L},\,1}(z) = \dfrac{c_1}{(z-1)}$	$\widehat{H}'_{\mathrm{L},\,1}(z) = \dfrac{c_1}{(z-1)} + \dfrac{\Delta c_{11}}{(z-1)}$ $\Delta c_{11} = c_1(\Delta\beta - \Delta\alpha)/(\beta - \alpha)$
$H'_{\mathrm{L},\,2}(z) = \dfrac{c_2}{(z-1)^2}$	$\widehat{H}'_{\mathrm{L},\,2}(z) = \dfrac{c_2}{(z-1)^2} + \dfrac{\Delta c_{22}}{(z-1)^2} + \dfrac{\Delta c_{21}}{(z-1)}$ $\Delta c_{22} = c_2(\Delta\beta - \Delta\alpha)/(\beta - \alpha)$ $\Delta c_{21} = -1/2\, c_2(\Delta\alpha + \Delta\beta)$
$H'_{\mathrm{L},\,3}(z) = \dfrac{c_3}{(z-1)^3}$	$\widehat{H}'_{\mathrm{L},\,3}(z) = \dfrac{c_3}{(z-1)^3} + \dfrac{\Delta c_{33}}{(z-1)^3} + \dfrac{\Delta c_{32}}{(z-1)^2} + \dfrac{\Delta c_{31}}{(z-1)}$ $\Delta c_{33} = c_3(\Delta\beta - \Delta\alpha)/(\beta - \alpha)$ $\Delta c_{32} = -1/2\, c_3(\Delta\alpha + \Delta\beta)$ $\Delta c_{31} = 1/12\, c_3[(\beta - \alpha)(\Delta\beta - \Delta\alpha) + 3(\Delta\alpha + \Delta\beta)]$

The expression for $\widehat{H}'_{\mathrm{L},\,2}(z)$ can then be simplified to

$$\widehat{H}'_{\mathrm{L},\,2}(z) \;=\; \frac{c_2}{(z-1)^2} + \frac{\Delta c_{22}}{(z-1)^2} + \frac{\Delta c_{21}}{(z-1)} \tag{3.12}$$

where Δc_{22} and Δc_{21} are defined in Table 3.1. The first term of $\widehat{H}'_{\mathrm{L},\,2}(z)$ corresponds to the nominal term $H'_{\mathrm{L},\,2}(z)$ in Equation (3.9), whereas the second and third terms are caused by time-delay errors $\Delta\alpha$ and $\Delta\beta$. Therefore, the expression in Equation (3.12) maps *time-delay* errors in the DAC pulses of a continuous-time $\Delta\Sigma$ modulator to *coefficient* errors in the loop transfer function of an equivalent discrete-time architecture.

Table 3.1 provides the error-mapping terms for 1st-, 2nd-, and 3rd-order terms of a loop transfer function with coincident poles at $z = 1$. Table 3.2 provides the error-mapping terms for a 1st-order term with a pole at $z = z_{\mathrm{p}}$, and for a 2nd-order term with complex-conjugate poles at $z = z_{\mathrm{p}}^*$ and $z = z_{\mathrm{p}}$. All of the error-mapping terms listed in Tables 3.1 and 3.2 were derived using the procedure described in this section.

Table 3.2: Error-mapping terms for poles at $z = z_\mathrm{p}$.

Nominal Term	Error-Mapping Term
$H'_{\mathrm{L},\,1\mathrm{p}}(z) = \dfrac{c_{1\mathrm{p}}}{(z - z_\mathrm{p})}$	$\widehat{H}'_{\mathrm{L},\,1\mathrm{p}}(z) = \dfrac{\delta c_{1\mathrm{p}}}{(z - z_\mathrm{p})}$ $\delta c_{1\mathrm{p}} = c_{1\mathrm{p}}(z_\mathrm{p}^{\beta-\Delta\alpha} - z_\mathrm{p}^{\alpha-\Delta\beta})/(z_\mathrm{p}^{\beta} - z_\mathrm{p}^{\alpha})$
$H'_{\mathrm{L},\,2\mathrm{p}}(z) = \dfrac{c_{2\mathrm{p}}}{(z - z_\mathrm{p})} + \dfrac{c_{2\mathrm{p}}^*}{(z - z_\mathrm{p}^*)}$ $= \dfrac{c_{21\mathrm{p}} z - c_{22\mathrm{p}}}{z^2 - 2\,\mathrm{Re}\{z_\mathrm{p}\} + 1}$	$\widehat{H}'_{\mathrm{L},\,2\mathrm{p}}(z) = \dfrac{\delta c_{21\mathrm{p}} z - \delta c_{22\mathrm{p}}}{z^2 - 2\,\mathrm{Re}\{z_\mathrm{p}\} + 1}$ $c_{2\mathrm{p}} = (c_{22\mathrm{p}} - c_{21\mathrm{p}} z_\mathrm{p})/(z_\mathrm{p}^* - z_\mathrm{p})$ $\delta c_{2\mathrm{p}} = c_{2\mathrm{p}}(z_\mathrm{p}^{\beta-\Delta\alpha} - z_\mathrm{p}^{\alpha-\Delta\beta})/(z_\mathrm{p}^{\beta} - z_\mathrm{p}^{\alpha})$ $\delta c_{21\mathrm{p}} = 2\,\mathrm{Re}\{\delta c_{2\mathrm{p}}\}$ $\delta c_{22\mathrm{p}} = 2\,\mathrm{Re}\{\delta c_{2\mathrm{p}} z_\mathrm{p}^*\}$

Note that the derivation approach presented in this section is not formally correct, since it involves taking the Laplace transform and z-transform of expressions that depend on error terms $\Delta\alpha(n)$ and $\Delta\beta(n)$, which can vary from one cycle to the next. Appendix A.2 provides an extended derivation of the 2nd-order error-mapping term, which demonstrates how these error terms can be shifted to the input of the loop filter, so that the same result is achieved without having to process $\Delta\alpha(n)$ and $\Delta\beta(n)$ in the Laplace and z-transforms.

3.3.2 Discrete-Time Simulation of Timing Errors

The error-mapping terms derived in Section 3.3.1 can be used, with a discrete-time simulator, to evaluate the performance loss that is caused by time-delay errors in the feedback DAC of a continuous-time ΔΣ modulator as follows:

1. (a) If starting from a continuous-time loop transfer function $H_\mathrm{L}(s)$, use the impulse invariant transform to derive an equivalent discrete-time transfer function $H'_\mathrm{L}(z)$, and then split $H'_\mathrm{L}(z)$ into its constituent terms.

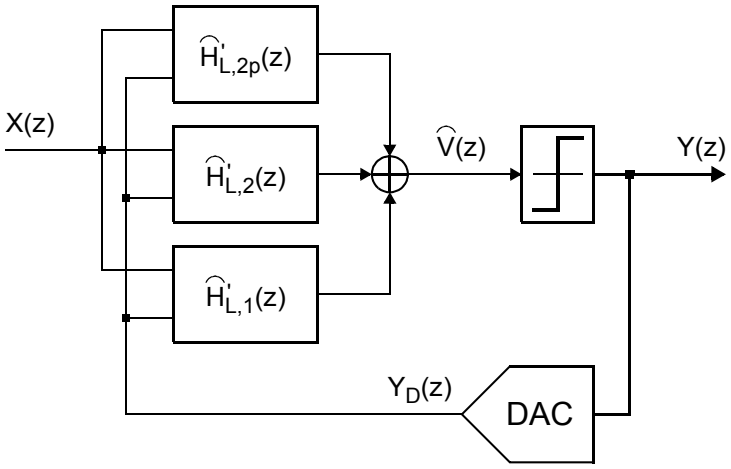


Figure 3.7: Block diagram for a discrete-time $\Delta\Sigma$ modulator that is realized using the error-mapping terms in Tables 3.1 and 3.2.

(b) If starting from a discrete-time loop transfer function $H'_{\mathrm{L}}(z)$, split $H'_{\mathrm{L}}(z)$ into its constituent terms using a partial-fraction expansion.

2. Replace each nominal term in the loop transfer function $H'_{\mathrm{L}}(z)$ with its corresponding error-mapping term, provided in Tables 3.1 and 3.2, to obtain the error-mapping loop transfer function $\widehat{H}'_{\mathrm{L}}(z)$.

3. Place the error-mapping transfer function $\widehat{H}'_{\mathrm{L}}(z)$ in a conventional $\Delta\Sigma$ feedback loop, and simulate the resulting system using a discrete-time simulator.

In a continuous-time $\Delta\Sigma$ modulator, timing errors in the DAC pulses affect the response of the feedback path, but do not modify the response of the forward path. In order to model this behaviour, the error-mapping terms in Tables 3.1 and 3.2 must be realized in such a way that coefficient errors modify the feedback path, but not the forward path. Figure 3.7 shows a block diagram for a discrete-time $\Delta\Sigma$ modulator that is realized using the developed error mapping terms. Figure 3.8 shows realizations of the $\widehat{H}'_{\mathrm{L},\,2}(z)$ and $\widehat{H}'_{\mathrm{L},\,2\mathrm{p}}(z)$ terms specified in Tables 3.1 and 3.2, respectively.

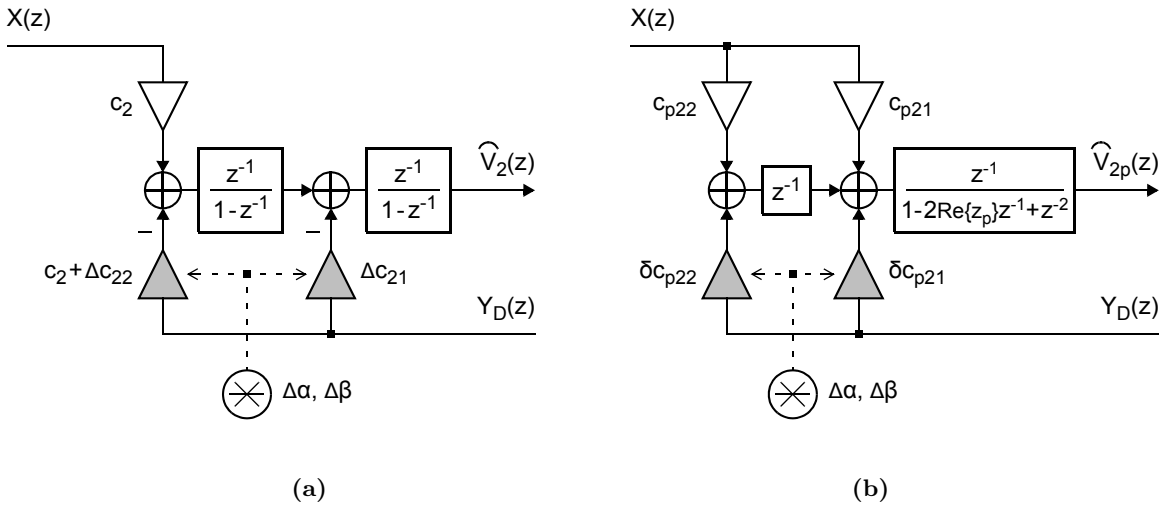


Figure 3.8: Realizations of: **(a)** $\widehat{H}'_{\mathrm{L},\,2}(z)$ in Table 3.1, and **(b)** $\widehat{H}'_{\mathrm{L},\,2\mathrm{p}}(z)$ in Table 3.2. The terminal names in this figure correspond to the discrete-time ΔΣ modulator in Figure 3.7.

3.4 Validation of the Modeling Technique

In order to validate the modeling technique proposed in Section 3.3, a behavioural model was developed in Simulink that *directly*, and therefore accurately, represents time-delay errors in the feedback DAC of a continuous-time ΔΣ modulator. This section describes the design of this behavioural model, and then uses it to demonstrate the simulation accuracy and speed of the presented modeling technique.

3.4.1 Simulink Behavioural Model

Figure 3.9 shows a block diagram for the Simulink behavioural model that was developed to simulate time-delay errors. Its input parameters are the nominal pulse-edge timing, α and β, and their errors, $\Delta\alpha$ and $\Delta\beta$, and its output is a delayed rectangular pulse with edge timing that is set by the supplied input parameters.

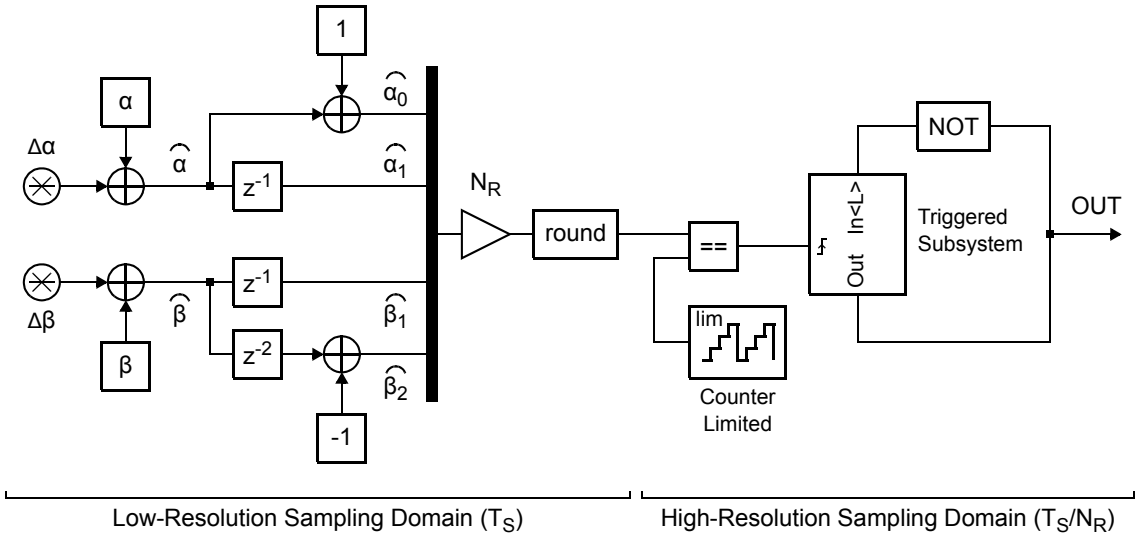


Figure 3.9: Block diagram for the developed Simulink model.

The developed Simulink model is realized completely using discrete-time blocks, since the continuous-time delay blocks that are provided in Simulink do not allow for sufficient timing accuracy. This model is divided into two sampling domains: a *low-resolution* domain, which operates at the sampling period T_{S}, and a *high-resolution* domain, which operates at $T_{\mathrm{S}}/N_{\mathrm{R}}$. Here, N_{R} is an integer that is used to divide the sampling period into smaller time segments. Increasing the value of N_{R} increases the resolution of time-delay variations, but also increases the associated simulation time (Section 3.4.3).

In Figure 3.9, the blocks that operate in the low-resolution sampling domain are used to generate the timing parameters for the α and β edges. Here, the nominal timing parameters, α and β, are added to the corresponding errors, $\Delta\alpha$ and $\Delta\beta$, in order to derive the non-ideal timing parameters, $\widehat{\alpha}$ and $\widehat{\beta}$. The non-ideal parameters are generated during the clock cycle immediately prior to the cycle that they are associated with, so that the model can account for large negative timing errors. These parameters are then offset and delayed in such a way that they are between 0 and 1 during the correct clock cycle. The corresponding sequence of operations is summarized in Table 3.3. The non-ideal timing parameters are combined into a bus, which then determines the edge timing in the high-resolution domain.

Table 3.3: The operations applied to the timing parameters.

Timing Parameter	Offset	Delay	Path
$-1 \leq \widehat{\alpha}(n) < 0$	$+1$	0 cycles	$\widehat{\alpha}_0$
$0 \leq \widehat{\alpha}(n) < 1$	0	1 cycle	$\widehat{\alpha}_1$
$0 \leq \widehat{\beta}(n) < 1$	0	1 cycle	$\widehat{\beta}_1$
$1 \leq \widehat{\beta}(n) < 2$	-1	2 cycles	$\widehat{\beta}_2$

In Figure 3.9, the blocks that operate in the high-resolution sampling domain are used to translate the $\widehat{\alpha}$ and $\widehat{\beta}$ values generated in the low-resolution domain into edge timing for the rectangular output pulse. This is achieved by first converting $\widehat{\alpha}$ and $\widehat{\beta}$ into integers, between 0 and $N_{\mathrm{R}} - 1$, using appropriate scaling and rounding. These integers are then compared to the output of a running counter, which has corresponding limits 0 and $N_{\mathrm{R}} - 1$. The result of this comparison is a series of impulses, which are then used as the clock signal for a positive edge triggered subsystem. The output of the subsystem switches, from $0 \rightarrow 1$ or $1 \rightarrow 0$, upon arrival of *either* an $\widehat{\alpha}$ or $\widehat{\beta}$ impulse, which simplifies the generation of the output signal and eliminates timing conflicts caused by an overlap of $\widehat{\alpha}$ and $\widehat{\beta}$.

RZ Pulse

The presented Simulink model can be used to simulate the response of an RZ DAC, together with associated timing errors, by applying its output as the clock signal and active-low reset of a triggered subsystem. This approach can be used in both single-bit and multi-bit designs, since the model only applies a delay to the input signal of the DAC.

NRZ Pulse

The presented Simulink model can also be used to simulate the response of an NRZ DAC by applying its output as the clock signal of a triggered subsystem. The β edge is not important when generating an NRZ pulse, provided that $\widehat{\beta} > \widehat{\alpha}$ in all cases.

3.4.2 Comparison of Simulation Results

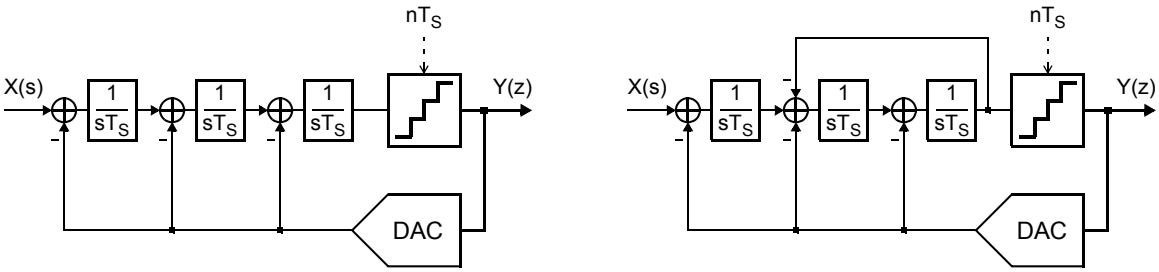
The accuracy of the modeling technique proposed in Section 3.3 is verified by comparing its simulation results to those generated by the direct Simulink behavioural model presented in Section 3.4.1. The proposed technique is validated for the case of dynamic time-delay errors, which are changed from one clock cycle to the next in such a way that they approximate the behaviour of clock jitter, as described next.

In general, clock jitter can be represented as an *additive* timing error on the edges of the DAC pulses, as defined in Equation (3.6). Here, assuming that the timing errors caused by clock jitter are independent from one edge to the next, $\Delta\alpha(n)$ and $\Delta\beta(n)$ can be modeled as sequences of independent and identically-distributed random variables, each of which follows a Gaussian distribution with a standard deviation of σ_{J}. Using this approximation, the errors introduced by clock jitter have a white power spectrum [Che99a].

Table 3.4 defines two continuous-time transfer functions $H_{\mathrm{L_A}}(s)$ and $H_{\mathrm{L_B}}(s)$. Figure 3.10 provides block diagrams for continuous-time $\Delta\Sigma$ modulators that realize these loop transfer functions directly, and Figure 3.11 provides block diagrams for discrete-time $\Delta\Sigma$ modulators that realize equivalent loop transfer functions using the derived error-mapping terms. Note that $H_{\mathrm{L_A}}(s)$ and $H_{\mathrm{L_B}}(s)$ utilize all of the mapping terms in Tables 3.1 and 3.2. The presented modeling technique was validated by simulating the continuous-time architectures shown in Figure 3.10 using the developed Simulink model (Section 3.4.1), simulating the discrete-time architectures shown in Figure 3.11 using the derived error-mapping terms (Section 3.3), and comparing the results of these two approaches.

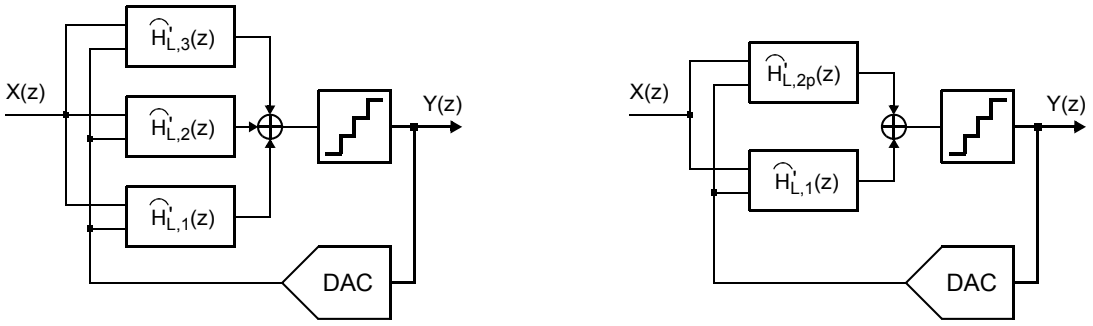
Table 3.4: Test architectures used to validate the modeling technique.

	Loop Transfer Function	DAC Pulse	B	OSR
A	$H_{\mathrm{L_A}}(s) = \frac{b_3}{(sT_{\mathrm{S}})^3} + \frac{b_2}{(sT_{\mathrm{S}})^2} + \frac{b_1}{(sT_{\mathrm{S}})}$	RZ ($\alpha = 0.25$, $\beta = 0.75$)	5	32
B	$H_{\mathrm{L_B}}(s) = \frac{b_{21}(sT_{\mathrm{S}}) + b_{22}}{(sT_{\mathrm{S}})^2 + s_{\mathrm{p}}^2} + \frac{b_1}{(sT_{\mathrm{S}})}$	NRZ ($\alpha = 0.5$, $\beta = 1.5$)	5	16



Architecture A **Architecture B**

Figure 3.10: Block diagrams for the continuous-time ΔΣ modulator architectures in Table 3.4.



Architecture A **Architecture B**

Figure 3.11: Block diagrams for discrete-time ΔΣ modulators that use the error-mapping terms in Tables 3.1 and 3.2 to realize loop transfer functions that are equivalent to those in Table 3.4.

Figure 3.12 plots the simulated SNR of Architectures A and B, specified in Table 3.4, as a function of the normalized clock jitter σ_J. The excellent agreement (to within 1 dB) between these results demonstrates the accuracy of the proposed modeling technique.

3.4.3 Comparison of Simulation Time

The speed advantage of the modeling technique proposed in Section 3.3 is demonstrated by comparing its simulation time to that of the direct Simulink behavioural model presented in Section 3.4.1. In order to optimize the simulation time required by the Simulink model, this section first derives the minimum value of its timing resolution variable N_R.

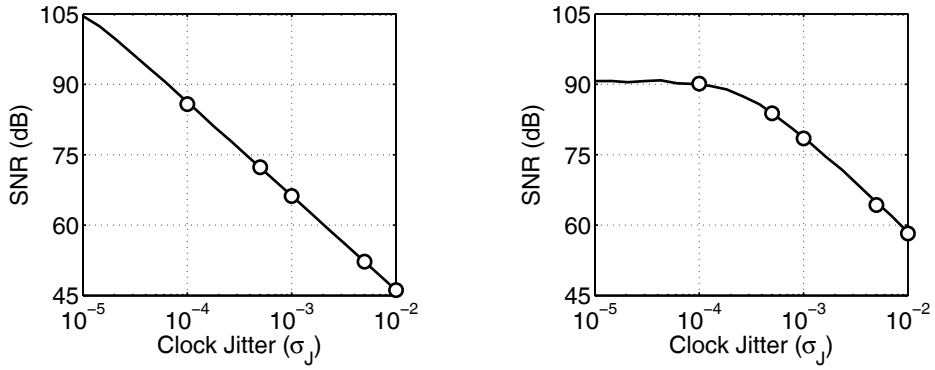


Figure 3.12: The simulated SNR, as a function of the normalized clock jitter, for Architectures A and B specified in Table 3.4. Here, — denotes results derived from the presented modeling technique, and ○ denotes results derived from the Simulink behavioural model.

Timing Resolution

The timing resolution variable N_{R} of the developed Simulink behavioural model (Figure 3.9) determines the minimum time-delay variation that it can represent. Since the high-resolution domain of this model operates at a sampling period of $T_{\mathrm{S}}/N_{\mathrm{R}}$, as described in Section 3.4.1, an increase in the value of N_{R} results in a proportional decrease in the maximum simulation step size. This improves the model accuracy, but also increases the simulation time.

In order to derive the minimum timing resolution that is required to accurately evaluate the effect of time-delay errors, Architecture A in Table 3.4 is simulated using the Simulink behavioural model for different values of N_{R}. Figure 3.13(a) plots the SNR of Architecture A as a function of the normalized timing resolution ($\sigma_{\mathrm{J}} N_{\mathrm{R}}$) for $\sigma_{\mathrm{J}} = 0.01$ and $\sigma_{\mathrm{J}} = 0.001$. This plot demonstrates that $N_{\mathrm{R}} = 2/\sigma_{\mathrm{J}}$ provides sufficient accuracy, independent of σ_{J}.

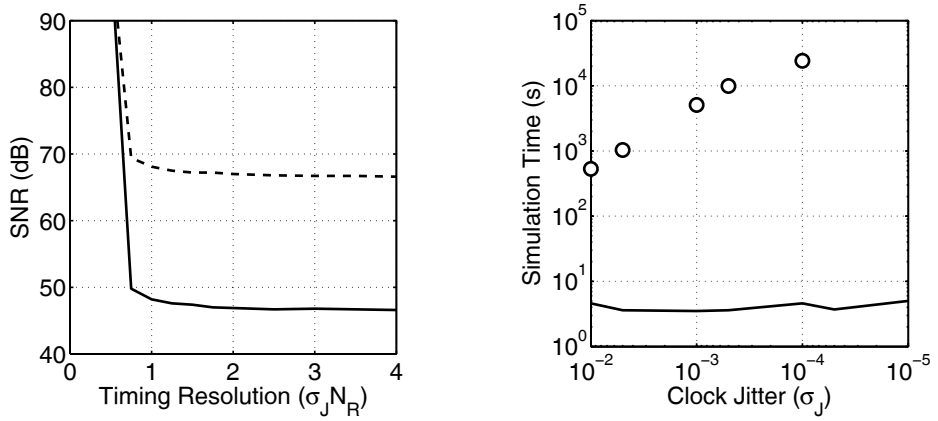


Figure 3.13: (a) The simulated SNR of Architecture A in Table 3.4, as a function of the normalized timing resolution ($\sigma_{\mathrm{J}} N_{\mathrm{R}}$), using the Simulink behavioural model. Here, — denotes $\sigma_{\mathrm{J}} = 0.01$ and - - - denotes $\sigma_{\mathrm{J}} = 0.001$. **(b)** The simulation time required to generate the results shown in Figure 3.12(a). Here, — denotes results derived from the modeling technique presented in Section 3.3 and ○ denotes results derived from the Simulink behavioural model. Each data point in (b) was generated using 2^{16} simulation points and, when using the Simulink behavioural model, each simulation step was divided into $N_{\mathrm{R}}/\sigma_{\mathrm{J}}$ time segments, with N_{R} set to 2.

Simulation Time

Figure 3.13(b) plots the simulation times of the proposed modeling technique (Section 3.3) and the developed Simulink behavioural model (Section 3.4.1) that were required to generate the results in Figure 3.12(a). Here, as the normalized clock jitter variation σ_{J} decreases, the required timing resolution N_{R} of the Simulink behavioural model increases, which increases the associated simulation time. Using the proposed modeling technique, the simulation time remains constant, independent of the jitter variation σ_{J}. As an example, for $\sigma_{\mathrm{J}} = 0.0001$, the Simulink model requires approximately 7 hours to simulate, whereas the proposed modeling technique requires less than a minute. Accordingly, the proposed modeling technique offers a significant speed advantage over direct simulation methods.

3.5 Analysis of Timing Errors

This section uses the modeling technique presented in Section 3.3 to evaluate the performance loss that results from timing errors in the feedback path of a continuous-time $\Delta\Sigma$ modulator. In particular, it analyses the relative ability of different rectangular DAC pulses to minimize the sensitivity of a continuous-time architecture to clock jitter. The analysis examines both lowpass and bandpass $\Delta\Sigma$ modulators, in single-bit and multi-bit configurations.

This analysis considers four different rectangular DAC pulses (Figure 3.14):

1. An NRZ pulse, where the α edge of the *current* clock cycle is equivalent to the β edge of the *previous* clock cycle, such that $\widehat{\alpha}(n) = \widehat{\beta}(n-1) - 1$.

2. An RZ pulse with independent errors $\Delta\alpha(n)$ and $\Delta\beta(n)$ on the α and β edges.

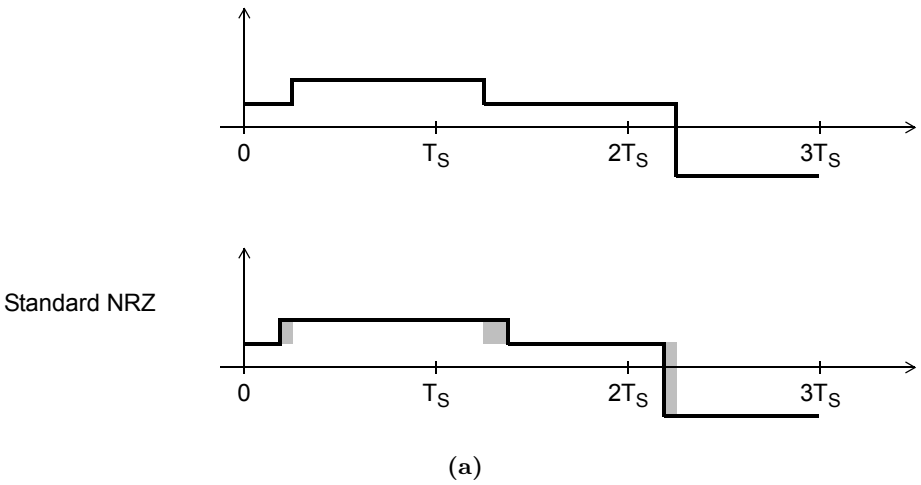
3. An RZ pulse with a fixed *off*-time duration (fixed-off RZ), where the α edge timing of the *current* clock cycle is generated from the β edge timing of the *previous* clock cycle, such that $\Delta\alpha(n) = \Delta\beta(n-1)$ [Pat04].

4. An RZ pulse with a fixed *on*-time duration (fixed-on RZ), where the β edge timing is derived from the α edge timing, such that $\Delta\beta(n) = \Delta\alpha(n)$ [Oli98].

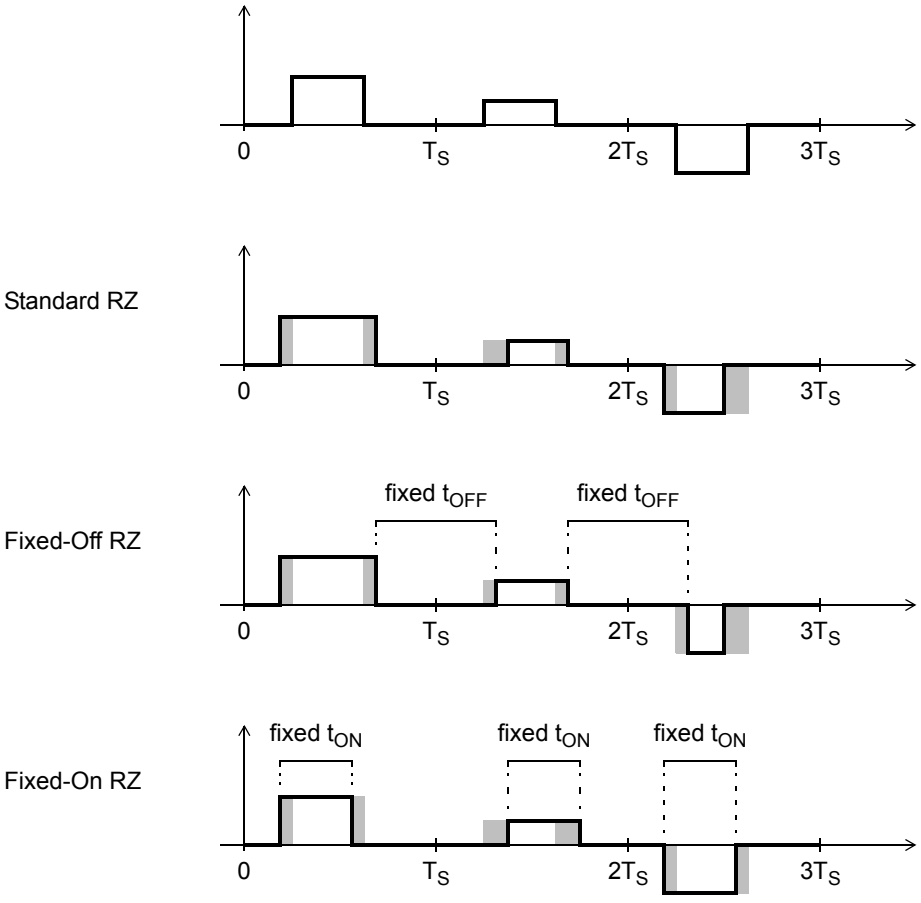
The analysis examines three different continuous-time $\Delta\Sigma$ modulator architectures. The loop transfer function of each architecture is specified in Table 3.5. These test architectures were each simulated using an OSR of 256, so that the jitter-induced errors dominated over the quantization errors in the signal band. The multi-bit configurations were designed with 5-bit internal quantizers and corresponding feedback DACs.

3.5.1 Lowpass $\Delta\Sigma$ Modulators

Figures 3.15(a)–(b) plot the SNR, as a function of the normalized clock jitter, for single-bit and multi-bit configurations of lowpass $\Delta\Sigma$ modulators A and B in Table 3.5. Both pairs of plots include curves for each of the DAC pulses shown in Figure 3.14. This section analyses the results of Figure 3.15 to form general conclusions about the effect of the pulse shape and number of quantization bits on the sensitivity of a lowpass $\Delta\Sigma$ modulator to clock jitter.



(a)



(b)

Figure 3.14: The rectangular DAC pulses that are studied in the analysis. **(a)** An NRZ pulse with ideal timing, and one affected by clock jitter. **(b)** An RZ pulse with ideal timing, and three affected by clock jitter. Here, the effect of timing errors is shown for RZ pulses with: standard timing, a fixed off-time duration, and a fixed on-time duration.

Table 3.5: Test architectures used in the clock-jitter analysis.

	Loop Transfer Function	Error-Mapping Loop Transfer Function
A	$H_{\mathrm{L_A}}(s) = \dfrac{b_3}{(sT_\mathrm{S})^3} + \dfrac{b_2}{(sT_\mathrm{S})^2} + \dfrac{b_1}{(sT_\mathrm{S})}$	$\widehat{H}'_{\mathrm{L_A}}(z) = \dfrac{c_3}{(z-1)^3} + \dfrac{\Delta c_{33}}{(z-1)^3} + \dfrac{\Delta c_{32}}{(z-1)^2} + \dfrac{\Delta c_{31}}{(z-1)} + \dfrac{c_2}{(z-1)^2} + \dfrac{\Delta c_{22}}{(z-1)^2} + \dfrac{\Delta c_{21}}{(z-1)} + \dfrac{c_1}{(z-1)} + \dfrac{\Delta c_{11}}{(z-1)}$
B	$H_{\mathrm{L_B}}(s) = \dfrac{b_{21}(sT_\mathrm{S}) + b_{22}}{(sT_\mathrm{S})^2 + s_\mathrm{p}^2} + \dfrac{b_1}{(sT_\mathrm{S})}$	$\widehat{H}'_{\mathrm{L_B}}(z) = \dfrac{\delta c_{21\mathrm{p}} z - \delta c_{22\mathrm{p}}}{z^2 - 2\,\mathrm{Re}\{z_\mathrm{p}\} + 1} + \dfrac{c_1}{(z-1)} + \dfrac{\Delta c_{11}}{(z-1)}$
C	$H_{\mathrm{L_C}}(s) = \dfrac{b_{21\mathrm{a}}(sT_\mathrm{S}) + b_{22\mathrm{a}}}{(sT_\mathrm{S})^2 + s_{\mathrm{pa}}^2} + \dfrac{b_{21\mathrm{b}}(sT_\mathrm{S}) + b_{22\mathrm{b}}}{(sT_\mathrm{S})^2 + s_{\mathrm{pb}}^2}$	$\widehat{H}'_{\mathrm{L_C}}(z) = \dfrac{\delta c_{21\mathrm{pa}} z - \delta c_{22\mathrm{pa}}}{z^2 - 2\,\mathrm{Re}\{z_{\mathrm{pa}}\} + 1} + \dfrac{\delta c_{21\mathrm{pb}} z - \delta c_{22\mathrm{pb}}}{z^2 - 2\,\mathrm{Re}\{z_{\mathrm{pb}}\} + 1}$

Pulse Shape

In a lowpass ΔΣ modulator, the fixed-on RZ pulse provides the lowest sensitivity to jitter by a significant margin. This result can be explained by examining the equivalent discrete-time loop transfer functions of Architectures A and B in Table 3.5.

- For Architecture A, the equivalent error-mapping transfer function is composed only of terms in Table 3.1. When it is realized in a conventional ΔΣ feedback loop, coefficient error Δc_{31} receives 2nd-order highpass shaping, errors Δc_{21} and Δc_{32} receive 1st-order highpass shaping, and errors Δc_{33}, Δc_{22}, and Δc_{11} do not receive noise shaping. For a fixed-on RZ pulse, $\Delta\alpha = \Delta\beta$, which causes coefficient errors Δc_{33}, Δc_{22}, and Δc_{11} to be reduced to zero (Table 3.1). As a result, the fixed-on RZ pulse provides significantly lower sensitivity to clock jitter than the remaining rectangular pulses [Oli98].

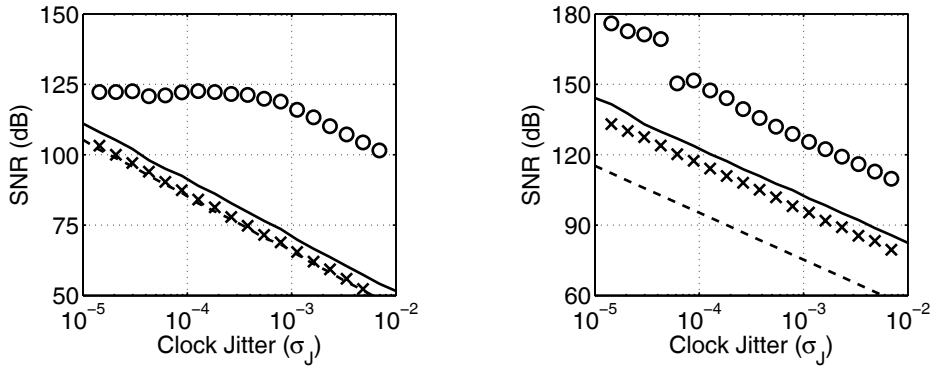
- For Architecture B, the equivalent error-mapping transfer function also includes terms in Table 3.2. When it is realized in a conventional ΔΣ feedback loop, coefficient errors $\delta c_{22\mathrm{p}}$ and $\delta c_{21\mathrm{p}}$ are not shaped. For a fixed-on RZ pulse, $\delta c_{2\mathrm{p}}$ reduces to

$$\delta c_{2\mathrm{p}} \;=\; c_{2\mathrm{p}} z_{\mathrm{p}}^{-\Delta\alpha} \;=\; c_{2\mathrm{p}} e^{-j2\pi(f_{\mathrm{p}}/f_{\mathrm{S}})\Delta\alpha} \tag{3.13}$$

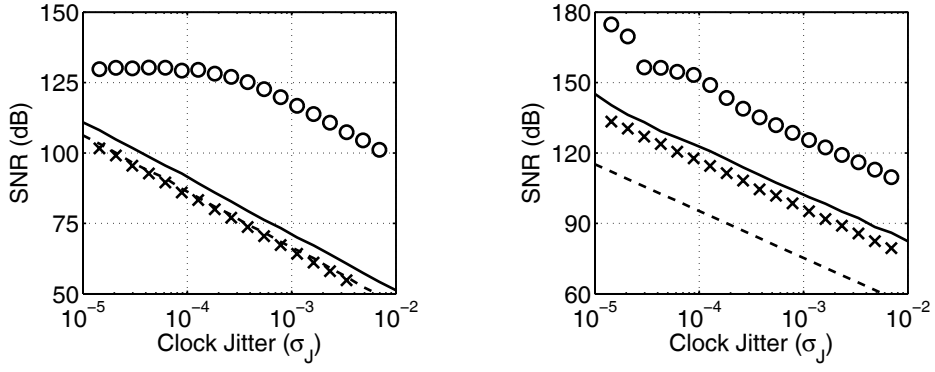
  where f_{S} is the sampling frequency and f_{p} is the frequency of pole z_{p}. In a lowpass ΔΣ modulator, the pole z_{p} is generally placed inside the signal band, and therefore $f_{\mathrm{p}} \ll f_{\mathrm{S}}$ assuming OSR $\gg 1$. Under this condition, coefficient error $\delta c_{2\mathrm{p}}$ approaches its nominal value of $c_{2\mathrm{p}}$. Accordingly, in a lowpass ΔΣ modulator, the fixed-on RZ pulse provides significantly lower sensitivity to clock jitter than the remaining pulses, independent of whether the loop filter includes one or more resonators.

Number of Quantization Bits

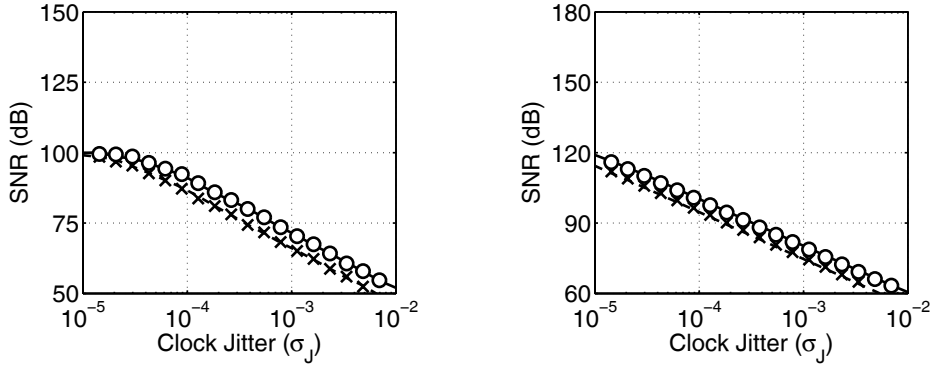
In a lowpass ΔΣ modulator, increasing the number of quantization bits decreases the jitter sensitivity of the NRZ pulse and fixed-off RZ pulse, relative to the standard RZ pulse. This result can be explained as follows.



(a) Architecture A



(b) Architecture B



(c) Architecture C

Figure 3.15: The simulated SNR, as a function of the normalized clock jitter, for: **(a)** a lowpass $\Delta\Sigma$ modulator with three NTF zeros at dc (A in Table 3.5), **(b)** a lowpass $\Delta\Sigma$ modulator with one zero at dc and one pair of complex zeros at the edge of the signal band (B in Table 3.5), and **(c)** a bandpass $\Delta\Sigma$ modulator with one pair of complex zeros at each edge of the signal band (C in Table 3.5). Here, $\bigcirc$ denotes fixed-on RZ, — denotes NRZ, $\times$ denotes fixed-off RZ, and - - - denotes RZ.

The input signal of a lowpass ΔΣ modulator is sampled at least f_S/f_B (i.e., 2OSR) times over its period. Therefore, assuming OSR $\gg 1$, an increase in the number of quantization bits decreases the sample-to-sample variation at the output of the feedback DAC, which reduces the magnitude of the pulse errors that are caused by clock jitter [Gee02]. This decreases the jitter sensitivity of the NRZ pulse and fixed-off RZ pulse, but does not affect the sensitivity of the standard RZ pulse. A fixed-off RZ pulse effectively compensates for errors introduced in the previous clock cycle during the current clock cycle and, therefore, is sensitive to only one pulse edge. In this way, a fixed-off RZ pulse provides performance that is comparable to an NRZ pulse, although approximately 6 dB lower.

3.5.2 Bandpass ΔΣ Modulators

Figure 3.15(c) plots the SNR, as a function of the normalized clock jitter, for single-bit and multi-bit configurations of bandpass ΔΣ modulator C in Table 3.5. Both plots include curves for each of the DAC pulses in Figure 3.14. This section analyses the results of Figure 3.15 to form general conclusions about the effect of the pulse shape and number of quantization bits on the sensitivity of a bandpass ΔΣ modulator to clock jitter.

Pulse Shape

In a bandpass ΔΣ modulator, the fixed-on RZ pulse does not provide an advantage over the remaining pulses. This result can be explained by examining the equivalent discrete-time loop transfer function of Architecture C in Table 3.5.

- For Architecture C, the equivalent error-mapping transfer function is only composed of terms in Table 3.2. When it is realized in a conventional ΔΣ feedback loop, coefficient errors δc_{22p} and δc_{21p} are not shaped. For a fixed-on RZ pulse, δc_{2p} again reduces to the form shown in Equation (3.13). However, in a bandpass ΔΣ modulator, the centre frequency f_C of the signal band, and therefore the frequency f_p of pole z_p, is generally a significant fraction of the sampling frequency f_S (Section 2.3). As a result, coefficient error δc_{2p} remains significant when $\Delta\beta = \Delta\alpha$.

Number of Quantization Bits

In a bandpass $\Delta\Sigma$ modulator, increasing the number of quantization bits does not decrease the jitter sensitivity of the NRZ pulse and fixed-off RZ pulse, as in a lowpass $\Delta\Sigma$ modulator. This result can be explained as follows.

The input signal of a bandpass $\Delta\Sigma$ modulator is only sampled approximately f_S/f_C times over its period, where f_C is generally a significant fraction of f_S (Section 2.3). Therefore, an increase in the number of quantization bits does not reduce the sample-to-sample variation at the output of the feedback DAC, and does not appreciably decrease the magnitude of the pulse errors that are caused by clock jitter. Accordingly, a multi-bit bandpass $\Delta\Sigma$ modulator does not provide lower sensitivity to clock jitter than a single-bit configuration.

3.6 Conclusion

This chapter presented a modeling technique that can be used to rapidly simulate the effect of time-delay errors in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator. The proposed technique is derived from the impulse-invariant transform, and maps *time-delay* errors in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator into *coefficient* errors in the loop filter of an equivalent discrete-time architecture. The proposed technique was applied in this chapter to analyse the effect of different rectangular DAC pulses on the clock jitter sensitivity of both lowpass and bandpass continuous-time $\Delta\Sigma$ modulators.

The simulation results presented in Section 3.4 demonstrated that the proposed modeling technique uses significantly less simulation time than a direct approach, such as the Simulink model described in Section 3.4.1. For example, to simulate the performance loss caused by a normalized jitter variation of $\sigma_J = 0.001$, the Simulink model required approximately 3 hours, whereas the proposed technique required less than a minute (Figure 3.13).

The simulation results presented in Section 3.5 demonstrated that the jitter sensitivity of a lowpass continuous-time $\Delta\Sigma$ modulator can be reduced by using a rectangular DAC pulse with specific timing constraints, such as a fixed on-time, and by using multi-bit quantization.

These results also demonstrated that the jitter sensitivity of a bandpass continuous-time ΔΣ modulator cannot be improved using either of the aforementioned techniques. In a bandpass ΔΣ modulator, all rectangular DAC pulses provide approximately the same jitter sensitivity, and this sensitivity is not reduced using multi-bit quantization.

The clock jitter sensitivity of a bandpass continuous-time ΔΣ modulator can be improved using pulse shaping, as outlined in Section 3.2, however its performance is ultimately limited by the accuracy of the clock signal that is applied to its feedback DAC. The simulation results presented in Section 3.5 demonstrated that, for a given jitter variation, the performance loss due to clock jitter is proportional to the sampling frequency of the ΔΣ modulator. Therefore, for a given centre frequency, the jitter sensitivity of a bandpass architecture can be reduced by decreasing its sampling frequency. This can be achieved by mixing in the ΔΣ loop, which is the approach that is used in a frequency-translating ΔΣ modulator (Section 2.3.1).

Chapter 4

Performance Limitations *of* Image-Reject Frequency-Translating $\Delta\Sigma$ Modulators

THE MOTIVATION for a bandpass $\Delta\Sigma$ modulator that uses frequency downconversion in its feedback loop comes from a desire to digitize high-frequency bandpass signals using low sampling frequencies and low-frequency filters. The *frequency-translating* $\Delta\Sigma$ modulator provides a number of advantages over conventional bandpass $\Delta\Sigma$ modulators, as outlined in Section 2.3. This chapter examines the frequency-translating architecture that was proposed in [Tao99a], which used a hybrid continuous-time/discrete-time loop filter and downconverted its input signal directly to baseband using image-reject mixing. This *image-reject* frequency-translating $\Delta\Sigma$ modulator was later modified in [Pul05] to use a strictly continuous-time loop filter, which enabled it to achieve reduced sensitivity to clock jitter.

This chapter examines the image-reject frequency-translating $\Delta\Sigma$ modulator architecture proposed in [Tao99a]. It outlines a procedure to synthesize this architecture from a prototype discrete-time NTF, and derives a set of design constraints that must be satisfied in order to achieve this synthesis. The derived constraints affect the selection of the timing parameters, and the filtering characteristic of the loop filter. This chapter also examines the performance limitations of an image-reject frequency-translating $\Delta\Sigma$ modulator, specifically its sensitivity to in-phase and quadrature path mismatch.

This chapter is divided into five sections. Section 4.1 provides an overview of image-reject frequency-translating ΔΣ modulators and their design parameters. Section 4.2 describes an NTF synthesis procedure for the image-reject architecture, and develops constraints on both its timing parameters and its loop filter. Section 4.3 presents behavioural simulation results, which demonstrate the importance of the derived constraints. Section 4.4 examines the effect of path mismatch on an image-reject frequency-translating ΔΣ modulator, and discusses its performance limitations. Section 4.5 provides a summary of the chapter.

4.1 Overview

Figure 4.1 shows a block diagram for a frequency-translating ΔΣ modulator that is designed with *image-reject* mixing [Tao99a]. Here, the forward-path mixers (m_{D}) implement frequency downconversion and the feedback-path mixers (m_{U}) implement frequency upconversion. This splits the ΔΣ feedback loop into a high-frequency section and a low-frequency section, where the latter section is divided into an in-phase path and a quadrature path. The high-frequency section of the loop filter is referred to as the outer-loop filter and the low-frequency section is referred to as the inner-loop filter. The *image-reject* frequency-translating ΔΣ modulator in Figure 4.1 has the following design parameters:

- The *input centre frequency* ($f_{\mathrm{C}i}$) is the centre frequency of the signal band at the input of the frequency-translating ΔΣ modulator. It determines the centre frequency of the outer-loop filter (H_{OL}).
- The *LO frequency* (f_{LO}) is generally set to the input centre frequency ($f_{\mathrm{C}i}$) in an image reject architecture. The *sampling frequency* (f_{S}) is then derived from the value of f_{LO} according to certain constraints, which are developed in Section 4.2.1.
- The *sampling delay* (T_{D}) of the quadrature path is similarly derived from the values of f_{LO} and f_{S}, according to the developed constraints.

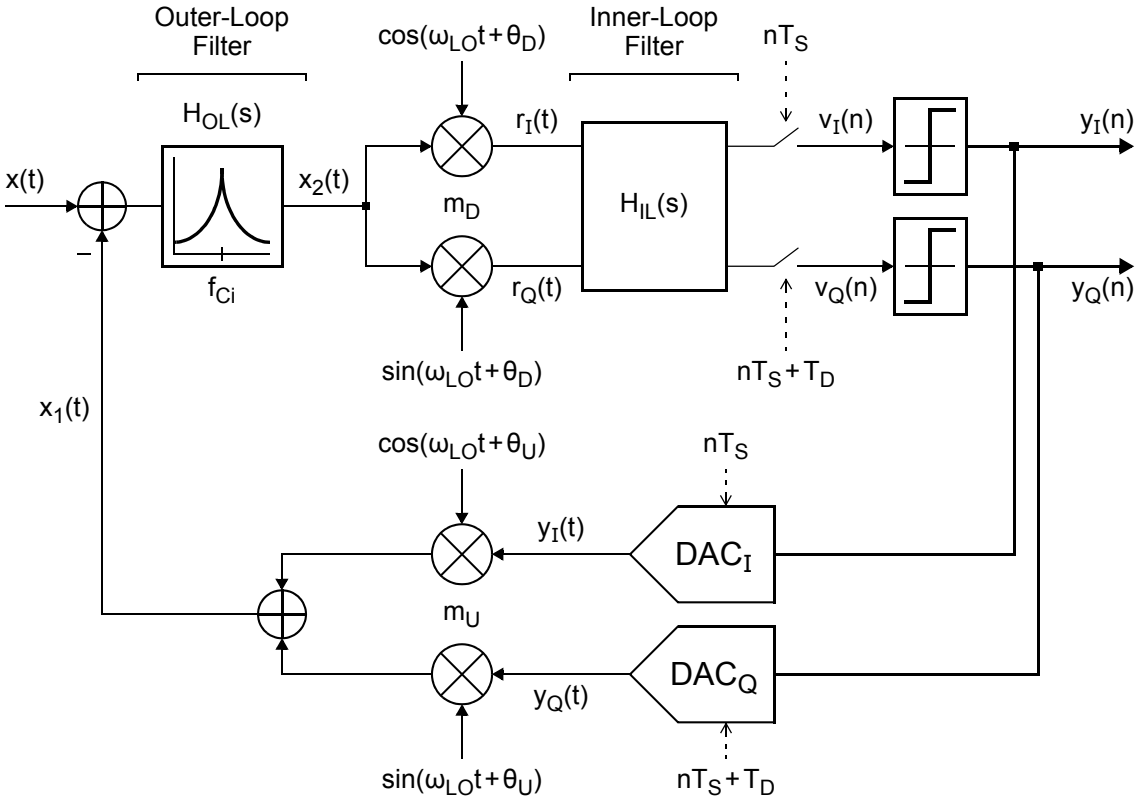


Figure 4.1: Block diagram for an image-reject frequency-translating $\Delta\Sigma$ modulator. Here, T_S is the sampling period, and T_D is the quadrature-path sampling delay.

- The *outer-loop filter* (H_{OL}) and the *inner-loop filter* (H_{IL}) determine the noise-shaping characteristic of the frequency-translating $\Delta\Sigma$ modulator. Section 4.2.2 develops basic constraints on the characteristic of the inner-loop filter.

- The *LO phases* (θ_U and θ_D) modify the response through the loop feedback path of the frequency-translating $\Delta\Sigma$ modulator and, in this way, modify its NTF. The effect of θ_U and θ_D is discussed briefly in Section 4.2, and in greater detail in Section 5.5.

Note that although the sampler is shown after the inner-loop filter $H_{\mathrm{IL}}(s)$ in Figure 4.1, it could also be placed prior to this filter, or between two stages. In such cases, the inner-loop filter is implemented using one or more discrete-time stages.

4.2 NTF Synthesis

The noise-shaping characteristic of an image-reject frequency-translating ΔΣ modulator can be derived from a prototype discrete-time ΔΣ modulator using the same procedure that was outlined in Section 3.1 for a conventional continuous-time architecture. Here, the prototype discrete-time architecture must have a *complex* loop filter in order to replicate the feedback path of an image-reject frequency-translating ΔΣ modulator. Figure 4.2 shows a prototype discrete-time complex ΔΣ modulator. It is important to note that, although the signal paths of the ΔΣ modulators in Figures 4.1 and 4.2 are different, their loop responses, and therefore their noise-shaping characteristics, are equivalent.

Figure 4.3(a) shows the loop feedback path of the image-reject frequency-translating ΔΣ modulator in Figure 4.1, while Figure 4.3(b) shows the loop feedback path of the equivalent discrete-time complex ΔΣ modulator in Figure 4.2.

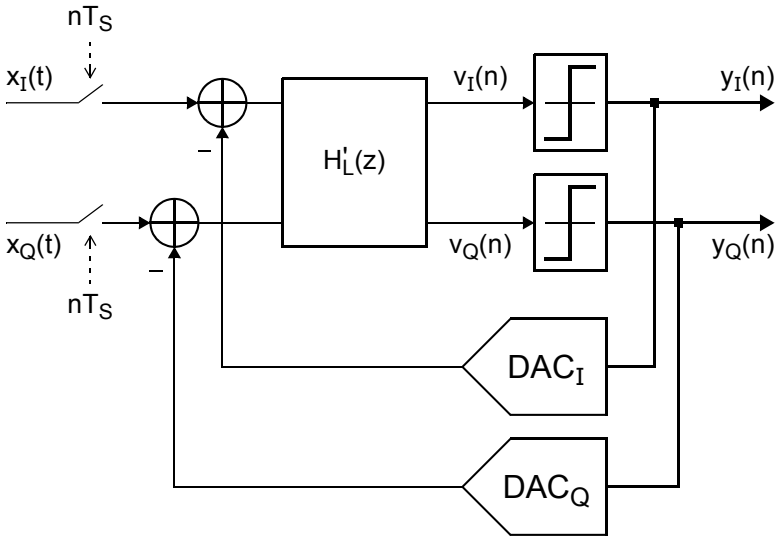
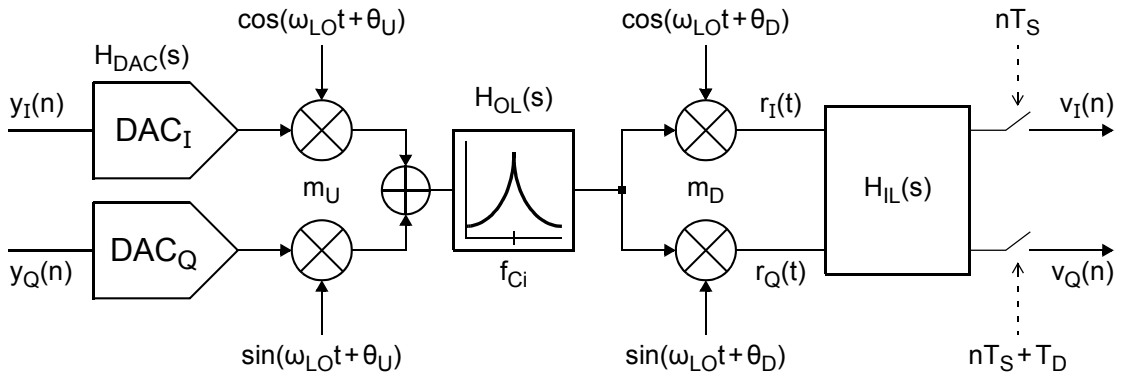
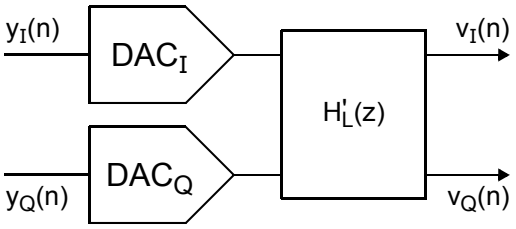


Figure 4.2: Block diagram for a discrete-time ΔΣ modulator with a complex loop filter.



(a)



(b)

Figure 4.3: The loop feedback paths of: **(a)** the image-reject frequency-translating $\Delta\Sigma$ modulator in Figure 4.1, and **(b)** the equivalent discrete-time complex $\Delta\Sigma$ modulator in Figure 4.2.

In order to achieve the same NTF as the prototype discrete-time complex $\Delta\Sigma$ modulator shown in Figure 4.2, the image-reject frequency-translating $\Delta\Sigma$ modulator in Figure 4.1 must provide the same loop response[1] at sampling instants (Section 3.1). This impulse equivalence can be achieved using the impulse-invariant transform, which is defined as

$$\hat{H}_{\mathrm{L}}(s) \;=\; \underset{z \to s}{\mathrm{IIT}}\Big\{ H'_{\mathrm{L}}(z) \Big\} \cdot \frac{1}{H_{\mathrm{DAC}}(s)} \;=\; \underset{z \to s}{\mathrm{IIT}}\left\{ \frac{1}{\mathrm{NTF}(z)} - 1 \right\} \cdot \frac{1}{H_{\mathrm{DAC}}(s)} \tag{4.1}$$

The design of $\mathrm{NTF}(z)$ is discussed in Section 2.1.3.

[1]The term *loop response* is used to refer to the impulse response of the loop feedback path of a $\Delta\Sigma$ modulator, from its output $y(n)$ to the input of its quantizer $v(n)$.

Here, $\hat{H}_{\mathrm{L}}(s)$ is used to represent the *effective* transfer function of the loop feedback path of the image-reject frequency-translating ΔΣ modulator shown in Figure 4.1. This effective loop transfer function combines the transfer functions of the outer-loop filter $H_{\mathrm{OL}}(s)$ and the inner-loop filter $H_{\mathrm{IL}}(s)$, and includes the effect of mixing. Chapter 5 develops an expression for the effective loop transfer function of a frequency-translating ΔΣ modulator.

Due to the use of mixing in the feedback loop of a frequency-translating ΔΣ modulator, the relationship in Equation (4.1) cannot be satisfied without imposing specific constraints on the sampling period T_{S} and the loop transfer function $\hat{H}_{\mathrm{L}}(s)$. Section 4.2.1 discusses the constraints on the timing parameters of an image-reject frequency-translating ΔΣ modulator and Section 4.2.2 discusses the constraints on its inner-loop filter.

4.2.1 Selection of Timing Parameters for Time Invariance

The loop response of a frequency-translating ΔΣ modulator is dependent on the response of its mixers (Section 2.3). Since mixers are time-variant blocks by definition, their introduction into feedback loop of a ΔΣ modulator causes its loop response to also become time-variant. Accordingly, certain constraints must be imposed on the timing of the sampling instants in a frequency-translating ΔΣ modulator to prevent its time-varying loop response from shifting out-of-band quantization noise into the signal band. These *sampling* constraints ensure that the loop response of a frequency-translating ΔΣ modulator is time-invariant after sampling. When the sampled response of a linear time-variant system is time-invariant, it is referred to as a periodically linear time-invariant (PLTI) system [Tao99a].

The in-phase and quadrature sampling instants of the image-reject frequency-translating ΔΣ modulator in Figure 4.1 can be expressed, respectively, as

$$t_n = nT_{\mathrm{S}} \quad \text{and} \quad t_{nd} = nT_{\mathrm{S}} + T_{\mathrm{D}} \tag{4.2}$$

where T_{S} is the sampling period and T_{D} is the delay of the quadrature-path sampling instants relative to the in-phase-path sampling instants.

The required sampling constraints are developed by first evaluating the response through the outer-loop path of the image-reject frequency-translating $\Delta\Sigma$ modulator in Figure 4.1, and then selecting its timing parameters, T_{S} and T_{D}, in such a way that time-varying terms of this response remain constant across all sampling instants.

Following upconversion mixing, the sum of the in-phase and quadrature feedback paths can be expressed as

$$x_1(t) \;=\; y_{\mathrm{I}}(t)\cos(\omega_{\mathrm{LO}}t) + y_{\mathrm{Q}}(t)\sin(\omega_{\mathrm{LO}}t) \tag{4.3}$$

where $y_{\mathrm{I}}(t)$ and $y_{\mathrm{Q}}(t)$ represent the outputs of the in-phase and quadrature feedback DACs, respectively. In order to make the derived equations more tractable, phase terms θ_{U} and θ_{D} in Figure 4.1 have both been set to zero.

The loop response is derived by setting the input signal $x(t)$ to zero. The response of the outer-loop filter in Figure 4.1 is then given by

$$\begin{aligned} x_2(t) \;=\; & \int_{-\infty}^{\infty} h_{\mathrm{OL}}(\tau) y_{\mathrm{I}}(t-\tau)\cos(\omega_{\mathrm{LO}}[t-\tau])\,\mathrm{d}\tau \\ & + \int_{-\infty}^{\infty} h_{\mathrm{OL}}(\tau) y_{\mathrm{Q}}(t-\tau)\sin(\omega_{\mathrm{LO}}[t-\tau])\,\mathrm{d}\tau \end{aligned} \tag{4.4}$$

By expanding the $\cos(\omega_{\mathrm{LO}}[t-\tau])$ and $\sin(\omega_{\mathrm{LO}}[t-\tau])$ terms using standard trigonometric identities, $x_2(t)$ can be rewritten as

$$x_2(t) \;=\; x_{2\mathrm{I}}(t)\cos(\omega_{\mathrm{LO}}t) + x_{2\mathrm{Q}}(t)\sin(\omega_{\mathrm{LO}}t) \tag{4.5}$$

where

$$x_{2\mathrm{I}}(t) \;=\; \big[\, h_{\mathrm{OL}}(t)\cos(\omega_{\mathrm{LO}}t)\,\big] \otimes y_{\mathrm{I}}(t) - \big[\, h_{\mathrm{OL}}(t)\sin(\omega_{\mathrm{LO}}t)\,\big] \otimes y_{\mathrm{Q}}(t) \tag{4.6}$$

$$x_{2\mathrm{Q}}(t) \;=\; \big[\, h_{\mathrm{OL}}(t)\sin(\omega_{\mathrm{LO}}t)\,\big] \otimes y_{\mathrm{I}}(t) + \big[\, h_{\mathrm{OL}}(t)\cos(\omega_{\mathrm{LO}}t)\,\big] \otimes y_{\mathrm{Q}}(t) \tag{4.7}$$

The in-phase and quadrature components in (4.6) and (4.7) are individually time-invariant, however the overall response in (4.5) is time-variant.

The outputs of the downconversion mixers can finally be expressed as

$$r_{\mathrm{I}}(t) \;=\; \frac{1}{2}\,x_{2\mathrm{I}}(t)\big[\,1+\cos(2\omega_{\mathrm{LO}}t)\,\big] + \frac{1}{2}\,x_{2\mathrm{Q}}(t)\sin(2\omega_{\mathrm{LO}}t) \tag{4.8}$$

$$r_{\mathrm{Q}}(t) \;=\; \frac{1}{2}\,x_{2\mathrm{I}}(t)\sin(2\omega_{\mathrm{LO}}t) + \frac{1}{2}\,x_{2\mathrm{Q}}(t)\big[\,1-\cos(2\omega_{\mathrm{LO}}t)\,\big] \tag{4.9}$$

Here, $r_{\mathrm{I}}(t)$ and $r_{\mathrm{Q}}(t)$ are the in-phase and quadrature components of the response through the outer-loop path, given inputs $y_{\mathrm{I}}(t)$ and $y_{\mathrm{Q}}(t)$.

The loop response of the image-reject frequency-translating ΔΣ modulator in Figure 4.1 is time-variant due to the presence of the periodic terms, $\cos(2\omega_{LO}t)$ and $\sin(2\omega_{LO}t)$, in (4.8) and (4.9). Accordingly, it can be designed as a PLTI system by selecting T_{S} and T_{D} in such a way that $\cos(2\omega_{LO}t)$ and $\sin(2\omega_{LO}t)$ remain constant across all sampling instants.

When the in-phase component $r_{\mathrm{I}}(t)$ in (4.8) is sampled at time instants $t_n = nT_{\mathrm{S}}$, with T_{S} set to an integer multiple of $T_{\mathrm{LO}}/2$, $r_{\mathrm{I}}(t_n)$ reduces to $x_{2\mathrm{I}}(t_n)$, and is therefore time-invariant. This constraint on the sampling period can be generalized as

$$T_{\mathrm{S}} \;=\; k_{\mathrm{S}}\,\frac{T_{\mathrm{LO}}}{2}\,, \qquad k_{\mathrm{S}} = 1, 2, 3, \ldots \tag{4.10}$$

When the quadrature component $r_{\mathrm{Q}}(t)$ in (4.9) is sampled at time instants $t_n = nT_{\mathrm{S}}$, with T_{S} selected according to the sampling constraint in (4.10), $r_{\mathrm{Q}}(t_n)$ reduces to 0 in all cases. Since the quadrature LO signal is 90° out-of-phase with the in-phase LO signal, sampling instants in the quadrature path must be delayed by $T_{\mathrm{D}} = T_{\mathrm{LO}}/4$ relative to the in-phase path. When $r_{\mathrm{Q}}(t)$ is sampled at delayed time instants $t_{nd} = nT_{\mathrm{S}} + T_{\mathrm{D}}$, $r_{\mathrm{Q}}(t_{nd})$ reduces to $x_{2\mathrm{Q}}(t_{nd})$, and is therefore time-invariant. Using (4.10), the constraint on the quadrature-path sampling delay can be generalized as

$$T_{\mathrm{D}} \;=\; \frac{1}{k_{\mathrm{S}}}\,\frac{T_{\mathrm{S}}}{2}\,, \qquad k_{\mathrm{S}} = 1, 2, 3, \ldots \tag{4.11}$$

Note that, when applying the constraints in (4.10) and (4.11), the ratio T_D/T_S decreases as the ratio T_S/T_{LO} increases (i.e., as k_S increases). As a result, it is increasingly difficult to accurately realize the quadrature-path sampling delay (T_D). In order to reduce this problem, the constraint in (4.10) is modified such that T_D scales with T_{LO}. This makes it possible to adjust the ratio T_S/T_{LO} without changing the ratio T_D/T_S.

Let the quadrature-path sampling delay be fixed at $T_D = T_S/2$. Consider the case where the sampling period is set to $T_S = T_{LO}/2$ (i.e., for $k_S = 1$). At the quadrature-path sampling instants, $\sin(2\omega_{LO}t_{nd}) = 0$ and $\cos(2\omega_{LO}t_{nd}) = -1$, which yields $r_Q(t_{nd}) = x_{2Q}(t_{nd})$ in (4.9). Figure 4.4(a) plots the $\cos(2\omega_{LO}t)$ term and demonstrates the timing of the quadrature-path sampling instants for $T_S = T_{LO}/2$ and $T_D = T_S/2$. In Figures 4.4(b) and (c), T_S is increased by multiples of $T_{LO}/2$, whereas T_D is fixed at $T_S/2$. Note that $\sin(2\omega_{LO}t_{nd}) = 0$ in both cases. In Figure 4.4(b), $\cos(2\omega_{LO}t_{nd}) = 1$, which yields $r_Q(t_{nd}) = 0$ in (4.9) and demonstrates that $T_S = T_{LO}$ is not a valid design option when $T_D = T_S/2$. In Figure 4.4(c), $\cos(2\omega_{LO}t_{nd}) = -1$, which yields $r_Q(t_{nd}) = x_{2Q}(t_{nd})$ in (4.9) and demonstrates that $3T_S = T_{LO}/2$ is a valid design option when $T_D = T_S/2$.

Therefore, when $T_D = T_S/2$, $r_Q(t_{nd})$ in (4.9) is time-invariant and non-zero only if T_S is an odd multiple of $T_{LO}/2$. This result can be generalized by introducing an additional design factor k_D into the sampling constraint in (4.10) as

$$T_S \;=\; k_D k_S \frac{T_{LO}}{2}\,, \qquad k_D = 1, 3, 5, \ldots \qquad k_S = 1, 2, 3, \ldots \tag{4.12}$$

Using (4.12), the constraint in (4.11) can be rewritten as

$$T_D \;=\; k_D \frac{T_{LO}}{4}\,, \qquad k_D = 1, 3, 5, \ldots \tag{4.13}$$

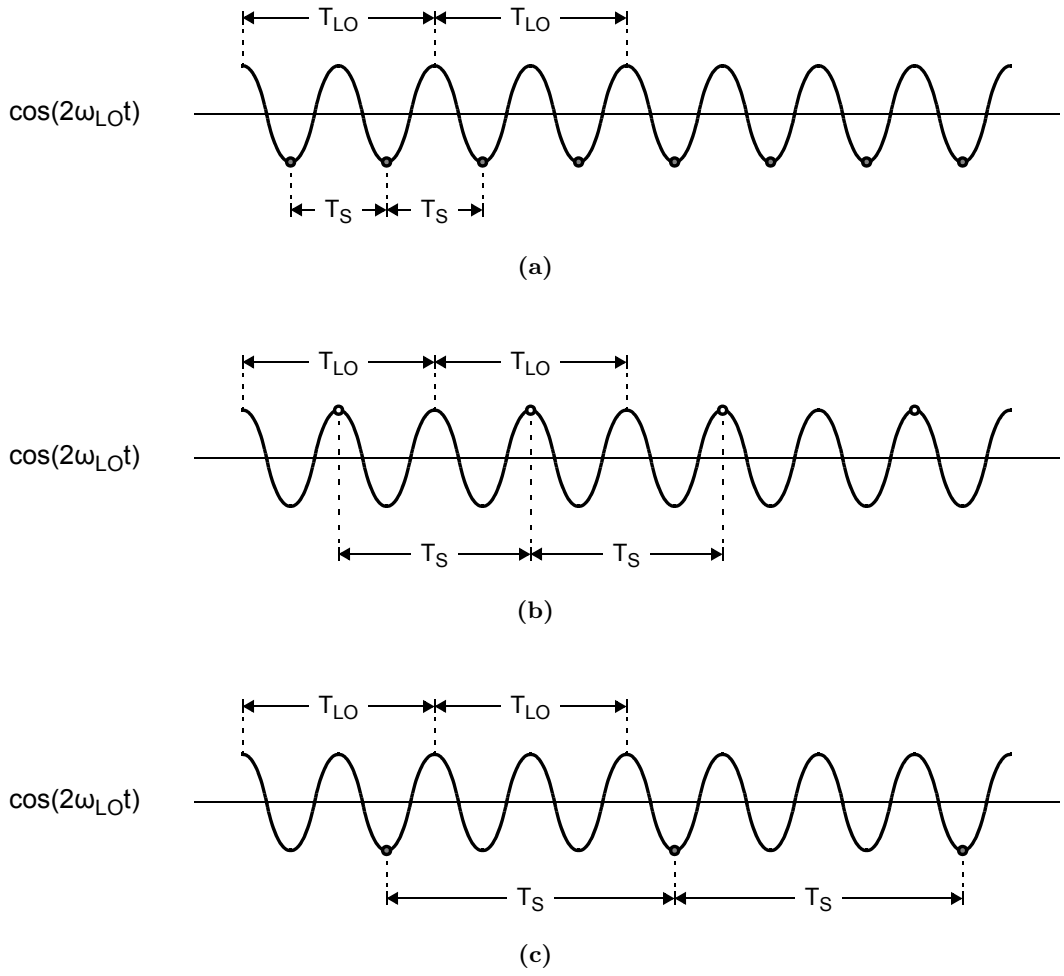


Figure 4.4: Timing of the quadrature-path sampling instants (t_{nd}) for $T_\mathrm{D} = T_\mathrm{S}/2$.

Accordingly, the sampling period of an image-reject frequency-translating ΔΣ modulator must be selected according to (4.12), and the sampling instants in its quadrature path must be delayed according to (4.13). It is important to note that the sampling constraints in (4.12) and (4.13) have been derived independent of the inner-loop filter and can therefore be applied to image-reject frequency-translating ΔΣ modulators with continuous-time or discrete-time, lowpass or complex inner-loop filters. Note, however, that a complex inner-loop filter cannot be implemented using a discrete-time circuit topology, since the cross-coupled feedback paths of a complex integrator cannot be correctly synchronized when the sampling instants of the in-phase and quadrature paths have different delays.

General LO Signals

The constraints in (4.12) and (4.13) have been derived here by assuming that the LO signals have the same phase as the sampling clock (i.e., $\theta_{\mathrm{U}} = 0$ and $\theta_{\mathrm{D}} = 0$ in Figure 4.1). In order to verify that (4.12) and (4.13) are valid beyond this particular case, $r_{\mathrm{I}}(t)$ and $r_{\mathrm{Q}}(t)$ in (4.8) and (4.9) have also been derived for the case that the LO signals have general phases. When the constraints in (4.12) and (4.13) are applied to these revised equations, the sampled response at the output of the downconversion mixers is equal to

$$r_{\mathrm{I}}(t_n) = \cos(\theta_{\mathrm{D}}) \left[\cos(\theta_{\mathrm{U}})\, x_{2\mathrm{I}}(t_n) + \sin(\theta_{\mathrm{D}})\, x_{2\mathrm{Q}}(t_n) \right] \tag{4.14}$$

$$r_{\mathrm{Q}}(t_{nd}) = \cos(\theta_{\mathrm{D}}) \left[\cos(\theta_{\mathrm{U}})\, x_{2\mathrm{I}}(t_{nd}) - \sin(\theta_{\mathrm{D}})\, x_{2\mathrm{Q}}(t_{nd}) \right] \tag{4.15}$$

Here, $r_{\mathrm{I}}(t_n)$ and $r_{\mathrm{Q}}(t_{nd})$ remain time-invariant, but are dependent on LO phases θ_{U} and θ_{D}. The effect of the LO phase on the loop response of a frequency-translating $\Delta\Sigma$ modulator is discussed further in Section 5.3.

Discrete-Time versus Continuous-Time

In an image-reject frequency-translating $\Delta\Sigma$ modulator (Figure 4.1), the output spectrum of the downconversion mixers includes both a low-frequency term, which is centred at dc, and a high-frequency term, which is centred at $2\omega_{\mathrm{LO}}$. When the inner-loop filters are implemented using a conventional discrete-time topology [Tao99a], the in-phase and quadrature paths are sampled immediately after the downconversion mixers. In this case, the high-frequency term is subsampled, and will be subtracted from the low-frequency term if the sampling instants in the quadrature path are not delayed by T_{D}, relative to those of the in-phase path.

In an image-reject frequency-translating $\Delta\Sigma$ modulator with *continuous-time* inner-loop filters [Pul05], the high-frequency term is significantly attenuated by the STF from the output of the downconversion mixers to the input of the quantizer. As a result, it does not affect the low-frequency term during sampling. This inherent STF filtering makes it possible to reduce the quadrature-path sampling delay T_{D} to zero, and to sample the in-phase and quadrature paths at the same instant.

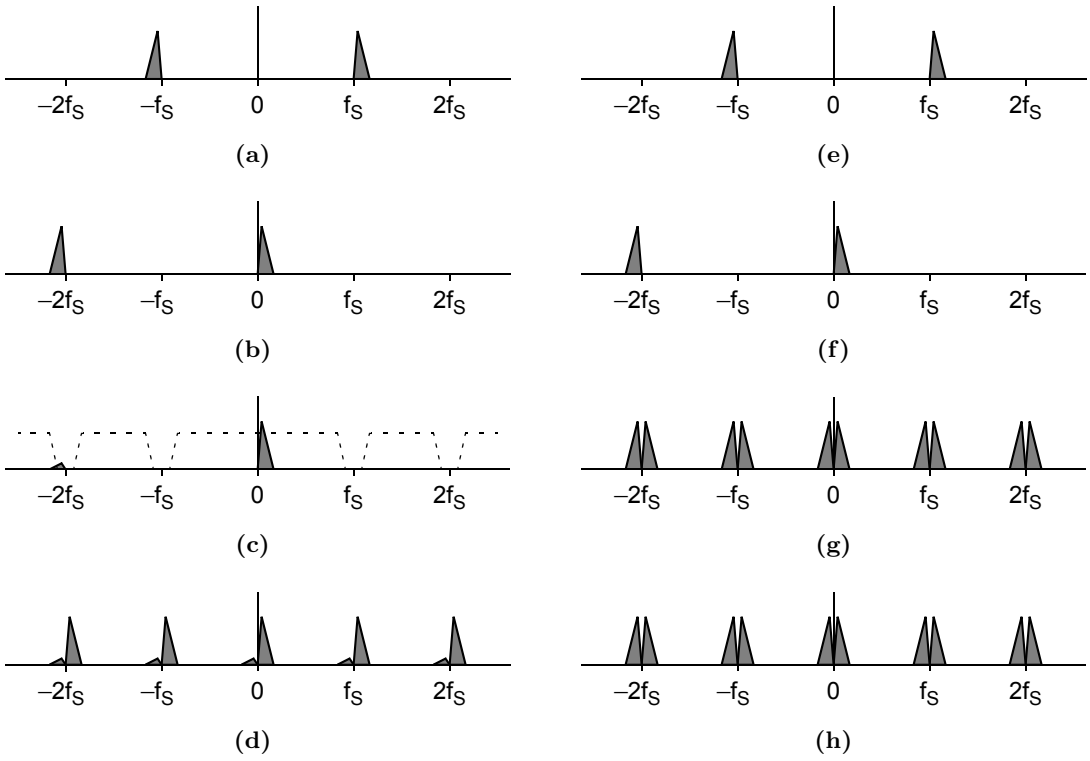


Figure 4.5: (a)–(d) Frequency spectrum at points in the forward path of an image-reject frequency translating ΔΣ modulator (Figure 4.1) with *continuous-time* inner-loop filters and a quadrature-path sampling delay T_{D} of *zero*: **(a)** before the downconversion mixers $x_2(t)$, **(b)** after the downconversion mixers $r(t)$, **(c)** before the sampler $v(t)$, after inherent filtering by the STF, and **(d)** at the output of the ΔΣ modulator $y(n)$. **(e)–(h)** The equivalent plots for an image-reject frequency-translating ΔΣ modulator with *discrete-time* inner-loop filters. In this figure, f_{LO} is set to $3f_{\mathrm{S}}/2$.

Figures 4.5(a)–(d) plot the frequency spectrum at various points in the forward path of an image-reject frequency-translating ΔΣ modulator with *continuous-time* inner-loop filters and a quadrature-path sampling delay T_{D} of zero. Figures 4.5(e)–(h) provide equivalent plots for an image-reject architecture with *discrete-time* inner-loop filters. These figures illustrate how the inherent filtering provided by the STF of a continuous-time loop filter can be used to reduce the quadrature-path sampling delay T_{D} to zero.

4.2.2 Constraints on the Characteristic of the Inner-Loop Filter

In order to achieve stable operation, the feedback loop of a $\Delta\Sigma$ modulator must be designed such that the spectral content of its input signal can be replicated by the spectral content of its feedback signal. As a result, the low-frequency output signal of a frequency-translating $\Delta\Sigma$ modulator must be upconverted into the same band as the high-frequency input signal. In an image-reject frequency-translating $\Delta\Sigma$ modulator (Figure 4.1), this upconversion, and the subsequent in-phase/quadrature path recombination, imposes a basic constraint on the filtering characteristic of the inner-loop filter when the quadrature-path sampling delay T_{D} is set to zero. Note that this section only considers a single value of k_{S} for each configuration, however the results are valid independent of the values of f_{S} and f_{LO}.

Lowpass Inner-Loop Filter

Figures 4.6(a)–(d) plot the frequency spectrum at various points in the feedback path of an image-reject frequency-translating $\Delta\Sigma$ modulator that is designed with a *lowpass* inner-loop filter and a quadrature-path sampling delay T_{D} of $T_{\mathrm{S}}/2$. Here, f_{LO} is equal to $3f_{\mathrm{S}}/2$, and the feedback DAC has a non-return-to-zero (NRZ) pulse, which results in a $\sin(f)/f$ magnitude response that has notches at multiples of f_{S}. Using this design, the signal band contains only the input signal and shaped quantization noise, as illustrated in Figure 4.6(d). Therefore, an image-reject frequency-translating $\Delta\Sigma$ modulator can be correctly designed using a lowpass inner-loop filter when T_{D} is selected according to Equation (4.13).

Figures 4.6(e)–(h) plot the frequency spectrum at the same points in the feedback path of an equivalent frequency-translating $\Delta\Sigma$ modulator that is designed with a quadrature-path sampling delay T_{D} of *zero*. Using this design, the signal band contains an attenuated image in addition to the input signal and shaped quantization noise, as illustrated in Figure 4.6(h). This image is significantly attenuated by the magnitude response of the feedback DAC and, in general, does not limit the resolution. Accordingly, an image-reject frequency-translating $\Delta\Sigma$ modulator can also be correctly designed using a lowpass inner-loop filter when T_{D} is set to zero, as described in Section 4.2.1.

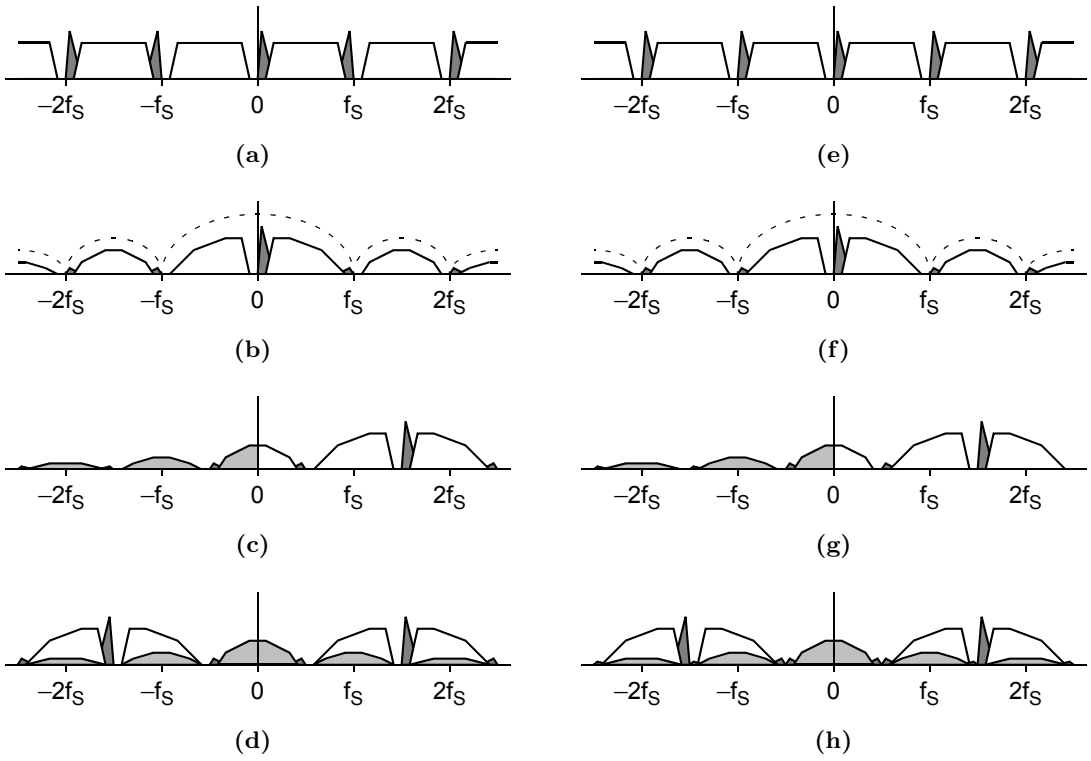


Figure 4.6: (a)–(d) Frequency spectrum at points in the feedback path of an image-reject frequency translating ΔΣ modulator with *lowpass* inner-loop filters and a quadrature-path sampling delay T_{D} of $T_{\mathrm{S}}/2$: **(a)** at the output of the ΔΣ modulator $y(n)$, **(b)** after the feedback DACs $y(t)$, **(c)**–**(d)** after the upconversion mixers and in-phase/quadrature path recombination $x_1(t)$. **(e)**–**(h)** The equivalent spectra for an image-reject frequency-translating ΔΣ modulator with lowpass inner-loop filters and a quadrature-path sampling delay T_{D} of *zero*. In this figure, f_{LO} is set to $3f_{\mathrm{S}}/2$.

Complex Inner-Loop Filter

Figures 4.7(a)–(d) plot the frequency spectrum at various points in the feedback path of an image-reject frequency-translating ΔΣ modulator that is designed with a *complex* inner-loop filter and a quadrature-path sampling delay T_{D} of $T_{\mathrm{S}}/2$. Here, f_{LO} is equal to $3f_{\mathrm{S}}/2$, and the output centre frequency $f_{\mathrm{C}o}$ is equal to $f_{\mathrm{S}}/4$. Using this design, the signal band contains only the input signal and shaped quantization noise, as illustrated in Figure 4.7(d). Therefore, an image-reject frequency-translating ΔΣ modulator can be correctly designed using a complex inner-loop filter when T_{D} is selected according to Equation (4.13).

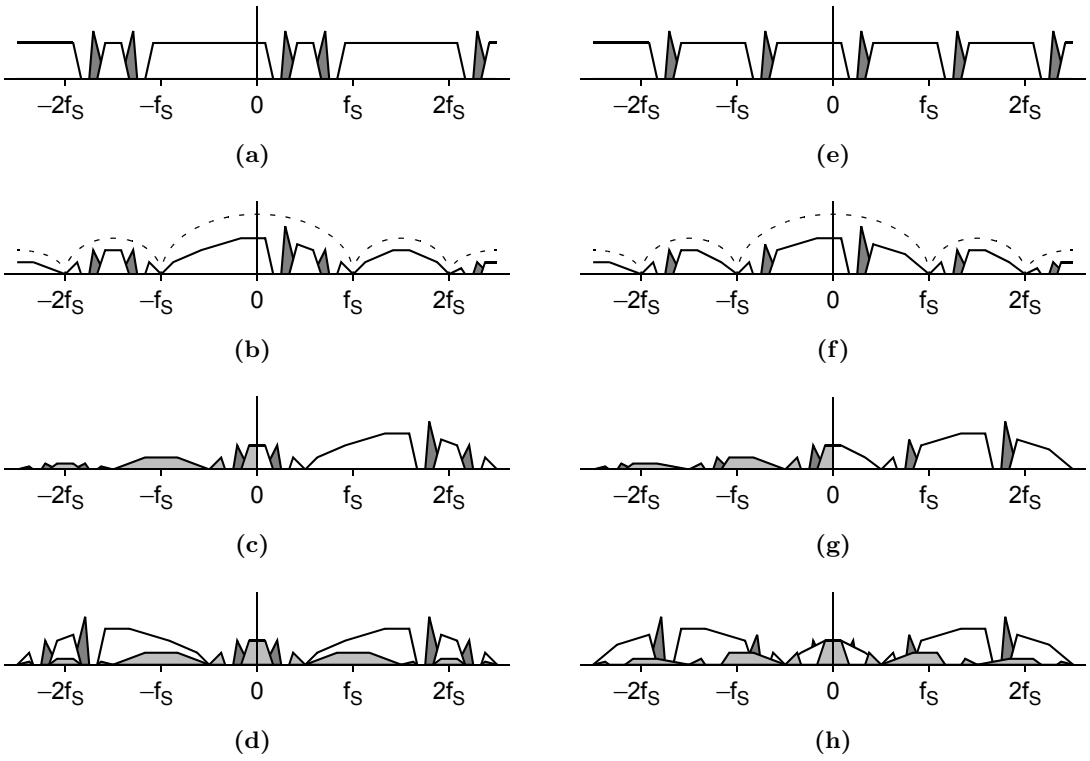


Figure 4.7: (a)–(d) Frequency spectrum at points in the feedback path of an image-reject frequency translating $\Delta\Sigma$ modulator with a *complex* inner-loop filter and a quadrature-path sampling delay T_{D} of $T_{\mathrm{S}}/2$: **(a)** at the output of the $\Delta\Sigma$ modulator $y(n)$, **(b)** after the feedback DACs $y(t)$, **(c)**–**(d)** after the upconversion mixers and in-phase/quadrature path recombination $x_1(t)$. **(e)**–**(h)** The equivalent spectra for an image-reject frequency-translating $\Delta\Sigma$ modulator with a complex inner-loop filter and a quadrature-path sampling delay T_{D} of *zero*. In this figure, f_{LO} is set to $3f_{\mathrm{S}}/2$.

Figures 4.7(e)–(h) plot the frequency spectrum at the same points in the feedback path of an equivalent frequency-translating $\Delta\Sigma$ modulator that is designed with a quadrature-path sampling delay T_{D} of *zero*. Using this design, quantization noise in the image band, which is centred at $-7f_{\mathrm{S}}/4$ in Figure 4.7(g), is mirrored into the signal band during the in-phase and quadrature path recombination, as illustrated in Figure 4.7(h). As a result, an image-reject frequency-translating $\Delta\Sigma$ modulator with a complex inner-loop filter and a quadrature-path sampling delay T_{D} of zero must have additional filtering prior to its upconversion mixers in order to attenuate quantization noise in its image band.

4.3 Behavioural Simulations

This section provides behavioural simulation results that demonstrate the importance of the constraints derived in Section 4.2. Figure 4.8 shows a block diagram for the test image-reject frequency-translating ΔΣ modulator architecture that is considered here. It has a 2nd-order continuous-time outer-loop filter, and 1st-order discrete-time lowpass inner-loop filters in its in-phase and quadrature paths. In addition, it has a single-bit quantizer in each path, and a corresponding feedback DAC.

Since the test architecture is designed with *lowpass* inner-loop filters, it downconverts its input signal directly to baseband. Therefore, the centre frequency of its outer-loop filter and the frequency of its LO signal f_{LO} are both set to its input centre frequency f_{Ci}. Its sampling period T_{S} and its quadrature-path sampling delay T_{D} are then modified for each test case. In this section, with the exception of the errors under consideration, all simulation parameters are set to their ideal values.

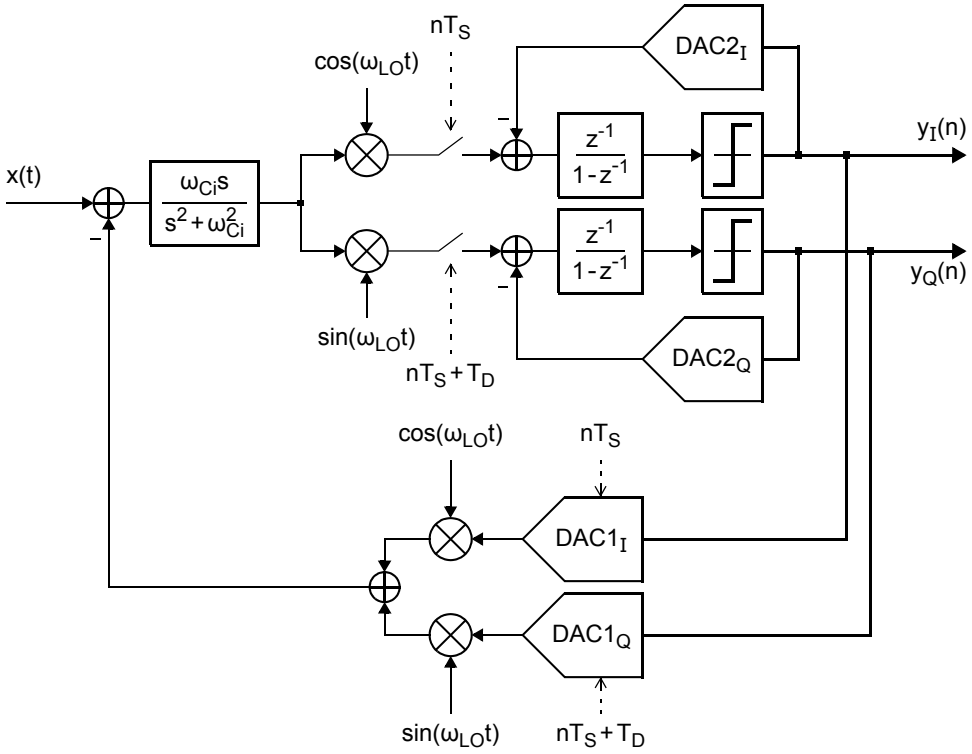


Figure 4.8: A test image-reject frequency-translating ΔΣ modulator architecture.

Figure 4.9(a) plots the output spectrum of the test architecture (Figure 4.8) for the case that $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$. Here, $k_S = 1$ and $k_D = 3$, which satisfy the constraints in Equations (4.12) and (4.13), and produce the correct output. In Figure 4.9(b), T_S is changed to $3.25\,T_{LO}/2$, which violates the constraint in Equation (4.12) and causes the loop response of the test architecture to be time-variant. This reduces the noise-shaping performance, and introduces additional signal tones into the output, in particular at $0.25f_S$. In Figure 4.9(c), T_S is set to $3.5\,T_{LO}/2$, which again decreases the noise-shaping performance, and introduces additional signal tones, in particular at $0.5f_S$.

Figure 4.10(a) plots the output spectrum of the test architecture (Figure 4.8) for the case that $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$, as outlined above. In Figure 4.10(b), the sampling delay of the quadrature path T_D is set to $0.95\,T_S/2$, which violates the constraint in Equation (4.13). This creates a mismatch between the in-phase and quadrature paths of the test architecture, and introduces a significant image tone at its output. In Figure 4.10(c), T_D is set to 0, which reduces the output of the test architecture to a real spectrum.

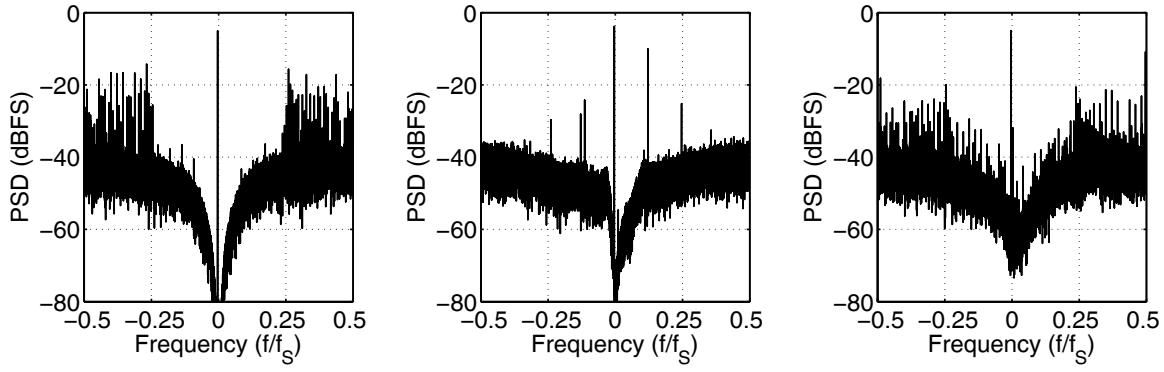


Figure 4.9: The output spectrum of the test architecture shown in Figure 4.8, when it is designed with: **(a)** $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$, **(b)** $T_S = 3.125\,T_{LO}/2$ and $T_D = T_S/2$, and **(c)** $T_S = 3.5\,T_{LO}/2$ and $T_D = T_S/2$. Here, the configuration in (a) satisfies the constraints in Equations (4.12) and (4.13), whereas those in (b) and (c) violate the constraint in Equation (4.12).

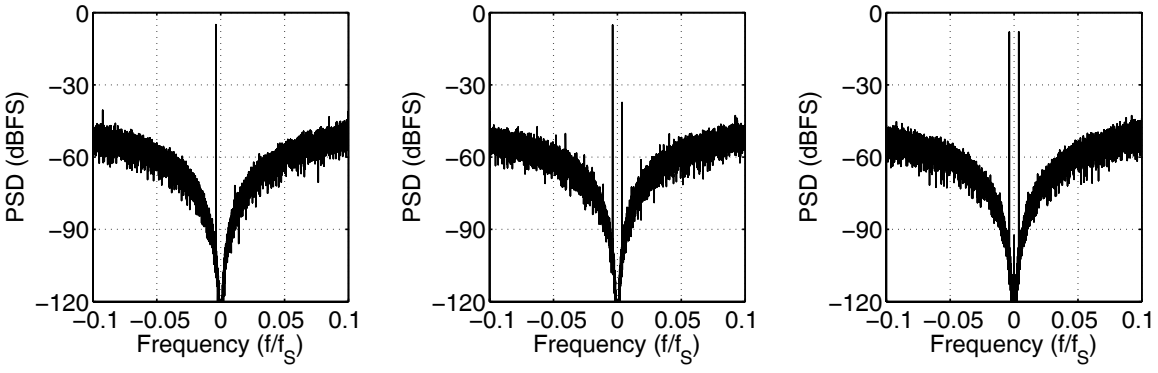


Figure 4.10: The output spectrum of the test architecture shown in Figure 4.8, when it is designed with: **(a)** $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$, **(b)** $T_S = 3\,T_{LO}/2$ and $T_D = 0.95\,T_S/2$, and **(c)** $T_S = 3\,T_{LO}/2$ and $T_D = 0$. Here, the configuration in (a) satisfies the constraints in Equations (4.12) and (4.13), whereas those in (b) and (c) violate the constraint in Equation (4.13).

4.4 Performance Limitations

This section examines the performance limitations of the image-reject frequency-translating ΔΣ modulator in Figure 4.1, in particular its sensitivity to mismatch. Section 4.4.1 examines the effect of phase mismatch in the LO signals and time-delay mismatch in the responses of the feedback DACs, and Section 4.4.2 examines the effect of amplitude mismatch in the LO signals. In this section, with the exception of the errors under consideration, all simulation parameters are set to their ideal values.

4.4.1 Phase and Delay Mismatch

In a frequency-translating ΔΣ modulator (Figure 4.1), timing errors can be introduced into the forward path, at the downconversion mixers and the sampler, and into the feedback path, at the upconversion mixers and the feedback DACs. Section 4.3 examined the effect of errors in the sampling period T_S and the quadrature-path sampling delay T_D. This section looks at the effect of phase mismatch in the LO signals and time-delay mismatch in the DACs.

Figures 4.11 and 4.12 plot the output spectrum of the test architecture in Figure 4.8 for the case that $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$, both of which satisfy the constraints derived in Section 4.2. In Figure 4.11(a), a phase error of 0.0015π is introduced into the LO signal that is applied to the quadrature mixer in the *feedback* path of the test architecture. This results in a mismatch between the in-phase and quadrature paths, which introduces an image tone into the output spectrum. In Figure 4.12(a), the same error is introduced at the quadrature mixer in the *forward* path of the test architecture. Although this also results in a mismatch, the associated image tone is suppressed by the gain of the outer-loop filter. Accordingly, the phase mismatch of the forward-path mixers has less of an effect on the resolution than that of the feedback-path mixers. Figures 4.11(b) and 4.12(b) plot equivalent results for a phase error of 0.015π. Here, the mismatch of the forward-path mixers is again suppressed, however it still has a significant effect on the performance.

Figure 4.13 plots the output spectrum of the test architecture in Figure 4.8 for the case that $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$, as outlined above. In Figure 4.13(a), a time-delay error of $0.0005\,T_S$ is introduced into the response of the quadrature-path feedback DAC. This delay error is equivalent[2] to the phase error simulated in Figure 4.11(a), however it introduces less mismatch into the feedback path. Figure 4.13(b) shows a comparable result for a delay error of $0.05\,T_S$. Since the test architecture is designed with lowpass inner-loop filters (Figure 4.8), and downconverts its input signal directly to baseband, its loop response approximates that of a lowpass $\Delta\Sigma$ modulator [Pul05]. As a result, it has similar sensitivity to time-delay errors in its DAC. Section 3.5.1 demonstrated that a lowpass $\Delta\Sigma$ modulator has low sensitivity to time-delay errors in its feedback DAC using the example of clock jitter.

4.4.2 Amplitude Mismatch

In an image-reject frequency-translating $\Delta\Sigma$ modulator (Figure 4.1), amplitude mismatch is introduced primarily by the LO signals, the feedback DACs, and the coefficients of the inner-loop filters. This section only examines the impact of amplitude mismatch in the LO signals, however the results are representative of DAC and coefficient mismatch.

[2]Here, a phase error ($\Delta\theta$) and a time-delay error (Δt) are considered to be equivalent if $\Delta\theta = \omega_{LO}\Delta t$.

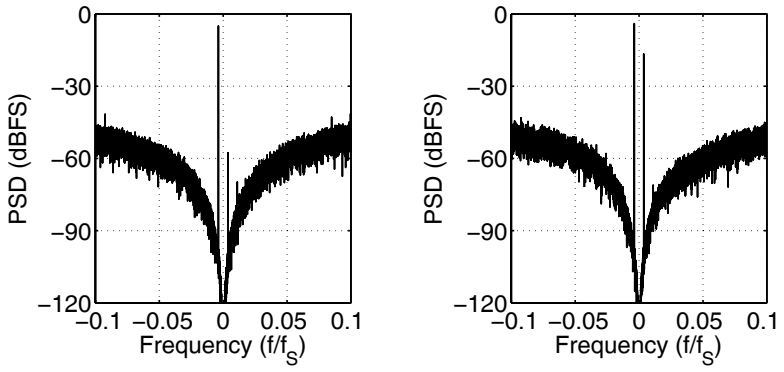


Figure 4.11: The output spectrum of the test architecture shown in Figure 4.8, when it is designed with $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$. Here, a phase error of $\Delta\theta$ is introduced into the LO signal that is applied to the quadrature mixer in the *feedback* path, where: **(a)** $\Delta\theta = 0.0015\pi$, and **(b)** $\Delta\theta = 0.15\pi$.

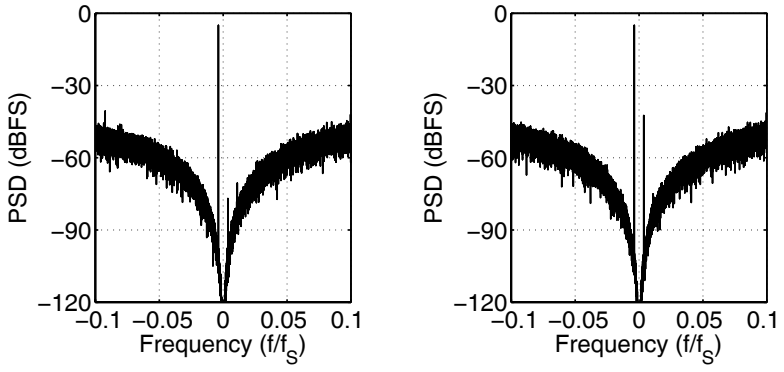


Figure 4.12: The output spectrum of the test architecture shown in Figure 4.8, when it is designed with $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$. Here, a phase error of $\Delta\theta$ is introduced into the LO signal that is applied to the quadrature mixer in the *forward* path, where: **(a)** $\Delta\theta = 0.0015\pi$, and **(b)** $\Delta\theta = 0.15\pi$.

Figure 4.14 plots the output spectrum of the test architecture in Figure 4.8 for the case that $T_S = 3\,T_{LO}/2$ and $T_D = T_S/2$, as described above. In Figure 4.14(a), the LO signal that is applied to the quadrature mixer in the *feedback* path of the test architecture is scaled by a factor of 0.995. This amplitude error is equivalent[3] to the phase error in Figure 4.10(a), and results in approximately the same mismatch. In Figure 4.14(b), the same error is introduced

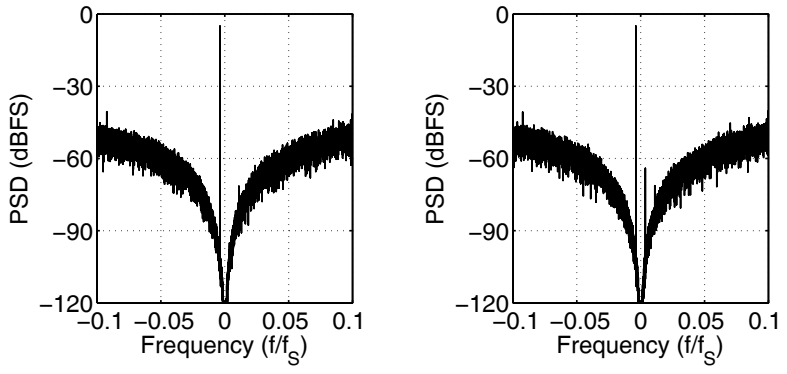


Figure 4.13: The output spectrum of the test architecture shown in Figure 4.8, when it is designed using $T_{\mathrm{S}} = 3\,T_{\mathrm{LO}}/2$ and $T_{\mathrm{D}} = T_{\mathrm{S}}/2$. Here, a time-delay error of Δt is introduced into the response of the quadrature-path feedback DAC, where: **(a)** $\Delta t = 0.0005\,T_{\mathrm{S}}$, and **(b)** $\Delta t = 0.05\,T_{\mathrm{S}}$.

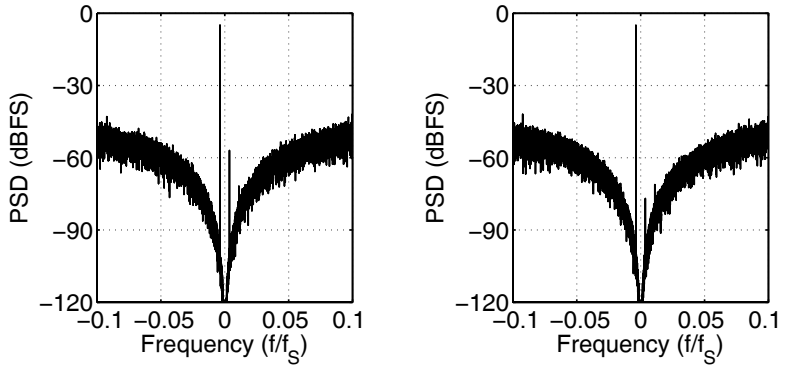


Figure 4.14: The output spectrum of the test architecture shown in Figure 4.8, when it is designed with $T_{\mathrm{S}} = 3\,T_{\mathrm{LO}}/2$ and $T_{\mathrm{D}} = T_{\mathrm{S}}/2$. Here, an amplitude error of 0.5 % is introduced into the LO signal that is applied to the quadrature mixer of: **(a)** the feedback path, and **(b)** the forward path.

at the quadrature mixer in the *forward* path of the test architecture. Here, as in Figures 4.10 and 4.11, the mismatch error of the forward path is suppressed, whereas that of the feedback path is added directly to the input signal.

[3]Here, a phase error ($\Delta\theta$) and an amplitude error (ΔA) are equivalent if $\left|1-\Delta A\right| = \left|1-\mathrm{e}^{-j\,\Delta\theta}\right|$ [Mar04].

4.5 Conclusion

This chapter investigated the image-reject frequency-translating ΔΣ modulator architecture proposed in [Tao99a]. It outlined a procedure to synthesize the image-reject architecture from a prototype discrete-time complex ΔΣ modulator, and derived a set of constraints that must be satisfied to achieve this synthesis. The derived constraints limit the selection of the timing parameters and the characteristic of the loop filter. The importance of these constraints was demonstrated using simulation results, which are shown in Figures 4.9 and 4.10.

The constraints on an image-reject frequency-translating ΔΣ modulator (Figure 4.1) can be summarized as follows:

- The sampling period T_S must be an integer multiple of $T_{LO}/2$, where T_{LO} is the period of the LO signal. This constraint is required to ensure that the sampled response of the ΔΣ feedback loop is time-invariant (Section 4.2.1).
- A delay T_D is required between the sampling instants of the in-phase and quadrature paths. The value of this delay depends on T_S and T_{LO}, and can be reduced to zero when the inner-loop filter has a continuous-time circuit topology (Section 4.2.1).
- The inner-loop filter can have a lowpass or complex characteristic. However, a complex inner-loop filter can only be implemented using a continuous-time circuit topology, and can require additional filtering in the feedback path (Section 4.2.2).

This chapter further examined the performance limitations of the image-reject frequency translating ΔΣ modulator, focusing on its sensitivity to path mismatch. Section 4.4 provided simulation results for the effect of phase and amplitude mismatch, as shown in Figures 4.11, 4.12, and 4.14, and demonstrated that both can significantly reduce the performance of the image-reject frequency-translating ΔΣ modulator. This mismatch problem can be solved by using *single-path* mixing in a frequency-translating ΔΣ modulator, rather than image-reject mixing. The single-path architecture is presented in the next chapter.

Chapter 5

A Novel Single-Path Frequency-Translating $\Delta\Sigma$ Modulator

DOWNCONVERSION mixing can be achieved using two different approaches: image-reject and single-path. An image-reject mixing process uses in-phase and quadrature phases of an LO signal to generate a complex output spectrum, which is defined over $f \in [-\infty, \infty]$. A single-path mixing process uses one LO phase to generate a real output spectrum, which is defined over $f \in [0, \infty]$. Chapter 4 investigated the limitations of a frequency-translating $\Delta\Sigma$ modulator architecture that is based on image-reject mixing [Tao99a]. This chapter presents the design procedure for a frequency-translating $\Delta\Sigma$ modulator that is based on single-path mixing [Cho11]. The primary advantage of the single-path architecture, over an image-reject architecture, is that it eliminates the potential for path mismatch introduced by phase, delay, and amplitude errors (Section 4.4).

This chapter first describes a procedure to synthesize a single-path frequency-translating $\Delta\Sigma$ modulator from a prototype discrete-time NTF, and develops a set of design constraints that are required to achieve this synthesis. It then discusses the realization of the loop filter, and develops an effective transfer function for the high-frequency, or *outer-loop* path, and an optimal configuration for the low-frequency, or *inner-loop* filter.

This chapter is organized into seven sections. Section 5.1 gives an overview of single-path frequency-translating ΔΣ modulators and describes their advantages relative to image-reject architectures. Section 5.2 outlines a synthesis procedure for the single-path architecture and derives constraints for its timing parameters and loop filter. Sections 5.3 and 5.4 discuss the realizations of the outer-loop filter and inner-loop filter, as described above, and Section 5.5 discusses the LO phase dependence of the NTF. Section 5.6 presents a technique to plot the effective STF of a single-path frequency-translating ΔΣ modulator, and develops additional design equations. Section 5.7 provides a summary of the chapter.

5.1 Overview

Figure 5.1 shows a block diagram for a frequency-translating ΔΣ modulator that is designed with *single-path* mixing [Cho11]. Here, the forward-path mixer (m_{D}) implements frequency downconversion, and the feedback-path mixer (m_{U}) implements frequency upconversion. This splits the ΔΣ feedback loop into a high-frequency section and a low-frequency section, where the high-frequency section of the loop filter is referred to as the outer-loop filter, and the low frequency section is referred to as the inner-loop filter. The *single-path* frequency-translating ΔΣ modulator in Figure 5.1 has the following design parameters:

- The *input* and *output centre frequencies* ($f_{\mathrm{C}i}$ and $f_{\mathrm{C}o}$) are the centre frequencies of the signal band at the input and output of the frequency-translating ΔΣ modulator. They determine the centre frequencies of its filters (H_{OL} and H_{IL}).
- The *LO frequency* (f_{LO}) determines the frequency separation between $f_{\mathrm{C}i}$ and $f_{\mathrm{C}o}$. Its value is selected, in conjunction with the *sampling frequency* (f_{S}), according to certain constraints, which are derived in Section 5.2.
- The *outer-loop filter* (H_{OL}) and the *inner-loop filter* (H_{IL}) determine the noise-shaping characteristic of the frequency-translating ΔΣ modulator. Their design is discussed in Sections 5.3 and 5.4, respectively.

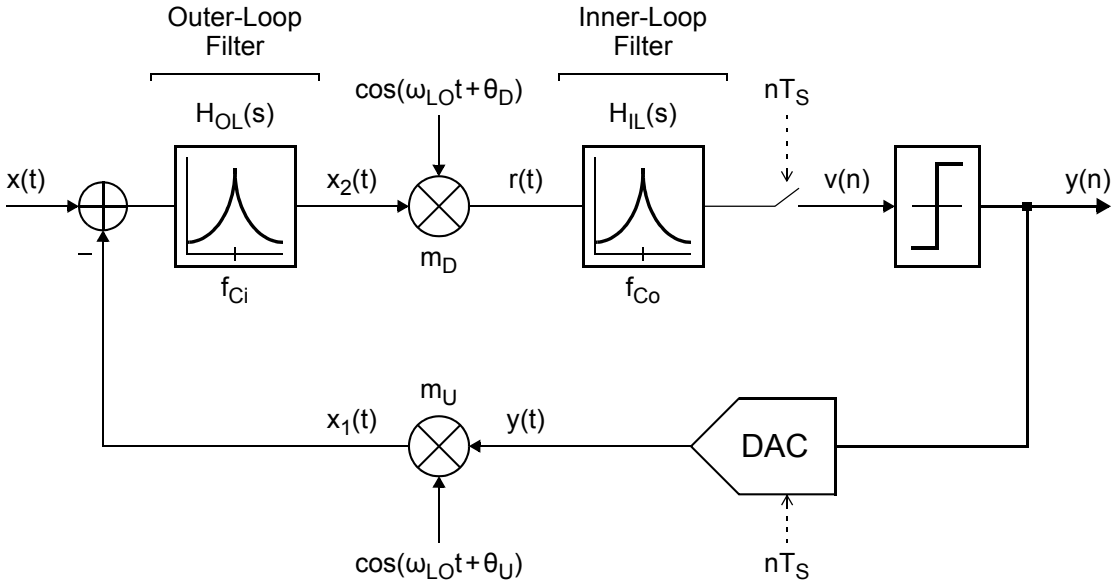


Figure 5.1: Block diagram for a single-path frequency-translating $\Delta\Sigma$ modulator.

- The *LO phases* (θ_{U} and θ_{D}) modify the response through the loop feedback path of the frequency-translating $\Delta\Sigma$ modulator and, in this way, modify its NTF. The selection of θ_{U} and θ_{D} is discussed in Section 5.5.

Comparison to the Image-Reject Architecture

The single-path frequency-translating $\Delta\Sigma$ modulator eliminates the path mismatch that can limit the resolution of the image-reject architecture. The trade-off for this advantage is that the signal transfer function (STF) of a single-path frequency-translating $\Delta\Sigma$ modulator does not provide the same degree of inherent filtering as that of an image-reject architecture.

Path Mismatch

The resolution of an image-reject frequency-translating ΔΣ modulator is limited by mismatch in its in-phase and quadrature paths. This path mismatch is caused by amplitude and phase errors in its LO signals, delay errors in its sampling clock, and scaling errors in its functional blocks. In an image-reject architecture, path mismatch introduces images of the input signal into the feedback and forward paths at the upconversion and downconversion mixers. In the feedback path, images are added directly to the input signal, and can significantly reduce the resolution of the ΔΣ modulator. In the forward path, images receive limited suppression by the outer-loop filter, and can still reduce the performance. Section 4.4 provided behavioural simulations that illustrate the effect of path mismatch on the performance of an image-reject frequency-translating ΔΣ modulator.

A single-path frequency-translating ΔΣ modulator only uses one phase of the LO signal, and is not affected by path mismatch. This enables it to achieve significantly lower sensitivity to amplitude and phase errors in the LO signal than an image-reject architecture.

It is important to note how the image of an image-reject architecture differs from that of a single-path architecture. In an image-reject architecture, images are caused by mismatch in the timing signals and in the functional blocks. These images are generated *inside* the signal band and limit the resolution of the ΔΣ modulator. In a single-path architecture, images are inherent to the mixing process. These images are generated *outside* the signal band and only result in signal-swing issues that can be resolved in the system-level design.

Inherent Filtering

In order to operate on high-frequency signals, the outer-loop filter of a frequency-translating ΔΣ modulator must be implemented using a continuous-time circuit topology (Section 2.3). As a result, the STF of a frequency-translating ΔΣ modulator always provides some degree of inherent filtering (Section 2.1.2). Figure 5.2 plots the STF of an image-reject architecture, and that of a single-path architecture. Here, although both architectures provide significant attenuation at aliases of their signal band, the STF of the single-path frequency-translating ΔΣ modulator provides limited attenuation within its image band.

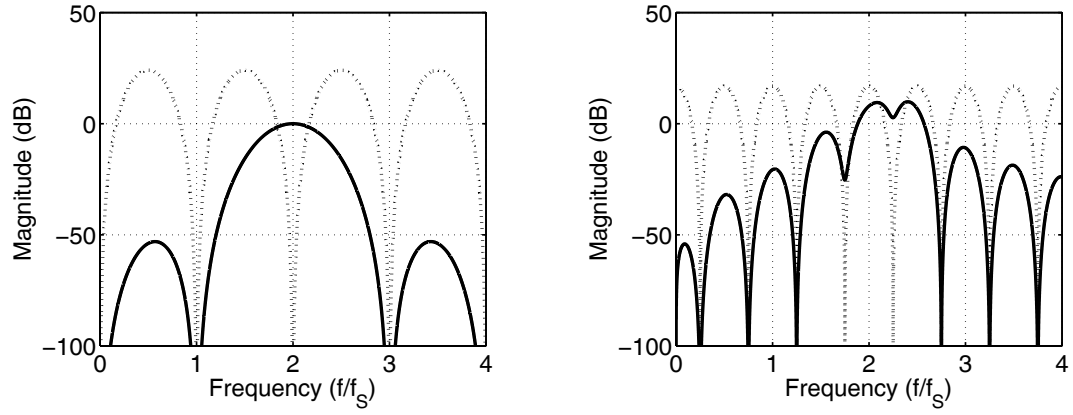


Figure 5.2: Simulated STF and NTF of: **(a)** an image-reject frequency-translating $\Delta\Sigma$ modulator with $f_{Ci} = 2f_S$, and **(b)** a single-path frequency-translating $\Delta\Sigma$ modulator with $f_{Ci} = 9/4f_S$. Here, the image band of the single-path architecture is centred at $7/4f_S$. (STF — and NTF $\cdots$)

Using a single-path mixing process, a signal and its image are downconverted to the same frequency. In the same way, a single-path frequency-translating $\Delta\Sigma$ modulator downconverts interferers from its image band into its signal band. These interferers are attenuated by the outer-loop filter, prior to downconversion, which provides partial image-reject filtering for the forward-path mixer. The inherent image-reject filtering of a single-path frequency-translating $\Delta\Sigma$ modulator is improved by increasing the order of its outer-loop filter, and by increasing its output centre frequency (f_{Co}), relative to its sampling frequency (f_S).

The image-reject and single-path frequency-translating $\Delta\Sigma$ modulator architectures both require additional filtering when they are incorporated into a wireless receiver. This filtering is necessary to ensure that the interferers close to the signal band, which are not significantly attenuated by the STF, do not overload the $\Delta\Sigma$ modulator. Since this filtering supplements the inherent image-reject filtering of a single-path frequency-translating $\Delta\Sigma$ modulator, the limited inherent filtering of the single-path architecture is not a significant disadvantage, as compared to an image-reject architecture.

Implementation Issues

In terms of their implementation, the single-path and image-reject frequency-translating ΔΣ modulators provide advantages and disadvantages comparable to conventional bandpass and complex-bandpass ΔΣ modulators (Section 2.1.3). An image-reject frequency-translating ΔΣ modulator uses two quantizers, and requires twice as many feedback DACs as an equivalent single-path architecture. However, since it generates a complex output spectrum, the OSR of an image-reject architecture is double that of a single-path architecture.

5.2 NTF Synthesis

The noise-shaping characteristic of a single-path frequency-translating ΔΣ modulator can be derived from a prototype discrete-time ΔΣ modulator, using the general procedure that was described in Section 3.1 for a conventional continuous-time architecture. Here, the prototype discrete-time architecture must have a *bandpass* loop filter to replicate the feedback path of a single-path frequency-translating ΔΣ modulator. Figure 5.3 shows a prototype discrete-time bandpass ΔΣ modulator. The loop feedback path of a single-path frequency-translating ΔΣ modulator is shown in Figure 5.4(a), and the loop feedback path of a prototype discrete-time bandpass ΔΣ modulator is shown in Figure 5.4(b).

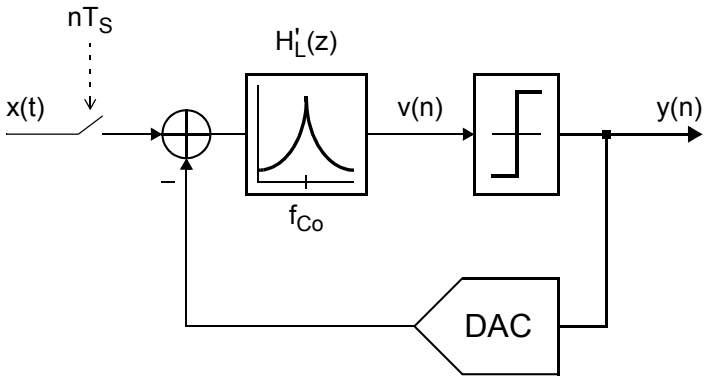
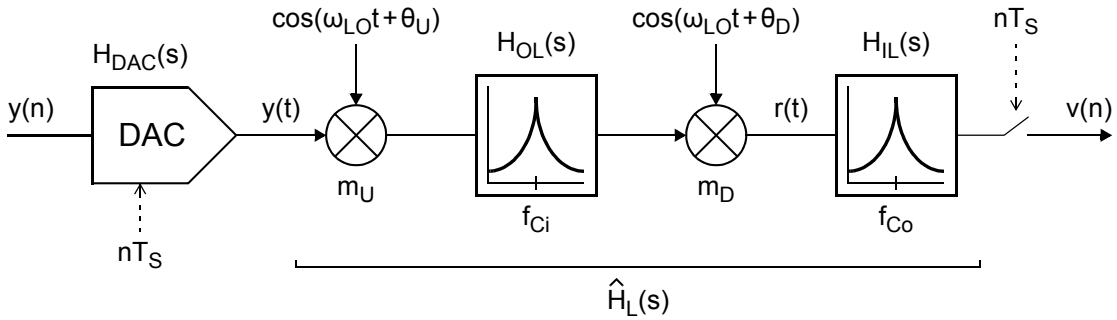
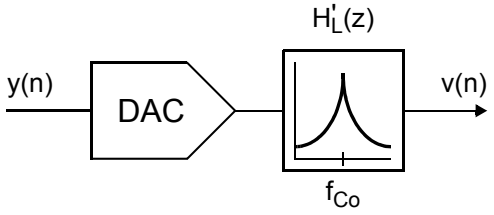


Figure 5.3: Block diagram for a discrete-time ΔΣ modulator with a bandpass loop filter.



(a)



(b)

Figure 5.4: The loop feedback paths of: **(a)** the single-path frequency-translating $\Delta\Sigma$ modulator in Figure 5.1, and **(b)** the equivalent discrete-time bandpass $\Delta\Sigma$ modulator in Figure 5.3.

In order to achieve the same NTF as the prototype discrete-time bandpass $\Delta\Sigma$ modulator in Figure 5.3, the single-path frequency-translating $\Delta\Sigma$ modulator in Figure 5.1 must provide the same loop response at sampling instants (Section 3.1). This impulse equivalence can be achieved using the impulse-invariant transform, which is defined as

$$\hat{H}_{\mathrm{L}}(s) \;=\; \underset{z\to s}{\mathrm{IIT}}\Big\{H'_{\mathrm{L}}(z)\Big\}\cdot\frac{1}{H_{\mathrm{DAC}}(s)} \;=\; \underset{z\to s}{\mathrm{IIT}}\left\{\frac{1}{\mathrm{NTF}(z)}-1\right\}\cdot\frac{1}{H_{\mathrm{DAC}}(s)} \tag{5.1}$$

The design of $\mathrm{NTF}(z)$ is discussed in Section 2.1.3. Here, $\hat{H}_{\mathrm{L}}(s)$ represents the *effective* loop transfer function of the single-path frequency-translating $\Delta\Sigma$ modulator.

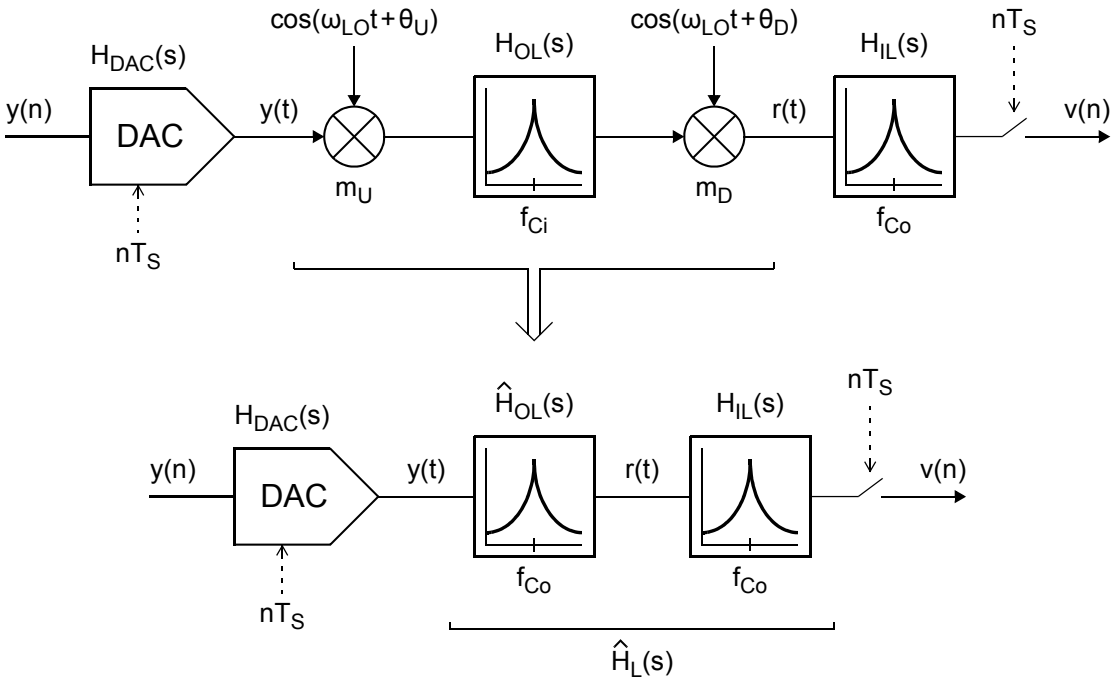
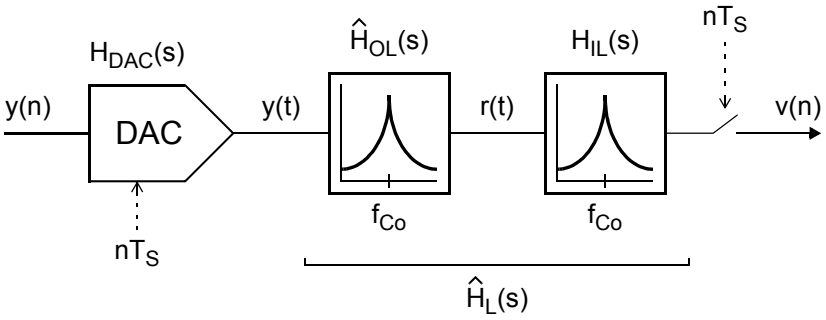


Figure 5.5: The *effective* loop feedback path of the single-path frequency-translating ΔΣ modulator in Figure 5.1, which combines the upconversion and downconversion operations with the response of the outer-loop filter $H_{\mathrm{OL}}(s)$.

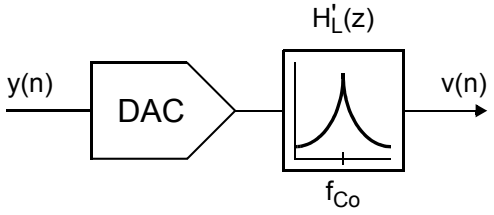
In order to use Equation (5.1) to map a prototype discrete-time NTF to the architecture shown in Figure 5.1, an *effective* transfer function is required for the time-varying response through its outer-loop path, from the input of the upconversion mixer $y(t)$ to the output of the downconversion mixer $r(t)$, as illustrated in Figure 5.5. This effective transfer function, denoted as $\hat{H}_{\mathrm{OL}}(s)$, is derived by imposing certain constraints on the timing parameters of the ΔΣ modulator (Section 5.2.1). The effective loop transfer function can be expressed as

$$\hat{H}_{\mathrm{L}}(s) \;=\; \hat{H}_{\mathrm{OL}}(s) H_{\mathrm{IL}}(s) \tag{5.2}$$

Figure 5.6(a) shows the *effective* loop feedback path of the single-path frequency-translating ΔΣ modulator in Figure 5.1, and Figure 5.6(b) shows the equivalent loop feedback path of the discrete-time bandpass ΔΣ modulator in Figure 5.3.



(a)



(b)

Figure 5.6: The *effective* loop feedback path of a single-path frequency-translating $\Delta\Sigma$ modulator, and the loop feedback path of a discrete-time bandpass $\Delta\Sigma$ modulator.

The effective transfer function of the outer-loop path, $\hat{H}_{\mathrm{OL}}(s)$, depends on the response of the outer-loop filter, $H_{\mathrm{OL}}(s)$ in Figure 5.1, and the frequency of the LO signal (f_{LO}). Given a 2nd-order filter, this effective transfer function has a general form of

$$\hat{H}_{\mathrm{OL}}(s) \;=\; \frac{\omega_{\mathrm{C}o}s + \omega_{\mathrm{C}o}^2}{\left(s + \frac{\omega_{\mathrm{C}i}}{2\mathrm{Q}}\right)^2 + \omega_{\mathrm{C}o}^2} \tag{5.3}$$

where $\omega_{\mathrm{C}i}$ and $\omega_{\mathrm{C}o}$ are the input and output centre frequencies of the frequency-translating $\Delta\Sigma$ modulator, and Q is the quality factor of its outer-loop filter $H_{\mathrm{OL}}(s)$. Section 5.3 derives an expression for $\hat{H}_{\mathrm{OL}}(s)$ assuming a prototype 2nd-order outer-loop filter.

The inner-loop transfer function, $H_{\mathrm{IL}}(s)$, that is required to implement a prototype NTF is then derived from the effective loop transfer function of the ΔΣ modulator $\hat{H}_{\mathrm{L}}(s)$, defined in Equation (5.1), and $\hat{H}_{\mathrm{OL}}(s)$, defined in Equation (5.3), where

$$H_{\mathrm{IL}}(s) \;=\; \frac{\hat{H}_{\mathrm{L}}(s)}{\hat{H}_{\mathrm{OL}}(s)} \tag{5.4}$$

The realization of the inner-loop filter is discussed in Section 5.4.

Due to the use of mixing in the feedback loop of a single-path frequency-translating ΔΣ modulator, the relationship in Equation (5.1) cannot be satisfied without setting additional constraints on its sampling period T_{S} and its inner-loop filter $H_{\mathrm{IL}}(s)$. Section 5.2.1 discusses the selection of the timing parameters in a single-path frequency-translating ΔΣ modulator, and Section 5.2.2 discusses the design of its inner-loop filter.

5.2.1 Selection of Timing Parameters for Time Invariance

The sampling constraint of a single-path frequency-translating ΔΣ modulator is identical to that of the in-phase path in an image-reject architecture, which was derived in Section 4.2.1. The previous derivation is summarized below.

The response through the outer-loop path of the single-path frequency-translating ΔΣ modulator in Figure 5.1 can be expressed as

$$r(t) \;=\; \frac{1}{2}\,x_{2\mathrm{I}}(t)\big[\,1+\cos(2\omega_{\mathrm{LO}}t)\,\big] + \frac{1}{2}\,x_{2\mathrm{Q}}(t)\sin(2\omega_{\mathrm{LO}}t) \tag{5.5}$$

where

$$x_{2\mathrm{I}}(t) \;=\; \big[\,h_{\mathrm{OL}}(t)\cos(\omega_{\mathrm{LO}}t)\,\big]\otimes y(t) \tag{5.6}$$

$$x_{2\mathrm{Q}}(t) \;=\; \big[\,h_{\mathrm{OL}}(t)\sin(\omega_{\mathrm{LO}}t)\,\big]\otimes y(t) \tag{5.7}$$

Note that Equation (5.5) is identical to (4.8) in Section 4.2.1, and Equations (5.6) and (5.7) are modified from (4.6) and (4.7) to remove the $y_{\mathrm{Q}}(t)$ term.

When $r(t)$ in (5.5) is sampled at time instants $t_n = nT_S$, defined in (4.2), with T_S set to an integer multiple of $T_{LO}/2$, $r(t_n)$ reduces to $x_{2I}(t_n)$, and is therefore time-invariant. This constraint on the sampling period can be generalized as

$$T_S = k_S \frac{T_{LO}}{2}, \qquad k_S = 1, 2, 3, \ldots \tag{5.8}$$

which is identical to the sampling constraint in Equation (4.10).

5.2.2 Constraints on the Characteristic of the Inner-Loop Filter

In order to achieve stable operation, the feedback loop of a $\Delta\Sigma$ modulator must be designed such that the spectral content of its input signal can be replicated by the spectral content of its feedback signal. This condition cannot be satisfied in a single-path frequency-translating $\Delta\Sigma$ modulator (Figure 5.1), since its feedback signal contains a full-scale image, in addition to the upconverted output signal. Therefore, in order for a single-path architecture to have a practical implementation, a constraint must be imposed on its inner-loop filter.

Lowpass Inner-Loop Filter

Figure 5.7 plots the frequency spectrum at different points in the feedback of a single-path frequency-translating $\Delta\Sigma$ modulator that is designed with a *lowpass* inner-loop filter. Here, f_{LO} is equal to $3f_S/2$, and the feedback DAC has an NRZ pulse, which results in a $\sin(f)/f$ response that has notches at multiples of f_S. In a single-path architecture, the feedback-path mixer upconverts both the output signal and its image. The signal component is subtracted at the input summation of the $\Delta\Sigma$ modulator, whereas the image is not attenuated prior to the outer-loop filter. In order to avoid swing issues at the output of the outer-loop filter, the frequency separation of the output signal and its image must be sufficient to ensure that the image falls well outside the bandwidth of the outer-loop filter. This condition is not satisfied when the signal and image bands are adjacent to one another, as illustrated in Figure 5.7(c). Accordingly, a single-path frequency-translating $\Delta\Sigma$ modulator cannot be correctly designed using a lowpass inner-loop filter.

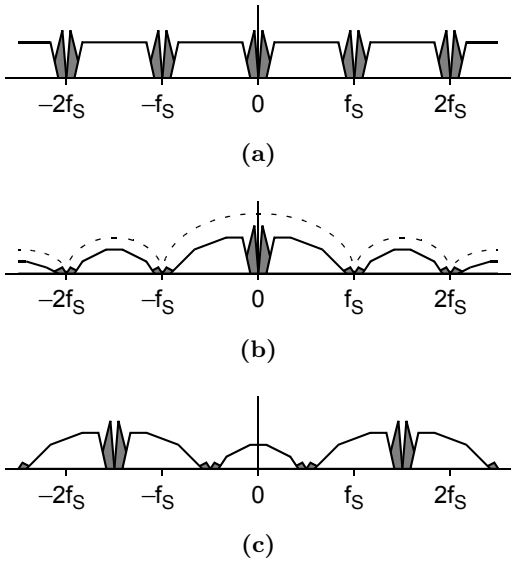


Figure 5.7: Frequency spectrum over the feedback path of a single-path frequency-translating ΔΣ modulator with a *lowpass* inner-loop filter: **(a)** at the output of the ΔΣ modulator $y(n)$, **(b)** after the feedback DAC $y(t)$, and **(c)** after the upconversion mixer $x_1(t)$. In this figure, f_{LO} is set to $3f_{\mathrm{S}}/2$.

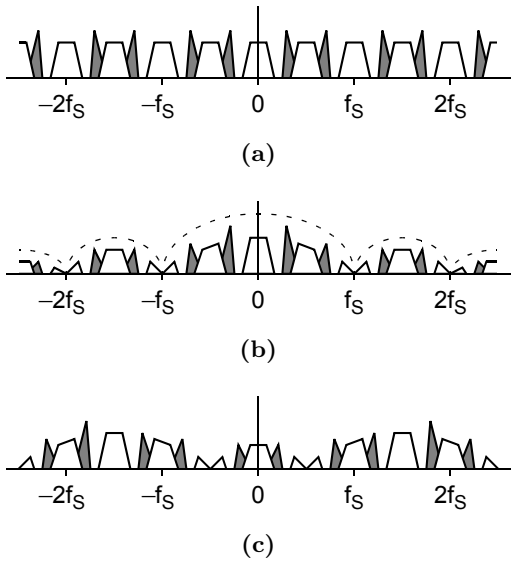


Figure 5.8: Frequency spectrum over the feedback path of a single-path frequency-translating ΔΣ modulator with a *bandpass* inner-loop filter: **(a)** at the output of the ΔΣ modulator $y(n)$, **(b)** after the feedback DAC $y(t)$, and **(c)** after the upconversion mixer $x_1(t)$. In this figure, f_{LO} is set to $3f_{\mathrm{S}}/2$.

Bandpass Inner-Loop Filter

Figure 5.8 plots the frequency spectrum at different points in the feedback of a single-path frequency-translating $\Delta\Sigma$ modulator that is designed with a *bandpass* inner-loop filter. Here, f_{LO} is equal to $3f_{\mathrm{S}}/2$, and the output centre frequency $f_{\mathrm{C}o}$ is set to $f_{\mathrm{S}}/4$. Using this design, the frequency separation of the signal and image bands is sufficient to ensure that the image band falls well outside the bandwidth of the outer-loop filter, as illustrated in Figure 5.8(c). Therefore, a single-path frequency-translating $\Delta\Sigma$ modulator can be correctly designed using a bandpass inner-loop filter.

5.3 Outer-Loop Filter Realization

This section develops an *effective* transfer function for the time-varying outer-loop path of a single-path frequency-translating $\Delta\Sigma$ modulator. It also demonstrates the dependence of the outer-loop path on the phase of the LO signal, and proposes a design technique that reduces the sensitivity of a frequency-translating $\Delta\Sigma$ modulator to phase variations.

Figure 5.9 shows a block diagram for the outer-loop path of a frequency-translating $\Delta\Sigma$ modulator that is designed with single-path mixing. The effective transfer function is derived here by applying a unit impulse $\delta(n)$ at the input of the feedback DAC, and then evaluating its associated response at the output of the downconversion mixer. This derivation assumes that the periods of the sampling clock and the LO signal, T_{S} and T_{LO} respectively, have been selected according to the constraint derived in Section 5.2.1 and, therefore, that the cascade of blocks in Figure 5.9 is periodically linear time-invariant (PLTI).

The derivation further assumes that the outer-loop bandpass filter, $H_{\mathrm{OL}}(s)$ in Figure 5.9, is implemented using a parallel RLC circuit that has a centre frequency of $f_{\mathrm{C}i}$ and a quality factor of Q. The transfer function of this 2nd-order filter can be expressed as

$$H_{\mathrm{OL}}(s) \;=\; \frac{\omega_{\mathrm{C}i}s}{s^2 + \frac{\omega_{\mathrm{C}i}}{\mathrm{Q}}s + \omega_{\mathrm{C}i}^2} \tag{5.9}$$

where $f_{\mathrm{C}i}$ is equal to the input centre frequency of the frequency-translating $\Delta\Sigma$ modulator, as defined in Section 5.1.

In a practical implementation, the quality factor of an LC resonator is typically limited by the series resistance of its inductor, rather than the parallel resistance of its LC tank. Such a configuration shifts the position of the zero in $H_{\mathrm{OL}}(s)$, however it has a minimal effect on the derived result and does not require further consideration.

For a sinusoidal LO signal with a frequency of f_{LO} and a phase of θ_{U}, relative to an edge of the sampling clock, the response of the upconversion mixer is given by

$$x_1(t) \;=\; \cos(\omega_{\mathrm{LO}} t + \theta_{\mathrm{U}})\, h_{\mathrm{DAC}}(t) \tag{5.10}$$

where $h_{\mathrm{DAC}}(t)$ is the impulse response of the feedback DAC.

It is assumed that the outer-loop DAC in Figure 5.9 uses an NRZ pulse that is delayed by $\delta_{\mathrm{E}} T_{\mathrm{S}}$ relative to the sampling clock. The response of this DAC can be expressed as

$$h_{\mathrm{DAC}}(t) \;=\; u(t - \delta_{\mathrm{E}} T_{\mathrm{S}}) - u(t - [1 + \delta_{\mathrm{E}}] T_{\mathrm{S}}) \tag{5.11}$$

where $u(t)$ represents the unit step function. This chapter presents a technique to design the inner-loop filter of a frequency-translating ΔΣ modulator, $H_{\mathrm{IL}}(s)$ in Figure 5.1, such that the response of its outer-loop path does not depend on the delay prior to its upconversion mixer. Therefore, this delay is not considered in subsequent equations (i.e., $\delta_{\mathrm{E}} = 0$).

In order to satisfy the time-shifting property of the Laplace transform, Equation (5.10) is modified so that the delay of the LO signal matches the delay of each term in $h_{\mathrm{DAC}}(t)$, where

$$x_1(t) \;=\; \cos(\omega_{\mathrm{LO}} t + \theta_{\mathrm{U}})\, u(t) - \cos(\omega_{\mathrm{LO}} [t - T_{\mathrm{S}}] + \theta_{\mathrm{U}})\, u(t - T_{\mathrm{S}}) \tag{5.12}$$

Note that Equation (5.10) can only be modified as shown in Equation (5.12) when T_{LO} and T_{S} are selected according to the constraint derived in Section 5.2.1.

By applying the constraint in Equation (5.8), the LO signal satisfies

$$\cos(\omega_{\mathrm{LO}} t + \theta_{\mathrm{U}}) \;=\; (-1)^{k_{\mathrm{S}}} \cos(\omega_{\mathrm{LO}} [t - T_{\mathrm{S}}] + \theta_{\mathrm{U}}) \tag{5.13}$$

where the sign inversion for odd values of k_{S} is reversed during downconversion mixing, and does not require further consideration.

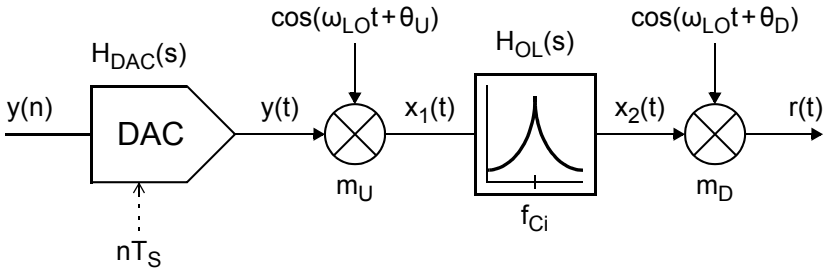


Figure 5.9: The outer-loop path of a single-path frequency-translating $\Delta\Sigma$ modulator.

The Laplace transform of Equation (5.12) yields

$$X_1(s) \;=\; \left[\cos(\theta_{\mathrm{U}})\,\frac{s}{s^2+\omega_{\mathrm{LO}}^2} - \sin(\theta_{\mathrm{U}})\,\frac{\omega_{\mathrm{LO}}}{s^2+\omega_{\mathrm{LO}}^2}\right]\left[1-\mathrm{e}^{-sT_{\mathrm{S}}}\right] \tag{5.14}$$

The response of the outer-loop filter $X_2(s)$ is derived by multiplying $X_1(s)$ and $H_{\mathrm{OL}}(s)$, and expanding their product using a partial fraction expansion. This results in

$$X_2(s) \;=\; \left[\frac{b_1 s - b_2\,\omega_{\mathrm{LO}}}{s^2+\omega_{\mathrm{LO}}^2} - \frac{b_1 s - b_2\eta_i\,\omega_{\mathrm{C}i}}{s^2+\frac{\omega_{\mathrm{C}i}}{\mathrm{Q}}s+\omega_{\mathrm{C}i}^2}\right]\left[1-\mathrm{e}^{-sT_{\mathrm{S}}}\right] \tag{5.15}$$

where $\eta_i = \frac{\omega_{\mathrm{C}i}}{\omega_{\mathrm{LO}}}$, and the phase components b_1 and b_2 are equal to

$$b_1 \;=\; \cos(\theta_{\mathrm{U}})\,c_2 - \sin(\theta_{\mathrm{U}})\,c_1 \tag{5.16}$$

$$b_2 \;=\; \cos(\theta_{\mathrm{U}})\,c_1 + \sin(\theta_{\mathrm{U}})\,c_2 \tag{5.17}$$

The coefficients c_1 and c_2 can be expressed in terms of η_i as

$$c_1 \;=\; \frac{\mathrm{Q}^2(\eta_i^2-1)\eta_i}{\mathrm{Q}^2(\eta_i^2-1)^2+\eta_i^2} \overset{\lim\limits_{\mathrm{Q}\to\infty}}{\cong} \frac{\eta_i}{\eta_i^2-1} \tag{5.18}$$

$$c_2 \;=\; \frac{\mathrm{Q}\eta_i^2}{\mathrm{Q}^2(\eta_i^2-1)^2+\eta_i^2} \overset{\lim\limits_{\mathrm{Q}\to\infty}}{\cong} 0 \tag{5.19}$$

Note that coefficient $c_2 \to 0$ as the quality factor $\mathrm{Q} \to \infty$, and therefore has a minimal effect on the response of the outer-loop path for practical values of Q.

The inverse Laplace transform of $X_2(s)$, given in Equation (5.15), is equal to

$$x_2(t) \;=\; \breve{x}_2(t)\,u(t) - \breve{x}_2(t-T_{\rm S})\,u(t-T_{\rm S}) \tag{5.20}$$

where

$$\begin{aligned}\breve{x}_2(\tau) \;=\; &[\,b_1\cos(\omega_{\rm LO}\tau) - b_2\sin(\omega_{\rm LO}\tau)\,] \\ &-\;[\,b_1\cos(\chi_i\omega_{{\rm C}i}\tau) - (b_2\eta_i + b_1\tfrac{1}{2{\rm Q}})\sin(\chi_i\omega_{{\rm C}i}\tau)\,]\,{\rm e}^{-\frac{\omega_{{\rm C}i}}{2{\rm Q}}\tau}\end{aligned} \tag{5.21}$$

Note that ${\rm Q}^2 \gg 1$ and, correspondingly, $\chi_i \cong 1$ for practical values of Q. Accordingly, χ_i is not included in subsequent equations.

The response of the downconversion mixer can be expressed as

$$r(t) \;=\; \cos(\omega_{\rm LO}t + \theta_{\rm D})\,x_2(t) \tag{5.22}$$

where $\theta_{\rm D}$ is the phase of the LO signal that is applied to the downconversion mixer, relative to the sampling clock. In order to satisfy the time-shifting property of the Laplace transform, the LO signal must be modified in the same way as in Equation (5.12).

The downconversion mixer splits the response of the outer-loop path into two terms: the required *low-frequency* term $r_{\rm low}(t)$, which is centred at $f_{{\rm C}o} \equiv (f_{{\rm C}i} - f_{\rm LO})$, and an additional *high-frequency* term $r_{\rm high}(t)$, which is centred at $(f_{{\rm C}i} + f_{\rm LO})$. The low-frequency term $r_{\rm low}(t)$ results from the difference in the arguments of the LO signals that are applied to the mixers, and has a scaling factor that depends primarily on the difference in their phases $(\theta_{\rm U} - \theta_{\rm D})$. The high-frequency term $r_{\rm high}(t)$ similarly results from the sum of these arguments, and has a scaling factor that depends primarily on the sum of their phases $(\theta_{\rm U} + \theta_{\rm D})$.

If the high-frequency term is significantly attenuated following the downconversion mixer, the response of the outer-loop path is effectively independent of the absolute values of phases $\theta_{\rm U}$ and $\theta_{\rm D}$, and instead depends only on their difference $(\theta_{\rm U} - \theta_{\rm D})$. This result can be further extended to excess loop delay. When the high-frequency term is significantly attenuated, the response of the outer-loop path is independent of the delay prior to the upconversion mixer, and instead depends only on the delay between the mixers, which is negligible. Accordingly, by

significantly attenuating the high-frequency term, the loop response of a frequency-translating $\Delta\Sigma$ modulator becomes independent of the delay between its LO signal and sampling clock, and is therefore insensitive to synchronization errors between these signals. Furthermore, the response of the outer-loop path becomes independent of the excess loop delay, can therefore be represented as an linear time-invariant (LTI) filter.

The remainder of this derivation assumes that the high-frequency term is attenuated, and therefore only considers the low-frequency term. The response of the low-frequency term can be expressed as

$$r_{\mathrm{low}}(t) \;=\; \breve{r}_{\mathrm{low}}(t)\, u(t) - \breve{r}_{\mathrm{low}}(t - T_{\mathrm{S}})\, u(t - T_{\mathrm{S}}) \tag{5.23}$$

where

$$\breve{r}_{\mathrm{low}}(\tau) \;=\; \frac{1}{2}\, d_1 \Big[\, 1 - \mathrm{e}^{-\frac{\omega_{\mathrm{C}i}}{2\mathrm{Q}}\tau} \cos(\omega_{\mathrm{C}o}\tau) \,\Big] + \frac{1}{2}\, d_2 \Big[\, \mathrm{e}^{-\frac{\omega_{\mathrm{C}i}}{2\mathrm{Q}}\tau} \sin(\omega_{\mathrm{C}o}\tau) \,\Big] \tag{5.24}$$

and the phase components d_1 and d_2 are equal to

$$d_1 \;=\; \cos(\theta_{\mathrm{M}})\, c_2 - \sin(\theta_{\mathrm{M}})\, c_1 \tag{5.25}$$

$$d_2 \;=\; \cos(\theta_{\mathrm{M}})\, c_1 + \sin(\theta_{\mathrm{M}})\, c_2 \tag{5.26}$$

Here, $\theta_{\mathrm{M}} \equiv (\theta_{\mathrm{U}} - \theta_{\mathrm{D}})$ represents the phase difference between the LO signals that are applied to the upconversion and downconversion mixers.

Note that a number of terms have been excluded from Equations (5.25) and (5.26). These secondary terms depend on both the sum and the difference of the LO phases, however their magnitudes are negligible as compared to d_1 and d_2. Therefore, they can be omitted from the derived transfer function without significantly affecting its accuracy.

The Laplace transform of Equation (5.23) yields the effective response of the outer-loop path. It can be expressed as

$$R_{\mathrm{low}}(s) \;=\; \hat{H}_{\mathrm{OL}}(s)\, H_{\mathrm{DAC}}(s)\, Y(\mathrm{e}^{sT_{\mathrm{S}}}) \tag{5.27}$$

where $H_{\mathrm{DAC}}(s)$ is the Laplace transform of $h_{\mathrm{DAC}}(t)$ in Equation (5.11).

Accordingly, the effective transfer function of the outer-loop path can be expressed as

$$\hat{H}_{\mathrm{OL}}(s) \;=\; \frac{\left(d_1 \frac{1}{2\hat{\mathrm{Q}}} + d_2\right)\omega_{\mathrm{C}o} s + d_1 \omega_{\mathrm{C}o}^2}{\left(s + \frac{\omega_{\mathrm{C}o}}{2\hat{\mathrm{Q}}}\right)^2 + \omega_{\mathrm{C}o}^2} \tag{5.28}$$

where $f_{\mathrm{C}o}$ represents the output centre frequency of the frequency-translating ΔΣ modulator and the quality factor $\hat{\mathrm{Q}} \equiv (\omega_{\mathrm{C}o}/\omega_{\mathrm{C}i})\,\mathrm{Q}$.

5.4 Inner-Loop Filter Realization

This section discusses the realization of the inner-loop filter of the frequency-translating ΔΣ modulator in Figure 5.1, focusing on the configuration of its coefficient paths. The inner-loop filter of a single-path frequency-translating ΔΣ modulator must provide a bandpass filtering characteristic (Section 5.2.2), and is implemented using a cascade of resonators. The transfer function of the inner-loop filter can be generalized as

$$H_{\mathrm{IL}}(s) \;=\; \frac{b_{N_i+1}\,\omega_{\mathrm{C}o} s^{N_i} + \cdots + b_2\,\omega_{\mathrm{C}o}^{N_i-1} s + b_1\,\omega_{\mathrm{C}o}^{N_i}}{(s^2 + \omega_{\mathrm{C}o}^2)^{N_i/2}} \tag{5.29}$$

where $f_{\mathrm{C}o}$ is the output centre frequency of the frequency-translating ΔΣ modulator and N_i is the order of the inner-loop filter.

In Equation (5.29), $H_{\mathrm{IL}}(s)$ provides $(N_i + 1)$ coefficients. The loop filter of a single-path frequency-translating ΔΣ modulator requires a total of $N = (N_o + N_i)$ coefficients to realize a prototype NTF, where N_o is the order of the outer-loop filter. The outer-loop filter $H_{\mathrm{OL}}(s)$ considered in Section 5.3 has $N_o = 2$, however it does not provide any additional coefficient paths. Accordingly, if the expressions in Equations (5.9) and (5.29) are realized directly, the resulting loop filter will be missing one coefficient path. This path, and its implementation, are discussed further in Section 6.1.4.

The loop filter of a $\Delta\Sigma$ modulator can be realized using *feedforward* coefficient paths or *feedback* coefficient paths (Section 2.1.3). In a frequency-translating $\Delta\Sigma$ modulator, the loop filter best implemented by combining both types of coefficient paths into a *hybrid* topology. This section discusses the advantages of feedforward and feedback paths in the context of a frequency-translating $\Delta\Sigma$ modulator. The analysis that is presented here is used to develop an optimized loop-filter topology in Section 6.1.

5.4.1 Feedforward Paths

In a frequency-translating $\Delta\Sigma$ modulator (Figure 5.1), a feedforward loop-filter topology can be used to decrease the signal swing through the forward-path mixer and, in this way, reduce the distortion introduced by the mixer. Figure 5.10 shows a single-path frequency-translating $\Delta\Sigma$ modulator that is realized using a strictly-feedforward loop-filter topology.

The advantages of a feedforward loop-filter topology are first described in the context of a conventional $\Delta\Sigma$ modulator. Figure 5.11(a) shows a conventional bandpass $\Delta\Sigma$ modulator that is realized using a strictly-feedback loop-filter topology. Here, the first stage of the loop filter $I_1(s)$ must generate an input-signal component proportional to feedback coefficient a_2, since the loop gain of the $\Delta\Sigma$ modulator forces the output of each subtraction node to zero. This large input-signal component means that the distortion introduced by $I_1(s)$ can limit the maximum signal swing at its output and, correspondingly, the dynamic range of the $\Delta\Sigma$ modulator. Although this input-signal component could be reduced by decreasing the values of coefficients a_1 and a_2 using *dynamic range scaling* [Sch05], this reduces the suppression of the circuit noise introduced by the remaining stages of the loop filter.

Figure 5.11(b) shows a strictly-feedforward realization of the conventional bandpass $\Delta\Sigma$ modulator shown in Figure 5.11(a). Here, the magnitude of the input-signal component that must be generated at the output of the first stage $I_1(s)$ is significantly lower than that in the feedback topology. As a result, the distortion that is introduced by this stage is reduced, and dynamic range scaling can be used to increase coefficients a_1 and a_2, in order to improve the suppression of circuit noise. Note that the linearity enhancement provided by a feedforward implementation is most effective for designs with high oversampling ratios [Sch05].

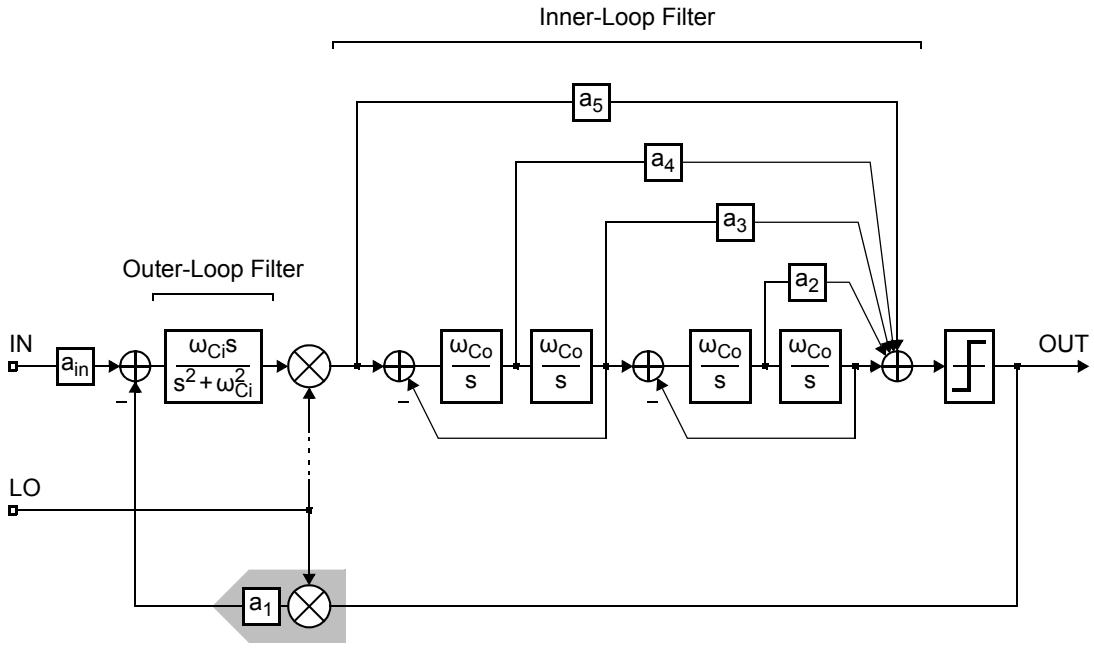
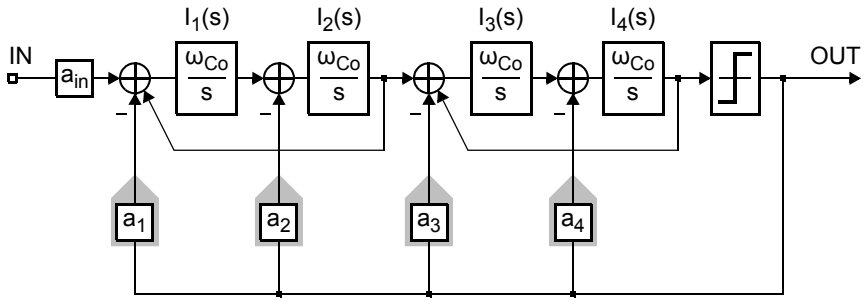


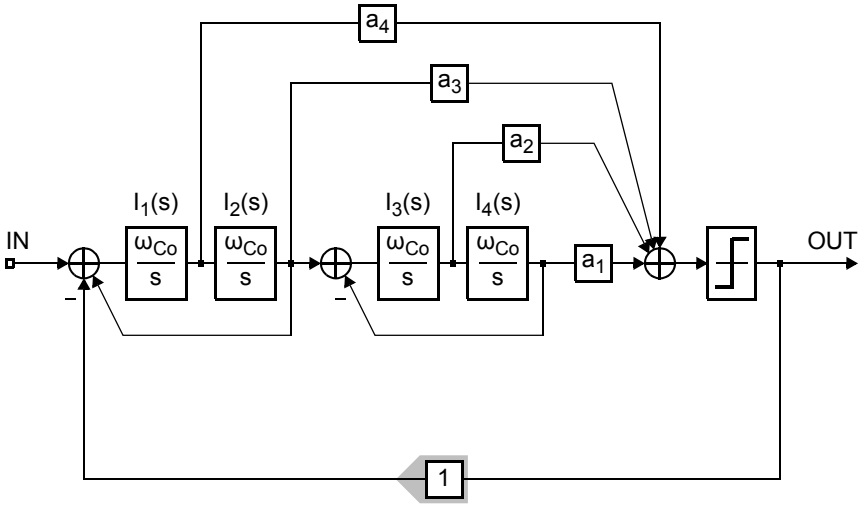
Figure 5.10: Block diagram for a 6th-order single-path frequency-translating ΔΣ modulator that is designed with a strictly-feedforward loop-filter topology.

In a frequency-translating ΔΣ modulator (Figure 5.10), a feedforward loop-filter topology reduces the magnitude of the signal component that must be passed by the downconversion mixer and, in this way, reduces the distortion that is introduced by the mixer. In addition, it facilitates the use of dynamic range scaling. Here, the coefficient a_1 of the outer-loop path is increased to improve the suppression of circuit noise introduced by the inner-loop filter.

Use of a feedforward implementation is particularly important in a frequency-translating ΔΣ modulator, since the nominal value of its outer-loop path coefficient a_1 is lower than that of the equivalent coefficient in a conventional bandpass ΔΣ modulator (Figure 5.11). When the filtering characteristic of the outer-loop filter is shifted from the input centre frequency to the output centre frequency (f_{Ci} to f_{Co}), its effective quality factor is decreased by (f_{Ci}/f_{Co}), however its mid-band gain is only decreased by 1/2 (Section 5.3). As a result, the effective filtering characteristic of the outer-loop path has a higher stopband gain than a conventional resonator and, therefore, requires a smaller nominal coefficient.



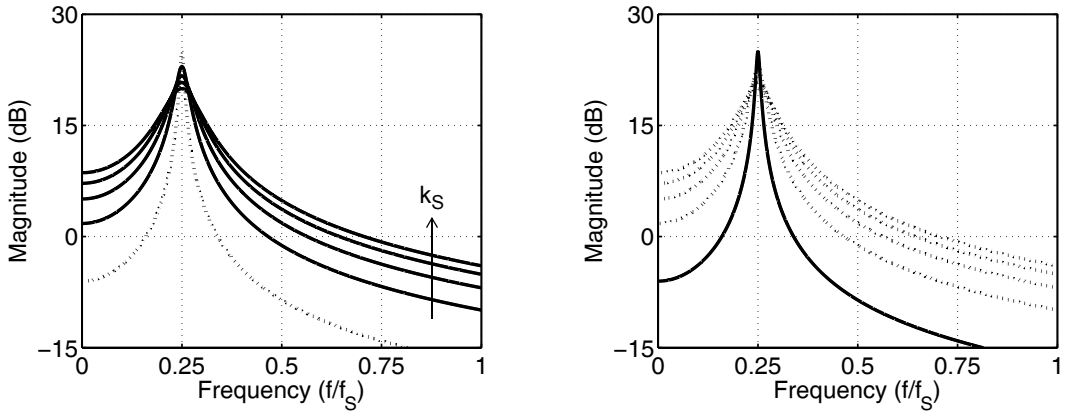
(a)



(b)

Figure 5.11: Block diagrams for a conventional 4th-order bandpass $\Delta\Sigma$ modulator that is designed with: **(a)** a strictly-feedback loop-filter topology, and **(b)** a strictly-feedforward topology.

Figure 5.12(a) uses Equations (5.8) and (5.28) to plot the effective filtering characteristic of the outer-loop path for a single-path frequency-translating $\Delta\Sigma$ modulator. Figure 5.12(b) provides an equivalent plot for one resonator in a conventional bandpass $\Delta\Sigma$ modulator.



(a) **(b)**

Figure 5.12: (a) The effective filtering characteristic of the outer-loop path $\hat{H}_{\mathrm{OL}}(s)$ of a single-path frequency-translating ΔΣ modulator (Section 5.3), where k_{S} is varied from 1 to 4, and **(b)** the filtering characteristic of one resonator in a conventional bandpass ΔΣ modulator.

As the value of k_{S} increases in Figure 5.12(a), the effective quality factor of the outer-loop filter decreases, whereas its mid-band gain remains approximately constant. In this way, the effective stopband gain of the outer-loop filter increases with k_{S}, so that the nominal value of the outer-loop path coefficient a_1 decreases, which reduces the suppression of circuit noise. Therefore, use of a feedforward implementation becomes increasingly important as the input centre frequency of a frequency-translating ΔΣ modulator is increased above its sampling frequency or, equivalently, as the value of k_{S} is increased.

5.4.2 Feedback Paths

In a frequency-translating ΔΣ modulator, feedback coefficient paths can be used in the loop filter to attenuate the high-frequency term of the loop response, as described in Section 5.3. Figure 5.13 depicts a single-path frequency-translating ΔΣ modulator that is realized using a *hybrid* feedforward-feedback loop-filter topology.

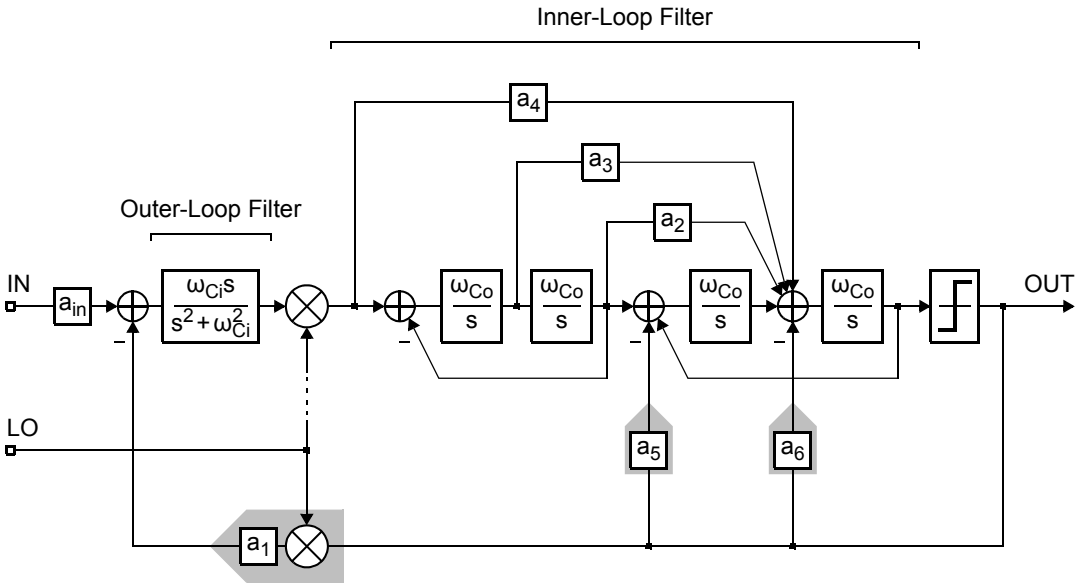


Figure 5.13: Block diagram for a 6th-order single-path frequency-translating $\Delta\Sigma$ modulator that is designed with a hybrid feedforward-feedback loop-filter topology.

The single-path frequency-translating $\Delta\Sigma$ modulator in Figure 5.13 is different from the general architecture shown in Figure 5.1, in that it has feedback paths connected directly to its inner-loop filter. Figure 5.14 shows a general block diagram for a single-path architecture that has a hybrid feedforward-feedback loop-filter topology.

The loop feedback path of the hybrid feedforward-feedback architecture in Figure 5.14 is shown in Figure 5.15. Here, the *effective* loop transfer function can be expressed as

$$\hat{H}_{\mathrm{L}}(s) \;=\; \hat{H}_{\mathrm{OL}}(s)H_{\mathrm{IL,F}}(s) + H_{\mathrm{IL,B}}(s) \tag{5.30}$$

where $H_{\mathrm{IL,F}}(s)$ denotes the forward[1] component of the inner-loop filter $H_{\mathrm{IL}}(s)$, and $H_{\mathrm{IL,B}}(s)$ denotes the feedback[2] component.

[1]The *forward* component, $H_{\mathrm{IL,F}}(s)$, is the transfer function from the output of the downconversion mixer to the input of the quantizer, excluding the effect of the feedback paths.

[2]The *feedback* component, $H_{\mathrm{IL,B}}(s)$, is the transfer function from the output of the $\Delta\Sigma$ modulator to the input of the quantizer, excluding the response of the outer-loop path.

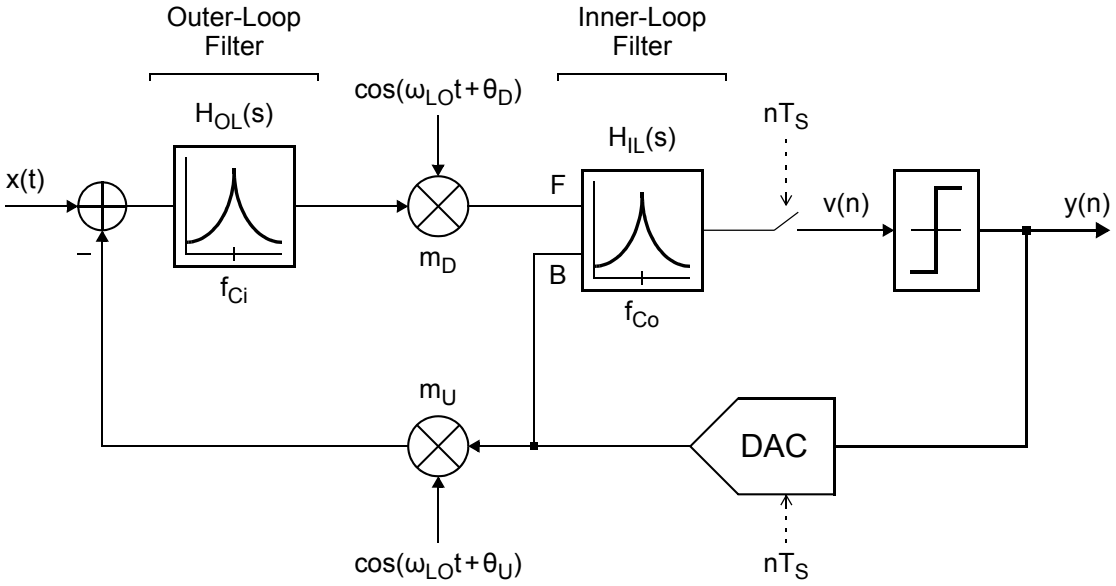


Figure 5.14: General block diagram for a single-path frequency-translating ΔΣ modulator that has a hybrid feedforward-feedback loop-filter topology.

The transfer functions that are implemented by the forward and feedback components of the inner-loop filter, $H_{\mathrm{IL,F}}(s)$ and $H_{\mathrm{IL,B}}(s)$, depend on the selected topology. The coefficient paths of the loop filter must be realized such that the effective loop transfer function of the frequency-translating ΔΣ modulator, $\hat{H}_{\mathrm{L}}(s)$ in Equation (5.30), can satisfy the relationship in Equation (5.1) for a prototype NTF. In particular, a loop filter of order N must provide an equal number of unique coefficient paths.

For the single-path frequency-translating ΔΣ modulator shown Figure 5.13, the forward and feedback components of the inner-loop filter can be expressed as

$$H_{\mathrm{IL,F}}(s) = \frac{a_4\,\omega_{\mathrm{C}o}s}{(s^2+\omega_{\mathrm{C}o}^2)} + \frac{a_3\,\omega_{\mathrm{C}o}^2}{(s^2+\omega_{\mathrm{C}o}^2)} + \frac{a_2\,\omega_{\mathrm{C}o}^3 s}{(s^2+\omega_{\mathrm{C}o}^2)^2} + \frac{\omega_{\mathrm{C}o}^4}{(s^2+\omega_{\mathrm{C}o}^2)^2} \tag{5.31}$$

$$H_{\mathrm{IL,B}}(s) = \frac{a_6\,\omega_{\mathrm{C}o}s}{(s^2+\omega_{\mathrm{C}o}^2)} + \frac{a_5\,\omega_{\mathrm{C}o}^2}{(s^2+\omega_{\mathrm{C}o}^2)} \tag{5.32}$$

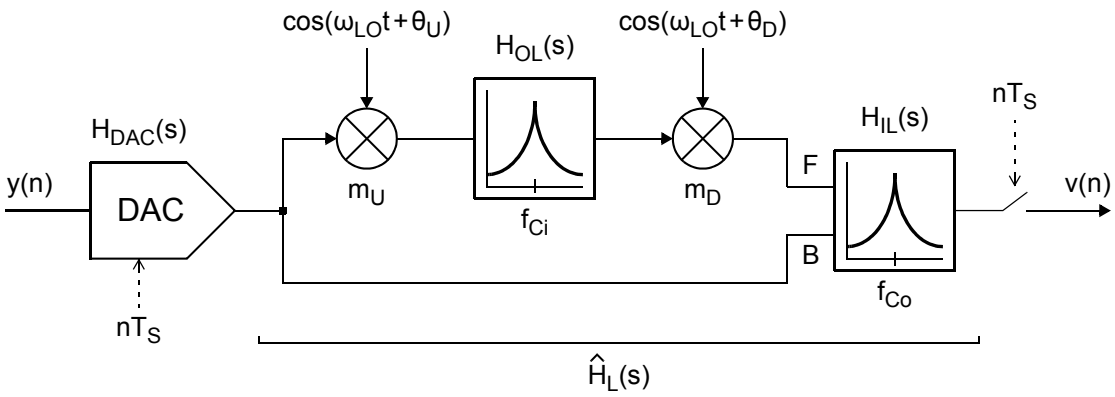


Figure 5.15: The loop feedback path of a single-path frequency-translating $\Delta\Sigma$ modulator that is designed with a hybrid feedforward-feedback loop-filter topology.

In a frequency-translating $\Delta\Sigma$ modulator (Figure 5.1), feedback coefficient paths can be used to attenuate the high-frequency term of the loop response. As described in Section 5.3, the loop response of a frequency-translating $\Delta\Sigma$ modulator contains two terms: the required *low-frequency* term, which is centred at $(f_{Ci} - f_{LO})$, and an additional *high-frequency* term, which is centred at $(f_{Ci} + f_{LO})$. When the inner-loop filter is designed with a continuous-time circuit topology, the high-frequency term is attenuated by the STF from the output of the downconversion mixer to the input of the quantizer. The resulting filtered term is then aliased by the sampling operation and, in this way, is added to the low-frequency term to form the overall loop response.

In order to satisfy the sampling constraints derived in Section 5.2, f_{LO} must be an integer multiple of $f_S/2$. As a result, the $2f_{LO}$ frequency separation between the high-frequency term and the low-frequency term always corresponds to a multiple of f_S. When the inner-loop filter is designed using a continuous-time topology, the centre of the high-frequency term coincides with one of the notches in the STF. Therefore, the in-band component of this term is always significantly attenuated. The proposed loop-filter topology uses feedback coefficient paths to increase the roll-off of the forward filter (Section 2.1.3), so that the STF also attenuates the out-of-band components of the high-frequency term.

Reducing the contribution of the high-frequency term to the overall loop response has the following advantages:

1. The sampled contribution of the high-frequency term depends on the degree to which it is attenuated by the STF. However, the STF is a function of the NTF, and therefore depends on the contribution of the high-frequency term. This interdependence between the STF and the high-frequency term makes it difficult to accurately include the latter in the design of the NTF. Therefore, significantly attenuating the high-frequency term improves the design accuracy of the NTF.

2. As described in Section 5.3, the loop response depends on the phase difference between the sampling clock and the LO signal:[3] the low-frequency term depends on $(\theta_{\mathrm{U}} - \theta_{\mathrm{D}})$, and the high-frequency term depends on $(\theta_{\mathrm{U}} + \theta_{\mathrm{D}})$. When the high-frequency term is significantly attenuated, the phase dependence of the loop response effectively reduces to that of the low-frequency term $\theta_{\mathrm{M}} \equiv (\theta_{\mathrm{U}} - \theta_{\mathrm{D}})$. In this case, since θ_{M} depends on the difference between θ_{U} and θ_{D}, and not on their sum, the loop response is independent of the delay between the sampling clock and the LO signal, and is therefore insensitive to synchronization errors between these signals.

3. In order to accurately process the high-frequency term, the operational amplifiers that are used to implement the inner-loop filter must provide a high signal gain at its centre frequency $(f_{Ci} + f_{\mathrm{LO}})$. When the high-frequency term is significantly attenuated, these amplifiers are only required to provide a high signal gain at the centre frequency of the low-frequency term f_{Co}. This advantage is described further in Section 6.1.3.

The attenuation of the high-frequency term, relative to the low-frequency term, is evaluated using Equation (5.39), derived in Section 5.6.3.

[3]Recall that θ_{U} and θ_{D} represent the phases of the LO signal, relative to an edge of the sampling clock, that are applied to the upconversion and downconversion mixers, respectively.

5.5 Phase of the LO Signal

The loop response of a frequency-translating $\Delta\Sigma$ modulator depends on the phase difference between its LO signal and its sampling clock, as described in Section 5.3. The low-frequency term of the loop response depends primarily on $(\theta_{\mathrm{U}} - \theta_{\mathrm{D}})$, whereas the high-frequency term depends primarily on $(\theta_{\mathrm{U}} + \theta_{\mathrm{D}})$. Here, θ_{U} and θ_{D} denote the phases of the LO signal, relative to an edge of the sampling clock, that are applied to the upconversion and downconversion mixers, respectively.

When the high-frequency term is significantly attenuated, as outlined in Section 5.3, the LO phase dependence of the loop response is effectively reduced to that of the low-frequency term, $\theta_{\mathrm{M}} \equiv (\theta_{\mathrm{U}} - \theta_{\mathrm{D}})$. This section discusses the selection of the relative LO phase (θ_{M}), and presents a design technique to reduce the sensitivity of the loop response to variations in the implemented value of θ_{M}.

5.5.1 Sensitivity to Phase Errors

In a frequency-translating $\Delta\Sigma$ modulator, the relative LO phase (θ_{M}) is set using an on-chip delay, and is therefore sensitive to the effect of process variations. An error in the value of θ_{M} modifies the response through the outer-loop path, which shifts the poles of the NTF from their nominal positions. This type of error can decrease the noise-shaping performance of a frequency-translating $\Delta\Sigma$ modulator and, if it is sufficiently large, can cause the closed-loop transfer function to become unstable.

The relative LO phase (θ_{M}) sets the position of the zero in the effective transfer function of the outer-loop path, which was derived in Section 5.3. As a result, the phase sensitivity of the loop response cannot be decreased using a conventional minimization procedure, since it would produce an optimal value of θ_{M} that is a function of frequency.

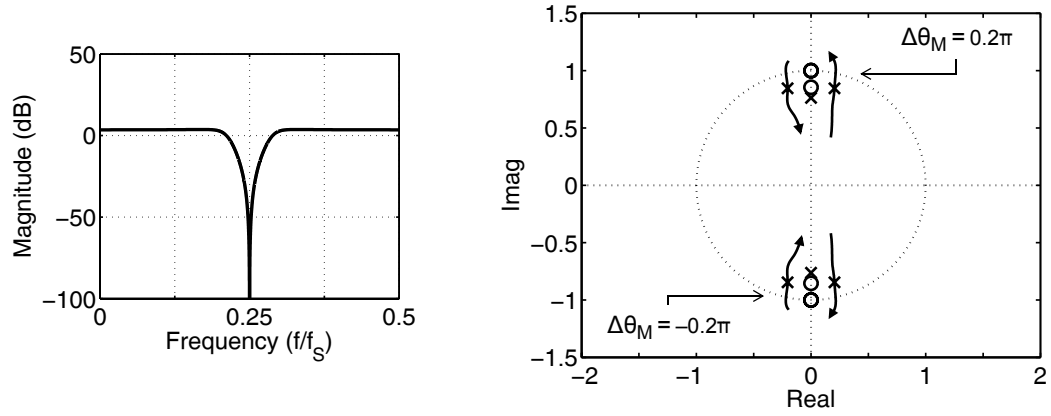
The phase sensitivity of a frequency-translating ΔΣ modulator can be reduced by noting that an error in the relative LO phase (θ_{M}) shifts the poles of the NTF in approximately the same way as an error in one of the loop-filter coefficients. Figure 5.16 plots three NTFs for a 6th-order single-path frequency-translating ΔΣ modulator that is designed with $f_{Co} = 1/4 f_{\mathrm{S}}$ and $f_{\mathrm{LO}} = f_{\mathrm{S}}$. Here, the poles of the NTF are selected so that its out-of-band gain[4] is equal to: (a) 3.5 dB, (b) 12.0 dB, and (c) 16.3 dB.

Figure 5.16 also plots a root locus for each NTF on the complex z-plane, illustrating the shift in the poles of the NTF as the relative LO phase (θ_{M}) is varied from its nominal value. Here, as the out-of-band gain increases, the minimum phase error ($\Delta\theta_{\mathrm{M}}$) that causes one or more poles of the NTF to move outside the unit circle (i.e., $|z| = 1$) decreases. Accordingly, the phase sensitivity of a frequency-translating ΔΣ modulator can be reduced by decreasing the out-of-band gain of its NTF.

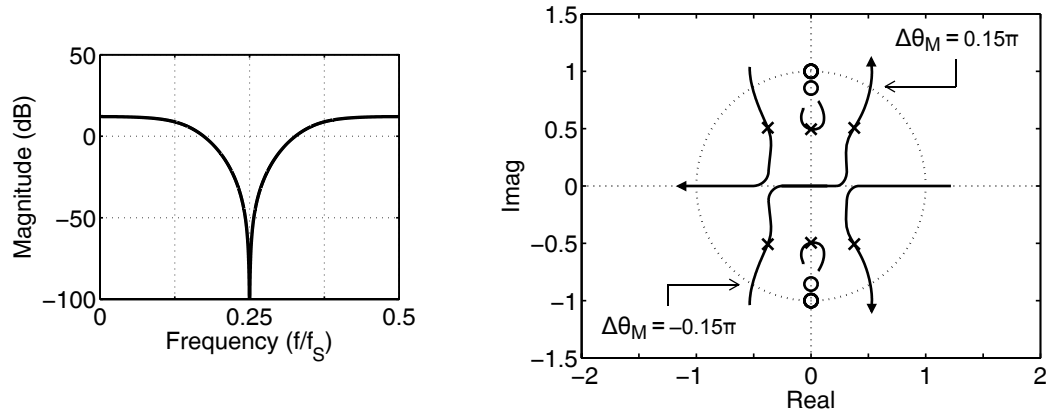
5.5.2 Selection of the LO Phase

The relative LO phase (θ_{M}) modifies the response through the outer-loop feedback path of a frequency-translating ΔΣ modulator, as derived in Section 5.3. However, with the exception of a phase shift, which can be referred to the input of the ΔΣ modulator, the value of θ_{M} does not affect the response of the forward path. As a result, the effective transfer function of the outer-loop path $\hat{H}_{\mathrm{OL}}(s)$, in the loop feedback path of a frequency-translating ΔΣ modulator, does not match the transfer function of the outer-loop filter $H_{\mathrm{OL}}(s)$ in its forward path. This difference affects the in-band STF gain of a frequency-translating ΔΣ modulator and, when the quality factor of the outer-loop filter is fixed, becomes increasingly important for higher values of the sampling parameter k_{S} (Section 5.2.1).

[4]Recall that increasing the NTF out-of-band gain improves the noise shaping performance of a ΔΣ modulator, but also reduces the maximum signal that can be applied at its input (Section 2.1.3).



(a)



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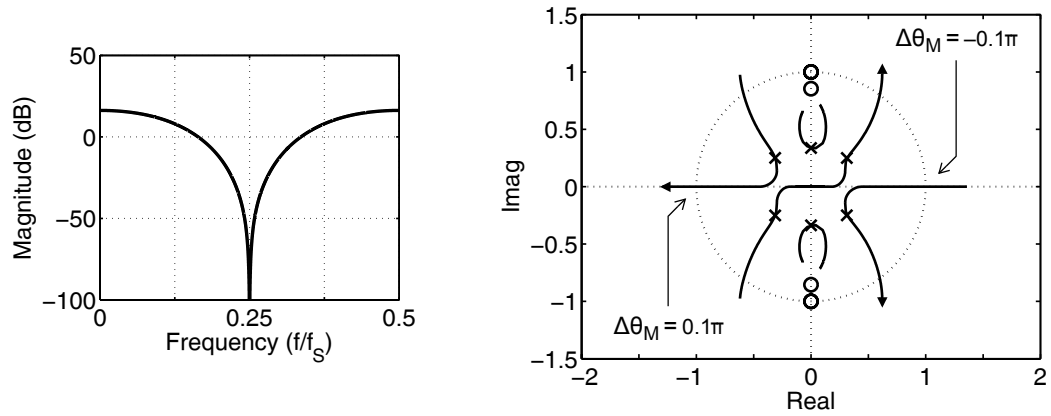

(c)

Figure 5.16: Root locus plots that illustrate the shift in the NTF poles of a frequency-translating $\Delta\Sigma$ modulator when the relative LO phase (θ_{M}) is varied from its nominal value. Here, the out-of-band gain is set to: **(a)** 3.5 dB, **(b)** 12.0 dB, and **(c)** 16.3 dB.

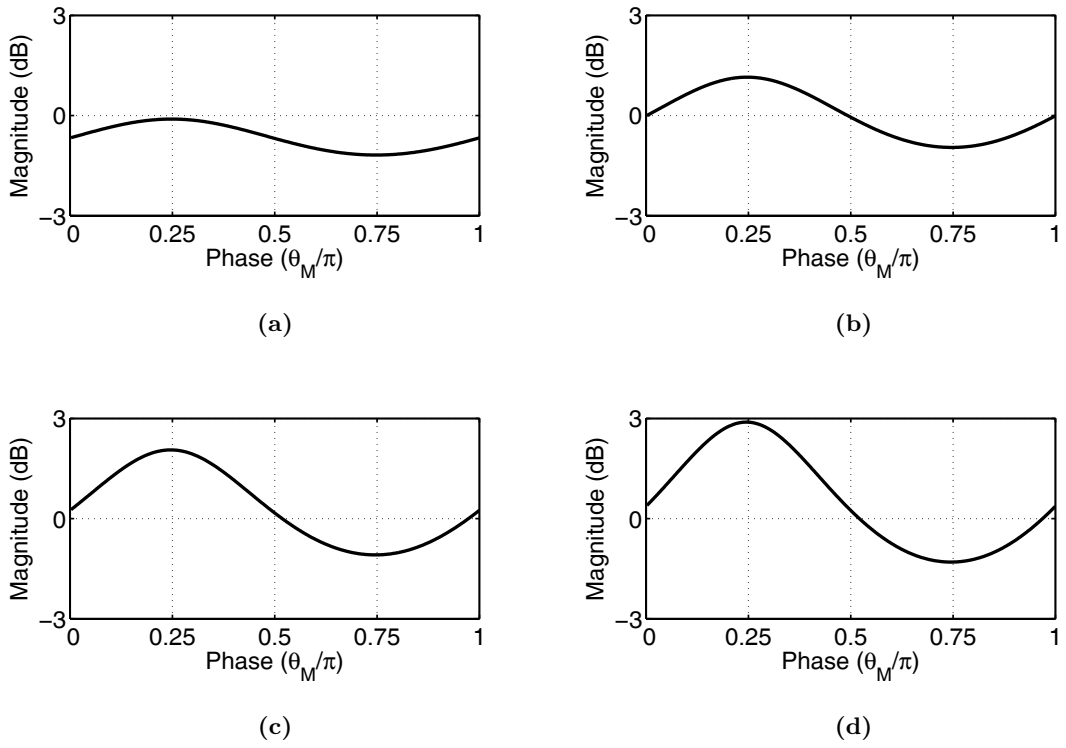

Figure 5.17: The STF gain, as a function of θ_{M}, at the input centre frequency ($f_{\mathrm{C}i}$) of a single-path frequency-translating $\Delta\Sigma$ modulator for: **(a)** $k_{\mathrm{S}} = 1$, **(b)** $k_{\mathrm{S}} = 2$, **(c)** $k_{\mathrm{S}} = 3$, and **(d)** $k_{\mathrm{S}} = 4$.

Figures 5.17(a)–(d) plot the STF gain, as a function of θ_{M}, at the input centre frequency of a single-path frequency-translating $\Delta\Sigma$ modulator that is designed with $f_{\mathrm{C}o} = 1/4 f_{\mathrm{S}}$, and k_{S} ranging from 1, in (a), to 4, in (d). In all four cases, the STF gain is maximized when the relative LO phase is set to

$$\theta_{\mathrm{M}} \;=\; (\theta_{\mathrm{U}} - \theta_{\mathrm{D}}) \;=\; \frac{\pi}{4} \tag{5.33}$$

The value of θ_{M} does not affect the noise-shaping performance of a single-path frequency translating $\Delta\Sigma$ modulator, assuming that the coefficients of its loop filter are selected using the procedure described in Section 5.2. However, increasing the STF gain is beneficial, since it decreases the signal swing that is required at the input of the $\Delta\Sigma$ modulator, and therefore reduces the linearity requirement on the first stage of the loop filter (Section 7.1).

5.6 Signal Transfer Function

This section outlines a general procedure to derive the *effective* signal transfer function (STF) of a single-path frequency-translating $\Delta\Sigma$ modulator. The derived STF is required to evaluate the inherent image-reject filtering of a single-path architecture, and to verify the attenuation of its high-frequency term.

The effective STF is derived using a variation on the standard procedure that is applied to continuous-time $\Delta\Sigma$ modulators [Ort06]. Here, the forward component of the loop filter is modified such that the filtering characteristic of the outer-loop filter $H_{\mathrm{OL}}(s)$ and that of the inner-loop filter $H_{\mathrm{IL}}(s)$ are both represented at the same centre frequency.

5.6.1 General Procedure

Figure 5.18(a) shows the linear model of a single-path frequency-translating $\Delta\Sigma$ modulator, where transfer functions $H_{\mathrm{OL}}(s)$ and $H_{\mathrm{IL}}(s)$ represent the outer-loop and inner-loop filters, respectively. In order to derive the effective STF, the continuous-time forward filter[5] must be separated from the discrete-time loop filter by moving $H_{\mathrm{OL}}(s)$ and $H_{\mathrm{IL}}(s)$ through the input summation, together with the downconversion mixer and the sampling switch. The resulting modified block diagram[6] is shown in Figure 5.18(b), where $H_{\mathrm{IL,F}}(s)$ represents the forward component of the inner-loop filter.

The cascade of filters and mixing operations in the feedback path of the modified system depicted in Figure 5.18(b), implements the loop transfer function of the $\Delta\Sigma$ modulator. Since both the input and the output of this path are sampled, these blocks can be combined into a single discrete-time[7] filter $H'_{\mathrm{L}}(\mathrm{e}^{sT_{\mathrm{S}}})$, as shown in Figure 5.18(c).

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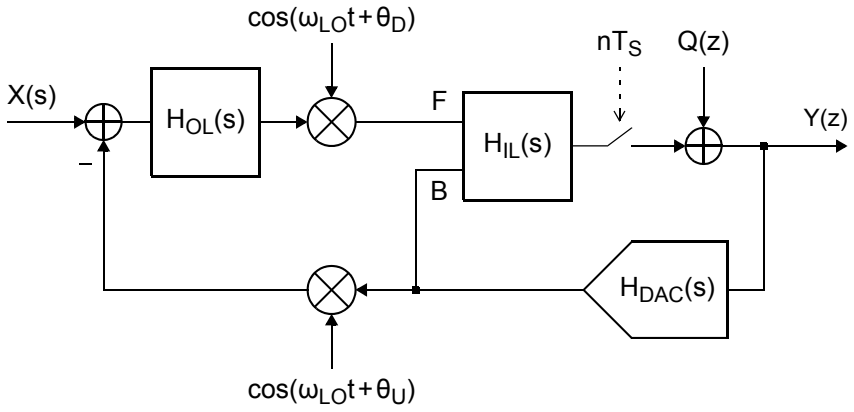
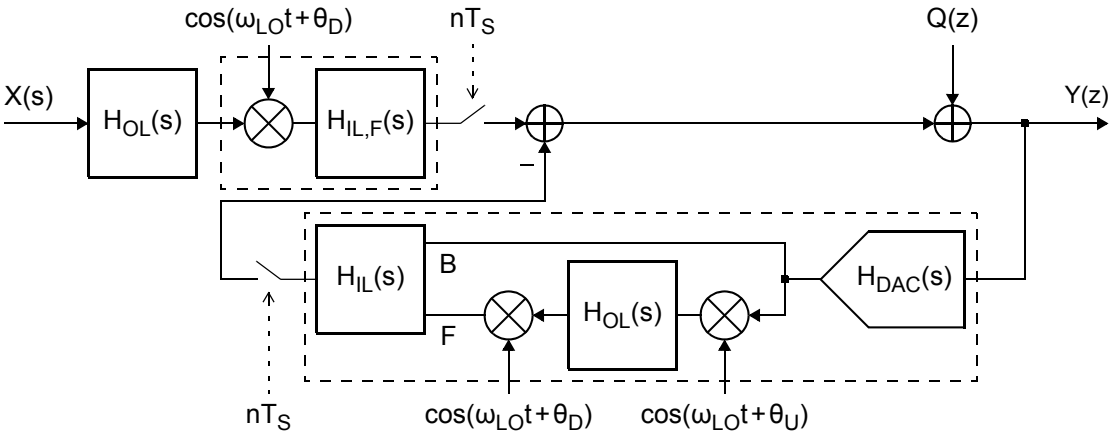
[5]The *forward filter* refers to the transfer function from the input of a $\Delta\Sigma$ modulator to its sampling switch, and excludes the effect of its feedback paths.

[6]The block diagram shown in Figure 5.18(b) is not strictly correct, since it does not account for the effect of the feedback paths on the STF prior to sampling. However, it is a useful representation for identifying the different components of the forward filter and the loop filter [Ort06].

[7]The continuous-time argument $\mathrm{e}^{sT_{\mathrm{S}}}$ is used here to emphasize the repetition of the loop filter and the NTF along the imaginary ($s = j\omega$) axis of the complex s-plane.



(a)



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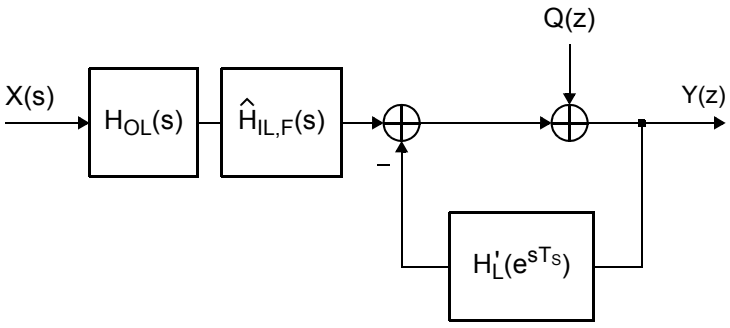


(c)

Figure 5.18: (a) The linear model of a single-path frequency-translating $\Delta\Sigma$ modulator, **(b)** the $\Delta\Sigma$ modulator in (a), modified so that the forward component of its inner-loop filter $H_{\mathrm{IL,F}}(s)$ is separated from $H_{\mathrm{IL}}(s)$, and **(c)** the model that is used to derive the effective STF.

In the forward path of the modified system, shown in Figure 5.18(b), the outer-loop filter is centred at f_{Ci}, whereas the inner-loop filter is centred at f_{Co}. In order to derive the effective STF, the forward component of the inner-loop filter $H_{\mathrm{IL,F}}(s)$ is therefore shifted by $\pm j f_{\mathrm{LO}}$, so that its frequency response is represented relative to f_{Ci}. The effective STF is referenced to the input centre frequency (f_{Ci}), rather than the output centre frequency (f_{Co}), so that the signal band can be distinguished from the image band. Since the modified inner-loop filter is different for the low-frequency and high-frequency terms of the loop response (Section 5.3), it is represented generally as $\hat{H}_{\mathrm{IL,F}}(s)$ in Figure 5.18(c).

Since a complex frequency shift is required to accurately represent the signal conditioning that is applied by the forward component of the inner-loop filter $H_{\mathrm{IL,F}}(s)$, the effective STFs of the low-frequency and high-frequency terms are only valid within the positive half of the frequency spectrum, $f \in [\,0, \infty\,]$.

5.6.2 Low-Frequency Term

For the low-frequency term (Section 5.3), the modified inner-loop filter is given by

$$\hat{H}_{\mathrm{IL,F}}(s) \;=\; \frac{1}{2}\, H_{\mathrm{IL,F}}(s - j\omega_{\mathrm{LO}}) \tag{5.34}$$

where $H_{\mathrm{IL,F}}(s)$ is shifted by $+j f_{\mathrm{LO}}$ and scaled by half to model, respectively, the frequency downconversion and the gain of the forward-path mixer. In this case, the centre frequency of the modified filter $\hat{H}_{\mathrm{IL,F}}(s)$ is equal to that of the outer-loop filter $H_{\mathrm{OL}}(s)$.

The effective STF of the low-frequency term is then derived by substituting $\hat{H}_{\mathrm{IL,F}}(s)$ in Figure 5.18(c) with the function in Equation (5.34), and solving for the closed-loop transfer function. This procedure yields

$$\hat{\mathrm{STF}}_{\mathrm{low}}(s) \;\equiv\; \left.\frac{Y(\mathrm{e}^{sT_{\mathrm{S}}})}{X(s)}\right|_{Q(z)\,=\,0} \;=\; \frac{1}{2}\frac{H_{\mathrm{OL}}(s) H_{\mathrm{IL,F}}(s - j\omega_{\mathrm{LO}})}{1 + H'_{\mathrm{L}}(\mathrm{e}^{sT_{\mathrm{S}}})} \tag{5.35}$$

Figure 5.19(a) uses this equation to plot the STF of the low-frequency term for a frequency-translating $\Delta\Sigma$ modulator that is designed with $f_{\mathrm{LO}} = f_{\mathrm{S}}$ and $f_{Co} = 1/4 f_{\mathrm{S}}$.

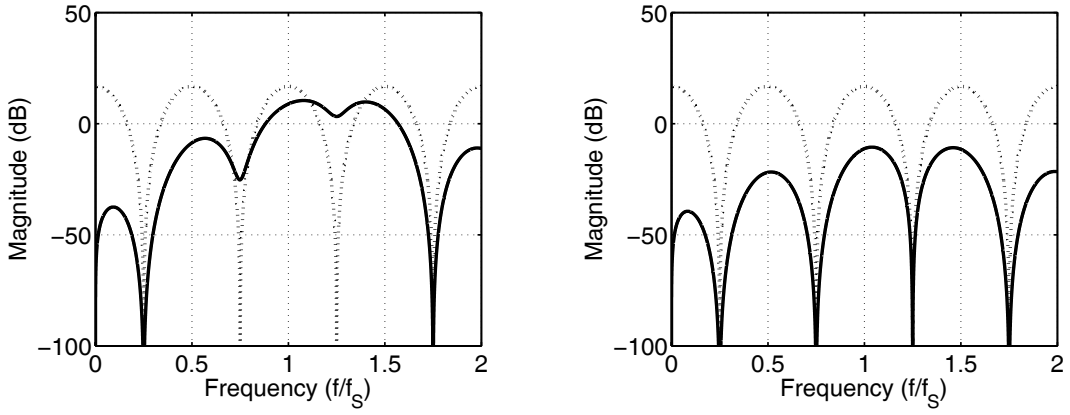


Figure 5.19: Simulated STF for the: **(a)** low-frequency term, and **(b)** high-frequency term of a single path frequency-translating ΔΣ modulator with $f_{Ci} = 5/4 f_S$. (STF — and NTF $\cdots$)

Inherent Image-Reject Filtering

The outer-loop filter of a single-path frequency-translating ΔΣ modulator implements partial image-reject filtering for the downconversion mixer in its forward path. This inherent filtering is applied to both its input and feedback signals, and reduces the design requirements on the image-reject filter that must be included prior to its input (Section 5.1).

The inherent image-reject filtering of a single-path frequency-translating ΔΣ modulator can be evaluated from the effective STF of its low-frequency term as

$$\mathrm{IR} = \frac{|\hat{\mathrm{STF}}_{\mathrm{low}}(j2\pi f_{Ci,\,\mathrm{img}})|}{|\hat{\mathrm{STF}}_{\mathrm{low}}(j2\pi f_{Ci})|} \tag{5.36}$$

where $f_{Ci,\,\mathrm{img}}$ is the centre frequency of the image band.

5.6.3 High-Frequency Term

For the high-frequency term (Section 5.3), the modified inner-loop filter is given by

$$\hat{H}_{\mathrm{IL,F}}(s) \;=\; \frac{1}{2}\, H_{\mathrm{IL,F}}(s + j\omega_{\mathrm{LO}}) \tag{5.37}$$

where $H_{\mathrm{IL,F}}(s)$ is shifted by $-jf_{\mathrm{LO}}$ and scaled by half to model, respectively, the frequency upconversion and the gain of the forward-path mixer. In this case, the centre frequency of the modified filter $\hat{H}_{\mathrm{IL,F}}(s)$ is offset by $2f_{\mathrm{LO}}$ from that of the outer-loop filter $H_{\mathrm{OL}}(s)$.

The effective STF of the high-frequency term is then derived by substituting $\hat{H}_{\mathrm{IL,F}}(s)$ in Figure 5.18(c) with the function in Equation (5.37), and solving for the closed-loop transfer function. This procedure yields

$$\hat{\mathrm{STF}}_{\mathrm{high}}(s) \;\equiv\; \left.\frac{Y(\mathrm{e}^{sT_{\mathrm{S}}})}{X(s)}\right|_{Q(z)=0} = \frac{1}{2}\frac{H_{\mathrm{OL}}(s)H_{\mathrm{IL,F}}(s + j\omega_{\mathrm{LO}})}{1 + H'_{\mathrm{L}}(\mathrm{e}^{sT_{\mathrm{S}}})} \tag{5.38}$$

Figure 5.19(b) uses this equation to plot the STF of the high-frequency term for a frequency-translating $\Delta\Sigma$ modulator that is designed with $f_{\mathrm{LO}} = f_{\mathrm{S}}$ and $f_{\mathrm{C}o} = 1/4f_{\mathrm{S}}$.

Attenuation of the High-Frequency Term

A number of advantages are achieved by significantly attenuating the high-frequency term of a frequency-translating $\Delta\Sigma$ modulator, as described in Section 5.3. The attenuation of the high-frequency term, relative to the low-frequency term, can be derived from the expressions in Equations (5.35) and (5.38) as

$$\mathrm{HFA}(j2\pi f) \;=\; \left|\frac{\hat{\mathrm{STF}}_{\mathrm{high}}\big(j2\pi f\big)}{\hat{\mathrm{STF}}_{\mathrm{low}}\big(j2\pi f\big)}\right| \;=\; \left|\frac{H_{\mathrm{IL,F}}\big(j2\pi[f + f_{LO}]\big)}{H_{\mathrm{IL,F}}\big(j2\pi[f - f_{LO}]\big)}\right| \tag{5.39}$$

Here, the relative magnitude of the high-frequency and low-frequency terms only depends on the forward-component of the inner-loop filter $H_{\mathrm{IL,F}}(s)$.

5.7 Conclusion

This chapter presented an architecture, and associated design considerations, for a frequency translating ΔΣ modulator that is based on single-path mixing. It described the procedure to synthesize this single-path architecture from a prototype bandpass ΔΣ modulator, and also derived constraints that must be satisfied in order to achieve the synthesis. These constraints can be summarized as follows:

- The sampling period T_S must be an integer multiple of $T_{LO}/2$, where T_{LO} is the period of the LO signal (Section 5.2.1).
- The inner-loop filter must have a bandpass characteristic (Section 5.2.2).

This chapter discussed the realization of both the high-frequency, or *outer-loop* filter of a frequency-translating ΔΣ modulator, and its low-frequency, or *inner-loop* filter. Section 5.3 developed an *effective* transfer function for the time-varying response of the outer-loop path, and Section 5.4 described the importance of using both feedback and feedforward coefficient paths to realize the inner-loop filter. The feedforward paths are used to reduce the distortion that is introduced by the forward-path mixer, whereas the feedback paths are used to reduce the LO phase sensitivity, and the implementation requirements on the inner-loop filter. This chapter further examined how the noise-shaping performance of a frequency-translating ΔΣ modulator is affected by errors in the phase of its LO signal. Section 5.5 demonstrated that LO phase sensitivity of the NTF can be reduced by decreasing its out-of-band gain.

Figure 5.14 provided a general block diagram for a single-path frequency-translating ΔΣ modulator with a feedforward-feedback loop-filter topology. Chapters 6, 7, and 8 present the system architecture, circuit implementation, and measurement results for an experimental ΔΣ modulator that is based on the single-path architecture in Figure 5.14.

Chapter 6

System Architecture *of the* Experimental $\Delta\Sigma$ Modulator

THIS CHAPTER presents a complete system architecture for an experimental single-path frequency-translating $\Delta\Sigma$ modulator. This experimental $\Delta\Sigma$ modulator is designed to operate on a wideband (4 MHz) signal that is centred at a high IF (225 MHz), while providing moderate (10 bit) resolution. It is used to validate the NTF synthesis procedure described in Section 5.2, and the design techniques presented in Sections 5.3, 5.4, and 5.5.

This chapter is divided into five sections. Section 6.1 describes the system architecture of the experimental $\Delta\Sigma$ modulator, and defines its frequency and phase parameters. Section 6.2 presents the synthesis of the experimental $\Delta\Sigma$ modulator from a prototype NTF, and derives its loop-filter coefficients. The remainder of this chapter analyses the results of behavioural simulations. Section 6.3 examines the ideal performance of the experimental $\Delta\Sigma$ modulator, and verifies the accuracy of both its NTF and STF. Section 6.4 examines the effect of circuit noise, non-linear distortion, and clock jitter on its performance, and Section 6.5 examines the effect of component variation and mismatch.

6.1 Architecture of the Experimental ΔΣ Modulator

Figure 6.1 depicts a simplified block diagram for the experimental frequency-translating ΔΣ modulator. Its topology is based on the single-path architecture presented in Chapter 5, and it is designed with a 6th-order continuous-time loop filter and a 3-bit internal quantizer. The high-frequency *outer-loop* filter is implemented using an LC resonator (RESON1), which has a centre frequency of f_{Ci}. The low-frequency *inner-loop* filter is implemented using a cascade of active-RC resonators (RESON2 and RESON3), each of which has a centre frequency of f_{Co}. The downconversion operation is implemented using a switching mixer and the upconversion operation is implemented using a current-steering DAC that has raised-cosine pulse shaping, as described in Section 3.2.1.

The experimental ΔΣ modulator (Figure 6.1) is designed to convert a 4 MHz signal band that is centred at $f_{Ci} = 225$ MHz. It uses an LO signal with a frequency of $f_{LO} = 200$ MHz to downconvert the signal band to $f_{Co} = 25$ MHz, and samples at $f_S = 100$ MHz. Here, f_{LO} and f_S are selected such that they satisfy the constraints in Section 5.2.1. Table 6.1 summarizes the frequency parameters of the experimental ΔΣ modulator.

Table 6.1: Frequency parameters of the experimental ΔΣ modulator.

Parameter		Value
Input Centre Frequency	f_{Ci}	225 MHz
Output Centre Frequency	f_{Co}	25 MHz
LO Frequency	f_{LO}	200 MHz
Sampling Frequency	f_S	100 MHz

6.1.1 Mixing Considerations

Figures 6.2(a)-(f) plot the frequency spectrum at various points around the feedback loop of the experimental ΔΣ modulator (Figure 6.1). These plots demonstrate important properties of the downconversion and upconversion mixing processes, as described next.

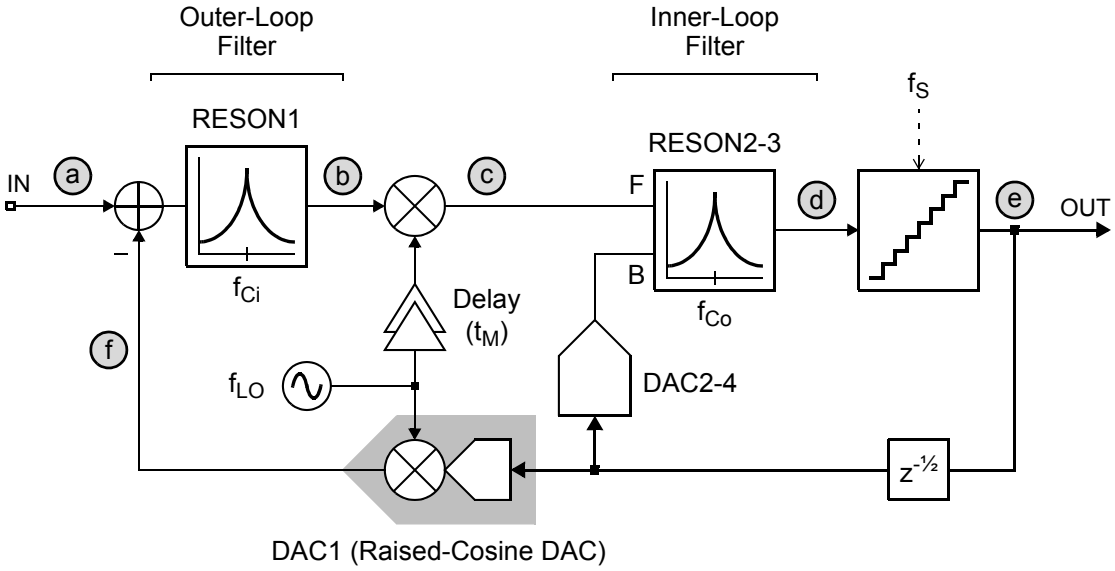


Figure 6.1: Simplified block diagram for the experimental ΔΣ modulator.

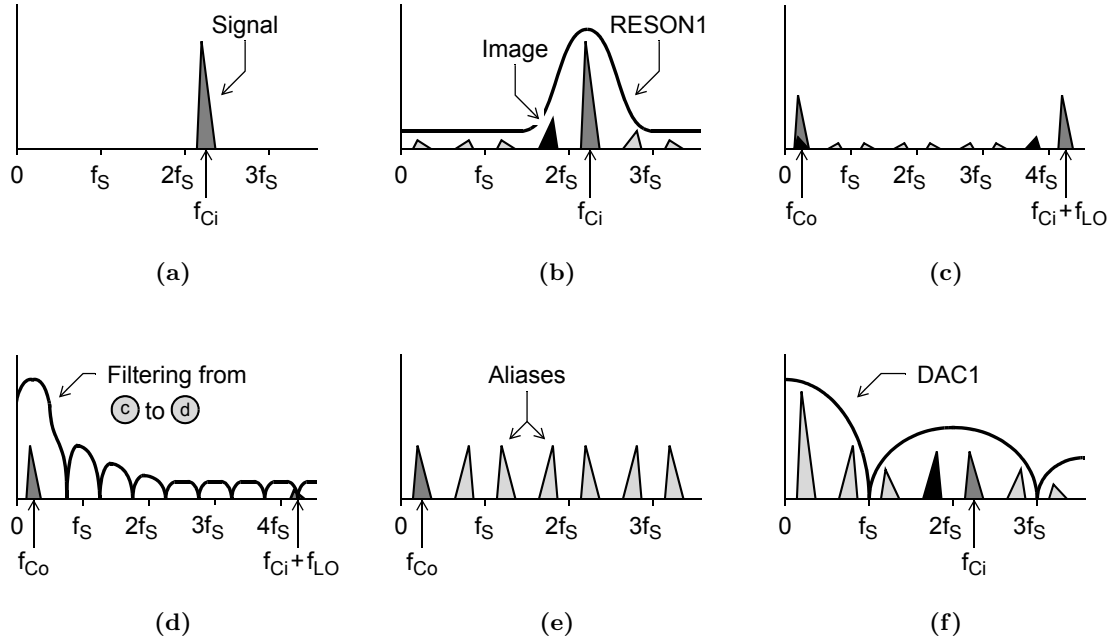


Figure 6.2: Frequency spectrum at various points around the feedback loop of the experimental ΔΣ modulator, shown in Figure 6.1.

Downconversion

In the forward path of the experimental ΔΣ modulator, the downconversion mixer splits the loop response into two mixing terms, as shown in Figure 6.2(c). Here, the *low-frequency* term is centred at $f_{Co} \equiv (f_{Ci} - f_{LO})$, and the *high-frequency* term is centred at $(f_{Ci} + f_{LO})$.

The high-frequency term of the loop response is attenuated by the STF of the continuous-time loop filter, from the output of the downconversion mixer to the input of the quantizer, as shown in Figure 6.2(d). The attenuated term is then subsampled at the quantizer, and is added to the low-frequency term to form the overall loop response.

The high-frequency term falls well outside the bandwidths of the amplifiers that are used to implement the active-RC resonators (RESON2 and RESON3), and is therefore sensitive to process variations (Section 6.1.3). Furthermore, due to its interdependence with the STF, it is difficult to *accurately* include the high-frequency term in the NTF synthesis. Accordingly, the loop filter of the experimental ΔΣ modulator is designed such that its STF significantly attenuates the high-frequency term and, in this way, reduces its contribution to the overall loop response, as described in Section 5.4.2.

Upconversion

In the feedback path of the experimental ΔΣ modulator, the mixer upconverts both the input signal and its image, as shown in Figure 6.2(f). This image is significantly attenuated by the LC resonator (RESON1), and does not limit the dynamic range.

In order to maximize the attenuation of the image, as well as the alias components of the feedback signal, the output centre frequency (f_{Co}) of the experimental ΔΣ modulator is set to $f_S/4$, as shown in Figure 6.2(b). Note that setting the output centre frequency to a simple fraction of the sampling frequency also reduces the complexity of the DAC mismatch-shaping logic and the digital image-reject mixing [Sch06c].

6.1.2 Phase Considerations

The loop response of the experimental ΔΣ modulator includes scaling factors that are set by the phase difference between its LO signal and sampling clock:[1] the low-frequency term is a function of $(\theta_U - \theta_D)$, and the high-frequency term is a function of $(\theta_U + \theta_D)$. By significantly attenuating the high-frequency term, as described in Section 6.1.1, the phase dependence of the loop response is reduced to that of its low-frequency term, $\theta_M \equiv (\theta_U - \theta_D)$.

The phase component of the low-frequency term (θ_M) is set using a delay block, as shown in Figure 6.1. The delay, denoted as t_M, is implemented on-chip, and is therefore sensitive to process variations. As outlined in Section 5.5.1, the phase sensitivity of a frequency-translating ΔΣ modulator can be improved by decreasing the out-of-band gain of its NTF. Accordingly, the NTF of the experimental ΔΣ modulator is designed with an out-of-band gain[2] of 12 dB in order to reduce its phase sensitivity.

The relative LO phase (θ_M) of the experimental ΔΣ modulator is set to $\pi/4$, as outlined in Section 5.5.2. This requires a delay of $t_M = (\theta_M/\omega_{LO})$, or 625 ps, in Figure 6.1. The phase of the LO signal that is applied to the upconversion mixer (θ_U) is then set to π, so that the outer-loop feedback DAC (DAC1) has a raised-cosine pulse of the form shown in Figure 3.5. Table 6.2 summarizes the phase parameters of the experimental ΔΣ modulator.

Table 6.2: Phase parameters of the experimental ΔΣ modulator.

Parameter		Value
Relative LO Phase	θ_M	$\pi/4$
Upconversion LO Phase	θ_U	π

[1] Recall that θ_U and θ_D represent the phases of the LO signal, relative to an edge of the sampling clock, that are applied to the upconversion and downconversion mixers, respectively.

[2] For an Nth-order bandpass ΔΣ modulator with a centre frequency of $f_S/4$, the NTF can be designed with a maximum out-of-band gain of $\|H\|_\infty = 20\log_{10}(2^{N/2})$. For $N = 6$, $\|H\|_\infty \cong 18.1$ dB.

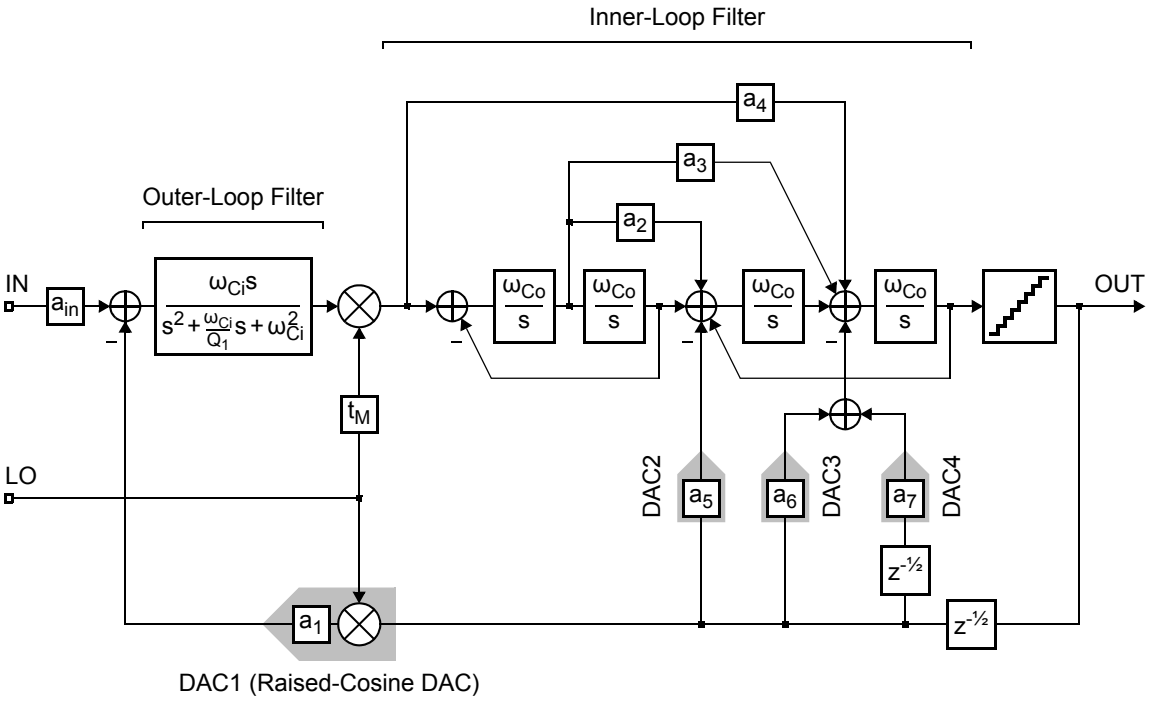


Figure 6.3: Complete block diagram for the experimental ΔΣ modulator.

6.1.3 Loop Filter

Figure 6.3 shows a complete block diagram of the experimental ΔΣ modulator. This section derives an expression for the *effective* loop transfer function of the experimental architecture, where the associated scaling coefficients are derived in Section 6.2 according to a prototype discrete-time NTF.

Outer-Loop Filter

In Figure 6.3, the transfer function of the outer-loop filter is given by

$$H_{\mathrm{OL}}(s) \;=\; \frac{\omega_{Ci}\, s}{s^2 + \frac{\omega_{Ci}}{\mathrm{Q}_1} s + \omega_{Ci}^2} \tag{6.1}$$

where ω_{Ci} is the input centre frequency of the experimental ΔΣ modulator (Table 6.1), and Q_1 is the quality factor of the LC resonator (RESON1).

The *effective* transfer function of the outer-loop path[3] can be derived using the approach described in Section 5.3. This results in

$$\hat{H}_{\mathrm{OL}}(s) \;=\; \frac{a_1}{2}\,\frac{\left(d_1\frac{1}{2\hat{\mathrm{Q}}_1}+d_2\right)\omega_{\mathrm{C}o}s+d_1\omega_{\mathrm{C}o}^2}{\left(s+\frac{\omega_{\mathrm{C}o}}{2\hat{\mathrm{Q}}_1}\right)^2+\omega_{\mathrm{C}o}^2} \tag{6.2}$$

where $\omega_{\mathrm{C}o}$ is the output centre frequency of the experimental ΔΣ modulator, and $\hat{\mathrm{Q}}_1$ is the *effective* quality factor of the response through its outer-loop path. Here, $\hat{\mathrm{Q}}_1 \equiv (\omega_{\mathrm{C}o}/\omega_{\mathrm{C}i})\,\mathrm{Q}_1$, and coefficients d_1 and d_2 depend on the relative LO phase (θ_{M}).

Inner-Loop Filter

In Figure 6.3, the transfer function of the inner-loop filter has both a forward component and a feedback component (Section 5.4.2). These components are given by

$$H_{\mathrm{IL,F}}(s) \;=\; \frac{a_4\,\omega_{\mathrm{C}o}s}{(s^2+\omega_{\mathrm{C}o}^2)}+\frac{a_3\,\omega_{\mathrm{C}o}^2}{(s^2+\omega_{\mathrm{C}o}^2)}+\frac{a_2\,\omega_{\mathrm{C}o}^3 s}{(s^2+\omega_{\mathrm{C}o}^2)^2}+\frac{\omega_{\mathrm{C}o}^4}{(s^2+\omega_{\mathrm{C}o}^2)^2} \tag{6.3}$$

$$H_{\mathrm{IL,B}}(s) \;=\; \frac{a_6\,\omega_{\mathrm{C}o}s}{(s^2+\omega_{\mathrm{C}o}^2)}+\frac{a_5\,\omega_{\mathrm{C}o}^2}{(s^2+\omega_{\mathrm{C}o}^2)} \tag{6.4}$$

The additional *delayed* coefficient path (a_7) is required to compensate for excess loop delay, and is discussed in Section 6.1.4.

The effective loop transfer function of the experimental ΔΣ modulator is then derived by combining the expressions in Equations (6.2), (6.3), and (6.4). This results in

$$\hat{H}_{\mathrm{L}}(s) \;=\; \hat{H}_{\mathrm{OL}}(s)\,H_{\mathrm{IL,F}}(s)+H_{\mathrm{IL,B}}(s) \tag{6.5}$$

Note that Equation (6.5) corresponds to Equation (5.30), derived in Section 5.4.2.

[3]The *outer-loop path* of a frequency-translating ΔΣ modulator refers to the signal path from the input of its upconversion mixer to the output of its downconversion mixer (Section 2.3.1).

The *hybrid* feedforward-feedback loop-filter topology of the experimental ΔΣ modulator provides a number of performance advantages, as described below.

Feedforward Paths

The loop filter of the experimental ΔΣ modulator (Figure 6.3) is designed with feedforward coefficient paths (a_2, a_3, a_4) to decrease the magnitude of the input-signal component that is passed by the switching mixer. This reduces the distortion that is introduced by the mixer, and facilitates an increase in the coefficient (a_1) of the outer-loop path (Section 5.4.1).

The feedforward paths of the loop filter are configured such that a summing amplifier is not required at the input of the quantizer (Figure 6.3). This reduces the power consumption of the experimental ΔΣ modulator, and decreases the delay through its feedback loop.

Feedback Paths

The loop filter of the experimental ΔΣ modulator is also designed with feedback coefficient paths (a_5, a_6) to increase the attenuation of the high-frequency term. Since f_{LO} must be an integer multiple of $f_S/2$, in order to satisfy the sampling constraint derived in Section 5.2.1, the $2f_{LO}$ frequency separation between the high-frequency term and the low-frequency term corresponds to a multiple of f_S. As a result, the signal-band component of the high-frequency term falls inside one of the notches of the STF and is significantly attenuated. The feedback paths of the loop filter are used to improve the filtering characteristic of the STF, so that it also attenuates the out-of-band components of the high-frequency term.

In addition to providing the advantages described in Section 5.4.2, attenuating the high-frequency term reduces the gain-bandwidth requirements of the amplifiers that are used to implement the active-RC resonators (RESON2 and RESON3). In order to accurately process the high-frequency term, these amplifiers must provide a high gain at its centre frequency. In the absence of a high gain, the high-frequency term is sensitive to process-related variations in the circuit parameters of the active-RC resonators, which could reduce the stability of the experimental ΔΣ modulator. By attenuating the high-frequency term, the feedback paths of the loop filter reduce the effect of these variations, and therefore reduce the gain-bandwidth requirements on the amplifiers.

6.1.4 Feedback DACs

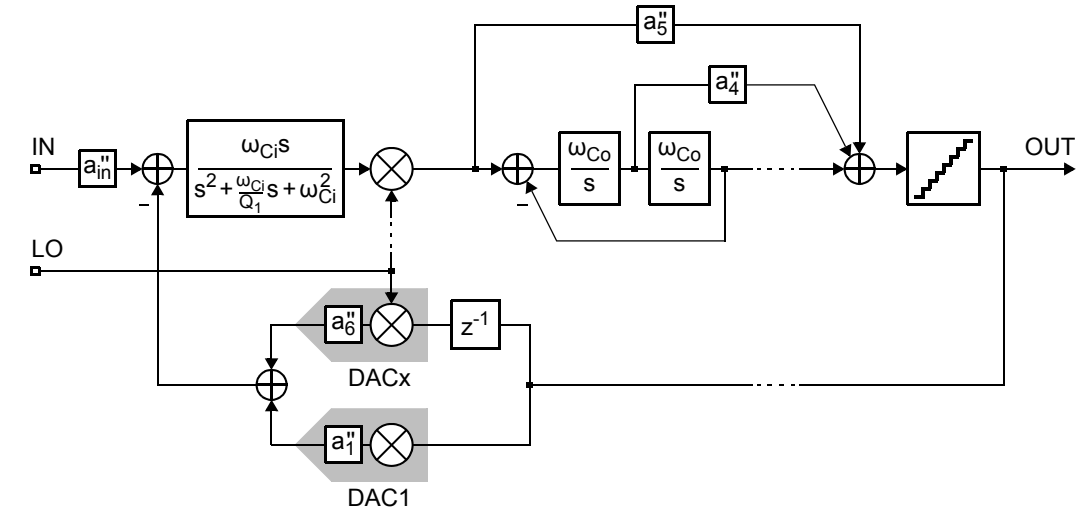
The feedback DACs of the experimental ΔΣ modulator (Figure 6.3) are configured in a way that reduces their implementation complexity and associated power consumption relative to a conventional bandpass ΔΣ modulator.

Additional Coefficient Path

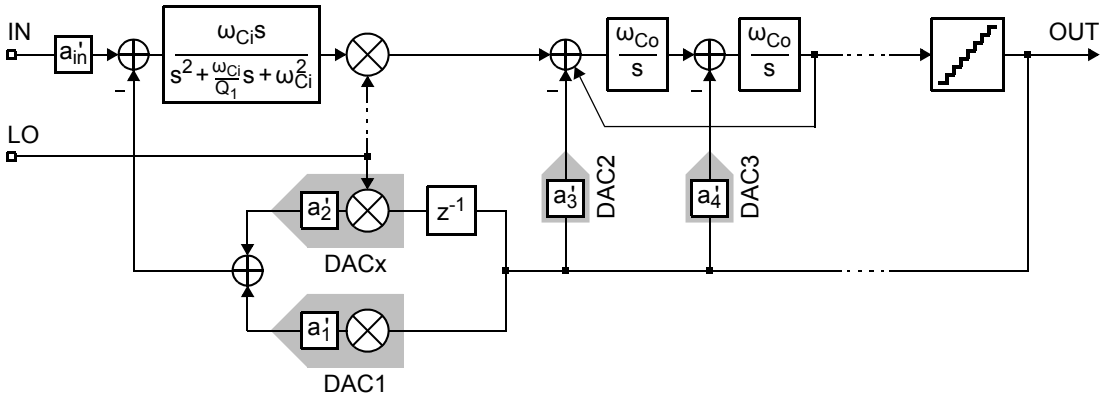
In addition to the advantages outlined in Section 6.1.3, the hybrid feedforward-feedback loop-filter topology of the experimental ΔΣ modulator facilitates an efficient implementation of the additional coefficient path that is required when using an LC resonator.

As illustrated in Figure 6.3, the LC resonator (RESON1) introduces a 2nd-order loop-filter term, but only provides one coefficient path. As a result, an additional coefficient path must be created to achieve full control over the design of the NTF. Figure 6.4 provides simplified block diagrams for equivalent strictly-feedforward and strictly-feedback configurations of the experimental ΔΣ modulator (Figure 6.3). In both diagrams, the required coefficient path is created by connecting a second DAC, referred to here as DACx, at the input summation of the ΔΣ modulator. This additional DAC can be implemented using either a modified pulse shape [Sho95b], or a delay [Bei05], as shown in Figure 6.4, however it has the same complexity and thermal-noise requirements as DAC1.

The hybrid loop filter of the experimental ΔΣ modulator (Figure 6.3) sets the high-order terms of the loop response using feedforward paths (a_2, a_3, a_4), and sets the low-order terms using feedback paths (a_5, a_6). Accordingly, relative to the strictly-feedback configuration in Figure 6.4(b), it replaces DACx (a_2') with a feedforward path (a_2) and, relative to the strictly-feedforward configuration in Figure 6.4(a), it replaces DACx (a_6'') with DAC3 (a_6). Note that, since DAC3 is connected at the input of the last integrator, rather than at the input of the ΔΣ modulator, it has lower thermal-noise requirements than DACx, and therefore consumes less power. Furthermore, since DAC3 is connected to the low-frequency section of the loop filter, it can be implemented with rectangular pulse shaping, and is less complex than DACx, which uses raised-cosine pulse shaping.



(a)



(b)

Figure 6.4: Block diagrams for: **(a)** a strictly-feedforward, and **(b)** a strictly-feedback configuration of the ΔΣ modulator in Figure 6.3, showing the additional required coefficient path (DACx).

Excess Loop Delay Compensation

The experimental ΔΣ modulator (Figure 6.3) is designed with a continuous-time loop filter, and therefore requires a direct feedback path to its quantizer to compensate for the effect of excess loop delay (Section 3.1.1). The excess loop delay of the experimental ΔΣ modulator is set to half of the sampling period (i.e., $T_S/2$), which provides sufficient time for its quantizer to settle and for its DAC mismatch-shaping logic to operate.

The excess loop delay compensation of the experimental ΔΣ modulator is implemented using the technique described in [Mit06], where the direct feedback term of the loop response is *differentiated* so that it can be applied to the input of the final integrator, rather than the input of the quantizer. This technique removes the requirement for a summing amplifier prior to the quantizer, and therefore reduces the overall power consumption. The direct feedback term of the loop response is implemented by coefficient paths a_6 and a_7 (DAC3 and DAC4) in Figure 6.3. It is differentiated, as outlined above, by delaying the input of coefficient path a_7 by $T_\mathrm{S}/2$ relative to that of coefficient path a_6.

In order to accommodate a delayed coefficient path (a_7), the impulse-invariant transform in Equation (5.1) must be modified to

$$H'_\mathrm{L}(z) \;=\; \underset{s\,\to\,z}{\mathrm{IIT}}\Big\{\hat{H}_\mathrm{L}(s)\,H_\mathrm{DAC}(s)\Big\} + \underset{s\,\to\,z}{\mathrm{IIT}}\Big\{\hat{H}_{\mathrm{L},\,d}(s)\,H_{\mathrm{DAC},\,d}(s)\Big\} \tag{6.6}$$

where $\hat{H}_\mathrm{L}(s)$ is the main component of the loop transfer function (Section 6.1.3), and $H'_\mathrm{L}(z)$ is the prototype discrete-time loop transfer function. In Figure 6.3, the delayed component of the loop transfer function is given by

$$\hat{H}_{\mathrm{L},\,d}(s) \;=\; \frac{a_7\,\omega_{\mathrm{C}o}s}{(s^2+\omega_{\mathrm{C}o}^2)} \tag{6.7}$$

and the transfer functions of the feedback DACs are equal to

$$H_\mathrm{DAC}(s) \;=\; \frac{1}{s}\Big(\mathrm{e}^{-s0.5T_\mathrm{S}} - \mathrm{e}^{-s1.5T_\mathrm{S}}\Big) \tag{6.8}$$

$$H_{\mathrm{DAC},\,d}(s) \;=\; \frac{1}{s}\Big(\mathrm{e}^{-sT_\mathrm{S}} - \mathrm{e}^{-s2T_\mathrm{S}}\Big) \tag{6.9}$$

Here, DAC1–DAC3 implement $H_\mathrm{DAC}(s)$, and DAC4 implements $H_{\mathrm{DAC},\,d}(s)$.

6.2 NTF Design and Synthesis

The loop filter of the experimental ΔΣ modulator is composed of three resonators, as shown in Figure 6.1. Each resonator introduces one pair of complex-conjugate zeros into the NTF, where the position of a zero pair is determined by the centre frequency and quality factor of its associated resonator. The high-frequency resonator (RESON1) is centred at f_{Ci}, in order to maximize the attenuation of the image and alias components of the upconverted feedback signal (Section 6.1.1). The low-frequency resonators (RESON2 and RESON3) are then centred at f_{Co}, in order to improve the signal-swing reduction provided by the feedforward paths of the loop filter (Section 6.1.3). Accordingly, the zeros of the prototype NTF are placed at the centre frequency of the signal band.

The poles of the NTF are configured so that it has a maximally-flat magnitude response with an out-of-band gain of 12 dB. The out-of-band gain has been reduced from its maximum upper limit in order to reduce the sensitivity of the loop response to variations in the phases of the LO signal, as described in Section 6.1.2.

The prototype NTF of the experimental ΔΣ modulator was designed with the specified characteristics using the Delta-Sigma Toolbox [Sch04]. It has a general form of

$$\mathrm{NTF}(z) \;=\; \frac{\left(z^2 + \mathrm{e}^{-\pi/(2\hat{\mathrm{Q}}_1)}\right)\left(z^2+1\right)^2}{\prod_{i=1}^{3}\left(z + z_{\mathrm{p}i}\right)\left(z + z_{\mathrm{p}i}^*\right)} \tag{6.10}$$

where the zeros, poles, and gain are listed in Table 6.3.

The high-frequency resonator (RESON1) has a quality factor of $\mathrm{Q}_1 = 25$, which is set by its implementation (Section 6.5.1). As a result, the outer-loop path of the experimental ΔΣ modulator has an effective quality factor of $\hat{\mathrm{Q}}_1 \cong 3$ (Section 6.1.3) for the selected frequency parameters (f_{Ci} and f_{Co} in Table 6.1). The low-frequency resonators (RESON2 and RESON3) have nominal quality factors of Q_2, $\mathrm{Q}_3 = \infty$. Section 6.5.1 examines how the performance of the experimental ΔΣ modulator is affected by Q_1, Q_2, and Q_3.

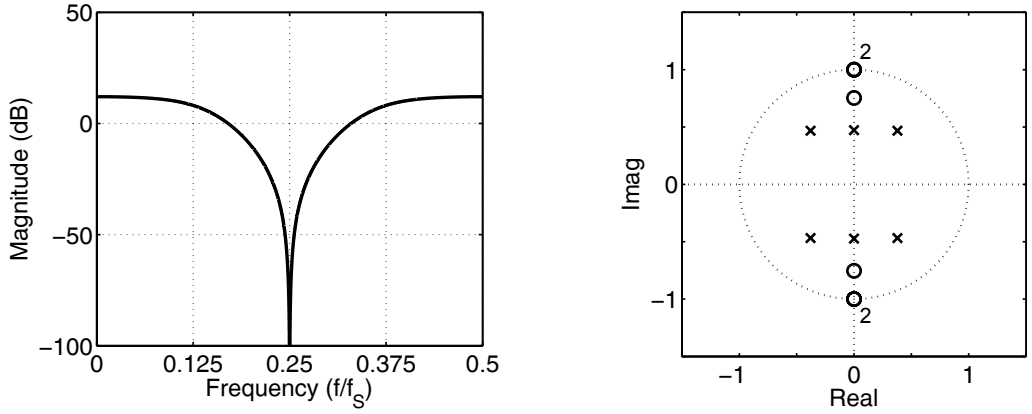


Figure 6.5: Magnitude response and pole-zero map of the prototype NTF.

Figure 6.5 plots the magnitude response and associated pole-zero map of NTF(z). Here, the zeros introduced by the low-frequency resonators (RESON2 and RESON3) are on the unit circle (i.e., $|z| = 1$), since these resonators have infinite quality factors. The zeros introduced by the high-frequency resonator (RESON1) are shifted toward the origin (i.e., $|z| = 0$), since this resonator has a finite quality factor.

Table 6.3: Zeros, poles, and gain of the prototype NTF.

Parameter		Value
Zeros	z_{z1}	$\pm\ 1.00j$
	z_{z2}	$\pm\ 1.00j$
	z_{z3}	$\pm\ 0.75j$
Poles	z_{p1}	$0.38 \pm 0.47j$
	z_{p2}	$-\ 0.38 \pm 0.47j$
	z_{p3}	$\pm\ 0.47j$
Gain		1

Table 6.4: Loop-filter coefficients of the experimental ΔΣ modulator.

Coefficient	a_1	a_2	a_3	a_4	a_5	a_6	a_7
Value	−0.1546	−0.4169	0.5846	0.7757	−1.0519	−0.3774	0.4480

In order to synthesize the prototype NTF, specified in Equation (6.10), the loop transfer function of the experimental ΔΣ modulator must satisfy the impulse-invariance relationship in Equation (6.6). This relationship can alternatively be expressed as

$$\underset{s\,\to\,z}{\mathrm{IIT}}\Big\{\hat{H}_{\mathrm{L}}(s)H_{\mathrm{DAC}}(s)\Big\}+\underset{s\,\to\,z}{\mathrm{IIT}}\Big\{\hat{H}_{\mathrm{L},\,d}(s)H_{\mathrm{DAC},\,d}(s)\Big\}\;=\;\frac{1}{\mathrm{NTF}(z)}-1 \tag{6.11}$$

where $H_{\mathrm{DAC}}(s)$ and $H_{\mathrm{DAC},\,d}(s)$ are defined in Equations (6.8) and (6.9).

The main and delayed components of the loop transfer function, $\hat{H}_{\mathrm{L}}(s)$ and $\hat{H}_{\mathrm{L},\,d}(s)$, are derived by substituting Equations (6.2), (6.3), and (6.4) into Equation (6.5), where

$$\begin{aligned}\hat{H}_{\mathrm{L}}(s)\;=\;&\frac{a_1}{2}\frac{\big[d_1/(2\hat{\mathrm{Q}}_1)+d_2\big]\omega_{\mathrm{Co}}s+d_1\omega_{\mathrm{Co}}^2}{\big[s+\omega_{\mathrm{Co}}/(2\hat{\mathrm{Q}}_1)\big]^2+\omega_{\mathrm{Co}}^2}\left[\frac{a_4\,\omega_{\mathrm{Co}}s}{(s^2+\omega_{\mathrm{Co}}^2)}+\frac{a_3\,\omega_{\mathrm{Co}}^2}{(s^2+\omega_{\mathrm{Co}}^2)}\right]\\&+\;\frac{a_1}{2}\frac{\big[d_1/(2\hat{\mathrm{Q}}_1)+d_2\big]\omega_{\mathrm{Co}}s+d_1\omega_{\mathrm{Co}}^2}{\big[s+\omega_{\mathrm{Co}}/(2\hat{\mathrm{Q}}_1)\big]^2+\omega_{\mathrm{Co}}^2}\left[\frac{a_2\,\omega_{\mathrm{Co}}^3s}{(s^2+\omega_{\mathrm{Co}}^2)^2}+\frac{\omega_{\mathrm{Co}}^4}{(s^2+\omega_{\mathrm{Co}}^2)^2}\right]\\&+\;\frac{a_6\,\omega_{\mathrm{Co}}s}{(s^2+\omega_{\mathrm{Co}}^2)}+\frac{a_5\,\omega_{\mathrm{Co}}^2}{(s^2+\omega_{\mathrm{Co}}^2)}\end{aligned} \tag{6.12}$$

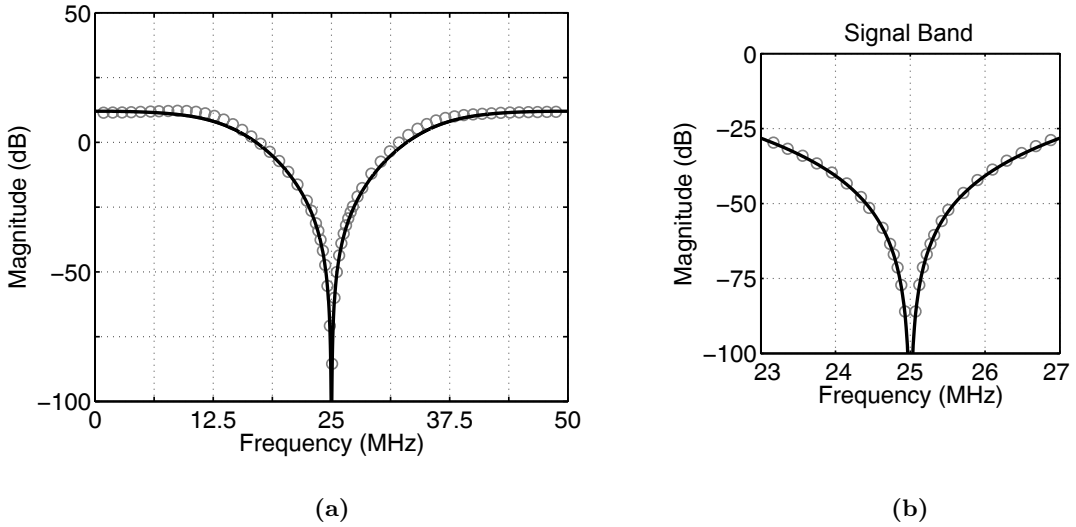
$$\hat{H}_{\mathrm{L},\,d}(s)\;=\;\frac{a_7\,\omega_{\mathrm{Co}}^2}{(s^2+\omega_{\mathrm{Co}}^2)} \tag{6.13}$$

The coefficients (a_1–a_7) of $\hat{H}_{\mathrm{L}}(s)$ and $\hat{H}_{\mathrm{L},\,d}(s)$ are solved by substituting the expressions in Equations (6.10), (6.12), and (6.13) into Equation (6.11), and equating corresponding powers of z on each side of (6.11). Table 6.4 lists the coefficients that result from this procedure, and correspond to the block diagram in Figure 6.3.

6.3 Behavioural Simulations

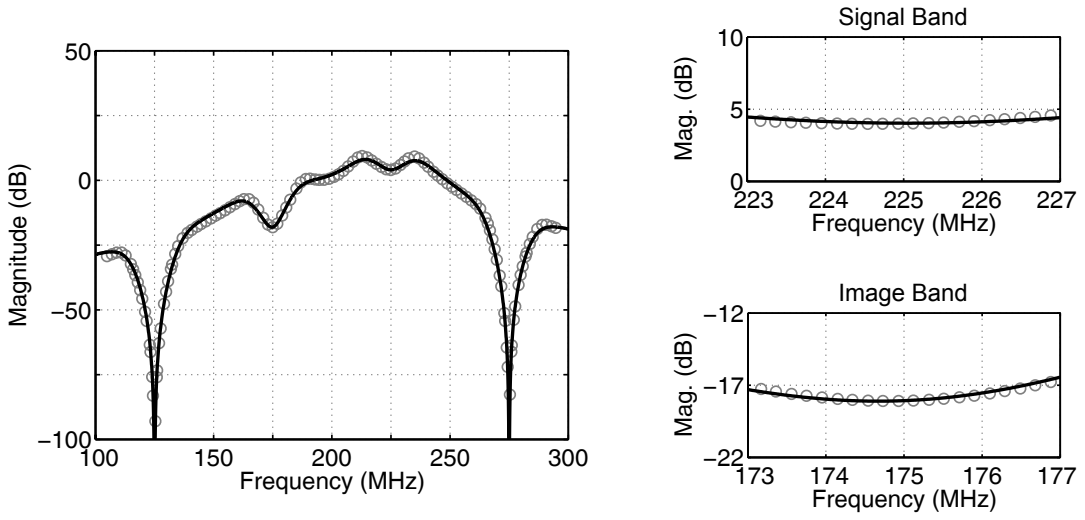
This section provides behavioural (system-level) simulation results for the experimental $\Delta\Sigma$ modulator (Figure 6.3), and compares its NTF and STF to the prototype transfer functions. In this section, the functional blocks of the experimental architecture (loop filter, quantizer, and feedback DACs) are simulated using ideal models. The effect of associated circuit-level non-idealities is discussed in Sections 6.4 and 6.5.

Figure 6.6(a) compares the NTF of the experimental $\Delta\Sigma$ modulator (Figure 6.3), derived from behavioural simulations, to the magnitude response of its prototype NTF (Figure 6.5). This plot demonstrates the accuracy of the synthesis procedure outlined in Section 5.2, and validates the techniques presented in Sections 5.3, 5.4, and 5.5. The deviation between these two plots, in particular around $f_S/8$ and $3f_S/8$, is a result of the limited attenuation of the high-frequency term (Section 5.4). The additional contribution of the high-frequency term to the loop response of the experimental $\Delta\Sigma$ modulator shifts the poles of its NTF from their nominal configuration (Figure 6.5). Figure 6.6(b) shows the signal band of the experimental $\Delta\Sigma$ modulator, where $f_{Co} = 25\,\text{MHz}$ and $f_B = 4\,\text{MHz}$.



(a) **(b)**

Figure 6.6: The simulated NTF of the experimental $\Delta\Sigma$ modulator (Figure 6.3): **(a)** from 0 to $f_S/2$, and **(b)** over the signal band ($f_{Co}-f_B/2$ to $f_{Co}+f_B/2$). In this figure, ○ denotes results derived from behavioural simulations, and — denotes results derived from equations.



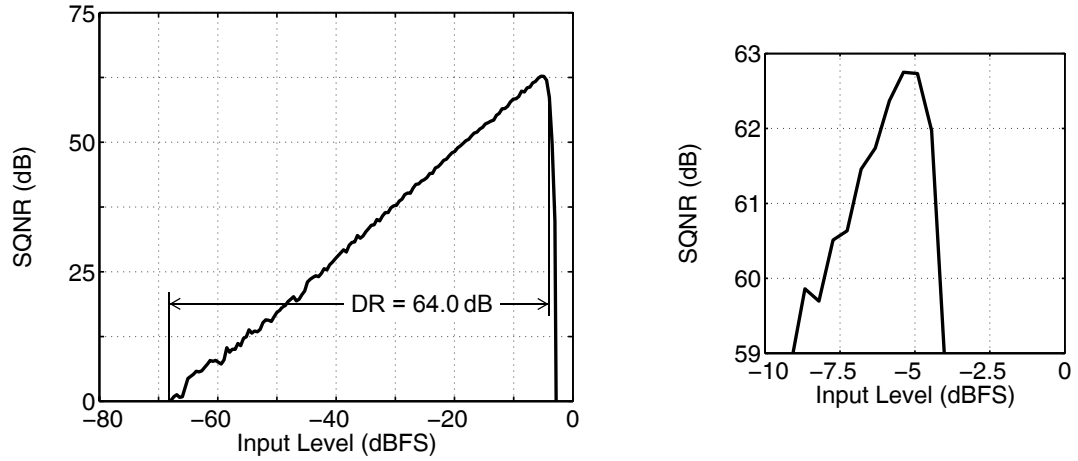
(a) **(b)**

Figure 6.7: The simulated STF of the experimental ΔΣ modulator (Figure 6.3): **(a)** from f_S to $3f_S$, **(b)** over the signal band ($f_{Ci}-f_B/2$ to $f_{Ci}+f_B/2$) and over the image band. Here, ○ denotes results derived from behavioural simulations, and — denotes results derived from equations.

Figure 6.7(a) compares the STF of the experimental ΔΣ modulator (Figure 6.3), derived from behavioural simulations, to the magnitude response of its prototype STF. This second plot was generated using the procedure described in Section 5.6. The deviation between these two plots is again caused by the limited attenuation of the high-frequency term. Figure 6.7(b) shows the signal and image bands of the experimental ΔΣ modulator, where $f_{Ci} = 225\,\text{MHz}$ and $f_B = 4\,\text{MHz}$. These plots demonstrate that the inherent image-reject filtering[4] is 22.0 dB at the centre frequency of the image band (175 MHz).

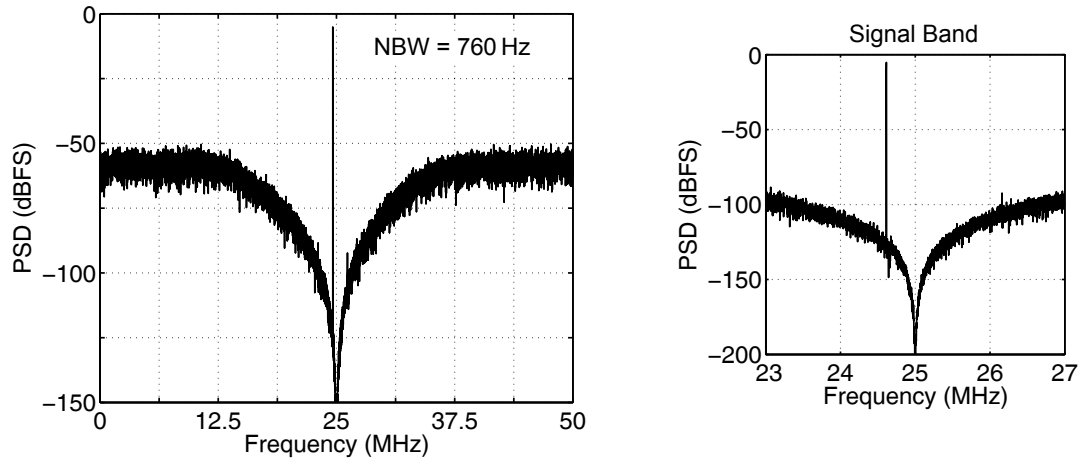
Figure 6.8 plots the simulated SQNR of the experimental ΔΣ modulator as a function of its input level for an input tone at $f_{in} = 224.6\,\text{MHz}$. It achieves a peak SQNR of 62.5 dB and a dynamic range of 64.0 dB over a signal bandwidth of $f_B = 4\,\text{MHz}$. Figure 6.9(a) plots the simulated output spectrum of the experimental ΔΣ modulator for a −5 dBFS input tone at $f_{in} = 224.6\,\text{MHz}$, which results in the peak SQNR. Figure 6.9(b) shows the signal band of the experimental ΔΣ modulator, where $f_{Co} = 25\,\text{MHz}$ and $f_B = 4\,\text{MHz}$

[4]The inherent image-reject filtering is evaluated using Equation (5.36) in Section 5.6.



(a) **(b)**

Figure 6.8: Simulated SQNR of the experimental $\Delta\Sigma$ modulator, as a function of its input level, for an input tone at 224.6 MHz.



(a) **(b)**

Figure 6.9: Simulated output spectrum of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone at 224.6 MHz: **(a)** from 0 to $f_S/2$, and **(b)** over the signal band ($f_{Co} - f_B/2$ to $f_{Co} + f_B/2$).

6.4 Performance Limitations

This section examines the effect of circuit noise, non-linear distortion, and clock jitter on the resolution of the experimental ΔΣ modulator (Figure 6.3). It extends the simulation results presented in Section 6.3, and provides additional performance metrics.

6.4.1 Circuit Noise

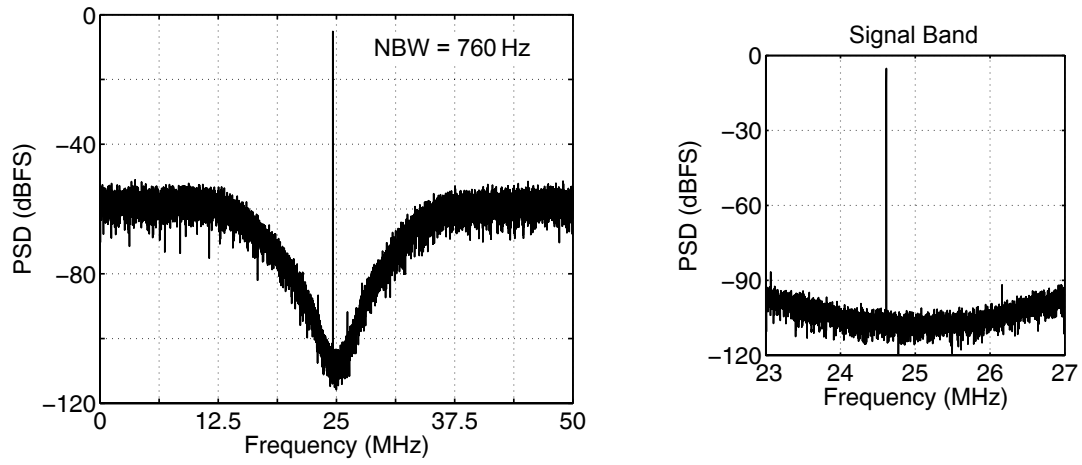
The primary sources of circuit noise in the experimental ΔΣ modulator (Figure 6.3) are the transconductor and output buffer of its LC resonator (RESON1), the resistors and amplifiers of its first active-RC resonator (RESON2), and the current sources of its outer-loop feedback DAC (DAC1).[5] The magnitude of each noise source is derived from circuit-level simulations, and is simulated here using standard behavioural models.

Figure 6.10(a) plots the simulated output spectrum of the experimental ΔΣ modulator, and includes the effect of the above mentioned noise sources. The spectrum in Figure 6.10 is generated using a −5 dBFS input tone, which results in the peak SNR. When circuit noise is incorporated into the behavioural simulations (Section 6.3), the experimental ΔΣ modulator achieves a peak SNR of 61.0 dB and a dynamic range of 62.0 dB over a signal bandwidth of $f_B = 4$ MHz. Therefore, circuit noise reduces the SNR of the experimental ΔΣ modulator by less than 2 dB from its nominal value (Section 6.3). Figure 6.10(b) shows the signal band of the experimental ΔΣ modulator.

6.4.2 Distortion

The primary sources of non-linear distortion in the experimental ΔΣ modulator (Figure 6.3) are the output buffer of its LC resonator (RESON1), and the amplifiers of its first active-RC resonator (RESON2). The distortion of these blocks is derived from circuit-level simulations, and is simulated here using standard behavioural models.

[5] The circuit noise introduced by the second active-RC resonator (RESON3), the quantizer, and the inner-loop feedback DACs (DAC2 – DAC4) is suppressed by the gain of preceding loop-filter stages, and does not have a significant effect on the resolution of the experimental ΔΣ modulator.

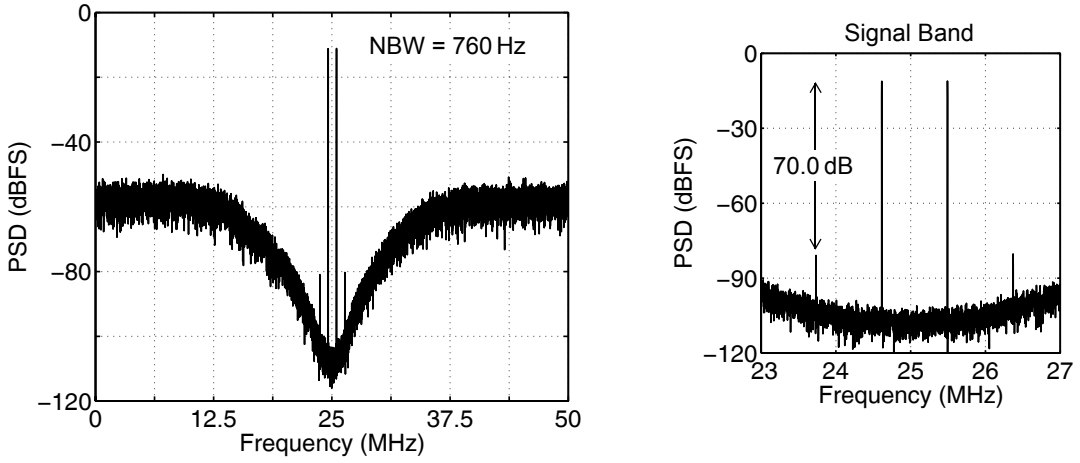


(a) **(b)**

Figure 6.10: Simulated output spectrum of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone at 224.6 MHz: **(a)** from 0 to $f_S/2$, and **(b)** over the signal band ($f_{Co}-f_B/2$ to $f_{Co}+f_B/2$). This plot demonstrates the effect of circuit noise, as compared to Figure 6.9.

Since the experimental $\Delta\Sigma$ modulator has a *bandpass* loop filter (Section 6.1), harmonic distortion products introduced by the above mentioned blocks appear at aliases of its signal band. As a result, they are attenuated by the STF of the continuous-time loop filter, and do not have a significant effect on the resolution of the experimental $\Delta\Sigma$ modulator. In general, the linearity of a bandpass ADC is evaluated using a two-tone input signal, which introduces intermodulation distortion products.

Figure 6.11(a) plots the simulated output spectrum of the experimental $\Delta\Sigma$ modulator, and includes the effect of non-linear distortion, described above, and circuit noise, described in Section 6.4.1. The spectrum in Figure 6.11 is generated using two -11 dBFS input tones that have a frequency separation of 880 kHz. When non-linear distortion is incorporated into the behavioural simulations (Section 6.4.1), the experimental $\Delta\Sigma$ modulator achieves a peak SNDR of 61.0 dB, and a third-order intermodulation distortion of -70.0 dBc. Figure 6.11(b) shows the signal band of the experimental $\Delta\Sigma$ modulator.



(a) **(b)**

Figure 6.11: Simulated output spectrum of the experimental ΔΣ modulator for two −11 dBFS tones separated by 880 kHz: **(a)** from 0 to $f_S/2$, and **(b)** over the signal band ($f_{Co} - f_B/2$ to $f_{Co} + f_B/2$). This plot demonstrates the effect of non-linear distortion, as compared to Figure 6.10.

6.4.3 Clock Jitter

The experimental ΔΣ modulator (Figure 6.3) is designed using a continuous-time loop filter, and is therefore sensitive to clock jitter. As described in Section 3.2.1, clock jitter introduces timing errors into both the forward and feedback paths of a continuous-time ΔΣ modulator. In the forward path, timing errors in the sampling instants are suppressed by the loop gain, and do not significantly affect the resolution. In the feedback path, timing errors in the pulses of the feedback DACs are added to the input signal of the ΔΣ modulator, and can reduce its resolution significantly.

This section extends the behavioural simulations presented in Section 6.4.2 to evaluate how the resolution of the experimental ΔΣ modulator (Figure 6.3) is affected by clock jitter introduced at its feedback DACs (DAC1–DAC4). Here, the effect of clock jitter is simulated using the Simulink behavioural model in Section 3.4.1, and it is considered to be significant when it reduces the SNDR of the experimental ΔΣ modulator by more than 3 dB from the nominal value (Section 6.4.2).

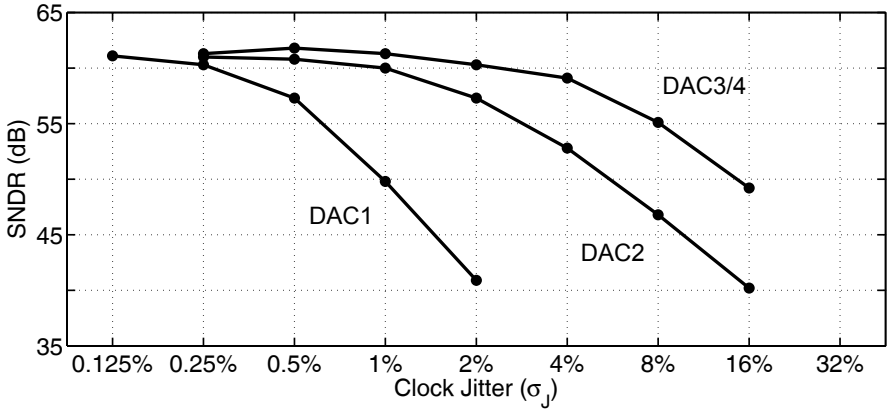


Figure 6.12: Simulated SNDR of the experimental $\Delta\Sigma$ modulator as a function of the clock jitter introduced at each of its feedback DACs (DAC1–DAC4).

Figure 6.12 plots the simulated SNDR of the experimental $\Delta\Sigma$ modulator as a function of the normalized clock jitter introduced at each of its feedback DACs (DAC1–DAC4). This figure demonstrates that the clock jitter introduced at DAC1 (σ_{J1}) has a significantly greater effect on the resolution of the experimental $\Delta\Sigma$ modulator than the clock jitter introduced at DAC2–DAC4. The loss of performance due to the clock jitter introduced at DAC1 becomes significant when $\sigma_{J1} > 0.25\,\%$.

6.5 Sensitivity Simulations for Design Centring

This section presents behavioural simulation results that are used to evaluate the sensitivity of the experimental $\Delta\Sigma$ modulator (Figure 6.3) to various circuit-level errors. Specifically, it analyses the effect of the finite quality factor and centre-frequency error of each resonator in the loop filter, the mismatch between the unit elements of the feedback DACs, and the phase errors in the LO signal. The presented simulation results are used to evaluate the magnitude of each error that leads to significant performance loss. These maximum errors are converted into design and tuning requirements for the associated circuits in Chapter 7. In this section, a circuit-level error is considered to be significant if it reduces the SNR of the experimental $\Delta\Sigma$ modulator by more than 3 dB from its nominal value (Section 6.3).

6.5.1 Resonator Quality Factor

The quality factor of a resonator determines its *selectivity*. A practical resonator has a finite quality factor (i.e., $Q < \infty$), which can reduce the in-band noise suppression of a bandpass ΔΣ modulator. In general, the loss of performance that results from a finite quality factor is significant when $Q < f_C/f_B$ [Sch06a]. Here, f_B is the signal bandwidth of the bandpass ΔΣ modulator and f_C is the centre frequency of the resonator.

This section uses behavioural simulations to evaluate how the noise-shaping performance of the experimental ΔΣ modulator (Figure 6.3) is affected by the finite quality factors of the resonators in its outer-loop and inner-loop filters.

Outer-Loop Filter

The outer-loop filter of the experimental ΔΣ modulator (Figure 6.3) is implemented using a conventional LC resonator (RESON1). The circuit-level implementation of the LC resonator is discussed in Section 7.1.

The quality factor of the LC resonator (RESON1) is set primarily by the series resistance of its inductors. The inductance and capacitance that are required to achieve a resonance at the input centre frequency of the experimental ΔΣ modulator ($f_{Ci} = 225\,\text{MHz}$) are too large for a practical on-chip implementation. Therefore, the capacitor is implemented on-chip and the inductors are placed off-chip (Section 7.1.2).

The *nominal* quality factor (Q_1) of the LC resonator (RESON1) is derived by simulating the selected off-chip inductors using available circuit-level models [Coi09]. These simulations demonstrated a nominal value of 25 for Q_1.

Figure 6.13(a) plots the simulated SQNR of the experimental ΔΣ modulator versus the quality factor (Q_1) of its LC resonator (RESON1). This figure demonstrates that the loss of performance due to the finite quality factor of the LC resonator is significant when $Q_1 < 25$. The quality factor of the LC resonator could be improved using a Q-enhancement technique, for example [Soo02], however this would increase the implementation complexity and require additional tuning circuitry.

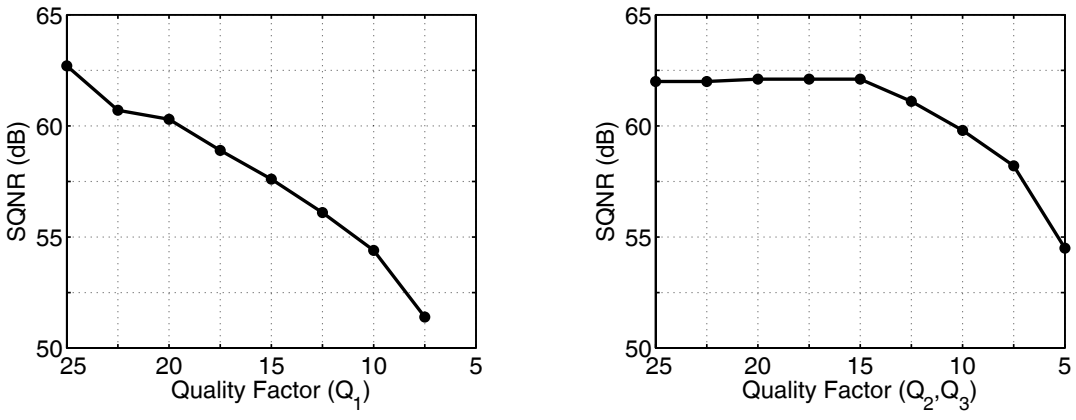


Figure 6.13: Simulated SQNR of the experimental $\Delta\Sigma$ modulator as a function of: **(a)** the quality factor (Q_1) of its LC resonator, and **(b)** the quality factors (Q_2, Q_3) of its active-RC resonators.

Inner-Loop Filter

The inner-loop filter of the experimental $\Delta\Sigma$ modulator (Figure 6.3) is implemented using a cascade of active-RC resonators (RESON2 and RESON3). The circuit-level implementation of the active-RC resonators is discussed in Section 7.2.

The quality factors of the active-RC resonators (RESON2 and RESON3) are set primarily by the finite gain-bandwidth of their amplifiers, and the series resistance of their integration capacitors (Section 7.2.1). Both of these parameters are subject to process-related variations that can cause significant errors in the quality factors of the active-RC resonators, as well as instability in their local feedback loops.

Figure 6.13(b) plots the simulated SQNR of the experimental $\Delta\Sigma$ modulator versus the quality factors (Q_2 and Q_3) of its active-RC resonators (RESON2 and RESON3). This figure demonstrates that the loss of performance due to the finite quality factors of the active-RC resonators is significant when Q_2, $Q_3 < 15$. The quality factors of the active-RC resonators are nominally set to 20. This is the maximum value, with additional margin, for which the local feedback loops of the resonators remain stable over every process corner.

6.5.2 Resonator Centre-Frequency Errors

The centre-frequency error of a resonator determines its *accuracy*. A practical resonator has a non-zero centre-frequency error (i.e., $\vartriangle f_C > 0$), which limits the in-band noise suppression in a bandpass ΔΣ modulator. In general, the loss of performance that results from a centre-frequency error is significant when $\vartriangle f_C$ is an appreciable fraction of the signal bandwidth f_B of the bandpass ΔΣ modulator [Sch06a].

This section uses behavioural simulations to evaluate how the noise-shaping performance of the experimental ΔΣ modulator (Figure 6.3) is affected by the centre-frequency errors of the resonators in its outer-loop and inner-loop filters.

Outer-Loop Filter

The outer-loop filter of the experimental ΔΣ modulator (Figure 6.3) is implemented using a conventional LC resonator (RESON1). The circuit-level implementation of the LC resonator is discussed in Section 7.1.

The centre frequency of the LC resonator (RESON1) is set by the values of its capacitor and inductors. Here, the capacitor is implemented on-chip, whereas the inductors are placed off-chip. The selected off-chip inductors have small tolerances (2 %), however the bond wires, package leads, and PCB traces associated with off-chip components all introduce additional parasitic inductances that can increase the overall error. The on-chip capacitor is subject to large process-related variations (25 %), and therefore also contributes significant error.

Figure 6.14(a) plots the simulated SQNR of the experimental ΔΣ modulator versus the centre-frequency error ($\vartriangle f_{C1}$) of its LC resonator (RESON1). This figure demonstrates that the loss of performance due to the centre-frequency error of the LC resonator is significant when $\vartriangle f_{C1} > 2\,\text{MHz}$. In order to correct for centre-frequency errors, the on-chip capacitor of the LC resonator is designed such that it is discretely tunable (Section 7.1.2). It provides a nominal tuning range of 30 MHz, with a maximum error of 1 MHz.

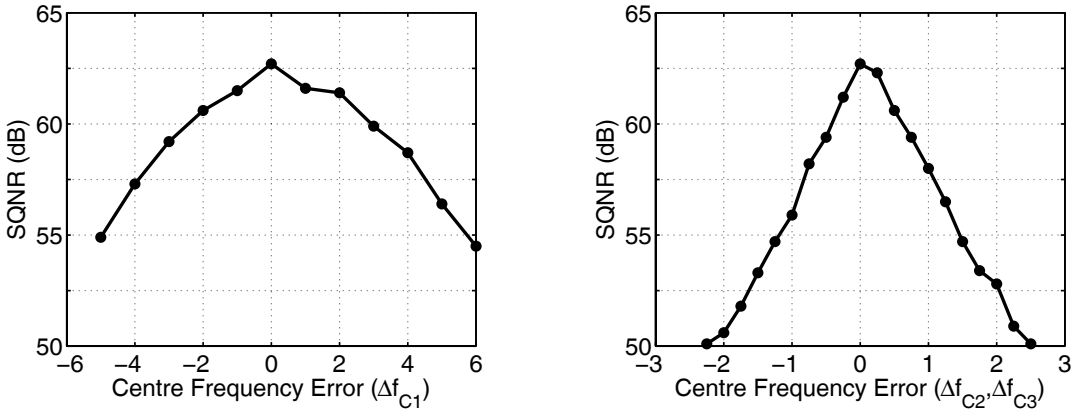


Figure 6.14: Simulated SQNR of the experimental $\Delta\Sigma$ modulator as a function of: **(a)** the centre-frequency error ($\Delta f_{\mathrm{C}1}$) of its LC resonator, and **(b)** the centre-frequency errors ($\Delta f_{\mathrm{C}2}$, $\Delta f_{\mathrm{C}3}$) of its active-RC resonators.

Inner-Loop Filter

The inner-loop filter of the experimental $\Delta\Sigma$ modulator (Figure 6.3) is implemented using a cascade of active-RC resonators (RESON2 and RESON3). The circuit-level implementation of the active-RC resonators is discussed in Section 7.2.

The centre frequencies of the active-RC resonators (RESON2 and RESON3) are set by the magnitudes of their capacitors and resistors, which are implemented on-chip. Both of these components are subject to large process-related variations (25 % for capacitors and 15 % for resistors), and can therefore introduce significant error.

Figure 6.14(b) plots the simulated SQNR of the experimental $\Delta\Sigma$ modulator versus the centre-frequency errors ($\Delta f_{\mathrm{C}2}$ and $\Delta f_{\mathrm{C}3}$) of its active-RC resonators (RESON2 and RESON3). This figure demonstrates that the loss of performance caused by the centre-frequency errors of the active-RC resonators is significant when $\Delta f_{\mathrm{C}2}$, $\Delta f_{\mathrm{C}3} > 500\,\mathrm{kHz}$. In order to correct for centre-frequency errors, the on-chip capacitors of the active-RC resonators are designed to be discretely tunable (Section 7.2.1). They provide a nominal tuning range of 20 MHz, with a maximum error of 500 kHz.

6.5.3 DAC Mismatch Errors

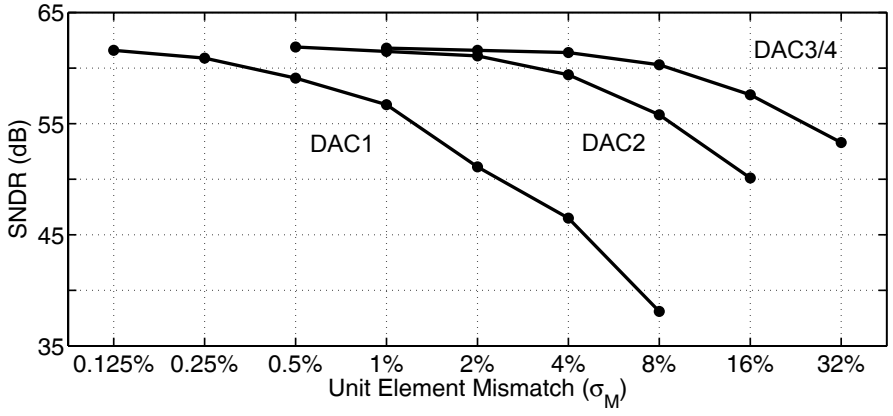
The feedback DACs of the experimental ΔΣ modulator (Figure 6.3) are implemented using two different multi-bit current-mode circuit topologies. The circuit-level implementations of the feedback DACs (DAC1–DAC4) are discussed in Section 7.4.

A multi-bit DAC is composed of an array of unit elements, which are nominally equal in value. The unit element of a current-mode DAC is implemented using a current source, and is therefore sensitive to transistor mismatch. The unit element mismatch (σ_{M}) of a multi-bit feedback DAC reduces the linearity of a ΔΣ modulator, and increases its in-band noise. The variable σ_{M} is used in this section to denote the normalized rms mismatch between the unit elements of a multi-bit DAC.

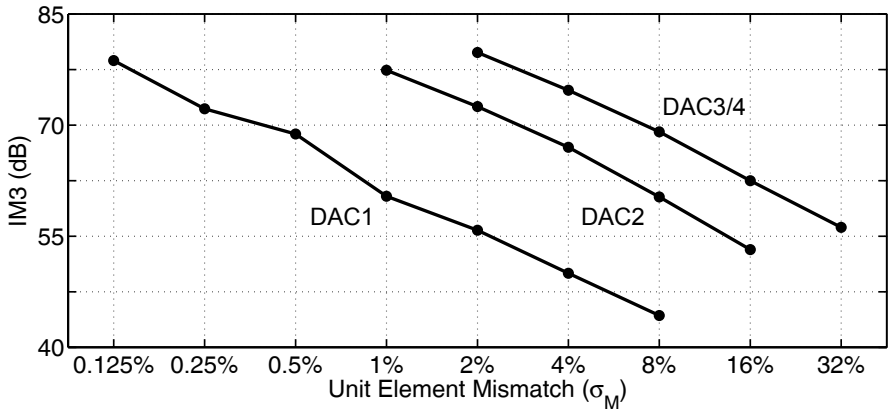
This section uses behavioural simulations to evaluate how the linearity and in-band noise of the experimental ΔΣ modulator (Figure 6.3) are affected by the unit element mismatch of its feedback DACs (DAC1–DAC4).

Figure 6.15(a) plots the simulated SNDR of the experimental ΔΣ modulator versus the unit element mismatch of its feedback DACs (DAC1–DAC4). This plot demonstrates that the mismatch of DAC1 (σ_{M1}) has a significantly greater effect on the SNDR of the experimental ΔΣ modulator than the mismatch of DAC2–DAC4. The loss of performance due to the unit element mismatch of DAC1 is significant when $\sigma_{\mathrm{M1}} > 0.5\,\%$.

Figure 6.15(b) plots the simulated IM3 of the experimental ΔΣ modulator versus the unit element mismatch of its feedback DACs (DAC1–DAC4). This plot demonstrates that the mismatch of DAC1 (σ_{M1}) has a significantly higher effect on the linearity of the experimental ΔΣ modulator than the mismatch of DAC2–DAC4. The loss of performance due to the unit element mismatch of DAC1 is significant when $\sigma_{\mathrm{M1}} > 0.25\,\%$. Here, the loss of performance is considered to be significant when the intermodulation products introduced by the mismatch of DAC1 are 3 dB lower than those introduced by the loop filter (Section 6.4.2).



(a)



(b)

Figure 6.15: (a) Simulated SNDR, and **(b)** simulated IM3 of the experimental $\Delta\Sigma$ modulator as a function of the unit element mismatch of its feedback DACs (DAC1–DAC4).

The unit element mismatch of the current-mode feedback DACs is reduced by increasing the area of their current-source transistors (Section 7.4.1). The noise and distortion that are introduced by the remaining mismatch errors are then suppressed using a bandpass mismatch shaping scheme (Section 7.4.3).

6.5.4 LO Phase Errors

As described in Section 6.1.2, the loop response of the experimental ΔΣ modulator includes scaling factors that are set by the phase difference between its LO signal and sampling clock: the low-frequency term is a function of $(\theta_U - \theta_D)$, and the high-frequency term is a function of $(\theta_U + \theta_D)$. By significantly attenuating the high-frequency term, the phase dependence of the loop response is reduced to that of the low-frequency term, $\theta_M \equiv (\theta_U - \theta_D)$.

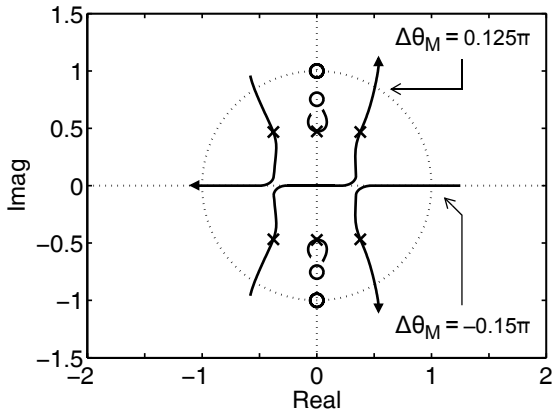
Figure 6.16(a) plots a root locus for the NTF of the experimental ΔΣ modulator, where the relative LO phase (θ_M) is varied from -0.25π to $+0.25\pi$ around its nominal value ($\pi/4$). This plot demonstrates that, for the selected out-of-band gain, the poles of the NTF remain inside the unit circle (i.e., $|z| = 1$) and, correspondingly, the NTF remains stable when the LO phase error ($\Delta\theta_M$) is between -0.15π and $+0.125\pi$.

Figure 6.16(b) plots the simulated SQNR of the experimental ΔΣ modulator versus the error ($\Delta\theta_M$) in its relative LO phase. This figure demonstrates that the loss of performance due to LO phase errors is significant when $\Delta\theta_M > 0.1\pi$ or $\Delta\theta_M < -0.1\pi$. In order to correct for phase errors, the delay in Figure 6.3 is designed with 2-bit tuning control. It provides a nominal tuning range of 0.2π, with a maximum error of 0.025π.

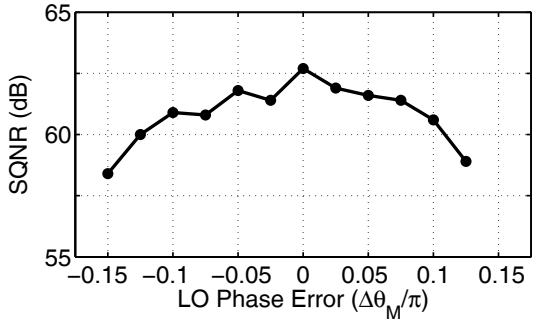
6.6 Conclusion

This chapter presented the system architecture of an experimental frequency-translating ΔΣ modulator. This experimental ΔΣ modulator was utilized to verify the accuracy of the NTF synthesis procedure proposed in Section 5.2, and to validate the design techniques proposed in Sections 5.3, 5.4, and 5.5. It is designed to convert a wideband (4 MHz) input signal that is centred at a high IF (225 MHz), while providing moderate (10 bit) resolution.

Section 6.1 presented the architecture of the experimental ΔΣ modulator, and specified its frequency and phase parameters. The experimental architecture is depicted in Figure 6.3, and its parameters are specified in Tables 6.1 and 6.2. Section 6.2 presented the synthesis of the experimental ΔΣ modulator from a prototype NTF. Table 6.3 summarizes the properties of the prototype NTF, and Table 6.4 specifies the associated loop-filter coefficients.



(a)



(b)

Figure 6.16: (a) Root locus plot for the NTF of the experimental $\Delta\Sigma$ modulator, where the relative LO phase is varied from -0.25π to $+0.25\pi$ around its nominal value ($\pi/4$). **(b)** Simulated SQNR of the experimental $\Delta\Sigma$ modulator as a function of the error ($\Delta\theta_{\mathrm{M}}$) in its relative LO phase.

This chapter also evaluated the nominal performance of the experimental $\Delta\Sigma$ modulator and its sensitivity to circuit-level non-idealities using behavioural (system-level) simulations. The experimental $\Delta\Sigma$ modulator achieves a peak SQNR of 62.5 dB over a signal bandwidth of 4 MHz. Figures 6.6 and 6.7 demonstrate the accuracy of the simulated NTF and STF, and validate the synthesis procedure and design techniques proposed in Chapter 5. When circuit noise and non-linear distortion are included in behavioural simulations, the experimental $\Delta\Sigma$ modulator achieves a peak SNDR of 61.0 dB, and an associated IM3 of -70.0 dB.

Chapter 7

Circuit Implementation *of the* Experimental $\Delta\Sigma$ Modulator

This chapter presents a circuit-level implementation for the experimental single-path frequency-translating $\Delta\Sigma$ modulator that was proposed in Section 6.1. The prototype architecture is implemented in a 1-V 65-nm CMOS process, and has been fabricated without any special process options. The measured performance of the experimental $\Delta\Sigma$ modulator is presented in Sections 8.3 and 8.4.

Figure 7.1 shows a circuit diagram for the experimental $\Delta\Sigma$ modulator, and is equivalent to the system diagram in Figure 6.3. This chapter is divided into four sections, each of which discusses one of the main functional blocks of the experimental $\Delta\Sigma$ modulator. Section 7.1 presents the circuit implementation of the LC resonator (RESON1), which is composed of a transconductor, an LC tank, and a voltage buffer. Section 7.2 presents the implementation of the active-RC resonators (RESON2 and RESON3), and discusses the operational amplifiers and the switching mixer. Sections 7.3 and 7.4 present the implementations of the flash ADC, the feedback DACs (DAC1 – DAC4), and the mismatch-shaping logic.

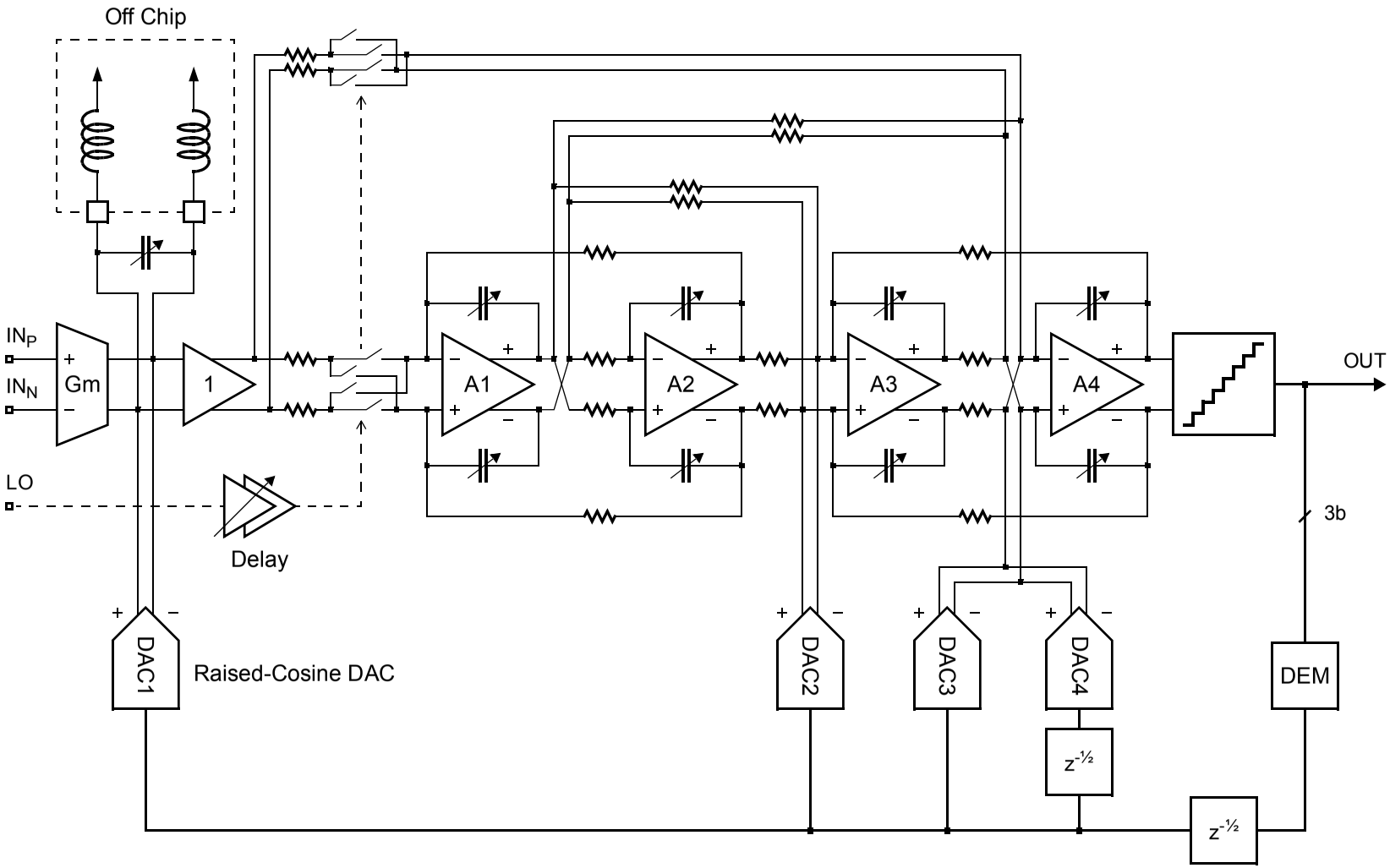


Figure 7.1: Circuit diagram of the experimental $\Delta\Sigma$ modulator. The capacitors and the delay block depicted in this diagram are tuned using manual off-chip control.

7.1 LC Resonator

This section presents the circuit-level design of the LC resonator, which is used to implement the outer-loop filter of the experimental $\Delta\Sigma$ modulator (Section 6.1). Figure 7.2 provides a circuit schematic for the LC resonator, which is composed of a transconductor, an LC tank, and a source follower.

7.1.1 Transconductor

The transconductor converts the differential input voltage of the experimental $\Delta\Sigma$ modulator into a corresponding current. Since it operates directly on the input signal, the transconductor has the same noise and linearity requirements as the overall $\Delta\Sigma$ modulator.

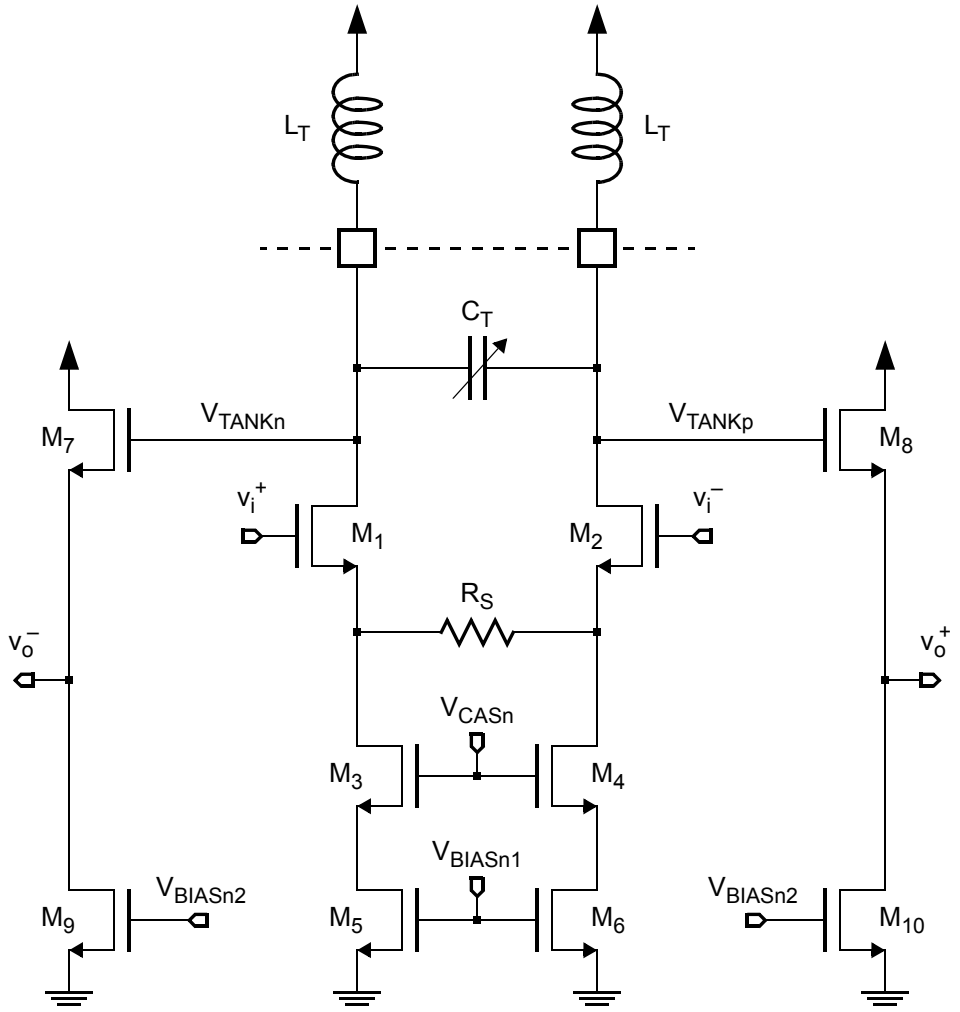
The input voltage-to-current conversion of the transconductor is achieved using an nMOS differential pair (M_1–M_2) that is linearized with a fixed source-degeneration resistor (R_S). Its tail current source is split (M_5–M_6), with R_S connected differentially, to reduce the required common-mode input voltage, and is further cascoded (M_3–M_4) to improve the common-mode rejection. Transistors M_5–M_6 are biased at the edge of saturation using a wide-swing cascode current mirror, which further reduces the common-mode input voltage [Joh97].

The transconductance of this circuit topology can be derived as

$$G_{m,\,\mathrm{in}} \;=\; \frac{i_o}{v_i^+ - v_i^-} \;=\; \frac{1}{2\,r_{s1,2} + (R_\mathrm{S} \parallel 2\,r_{d3,4})} \tag{7.1}$$

where $r_{s1,2}$ is the small-signal source resistance of M_1–M_2 and $r_{d3,4}$ is the resistance looking into the drains of M_3–M_4.

The required transconductance ($G_{m,\,\mathrm{in}}$) is set by the full-scale current of DAC1 ($i_{\,\mathrm{DAC1}}$), and by the input coefficient of the loop filter (a_in). The value of $i_{\,\mathrm{DAC1}}$ is selected according to the matching and thermal-noise requirements of DAC1, as described in Section 7.4.1. The value of a_in is selected so that it maximizes the input voltage swing of the experimental $\Delta\Sigma$ modulator, which reduces the required value of $G_{m,\,\mathrm{in}}$ and, therefore, the power consumption of the transconductor. The maximum input voltage ($v_{id,\,\mathrm{max}}$) is limited by the linearity of the input voltage-to-current conversion.



Device	M_1–M_2	M_3–M_4	M_5–M_6	M_7–M_8	M_9–M_{10}
W(μm)/L(μm)	32/0.12	32/0.12	32/0.12	7.5/0.12	7.5/0.12

Component	R_S	$C_{\mathrm{T,\,nom}}$	L_T
Value	575 Ω	5.8 pF	33 nH

Figure 7.2: Circuit diagram of the LC resonator.

Linearity

The linearity of the input voltage-to-current conversion is determined by the distortion of the input transistors (M_1–M_2) and that of the cascode transistors (M_3–M_4), as follows:

1. The distortion of M_1–M_2 dominates when the tail current (I_{tail}) of the transconductor is low. The small-signal source resistances (r_{s1} and r_{s2}) of M_1–M_2 appear in series with the fixed source resistor (R_{S}), as shown in Equation (7.1). Therefore, their effect on the input voltage-to-current conversion increases as their magnitude increases. The value of $r_{s1,2}$ scales inversely with I_{tail}, and therefore increases as I_{tail} is decreased.

2. The distortion of M_3–M_4 dominates when the tail current (I_{tail}) of the transconductor is high. The sum of the drain resistances ($r_{d3} + r_{d4}$) of M_3–M_4 appears in parallel with the fixed source resistor (R_{S}), as shown in Equation (7.1). Therefore, their effect on the input voltage-to-current conversion increases as their magnitude decreases. The value of $r_{d3,4}$ scales inversely with I_{tail}, and therefore decreases as I_{tail} is increased.

Since the distortion of M_3–M_4 is dominant when I_{tail} is high, and the distortion of M_1–M_2 is dominant when I_{tail} is low, there is an optimal tail current (I_{tail}), for each R_{S}, that maximizes the linear input range of the transconductor. The maximum input voltage ($v_{id,\,\max}$) remains approximately constant with R_{S}.

The transconductor is nominally designed for $G_{m,\,\text{in}} = 1.35\,\text{mA/V}$ with a source resistance of $R_{\text{S}} = 575\,\Omega$ and a tail current of $I_{\text{tail}} = 2 \times 800\,\mu\text{A}$. In simulation, the transconductor has a linear input range of approximately $\pm\,200\,\text{mV}$.

Noise

The transconductor operates on the signal band of the experimental $\Delta\Sigma$ modulator when it is centred at $f_{Ci} = 225\,\text{MHz}$. As a result, the in-band noise performance of the transconductor is dominated by the thermal noise of its source resistor and transistors. The flicker ($1/f$) noise of the transistors is negligible at 225 MHz, and is not considered here.

Figure 7.3 illustrates the sources of thermal noise[1] in the transconductor. Since the input transistors (M_1–M_2) are biased in their active region, their thermal noise contribution can be represented using an equivalent voltage source connected in series with their gate. The power spectral density of this noise voltage is white, and is approximated [Joh97] as

$$V^2_{n,\,M_{1,2}}(f) \;=\; 4kT\gamma_T \frac{1}{g_{m1,2}} \qquad (\mathrm{V}^2/\mathrm{Hz}) \tag{7.2}$$

The thermal noise contribution of the bias transistors (M_5–M_6) can be similarly represented using a current source[2] connected in parallel with their source and drain. The power spectral density of this noise current is white, and is approximated as

$$I^2_{n,\,M_{5,6}}(f) \;=\; 4kT\gamma_T g_{m5,6} \qquad (\mathrm{A}^2/\mathrm{Hz}) \tag{7.3}$$

The thermal noise contribution of the source resistor (R_S) can be represented using a voltage source connected in series with R_S. The power spectral density of this noise voltage is white, and is approximated as

$$V^2_{n,\,R_\mathrm{S}}(f) \;=\; 4kTR_\mathrm{S} \qquad (\mathrm{V}^2/\mathrm{Hz}) \tag{7.4}$$

In these equations, $k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant, T is the temperature in degrees Kelvin, and γ_T is the excess thermal-noise factor.

The noise voltages of the input transistors (M_1–M_2) and the source resistor (R_S) appear directly between the input terminals of the transconductor, and can be referred to the input without modification. The noise currents of the bias transistors (M_5–M_6) are referred to the input by first evaluating their contribution to the output current of the transconductor, and then dividing by $G_{m,\,\mathrm{in}}$ [San00].

---

[1] The noise contribution of the cascode transistors (M_3–M_4) is degenerated by the output resistance of the bias transistors (M_5–M_6), and can therefore be neglected.

[2] A current-domain representation is used here so that the noise contribution of M_5–M_6 can be easily referred to the input of the transconductor.

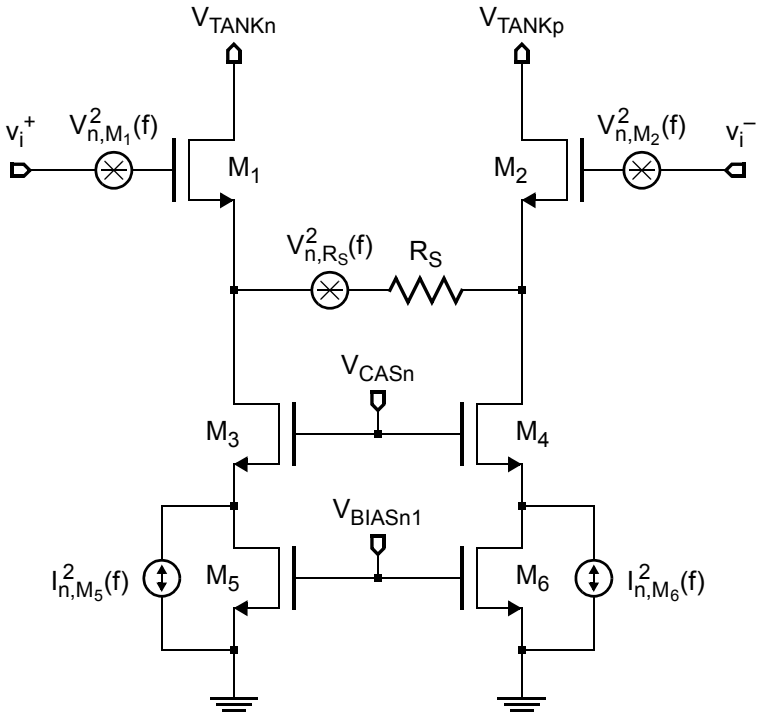


Figure 7.3: Sources of thermal noise in the transconductor.

The total input-referred thermal noise of the transconductor can be expressed as

$$V^2_{n,\,\mathrm{in}}(f) \;=\; 2\,V^2_{n,\,M_{1,2}}(f) + V^2_{n,\,R_\mathrm{S}}(f) + 2\left(\frac{R_\mathrm{S}}{2}\right)^2 I^2_{n,\,M_{5,6}}(f) \qquad (\mathrm{V^2/Hz}) \qquad (7.5)$$

The source resistance (R_S) must be greater than the small-signal source resistances ($1/g_{m1,2}$) of M_1–M_2 for the transconductor to achieve adequate linearity. As a result, the in-band noise performance is dominated by the contributions of R_S and the bias transistors (M_5–M_6).

In simulation, the transconductor achieves an input-referred rms thermal noise density of $7.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ around $f_{Ci} = 225\,\mathrm{MHz}$. Since the experimental $\Delta\Sigma$ modulator is designed with a continuous-time loop filter (Section 6.1), its resolution is only affected by the thermal noise within its signal band.

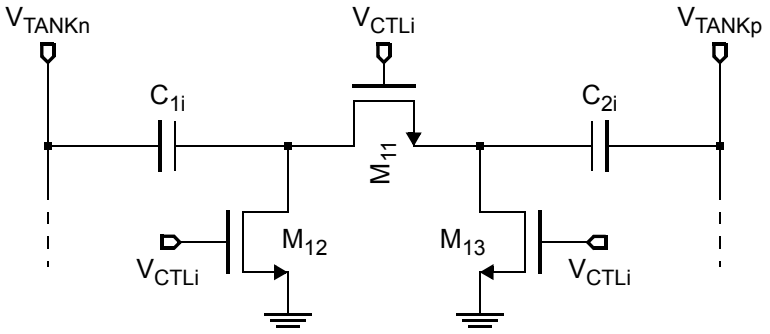
7.1.2 LC Tank

The LC tank must implement a resonance at the input centre frequency of the experimental ΔΣ modulator ($f_{Ci} = 225\,\text{MHz}$). Since the associated capacitance and inductance require too much layout area for a practical on-chip implementation, the inductor is placed off-chip, and the capacitor is placed on-chip. The on-chip capacitor is implemented using an interdigitated metal-oxide-metal (MOM) fringe capacitor. It is subject to process-related variations as high as $\pm 25\,\%$ in the selected 65-nm technology, and is therefore designed such that it is discretely tunable. The implemented tuning array is also required to correct for the additional parasitic inductances that are introduced when the inductors are placed off-chip.

The values of the off-chip inductors (L_T) are maximized in order to minimize the relative contribution of the parasitics that are introduced by the PCB traces, the package leads, and the bond wires. The maximum value of L_T is limited by the self-resonant frequency (SRF) of available discrete inductors. The SRF should be at least a decade higher than the required resonance frequency in order to ensure that the inductors have a flat impedance characteristic over the frequency range of interest [Coi08]. These considerations resulted in the selection of two 33 nH (L_T) inductors, which have a SRF of 2.7 GHz.

The on-chip capacitor (C_T) is composed of a base component and a 4-bit binary-weighted tuning array. In order to reduce the area of the on-chip capacitor, the array is only designed to cover half of the required tuning range. It can correct for small-to-large positive variations in the capacitance, and small negative variations. The tuning array is not required to correct for large negative variations, since these can be corrected using off-chip capacitors. The base capacitor is designed with a nominal value of 4.8 pF, which provides the required capacitance, including additional margin, for the maximum positive process variation. The tuning array is designed with binary-weighted values ranging from 100 fF to 800 fF. It provides a nominal tuning range of 30 MHz, with a maximum error of 1 MHz.

Figure 7.4 shows a circuit diagram for one element of the tuning array. Here, the control switches are designed using a three-transistor configuration that maximizes both the linearity and the quality factor of the LC tank for a given tuning code. When an element of the tuning



Device	M_{11}	M_{12}–M_{13}
W(μm)/L(μm)	6–36/0.06	0.2/0.06

Figure 7.4: Circuit diagram for one element of the tuning array that is used by the LC tank.

array is active, transistor M_{11} provides a low-resistance path between capacitors C_1 and C_2, while minimum-sized devices M_{12} and M_{13} provide the bias voltages at its source and drain. Use of a single wide-channel device (M_{11}) minimizes the series resistance that is connected to the LC tank when an element of the tuning array is active, which maximizes the achievable quality factor. In addition, it minimizes the non-linear parasitic capacitance that is connected to the LC tank when an element is not active, which maximizes the achievable linearity. The gate capacitance of transistor M_{11} is significantly lower than C_1 and C_2, and does not reduce the accuracy of the tuning array.

7.1.3 Source Follower

A conventional source follower (M_7–M_{10}) is used at the output of the LC resonator, as shown in Figure 7.2. This follower is required to isolate the LC tank from the input resistors of the active-RC resonators, which would otherwise reduce the quality factor. It is also required to shift the common-mode level from 1 V at the LC tank to 450 mV at the switching mixer and the active-RC resonators (Section 7.2).

Noise

The source follower operates on the signal band of the experimental ΔΣ modulator when it is centred at $f_{Ci} = 225\,\text{MHz}$. As a result, the in-band noise performance of the source follower is dominated by the thermal noise of its transistors. The flicker $(1/f)$ noise of the transistors is negligible at 225 MHz, and is not considered.

The source follower is biased with a tail current of $I_{\text{tail}} = 2 \times 300\,\mu\text{A}$. In simulation, this bias results in an rms thermal noise density of $9.5\,\text{nV}/\sqrt{\text{Hz}}$ at $f_{Ci} = 225\,\text{MHz}$.

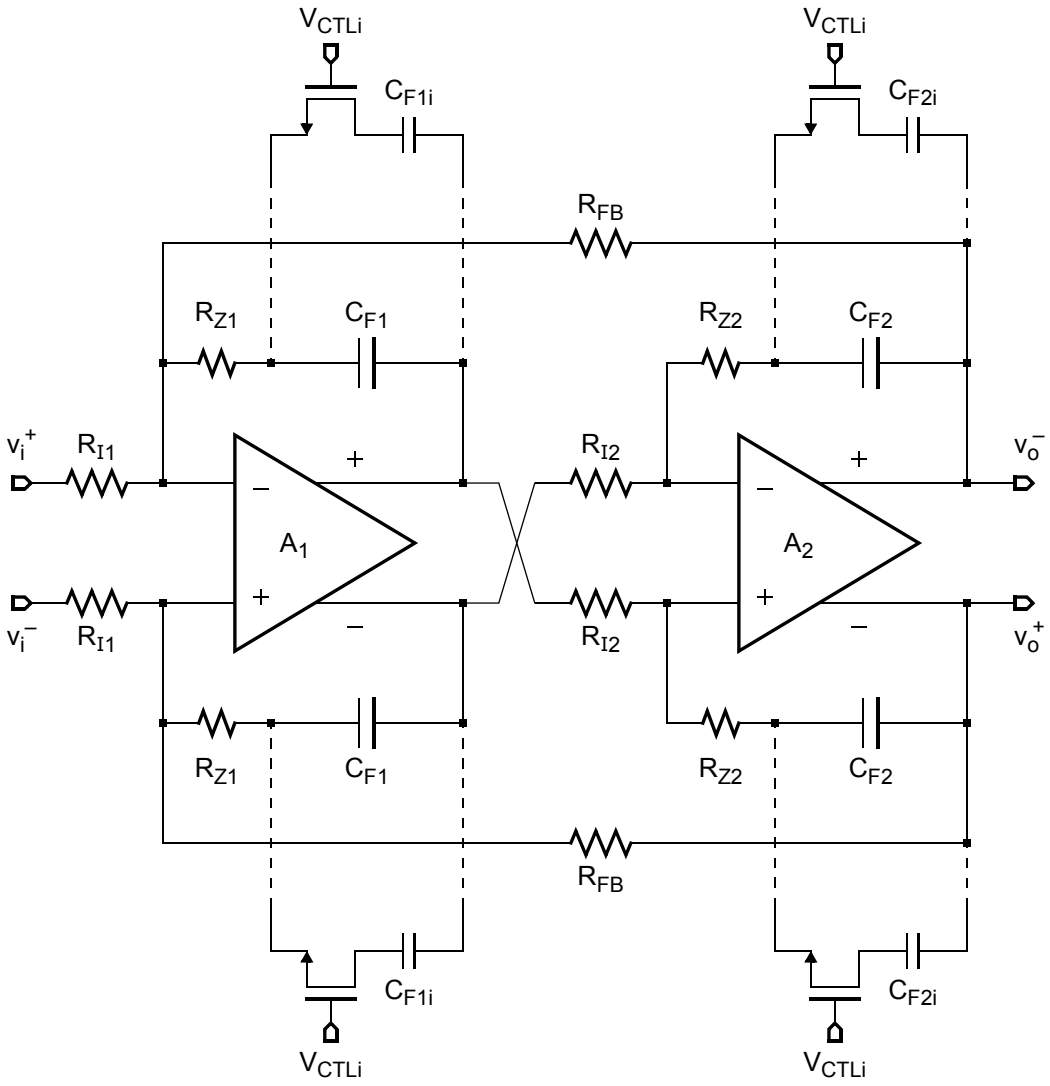
7.2 Active-RC Resonators

This section describes the circuit-level design of the active-RC resonators that are used to implement the inner-loop filter of the experimental ΔΣ modulator (Section 6.1).

7.2.1 Resonator

Figure 7.5 shows a general circuit diagram for an active-RC resonator. It is composed of two active-RC integrators connected in negative feedback, where each integrator is implemented using an operational amplifier, a feedback capacitor and an input resistor. The input voltage of an active-RC integrator is converted into a current over the resistor, which is connected to the virtual ground of the amplifier. This current is then integrated on the feedback capacitor, which generates a corresponding output voltage.

The centre frequency of an active-RC resonator is determined by the product of its input resistance and feedback capacitance. A centre frequency of $f_{Co} = 25\,\text{MHz}$ is achieved here by using a nominal resistance of $4\,\text{k}\Omega$ and a nominal capacitance of 1.5 pF. Both components are implemented on-chip, and tuning is required to correct for process variations.



RESON2

Component	R_{I1}	R_{I2}	C_{F1}–C_{F2}	R_{Z1}–R_{Z2}	R_{FB}
Value	5.5 kΩ	4 kΩ	950 fF	250 Ω	4 kΩ

RESON3

Component	R_{I1}	R_{I2}	C_{F1}–C_{F2}	R_{Z1}–R_{Z2}	R_{FB}
Value	3.75 kΩ	2 kΩ	775 fF	250 Ω	8 kΩ

Figure 7.5: Circuit diagram of the active-RC resonator.

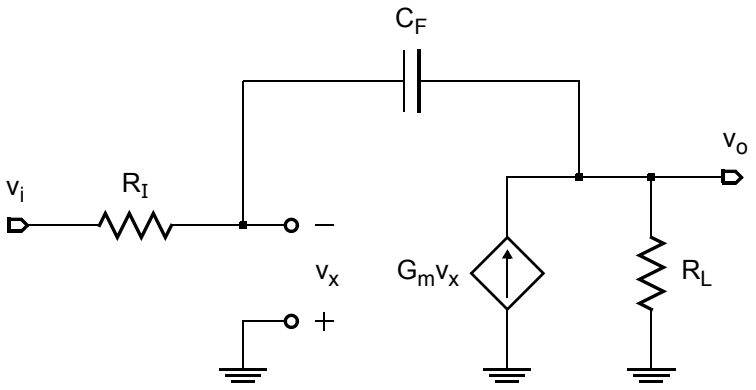


Figure 7.6: Circuit diagram of a standard active-RC integrator.

Finite Amplifier Gain

Figure 7.6 shows a circuit diagram for a standard active-RC integrator, where the amplifier is modeled as a voltage-controlled current source with a finite transconductance (G_m), and an infinite bandwidth ($\omega_{3\mathrm{dB}} = \infty$). Here, R_L is used to represent the resistive loading of the next stage. The transfer function of this integrator can be approximated as

$$I_1(s) \;=\; \frac{v_o(s)}{v_i(s)} \;\cong\; -\frac{A_v(1 - s/\omega_{z1})}{1 + s/\omega_{p1}} \tag{7.6}$$

$$\omega_{p1} \;=\; \omega_\mathrm{T}/A_v$$

$$\omega_{z1} \;=\; G_m/C_\mathrm{F}$$

where $A_v = G_m R_\mathrm{L}$ is the equivalent voltage gain of the amplifier, and $\omega_\mathrm{T} = 1/(R_\mathrm{I} C_\mathrm{F})$ is the ideal unity-gain frequency of the integrator ($A_v \to \infty$). Note that Equation (7.6) is simplified by assuming that $A_v \gg 1$.

The right-half-plane zero (ω_{z1}) in Equation (7.6) is the result of the forward signal path through the feedback capacitor of the integrator. This zero introduces a negative phase shift into the response of the integrator that can lead to instability when two integrators are placed in feedback to implement a resonator. In general, this negative phase shift is compensated by adding a small resistor (R_{Z}) in series with the feedback capacitor [Lin00]. This resistor shifts the right-half-plane zero to $\omega'_{z1} = \omega_{z1}/(1 - G_m R_{\mathrm{Z}})$, and can be selected such that $G_m R_{\mathrm{Z}} = 1$, which results in $\omega'_{z1} = \infty$.

Finite Amplifier Gain-Bandwidth

If the amplifier in Figure 7.6 is instead modeled as a voltage-controlled current source with a finite transconductance (G_m) and a finite bandwidth ($\omega_{3\mathrm{dB}}$), the integrator transfer function can be approximated as

$$I_2(s) \;=\; \frac{v_o(s)}{v_i(s)} \;\cong\; -\frac{A_v(1 - s/\omega_{z1})(1 + s/\omega_{z2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \tag{7.7}$$

$$\begin{aligned} \omega_{p1} &= \omega_{\mathrm{T}}/A_v \\ \omega_{p2} &= A_v\,\omega_{3\mathrm{dB}}/2 \end{aligned}$$

where the derived expression is simplified by assuming that real poles ω_{p1} and ω_{p2} are widely separated [Joh97], and that $A_v\,\omega_{3\mathrm{dB}} \gg \omega_{\mathrm{T}}$.

The non-dominant pole (ω_{p2}) in Equation (7.7) is caused by the finite gain-bandwidth of the amplifier. This pole introduces a negative phase shift that causes the total phase shift of the integrator to be greater than 90° at its unity-gain frequency (ω_{T}). When two integrators are connected in feedback, these additional poles cause the phase shift in the local feedback loop of the corresponding resonator to be greater than 180° at its unity-gain frequency. This results in positive feedback, which causes the local feedback loops to oscillate.

The negative phase shift that is introduced by the finite gain-bandwidth of the amplifier can be compensated by inserting a small resistor (R_Z) in series with its feedback capacitor, as described previously. This resistor decreases the frequency of the left-half-plane zero (ω_{z2}) in Equation (7.7), which reduces the phase shift of the integrator at its unity-gain frequency. In this way, it compensates for the finite gain-bandwidth of the amplifier, and is used both to stabilize the local feedback loop of an associated resonator and to set its quality factor.

Quality Factor

The quality factor (Q) of a resonator depends on the phase margin of its loop response. The value of Q can be maximized by increasing the phase shift inside the local feedback loop of a resonator so that its phase margin is as close as possible to zero, without becoming negative. As described previously, the phase shift of an active-RC integrator is adjusted by inserting a small resistor (R_Z) in series with its feedback capacitor. Accordingly, the quality factor of an active-RC resonator can be adjusted by changing the series resistance (R_Z) that is used by its composite integrators [Sch06a].

In the experimental ΔΣ modulator, the active-RC resonators (RESON2 and RESON3) are both designed with a series resistance of $R_Z = 250\,\Omega$. This is the minimum series resistance for which their local feedback loops do not oscillate over any process corner. In simulation, this value of R_Z results in a quality factor of 20 for both resonators.

Tuning

The active-RC resonators (RESON2 and RESON3) are implemented using on-chip capacitors and resistors, which are sensitive to process variations. In the selected 65-nm CMOS process, the absolute capacitor variation[3] is $\pm 25\,\%$, whereas the absolute resistor variation is $\pm 15\,\%$. Therefore, tuning is required to set the centre frequency of each resonator.

[3]The specified tolerances are for fringe capacitors and N+ polysilicon resistors.

The centre frequencies of the active-RC resonators (RESON2 and RESON3) are tuned by switching the feedback capacitance of their composite integrators. Each feedback capacitor is composed of a base component and a 5-bit binary-weighted tuning array. The base component of RESON2 is designed with a nominal value of 950 fF and the base component of RESON3 is designed with a nominal value of 775 fF. These components are selected so that they provide the required time constant under the maximum positive process variation. The tuning arrays are designed with binary-weighted capacitor values ranging from 50 fF to 800 fF. They have a nominal tuning range of 20 MHz, with a maximum error of 500 kHz.

In the selected 65-nm CMOS process, the capacitors and resistors provide better than 1 % matching for the required component values. Accordingly, the same tuning code is applied to both active-RC resonators, using RESON2 as a reference. The centre frequency of RESON2 is tuned by disconnecting its inputs, using the switches of the mixer, and connecting a positive feedback path in order to reconfigure it as an oscillator.

Noise

The in-band noise performance of an active-RC resonator is determined by the thermal noise of its resistors and the noise of its operational amplifiers. The noise of both integrators must be considered since, by definition, the voltage gain of the first integrator is unity at the centre frequency of the resonator (f_{Co}).

Figure 7.7 illustrates the sources of noise[4] in an active-RC resonator. The thermal noise contributions of the input resistors (R_{I1} and R_{I2}) and the local feedback resistors (R_{FB}) can be represented using equivalent voltage sources connected in series with R_{I1}, R_{I2}, and R_{FB}, as described in Section 7.1.1. The power spectral density of each noise voltage is white, and is approximated in the same way as Equation (7.4). The noise contributions of the operational amplifiers (A_1 and A_2) can be represented using equivalent voltage sources connected in series with their non-inverting input terminals.

[4]The series resistors (R_{Z}) also introduce thermal noise, however their contribution is relatively small and has been excluded to simplify Equation (7.8).

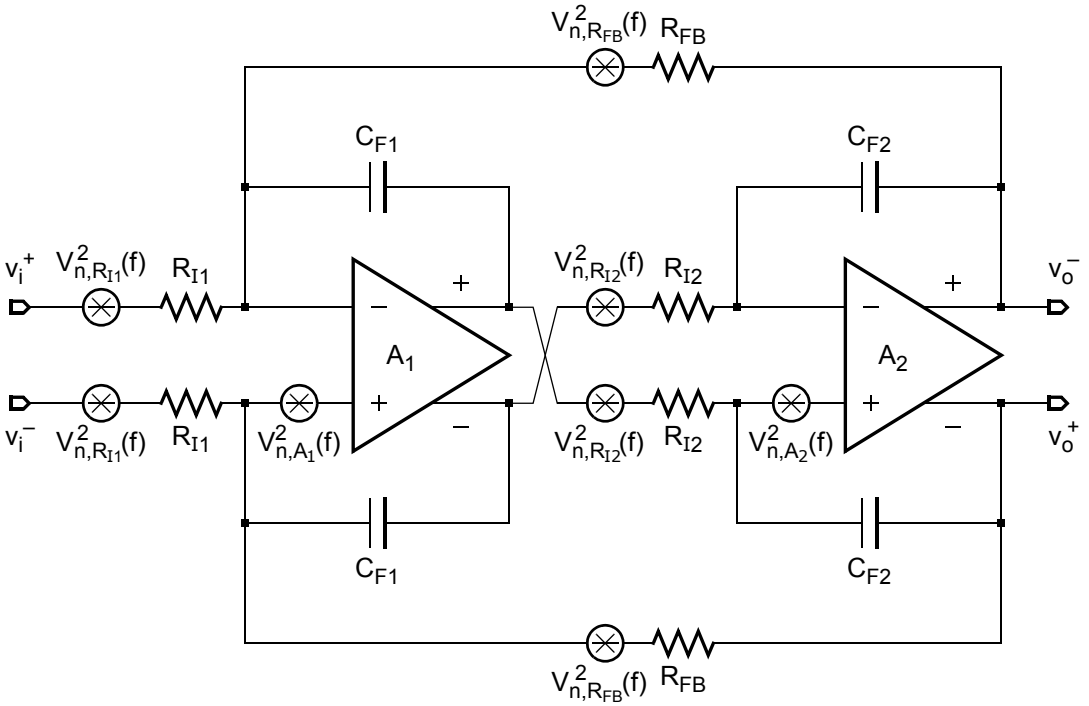


Figure 7.7: Sources of thermal noise in the active-RC resonators.

The total input-referred noise of the active-RC resonator can be expressed as

$$V^2_{n,\,\mathrm{in}}(f) \;=\; 2\,V^2_{n,\,R_{\mathrm{I1}}}(f) + 2\left(\frac{R_{\mathrm{I1}}}{R_{\mathrm{FB}}}\right)^2 V^2_{n,\,R_{\mathrm{FB}}}(f) + \left(1+\frac{R_{\mathrm{I1}}}{R_{\mathrm{FB}}}+\frac{R_{\mathrm{I1}}}{Z_{\mathrm{F}}}\right)^2 V^2_{n,\,A_1}(f) \qquad (7.8)$$

$$+\,2\left(\frac{R_{\mathrm{I1}}}{Z_{\mathrm{F}}}\right)^2 V^2_{n,\,R_{\mathrm{I2}}}(f) + \left(\frac{R_{\mathrm{I1}}}{Z_{\mathrm{F}}}+\frac{R_{\mathrm{I1}}R_{\mathrm{I2}}}{Z^2_{\mathrm{F}}}\right)^2 V^2_{n,\,A_2}(f) \qquad (\mathrm{V}^2/\mathrm{Hz})$$

where Z_{F} represents the impedance of the feedback capacitor. This expression is simplified by assuming that the operational amplifiers have infinite gain-bandwidth [Ort06].

The in-band noise of the first active-RC resonator (RESON2) has a more significant effect on the performance of the experimental ΔΣ modulator than that of RESON3, since the latter is largely suppressed by the loop gain. In simulation, RESON2 achieves an input-referred rms thermal noise density of $26.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $f_{Co} = 25\,\mathrm{MHz}$.

7.2.2 Operational Amplifier

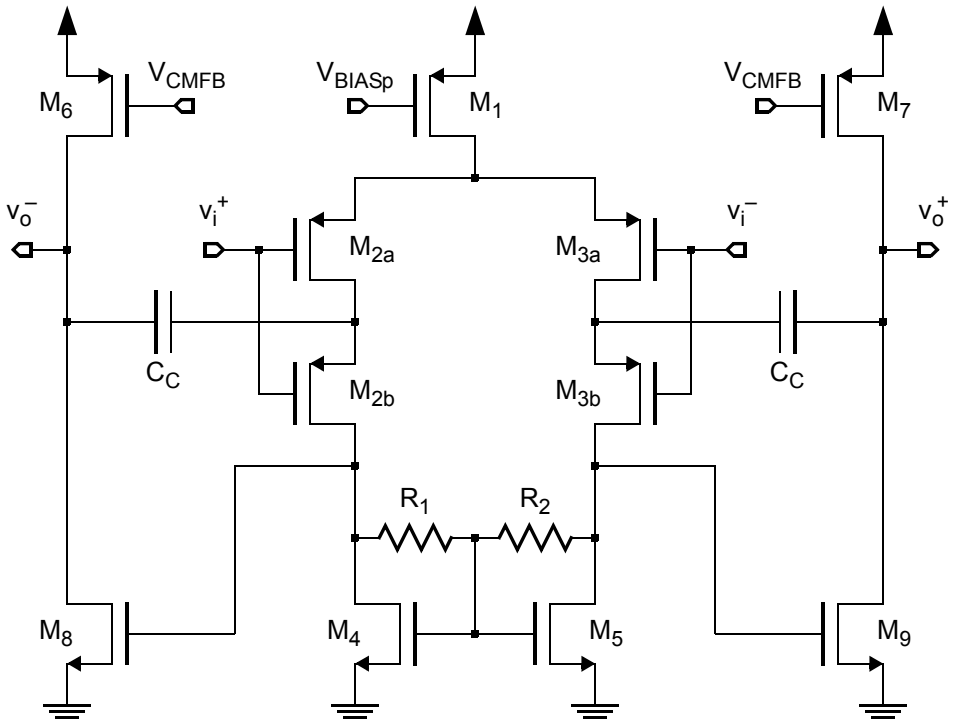
The operational amplifier (opamp) is implemented using a fully-differential two-stage design that provides moderate voltage gain and high output signal swing. Figure 7.8 shows a circuit diagram of the opamp and its common-mode feedback (CMFB) circuit. Here, the first stage is composed of a pMOS differential pair (M_2–M_3), and an nMOS active load (M_4–M_5), and the second stage is composed of an nMOS common-source amplifier (M_8–M_9), and a pMOS active load (M_6–M_7). The opamp is not buffered from its resistive load, since the addition of an output buffer would increase the complexity of the frequency compensation.

The opamp is designed with pMOS input transistors so that the common-mode level that is required at its input ($V_{\mathrm{CM,\,in}}$) can also be used at its output ($V_{\mathrm{CM,\,out}}$) without significantly limiting its output signal swing. In the selected 65-nm CMOS process, the threshold voltage of an nMOS device (V_{tn}) is approximately 50 mV higher than that of the pMOS device (V_{tp}) under equivalent bias conditions. Accordingly, the gates of a pMOS input pair can be biased closer to $V_{\mathrm{DD}}/2$ than the gates of an nMOS input pair, which results in higher output signal swing when $V_{\mathrm{CM,\,out}} = V_{\mathrm{CM,\,in}}$. The same common-mode level is used at the input and output of the opamp to avoid dc level-shifting, which would increase the thermal noise and power consumption of the active-RC integrators [Kar00].

The voltage gain (A_{v1}) of the first stage can be expressed as

$$A_{v1} \;=\; g_{m2,3}\left(\, r_{ds2,3} \,\|\, r_{ds4,5} \,\right) \tag{7.9}$$

where $r_{ds2,3}$ and $r_{ds4,5}$ are the drain-source resistances of M_2–M_3 and M_4–M_5, and $g_{m2,3}$ is the transconductance of M_2–M_3. For a given overdrive voltage, g_m scales directly with the bias current, through the transistor W/L ratio, and r_{ds} scales inversely with the bias current. Accordingly, the bias current of the first stage (I_{bias1}) does not affect the value of A_{v1}, and is selected according to thermal noise requirements.



RESON2

Device	M_1	M_{2a}–M_{3a}	M_{2b}–M_{3b}	M_4–M_5	M_6–M_7	M_8–M_9
W(μm)/L(μm)	48/0.12	80/0.12	80/0.12	21.6/0.36	32/0.12	43.2/0.36

Component	C_C	R_1–R_2
Value	1.2 pF	50 kΩ

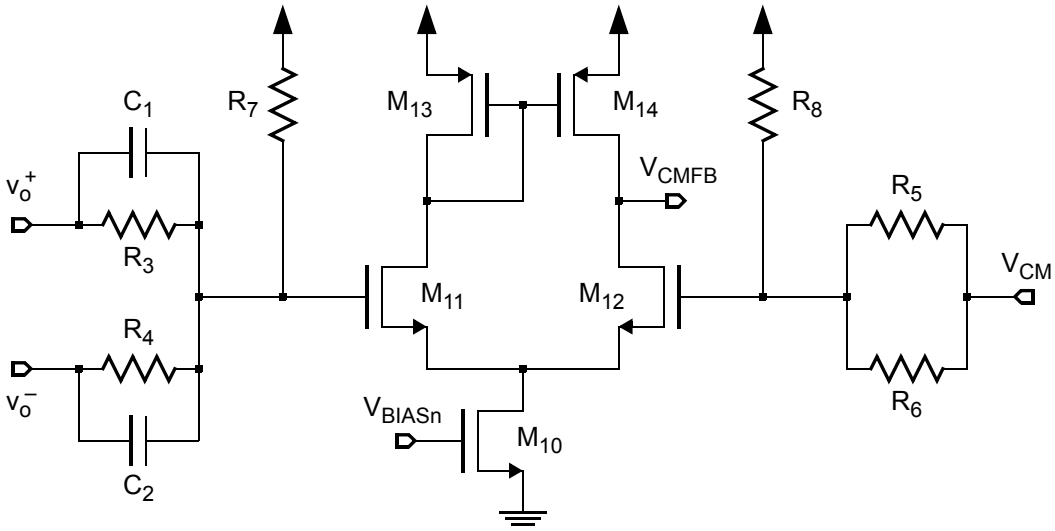
RESON3

Device	M_1	M_{2a}–M_{3a}	M_{2b}–M_{3b}	M_4–M_5	M_6–M_7	M_8–M_9
W(μm)/L(μm)	24/0.12	40/0.12	40/0.12	10.8/0.36	16/0.12	21.6/0.36

Component	C_C	R_1–R_2
Value	0.6 pF	50 kΩ

(a)

Figure 7.8: Circuit diagrams for: **(a)** the operational amplifier, and **(b)** the common-mode feedback circuit of its second stage.



RESON2

Device	M_{10}	M_{11}–M_{12}	M_{13}–M_{14}
W(μm)/L(μm)	10/0.12	5/0.12	9/0.12

Component	R_3–R_6	R_7–R_8	C_1–C_2
Value	25 kΩ	15 kΩ	100 fF

RESON3

Device	M_{10}	M_{11}–M_{12}	M_{13}–M_{14}
W(μm)/L(μm)	5/0.12	2.5/0.12	4.5/0.12

Component	R_3–R_6	R_7–R_8	C_1–C_2
Value	25 kΩ	15 kΩ	100 fF

(b)

The voltage gain (A_{v2}) of the second stage can be expressed as

$$A_{v2} \;=\; g_{m8,9}(\, r_{ds8,9} \,\|\, r_{ds6,7} \,\|\, R_{\mathrm{L}} \,) \tag{7.10}$$

where R_{L} represents the load resistance of the opamp. The value of A_{v2} depends on the bias current of the second stage (I_{bias2}) as follows:

1. When I_{bias2} is low, $r_{ds} \gg R_{\mathrm{L}}$ and $A_{v2} \cong g_{m8,9}(R_{\mathrm{L}})$. Since g_m scales directly with the bias current, for a fixed overdrive voltage, an increase in I_{bias2} results in a proportional increase in the value of A_{v2}.

2. When I_{bias2} is high, $r_{ds} < R_{\mathrm{L}}$ and $A_{v2} \cong g_{m8,9}(\, r_{ds6,7} \,\|\, r_{ds8,9} \,)$. Since r_{ds} scales inversely with the bias current, further increases in I_{bias2} do not result in proportional increases in the value of A_{v2}.

Accordingly, the bias current of the second stage (I_{bias2}) is selected so that $r_{ds} > R_{\mathrm{L}}$, in order to maximize the gain efficiency for a given value of R_{L}.

Common-Mode Feedback

The operational amplifier is designed with separate common-mode feedback (CMFB) circuits for its first and second stages, as shown in Figure 7.8. The common-mode levels of the first and second stages are set to 515 mV and 450 mV, respectively.

The common-mode level of the first stage does not need to be set to an external reference, and is established using feedback resistors R_1–R_2. These resistors are selected such that they do not limit the voltage gain. The common-mode level of the second stage must be set to an external reference, since it drives the next integrator. This common-mode level is established by a CMFB loop, which senses the voltage at the output of the opamp using resistors R_3–R_4, and adjusts the voltage at the gates of transistors M_6–M_7. Since the output resistance of the opamp is relatively small, the voltage at the output can be sensed without a source follower, which improves its output signal swing [Joh97].

The CMFB loop of the second stage uses a single-stage amplifier with a differential input and a single-ended output. Since this amplifier drives the gates of pMOS transistors M_6–M_7, it must have pMOS load transistors and, therefore, nMOS input transistors. In order to drive an nMOS input pair, the common-mode level of the second stage is shifted to 725 mV using a resistive voltage divider formed by R_3, R_4, and R_7. The reference common-mode level is also shifted, using a corresponding resistive voltage divider formed by R_5, R_6, and R_8, in order to correct for process variations. The frequency compensation of the CMFB loop is provided by capacitors C_1–C_2 [Raz01].

Frequency Compensation

The frequency compensation of the operational amplifier is implemented using the modified cascode compensation technique described in [Tah11]. Here, the input transistors (M_2–M_3) are each split, and the compensation capacitors (C_C) are connected to the intermediate nodes of the split transistors.

This modified cascode compensation technique is better suited to low-voltage design than Miller compensation, since its compensation network does not require a transistor biased in triode [Tah11]. Furthermore, it requires less bias circuitry, and therefore consumes less power than conventional cascode compensation, while maintaining the same advantages relative to Miller compensation: process-insensitive poles and zeros, higher power-supply rejection, and higher phase margin for the same compensation capacitance [Ahu83][Hur04].

When the input transistors (M_2–M_3) are split, M_{2a}–M_{3a} operate in triode and M_{2b}–M_{3b} operate in saturation. In order to bring transistors M_{2a}–M_{3a} closer to the edge of saturation, the bulk terminals of M_{2a}–M_{3a} are connected to V_DD, while the bulk terminals of M_{2b}–M_{3b} are connected to the sources of M_{2a}–M_{3a}. This increases the threshold voltages of M_{2a}–M_{3a}, relative to those of M_{2b}–M_{3b}, and increases their gate-source voltages correspondingly. Since the gates of M_{2a}–M_{2b} and M_{3a}–M_{3b} are each connected, increasing the gate-source voltages of M_{2a}–M_{3a}, relative to those of M_{2b}–M_{3b}, increases the drain-source voltages of M_{2a}–M_{3a}, and therefore moves them closer to saturation. This bias configuration increases the dc gain of the opamp without reducing its phase margin.

Noise

The in-band noise performance of the operational amplifier is dominated by the noise of its first stage. The noise that is introduced in its second stage is effectively divided by the gain of its first stage, and is therefore negligible. The noise performance of first stage is dominated by thermal noise. The channel lengths of the input and load transistors are increased to $3L_{\min}$ so that their flicker ($1/f$) noise is negligible over the frequency range of interest.

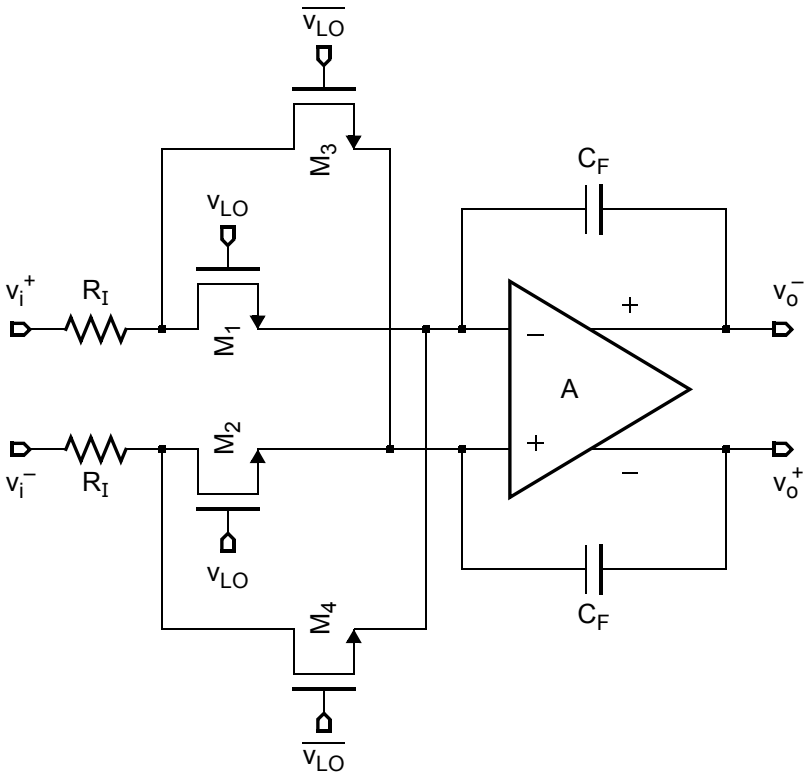
The first stage of the opamp is biased with a tail current of $I_{\text{tail}} = 400\,\mu\text{A}$. In simulation, this bias results in an rms thermal noise density of $5.5\,\text{nV}/\sqrt{\text{Hz}}$ at $f_{Co} = 25\,\text{MHz}$.

7.2.3 Switching Mixer

The downconversion mixer is implemented using a passive, or switching, topology. Figure 7.9 shows a circuit schematic for the switching mixer, as it would be incorporated into the input resistors of an active-RC integrator. The switching mixer provides a conversion gain of $2/\pi$, which is compensated for in the corresponding loop filter coefficient.

The switches of the downconversion mixer are implemented using simple nMOS devices, which facilitate high-speed operation. In general, the design of the switching transistors is a trade-off between LO leakage and linearity: the LO leakage is reduced by decreasing the gate capacitance of the switches (i.e., decreasing WL), and the linearity is improved by decreasing the on-resistance (r_{on}) of the switches (i.e., increasing W/L). However, since the experimental ΔΣ modulator has a bandpass loop filter and feedforward coefficient paths (Section 6.1), the LO leakage and linearity of the downconversion mixer do not have a significant effect on the resolution. In particular, use of feedforward paths reduces the signal swing through the mixer and facilitates the use of nMOS switches, rather than transmission gates.

The size of the switching transistors (M_1–M_4) is instead selected to reduce the effect of process variations on the loop-filter coefficients of the experimental ΔΣ modulator. Since the switching transistors are connected in series with the input resistors (R_{I}) of the active-RC integrator, their on-resistance ($r_{\text{on1–4}}$) modifies the corresponding loop-filter coefficient. The value of $r_{\text{on1–4}}$ varies significantly with the process, and can therefore limit the noise-shaping performance of the experimental ΔΣ modulator.



Device	M_1–M_4
W(μm)/L(μm)	3/0.06

Figure 7.9: Circuit diagram of the switching mixer.

Accordingly, the size of M_1–M_4 is selected such that the corresponding coefficient varies by less than 5 % under the maximum possible process variation. In behavioural simulations, a 5 % coefficient error results in a loss of SQNR of less than 1 dB. Using this approach, the nominal on-resistance ($r_{\text{on1–4}}$) of M_1–M_4 is equal to 480 Ω.

7.3 Flash ADC

The internal quantizer of the experimental ΔΣ modulator (Section 6.1) is implemented using a 3-bit flash ADC, which has seven binary comparators and a corresponding reference ladder. The comparators are each designed with a single-stage pre-amplifier and a regenerative latch, and the reference ladder is implemented with a single string of resistors. Figure 7.10 shows a circuit diagram of the flash ADC.

7.3.1 Pre-Amplifier

Figure 7.11 shows a circuit diagram for the pre-amplifier that forms the first stage of each comparator in the flash ADC. The pre-amplifier is used to reduce the input-referred offset of the regenerative latch, and to reduce the capacitive feedthrough from the clock input of the latch to the reference ladder. The input transistors of the pre-amplifier (M_3–M_4 and M_5–M_6) subtract the input signal from the corresponding reference level, and pass the resulting signal current to the diode-connected load transistors (M_9–M_{10}). The input and load transistors are designed with long channel lengths ($L = 3L_{\min}$) to improve their matching.

The voltage gain of the pre-amplifier can be expressed as

$$A_v = \frac{g_{m3\text{–}6}}{g_{m9,10}} \tag{7.11}$$

where $g_{m3\text{–}6}$ is the transconductance of the input transistors (M_3–M_6), and $1/g_{m9,10}$ is the input resistance of the load transistors (M_9–M_{10}).

The voltage gain of the pre-amplifier is increased by adding shunt transistors (M_7–M_8) in parallel with its load transistors (M_9–M_{10}). These shunt transistors decrease the bias current through the load transistors, which decreases their transconductance ($g_{m9,10}$) and, therefore, increases the voltage gain [Gre99]. Here, the shunt current is four times higher than the load current, which increases the voltage gain by approximately 11 dB.

In simulation, the pre-amplifier achieves a voltage gain of 6.1 dB. It has an input-referred rms thermal noise density of $25\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $f_{Co} = 25\,\mathrm{MHz}$, and an rms offset of 11.9 mV. The pre-amplifier consumes 50 μW from a 1-V power supply.

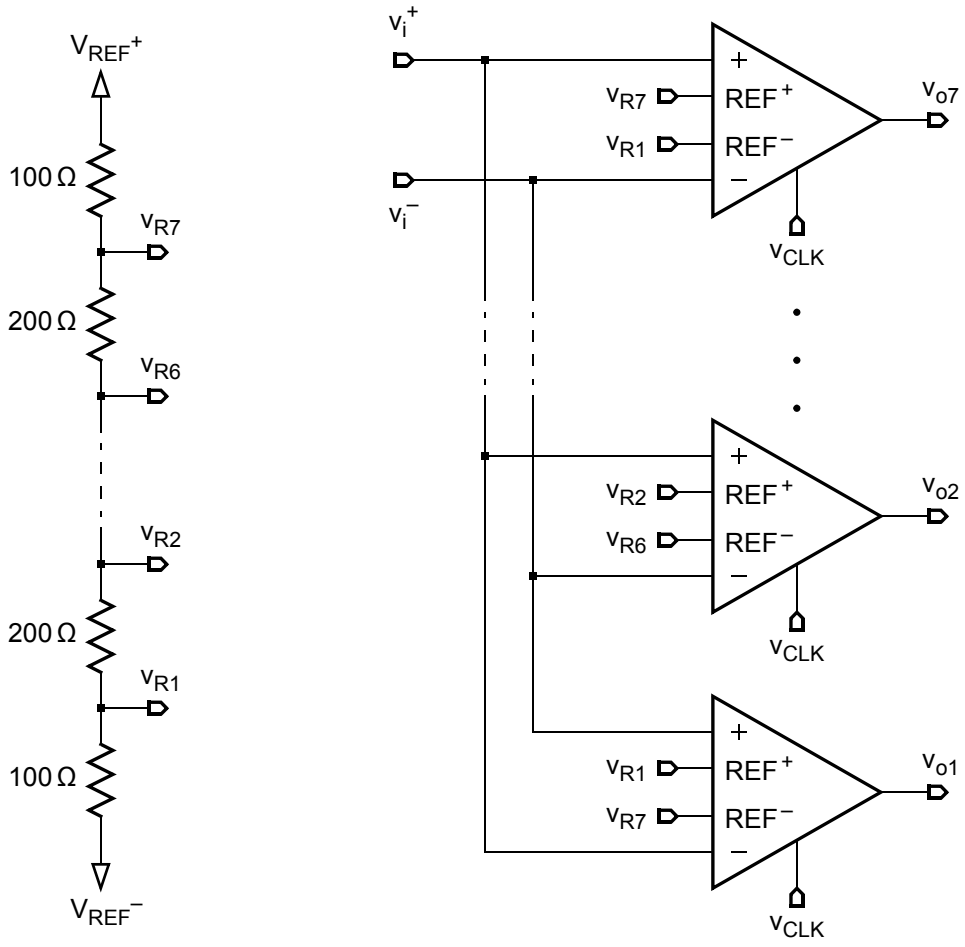
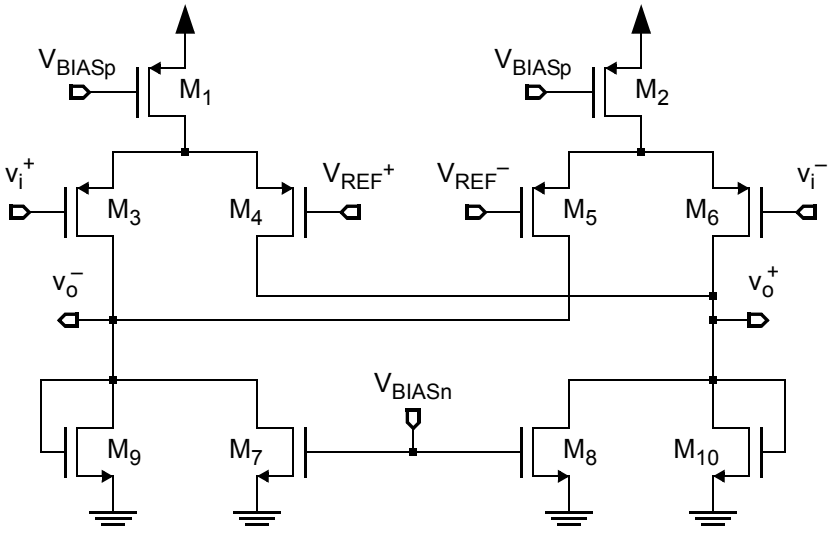


Figure 7.10: Circuit diagram of the flash ADC.

7.3.2 Regenerative Latch

Figure 7.12 shows a circuit diagram for the regenerative latch that forms the second stage of each comparator in the flash ADC. When the sampling clock is low, transistors M_9–M_{10} connect the outputs of the latch to V_{DD}, so that it is reset. When the sampling clock is high, transistors M_5–M_6 connect the cross-coupled inverters implemented by M_3–M_4 and M_7–M_8, and the input transistors (M_1–M_2) force the next input onto the latch. The input transistors are designed with long channel lengths ($L = 3L_{min}$) to improve their matching.



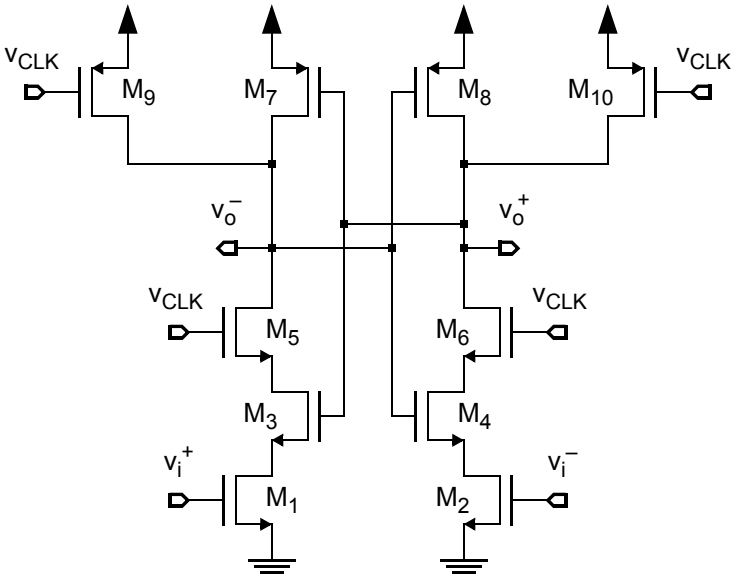
Device	M_1–M_2	M_3–M_6	M_7–M_8	M_9–M_{10}
W(μm)/L(μm)	5.6/0.12	5/0.18	1.6/0.18	0.4/0.18

Figure 7.11: Circuit diagram of the pre-amplifier.

In simulation, the regenerative latch achieves an rms offset of 10.6 mV. In order to derive the total offset of the comparator, the offset of the latch is referred to the input, and is added to the offset of the pre-amplifier.

7.3.3 Reference Ladder

The reference ladder of the flash ADC is composed of six 200 Ω unit resistors. It is designed using positive and negative references of 625 mV and 275 mV, which result in a step size (Δ) of 100 mV. The reference ladder is connected to the positive and negative references through two 100 Ω resistors, which reduce the effect of process variations. The size of the unit resistor is selected to reduce the power consumption and capacitive feedthrough.



Device	M_1–M_2	M_3–M_4	M_5–M_6	M_7–M_8	M_9–M_{10}
W(μm)/L(μm)	4/0.18	1/0.06	1/0.06	2.5/0.06	0.5/0.06

Figure 7.12: Circuit diagram of the regenerative latch.

The capacitive feedthrough, or *kick-back*, from the clock input of the regenerative latch to the reference ladder introduces errors into the reference levels that can affect the decisions of the comparators. The kick-back error scales with the input capacitances of the pre-amplifier and latch, and the unit resistance of the reference ladder [Ort06]. Since the channel lengths of the input transistors are determined by matching requirements, the input capacitances of the latch and pre-amplifier are effectively fixed. Accordingly, the kick-back error is decreased by reducing the size of the unit resistors.

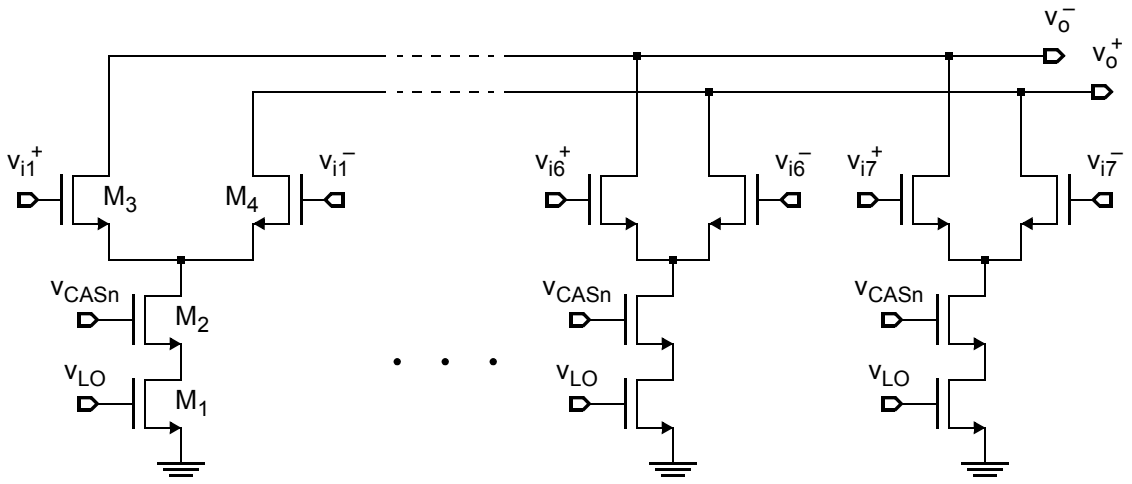
The reference ladder consumes 250 μW. In simulation, the ladder results in a maximum kick-back error of 6.5 mV for a clock signal with a rise time of 50 ps.

7.4 Feedback DACs

This section describes the circuit-level design of the feedback DACs of the experimental ΔΣ modulator (Section 6.1).

7.4.1 Outer-Loop DAC

Figure 7.13 shows a circuit diagram for the outer-loop DAC (DAC1). It is implemented with a current-mode topology, and uses the LO signal to generate raised-cosine pulse shaping. Here, the digital input signal (the thermometer-coded output of the flash ADC) controls the input transistors (M_3–M_4), which steer the current of the tail transistor (M_1) either to the positive or negative output. The tail transistor is cascoded (M_2) to provide isolation from the digital input signal, and to increase the output resistance of the DAC. The outer-loop DAC (DAC1) is connected directly to RESON1, and must therefore have a high output resistance to prevent it from reducing the quality factor of the LC tank.



Device	M_1	M_2	M_3–M_4
W(μm)/L(μm)	24/0.72	10/0.12	4/0.12

Figure 7.13: Circuit diagram of the outer-loop DAC (DAC1).

The outer-loop DAC (DAC1) is designed with raised-cosine pulse shaping. This enables it to upconvert the feedback signal of the experimental $\Delta\Sigma$ modulator, and to achieve reduced sensitivity to clock jitter [Lus04]. A raised-cosine pulse is generated by applying the LO signal to the gate of the tail transistor (M_1) in the place of a fixed bias voltage. The sampling clock and the LO signal are then synchronized such that, during an input transition, the LO signal is low and M_1 is turned off. This reduces the effect of timing errors on the shape of the DAC pulse, and therefore gives the experimental $\Delta\Sigma$ modulator high immunity to clock jitter.

Figure 7.14 shows circuit diagrams for the driver and latch that are used before each unit element of the outer-loop DAC (DAC1). These circuits are designed to reduce the effect of the following issues, which limit the dynamic performance of a current-mode DAC [Bos99]:

1. The capacitive feedthrough of the digital input signal to the output. The transitions on the input signal of the DAC can couple to its output across the gate capacitance of the input transistors (M_3–M_4). These errors are reduced by decreasing the output swing of the high-crossing switch driver [Fal99]. The low output level (V_{DRV}) of the driver is set using a bias voltage of 600 mV, which is generated off-chip.

2. The variation in the drain-source voltage of the tail transistor (M_1). If the digital input signal of the DAC is applied directly to the gates of M_3–M_4, both devices turn off for a short period of time during each input transition. This causes the parasitic capacitance at the sources of M_3–M_4 to discharge, which decreases the drain-source voltage of M_1, and therefore introduces an error into the output current. This error is reduced by using a high-crossing switch driver [Fal99], as shown in Figure 7.14(b). This driver ensures that M_3–M_4 are never off at the same time.

3. The synchronization of the input signals in a multi-bit design. The digital input signals of the DAC are latched immediately prior to the drivers, in order to ensure that all unit elements switch at the same time when new data arrives. Figure 7.14(a) shows a circuit diagram for the latch.

The full-scale current of DAC1 is selected to meet thermal-noise requirements, whereas its unit elements are sized to meet matching requirements, as described below.

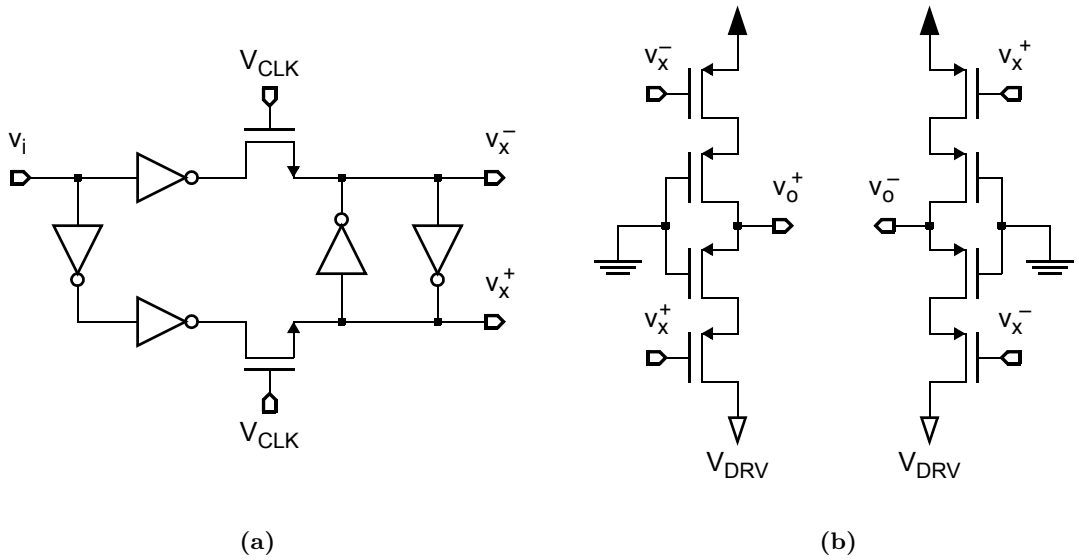


Figure 7.14: Circuit diagrams for: **(a)** the latch, and **(b)** the driver that are used prior to each unit element of the feedback DACs.

Matching

The experimental ΔΣ modulator (Section 6.1) is implemented with multi-bit feedback DACs, and is therefore sensitive to unit element mismatch. This mismatch can reduce the linearity of the ΔΣ modulator, and increase its in-band noise (Section 6.5.3). The static mismatch of the feedback DACs is reduced by increasing the area of their tail transistors. The remaining errors are then suppressed using a bandpass mismatch-shaping scheme.

A conventional[5] bandpass mismatch-shaping scheme suppresses the in-band noise caused by mismatch errors [Shu98] by

$$N_o^2 \;=\; \frac{8\pi^2}{3\,\mathrm{OSR}^3} \tag{7.12}$$

where it is assumed that the *mismatch noise* has a white power spectral density. Therefore, given an OSR of 12.5 ($f_\mathrm{B} = 4\,\mathrm{MHz}$), the mismatch noise is suppressed by 18.7 dB.

[5]This expression is valid for 2nd-order bandpass mismatch shaping around a centre frequency of $f_\mathrm{S}/4$.

According to the behavioural simulation results presented in Section 6.5.3, the mismatch of DAC1 must be reduced below 0.5 % to prevent mismatch errors from significantly affecting the performance of the experimental $\Delta\Sigma$ modulator. The matching of the outer-loop DAC is improved by increasing the lengths of its tail transistors (M_1). In the selected 65 nm process, the required matching is achieved when the channel length of M_1 is set to $12L_{\min}$.

Noise

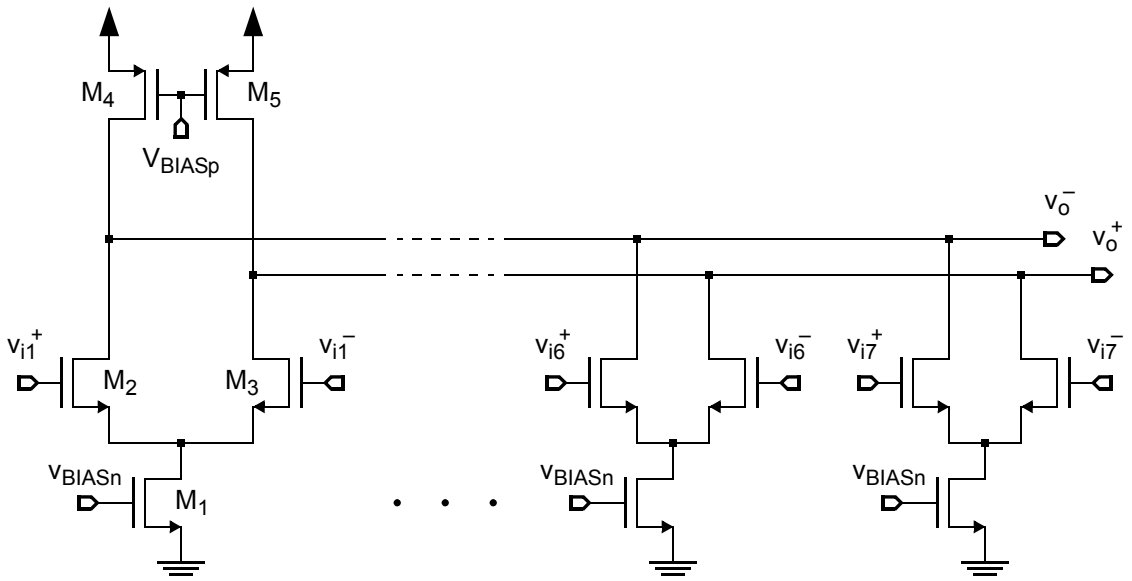
The in-band noise performance of the outer-loop DAC is dominated by the thermal noise of its tail transistor (M_1). The noise contributions of the cascode transistor (M_2) and the input transistors (M_3–M_4) are both degenerated by the output resistance of M_1, and can therefore be neglected. In addition, since M_1 must have a long channel to achieve adequate matching, its flicker ($1/f$) noise can also be neglected.

The thermal noise contribution of the tail transistor (M_1) can be represented using an equivalent voltage source connected in series with its gate, as described in Section 7.1.1. The power spectral density of this noise voltage is white, and is approximated in the same way as Equation (7.2). The total thermal noise of DAC1 is derived by evaluating the noise of one of its unit elements, and multiplying by the number of unit elements. Note that since the input of the DAC is a digital signal, its noise is referred to the input of the transconductor.

The outer-loop DAC is designed with a least significant bit of $I_{\mathrm{LSB}} = 200\,\mu\mathrm{A}$. This results in an input-referred rms thermal noise density of $2\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $f_{\mathrm{C}i} = 225\,\mathrm{MHz}$.

7.4.2 Inner-Loop DACs

Figure 7.15 shows a circuit diagram for one of the inner-loop DACs (DAC2–DAC4). They are implemented with a current-mode topology, and use a fixed bias to generate rectangular pulse shaping. Here, since the nMOS input transistors (M_3–M_4) can only sink current, each of the DACs must be designed with an additional pMOS current source (M_5–M_6), which provides the required offset current.



Device	M_1	M_2–M_3	M_4–M_5
W(μm)/L(μm)	0.25/0.36	0.4/0.12	2.2/0.18

Figure 7.15: Circuit diagram of the inner-loop DACs (DAC2–DAC4).

The inner-loop DACs (DAC2–DAC4) are connected to the last resonator (RESON3) of the loop filter. Therefore, their noise and distortion are largely suppressed by the loop gain of the experimental ΔΣ modulator. This suppression reduces their matching requirements relative to those of the outer-loop DAC (DAC1). Furthermore, since the clock jitter that is introduced at DAC2–DAC4 is also suppressed, it facilitates rectangular pulse shaping.

7.4.3 Mismatch Shaping

The static mismatch between the unit elements of the multi-bit feedback DACs is decreased by increasing the size of their tail transistors, as described in Section 7.4.1. The noise and distortion that are introduced by the remaining mismatch errors are then reduced using a bandpass mismatch-shaping scheme.

The implemented bandpass mismatch-shaping algorithm is based on an element rotation scheme. In an element rotation scheme, the mismatch-shaping logic rotates through the unit elements of the DAC in such a way that the noise and distortion introduced by mismatch are reduced at its output. One of the most widely-used element rotation schemes is data-weighted averaging (DWA) [Bai95]. The DWA algorithm achieves highpass shaping of mismatch errors by rotating forward through the least-recently-used unit elements of the DAC.

The signal band of the experimental $\Delta\Sigma$ modulator is centred at $f_S/4$ when it is processed by the mismatch-shaping logic (Section 6.1). In order to implement bandpass shaping at $f_S/4$, this logic must provide a mismatch transfer function[6] of

$$H_2(z) \;=\; 1 + z^{-2} \tag{7.13}$$

An element rotation scheme can be specified in terms of its selection pattern. The mismatch transfer function in Equation (7.13) is implemented by the element selection pattern defined in [Shu98], which is derived from a two-path transformation ($z \rightarrow z^2$) of

$$H_1(z) \;=\; 1 + z^{-1} \tag{7.14}$$

Figure 7.16 shows element selection patterns for both $H_1(z)$ and $H_2(z)$ [Shu98]. Here, $H_1(z)$ is implemented by rotating back and forth through the most-recently-used unit elements of the DAC, and $H_2(z)$ is a time-interleaved version of $H_1(z)$.

Figure 7.17 provides a block diagram for the bandpass mismatch-shaping logic. Here, the thermometer-coded output $\texttt{out}_\texttt{t}\texttt{(n)}$ of the flash ADC is rotated according to the value of the pointer `ptr(n)`, which is derived from the addition of the previous output codes. In order to implement bandpass mismatch shaping around $f_S/4$, a two-cycle delay is required between the output and the input of the adder. That is, the next pointer $\texttt{ptr}_\texttt{nn}\texttt{(n)}$ is equal to the sum of the current digital output code $\texttt{out}_\texttt{d}\texttt{(n)}$ and the pointer generated two cycles previously $\texttt{ptr(n) = ptr}_\texttt{nn}\texttt{(n-2)}$. Furthermore, the thermometer-coded output $\texttt{out}_\texttt{t}\texttt{(n)}$ must be flipped at four-cycle intervals, and the digital output code $\texttt{out}_\texttt{d}\texttt{(n)}$ must be similarly inverted. Both of these operations use a divided clock (`clk4`), which is generated locally.

[6]The mismatch transfer function (MTF) is used to specify the mismatch-shaping performance.

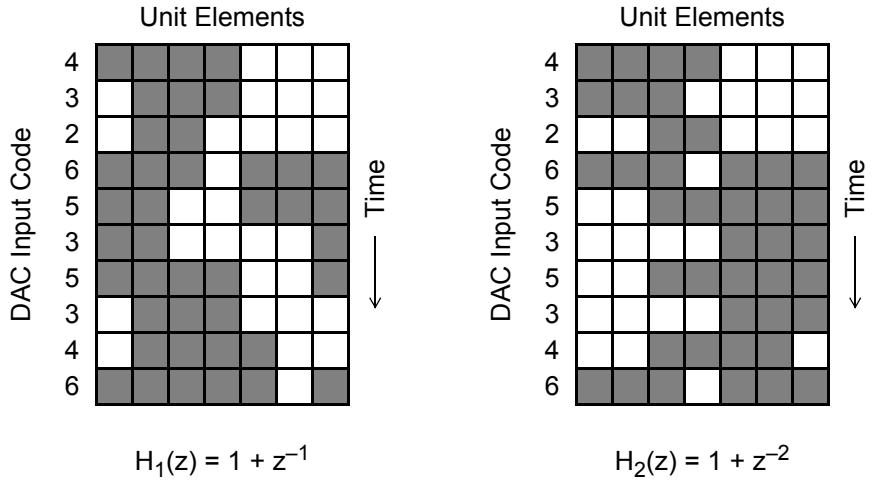


Figure 7.16: Element selection patterns for: **(a)** $H_1(z)$, and **(b)** $H_2(z)$ [Shu98].

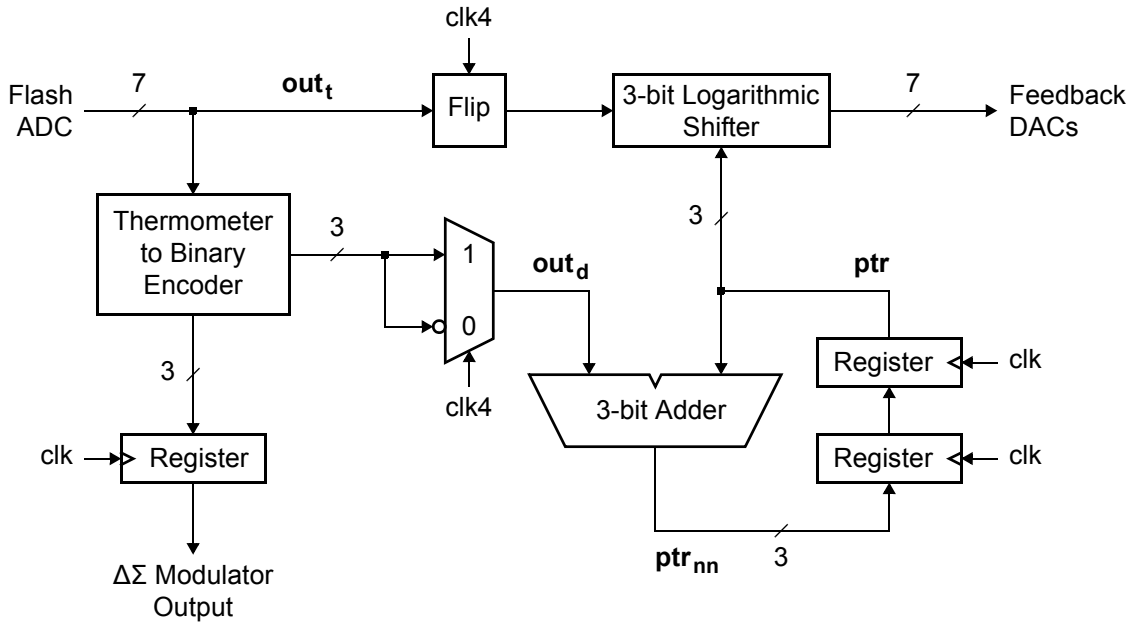


Figure 7.17: Block diagram for the bandpass mismatch-shaping logic.

Chapter 8

Experimental Results

The experimental single-path frequency-translating $\Delta\Sigma$ modulator (Figure 7.1) was fabricated in a 65-nm digital CMOS process, and operates from a nominal 1-V supply. This chapter presents the layout and test setup of the experimental prototype, and compares its measured performance to state-of-the-art bandpass $\Delta\Sigma$ modulators. This comparison only considers designs that are implemented in CMOS technology.

The experimental $\Delta\Sigma$ modulator (Figure 7.1) is designed to digitize a 4 MHz signal band that is centred at 225 MHz. It uses an LO signal with a frequency of 200 MHz to downconvert the signal band to a centre frequency of 25 MHz inside its $\Delta\Sigma$ loop, and samples at 100 MHz. The experimental prototype achieves a peak SNR of 55.5 dB, a peak SNDR of 55.0 dB, and a dynamic range of 57.5 dB. It consumes 13 mW from a 1-V power supply, where its analog and digital circuits consume 12.75 mW and 0.25 mW, respectively. The measured performance of the experimental prototype is competitive with state-of-the-art bandpass $\Delta\Sigma$ modulators, as demonstrated by Table 8.2.

This chapter is divided into four sections. Section 8.1 discusses layout considerations for the experimental $\Delta\Sigma$ modulator, and provides the chip micrograph. Section 8.2 describes the printed circuit board (PCB) and experimental test setup. Section 8.3 presents the measured performance of the experimental prototype, and Section 8.4 then compares this performance to state-of-the-art bandpass $\Delta\Sigma$ modulators.

8.1 Layout

The experimental $\Delta\Sigma$ modulator is implemented in a 1-poly 7-metal 65-nm CMOS process, without any special options. The selected process provides both low-power (LP) devices and general-purpose (GP) devices in its standard options; the GP devices nominally operate from a 1-V supply and the LP devices nominally operate from a 1.2-V supply. The analog circuits of the experimental $\Delta\Sigma$ modulator are implemented using the GP devices, whereas its digital circuits are implemented using the LP devices. However, both the analog and digital circuits of the experimental $\Delta\Sigma$ modulator operate from a 1-V supply.

Figure 8.1 shows the chip micrograph of the experimental $\Delta\Sigma$ modulator. It occupies an active area of $0.55\,\mathrm{mm}^2$. Here, REF denotes a voltage reference, BIAS denotes a current bias, and CTL denotes a control signal.

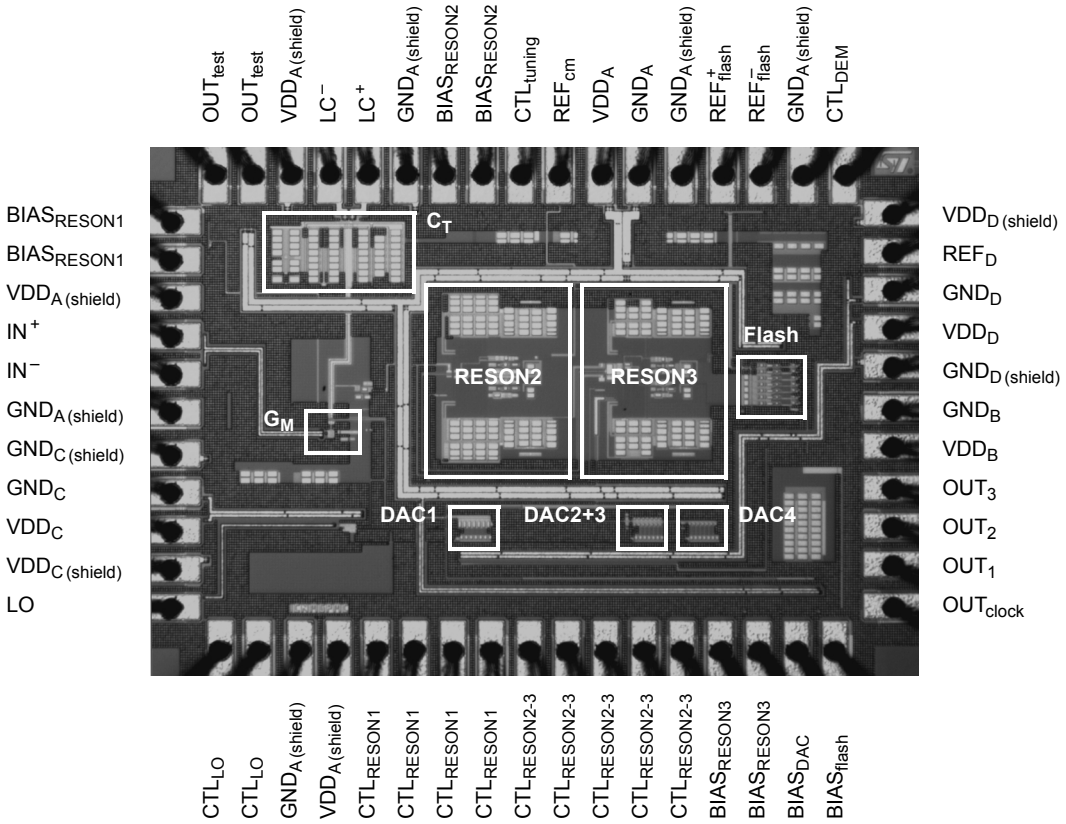


Figure 8.1: Chip micrograph of the experimental $\Delta\Sigma$ modulator.

The experimental $\Delta\Sigma$ modulator is implemented with four separate pairs of supply and ground lines. The *analog* supply ($\mathrm{VDD_A}$, $\mathrm{GND_A}$) is used for the LC resonator, the active-RC resonators, the unit elements of the feedback DACs, and the pre-amplifiers of the flash ADC. The *digital* supply ($\mathrm{VDD_D}$, $\mathrm{GND_D}$) is used for the latches of the flash ADC, and those of the feedback DACs, and for the mismatch-shaping logic. The *clock* supply ($\mathrm{VDD_C}$, $\mathrm{GND_C}$) is used for the clock generator, and the *buffer* supply ($\mathrm{VDD_B}$, $\mathrm{GND_B}$) is used for the output buffers. The supply lines are separated in this way to reduce the coupling of switching noise from the digital, clock, and buffer circuits into the sensitive analog circuits [Raz01]. The ground lines are connected off-chip to prevent latch-up.

In order to reduce the coupling of substrate noise into sensitive circuits, the main blocks of the experimental $\Delta\Sigma$ modulator (e.g., the transconductor and operational amplifiers) are surrounded by guard rings, and long signal interconnects are placed over n-wells. In order to reduce crosstalk, sensitive signals are shielded from one another with additional lines biased at signal ground. These additional layout elements are connected to separate *shield* supplies, which are associated with the above mentioned power supplies.

Decoupling capacitors are placed on the supply and reference lines to reduce the effect of switching transients, and to bypass the noise introduced by the dc power supplies. Additional decoupling capacitors are placed off-chip, as outlined in Section 8.2. Damping resistors ($15\,\Omega$) are connected in series with the on-chip decoupling capacitors to minimize ringing on the supply and reference lines [Raz01].

8.2 Test Setup

The experimental prototype was packaged in a 80-pin ceramic quad flat pack (CQFP), which was mounted on a custom printed circuit board (PCB). Figure 8.2 shows the test setup for a single-tone input signal.

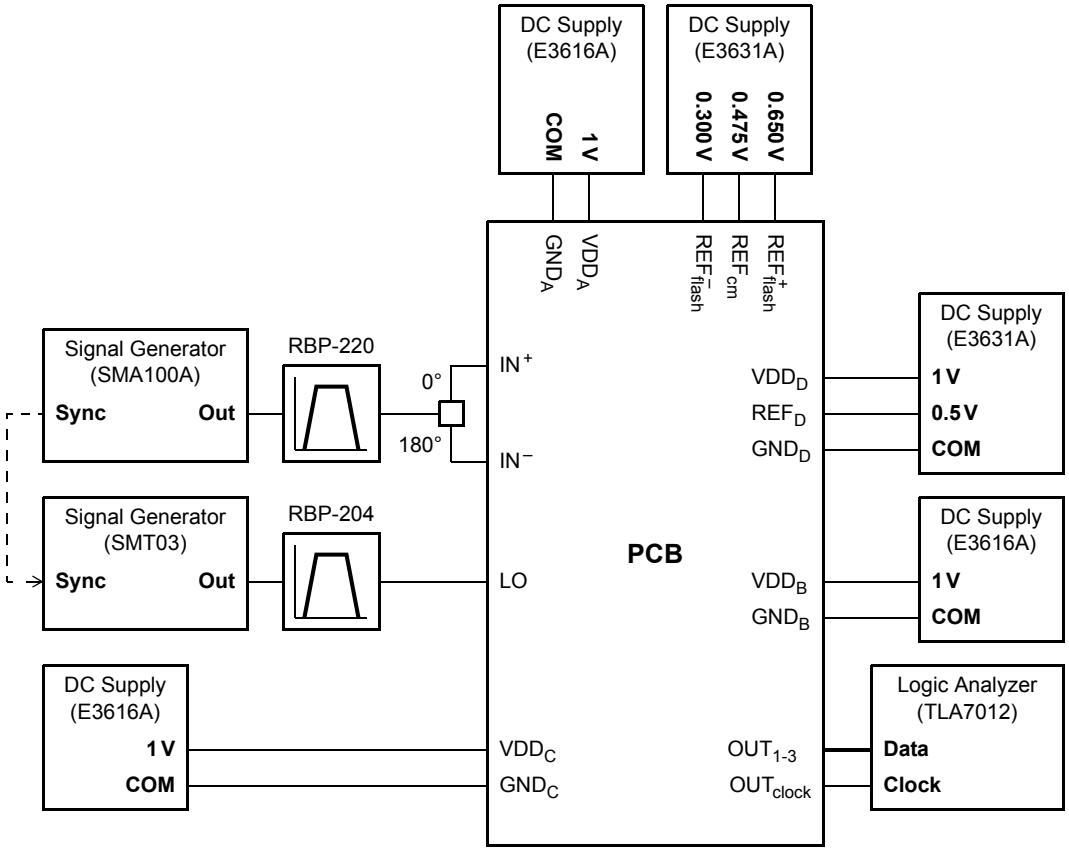


Figure 8.2: Test setup of the experimental prototype for a single-tone input signal.

The PCB is designed with four layers. The top layer contains the input/output connectors, the tuning control, and the components related to biasing. The middle two layers are ground and power planes, each of which is split into four sections that correspond to the supplies on the chip (analog, digital, clock, and buffer). The bottom layer is used primarily for decoupling capacitors. The inductors of the LC tank are also placed on the bottom layer of the PCB in order to ensure that they are as close as possible to the corresponding pins of the chip.

Decoupling capacitors are placed on each of the supply and reference traces at the point where the wires from the associated dc power supplies are connected to the PCB. The supply and reference voltages each pass through capacitors ranging from 100 μF to 0.001 μF, where the smallest capacitors are repeated close to the chip. Here, multiple capacitors are placed in parallel to increase the range over which they provide effective decoupling [Mon00].

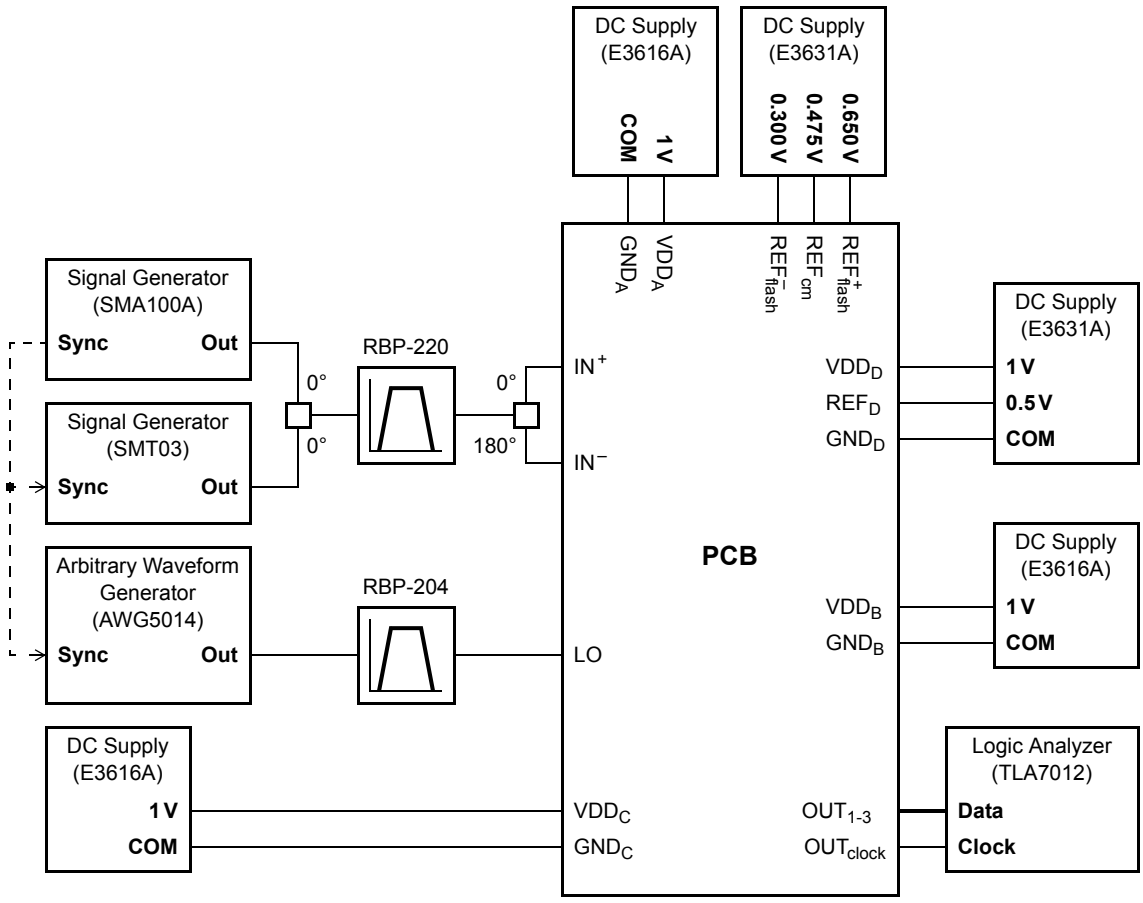


Figure 8.3: Test setup of the experimental prototype for a two-tone input signal.

The input and LO signals of the experimental $\Delta\Sigma$ modulator are generated using analog signal generators (SMA100A and SMT03), which are synchronized with a 10 MHz pulse. The clock signal is derived from the LO signal on-chip in order to ensure correct synchronization between these signals. When a two-tone input is required, the input signals are generated by the aforementioned analog signal generators, and the LO signal is generated by an arbitrary waveform generator (AWG5014). Figure 8.3 shows the test setup for a two-tone input signal. The input signal and LO signal are processed using bandpass filters RBP-220 and RBP-204 before they reach the PCB.

The 3-bit output of the $\Delta\Sigma$ modulator is captured on a logic analyser (TLA7012), and is processed in Matlab. The experimental prototype is implemented with a clock output, which is used to synchronize the logic analyser with the output data.

8.3 Measurement Results

This section summarizes the measured performance of the experimental $\Delta\Sigma$ modulator, and compares these results to its simulated performance (Section 6.3).

During the initial phase of testing, the LC resonator (Figure 7.2) demonstrated common mode oscillations around 375 MHz. These oscillations were caused by signal feedback through the gate-drain capacitance of the input transistors. In order to reduce these oscillations, two 1.5 kΩ resistors were connected in parallel with the discrete inductors of the LC tank. These resistors decreased the quality factor of the tank, from 25 to approximately 15, and therefore decreased the noise-shaping performance of the experimental $\Delta\Sigma$ modulator (Section 6.5.1). The observed oscillations could be eliminated in a revised implementation by adding cascode transistors between the input transistors and the LC tank. Cascode transistors were not used in the experimental $\Delta\Sigma$ modulator because they decreased its linearity, and the oscillations were not present in simulation.

Figure 8.4 shows an example of the measured output of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone at $f_{\text{in}} = 224.6$ MHz. Note that this input tone is downconverted to a frequency of $f_{\text{out}} = 24.6$ MHz at the output of the experimental prototype.

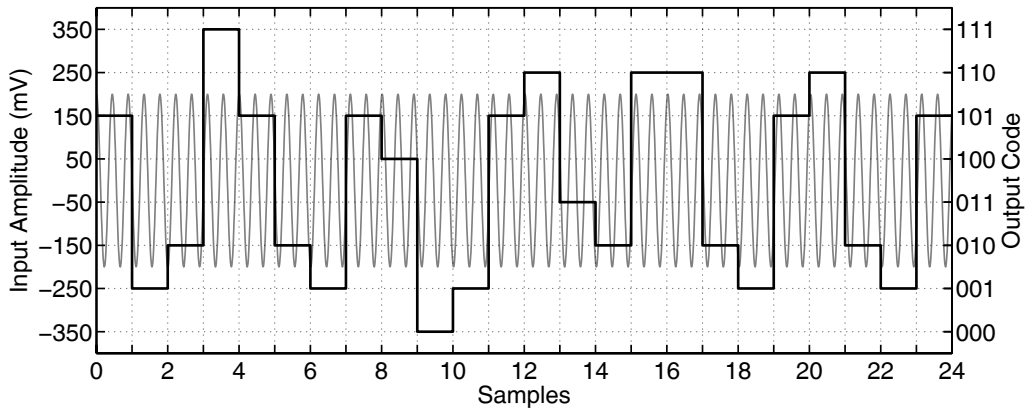
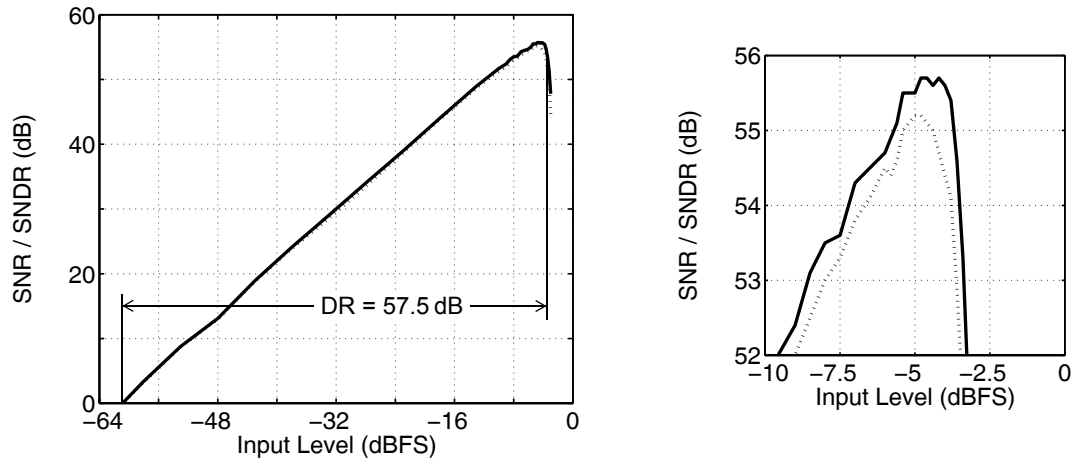


Figure 8.4: Measured output of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone.

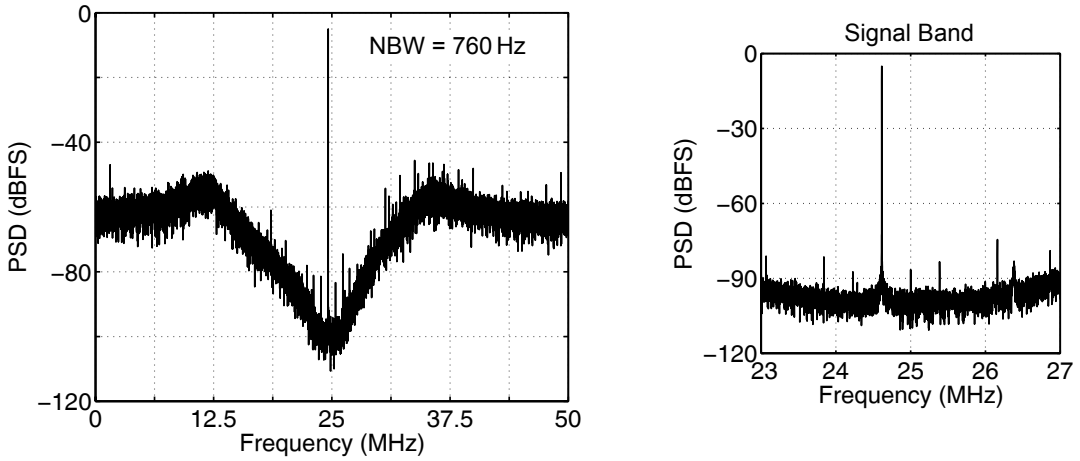


(a) **(b)**

Figure 8.5: Measured SNR and SNDR of the experimental $\Delta\Sigma$ modulator as a function of its input level for an input tone at 224.6 MHz. (SNR — and SNDR $\cdots$)

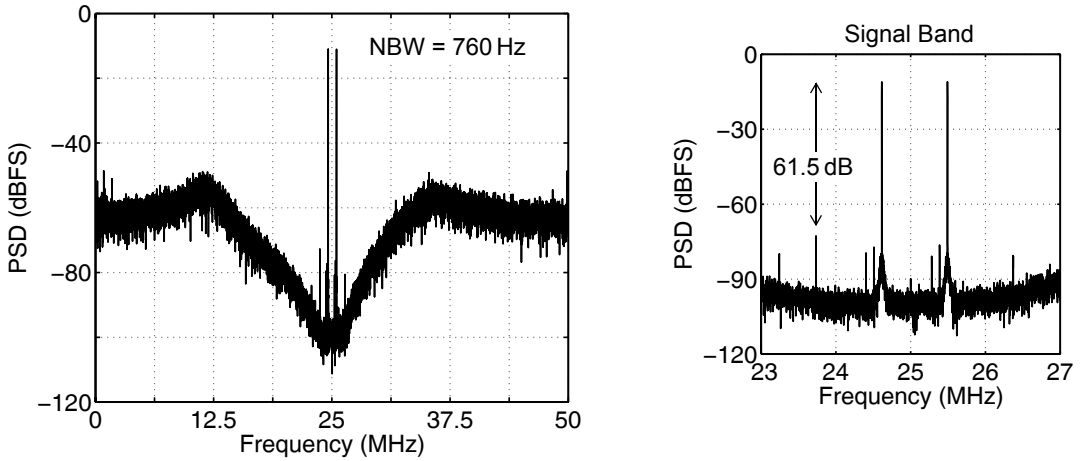
Figure 8.5 plots the measured SNR and SNDR versus the input level for an input tone at $f_{\text{in}} = 224.6\,\text{MHz}$. The experimental $\Delta\Sigma$ modulator achieves a peak SNR of 55.5 dB, a peak SNDR of 55 dB, and a dynamic range of 57.5 dB for a signal bandwidth of $f_{\text{B}} = 4\,\text{MHz}$. The peak SNDR was measured at a differential input-signal amplitude of $395\,\text{mV}_{\text{P-P}}$ (-5 dBFS), where the full-scale range of the quantizer is equal to $700\,\text{mV}_{\text{P-P}}$ (0 dBFS). Figure 8.6 plots the measured output spectrum of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone at 224.6 MHz. Figure 8.7 plots the output spectrum for two -11 dBFS input tones separated by 880 kHz, and demonstrates a third-order intermodulation distortion (IM3) of -61.5 dBc. Both plots use a noise bandwidth (NBW) of 760 Hz.

Figure 8.8 compares the measured output spectrum of the experimental $\Delta\Sigma$ modulator to its simulated output spectrum, where the latter incorporates the effect of circuit noise and non-linear distortion (Section 6.4). This plot demonstrates that the measured noise floor of the experimental $\Delta\Sigma$ modulator is higher than its simulated noise floor. This increase in the



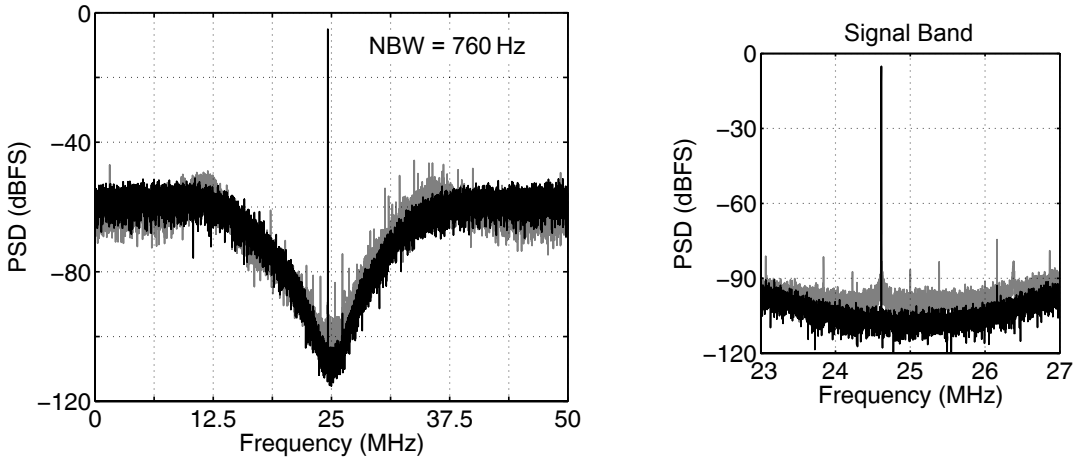
(a) **(b)**

Figure 8.6: Measured output spectrum of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone at 224.6 MHz: **(a)** from 0 to $f_S/2$, and **(b)** over the signal band.



(a) **(b)**

Figure 8.7: Measured output spectrum of the experimental $\Delta\Sigma$ modulator for two -11 dBFS tones separated by 880 kHz: **(a)** from 0 to $f_S/2$, and **(b)** over the signal band.

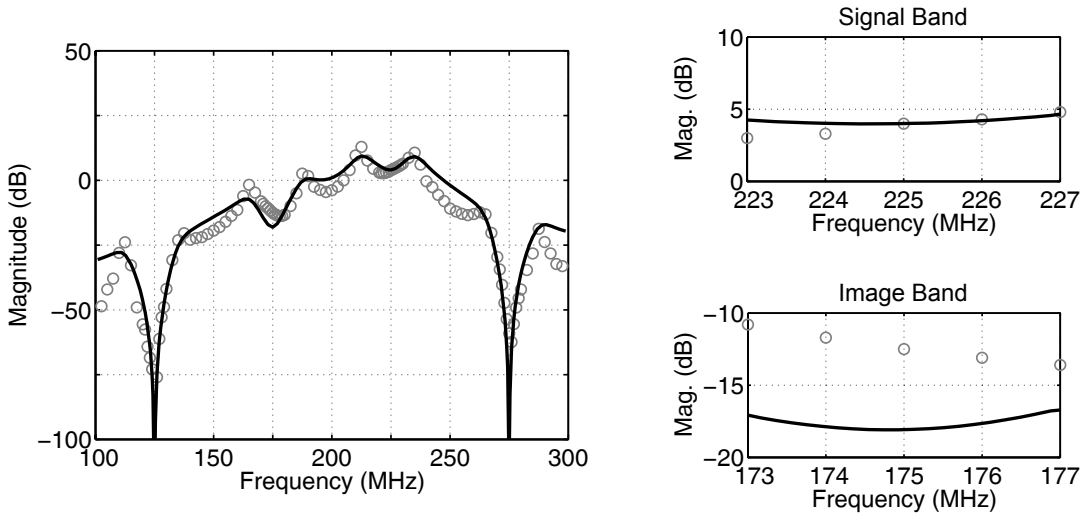


(a) **(b)**

Figure 8.8: The simulated and measured output spectrum of the experimental $\Delta\Sigma$ modulator for a -5 dBFS input tone at 224.6 MHz: **(a)** from 0 to $f_S/2$, and **(b)** in the signal band. Here, the black spectrum denotes simulation results, and the grey spectrum denotes measurement results.

noise floor is caused primarily by the reduced quality factor of the LC resonator (RESON1), as described above. It decreases the measured SNDR of the experimental $\Delta\Sigma$ modulator by approximately 6 dB from its simulated value.

The measured output spectrum of the experimental $\Delta\Sigma$ modulator further deviates from its simulated output spectrum around $f_S/8$ and $3f_S/8$. This deviation is a result of reducing the bias currents of the inner-loop feedback DACs (DAC2–DAC4). These bias currents were reduced to decrease the values of loop-filter coefficients $a_5 - a_7$ in Figure 6.3. It was necessary to decrease these coefficients in order to improve the linearity of the experimental prototype, which was limited by the distortion of its first active-RC resonator (RESON2). Note that the additional peaking in the NTF (Figure 8.8) did not significantly limit the input amplitude of the experimental prototype.



(a) **(b)**

Figure 8.9: The measured STF of the experimental $\Delta\Sigma$ modulator: **(a)** from f_S to $3f_S$, **(b)** over the signal band and over the image band. Here, — denotes simulation results (Figure 6.7), and ○ denotes measurement results.

Figure 8.9 plots the measured STF of the experimental $\Delta\Sigma$ modulator, together with the simulated STF (Section 6.3). The measured STF has lower attenuation over the image band, as compared to the simulated STF, and has additional peaking around aliases of the signal band. The lower attenuation over the image band is a result of the reduced quality factor of the LC resonator (RESON1), whereas the additional peaking is a result of the reduced bias currents of the inner-loop feedback DACs (DAC2–DAC4). These implementation issues were discussed previously in the context of the noise-shaping performance. This plot demonstrates that the measured image-reject filtering[1] of the experimental $\Delta\Sigma$ modulator is 16.5 dB at the centre frequency of its image band (175 MHz).

The experimental $\Delta\Sigma$ modulator consumes 13 mW under a 1-V voltage supply. The analog circuits consume 12.75 mW, whereas the digital circuits and clock buffers consume 0.25 mW. Table 8.1 summarizes the measured performance.

[1]The inherent image-reject filtering is evaluated using Equation (5.36) in Section 5.6.

Table 8.1: Measured performance of the experimental ΔΣ modulator.

Parameter		Value
Input Centre Frequency	f_{Ci}	225 MHz
Output Centre Frequency	f_{Co}	25 MHz
LO Frequency	f_{LO}	200 MHz
Sampling Frequency	f_S	100 MHz
Signal Bandwidth	f_B	4 MHz
Peak SNR		55 dB
Peak SNDR		55.5 dB
Dynamic Range	DR	57.5 dB
Intermodulation Distortion	IM3	−61.5 dBc
Image-Reject Filtering	IR	16.5 dB
Power Consumption	P_{total}	13 mW
Analog		12.75 mW
Digital/Clock		0.25 mW
Supply Voltage		1 V
Process		65 nm CMOS

8.4 Comparison to the State-of-the-Art

Table 8.2 compares the measured performance of the experimental ΔΣ modulator to that of state-of-the-art bandpass ΔΣ modulators. This table only includes CMOS implementations, and is restricted to wideband ($f_B \geq 1$ MHz) bandpass ΔΣ modulators that have high input centre frequencies ($f_{Ci} \geq 20$ MHz). It considers conventional bandpass architectures, as well as frequency-translating and subsampling architectures (Section 2.3).

Table 8.2: State-of-the-art CMOS bandpass $\Delta\Sigma$ modulators ($f_B \geq 1\,\text{MHz}$ and $f_{Ci} \geq 20\,\text{MHz}$).

Reference	Arch.[a]	f_{Ci} (MHz)	f_S (MHz)	f_B (MHz)	DR (dB)	SNDR (dB)	SNR (dB)	IM3 (dB)	CMOS Process	Supply (V)	Power (mW)	FOM
[Sal02]	CN	20	80	3.84	50	48	48	-	0.35 μm	3	38	24.1
[Sal03]	CN	20	80	1.25	82	75	75	-	0.35 μm	3	37	3.2
	CN			1.762	72	69	70	-			37	4.6
	CN			3.84	50	48	48	-			38	24.1
[Tha03]	CN	23	92	3.84	-	-	54	58	0.35 μm	2.5	47.5	18.0
[Yin04]	CN	40	2×60	2.5	-	69	72	-	0.18 μm	1.8	150	13.0
[Che04]	CN	60	2×120	1.25	-	52	-	51	0.35 μm	3.3	37	4.5
[Sch06b]	CN	44	264	8.5	85	-	77	72	0.18 μm	3.3/1.8	375	7.6
[Gal07]	CN	40	2×60	1	72	-	65.1	68	0.18 μm	1.8	16	6.7
[Ryc08]	SB	2.4e3	3e3	60	-	40	-	51	90 nm	1	40	4.1
[Bei09]	SB	2.442e3	3.256e3	25	-	34	-	-	0.13 μm	1.3	26	12.7
[Ryc10]	CN	2.44e3	6.1e3	80	43	41	-	-	40 nm	1.1	52.8	3.6
[Kol10]	FT	900	1e3	9	-	56	-	-	65 nm	1.2	80	8.6
[Lu10]	CN	200	800	10	70	68.4	70	73.5	0.18 μm	1.8	160	3.7
[Ash11b]	SB	2.4e3	3.2e3	25	44	40	-	51	0.13 μm	1.2	19	4.7
[Ash11a]	CN	900	3.6e3	28	53	50	-	52	0.13 μm	1.2	15	1.0
[Cho11]	**FT**	**225**	**100**	**4**	**57.5**	**55**	**55.5**	**61.5**	**65 nm**	**1**	**13**	**3.5**

[a]Here, CN denotes a conventional bandpass $\Delta\Sigma$ modulator, SB denotes a subsampling $\Delta\Sigma$ modulator, and FT denotes a frequency-translating $\Delta\Sigma$ modulator.

The bandpass $\Delta\Sigma$ modulators listed in Table 8.2 are compared in terms of their energy efficiency (i.e., energy/conversion step), which can be quantified using the following standard figure of merit (FOM):

$$\text{FOM} = \frac{P_{\text{total}}}{2^{\text{ENOB}} \cdot 2f_B} \qquad (\text{pJ/step}) \tag{8.1}$$

Here, P_{total} is the power consumption of the $\Delta\Sigma$ modulator, ENOB is its effective number of bits, as defined in Equation (2.20), and f_B is its signal bandwidth.

The comparison in Table 8.2 demonstrates that the single-path frequency-translating $\Delta\Sigma$ modulator presented in this thesis achieves a FOM that is competitive with state-of-the-art CMOS bandpass $\Delta\Sigma$ modulators.

Chapter 9

Conclusion

THIS CHAPTER reviews the main research contributions of this thesis, and summarizes the measured results of the experimental prototype. In addition, it suggests a number of directions for future research.

9.1 Thesis Summary

This thesis examined delta-sigma ($\Delta\Sigma$) modulator architectures for direct analog-to-digital conversion of high-frequency bandpass signals, without prior downconversion to baseband. It focused on a particular type of $\Delta\Sigma$ modulator that uses mixing inside its $\Delta\Sigma$ feedback loop to convert high-frequency analog signals into corresponding low-frequency digital signals. This architecture is referred to as the frequency-translating $\Delta\Sigma$ modulator.

As a starting point, this thesis examined the effect of timing errors on the resolution of a continuous-time $\Delta\Sigma$ modulator. It developed a modeling technique to rapidly simulate the effect of timing errors introduced in the feedback path of a continuous-time $\Delta\Sigma$ modulator, which can limit the performance. The proposed technique demonstrated a considerable speed advantage over direct simulation methods, and is therefore particularly useful for evaluating the performance loss caused by clock jitter. The speed advantage of the proposed technique was applied simulate a variety of rectangular DAC pulses, and to analyse their impact on the clock-jitter sensitivity of various continuous-time $\Delta\Sigma$ modulator architectures.

This thesis then examined an existing type of frequency-translating $\Delta\Sigma$ modulators that is based on quadrature, or *image-reject* mixing. It presented a complete synthesis procedure for the image-reject frequency-translating $\Delta\Sigma$ modulator, and developed a set of system-level constraints that must be satisfied to achieve the synthesis. It then examined the performance limitations of the image-reject architecture, and demonstrated that in-phase and quadrature path mismatch, introduced by phase, delay, and amplitude errors, can significantly limit the resolution. As a solution to the problem of path mismatch, this thesis proposed a novel type of frequency-translating $\Delta\Sigma$ modulators that is based on *single-path* mixing.

A synthesis procedure was developed for the proposed single-path frequency-translating $\Delta\Sigma$ modulator, including its required system-level constraints. Additional design techniques were then developed to improve the resolution of the proposed architecture, and decrease its sensitivity to timing errors. The accuracy of the synthesis procedure, and the validity of the presented design techniques were demonstrated using an experimental single-path frequency translating $\Delta\Sigma$ modulator. Both the system architecture and circuit implementation of this experimental prototype were described in detail.

The experimental $\Delta\Sigma$ modulator was implemented in a standard 65-nm CMOS process, and operates from a 1-V power supply. It was designed to digitize a 4 MHz input-signal band that is centred at 225 MHz, and further downconverts this signal band to a centre frequency of 25 MHz inside its $\Delta\Sigma$ loop. The experimental prototype achieves a peak SNR of 55.5 dB, a peak SNDR of 55.0 dB, and a dynamic range of 57.5 dB, and has a power consumption of 13 mW. The measured performance of the experimental $\Delta\Sigma$ modulator was demonstrated to be competitive with state-of-the-art bandpass $\Delta\Sigma$ modulators.

The research work presented in this thesis resulted in the following publications:

1. P. M. Chopp and A. A. Hamoui, "A 1V 13mW frequency-translating $\Delta\Sigma$ ADC with 55dB SNDR for a 4MHz band at 225MHz," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2011.

2. P. M. Chopp and A. A. Hamoui, "Design constraints for image-reject frequency-translating $\Delta\Sigma$ modulators," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 12, pp. 896–900, Dec. 2009.

3. P. M. Chopp and A. A. Hamoui, "Analysis of clock-jitter effects in continuous-time $\Delta\Sigma$ modulators using discrete-time models," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 6, pp. 1134–1145, Jun. 2009.

4. P. M. Chopp and A. A. Hamoui, "Discrete-time modeling of clock jitter in continuous-time $\Delta\Sigma$ modulators," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 497–500.

9.2 Suggestions for Future Research

This thesis proposed the *single-path* frequency-translating $\Delta\Sigma$ modulator, and demonstrated its performance using an experimental prototype. It also developed a technique to model the effect of timing errors introduced in the feedback DAC of a continuous-time $\Delta\Sigma$ modulator. These contributions could potentially be extended as follows:

- The modeling technique proposed in Chapter 3 only considered the effect of time-delay errors in *rectangular* DAC pulses. A rectangular pulse was selected because it is simple to implement, widely-used in the literature, and has high sensitivity to clock jitter. The developed modeling technique could be further extended to a variety of different pulse shapes (e.g., raised cosine, exponential) in order to evaluate their relative effectiveness in reducing the jitter sensitivity of a continuous-time $\Delta\Sigma$ modulator.

- The primary motivation for the frequency-translating $\Delta\Sigma$ modulator is that it directly and efficiently digitizes high-frequency bandpass signals. Therefore, a natural extension to the research presented in this thesis is to increase the input centre frequency of the experimental $\Delta\Sigma$ modulator. It is not practical to increase the ratio of the input centre frequency to the output centre frequency, since this reduces the effective quality factor of the outer-loop filter and affects the noise-shaping performance. However, the centre frequency of the inner-loop filter could be increased, and the input centre frequency of the experimental $\Delta\Sigma$ modulator then scaled proportionally.

  The inner-loop filter of the experimental $\Delta\Sigma$ modulator is centred around 25 MHz, and is designed using active-RC resonators. In the literature, active-RC implementations of bandpass $\Delta\Sigma$ modulators have achieved centre frequencies as high as 200 MHz [Lu10], by using multi-stage amplifiers and linearity enhancement. The centre frequency of the inner-loop filter could be increased using similar circuit techniques.

- An additional advantage of increasing the input centre frequency of the experimental $\Delta\Sigma$ modulator is that it facilitates an on-chip implementation for the inductors of the LC resonator. This eliminates the parasitics introduced by the bond wires, the package leads, and the PCB traces, and therefore improves the accuracy of the centre frequency of the LC resonator, and that of its associated loop filter coefficient.

- At the circuit level, the noise shaping performance of the experimental $\Delta\Sigma$ modulator could be further improved by increasing the quality factor (Q) of its LC resonator using Q-enhancement techniques. The LC resonator was designed without Q-enhancement in order to simplify its implementation and tuning. The linearity of the experimental $\Delta\Sigma$ modulator could be improved by reducing the distortion that is introduced by its first active-RC resonator, which limits the performance. This can be achieved by increasing the gain of the associated amplifiers using standard techniques.

Appendix A

Derivations

THIS APPENDIX provides an example of the impulse-invariant transform, as well as an extended derivation of the error-mapping terms developed in Section 3.3.

A.1 Example of the Impulse-Invariant Transform

This section provides an example of the impulse-invariant transform. It demonstrates how to derive a continuous-time loop transfer function $H_{\mathrm{L}}(s)$ that achieves the same noise-shaping performance as a prototype discrete-time loop transfer function $H'_{\mathrm{L}}(z)$. The impulse-invariant transform was defined in Equation (3.3) as

$$H_{\mathrm{L}}(s) \;=\; \underset{z \to s}{\mathrm{IIT}} \Big\{ H'_{\mathrm{L}}(z) \Big\} \cdot \frac{1}{H_{\mathrm{DAC}}(s)} \tag{A.1}$$

The objective of this example is to develop a loop transfer function for a continuous-time $\Delta\Sigma$ modulator that achieves 1st-order highpass shaping of quantization errors. The required noise-shaping characteristic can be achieved using an NTF of

$$\mathrm{NTF}(z) \;=\; 1 - z^{-1} \tag{A.2}$$

which corresponds to a discrete-time loop transfer function of

$$H'_{\mathrm{L}}(z) \;=\; \frac{1}{\mathrm{NTF}(z)} - 1 \;=\; \frac{z^{-1}}{1 - z^{-1}} \tag{A.3}$$

This example first converts a continuous-time loop transfer function $H_{\mathrm{L}}(s)$, which has the required order and *general* coefficients, into an equivalent discrete-time transfer function. It then solves for the coefficients by comparing the result with Equation (A.3).

This example assumes that the feedback DAC of the continuous-time $\Delta\Sigma$ modulator has a return-to-zero (RZ) pulse with rising and falling edges at $0.5\,T_\mathrm{S}$ and T_S, respectively. The transfer function of this rectangular DAC is equal to

$$H_\mathrm{DAC}(s) \;=\; \frac{1}{s}\Big(\mathrm{e}^{-s0.5T_\mathrm{S}} - \mathrm{e}^{-sT_\mathrm{S}}\Big) \tag{A.4}$$

where T_S denotes the sampling period.

In order to achieve the NTF that is specified in Equation (A.2), the loop transfer function of the continuous-time $\Delta\Sigma$ modulator must have a general form of

$$H_\mathrm{L}(s) \;=\; \frac{b_1}{sT_\mathrm{S}} \tag{A.5}$$

The combined transfer function of the continuous-time loop filter and the feedback DAC is then expressed as

$$H'_\mathrm{L}(s) \;=\; H_\mathrm{L}(s)H_\mathrm{DAC}(s) \;=\; \frac{b_1}{s^2T_\mathrm{S}}\Big(\mathrm{e}^{-s0.5T_\mathrm{S}} - \mathrm{e}^{-sT_\mathrm{S}}\Big) \tag{A.6}$$

where the objective is to solve for coefficient b_1.

The expression in Equation (A.6) can be converted into the time domain using an inverse Laplace transform. This operation yields a loop response of

$$h'_\mathrm{L}(t) \;=\; \mathcal{L}^{-1}\big\{H'_\mathrm{L}(s)\big\} \;=\; \frac{b_1}{T_\mathrm{S}}\,(t - T_\mathrm{S}/2)\,u(t - T_\mathrm{S}/2) - \frac{b_1}{T_\mathrm{S}}\,(t - T_\mathrm{S})\,u(t - T_\mathrm{S}) \tag{A.7}$$

The corresponding sampled loop response of the continuous-time $\Delta\Sigma$ modulator can then be derived by setting $t = nT_\mathrm{S}$ in Equation (A.7). This substitution results in

$$h'_\mathrm{L}(n) \;=\; h'_\mathrm{L}(t)\big|_{t\,=\,nT_\mathrm{S}} \;=\; b_1(n - 1/2)\,u(n-1) - b_1(n-1)\,u(n-1) \tag{A.8}$$

The expression in Equation (A.8) is finally processed using the z-transform, which yields a discrete-time loop transfer function of

$$H'_\mathrm{L}(z) \;=\; \mathcal{Z}\big\{\,h'_\mathrm{L}(n)\,\big\} \;=\; \frac{b_1}{2}\frac{z^{-1}}{1 - z^{-1}} \tag{A.9}$$

Accordingly, for correspondence with Equation (A.3), the coefficient (b_1) of the loop transfer function of the continuous-time $\Delta\Sigma$ modulator must be set to 2.

A.2 Extended Derivation of the Error-Mapping Terms

This section provides an extended derivation of the 2nd-order error-mapping term, for which a simple derivation was presented in Section 3.3. This extended derivation demonstrates how continuous-time delay errors, in the pulses of the feedback DAC, can be shifted to the input of the loop response. In this way, it shows how the error-mapping terms given in Tables 3.1 and 3.2 can be derived without processing these potentially time-varying delay errors using the Laplace and z-transforms.

In the same way as Section 3.3.1, this extended derivation starts with the 2nd-order term of a prototype discrete-time loop transfer function

$$H'_{\mathrm{L},\,2}(z) \;=\; \frac{c_2}{(z-1)^2} \tag{A.10}$$

Using α and β to represent the nominal start and end times of the DAC pulse, as shown in Figure 3.7, $H'_{\mathrm{L},\,2}(z)$ can be transformed into an equivalent continuous-time filter by way of a $z \to s$ impulse-invariant transform. This transform results in

$$H_{\mathrm{L},\,2}(s) \;=\; \underset{z\,\to\,s}{\mathrm{IIT}}\Big\{H'_{\mathrm{L},\,2}(z)\Big\} \cdot \frac{1}{H_{\mathrm{DAC}}(s)} \;=\; \frac{b_1(sT_{\mathrm{S}}) + b_2}{(sT_{\mathrm{S}})^2} \tag{A.11}$$

where

$$\begin{aligned} b_1 \;&=\; \frac{1}{2}\frac{c_2\,(\alpha+\beta-2)}{\beta-\alpha} \\ b_2 \;&=\; \frac{c_2}{\beta-\alpha} \end{aligned}$$

and $H_{\mathrm{DAC}}(s)$ is the transfer function of the feedback DAC. For a rectangular pulse

$$H_{\mathrm{DAC}}(s) \;=\; \frac{1}{s}\Big(\mathrm{e}^{-s\alpha T_{\mathrm{S}}} - \mathrm{e}^{-s\beta T_{\mathrm{S}}}\Big) \tag{A.12}$$

where α and β are normalized with respect to the sampling period T_{S}.

The combined transfer function of the continuous-time loop filter and the feedback DAC will be denoted here as

$$H'_{\mathrm{L},\,2}(s) \;=\; H_{\mathrm{L},\,2}(s)H_{\mathrm{DAC}}(s) \tag{A.13}$$

In order to demonstrate how continuous-time delay errors can be mapped into coefficient errors in an equivalent z-domain expression, $H'_{\mathrm{L},\,2}(s)$ must first be transformed into the time domain using an inverse Laplace transform, where

$$h'_{\mathrm{L},\,2}(t) \;=\; \mathcal{L}^{-1}\Big\{H'_{\mathrm{L},\,2}(s)\Big\} \;=\; \bigg[\big(t-\alpha T_{\mathrm{S}}\big)\frac{b_1}{T_{\mathrm{S}}} + \big(t-\alpha T_{\mathrm{S}}\big)^2\frac{b_2}{2T_{\mathrm{S}}^2}\bigg]u\big(t-\alpha T_{\mathrm{S}}\big) \\ +\; \bigg[\big(t-\beta T_{\mathrm{S}}\big)\frac{b_1}{T_{\mathrm{S}}} + \big(t-\beta T_{\mathrm{S}}\big)^2\frac{b_2}{2T_{\mathrm{S}}^2}\bigg]u\big(t-\beta T_{\mathrm{S}}\big) \tag{A.14}$$

and $u(t)$ represents the unit step function.

The remaining steps of this derivation differ depending on whether the feedback DAC is designed with: an RZ pulse, where the α and β pulse edges both occur in the same cycle of the sampling clock, or an NRZ pulse, where the α edge occurs in the clock cycle prior to the one that contains the β edge. Each case is discussed separately below.

RZ Pulse

The edges of an RZ pulse are generally defined so that $0 \le \alpha \le 1$ and $0 \le \beta \le 1$. Therefore, when $h'_{\mathrm{L},\,2}(t)$ in Equation (A.14) is sampled with a period of T_{S}, $u(t-\alpha T_{\mathrm{S}})$ and $u(t-\beta T_{\mathrm{S}})$ both reduce to $u(n-1)$. In this case, the sampled impulse response is equal to

$$h'_{\mathrm{L},\,2\mathrm{RZ}}(n) \;=\; h'_{\mathrm{L},\,2}(t)\big|_{t\,=\,nT_{\mathrm{S}}} \;=\; \bigg[(n-\alpha)\,b_1 + (n-\alpha)^2\frac{b_2}{2}\bigg]u(n-1) \\ +\; \bigg[(n-\beta)\,b_1 + (n-\beta)^2\frac{b_2}{2}\bigg]u(n-1) \tag{A.15}$$

In order to the model the effect of time-delay errors, the nominal edge timing parameters, α and β, in Equation (A.15) are replaced by non-ideal timing parameters $\widehat{\alpha}(m)$ and $\widehat{\beta}(m)$, defined in Equation (3.6). The resulting *time-varying* impulse response can be expressed as

$$\widehat{h}'_{\mathrm{L},\,2\mathrm{RZ}}(n,m) \;=\; h'_{\mathrm{L},\,2\mathrm{RZ}}(d) + \big[\,h'_{\mathrm{L},\,2\mathrm{RZ}_\beta}(d)\,\Delta\beta(m) - h'_{\mathrm{L},\,2\mathrm{RZ}_\alpha}(d)\,\Delta\alpha(m)\,\big] \tag{A.16}$$

where $d = n - m$ and

$$h'_{\mathrm{L},\,2\mathrm{RZ}_\alpha}(d) \;=\; \big[b_1 + (d-1)\,b_2 + (1-\alpha)\,b_2\big]u(d-1)$$
$$h'_{\mathrm{L},\,2\mathrm{RZ}_\beta}(d) \;=\; \big[b_1 + (d-1)\,b_2 + (1-\beta)\,b_2\big]u(d-1)$$

Here, d is the delay between time m when the input sample is applied, and time n when the output sample is observed. Note that the second-order error terms, $\Delta\alpha(m)^2$ and $\Delta\beta(m)^2$, are not included in Equation (A.16), since $|\Delta\alpha(m)| < 1$ and $|\Delta\beta(m)| < 1$, and therefore the 1st-order error terms, $\Delta\alpha(m)$ and $\Delta\beta(m)$, are dominant.

The impulse responses $h'_{\mathrm{L,\,2RZ}}(d)$, $h'_{\mathrm{L,\,2RZ}_\alpha}(d)$ and $h'_{\mathrm{L,\,2RZ}_\beta}(d)$ in (A.15) and (A.16) are all individually time-invariant. Therefore, their z-transforms can be directly evaluated as

$$H'_{\mathrm{L,\,2RZ}}(z) \;=\; \frac{c_2}{(z-1)^2} \tag{A.17}$$

$$H'_{\mathrm{L,\,2RZ}_\alpha}(z) \;=\; \frac{c_2}{\beta-\alpha}\frac{1}{(z-1)^2} + \frac{c_2}{2}\frac{1}{(z-1)} \tag{A.18}$$

$$H'_{\mathrm{L,\,2RZ}_\beta}(z) \;=\; \frac{c_2}{\beta-\alpha}\frac{1}{(z-1)^2} - \frac{c_2}{2}\frac{1}{(z-1)} \tag{A.19}$$

In Equation (A.16), the timing errors $\Delta\alpha(m)$ and $\Delta\beta(m)$ depend only on time m, when the input sample is applied. This models the behaviour of a continuous-time $\Delta\Sigma$ modulator, where the input of the loop filter during clock cycle m, equivalent to $y(m)$ in Figure 3.1(a), is only affected by the timing errors, $\Delta\alpha(m)$ and $\Delta\beta(m)$, that are introduced during clock cycle m. Since $\Delta\alpha(m)$ and $\Delta\beta(m)$ only depend on time instant m when the input is applied, they can be shifted from the impulse response, $\widehat{h}'_{\mathrm{L,\,2RZ}}(n,m)$, to the input, $y(m)$.

In this way, the response of $\widehat{h}'_{\mathrm{L,\,2RZ}}(n,m)$ to $y(m)$ can be expressed as

$$\widehat{v}_{\mathrm{2RZ}}(n) \;=\; -\sum_{m=0}^{n} \widehat{h}'_{\mathrm{L,\,2RZ}}(n,m)\, y(m) \tag{A.20}$$

The output of Equation (A.20) can be split into

$$\widehat{v}_{\mathrm{2RZ}}(n) \;=\; \widehat{v}_{\mathrm{2RZ}}(n) + \left[\, \widehat{v}_{\mathrm{2RZ}_\beta}(n) - \widehat{v}_{\mathrm{2RZ}_\alpha}(n) \,\right] \tag{A.21}$$

where

$$\widehat{v}_{\mathrm{2RZ}}(n) \;=\; -\sum_{m=0}^{n} h'_{\mathrm{L,\,2RZ}}(n-m)\, y(m) \tag{A.22}$$

$$\widehat{v}_{\mathrm{2RZ}_\alpha}(n) \;=\; -\sum_{m=0}^{n} h'_{\mathrm{L,\,2RZ}_\alpha}(n-m)\, \Delta\alpha(m)\, y(m) \tag{A.23}$$

$$\widehat{v}_{\mathrm{2RZ}_\beta}(n) \;=\; -\sum_{m=0}^{n} h'_{\mathrm{L,\,2RZ}_\beta}(n-m)\, \Delta\beta(m)\, y(m) \tag{A.24}$$

Here, $y(m)$, $\Delta\alpha(m)y(m)$, and $\Delta\beta(m)y(m)$ can be interpreted as the inputs of loop filter components $H'_{\mathrm{L},\,2\mathrm{RZ}}(z)$, $H'_{\mathrm{L},\,2\mathrm{RZ}_\alpha}(z)$, and $H'_{\mathrm{L},\,2\mathrm{RZ}_\beta}(z)$ in Equations (A.17) – (A.19). Therefore, error sequences $\Delta\alpha(m)$ and $\Delta\beta(m)$ only act as scaling factors on the input of the loop filter and can be accurately modeled as errors in the coefficients of an equivalent discrete-time $\Delta\Sigma$ modulator. Note that the 2nd-order error-mapping term derived in Section 3.3.1 can be split into the form shown in Equations (A.17)–(A.19).

NRZ Pulse

The edges of an NRZ pulse are generally defined so that $0 \leq \alpha \leq 1$ and $1 \leq \beta \leq 2$. Therefore, when $h'_{\mathrm{L},\,2}(t)$ in Equation (A.14) is sampled with a period of T_S, $u(t-\alpha T_\mathrm{S})$ and $u(t-\beta T_\mathrm{S})$ reduce to $u(n-1)$ and $u(n-2)$. In this case, the sampled impulse response is equal to

$$\begin{aligned} h'_{\mathrm{L},\,2\mathrm{NRZ}}(n) \;=\; h'_{\mathrm{L},\,2}(t)\big|_{t\,=\,nT_\mathrm{S}} \;&=\; \left[(n-\alpha)\,b_1 + (n-\alpha)^2\frac{b_2}{2}\right]u(n-1) \\ &+\; \left[(n-\beta)\,b_1 + (n-\beta)^2\frac{b_2}{2}\right]u(n-2) \end{aligned} \tag{A.25}$$

In order to the model the effect of time-delay errors, the nominal edge timing parameters, α and β, in Equation (A.25) are replaced by non-ideal timing parameters $\widehat{\alpha}(m)$ and $\widehat{\beta}(m)$, defined in Equation (3.6). The resulting *time-varying* impulse response can be expressed as

$$\widehat{h}'_{\mathrm{L},\,2\mathrm{NRZ}}(n,m) \;=\; h_2(d) + \left[\, h_{2\mathrm{NRZ}_\beta}(d)\,\Delta\beta(m) - h_{2\mathrm{NRZ}_\alpha}(d)\,\Delta\alpha(m)\,\right] \tag{A.26}$$

where $d = n - m$ and

$$\begin{aligned} h'_{\mathrm{L},\,2\mathrm{NRZ}_\alpha}(d) \;&=\; \big[b_1 + (d-1)\,b_2 + (1-\alpha)\,b_2\big]u(d-1) \\ h'_{\mathrm{L},\,2\mathrm{NRZ}_\beta}(d) \;&=\; \big[b_1 + (d-2)\,b_2 + (2-\beta)\,b_2\big]u(d-2) \end{aligned}$$

Here, d is the delay between time m when the input sample is applied, and time n when the output sample is observed. Note that the second-order error terms, $\Delta\alpha(m)^2$ and $\Delta\beta(m)^2$, are not included in Equation (A.26), since $|\Delta\alpha(m)| < 1$ and $|\Delta\beta(m)| < 1$, and therefore the 1st-order error terms, $\Delta\alpha(m)$ and $\Delta\beta(m)$, are dominant.

In Equation (A.26), the z-transform of $h'_{\mathrm{L,\,2NRZ}}(d)$ is equal to $H'_{\mathrm{L,\,2RZ}}(z)$ in (A.17), after it is compensated for excess loop delay, the z-transform of $h'_{\mathrm{L,\,2NRZ}_\alpha}(d)$ is equal to $H'_{\mathrm{L,\,2RZ}_\alpha}(z)$ in (A.18), and the z-transform of $h'_{\mathrm{L,\,2NRZ}_\beta}(d)$ is equal to

$$H'_{\mathrm{L,\,2NRZ}_\beta}(z) \;=\; \frac{c_2}{\beta-\alpha}\frac{z^{-1}}{(z-1)^2} + \frac{c_2}{2}\frac{z^{-1}}{(z-1)} \tag{A.27}$$

where $\beta = 1+\alpha$. The additional delay in $H'_{\mathrm{L,\,2NRZ}_\beta}(z)$, as compared to $H'_{\mathrm{L,\,2RZ}_\beta}(z)$ in (A.19), is due to the fact that the input of $H'_{\mathrm{L,\,2NRZ}_\beta}(z)$ is generated in the previous clock cycle. The difference in the signs of the 1st-order terms of $H'_{\mathrm{L,\,2NRZ}_\beta}(z)$ and $H'_{\mathrm{L,\,2RZ}_\beta}(z)$ does not have a significant effect on the results of the modeling technique, since the errors introduced by this term receive 1st-order highpass shaping (Section 3.5).

The remainder of the derivation for the case of an NRZ pulse matches the derivation for an RZ pulse. Once again, error sequences $\Delta\alpha(m)$ and $\Delta\beta(m)$ only act as scaling factors on the input of the loop filter, and can therefore be represented as gain errors in the coefficients of an equivalent discrete-time $\Delta\Sigma$ modulator.

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