Silicon Photonic Switches for Single Mode and Multimode Networks

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Abstract

The advancement of silicon photonics (SiPh) technology in communication systems has been rising rapidly day by day. Silicon photonics, compatible with complementary metal-oxide-semiconductor (CMOS), is one of the most promising technologies that provides large capacity and high integration density with an established fabrication process. The mature and low-cost silicon photonic technology has all the potentials to develop high-performance photonic switches required for advanced datacenter networks. This thesis is a theoretical and experimental demonstration of several silicon photonic switches featuring low loss, low crosstalk, low power consumption, and broadband applications.

We design and experimentally demonstrate scalable 2×2, 4×4, and 8×8 SiPh thermo-optic switches exhibiting low loss, low crosstalk, and low power consumption with a bit error rate (BER) below 10^{-10} for payload data transmission. For 8×8 switch, less than 3.13 dB insertion loss and approximately 20.5 dB crosstalk is measured over a bandwidth range of 25 nm with 5.2 pJ/bit power consumption. Using more optimized multimode interferometer (MMI) and waveguide crossing, an ultra-broadband 16×16 thermo-optic switch has also been designed and experimentally demonstrated using continuous wave (CW) and payload transmission (RF). This switch provides 100 nm of bandwidth, at most 8 dB in crosstalk, and less than 3.8 dB of insertion loss for the longest path. At 10 Gb/s, this energy-efficient switch consumes less than 7 pJ/bit.

Recently, mode division multiplexing (MDM) technology has attracted widespread

attention due to a new dimension of freedom to increase the data capacity by utilizing the spatial modes of waveguide using a single wavelength carrier. We proposed and experimentally demonstrated a novel design topology for scalable 3 × 3 and 4 × 4 mode insensitive multimode SiPh switching matrices for the first two quasi-transverse electric (TE) modes. At 1550 nm, the 3 × 3 switch exhibits approximately 2.6 dB and 3.3 dB insertion loss with a maximum crosstalk measured 10 dB and 8 dB for the longest channel over a bandwidth range of 40 nm for TE_0 and TE_1 mode respectively. For 4 × 4 switch, the insertion loss is approximately 2.7 dB and 3.6 dB for the longest channel at 1550 nm with a corresponding crosstalk of at most 8 dB over a bandwidth range of 40 nm. Clear open eyes are observed for all the simultaneous multimode transmission with 2 and 2.5 pJ/bit power consumption for 3 × 3 and 4 × 4 switch, respectively.

Combining the silicon photonics (SiPh) and indium phosphide (InP) technologies, we propose a lossless hybrid switch matrix with distributed semiconductor optical amplifier (SOA) based gain capable of transmitting data with near-zero loss and low crosstalk over a large switching matrix. In hybrid SiPh/InP switches, the SOA gain compensates for the SiPh switch loss at the cost of amplified spontaneous emission (ASE) noise but mitigated by bandpass optical filters. Lower insertion loss from the SiPh switch requires less gain from the SOAs leading to less optical signal-to-noise ratio (OSNR) degradation. Experimentally validated building blocks confirm scalability up to 64 × 64 in the SiPh-InP hybrid platform.

In summary, this thesis is an intensive study of some state-of-the-art design approaches

and their experimental validations. Both single and multimode switches are designed and experimentally investigated for continuous wave and payload data transmission. The low loss, low crosstalk, and low power consumption with a good signal-to-noise ratio (SNR) validate the scalability of these switches in datacenter networks.

Abrégé

Les avancées technologiques de photonique sur silicium (SiPh) dans les systèmes de communication accélèrent à chaque jour. La photonique sur silicium, compatible avec le procédé d'oxyde métallique-semi-conducteur complémentaire (CMOS), est une des technologies les plus prometteuses, offrant une grande capacité de production ainsi qu'une intégration serrée avec les processus de fabrication établis. La technologie mature et à faible-coût de photonique sur silicium possède tout le potentiel nécessaire pour développer les commutateurs photoniques à haute performances nécessaires pour les réseaux avancés de centres de données. Cette thèse est une démonstration théorique et expérimentale de plusieurs commutateurs à photonique sur silicium démontrant de faibles pertes, peu de diaphonie, une faible consommation de puissance ainsi que de larges bandes passantes.

Nous faisons la conception ainsi que la démonstration expérimentale de commutateurs SiPh thermo-optiques adaptatifs 2×2, 4×4 et 8×8 démontrant de faibles pertes, peu de diaphonie ainsi qu'une faible consommation de puissance avec un ratio d'erreur de bit (BER) sous 10^{-10} pour un transfert de donnée. Les commutateurs 8×8 montrent moins de 3.13 dB de perte d'insertion ainsi qu'environ 20.5 dB de diaphonie sur une largeur de bande de 25 nm avec une consommation de puissance de 5.2pJ/bit. En utilisant un interféromètre multimode (MMI) plus optimisé ainsi qu'un croisement de guide d'onde, un commutateur thermo-optique 16×16 à très large bande a aussi été conçu et démontré expérimentalement à l'aide d'un laser et d'une transmission de données. Ce commutateur offre 100 nm de largeur

de bande, au plus 8 dB de diaphonie et moins de 3.8 dB de perte d'insertion pour les plus longs canaux. À 10 Gb/s, ce commutateur efficace consomme moins de 7 pJ/bit.

Récemment, la technologie de division et multiplexage de modes (MDM) a attirée beaucoup d'attention grâce à sa capacité d'utiliser un nouveau degré de liberté pour augmenter la capacité de transmission en utilisant les modes spatiaux de guides d'onde en utilisant une seule longueur d'onde. Nous avons proposé et démontré expérimentalement un nouveau concept topologique pour une matrice de commutation multimode SiPh à 3 × 3 et 4 × 4 modes pour les deux premiers modes quasi-transverse électrique (TE). À 1550 nm, le commutateur 3 × 3 démontre approximativement 2.6 dB et 3.3 dB de perte d'insertion avec une diaphonie maximale de 10 dB et 8 dB pour le canal le plus long sur une largeur de bande de 40 nm pour les modes TE_0 et TE_1, respectivement. Pour un commutateur 4 × 4, la perte d'insertion est d'environ 2.7 dB et 3.6 dB pour le canal le plus long à 1550 nm avec une diaphonie correspondante d'au plus 8 dB sur une largeur de bande de 40 nm. On observe un diagramme de l'oeil ouvert pour toutes les transmissions multimodes simultanées avec une consommation de puissance de 2 et 2.5 pJ/bit pour le commutateur 3 × 3 et 4 × 4, respectivement.

En combinant les technologies de photonique sur silicium (SiPh) et de phosphure d'indium (InP), nous proposons une matrice commutative hybride sans pertes avec un gain distribué amplificateur optique semi-conducteur (SOA) capable de transmettre des données avec une perte presque nulle ainsi qu'une faible diaphonie sur une grande matrice

commutative. Avec les commutateurs hybrides SiPh/InP, le gain du SOA compense pour les perte du commutateur SiPh au coût de bruit d'émission amplifiée spontanée (ASE), mais limité par la bande passante des filtres optiques. La faible perte d'insertion des commutateurs SiPh nécessite moins de gain des SOAs, menant à moins de dégradation du rapport signal/bruit optique (OSNR). La validation expérimentale des différentes composantes confirme l'adaptabilité jusqu'à 64×64 de la plateforme SiPh/InP.

En résumé, cette thèse est une étude en profondeur de certains des concepts à la fine pointe de la technologie ainsi que de leur preuve expérimentale. Les commutateurs à simple mode ainsi qu'à multi-mode sont conçues et examinées expérimentalement. La faible perte, faible diaphonie et faible consommation de puissance jumelée avec un bon rapport signal sur bruit (SNR) valide l'adaptabilité de ces commutateurs pour le réseaux de centres de données.

Acknowledgements

First and foremost, I want to express my gratitude to Almighty God for giving me the continued strength and patience throughout the journey of M.Sc studies. Next, I cordially thank my thesis supervisor, Prof. Odile Liboiron-Ladouceur, for giving me the opportunity to be a part of her research team. Her guidance, advice, and continuous support inspire me to improve my knowledge and research skill to a higher level. Her unique way of approaching a technical problem in a systematic and appropriate manner helps me overcome all the obstacles and produce high-quality research contributions. I like to acknowledge Prof. David Plant and others involved with "McGill Photonic Systems Group" to share their equipment with me for several experiments.

Heartfelt thanks to my colleagues working with me as a part of "Photonic Datacom team." Together we learnt and explored new technologies to gain enormous research experiences. Special thanks goes to Dr. Hassan Rahbardar Mojaver, Guowu Zhang, and Rubana Bahar Priti, who always encourage me and share their research experiences. I like to show my appreciation to my friends: Samiul Alam, Imtiaz Alamgir, and Hosne Mobarok Shamim, for their continuous support throughout my entire journey.

Finally, I want to dedicate all of my achievements to my lovely family. Their unconditional love and continuous motivation make my journey much easy and enjoyable.

Contents

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List of Acronyms

BER	Bit Error Rate.
BOX	Buried OXide.
CLK	Clock.
CMOS	Complementary Metal Oxide Semiconductor.
CVD	Chemical Vapour Deposition.
CW	Continuous Wave.
DC	Directional Coupler.
DCA	Digital Communication Analyzer.
deMUX	Demultiplexer.
DUT	Device Under Test.
EBL	Electron Beam Lithography.
ED	Error Detector.
EDFA	Erbium Doped Fiber Amplifier.
EME	EigenMode Expansion.

EO	Electro-Optic.
ER	Extinction Ratio.
FA	Fiber Array.
FSR	Free Spectral Range.
GC	Grating Coupler.
IL	Insertion Loss.
InP	Indium Phosphide.
MDM	Mode-Division Multiplexing.
MMF	MultiMode Fiber.
MMI	MultiMode Interference.
MRR	Micro-Ring Resonator.
MUX	Multiplexer.
MZI	Mach-Zehnder Interferometer.
NRZ	Non-Return-to-Zero.
OSNR	Optical Signal-to-Noise Ratio.
PC	Polarization Controller.
PD	Photo Detector.
PIC	Photonic Integrated Circuit.
PPG	Pulse Pattern Generator.
PRBS	Pseudo Random Bit Sequence.

PS	Phase Shifter.
RIE	Reactive Ion Etching.
SiN	Silicon Nitride.
SiPh	Silicon Photonic.
SMF	Single Mode Fiber.
SNR	Signal-to-Noise Ratio.
SOA	Semiconductor Optical Amplifier.
SOI	Silicon-On-Insulator.
SWG	Sub-Wavelength Grating.
TE	Transverse Electric.
TiW	Titanium-Tungsten.
TO	Thermo-Optic.
TOC	Thermo-Optic Coefficient.
VOA	Variable Optical Attenuator.
WDM	Wavelength-Division Multiplexing.

Chapter 1

Introduction

Over the past few years, the rapid developments of our information based society rapidly increased the data volume. Well established electronic interconnects are serving the increasing demand mostly in datacenters as well as communication networks which are suffering from various constraints like low scalability, limited bandwidth, high thermal dissipation, etc [1]. Thus, the growing demand for network traffic needs enormous developments in future datacenters. The combination of photonic and electronic circuits in a single interconnect can make that revolutionary change enabling higher capacity and scalability with low latency and power consumption. Electronically controlled efficient and highly dense photonic interconnects are capable to meet all the requirements for increasing network traffic in future datacenters and high speed communication networks.

1.1 Optical Switches

The increasing demand for ultra-fast processing, storage and communication capacity in datacenters putting ever growing load on electronic switches due to limited bandwidth, port count and high power consumption [2]. Optical switching technology has all the potentials to replace the electronic switches in the application of short/long haul telecommunication networks, high speed computing, and datacenters as shown in figure 1.1.

Recently, various types of optical switching technology has been developed based on silicon photonics (SiPh) [4], indium phosphide (InP) [5], liquid crystal on silicon [6], piezo-electric beam-steering [7], silica planar-lightwave circuits (PLCs) [8] and micro-electro-mechanical systems (MEMS) [9] technology. Among them, silicon photonics is the most promising technology compatible with complementary metal-oxide-semiconductor (CMOS) technology. This well-established CMOS technology facilitate inexpensive fabrication process using silicon-on-insulator (SOI) wafer similar to advanced micro-electronic fabrication. As silicon photonic offers large-scale high-density integration with CMOS compatible electronics in the same wafer, researchers are utilizing this advantages by developing various silicon photonic passive and active devices such as switch, splitter/combiner, circulator, mode-mux/mode-demux, filter, modulator, detector and so on. Universities and many renowned companies like IBM [10], Intel [11], Luxtera [12] are investing in silicon photonic research to make the next generation telecommunication networks.

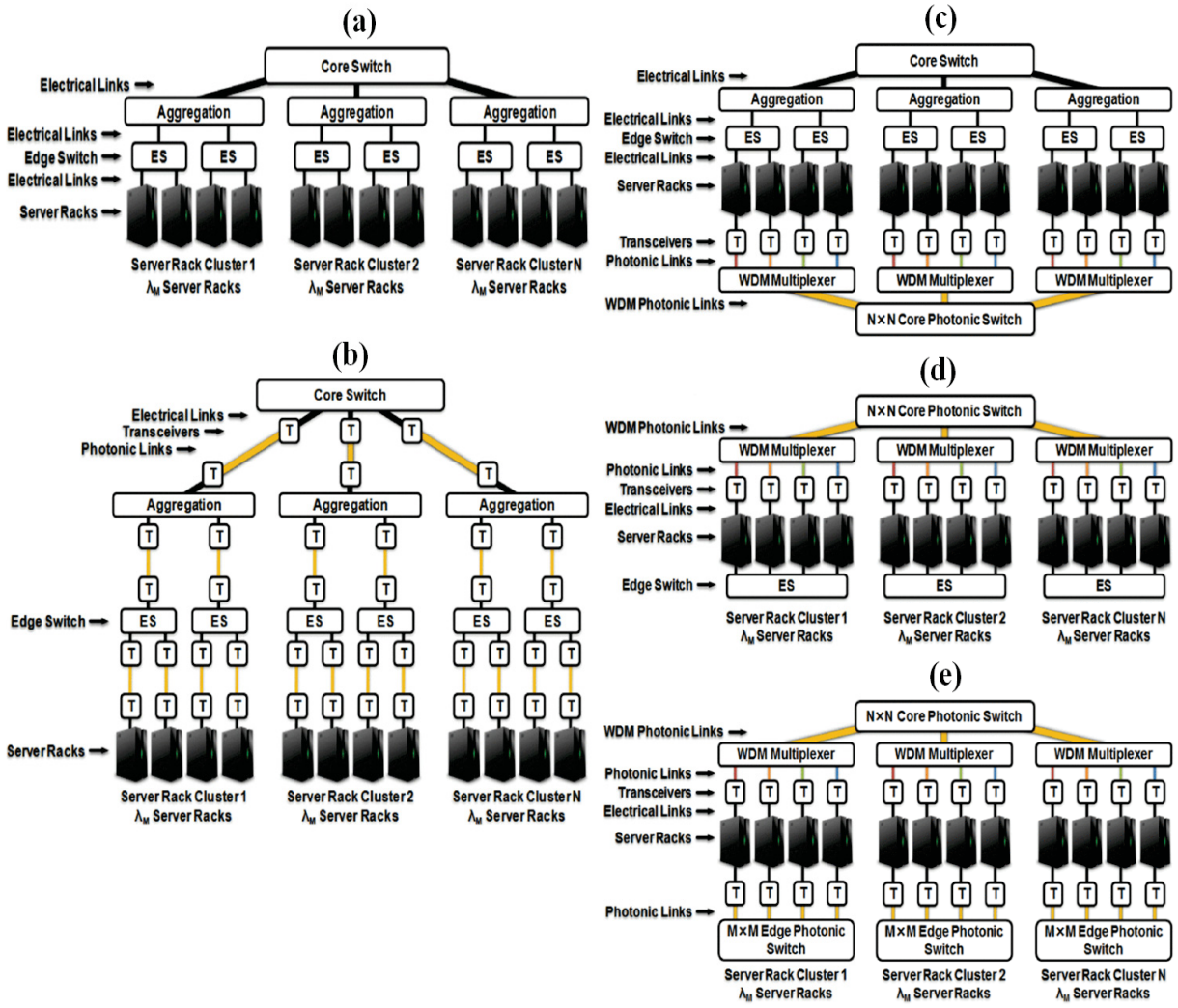

Figure 1.1: Interconnected datacenter networks; (a) typical electrically-interconnected data center network; (b) electrically-interconnected data center network with optical point-to-point links; (c) hybridly-interconnected data center network, routing short packets in the electrical domain, and long packets in the optical domain; (d) optically-interconnected data center network, densely aggregating server rack clusters using WDM, and routing all data between server rack clusters in the optical domain using a high-radix photonic core switch; (e) optically-interconnected data center network utilizing both core and edge photonic switches [3].

The high index contrast and low cost fabrication process make silicon photonic switches more suitable for datacenter applications. Compare to other technologies, silicon photonic switches provide low optical insertion loss, low power consumption, high bandwidth and large port count [13]. In this thesis, several types of single mode and multimode silicon photonic switches are demonstrated based on port count, insertion loss, and bandwidth. Large radix scalable hybrid switches in SiPh-InP platform are also reported.

1.2 Motivations

Over the past two decade, several types of optical switches have been studied intensively, such as SiPh single mode/multimode switches [4], liquid crystal switches [6], silicon nitride (SiN) switches [14], InP switches [5], MEMS actuated switches [9] etc. All of these switches have their own unique and remarkable characteristics which offer several advantages and disadvantages in switching. For instance, MEMS technology is suitable for large port count optical switches with low wavelength and polarization dependence loss, and low crosstalk while the PLC-based optical switches are also well-suited for large switching matrix with their insertion loss and easy coupling with optical fibers. However, both of them have some common limitations, such as large footprint, high power consumption, and low operation speed. Compared with these technologies, silicon photonic switches have more potentials due to small footprint, low insertion loss, high extinction ratio (ER), low manufacturing cost and large bandwidth. Lots of switching topologies and components already have been

developed in silicon photonics. However, more development is required to improve the switching components to achieve more satisfactory system performance both in short and long haul networks.

Interferometers are one of the most important and widely used elements in most of the silicon photonic switches. Mach-Zehnder interferometers (MZIs) and micro-ring resonators (MRRs) are the most common forms of interferometers where constructive and destructive interferences are used to switch the light from one port to another port. To actuate the state of an interferometer from constructive to destructive, or destructive to constructive interference of light, a phase shifter is necessary to use in silicon photonic switches.

In this thesis, Mach-Zehnder interferometer based large radix silicon photonic switches have been discussed in the application of low loss and broadband operation. One of the most significant contribution of thesis is the development of both single mode and multimode MZIs comprises by low loss and broadband multimode interferometers (MMIs) as splitter/combiner and power effective titanium tungsten (TiW) heater as phase shifter. Using the building block of SiPh MZI, distributed SOA gain block based scalable SiPh/InP large radix hybrid switch matrices has been reported. All the above switches were fabricated at Applied Nanotools Inc. (ANT) foundry based in Alberta, Canada.

1.3 Thesis Contributions

All the research works presented in this thesis including the concept, design, and experiment were conducted by the candidate, Alok Das though a continuous collaboration with Prof. Odile Liboiron-Ladouceur. Most of the contents of this thesis are published or submitted to publish in peer-reviewed journals or conference proceedings. The major contributions of this thesis including the details of related publications are presented below.

- Design, fabrication and experimental demonstration of a low loss 2 × 2 MMI used in a 2 × 2 SiPh MZI switch, which is used as the building block for 4 × 4 and 8 × 8 SiPh Banyan switches for low loss operation.

  This work was presented at 2020 IEEE Photonics Conference (IPC) by the candidate on 30^{rd} September, 2020. The design, simulation and experimental validation are conducted by the candidate. Dr. Hassan Rahbardar Mojaver and Guowu Zhang helped the candidate to measure the device and Prof. Odile Liboiron-Ladouceur supervised the work and edited the paper which was written by the candidate.

  1. A. Das, G. Zhang, H. Rahbardar Mojaver and O. Liboiron-Ladouceur, "Low Loss 8 × 8 Silicon Photonic Banyan Switch," *2020 IEEE Photonics Conference (IPC)*, Vancouver, BC, Canada, 2020, pp. 1-2.

- Design, fabrication and experimental demonstration of a low loss and ultra-broadband

MMI, used as a building block in a 2 × 2 and 16 × 16 Banyan switches for ulta-broadband and low loss operation in SiPh platform.

The candidate is the main author of the work which is submitted to present at 2021 Conference on Lasers and Electro-Optics (CLEO), titled "Ultra-broadband and Low-loss 16 × 16 SiPh Switch". Guowu Zhang helped the candidate to improve the building block in simulation. Prof. Odile Liboiron-Ladouceur supervised the work and revised the manuscript which is written by the candidate.

- Design, fabrication and experimental validation of a mode insensitive 3 × 3 and 4 × 4 switch matrices for first two quasi-transverse electric (TE) modes using multimode building blocks in SiPh platform.

  The building blocks used in the multimode switches was designed and characterised by our group and published in OSA Optics Letters Vol. 45, Issue 4, pp. 811-814 (2020). Part of this work was presented at 2020 IEEE Photonics Conference (IPC) by Guowu Zhang who was the first author of these peer-reviewed journal and conference proceedings. Dr. Hassan Rahbardar Mojaver and the candidate were the co-authors of these papers who helped the first author to do the experimental measurements and editing the manuscript. The details of this work is discussed in the background chapter of this thesis. After this successful work, the candidate conceived the idea to develop higher radix multimode switches using more optimized building blocks. This work is submitted in IEEE Photonics Technology Letters by the candidate, titled "Scalable

Two-mode 3-port and 4-port Mode Insensitive Silicon Photonic Switches". Guowu Zhang helped the candidate to optimized the building blocks. Prof. Odile Liboiron-Ladouceur supervised the work and edited the manuscript.

1. G. Zhang, H. R. Mojaver, A. Das, and O. Liboiron-Ladouceur, "Mode insensitive switch for on-chip interconnect mode division multiplexing systems," *Opt. Lett.* 45, 811-814 (2020).
2. G. Zhang, A. Das and O. Liboiron-Ladouceur, "A broadband MZI-based thermal-optic mode insensitive switch in Silicon-on-Insulator," *2020 IEEE Photonics Conference (IPC)*, Vancouver, BC, Canada, 2020, pp. 1-2.

- Design and experimental demonstration of distributed SOA based, scalable 16 × 16, 32 × 32 and 64 × 64 SiPh/InP hybrid switch matrices for lossless operation.

  Our research group demonstrated InP-SOA gain block based hybrid switches which were published in IEEE Photonics Technology Letters (Volume: 32, Issue: 11, June1, 1 2020) and presented at 2020 IEEE Photonics Conference (IPC) by Dr. Hassan Rahbardar Mojaver. The candidate was partially involved with this project by doing simulations related to InP-SOA gain block. InP-SOA gain block demonstrated through this project is described in the background chapter of this thesis. Using the experimentally validated results of the InP-SOA gain block, the candidate conceived the design idea to develop higher radix hybrid switches for lossless operation. This

work was published in IEEE Photonics Technology Letters (Volume: 32, Issue: 21, Nov.1, 1 2020) by the candidate. Dr. Hassan Rahbardar Mojaver was the second author of this paper who helped the candidate by providing all required data related to InP-SOA gain block and edited the manuscript. Guowu Zhang helped the candidate to revise the manuscript and Prof. Odile Liboiron-Ladouceur supervised the whole works and edited the manuscript.

1. A. Das, H. R. Mojaver, G. Zhang and O. Liboiron-Ladouceur, "Scalable SiPh-InP Hybrid Switch Based on Low-Loss Building Blocks for Lossless Operation," in *IEEE Photonics Technology Letters*, vol. 32, no. 21, pp. 1401-1404, 1 Nov.1, 2020.

2. H. R. Mojaver, A. Das, B. Rad, V. Tolstikhin, K. -W. Leong and O. Liboiron-Ladouceur, "Scalable SOA-Based Lossless Photonic Switch in InP Platform," *2020 IEEE Photonics Conference (IPC)*, Vancouver, BC, Canada, 2020, pp. 1-2.

1.4 Thesis Overview

This thesis consists of six chapters. The initial chapter is an introduction. Motivation, contributions and thesis organization are discussed briefly in this chapter.

In chapter 2, the theoretical background including the state-of-the-art of several types of silicon photonic switching technologies are investigated. This section also includes related

works and literature review. At the end of this chapter, performance parameters and current state of SiPh switches are discussed.

In chapter 3, we focus on the design and experimental demonstration of low loss and ultra-broadband SiPh MMIs as building blocks of large switch matrices. We start from the designing of MMIs then we also experimentally demonstrate SiPh thermo-optic switching matrices up to 16 $\times$ 16 port count.

In chapter 4, we explore multimode switching matrixes. we design and experimentally demonstrate mode insensitive 3 $\times$ 3 and 4 $\times$ 4 switching matrices for first two quasi-transverse electric (TE) modes based on the building blocks discussed in chapter 2.

In chapter 5, we propose large radix SiPh/InP hybrid switches up to 64 $\times$ 64 port count for lossless operation. Performance is discussed to validate these proposed switches.

The thesis concludes in chapter 6, which includes a summary of the contributions and a brief discussion regarding the future research directions.

Chapter 2

Background

2.1 Silicon Photonic Switches

The advancement of silicon photonics (SiPh) switches in communication systems has been rising rapidly in the last two decades due to several appealing features, such as high-index contrast between the silicon waveguide core and the surrounding oxide, low absorption coefficients within a large wavelength range, and the compatibility with the existing fabrication technology [15]. Silicon photonic switches often use interferometers or micro-electro-mechanical systems (MEMS) to perform switching. The most common types of interferometers are Mach-Zehnder interferometers (MZIs) and micro-ring resonators (MRRs). Interferometer based switch needs a phase shifter as an actuator which changes the direction of optical light by changing the optical phase. Phase shifter silicon photonic

switches can be classified in two types:

1. Thermo-optic (TO) switch

2. Electro-optic (EO) switch

Electro-optic switches exhibit fast switching time but suffer from high optical loss due to free-carrier absorption [16] whereas thermo-optic switch can achieve lower insertion loss at the cost of higher power consumption [17]. On the other hand, micro-electro-mechanical systems (MEMS) based switch allows high port count with fast switching time and low insertion loss [18].

2.1.1 Thermo-optic Switch

The silicon photonic thermo-optic phase shifter works based on the refractive index change dn/dT due to a certain temperature change (ΔT) at a specific wavelength (λ). The optical intensity distribution inside the waveguide can change significantly by a small change in the thermally tuned refractive index [19]. This refractive index change can alter the phase direction of light inside the waveguide at a specific wavelength. Based on this thermo-optic property, silicon photonic TO switches perform switching using micro-heater or thermal phase shifter [20]. The equation showing the relation between refractive index (n) and temperature (T) is,

$$n(T) = n(T_0) + \frac{dn(T - T_0)}{dT} \tag{2.1}$$

Here, n(T) and n(T_0) are the refractive indices at the specific temperature T and initial temperature T_0 respectively.

Silicon has a high thermo-optic coefficient at room temperature, it is $dn/dT = 1.86 \times 10^{-4}/K$. This thermo-optic coefficient enables precise phase tuning with a low temperature change. This facilitate the use of TO switches with low power consumption for switching application. The thermo-optic phase tuning ($\Delta\varphi$) can be express as,

$$\Delta\varphi \propto \frac{2\pi}{\lambda}\frac{dn}{dT}\Delta T L \tag{2.2}$$

where ΔT and L are the waveguide temperature change and heating length respectively and λ is the wavelength.

The absolute refractive index and thermo-optic coefficient (dn/dT) of silicon has been measured using the Cryogenic, High-Accuracy Refraction Measuring System (CHARMS) at NASA's Goddard Space Flight Center, as a function of both wavelength and temperature [21] are shown in figure 2.1 and 2.2 respectively.

The simplest method to implement a thermo-optic phase shift in silicon-on-insulator (SOI) platform is to heat a SiPh waveguide by placing a metallic thin film heater over it as shown in figure 2.3 (a). The metal thin film should be sufficiently separated to reduce the

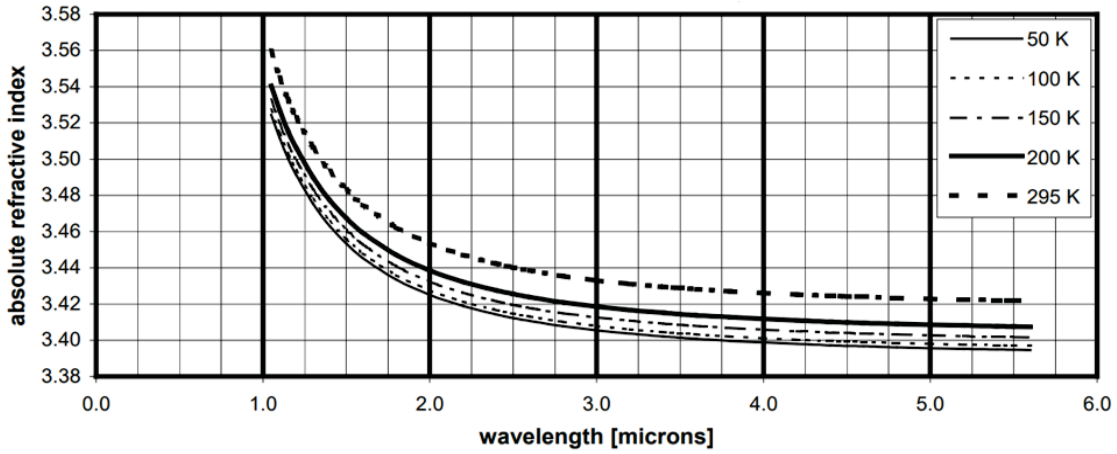

Figure 2.1: Measured absolute refractive index of silicon as a function of wavelength for selected temperatures [21].

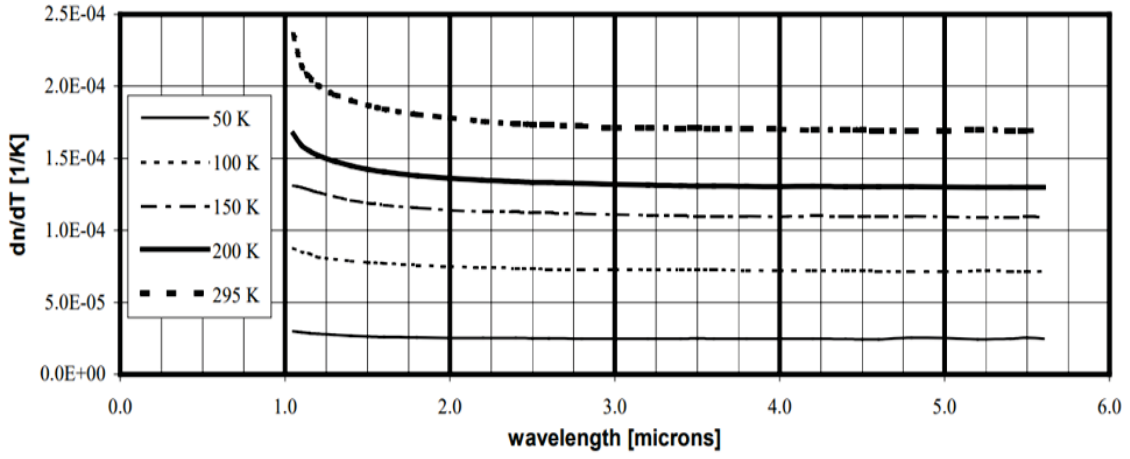

Figure 2.2: Measured thermo-optic coefficient of silicon as a function of wavelength for selected temperatures [21].

waveguide propagation loss. Usually 1-2 µm SiO_2 cladding layer is used to separate the metal heater from the Si waveguide. As the metal heater cannot heat the waveguide directly so the switching time is longer in TO switches (microseconds) [22]. The thermal tuning efficiency of this kind of heater is highly dependable on the thermal conductivity of the cladding materials, and the distance between the heater and the waveguide. The thin film materials also have important role in terms of power consumption. A high resistivity and high melting point is required for a heater material to ensure low power consumption and high temperature operation. Most SiPh foundries (e.g. IMEC, IME, ANT, etc.) are capable of fabricating this kind of heater, and all of them have their own standard specifications regarding the heater materials and the distance required between the metal and the waveguide.

Another most common and efficient method of thermo-optic phase shift is to use doped silicon phase shifter on both side of a rib waveguide as shown in figure 2.3 (b and c). The integrated heater is formed by an N++/N/N++ or P++/P/P++ structure where two heavily doped Si waveguide are electrically contacted by a lightly doped Si waveguide core, and due to the high resistivity of lightly doped region, heat is only produce onto the waveguide core. In this structure, sufficient distance should be maintained between the edge of the waveguide core and the heavily doped region to reduce the optical loss induced by free-carrier absorption. Therefore, proper design and precise fabrication are required in these such heaters to make it efficient enough in terms of optical loss reduction and high speed switching (nanosecond) in a SiPh platform.

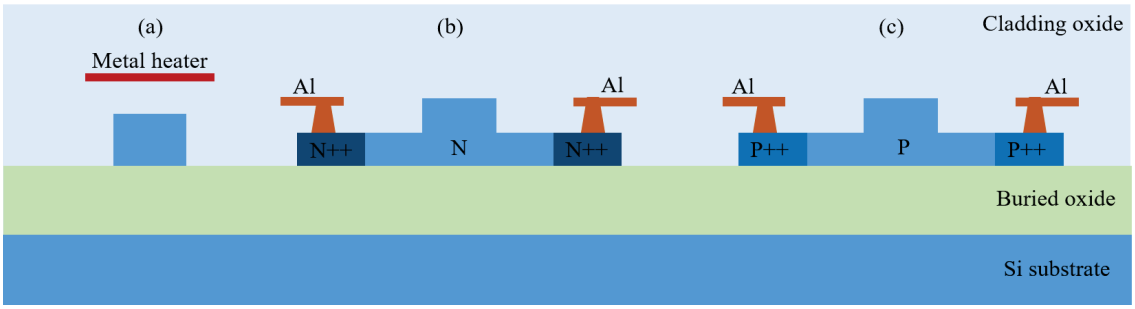

Figure 2.3: Cross section schematics of thermo-optic phase shifters in SOI platform; (a) metallic thin film heater; (b) doped Si heater using N++/N/N++ structure; (c) doped Si heater using P++/P/P++ structure.

Recently, several single and multimode SiPh switches have been published based on energy efficient thermo-optic phase shifter [4, 16, 23, 24]. Mode insensitive phase shifter able to switch TE_0, TE_1 and TE_2 mode simultaneously has also been reported [25].

2.1.2 Electro-optic Switch

Silicon has good response through free carrier dispersion effect also referred as plasma dispersion effect. Silicon exhibits weak or even zero coefficients of other common electro-optic effects, e.g., the Pockels effect, the Kerr effect, and the Franz–Keldysh effect [26–28]. Electro-optic phase shifter use plasma dispersion effect where refractive index change due to carriers [26]. The concentration of carriers in a waveguide core can change through either injection or depletion of carriers from the device.

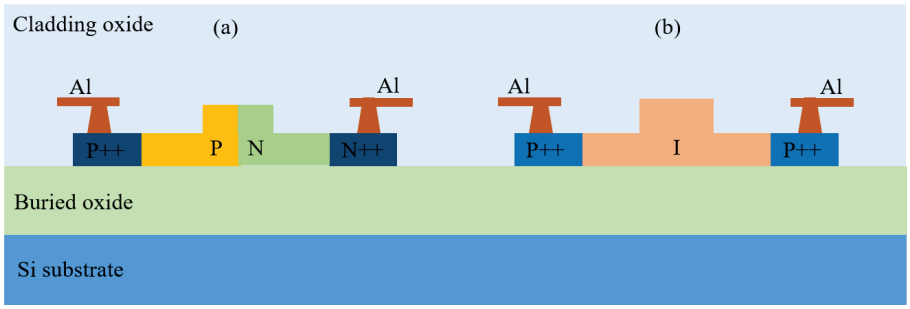

Figure 2.4: Cross section of electro-optic phase shifter; (a) carrier depletion phase shifter; (b) carrier injection phase shifter.

In silicon photonic EO switches, a PN or PIN junction is used to achieve either carrier depletion or carrier injection, respectively, to modify the carrier concentration in Si waveguide as depicted in figure 2.4. Typically, carrier injection has a strong effect onto the Si waveguide to change the refractive index compared to carrier depletion. However, carrier depletion can offer higher operation speed [29] while carrier injection is comparatively slow due to slow carrier injection or recombination process [30]. As carrier depletion is weaker, so device size need to be larger to ensure more interaction length [29, 31, 32] or require higher driving voltage to ensure enough modulation depth [33]. Due to free-carrier absorption used on the EO phase shifters, EO switches usually have high insertion loss and large crosstalk compared to TO switches. Several SiPh switches intended for energy efficient and high speed switching using electro-optic phase shifter have been reported [29, 31–33].

2.1.3 MEMS based Switch

Thermo-optic and electro-optic switches traditionally use material properties such as refractive index change by thermal or carrier density tuning. Although the change in material properties are limited (a few percent), there have non-negligible insertion losses and fabrication tolerance. Especially, in EO switches, the insertion loss is significantly high due to free carrier absorption. On the other hand, in MZI or ring resonator assisted switches, there have degraded extinction ratio and crosstalk due to imbalanced MZI arms for fabrication variations. In such situation, large radix switches realized by TO or EO methods typically have large insertion loss, crosstalk, limited bandwidth and need large driving power for bias offset to overcome the imbalance fabrication errors in MZI. Consequently, TO and EO switches typically limited to few port counts in a silicon photonic platform.

Silicon photonic MEMS technology can be a good solution to solve these above drawbacks for large radix switching matrix and mass production for growing datacenter. Even the switching speed (microseconds) is also better than regular 3D-MEMS based switches used in free space optics. Using silicon photonic MEMS technology, up to 240 $\times$ 240 has been reported [34] and the scaling for large port counts switching matrix is increasing rapidly as shown in figure 2.5.

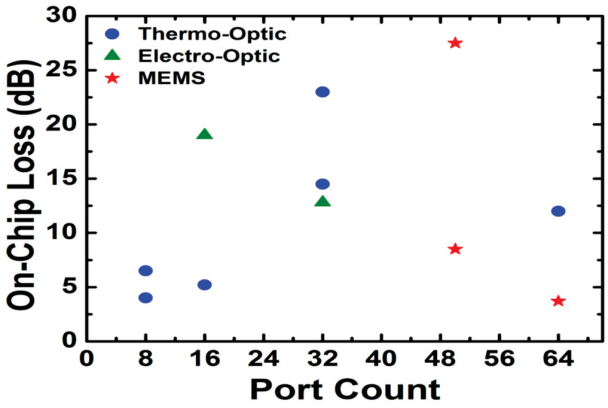

Figure 2.5: Switch size (port count) of published silicon photonic switches versus year of publication [35].

2.2 Multimode Switch and Building Blocks

Switching and routing of data signals are one of the most basic requirements in optical data center networks. Conventional SiPh switches use wavelength division multiplexing (WDM) system, which is the most mature and widely used technology in the optical data center networks. However, multiple laser sources are required to generate multiple wavelengths to transmit signals through WDM systems. This increases the power consumption and make is difficult to manage for an on-chip applications [36]. The capacity of data transmission over a limited bandwidth to meet the increasing demand is the main challenge of WDM systems. In this circumstance, Mode division multiplexing (MDM) technology has attracted widespread attention due to offering a new dimension to increase the data capacity by utilizing the spatial modes of waveguide using single wavelength carrier [37]. To utilize the extended

capacity of bandwidth mentioned above, various SiPh devices has been developed for MDM networks, such as mode multiplexer/de-multiplexer [38], switchable mode exchanger [39], multimode optical switches [23–25, 40–43], power splitter [44], etc.

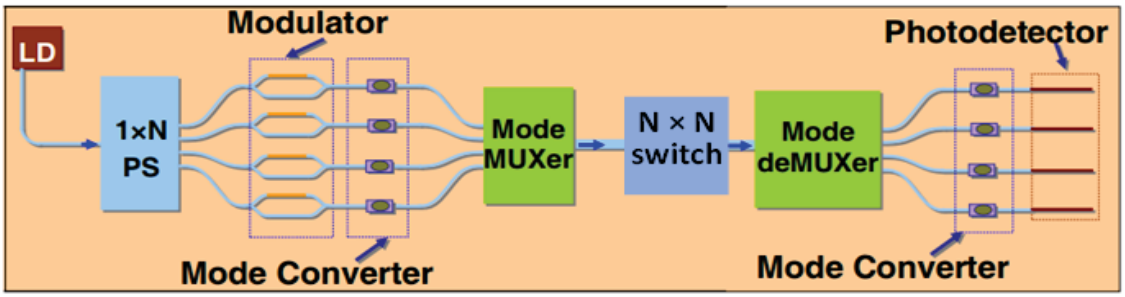

Figure 2.6: Schematic of a conventional silicon photonics mode division multiplexing (MDM) link [45].

Among them, the multimode optical switch is a key component to route the multimode signals in a MDM network as shown in figure 2.6. Over the past few years, several efforts have been taken to obtain the multimode switches [23–25, 40–43]. Most of them depend on mode multiplexing and de-multiplexing to decode and encode the multimode signals to the fundamental mode signals and vice versa, respectively. Between these, single mode optical switches have been used to switch the signals for different outputs as depicted in figure 2.7. This process is stable but large footprint and high power consumption are the bottlenecks of this approach. On the other hand, simultaneously controlling several spatial modes on a same waveguide is challenging due to the different structural relationship between the waveguide and the different modes. Very few approaches for MDM switch has been proposed, such as microring resonator based WDM compatible MDM switch [40, 46], symmetric Y junctions

and multimode interference (MMI) couplers based two-mode switch [41], densely packed waveguide array based two-mode switch [47], MDM compatible large radix switch using demultiplexing-switching-multiplexing technique [48] and single mode phase shifter assist MDM mode switches [23, 49] are also recently investigated.

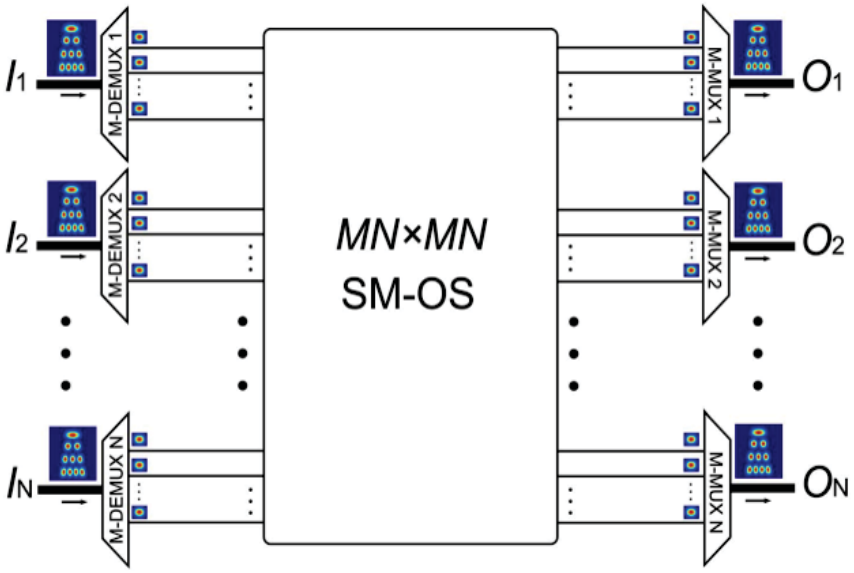

Figure 2.7: Schematic of a conventional N × N multimode optical switch using demultiplexing-switching-multiplexing technique [50].

Recently, we reported a balanced Mach–Zehnder interferometer (MZI) based 2 × 2 switch with a mode insensitive phase shifter for the first three quasi-transverse electric (TE) modes [25]. In this section, the optimized design parameters of several essential building blocks used in our design, such as mode multiplexer/de-multiplexer, multimode 2 × 2 MMI, multimode S-bend, mode insensitive phase shifter, and mode insensitive MZI switch are discussed.

2.2.1 Multimode 2 × 2 MMI and S-bend

Multimode interference (MMI) based optical components stand itself as a game-changer in the photonic industry. MMI works based on optical self-imaging properties discovered around 184 years back [51]. Self-imaging is a property of a multimode waveguide that allows the reproduction of the input field profile to single or multiple images at periodic intervals along the propagation direction of the waveguide [52].

The beat length (L_π) is the distance between two lowest order modes and can be expressed as,

$$L_\pi = \frac{\pi}{\beta_0 - \beta_1} = \frac{4 n_{eff} {W_m}^2}{3\lambda_0} \tag{2.3}$$

where β_0 and β_1 are the propagation constants of the first two TE modes in the multimode region, n_{eff} is the effective index, W_m is the width of MMI, and λ_0 is the desired wavelength.

Table 2.1: The characteristics of general, paired, and symmetric interference mechanisms.

Interference mechanism	General	Paired	Symmetric
Input × Outputs	N × N	2 × N	1 × N
First single order image distance	$(3L_\pi)$	(L_π)	$(3L_\pi)/4$
First N-fold image distance	$(3L_\pi)/N$	$(L_\pi)/N$	$(L_\pi)/4N$
Excitation requirements	none	$c_v = 0$; For v = 2, 5, 8...	$c_v = 0$; For v = 1, 3, 8...
Input (s) location (s)	any	y = ± $W_e/6$	y = 0

According to L. B. Soldano et al. [52], the characteristics of general, paired, and

symmetric interference mechanisms are summarized in table 2.1, where, c is the mode coefficient, and v is the mode number.

Using the self-imaging property discussed above, a 0.22 µm thick, 10 µm wide and 362 µm long 2 × 2 MMI core has been designed. The slab waveguides used to connect each component have a width of 1.45 μm tapered to 3.8 μm over a 20 μm length before connecting with the MMI core. This design approach reduce the insertion loss between the MMI cores and the connecting waveguides as illustrated in figure 2.8. The beat length (L_π) is initially calculated using the equation above and further optimized by Lumerical tools [53].

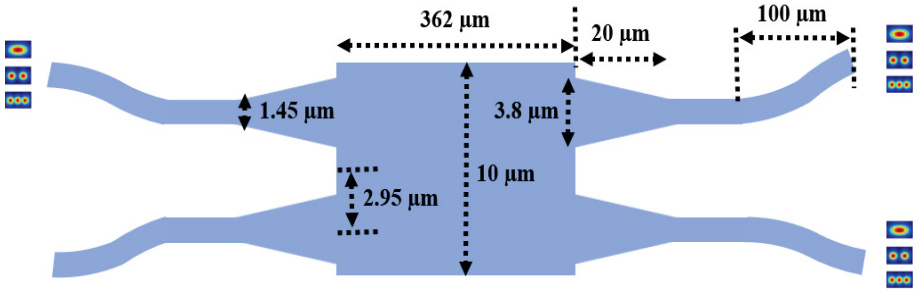

Figure 2.8: 2 × 2 MMI splitter/combiner with multimode S-bend (regenerated from [25]).

In MZI building block, two MMIs are separated by multimode S-bends to make sure the separation of the arms of MZI is large enough to prevent thermal crosstalk between MZIs induced by the thermal phase shifter. A compact S-bend with a 1000 µm radius and 100 µm length has been designed to reduce the mode mismatch as shown in Figure 2.8.

2.2.2 Multimode Waveguide and Mode MUX/deMUX

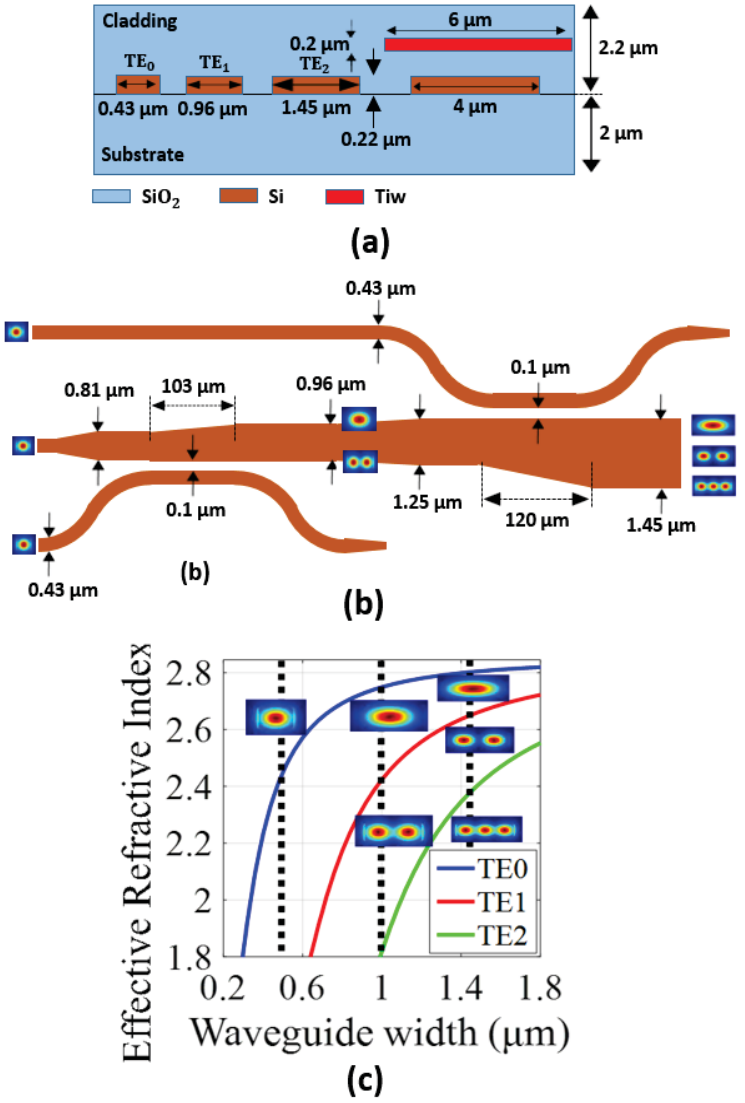

Figure 2.9: (a) Cross section of the TE_0, TE_1, TE_2 waveguide, and phase shifter; (b) schematic of the mode MUX and deMUX; (c) simulated effective refractive index as a function of waveguide width (regenerated from [25]).

The proposed building blocks are designed for fabrication on a silicon-on-insulator (SOI) chip with a device thickness of 220 nm. The widths of the waveguides for fundamental mode (TE_0), two-mode (TE_0 and TE_1), and three-mode (TE_0, TE_1 and TE_3) are selected to 0.43 µm, 0.96 µm, and 1.45 µm, respectively, as shown in figure 2.9 (a). In figure 2.9 (c), the simulated effective refractive index is shown as a function of waveguide width. An adiabatic directional coupler-based mode multiplexer (MUX)/de-multiplexer (deMUX) is used for corresponding mode conversion at the input and output respectively as depicted in figure 2.9 (b). The input and output waveguide widths of the bus waveguide and the length of the taper are 0.81 µm (1.25 µm), 0.96 µm (1.45 µm), and 103 µm (120 µm) for TE_1 (TE_2) mode multiplexers, respectively [25].

2.2.3 Mode Insensitive Phase Shifter

To make mode insensitive switch, a mode insensitive phase shifter is necessary. However, as different modes have different propagation constant, mode insensitive phase shifter is challenging to realize. In simulation, using Lumerical MODE and DEVICE, we observed that the change in the rate of effective index with respect to the local temperature (dn_{eff}/dT) converges toward almost the same value for three different TE modes by increasing the phase shifter width. When the waveguide width is larger than 4 µm, the difference between the values of the dn_{eff}/dT for the first three TE modes (TE_0, TE_1 and TE_2) is less than 2% (±1%) as shown in Figure 2.10 (b). Thus, a mode insensitive phase shifter that works

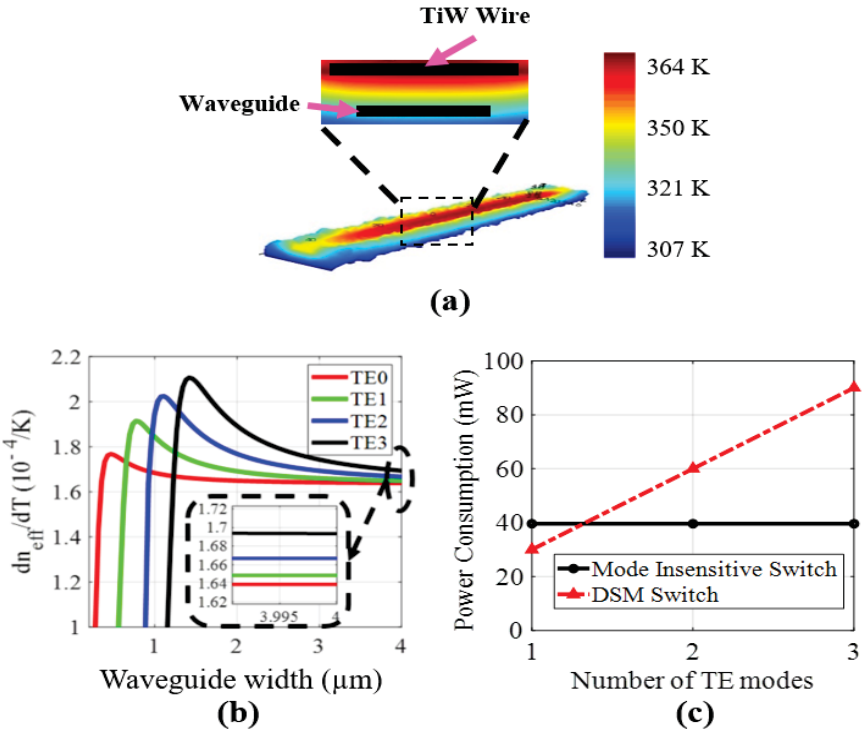

Figure 2.10: Phase shifter; (a) simulated temperature distribution of the phase shifter; (b) simulated dn_{eff}/dT as a function of phase shifter width for the first four TE modes; (c) power consumption as a function of the number of modes (regenerated from [25]).

for TE_0 , TE_1, and TE_2 simultaneously is obtained. The phase shifter can remain mode insensitive even for the higher order modes (e.g.,TE_3, TE_4 etc.) by increasing the width of the waveguide and phase shifter. However, heater power consumption will increase with the waveguide and heater width as depicted in 2.10 (c). In our design, we choose the width of the phase shifter as 4 µm to optimize the power consumption and the mode insensitivity. Finally, a 200 nm thick, 200 µm long and 6 µm wide TiW thin-film heater is designed to realize the phase shifter as shown in Figure 2.9 (a). For the first three input TE modes, the

mode insensitive power consumption is measured around 40 mW per phase shift. In Figure 2.10 (a), the simulated temperature distribution profile is shown.

2.2.4 2 × 2 Mode Insensitive MZI

Using the building blocks discussed above, a multimode mode insensitive 2 × 2 MZI switch is designed for the first three quasi-transverse electric (TE) modes. The MZI consists of two 2 × 2 multimode interferometer (MMI) connected by 4 µm wide Si waveguides with 100 µm long S-bend to prevent the thermal crosstalk induced by 200 µm long and 6 µm wide Titanium Tungsten (TiW) phase shifter placed between the two MMIs and 2 µm above one of the MZI balanced paths as shown in figure 2.11 (a).

Both continuous wave and payload transmission is done to characterize the switch for the real data transmission system. Figure 2.11 (b) shows the normalized transmission spectrum as a function of the phase shifter voltage. When no voltage is applied to the phase shifter, all the three-mode propagate through the cross port. When an appropriate voltage is applied to the phase shifter, the switch works on the bar port. For the TE_0, switching occurs at 2.46 V, where the extinction ratio (ER) is approximately -34.5 dB. For TE_1 and TE_2 the required switching voltage is measured 2.38 V and 2.32 V, where the extinction ratio is approximately -25.5 dB and -23 dB respectively. It is observed that the voltage difference among the three-mode is less than 0.14 V (±3%). To make the switch mode insensitive, 2.4 V is used for all experiments. At this bias voltage, The extinction ration is measured 20.7

db, 26.5 dB, and 17.8 dB for TE_0, TE_1, and TE_2, respectively at 1560 nm [25].

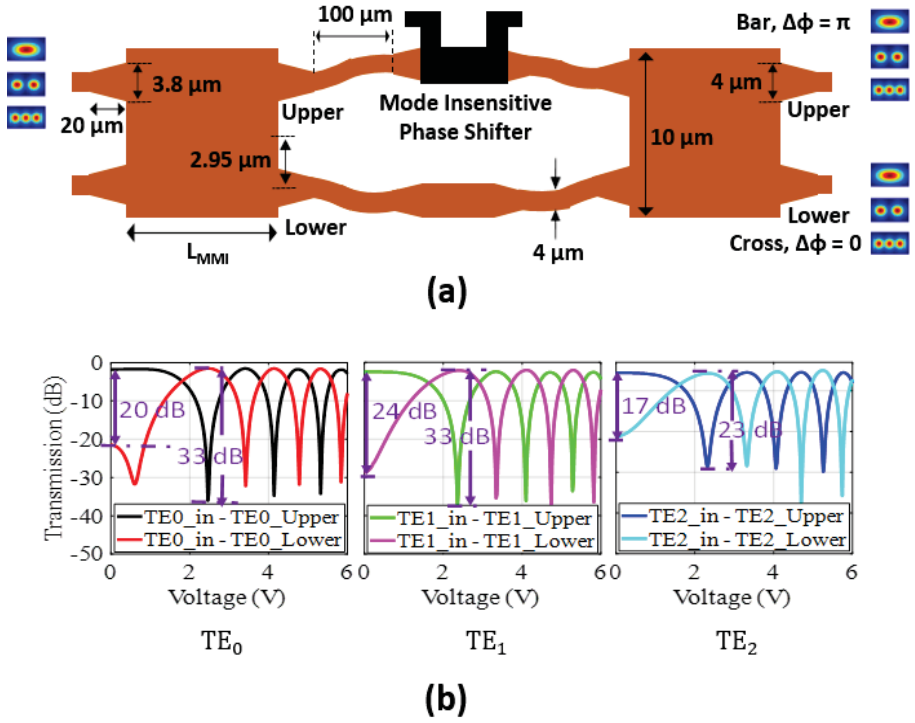

Figure 2.11: (a) Schematic of the mode insensitive MZI switch; (b) measured normalized transmission spectrum versus the applied voltage for all three-modes [25].

For TE_0, TE_1, and TE_2 mode, the insertion loss (IL) is -2 dB (-2.1 dB), -3.6 dB (-3.2 dB), and -5.1 dB (-5.7 dB) for cross (bar) state at 1550 nm. The crosstalk for TE_0 is measured approximately -8.6 dB and -9 dB for the cross and bar state within 40 nm of the wavelength range from 1535 nm to 1575 nm. For TE_1, the crosstalk is -8 dB and -10.3 dB for the cross and bar state within the same wavelength range. For TE_2, the crosstalk is -10 dB and -10.3 dB for the cross and bar state within the same wavelength range. Almost clear open eyes are observed for both the single and simultaneous mode transmission. It is realized that,

most of the insertion loss and crosstalk comes from the mode multiplexer and demultiplexer in experiment, which is further optimized and used in larger matrix switches in chapter 4.

2.3 InP-SOA Gain Block

Integrated switches fabricated in an III-V semiconductor platform such as indium phosphide (InP) can offer high speed switching with inherent on-chip gain in direct bandgap region. The on-chip gain can be used to reduce the optical losses realized from multiple switching stages; thus, lossless switching operation can be obtained. Several switching matrices have been recently introduced utilizing the integration of SiPh switches with III-V semiconductor gain block to perform the lossless operation using the on-chip gain in the active medium [54–59]. Recently, our group experimentally demonstrated InP-SOA gain block based several SiPh/InP hybrid optical switches for lossless operation [4, 54, 60, 61]. In chapter 5, this InP-SOA is further studied for larger switch matrix.

Semiconductor optical amplifier (SOA) uses semiconductor as a gain medium to amplify the optical signal. Typically, an SOA is like a semiconductor laser without feedback. In this case, the anti-reflection coating is used instead of end mirrors and the end reflections also can be reduced further by using a tilted waveguide. SOA use stimulated emission to amplify the incident light. The SOA can be characterized using key parameters such as gain, bandwidth, saturation power, and noise figure. Indium phosphide (InP), a direct bandgap semiconductor, can feature a strong inter-band gain in the desired wavelength. Our research

group experimentally validated a InP-SOA chipset that can provide gain exceeding 25 dB with less than 7 dB noise figure. This gain block allows distortion-free 12.5 Gb/s optical data transfer [54, 60].

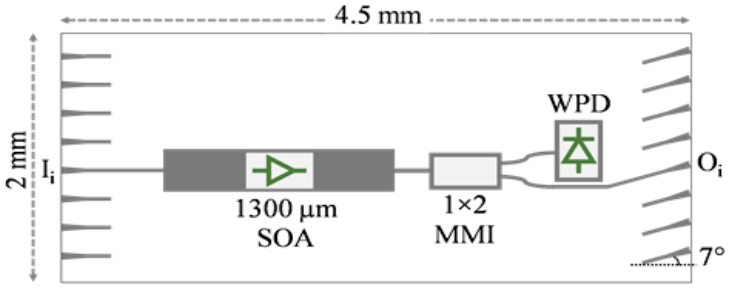

Figure 2.12: Schematic of the SOA gain block. Ii and Oi are the i-th input and output ports [54].

The InP gain block comprises a booster SOA coupled to a 1 × 2 multimode interference (MMI) splitter (85:15) and a waveguide photodetector (WPD) for on-chip optical power measurement as shown in figure 2.12. The front and back facets of the input and output ports of the SOA are coated to reduce the reflectivity to below -30 dB. To minimize the residual Fabry-Perot effects, the output ports of the InP gain block are tilted at seven degrees. The amplification is intrinsically polarization-sensitive, but the amplifier designs used, provide nearly polarization-independent characteristics [62]. The specification of the InP-SOA gain block is given in table 2.2.

The InP gain block is fabricated through SMART Photonics [62] and characterized by our research group. The continuous wave (CW) measurement and payload data transmission (RF) are then experimentally performed to demonstrate the overall performance of the gain

Table 2.2: Gain block specifications

Parameter	Minimum value	Typical value	Maximum value	Units
SOA Length	—	1300	—	μm
SOA Net Gain	25	—	—	dBm
SOA Noise Figure	—	—	7	dB
SOA Gain Saturation	10	—	—	dBm

block. Considering the on-chip (2.9 dB) and coupling loss (3 dB), a minimum net gain of 24.6 dB is measured from the experiment [54]. To obtain a 25 dB gain, 75 mA bias current is required corresponding to 1.54 V voltage. By changing the bias current from 30 mA to 75 mA the gain can be tuned from 0 dB to 25 dB. Therefore, each gain block consumes 115.5 mW of power for each 25 dB of gain. For a bias current above 90 mA, gain saturated deeply [54]. The minimum value of measured noise figure (NF_{SOA}) is 7.7 dB, which is close to the reported value (7 dB) of the fabrication foundry (SMART Photonics).

2.4 SiPh Fabrication Process

As mentioned, all of the silicon photonic switches are designed for fabrication on a silicon-on-insulator (SOI) wafer through Applied Nanotools Inc. (ANT) [63]. The device layer is a 220 nm thick silicon layer with a 2 µm buried oxide layer placed on top of a 675 µm thick silicon handle (substrate) wafer shown in figure 2.13. The device is patterned onto SOI using electron beam lithography (EBL) and reactive ion etching (RIE) processes. The patterning process begins by cleaning and spin-coating, then 100 KeV EBL is used to define

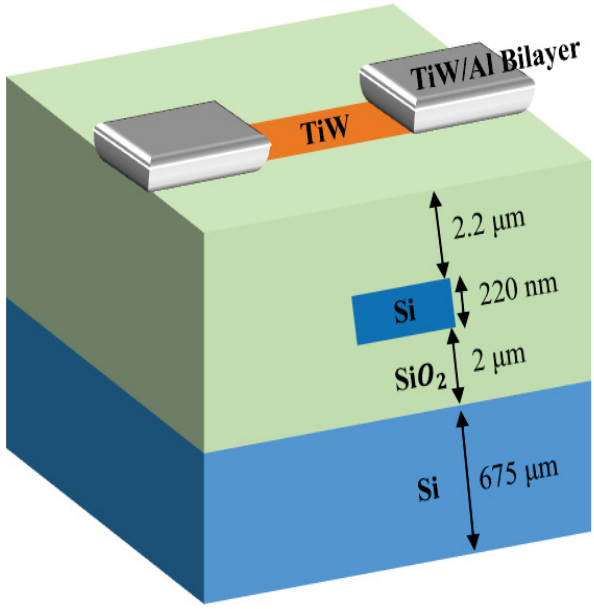

Figure 2.13: Schematic blocks indicating the fabricated layers (passivation layer is not shown).

the device pattern into the materials, which is very sensitive to electron beam exposure. An anisotropic inductively-coupled-plasma reactive ion etching (ICP-RIE) process is conducted on the substrate to transfer the pattern into the underlying silicon layer once the material has been chemically developed. After the patterning, an etching process is performed to remove the remaining silicon from the device layer. In this fabrication process, the minimum feature size and spacing are 60 nm where the duty cycle of the surrounding region is no more than 50% for better resolution. Once the device is patterned correctly, a plasma-enhanced chemical vapour deposition (PECVD) process is used to deposit 2.2 µm cladding oxide (SiO_2) layer to ensure optical and thermal isolation from the outside environment. This oxide deposition process and tri-layer metallization process can be combined to fabricate

the thermal heater with an oxide passivation layer on top of it. For a 500 nm wide and 2.2 µm thick straight waveguide, 1.5 dB/cm propagation loss is guaranteed for fundamental TE mode while 3.8 dB/cm in curved waveguide [63]. All designs discussed in this thesis were fabricated at Applied Nanotools Inc. (ANT) through Silicon Electronic-Photonic Integrated Circuits (SiEPIC) consortium.

2.5 Coupling Technologies

Several approaches, such as wafer bonding [64], flip-chip [55, 57, 59] and photonic wire bonding [65, 67–70] have been investigated to integrate InP-SOA on a SiPh platform. In wafer bonding, the alignments are determined lithographically on the wafer as illustrated in figure 4.7(a), which provides efficient coupling between SOAs and Si platforms. However, existing foundries still have challenges in fabricating such III-V process on a Si wafer. Flip-chip technology shows less complexity to integrate SOAs on the Si platform compare to the wafer bonding technique, as wafer bonding is difficult for dissimilar materials [71]. Optimized InP-SOAs can easily be placed on top of the Si wafer where the mode field on the InP-SOA and Si waveguide is expended by the spot-size converter (SSC) for efficient coupling as depicted in figure 2.14(b). Still, it remains challenging because the coupling losses may increase significantly due to small misalignment between the SOAs and Si wafer [55]. According to SMART Photonics, the maximum coupling loss between two chips is between 5 dB and 7 dB. However, lossless operation also has been reported by

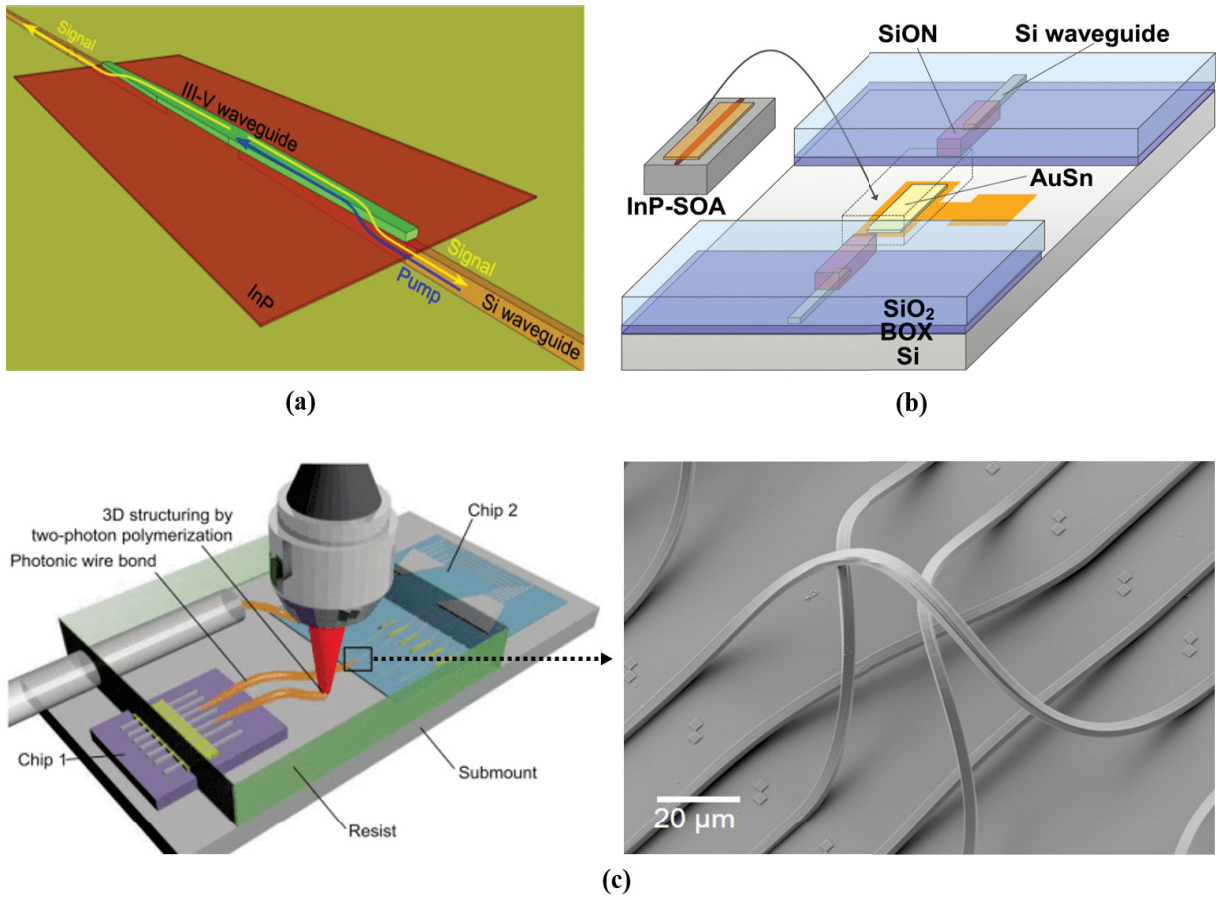

Figure 2.14: Hybrid-integration technologies. (a) illustration of the optically pumped LED using wafer bonding [64]; (b) configuration of flip-chip bonding for in-line amplification [55]; (c) artist's view of photonic wire bonding for chip-to-chip interconnects between different photonic devices on several substrates and photonic wire bonded waveguide crossing (inset) [65, 66].

maintaining precise alignment procedures in flip-chip technology [57]. Recently, photonic wire bonding technology may provide efficient coupling with relaxed alignment tolerance [65, 67–70] as shown in figure 2.14(c). The average insertion loss for the photonic wire bonding is measured and ranges from 1.7 dB to 3.5 dB [70]. In similar work [72], the total

insertion loss, including coupling from the InP device to the photonic wire bonding, propagation within the photonic wire bonding, and coupling from the photonic wire bonding to the silicon photonic waveguide is reported to be 4.3 dB. Using the photonic wire bonding technology, waveguide crossing-oriented losses can also be reduced significantly in the packaging step as shown in figure 2.14(c) (inset). In chapter 5, the hybrid integration of SiPh and InP chips is investigated using both photonic wire bonding and flip-chip techniques. In both of these techniques, we are considering 5 dB coupling loss for each SiPh to InP inter-chip connection as a worst-case scenario, while for fiber to SiPh chip coupling loss is measured 3.5 dB.

2.6 Important Parameters

There are several parameters to consider while designing a silicon photonics switch. The most common and important performance metrics are described below.

- **Insertion loss:** The most important parameters for both passive and active components is the material insertion loss. It can be defined by the optical propagation loss induced by the material optical properties such as refractive index, propagation constant, etc. The on-chip insertion loss can also be affected by the side wall roughness, waveguide bending, etc. The total insertion loss of a large switch matrix is the combination of all losses comes from the building blocks such as MZI,

waveguide crossing and phase shifter. There have also some unavoidable optical loss comes from fiber to chip or chip to fiber coupling through grating coupler, edge coupler, or optical wire bonding. High insertion loss is one of the most common limiting factors of large switching matrix.

- **Crosstalk and Extinction ratio:** Signal leakage through an unintended output port of a switch is called optical crosstalk. As crosstalk is treated as noise, it can reduce the optical signal-to-noise-ratio (OSNR). It is often expressed by extinction ratio (ER). The ER of a 2 × 2 switch defined by the output power ratio between two switching states such as 'ON' and 'OFF' state of an optical port on a logarithm scale while the optical power comes from the same input port,

$$ER = 10log_{10}\frac{P_{high}}{P_{low}} \tag{2.4}$$

where, P_{high} and P_{low} represent the optical power transmission a high power ('ON' state) and low power ('OFF' state), respectively. High extinction ratio is required to prevent power leakage through the unwanted output ports of an optical switch typically determined by the cross-coupling and through-coupling ratios of MMIs or directional couplers. Basically, higher crosstalk is a result of lower extinction ratio. The crosstalk can be improved by incorporating tunable couplers [73] or using nested MZI [74]. Phase shifter used in MZI also can use to tune the ER by external bias voltage.

- **Bandwidth:** Optical bandwidth is the range of optical frequency that can be handled by an optical device. In silicon photonic switch, optical bandwidth is one of the most common limiting factors for WDM syetems. For large matrix switch, bandwidth gradually reduces due to multiple stages of building blocks.

- **Power consumption:** In modern datacenter, high power consumption is a serious concern in order to reduce the total energy cost of a system. So, photonic switch should be energy efficient with a lower power budget. In silicon photonic switch matrix, electrical power (mW) is use to tune the phase shifters as well as actuate the gain blocks in hybrid platform.

- **Switching speed:** High speed tuning is desired in photonic switches according to their applications. EO switches have high switching speed in the nanosecond stage compared to TO switches (ms) due to faster response time of carrier injection or carrier depletion in SiPh platform.

- **Scalability:** As the communication system is growing, SiPh switches should be sufficiently compact to accommodate large number of port counts. Insertion loss, crosstalk, bandwidth, and footprint are the most affecting factors for scalability. For instance, port-to-port optical loss, crosstalk, or bandwidth of a photonic switch is a function of the number of ports of the switch. The increasing footprint also can increase the fabrication cost which also can be a limiting factor for large scale

production in industry. To make more flexible system, photonic switches should be scalable with a compact footprint.

- **Packaging:** Photonic packaging is an interesting feature used to convert photonic integrated circuit into device. Photonics packaging requires extremely accurate placement of components to ensure appropriate suitable alignment and coupling of light into and out of devices. Any inappropriate alignment can introduce additional coupling loss in packaging. Due to this challenges, photonic packaging is still expensive for small scale production.

2.7 Current State of Silicon Photonic Switches

In recent years silicon photonic switches have improved due to the commercialization of photonic technology. New features are revealing gradually to meet the growing demands of next generation applications.

Most of the demonstrated silicon photonic switches are suffering from inevitable optical losses and crosstalk [75]. Bandwidth limitation is also an important issue because of 2×2 couplers and most of the switching components are wavelength-dependence. Large matrix silicon photonic switch comprises thousands of MMIs/ directional couplers, phase shifters, waveguide crossings and bendings while designers pay attention to the footprint and the power consumption [76]. Larger footprint of photonic switch increases the fabrication cost

while compact MZI or ring resonator based TO switches are affected by thermal crosstalk [77].

As millions of switches are employed in datacenters, large power consumption in each switching block contributes to the enormous power load leading to rise in the total operational cost. Phase tuning time is also playing an important role in high-speed applications. Electro-optic switches have potential in applications where high speed data processing and storage are necessary. However, EO switches still have larger insertion loss compared to TO switches due to the change in carrier density and the fact that, EO phase tuning may break the power balance in the MZI structure as reported in [78].

Multimode switches can be key components in silicon photonic industry where different optical modes are used to transmit data using one single coherent optical source. Several multimode switches have been demonstrated using multimode MMI, Y-junction, and micro-ring resonator. However, multimode optical components like multimode waveguide crossing, multimode S-bend, energy efficient mode insensitive phase shifter are still under-development for higher order modes.

Further, fabrication uniformity is highly desired for better performance from silicon photonics integrated circuits. Small changes even in the nanometre scale can make a balanced MZI to become unbalanced, or can change the coupling ratio inside the MMI or directional coupler adding unexpected loss or crosstalk. Sidewall roughness also a common problem for photonic components introduced by fabrication imperfections.

This thesis presents development addressing the above challenges. Both single mode and multimode switches including the hybrid switching for lossless operation are studied intensively focusing on the state-of-the-arts of silicon photonic switches.

Chapter 3

SiPh Thermo-optic Switches for Low Loss and Broadband Operation

Silicon photonic switches with low insertion loss and wide bandwidth are highly expected in large-scale switch matrices. Thermo-optic (TO) switches usually allow lower insertion loss compared to their electro-optic counterparts. Although TO switch has a slower switching time, in terms of optical loss and robustness, it is more suitable to use in a larger switching matrix. In recent years, multimode interferometer (MMI) has received more attention for optical switching applications. As a power splitter or combiner in a MZI structure, MMI can realize superior performance compare to Y-splitter or directional coupler in terms of optical bandwidth, insertion loss, crosstalk, footprint, and higher fabrication tolerance.

In this chapter, a low loss 2 $\times$ 2 MMI with 3 dB splitting ratio and wide bandwidth at

1550 nm has been designed and demonstrated. One MMI has been designed to achieve low insertion loss with a compact footprint, and another MMI has been developed for both low insertion loss and ultra-broadband data transmission. A Titanium-tungsten (TiW) heater has been designed with reasonable power consumption. The heater is used in one of the MZI's balanced paths to realize the π-phase shift required for switching. For large-scale switch matrices, Banyan topology with blocking behavior has been used to reduce the optical power budget and the footprint [79–83]. Banyan switches are compact in size and suitable for large port count due to significantly lower insertion loss and simple structures [84, 85] compare to other topologies such as Benes, Spanke-Benes, and Crossbar, etc.

3.1 Building Blocks

In this section, the design, simulation, and experimental demonstration of the building blocks used in the intended switches are discussed. All switches including the building blocks were fabricated at Applied Nanotools Inc. (ANT) and characterized in McGill Photonic Systems laboratories.

3.1.1 Design of the Low Loss 2 $\times$ 2 MMI

Based on the self-imaging properties of multimode waveguide, a 0.22 μm thick, 6 μm wide and 131 μm long 2 $\times$ 2 MMI core has been designed using the commercial simulation software Lumerical MODE and FDTD [53]. The slab waveguides used to connect each component

have a width of 0.5 μm tapered to 1.4 μm over a 20 μm length before connecting to the MMI core. The design approach reduces the insertion loss between the MMI cores and the connecting waveguides shown in figure 3.1(a). In figure 3.1(b), the optical field profile inside the MMI is shown.

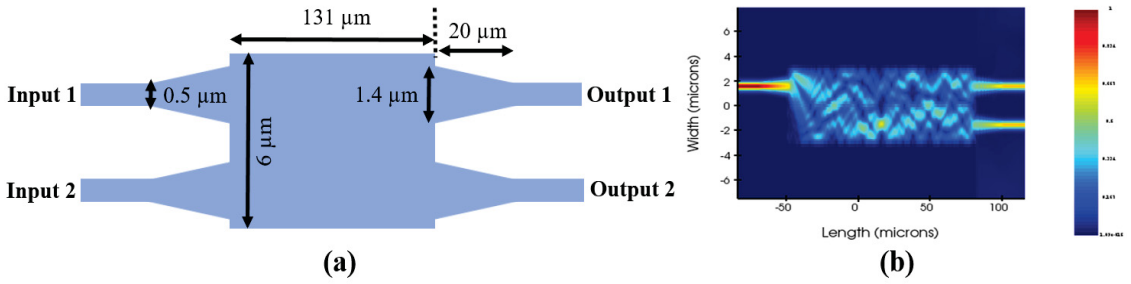

Figure 3.1: 2 × 2 MMI; (a) schematic of 2 × 2 MMI; (b) optical field profile of MMI.

Figure 3.2(a) shows the simulated output power spectrum of a 3 dB MMI splitter when 0.0 dBm optical power is inserted into one of the inputs using the software Lumerical Interconnect. Continuous wave (CW) measurement is also done, and the normalized output power is shown in figure 3.2(b). The 3 dB splitting ratio is assessed on the MMI in both simulation and measurement at 1550 nm. However, it is observed that the bandwidth is limited in the measurement because of the less optimized grating coupler with comparatively narrow bandwidth.

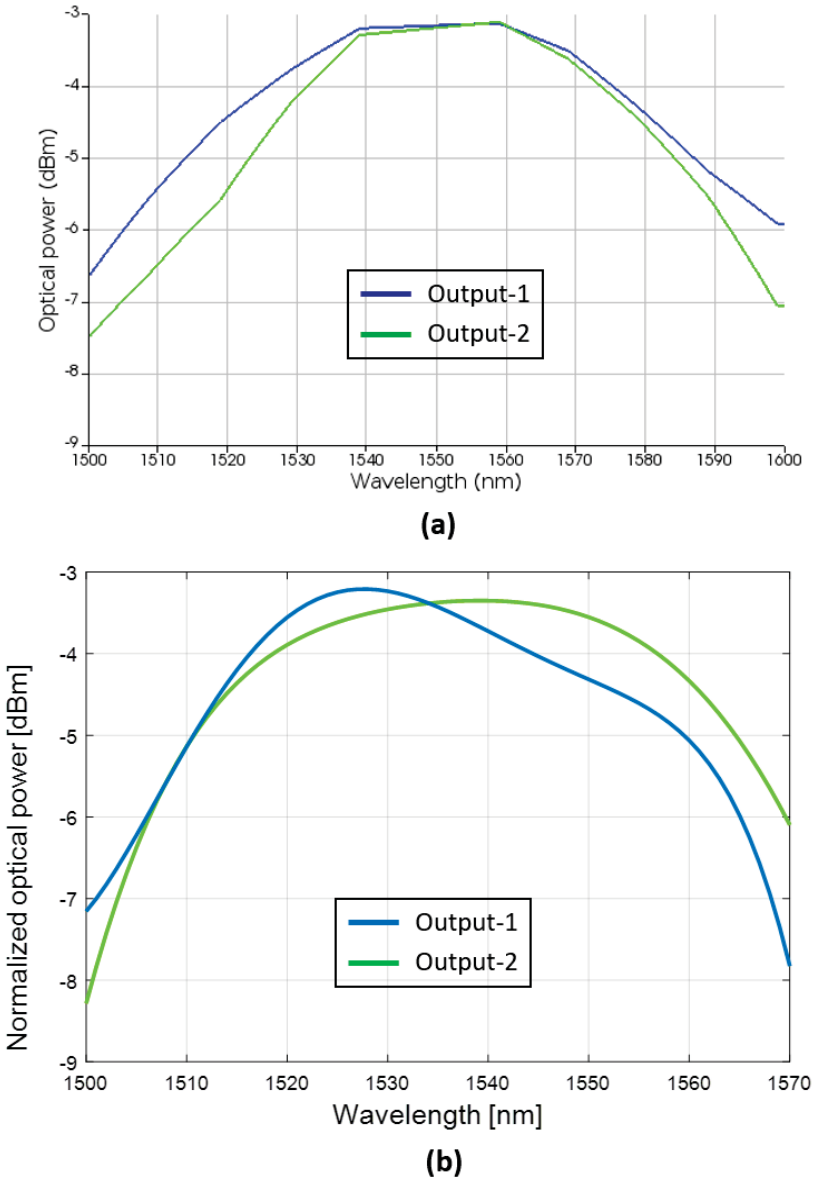

Figure 3.2: Output power spectrum of the 3 dB MMI splitter while one of the input power is 0 dBm; (a) simulated optical power; (b) measured normalized optical power.

3.1.2 Design of the Thermo-optic Phase Shifter

The total power budget and footprint of silicon photonic switches are highly dependable on the phase shifter integrated into the device. Low power consumption and compact size with fast tunability are desired for silicon photonic switches. All the designs discussed in this chapter have been done using the thermo-optic phase shifter. As we described theoretically in chapter 2, the silicon photonic thermo-optic phase shifter works based on the refractive index change due to a particular temperature change at a specific wavelength. The tuning efficiency of thermal phase shifter is proportional to the heating length and the waveguide temperature change.

In this work, Titanium-tungsten (TiW) metal heater is used as a phase shifting element due to its high melting point and high resistivity ensuring no unwanted electro-migration incidence at a higher temperature. Our designed phase shifter is fabricated through Applied Nanotools Inc. (ANT) [63]. According to ANT fabrication process, Titanium-tungsten alloy (TiW) is made of 10% Titanium and 90% Tungsten with an overall density of 14675 kg/m^3. Tri-layer metallization has been used to design and fabricate compact heater using a high-resistance (3.07 Ω/sq) TiW sheet with 200 nm thickness shown in figure 3.3. A 200 µm long and 5 µm wide TiW thin film is used and placed 200 nm above the waveguide to prevent direct heating. However, this small distance may increase the tuning time of the heater up to tens of microseconds. Low resistance (0.08 Ω/sq) Titanium-tungsten/Aluminum bi-layer (TiW/Al) is used as a contact layer of the heater with a total 700 nm thickness.

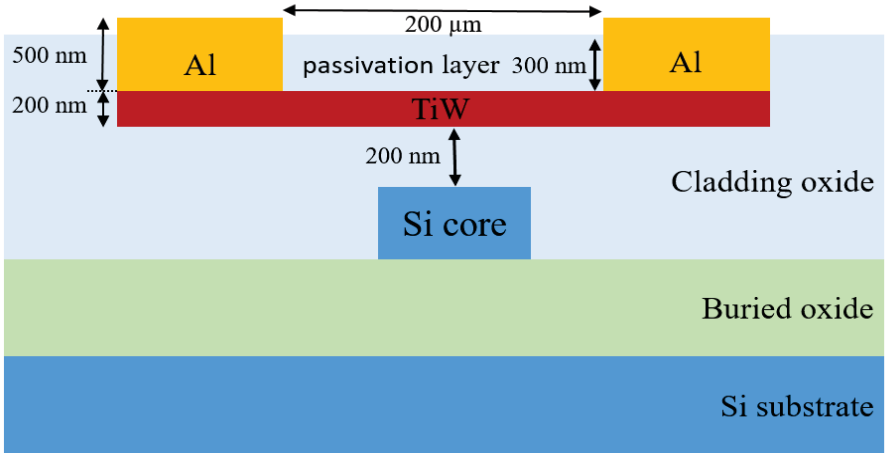

Figure 3.3: Cross-sectional view of the proposed thermo-optic heater.

This bi-layer junction allows good conductivity on the conduction part, and the majority of the heat generated on the targeted device area of the chip. Titanium-tungsten/Aluminum bi-layer is also used as the routing channel to ensure good electrical conduction between the Aluminum (Al) routing layer and TiW heater layer, which reduce contact resistance and improves uniformity. A 300 nm thick silicon dioxide SiO_2 passivation layer is used to protect the thin metal heater from oxidation damage and this oxide layer is etched away to create the windows over the Aluminum pads to allow electrical wire bonding or probing.

Based on the design specification discussed above, a detailed simulation has been conducted using the Lumerical Device and MODE. A cross sectional view of the simulated 2D thermal field profile of the wafer as a function of waveguide width is shown in figure 3.4(a). For a π-phase shift, 1.2 volts are required to heat the waveguide through the proposed heater in simulation (figure 3.4(b)).

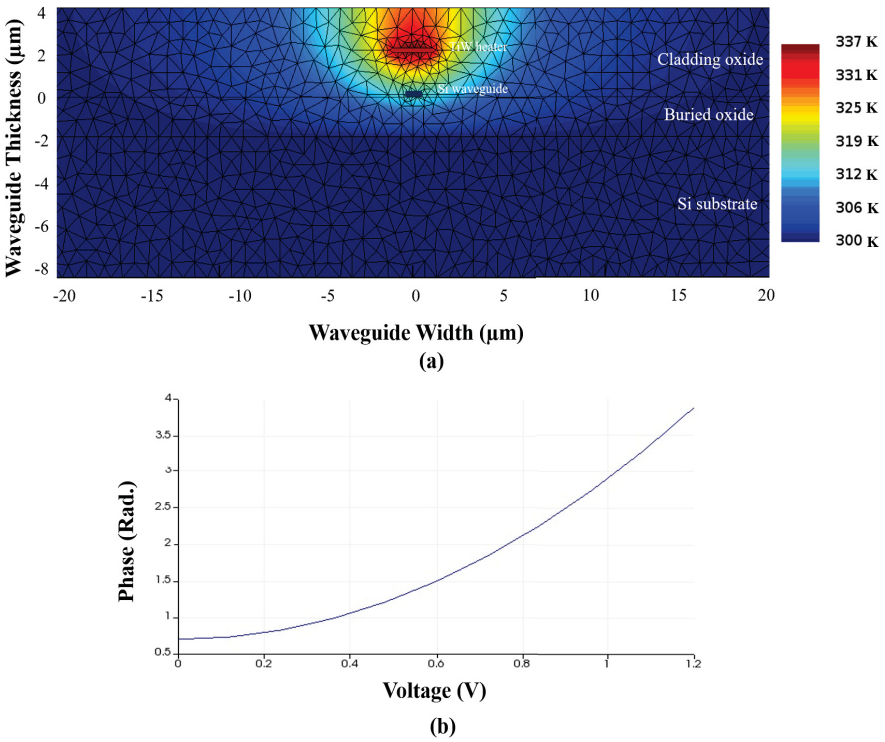

Figure 3.4: (a) Cross sectional view of the simulated 2D Thermal field profile with mesh as a function of waveguide width; (b) phase versus voltage curve of the designed heater.

3.2 Experimental Setups

Both Continuous wave (CW) and payload data transmission (RF) measurements are done to characterize the MMI and MZI building blocks, as well the designed switch matrices. First, CW measurement has been done to find the on-chip insertion loss and the crosstalk for all possible switching channels. Then, RF measurement is demonstrated to show the switching performance in a payload data transmission environment. Both eye diagrams and BER curves have been generated to analyze the payload data transmission.

3.2.1 Continuous Wave (CW) Measurement Setup

A C-band tunable laser is used to perform the continuous wave (CW) measurements. A polarization controller (PC) is connected to the output of the laser source to maintain the on-chip polarization of the optical signal to a quasi-TE optical mode. The optical signal is coupled into the chip through a grating coupler with another grating coupler used at the output of the chip as shown in figure 3.5. The output is measured by an optical power meter. An on-chip loopback structure that contains two grating couplers with a short waveguide is measured. The loss is -17 dB at 1550 nm, used to normalize all the CW measurements.

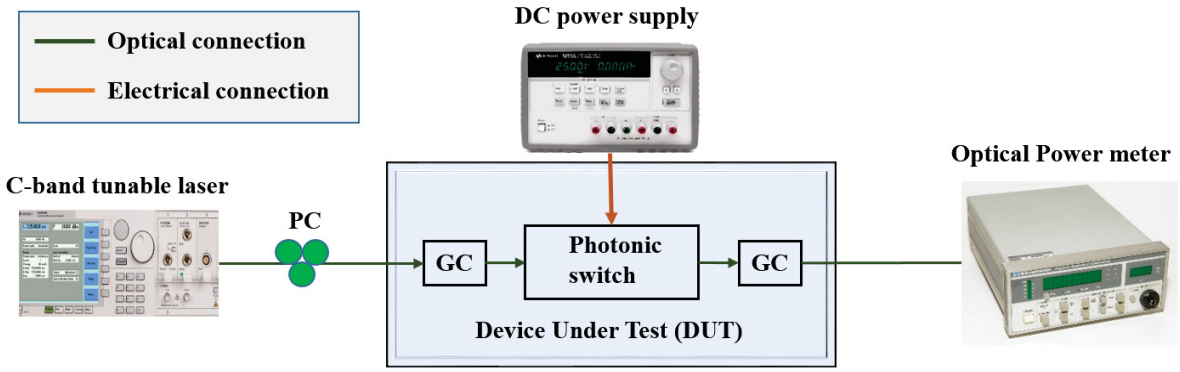

Figure 3.5: A schematic diagram of the CW experimental setup.

3.2.2 Payload Data Transmission (RF) Measurement Setup

Payload transmission is performed to demonstrate the switching performance within a real data transmission system as depicted in figure 3.6. The C-band tunable laser's output is connected to a modulator with 12.3 GHz 3 dB RF bandwidth through a polarization

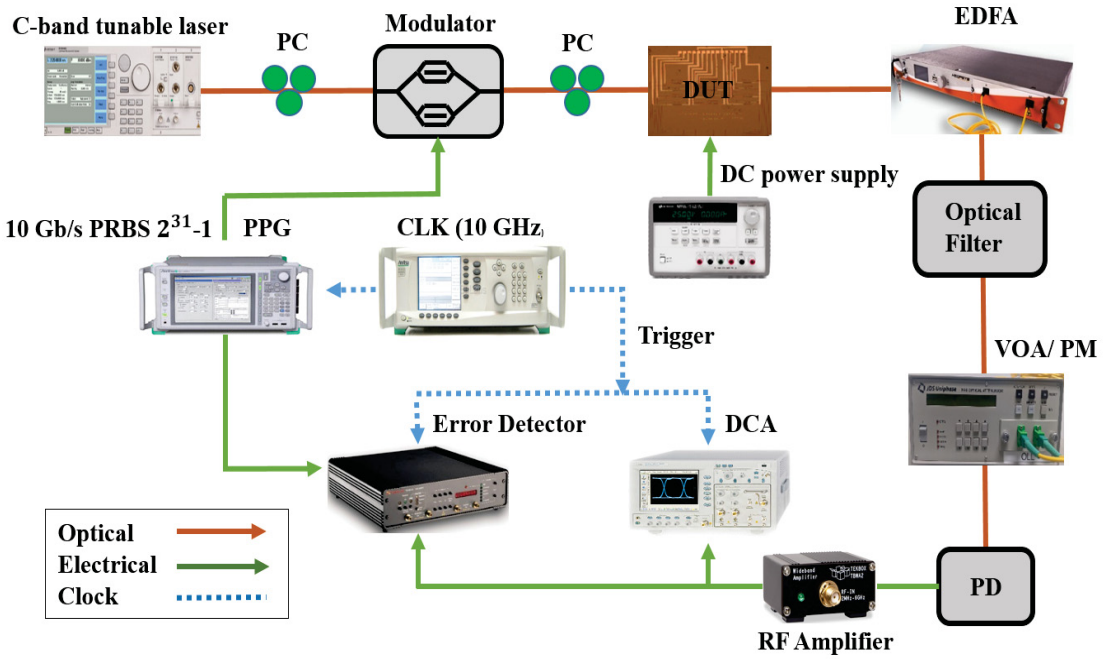

Figure 3.6: Experimental setup of the switch (DUT) for 10 Gb/s data transmission. PC: Polarization Controller; EDFA: Erbium Doped Fiber Amplifier; DC: Voltage Supply; PPG: Programmable Pattern Generator; CLK: Clock synthesizer; ED: Error Detector; DCA: Digital Communication Analyzer; VOA/PM: Variable Optical Amplifier/Optical Power Meter; RF Amp: RF Amplifier.

controller (PC). The 1550 nm CW signal is modulated by a 10 Gb/s NRZ PRBS-31 signal from a pulse pattern generator (PPG). The modulated signal passed through another PC to the DUT chip (device under test) where light is coupled by a grating coupler. The DUT output signal is amplified by an Erbium-doped fiber amplifier (EDFA) to compensate for the device's insertion loss. Then, it passes through a C-band tunable filter with 0.5 dB bandwidth at 0.8 nm to reduce the unwanted ASE noise generated by the EDFA. A variable optical attenuator (VOA) is combined with an optical power meter in the same module used

to maintain the optical power at the sensitivity level ($\simeq$ 20 dBm) for the photodetector (PD). After the PD, the RF signal is amplified by an RF signal amplifier with 3 dB of gain then to a Digital Communication Analyzer (DCA) and an Error Detector (ED) module to capture the eye diagram and bit error rate (BER), respectively. A synthesized clock (CLK) synchronizes the PPG, ED, and DCA.

3.3 Low Loss 2 $\times$ 2 Thermo-optic MZI

Mach-Zehnder interferometer (MZI) is one of the most widely used phenomena in silicon photonic switches. The transmission characteristic of the MZI switch depends on the power splitting and coupling ratio of the directional coupler (DC) or the MMI, and the phase difference of the traveling light in two arms. The MZI may have balanced or unbalanced arms based on their applications shown is figure 3.7. In our proposed switch, MZIs have balanced paths with a thermal heater, which can tune the phase difference between two paths. Typically, the phase difference can be expressed at a specific wavelength λ,

$$\Delta\varphi = \beta_1 l_1 - \beta_2 l_2 = \frac{2\pi}{\lambda}[n_{eff1} l_1 - n_{eff2} l_2] \tag{3.1}$$

Where, β_1 and β_2 represent the propagation constants, n_{eff1} and n_{eff2} are the effective indices and l_1 and l_2 are the waveguide length of two MZI arms respectively. For balanced path, $\beta_1 l_1 = \beta_2 l_2$, so $\Delta\varphi$ should be zero (0) while no phase shift.

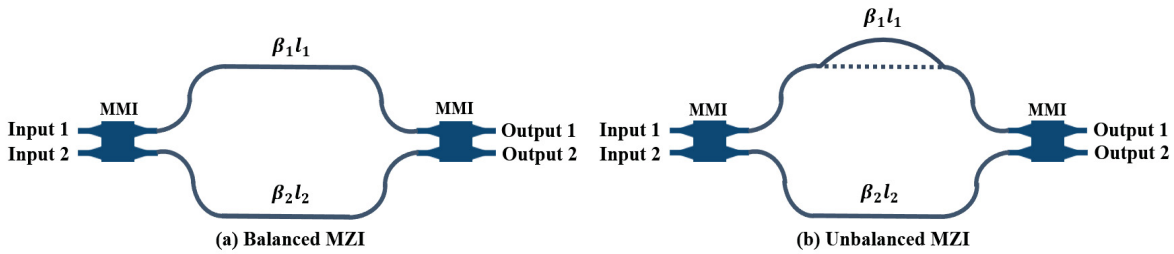

Figure 3.7: 2 × 2 MZI; (a) balanced MZI ($\beta_1 l_1 = \beta_2 l_2$); (b) unbalanced MZI ($\beta_1 l_1 \neq \beta_2 l_2$).

3.3.1 Design and Simulation

Our proposed 2 × 2 MZI switch consists of two MMI as 3 dB splitter/coupler and a dual-waveguide balanced arm to connect them as shown in figure 3.8(a). One of the arms has a phase shifter able to change the phase difference between two arms from 0 to π by thermally changing the Si refractive index. As we discussed before, 200 µm long and 5 µm wide Titanium-tungsten (TiW) heater is designed as a phase shifter placed between the two MMIs and 2 µm above one of the MZI balanced paths. The MMI is designed by Lumerical MODE and FDTD and the 2 × 2 MZI switch is characterized by Lumerical Interconnect using the S-parameter abstracted from Lumerical MODE and FDTD. S-parameter means the scattering parameter which describes the response of an N-port network to signal(s) incident to any or all of the ports.

We abstract the S-parameters of the switching elements from the Lumerical FDTD and import it to Lumerical Interconnect. Using the component model library along with the corresponding S-parameters in Lumerical Interconnect, we make the circuit model of the switch to demonstrate the switching characteristics of the switch using the Optical Network

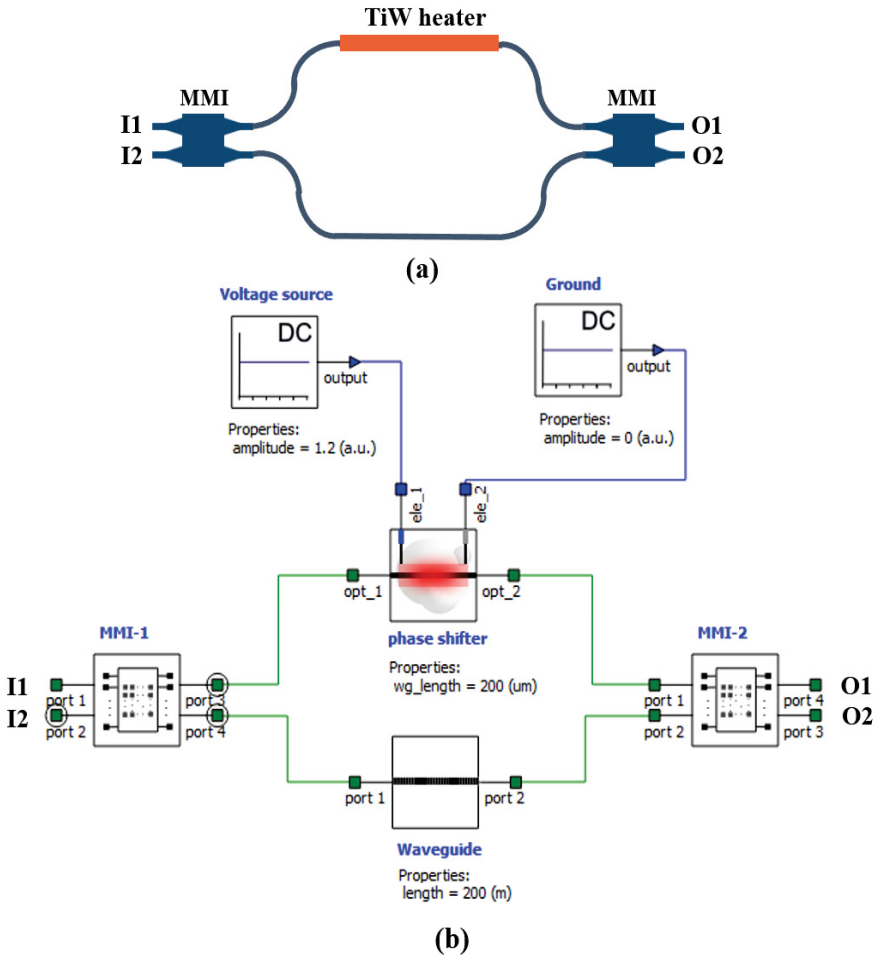

Figure 3.8: 2 × 2 MZI switch; (a) schematic architecture of 2 × 2 MZI switch; (b) corresponding circuit model using Lumerical Interconnect.

Analyzer (ONA). The insertion loss is measured 0.43 dB with a crosstalk of at least 30 dB when 0 dB optical power is applied to the input ports at 1550 nm. In this simulation, we use only two MMI and a phase shifter as a building block without considering the waveguide propagation loss, which is 3.5 dB/cm measurement measured by the fabricator.

3.3.2 CW and RF Measurements Results

For characterization, the continuous wave (CW) measurement setup is used to measure the insertion loss and crosstalk. The MZI with the thermal phase shifter works as a 2 × 2 thermo-optic switch and exhibits 0.6 dB insertion loss with crosstalk less than -24 dB over the wavelength range from 1500 nm to 1600 nm. The minimum extinction ration (ER) is measured approximately 20 dB at bar port. The electrical power dissipated by the 2 × 2 MZI building block for the 'ON' state and 'OFF' state is 34.8 mW and 4.8 mW respectively. Thus, the required 30 mW/π-phase shift represents a V_π of 1.6 V as shown in figure 3.9.

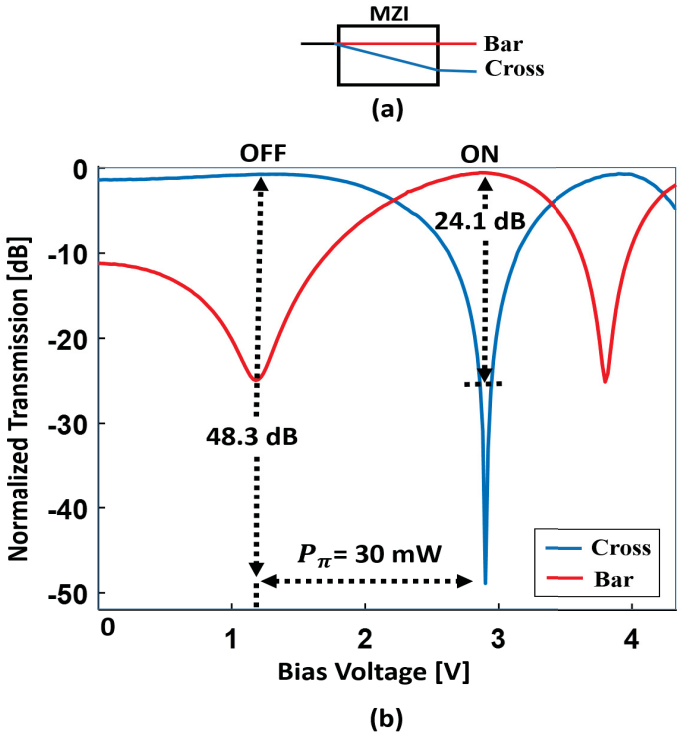

Figure 3.9: (a) Schematic of bar and cross ports; (b) experimentally demonstrated optical transmission as a function of bias voltage for the 2 × 2 MZI switch at 1550 nm.

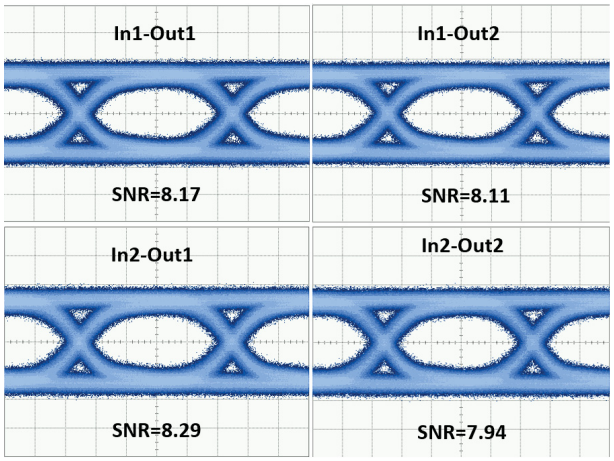

Figure 3.10: Eye diagram of the 2 × 2 MZI switch for both the corresponding outputs (100 mV/div) with the data at input port I1 and I2.

Payload transmission is then experimentally performed to demonstrate the switching performance using the setup discussed before. The corresponding output eye diagrams for input I1 and I2 to both outputs are shown in figure 3.10 for 10 Gb/s payload signal transmission. Clear open eye diagrams are observed for all the routing channels with a signal-to-noise ratio (SNR) of at least 7.9 at a BER of 10^{-10}.

The corresponding bit error rate (BER) power penalties are shown in figure 3.11 for input-1 to both outputs at the BER of 10^{-10}. The back-to-back BER is measured without connecting the device, using the same setup. The power penalty varies with routing paths with a worst-case (best case) power penalties are 0.5 dB (0.3 dB) for the 2 × 2 MZI switch.

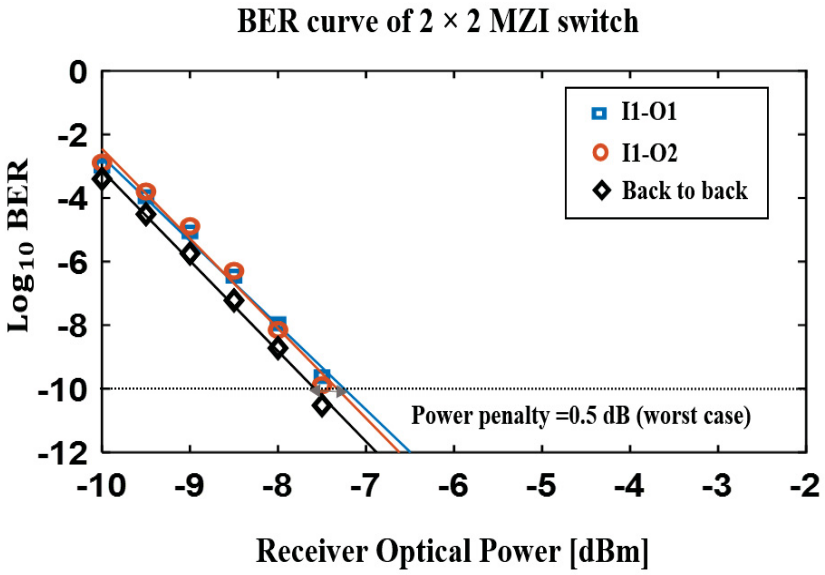

Figure 3.11: Logarithmic BER as a function of received optical power for input I1 to both outputs and back-to-back connection for 2 × 2 MZI switch.

3.4 4 × 4 Thermo-optic Switch

Using the 2 × 2 MZI switch as a building block and waveguide crossing from SiEPIC process design kit (PDK) we have designed and simulated the low loss 4 × 4 thermo-optic switch matrix.

3.4.1 Design and Simulation

Banyan blocking topology is used to design the 4 × 4 switch where two stages of cascaded thermo-optic MZI is employed to realize the switching as shown in figure 3.12(a). In figure 3.12(b), the corresponding circuit model is illustrated using Lumerical Interconnect to

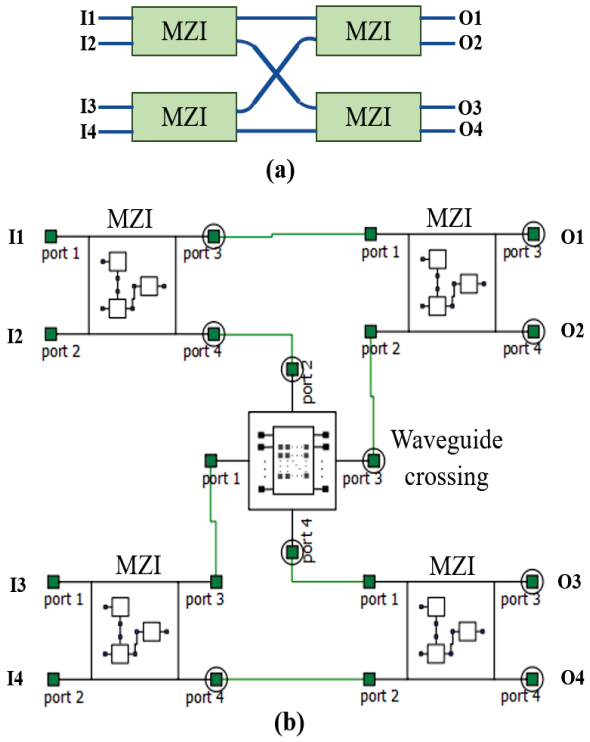

Figure 3.12: 4 × 4 Banyan switch; (a) schematic architecture of the 4 × 4 MZI switch; (b) corresponding circuit model using Lumerical Interconnect.

simulate the switch. An Optical Network Analyzer (ONA) from the component model library measure the transmission characteristics of this switch at 1550 nm. Four 2 × 2 MZI thermal switches and a waveguide crossing are used as building blocks in the 4 × 4 Banyan switch. The insertion loss is measured to be 0.86 dB and 1.2 dB for the shortest, and longest path, respectively with a crosstalk of at most 30 dB at 1550 nm when 0 dB optical power inserts into the input-1.

3.4.2 CW and RF Measurements Results

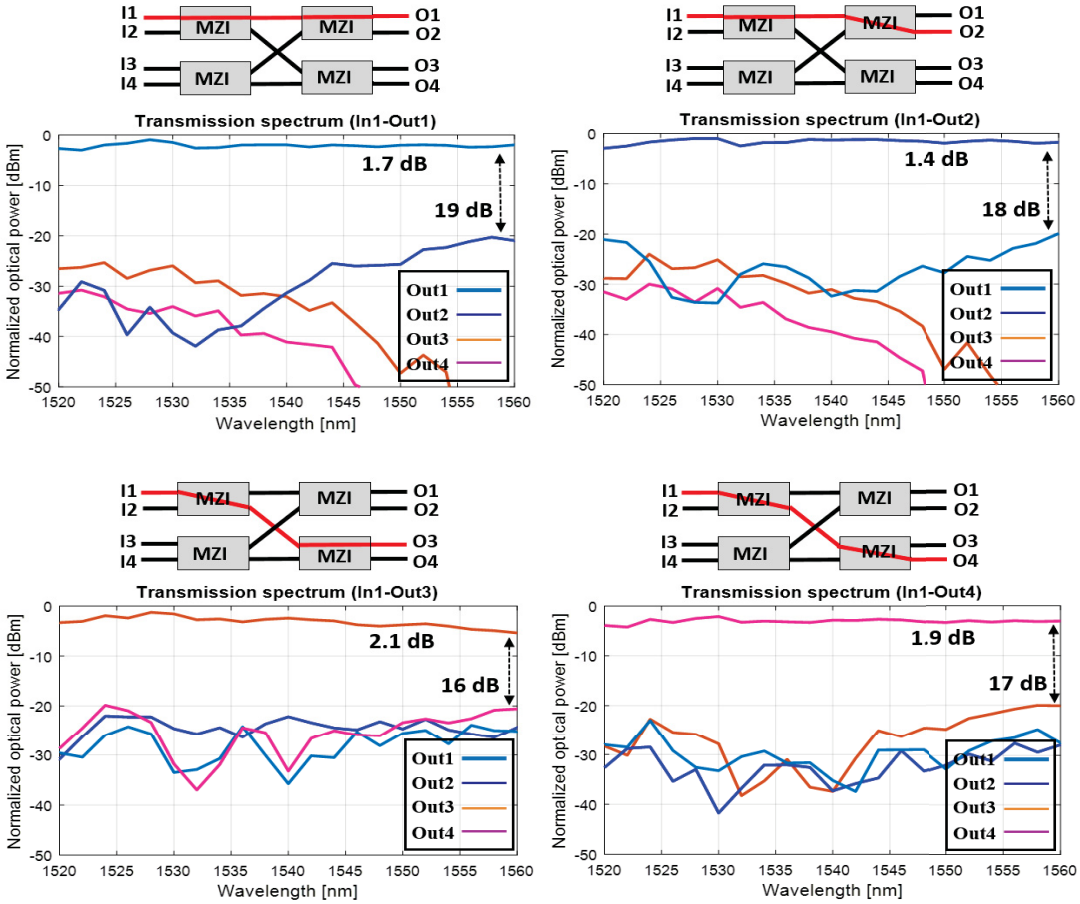

Figure 3.13: Switching channels and corresponding normalized transmission spectrum of the 4 × 4 thermal switch within the wavelength range from 1500 nm to 1600 nm.

Continuous wave (CW) measurement is performed to find the loss and crosstalk for all the output ports at 1550 nm. At 1550 nm, the insertion loss measured for the shortest switching path (I1-O1) of the 4 × 4 switch is less than 1.4 dB and approximately 2.1 dB for the longest path (I1-O4) as depicted in figure 3.13. The worst crosstalk recorded is -16 dB. If all the phase shifters are active ('ON state'), the total power (energy) consumption of the 4 × 4

thermal switch is measured to be 139 mW (3.5 pJ/bit).

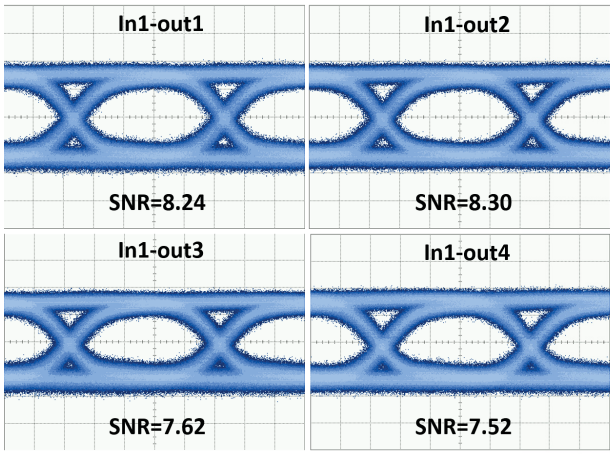

Figure 3.14: Eye diagram of the 4 × 4 Banyan switch for all the corresponding outputs (100 mV/div) with the data at input port I1.

After the CW measurement, the payload transmission is performed. Clear open eye diagrams are observed for input-1 to all the output ports for 10 Gb/s payload signal transmission as shown in figure 3.14. The minimum signal-to-noise ratio (SNR) is measured 7.5 at a BER of 10^{-10}. We measure eye diagrams for all the corresponding ports. As the SNR are similar, thus we only show the eyes for Input-1 to all outputs.

Figure 3.15 shows the corresponding bit error rate (BER) and BER power penalties for input-1 to all of the output ports of 4 × 4 Banyan switch at a BER of 10^{-10}. For the shortest (best case) routing path, the power penalty is measured 0.4 dB; while in the longest channel, the worst-case power penalty is observed 0.7 dB. The power penalties come from the insertion loss and grating couplers of the device.

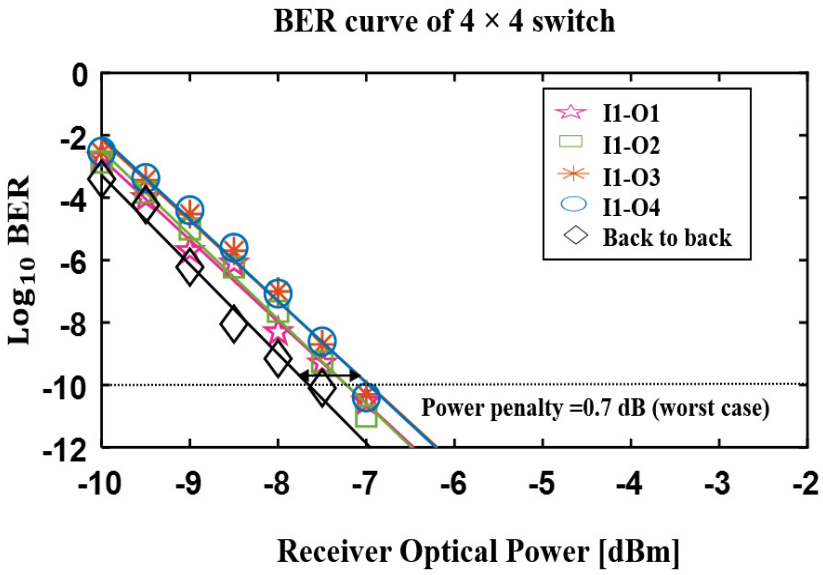

Figure 3.15: Logarithmic BER as a function of received optical power for input I1 to all outputs and back-to-back connection for 4 × 4 Banyan switch.

3.5 8 × 8 Thermo-optic Switch

The 8 × 8 thermal switch is designed using a Banyan topology for a more relaxed optical power budget at the cost of a blocking behavior. Such blocking switches can be used in interconnect switches for WDM-based networks where the controller accounts for blocking scenarios. The mask layout of the switch is drawn by using KLayout and the device is fabricated through Applied Nanotools Inc. (ANT) through the SiEPIC consortium. Both CW and payload measurements have been done to analyze the switching behaviors of the switch.

3.5.1 Design and Simulation

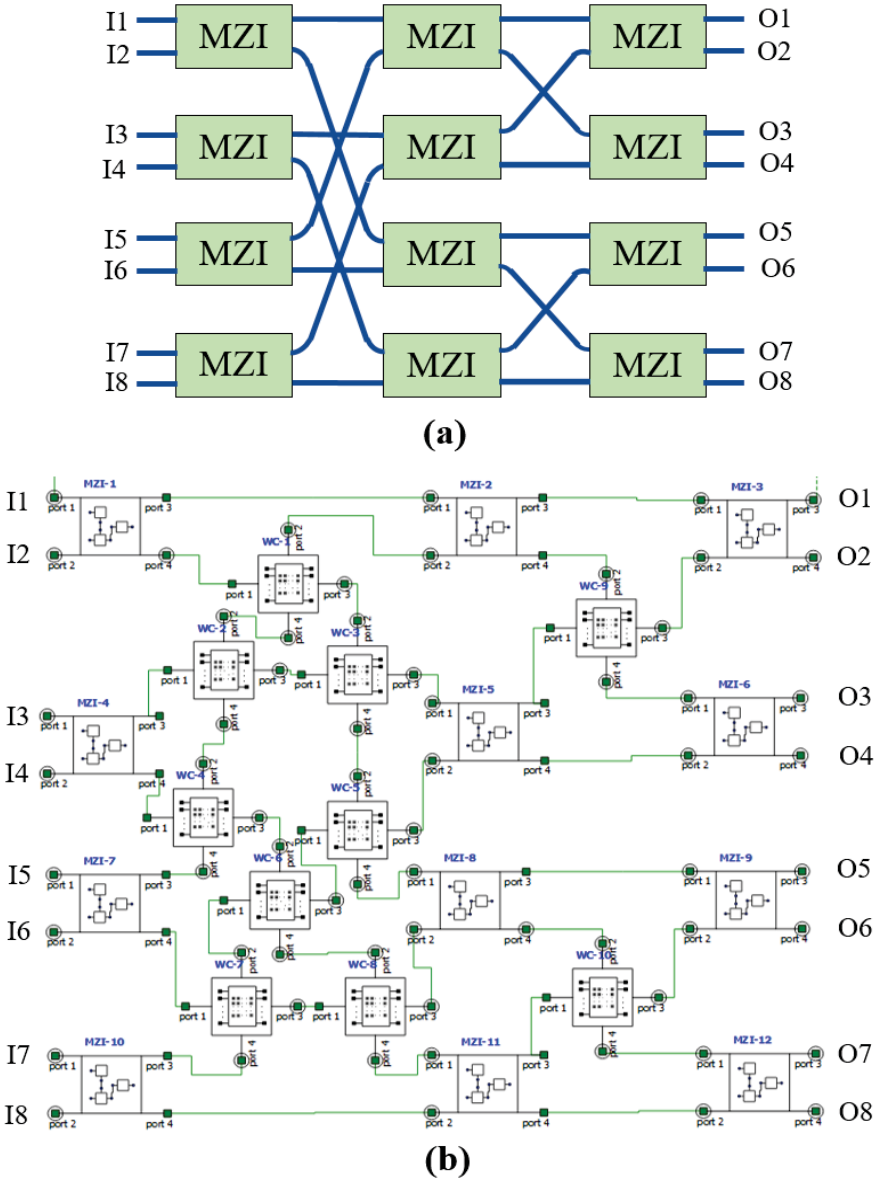

Figure 3.16: 8 × 8 switch matrix; (a) schematic structure of the 8 × 8 switch; (b) corresponding circuit model of the 8 × 8 switch matrix using Lumerical Interconnect.

We use the same 2 × 2 MZI building block discussed before to design the low loss 8

× 8 Banyan switch matrix. The waveguide crossing (WC) used in this switch is available in the SiEPIC PDK, guaranteeing less than 0.3 dB optical insertion loss per crossing. The schematics and the circuit model of the 8 × 8 switch matrix using the Lumerical Interconnect are shown in figure 3.16(a) and (b), respectively.

Using the S-parameters abstracted from Lumerical FDTD for the MMI and waveguide crossing, we have designed the circuit model using Lumerical Interconnect to simulate the transmission characteristics of the switch. The MZI used in the circuit model comprises two MMIs and a phase shifter. The bias voltage of each phase shifter is 1.2 volt/π-phase shift. The insertion loss is 1.3 dB and 2.5 dB for the shortest and longest channels, respectively, with a maximum crosstalk of 30 dB, while 0 dBm optical power travels from input-1 to all the output ports at 1550 nm. The loss and crosstalk are measured based on the S-parameter of MMI and waveguide crossing without considering the waveguide propagation loss. Therefore, the loss will increase slightly due to the waveguide propagation loss, sidewall roughness, backscattering, and fabrication imperfection.

3.5.2 CW and RF Measurements Results

The continuous wave (CW) measurement has been done to demonstrate the DC performance of the switch. For the 8 × 8 Banyan switch, light passes through three cascaded MZIs as shown in figure 3.16(a). The scanning electron microscope (SEM) image of the fabricated 8 × 8 switch matrix is shown in figure 3.17. The insertion loss of the shortest switching

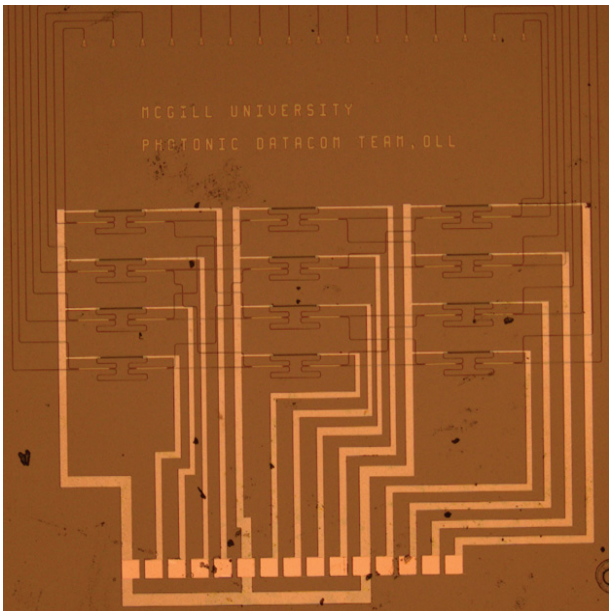

Figure 3.17: The scanning electron microscope (SEM) image of the fabricated 8 × 8 Banyan switch.

path (I1-O1) is measured to be less than 3.1 dB with no waveguide crossing employed. For the longest path (I1-O8), which includes four waveguide crossings, the insertion loss is approximately 5.0 dB. Insertion loss measured approximately 0.3 dB for each crossing. The maximum crosstalk measured is at most -20.5 dB over the wavelength range from 1515 nm to 1585 nm. The 3 dB bandwidth of this switch is 25 nm. When all the phase shifters are in 'ON' state, the total power (energy) consumption of the 8 × 8 thermal switches is estimated at approximately 417 mW (5.2 pJ/bit), enabling further scalability for the greater port count.

All the building blocks are measured individually. Table 3.1 shows an estimate of insertion losses for the longest path of the 8 × 8 Banyan switch based on the measurement results of

Table 3.1: The estimation of insertion losses for the longest path of the 8 × 8 switch

Building block	Unit loss (dB)	Quantity	Total (dB)
2 × 2 MZI cell	0.6	3	1.8
Waveguide length (mm)	0.38	5	1.9
Waveguide Crossing	0.3	4	1.2
Total maximum on-chip loss	—	—	4.9

the building blocks. The measured loss of the 8 × 8 switch is inline with the estimate, which allows us to scale the number of ports though simulation.

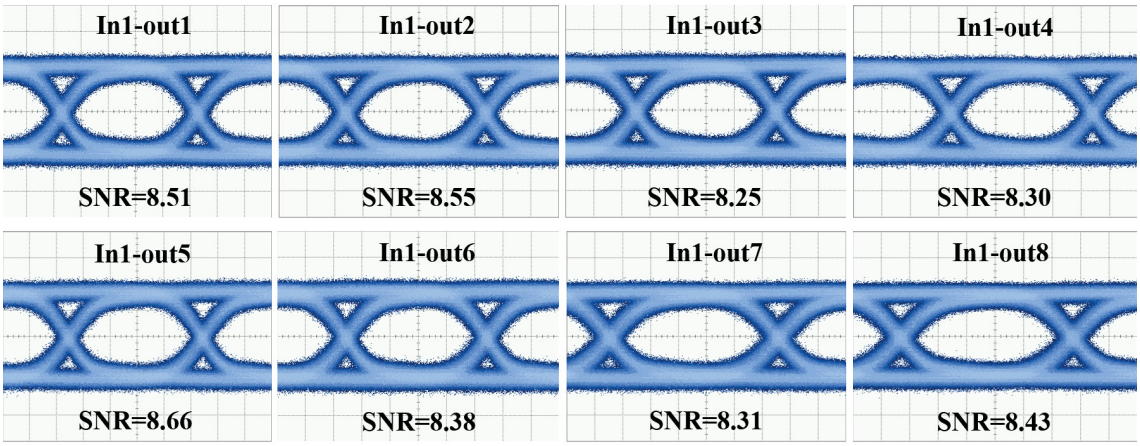

Figure 3.18: Eye diagram of the 8 × 8 Banyan switch for all the corresponding outputs (100 mV/div) with the data at input port I1.

The corresponding output eye diagrams are measured for 10 Gb/s payload signal transmission. In figure 3.18, clear open eye diagrams are observed for input-1 to all output ports with a signal-to-noise ratio (SNR) of at least 8.2 at a BER of 10^{-10}. Due to limited number of ports in fiber array, we could not measure eye diagrams for all the corresponding inputs. The grating coupler and corresponding fiber array used for the 8 × 8 switch is less

lossy (-8.5 dB) and more stable than the ones used for the 4 × 4 and 2 × 2 switches (-11 dB) due to different polished angles. Consequently, testing the 8 × 8 switch requires less gain from the EDFA leading to better eye diagrams and SNR in the payload transmission.

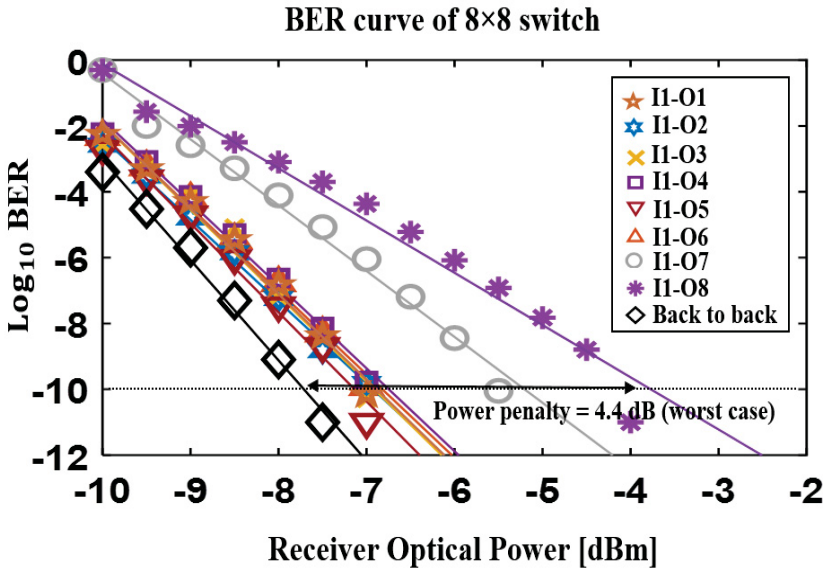

Figure 3.19: Logarithmic BER as a function of received optical power for input I1 to all outputs and back-to-back connection for 8 × 8 Banyan switch.

The relative bit error rate (BER) power penalties are also measured for input-1 to all the outputs ports at the BER of 10^{-10} as shown in figure 3.19. For the shortest routing path the power penalty is 0.5 dB, while the worst power penalty is found 4.4 dB for the longest routing path. In the 8 × 8 switch, the longest paths (I1-O7 and I1-O8) have more crossings leading to higher loss, as well as possible additional coupling loss from the fiber array due to the larger distance between input port I1 and output ports O7 and O8.

For NRZ PRBS31 transmission, BER below 10^{-12} is usually considered as error-free

payload transmission in the literature. The BER for the presented optical switches decreases with the received optical power and eventually goes below 10^{-12}. However, due to the experimental testbed limitations, we did not continue measuring the BER for values below 10^{-10}. The BER tester used for our measurement was placed on a non-floating optical table and the waiting time to get a stable reading was more than one minute. This is one of the reasons why we could not go below 10^{-11} even for the back-to-back scenario. Finally, the clear eye and BER curve show strong evidence that this switch is compatible with wavelength division multiplexing (WDM) systems with low power penalty and error-free data transmission (10^{-10}).

3.6 Ultra-broadband and Low Loss 16 × 16 Thermo-optic Switch

The bottleneck of a large radix photonic switch matrix is its high optical loss and cascaded bandwidth from multiple stages. Thus, designing a broadband and low loss building block is one of the most challenging tasks to realize an efficient large radix switch matrix for wavelength-division multiplexing (WDM) systems. In this section, a Mach-Zehnder Interferometer (MZI) based scalable 16 × 16 thermo-optic Banyan blocking switch is demonstrated as shown in figure 3.20.

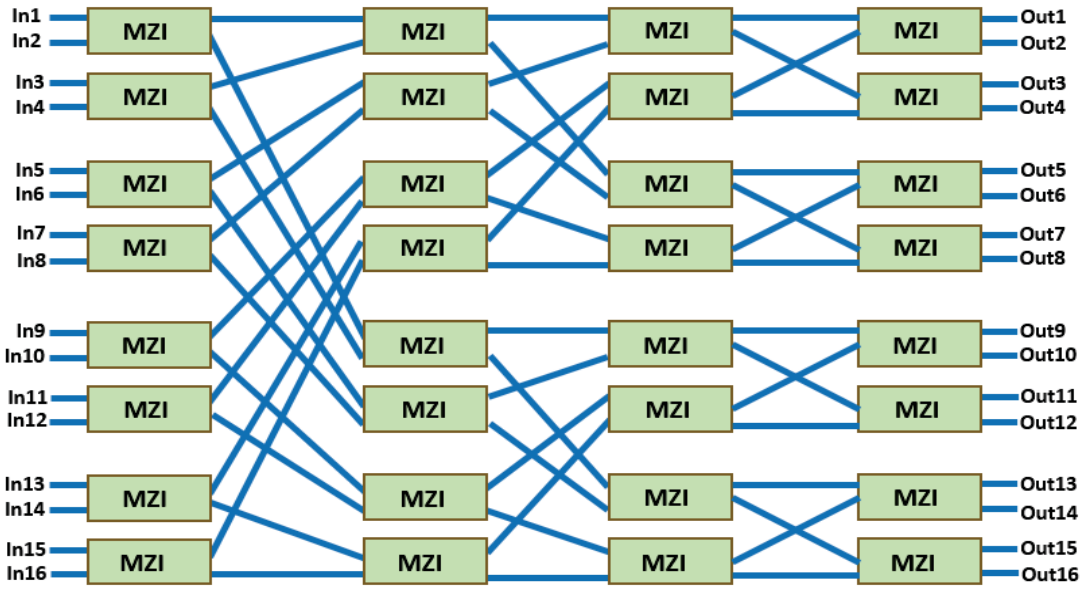

Figure 3.20: 16 × 16 Banyan blocking topology.

3.6.1 Design of the Ultra-broadband 2 × 2 MMI

In this section, we have further optimized our MMI used in the previous switches. The optimization is done by changing the taper length, width, and the distance between two taper precisely using Lumerical optimization tools. After optimization, the 3 dB bandwidth of this MMI increases significantly from 90 nm to 500 nm. Using this optimized MMI, a low loss and broadband 2 × 2 and 16 × 16 thermo-optic switches have been designed.

The MMI is optimized for broadband and low loss operation; the power-splitting ratio is 50/50 as well. The taper length, width, and taper position have been changed to optimize the MMI, improving the bandwidth and splitting ratio of the MMI. Considering the self-imaging properties of silicon waveguide, a 0.22 μm thick, 6 μm wide and 131 μm long 2 ×

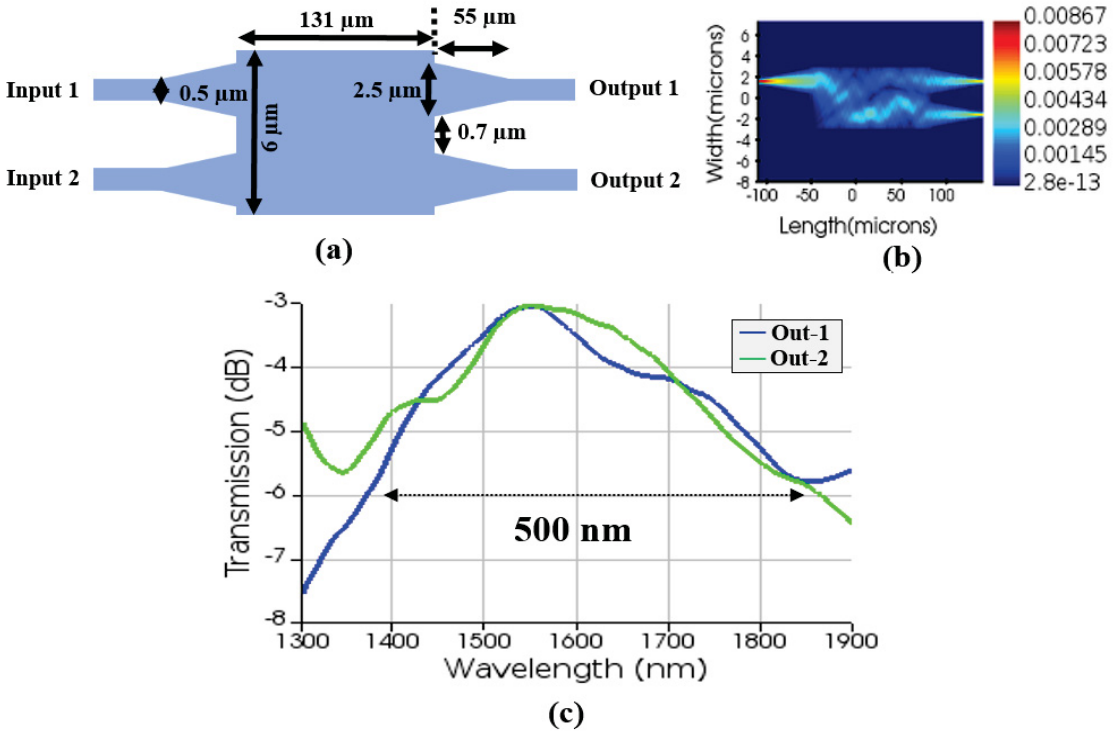

Figure 3.21: 2 × 2 Broadband MMI: (a) schematic of the 2 × 2 MMI; (b) optical field profile of the MMI; (c) simulated broadband spectrum response of the 3 dB MMI splitter/coupler.

2 MMI core has been designed using the Eigen-Mode Expansion (EME) solver in Lumerical MODE, same as the previous designs. The slab waveguides used to connect each component have a width of 0.5 μm tapered to 2.5 μm over a 55 μm length before connecting with the MMI core to reduce the insertion loss between the MMI core and the connecting waveguides that also increase the bandwidth of the MMI as shown in figure 3.21(a). In figure 3.21(b) optical field profile inside the MMI has been shown when light comes from input-1. In the simulation, this optimized MMI is offering around 500 nm of 3 dB bandwidth with 0.034 dB insertion loss (IL) at 1550 nm as shown in figure 3.21(c).

3.6.2 Ultra-broadband 2 × 2 MZI Switch

In this section, the optimized MMI discussed in the previous section is used to design the ultra-broadband and low loss MZI switch. This design consists of two 3 dB MMI splitter/combiner as build blocks to realize the ultra-broadband and low loss 2 × 2 MZI switch as shown in Figure 3.22(a).

Using the S-parameter of the MMI abstracted from Lumerical MODE, this MZI is simulated through Lumerical Interconnect. In the simulation, around 403 nm bandwidth is found from 1387 nm to 1790 nm of wavelength range with less than 0.16 dB insertion loss at 1550 nm. Experimentally, the 2 × 2 thermo-optic MZI exhibits less than 0.3 dB of insertion loss with a crosstalk of at most 19 dB over a 1 dB bandwidth range more than 100 nm as shown in Figure 3.22(c). This switch is characterized within a narrow wavelength range of 1500 nm to 1600 nm due to the limitation of tunable laser source and the grating coupler. The experimentally demonstrated optical transmission as a function of bias voltage for the 2 × 2 MZI switch at 1550 nm is shown in Figure 3.22(b). The electrical power consumption per MZI is measured at approximately 24 mW/π-phase shift.

The payload transmission (RF) is also performed to demonstrate the switching performance in a real data transmission systems. In all scenarios, a clear open eye is found with a good SNR for 10 Gb/s payload signal transmission as shown in Figure 3.22(c) (insets).

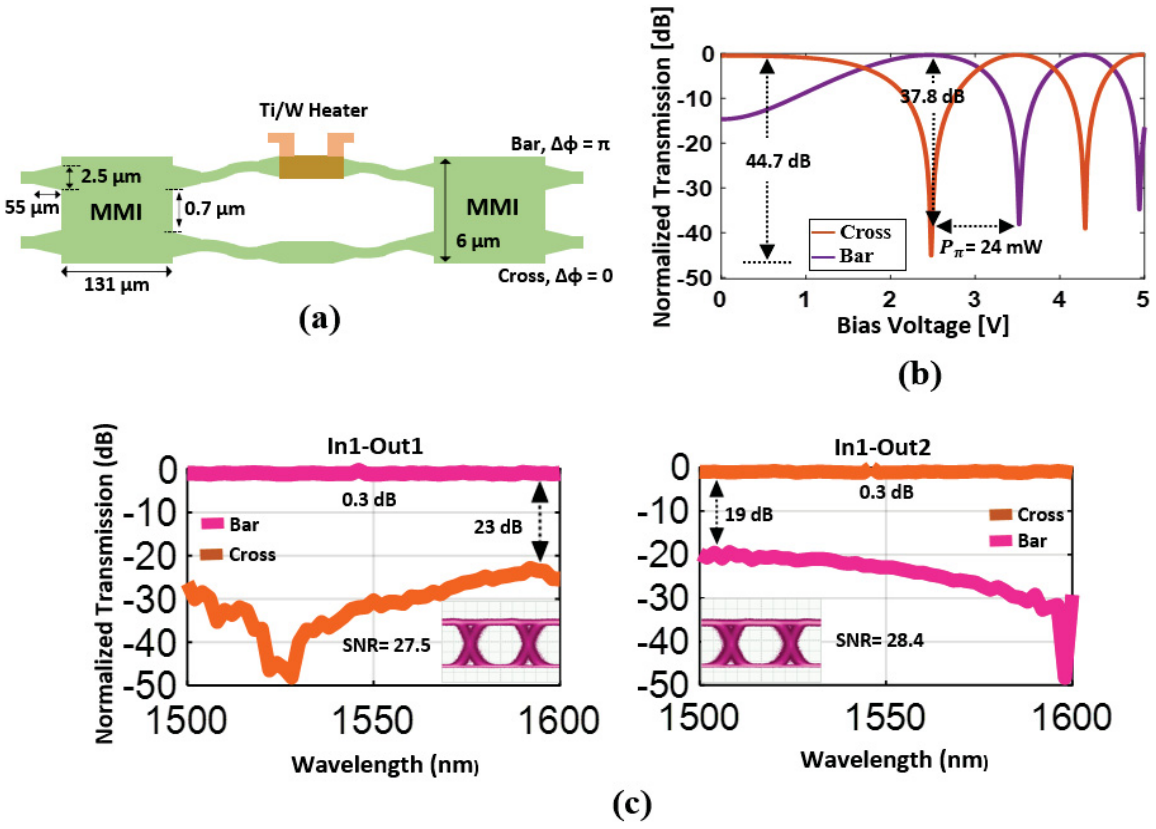

Figure 3.22: Optimized 2 × 2 broadband MZI switch; (a) schematic of the MZI building block; (b) experimentally demonstrated optical transmission as a function of bias voltage for the 2 × 2 MZI switch at 1550 nm.; (c) measured transmission spectrum and 10 Gb/s eye diagram (insets) of the 2 × 2 MZI switch (1.07 mW/div).

3.6.3 Experimental Results of 16 × 16 Ultra-broadband Switch

Optical bandwidth limitation is a severe concern for large radix switches. Due to multiple stages of building blocks, the bandwidth decreases. In this section, we use the broadband and low loss MMI to realize the broadband and low loss response from the 16 × 16 switch

matrix. To characterize the switching performance, both CW and RF measurements are done using the same setup discussed at the beginning of this chapter.

For 16 × 16 Banyan switch, each channel consists of four cascaded MZI building blocks as shown in figure 3.20. In figure 3.23, the transmission spectrums from Input-1 to all output ports of the 16 × 16 switch are demonstrated. The insertion loss is approximately 2.1 dB with a crosstalk of at most 8 dB over a wide range of 100 nm (1500 nm to 1600 nm) for the shortest channel (I1-O1) where no waveguide crossing is used. In the longest switching channel (I1-O16), the insertion loss increases to 3.8 dB with a crosstalk of at most 10 dB within the same wavelength range where eleven waveguide crossings are used, and each has 0.02 dB insertion loss. This waveguide crossing is designed and measured by Canadian Microsystems Corporation (CMC) and available as CMC PDK. All switches are characterized from 1500 nm to 1600 nm limited by the tunable laser source and the grating coupler. If all the phase shifters work simultaneously ('ON state'), the total electrical power consumption is estimated to be 1.1 W (6.9 pJ/bit). The experimental results of 16 × 16 switch is summarized in table 3.2.

Table 3.2: Experimental summary of the 16 × 16 switch for input 1

Output	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
IL (dB)	2.1	2.3	2	2.1	2.8	2.6	2.7	2.3	3.1	2.9	3.2	3.3	3.5	3.3	3.6	3.8
XT (dB)	8	15	11	16	8	8	9	9	10	14	11	10	12	13	11	10
SNR	23.1	22.7	22.9	22.6	22	22.8	22.4	22.4	23.2	23.5	21.8	20.7	21.5	22.4	21.4	22

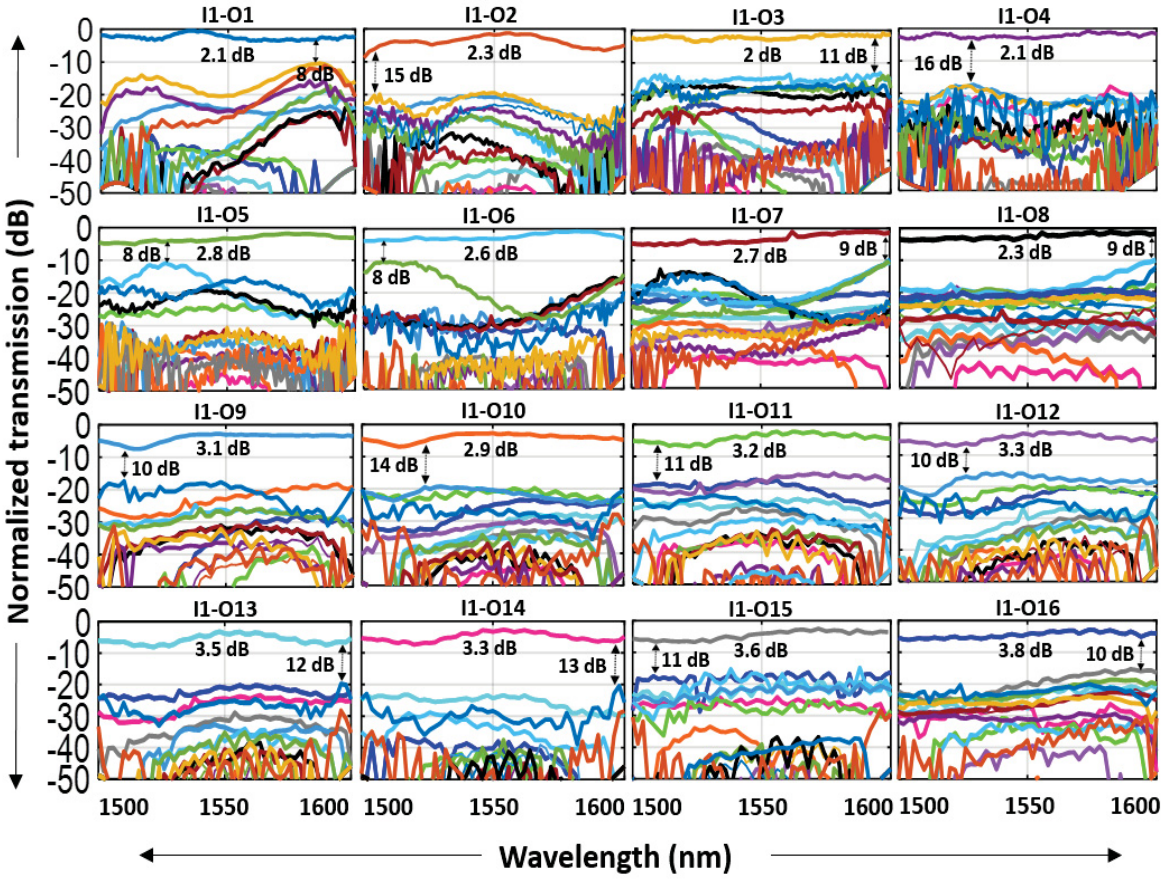

Figure 3.23: Normalized transmission spectra of the 16 × 16 switch for light path from input-1 to all output ports.

The payload transmission is also performed to demonstrate the switching performance in a real data transmission system. A clear open eye is observed for all scenarios. In figure 3.24, eye diagrams are shown for input-1 to all output ports with a good signal-to-noise ratio for 10 Gb/s payload signal transmission. The SNR is different than previous switches because of the different amplitude (power) and rise time (ms) of eyes. The fiber array used in this measurement is limited by port number. Thus, we could not measure all the ports

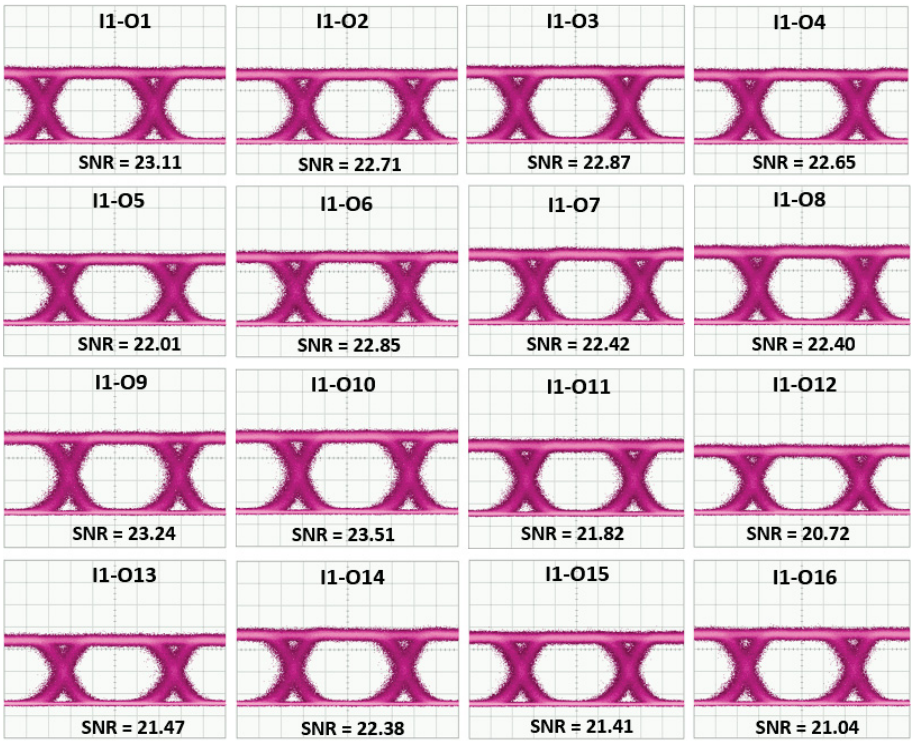

Figure 3.24: Eye diagram of the 16 × 16 Banyan switch for all the corresponding outputs (1.07 mV/div) with the data at input port I1.

during CW and RF measurement. However, as the switch is symmetric, bidirectional and most of the ports are measured, it is predicted that, performances for other ports should be laid between the results of the shortest (I1-O1) and longest (I1-O16) paths.

3.7 Conclusion

Several switching matrices using Banyan blocking topology have been designed and experimentally demonstrated for low loss and broadband operation. The optimized MMI

building blocks allow greater port count with better insertion loss and bandwidth. The CW and payload transmissions representing the switching performance in WDM networks and the power efficient larger radix switches with low loss and broadband response validate further scalability of these switches.

Chapter 4

SiPh Multimode Switches

MDM is one of the most effective techniques to transmit data with a low power consumption, as less number of laser sources are required compared to other techniques. Thus, multimode switching topology adds a new dimension of freedom for extended bandwidth. In this chapter, we propose a novel design of mode insensitive 3×3 and 4×4 switch for the first two quasi-transverse electric (TE) modes, having low insertion loss, low intermodal crosstalk, and low power consumption with a dynamic control in MDM networks.

4.1 3×3 Mode Insensitive Switch

Conventional multimode switching matrices use demultiplexing-processing-multiplexing technique, where processing works based on single mode switching topology. As mode insensitive switching is challenging to realize for the large insertion loss induced by the

higher order modes and the intermodal crosstalk are also large due to the complex building blocks such as multimode waveguide crossing, multimode S-bend and phase shifters. Thus large port count mode insensitive multimode switch for higher order modes is still unavailable commercially. However, we experimental demonstrate a 3 × 3 mode insensitive switch with no waveguide crossing.

4.1.1 Design and Modelling

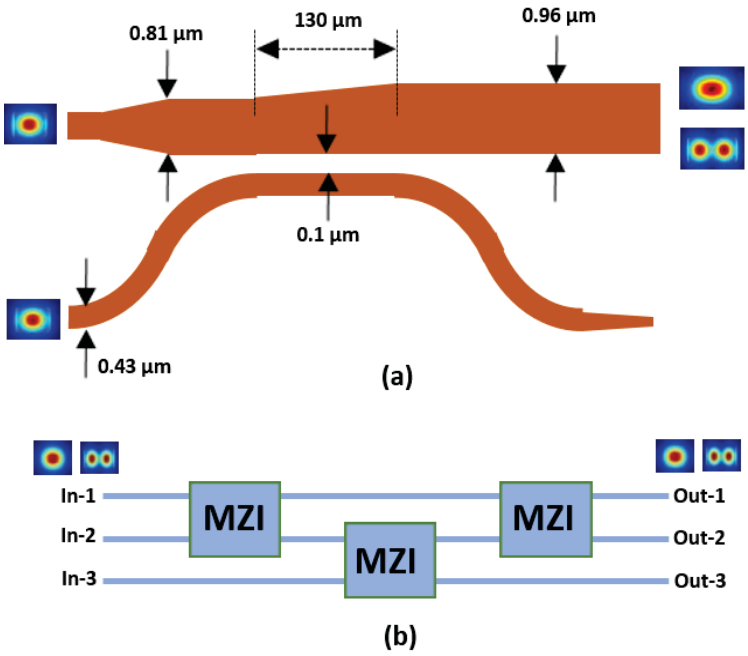

Figure 4.1: (a) Schematic of the optimized mode multiplexer and demultiplexer for first two quasi-transverse electric (TE) modes; (b) proposed topology for the 3 × 3 mode insensitive switch matrix.

Recently, our research group experimentally demonstrated a 2 × 2 mode insensitive

switch for the first three quasi-transverse electric (TE) modes, exhibits good extinction ratio, bandwidth, reasonable insertion loss and crosstalk [25]. It was observed that, most of the insertion loss comes from the mode MUX and deMUX and it is larger for higher order modes. Thus, we have further optimized the mode MUX/deMUX for the first two quasi-transverse electric (TE) modes by changing the length of coupling region as shown in figure 4.1 (a). Then, using the optimized 2×2 mode insensitive switch as a building block, we have designed scalable 3×3 mode insensitive switch for the TE_0 and TE_1 modes with significantly improved insertion loss and crosstalk as depicted in figure 4.1 (b).

4.1.2 Experimental Setups

Both continuous wave (CW) and payload data transmission (RF) measurements have been done to characterize the switch. As describe in chapter 3, a C-bend tunable laser is used to perform the CW measurements. At the output of this laser source, a polarization controller (PC) is connected to maintain the on-chip polarization of the optical signal to a quasi-TE optical mode. At the output of the chip, a power meter is connected to measure the optical power. The CW measurements are normalized to the grating couplers' losses.

Payload transmission is also experimentally performed to demonstrate the switching performance in a real data transmission system as shown in figure 4.2. To observe the impact of the intermodal crosstalk, we divide this experiment into two parts. In the first part, we transmit only one mode and in the second part, both TE_0 and TE_1 modes are

transmitted simultaneously to understand the system impact of modal crosstalk.

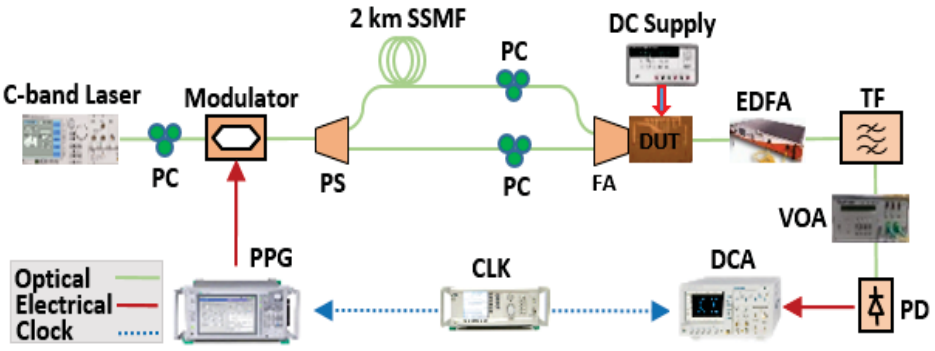

Figure 4.2: Experimental setup of the switch (DUT) for real data transmission. PC: polarization controller; PS: power splitter; SSMF: standard single-mode fiber; FA: fiber array; TF: tunable filter; EDFA: erbium doped fiber amplifier; CLK: clock synthesizer; DCA: digital communication analyzer; VOA: variable optical attenuator; PPG: pulse pattern generator.

The output of the C-band tunable laser is connected to a modulator with 12.3 GHz and 40 GHz 3-dB RF bandwidth for NRZ and PAM4 data signals, respectively, through a polarization controller (PC). The 1550 nm CW signal is modulated by a 10 Gb/s NRZ or 14.0625 Gbaud PAM4 PRBS-31 signal from a pulse pattern generator (PPG). The modulated signal then goes through a 1 $\times$ 2 power splitter to generate two channel signals to fed the two-mode switch. One channel is delayed by passing through a 2 km standard single-mode fiber (SSMF) to decorrelate the signals. Then the signals passed through another PC to the DUT (device under test) where light is coupled by a grating coupler. The output signal is amplified by an erbium-doped amplifier (EDFA) to compensate for the insertion loss of the device; then it passes through a C-bend tunable filter to reduce the unwanted amplified

spontaneous emission (ASE) noise generated by the EDFA. A variable optical attenuator (VOA) is used to maintain the optical power at the desired level for the photodetector (PD). After the PD, the RF signal is fed to a digital communication analyzer (DCA) to capture the eye diagram. A synthesized clock (CLK) synchronizes the PPG and DCA.

4.1.3 Experimental Results

The corresponding spectrum response for the 3 × 3 mode insensitive switch at 1550 nm is shown in figure 4.3. For TE_0 and TE_1 modes, the lowest insertion loss measured 1.8 dB and 2.4 dB, respectively, at I3-O3 where only one MZI building block is employed and the highest insertion loss is measured 2.6 dB and 3.3 dB for TE_0 and TE_1, respectively, where two MZI building is used. The maximum crosstalk is measured approximately 10 dB and 8 dB for TE_0 and TE_1 modes, respectively, within the 40 nm wavelength range from 1530 to 1570 nm.

Payload transmission is done to measure the performance of this switch. Eye diagrams are measured using both the 10 Gb/s NRZ (figure 4.4) and 14.0625 Gbaud PAM4 (figure 4.5) PRBS-31 signals. For single mode transmission, clear open eye is observed. The corresponding eye diagrams are slightly deteriorated in simultaneous transmission owing to the intermodal crosstalk. However, in all scenarios, clear open eye is measured with a reasonable signal-to-noise ratio (SNR).

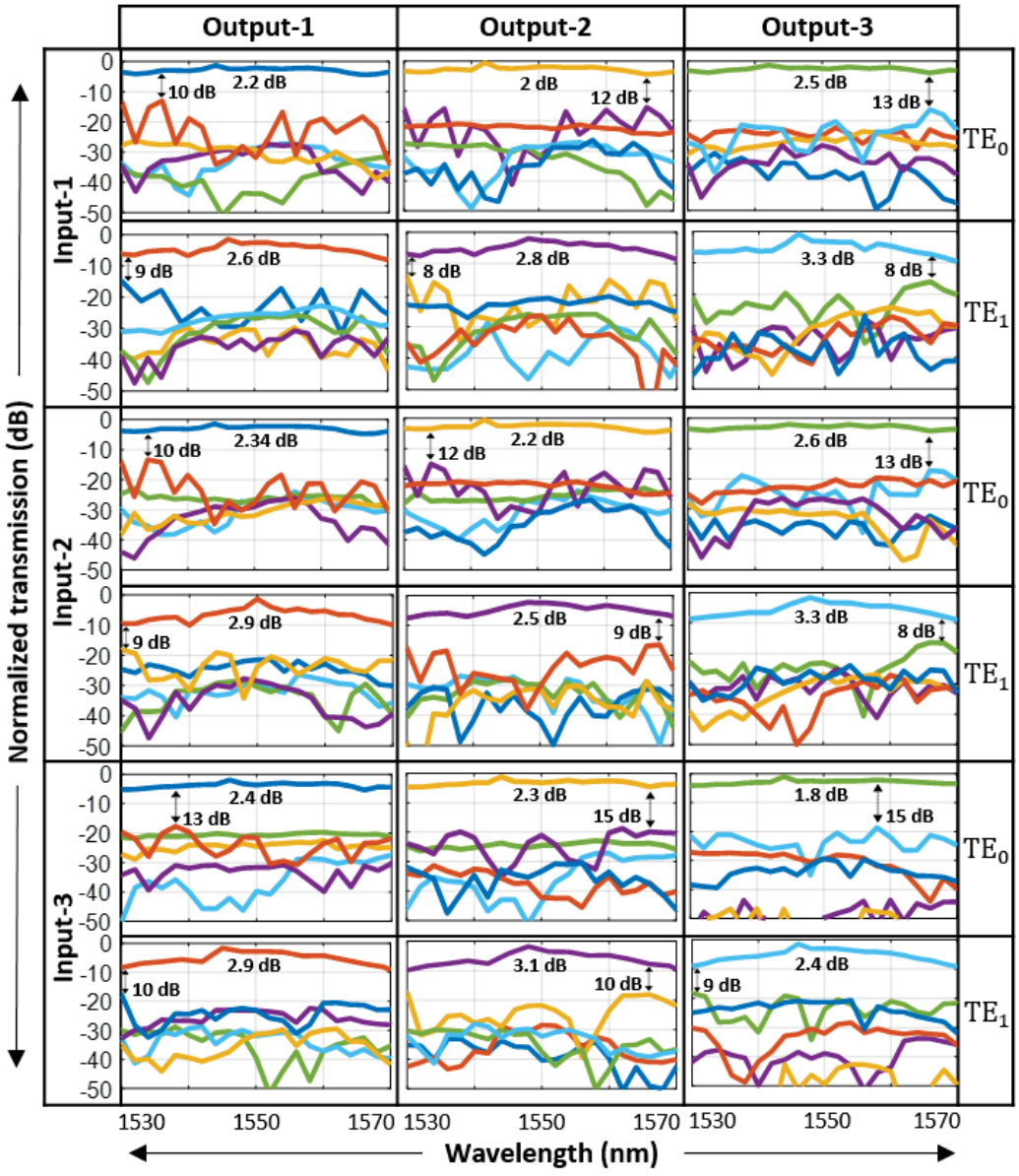

Figure 4.3: Measured normalized transmission spectrum as a function of wavelength for 3 × 3 mode insensitive switch matrix.

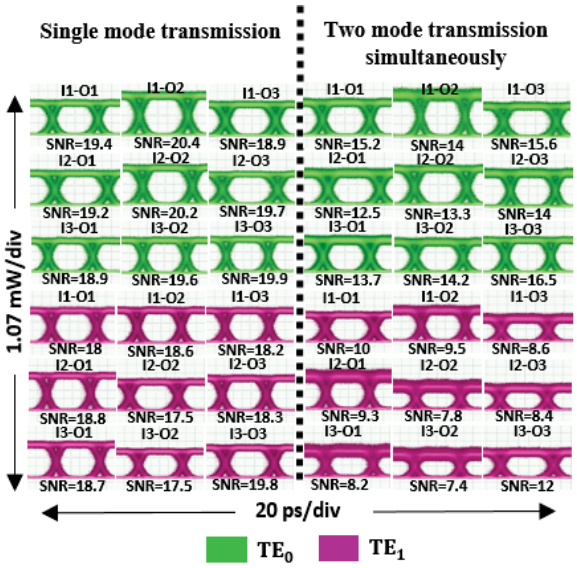

Figure 4.4: Eye diagrams for the 3 × 3 mode insensitive switch using 10 Gb/s NRZ PRBS-31 signal for both single-mode and two-mode simultaneous transmission.

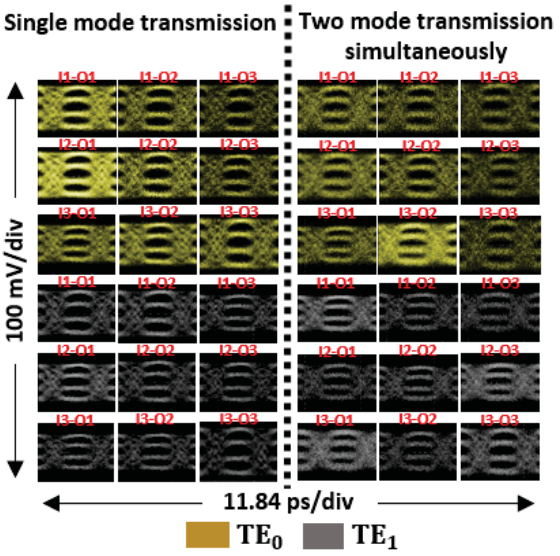

Figure 4.5: Eye diagrams for the 3 × 3 mode insensitive switch using 14.0625 Gbaud PAM4 PRBS-31 signal for both single-mode and two-mode simultaneous transmission.

4.2 4 × 4 Mode Insensitive Switch

In previous section, we demonstrated a 3 × 3 mode insensitive switch matrix for the first two quasi-transverse electric (TE) modes. Using the same approach, we extend the port count and design the topology for a 4 × 4 switch matrix. As the number of building blocks used in 4 × 4 is almost the same as 3 × 3 switch, thus both the switches have similar performance in CW and RF measurement.

4.2.1 Design Topology

A 4 × 4 mode insensitive switch consists of five mode insensitive MZIs where one of the MZI is used as a waveguide crossing for routing the signals to increase port numbers as shown in figure 4.6. As efficient multimode waveguide crossing is still under development for the higher order modes, the multimode MZI with low insertion loss and crosstalk is used as a waveguide crossing.

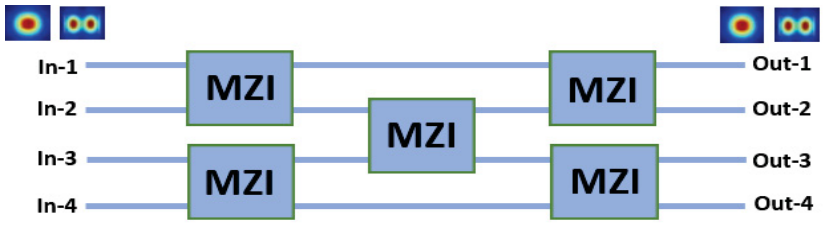

Figure 4.6: Proposed topology for the 4 × 4 mode insensitive switch matrix.

4.2.2 Experimental Results

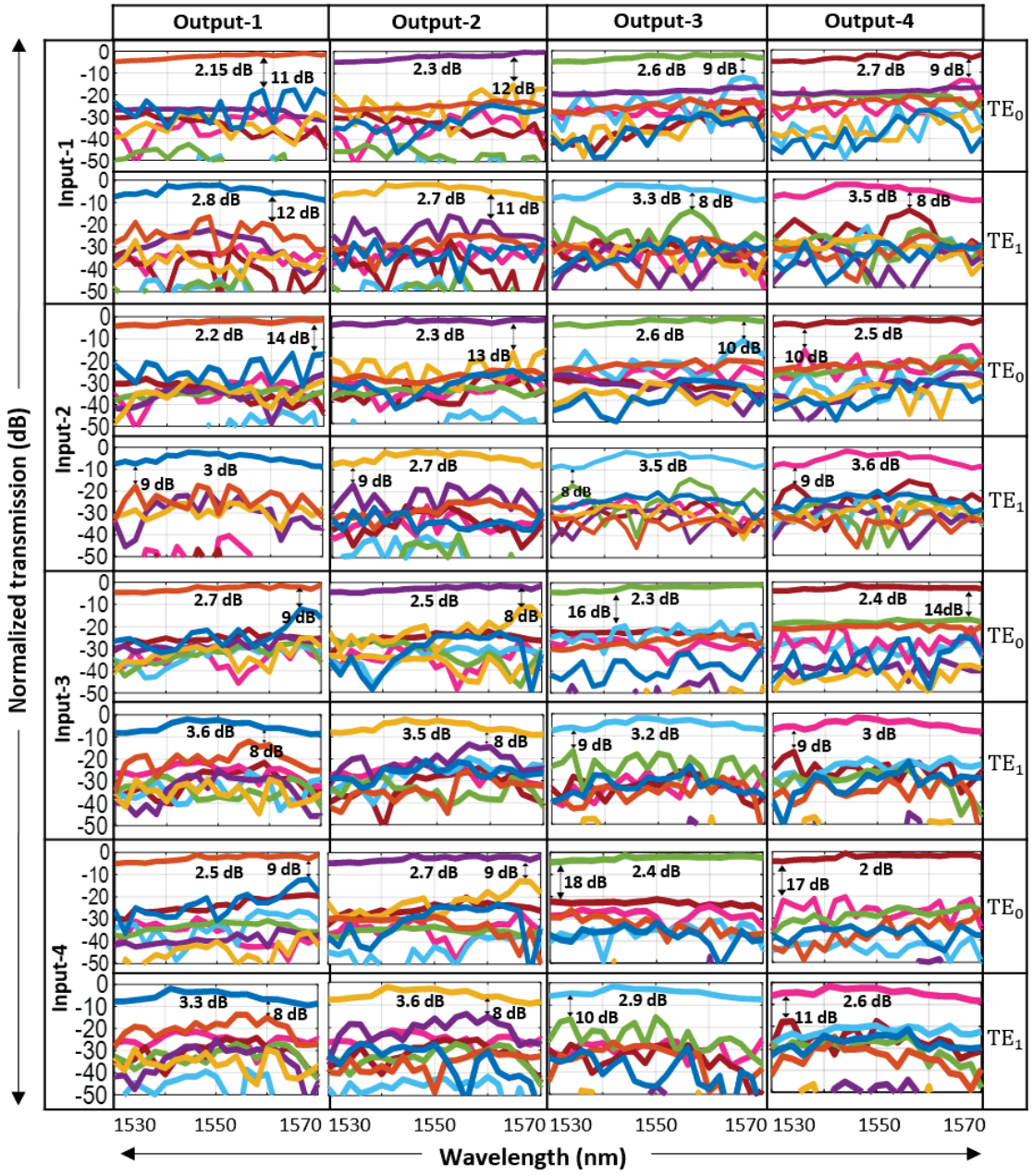

Figure 4.7: Measured normalized transmission spectrum as a function of wavelength for 4 × 4 mode insensitive switch matrix.

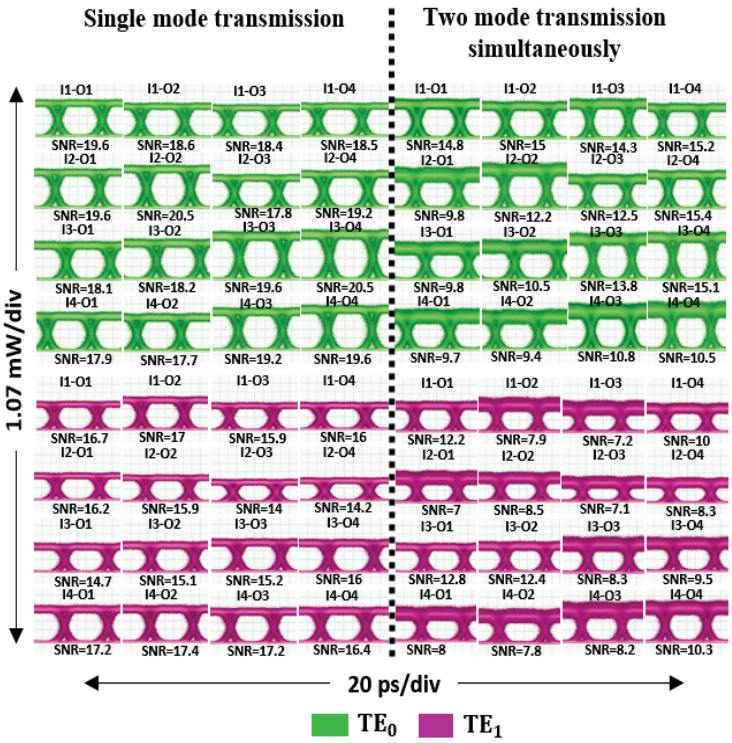

Figure 4.8: Eye diagrams for the 4 × 4 mode insensitive switch using 10 Gb/s NRZ PRBS-31 signal for both single-mode and two-mode simultaneous transmission.

We use the same experimental setup discussed in the previous section, to characterize the 4 × 4 switch. The corresponding spectrum response for the 4 × 4 mode insensitive switch is demonstrated in figure 4.7. The lowest (highest) insertion loss measured for TE_0 and TE_1 is 2 dB (2.7 dB) and 2.6 dB (3.6 dB), respectively at 1550 nm. After using the multiple stages of cascaded MZI, the crosstalk is measured at most approximately 8 dB for both of the TE_0 and TE_1 modes, respectively, within the 40 nm wavelength range from 1530 to 1570 nm.

Payload transmission is performed to show the performance of the switch in real data transmission system. Eye diagrams are measured using both the 10 Gb/s NRZ (figure 4.8)

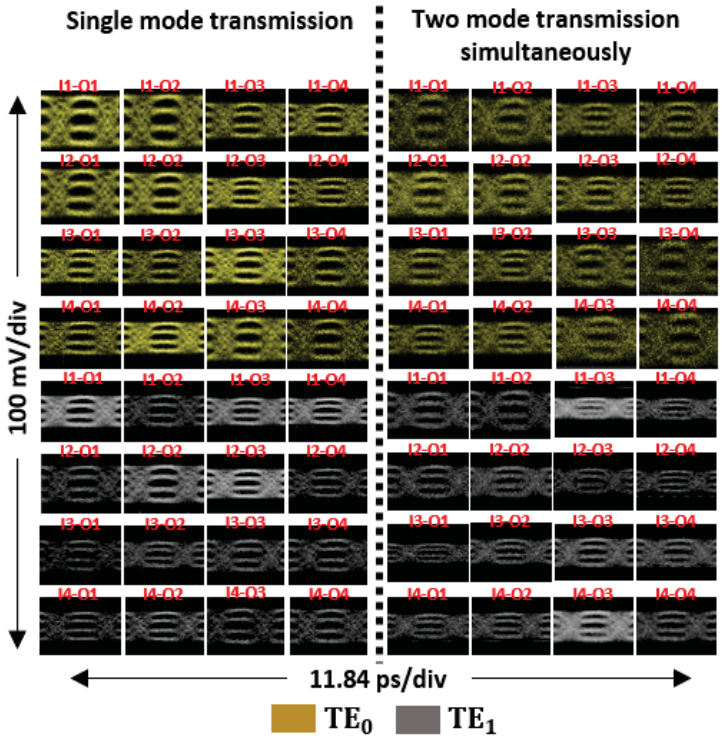

Figure 4.9: Eye diagrams for the 4 × 4 mode insensitive switch using 14.0625 Gbaud PAM4 PRBS-31 signal for both single-mode and two-mode simultaneous transmission.

and 14.0625 Gbaud PAM4 (figure 4.9) PRBS-31 signals. Same as 3 × 3 switch matrix, clear open eye is observed for all the single mode transmissions and the eye diagrams are bit deteriorated in simultaneous transmission due to intermodal crosstalk. The TE_1 mode suffers much from the deterioration because of higher insertion loss. However, in all cases, a clear open eye is measured with a good signal-to-noise ratio (SNR).

4.3 Discussion

In this chapter, we propose and experimentally demonstrate mode insensitive switches for the MDM system. The mode insensitive heater benefits simultaneous transmissions for all the modes. By sharing the phase shifter for different modes, the power consumption of the MDM switch is considerably reduced. If all the phase shifters are on 'ON state', the total power (energy) consumption for the 3×3 and 4×4 thermal switches is approximately 120 mW (2 pJ/bit) and 200 mW (2.5 pJ/bit), respectively at 10 Gb/s. Table 4.1 summarizes experimental results for these mode insensitive switches within 40 nm of bandwidth range from 1530 nm to 1570 nm.

Table 4.1: Summary of the experimental results at 1550 nm

Switch	Mode	Insertion loss (dB)	Maximum crosstalk (dB)	Bandwidth range (nm)	Power consumption (pJ/bit)
3×3	TE_0	2.6	10	40	2
3×3	TE_1	3.3	8	40	2
4×4	TE_0	2.7	8	40	2.5
4×4	TE_1	3.6	8	40	2.5

All the proposed switches described in this chapter showing low insertion losses and intermodal crosstalks over a sufficient bandwidth range. The clear open eyes with good SNR showing the evidence that these switches are fully compatible for error-free data transmissions in MDM systems. The scalable switching topology along with existing building blocks used, showing the potentials to design larger switching matrices with greater port count. After

further optimization of the building blocks for the higher order modes, these topologies can be used even for the higher-order modes (TE_3, TE_4, TE_5 etc).

Chapter 5

Scalable SiPh/InP Hybrid Switches for Lossless Operation

In this chapter, we propose several hybrid switches for lossless operation. The integration of InP-SOA gain block with large port count SiPh switches are studied. Our proposed hybrid switches consist of SOA gain blocks, bandpass filter and large radix switch matrix where SiPh and InP chipset has been combined by using photonic wire bonding and flip-chip technology. The InP-SOAs are used to provide the on-chip gain and a bandpass filter is used to reduce the noise introduced by SOA gain blocks. Both photonic wire bonding and flip-chip integration techniques have been demonstrated to implement the proposed SiP/InP hybrid switch matrices for lossless operation.

We use the SiPh switch presented in chapter 3 for the design of lossless scalable SiPh/InP

hybrid switches. Recently, our research group reported on employing an InP gain block, coupled to the SiPh switch, providing over 25 dB of optical gain in SiPh/InP hybrid switch [4, 54]. The SOA optical gain comes with inevitable amplified spontaneous emission (ASE) noise degrading the optical signal-to-noise ratio (OSNR) at the output of the hybrid switch. The ASE noise level and OSNR degradation are the main challenges in cascading the hybrid switches to realize a higher radix switch. Also, large gain from SOAs leads to saturation and non-linearity effects that degrade the payload integrity and increase the power penalty [86]. Furthermore, the sensitivity of the SOAs is limited (approximately -20 dBm). As the switch radix increases, more than one gain block are needed to boost the signal power repeatedly, whereas, each gain block comes with inevitable coupling loss and fabrication cost. The low loss SiPh switch improves the optical power budget and thereby reduces the required gain from the SOAs.

5.1 16 × 16 Hybrid Switch

Figure 5.1 presents the novel design proposed for a lossless 16 × 16 SiPh/InP hybrid switch with distributed gain blocks. We use Banyan blocking topology for more relax power budget and each channel has four stages of SiPh MZIs with two distributed InP gain blocks. The SiPh and InP chips are assumed to be coupled using the photonic wire-bonding technique [66, 68]. As our designed and commercially available InP-SOAs has minimum sensitivity above -20 dB, so the input optical power of the SOA gain block should be large enough to

be amplified. Based on the optical power budget, we divide the 16 × 16 SiPh switch matrix into two parts. After each part, an SOA gain block that provides 16.2 dBm optical gain to compensate for the optical loss induced by the SiPh switch matrix and filter, including the SiPh to InP coupling losses (5 dB/coupling for the worst-case). A footprint of 3 mm × 5.5 mm has been estimated for the proposed 16 × 16 SiPh/InP hybrid switch matrix formed by the photonic wire bonding.

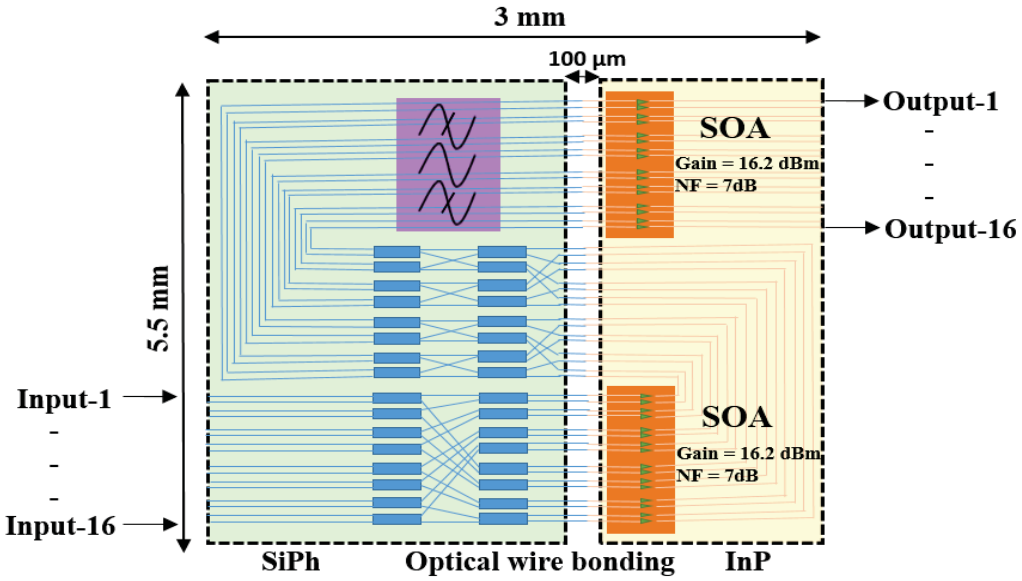

Figure 5.1: Proposed lossless 16 × 16 SiPh/InP hybrid switch matrix using optical wire bonding.

After the SiPh switch matrix and just before the second SOA, a SiPh optical bandpass filter removes the out of band ASE noise generated by the first stage SOA. In MZI based filter, typically a multiplexed optical beam is split into two optical waveguides with a 50/50 optical power ratio provided by an MMI. The two waveguides have two different arm lengths

to make a specific phase difference and after traveling through the arms, the beam will be combined by another 50/50 splitter. The output power from the combiner will be high for the constructively interfered wavelength and low for the destructively interfered wavelength. This filtering property relays on the arm's length difference of the asymmetric MZI. Using the combination of SiPh MZI and microring resonators, several on-chip bandpass filters have been reported [87–89]. In our designed bandpass filter, we use an asymmetric MZI with 7 μm waveguide path difference (ΔL) and two microring resonators with 0.5 coupling coefficient shown in figure 5.2(a), which exhibits a 30 nm wide 3 dB bandwidth and an insertion loss below 0.5 dB at 1550 nm in simulation as depicted in figure 5.2(b). This filter is simulated and characterized by Lumerical MODE and Interconnect, respectively.

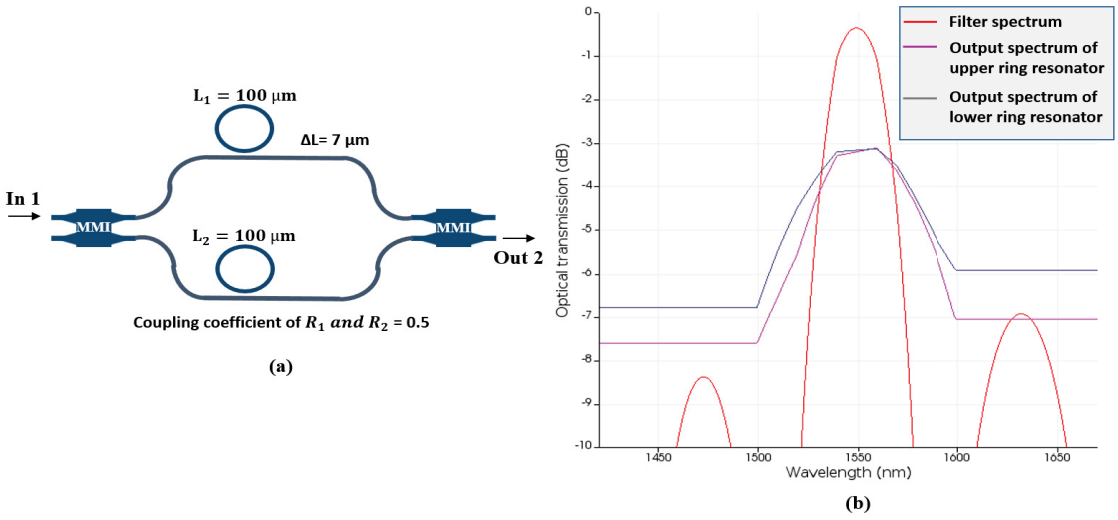

Figure 5.2: Optical filter; (a) designed bandpass filter; (b) simulated optical spectrum with 3 dB bandwidth.

The main advantage of using a bandpass filter before the 2nd stage SOA is to remove the

out of band ASE noise generated by the first stage SOA to reduce the input power to the second stage SOA and prevent its saturation. To investigate this point through simulations, we compare the input power spectrum to the second SOA in three cases: I) when a bandpass filter is used before the second SOA, II) when the filter is after the second SOA, and III) when there is no filter. We performed the simulations using Lumerical Interconnect. The figure 5.3 presents the input power spectrum to the second SOA for the three aforementioned cases. According to this figure 5.3, by using a filter before the second SOA, we reduce the input power to this SOA by 6.26 dB. This prevents saturation of second SOA as the input saturation power is around -6.2 dBm for this gain. It is observed that, using filter after the second stage SOA does not prevent the saturation, however it can reduce the ASE noise at the output.

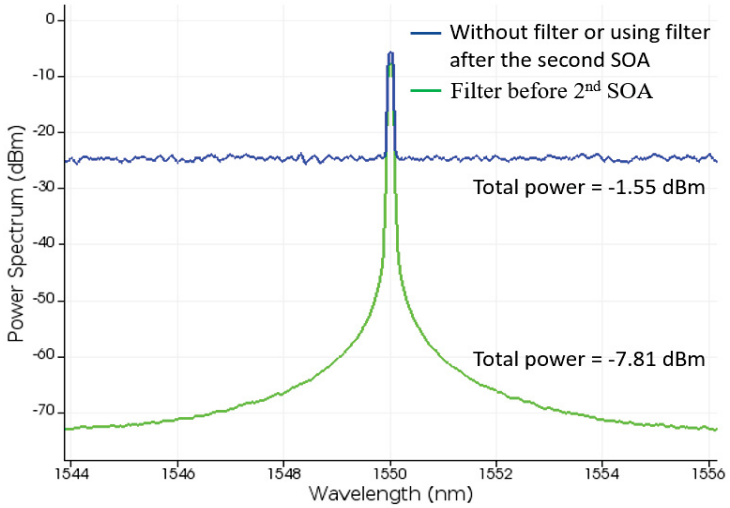

Figure 5.3: Input power spectrum to the second SOA when filter is using before the second SOA, after the second SOA, and without filter in 16 × 16 switch.

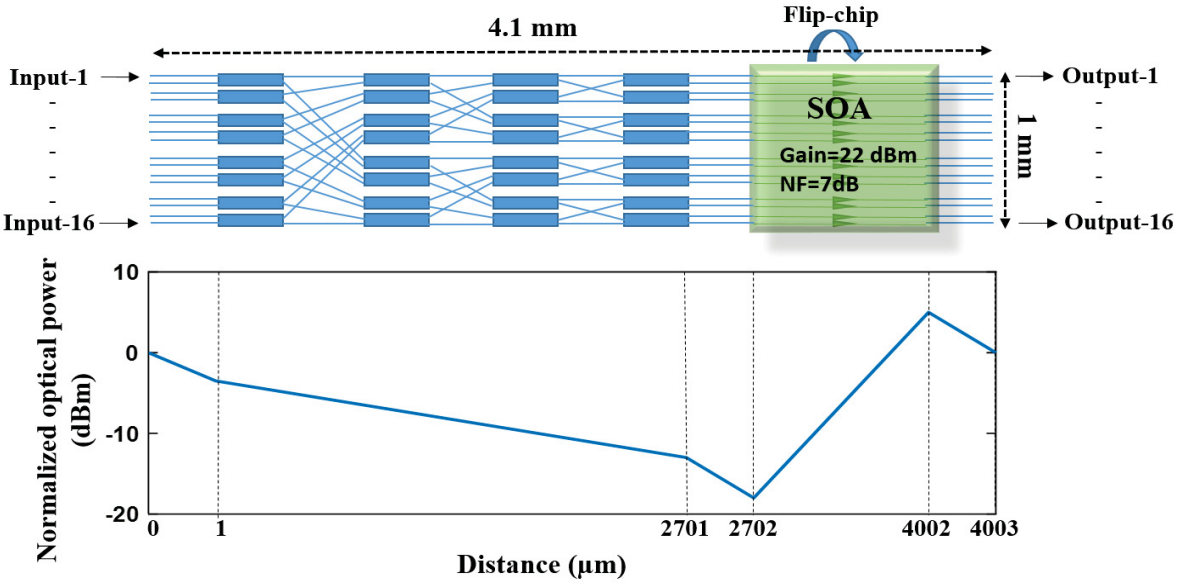

Figure 5.4: Proposed lossless 16 × 16 SiPh/InP hybrid switch matrix using flip-chip technology (top) and normalized optical power as a function of distance (bottom).

Another design topology using flip-chip technology also has been proposed for 16 × 16 switch matrix for lossless operation as shown in figure 5.4 (top). The proposed 16 × 16 SiPh/InP hybrid switch matrix has a compact footprint of 4.1 mm × 1 mm and the normalized optical power of this switch also has been demonstrated as a function of propagation distance of input light through the chip for lossless operation as shown in figure 5.4 (bottom). In this design, an InP-SOA gain block with 22 dBm gain is used to compensate for the overall optical loss, including the fiber to chip (3.5 dB) and chip to chip (5 dB) coupling losses. As one InP-SOA gain block is involved to compensate the total insertion losses, there are no need to use a bandpass optical filter in this switch. However, one may use an off-chip bandpass filter at the output of the hybrid switch to improve the

OSNR.

5.2 32 × 32 Hybrid Switch

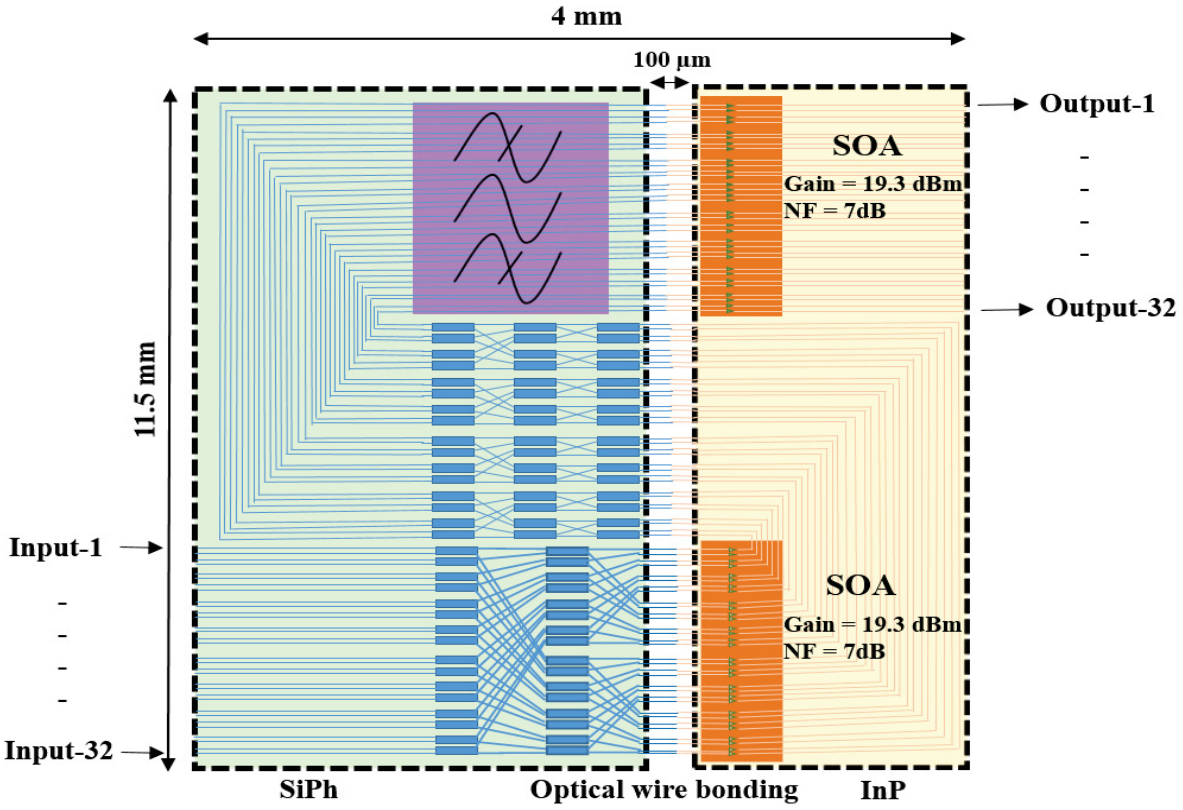

Figure 5.5: Proposed lossless 32 × 32 SiPh/InP hybrid switch matrix using optical wire bonding.

Based on the approach presented in the previous section, novel design for lossless 32 × 32 SiPh/InP hybrid switch using photonic wire bonding is shown in figure 5.5. This design includes two InP-SOA with 19.3 dBm gain and 7 dB noise figure. A SiPh bandpass filter is

used to reduce the out of band ASE noise after the first SOA gain block similar to the 16 × 16 hybrid switch discussed in the previous section. This compact wire-bonded switch matrix allows us to fabricate it within a 4 mm × 11.5 mm footprint area.

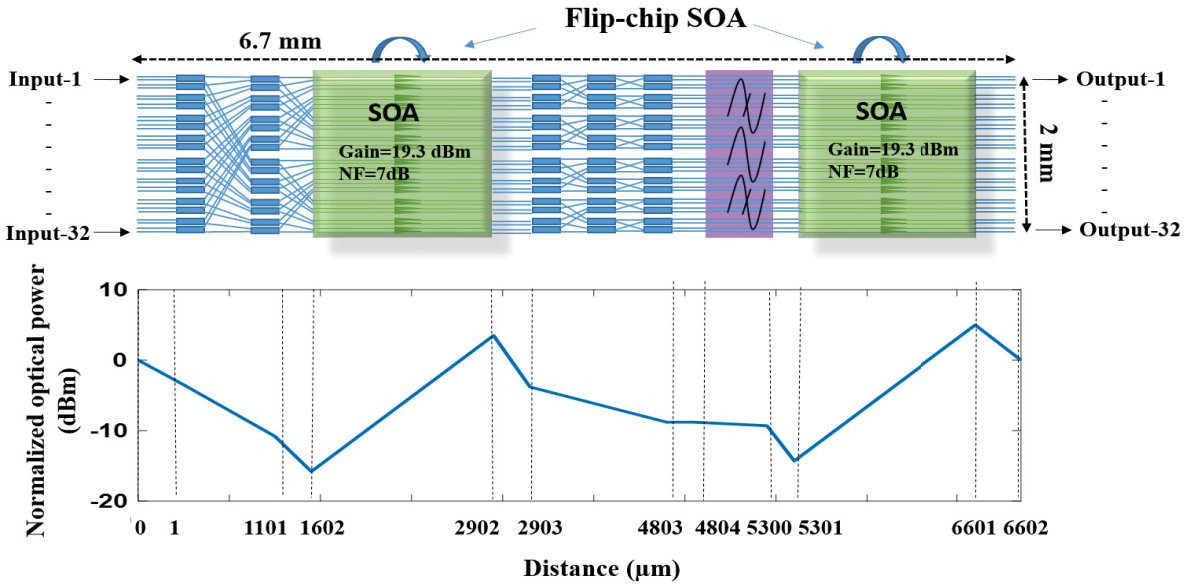

Figure 5.6: Proposed lossless 32 × 32 SiPh/InP hybrid switch matrix using flip-chip technology (top) and normalized optical power as a function of distance (bottom).

A similar port counts switch matrix has been investigated using flip-chip technology as shown in figure 5.6 (top) and the normalized optical power budget as a function of distance indicating the optical power consumption in the multiple stages is also shown in figure 5.6 (bottom). In this switch matrix, we use two InP-SOA building blocks, while in 16 × 16 hybrid switch using similar technology, we used one because of the lower power budget. As we are using two InP-SOA gain blocks, we need to integrate a SiPh bandpass filter before the second stage SOA to prevent the gain saturation and reduce the ASE noise coming from the

first stage SOA to improve the overall OSNR at the output. The proposed 32 × 32 hybrid switch with flip-chip technology allows us to fabricate within a 6.7 mm × 2 mm footprint.

5.3 64 × 64 Hybrid Switch

Using the same building blocks discussed in the previous section, we are also proposing a 64 × 64 hybrid switch matrix using the photonic wire bonding technique as shown in figure 5.7. In this design, we use two cascaded InP-SOA gain blocks with maximum gain (25 dB), which is capable to compensate the total optical losses induced by the multiple stages for lossless operation. A bandpass filter is also used here, similar to the previous switch matrices. The distance between SiPh and InP chip, and pitch length between two wires are taken 100 μm in proposed switch. The footprint area of 64 × 64 switch is estimated at 5.5 mm × 20 mm based on the fabricated building blocks reported previously.

Another hybrid approach for 64 × 64 switch matrix also has been studied using the flip-chip technique as shown in figure 5.8 (top) as well as the optical power distribution as a function of chip length (bottom). The footprint is estimated 7.5 mm × 4 mm based on the building blocks discussed before.

The fabrication method of photonic flip-chip technology is still challenging to meet the optical power budget due to the high coupling loss from any misalignment. However, precise fabrication can make it more suitable for hybrid switch matrix with high integration density within small footprint, while performances are almost the same compare to similar port

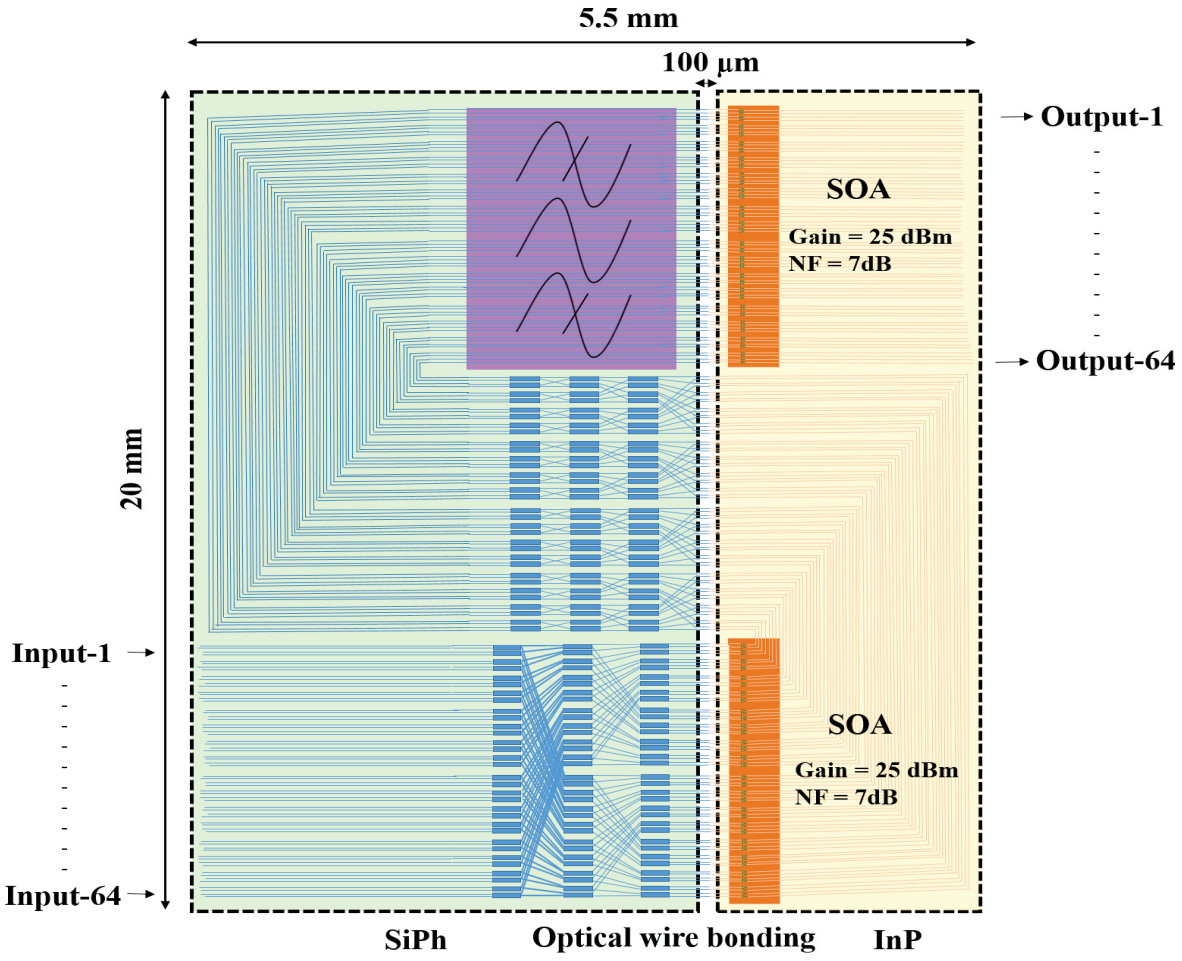

Figure 5.7: Proposed lossless 64 × 64 SiPh/InP hybrid switch matrix using optical wire bonding.

count switches with photonic wire bonding technology. On the other hand, photonic wire bonding offers excellent fabrication tolerance and able to reduce the number of crossing as shown in figure 2.14 (c).

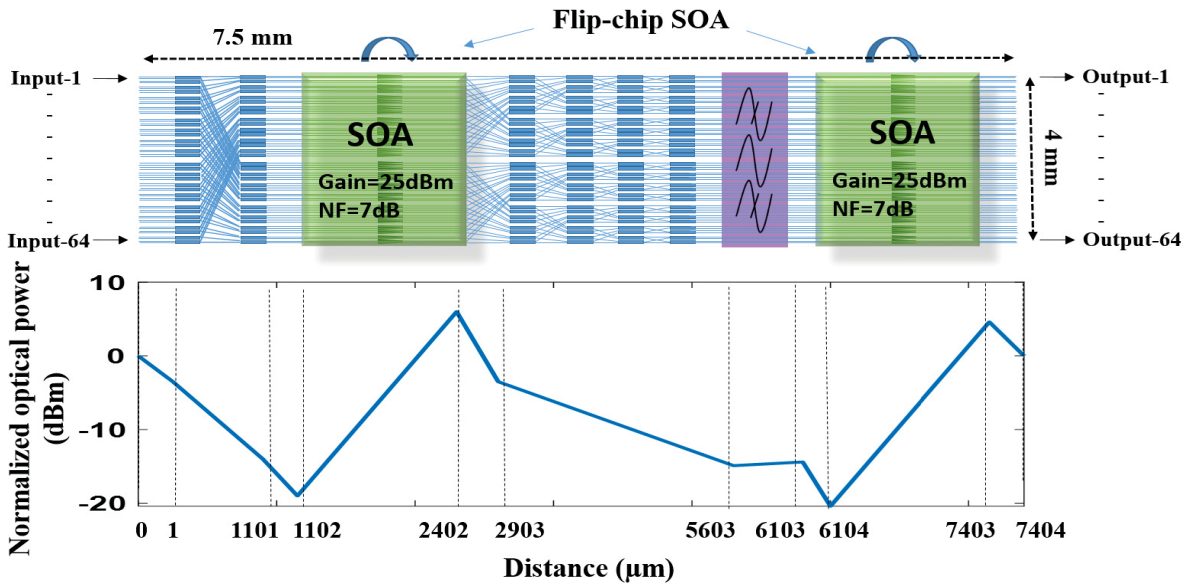

Figure 5.8: Proposed lossless 32 × 32 SiPh/InP hybrid switch matrix using flip-chip technology (top) and normalized optical power as a function of distance (bottom).

5.4 Performance Analysis of Lossless Hybrid Switch

In Table 5.1, the SiPh on-chip loss estimation for the longest path of the 4 × 4, 8 × 8, 16 × 16, 32 × 32 and 64 × 64 Banyan switches is assessed. The loss estimate uses the experimental results of the 2 × 2 MZI building block, waveguide crossing, and waveguide propagation loss. The experimentally measured insertion losses are 0.6 dB, 0.3 dB, and 3.8 dB/cm for 2 × 2 switch cell (MZI), waveguide crossing, and waveguide respectively. It is observed that the total on-chip loss estimated for the building blocks for 4 × 4 and 8 × 8 switches are approximately the same as the experimental measurement reported in chapter 3, which contributes to validate the total on-chip loss estimated for 16 × 16, 32 × 32 and 64

× 64 (hybrid) switches shown in Table 5.1.

Table 5.1: Optical loss estimation for the longest channel in the SiPh Banyan switch.

Switch radix	Longest optical path	Number of MZI stages	Longest waveguide length (mm)	Number of waveguide crossing	Total on-chip loss (dB)
4 × 4	I1-O4	2	1.5	1	2.1
8 × 8	I1-O8	3	5	4	4.9
16 × 16	I1-O16	4	7	11	8.4
32 × 32	I1-O32	5	10	26	14.6
64 × 64	I1-O64	6	15	57	26.4

Table 5.2 presents the estimated power budget for the longest paths of the hybrid switches showing that the SOAs are capable of compensating for coupling losses along with the on-chip losses towards lossless operation.

Table 5.2: Budgeted loss/gain (dB) values for the hybrid switches.

Loss/gain (dB) per stage	16 × 16	32 × 32	64 × 64
Input coupling loss to the SiPh chip	-3.5	-3.5	-3.5
Loss of SiPh building blocks	-4.4	-9.7	-13
Inter-chip coupling loss (SiPh to InP)	-5	-5	-5
SOA_1 gain	+16.2	+19.3	+25
Inter-chip coupling loss (InP to SiPh)	-5	-5	-5
Loss of SiPh building blocks	-4	-4.9	-13
Bandpass filter loss	-2	-2	-2
Inter-chip coupling loss (SiPh to InP)	-5	-5	-5
SOA_2 gain	+16.2	+19.3	+25
Output coupling loss from the InP chip	-3.5	-3.5	-3.5
Total fiber to fiber insertion loss	0	0	0

The noise figure (NF) of the hybrid switch is the noise factor expressed in decibel. To

calculate the noise factor of the proposed hybrid switch, we use the Friis formula that expresses the total noise factor of multiple cascaded stages:

$$F_{SiPh/InP} = F_1 + \frac{F_{SOA_1}-1}{1/L_1} + \frac{F_2-1}{1/L_1 \times G_{SOA_1}} + \frac{F_{SOA_2}-1}{1/L_1 \times G_{SOA_1} \times 1/L_2} + \frac{F_3-1}{1/L_1 \times G_{SOA_1} \times 1/L_2 \times G_{SOA_1}} \quad (5.1)$$

where, F_1 and L_1 are the noise factor and the aggregate loss of all the cascaded passive elements from the input to the first SOA (i.e., the input coupling to the SiPh chip, the switching elements in SiPh, the inter-chip coupling). F_{SOA_1} and G_{SOA_1} are the noise factor and gain of the first SOA. F_2 and L_2 are the noise factor and loss of the passive elements between the first and the second SOA (i.e., two inter-chip couplings, the switching elements in the SiPh, and the bandpass filter). F_3 is the noise factor of the output coupling. The noise factor of a passive lossy device is identical to its loss (in a linear ratio) [90].

Figure 5.9 presents the calculated noise figure (NF) for the 16 × 16, 32 × 32 and 64 × 64 hybrid switches. In calculating the NF, we use the values presented in Table 5.1 for the SiPh on-chip loss. The NF of SOAs is 7 dB [62]. We distribute the SiPh loss and InP gain between two equal stages. We find the NF for two different scenarios: when the inter-chip coupling is budgeted at 1.7 dB and 5 dB; and the filter loss is 0.5 dB and 3.5 dB, representing the best case and worst-case scenarios, respectively [70, 72, 87, 88]. The NF of 4 × 4 and 8 × 8 switches are for the single stage gain hybrid switches presented in [59] and [54], respectively. Employing the distributed gain design, one can achieve lossless operation

for the 64 × 64 switch with a NF below 30 dB. Although the distributed gain design comes with inevitable extra coupling loss, it prevents the SOAs' saturation by dividing the gain between the stages. The output OSNR remains above 30 dB supporting low noise data transmission. Larger switch matrices greater than 64 × 64 with reasonable OSNR can be achieved using more SOA gain blocks and the NF and output OSNR can be further improved by using off-chip bandpass filters at the switch output. All estimations are done based on the longest path of the switching matrix. Changing the bias current, the gain can be tuned accordingly for the shorter paths to prevent gain saturation.

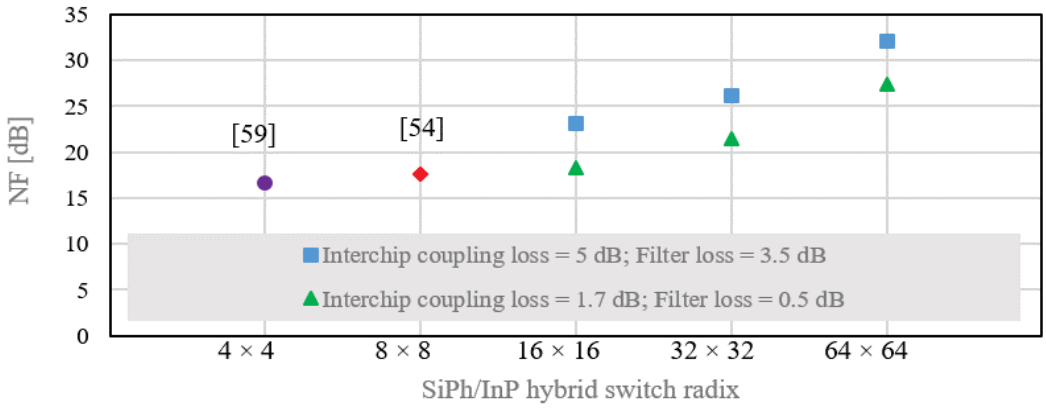

Figure 5.9: Hybrid switch noise figure (NF) versus switch radix.

The electrical power dissipated by each 2 × 2 MZI switch in 'OFF' state and 'ON' state is 4.8 mW and 34.8 mW, respectively, requiring 30 mW/π-phase shift representing a V_π of 1.6 V as reported in chapter 3. The total power consumption in SiPh switch is the summation of the individual power consumption from the thermal phase shifter of the 2 × 2 MZI switches. For 25 dB of optical gain, the SOA gain block needs 115.5 mW electrical power where the

biased current is 75 mA with a corresponding 1.54 V. Therefore, for the lossless operation of 16 × 16, 32 × 32 and 64 × 64 hybrid switches, the total power (energy) consumptions are approximately 2.96 W (18.5 pJ/bit), 6.48 W (20.2 pJ/bit) and 14.1 W (22 pJ/bit), respectively, while all the switching channels (all paths) are active ('ON' state).

5.5 Conclusion

In this chapter, we reported a InP-SOA gain block with large gain and low NF compatible for payload data transmission with high OSNR. We also demonstrated a bandpass optical filter that removes the out-of-band ASE noise generated by the first stage SOA, which improves the OSNR at the output. At the same time, this filter reduces the average optical power received by the second SOA and prevents its saturation leading to nonlinearities. Finally, we proposed a hybrid switch approach combining SiPh switch and InP-SOA components with SiPh bandpass filter, exhibits high scalability, sufficient crosstalk suppression, and lossless optical transmission at the output ports. The proposed design idea can be implemented using other switching architectures such as Beneš or dilated Beneš according to the application.

Chapter 6

Conclusion

In this chapter, we summarize the thesis content, including the demonstrated results with possible applications in datacenter networks. Future works related to this thesis are also discussed briefly in this chapter.

6.1 Thesis Summary

In this thesis, several SiPh switches have been designed, simulated, and experimentally demonstrated. Both single-mode and multimode switches are investigated for WDM and MDM systems respectively. The experimental results, including continuous wave measurement and payload transmission, validate the performance of these switches for datacenter applications. The detailed summary of the particular chapters is presented below.

- In chapter 2, the theoretical background of this thesis has been reported. Several switching mechanisms with state-of-the-art are mentioned and discussed in details. Thermo-optic, electro-optic, MEMS, and multimode switches, including the existing challenges and the possible solutions of them are also investigated based on the published literature. InP-SOA, multimode building blocks, and other recent works related to this thesis are discussed in details. At the end of that chapter, the performance matrices and current state of the SiPh switches are also discussed based on the proposed switches.

- In chapter 3, SiPh components such as MMIs, thermal phase shifter are designed and experimentally demonstrated. Several types of switches are designed and fabricated to demonstrate the system level performance in WDM systems using these components. We experimentally demonstrated scalable 2×2, 4×4, and 8×8 SiPh thermo-optic switches exhibiting low loss, low crosstalk, and low power consumption with a BER below 10^{-10} for payload data transmission. For 8×8 switch, less than 3.13 dB insertion loss and approximately 20.5 dB crosstalk is measured with 5.2 pJ/bit power consumption. At the end of that chapter, an ultra-broadband 16×16 thermo-optic switch has been designed and experimentally demonstrated using an optimized broadband MMI. This 16×16 SiPh thermo-optic switch provides 100 nm of bandwidth, at most 8 dB in crosstalk, and less than 3.8 dB of insertion loss for the longest path. At 10 Gb/s, this energy-efficient switch consumes less than 7 pJ/bit.

All of these demonstrated switches are designed using Banyan topology for a more relax optical power budget at the cost of a blocking behavior, which can be used in interconnect switches for WDM-based networks where the controller accounts for the blocking scenarios. The low loss, low crosstalk, low power consumption with a good SNR in payload data transmission show the scalability of these switches in a WDM network

- In chapter 4, a novel design topology for scalable 3 × 3 and 4 × 4 mode insensitive multimode switching matrices for the first two quasi-transverse electric (TE) modes has been proposed and experimentally demonstrated. At 1550 nm, the 3 × 3 switch exhibits approximately 2.6 dB and 3.3 dB insertion loss with a maximum crosstalk measured 10 dB and 8 dB for the longest channel over a bandwidth range of 40 nm for TE_0 and TE_1 mode, respectively. For 4 × 4 switch, the insertion loss is approximately 2.7 dB and 3.6 dB for the longest channel at 1550 nm with a corresponding crosstalk of at most 8 dB over a bandwidth range of 40 nm for TE_0 and TE_1 mode, respectively. The mode insensitive phase shifter ensures less power consumption for simultaneous multimode signal transmission in a mode division multiplexing (MDM) network. When all the ports are active 'ON state', the total power (energy) consumption for the 3 × 3 and 4 × 4 thermal switches is approximately 2 pJ/bit and 2.5 pJ/bit, respectively at 10 Gb/s for simultaneous two-mode transmission. The low insertion loss, intermodal crosstalk, and power consumption with a good SNR validate the scalability of these

switches in MDM networks.

- In chapter 5, we propose and theoretically demonstrate SiPh/InP hybrid switches up to 64 × 64, using the photonic wire bonding and flip-chip coupling technologies. Using multiple stages of distributed InP-SOAs, integrated by photonic wire bonding and flip-chip technology, lossless operation is realized with a reasonable NF. It is also investigated that larger switch matrices greater than 64 × 64 with reasonable OSNR also be achievable using enough InP-SOA gain blocks.

6.2 Future Works

With the accomplishment of this thesis, several possible research directions related to the accomplished works are discussed in this section. Suggested future works include:

- Utilizing the building blocks used in the ultra-broadband and low loss 16 × 16 switch, a 32 × 32 Banyan non-blocking switch matrix can be designed and fabricated with packaging and characterize for PAM4 transmission.

- The proposed distributed InP-SOA based SiPh hybrid switches can be fabricated and packaged using photonic wire bonding technique and experimentally characterize for the real data transmission system.

- Lots of works need to be done to design more optimized multimode MMI, waveguide crossing, and S-bend for higher-order modes (TE_3, TE_4, TE_5 etc). After further

optimization of these building blocks, our proposed switches can be scaled for the larger port count and higher-order modes simultaneously.

- Silicon nitride (SiN) based thermo-optic switches can be designed both for single and multimode networks using the same design approaches discussed in this thesis.

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