Design and Implementation of a 1.8 Volt Wide Band CMOS Fractional-N Frequency Synthesizer for the Complete 5 to 6 Giga-Hertz Band

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CONTENTS

Abstract

The demand for wireless devices is increasing, new standards are constantly evolving and the operating frequencies are spreading towards higher spectrums. The stress on lowering the voltage supply, the power consumption, the cost and increasing level of integration are the driving forces behind today's RF microelectronics research.

The goal of this thesis is to show the possibility of standard CMOS technology replacing the traditional technologies in RFIC applications, specifically in the design and implementation of frequency synthesizers for 5GHz WLAN applications. The frequency synthesizer is a key building block of WLAN transceivers. To generate multiple frequencies with the resolution required by 5GHz WLAN standards, a fractional-N frequency synthesizer architecture was successfully implemented in 1.8V 0.18μm CMOS technology. To be able to cover the lower and upper 5GHz bands of both HiperLan and 802.11a standards, a wide tuning range quadrature voltage controlled oscillator (VCO), providing a 4-phase output and operating from 5GHz to 6GHz, was used in the phase lock loop (PLL) design. The 5GHz WLAN standards are targeted since they are the most promising, they have few interferers and large data throughputs.

This thesis presents one of the few frequency synthesizers having a large bandwidth of operation and a small resolution reported to-date for this type of application. Also, the digital components used in this frequency synthesizer, namely the fractional-N divider and prescaler have the lowest power consumption reported to-date.

Sommaire

La demande pour de nouveaux appareils de télécommunication sans fil ne cesse d'augmenter. De nouveaux standards évoluent très rapidement et cela toujours à des bandes de fréquences de plus en plus hautes. La recherche est poussée à ses limites par l'incessante demande pour des appareils disposants de sources de tension, consommation en puissance et de coûts toujours plus bas, tout en augmentant le niveau d'intégration RF de l'appareil.

Le but ultime de cette thèse est de démontrer la possibilité de la technologie standard CMOS à remplacer les technologies traditionnelles pour les applications RFIC, tout spécialement pour la conception et la fabrication de synthétiseurs de fréquence pour les applications WLAN à 5GHz. Le synthétiseur de fréquence est un des blocks clé dans la conception d'émetteur- récepteur radio. Pour obtenir la résolution requise par les standards WLAN 5GHz, une architecture de synthétiseur N-fractionnel fut implémentée avec succès en utilisant la technologie CMOS 0.18µm à 1.8V. Il utilise un oscillateur en quadrature, contrôlé par voltage (VCO), pouvant générer des fréquences couvrant les deux bandes de fréquences, basse et haute, des standards HiperLan et 802.11a. Il fut utilisé avec une boucle en verrouillage de phase pour couvrir la bande de fréquence allant de 5GHz à 6GHz. Les standards WLAN 5GHz sont la cible de cette recherche, car ils sont les plus prometteurs, ils ont des capacités de transfert de données très élevées et ne font face qu'à très peu d'interférence.

Cette thèse présente un synthétiseur de fréquence ayant une des plus large bande de fréquence opérationnelle et une des résolutions en fréquence les plus petite rapportée jusqu'à ce jour pour ce type d'application. De plus, les composantes numériques de la boucle en verrouillages de phase, soit le diviseur N-fractionnel et le pré-diviseur consomment la plus base puissance rapporté jusqu'à ce jour.

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Chapter 1 Introduction

In wireless telecommunications, the radio spectrum is allocated by different organizations that govern the use of the spectrum in the areas they have control over. The International Telecommunication Union (ITU) has the responsibility of maintaining and extending the cooperation between its members in regulating the radio spectrum and the standardization of telecommunication as a whole [1]. The main players in this organization, or at least its most influential members, are the US Federal Communication Commission (FCC) [2], and the European Conference of Postal and Telecommunications Administrations (CEPT) [3]. These organizations regulate the use of the frequency spectrum, and divide the spectrum into frequency bands that are allocated to different applications and standards [4].

In wireless telecommunication systems, the allocated frequency spectrum is subdivided into multiple channels in order to maximize efficiency [5]. The data is transmitted over the channels, and then processed at baseband. Figure 1.1 shows how data is down converted in a receiver using a mixer. Generating the proper local oscillator (LO) signals is a key element in down converting the data from a specific channel to baseband. The LO signals are generated through the use of frequency synthesizers. They consist of a voltage controlled oscillator (VCO) in a feedback loop. This type of loop is better known as a phase locked loop (PLL), where the error signal is the phase difference between a reference signal and the VCO. A synthesizer must be able to generate multiple frequencies with the resolution needed to meet the required number of channels in a system.

The mobile phone and wireless local area network (WLAN) vendors have recently seen an increasing demand for smaller hardware. These new smaller devices must support multiple features such as basic voice over multiple frequency bands, multiple high-speed wireless data transfer standards, GPS location technology, and multi-media applications. To keep the devices small, while at the same time increasing the number of features available, the hardware size of individual components must be reduced.

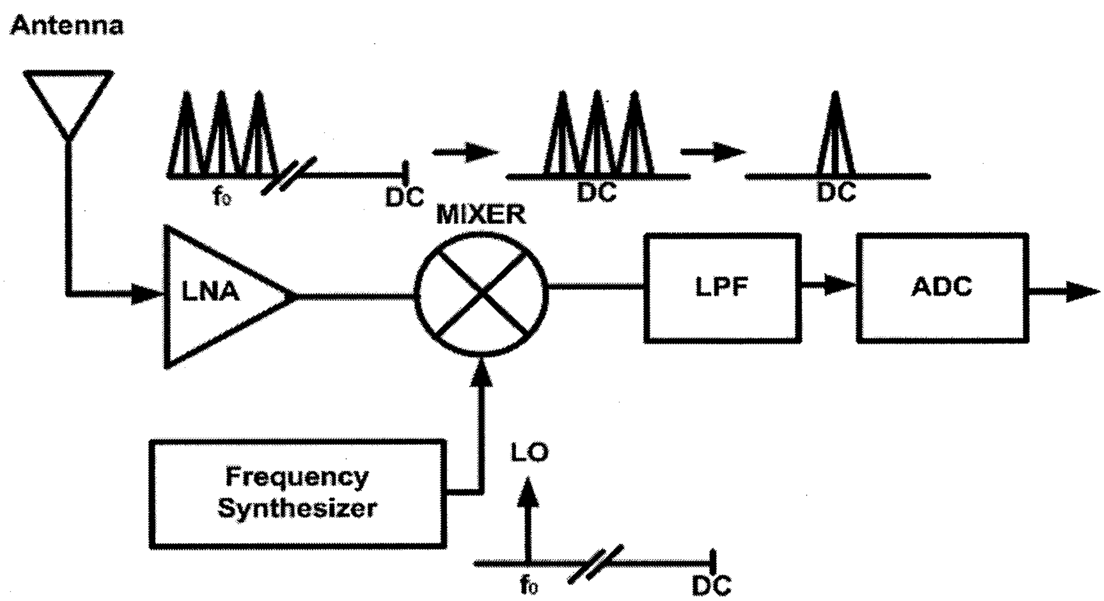

Figure 1.1.1 Direct down conversion receiver architecture

The first step toward making the devices smaller was to reduce the battery size. This effectively reduced the possible available power. The second step was to reduce the space occupied by the hardware. The continuous development of integrated circuit (IC) technologies and new circuit techniques is enabling low power and small area designs. One of the most popular IC technologies is the standard planar CMOS. Its continuous dimension down scaling is enabling low voltage supplies, high frequency operation, an unprecedented high level of integration, low power consumption, and low cost. To further reduce the space occupied by the hardware, the transceiver architecture trend is toward the use of direct conversion schemes to bring signals from the radio frequency (RF) bands (*i.e. in the GHz range*) to baseband. By using direct conversion, instead of the more traditional super heterodyne architecture, intermediate frequency (IF) filter circuits, such as expensive off chip image reject and channel select filters, can be removed, and a single frequency synthesizer operating at the RF frequency is required. Direct conversion offers a solution that is both highly integrated and which potentially consumes lower power. The direct conversion architecture is the de-facto standard for many mobile phone and RFIC vendors such as Alcatel, Nokia, Ericsson, Samsung, Siemens, Infineon, Conexant, Analog Devices, Phillips, Qualcomm, and TI to name a few [6].

1.1 Motivation

The IC industry is constantly trying to reduce costs, while at the same time improving the chip's performances. The technology of choice to achieve these two requirements is CMOS. Mainstream CMOS technology is normally optimized for digital applications. The continuous transistor dimension downscaling of CMOS technologies has led to an increase in the maximum operating frequencies. Research has demonstrated the potential of CMOS as a real contender for RF designs [9], [14]-[17], [20]-[23]. Standard CMOS now competes with traditional RF technologies, such as GaAs, InP, HEMT, HBT, and BJT. The use of CMOS for both analog and digital circuitry will bring devices to an unprecedented level of integration, enabling the implementation of single-chip RF transceivers. An RF frequency synthesizer is a critical building block in direct conversion communications systems. It is the only single circuit that is capable of generating multiple LO signals to directly down/up convert the data signals between the multiple RF channels and baseband, while introducing as little noise and interference as possible. The spectral purity of the synthesized frequency will affect the overall performance of the system, for instance, the number of available channels. Also, a lower phase noise will introduce less noise in the system thus improving receiver sensitivity and reducing the bit error rate (BER), which in turn will improve the maximum possible throughput of the system.

1.2 State-of-the-Art Synthesizers Designs

In this section, examples of synthesizers, both from research laboratories and from industry, will be presented. The most recent work on CMOS synthesizers reported in the literature is summarized and compared. The applications considered are limited to the 2.4GHz and 5GHz frequency ranges. The standardization of these frequency bands has been the most sought after, for current and future WLAN commercial products.

The three most popular frequency synthesis techniques are the direct digital synthesis (DDS), delay locked loop (DLL), and the PLL. The PLL is also subdivided into two types, the conventional PLL and the charge pump based PLL.

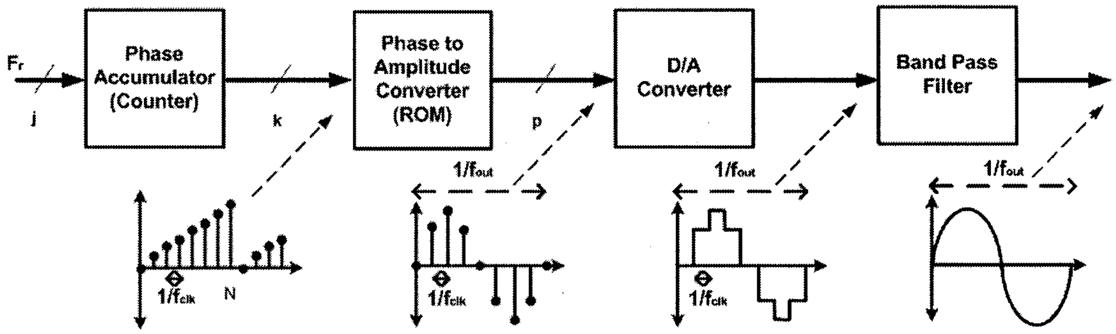

Figure 1.1.2 Conventional direct digital synthesizer architecture [7]

Figure 1.1.2 displays the conventional direct digital synthesizer architecture. This architecture is based on a rather simple four-step technique. First, a counter is set to count up to N, where N is an integer. Then a ROM look up table converts the counter value [0, N] into a voltage level. The resulting voltage level goes through a digital-to-analog (D/A) converter, the output of which is then filtered into a pure sinewave signal. The main draw back of this synchronous architecture is that the system clock must be highly stable, but since stable clocks are only available at rather low frequencies, the system will be limited. In [8], a 9.2GHz clock rate was taken from a high speed clock generator, and due to the Nyquist rate limitation, the highest frequency that could be generated was less than half the clock rate. Also, note that in order to achieve very low phase noise, the output filter needs to be of very high quality and highly selective. This filter is required to operate at high frequency as well, adding to the already large complexity of the transistor level implementation.

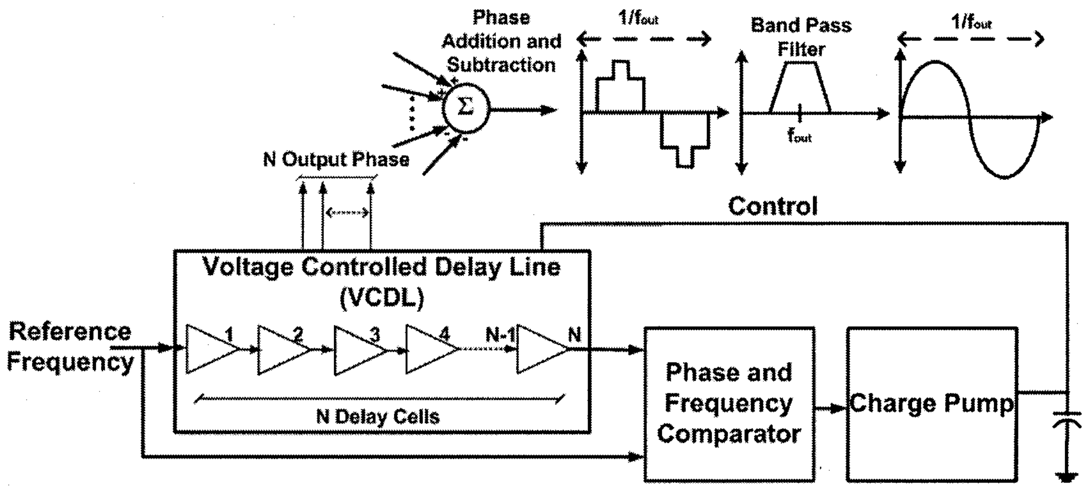

Figure 1.1.3 Conventional Delay Locked Loop Architecture [9]

Figure 1.1.3 shows the conventional delay locked loop architecture. A voltage controlled delay line is placed in a phase locked loop. The phase and frequency are compared with the reference frequency and are kept in lock by the feedback loop. The different phases generated are processed by a phase selector, an add/subtract circuit, and a bandpass filter that generates the output signal. The limitation of this circuit for high frequency synthesis is its need for a stable and high frequency reference. The possible output frequency and operating range are also limited by the minimum/maximum achievable delay through each delay element. The complexity of the digital circuitry (i.e., N delay cells, phase and frequency detector, phase selector, add/subtract circuit and bandpass filter) is also one of its main drawbacks.

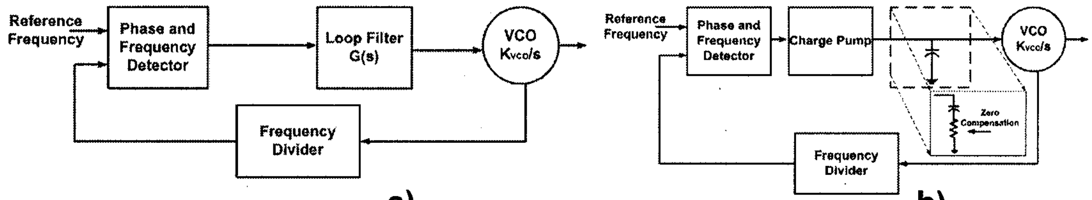

Figure 1.1.4 a) Conventional PLL, b) charge pump based PLL [10]

Figure 1.1.4 presents the two main types of PLLs, the conventional and the charge pump based. They are also known as frequency multipliers. This architecture enables high frequency synthesis using a relatively lower reference frequency. Compared to the DDS technique, which is only able to synthesize fractions of the reference clock, this architecture multiplies the reference frequency by the value of the divider. This can be either an integer or a fraction. There is one main difference between the two types of PLL. The transfer function of the charge pump based PLL includes an extra pole introduced by the charge pump. In order to stabilize the charge pump PLL, the capacitive load of the charge pump must be modified as shown in Figure.4 b. The main advantage of a charge pump PLL is its wide capture range, which is only limited by the VCO output frequency range, rather than being limited by the loop bandwidth as is the case for a conventional PLL. We will see in Chapter 2 that the charge pump PLL also adds a third degree of freedom in the loop behavior design by including the charge pump current into the design equations.

High performance frequency synthesizers are often implemented in technologies other than CMOS, such as the compound III-V processes. The main reason for this is their superior 1/f noise, and high frequency of operation compared with CMOS. The 1/f noise is the dominant factor in VCOs close in phase noise.

	DDS[8]	PLL[11]	PLL[12]	PLL[13]
Technology	InP (DHBT)	Si B6HF (BJT)	SiGe BiCMOS (HBT/CMOS)	GaAs (MESFET)
Frequency	36MHz-4.62GHz	6.4-6.75GHz	4.85-5.325GHz	2.3-2.55GHz
Phase Noise dBc/Hz	-140@2.5GHz offset@1kHz	-103@6.7GHz offset@1MHz	-101@5.075GHz offset@1MHz	-102@2.488GHz offset@10kHz
Supply	~5V	3V	3.3V	5V
Settling Time	-	170μs	10 μs	150ns
Power	15W	82mW	255mW	300mW
Area (mm²)	8x5	0.776x0.776	2	2

Table 1.1 Example of high performance frequency synthesizers

Table 1.1 is a summary of some existing high frequency synthesizers [8], [11]-[13]. Note that all the frequency synthesizers operate in the 2.4GHz and 5GHz WLAN frequency bands, which enables a fair comparison between the different implementations. The main drawbacks of these synthesizers are their high voltage supplies and power consumption, which makes them unsuitable for small, lightweight portable devices. Also, these are rather expensive processes, which make them unsuitable for low-cost commercial devices. These technologies are more suitable for high-end, high performance applications, such as satellites.

	[14]	[15]	[16]	[17]
Technology	**0.4μm CMOS**	**0.25μm CMOS**	**0.24μm CMOS**	**0.25μm CMOS**
Frequency	**2.6/5.2GHz**	**5.25-5.54**	**4.840-4.994GHz**	**5.14-5.70GHz**
Phase Noise dBc/Hz	**-100@5.2GHz offset@10MHz**	**-88@5.46GHz offset@40kHz**	**-101@4.96GHz offset@1MHz**	**-122@5.18GHz offset@1MHz**
Supply	**2.6V**	**1.5V**	**2.0V**	**2.5V**
Settling Time	**40μs**	**-**	**7.3 μs**	**100 μs**
Power	**47mW**	**23mW**	**35mW**	**13.5mW**
Area (mm²)	**1.75x1.15**	**-**	**1.6**	**-**

Table 1.2 State-of-the-art CMOS synthesizers

Table 1.2 presents state-of-the-art CMOS frequency synthesizers operating in the 5GHz WLAN band. The three circuits require low supply voltages (1.5-2.6V). As a result, their power consumption is very low (13.5-47mW). The CMOS technology down-scaling enables these low supply, low power circuits. When compared with the entries in Table 1.1, it is clear that the phase noise is much higher, thus making CMOS much less attractive for high-end applications.

1.3 Research Contributions

This thesis discusses research concentrated on the design of frequency synthesizers. The purpose of this research is to take advantage of the state-of-the-art 0.18μm CMOS technology in the implementation of RF wireless frequency synthesizers operating in multiple channel 5GHz WLAN applications. Even though CMOS could not match the ultra high-speed operation of the well established RF technologies mentioned earlier, it is to date the most cost-effective technology. Wireless transceiver circuits (including frequency synthesizers) implemented in a CMOS technology can be integrated with microprocessor and memory on the same chip. In an effort to optimize the performance of wireless frequency synthesizer circuits, different circuit topologies and layout techniques were used. To meet the low power requirements of battery operated devices, minimum size transistors were used whenever possible. This permitted the synthesizer digital circuitry to be driven by very small currents. This required the use of high density low parasitic layout techniques.

The following is a summary of the contributions of this thesis:

a) It describes a design methodology and layout techniques to minimize the parasitic capacitances and power consumption in digital circuitry. These methods and techniques have many useful properties: 1) High density layout and floor-planning reduces chip area and loading caused by long interconnects. 2) Low parasitic layout techniques will increase the maximum operating frequency and enable the use of smaller transistors. 3) A smaller transistor width reduces power consumption by decreasing the current through the devices. 4) Current reduction means smaller fluctuations on the supply lines, reducing unwanted digital noise, as well as the MOSFET generated noise in the case of thermal and shot noise.

b) It includes a design methodology to meet the required specifications for a frequency synthesizer and the fundamentals needed to fully understand the subject at hand. Mathematical modeling of well known PLL structures is also discussed.

c) It presents a successful chip implementation one of the *first reported* 0.18μm CMOS differential frequency synthesizer capable of generating frequencies over the complete 5-6GHz unlicensed frequency spectrum and with the best resolution reported in this frequency band. Lower phase noise measurements are obtained compared with results presented for example by Lam et al [22].

d) It describes a very low power, high frequency prescaler and fractional-N divider combination for high frequency resolution performance in frequency synthesis. *The lowest reported power consumption for this type of circuit in the literature, 4.5mW. Also, it reports a very low power consumption for a PFD and CP combination, 2.7mW.*

1.4 Thesis Organization

This thesis consists of five chapters. The first chapter discusses the motivation for frequency synthesizer's research in CMOS technology. It gives an introduction to spectrum regulation mechanisms and to the pressing need for high resolution frequency synthesizers in wireless communications. A discussion of the research contributions is included. Chapter 2 covers CMOS frequency synthesizer fundamentals, such as the basic theory of the noise sources present in RF integrated circuits (RFICs). The mathematical modeling of a PLL and its different noise sources and noise transfer functions are discussed. Design equations and constraints necessary to meet specific requirements are presented, along with a brief introduction to the HiperLan/2 and 802.11a standards.

Chapter 3 presents the design of each building block of the frequency synthesizer. Design issues to be considered, in order to meet the requirements of both the HiperLAN/2 and 802.11a standards are discussed. Layout considerations to minimize noise, power consumption, and area are presented for each block. A specific discussion is included on improving the VCO resonating tank quality factor by proper varactors' and inductors' design.

Chapter 4 presents a successful implementation of a dual standard frequency synthesizer for direct conversion transceivers. Measured results demonstrate very low power, a wide range of operation, a high frequency resolution, and a phase noise that compares very well with what has been reported in the literature to date. Testing and measurement procedures are described.

Chapter 5 summarizes the results of this work, presents possibilities for future improvement, and suggests combinations with other circuitry to create a complete direct conversion transceiver.

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Chapter 2 Synthesizer Theory

As introduced in Chapter 1, the frequency synthesizer is the circuit that enables the implementation of multiple channel communication systems. Its purpose is to synthesize frequencies over a specified frequency spectrum with the required resolution. The synthesized tones are used to drive the down/up converting mixers that allow bringing the information signal to the desired frequency band. Synthesizers enable a multi-channel communication system to maximize its data throughput by using the allocated spectrum to its maximum.

The noise introduced by a synthesizer will impede the performance of the communication system, hence increasing the bit error rate of the system. This will decrease the sensitivity of a receiver. Noise is not the only unwanted effect that a synthesizer may introduce. In a fractional-N synthesizer implementation, undesired spurs are also introduced in the output. These spurs may appear in the vicinity of the actual desired channel or in adjacent ones. They may cause interference and might down/up convert unwanted interferers with the data signal. It is important that in a transmitting system these spurs be minimized and placed at a large offset away from the center frequency. One must keep in mind that the output power spectrum of any transmitting system is regulated by standards. The reduction in the power of these spurs is necessary to achieve high data rates and to respect the guidelines given by the regulating authority.

In this chapter, different sources of noise are presented. This is followed by an in-depth noise analysis of frequency synthesizers, fundamental synthesizer theory and different PLL topologies. Finally, a brief introduction to the IEEE standards 802.11a and HIPERLAN is given in order to increase the awareness to application specific designs of synthesizers for multiple band compliant devices.

2.1 NOISE

2.1.1 Noise in Integrated Circuits

	Thermal Noise (Johnson Noise)	1/f Noise (Flicker Noise)	Shot Noise
RMS Noise Current	$\overline{i_n^2} = \frac{4kT\Delta f}{R}$	$\overline{i_n^2} = K\frac{I^a}{f^b}f$	$\overline{i_n^2} = 2qI_D\Delta f$

Table 2.1 Noise in Integrated Circuits

Table 2.1 presents the different types of noise occurring in integrated circuits. The theory of each type of noise is well covered in reference [24]. Thermal noise is associated with the thermal excitation of charge carriers in conductors (i.e., R the resistors), where k is the Boltzmann constant, T is the absolute temperature, and Δf is the noise bandwidth. The 1/f noise is known for its spectral density decay following a 1/f roll-off near DC, where a, b and K are empirical constants, I is the biasing current, and f is the operating frequency. Finally, shot noise is related to the DC current flow in semiconductor devices, where q is one electronic charge, I_D is the biasing current, and Δf is the noise bandwidth.

2.1.2 Phase Noise in Voltage Controlled Oscillators

2.1.2.1 Definition of Phase Noise

Phase noise is characterized by its frequency domain spectrum. The manner in which the power spectrum decreases as it moves away from the center frequency f_0 characterizes the phase noise performance of the oscillator. The sharper the power spectrum, the closer the oscillator is to an ideal Dirac impulse. Poor phase noise directly degrades a system's overall performance and reduces its throughput.

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{\text{noise power in a 1 Hz bandwidth at } \omega_0 + \Delta\omega}{\text{center frequency power}}\right) \qquad \text{Eq. 2.1}$$

Eq. 2.1 is used to quantify the phase noise performance of a voltage controlled oscillator (VCO). Phase noise is quantified by comparing the power residing in the sidebands to the power of the center frequency. A unit bandwidth at an offset of the center frequency is used in the comparison. The power in this unit bandwidth is calculated, giving an amount of power per Hertz, and then divided by the center frequency power. This ratio is then converted into dBc/Hz.

2.1.2.2 VCO Phase Noise Modeling

A major figure of merit of VCO design is phase noise. A model known as "Leesson's equation" can be used to approximate the output phase noise at a frequency offset $\Delta\omega$ from ω_o, the VCO center frequency [25]-[27].

$$\mathcal{L}\{\Delta\omega\} = k \cdot T \cdot Z_0 \cdot \frac{1}{Q_{\tan k}} \cdot [1 + A] \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1}{V_{rms}^2} \qquad \text{Eq. 2.2}$$

Eq. 2.2 is Leesson's equation, where k is the Boltzmann constant, T is the absolute temperature, A is the excess noise factor (a safety margin to ensure oscillation start-up), Z_0 is the VCO's tank characteristic impedance, and Q_{tank} is the overall quality factor of the tank. V_{rms} is the VCO output root-mean square voltage. This approximation will fairly describe the free running VCO phase noise when neglecting other noise sources such as the close in 1/f noise.

2.2 Synthesizers Fundamentals

A synthesizer consists of a local oscillator in a phase locked loop (PLL). The loop controls the frequency and the phase of the oscillator in order to stabilize it at a specific frequency. Frequency acquisition, settling time, noise, and spectral purity are all performance metrics that will be discussed in this section. In the following section, noise analysis will be performed for a basic 2nd order synthesizer system, including the case of a charge pump PLL. Sections on loop design, 2nd order settling time and fractional synthesis will also be presented.

2.2.1 Synthesizer Second Order Noise Analysis

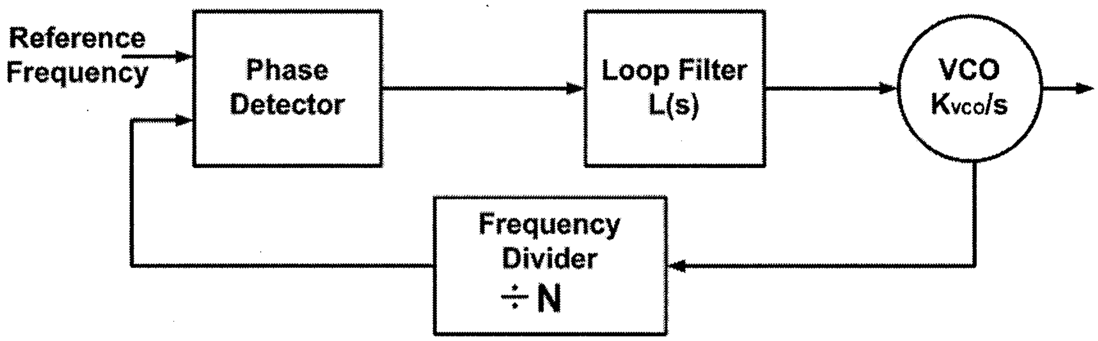

Figure 2.1 Standard PLL architecture

Figure 2.1 illustrates a typical phase-locked loop system consisting of a phase detector, loop filter, voltage controlled oscillator, and a frequency divider. It is easy to translate this system into a feedback system representation.

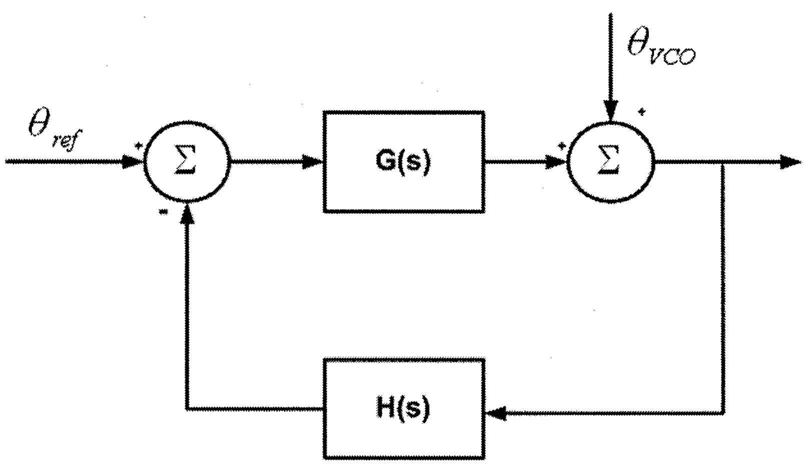

Figure 2.2 Synthesizer as a feedback system

Noise modeling in a synthesizer is analogous to modeling noise in a feedback system. Figure 2.2 displays the input noise sources as θ_{ref} and θ_{VCO}. These sources are the major noise entry ports. Other noise inputs come from the substrate and the power supplies. From Figure 2.2, the open loop transfer function can be derived as follows:

$$G(s) \cdot H(s) = \frac{K_F \cdot L(s)}{N \cdot s} \qquad \text{Eq. 2.3}$$

where

$$G(s) = \frac{K_F \cdot L(s)}{s},\ H(s) = \frac{1}{N},\ \text{and } K_F \approx K_{VCO} \qquad \text{Eq. 2.4}$$

Eq. 2.3 is the open-loop transfer function, and Eq. 2.4 is used modeling the synthesizer. The *1/s* term comes from the VCO transfer function. *N* is the frequency divider ratio. K_F is the forward gain, in this case the combined gains of the VCO, the phase detector, and the low pass filter. The VCO gain is the dominant term. *L(s)* is the low-pass filter transfer function with a pole at ω_{LP}. The following two noise transfer functions represent the two most important sources of noise in a PLL:

$$\frac{\theta_{out}(s)}{\theta_{VCO}(s)} = \frac{1}{1+GH(s)} = \frac{N \cdot s}{N \cdot s + K_F \cdot L(s)} = \frac{s(\omega_{LP}+s)}{s^2 + \omega_{LP}s + \frac{\omega_{LP}K_F}{N}} \qquad \text{Eq. 2.5}$$

$$\frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{G(s)}{1+GH(s)} = \frac{N \cdot K_F \cdot L(s)}{N \cdot s + K_F \cdot L(s)} = \frac{\omega_{LP}K_F}{s^2 + \omega_{LP}s + \frac{\omega_{LP}K_F}{N}} \qquad \text{Eq. 2.6}$$

Eq. 2.5 is the noise transfer function due to the presence of VCO phase noise. Eq. 2.6 is the noise transfer function due to an introduced reference phase noise. Note that both transfer functions are affected by the factor *N*, and that their noise magnitude increases with *N*. Eq. 2.7 and Eq. 2.8 represent the natural frequency of the synthesizer and damping factor respectively. They both depend on the values of N, ω_{LP}, and K_{VCO}.

$$\omega_n = \sqrt{\frac{\omega_{LP} K_{VCO}}{N}} \quad \text{Eq. 2.7}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{N \cdot \omega_{LP}}{K_{VCO}}} \quad \text{Eq. 2.8}$$

2.2.2 Noise Transfer Functions Example

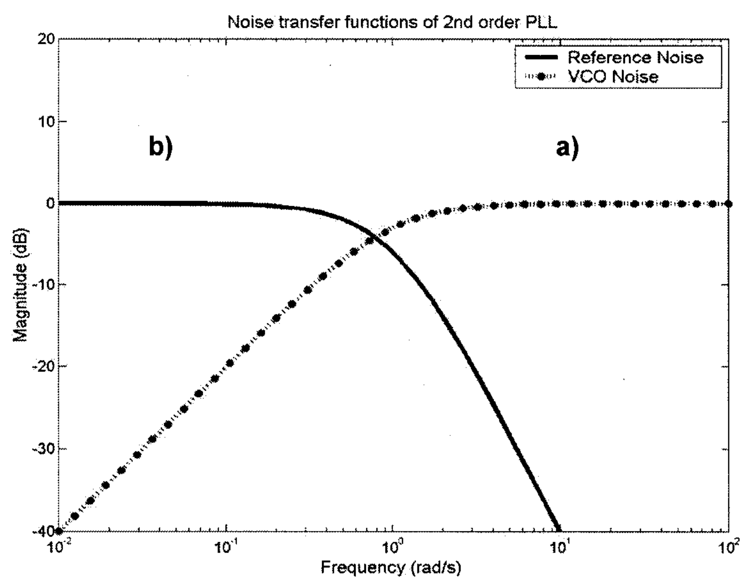

Figure 2.3 Noise transfer functions: a) VCO Noise, b) Reference Noise

Figure 2.3 corresponds to the VCO and reference noise transfer functions obtained with equations similar to Eq. 2.5 and Eq. 2.6. For simplicity, in both cases the damping factor and N are set equal to 1. The VCO noise transfer function behaves as a high-pass filter and the reference noise transfer function has a lowpass filter response. Effectively, the high-pass behavior of the VCO noise transfer function will shape the free running VCO phase noise by removing noise in the vicinity of the VCO center frequency. By increasing the loop bandwidth, the VCO noise transfer function will enclose less noise. Since both transfer functions are interdependent more reference noise will be introduced. However, a smaller loop bandwidth comes at the expense of a slower locking transient. In commercial implementations, the use of low noise crystals as reference sources enables the use of large loop bandwidths. These crystals introduce negligible amount of noise.

2.2.3 Charge Pump Synthesizer Noise Analysis

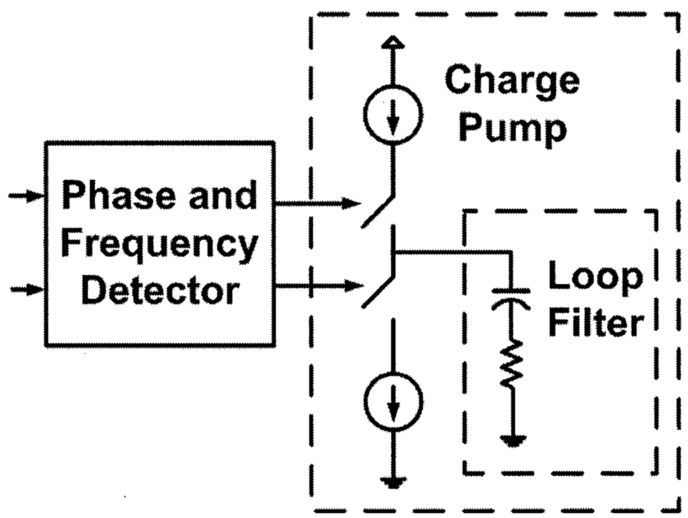

Figure 2.4 PFD and Charge Pump

Figure 2.4 illustrates a PFD and charge pump implementation. Synthesizers implemented with the use of a phase and frequency detector charge pump combination are quite popular in today's state-of-the-art designs. It has two main advantages: the capture range is only limited to the VCO frequency range, and the static phase error is zero assuming negligible charge pump mismatches and offsets [29]. The modeling of such designs is different than the standard models previously discussed, but they can still be looked at as second-order systems. The open loop transfer function is modified and the loop filter is included in the model of the charge pump gain as shown by Eq. 2.9 and Eq. 2.10 respectively.

$$G(s)\cdot H(s)=\frac{K_F\cdot G(s)}{N\cdot s}\xrightarrow{\text{for PLL with Charge Pump}}\frac{K_{CP}(s)K_{VCO}}{N\cdot s^2} \qquad \text{Eq. 2.9}$$

$$K_{CP}(s)=\frac{I_{CP}}{2\pi}\left(R+\frac{1}{C_p\cdot s}\right) \qquad \text{Eq. 2.10}$$

Eq. 2.10 describes the transfer function of the charge pump $K_{CP}(s)$ where C_p and R represent the added zero needed for stabilizing the PLL. Without the series resistor, the charge pump PLL would be inherently unstable. The charge pump current is represented by I_{CP}.

$$\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{\frac{I_{CP}}{2\pi C_p}\left(RC_p s+1\right)K_{VCO}}{s^2+\frac{I_{CP}}{2\pi}\frac{K_{VCO}}{N}Rs+\frac{I_{CP}}{2\pi C_p}\frac{K_{VCO}}{N}} \qquad \text{Eq. 2.11}$$

$$\omega_n=\sqrt{\frac{I_{CP}}{2\pi C_p}\frac{K_{VCO}}{N}} \qquad \text{Eq. 2.12}$$

$$\zeta=\frac{R}{2}\sqrt{\frac{I_{CP}C_p}{2\pi}\frac{K_{VCO}}{N}} \qquad \text{Eq. 2.13}$$

The overall synthesizer transfer function is described by Eq. 2.11. The addition of the charge pump current term in the transfer function adds more control to the loop behavior, which is desirable. Eq. 2.12 and Eq. 2.13 are the charge pump synthesizer's natural frequency and damping factor equations respectively. Note that they both depend on the value of I_{CP}.

2.2.4 Loop Behavior

The loop design is set mostly by the loop filter, VCO gain and charge pump current. Each application has its own specifications. This section will deal with noise shaping in PLL's, integrator phase noise optimization and second-order PLL settling time.

2.2.4.1 Noise Shaping in Phase Locked Loop Systems

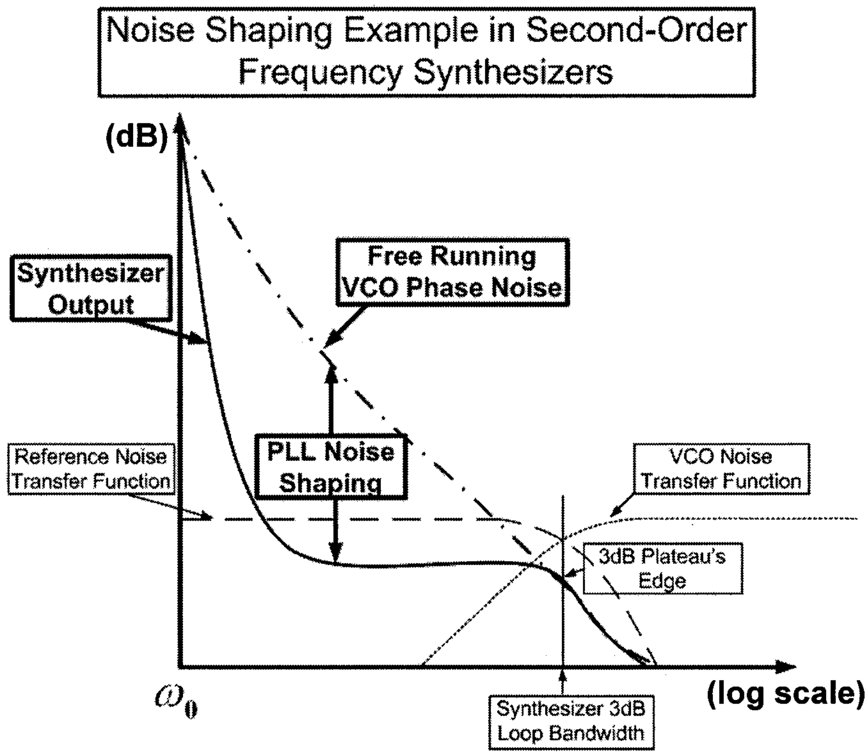

Figure 2.5 Noise shaping example for an optimized second-order synthesizer

Figure 2.5 illustrates how PLL noise shaping occurs. First, consider each of the curves of this figure. These are the free running VCO phase noise, the reference noise transfer function, the VCO noise transfer function, and the synthesizer output. The free running VCO phase noise is an almost straight line. The reference noise transfer function has a lowpass behavior and is characterized by its natural frequency. In this case, having a damping factor of one, the 3 dB loop bandwidth coincides with the natural frequency. Due to the very high quality of reference sources, the noise they introduce is negligible. In the case of the VCO transfer function its behavior is highpass. This particular behavior is the main mechanism of PLL noise shaping. Low frequency phase variations (i.e. phase noise) are removed by the highpass filtering behavior. Figure 2.5 illustrates the change from a free running VCO to a synthesizer output. The VCO close-in phase noise is removed by the PLL noise shaping. The noise contribution of the PLL is called integrator noise and creates a plateau as shown. This plateau is due to the noise generated by the PLL and will be as wide as the designer sees fit. The 3 dB width of the plateau is controlled by the loop design and VCO noise transfer function.

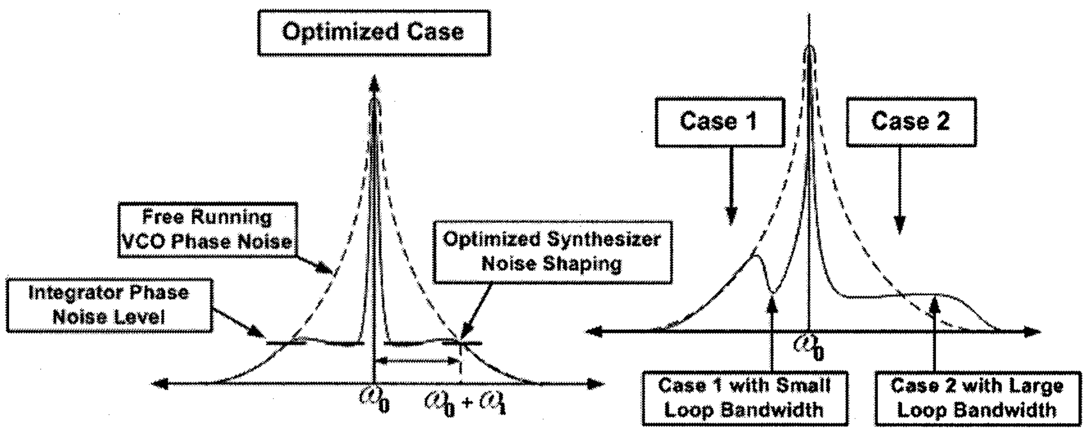

Figure 2.6 Integrator phase noise optimization

Figure 2.6 illustrates the three possible design outcomes for synthesizer output. Case 1 displays an under-designed loop bandwidth. This has the effect of not removing all of the VCO close-in phase noise. A characteristic side lobe is present in the synthesizer output where noise removal starts to fail. Case 2 has an over-designed loop bandwidth. In this case, the integrator noise plateau, introduced by the PLL, extends beyond the point of equal noise contribution. This point is where both the PLL noise and free running VCO phase noise contribute equally. A larger than necessary loop bandwidth will introduce more undesired noise in the system. The loop bandwidth in the optimized case is made so that the 3 dB plateau's edge coincides with the point of equal noise contribution. This has the effect of maximizing the noise removal while also generating the fastest settling time possible. The settling time is controlled by the loop bandwidth. The larger the loop bandwidth, the faster the settling time will be.

2.2.4.2 Settling Time in Second-Order Systems

The settling time is the time the PLL takes to shift from one frequency to another. It is one of the most important figures of merit in PLL design. The settling time can be calculated for a specific loop design, giving rise to a transient response. The settling time requirement is application specific. To obtain the settling time, a few assumptions and derivations need to be made. The first assumption is that we have a linear time invariant system, which implies a constant settling time regardless of the value of the voltage step. The second necessary assumption is that the desired damping factor is equal to one (ζ=1). This assumption actually optimizes the loop for fast response. This optimized response allows the fastest rise time without overshoot and consequently the shortest settling time [30]. The step response in this case is given by the following equation:

$$V_{out} \pm \Delta = \left(1 - e^{-\omega_n t} - \omega_n \cdot te^{-\omega_n t}\right) \cdot V_{step} \qquad \text{Eq. 2.14}$$

This expression models a second-order step response with respect to a change in voltage. V_{out} is the final VCO control voltage, V_{step} is the voltage step corresponding to the frequency jump, t is the required settling time, Δ is the required accuracy to be considered in lock condition, and ω_n is the natural frequency of the synthesizer. The voltage values are obtained from the VCO frequency vs. control voltage characteristics. What needs to be determined now is the time it would take for the system to reach the final value within a specific accuracy Δ. This equation can be solved graphically in order to find ω_n corresponding to the desired settling time t and required accuracy Δ. Once the natural frequency is obtained, the loop filter can be designed to meet the requirements. One must make sure that the behavior of the system is second order to use the method described above. It can also be used to provide a first approximation for a third-order system when its behavior follows closely that of a second-order model. Such a case is presented in the following chapter.

2.3 Static versus Fractional-N Topologies

A static design would have a specific integer divider value for each channel needed by the application. The disadvantage of this is that the minimum frequency resolution is set by the reference frequency. To obtain good resolution, the reference frequency has to be kept small. This will force the use of a large value of dividers (N). As noted earlier, the noise magnitude increases as N increases.

In the case of a fractional-N implementation, a single dual divider circuit is needed. The implementation is capable of generating fractions of the reference frequency such that it can be increased. This effectively reduces the value of N. As previously mentioned, this reduces the noise in the system. The only compromise to this approach is the fractional spurs that appear at the synthesizer's output.

2.3.1 Fractional Spurs

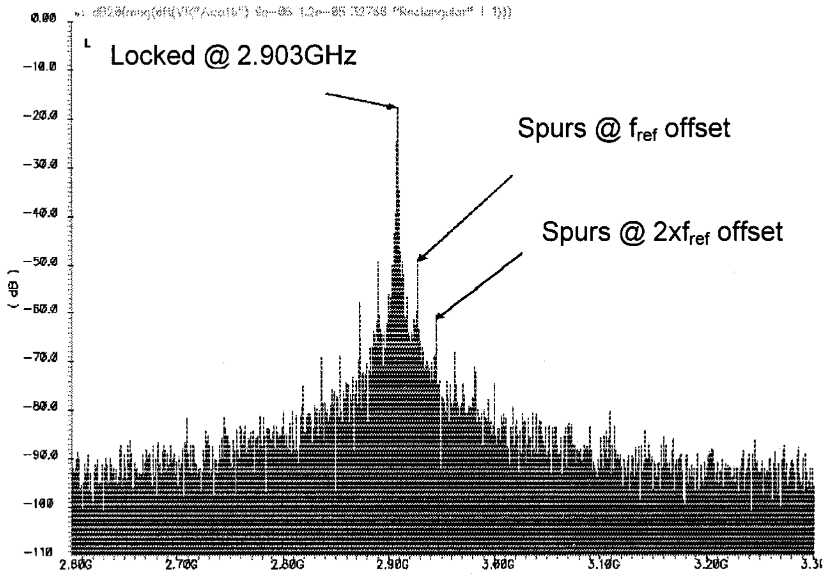

Figure 2.7 Example of spurs in a synthesizer output power spectrum

Figure 2.7 is an example of fractional spurs present in the synthesizer output spectrum. These spurs are due to the periodicity of the control signal of the dual modulus divider. They appear in the spectrum at a specific frequency offset away from the main tone of the synthesizer. This frequency offset is M times the reference frequency, where M is an integer.

2.4 IEEE Standard 802.11a & HIPERLAN/2

2.4.1 Spectrum

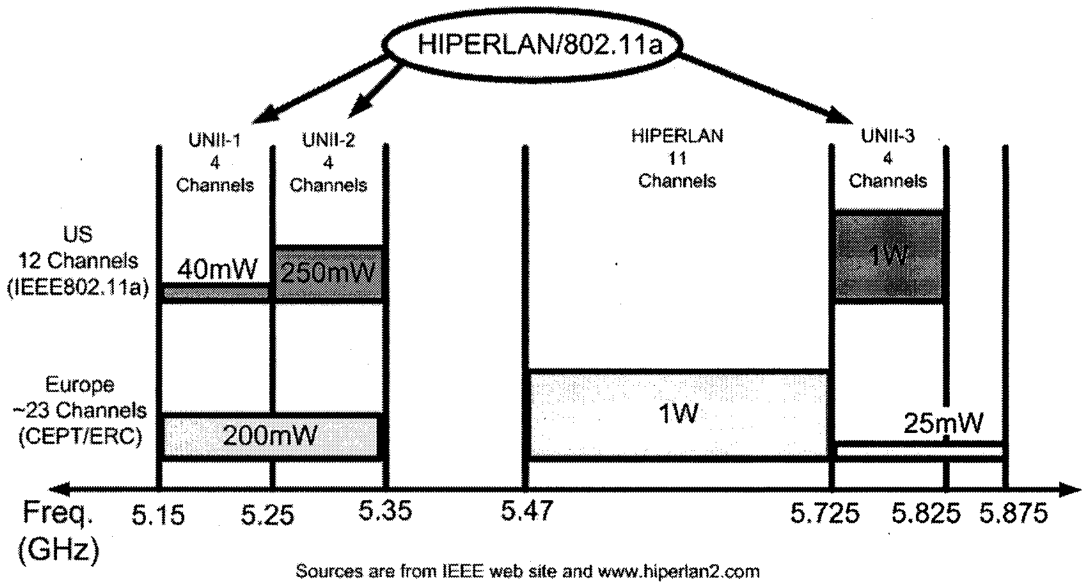

Figure 2.8 HIPERLAN/2 and 802.11a spectrum regulations

Figure 2.8 illustrates two main operating specifications, namely the allowed power levels and the sub-divisions of the 5 GHz frequency band. Note that the number of channels available in Europe is almost twice that in the US. Figure 2.8 also presents an overlap in specific channels where a WLAN system could operate both in Europe and in the US. The information has been gathered from references [31]-[33]. The WLAN is available now in the US from vendors such as Atheros, Intel, Cisco, and Proxim. Note that they only operate in the lower and mid bands from 5.15 to 5.35 GHz. It can be observed that over these particular bands, it can operate in Europe as well.

2.4.2 Transmit Power Spectral Mask

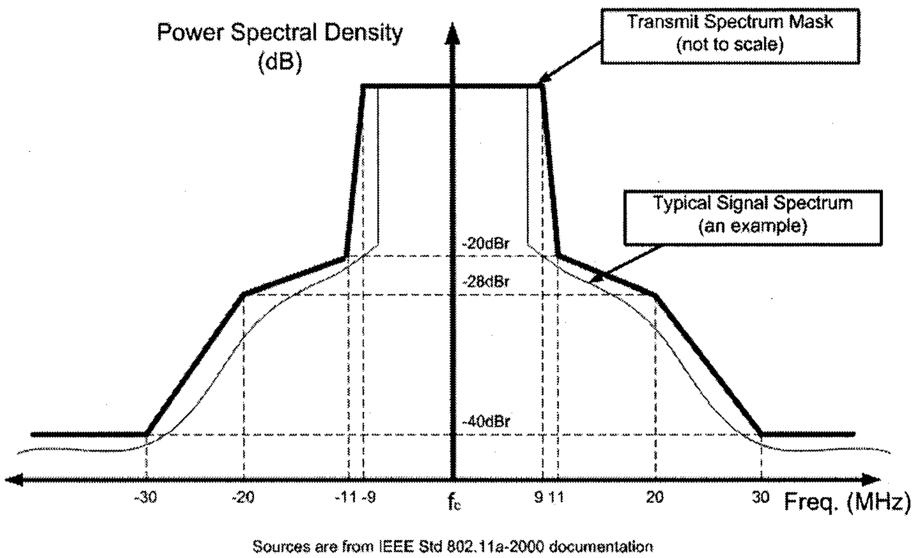

Figure 2.9 Transmit power spectral mask

Figure 2.9 illustrates the transmit spectrum mask of the IEEE 802.11a standard [31]. It shows a clear bandwidth of a little less than 20 MHz. The adjacent channels are exactly 20 MHz away on each side. To reduce co-channel interferences (CCI), two adjacent channels should not be used in the same cell. In fact, the company Atheros presents a spectrum management method in reference [34], where a single channel is used per cell.

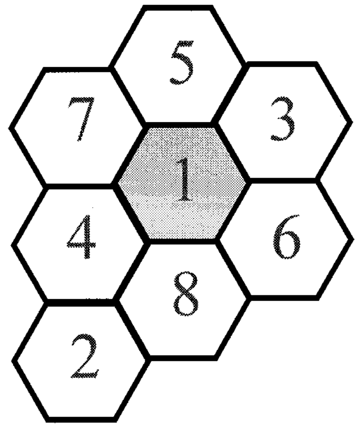

Figure 2.10 Spectrum management method to reduce CCI

Figure 2.10 illustrates the spectrum management method that minimizes the CCI. This method is used in office environments and is referred to as non-overlapping channels. The throughput can be maximized by reducing the cell radius. This approach reduces the requirements on distortion such as those caused by fractional-N PLL spurs, and power amplifier distortion.

2.5 References

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Chapter 3 Synthesizer Design

3.1 Synthesizer Building Blocks

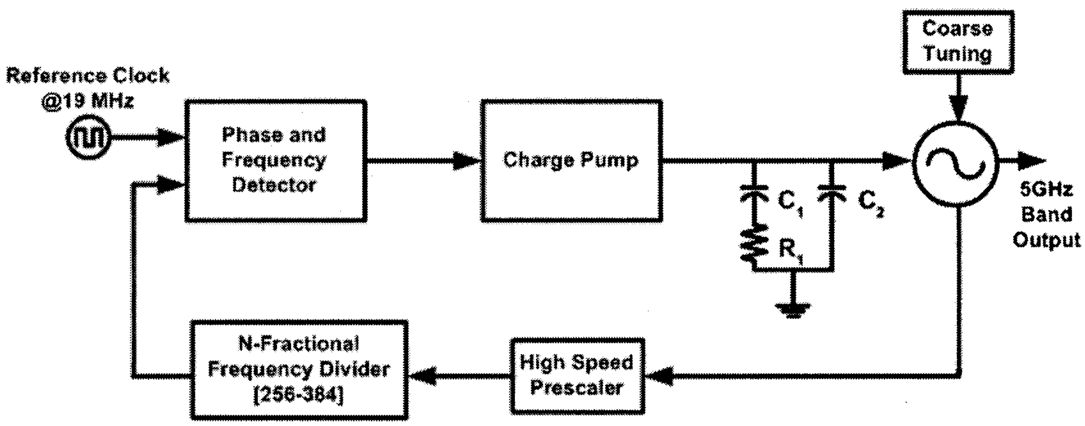

Figure 3.1 Synthesizer architecture

To meet the requirements of multiple band coverage and of the high-frequency resolution needed to enable every channel, a fractional-N PLL architecture is employed. Figure 3.1 shows the synthesizer architecture in detail. It allows the use of a relatively high-frequency reference signal, enabling higher loop bandwidth and faster locking time, while reducing the VCO phase noise. An external control provides coarse tuning of the VCO, while the PLL provides the fine automatic tuning.

The following sections present the building blocks used in the implementation of the frequency synthesizer. The choice of each block structural design will be discussed in detail. Their individual effect on the overall behavior of the system and the specific characteristics involved in their design and layout will also be presented.

3.1.1 Prescaler

The prescaler needs to operate at the highest frequency of the circuit. It will perform frequency division of the VCO signal so that the more complex divider circuit be able to operate at lower frequencies, where its performance is optimal. These devices are not only the bottleneck in the maximum operating frequency, but they also consume a relatively high dynamic power.

$$P_{dyn} = C_{Load} V_{DD}^2 f \qquad \text{Eq. 3.1}$$

Eq. 3.1 illustrates the relation of the dynamic power consumption P_{dyn} to the operating frequency f, supply voltage V_{DD}, and capacitive load C_{Load} in digital circuits [35]. This equation was used as a guideline to optimize the prescaler for low-power operation. Since the frequency is set by the application, reducing the supply voltage and the capacitive loading of the circuit are the only two parameters available for setting the dynamic power consumption.

It is well known that the two main limiting factors in high-speed designs are the series resistances of the interconnections and the loading of the parasitic capacitances. These two combine to form dominant parasitic poles in circuits, limiting the maximum operating frequency. To optimize for high-frequency operation, it is very important to follow specific layout guide lines.

Also, it should be noted that parasitic capacitances occur between metal traces carrying different signals, ground/supply lines, and other biasing interconnects. It is know that these capacitances couple noise and signals between any of the aforementioned structures, and as frequency increases their impedances are reduced resulting in even greater signal and noise coupling. Therefore, as the supply voltage is reduced, it becomes very important to minimize coupling between structures to maximize signal integrity.

From the above mentioned issues, a list of specific guidelines were established to optimize the circuit layout for low-power, low-supply voltages, and high-speed operation. In short, a reduction in parasitic capacitances improves all of these issues. This approach will be the main focus of the following layout guidelines.

3.1.1.3 Interconnections Design Rules

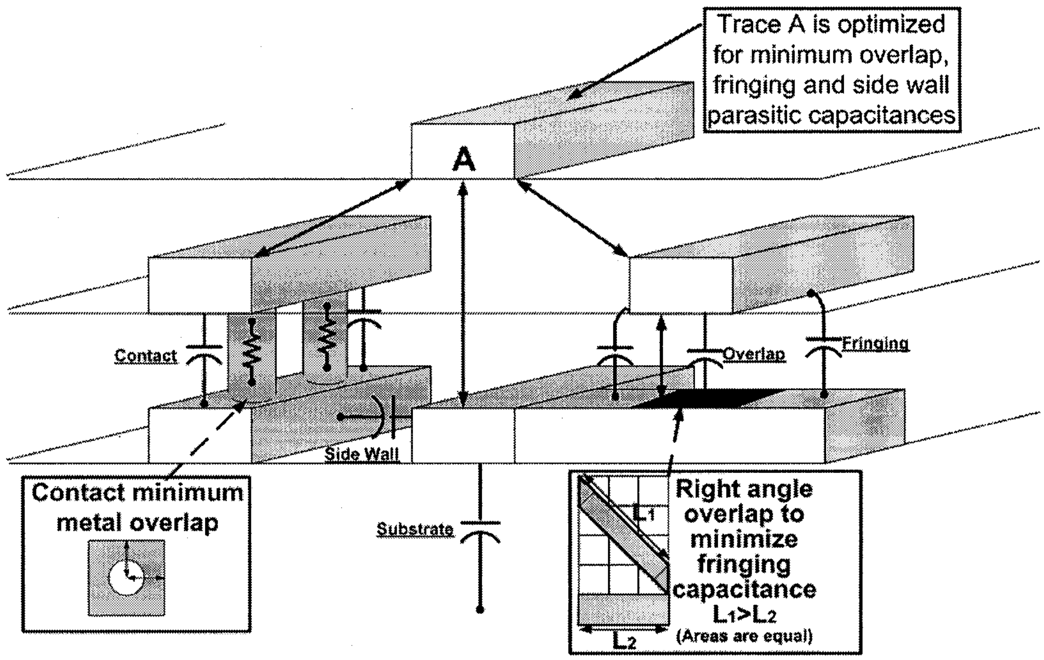

Figure 3.2 Description of layout issues

3.1.1.3.1 Rule 1- Interconnection Dimensions

$$\lambda_{Physical\_Dimension} << \lambda_{Operating\_Frequency} \qquad \text{Eq. 3.2}$$

The lengths of the interconnects must be kept as short as possible to reduce the non-desirable high-frequency effects, and to keep the modeling of the interconnection as ideal wires. Failure to do so will turn a long trace into an inductor, and it will have more resistance, resulting in an increase in signal loss. Large traces also increase capacitive loading effects. Eq. 3.2 is a rule of thumb in high-frequency design in order to maintain ideal wire behavior of interconnections. By keeping the physical dimensions of the circuitry much smaller than the operating wavelength, the absence of standing waves and wave reflections can be assumed. There are only very small losses due to the interconnects left, and no high-frequency modeling is necessary.

$$\alpha = \frac{\omega\sqrt{\mu\varepsilon}}{\sqrt{2}}\left[\sqrt{1+\left(\frac{\varepsilon''}{\varepsilon'}\right)^2}-1\right]^{\frac{1}{2}} \qquad \text{Eq. 3.3}$$

$$\beta = \frac{\omega\sqrt{\mu\varepsilon}}{\sqrt{2}}\left[\sqrt{1+\left(\frac{\varepsilon''}{\varepsilon'}\right)^2}+1\right]^{\frac{1}{2}} \qquad \text{Eq. 3.4}$$

$$E_x^+(z,t) = E_m^+ e^{-\alpha z}\cos(\omega t - \beta z) \qquad \text{Eq. 3.5}$$

Eq. 3.3 to Eq. 3.5 from reference [38], illustrate the effects of frequency on a forward traveling wave in a conductor, where α represent the attenuation, ω the frequency and β the phase shift. An increase in frequency introduces an increase in loss and phase shift. The phase shift is usually modeled by introducing capacitors and inductors in the transmission line model. It can be observed that by keeping the dimensions small, the term βz has limited effects on the traveling wave. This proves the veracity of the aforementioned rule of thumb.

3.1.1.3.2 Rule 2- Substrate Parasitic Capacitance

$$C = \frac{\varepsilon \cdot Area}{d} \qquad \text{Eq. 3.6}$$

The width of the traces close to the substrate must be kept as small as possible to prevent generating large substrate capacitances. This will prevent large capacitances to couple signals to the substrate and slow down the circuit. Figure 3.2 illustrates this layout issue. Eq. 3.6 represents the well known parallel plate capacitance equation, where the plate area *Area*, multiplied by the effective permittivity of the insulator ε, in this case the substrate, is divided by the distance d between the two plates.

3.1.1.3.3 Rule 3- Overlap and Fringing Parasitic Capacitances

Parasitic capacitances between two overlapping traces must be minimized in order not to degrade the circuit operation. The distance between the two overlapping structures must be kept as wide as possible, and the overlap area must be minimized. The fringing capacitances must also be minimized. One key technique is to always run overlapping traces at right angles. Figure 3.2 demonstrates that a right-angle overlapping minimizes fringing capacitance for two different parallel plates having equal areas. It is clear that L_1 is much larger than L_2; therefore L_1 is more prone to generating fringing capacitances.

3.1.1.3.4 Rule 4- Side-Walls Parasitic Capacitance

When carrying out the floor planning of the circuit it is important to keep in mind a few key points. Having two wires running too close to each other gives rise to cross-talk. Cross-talk is due to parasitic capacitances of the traces side walls. The side walls act as parallel plate capacitors and couple AC signals. To prevent cross-talk, the distance between side walls must be relatively large. When this is not possible, two different metal layers should be used to increase the effective distance.

3.1.1.3.5 Rule 5- Metal Contacts Parasitic Resistances and Capacitances

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma_{conductor}}}, \; R_{AC} = R_{DC}\frac{a}{2\delta}, \; R_{DC} = \frac{1}{\pi a^2 \sigma_{conductor}} \quad \text{Eq. 3.7}$$

When using contacts to connect two metal layers, contacts should be placed as frequently as possible to reduce the added contact resistance and to increase the amount of current the connection can sustain. Individual contacts are limited in their current carrying capacity. A safety factor is often necessary to overcome process variation. In this work a safety factor of at least 15% was used. The number of contacts needs to be optimized to decrease series resistance while not degrading the frequency response by introducing large parasitic capacitances. To minimize the metal overlap parasitic capacitances, the minimum metal-contact overlap area must always be used. This minimum metal-contact overlap area is guided by the DRC rules of each specific process. Figure 3.2 illustrates this issue. Eq. 3.7 from reference [39] describes the skin depth δ as a function of frequency f, permeability μ, and conductivity $\sigma_{conductor}$. Also described, is the AC resistance R_{AC} of a cylindrical conductor as a function of the skin depth, conductor radius a, and DC resistance R_{DC}. Note that R_{DC} is also a function of $\sigma_{conductor}$ and a. Also note that the expression clearly illustrate that an increase in frequency will increase the resistance. Therefore, as the frequency of operation is increased, the current handling capacity of the contact will be reduced due to skin effects. This is very important for the interconnect design of metal contacts for high frequency of operation. The same issue applies to all shapes of conductors with different modeling equations.

3.1.1.3.6 Rule 6- Required Current Densities

It is required to keep the traces large enough to satisfy their rated current densities capabilities. Failure to do so will increase the resistance seen by the signal, resulting in signal loss and heating of the conductor (and eventually the entire chip). Excessive heating will affect the behavior of the circuitry, possibly rendering it unusable or enduring permanent damage. Traces can be modeled: Their resistive behavior as a function of frequency would be very similar to Eq. 3.7, i.e. their current density handling capacity will decrease with frequency.

Rules 1 to 6 will minimize the loading effect of the interconnections and, as mentioned earlier, this will dramatically reduce the dynamic power consumption. If a low supply voltage is used, the dynamic power consumption will decrease even further. Note that the reduced capacitive loading will improve the operating frequency very rapidly if all rules are satisfied. Also, limiting signal and noise coupling between traces improves the overall noise immunity of the circuit.

3.1.1.4 Transistor Layout Design Rules

To optimize the power consumption and the operating speed of the transistors some design rules must be followed. The optimized minimum width and length of the transistor channel must be used. Using the smallest featured dimensions for the gate length allowed by the process will enable the fastest operating frequency. Optimizing the transistor width will give rise to the maximized current drive for minimum parasitic capacitance, thus enabling the highest frequency of operation possible.

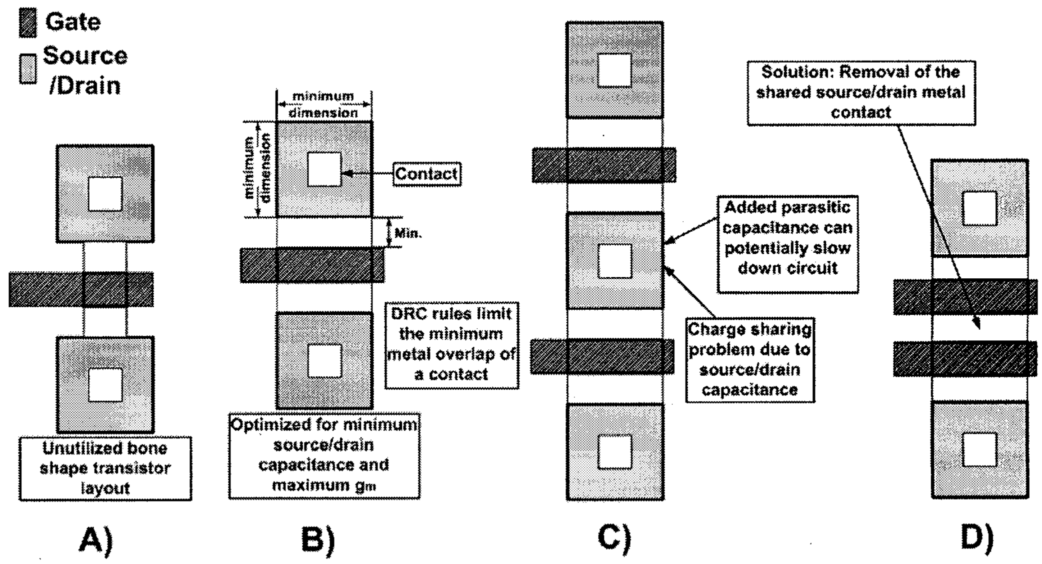

Figure 3.3 Transistor layout issues

Figure 3.3 illustrates many key points in transistor layout. Transistor A illustrates the bone-shaped transistor. This type of structure is not optimized, having large capacitances compared to their current drive. The only case when they may be useful is when they are not required to switch quickly, and when it is necessary for them to have very little current drive. On the other hand, transistor B is the optimized layout for maximum drive and frequency. Also, using the minimum optimized width, as the standard transistor cell, enables small currents to be used, effectively lowering the overall power consumption. Transistor C has a useless source/drain capacitance often forgotten when using transistors directly from a standard device library. In the case of pushing the edge of the process frequency of operation, custom layout of transistors is necessary. Transistor D illustrates a proper layout for high-speed transistors. It reduces the problem of charge sharing. Also, it enables less interconnections and a more compact layout. Note that the gate to gate distance is also limited by the DRC rules, i.e., the process characteristics.

To improve signal isolation, the sharing of guard rings around specific groups of devices is necessary. One of the most important elements in minimizing the parasitic capacitances in a layout is to maximize the sharing of the source/drain contacts and the metal of common node transistors. This is even more important in multi-finger layouts, where interdigitization is used to maximize transistors matching.

3.1.1.5 Fully Differential Circuit Architectures

Fully differential circuit architectures must be used to improve noise immunity. Since supply voltages are considerably reduced to minimize power consumption, this type of architectures is necessary. They may result in an increase in transistor count, but this is easily justified by a dramatic supply voltage reduction. To prevent forming mismatches in signals delays, high symmetry of the circuit layout is required. At high speeds, timing of digital circuitry is crucial for optimal performance of synchronous and asynchronous switching.

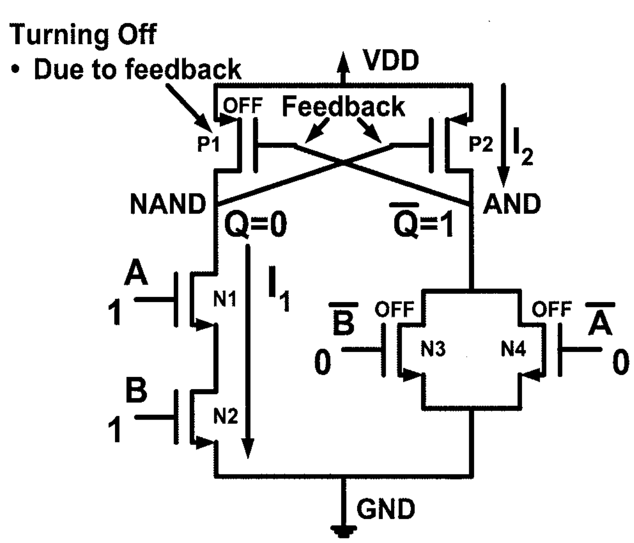

Figure 3.4 DCVSL NAND logic gate

Figure 3.4 shows the differential cascode voltage switch logic (DCVSL) gate transistor level implementation for high speed digital logic [35]. The fast response of this circuit is mainly attributed to the feedback provided by the two PMOS loads. These two PMOS transistors are designed to be as small as possible to minimize their parasitic capacitances, and further maximize speed. The NMOS transistors can also be kept small, since they only drive small capacitive loads. An added advantage to this logic family is the absence of static power consumption. The minimum sizing of the transistors results in further reduction of the power consumption. For this same reason, minimum size transistors were used whenever possible throughout the other designs in this work.

3.1.1.6 Prescaler Transistor Level Implementation

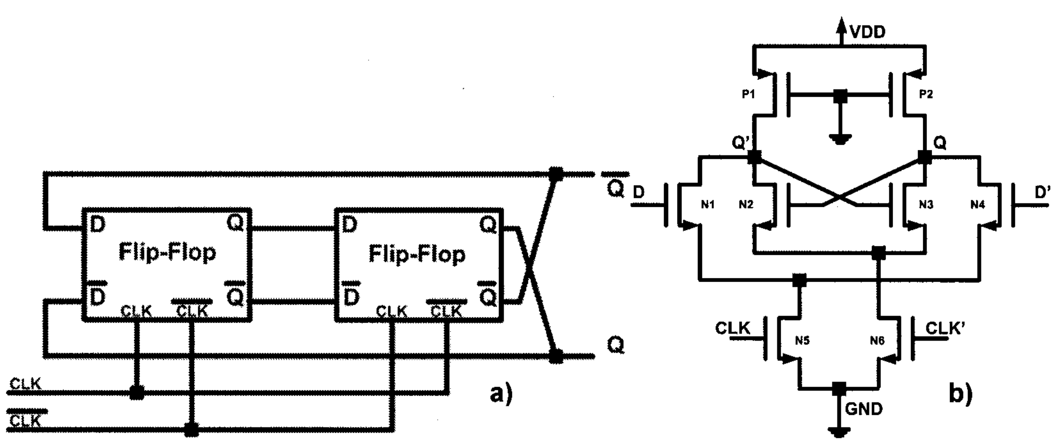

Figure 3.5 a) Divide-by-two circuit building block, b) D-flip flop transistor level circuit

The implementation consists of a conventional two D-flip-flop counter design [35], [42]. Figure 3.5 shows the implementation of the divide-by-two prescalers and the DFF circuit level implementation. The DFF is fully differential. It uses a small PMOS active load and an optimized transistor layout for high speed operation. It also has a memory feedback element composed of N_2 and N_3, which effectively stores the output during the second half cycle, i.e., when *CLK'* is asserted high.

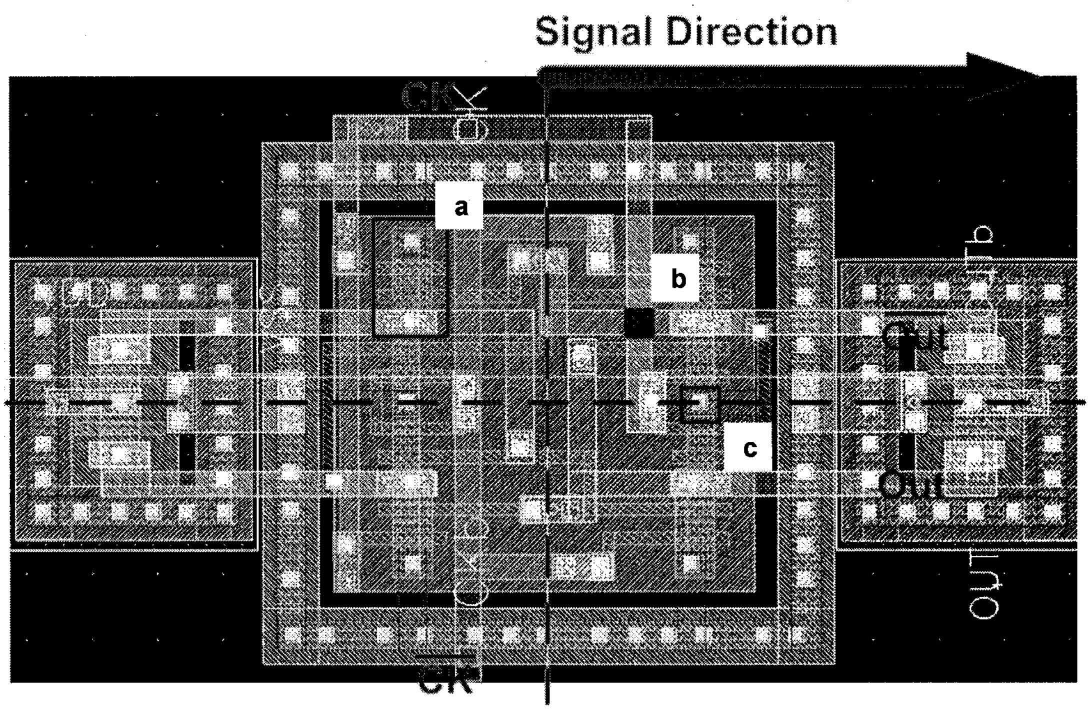

Figure 3.6 High-speed prescaler design respecting rules 1 to 6.

Figure 3.6 illustrates the prescaler layout following the high-speed, low power design rules, whenever applicable. We can see that two axes of symmetry are used to minimize delay mismatches. Also different rules are highlighted, a) the removal of unnecessary source/drain, b) 90° minimum metal overlap and fringing capacitance, and c) minimum contact-metal overlap. The dimensions of the interconnect were kept to a minimum to prevent undesired high-frequency effects.

The signal propagation starts from left to right and guard rings are used. Both techniques are known to improve signal isolation and minimize feedthrough.

3.1.2 Fractional-N Divider

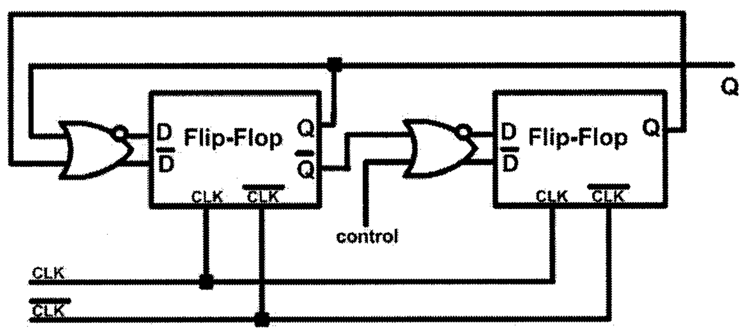

Figure 3.7 Dual modulus divider

3.1.2.1 Dual Modulus Divider

The fractional-N divider allows the fine frequency resolution. The implementation is based on the counter circuit shown in Figure 3.7 [41]. Figure 3.5 b illustrates the DFF used. In this implementation, the NOR gate was a DCVSL type, again to benefit from its high speed. By modulating the duty cycle of the control signal, it is possible to create fractional dividers. The fractional divider in this system is a 2/3 dual modulus divider. Figure 3.8 displays simulation results for operation at *800 MHz*. The input signal is first divided by 3 for the number of input cycles A, then by 2 for the number of input cycles B. The time span covered by the sum of cycles A and B represents the period of the control signal. The division ratio is the result of the time average given by reference [36].

$$ratio = \frac{A+B}{\frac{A}{3}+\frac{B}{2}} = \frac{24+14}{\frac{24}{3}+\frac{14}{2}} = 2.533 \qquad \text{Eq. 3.8}$$

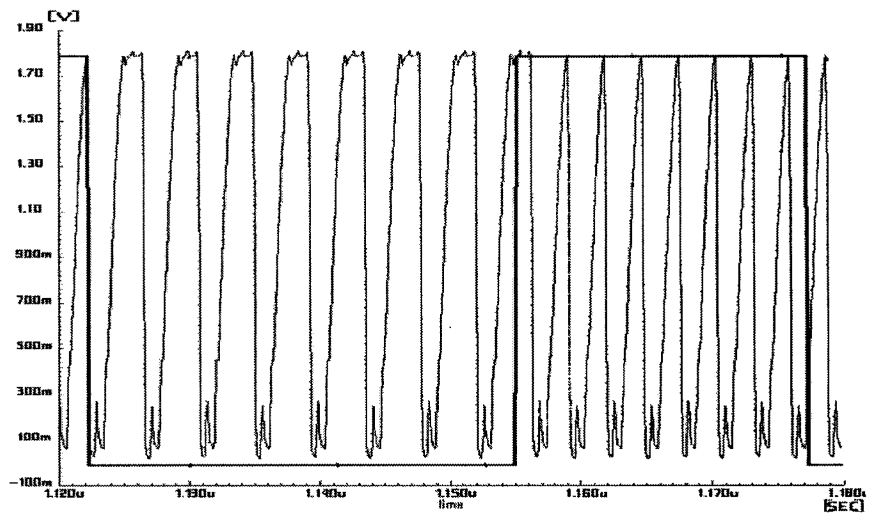

Figure 3.8 Dual modulus divider output

In simulation, the narrowest achievable control pulse was 1.3 ns wide, suggesting the capability for a very high frequency resolution. The fractions available from the combined fractional-N divider and prescaler allow a wide range of dividers, 256 to 384. The actual synthesized frequencies at the output of the VCO are *M* times the reference frequency, where *M* is the divider value. In this case, using a reference signal of roughly *19 MHz*, frequencies over a wide range starting from *4.8 GHz* to *7.3 GHz* can be generated. As previously noted, the actual frequency generation range is limited by the VCO.

3.1.3 Phase and Frequency Detector (PFD)

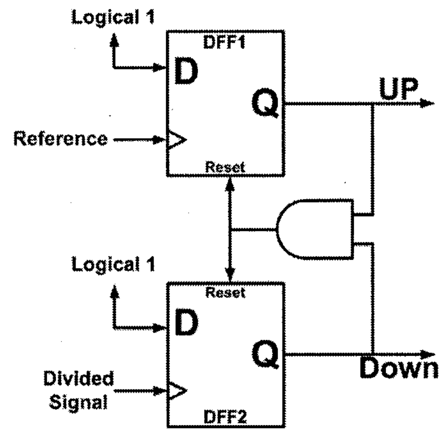

Figure 3.9 Conventional PFD block implementation

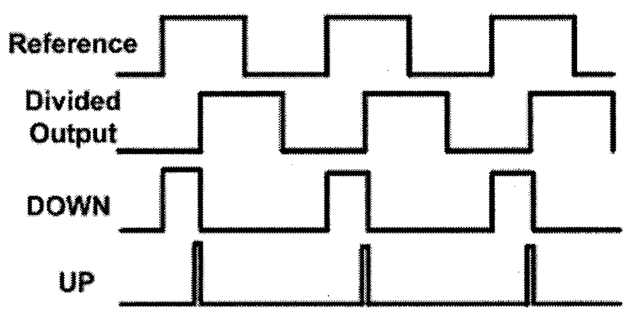

Figure 3.10 PFD characteristic response

Figure 3.10 shows the characteristic response of the PFD circuit shown in Figure 3.9 [37]. When a clock is asserted high on any of the two D-flip-flops (DFF), its output goes high. When both DFF outputs are high, the AND gate will reset both DFF outputs to zero. The sharp pulses on the UP output signal, during the phase error detection, are due to the delay through the AND gate and the reset circuitry of the DFF. These signals will then be fed to the UP/DOWN input of the charge pump.

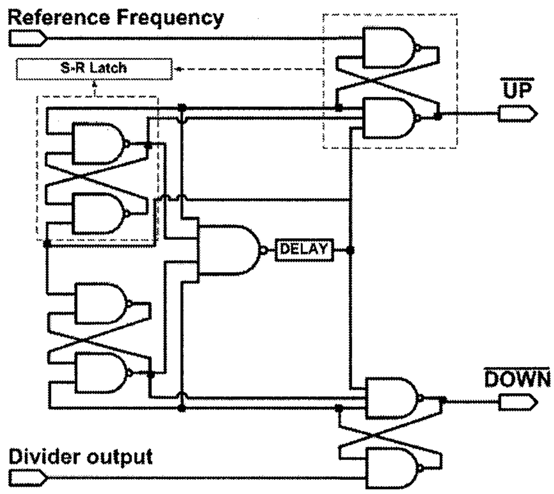

Figure 3.11 PFD gate level implementation

Figure 3.11 presents a gate level implementation of the previously discussed PFD circuit [37]. The DFF is implemented using two S-R latches, where the AND gate is integrated with the reset circuitry. Now the AND gate is replaced by a four-input NAND gate and the extra inputs come from the leftmost S-R latch. The minimum pulse width can be controlled by the delay element introduced after the four-input NAND gate. Figure 3.10, PFD characteristic response, also applies to this implementation with the added benefit that the minimum width of the sharp pulses on the UP output lines can be controlled by the added delay element. PFDs without delay element are known as conventional PFDs, and have a dead zone.

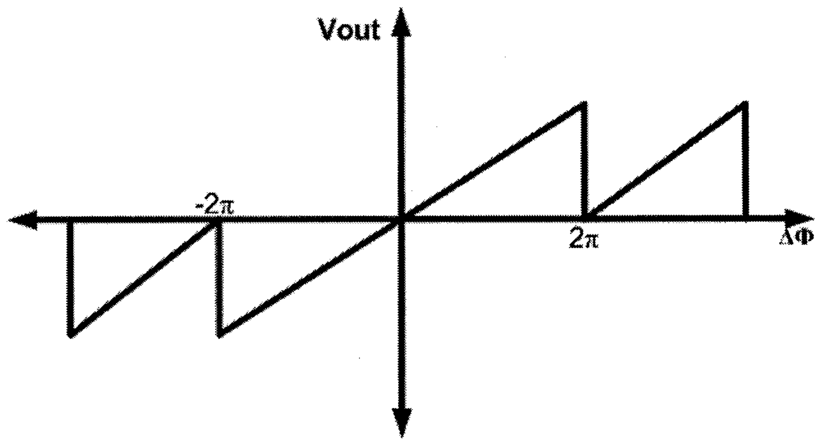

Figure 3.12 PFD response to phase errors and capture range

Figure 3.12 shows that the PFD capture range is limitless. Regardless of the frequency difference magnitude, the PFD will always respond correctly. This is not the case with phase detectors. We can see that this idealized response is linear for the $\pm 2\pi$ range. In reality, the PFD gain decreases for small phase errors, as technology and loading effects limit the rise and fall times. The pulse width cannot be reduced below a certain threshold value, while also reaching the supply.

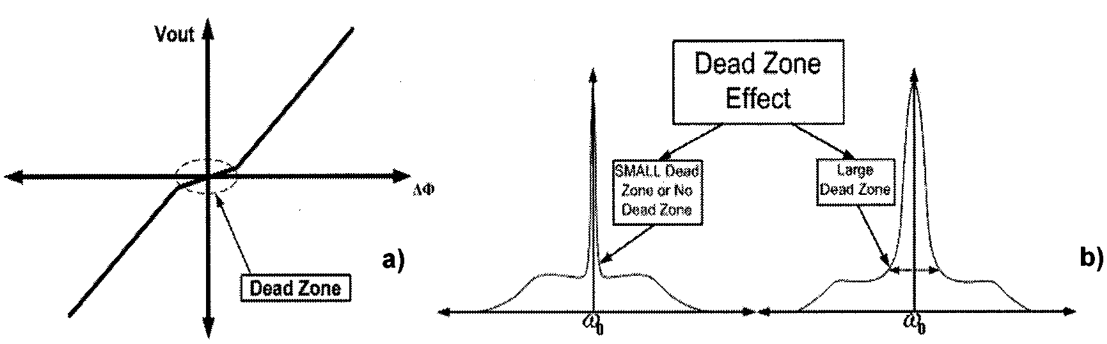

Figure 3.13 a) Dead zone in PFD and b) its effect on synthesizer output

Figure 3.13 a) shows the effect of a dead zone in the PFD response on the noise close to zero phase error. Figure 3.13 b) illustrates the difference between a synthesizer implemented with and without a dead zone. The width of the center tone is proportional to the width of the PFD dead zone. The method used to prevent this situation is to insert a periodic pulse on the output line of the PFD. As discussed earlier, the delay element generates minimum width for the pulse. Effectively, the pulse width is fixing the gain for small phase errors to a constant value (see Figure 3.10). Then, a phase error will vary the output pulse width. A lagging divided signal would create a wider pulse on the UP output, where the pulse on the Down output would be of minimum width. The charge pump would then pump a current proportional to the difference of the two pulses so that the VCO control voltage enables a locking transient. The minimum pulse width cannot be made arbitrarily long, since it is the limiting factor in the operating frequency of the PFD. The minimum reference signal period must be at least twice the minimum pulse width, so that a signal *180°* out of phase does not generate a PFD response that would overlap the next comparison cycle. Eq. 3.9 express the relationship between the minimum pulse width Δt and the maximum operating frequency for the PFD circuit.

$$f_{\max} = \frac{1}{2\Delta t} \qquad \text{Eq. 3.9}$$

3.1.3.1 Logic Gate Implementation Using DCVSL

The NAND gate building block of the PFD was implemented using the DCVSL logic family. Its differential structure was adopted for common mode noise immunity. The circuitry was optimized for fast response and for low power consumption. The fast response enables a smaller dead zone, since the constant gain region is reduced by a smaller minimum pulse width. The reduction of the requirements on the pulse width allows the maximum input reference frequency to be increased. An increase in the reference frequency pushes the fractional spurs further away from the communication channel. The increase in reference frequency corresponds to a possible decrease of the divider value N. Since N effectively multiplies the noise introduced by the reference, PFD, and loop filter, reducing it is important (see discussion in Chapter 2).

3.1.4 Charge Pump (CP)

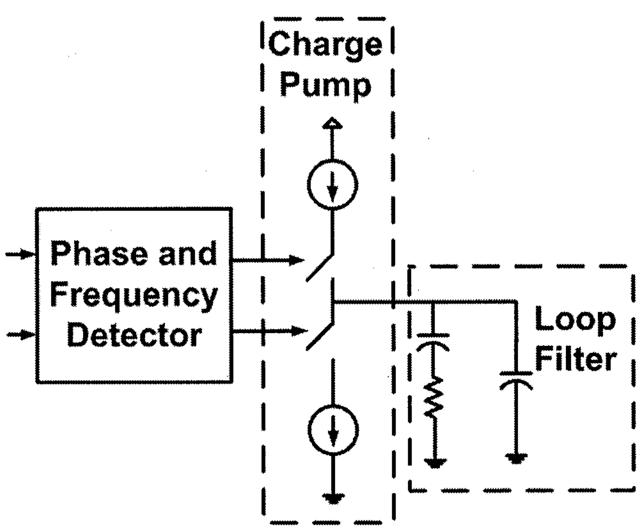

Figure 3.14 PFD/CP/LPF circuits

As previously discussed, CPPLLs have many great advantages over conventional PLLs. The capture range is only limited by the VCO output range, and static phase errors can be eliminated by adequate transistor matching of the CP.

A differential CP architecture was implemented for its known advantages in common mode noise rejection, removal of the mismatch problem, and charge sharing problem [37]. Figure 3.14 shows a charge pump where the two pumps must be matched. In a differential implementation, the PFD output triggers only the pull-down current sources and the pull-up current sources are passive. This effectively removes the need for well matched complementary current sources, i.e., matching between the NMOS and PMOS devices.

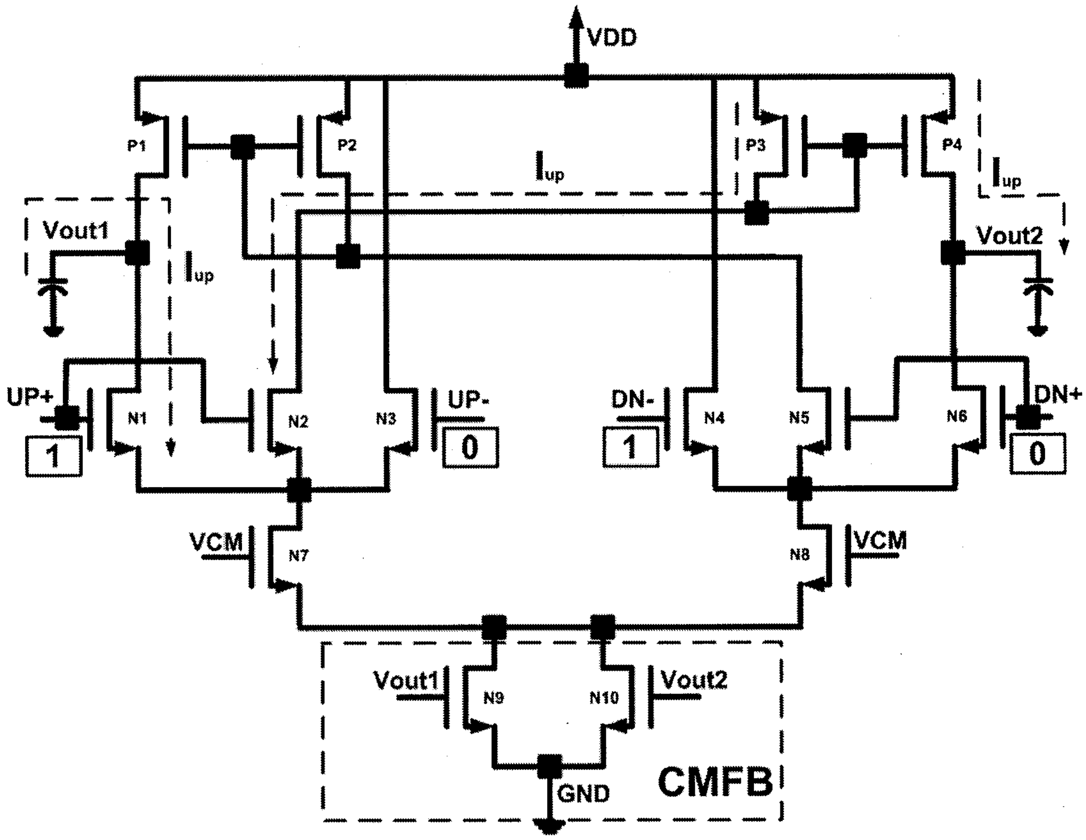

Figure 3.15 Fully differential charge pump circuit implementation

Figure 3.15 illustrates the operation of the CP: when UP+ is high, I_{up} is pulled off the load at V_{out1}, since both N_1 and N_2 are on and have a *1:1* sizing, I_{up} will also be drawn from P_3 and mirrored to P_4, since they also have a *1:1* sizing. This effectively has the action of pushing current on to the load at V_{out2}. The inverse is also true in the case of DN+ being high. Since the NMOS transistors N_1 through N_6 are matched, the currents are identical and no charges are added or removed from the loads when both UP+ and DN+ are logical ones. The common mode feedback at the base of the circuit limits the amount of current that can be driven and keeps the internal nodes of the circuit at proper DC levels.

When both the UP and Down inputs are equal to zero, transistors N_3 and N_4 prevent N_7 and N_8 from slowly discharging the output nodes V_{out1} and V_{out2}. This discharge would be due to the problem of sub-threshold current in the NMOS devices [37] and noise on the input lines. Without N_3 and N_4, N_7 and N_8 would increase the drain-to-source voltage (V_{ds}) of both N_1 and N_6, increasing the sub-threshold current. But instead, V_{ds} is almost zero, if not less than zero. In fact, N_1 and N_6's V_{ds}'s would be equal to approximately $[V_{out} - (V_{dd}-V_{tn})]$, when neglecting the body effects. Since V_{out} is necessarily less than or equal to V_{dd}, the maximum V_{ds} is V_{tn}. By having N_3 and N_4 turned on, their source voltages will be very close to the supply.

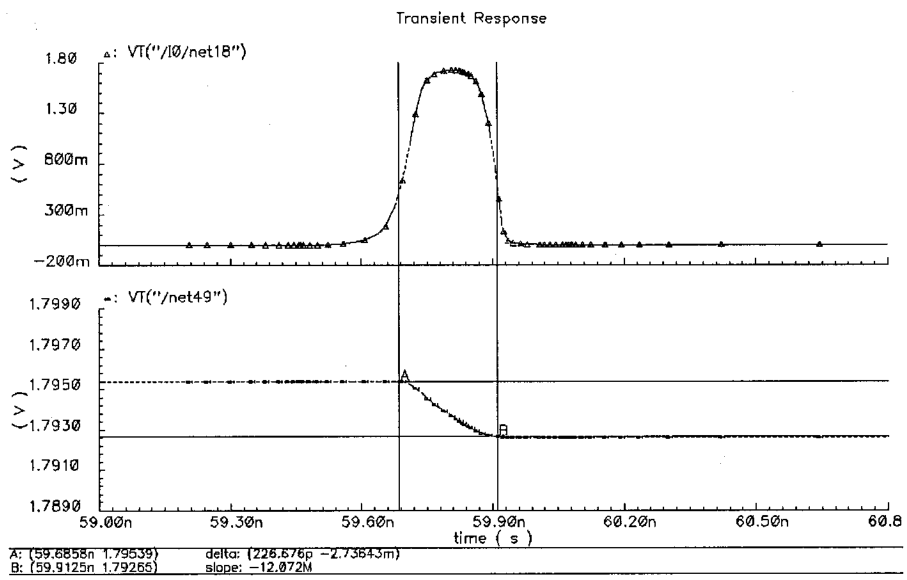

Figure 3.16 Simulated minimum linear output of PFD and CP

Figure 3.16 shows the response of a conventional PFD and CP at the edge of the linear region, just before the dead zone. The pulse has rounded edges. This small pulse corresponds to a control voltage variation of *~2.7 mV*. From experimental measurements, *2.7 mV* is well below the peak-to-peak noise jitter levels of the external DC supplies. This is an indicator of the PFD/CP combination's high-precision performance. For example, a VCO having a gain of 100 MHz/V corresponds to a maximum error of 270 kHz, which is not enough to lose lock condition in the 5GHz WLAN application. Also, the non-linear PFD region can still give rise to frequency corrections, effectively reducing the error to just a few kHz. In the case of an external loop filter, experimental measurements show that noise on the VCO control signal can reach peak-to-peak values of *80 mV* and beyond.

3.1.4.1 Charge Pump Layout Considerations

Figure 3.15 illustrate a schematic-level design with a perfect symmetry axis across the supply to ground. By folding the circuit about this axis and interdigitizing the overlapping transistors in a common centroide fashion, an extremely high level of matching can be obtained.

3.1.5 Loop Filter

In this design the loop filter is the load of the CP. It consists mainly of a capacitive load, and parts of it was kept off chip. This approach enables the loop filter to be redesigned if necessary. As previously discussed in Chapter 2, in order to ensure stability, a resistor needs to be added in series with the load capacitor [37]. Figure 3.14 illustrates this configuration and also shows an additional capacitor in parallel with the two. The purpose of this second capacitor is to remove unwanted noise at high frequencies [37]. This will give rise to a cleaner and smoother control signal for the VCO.

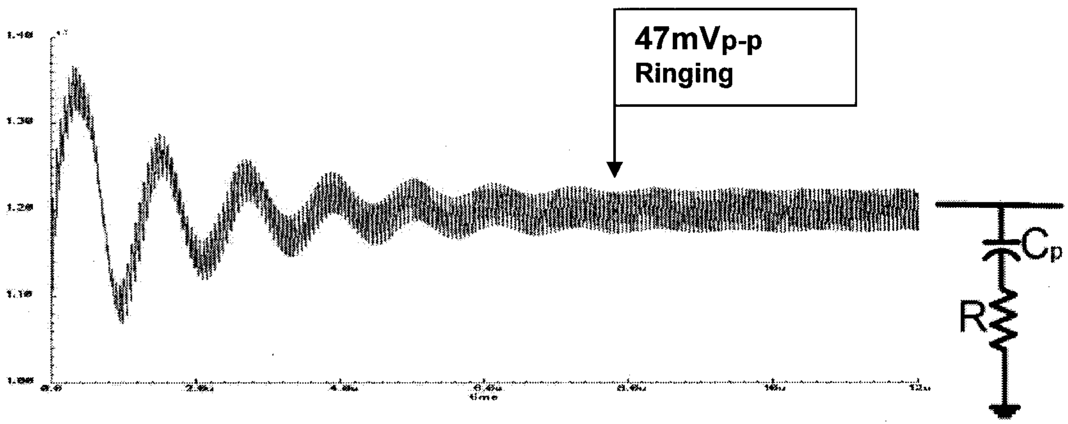

Figure 3.17 Simulated oscillator control voltage locking transient for a first-order filter

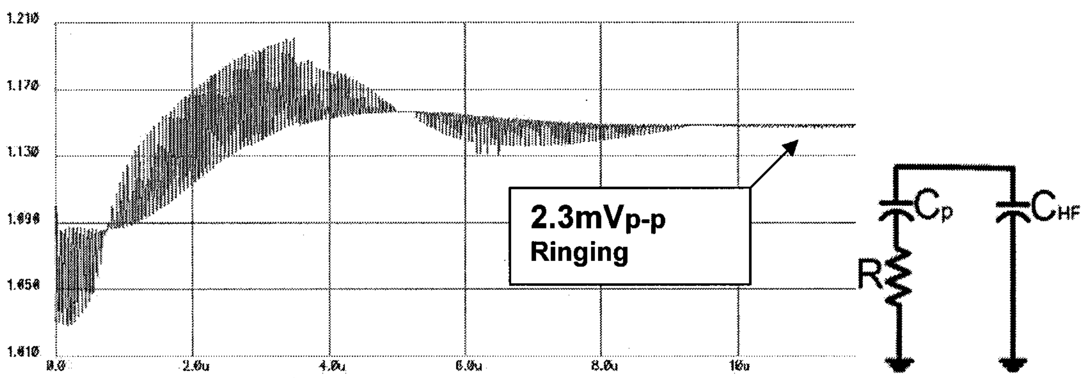

Figure 3.18 Simulated oscillator control voltage locking transient for a second order filter

Figure 3.17 and Figure 3.18 illustrate the advantage of including the extra parallel capacitor. It is clear that most of the high-frequency noise is removed from the control voltage by the addition of the second pole, with little or no effect on the settling time of the CPPLL. The actual reduction of the ringing is from $47\ mV_{p\text{-}p}$ to $2.3\ mV_{p\text{-}p}$. The ringing shown in the simulated results are in no way comparable to the expected measurement results. It should be expected that higher levels of noise may come from the DC supplies.

The mathematical modeling of the CPPLL was introduced in Chapter 2. The equations for the natural frequency and the damping factor were also presented. Here, we are dealing with a third-order PLL due to the addition of the parallel capacitor. The insertion of this extra pole is critical, and in this case its purpose is to remove undesired ripples caused by high-frequency noise. To achieve the necessary results, the pole must be placed above the natural frequency, so that the gain fall-off is increased for high frequency noise. This effectively changes the drop per decade from 40 dB to 60 dB. On the other hand, placing the pole away from the loop bandwidth has little or no effect on the loop behavior. So, as described in Chapter 2, the natural frequency and the damping factor are governed by the two following equations:

$$\omega_n = \sqrt{\frac{I_{CP}}{2\pi C_p}\frac{K_{VCO}}{N}} \qquad \text{Eq. 3.10}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{CP}C_p}{2\pi}\frac{K_{VCO}}{N}} \qquad \text{Eq. 3.11}$$

3.1.5.1 Loop Filter for Low Power Design

To achieve low-power design, two things are required: a relatively low voltage supply and small currents. In our CPPLL design, a low-power implementation can be obtained by reducing the CP's pumping current. The current labeled I_{CP} in the two equations can be scaled down by compensating with the capacitor C_p and the resistance R. For the natural frequency which set the upper bound on the loop bandwidth and the settling time, a decrease in I_{CP} can be overcome by a decrease in C_p. For the damping factor, generating a small I_{CP} with a small C_p can be compensated for by increasing R. Since R is not affected by the square root term, its increase will not be dramatic. Obviously, small current means small slew rate, but a compromise can easily be obtained by a proper choice of R, since it is the dominant term in the damping factor equation.

From Chapter 2, we know that the natural frequency is set by the required settling time of the application. In the case of a CPPLL, the charge pump current is taken into consideration, and a low-power system can then be designed. Depending on the power budget of the overall system, a value of current will be assigned to the charge pump. From this result, the capacitor C_p is chosen, the VCO gain is set by the VCO tuning method, and the divider values are set by the requirements on the frequency synthesis range. Then, the value of the resistor is set to obtain an optimized damping factor value of $\zeta=1$.

The second parallel capacitor C_{HF} is made at least ten times smaller than C_p, so that it does not affect the settling time, natural frequency, and damping factor of the system. As previously explained, its purpose is to remove high-frequency noise on the control line. It must be understood that this analysis is a first approximation, and Hspice simulations give a more accurate and better understanding of the loop behavior. Also, since the divider value will not remain constant for all frequencies generated, the design must take this into account and meet specifications across the entire frequency range.

3.1.5.2 Loop Transient Response Example

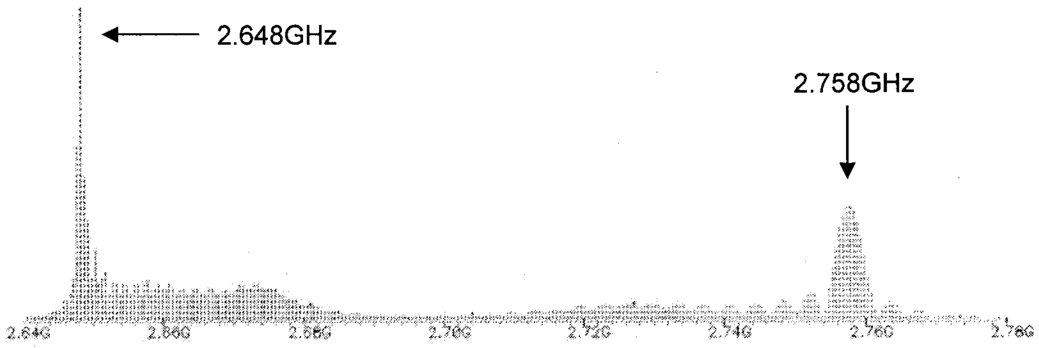

Figure 3.19 FFT of a simulated locking transient

Figure 3.19 is the resulting fast Fourier transform (FFT) of a 2.5 GHz CPPLL design. It shows an initial frequency of approximately 2.758 GHz; once the PLL is turned on, the feedback adjusts the VCO to 2.648 GHz. We can clearly see the noise shaping effect of the PLL on the spectrum. The reason the magnitude are at such an offset is that the FFT is accumulating power over time in each frequency bins, so the offset only means that most of the power within the transient is centered at 2.648 GHz.

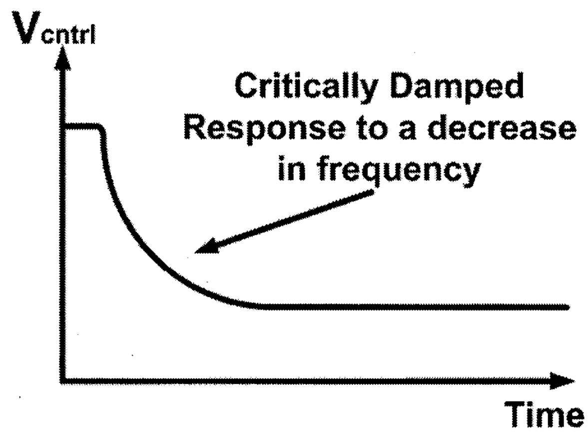

Figure 3.20 Theoretical damped transient response

Figure 3.20 illustrates a theoretical VCO control transient response that would generate such an FFT [30]. Figure 3.19 presents a plateau from 2.65 GHz to 2.68 GHz which is caused by the slow portion at the end of the 2nd order exponential decay, and by the PLL noise shaping. The plateau is not symmetric in this case because the transient response is limited in time and no power was accumulated at these frequencies during the sampled response.

3.1.6 The VCO

In this CPPLL implementation, the use of ring oscillators is ruled out due to their high phase noise. An LC-tune oscillator approach has been selected instead because of its superior high frequency operation performance. In order to maintain a high level of integration and keep the dimensions as small as possible, the transceiver design must use an on-chip VCO with on-chip inductors. Then, inductors design becomes the main bottle neck in achieving low phase noise.

3.1.6.1 LC-Tuned VCO Design

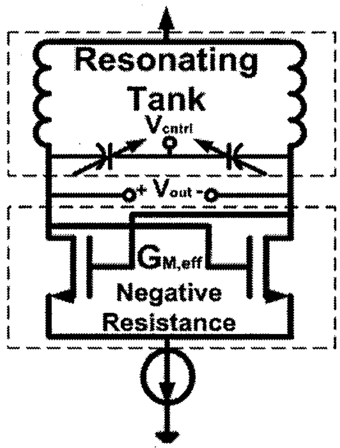

Figure 3.21 Typical LC tuned oscillator

The LC-tuned VCO is based on two components, the resonating tank and the concept of negative resistance. Figure 3.21 shows a typical LC-tuned VCO- the circuit of choice for high frequency application requiring low phase noise. An LC-tank is used as an on chip resonator enabling a highly integrated design for the RF frequency band. The negative resistance is provided by the cross-coupled transistor pair. The negative resistance concept illustrates a source of energy that will be used to counteract the losses in the resonating tank. The negative resistance is modeled by the oscillators effective transconductance $G_{M,eff}$.

3.1.6.2 Inductor Design

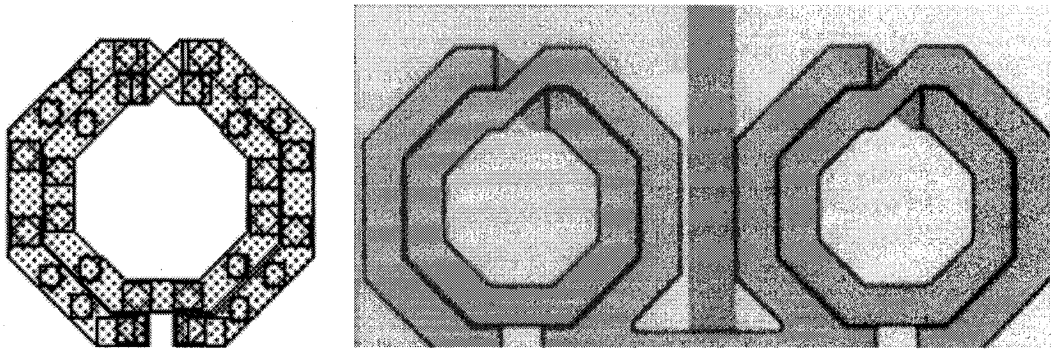

Figure 3.22 a) Inductor design using Cadence layout tools, b) fabricated inductors in CMOS 0.18µm

Integrated inductors are known to have poor quality factors (i.e. 4-5) and will be the limiting factor in the tank overall quality factor. Figure 3.22 a) and b) illustrate the high level of symmetry required in inductor design. To optimize the inductor for high Q, only top metal layers were used to minimize the parasitic substrate capacitances, effectively reducing substrate loss and coupling. Also, the top two metal layers were used to reduce the series resistances of the inductors. They were connected through massive amounts of contacts that were placed around the inductor loops in a symmetrical fashion. The inductor modeling software called ASITIC, developed by Berkeley University, was used to design the inductor dimensions for a specific frequency of operation. Figure 3.22 b) are the resulting fabricated inductors used in the VCO.

3.1.6.3 The LC Tank Resonator

In an LC-tuned VCO, the overall tank quality factor can be approximated by the inductor quality factor. Because the quality factors of the transistors and varactors is higher than that of the inductors, their effect is counteract by the poor inductor quality factor. The tank is composed mainly of the inductors, the drain and gate capacitances of the cross-coupled transistors, and the capacitive loading of the varactors.

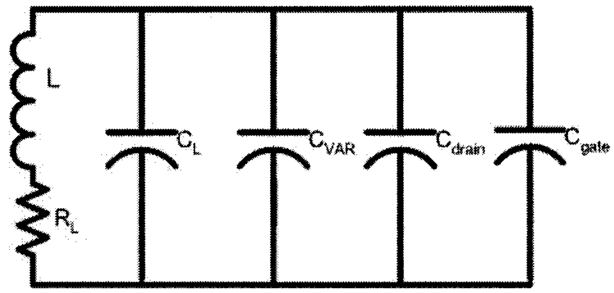

Figure 3.23 Typical resonant tank components for the circuit in Figure 3.21

Figure 3.23 illustrates the resonant tank components for each tank (i.e. inductor) of the VCO circuit presented in Figure 3.21. The following equations are used to design the center frequency [40]:

$$\omega_0 = \frac{1}{\sqrt{L \cdot C_{\tan k}}} \qquad \text{Eq. 3.12}$$

where the tank capacitance is obtained with the following equation:

$$C_{\text{tank}} = C_L + C_{\text{var}} + C_{drain} + C_{gate} \qquad \text{Eq. 3.13}$$

Where C_L is the capacitance due to the inductor, C_{var} is due to the varactors, C_{gate} and C_{drain} are due to the cross coupled transistors gates and drains, respectively. These capacitances are designed so that they enable a wide tuning range. C_{gate} and C_{drain} will vary with I_{bias} and must be designed to enable the complete WLAN range of frequency. The amplitude of the VCO output is described by the following equation [40]:

$$V_{VCO} = Z_{\tan k} \cdot I_{bias} \qquad \text{Eq. 3.14}$$

where I_{bias} is the current biasing provided by the current source at the bottom of the circuit in the VCO figure. Z_{tank} is the equivalent impedance of the tank seen at the output node. This combination of factors must be designed so that the amplitude satisfies the output power requirements over the entire WLAN range of frequencies. The tank impedance is proportional to L. A larger L could be used, enabling smaller current biasing to meet the amplitude requirements.

3.1.6.4 The Cross-Coupled Amplifier

The cross-coupled amplifier is designed so that it counteracts the losses encountered by the tank through its parasitic resistances. The design of the resonant tank is specific to a relatively narrow band of frequencies. This enables us to make the assumption that the losses can be modeled by a single resistance. Due to the poor quality of the inductor, its series resistance can be used as the single source of losses. The inductor series resistance can be transformed into a parallel tank impedance by the following relationship [45]:

$$R_{||} \approx Q_{\tan k}^2 \cdot R_L \approx Q_L^2 \cdot R_L \qquad \text{Eq. 3.15}$$

Using the resulting $R_{||}$ the cross-coupled amplifier can be designed to counteract the losses introduced by $R_{||}$. The cross-coupled transistors are the equivalent of a negative resistance (i.e. $-R=2/g_{m12}$). The following relationship must be satisfied to ensure stable oscillation [40]:

$$G_m \geq \frac{2}{Q_L^2 \cdot R_L} = \frac{2 \cdot R_L}{(\omega_0 \cdot L)^2} \qquad \text{Eq. 3.16}$$

where

$$G_m = g_{m12} \qquad \text{Eq. 3.17}$$

To ensure oscillation start-up, a safety factor of 2 was used in the design of the estimated transistor transconductance. This should ensure oscillation start-up. In the case of a wide tuning range VCO, once a specific G_m is selected, the safety factor will increase with frequency as can be seen from Eq. 2.2 and Eq. 3.16. This will also cause the phase noise to increase with frequency, illustrating a trade-off between wide tuning range and phase noise.

3.1.6.5 Varactor Tuning

The varactor concept is to have a tunable capacitive device. Many types of devices are used in integrated circuits, micro-electromechanical structures (MEMS) varicaps [46], digitally switched capacitor banks and semiconductor capacitive junction devices. The MEMS is basically a micro version of a parallel plate capacitor, where the overlap area and/or the distance between the two plates can be varied. The MEMS minimum dimensions can be in the order of a few tens of microns. They can have very high quality factors, they are linear and can have wide tuning ranges. On the other hand they are very costly to implement and integrate with standard processes. The digitally switched bank of capacitors does not provide continuous tuning. To integrate it in a PLL system would require an analog to digital converter, and a very large number of capacitive cells. This is prohibitive in terms of silicon area and design complexity. Also, this would create discrete jumps in the PLL output, generating spurs in the frequency spectrum. The semiconductor devices make use of the device junction capacitances. They have reasonably high quality factors and are fully integrated, but compared with the MEM alternative, their tuning range suffers from a non-linear behavior, and from a rather smaller linear tuning range.

3.1.6.5.1 Inversion Mode PMOS Varactors

The CMOS technology offers many variable capacitance possibilities, such as the gate capacitance of NMOS over N-well devices, drain/source diffusions with N-well type PMOS transistor technology, and PN junction diodes [47]. A PMOS inversion mode varactor is used in this implementation. These types of varactors are controlled by the body-gate voltage. The intent is to enable differential control, rendering the design immune to noise. Also PMOS varactors are the only ones that can easily be simulated with the tools we had access to; they also offer better tuning ranges than the PN junction diodes. Cadence extracted layout and Hspice were used to determine the inversion mode PMOS varactor sizing that would enable the required tuning range.

In this design, PMOS type varactors where used to implement a fully differential VCO. Two banks of PMOS varactors were used. Both have opposite capacitance vs. voltage curves, which enables a fully differential control of the oscillator. Again this produces a VCO that is relatively immune to noise. Also, since this implementation is on a P-substrate technology, the PMOS varactors are protected from substrate noise coupling by the N-well isolation.

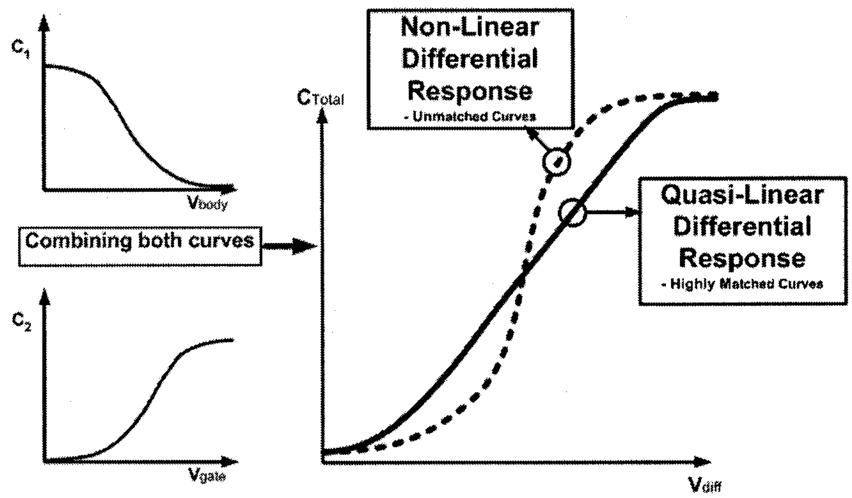

Figure 3.24 Differential varactor control

Figure 3.24 illustrates how a well matched set of C-V curves can generate a highly linear varactor control. Any mismatches will result in reduction of noise rejection. Mismatch may occur due to the limitation introduced by process variations and available biasing voltage. Even badly matched curves would still reject some level of noise. Any level of mismatch can be tolerated as long as the PLL can operate properly with the resulting VCO gain. In this case of PLL prototyping, having an external loop filter enables loop design to overcome any unexpected VCO gain, and still implement a successful PLL design.

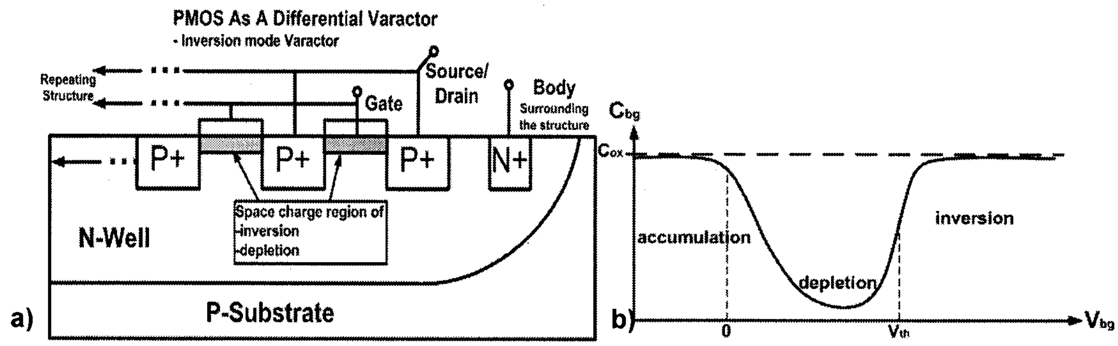

Figure 3.25 a) PMOS inversion mode varactor, b) PMOS capacitance regions versus V_{bg} tuning [45]

Figure 3.25 a) shows the layout of the PMOS inversion mode varactor. Figure 3.25 b) illustrates the different theoretical regions of operation of this type of varactors. To enable differential VCO control, the PMOS varactor needs to be used as a three terminal device. The source/drain terminal is connected at the oscillating node. The goal is to have two varactors, one controlled at the gate and the other at the body. Both varactors follow the inversion curve, one from C_{min} to C_{max} and the other in the opposite direction. The two varactors structure should enable a fully differential control. The remaining terminal is used to set the varactor in the inversion region of operation, by biasing either the gate at ground or the body at 1.8V. The ultimate goal is to have the two opposite behaviors available in the center of the inversion curve, enabling the largest capacitive variation, while having highly matched slopes. If both slopes are not centered at the capacitive mid-point, an offset will be introduced and slope mismatch will occur, reducing noise rejection. The worst case scenario is when the two behaviors will not overlap and differential control is impossible.

Unfortunately accurate varactor behavior is hard to predict since they are very sensitive to layout, voltage biasing, and doping profiles. Moreover, they are usually not part of standard libraries. In the case of layout, it is rather difficult to accurately predict the effect of a specific layout technique when it is used in a new configuration. In this design the voltage biasing is 1.8V, limiting the possible operating regions of the varactor. For the doping profile, since doping profiles vary from one CMOS process to the other, it is naive to rely too much on results obtained in previous publications. It is wise to have a second plan to fall back on if things go wrong. This is another reason why the loop filter was implemented off-chip to safeguard the success of the overall project.

The inductor is usually the limiting element for the Q-factor. For on-chip inductors, the typical values reach *5*. It is very important to make sure that the varactor does not degrade the resonator tank's Q-factor. In our case, the structure is repetitive in nature. It is a bank of individual varactors sharing the same controls and outputs. This method reduces losses due to the interconnection. Also, minimum channel lengths were used to reduce the parasitic series resistances of the varactors. This will effectively increase the quality factor of the varactor. It must be noted, that to ensure high varactor quality factor, the voltage across the PN junction must remain reverse-biased. This will prevent forward bias current leakage to degrade the overall tank quality factor.

3.1.6.6 VCO Coarse Tuning

To enable coverage of the 5 GHz to 6 GHz band, the use of extra coarse tuning was required. Since the varactor linear tuning mechanism is very limited, a more robust and controllable tuning method was required. The coarse tuning of the VCO is provided by external biasing of its current drive. It is well known that by varying the current through the VCO, its nodal voltage biasing will change. As in the case of varactors, the nodal effective capacitance appearing at the oscillating node will also change.

The current tuning needs to be designed with great care. The VCO oscillation must be sustained while its current drive is reduced. Also, as the current drive is increased, the output voltage swing should always remains above the minimum required swing to drive the mixers. The transistor feedback circuit will experience large V_{ds} values for large currents, naturally limiting the VCO's output voltage swing.

3.1.7 Quadrature VCO's

The choice of designing a quadrature VCO enables this PLL to be used with key architectures. Having a four phase output is the main element that distinguishes it from the simple differential VCO. It can be used in Weaver image rejection architectures, and in I-Q modulation architectures [36]. The architecture of the VCO was based on that reported by Lee et al. [49].

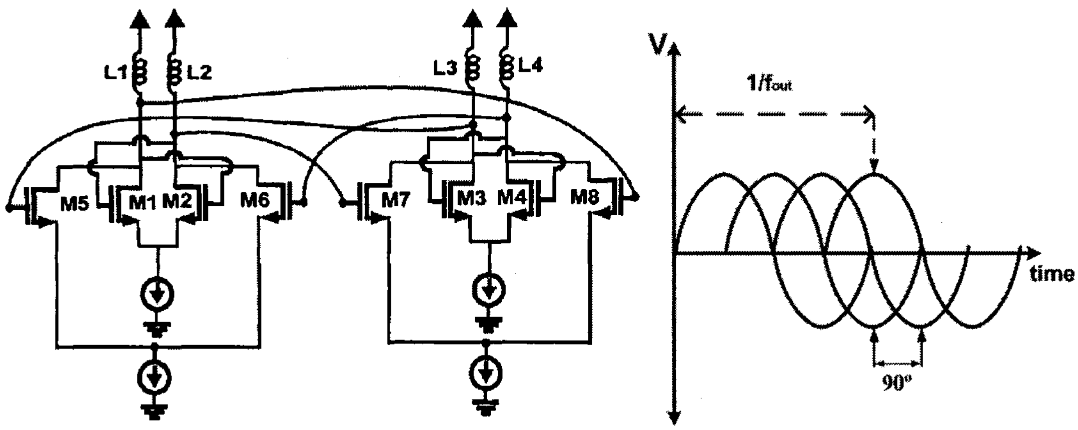

Figure 3.26 Quadrature VCO circuit and its four output phases

Figure 3.26 presents the quadrature VCO used in this PLL implementation. The phases are coupled from one cross-coupled VCO cell to the other. The VCO cells were designed using the method presented earlier. This coupling technique, using M5-8, ensures that the four phases will be exactly *90°* out of phase from each other. To tune the VCO, banks of varactors are added to each oscillating node. Each bank is composed of two varactor sub-banks, both having opposite voltage/capacitance relationships, enabling differential control of the quadrature VCO.

3.2 References

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Chapter 4 Testing, Measurements and Results

4.1 Introduction

This chapter is divided into five sections: the introduction, the chip layout micrograph description, the test setup, the synthesizer measurements and results, and the frequency divider power consumption results compared with recent publications.

4.2 Chip Micrograph of the Synthesizer

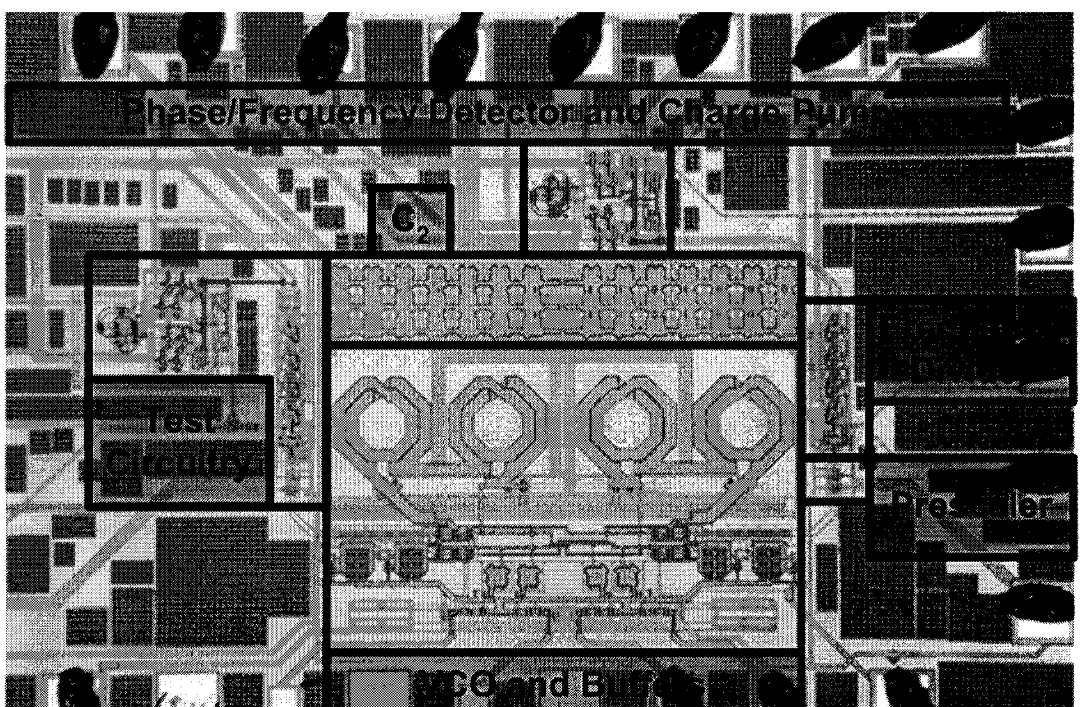

Figure 4.1 Chip micrograph of the synthesizer

Figure 4.1 shows the frequency synthesizer. The quadrature VCO with its four inductors is located in the center of the figure. Note that the VCO layout is kept as symmetric as possible. Also seen are the prescaler, frequency divider, phase frequency detector, charge pump, test circuitry, and part of the loop filter. The prescaler layout was explicitly designed for the smallest possible area. The area of each divided-by-two element is 7.1 x 10.6 μm^2, and the overall design is 750 x 850 μm^2.

4.3 Testing and Test Setup

In this work, a printed circuit board (PCB) was manufactured using 2 layers with standard FR4 material. Orcad layout tools were used to generate the PCB files required for fabrication. The design of the PCB was done carefully: the main guideline in PCB design is to keep the RF lines short and matched at 50Ω. Differential outputs are laid out symmetrically with ground shielding. The DC supply lines can be designed with more flexibility. Capacitor ground coupling were widely used to remove noise on the DC supply lines.

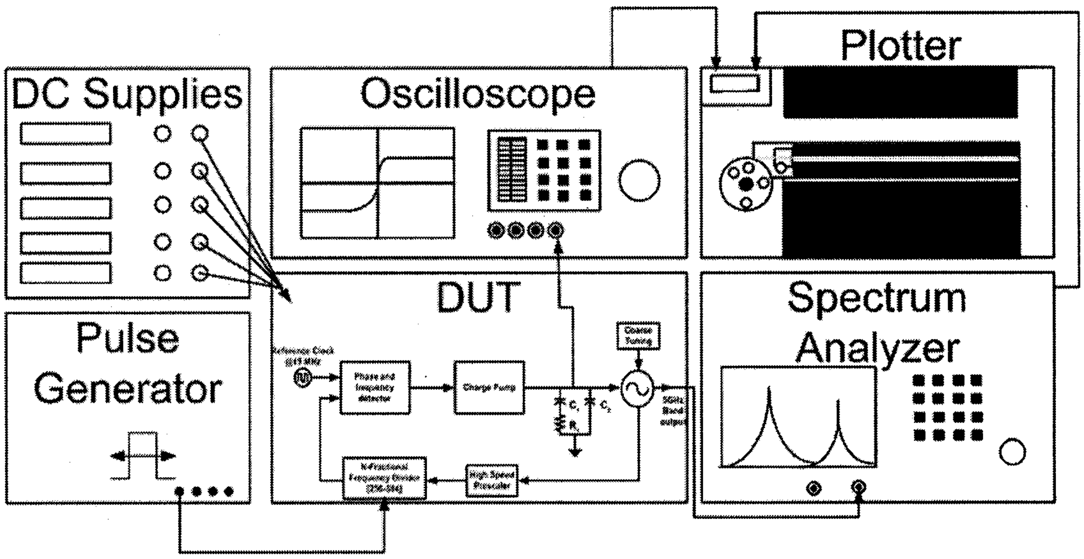

Figure 4.2: Test setup

Figure 4.2 shows the complete set of instruments that were used to measure the frequency synthesizer's behavior and figures of merit. The main input sources are the DC supplies which provide all necessary voltage biasing and current supplies. The pulse generator is connected to the control of the fractional-N divider, and it also generates the reference signal. The equipment used to make the measurements are an oscilloscope and a spectrum analyzer. Two different spectrum analyzers were used: the HP 8593E and the power spectrum analyzer (PSA) Agilent E4446. The PSA is the latest state-of-the-art spectrum analyzer which includes a phase noise personality. The PSA is a less noisy system than the 8593E. The two systems were used to obtain the synthesizer figures of merit.

4.3.1 Noise in Testing

To reduce the presence of noise in the measurements, all possible noise sources must be eliminated. It goes without saying that absolute noise removal is impossible, but high levels of noise reduction can be obtained by proper test set up.

One of the noise and EMI-immunity measures is to perform all measurements in a Faraday cage. A Faraday cage will isolate the device under test (DUT) from any external sources of noise and interference. The noise floor for a specific measurement went from around -65 dBm to -75 dBm when measured outside and inside a cage, respectively. The 10 dB improvement in noise floor is rather large.

The transistor level implementation of the synthesizer has many circuit structures that are similar in behavior to frequency multiplier cells. This is the case of the VCO, prescaler, divider, and charge pump circuits. These cells are known to be used in frequency conversions. Low frequency noise can be up converted close to the carrier. An example of this frequency conversion is that noise at baseband can modulate the VCO control. Noise can also be up-converted by an internal node of the VCO to its frequency of oscillation. These unwanted effects effectively increase the necessity for the testing setup to be as noiseless as possible. Many precautions must be taken in order to reduce signal corruption.

Since testing takes place in a Faraday cage, the noise is mostly introduced by the test equipment themselves. These instruments became the main sources of noise and interference. The DC supplies must be coupled to ground by a parallel combination of small and very large capacitors. These will remove most of the DC supply generated noise. The small surface mount capacitors used in this configuration reduce the effective inductance, allowing high-frequency current pulling and pushing. Very high precision DC supplies may introduce noise levels up to 2 mV in amplitude. The supplies used in this work were not of such high quality, and thus introduced relatively larger noise amplitudes in the range of 10 to

40 mV. Two other noise sources existed: the divider control and the reference signal. The high frequency noise signals embedded within these signals were filtered out using small grounded capacitors. Obviously, some level of noise will still be introduced in order not to damp or filter out the two signals of interest. The final source of noise is the measurement equipment. It usually introduced limited and expected amounts of noise. Also, some quantization effects and distortion may be introduced. Ideally, the DUT should be put in a grounded casing in order to provide further shielding. When measuring with high accuracy, placing the different measurement equipment on separate power outlets is recommended.

4.4 Synthesizer Measurements and Results

4.4.1 VCO Fine-Tuning

The frequency fine-tuning is provided by the CPPLL feedback mechanism and by an inversion-mode PMOS varactor. The goal was to create a fully differential CPPLL system. The method used was presented in Chapter 3. Each end of the body-gate junction voltages can be controlled. This will generate an opposite tuning behaviour. Both varactors follow the inversion curve, one from C_{min} to C_{max} and the other in the opposite direction.

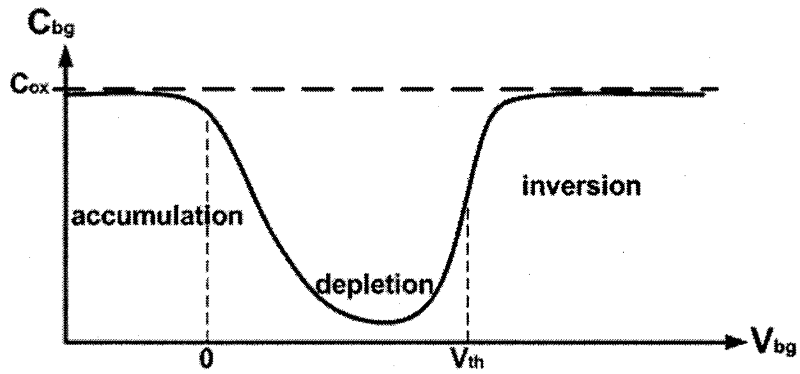

Figure 4.3 Theoretical PMOS varactor behaviour [45]

Figure 4.3 shows the theoretical capacitive behaviour of a PMOS varactor [50]. This can be used to predict the behaviour with different biasing and control methods. It was used in the design of the differential PMOS varactor control implemented in this work.

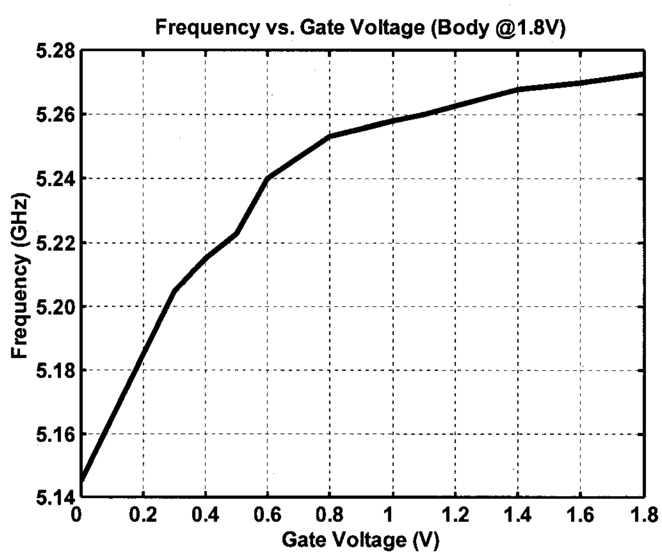

Figure 4.4 VCO frequency versus tuning the gate voltage of the varactor

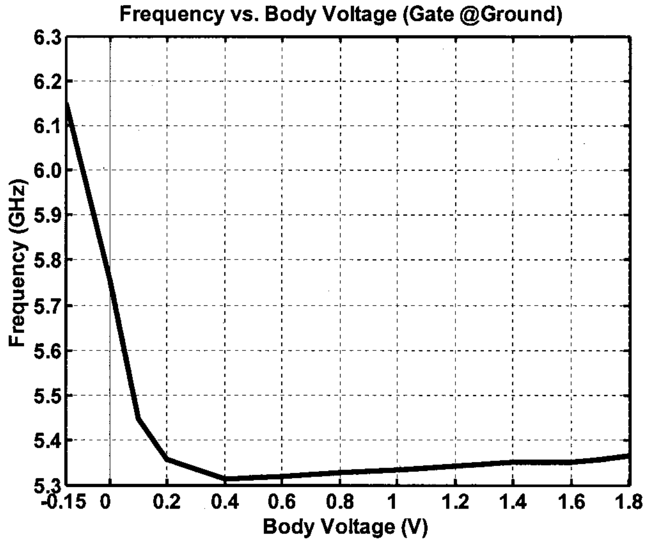

Figure 4.5 VCO frequency versus tuning the body voltage of the varactor

Figure 4.4 illustrates the tuning behaviour of the gate-controlled varactor. Its tuning range is limited by the available voltage biasing (0-1.8V) which corresponds to the bottom of the inversion curve, in the transition region between weak inversion and depletion. In fact, this section of the curve has a relatively small slope, limiting the tuning range of the VCO to a maximum of 128MHz. Figure 4.5 demonstrates the opposite tuning behaviour, corresponding to the top of the inversion curve and the strong inversion region, before reaching the maximum value of capacitance available. The slight increase in frequency, from 0.4 V to 1.8 V, is due to the reverse biased PN junction capacitance being reduced as the body-source/drain voltage difference is increased. The inversion behaviour is limited to the -0.15 V to 0.40 V range. Because biasing is limited to a voltage value between 0 V and 1.8 V, the available tunable frequency range is ~390 MHz out of a possible maximum range of 840 MHz. The combination of the two methods of varactor tuning reaches a total of 965 MHz. This is an impressive result compared to a simple inversion mode PMOS varactor.

Unfortunately, the two curves cannot be shifted to overlap significantly, and the CP output voltage is limited by a minimum of ~0.3 V. This, in fact, makes it impossible to use the VCO in a fully differential mode for the entire tuning range, which also implies that the CPPLL will not be fully differential over that range. This reduces the VCO gain, the output CP current, and the noise immunity of the overall system. The VCO tuning range is reduced to only 128 MHz, which is still more than enough to meet the standard specifications. After all, the loop filter's initial design can be reviewed to compensate for the losses in the VCO gain and in the charge pump current. The average VCO power consumption was 40mW at mid-band (5.5 GHz), which is not bad considering it required a large variation in G_m to operate over the entire 5 to 6 GHz band.

4.4.2 Synthesizer Coarse Tuning

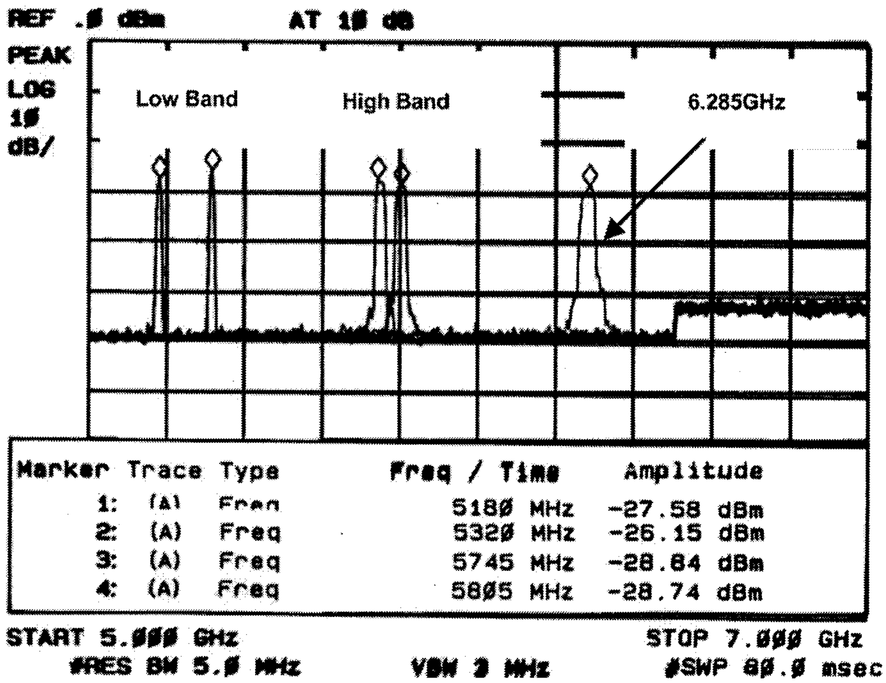

Figure 4.6 Coarse tuning enables wide synthesizer capture range

Figure 4.6 illustrates the wide frequency range enabled by the VCO current tuning method discussed in Chapter 2. The two leftmost tones are the two channels at the lower/upper edges of the lower unlicensed WLAN frequency band, and the two tones in the middle delimitate the upper unlicensed WLAN frequency band. The rightmost tone, at 6.285 GHz, demonstrates the upper limit of the VCO tuning range. It can also be seen that the output power remains relatively constant across the bandwidth of interest, enabling a 1.2 GHz capture range. When pushing the frequency above 6.3 GHz, the output power decreases rapidly. Similarly, when the current is reduced beyond a certain threshold, suitable output power cannot be sustained below 5.1 GHz. Since the VCO cannot be operated without the CPPLL being turned on, no free running VCO phase noise measurements were possible.

4.4.3 Phase Noise Measurements

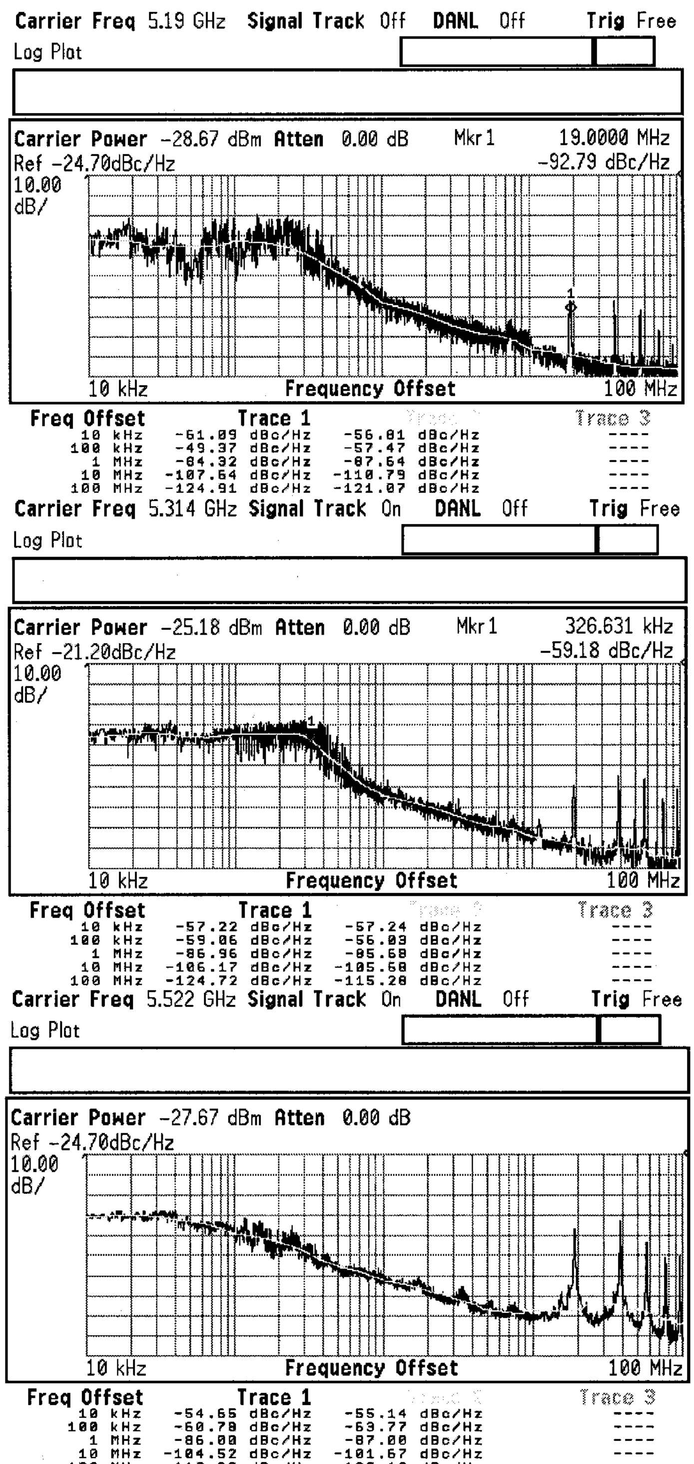

Figure 4.7 Phase Noise @5.19GHz, @5.314GHz, and @5.522GHz

Figure 4.7 illustrates the phase noise degradation over an increase in frequency for a phase noise measurement at a 10 MHz offset. Results show an increase of ~3 dB in phase noise from 5.19 GHz to 5.52 GHz. Leesson's equation shows that VCO phase noise increases with frequency [25]-[27], which explains the observed degradation in phase noise. The offset frequency of 10 MHz was chosen since it falls at the edge of the adjacent channel and because, at this offset, the effect of variation in the loop behavior is negligible. This is one of the main figures of merit often reported in the literature for 5 GHz WLAN applications. Furthermore, measurements taken in the 5.725 GHz to 5.825 GHz band, not shown for conciseness, revealed a phase noise of -94 dBc/Hz@10 MHz. Also, from Figure 4.7, it can be observed that the -3 dB integrator noise plateau reaches frequencies in the order of a few hundreds of kHz. It is clear that the integrator phase noise is not optimized for measurements @5.19 GHz and @5.314 GHz and that the loop bandwidth is too large. The phase noise measurement @5.522 GHz clearly illustrates the optimized case with a loop bandwidth of ~65 kHz. This discrepancy is caused by a non linear VCO gain and can be corrected as shown @5.522 GHz by proper use of coarse tuning, enabling the required VCO gain for optimal noise shaping.

The loop behaviour varies with the operating frequency due to the loop division factor and the VCO gain. It is therefore only normal for the loop bandwidth to be different for each synthesized frequency. From the phase noise measurements, it can be observed that the integrator phase noise power remains relatively constant for all measurements. At a 10 MHz offset, the effect of the noise shaping diminishes, and we are left with the VCO's unshaped phase noise. This demonstrates that the noise shaping is well optimized to maximize the VCO's close-in phase noise removal. The measurements illustrate that the system has an optimal response at 5.522 GHz with regard to the noise shaping of the VCO phase noise. It is very difficult to optimize for such a wide range of synthesized frequencies, when taking into account the non-linear VCO tuning behaviour. The results shown demonstrate a well optimized synthesizer for multiple frequencies. Note that the spurious tones appearing at 19 MHz and its integer multiples are below the integrator phase noise level. Therefore, these tones will not affect the throughput of non-overlapping spectrums in WLAN's.

4.4.4 Loop Filter Behaviour

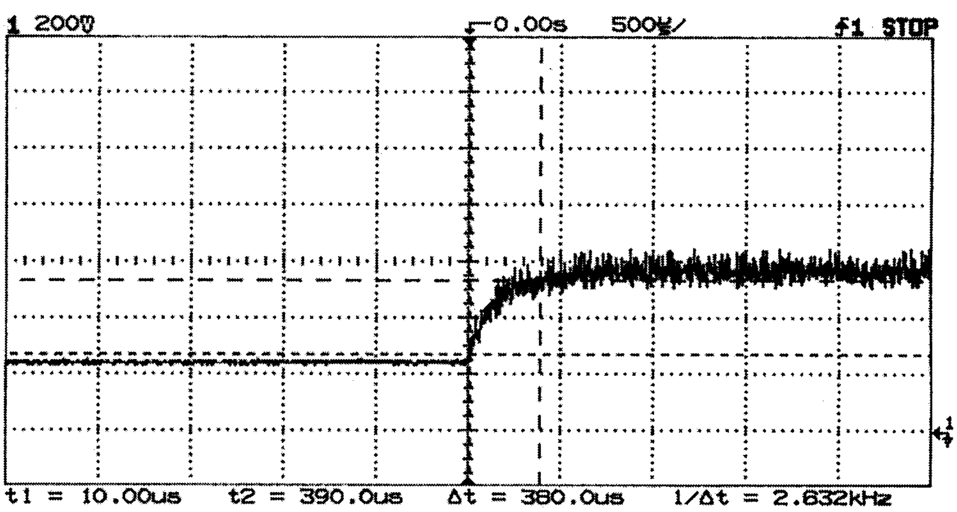

Figure 4.8 VCO control transient response of CPPLL to a step in frequency

Figure 4.8 illustrates the CPPLL response of the control input of the VCO, to a step in frequency. From the absence of overshoot and the steepness of the slope, it is clear that the system was optimized for a damping factor of $\zeta \approx 1$. The measured settling time is ~400μs. This response is different for different frequencies. The captured transient response of the VCO input shown in Figure 4.8 was obtained by loading the CPPLL with an oscilloscope, effectively slightly over-damping the loop behaviour and slowing down the CPPLL response. However, even with this undesired loading, the behaviour was satisfactory, closely approaching the optimized critically damped response.

f_0	Kvco	Icp	Cp	C_{HF}	R	N	ω_n	ζ
5.282 GHz	125 MHz/V	550 μA	180 pF	28 pF	33 kΩ	278	470 krad/s	1

Table 4.1 Summary of the loop behavior

Table 4.1 presents the values corresponding to the transient response of Figure 4.8. The value of the VCO gain is specific to 600 mV biasing region, and the I_{CP} was obtained from simulation. Also included are the loop filter components values and the resulting natural frequency (e.g. ~75kHz) obtained by following the second-order theoretical modeling. The other values correspond to the settings of the transient response presented in Figure 4.8. Since the CPPLL cannot be used fully differentially, the effective VCO gain is reduced. The I_{CP} value refers to the single ended CP current output. By designing for an optimized response with a damping factor of ζ=1, the undesired ripples due to an under damped response are avoided. This resulted in an optimized settling time.

In Chapter 2 we discussed the CPPLL behavior as similar to a second order system, with the added charge pump current control over the loop behavior. Using the values obtained from measurements and Hspice simulations presented in Table 4.1, comparison with theory can be made. When comparing the approximated natural frequency value obtained earlier (~65 kHz) with the theoretical second-order model (~75 kHz), it is clear that they are matched within a few kHz. These results confirm that the methodology used in the comparison is appropriate.

The CPPLL was optimized for low power and low noise. The low CP currents and loop bandwidth are results of this optimization. Obviously, the use of less current will result in more time to charge and discharge the capacitive load, slowing down the response of the CPPLL. Some discrepancies between the simulated and measured settling time can be explained by the limitations of the model used in the analysis. The actual synthesizer implementation is a third-order loop design, while the approximations are based on a second-order model. The simpler second-order model starts to deviate from the actual behavior when the difference in the size of the two CP load capacitors is small. In this work, the parallel capacitor is nearly eight times smaller than the main capacitance load, which permits the safe use of second-order modeling. The added loading due to the parallel capacitor will effectively slow down the response, while not degrading it too much. The advantage of working just before the breakdown region of the second order model is to obtain a large reduction in noise, while retaining a simple and efficient design methodology. Also, to accurately compare the initial modeling and the measured results, all the elements of the modeling equation must be precisely measured. In this work, the current output of the CP is difficult to obtain, and the actual capacitive load of the CP can only be roughly estimated since several parasitic capacitances are added through the interconnects, and not accounted for by the model. The use of an external loop filter introduces many parasitics, but it provided much needed flexibility in testing.

4.4.5 Fractional Spurs

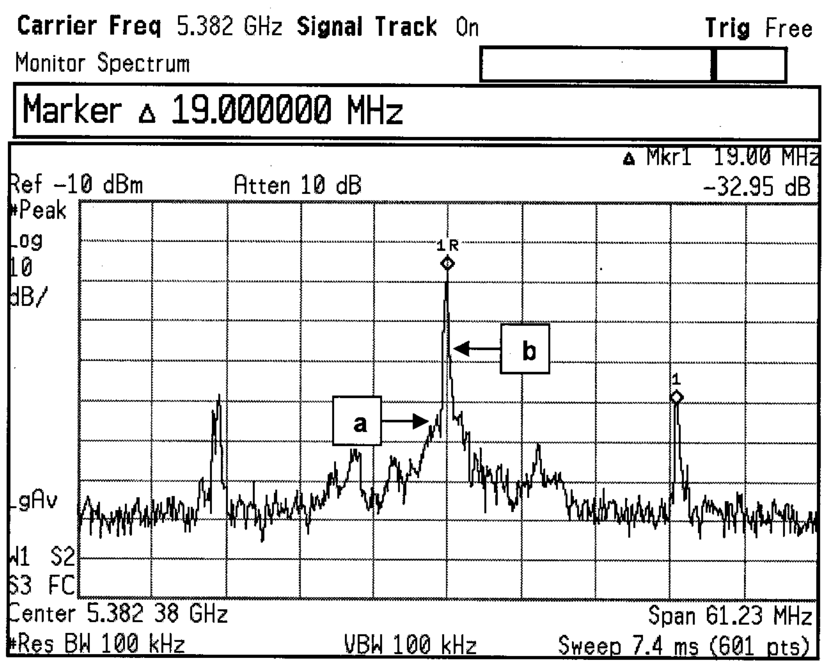

Figure 4.9 Spurious tones of fractional-N synthesis

Figure 4.9 illustrates the spurious tone rejection. At 5.382 GHz the rejection obtained is -32.95 dBc. Figure 4.7 shows a fractional spurs rejection at 5.19 GHz of -92.79 dBc/Hz. All measurements taken using the phase noise personality of the PSA were optimized by internal routines proprietary to Agilent. Figure 4.9 also illustrates the distinct shape of PLL noise shaping of the close-in phase noise, where the center tone abruptly changes from a narrow tone to a plateau (see marker **a**). Also, the effects of the conventional PFD with dead zone, as presented in Chapter 3, can be observed (see marker **b**). The center tone exhibits a width typical in shape to PLL's with dead zones. It is clear that further improvements would come from a no dead zone PFD implementation.

4.4.6 Frequency Resolution

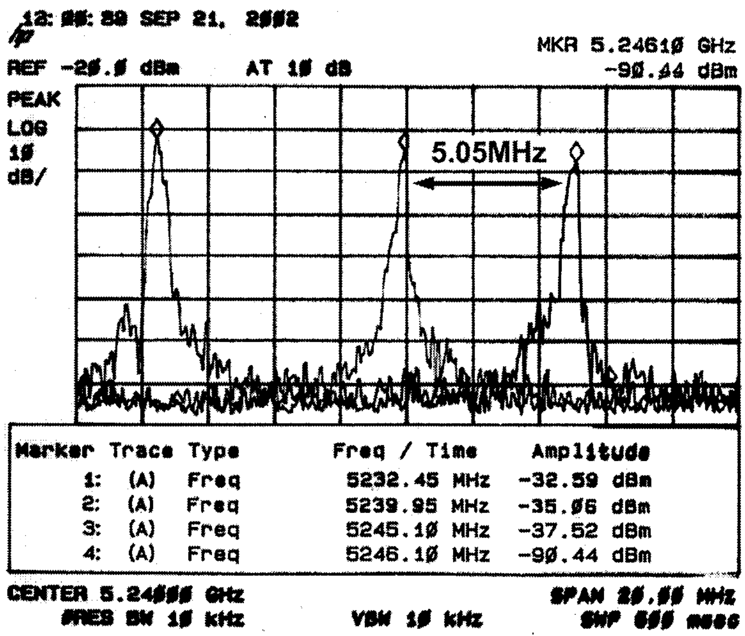

Figure 4.10 CPPLL frequency resolution @ 5.24 GHz of 5.05 MHz, and phase noise of -92 dBc/Hz @ 1 MHz offset.

Figure 4.10 displays three tones at 5232.45 MHz, 5239.95 MHz, and 5245.10 MHz. This demonstrates a frequency resolution as precise as 5.05 MHz. The fourth marker shows a power level of -90.44 dBm at an offset frequency of 1 MHz from 5245.1 MHz, which corresponds to a -92 dBc/Hz phase noise. These measurements were taken with the HP 8593E and show how important it is to perform measurements using the latest state-of-the-art equipment. This version of spectrum analyzer is no longer supported by HP! The measurements were very noisy, and obtained with a very old pencil plotter, but they do show the resolution of the CPPLL properly. With the 1.2 GHz capture range and a maximum resolution of 5.05MHz, hundreds of channels can be enabled. By interpolation, a maximum of roughly 237 channels are possible.

4.4.7 Comparison to Other Published Synthesizers

	Unlicensed Frequency Bands (GHz)	Tech. (μm)	Freq. Res. (MHz)	**V_{DD} (V)**	Phase Noise dBc/Hz
This Work	**5.15-5.35**	**0.18**	**5.05**	**1.8**	**-107@10MHz**
This Work	**5.725-5.825**	**0.18**	**5.05**	**1.8**	**-94@10MHz**
[17]	**5.14-5.70**	**0.25**	**20**	**2.5**	**-116@1MHz**
[51]	**5.2**	**0.4**	**-**	**2.6**	**-100@10MHz**
[52]	**5.5**	**0.25**	**-**	**1.5**	**-88@40kHz**
[53]	**4.840-4.994**	**0.24**	**22**	**2.0**	**-101@1MHz**

Table 4.2 Comparison to other published synthesizer

Table 4.2 presents some of the latest work reported on CMOS synthesizers, operating in the 5 GHz range. Clearly, the work in this thesis compares well with state-of-the-art designs in terms of phase noise, the diversity of the operating frequency bands, and the frequency resolution.

4.5 Power Consumption of the Divider

This section presents the low power consumption results achieved using the techniques presented in Chapter 3. A comparison is made to different state-of-the-art CMOS implementations operating in the multi-GHz range.

	÷	Tech. (µm)	$f_{in, max}$ (GHz)	Vdd (V)	P_d (mW)	SENS[1]. (V_{PK})
This Work	**256-384**	**0.18**	**7.0**	**1.8**	**4.5**	**0.6**
[17][2]	**512-576**	**0.25**	**5.7**	**2.5**	**6.25**	**-**
[54]	**220-224**	**0.25**	**5.5**	**2.2**	**59**	**0.3**
[55]	**8-9**	**0.7**	**1.5**	**5.0**	**55**	**0.16**
[56]	**4**	**0.15**	**11.8**	**2.0**	**20**	**1.0**
[57]	**16**	**1.2**	**1.5**	**5.0**	**13**	**0.35**
[58]	**4-5**	**0.4**	**4.2**	**3.5**	**-**	**0.5**
[59]	**128**	**0.7**	**1.7**	**3.0**	**24**	**-**
[60]	**2**	**0.1**	**13.4**	**2.6**	**26**	**1.3**

Table 4.3 Comparison to other published CMOS dividers

Table 4.3 summarizes a comparison between the divider realized in this work and recently reported dividers. Furthermore, it illustrates how well the

[1]The value V_{PK} is the minimum peak signal voltage required for the divider to function properly.
[2] This work presents a single ended divider design (i.e. less transistors).

prescaler and divider designs were successful in producing one of the best low power CMOS divider ever reported. This work shows a divider dynamic power consumption of 4.5 mW, obtained from measured results. This summary demonstrates the feasibility of operating dividers from a lower voltage supply, and achieving low power consumption at high frequencies in standard CMOS processes. Also, the dynamic power consumption of the PFD/CP combination of only 2.7 mW compares well with reported values [51]-[53].

4.6 References

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Chapter 5 Conclusion

The world market of consumer electronics is orienting itself toward wireless devices. One of the most thriving markets is that of cellular phones. We are seeing more and more multiple-band cellular phones. These operate across different cellular networks and also are able to carry data as wireless modems. This, and the ever growing popularity of WLAN, are today's driving forces in RF microelectronics research. To enable WLAN to be integrated into cellular phones, the technology must be optimized for low voltage, low power design, and the WLAN applications, which means that the front-end frequency of operation will be pushed toward the gigahertz range. It was demonstrated that CMOS is capable of meeting these requirements. Also, CMOS offers the added value of increasing the level of integration, thus further reducing the cost of each device.

This work presented a CMOS fractional-N charge pump synthesizer for the 5GHz WLAN application. This standard offers the largest throughput available for data transfer. In Chapter 1, an overview of the synthesizers is presented with an emphasis on presenting CMOS as a real contender in RF microelectronics.

In Chapter 2, a brief theoretical explanation of the basic design concepts of PLLs is introduced. The problem of noise in PLL is discussed by thoroughly inspecting the sources of noise in microelectronics and how they are present in a

PLL system. Simple mathematical noise modeling is introduced with other methods of modeling the behaviour of a PLL, showing how to design for targeted specifications.

In Chapter 3, the CPPLL building blocks implementations are presented. Each block design is discussed from its high level design down to the transistor level implementation. The importance of low power and high frequency layout techniques are stressed. A set of rules to follow are introduced to ensure the success of any high frequency and low power circuit implementation.

In Chapter 4, the measured results of the CPPLL implementation are presented. Also, a comparison with state-of-the art synthesizer design is shown. An emphasis on the success of the low power design methodology is presented by comparing this work with recently published frequency dividers, as they are one of the most power consuming circuitry of typical PLL implementations.

5.1 Overall System Performance

Table 5.1 summarize the performance of the CMOS CPPLL implementation of this work. Its low power components and its wide frequency range of operation are the key points of this work. Also, the low phase noise measurement in the adjacent channel demonstrates how little noise the system will leak into the other channels. The results presented show how well the design fits within the requirements of today's low power and high frequency WLAN applications. This fulfills the goal of this work by demonstrating that the RF CMOS technology is a real contender for WLAN front-end design.

Parameter	Value
Reference Frequency	19MHz
Capture Range	5.1 to 6.3GHz
Power Supply	1.8V
Max. Number of Channels	237
Settling Time	~400μs
Phase Noise @ 5.15 to 5.35 GHz	-107dBc/Hz @10MHz
Phase Noise @ 5.725 to 5.825 GHz	-94dBc/Hz @10MHz
Dual Modulus Divider • Max. Freq. • Min. Control Pulse • Freq. Resolution	 800MHz 1.3ns 5.05MHz
Prescaler Max. Freq.	7.0GHz
VCO Power	40mW
Low Power Circuitry	
Prescaler + Divider	4.5mW
Charge Pump+PFD	2.7mW

Table 5.1 Summary of measured synthesizer performance

5.2 Topics for Future Research

This thesis has demonstrated that CMOS is capable of implementing synthesizers operating in the gigahertz range. The literature has shown that up to 50GHz operating frequencies are possible for specific building blocks (e.g. the VCO). Also, it was demonstrated that very low voltage operation is possible (<1V). The importance of this work is in providing the stepping stone for more in-depth research of CMOS multi-giga-Hertz RF synthesizers.

5.2.1 OC-192 SONET Receiver

The OC-192 SONET standard operates in the 10GHz range. The clock used to sample the data needs to run for specific forward error correcting (FEC) frequencies. A synthesizer operating at these high frequencies would be very challenging to implement in CMOS due to the stringent specifications on low noise and clock jitter. The design of the complete receiver would be both exciting and demanding.

5.2.2 Wide Tuning VCO with Low Noise, Voltage, and Power

A CMOS VCO operating at very low voltage, consuming minimum power and generating an extremely wide range of frequencies is a very interesting field of research. The study of accumulation and gated varactors could be the solution to creating a truly linearly controlled fully differential VCO. Further research on CMOS integrated inductor design could potentially greatly improve VCO phase noise by improving its overall tank quality factor. VCO architectures could be studied to obtain very low voltage implementations.

5.2.3 Synthesizers with an Integrated Controllable Loop Filter

A synthesizer generating a wide range of frequencies needs an adjustable loop filter to maintain the loop behaviour in its optimal mode of operation. Since the divider value varies over a wide range of values, it is hard to keep the mode of operation optimal. This is why wide range frequency synthesizers should be designed with adjustable loop dynamics. By making the loop filter characteristics controllable, any deviations from the initial hypothesis can be corrected online while keeping the loop filter on chip and reducing the overall dimensions of the system.