Design and Implementation of High-Speed Transmitters and Receivers for Optical Interconnects in CMOS Technology

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Abstract

Optoelectronic very-large scale integrated (OE-VLSI) technology provides for the integration of photonic devices, such as the laser-diode and the photodiode, with silicon VLSI electronics. This technology is capable of providing high bandwidth and high-density optical input/output (I/O) to silicon VLSI chips, with an aggregate data bit rate of over a Terabit per second. The development of the vertical-cavity surface-emitting laser (VCSEL) and the high-speed p-i-n photodiode has made this technology possible. Optical transmitter and receiver circuits are responsible for the interfacing between the photonic devices and the silicon VLSI electronics. This thesis presents designs of optical transmitter and receiver circuits implemented in a 0.18 μm CMOS technology. These circuits are designed to achieve minimum power consumption and circuit area, and maximum high-speed performance. Different circuit topologies are studied and implemented. Three different topologies of laser drivers for transmitter and two different preamplifiers for receivers are studied and presented in this thesis.

Sommaire

L'intégration optoélectronique à très grande échelle permet l'incorporation de dispositifs photoniques tels que la diode-laser et la photodiode avec l'électronique. Cette technologie permet donc à une puce de silicium de fournir une largeur de bande appréciable par le biais d'une grande densité d'entrées et de sorties optiques. Le débit de données total peut atteindre l'ordre des térabits par seconde. Le développement de VCSELs et de photodiodes de type p-i-n a contribué à rendre cette technologie possible. Les circuits d'émetteurs et de récepteurs optiques sont responsables de l'interface entre les dispositifs photoniques et l'électronique. Cette thèse présente la conception de quelques émetteurs/récepteurs dans la technologie CMOS 0.18 μm. Ces circuits sont conçus pour minimiser la quantité d'énergie dissipée, minimiser l'espace nécessaire à leur implémentation et enfin, maximiser leur vitesse d'opération. Différentes topologies de circuit sont étudiées et implémentées. En particulier, trois topologies d'émetteurs et deux topologies de récepteurs sont présentées dans cette thèse.

Acknowledgement

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I would like to dedicate this thesis to my parents. I would like to take this opportunity to thank my parents for their supports both financially and mentally, and providing me the golden opportunity of education. I would like to thank them for their endless love and cares.

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Chapter 1: Introduction

1.1 Motivation

The progress in high-performance integrated circuit (IC) technology according to Moore's Law [1], which predicts that the performance of silicon chips increases by a factor of two every eighteen months, has made possible the integration of millions of transistors on a single silicon chip with on-chip clock speeds of multiple gigabits per second. According to the International Technology Roadmap for Semiconductors, 1999 Edition (see Table 1-1) [2], [3], in year 1999, the industry has achieved integration of 24 million transistors per centimeter-square of chip area, with an on-chip local clock speed of 1.25 GHz. According to the roadmap, by the year 2014, chip density is predicted to reach over 2 billion transistors per centimeter-square of chip area, with an on-chip local clock of 13.5 GHz.

Unfortunately, as the performance of transistors continues to improve,

Year of Introduction	1999	2003	2005	2008	2011	2014
Technology node	180 nm	120 nm	100 nm	70 nm	50 nm	35 nm
Density (Mtransistors/cm^2)	24	78	142	350	863	2,130
On-chip local clock (MHz)	1,250	2,490	3,500	6,000	10,000	13,500
Off-chip high-speed pins	700	1,500	*1,900*	*2,300*	*2,700*	*3,000*
Off-chip speed (MHz)	600	862	1,000	*1,250*	*1,500*	*1,800*

Table 1-1: Statistics produced by the International Technology Roadmap for Semiconductor, 1999 Edition [2], [3]. Highlighted region indicates performances that are unachievable by current technology.

conventional electrical interconnect technology has started to hit its limitation. In order to keep up with the improvement in chip performance, interconnect technology needs to be scaled accordingly, as shown in Table 1-1. However, conventional interconnect technology will not be able to meet the requirements for off-chip high-speed pin-count by 2005, and off-chip speed by 2008.

The limitations in the performance of convention electrical interconnect are mostly due to high power consumption, wave reflection, crosstalk, loss at high frequencies, pin-out capacity, and pin inductance. *David A. B. Miller* pointed out that the bit-rate capacity, B, of an LC line is limited by an aspect ratio of

$$B \cong 10^{15} \frac{A}{l^2} \text{ bits/s} \qquad (1.1)$$

where A is the effective cross-section area of the line, and l is the length of the line [4]. In order to overcome the above limitation, a number of researchers have proposed optical interconnect as the replacement to conventional electrical interconnect [4], [5]. The idea is to use optics to provide board-to-board, chip-to-chip, as well as on-chip interconnects. Recent developments in optoelectronic very large-scale integrated (OE-VLSI) technology allows integration of photonic devices such as laser sources and photodetectors onto conventional silicon chips. This supplies multiple optical input and output to a VLSI chip with an aggregate data bit-rate in the order of terabits per second [6].

While optical interconnect presents a bright future for the continued scaling of IC technology according to Moore's Law, the realization of a cost effective optically interconnected system remains a challenge. The challenges of realizing optical interconnects and possible solutions were discussed by *David V. Plant* and *Andrew G. Kirk* in [7].

1.2 Research Contributions

This thesis discusses the research work concentrated on the design of transmitter and receiver circuits for optical interconnects. The purpose of this research is to exploit the capability of state-of-the-art 0.18 μm CMOS technology in the implementation of high-speed optical transmitters and receivers operating in the multiple gigabit range. Even though CMOS could not match the ultra high-speed capability of technologies such as BJT and GaAs, it is so far the most cost-effective technology. Optical transmitter and receiver circuits implemented in CMOS technology can be integrated together with microprocessor and memory on a same chip.

In an effort to maximize speed performance of the optical transmitter and receiver circuits, different circuit topologies were exploited. Two different designs of laser driver circuits were used in the implementation of the optical transmitters. These laser drivers are referred as 1) fast discharge laser driver and 2) push-pull laser driver. In the case of the optical receiver, two different kinds of current mode preamplifiers were used in the design, instead of the conventional transimpedance preamplifier. These current mode preamplifiers are 1) common gate preamplifier and 2) current mirror preamplifier. Current mode preamplifiers have the advantage of smaller input impedance, hence better speed performance.

Besides the circuit design, packaging of the optical transmitter and receiver chips is an important issue to be considered in order to achieve high bit-rate performance. Effects of parasitic on high-speed performance of the circuits due to chip packaging were studied. An optical system was designed to allow testing of the circuits optically.

1.3 Thesis Organization

This thesis consists of five chapters. The first chapter is an introduction chapter that discussed the motivations behind this research. The second chapter discusses circuit designs, detail circuit analysis, and simulation results of the optical transmitter circuits. Chapter 3 presents circuit designs, detail circuit analysis, and simulation results of the optical receiver circuits. In Chapter 4, layouts of the optical transmitter chip and the optical receiver chip are presented. Layout techniques used to reduce power noise and substrate noise, are discussed. Layout strategies are considered to ensure circuit testability. Chip packaging is another topic discussed in Chapter 4. Two packaging methodologies are discussed: wire-bonding and flip-chip bonding. Following that, how packaging is done for the chips is presented. The last section of Chapter 4 discusses how tests and measurements were done and test results are presented. Chapter 5 concludes this research work and possible future work is proposed.

1.4 References

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Chapter 2: Optical Transmitter

2.1. Introduction

The optical transmitter is a key component in the implementation of high-performance optical communication systems. In recent years, it has also found application in chip-to-chip and board-to-board optical interconnect systems. Even though chip-to-chip and board-to-board optical interconnect is still limited to the research phase, it is believed to be a solution to providing high-bandwidth input and/or output (I/O) at low power dissipation to very-large scale integrated (VLSI) circuit.

In the design of an optical transmitter, a reliable light source is critical. There are three kinds of technology available: LED sources, light modulators and laser sources. An 8×8 digital smart pixel array for parallel image processing that uses LED as light sources has been demonstrated [1]. LED sources have the advantage of simpler fabrication and larger tolerance to process variation, but suffer from higher on-chip power dissipation, lower output optical power and lower modulation bandwidth.

Several optical interconnect systems that use light modulators, in particular, multiple-quantum-well (MQW) modulators, have also been demonstrated [2]-[5]. Light modulators are high-impedance, capacitive devices, which consume less on-chip power. However, external lasers will be required. One popular laser source technology is the vertical-cavity surface emitting laser (VCSEL). There have been optical interconnect systems developed based on VCSELs [6]-[8].

A lot of research has been done in the community to develop high-performance optical transmitter circuitry using laser diodes. Several high-speed optical transmitters operating at data bit-rate of over 10Gb/s have been developed using silicon bipolar

technology [9], AlGaAs/GaAs heterostructure bipolar transistors (HBT) [10], InP/InGaAs HBT [11], and AlGaAs/InGaAs high electron mobility transistors (HEMT) [12], for optical communication systems. Although CMOS technology is not capable of providing such ultra-high speed performance, implementation of optical transmitters in CMOS at moderate data bit-rate of over 1Gb/s will be an economical solution to the mass installation of optical communication systems. In addition, optical transmitter circuitries implemented in CMOS can be integrated in a CMOS digital processor or memory chip, to provide high-density, wide-bandwidth I/O at a low cost. CMOS optical transmitters operating at a data bit-rate of 1Gb/s or better have been shown in [13], [14].

In this chapter, the author will discuss the design of optical transmitter circuitry using CMOS and VCSEL technology. The discussion will begin with an introduction to the architecture of an optical transmitter circuit in section 2.2, followed by a detailed explanation and analysis of each circuit building blocks. These details are presented in section 2.3, for the pre-amplifier; section 2.4 for the decision stage; and section 2.5 for the laser driver. The author will present three different designs of laser driver and compare their performance with simulation results. The optical transmitter circuit is designed and implemented in a 0.18μm CMOS technology.

2.2. Architecture

Figure 2-1 shows a general architecture of an optical transmitter circuitry. It consists of three basic stages: 1) the pre-amplifier, 2) the decision stage, and 3) the laser driver.

As shown in Figure 2-1, the input signal is differential. In some cases, the input signals are single-ended, and the pre-amplifier is a single-input buffer. However, in recent high-speed digital communication systems, a differential signaling scheme is used vastly. A popular differential signaling standard is the "low-voltage differential signals" (LVDS) that is specified in IEEE standard 1596.3-1996 [15]. The transmitters designed by the author are based on LVDS input. The advantages of LVDS will be discussed in more detail in the following chapter, where the design of a LVDS output driver is explained.

The pre-amplifier is implemented with a gain-controlled fully differential amplifier. The differential signals that are fed to the chip need to be amplified by the pre-amplifier, before being fed to the decision stage. The decision stage will then restore the input signals to digital outputs of zeros and ones, with rail-to-rail voltage values. In order to minimize error incurred during this restoration process, the input signals at the decision stage must have a magnitude larger than the undefined region of the decision stage. The design of a pre-amplifier and decision stage will be discussed in section 2.3 and 2.4.

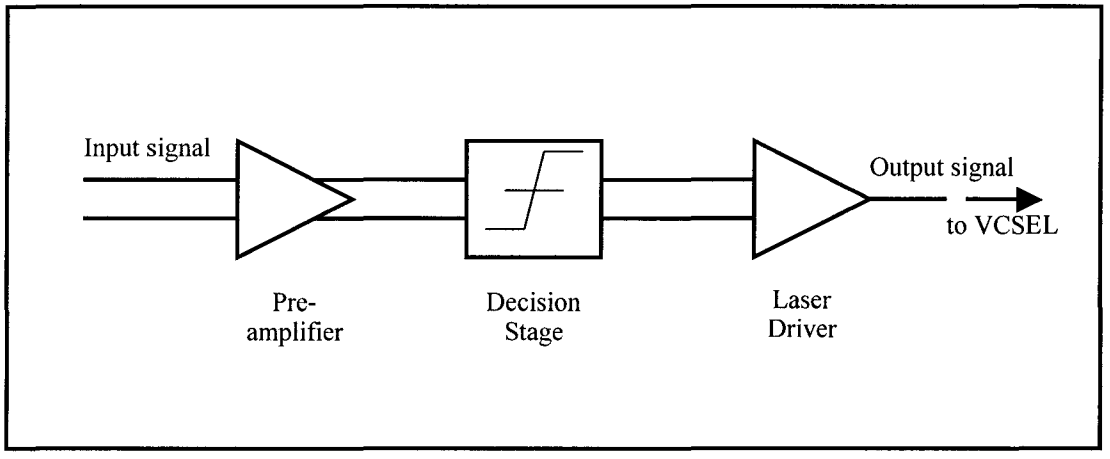


Figure 2-1: A block diagram showing the architecture of an optical transmitter circuitry.

A laser driver is actually a high-speed current modulator that is capable of switching current rapidly. For optical transmitters that transmit data at gigabits per second, the laser driver needs to modulate current at rise and fall times of less than 250ps, assuming that the rise-fall time is ¼ of a pulse width. In section 2.5, the author will look into how these laser drivers are designed.

2.3. Preamplifier

The pre-amplifier is designed based on LVDS input. Since a LVDS driver is a current driver, the differential input signal to the pre-amplifier is terminated with a resistive load having a differential resistance of 100Ω. The 100Ω resistor is implemented on chip. The pre-amplifier designed by the author consists of a gain-controlled fully differential amplifier, and an output voltage-offset control.

2.3.1. Gain-Controlled Fully Differential (GCFD) Amplifier

Figure 2-2 shows a schematic of the gain-controlled fully differential amplifier designed. The differential signal termination resistor is also shown in the schematic, as R_L. R_L is chosen to be 100Ω, to match the impedance of the microstrip lines on the test fixture.

The transistors M1 and M2 form a differential amplifier, with M4 and M5 as the active loads. The transistors M6, M7, and M8 construct a current mirror that provides biasing current, I_{bias} to the amplifier. The gate-source voltage of M6, and the sizes of

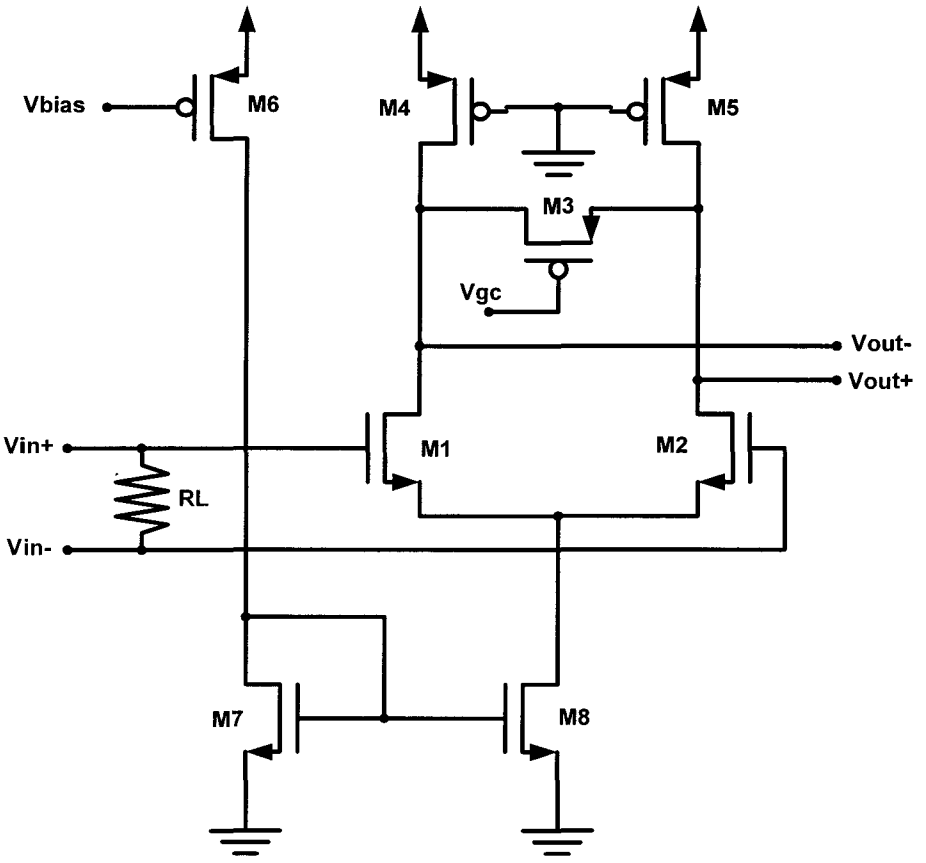


Figure 2-2: Schematic of the gain-controlled fully differential (GCFD) amplifier.

the transistors M6, M7, M8, determine the amplitude of I_{bias}. The gate-source voltage of M6 is controlled by an external, tunable DC voltage supply, V_{bias}. With the differential amplifier matched, I_{bias} splits equally between the two transistors M1 and M2. The drain current of M1 and M2 is equal to $I_{bias}/2$. This also implies that the drain voltage of M1 is equal to the drain voltage of M2, provided that the DC components of V_{in+} and V_{in-} are the same. Since the transistor M3 has its drain and source connected to the drains of M1 and M2, the DC voltage difference between these two nodes is zero. If M3 is turned on, i.e. $V_{GS} > V_t$, the gate-drain junction voltage, V_{GD}, will also be larger than V_t. Hence, M3

will be in triode as long as it is turned on. The gate of M3 is connected to an external tunable DC voltage source, V_{gc}. By varying the gate voltage of M3, the gain of the amplifier can be varied. A more detail discussion will follow.

2.3.1.1 Gain analysis

In this section, the author will perform small-signal analysis to study the design parameters for the voltage gain of a GCFD amplifier. Even though the signal involved might not be necessarily small, the analysis performed still provides a good idea of the design parameters for the voltage gain.

When a pair of differential signals V_{in+} and V_{in-} appears at the gate of the transistors M1 and M2, they will induce currents of $g_m V_{in+}$ and $g_m V_{in-}$ at the drain of M1 and M2 respectively. Each of the output voltages V_{out+} and V_{out-} is equal to the respective drain current multiplied by the respective load resistance. When M3 is in cut-off mode, $V_{out+} = g_{m2}(r_{DS5} || r_{o2}) V_{in-}$ and $V_{out-} = g_{m1}(r_{DS4} || r_{o1}) V_{in+}$. The amplifier will have a voltage gain of:

$$\left| \frac{V_{out}}{V_{in}} \right| = g_{m1,2}(r_{DS4,5} \parallel r_{o1,2}) \tag{2.1}$$

with $V_{out} = V_{out+} - V_{out-}$, $V_{in} = V_{in+} - V_{in-}$, and

$$g_{m1,2} = g_{m1} = g_{m2} = \sqrt{2\mu_n C_{OX} \left(\frac{W}{L}\right)_{1,2} \left(\frac{I_{bias}}{2}\right)} \tag{2.2}$$

$$r_{o1,2} = r_{o1} = r_{o2} = \frac{2V_A}{I_{bias}} \tag{2.3}$$

Since the gate of M4 and M5 is tied to ground (0V), such that $V_{SG} > |V_t|$ and $V_{DG} > |V_t|$, the transistors are biased in triode mode. The resistance that appears across the drain and source of M4 and M5 is

$$r_{DS4,5} = r_{DS4} = r_{DS5} = \left[\mu_p C_{OX} \left(\frac{W}{L} \right)_{4,5} \left(|V_{GD4,5}| - V_t \right) \right]^{-1} \quad (2.4)$$

Since it can be shown that the resistance $r_{o1,2}$ is normally much larger than $r_{DS4,5}$, the voltage gain of the amplifier is approximately

$$\left| \frac{V_{out}}{V_{in}} \right| \approx g_{m1,2} r_{DS4,5} \quad (2.5)$$

Equation 2.5 shows that the voltage gain of the amplifier is directly proportional to the transconductance gain, $g_{m1,2}$, of M1 and M2, and the drain-source resistance, $r_{DS4,5}$, of M4 and M5. According to equation (2.2) and (2.5), the voltage gain will be large if the width of transistors M1, M2 and I_{bias} is chosen to be large. Meanwhile, smaller transistors should be used for M4 and M5, to obtain a larger voltage gain, according to equation (2.4) and (2.5). Recognizing that the transistors M4 and M5 could be biased in saturation mode, if a higher voltage gain is desired. If M4 and M5 were in saturation, their drain-source resistance would have been

$$r_{DS4,5} = \frac{2V_A}{I_{bias}} \quad (2.6)$$

which will have a value larger than that of (2.4). However, the author designed the amplifier with a smaller $r_{DS4,5}$ (2.4), in favor of a higher bandwidth performance. This will be explained in the following subsection.

When M3 is turned on, it will be operating in triode mode with $V_{DS3} \approx 0V$. The resistance that appears across the drain and source terminals of M3 is

$$r_{DS3} = \left[\mu_n C_{OX} \left(\frac{W}{L} \right)_3 (V_{GS3} - V_t) \right]^{-1} \qquad (2.7)$$

When a differential signal is applied to the input of the amplifier, the voltage gain will be

$$\left| \frac{V_{out}}{V_{in}} \right| = g_{m1,2} \left(r_{DS4,5} \parallel \frac{r_{DS3}}{2} \right) \qquad (2.8)$$

Note that r_{DS3} can be varied by varying V_{GS3}. Hence, by tuning the voltage supply that determines V_{GS3}, the voltage gain of the amplifier can be varied. Note that even though M3 affects the signal voltage gain of the amplifier, it does not affect the DC biasing point [16]. This is true when the differential amplifier is perfectly matched, and hence causing the difference in the drain-source voltage of M3 in DC to be zero. Thus, the amount of DC current that flows through M3 is negligible. M3 is practically open-circuited under DC condition, regardless of the gate-source voltage.

2.3.1.2 Frequency analysis

In this section, the author will perform analysis that approximates the cut-off frequency of the GCFD amplifier, using open-circuit time-constant approximation [17]. Note that the purpose of the analysis here is not to obtain an exact expression for the cut-off frequency, but to illustrate the circuit design parameters that affect the circuit's speed performance. In order to simplify the analysis, the half-circuit equivalent of the GCFD amplifier will be considered. The half-circuit equivalent appears to be a common source amplifier, and the circuit model used for the analysis is as shown in Figure 2-3.

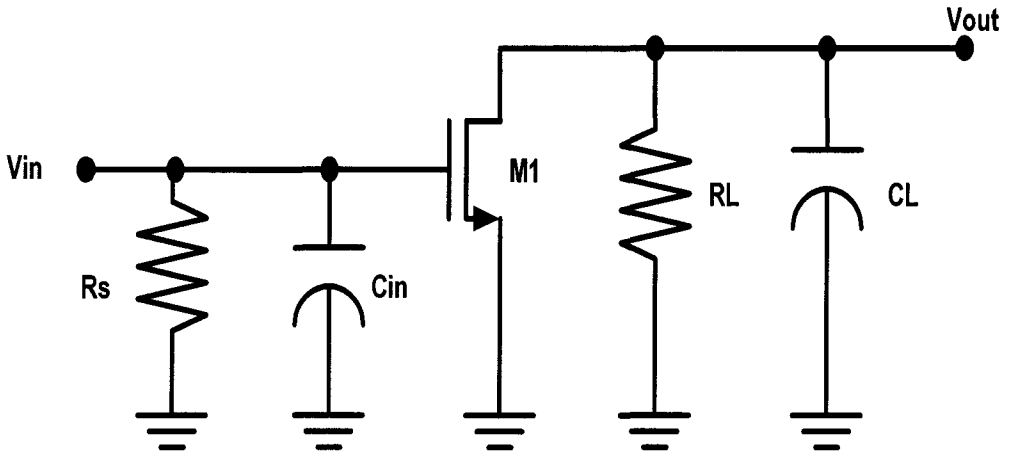


Figure 2-3: Half-circuit equivalent of the GCFD amplifier for frequency analysis.

In Figure 2-3, R_S represents the resistance that appears at the gate of the input transistor M1 or M2 of Figure 2-2. In this case, R_S is approximately 50Ω, the value of the termination resistor divided by two. C_{in} represents the effect of the transistor's gate-drain capacitance, $C_{gd1,2}$, and gate-source capacitance, $C_{gs1,2}$, of transistor M1 or M2. Since $C_{gd1,2}$ is connected between the input node (at the gate) and the output node (at the drain), it introduces feedback and complicates the analysis. However, Miller's theorem can be applied here to simplify the analysis by replacing the bridging $C_{gd1,2}$ with two grounded capacitors, one connected between the gate and ground, and the other between the drain and ground. Applying Miller's theorem [17],

$$C_{in} = C_{gs1,2} + (1 - A)C_{gd1,2} \tag{2.9}$$

A is the voltage gain from the input node to the output node. In this case, A is as given in equation (2.8), hence

$$C_{in} = C_{gs1,2} + \left[1 + g_{m1,2}\left(r_{DS4,5} \parallel \frac{r_{DS3}}{2}\right)\right]C_{gd1,2} \tag{2.10}$$

At the output node, the resistance R_L is a parallel combination of the resistances $r_{DS4,5}$ (equation 2.4), $\frac{r_{DS3}}{2}$ (equation 2.7), and $r_{o1,2}$ (equation 2.3).

$$R_L = r_{DS4,5} \| \frac{r_{DS3}}{2} \| r_{o1,2} \approx r_{DS4,5} \| \frac{r_{DS3}}{2} \tag{2.11}$$

C_L includes the effect of the gate-drain capacitance of the transistor M1 or M2, $C_{gd1,2}$, the gate-drain capacitance of the transistor M4 or M5, $C_{gd4,5}$, the gate-drain or gate-source capacitance of M3, and the load capacitance, C_{load}. Since M3 is biased in triode, its gate-drain capacitance is equal to its gate-source capacitance. Due to the feedback connection of $C_{gd1,2}$ between the input and the output node, Miller's theorem is used in order to determine the effect of $C_{gd1,2}$ on C_L. Applying Miller's theorem [17] on $C_{gd1,2}$,

$$\begin{aligned} C_L &= C_{gd3} + C_{gd4,5} + \left(1 - \frac{1}{A}\right) C_{gd1,2} + C_{load} \\ &\approx C_{gd3} + C_{gd4,5} + C_{load} \end{aligned} \tag{2.12}$$

A is as given in equation (2.8).

In an open-circuit time constant approximation approach, the locations of the high-frequency poles can be found by taking the inverse of the RC time constant. The cut-off frequency of the circuit will then be approximately the frequency of the lowest frequency pole. In other words, that would be the pole with the largest RC time constant.

For the GCFD amplifier, there are two poles, one at the input node and one at the output node. The frequencies of the two poles are

$$\omega_{p1} = \frac{1}{R_S C_{in}} \tag{2.13}$$

and

$$\omega_{p2} = \frac{1}{R_L C_L} \tag{2.14}$$

Either one of ω_{p1} or ω_{p2} can be the cut-off frequency of the circuit, depending on which one has a smaller value. The value of ω_{p1} is dependent on R_S and C_{in}. R_S has a small value, but C_{in} could have a considerably large value, due to the $(1-A)C_{gd1,2}$ factor (equation 2.9). On the other hand, the value of ω_{p2} is depending on R_L and C_L. R_L, as given in equation 2.11, is almost always greater than R_S. At the same time C_L (equation 2.12) could be considerably large, depending on the value of C_{load}. C_{load} depends on he design of the succeeding stage. For example, if the succeeding stage is another differential amplifier, C_{load} will have a similar expression as equation 2.9.

Two ways to increase the cut-off frequency are 1) reduce R_L and 2) reduce C_{in}. Approach 1) explains directly why the author chooses to bias M4 and M5 in triode. By biasing M4 and M5 in triode, $r_{DS4,5}$ will have a smaller value, as given in equation 2.4, as oppose to the expression given by equation 2.6. In addition to the reduction of R_L, a smaller $r_{DS4,5}$ results in a smaller voltage gain A (equation 2.8), and hence a smaller C_{in}. This contributes to an increase in ω_{p1}. Note that the increase in data bit-rate comes in the expense of a decrease in voltage gain.

Before leaving the frequency analysis of the GCFD amplifier, the author would like to point out that the effect of the parasitic capacitance, resistance, and inductance of the bonding pad, the bond wire, and the microstrip line to the data bit-rate is not considered in the analysis above. Even though the author chose to concentrate the frequency analysis on the circuit itself, the effect of these parasitic elements on the design's speed limit is not negligible. While the above analysis concentrate solely on the CMOS circuit, the effect of such parasitic elements on a high-speed circuit design is discussed in [18] and [19].

2.3.1.3 Simulation results

A GCFD amplifier was designed and simulated to study its gain and frequency performance, as well as its gain controlling ability. Figure 2-4 shows the frequency response of the circuit due to different values of the gain controlling voltage V_{gc}. The simulation results show that the signal voltage gain decreases with smaller gain controlling voltages. The GCFD amplifier has the largest voltage gain when the transistor M3 is in cutoff. From simulation, when V_{gc}=1.8V (M3 is in cutoff since it is a PMOS), the amplifier has a voltage gain of 17.9dB. When V_{gc}=0V, the voltage gain is 11.2dB. As the gain increases, the 3dB cutoff frequency f_{3dB} decreases. For V_{gc}=1.8V, f_{3dB} is 0.99GHz, while for V_{gc}=0V, f_{3dB} is 1.87GHz. These simulation results verify the effect of varying V_{gc} (or in other words, the effective resistance across M3, r_{DS3}) on the amplifier's voltage gain and frequency response, which correspond to the analysis in section 2.3.1.1

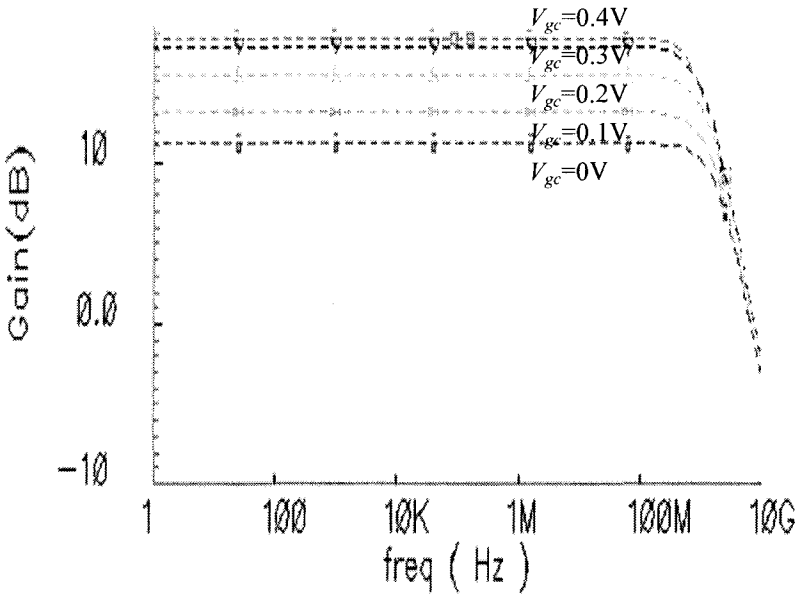


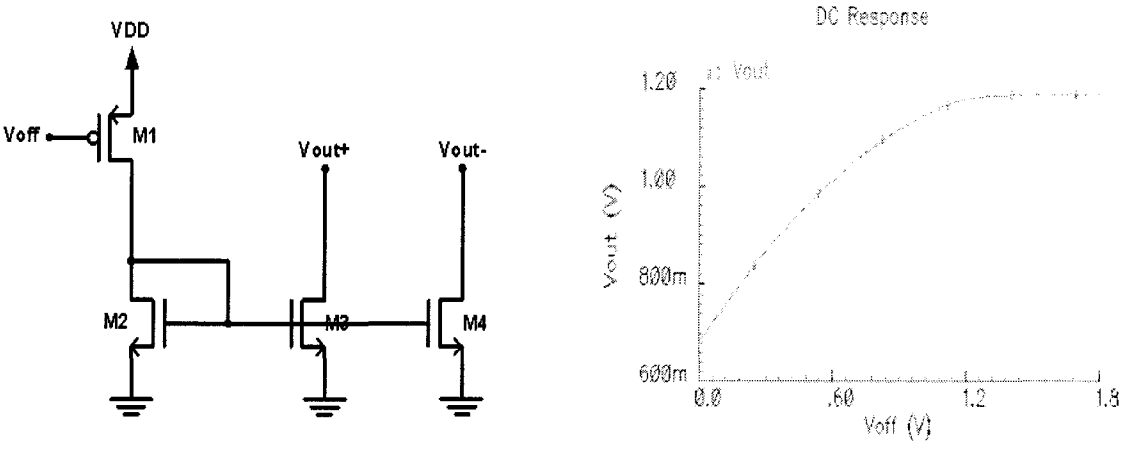
Figure 2-4: Frequency response of a GCFD amplifier due to different values of gain controlling voltage.

and 2.3.1.2. Note that the GCFD amplifier is not designed to have a large voltage gain here, as the expected input signal is LVDS signal with voltage swing of 400mV. Rather, it is designed to handle a data bit-rate of at least 4Gbps.

Simulations were also performed to show that the transistor M3 does not affect the DC operating point at the output of the amplifier. According to simulation results, the variation in the DC output voltage is only 0.9mV, when V_{gc} is varied from 0V to 1.8V.

2.3.2 Offset Control Circuit

The output of the preamplifier is connected to a decision stage and its output waveform will be restored to digital levels of zeros and ones. In order to obtain a 50% duty-cycle digital output waveform, the input signal to the decision stage is required to have an average voltage equal to the threshold voltage of the decision stage. Therefore, the output of the preamplifier needs to be controlled at an appropriate average value. This could be done with a simple offset control circuit as shown in Figure 2-5a).



a) b)

Figure 2-5: a) Schematic of an offset control circuit. b) The average output voltage of the preamplifier with respect to V_{off}.

The offset control circuitry consists of two simple current mirrors constructed by M1, M2, M3 and M4. The output of each current mirror is connected to either one of the two differential outputs of the preamplifier. The amount of current sunk by M3 and M4 changes according to the variation in the control voltage, V_{off}, at the gate of M1. Since these two transistors are connected to the outputs of the preamplifier, the DC output offset voltage of the preamplifier will be affected by the amount of current sunk by M3 and M4. Note that the resolution and the range of the DC output offset voltage controllable by V_{off} is determined by the ratio of the transistors' sizes M3 to M2, and M4 to M2, as well as the size of M1.

Figure 2-5b) shows the variation of the preamplifier's average output voltage with respect to V_{off}. V_{off} could be controlled by off-chip variable voltage supply, or on-chip automatic offset control circuitry with feedback. The result was obtained from a simulation performed on a preamplifier with an offset control circuitry. As shown in the plot, the average output voltage does not change when V_{off} gets greater than 1.2V. That is because M1 is cut-off when V_{off} is greater than 1.2V, and the offset control circuit is no longer functioning.

2.4 Decision Stage

A decision stage is practically a non-linear amplifier that amplifies any input voltage greater than a certain threshold value, V_M, to a defined high-level output voltage, and restores any input voltage smaller than that same threshold value, to a defined low-level output voltage. In digital circuits, the high-level output voltage dictates a one, and the low-level output voltage dictates a zero; and they are represented by the circuit's

maximum and minimum supply voltage respectively. Such non-linear amplifier can be implemented with a static CMOS inverter, which will be discussed in the following subsection (2.4.1).

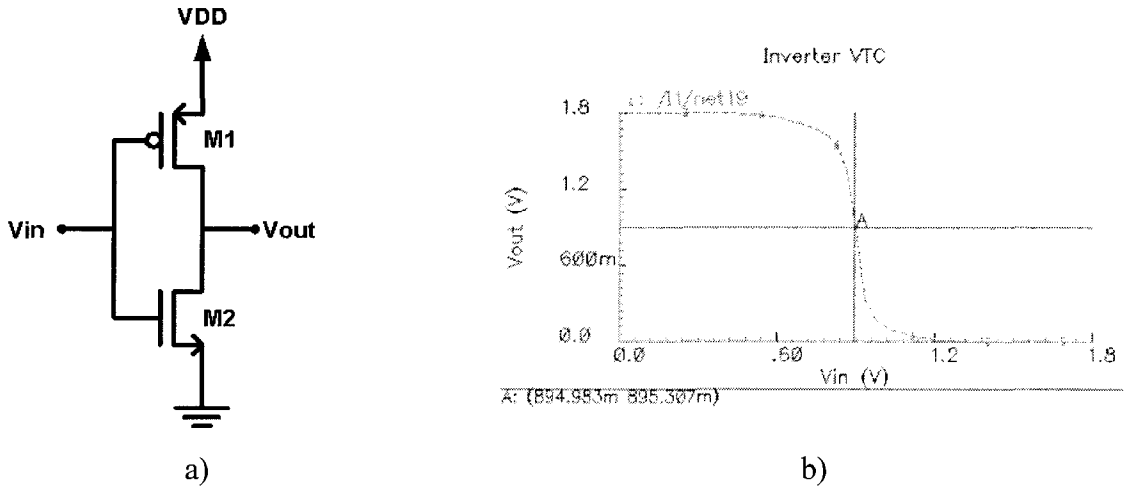
The outputs of the decision stage are connected to the inputs of a laser driver. Laser drivers are usually comparatively large circuits, which present huge load capacitance to the outputs of a decision stage. In order to achieve good speed performance, a buffer circuit is needed to drive the huge load capacitance. Possible designs of buffer circuit will be discussed in 2.4.2.

In section 2.4.3, the author will discuss a digital level converter that converts the high-level voltage from one voltage value (i.e. 1.8V), to another (3.3V). This is needed for a circuit design that uses a different maximum positive power supply.

All these circuits are represented by the black box of the decision stage.

2.4.1 Static CMOS inverter

Figure 2-6a) shows a schematic of a static CMOS inverter, and Figure 2-6b) shows its voltage transfer characteristic (VTC). The circuit is designed in TSMC 0.18μm CMOS technology that utilizes 1.8V as VDD [20], [21]. The VTC of 2-6b) shows that when the input voltage is lower than the switching threshold voltage V_M, denoted by the marker 'A', the inverter has a high output voltage level equals to VDD. As the input voltage is greater than V_M, the inverter has a low output voltage level equals to 0V. The switching threshold voltage V_M is defined as the point where $V_{in} = V_{out}$. It can be shown that V_M of a static CMOS inverter can be set by designing the ratio of the sizes of the



a) b)

Figure 2-6: a) Schematic of a static CMOS inverter. b) Voltage transfer characteristic (VTC) of a static CMOS inverter.

PMOS transistor to the NMOS transistor [22]. In this design, the author has chosen the size ratio such that V_M is ½ of VDD, so that the circuit has equal noise margin (NM) for both the low and the high input signal.

In order to study the circuit design parameters that affect speed performance, the inverter is assumed to be connected to a capacitive load, C_L, which includes the parasitic capacitance of the succeeding circuit, the parasitic capacitance of the inverter itself, and the interconnect capacitance. The speed performance (data-bit rate) is determined by the inverter's rise-fall time.

When the input of the inverter changes from high to low, the output of the static CMOS inverter will be changing from low to high. During this transition, an amount of output current will be charging up the load capacitance. An expression of this output current is given by

$$i_{out} = C_L \frac{dV_{out}}{dt} = C_M \left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt} \right) + i_P - i_N \qquad (2.16)$$

where C_M is the gate-drain capacitance of the PMOS and the NMOS transistors, i_P and i_N are the instantaneous drain currents of the PMOS and NMOS transistors respectively. Cross multiplying equation (2.16) by dt and taking an integration of the equation gives

$$\int_{0.1VDD}^{0.9VDD} dV_{out} = \left(\frac{C_M}{C_L + C_M} \right) \int_{VDD}^{0} dV_{in} + \frac{1}{C_L + C_M} \int_{t_r} (i_P - i_N) dt \qquad (2.17)$$

The mathematics can be greatly simplified if $(i_P - i_N)$ is replaced by its average value. During the transition, the NMOS transistor is assumed to switch from saturation to cutoff, and the other way round for the PMOS transistor. Using the *n*th-power law MOSFET model proposed by T. Sakurai and A. Newton [23] for submicron devices, the average value for $(i_P - i_N)$ is

$$(i_P - i_N)_{ave} = \frac{\frac{W_P}{L_{effP}} B_P (VDD - V_{tP})^n - \frac{W_N}{L_{effN}} B_N (VDD - V_{tN})^n}{2} \qquad (2.18)$$

Solving equation (2.17) gives an expression for the rise-time of the static CMOS inverter's output:

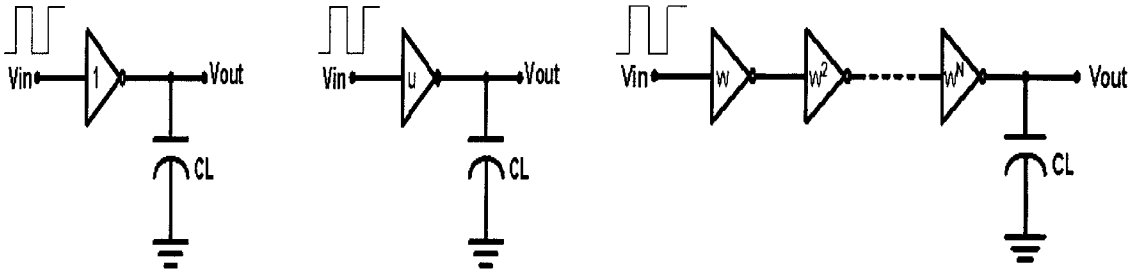
$$t_r = \frac{VDD(1.8C_M + 0.8C_L)}{(i_P - i_N)_{ave}} \qquad (2.19)$$

Even though equation 2.19 is only an approximation of the rise time, it illustrates how the design parameters affect the rise time. An inverter will have a longer rise time if it has to drive a larger load capacitance. In addition to that, equations 2.18 and 2.19 show that the rise time of the inverter is a function of the transistors' sizes. Note that a similar analysis

and conclusion can be made for the fall-time of the inverter. In order to optimize the data bit-rate performance, the rise time is designed to be equal to the fall time.

2.4.2 Buffer

From the previous subsection, it was shown that the rise-fall time of a static CMOS inverter is directly proportional to the load capacitance and inversely proportional to the transistors' width. Hence, a shorter rise-fall time can be obtained from an inverter constructed of wider transistors. However, as the width of the transistors is increased, the parasitic capacitance at the input of the inverter will be increased at the same time. This means that the preceding circuit will have to drive a larger load capacitance. Therefore, there is an optimum value for the size of the inverter. If the transistors' width is increased beyond such optimum value, the overall speed performance of the system will not improve as predicted in equations 2.18 and 2.19, but in fact, it will degrade. In the case where a very large load capacitance appears at the output, a buffer circuit can help to improve the overall speed performance. Figure 2-7 shows how the buffer circuit improves overall speed performance in terms of the rise-fall time.



a) b) c)

Figure 2-7: a) A minimum-size buffer, b) a buffer u times the minimum size, c) cascade of N buffers with increasing gate size, connected to load capacitance, C_L.

Figure 2-7a) shows a minimum-size buffer connected to a load capacitance C_L. Assume that the buffer has an input capacitance C_{in}, k times smaller than C_L and it is driven by a preceding stage (which can be a static CMOS inverter) with a rise-fall time of t_{r_in0}, at the input of the buffer. Note that the buffer can be designed to have equal rise time and fall time. According to equations 2.18 and 2.19, the buffer's output rise-fall time is directly proportional to C_L and inversely proportional to its gate size. Thus, the output rise-fall time is

$$t_{r\_out1} = kt_{r\_in0} \tag{2.20}$$

The overall system performance is dominated by the worst case rise-fall time, which is given by the relationship in 2.20.

In Figure 2-7b), a buffer u times larger is used. The input capacitance of the buffer will also be u times larger. Assuming that the buffer is also driven by a same signal source as in the previous case, the input rise-fall time at the is now

$$t_{r\_in2} = ut_{r\_in0} \tag{2.21}$$

which is also u times longer than the previous case, due to the larger input capacitance of the buffer. However, since the buffer size has been increased, the rise-fall time of the output signal will also decrease accordingly, hence by assuming a same load capacitance,

$$t_{r\_out2} = \frac{k}{u} t_{r\_in0} \tag{2.22}$$

The rise-fall time of the overall system is optimized when t_{r_in2} is equal to t_{r_out2}. This can be achieved when the buffer is designed to have a size of $u = \sqrt{k}$. The optimum rise-fall time of the system will be $t_{r2} = \sqrt{k} t_{r\_in0}$, which is smaller than the previous circuit.

In Figure 2-7c), N buffers are connected in cascade, and each buffer is w times larger than its preceding circuit. In this case, the input of the first buffer is still driven by a same signal source as the previous two cases. The rise-fall time at the input of each buffer is now

$$t_{r\_in3} = wt_{r\_in0} \tag{2.23}$$

and the rise-fall time at the output is

$$t_{r\_out3} = \frac{k}{w^N} t_{r\_in0} \tag{2.24}$$

In order to optimize the rise-fall time of the overall system, the buffers will have to be designed such that $w = k^{\frac{1}{N+1}}$. This gives an optimum rise-fall time of $t_{r3} = k^{\frac{1}{N+1}} t_{r\_in0}$, which is superior to the previous two circuits in terms of speed performance.

Figure 2-8a) shows a schematic of a decision stage designed by the author. There are two pairs of static CMOS inverter in the schematic, which forms a 2-stage buffer circuit. Each pair of the inverter handles an equal but opposite differential signals. The The second buffer is four times as large as the first buffer.

Figure 2-8b) presents the voltage transfer characteristic (VTC) of the decision stage from simulation. The VTC shows that the decision stage has a low output (0V) when the input voltage is lower than the threshold voltage and a high output (1.8V) when the input is higher than the threshold voltage. The switching threshold is shown by cursor 'A', at a value of 0.88V. The steep slope around the threshold voltage contributes to a very-small undefined region that is only 44mV.

Figure 2–8c) shows the transient response of the decision stage when it is connected to a 40fF capacitor. The output waveform has a rise time of 55ps and a fall

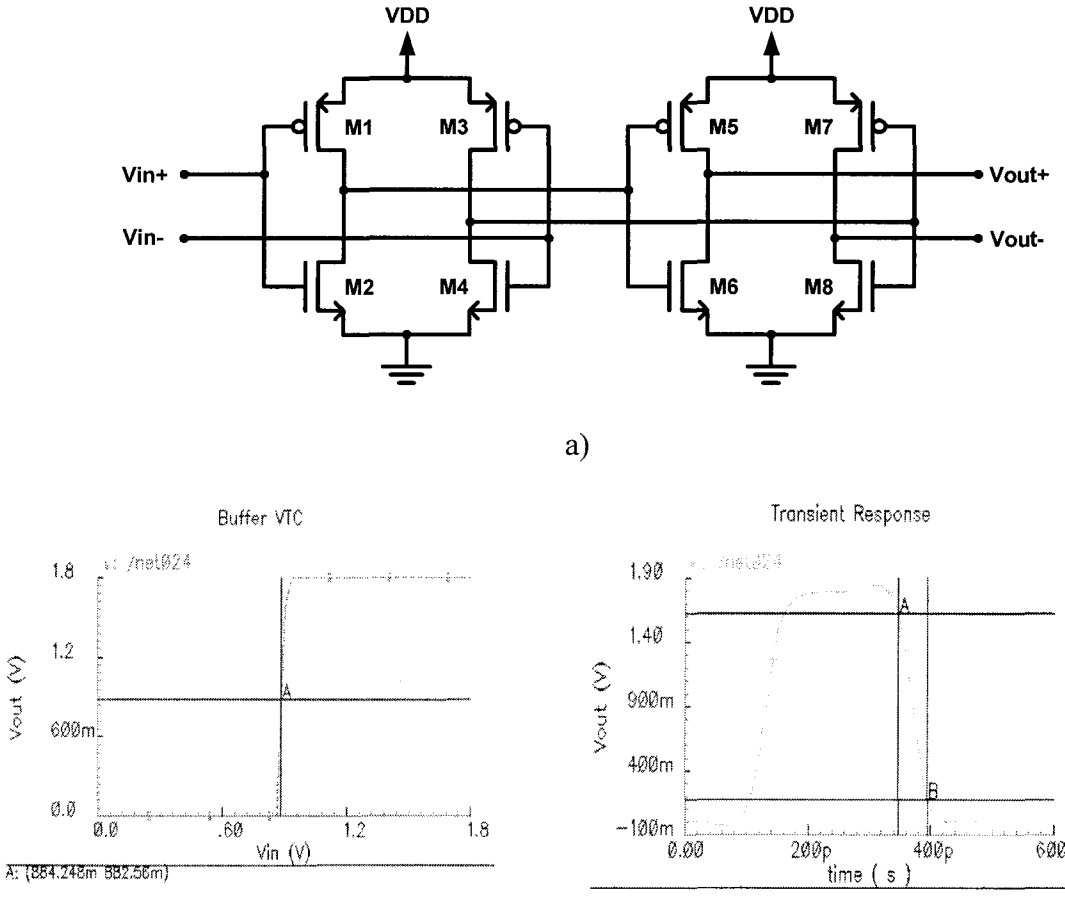


Figure 2-8: a) Schematic of a decision stage. b) Voltage transfer characteristic of the decision stage shows a switching threshold at 0.88V. c) Transient response of the decision stage connected to a 40fF capacitor shows t_r = 55ps, t_f = 48ps.

time of 48ps. In the design of the optical transmitters, the decision stage will be connected to circuits that have input capacitance smaller than 40fF. Thus, the decision stage is capable of handling data bit rate of 4Gbps or better.

2.4.3 Digital Level Converter

One of the three VCSEL drivers that will be discussed in the following section utilizes a 3.3V power supply. Since the digital high voltage level of the decision stage designed is 1.8V, a circuit that interfaces the decision stage with that particular VCSEL driver is required to convert the digital high voltage level to 3.3V. This circuit is no more than cascades of static CMOS inverters (buffers), where the sizes of the transistors are designed to provide a VTC with high level output voltage of 3.3V and low level output voltage of 0V, and an appropriate switching threshold. Since the output of the decision stage has a range of 0V-1.8V, the switching threshold of the level converter is designed to be close to 0.9V (half of the input range).

2.5 Laser Driver

A laser driver modulates the optical output power of a laser by modulating the amount of current flowing through the laser, according to the signal to be transmitted. In most cases, the laser drivers also provide a DC constant current, I_{BIAS}, to bias the laser above threshold. This is to minimize the turn-on delay of the laser due to relaxation oscillation that happens when the laser crosses the threshold point [24]-[27]. The modulation current is then superimposed on top of the biasing current.

The design of a laser driver is influenced by the characteristic of the laser. The circuits that are discussed here are designed to drive a 4×1 VCSEL chip supplied by *EMCORE Corporation* [28]. Before going into the details of the design of the laser

Characteristics	Typical value	Unit
Peak emission wavelength	850	nm
Optical rise and fall time	60	ps
Slope efficiency	0.45	mW/mA
Threshold current (P = 80μW)	1.5	mA
Laser forward voltage (I = 8mA)	1.9	V
Differential resistance	50	Ω

Table 2-1: Summary of the VCSEL characteristic [29].

drivers, some important characteristics of the VCSEL used are summarized in Table 2-1 [29]. The VCSEL has a typical threshold current of 1.5mA. Thus, the laser drivers will be designed to provide a biasing current well above that value.

In the following subsections, the author will present three different designs of laser drivers. These laser drivers are designed in a 0.18μm CMOS technology. They are referred by the author as 1) current steering laser driver, 2) fast-discharge laser driver, and 3) push-pull laser driver. The fast-discharge and the push-pull laser drivers are implemented on a CMOS chip and fabricated by Taiwan Semiconductor Manufacturing Co. (TSMC) through Canadian Microelectronics Corporation (CMC).

2.5.1 Current Steering Laser Driver

Figure 2-9 shows a schematic of the current steering laser driver. This circuit

design is similar to the designs presented by *D. V. Plant, et al*, in [30], and *N. Harabidis* and *G. Halkias* in [14]. In [14] and [30], the laser drivers are designed with NMOS devices, as opposed to the design in Figure 2-9 that uses PMOS devices.

The author designed the laser driver in PMOS for the following two reasons. First of all, the VCSELs available (a 4×1 VCSEL array) have common n-contact. Thus the n-contact of the VCSELs will have to be connected to a common DC biasing voltage. Only the p-contact of each VCSEL is available to the laser driver circuits. With this configuration, the laser driver designed pushes current into the VCSEL, whereas the designs in [14] and [30] pull current. Secondly, V_{ln}, the DC biasing voltage at the n-contact of VCSEL, is a negative voltage. A negative voltage could possibly appear at the drain/source terminal of the MOSFET devices connected to the VCSEL. If NMOS

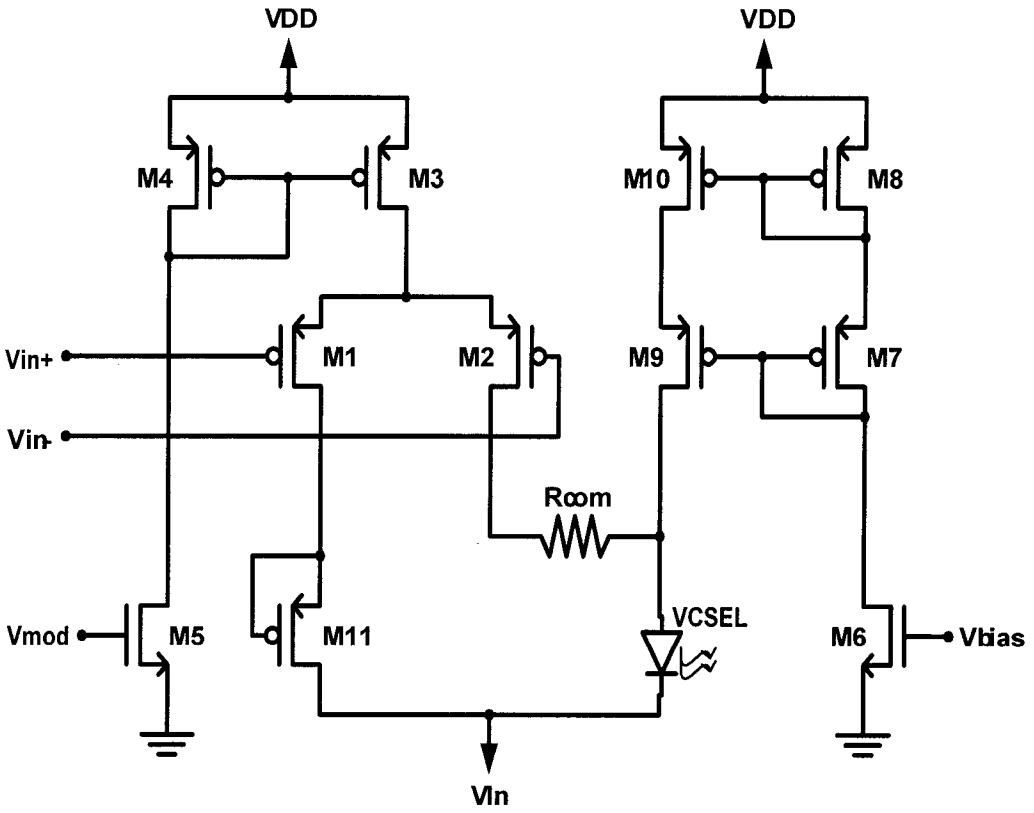


Figure 2-9: Schematic of a current steering laser driver.

devices were used, a negative voltage appearing at the drain/source terminal of the devices could cause a forward biasing at the body-drain or body-source junction (since the NMOS's p-substrate is always connected to ground). This may cause substantial, undesirable current flow, and hence damaging the devices. The same phenomenon will not happen with PMOS devices since its body (n-substrate) is always connected to VCC, hence reverse biasing the drain-body and source-body junctions.

In Figure 2-9, the transistors M6-M10 form a cascode current mirror that provides the DC biasing current, I_{BIAS}, to the VCSEL. The amount of current sourced by the current mirror is adjustable between 0 to 2.1mA by varying V_{bias} using an external voltage supply. For normal operation, V_{bias} is set such that I_{BIAS} is 2mA, which is above the threshold current of the VCSEL. The cascode current mirror design has an advantage of high output resistance that minimizes loading effect to the laser driver's output.

M3, M4 and M5 form a simple current mirror that provides the modulation current, I_{mod}. The amount of modulation current is again adjustable by an external voltage supply, V_{mod}. I_{mod} is adjustable between a range of 0 to 10.7mA. For normal operation, V_{mod} is selected to give a modulation current of 10mA.

M1 and M2 form a differential pair that steers the modulation current either into the VCSEL, or into the diode-connected transistor, M11. The size of the transistor M11 is chosen such that it presents an active load that is matched to the output load, i.e. the VCSEL. This load matching helps to reduce the switching noise induced by the laser driver. M1 and M2 are designed with relatively large transistors, in order to handle the large amount of modulation current ($\geq$ 10mA). Hence, the differential pair formed by M1 and M2 has small output resistance. The input voltages V_{in+} and V_{in-} are rail-to-rail (0V –

1.8V) digital signals. These signals will switch the transistors M1 and M2 between cut-off mode and triode mode.

The laser driver will be connected to a VCSEL chip through a bond-wire. At the speed of which the laser driver is designed, the parasitic inductance of the bond-wire can cause signal ringing (oscillations). This will impair the speed performance of the laser driver. Thus, as shown in Figure 2-9, an on-chip resistor, R_{com}, is placed between the output of the differential pair and the output wire-bonding pad (not shown in Figure 2-9) connected to the VCSEL, in order to damp signal ringing caused by the parasitic inductance. More detail discussions of the effect of the wire-bond inductance and R_{com} is presented in the following subsection with simulation results of a simple circuit model.

2.5.1.1 Effect of parasitic inductance and compensation resistor on high-speed performance of a laser driver

The effect of interconnection parasitic on high-speed circuits has been analyzed by *N. Hassaine et al*, in [18] and *A. J. Rainal* in [31]. A relatively short bond-wire of approximately 1mm can have a parasitic inductance of ~1nH, which could cause signal ringing if the signal has a short rise-fall time, or in other word, a large $\frac{dI}{dt}$. In [32], John R. Brews derived that for a driver circuit with an output resistance R_D driving a *RLC* interconnect with negligible parasitic resistance, that is connected to a capacitive load C_L, signal ringing can be eliminated by having

$$R_D \geq \sqrt{\frac{L}{C}}\left\{1-\left(\frac{C_L/Cl}{1+C_L/Cl}\right)^2\right\}^{1/2} \qquad (2.25)$$

; where L and C are the interconnect parasitic inductance and capacitance respectively, and l is the interconnect length.

The laser driver circuit presented has a similar situation to the 2nd order *RLC* network used by Brews to derive (2.25). The circuit model shown in Figure 2-10 is used to simulate the effect of parasitic inductance and compensation resistor, R_{com}, to the laser driver's signal. In Figure 2-10, C_S represents the parasitic capacitance of the laser driver, C_p is the capacitance of the bonding pad, and C_L includes the parasitic capacitance of the bond-wire, the bonding pad, and the VCSEL. L is the inductance of the bond-wire, R_L is the differential resistance of the VCSEL, and R_{com} is the on-chip compensation resistor. Unfortunately, the circuit model in Figure 2-10 represents a 4th order *RLC* network. It is impossible to obtain a simple, close-form solution as in (2.25) to determine an appropriate value for R_{com} for which signal ringing is minimized. Thus, the value of R_{com} will have to be obtained from circuit simulations. A circuit simulation is performed for the circuit in Figure 2-10, with C_S= 50fF, C_p= 500fF, C_L= 1.35pF, L= 1nH, and R_L= 50Ω. Input current that has a 2mA-10mA current swing and 10ps rise-fall time at 1Gbps is used. The output current that flows into the VCSEL's differential resistance R_L is

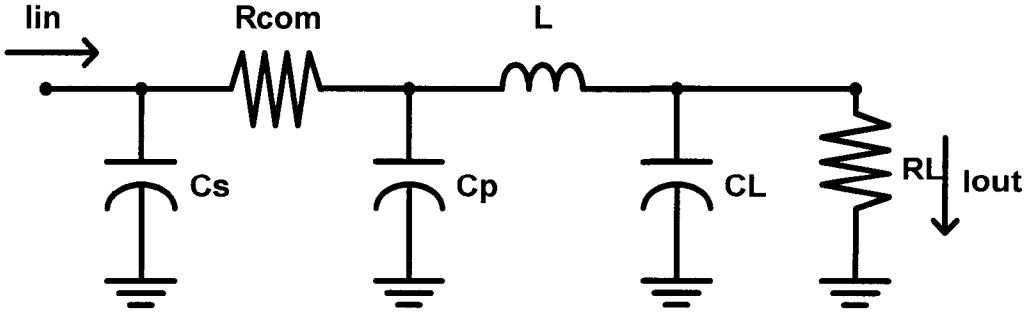
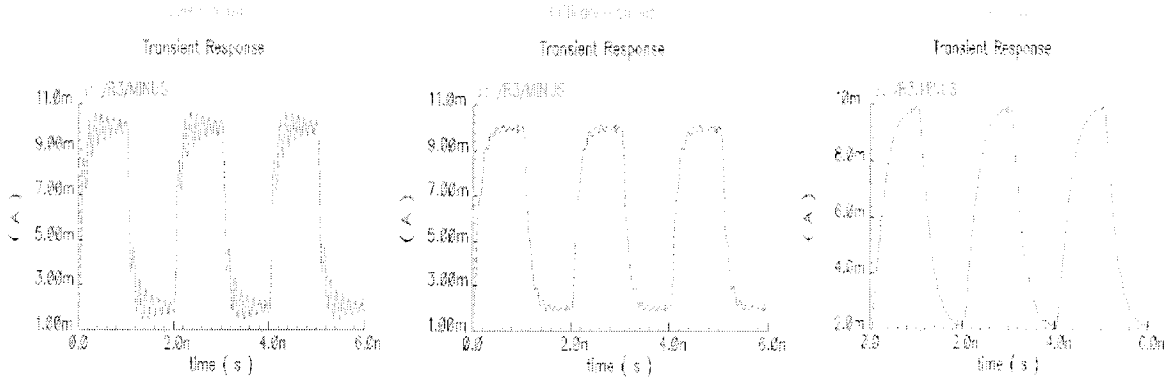


Figure 2-10: *RLC* circuit model to simulate the effect of bond-wire parasitic and compensation resistor.

plotted in Figure 2-11 for a) R_{com} = 0Ω, where the signal is underdamped and signal ringing occurs, b) R_{com} = 1kΩ, where the signal ringing is minimized, and c) R_{com} = 4kΩ, where the signal is overdamped.

In the design of the laser driver, the compensation resistor is selected carefully to minimize signal ringing. And yet, the compensation resistor should not be too large to overdamp the signal. The compensation resistor is also utilized in the other two laser driver designs that are presented in subsequent sections.



a) b) c)

Figure 2-11: Transient response of I_{out} in Figure 2-10 for a) R_{com} = 0Ω, b) R_{com} = 1kΩ, and c) R_{com} = 4kΩ.

2.5.1.2 Circuit simulation

The current steering laser driver is simulated with *Spectra*, together with the preamplifier and the decision stage. Figure 2-12 shows a block diagram of the circuit simulated. The input signal used for the simulation is a pair of LVDS signal, applied to a pair of microstrip lines. The LVDS signals have voltage swing of 1V to 1.4V, and rise-fall time of 50ps. The microstrip lines are connected to the inputs of the preamplifier

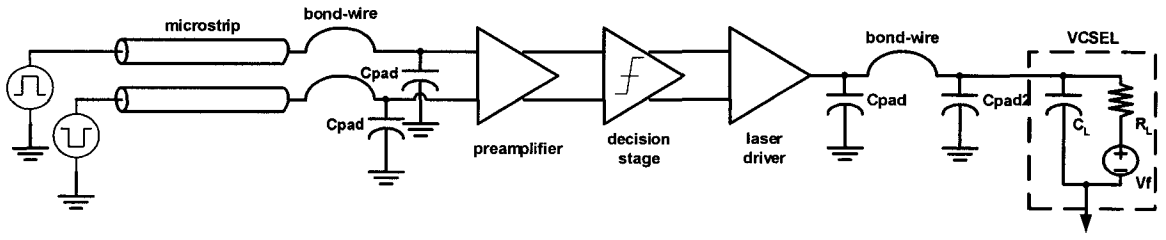


Figure 2-12: Block diagram of circuit used to simulate the optical transmitter.

through a pair of 1mm long bond-wires. The parasitic capacitance of the bonding pads (C_{pad} = 0.5pF) is also included. The output of the laser driver is connected to the VCSEL through another bond-wire (1mm), including the bonding pad of the CMOS chip (C_{pad} = 0.5pF) and the bonding pad of the VCSEL (C_{pad} = 0.35pF). The VCSEL is modeled by a parasitic capacitance, C_L = 1pF in parallel with its differential resistance, R_L = 50Ω. A DC voltage source models the VCSEL's forward bias voltage, V_f, of 1.9V.

Figure 2-13 shows a transient response of the current provided to the VCSEL, at a data bit-rate of 1Gbps. The current swings between 2.2mA to 11.4mA. The current rise time is 143ps and the current fall time is 278ps. The static power consumption of the circuit is 15.4mW.

Two important characteristics of this current steering laser driver can be observed from the transient response in Figure 2-13. First of all, the current fall time is more than twice as large as the current rise time. This is because the transistor M2 (Figure 2-9) has to switch from triode mode to cutoff mode when the input signal at the gate of M2 switches from a high voltage level (1.8V) to a low voltage level (0V). When the transistor is in triode mode, a parasitic capacitance appears at the gate-drain junction. It takes time

to discharge the gate-drain capacitance as the transistor switches, and hence increasing the fall time of the current provided to the VCSEL.

Second of all, when the gate voltage of M2 switches from high to low, there are current undershoots and overshoots at the rising edge of the output signal. This is because during the transition, the gate voltage of M2 crosses the threshold point before the gate voltage of M1. Hence, M2 is turned on before M1 is completely cut off. During this transition, the modulation current sourced by M3 (Figure 2-9) fluctuates, and hence causing current-overshoot and current-undershoot at the output.

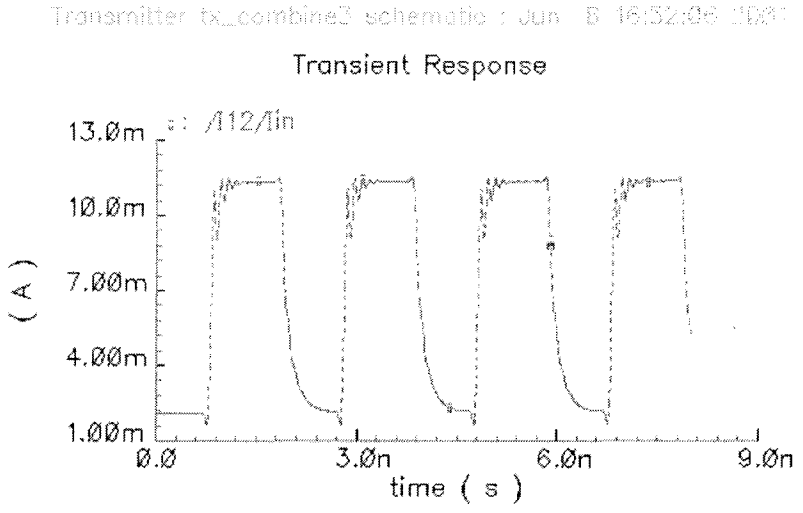


Figure 2-13: Transient response of the current provided to VCSEL by the current steering laser driver, at 1Gbps.

2.5.2 Fast-Discharge Laser Driver

The fast-discharge laser driver designed by the author is similar to the designs presented in [33], [34], and [35]. As shown in Figure 2-14, a fast-discharge laser driver consists of an extra stage formed by M1, M2, M3, and M4. This stage is a special-

purpose fully differential amplifier referred as the pulse shaping stage in [33] and [34]. M8, M9 and M10 form a simple current mirror that sets the biasing current of the pulse shaping stage. M5 and M6 form a current steering laser driver similar to the design presented in the previous section.

A major distinction of this design is that the current steering stage formed by M5 and M6 is always operating in saturation mode, as oppose to the previous design where the current steering laser driver is switched between cutoff and triode mode during operation. This distinctive characteristic of a fast-discharge laser driver leads to two advantages over a current steering laser driver. Firstly, the transistors M5 and M6 will

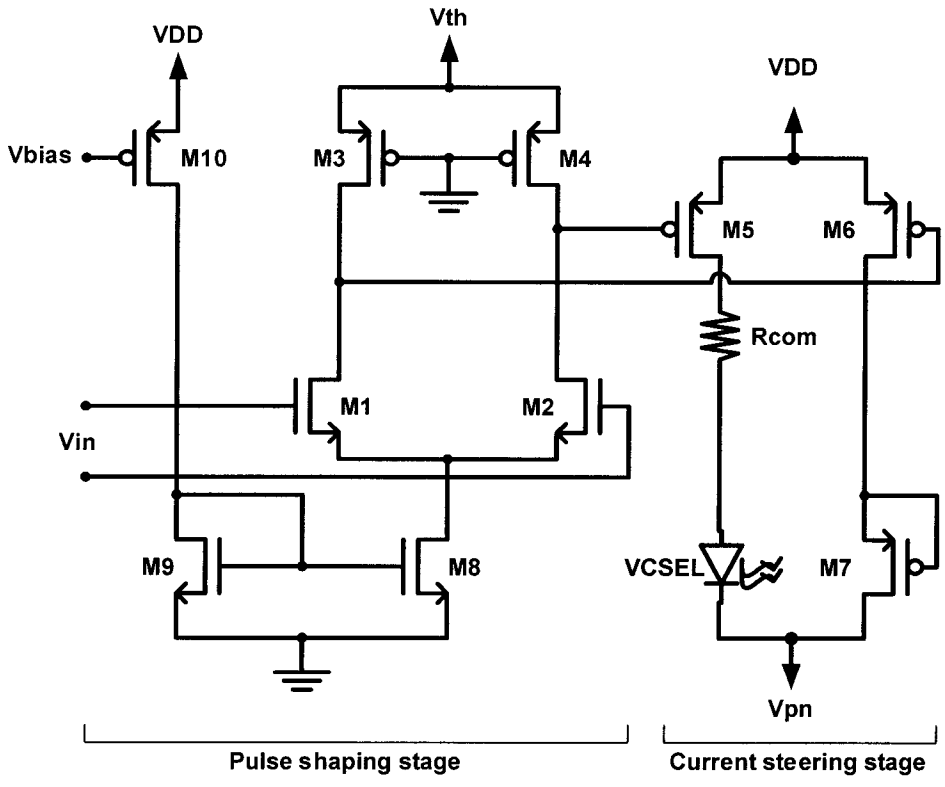


Figure 2-14: Schematic of a fast-discharge laser driver.

never cross the threshold point. Thus, current fluctuation due to the unsynchronized switching of M5 and M6 is avoided, and hence minimizes the overshoot and undershoot at the rising edge of the current signal. Secondly, since the driver is always operating in saturation mode, it does not have to discharge the gate-drain capacitance (which is significant in triode mode) during the falling edge of the current signal. The laser driver has a shorter current fall-time and hence it is called the fast-discharge laser driver.

The pulse shaping stage takes in rail-to-rail digital signals and is designed to provide signals with appropriate voltage levels to the current steering stage such that it is always operating in saturation mode. Note that the source of M3 and M4 are connected to a positive DC voltage, V_{th}, which is also the maximum voltage available to the input of the current steering stage. Since M5 and M6 are PMOS devices, V_{th} determines the minimum amount of current sourced by the transistors. V_{th} is carefully chosen such that the minimum current sourced by the transistors are larger than the threshold current of the VCSEL.

On the other hand, the amount of modulation current sourced by M5 and M6 is determined by the minimum voltage level available at the inputs of the current steering stage. This minimum voltage level is given by

$$V_{\min} = I_{D8}\left(r_{DS4} \,||\, r_{DS2}\right) \approx I_{D8} r_{DS4} \qquad (2.26)$$

Since I_{D8} is set by the DC gate voltage of M10, V_{bias} directly affects the value of V_{min}, and indirectly controls the amount of modulation current provided to the VCSEL. In addition, I_{D8}, M3 and M4 are carefully designed such that V_{min} is not too small and switches M5 and M6 into triode mode.

M5 and M6 are designed with large transistors in order to drive the large amount of current required by the VCSEL. In addition, larger M5 and M6 also mean faster current switching at the output of the laser driver. However, larger M5 and M6 will degrade the frequency response of the pulse shaping stage, as they introduce larger parasitic capacitance. Careful design of the transistors' sizes of M5, M6, M1, and M2 is crucial to optimize the laser driver's speed performance. A compensation resistor, R_{com}, is also placed between the output of the laser driver and bond-wire to minimize signal ringing.

A same circuit setup as in Figure 2-12 of section 2.5.1.2 is used to simulate the fast-discharge laser driver. The transient response of the current supplied to the VCSEL, at 2Gbps, is shown in Figure 2-15. The current swings between 2.1mA and 11.3mA, with a rise-time of 211ps and fall-time of 249ps. The static power consumption is 24.7mW. According to this simulation result, the fast-discharge laser driver has a shorter current signal fall time compared to a current steering laser driver.

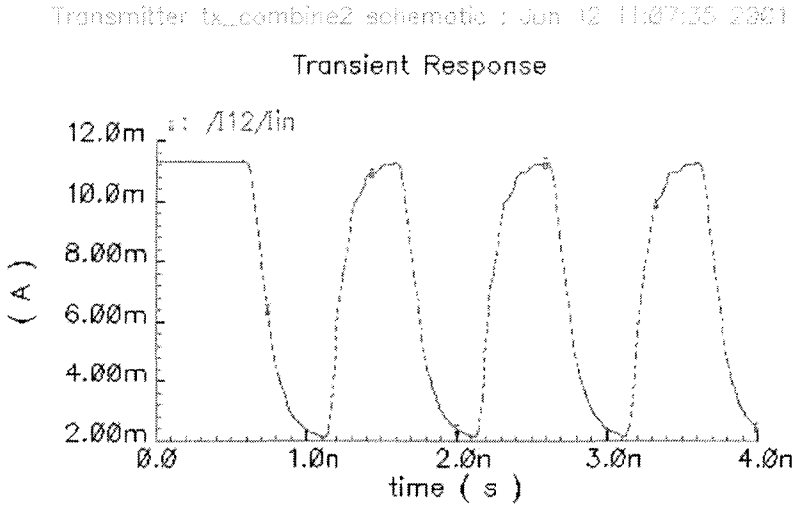


Figure 2-15: Transient response of the current provided to VCSEL by the fast-discharge laser driver, at 2Gbps.

2.5.3 Push-Pull Laser Driver

The previous two laser driver designs apply a differential pair to steer current into the VCSEL. Both designs apply a mechanism to source current into the VCSEL during a signal's rising edge, and "let" the VCSEL discharge current during a signal's falling edge. Hence, the output current of the laser drivers has relatively slow fall-time.

A push-pull laser driver is designed to source (or push) current into the VCSEL during a rising edge, and sink (or pull) current from the VCSEL during a falling edge

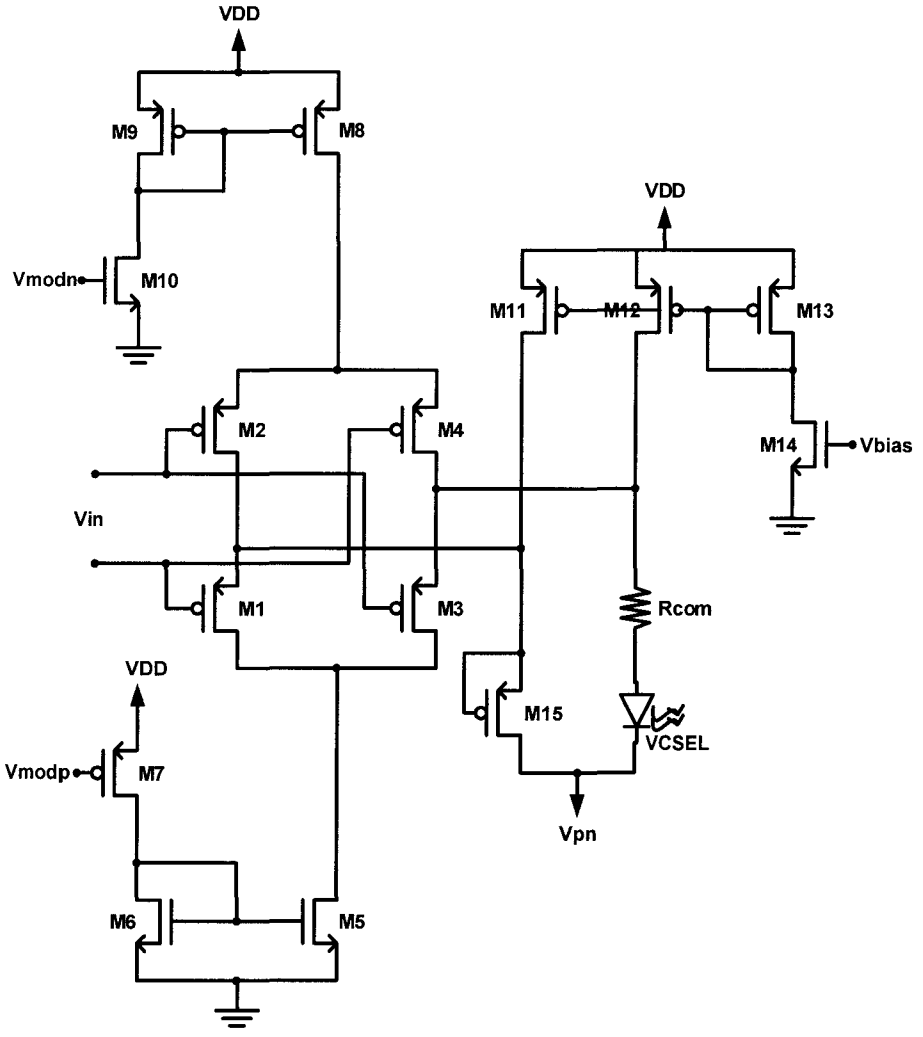


Figure 2-16: Schematic of a push-pull laser driver.

[36]. By applying both push-pull mechanisms, the rise-fall time of the laser driver's output current can become comparably short.

Figure 2-16 shows a circuit schematic of the push-pull laser driver. The gate of the transistors M3 and M4 are connected to a complementary pair of input signals. The input signals are rail-to-rail digital signals. When M3 is switched on, it will pull an amount of current equal to that sunk by M5, away from the VCSEL. When M4 is switched on, it will push an amount of current equal to that sourced by M8, into the VCSEL. The current mirror formed by M12, M13, and M14 provides a constant DC biasing current to the VCSEL. It is designed such that the difference between the biasing current and the current sunk by M5 is larger than the threshold current of the VCSEL; and the sum of the biasing current and the current sourced by M8 is the maximum amplitude of the modulation current. M1 and M2 form the complementary circuit to M3 and M4, and M11 is the complementary to M12. Again, a compensation resistor, R_{com}, is placed between the output of the laser driver and bond-wire to minimize signal ringing.

One drawback of this design is that the laser driver has 4 transistors in cascode (M5, M3, M4, and M8) and hence requires larger voltage supply for proper biasing of the transistors. The VCC voltage supply of 3.3V is used for this design, in stead of 1.8V. Hence, a digital level converter (section 2.4.3) is inserted at the decision stage, to convert the 0V and 1.8V digital levels to the 0V and 3.3V digital levels.

A circuit setup similar to Figure 2-12 of section 2.5.1.2 is used to simulate the push-pull laser driver. The transient response of the current provided to VCSEL, at 4Gbps, is shown in Figure 2-17. The current swings between 3.1mA to 9.8mA, with a rise-time of 73ps and a fall-time of 64ps. The static power consumption is 54.2mW. This

simulation shows that a push-pull laser driver has superior current signal rise-fall time performance over the previous two designs, at the expense of higher static power consumption.

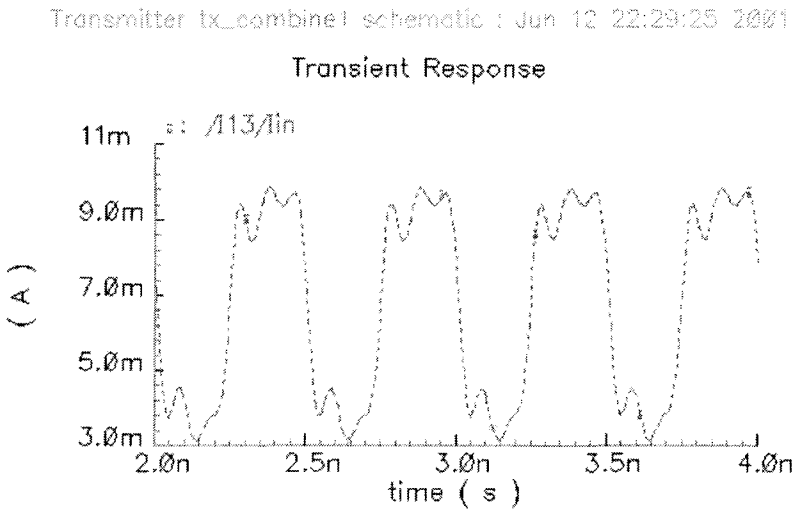


Figure 2-17: Transient response of the current provided to VCSEL by the push-pull laser driver, at 4Gbps.

2.6 Conclusion

Three designs of laser driver are presented along with simulation results. The fast-discharge laser driver and the push-pull laser driver were used in the implementation of an optical transmitter chip fabricated by CMC. Aside from the laser drivers, the optical transmitters implemented include the preamplifier and the decision stage. Simulation results show that the optical transmitter could achieve a maximum data bit-rate of 4Gbps.

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Chapter 3: Optical Receiver

3.1 Introduction

To date, optical receiver design has received quite a lot of research attention. There have been a large number of publications related to optical receiver design. In general, these publications involve two major types of optical receivers, distinguished by their application, and design requirements [1]. These are optical receivers that are designed for long haul, fiber-based telecommunication networks [2], [3]; and optical receivers that are designed for OE-VLSI interconnects [4], [5].

The design of optical receivers for OE-VLSI interconnects is somewhat different from the optical receivers designed for long haul telecommunication networks, due to differences in design requirements. Telecommunication optical receivers require high sensitivity, and the circuit designs are usually optimized at the expense of chip area and power consumption. In telecommunication optical receivers, extra circuits such as clock recovery circuitry, automatic gain control, and automatic offset control are often required. On the other hand, OE-VLSI optical receivers are designed to be as simple as possible. The designs are optimized for low power consumption and small chip area. It is only possible to integrate thousands of receivers onto a single VLSI chip, provided each receiver consumes power in the order of a few milliwatts and occupies very small chip area.

In this chapter, the author will discuss the design of OE-VLSI optical receivers. In section 3.2, the architecture of an optical receiver is introduced. In section 3.3, the preamplifier stage of an optical receiver is discussed. Two designs are presented: a

common gate preamplifier, and a current mirror preamplifier. In section 3.4, the author discusses the design of the post-amplifier stage, followed by the design of the decision stage in section 3.5. The design of the receivers' output driver is presented in section 3.6. In section 3.7, the simulation results of the receivers are presented.

These optical receiver circuits are designed and implemented in 0.18μm CMOS technology. Implementation of optical receivers in CMOS technology allows cost effective integration of such circuit in a CMOS VLSI chip. The receivers are designed to operate at a maximum data bit rate of 2Gbps.

3.2 Architecture

Figure 3-1 shows a block diagram representing the architecture of an optical receiver circuit. The optical receiver is divided into a preamplifier stage, a post-amplifier stage, a decision stage and an output driver. The input of the receiver is connected to a photodiode (PD) which converts intensity-modulated optical signal into photocurrent. On the other hand, the differential output signals will go off-chip, through a printed circuit board (PCB) to a signal analyzer.

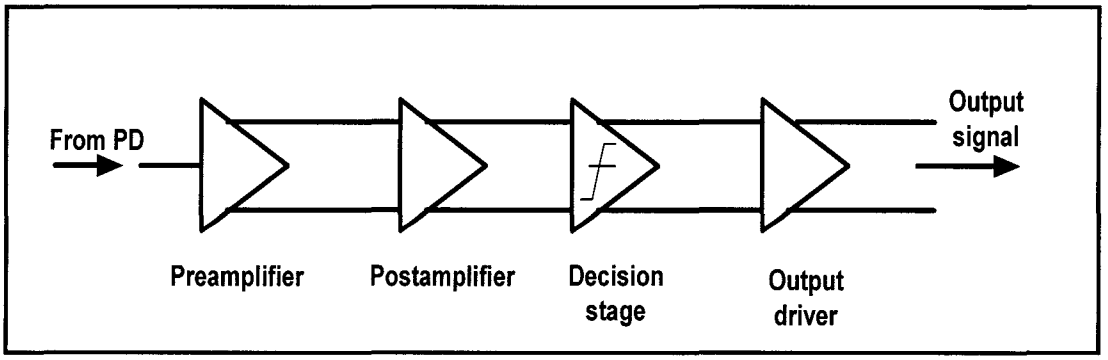


Figure 3-1: A block diagram showing the architecture of an optical receiver circuitry.

Since the input signal to the receiver is a current signal, the preamplifier will have to 1) convert the current signal to a voltage signal, and 2) amplify the signal. Hence, the preamplifier of an optical receiver is often known as a transimpedance amplifier. The post-amplifier will further amplify the voltage signal from the preamplifier, so that the amplitude of the signal is greater than the undefined region of the decision stage. The combination of the preamplifier and the post-amplifier stages provide high-bandwidth, high-sensitivity and low noise performance to the optical receiver. The decision stage will further amplify the signals from the post-amplifier to rail-to-rail logic levels of ones and zeros.

The signal received will be sent off the receiver chip to a PCB. Thus, an efficient signal driver is necessary to drive the microstrip lines that will carry the output signals on the PCB. A low-voltage differential signals (LVDS) design is used for the output driver as it provides low power dissipation, low noise, and high-speed signal driving capability. The circuit design and the advantage of a LVDS driver will be discussed in further detail in this chapter.

3.3 Preamplifier

The preamplifier of an optical receiver receives current input and converts it into voltage signal. Thus, it is often referred to as transimpedance amplifier.

Designs of conventional transimpedance amplifier for optical receivers are illustrated in [2] and [5]. Figure 3-2 shows two examples of transimpedance amplifiers. Since the input of these circuits is connected to the gate of the transistor, these amplifiers have high input impedance.

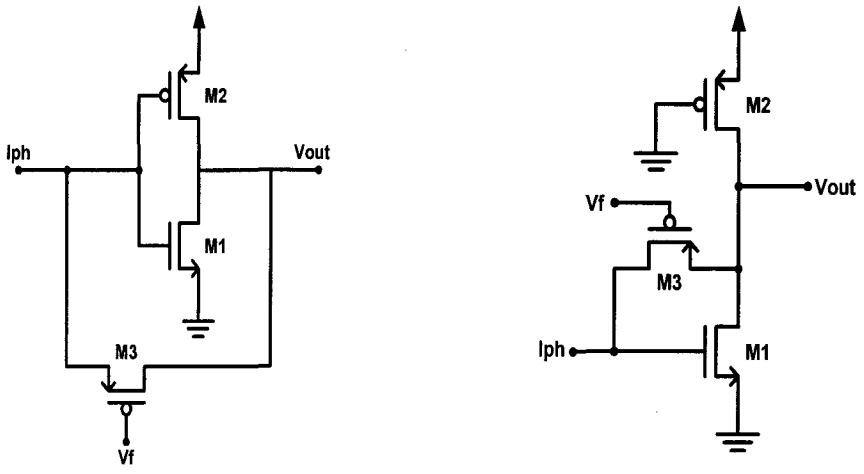


Figure 3-2: Examples of transimpedance amplifier with high input impedance.

Another class of design referred to as current-mode transimpedance preamplifier is presented in [6]-[11]. Since the input of these current-mode transimpedance preamplifiers is connected to either the source or the drain of a transistor, they have low input impedance. Such designs provide high bandwidth performance, and due to the low input impedance, the parasitic capacitance of photodiode has virtually insignificant effect in determining the bandwidth of the amplifier.

In the following subsections, the author presents two different current-mode transimpedance preamplifiers designed and implemented in 0.18μm CMOS technology.

3.3.1 Common Gate Preamplifier

Figure 3-3 shows a schematic of the common gate preamplifier implemented in the optical receiver designed by the author. M3, M4 and M5 form a simple current mirror that provides the biasing for the amplifier. M1 is the common gate amplifier, with its gate

connected to a fixed DC biasing. The input current signal flows into the source of M1, and the drain of M1 is connected to M2, which acts as an active load, biased in triode region.

Since the input is at the source of the transistor, a common gate amplifier does not suffer from the Miller's effect [12], as a common source amplifier does. This means that it has smaller input capacitance compare to a common source amplifier. The input resistance is the inverse of the transconductance of M1, $1/g_{m1}$, which has a small value and can be minimized by using a large transistor size for M1.

The transimpedance gain of the amplifier is $\sim r_{DS2}$. The exact value of the transimpedance gain will be smaller than r_{DS2} due to the finite resistances at the source of M1 and the drain of M5. Since M2 is biased in triode region,

$$r_{DS2} = \left[\mu_p C_{OX} \left(\frac{W}{L} \right)_2 \left(|V_{GD2}| - V_t \right) \right]^{-1} \tag{3.1}$$

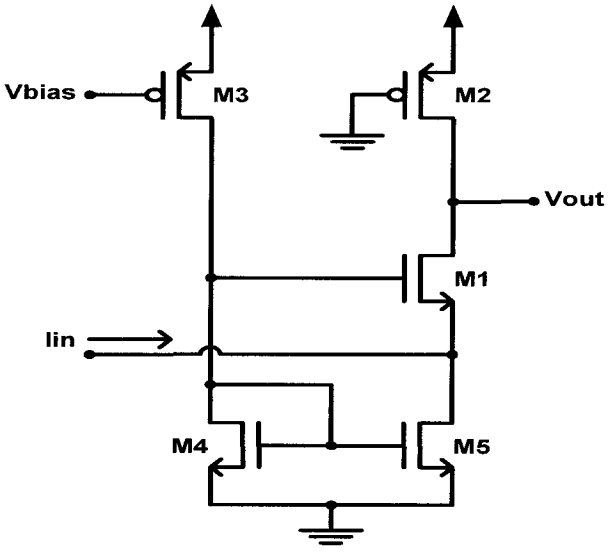


Figure 3-3: Schematic of a common gate preamplifier.

According to equation (3.1), r_{DS2} reduces for a larger transistor M2. In other words, choosing a smaller transistor for M2 can increase the transimpedance gain of the common gate preamplifier.

The common gate preamplifier has two poles, one at the input node and the other at the output node. The frequency of the input pole is approximately given by

$$\omega_{p1} \approx \left[\left(\frac{1}{g_{m1}}\right)\left(C_{gs1} + C_{gd5} + C_{pd}\right)\right]^{-1}$$

$$\approx \left[\frac{1}{g_{m1}} C_{pd}\right]^{-1} \qquad (3.2)$$

where C_{pd} is parasitic capacitance of the photodiode. Meanwhile, the frequency of the output pole is

$$\omega_{p2} \approx \left[r_{DS2}(C_{gd1} + C_{gd2} + C_L)\right]^{-1} \qquad (3.3)$$

where C_L is the load capacitance the output node is connected to. Since $1/g_{m1}$ has a small value, ω_{p2} is dominant. According to equation (3.3), the pole frequency is high if r_{DS2} is small. Hence, there is a design trade-off between the transimpedance gain and the frequency performance.

The common gate preamplifier circuit in Figure 3-3 is simulated with a photodiode modeled by a 0.4pF capacitance. The frequency response of the circuit is shown in Figure 3-4. The circuit has a maximum transimpedance gain of 31.48 dBΩ, and 3-dB frequency of 8.4GHz. The small transimpedance gain and high frequency response of the preamplifier is due to the small resistance, r_{DS2}, across M2 that is operating in triode region.

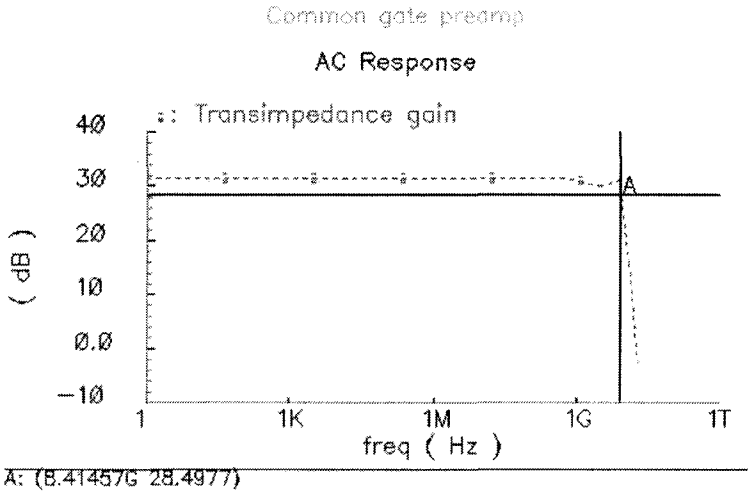


Figure 3-4: Frequency response of the common gate preamplifier (shown in Figure 3-3).

3.3.2 Current Mirror Preamplifier

Figure 3-5 shows a schematic of the current mirror preamplifier implemented in the optical receiver designed by the author. This circuit is similar to the circuit presented by *J. J. Chang, et al*, in [11].

Note that the preamplifier in Figure 3-5 has a single input and differential output. M1 and M2 form a current mirror, while M3 and M4 form another complementary pair of current mirror. M5-M10 form cascode current mirrors that supply bias current to the current mirrors formed by M1-M4. M11 and M14 set the biasing for the current mirrors. The input of the current mirror formed by M1 and M2 is connected to the photodiode, which provides the input photocurrent. An equal but opposite amount of signal current will flow in the current mirror formed by M3 and M4, provided the circuit is designed symmetrically. The outputs of the current mirrors are connected to the active loads M12 and M13 respectively.

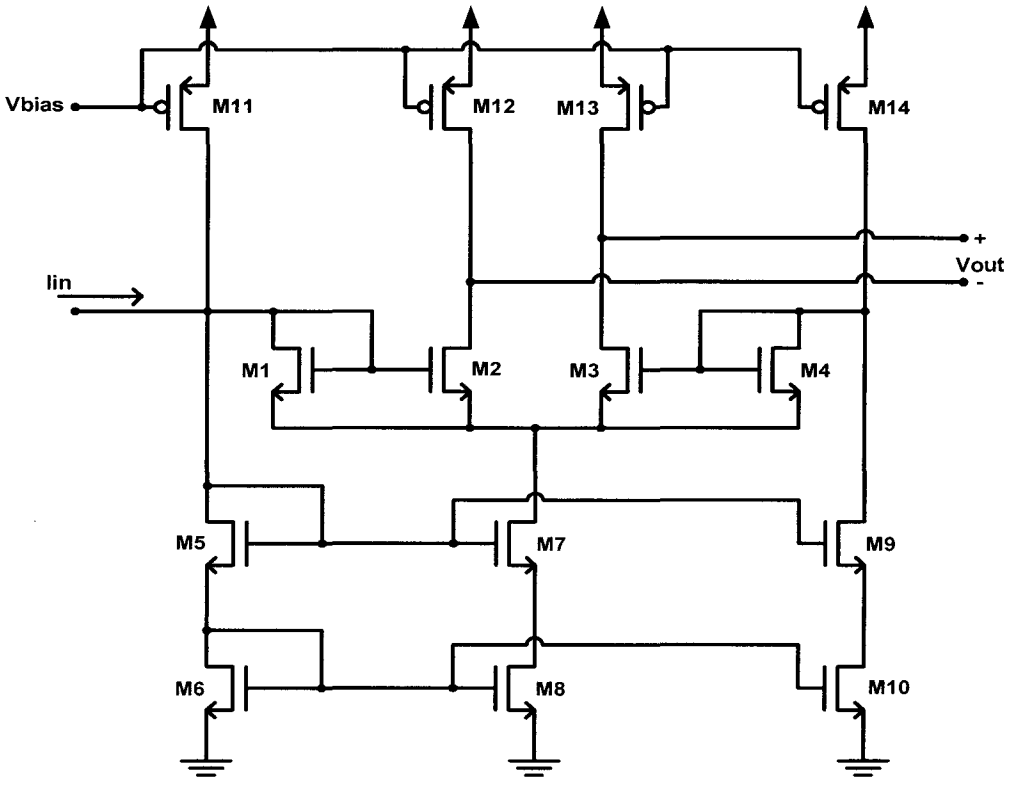


Figure 3-5: Schematic of a current mirror preamplifier.

Since M1 and M2 form a simple current mirror, the current gain of the circuit is the ratio of the transistor's size, W_2/W_1 . The transimpedance gain of the preamplifier is

$$\frac{V_{out}}{I_{in}} = 2\left(\frac{W_2}{W_1}\right) r_{DS12,13} \tag{3.4}$$

where

$$r_{DS12,13} = r_{DS12} = r_{DS13} = \frac{V_A}{\frac{1}{2} k_p \left(\frac{W}{L}\right)_{12,13} \left(V_{GS12,13} - V_t\right)^2} \tag{3.5}$$

The factor of two in the expression (3.4) is due to the fact that the preamplifier has single-ended input and differential output. According to equation (3.4) and (3.5), the

transimpedance gain of the current mirror amplifier can be improved by 1) increasing the M2 to M1 transistor's size ratio, 2) decreasing the size of M12 and M13, and 3) decreasing the gate-source voltage difference of M12 and M13.

The high-speed performance of the current mirror preamplifier can be studied by analyzing the pole frequencies of the circuit. The input pole of the circuit is located at a frequency approximated by

$$\omega_{p1} = \left[\frac{1}{g_{m1}}\left\{C_{pd} + C_{gs1} + C_{gs2} + C_{gd2}(1 - A_V)\right\}\right]^{-1}$$

$$\approx \left[\frac{1}{g_{m1}}\left\{C_{pd} + C_{gd2}(1 - A_V)\right\}\right]^{-1} \qquad (3.6)$$

$1/g_{m1}$ is the input resistance of the preamplifier, while C_{pd} is the capacitance of the photodiode and C_{gd2} is the gate-drain capacitance of transistor M2. Note that in this design, the preamplifier suffers from Miller effect, with A_V the voltage gain between the gate and the drain of M2. The expression for A_V is $-g_{m2}r_{DS12}$. Meanwhile, the output pole frequency is approximately

$$\omega_{p2} = \left[(r_{o2} \parallel r_{DS12})C_L\right]^{-1} \qquad (3.7)$$

where C_L is the load capacitance connected to the output node of the circuit. By comparing the expressions of transimpedance gain and pole frequency for the current mirror and the common gate preamplifiers, it can be concluded that the current mirror preamplifier could achieve a higher transimpedance gain, but the common gate preamplifier has a better frequency performance.

The circuit in Figure 3-5 is simulated with a photodiode modeled by a 0.4pF capacitor. Figure 3-6 shows the frequency response of the circuit. The maximum transimpedance gain is found to be 44.2 dBΩ, and the 3-dB frequency is 1.6GHz.

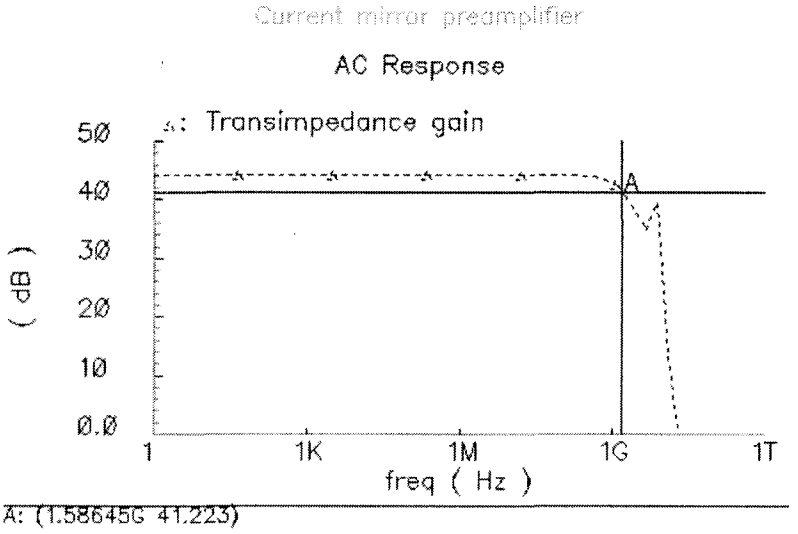


Figure 3-6: Frequency response of the current mirror preamplifier.

3.4 Post-Amplifier

The post-amplifier provides additional signal gain, and thus improves sensitivity of the optical receiver. It is designed to amplify the voltage signal received from the preamplifier to a peak-to-peak voltage swing that is greater than the undefined region of the decision stage. This is to ensure proper operation of the decision stage, as mentioned in chapter 2. In this section, the design of a fully differential amplifier, a single input differential output (SIDO) amplifier, and an offset control circuit is presented.

3.4.1 Fully Differential Post-Amplifier

Figure 3-7 shows a schematic of the post-amplifier implemented in the optical receiver designed by the author. It consists of three fully differential amplifier stages, implemented with transistors M1-M13. The first stage is a gain-controlled fully differential (GCFD) amplifier, which is discussed in section 2.3.1. The gain of the amplifier is adjustable by varying the gate voltage of M7, through an external DC voltage source, V_{gc}. The analysis performed in section 2.3.1 for the gain and frequency response of the amplifier applies here. The second and the third amplifier stages have similar circuit topology as the first stage. The only difference is that the triode-biased transistor that appears across the positive and negative outputs of the first amplifier stage does not exist in the second and the third amplifier stages. Thus the analysis performed in section 2.3.1 still applies to these two amplifier stages.

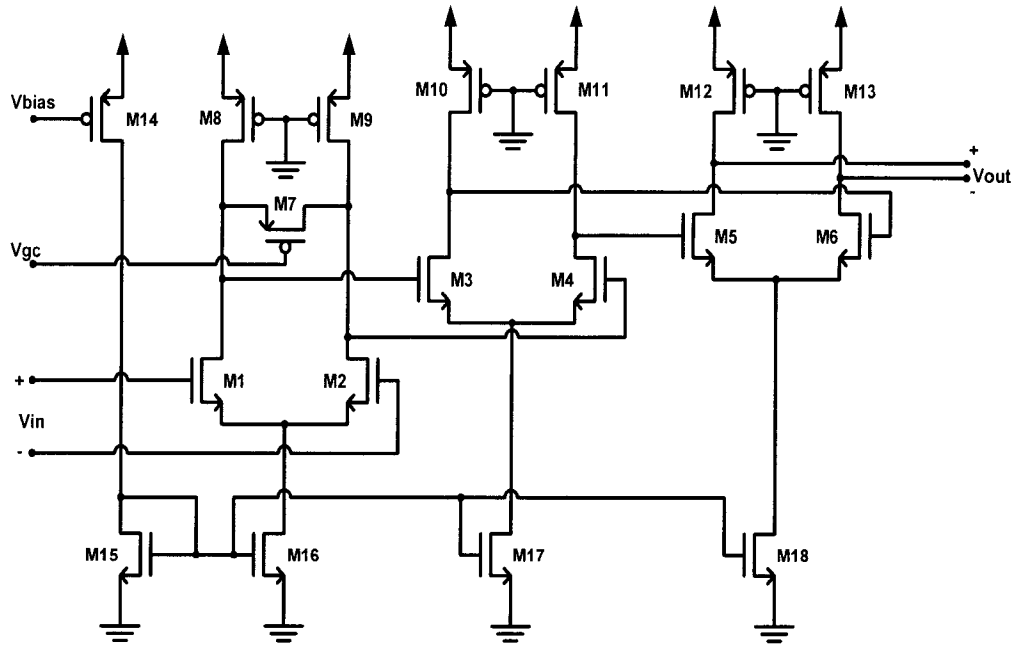


Figure 3-7: Schematic of the fully differential post-amplifier.

Figure 3-8 shows the frequency response of the post-amplifier for different gain control voltage (between 0 to 0.6V). The maximum signal gain of the circuit varies from 31.5 dB to 39.9 dB. The 3-dB frequency varies between 1 GHz to 0.6 GHz. The frequency response of the post-amplifier can be improved if a folded-cascode design is used.

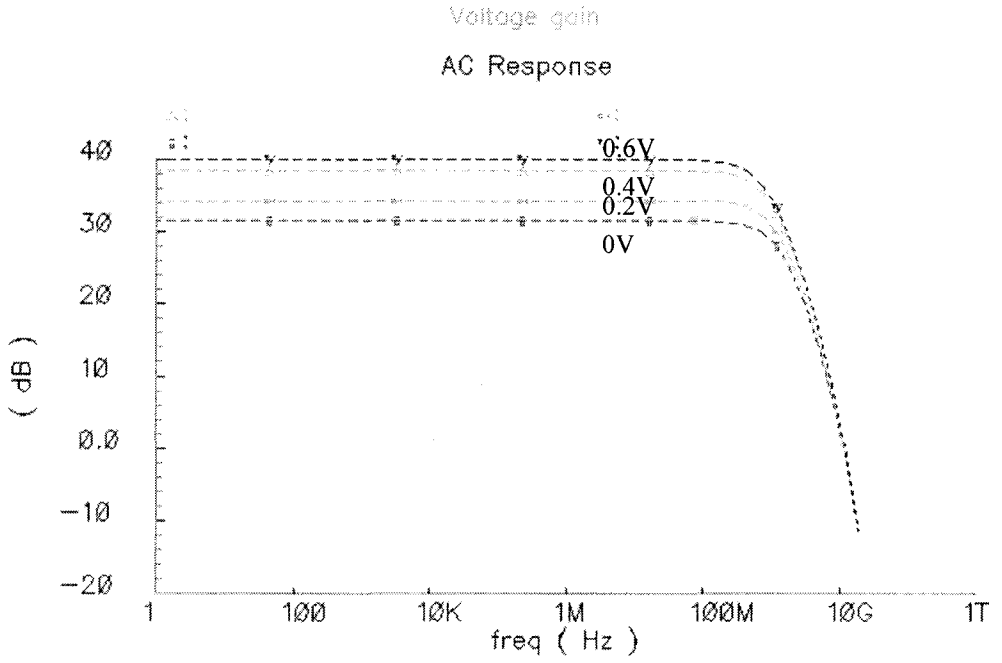


Figure 3-8: Frequency response of the post-amplifier for V_{gc}= 0V, 0.2V, 0.4V, and 0.6V.

3.4.2 Single Input Differential Output (SIDO) Amplifier

Since the common gate preamplifier (section 3.3.1) has a single-ended output, a single input differential output (SIDO) amplifier is implemented to convert the single-ended signal to a differential-ended output. Figure 3-9 shows a schematic of the SIDO implemented in the optical receiver design.

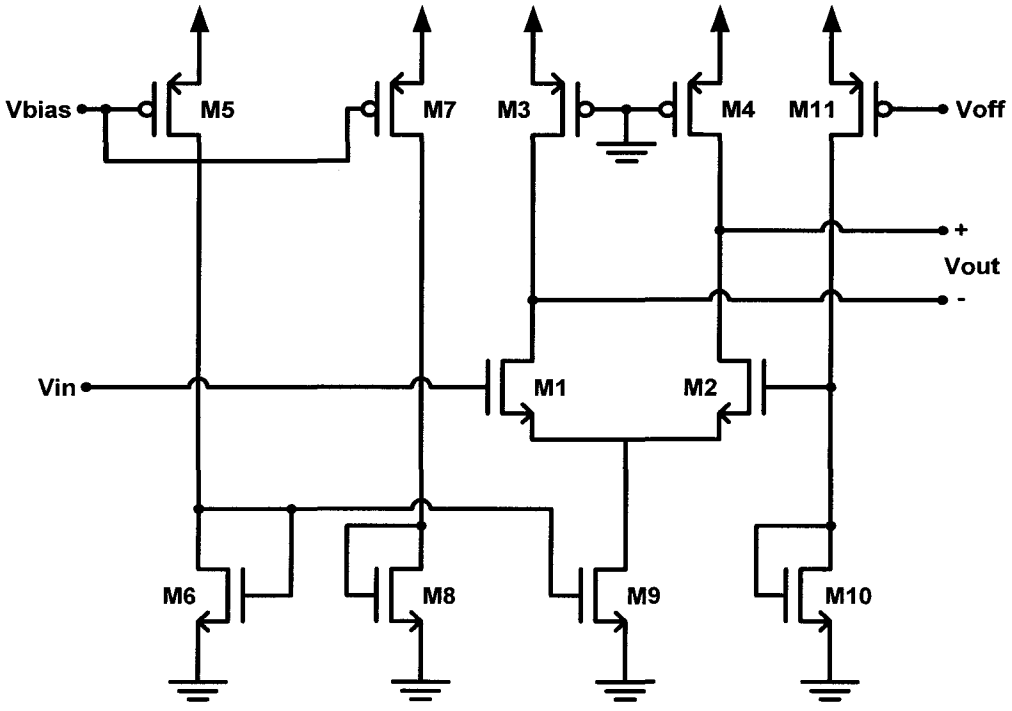


Figure 3-9: Schematic of a single input differential output (SIDO) amplifier.

In Figure 3-9, the transistors M1–M4 form a gain stage similar to a fully differential amplifier. In this case, one input terminal (at the gate of M1) is connected to the input signal, whilst the other (at the gate of M2) is connected to a fixed DC bias. The DC bias at the gate of M2 is controlled indirectly by an external voltage source, V_{off}. Another external voltage source, V_{bias}, is used to set the biasing points of the amplifier.

The SIDO amplifier is simulated using *SPECTRE*. The frequency response of the amplifier is shown in Figure 3-10. The maximum voltage gain (V_{out}/V_{in}) obtained is 15dB, and the 3-dB frequency is 4.3GHz.

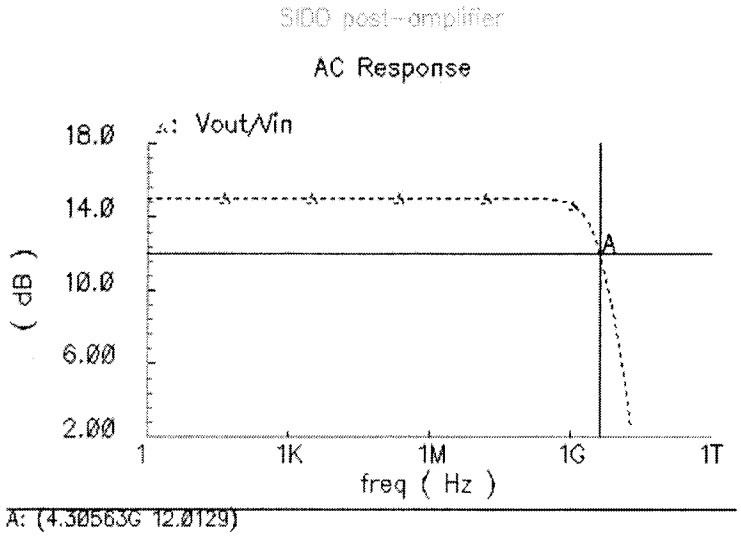


Figure 3-10: Frequency response of the SIDO amplifier.

3.4.3 Offset Control Circuitry

The purpose of an offset control circuitry is to set the average voltage level of the post-amplifier's output signal. The circuit has to set the average value of the output signal from the post-amplifier to the threshold value of the decision stage that succeeds. This helps to ensure that the output signal from the decision stage has a 50% duty cycle. Since the optical power received by the photodetector may vary, the average value of the received signal may vary too. Thus, it is desirable to be able to readjust the offset level of the signal, before reaching the decision stage.

Figure 3-11 shows a schematic of the offset control circuitry. It is implemented using a pair of simple current mirrors. The principle behind the operation of the circuit has been explained in section 2.3.2. For the circuit in Figure 3-11, the offset voltage at the nodes V_{out+} and V_{out-} can be controlled by external voltage sources V_{off+} and V_{off-} independently.

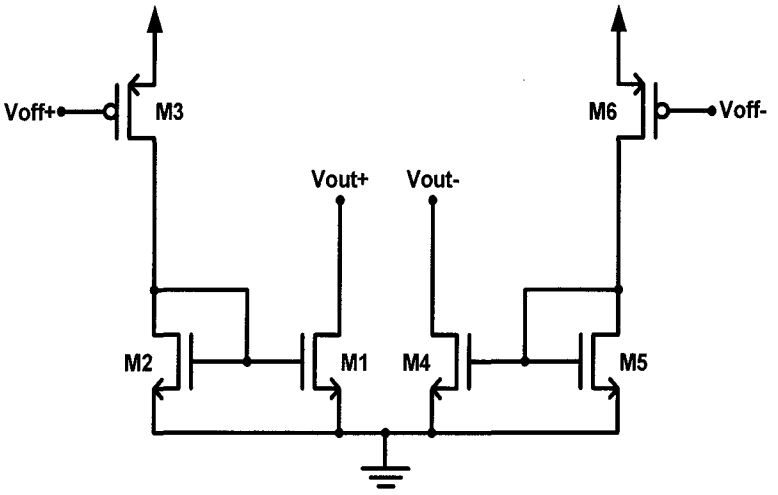


Figure 3-11: Schematic of an offset control circuitry.

3.5 Decision Stage

Detail discussions about the design of decision stage have been presented in section 2.4. Figure 3-12 shows a schematic of the decision stage implemented in the optical receiver. Note that only half of the fully differential circuitry is shown in the figure.

The decision stage circuitry in Figure 3-12 is composed of five inverter stages, and a shunt feedback connected inverter constructed by M3 and M4. The purpose of this shunt feedback connected inverter is to broaden the linear region of the first inverter stage [13]. A broader linear region at the input of the decision stage offers a higher tolerance to offset in the post-amplifier's average output signal. This also means a higher dynamic range for the optical receiver.

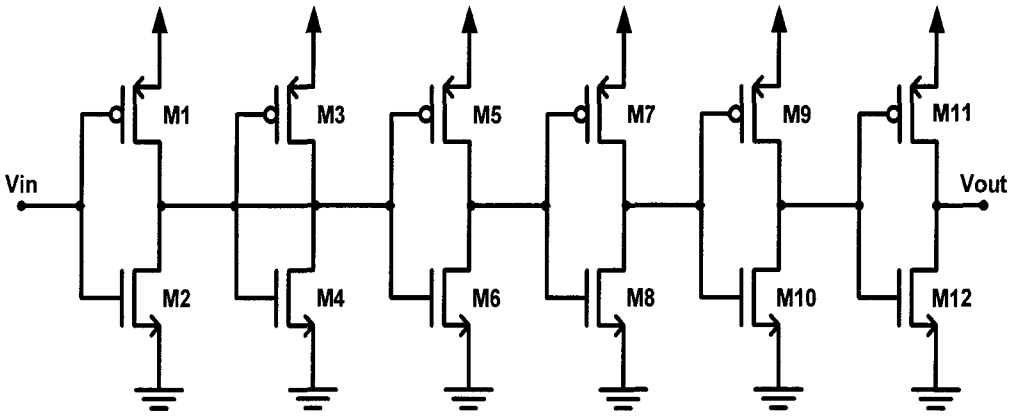


Figure 3-12: Schematic of the decision stage implemented for the optical receiver.

The transistors M3 and M4 of the shunt feedback connected inverter operate in saturation and cut-off mode only, depending on the input signal. The output of the shunt feed connected inverter follows the input. To find an expression for the voltage gain of the combination of the first and the second stage, the transistors M1–M4 are considered in saturation mode. A small signal model for the circuit in the first two stages, as shown in Figure 3-13, can be used to derive the gain within the linear region. It can be derived from the figure that

$$\left|\frac{V_{out}}{V_{in}}\right| = (g_{m1} + g_{m2})\left(r_{o1} \parallel r_{o2} \parallel r_{o3} \parallel r_{o4} \parallel \frac{1}{g_{m3}} \parallel \frac{1}{g_{m4}}\right)$$

$$\approx \frac{(g_{m1} + g_{m2})}{(g_{m3} + g_{m4})}$$

$$= \frac{(W/L)_{stage1}}{(W/L)_{stage2}} \qquad (3.8)$$

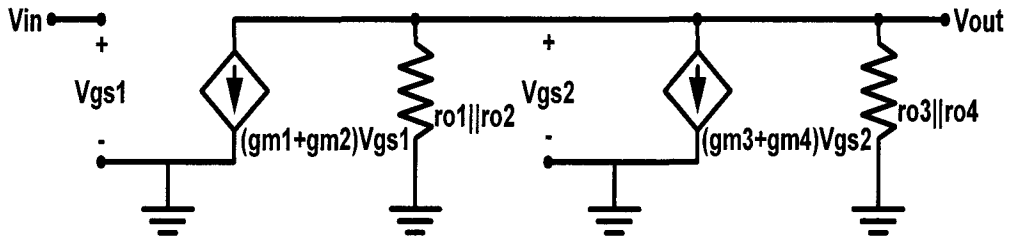
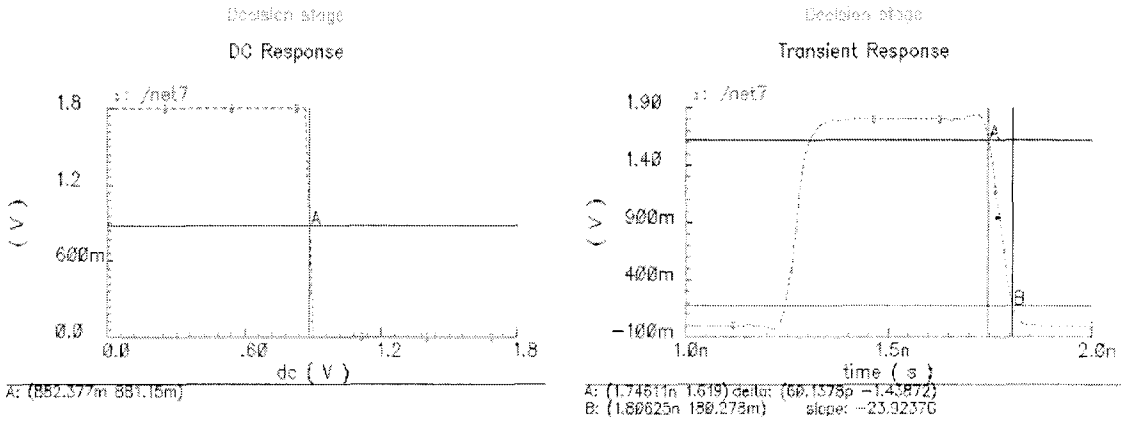


Figure 3-13: Small signal model of the first and second inverter stage in Figure 3-12.

Thus, according to equation (3.8), the voltage gain within the linear region of the first two inverter stages is the ratio of the transistors' size of the first stage to the transistors' size of the second stage. For the reason, the shunt feedback connected inverter has smaller transistors than its preceding stage. Note that the subsequent inverter stages have transistors that are twice as large as their preceding stage, as explained in section 2.4.2.

The decision stage circuit of Figure 3-12 is connected to a capacitive load of 40fF and simulated at 2Gbps. Figure 3-14a) shows its voltage transfer characteristic, and figure 3-14b) shows its transient response. The switching threshold of the decision stage is marked by marker 'A' in Figure 3-14a), which is 0.88V. The rise time and fall time of the output signal is found to be 60ps when a capacitive load of 40fF is connected to its output.



a) b)

Figure 3-14: a) Voltage transfer characteristic, and b) transient response of the decision stage circuit.

3.6 Output Driver

The output driver of the optical receivers is responsible for sending the received signal off-chip. The design of the output driver is critical since it must be capable of driving huge capacitive load at high data bit-rate (>2Gbps), while consuming as little power as possible.

A low-voltage differential signal (LVDS) output driver design is used in the design of the high-speed optical receivers. The two main properties of a LVDS design are self-explained by its name: 1) low voltage swing and 2) differential signal. IEEE Standard Board specifies a minimum output differential voltage of 250mV, and a maximum of 400mV for a LVDS driver [14]. With the differential signals terminated in a 100Ω resistor, the maximum amount of current supplied by the driver is 4mA. This gives a maximum power consumption of only 1.6mW.

A differential signaling scheme is less susceptible to externally generated common-mode noise. On the other hand, differential signal generates equal and opposite currents that cancel electromagnetic field. This dramatically reduces electromagnetic emissions. A LVDS driver circuit consumes a constant amount of current (except a little spike during switching of the circuit), which minimizes the power supply noise.

Figure 3-15 shows a schematic of a LVDS driver implemented in the optical receiver designed by the author. It has differential input and differential output. When V_{in+} is positive and V_{in-} is negative, M1 and M4 will be switched on while M2 and M3 off. Current will be sourced by M1, leaving node V_{out+}, and sunk by M4, entering from node V_{out-}. When the polarity of the input signal is changed, the current will flow in an opposite direction. The transistors M5-M10 form two simple current mirrors that supply

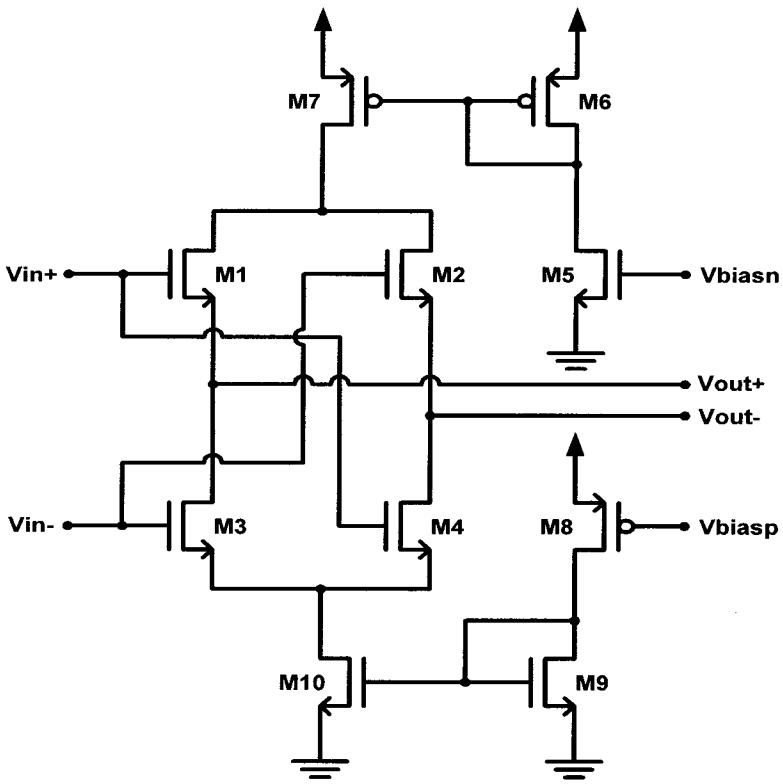


Figure 3-15: Schematic of a LVDS driver implemented in the optical receivers.

the source/sink currents. The two DC biasing voltages V_{biasp} and V_{biasn} are adjustable externally to control the amount of current sourced/sunk by the driver.

In order to simulate the performance of the LVDS driver, the circuit is simulated with a circuit model of the CFP80TF printed circuit board's microstrip lines, provided by CMC. The parasitic capacitance and inductance of the bond wire and the bonding pad are also included. The differential signal is terminated with a 100Ω resistor. Figure 3-16 shows the output waveforms V_{out+} and V_{out-} for a rail-to-rail (0V-1.8V) input signal at 2Gbps. The simulation result shows symmetric output signals that have voltage swing of 400mV.

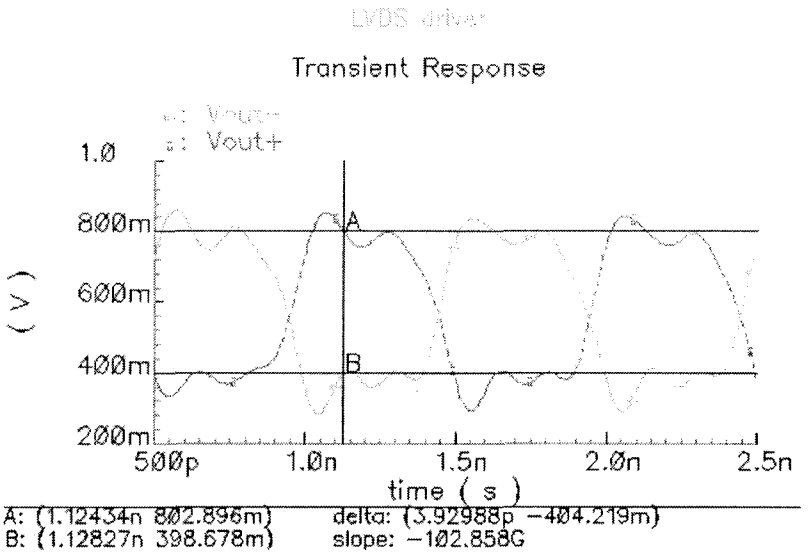


Figure 3-16: Output waveforms of the LVDS driver, simulated at 2Gbps. The markers measure the output voltage swing at 400mV.

Before leaving this section, the author would like to refer to several other LVDS driver designs. *E. Hazen* presented a LVDS driver circuit similar to the circuit in Figure 3-15 in [15]. *T. Gabara, et al*, presented a LVDS I/O buffer with a controlled reference circuit, which maintains a constant output voltage and current level of a LVDS driver,

over process, voltage supply, and temperature variations, in [16]. *T. Knight and A. Krymm* showed a self-terminating low-voltage swing output driver in [17], which could be modified for the implementation of a LVDS driver. With a self-terminating output driver, the signal ringing due to impedance mismatch can be greatly reduced. Although the circuits presented in [16] and [17] are more robust, they are more complicated compared to the circuit presented in [15].

3.7 Optical Receiver Circuits Simulation

Two different optical receivers, one implemented with common gate preamplifier and the other with current mirror preamplifier, are implemented in 0.18μm CMOS technology. The circuits are simulated in *SPECTRE*, and the simulations include the effect of bond-pads' and bond-wires' parasitic elements, the PCB's microstrip lines, and most importantly, parasitic elements of the photodiode.

The characteristics of the photodiode used in an optical receiver will affect the circuit's performance. Table 3-1 lists some of the important characteristics of the photodiode used in the implementation of the optical receivers, which are obtained from the datasheet provided by *EMCORE Corporation* [18], [19]. Figure 3-17 shows the circuit model of the photodiode used in the simulations. Note that for the purpose of the simulations, the maximum values for the capacitance and dark current are used in the model.

Characteristics	Typical value	Unit
Responsivity @ 850nm	0.5	A/W
Rise time	32	ps
Fall time	75	ps
Capacitance	0.4	pF
Dark current @ -1.6V	0.5	nA
Active area	70	μm

Table 3-1: Characteristics of the photodiode provided by *EMCORE Corporation* [19].

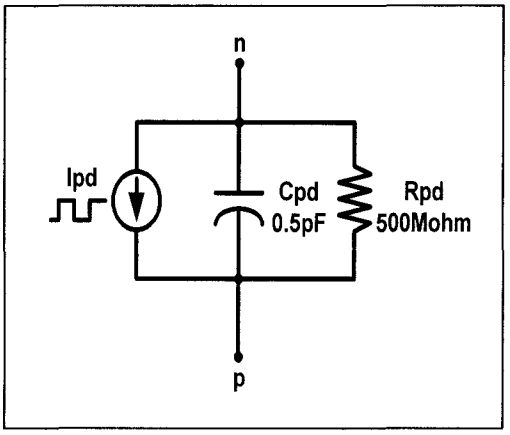
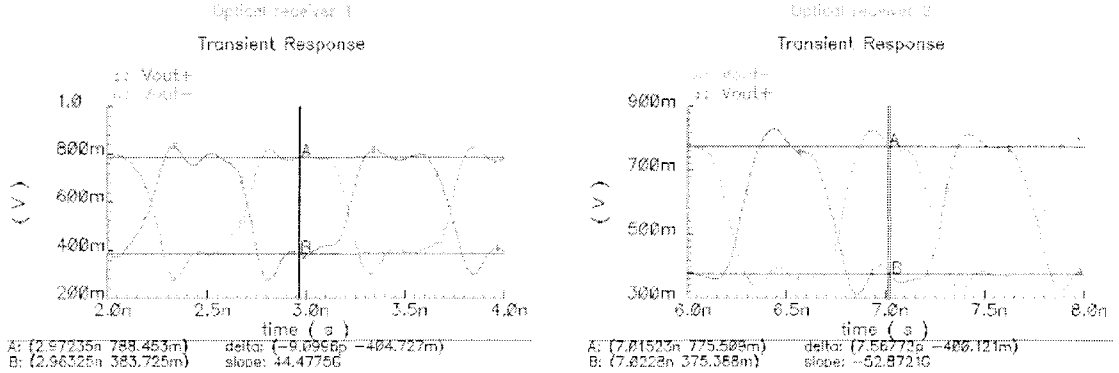


Figure 3-17: Circuit model of the photodiode used in optical receiver simulations.

Figure 3-18 shows the simulation results for the two optical receivers. Figure 3-18a) shows the output waveform of the receiver that is designed with a common gate preamplifier. Figure 3-18b) shows the output waveform of the receiver that is designed with a current mirror preamplifier. Both receivers are simulated at a data bit rate of 2Gbps, using a 2.5μA to 25μA current swing as the input photocurrent. Assuming a photodiode responsivity of 0.5A/W, the corresponding received optical power is 50μW, or –26dBm. The markers on the figures show that the amplitude of the LVDS output signal of the optical receivers are ~400mV. According to the simulations, the optical

receiver with a common gate preamplifier consumes a static power of 17.53mW, and the optical receiver with a current mirror preamplifier consumes a static power of 14.4mW.



a) b)

Figure 3-18: Output waveform of the optical receivers designed with a) common gate preamplifier, b) current mirror preamplifier, at 2Gbps.

3.8 Conclusion

All four stages of an optical receiver circuitry are presented in this chapter. In section 3.3, two different designs of preamplifier stage are presented: common gate preamplifier and current mirror preamplifier. These circuits are implemented in 0.18μm CMOS technology. Simulation results of the optical receivers implemented with two different types of preamplifiers are presented. The simulation results show that the circuits are capable of handling digital data at 2Gbps.

3.9 References

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Chapter 4: Chip Layout, Packaging and Testing

4.1 Introduction

The optical transmitters and receivers discussed in the previous chapters are implemented in 0.18μm CMOS technology and fabricated by TSMC [1] through CMC [2]. In section 4.2, the author will present the layout of the transmitter and the receiver chips. The circuits and the features that are implemented on the chips will be discussed. The layout of the circuits is done according to the design rules specified in [3].

In high-speed operation, the performance of the chips will be affected by the packaging technique used. In section 4.2, several different packaging techniques will be discussed. The packaging technique used by the author to package the transmitter and the receiver chips will also be discussed.

In section 4.3, the author will describe the test procedure for the chips, and the test results will be presented. The results obtained will then be compared with the results from simulations and theoretical analysis.

4.2 Chip Layout

The optical transmitters and the optical receivers are implemented on two separate 0.18μm-CMOS chips. The transmitter chip has a dimension of 3.2mm × 1.3mm, and the receiver chip has a dimension of 3.2mm × 1.5mm. The transmitter chip has a total of 82 bond pads, and the receiver chip has a total of 84 bond pads.

As mentioned in the previous chapters, two different designs of transmitter circuitry and receiver circuitry are implemented. Thus, a total of four designs are implemented. The following subsections describe the features of the chips.

4.2.1 Design for Testability

Figure 4-1 shows the layout of the transmitter chip and Figure 4-2 shows the layout of the receiver chip. Each chip has two different designs of transmitters and receivers. For each design, three circuits are implemented. Thus, there are a total of six circuits on each chip. These circuits are clearly shown in Figure 4-1 and Figure 4-2. The prefixes txa- and txb- indicate the location of the transmitter circuitries and the prefixes rxa- and rxb- indicate the location of the receiver circuits.

Each transmitter circuit has a pair of differential inputs connected to the bond pads along the bottom perimeter of the chip. Each transmitter has an output connected to a bond pad located along the upper perimeter of the chip. On the other hand, each receiver circuit has input connected to a bond pad along the upper perimeter of the chip, and a pair of differential output connected to bond pads along the bottom perimeter of the chip. In order to test the circuits, test data is generated off the chip, and the output signal of the circuits can be observed on a data analyzer or oscilloscope off the bond pad(s) connected to the output(s) of the circuit. The third circuit of each design (txa3, txb3, rxa3 and rxb3) has extra connections from the inputs/outputs of intermediate stages to bond pads. This allows measurement of signals at intermediate stages of the circuits. Since the extra connections causes extra parasitic capacitance, these circuits are expected to have poorer frequency performance.

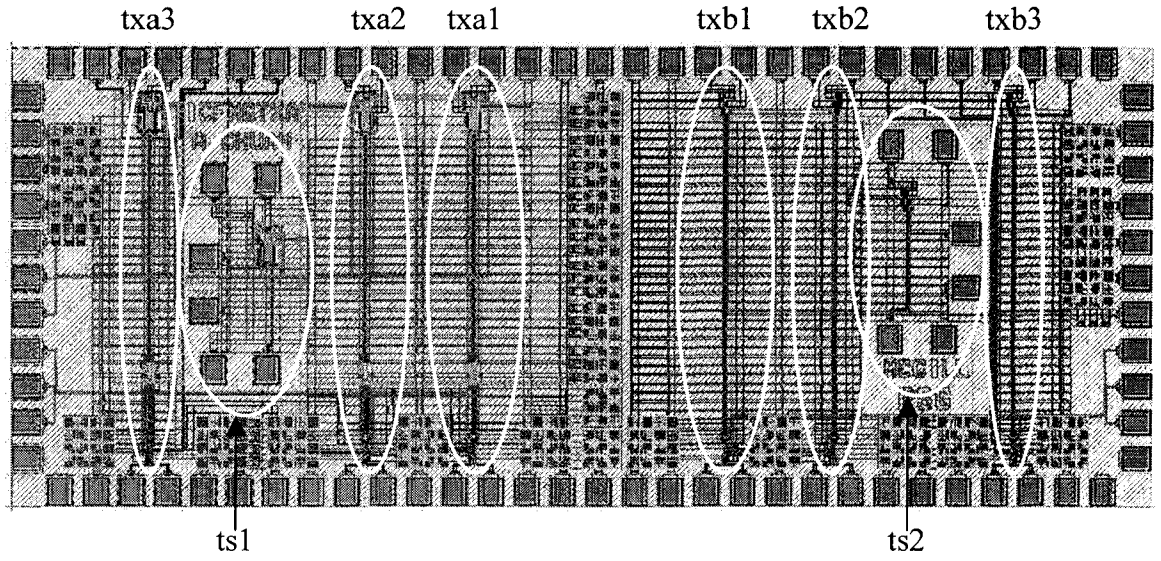


Figure 4-1: Layout of the optical transmitter chip.

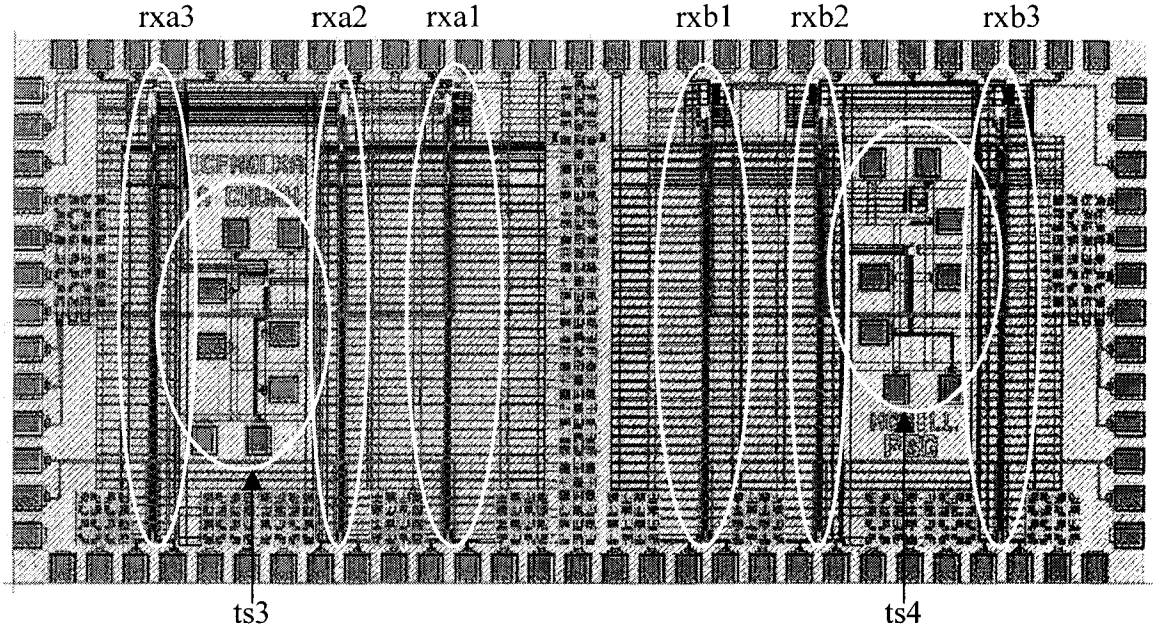


Figure 4-2: Layout of the optical receiver chip.

Additional test structures are implemented on the chips, which are indicated with the prefix ts-. These test structures consist of test circuits that are connected to probing pads that are designed to allow direct circuit probing with high-speed microprobes (ACP40) from *Cascade Microtech, Inc.* These microprobes have frequency range up to 40GHz [4].

4.2.2 Design for Noise Reduction

Two major sources of noise being considered are the substrate noise, and the simultaneous switching noise (SSN). The SSN is sometimes also referred as power-supply noise, ground bounce or ΔI noise. Capacitive crosstalk among adjacent circuits is not a considered issue for these chips as the circuits on these chips are placed far apart from one and other.

Whenever a digital circuit changes state, a current spike will be injected into the power supply and the chip substrate. Since the substrate of a CMOS process has small resistance, the noise induced by this current spike will propagate to adjacent circuits. In order to reduce the effect of this substrate noise to the analog circuits, the analog and the digital circuits are placed in separate sections of the microchip. These sections are separated by guard rings and wells. Figure 4-3 shows a layout of the analog circuits (preamplifier and post-amplifier) surrounded by guard rings. The rings are constructed by two p+ regions connected to ground (outer rings) and an n well region connected to the positive power-supply (middle ring). The p+ connections to ground provide low impedance path between the substrate and ground to keep substrate noise from

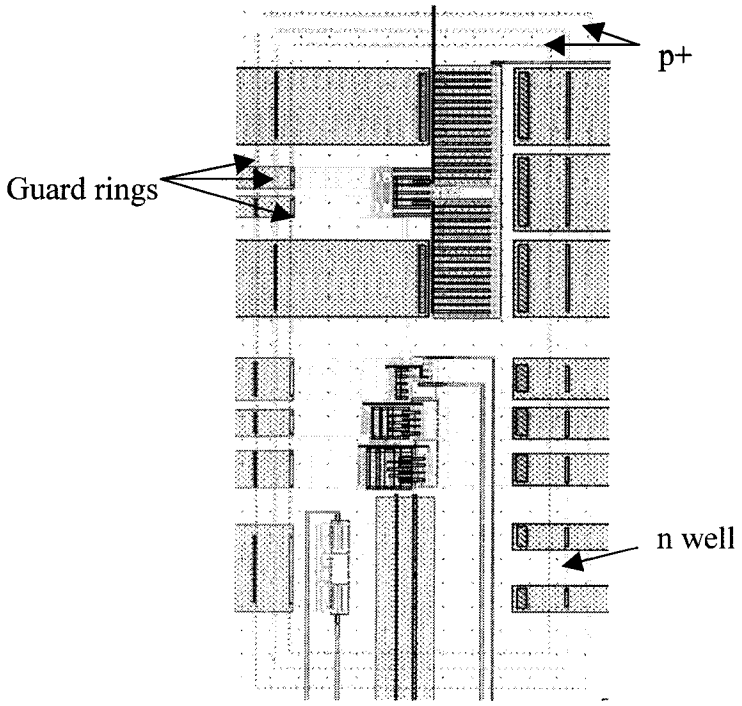


Figure 4-3: Layout of analog circuits (preamplifier and post-amplifier) with their guard rings.

propagating through the resistive substrate. The n well region between the p+ connections further increases the substrate resistance between the analog and the digital sections [5].

The current spike injected into the power supply of the microchip will induce a voltage drop at the internal supply according to the relationship:

$$V = L\frac{dI}{dt} \qquad (4.1)$$

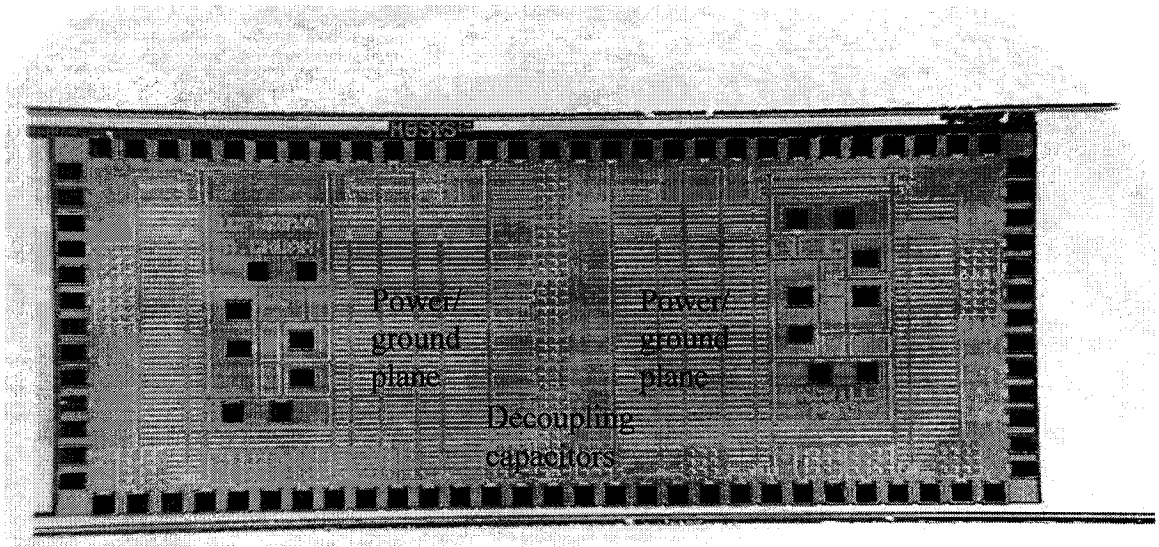
L is the inductance of the power-supply interconnects. This voltage drop causes the noise at the power supply, also known as ground bounce, SSN, or ΔI noise. The reason for the name is obvious from equation (4.1).

In the layout of the microchips, separate I/O pins are used for the power-supply to the analog circuits and the digital circuits. This is to prevent the power-supply noise of

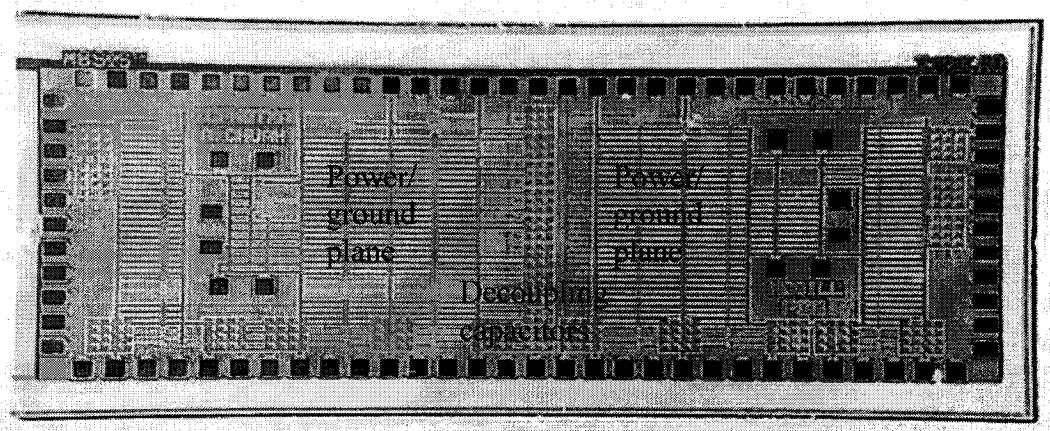
the digital circuits from affecting the analog circuits. In addition, by using multiple power pins, the amount of current handled by each pin is reduced; thus reducing the ΔI factor in equation (4.1). In other word, the effective inductance of the power supply connections is reduced, as there are multiple inductors in parallel. Further more, decoupling capacitors are implemented on unoccupied chip area, as shown in the photographs of the chips in Figure 4-4. These capacitors are connected between the power-supply and ground distribution networks on the chips. These capacitors bypass the current spike induced during switching of the circuits, and hence reducing the SSN [6]-[8]. In order to reduce the parasitic inductance of the power-supply and ground distribution networks on the chips, these distribution networks are implemented with wide metal lines in parallel, which resemble a huge power/ground plane. This is also indicated in the photographs of Figure 4-4.

4.3 Chip Packaging

The packaging of the chip(s) will affect the high-speed performance of the circuit. Aside from the circuit performance, the cost and the availability of the packaging technique is also a factor in the consideration of packaging options. In the following subsection, the author will briefly discuss two different packaging techniques. Then, the packaging technique used for the optical transmitter and receiver is presented.



a)



b)

Figure 4-4: Photographs of the a) receiver chip, b) transmitter chip. The on-chip decoupling capacitors and power/ground planes are indicated on the photographs.

4.3.1 Wire-Bonded versus Flip-Chip Bonded Photonics

The most common way of providing electrical connection between the optical transmitter/receiver circuits and the lasers/photodetectors are by wire bonding. In this case, the lasers/photodetectors and the transmitter/receiver circuits are fabricated in separate chips. The chips are then connected electrically by bond wires. This method is commonly used in the packaging of most fiber-based telecommunication transceiver modules. This packaging methodology is straightforward and cost effective. However, a 1mm bond wire of 50μm in diameter has a parasitic inductance of ~1.5nH. This could affect the high-speed performance of the circuits, especially the driver circuitries. The inductance of the bond wire together with the capacitance of the bond pads cause signal ringing when the signal has a fast rise and fall time. This ringing limits the speed of the circuits. Note that the effect of parasitic inductance to high-speed laser driver has been presented in section 2.5.1.1.

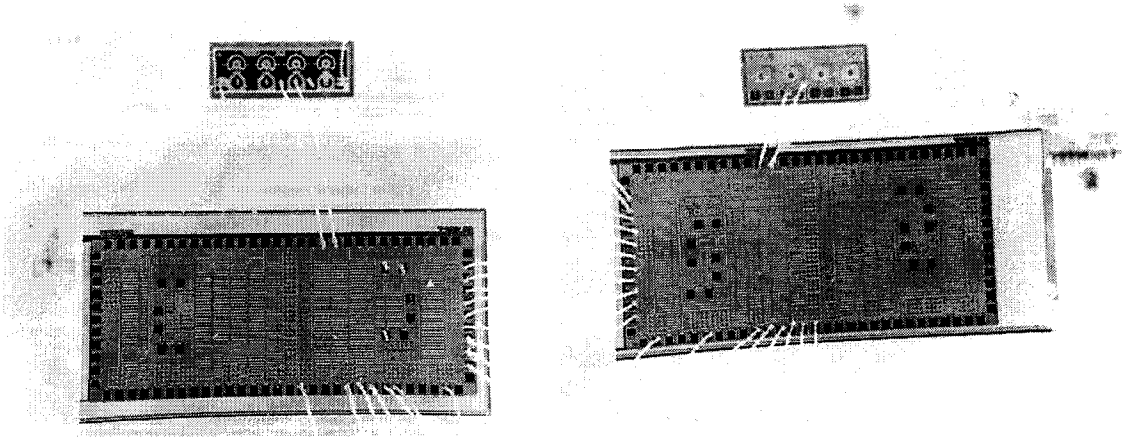
Many techniques have been developed to integrate photonic devices directly on microelectronic chip. One of these techniques is flip-chip bonding. This is a mature and well-understood technique. Flip-chip bonding introduces much lower parasitic capacitance and inductance compared to wire bonding, which provides better bit rate performance to the circuits. A. V. Krishnamoorthy and K. W. Goosen showed in their analysis in [9] that flip-chip bonding allows better bit rate performance and lower power dissipation. Not only that, flip-chip bonding also allows high-density, 2-D integration of optoelectronic devices. Several high-density optoelectronic VLSI chips based on flip-chip bonding of MQW modulators and detectors or VCSEL and p-i-n photodiodes on silicon CMOS chips have been demonstrated [10]-[12].

4.3.2 How is it done?

For cost and time saving purposes, the author chose to use wire-bonding technique to provide electrical connections between the CMOS chips and the photonic chips. Wire bonding is done in the packaging lab of Photonic Systems Group in McGill University.

In the case of an optical transmitter, a CMOS transmitter chip and a VCSEL chip are placed in an 80-pin ceramic quad flat-pack chip carrier provided by CMC. The substrate of the CMOS transmitter chip and the VCSEL chip are conductive. Since the substrate of the CMOS transmitter chip and the VCSEL chip need to be biased at different potential, the base plane of the chip carrier is laser trimmed by CCT Laser Services, so that the substrate of the chips can be electrically isolated from each other. Different biasing voltages are provided to each isolated base plane through bond wires.

In the case of an optical receiver, a CMOS receiver chip and a p-i-n photodiode



a) b)

Figure 4-5: Microscope photoes of a) CMOS transmitter chip and VCSEL chip, b) CMOS receiver chip and p-i-n photodiode chip, sitting in chip carrier after wire-bonding.

chip are placed in another 80-pin ceramic quad flat-pack chip carrier. Since the substrate of the photodiode chip is nonconductive, laser trimming at the base plane of the chip carrier is not necessary. Figure 4-5 shows microscope photoes of a) CMOS transmitter chip and VCSEL chip and b) CMOS receiver chip and p-i-n photodiode chip sitting in the chip carrier after wire bonding.

After the chips are wire-bonded, the chip carrier is clamped to a printed circuit board test fixture (CFP80TF) provided by CMC. The printed circuit board provides impedance matched microstrip lines for high-speed signals operating up to 4.5 GHz [13]. It also provides two power planes and a ground plane that have on-board decoupling capacitors that reduce power noise. Biasing voltages are provided to the chips through the control lines available on board. Figure 4-6 shows a photograph of the CFP80TF printed circuit board test fixture with a chip carrier containing the CMOS receiver and p-i-n photodiode chips.

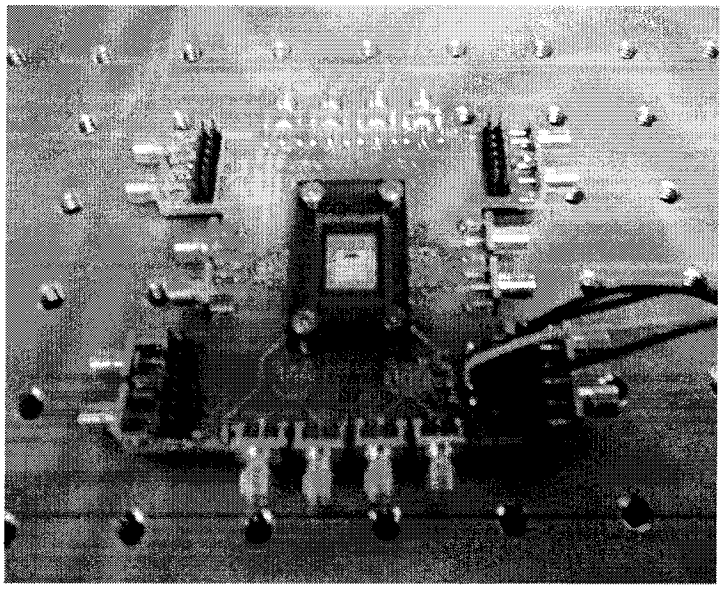


Figure 4-6: Photograph of the CFP80TF printed circuit board test fixture with a chip carrier containing the CMOS receiver and p-i-n photodiode chips.

4.4 Chip Testing

After the chips are fabricated and packaged, they are ready to be tested. Details about what kind of tests and measurements to be carried out and how they are done is described in section 4.4.1. Test results are presented in section 4.4.2.

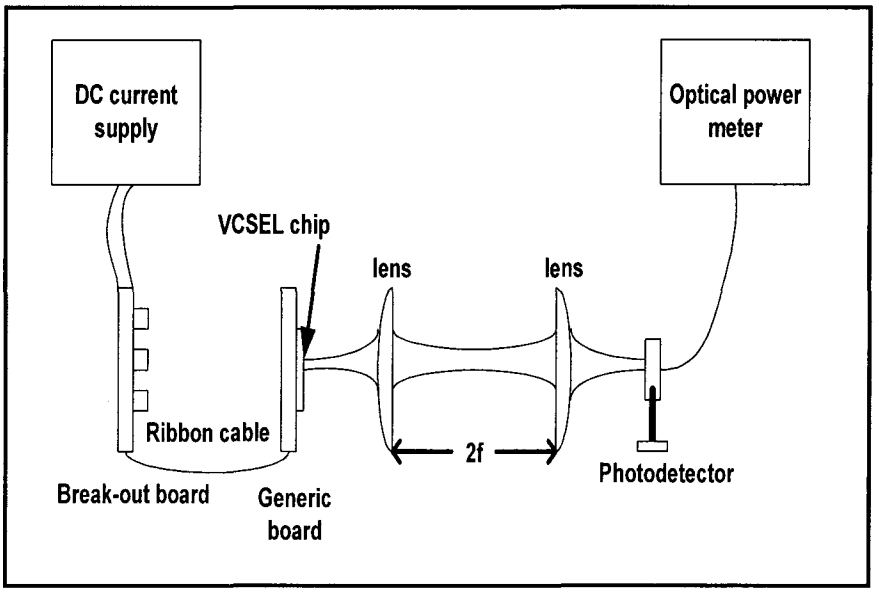
4.4.1 Test Plan

The testing of the optical transmitters and receivers involves tremendous amount of planning and execution. These works are split into three major parts. First of all, the VCSEL that is going to be used for the transmitter is characterized. Then, a transmitter chip packaged together with a VCSEL chip is tested. Finally, a receiver chip packaged together with a p-i-n photodiode chip is tested.

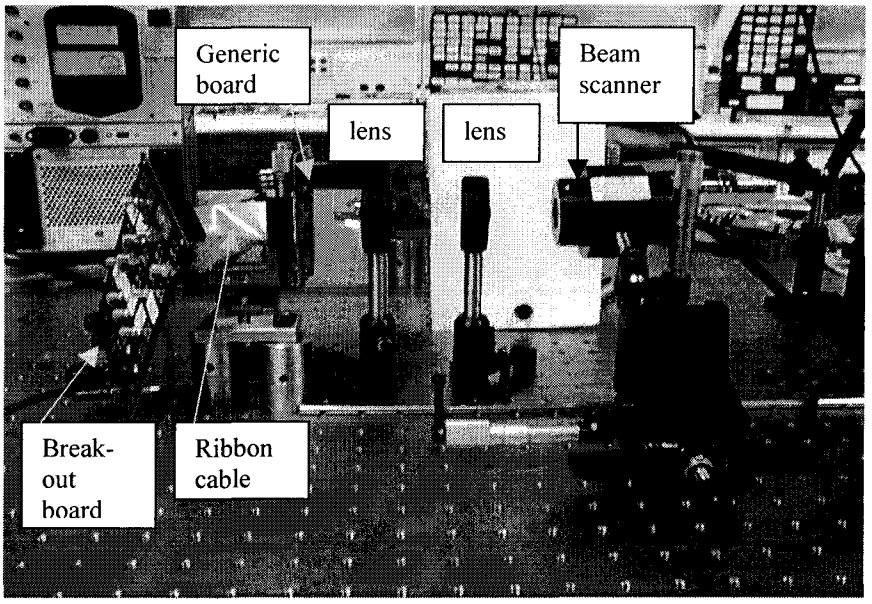
4.4.1.1 VCSEL Characterization

In order to obtain an optical power versus current (L-I) characteristic of the VCSEL, a VCSEL chip is mounted on a generic printed circuit board [14], and wire-bonded to bonding pads on the board which are connected to power supply. DC current is injected into one out of four of the VCSELs on the VCSEL chip. The DC current is varied and the output optical power of the VCSEL is monitored using an optical power meter. The generic printed circuit board is itself connected to the power supply through another breakout board, which is simply a printed circuit board occupied with power jacks and high-speed connectors. Figure 4-7 a) shows a block diagram of the test setup, whereas Figure 4-7b) shows a photograph of the actual test setup, except that the

photodetector has been replaced with a beam scanner to capture the beam profile of the laser output.



a)



b)

Figure 4-7: a) Block diagram of the test-setup to characterize the VCSEL. b) Photograph of the actual test-setup. The VCSEL chip is mounted on the generic board and a beam scanner is used to capture the beam profile of the laser output.

4.4.1.2. Testing of Transmitter Chip

The transmitter chip is packaged together with a VCSEL chip in a CFP80 flat-pack chip carrier, that is then mounted on the CFP80TF PCB test fixture for the testing. The details have been discussed in section 4.3.2.

To start the testing of the transmitter chip, the chip is powered up and a DC test is carried out to check for shorts in the circuit. After passing the DC test, the PCB test fixture is hooked up to a data generator for functional test at low frequency range. The test is done with an ARX-SA Amplified Photodetector (APD) [15] from *Antel Optronics Inc.* to detect the optically transmitted signal. Figure 4-8 shows a block diagram of the test setup for the functional test.

An optical system needs to be designed in order to collimate the light from the VCSEL to the high-speed photodetector. In this case, a telecentric (4f) optical relay system is used [16]. A telecentric optical relay system composed of two lenses, as shown

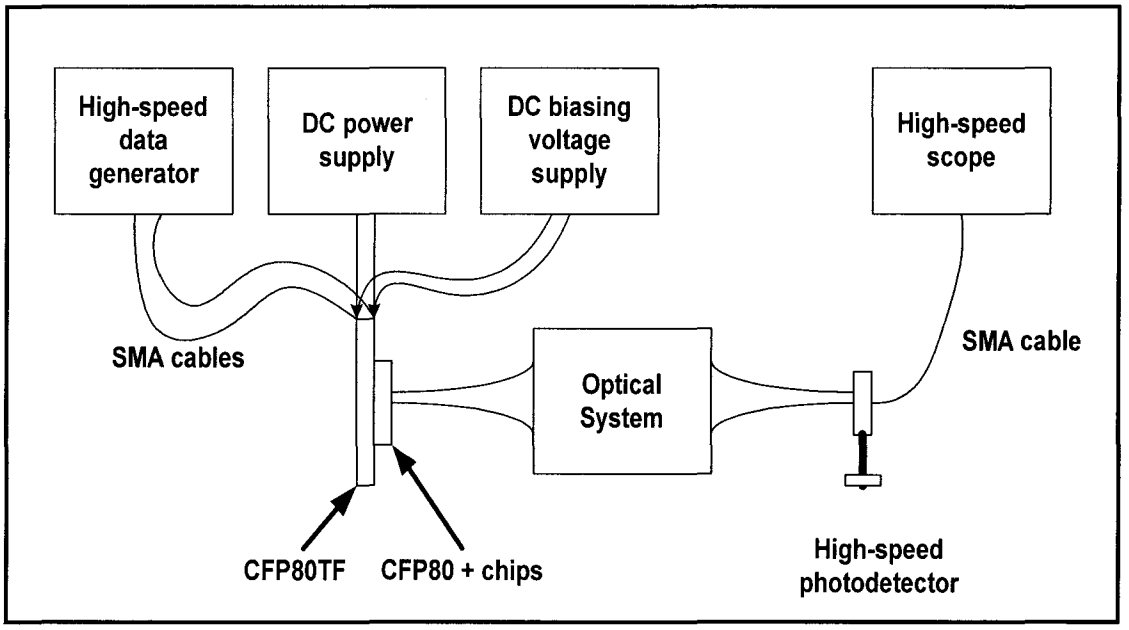


Figure 4-8: Block diagram of the test setup for the optical transmitter.

in Figure 4-9, with a same focal length, *f*. The two lenses are placed at a distance of 2*f* apart. The object is placed at the focal point of the first lens and the image is focused at the focal point of the second lens. The lenses were chosen to have a focal length of 40mm. A 50/50-beam splitter is used to allow for the monitoring of the position of the optical signal on the photodetector with a CCD camera.

According to the data sheet for the 1×4 VCSEL array chip from *EMCORE Corporation* [17], the maximum divergence angle ($1/e^2$) of the VCSEL is 32 degrees. Hence, for lenses with a focal length of 40mm, the diameter has to be at least 22.9mm, or a f/# of less than 1.74.

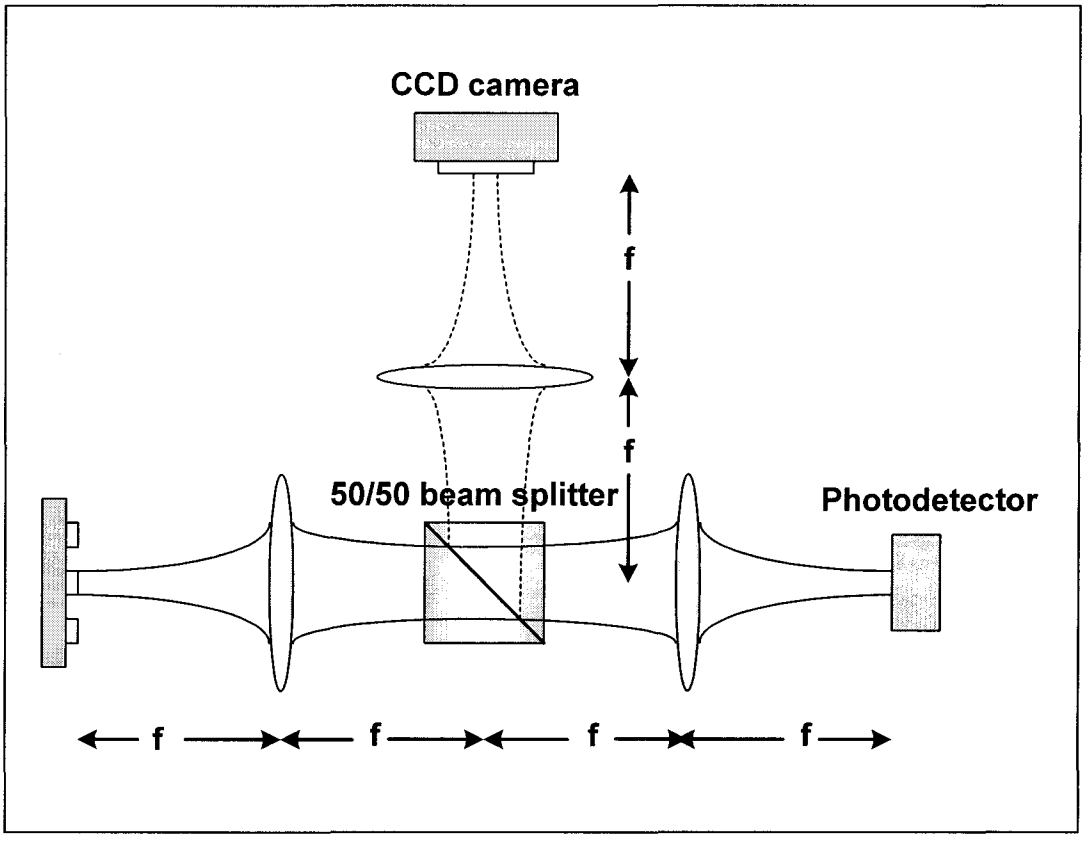


Figure 4-9: Block diagram of a telecentric optical relay system of the test setup for the optical transmitter.

If the chip passes the functional test, the operation frequency of the circuit is slowly increased for high-speed test. These tests are performed on txa1 and txb1 (refer to Figure 4-2). Eye pattern generated by the transmitter's optical signal will be used to qualify the performance of the circuits. In case of failure, the circuits txa3 and txb3 as well as the test structures ts1 and ts2 (Figure 4-2) can be used to help debug the problem. Figure 4-10 shows a flowchart that summarizes the test process of an optical transmitter.

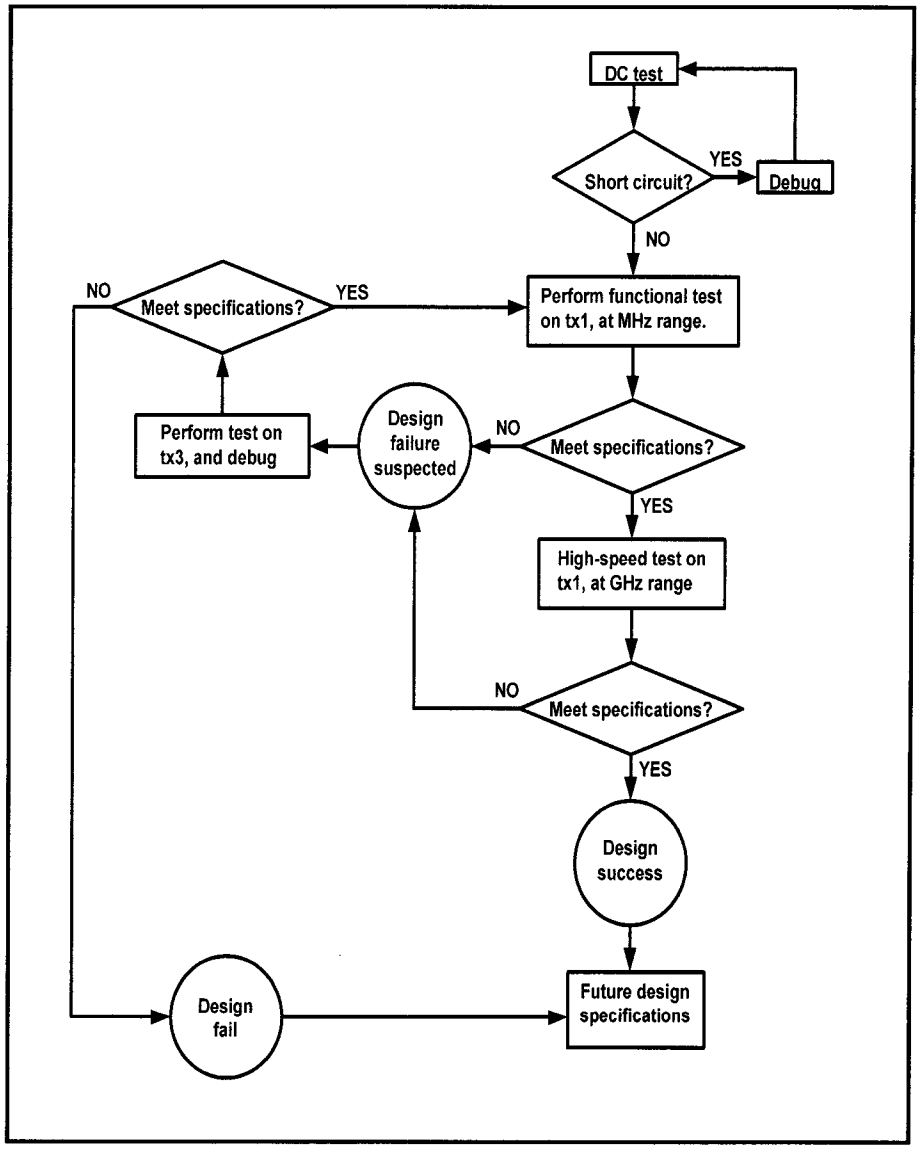


Figure 4-10: A flowchart summarizing the test process for an optical transmitter.

4.4.1.3 Testing of Receiver Chip

The test procedure for the receiver chip is very similar to the test procedure for the transmitter chip. It can be summarized with a flowchart very similar to the one in Figure 4-10. However, the test setup for the optical receiver is different from that for the transmitter.

Figure 4-11 shows a block diagram of the test setup for the receiver. A high-speed light source is used to generate the test signal for the receiver. The high-speed light source used is a printed circuit board consisting of a high-speed laser driver chip (VSC7923) from *Vitesse Semiconductor Corporation*, and an 850nm-laser source. The biasing current and the modulation current to the laser source is adjustable with two potentiometers on the circuit board. This high-speed light source can provide optical signal with modulation bit-rate of up to 1Gbps [18]. The receiver chip and a 1×4 photodiode array chip are packaged in a ceramic flat-pack chip carrier (CFP80), which is mounted on the CFP80TF PCB test fixture as described in section 4.3.2.

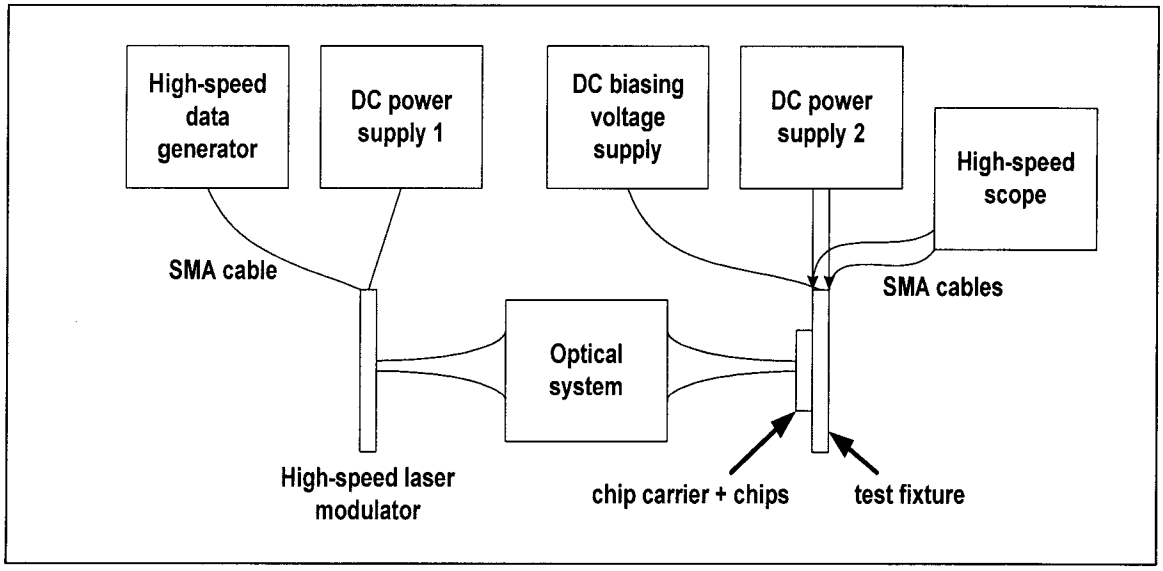


Figure 4-12: Block diagram of the test setup for the optical receiver.

In order to focus most of the transmitted optical power to the active area of the photodiode, the optical system is designed with a microscope configuration. Two lenses with different focal length f_1 and f_2 are placed at a distance of $(f_1 + f_2)$ apart. The high-speed light source is placed at the focal point of the first lens, and the photodiode is placed at the focal point of the second lens. With a beam waist of ω_o at the light source, it can be shown that the beam waist that appears at the photodetector, ω_o', is magnified by a factor given by the ratio of the focal lengths of the two lenses, that is:

$$\omega_o' = \frac{f_2}{f_1}\omega_o \qquad (4.2)$$

With a smaller beam waist appearing at the photodiode, the transmitted optical power is focused to a smaller area. Figure 4-13 shows a photograph of the actual test setup to test the receiver chip.

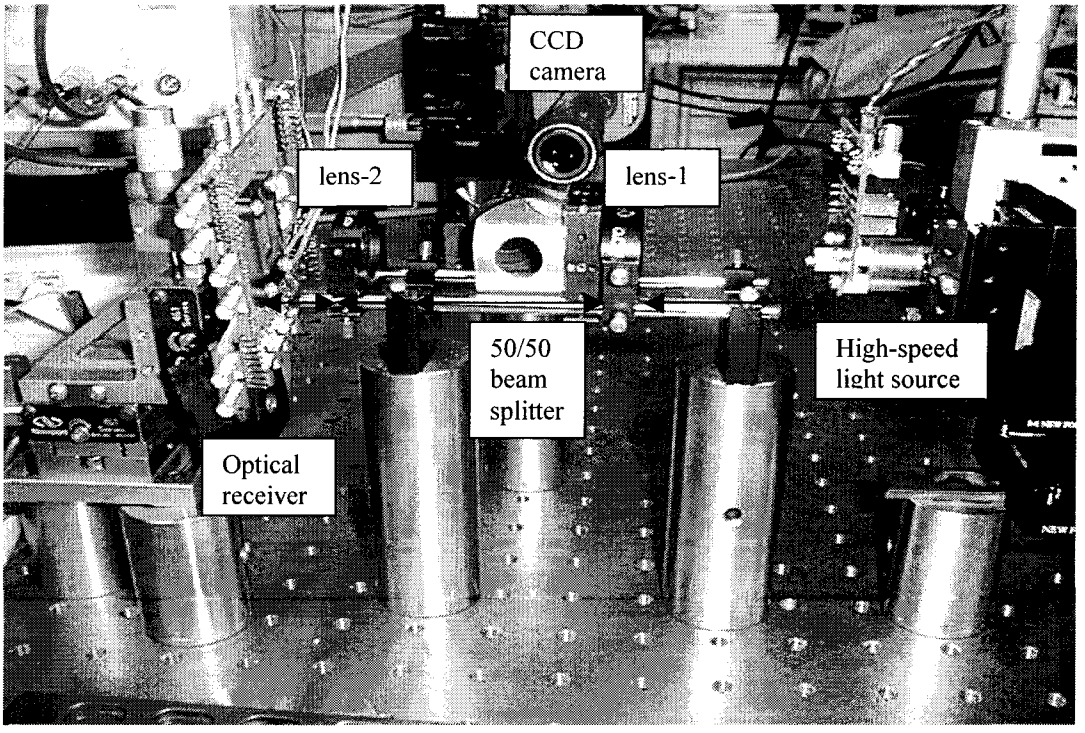


Figure 4-13: Photograph of the actual test setup to test the receiver chip.

4.4.2 Test and Measurement Result

4.4.2.1 VCSEL Characterization

One out of four VCSEL on a 1×4 VCSEL array chip is randomly picked and characterized. Biasing current supplied to the VCSEL was varied and the output optical power is recorded. Figure 4-14 is a plot of laser output power versus bias current (L-I curve), together with beam profiles of the output when the laser is biased at 2mA and 10mA respectively. A photograph of the VCSEL biased at threshold is attached at the left upper corner of the plot.

According to the measurement, the VCSEL has a threshold current of 1.2mA, and a slope efficiency of 0.34mW/mA. The output power saturates at 4mW when the bias

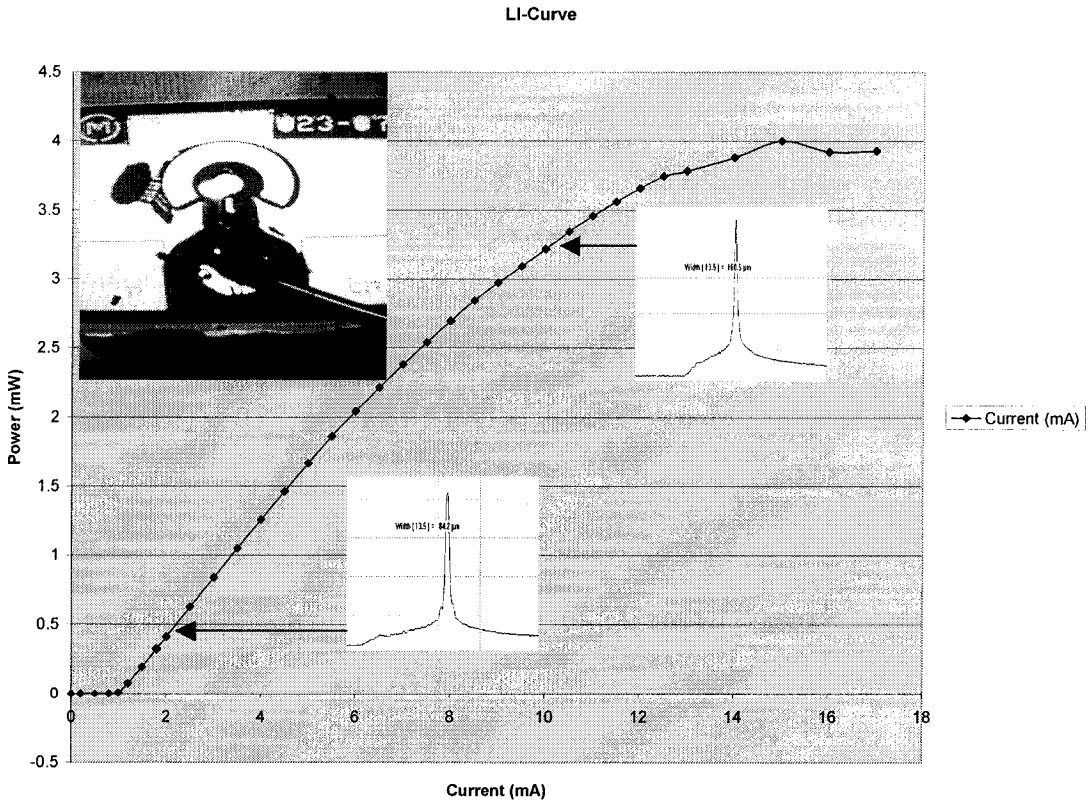


Figure 4-14: Plot of output optical power versus bias current of the VCSEL. Photograph at the top left corner shows the VCSEL biased at threshold. Beam profiles of the output when biased at 2mA and 10mA are also shown.

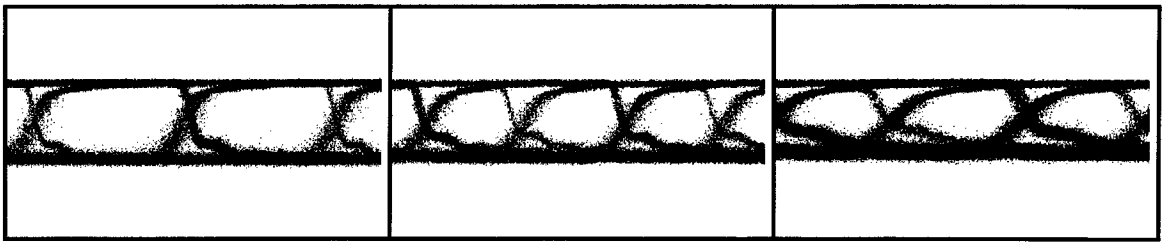
current is more than 15mA. The result obtained from this measurement is close to the specifications provided in the data sheet [17].

4.4.2.2 Optical Transmitter Circuits

Two different designs of optical transmitter circuits were implemented. These two circuits differ by the circuit topology of the laser drivers. One is implemented with the "fast-discharge" laser driver and the other with the "push-pull" laser driver. Both designs were tested.

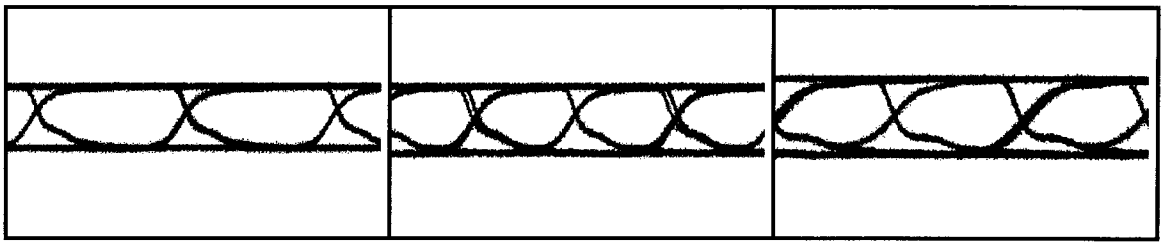
In order to test the performance of the optical transmitter circuits, a pseudo random bit sequence (PRBS) of $2^{32}-1$ is generated. The bit sequence is generated as low-voltage differential signal (LVDS) which has voltage swing between 1V to 1.4V. The modulated optical signal is detected by the amplified photodetector and eye pattern is captured on a 50Ω termination digital analyzer. Figure 4-15 shows the eye patterns obtained. Figure 4-15 a) shows eye patterns generated by the transmitter with "fast-discharge" laser driver at i) 500Mbps, ii) 750Mbps and iii) 1Gbps. Figure 4-15 b) shows eye patterns generated by the transmitter with "push-pull" laser driver at i) 500Mbps, ii) 750Mbps and iii) 1Gbps. The high-speed performance testing was limited by the performance of the available test equipment. The fastest digital data that can be generated in the lab was 1Gbps.

For circuit operation at 1Gbps, the fast-discharge laser driver delivers an average optical power of 250μW with a rise time of 490ps and fall time of 240ps; whereas the push-pull laser driver delivers an average optical power of 330μW with a rise time of 490ps and fall time of 350ps. Recall that simulation results in Chapter 2 predicted a



i) 500Mbps ii) 750Mbps iii) 1Gbps

a)



i) 500Mbps ii) 750Mbps iii) 1Gbps

b)

Figure 4-15: Eye patterns generated by the optical transmitter circuits with a) fast-discharge laser driver, b) push-pull laser driver using $2^{32}-1$ PRBS.

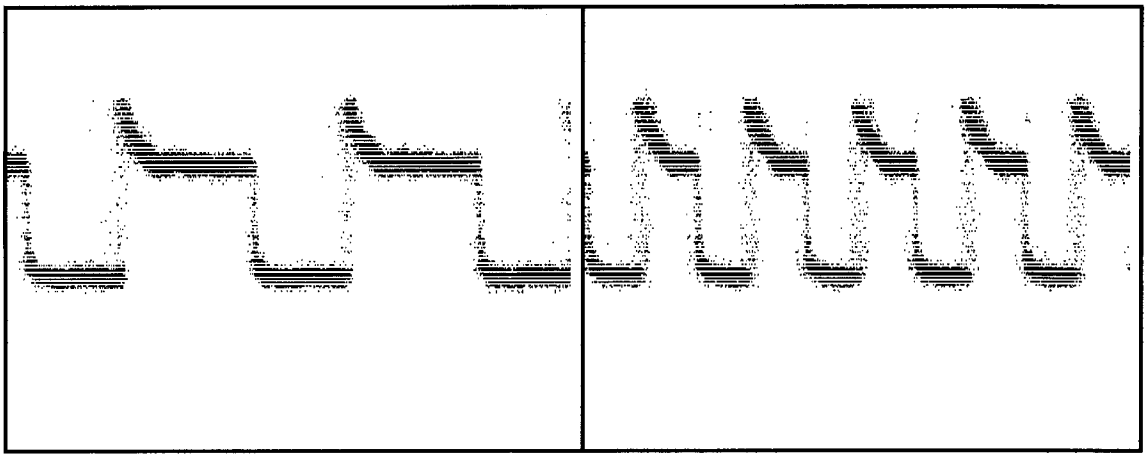
faster rise-fall time for the push-pull laser driver. However, the circuit test performed here was not able to verify that, due to limitations of the test equipment. On the other hand, Figure 4-15 shows that the transmitter with push-pull laser driver exhibits cleaner eye patterns, compare to the transmitter with fast-discharge laser driver. In addition to that, the eye patterns show no signs of current overshoots and undershoots.

4.4.2.3 Optical Receiver Circuits

Due to time constraints, only one receiver circuit was tested even though there were two designs implemented. The receiver circuit tested was the one designed with a current mirror preamplifier. The circuit was tested with square waveform up to 200Mbps.

The testing was difficult as the circuit was sensitive to offset voltage level, signal gain, as well as input optical power, so does the alignment of the optical system.

Figure 4-16 shows the signal waveforms of one of the differential outputs of the receiver circuit, at a) 100Mbps and b) 200Mbps. The signal is obtained for an average input optical power of 300μW.



a) b)

Figure 4-16: Square waveforms from the output of the optical receiver with a current mirror preamplifier at a) 100Mbps and b) 200Mbps.

4.5 Conclusion

Circuit layout and chip packaging technique can affect high-speed performance of a circuit. Good circuit layout strategy and packaging technique can improve signal integrity. On chip decoupling capacitors were implemented for the transmitter and receiver chips to power supply. Wide power and ground planes were implemented for the same purpose. Wire-bonding packaging technique was used for cost and time saving purposes, even though flip-chip bonding technique can provide better signal integrity.

Testing of an optical transmitter or receiver chip is a very involved process. Proper design of an optical system is critical for the testing of these circuits. Implementation of additional on chip test structures made the debugging of the chip easier in case of failure. The transmitter circuits were tested to be operating at 1Gbps, whereas a receiver circuit has been tested up to 200Mbps.

4.6 References

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Chapter 5: Conclusion and Future Work

5.1 Conclusion

Two designs of optical transmitter and two designs of optical receiver have been successfully designed and implemented. Both transmitter circuits were successfully tested at a data bit rate of 1Gbps. Due to constraint on the data generator, the circuits were not tested at data bit rate higher than 1Gbps. For the same reason, the performance of the two different designs could not be compared among one another.

The optical receiver circuit with a current mirror preamplifier was tested up to 200Mbps as time was running out. The test result produced a 50% duty cycle square waveform at 200Mbps.

5.2 Future Work

Testing of the transmitter circuits will be carried on as faster data generator and photodetector are purchased. The ongoing testing is aimed to verify the circuit performance at 4Gbps and faster.

There are still a lot of rooms for improvement in terms of circuit design and chip packaging. For the case of the optical receiver, automatic gain control (AGC) and automatic offset control (AOC) circuitry should be implemented for future designs. These circuits should reduce the number of off-chip biasing voltage supply, and make chip testing easier.

Flip-chip bonding technique should be used to integrate the photonic devices to the CMOS circuits. This will improve the performance of the circuits at high-speed,

especially the transmitter. Flip-chip bonding eliminates the parasitic due to bond wires, and hence will improve signal integrity. A simulation was performed on the push-pull laser driver without the inclusion of bond wire's parasitic. The simulation predicts a maximum modulation speed of 20Gbps. The signal waveform of the modulating current is shown in Figure 5-1.

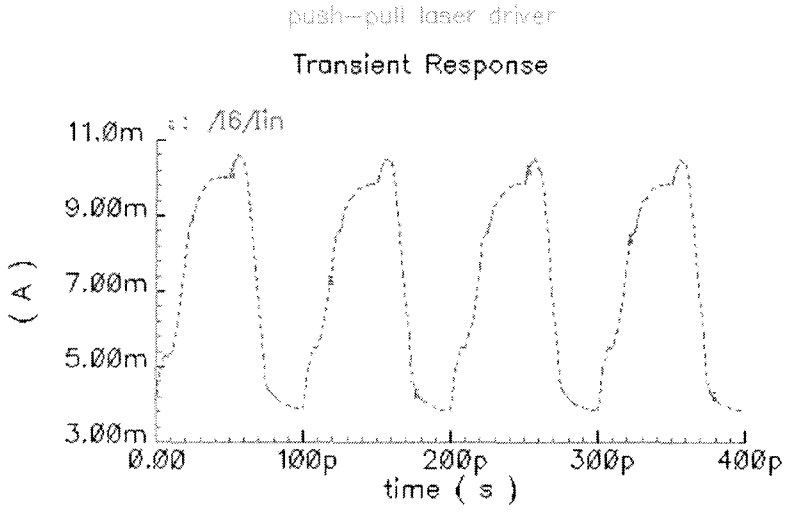

Figure 5-1: Output current of the push-pull laser driver without the parasitic of bond wires, modulating at 20Gbps.