Techniques for Simultaneous Optimization of Transimpedance Gain and Bandwidth for the Development of High-Speed, Low-Noise and Area-Efficient Transimpedance Amplifier Designs

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Abstract in English

This work presents techniques for designs of high speed and low noise transimpedance amplifiers for applications in next generation optical receivers and SerDes. Various trade off opportunities available in the transimpedance amplifiers architectures are discussed and designs are proposed to reduce the input-referred noise without compromising the bandwidth. For this purpose, three designs are proposed in this work. Each of these designs tend to minimize the noise without compromising bandwidth and gain. Some designs focus on reducing area consumption while the others focus on reducing the power consumption. The designs have been simulated in a 90 nm BiCMOS process (f_t = 310 GHz) from Global Foundries, while one of the designs has been fabricated in this process for experimental validation. The proposed designs offer an efficient area-power-noise-gain-bandwidth trade-off. The proposed techniques are compared with the recent state-of-the-art designs. Results suggest that the proposed designs can reduce the noise without any significant deterioration of bandwidth. The proposed designs achieve a bandwidth in the range of 34 GHz to 83 GHz with a minimum input-referred noise density of 0.87 pA/√Hz and a maximum input-referred noise density of 2.32 pA/√Hz. All simulated results include the effect of photodiode modeled as a current source with 65 fF capacitance. On-wafer probing is used for experimental verification and hence the measured results don't incorporate the effect of photodiode. Rather, the measured transimpedance gain has been extracted form the measured S-parameter data based on the mathematical conversion which is a typical procedure in literature. As per the author's best knowledge, the proposed designs have the lowest input-referred noise and highest transimpedance for targeted bandwidths. These TIAs are aimed to support data streams beyond 100 Gb/s.

Abstract in French

Ce travail présente des techniques de conception d'amplificateurs de transimpédance à haute vitesse et à faible bruit pour des applications dans les récepteurs optiques et les SerDes de la prochaine génération. Les différentes possibilités de compromis disponibles dans les architectures TIA sont discutées et des conceptions sont proposées pour réduire le bruit référencé en entrée sans compromettre la bande passante. À cette fin, trois conceptions sont proposées dans ce travail. Chacune de ces conceptions tend à minimiser le bruit sans compromettre la bande passante et le gain. Certaines conceptions se concentrent sur la réduction de la consommation de surface tandis que d'autres se concentrent sur la réduction de la consommation d'énergie. Les conceptions ont été simulées dans un processus BiCMOS 90 nm (f_t = 310 GHz) de Global Foundries (GF-9HP), tandis qu'une des conceptions a été fabriquée dans ce processus pour une validation expérimentale. Les conceptions proposées offrent un compromis efficace entre surface, puissance, bruit, gain et bande passante. Les techniques proposées sont comparées aux conceptions récentes de la littérature scientifique. Les résultats suggèrent que les conceptions proposées peuvent réduire le bruit sans détérioration significative de la bande passante. Les conceptions proposées permettent d'obtenir une bande passante comprise entre 34 GHz et 83 GHz avec une densité de bruit référencée en entrée minimale de 0,87 pA/√Hz et une densité de bruit référencée en entrée maximale de 2,32 pA/√Hz. Tous les résultats simulés incluent l'effet de la photodiode modélisée comme une source de courant avec une capacité de 65 fF. Des mesures sur *wafer* sont utilisées pour la vérification expérimentale, et donc les résultats mesurés n'incorporent pas l'effet de la photodiode. Le gain de transimpédance mesuré a été extrait des données de paramètres S mesurées sur la base d'une conversion mathématique, ce qui est une procédure typique dans la littérature. D'après les

connaissances de l'auteur, les conceptions proposées présentent le bruit d'entrée le plus faible et la transimpédance la plus élevée pour les bandes passantes ciblées. Ces TIA sont destinés à supporter des flux de données au-delà de 100 Gb/s.

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Contribution of Authors

With the supervision of Professor Gordon Roberts, Muhammad Bilal Babar conceived the ideas of the designs proposed in this thesis. Under the supervision of Professor Gordon Roberts, Muhammad Bilal Babar developed the theory, performed computations and designed tape-outs for the designs. Muhammad Bilal Babar wrote this thesis and Professor Gordon Roberts has supervised, edited and reviewed this thesis.

Reza Maram, from FONEX Data Systems, helped in understanding the background of optical receivers. He gave insight regarding the challenges and applications of high-speed TIA designs. He also helped in arrangement of the apparatus for measurements of the chips.

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List of Acronyms

TIA	Transimpedance Amplifier
TI	Transimpedance
DMUX	Demultiplexer
ADC	Analog to Digital Converter
DSP	Digital Signal Processor
CDR	Clock and Data Recovery
SerDes	Serializer/Deserializer
GA	Gain Amplifier
CTLE	Continuous-Time Linear Equalization
CB	Common Base
CG	Common Gate
CS	Common Source
CE	Common Emitter
CC	Common Collector
RMS	Root Mean Square

BW	Bandwidth
VEO	Vertical Eye Opening
GBP	Gain Bandwidth Product
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
ISI	Inter Symbol Interference
NRZ	Non-return to Zero
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio

1 Introduction

1.1 Motivations and Applications

1.1.1 Structure of optical receivers and their applications

Increase in complexity of modern applications such as cloud computing, internet of things, smart cities and high-definition video has resulted in increased demand for development of high bandwidth infrastructure in the data center communications. Due to high speed, noise rejection and electrical isolation properties, optical fiber technology is used in such communication systems. Therefore, for electro-optical and vice versa conversion, high bandwidth optical transceivers are in high demand.

Coherent optical transceivers are usually employed in long haul communication between data centers. A typical coherent optical receiver is shown in Fig. 1.1. Front-end photodiode detects the optical signal and converts it into a photodiode current. This current is then amplified manifolds and converted to voltage by the transimpedance amplifier (TIA). TIA usually involves a transimpedance (TI) stage followed by a Continuous-Time Linear Equalization (CTLE). This will be elaborated further in subsequent sections. The output of the TIA is fed to an analog-to-digital converter (ADC) followed by a demultiplexer (DMUX). The output of the DMUX is passed to the digital signal processor (DSP) for digital processing. A clock and data recovery unit (CDR) is used to recover the clock which is then used to synchronize the actions of the ADC, DMUX and DSP blocks.

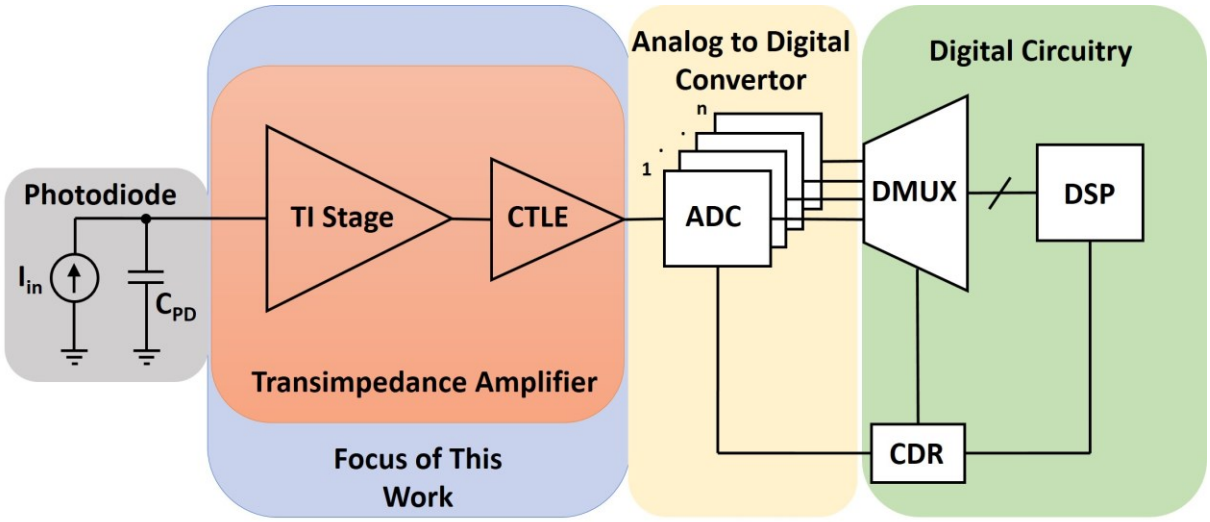


Fig. 1.1: A typical coherent optical receiver.

1.1.2 The need for high speed and low noise TIAs in optical receivers

The output current of a photodiode is usually very small (in the order of few hundred µAs), which needs to be converted to a voltage level and amplified many folds so that a valid logic level can be extracted from the incoming optical data. The TIA serve as the analog front-end in the optical receivers and their main purpose is to transform the very small input current pulse to a much larger digital voltage pulse using a very high transimpedance gain. Further, the TIA must be able to detect low level currents. To do so, a TIA must exhibit very low noise properties. In this thesis, this noise is measured in terms of the input-referred noise current spectral density. Additionally, to support high data rates, the 3-dB bandwidth of the TIA must be larger than at least half of the data rate of the incoming data stream, typically in the form of a non-return-to-zero (NRZ) line code. Therefore, there is a high need for simultaneous optimization of gain, noise and bandwidth, which remains the central challenge associated with TIA designs. This will be further elaborated in chapter 0.

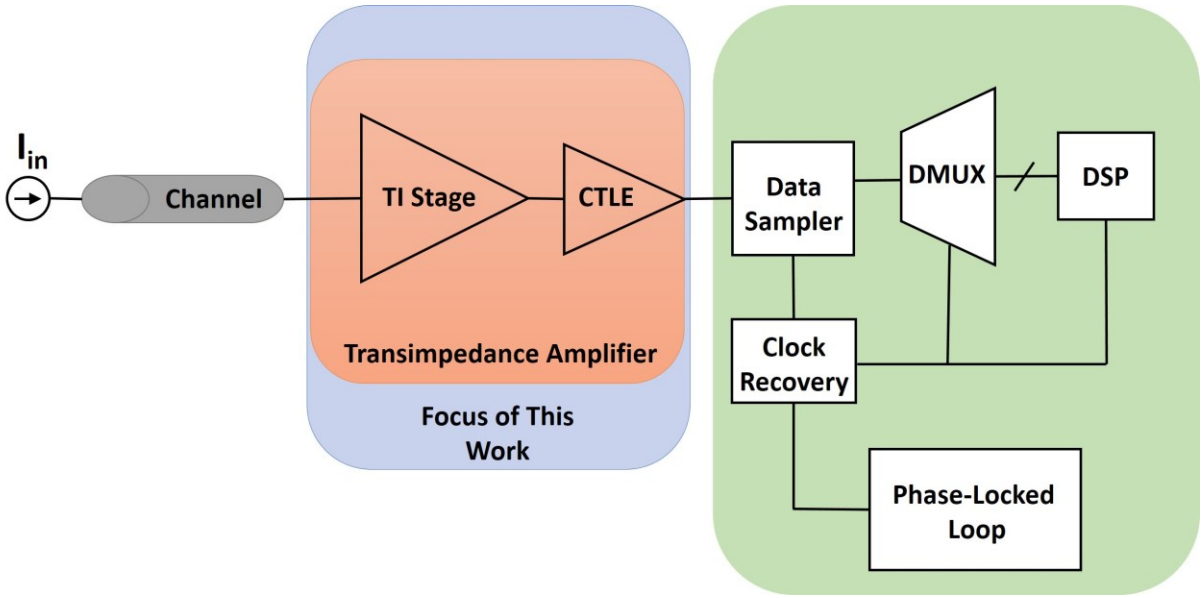


Fig. 1.2: A typical receiver in current-mode SerDes.

1.1.3 Need for high-speed and low-noise TIAs in SerDes

Although the main focus of this work is to explore TIA deigns targeting optical receivers, the need for high-speed and low-noise TIAs is not only limited to optical receivers. High-speed/low-noise TIAs find applications as the receive circuit for the current-mode transmitters in serial-to-parallel or parallel-to-serial interface [1], shorten to SerDes. Fig. 1.2 shows a typical receiver used in SerDes with current-mode driver transmitters. The circuits needed in a SerDes interface are more area critical than those in an optical receiver. Therefore, inductorless design approaches find more applications in SerDes. The work of Chapter 5 will present such inductorless approach in which high-speed/low-noise TIAs will be developed without the need for and inductors, thereby providing large silicon area savings. Even in the case of voltage-mode driver transmitters for SerDes interfaces, CTLE circuits are needed to equalize for channel losses. Therefore, high speed CTLE schemes discussed in this work find wide applications in current-mode as well as voltage-mode SerDes.

1.2 Research Goals

The primary objective of this research is to analyse and exploit various trade-off opportunities available in the TIA architectures and to propose new methodologies to develop area efficient TIAs that can achieve high speeds with very low noise and optimum power consumption. The proposed designs will be shown to exceed the performance of the present state-of-the-art designs.

For this purpose, three different TIA circuit designs will be proposed in this thesis. Each design will be optimized for crucial performance parameters of bandwidth, noise, and transimpedance gain. Further, circuit considerations such as silicon area and power consumption will also be addressed. The proposed designs will be validated using a 90-nm Global Foundry GF-9HP BiCMOS process technology and compared to cutting-edge designs. The proposed designs will act as the foundation for even faster next-generation TIA designs.

1.3 Structure of Thesis

This thesis is organized as follows.

Chapter 2 provides background of TIA designs including typical TIA architectures, noise analysis of TIAs and description of the concept of CTLE for high-speed designs. This chapter also presents detailed analysis of the recent progress in high-speed TIA designs.

Chapter 3 presents a feedback inductive peaking approach to increase the TI limit. This approach is based on enhancement of gain-bandwidth product of TI stage via the introduction of transmission zeros in open loop response. The enhanced gain-bandwidth product is then traded-off with higher transimpedance gain in the closed-loop operation. Simulations of a fully differential TIA designed using this approach are presented along with comparison with the state-of-the-art designs.

Chapter 4 presents the proposed methodology for a multi-stage RC compensation technique for decoupling the transimpedance and BW. This design provides a way forward for the high-speed/low-noise TIA designs. The proposed technique is then combined with the conventional CTLE buffer approach to develop a high-speed/low-noise prototype TIA. The experimental validation of the prototype is presented along with detailed comparison with the state-of-the-art designs.

Chapter 5 presents an area efficient and inductorless implementation of CTLE scheme. A fully differential high-speed TIA is then developed based on this CTLE scheme and its post-layout simulations are provided along with comparison with state-of-the-art designs.

Chapter 6 provides a conclusion of this thesis, along with the way forward for the development of next generation optical receivers and SerDes.

2 Literature Review

In order to successfully amplify the photodiode current and to convert it to a digitally processable voltage signal, the TIA must have sufficient gain, enough 3dB bandwidth and low input-referred noise. As in any other system, the gain is specified by the desired output signal level and, to some extent, the linearity of the system. Bandwidth is specified by the maximum data rate that needs to be applied to the receiver. For NRZ data stream, the 3dB bandwidth of TIA should be at least half of the data rate to get an open eye diagram at the output. Finally, the input-referred noise specification is determined by the amplitude of smallest signal that needs to be detected and processed by the TIA.

Input-referred noise is one of the most critical specifications and is a major bottleneck in the TIA designs. This is because the gain or bandwidth specifications can be easily achieved by cascading more gain or bandwidth peaking stages, but reducing the noise poses some challenges and, as it will be shown in this chapter, most of the recent TIA research is focused on reducing the input-referred noise.

Due to the technology scaling and inherent gain-bandwidth product of any amplifier, usually it is not possible to get the desired gain specification from a single amplifier stage. Therefore, TIA amplifiers are typically realized as a cascade of several amplifier stages, the transimpedance (TI) stage that receives the photodiode signal, followed by an additional cascade of gain stages, referred to here as gain amplifier (GA), as depicted in Fig. 2.1. This gain amplifier is necessary to achieve

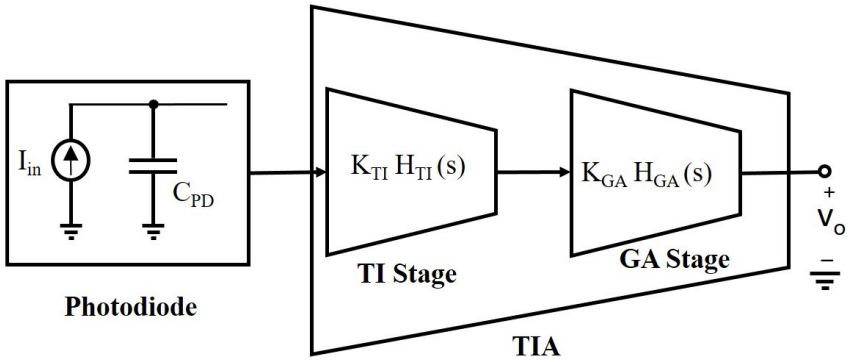


Fig. 2.1: Block diagram of a typical TIA used in optical receivers.

the overall gain specifications. Additionally, this gain amplifier cascade can also be used to enhance the overall bandwidth by implementing a CTLE. This will be elaborated in section 2.4.

In the subsection 2.1 typical architectures will be discussed for the implementation of the front-end TI stage of the TIA cascade of Fig. 2.1. This analysis will be presented in terms of key parameters, i.e., gain, bandwidth and input-referred noise.

2.1 Typical TI Stage Implementations

Typical implementation architectures for TI stage with promising high frequency response include the feed-forward common-base (CB)/common-gate (CG) amplifier, shunt-feedback amplifier, and shunt-feedback amplifier with a CB/CG input stage arrangement as analyzed in [2]-[3]. These are displayed in Fig. 2.2 and their gain, bandwidth and noise performance will be analysed in following subsections.

2.1.1 Common base TI stage

The low frequency transimpedance of the common-base TI stage is derived in [2] to be

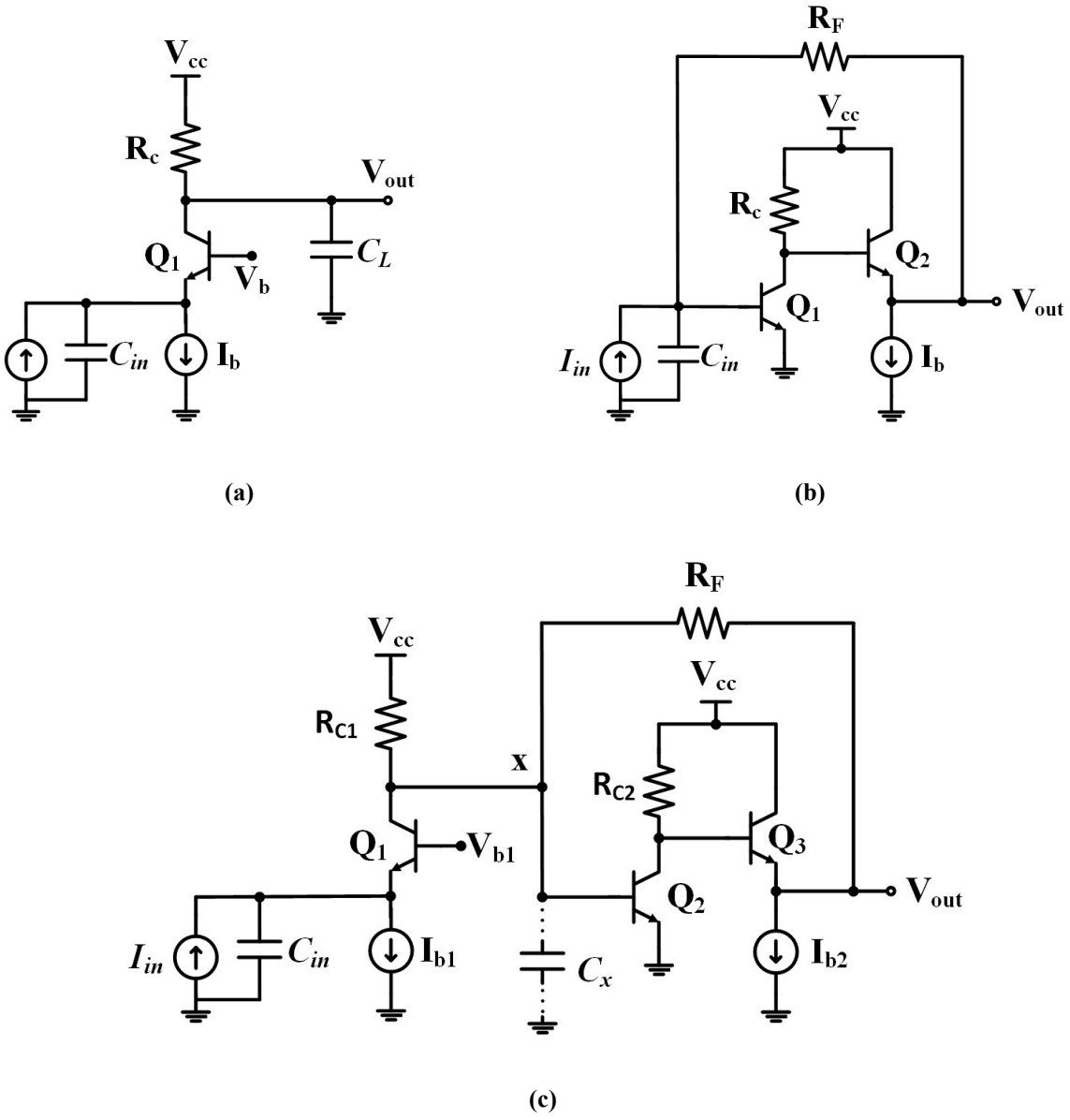


Fig. 2.2: Typical transimpedance stage implementations: **(a)** common base, **(b)** shunt-feedback and **(c)** shunt-feedback with common base input stage.

$$\frac{V_{out}}{I_{in}} = R_T = \frac{(1 + g_m r_o)r_\pi + r_b}{(1 + g_m r_o)r_\pi + r_b + R_c + r_o} R_c \tag{2.1}$$

Here, R_T denotes the total input-output low frequency transimpedance, r_o represents the channel length modulation of Q_1, r_b represents the base resistance of Q_1 and r_π represents the base-emitter

resistance of Q_1. Additionally, using the assumption that $(1 + g_m r_o)r_\pi + r_b \gg R_c + r_o$, the above expression reduces to

$$\frac{V_{out}}{I_{in}} = R_T \approx R_c \tag{2.2}$$

The expression for high frequency transimpedance of this circuit is derived in [4] to be

$$TI\ (s) = \frac{V_{out}}{I_{in}}(s) = \frac{R_T}{(1 + s/\omega_{p1})(1 + \frac{s}{\omega_{p2}})} \tag{2.3}$$

where $\omega_{p1} = \frac{g_m}{C_{in}}$ and $\omega_{p2} = \frac{1}{R_c C_L}$. C_{in} represents the total capacitance at the input node while C_L represents the total capacitance at the output node. If the ratio of these two poles is denoted as $\frac{\omega_{p1}}{\omega_{p2}} = x$ then the bandwidth of this circuit is given as

$$BW \leq \sqrt{\frac{f_t}{2\pi R_T C_{in} x}} \tag{2.4}$$

Here, f_t represents the unity gain bandwidth which is essentially a technology dependent parameter. The equality is reached in the expression of (2.14) for higher values of $'x'$. It is important to appreciate the fact that C_{in} in the common base approach will be very small as compared to the C_{in} in the shunt-feedback approach. This is because unlike shunt-feedback TI, in common base stage, the total input capacitance is not increased due to the absence of miller's capacitance which is a dominant capacitance for the case of shunt-feedback TI stage. Hence in the case of common base TI, C_{in} will be mainly dominated by the photodiode capacitance. Consequently, the common base TI stage can achieve higher bandwidth than its shunt-feedback TI stage counterpart.

The input referred noise of the common-base TI stage shown in Fig. 2.2 (a) is found in [2] to be

$$S_{i,in,TI}(f) = S_{i,R_c}(f) + S_{i,Q_2}(f) \tag{2.5}$$

Here, *S(f)* represents the power-spectral density (PSD), the first subscript letter represents the circuit variable, *v* for voltage or *i* for current, the second and/or third subscript refers to the input or output port of the amplifier, or the noise contributing component. The input-referred noise current spectral density has units of A^2/Hz. If the PSD is for a voltage signal, then it will be expressed in units of V^2/Hz. As it is obvious from (2.5) the noise current spectral density for R_c and Q_2 contributes directly to the input-referred noise current spectral density. Consequently, the common-base architecture is noisy when compared with the other realizations.

2.1.2 Shunt-feedback TI stage

The low frequency transimpedance of the shunt-feedback TI stage shown in the Fig. 2.2 (b) is approximated in [2] to be

$$\frac{V_{out}}{I_{in}} = R_T = \frac{g_{m1}R_c}{1 + g_{m1}R_c}R_F \tag{2.6}$$

The high frequency expression for the transimpedance is derived in [4] to be

$$TI\,(s) = \frac{V_{out}}{I_{in}}(s) = \frac{-R_T}{\frac{s^2}{{\omega_o}^2} + \frac{s}{\omega_o Q} + 1} \tag{2.7}$$

Here,

$$A_o = g_{m1}R_c \tag{2.8}$$

$$\omega_o = \sqrt{\frac{2\pi f_A(A_o + 1)}{R_F C_{in}}}$$

$$Q = \frac{\sqrt{(A_o + 1)R_F C_{in}}}{2\pi f_A R_F C_{in} + 1}$$

The 3dB bandwidth of this TI stage is derived in [4] to be

$$BW \leq \sqrt{\frac{f_t}{2\pi R_T C_{in}}} \tag{2.9}$$

The equality is reached for $Q = 1/\sqrt{2}$. Here, f_A represents the dominant pole frequency of the open-loop common emitter amplifier which is used to construct the shunt-feedback TI stage in the Fig. 2.2 (b).

Although (2.9) might seem very similar to the case of the bandwidth of common base given by (2.4), the key difference is in the value of C_{in}. In the case of shunt-feedback TI stage, due to the miller's effect, the effective value of C_{in} is increased due to multiplication of the collector to base capacitance by the factor of the open loop gain. This is not the case for common base TI stage. Therefore, for a same technology node, gain, transistor size and power consumption, the bandwidth achieved by shunt-feedback TI stage will be less than that of common base TI stage.

The input-referred noise current spectral density of the shunt-feedback architecture can be described as

$$S_{i,in,TI}(f) = S_{i,R_F}(f) + \frac{S_{v,in,OLA}(f)}{R_F^2} \tag{2.10}$$

where this input-referred noise current spectral density is a combination of the noise current spectral density from the feedback resistor R_F and the input-referred noise voltage spectral density

of the open-loop amplifier. Equation (2.10) shows that the noise of R_F is directly referred to the input. This is comparable to the noise contributed by R_c in the common-base TI stage of Fig. 2.2 (a). However, in contrast, the noise-voltage spectral density of the open-loop amplifier is divided by R_F^2. Therefore, for a large R_F, the second term in (2.10) for the shunt-feedback arrangement is made insignificant in contrast to the second term of the common-base amplifier configuration.

2.1.3 Shunt-feedback TI stage with common-base input

Since a common-base amplifier results in smaller C_{in} and has a better high frequency response, it might be favorable to use it as the first stage with a shunt-feedback architecture to construct the TI stage. Such a configuration is shown in Fig. 2.2 (c). If the common-base stage is designed to provide a unity current gain, then the overall transimpedance has been found in [4] to be

$$TI\,(s) = \frac{V_{out}}{I_{in}}(s) = \frac{-R_T}{(1 + s/\omega_{p1})\left[\frac{s^2}{{\omega_o}^2} + \frac{s}{\omega_o Q} + 1\right]} \tag{2.11}$$

Here,

$$A_o = g_{m2}R_c$$

$$R_T = \frac{A_o}{A_o + 1}R_F$$

$$\omega_{p1} = \frac{g_m}{C_{in}} \tag{2.12}$$

$$\omega_o = \sqrt{\frac{2\pi f_A(A_o + 1)}{R_F C_x}}$$

$$Q = \frac{\sqrt{(A_o + 1)R_F C_x}}{2\pi f_A R_F C_x + 1}$$

C_x represents the total capacitance at the node 'x' which is the input of shunt-feedback stage. The 3dB bandwidth is then found to be in [4] as

$$BW \leq \sqrt[3]{\frac{f_t^{\,2}}{2\pi R_T C_{in} x}} \tag{2.13}$$

Here, $x = \frac{\omega_{p1}}{\omega_{b2}}$, where ω_{b2} is the 3dB bandwidth of standalone shunt-feedback stage. The equality is reached in (2.13) for higher values of x and for $Q = 1/\sqrt{2}$.

Consequently, as described in [4], comparison of (2.9) and (2.13) shows that for $\frac{f_t}{BW} > x$, the shunt-feedback TI stage with common-base input can achieve higher bandwidth than that achieved by shunt-feedback TI stage alone. However, as it will be shown next, this bandwidth extension comes at the cost of increased noise.

The input-referred noise current spectral density of the shunt-feedback TI stage with common-base input is

$$S_{i,in,TI}(f) = S_{i,RC}(f) + S_{i,Q2}(f) + \frac{1}{A_{CB}^2}\left[S_{i,R_F}(f) + \frac{S_{v,in,OLA}(f)}{R_F^2}\right] \tag{2.14}$$

A_{CB} represents the DC gain of common-base stage which will be unity for a unity current gain stage. As the first two terms are identical to that of the common-base amplifier, the shunt-feedback TI stage with common-base input has a higher input-referred noise spectral density than the common-base or shunt-feedback arrangement alone.

2.2 Noise Analysis of Multi-Stage TIAs

Since most of the TIAs are built as cascade of many stages to meet the gain and bandwidth requirements, it becomes very important to analyze the noise of a multi-stage system. In such a cascade network of many stages, input-referred noise of front-end stage is of primary interest to optimize the overall noise. Hence it is very important to design a very low noise front-end TI stage because the noise performance of any cascade network is predominantly limited by the noise of first stage. To elaborate this, noise analysis of multi-stage TIA of Fig. 2.1 is presented in this section.

The overall mean squared RMS output noise voltage of a TIA cascade shown in Fig. 2.1 can be expressed as

$$v_{n,o,rms}^2 = \int_0^\infty |K_{TI}H_{TI}(s)|^2 |K_{GA}H_{GA}(s)|^2 S_{i,in,TI}(f)df + \int_0^\infty |K_{GA}H_{GA}(s)|^2 S_{v,in,GA}(f)df \tag{2.15}$$

Here the input-referred current noise spectral density of the TI stage is denoted by $S_{i,in,TI}(f)$ and the input-referred voltage noise spectral density of the GA stage is denoted by $S_{v,in,GA}(f)$. The input-current to output voltage transfer function of the TI stage is denoted as $K_{TI}H_{TI}(s)$ and the input-voltage to output-voltage transfer function of GA is denoted as $K_{GA}H_{GA}(s)$. In these two cases, the leading terms K_{TI} and K_{GA} represent the DC gain of the TI and GA stages, respectively. Collectively, the overall DC gain of the cascade can be represented as $K_{DC} = K_{TI}K_{GA}$ which allows one to re-write (2.15) as

$$v_{n,o,rms}^2 = K_{DC}^2 \int_0^\infty |H_{TI}(s)|^2 |H_{GA}(s)|^2 S_{i,in,TI}(f) df + \frac{K_{DC}^2}{K_{TI}^2} \int_0^\infty |H_{GA}(s)|^2 S_{v,in,GA}(f) df \quad (2.16)$$

Two important conclusions can be drawn from (2.16), i.e., the maximum achievable DC gain should be obtained from the TI stage to minimize the effect of noise contribution from the GA stage in the total output noise. Additionally, the noise of the TI stage $S_{i,in,TI}(f)$ is more critical than subsequent stages because it has profound effect on the total output noise due to multiplication with overall DC gain K_{DC}. Furthermore, it is not easy to achieve high K_{TI} in high-speed applications because of the inherent gain-BW trade-off associated with an amplifier. Instead, one must rely on the high-speed nature of the TIA circuit to maximize its unity-gain frequency.

It is obvious from (2.16) that the noise of TI stage ($S_{i,in,TI}(f)$) should be minimized to reduce the overall input referred noise. Consequently, it is customary to select the architecture for TI stage which offers the least input-referred noise so that the TIAs with minimum overall noise can be built. The noise analysis of typical TI stage implementations presented in section 2.1 shows that the shunt-feedback TI architecture shown in Fig. 2.2 (b) results in the lowest input-referred noise spectral density. Therefore, this architecture will be used to build designs in rest of this thesis. Consequently, the remainder of this thesis will only consider the shunt-feedback architecture for implementation of TI stages in its discussions.

2.3 Noise-BW Trade-off in Shunt-Feedback Based TIAs

Now that the shunt-feedback implementation has been selected for the TI stage implementation due to its low noise properties, it is important to explore the noise-bandwidth trade-off in such amplifier.

The output RMS noise level for the shunt-feedback TI architecture of Fig. 2.2 (b) can be obtained by substituting for the current-noise spectral density for the feedback resistor R_F, expressed as $S_{i,RF}(f) = 4KT/R_f$, into (2.10), then further substituting into (2.16) to obtain

$$v_{n,o,rms}^2 = \frac{4KTK_{DC}^2}{R_F}\int_0^\infty |H_{TI}(s)|^2|H_{GA}(s)|^2 df + \frac{K_{DC}^2}{R_F^2}\int_0^\infty |H_{TI}(s)|^2|H_{GA}(s)|^2 S_{v,in,OLA}(f)df + \frac{K_{DC}^2}{K_{TI}^2}\int_0^\infty |H_{GA}(s)|^2 S_{v,in,GA}(f)df \quad (2.17)$$

The expressions for $S_{v,in,OLA}(f)$ and $S_{v,in,GA}(f)$ are not important here as they depend on the parameters of the open-loop amplifier and are independent of R_F. Equation (2.17) makes clear that for a low output RMS noise voltage from the TIA circuit, the DC gain of the front-end stage K_{TI} of the open-loop TI amplifier should be maximized. This leaves the first two terms on the right-hand side inversely proportional to R_F and R_F^2. Thus, a larger R_F (equivalent to a larger closed loop transimpedance gain) reduces the output RMS noise voltage from the TIA circuit. However, it will be shown in Section 3.1 that the bandwidth of the TIA circuit is also inversely proportional to R_F^{N+1}, where N is the number of stages in the open-loop amplifier cascade. Consequently, simultaneous optimization of output RMS noise level and bandwidth is a challenge, as there is an obvious *output noise level vs. bandwidth trade-off*. This is in addition to the classical gain-bandwidth trade-off associated with closed loop amplifiers. Due to this trade-off, only limited

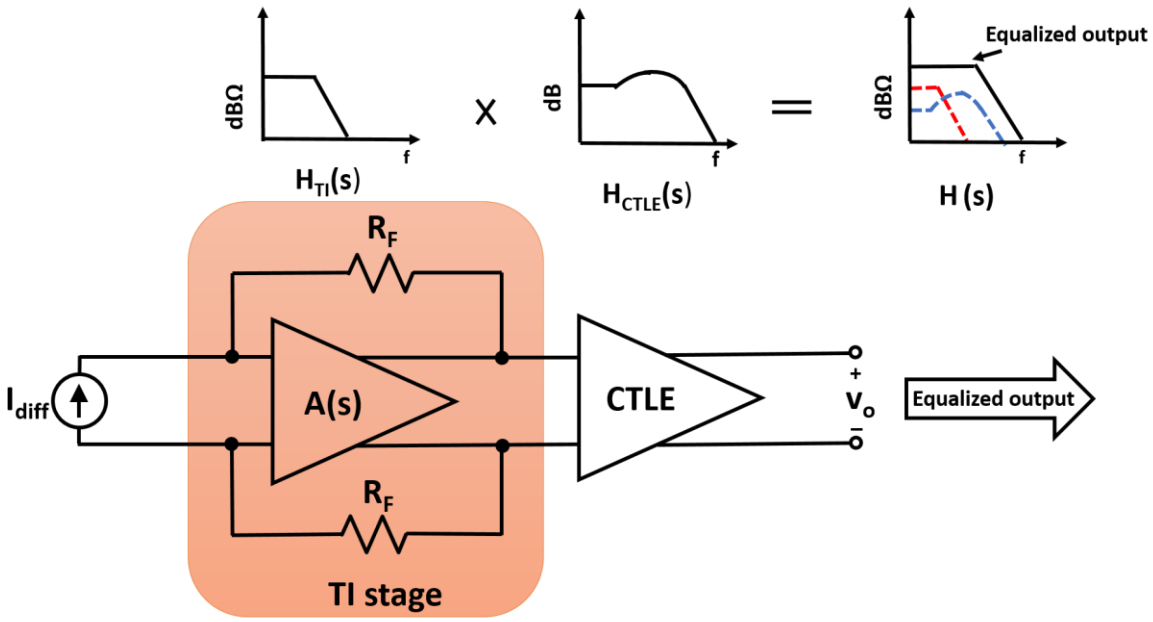


Fig. 2.3: CTLE based TIA architecture for simultaneous optimization of bandwidth, noise and transimpedance gain.

bandwidth can be achieved from TI stage for a particular noise level. To overcome this issue, CTLE is usually employed in TIAs which will be explained in next subsection.

2.4 Concept of CTLE

Due to the noise-BW trade-off presented in Section 2.3 and the inherent gain-BW trade-off in shunt-feedback TIAs which is commonly referred to as the TI limit (more on this in Section 3.1), it is challenging to achieve high bandwidth while reducing the noise and maximizing the TI gain. To overcome this challenge, the CTLE is usually employed after the TI stage [5]-[9]. The main objective of CTLE is to provide high frequency gain peaking for bandwidth equalization. Such a configuration is shown in Fig. 2.3. This configuration is identical to that of Fig. 2.1 in the sense that in the later, CTLE can be implemented with the gain amplifier cascade stages.

In a shunt-feedback TIA with CTLE, the bandwidth of the front-end TI stage is intentionally traded off for a higher value of the feedback resistance R_F. A higher R_F results in high transimpedance gain and lower input-referred noise spectral densities. The bandwidth lost in the TI stage due to the use of a higher R_F can be restored using high-frequency gain peaking obtained from the CTLE. With overall gain and bandwidth fixed by the system requirements, a designer is mainly left with two degrees of design freedom in CTLE based design: (1) the gain distribution per stage and, (2) the bandwidth extension ratio of CTLE.

Therefore, it is important to analyse the effects of gain and bandwidth distribution per stage on the output noise. These effects can be easily observed by simplifying (2.17). Since the noise spectral densities are usually uniformly distributed over entire bandwidth, $S_{v,in,OLA}(f)$ and $S_{v,in,GA}(f)$ can be replaced with the constants η_{OLA}^2 and η_{GA}^2 which represent the averaged noise power spectral densities of the open-loop amplifier and the gain amplifier respectively. After this substitution (2.17) becomes

$$v_{n,o,rms}^2 = \frac{4KTK_{DC}^2}{R_f}\int_0^\infty |H_{TI}(s)|^2|H_{GA}(s)|^2 df + \frac{K_{DC}^2}{R_f^2}\eta_{OLA}^2\int_0^\infty |H_{TI}(s)|^2|H_{GA}(s)|^2 df + \frac{K_{DC}^2}{K_{TI}^2}\eta_{GA}^2\int_0^\infty |H_{GA}(s)|^2 df \quad (2.18)$$

Additionally, this equation can be further simplified by approximating H_{TI}(s) and H_{GA}(s) as low pass filters with a uniform gain over the effective noise bandwidth of the amplifiers. For the sake of clarity, and to establish clear meaning, the effective bandwidth of the TI stage is denoted by $BW_{TI,eff}$. The effective noise bandwidth of the gain amplifier is denoted by BW_{GA_eff} and the overall effective noise bandwidth of the TIA is denoted as BW_{eff}. Further, if the open loop gain of the

amplifier is high, K_{TI} can be replaced by R_F. These substitutions result in the following equation for the output noise

$$v_{n,o,rms}^2 = \frac{4KTK_{DC}^2}{R_f} \times \mathrm{BW}_{eff} + \frac{K_{DC}^2}{R_f^2}\eta_{OLA}^2 \times \mathrm{BW}_{eff} + \frac{K_{DC}^2}{R_f^2}\eta_{GA}^2 \times \mathrm{BW}_{GA-eff} \tag{2.19}$$

Since K_{DC} and BW_{eff} are the constants representing the overall gain and bandwidth respectively, the effects of distribution of gain per stage and the bandwidth extension ratio of CTLE can be easily observed by deriving the expressions for sensitivities of the output noise with respect to R_F and BW_{GA_eff} respectively. These are obtained by taking partial derivatives of (2.19) as follows:

$$\frac{\partial_{v_{n,o,rms}^2}}{\partial_{R_F}} = \left[-\frac{4KTK_{DC}^2}{{R_f}^2} - 2 \times \frac{K_{DC}^2}{R_f^3}\eta_{OLA}^2\right] \times \mathrm{BW}_{ov-eff} - 2 \times \frac{K_{DC}^2}{R_f^2}\eta_{GA}^2 \times \mathrm{BW}_{GA-eff} \tag{2.20}$$

and

$$\frac{\partial_{v_{n,o,rms}^2}}{\partial_{BW_{GA-eff}}} = \frac{K_{DC}^2}{R_f^2}\eta_{GA}^2 \tag{2.21}$$

Equation (2.20) shows that R_F has a very strong impact on the output noise. An increase in R_F (gain of first stage) will result in a quadratic reduction of output noise power. On the other hand, due to the gain-bandwidth trade-off, increase of R_F demands that bandwidth of CTLE (BW_{GA_eff}) needs to be increased to provide higher bandwidth extension ratio so that overall targeted bandwidth can be achieved.

One may expect that increase in BW_{GA_eff} will significantly increase the output noise. However, this is not the case. As is apparent from (2.21), the sensitivity of output noise with respect to BW_{GA_eff} is essentially independent of the term BW_{GA_eff}. That means increase in BW_{GA_eff} results in only a linear increase in output noise as opposed to the quadratic effect of R_F.

Consequently, the concept of CTLE, in which the gain of first stage is increased at the cost of reduced front-end bandwidth and then the overall bandwidth is restored by high frequency peaking of the gain amplifier stage, proves to be very powerful technique for reducing the overall output noise power, and hence the input-referred noise current spectral density as well. As it will be described in Section 2.5, this concept is widely used in recent high-speed TIA designs.

2.5 Recent Advances in High-Speed TIA Designs

The design presented in [10] is among the pioneers in TIA designs. A shunt-feedback TI stage was used with additional inductor for additional gain peaking. Further, a CG/CS cascade was employed for better high frequency response. The circuit diagram for this implementation is shown in Fig. 2.4. Further, a CG stage was introduced before the shunt-feedback stage to reduce the input impedance. Though this structure provides better high frequency response than the shunt-feedback structure, it unfortunately results in a higher input-referred noise-current PSD. The major noise contributing element in this structure is the front-end CG stage as evident form the analysis presented in Section 2.1.3. Therefore, this structure is not useful for simultaneous optimization of noise and bandwidth. Additionally, it uses two inductors for fully differential realization of the TI stage which makes it very expensive in terms of silicon area.

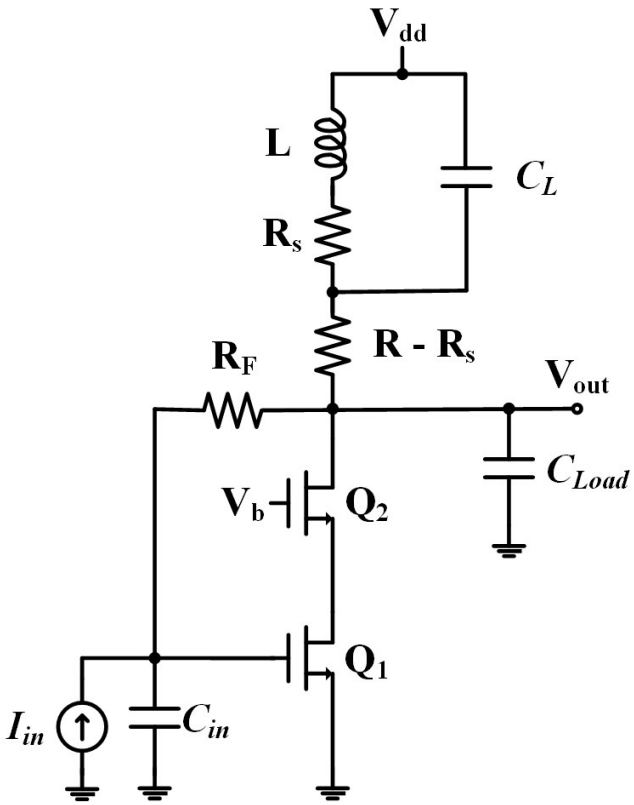


Fig. 2.4: A shunt-feedback TI stage with inductive peaking proposed in [10].

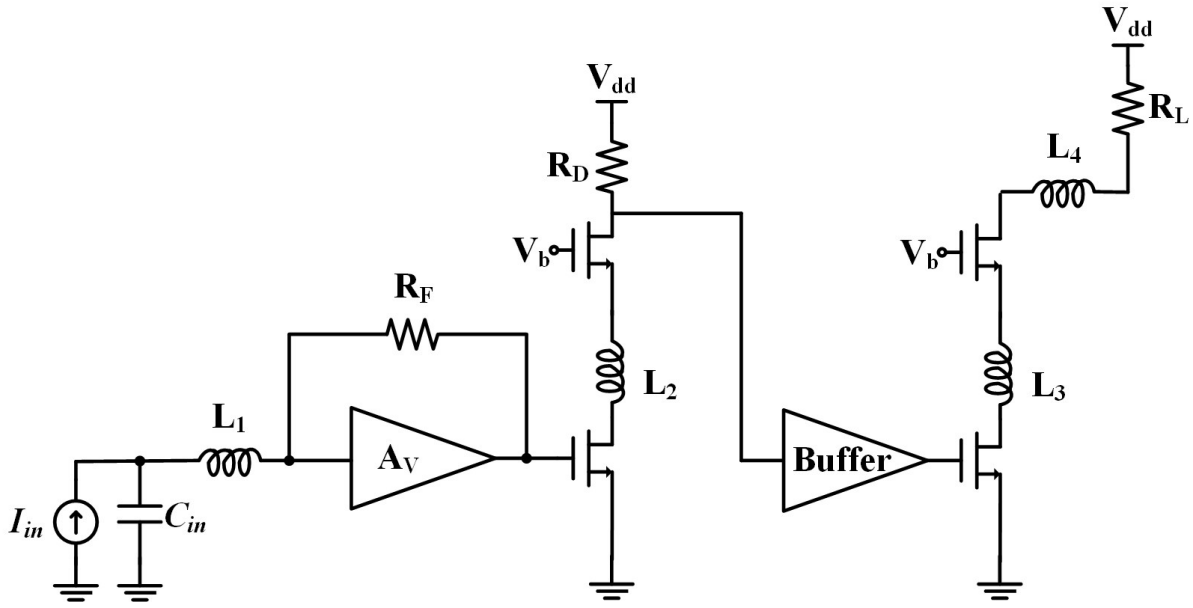


Fig. 2.5: TIA architecture with inductive ladder structure proposed in [11].

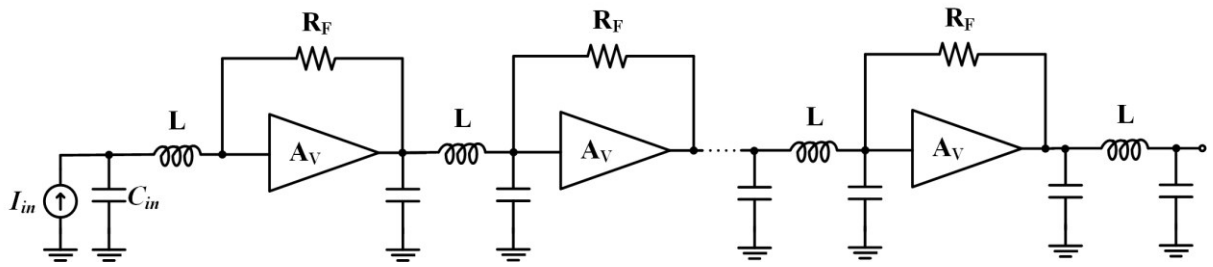


Fig. 2.6: Wideband TIA architecture proposed in [12].

In [11], passive networks are proposed to compensate for the parasitic capacitance effects of transistors. The proposed concept of the compensation is shown in Fig. 2.5 which is indeed quite similar to the concept of CTLE explained in Section 2.4. However, it will be shown later that there are better area-efficient ways to implement a CTLE than simply using passive networks.

In [12], a cascade of shunt-feedback CMOS inverter stages is proposed to implement the TIA and is shown in Fig. 2.6. Series inductors are inserted between the stages to compensate the effects of parasitic capacitances of transistors. While this design can achieve high gain and bandwidth, the input-referred noise PSD of this cascade will be very high. This is because the noise of first stage of the cascade will be multiplied by the gain of subsequent stages and amplified many folds. This is also evident from the noise analysis of a cascade structure presented in Section 2.2. Though this design can optimize the gain-bandwidth trade-off, it cannot optimize the noise-bandwidth trade-off. Moreover, this design is not area efficient due to the numerous series-peaking inductors. It will be shown later in Chapter 0 that other arrangements of inductive coils can give more bandwidth enhancement as compared to series-peaking inductors.

In [13], a π-type inductive peaking (PIP) approach is proposed to achieve a higher bandwidth extension ratio. The comparison suggests that the PIP technique can result in more bandwidth as compared to the shunt-peaking, T-coil peaking and shunt-series peaking. However, this analysis

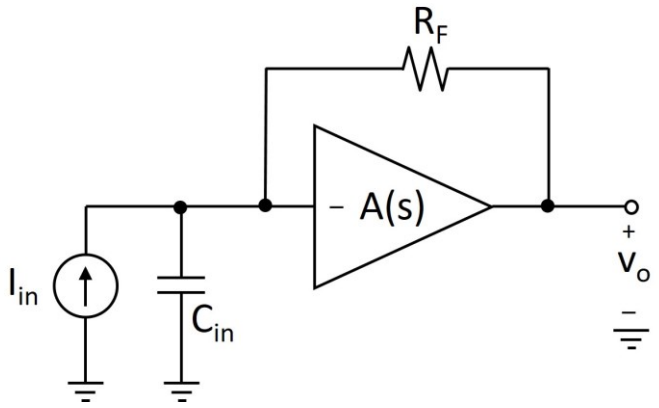


Fig. 2.7: Shunt-feedback TI stage analyzed in [4].

is lacking the comparison of group delay variations which are very important in reducing the ringing in pulse response. Additionally, a single stage π-type inductive peaking technique involves three area consuming inductive coils. It will be shown in the proposed designs of Chapter 0 and chapter 0 that better bandwidths can be achieved with fewer or no inductors at all.

In [4], Sackinger introduced the concept of transimpedance limit as the maximum achievable transimpedance gain by a shunt-feedback TI stage for a desired closed-loop bandwidth. This TI stage is shown in Fig. 2.7. For a single stage shunt-feedback architecture having following open-loop response

$$A(s) = \frac{A_O}{(1 + s/\omega_A)} \tag{2.22}$$

the transimpedance limit or TI limit for short, was found to be

$$R_T \leq \frac{A_o f_A}{2\pi C_{in} BW^2} \tag{2.23}$$

Here, R_T represents the total input-output transimpedance gain. It is related to the feedback resistance R_F of the TI amplifier as $R_T = R_F \frac{A_o}{A_o+1}$, where A_o is the open loop gain of the open-loop

amplifier, f_A is the dominant pole of the open-loop amplifier, C_{in} is the total capacitance present at the input terminal and BW is the overall closed-loop bandwidth of the TI stage. This limit indicates that there exists a strong coupling between R_F and BW. An increase in R_F results in a quadratic reduction in the closed-loop BW. This is assumed to be the biggest drawback of the shunt-feedback TIAs. However, it will be shown in this thesis that the TI limit can be enhanced by introducing a zero and complex poles in the open-loop amplifier. In fact, the proposed technique tends to make R_F independent of BW.

In [5], an innovative dynamic gain control approach is presented in which the gain of the TI stage can be varied by changing the value of R_F. This is achieved by physically placing two different valued feedback resistances (1 kΩ and 200 Ω) in the design and switching between them for gain variability. In high gain mode, R_F is set to 1 kΩ while in low gain mode it is set to 200 Ω. Since the open-loop amplifier is a cascade of three gain stages, the stability of the closed loop system is sensitive to the feedback gain (R_F). This means that if R_F is reduced significantly, the system can become unstable. To overcome this issue, a shunt capacitor is included in the low gain (R_F = 200 Ω) operation. While this resolves the issue of stability, this approach is disastrous for high-speed designs. This is because increasing the total input capacitance via the use of a shunt capacitor in low R_F mode will cause the pole at $1/R_FC_{in}$ to remain fixed. As a result, the opportunity of bandwidth improvement that could have been realized by pushing this pole to higher frequency via reduction in R_F is lost. Moreover, for gain variability of TI stage and switching of the shunt capacitor, MOSFET switches are used which appear directly in the front-end stage. The noise of these switches will be therefore amplified many folds by the subsequent stages. This will result in higher input-referred noise power.

In [14], a 92 GHz bandwidth TIA design is presented in 55 nm SiGe BiCMOS technology. While this design achieves a high bandwidth, the voltage gain is only 13 dB and for R_F = 220 Ω, the maximum TI gain is 47 dBΩ, which is neither enough for high sensitivity applications nor comparable to other more recent high-speed TIA designs [6]-[9]. Additionally, since the value of R_F is very small, the input-referred noise current spectral density of this design will be very high as indicated by (2.17). Finally, inductors are used in the open-loop amplifier of TI stage to provide high frequency peaking. It will be shown in Chapter 0 that same phenomenon of frequency peaking could be realized simply with RC elements alone.

In [6], [7] and [9], the concept of CTLE was proposed for simultaneous optimization of noise and bandwidth. In these designs, the frequency of front-end TI stage is intentionally reduced and the bandwidth equalization is achieved through subsequent CTLE stages. While this method proves very useful in reducing noise, it cannot optimize the noise-bandwidth trade-off beyond a certain limit. Typically, CTLE stages can reliably achieve a bandwidth extension ratio of approximately 2 [7]. Increasing the bandwidth extension ratio beyond this requires more aggressive peaking from CTLE stages, which results in high group delay variations and hence increase in ringing which results in reduction in the vertical eye opening. Therefore, further reduction of noise while increasing bandwidth requires enhancement in the TI limit of the front-end TI stage as described by (2.23).

In [8], a similar CTLE concept is employed where the capacitive degeneration is used in the variable gain amplifier stage to implement the CTLE. Additionally, a cascode stage is used in the front-end TI stage to increase the TI limit. This, however, is not a good approach from the view point of input-referred noise. This is because the additional CB/CG stage used to implement the cascode configuration will increase the noise power of open-loop amplifier as captured by the term

$S_{v,in,OLA}$ in (2.17). Since TI stage is the first stage of the subsequent cascade network, a higher $S_{v,in,OLA}$ will significantly increase the overall noise power as indicated by (2.16). It will be shown in the next chapter that the same enhancement of TI limit can be achieved by noiseless passive elements only.

2.6 Summary

This chapter presented a detailed background and literature review of TIAs. Typical TI stage implementations were analysed from the view point of gain, bandwidth and input-referred noise. Noise analysis of multi-stage cascade network was presented along with the analysis of noise-bandwidth trade-off in shunt-feedback TI stage. Based on these analyses, shunt-feedback based TI stage was selected to be the focus in rest of this thesis owing to its low input-referred noise as compared to other counterparts.

Additionally, the concept of CTLE was introduced and its application for simultaneous optimization of noise and bandwidth in TIAs was elaborated. Finally, a detailed review of recent high speed TIAs was presented along with critical analysis of each design in terms of key performance parameters such as TI gain, bandwidth, noise, silicon area and power consumption.

3 A Feedback Inductive Peaking Technique to Increase the TI Limit

This chapter presents a fully differential TIA design consisting of a cascade of TI front-end stage, gain amplifier and output buffer. Various trade off opportunities available in shunt-feedback TIAs are discussed and a circuit topology is proposed to reduce the input-referred noise without compromising its bandwidth. The design has been simulated in a 90 nm BiCMOS process from Global Foundries (GF-9HP) and offers an efficient area-noise trade-off. The proposed approach is compared with a conventional post-amplifier-based equalization methodology. Results suggest that the proposed approach can reduce the noise by allowing a bigger value of first stage transimpedance gain without any significant deterioration of bandwidth. The proposed design achieves a BW of 83 GHz with an average input-referred noise current spectral density of 2.32 pA/√Hz. All simulations include the effect of the photodiode modeled as a current source with 65 fF shunt capacitance. As per the author's best knowledge, the proposed design has the lowest input-referred noise current spectral density and highest value of feedback resistance (R_F) for an overall BW of 83 GHz. This TIA is aimed to support data streams beyond 100 Gb/s.

This design is mainly focused on increasing the TI limit of the front-end TI stage using feedback inductive peaking. The concept of TI limit, which will be elaborated in next subsection, was first introduced in [4] by Eduard Säckinger as the largest transimpedance gain achievable by a TIA for a desired bandwidth in a specific semiconductor technology. Numerous prototypes [6]-[9] have

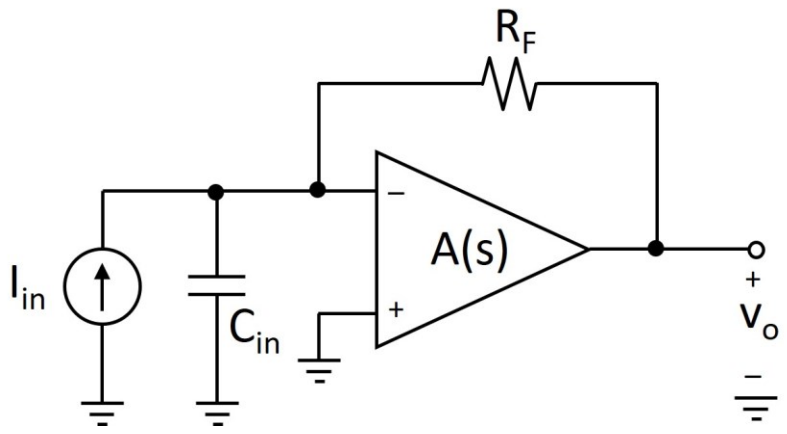


Fig. 3.1: A typical shunt-feedback-based TI stage.

been fabricated and tested that seem to give credence to this transimpedance limit. This limit, however, overlooked various design opportunities available for TIAs. This chapter exploits these opportunities and demonstrates that the transimpedance limit is actually higher than what Säckinger suggested.

3.1 Significance of the TI limit

A typical shunt-feedback TI stage is shown in Fig. 3.1 where A(s) is the open loop transfer function of the amplifier and R_F is the feedback resistance and C_{in} is the total input capacitance, which includes the photodiode and package parasitic capacitances. Assuming the amplifier has arbitrary transfer function A(s), one can easily show that the input-output transfer function of the closed-loop configuration, also referred to as the transimpedance function, can be expressed as

$$\frac{V_o(s)}{I_{in}(s)} = -\frac{R_f}{1+\frac{1+sC_{in}R_f}{A(s)}}. \tag{3.1}$$

If the feedback amplifier has infinite gain and bandwidth, i.e., $A \to \infty$, then the above transimpedance function is set exclusively by the feedback resistor R_F, i.e.,

$$\frac{V_o(s)}{I_{in}(s)} = -R_F. \tag{3.2}$$

Conversely, if the feedback amplifier is assumed to have a single pole response, i.e.,

$$A(s) = \frac{A_o}{(1 + {}^{s}/_{\omega_p})} \tag{3.3}$$

where A_o is the DC gain and ω_p is the frequency of the pole in rad/s, then the transimpedance function becomes

$$\frac{V_o(s)}{I_{in}(s)} = \frac{-R_f\left(\frac{A_o}{1+A_o}\right)}{\left[\frac{C_{in}R_f}{\omega_p(1+A_o)}\right]s^2 + \left[\frac{1+C_{in}R_f\omega_p}{\omega_p(1+A_o)}\right]s + 1}. \tag{3.4}$$

In [4], Sackinger showed that the above mentioned transimpedance function will reach maximum closed-loop bandwidth conditions when the transimpedance function has a Butterworth response, i.e.,

$$\frac{V_o(s)}{I_{in}(s)} = \frac{-R_f\left(\frac{A_o}{1+A_o}\right)}{\left(\frac{s}{BW_{CL}}\right)^2 + \sqrt{2}\left(\frac{s}{BW_{CL}}\right) + 1} \tag{3.5}$$

where the natural frequency of the characteristic equation ω_o is assumed to be equal to the 3-dB bandwidth (expressed in Hz), i.e.,

$$BW_{CL} = \frac{\omega_o}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{\omega_p(1+A_o)}{C_{in}R_f}} \tag{3.6}$$

The above equality holds if the following condition is met

$$C_{in}^2 R_f^2 \omega_p^2 - 2C_{in} R_f \omega_p A_o + 1 = 0 \tag{3.7}$$

One way to achieve this condition is to set the DC gain of the feedback amplifier to the following value,

$$A_o = \frac{C_{in}^2 R_f^2 \omega_p^2 + 1}{2C_{in} R_f \omega_p}. \tag{3.8}$$

Another way is to solve for the pole frequency ω_p assuming values for C_{in}, R_f and A_o. Regardless, to achieve a Butterworth response requires setting the circuit parameters to specific values.

As the magnitude of the transimpedance under the Butterworth conditions imposed above at DC is equal to $R_f \left(\frac{A_o}{1+A_o}\right)$, we shall substitute

$$R_T = R_f \left(\frac{A_o}{1 + A_o}\right) \tag{3.9}$$

and renormalize the closed-loop bandwidth expression in (3.6) as

$$BW_{CL} = \frac{1}{2\pi} \sqrt{\frac{\omega_p A_o}{C_{in} R_T}} \tag{3.10}$$

Recognizing that the product of $\frac{\omega_p}{2\pi} \times A_o$ is equivalent to the gain-bandwidth product of the chosen technology expressed in Hz and denoted by f_t , (3.6) can be rewritten in the following form

$$R_T \times BW_{CL}^2 = \frac{f_t}{2\pi C_{in}} \tag{3.11}$$

This expression takes on a similar form as the gain-bandwidth product but involves the squared-bandwidth term. Thus, this expression will be referred to as the *transimpedance-squared-bandwidth product* for the TIA circuit of Fig. 3.1. This expression demonstrates the trade-off

between the transimpedance at DC and the closed-loop bandwidth of the TIA circuit of Fig. 3.1. In [4], Sackinger defines the transimpedance limit as the maximum transimpedance available from a particular circuit under a specific bandwidth condition, i.e., for the circuit of Fig. 3.1, the TI limit is

$$R_{T,limit} = \frac{f_t}{2\pi C_{in} BW_{CL}^2} \tag{3.12}$$

The gain-bandwidth trade-off given by (3.12) and the noise-bandwidth trade-off given by (2.17) presents the challenge in simultaneous optimization of the noise, bandwidth and gain specifications. In order to overcome this challenge, the CTLE technique was used in recent TIA designs [6]-[9] and [15]-[16]. As explained in Section 2.4, the bandwidth of the front-end transimpedance stage is reduced intentionally by using a larger value of R_F which results in a higher transimpedance gain with less noise. The bandwidth is then restored by using a gain peaking technique in the secondary stage. The maximum bandwidth achievable with this approach, however, is limited as the transmission bit error rate is significantly degraded.

As explained in [7], the TI stage bandwidth needs to be around half that of the overall TIA bandwidth. Any smaller TI stage bandwidth requires large amount of gain peaking in the secondary stages, which in turn leads to higher levels of group delay variation across its bandwidth. This manifests itself in greater levels of overshoot and undershoot in the output pulse response of the TIA, which degrades the vertical eye opening of the output eye diagram.

Consequently, TIA implementations that operate beyond 100 GHz with noise levels smaller than 4 pA/√Hz remains a challenge even with CTLE approach.

3.2 Enhancing the Gain-Bandwidth-Product of TI Stage

In this section a technique that will reduce the TIA noise without any reduction in its bandwidth will be described. This is achieved by relaxing the upper bound on R_F limit set by the transimpedance limit described by (3.12).

It is evident from (3.12) that the transimpedance limit can be increased if the gain-3dB bandwidth product ($A_o \times f_A = f_t$) of the TI stage is increased. This can be achieved with the addition of a transmission zero in the TI stage. However, the introduction of zero(s) will result in gain peaking in the TI stage. This will increase the ringing in the pulse response which will result in a reduced vertical eye opening [6]-[7]. Therefore, after introduction of the zero(s), damping needs to be increased as well to maintain an overall maximally flat response. This is achieved by the clever placement of the poles and zeros by which the behavior of the closed-loop TI stage can be made to have a magnitude response whose behavior is flat across its bandwidth, i.e., no gain peaking.

Fortunately, this is very easy to realize in a shunt-feedback TI stage. A zero can be introduced by using an inductor in the feedback path, while the damping can be increased by simply increasing the value of the feedback resistance R_F. Single-ended small signal representation of the proposed shunt-feedback TI stage is shown in Fig. 3.2, where the feedback peaking inductor 'L_F' is used to introduce zero in the transfer function of closed loop system. R_F is the shunt-feedback resistance, G_m represents the transconductance and R_C is the total resistance at the output node which in case of CE/CS amplifier represents the collector/drain resistance. C_p represents the total capacitance at the output node which is a combination of the parasitic capacitance of the G_m stage and the input capacitance of the subsequent circuitry. I_{in} represents the output current of the photodiode and C_{in} represents the total capacitance at the input which is a combination of the photodiode capacitance

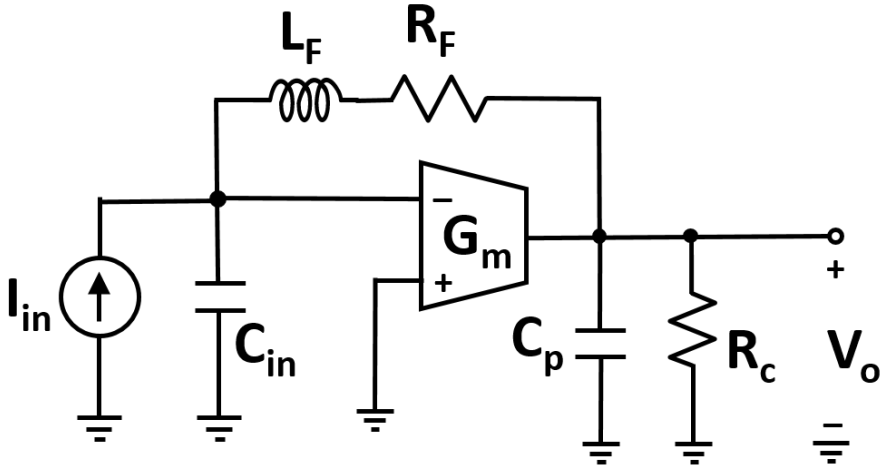


Fig. 3.2: Single-ended small signal representation of the proposed shunt-feedback first stage with feedback inductive peaking.

and the input capacitance of the G_m stage. These inductors are placed within the feedback loop instead of the open-loop amplifier for efficient area utilization. Therefore, this technique essentially trades-off chip area with noise. The closed-loop transfer function of the model shown in Fig. 3.2 is given as

$$T(s) = \frac{V_o(s)}{I_{in}(s)} = \frac{(G_m L_F + G_m R_F - 1)R_c}{\left[\begin{array}{c} C_{in}C_p L_F R_c s^3 + C_{in}\left(C_p R_F R_c + L_F\right)s^2 + \left((R_F + R_c)C_{in} + R_c C_p\right)s \\ + G_m R_c + 1 \end{array}\right]} \quad (3.13)$$

Equation (3.13) shows that the zero is created at the location $\frac{1-G_m R_F}{G_m L_F}$ which indicates that for a big inductor (L_F), the zero can be brought to lower frequency which will give more frequency peaking. Moreover, the damping can be increased by simply increasing the value of R_F because doing so will push the pole created by C_{in} and R_F to lower frequency which will result in overall smooth frequency response with less group delay variations. Therefore, increasing R_F serves two purposes: 1) it results in reduction of overall noise as evident from (2.17), and 2): it helps in reducing group delay variations, and hence increasing the vertical eye opening.

3.3 Circuit Realization of TI Stage

Fig. 3.3 shows the circuit level fully differential realization of the TI stage proposed in Fig. 3.2. Each of the two inductors introduces a zero in each path. A differential pair is used owing to its better CMRR, PSRR and linearity as compared to the single-ended counterparts. It is important to note that further bandwidth extension techniques can be employed on top of the inductor peaking to further enhance the bandwidth. These techniques include cascoding and capacitive degeneration peaking. However, these are not the main focus of this design and hence not analyzed here.

As discussed before, R_F is limited by the transimpedance limit given by (2.23) in conventional shunt-feedback transimpedance stage. For realization in the 90 nm GF-9HP BiCMOS technology of Global Foundries (f_T = 310 GHz), R_F should be as low as 350 Ω to achieve a bandwidth of 50 GHz from the first stage so that it can be extended to 100 GHz by post-equalization. In proposed design, this value of R_F is doubled to 700 Ω by increasing the amount of damping to remove unwanted gain peaking. Fig. 3.4 shows these frequency responses. Therefore, the proposed design achieves a transimpedance that is double that of a conventional design without significant gain peaking and deterioration of its bandwidth. This will essentially reduce the overall noise as given by (2.17).

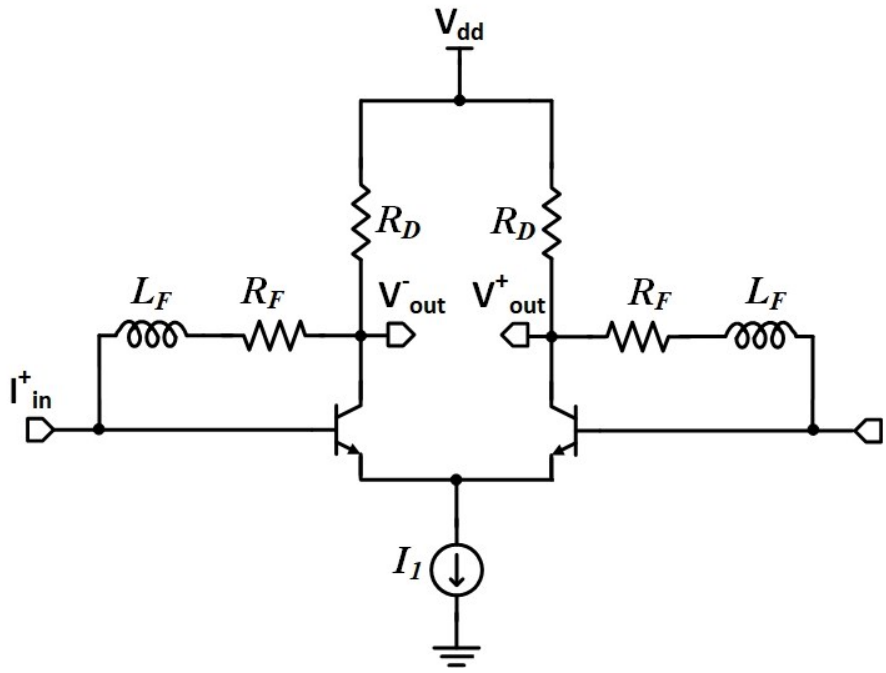


Fig. 3.3: Circuit diagram of the proposed shunt-feedback TI stage.

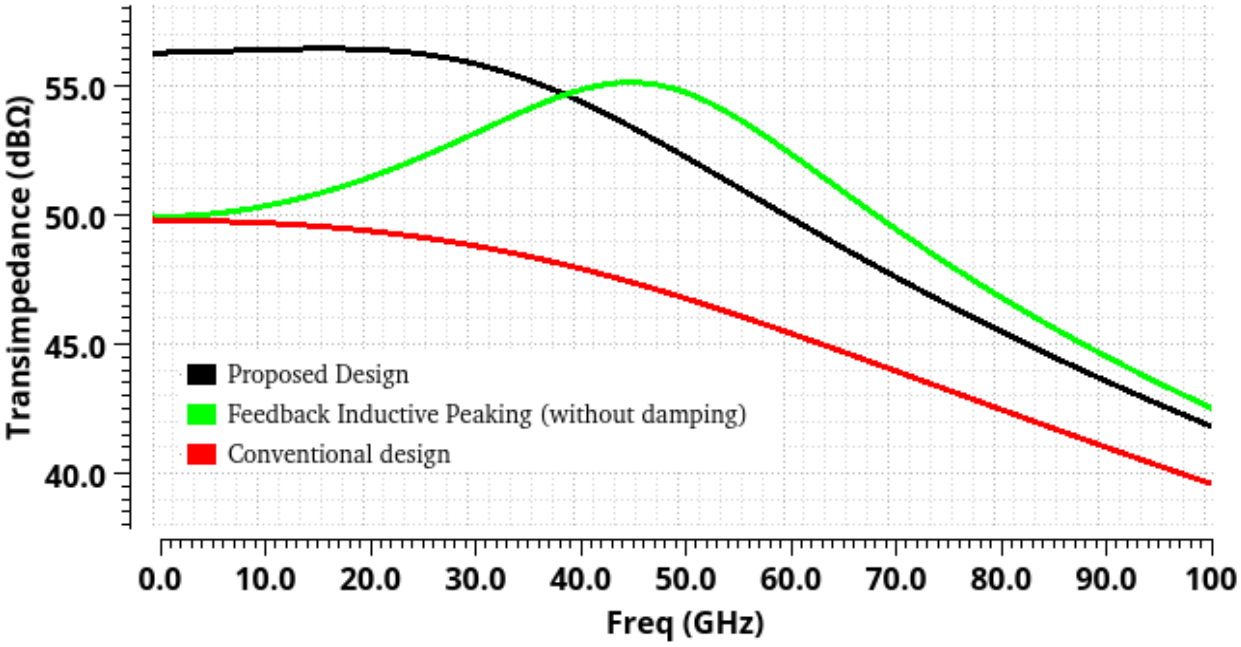


Fig. 3.4: Frequency response comparison of transimpedance stages.

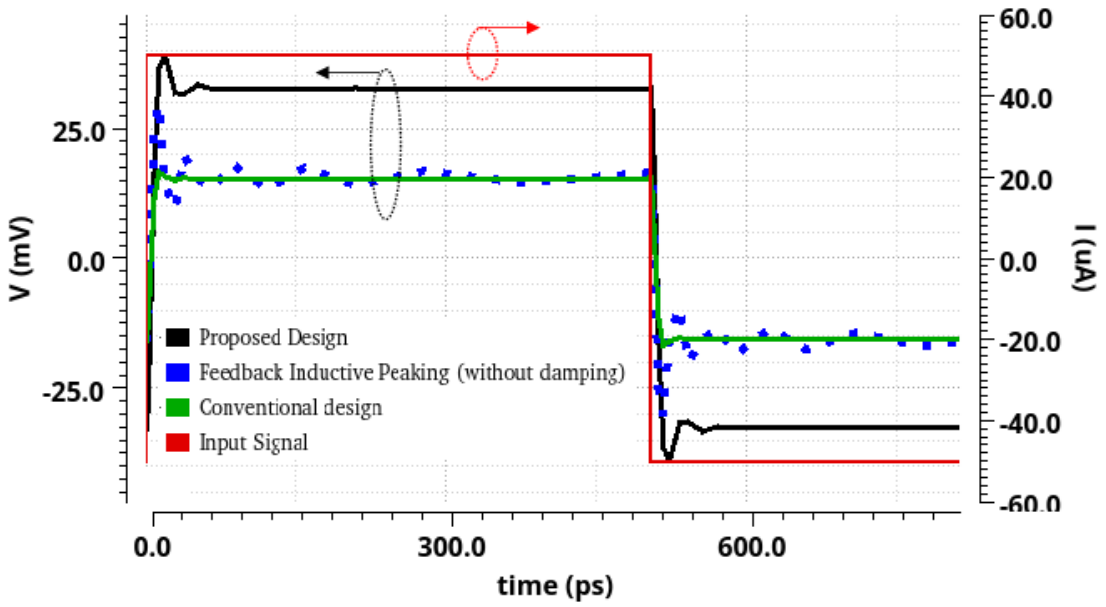


Fig. 3.5: Step response comparison of transimpedance stages.

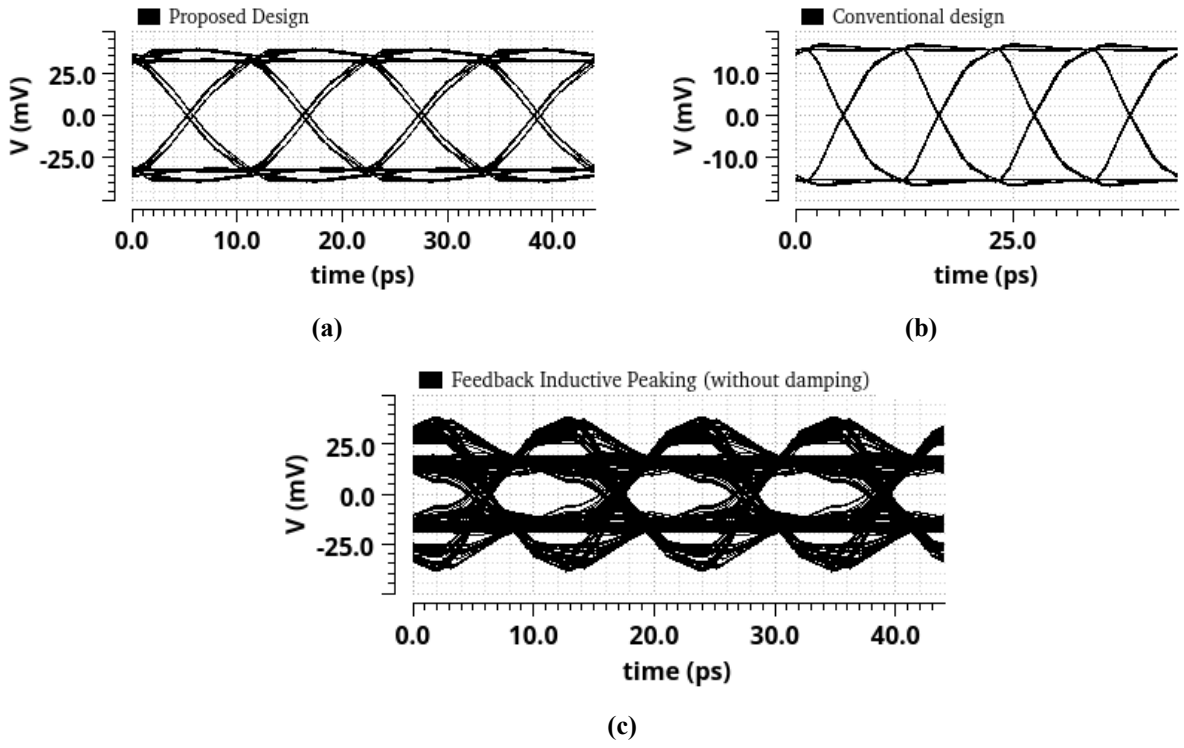


Fig. 3.6: Eye diagrams of transimpedance stage for 100 µApp 90 Gb/s NRZ PRBS31 input data stream. **(a)** Proposed design with R_F = 700 Ω. **(b)** Conventional design with R_F = 350 Ω. **(c)** Feedback Inductive Peaking (without damping) with R_F = 350Ω.

The step response comparison is shown in Fig. 3.5 which makes the effect of damping more obvious. An input signal of 100 µApp (where the subscript pp represents its peak-to-peak value)

is applied to each system. It is obvious that the conventional design is almost free from ringing but has very low transimpedance gain (R_F =350 Ω). The transimpedance stage with feedback inductive peaking without additional damping (R_F =350 Ω), has similar transimpedance gain as the conventional, but with significant ringing. Finally, the proposed damped design (R_F =700 Ω) has a transimpedance gain that is double than the conventional without any significant ringing.

Additionally, a 90 Gb/s NRZ PRBS31 data stream with an amplitude of 100-μApp was applied to each design and the resulting eye diagrams are shown in Fig. 3.6. Clearly, the vertical eye opening of the proposed damped system is double than that of the conventional implementation. Even though the bandwidth of the underdamped system is about twice the bandwidth of a conventional design, the vertical eye opening of the latter is greater. This implies that in addition to the bandwidth requirement, its group delay needs to be optimized as well to improve the system performance and increase the vertical eye opening.

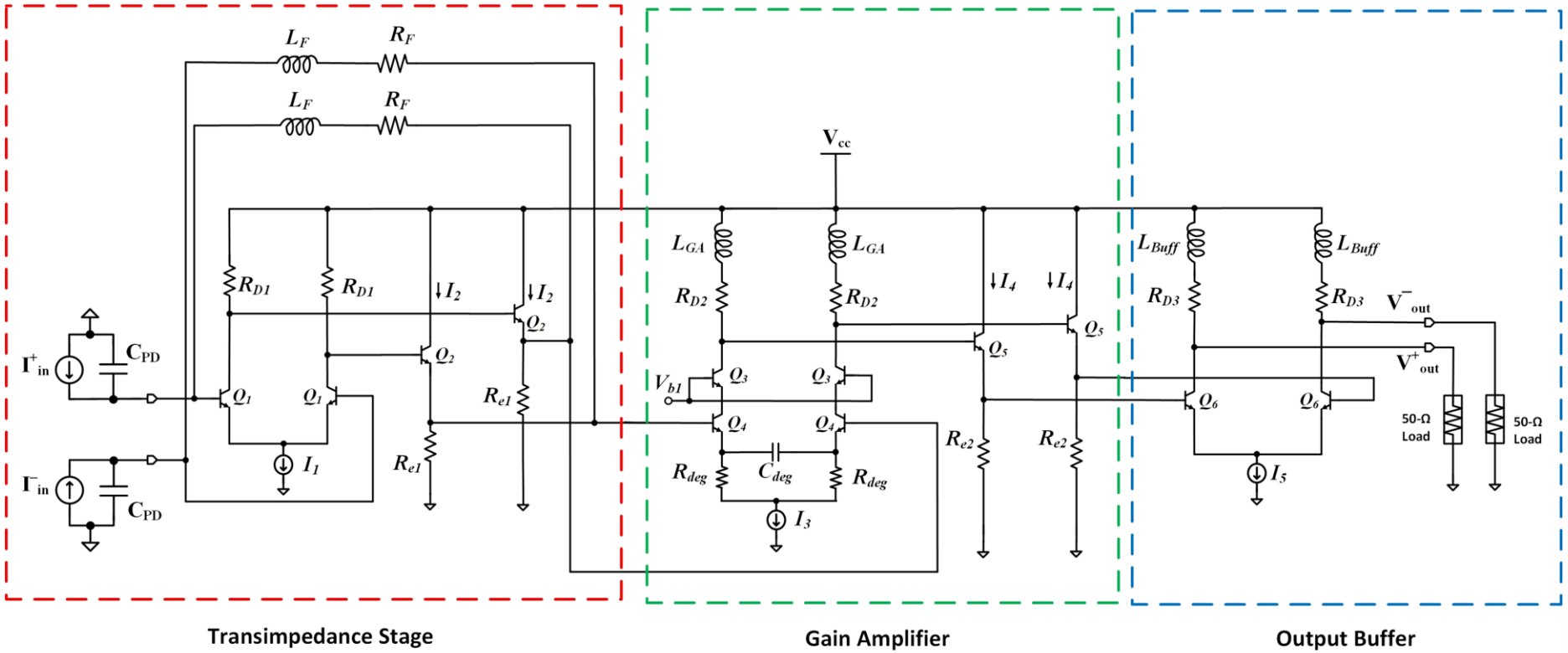


Fig. 3.7: Circuit diagram of proposed TIA design.

3.4 Circuit Realization of the Overall Proposed TIA Design

In addition to a front-end transimpedance design presented in Section 3.3, a CTLE approach is used in the overall design to increase its bandwidth. Fig. 3.7 shows the schematic diagram of overall TIA design proposed in this study. After the common-emitter based amplifier, emitter follower is used to reduce the output impedance of the shunt-feedback TI stage. This reduces the bandwidth loss upon connection with subsequent gain amplifier stages.

The gain amplifier is implemented as a fully differential cascode of CE and CB amplifiers. Use of CB cascode stage enhances the bandwidth because of its better high frequency response [17]. Inductive peaking and capacitive degeneration is implemented by L_{GA}, C_{deg} and R_{deg} which provides high frequency peaking to aid the post-amplifier equalization. Emitter follower is again used as buffer between gain amplifier and output buffer to avoid bandwidth loss. Finally, the output buffer is implemented using a CE fully-differential stage. This buffer is designed to provide an output impedance of 50 Ω. Inductive peaking is used again in the buffer stage to provide high frequency peaking and to compensate the effects of output bond pad capacitance and wirebonds of the packaged IC. R_F is increased from 700 Ω to 950 Ω based on simultaneous BW and group delay tuning.

3.5 Simulation Results

For verification of the proposed methodology, the TIA arrangement of Fig. 3.7 was implemented in the GF-9HP 90 nm BiCMOS technology and its simulated performance will be presented in this section.

All simulations include a photodiode model of 65 fF capacitor with a 165 pH inductor as bond pad inductance as used in [7] and [9].

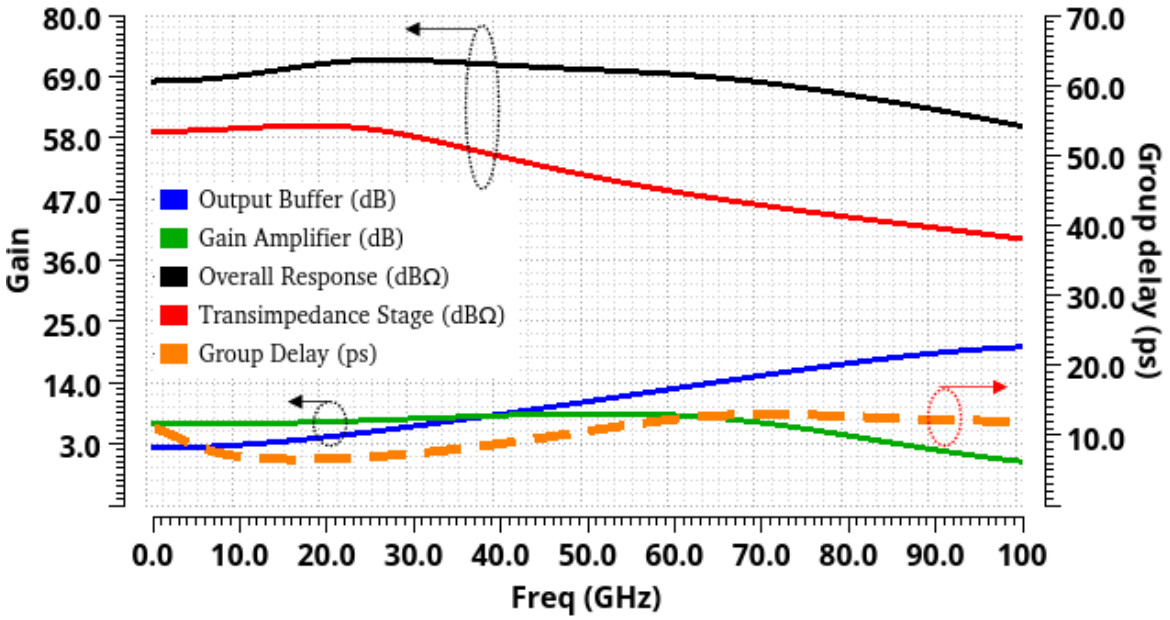


Fig. 3.8: Frequency response of individual stages along with group delay variation.

Fig. 3.8 shows frequency response of different stages within the TIA along with overall response. The TIA achieves a transimpedance of 68 dBΩ and a bandwidth of 83 GHz with a group delay variation (GDV) of ± 3.5 ps. Eye diagram of the overall TIA for 100-µApp and 90 Gb/s NRZ PRBS31 input data stream is shown in Fig. 3.9. It has a peak-to-peak vertical eye opening of about 200 mV.

Output noise spectral density of the overall TIA is shown in Fig. 3.10 which gives the output RMS noise value of 1.86 mV. Input-referred RMS noise is estimated by dividing the output RMS noise with the total transimpedance gain (68 dBΩ). Finally, input-referred noise spectral density is obtained by dividing the input RMS noise with 83 GHz (bandwidth of the TIA) which gives a value of 2.32 pA/√Hz. Table 3.1 compares the performance of the proposed design with the state-of-the-art. Wherever possible, the simulated results are cited from reference designs for the sake of fair comparison with the proposed design. Clearly, the proposed design outperforms the recent

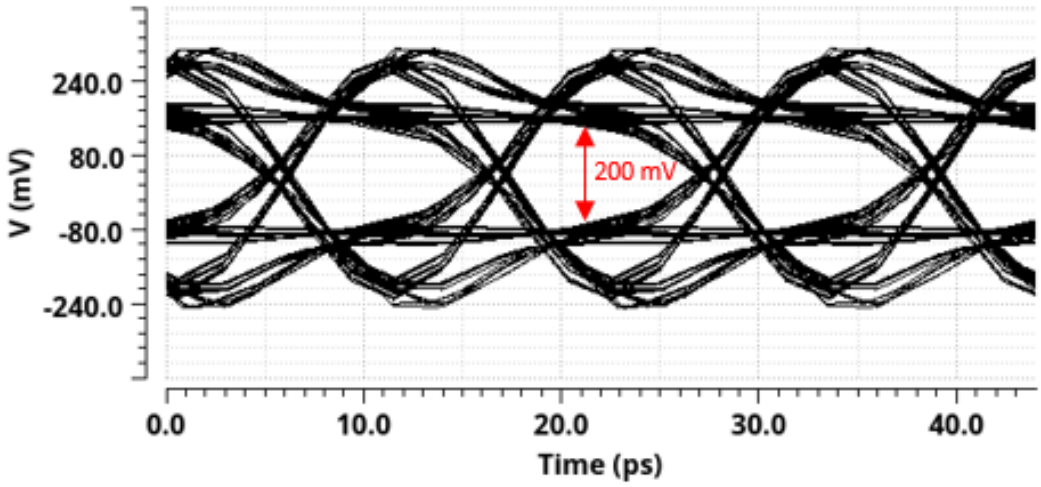


Fig. 3.9: Eye diagram of the overall TIA for 100 µApp and 90 Gb/s NRZ PRBS31 input data stream.

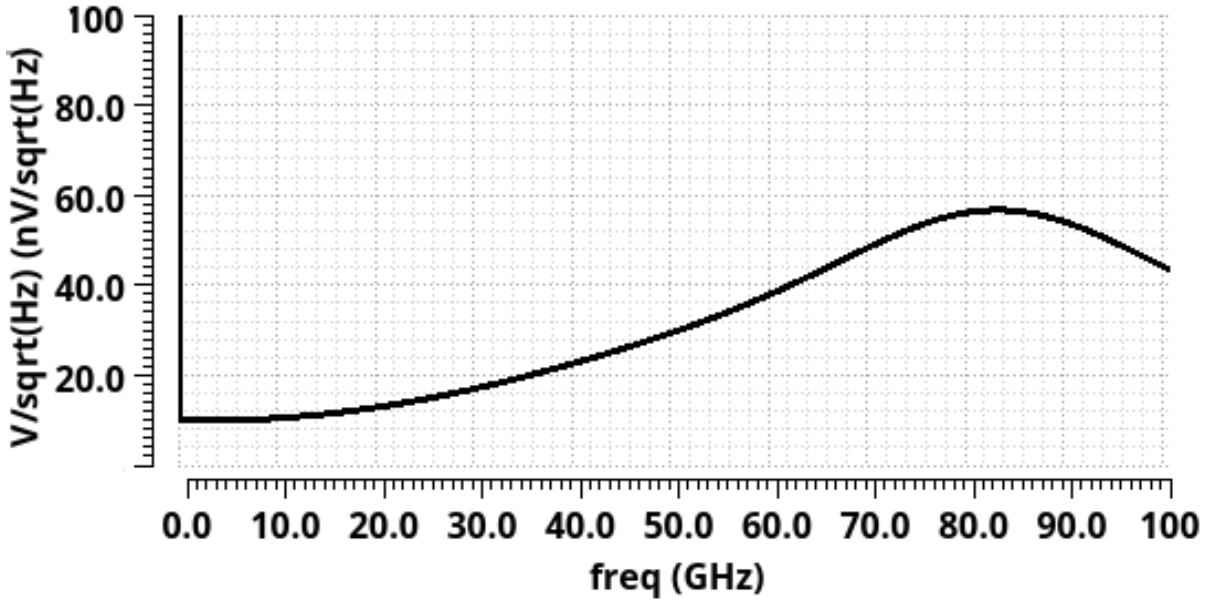


Fig. 3.10: Output noise voltage spectral density.

TIA designs in key performance parameters like BW, noise, group delay variation and transimpedance.

TABLE 3.1

PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART TIAS

Reference / Year	[7] / 2017	[8] / 2021	[9] / 2021	This / 2022
f_T (GHz)	300	300	300	310
C_{PD} (fF)	N/A	65	65	65
BW (GHz)	66 [b]	65 [a]	76 [b]	83 [b]
TI (dBΩ)	66 [b]	71 [a]	70 [b]	68 [b]
Noise (pA/√Hz)	7.6 [a]	7.2 [a]	6.3 [a]	2.32 [b]
GDV (ps)	± 5 [b]	± 4 [a]	± 4 [b]	± 3.5 [b]
DC Power (mW)	150	345	145	116

[a.] Measured results. [b.] Simulated results.

3.6 Summary

The proposed design simultaneously optimizes the noise, transimpedance and bandwidth of a transimpedance amplifier. This approach provides a path forward for the development of high speed, high-input sensitivity, and low-noise TIA circuits to serve the needs of modern optical communication equipment. The proposed technique can be used to achieve lower levels of input-referred noise without compromising bandwidth or it can be used to achieve higher bandwidth without any deterioration in the input-referred noise. Additionally, this technique offers efficient compromise between the chip area and noise by including peaking inductors within the feedback loop. In the future work, a chip targeting beyond 100 GHz applications will be manufactured based on this proposed design for experimental verification.

4 A Multi-Stage RC Compensation Technique for Decoupling the Transimpedance and Bandwidth

In this chapter, a multi-stage amplifier with an RC compensation scheme will be proposed as the open-loop amplifier for a closed-loop shunt-feedback-based TI stage. It will be shown that with the appropriate pole-zero positioning, the DC transimpedance gain can be decoupled from the closed-loop TI bandwidth. As a result, without the need for area consuming inductors, a TI stage can be realized which can have a transimpedance limit that is larger than the limit proposed by Säckinger in [4], which is discussed in Section 3.1.

As explained in [4], different circuits have different transimpedance limits. For instance, a cascade of *N* amplifiers with identical poles has the following open-loop transfer function

$$A(s) = \frac{A_o^N}{(1 + {}^{s}/_{\omega_p})^N} \tag{4.1}$$

Circuit analysis reveals that for a Butterworth closed-loop response, the circuit of Fig. 3.1 has a *transimpedance-N+1-power-bandwidth product* of

$$R_{T,limit,Nstage} \times BW_{CL}^{N+1} = \frac{f_t^N}{2\pi C_{in}} \tag{4.2}$$

and a transimpedance limit of

$$R_{T,limit,Nstage} = \frac{f_t^N}{2\pi C_{in} BW_{CL}^{N+1}} \tag{4.3}$$

Under closed-loop bandwidth conditions set less than f_t, the ratio of the transimpedance limit of an N-stage amplifier versus a single-stage amplifier is

$$\frac{R_{T,limit,Nstage}}{R_{T,limit,1stage}} = \left(\frac{f_t}{BW_{CL}}\right)^{N-1} \tag{4.4}$$

Here one can see that an N-stage open-loop amplifier configuration will be capable of achieving a higher transimpedance limit than one that uses a single-stage amplifier configuration. This provides the motivation to use a multi-stage cascade to implement the TI stage.

In addition to the use of multi-stage cascade, if the proposed RC compensation scheme is also used in the TI stage, then the transimpedance can be effectively decoupled from the bandwidth. This means that for an N stage cascade, the TI limit can be enhanced by a bigger factor than that given by (4.4). This will be elaborated in next sections.

4.1 Decoupling the Transimpedance and Bandwidth

The transimpedance analysis of Säckinger on a range of TIAs in [4] was limited to open-loop amplifiers with only real-valued repeated poles. As such, it was shown in [4] that with any increase in the low frequency transimpedance level, the bandwidth deteriorates by a factor proportional to R_F^{N+1}, where N is the number of stages connected in cascade.

In this section, it will be shown that if an additional zero and pole is introduced in the transfer function of the open-loop amplifier, the bandwidth can be made independent of the R_F. This will allow use of larger R_F for same targeted bandwidth.

Consequently, based on the noise analysis of the Section 2.2 and Section 2.3, increase in R_F will allow reduction in the output noise RMS level while increasing its bandwidth and low frequency transimpedance level.

In this work, a two-stage amplifier will be analyzed to avoid discussion of the stability needs of high-order multi-stage designs, i.e., N>2. Nonetheless, the principles discussed here also apply to these higher order systems.

Consider a two-stage amplifier having two coincident real-valued poles at ω_{p1} as in the conventional Säckinger's transfer function of (4.1) but having an additional zero at $s = -1/C_{in}R_F$ and another real pole at ω_{p2}. The pole at ω_{p2} is introduced to ensure a maximally flat Butterworth response in a closed-loop configuration. The zero at $s = -1/C_{in}R_F$ is introduced to eliminate the presence of the term created by C_{in} and R_F in the characteristic equation of the closed-loop transfer function. Consequently, the transfer function of the open-loop amplifier can be expressed as follows

$$A(s) = A_o^2 \frac{(1 + sC_{in}R_F)}{(1 + {}^{s}/_{\omega_{p1}})^2(1 + {}^{s}/_{\omega_{p2}})} \tag{4.5}$$

The resulting closed-loop transfer function is then given as

$$\frac{V_o(s)}{I_{in}(s)} = \frac{-R_F\omega_{p2}{\omega_{p1}}^2{A_o}^2}{\left[\begin{matrix} s^3 + s^2(2\omega_{p1} + \omega_{p2}) + s({\omega_{p1}}^2 + 2\omega_{p1}\omega_{p2}) \\ + {\omega_{p1}}^2\omega_{p2}({A_o}^2 + 1) \end{matrix}\right]} \tag{4.6}$$

Replacing $A_o\omega_{p1} = 2\pi f_t$ and using ${A_o}^2 + 1 \approx {A_o}^2$, the 3-dB bandwidth of this closed-loop system can be identified as

$$BW_{CL} \leq \left[\frac{{f_t}^2 \omega_{p2}}{2\pi}\right]^{1/3} \tag{4.7}$$

The equality is reached in (4.7) for a maximally flat Butterworth response. Therefore, the open-loop transfer function (4.5) results in a closed-loop transfer function whose bandwidth is independent of R_F. This is not surprising given that R_F no longer appears in the denominator term of (4.6).

Furthermore, if instead of two coincident real-poles in (4.5), two complex conjugate poles are used, the resulting bandwidth of the closed-loop system will be greater than that in (4.7) while still being independent of R_F. Such an amplifier having two complex-conjugate poles is defined as follows

$$A(s) = \frac{A_o^2\,(1 + sC_{in}R_F)}{(1 + \frac{s}{\omega_{p1}(1 + j\eta)})(1 + \frac{s}{\omega_{p1}(1 - j\eta)})(1 + {}^{s}/_{\omega_{p2}})} \tag{4.8}$$

Here the term η accounts for the separation distance between the real and imaginary parts of the complex-conjugate poles, i.e.,

$$\eta \triangleq \left|\frac{imag\ part\ of\ pole}{real\ part\ of\ pole}\right| \tag{4.9}$$

This parameter will become the central focus for the design of high-speed TIA circuits and will be referred to as the complex pole spreading factor.

The resulting closed-loop transfer function for this circuit is given as follows

$$T(s) = \frac{V_o(s)}{I_{in}(s)} = \frac{{A_o}^2 R_F}{\left\{ \begin{array}{c} \dfrac{s^3}{{\omega_{p1}}^2 \omega_{p2}(1+\eta^2)} + s^2 \left[\begin{array}{c} \dfrac{2}{\omega_{p1}\omega_{p2}(1+\eta^2)} \\ + \dfrac{1}{{\omega_{p1}}^2(1+\eta^2)} \end{array} \right] \\ + s\left[\dfrac{2\omega_{p1}}{{\omega_{p1}}^2(1+\eta^2)} + \dfrac{1}{\omega_{p2}} \right] + {A_o}^2 + 1 \end{array} \right\}} \tag{4.10}$$

In closed-loop operation, the 3-dB bandwidth of this system is given as

$$BW_{CL} \leq \left[\frac{{f_t}^2 \omega_{p2}(1+\eta^2)}{2\pi} \right]^{1/3} \tag{4.11}$$

Once again, the equality is reached in (4.11) for a maximally flat Butterworth response. As is evident, the bandwidth of the complex-conjugate pole system remains independent of R_F. Further, this bandwidth is greater than that of the repeated real poles transfer function by a factor of about $\sqrt[3]{\frac{\omega_{p2,complex\ poles}}{\omega_{p2,real\ poles}}(1+\eta^2)}$. Consequently, a greater closed-loop bandwidth is possible for any R_F from the circuit of Fig. 3.1 if the open-loop amplifier has complex conjugate poles and a zero located at $s = -1/C_{in}R_F$.

4.1.1 Validation of hypothesis via numerical example

To demonstrate the bandwidth enhancements claimed in previous section, the TIA circuit of Fig. 3.1 will be analyzed here for four different open-loop amplifier configurations. For a fair comparison, the DC gain for all systems is fixed at 25 V/V and the corresponding technology dependent dominant parasitic pole is fixed at 20 GHz. The latter places an upper bound on the placement of poles or zeros set by the compensation network and components of the amplifier.

Firstly, the amplifier configuration of (4.5) is considered which consists of two co-incident real-valued LHP poles at $\omega_{p1} = 20\,\text{GHz}$ and a real-valued left-half plane zero at $1/C_{in}R_F$.

Another real valued left-half plane pole is placed at $\omega_{p2} = 0.27$ GHz to ensure a non-peaked magnitude response in the closed loop. The value of C_{in} is set to a typical photodiode capacitance of 65 fF while R_F will be changed for different tests in this example. The corresponding open loop transfer function for (4.5) with R_F explicitly shown is

$$A(s) = \frac{25 \times (1 + s \times 65\text{x}10^{-15} R_F)}{(1 + \frac{s}{2\pi \times 20\text{x}10^{9}})^2 (1 + \frac{s}{2\pi \times 2.7\text{x}10^{8}})}. \tag{4.12}$$

A second open-loop amplifier having the general form as (4.5) is considered. Here the transfer function is given the same DC gain as the previous case but instead of two repeated real poles, it has two complex-conjugate poles but with the same real-value of $\omega_{p1} = 20$ GHz and a pole spreading factor η = 1. The real-valued zero is placed at the same location of $1/C_{in}R_F$. The real-valued pole is located at $\omega_{p2} = 0.4$ GHz so that a Butterworth response is realized in the close-loop operation. The open loop transfer function of this system is given as

$$A(s) = \frac{25 \times (1 + s \times 65\text{x}10^{-15} R_F)}{\left[\begin{array}{c} \left(1 + \frac{s}{2\pi \times 4\text{x}10^{8}}\right)\left(1 + \frac{s}{2\pi \times 20\text{x}10^{9}(1+j)}\right) \times \\ \left(1 + \frac{s}{2\pi \times 20\text{x}10^{9}(1-j)}\right) \end{array}\right]} \tag{4.13}$$

Similarly, one can increase the bandwidth improvement factor by increasing the complex pole spreading factor to create a third case. To do this, η is increased to 2 in (4.13) and the single real-valued pole is changed to 0.57 GHz to ensure a closed-loop non-peaked magnitude response. The modified open loop transfer function becomes

$$A(s) = \frac{25 \times (1 + s \times 65\text{x}10^{-15} R_F)}{\left[\begin{array}{c}\left(1 + \frac{s}{2\pi \times 5.7\text{x}10^{8}}\right)\left(1 + \frac{s}{2\pi \times 20\text{x}10^{9}(1 + j2)}\right) \\ \left(1 + \frac{s}{2\pi \times 20\text{x}10^{9}(1 - j2)}\right)\end{array}\right]}. \tag{4.14}$$

It is interesting to compare the closed-loop operation of the above three transfer functions to the open-loop transfer function with a repeated pole proposed by Säckinger. The open-loop transfer function having a repeated pole at 20 GHz and a DC gain of 25 V/V would be described as

$$A(s) = \frac{25}{(1 + \frac{s}{2\pi \times 20\text{x}10^{9}})^2}. \tag{4.15}$$

Without the real-value zero used in the previous three cases, a closed-loop Butterworth response is only possible for R_F equal to 10 kΩ in (4.15). This implies a TIA amplifier with a DC transimpedance of about 80 dBΩ. Fig. 4.1 compares the TIA closed-loop frequency responses for the above mentioned four open-loop amplifier configurations using a feedback resistor R_F of 10 kΩ. As is evident, all four circuit responses have the same low-frequency transimpedance of 80 dBΩ. It is also clear from this figure that the complex pole response with the largest pole spreading factor of $\eta = 2$ (red color line) has the highest bandwidth at 40 GHz. Next, the complex poles with $\eta = 1$ (green color line) has the next highest bandwidth of 20 GHz. The bandwidth of the two cases that use repeated poles seem to have similar bandwidths of 12 GHz (blue color line and black color line).

It is therefore reasonable to conclude that an open-loop response with complex poles provide a much higher bandwidth than one with repeated real poles. One can also conclude that the higher the complex pole spreading factor η, the higher the bandwidth.

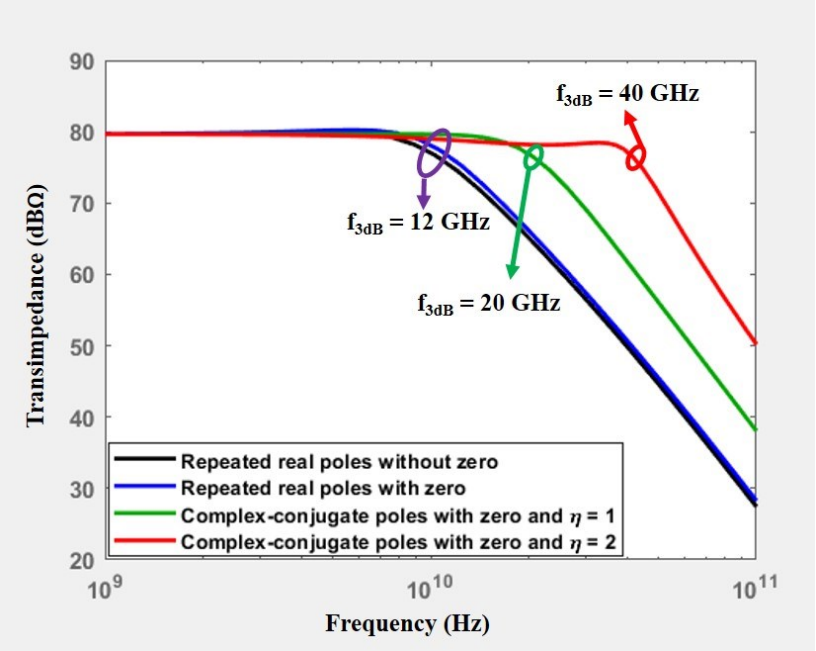


Fig. 4.1: Comparing the frequency response behavior of four different open-loop transfer functions: repeated real poles without zero, repeated real poles with a zero, complex poles having η=1 with a zero, and complex poles having η=2 with a zero. R_F is set to 10 kΩ.

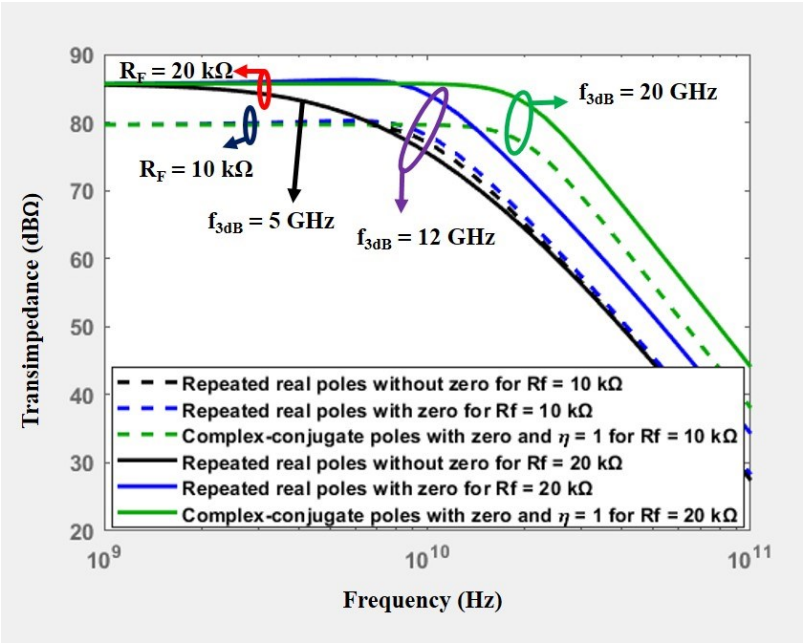


Fig. 4.2: Observing the effect of R_F on the 3-dB bandwidth and DC gain of three different open-loop transfer functions: repeated real poles without zero, repeated real poles with zero and complex poles with zero having η=1.

Finally, to demonstrate the insensitivity of the TIA closed-loop operation to the feedback resistor R_F value, consider comparing the frequency response of the TIA subject to different open-loop responses with and without the zero at $s = 1/C_{in}R_F$ and for varying values of R_F. This comparison will be repeated for R_F equal to 10 kΩ and 20 kΩ. Three different open-loop transfer functions will be used in this comparison. One with repeated real poles without a zero (Sackinger proposal in [4] given by (4.15)), another with repeated real poles with a zero as described by (4.12) and another with complex poles having η=1 and a zero as described by (4.13).

The results are shown in Fig. 4.2. As is evident, the bandwidth of the TIA with an open-loop transfer function containing a zero is invariant to the feedback resistor R_F value. This includes the open-loop transfer functions with repeated real poles with a zero (blue line), and one with complex-poles and a zero (green line). Specifically, for the repeated real-pole case with zero, one sees for R_F = 10 kΩ, the bandwidth is 12 GHz for a DC gain of 80 dBΩ. However, with R_F = 20 kΩ, the bandwidth is again 12 GHz for a DC gain of about 86 dBΩ. Likewise, for the complex poles case with a zero, the bandwidth is 20 GHz for a DC gain of 80 dBΩ. However, with R_F = 20 kΩ, the bandwidth is again 20 GHz for a DC gain of about 86 dBΩ. However, implementing the TIA using an open-loop transfer function without a zero (black line, Sackinger proposal in [4]) is very sensitive to the feedback resistor R_F value. Specifically, the bandwidth can be seen to trade-off with its low-frequency gain. In the case of R_F = 10 kΩ, the 3-dB bandwidth is equal to 12 GHz and the DC gain is equal to 80 dBΩ. However, with R_F set to 20 kΩ, the bandwidth reduces to 5 GHz while the DC gain increases to about 86 dBΩ.

4.2 Open-Loop Amplifier with Complex Poles and a Zero

It is now time to turn our attention to the realization of an open-loop amplifier with complex poles and a zero. The circuit shown in Fig. 4.3 can be used to realize a voltage amplifier with

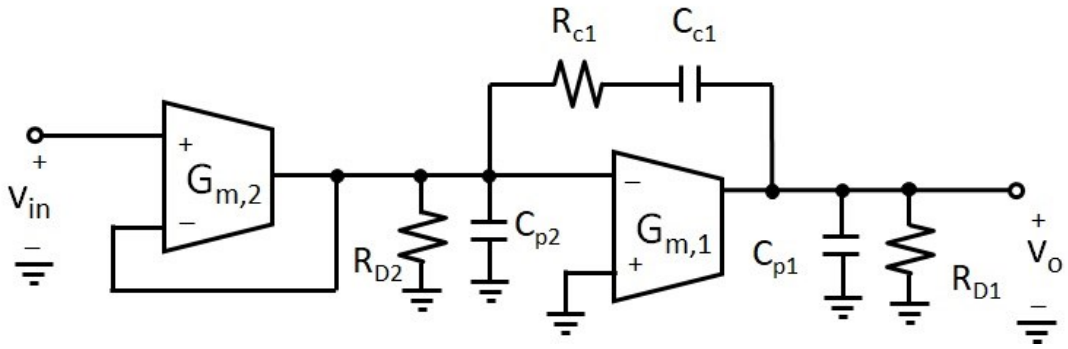


Fig. 4.3: Proposed multi-stage amplifier capable of realizing complex conjugate poles.

complex poles and a zero. It consists of a cascade of two transconductance (G_m) stages. The G_m stages are assumed to have a finite output resistance R_D and shunt capacitance C_p. It also includes a bridging RC network to establish the complex pole locations. The input-output transfer function for this circuit can be derived as

$$\frac{V_o(s)}{V_{in}(s)} = -\frac{G_{m1}R_{D1}\dfrac{G_{m2}R_{D2}}{G_{m2}R_{D2}+1}(\alpha s+1)}{\beta_3 s^3+\beta_2 s^2+\beta_1 s+1} \tag{4.16}$$

where

$$\alpha = C_{c1}R_{c1} - \frac{C_{c1}}{G_{m1}}$$

$$\beta_1 = \frac{\begin{pmatrix}\big((G_{m1}+G_{m2})R_{D1}+G_{m2}R_{c1}+1\big)C_{c1}\\ +C_{p1}G_{m2}R_{D1}+C_{p2}\end{pmatrix}R_{D2} + (R_{D1}+R_{c1})C_{c1}+R_{D1}C_{p1}}{G_{m2}R_{D2}+1} \tag{4.17}$$

$$\beta_2 = \frac{\begin{pmatrix}\Big(\big(C_{p1}G_{m2}R_{c1}+C_{p2}+C_{p1}\big)R_{D1}+C_{p2}R_{c1}\Big)C_{c1}\\ +C_{p1}C_{p2}R_{D1}\end{pmatrix}R_{D2} + C_{c1}C_{p1}R_{D1}R_{c1}}{G_{m2}R_{D2}+1}$$

$$\beta_3 = \frac{C_{c1}C_{p1}C_{p2}R_{D1}R_{D2}R_{c1}}{G_{m2}R_{D2}+1}$$

One can equate the denominator term of (4.16) to the desired position of the poles in the complex plane as

$$\beta_3 s^3 + \beta_2 s^2 + \beta_1 s + 1 = (1 + \frac{s}{\omega_{p1}(1+j\eta)})(1 + \frac{s}{\omega_{p1}(1-j\eta)})\left(1 + {}^{s}/_{\omega_{p2}}\right) \tag{4.18}$$

from which the β-terms can be identified as

$$\beta_3 = \frac{1}{{\omega_{p1}}^2(1+\eta^2)\omega_{p2}},$$

$$\beta_2 = \frac{2\omega_{p1} + \omega_{p2}}{{\omega_{p1}}^2(1+\eta^2)\omega_{p2}} \tag{4.19}$$

and

$$\beta_1 = \frac{\omega_{p1}(1+\eta^2) + 2\omega_{p2}}{\omega_{p1}(1+\eta^2)\omega_{p2}}$$

As the amplifier of Fig. 4.3 is intended for closed-loop operation in the circuit of Fig. 3.1, its input-output transfer function would take on the general form displayed in (4.10). Moreover, as the goal is to achieve a 3rd-order Butterworth response, the denominator polynomial in (4.10) must appear as

$$\left(\frac{s}{\omega_o}\right)^3 + 2\left(\frac{s}{\omega_o}\right)^2 + 2\left(\frac{s}{\omega_o}\right) + 1 \tag{4.20}$$

resulting in the following two constraint equations on the pole positions:

$$2\omega_{p1}\,(A_o+1){\omega_{p2}}^2 - 2\omega_{p2}{\omega_o}^2(A_o+1) = -{\omega_o}^3 \tag{4.21}$$

$$2\omega_{p1} + \omega_{p2} = 2\omega_o \tag{4.22}$$

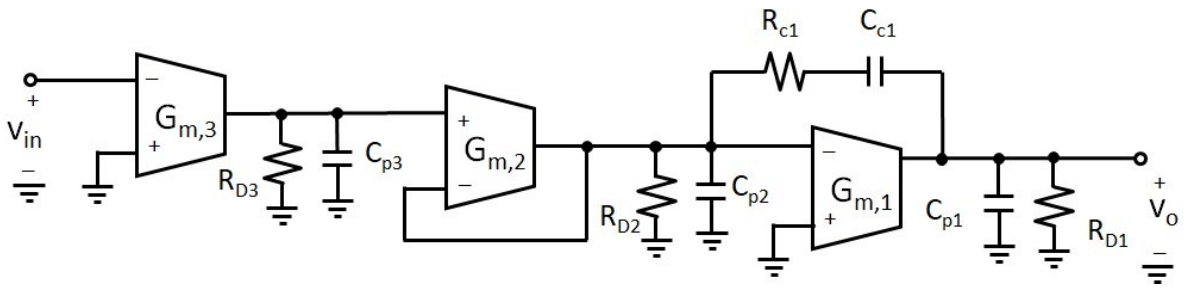
with $\omega_o = BW_{CL}/2\pi$.

For a particular open-loop gain (A_o) and a desired closed-loop bandwidth (BW_{CL}), ω_{p1} and ω_{p2} can be found as the simultaneous solution to equations (39) and (40). Further, the required complex pole spreading factor (η) is found by solving the following equation using the newly acquired information

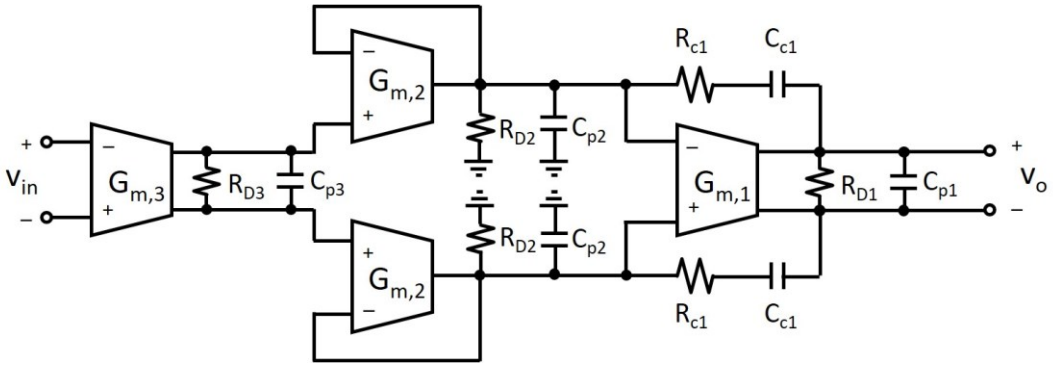
$$\eta = \sqrt{\frac{{\omega_o}^3}{(A_o + 1){\omega_{p1}}^2\omega_{p2}} - 1} \tag{4.23}$$

With ω_{p1}, ω_{p2} and η now determined, one can equate the β-terms in (4.17) with those in (4.19), together with the constraint on the zero location, i.e., $\alpha = C_{in}R_F$, and solve for the circuit parameters of Fig. 4.3 from the resulting nonlinear equations.

The circuit of Fig. 4.3 can be further enhanced by adding another gain stage G_{m3} at the front-end of the cascade structure. The resulting architecture is shown in Fig. 4.4(a). This additional gain stage serves two important purposes: *i)* it increases the open-loop low-frequency gain, and *ii)* it reduces the noise of the open-loop amplifier because, as shown by (2.17), the noise of any cascade architecture can be reduced by setting greater gain in the first stage. On contrary, if the transconductance stage involving G_{m2} is used as front-end stage, the noise of the open-loop amplifier will be high due to its unity gain feedback loop, which will directly increase the TIA input-referred noise as per (2.17). Moreover, the addition of G_{m3} introduces a pole at high frequency set by the parasitic capacitance C_{p3} and R_{D3}. Therefore, it will not affect the pole-zero distribution already mentioned.



(a)



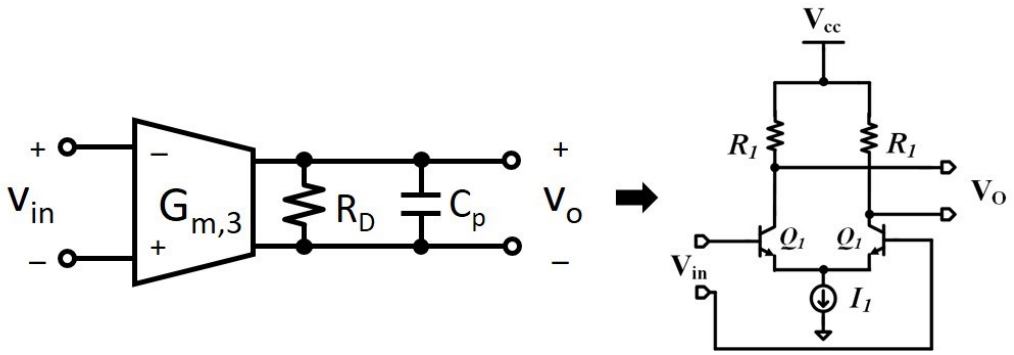
(b)

Fig. 4.4: Proposed multi-stage amplifier capable of realizing complex conjugate poles with additional gain stage G_{m3}. **(a)** single-end realization, and **(b)** fully differential realization.

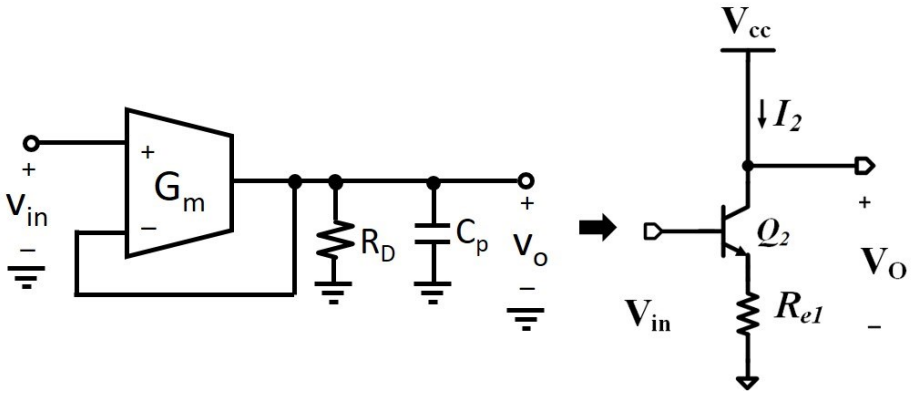
Extension to a fully differential realization is shown in Fig. 4.4(b). Here there are two types of transconductances stages identified. One type of G_m stage has a fully differential output and the other has a single-ended output together with unity-gain feedback.

4.3 Circuit Implementation

In terms of transistor realization, the fully differential transconductance stage of Fig. 4.4(b) can be realized using a resistive-loaded differential pair circuit as depicted in Fig. 4.5(a). Conversely, the single-ended transconductance stage with unity feedback can be realized using an emitter follower circuit as shown in Fig. 4.5(b).



(a)



(b)

Fig. 4.5: Two BJT arrangements of the transconductance stages of the multi-stage amplifier: **(a)** open-loop transconductance stage, and **(b)** closed-loop transconductance stage acting as a buffer.

Substituting these circuits into the open-loop transimpedance amplifier circuit of Fig. 4.4(b) and arranging the overall amplifier in the shunt-feedback arrangement of Fig. 3.1 results in the fully differential circuit shown in Fig. 4.6.

An important feature of this circuit is its ability to tune the position of the closed-loop poles and zero of the TIA circuit by adjusting the values of either R_{c1} or C_{c1} in the RC compensation network.

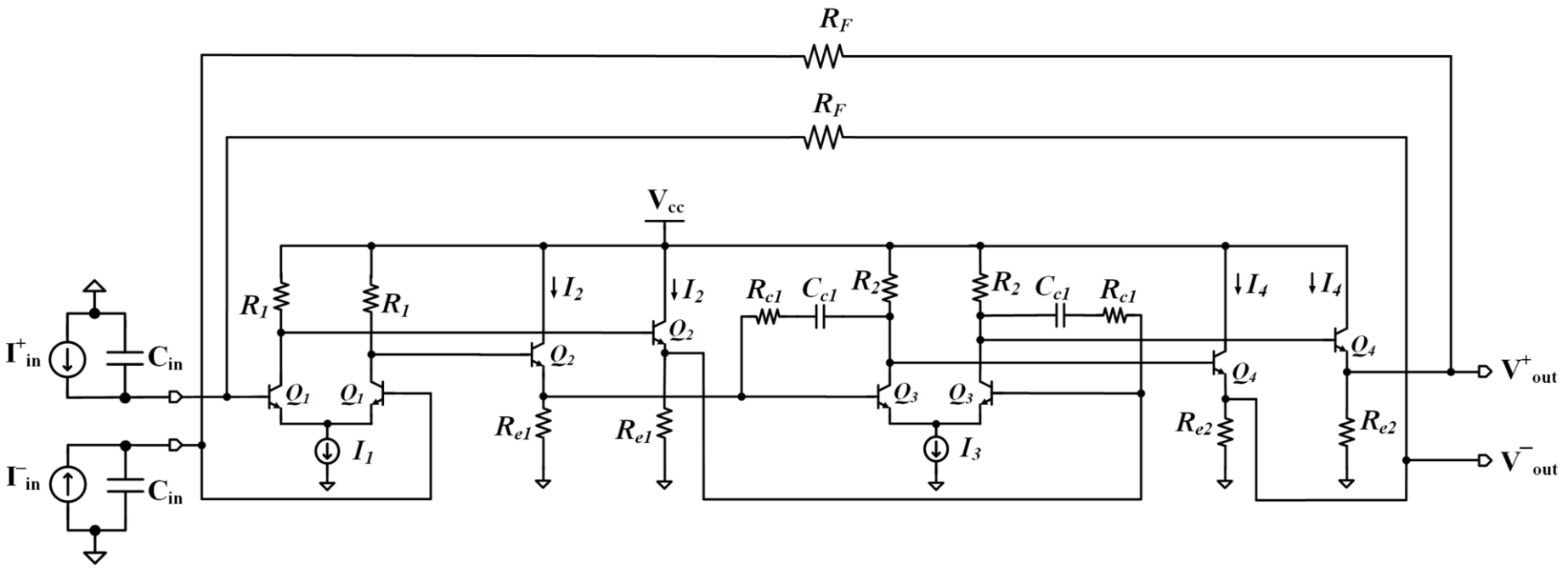
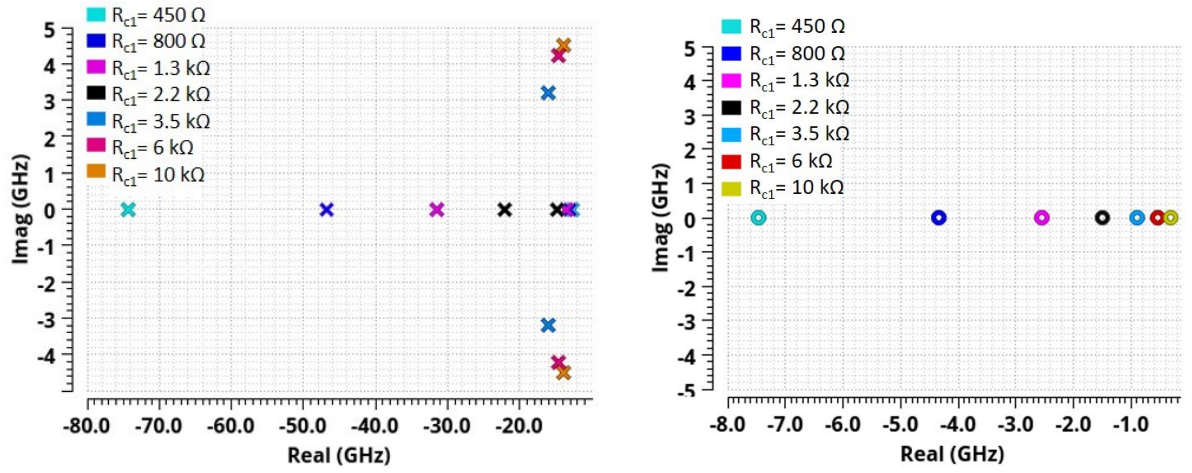


Fig. 4.6: Incorporating the transistorized realization of the multi-stage voltage amplifier of Fig. 4.4(b).

To demonstrate this capability, a test case was setup with $R_1 = R_2 = R_{e1} = R_{e2} = 1$ kΩ for simulation in Spectre using GF BiCMOS 9HP process node. With C_{c1} fixed to 50 fF, the value of R_{c1} was swept from 450 Ω to 10 kΩ and the position of the poles and zero of the closed-loop TIA circuit were computed using Spectre. The results are captured in the two s-plane pole and zero plots of Fig. 4.7. The position of two poles as a function of R_{c1} is shown in Fig. 4.7(a). As is evident, the pole plot consists of two poles that are real for $R_{c1} \leq 2.2$kΩ and become complex conjugate for $R_{c1}>2.2$kΩ. As R_{c1} increases, so too does the complex pole spreading factor, η.

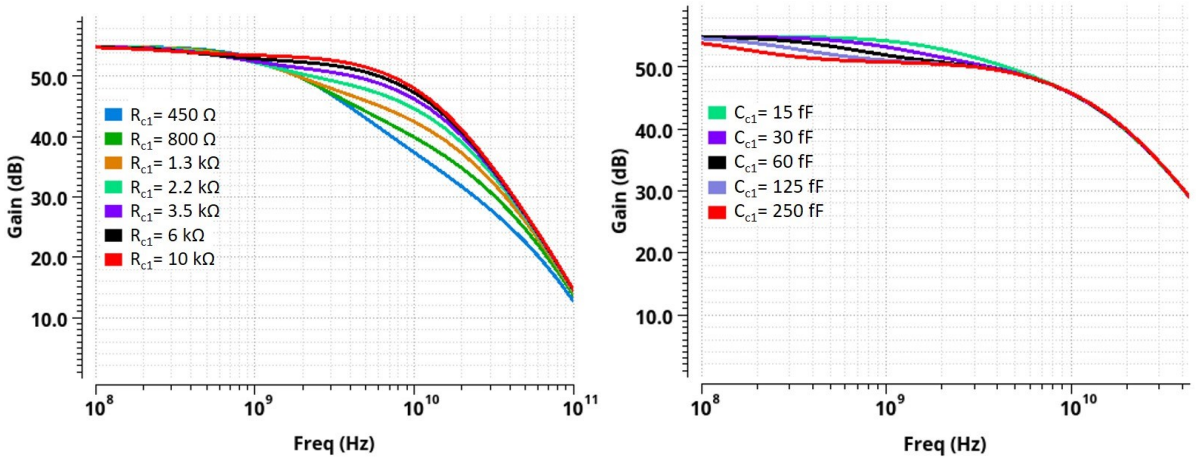
In the case of the real-valued zero, one can see from Fig. 4.7(b) that it moves downward in frequency with increasing value of R_{c1}. The impact of a change in R_{c1} on the magnitude response of the closed-loop behavior of the TIA circuit can be seen in Fig. 4.8(a). Here one sees that the effect on the pole-zero changes gives rise to an increasing 3-dB bandwidth with increasing R_{c1}. It is also interesting to see the effect of changes in C_{c1} when R_{c1} is held constant at 3 kΩ. This is shown in Fig. 4.8(b) for C_{c1} sweeping from 15 fF to 250 fF. Here, one sees that change in C_{c1} mainly affects the position of real-valued zero. Increase in C_{c1} decreases the frequency of the zero while change in C_{c1} has minimal effect on the positioning of poles. Therefore, tuning of R_{c1} and C_{c1} based on the closed loop specifications can give the desired pole-zero configuration in the open loop response.

The shunt-feedback TIA circuit of Fig. 4.6 was fabricated in the 90 nm Global Foundry SiGe BiCMOS 9HP process. This fabrication process was chosen for its high-f_t (310 GHz) and low-noise transistors, as the intent here is to design a closed-loop amplifier with a 3-dB bandwidth of



(a) **(b)**

Fig. 4.7: Effect of R_{c1} on the positioning of **(a)** complex conjugate poles, and **(b)** the real-valued zero with C_{c1} = 50 fF.



(a) **(b)**

Fig. 4.8: The effect of a change in the RC compensation network on the magnitude response of the open-loop amplifier: **(a)** subject to changes in R_{c1} alone with C_{c1}= 50 fF, and **(b)** subject to changes in C_{c1} alone when R_{c1} = 3kΩ.

approximately 34 GHz with low input-referred noise properties (0.87pA/√Hz). As per the author's best knowledge, this is the highest transimpedance stage bandwidth for this noise level.

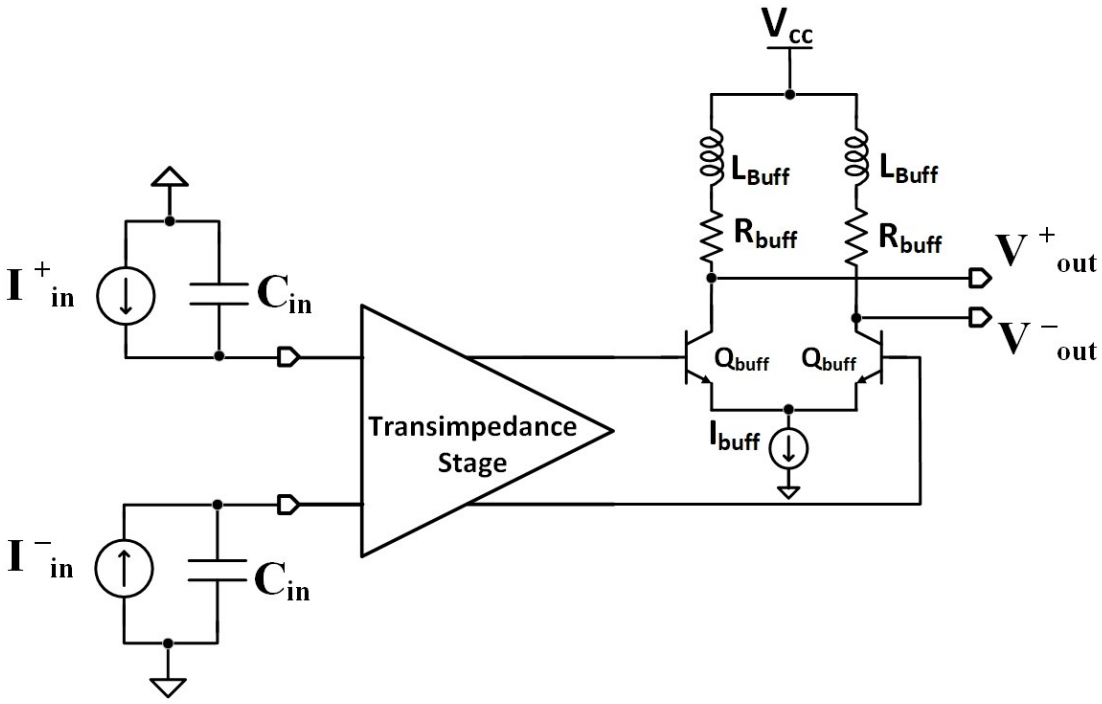


Fig. 4.9: Circuit details of the 50 Ω output voltage buffer with inductive peaking placed in cascade with the transimpedance stage.

4.4 Simulation Results

For a closed loop overall bandwidth of 34 GHz and transimpedance of 70 dBΩ in the presence of a photodiode having a parasitic capacitance of 65 fF (as used in [8] and [9]), the circuit of Fig. 4.6 was designed using the methodology of Section 4.2. The resulting circuit parameters for this design are summarized in table 4.1. Additionally, a 50 Ω output buffer stage follows the transimpedance stage so that the TIA can be connected in a 50 Ω balanced system. This buffer is implemented with a fully differential stage having a 50 Ω collector resistance and is shown in Fig. 4.9. Series inductors were used in the collectors of the resistive-loaded differential-pair amplifier to compensate for bond pads, wire bonds, and other packaging losses.

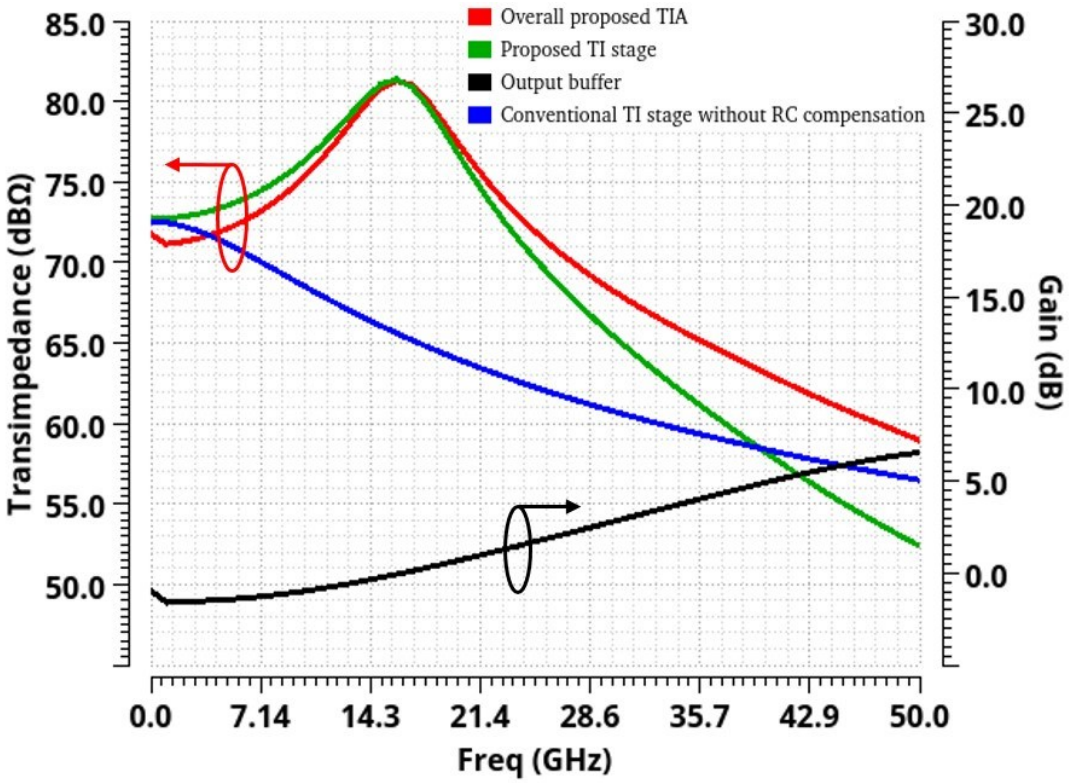


Fig. 4.10: The stage-wise and overall magnitude frequency response as predicted by the transistor level circuit simulations for the closed-loop TIA amplifier of Fig. 4.9 in single-ended operation along with the response of a conventional TI stage without RC compensation for same targeted overall gain.

The overall magnitude of the input-output frequency response of the proposed shunt-feedback TIA is shown in Fig. 4.10 along with stage wise responses of the transimpedance stage and the output buffer. Also included in this plot is the frequency response behavior of a conventional transimpedance stage implemented without the RC compensation scheme. Clearly, the proposed transimpedance stage achieves a higher bandwidth (28 GHz) as compared to the conventional design (8 GHz) for the same transimpedance gain (71 dBΩ). It is important to note that this bandwidth extension is achieved without using any inductors because the effect of peaking inductors of the buffer only appear in the overall response shown with red line in Fig. 4.10. These results were obtained through a transistor level simulation of the circuit using the Cadence Spectre

TABLE 4.1

COMPONENT VALUES USED IN THE TIA DESIGN

Parameter	Value	Parameter	Value
Technology	GF BiCMOS 9HP (90nm) (f_t =310 GHz)	Q_1-Q_4	1 x 0.1µm x 2µm
R_F	4.5 kΩ	Q_{buff}	3 x 0.1µm x 2µm
R_{c1}	3 kΩ	I_1	1.8 mA
C_{c1}	50 fF	I_2	1.4 mA
R_1/R_2	1 kΩ	I_3	2.7 mA
R_{e1} /R_{e2}	1 kΩ	I_4	1.1 mA
R_{buff}	50 Ω	I_{buff}	12 mA
L_{Buff}	550 pH (6µm x 3µm)		

simulation platform. Models for the transistors and other components were provided in the design kit associated with the Global Foundries SiGe BiCMOS 9HP process.

4.5 Experimental Validation

The TIA was fabricated in the BiCMOS GF-9HP process for experimental validation of the proposed circuit and design methodology. A die photograph of the fabricated chip is shown in Fig. 4.11.

Firstly, the TIA was fully characterized by measuring S-parameters using the Keysight N5247B PNA-X microwave network analyzer as illustrated in the setup of Fig. 4.12. For on-wafer probing, T-plus 5 pin ground-signal-ground-signal-ground-signal (GSGSG) probes with 110 µm pitch were used. Two Hewlett Packard E3631A variable DC power supplies were used in the experiment. One DC power supply was used to set V_{CC} of the chip to 3.3 V. The other power

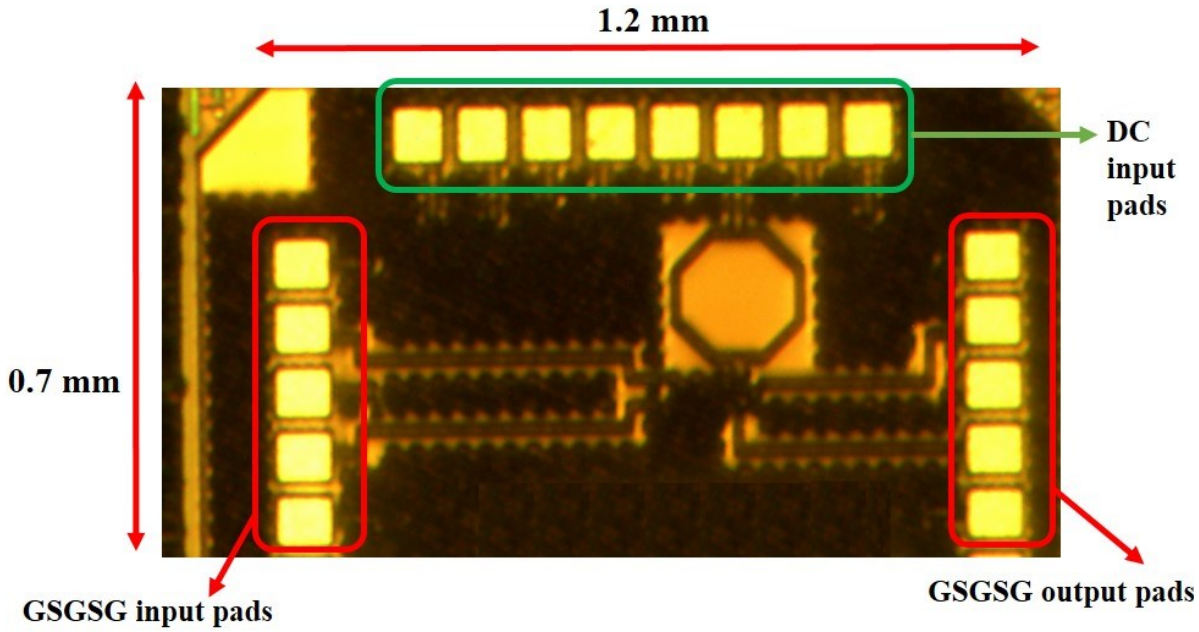


Fig. 4.11: Photograph of the TIA section of the chip.

supply was set to 10 V to power three separate linear voltage regulators (LT3085) operating as current sources. These current sources were used to generate the bias currents I_1 and I_3 associated with the two resistor-loaded differential pairs of Fig. 4.6 and I_{buff} for the bias current associated with the output buffer of Fig. 4.9.

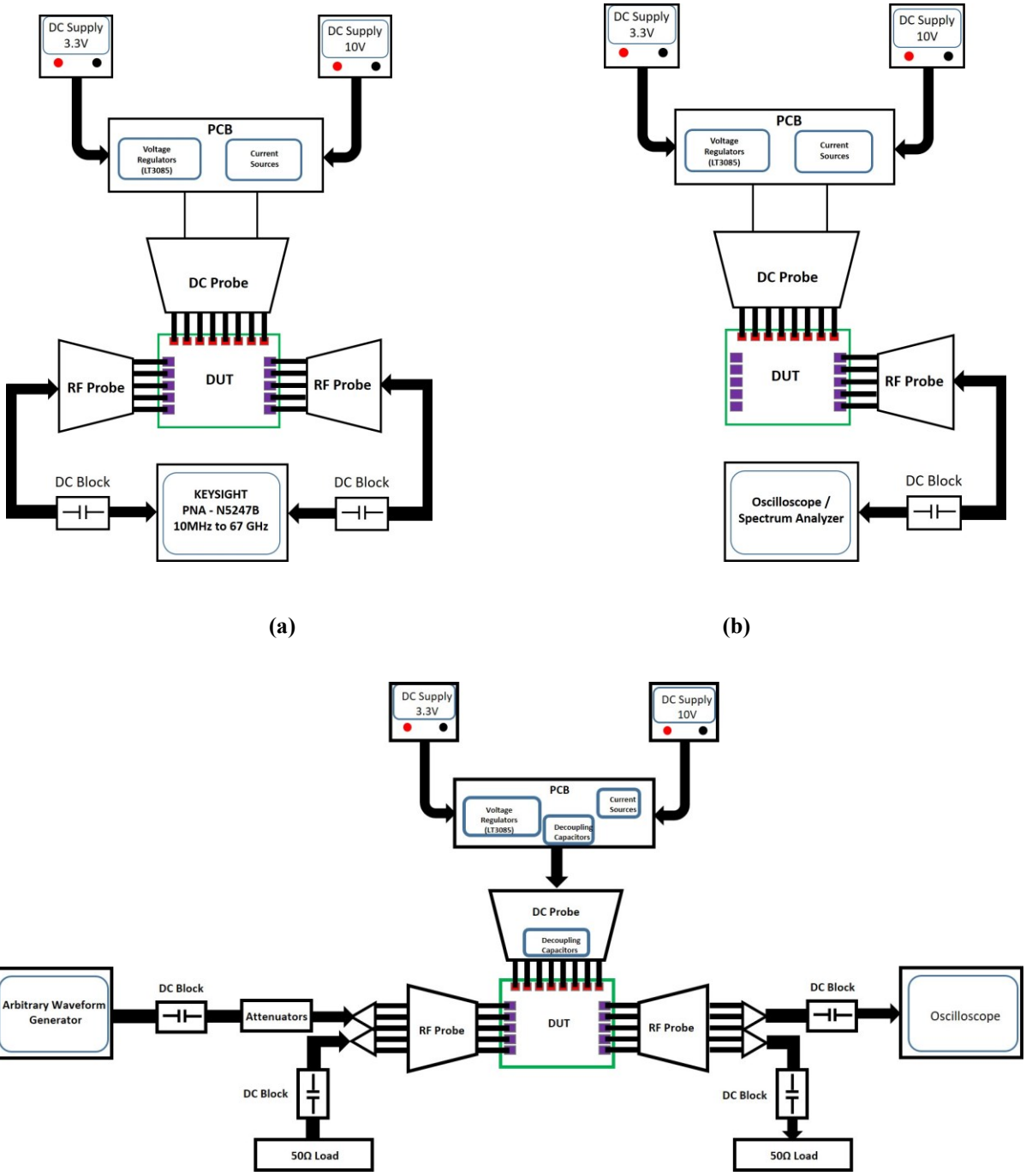


Fig. 4.12: Experimental setup for measurement of **(a)** the S-parameters of the TIA circuit using on-wafer probing, **(b)** the output noise voltage using a Spectrum Analyzer and Oscilloscope and **(c)** the eye diagrams for PRBS-31 NRZ data stream.

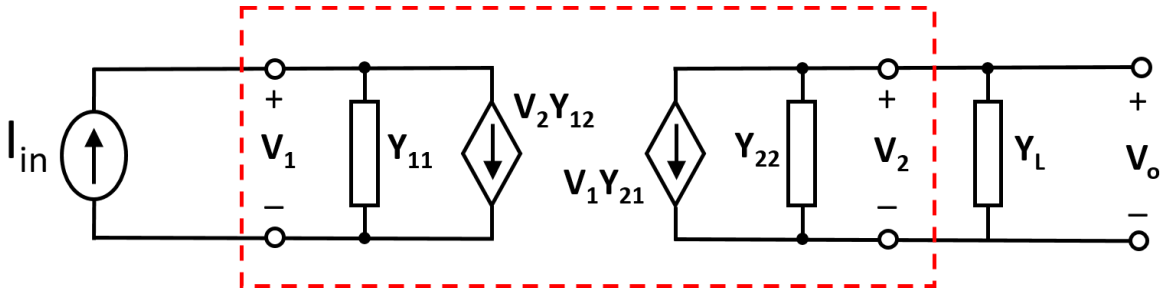


Fig. 4.13: A 2-port network represented in terms of Y-parameters and excited with photodiode current source for extraction of transimpedance gain.

The transimpedance gain was extracted from the measured S-parameters by using R_T (f) = V_{diff} / I_{diff} . To further elaborate the extraction of transimpedance gain from the S-parameters, consider the general 2-port network represented in terms of Y-parameters shown with dotted red lines in Fig. 4.13. This 2-port network is then excited with a photodiode which is modeled as current source. Circuit analysis of this configuration results in following relationship for transimpedance gain

$$TI = \frac{V_o}{I_{in}} = -\frac{Y_{21}}{Y_{11}(Y_{22} + Y_L) - Y_{12}Y_{21}} \tag{4.24}$$

Additionally, the Y-parameters can be converted to S-parameters using following relationships

$$Y_{11} = Y_L \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

$$Y_{12} = Y_L \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{4.25}$$

$$Y_{21} = Y_L \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

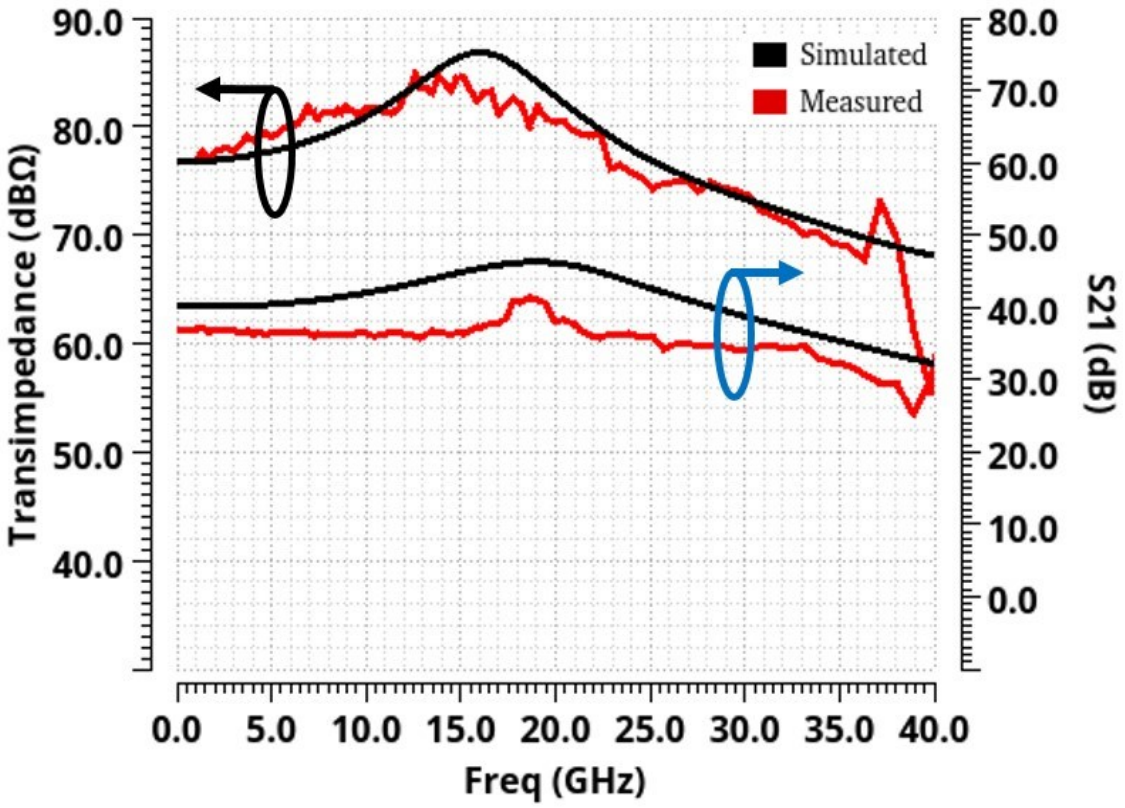


Fig. 4.14: Comparison of the measured and transistor level simulated frequency response of the TIA circuit in fully differential mode operation.

$$Y_{22} = Y_L \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$$

Finally, substituting (4.25) in (4.24) results in the following relationship between transimpedance and S-parameters

$$TI = \frac{V_o}{I_{in}} = \frac{S_{21}}{Y_L(1-S_{11})} \tag{4.26}$$

This transimpedance gain is compared with the simulated transimpedance in Fig. 4.14 along with the measured and simulated S_{21}. Clearly, the measured results are in close match with the post-layout simulation results. The measured S_{21} is only 3 dB less than the simulated while the bandwidth is same.

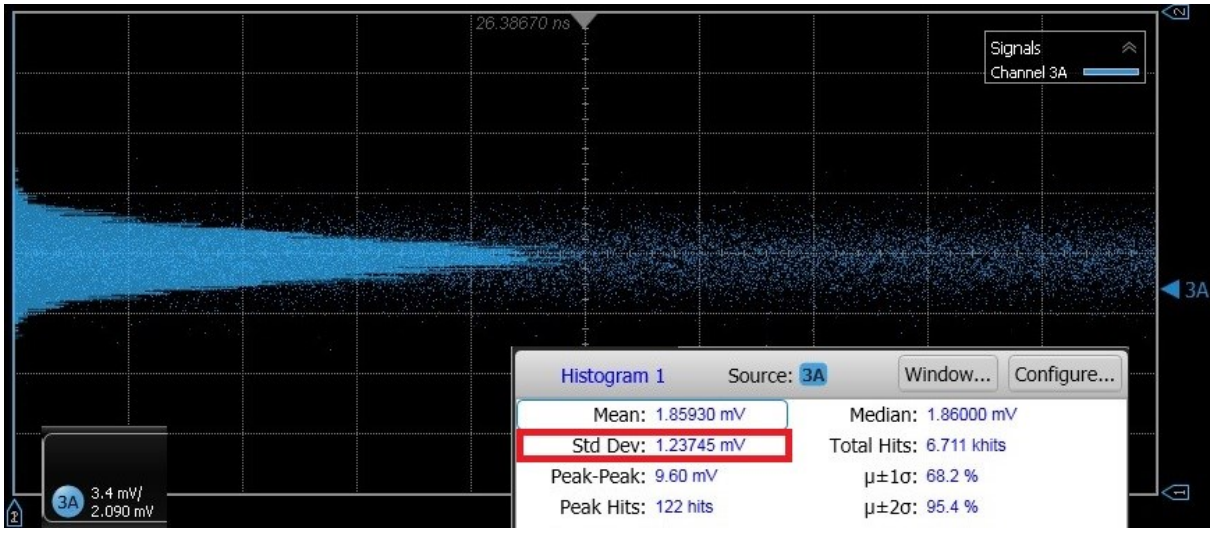


Fig. 4.15: Histogram of output noise voltage measured using digital sampling oscilloscope.

A second test setup involving a Keysight DCA-X 86100D digital sampling oscilloscope and Keysight N9040B Spectrum Analyzer was used to extract the noise properties of the TIA circuit. In the first case, the oscilloscope was used to extract a histogram of the output voltage noise from which the standard deviation of the noise voltage can be computed. In second case, the spectrum analyzer was used to measure the output noise voltage spectral density. The setup for these two tests is shown in Fig. 4.12 (b).

During each noise test, the inputs to TIA circuit were left open, while one of the differential outputs were terminated to 50 Ω resistor and noise was measured on the other output. Histogram of the output voltage noise obtained form the oscilloscope is shown in Fig. 4.15. The standard deviation of this histogram shows the equivalent output RMS noise voltage, which is 1.273 mV in this case. In order to de-embed the noise of measurement setup, the noise of the oscilloscope (1.12 mV) needs to be subtracted from the measured noise. Since the noise at the two outputs of the differential TIA and the noise of oscilloscope itself is high uncorrelated, the method of [18] and [7] was used to calculate the input-referred current noise as

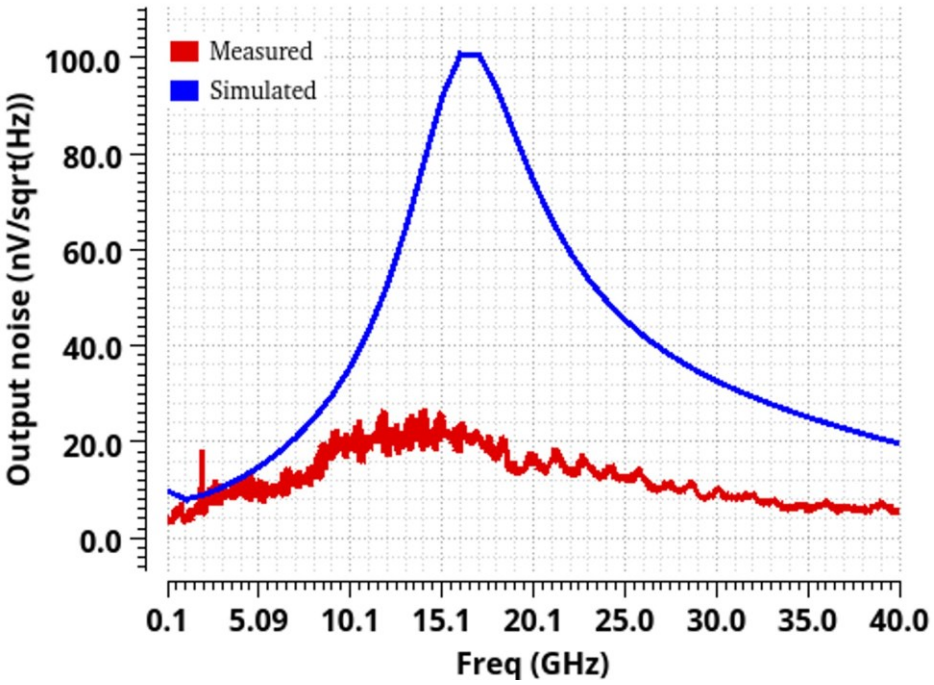


Fig. 4.16: Comparison of the measured and simulated output voltage noise spectral densities.

$$I_{n,in} = \frac{\text{Output RMS noise}}{\text{Transimpedance gain}} = \frac{2\sqrt{(1.23mV)^2 - (1.12mV)^2}}{76\ \text{dB}\Omega} = \frac{0.508mV}{76\ \text{dB}\Omega} = 0.16\ \mu\text{A} \quad (4.27)$$

Finally, the input-referred noise current spectral density is calculated as

$$S_{i,in,TI}^{1/2}(f) = \frac{I_{n,in}}{\sqrt{BW}} = \frac{0.16\ \mu\text{A}}{\sqrt{34\ GHz}} = 0.87\ pA/\sqrt{Hz} \quad (4.28)$$

Output noise voltage spectral density measured from Spectrum Analyzer after noise calibration is shown in Fig. 4.16 along with the simulated noise density. This noise density results in the measured input-referred current noise density of 0.5 pA/√Hz. The simulated average input-referred noise spectral density was 0.689 pA/√Hz.

Therefore, the noise measured via oscilloscope as well as via spectrum analyzer are closely matched with the simulated noise density. The simulated output noise spectral density is higher

than the measured density between 10 GHz to 25 GHz obtained via spectrum analyzer. This is mainly because there is less peaking in the measured transimpedance gain across this frequency range as compared to the simulated one, as is evident from Fig. 4.14. This peak reduction in the measured results is due to the bond-pad loading, the measurement setup losses and the process variations.

Finally, the measured noise from oscilloscope is slightly higher than that measured from spectrum analyzer. This is because the de-embeding of ambient noise could be achieved to a greater accuracy via spectrum analyzer as compared to that for oscilloscope. Therefore, the ambient noise is mainly causing slighlty higer noise from osccilloscope as compared to spectrum analyzer (0.87 pA/√Hz vs 0.5 pA/√Hz). However, for a fair comparison, the higher noise (0.87 pA/√Hz) will be used for comparison with the state-of-the-art.

To measure the transient behavior of the TIA, a PRBS-31 NRZ data stream was applied by using Exosight EX05608 signal generator. The experimental setup for this is shown in Fig. 4.12 (c). The TIA was used in single-ended mode for these measurements and the spare input and output were terminated to 50 Ω loads to create a 50 Ω balanced system. A series of attenuators were used to reduce the input to an equivalent current level of $100\mu A_{pp}$ ($5mV_{pp}$) amplitude to verify the sensitivity of the TIA.

Due to hardware limitation of the signal generator, its maximum data rate limit is 30 Gb/s for NRZ stream. Therefore, eye diagram could be measured only up to 30 Gb/s stream. Since the system was operating at the maximum limit of the signal generator, attenuators and DC blocks, the data available at the input of the TIA had severe high frequency attenuation. Because it is not possible to de-embed the losses due to signal generator, attenuators, DC blocks and cables, this data was supplied directly to the TIA. Even with low quality input data, wide open eye diagram is

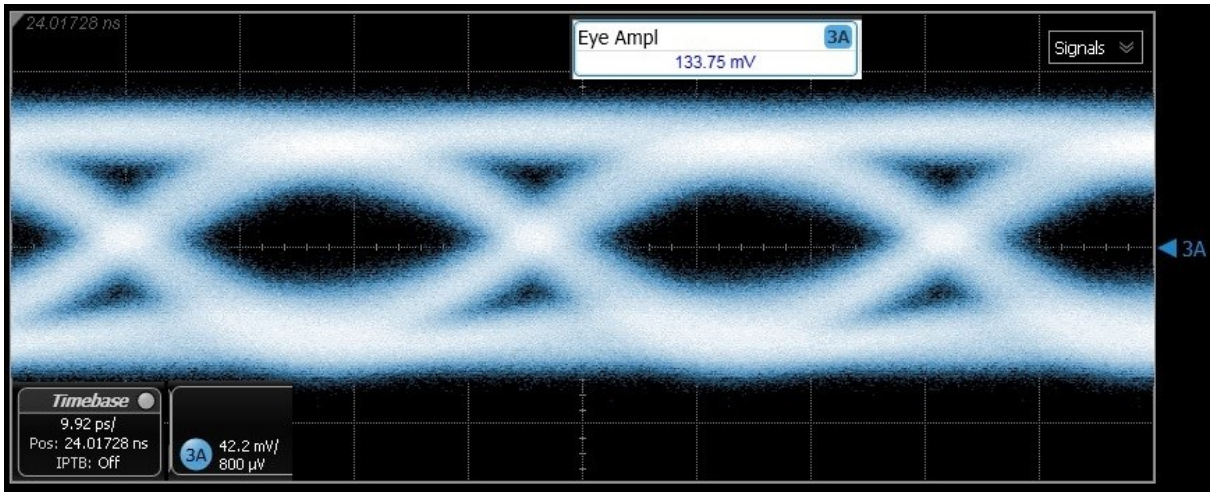


Fig. 4.17: Measured eye diagram for 30 Gb/s PRBS-31 NRZ data stream with an equivalent input current amplitude of $100\mu A_{pp}$ in single-ended operation mode.

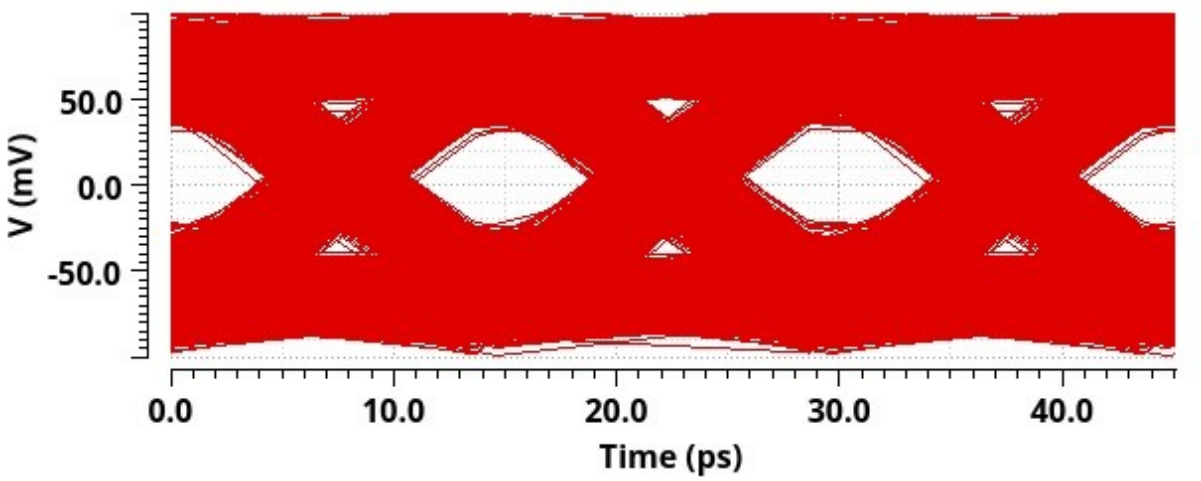


Fig. 4.18: Eye diagram extracted from measured S-parameters for 67 Gb/s PRBS-31 NRZ data stream with an equivalent input current amplitude of $100\mu A_{pp}$ in single-ended operation mode.

achieved at the output of the TIA as shown in Fig. 4.17 with a peak-to-peak eye amplitude of $133mV_{pp}$.

However, as it obvious from Fig. 4.14, the measured 3dB bandwidth is 34 GHz. This indicates that the TIA should be able to support up to a mximum of 68 Gb/s NRZ data stream. To

demonstrate this, eye diagrams were extracted from measured S-paramaters by simulating the application of 67 Gb/s PRBS-31 NRZ data stream to measured S-parameters as a 2-port network. This eye diagram is shown in Fig. 4.18 which shows that a wide $55mV_{pp}$ open eye is obtained. This shows that the TIA can easily support up to 67 Gb/s data rate.

Table 4.2 compares the proposed design with other state-of-the-art TIAs. It is obvious that the proposed design outperforms other TIA designs in most of the critical parameters while achieving the lowest input-referred noise.

4.6 Summary

This chapter presented a multi-stage RC compensation technique for application in a transimpedance amplifier that decouples its bandwidth from its low frequency transimpedance gain. This further allows for the simultaneous optimization of low frequency transimpedance gain, bandwidth and noise properties.

Experimental results suggests that the proposed technique achieves a transimpedance level which is higher than that of the conventional limit without the use of any inductors in the transimpedance stage.

This design was fabricated in a 90 nm BiCMOS process from Global Foundries (GF-9HP). To the best of the authors' knowledge, the proposed experimental prototype has the lowest input-referred noise current spectral density and highest value of transimpedance gain for an overall bandwidth of 34 GHz.

TABLE 4.2

PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART TIAS

Reference /Year	**Process**	**f_T (GHz)**	**C_{PD} (fF)**	**BW (GHz)**	**TI gain (dBΩ)**	**Noise (pA/√Hz)**	**DC Power (mW)**
[19]/2014	65nm CMOS	NA	160	18	83	15.3	93
[20]/2014	65nm CMOS	NA	NA	21.4	76.8	17.8	137.5
[21]/2016	250nm BiCMOS	110	NA	32	52.5	13.1	70
[22]/2013	130nm BiCMOS	NA	65	23	76.5	15.8	68
[23]/2014	65nm CMOS	NA	NA	24	42	16	3
[24]/2016	130nm BiCMOS	NA	NA	34	77	20	285
[25]/2016	130nm BiCMOS	NA	NA	38.4	72	14.8	261
[26]/2010	250nm BiCMOS	180	100	37.6	75.5	20	150
[27]/2012	250nm BiCMOS	180	100	20.5	70.8	18	57
[28]/2004	InGAAs-InP	160	NA	47	56	35	484
[29]/2019	SiGe 130nm	NA	NA	27	73	20	313
This work /2022	90nm BiCMOS	310	NA	34	76	0.87	100

5 An Area Efficient and Inductorless Implementation of CTLE Scheme for High Speed and Low Noise TIA Designs

This chapter presents an area efficient approach to design high speed TIA circuits. In contrast to a conventional inductor based implementation of CTLE, an inductorless gain amplifier cascade and output buffer is proposed in this work to reduce the silicon footprint. This design is first of its kind for beyond 100 Gb/s applications in the sense that it does not require any area consuming inductors. This design has been implemented in a 90 nm BiCMOS process from Global Foundaries. While optimizing overall area for high speed, this design achieves low input-referred noise as well. This design achieves an overall BW of 40 GHz with an average input-referred noise spectral density of 1.25 pA/√Hz and the overall transimpedance gain of 72 dBΩ. As before, all simulations include the effect of photodiode modeled as a current source with 65 fF capacitance.

As explained in section 2.4, CTLE is a useful approach for bandwidth extension in which zero(s) are introduced to achieve high frequency gain peaking. In a conventional design approach, inductors are used to implement these zero(s). This is often not a feasible option for area critical applications because inductors are area consuming devices and impose many design constraints due to increased parasitics and electromagnetic effects.

Due to their substantial area consumption and electromagnetic interference, inductive coils must be avoided in integrated circuit designs. There have been many efforts to realize the effect of inductance using active devices instead of passive coils, but such solutions suffer from increased noise due to active devices and higher power consumption [30]-[31].

The proposed design uses a cascade architecture for the gain amplifier (GA) in which transmission zero(s) are implemented by passive elements only (resistances and capacitances). While providing high-frequency-gain peaking, this architecture increases the overall transimpedance and provides more control over frequency response smoothening to reduce the group delay variations.

This chapter will also compare the proposed approach with the conventional CTLE approach that uses an inductor-based implementation. The comparison suggests that the proposed CTLE not only achieves the same equalized bandwidth but also results in less group delay variations as compared to its inductor-based counterpart.

5.1 Proposed Implementation of Inductorless CTLE

Conventionally, CTLE is implemented using inductive peaking which involves connecting an inductor in series with the collector/drain load resistors [9], [32]-[35]. Such a configuration is shown in Fig. 5.1(a). Here C_p represents the total effective parasitic capacitance at the output node, R_{c1} is the collector resistance and L_1 is the peaking inductor. The transfer function of this system is given as

$$H_{CTLE}(s) = \frac{-G_m R_{c1}(1 + s\frac{L_1}{R_{c1}})}{s^2 C_p L_1 + sC_p R_{c1} + 1}. \tag{5.1}$$

Here the inductive peaking creates a zero at $-R_{c1}/L_1$ which introduces frequency peaking in the input-output frequency response of the CTLE.

This work proposes the use of negative feedback along with an RC compensation scheme to achieve a peaked magnitude response for realization of CTLE. The proposed configuration is shown in Fig. 5.1(b) which results in the following transfer function

$$H_{CTLE}(s) = \frac{-R_{c1}(G_m R_{cc1} - 1)(1 + sC_{cc2}R_{cc2})}{\beta_2 s^2 + \beta_1 s + \beta_o}. \tag{5.2}$$

Here,

$$\beta_2 = C_{cc2}C_p R_{c1}R_{cc1}R_{cc2},$$

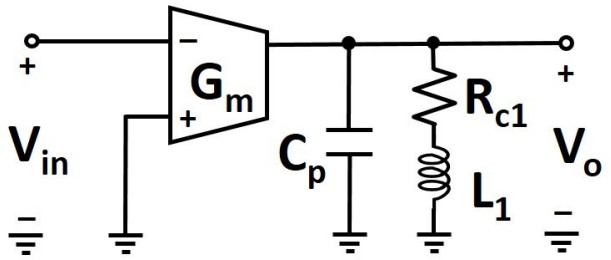
$$\beta_1 = C_{cc2}R_{c1}R_{cc2} + C_{cc2}R_{cc1}R_{cc2} + C_p R_{c1}(R_{cc1} + R_{cc2}) \tag{5.3}$$

and

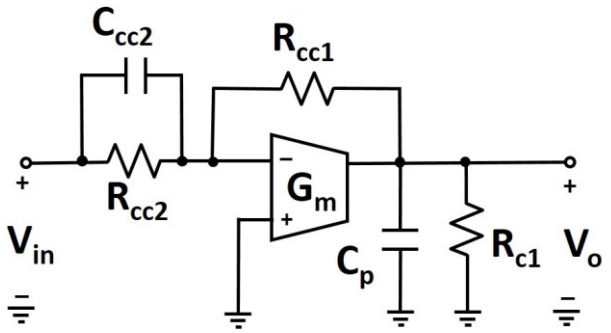
$$\beta_0 = G_m R_{c1}R_{cc2} + R_{c1} + R_{cc1} + R_{cc2}.$$

Consequently, this configuration results in a zero at $-1/R_{cc2}C_{cc2}$. Moreover, due to the use of negative feedback, the resulting system will have increased linearity and reduced sensitivity to process-voltage-temperature (PVT) variations.

Additionally, the comparison of denominators of (5.1) and (5.2) reveals that the poles are pushed to lower frequencies in the conventional approach with the use of the inductor, while the



(a)



(b)

Fig. 5.1: Small signal representations of the implementations of CTLEs. **(a)** Conventional approach. **(b)** Proposed approach with RC compensation and negative feedback.

poles in the proposed inductorless CTLE are pushed to higher frequencies due to the scaling terms introduced by C_{cc1}, R_{cc1} and R_{cc2}. Therefore, the proposed RC compensation scheme results in the frequency peaking over a relatively larger bandwidth, which is crucial to obtain overall smoother frequency response of the equalized output. Smooth frequency response of the equalized output is very important in reducing the group delay variations and consequently the ringing in the overall TIA response.

To elaborate this, consider a design example in GF BiCMOS 90 nm process in which a low frequency single-pole front-end TI stage having following transfer function precedes the conventional and proposed CTLEs

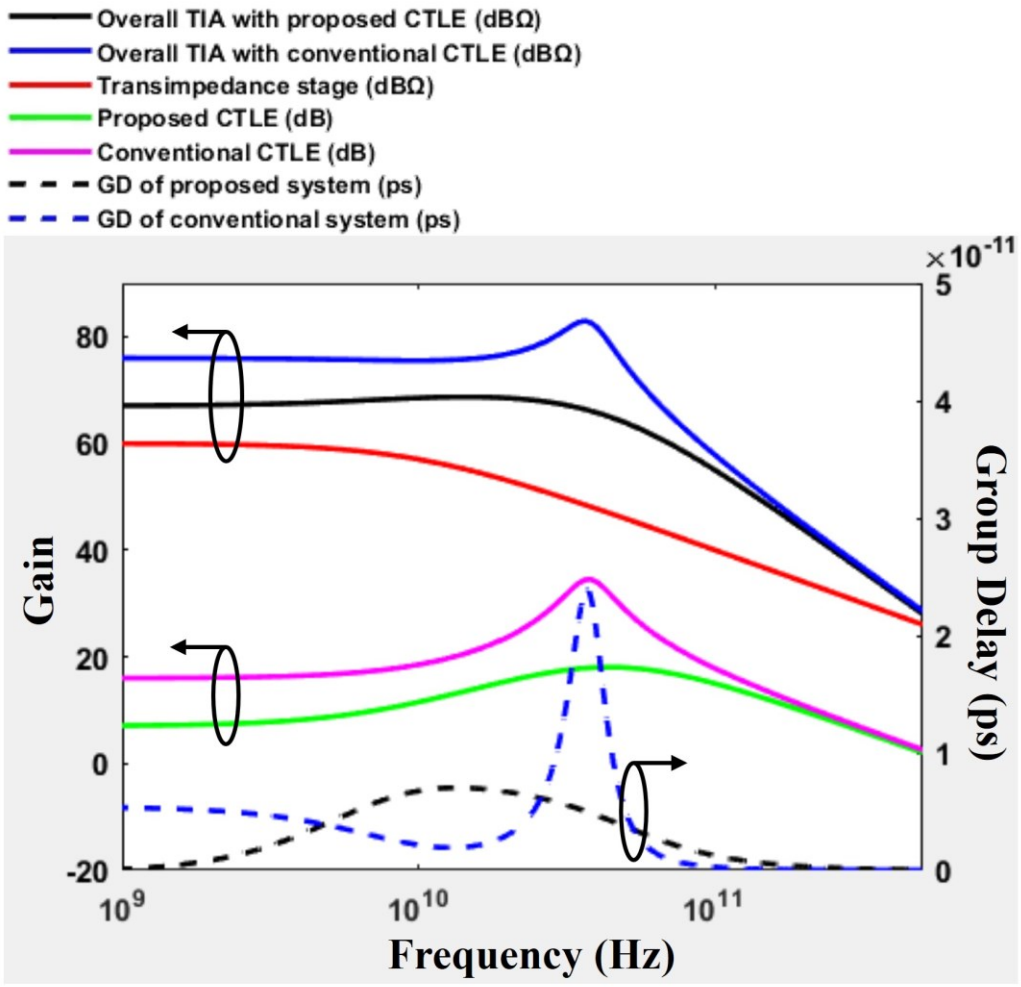


Fig. 5.2: Frequency response and group delay comparisons of the proposed and conventional CTLEs in the presence of a 60 dBΩ and 20 GHz TI front-end stage for a targeted equalized bandwidth of 50 GHz.

$$H_{TI}(s) = \frac{K}{(1 + \frac{s}{2\pi f_{TI}})}. \tag{5.4}$$

Here *K* is the low frequency transimpedance gain and f_{TI} is the location of the pole of the TI stage. In this example, K and f_{TI} are set to 60 dBΩ and 20 GHz, respectively, which are typical values that can be realized easily in the mentioned technology process. The overall transfer function is therefore given by

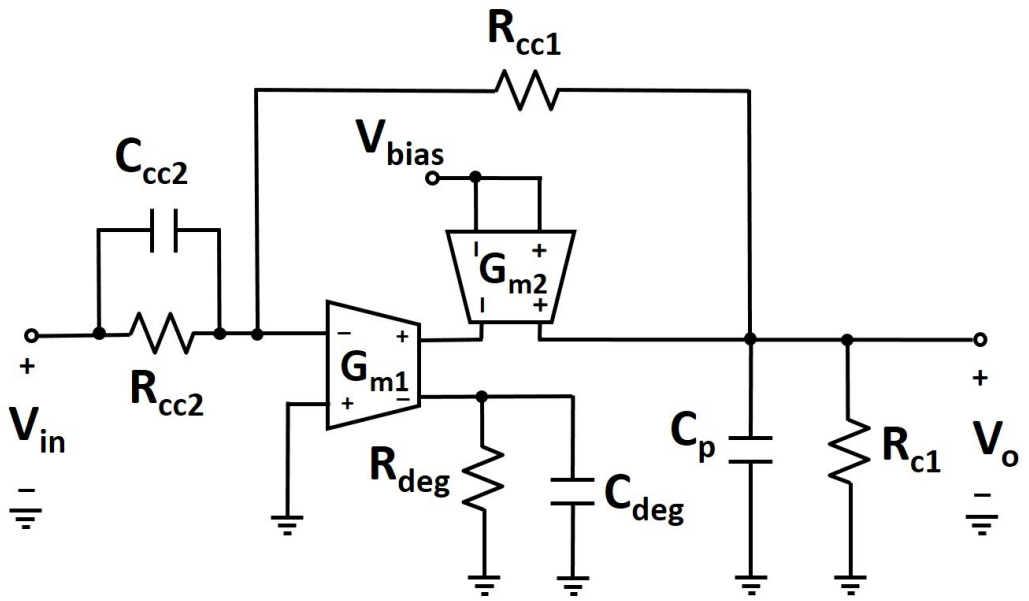


Fig. 5.3: Proposed CTLE architecture with cascode stage and capacitive degeneration to provide enhanced high frequency peaking.

$$H(s) = H_{TI}(s) \times H_{CTLE}(s). \tag{5.5}$$

$H_{CTLE}(s)$ for the cases of conventional and proposed designs are given by (5.1) and (5.2), respectively. For both designs, G_m is fixed to 125 mA/V while the C_p is set to 30 fF, which models the parasitic capacitance for GF BiCMOS 90 nm process.

To achieve an overall bandwidth of 50 GHz, the conventional CTLE approach requires a 600 pH inductor while the proposed CTLE requires R_{cc1} = 150 Ω, R_{cc2} = 45 Ω and C_{cc2} = 500 fF. Magnitude responses for each case are shown in Fig. 5.2 along with the overall equalized response in the presence of the front-end TI stage having a bandwidth of 20 GHz.

It is obvious that a 500 fF capacitance is more favorable for integrated circuits than a 600 pH inductor when the layout implementation of a capacitor is compared to that of an inductor. Moreover, due to the previously mentioned effect of C_{cc2}, R_{cc2} and R_{cc1} on the pole positioning,

the resulting overall response has much smaller group delay variations than the inductive peaking based CTLE, as shown in Fig. 5.2. Due to negative feedback structure, the closed loop gain of the proposed CTLE is slightly less than the conventional approach. However, this gain drop can be easily compensated with subsequent stages.

Additionally, the high frequency response of the CTLE can be improved by using a CE and CB cascode configuration. This is because the low input impedance of the CB configuration reduces the output resistance of G_{m1} (CE stage), hence reducing the effect of miller capacitance as explained in [17].

This configuration is shown in Fig. 5.3 using a generalized transconductance building block, G_{m2}. Capacitive degeneration is also used here which is implemented by the parallel combination of C_{deg} and R_{deg} to provide additional high frequency peaking.

5.2 Circuit Implementation of Proposed TIA

Based on the CTLE proposed in the Fig. 5.3 of Section 5.1, a TIA was designed in GF BiCMOS 90 nm process node. As before, SiGe BiCMOS technology was chosen due to high f_t (310 GHz) and low noise of the BJTs. A fully differential implementation of the proposed CTLE along with a differential amplifier-based shunt-feedback front-end TI stage is shown in Fig. 5.4. For operation in a 50 Ω matched system, the output impedance of the TIA is desired to be about 50 Ω over its entire bandwidth. To achieve this, an output buffer is designed using a common emitter differential amplifier with 50 Ω collector resistances. Capacitive degeneration is employed in CTLE and output buffer to maximize the bandwidth extension. Emitter follower stages are used as buffers and voltage level shifters between different stages.

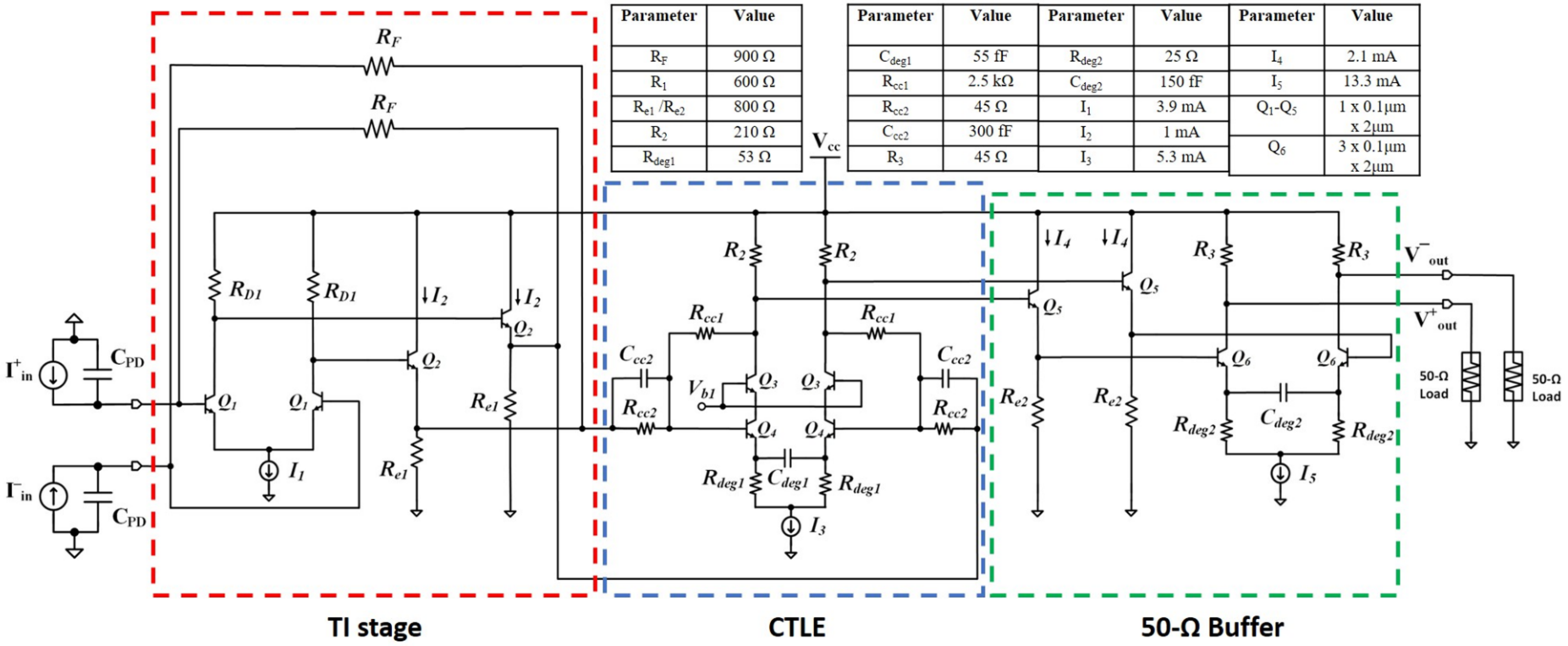
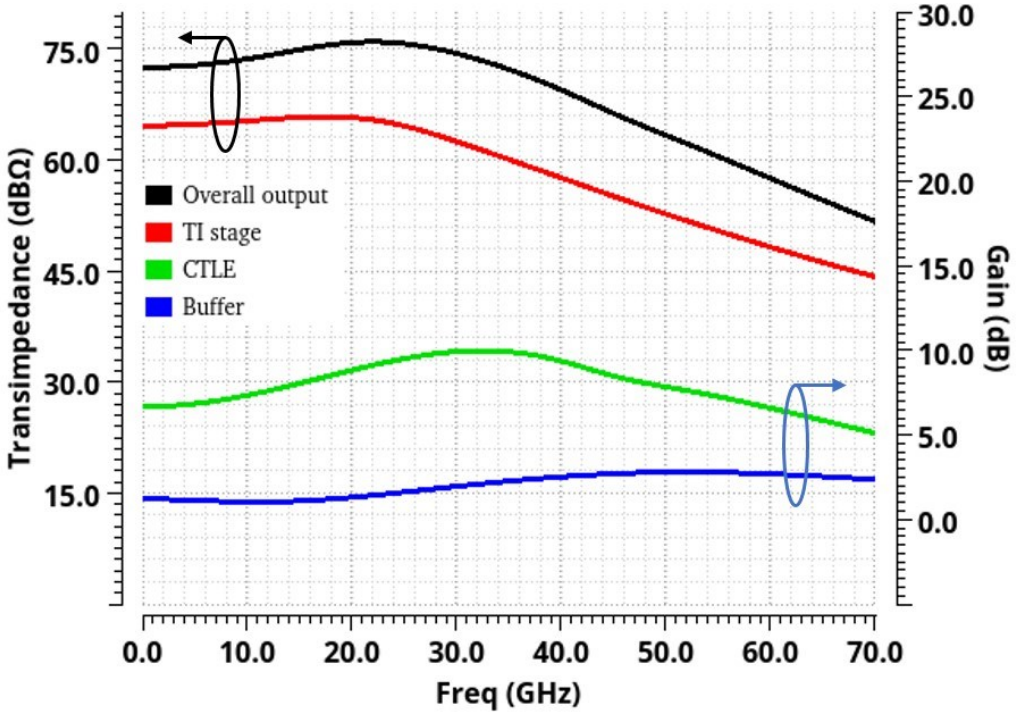
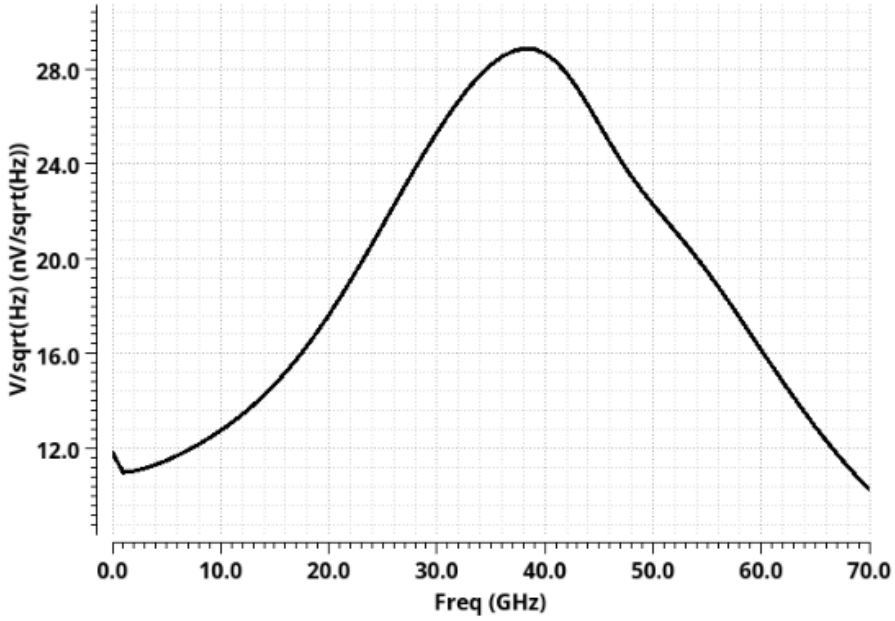


Fig. 5.4: Circuit level implementation of the fully differential and linear TIA with shunt-feedback TI stage, proposed CTLE and 50 Ω output buffer.



(a)



(b)

Fig. 5.5: Post-layout simulation results. **(a)** The stage wise magnitude response of the proposed TIA design in the presence of 65 fF photodiode capacitance. **(b)** Output noise voltage spectral density.

5.3 Post-Layout Simulation Results

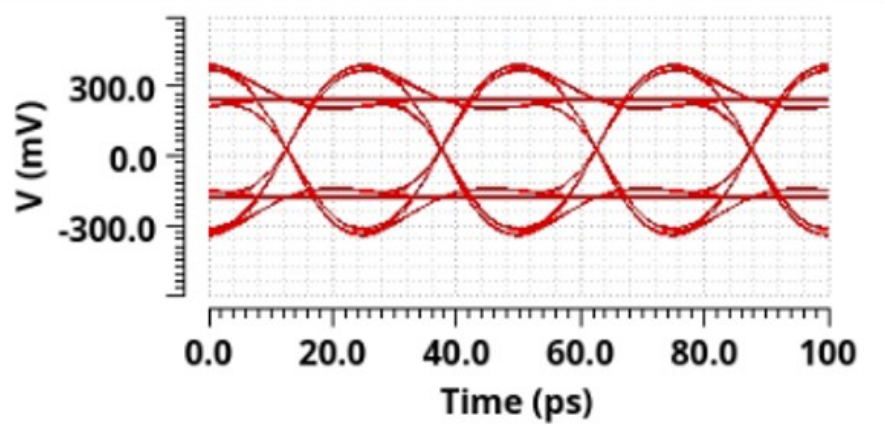
This section will present the post-layout simulations of the TIA of Fig. 5.4. Except for a noise analysis, all simulations are performed with the outputs terminated in 50 Ω loads and the inputs are loaded with 65 fF photodiode capacitance. The magnitude response of each stage are shown in Fig. 5.5 (a), along with the overall equalized response.

Output noise voltage spectral density is shown in Fig. 5.5(b), which is obtained by opening the input ports and terminating one of the output ports to 50 Ω load resistance. The noise is measured on the other output, as is described in [7]-[9]. This results in an input-referred noise current spectral density of 1.25 pA/√(Hz). This low level of noise was made possible due to higher value of R_F (900 Ω). The eye diagrams for an input of 100-μA_p PRBS31 NRZ data streams are shown in Fig. 5.6.

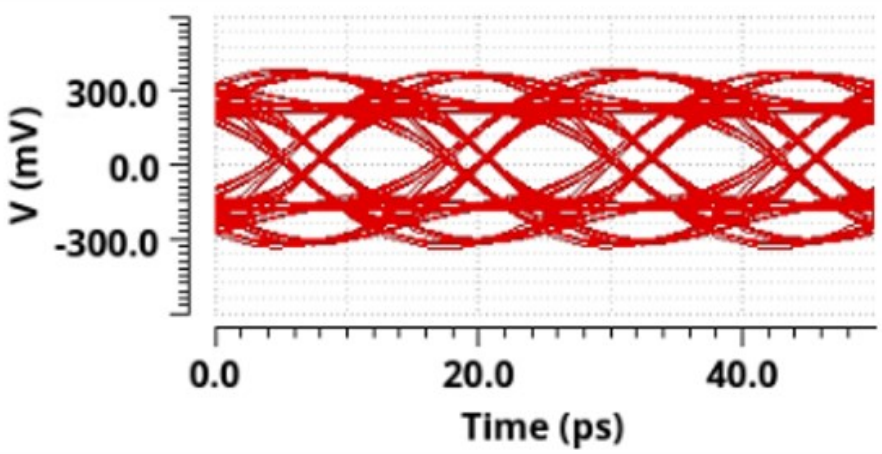
To compare the proposed design with the state-of-the-art, a figure of merit (FoM) is defined as follows

$$FoM = \frac{TI\ gain\ (dB\Omega) \times BW(GHz)}{Noise\left(\frac{pA}{\sqrt{Hz}}\right) \times Power\ (mW) \times Area(mm^2)} \tag{5.6}$$

Table 5.1 compares the proposed design with other state-of-the-art TIAs. It is obvious that the proposed design outperforms other TIA designs in most of the critical parameters. This is reflected in the comparison of the FoM as well.



(a)



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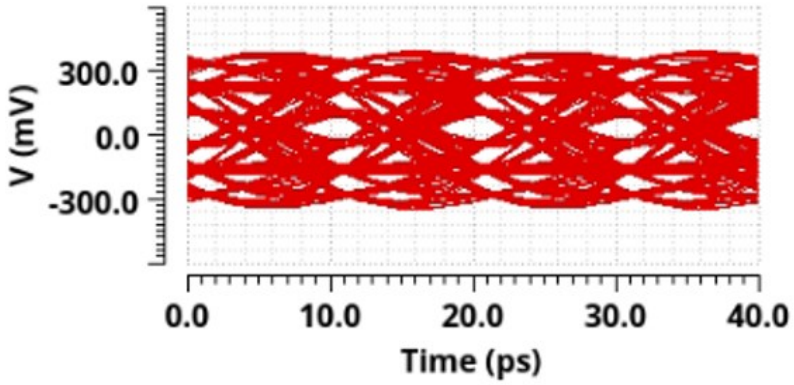

(c)

Fig. 5.6: Eye diagrams for 100- μA_p PRBS31 NRZ data streams for **(a)** 50 Gb/s, **(b)** 80 Gb/s and **(c)** 100 Gb/s.

TABLE 5.1

PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART TIAS

Reference /Year	[7] / 2017 [a]	[8] / 2021 [a]	[9] / 2021 [a]	This work/ 2022 [b]
f_T (GHz)	300	300	300	310
C_{PD} (fF)	N/A	65	65	65
BW (GHz)	66	65	76	40
TI gain (dBΩ)	66	71	70	72
Noise (pA/√Hz)	7.6	7.2	6.3	1.25
DC Power (mW)	150	345	145	130
Chip area (mm^2)	0.42	1	0.33	0.2
FoM	9.09	1.86	17.64	88

[a.] Measured results. [b.] Post-layout simulation results including photodiode and output loading effects.

5.4 Summary

This chapter proposed an inductorless implementation of CTLE for bandwidth equalization to simultaneously optimize the bandwidth and noise of TIAs. Based on the proposed CTLE, a fully differential and linear design of TIA was presented and verified by the post-layout simulations. The proposed CTLE can be used as a building block for the design of even higher BW TIAs. In future, the proposed design will be fabricated in GF BiCMOS 90 nm process for experimental verification.

6 Conclusion

This thesis began with a discussion of applications of high speed and low noise TIAs in optical receivers and SerDes. Then a detailed analysis of typical TI stage implementations was presented in terms of key performance parameters such as gain, bandwidth and input-referred noise. Further, noise analysis of multi-stage TIAs was presented. Based on these analyses, shunt-feedback TI architecture was selected to be used for implementation in the proposed designs of this work due to its low input-referred noise as compared to its counterparts. Then, noise-bandwidth trade-off in shunt-feedback TIAs was presented and the concept of CTLE was introduced for simultaneous optimization of noise and bandwidth. Furthermore, a detailed critical analysis of recent state-of-the-art TIA designs was presented.

In chapter 3, the concept of TI limit was revisited and a feedback inductive peaking technique was proposed to increase the TI limit of shunt-feedback TI stage. A CTLE-based fully-differential TIA was then designed based on the proposed technique and due consideration was given to minimize the overall group delay variations so that the ringing could be avoided in pulse response. This TIA was targeted to support beyond 100 Gb/s NRZ data streams.

In chapter 4, a multi-stage RC compensation technique was proposed to decouple the transimpedance and bandwidth of the shunt-feedback TI stage. A TIA was then designed based on this technique which was fabricated in BiCMOS 90nm (f_t = 310GHz) process for experimental validation. The comparison of measured results with recent designs indicate that this design

achieves the lowest input-referred noise ever reported (0.87 pA/√Hz) for a bandwidth of 34 GHz and transimpedance gain of 76 dBΩ.

While chapter 3 and chapter 4 mainly focused on performance enhancements of TI stage, chapter 5 focused on the improvements in the implementation of CTLE scheme. In this chapter, an area-efficient and inductorless implementation scheme was presented for CTLE. A fully-differential TIA design was then presented using the proposed CTLE and conventional single-stage shunt-feedback TI stage. Comparison of post-layout simulation results with recent designs available in literature indicates that this design is first of its kind that it can support beyond 100 Gb/s NRZ data stream without the use of inductors in any stage of the TIA. This shows that this design can be very useful in area-critical SerDes applications.

In future, the TIA design presented in chapter 5 will be fabricated in 90nm process for experimental validation. Additionally, another TIA will be designed based on the TI stage proposed in chapter 4 and the CTLE proposed in chapter 5 so that a totally inductorless low noise TIA can be designed for high speed and area-critical applications without compromising bandwidth and transimpedance gain.

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1. Fig. 2.2 has been adapted from [2] and [3].
2. Fig. 2.4 has been adapted from [10].
3. Fig. 2.5 has been adapted from [11].
4. Fig. 2.6 has been adapted from [12].
5. Fig. 2.7 has been adapted from [4].
6. The work presented in chapter 3 has been published in [36] in which Muhammad Bilal Babar (the student himself) is the main author.